C28SOI_IO_EXT_ALLF_CORESUPPLY_EG User's manual

1.0 V / 1.8 V / 3.3 V dedicated supply IO library designed in 28 nm FDSOI technology

Overview

The C28SOI_IO_ALLF_CORESUPPLY_EG library provides ESD core clamp and dedicated core supply cells.

Features

- Uses the standard process option and 28 Å gate oxide.
- Supports CSF and 3V3SF frames.
- Supports single and double rows configuration for an IO ring[1].
- FC (Flip-chip) and CL (Cluster) frames provided.

Applications

- Used as dedicated 1.0V, 1.8V and 3.3V supply cells with ESD protection.

Information Snapshot

Process Options

- GO1: SVT
- GO2: 28 Å

Packaging

- Flip-chip

1 . Single row configuration is also called as linear configuration.

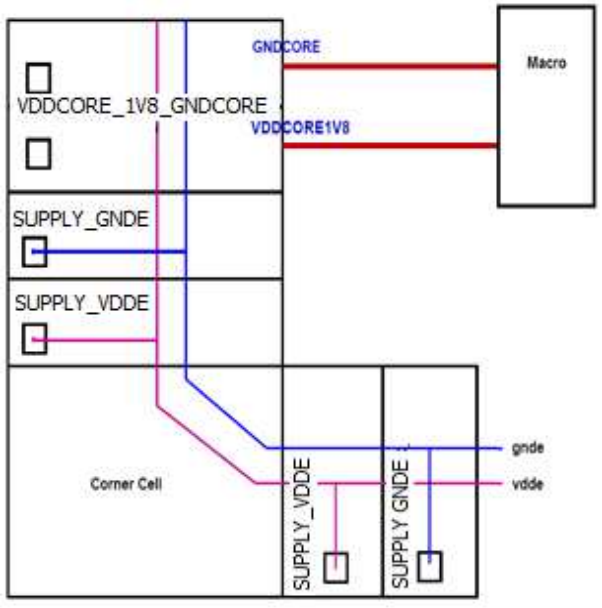
Table 1 : Operating values

Symbol	Parameter	Min	Typ	Max	Unit
vdd/ vddcore1v0	Supply voltage for 1.0 V node	*	1.0	1.1	V
vddcore1v8	Supply voltage for 1.8 V node	*	1.8	1.95	V
vddcore3v3	Supply voltage for 3.3 V node	*	3.3	3.6	V
vdde	Supply voltage for 1.8 V IO ring	*	1.8	1.95	V
	Supply voltage for 3.3 V IO ring	*	3.3	3.6	V
$T_{junction}$	Operating junction temperature	- 40	25	125	°C

* As per design Platform specification

For more details about electrical specifications, please refer to *Section 3: Electrical Specifications*.

Figure 1 : Example of dedicated supplies usage



1. Quick References

	*The document uses the following convention to indicate logic levels:* *L indicates logic low.* *H indicates logic high.* *X indicates don't care state.* *Z indicates high impedance state.* *'-' (Hyphen) indicates 'No activity'.*

	** suffixed in library name indicates multiple metallization options.* *** suffixed in cell name indicates multiple packages / configurations.*

1.1 Metal Stacking Convention

The metallization option supported by this library can be referred from its product package. The following is the convention that can be used to decode the segment in the library name:

- 7 metal option (5U1X2T8XLB) known as 5002 refers as follows:
  - 5U1X refers to the first 5 levels with 1X pitch (thin) metal.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 8 metal option (6U1X2T8XLB) known as 6002 refers as follows:
  - 6U1X refers to the first 6 levels with 1X pitch (thin) metal in ultra-low-K.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 10 metal option (6U1X2U2X2T8XLB) known as 6202 refers as follows:
  - 6U1X refers to the first 6 levels with 1x pitch (thin) metal in ultra-low-K.
  - 2U2X refers to the next 2 levels with 2x pitch (thin) metal in ultra-low-K.
  - 2T8X refers to 2 levels with 8x (thick) metal in oxide.
  - LB is the Alucap.

1.2 Reference Documentation

For details on the following topics:

- Power Sequencing Recommendation in IOs
- Specifications and Analysis of Overshoots and Undershoots
- SSN Application Notes
- ESD qualification
- Latch-up qualification
- Maturity information
- RDL recommended rules
  - ST users, refer to the IO Reference catalog

    (http://ccds.st.com/cps/sections/library/io/io_reference_catalog/downloadFile/file/IO_Helpdesk_Solutions.pdf).
  - Non-ST users, contact Customer Support personnel

1.3 Reference Library

The C28SOI_IO_EXT_ALLF_CORESUPPLY_EG library refers to some cells from 28nm FDSOI libraries listed below. For a correct usage, these libraries are mandatory:

- C28SOI_IO_ALLF_FRAMEKIT_EG
- C28SOI_IO_ALLF_IOSUPPLYKIT_EG

1.4 Acronyms and Abbreviations Used

Table 2 : Acronyms and Abbreviation

Acronym/Abbreviation	Description
B2B	Back-to-Back
CDM	Charge Device Model
DC	Direct Current
DRM	Design Rule Manual
ESD	Electrostatic Discharge
HBM	Human Body Model
FC	Flip-chip
CL	Cluster
MM	Machine Model
RMS	Root Mean Square
SVT	Standard V_T
2ROWS	Two rows

2. Functional Specifications

The C28SOI_IO_EXT_ALLF_CORESUPPLY_EG library includes 65 cells.

Table 3 : Cell List

Cell Name	Width x Height (µm)	Cell Description
Core cells		
ESDCLAMP_1V0_45U_130U_EXT	130 x 45	Core cell including 1.0 V ESD clamp
ESDCLAMP_1V0_EXT	73 x 79	Core cell including 1.0 V ESD clamp
ESDCLAMP_1V8_EXT	73 x 79	Core cell including 1.8 V ESD clamp
ESDCLAMP_3V3_EXT	103 x 78	Core cell including 3.3 V ESD clamp
CORECELL_B2B_EXT	21.1 x 19.7	Core cell including B2B diodes
CSF frame, FC view, linear placement		
GNDCORE_EXT_CSF_FC_LIN	20 x 90.8	Dedicated core ground supply cell
VDDCORE_1V0_GNDCORE_EXT_CSF_FC_LIN	70 x 90.8	Dedicated 1.0V power supply referring to a dedicated ground node
VDDCORE_1V0_GNDE_EXT_CSF_FC_LIN	70 x 90.8	Dedicated 1.0V power supply referring to gnde ground node
VDDCORE_1V0_GND_EXT_CSF_FC_LIN	70 x 90.8	Dedicated 1.0V power supply referring to gnd ground node
VDDCORE_1V8_GNDCORE_EXT_CSF_FC_LIN	70 x 90.8	Dedicated 1.8V power supply referring to a dedicated ground node
VDDCORE_1V8_GNDE_EXT_CSF_FC_LIN	70 x 90.8	Dedicated 1.8V power supply referring to gnde ground node
VDDCORE_1V8_GND_EXT_CSF_FC_LIN	70 x 90.8	Dedicated 1.8V power supply referring to gnd ground node
VDDCORE_3V3_GNDCORE_EXT_CSF_FC_LIN	100 x 90.8	Dedicated 3.3V power supply referring to a dedicated ground node
VDDCORE_3V3_GNDE_EXT_CSF_FC_LIN	100 x 90.8	Dedicated 3.3V power supply referring to gnde ground node
VDDCORE_3V3_GND_EXT_CSF_FC_LIN	100 x 90.8	Dedicated 3.3V power supply referring to gnd ground node
CSF frame, FC view, 2rows placement		
GNDCORE_EXT_CSF_FC_INNER	40 x 90.8	Dedicated core ground supply cell
VDDCORE_1V0_GNDCORE_EXT_CSF_FC_INNER	70 x 90.8	Dedicated 1.0V power supply referring to a dedicated ground node
VDDCORE_1V0_GNDE_EXT_CSF_FC_INNER	70 x 90.8	Dedicated 1.0V power supply referring to gnde ground node
VDDCORE_1V0_GND_EXT_CSF_FC_INNER	70 x 90.8	Dedicated 1.0V power supply referring to gnd ground node

Table 3 : Cell List

Cell Name	Width x Height (µm)	Cell Description
VDDCORE_1V8_GNDCORE_EXT_CSF_FC_INNER	70 x 90.8	Dedicated 1.8V power supply referring to a dedicated ground node
VDDCORE_1V8_GNDE_EXT_CSF_FC_INNER	70 x 90.8	Dedicated 1.8V power supply referring to gnde ground node
VDDCORE_1V8_GND_EXT_CSF_FC_INNER	70 x 90.8	Dedicated 1.8V power supply referring to gnd ground node
VDDCORE_3V3_GNDCORE_EXT_CSF_FC_INNER	100 x 90.8	Dedicated 3.3V power supply referring to a dedicated ground node
VDDCORE_3V3_GNDE_EXT_CSF_FC_INNER	100 x 90.8	Dedicated 3.3V power supply referring to gnde ground node
VDDCORE_3V3_GND_EXT_CSF_FC_INNER	100 x 90.8	Dedicated 3.3V power supply referring to gnd ground node
CSF frame, CL view, cluster placement		
GNDCORE_EXT_CSF_CL_LIN	20 x 106.3	Dedicated core ground supply cell
VDDCORE_1V0_GNDCORE_EXT_CSF_CL_LIN	70 x 106.3	Dedicated 1.0V power supply referring to a dedicated ground node
VDDCORE_1V0_GNDE_EXT_CSF_CL_LIN	70 x 106.3	Dedicated 1.0V power supply referring to gnde ground node
VDDCORE_1V0_GND_EXT_CSF_CL_LIN	70 x 106.3	Dedicated 1.0V power supply referring to gnd ground node
VDDCORE_1V8_GNDCORE_EXT_CSF_CL_LIN	70 x 106.3	Dedicated 1.8V power supply referring to a dedicated ground node
VDDCORE_1V8_GNDE_EXT_CSF_CL_LIN	70 x 90.8	Dedicated 1.8V power supply referring to gnde ground node
VDDCORE_1V8_GND_EXT_CSF_CL_LIN	70 x 90.8	Dedicated 1.8V power supply referring to gnd ground node
VDDCORE_3V3_GNDCORE_EXT_CSF_CL_LIN	100 x 106.3	Dedicated 3.3V power supply referring to a dedicated ground node
VDDCORE_3V3_GNDE_EXT_CSF_CL_LIN	100 x 90.8	Dedicated 3.3V power supply referring to gnde ground node
VDDCORE_3V3_GND_EXT_CSF_CL_LIN	100 x 90.8	Dedicated 3.3V power supply referring to gnd ground node
3V3SF frame, FC view, linear placement		
GNDCORE_EXT_3V3SF_FC_LIN	20 x 90.8	Dedicated core ground supply cell
VDDCORE_1V0_GNDCORE_EXT_3V3SF_FC_LIN	70 x 90.8	Dedicated 1.0V power supply referring to a dedicated ground node
VDDCORE_1V0_GNDE_EXT_3V3SF_FC_LIN	70 x 90.8	Dedicated 1.0V power supply referring to gnde ground node
VDDCORE_1V0_GND_EXT_3V3SF_FC_LIN	70 x 90.8	Dedicated 1.0V power supply referring to gnd ground node
VDDCORE_1V8_GNDCORE_EXT_3V3SF_FC_LIN	70 x 90.8	Dedicated 1.8V power supply referring to a dedicated ground node
VDDCORE_1V8_GNDE_EXT_3V3SF_FC_LIN	70 x 90.8	Dedicated 1.8V power supply referring to gnde ground node

Table 3 : Cell List

Cell Name	Width x Height (µm)	Cell Description
VDDCORE_1V8_GND_EXT_3V3SF_FC_LIN	70 x 90.8	Dedicated 1.8V power supply referring to gnd ground node
VDDCORE_3V3_GNDCORE_EXT_3V3SF_FC_LIN	100 x 90.8	Dedicated 3.3V power supply referring to a dedicated ground node
VDDCORE_3V3_GNDE_EXT_3V3SF_FC_LIN	100 x 90.8	Dedicated 3.3V power supply referring to gnde ground node
VDDCORE_3V3_GND_EXT_3V3SF_FC_LIN	100 x 90.8	Dedicated 3.3V power supply referring to gnd ground node
3V3SF frame, FC view, 2rows placement		
GNDCORE_EXT_3V3SF_FC_INNER	20 x 90.8	Dedicated core ground supply cell
VDDCORE_1V0_GNDCORE_EXT_3V3SF_FC_INNER	70 x 90.8	Dedicated 1.0V power supply referring to a dedicated ground node
VDDCORE_1V0_GNDE_EXT_3V3SF_FC_INNER	70 x 90.8	Dedicated 1.0V power supply referring to gnde ground node
VDDCORE_1V0_GND_EXT_3V3SF_FC_INNER	70 x 90.8	Dedicated 1.0V power supply referring to gnd ground node
VDDCORE_1V8_GNDCORE_EXT_3V3SF_FC_INNER	70 x 90.8	Dedicated 1.8V power supply referring to a dedicated ground node
VDDCORE_1V8_GNDE_EXT_3V3SF_FC_INNER	70 x 90.8	Dedicated 1.8V power supply referring to gnde ground node
VDDCORE_1V8_GND_EXT_3V3SF_FC_INNER	70 x 90.8	Dedicated 1.8V power supply referring to gnd ground node
VDDCORE_3V3_GNDCORE_EXT_3V3SF_FC_INNER	100 x 90.8	Dedicated 3.3V power supply referring to a dedicated ground node
VDDCORE_3V3_GNDE_EXT_3V3SF_FC_INNER	100 x 90.8	Dedicated 3.3V power supply referring to gnde ground node
VDDCORE_3V3_GND_EXT_3V3SF_FC_INNER	100 x 90.8	Dedicated 3.3V power supply referring to gnd ground node
3V3SF frame, CL view, cluster placement		
GNDCORE_EXT_3V3SF_CL_LIN	20 x 106.3	Dedicated core ground supply cell
VDDCORE_1V0_GNDCORE_EXT_3V3SF_CL_LIN	70 x 106.3	Dedicated 1.0V power supply referring to a dedicated ground node
VDDCORE_1V0_GNDE_EXT_3V3SF_CL_LIN	70 x 106.3	Dedicated 1.0V power supply referring to gnde ground node
VDDCORE_1V0_GND_EXT_3V3SF_CL_LIN	70 x 106.3	Dedicated 1.0V power supply referring to gnd ground node
VDDCORE_1V8_GNDCORE_EXT_3V3SF_CL_LIN	70 x 106.3	Dedicated 1.8V power supply referring to a dedicated ground node
VDDCORE_1V8_GNDE_EXT_3V3SF_CL_LIN	70 x 90.8	Dedicated 1.8V power supply referring to gnde ground node
VDDCORE_1V8_GND_EXT_3V3SF_ CL_LIN	70 x 90.8	Dedicated 1.8V power supply referring to gnd ground node
VDDCORE_3V3_GNDCORE_EXT_3V3SF_CL_LIN	100 x 106.3	Dedicated 3.3V power supply referring to a dedicated ground node

Table 3 : Cell List		
Cell Name	**Width x Height (µm)**	**Cell Description**
VDDCORE_3V3_GNDE_EXT_3V3SF_ CL_LIN	100 x 90.8	Dedicated 3.3V power supply referring to gnde ground node
VDDCORE_3V3_GND_EXT_3V3SF_ CL_LIN	100 x 90.8	Dedicated 3.3V power supply referring to gnd ground node

The ALLCELLS cells are not considered part of the Deliverable. These cells are specifically for QA check and hence subject to change, without prior notice.

2.1 Lateral pins

As all CSF / 3V3SF dedicated IO supply cells share the same set of data lateral pins, these pins are described only one time in the table below .

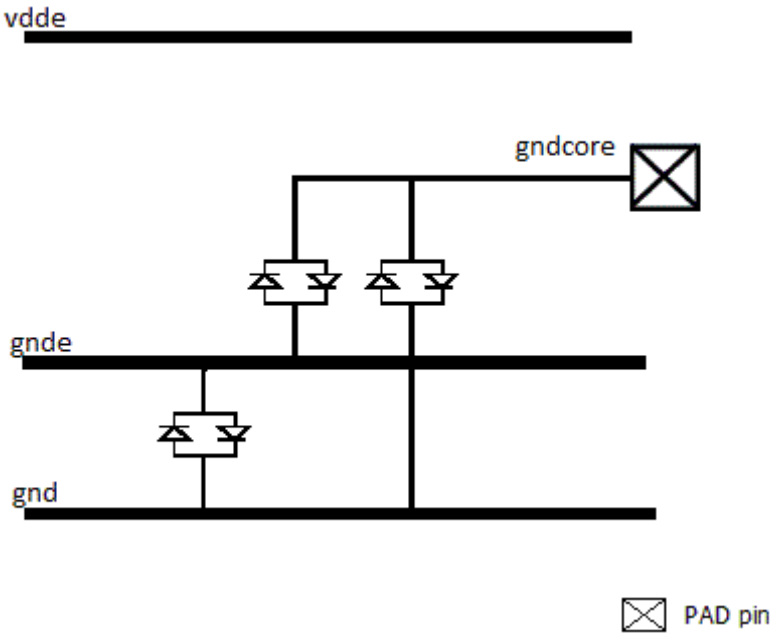
Table 4 : Track pins description

Pin	Type	Voltage Level (V)	Description
CSF FRAME			
ASRCN<0:6>	Input/Output	0 or vdde	ASRCN <0:6> signal nodes
ASRCP<0:6>	Input/Output	0 or vdde	ASRCP <0:6> signal nodes
REFIOA	Input/Output	Vref	REFIOA reference node
REFIOB	Input/Output	Vref	REFIOB reference node
3V3SF FRAME			
ASRCN3V3<4:0>	Input/Output	0 or vdde	ASRCN3V3 <4:0> signal nodes
ASRCP3V3<4:0>	Input/Output	0 or vdde	ASRCP3V3 <4:0> signal nodes
REFAPBIAS3V3	Input/Output	Vref	REFAPBIAS3V3 reference node
REFBAMPL3V3	Input/Output	Vref	REFBAMPL3V3 reference node
REFCAMPH3V3	Input/Output	Vref	REFCAMPH3V3 reference node
REFDNBIAS3V3	Input/Output	Vref	REFDNBIAS3V3 reference node
REFE3V3	Input/Output	Vref	REFE3V3 reference node
REFL3V3	Input/Output	Vref	REFL3V3 reference node
REFH3V3	Input/Output	Vref	REFH3V3 reference node

2.2 GNDCORE_EXT_CSF_FC_LIN/FC_INNER/CL_LIN

2.2.1 Functional Diagram

Figure 2 : Block diagram



2.2.2 Interface Description

Table 5 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pin			
gndcore	Input / Output	0	Dedicated ground node, pad side
Track and core pins			
gndcore	Input / Output	0	Dedicated ground node, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.2.3 Cell Information

Table 6 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vdde node)	-	-	< 150	pA
		Fast Process, Max voltage, 125 °C (vdde node)	-	-	< 150	
I_{DC}	DC current Pad To Core [1]	110 °C (gndcore node)	-	-	81	mA
		125 °C (gndcore node)	-	-	29	
	DC current Pad To Core [2]	110 °C (gndcore node)	-	-	38	
		125 °C (gndcore node)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (gndcore node)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (gndcore node)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

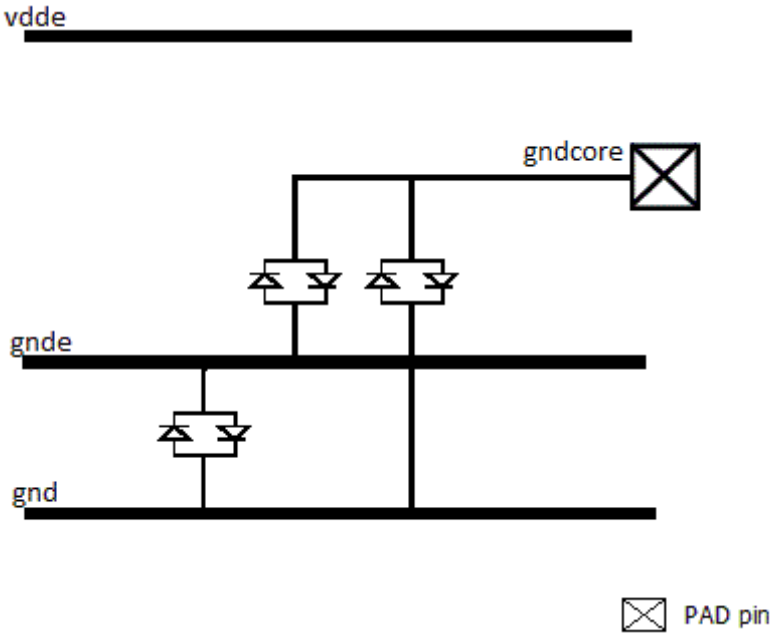
2.2.4 Functional Description

These cells are dedicated core ground CSF supplies with a core pin provided in metal top (IB).

2.3 GNDCORE_EXT_3V3SF_FC_LIN/FC_INNER/CL_LIN

2.3.1 Functional Diagram

Figure 3 : Block diagram



2.3.2 Interface Description

Table 7 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pin			
gndcore	Input / Output	0	Dedicated ground node, pad side
Track and core pins			
gndcore	Input / Output	0	Dedicated ground node, only core side
vdde	Input / Output	vdde	IO power node (3.3 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.3.3 Cell Information

Table 8 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vdde node)	-	-	< 150	pA
		Fast Process, Max voltage, 125 °C (vdde node)	-	-	< 150	
I_{DC}	DC current Pad To Core [1]	110 °C (gndcore node)	-	-	81	mA
		125 °C (gndcore node)	-	-	29	
	DC current Pad To Core [2]	110 °C (gndcore node)	-	-	38	
		125 °C (gndcore node)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (gndcore node)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (gndcore node)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

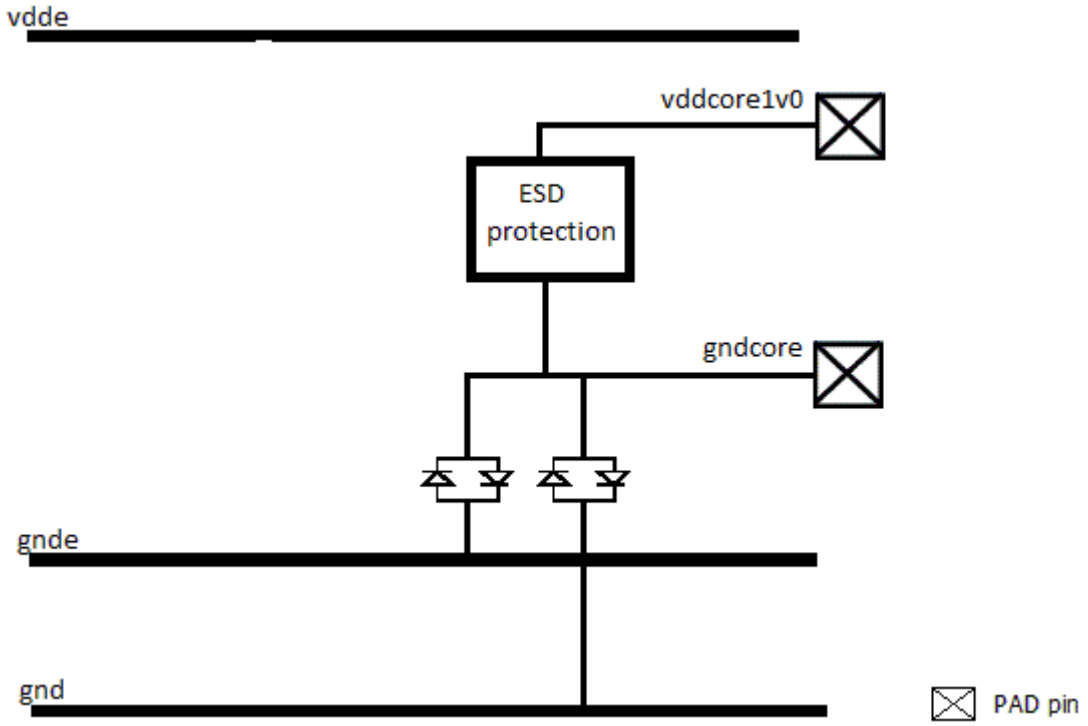
2.3.4 Functional description

These cells are dedicated core ground 3V3SF supplies with a core pin provided in metal top (IB).

2.4 VDDCORE_1V0_GNDCORE_EXT_CSF_FC_LIN/FC_INNER/CL_LIN

2.4.1 Functional Diagram

Figure 4 : Block diagram



2.4.2 Interface Description

Table 9 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, pad side
gndcore	Input / Output	0	Dedicated ground node, pad side
Track and core pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, only core side
gndcore	Input / Output	0	Dedicated ground node, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.4.3 Cell Information

Table 10 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v0 node)	-	-	64	nA
		Fast Process, Max voltage, 125 °C (vddcore1v0 node)	-	-	11	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v0 and gndcore nodes)	-	-	81	mA
		125 °C (vddcore1v0 and gndcore nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore1v0 and gndcore nodes)	-	-	38	
		125 °C (vddcore1v0 and gndcore nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore1v0 and gndcore nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (vddcore1v0 and gndcore nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

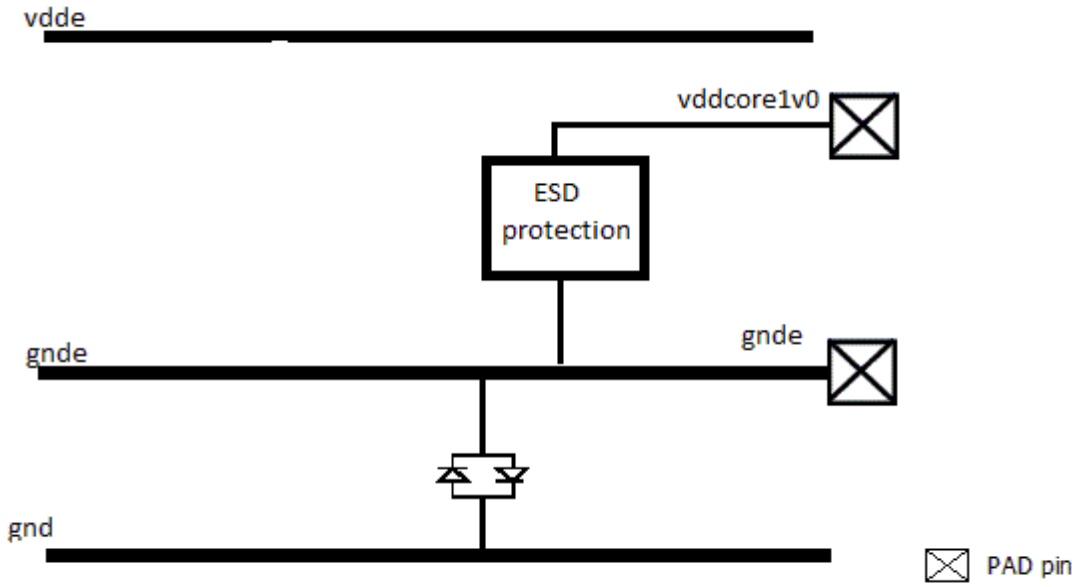
2.4.4 Functional Description

These cells represent a dedicated 1.0V CSF power supply referring to a dedicated ground node. Core pins are provided in metal top (IB).

2.5 VDDCORE_1V0_GNDE_EXT_CSF_FC_LIN/FC_INNER/CL_LIN

2.5.1 Functional Diagram

Figure 5 : Block diagram



2.5.2 Interface Description

Table 11 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, pad side
gnde	Input / Output	0	IO ground node, pad side
Track and core pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.5.3 Cell Information

Table 12 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v0 node)	-	-	64	nA
		Fast Process, Max voltage, 125 °C (vddcore1v0 node)	-	-	11	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v0 and gnde nodes)	-	-	81	mA
		125 °C (vddcore1v0 and gnde nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore1v0 and gnde nodes)	-	-	38	
		125 °C (vddcore1v0 and gnde nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore1v0 and gnde nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (vddcore1v0 and gnde nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

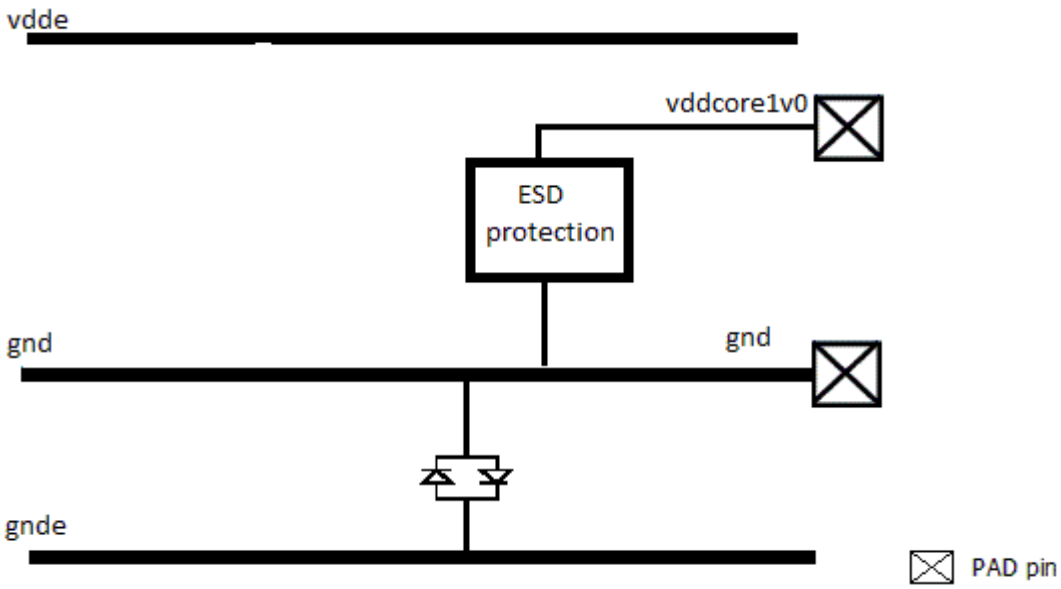
2.5.4 Functional Description

These cells represent a dedicated 1.0V CSF power supply referring to gnde ground node. Core pins are provided in metal top (IB).

2.6 VDDCORE_1V0_GND_EXT_CSF_FC_LIN/FC_INNER/CL_LIN

2.6.1 Functional Diagram

Figure 6 : Block diagram



2.6.2 Interface Description

Table 13 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, pad side
gnd	Input / Output	0	Core and substrate ground node, pad side
Track and core pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.6.3 Cell Information

Table 14 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v0 node)	-	-	64	nA
		Fast Process, Max voltage, 125 °C (vddcore1v0 node)	-	-	11	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v0 and gnd nodes)	-	-	81	mA
		125 °C (vddcore1v0 and gnd nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore1v0 and gnd nodes)	-	-	38	
		125 °C (vddcore1v0 and gnd nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore1v0 and gnd nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (vddcore1v0 and gnd nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

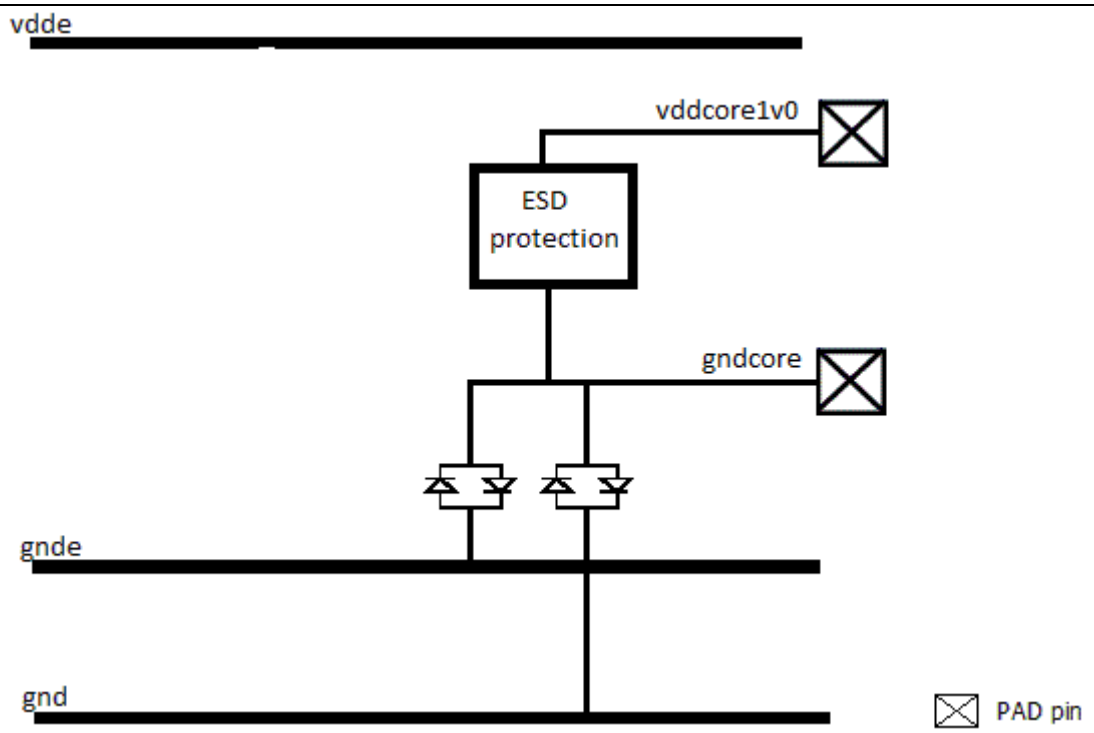
2.6.4 Functional Description

These cells represent a dedicated 1.0V CSF power supply referring to gnd ground node. Core pins are provided in metal top (IB).

2.7 VDDCORE_1V0_GNDCORE_EXT_3V3SF_FC_LIN/FC_INNER/CL_LIN

2.7.1 Functional Diagram

Figure 7 : Block diagram



2.7.2 Interface Description

Table 15 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, pad side
gndcore	Input / Output	0	Dedicated ground node, pad side
Track and core pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, only core side
gndcore	Input / Output	0	Dedicated ground node, only core side
vdde	Input / Output	vdde	IO power node (3.3 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.7.3 Cell Information

Table 16 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v0 node)	-	-	64	nA
		Fast Process, Max voltage, 125 °C (vddcore1v0 node)	-	-	11	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v0 and gndcore nodes)	-	-	81	mA
		125 °C (vddcore1v0 and gndcore nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore1v0 and gndcore nodes)	-	-	38	
		125 °C (vddcore1v0 and gndcore nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore1v0 and gndcore nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (vddcore1v0 and gndcore nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

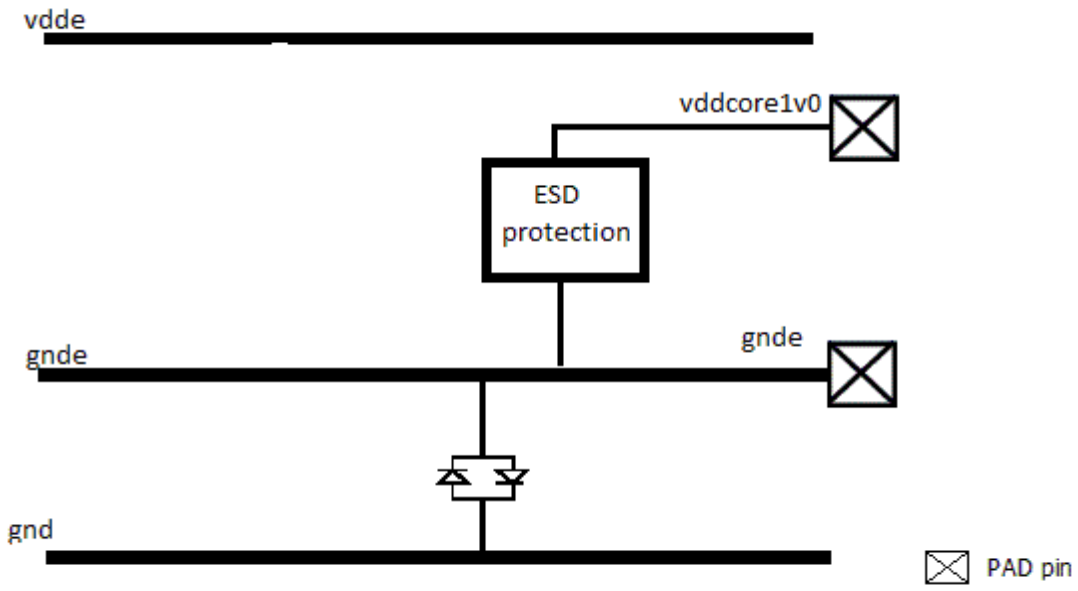
2.7.4 Functional Description

These cells represent a dedicated 1.0V 3V3SF power supply referring to a dedicated ground node. Core pins are provided in metal top (IB).

2.8 VDDCORE_1V0_GNDE_EXT_3V3SF_FC_LIN/FC_INNER/CL_LIN

2.8.1 Functional Diagram

Figure 8 : Block diagram



2.8.2 Interface Description

Table 17 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, pad side
gnde	Input / Output	0	IO ground node, pad side
Track and core pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (3.3 V), only track side
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.8.3 Cell Information

Table 18 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v0 node)	-	-	64	nA
		Fast Process, Max voltage, 125 °C (vddcore1v0 node)	-	-	11	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v0 and gnde nodes)	-	-	81	mA
		125 °C (vddcore1v0 and gnde nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore1v0 and gnde nodes)	-	-	38	
		125 °C (vddcore1v0 and gnde nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore1v0 and gnde nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (vddcore1v0 and gnde nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

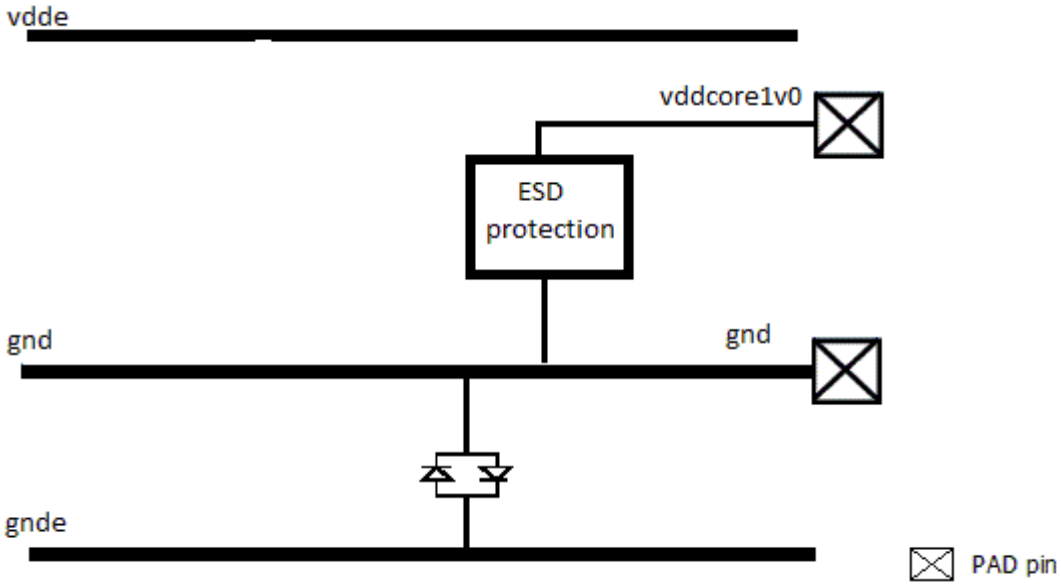
2.8.4 Functional Description

These cells represent a dedicated 1.0V 3V3SF power supply referring to gnde ground node. Core pins are provided in metal top (IB).

2.9 VDDCORE_1V0_GND_EXT_3V3SF_FC_LIN/FC_INNER/CL_LIN

2.9.1 Functional Diagram

Figure 9 : Block diagram



2.9.2 Interface Description

Table 19 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, pad side
gnd	Input / Output	0	Core and substrate ground node, pad side
Track and core pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (3.3 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.9.3 Cell Information

Table 20 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v0 node)	-	-	64	nA
		Fast Process, Max voltage, 125 °C (vddcore1v0 node)	-	-	11	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v0 and gnd nodes)	-	-	81	mA
		125 °C (vddcore1v0 and gnd nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore1v0 and gnd nodes)	-	-	38	
		125 °C (vddcore1v0 and gnd nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore1v0 and gnd nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (vddcore1v0 and gnd nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

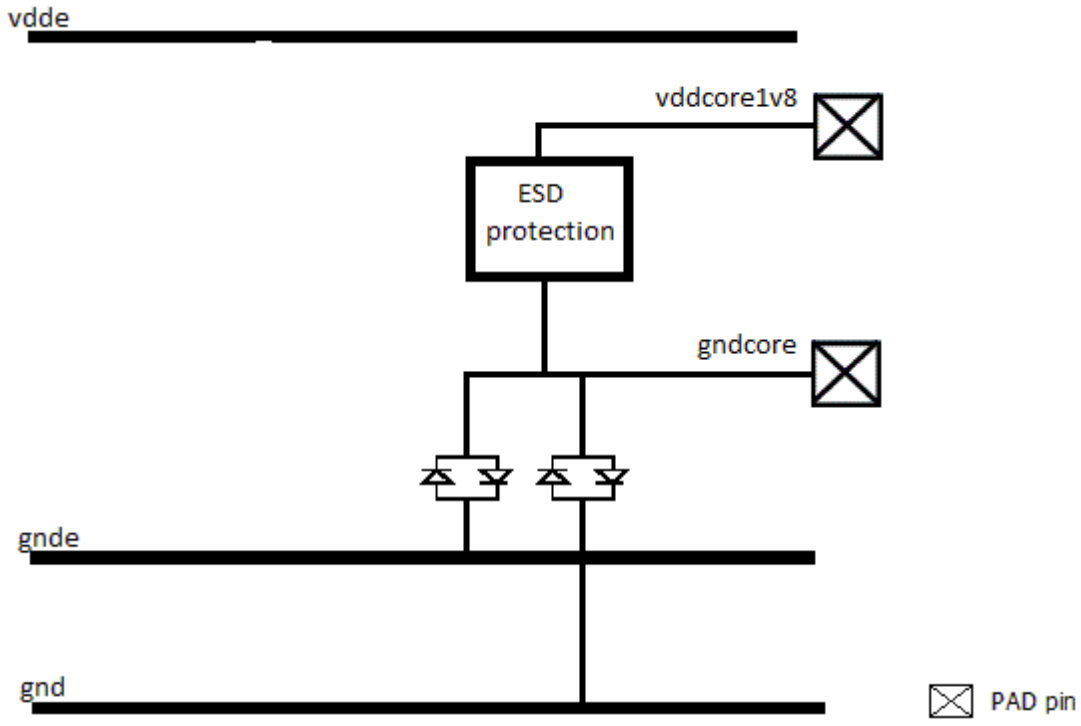
2.9.4 Functional Description

These cells represent a dedicated 1.0V 3V3SF power supply referring to gnd ground node. Core pins are provided in metal top (IB).

2.10 VDDCORE_1V8_GNDCORE_EXT_CSF_FC_LIN/FC_INNER/CL_LIN

2.10.1 Functional Diagram

Figure 10 : Block diagram



2.10.2 Interface Description

Table 21 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, pad side
gndcore	Input / Output	0	Dedicated ground node, pad side
Track and core pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, only core side
gndcore	Input / Output	0	Dedicated ground node, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.10.3 Cell Information

Table 22 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v8 node)	-	-	495	nA
		Fast Process, Max voltage, 125 °C (vddcore1v8 node)	-	-	3.8	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v8 and gndcore nodes)	-	-	81	mA
		125 °C (vddcore1v8 and gndcore nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore1v8 and gndcore nodes)	-	-	38	
		125 °C (vddcore1v8 and gndcore nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore1v8 and gndcore nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (vddcore1v8 and gndcore nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

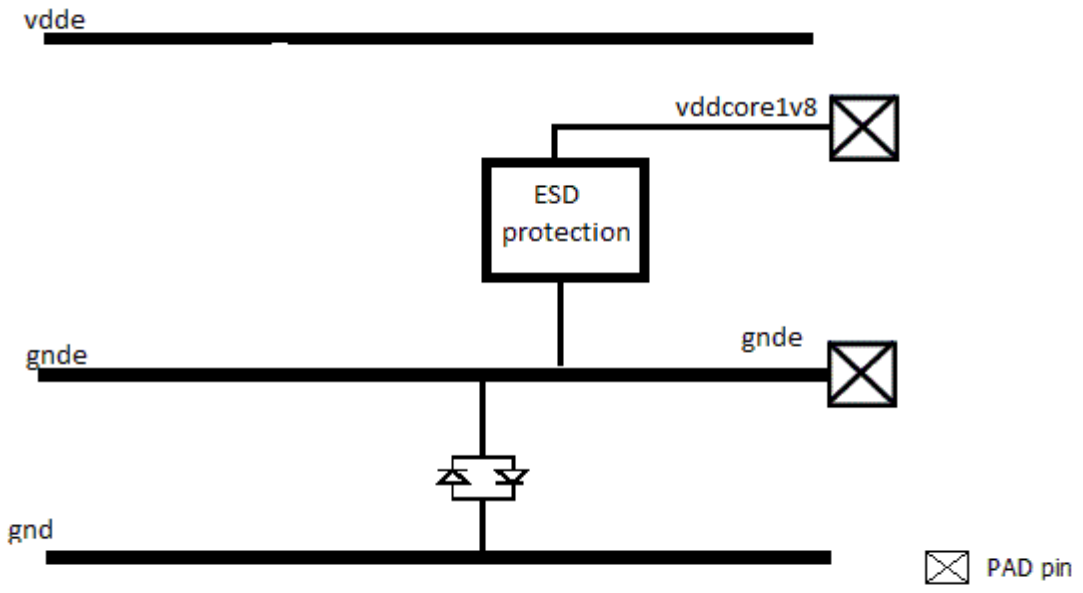
2.10.4 Functional Description

These cells represent a dedicated 1.8V CSF power supply referring to a dedicated ground node. Core pins are provided in metal top (IB).

2.11 VDDCORE_1V8_GNDE_EXT_CSF_FC_LIN/FC_INNER/CL_LIN

2.11.1 Functional Diagram

Figure 11 : Block diagram



2.11.2 Interface Description

Table 23 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, pad side
gnde	Input / Output	0	IO ground node, pad side
Track and core pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.11.3 Cell Information

Table 24 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v8 node)	-	-	495	nA
		Fast Process, Max voltage, 125 °C (vddcore1v8 node)	-	-	3.8	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v8 and gnde nodes)	-	-	81	mA
		125 °C (vddcore1v8 and gnde nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore1v8 and gnde nodes)	-	-	38	
		125 °C (vddcore1v8 and gnde nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore1v8 and gnde nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (vddcore1v8 and gnde nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

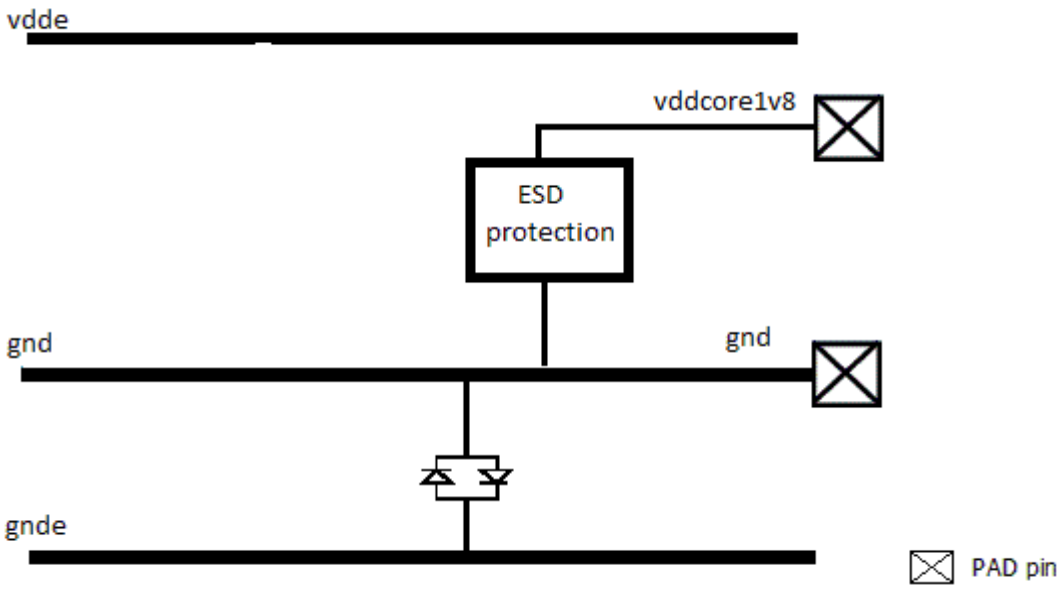
2.11.4 Functional Description

These cells represent a dedicated 1.8V CSF power supply referring to IO ground node. Core pins are provided in metal top (IB).

2.12 VDDCORE_1V8_GND_EXT_CSF_FC_LIN/FC_INNER/CL_LIN

2.12.1 Functional Diagram

Figure 12 : Block diagram



2.12.2 Interface Description

Table 25 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, pad side
gnd	Input / Output	0	Core and substrate ground node, pad side
Track and core pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.12.3 Cell Information

Table 26 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v8 node)	-	-	495	nA
		Fast Process, Max voltage, 125 °C (vddcore1v8 node)	-	-	3.8	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v8 and gnd nodes)	-	-	81	mA
		125 °C(vddcore1v8 and gnd nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C(vddcore1v8 and gnd nodes)	-	-	38	
		125 °C(vddcore1v8 and gnd nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C(vddcore1v8 and gnd nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C(vddcore1v8 and gnd nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

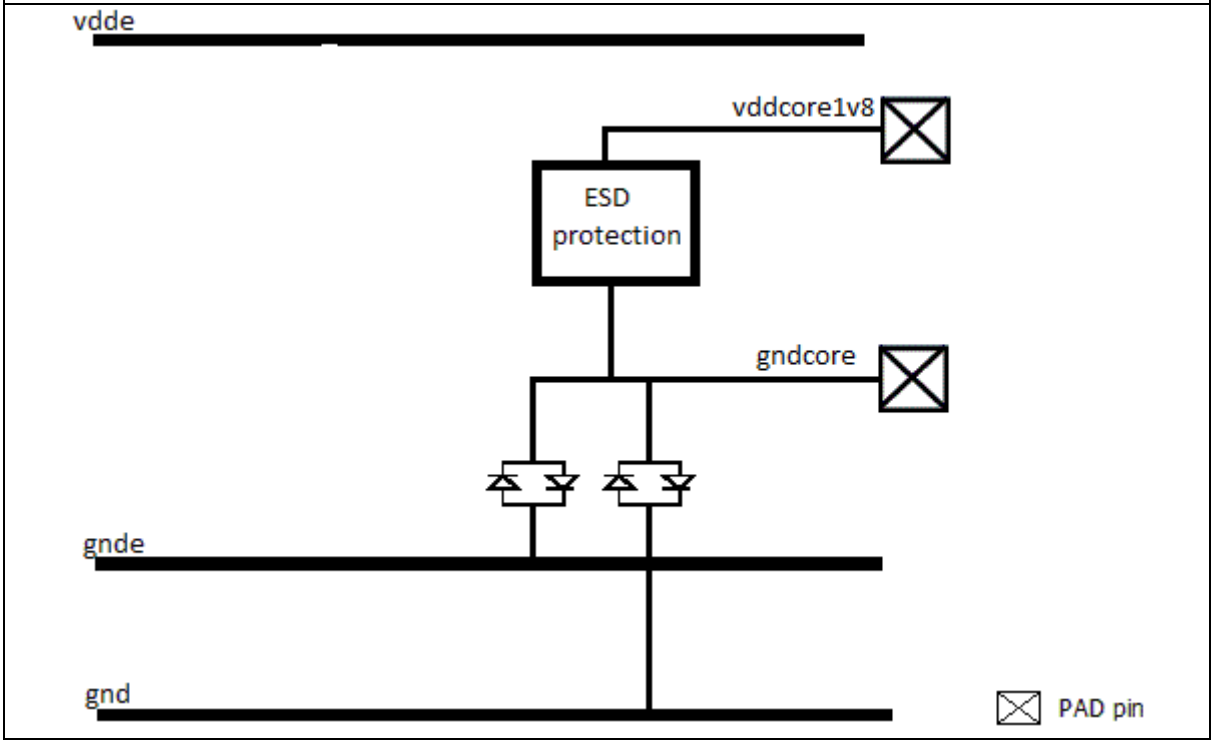
2.12.4 Functional Description

These cells represent a dedicated 1.8V CSF power supply referring to common core ground node. Core pins are provided in metal top (IB).

2.13 VDDCORE_1V8_GNDCORE_EXT_3V3SF_FC_LIN/FC_INNER/CL_LIN

2.13.1 Functional Diagram

Figure 13 : Block diagram



2.13.2 Interface Description

Table 27 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, pad side
gndcore	Input / Output	0	Dedicated ground node, pad side
Track and core pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, only core side
gndcore	Input / Output	0	Dedicated ground node, only core side
vdde	Input / Output	vdde	IO power node (3.3 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.13.3 Cell Information

Table 28 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v8 node)	-	-	495	nA
		Fast Process, Max voltage, 125 °C (vddcore1v8 node)	-	-	3.8	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v8 and gndcore nodes)	-	-	81	mA
		125 °C (vddcore1v8 and gndcore nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore1v8 and gndcore nodes)	-	-	38	
		125 °C (vddcore1v8 and gndcore nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore1v8 and gndcore nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (vddcore1v8 and gndcore nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

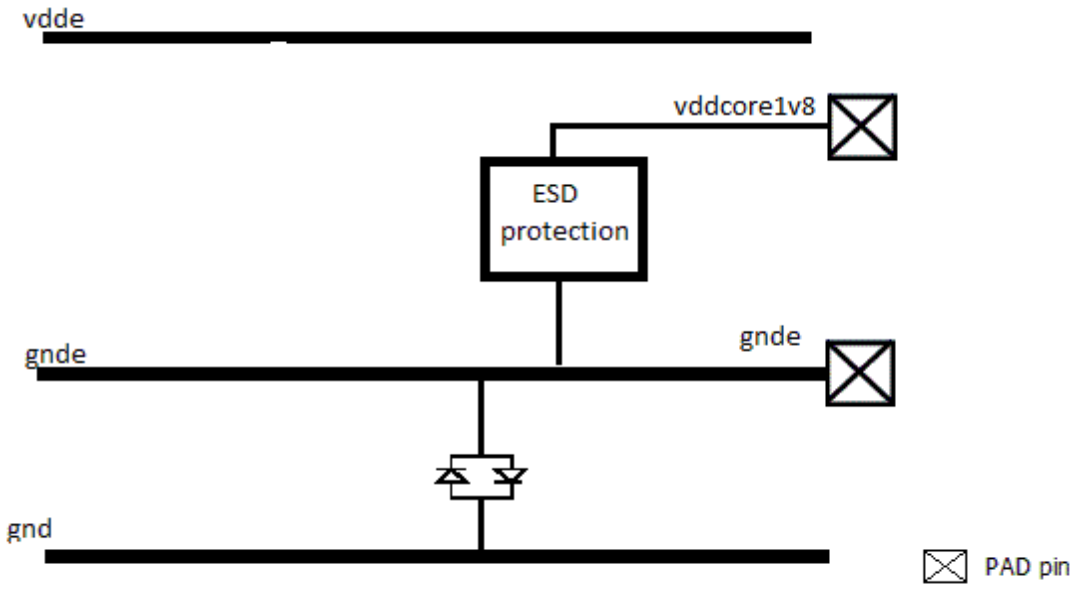
2.13.4 Functional Description

These cells represent a dedicated 1.8V 3V3SF power supply referring to a dedicated ground node. Core pins are provided in metal top (IB).

2.14 VDDCORE_1V8_GNDE_EXT_3V3SF_FC_LIN/FC_INNER/CL_LIN

2.14.1 Functional Diagram

Figure 14 : Block diagram



2.14.2 Interface Description

Table 29 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, pad side
gnde	Input / Output	0	IO ground node, pad side
Track and core pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (3.3 V), only track side
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.14.3 Cell Information

Table 30 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v8 node)	-	-	495	nA
		Fast Process, Max voltage, 125 °C (vddcore1v8 node)	-	-	3.8	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v8 and gnde nodes)	-	-	81	mA
		125 °C (vddcore1v8 and gnde nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore1v8 and gnde nodes)	-	-	38	
		125 °C (vddcore1v8 and gnde nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore1v8 and gnde nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (vddcore1v8 and gnde nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

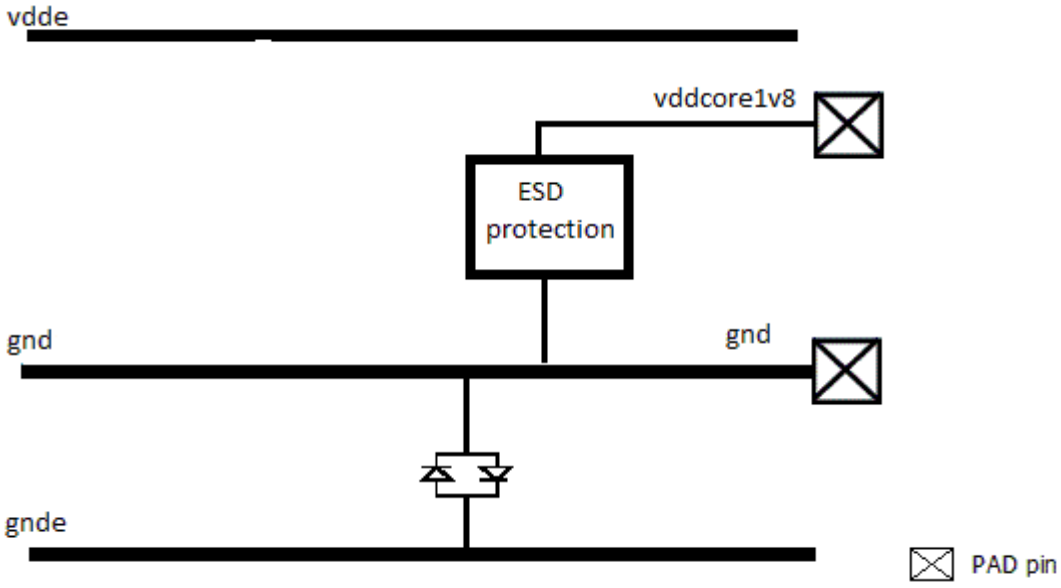
2.14.4 Functional Description

These cells represent a dedicated 1.8V 3V3SF power supply referring to the IO ground node. Core pins are provided in metal top (IB).

2.15 VDDCORE_1V8_GND_EXT_3V3SF_FC_LIN/FC_INNER/CL_LIN

2.15.1 Functional Diagram

Figure 15 : Block diagram



2.15.2 Interface Description

Table 31 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, pad side
gnd	Input / Output	0	Core and substrate ground node, pad side
Track and core pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (3.3 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.15.3 Cell Information

Table 32 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v8 node)	-	-	495	nA
		Fast Process, Max voltage, 125 °C (vddcore1v8 node)	-	-	3.8	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore1v8 and gnd nodes)	-	-	81	mA
		125 °C (vddcore1v8 and gnd nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore1v8 and gnd nodes)	-	-	38	
		125 °C (vddcore1v8 and gnd nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore1v8 and gnd nodes)	-	-	139	mA
	RMS current Pad To Core [2]	100 °C (vddcore1v8 and gnd nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

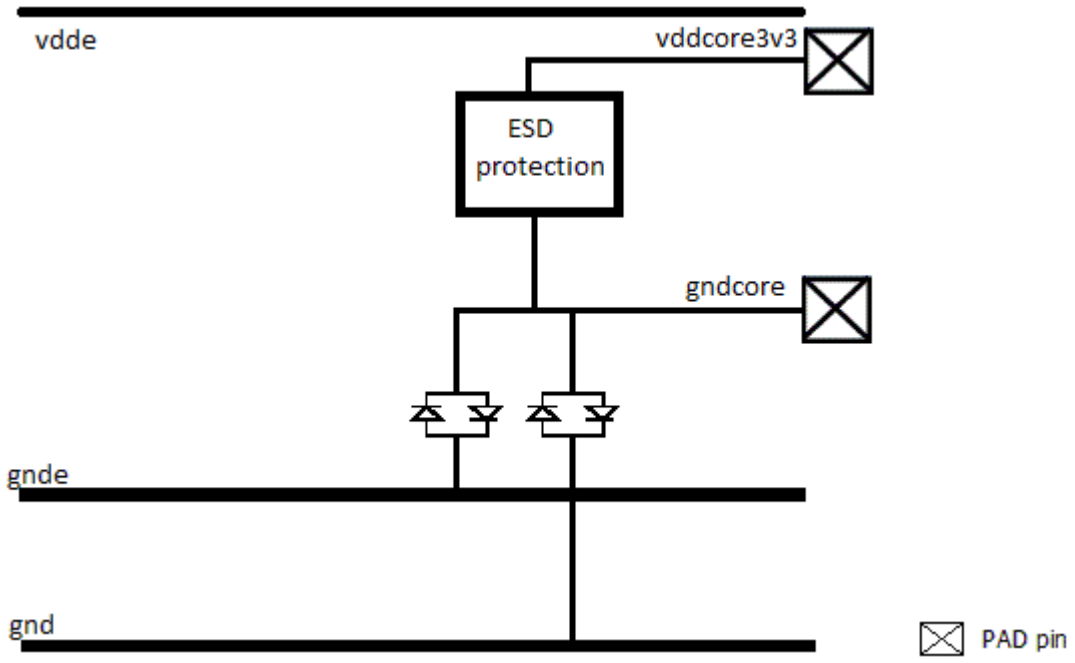
2.15.4 Functional Description

These cells represent a dedicated 1.8V 3V3SF power supply referring to a dedicated ground node. Core pins are provided in metal top (IB).

2.16 VDDCORE_3V3_GNDCORE_EXT_CSF_FC_LIN/FC_INNER/CL_LIN

2.16.1 Functional Diagram

Figure 16 : Block diagram



2.16.2 Interface Description

Table 33 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, pad side
gndcore	Input / Output	0	Dedicated ground node, pad side
Track and core pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, only core side
gndcore	Input / Output	0	Dedicated ground node, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.16.3 Cell Information

Table 34 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vddcore3v3 node)	-	-	2.5	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore3v3 and gndcore nodes)	-	-	81	mA
		125 °C (vddcore3v3 and gndcore nodes)	-	-	29	
	DC current Pad To Core [2]	110 °C (vddcore3v3 and gndcore nodes)	-	-	38	
		125 °C (vddcore3v3 and gndcore nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore3v3 and gndcore nodes)	-	-	167	mA
	RMS current Pad To Core [2]	100 °C (vddcore3v3 and gndcore nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

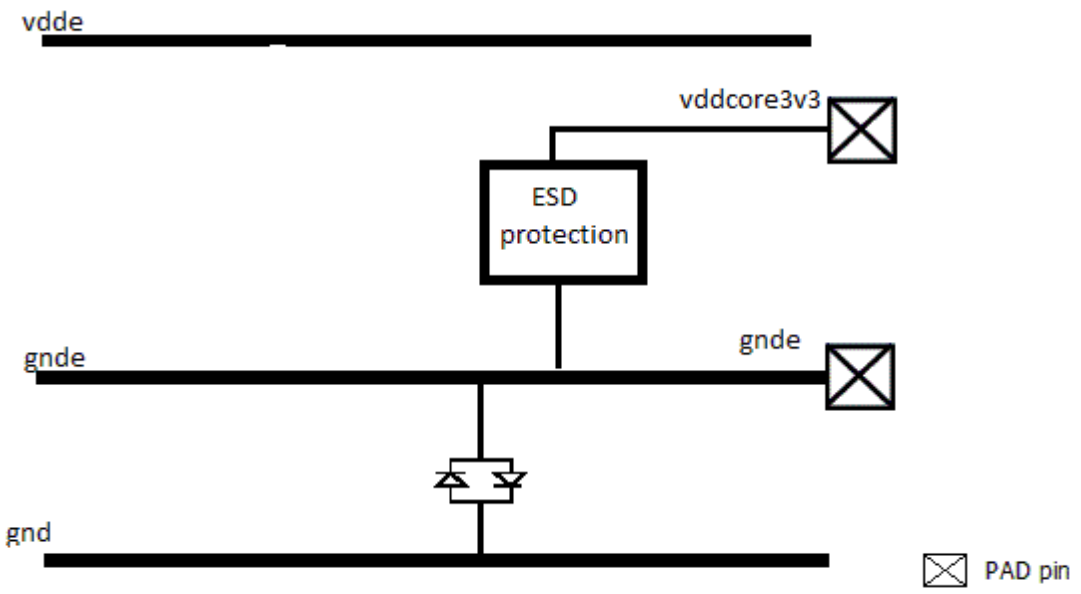
2.16.4 Functional Description

These cells represent a dedicated 3.3V CSF power supply referring to a dedicated ground node. Core pins are provided in metal top (IB).

2.17 VDDCORE_3V3_GNDE_EXT_CSF_FC_LIN/FC_INNER/CL_LIN

2.17.1 Functional Diagram

Figure 17 : Block diagram



2.17.2 Interface Description

Table 35 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, pad side
gnde	Input / Output	0	IO ground node, pad side
Track and core pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.17.3 Cell Information

Table 36 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vddcore3v3 node)	-	-	2.5	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore3v3 and gnde nodes)	-	-	110	mA
		125 °C (vddcore3v3 and gnde nodes)	-	-	40	
	DC current Pad To Core [2]	110 °C (vddcore3v3 and gnde nodes)	-	-	38	
		125 °C (vddcore3v3 and gnde nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore3v3 and gnde nodes)	-	-	167	mA
	RMS current Pad To Core [2]	100 °C (vddcore3v3 and gnde nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

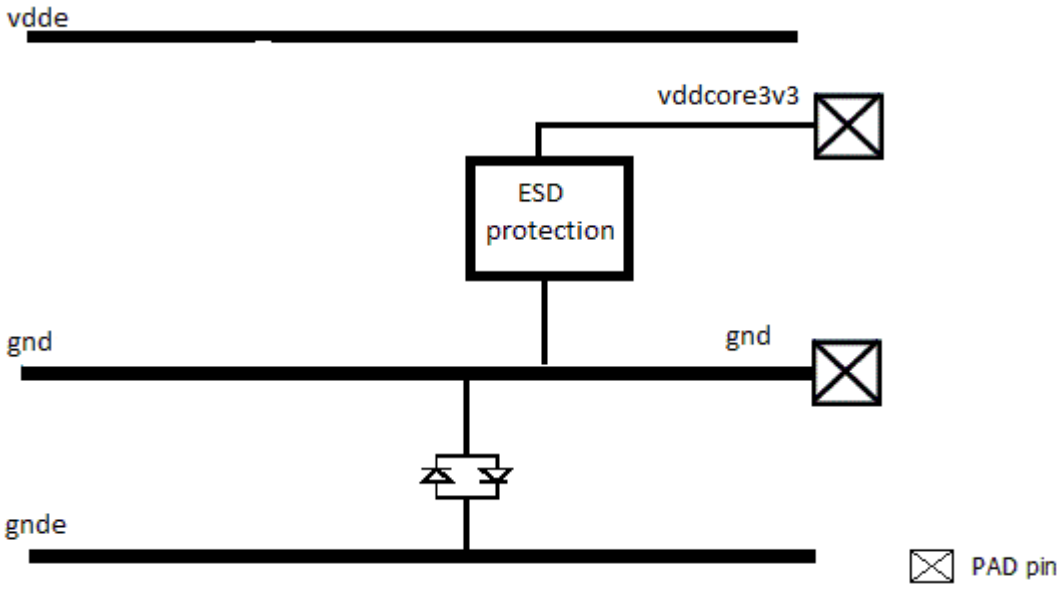
2.17.4 Functional Description

These cells represent a dedicated 3.3V CSF power supply referring to a dedicated ground node. Core pins are provided in metal top (IB).

2.18 VDDCORE_3V3_GND_EXT_CSF_FC_LIN/FC_INNER/CL_LIN

2.18.1 Functional Diagram

Figure 18 : Block diagram



2.18.2 Interface Description

Table 37 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, pad side
gnd	Input / Output	0	Core and substrate ground node, pad side
Track and core pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.18.3 Cell Information

Table 38 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vddcore3v3 node)	-	-	2.5	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore3v3 and gnd nodes)	-	-	110	mA
		125 °C (vddcore3v3 and gnd nodes)	-	-	40	
	DC current Pad To Core [2]	110 °C (vddcore3v3 and gnd nodes)	-	-	38	
		125 °C (vddcore3v3 and gnd nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore3v3 and gnd nodes)	-	-	167	mA
	RMS current Pad To Core [2]	100 °C (vddcore3v3 and gnd nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

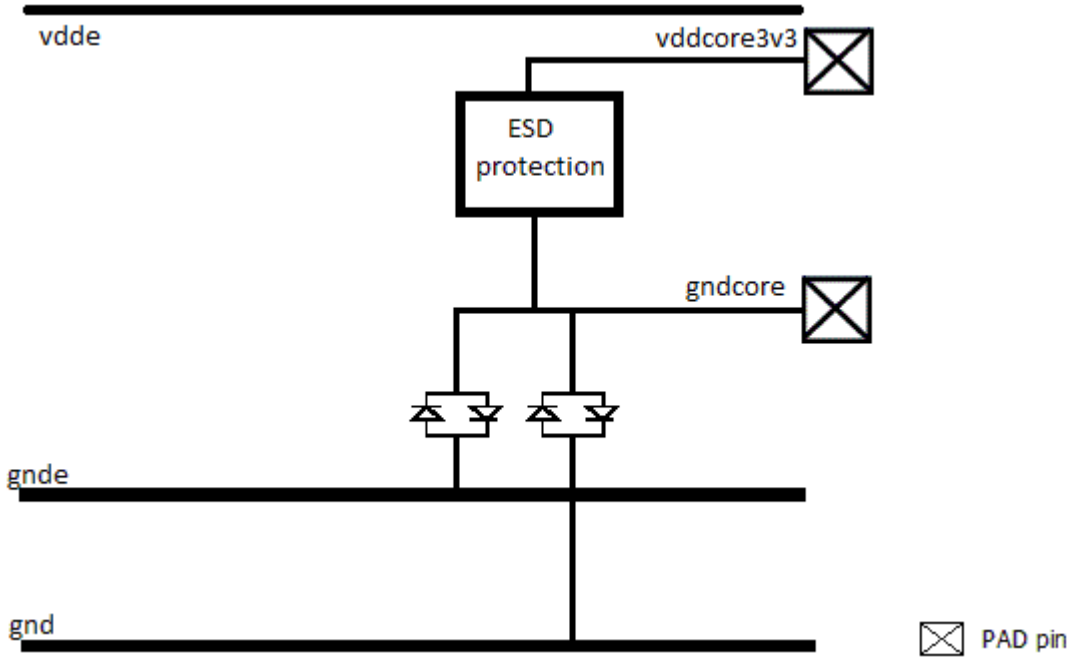
2.18.4 Functional Description

These cells represent a dedicated 3.3V CSF power supply referring to a dedicated ground node. Core pins are provided in metal top (IB).

2.19 VDDCORE_3V3_GNDCORE_EXT_3V3SF_FC_LIN/FC_INNER/CL_LIN

2.19.1 Functional Diagram

Figure 19 : Block diagram



2.19.2 Interface Description

Table 39 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, pad side
gndcore	Input / Output	0	Dedicated ground node, pad side
Track and core pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, only core side
gndcore	Input / Output	0	Dedicated ground node, only core side
vdde	Input / Output	vdde	IO power node (3.3 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.19.3 Cell Information

Table 40 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vddcore3v3 node)	-	-	2.5	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore3v3 and gndcore nodes)	-	-	110	mA
		125 °C (vddcore3v3 and gndcore nodes)	-	-	40	
	DC current Pad To Core [2]	110 °C (vddcore3v3 and gndcore nodes)	-	-	38	
		125 °C (vddcore3v3 and gndcore nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore3v3 and gndcore nodes)	-	-	167	mA
	RMS current Pad To Core [2]	100 °C (vddcore3v3 and gndcore nodes)	-	-	103	mA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

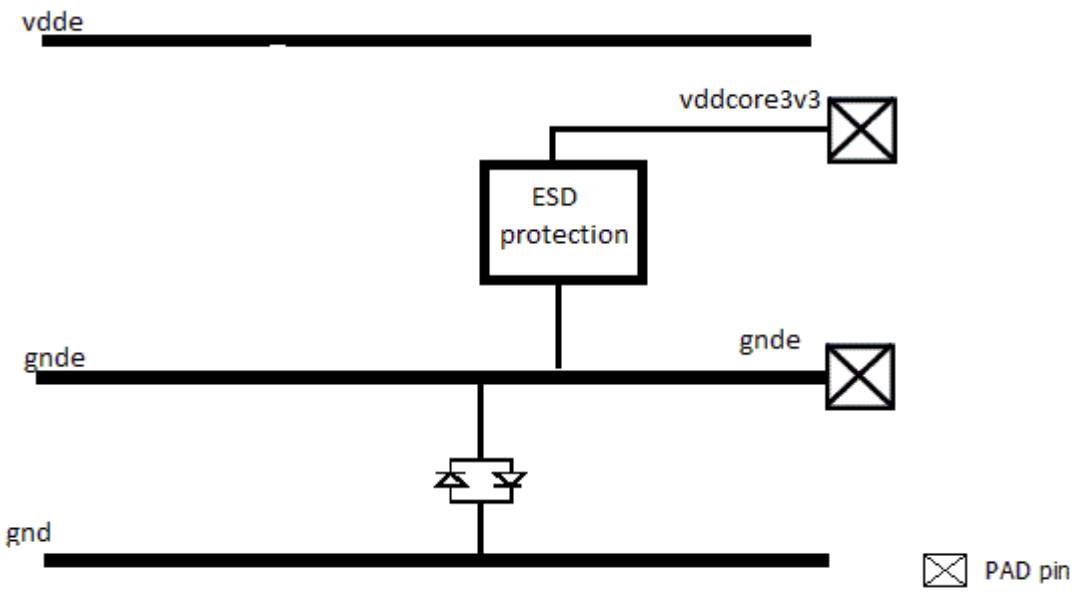
2.19.4 Functional Description

These cells represent a dedicated 3.3V CSF power supply referring to a dedicated ground node. Core pins are provided in metal top (IB).

2.20 VDDCORE_3V3_GNDE_EXT_3V3SF_FC_LIN/FC_INNER/CL_LIN

2.20.1 Functional Diagram

Figure 20 : Block diagram



2.20.2 Interface Description

Table 41 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, pad side
gnde	Input / Output	0	IO ground node, pad side
Track and core pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (3.3 V), only track side
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.20.3 Cell Information

Table 42 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vddcore3v3 node)	-	-	2.5	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore3v3 and gnde nodes)	-	-	110	mA
		125 °C (vddcore3v3 and gnde nodes)	-	-	40	
	DC current Pad To Core [2]	110 °C (vddcore3v3 and gnde nodes)	-	-	38	
		125 °C (vddcore3v3 and gnde nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (vddcore3v3 and gnde nodes)	-	-	167	mA
	RMS current Pad To Core [2]	100 °C (vddcore3v3 and gnde nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

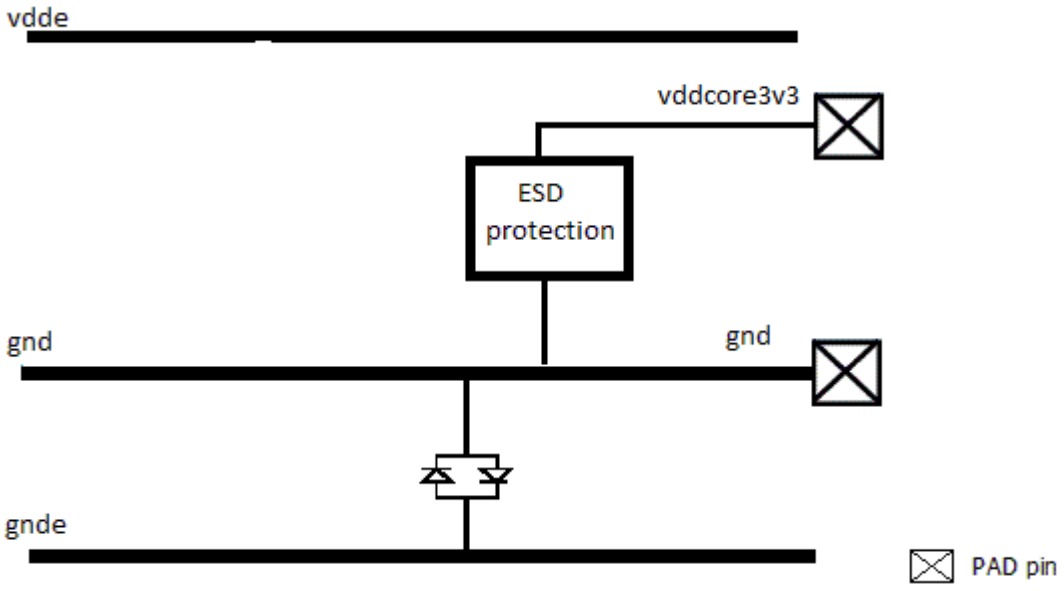
2.20.4 Functional Description

These cells represent a dedicated 3.3V CSF power supply referring to a dedicated ground node. Core pins are provided in metal top (IB).

2.21 VDDCORE_3V3_GND_EXT_3V3SF_FC_LIN/FC_INNER/CL_LIN

2.21.1 Functional Diagram

Figure 21 : Block diagram



2.21.2 Interface Description

Table 43 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, pad side
gnd	Input / Output	0	Core and substrate ground node, pad side
Track and core pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (3.3 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.21.3 Cell Information

Table 44 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vddcore3v3 node)	-	-	3.5	µA
I_{DC}	DC current Pad To Core [1]	110 °C (vddcore3v3 and gnd nodes)	-	-	110	mA
		125 °C (vddcore3v3 and gnd nodes)	-	-	40	
	DC current Pad To Core [2]	110 °C (vddcore3v3 and gnd nodes)	-	-	38	
		125 °C (vddcore3v3 and gnd nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core[1]	100 °C (vddcore3v3 and gnd nodes)	-	-	167	mA
	RMS current Pad To Core [2]	100 °C (vddcore3v3 and gnd nodes)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

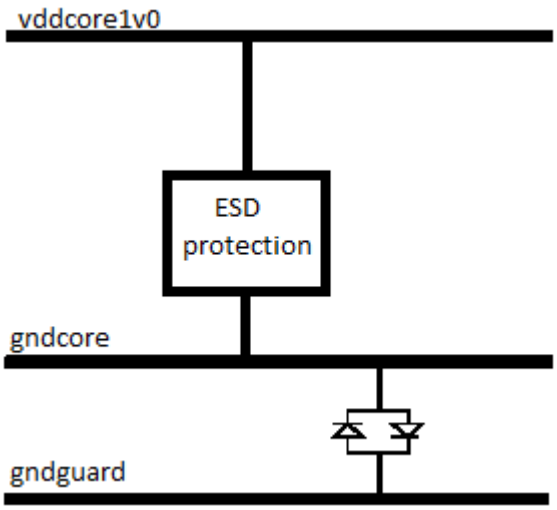
2.21.4 Functional Description

These cells represent a dedicated 3.3V CSF power supply referring to a dedicated ground node. Core pins are provided in metal top (IB).

2.22 ESDCLAMP_1V0_45U_130U_EXT

2.22.1 Functional Diagram

Figure 22 : Block diagram



2.22.2 Interface Description

Table 45 : Pin description

Pin	Type	Voltage Level (V)	Description
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.22.3 Cell Information

Table 46 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v0 node)	-	-	68	nA
		Fast Process, Max voltage, 125 °C (vddcore1v0 node)	-	-	11.7	µA

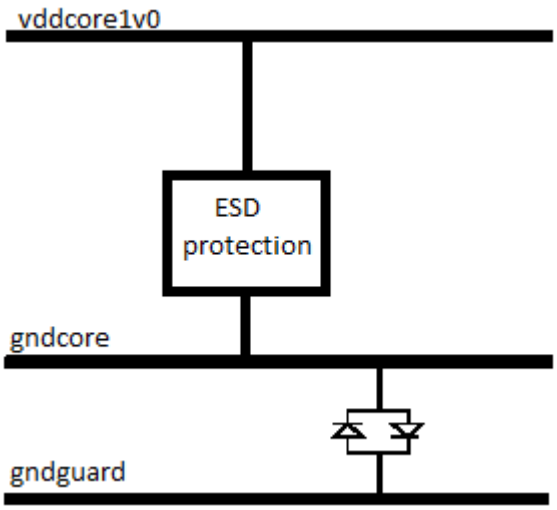
2.22.4 Functional Description

The cell is a core block that protects devices plugged between vddcore1v0 and gndcore. Pins are provided in metal 5.

2.23 ESDCLAMP_1V0_EXT

2.23.1 Functional Diagram

Figure 23 : Block diagram



2.23.2 Interface Description

Table 47 : Pin description

Pin	Type	Voltage Level (V)	Description
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.23.3 Cell Information

Table 48 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v0 node)	-	-	64	nA
		Fast Process, Max voltage, 125 °C (vddcore1v0 node)	-	-	11	µA

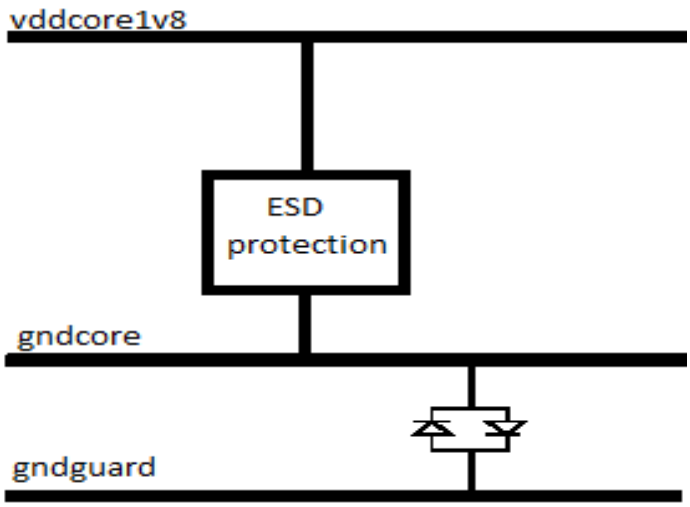
2.23.4 Functional Description

The cell is a core block that protects devices plugged between vddcore1v0 and gndcore. Pins are provided in metal 5.

2.24 ESDCLAMP_1V8_EXT

2.24.1 Functional Diagram

Figure 24 : Block diagram



2.24.2 Interface Description

Table 49 : Pin description

Pin	Type	Voltage Level (V)	Description
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.24.3 Cell Information

Table 50 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v8 node)	-	-	495	nA
		Fast Process, Max voltage, 125 °C (vddcore1v8 node)	-	-	3.8	µA

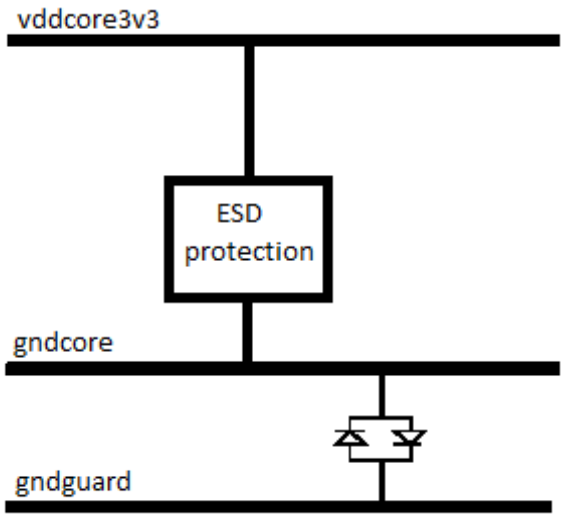
2.24.4 Functional Description

The cell is a core block that protects devices plugged between vddcore1v8 and gndcore. Pins are provided in metal 5.

2.25 ESDCLAMP_3V3_EXT

2.25.1 Functional Diagram

Figure 25 : Block diagram



2.25.2 Interface Description

Table 51 : Pin description

Pin	Type	Voltage Level (V)	Description
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.25.3 Cell Information

Table 52 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vddcore3v3 node)	-	-	2.5	µA

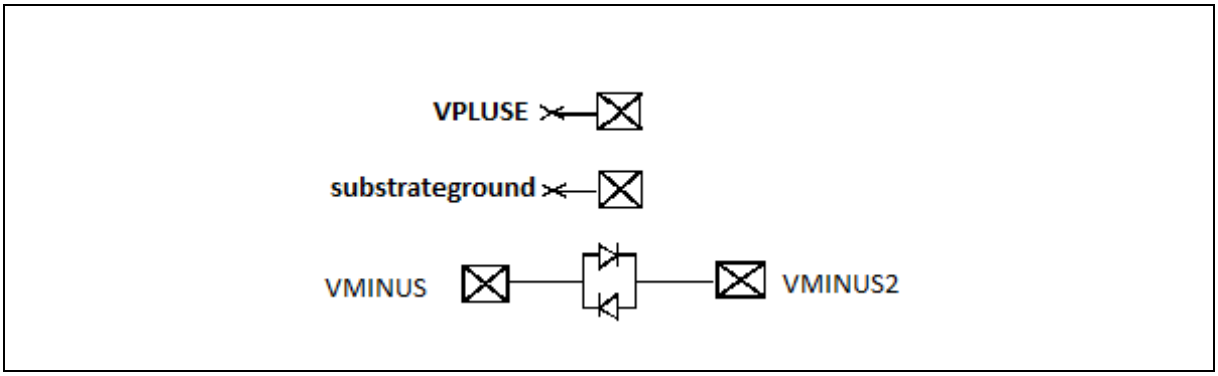
2.25.4 Functional Description

The cell is a core block that protects devices plugged between vddcore3v3 and gndcore. Pins are provided in metal 5.

2.26 CORECELL_B2B_EXT

2.26.1 Functional Diagram

Figure 26 : Block diagram



2.26.2 Interface Description

Table 53 : Pin Description

Pin	Type	Voltage Level (V)	Description
VPLUSE	Input/Output	vdde	IO power node
VMINUS	Input/Output	0	Core and substrate ground node
VMINUS2	Input/Output	0	Core and substrate ground node
substrateground	Input/Output	0	Substrate ground node

2.26.3 Cell Information

Table 54 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C	-	-	< 150	pA
		Fast Process, Max voltage, 125 °C	-	-	< 150	

2.26.4 Functional Description

This cell is intended to be placed in core area. It includes B2B diodes between 2 grounds VMINUS/VMINUS2 dedicated to ensure ESD continuity between these two ground nodes. Power and ground pins are available in M5.

3. Electrical Specifications

3.1 ESD and Latch-up Characteristics

Table 55 : ESD and Latch-up Characteristics

Symbol	Parameter	Condition	Target	Unit
V_{ESD}	Electrostatic discharge voltage	Human Body Model (HBM) [1]	2000	V
		Machine Model (MM) [1]	100	V
		Charge Device Model (CDM) except 1V0 dedicated supply and 1V0 Core Clamps [1]	500V JEDEC	V
		1V0 dedicated supply and 1V0 Core Clamps[1]	250 V JEDEC	V
$I_{latch-up}$	Injection current	Maximum operating junction temperature 125 °C [2]	100	mA
	Over-voltage stress		1.5* vdde	V

[1] ESD qualification: According to electrostatic discharge sensitivity measurement
[2] Latch-up qualification: According to latch-up sensitivity measurement.

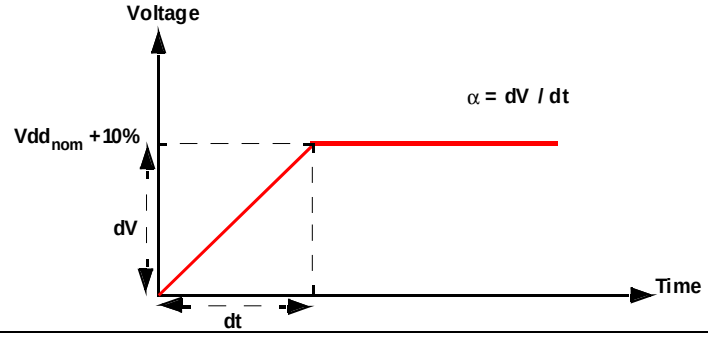
The level of CDM current seen at a given pre-charge voltage varies significantly with the chip size and package type. For instance, larger dies/packages generates higher CDM current.

However, this package size dependence has been considered during IO qualification, so that the above CDM commitment remains valid for any die/package size (even for large die/package sizes of hundreds of mm^2).

3.2 ESD Clamps Power-up Sensitivity

For correct power-up sequence without parasitic clamp switch-on, it is necessary to limit the power rise time as per next table.

Figure 27 : ESD Clamp Power-up Sensitivity



Power Ramp-Up should be equal or slower than 0.5V/us.

4. Usage Guidelines

4.1 Design Requirements

Libraries given by the table below are required to be used with this library.

Table 56 : Mandatory Libraries

Library Name	Description
C28SOI_IO_EXT_CSF_BASIC_EG*	Contains supply, corner and place and route cells needed for a CSF IO ring construction
C28SOI_IO_EXT_3V3SF_BASIC_EG*	Contains supply, corner and place and route cells needed for a 3V3SF IO ring construction

Only supply cells from other BASICs libraries must be used with dedicated supplies to build an IO ring. The following table lists the mandatory cells required.

Table 57 : Mandatory Cells

Cell Name	Mandatory Nodes	Cell Type
VDDE_*	vdde/ vdde1v8 / vdde3v3	Supply cell
GNDE_*	gnde	Supply cell
GND_EXT_CSF* GND_EXT_3V3SF_	gnd	Supply cell

4.2 Physical implementation

4.2.1 General placement rules

Cells to be used within an IO ring section in this library have their origin at (0, 0) and the ‘pr boundary’ abutted to the origin axes. The strategy to build the IO pad ring or the IO cluster is to abut laterally ‘pr boundary’ layers.

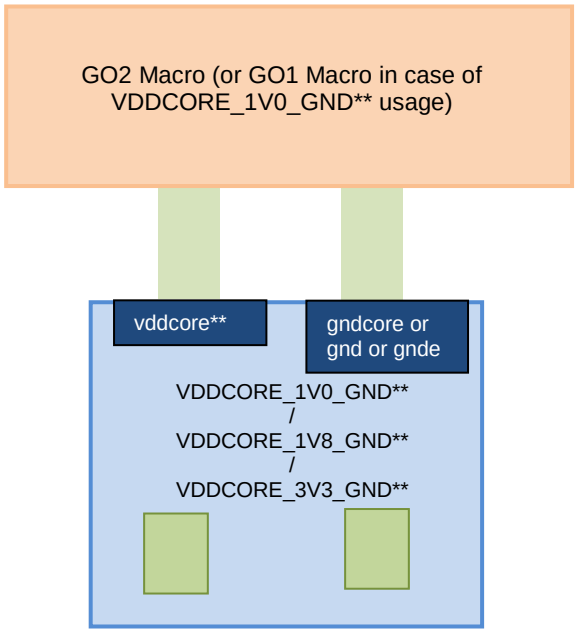
	*The rails of the IO pad ring should not be modified. Only the appropriate filler cut cells supplied within the library should be used. Non-compliance of this constraint disengages the responsibility of the IO supplier and prevents final implementation for full solution / services and support that could be provided for this deliverable.*

	To guaranty the good functionality of core clamp cells, connection have to be done through ALL available vddcore* and gndcore* pins and the entire M5 pin have to be covered by the metal used to make connection.
	For 500 V CDM target, 1V0 dedicated supply and 1V0 Core Clamps provided by this library must be used by pair

4.2.2 Dedicated supply usage

Dedicated supply cells are available in 1V0, 1V8 and 3V3 voltage range. These cells are embedding an ESD clamp between the dedicated supply and its relative ground.3 possible relative grounds are possible: gndcore separated ground, gnde IO ground, gnd common core ground

Figure 28 : Macro connection to VDDCORE__GND** dedicated supplies**

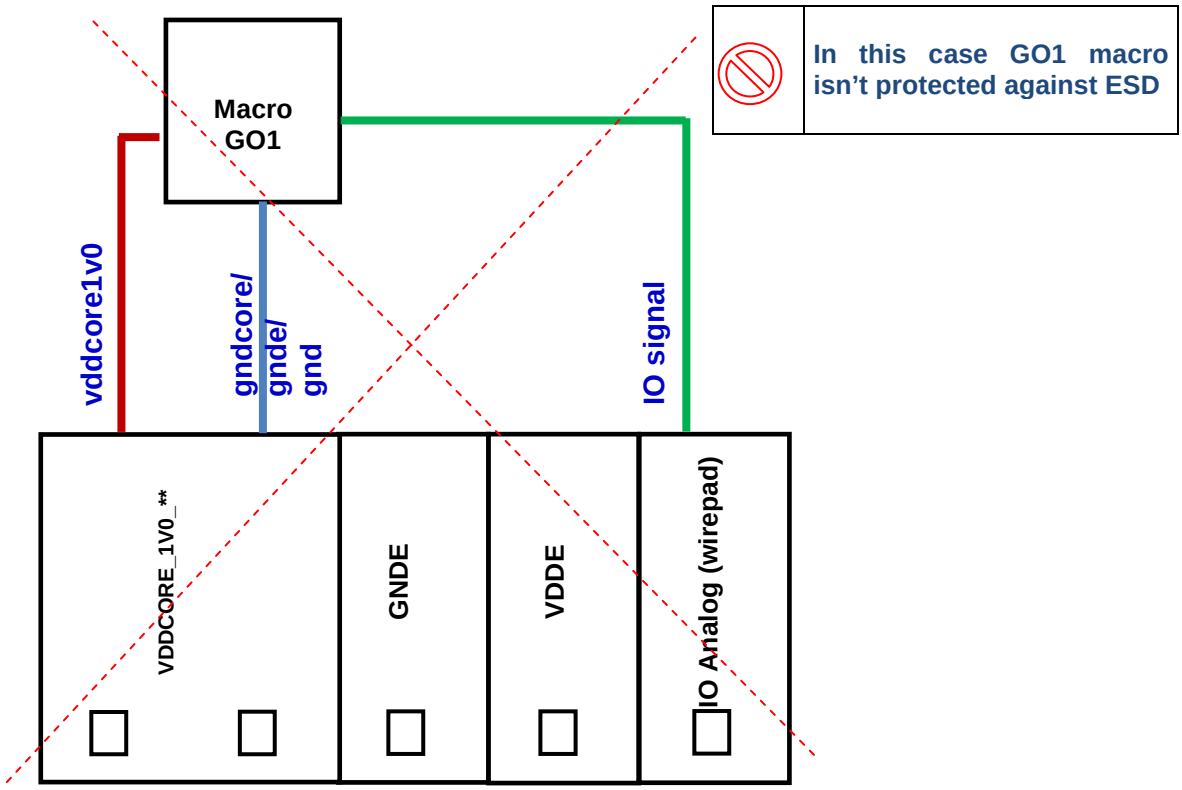


Next table describes the cells usage correspondence:

Macro supply voltage level	Devices to protect	Macro ground	Cell to use
1V0	GO1/GO2 devices	Dedicated ground	VDDCORE_1V0_GNDCORE_**
1V0	GO1/GO2 devices	Shared IO ground	VDDCORE_1V0_GNDE_**
1V0	GO1/GO2 devices	Shared core ground	VDDCORE_1V0_GND_**
1V8	GO2 devices	Dedicated ground	VDDCORE_1V8_GNDCORE_**
1V8	GO2 devices	Shared IO ground	VDDCORE_1V8_GNDE_**
1V8	GO2 devices	Shared core ground	VDDCORE_1V8_GND_**
3V3	Cascaded GO2 devices	Dedicated ground	VDDCORE_3V3_GNDCORE_**
3V3	Cascaded GO2 devices	Shared IO ground	VDDCORE_3V3_GNDE_**
3V3	Cascaded GO2 devices	Shared core ground	VDDCORE_3V3_GND_**

	VDDCORE_1V0_** dedicated supply cannot be used to protect GO1 devices connected to IO signal as highlighted in the figure below

Figure 29 : Prohibited configuration

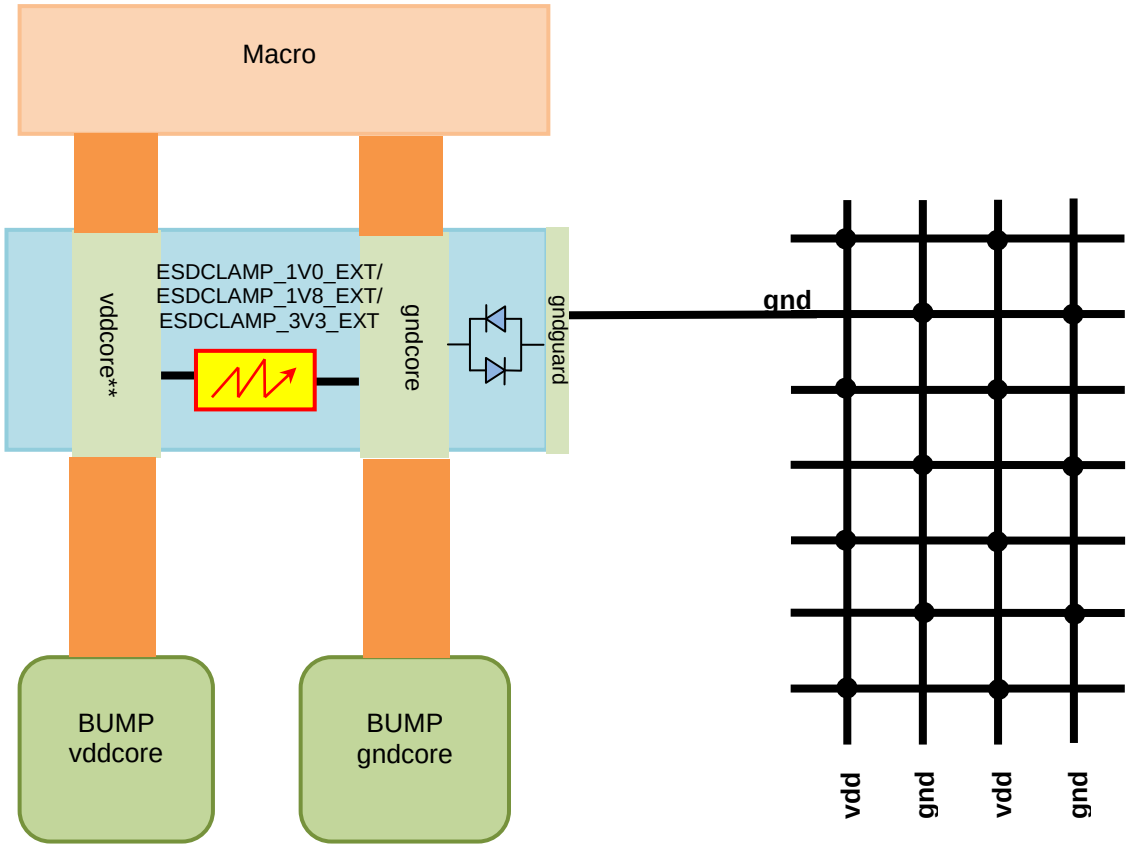


	When dedicated supply cells are used, It is necessary to supply all nodes having a pad connection.
	One 1V0 dedicated supply support 250V CDM. For 500 V CDM dedicated supplies should be placed by pair or on parallel with an 1V0 Core Clamp. For such usage, please refer to the section 'Example of 1V0 clamp usage by pair'
	For dedicated supplies or ESD Core Clamp cells placement rules please refer to 'Place and route requirements' section

4.2.3 CORE CLAMP usage

Core clamp provided by C28SOI_IO_EXT_ALLF_CORESUPPLY_EG library can be used to protect macro against ESD phenomena. These core clamps should be connected to the power BUMP and to the macro to protect.

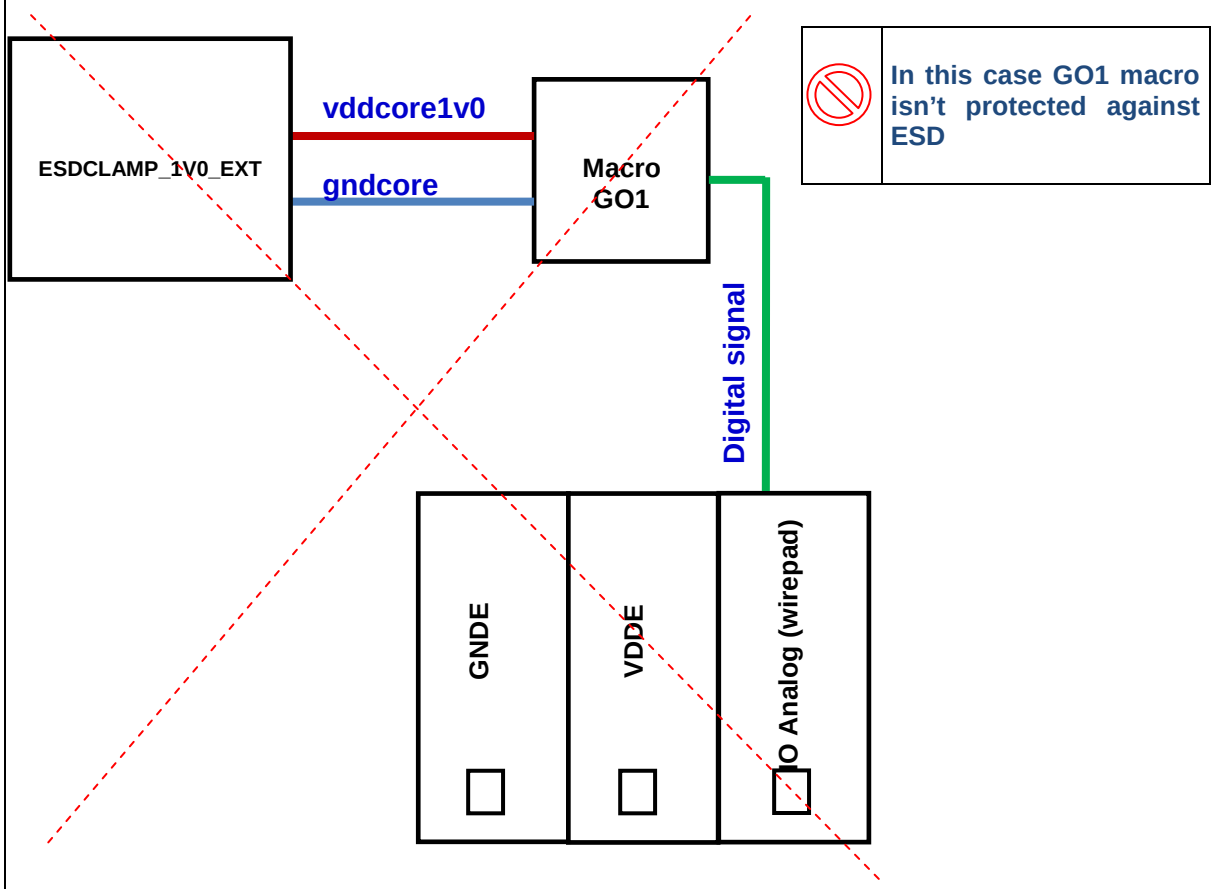
Figure 30 : Core cells usage



	*ESDCLAMP_3V3_** protects cascaded GO2 devices.* *ESDCLAMP_1V8_** protects single GO2 devices.* *Only ESDCLAMP_1V0_** clamp can be used to protect GO1 devices as well as GO2 devices*

	ESDCLAMP_1V0_EXT core clamp can be used to protect GO1 devices except those connected to a digital IO signal as highlighted in the figure below.

Figure 31 : Prohibited configuration



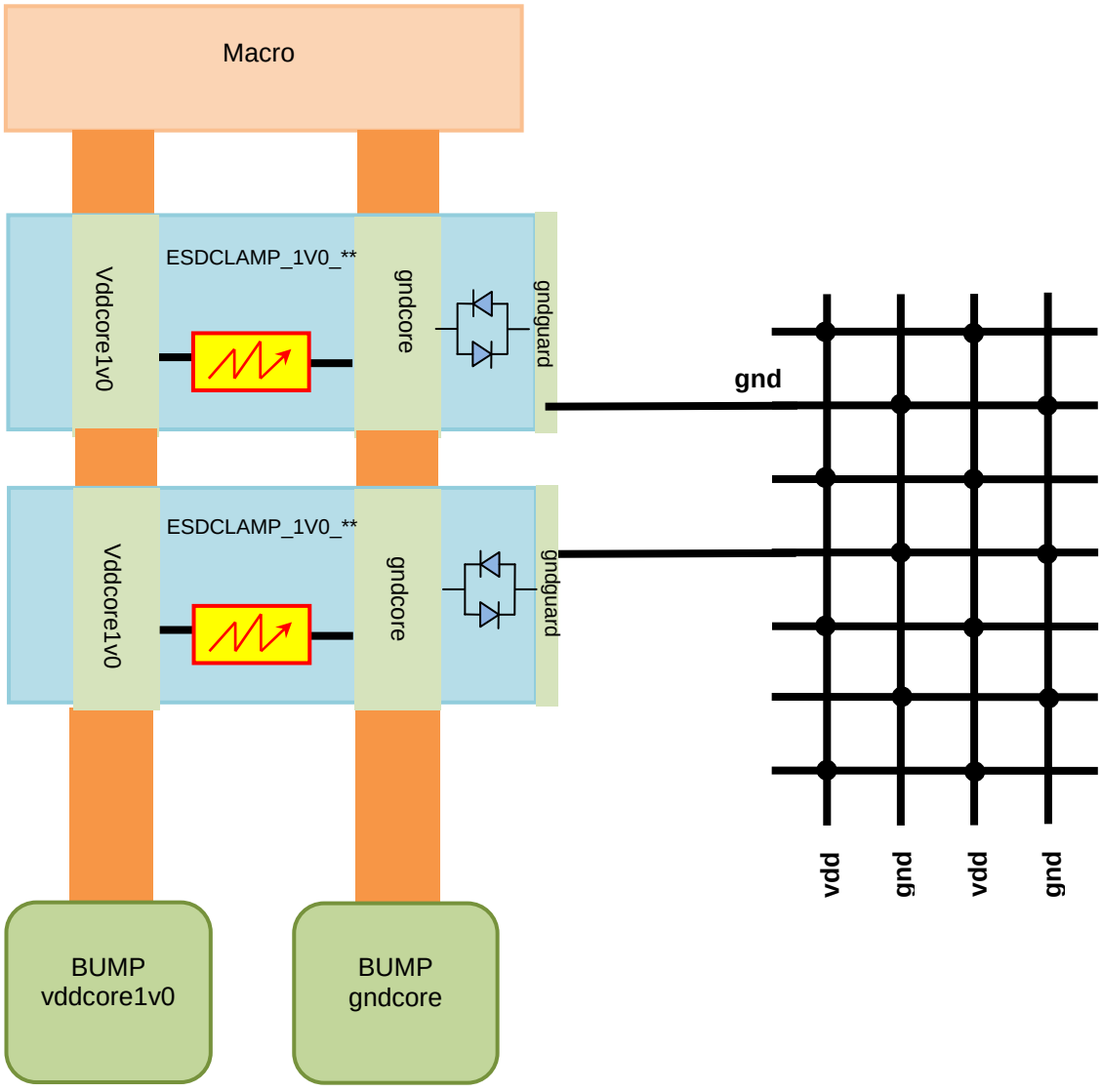
	One 1V0 core clamp support 250V CDM. For 500 V CDM 1V0 Core Clamp should be placed by pair or on parallel with a 1V0 dedicated supply. For such usage, please refer to the section 'Example of 1V0 clamp usage by pair'
	For dedicated supplies or ESD Core Clamp cells placement rules please refer to 'Place and route requirements' section

4.2.4 Example of 1V0 clamp usage by pair

In this section we give some example of 1V0 core clamp or dedicated supplies usage by pair for a 500V CDM.

Case 1: Two Core clamp on parallel

Figure 32 : Example of two 1V0 Core Clamps usage on parallel



Case 2: Core clamp on parallel with a dedicated supply cell

Figure 33 : Example of 1V0 Core clamp usage on parallel with a dedicated 1V0 supply cell

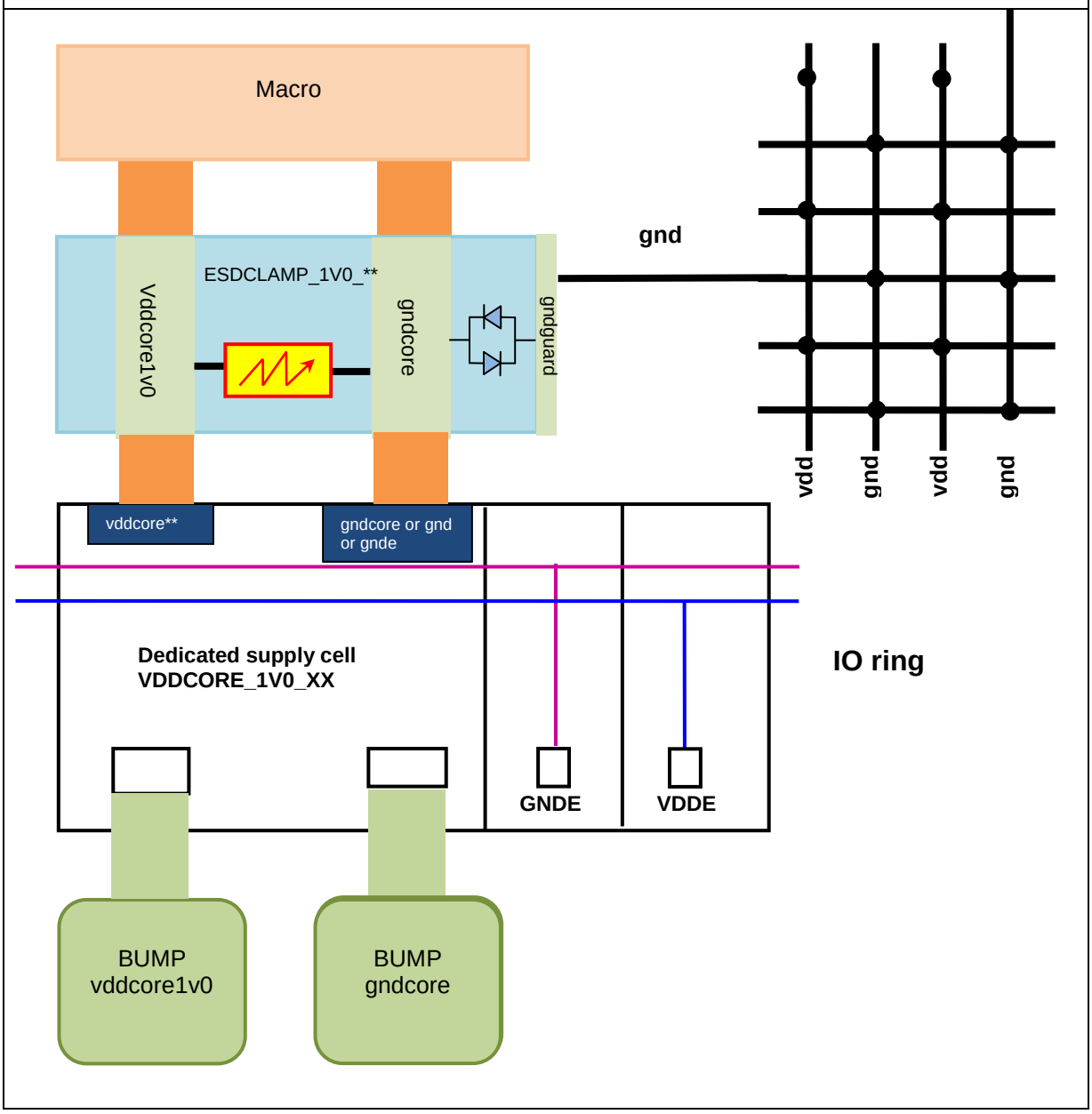
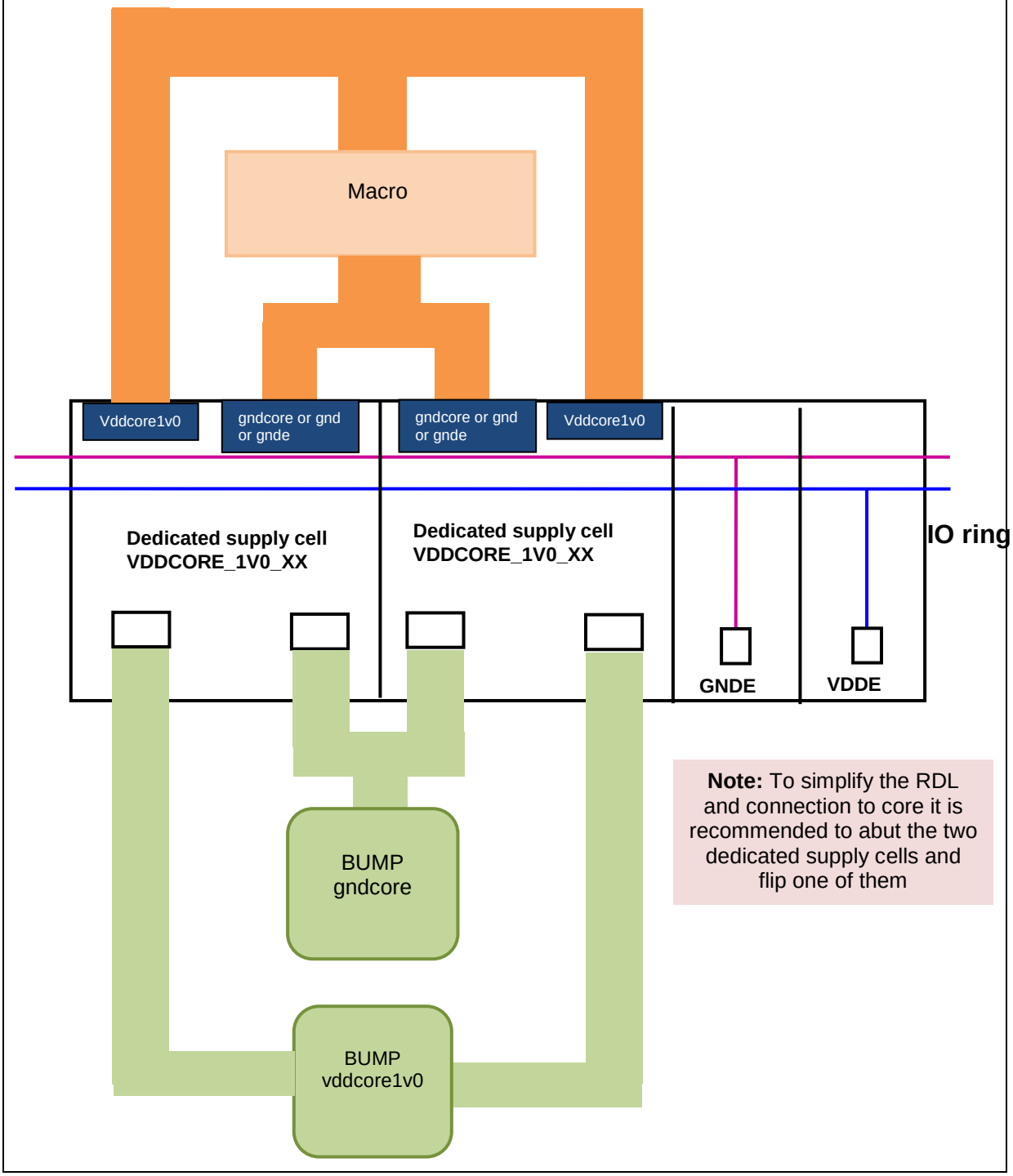


Figure 34 : Example of two dedicated 1V0 supplies connected on parallel



	For more information about clamp usage by pair or for specific configuration not listed above, please ask support through helpdesk
	For dedicated supplies or ESD core clamp cells placement rules please refer to 'Place and route requirements' section

4.2.5 Place and Route Requirements

A resistance constraint has to be respected when dedicated supplies or ESD core clamp cells are used. Figures below give more details about this constraint for different deployment cases.

Figure 35 : Dedicated supply cells used between BUMP and Macro

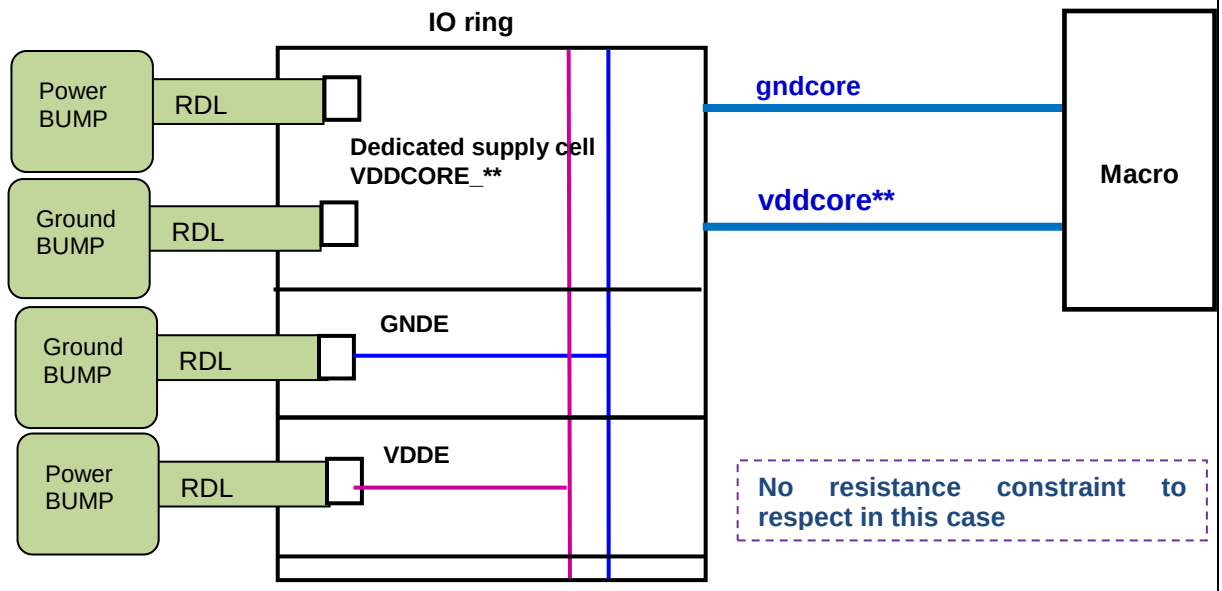


Figure 36 : ESD core clamp placed between BUMP and macro

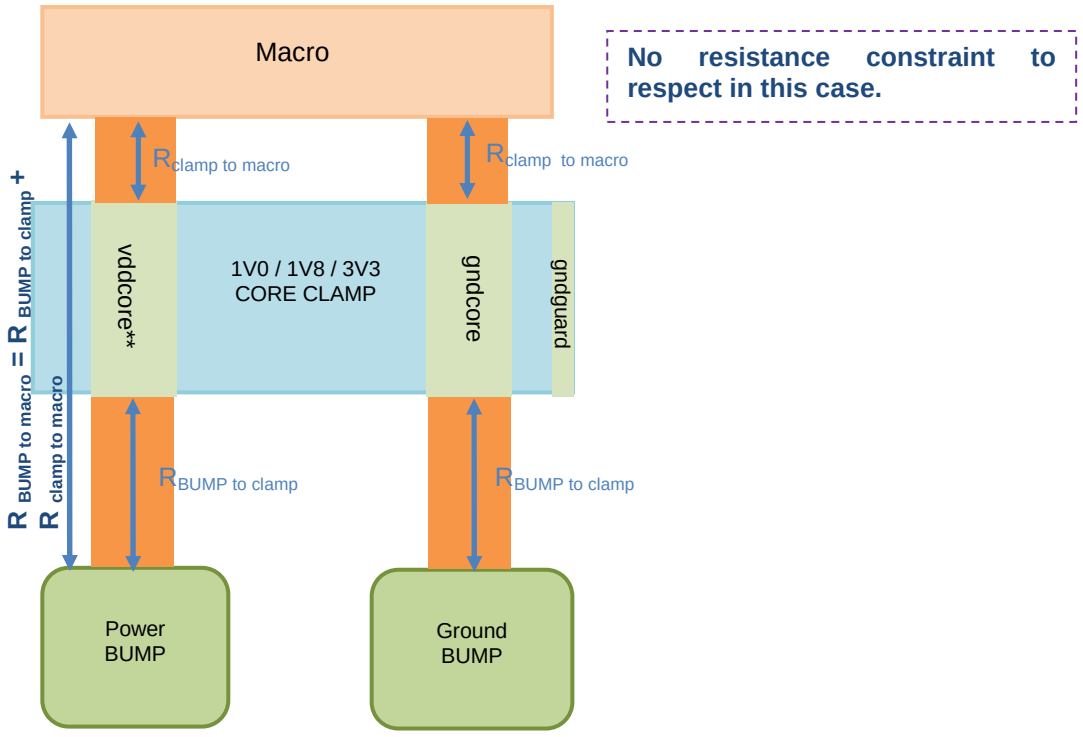
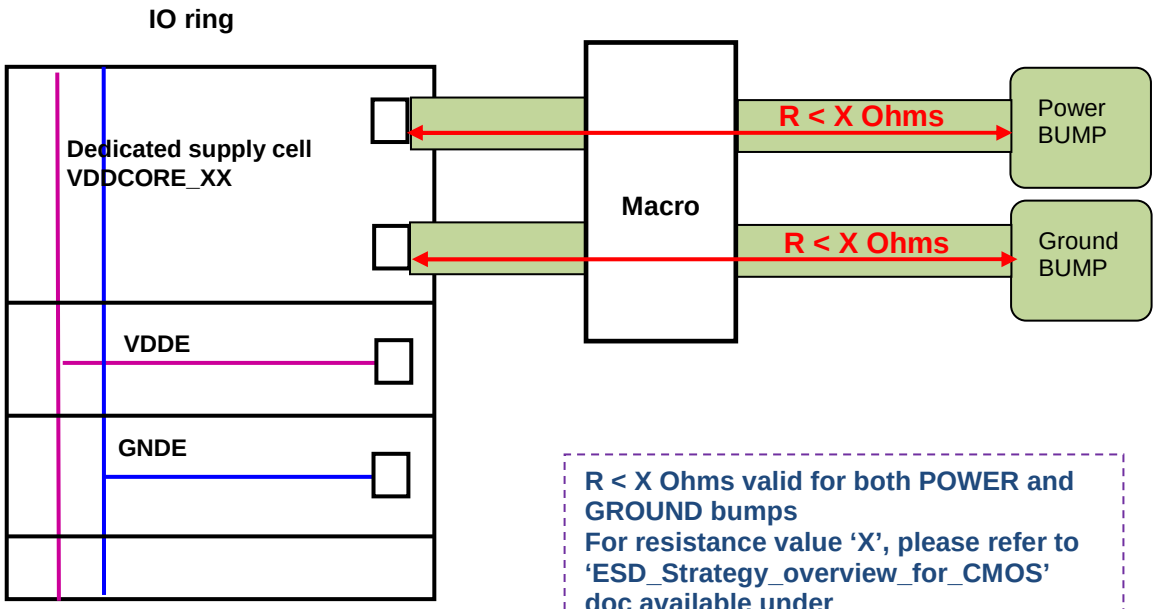
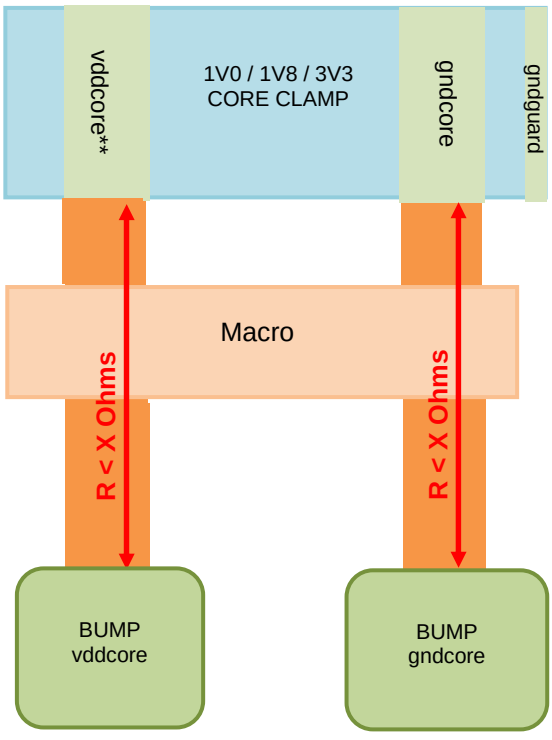


Figure 37 : Macro placed between BUMP and dedicated supply cells



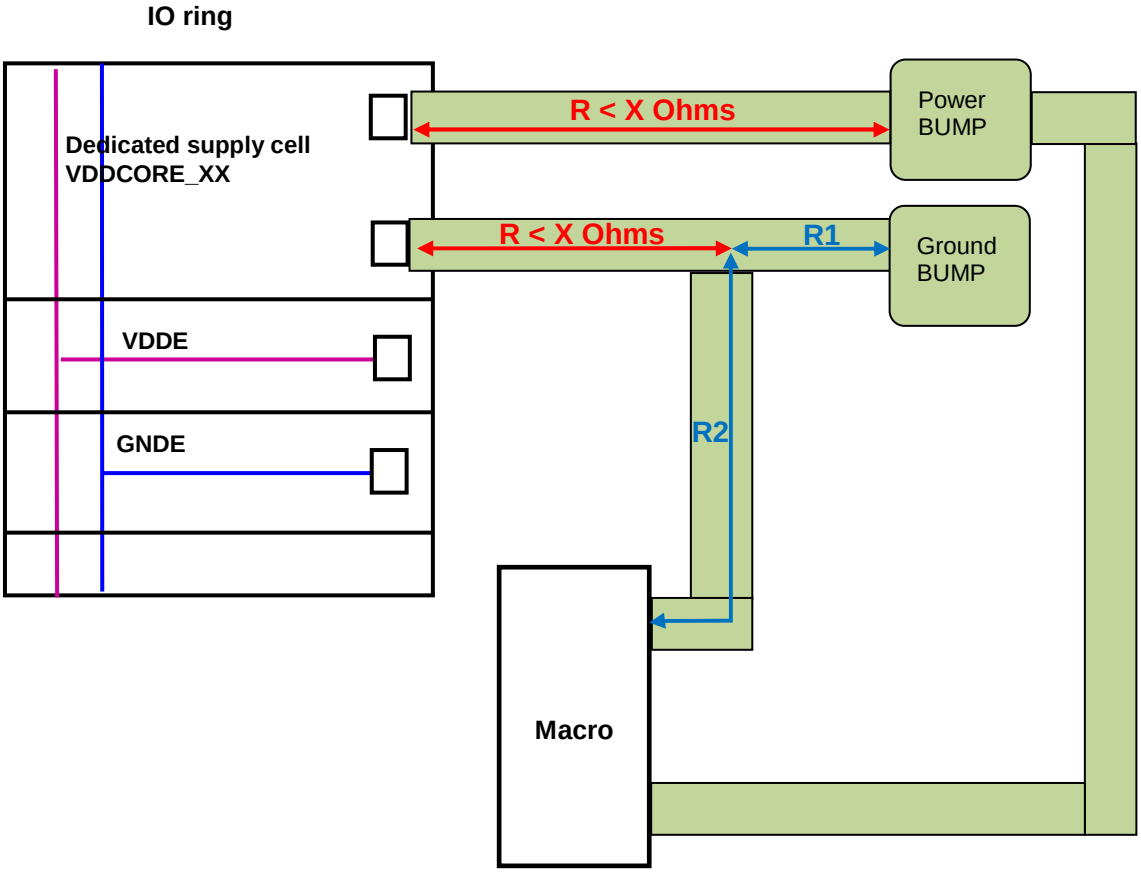
R < X Ohms valid for both POWER and GROUND bumps
For resistance value 'X', please refer to 'ESD_Strategy_overview_for_CMOS' doc available under
http://ccds.st.com/cps/sections/key-domains/esd/guideline-documents

Figure 38 : Macro placed between BUMP and ESD core clamp



R < X Ohms valid for both POWER and GROUND bumps
For resistance value 'X', please refer to 'ESD_Strategy_overview_for_CMOS' doc available under
http://ccds.st.com/cps/sections/key-domains/esd/guideline-documents

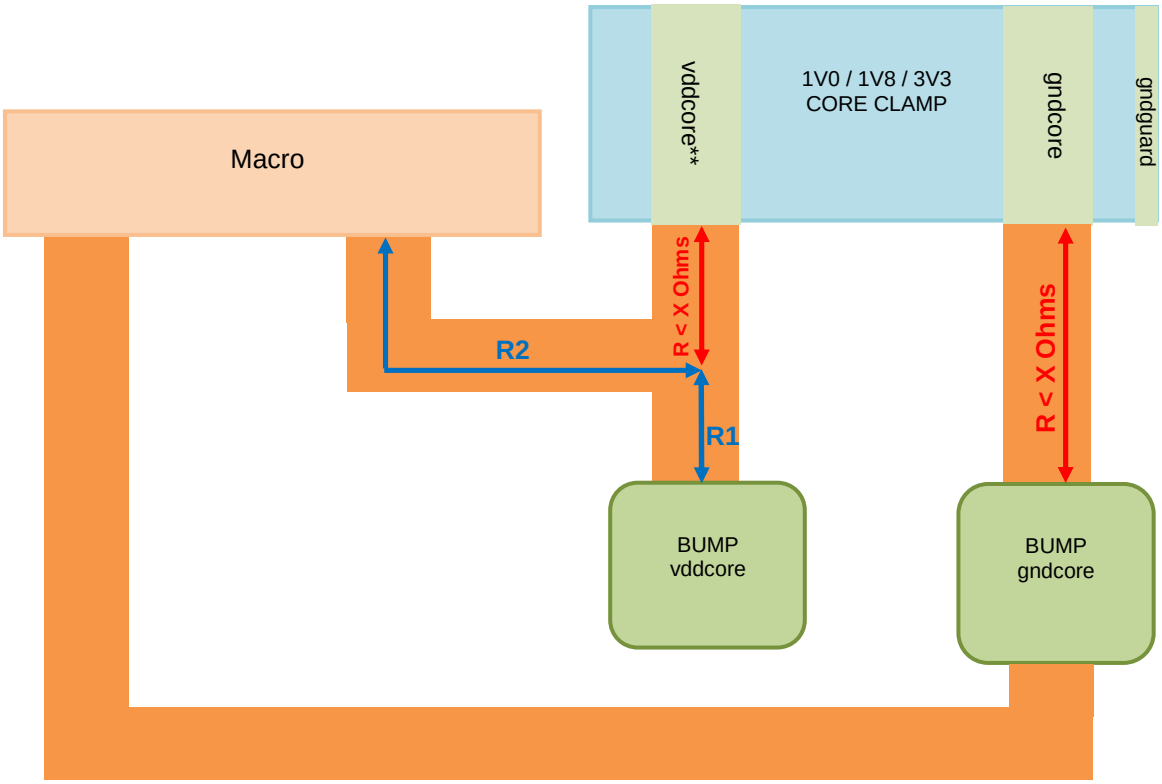
Figure 39 : Generic dedicated supply placement case



- **For resistance value 'X', please refer to 'ESD_Strategy_overview_for_CMOS' doc available under http://ccds.st.com/cps/sections/key-domains/esd/guideline-documents**
- **When we have a star routing, there are no resistance constraints for R1 and R2.**

Note: Star routing can be used also to connect ground BUMP.

Figure 40 : Generic ESD core clamp placement case



- **For resistance value 'X', please refer to 'ESD_Strategy_overview_for_CMOS' doc available under http://ccds.st.com/cps/sections/key-domains/esd/guideline-documents**
- **When we have a star routing, there are no resistance constraints for R1 and R2.**

Note: Star routing can be used also to connect GNDCORE BUMP.

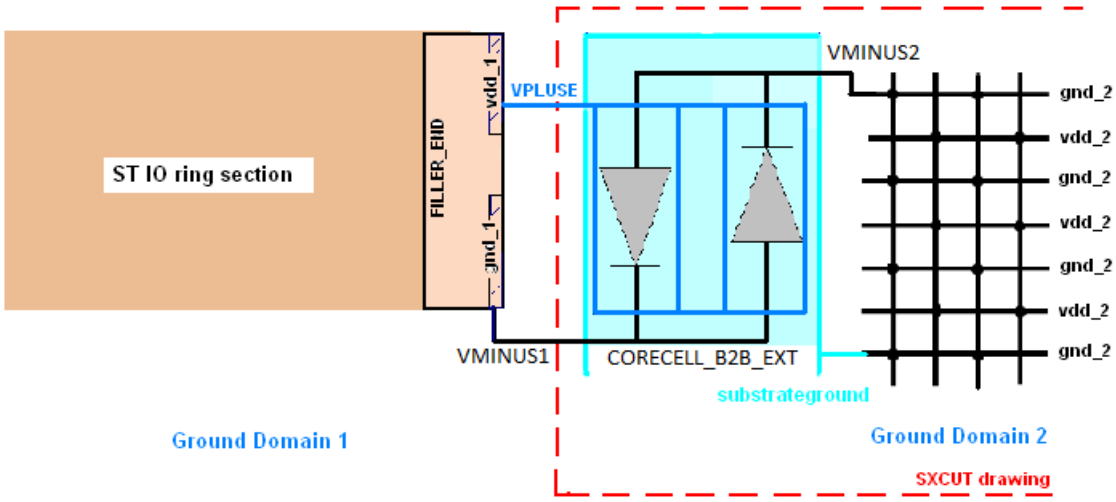
For more information about clamp usage and for specific configuration not listed above, please ask support through helpdesk

When dedicated supply cells are used, It is necessary to supply all nodes having a pad connection.

4.2.6 CORECELL_B2B_EXT usage

The CORECELL_B2B_EXT cell ensures ground continuity through two B2B diodes. The figure below gives an example of this cell usage.

Figure 41 : CORECELL_B2B_EXT usage example



The substrate ground node must be connected to the reference ground node of the ground domain where it is placed.
It is recommended to connect VPLUSE to the highest power node available.

5. Contact Information

ST users, login to **HELPDESK**. (http://col2.cro.st.com/helpdesk) for submitting queries or support requests.

Non-ST users, contact Customer Support personnel.

Appendix A: Cell Naming Convention

Table 58 : Naming Convention for Core Supply Cells

Segment Name	Description
Cell type	Refers to the functionality of cell. It can have any of the following values: – GNDCORE (dedicated ground). – VDDCORE_1V0 (dedicated supply 1.0 V). – VDDCORE_1V8 (dedicated supply 1.8 V). – VDDCORE_3V3 (dedicated supply 3.3 V).
1st suffix	Refers to the cell offer. It can have either of the following values: – <none> – EXT: extended CDM specification offer
2nd suffix	Refers to the functionality of cell. It can have any of the following values: – CSF: refers to compatible standard frame. – 3V3SF: refers to 3.3 V standard frame.
3rd suffix	Refers to the layout view of cell. It can have any of the following values: – FC: represents flip-chip configuration. – CL: represents cluster configuration.
4th suffix	Refers to the layout view of cell. It can have any of the following values: – LIN: represents single row configuration.

Table 59 : Example Segments in Name of GNDCORE_EXT_CSF_FC_LIN Cell

Segment Name	Segment Value	Description
Cell type	GNDCORE	Dedicated ground supply.
1st suffix	EXT	Extended CDM specification
2nd suffix	CSF	Uses compatible standard frame.
3rd suffix	FC	Uses flip-chip configuration.
4th suffix	LIN	Uses single row configuration.

Appendix B: Document Revision History

Table 60 : Document Revision History

Date	Document Version	Comments
-January-2016	1.3	• Reference Library added • Table 2 “Acronyms and Abbreviations” added • ESDCLAMP_1V0_45U_130U_EXT added • Aligned to ESD and Latch-up guideline
03-July-2015	1.2	• “ Pin description” tables improved • “ Cell Information“ tables updated
07-Oct-2014	1.1	• Track pins description added • Typo fixed
24-Sept-2014	1.0	• First release

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