C28SOI_SC_12_COREPBP4_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 4 nm

Overview

- C28SOI_SC_12_COREPBP4_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

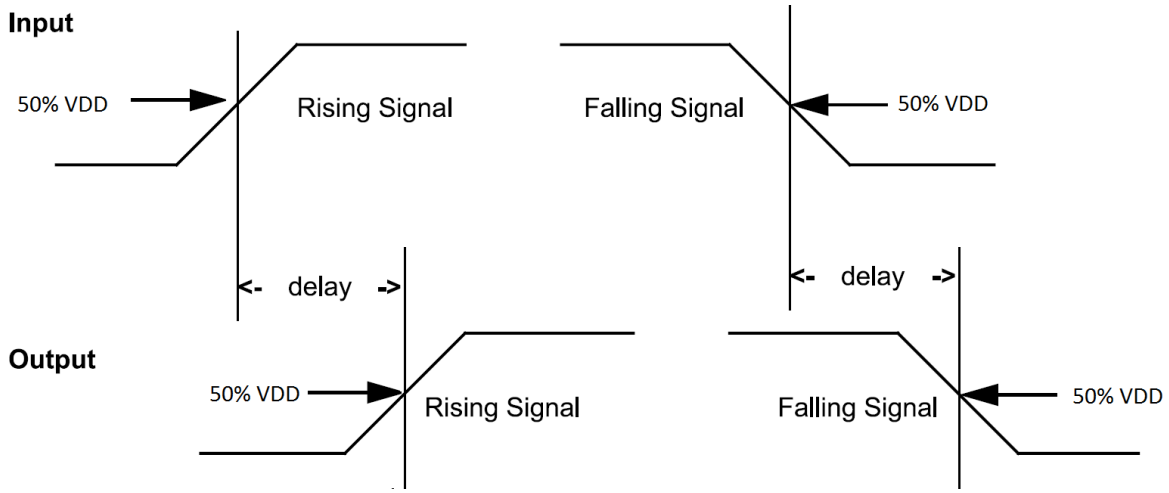


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

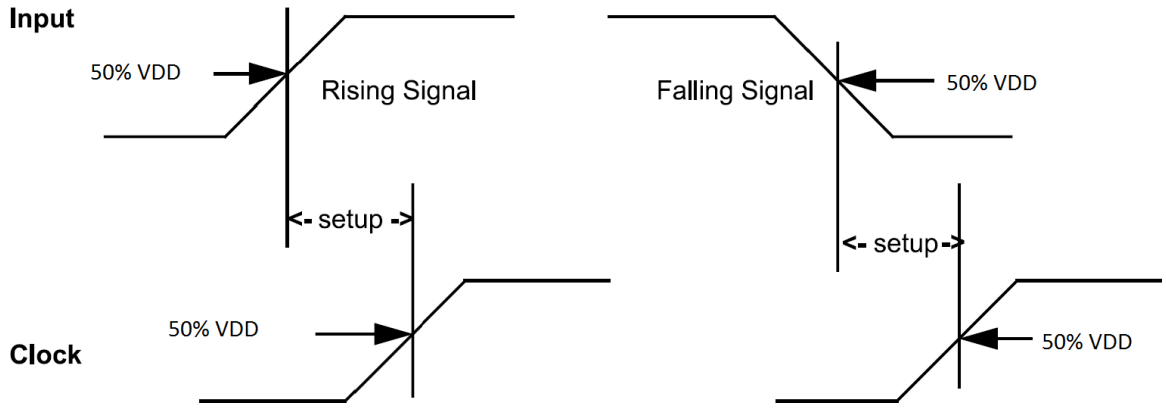


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

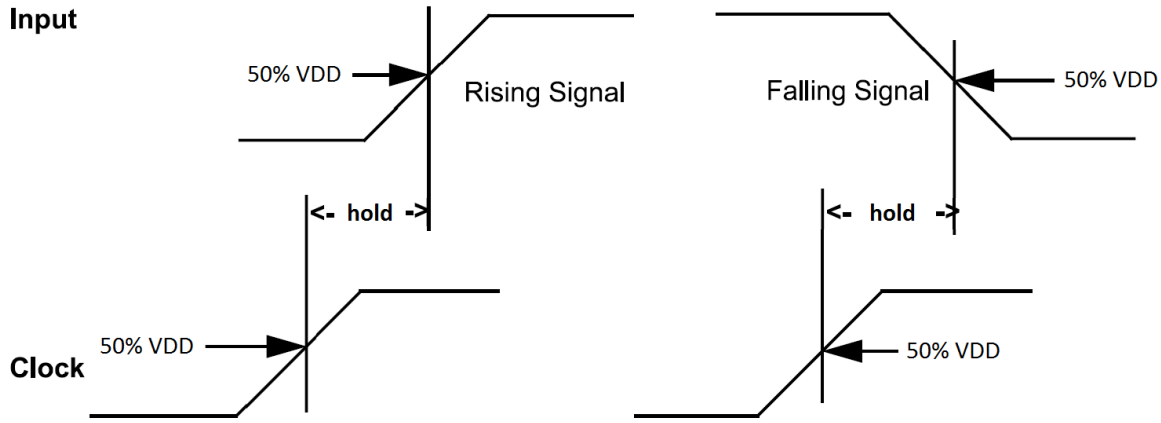


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

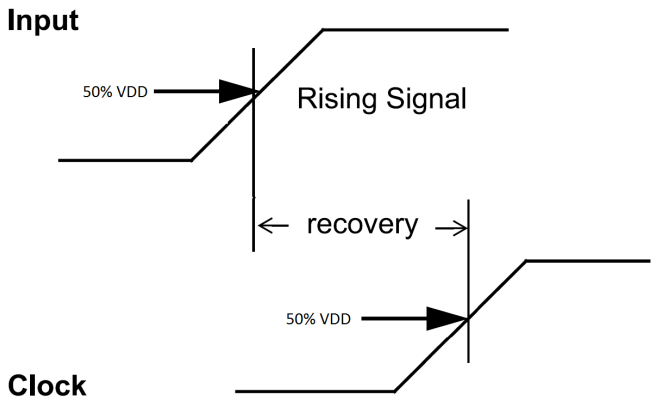


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

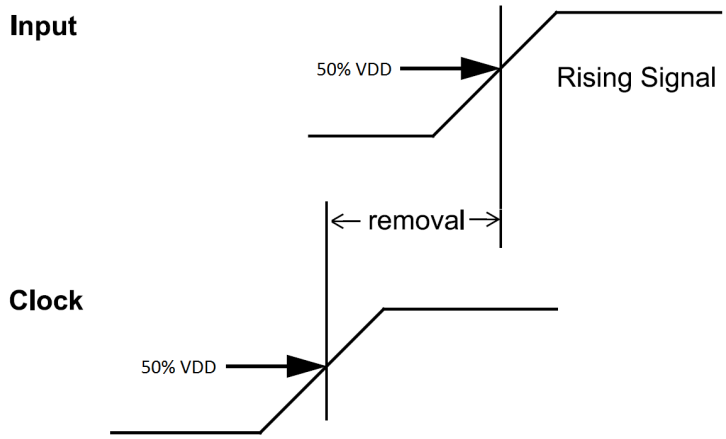


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

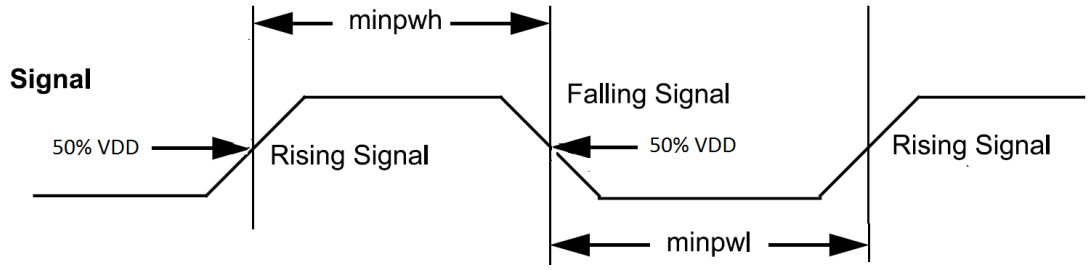


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

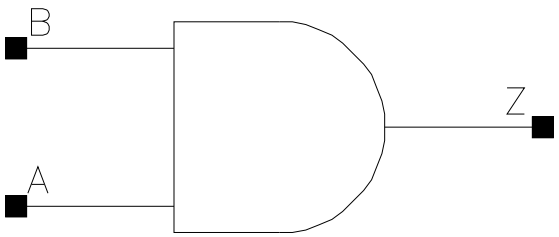
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X25_P4	1.200	1.088	1.3056
X33_P4	1.200	1.360	1.6320
X42_P4	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0008	0.0011	0.0017	0.0020
B	0.0007	0.0010	0.0016	0.0021
	X42_P4			
A	0.0020			
B	0.0020			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0260	0.0214	1.6635	0.8448
A to Z ↑	0.0208	0.0198	2.4583	1.1863
B to Z ↓	0.0247	0.0202	1.6650	0.8435
B to Z ↑	0.0222	0.0209	2.4548	1.1851
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0220	0.0213	0.5603	0.4168

A to Z ↑	0.0193	0.0201	0.7844	0.5930
B to Z ↓	0.0209	0.0195	0.5593	0.4161
B to Z ↑	0.0205	0.0206	0.7845	0.5922
	X42_P4		**X42_P4**	
A to Z ↓	0.0229		0.3386	
A to Z ↑	0.0217		0.4750	
B to Z ↓	0.0212		0.3383	
B to Z ↑	0.0225		0.4749	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	3.101e-06	1.000e-20
X16_P4	7.149e-06	1.000e-20
X25_P4	1.023e-05	1.000e-20
X33_P4	1.415e-05	1.000e-20
X42_P4	1.656e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	1.514e-05	2.907e-05	4.493e-05	9.955e-05
B (output stable)	4.254e-05	7.862e-05	1.239e-04	4.229e-04
A to Z	2.512e-03	4.244e-03	6.511e-03	8.612e-03
B to Z	2.397e-03	4.051e-03	6.208e-03	7.915e-03
	X42_P4			
A (output stable)	1.006e-04			
B (output stable)	4.146e-04			
A to Z	1.029e-02			
B to Z	9.615e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

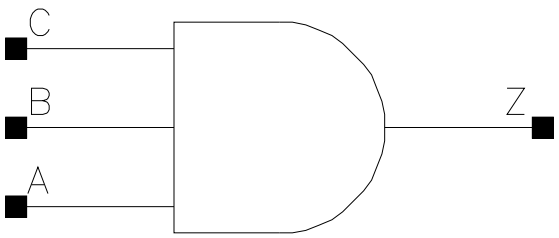
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X25_P4	1.200	1.360	1.6320
X33_P4	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0007	0.0011	0.0018	0.0021
B	0.0006	0.0011	0.0016	0.0020
C	0.0007	0.0011	0.0015	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0281	0.0234	1.6806	0.8227
A to Z ↑	0.0262	0.0247	2.4809	1.1771
B to Z ↓	0.0272	0.0224	1.6813	0.8216
B to Z ↑	0.0273	0.0258	2.4827	1.1766
C to Z ↓	0.0260	0.0211	1.6788	0.8214
C to Z ↑	0.0283	0.0262	2.4817	1.1747
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0235	0.0223	0.5658	0.4231

A to Z ↑	0.0240	0.0234	0.8060	0.6039
B to Z ↓	0.0226	0.0213	0.5661	0.4225
B to Z ↑	0.0251	0.0245	0.8074	0.6045
C to Z ↓	0.0213	0.0202	0.5655	0.4224
C to Z ↑	0.0258	0.0252	0.8056	0.6038

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	3.186e-06	1.000e-20
X17_P4	7.319e-06	1.000e-20
X25_P4	1.028e-05	1.000e-20
X33_P4	1.425e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	1.385e-05	2.771e-05	3.694e-05	5.014e-05
B (output stable)	4.378e-05	8.652e-05	1.232e-04	1.669e-04
C (output stable)	8.358e-05	1.612e-04	2.365e-04	3.250e-04
A to Z	2.776e-03	4.895e-03	7.082e-03	9.172e-03
B to Z	2.652e-03	4.674e-03	6.738e-03	8.720e-03
C to Z	2.548e-03	4.462e-03	6.421e-03	8.285e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

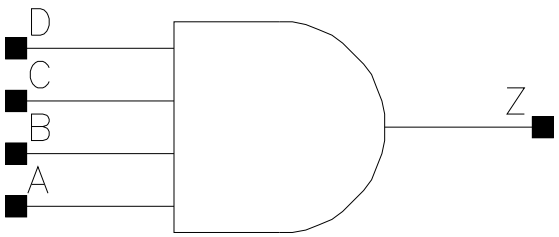
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X6_P4	1.200	1.088	1.3056
X20_P4	1.200	2.312	2.7744
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P4	X6_P4	X20_P4	X27_P4
A	0.0005	0.0008	0.0018	0.0020
B	0.0005	0.0008	0.0018	0.0021
C	0.0005	0.0008	0.0018	0.0020
D	0.0005	0.0008	0.0018	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X6_P4	X4_P4	X6_P4
A to Z ↓	0.0292	0.0254	3.1185	2.0345
A to Z ↑	0.0274	0.0216	8.4801	4.5377
B to Z ↓	0.0283	0.0238	3.1200	2.0344
B to Z ↑	0.0290	0.0225	8.4851	4.5411
C to Z ↓	0.0301	0.0271	3.0849	2.0436
C to Z ↑	0.0273	0.0215	8.4908	4.5456

D to Z ↓	0.0292	0.0253	3.0849	2.0395
D to Z ↑	0.0295	0.0226	8.4983	4.5460
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0245	0.0227	0.5959	0.4214
A to Z ↑	0.0225	0.0251	1.5228	1.1588
B to Z ↓	0.0225	0.0209	0.5947	0.4214
B to Z ↑	0.0230	0.0258	1.5231	1.1599
C to Z ↓	0.0239	0.0220	0.5997	0.4229
C to Z ↑	0.0202	0.0222	1.5227	1.1589
D to Z ↓	0.0216	0.0203	0.5983	0.4224
D to Z ↑	0.0204	0.0230	1.5225	1.1585

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	1.097e-06	1.000e-20
X6_P4	3.263e-06	1.000e-20
X20_P4	1.056e-05	1.000e-20
X27_P4	1.435e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	4.373e-04	6.881e-04	2.036e-03	2.491e-03
B (output stable)	4.135e-04	6.407e-04	1.925e-03	2.375e-03
C (output stable)	4.275e-04	7.095e-04	1.817e-03	2.254e-03
D (output stable)	4.071e-04	6.588e-04	1.691e-03	2.135e-03
A to Z	1.791e-03	2.791e-03	8.440e-03	1.086e-02
B to Z	1.715e-03	2.634e-03	7.758e-03	1.016e-02
C to Z	1.771e-03	2.834e-03	7.243e-03	9.125e-03
D to Z	1.693e-03	2.670e-03	6.542e-03	8.460e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

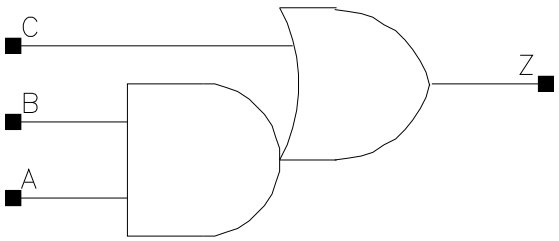
Pin Cycle (vdds)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0010	0.0021
B	0.0007	0.0011	0.0019
C	0.0007	0.0011	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0323	0.0288	1.7008	0.8347
A to Z ↑	0.0214	0.0196	2.3785	1.1661
B to Z ↓	0.0299	0.0266	1.6988	0.8324
B to Z ↑	0.0231	0.0211	2.3795	1.1665
C to Z ↓	0.0313	0.0279	1.6952	0.8314
C to Z ↑	0.0202	0.0192	2.3612	1.1605
	X33_P4		**X33_P4**	
A to Z ↓	0.0284		0.4240	
A to Z ↑	0.0197		0.5884	

B to Z ↓	0.0264		0.4234	
B to Z ↑	0.0208		0.5878	
C to Z ↓	0.0278		0.4226	
C to Z ↑	0.0188		0.5854	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	2.626e-06	1.000e-20
X17_P4	6.062e-06	1.000e-20
X33_P4	1.188e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.434e-05	4.540e-05	1.081e-04
B (output stable)	3.365e-05	6.315e-05	1.791e-04
C (output stable)	6.031e-05	1.018e-04	2.331e-04
A to Z	2.593e-03	4.538e-03	8.842e-03
B to Z	2.469e-03	4.304e-03	8.298e-03
C to Z	2.818e-03	4.923e-03	9.664e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

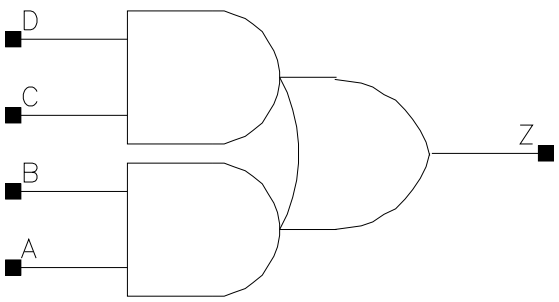
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0010	0.0020
B	0.0007	0.0010	0.0018
C	0.0006	0.0010	0.0020
D	0.0007	0.0011	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0366	0.0315	1.6426	0.8295
A to Z ↑	0.0274	0.0252	2.3476	1.1660
B to Z ↓	0.0340	0.0292	1.6378	0.8278
B to Z ↑	0.0286	0.0266	2.3465	1.1669

C to Z ↓	0.0333	0.0293	1.6390	0.8278
C to Z ↑	0.0233	0.0215	2.3400	1.1621
D to Z ↓	0.0318	0.0278	1.6359	0.8268
D to Z ↑	0.0252	0.0230	2.3406	1.1622
	X33_P4		**X33_P4**	
A to Z ↓	0.0304		0.4246	
A to Z ↑	0.0233		0.5911	
B to Z ↓	0.0287		0.4244	
B to Z ↑	0.0249		0.5911	
C to Z ↓	0.0280		0.4239	
C to Z ↑	0.0201		0.5889	
D to Z ↓	0.0265		0.4237	
D to Z ↑	0.0214		0.5886	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	3.366e-06	1.000e-20
X17_P4	7.523e-06	1.000e-20
X33_P4	1.462e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	3.526e-05	5.107e-05	8.048e-05
B (output stable)	1.354e-04	1.920e-04	1.391e-04
C (output stable)	3.020e-05	5.746e-05	1.194e-04
D (output stable)	4.502e-05	8.624e-05	1.866e-04
A to Z	3.419e-03	5.721e-03	1.074e-02
B to Z	3.163e-03	5.340e-03	1.025e-02
C to Z	2.917e-03	4.930e-03	9.133e-03
D to Z	2.807e-03	4.725e-03	8.704e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

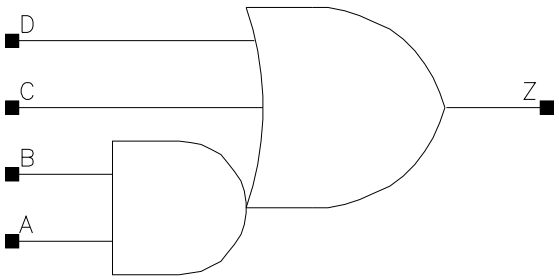
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	0.952	1.1424
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0010	0.0019
B	0.0007	0.0010	0.0019
C	0.0007	0.0010	0.0019
D	0.0006	0.0010	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0415	0.0362	1.7703	0.8776
A to Z ↑	0.0231	0.0214	2.3681	1.2168
B to Z ↓	0.0398	0.0340	1.7677	0.8757
B to Z ↑	0.0249	0.0225	2.3688	1.2173
C to Z ↓	0.0426	0.0369	1.7636	0.8744
C to Z ↑	0.0218	0.0205	2.3500	1.2093

D to Z ↓	0.0426	0.0373	1.7645	0.8755
D to Z ↑	0.0214	0.0204	2.3484	1.2092
	X33_P4		**X33_P4**	
A to Z ↓	0.0369		0.4391	
A to Z ↑	0.0213		0.5894	
B to Z ↓	0.0334		0.4375	
B to Z ↑	0.0221		0.5888	
C to Z ↓	0.0382		0.4372	
C to Z ↑	0.0202		0.5864	
D to Z ↓	0.0375		0.4376	
D to Z ↑	0.0194		0.5856	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	2.077e-06	1.000e-20
X17_P4	4.825e-06	1.000e-20
X33_P4	9.542e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	1.807e-05	4.050e-05	1.085e-04
B (output stable)	2.269e-05	4.699e-05	1.555e-04
C (output stable)	3.360e-05	6.116e-05	1.756e-04
D (output stable)	2.374e-05	5.157e-05	1.377e-04
A to Z	2.900e-03	4.929e-03	9.900e-03
B to Z	2.792e-03	4.695e-03	9.153e-03
C to Z	3.271e-03	5.572e-03	1.139e-02
D to Z	3.103e-03	5.287e-03	1.055e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

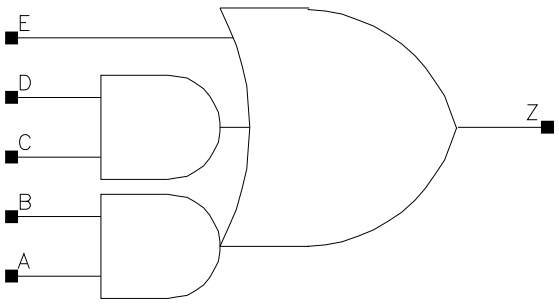
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.088	1.3056
X17_P4	1.200	1.224	1.4688
X33_P4	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0010	0.0020
B	0.0007	0.0010	0.0018
C	0.0008	0.0012	0.0020
D	0.0007	0.0010	0.0019
E	0.0006	0.0010	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0499	0.0427	1.6842	0.8513
A to Z ↑	0.0288	0.0255	2.3228	1.1728

B to Z ↓	0.0482	0.0408	1.6796	0.8502
B to Z ↑	0.0311	0.0273	2.3235	1.1718
C to Z ↓	0.0432	0.0383	1.6795	0.8497
C to Z ↑	0.0245	0.0216	2.3037	1.1651
D to Z ↓	0.0403	0.0350	1.6732	0.8460
D to Z ↑	0.0262	0.0229	2.3045	1.1653
E to Z ↓	0.0444	0.0382	1.6711	0.8463
E to Z ↑	0.0228	0.0204	2.2842	1.1579
	X33_P4		**X33_P4**	
A to Z ↓	0.0421		0.4386	
A to Z ↑	0.0262		0.5934	
B to Z ↓	0.0396		0.4381	
B to Z ↑	0.0279		0.5930	
C to Z ↓	0.0368		0.4375	
C to Z ↑	0.0215		0.5882	
D to Z ↓	0.0341		0.4363	
D to Z ↑	0.0229		0.5884	
E to Z ↓	0.0373		0.4362	
E to Z ↑	0.0203		0.5847	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	2.725e-06	1.000e-20
X17_P4	6.128e-06	1.000e-20
X33_P4	1.163e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.265e-05	3.668e-05	8.187e-05
B (output stable)	3.315e-05	4.739e-05	1.215e-04
C (output stable)	3.565e-05	5.490e-05	1.286e-04
D (output stable)	4.372e-05	7.125e-05	1.738e-04
E (output stable)	6.541e-05	1.062e-04	2.433e-04
A to Z	3.941e-03	6.425e-03	1.264e-02
B to Z	3.829e-03	6.180e-03	1.200e-02
C to Z	3.146e-03	5.250e-03	1.009e-02
D to Z	3.011e-03	4.977e-03	9.518e-03
E to Z	3.409e-03	5.602e-03	1.081e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

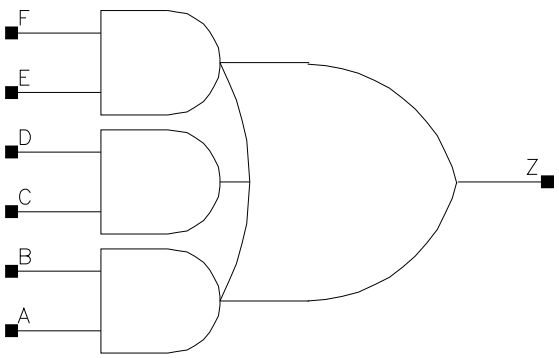
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.360	1.6320
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
A	0.0006	0.0007	0.0010	0.0020

B	0.0007	0.0008	0.0013	0.0018
C	0.0006	0.0007	0.0009	0.0019
D	0.0006	0.0007	0.0009	0.0018
E	0.0007	0.0008	0.0010	0.0020
F	0.0007	0.0008	0.0010	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0503	0.0477	3.2106	1.6918
A to Z ↑	0.0307	0.0297	4.6586	2.3773
B to Z ↓	0.0464	0.0443	3.1942	1.6841
B to Z ↑	0.0317	0.0310	4.6554	2.3768
C to Z ↓	0.0460	0.0441	3.2026	1.6887
C to Z ↑	0.0277	0.0268	4.6299	2.3637
D to Z ↓	0.0440	0.0422	3.1941	1.6840
D to Z ↑	0.0298	0.0288	4.6308	2.3635
E to Z ↓	0.0388	0.0382	3.1892	1.6825
E to Z ↑	0.0234	0.0228	4.6076	2.3528
F to Z ↓	0.0364	0.0358	3.1817	1.6779
F to Z ↑	0.0250	0.0244	4.6083	2.3522
	X17_P4	X33_P4	X17_P4	X33_P4
A to Z ↓	0.0453	0.0437	0.8541	0.4368
A to Z ↑	0.0279	0.0279	1.1772	0.5956
B to Z ↓	0.0427	0.0415	0.8497	0.4365
B to Z ↑	0.0297	0.0296	1.1766	0.5953
C to Z ↓	0.0426	0.0409	0.8523	0.4367
C to Z ↑	0.0253	0.0258	1.1712	0.5919
D to Z ↓	0.0402	0.0389	0.8496	0.4361
D to Z ↑	0.0271	0.0275	1.1708	0.5922
E to Z ↓	0.0368	0.0372	0.8488	0.4357
E to Z ↑	0.0214	0.0224	1.1659	0.5903
F to Z ↓	0.0345	0.0346	0.8463	0.4344
F to Z ↑	0.0230	0.0240	1.1662	0.5906

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	2.035e-06	1.000e-20
X8_P4	3.967e-06	1.000e-20
X17_P4	7.514e-06	1.000e-20
X33_P4	1.422e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	3.866e-05	4.419e-05	5.741e-05	1.112e-04
B (output stable)	1.120e-04	1.259e-04	1.440e-04	1.812e-04
C (output stable)	3.243e-05	3.929e-05	5.266e-05	1.028e-04
D (output stable)	4.255e-05	5.299e-05	7.284e-05	1.824e-04
E (output stable)	5.484e-05	6.603e-05	8.946e-05	1.476e-04
F (output stable)	6.239e-05	7.630e-05	1.098e-04	2.180e-04

A to Z	3.504e-03	4.690e-03	7.170e-03	1.359e-02
B to Z	3.222e-03	4.362e-03	6.728e-03	1.296e-02
C to Z	2.974e-03	4.059e-03	6.327e-03	1.199e-02
D to Z	2.855e-03	3.908e-03	6.077e-03	1.143e-02
E to Z	2.414e-03	3.429e-03	5.386e-03	1.057e-02
F to Z	2.293e-03	3.272e-03	5.153e-03	1.001e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

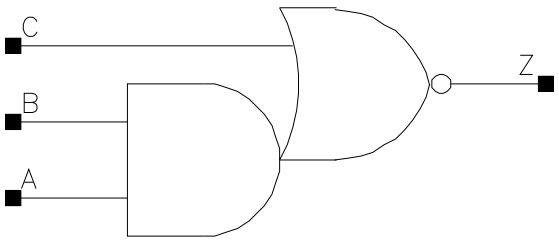
Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008
X44_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X33_P4	X44_P4
A	0.0008	0.0024	0.0048	0.0064
B	0.0008	0.0022	0.0044	0.0059
C	0.0009	0.0025	0.0049	0.0065

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0087	0.0091	2.9873	1.0143
A to Z ↑	0.0149	0.0152	4.6732	1.5699
B to Z ↓	0.0089	0.0092	3.0169	1.0285
B to Z ↑	0.0123	0.0121	4.5949	1.5692
C to Z ↓	0.0090	0.0092	1.7338	0.5973
C to Z ↑	0.0149	0.0149	4.2686	1.4474
	X33_P4	**X44_P4**	**X33_P4**	**X44_P4**
A to Z ↓	0.0093	0.0092	0.5173	0.3932

A to Z ↑	0.0152	0.0152	0.7868	0.5985
B to Z ↓	0.0091	0.0092	0.5245	0.3988
B to Z ↑	0.0120	0.0120	0.7848	0.5948
C to Z ↓	0.0105	0.0107	0.3549	0.2760
C to Z ↑	0.0151	0.0150	0.7241	0.5496

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P4	2.538e-06	1.000e-20
X17_P4	7.326e-06	1.000e-20
X33_P4	1.416e-05	1.000e-20
X44_P4	1.879e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	4.675e-05	1.437e-04	3.117e-04	4.076e-04
B (output stable)	6.356e-05	2.549e-04	5.482e-04	7.080e-04
C (output stable)	1.003e-04	3.017e-04	6.660e-04	8.783e-04
A to Z	1.267e-03	3.985e-03	8.027e-03	1.059e-02
B to Z	1.063e-03	3.124e-03	6.239e-03	8.230e-03
C to Z	1.709e-03	5.089e-03	1.030e-02	1.354e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

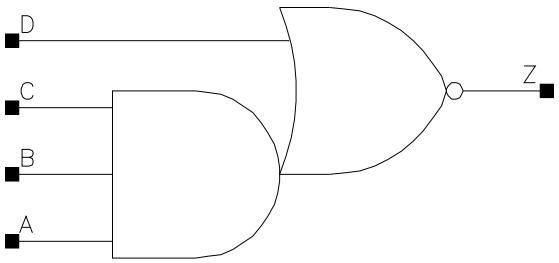
Pin Cycle (vdds)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X29_P4	1.200	3.536	4.2432
X38_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X29_P4	X38_P4
A	0.0008	0.0048	0.0064
B	0.0008	0.0046	0.0060
C	0.0008	0.0044	0.0058
D	0.0009	0.0050	0.0062

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X29_P4	X5_P4	X29_P4
A to Z ↓	0.0128	0.0136	4.2257	0.7352
A to Z ↑	0.0190	0.0190	4.6755	0.7777
B to Z ↓	0.0133	0.0135	4.2460	0.7395
B to Z ↑	0.0170	0.0168	4.6797	0.7844
C to Z ↓	0.0131	0.0129	4.2638	0.7442
C to Z ↑	0.0146	0.0140	4.6087	0.7906
D to Z ↓	0.0109	0.0125	1.7733	0.3574

D to Z ↑	0.0174	0.0177	3.9992	0.6736
	X38_P4		**X38_P4**	
A to Z ↓	0.0134		0.5706	
A to Z ↑	0.0186		0.5871	
B to Z ↓	0.0134		0.5745	
B to Z ↑	0.0164		0.5937	
C to Z ↓	0.0128		0.5781	
C to Z ↑	0.0137		0.6011	
D to Z ↓	0.0133		0.2980	
D to Z ↑	0.0173		0.5094	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	2.509e-06	1.000e-20
X29_P4	1.389e-05	1.000e-20
X38_P4	1.817e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X29_P4	X38_P4
A (output stable)	2.762e-05	2.056e-04	2.646e-04
B (output stable)	5.065e-05	4.199e-04	5.398e-04
C (output stable)	8.430e-05	8.061e-04	1.022e-03
D (output stable)	1.217e-04	9.066e-04	1.182e-03
A to Z	1.811e-03	1.130e-02	1.444e-02
B to Z	1.578e-03	9.387e-03	1.203e-02
C to Z	1.366e-03	7.551e-03	9.668e-03
D to Z	2.194e-03	1.331e-02	1.708e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

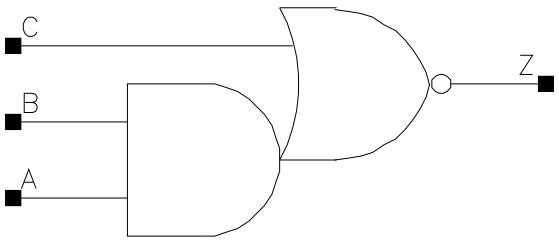
Pin Cycle (vdds)	X5_P4	X29_P4	X38_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X11_P4	1.200	1.088	1.3056
X16_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X11_P4	X16_P4	X23_P4
A	0.0009	0.0017	0.0026	0.0034
B	0.0009	0.0016	0.0024	0.0032
C	0.0009	0.0015	0.0023	0.0033
	X46_P4			
A	0.0066			
B	0.0062			
C	0.0064			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X11_P4	X6_P4	X11_P4
A to Z ↓	0.0105	0.0113	2.8811	1.4696
A to Z ↑	0.0163	0.0171	4.6621	2.2801
B to Z ↓	0.0112	0.0114	2.9097	1.4865

B to Z ↑	0.0142	0.0145	4.5961	2.2872
C to Z ↓	0.0062	0.0066	1.7875	1.0553
C to Z ↑	0.0122	0.0118	4.2811	2.1146
	X16_P4	**X23_P4**	**X16_P4**	**X23_P4**
A to Z ↓	0.0108	0.0111	1.0141	0.7638
A to Z ↑	0.0160	0.0163	1.5364	1.1649
B to Z ↓	0.0113	0.0113	1.0272	0.7726
B to Z ↑	0.0133	0.0135	1.5350	1.1694
C to Z ↓	0.0067	0.0059	0.7329	0.4618
C to Z ↑	0.0112	0.0118	1.4241	1.0801
	X46_P4		**X46_P4**	
A to Z ↓	0.0107		0.3925	
A to Z ↑	0.0157		0.6076	
B to Z ↓	0.0111		0.3974	
B to Z ↑	0.0128		0.6056	
C to Z ↓	0.0062		0.2366	
C to Z ↑	0.0119		0.5620	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P4	2.539e-06	1.000e-20
X11_P4	5.168e-06	1.000e-20
X16_P4	7.334e-06	1.000e-20
X23_P4	1.005e-05	1.000e-20
X46_P4	1.953e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	3.251e-05	8.725e-05	1.138e-04	1.610e-04
B (output stable)	4.997e-05	1.865e-04	2.094e-04	3.212e-04
C (output stable)	1.716e-04	3.952e-04	5.235e-04	7.178e-04
A to Z	1.732e-03	3.779e-03	5.172e-03	7.054e-03
B to Z	1.508e-03	3.131e-03	4.233e-03	5.726e-03
C to Z	1.075e-03	2.168e-03	2.988e-03	4.219e-03
	X46_P4			
A (output stable)	2.857e-04			
B (output stable)	5.660e-04			
C (output stable)	1.251e-03			
A to Z	1.304e-02			
B to Z	1.060e-02			
C to Z	8.050e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

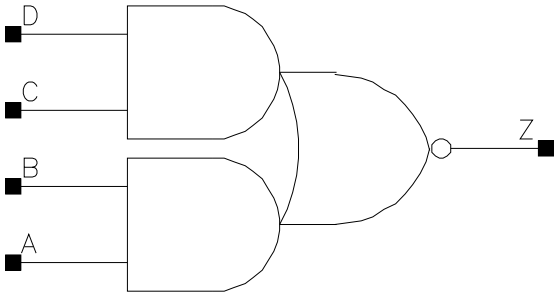
	X46_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P4	X10_P4	X16_P4	X21_P4
A	0.0007	0.0018	0.0026	0.0033
B	0.0007	0.0016	0.0024	0.0032
C	0.0007	0.0017	0.0024	0.0032
D	0.0007	0.0015	0.0022	0.0030
	X42_P4			
A	0.0068			
B	0.0063			
C	0.0064			
D	0.0060			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X10_P4**	**X4_P4**	**X10_P4**
A to Z ↓	0.0118	0.0117	3.5719	1.4103
A to Z ↑	0.0214	0.0179	6.4041	2.1092
B to Z ↓	0.0128	0.0128	3.6124	1.4267
B to Z ↑	0.0192	0.0163	6.3831	2.1651
C to Z ↓	0.0088	0.0084	3.6619	1.4194
C to Z ↑	0.0173	0.0149	6.3856	2.1186
D to Z ↓	0.0092	0.0089	3.7131	1.4404
D to Z ↑	0.0148	0.0128	6.3616	2.1519
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0127	0.0126	1.0184	0.7670
A to Z ↑	0.0187	0.0185	1.4229	1.1043
B to Z ↓	0.0136	0.0131	1.0296	0.7757
B to Z ↑	0.0163	0.0161	1.4223	1.1057
C to Z ↓	0.0092	0.0093	1.0179	0.7679
C to Z ↑	0.0154	0.0157	1.4207	1.1008
D to Z ↓	0.0095	0.0091	1.0328	0.7790
D to Z ↑	0.0127	0.0128	1.4219	1.1024
	X42_P4		**X42_P4**	
A to Z ↓	0.0133		0.3992	
A to Z ↑	0.0188		0.5550	
B to Z ↓	0.0136		0.4038	
B to Z ↑	0.0161		0.5523	
C to Z ↓	0.0098		0.3954	
C to Z ↑	0.0159		0.5546	
D to Z ↓	0.0097		0.4015	
D to Z ↑	0.0130		0.5524	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	1.743e-06	1.000e-20
X10_P4	6.211e-06	1.000e-20
X16_P4	8.714e-06	1.000e-20
X21_P4	1.163e-05	1.000e-20
X42_P4	2.275e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	3.320e-05	7.770e-05	1.472e-04	1.980e-04
B (output stable)	5.592e-05	1.365e-04	3.473e-04	4.993e-04
C (output stable)	4.199e-05	1.155e-04	1.998e-04	2.703e-04
D (output stable)	6.624e-05	1.783e-04	4.016e-04	5.729e-04
A to Z	1.746e-03	4.280e-03	6.703e-03	8.655e-03
B to Z	1.542e-03	3.791e-03	5.738e-03	7.399e-03
C to Z	1.092e-03	2.786e-03	4.351e-03	5.828e-03
D to Z	9.208e-04	2.356e-03	3.482e-03	4.600e-03
	X42_P4			
A (output stable)	3.802e-04			
B (output stable)	9.198e-04			
C (output stable)	5.128e-04			
D (output stable)	1.053e-03			

A to Z	1.702e-02			
B to Z	1.451e-02			
C to Z	1.138e-02			
D to Z	9.073e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

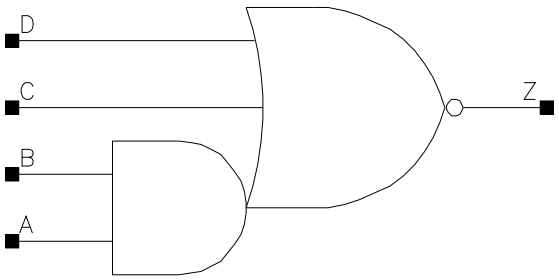
Pin Cycle (vdds)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X35_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P4	X35_P4
A	0.0008	0.0062
B	0.0008	0.0056
C	0.0008	0.0059
D	0.0008	0.0055

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X35_P4	X5_P4	X35_P4
A to Z ↓	0.0102	0.0106	3.0170	0.4467
A to Z ↑	0.0198	0.0185	6.8596	0.8856
B to Z ↓	0.0107	0.0107	3.0558	0.4534
B to Z ↑	0.0167	0.0150	6.8028	0.8844
C to Z ↓	0.0111	0.0145	1.8510	0.3546
C to Z ↑	0.0215	0.0210	6.4692	0.8361
D to Z ↓	0.0106	0.0132	1.8670	0.3544

D to Z ↑	0.0213	0.0199	6.4843	0.8398

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	2.081e-06	1.000e-20
X35_P4	1.532e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X35_P4
A (output stable)	3.961e-05	3.610e-04
B (output stable)	4.680e-05	4.764e-04
C (output stable)	5.862e-05	6.390e-04
D (output stable)	4.934e-05	4.623e-04
A to Z	1.499e-03	1.082e-02
B to Z	1.279e-03	8.667e-03
C to Z	2.245e-03	1.710e-02
D to Z	1.936e-03	1.391e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

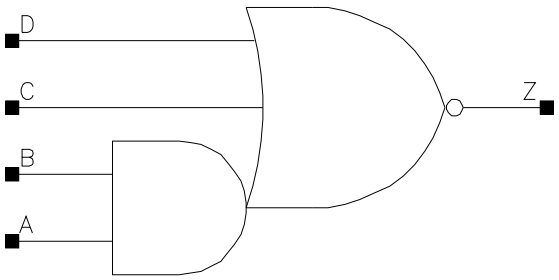
Pin Cycle (vdds)	X5_P4	X35_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X17_P4	1.200	2.448	2.9376
X34_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P4	X17_P4	X34_P4
A	0.0008	0.0034	0.0067
B	0.0008	0.0032	0.0063
C	0.0007	0.0029	0.0056
D	0.0007	0.0026	0.0052

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X17_P4	X4_P4	X17_P4
A to Z ↓	0.0123	0.0134	3.2559	0.8619
A to Z ↑	0.0214	0.0225	6.9080	1.7047
B to Z ↓	0.0134	0.0139	3.2927	0.8716
B to Z ↑	0.0190	0.0192	6.8250	1.7067
C to Z ↓	0.0114	0.0112	2.9260	0.7110
C to Z ↑	0.0158	0.0167	6.5186	1.6183

D to Z ↓	0.0095	0.0085	2.9848	0.7155
D to Z ↑	0.0147	0.0135	6.5422	1.6255
	X34_P4		**X34_P4**	
A to Z ↓	0.0132		0.4424	
A to Z ↑	0.0220		0.8717	
B to Z ↓	0.0139		0.4476	
B to Z ↑	0.0189		0.8675	
C to Z ↓	0.0116		0.3791	
C to Z ↑	0.0162		0.8254	
D to Z ↓	0.0089		0.3826	
D to Z ↑	0.0133		0.8293	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	1.995e-06	1.000e-20
X17_P4	7.923e-06	1.000e-20
X34_P4	1.556e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X17_P4	X34_P4
A (output stable)	3.058e-05	1.456e-04	2.870e-04
B (output stable)	3.613e-05	2.175e-04	4.125e-04
C (output stable)	4.479e-05	2.660e-04	5.027e-04
D (output stable)	7.248e-05	4.571e-04	8.429e-04
A to Z	2.086e-03	9.006e-03	1.736e-02
B to Z	1.867e-03	7.679e-03	1.489e-02
C to Z	1.319e-03	5.728e-03	1.089e-02
D to Z	1.031e-03	3.954e-03	7.535e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

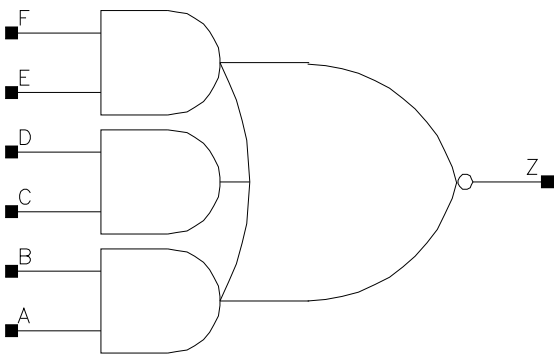
Pin Cycle (vdds)	X4_P4	X17_P4	X34_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X8_P4	1.200	2.176	2.6112
X13_P4	1.200	2.720	3.2640
X17_P4	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P4	X8_P4	X13_P4	X17_P4
A	0.0008	0.0016	0.0025	0.0033

B	0.0008	0.0016	0.0024	0.0031
C	0.0008	0.0016	0.0024	0.0031
D	0.0008	0.0015	0.0022	0.0029
E	0.0010	0.0016	0.0023	0.0030
F	0.0008	0.0014	0.0021	0.0028

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0146	0.0174	2.8858	1.6697
A to Z ↑	0.0309	0.0303	6.6337	3.0797
B to Z ↓	0.0162	0.0183	2.9163	1.6833
B to Z ↑	0.0284	0.0275	6.6209	3.0858
C to Z ↓	0.0131	0.0155	2.8688	1.6867
C to Z ↑	0.0272	0.0274	6.6786	3.0957
D to Z ↓	0.0143	0.0166	2.9062	1.7051
D to Z ↑	0.0246	0.0245	6.6368	3.0946
E to Z ↓	0.0099	0.0118	2.8359	1.6904
E to Z ↑	0.0216	0.0216	6.6019	3.0725
F to Z ↓	0.0105	0.0122	2.8851	1.7162
F to Z ↑	0.0189	0.0183	6.6489	3.0756
	X13_P4	X17_P4	X13_P4	X17_P4
A to Z ↓	0.0166	0.0168	1.1356	0.8669
A to Z ↑	0.0281	0.0283	2.0322	1.5603
B to Z ↓	0.0179	0.0178	1.1448	0.8740
B to Z ↑	0.0257	0.0255	2.0392	1.5600
C to Z ↓	0.0148	0.0149	1.1439	0.8598
C to Z ↑	0.0251	0.0255	2.0462	1.5729
D to Z ↓	0.0161	0.0156	1.1555	0.8689
D to Z ↑	0.0226	0.0226	2.0486	1.5690
E to Z ↓	0.0113	0.0112	1.1407	0.8618
E to Z ↑	0.0201	0.0202	2.0355	1.5573
F to Z ↓	0.0118	0.0113	1.1569	0.8746
F to Z ↑	0.0171	0.0171	2.0386	1.5643

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	3.228e-06	1.000e-20
X8_P4	6.877e-06	1.000e-20
X13_P4	9.790e-06	1.000e-20
X17_P4	1.302e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	5.239e-05	1.196e-04	1.678e-04	2.261e-04
B (output stable)	6.867e-05	2.350e-04	2.771e-04	4.279e-04
C (output stable)	5.047e-05	1.160e-04	1.595e-04	2.222e-04
D (output stable)	6.943e-05	2.370e-04	2.718e-04	4.173e-04
E (output stable)	6.806e-05	1.678e-04	2.373e-04	3.208e-04
F (output stable)	9.017e-05	2.813e-04	3.514e-04	5.150e-04

A to Z	3.303e-03	6.948e-03	9.615e-03	1.278e-02
B to Z	3.040e-03	6.291e-03	8.745e-03	1.145e-02
C to Z	2.501e-03	5.482e-03	7.363e-03	9.834e-03
D to Z	2.270e-03	4.871e-03	6.575e-03	8.638e-03
E to Z	1.706e-03	3.833e-03	5.119e-03	6.803e-03
F to Z	1.494e-03	3.221e-03	4.338e-03	5.653e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

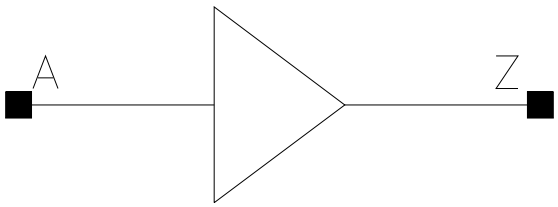
Pin Cycle (vdds)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.408	0.4896
X6_P4	1.200	0.408	0.4896
X8_P4	1.200	0.408	0.4896
X13_P4	1.200	0.544	0.6528
X16_P4	1.200	0.544	0.6528
X21_P4	1.200	0.680	0.8160
X25_P4	1.200	0.680	0.8160
X29_P4	1.200	0.952	1.1424
X33_P4	1.200	0.952	1.1424
X42_P4	1.200	1.088	1.3056
X50_P4	1.200	1.224	1.4688
X58_P4	1.200	1.496	1.7952
X67_P4	1.200	1.632	1.9584
X75_P4	1.200	1.768	2.1216
X84_P4	1.200	1.904	2.2848
X100_P4	1.200	2.312	2.7744
X134_P4	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0008	0.0008	0.0008	0.0008
	X16_P4	X21_P4	X25_P4	X29_P4
A	0.0008	0.0011	0.0011	0.0015
	X33_P4	X42_P4	X50_P4	X58_P4
A	0.0015	0.0017	0.0020	0.0030

	X67_P4	X75_P4	X84_P4	X100_P4
A	0.0030	0.0030	0.0030	0.0040
	X134_P4			
A	0.0050			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0206	0.0208	3.0356	2.2190
A to Z ↑	0.0164	0.0163	4.5547	3.3364
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0217	0.0243	1.6459	1.0615
A to Z ↑	0.0170	0.0192	2.3710	1.5586
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0262	0.0216	0.8450	0.6546
A to Z ↑	0.0203	0.0178	1.1918	0.9368
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0229	0.0219	0.5622	0.4727
A to Z ↑	0.0187	0.0170	0.7830	0.6678
	X33_P4	**X42_P4**	**X33_P4**	**X42_P4**
A to Z ↓	0.0230	0.0224	0.4205	0.3417
A to Z ↑	0.0178	0.0181	0.5847	0.4709
	X50_P4	**X58_P4**	**X50_P4**	**X58_P4**
A to Z ↓	0.0217	0.0204	0.2836	0.2447
A to Z ↑	0.0177	0.0169	0.3907	0.3360
	X67_P4	**X75_P4**	**X67_P4**	**X75_P4**
A to Z ↓	0.0213	0.0226	0.2146	0.1939
A to Z ↑	0.0175	0.0186	0.2946	0.2640
	X84_P4	**X100_P4**	**X84_P4**	**X100_P4**
A to Z ↓	0.0235	0.0220	0.1753	0.1473
A to Z ↑	0.0192	0.0182	0.2384	0.1997
	X134_P4		**X134_P4**	
A to Z ↓	0.0232		0.1144	
A to Z ↑	0.0193		0.1533	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	1.515e-06	1.000e-20
X6_P4	2.039e-06	1.000e-20
X8_P4	2.815e-06	1.000e-20
X13_P4	3.513e-06	1.000e-20
X16_P4	4.899e-06	1.000e-20
X21_P4	6.874e-06	1.000e-20
X25_P4	8.077e-06	1.000e-20
X29_P4	8.730e-06	1.000e-20
X33_P4	9.774e-06	1.000e-20
X42_P4	1.259e-05	1.000e-20
X50_P4	1.545e-05	1.000e-20
X58_P4	1.914e-05	1.000e-20
X67_P4	2.099e-05	1.000e-20
X75_P4	2.283e-05	1.000e-20

X84_P4	2.468e-05	1.000e-20
X100_P4	3.022e-05	1.000e-20
X134_P4	3.945e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	1.727e-03	1.938e-03	2.303e-03	3.086e-03
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	3.750e-03	4.998e-03	5.721e-03	6.390e-03
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	7.116e-03	8.953e-03	1.043e-02	1.279e-02
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	1.417e-02	1.606e-02	1.758e-02	2.093e-02
	X134_P4			
A to Z	2.899e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

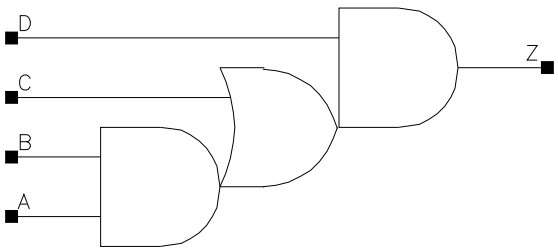
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P4			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.632	1.9584
X25_P4	1.200	1.768	2.1216
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0010	0.0021	0.0021	0.0020
B	0.0010	0.0019	0.0019	0.0018
C	0.0011	0.0023	0.0023	0.0023
D	0.0015	0.0020	0.0020	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0274	0.0260	1.6775	0.8325
A to Z ↑	0.0260	0.0247	2.4081	1.1703
B to Z ↓	0.0253	0.0237	1.6748	0.8331
B to Z ↑	0.0265	0.0247	2.4073	1.1713
C to Z ↓	0.0237	0.0220	1.6726	0.8307
C to Z ↑	0.0197	0.0182	2.3825	1.1601

D to Z ↓	0.0232	0.0205	1.6577	0.8247
D to Z ↑	0.0225	0.0198	2.3877	1.1623
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0284	0.0302	0.5658	0.4259
A to Z ↑	0.0270	0.0285	0.7950	0.5968
B to Z ↓	0.0262	0.0284	0.5656	0.4257
B to Z ↑	0.0272	0.0292	0.7930	0.5964
C to Z ↓	0.0246	0.0267	0.5643	0.4243
C to Z ↑	0.0202	0.0218	0.7856	0.5895
D to Z ↓	0.0222	0.0235	0.5588	0.4189
D to Z ↑	0.0216	0.0229	0.7871	0.5905

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	5.051e-06	1.000e-20
X17_P4	9.988e-06	1.000e-20
X25_P4	1.225e-05	1.000e-20
X33_P4	1.452e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	1.057e-04	2.076e-04	2.070e-04	2.002e-04
B (output stable)	1.265e-04	2.697e-04	2.690e-04	2.345e-04
C (output stable)	3.394e-04	5.740e-04	5.726e-04	5.517e-04
D (output stable)	9.674e-05	1.282e-04	1.294e-04	1.291e-04
A to Z	3.809e-03	7.014e-03	8.776e-03	1.040e-02
B to Z	3.559e-03	6.366e-03	8.130e-03	9.880e-03
C to Z	3.054e-03	5.344e-03	7.030e-03	8.639e-03
D to Z	3.896e-03	6.813e-03	8.433e-03	9.916e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

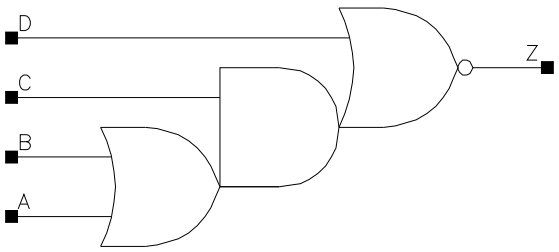
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.952	1.1424
X11_P4	1.200	1.496	1.7952
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X16_P4	X21_P4
A	0.0009	0.0017	0.0026	0.0033
B	0.0009	0.0016	0.0025	0.0033
C	0.0009	0.0016	0.0024	0.0033
D	0.0011	0.0016	0.0024	0.0032

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0130	0.0125	2.8443	1.4989
A to Z ↑	0.0258	0.0239	6.7707	3.5493
B to Z ↓	0.0124	0.0120	2.7709	1.4714
B to Z ↑	0.0247	0.0234	6.7864	3.5555
C to Z ↓	0.0119	0.0114	2.6348	1.3910
C to Z ↑	0.0162	0.0149	4.5795	2.3614

D to Z ↓	0.0069	0.0058	1.7333	0.8771
D to Z ↑	0.0150	0.0131	4.9043	2.5368
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0124	0.0127	1.0073	0.7782
A to Z ↑	0.0221	0.0235	2.2649	1.7576
B to Z ↓	0.0116	0.0120	1.0154	0.7808
B to Z ↑	0.0220	0.0227	2.2692	1.7612
C to Z ↓	0.0115	0.0116	0.9538	0.7327
C to Z ↑	0.0142	0.0145	1.5583	1.1704
D to Z ↓	0.0058	0.0059	0.6114	0.4667
D to Z ↑	0.0122	0.0122	1.6585	1.2578

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	2.862e-06	1.000e-20
X11_P4	5.443e-06	1.000e-20
X16_P4	7.748e-06	1.000e-20
X21_P4	1.021e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	3.577e-05	6.420e-05	8.405e-05	1.375e-04
B (output stable)	1.915e-05	3.706e-05	5.093e-05	7.347e-05
C (output stable)	1.138e-04	2.286e-04	3.143e-04	4.418e-04
D (output stable)	1.728e-04	3.557e-04	5.152e-04	7.086e-04
A to Z	2.681e-03	4.697e-03	6.560e-03	9.198e-03
B to Z	2.209e-03	3.928e-03	5.636e-03	7.623e-03
C to Z	1.895e-03	3.293e-03	4.681e-03	6.406e-03
D to Z	1.284e-03	2.234e-03	3.066e-03	4.082e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

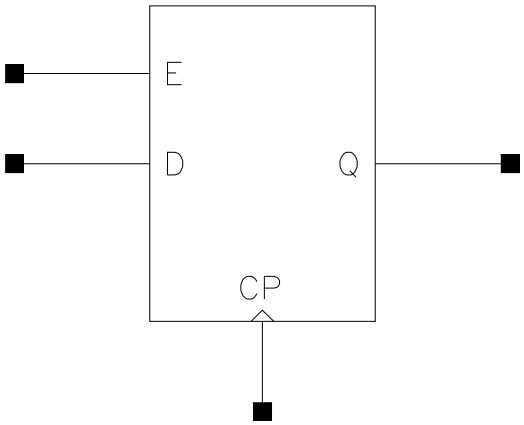
Pin Cycle (vdds)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.128	3.7536
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0011	0.0009	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0325	0.0371	1.6602	0.8560
CP to Q ↑	0.0405	0.0432	2.4226	1.2134
	X33_P4		**X33_P4**	
CP to Q ↓	0.0553		0.4258	
CP to Q ↑	0.0679		0.6013	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0433	0.0433	0.0433
CP ↑	min_pulse_width to CP	0.0270	0.0317	0.0270
D ↓	hold_rising to CP	-0.0093	-0.0093	-0.0093
D ↑	hold_rising to CP	0.0010	0.0010	-0.0017
D ↓	setup_rising to CP	0.0415	0.0415	0.0415
D ↑	setup_rising to CP	0.0265	0.0265	0.0265
E ↓	hold_rising to CP	-0.0040	-0.0040	-0.0040
E ↑	hold_rising to CP	-0.0022	-0.0022	-0.0022
E ↓	setup_rising to CP	0.0489	0.0489	0.0489
E ↑	setup_rising to CP	0.0440	0.0440	0.0440

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	9.666e-06	1.000e-20
X17_P4	1.157e-05	1.000e-20
X33_P4	1.786e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

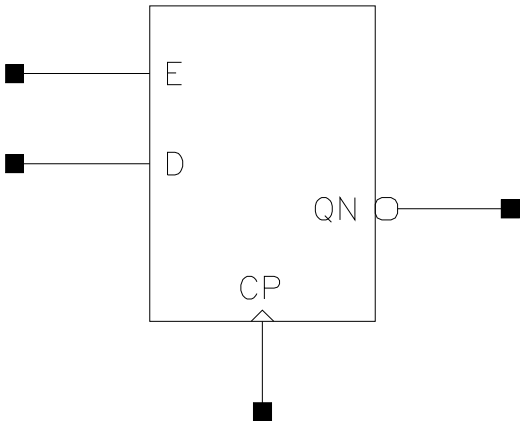
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	8.105e-03	8.106e-03	8.115e-03
Clock 100Mhz Data 25Mhz	1.064e-02	1.146e-02	1.418e-02
Clock 100Mhz Data 50Mhz	1.318e-02	1.482e-02	2.024e-02
Clock = 0 Data 100Mhz	5.133e-03	5.133e-03	5.133e-03
Clock = 1 Data 100Mhz	1.441e-03	1.441e-03	1.441e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.264	3.9168
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0009	0.0011	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0556	0.0525	1.7120	0.8202
CP to QN ↑	0.0434	0.0442	2.4573	1.1751
	X33_P4		**X33_P4**	
CP to QN ↓	0.0561		0.4273	
CP to QN ↑	0.0485		0.6029	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0433	0.0433	0.0433
CP ↑	min_pulse_width to CP	0.0270	0.0270	0.0283
D ↓	hold_rising to CP	-0.0093	-0.0093	-0.0093
D ↑	hold_rising to CP	-0.0017	0.0010	0.0010
D ↓	setup_rising to CP	0.0415	0.0415	0.0415
D ↑	setup_rising to CP	0.0265	0.0265	0.0265
E ↓	hold_rising to CP	-0.0040	-0.0040	-0.0040
E ↑	hold_rising to CP	-0.0022	-0.0022	-0.0022
E ↓	setup_rising to CP	0.0489	0.0489	0.0489
E ↑	setup_rising to CP	0.0440	0.0440	0.0440

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	9.578e-06	1.000e-20
X17_P4	1.308e-05	1.000e-20
X33_P4	1.736e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

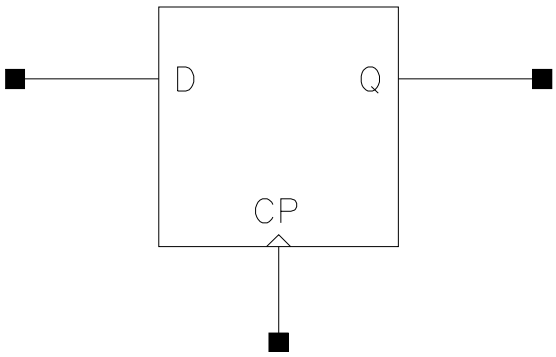
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	8.103e-03	8.105e-03	8.106e-03
Clock 100Mhz Data 25Mhz	1.068e-02	1.190e-02	1.403e-02
Clock 100Mhz Data 50Mhz	1.326e-02	1.569e-02	1.996e-02
Clock = 0 Data 100Mhz	5.132e-03	5.133e-03	5.133e-03
Clock = 1 Data 100Mhz	1.441e-03	1.441e-03	1.441e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.176	2.6112
X17_P4	1.200	2.448	2.9376
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0338	0.0372	1.6492	0.8484
CP to Q ↑	0.0408	0.0452	2.3358	1.1882
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to Q ↓	0.0465	0.0480	0.4999	0.4546
CP to Q ↑	0.0509	0.0521	0.6715	0.6103

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0385	0.0385	0.0385	0.0385
CP ↑	min_pulse_width to CP	0.0270	0.0317	0.0376	0.0411
D ↓	hold_rising to CP	0.0124	0.0124	0.0124	0.0124
D ↑	hold_rising to CP	0.0124	0.0097	0.0124	0.0124
D ↓	setup_rising to CP	0.0224	0.0224	0.0224	0.0224
D ↑	setup_rising to CP	0.0151	0.0151	0.0151	0.0151

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	7.453e-06	1.000e-20
X17_P4	9.604e-06	1.000e-20
X30_P4	1.267e-05	1.000e-20
X33_P4	1.332e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

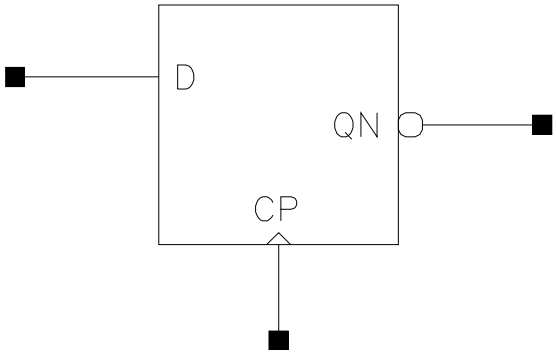
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	8.492e-03	8.540e-03	8.559e-03	8.567e-03
Clock 100Mhz Data 25Mhz	9.753e-03	1.093e-02	1.285e-02	1.330e-02
Clock 100Mhz Data 50Mhz	1.101e-02	1.332e-02	1.715e-02	1.804e-02
Clock = 0 Data 100Mhz	3.419e-03	3.523e-03	3.554e-03	3.570e-03
Clock = 1 Data 100Mhz	2.708e-05	2.704e-05	2.715e-05	2.721e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0330	0.0387	1.7045	0.8747
CP to QN ↑	0.0349	0.0370	2.3326	1.1889
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to QN ↓	0.0557	0.0561	0.4691	0.4256
CP to QN ↑	0.0454	0.0519	0.6481	0.6025

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0385	0.0385	0.0385	0.0385
CP ↑	min_pulse_width to CP	0.0269	0.0316	0.0270	0.0316
D ↓	hold_rising to CP	0.0150	0.0146	0.0124	0.0124
D ↑	hold_rising to CP	0.0156	0.0156	0.0097	0.0124
D ↓	setup_rising to CP	0.0175	0.0175	0.0224	0.0224
D ↑	setup_rising to CP	0.0146	0.0146	0.0151	0.0151

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	7.031e-06	1.000e-20
X17_P4	8.951e-06	1.000e-20
X30_P4	1.443e-05	1.000e-20
X33_P4	1.516e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

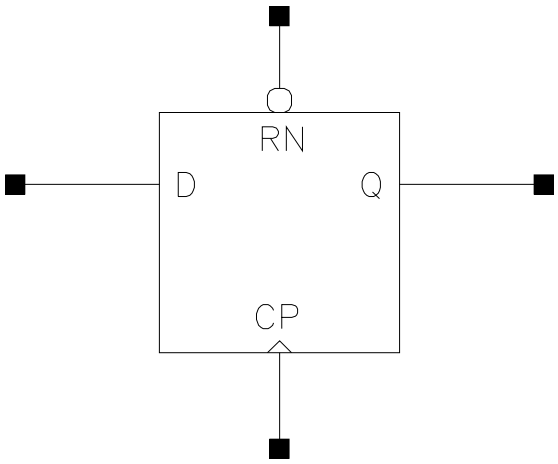
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	8.166e-03	8.168e-03	8.303e-03	8.361e-03
Clock 100Mhz Data 25Mhz	9.302e-03	1.021e-02	1.243e-02	1.312e-02
Clock 100Mhz Data 50Mhz	1.044e-02	1.225e-02	1.656e-02	1.787e-02
Clock = 0 Data 100Mhz	3.027e-03	3.027e-03	3.225e-03	3.275e-03
Clock = 1 Data 100Mhz	2.682e-05	2.687e-05	2.705e-05	2.708e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0388	0.0479	0.8556	0.5087
CP to Q ↑	0.0466	0.0521	1.1923	0.6745
RN to Q ↓	0.0623	0.0814	0.8907	0.5268

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0433	0.0433
CP ↑	min_pulse_width to CP	0.0316	0.0410
D ↓	hold_rising to CP	0.0124	0.0124
D ↑	hold_rising to CP	0.0103	0.0098
D ↓	setup_rising to CP	0.0220	0.0220
D ↑	setup_rising to CP	0.0142	0.0142
RN ↓	min_pulse_width to RN	0.0757	0.0974
RN ↑	recovery_rising to CP	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0055	-0.0055

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P4	1.094e-05	1.000e-20
X30_P4	1.458e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

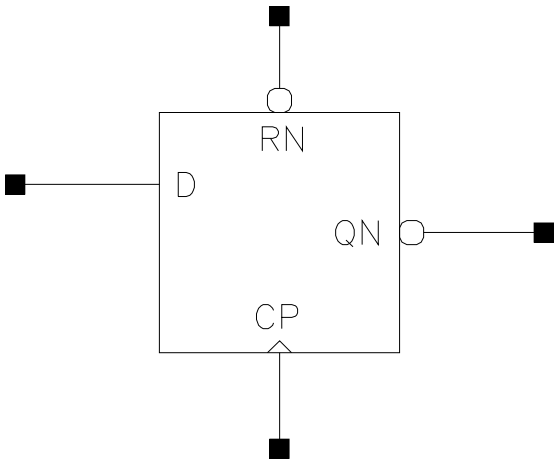
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	9.074e-03	9.073e-03
Clock 100Mhz Data 25Mhz	1.164e-02	1.352e-02
Clock 100Mhz Data 50Mhz	1.420e-02	1.797e-02
Clock = 0 Data 100Mhz	4.184e-03	4.187e-03
Clock = 1 Data 100Mhz	2.732e-05	2.743e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0538	0.0579	0.8149	0.4704
CP to QN ↑	0.0441	0.0475	1.1635	0.6519
RN to QN ↑	0.0640	0.0684	1.1669	0.6538

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0433	0.0433
CP ↑	min_pulse_width to CP	0.0269	0.0269
D ↓	hold_rising to CP	0.0134	0.0128
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0219	0.0219
D ↑	setup_rising to CP	0.0142	0.0142
RN ↓	min_pulse_width to RN	0.0610	0.0659
RN ↑	recovery_rising to CP	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0055	-0.0055

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P4	1.182e-05	1.000e-20
X30_P4	1.424e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

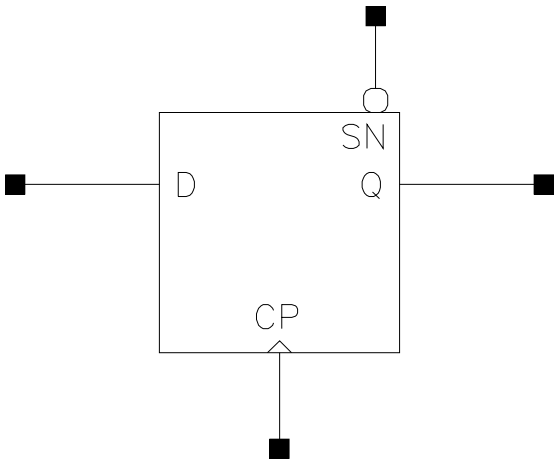
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	9.074e-03	9.073e-03
Clock 100Mhz Data 25Mhz	1.202e-02	1.343e-02
Clock 100Mhz Data 50Mhz	1.496e-02	1.779e-02
Clock = 0 Data 100Mhz	4.233e-03	4.220e-03
Clock = 1 Data 100Mhz	2.719e-05	2.735e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0388	0.0486	0.8573	0.5057
CP to Q ↑	0.0461	0.0521	1.1934	0.6746
SN to Q ↑	0.0469	0.0544	1.1954	0.6746

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0432	0.0433
CP ↑	min_pulse_width to CP	0.0316	0.0410
D ↓	hold_rising to CP	0.0134	0.0134
D ↑	hold_rising to CP	0.0098	0.0097
D ↓	setup_rising to CP	0.0273	0.0273
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0452	0.0527
SN ↑	recovery_rising to CP	0.0054	0.0054
SN ↑	removal_rising to CP	0.0211	0.0211

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P4	9.800e-06	1.000e-20
X30_P4	1.228e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

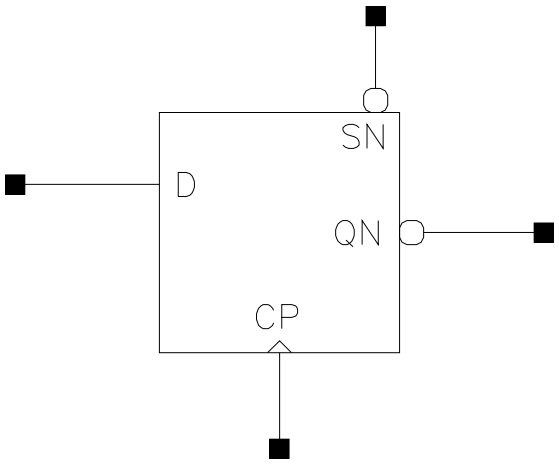
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	9.167e-03	9.152e-03
Clock 100Mhz Data 25Mhz	1.172e-02	1.361e-02
Clock 100Mhz Data 50Mhz	1.428e-02	1.807e-02
Clock = 0 Data 100Mhz	4.153e-03	4.152e-03
Clock = 1 Data 100Mhz	2.746e-05	2.751e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0534	0.0575	0.8167	0.4718
CP to QN ↑	0.0444	0.0477	1.1603	0.6500
SN to QN ↓	0.0535	0.0578	0.8174	0.4716

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0432	0.0432
CP ↑	min_pulse_width to CP	0.0269	0.0269
D ↓	hold_rising to CP	0.0134	0.0134
D ↑	hold_rising to CP	0.0098	0.0098
D ↓	setup_rising to CP	0.0273	0.0273
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0403	0.0403
SN ↑	recovery_rising to CP	0.0028	0.0028
SN ↑	removal_rising to CP	0.0211	0.0211

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P4	1.262e-05	1.000e-20
X30_P4	1.617e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

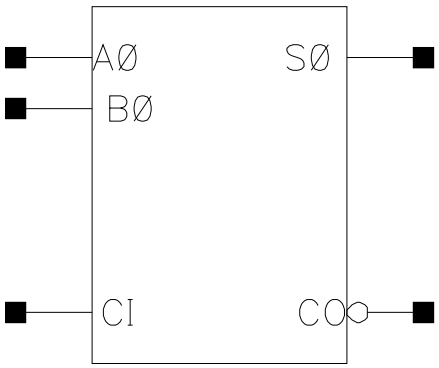
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	9.165e-03	9.159e-03
Clock 100Mhz Data 25Mhz	1.208e-02	1.349e-02
Clock 100Mhz Data 50Mhz	1.499e-02	1.782e-02
Clock = 0 Data 100Mhz	4.154e-03	4.153e-03
Clock = 1 Data 100Mhz	2.743e-05	2.756e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_P4	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_-P4	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_-P4	1.200	3.672	4.4064
C12T28SOI_LLS1_-FA1X33_P4	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4
A0	0.0032	0.0065	0.0029	0.0057
B0	0.0029	0.0063	0.0031	0.0055
CI	0.0021	0.0048	0.0022	0.0039

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P4	**C12T28SOI_LL_-FA1X33_P4**	**C12T28SOI_LL_-FA1X8_P4**	**C12T28SOI_LL_-FA1X33_P4**
A0 to CO ↓	0.0360	0.0392	1.7220	0.4531
A0 to CO ↑	0.0278	0.0291	2.4154	0.6224
A0 to S0 ↓	0.0378	0.0476	1.7044	0.4423
A0 to S0 ↑	0.0387	0.0473	2.3857	0.6145
B0 to CO ↓	0.0355	0.0396	1.7274	0.4553
B0 to CO ↑	0.0285	0.0303	2.4166	0.6203
B0 to S0 ↓	0.0381	0.0485	1.7061	0.4423
B0 to S0 ↑	0.0389	0.0481	2.3871	0.6146
CI to CO ↓	0.0349	0.0392	1.7304	0.4539
CI to CO ↑	0.0285	0.0296	2.4156	0.6226
CI to S0 ↓	0.0378	0.0481	1.7061	0.4424
CI to S0 ↑	0.0390	0.0484	2.3859	0.6140
	C12T28SOI_LLS1_-FA1X8_P4	**C12T28SOI_LLS1_-FA1X33_P4**	**C12T28SOI_LLS1_-FA1X8_P4**	**C12T28SOI_LLS1_-FA1X33_P4**
A0 to CO ↓	0.0241	0.0295	3.3376	0.5757
A0 to CO ↑	0.0213	0.0246	2.4615	0.6149
A0 to S0 ↓	0.0502	0.0617	1.8470	0.4635
A0 to S0 ↑	0.0462	0.0500	2.4840	0.6252
B0 to CO ↓	0.0249	0.0306	3.3393	0.5762
B0 to CO ↑	0.0198	0.0235	2.4594	0.6150
B0 to S0 ↓	0.0504	0.0632	1.8473	0.4634
B0 to S0 ↑	0.0463	0.0513	2.4855	0.6255
CI to CO ↓	0.0248	0.0423	3.3339	0.5827
CI to CO ↑	0.0219	0.0265	2.5314	0.6198
CI to S0 ↓	0.0297	0.0384	1.8493	0.4640
CI to S0 ↑	0.0253	0.0256	2.4839	0.6260

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_FA1X8_P4	1.059e-05	1.000e-20
C12T28SOI_LL_FA1X33_P4	2.875e-05	1.000e-20
C12T28SOI_LLS1_FA1X8_P4	2.339e-05	1.000e-20
C12T28SOI_LLS1_FA1X33_P4	4.773e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4
A0 to CO	3.954e-03	1.153e-02	6.081e-03	1.525e-02
A0 to S0	3.991e-03	1.199e-02	8.172e-03	1.894e-02
B0 to CO	3.982e-03	1.172e-02	6.110e-03	1.543e-02
B0 to S0	3.905e-03	1.190e-02	8.273e-03	1.928e-02
CI to CO	3.987e-03	1.179e-02	4.348e-03	1.377e-02
CI to S0	3.879e-03	1.185e-02	4.918e-03	1.481e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00

A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X33_P4	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X33_P4
A0	0.0011	0.0032
B0	0.0010	0.0028

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
A0 to CO ↓	0.0281	0.0257	1.7083	0.4254
A0 to CO ↑	0.0255	0.0235	2.3834	0.6164
A0 to S0 ↓	0.0355	0.0339	1.6736	0.4248
A0 to S0 ↑	0.0344	0.0384	2.3517	0.6074
B0 to CO ↓	0.0272	0.0237	1.7074	0.4223
B0 to CO ↑	0.0275	0.0248	2.3847	0.6164
B0 to S0 ↓	0.0370	0.0341	1.6735	0.4248
B0 to S0 ↑	0.0337	0.0368	2.3519	0.6073

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	6.480e-06	1.000e-20
X33_P4	2.938e-05	1.000e-20

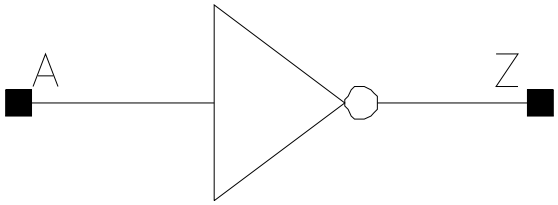
Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X33_P4
A0 to CO	3.046e-03	1.013e-02
A0 to S0	2.828e-03	9.935e-03
B0 to CO	3.084e-03	1.025e-02
B0 to S0	2.790e-03	9.646e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X8_P4	X33_P4
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.272	0.3264
X6_P4	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X13_P4	1.200	0.408	0.4896
X17_P4	1.200	0.408	0.4896
X21_P4	1.200	0.544	0.6528
X25_P4	1.200	0.544	0.6528
X29_P4	1.200	0.680	0.8160
X33_P4	1.200	0.680	0.8160
X50_P4	1.200	0.952	1.1424
X58_P4	1.200	1.088	1.3056
X67_P4	1.200	1.224	1.4688
X75_P4	1.200	1.360	1.6320
X84_P4	1.200	1.496	1.7952
X100_P4	1.200	1.768	2.1216
X134_P4	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0006	0.0007	0.0009	0.0013
	X17_P4	X21_P4	X25_P4	X29_P4
A	0.0016	0.0021	0.0025	0.0030
	X33_P4	X50_P4	X58_P4	X67_P4
A	0.0033	0.0050	0.0058	0.0066
	X75_P4	X84_P4	X100_P4	X134_P4

A	0.0076	0.0086	0.0105	0.0146

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0061	0.0058	3.2357	2.4852
A to Z ↑	0.0105	0.0095	4.7140	3.5437
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0052	0.0044	1.7064	1.1057
A to Z ↑	0.0085	0.0078	2.4378	1.6158
	X17_P4	**X21_P4**	**X17_P4**	**X21_P4**
A to Z ↓	0.0044	0.0048	0.8487	0.6841
A to Z ↑	0.0074	0.0079	1.2007	0.9711
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0048	0.0045	0.5823	0.4934
A to Z ↑	0.0075	0.0073	0.8088	0.6929
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0045	0.0046	0.4379	0.2958
A to Z ↑	0.0070	0.0070	0.6061	0.4060
	X58_P4	**X67_P4**	**X58_P4**	**X67_P4**
A to Z ↓	0.0049	0.0048	0.2567	0.2256
A to Z ↑	0.0073	0.0071	0.3504	0.3073
	X75_P4	**X84_P4**	**X75_P4**	**X84_P4**
A to Z ↓	0.0054	0.0055	0.2037	0.1846
A to Z ↑	0.0076	0.0077	0.2757	0.2498
	X100_P4	**X134_P4**	**X100_P4**	**X134_P4**
A to Z ↓	0.0062	0.0070	0.1575	0.1232
A to Z ↑	0.0083	0.0090	0.2113	0.1633

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	7.873e-07	1.000e-20
X6_P4	1.201e-06	1.000e-20
X8_P4	2.038e-06	1.000e-20
X13_P4	2.798e-06	1.000e-20
X17_P4	4.191e-06	1.000e-20
X21_P4	4.812e-06	1.000e-20
X25_P4	6.055e-06	1.000e-20
X29_P4	6.830e-06	1.000e-20
X33_P4	7.899e-06	1.000e-20
X50_P4	1.159e-05	1.000e-20
X58_P4	1.343e-05	1.000e-20
X67_P4	1.528e-05	1.000e-20
X75_P4	1.713e-05	1.000e-20
X84_P4	1.897e-05	1.000e-20
X100_P4	2.266e-05	1.000e-20
X134_P4	3.005e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4

A to Z	5.669e-04	7.041e-04	9.391e-04	1.318e-03
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	1.729e-03	2.259e-03	2.655e-03	2.977e-03
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	3.283e-03	4.886e-03	5.894e-03	6.475e-03
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	7.576e-03	8.291e-03	1.023e-02	1.418e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

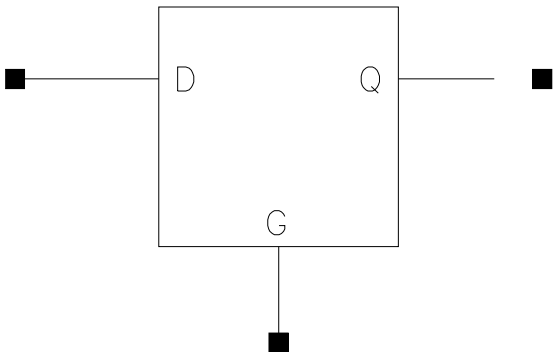
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X23_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P4	X23_P4
D	0.0006	0.0014
G	0.0012	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X23_P4	X8_P4	X23_P4
D to Q ↓	0.0407	0.0319	1.7193	0.8151
D to Q ↑	0.0272	0.0271	2.3483	0.6273
G to Q ↓	0.0420	0.0336	1.7134	0.8142
G to Q ↑	0.0266	0.0244	2.3468	0.6279

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P4	X23_P4
D ↓	hold_falling to G	-0.0013	0.0032
D ↑	hold_falling to G	0.0051	0.0019
D ↓	setup_falling to G	0.0386	0.0264
D ↑	setup_falling to G	0.0302	0.0327
G ↑	min_pulse_width to G	0.0365	0.0362

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	4.225e-06	1.000e-20
X23_P4	1.170e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X23_P4
D (output stable)	1.914e-05	7.727e-05
G (output stable)	1.064e-03	2.115e-03
D to Q	4.898e-03	9.471e-03
G to Q	4.576e-03	8.572e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

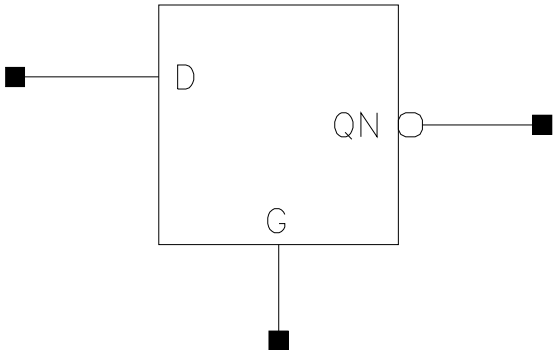
Pin Cycle (vdds)	X8_P4	X23_P4
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P4
D	0.0006
G	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P4	X17_P4
D to QN ↓	0.0353	0.8180
D to QN ↑	0.0449	1.1533
G to QN ↓	0.0340	0.8178
G to QN ↑	0.0449	1.1535

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P4
D ↓	hold_falling to G	-0.0071
D ↑	hold_falling to G	0.0019
D ↓	setup_falling to G	0.0317
D ↑	setup_falling to G	0.0231
G ↑	min_pulse_width to G	0.0283

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P4	7.221e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X17_P4
D (output stable)	1.950e-05
G (output stable)	1.243e-03
D to QN	6.071e-03
G to QN	5.694e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

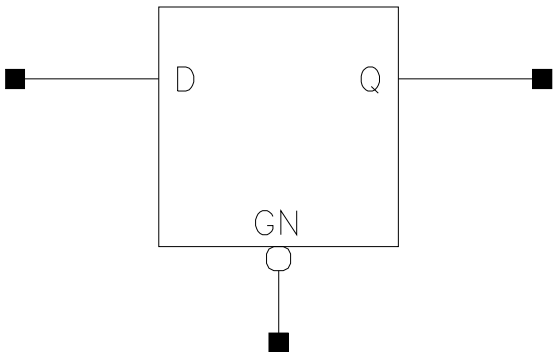
Pin Cycle (vdds)	X17_P4
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
D	0.0005	0.0008	0.0018
GN	0.0011	0.0014	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D to Q ↓	0.0411	0.0355	1.7225	0.8510
D to Q ↑	0.0277	0.0263	2.3503	1.2072
GN to Q ↓	0.0376	0.0319	1.7249	0.8527
GN to Q ↑	0.0398	0.0384	2.3469	1.2038

	X33_P4		X33_P4	
D to Q ↓	0.0346		0.4368	
D to Q ↑	0.0227		0.6058	
GN to Q ↓	0.0304		0.4370	
GN to Q ↑	0.0299		0.6048	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X33_P4
D ↓	hold_rising to GN	-0.0042	-0.0025	-0.0030
D ↑	hold_rising to GN	0.0053	0.0081	0.0106
D ↓	setup_rising to GN	0.0445	0.0397	0.0406
D ↑	setup_rising to GN	0.0265	0.0244	0.0190
GN ↓	min_pulse_width to GN	0.0509	0.0434	0.0424

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	4.278e-06	1.000e-20
X17_P4	7.456e-06	1.000e-20
X33_P4	1.340e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
D (output stable)	1.902e-05	3.117e-05	8.429e-05
GN (output stable)	1.058e-03	1.454e-03	1.880e-03
D to Q	4.919e-03	7.002e-03	1.146e-02
GN to Q	6.917e-03	9.513e-03	1.425e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

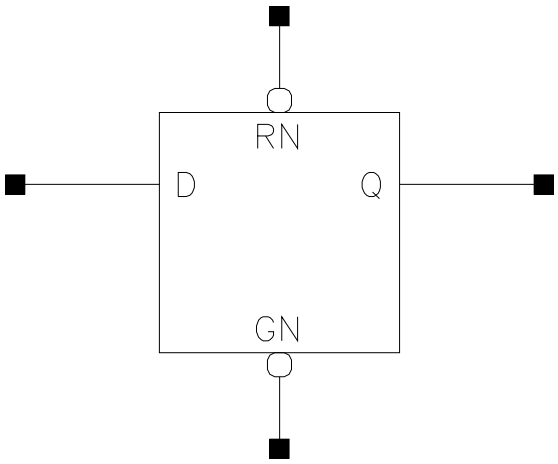
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.496	1.7952
X33_P4	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X33_P4
D	0.0006	0.0014
GN	0.0013	0.0024
RN	0.0006	0.0006

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
D to Q ↓	0.0385	0.0347	1.6835	0.4385
D to Q ↑	0.0355	0.0456	2.3984	0.6257

GN to Q ↓	0.0355	0.0323	1.6863	0.4391
GN to Q ↑	0.0452	0.0474	2.3978	0.6252
RN to Q ↓	0.0322	0.0590	1.6376	0.4683
RN to Q ↑	0.0368	0.0502	2.3957	0.6257

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P4	X33_P4
D ↓	hold_rising to GN	-0.0052	0.0002
D ↑	hold_rising to GN	-0.0017	-0.0110
D ↓	setup_rising to GN	0.0397	0.0349
D ↑	setup_rising to GN	0.0368	0.0513
GN ↓	min_pulse_width to GN	0.0464	0.0496
RN ↓	min_pulse_width to RN	0.0398	0.0686
RN ↑	recovery_rising to GN	0.0362	0.0562
RN ↑	removal_rising to GN	-0.0249	-0.0365

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	5.118e-06	1.000e-20
X33_P4	1.427e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X33_P4
D (output stable)	7.234e-05	9.155e-05
GN (output stable)	1.227e-03	1.918e-03
RN (output stable)	2.872e-05	5.223e-05
D to Q	4.915e-03	1.310e-02
GN to Q	7.068e-03	1.641e-02
RN to Q	3.802e-03	1.058e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

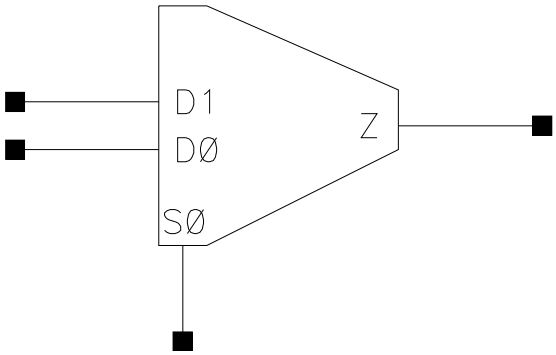
Pin Cycle (vdds)	X8_P4	X33_P4
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
D0	0.0008	0.0011	0.0014	0.0020
D1	0.0007	0.0011	0.0015	0.0020
S0	0.0013	0.0015	0.0017	0.0025

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D0 to Z ↓	0.0322	0.0286	1.7025	0.8354
D0 to Z ↑	0.0259	0.0238	2.4128	1.1796
D1 to Z ↓	0.0306	0.0280	1.6981	0.8341
D1 to Z ↑	0.0236	0.0224	2.4103	1.1800
S0 to Z ↓	0.0279	0.0270	1.6920	0.8312
S0 to Z ↑	0.0263	0.0265	2.4091	1.1784

	X25_P4	X33_P4	X25_P4	X33_P4
D0 to Z ↓	0.0307	0.0275	0.5744	0.4311
D0 to Z ↑	0.0253	0.0235	0.7942	0.5951
D1 to Z ↓	0.0328	0.0286	0.5770	0.4318
D1 to Z ↑	0.0245	0.0228	0.7937	0.5950
S0 to Z ↓	0.0310	0.0284	0.5742	0.4305
S0 to Z ↑	0.0293	0.0269	0.7932	0.5945

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	5.073e-06	1.000e-20
X17_P4	1.071e-05	1.000e-20
X25_P4	1.336e-05	1.000e-20
X33_P4	2.130e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	9.621e-04	1.482e-03	1.660e-03	2.339e-03
D1 (output stable)	8.118e-04	1.400e-03	1.818e-03	2.424e-03
S0 (output stable)	1.223e-03	1.381e-03	1.786e-03	2.242e-03
D0 to Z	3.357e-03	5.576e-03	8.630e-03	1.088e-02
D1 to Z	3.096e-03	5.401e-03	8.709e-03	1.079e-02
S0 to Z	3.850e-03	5.913e-03	9.617e-03	1.181e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

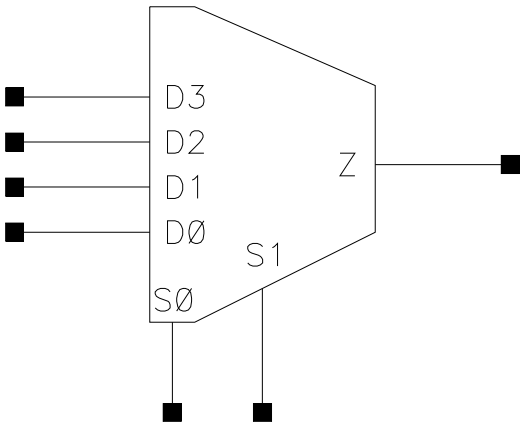
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.312	2.7744
X31_P4	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P4	X31_P4
D0	0.0006	0.0015
D1	0.0006	0.0015
D2	0.0006	0.0015
D3	0.0006	0.0015
S0	0.0019	0.0038
S1	0.0012	0.0024

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X31_P4	X8_P4	X31_P4

D0 to Z ↓	0.0534	0.0547	1.7663	0.4911
D0 to Z ↑	0.0365	0.0390	2.4267	0.6578
D1 to Z ↓	0.0530	0.0548	1.7643	0.4912
D1 to Z ↑	0.0367	0.0389	2.4267	0.6578
D2 to Z ↓	0.0571	0.0515	1.7744	0.4868
D2 to Z ↑	0.0386	0.0359	2.4351	0.6529
D3 to Z ↓	0.0569	0.0509	1.7738	0.4858
D3 to Z ↑	0.0382	0.0373	2.4333	0.6554
S0 to Z ↓	0.0583	0.0594	1.7670	0.4880
S0 to Z ↑	0.0445	0.0473	2.4312	0.6564
S1 to Z ↓	0.0426	0.0422	1.7690	0.4882
S1 to Z ↑	0.0350	0.0370	2.4294	0.6560

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	4.871e-06	1.000e-20
X31_P4	1.690e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X31_P4
D0 (output stable)	2.035e-05	1.092e-04
D1 (output stable)	2.410e-05	1.335e-04
D2 (output stable)	2.863e-05	1.114e-04
D3 (output stable)	2.878e-05	1.426e-04
S0 (output stable)	1.770e-03	3.991e-03
S1 (output stable)	1.410e-03	3.101e-03
D0 to Z	3.696e-03	1.282e-02
D1 to Z	3.683e-03	1.286e-02
D2 to Z	3.952e-03	1.200e-02
D3 to Z	3.938e-03	1.199e-02
S0 to Z	5.650e-03	1.685e-02
S1 to Z	4.296e-03	1.260e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

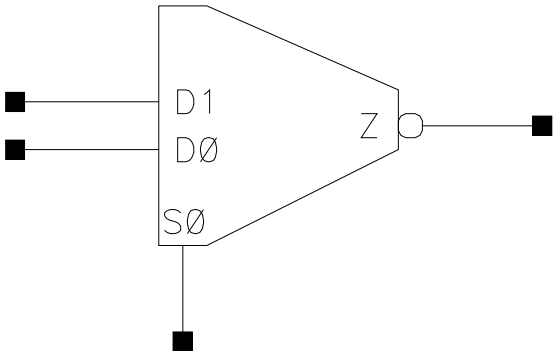
Pin Cycle (vdds)	X8_P4	X31_P4
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.816	0.9792
X5_P4	1.200	0.952	1.1424
X10_P4	1.200	1.768	2.1216
X16_P4	1.200	2.448	2.9376
X21_P4	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P4	X5_P4	X10_P4	X16_P4
D0	0.0005	0.0008	0.0017	0.0026
D1	0.0005	0.0008	0.0016	0.0025
S0	0.0012	0.0020	0.0026	0.0039
	X21_P4			
D0	0.0034			
D1	0.0034			
S0	0.0044			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X5_P4	X3_P4	X5_P4
D0 to Z ↓	0.0114	0.0115	5.3562	3.3648

D0 to Z ↑	0.0187	0.0165	9.8433	5.0427
D1 to Z ↓	0.0112	0.0111	5.3162	3.1835
D1 to Z ↑	0.0193	0.0172	9.8555	5.2657
S0 to Z ↓	0.0170	0.0143	5.3189	3.2674
S0 to Z ↑	0.0183	0.0152	9.8224	5.1423
	X10_P4	**X16_P4**	**X10_P4**	**X16_P4**
D0 to Z ↓	0.0130	0.0121	1.5893	1.0383
D0 to Z ↑	0.0180	0.0171	2.3584	1.5575
D1 to Z ↓	0.0118	0.0116	1.5328	1.0103
D1 to Z ↑	0.0179	0.0174	2.4031	1.5753
S0 to Z ↓	0.0174	0.0150	1.5571	1.0226
S0 to Z ↑	0.0181	0.0156	2.3769	1.5647
	X21_P4		**X21_P4**	
D0 to Z ↓	0.0120		0.7944	
D0 to Z ↑	0.0168		1.1818	
D1 to Z ↓	0.0117		0.7679	
D1 to Z ↑	0.0175		1.1751	
S0 to Z ↓	0.0158		0.7797	
S0 to Z ↑	0.0161		1.1766	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	1.598e-06	1.000e-20
X5_P4	4.516e-06	1.000e-20
X10_P4	8.164e-06	1.000e-20
X16_P4	1.301e-05	1.000e-20
X21_P4	1.592e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	1.907e-05	4.048e-05	1.190e-04	1.887e-04
D1 (output stable)	1.884e-05	4.509e-05	1.035e-04	1.761e-04
S0 (output stable)	1.059e-03	1.631e-03	2.740e-03	4.349e-03
D0 to Z	9.857e-04	1.659e-03	4.108e-03	5.788e-03
D1 to Z	9.858e-04	1.645e-03	3.908e-03	5.699e-03
S0 to Z	1.793e-03	2.714e-03	5.458e-03	7.863e-03
	X21_P4			
D0 (output stable)	2.473e-04			
D1 (output stable)	2.392e-04			
S0 (output stable)	4.825e-03			
D0 to Z	7.479e-03			
D1 to Z	7.547e-03			
S0 to Z	9.572e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

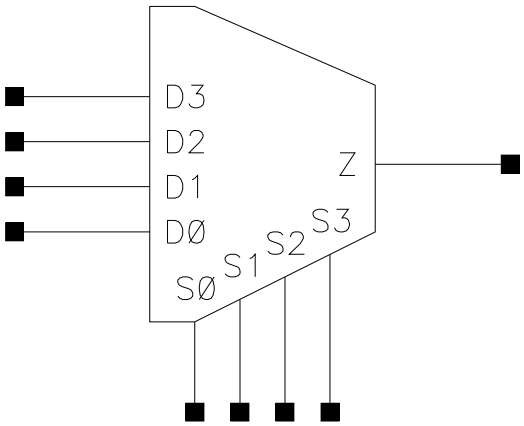
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P4			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	1.768	2.1216
X27_P4	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P4	X27_P4
D0	0.0007	0.0020
D1	0.0007	0.0021
D2	0.0007	0.0020
D3	0.0007	0.0021
S0	0.0007	0.0019
S1	0.0007	0.0019
S2	0.0007	0.0019
S3	0.0007	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	X27_P4	X7_P4	X27_P4
D0 to Z ↓	0.0416	0.0346	2.7644	0.7604
D0 to Z ↑	0.0305	0.0262	2.3644	0.5913
D1 to Z ↓	0.0385	0.0322	2.7629	0.7602
D1 to Z ↑	0.0274	0.0229	2.3555	0.5885
D2 to Z ↓	0.0421	0.0333	2.7699	0.7610
D2 to Z ↑	0.0300	0.0247	2.3736	0.5935
D3 to Z ↓	0.0391	0.0309	2.7657	0.7600
D3 to Z ↑	0.0269	0.0215	2.3630	0.5907
S0 to Z ↓	0.0402	0.0327	2.7636	0.7603
S0 to Z ↑	0.0328	0.0277	2.3647	0.5909
S1 to Z ↓	0.0373	0.0303	2.7613	0.7599
S1 to Z ↑	0.0294	0.0241	2.3537	0.5888
S2 to Z ↓	0.0407	0.0313	2.7685	0.7608
S2 to Z ↑	0.0322	0.0263	2.3731	0.5933
S3 to Z ↓	0.0380	0.0290	2.7654	0.7596
S3 to Z ↑	0.0289	0.0227	2.3639	0.5911

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X7_P4	4.705e-06	1.000e-20
X27_P4	2.155e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X7_P4	X27_P4
D0 (output stable)	5.291e-04	1.670e-03
D1 (output stable)	4.412e-04	1.367e-03
D2 (output stable)	4.978e-04	1.603e-03
D3 (output stable)	4.101e-04	1.301e-03
S0 (output stable)	5.216e-04	1.633e-03
S1 (output stable)	4.310e-04	1.344e-03
S2 (output stable)	4.905e-04	1.568e-03
S3 (output stable)	3.999e-04	1.281e-03
D0 to Z	4.153e-03	1.290e-02
D1 to Z	3.680e-03	1.125e-02
D2 to Z	4.035e-03	1.144e-02
D3 to Z	3.569e-03	9.812e-03
S0 to Z	4.049e-03	1.229e-02
S1 to Z	3.578e-03	1.070e-02
S2 to Z	3.929e-03	1.081e-02
S3 to Z	3.465e-03	9.260e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

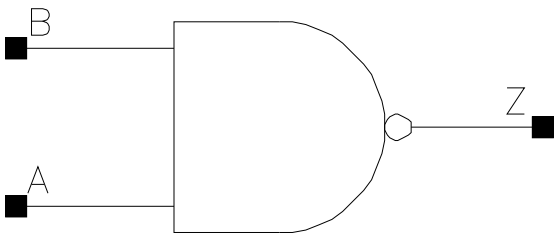
Pin Cycle (vdds)	X7_P4	X27_P4
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P4	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P4	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P4	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P4	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P4	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P4	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P4	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P4	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P4	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P4	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P4	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P4	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P4	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P4	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P4	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P4	C12T28SOI_LL_-NAND2X5_P4	C12T28SOI_LL_-NAND2X7_P4	C12T28SOI_LL_-NAND2X10_P4
A	0.0006	0.0007	0.0008	0.0014
B	0.0006	0.0007	0.0008	0.0013
	C12T28SOI_LL_-NAND2X13_P4	C12T28SOI_LL_-NAND2X17_P4	C12T28SOI_LL_-NAND2X20_P4	C12T28SOI_LL_-NAND2X24_P4
A	0.0017	0.0022	0.0025	0.0030
B	0.0016	0.0021	0.0024	0.0028
	C12T28SOI_LL_-NAND2X27_P4	C12T28SOI_LL_-NAND2X42_P4	C12T28SOI_LL_-NAND2X47_P4	C12T28SOI_LL_-NAND2X50_P4
A	0.0033	0.0010	0.0010	0.0010
B	0.0031	0.0011	0.0011	0.0011
	C12T28SOI_LL_-NAND2X58_P4	C12T28SOI_LL_-NAND2X67_P4	C12T28SOI_-LLBR0D8_-NAND2X7_P4	C12T28SOI_-LLBR0D8_-NAND2X14_P4
A	0.0010	0.0010	0.0008	0.0017
B	0.0011	0.0011	0.0008	0.0016
	C12T28SOI_LLS_-NAND2X40_P4	C12T28SOI_LLS_-NAND2X54_P4		
A	0.0051	0.0068		
B	0.0047	0.0063		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P4	**C12T28SOI_LL_-NAND2X5_P4**	**C12T28SOI_LL_-NAND2X3_P4**	**C12T28SOI_LL_-NAND2X5_P4**
A to Z ↓	0.0086	0.0079	5.2389	3.4071
A to Z ↑	0.0126	0.0113	4.7420	3.0238
B to Z ↓	0.0094	0.0084	5.3140	3.4500
B to Z ↑	0.0113	0.0098	4.7776	3.0452
	C12T28SOI_LL_-NAND2X7_P4	**C12T28SOI_LL_-NAND2X10_P4**	**C12T28SOI_LL_-NAND2X7_P4**	**C12T28SOI_LL_-NAND2X10_P4**
A to Z ↓	0.0078	0.0089	2.8584	1.8963
A to Z ↑	0.0108	0.0117	2.4268	1.6001
B to Z ↓	0.0084	0.0082	2.8912	1.9213
B to Z ↑	0.0093	0.0092	2.4484	1.6142
	C12T28SOI_LL_-NAND2X13_P4	**C12T28SOI_LL_-NAND2X17_P4**	**C12T28SOI_LL_-NAND2X13_P4**	**C12T28SOI_LL_-NAND2X17_P4**
A to Z ↓	0.0086	0.0084	1.4662	1.1646

A to Z ↑	0.0110	0.0111	1.1955	0.9673
B to Z ↓	0.0080	0.0084	1.4850	1.1788
B to Z ↑	0.0086	0.0091	1.2064	0.9755
	C12T28SOI_LL_-NAND2X20_P4	**C12T28SOI_LL_-NAND2X24_P4**	**C12T28SOI_LL_-NAND2X20_P4**	**C12T28SOI_LL_-NAND2X24_P4**
A to Z ↓	0.0084	0.0086	1.0028	0.8510
A to Z ↑	0.0107	0.0110	0.8057	0.6896
B to Z ↓	0.0085	0.0082	1.0154	0.8619
B to Z ↑	0.0088	0.0086	0.8140	0.6958
	C12T28SOI_LL_-NAND2X27_P4	**C12T28SOI_LL_-NAND2X42_P4**	**C12T28SOI_LL_-NAND2X27_P4**	**C12T28SOI_LL_-NAND2X42_P4**
A to Z ↓	0.0084	0.0299	0.7621	0.3436
A to Z ↑	0.0106	0.0306	0.6045	0.4697
B to Z ↓	0.0081	0.0311	0.7716	0.3437
B to Z ↑	0.0083	0.0294	0.6101	0.4700
	C12T28SOI_LL_-NAND2X47_P4	**C12T28SOI_LL_-NAND2X50_P4**	**C12T28SOI_LL_-NAND2X47_P4**	**C12T28SOI_LL_-NAND2X50_P4**
A to Z ↓	0.0308	0.0310	0.3048	0.2864
A to Z ↑	0.0311	0.0313	0.4097	0.3922
B to Z ↓	0.0319	0.0322	0.3048	0.2862
B to Z ↑	0.0299	0.0301	0.4097	0.3926
	C12T28SOI_LL_-NAND2X58_P4	**C12T28SOI_LL_-NAND2X67_P4**	**C12T28SOI_LL_-NAND2X58_P4**	**C12T28SOI_LL_-NAND2X67_P4**
A to Z ↓	0.0325	0.0336	0.2484	0.2181
A to Z ↑	0.0324	0.0333	0.3379	0.2973
B to Z ↓	0.0336	0.0347	0.2483	0.2182
B to Z ↑	0.0313	0.0321	0.3381	0.2972
	C12T28SOI_-LLBR0D8_-NAND2X7_P4	**C12T28SOI_-LLBR0D8_-NAND2X14_P4**	**C12T28SOI_-LLBR0D8_-NAND2X7_P4**	**C12T28SOI_-LLBR0D8_-NAND2X14_P4**
A to Z ↓	0.0061	0.0070	2.1688	1.1467
A to Z ↑	0.0135	0.0137	3.2142	1.5731
B to Z ↓	0.0060	0.0056	2.2069	1.1698
B to Z ↑	0.0113	0.0102	3.3283	1.6081
	C12T28SOI_LLS_-NAND2X40_P4	**C12T28SOI_LLS_-NAND2X54_P4**	**C12T28SOI_LLS_-NAND2X40_P4**	**C12T28SOI_LLS_-NAND2X54_P4**
A to Z ↓	0.0084	0.0085	0.5168	0.3914
A to Z ↑	0.0105	0.0106	0.4054	0.3059
B to Z ↓	0.0081	0.0083	0.5235	0.3964
B to Z ↑	0.0082	0.0083	0.4095	0.3090

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P4	7.784e-07	1.000e-20
C12T28SOI_LL_NAND2X5_P4	1.575e-06	1.000e-20
C12T28SOI_LL_NAND2X7_P4	2.081e-06	1.000e-20
C12T28SOI_LL_NAND2X10_P4	2.731e-06	1.000e-20
C12T28SOI_LL_NAND2X13_P4	4.115e-06	1.000e-20
C12T28SOI_LL_NAND2X17_P4	4.750e-06	1.000e-20
C12T28SOI_LL_NAND2X20_P4	5.992e-06	1.000e-20
C12T28SOI_LL_NAND2X24_P4	6.783e-06	1.000e-20
C12T28SOI_LL_NAND2X27_P4	7.873e-06	1.000e-20

C12T28SOI_LL_NAND2X42_P4	1.397e-05	1.000e-20
C12T28SOI_LL_NAND2X47_P4	1.518e-05	1.000e-20
C12T28SOI_LL_NAND2X50_P4	1.525e-05	1.000e-20
C12T28SOI_LL_NAND2X58_P4	1.653e-05	1.000e-20
C12T28SOI_LL_NAND2X67_P4	1.781e-05	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_P4	1.716e-06	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_-P4	3.315e-06	1.000e-20
C12T28SOI_LLS_NAND2X40_P4	1.164e-05	1.000e-20
C12T28SOI_LLS_NAND2X54_P4	1.540e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND2X3_P4	C12T28SOI_LL_-NAND2X5_P4	C12T28SOI_LL_-NAND2X7_P4	C12T28SOI_LL_-NAND2X10_P4
A (output stable)	1.488e-05	2.314e-05	2.753e-05	8.175e-05
B (output stable)	3.835e-05	5.933e-05	7.179e-05	3.495e-04
A to Z	7.454e-04	1.029e-03	1.237e-03	2.092e-03
B to Z	6.371e-04	8.673e-04	1.038e-03	1.558e-03
	C12T28SOI_LL_-NAND2X13_P4	C12T28SOI_LL_-NAND2X17_P4	C12T28SOI_LL_-NAND2X20_P4	C12T28SOI_LL_-NAND2X24_P4
A (output stable)	9.842e-05	1.193e-04	1.339e-04	1.791e-04
B (output stable)	4.070e-04	4.040e-04	4.482e-04	6.680e-04
A to Z	2.617e-03	3.252e-03	3.752e-03	4.537e-03
B to Z	1.975e-03	2.557e-03	2.973e-03	3.440e-03
	C12T28SOI_LL_-NAND2X27_P4	C12T28SOI_LL_-NAND2X42_P4	C12T28SOI_LL_-NAND2X47_P4	C12T28SOI_LL_-NAND2X50_P4
A (output stable)	1.937e-04	3.051e-05	3.058e-05	3.064e-05
B (output stable)	7.195e-04	7.991e-05	7.940e-05	8.010e-05
A to Z	4.950e-03	1.161e-02	1.260e-02	1.296e-02
B to Z	3.747e-03	1.142e-02	1.241e-02	1.276e-02
	C12T28SOI_LL_-NAND2X58_P4	C12T28SOI_LL_-NAND2X67_P4	C12T28SOI_-LLBR0D8_-NAND2X7_P4	C12T28SOI_-LLBR0D8_-NAND2X14_P4
A (output stable)	3.071e-05	3.091e-05	3.616e-05	1.238e-04
B (output stable)	8.017e-05	8.048e-05	9.525e-05	5.100e-04
A to Z	1.482e-02	1.628e-02	1.259e-03	2.669e-03
B to Z	1.462e-02	1.608e-02	9.742e-04	1.792e-03
	C12T28SOI_LLS_-NAND2X40_P4	C12T28SOI_LLS_-NAND2X54_P4		
A (output stable)	2.868e-04	3.725e-04		
B (output stable)	1.025e-03	1.297e-03		
A to Z	7.331e-03	9.755e-03		
B to Z	5.566e-03	7.442e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND2X3_P4	C12T28SOI_LL_-NAND2X5_P4	C12T28SOI_LL_-NAND2X7_P4	C12T28SOI_LL_-NAND2X10_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

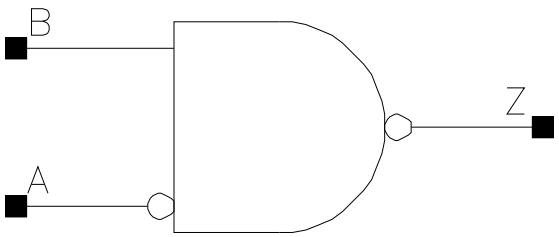
	C12T28SOI_LL_-NAND2X13_P4	C12T28SOI_LL_-NAND2X17_P4	C12T28SOI_LL_-NAND2X20_P4	C12T28SOI_LL_-NAND2X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P4	C12T28SOI_LL_-NAND2X42_P4	C12T28SOI_LL_-NAND2X47_P4	C12T28SOI_LL_-NAND2X50_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P4	C12T28SOI_LL_-NAND2X67_P4	C12T28SOI_-LLBR0D8_-NAND2X7_P4	C12T28SOI_-LLBR0D8_-NAND2X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P4	C12T28SOI_LLS_-NAND2X54_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X7_P4	1.200	0.544	0.6528
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X40_P4	1.200	2.312	2.7744
X54_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P4	X7_P4	X13_P4	X27_P4
A	0.0008	0.0008	0.0011	0.0020
B	0.0006	0.0008	0.0015	0.0032
	X40_P4	X54_P4		
A	0.0031	0.0040		
B	0.0046	0.0062		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0224	0.0238	5.1711	2.8264
A to Z ↑	0.0176	0.0185	4.5422	2.3667
B to Z ↓	0.0097	0.0084	5.3591	2.9108
B to Z ↑	0.0114	0.0093	4.7791	2.4732
	X13_P4	**X27_P4**	**X13_P4**	**X27_P4**

A to Z ↓	0.0219	0.0215	1.5310	0.7600
A to Z ↑	0.0177	0.0174	1.2243	0.5912
B to Z ↓	0.0080	0.0080	1.5781	0.7840
B to Z ↑	0.0085	0.0082	1.2363	0.6107
	X40_P4	**X54_P4**	**X40_P4**	**X54_P4**
A to Z ↓	0.0216	0.0215	0.5069	0.3845
A to Z ↑	0.0177	0.0175	0.3934	0.2974
B to Z ↓	0.0080	0.0081	0.5228	0.3967
B to Z ↑	0.0082	0.0082	0.4109	0.3105

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	1.485e-06	1.000e-20
X7_P4	2.755e-06	1.000e-20
X13_P4	6.256e-06	1.000e-20
X27_P4	1.199e-05	1.000e-20
X40_P4	1.760e-05	1.000e-20
X54_P4	2.321e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	1.110e-03	1.383e-03	2.294e-03	4.530e-03
B (output stable)	3.937e-05	7.307e-05	3.753e-04	6.651e-04
A to Z	1.867e-03	2.583e-03	4.756e-03	9.386e-03
B to Z	6.433e-04	1.029e-03	1.934e-03	3.798e-03
	X40_P4	X54_P4		
A (output stable)	6.851e-03	8.924e-03		
B (output stable)	9.873e-04	1.273e-03		
A to Z	1.401e-02	1.833e-02		
B to Z	5.554e-03	7.342e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

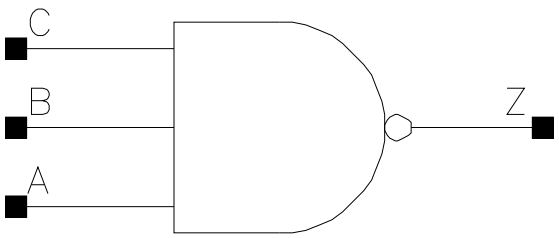
Pin Cycle (vdds)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P4	X54_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P4	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P4	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P4	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P4	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P4	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P4	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P4	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P4	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P4	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P4	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P4	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P4	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P4	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P4	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P4	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A	0.0007	0.0009	0.0014	0.0017
B	0.0007	0.0009	0.0013	0.0016
C	0.0007	0.0008	0.0013	0.0016
	C12T28SOI_LL_-NAND3X15_P4	C12T28SOI_LL_-NAND3X18_P4	C12T28SOI_LL_-NAND3X21_P4	C12T28SOI_LL_-NAND3X24_P4
A	0.0022	0.0025	0.0030	0.0034
B	0.0021	0.0024	0.0029	0.0032
C	0.0020	0.0023	0.0028	0.0031
	C12T28SOI_LL_-NAND3X35_P4	C12T28SOI_LL_-NAND3X47_P4	C12T28SOI_-LLBR0P6_-NAND3X6_P4	C12T28SOI_-LLBR0P6_-NAND3X12_P4
A	0.0051	0.0067	0.0009	0.0017
B	0.0048	0.0064	0.0009	0.0016
C	0.0046	0.0062	0.0008	0.0015
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	C12T28SOI_-LLBR0P6_-NAND3X24_P4	C12T28SOI_-LLBR0P6_-NAND3X35_P4	C12T28SOI_-LLBR0P6_-NAND3X47_P4
A	0.0025	0.0033	0.0050	0.0066
B	0.0024	0.0032	0.0046	0.0062
C	0.0022	0.0030	0.0045	0.0059
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4			
A	0.0026			
B	0.0025			
C	0.0023			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4
A to Z ↓	0.0138	0.0127	5.4781	3.9462
A to Z ↑	0.0159	0.0142	3.4409	2.3613
B to Z ↓	0.0150	0.0134	5.5042	3.9651
B to Z ↑	0.0151	0.0133	3.4501	2.3681
C to Z ↓	0.0136	0.0124	5.5311	3.9838
C to Z ↑	0.0129	0.0114	3.4526	2.3846

	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A to Z ↓	0.0139	0.0131	2.6764	2.0930
A to Z ↑	0.0150	0.0139	1.6126	1.2111
B to Z ↓	0.0135	0.0128	2.6908	2.1041
B to Z ↑	0.0135	0.0126	1.6172	1.2143
C to Z ↓	0.0123	0.0118	2.7045	2.1152
C to Z ↑	0.0114	0.0104	1.6121	1.2048
	C12T28SOI_LL_-NAND3X15_P4	**C12T28SOI_LL_-NAND3X18_P4**	**C12T28SOI_LL_-NAND3X15_P4**	**C12T28SOI_LL_-NAND3X18_P4**
A to Z ↓	0.0125	0.0122	1.6830	1.4456
A to Z ↑	0.0136	0.0131	0.9688	0.8045
B to Z ↓	0.0127	0.0125	1.6925	1.4531
B to Z ↑	0.0123	0.0118	0.9722	0.8076
C to Z ↓	0.0119	0.0117	1.7014	1.4603
C to Z ↑	0.0103	0.0098	0.9800	0.8139
	C12T28SOI_LL_-NAND3X21_P4	**C12T28SOI_LL_-NAND3X24_P4**	**C12T28SOI_LL_-NAND3X21_P4**	**C12T28SOI_LL_-NAND3X24_P4**
A to Z ↓	0.0129	0.0127	1.2208	1.0957
A to Z ↑	0.0137	0.0134	0.6951	0.6099
B to Z ↓	0.0128	0.0127	1.2272	1.1011
B to Z ↑	0.0124	0.0120	0.6969	0.6114
C to Z ↓	0.0119	0.0118	1.2336	1.1070
C to Z ↑	0.0103	0.0100	0.6984	0.6120
	C12T28SOI_LL_-NAND3X35_P4	**C12T28SOI_LL_-NAND3X47_P4**	**C12T28SOI_LL_-NAND3X35_P4**	**C12T28SOI_LL_-NAND3X47_P4**
A to Z ↓	0.0123	0.0125	0.7479	0.5699
A to Z ↑	0.0131	0.0132	0.4094	0.3099
B to Z ↓	0.0125	0.0126	0.7521	0.5731
B to Z ↑	0.0117	0.0118	0.4096	0.3089
C to Z ↓	0.0117	0.0118	0.7562	0.5761
C to Z ↑	0.0097	0.0096	0.4120	0.3105
	C12T28SOI_-LLBR0P6_-NAND3X6_P4	**C12T28SOI_-LLBR0P6_-NAND3X12_P4**	**C12T28SOI_-LLBR0P6_-NAND3X6_P4**	**C12T28SOI_-LLBR0P6_-NAND3X12_P4**
A to Z ↓	0.0098	0.0104	2.6829	1.4263
A to Z ↑	0.0202	0.0200	3.6923	1.8902
B to Z ↓	0.0099	0.0093	2.7102	1.4417
B to Z ↑	0.0183	0.0172	3.7055	1.8961
C to Z ↓	0.0080	0.0072	2.7442	1.4607
C to Z ↑	0.0144	0.0131	3.7279	1.9018
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	**C12T28SOI_-LLBR0P6_-NAND3X24_P4**	**C12T28SOI_-LLBR0P6_-NAND3X18_P4**	**C12T28SOI_-LLBR0P6_-NAND3X24_P4**
A to Z ↓	0.0095	0.0100	0.9879	0.7494
A to Z ↑	0.0189	0.0193	1.2572	0.9507
B to Z ↓	0.0090	0.0091	0.9990	0.7578
B to Z ↑	0.0162	0.0166	1.2626	0.9535
C to Z ↓	0.0073	0.0072	1.0103	0.7671
C to Z ↑	0.0125	0.0125	1.2722	0.9554
	C12T28SOI_-LLBR0P6_-NAND3X35_P4	**C12T28SOI_-LLBR0P6_-NAND3X47_P4**	**C12T28SOI_-LLBR0P6_-NAND3X35_P4**	**C12T28SOI_-LLBR0P6_-NAND3X47_P4**

A to Z ↓	0.0096	0.0099	0.5136	0.3932
A to Z ↑	0.0192	0.0194	0.6561	0.4973
B to Z ↓	0.0090	0.0092	0.5199	0.3978
B to Z ↑	0.0164	0.0165	0.6571	0.4974
C to Z ↓	0.0072	0.0076	0.5265	0.4025
C to Z ↑	0.0123	0.0126	0.6644	0.4992
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P4**	
A to Z ↓	0.0105		0.9693	
A to Z ↑	0.0191		1.1850	
B to Z ↓	0.0093		0.9792	
B to Z ↑	0.0164		1.1880	
C to Z ↓	0.0072		0.9915	
C to Z ↑	0.0122		1.1787	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P4	1.019e-06	1.000e-20
C12T28SOI_LL_NAND3X6_P4	1.762e-06	1.000e-20
C12T28SOI_LL_NAND3X9_P4	2.179e-06	1.000e-20
C12T28SOI_LL_NAND3X12_P4	3.254e-06	1.000e-20
C12T28SOI_LL_NAND3X15_P4	3.680e-06	1.000e-20
C12T28SOI_LL_NAND3X18_P4	4.622e-06	1.000e-20
C12T28SOI_LL_NAND3X21_P4	5.340e-06	1.000e-20
C12T28SOI_LL_NAND3X24_P4	6.186e-06	1.000e-20
C12T28SOI_LL_NAND3X35_P4	9.118e-06	1.000e-20
C12T28SOI_LL_NAND3X47_P4	1.205e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_P4	1.376e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P4	2.446e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P4	3.320e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P4	4.496e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P4	6.545e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P4	8.592e-06	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P4	4.575e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A (output stable)	1.974e-05	2.792e-05	6.493e-05	7.795e-05
B (output stable)	7.600e-05	9.801e-05	2.130e-04	2.543e-04
C (output stable)	2.444e-04	3.054e-04	4.553e-04	5.463e-04
A to Z	1.590e-03	1.985e-03	3.165e-03	3.801e-03
B to Z	1.434e-03	1.764e-03	2.613e-03	3.150e-03
C to Z	1.157e-03	1.439e-03	2.076e-03	2.527e-03

	C12T28SOI_LL_-NAND3X15_P4	C12T28SOI_LL_-NAND3X18_P4	C12T28SOI_LL_-NAND3X21_P4	C12T28SOI_LL_-NAND3X24_P4
A (output stable)	8.690e-05	9.541e-05	1.340e-04	1.447e-04
B (output stable)	2.971e-04	3.417e-04	4.417e-04	4.867e-04
C (output stable)	6.112e-04	6.909e-04	8.897e-04	9.612e-04
A to Z	4.547e-03	5.181e-03	6.480e-03	7.131e-03
B to Z	3.766e-03	4.289e-03	5.364e-03	5.895e-03
C to Z	3.072e-03	3.486e-03	4.309e-03	4.736e-03
	C12T28SOI_LL_-NAND3X35_P4	C12T28SOI_LL_-NAND3X47_P4	C12T28SOI_-LLBR0P6_-NAND3X6_P4	C12T28SOI_-LLBR0P6_-NAND3X12_P4
A (output stable)	1.959e-04	2.567e-04	3.971e-05	1.085e-04
B (output stable)	6.902e-04	9.006e-04	1.437e-04	3.781e-04
C (output stable)	1.427e-03	1.816e-03	4.268e-04	8.106e-04
A to Z	1.031e-02	1.362e-02	2.116e-03	4.138e-03
B to Z	8.506e-03	1.122e-02	1.764e-03	3.143e-03
C to Z	6.750e-03	8.984e-03	1.257e-03	2.122e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	C12T28SOI_-LLBR0P6_-NAND3X24_P4	C12T28SOI_-LLBR0P6_-NAND3X35_P4	C12T28SOI_-LLBR0P6_-NAND3X47_P4
A (output stable)	1.378e-04	2.032e-04	2.747e-04	3.598e-04
B (output stable)	4.912e-04	7.041e-04	9.746e-04	1.293e-03
C (output stable)	9.814e-04	1.435e-03	2.104e-03	2.722e-03
A to Z	5.566e-03	7.697e-03	1.112e-02	1.469e-02
B to Z	4.222e-03	5.848e-03	8.426e-03	1.114e-02
C to Z	2.976e-03	3.977e-03	5.641e-03	7.533e-03
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4			
A (output stable)	1.605e-04			
B (output stable)	5.720e-04			
C (output stable)	1.206e-03			
A to Z	6.146e-03			
B to Z	4.689e-03			
C to Z	3.178e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P4	C12T28SOI_LL_-NAND3X18_P4	C12T28SOI_LL_-NAND3X21_P4	C12T28SOI_LL_-NAND3X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

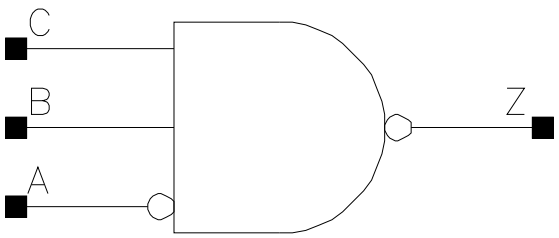
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P4	C12T28SOI_LL_-NAND3X47_P4	C12T28SOI_-LLBR0P6_-NAND3X6_P4	C12T28SOI_-LLBR0P6_-NAND3X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	C12T28SOI_-LLBR0P6_-NAND3X24_P4	C12T28SOI_-LLBR0P6_-NAND3X35_P4	C12T28SOI_-LLBR0P6_-NAND3X47_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.816	0.9792
X12_P4	1.200	1.224	1.4688
X18_P4	1.200	1.496	1.7952
X24_P4	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0008	0.0011	0.0011	0.0020
B	0.0008	0.0016	0.0024	0.0032
C	0.0008	0.0016	0.0023	0.0031

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X12_P4**	**X6_P4**	**X12_P4**
A to Z ↓	0.0269	0.0255	3.9216	2.1057
A to Z ↑	0.0197	0.0191	2.2986	1.1555
B to Z ↓	0.0118	0.0121	3.9740	2.1328
B to Z ↑	0.0119	0.0118	2.3787	1.1995
C to Z ↓	0.0119	0.0109	3.9940	2.1439
C to Z ↑	0.0105	0.0094	2.3940	1.2101
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0293	0.0252	1.4419	1.0950

A to Z ↑	0.0223	0.0184	0.7780	0.5837
B to Z ↓	0.0125	0.0122	1.4577	1.1084
B to Z ↑	0.0117	0.0116	0.8086	0.6085
C to Z ↓	0.0118	0.0112	1.4645	1.1141
C to Z ↑	0.0100	0.0094	0.8151	0.6137

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P4	2.402e-06	1.000e-20
X12_P4	5.370e-06	1.000e-20
X18_P4	6.713e-06	1.000e-20
X24_P4	1.038e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	1.343e-03	2.392e-03	3.190e-03	4.562e-03
B (output stable)	8.372e-05	2.005e-04	3.007e-04	4.272e-04
C (output stable)	1.609e-04	5.573e-04	7.017e-04	1.055e-03
A to Z	3.088e-03	6.016e-03	8.671e-03	1.177e-02
B to Z	1.480e-03	2.882e-03	4.290e-03	5.570e-03
C to Z	1.278e-03	2.223e-03	3.489e-03	4.323e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

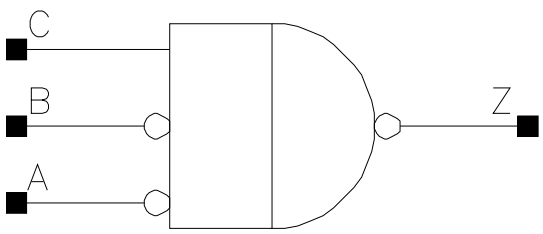
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	0.816	0.9792
X13_P4	1.200	1.088	1.3056
X20_P4	1.200	1.632	1.9584
X27_P4	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P4	X13_P4	X20_P4	X27_P4
A	0.0010	0.0010	0.0020	0.0018
B	0.0011	0.0011	0.0020	0.0019
C	0.0008	0.0016	0.0023	0.0031

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	**X13_P4**	**X7_P4**	**X13_P4**
A to Z ↓	0.0245	0.0297	2.7188	1.4507
A to Z ↑	0.0172	0.0198	2.2751	1.1469
B to Z ↓	0.0252	0.0306	2.7199	1.4503
B to Z ↑	0.0161	0.0188	2.2740	1.1459
C to Z ↓	0.0083	0.0078	2.7944	1.4862
C to Z ↑	0.0092	0.0084	2.3775	1.2057
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0273	0.0297	0.9896	0.7541
A to Z ↑	0.0185	0.0221	0.7750	0.5816
B to Z ↓	0.0264	0.0292	0.9893	0.7543

B to Z ↑	0.0168	0.0207	0.7739	0.5806
C to Z ↓	0.0087	0.0084	1.0157	0.7730
C to Z ↑	0.0090	0.0087	0.8136	0.6107

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X7_P4	3.650e-06	1.000e-20
X13_P4	4.833e-06	1.000e-20
X20_P4	7.912e-06	1.000e-20
X27_P4	8.841e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	7.751e-04	1.022e-03	1.758e-03	2.024e-03
B (output stable)	6.902e-04	9.332e-04	1.487e-03	1.764e-03
C (output stable)	7.719e-05	4.254e-04	4.472e-04	5.719e-04
A to Z	3.450e-03	5.645e-03	8.889e-03	1.100e-02
B to Z	3.176e-03	5.373e-03	7.938e-03	1.013e-02
C to Z	1.076e-03	1.943e-03	3.088e-03	4.063e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

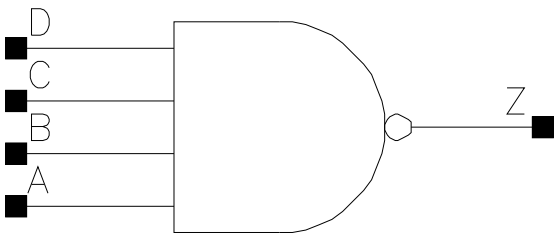
Pin Cycle (vdds)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0007	0.0006	0.0008	0.0010
B	0.0007	0.0007	0.0009	0.0011
C	0.0006	0.0007	0.0009	0.0011
D	0.0007	0.0007	0.0009	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0385	0.0379	1.6593	0.8300
A to Z ↑	0.0319	0.0344	2.3361	1.1547
B to Z ↓	0.0398	0.0398	1.6577	0.8297
B to Z ↑	0.0306	0.0338	2.3366	1.1568
C to Z ↓	0.0390	0.0378	1.6574	0.8290
C to Z ↑	0.0328	0.0357	2.3362	1.1547

D to Z ↓	0.0406	0.0393	1.6586	0.8299
D to Z ↑	0.0319	0.0343	2.3346	1.1548
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0403	0.0374	0.5733	0.4287
A to Z ↑	0.0332	0.0325	0.7810	0.5852
B to Z ↓	0.0418	0.0386	0.5735	0.4289
B to Z ↑	0.0322	0.0314	0.7812	0.5857
C to Z ↓	0.0376	0.0347	0.5737	0.4284
C to Z ↑	0.0335	0.0325	0.7788	0.5842
D to Z ↓	0.0391	0.0361	0.5733	0.4287
D to Z ↑	0.0322	0.0313	0.7792	0.5845

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	3.225e-06	1.000e-20
X17_P4	5.306e-06	1.000e-20
X25_P4	7.678e-06	1.000e-20
X33_P4	1.128e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	5.514e-04	6.809e-04	9.905e-04	1.197e-03
B (output stable)	5.198e-04	6.535e-04	9.451e-04	1.136e-03
C (output stable)	5.573e-04	6.686e-04	1.017e-03	1.181e-03
D (output stable)	5.232e-04	6.325e-04	9.632e-04	1.119e-03
A to Z	4.067e-03	6.134e-03	9.532e-03	1.173e-02
B to Z	3.953e-03	6.030e-03	9.370e-03	1.151e-02
C to Z	4.164e-03	6.049e-03	8.956e-03	1.089e-02
D to Z	4.060e-03	5.931e-03	8.787e-03	1.069e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

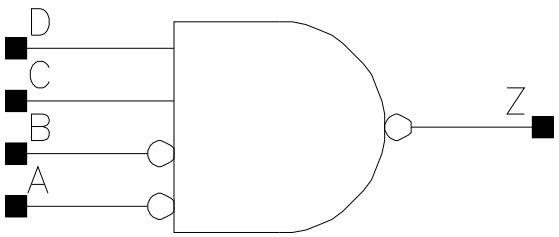
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X12_P4	1.200	1.496	1.7952
X18_P4	1.200	2.040	2.4480
X24_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0010	0.0011	0.0020	0.0018
B	0.0010	0.0015	0.0021	0.0019
C	0.0008	0.0016	0.0024	0.0032
D	0.0008	0.0016	0.0023	0.0031

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X12_P4	X6_P4	X12_P4
A to Z ↓	0.0262	0.0348	4.0420	2.1104
A to Z ↑	0.0181	0.0222	2.2770	1.1494
B to Z ↓	0.0265	0.0350	4.0441	2.1108
B to Z ↑	0.0164	0.0208	2.2770	1.1473
C to Z ↓	0.0119	0.0121	4.0932	2.1321
C to Z ↑	0.0121	0.0117	2.5360	1.1990

D to Z ↓	0.0117	0.0109	4.1130	2.1428
D to Z ↑	0.0106	0.0094	2.5527	1.2096
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0305	0.0339	1.4390	1.0953
A to Z ↑	0.0197	0.0250	0.7755	0.5826
B to Z ↓	0.0297	0.0333	1.4393	1.0956
B to Z ↑	0.0180	0.0235	0.7745	0.5819
C to Z ↓	0.0122	0.0126	1.4541	1.1057
C to Z ↑	0.0116	0.0118	0.8121	0.6062
D to Z ↓	0.0115	0.0116	1.4612	1.1114
D to Z ↑	0.0098	0.0097	0.8306	0.6123

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P4	3.165e-06	1.000e-20
X12_P4	4.201e-06	1.000e-20
X18_P4	6.977e-06	1.000e-20
X24_P4	7.548e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	8.821e-04	1.433e-03	2.204e-03	2.612e-03
B (output stable)	7.768e-04	1.255e-03	1.850e-03	2.261e-03
C (output stable)	1.015e-04	2.580e-04	3.779e-04	5.105e-04
D (output stable)	1.845e-04	6.131e-04	7.484e-04	1.093e-03
A to Z	3.658e-03	6.847e-03	1.022e-02	1.335e-02
B to Z	3.421e-03	6.420e-03	9.319e-03	1.246e-02
C to Z	1.437e-03	2.872e-03	4.197e-03	5.820e-03
D to Z	1.232e-03	2.214e-03	3.440e-03	4.608e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

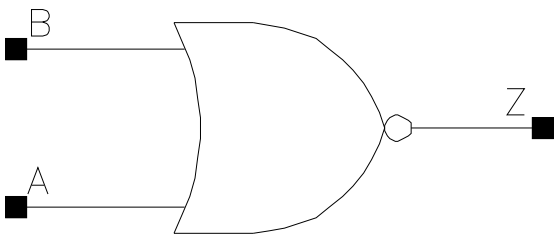
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.408	0.4896
X5_P4	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X10_P4	1.200	0.680	0.8160
X14_P4	1.200	0.680	0.8160
X17_P4	1.200	0.952	1.1424
X21_P4	1.200	0.952	1.1424
X24_P4	1.200	1.224	1.4688
X27_P4	1.200	1.224	1.4688
X34_P4	1.200	1.496	1.7952
X40_P4	1.200	1.360	1.6320
X41_P4	1.200	1.768	2.1216
X49_P4	1.200	1.496	1.7952
X53_P4	1.200	1.904	2.2848
X55_P4	1.200	2.312	2.7744
X57_P4	1.200	1.904	2.2848
X65_P4	1.200	2.040	2.4480
X84_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P4	X5_P4	X7_P4	X10_P4
A	0.0006	0.0007	0.0008	0.0014
B	0.0006	0.0007	0.0009	0.0013
	X14_P4	X17_P4	X21_P4	X24_P4

A	0.0017	0.0022	0.0026	0.0030
B	0.0016	0.0020	0.0024	0.0028
	X27_P4	X34_P4	X40_P4	X41_P4
A	0.0033	0.0042	0.0010	0.0051
B	0.0031	0.0038	0.0011	0.0048
	X49_P4	X53_P4	X55_P4	X57_P4
A	0.0010	0.0011	0.0067	0.0011
B	0.0011	0.0010	0.0063	0.0010
	X65_P4	X84_P4		
A	0.0010	0.0011		
B	0.0010	0.0010		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X5_P4**	**X3_P4**	**X5_P4**
A to Z ↓	0.0079	0.0075	3.2489	2.3552
A to Z ↑	0.0141	0.0129	8.9014	6.4833
B to Z ↓	0.0068	0.0062	3.3294	2.3748
B to Z ↑	0.0144	0.0130	8.9546	6.5098
	X7_P4	**X10_P4**	**X7_P4**	**X10_P4**
A to Z ↓	0.0074	0.0077	1.7346	1.1240
A to Z ↑	0.0119	0.0136	4.5605	3.0662
B to Z ↓	0.0059	0.0053	1.7579	1.1375
B to Z ↑	0.0119	0.0112	4.5824	3.0852
	X14_P4	**X17_P4**	**X14_P4**	**X17_P4**
A to Z ↓	0.0076	0.0076	0.8574	0.6890
A to Z ↑	0.0126	0.0127	2.2670	1.8369
B to Z ↓	0.0052	0.0059	0.8682	0.6962
B to Z ↑	0.0105	0.0115	2.2820	1.8481
	X21_P4	**X24_P4**	**X21_P4**	**X24_P4**
A to Z ↓	0.0076	0.0075	0.5860	0.4989
A to Z ↑	0.0121	0.0124	1.5268	1.3390
B to Z ↓	0.0058	0.0054	0.5922	0.5049
B to Z ↑	0.0110	0.0108	1.5359	1.3480
	X27_P4	**X34_P4**	**X27_P4**	**X34_P4**
A to Z ↓	0.0075	0.0078	0.4439	0.3584
A to Z ↑	0.0120	0.0121	1.1780	0.9371
B to Z ↓	0.0054	0.0058	0.4497	0.3625
B to Z ↑	0.0105	0.0110	1.1856	0.9427
	X40_P4	**X41_P4**	**X40_P4**	**X41_P4**
A to Z ↓	0.0271	0.0076	0.3504	0.2986
A to Z ↑	0.0360	0.0119	0.4803	0.7753
B to Z ↓	0.0258	0.0054	0.3502	0.3025
B to Z ↑	0.0370	0.0104	0.4808	0.7804
	X49_P4	**X53_P4**	**X49_P4**	**X53_P4**
A to Z ↓	0.0281	0.0293	0.2915	0.2670
A to Z ↑	0.0369	0.0418	0.3996	0.3698
B to Z ↓	0.0268	0.0282	0.2915	0.2671
B to Z ↑	0.0379	0.0426	0.3997	0.3700
	X55_P4	**X57_P4**	**X55_P4**	**X57_P4**
A to Z ↓	0.0077	0.0296	0.2258	0.2511
A to Z ↑	0.0119	0.0420	0.5848	0.3441

B to Z ↓	0.0056	0.0284	0.2291	0.2512
B to Z ↑	0.0104	0.0428	0.5888	0.3439
	X65_P4	**X84_P4**	**X65_P4**	**X84_P4**
A to Z ↓	0.0304	0.0316	0.2200	0.1748
A to Z ↑	0.0428	0.0433	0.3009	0.2389
B to Z ↓	0.0293	0.0304	0.2199	0.1747
B to Z ↑	0.0437	0.0442	0.3006	0.2391

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	7.844e-07	1.000e-20
X5_P4	1.291e-06	1.000e-20
X7_P4	2.111e-06	1.000e-20
X10_P4	2.774e-06	1.000e-20
X14_P4	4.188e-06	1.000e-20
X17_P4	4.828e-06	1.000e-20
X21_P4	6.106e-06	1.000e-20
X24_P4	6.900e-06	1.000e-20
X27_P4	8.026e-06	1.000e-20
X34_P4	9.948e-06	1.000e-20
X40_P4	1.730e-05	1.000e-20
X41_P4	1.187e-05	1.000e-20
X49_P4	1.980e-05	1.000e-20
X53_P4	2.232e-05	1.000e-20
X55_P4	1.571e-05	1.000e-20
X57_P4	2.407e-05	1.000e-20
X65_P4	2.657e-05	1.000e-20
X84_P4	3.085e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	2.506e-05	3.312e-05	4.472e-05	1.357e-04
B (output stable)	2.074e-05	3.199e-05	5.117e-05	1.431e-04
A to Z	7.462e-04	9.283e-04	1.247e-03	2.107e-03
B to Z	6.070e-04	7.492e-04	9.894e-04	1.391e-03
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	1.592e-04	1.898e-04	2.088e-04	2.638e-04
B (output stable)	1.897e-04	2.084e-04	2.300e-04	2.841e-04
A to Z	2.650e-03	3.308e-03	3.822e-03	4.499e-03
B to Z	1.792e-03	2.397e-03	2.788e-03	3.156e-03
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	2.801e-04	3.362e-04	4.494e-05	4.392e-04
B (output stable)	3.191e-04	3.539e-04	5.120e-05	4.870e-04
A to Z	4.965e-03	6.257e-03	1.138e-02	7.459e-03
B to Z	3.471e-03	4.579e-03	1.113e-02	5.160e-03
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	4.513e-05	4.677e-05	5.719e-04	4.685e-05
B (output stable)	5.104e-05	5.410e-05	6.463e-04	5.410e-05
A to Z	1.278e-02	1.576e-02	9.865e-03	1.634e-02
B to Z	1.253e-02	1.548e-02	6.884e-03	1.606e-02
	X65_P4	X84_P4		

A (output stable)	4.686e-05	4.874e-05		
B (output stable)	5.427e-05	5.502e-05		
A to Z	1.778e-02	2.117e-02		
B to Z	1.751e-02	2.083e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

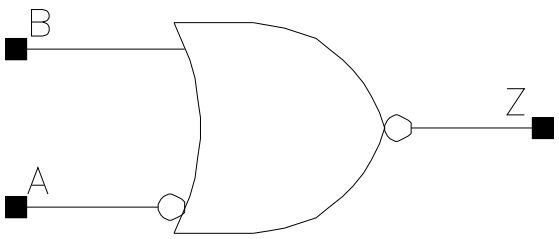
Pin Cycle (vdds)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P4	X84_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X7_P4	1.200	0.680	0.8160
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X41_P4	1.200	2.312	2.7744
X55_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X7_P4	X13_P4
A	0.0008	0.0008	0.0008	0.0011
B	0.0006	0.0009	0.0008	0.0015
	X27_P4	X41_P4	X55_P4	
A	0.0020	0.0030	0.0040	
B	0.0031	0.0048	0.0063	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0210	0.0232	3.0601	2.0149
A to Z ↑	0.0198	0.0200	8.7729	4.5109
B to Z ↓	0.0070	0.0071	3.2995	2.1768
B to Z ↑	0.0145	0.0117	8.9346	4.6004

	X7_P4	X13_P4	X7_P4	X13_P4
A to Z ↓	0.0236	0.0211	1.6061	0.8752
A to Z ↑	0.0217	0.0210	4.4809	2.3957
B to Z ↓	0.0064	0.0056	1.6832	0.9145
B to Z ↑	0.0130	0.0116	4.5492	2.4369
	X27_P4	**X41_P4**	**X27_P4**	**X41_P4**
A to Z ↓	0.0203	0.0208	0.4177	0.2834
A to Z ↑	0.0200	0.0203	1.1424	0.7675
B to Z ↓	0.0055	0.0056	0.4524	0.3047
B to Z ↑	0.0109	0.0108	1.1633	0.7815
	X55_P4		**X55_P4**	
A to Z ↓	0.0204		0.2145	
A to Z ↑	0.0200		0.5800	
B to Z ↓	0.0056		0.2310	
B to Z ↑	0.0107		0.5904	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	1.492e-06	1.000e-20
X6_P4	2.746e-06	1.000e-20
X7_P4	3.095e-06	1.000e-20
X13_P4	6.213e-06	1.000e-20
X27_P4	1.214e-05	1.000e-20
X41_P4	1.783e-05	1.000e-20
X55_P4	2.352e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	1.099e-03	1.349e-03	1.443e-03	2.385e-03
B (output stable)	3.443e-05	6.749e-05	1.401e-04	2.648e-04
A to Z	1.859e-03	2.542e-03	2.954e-03	4.998e-03
B to Z	6.161e-04	9.548e-04	1.159e-03	1.907e-03
	X27_P4	X41_P4	X55_P4	
A (output stable)	4.663e-03	7.096e-03	9.182e-03	
B (output stable)	5.374e-04	7.720e-04	9.990e-04	
A to Z	9.889e-03	1.474e-02	1.923e-02	
B to Z	3.714e-03	5.435e-03	7.152e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

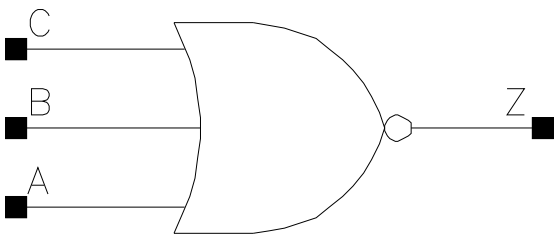
Pin Cycle (vdds)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P4	X41_P4	X55_P4	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X9_P4	1.200	0.952	1.1424
X13_P4	1.200	0.952	1.1424
X16_P4	1.200	1.360	1.6320
X19_P4	1.200	1.496	1.7952
X22_P4	1.200	1.768	2.1216
X25_P4	1.200	1.904	2.2848
X37_P4	1.200	2.584	3.1008
X49_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P4	X6_P4	X9_P4	X13_P4
A	0.0007	0.0008	0.0013	0.0016
B	0.0007	0.0008	0.0015	0.0018
C	0.0007	0.0009	0.0012	0.0015
	X16_P4	X19_P4	X22_P4	X25_P4
A	0.0022	0.0025	0.0030	0.0033
B	0.0022	0.0029	0.0032	0.0039
C	0.0020	0.0023	0.0028	0.0030
	X37_P4	X49_P4		
A	0.0050	0.0068		
B	0.0051	0.0068		

C	0.0045	0.0063		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0094	0.0090	2.3835	1.7590
A to Z ↑	0.0189	0.0172	9.5804	6.7539
B to Z ↓	0.0086	0.0082	2.3923	1.7645
B to Z ↑	0.0182	0.0163	9.6011	6.7709
C to Z ↓	0.0075	0.0069	2.4128	1.7825
C to Z ↑	0.0176	0.0155	9.6198	6.7838
	X9_P4	**X13_P4**	**X9_P4**	**X13_P4**
A to Z ↓	0.0093	0.0092	1.1576	0.8916
A to Z ↑	0.0190	0.0177	4.5134	3.3613
B to Z ↓	0.0085	0.0081	1.1299	0.8556
B to Z ↑	0.0190	0.0171	4.5249	3.3699
C to Z ↓	0.0063	0.0060	1.1420	0.8734
C to Z ↑	0.0146	0.0135	4.5316	3.3759
	X16_P4	**X19_P4**	**X16_P4**	**X19_P4**
A to Z ↓	0.0092	0.0091	0.6923	0.5861
A to Z ↑	0.0182	0.0178	2.7244	2.2506
B to Z ↓	0.0086	0.0085	0.6954	0.5745
B to Z ↑	0.0177	0.0179	2.7314	2.2559
C to Z ↓	0.0066	0.0065	0.7005	0.5986
C to Z ↑	0.0151	0.0143	2.7364	2.2611
	X22_P4	**X25_P4**	**X22_P4**	**X25_P4**
A to Z ↓	0.0092	0.0091	0.5083	0.4468
A to Z ↑	0.0179	0.0177	1.9462	1.6934
B to Z ↓	0.0084	0.0082	0.5002	0.4306
B to Z ↑	0.0176	0.0176	1.9508	1.6979
C to Z ↓	0.0062	0.0061	0.5066	0.4485
C to Z ↑	0.0141	0.0134	1.9556	1.7014
	X37_P4	**X49_P4**	**X37_P4**	**X49_P4**
A to Z ↓	0.0091	0.0092	0.3074	0.2329
A to Z ↑	0.0172	0.0172	1.1362	0.8563
B to Z ↓	0.0083	0.0084	0.3045	0.2309
B to Z ↑	0.0165	0.0165	1.1394	0.8586
C to Z ↓	0.0065	0.0066	0.3088	0.2342
C to Z ↑	0.0136	0.0137	1.1416	0.8607

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	1.023e-06	1.000e-20
X6_P4	1.699e-06	1.000e-20
X9_P4	2.220e-06	1.000e-20
X13_P4	3.424e-06	1.000e-20
X16_P4	3.875e-06	1.000e-20
X19_P4	5.131e-06	1.000e-20
X22_P4	5.563e-06	1.000e-20
X25_P4	6.757e-06	1.000e-20
X37_P4	9.924e-06	1.000e-20

X49_P4	1.318e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	3.701e-05	4.998e-05	9.269e-05	1.193e-04
B (output stable)	8.375e-06	1.593e-05	5.206e-05	6.480e-05
C (output stable)	2.914e-05	4.844e-05	1.129e-04	1.526e-04
A to Z	1.302e-03	1.676e-03	2.786e-03	3.466e-03
B to Z	1.082e-03	1.373e-03	2.376e-03	2.886e-03
C to Z	8.930e-04	1.105e-03	1.593e-03	1.959e-03
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	1.428e-04	1.717e-04	2.055e-04	2.373e-04
B (output stable)	6.716e-05	9.198e-05	1.078e-04	1.301e-04
C (output stable)	1.623e-04	2.156e-04	2.435e-04	2.965e-04
A to Z	4.416e-03	5.248e-03	6.085e-03	6.906e-03
B to Z	3.689e-03	4.457e-03	5.110e-03	5.851e-03
C to Z	2.741e-03	3.122e-03	3.572e-03	3.889e-03
	X37_P4	X49_P4		
A (output stable)	3.467e-04	4.582e-04		
B (output stable)	1.708e-04	2.196e-04		
C (output stable)	4.224e-04	5.528e-04		
A to Z	1.002e-02	1.334e-02		
B to Z	8.259e-03	1.099e-02		
C to Z	5.755e-03	7.724e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

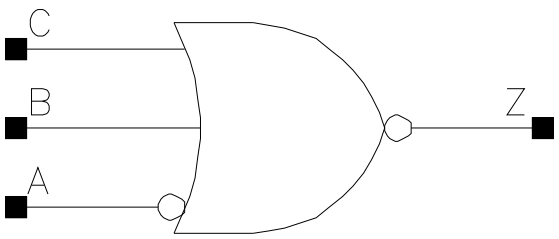
Pin Cycle (vdds)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P4	X49_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.680	0.8160
X13_P4	1.200	1.224	1.4688
X19_P4	1.200	1.496	1.7952
X25_P4	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0008	0.0011	0.0011	0.0021
B	0.0008	0.0017	0.0025	0.0034
C	0.0009	0.0015	0.0023	0.0031

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X13_P4**	**X6_P4**	**X13_P4**
A to Z ↓	0.0235	0.0221	1.6678	0.9314
A to Z ↑	0.0258	0.0253	6.8145	3.3498
B to Z ↓	0.0084	0.0081	1.7712	0.8608
B to Z ↑	0.0166	0.0170	6.8618	3.3702
C to Z ↓	0.0070	0.0059	1.7825	0.8743
C to Z ↑	0.0158	0.0133	6.8745	3.3760
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0252	0.0222	0.5649	0.4294

A to Z ↑	0.0279	0.0255	2.2574	1.6934
B to Z ↓	0.0086	0.0083	0.5984	0.4468
B to Z ↑	0.0167	0.0166	2.2730	1.7052
C to Z ↓	0.0065	0.0062	0.5994	0.4510
C to Z ↑	0.0143	0.0136	2.2777	1.7089

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P4	2.439e-06	1.000e-20
X13_P4	5.674e-06	1.000e-20
X19_P4	7.140e-06	1.000e-20
X25_P4	1.086e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	1.394e-03	2.493e-03	3.232e-03	4.925e-03
B (output stable)	3.085e-05	1.026e-04	1.275e-04	1.850e-04
C (output stable)	6.147e-05	2.130e-04	2.503e-04	3.732e-04
A to Z	3.112e-03	6.129e-03	8.437e-03	1.191e-02
B to Z	1.382e-03	2.872e-03	4.175e-03	5.563e-03
C to Z	1.121e-03	1.947e-03	3.101e-03	3.914e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

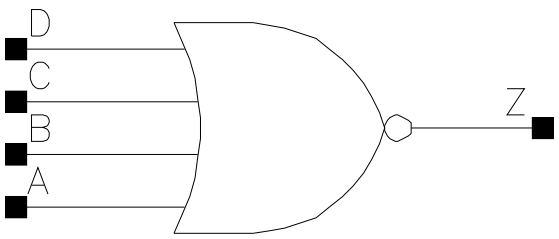
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	1.904	2.2848
X32_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X32_P4
A	0.0007	0.0007	0.0007	0.0009
B	0.0007	0.0007	0.0009	0.0011
C	0.0006	0.0006	0.0008	0.0010
D	0.0007	0.0006	0.0008	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0276	0.0276	1.6291	0.8036
A to Z ↑	0.0397	0.0427	2.3695	1.1735
B to Z ↓	0.0263	0.0266	1.6298	0.8039
B to Z ↑	0.0402	0.0435	2.3663	1.1728
C to Z ↓	0.0271	0.0276	1.6304	0.8033
C to Z ↑	0.0404	0.0438	2.3703	1.1733

D to Z ↓	0.0264	0.0270	1.6299	0.8029
D to Z ↑	0.0412	0.0450	2.3696	1.1740
	X25_P4	**X32_P4**	**X25_P4**	**X32_P4**
A to Z ↓	0.0284	0.0302	0.5603	0.4398
A to Z ↑	0.0419	0.0405	0.8061	0.6082
B to Z ↓	0.0275	0.0291	0.5601	0.4395
B to Z ↑	0.0429	0.0412	0.8061	0.6083
C to Z ↓	0.0275	0.0298	0.5585	0.4381
C to Z ↑	0.0415	0.0408	0.8043	0.6091
D to Z ↓	0.0264	0.0282	0.5584	0.4386
D to Z ↑	0.0424	0.0414	0.8047	0.6080

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	4.685e-06	1.000e-20
X17_P4	8.257e-06	1.000e-20
X25_P4	1.267e-05	1.000e-20
X32_P4	1.717e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	5.495e-04	6.677e-04	9.326e-04	1.180e-03
B (output stable)	4.837e-04	6.006e-04	8.536e-04	1.070e-03
C (output stable)	5.227e-04	6.221e-04	9.836e-04	1.257e-03
D (output stable)	4.586e-04	5.596e-04	8.946e-04	1.142e-03
A to Z	3.832e-03	5.919e-03	8.946e-03	1.121e-02
B to Z	3.682e-03	5.777e-03	8.724e-03	1.095e-02
C to Z	3.875e-03	5.901e-03	8.426e-03	1.066e-02
D to Z	3.719e-03	5.758e-03	8.231e-03	1.038e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

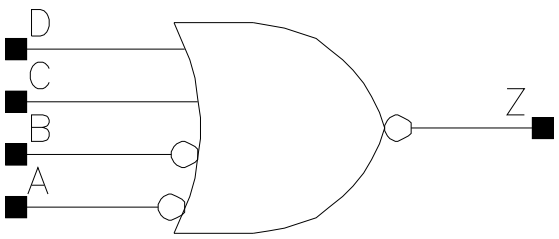
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X13_P4	1.200	1.496	1.7952
X19_P4	1.200	2.040	2.4480
X25_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0010	0.0011	0.0020	0.0020
B	0.0011	0.0015	0.0020	0.0021
C	0.0008	0.0017	0.0024	0.0032
D	0.0008	0.0015	0.0023	0.0030

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X13_P4	X6_P4	X13_P4
A to Z ↓	0.0203	0.0252	1.6242	0.8144
A to Z ↑	0.0258	0.0320	6.5601	3.4128
B to Z ↓	0.0189	0.0241	1.6234	0.8142
B to Z ↑	0.0264	0.0331	6.5634	3.4137
C to Z ↓	0.0088	0.0083	1.7991	0.8618
C to Z ↑	0.0167	0.0174	6.6126	3.4347

D to Z ↓	0.0072	0.0062	1.8017	0.8714
D to Z ↑	0.0156	0.0140	6.6215	3.4398
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0222	0.0243	0.5589	0.4210
A to Z ↑	0.0287	0.0311	2.2594	1.7097
B to Z ↓	0.0203	0.0227	0.5580	0.4206
B to Z ↑	0.0291	0.0319	2.2590	1.7096
C to Z ↓	0.0086	0.0085	0.5988	0.4486
C to Z ↑	0.0166	0.0167	2.2742	1.7203
D to Z ↓	0.0065	0.0062	0.6000	0.4508
D to Z ↑	0.0143	0.0136	2.2783	1.7234

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P4	3.586e-06	1.000e-20
X13_P4	4.998e-06	1.000e-20
X19_P4	8.200e-06	1.000e-20
X25_P4	9.482e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	8.772e-04	1.424e-03	2.179e-03	2.604e-03
B (output stable)	8.186e-04	1.375e-03	2.057e-03	2.510e-03
C (output stable)	2.903e-05	9.488e-05	1.367e-04	1.935e-04
D (output stable)	6.930e-05	2.254e-04	2.889e-04	4.463e-04
A to Z	3.782e-03	7.010e-03	1.045e-02	1.335e-02
B to Z	3.586e-03	6.666e-03	9.751e-03	1.271e-02
C to Z	1.437e-03	2.905e-03	4.150e-03	5.486e-03
D to Z	1.164e-03	2.035e-03	3.104e-03	3.878e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

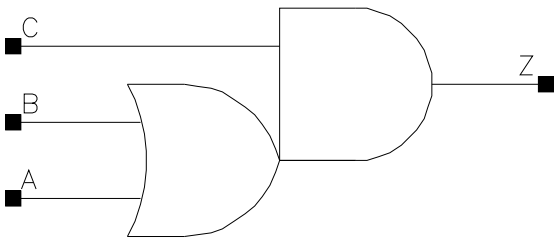
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0010	0.0010	0.0019
B	0.0011	0.0011	0.0021
C	0.0011	0.0011	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0220	0.0254	1.6842	0.8404
A to Z ↑	0.0200	0.0224	2.3892	1.1768
B to Z ↓	0.0224	0.0262	1.6836	0.8410
B to Z ↑	0.0181	0.0206	2.3823	1.1754
C to Z ↓	0.0203	0.0223	1.6676	0.8290
C to Z ↑	0.0188	0.0208	2.3859	1.1764
	X33_P4		**X33_P4**	
A to Z ↓	0.0265		0.4263	
A to Z ↑	0.0241		0.5906	

B to Z ↓	0.0273		0.4266	
B to Z ↑	0.0219		0.5887	
C to Z ↓	0.0228		0.4196	
C to Z ↑	0.0215		0.5891	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	4.734e-06	1.000e-20
X17_P4	7.208e-06	1.000e-20
X33_P4	1.410e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	1.237e-04	1.245e-04	2.405e-04
B (output stable)	1.262e-04	1.262e-04	2.434e-04
C (output stable)	6.174e-05	6.421e-05	1.233e-04
A to Z	2.949e-03	4.424e-03	9.231e-03
B to Z	2.670e-03	4.139e-03	8.678e-03
C to Z	3.226e-03	4.584e-03	9.405e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

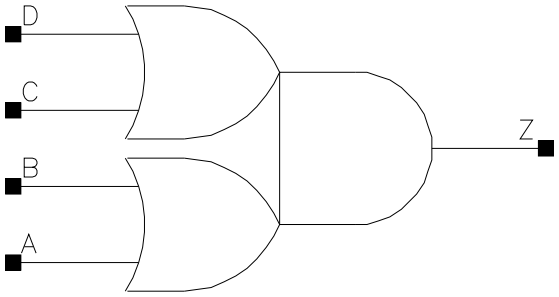
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0010	0.0019
B	0.0007	0.0011	0.0019
C	0.0007	0.0010	0.0020
D	0.0007	0.0010	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0370	0.0314	1.6303	0.8318
A to Z ↑	0.0267	0.0239	2.3400	1.1708
B to Z ↓	0.0382	0.0325	1.6315	0.8319
B to Z ↑	0.0256	0.0226	2.3372	1.1689

C to Z ↓	0.0323	0.0278	1.6216	0.8285
C to Z ↑	0.0260	0.0241	2.3398	1.1709
D to Z ↓	0.0328	0.0284	1.6212	0.8286
D to Z ↑	0.0245	0.0221	2.3369	1.1689
	X33_P4		**X33_P4**	
A to Z ↓	0.0320		0.4284	
A to Z ↑	0.0241		0.5889	
B to Z ↓	0.0318		0.4287	
B to Z ↑	0.0223		0.5876	
C to Z ↓	0.0279		0.4266	
C to Z ↑	0.0239		0.5883	
D to Z ↓	0.0273		0.4270	
D to Z ↑	0.0217		0.5873	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	3.150e-06	1.000e-20
X17_P4	7.136e-06	1.000e-20
X33_P4	1.366e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.551e-05	4.276e-05	1.279e-04
B (output stable)	2.192e-05	4.515e-05	1.530e-04
C (output stable)	8.802e-05	1.212e-04	2.820e-04
D (output stable)	8.750e-05	1.251e-04	3.170e-04
A to Z	3.442e-03	5.638e-03	1.116e-02
B to Z	3.285e-03	5.331e-03	1.029e-02
C to Z	2.992e-03	5.019e-03	9.894e-03
D to Z	2.834e-03	4.719e-03	8.989e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

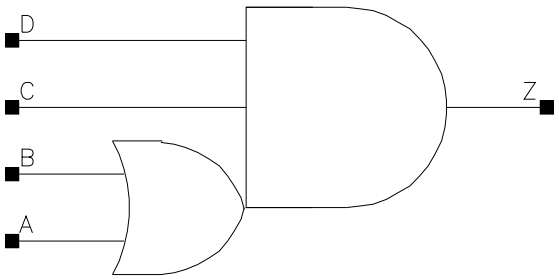
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	1.088	1.3056
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0007	0.0010	0.0016	0.0020
B	0.0007	0.0011	0.0017	0.0020
C	0.0007	0.0010	0.0017	0.0020
D	0.0007	0.0011	0.0017	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0315	0.0295	1.7187	0.8399
A to Z ↑	0.0313	0.0297	2.4263	1.1731
B to Z ↓	0.0324	0.0296	1.7178	0.8398
B to Z ↑	0.0297	0.0272	2.4250	1.1728
C to Z ↓	0.0271	0.0249	1.6827	0.8249

C to Z ↑	0.0287	0.0270	2.4214	1.1714
D to Z ↓	0.0262	0.0240	1.6828	0.8249
D to Z ↑	0.0303	0.0284	2.4217	1.1720
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0308	0.0296	0.5726	0.4282
A to Z ↑	0.0303	0.0310	0.7993	0.5983
B to Z ↓	0.0306	0.0294	0.5725	0.4286
B to Z ↑	0.0279	0.0283	0.7974	0.5966
C to Z ↓	0.0262	0.0251	0.5629	0.4208
C to Z ↑	0.0278	0.0278	0.7967	0.5965
D to Z ↓	0.0249	0.0240	0.5620	0.4205
D to Z ↑	0.0283	0.0286	0.7973	0.5971

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	3.332e-06	1.000e-20
X17_P4	7.576e-06	1.000e-20
X25_P4	1.102e-05	1.000e-20
X33_P4	1.478e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	8.623e-05	1.627e-04	2.901e-04	3.227e-04
B (output stable)	9.010e-05	1.740e-04	2.884e-04	3.247e-04
C (output stable)	1.468e-05	3.077e-05	7.357e-05	8.502e-05
D (output stable)	3.670e-05	8.142e-05	2.378e-04	2.632e-04
A to Z	2.896e-03	5.258e-03	8.377e-03	1.053e-02
B to Z	2.751e-03	4.892e-03	7.715e-03	9.677e-03
C to Z	3.084e-03	5.488e-03	8.973e-03	1.101e-02
D to Z	2.965e-03	5.268e-03	8.388e-03	1.042e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

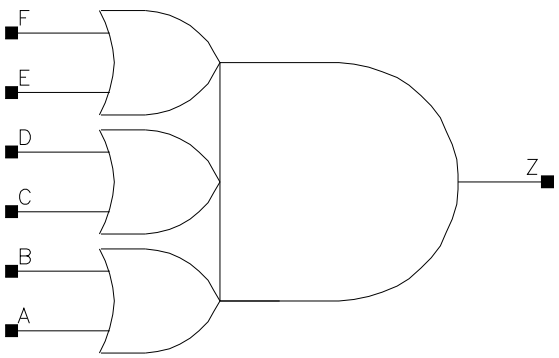
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0010	0.0017
B	0.0007	0.0010	0.0019
C	0.0007	0.0010	0.0017
D	0.0007	0.0010	0.0020
E	0.0007	0.0010	0.0018
F	0.0007	0.0010	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0421	0.0361	1.7473	0.8511
A to Z ↑	0.0335	0.0313	2.4068	1.1873
B to Z ↓	0.0431	0.0373	1.7476	0.8516
B to Z ↑	0.0323	0.0302	2.4061	1.1874
C to Z ↓	0.0387	0.0343	1.7377	0.8502
C to Z ↑	0.0343	0.0315	2.4072	1.1875
D to Z ↓	0.0399	0.0353	1.7384	0.8508
D to Z ↑	0.0327	0.0299	2.4046	1.1874
E to Z ↓	0.0338	0.0303	1.7288	0.8466
E to Z ↑	0.0321	0.0301	2.4052	1.1865
F to Z ↓	0.0350	0.0312	1.7299	0.8471
F to Z ↑	0.0306	0.0285	2.4019	1.1851
	X33_P4		X33_P4	
A to Z ↓	0.0363		0.4353	
A to Z ↑	0.0320		0.5986	
B to Z ↓	0.0376		0.4355	
B to Z ↑	0.0298		0.5972	
C to Z ↓	0.0335		0.4332	
C to Z ↑	0.0321		0.5985	
D to Z ↓	0.0346		0.4335	
D to Z ↑	0.0300		0.5969	
E to Z ↓	0.0298		0.4313	
E to Z ↑	0.0309		0.5977	
F to Z ↓	0.0307		0.4317	
F to Z ↑	0.0287		0.5965	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	3.434e-06	1.000e-20
X17_P4	8.104e-06	1.000e-20
X33_P4	1.534e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	1.989e-05	3.520e-05	6.561e-05
B (output stable)	1.703e-05	4.058e-05	6.948e-05
C (output stable)	5.561e-05	8.828e-05	1.840e-04
D (output stable)	5.369e-05	9.315e-05	1.907e-04
E (output stable)	1.321e-04	2.036e-04	3.855e-04
F (output stable)	1.409e-04	2.160e-04	4.148e-04
A to Z	3.952e-03	6.657e-03	1.299e-02
B to Z	3.784e-03	6.367e-03	1.240e-02
C to Z	3.607e-03	6.167e-03	1.193e-02
D to Z	3.448e-03	5.870e-03	1.133e-02
E to Z	3.175e-03	5.537e-03	1.074e-02
F to Z	3.034e-03	5.261e-03	1.019e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

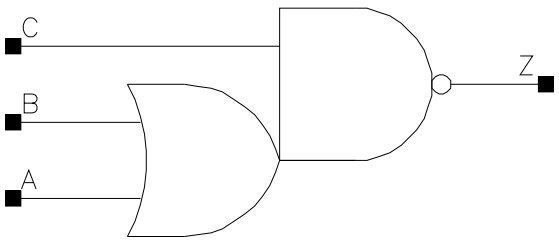
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X34_P4	1.200	2.720	3.2640
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X34_P4	X46_P4
A	0.0008	0.0024	0.0049	0.0064
B	0.0008	0.0022	0.0044	0.0059
C	0.0009	0.0026	0.0052	0.0068

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0111	0.0115	3.1486	1.0297
A to Z ↑	0.0126	0.0135	4.5590	1.5570
B to Z ↓	0.0090	0.0093	3.0785	1.0343
B to Z ↑	0.0125	0.0125	4.5862	1.5669
C to Z ↓	0.0103	0.0104	2.8588	0.9447
C to Z ↑	0.0125	0.0124	2.4397	0.8129
	X34_P4	**X46_P4**	**X34_P4**	**X46_P4**
A to Z ↓	0.0120	0.0120	0.5253	0.4015

A to Z ↑	0.0140	0.0138	0.7768	0.5986
B to Z ↓	0.0096	0.0097	0.5328	0.4089
B to Z ↑	0.0127	0.0128	0.7820	0.6030
C to Z ↓	0.0108	0.0107	0.4843	0.3707
C to Z ↑	0.0126	0.0126	0.4066	0.3118

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P4	2.526e-06	1.000e-20
X17_P4	7.450e-06	1.000e-20
X34_P4	1.470e-05	1.000e-20
X46_P4	1.941e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	1.118e-04	3.685e-04	7.764e-04	9.632e-04
B (output stable)	1.148e-04	3.768e-04	7.949e-04	9.825e-04
C (output stable)	5.789e-05	1.919e-04	4.029e-04	5.072e-04
A to Z	1.329e-03	4.261e-03	8.878e-03	1.144e-02
B to Z	1.065e-03	3.197e-03	6.579e-03	8.579e-03
C to Z	1.615e-03	4.941e-03	1.022e-02	1.321e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

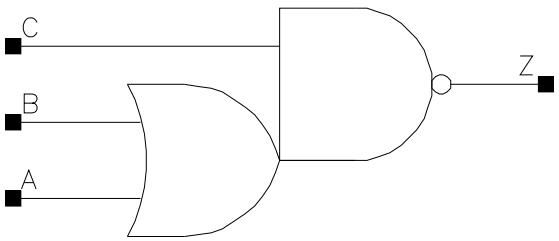
Pin Cycle (vdds)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.544	0.6528
X11_P4	1.200	0.952	1.1424
X17_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X17_P4	X23_P4
A	0.0008	0.0016	0.0025	0.0035
B	0.0008	0.0017	0.0024	0.0031
C	0.0008	0.0016	0.0024	0.0033
	X46_P4			
A	0.0069			
B	0.0063			
C	0.0066			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0114	0.0115	3.1751	1.4813
A to Z ↑	0.0160	0.0160	4.8121	2.2765
B to Z ↓	0.0097	0.0096	3.1160	1.4408

B to Z ↑	0.0162	0.0161	4.8336	2.2868
C to Z ↓	0.0091	0.0091	2.9690	1.3792
C to Z ↑	0.0095	0.0094	2.6267	1.2340
	X17_P4	**X23_P4**	**X17_P4**	**X23_P4**
A to Z ↓	0.0111	0.0117	1.0286	0.7625
A to Z ↑	0.0151	0.0166	1.5072	1.1522
B to Z ↓	0.0092	0.0096	1.0255	0.7625
B to Z ↑	0.0150	0.0157	1.5141	1.1579
C to Z ↓	0.0088	0.0091	0.9695	0.7175
C to Z ↑	0.0087	0.0090	0.8203	0.6255
	X46_P4		**X46_P4**	
A to Z ↓	0.0116		0.3984	
A to Z ↑	0.0163		0.5834	
B to Z ↓	0.0094		0.3943	
B to Z ↑	0.0154		0.5868	
C to Z ↓	0.0091		0.3734	
C to Z ↑	0.0087		0.3168	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	2.443e-06	1.000e-20
X11_P4	5.188e-06	1.000e-20
X17_P4	7.617e-06	1.000e-20
X23_P4	1.010e-05	1.000e-20
X46_P4	1.962e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	2.918e-05	6.263e-05	9.245e-05	1.680e-04
B (output stable)	2.873e-05	6.697e-05	9.477e-05	1.731e-04
C (output stable)	2.833e-04	6.670e-04	8.212e-04	1.267e-03
A to Z	1.655e-03	3.518e-03	4.920e-03	7.304e-03
B to Z	1.368e-03	2.939e-03	3.983e-03	5.637e-03
C to Z	1.094e-03	2.384e-03	3.304e-03	4.705e-03
	X46_P4			
A (output stable)	3.200e-04			
B (output stable)	3.255e-04			
C (output stable)	2.314e-03			
A to Z	1.410e-02			
B to Z	1.077e-02			
C to Z	9.016e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

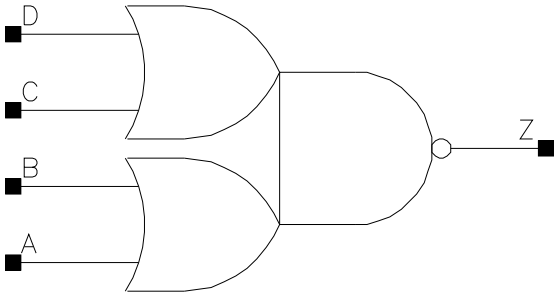
	X46_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0009	0.0017	0.0025	0.0034
B	0.0008	0.0015	0.0023	0.0031
C	0.0008	0.0016	0.0024	0.0033
D	0.0008	0.0015	0.0022	0.0030
	X42_P4			
A	0.0069			
B	0.0063			
C	0.0065			
D	0.0061			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0125	0.0135	2.9240	1.4554
A to Z ↑	0.0187	0.0188	5.0793	2.3281
B to Z ↓	0.0111	0.0115	2.8585	1.4595
B to Z ↑	0.0187	0.0177	5.0939	2.3404
C to Z ↓	0.0113	0.0123	2.9805	1.4702
C to Z ↑	0.0136	0.0145	4.9544	2.3365
D to Z ↓	0.0094	0.0098	2.8967	1.4792
D to Z ↑	0.0133	0.0126	4.9812	2.3545
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0128	0.0131	0.9963	0.7184
A to Z ↑	0.0176	0.0182	1.5693	1.1572
B to Z ↓	0.0112	0.0110	0.9991	0.7177
B to Z ↑	0.0171	0.0174	1.5779	1.1629
C to Z ↓	0.0119	0.0120	1.0088	0.7268
C to Z ↑	0.0134	0.0136	1.5757	1.1591
D to Z ↓	0.0098	0.0096	1.0178	0.7294
D to Z ↑	0.0122	0.0122	1.5880	1.1676
	X42_P4		**X42_P4**	
A to Z ↓	0.0134		0.3775	
A to Z ↑	0.0183		0.5907	
B to Z ↓	0.0114		0.3730	
B to Z ↑	0.0176		0.5937	
C to Z ↓	0.0127		0.3833	
C to Z ↑	0.0140		0.5870	
D to Z ↓	0.0101		0.3794	
D to Z ↑	0.0126		0.5916	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	2.832e-06	1.000e-20
X10_P4	6.225e-06	1.000e-20
X15_P4	9.070e-06	1.000e-20
X21_P4	1.206e-05	1.000e-20
X42_P4	2.362e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	3.879e-05	1.243e-04	1.584e-04	2.357e-04
B (output stable)	4.009e-05	1.488e-04	1.753e-04	2.540e-04
C (output stable)	1.046e-04	2.704e-04	3.515e-04	5.102e-04
D (output stable)	1.091e-04	2.948e-04	3.670e-04	5.324e-04
A to Z	1.983e-03	4.462e-03	6.153e-03	8.650e-03
B to Z	1.703e-03	3.581e-03	4.968e-03	6.956e-03
C to Z	1.414e-03	3.337e-03	4.545e-03	6.300e-03
D to Z	1.160e-03	2.462e-03	3.442e-03	4.715e-03
	X42_P4			
A (output stable)	4.609e-04			
B (output stable)	5.029e-04			
C (output stable)	9.914e-04			
D (output stable)	1.043e-03			

A to Z	1.721e-02			
B to Z	1.385e-02			
C to Z	1.275e-02			
D to Z	9.615e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

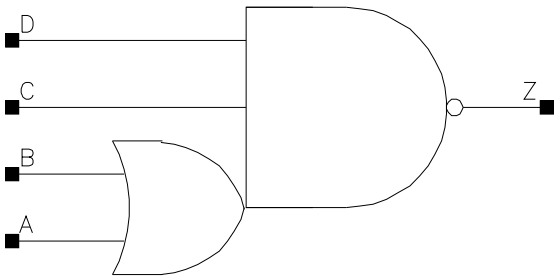
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X21_P4	1.200	2.448	2.9376
X31_P4	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X21_P4	X31_P4
A	0.0008	0.0015	0.0031	0.0047
B	0.0010	0.0015	0.0029	0.0043
C	0.0008	0.0017	0.0034	0.0051
D	0.0008	0.0016	0.0032	0.0048

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0161	0.0155	3.9770	2.1346
A to Z ↑	0.0171	0.0158	4.5855	2.3101
B to Z ↓	0.0140	0.0125	4.0352	2.1458
B to Z ↑	0.0170	0.0144	4.6208	2.3263
C to Z ↓	0.0143	0.0148	3.7594	2.0108

C to Z ↑	0.0153	0.0149	2.3806	1.2001
D to Z ↓	0.0153	0.0146	3.7838	2.0242
D to Z ↑	0.0145	0.0135	2.4161	1.2034
	X21_P4	**X31_P4**	**X21_P4**	**X31_P4**
A to Z ↓	0.0157	0.0159	1.1147	0.7574
A to Z ↑	0.0154	0.0154	1.1541	0.7756
B to Z ↓	0.0127	0.0129	1.1218	0.7648
B to Z ↑	0.0140	0.0141	1.1616	0.7812
C to Z ↓	0.0146	0.0147	1.0515	0.7155
C to Z ↑	0.0146	0.0146	0.6092	0.4121
D to Z ↓	0.0148	0.0150	1.0576	0.7196
D to Z ↑	0.0133	0.0133	0.6102	0.4115

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	2.234e-06	1.000e-20
X10_P4	4.214e-06	1.000e-20
X21_P4	8.067e-06	1.000e-20
X31_P4	1.193e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	1.616e-04	3.447e-04	6.556e-04	9.689e-04
B (output stable)	1.752e-04	3.497e-04	6.539e-04	9.618e-04
C (output stable)	2.927e-05	8.618e-05	1.654e-04	2.406e-04
D (output stable)	8.428e-05	2.573e-04	4.602e-04	6.615e-04
A to Z	1.978e-03	3.476e-03	6.735e-03	1.002e-02
B to Z	1.559e-03	2.611e-03	5.031e-03	7.528e-03
C to Z	2.361e-03	4.544e-03	8.697e-03	1.289e-02
D to Z	2.135e-03	3.840e-03	7.396e-03	1.100e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

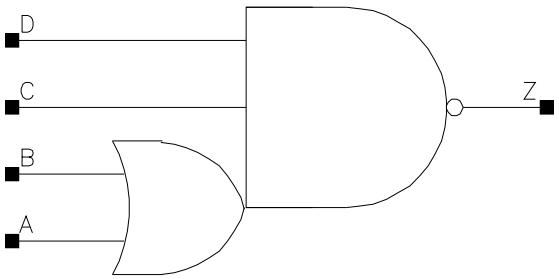
Pin Cycle (vdds)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0009	0.0017	0.0026	0.0035
B	0.0008	0.0016	0.0024	0.0032
C	0.0008	0.0016	0.0025	0.0033
D	0.0008	0.0016	0.0024	0.0032

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0147	0.0159	4.0536	2.1218
A to Z ↑	0.0185	0.0202	4.4401	2.2683
B to Z ↓	0.0129	0.0135	3.9761	2.1243
B to Z ↑	0.0188	0.0193	4.4560	2.2789
C to Z ↓	0.0120	0.0135	3.8352	2.0252

C to Z ↑	0.0119	0.0126	2.4322	1.2297
D to Z ↓	0.0121	0.0128	3.8603	2.0379
D to Z ↑	0.0104	0.0106	2.4509	1.2402
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0156	0.0157	1.4599	1.1026
A to Z ↑	0.0193	0.0198	1.5304	1.1621
B to Z ↓	0.0135	0.0134	1.4530	1.1010
B to Z ↑	0.0188	0.0193	1.5386	1.1672
C to Z ↓	0.0132	0.0134	1.3888	1.0498
C to Z ↑	0.0120	0.0123	0.8206	0.6174
D to Z ↓	0.0126	0.0131	1.3978	1.0562
D to Z ↑	0.0101	0.0104	0.8270	0.6221

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	2.233e-06	1.000e-20
X10_P4	4.281e-06	1.000e-20
X15_P4	6.139e-06	1.000e-20
X21_P4	8.241e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	2.273e-05	4.992e-05	7.231e-05	9.659e-05
B (output stable)	2.183e-05	5.465e-05	7.343e-05	9.866e-05
C (output stable)	1.005e-04	2.118e-04	3.182e-04	4.157e-04
D (output stable)	1.747e-04	5.701e-04	7.036e-04	1.026e-03
A to Z	2.238e-03	4.875e-03	6.897e-03	9.426e-03
B to Z	1.908e-03	3.939e-03	5.590e-03	7.626e-03
C to Z	1.546e-03	3.425e-03	4.770e-03	6.598e-03
D to Z	1.339e-03	2.822e-03	3.966e-03	5.457e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

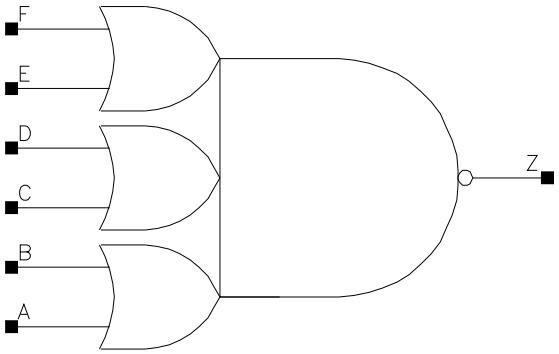
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	1.088	1.3056
X9_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X9_P4
A	0.0007	0.0017
B	0.0007	0.0016
C	0.0007	0.0017
D	0.0007	0.0015
E	0.0007	0.0016
F	0.0007	0.0015

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X9_P4	X3_P4	X9_P4
A to Z ↓	0.0186	0.0199	4.6632	1.9310
A to Z ↑	0.0250	0.0239	6.2545	2.2830
B to Z ↓	0.0174	0.0177	4.7001	1.9338
B to Z ↑	0.0260	0.0234	6.2756	2.2917
C to Z ↓	0.0182	0.0190	4.7153	1.9459
C to Z ↑	0.0218	0.0207	6.2791	2.2788
D to Z ↓	0.0166	0.0167	4.7559	1.9518
D to Z ↑	0.0226	0.0199	6.3057	2.2902
E to Z ↓	0.0157	0.0169	4.7478	1.9489
E to Z ↑	0.0170	0.0163	6.3049	2.2843
F to Z ↓	0.0142	0.0141	4.7922	1.9547
F to Z ↑	0.0175	0.0149	6.3465	2.3003

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	2.292e-06	1.000e-20
X9_P4	7.146e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X9_P4
A (output stable)	2.706e-05	1.024e-04
B (output stable)	2.616e-05	1.168e-04
C (output stable)	7.668e-05	2.219e-04
D (output stable)	8.045e-05	2.471e-04
E (output stable)	1.816e-04	4.360e-04
F (output stable)	1.921e-04	4.856e-04
A to Z	2.553e-03	6.687e-03
B to Z	2.326e-03	5.761e-03
C to Z	2.086e-03	5.441e-03
D to Z	1.870e-03	4.611e-03
E to Z	1.546e-03	4.230e-03
F to Z	1.353e-03	3.369e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

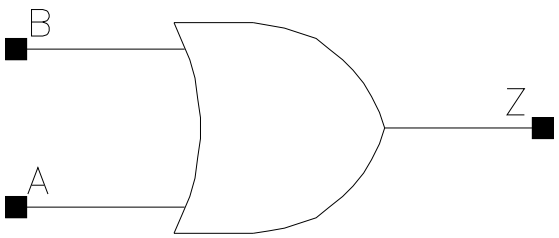
Pin Cycle (vdds)	X3_P4	X9_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X33_P4	1.200	1.360	1.6320
X50_P4	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P4	X16_P4	X33_P4	X50_P4
A	0.0008	0.0010	0.0019	0.0020
B	0.0007	0.0010	0.0019	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0287	0.0255	1.6880	0.8523
A to Z ↑	0.0188	0.0199	2.3543	1.1880
B to Z ↓	0.0292	0.0260	1.6886	0.8528
B to Z ↑	0.0176	0.0186	2.3530	1.1877
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0262	0.0310	0.4218	0.2898
A to Z ↑	0.0198	0.0199	0.5777	0.3920
B to Z ↓	0.0256	0.0308	0.4219	0.2899
B to Z ↑	0.0180	0.0184	0.5772	0.3914

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	2.297e-06	1.000e-20
X16_P4	4.908e-06	1.000e-20
X33_P4	9.763e-06	1.000e-20
X50_P4	1.251e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	2.579e-05	4.769e-05	1.571e-04	1.495e-04
B (output stable)	2.305e-05	5.172e-05	2.072e-04	1.926e-04
A to Z	2.592e-03	4.295e-03	8.942e-03	1.244e-02
B to Z	2.440e-03	4.035e-03	8.081e-03	1.164e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

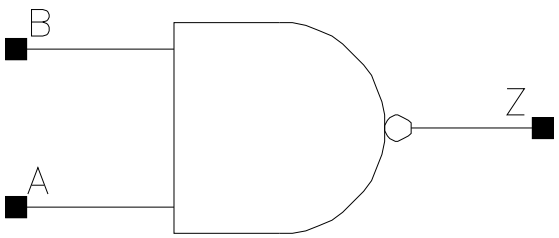
Pin Cycle (vdds)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X16_P4	1.200	0.952	1.1424
X24_P4	1.200	1.088	1.3056
X32_P4	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P4	X16_P4	X24_P4	X32_P4
A	0.0010	0.0010	0.0010	0.0010
B	0.0011	0.0011	0.0011	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0247	0.0256	1.6462	0.8581
A to Z ↑	0.0265	0.0273	2.3924	1.2232
B to Z ↓	0.0259	0.0268	1.6462	0.8580
B to Z ↑	0.0252	0.0255	2.3903	1.2209
	X24_P4	**X32_P4**	**X24_P4**	**X32_P4**
A to Z ↓	0.0281	0.0292	0.5796	0.4338
A to Z ↑	0.0292	0.0299	0.8179	0.6098
B to Z ↓	0.0294	0.0306	0.5796	0.4335
B to Z ↑	0.0274	0.0286	0.8174	0.6098

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	6.074e-06	1.000e-20
X16_P4	7.492e-06	1.000e-20
X24_P4	8.839e-06	1.000e-20
X32_P4	1.242e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	2.807e-05	2.808e-05	2.816e-05	2.957e-05
B (output stable)	7.100e-05	7.092e-05	7.104e-05	7.422e-05
A to Z	4.929e-03	5.748e-03	7.314e-03	9.644e-03
B to Z	4.732e-03	5.561e-03	7.138e-03	9.454e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

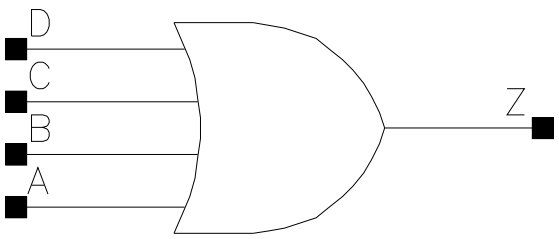
Pin Cycle (vdds)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P4	1.200	2.176	2.6112
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P4	X27_P4
A	0.0017	0.0020
B	0.0016	0.0020
C	0.0017	0.0020
D	0.0016	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P4	X27_P4	X20_P4	X27_P4
A to Z ↓	0.0292	0.0305	1.0008	0.7478
A to Z ↑	0.0203	0.0198	0.7765	0.5780
B to Z ↓	0.0290	0.0298	1.0013	0.7481
B to Z ↑	0.0191	0.0181	0.7756	0.5768
C to Z ↓	0.0283	0.0297	0.9999	0.7470
C to Z ↑	0.0194	0.0194	0.7777	0.5797
D to Z ↓	0.0280	0.0293	0.9997	0.7473
D to Z ↑	0.0182	0.0179	0.7771	0.5796

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X20_P4	7.712e-06	1.000e-20
X27_P4	1.151e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X20_P4	X27_P4
A (output stable)	1.883e-03	2.607e-03
B (output stable)	1.628e-03	2.240e-03
C (output stable)	1.753e-03	2.525e-03
D (output stable)	1.496e-03	2.207e-03
A to Z	8.029e-03	1.125e-02
B to Z	7.423e-03	1.031e-02
C to Z	7.162e-03	9.908e-03
D to Z	6.573e-03	9.116e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

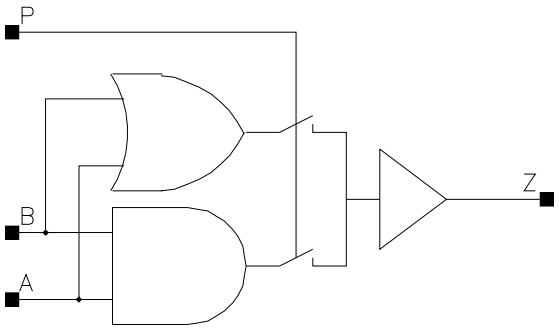
Pin Cycle (vdds)	X20_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X16_P4	1.200	1.224	1.4688
X25_P4	1.200	2.040	2.4480
X33_P4	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0012	0.0018	0.0032	0.0032
B	0.0012	0.0018	0.0036	0.0037
P	0.0007	0.0010	0.0019	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0349	0.0316	1.7153	0.8397
A to Z ↑	0.0247	0.0236	2.3955	1.1978
B to Z ↓	0.0349	0.0318	1.7240	0.8449
B to Z ↑	0.0256	0.0244	2.3979	1.1998
P to Z ↓	0.0323	0.0299	1.7228	0.8443
P to Z ↑	0.0249	0.0238	2.3956	1.1989
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**

A to Z ↓	0.0302	0.0322	0.5722	0.4324
A to Z ↑	0.0233	0.0245	0.8070	0.6040
B to Z ↓	0.0303	0.0320	0.5750	0.4343
B to Z ↑	0.0244	0.0255	0.8085	0.6051
P to Z ↓	0.0289	0.0309	0.5751	0.4339
P to Z ↑	0.0234	0.0246	0.8068	0.6037

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	3.034e-06	1.000e-20
X16_P4	7.083e-06	1.000e-20
X25_P4	1.189e-05	1.000e-20
X33_P4	1.384e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	5.707e-05	9.135e-05	1.997e-04	2.014e-04
B (output stable)	6.793e-05	1.283e-04	3.178e-04	3.182e-04
P (output stable)	1.527e-04	2.769e-04	4.769e-04	4.901e-04
A to Z	3.009e-03	5.226e-03	8.854e-03	1.041e-02
B to Z	2.923e-03	5.106e-03	8.504e-03	1.007e-02
P to Z	2.688e-03	4.774e-03	8.087e-03	9.652e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

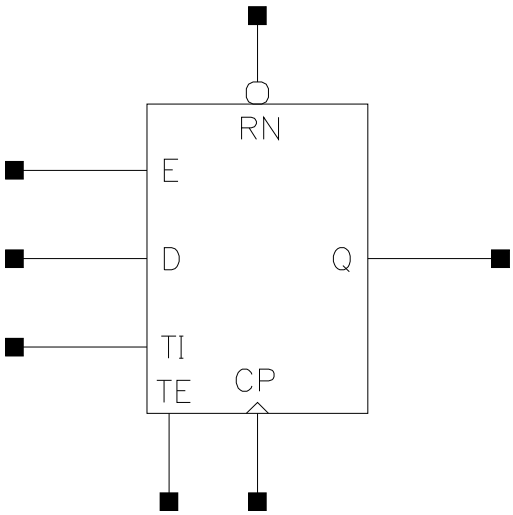
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.488	5.3856
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
E	0.0009	0.0011	0.0011	0.0011
RN	0.0009	0.0007	0.0008	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0625	0.0347	3.5726	1.6681
CP to Q ↑	0.0533	0.0458	4.8800	2.3702
RN to Q ↓	0.0545	0.0474	3.1602	1.7371
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0594	0.0623	0.8181	0.4295
CP to Q ↑	0.0731	0.0766	1.1614	0.5936
RN to Q ↓	0.0782	0.0811	0.8172	0.4292

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0835	0.0565	0.0565	0.0565
CP ↑	min_pulse_width to CP	0.0565	0.0317	0.0269	0.0269
D ↓	hold_rising to CP	-0.0838	-0.0387	-0.0387	-0.0387
D ↑	hold_rising to CP	-0.0533	-0.0137	-0.0137	-0.0137
D ↓	setup_rising to CP	0.1242	0.0750	0.0750	0.0750
D ↑	setup_rising to CP	0.0827	0.0444	0.0444	0.0444
E ↓	hold_rising to CP	-0.0577	-0.0598	-0.0598	-0.0598
E ↑	hold_rising to CP	-0.0484	-0.0143	-0.0143	-0.0143
E ↓	setup_rising to CP	0.1074	0.1051	0.1051	0.1051
E ↑	setup_rising to CP	0.1177	0.0803	0.0803	0.0803
RN ↓	min_pulse_width to RN	0.0566	0.0637	0.0566	0.0566
RN ↑	recovery_rising to CP	0.0151	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0103	-0.0055	-0.0055	-0.0055
TE ↓	hold_rising to CP	-0.0403	-0.0236	-0.0236	-0.0236
TE ↑	hold_rising to CP	-0.0337	-0.0181	-0.0181	-0.0181
TE ↓	setup_rising to CP	0.0777	0.0657	0.0657	0.0657
TE ↑	setup_rising to CP	0.1470	0.1030	0.1030	0.1030
TI ↓	hold_rising to CP	-0.1085	-0.0527	-0.0570	-0.0570
TI ↑	hold_rising to CP	-0.0383	-0.0204	-0.0202	-0.0202
TI ↓	setup_rising to CP	0.1439	0.0923	0.0923	0.0923
TI ↑	setup_rising to CP	0.0686	0.0502	0.0502	0.0502

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	7.910e-06	1.000e-20
X8_P4	9.580e-06	1.000e-20
X17_P4	1.290e-05	1.000e-20
X33_P4	1.806e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

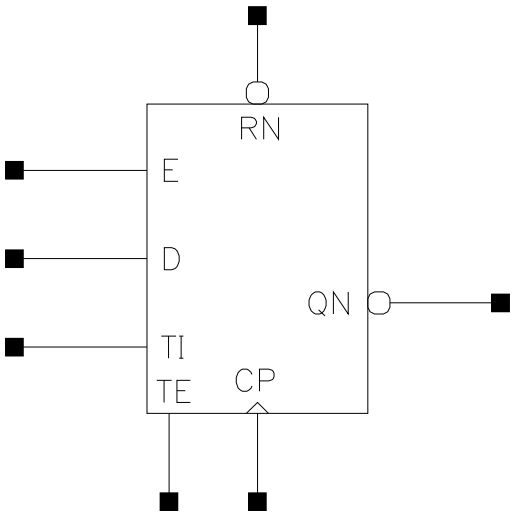
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	9.105e-03	9.163e-03	9.177e-03	9.185e-03
Clock 100Mhz Data 25Mhz	9.782e-03	9.898e-03	1.063e-02	1.152e-02
Clock 100Mhz Data 50Mhz	1.046e-02	1.063e-02	1.208e-02	1.385e-02
Clock = 0 Data 100Mhz	6.754e-03	6.465e-03	6.370e-03	6.323e-03
Clock = 1 Data 100Mhz	2.454e-03	2.500e-03	2.517e-03	2.525e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.624	5.5488
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
E	0.0009	0.0011	0.0011	0.0011
RN	0.0009	0.0008	0.0008	0.0008
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.0653	0.0615	3.1016	1.6157
CP to QN ↑	0.0701	0.0461	4.7753	2.2961
RN to QN ↑	0.0665	0.0663	4.7613	2.2955
	X17_P4	X33_P4	X17_P4	X33_P4
CP to QN ↓	0.0587	0.0618	0.8188	0.4288
CP to QN ↑	0.0475	0.0516	1.1608	0.5945
RN to QN ↑	0.0647	0.0712	1.1612	0.5938

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0835	0.0565	0.0565	0.0565
CP ↑	min_pulse_width to CP	0.0416	0.0269	0.0309	0.0315
D ↓	hold_rising to CP	-0.0864	-0.0387	-0.0387	-0.0387
D ↑	hold_rising to CP	-0.0533	-0.0137	-0.0137	-0.0137
D ↓	setup_rising to CP	0.1242	0.0750	0.0750	0.0750
D ↑	setup_rising to CP	0.0827	0.0444	0.0444	0.0444
E ↓	hold_rising to CP	-0.0577	-0.0598	-0.0598	-0.0598
E ↑	hold_rising to CP	-0.0484	-0.0143	-0.0143	-0.0143
E ↓	setup_rising to CP	0.1090	0.1051	0.1051	0.1051
E ↑	setup_rising to CP	0.1177	0.0803	0.0803	0.0803
RN ↓	min_pulse_width to RN	0.0540	0.0566	0.0659	0.0708
RN ↑	recovery_rising to CP	0.0151	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0103	-0.0051	-0.0055	-0.0055
TE ↓	hold_rising to CP	-0.0403	-0.0236	-0.0236	-0.0236
TE ↑	hold_rising to CP	-0.0337	-0.0181	-0.0181	-0.0185
TE ↓	setup_rising to CP	0.0777	0.0657	0.0652	0.0652
TE ↑	setup_rising to CP	0.1470	0.1030	0.1030	0.1030
TI ↓	hold_rising to CP	-0.1100	-0.0570	-0.0527	-0.0527
TI ↑	hold_rising to CP	-0.0383	-0.0202	-0.0204	-0.0204
TI ↓	setup_rising to CP	0.1439	0.0923	0.0966	0.0966
TI ↑	setup_rising to CP	0.0686	0.0502	0.0502	0.0502

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	7.824e-06	1.000e-20
X8_P4	8.980e-06	1.000e-20
X17_P4	1.181e-05	1.000e-20
X33_P4	1.588e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

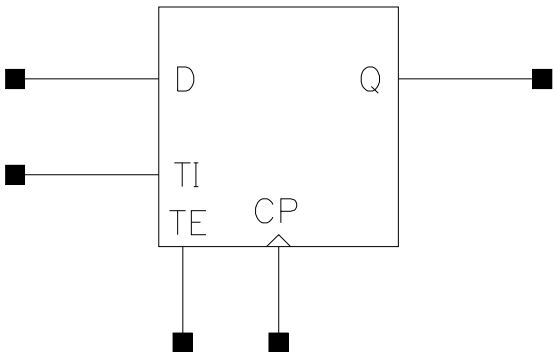
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	9.103e-03	9.160e-03	9.169e-03	9.174e-03
Clock 100Mhz Data 25Mhz	9.714e-03	9.939e-03	1.058e-02	1.148e-02
Clock 100Mhz Data 50Mhz	1.032e-02	1.072e-02	1.199e-02	1.378e-02
Clock = 0 Data 100Mhz	6.755e-03	6.469e-03	6.373e-03	6.325e-03
Clock = 1 Data 100Mhz	2.451e-03	2.503e-03	2.520e-03	2.528e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.400	4.0800
X8_P4	1.200	3.128	3.7536
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0516	0.0324	3.3875	1.6727
CP to Q ↑	0.0478	0.0417	4.9031	2.3355
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0488	0.0532	0.8043	0.4220
CP to Q ↑	0.0701	0.0741	1.1595	0.5936

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0740	0.0779	0.0779	0.0779
CP ↑	min_pulse_width to CP	0.0411	0.0269	0.0269	0.0269
D ↓	hold_rising to CP	-0.0496	-0.0169	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0185	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0852	0.0538	0.0538	0.0538
D ↑	setup_rising to CP	0.0432	0.0245	0.0245	0.0245
TE ↓	hold_rising to CP	-0.0337	-0.0143	-0.0169	-0.0143
TE ↑	hold_rising to CP	-0.0230	-0.0147	-0.0147	-0.0147
TE ↓	setup_rising to CP	0.0680	0.0516	0.0516	0.0516
TE ↑	setup_rising to CP	0.1269	0.1030	0.1030	0.1030
TI ↓	hold_rising to CP	-0.1036	-0.0635	-0.0635	-0.0635
TI ↑	hold_rising to CP	-0.0285	-0.0110	-0.0169	-0.0169
TI ↓	setup_rising to CP	0.1349	0.1030	0.1030	0.1030
TI ↑	setup_rising to CP	0.0575	0.0417	0.0417	0.0417

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	6.504e-06	1.000e-20
X8_P4	8.229e-06	1.000e-20
X17_P4	1.255e-05	1.000e-20
X33_P4	1.626e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

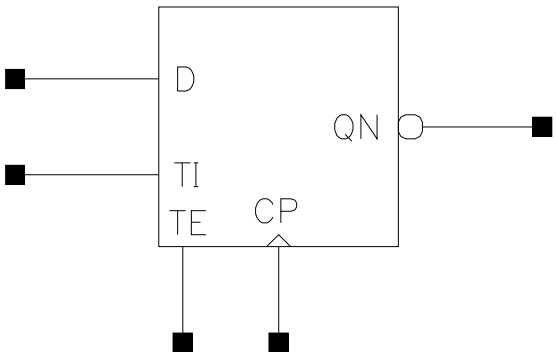
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	8.218e-03	8.326e-03	8.356e-03	8.371e-03
Clock 100Mhz Data 25Mhz	8.225e-03	8.351e-03	9.095e-03	9.861e-03
Clock 100Mhz Data 50Mhz	8.233e-03	8.377e-03	9.834e-03	1.135e-02
Clock = 0 Data 100Mhz	5.290e-03	4.949e-03	4.836e-03	4.781e-03
Clock = 1 Data 100Mhz	1.389e-03	7.190e-04	4.959e-04	3.843e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.536	4.2432
X8_P4	1.200	3.264	3.9168
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0607	0.0641	3.5280	1.6589
CP to QN ↑	0.0561	0.0424	4.8613	2.3035
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0504	0.0553	0.8046	0.4224
CP to QN ↑	0.0419	0.0461	1.1602	0.5924

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0741	0.0779	0.0779	0.0779
CP ↑	min_pulse_width to CP	0.0329	0.0269	0.0269	0.0269
D ↓	hold_rising to CP	-0.0496	-0.0169	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0181	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0826	0.0538	0.0538	0.0538
D ↑	setup_rising to CP	0.0432	0.0245	0.0245	0.0245
TE ↓	hold_rising to CP	-0.0333	-0.0143	-0.0143	-0.0143
TE ↑	hold_rising to CP	-0.0230	-0.0147	-0.0147	-0.0147
TE ↓	setup_rising to CP	0.0680	0.0516	0.0516	0.0516
TE ↑	setup_rising to CP	0.1269	0.1030	0.1025	0.1030
TI ↓	hold_rising to CP	-0.1036	-0.0635	-0.0635	-0.0635
TI ↑	hold_rising to CP	-0.0285	-0.0169	-0.0110	-0.0110
TI ↓	setup_rising to CP	0.1349	0.1030	0.1027	0.1030
TI ↑	setup_rising to CP	0.0575	0.0417	0.0417	0.0417

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	6.584e-06	1.000e-20
X8_P4	8.282e-06	1.000e-20
X17_P4	1.242e-05	1.000e-20
X33_P4	1.613e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

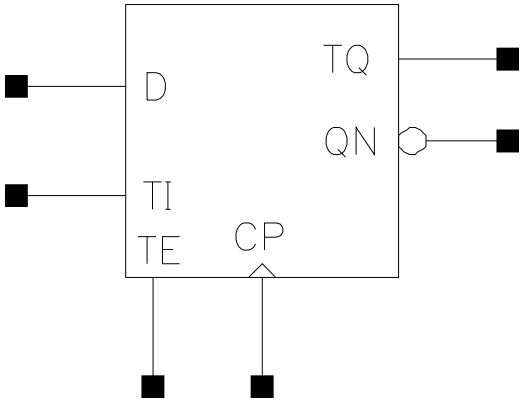
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	8.131e-03	8.279e-03	8.326e-03	8.349e-03
Clock 100Mhz Data 25Mhz	8.171e-03	8.438e-03	9.035e-03	9.820e-03
Clock 100Mhz Data 50Mhz	8.212e-03	8.597e-03	9.744e-03	1.129e-02
Clock = 0 Data 100Mhz	5.307e-03	4.957e-03	4.841e-03	4.782e-03
Clock = 1 Data 100Mhz	1.379e-03	7.142e-04	4.926e-04	3.819e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.536	4.2432
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0012	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0674	0.0585	3.2122	1.6316
CP to QN ↑	0.0678	0.0439	4.7904	2.3163
CP to TQ ↓	0.0477	0.0299	4.3275	3.0378
CP to TQ ↑	0.0492	0.0416	9.0686	6.4709
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0553	0.0598	0.8214	0.4314
CP to QN ↑	0.0452	0.0486	1.1763	0.6061
CP to TQ ↓	0.0308	0.0320	4.0451	4.0582
CP to TQ ↑	0.0423	0.0434	8.3909	8.8556

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0740	0.0779	0.0779	0.0779
CP ↑	min_pulse_width to CP	0.0410	0.0269	0.0269	0.0269
D ↓	hold_rising to CP	-0.0502	-0.0169	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0185	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0793	0.0538	0.0538	0.0538
D ↑	setup_rising to CP	0.0432	0.0245	0.0245	0.0245
TE ↓	hold_rising to CP	-0.0305	-0.0147	-0.0143	-0.0147
TE ↑	hold_rising to CP	-0.0230	-0.0147	-0.0147	-0.0147
TE ↓	setup_rising to CP	0.0680	0.0516	0.0516	0.0516
TE ↑	setup_rising to CP	0.1275	0.1030	0.1030	0.1030
TI ↓	hold_rising to CP	-0.1036	-0.0635	-0.0592	-0.0592
TI ↑	hold_rising to CP	-0.0285	-0.0153	-0.0153	-0.0153
TI ↓	setup_rising to CP	0.1349	0.1030	0.1030	0.1030
TI ↑	setup_rising to CP	0.0575	0.0417	0.0417	0.0417

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	6.956e-06	1.000e-20
X8_P4	9.101e-06	1.000e-20
X17_P4	1.151e-05	1.000e-20
X33_P4	1.588e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4

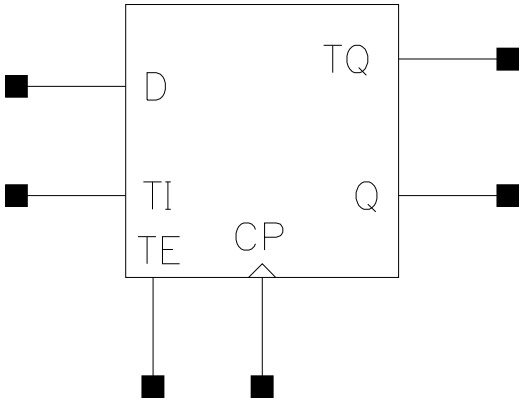
Clock 100Mhz Data 0Mhz	8.345e-03	8.389e-03	8.404e-03	8.414e-03
Clock 100Mhz Data 25Mhz	8.546e-03	8.758e-03	9.090e-03	9.995e-03
Clock 100Mhz Data 50Mhz	8.747e-03	9.127e-03	9.775e-03	1.158e-02
Clock = 0 Data 100Mhz	5.305e-03	4.964e-03	4.851e-03	4.796e-03
Clock = 1 Data 100Mhz	1.389e-03	7.190e-04	4.958e-04	3.843e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.400	4.0800
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.0676	0.0362	3.5556	1.6601
CP to Q ↑	0.0547	0.0442	4.9655	2.3534
CP to TQ ↓	0.0645	0.0370	3.5382	4.1470
CP to TQ ↑	0.0559	0.0485	6.5548	8.9974
	X17_P4	X33_P4	X17_P4	X33_P4
CP to Q ↓	0.0500	0.0545	0.8278	0.4308
CP to Q ↑	0.0713	0.0752	1.1881	0.5965
CP to TQ ↓	0.0518	0.0569	4.0251	4.0922
CP to TQ ↑	0.0757	0.0814	8.7465	8.8544

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0747	0.0779	0.0779	0.0779
CP ↑	min_pulse_width to CP	0.0565	0.0269	0.0269	0.0269
D ↓	hold_rising to CP	-0.0496	-0.0169	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0185	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0852	0.0538	0.0538	0.0538
D ↑	setup_rising to CP	0.0432	0.0245	0.0245	0.0245
TE ↓	hold_rising to CP	-0.0337	-0.0147	-0.0169	-0.0143
TE ↑	hold_rising to CP	-0.0230	-0.0147	-0.0147	-0.0147
TE ↓	setup_rising to CP	0.0680	0.0516	0.0516	0.0516
TE ↑	setup_rising to CP	0.1269	0.1030	0.1030	0.1030
TI ↓	hold_rising to CP	-0.1036	-0.0592	-0.0635	-0.0635
TI ↑	hold_rising to CP	-0.0285	-0.0110	-0.0169	-0.0169
TI ↓	setup_rising to CP	0.1349	0.1030	0.1030	0.1030
TI ↑	setup_rising to CP	0.0575	0.0417	0.0417	0.0417

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	7.089e-06	1.000e-20
X8_P4	8.546e-06	1.000e-20
X17_P4	1.277e-05	1.000e-20
X33_P4	1.647e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

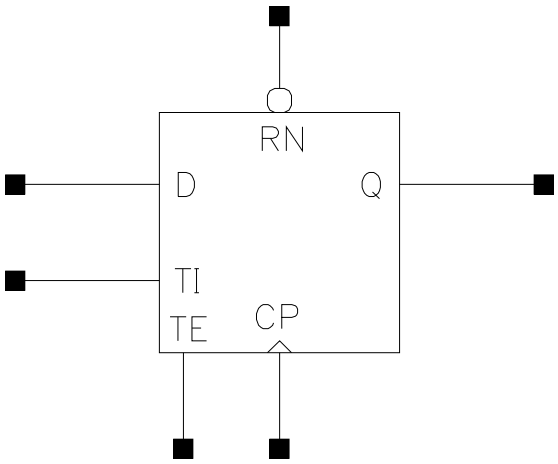
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	8.187e-03	8.307e-03	8.343e-03	8.361e-03
Clock 100Mhz Data 25Mhz	8.627e-03	8.592e-03	9.292e-03	1.011e-02
Clock 100Mhz Data 50Mhz	9.066e-03	8.877e-03	1.024e-02	1.186e-02
Clock = 0 Data 100Mhz	5.282e-03	4.945e-03	4.836e-03	4.781e-03
Clock = 1 Data 100Mhz	1.377e-03	7.134e-04	4.921e-04	3.815e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.672	4.4064
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
RN	0.0009	0.0007	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0618	0.0346	3.6194	1.6733
CP to Q ↑	0.0527	0.0448	4.9043	2.3704
RN to Q ↓	0.0539	0.0481	3.1956	1.7238
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0511	0.0558	0.8127	0.4285
CP to Q ↑	0.0650	0.0688	1.1568	0.5923
RN to Q ↓	0.0705	0.0752	0.8122	0.4280

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0818	0.0796	0.0819	0.0813
CP ↑	min_pulse_width to CP	0.0518	0.0269	0.0270	0.0270
D ↓	hold_rising to CP	-0.0457	-0.0093	-0.0093	-0.0093
D ↑	hold_rising to CP	-0.0240	-0.0017	-0.0049	-0.0049
D ↓	setup_rising to CP	0.0798	0.0516	0.0516	0.0516
D ↑	setup_rising to CP	0.0535	0.0294	0.0294	0.0294
RN ↓	min_pulse_width to RN	0.0540	0.0588	0.0544	0.0544
RN ↑	recovery_rising to CP	0.0147	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0099	-0.0051	-0.0055	-0.0055
TE ↓	hold_rising to CP	-0.0305	-0.0071	-0.0071	-0.0071
TE ↑	hold_rising to CP	-0.0337	-0.0196	-0.0191	-0.0191
TE ↓	setup_rising to CP	0.0684	0.0479	0.0538	0.0538
TE ↑	setup_rising to CP	0.1275	0.0982	0.0982	0.0982
TI ↓	hold_rising to CP	-0.0954	-0.0486	-0.0486	-0.0486
TI ↑	hold_rising to CP	-0.0374	-0.0217	-0.0215	-0.0215
TI ↓	setup_rising to CP	0.1333	0.0981	0.0981	0.0981
TI ↑	setup_rising to CP	0.0630	0.0472	0.0515	0.0515

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	7.441e-06	1.000e-20
X8_P4	8.841e-06	1.000e-20
X17_P4	1.295e-05	1.000e-20
X33_P4	1.738e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	9.102e-03	9.177e-03	9.243e-03	9.278e-03

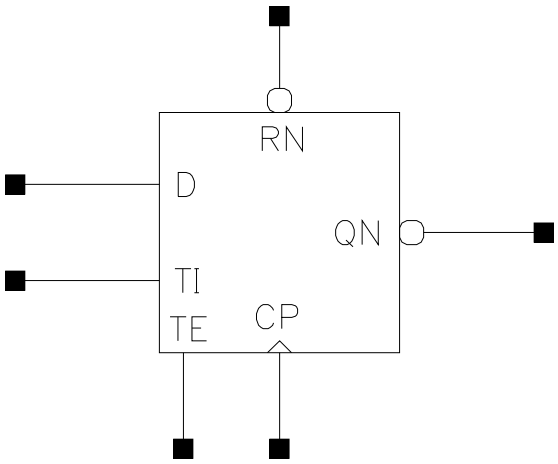
Clock 100Mhz Data 25Mhz	9.202e-03	9.165e-03	1.001e-02	1.082e-02
Clock 100Mhz Data 50Mhz	9.301e-03	9.152e-03	1.078e-02	1.237e-02
Clock = 0 Data 100Mhz	5.383e-03	4.963e-03	4.825e-03	4.757e-03
Clock = 1 Data 100Mhz	1.413e-03	7.330e-04	5.064e-04	3.932e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	3.944	4.7328
X33_P4	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0591	0.0550	3.0394	1.5801
CP to QN ↑	0.0638	0.0414	4.7631	2.2849
RN to QN ↑	0.0614	0.0622	4.7565	2.2786
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0546	0.0595	0.8132	0.4280
CP to QN ↑	0.0454	0.0500	1.1676	0.6000
RN to QN ↑	0.0637	0.0694	1.1719	0.6009

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0818	0.0796	0.0796	0.0796
CP ↑	min_pulse_width to CP	0.0410	0.0270	0.0269	0.0316
D ↓	hold_rising to CP	-0.0457	-0.0093	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0240	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0798	0.0516	0.0516	0.0516
D ↑	setup_rising to CP	0.0535	0.0294	0.0294	0.0294
RN ↓	min_pulse_width to RN	0.0540	0.0544	0.0659	0.0659
RN ↑	recovery_rising to CP	0.0151	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0099	-0.0077	-0.0051	-0.0051
TE ↓	hold_rising to CP	-0.0338	-0.0071	-0.0071	-0.0071
TE ↑	hold_rising to CP	-0.0337	-0.0191	-0.0191	-0.0191
TE ↓	setup_rising to CP	0.0680	0.0479	0.0479	0.0479
TE ↑	setup_rising to CP	0.1275	0.0982	0.0982	0.0982
TI ↓	hold_rising to CP	-0.0954	-0.0486	-0.0486	-0.0486
TI ↑	hold_rising to CP	-0.0374	-0.0217	-0.0217	-0.0217
TI ↓	setup_rising to CP	0.1333	0.0981	0.0981	0.0981
TI ↑	setup_rising to CP	0.0630	0.0472	0.0515	0.0515

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	7.435e-06	1.000e-20
X8_P4	8.240e-06	1.000e-20
X17_P4	1.227e-05	1.000e-20
X33_P4	1.521e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	9.027e-03	9.137e-03	9.173e-03	9.192e-03

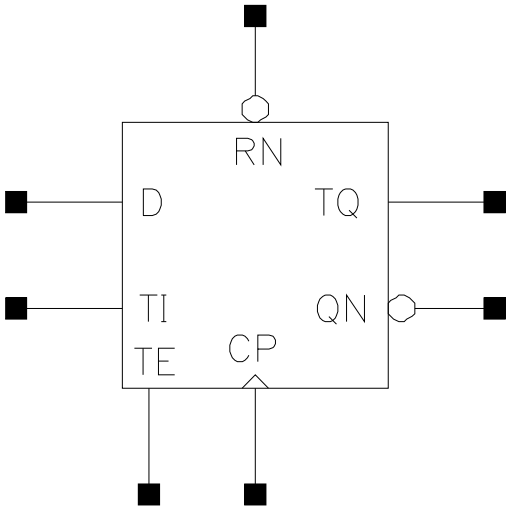
Clock 100Mhz Data 25Mhz	9.032e-03	9.152e-03	9.856e-03	1.065e-02
Clock 100Mhz Data 50Mhz	9.036e-03	9.167e-03	1.054e-02	1.210e-02
Clock = 0 Data 100Mhz	5.378e-03	4.958e-03	4.824e-03	4.757e-03
Clock = 1 Data 100Mhz	1.412e-03	7.323e-04	5.060e-04	3.929e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

RN	0.0010	0.0007	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0657	0.0571	3.0506	1.6694
CP to QN ↑	0.0818	0.0460	4.2654	2.3834
CP to TQ ↓	0.0586	0.0316	3.8345	3.1767
CP to TQ ↑	0.0544	0.0452	7.3382	6.8110
RN to QN ↑	0.0604	0.0605	4.2974	2.3770
RN to TQ ↓	0.0423	0.0419	3.5063	3.2984
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0589	0.0635	0.8288	0.4379
CP to QN ↑	0.0466	0.0493	1.1929	0.6029
CP to TQ ↓	0.0327	0.0338	3.9602	3.8739
CP to TQ ↑	0.0452	0.0462	6.3887	6.4797
RN to QN ↑	0.0627	0.0670	1.1911	0.6017
RN to TQ ↓	0.0446	0.0465	4.0805	4.0145

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0818	0.0796	0.0813	0.0813
CP ↑	min_pulse_width to CP	0.0551	0.0269	0.0269	0.0269
D ↓	hold_rising to CP	-0.0457	-0.0093	-0.0093	-0.0093
D ↑	hold_rising to CP	-0.0240	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0798	0.0516	0.0516	0.0516
D ↑	setup_rising to CP	0.0535	0.0294	0.0294	0.0294
RN ↓	min_pulse_width to RN	0.0588	0.0588	0.0610	0.0659
RN ↑	recovery_rising to CP	0.0173	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0125	-0.0051	-0.0051	-0.0051
TE ↓	hold_rising to CP	-0.0305	-0.0071	-0.0071	-0.0071
TE ↑	hold_rising to CP	-0.0337	-0.0191	-0.0191	-0.0191
TE ↓	setup_rising to CP	0.0680	0.0479	0.0538	0.0505
TE ↑	setup_rising to CP	0.1275	0.0982	0.0982	0.0982
TI ↓	hold_rising to CP	-0.0954	-0.0486	-0.0486	-0.0486
TI ↑	hold_rising to CP	-0.0374	-0.0217	-0.0217	-0.0217
TI ↓	setup_rising to CP	0.1333	0.0981	0.0981	0.0981
TI ↑	setup_rising to CP	0.0630	0.0472	0.0515	0.0515

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	8.317e-06	1.000e-20
X8_P4	8.717e-06	1.000e-20
X17_P4	1.088e-05	1.000e-20
X33_P4	1.458e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

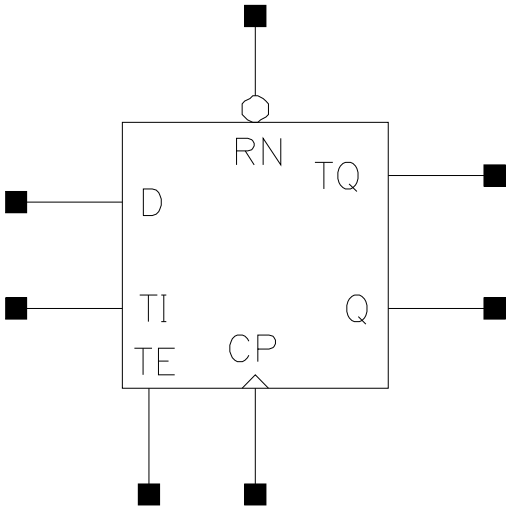
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	9.028e-03	9.134e-03	9.215e-03	9.257e-03
Clock 100Mhz Data 25Mhz	9.311e-03	9.331e-03	9.772e-03	1.071e-02
Clock 100Mhz Data 50Mhz	9.595e-03	9.528e-03	1.033e-02	1.217e-02
Clock = 0 Data 100Mhz	5.378e-03	4.959e-03	4.818e-03	4.748e-03
Clock = 1 Data 100Mhz	1.411e-03	7.321e-04	5.058e-04	3.927e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

RN	0.0009	0.0009	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0694	0.0374	3.8183	1.7201
CP to Q ↑	0.0562	0.0467	5.0984	2.4643
CP to TQ ↓	0.0656	0.0370	4.7693	4.1846
CP to TQ ↑	0.0580	0.0492	9.8721	8.9748
RN to Q ↓	0.0556	0.0543	3.3468	1.7756
RN to TQ ↓	0.0544	0.0526	4.2518	4.3133
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0525	0.0576	0.8226	0.4338
CP to Q ↑	0.0654	0.0695	1.1613	0.5941
CP to TQ ↓	0.0543	0.0608	4.0464	4.1149
CP to TQ ↑	0.0695	0.0760	8.8640	8.9106
RN to Q ↓	0.0719	0.0769	0.8233	0.4339
RN to TQ ↓	0.0736	0.0801	4.0421	4.1115

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0818	0.0796	0.0796	0.0796
CP ↑	min_pulse_width to CP	0.0599	0.0316	0.0270	0.0270
D ↓	hold_rising to CP	-0.0457	-0.0094	-0.0093	-0.0093
D ↑	hold_rising to CP	-0.0240	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0798	0.0516	0.0516	0.0516
D ↑	setup_rising to CP	0.0535	0.0294	0.0294	0.0294
RN ↓	min_pulse_width to RN	0.0588	0.0686	0.0544	0.0544
RN ↑	recovery_rising to CP	0.0151	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0104	-0.0051	-0.0051	-0.0051
TE ↓	hold_rising to CP	-0.0305	-0.0071	-0.0071	-0.0071
TE ↑	hold_rising to CP	-0.0337	-0.0196	-0.0191	-0.0191
TE ↓	setup_rising to CP	0.0684	0.0479	0.0479	0.0479
TE ↑	setup_rising to CP	0.1275	0.0982	0.0982	0.0982
TI ↓	hold_rising to CP	-0.0954	-0.0488	-0.0486	-0.0486
TI ↑	hold_rising to CP	-0.0374	-0.0217	-0.0217	-0.0217
TI ↓	setup_rising to CP	0.1333	0.0981	0.0981	0.0981
TI ↑	setup_rising to CP	0.0630	0.0472	0.0472	0.0472

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	7.670e-06	1.000e-20
X8_P4	9.164e-06	1.000e-20
X17_P4	1.308e-05	1.000e-20
X33_P4	1.751e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

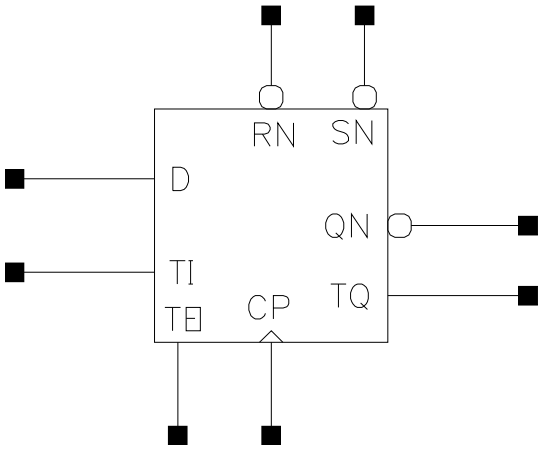
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	9.086e-03	9.165e-03	9.190e-03	9.204e-03
Clock 100Mhz Data 25Mhz	9.399e-03	9.335e-03	1.013e-02	1.099e-02
Clock 100Mhz Data 50Mhz	9.711e-03	9.506e-03	1.107e-02	1.278e-02
Clock = 0 Data 100Mhz	5.381e-03	4.961e-03	4.821e-03	4.752e-03
Clock = 1 Data 100Mhz	1.413e-03	7.331e-04	5.065e-04	3.932e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.352	5.2224
X17_P4	1.200	4.488	5.3856
X33_P4	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0008	0.0008	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0633	0.0672	1.6142	0.8313
CP to QN ↑	0.0474	0.0497	2.2991	1.1664
CP to TQ ↓	0.0365	0.0365	4.9965	5.0023
CP to TQ ↑	0.0526	0.0525	11.4682	11.4937
RN to QN ↓	0.0684	0.0723	1.6139	0.8314
RN to QN ↑	0.0669	0.0703	2.3029	1.1686
RN to TQ ↓	0.0518	0.0515	5.3028	5.3028
RN to TQ ↑	0.0581	0.0580	11.4428	11.4632
SN to QN ↓	0.0727	0.0773	1.6203	0.8331
SN to TQ ↑	0.0605	0.0604	11.5998	11.6194
	X33_P4		**X33_P4**	
CP to QN ↓	0.0767		0.4408	
CP to QN ↑	0.0555		0.5996	
CP to TQ ↓	0.0365		5.0120	
CP to TQ ↑	0.0527		11.5136	
RN to QN ↓	0.0815		0.4409	
RN to QN ↑	0.0777		0.5998	
RN to TQ ↓	0.0515		5.3180	
RN to TQ ↑	0.0582		11.4858	
SN to QN ↓	0.0879		0.4412	
SN to TQ ↑	0.0604		11.6568	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0843	0.0843	0.0843
CP ↑	min_pulse_width to CP	0.0268	0.0316	0.0316
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0565	0.0565	0.0565
D ↑	setup_rising to CP	0.0320	0.0320	0.0320
RN ↓	min_pulse_width to RN	0.0659	0.0659	0.0708
RN ↑	non_seq_hold_rising to SN	-0.0237	-0.0237	-0.0237
RN ↑	non_seq_setup_rising to SN	0.0573	0.0573	0.0573
RN ↑	recovery_rising to CP	0.0222	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0152	-0.0152	-0.0152
SN ↓	min_pulse_width to SN	0.0549	0.0549	0.0576
SN ↑	recovery_rising to CP	0.0054	0.0054	0.0054
SN ↑	removal_rising to CP	0.0260	0.0260	0.0260

TE ↓	hold_rising to CP	-0.0071	-0.0071	-0.0071
TE ↑	hold_rising to CP	-0.0196	-0.0191	-0.0196
TE ↓	setup_rising to CP	0.0538	0.0538	0.0538
TE ↑	setup_rising to CP	0.1030	0.1030	0.1030
TI ↓	hold_rising to CP	-0.0501	-0.0501	-0.0501
TI ↑	hold_rising to CP	-0.0217	-0.0217	-0.0217
TI ↓	setup_rising to CP	0.1030	0.1030	0.1030
TI ↑	setup_rising to CP	0.0515	0.0515	0.0515

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	9.698e-06	1.000e-20
X17_P4	1.144e-05	1.000e-20
X33_P4	1.470e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

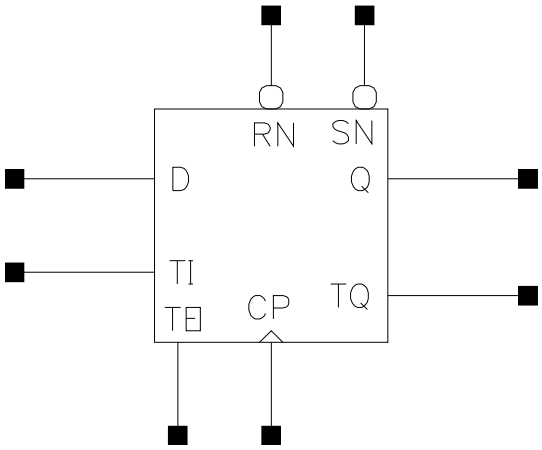
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	9.703e-03	9.703e-03	9.704e-03
Clock 100Mhz Data 25Mhz	9.798e-03	1.018e-02	1.121e-02
Clock 100Mhz Data 50Mhz	9.893e-03	1.065e-02	1.271e-02
Clock = 0 Data 100Mhz	4.715e-03	4.715e-03	4.716e-03
Clock = 1 Data 100Mhz	5.386e-05	5.397e-05	5.403e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.216	5.0592
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0008	0.0008	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0407	0.0454	1.6656	0.8635
CP to Q ↑	0.0513	0.0543	2.3645	1.2065
CP to TQ ↓	0.0411	0.0461	5.0737	5.1335
CP to TQ ↑	0.0564	0.0620	11.2450	11.3360
RN to Q ↓	0.0612	0.0708	1.8384	0.9561
RN to Q ↑	0.0462	0.0526	2.4464	1.2524
RN to TQ ↓	0.0602	0.0694	5.4228	5.5372
RN to TQ ↑	0.0541	0.0647	11.3603	11.4490
SN to Q ↑	0.0610	0.0671	2.4492	1.2534
SN to TQ ↑	0.0688	0.0791	11.3620	11.4566
	X33_P4		**X33_P4**	
CP to Q ↓	0.0571		0.4637	
CP to Q ↑	0.0620		0.6285	
CP to TQ ↓	0.0550		5.3092	
CP to TQ ↑	0.0723		11.4855	
RN to Q ↓	0.0931		0.5193	
RN to Q ↑	0.0678		0.6577	
RN to TQ ↓	0.0858		5.8367	
RN to TQ ↑	0.0848		11.6129	
SN to Q ↑	0.0820		0.6578	
SN to TQ ↑	0.0990		11.6156	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0843	0.0843	0.0843
CP ↑	min_pulse_width to CP	0.0316	0.0363	0.0470
D ↓	hold_rising to CP	-0.0126	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0565	0.0565	0.0565
D ↑	setup_rising to CP	0.0320	0.0320	0.0320
RN ↓	min_pulse_width to RN	0.0735	0.0854	0.1099
RN ↑	non_seq_hold_rising to SN	-0.0260	-0.0336	-0.0434
RN ↑	non_seq_setup_rising to SN	0.0523	0.0546	0.0721
RN ↑	recovery_rising to CP	0.0200	0.0200	0.0200
RN ↑	removal_rising to CP	-0.0099	-0.0099	-0.0099
SN ↓	min_pulse_width to SN	0.0576	0.0674	0.0869
SN ↑	recovery_rising to CP	0.0054	0.0054	0.0054
SN ↑	removal_rising to CP	0.0260	0.0260	0.0260

TE ↓	hold_rising to CP	-0.0071	-0.0071	-0.0071
TE ↑	hold_rising to CP	-0.0196	-0.0196	-0.0196
TE ↓	setup_rising to CP	0.0538	0.0538	0.0538
TE ↑	setup_rising to CP	0.1030	0.1030	0.1030
TI ↓	hold_rising to CP	-0.0501	-0.0486	-0.0486
TI ↑	hold_rising to CP	-0.0217	-0.0217	-0.0217
TI ↓	setup_rising to CP	0.1030	0.1030	0.1030
TI ↑	setup_rising to CP	0.0515	0.0515	0.0515

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P4	1.006e-05	1.000e-20
X17_P4	1.222e-05	1.000e-20
X33_P4	1.638e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

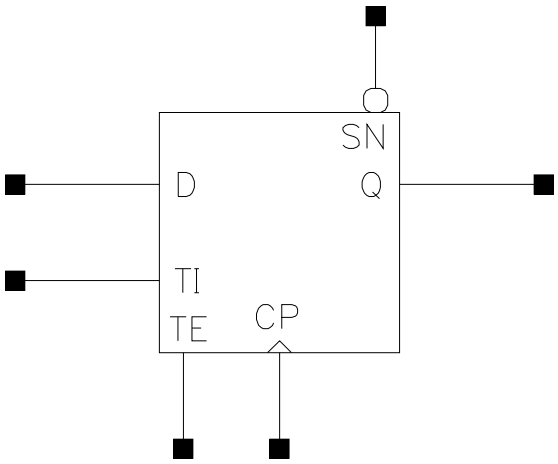
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	9.684e-03	9.686e-03	9.688e-03
Clock 100Mhz Data 25Mhz	9.720e-03	1.022e-02	1.159e-02
Clock 100Mhz Data 50Mhz	9.756e-03	1.076e-02	1.350e-02
Clock = 0 Data 100Mhz	4.713e-03	4.713e-03	4.713e-03
Clock = 1 Data 100Mhz	5.352e-05	5.358e-05	5.370e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0015	0.0014	0.0013	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0009			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.0620	0.0358	3.6290	1.6563
CP to Q ↑	0.0549	0.0471	4.9512	2.3532
SN to Q ↑	0.0421	0.0480	4.8221	2.3495
	X17_P4	X25_P4	X17_P4	X25_P4
CP to Q ↓	0.0503	0.0530	0.8134	0.5643
CP to Q ↑	0.0655	0.0676	1.1563	0.7863
SN to Q ↑	0.0658	0.0680	1.1552	0.7874
	X33_P4		X33_P4	
CP to Q ↓	0.0549		0.4291	
CP to Q ↑	0.0691		0.5919	
SN to Q ↑	0.0694		0.5922	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.0859	0.0849	0.0842	0.0849
CP ↑	min_pulse_width to CP	0.0518	0.0270	0.0271	0.0271
D ↓	hold_rising to CP	-0.0448	-0.0120	-0.0116	-0.0116
D ↑	hold_rising to CP	-0.0240	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0852	0.0565	0.0565	0.0565
D ↑	setup_rising to CP	0.0481	0.0266	0.0266	0.0266
SN ↓	min_pulse_width to SN	0.0403	0.0452	0.0425	0.0425
SN ↑	recovery_rising to CP	0.0048	0.0054	0.0054	0.0054
SN ↑	removal_rising to CP	0.0221	0.0265	0.0265	0.0265
TE ↓	hold_rising to CP	-0.0338	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0279	-0.0142	-0.0163	-0.0163
TE ↓	setup_rising to CP	0.0701	0.0508	0.0508	0.0508
TE ↑	setup_rising to CP	0.1297	0.1079	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0944	-0.0534	-0.0550	-0.0550
TI ↑	hold_rising to CP	-0.0334	-0.0166	-0.0159	-0.0159
TI ↓	setup_rising to CP	0.1341	0.1027	0.1027	0.1027
TI ↑	setup_rising to CP	0.0640	0.0466	0.0466	0.0466
		X33_P4			

CP ↓	min_pulse_width to CP	0.0842			
CP ↑	min_pulse_width to CP	0.0271			
D ↓	hold_rising to CP	-0.0116			
D ↑	hold_rising to CP	0.0004			
D ↓	setup_rising to CP	0.0565			
D ↑	setup_rising to CP	0.0266			
SN ↓	min_pulse_width to SN	0.0425			
SN ↑	recovery_rising to CP	0.0054			
SN ↑	removal_rising to CP	0.0265			
TE ↓	hold_rising to CP	-0.0120			
TE ↑	hold_rising to CP	-0.0163			
TE ↓	setup_rising to CP	0.0508			
TE ↑	setup_rising to CP	0.1079			
TI ↓	hold_rising to CP	-0.0550			
TI ↑	hold_rising to CP	-0.0159			
TI ↓	setup_rising to CP	0.1027			
TI ↑	setup_rising to CP	0.0466			

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	7.048e-06	1.000e-20
X8_P4	8.588e-06	1.000e-20
X17_P4	1.254e-05	1.000e-20
X25_P4	1.402e-05	1.000e-20
X33_P4	1.549e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	8.845e-03	9.085e-03	9.166e-03	9.207e-03
Clock 100Mhz Data 25Mhz	8.992e-03	9.166e-03	9.937e-03	1.038e-02
Clock 100Mhz Data 50Mhz	9.138e-03	9.246e-03	1.071e-02	1.155e-02
Clock = 0 Data 100Mhz	5.166e-03	4.870e-03	4.771e-03	4.722e-03
Clock = 1 Data 100Mhz	1.412e-03	7.326e-04	5.061e-04	3.929e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	9.231e-03			

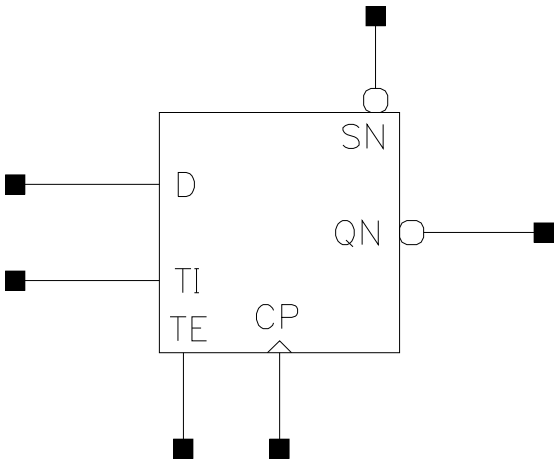
Clock 100Mhz Data 25Mhz	1.076e-02			
Clock 100Mhz Data 50Mhz	1.229e-02			
Clock = 0 Data 100Mhz	4.692e-03			
Clock = 1 Data 100Mhz	3.250e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0015	0.0014	0.0014	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0009			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.0615	0.0556	3.0432	1.5831
CP to QN ↑	0.0643	0.0411	4.7527	2.2932
SN to QN ↓	0.0496	0.0559	3.0321	1.5831
	X17_P4	X25_P4	X17_P4	X25_P4
CP to QN ↓	0.0582	0.0613	0.8164	0.5666
CP to QN ↑	0.0480	0.0508	1.1573	0.7879
SN to QN ↓	0.0596	0.0628	0.8162	0.5660
	X33_P4		X33_P4	
CP to QN ↓	0.0638		0.4301	
CP to QN ↑	0.0529		0.5928	
SN to QN ↓	0.0652		0.4300	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.0859	0.0849	0.0849	0.0849
CP ↑	min_pulse_width to CP	0.0411	0.0270	0.0283	0.0317
D ↓	hold_rising to CP	-0.0448	-0.0116	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0240	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0852	0.0565	0.0565	0.0565
D ↑	setup_rising to CP	0.0481	0.0266	0.0266	0.0266
SN ↓	min_pulse_width to SN	0.0376	0.0425	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0054	0.0054	0.0054	0.0054
SN ↑	removal_rising to CP	0.0221	0.0265	0.0265	0.0265
TE ↓	hold_rising to CP	-0.0338	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0279	-0.0163	-0.0142	-0.0142
TE ↓	setup_rising to CP	0.0701	0.0508	0.0540	0.0540
TE ↑	setup_rising to CP	0.1297	0.1079	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0944	-0.0550	-0.0534	-0.0534
TI ↑	hold_rising to CP	-0.0334	-0.0166	-0.0166	-0.0166
TI ↓	setup_rising to CP	0.1341	0.1027	0.1027	0.1027
TI ↑	setup_rising to CP	0.0640	0.0466	0.0466	0.0466
		X33_P4			

CP ↓	min_pulse_width to CP	0.0849			
CP ↑	min_pulse_width to CP	0.0316			
D ↓	hold_rising to CP	-0.0120			
D ↑	hold_rising to CP	0.0004			
D ↓	setup_rising to CP	0.0565			
D ↑	setup_rising to CP	0.0266			
SN ↓	min_pulse_width to SN	0.0474			
SN ↑	recovery_rising to CP	0.0054			
SN ↑	removal_rising to CP	0.0265			
TE ↓	hold_rising to CP	-0.0120			
TE ↑	hold_rising to CP	-0.0142			
TE ↓	setup_rising to CP	0.0540			
TE ↑	setup_rising to CP	0.1079			
TI ↓	hold_rising to CP	-0.0534			
TI ↑	hold_rising to CP	-0.0166			
TI ↓	setup_rising to CP	0.1027			
TI ↑	setup_rising to CP	0.0466			

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	7.163e-06	1.000e-20
X8_P4	9.226e-06	1.000e-20
X17_P4	1.325e-05	1.000e-20
X25_P4	1.546e-05	1.000e-20
X33_P4	1.768e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	8.850e-03	9.102e-03	9.178e-03	9.216e-03
Clock 100Mhz Data 25Mhz	8.849e-03	9.111e-03	9.978e-03	1.042e-02
Clock 100Mhz Data 50Mhz	8.847e-03	9.120e-03	1.078e-02	1.162e-02
Clock = 0 Data 100Mhz	5.167e-03	4.872e-03	4.773e-03	4.724e-03
Clock = 1 Data 100Mhz	1.413e-03	7.329e-04	5.063e-04	3.931e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	9.239e-03			

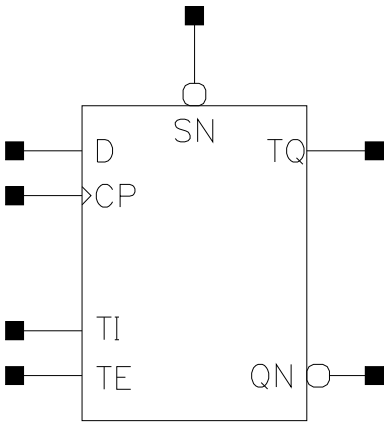
Clock 100Mhz Data 25Mhz	1.082e-02			
Clock 100Mhz Data 50Mhz	1.240e-02			
Clock = 0 Data 100Mhz	4.694e-03			
Clock = 1 Data 100Mhz	3.251e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.216	5.0592
X8_P4	1.200	4.080	4.8960
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0016	0.0016	0.0016
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0703	0.0582	3.0431	1.5914
CP to QN ↑	0.0819	0.0462	4.6926	2.3464
CP to TQ ↓	0.0595	0.0320	4.3178	3.7002
CP to TQ ↑	0.0545	0.0444	6.5357	6.3465
SN to QN ↓	0.0472	0.0450	3.0381	1.5925
SN to TQ ↑	0.0333	0.0325	6.4188	6.3229
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0578	0.0638	0.8413	0.4256
CP to QN ↑	0.0511	0.0567	1.1717	0.5990
CP to TQ ↓	0.0390	0.0389	3.8281	3.8384
CP to TQ ↑	0.0495	0.0495	6.4202	6.4379
SN to QN ↓	0.0434	0.0557	0.8396	0.4252
SN to TQ ↑	0.0412	0.0412	6.4098	6.4323

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0859	0.0849	0.0867	0.0849
CP ↑	min_pulse_width to CP	0.0552	0.0270	0.0316	0.0329
D ↓	hold_rising to CP	-0.0448	-0.0116	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0240	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0852	0.0565	0.0565	0.0565
D ↑	setup_rising to CP	0.0481	0.0266	0.0266	0.0266
SN ↓	min_pulse_width to SN	0.0354	0.0376	0.0381	0.0381
SN ↑	recovery_rising to CP	0.0048	0.0054	0.0054	0.0054
SN ↑	removal_rising to CP	0.0221	0.0265	0.0265	0.0265
TE ↓	hold_rising to CP	-0.0338	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0279	-0.0142	-0.0142	-0.0142
TE ↓	setup_rising to CP	0.0701	0.0540	0.0540	0.0540
TE ↑	setup_rising to CP	0.1297	0.1079	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0944	-0.0550	-0.0550	-0.0534
TI ↑	hold_rising to CP	-0.0334	-0.0166	-0.0166	-0.0166
TI ↓	setup_rising to CP	0.1341	0.1027	0.1043	0.1027
TI ↑	setup_rising to CP	0.0640	0.0466	0.0466	0.0466

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	8.172e-06	1.000e-20
X8_P4	1.021e-05	1.000e-20
X17_P4	1.424e-05	1.000e-20
X33_P4	1.866e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

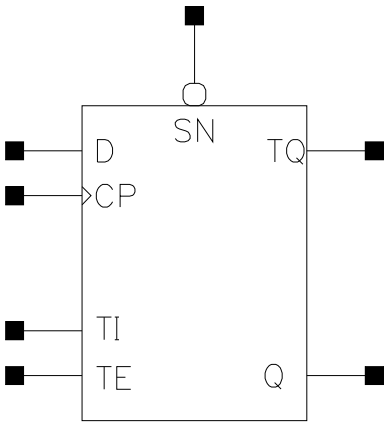
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	8.854e-03	9.099e-03	9.180e-03	9.222e-03
Clock 100Mhz Data 25Mhz	9.221e-03	9.367e-03	1.015e-02	1.101e-02
Clock 100Mhz Data 50Mhz	9.587e-03	9.636e-03	1.111e-02	1.280e-02
Clock = 0 Data 100Mhz	5.179e-03	4.881e-03	4.782e-03	4.732e-03
Clock = 1 Data 100Mhz	1.413e-03	7.330e-04	5.064e-04	3.932e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.944	4.7328
X17_P4	1.200	4.216	5.0592
X33_P4	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0014	0.0014	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0704	0.0385	3.7094	1.6923
CP to Q ↑	0.0582	0.0489	4.9627	2.3846
CP to TQ ↓	0.0699	0.0393	5.3849	4.2004
CP to TQ ↑	0.0572	0.0537	6.5904	9.0509
SN to Q ↑	0.0355	0.0502	4.8285	2.3840
SN to TQ ↑	0.0348	0.0557	6.4389	9.0322
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0514	0.0562	0.8353	0.4367
CP to Q ↑	0.0663	0.0701	1.1627	0.5948
CP to TQ ↓	0.0531	0.0593	4.0446	4.1084
CP to TQ ↑	0.0705	0.0767	8.8680	8.9205
SN to Q ↑	0.0666	0.0704	1.1634	0.5956
SN to TQ ↑	0.0708	0.0771	8.8680	8.9232

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0859	0.0849	0.0849	0.0849
CP ↑	min_pulse_width to CP	0.0611	0.0317	0.0271	0.0271
D ↓	hold_rising to CP	-0.0448	-0.0120	-0.0116	-0.0116
D ↑	hold_rising to CP	-0.0240	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0852	0.0565	0.0565	0.0565
D ↑	setup_rising to CP	0.0481	0.0266	0.0266	0.0266
SN ↓	min_pulse_width to SN	0.0354	0.0474	0.0425	0.0425
SN ↑	recovery_rising to CP	0.0048	0.0054	0.0054	0.0054
SN ↑	removal_rising to CP	0.0221	0.0265	0.0265	0.0265
TE ↓	hold_rising to CP	-0.0338	-0.0094	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0279	-0.0142	-0.0163	-0.0163
TE ↓	setup_rising to CP	0.0733	0.0508	0.0508	0.0508
TE ↑	setup_rising to CP	0.1297	0.1079	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0944	-0.0534	-0.0550	-0.0550
TI ↑	hold_rising to CP	-0.0334	-0.0166	-0.0159	-0.0159
TI ↓	setup_rising to CP	0.1341	0.1027	0.1027	0.1027
TI ↑	setup_rising to CP	0.0640	0.0466	0.0466	0.0466

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	7.886e-06	1.000e-20
X8_P4	8.863e-06	1.000e-20
X17_P4	1.277e-05	1.000e-20
X33_P4	1.571e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

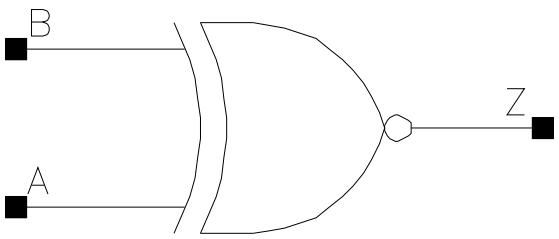
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	8.847e-03	9.090e-03	9.170e-03	9.210e-03
Clock 100Mhz Data 25Mhz	9.248e-03	9.374e-03	1.013e-02	1.101e-02
Clock 100Mhz Data 50Mhz	9.650e-03	9.659e-03	1.110e-02	1.281e-02
Clock = 0 Data 100Mhz	5.178e-03	4.875e-03	4.775e-03	4.725e-03
Clock = 1 Data 100Mhz	1.414e-03	7.334e-04	5.067e-04	3.934e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P4	X8_P4	X17_P4	X25_P4
A	0.0016	0.0007	0.0009	0.0015
B	0.0015	0.0014	0.0018	0.0025
	X33_P4			
A	0.0017			
B	0.0029			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X8_P4**	**X6_P4**	**X8_P4**
A to Z ↓	0.0177	0.0386	2.9486	1.7139
A to Z ↑	0.0181	0.0351	3.6344	2.4356
B to Z ↓	0.0166	0.0269	2.9473	1.6998
B to Z ↑	0.0186	0.0253	3.6433	2.4226
	X17_P4	**X25_P4**	**X17_P4**	**X25_P4**
A to Z ↓	0.0367	0.0371	0.8428	0.5815
A to Z ↑	0.0324	0.0326	1.1928	0.7936

B to Z ↓	0.0278	0.0269	0.8397	0.5797
B to Z ↑	0.0254	0.0246	1.1900	0.7916
	X33_P4		**X33_P4**	
A to Z ↓	0.0351		0.4358	
A to Z ↑	0.0317		0.5974	
B to Z ↓	0.0259		0.4347	
B to Z ↑	0.0244		0.5959	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P4	5.773e-06	1.000e-20
X8_P4	5.877e-06	1.000e-20
X17_P4	1.091e-05	1.000e-20
X25_P4	1.638e-05	1.000e-20
X33_P4	2.397e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	2.810e-03	5.232e-03	7.632e-03	1.207e-02
B to Z	2.739e-03	3.683e-03	5.898e-03	9.130e-03
	X33_P4			
A to Z	1.481e-02			
B to Z	1.158e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

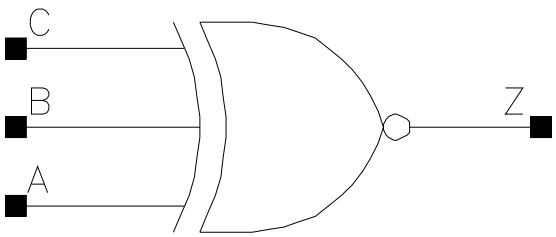
Pin Cycle (vdds)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P4			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	2.176	2.6112
X16_P4	1.200	2.720	3.2640
X25_P4	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X16_P4	X25_P4
A	0.0028	0.0023	0.0029	0.0043
B	0.0031	0.0021	0.0029	0.0039
C	0.0020	0.0007	0.0007	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0271	0.0441	3.4706	1.8111
A to Z ↑	0.0258	0.0408	5.1593	2.4069
B to Z ↓	0.0278	0.0444	3.4750	1.8107
B to Z ↑	0.0260	0.0412	5.1611	2.4075
C to Z ↓	0.0275	0.0583	3.4814	1.8086
C to Z ↑	0.0253	0.0546	5.1644	2.4062
	X16_P4	**X25_P4**	**X16_P4**	**X25_P4**
A to Z ↓	0.0444	0.0449	0.9295	0.5951
A to Z ↑	0.0442	0.0439	1.2643	0.7965
B to Z ↓	0.0449	0.0459	0.9293	0.5952

B to Z ↑	0.0445	0.0451	1.2650	0.7972
C to Z ↓	0.0618	0.0661	0.9289	0.5949
C to Z ↑	0.0607	0.0649	1.2644	0.7968

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	5.476e-06	1.000e-20
X8_P4	5.218e-06	1.000e-20
X16_P4	9.687e-06	1.000e-20
X25_P4	1.386e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	2.962e-03	4.073e-03	6.719e-03	1.026e-02
B to Z	2.913e-03	4.009e-03	6.675e-03	1.026e-02
C to Z	2.836e-03	6.077e-03	9.141e-03	1.387e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

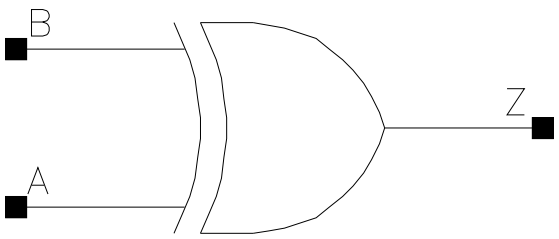
Pin Cycle (vdds)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.224	1.4688
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.224	1.4688
X16_P4	1.200	1.360	1.6320
X25_P4	1.200	2.176	2.6112
X31_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X16_P4
A	0.0008	0.0015	0.0010	0.0011
B	0.0012	0.0014	0.0015	0.0016
	X25_P4	X31_P4		
A	0.0014	0.0019		
B	0.0025	0.0033		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0346	0.0172	3.0865	2.2797
A to Z ↑	0.0330	0.0189	4.6623	4.5762
B to Z ↓	0.0250	0.0178	3.0730	2.2948
B to Z ↑	0.0251	0.0176	4.6565	4.5761
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0312	0.0327	1.6777	0.8677

A to Z ↑	0.0286	0.0303	2.3606	1.1939
B to Z ↓	0.0243	0.0254	1.6730	0.8656
B to Z ↑	0.0230	0.0245	2.3589	1.1923
	X25_P4	**X31_P4**	**X25_P4**	**X31_P4**
A to Z ↓	0.0347	0.0326	0.5770	0.4624
A to Z ↑	0.0317	0.0303	0.7926	0.6405
B to Z ↓	0.0264	0.0246	0.5769	0.4619
B to Z ↑	0.0242	0.0232	0.7916	0.6403

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	4.493e-06	1.000e-20
X6_P4	5.273e-06	1.000e-20
X8_P4	7.912e-06	1.000e-20
X16_P4	1.301e-05	1.000e-20
X25_P4	1.644e-05	1.000e-20
X31_P4	2.431e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	3.903e-03	2.769e-03	4.804e-03	7.111e-03
B to Z	3.050e-03	2.643e-03	4.015e-03	6.004e-03
	X25_P4	X31_P4		
A to Z	1.116e-02	1.369e-02		
B to Z	8.317e-03	1.021e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

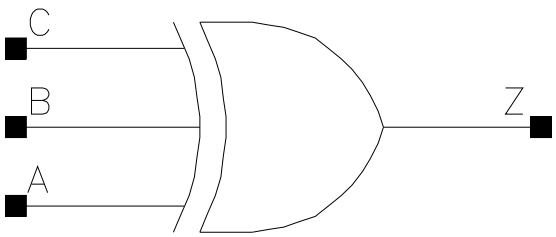
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P4	X31_P4		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X24_P4	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X24_P4
A	0.0024	0.0023	0.0029	0.0052
B	0.0024	0.0022	0.0027	0.0043
C	0.0008	0.0016	0.0022	0.0033

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0276	0.0441	3.6576	1.8106
A to Z ↑	0.0261	0.0408	5.6570	2.4045
B to Z ↓	0.0279	0.0444	3.6628	1.8104
B to Z ↑	0.0265	0.0412	5.6563	2.4049
C to Z ↓	0.0468	0.0434	3.6336	1.8109
C to Z ↑	0.0456	0.0400	5.6259	2.4043
	X17_P4	**X24_P4**	**X17_P4**	**X24_P4**
A to Z ↓	0.0406	0.0474	0.8660	0.6228
A to Z ↑	0.0405	0.0367	1.1722	0.8000
B to Z ↓	0.0409	0.0477	0.8662	0.6226

B to Z ↑	0.0408	0.0369	1.1728	0.7997
C to Z ↓	0.0404	0.0465	0.8660	0.6224
C to Z ↑	0.0403	0.0367	1.1720	0.8001

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	5.823e-06	1.000e-20
X8_P4	4.452e-06	1.000e-20
X17_P4	9.479e-06	1.000e-20
X24_P4	1.431e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	2.800e-03	4.075e-03	6.464e-03	1.097e-02
B to Z	2.797e-03	4.006e-03	6.402e-03	1.083e-02
C to Z	5.556e-03	3.908e-03	6.346e-03	1.064e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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