Layout Finishing and SoC Tiling: **BE tiling**

December 11th, 2012

CMOS and derivative PDK

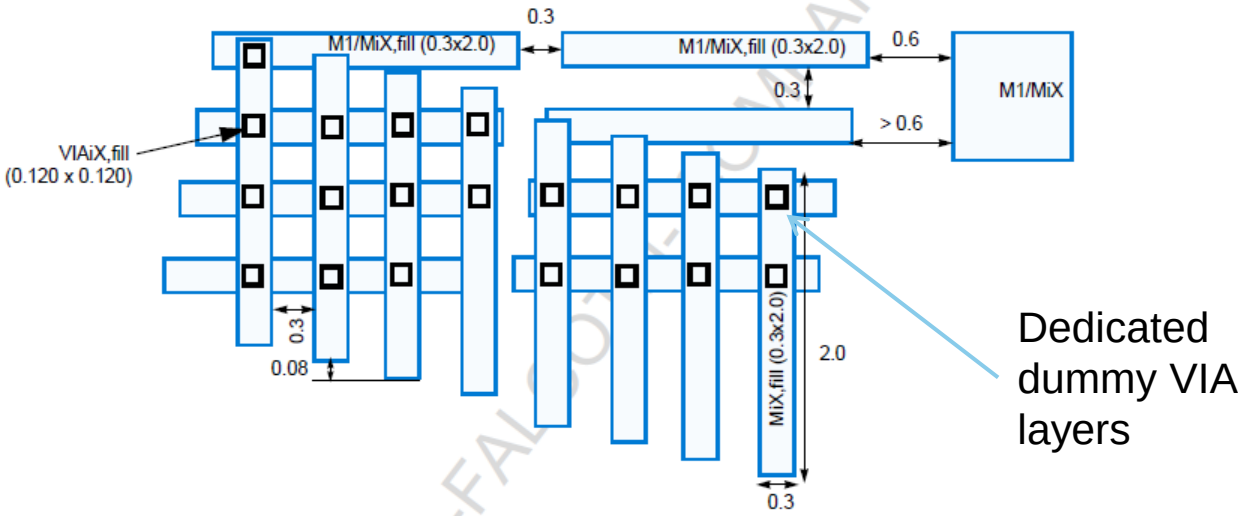
life.augmented

Program Management & Services / Process Design Kit

VIA-Tiling Implementation

Metal Via-Tiling has been added in several technologies (H9A, 55/65nm, 40/45nm, 28/32nm) in order to reinforce the Flip Chip / Bumping pads robustness and so IC/circuit package-qualification.

- Via;fill are added only in the (ultra)low-K metals (M1/Mx : thin metals)
- The density on a common layer level rises from 20% to 43%
  - it brought concerns regarding impact on electrical performances, but it seems spaces are big enough : no negative feedback since 2010
  - metal fill uniformity appears to be also important : via matrix only would have lower mechanical resistance (metal stripes are required)

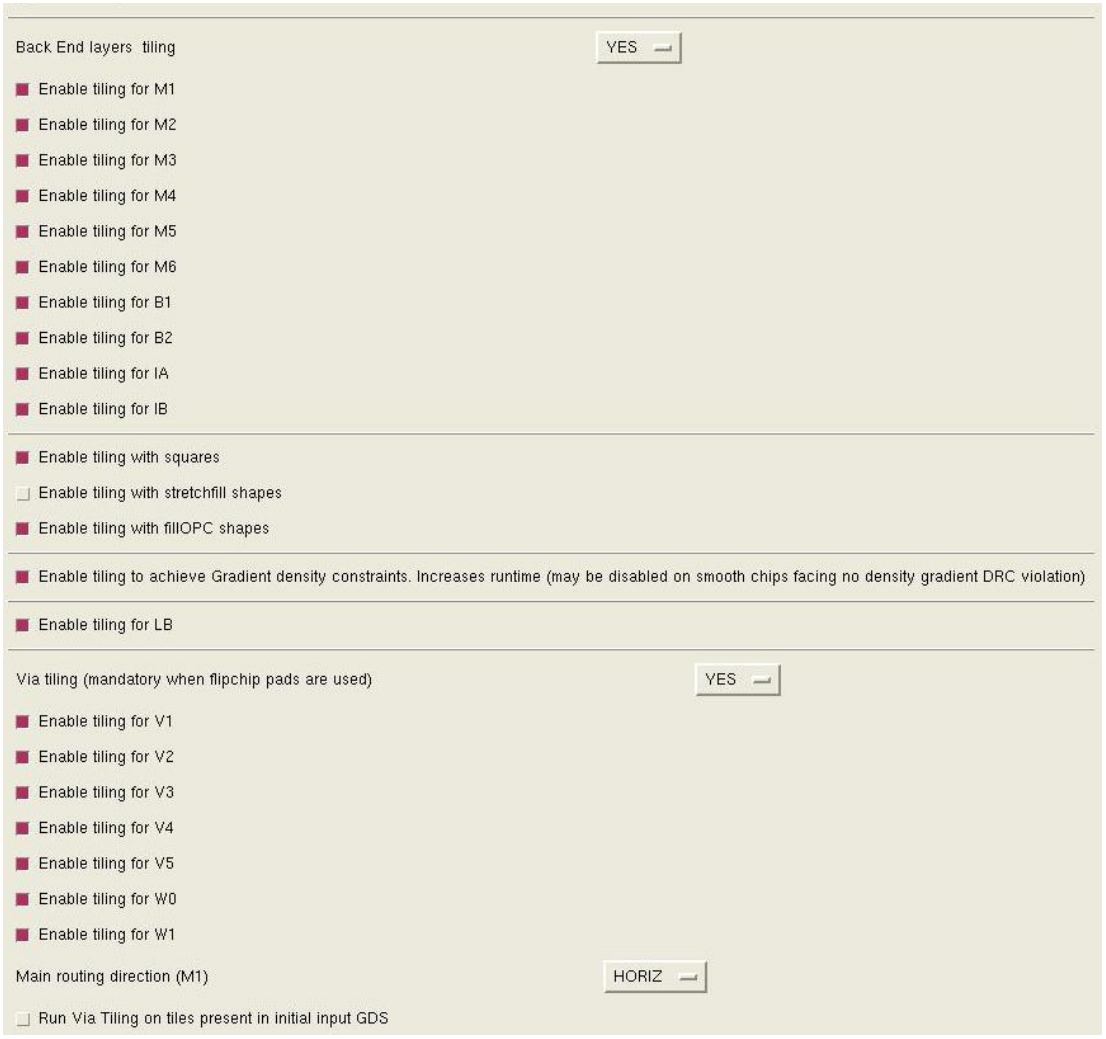


BE tiler passes

• Please refer to DRM (provided within DKs) to get accurate definition of tiler passes. They come along with targets to be reached:

1. Via tiling
   - tile both metal stripes and via;fill between them
   - tile with 65% as target, but do not violate max density
2. Metal;fill (squares)
   - tile with 45% as target, but do not violate max density
3. Metal;fillOPC (stripes)
   - tile with 45% as target, but do not violate max density

Tiler GUI



metals

shapes

gradient (runtime)

RDL L-shapes

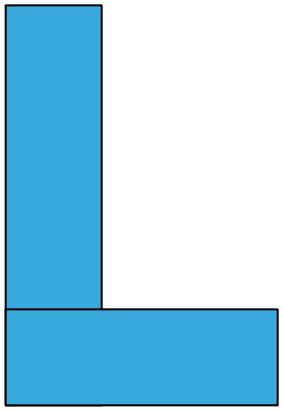
Via tiling (pre-requires metals tiling to be enabled)

Routing direction

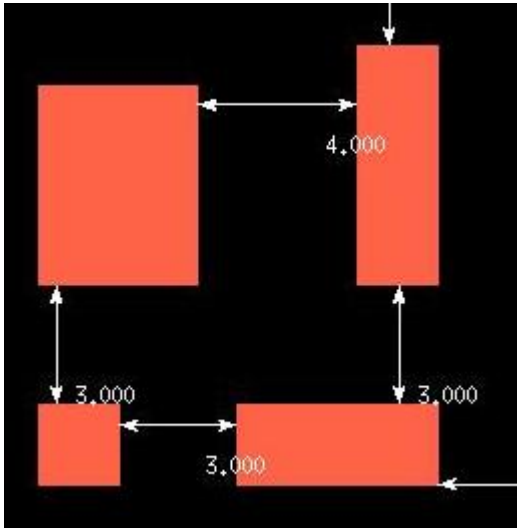
Via tiling to include pre-existing metal;fill

L-shapes

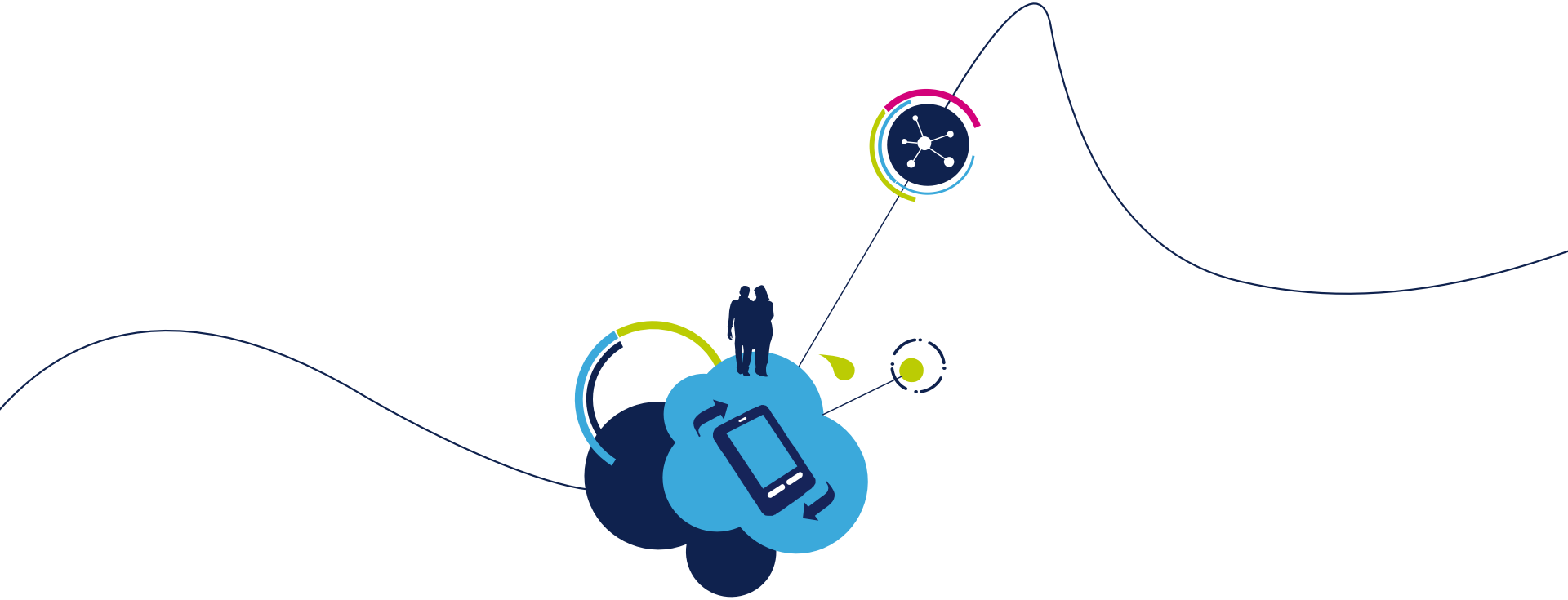
- The last level, usually Alucap, is tiled with specific shapes, named L-shapes
- They are designed to allow the FIB team to calibrate their optical tool
- The new shape takes into account extra DFM constraints in recent processes



Current shape



Future shape



Thank You