C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG_-6U1X2T8XLB
Release Notes and Known Problems and Solutions

1. Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library Name	C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG_6U1X2T8XLB
Library Version	7.0
Library Type	IO Cells
Technology	CMOS028_FDSOI
DK Version	DK_cmos28FDSOI_RF_6U1x_2T8x_LB 2.8.c-08

1.2 Impact of Product Release

For latest information, please refer to LYS *(http://col2.cro.st.com/libyield).*

1.3 Related Documentation

- **C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG_7.0 User Manual**
- **C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG_7.0 Release Notes and Known Problems and Solutions**
- **C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG_ff28_1.05V_1.95V_125C_7y50kR_ss28_1.10V_1.65V_-m40C_7y50kR_7.0 DataBook**
- **C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG_ff28_1.10V_1.95V_m40C_tt28_1.00V_1.80V_25C_ss28_-0.90V_1.65V_125C_7.0 DataBook**
- **C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG_ff28_0.90V_1.95V_125C_2ey_ss28_0.90V_1.65V_m40C_-2ey_7.0 DataBook**

- **C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG_ff28_0.90V_1.95V_m40C_2ey_ss28_0.90V_1.65V_125C_-2ey_7.0 DataBook**
- **C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG_ff28_1.10V_1.95V_125C_ss28_0.90V_1.65V_m40C_-7.0 DataBook**
- **C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG_ff28_1.10V_1.95V_m40C_7y50kR_ss28_1.10V_1.65V_-125C_7y50kR_7.0 DataBook**
- **C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG_7.0 HDL MODELS model usage guidelines**

2. Changes with respect to all Previous Versions

2.1 Changes in Version 7.0 w.r.t Version 6.0

A. STF are Characterized with SPICE DK_cmos28FDSOI_RF_6U1x_2T8x_LB 2.8.c-08

B. 86 corners are added in this release

Spice Updated and Align with New DK.

2.2 Version 6.0

A. This is the Final release.

B. This package contains Verilog, libs, Cadence LEF, SIGNOFF LEF, SIP, SIGNOFF GDS, CDL and SYNOPSYS LAYOUT & FRAM.

(1) Verilog Models:

I. Verilog (.v) model : Compliance with power aware flow.

II. In VERILOG Pin name, Pin direction and functionality is aligned with Usermanual .

(2) Liberty NLDM (STF) :

I. STF view is compliance with UPF flow .

First Release

3. Known Problems and Solutions of this release

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Stand alone Level

ERROR : Rule B1.DEN.1 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule B2.DEN.1 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.1 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.10 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.11 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.12 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.2 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.3 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.4 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.5 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.6 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.7 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.8 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule EMET.DEN.9 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule FD_131a_V5_C - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule FD_131a_W0_C - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

ERROR : Rule FD_131a_W1_C - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.

	ERROR : Rule FD_131a_YZ_C - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error. **ERROR : Rule IA.DEN.1 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.** **ERROR : Rule IB.DEN.1 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.** **ERROR : Rule M2.DEN.1 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.** **ERROR : Rule M3.DEN.1 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.** **ERROR : Rule M5.DEN.1 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.** **ERROR : Rule M6.DEN.1 - ERROR will be corrected at SOC level after EMAT (Embedded Metrology Structures Description) structures placement. These structures are placed through Flow (as per DRM) at SOC level and these DRC errors will go away Antenna Error will be corrected at SOC level. checked ALL cell. no Antenna error.**

	**Ignorable LVS/ERC Errors** **cell Level** **ERC_1a, ERC, OPT1**

	**Average consumption is provided in the leakage value for Normal Mode.**

For normal mode typical code is modeled in HDL views while in actual design the compensation code will depend on PVT in the normal mode.

Delay are modeled in Verilog models are as follows:-

1. **Normal to (any mode except invalid) =15 ns**
2. **(any mode except fastfreeze) to normal = 10000 ns**
3. **Fastfreeze to normal =15 ns**
4. **any mode to Invalid = 0 ns**
5. **Invalid to (any mode except normal) = 15 ns**
6. **Invalid to normal =10000 ns**
7. **Default delay other than the above mentioned modes = 15 ns (Example Read mode to IDDQ mode)**

4. Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact HELPDESK (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.

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