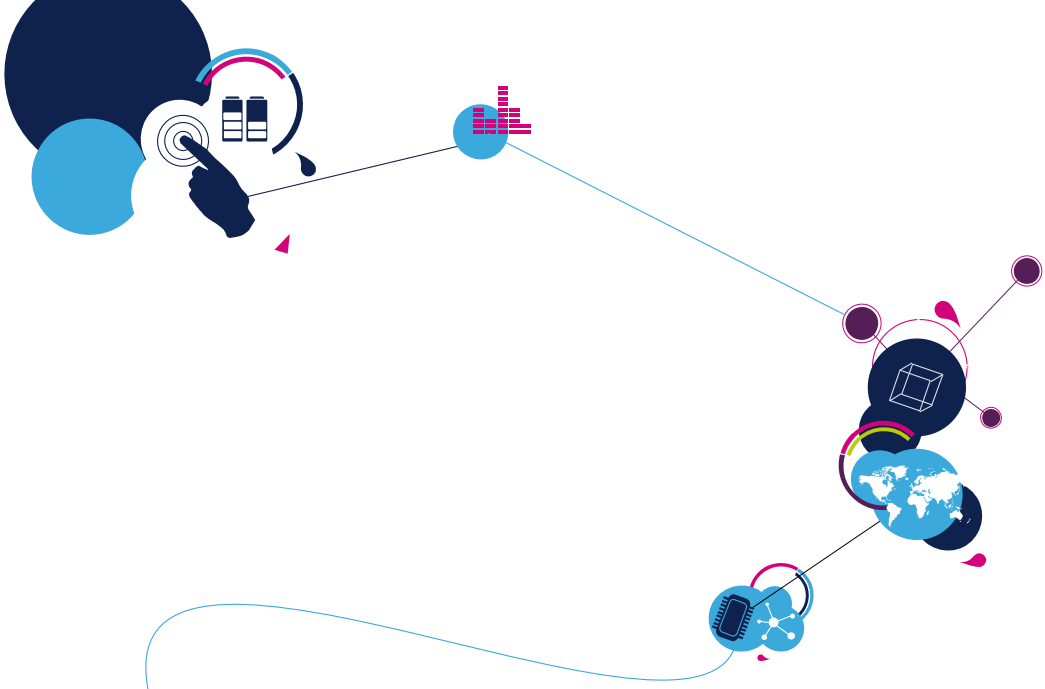

FDSOI – C028FDSOI

Spice Models

ESD Protection NFET documentation

Design Kit Release:	*1.1_RF_mmW*
Document Revision:	*2.0*

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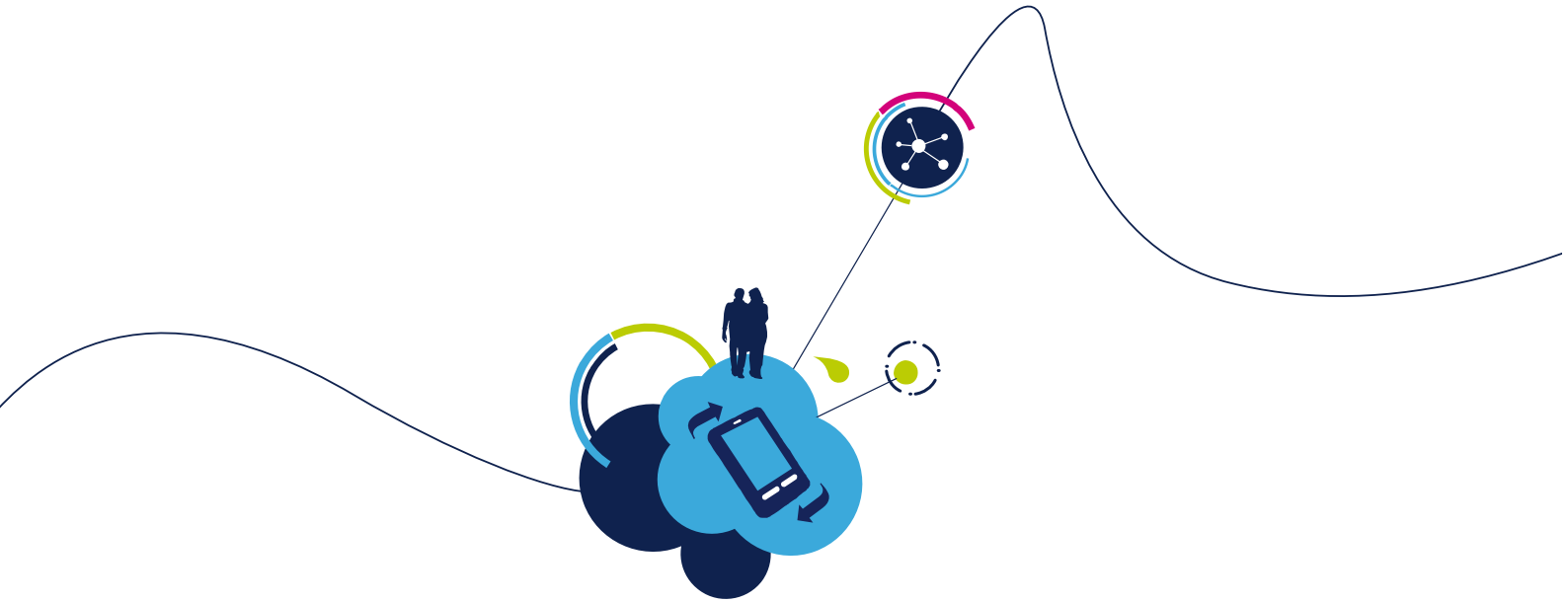

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USER'S MANUAL PURPOSE

The document provides information concerning the C028FDSOI Spice Models - ESD protection NFET from device description to physics.

DOCUMENT REVISION HISTORY

Date	Revision	Revision information
October, 2013	*1.0*	*1st Edition of C028FDSOI Spice Models - ESD protection NFET documentation.*
September, 2014	*1.1*	*Update*
June, 2018	*2.0*	*Major silicon based update*

AUTHORS

Revision	***Author***
1.0	*SZCZAP Melanie*
1.1	*ORTOLLAND Sylvie*
2.0	*ORTOLLAND Sylvie*

TABLE OF CONTENTS

GENERAL INFORMATION

1. SCOPE

This documentation contains the following types of information:

- NFET modeling methodology overview
- Description of statistical process distributions and corner simulation using ELDO/HSPICE/SPECTRE
- Model-to-Hardware correlation plots
- Model features and limitations
- Conditions used for device characterization or model extraction

The version of the models referred in this documentation is C028FDSOI Spice Models - ESD protection NFETs V 1.1 unless otherwise specified.

2. ADDITIONAL REFERENCES

Other modeling information can also be found in the following sources:

- Model syntax, input parameter options and basic topology diagrams are included
- Device performance specifications
- Circuit simulator manuals. For ELDO, HSPICE or SPECTRE users, please see the associated user manuals.

3. SIMULATION APPROACH

Two levels of simulation are available:

- Spice model as default model for AC/DC simulation (no extension or “_nova” extension).
- VerilogA models dedicated to esd simulations (“_va” extension)

The models are ***physic-based and include***

- ***Bias***
- ***Geometry***
- ***Temperature dependencies***
- ***Full range simulation from DC (Spice model) to ESD (VerilogA model) range.***

4. STATISTICS

The model has dedicated pre-defined corners and statistics (Montecarlo) in order to take into account process variations of devices features.

Pre-defined Corners	
Name	Description
TT	Typical performances
ESDBC	Best performances
ESDWC	Worst performances

Table 1 : Pre-defined corners

5. SOA

SOA (Safe Operating Area) are included with the models. SOA libraries are used to alert the user if the device is used out of its operating area. SOAs are activated by default but be deactivated by changing the soa value to 0.

6. NOTES ON CIRCUIT SIMULATORS

The default numerical error controls may be different between simulators, which could affect accuracy of some circuit but not others. User may try to tighten error controls if simulation results difference is noticeable.

MODELS OVERVIEW

1. MODEL STATUS

This section gives a summary about the model with its instance parameters and associated features.

Cellname in DK	Model name	Maturity	Release	Model features								
				Process variations			Mismatch			Post-Layout		
										LPE		
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte carlo	Resistance	Capacitance	SOA
esdnfet	esdnfet esdnfet_nova esdnfet_va	Production	1.1	✓		✓						✓
esdegnfet	esdegnfet esdegnfet_nova esdegnfet_va	Production	1.1	✓		✓						✓

Table 2 : Status.

Instance parameters					Unit
Name	Description	Value			
		min	default	max	
W	Total Gate Width	2.6e-06	286e-06	4e-04	m
L	Gate Length NFET Gate Length EGNFET	0.048e-06 0.15e-06	0.048e-06 0.15e-06	0.080e-06 0.2e-06	m
nf	Number of fingers	1	40	100	
Ldop	Drain side sblk layer length	0.3e-06	0.5e-06	1e-06	m
Lsop	Source side sblk layer length	0.2e-06	0.2e-06	1e-06	m
soa	Soa flag	0	1	1	

Table 3 : Instance parameters.

2. DEVICE DESCRIPTION

2.1. GEOMETRY

The NFET model covers the following geometrical variations which are CAD dimensions:
L : The gate length.
W : The total gate width.
Nfing : The number of hot fingers from 8 to 60.
Ldop: The unsilicided region on drain.
Lsop: The unsilicided region on source.

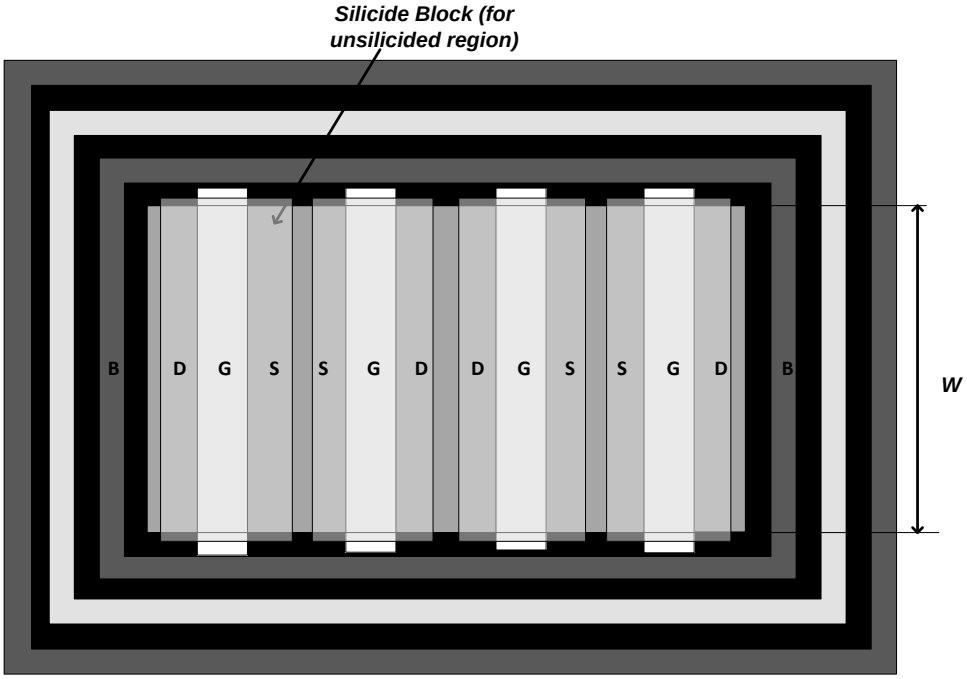

Figure 1 : Top view.

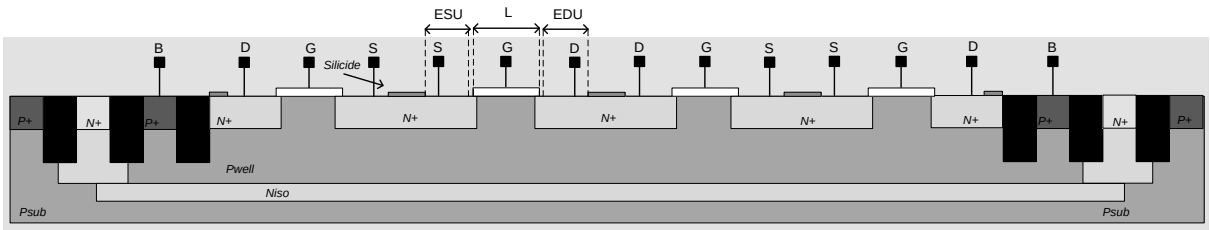

Figure 2 : Cross section (EDU=Ldop, ESU=Lsop).

2.1. MODELS DESCRIPTION

2.1.1 Spice model

This model is dedicated to **AC/DC simulations**. The following features were modeled:

- Fully scalable from frontend to backend.
- Full flavor: EG, RVT.
- Four nodes for different configurations.
- Corners TT, ESDBC, ESDWC.
- DC, AC range coverage:
  - DC behavior: leakage (pn junctions, GIDL, etc.).
  - AC behavior: capacitance
- Temperature dependences.
-

This NFET model covers the NFETs behavior for forward and reverse leakages and capacitances, it includes ***temperature impact*** and ***corners***. It is used for faster simulations for which ESD event is not required.

2.1.2 VerilogA model

This model is dedicated to **ESD simulations**. The following features were modeled:

- Fully scalable from frontend to backend.
- Full flavor: EG, RVT.
- Four nodes for different configurations.
- Corners TT, ESDBC, ESDWC.
- DC, AC and ESD range coverage:
  - DC behavior: leakage (pn junctions, GIDL, etc.) and breakdown.
  - AC behavior: capacitance
  - ESD behavior: self-heating and thermal failure, whatever the ESD waveform: a warning appears when the failure is reached, and the series resistance becomes high (OPEN-like value).
- Temperature dependences.
- Backend connections: Flexframe.

This NFET model covers the NFETs behavior in ***AC, DC, Transient and ESD range,*** and includes ***temperature impact*** and ***corners***.

The sub circuit of the NFET model is described in the figure below.

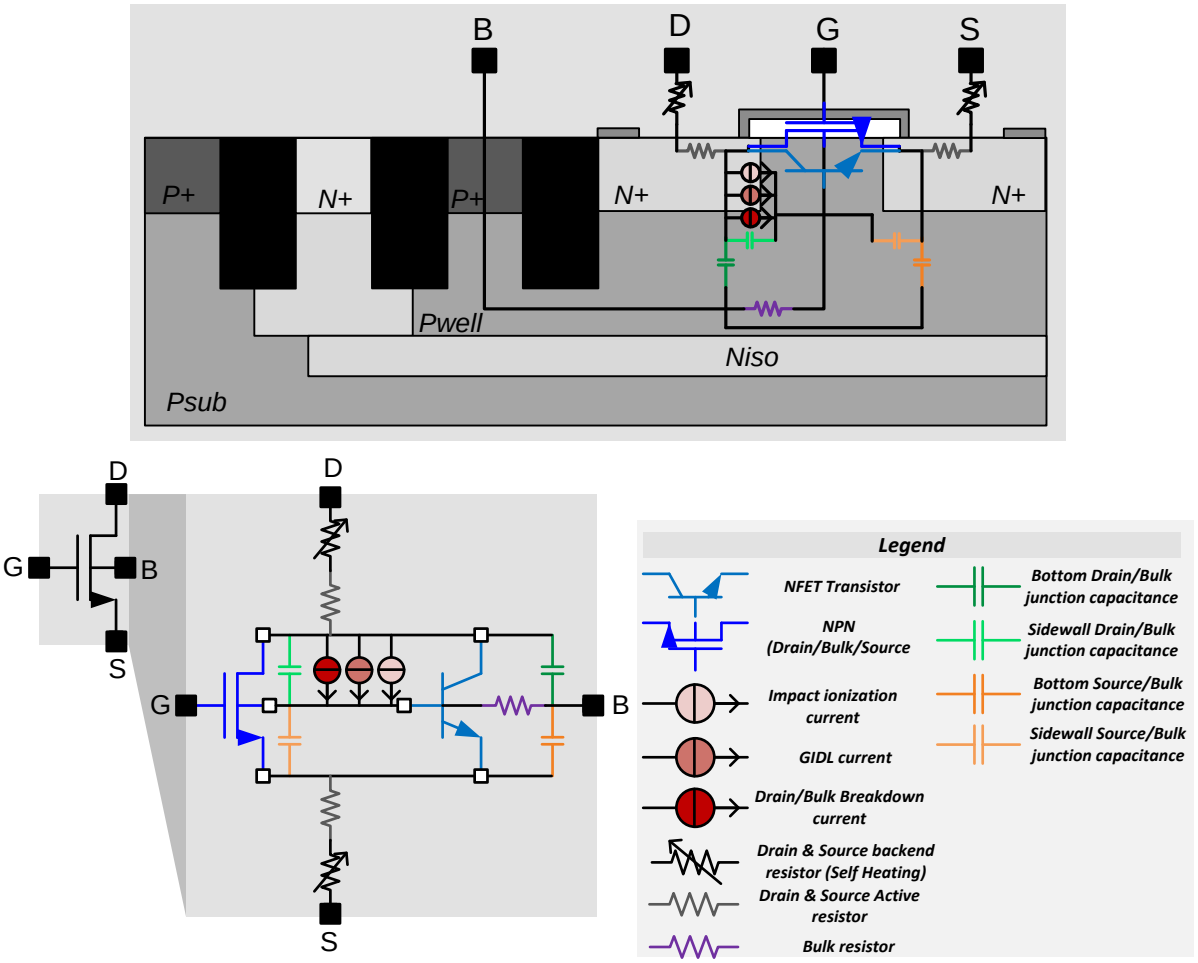

Figure 3: NFET VerilogA Model.

3. DC SIMULATIONS

Comparisons between DC simulations and measurements performed at 25C and 125C are given in this section (dots: measurements, lines: simulations).

3.1. ESDNFET

The Nfets instances are the following: W=15um, Nf=30, L=0.048um, LDOP=0.5um, LSOP=0.2um.

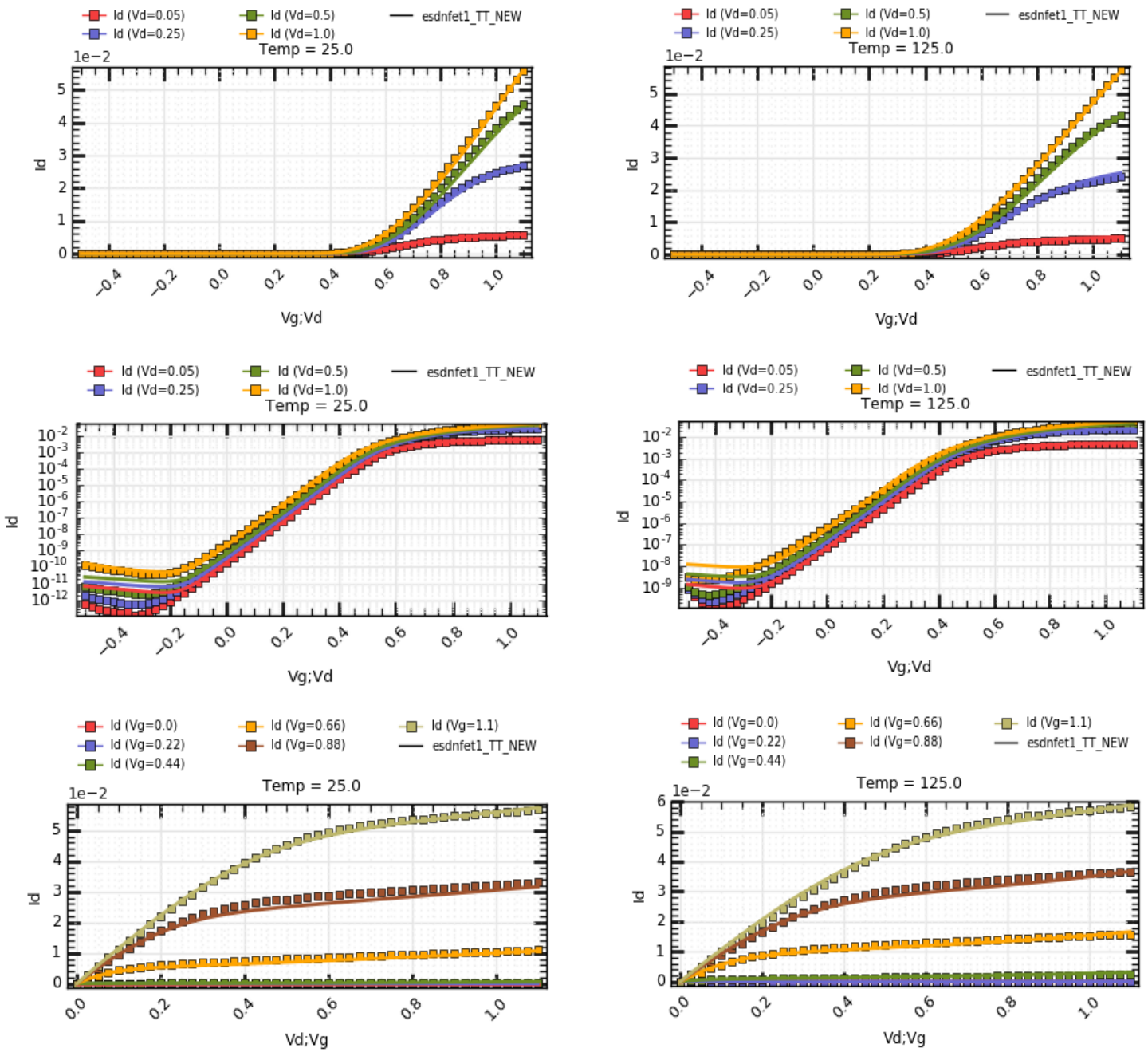

Figure 4: esdnfet DC measurement and simulations @ 25°C/125°C.

3.2. ESDEGNFET

The Nfets instances are the following: W=15um, Nf=30, L=0.15um, LDOP=0.5um, LSOP=0.2um.

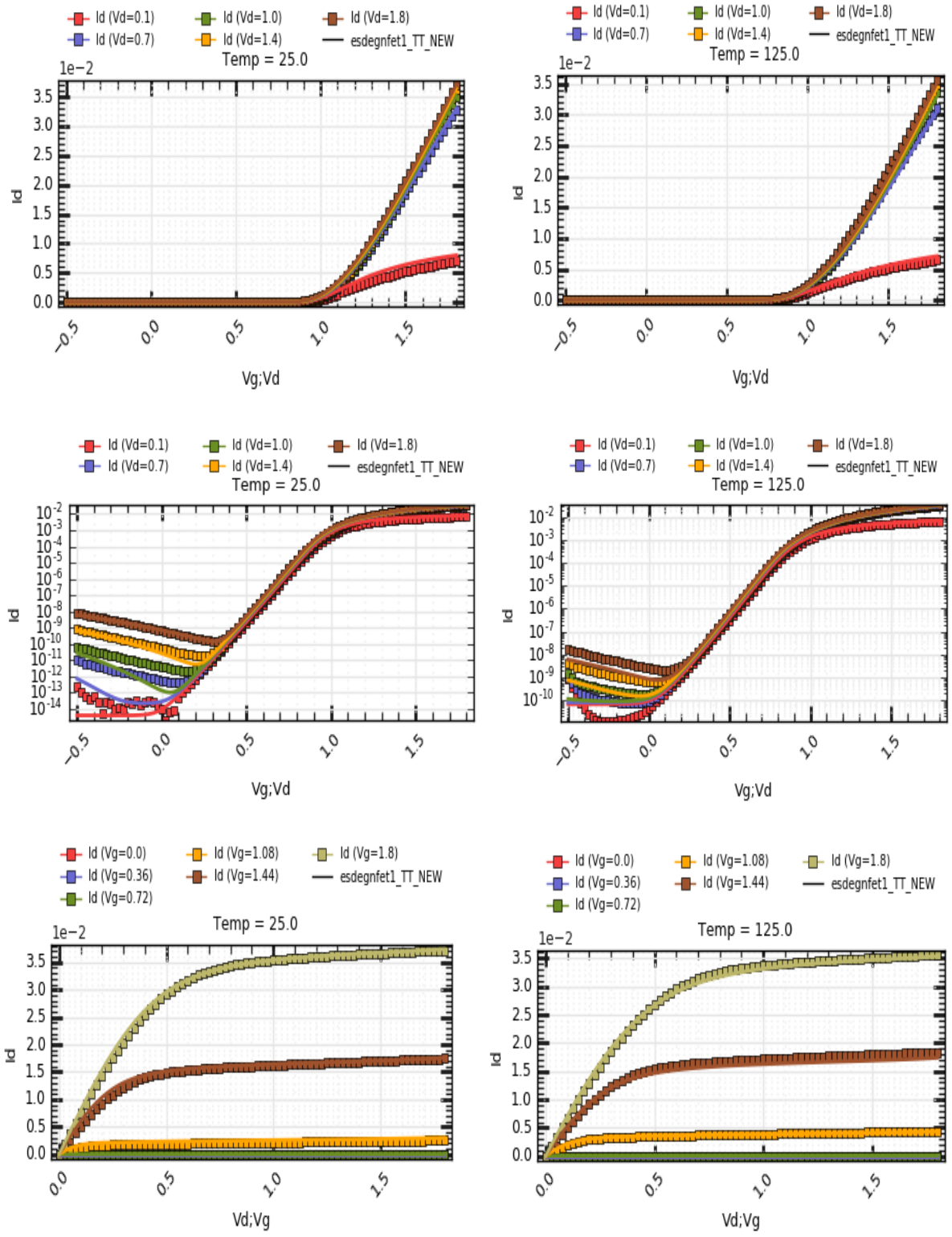

Figure 5: esdegnfet DC simulations @ 25°C/125°C.

4. ESD TRANSIENT SIMULATIONS

Simulations were performed with the NFET model for ***BIMOS*** configuration with a de-biasing poly resistor connected to the bulk, according to the following schematic:

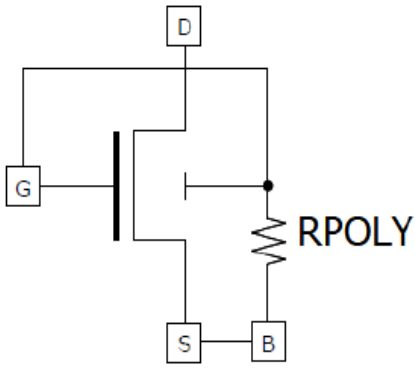

Figure 6: Schematic of BIMOS for TLP measurements.

Voltage pulse is applied to the drain with a 100ns (TLP, HBM conditions) and 1 ns duration (VFTLP, CDM conditions) with a rise/fall time of 10ns and 100ps respectively.

ESD simulations performed with the VerilogA models are given in this section (dots: measurements, lines: simulations).

4.1. ESDNFET

The Nfets instances are the following: W=300um, Nf=60, L=0.048um, LDOP=0.5um, LSOP=0.2um with a Rpoly=5000 Ohm.

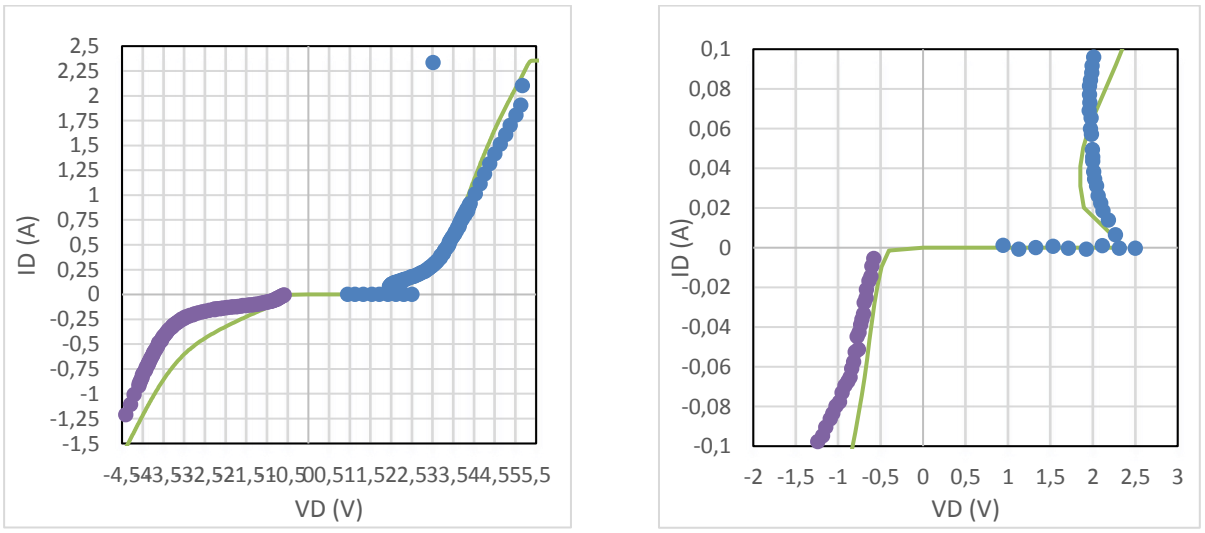

Figure 7: esdnfet TLP 100ns – measurement and simulation @ 25°C (full range and zoom).

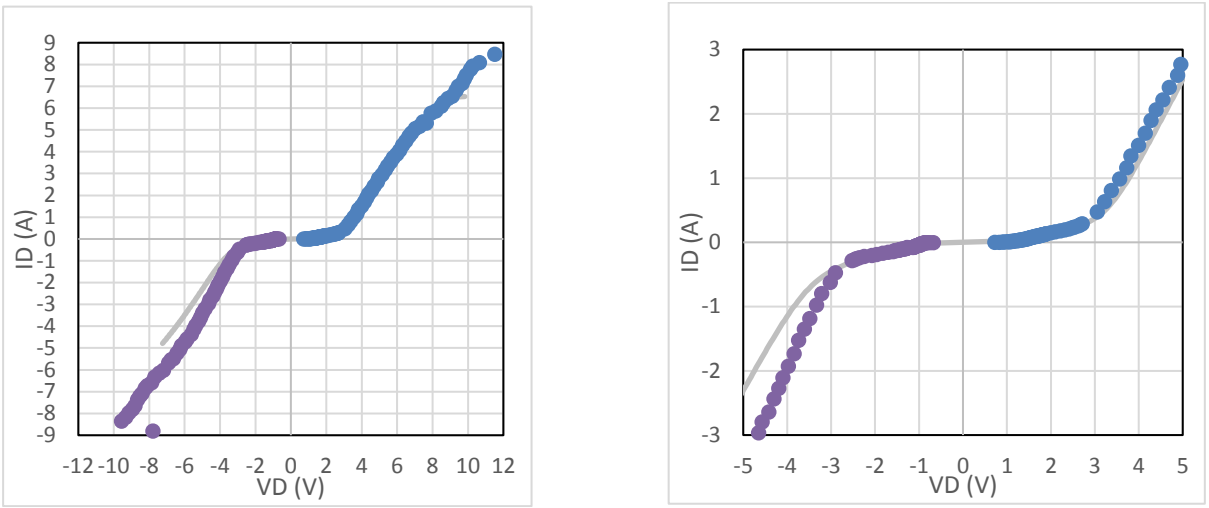

Figure 8: esdnfet VFTLP 1ns – measurement and simulation @ 25°C (full range and zoom).

4.2. ESDEGNFET

The Nfets instances are the following: Wf=300um, Nf=60, L=0.16um, LDOP=0.5um, LSOP=0.2um with a Rpoly=5000 Ohm.

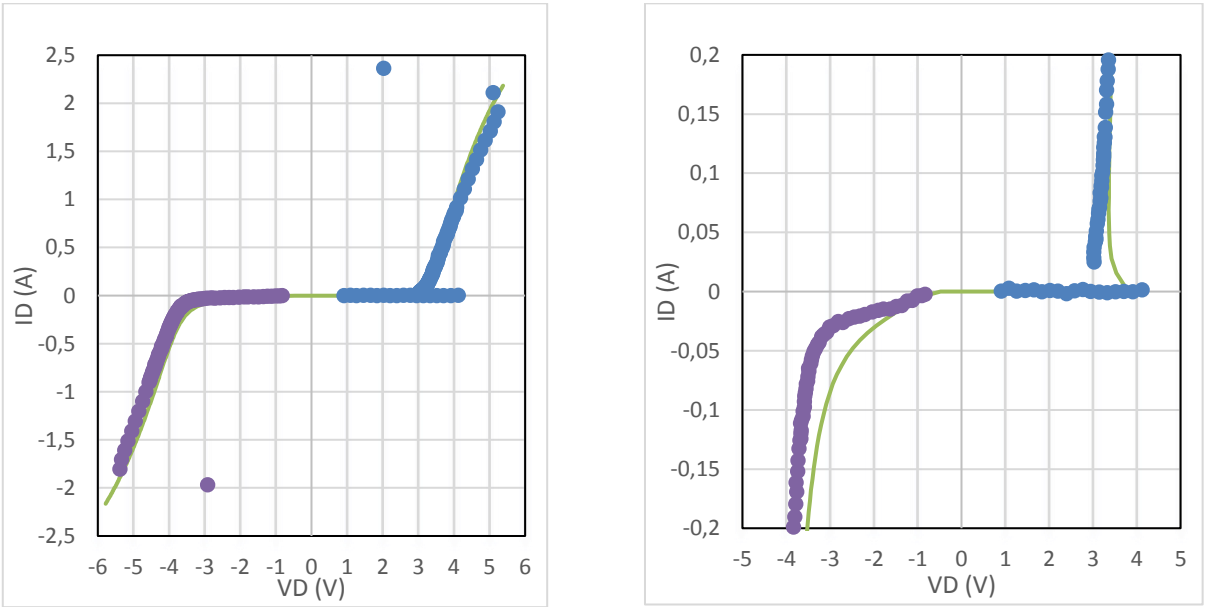

Figure 9: esdegnfet TLP 100ns – measurement and simulation @ 25°C (full range and zoom).

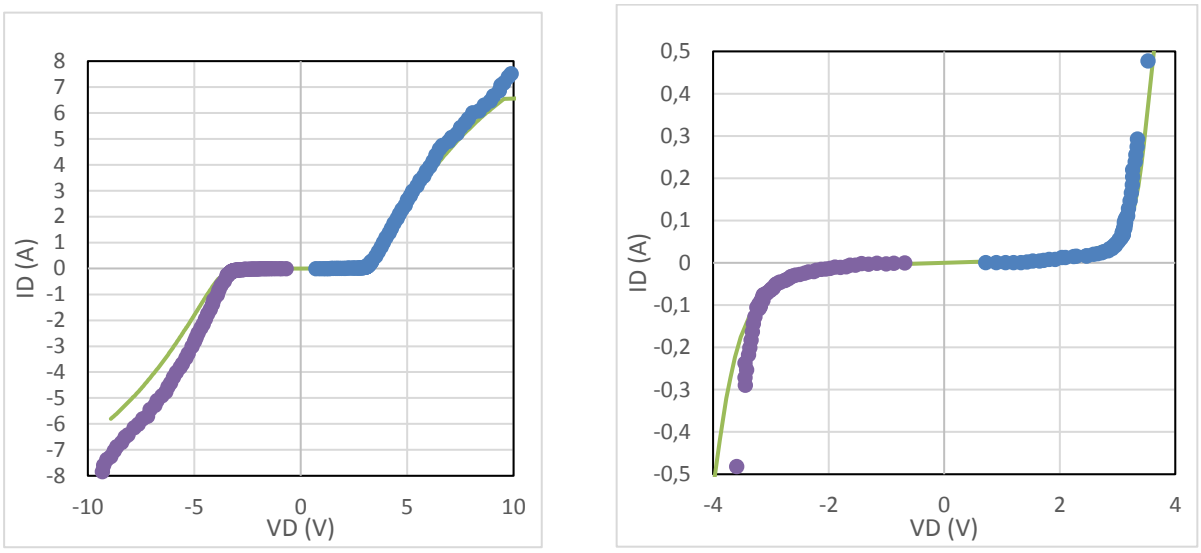

Figure 10: esdegnfet VFTLP 1ns – measurement and simulation @ 25°C (full range and zoom)..