

TITLE:CMOS28FDSOI CALIBRE LVS AND PEX TOOLS MANUAL**Table of Contents****Table of Contents**

1 – IMPORTANT NOTE	3
2 – Set-up	3
3 – PURPOSE	3
3.1 – Layout Versus Schematic (LVS)	3
3.2 – Post-Layout Simulation (PLS)	3
4 – LVS/PEX related files and variables within the DK	4
4.1 – Architecture & files	4
4.2 – LVS Variables	4
5 – LVS/PEX from Unix:	5
5.1 – Calibre	5
5.2 – PVS	5
5.3 – Star-rcxt	5
5.4 – Quantus-QRC	6
5.4.1 – Calibre-Quantus-QRC	6
5.4.2 – PVS-Quantus-QRC	6
6 – LVS/PEX from Cadence Virtuoso	7
6.1 – Calibre LVS Menu	7
6.2 – PVS LVS Menu	7
6.3 – QRC Menu	8
7 – LVS configuration	8
7.1 – Customization choices	8
7.2 – texting and port methodology	11
7.3 – LVS Resistor Methodology:	12
7.4 – Reviewing Results:	12
8 – SIGNATURE	12
8.1 – Signature ToolBox Description	12
8.2 – Graphical User Interface of Signature Toolbox	13
9 – Diode management in LVS	13
10 – LVS Layers usage:	13
11 – cadence PVs-lvs vs mentor calibre-lvs	14
11.1 – Customization window / switches	14
11.2 – LVS inputs : layout and schematic databases	15
11.3 – LVS inputs : layout only	16
.....	16
11.4 – PVS specific : use DFII direct read	17
.....	17

11.5 – Hierarchy management	18
11.6 – Power and ground nets / virtual connect	19
11.7 – Inclusion of new LVS rules	20
11.8 – LVS browser and debugger	21
11.9 – Softcheck errors	22
11.10 – PVS-specific : Stamping Conflict Isolation tool	23
11.11 – LVS for parasitic extraction with QRC	24

1 - IMPORTANT NOTE

The present document is designed to explain how to use Mentor Graphics Calibre LVS, cadence PVS LVS and synopsys StarRCXT, cadence Quantus-QRC within the CMOS028fdsoi DK.

2 - SET-UP

The LVS_PEX (Layout Versus Schematic / Parasitic EXtraction) Module is included in this Design Kit. No supplementary manipulation should be done to access the LVS & PEX features. You must setup the Calibre/Starrcxt versions to the qualified versions, indicated in the release notes.

Warning:

- ^ Always read the release notes before using the related LVS/PEX.
- ^ Always set the Calibre/Starrcxt versions to the qualified version.

3 - PURPOSE

3.1 - Layout Versus Schematic (LVS)

The goal of the LVS extraction is to interpret and extract a netlist from a layout view, and to detect all discrepancies compared to a CDL netlist. Be aware it does not extract natural parasitic devices, like parasitic capacitors between 2 metal interconnexion lines, because this is the goal of PEX tools (Parasitic extraction).

Calibre LVS tool is able :

- to extract all supported devices of a design-kit with their properties from a layout ;
- to detect the connectivity and the hierarchy of all the devices in the layout ;
- to compare connectivity and devices with a reference netlist, and to highlight discrepancies ;
- if necessary, to reduce some devices in parallel or series (for instance, 2 resistors with R resistivity in series are equivalent to a single resistor with $2 \cdot R$ resistivity) during comparison ;
- to execute ERC (Electrical rule check) rules, that are defined to check if the way the circuit has been connected is coherent with technology (well biasing, etc.).

3.2 - Post-Layout Simulation (PLS)

The Post-Layout Simulation (PLS) flow is automating the interconnect RC parasitics extraction from a GDSII database and a CDL netlist to a Spice (ELDO format) or a DSPF netlist at device (transistor) level. The interconnect parasitics extraction is performed by an Interconnect Extractor tool for the full chip, or by a Field Solver for very accurate extraction on specific nets. The device extraction and connectivity is performed by a Device Extractor tool which provides a database in which the device recognition is made and the design network is established, and on which the Interconnect Extractor tool is used. In fact, the Interconnect Extractor uses the Device Extractor LVS database to extract the RC parasitics on the interconnect layers and to generate the suitable spice netlist according to the devices extraction, terminals and pins recognition performed by the Device Extractor.

4 - LVS/PEX RELATED FILES AND VARIABLES WITHIN THE DK

4.1 - Architecture & files

- ⤴ \$PDKITROOT/DATA/LVS: contains all lvs and extraction files.
- ⤴ \$PDKITROOT/DATA/PEX: contains all lvs and extraction files.

4.2 - LVS Variables

Variable	Usage
MGC_CALIBRE_LVS_RUNSET_FILE	LVS calibre runset file
MGC_CALIBRE_CUSTOMIZATION_FILE	DRC & LVS customization file

5 - LVS/PEX FROM UNIX:

5.1 - Calibre

From Unix terminal, you just have to execute:

calibre -gui or calibre -gui -lvs

By default, the LVS runset will be loaded by the one indicated through MGC_CALIBRE_LVS_RUNSET_FILE environment variable. You can indicate PEX runset, or directly load it through the command *calibre -gui -lvs -runset \$PDKITROOT/DATA/PEX/STAR/calibrestartrrcxtGuiRunsetlvs* (or QRC runset) for instance.

Batch calibre run can also be executed through the command:

calibre -hier -lvs <lvs ctrl file> > lvs.log

Batch commands and example of <lvs ctrl file> with pre-configured settings to properly run the different flows are also described in the different README files, present in the corresponding directories:

\$PDKITROOT/DATA/LVS/CALIBRE/README

\$PDKITROOT/DATA/PEX/STAR/README

\$PDKITROOT/DATA/PEX/QRC/README

5.2 - PVS

From Unix terminal, you just have to execute:

pvsgui

Then, in the interface, enter the path of the pvtech.lib located in PVS or QRC directory:



Batch PVS run can also be executed through the command:

pvs -lvs -top_cell "<cellname>" -gds "<GDS file>" -source_top_cell "<cellname>" -source_cdl "<CDL file>" {-qrc_data} <PVS ctrl file> & log

Batch commands and example of <PVS ctrl file> with pre-configured settings to properly run the different flows are also described in the different README files, present in the corresponding directories:

\$PDKITROOT/DATA/LVS/PVS/README

\$PDKITROOT/DATA/PEX/QRC/README

5.3 - Star-rcxt

Once the calibre for star-rcxt run has been performed, you have to create an 'AGF' database to link LVS calibre results with star-rcxt extraction with the command:

calibre -query svdb < calibrestartrrcxt.query.ctrl

A template of <calibrestarrcxt.query.ctrl> is provided in \$PDKITROOT/DATA/PEX/STAR directory. Please update it with the correct cell name by replacing all 'myCell' string.

Then, a star-rcxt parasitic extraction can be performed through the command:

```
StarXtract -clean starrcxt.cmd >& starRCXT.log
```

Template of starrcxt.cmd file is provided in \$PDKITROOT/DATA/PEX/STAR directory. Please configure the file with the help of README file provided in the same directory.

Note a "run_dspf" file is also provided to chain all the commands from caliber LVS to Star final extraction.

5.4 - Quantus-QRC

5.4.1 - Calibre-Quantus-QRC

Once the calibre for QRC run has been performed, you have to create an 'AGF' database to link LVS calibre results with quantus-QRC extraction with the command:

```
calibre -query svdb < calibreQRC.query.ctrl
```

A template of <calibreQRC.query.ctrl> is provided in \$PDKITROOT/DATA/PEX/QRC directory. Please update it with the correct cell name by replacing all 'myCell' string.

Then, a quantus-QRC parasitic extraction can be performed through the command:

```
qrc -cmd qrc.ccl
```

Template of qrc.ccl file is provided in \$PDKITROOT/DATA/PEX/QRC directory. Please configure the file with the help of README file provided in the same directory.

5.4.2 - PVS-Quantus-QRC

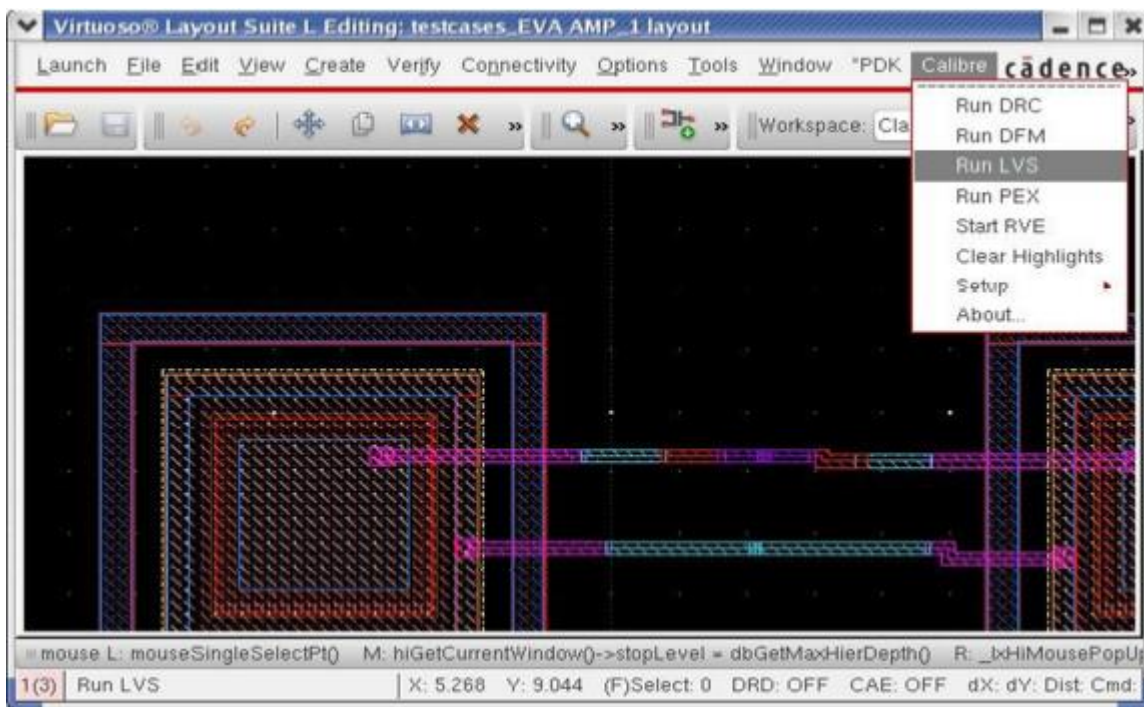
Once the PVS for QRC run has been performed with the option {-qrc_data}, you can directly launch the quantus-QRC command:

```
qrc -cmd qrc.ccl
```

Template of qrc.ccl file is provided in \$PDKITROOT/DATA/PEX/QRC directory. Please configure the file with the help of README file provided in the same directory.

6 - LVS/PEX FROM CADENCE VIRTUOSO

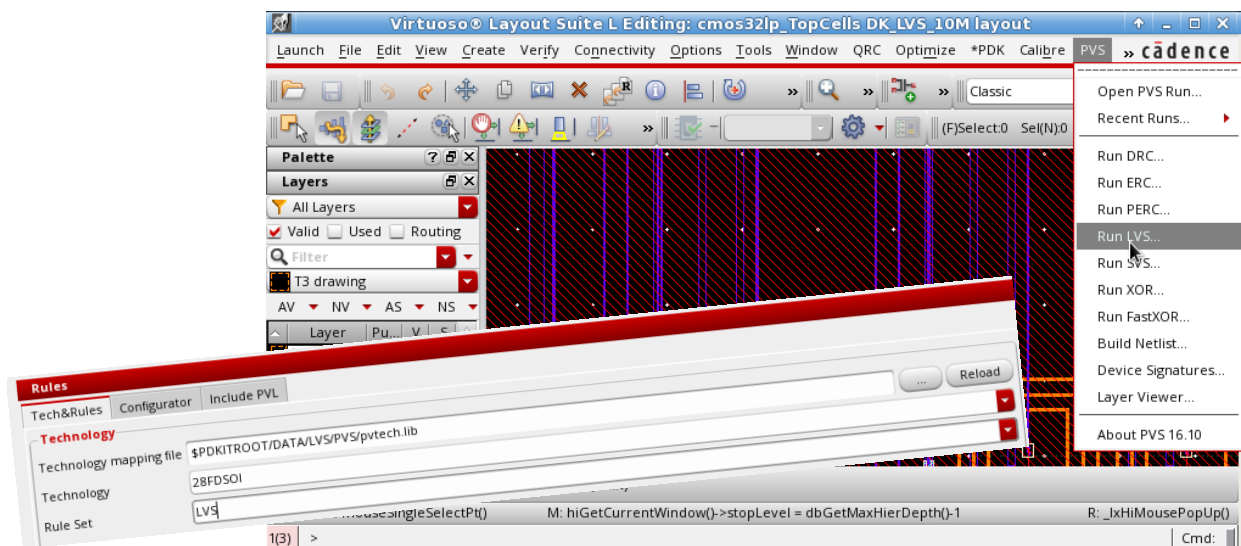
6.1 - Calibre LVS Menu



Calibre Menu from Virtuoso

Click on 'Run LVS' for LVS.

6.2 - PVS LVS Menu

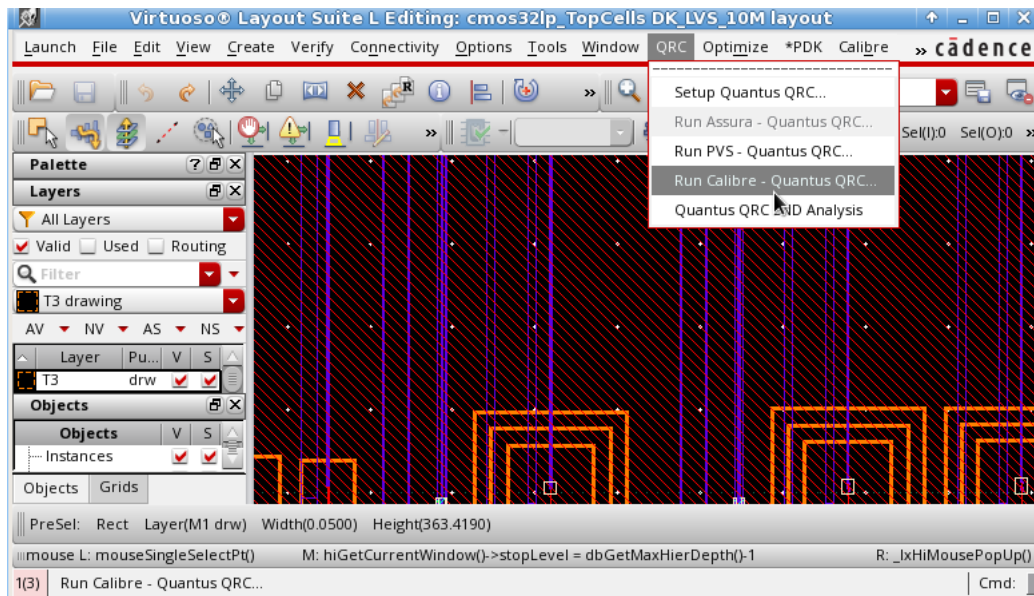


PVS Menu from Virtuoso

Click on 'Run LVS' for LVS.

Configure PVS form by selecting pvtech.lib located in PVS or QRC directory.

6.3 - QRC Menu



After a calibre for QRC or PVS for QRC run, just select the proper flow from QRC menu in your layout view

7 - LVS CONFIGURATION

7.1 - Customization choices

Switch name	Default value	Choice	Description
Check earliest caliber pre-requisite	True	True/False	Check if caliber release is at least as up-to-date that the one used for DK qualification
Disable extraction and comparison of nf	True	True/False	Choose if LVS must or mustn't check the number of fingers for all the MOSFETs.
Disable extraction and comparison of plorlent	True	True/False	Choose if LVS must or mustn't check the gate orientation for all the MOSFETs.
Disable extraction and comparison of ngcon	True	True/False	Choose if LVS must or mustn't check the number of gate access for all the MOSFETs.
Disable comparison of bp of resistors	True	True/False	Choose if LVS must or mustn't check the backplane type (NW, PW or T3) of all the resistances.
Disable comparison of ncr of resistors	True	True/False	Choose if LVS must or mustn't check the number of contact rows of all the resistances.
Disable comparison of area & perim of esd devices	True	True/False	Choose if LVS must or mustn't check the area and perim properties of ESD devices.
Disable comparison of area & perim of pw/tw diodes under LVS1;dg8	True	True/False	When LVS1; dg8 is placed on tw/t3 diodes, diodes are extracted. This switch controls if LVS checks area/perim properties of these diodes.

Do not reduce parallel mos	False	True/False	Manage parallel or series reduction of the corresponding devices (mos, esd devices, resistances or metal resistances, diodes)
Do not reduce parallel or series res			
Do not reduce parallel esd devices			
Do not reduce metal resistances in series			
Do not reduce metal resistances in parallel			
Do not reduce parallel diodes			
Enable Push Down Back Annotation flow	True	True/False	Internal calibre option for hierarchy optimization. Should not be used outside debug purpose.
Disable command expanding seed promotion	False	True/False	Internal calibre option for hierarchy optimization. Should not be used outside debug purpose.
Reduction of split gates for MOSFETS	True	True/False	Manage split gate mosfet reduction.
Disable layout Magnify 'AUTO' option	False	True/False	Internal calibre option for label placement. Should not be used outside debug purpose.
RUN ERC	True	True/False	Execute Electrical Rule Checks: check if wells, substrate, devices are correctly connected.
Power 1V0 (or 1V1, 1V8, 2V5, etc.) net list	"vdd1V0" (or "vdd1V1" etc.)	String into quote ("net1 net2 ...")	For some ERC checks, it is necessary to indicate the nets used for power supplies. All nets are indicated in quote and separated by space.
Power ground net list	"gnd"	String into quote ("net1 net2 ...")	For some ERC checks, it is necessary to indicate the nets used for ground supplies. All nets are indicated in quote and separated by space.
Check for high ohmic paths	False	True/False	Additional ERC aiming at detecting in the layout the paths which could cause an Irdrop in the sources.
FET tolerance for comparison on L & W	L (%) - > 0 W (%) - > 1	Percentage Values	Percentage of difference on L & W values for FET tolerated by LVS.
Resistor tolerance for comparison on L, W & R	L (%) - > 0 W (%) - > 1 R (%) - > 1	Percentage Values	Percentage of difference on L, W & R values for resistors tolerated by LVS.
Capacitor tolerance for comparison on L & W	L (%) - > 0 W (%) - > 1	Percentage Values	Percentage of difference on L & W values for capacitors tolerated by LVS.
Diod tolerance for comparison on area & perim	Area (%) - > 0 Perim (%) - > 0	Percentage Values	Percentage of difference on area & perimeter values for diods tolerated by LVS.
Inductor tolerance for comparison on W, S & X	W (%) - > 0	Percentage Values	Percentage of difference on W, S & X values for inductors tolerated by LVS.

	S (%) - > 0 X (%) - > 0		
ESD devices tolerance for comparison on W	W (%) - > 0	Percentage Values	Percentage of difference on W values for ESD devices tolerated by LVS.
ESDSH devices tolerance for comparison on Wesd, Lesd, Ldop, Lsop	Wesd (%) - > 0 Lesd (%) - > 0 Ldop (%) - > 0 Lsop (%) - > 0	Percentage Values	Percentage of difference on Wesd, Lesd, Ldop, & Lsop values for ESDSH devices tolerated by LVS.
sblk resistor tolerance for comparison on L, W	L (%) - > 0 W (%) - > 0	Percentage Values	Percentage of difference on L & W values for sblk resistors tolerated by LVS.
vpnp device tolerance for comparison on L, W	L (%) - > 0 W (%) - > 0	Percentage Values	Percentage of difference on L & W values for vpnp devices tolerated by LVS.

For Help on ST SWITCHES type unix command : calibreSTSwitchesHelp -lvs

☒ Check earliest Calibre pre-requisite

LVS parameters

☒ Disable extraction and comparison of nf

☒ Disable extraction and comparison of plorient

☒ Disable extraction and comparison of ngcon

☒ Disable extraction and comparison of ptwell

☒ Disable comparison of bp of resistors

☒ Disable comparison of ncr of resistors

☒ Disable comparison of area & perim of esd devices

☒ Disable comparison of area & perim of pw/tw diodes under LVS1;dg8

☐ Do not reduce parallel mos

☐ Do not reduce parallel or series res

☐ Do not reduce parallel esd devices

☐ Do not reduce parallel diodes

☐ Do not reduce metal resistances in series

☐ Do not reduce metal resistances in parallel

☒ Enable Push Down Back Annotation flow

☐ Disable command expanding seed promotions

☒ Reduction of split gates for the MOSFETs

☐ Disable Layout Magnify 'AUTO' option (only if regression with labels)

Hier depth for reading port objects from the layout db

Hier depth for selecting text objects from the layout db

☐ RUN Optional ERC

☒ Enable ERC fill layers connectivity check

only 1.0v/1.1v power nets list

only 1.5v power nets list

only 1.8v power nets list

only 2.5v power nets list

only 3.3v power nets list

all ground net list

all powers net list

all negative powers net list

NOT RECOMMENDED SWITCHES FOR A MORE FLEXIBLE LVS

☒ Allow unused devices filtering (AB AE RC RE RG YC ZB ZC ZD ZE)

Tolerance parameters

FET tolerance for comparison on L(%)

FET tolerance for comparison on W(%)

resistor tolerance for comparison on L(%)

resistor tolerance for comparison on W(%)

resistor tolerance for comparison on R(%)

capacitor tolerance for comparison on L(%)

capacitor tolerance for comparison on W(%)

diode tolerance for comparison on area(%)

diode tolerance for comparison on perimeter(%)

inductor tolerance for comparison on W(%)

inductor tolerance for comparison on S(%)

inductor tolerance for comparison on X(%)

ESD devices tolerance for comparison on W(%)

ESDSH devices tolerance for comparison on Wesd(%)

ESDSH devices tolerance for comparison on Lesd(%)

ESDSH devices tolerance for comparison on Ldop(%)

ESDSH devices tolerance for comparison on Lsop(%)

ESD devices tolerance for comparison on area(%)

ESD devices tolerance for comparison on perimeter(%)

sblk resistor tolerance for comparison on L(%)

sblk resistor tolerance for comparison on W(%)

vpnp device tolerance for comparison on L(%)

vpnp device tolerance for comparison on W(%)

Tolerance for varactor comparison (%)

Customization window for LVS run

7.2 - texting and port methodology

If a label is placed on purpose pin, then the net will be texted with the information but a port will not be created. If a label is placed on purpose label then the net will be texted and a port will be created.

Layers supported for Texting and Port methodology are:

SXCUT, T3, N3, NW, PC, RX, M1, M2, M3, M4, M5, M6, C1, C2 B1, B2, B3, L1, L2, L3, IA, IB, E1, MA, MB, LB

7.3 - LVS Resistor Methodology:

In order to create an lvs resistor (lvsres), a rectangle of purpose lvsres should be placed that covers the entire width of a piece of interconnect. Supported lvsres layers are:

PC, M1, M2, M3, M4, M5, M6, C1, C2 B1, B2, B3, L1, L2, L3, IA, IB, E1, MA, MB, LB

If lvsres is placed over a device terminal or device seed it may not be properly recognized. To be sure the lvsres is properly recognized it should be placed over interconnect. LVS resistors support parallel and series reduction. The lvsres pcell can also be used for lvsres creation.

7.4 - Reviewing Results:

When reviewing the results of a run it is vital to check both the lvs report (run_name.lvs.report) and the extraction report (run_name.lvs.report.ext). Both files contain information that needs to be reviewed to ensure the design is properly passing LVS. It is possible for the LVS Report to be clean but for the Extraction report to have softconnect errors which impact a design. Please see Calibre documentation for description of both of these files.

8 - SIGNATURE

8.1 - Signature ToolBox Description

Signature ToolBox is a product that helps designers to create the LVS extraction deck for their own custom signed devices in STMicroelectronics design kits.

This application uses the Mentor Graphics Calibre Signature feature, which allows to identify a device based upon a set of polygons in the vicinity of the device. The polygons are used as a geometric identification template, called a signature, which is used to match a layout device.

The Signature ToolBox core uses a Tcl program to compute all the parameters entered by the user through a graphical interface and generate the LVS code corresponding to the device which is to be extracted. Then, the computation of the Signature of the device is launched by using Calibre and the final LVS code of the signed device is generated.

Signature ToolBox is useful to easily create LVS code for custom signed device.

You don't need to load additional tools in your environment: only a Design Kit and Mentor Graphics Calibre (release according to the DK used) are needed.

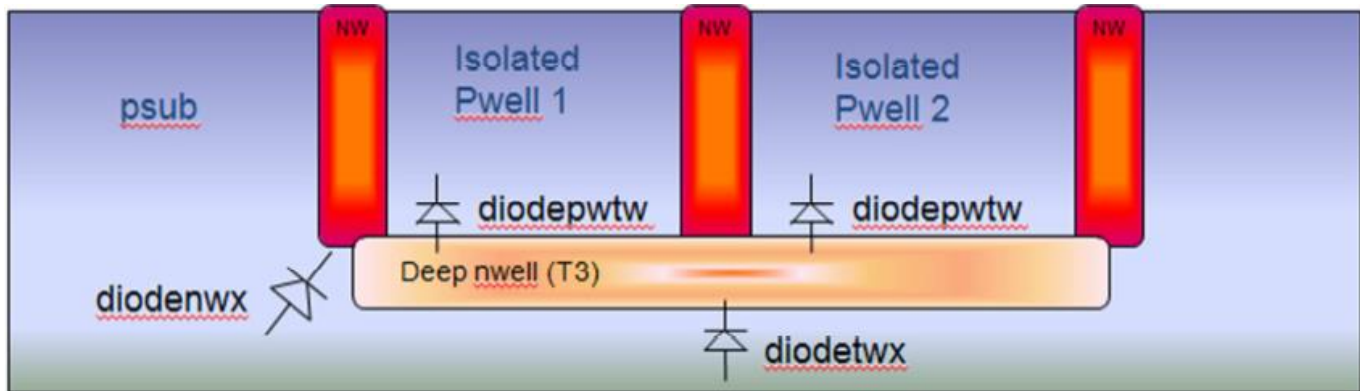
This application presents a graphical user interface with these key elements:

- . LVS rule file selection
- . Mapping file selection
- . Pin layers selection
- . Signature layers selection
- . All the LVS options needed

8.2 - Graphical User Interface of Signature Toolbox

Please consult signature_doc.pdf file to get more information on this feature.

9 - DIODE MANAGEMENT IN LVS



	Inside LVS1 drawing8 marker (200;218)				Outside LVS1 drawing8 marker (200;218)			
	LVS		LVS for PLS		LVS		LVS for PLS	
parasitic diodes	Extracted	Compared	Extracted	Compared	Extracted	Compared	Extracted	Compared
diodenwx	no	no	no	no	no	no	yes	no
diodetwx	no	no	no	no	no	no	yes	no
diodepwtw	no	no	no	no	no	no	yes	no
diodenwx_lvs	yes	no	yes	no	no	no	no	no
diodetwx_lvs	yes	no	yes	no	no	no	no	no
diodepwtw_lvs	yes	yes	yes	yes	no	no	no	no

10 - LVS LAYERS USAGE:

LVS; drawing: Used to identify nwres resistor

LVS; drawing1: mandatory for vnp device to compute W property

LVS; drawing2: Used for esdnfet and esdegnfet_eg devices to identify drain.

LVS; drawing3: Used to identify diodes: tdndsx, egtndsx, egtdpdnw, tdpdnw. If the marker is not present, these diodes are extracted as parasitic components: diodenx, egdiodenx, diodepnw, egdiodepnw.

LVS; drawing4: Used on pcap, ncap, egncap, egpcap devices: used to regroup several devices of a same type into a single one with property ncap, nrep

esdvnpn, esdvnpn, esdvnpn_eg and esdvnpn_eg devices: used to identify

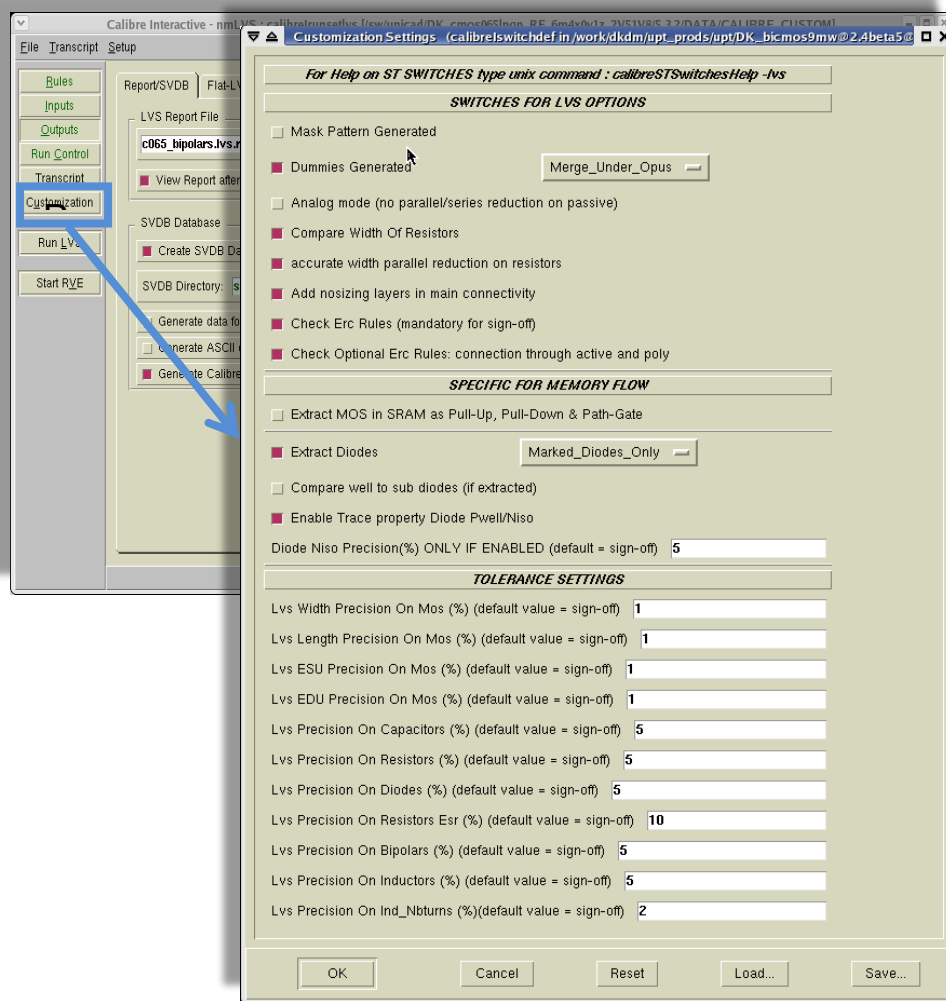
LVS1; drawing8: Used to manage diodenwx, diodetwx, diodepwtw, diodenwx_lvs, diodetwx_lvs, diodepwtw_lvs => See paragraph below.

Other LVS layers have no effect.

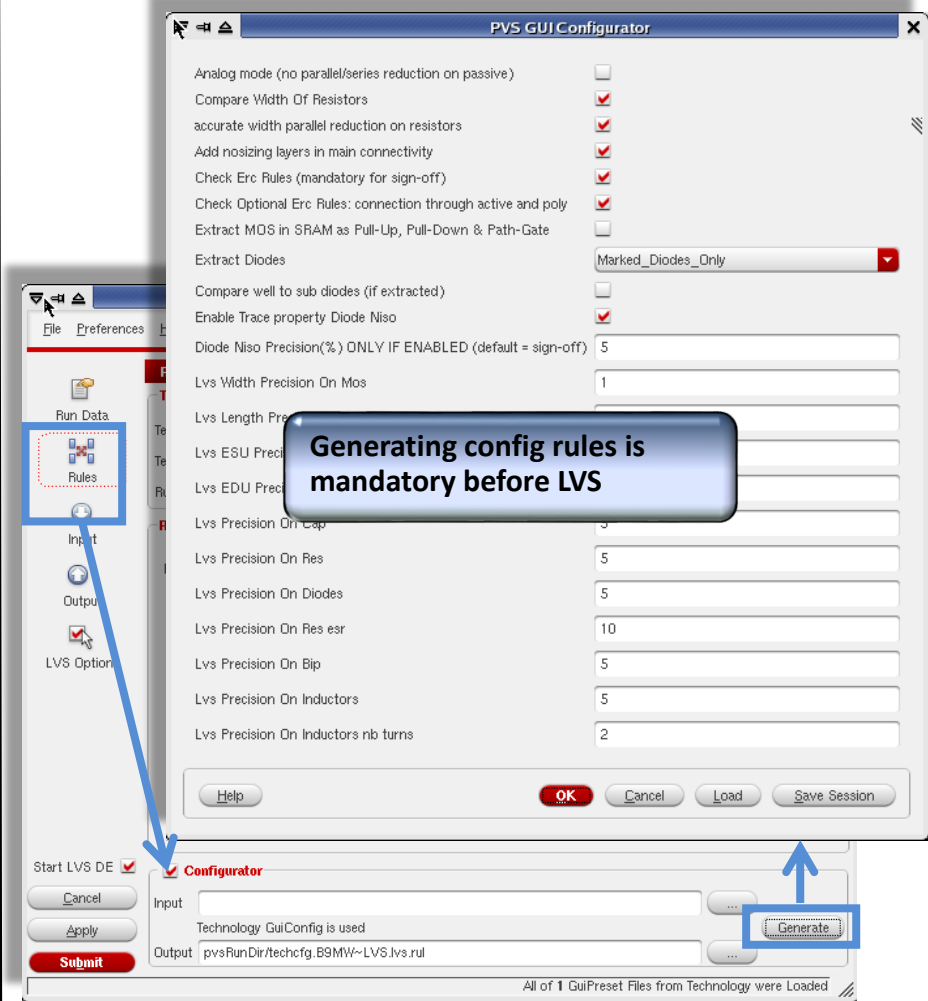
11 - CADENCE PVS-LVS VS MENTOR CALIBRE-LVS

11.1 - Customization window / switches

Calibre :

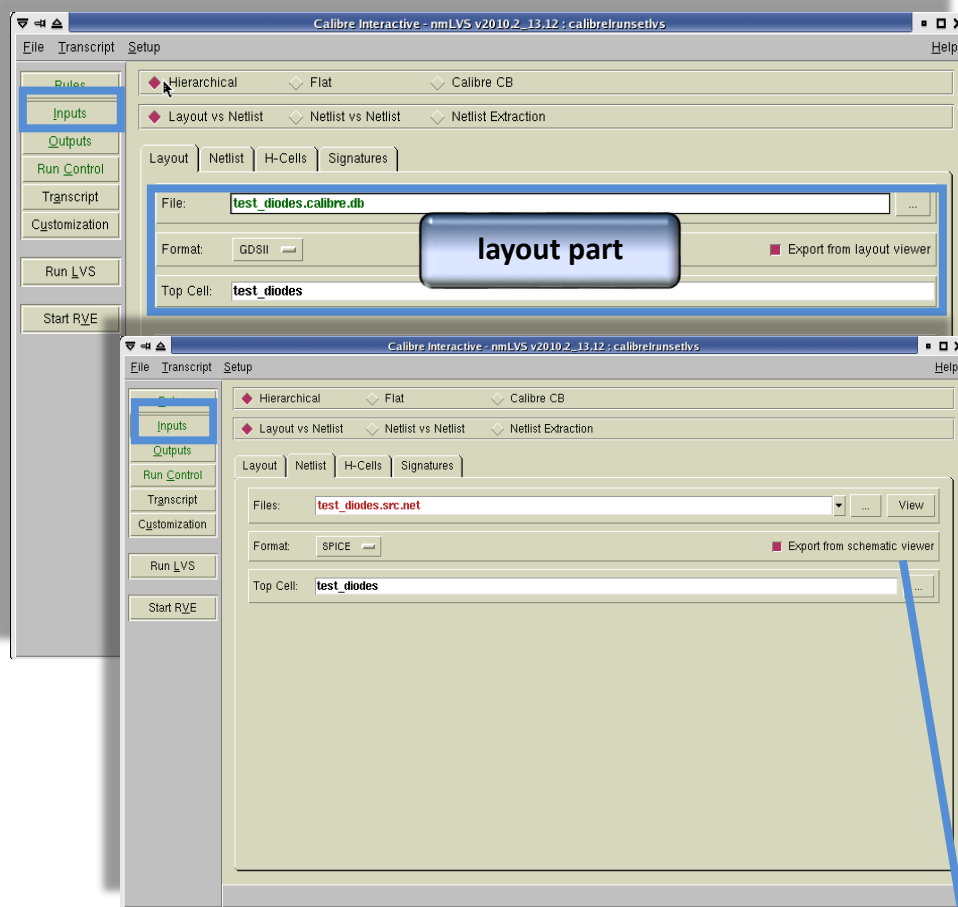


PVS :

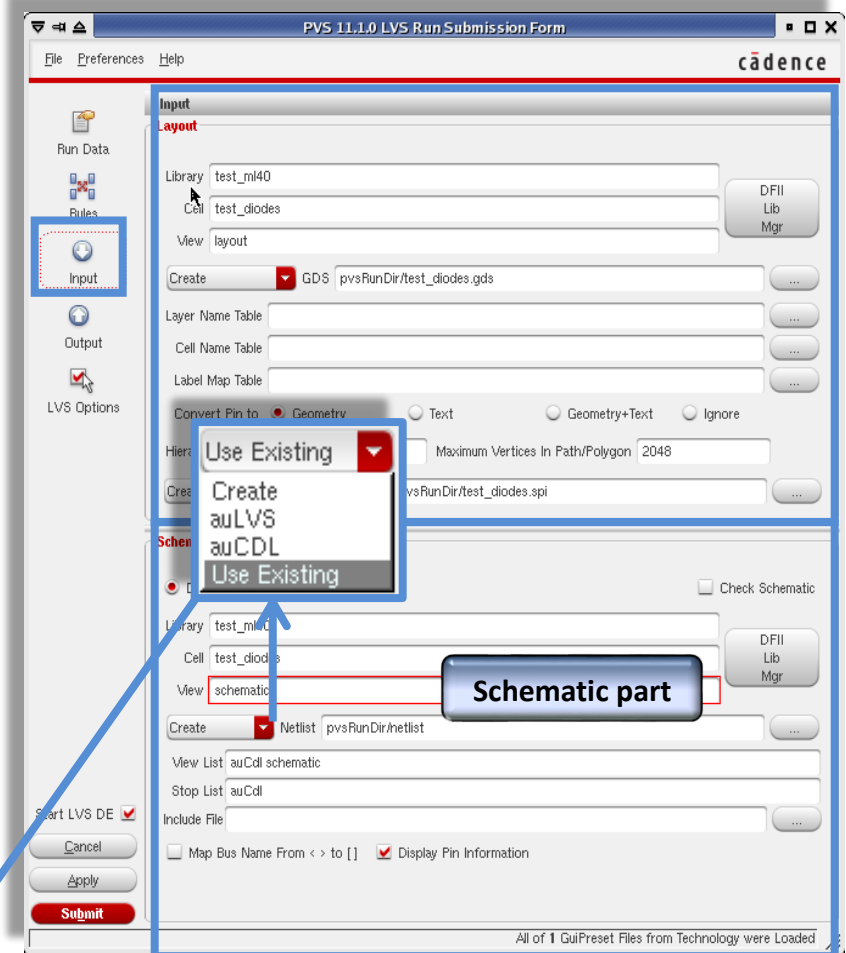


11.2 - LVS inputs : layout and schematic databases

Calibre :



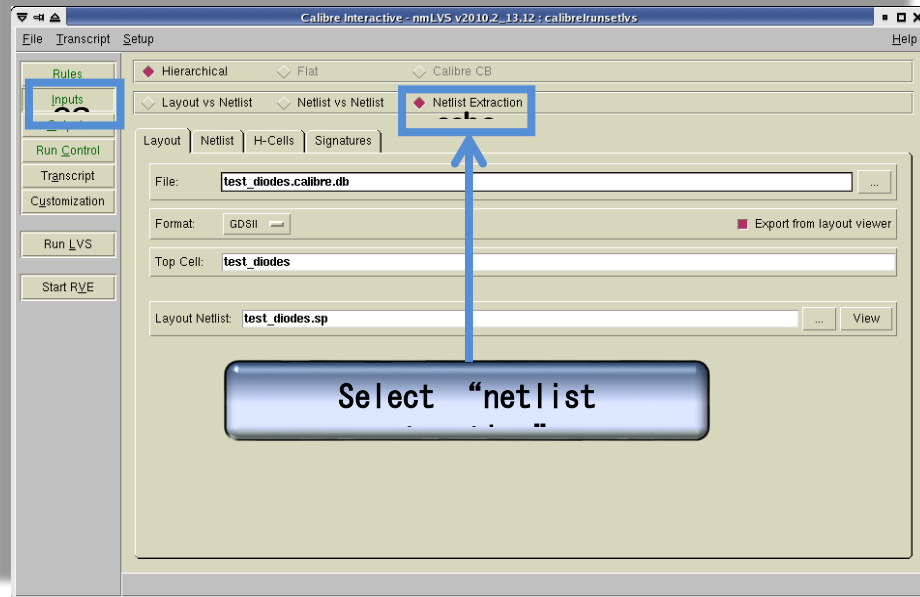
PVS :



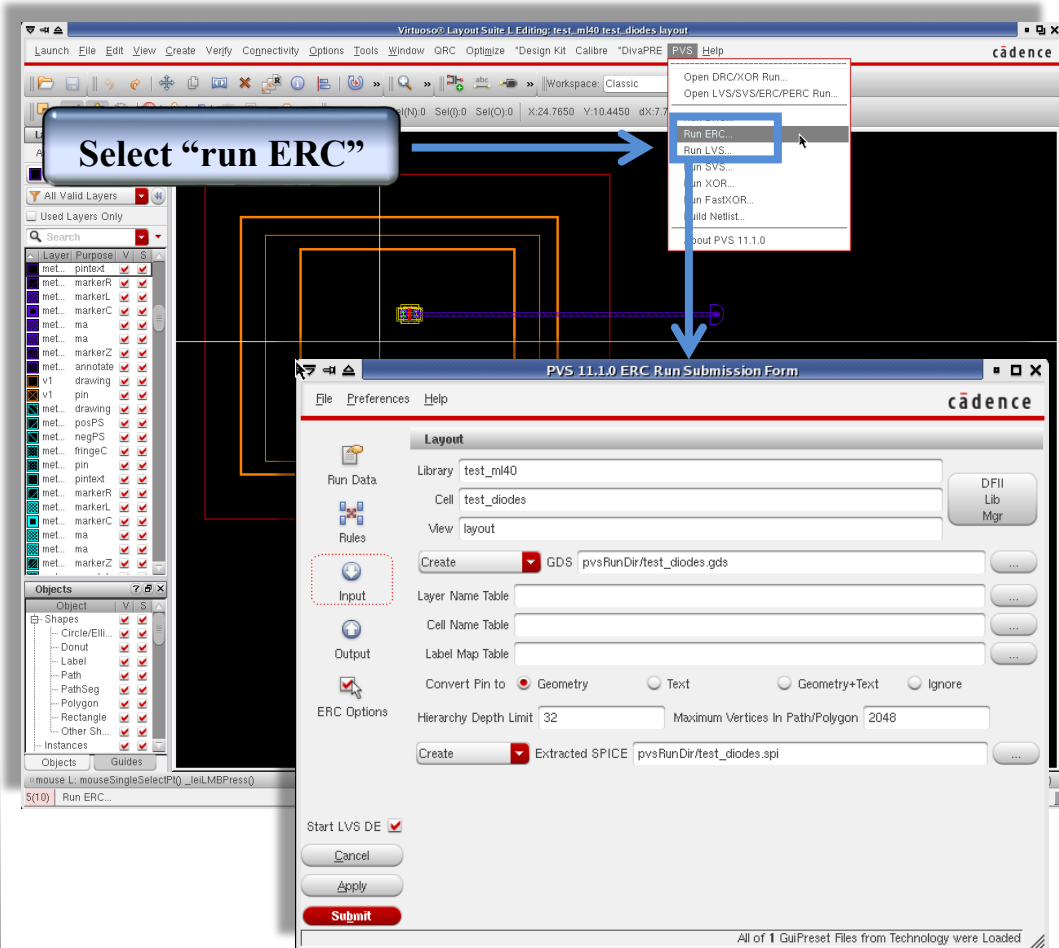
use existing db when
already created

11.3 - LVS inputs : layout only

Calibre :



PVS :



11.4 - PVS specific : use DFII direct read

The screenshot shows the 'PVS 11.1.0 LVS Run Submission Form' window. The 'Input' section is active, showing fields for Library (test_ml40), Cell (test_diodes), and View (layout). The 'DFII Direct Read' option is highlighted in the 'Create' dropdown menu. The 'Schematic' section is also visible, showing fields for Library (test_ml40), Cell (test_diodes), and View (schematic). The 'DFII' radio button is selected under the 'Schematic' section. The 'Start LVS DE' checkbox is checked. The 'Submit' button is at the bottom.

Input

Library: test_ml40
Cell: test_diodes
View: layout

Create: DFII Direct Read
Create: Use Existing
Create: Layer map table

Convert Pin to: ☒ Geometry ☐ Text ☐ Geometry+Text ☐ Ignore

Hierarchy Depth Limit: 32 Maximum Vertices In Path/Polygon: 2048

Create: ☒ Extracted SPICE pvsRunDir/test_diodes.spi

Schematic

☒ DFII ☐ Netlist ☐ Check Schematic

Library: test_ml40
Cell: test_diodes
View: schematic

Create: ☒ Netlist pvsRunDir/netlist

View List: auCdl schematic
Stop List: auCdl

Include File:

☐ Map Bus Name From < > to [] ☒ Display Pin Information

Start LVS DE ☒

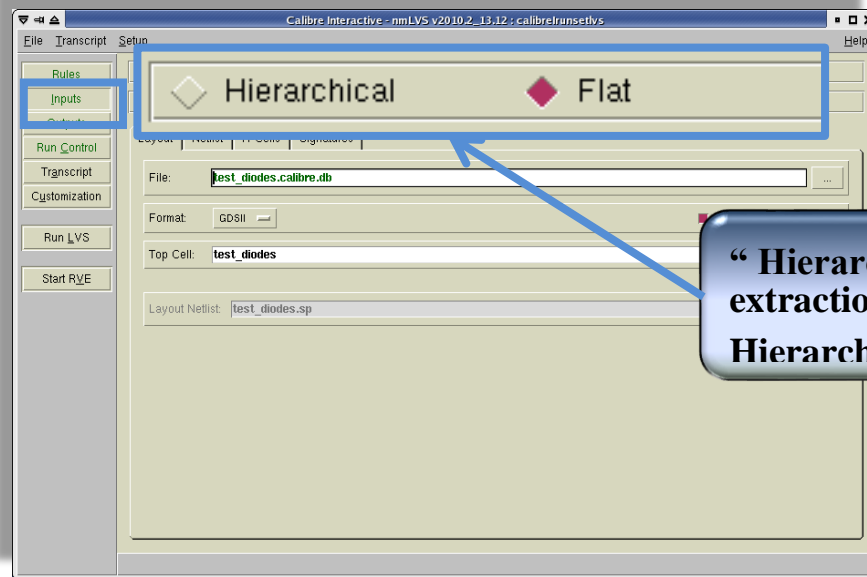
Cancel Apply Submit

All of 1 GuiPreset Files from Technology were Loaded

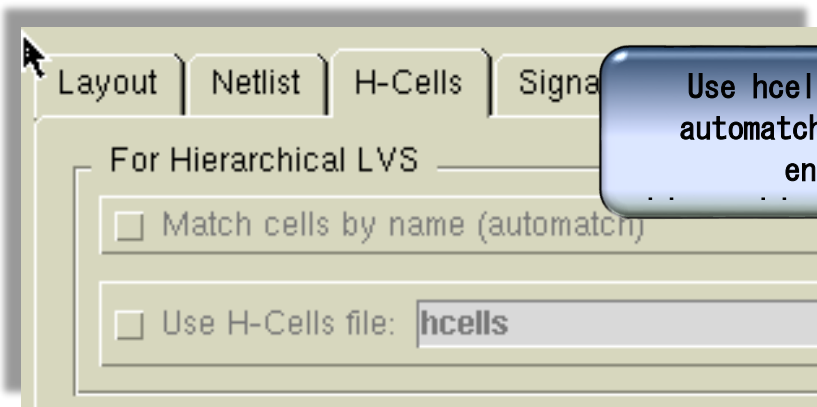
disk space saving :
No streamout !

11.5 - Hierarchy management

Calibre :

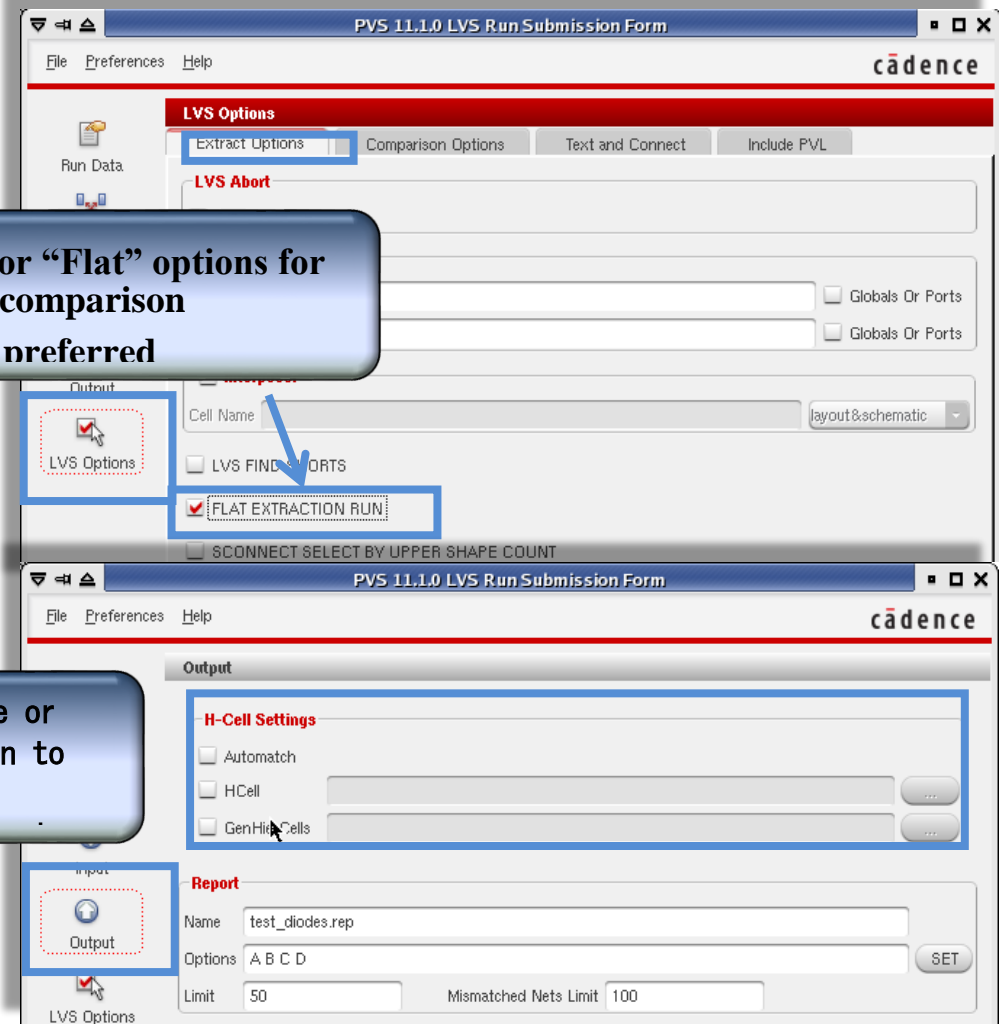


“ Hierarchical or “Flat” options for extraction and comparison
Hierarchical is preferred



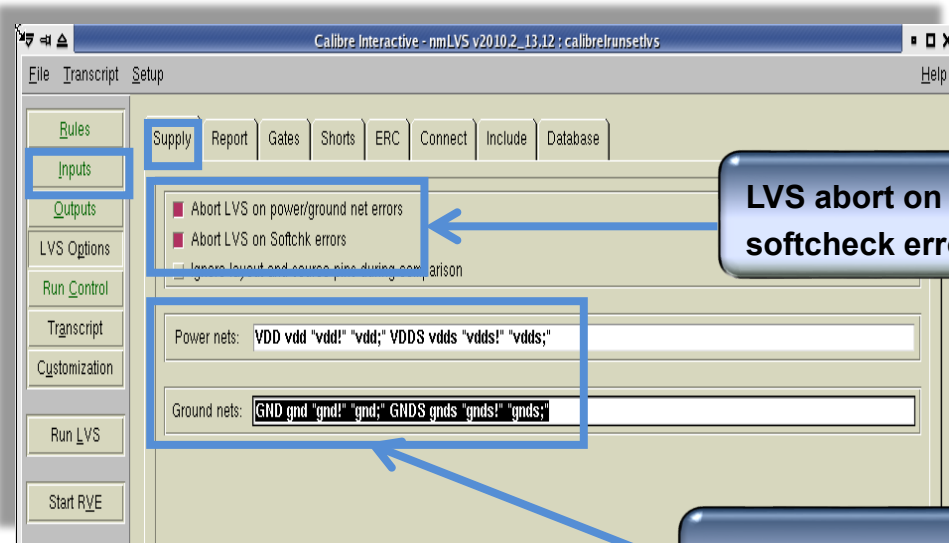
Use hcells file or automatch option to enable

PVS :



11.6 - Power and ground nets / virtual connect

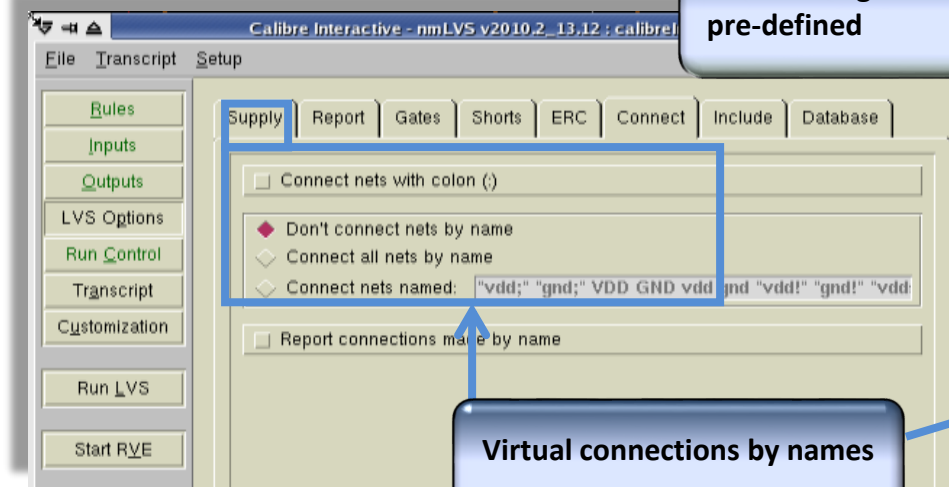
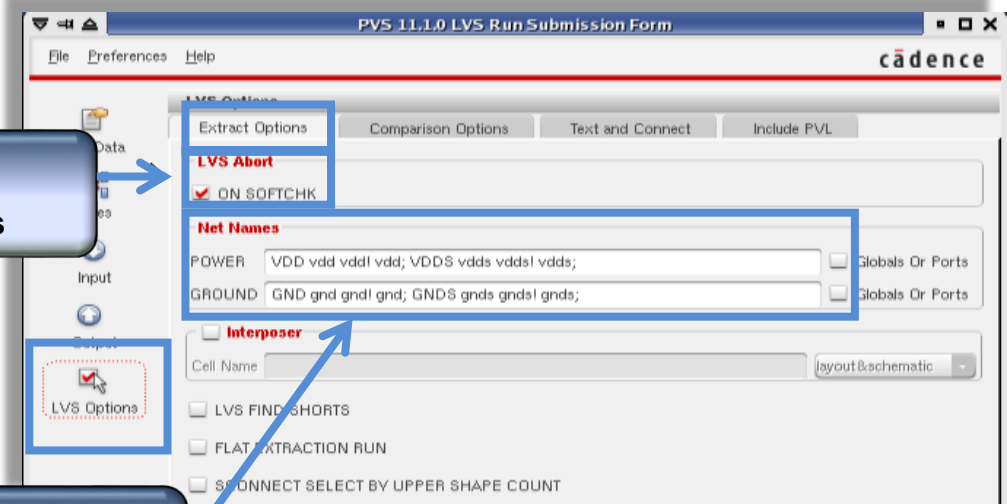
calibre:



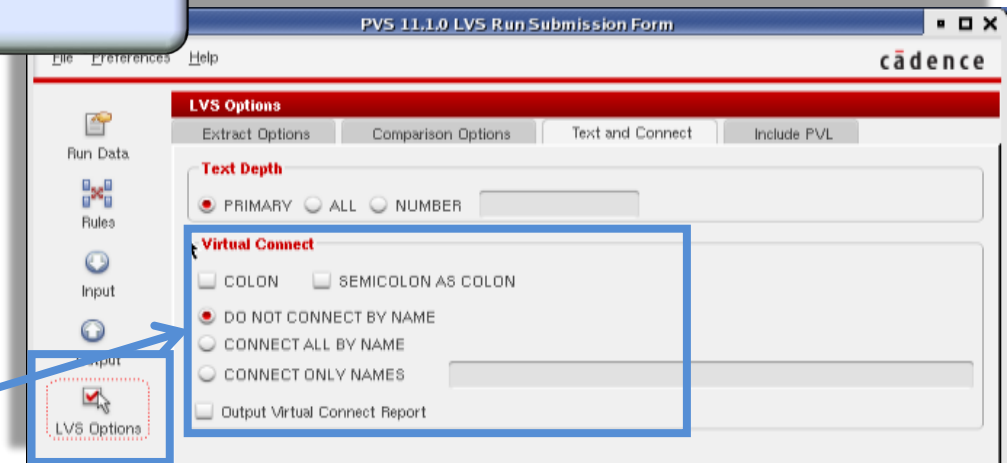
LVS abort on
softcheck errors

Power and ground net names
pre-defined

PVS :

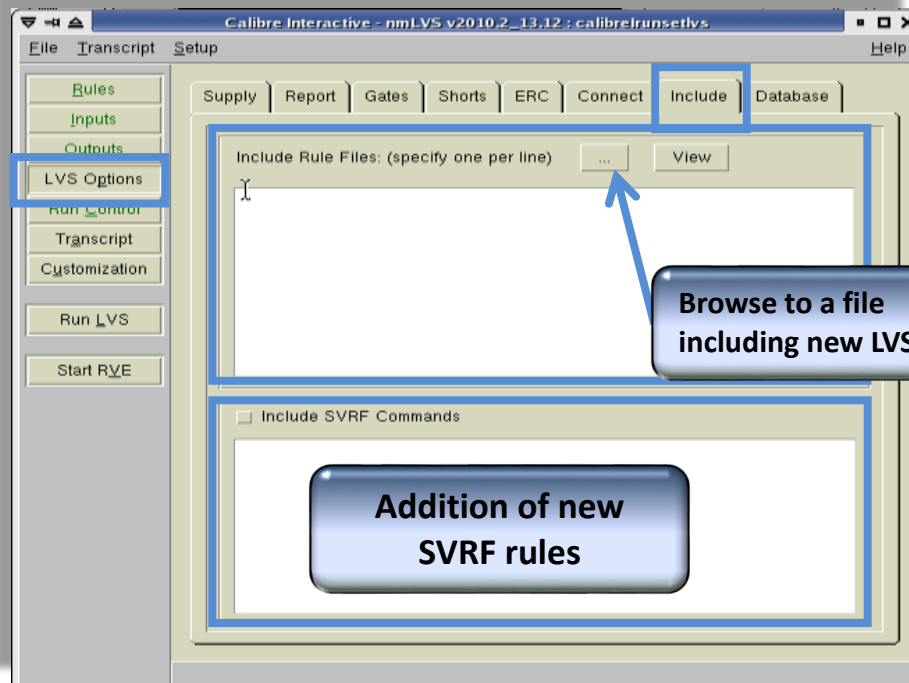


Virtual connections by names

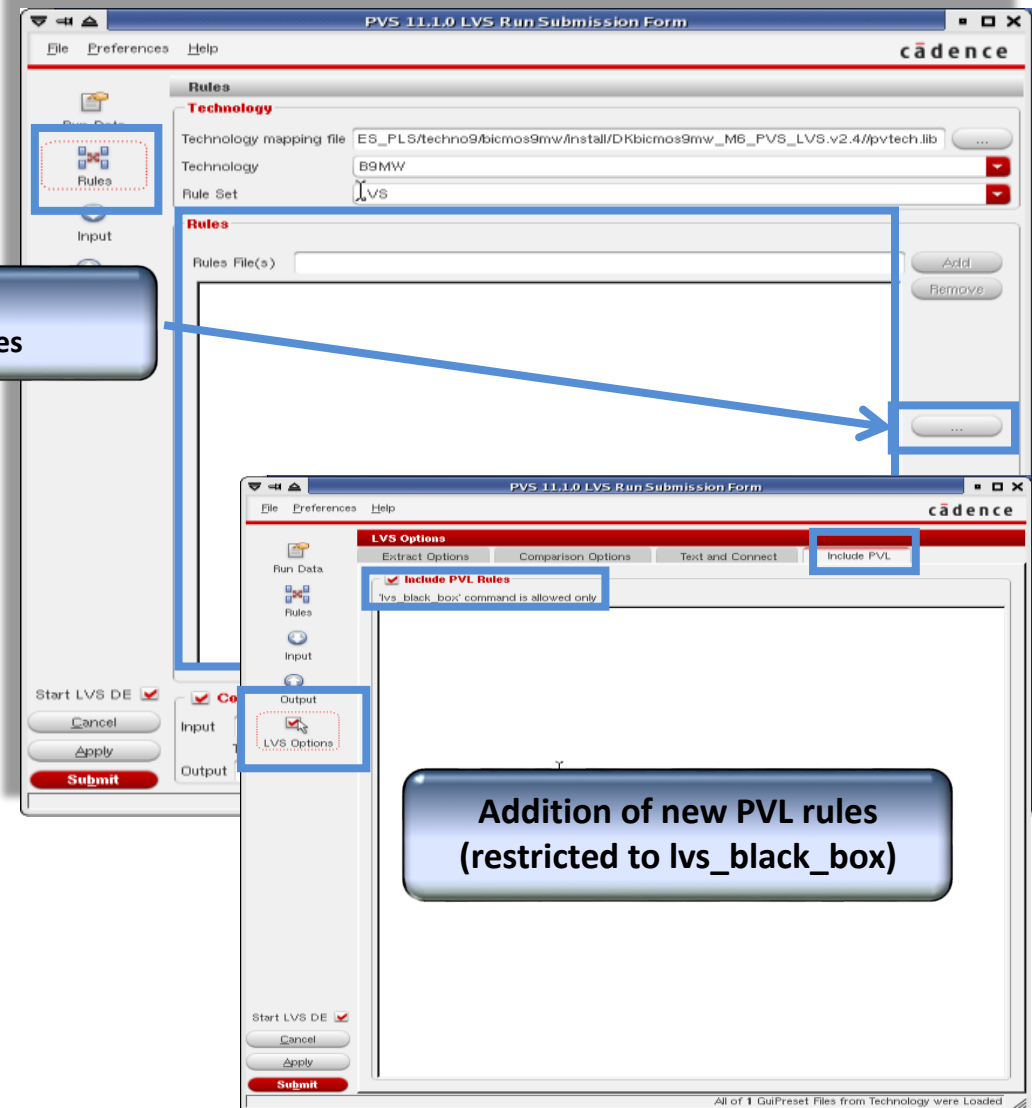


11.7 - Inclusion of new LVS rules

calibre:



PVS :



11.8 - LVS browser and debugger

Calibre :

PVS :

The image displays two software interfaces side-by-side, with blue callout boxes pointing to specific features.

Calibre Interface (Left):

- Comparison report:** Points to the 'Comparison Results' tab in the 'Results' pane.
- ERC rules:** Points to the 'ERC Results' section in the 'Results' pane.
- CDL & Layout netlists:** Points to the 'Layout Netlist' window at the bottom.

PVS Interface (Right):

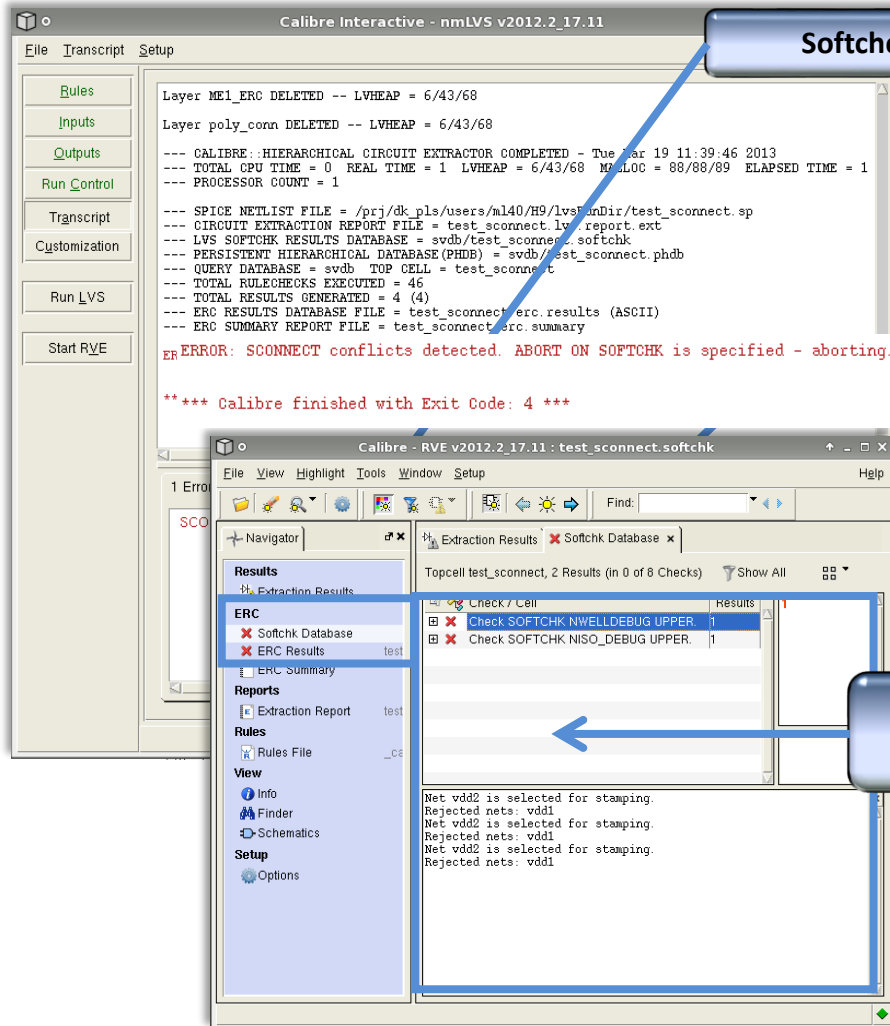
- Comparison report:** Points to the 'Comparison' button in the 'Navigation Report Browser'.
- ERC rules:** Points to the 'Input Files' section, specifically the 'Rule File'.
- CDL & Layout netlists:** Points to the 'Output Files' section, specifically the 'Schematic Netlist (netlist)'.

Statistical Data from PVS:

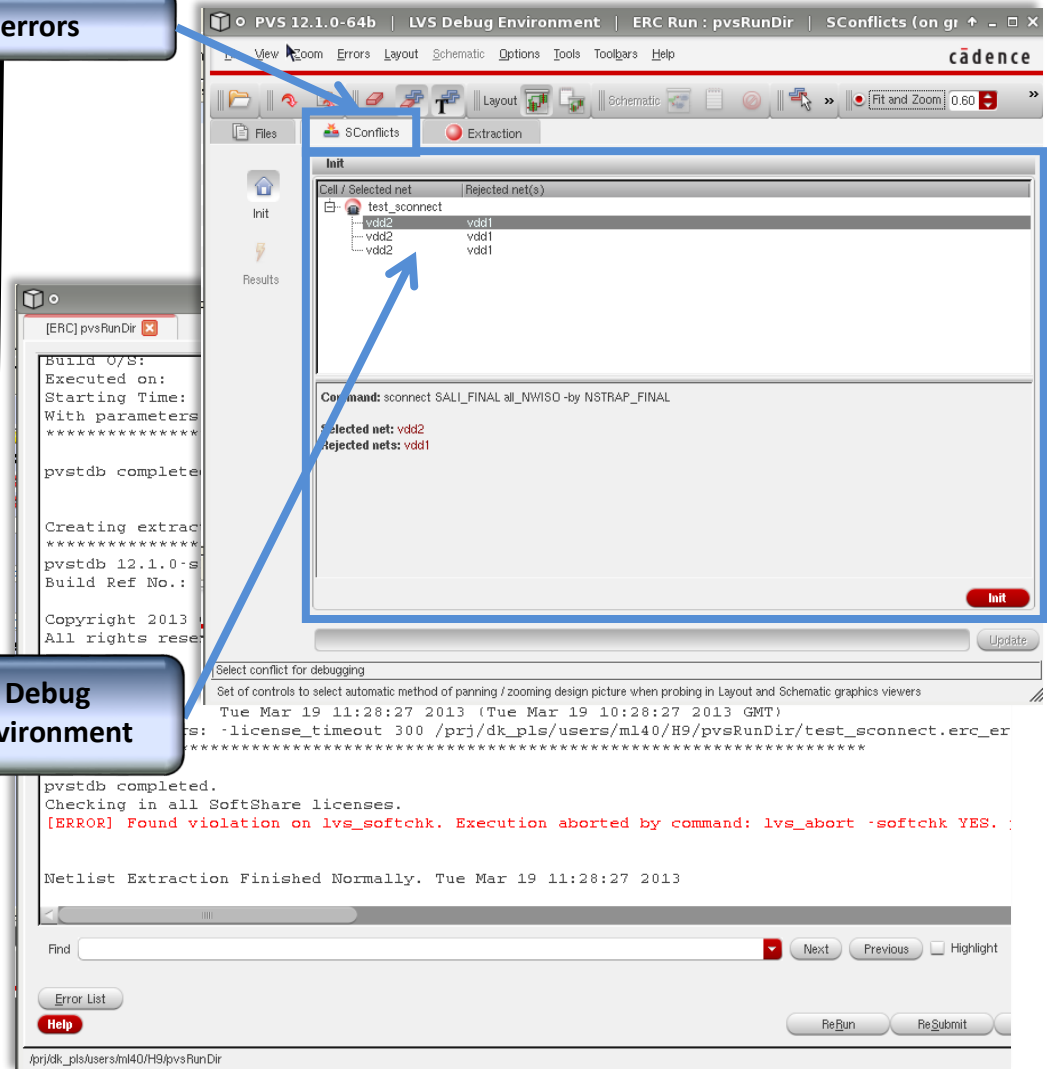
MATCH STATISTICS	
Statistic Descriptions	Count
all matched	1
all expanded	0
all not run	0
all which mismatch	0
all	1

11.9 - Softcheck errors

Calibre :



PVS :



11.10 - PVS-specific : Stamping Conflict Isolation tool

Requires additional “Phys_Ver_sys_int_Short” license :

Left Screenshot: Init Tab

Cell / Selected net	Rejected net(s)
test_sconnect	
vdd2	vdd1
vdd2	vdd1
vdd2	vdd1

Command: sconnect SALI_FINAL all_NWISO -by NSTRAP_FINAL
 Selected net: vdd2
 Rejected nets: vdd1

Right Screenshot: Results Tab

Net	Layer	Layer type
Output 1. vdd2 - vdd1 (5)		
vdd2	SALI_FINAL	upper
vdd2	NSTRAP_FINAL	contact
vdd2	all_NWISO	lower
vdd1	NSTRAP_FINAL	contact
vdd1	SALI_FINAL	upper

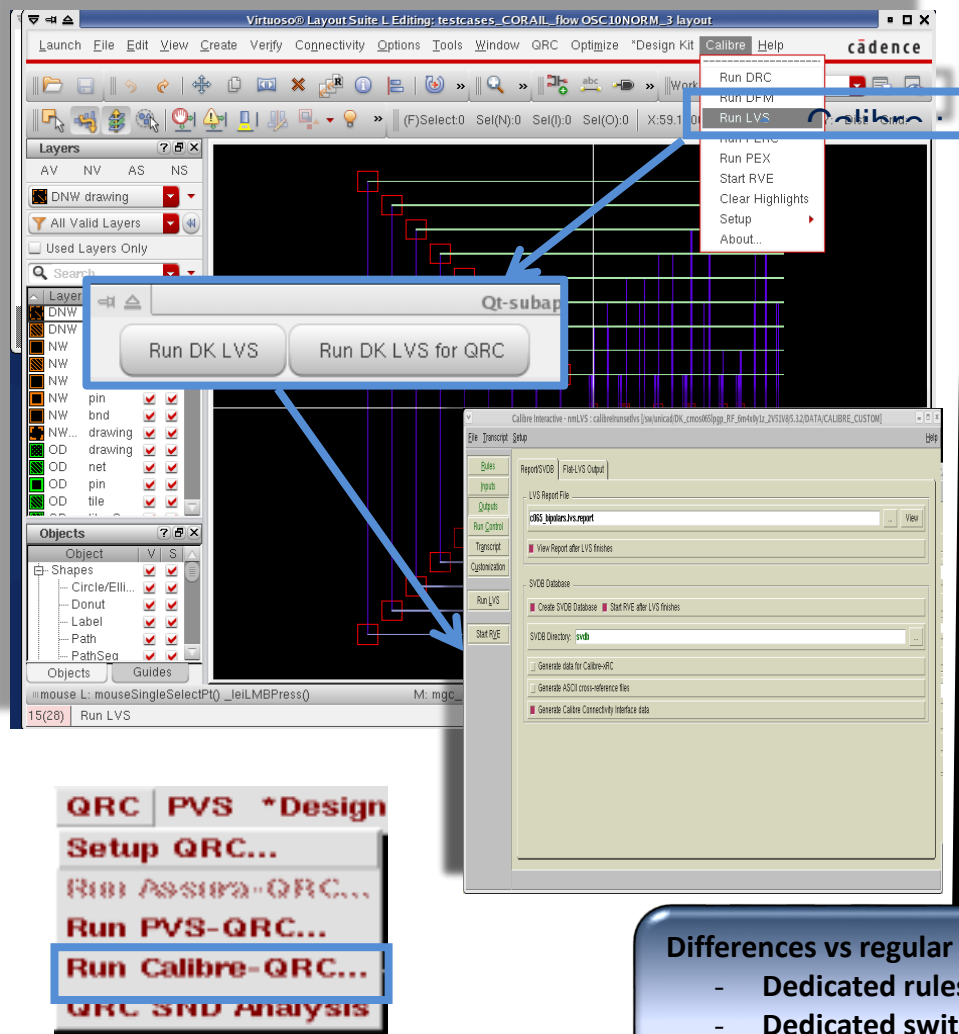
Command: sconnect SALI_FINAL all_NWISO -by NSTRAP_FINAL
 Selected net: vdd2
 Rejected nets: vdd1

Annotations:

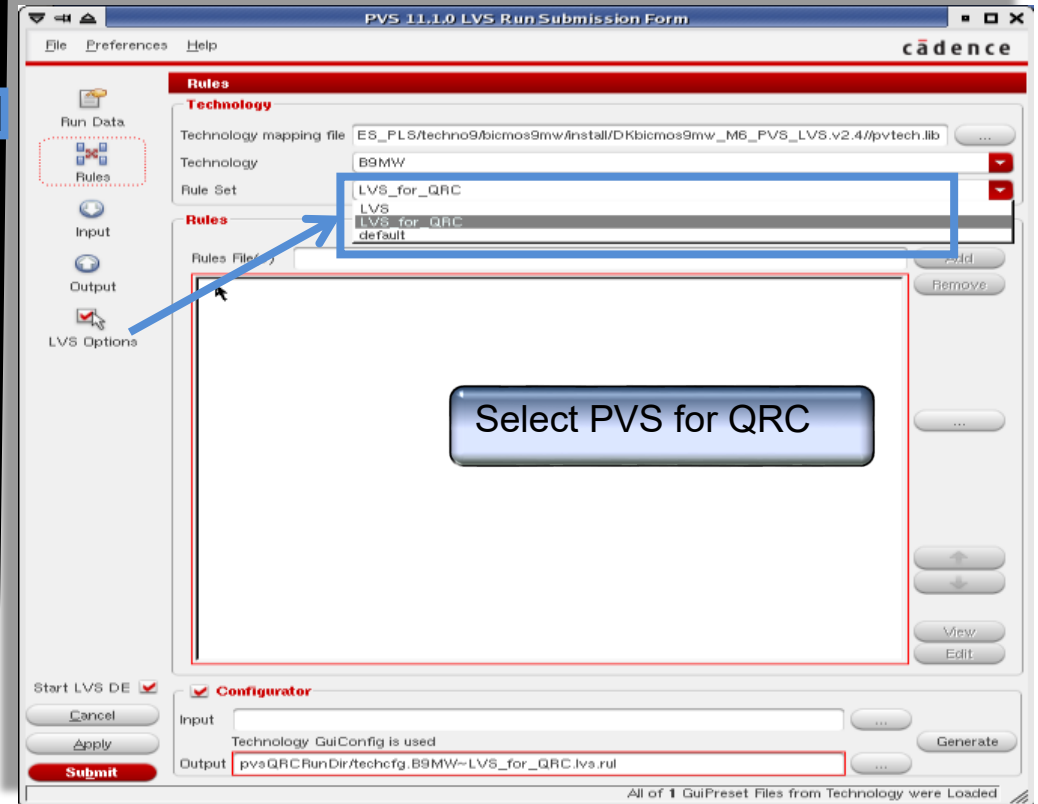
- Run “Init” from softcheck errors tab (points to the Init button in the left screenshot)
- Dedicated GUI showing the path and the layers involved in softcheck error (points to the Results table in the right screenshot)
- Highlight on layout selected shapes (points to the Results table in the right screenshot)

11.11 - LVS for parasitic extraction with QRC

Calibre :



PVS :



Differences vs regular LVS :

- Dedicated rules to split layers
- Dedicated switches (no ERC checks, SNA)
- Automatic database creation for QRC

