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C28SOI_SC_12_COREPBP4_LR Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 4 nm

Overview

- C28SOI_SC_12_COREPBP4_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

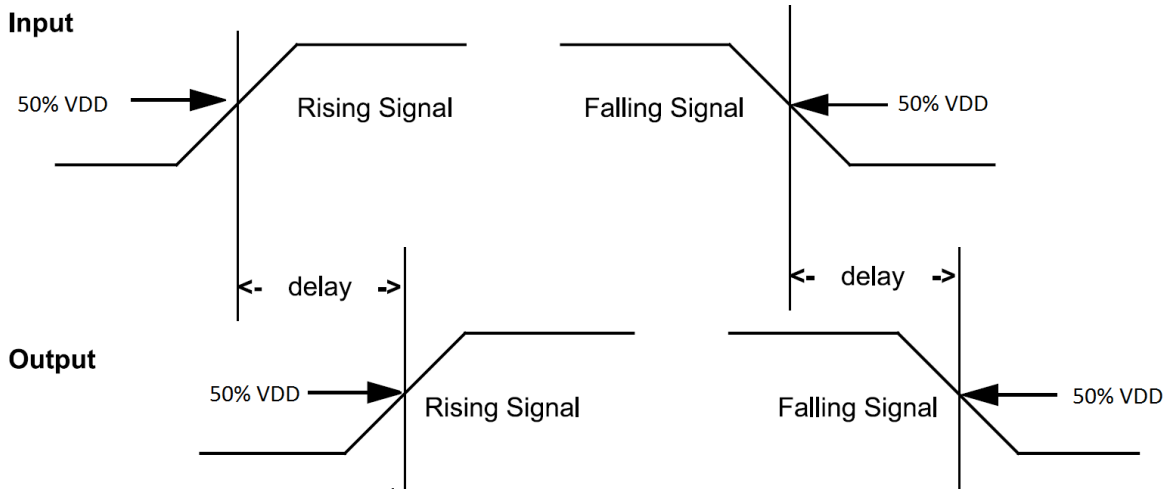


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

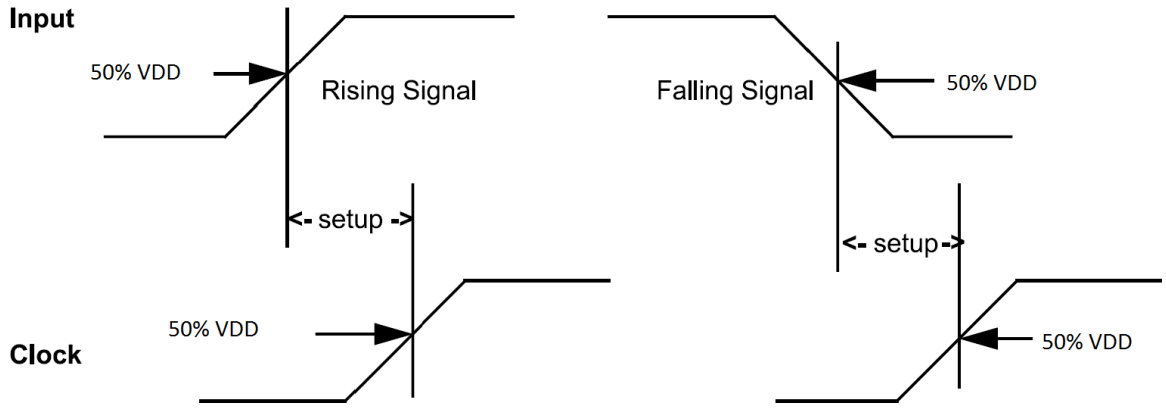


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

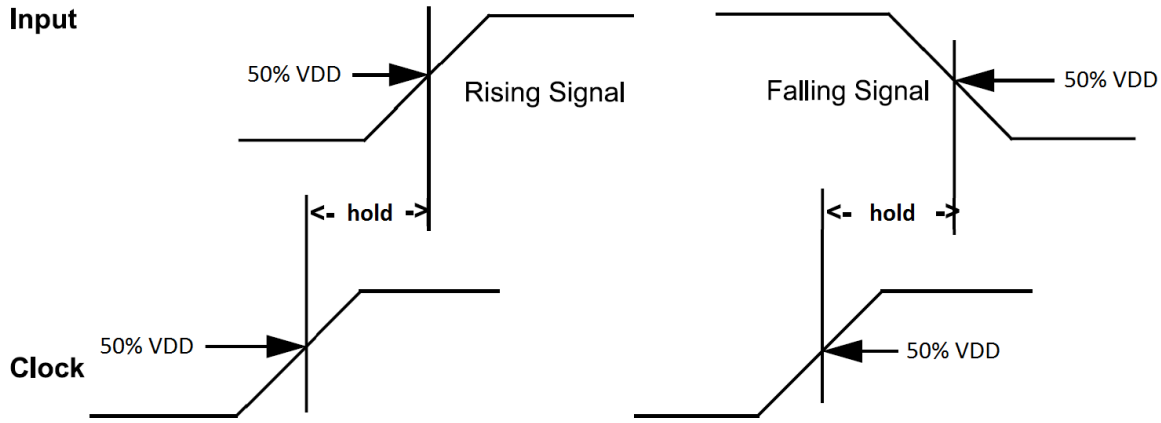


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

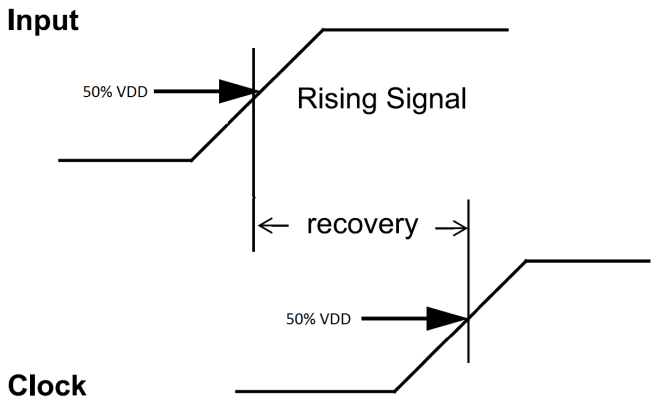


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

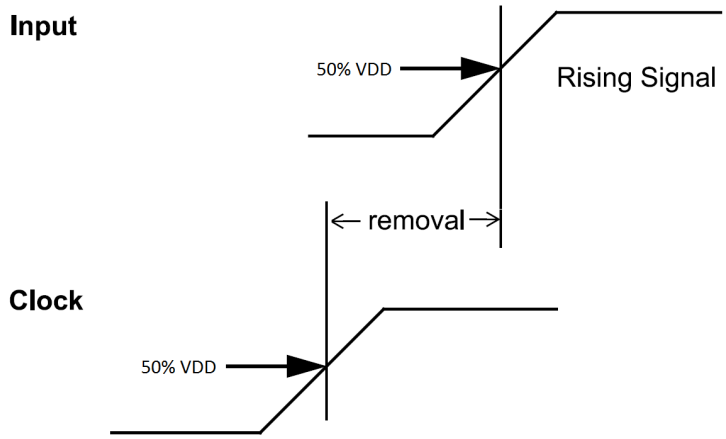


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

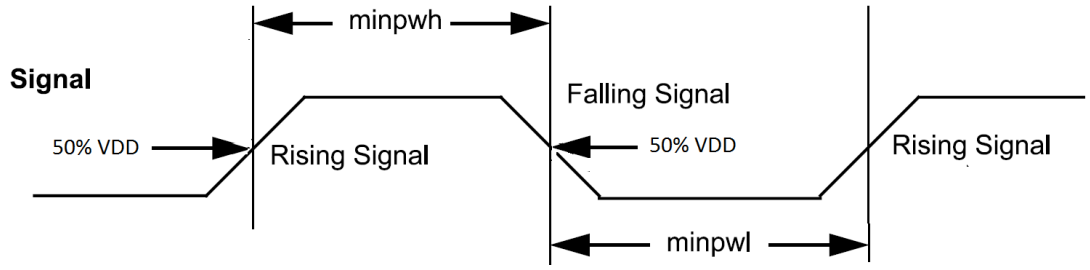


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

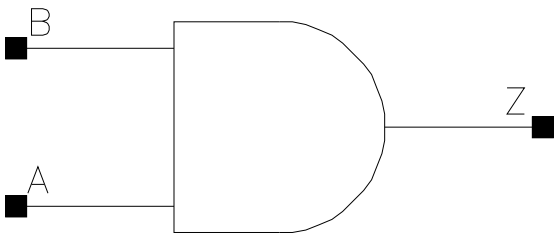
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X25_P4	1.200	1.088	1.3056
X33_P4	1.200	1.360	1.6320
X42_P4	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0008	0.0012	0.0018	0.0022
B	0.0007	0.0011	0.0017	0.0022
	X42_P4			
A	0.0021			
B	0.0022			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0254	0.0216	1.6310	0.8256
A to Z ↑	0.0187	0.0179	2.5895	1.2538
B to Z ↓	0.0241	0.0204	1.6306	0.8247
B to Z ↑	0.0201	0.0192	2.5860	1.2529
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0221	0.0216	0.5463	0.4071

A to Z ↑	0.0175	0.0181	0.8292	0.6270
B to Z ↓	0.0210	0.0199	0.5463	0.4060
B to Z ↑	0.0187	0.0191	0.8290	0.6260
	X42_P4		**X42_P4**	
A to Z ↓	0.0233		0.3304	
A to Z ↑	0.0199		0.5020	
B to Z ↓	0.0216		0.3298	
B to Z ↑	0.0209		0.5021	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	1.813e-05	1.145e-09
X16_P4	3.429e-05	1.310e-09
X25_P4	4.990e-05	1.807e-09
X33_P4	6.744e-05	2.139e-09
X42_P4	7.647e-05	2.304e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	1.809e-05	3.446e-05	5.323e-05	1.259e-04
B (output stable)	2.784e-05	4.956e-05	7.792e-05	2.896e-04
A to Z	3.349e-03	5.778e-03	8.842e-03	1.172e-02
B to Z	3.205e-03	5.546e-03	8.469e-03	1.093e-02
	X42_P4			
A (output stable)	1.269e-04			
B (output stable)	2.868e-04			
A to Z	1.417e-02			
B to Z	1.335e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

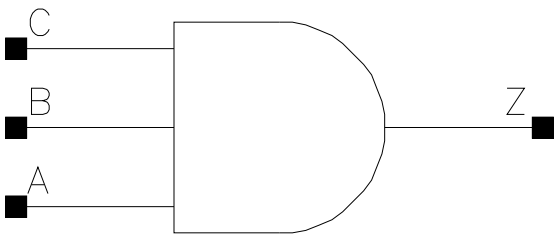
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	8.340e-08	5.895e-08	-7.700e-09	5.050e-08
B (output stable)	8.990e-08	7.316e-08	5.370e-08	3.590e-08
A to Z	5.206e-07	5.858e-07	1.393e-06	9.421e-07
B to Z	2.366e-07	6.111e-08	3.347e-07	1.250e-07
	X42_P4			
A (output stable)	5.550e-08			
B (output stable)	3.660e-08			
A to Z	2.015e-07			
B to Z	2.167e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X25_P4	1.200	1.360	1.6320
X33_P4	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0007	0.0011	0.0019	0.0023
B	0.0007	0.0011	0.0017	0.0021
C	0.0007	0.0011	0.0016	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0275	0.0236	1.6489	0.8045
A to Z ↑	0.0237	0.0226	2.6056	1.2434
B to Z ↓	0.0265	0.0225	1.6477	0.8040
B to Z ↑	0.0248	0.0237	2.6078	1.2439
C to Z ↓	0.0253	0.0213	1.6465	0.8026
C to Z ↑	0.0259	0.0244	2.6063	1.2429
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0235	0.0226	0.5521	0.4126

A to Z ↑	0.0219	0.0213	0.8502	0.6362
B to Z ↓	0.0225	0.0215	0.5521	0.4120
B to Z ↑	0.0232	0.0225	0.8494	0.6366
C to Z ↓	0.0212	0.0204	0.5515	0.4119
C to Z ↑	0.0240	0.0233	0.8489	0.6361

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	1.468e-05	1.310e-09
X17_P4	2.872e-05	1.476e-09
X25_P4	4.163e-05	2.139e-09
X33_P4	5.497e-05	2.304e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	2.146e-05	4.229e-05	5.797e-05	7.743e-05
B (output stable)	2.873e-05	5.706e-05	8.119e-05	1.123e-04
C (output stable)	5.836e-05	1.152e-04	1.691e-04	2.378e-04
A to Z	3.714e-03	6.679e-03	9.664e-03	1.253e-02
B to Z	3.556e-03	6.393e-03	9.222e-03	1.194e-02
C to Z	3.421e-03	6.128e-03	8.817e-03	1.139e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

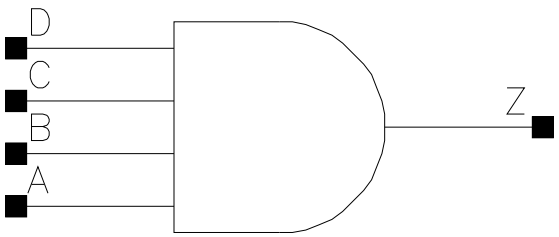
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	9.767e-08	6.911e-08	3.323e-08	1.100e-09
B (output stable)	1.055e-07	7.227e-08	5.403e-08	3.776e-08
C (output stable)	1.080e-07	8.351e-08	5.840e-08	3.708e-08
A to Z	1.197e-07	1.930e-08	5.562e-07	3.979e-07
B to Z	-1.627e-07	-8.680e-08	-1.799e-07	-2.288e-07
C to Z	-5.460e-08	2.290e-08	-2.044e-07	-1.548e-07

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X6_P4	1.200	1.088	1.3056
X20_P4	1.200	2.312	2.7744
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P4	X6_P4	X20_P4	X27_P4
A	0.0006	0.0008	0.0019	0.0021
B	0.0005	0.0008	0.0019	0.0021
C	0.0005	0.0008	0.0019	0.0021
D	0.0006	0.0008	0.0019	0.0022

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X6_P4	X4_P4	X6_P4
A to Z ↓	0.0285	0.0251	2.9771	1.9752
A to Z ↑	0.0256	0.0199	8.6916	4.7735
B to Z ↓	0.0276	0.0234	2.9759	1.9741
B to Z ↑	0.0273	0.0208	8.6979	4.7740
C to Z ↓	0.0293	0.0266	2.9488	1.9843
C to Z ↑	0.0256	0.0196	8.7042	4.7810

D to Z ↓	0.0283	0.0248	2.9447	1.9835
D to Z ↑	0.0277	0.0207	8.7081	4.7804
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0243	0.0229	0.5809	0.4120
A to Z ↑	0.0204	0.0233	1.5992	1.2177
B to Z ↓	0.0223	0.0211	0.5801	0.4110
B to Z ↑	0.0211	0.0243	1.5990	1.2173
C to Z ↓	0.0239	0.0222	0.5847	0.4131
C to Z ↑	0.0182	0.0203	1.5986	1.2168
D to Z ↓	0.0216	0.0205	0.5827	0.4124
D to Z ↑	0.0187	0.0213	1.5986	1.2165

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	1.289e-05	1.807e-09
X6_P4	2.582e-05	1.807e-09
X20_P4	7.002e-05	3.298e-09
X27_P4	8.017e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	5.768e-04	9.170e-04	2.665e-03	3.290e-03
B (output stable)	5.391e-04	8.406e-04	2.439e-03	3.049e-03
C (output stable)	5.488e-04	9.136e-04	2.348e-03	2.930e-03
D (output stable)	5.157e-04	8.349e-04	2.091e-03	2.671e-03
A to Z	2.364e-03	3.687e-03	1.098e-02	1.428e-02
B to Z	2.268e-03	3.490e-03	1.021e-02	1.349e-02
C to Z	2.325e-03	3.724e-03	9.561e-03	1.212e-02
D to Z	2.228e-03	3.520e-03	8.747e-03	1.133e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

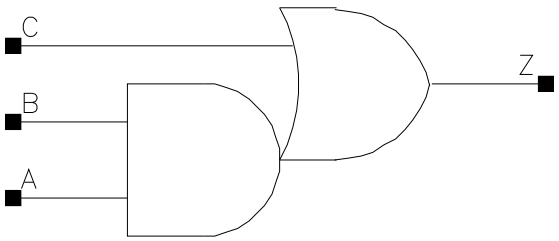
Pin Cycle (vdds)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	3.118e-07	3.570e-07	1.254e-06	2.030e-06
B (output stable)	3.032e-07	4.687e-07	1.351e-06	1.662e-06
C (output stable)	2.100e-06	2.189e-06	1.742e-05	3.836e-05
D (output stable)	2.183e-06	2.070e-06	1.706e-05	3.862e-05
A to Z	6.729e-07	3.162e-07	5.880e-06	7.087e-06
B to Z	2.824e-07	1.833e-06	5.072e-06	4.928e-06
C to Z	-1.892e-07	1.189e-07	5.615e-07	-9.265e-07
D to Z	-8.665e-08	-2.377e-07	-8.184e-07	-1.511e-06

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0010	0.0022
B	0.0007	0.0011	0.0021
C	0.0008	0.0012	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0323	0.0296	1.6749	0.8193
A to Z ↑	0.0194	0.0176	2.5143	1.2348
B to Z ↓	0.0299	0.0274	1.6693	0.8156
B to Z ↑	0.0211	0.0193	2.5126	1.2348
C to Z ↓	0.0307	0.0281	1.6662	0.8154
C to Z ↑	0.0186	0.0177	2.4997	1.2289
	X33_P4		**X33_P4**	
A to Z ↓	0.0296		0.4160	
A to Z ↑	0.0181		0.6230	

B to Z ↓	0.0277		0.4152	
B to Z ↑	0.0194		0.6228	
C to Z ↓	0.0284		0.4144	
C to Z ↑	0.0175		0.6196	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	2.464e-05	1.310e-09
X17_P4	4.590e-05	1.476e-09
X33_P4	9.123e-05	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	3.748e-05	6.709e-05	1.585e-04
B (output stable)	4.120e-05	7.436e-05	1.950e-04
C (output stable)	7.742e-05	1.300e-04	2.973e-04
A to Z	3.519e-03	6.276e-03	1.249e-02
B to Z	3.353e-03	5.969e-03	1.179e-02
C to Z	3.774e-03	6.683e-03	1.334e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

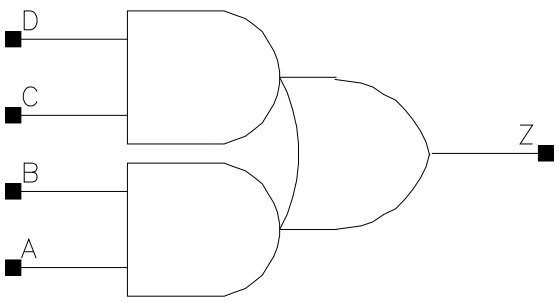
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	1.371e-05	1.757e-05	3.752e-05
B (output stable)	1.400e-05	1.871e-05	3.823e-05
C (output stable)	-4.008e-08	5.156e-07	6.702e-07
A to Z	7.740e-08	4.838e-07	7.876e-07
B to Z	6.100e-09	5.796e-08	1.172e-07
C to Z	4.348e-07	7.703e-07	2.251e-06

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0010	0.0021
B	0.0008	0.0011	0.0020
C	0.0007	0.0010	0.0022
D	0.0007	0.0011	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0358	0.0318	1.6229	0.8160
A to Z ↑	0.0251	0.0231	2.4813	1.2354
B to Z ↓	0.0333	0.0295	1.6136	0.8128
B to Z ↑	0.0267	0.0250	2.4804	1.2347

C to Z ↓	0.0332	0.0299	1.6162	0.8138
C to Z ↑	0.0214	0.0196	2.4734	1.2304
D to Z ↓	0.0317	0.0284	1.6116	0.8116
D to Z ↑	0.0233	0.0213	2.4741	1.2300
	X33_P4		**X33_P4**	
A to Z ↓	0.0306		0.4164	
A to Z ↑	0.0213		0.6248	
B to Z ↓	0.0290		0.4159	
B to Z ↑	0.0232		0.6246	
C to Z ↓	0.0287		0.4155	
C to Z ↑	0.0182		0.6228	
D to Z ↓	0.0271		0.4146	
D to Z ↑	0.0197		0.6231	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	2.592e-05	1.642e-09
X17_P4	4.824e-05	1.807e-09
X33_P4	8.964e-05	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	4.680e-05	6.726e-05	9.809e-05
B (output stable)	1.413e-04	1.661e-04	1.135e-04
C (output stable)	4.413e-05	8.026e-05	1.725e-04
D (output stable)	4.826e-05	8.929e-05	1.969e-04
A to Z	4.566e-03	7.768e-03	1.457e-02
B to Z	4.245e-03	7.298e-03	1.394e-02
C to Z	3.945e-03	6.771e-03	1.258e-02
D to Z	3.795e-03	6.501e-03	1.202e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

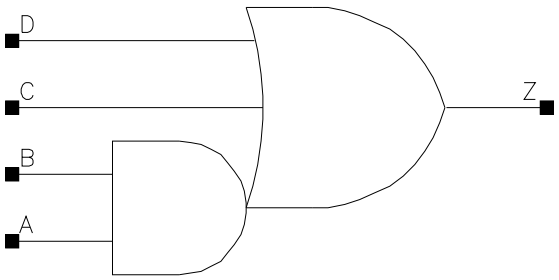
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	1.218e-07	1.955e-07	2.891e-07
B (output stable)	-1.712e-07	1.613e-07	2.709e-07
C (output stable)	5.845e-06	6.917e-06	2.148e-05
D (output stable)	5.558e-06	6.778e-06	2.208e-05
A to Z	1.916e-07	2.243e-07	9.260e-07
B to Z	2.451e-07	6.037e-07	1.452e-06
C to Z	8.913e-08	1.394e-07	4.134e-07
D to Z	5.973e-08	1.242e-07	2.001e-08

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	0.952	1.1424
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0011	0.0020
B	0.0007	0.0011	0.0021
C	0.0007	0.0011	0.0020
D	0.0007	0.0011	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0417	0.0373	1.7497	0.8627
A to Z ↑	0.0210	0.0193	2.5042	1.2807
B to Z ↓	0.0399	0.0349	1.7433	0.8594
B to Z ↑	0.0227	0.0205	2.5037	1.2822
C to Z ↓	0.0424	0.0379	1.7420	0.8592
C to Z ↑	0.0202	0.0190	2.4888	1.2749

D to Z ↓	0.0426	0.0384	1.7418	0.8603
D to Z ↑	0.0198	0.0188	2.4893	1.2746
	X33_P4		**X33_P4**	
A to Z ↓	0.0378		0.4323	
A to Z ↑	0.0192		0.6237	
B to Z ↓	0.0343		0.4294	
B to Z ↑	0.0202		0.6231	
C to Z ↓	0.0390		0.4301	
C to Z ↑	0.0186		0.6205	
D to Z ↓	0.0385		0.4304	
D to Z ↑	0.0179		0.6197	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	2.492e-05	1.476e-09
X17_P4	4.732e-05	1.642e-09
X33_P4	9.570e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	3.258e-05	6.443e-05	1.646e-04
B (output stable)	3.340e-05	6.452e-05	1.907e-04
C (output stable)	4.371e-05	8.046e-05	2.209e-04
D (output stable)	3.887e-05	7.709e-05	2.181e-04
A to Z	3.972e-03	6.858e-03	1.377e-02
B to Z	3.821e-03	6.536e-03	1.279e-02
C to Z	4.434e-03	7.665e-03	1.558e-02
D to Z	4.214e-03	7.293e-03	1.453e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

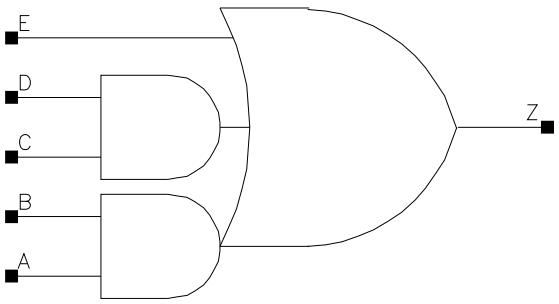
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	2.482e-05	3.966e-05	8.120e-05
B (output stable)	2.452e-05	3.813e-05	8.113e-05
C (output stable)	-6.675e-07	-5.340e-07	-1.949e-06
D (output stable)	9.041e-06	1.445e-05	5.731e-05
A to Z	-3.610e-08	-4.292e-08	-9.085e-08
B to Z	-2.500e-09	-2.269e-07	-3.411e-07
C to Z	7.517e-07	1.122e-06	4.007e-06
D to Z	6.714e-07	8.113e-07	1.707e-06

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.088	1.3056
X17_P4	1.200	1.224	1.4688
X33_P4	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0010	0.0021
B	0.0007	0.0010	0.0020
C	0.0008	0.0013	0.0021
D	0.0007	0.0011	0.0021
E	0.0007	0.0011	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0497	0.0438	1.6737	0.8411
A to Z ↑	0.0266	0.0235	2.4586	1.2411

B to Z ↓	0.0479	0.0417	1.6674	0.8383
B to Z ↑	0.0289	0.0254	2.4572	1.2403
C to Z ↓	0.0431	0.0391	1.6672	0.8384
C to Z ↑	0.0224	0.0195	2.4398	1.2334
D to Z ↓	0.0402	0.0358	1.6579	0.8333
D to Z ↑	0.0240	0.0210	2.4386	1.2329
E to Z ↓	0.0441	0.0389	1.6579	0.8344
E to Z ↑	0.0212	0.0188	2.4226	1.2267
	X33_P4		**X33_P4**	
A to Z ↓	0.0430		0.4323	
A to Z ↑	0.0241		0.6268	
B to Z ↓	0.0405		0.4309	
B to Z ↑	0.0261		0.6262	
C to Z ↓	0.0379		0.4309	
C to Z ↑	0.0196		0.6230	
D to Z ↓	0.0350		0.4286	
D to Z ↑	0.0211		0.6221	
E to Z ↓	0.0382		0.4292	
E to Z ↑	0.0189		0.6190	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	2.913e-05	1.807e-09
X17_P4	5.408e-05	1.973e-09
X33_P4	9.911e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.687e-05	4.444e-05	9.995e-05
B (output stable)	3.321e-05	4.657e-05	1.138e-04
C (output stable)	5.299e-05	8.161e-05	1.953e-04
D (output stable)	5.885e-05	9.313e-05	2.172e-04
E (output stable)	1.048e-04	1.623e-04	3.663e-04
A to Z	5.333e-03	8.864e-03	1.734e-02
B to Z	5.175e-03	8.521e-03	1.649e-02
C to Z	4.298e-03	7.301e-03	1.411e-02
D to Z	4.111e-03	6.935e-03	1.332e-02
E to Z	4.602e-03	7.693e-03	1.490e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	-1.714e-07	8.163e-08	-4.395e-08
B (output stable)	-1.895e-07	3.900e-08	-1.041e-07
C (output stable)	1.862e-05	2.295e-05	5.751e-05
D (output stable)	2.041e-05	2.620e-05	5.785e-05
E (output stable)	1.778e-05	1.753e-05	4.079e-05
A to Z	1.152e-06	1.230e-06	2.739e-06
B to Z	1.043e-06	1.259e-06	2.829e-06
C to Z	-8.637e-08	-4.852e-08	-5.504e-07
D to Z	-1.091e-07	-5.817e-08	-4.076e-07

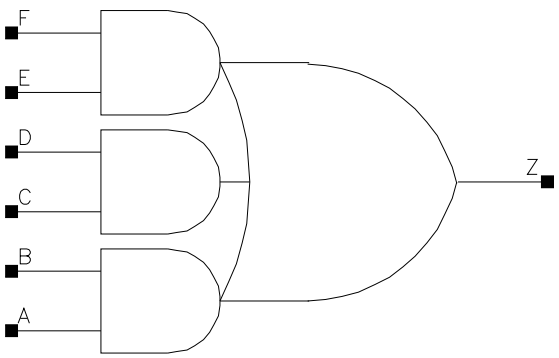
E to Z	4.594e-07	7.554e-07	1.332e-06

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.360	1.6320
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
A	0.0007	0.0008	0.0010	0.0021

B	0.0007	0.0008	0.0014	0.0020
C	0.0007	0.0008	0.0010	0.0021
D	0.0007	0.0008	0.0010	0.0020
E	0.0007	0.0008	0.0011	0.0022
F	0.0007	0.0008	0.0011	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0498	0.0476	3.1099	1.6785
A to Z ↑	0.0279	0.0273	4.7405	2.5107
B to Z ↓	0.0460	0.0443	3.0851	1.6662
B to Z ↑	0.0293	0.0291	4.7350	2.5101
C to Z ↓	0.0457	0.0441	3.0987	1.6733
C to Z ↑	0.0253	0.0248	4.7089	2.4962
D to Z ↓	0.0436	0.0421	3.0841	1.6659
D to Z ↑	0.0274	0.0270	4.7086	2.4961
E to Z ↓	0.0385	0.0381	3.0819	1.6659
E to Z ↑	0.0211	0.0208	4.6866	2.4854
F to Z ↓	0.0360	0.0357	3.0674	1.6584
F to Z ↑	0.0226	0.0225	4.6864	2.4840
	X17_P4	X33_P4	X17_P4	X33_P4
A to Z ↓	0.0465	0.0448	0.8453	0.4310
A to Z ↑	0.0258	0.0259	1.2447	0.6289
B to Z ↓	0.0440	0.0424	0.8390	0.4296
B to Z ↑	0.0280	0.0279	1.2446	0.6286
C to Z ↓	0.0437	0.0419	0.8429	0.4307
C to Z ↑	0.0235	0.0239	1.2382	0.6256
D to Z ↓	0.0413	0.0398	0.8389	0.4293
D to Z ↑	0.0256	0.0258	1.2380	0.6256
E to Z ↓	0.0378	0.0381	0.8390	0.4293
E to Z ↑	0.0197	0.0205	1.2337	0.6241
F to Z ↓	0.0355	0.0354	0.8350	0.4273
F to Z ↑	0.0214	0.0223	1.2330	0.6240

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	2.338e-05	2.139e-09
X8_P4	3.426e-05	2.139e-09
X17_P4	5.680e-05	2.304e-09
X33_P4	1.021e-04	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	5.032e-05	5.893e-05	7.490e-05	1.398e-04
B (output stable)	1.150e-04	1.246e-04	1.242e-04	1.684e-04
C (output stable)	4.340e-05	5.385e-05	7.276e-05	1.488e-04
D (output stable)	4.802e-05	5.980e-05	7.907e-05	1.889e-04
E (output stable)	8.345e-05	1.021e-04	1.356e-04	2.281e-04
F (output stable)	8.568e-05	1.038e-04	1.426e-04	2.609e-04

A to Z	4.586e-03	6.239e-03	9.836e-03	1.864e-02
B to Z	4.245e-03	5.827e-03	9.277e-03	1.777e-02
C to Z	3.916e-03	5.430e-03	8.742e-03	1.658e-02
D to Z	3.751e-03	5.218e-03	8.403e-03	1.584e-02
E to Z	3.193e-03	4.606e-03	7.544e-03	1.473e-02
F to Z	3.033e-03	4.397e-03	7.222e-03	1.398e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

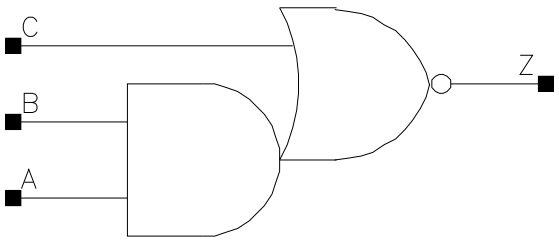
Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	-4.039e-07	-2.825e-07	-1.774e-07	-2.923e-07
B (output stable)	-6.080e-07	-3.161e-07	1.150e-08	-3.444e-07
C (output stable)	6.054e-06	6.763e-06	8.268e-06	2.151e-05
D (output stable)	6.362e-06	7.128e-06	8.136e-06	2.170e-05
E (output stable)	2.690e-05	3.123e-05	3.867e-05	6.049e-05
F (output stable)	2.642e-05	3.030e-05	3.858e-05	6.064e-05
A to Z	1.409e-06	1.798e-06	1.929e-06	3.550e-06
B to Z	1.681e-06	2.067e-06	2.232e-06	4.189e-06
C to Z	6.200e-07	7.413e-07	5.799e-07	6.411e-08
D to Z	8.008e-07	8.604e-07	8.134e-07	6.548e-07
E to Z	-1.490e-08	-4.633e-08	-3.498e-08	-7.229e-07
F to Z	-1.634e-07	-1.199e-07	-2.281e-07	-5.404e-07

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008
X44_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X33_P4	X44_P4
A	0.0009	0.0026	0.0053	0.0072
B	0.0008	0.0025	0.0050	0.0069
C	0.0009	0.0028	0.0056	0.0073

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0066	0.0068	2.7673	0.9393
A to Z ↑	0.0159	0.0163	4.8976	1.6432
B to Z ↓	0.0069	0.0071	2.8040	0.9550
B to Z ↑	0.0131	0.0131	4.8196	1.6431
C to Z ↓	0.0071	0.0074	1.6948	0.5810
C to Z ↑	0.0153	0.0154	4.4624	1.5121
	X33_P4	**X44_P4**	**X33_P4**	**X44_P4**
A to Z ↓	0.0070	0.0069	0.4793	0.3634

A to Z ↑	0.0162	0.0163	0.8237	0.6259
B to Z ↓	0.0071	0.0071	0.4872	0.3696
B to Z ↑	0.0130	0.0130	0.8219	0.6224
C to Z ↓	0.0088	0.0089	0.3448	0.2674
C to Z ↑	0.0156	0.0155	0.7566	0.5739

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P4	1.785e-05	1.145e-09
X17_P4	4.835e-05	2.139e-09
X33_P4	8.952e-05	3.629e-09
X44_P4	1.194e-04	4.623e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	6.902e-05	2.089e-04	4.566e-04	5.977e-04
B (output stable)	7.452e-05	2.644e-04	5.618e-04	7.306e-04
C (output stable)	1.280e-04	3.964e-04	8.559e-04	1.122e-03
A to Z	1.724e-03	5.379e-03	1.076e-02	1.422e-02
B to Z	1.482e-03	4.356e-03	8.706e-03	1.148e-02
C to Z	2.297e-03	6.881e-03	1.381e-02	1.818e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

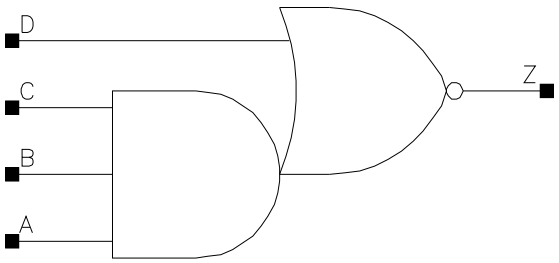
Pin Cycle (vdds)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	1.718e-05	3.895e-05	9.542e-05	1.186e-04
B (output stable)	1.724e-05	4.011e-05	9.528e-05	1.200e-04
C (output stable)	4.313e-07	9.238e-07	1.083e-06	1.937e-06
A to Z	7.981e-07	1.237e-06	3.908e-06	5.198e-06
B to Z	9.317e-07	2.762e-06	4.786e-06	6.704e-06
C to Z	2.115e-06	5.485e-06	4.967e-06	9.780e-06

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X29_P4	1.200	3.536	4.2432
X38_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X29_P4	X38_P4
A	0.0009	0.0054	0.0071
B	0.0008	0.0052	0.0069
C	0.0008	0.0050	0.0067
D	0.0010	0.0056	0.0069

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X29_P4	X5_P4	X29_P4
A to Z ↓	0.0102	0.0109	3.8566	0.6719
A to Z ↑	0.0199	0.0200	4.8998	0.8149
B to Z ↓	0.0109	0.0111	3.8738	0.6759
B to Z ↑	0.0178	0.0177	4.9020	0.8218
C to Z ↓	0.0109	0.0109	3.8970	0.6807
C to Z ↑	0.0153	0.0148	4.8327	0.8279
D to Z ↓	0.0091	0.0109	1.7306	0.3469

D to Z ↑	0.0179	0.0182	4.1697	0.7023
	X38_P4		**X38_P4**	
A to Z ↓	0.0107		0.5206	
A to Z ↑	0.0197		0.6148	
B to Z ↓	0.0110		0.5238	
B to Z ↑	0.0174		0.6216	
C to Z ↓	0.0108		0.5276	
C to Z ↑	0.0145		0.6288	
D to Z ↓	0.0116		0.2874	
D to Z ↑	0.0179		0.5309	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P4	1.798e-05	1.310e-09
X29_P4	8.928e-05	4.789e-09
X38_P4	1.128e-04	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P4	X29_P4	X38_P4
A (output stable)	4.232e-05	3.332e-04	4.253e-04
B (output stable)	4.817e-05	4.141e-04	5.334e-04
C (output stable)	7.306e-05	7.715e-04	9.648e-04
D (output stable)	1.601e-04	1.159e-03	1.527e-03
A to Z	2.341e-03	1.459e-02	1.874e-02
B to Z	2.057e-03	1.225e-02	1.580e-02
C to Z	1.803e-03	1.017e-02	1.303e-02
D to Z	2.906e-03	1.757e-02	2.261e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

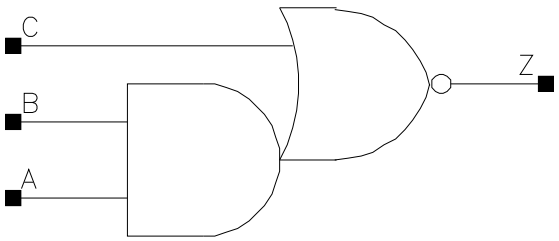
Pin Cycle (vdds)	X5_P4	X29_P4	X38_P4
A (output stable)	7.586e-06	6.801e-05	8.629e-05
B (output stable)	7.982e-06	6.777e-05	8.553e-05
C (output stable)	7.773e-06	6.627e-05	8.487e-05
D (output stable)	2.060e-07	-4.860e-07	-7.981e-07
A to Z	6.790e-07	2.827e-06	4.013e-06
B to Z	3.620e-07	1.495e-06	1.892e-06
C to Z	4.000e-07	-2.768e-06	-5.740e-07
D to Z	8.547e-07	6.120e-06	3.950e-06

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X11_P4	1.200	1.088	1.3056
X16_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X11_P4	X16_P4	X23_P4
A	0.0009	0.0019	0.0028	0.0038
B	0.0010	0.0018	0.0027	0.0036
C	0.0010	0.0018	0.0026	0.0037
	X46_P4			
A	0.0073			
B	0.0071			
C	0.0072			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X11_P4	X6_P4	X11_P4
A to Z ↓	0.0082	0.0090	2.6715	1.3616
A to Z ↑	0.0165	0.0175	4.8854	2.3912
B to Z ↓	0.0091	0.0094	2.7042	1.3802

B to Z ↑	0.0143	0.0147	4.8206	2.3993
C to Z ↓	0.0041	0.0047	1.7483	1.0218
C to Z ↑	0.0131	0.0127	4.4880	2.2168
	X16_P4	**X23_P4**	**X16_P4**	**X23_P4**
A to Z ↓	0.0085	0.0088	0.9386	0.7077
A to Z ↑	0.0164	0.0167	1.6108	1.2207
B to Z ↓	0.0093	0.0093	0.9528	0.7173
B to Z ↑	0.0136	0.0139	1.6099	1.2253
C to Z ↓	0.0049	0.0039	0.7084	0.4494
C to Z ↑	0.0122	0.0128	1.4917	1.1308
	X46_P4		**X46_P4**	
A to Z ↓	0.0084		0.3637	
A to Z ↑	0.0162		0.6351	
B to Z ↓	0.0090		0.3689	
B to Z ↑	0.0132		0.6333	
C to Z ↓	0.0042		0.2298	
C to Z ↑	0.0128		0.5867	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P4	1.775e-05	1.145e-09
X11_P4	3.482e-05	1.807e-09
X16_P4	4.644e-05	2.139e-09
X23_P4	6.703e-05	2.801e-09
X46_P4	1.272e-04	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	3.783e-05	1.039e-04	1.370e-04	1.937e-04
B (output stable)	4.479e-05	1.559e-04	1.774e-04	2.663e-04
C (output stable)	2.694e-04	6.095e-04	8.104e-04	1.113e-03
A to Z	2.259e-03	4.917e-03	6.791e-03	9.232e-03
B to Z	1.989e-03	4.147e-03	5.689e-03	7.710e-03
C to Z	1.512e-03	3.026e-03	4.251e-03	5.975e-03
	X46_P4			
A (output stable)	3.528e-04			
B (output stable)	4.687e-04			
C (output stable)	1.931e-03			
A to Z	1.723e-02			
B to Z	1.435e-02			
C to Z	1.144e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	2.421e-07	4.288e-07	4.688e-07	5.153e-07
B (output stable)	2.148e-07	4.078e-07	3.976e-07	5.039e-07
C (output stable)	2.907e-05	9.574e-05	7.691e-05	1.109e-04
A to Z	2.450e-06	4.978e-06	5.978e-06	6.492e-06
B to Z	1.234e-06	2.759e-06	3.808e-06	5.158e-06
C to Z	3.803e-07	3.340e-07	4.943e-07	1.331e-06

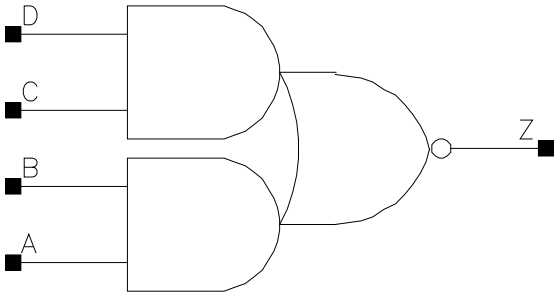
	X46_P4			
A (output stable)	8.339e-07			
B (output stable)	6.970e-07			
C (output stable)	1.461e-04			
A to Z	1.168e-05			
B to Z	9.510e-06			
C to Z	1.952e-06			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P4	X10_P4	X16_P4	X21_P4
A	0.0008	0.0020	0.0029	0.0037
B	0.0008	0.0018	0.0027	0.0036
C	0.0007	0.0019	0.0027	0.0036
D	0.0008	0.0017	0.0026	0.0034
	X42_P4			
A	0.0074			
B	0.0072			
C	0.0072			
D	0.0070			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X10_P4**	**X4_P4**	**X10_P4**
A to Z ↓	0.0096	0.0096	3.2910	1.3070
A to Z ↑	0.0215	0.0184	6.5924	2.2064
B to Z ↓	0.0107	0.0109	3.3358	1.3253
B to Z ↑	0.0191	0.0167	6.5705	2.2614
C to Z ↓	0.0067	0.0064	3.3753	1.3163
C to Z ↑	0.0180	0.0159	6.5877	2.2189
D to Z ↓	0.0072	0.0070	3.4306	1.3395
D to Z ↑	0.0155	0.0137	6.5669	2.2527
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0106	0.0105	0.9422	0.7099
A to Z ↑	0.0192	0.0191	1.4888	1.1524
B to Z ↓	0.0117	0.0113	0.9543	0.7190
B to Z ↑	0.0167	0.0165	1.4882	1.1542
C to Z ↓	0.0070	0.0071	0.9426	0.7112
C to Z ↑	0.0164	0.0167	1.4892	1.1510
D to Z ↓	0.0076	0.0073	0.9581	0.7229
D to Z ↑	0.0136	0.0137	1.4908	1.1528
	X42_P4		**X42_P4**	
A to Z ↓	0.0111		0.3692	
A to Z ↑	0.0194		0.5793	
B to Z ↓	0.0118		0.3739	
B to Z ↑	0.0166		0.5767	
C to Z ↓	0.0076		0.3651	
C to Z ↑	0.0169		0.5797	
D to Z ↓	0.0079		0.3712	
D to Z ↑	0.0139		0.5777	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	1.654e-05	1.310e-09
X10_P4	4.276e-05	2.139e-09
X16_P4	5.788e-05	2.635e-09
X21_P4	7.839e-05	3.464e-09
X42_P4	1.511e-04	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	3.946e-05	9.412e-05	1.835e-04	2.457e-04
B (output stable)	4.580e-05	1.139e-04	2.773e-04	3.922e-04
C (output stable)	6.384e-05	1.677e-04	2.876e-04	3.816e-04
D (output stable)	7.283e-05	1.920e-04	3.850e-04	5.251e-04
A to Z	2.256e-03	5.610e-03	8.704e-03	1.129e-02
B to Z	2.003e-03	5.011e-03	7.556e-03	9.765e-03
C to Z	1.479e-03	3.795e-03	5.841e-03	7.762e-03
D to Z	1.270e-03	3.267e-03	4.815e-03	6.366e-03
	X42_P4			
A (output stable)	4.702e-04			
B (output stable)	7.123e-04			
C (output stable)	7.331e-04			
D (output stable)	9.704e-04			

A to Z	2.227e-02			
B to Z	1.923e-02			
C to Z	1.528e-02			
D to Z	1.258e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

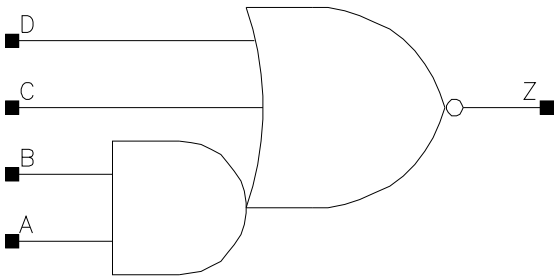
Pin Cycle (vdds)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	1.225e-07	2.283e-07	3.216e-07	4.263e-07
B (output stable)	1.254e-07	2.401e-07	2.712e-07	3.002e-07
C (output stable)	1.405e-05	2.196e-05	3.375e-05	3.827e-05
D (output stable)	1.437e-05	2.244e-05	3.428e-05	3.828e-05
A to Z	1.334e-06	3.265e-06	4.678e-06	6.070e-06
B to Z	1.001e-06	1.843e-06	2.632e-06	3.863e-06
C to Z	3.988e-07	7.057e-07	9.563e-07	1.041e-06
D to Z	3.872e-07	1.809e-06	1.719e-06	2.738e-06
	X42_P4			
A (output stable)	8.060e-07			
B (output stable)	6.204e-07			
C (output stable)	6.885e-05			
D (output stable)	6.921e-05			
A to Z	8.000e-06			
B to Z	6.040e-06			
C to Z	1.552e-06			
D to Z	3.346e-06			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X35_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P4	X35_P4
A	0.0009	0.0068
B	0.0009	0.0065
C	0.0009	0.0066
D	0.0009	0.0062

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X35_P4	X5_P4	X35_P4
A to Z ↓	0.0079	0.0083	2.7964	0.4136
A to Z ↑	0.0208	0.0197	7.2246	0.9295
B to Z ↓	0.0085	0.0087	2.8393	0.4212
B to Z ↑	0.0176	0.0160	7.1697	0.9285
C to Z ↓	0.0091	0.0128	1.8015	0.3440
C to Z ↑	0.0221	0.0218	6.8147	0.8785
D to Z ↓	0.0086	0.0116	1.8169	0.3439

D to Z ↑	0.0220	0.0208	6.8279	0.8815

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P4	1.435e-05	1.310e-09
X35_P4	8.613e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P4	X35_P4
A (output stable)	6.243e-05	5.478e-04
B (output stable)	6.418e-05	5.975e-04
C (output stable)	7.681e-05	8.233e-04
D (output stable)	7.421e-05	7.254e-04
A to Z	1.956e-03	1.431e-02
B to Z	1.688e-03	1.176e-02
C to Z	2.923e-03	2.245e-02
D to Z	2.510e-03	1.831e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

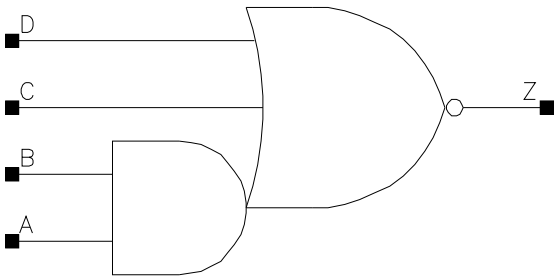
Pin Cycle (vdds)	X5_P4	X35_P4
A (output stable)	3.772e-05	2.377e-04
B (output stable)	3.699e-05	2.387e-04
C (output stable)	-5.545e-07	-5.493e-06
D (output stable)	1.394e-05	1.444e-04
A to Z	3.026e-07	2.582e-06
B to Z	1.098e-07	1.627e-06
C to Z	1.241e-06	1.106e-05
D to Z	8.407e-07	2.683e-06

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X17_P4	1.200	2.448	2.9376
X34_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P4	X17_P4	X34_P4
A	0.0009	0.0037	0.0075
B	0.0009	0.0036	0.0071
C	0.0008	0.0032	0.0063
D	0.0008	0.0030	0.0059

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X17_P4	X4_P4	X17_P4
A to Z ↓	0.0100	0.0109	3.0245	0.7995
A to Z ↑	0.0222	0.0234	7.2698	1.7972
B to Z ↓	0.0113	0.0118	3.0664	0.8100
B to Z ↑	0.0195	0.0199	7.1945	1.8001
C to Z ↓	0.0099	0.0097	2.8161	0.6852
C to Z ↑	0.0166	0.0174	6.8493	1.7027

D to Z ↓	0.0078	0.0069	2.8760	0.6899
D to Z ↑	0.0157	0.0146	6.8699	1.7083
	X34_P4		**X34_P4**	
A to Z ↓	0.0107		0.4105	
A to Z ↑	0.0230		0.9173	
B to Z ↓	0.0117		0.4159	
B to Z ↑	0.0195		0.9138	
C to Z ↓	0.0100		0.3653	
C to Z ↑	0.0170		0.8671	
D to Z ↓	0.0072		0.3692	
D to Z ↑	0.0144		0.8702	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	1.196e-05	1.310e-09
X17_P4	4.603e-05	3.464e-09
X34_P4	8.707e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P4	X17_P4	X34_P4
A (output stable)	3.593e-05	1.762e-04	3.476e-04
B (output stable)	3.796e-05	2.100e-04	4.014e-04
C (output stable)	7.334e-05	3.969e-04	7.641e-04
D (output stable)	1.205e-04	7.208e-04	1.341e-03
A to Z	2.719e-03	1.164e-02	2.255e-02
B to Z	2.450e-03	1.008e-02	1.960e-02
C to Z	1.775e-03	7.607e-03	1.452e-02
D to Z	1.408e-03	5.443e-03	1.041e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

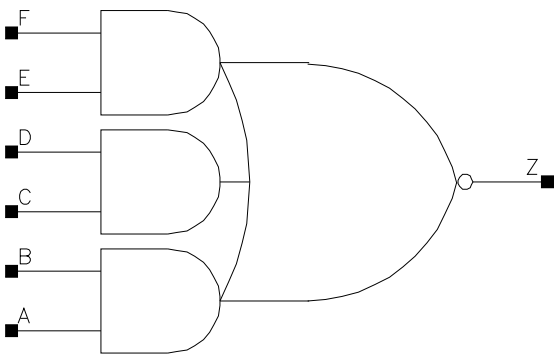
Pin Cycle (vdds)	X4_P4	X17_P4	X34_P4
A (output stable)	1.320e-07	-2.726e-07	-4.287e-07
B (output stable)	1.156e-07	-3.281e-07	-6.064e-07
C (output stable)	1.228e-05	4.900e-05	9.531e-05
D (output stable)	2.225e-05	1.690e-04	2.918e-04
A to Z	1.606e-06	7.092e-06	1.242e-05
B to Z	1.625e-06	6.631e-06	1.092e-05
C to Z	3.243e-07	2.379e-06	3.332e-06
D to Z	4.750e-08	1.309e-06	2.332e-06

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X8_P4	1.200	2.176	2.6112
X13_P4	1.200	2.720	3.2640
X17_P4	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P4	X8_P4	X13_P4	X17_P4
A	0.0009	0.0018	0.0028	0.0037

B	0.0009	0.0017	0.0026	0.0035
C	0.0009	0.0018	0.0026	0.0034
D	0.0009	0.0017	0.0025	0.0033
E	0.0011	0.0017	0.0026	0.0033
F	0.0009	0.0016	0.0024	0.0032

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0123	0.0150	2.6780	1.5482
A to Z ↑	0.0319	0.0316	6.9565	3.2380
B to Z ↓	0.0140	0.0163	2.7124	1.5624
B to Z ↑	0.0291	0.0284	6.9493	3.2459
C to Z ↓	0.0110	0.0132	2.6583	1.5622
C to Z ↑	0.0283	0.0285	6.9902	3.2500
D to Z ↓	0.0124	0.0147	2.6998	1.5815
D to Z ↑	0.0254	0.0253	6.9539	3.2492
E to Z ↓	0.0077	0.0095	2.6323	1.5663
E to Z ↑	0.0226	0.0226	6.9129	3.2257
F to Z ↓	0.0083	0.0103	2.6866	1.5931
F to Z ↑	0.0198	0.0193	6.9619	3.2301
	X13_P4	X17_P4	X13_P4	X17_P4
A to Z ↓	0.0143	0.0145	1.0529	0.8033
A to Z ↑	0.0294	0.0296	2.1398	1.6399
B to Z ↓	0.0160	0.0159	1.0623	0.8107
B to Z ↑	0.0267	0.0265	2.1477	1.6405
C to Z ↓	0.0127	0.0127	1.0584	0.7957
C to Z ↑	0.0262	0.0267	2.1508	1.6499
D to Z ↓	0.0142	0.0138	1.0705	0.8051
D to Z ↑	0.0235	0.0235	2.1539	1.6470
E to Z ↓	0.0091	0.0091	1.0563	0.7982
E to Z ↑	0.0212	0.0213	2.1396	1.6343
F to Z ↓	0.0099	0.0094	1.0732	0.8112
F to Z ↑	0.0181	0.0181	2.1433	1.6416

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	2.500e-05	1.807e-09
X8_P4	4.769e-05	3.132e-09
X13_P4	6.505e-05	3.795e-09
X17_P4	8.722e-05	4.954e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	6.408e-05	1.499e-04	2.115e-04	2.853e-04
B (output stable)	6.742e-05	2.096e-04	2.575e-04	3.844e-04
C (output stable)	7.281e-05	1.641e-04	2.275e-04	3.132e-04
D (output stable)	7.898e-05	2.392e-04	2.842e-04	4.118e-04
E (output stable)	1.056e-04	2.552e-04	3.610e-04	4.867e-04
F (output stable)	1.182e-04	3.204e-04	4.175e-04	5.802e-04

A to Z	4.227e-03	8.853e-03	1.238e-02	1.636e-02
B to Z	3.903e-03	8.033e-03	1.132e-02	1.480e-02
C to Z	3.222e-03	6.968e-03	9.475e-03	1.261e-02
D to Z	2.935e-03	6.233e-03	8.517e-03	1.119e-02
E to Z	2.227e-03	4.872e-03	6.673e-03	8.817e-03
F to Z	1.965e-03	4.180e-03	5.736e-03	7.497e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

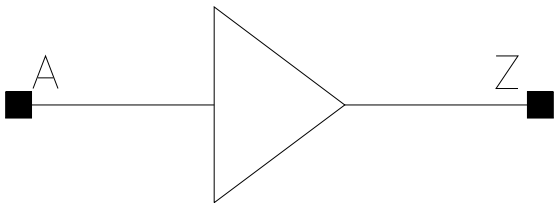
Pin Cycle (vdds)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	-3.525e-07	-7.122e-07	-7.992e-07	-1.078e-06
B (output stable)	-3.782e-07	-7.841e-07	-8.933e-07	-1.203e-06
C (output stable)	1.367e-05	2.469e-05	2.851e-05	3.627e-05
D (output stable)	1.364e-05	2.465e-05	2.853e-05	3.610e-05
E (output stable)	3.992e-05	9.345e-05	1.005e-04	1.365e-04
F (output stable)	4.336e-05	9.423e-05	1.016e-04	1.357e-04
A to Z	3.506e-06	6.244e-06	6.032e-06	7.788e-06
B to Z	3.498e-06	6.537e-06	6.109e-06	8.023e-06
C to Z	1.125e-06	2.014e-06	1.608e-06	2.961e-06
D to Z	9.691e-07	2.025e-06	1.661e-06	2.220e-06
E to Z	-2.267e-07	-4.572e-07	-5.438e-07	-7.432e-07
F to Z	-2.719e-07	-8.721e-07	-9.868e-07	-1.557e-06

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.408	0.4896
X6_P4	1.200	0.408	0.4896
X8_P4	1.200	0.408	0.4896
X13_P4	1.200	0.544	0.6528
X16_P4	1.200	0.544	0.6528
X21_P4	1.200	0.680	0.8160
X25_P4	1.200	0.680	0.8160
X29_P4	1.200	0.952	1.1424
X33_P4	1.200	0.952	1.1424
X42_P4	1.200	1.088	1.3056
X50_P4	1.200	1.224	1.4688
X58_P4	1.200	1.496	1.7952
X67_P4	1.200	1.632	1.9584
X75_P4	1.200	1.768	2.1216
X84_P4	1.200	1.904	2.2848
X100_P4	1.200	2.312	2.7744
X134_P4	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0008	0.0008	0.0008	0.0008
	X16_P4	X21_P4	X25_P4	X29_P4
A	0.0009	0.0012	0.0012	0.0016
	X33_P4	X42_P4	X50_P4	X58_P4
A	0.0016	0.0018	0.0022	0.0032

	X67_P4	X75_P4	X84_P4	X100_P4
A	0.0032	0.0032	0.0031	0.0042
	X134_P4			
A	0.0053			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0203	0.0205	2.8899	2.1530
A to Z ↑	0.0146	0.0146	4.6441	3.4615
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0214	0.0241	1.6148	1.0310
A to Z ↑	0.0154	0.0177	2.5115	1.6210
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0258	0.0221	0.8259	0.6339
A to Z ↑	0.0188	0.0163	1.2576	0.9801
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0232	0.0220	0.5482	0.4605
A to Z ↑	0.0171	0.0157	0.8288	0.7012
	X33_P4	**X42_P4**	**X33_P4**	**X42_P4**
A to Z ↓	0.0231	0.0226	0.4102	0.3328
A to Z ↑	0.0165	0.0166	0.6196	0.4980
	X50_P4	**X58_P4**	**X50_P4**	**X58_P4**
A to Z ↓	0.0223	0.0207	0.2764	0.2381
A to Z ↑	0.0163	0.0153	0.4138	0.3559
	X67_P4	**X75_P4**	**X67_P4**	**X75_P4**
A to Z ↓	0.0217	0.0230	0.2093	0.1886
A to Z ↑	0.0160	0.0170	0.3116	0.2792
	X84_P4	**X100_P4**	**X84_P4**	**X100_P4**
A to Z ↓	0.0240	0.0225	0.1709	0.1436
A to Z ↑	0.0179	0.0167	0.2518	0.2110
	X134_P4		**X134_P4**	
A to Z ↓	0.0237		0.1115	
A to Z ↑	0.0180		0.1614	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	1.607e-05	9.792e-10
X6_P4	1.919e-05	9.792e-10
X8_P4	2.263e-05	9.792e-10
X13_P4	2.997e-05	1.145e-09
X16_P4	3.593e-05	1.145e-09
X21_P4	4.855e-05	1.310e-09
X25_P4	5.254e-05	1.310e-09
X29_P4	6.413e-05	1.642e-09
X33_P4	6.635e-05	1.642e-09
X42_P4	8.155e-05	1.807e-09
X50_P4	9.748e-05	1.973e-09
X58_P4	1.200e-04	2.304e-09
X67_P4	1.312e-04	2.470e-09
X75_P4	1.425e-04	2.635e-09

X84_P4	1.538e-04	2.801e-09
X100_P4	1.876e-04	3.298e-09
X134_P4	2.439e-04	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	2.320e-03	2.605e-03	3.106e-03	4.246e-03
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	5.145e-03	6.895e-03	7.810e-03	8.875e-03
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	9.947e-03	1.229e-02	1.454e-02	1.758e-02
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	1.959e-02	2.220e-02	2.466e-02	2.905e-02
	X134_P4			
A to Z	4.069e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

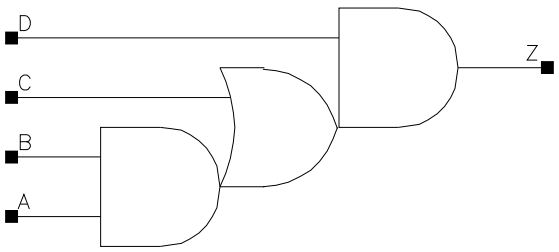
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	1.323e-06	1.683e-06	-5.420e-08	5.185e-07
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	2.438e-07	1.912e-06	1.446e-06	-3.371e-07
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	1.445e-06	2.452e-06	2.600e-06	6.563e-06
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	-5.990e-07	3.105e-06	1.578e-06	4.034e-06
	X134_P4			
A to Z	2.555e-06			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.632	1.9584
X25_P4	1.200	1.768	2.1216
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0010	0.0022	0.0022	0.0022
B	0.0011	0.0020	0.0020	0.0020
C	0.0011	0.0025	0.0025	0.0024
D	0.0016	0.0021	0.0021	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0273	0.0261	1.6488	0.8164
A to Z ↑	0.0238	0.0225	2.5406	1.2399
B to Z ↓	0.0252	0.0237	1.6436	0.8147
B to Z ↑	0.0244	0.0228	2.5397	1.2390
C to Z ↓	0.0241	0.0225	1.6400	0.8132
C to Z ↑	0.0179	0.0165	2.5200	1.2293

D to Z ↓	0.0232	0.0207	1.6252	0.8062
D to Z ↑	0.0202	0.0177	2.5250	1.2310
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0287	0.0305	0.5547	0.4179
A to Z ↑	0.0250	0.0265	0.8387	0.6301
B to Z ↓	0.0265	0.0288	0.5536	0.4168
B to Z ↑	0.0254	0.0274	0.8388	0.6293
C to Z ↓	0.0254	0.0275	0.5522	0.4155
C to Z ↑	0.0187	0.0202	0.8310	0.6234
D to Z ↓	0.0225	0.0238	0.5461	0.4097
D to Z ↑	0.0196	0.0209	0.8328	0.6245

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	3.016e-05	1.642e-09
X17_P4	5.608e-05	2.470e-09
X25_P4	6.565e-05	2.635e-09
X33_P4	7.524e-05	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	8.412e-05	1.799e-04	1.815e-04	1.601e-04
B (output stable)	1.159e-04	2.526e-04	2.550e-04	2.193e-04
C (output stable)	3.126e-04	5.028e-04	5.051e-04	4.792e-04
D (output stable)	1.441e-04	2.191e-04	2.207e-04	2.176e-04
A to Z	5.003e-03	9.296e-03	1.190e-02	1.430e-02
B to Z	4.685e-03	8.498e-03	1.108e-02	1.362e-02
C to Z	4.087e-03	7.263e-03	9.712e-03	1.199e-02
D to Z	5.092e-03	9.055e-03	1.138e-02	1.344e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

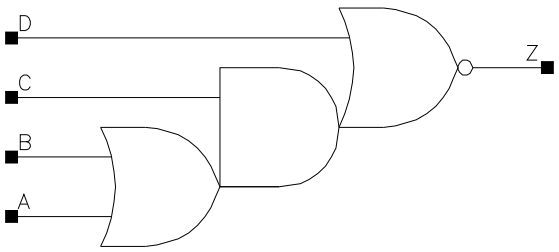
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	6.308e-08	-1.098e-08	-1.107e-08	1.950e-08
B (output stable)	-1.046e-08	-1.089e-07	-1.173e-07	-4.947e-08
C (output stable)	6.101e-06	1.102e-05	1.109e-05	1.107e-05
D (output stable)	7.480e-08	1.341e-08	2.455e-08	4.262e-08
A to Z	5.180e-07	5.420e-07	5.220e-07	1.109e-06
B to Z	6.000e-07	1.000e-06	9.550e-07	5.980e-07
C to Z	3.588e-07	4.684e-07	-1.323e-08	4.550e-08
D to Z	6.111e-07	2.487e-07	1.459e-07	8.152e-08

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.952	1.1424
X11_P4	1.200	1.496	1.7952
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X16_P4	X21_P4
A	0.0010	0.0018	0.0028	0.0037
B	0.0009	0.0018	0.0028	0.0036
C	0.0009	0.0018	0.0027	0.0037
D	0.0013	0.0018	0.0027	0.0037

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0104	0.0098	2.6433	1.3911
A to Z ↑	0.0266	0.0248	7.1370	3.7271
B to Z ↓	0.0098	0.0095	2.5742	1.3641
B to Z ↑	0.0256	0.0244	7.1489	3.7329
C to Z ↓	0.0097	0.0092	2.4670	1.2994
C to Z ↑	0.0165	0.0152	4.8049	2.4718

D to Z ↓	0.0048	0.0037	1.7002	0.8588
D to Z ↑	0.0158	0.0141	5.1452	2.6540
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0099	0.0102	0.9343	0.7220
A to Z ↑	0.0231	0.0245	2.3872	1.8482
B to Z ↓	0.0091	0.0095	0.9411	0.7238
B to Z ↑	0.0230	0.0237	2.3906	1.8515
C to Z ↓	0.0094	0.0095	0.8895	0.6832
C to Z ↑	0.0146	0.0148	1.6330	1.2263
D to Z ↓	0.0038	0.0039	0.5964	0.4545
D to Z ↑	0.0132	0.0132	1.7380	1.3174

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P4	2.045e-05	1.642e-09
X11_P4	3.765e-05	2.304e-09
X16_P4	5.000e-05	2.635e-09
X21_P4	6.674e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	4.232e-05	7.951e-05	1.050e-04	1.684e-04
B (output stable)	3.072e-05	5.893e-05	7.926e-05	1.200e-04
C (output stable)	1.108e-04	2.228e-04	3.095e-04	4.320e-04
D (output stable)	2.785e-04	5.809e-04	8.415e-04	1.145e-03
A to Z	3.398e-03	6.024e-03	8.497e-03	1.187e-02
B to Z	2.801e-03	5.020e-03	7.274e-03	9.822e-03
C to Z	2.472e-03	4.341e-03	6.258e-03	8.583e-03
D to Z	1.744e-03	3.110e-03	4.342e-03	5.767e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

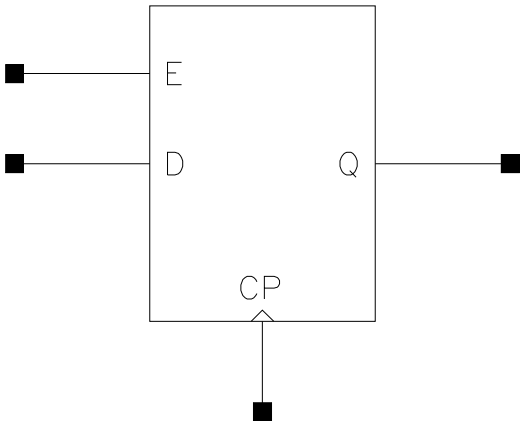
Pin Cycle (vdds)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	1.603e-07	1.349e-07	1.878e-07	2.398e-07
B (output stable)	9.662e-06	1.314e-05	1.658e-05	3.317e-05
C (output stable)	1.327e-07	2.781e-07	3.992e-07	3.668e-07
D (output stable)	5.595e-05	1.137e-04	1.516e-04	2.264e-04
A to Z	2.292e-06	3.572e-06	3.025e-06	7.263e-06
B to Z	8.750e-07	9.610e-07	6.410e-07	2.195e-06
C to Z	1.506e-06	2.454e-06	3.662e-06	4.697e-06
D to Z	8.352e-07	1.478e-06	1.702e-06	1.198e-06

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.128	3.7536
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0012	0.0012	0.0009

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0309	0.0358	1.6343	0.8431
CP to Q ↑	0.0383	0.0413	2.5495	1.2782
	X33_P4		**X33_P4**	
CP to Q ↓	0.0544		0.4156	
CP to Q ↑	0.0659		0.6342	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0412	0.0412	0.0412
CP ↑	min_pulse_width to CP	0.0242	0.0290	0.0205
D ↓	hold_rising to CP	-0.0117	-0.0117	-0.0117
D ↑	hold_rising to CP	0.0009	0.0006	0.0009
D ↓	setup_rising to CP	0.0415	0.0415	0.0415
D ↑	setup_rising to CP	0.0239	0.0239	0.0239
E ↓	hold_rising to CP	-0.0060	-0.0060	-0.0090
E ↑	hold_rising to CP	0.0036	0.0036	0.0036
E ↓	setup_rising to CP	0.0455	0.0429	0.0429
E ↑	setup_rising to CP	0.0442	0.0442	0.0442

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	9.089e-05	4.126e-09
X17_P4	1.031e-04	4.292e-09
X33_P4	1.423e-04	4.954e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

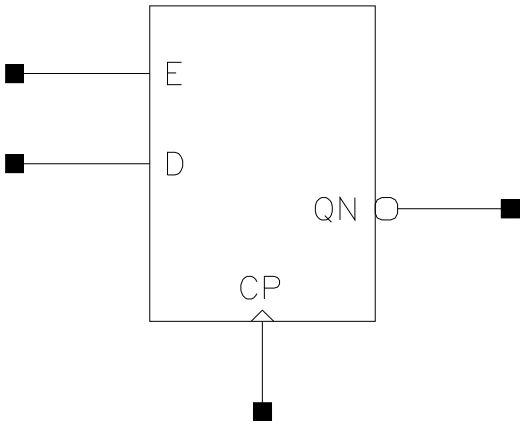
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.250e-03	5.250e-03	5.256e-03
Clock 100Mhz Data 25Mhz	1.123e-02	1.250e-02	1.601e-02
Clock 100Mhz Data 50Mhz	1.721e-02	1.975e-02	2.676e-02
Clock = 0 Data 100Mhz	6.755e-03	6.756e-03	6.756e-03
Clock = 1 Data 100Mhz	1.897e-03	1.897e-03	1.897e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.264	3.9168
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0009	0.0012	0.0012

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0529	0.0503	1.6802	0.8036
CP to QN ↑	0.0421	0.0431	2.5840	1.2425
	X33_P4		**X33_P4**	
CP to QN ↓	0.0541		0.4173	
CP to QN ↑	0.0477		0.6362	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0412	0.0412	0.0412
CP ↑	min_pulse_width to CP	0.0205	0.0242	0.0253
D ↓	hold_rising to CP	-0.0117	-0.0117	-0.0117
D ↑	hold_rising to CP	0.0009	0.0009	0.0006
D ↓	setup_rising to CP	0.0415	0.0415	0.0412
D ↑	setup_rising to CP	0.0239	0.0239	0.0239
E ↓	hold_rising to CP	-0.0090	-0.0060	-0.0060
E ↑	hold_rising to CP	0.0005	0.0036	0.0036
E ↓	setup_rising to CP	0.0455	0.0429	0.0429
E ↑	setup_rising to CP	0.0442	0.0442	0.0442

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	9.048e-05	4.126e-09
X17_P4	1.098e-04	4.457e-09
X33_P4	1.392e-04	4.954e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

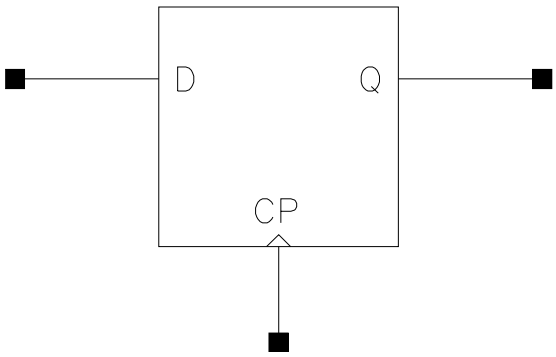
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.247e-03	5.247e-03	5.248e-03
Clock 100Mhz Data 25Mhz	1.126e-02	1.287e-02	1.585e-02
Clock 100Mhz Data 50Mhz	1.727e-02	2.050e-02	2.646e-02
Clock = 0 Data 100Mhz	6.757e-03	6.757e-03	6.754e-03
Clock = 1 Data 100Mhz	1.897e-03	1.897e-03	1.897e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.176	2.6112
X17_P4	1.200	2.448	2.9376
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0321	0.0358	1.6275	0.8352
CP to Q ↑	0.0385	0.0431	2.4721	1.2545
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to Q ↓	0.0457	0.0480	0.4921	0.4488
CP to Q ↑	0.0490	0.0506	0.7018	0.6417

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0412	0.0412	0.0412	0.0412
CP ↑	min_pulse_width to CP	0.0242	0.0290	0.0386	0.0386
D ↓	hold_rising to CP	0.0131	0.0103	0.0103	0.0103
D ↑	hold_rising to CP	0.0124	0.0124	0.0124	0.0124
D ↓	setup_rising to CP	0.0220	0.0220	0.0220	0.0220
D ↑	setup_rising to CP	0.0122	0.0123	0.0123	0.0123

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	7.364e-05	3.132e-09
X17_P4	8.674e-05	3.464e-09
X30_P4	1.081e-04	3.795e-09
X33_P4	1.097e-04	3.795e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

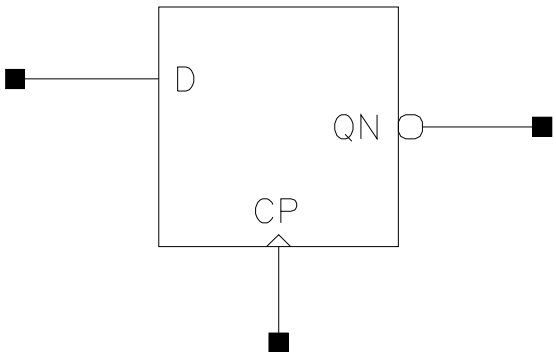
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.456e-03	5.480e-03	5.489e-03	5.494e-03
Clock 100Mhz Data 25Mhz	9.923e-03	1.159e-02	1.463e-02	1.545e-02
Clock 100Mhz Data 50Mhz	1.439e-02	1.771e-02	2.377e-02	2.540e-02
Clock = 0 Data 100Mhz	4.498e-03	4.628e-03	4.668e-03	4.689e-03
Clock = 1 Data 100Mhz	3.390e-05	3.403e-05	3.417e-05	3.422e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0311	0.0362	1.6769	0.8624
CP to QN ↑	0.0328	0.0352	2.4679	1.2559
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to QN ↓	0.0536	0.0540	0.4578	0.4160
CP to QN ↑	0.0445	0.0509	0.6812	0.6351

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0375	0.0375	0.0412	0.0412
CP ↑	min_pulse_width to CP	0.0242	0.0253	0.0242	0.0290
D ↓	hold_rising to CP	0.0127	0.0152	0.0103	0.0131
D ↑	hold_rising to CP	0.0177	0.0177	0.0125	0.0121
D ↓	setup_rising to CP	0.0171	0.0171	0.0220	0.0220
D ↑	setup_rising to CP	0.0122	0.0122	0.0123	0.0122

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	6.881e-05	2.801e-09
X17_P4	8.130e-05	2.967e-09
X30_P4	1.158e-04	3.795e-09
X33_P4	1.221e-04	3.961e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

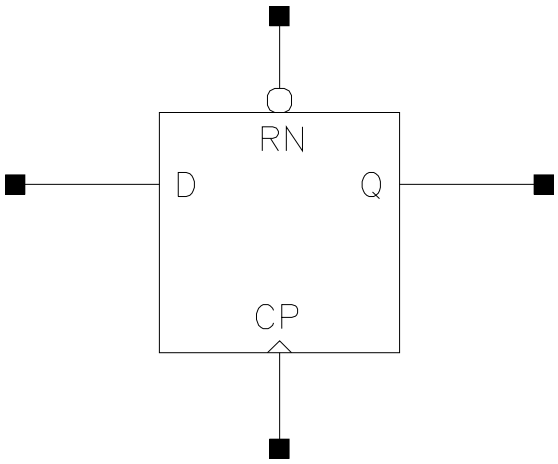
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.281e-03	5.282e-03	5.355e-03	5.386e-03
Clock 100Mhz Data 25Mhz	9.458e-03	1.080e-02	1.366e-02	1.458e-02
Clock 100Mhz Data 50Mhz	1.363e-02	1.631e-02	2.197e-02	2.377e-02
Clock = 0 Data 100Mhz	3.979e-03	3.979e-03	4.237e-03	4.303e-03
Clock = 1 Data 100Mhz	3.375e-05	3.365e-05	3.390e-05	3.412e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0008	0.0008
RN	0.0010	0.0010

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0375	0.0471	0.8429	0.5000
CP to Q ↑	0.0444	0.0502	1.2588	0.7040
RN to Q ↓	0.0508	0.0569	0.8193	0.4816

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0412	0.0412
CP ↑	min_pulse_width to CP	0.0290	0.0386
D ↓	hold_rising to CP	0.0103	0.0103
D ↑	hold_rising to CP	0.0128	0.0128
D ↓	setup_rising to CP	0.0213	0.0244
D ↑	setup_rising to CP	0.0144	0.0144
RN ↓	min_pulse_width to RN	0.0757	0.0952
RN ↑	recovery_rising to CP	0.0127	0.0127
RN ↑	removal_rising to CP	-0.0027	-0.0027

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P4	9.121e-05	4.292e-09
X30_P4	1.093e-04	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

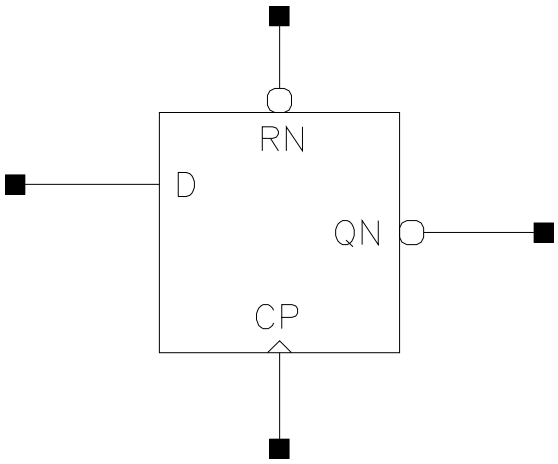
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	5.801e-03	5.795e-03
Clock 100Mhz Data 25Mhz	1.230e-02	1.528e-02
Clock 100Mhz Data 50Mhz	1.879e-02	2.476e-02
Clock = 0 Data 100Mhz	5.441e-03	5.444e-03
Clock = 1 Data 100Mhz	3.425e-05	3.440e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0008	0.0008
RN	0.0010	0.0010

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0513	0.0557	0.7967	0.4592
CP to QN ↑	0.0427	0.0467	1.2331	0.6833
RN to QN ↑	0.0580	0.0614	1.2307	0.6829

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0412	0.0412
CP ↑	min_pulse_width to CP	0.0242	0.0253
D ↓	hold_rising to CP	0.0078	0.0078
D ↑	hold_rising to CP	0.0128	0.0128
D ↓	setup_rising to CP	0.0244	0.0213
D ↑	setup_rising to CP	0.0144	0.0119
RN ↓	min_pulse_width to RN	0.0610	0.0659
RN ↑	recovery_rising to CP	0.0127	0.0127
RN ↑	removal_rising to CP	-0.0027	-0.0027

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P4	1.076e-04	4.292e-09
X30_P4	1.313e-04	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

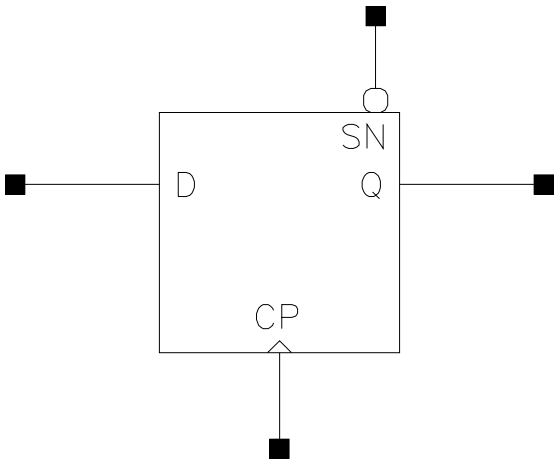
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	5.788e-03	5.796e-03
Clock 100Mhz Data 25Mhz	1.258e-02	1.463e-02
Clock 100Mhz Data 50Mhz	1.937e-02	2.346e-02
Clock = 0 Data 100Mhz	5.503e-03	5.487e-03
Clock = 1 Data 100Mhz	3.432e-05	3.446e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0008	0.0008
SN	0.0013	0.0013

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0377	0.0479	0.8433	0.4974
CP to Q ↑	0.0439	0.0501	1.2586	0.7046
SN to Q ↑	0.0370	0.0407	1.2449	0.6936

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0460	0.0460
CP ↑	min_pulse_width to CP	0.0290	0.0386
D ↓	hold_rising to CP	0.0078	0.0078
D ↑	hold_rising to CP	0.0128	0.0125
D ↓	setup_rising to CP	0.0269	0.0269
D ↑	setup_rising to CP	0.0119	0.0119
SN ↓	min_pulse_width to SN	0.0452	0.0549
SN ↑	recovery_rising to CP	0.0029	0.0029
SN ↑	removal_rising to CP	0.0239	0.0239

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P4	9.862e-05	4.292e-09
X30_P4	1.227e-04	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

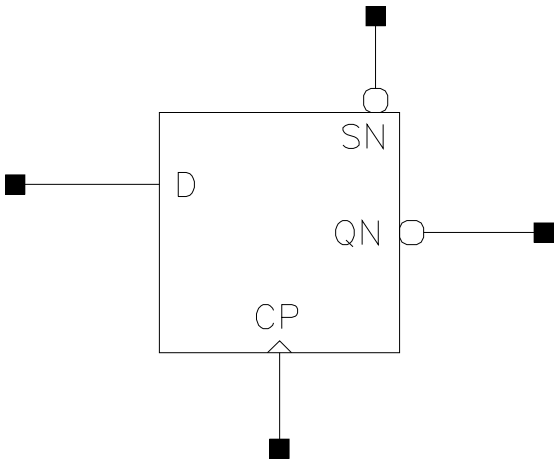
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	5.867e-03	5.853e-03
Clock 100Mhz Data 25Mhz	1.238e-02	1.537e-02
Clock 100Mhz Data 50Mhz	1.889e-02	2.489e-02
Clock = 0 Data 100Mhz	5.384e-03	5.384e-03
Clock = 1 Data 100Mhz	3.452e-05	3.464e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0008	0.0008
SN	0.0013	0.0013

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0508	0.0552	0.7995	0.4601
CP to QN ↑	0.0429	0.0467	1.2297	0.6823
SN to QN ↓	0.0445	0.0487	0.7985	0.4594

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0460	0.0460
CP ↑	min_pulse_width to CP	0.0242	0.0253
D ↓	hold_rising to CP	0.0078	0.0078
D ↑	hold_rising to CP	0.0128	0.0128
D ↓	setup_rising to CP	0.0269	0.0269
D ↑	setup_rising to CP	0.0119	0.0119
SN ↓	min_pulse_width to SN	0.0403	0.0403
SN ↑	recovery_rising to CP	0.0029	0.0029
SN ↑	removal_rising to CP	0.0239	0.0239

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P4	9.874e-05	4.292e-09
X30_P4	1.163e-04	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

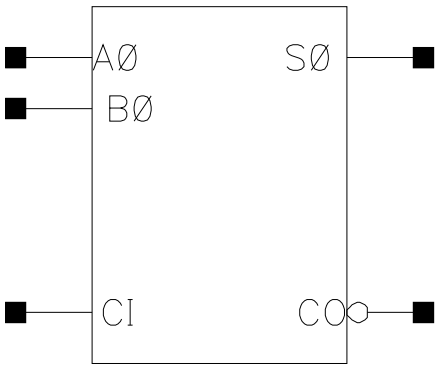
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	5.855e-03	5.855e-03
Clock 100Mhz Data 25Mhz	1.262e-02	1.462e-02
Clock 100Mhz Data 50Mhz	1.938e-02	2.339e-02
Clock = 0 Data 100Mhz	5.382e-03	5.384e-03
Clock = 1 Data 100Mhz	3.467e-05	3.479e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_P4	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_-P4	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_-P4	1.200	3.672	4.4064
C12T28SOI_LRS1_-FA1X33_P4	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_-FA1X8_P4	C12T28SOI_LR_-FA1X33_P4	C12T28SOI_LRS1_-FA1X8_P4	C12T28SOI_LRS1_-FA1X33_P4
A0	0.0035	0.0070	0.0031	0.0060
B0	0.0031	0.0067	0.0033	0.0058
CI	0.0023	0.0050	0.0023	0.0042

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P4	**C12T28SOI_LR_-FA1X33_P4**	**C12T28SOI_LR_-FA1X8_P4**	**C12T28SOI_LR_-FA1X33_P4**
A0 to CO ↓	0.0359	0.0394	1.6997	0.4441
A0 to CO ↑	0.0255	0.0269	2.5444	0.6535
A0 to S0 ↓	0.0367	0.0466	1.6759	0.4342
A0 to S0 ↑	0.0377	0.0465	2.5230	0.6455
B0 to CO ↓	0.0357	0.0400	1.7048	0.4464
B0 to CO ↑	0.0264	0.0283	2.5460	0.6510
B0 to S0 ↓	0.0371	0.0476	1.6758	0.4342
B0 to S0 ↑	0.0381	0.0474	2.5237	0.6455
CI to CO ↓	0.0352	0.0398	1.7073	0.4453
CI to CO ↑	0.0265	0.0278	2.5442	0.6532
CI to S0 ↓	0.0369	0.0472	1.6766	0.4341
CI to S0 ↑	0.0383	0.0479	2.5222	0.6453
	C12T28SOI_LRS1_-FA1X8_P4	**C12T28SOI_LRS1_-FA1X33_P4**	**C12T28SOI_LRS1_-FA1X8_P4**	**C12T28SOI_LRS1_-FA1X33_P4**
A0 to CO ↓	0.0239	0.0293	3.0709	0.5308
A0 to CO ↑	0.0195	0.0224	2.5893	0.6398
A0 to S0 ↓	0.0483	0.0596	1.8083	0.4537
A0 to S0 ↑	0.0449	0.0487	2.6182	0.6576
B0 to CO ↓	0.0250	0.0307	3.0729	0.5318
B0 to CO ↑	0.0179	0.0213	2.5880	0.6401
B0 to S0 ↓	0.0487	0.0613	1.8093	0.4537
B0 to S0 ↑	0.0452	0.0503	2.6185	0.6574
CI to CO ↓	0.0247	0.0425	3.0666	0.5394
CI to CO ↑	0.0197	0.0243	2.6552	0.6443
CI to S0 ↓	0.0280	0.0363	1.8115	0.4545
CI to S0 ↑	0.0240	0.0244	2.6183	0.6578

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_FA1X8_P4	7.230e-05	3.132e-09
C12T28SOI_LR_FA1X33_P4	1.889e-04	6.445e-09
C12T28SOI_LRS1_FA1X8_P4	1.591e-04	4.954e-09
C12T28SOI_LRS1_FA1X33_P4	3.327e-04	1.025e-08

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P4	C12T28SOI_LR_-FA1X33_P4	C12T28SOI_LRS1_-FA1X8_P4	C12T28SOI_LRS1_-FA1X33_P4
A0 to CO	5.261e-03	1.591e-02	7.915e-03	2.020e-02
A0 to S0	5.296e-03	1.650e-02	1.059e-02	2.493e-02
B0 to CO	5.319e-03	1.623e-02	7.989e-03	2.049e-02
B0 to S0	5.210e-03	1.642e-02	1.078e-02	2.548e-02
CI to CO	5.368e-03	1.640e-02	5.732e-03	1.864e-02
CI to S0	5.171e-03	1.635e-02	6.486e-03	1.991e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P4	C12T28SOI_LR_-FA1X33_P4	C12T28SOI_LRS1_-FA1X8_P4	C12T28SOI_LRS1_-FA1X33_P4
A0 to CO	-2.045e-08	-2.867e-07	3.029e-07	1.964e-07

A0 to S0	2.493e-07	3.340e-08	1.796e-07	-2.800e-09
B0 to CO	-4.514e-08	5.655e-08	1.086e-07	1.578e-06
B0 to S0	7.461e-06	1.356e-05	1.194e-06	3.929e-06
CI to CO	1.034e-05	1.976e-05	7.702e-07	-4.507e-07
CI to S0	1.286e-05	1.789e-05	1.396e-06	-5.651e-07

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X33_P4	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X33_P4
A0	0.0012	0.0035
B0	0.0010	0.0029

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
A0 to CO ↓	0.0276	0.0259	1.6748	0.4153
A0 to CO ↑	0.0234	0.0216	2.5153	0.6481
A0 to S0 ↓	0.0338	0.0328	1.6434	0.4153
A0 to S0 ↑	0.0330	0.0377	2.4885	0.6394
B0 to CO ↓	0.0267	0.0239	1.6743	0.4124
B0 to CO ↑	0.0255	0.0231	2.5155	0.6480
B0 to S0 ↓	0.0355	0.0334	1.6440	0.4151
B0 to S0 ↑	0.0323	0.0360	2.4889	0.6394

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	4.337e-05	1.973e-09
X33_P4	1.581e-04	4.126e-09

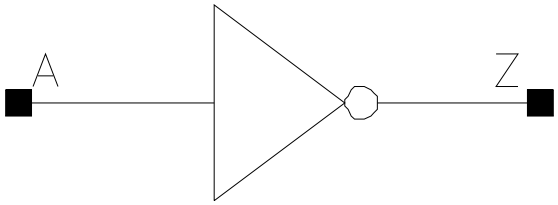
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X33_P4
A0 to CO	4.025e-03	1.366e-02
A0 to S0	3.778e-03	1.355e-02
B0 to CO	4.099e-03	1.396e-02
B0 to S0	3.731e-03	1.317e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X8_P4	X33_P4
A0 to CO	9.063e-08	4.964e-07
A0 to S0	2.417e-08	3.822e-07
B0 to CO	3.399e-07	1.070e-05
B0 to S0	2.413e-07	5.169e-06

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.272	0.3264
X6_P4	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X13_P4	1.200	0.408	0.4896
X17_P4	1.200	0.408	0.4896
X21_P4	1.200	0.544	0.6528
X25_P4	1.200	0.544	0.6528
X29_P4	1.200	0.680	0.8160
X33_P4	1.200	0.680	0.8160
X50_P4	1.200	0.952	1.1424
X58_P4	1.200	1.088	1.3056
X67_P4	1.200	1.224	1.4688
X75_P4	1.200	1.360	1.6320
X84_P4	1.200	1.496	1.7952
X100_P4	1.200	1.768	2.1216
X134_P4	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0006	0.0008	0.0010	0.0015
	X17_P4	X21_P4	X25_P4	X29_P4
A	0.0019	0.0025	0.0028	0.0034
	X33_P4	X50_P4	X58_P4	X67_P4
A	0.0038	0.0057	0.0066	0.0076
	X75_P4	X84_P4	X100_P4	X134_P4

A	0.0086	0.0097	0.0118	0.0163

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0044	0.0040	3.0829	2.4123
A to Z ↑	0.0108	0.0100	4.7795	3.6558
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0034	0.0026	1.6698	1.0709
A to Z ↑	0.0093	0.0086	2.5637	1.6740
	X17_P4	**X21_P4**	**X17_P4**	**X21_P4**
A to Z ↓	0.0027	0.0030	0.8286	0.6619
A to Z ↑	0.0083	0.0087	1.2636	1.0102
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0030	0.0027	0.5672	0.4798
A to Z ↑	0.0084	0.0081	0.8502	0.7227
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0027	0.0029	0.4262	0.2875
A to Z ↑	0.0079	0.0079	0.6370	0.4266
	X58_P4	**X67_P4**	**X58_P4**	**X67_P4**
A to Z ↓	0.0032	0.0032	0.2493	0.2192
A to Z ↑	0.0082	0.0081	0.3678	0.3224
	X75_P4	**X84_P4**	**X75_P4**	**X84_P4**
A to Z ↓	0.0036	0.0038	0.1980	0.1794
A to Z ↑	0.0085	0.0086	0.2888	0.2616
	X100_P4	**X134_P4**	**X100_P4**	**X134_P4**
A to Z ↓	0.0046	0.0054	0.1528	0.1194
A to Z ↑	0.0093	0.0101	0.2206	0.1697

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	8.463e-06	8.135e-10
X6_P4	1.046e-05	8.135e-10
X8_P4	1.476e-05	8.135e-10
X13_P4	2.302e-05	9.792e-10
X17_P4	2.873e-05	9.792e-10
X21_P4	3.600e-05	1.145e-09
X25_P4	4.036e-05	1.145e-09
X29_P4	4.844e-05	1.310e-09
X33_P4	5.163e-05	1.310e-09
X50_P4	7.410e-05	1.642e-09
X58_P4	8.536e-05	1.807e-09
X67_P4	9.662e-05	1.973e-09
X75_P4	1.079e-04	2.139e-09
X84_P4	1.191e-04	2.304e-09
X100_P4	1.417e-04	2.635e-09
X134_P4	1.867e-04	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4

A to Z	8.484e-04	1.059e-03	1.435e-03	2.096e-03
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	2.694e-03	3.538e-03	4.093e-03	4.677e-03
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	5.184e-03	7.734e-03	9.228e-03	1.032e-02
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	1.187e-02	1.311e-02	1.618e-02	2.250e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

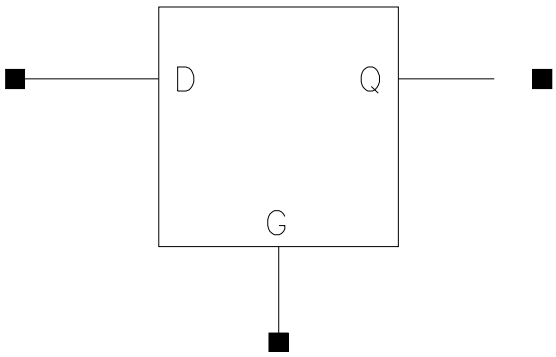
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	6.074e-07	7.611e-07	-1.022e-07	-2.132e-07
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	-4.920e-08	-2.260e-07	-2.450e-07	-2.610e-07
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	-2.060e-07	-4.831e-06	-6.196e-06	-7.012e-06
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	-4.981e-06	6.440e-07	-9.260e-07	1.415e-06

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X23_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P4	X23_P4
D	0.0006	0.0015
G	0.0012	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X23_P4	X8_P4	X23_P4
D to Q ↓	0.0403	0.0327	1.6997	0.7768
D to Q ↑	0.0252	0.0254	2.4789	0.6578
G to Q ↓	0.0403	0.0328	1.6948	0.7753
G to Q ↑	0.0247	0.0226	2.4808	0.6582

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P4	X23_P4
D ↓	hold_falling to G	-0.0017	0.0033
D ↑	hold_falling to G	0.0068	0.0038
D ↓	setup_falling to G	0.0415	0.0294
D ↑	setup_falling to G	0.0282	0.0333
G ↑	min_pulse_width to G	0.0350	0.0349

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	4.040e-05	1.973e-09
X23_P4	7.642e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X23_P4
D (output stable)	2.421e-05	9.707e-05
G (output stable)	1.414e-03	2.798e-03
D to Q	6.725e-03	1.313e-02
G to Q	6.380e-03	1.209e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

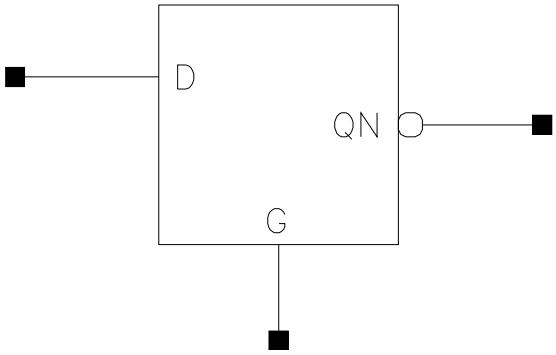
Pin Cycle (vdds)	X8_P4	X23_P4
D (output stable)	1.716e-07	3.267e-07
G (output stable)	5.133e-06	1.746e-05
D to Q	2.399e-07	-4.410e-08
G to Q	5.183e-05	2.785e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P4
D	0.0006
G	0.0014

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P4	X17_P4
D to QN ↓	0.0331	0.8015
D to QN ↑	0.0452	1.2226
G to QN ↓	0.0319	0.8016
G to QN ↑	0.0437	1.2223

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P4
D ↓	hold_falling to G	-0.0069
D ↑	hold_falling to G	0.0038
D ↓	setup_falling to G	0.0315
D ↑	setup_falling to G	0.0236
G ↑	min_pulse_width to G	0.0290

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P4	5.960e-05	2.139e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X17_P4
D (output stable)	2.467e-05
G (output stable)	1.705e-03
D to QN	8.132e-03
G to QN	7.781e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

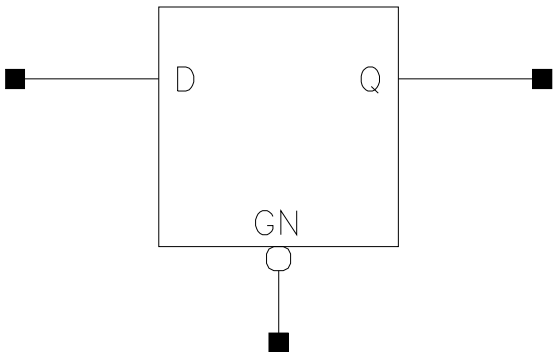
Pin Cycle (vdds)	X17_P4
D (output stable)	1.746e-07
G (output stable)	4.929e-06
D to QN	3.434e-07
G to QN	9.624e-05

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
D	0.0006	0.0009	0.0019
GN	0.0012	0.0015	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D to Q ↓	0.0407	0.0358	1.7047	0.8395
D to Q ↑	0.0257	0.0244	2.4790	1.2714
GN to Q ↓	0.0375	0.0323	1.7055	0.8406
GN to Q ↑	0.0393	0.0380	2.4784	1.2699

	X33_P4		X33_P4	
D to Q ↓	0.0348		0.4287	
D to Q ↑	0.0208		0.6389	
GN to Q ↓	0.0306		0.4292	
GN to Q ↑	0.0301		0.6383	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P4	X17_P4	X33_P4
D ↓	hold_rising to GN	-0.0048	-0.0029	-0.0029
D ↑	hold_rising to GN	0.0076	0.0106	0.0128
D ↓	setup_rising to GN	0.0443	0.0394	0.0401
D ↑	setup_rising to GN	0.0242	0.0246	0.0193
GN ↓	min_pulse_width to GN	0.0529	0.0473	0.0416

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	3.733e-05	1.973e-09
X17_P4	5.669e-05	2.304e-09
X33_P4	9.212e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
D (output stable)	2.382e-05	3.892e-05	1.047e-04
GN (output stable)	1.408e-03	1.906e-03	2.485e-03
D to Q	6.765e-03	9.748e-03	1.590e-02
GN to Q	9.332e-03	1.290e-02	1.940e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

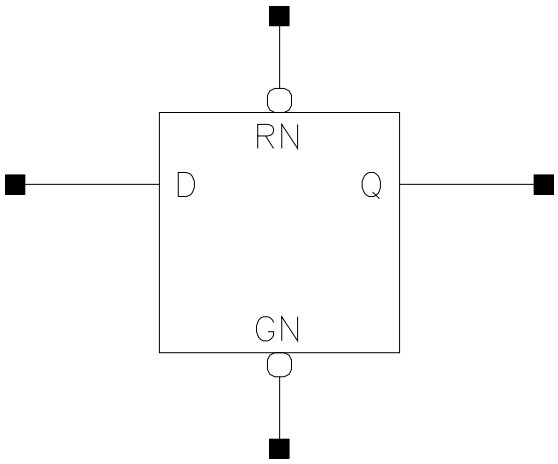
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
D (output stable)	1.886e-07	1.979e-07	3.595e-07
GN (output stable)	5.173e-06	5.394e-06	1.571e-05
D to Q	2.430e-07	2.348e-07	1.451e-07
GN to Q	-5.512e-05	-3.274e-05	-4.967e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.496	1.7952
X33_P4	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X33_P4
D	0.0006	0.0016
GN	0.0013	0.0025
RN	0.0006	0.0007

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
D to Q ↓	0.0380	0.0350	1.6653	0.4307
D to Q ↑	0.0331	0.0430	2.5213	0.6535

GN to Q ↓	0.0352	0.0326	1.6671	0.4314
GN to Q ↑	0.0446	0.0470	2.5213	0.6540
RN to Q ↓	0.0309	0.0531	1.5864	0.4379
RN to Q ↑	0.0342	0.0478	2.5209	0.6544

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P4	X33_P4
D ↓	hold_rising to GN	-0.0051	-0.0002
D ↑	hold_rising to GN	0.0009	-0.0088
D ↓	setup_rising to GN	0.0394	0.0377
D ↑	setup_rising to GN	0.0313	0.0489
GN ↓	min_pulse_width to GN	0.0471	0.0499
RN ↓	min_pulse_width to RN	0.0398	0.0686
RN ↑	recovery_rising to GN	0.0340	0.0511
RN ↑	removal_rising to GN	-0.0191	-0.0335

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	3.425e-05	2.304e-09
X33_P4	7.542e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X33_P4
D (output stable)	8.268e-05	1.723e-04
GN (output stable)	1.613e-03	2.556e-03
RN (output stable)	6.285e-05	1.170e-04
D to Q	6.785e-03	1.865e-02
GN to Q	9.558e-03	2.282e-02
RN to Q	5.116e-03	1.529e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

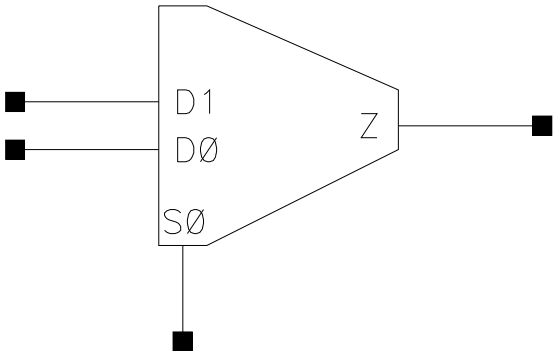
Pin Cycle (vdds)	X8_P4	X33_P4
D (output stable)	-4.335e-08	-1.617e-07
GN (output stable)	2.710e-06	3.448e-06
RN (output stable)	1.233e-07	1.591e-07
D to Q	1.226e-07	-8.000e-08
GN to Q	-5.483e-05	3.854e-05
RN to Q	6.303e-06	-2.321e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
D0	0.0008	0.0012	0.0015	0.0021
D1	0.0008	0.0011	0.0016	0.0021
S0	0.0014	0.0015	0.0018	0.0026

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D0 to Z ↓	0.0307	0.0281	1.6776	0.8204
D0 to Z ↑	0.0240	0.0222	2.5474	1.2478
D1 to Z ↓	0.0293	0.0276	1.6735	0.8192
D1 to Z ↑	0.0220	0.0209	2.5430	1.2470
S0 to Z ↓	0.0264	0.0261	1.6661	0.8164
S0 to Z ↑	0.0253	0.0257	2.5432	1.2464

	X25_P4	X33_P4	X25_P4	X33_P4
D0 to Z ↓	0.0297	0.0270	0.5639	0.4230
D0 to Z ↑	0.0238	0.0219	0.8385	0.6286
D1 to Z ↓	0.0316	0.0280	0.5670	0.4237
D1 to Z ↑	0.0230	0.0214	0.8377	0.6285
S0 to Z ↓	0.0294	0.0271	0.5635	0.4220
S0 to Z ↑	0.0286	0.0263	0.8375	0.6283

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	4.638e-05	1.973e-09
X17_P4	7.596e-05	2.139e-09
X25_P4	1.065e-04	3.298e-09
X33_P4	1.430e-04	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	1.316e-03	2.060e-03	2.407e-03	3.393e-03
D1 (output stable)	1.143e-03	1.972e-03	2.578e-03	3.483e-03
S0 (output stable)	1.635e-03	1.844e-03	2.370e-03	2.997e-03
D0 to Z	4.507e-03	7.655e-03	1.181e-02	1.494e-02
D1 to Z	4.187e-03	7.451e-03	1.194e-02	1.488e-02
S0 to Z	5.163e-03	8.079e-03	1.305e-02	1.607e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

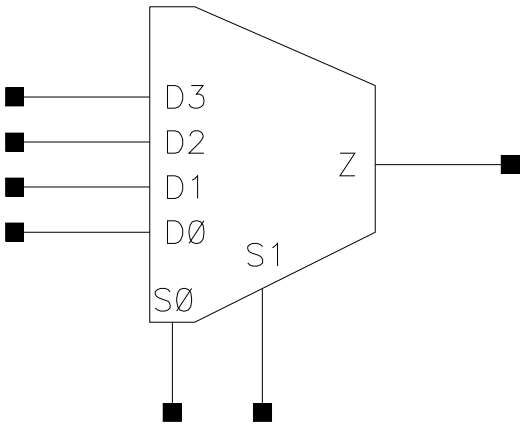
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	1.386e-06	1.788e-06	2.958e-07	4.200e-07
D1 (output stable)	7.198e-07	2.980e-07	4.560e-07	3.390e-07
S0 (output stable)	3.175e-07	2.446e-07	2.460e-07	1.394e-07
D0 to Z	-4.215e-08	1.060e-07	9.425e-08	1.900e-08
D1 to Z	2.571e-07	3.513e-07	-5.000e-09	-2.250e-08
S0 to Z	5.524e-07	3.982e-07	4.279e-07	7.238e-07

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.312	2.7744
X31_P4	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P4	X31_P4
D0	0.0006	0.0017
D1	0.0006	0.0016
D2	0.0006	0.0017
D3	0.0006	0.0016
S0	0.0021	0.0042
S1	0.0012	0.0025

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X31_P4	X8_P4	X31_P4

D0 to Z ↓	0.0534	0.0558	1.7577	0.4847
D0 to Z ↑	0.0337	0.0363	2.5568	0.6878
D1 to Z ↓	0.0530	0.0558	1.7558	0.4848
D1 to Z ↑	0.0339	0.0361	2.5572	0.6877
D2 to Z ↓	0.0571	0.0524	1.7667	0.4799
D2 to Z ↑	0.0356	0.0333	2.5630	0.6835
D3 to Z ↓	0.0569	0.0519	1.7670	0.4790
D3 to Z ↑	0.0352	0.0347	2.5611	0.6859
S0 to Z ↓	0.0576	0.0598	1.7589	0.4818
S0 to Z ↑	0.0424	0.0456	2.5602	0.6866
S1 to Z ↓	0.0413	0.0415	1.7603	0.4816
S1 to Z ↑	0.0337	0.0360	2.5588	0.6859

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	4.503e-05	3.298e-09
X31_P4	1.238e-04	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X31_P4
D0 (output stable)	2.335e-05	1.154e-04
D1 (output stable)	2.569e-05	1.354e-04
D2 (output stable)	3.100e-05	1.215e-04
D3 (output stable)	3.349e-05	1.436e-04
S0 (output stable)	2.334e-03	5.268e-03
S1 (output stable)	1.850e-03	3.786e-03
D0 to Z	5.078e-03	1.799e-02
D1 to Z	5.059e-03	1.804e-02
D2 to Z	5.406e-03	1.684e-02
D3 to Z	5.388e-03	1.688e-02
S0 to Z	7.658e-03	2.328e-02
S1 to Z	6.020e-03	1.796e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

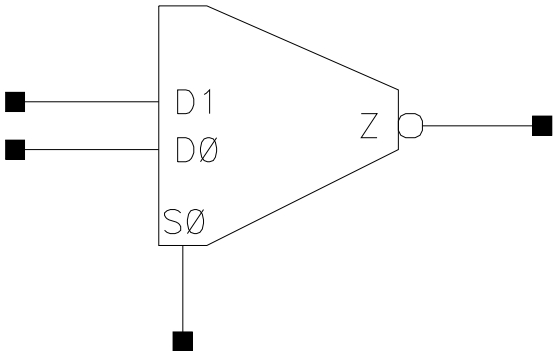
Pin Cycle (vdds)	X8_P4	X31_P4
D0 (output stable)	3.707e-06	1.502e-05
D1 (output stable)	3.664e-06	1.294e-05
D2 (output stable)	3.507e-06	1.497e-05
D3 (output stable)	3.492e-06	1.304e-05
S0 (output stable)	2.036e-07	-2.868e-08
S1 (output stable)	5.963e-05	1.811e-04
D0 to Z	1.591e-06	2.200e-06
D1 to Z	1.588e-06	4.315e-06
D2 to Z	2.479e-06	7.758e-07
D3 to Z	2.514e-06	2.757e-06
S0 to Z	2.402e-06	3.825e-06
S1 to Z	4.338e-05	1.411e-04

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.816	0.9792
X5_P4	1.200	0.952	1.1424
X10_P4	1.200	1.768	2.1216
X16_P4	1.200	2.448	2.9376
X21_P4	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P4	X5_P4	X10_P4	X16_P4
D0	0.0006	0.0009	0.0019	0.0029
D1	0.0006	0.0009	0.0018	0.0028
S0	0.0012	0.0021	0.0027	0.0040
	X21_P4			
D0	0.0038			
D1	0.0037			
S0	0.0046			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X5_P4	X3_P4	X5_P4
D0 to Z ↓	0.0093	0.0093	4.8819	3.1180

D0 to Z ↑	0.0187	0.0170	10.0420	5.2625
D1 to Z ↓	0.0092	0.0090	4.8451	2.9494
D1 to Z ↑	0.0193	0.0177	10.0539	5.4855
S0 to Z ↓	0.0157	0.0133	4.8531	3.0334
S0 to Z ↑	0.0177	0.0151	10.0271	5.3605
	X10_P4	**X16_P4**	**X10_P4**	**X16_P4**
D0 to Z ↓	0.0105	0.0096	1.4737	0.9635
D0 to Z ↑	0.0184	0.0175	2.4686	1.6313
D1 to Z ↓	0.0096	0.0093	1.4204	0.9365
D1 to Z ↑	0.0185	0.0180	2.5115	1.6495
S0 to Z ↓	0.0165	0.0142	1.4452	0.9491
S0 to Z ↑	0.0180	0.0155	2.4860	1.6393
	X21_P4		**X21_P4**	
D0 to Z ↓	0.0095		0.7375	
D0 to Z ↑	0.0172		1.2371	
D1 to Z ↓	0.0094		0.7118	
D1 to Z ↑	0.0181		1.2315	
S0 to Z ↓	0.0150		0.7237	
S0 to Z ↑	0.0160		1.2321	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P4	1.776e-05	1.476e-09
X5_P4	3.345e-05	1.642e-09
X10_P4	5.690e-05	2.635e-09
X16_P4	8.674e-05	3.464e-09
X21_P4	1.058e-04	4.292e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	2.401e-05	5.253e-05	1.531e-04	2.353e-04
D1 (output stable)	2.427e-05	5.574e-05	1.304e-04	2.255e-04
S0 (output stable)	1.417e-03	2.183e-03	3.444e-03	5.640e-03
D0 to Z	1.308e-03	2.191e-03	5.315e-03	7.522e-03
D1 to Z	1.310e-03	2.182e-03	5.096e-03	7.450e-03
S0 to Z	2.421e-03	3.738e-03	7.276e-03	1.073e-02
	X21_P4			
D0 (output stable)	3.046e-04			
D1 (output stable)	3.038e-04			
S0 (output stable)	6.189e-03			
D0 to Z	9.716e-03			
D1 to Z	9.874e-03			
S0 to Z	1.302e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	1.756e-07	2.179e-07	3.246e-07	7.589e-07
D1 (output stable)	1.976e-07	3.408e-07	3.228e-07	6.569e-07
S0 (output stable)	5.889e-06	2.620e-05	2.649e-05	5.919e-05
D0 to Z	5.296e-07	1.360e-06	1.678e-06	4.497e-06

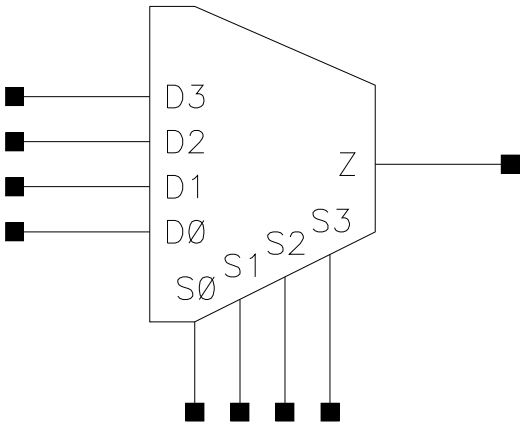
D1 to Z	5.714e-07	1.399e-06	2.610e-06	4.101e-06
S0 to Z	2.088e-06	1.049e-05	8.556e-06	2.041e-05
	X21_P4			
D0 (output stable)	1.024e-06			
D1 (output stable)	8.532e-07			
S0 (output stable)	8.381e-05			
D0 to Z	6.719e-06			
D1 to Z	6.219e-06			
S0 to Z	2.241e-05			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	1.768	2.1216
X27_P4	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P4	X27_P4
D0	0.0007	0.0022
D1	0.0007	0.0022
D2	0.0007	0.0021
D3	0.0007	0.0022
S0	0.0007	0.0020
S1	0.0008	0.0021
S2	0.0007	0.0020
S3	0.0008	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	X27_P4	X7_P4	X27_P4
D0 to Z ↓	0.0406	0.0345	2.5752	0.7065
D0 to Z ↑	0.0283	0.0242	2.4987	0.6258
D1 to Z ↓	0.0379	0.0325	2.5729	0.7059
D1 to Z ↑	0.0252	0.0210	2.4904	0.6231
D2 to Z ↓	0.0414	0.0336	2.5853	0.7077
D2 to Z ↑	0.0277	0.0227	2.5061	0.6277
D3 to Z ↓	0.0387	0.0316	2.5795	0.7062
D3 to Z ↑	0.0246	0.0195	2.4983	0.6246
S0 to Z ↓	0.0392	0.0326	2.5733	0.7062
S0 to Z ↑	0.0306	0.0260	2.4986	0.6254
S1 to Z ↓	0.0366	0.0305	2.5709	0.7057
S1 to Z ↑	0.0271	0.0224	2.4890	0.6233
S2 to Z ↓	0.0399	0.0315	2.5835	0.7068
S2 to Z ↑	0.0300	0.0244	2.5064	0.6273
S3 to Z ↓	0.0375	0.0296	2.5783	0.7054
S3 to Z ↑	0.0266	0.0209	2.4969	0.6248

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X7_P4	3.891e-05	2.635e-09
X27_P4	1.345e-04	4.954e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X7_P4	X27_P4
D0 (output stable)	6.813e-04	2.166e-03
D1 (output stable)	5.756e-04	1.815e-03
D2 (output stable)	6.277e-04	1.972e-03
D3 (output stable)	5.228e-04	1.617e-03
S0 (output stable)	6.593e-04	2.051e-03
S1 (output stable)	5.515e-04	1.719e-03
S2 (output stable)	6.061e-04	1.858e-03
S3 (output stable)	4.989e-04	1.522e-03
D0 to Z	5.419e-03	1.688e-02
D1 to Z	4.805e-03	1.485e-02
D2 to Z	5.281e-03	1.519e-02
D3 to Z	4.681e-03	1.317e-02
S0 to Z	5.281e-03	1.612e-02
S1 to Z	4.671e-03	1.417e-02
S2 to Z	5.140e-03	1.440e-02
S3 to Z	4.545e-03	1.246e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

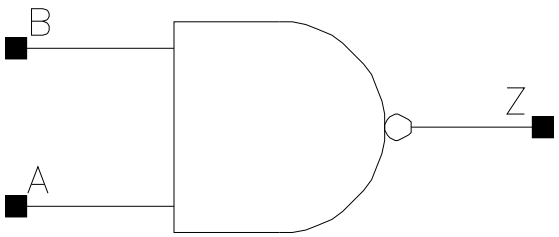
Pin Cycle (vdds)	X7_P4	X27_P4
D0 (output stable)	1.688e-07	4.536e-07
D1 (output stable)	9.381e-06	1.844e-05
D2 (output stable)	1.349e-07	5.026e-07
D3 (output stable)	9.029e-06	1.827e-05
S0 (output stable)	1.691e-07	4.805e-07
S1 (output stable)	9.543e-06	1.856e-05
S2 (output stable)	1.721e-07	5.271e-07
S3 (output stable)	9.289e-06	1.822e-05
D0 to Z	4.619e-07	1.338e-06
D1 to Z	1.344e-07	1.377e-06
D2 to Z	6.093e-07	1.652e-06
D3 to Z	1.520e-07	1.464e-06
S0 to Z	4.548e-07	1.493e-06
S1 to Z	9.837e-08	7.129e-07
S2 to Z	6.062e-07	1.620e-06
S3 to Z	1.210e-07	8.508e-07

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P4	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P4	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P4	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P4	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P4	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P4	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P4	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P4	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P4	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P4	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P4	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P4	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P4	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P4	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P4	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P4	C12T28SOI_LR_-NAND2X5_P4	C12T28SOI_LR_-NAND2X7_P4	C12T28SOI_LR_-NAND2X10_P4
A	0.0006	0.0008	0.0009	0.0015
B	0.0007	0.0008	0.0009	0.0014
	C12T28SOI_LR_-NAND2X13_P4	C12T28SOI_LR_-NAND2X17_P4	C12T28SOI_LR_-NAND2X20_P4	C12T28SOI_LR_-NAND2X24_P4
A	0.0019	0.0024	0.0028	0.0034
B	0.0018	0.0023	0.0027	0.0032
	C12T28SOI_LR_-NAND2X27_P4	C12T28SOI_LR_-NAND2X42_P4	C12T28SOI_LR_-NAND2X47_P4	C12T28SOI_LR_-NAND2X50_P4
A	0.0038	0.0011	0.0011	0.0011
B	0.0036	0.0011	0.0011	0.0012
	C12T28SOI_LR_-NAND2X58_P4	C12T28SOI_LR_-NAND2X67_P4	C12T28SOI_-LRBR0D8_-NAND2X7_P4	C12T28SOI_-LRBR0D8_-NAND2X14_P4
A	0.0011	0.0011	0.0009	0.0019
B	0.0012	0.0011	0.0010	0.0018
	C12T28SOI_LRS_-NAND2X40_P4	C12T28SOI_LRS_-NAND2X54_P4		
A	0.0057	0.0076		
B	0.0054	0.0073		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P4	**C12T28SOI_LR_-NAND2X5_P4**	**C12T28SOI_LR_-NAND2X3_P4**	**C12T28SOI_LR_-NAND2X5_P4**
A to Z ↓	0.0067	0.0058	4.7846	3.1385
A to Z ↑	0.0128	0.0117	4.8070	3.1378
B to Z ↓	0.0075	0.0065	4.8618	3.1865
B to Z ↑	0.0113	0.0102	4.8432	3.1611
	C12T28SOI_LR_-NAND2X7_P4	**C12T28SOI_LR_-NAND2X10_P4**	**C12T28SOI_LR_-NAND2X7_P4**	**C12T28SOI_LR_-NAND2X10_P4**
A to Z ↓	0.0058	0.0066	2.6516	1.7506
A to Z ↑	0.0114	0.0122	2.5520	1.6600
B to Z ↓	0.0064	0.0065	2.6863	1.7745
B to Z ↑	0.0098	0.0097	2.5778	1.6729
	C12T28SOI_LR_-NAND2X13_P4	**C12T28SOI_LR_-NAND2X17_P4**	**C12T28SOI_LR_-NAND2X13_P4**	**C12T28SOI_LR_-NAND2X17_P4**
A to Z ↓	0.0064	0.0062	1.3600	1.0721

A to Z ↑	0.0116	0.0117	1.2592	1.0069
B to Z ↓	0.0063	0.0066	1.3778	1.0858
B to Z ↑	0.0092	0.0096	1.2694	1.0149
	C12T28SOI_LR_-NAND2X20_P4	**C12T28SOI_LR_-NAND2X24_P4**	**C12T28SOI_LR_-NAND2X20_P4**	**C12T28SOI_LR_-NAND2X24_P4**
A to Z ↓	0.0062	0.0063	0.9297	0.7891
A to Z ↑	0.0113	0.0115	0.8480	0.7198
B to Z ↓	0.0067	0.0064	0.9418	0.7993
B to Z ↑	0.0093	0.0092	0.8556	0.7255
	C12T28SOI_LR_-NAND2X27_P4	**C12T28SOI_LR_-NAND2X42_P4**	**C12T28SOI_LR_-NAND2X27_P4**	**C12T28SOI_LR_-NAND2X42_P4**
A to Z ↓	0.0062	0.0281	0.7059	0.3345
A to Z ↑	0.0112	0.0313	0.6362	0.4972
B to Z ↓	0.0063	0.0294	0.7153	0.3344
B to Z ↑	0.0089	0.0300	0.6414	0.4978
	C12T28SOI_LR_-NAND2X47_P4	**C12T28SOI_LR_-NAND2X50_P4**	**C12T28SOI_LR_-NAND2X47_P4**	**C12T28SOI_LR_-NAND2X50_P4**
A to Z ↓	0.0290	0.0292	0.2968	0.2790
A to Z ↑	0.0318	0.0320	0.4314	0.4154
B to Z ↓	0.0303	0.0306	0.2968	0.2790
B to Z ↑	0.0305	0.0308	0.4318	0.4152
	C12T28SOI_LR_-NAND2X58_P4	**C12T28SOI_LR_-NAND2X67_P4**	**C12T28SOI_LR_-NAND2X58_P4**	**C12T28SOI_LR_-NAND2X67_P4**
A to Z ↓	0.0307	0.0318	0.2419	0.2128
A to Z ↑	0.0332	0.0340	0.3571	0.3141
B to Z ↓	0.0321	0.0331	0.2417	0.2126
B to Z ↑	0.0319	0.0327	0.3574	0.3139
	C12T28SOI_-LRBR0D8_-NAND2X7_P4	**C12T28SOI_-LRBR0D8_-NAND2X14_P4**	**C12T28SOI_-LRBR0D8_-NAND2X7_P4**	**C12T28SOI_-LRBR0D8_-NAND2X14_P4**
A to Z ↓	0.0037	0.0044	2.0216	1.0673
A to Z ↑	0.0142	0.0143	3.3472	1.6416
B to Z ↓	0.0039	0.0036	2.0624	1.0894
B to Z ↑	0.0118	0.0108	3.4616	1.6740
	C12T28SOI_LRS_-NAND2X40_P4	**C12T28SOI_LRS_-NAND2X54_P4**	**C12T28SOI_LRS_-NAND2X40_P4**	**C12T28SOI_LRS_-NAND2X54_P4**
A to Z ↓	0.0062	0.0063	0.4785	0.3624
A to Z ↑	0.0111	0.0112	0.4264	0.3216
B to Z ↓	0.0064	0.0066	0.4852	0.3672
B to Z ↑	0.0088	0.0090	0.4302	0.3245

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P4	8.366e-06	9.792e-10
C12T28SOI_LR_NAND2X5_P4	1.278e-05	9.792e-10
C12T28SOI_LR_NAND2X7_P4	1.493e-05	9.792e-10
C12T28SOI_LR_NAND2X10_P4	2.194e-05	1.310e-09
C12T28SOI_LR_NAND2X13_P4	2.766e-05	1.310e-09
C12T28SOI_LR_NAND2X17_P4	3.504e-05	1.642e-09
C12T28SOI_LR_NAND2X20_P4	3.951e-05	1.642e-09
C12T28SOI_LR_NAND2X24_P4	4.808e-05	1.973e-09
C12T28SOI_LR_NAND2X27_P4	5.141e-05	1.973e-09

C12T28SOI_LR_NAND2X42_P4	1.057e-04	2.139e-09
C12T28SOI_LR_NAND2X47_P4	1.196e-04	2.304e-09
C12T28SOI_LR_NAND2X50_P4	1.192e-04	2.304e-09
C12T28SOI_LR_NAND2X58_P4	1.326e-04	2.470e-09
C12T28SOI_LR_NAND2X67_P4	1.461e-04	2.635e-09
C12T28SOI_LRBR0D8_NAND2X7_P4	1.705e-05	1.804e-09
C12T28SOI_LRBR0D8_NAND2X14_-P4	3.127e-05	2.156e-09
C12T28SOI_LRS_NAND2X40_P4	7.521e-05	2.635e-09
C12T28SOI_LRS_NAND2X54_P4	9.903e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P4	C12T28SOI_LR_-NAND2X5_P4	C12T28SOI_LR_-NAND2X7_P4	C12T28SOI_LR_-NAND2X10_P4
A (output stable)	1.785e-05	2.728e-05	3.239e-05	1.038e-04
B (output stable)	2.465e-05	3.761e-05	4.597e-05	2.400e-04
A to Z	1.037e-03	1.447e-03	1.733e-03	2.874e-03
B to Z	9.053e-04	1.253e-03	1.489e-03	2.292e-03
	C12T28SOI_LR_-NAND2X13_P4	C12T28SOI_LR_-NAND2X17_P4	C12T28SOI_LR_-NAND2X20_P4	C12T28SOI_LR_-NAND2X24_P4
A (output stable)	1.236e-04	1.480e-04	1.646e-04	2.224e-04
B (output stable)	2.726e-04	2.741e-04	3.151e-04	4.529e-04
A to Z	3.596e-03	4.539e-03	5.214e-03	6.281e-03
B to Z	2.894e-03	3.739e-03	4.312e-03	5.068e-03
	C12T28SOI_LR_-NAND2X27_P4	C12T28SOI_LR_-NAND2X42_P4	C12T28SOI_LR_-NAND2X47_P4	C12T28SOI_LR_-NAND2X50_P4
A (output stable)	2.417e-04	3.611e-05	3.647e-05	3.671e-05
B (output stable)	4.867e-04	4.993e-05	5.024e-05	5.054e-05
A to Z	6.868e-03	1.545e-02	1.692e-02	1.742e-02
B to Z	5.519e-03	1.520e-02	1.668e-02	1.719e-02
	C12T28SOI_LR_-NAND2X58_P4	C12T28SOI_LR_-NAND2X67_P4	C12T28SOI_-LRBR0D8_-NAND2X7_P4	C12T28SOI_-LRBR0D8_-NAND2X14_P4
A (output stable)	3.691e-05	3.709e-05	4.253e-05	1.548e-04
B (output stable)	5.066e-05	5.084e-05	6.031e-05	3.508e-04
A to Z	1.993e-02	2.230e-02	1.749e-03	3.631e-03
B to Z	1.970e-02	2.206e-02	1.406e-03	2.665e-03
	C12T28SOI_LRS_-NAND2X40_P4	C12T28SOI_LRS_-NAND2X54_P4		
A (output stable)	3.570e-04	4.625e-04		
B (output stable)	6.660e-04	8.627e-04		
A to Z	1.018e-02	1.356e-02		
B to Z	8.194e-03	1.097e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P4	C12T28SOI_LR_-NAND2X5_P4	C12T28SOI_LR_-NAND2X7_P4	C12T28SOI_LR_-NAND2X10_P4
A (output stable)	7.300e-08	6.040e-08	5.235e-08	2.230e-08
B (output stable)	8.350e-08	7.290e-08	6.517e-08	-5.600e-09
A to Z	4.447e-07	7.867e-07	6.339e-07	1.556e-06
B to Z	3.963e-07	8.369e-07	-2.800e-08	1.502e-06

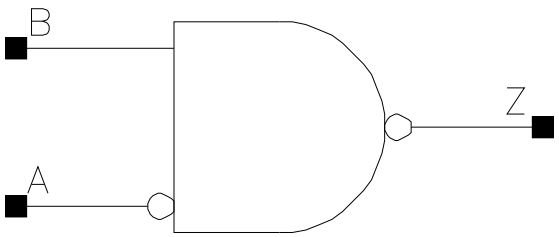
	C12T28SOI_LR_-NAND2X13_P4	C12T28SOI_LR_-NAND2X17_P4	C12T28SOI_LR_-NAND2X20_P4	C12T28SOI_LR_-NAND2X24_P4
A (output stable)	2.610e-08	-3.200e-08	-2.910e-08	-9.410e-08
B (output stable)	-1.960e-08	-3.840e-08	-2.040e-08	-1.163e-07
A to Z	1.218e-06	1.458e-06	2.552e-06	3.219e-06
B to Z	1.468e-06	2.030e-06	-7.380e-07	2.205e-06
	C12T28SOI_LR_-NAND2X27_P4	C12T28SOI_LR_-NAND2X42_P4	C12T28SOI_LR_-NAND2X47_P4	C12T28SOI_LR_-NAND2X50_P4
A (output stable)	-1.220e-07	6.690e-08	6.733e-08	6.781e-08
B (output stable)	-1.403e-07	7.430e-08	7.503e-08	7.512e-08
A to Z	3.499e-06	1.040e-07	1.440e-07	1.040e-07
B to Z	3.199e-06	-1.790e-07	-1.740e-07	-2.100e-07
	C12T28SOI_LR_-NAND2X58_P4	C12T28SOI_LR_-NAND2X67_P4	C12T28SOI_-LRBR0D8_-NAND2X7_P4	C12T28SOI_-LRBR0D8_-NAND2X14_P4
A (output stable)	6.805e-08	6.832e-08	6.809e-08	1.520e-08
B (output stable)	7.524e-08	7.606e-08	7.620e-08	-1.283e-07
A to Z	8.900e-08	6.000e-08	4.198e-07	1.190e-06
B to Z	-1.680e-07	-2.660e-07	1.054e-06	3.160e-07
	C12T28SOI_LRS_-NAND2X40_P4	C12T28SOI_LRS_-NAND2X54_P4		
A (output stable)	-1.768e-07	-2.678e-07		
B (output stable)	-2.603e-07	-3.662e-07		
A to Z	5.277e-06	6.689e-06		
B to Z	4.696e-06	7.544e-06		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X7_P4	1.200	0.544	0.6528
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X40_P4	1.200	2.312	2.7744
X54_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P4	X7_P4	X13_P4	X27_P4
A	0.0008	0.0009	0.0011	0.0022
B	0.0007	0.0009	0.0017	0.0036
	X40_P4	X54_P4		
A	0.0032	0.0042		
B	0.0053	0.0072		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0218	0.0232	4.7087	2.6235
A to Z ↑	0.0160	0.0169	4.6394	2.5040
B to Z ↓	0.0077	0.0065	4.8964	2.7041
B to Z ↑	0.0114	0.0097	4.8441	2.6002
	X13_P4	**X27_P4**	**X13_P4**	**X27_P4**

A to Z ↓	0.0218	0.0214	1.4197	0.7042
A to Z ↑	0.0162	0.0159	1.2897	0.6254
B to Z ↓	0.0063	0.0062	1.4649	0.7273
B to Z ↑	0.0091	0.0088	1.2971	0.6421
	X40_P4	**X54_P4**	**X40_P4**	**X54_P4**
A to Z ↓	0.0216	0.0215	0.4698	0.3565
A to Z ↑	0.0163	0.0161	0.4166	0.3142
B to Z ↓	0.0063	0.0064	0.4849	0.3677
B to Z ↑	0.0088	0.0088	0.4316	0.3259

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P4	1.555e-05	1.145e-09
X7_P4	2.197e-05	1.145e-09
X13_P4	4.340e-05	1.642e-09
X27_P4	7.903e-05	2.470e-09
X40_P4	1.142e-04	3.298e-09
X54_P4	1.493e-04	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	1.527e-03	1.875e-03	3.153e-03	6.215e-03
B (output stable)	2.521e-05	4.612e-05	2.529e-04	4.373e-04
A to Z	2.468e-03	3.376e-03	6.207e-03	1.227e-02
B to Z	9.107e-04	1.475e-03	2.839e-03	5.590e-03
	X40_P4	X54_P4		
A (output stable)	9.437e-03	1.229e-02		
B (output stable)	6.296e-04	8.410e-04		
A to Z	1.850e-02	2.429e-02		
B to Z	8.221e-03	1.088e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

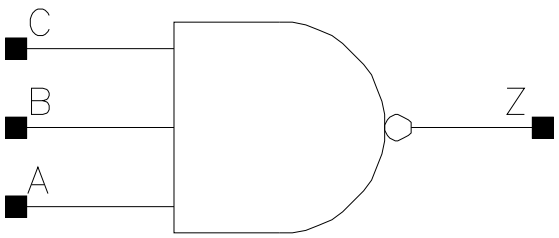
Pin Cycle (vdds)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	1.728e-07	1.309e-07	9.680e-08	-1.022e-07
B (output stable)	8.450e-08	6.530e-08	2.340e-08	-1.169e-07
A to Z	1.146e-06	1.022e-06	2.678e-06	4.938e-06
B to Z	1.807e-07	-1.110e-07	1.854e-06	6.600e-07
	X40_P4	X54_P4		
A (output stable)	8.700e-08	-3.510e-07		
B (output stable)	-2.850e-07	-3.459e-07		
A to Z	-9.000e-09	-1.282e-06		
B to Z	4.376e-06	5.755e-06		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P4	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P4	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P4	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P4	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P4	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P4	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P4	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P4	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P4	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P4	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P4	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P4	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P4	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P4	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P4	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A	0.0008	0.0009	0.0015	0.0019
B	0.0008	0.0010	0.0015	0.0018
C	0.0007	0.0009	0.0014	0.0018
	C12T28SOI_LR_-NAND3X15_P4	C12T28SOI_LR_-NAND3X18_P4	C12T28SOI_LR_-NAND3X21_P4	C12T28SOI_LR_-NAND3X24_P4
A	0.0024	0.0028	0.0034	0.0037
B	0.0023	0.0027	0.0033	0.0036
C	0.0023	0.0026	0.0031	0.0035
	C12T28SOI_LR_-NAND3X35_P4	C12T28SOI_LR_-NAND3X47_P4	C12T28SOI_-LRBR0P6_-NAND3X6_P4	C12T28SOI_-LRBR0P6_-NAND3X12_P4
A	0.0057	0.0075	0.0009	0.0019
B	0.0054	0.0073	0.0010	0.0018
C	0.0053	0.0070	0.0009	0.0018
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	C12T28SOI_-LRBR0P6_-NAND3X24_P4	C12T28SOI_-LRBR0P6_-NAND3X35_P4	C12T28SOI_-LRBR0P6_-NAND3X47_P4
A	0.0028	0.0037	0.0055	0.0074
B	0.0026	0.0036	0.0053	0.0072
C	0.0025	0.0035	0.0052	0.0070
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4			
A	0.0028			
B	0.0028			
C	0.0026			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4
A to Z ↓	0.0111	0.0099	4.9918	3.6089
A to Z ↑	0.0160	0.0146	3.5543	2.4881
B to Z ↓	0.0122	0.0108	5.0164	3.6266
B to Z ↑	0.0152	0.0136	3.5657	2.4945
C to Z ↓	0.0114	0.0103	5.0426	3.6462
C to Z ↑	0.0129	0.0116	3.5688	2.5118

	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A to Z ↓	0.0111	0.0104	2.4363	1.9157
A to Z ↑	0.0153	0.0144	1.6731	1.2744
B to Z ↓	0.0110	0.0104	2.4477	1.9249
B to Z ↑	0.0138	0.0130	1.6766	1.2777
C to Z ↓	0.0104	0.0100	2.4609	1.9352
C to Z ↑	0.0115	0.0108	1.6718	1.2684
	C12T28SOI_LR_-NAND3X15_P4	**C12T28SOI_LR_-NAND3X18_P4**	**C12T28SOI_LR_-NAND3X15_P4**	**C12T28SOI_LR_-NAND3X18_P4**
A to Z ↓	0.0099	0.0097	1.5258	1.3209
A to Z ↑	0.0141	0.0137	1.0086	0.8471
B to Z ↓	0.0104	0.0103	1.5338	1.3272
B to Z ↑	0.0126	0.0123	1.0125	0.8502
C to Z ↓	0.0100	0.0099	1.5423	1.3340
C to Z ↑	0.0107	0.0103	1.0195	0.8559
	C12T28SOI_LR_-NAND3X21_P4	**C12T28SOI_LR_-NAND3X24_P4**	**C12T28SOI_LR_-NAND3X21_P4**	**C12T28SOI_LR_-NAND3X24_P4**
A to Z ↓	0.0102	0.0101	1.1173	1.0021
A to Z ↑	0.0142	0.0139	0.7252	0.6415
B to Z ↓	0.0105	0.0103	1.1225	1.0069
B to Z ↑	0.0128	0.0125	0.7269	0.6429
C to Z ↓	0.0101	0.0100	1.1283	1.0121
C to Z ↑	0.0107	0.0105	0.7282	0.6433
	C12T28SOI_LR_-NAND3X35_P4	**C12T28SOI_LR_-NAND3X47_P4**	**C12T28SOI_LR_-NAND3X35_P4**	**C12T28SOI_LR_-NAND3X47_P4**
A to Z ↓	0.0096	0.0099	0.6836	0.5208
A to Z ↑	0.0136	0.0138	0.4304	0.3254
B to Z ↓	0.0100	0.0104	0.6873	0.5235
B to Z ↑	0.0121	0.0123	0.4306	0.3246
C to Z ↓	0.0097	0.0101	0.6911	0.5263
C to Z ↑	0.0100	0.0101	0.4329	0.3259
	C12T28SOI_-LRBR0P6_-NAND3X6_P4	**C12T28SOI_-LRBR0P6_-NAND3X12_P4**	**C12T28SOI_-LRBR0P6_-NAND3X6_P4**	**C12T28SOI_-LRBR0P6_-NAND3X12_P4**
A to Z ↓	0.0069	0.0073	2.4770	1.3114
A to Z ↑	0.0207	0.0206	3.8261	1.9530
B to Z ↓	0.0071	0.0065	2.5036	1.3263
B to Z ↑	0.0186	0.0177	3.8385	1.9581
C to Z ↓	0.0057	0.0050	2.5379	1.3452
C to Z ↑	0.0146	0.0135	3.8594	1.9662
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	**C12T28SOI_-LRBR0P6_-NAND3X24_P4**	**C12T28SOI_-LRBR0P6_-NAND3X18_P4**	**C12T28SOI_-LRBR0P6_-NAND3X24_P4**
A to Z ↓	0.0066	0.0069	0.9048	0.6858
A to Z ↑	0.0196	0.0199	1.3012	0.9837
B to Z ↓	0.0063	0.0063	0.9152	0.6937
B to Z ↑	0.0167	0.0171	1.3060	0.9860
C to Z ↓	0.0051	0.0050	0.9266	0.7031
C to Z ↑	0.0130	0.0130	1.3149	0.9862
	C12T28SOI_-LRBR0P6_-NAND3X35_P4	**C12T28SOI_-LRBR0P6_-NAND3X47_P4**	**C12T28SOI_-LRBR0P6_-NAND3X35_P4**	**C12T28SOI_-LRBR0P6_-NAND3X47_P4**

A to Z ↓	0.0066	0.0068	0.4688	0.3585
A to Z ↑	0.0199	0.0201	0.6766	0.5123
B to Z ↓	0.0062	0.0063	0.4747	0.3628
B to Z ↑	0.0170	0.0171	0.6776	0.5122
C to Z ↓	0.0050	0.0054	0.4813	0.3674
C to Z ↑	0.0129	0.0132	0.6836	0.5139
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P4**	
A to Z ↓	0.0073		0.8869	
A to Z ↑	0.0199		1.2494	
B to Z ↓	0.0064		0.8961	
B to Z ↑	0.0170		1.2520	
C to Z ↓	0.0049		0.9081	
C to Z ↑	0.0128		1.2424	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P4	9.650e-06	1.310e-09
C12T28SOI_LR_NAND3X6_P4	1.331e-05	1.310e-09
C12T28SOI_LR_NAND3X9_P4	1.901e-05	1.807e-09
C12T28SOI_LR_NAND3X12_P4	2.389e-05	1.807e-09
C12T28SOI_LR_NAND3X15_P4	2.856e-05	2.139e-09
C12T28SOI_LR_NAND3X18_P4	3.232e-05	2.139e-09
C12T28SOI_LR_NAND3X21_P4	4.103e-05	2.801e-09
C12T28SOI_LR_NAND3X24_P4	4.398e-05	2.801e-09
C12T28SOI_LR_NAND3X35_P4	6.402e-05	3.795e-09
C12T28SOI_LR_NAND3X47_P4	8.404e-05	4.789e-09
C12T28SOI_LRBR0P6_NAND3X6_P4	1.599e-05	2.248e-09
C12T28SOI_LRBR0P6_NAND3X12_-P4	2.932e-05	2.790e-09
C12T28SOI_LRBR0P6_NAND3X18_-P4	3.960e-05	3.151e-09
C12T28SOI_LRBR0P6_NAND3X24_-P4	5.500e-05	3.874e-09
C12T28SOI_LRBR0P6_NAND3X35_-P4	8.071e-05	4.958e-09
C12T28SOI_LRBR0P6_NAND3X47_-P4	1.064e-04	6.042e-09
C12T28SOIDV_LRBR0P6_-NAND3X18_P4	4.672e-05	2.606e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A (output stable)	3.644e-05	4.840e-05	1.128e-04	1.322e-04
B (output stable)	5.984e-05	7.467e-05	1.666e-04	1.980e-04
C (output stable)	2.312e-04	2.704e-04	4.374e-04	5.048e-04
A to Z	2.036e-03	2.556e-03	4.095e-03	4.942e-03
B to Z	1.837e-03	2.270e-03	3.437e-03	4.159e-03
C to Z	1.532e-03	1.922e-03	2.839e-03	3.471e-03

	C12T28SOI_LR_-NAND3X15_P4	C12T28SOI_LR_-NAND3X18_P4	C12T28SOI_LR_-NAND3X21_P4	C12T28SOI_LR_-NAND3X24_P4
A (output stable)	1.486e-04	1.675e-04	2.286e-04	2.491e-04
B (output stable)	2.217e-04	2.594e-04	3.427e-04	3.770e-04
C (output stable)	5.456e-04	6.168e-04	8.343e-04	9.018e-04
A to Z	6.007e-03	6.853e-03	8.498e-03	9.356e-03
B to Z	5.056e-03	5.777e-03	7.160e-03	7.872e-03
C to Z	4.284e-03	4.861e-03	5.982e-03	6.562e-03
	C12T28SOI_LR_-NAND3X35_P4	C12T28SOI_LR_-NAND3X47_P4	C12T28SOI_-LRBR0P6_-NAND3X6_P4	C12T28SOI_-LRBR0P6_-NAND3X12_P4
A (output stable)	3.427e-04	4.554e-04	6.971e-05	1.890e-04
B (output stable)	5.277e-04	6.971e-04	1.089e-04	2.891e-04
C (output stable)	1.323e-03	1.684e-03	3.700e-04	7.258e-04
A to Z	1.344e-02	1.801e-02	2.709e-03	5.301e-03
B to Z	1.123e-02	1.512e-02	2.268e-03	4.118e-03
C to Z	9.222e-03	1.253e-02	1.703e-03	2.973e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	C12T28SOI_-LRBR0P6_-NAND3X24_P4	C12T28SOI_-LRBR0P6_-NAND3X35_P4	C12T28SOI_-LRBR0P6_-NAND3X47_P4
A (output stable)	2.383e-04	3.539e-04	4.858e-04	6.445e-04
B (output stable)	3.694e-04	5.395e-04	7.335e-04	9.784e-04
C (output stable)	8.440e-04	1.308e-03	1.867e-03	2.432e-03
A to Z	7.274e-03	9.991e-03	1.454e-02	1.928e-02
B to Z	5.650e-03	7.767e-03	1.126e-02	1.494e-02
C to Z	4.221e-03	5.643e-03	8.092e-03	1.082e-02
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4			
A (output stable)	2.742e-04			
B (output stable)	4.261e-04			
C (output stable)	1.016e-03			
A to Z	7.862e-03			
B to Z	6.138e-03			
C to Z	4.449e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A (output stable)	8.107e-08	6.254e-08	5.047e-08	4.320e-08
B (output stable)	9.002e-08	7.179e-08	-7.137e-08	4.852e-08
C (output stable)	9.663e-08	9.007e-08	-7.909e-07	3.100e-08
A to Z	8.300e-07	1.707e-06	1.707e-06	2.759e-06
B to Z	4.610e-07	1.315e-06	-4.700e-08	1.574e-06
C to Z	-6.400e-08	-4.210e-07	3.100e-07	-3.320e-07
	C12T28SOI_LR_-NAND3X15_P4	C12T28SOI_LR_-NAND3X18_P4	C12T28SOI_LR_-NAND3X21_P4	C12T28SOI_LR_-NAND3X24_P4
A (output stable)	2.033e-09	-2.430e-08	-6.893e-08	-4.843e-08
B (output stable)	-1.182e-07	-1.306e-07	-4.090e-07	-3.015e-07
C (output stable)	-5.316e-07	-5.510e-07	-1.664e-06	-1.226e-06
A to Z	3.385e-06	3.880e-06	4.730e-06	3.569e-06
B to Z	1.722e-06	8.910e-07	2.395e-06	9.410e-07

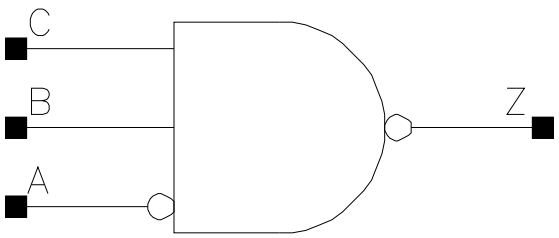
C to Z	-3.260e-07	-6.470e-07	-5.710e-07	-6.970e-07
	C12T28SOI_LR_-NAND3X35_P4	C12T28SOI_LR_-NAND3X47_P4	C12T28SOI_-LRBR0P6_-NAND3X6_P4	C12T28SOI_-LRBR0P6_-NAND3X12_P4
A (output stable)	-1.594e-07	-1.890e-07	7.572e-08	3.307e-08
B (output stable)	-4.960e-07	-9.207e-07	-9.223e-08	-4.445e-07
C (output stable)	-1.936e-06	-2.736e-06	-1.637e-06	-2.498e-06
A to Z	7.121e-06	9.257e-06	1.076e-06	1.508e-06
B to Z	4.835e-06	1.404e-06	4.230e-07	1.899e-06
C to Z	-1.013e-06	-2.040e-06	1.790e-06	3.540e-07
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	C12T28SOI_-LRBR0P6_-NAND3X24_P4	C12T28SOI_-LRBR0P6_-NAND3X35_P4	C12T28SOI_-LRBR0P6_-NAND3X47_P4
A (output stable)	3.043e-08	-8.567e-09	-4.333e-08	-5.480e-08
B (output stable)	2.067e-08	-7.183e-07	-4.743e-07	-7.000e-07
C (output stable)	4.293e-08	-3.005e-06	-2.246e-06	-2.864e-06
A to Z	2.001e-06	2.702e-06	3.297e-06	3.044e-06
B to Z	2.732e-06	3.406e-06	4.536e-06	5.761e-06
C to Z	1.825e-06	1.715e-06	2.723e-06	6.445e-06
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4			
A (output stable)	3.227e-08			
B (output stable)	2.720e-08			
C (output stable)	1.280e-08			
A to Z	2.248e-06			
B to Z	1.933e-06			
C to Z	2.059e-06			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.816	0.9792
X12_P4	1.200	1.224	1.4688
X18_P4	1.200	1.496	1.7952
X24_P4	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0008	0.0012	0.0012	0.0021
B	0.0009	0.0018	0.0027	0.0036
C	0.0009	0.0018	0.0026	0.0035

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X12_P4**	**X6_P4**	**X12_P4**
A to Z ↓	0.0260	0.0253	3.5829	1.9245
A to Z ↑	0.0183	0.0179	2.4369	1.2239
B to Z ↓	0.0097	0.0098	3.6277	1.9489
B to Z ↑	0.0125	0.0123	2.5043	1.2633
C to Z ↓	0.0100	0.0092	3.6503	1.9589
C to Z ↑	0.0109	0.0100	2.5195	1.2730
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0291	0.0248	1.3180	1.0005

A to Z ↑	0.0210	0.0171	0.8251	0.6186
B to Z ↓	0.0102	0.0099	1.3317	1.0124
B to Z ↑	0.0122	0.0121	0.8511	0.6400
C to Z ↓	0.0100	0.0094	1.3381	1.0178
C to Z ↑	0.0104	0.0098	0.8569	0.6448

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P4	1.928e-05	1.476e-09
X12_P4	3.757e-05	1.973e-09
X18_P4	4.561e-05	2.304e-09
X24_P4	7.275e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	1.829e-03	3.341e-03	4.382e-03	6.332e-03
B (output stable)	5.399e-05	1.729e-04	2.780e-04	3.849e-04
C (output stable)	1.102e-04	5.078e-04	6.329e-04	9.418e-04
A to Z	3.995e-03	7.796e-03	1.119e-02	1.510e-02
B to Z	2.006e-03	3.862e-03	5.766e-03	7.484e-03
C to Z	1.764e-03	3.137e-03	4.863e-03	6.094e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

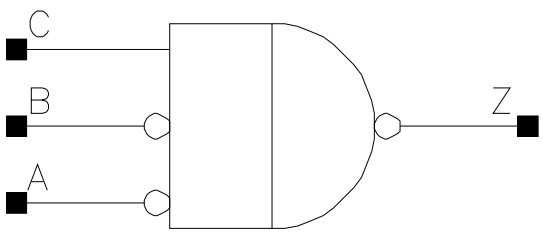
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	1.411e-07	1.891e-07	7.530e-08	2.027e-07
B (output stable)	7.279e-08	-7.104e-08	-1.520e-08	-3.539e-07
C (output stable)	7.653e-08	-6.551e-07	-3.010e-08	-1.296e-06
A to Z	1.644e-06	2.448e-06	1.967e-06	5.176e-06
B to Z	2.260e-07	1.682e-06	2.375e-06	3.710e-06
C to Z	1.920e-07	-1.000e-08	-1.640e-07	-1.510e-07

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	0.816	0.9792
X13_P4	1.200	1.088	1.3056
X20_P4	1.200	1.632	1.9584
X27_P4	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P4	X13_P4	X20_P4	X27_P4
A	0.0010	0.0010	0.0021	0.0020
B	0.0012	0.0011	0.0022	0.0020
C	0.0009	0.0018	0.0026	0.0036

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	**X13_P4**	**X7_P4**	**X13_P4**
A to Z ↓	0.0243	0.0295	2.5255	1.3463
A to Z ↑	0.0155	0.0183	2.4130	1.2168
B to Z ↓	0.0254	0.0309	2.5283	1.3466
B to Z ↑	0.0144	0.0171	2.4136	1.2158
C to Z ↓	0.0063	0.0061	2.5981	1.3795
C to Z ↑	0.0097	0.0090	2.5050	1.2681
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0271	0.0298	0.9181	0.7002
A to Z ↑	0.0169	0.0207	0.8216	0.6165
B to Z ↓	0.0268	0.0298	0.9184	0.7000

B to Z ↑	0.0152	0.0192	0.8201	0.6162
C to Z ↓	0.0069	0.0066	0.9421	0.7173
C to Z ↑	0.0096	0.0092	0.8550	0.6421

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X7_P4	2.916e-05	1.476e-09
X13_P4	3.995e-05	1.807e-09
X20_P4	6.225e-05	2.470e-09
X27_P4	6.931e-05	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	1.031e-03	1.347e-03	2.311e-03	2.676e-03
B (output stable)	9.301e-04	1.241e-03	2.035e-03	2.402e-03
C (output stable)	5.024e-05	2.927e-04	3.011e-04	3.731e-04
A to Z	4.508e-03	7.355e-03	1.156e-02	1.448e-02
B to Z	4.184e-03	6.999e-03	1.050e-02	1.344e-02
C to Z	1.540e-03	2.857e-03	4.461e-03	5.878e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

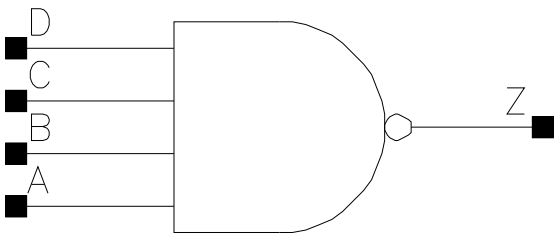
Pin Cycle (vdds)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	4.283e-07	2.694e-07	7.653e-07	4.536e-07
B (output stable)	3.273e-06	3.142e-06	4.140e-05	4.144e-05
C (output stable)	6.401e-08	2.240e-08	-3.293e-08	-7.480e-08
A to Z	2.151e-06	4.070e-07	5.482e-06	1.503e-06
B to Z	-4.494e-08	1.810e-06	4.600e-08	1.611e-06
C to Z	1.159e-06	1.319e-06	-8.370e-07	2.904e-06

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0007	0.0007	0.0008	0.0011
B	0.0008	0.0008	0.0009	0.0011
C	0.0007	0.0008	0.0009	0.0011
D	0.0007	0.0007	0.0010	0.0012

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0363	0.0364	1.6290	0.8135
A to Z ↑	0.0318	0.0345	2.4743	1.2256
B to Z ↓	0.0377	0.0383	1.6291	0.8137
B to Z ↑	0.0305	0.0337	2.4726	1.2255
C to Z ↓	0.0367	0.0359	1.6303	0.8130
C to Z ↑	0.0326	0.0355	2.4718	1.2240

D to Z ↓	0.0383	0.0374	1.6292	0.8137
D to Z ↑	0.0316	0.0341	2.4721	1.2246
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0386	0.0359	0.5612	0.4193
A to Z ↑	0.0335	0.0332	0.8270	0.6203
B to Z ↓	0.0402	0.0371	0.5613	0.4195
B to Z ↑	0.0324	0.0319	0.8271	0.6200
C to Z ↓	0.0358	0.0332	0.5612	0.4192
C to Z ↑	0.0337	0.0332	0.8254	0.6190
D to Z ↓	0.0373	0.0346	0.5611	0.4193
D to Z ↑	0.0324	0.0318	0.8260	0.6191

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	3.974e-05	1.973e-09
X17_P4	6.068e-05	2.304e-09
X25_P4	8.576e-05	2.801e-09
X33_P4	1.091e-04	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	7.367e-04	9.052e-04	1.312e-03	1.582e-03
B (output stable)	6.853e-04	8.570e-04	1.237e-03	1.485e-03
C (output stable)	7.302e-04	8.580e-04	1.310e-03	1.517e-03
D (output stable)	6.745e-04	8.005e-04	1.224e-03	1.416e-03
A to Z	5.386e-03	8.232e-03	1.279e-02	1.569e-02
B to Z	5.257e-03	8.099e-03	1.258e-02	1.543e-02
C to Z	5.490e-03	8.079e-03	1.207e-02	1.467e-02
D to Z	5.363e-03	7.932e-03	1.185e-02	1.441e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

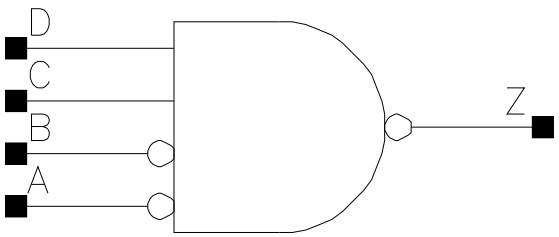
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	3.902e-07	6.333e-07	7.160e-07	1.112e-06
B (output stable)	3.772e-07	4.736e-07	6.338e-07	1.061e-06
C (output stable)	2.062e-06	2.140e-06	2.045e-05	2.155e-05
D (output stable)	1.974e-06	2.234e-06	2.065e-05	2.132e-05
A to Z	1.138e-06	1.735e-06	2.575e-06	4.327e-06
B to Z	2.721e-07	1.359e-06	1.483e-06	2.901e-06
C to Z	4.530e-08	-3.084e-07	-7.960e-07	-1.002e-06
D to Z	-2.653e-07	-2.389e-07	-5.950e-07	-1.043e-06

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X12_P4	1.200	1.496	1.7952
X18_P4	1.200	2.040	2.4480
X24_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0011	0.0011	0.0021	0.0019
B	0.0011	0.0016	0.0022	0.0020
C	0.0009	0.0018	0.0026	0.0036
D	0.0009	0.0018	0.0026	0.0036

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X12_P4	X6_P4	X12_P4
A to Z ↓	0.0258	0.0341	3.6939	1.9301
A to Z ↑	0.0166	0.0207	2.4175	1.2197
B to Z ↓	0.0264	0.0349	3.6935	1.9301
B to Z ↑	0.0148	0.0193	2.4170	1.2182
C to Z ↓	0.0098	0.0098	3.7369	1.9478
C to Z ↑	0.0126	0.0122	2.6522	1.2630

D to Z ↓	0.0098	0.0091	3.7584	1.9579
D to Z ↑	0.0110	0.0099	2.6687	1.2724
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0300	0.0335	1.3156	1.0018
A to Z ↑	0.0182	0.0237	0.8225	0.6178
B to Z ↓	0.0298	0.0333	1.3154	1.0018
B to Z ↑	0.0165	0.0221	0.8214	0.6167
C to Z ↓	0.0100	0.0103	1.3281	1.0103
C to Z ↑	0.0121	0.0123	0.8543	0.6380
D to Z ↓	0.0097	0.0099	1.3350	1.0155
D to Z ↑	0.0103	0.0102	0.8716	0.6437

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P4	2.319e-05	1.642e-09
X12_P4	3.437e-05	2.304e-09
X18_P4	5.353e-05	2.967e-09
X24_P4	5.671e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	1.188e-03	1.887e-03	2.939e-03	3.472e-03
B (output stable)	1.060e-03	1.694e-03	2.549e-03	3.073e-03
C (output stable)	6.318e-05	1.848e-04	2.733e-04	3.968e-04
D (output stable)	1.324e-04	5.595e-04	6.724e-04	1.071e-03
A to Z	4.754e-03	8.778e-03	1.317e-02	1.717e-02
B to Z	4.458e-03	8.294e-03	1.210e-02	1.609e-02
C to Z	1.946e-03	3.847e-03	5.662e-03	7.783e-03
D to Z	1.705e-03	3.125e-03	4.799e-03	6.431e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

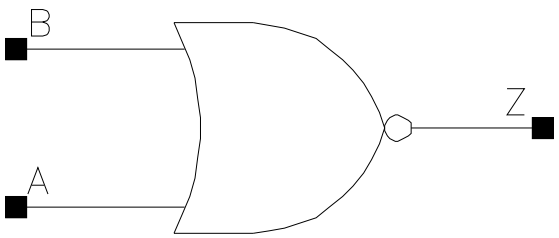
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	5.507e-07	4.557e-07	8.237e-07	3.352e-07
B (output stable)	3.224e-06	2.368e-05	3.518e-05	3.951e-05
C (output stable)	8.339e-08	-9.320e-08	-1.530e-07	-4.437e-07
D (output stable)	8.605e-08	-8.200e-07	-6.140e-07	-2.038e-06
A to Z	3.184e-06	1.723e-06	5.022e-06	1.194e-06
B to Z	5.893e-07	7.100e-08	4.880e-06	8.900e-08
C to Z	7.100e-08	1.837e-06	2.312e-06	3.123e-06
D to Z	1.950e-07	5.800e-08	1.100e-08	-1.140e-07

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.408	0.4896
X5_P4	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X10_P4	1.200	0.680	0.8160
X14_P4	1.200	0.680	0.8160
X17_P4	1.200	0.952	1.1424
X21_P4	1.200	0.952	1.1424
X24_P4	1.200	1.224	1.4688
X27_P4	1.200	1.224	1.4688
X34_P4	1.200	1.496	1.7952
X40_P4	1.200	1.360	1.6320
X41_P4	1.200	1.768	2.1216
X49_P4	1.200	1.496	1.7952
X53_P4	1.200	1.904	2.2848
X55_P4	1.200	2.312	2.7744
X57_P4	1.200	1.904	2.2848
X65_P4	1.200	2.040	2.4480
X84_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P4	X5_P4	X7_P4	X10_P4
A	0.0006	0.0007	0.0009	0.0015
B	0.0006	0.0007	0.0010	0.0014
	X14_P4	X17_P4	X21_P4	X24_P4

A	0.0019	0.0025	0.0029	0.0034
B	0.0018	0.0023	0.0027	0.0032
	X27_P4	X34_P4	X40_P4	X41_P4
A	0.0037	0.0047	0.0010	0.0057
B	0.0035	0.0044	0.0012	0.0054
	X49_P4	X53_P4	X55_P4	X57_P4
A	0.0010	0.0011	0.0076	0.0011
B	0.0012	0.0010	0.0072	0.0010
	X65_P4	X84_P4		
A	0.0011	0.0012		
B	0.0010	0.0011		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X5_P4**	**X3_P4**	**X5_P4**
A to Z ↓	0.0060	0.0055	3.1034	2.2835
A to Z ↑	0.0141	0.0131	9.0924	6.6996
B to Z ↓	0.0047	0.0040	3.1823	2.3046
B to Z ↑	0.0149	0.0137	9.1458	6.7301
	X7_P4	**X10_P4**	**X7_P4**	**X10_P4**
A to Z ↓	0.0053	0.0056	1.6951	1.0902
A to Z ↑	0.0124	0.0137	4.7851	3.1796
B to Z ↓	0.0038	0.0033	1.7201	1.1037
B to Z ↑	0.0128	0.0121	4.8074	3.1942
	X14_P4	**X17_P4**	**X14_P4**	**X17_P4**
A to Z ↓	0.0055	0.0056	0.8377	0.6668
A to Z ↑	0.0129	0.0130	2.3792	1.9100
B to Z ↓	0.0032	0.0037	0.8487	0.6741
B to Z ↑	0.0116	0.0123	2.3918	1.9209
	X21_P4	**X24_P4**	**X21_P4**	**X24_P4**
A to Z ↓	0.0056	0.0055	0.5712	0.4853
A to Z ↑	0.0126	0.0127	1.6019	1.3925
B to Z ↓	0.0038	0.0034	0.5776	0.4914
B to Z ↑	0.0121	0.0119	1.6104	1.4004
	X27_P4	**X34_P4**	**X27_P4**	**X34_P4**
A to Z ↓	0.0054	0.0058	0.4327	0.3488
A to Z ↑	0.0124	0.0126	1.2331	0.9815
B to Z ↓	0.0033	0.0037	0.4382	0.3529
B to Z ↑	0.0116	0.0120	1.2397	0.9865
	X40_P4	**X41_P4**	**X40_P4**	**X41_P4**
A to Z ↓	0.0255	0.0056	0.3414	0.2907
A to Z ↑	0.0367	0.0123	0.5069	0.8123
B to Z ↓	0.0243	0.0034	0.3414	0.2945
B to Z ↑	0.0383	0.0115	0.5077	0.8171
	X49_P4	**X53_P4**	**X49_P4**	**X53_P4**
A to Z ↓	0.0266	0.0280	0.2837	0.2595
A to Z ↑	0.0376	0.0430	0.4217	0.3891
B to Z ↓	0.0253	0.0267	0.2840	0.2597
B to Z ↑	0.0391	0.0443	0.4219	0.3895
	X55_P4	**X57_P4**	**X55_P4**	**X57_P4**
A to Z ↓	0.0057	0.0282	0.2196	0.2443
A to Z ↑	0.0123	0.0432	0.6127	0.3626

B to Z ↓	0.0035	0.0269	0.2230	0.2445
B to Z ↑	0.0116	0.0444	0.6163	0.3627
	X65_P4	**X84_P4**	**X65_P4**	**X84_P4**
A to Z ↓	0.0288	0.0303	0.2143	0.1705
A to Z ↑	0.0436	0.0445	0.3172	0.2526
B to Z ↓	0.0276	0.0291	0.2144	0.1706
B to Z ↑	0.0449	0.0459	0.3176	0.2525

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P4	8.331e-06	9.792e-10
X5_P4	1.119e-05	9.792e-10
X7_P4	1.480e-05	9.792e-10
X10_P4	2.181e-05	1.310e-09
X14_P4	2.744e-05	1.310e-09
X17_P4	3.490e-05	1.642e-09
X21_P4	3.923e-05	1.642e-09
X24_P4	4.776e-05	1.973e-09
X27_P4	5.105e-05	1.973e-09
X34_P4	6.289e-05	2.304e-09
X40_P4	9.053e-05	2.139e-09
X41_P4	7.473e-05	2.635e-09
X49_P4	9.991e-05	2.304e-09
X53_P4	1.240e-04	2.801e-09
X55_P4	9.840e-05	3.298e-09
X57_P4	1.287e-04	2.801e-09
X65_P4	1.381e-04	2.967e-09
X84_P4	1.534e-04	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	3.203e-05	4.235e-05	5.801e-05	1.626e-04
B (output stable)	3.931e-05	5.446e-05	7.767e-05	2.340e-04
A to Z	1.032e-03	1.295e-03	1.733e-03	2.878e-03
B to Z	8.539e-04	1.060e-03	1.403e-03	2.046e-03
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	1.924e-04	2.341e-04	2.633e-04	3.218e-04
B (output stable)	2.924e-04	3.356e-04	3.568e-04	4.566e-04
A to Z	3.626e-03	4.590e-03	5.290e-03	6.248e-03
B to Z	2.621e-03	3.458e-03	4.012e-03	4.626e-03
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	3.481e-04	4.244e-04	5.899e-05	5.420e-04
B (output stable)	4.946e-04	5.596e-04	7.770e-05	7.524e-04
A to Z	6.849e-03	8.718e-03	1.524e-02	1.034e-02
B to Z	5.050e-03	6.595e-03	1.493e-02	7.569e-03
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	5.915e-05	6.014e-05	6.980e-04	5.974e-05
B (output stable)	7.770e-05	8.294e-05	9.331e-04	8.255e-05
A to Z	1.722e-02	2.141e-02	1.359e-02	2.208e-02
B to Z	1.690e-02	2.108e-02	1.009e-02	2.174e-02
	X65_P4	X84_P4		

A (output stable)	5.995e-05	6.301e-05		
B (output stable)	8.292e-05	8.367e-05		
A to Z	2.392e-02	2.890e-02		
B to Z	2.358e-02	2.850e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

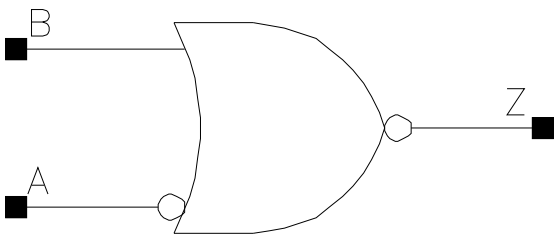
Pin Cycle (vdds)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	2.104e-07	2.303e-07	2.384e-07	2.077e-07
B (output stable)	4.846e-06	4.611e-06	4.573e-06	6.152e-05
A to Z	4.819e-07	1.557e-06	1.863e-06	2.499e-06
B to Z	7.974e-07	7.839e-07	2.407e-07	7.719e-07
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	4.370e-07	5.571e-07	4.920e-07	8.727e-07
B (output stable)	6.562e-05	4.673e-05	4.271e-05	8.304e-05
A to Z	2.162e-06	2.361e-06	3.033e-06	3.169e-06
B to Z	9.225e-07	1.831e-06	2.373e-06	1.659e-06
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	1.047e-06	7.686e-07	2.420e-07	1.089e-06
B (output stable)	8.852e-05	6.758e-05	4.419e-06	1.238e-04
A to Z	3.880e-06	4.526e-06	6.880e-07	4.216e-06
B to Z	2.188e-06	3.218e-06	6.470e-07	2.144e-06
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	2.429e-07	2.891e-07	1.337e-06	2.894e-07
B (output stable)	4.406e-06	5.060e-06	1.279e-04	5.060e-06
A to Z	5.470e-07	1.480e-07	5.274e-06	1.290e-07
B to Z	6.010e-07	7.400e-08	2.980e-06	1.450e-07
	X65_P4	X84_P4		
A (output stable)	2.899e-07	2.990e-07		
B (output stable)	5.052e-06	5.572e-06		
A to Z	5.200e-08	-3.400e-08		
B to Z	5.500e-08	2.400e-08		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X7_P4	1.200	0.680	0.8160
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X41_P4	1.200	2.312	2.7744
X55_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X7_P4	X13_P4
A	0.0008	0.0008	0.0008	0.0012
B	0.0006	0.0010	0.0009	0.0017
	X27_P4	X41_P4	X55_P4	
A	0.0022	0.0032	0.0042	
B	0.0035	0.0054	0.0072	

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0207	0.0229	2.9112	1.9544
A to Z ↑	0.0182	0.0186	8.9851	4.7460
B to Z ↓	0.0050	0.0050	3.1553	2.1080
B to Z ↑	0.0150	0.0125	9.1260	4.8245

	X7_P4	X13_P4	X7_P4	X13_P4
A to Z ↓	0.0231	0.0212	1.5735	0.8514
A to Z ↑	0.0203	0.0195	4.7131	2.5079
B to Z ↓	0.0040	0.0035	1.6506	0.8918
B to Z ↑	0.0136	0.0126	4.7708	2.5424
	X27_P4	**X41_P4**	**X27_P4**	**X41_P4**
A to Z ↓	0.0207	0.0211	0.4078	0.2759
A to Z ↑	0.0187	0.0191	1.2018	0.8070
B to Z ↓	0.0034	0.0035	0.4404	0.2965
B to Z ↑	0.0119	0.0119	1.2184	0.8184
	X55_P4		**X55_P4**	
A to Z ↓	0.0207		0.2088	
A to Z ↑	0.0186		0.6091	
B to Z ↓	0.0035		0.2246	
B to Z ↑	0.0118		0.6180	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P4	1.547e-05	1.145e-09
X6_P4	2.061e-05	1.145e-09
X7_P4	2.438e-05	1.310e-09
X13_P4	4.254e-05	1.642e-09
X27_P4	7.858e-05	2.470e-09
X41_P4	1.136e-04	3.298e-09
X55_P4	1.486e-04	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	1.520e-03	1.845e-03	1.954e-03	3.230e-03
B (output stable)	4.635e-05	8.362e-05	1.768e-04	3.473e-04
A to Z	2.484e-03	3.375e-03	3.865e-03	6.588e-03
B to Z	8.625e-04	1.338e-03	1.560e-03	2.727e-03
	X27_P4	X41_P4	X55_P4	
A (output stable)	6.439e-03	9.746e-03	1.265e-02	
B (output stable)	6.858e-04	9.926e-04	1.211e-03	
A to Z	1.320e-02	1.970e-02	2.562e-02	
B to Z	5.344e-03	7.870e-03	1.038e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

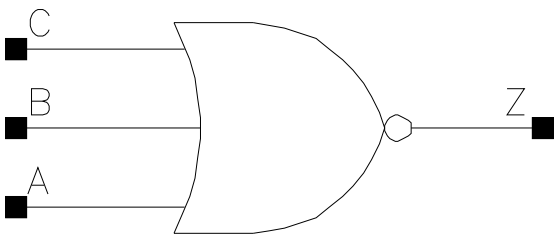
Pin Cycle (vdds)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	6.350e-07	7.762e-07	1.259e-06	2.251e-06
B (output stable)	4.780e-06	4.392e-06	3.193e-05	5.321e-05
A to Z	6.391e-07	5.250e-07	1.018e-06	1.426e-06
B to Z	2.674e-07	1.052e-06	9.801e-07	5.178e-07
	X27_P4	X41_P4	X55_P4	
A (output stable)	2.805e-06	4.026e-06	4.785e-06	
B (output stable)	9.014e-05	1.209e-04	1.283e-04	
A to Z	2.756e-06	3.222e-06	3.503e-06	
B to Z	4.960e-07	2.988e-06	4.290e-06	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X9_P4	1.200	0.952	1.1424
X13_P4	1.200	0.952	1.1424
X16_P4	1.200	1.360	1.6320
X19_P4	1.200	1.496	1.7952
X22_P4	1.200	1.768	2.1216
X25_P4	1.200	1.904	2.2848
X37_P4	1.200	2.584	3.1008
X49_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P4	X6_P4	X9_P4	X13_P4
A	0.0008	0.0009	0.0015	0.0018
B	0.0007	0.0009	0.0016	0.0019
C	0.0008	0.0009	0.0014	0.0017
	X16_P4	X19_P4	X22_P4	X25_P4
A	0.0024	0.0028	0.0033	0.0037
B	0.0025	0.0032	0.0035	0.0043
C	0.0023	0.0026	0.0031	0.0034
	X37_P4	X49_P4		
A	0.0057	0.0075		
B	0.0057	0.0075		

C	0.0050	0.0071		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0073	0.0069	2.3149	1.7200
A to Z ↑	0.0193	0.0179	9.9789	7.1231
B to Z ↓	0.0066	0.0061	2.3236	1.7248
B to Z ↑	0.0189	0.0173	9.9934	7.1347
C to Z ↓	0.0053	0.0047	2.3445	1.7451
C to Z ↑	0.0185	0.0166	10.0085	7.1459
	X9_P4	**X13_P4**	**X9_P4**	**X13_P4**
A to Z ↓	0.0071	0.0070	1.1219	0.8697
A to Z ↑	0.0193	0.0182	4.7080	3.5455
B to Z ↓	0.0063	0.0059	1.0970	0.8372
B to Z ↑	0.0193	0.0177	4.7185	3.5522
C to Z ↓	0.0041	0.0038	1.1089	0.8535
C to Z ↑	0.0157	0.0146	4.7192	3.5544
	X16_P4	**X19_P4**	**X16_P4**	**X19_P4**
A to Z ↓	0.0070	0.0069	0.6715	0.5724
A to Z ↑	0.0187	0.0185	2.8513	2.3743
B to Z ↓	0.0065	0.0064	0.6738	0.5619
B to Z ↑	0.0184	0.0186	2.8566	2.3788
C to Z ↓	0.0044	0.0043	0.6791	0.5840
C to Z ↑	0.0162	0.0154	2.8590	2.3810
	X22_P4	**X25_P4**	**X22_P4**	**X25_P4**
A to Z ↓	0.0070	0.0069	0.4949	0.4357
A to Z ↑	0.0184	0.0183	2.0393	1.7859
B to Z ↓	0.0063	0.0061	0.4876	0.4212
B to Z ↑	0.0182	0.0184	2.0434	1.7892
C to Z ↓	0.0041	0.0040	0.4938	0.4374
C to Z ↑	0.0152	0.0147	2.0455	1.7907
	X37_P4	**X49_P4**	**X37_P4**	**X49_P4**
A to Z ↓	0.0070	0.0071	0.2984	0.2264
A to Z ↑	0.0178	0.0179	1.1976	0.9022
B to Z ↓	0.0062	0.0063	0.2956	0.2246
B to Z ↑	0.0172	0.0173	1.2001	0.9041
C to Z ↓	0.0043	0.0044	0.3000	0.2275
C to Z ↑	0.0148	0.0150	1.2009	0.9051

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	8.591e-06	1.145e-09
X6_P4	1.148e-05	1.145e-09
X9_P4	1.711e-05	1.642e-09
X13_P4	2.181e-05	1.642e-09
X16_P4	2.754e-05	2.139e-09
X19_P4	3.315e-05	2.304e-09
X22_P4	3.804e-05	2.635e-09
X25_P4	4.320e-05	2.801e-09
X37_P4	6.194e-05	3.629e-09

X49_P4	8.200e-05	4.623e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	4.785e-05	6.534e-05	1.190e-04	1.539e-04
B (output stable)	2.169e-05	3.232e-05	8.308e-05	1.004e-04
C (output stable)	5.685e-05	8.456e-05	1.967e-04	2.509e-04
A to Z	1.741e-03	2.249e-03	3.690e-03	4.587e-03
B to Z	1.456e-03	1.858e-03	3.138e-03	3.826e-03
C to Z	1.218e-03	1.518e-03	2.230e-03	2.743e-03
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	1.842e-04	2.224e-04	2.654e-04	3.069e-04
B (output stable)	1.173e-04	1.509e-04	1.788e-04	2.060e-04
C (output stable)	2.827e-04	3.619e-04	4.177e-04	4.945e-04
A to Z	5.913e-03	7.016e-03	8.123e-03	9.212e-03
B to Z	4.943e-03	5.953e-03	6.820e-03	7.813e-03
C to Z	3.796e-03	4.327e-03	5.006e-03	5.481e-03
	X37_P4	X49_P4		
A (output stable)	4.496e-04	5.965e-04		
B (output stable)	2.801e-04	3.664e-04		
C (output stable)	6.985e-04	9.173e-04		
A to Z	1.340e-02	1.787e-02		
B to Z	1.107e-02	1.475e-02		
C to Z	8.098e-03	1.085e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

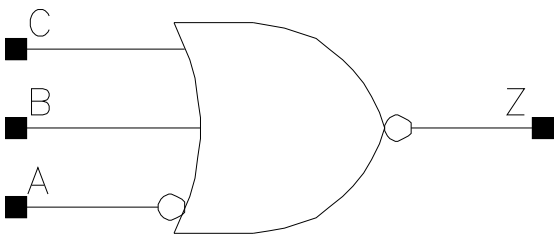
Pin Cycle (vdds)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	-5.668e-08	-5.519e-09	-1.332e-06	-1.218e-06
B (output stable)	1.168e-05	1.490e-05	3.222e-05	3.938e-05
C (output stable)	2.181e-05	2.832e-05	1.105e-04	1.284e-04
A to Z	6.250e-07	2.694e-06	4.117e-06	5.699e-06
B to Z	3.010e-07	1.898e-06	2.719e-06	2.980e-06
C to Z	8.770e-07	8.526e-07	1.430e-08	2.265e-07
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	-7.939e-07	-1.287e-06	-1.743e-06	-2.321e-06
B (output stable)	4.206e-05	5.749e-05	6.587e-05	8.374e-05
C (output stable)	1.051e-04	1.480e-04	1.860e-04	2.351e-04
A to Z	7.067e-06	8.917e-06	9.723e-06	1.027e-05
B to Z	4.454e-06	4.612e-06	5.194e-06	4.769e-06
C to Z	8.780e-07	3.290e-07	6.890e-07	8.820e-07
	X37_P4	X49_P4		
A (output stable)	-2.353e-06	-2.926e-06		
B (output stable)	1.070e-04	1.391e-04		
C (output stable)	2.854e-04	3.640e-04		
A to Z	1.614e-05	2.020e-05		
B to Z	6.918e-06	8.363e-06		
C to Z	-3.700e-08	-1.300e-08		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.680	0.8160
X13_P4	1.200	1.224	1.4688
X19_P4	1.200	1.496	1.7952
X25_P4	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0009	0.0011	0.0012	0.0022
B	0.0009	0.0019	0.0028	0.0038
C	0.0010	0.0017	0.0026	0.0035

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X13_P4**	**X6_P4**	**X13_P4**
A to Z ↓	0.0231	0.0225	1.6326	0.9010
A to Z ↑	0.0249	0.0246	7.1882	3.5372
B to Z ↓	0.0063	0.0060	1.7311	0.8413
B to Z ↑	0.0175	0.0178	7.2239	3.5530
C to Z ↓	0.0048	0.0038	1.7450	0.8541
C to Z ↑	0.0169	0.0147	7.2350	3.5547
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0255	0.0225	0.5520	0.4186

A to Z ↑	0.0271	0.0247	2.3822	1.7873
B to Z ↓	0.0065	0.0061	0.5829	0.4354
B to Z ↑	0.0175	0.0173	2.3947	1.7962
C to Z ↓	0.0043	0.0039	0.5848	0.4398
C to Z ↑	0.0155	0.0147	2.3974	1.7983

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P4	1.886e-05	1.310e-09
X13_P4	3.759e-05	1.973e-09
X19_P4	4.508e-05	2.304e-09
X25_P4	7.042e-05	3.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	1.896e-03	3.451e-03	4.375e-03	6.775e-03
B (output stable)	4.450e-05	1.348e-04	1.758e-04	2.485e-04
C (output stable)	9.740e-05	3.198e-04	3.859e-04	5.645e-04
A to Z	4.103e-03	8.118e-03	1.110e-02	1.574e-02
B to Z	1.866e-03	3.850e-03	5.612e-03	7.421e-03
C to Z	1.534e-03	2.754e-03	4.301e-03	5.459e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

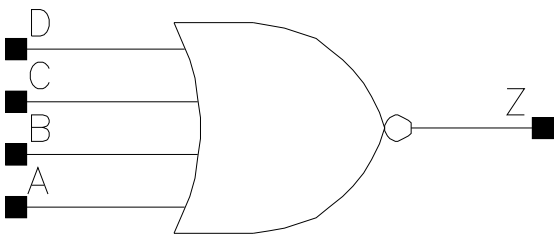
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	4.966e-07	5.888e-07	1.568e-06	7.972e-07
B (output stable)	1.478e-05	3.702e-05	4.894e-05	7.040e-05
C (output stable)	2.802e-05	1.219e-04	1.181e-04	1.948e-04
A to Z	1.245e-06	6.457e-06	8.016e-06	6.183e-06
B to Z	1.980e-06	2.640e-06	4.974e-06	4.446e-06
C to Z	7.162e-07	1.482e-07	1.287e-06	-3.910e-07

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	1.904	2.2848
X32_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X32_P4
A	0.0007	0.0007	0.0008	0.0010
B	0.0008	0.0008	0.0009	0.0012
C	0.0006	0.0006	0.0009	0.0010
D	0.0007	0.0007	0.0009	0.0010

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0256	0.0259	1.6012	0.7875
A to Z ↑	0.0390	0.0420	2.5084	1.2418
B to Z ↓	0.0243	0.0248	1.6024	0.7874
B to Z ↑	0.0401	0.0435	2.5073	1.2399
C to Z ↓	0.0251	0.0259	1.5988	0.7862
C to Z ↑	0.0400	0.0438	2.5052	1.2415

D to Z ↓	0.0244	0.0252	1.5996	0.7864
D to Z ↑	0.0415	0.0456	2.5066	1.2397
	X25_P4	**X32_P4**	**X25_P4**	**X32_P4**
A to Z ↓	0.0266	0.0287	0.5473	0.4294
A to Z ↑	0.0417	0.0406	0.8496	0.6417
B to Z ↓	0.0256	0.0275	0.5470	0.4292
B to Z ↑	0.0432	0.0417	0.8492	0.6419
C to Z ↓	0.0259	0.0283	0.5449	0.4275
C to Z ↑	0.0418	0.0414	0.8489	0.6425
D to Z ↓	0.0247	0.0266	0.5443	0.4274
D to Z ↑	0.0432	0.0425	0.8487	0.6423

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	2.917e-05	1.973e-09
X17_P4	4.159e-05	2.139e-09
X25_P4	6.233e-05	2.801e-09
X32_P4	7.581e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	7.353e-04	8.860e-04	1.241e-03	1.571e-03
B (output stable)	6.590e-04	8.077e-04	1.140e-03	1.428e-03
C (output stable)	6.913e-04	8.052e-04	1.204e-03	1.526e-03
D (output stable)	6.148e-04	7.321e-04	1.100e-03	1.386e-03
A to Z	5.024e-03	7.825e-03	1.184e-02	1.493e-02
B to Z	4.837e-03	7.648e-03	1.157e-02	1.462e-02
C to Z	5.075e-03	7.813e-03	1.125e-02	1.429e-02
D to Z	4.876e-03	7.637e-03	1.100e-02	1.395e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

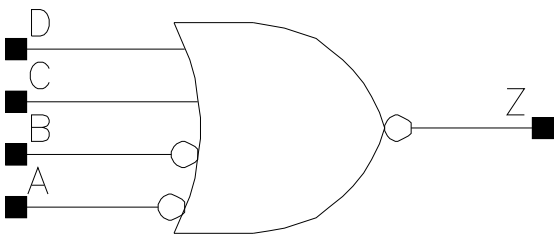
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	2.600e-07	2.109e-07	2.516e-07	2.505e-07
B (output stable)	2.733e-06	2.499e-06	2.947e-06	3.035e-06
C (output stable)	4.126e-07	2.812e-07	3.408e-07	3.043e-07
D (output stable)	3.106e-06	2.997e-06	2.928e-06	2.798e-06
A to Z	8.790e-07	1.980e-07	9.000e-08	5.617e-07
B to Z	9.459e-07	5.327e-07	9.087e-07	4.807e-07
C to Z	9.070e-07	2.550e-07	1.220e-07	3.310e-07
D to Z	9.536e-07	4.754e-07	7.980e-07	4.676e-07

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X13_P4	1.200	1.496	1.7952
X19_P4	1.200	2.040	2.4480
X25_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0011	0.0011	0.0021	0.0021
B	0.0011	0.0016	0.0022	0.0022
C	0.0009	0.0018	0.0027	0.0036
D	0.0009	0.0017	0.0026	0.0034

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X13_P4	X6_P4	X13_P4
A to Z ↓	0.0204	0.0252	1.5879	0.7985
A to Z ↑	0.0245	0.0304	6.9340	3.5971
B to Z ↓	0.0189	0.0242	1.5870	0.7979
B to Z ↑	0.0253	0.0319	6.9339	3.5980
C to Z ↓	0.0067	0.0061	1.7517	0.8421
C to Z ↑	0.0176	0.0181	6.9750	3.6158

D to Z ↓	0.0050	0.0040	1.7571	0.8517
D to Z ↑	0.0168	0.0152	6.9817	3.6171
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0224	0.0244	0.5458	0.4116
A to Z ↑	0.0274	0.0297	2.3843	1.8032
B to Z ↓	0.0204	0.0227	0.5450	0.4109
B to Z ↑	0.0280	0.0307	2.3844	1.8035
C to Z ↓	0.0065	0.0063	0.5833	0.4371
C to Z ↑	0.0174	0.0174	2.3965	1.8115
D to Z ↓	0.0043	0.0040	0.5852	0.4395
D to Z ↑	0.0155	0.0147	2.3982	1.8124

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P4	2.158e-05	1.642e-09
X13_P4	3.038e-05	2.304e-09
X19_P4	4.865e-05	2.967e-09
X25_P4	5.517e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	1.179e-03	1.858e-03	2.888e-03	3.443e-03
B (output stable)	1.085e-03	1.748e-03	2.648e-03	3.232e-03
C (output stable)	4.318e-05	1.364e-04	1.928e-04	2.688e-04
D (output stable)	1.097e-04	3.293e-04	4.248e-04	6.415e-04
A to Z	4.964e-03	9.049e-03	1.360e-02	1.733e-02
B to Z	4.730e-03	8.673e-03	1.282e-02	1.658e-02
C to Z	1.930e-03	3.868e-03	5.571e-03	7.347e-03
D to Z	1.590e-03	2.838e-03	4.302e-03	5.428e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

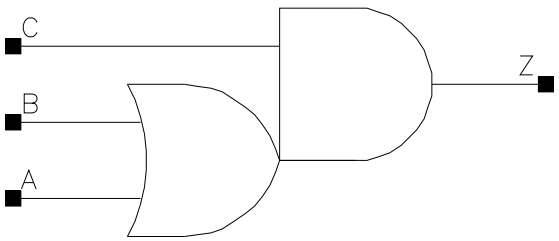
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	3.350e-07	-7.022e-08	8.380e-07	6.067e-07
B (output stable)	2.698e-07	-7.691e-08	2.389e-08	3.760e-07
C (output stable)	1.970e-05	5.456e-05	7.334e-05	1.022e-04
D (output stable)	3.707e-05	1.374e-04	1.455e-04	2.339e-04
A to Z	2.518e-06	4.694e-06	8.722e-06	9.752e-06
B to Z	1.865e-06	4.399e-06	2.758e-06	7.933e-06
C to Z	4.680e-07	3.384e-06	4.991e-06	5.442e-06
D to Z	9.872e-07	2.511e-07	9.260e-07	1.900e-08

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0010	0.0010	0.0020
B	0.0011	0.0012	0.0022
C	0.0011	0.0011	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0220	0.0258	1.6507	0.8229
A to Z ↑	0.0182	0.0208	2.5249	1.2443
B to Z ↓	0.0228	0.0271	1.6510	0.8227
B to Z ↑	0.0162	0.0189	2.5202	1.2424
C to Z ↓	0.0203	0.0226	1.6309	0.8096
C to Z ↑	0.0167	0.0189	2.5239	1.2440
	X33_P4		**X33_P4**	
A to Z ↓	0.0267		0.4172	
A to Z ↑	0.0223		0.6239	

B to Z ↓	0.0278		0.4171	
B to Z ↑	0.0200		0.6225	
C to Z ↓	0.0231		0.4102	
C to Z ↑	0.0196		0.6234	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	2.817e-05	1.310e-09
X17_P4	3.965e-05	1.476e-09
X33_P4	7.857e-05	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	8.835e-05	9.009e-05	1.870e-04
B (output stable)	9.866e-05	1.009e-04	1.989e-04
C (output stable)	8.930e-05	9.281e-05	1.776e-04
A to Z	3.943e-03	6.118e-03	1.266e-02
B to Z	3.586e-03	5.758e-03	1.195e-02
C to Z	4.252e-03	6.227e-03	1.281e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

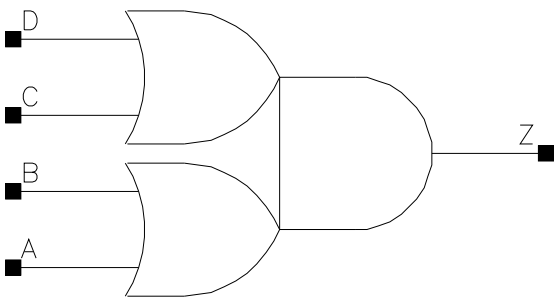
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	9.401e-08	8.035e-08	7.214e-08
B (output stable)	1.573e-06	1.585e-06	3.780e-06
C (output stable)	6.616e-08	8.581e-08	4.875e-08
A to Z	4.599e-07	2.476e-07	4.410e-07
B to Z	1.188e-06	1.666e-07	9.140e-08
C to Z	1.236e-06	4.143e-08	-4.207e-08

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0010	0.0021
B	0.0008	0.0011	0.0021
C	0.0007	0.0011	0.0021
D	0.0007	0.0011	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0363	0.0317	1.6167	0.8198
A to Z ↑	0.0245	0.0219	2.4759	1.2393
B to Z ↓	0.0381	0.0332	1.6171	0.8197
B to Z ↑	0.0233	0.0206	2.4740	1.2386

C to Z ↓	0.0316	0.0281	1.6018	0.8150
C to Z ↑	0.0242	0.0225	2.4739	1.2388
D to Z ↓	0.0328	0.0291	1.6006	0.8147
D to Z ↑	0.0225	0.0205	2.4709	1.2360
	X33_P4		**X33_P4**	
A to Z ↓	0.0324		0.4212	
A to Z ↑	0.0221		0.6227	
B to Z ↓	0.0325		0.4215	
B to Z ↑	0.0202		0.6221	
C to Z ↓	0.0281		0.4181	
C to Z ↑	0.0222		0.6222	
D to Z ↓	0.0280		0.4183	
D to Z ↑	0.0200		0.6215	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	2.739e-05	1.642e-09
X17_P4	5.114e-05	1.807e-09
X33_P4	9.549e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	3.486e-05	5.665e-05	1.599e-04
B (output stable)	3.754e-05	6.683e-05	2.311e-04
C (output stable)	8.068e-05	1.083e-04	2.568e-04
D (output stable)	8.415e-05	1.197e-04	3.386e-04
A to Z	4.611e-03	7.696e-03	1.519e-02
B to Z	4.412e-03	7.309e-03	1.409e-02
C to Z	4.046e-03	6.921e-03	1.352e-02
D to Z	3.846e-03	6.548e-03	1.246e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

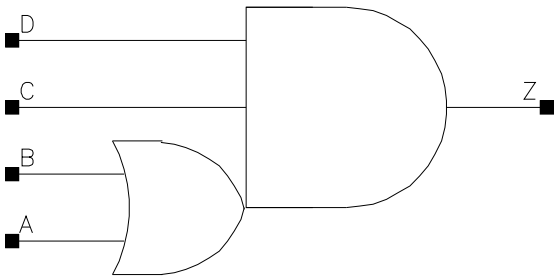
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	1.799e-07	1.967e-07	4.909e-07
B (output stable)	2.972e-06	2.871e-06	4.130e-05
C (output stable)	1.045e-07	1.721e-07	2.534e-07
D (output stable)	3.128e-06	3.153e-06	3.765e-05
A to Z	-1.421e-08	1.149e-07	9.463e-07
B to Z	-1.467e-08	-3.563e-08	2.795e-07
C to Z	2.685e-07	3.440e-07	1.579e-06
D to Z	1.806e-08	1.806e-07	7.581e-07

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	1.088	1.3056
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0007	0.0011	0.0018	0.0021
B	0.0007	0.0011	0.0018	0.0022
C	0.0008	0.0011	0.0018	0.0021
D	0.0007	0.0011	0.0018	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0308	0.0295	1.6886	0.8234
A to Z ↑	0.0289	0.0276	2.5530	1.2402
B to Z ↓	0.0322	0.0299	1.6882	0.8228
B to Z ↑	0.0272	0.0249	2.5548	1.2378
C to Z ↓	0.0265	0.0249	1.6505	0.8076

C to Z ↑	0.0261	0.0245	2.5532	1.2384
D to Z ↓	0.0256	0.0240	1.6498	0.8071
D to Z ↑	0.0278	0.0260	2.5528	1.2391
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0307	0.0301	0.5606	0.4202
A to Z ↑	0.0282	0.0294	0.8416	0.6308
B to Z ↓	0.0309	0.0303	0.5610	0.4197
B to Z ↑	0.0257	0.0267	0.8408	0.6302
C to Z ↓	0.0261	0.0255	0.5505	0.4119
C to Z ↑	0.0252	0.0257	0.8409	0.6303
D to Z ↓	0.0247	0.0243	0.5491	0.4112
D to Z ↑	0.0259	0.0267	0.8407	0.6304

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	1.703e-05	1.476e-09
X17_P4	3.336e-05	1.807e-09
X25_P4	5.297e-05	2.801e-09
X33_P4	6.587e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	8.399e-05	1.609e-04	2.737e-04	3.031e-04
B (output stable)	8.691e-05	1.665e-04	2.914e-04	3.208e-04
C (output stable)	2.689e-05	5.373e-05	1.275e-04	1.407e-04
D (output stable)	3.759e-05	7.519e-05	2.151e-04	2.330e-04
A to Z	3.915e-03	7.142e-03	1.142e-02	1.465e-02
B to Z	3.729e-03	6.633e-03	1.058e-02	1.359e-02
C to Z	4.115e-03	7.376e-03	1.206e-02	1.509e-02
D to Z	3.958e-03	7.082e-03	1.131e-02	1.433e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

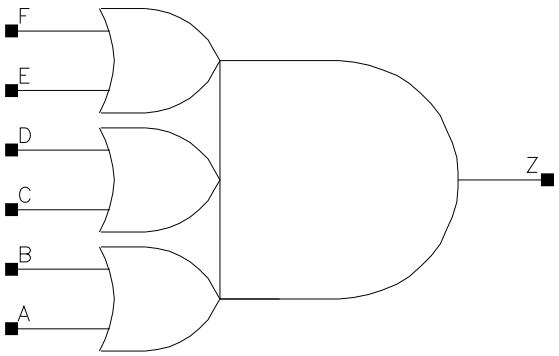
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	-2.141e-07	-2.286e-07	-3.281e-07	1.396e-07
B (output stable)	5.023e-07	5.110e-06	7.879e-06	9.091e-06
C (output stable)	8.158e-08	6.961e-08	5.508e-08	4.980e-08
D (output stable)	7.252e-08	3.419e-08	-2.314e-08	4.821e-08
A to Z	2.028e-07	3.540e-07	4.990e-07	3.830e-07
B to Z	-1.613e-07	-4.710e-08	3.230e-07	-4.620e-07
C to Z	1.234e-07	7.152e-07	1.222e-06	9.883e-07
D to Z	1.277e-08	4.141e-07	1.375e-06	9.260e-07

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0008	0.0010	0.0018
B	0.0007	0.0011	0.0021
C	0.0007	0.0011	0.0019
D	0.0007	0.0011	0.0021
E	0.0007	0.0011	0.0019
F	0.0007	0.0011	0.0022

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0415	0.0361	1.7309	0.8392
A to Z ↑	0.0309	0.0286	2.5377	1.2527
B to Z ↓	0.0432	0.0379	1.7311	0.8392
B to Z ↑	0.0296	0.0274	2.5379	1.2526
C to Z ↓	0.0380	0.0343	1.7182	0.8367
C to Z ↑	0.0317	0.0291	2.5384	1.2523
D to Z ↓	0.0397	0.0357	1.7183	0.8371
D to Z ↑	0.0301	0.0274	2.5371	1.2522
E to Z ↓	0.0329	0.0301	1.7021	0.8308
E to Z ↑	0.0300	0.0281	2.5357	1.2514
F to Z ↓	0.0346	0.0312	1.7026	0.8307
F to Z ↑	0.0283	0.0262	2.5332	1.2506
	X33_P4		X33_P4	
A to Z ↓	0.0366		0.4288	
A to Z ↑	0.0296		0.6314	
B to Z ↓	0.0384		0.4288	
B to Z ↑	0.0273		0.6300	
C to Z ↓	0.0337		0.4259	
C to Z ↑	0.0298		0.6313	
D to Z ↓	0.0352		0.4260	
D to Z ↑	0.0277		0.6296	
E to Z ↓	0.0295		0.4230	
E to Z ↑	0.0288		0.6303	
F to Z ↓	0.0309		0.4230	
F to Z ↑	0.0266		0.6290	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	2.610e-05	1.973e-09
X17_P4	4.867e-05	2.139e-09
X33_P4	9.242e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	3.195e-05	5.469e-05	1.027e-04
B (output stable)	3.372e-05	6.614e-05	1.190e-04
C (output stable)	4.779e-05	7.809e-05	1.558e-04
D (output stable)	5.117e-05	8.666e-05	1.720e-04
E (output stable)	1.351e-04	1.986e-04	3.777e-04
F (output stable)	1.333e-04	2.022e-04	3.921e-04
A to Z	5.323e-03	9.042e-03	1.786e-02
B to Z	5.107e-03	8.672e-03	1.707e-02
C to Z	4.864e-03	8.406e-03	1.642e-02
D to Z	4.657e-03	8.029e-03	1.564e-02
E to Z	4.277e-03	7.544e-03	1.472e-02
F to Z	4.095e-03	7.175e-03	1.401e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

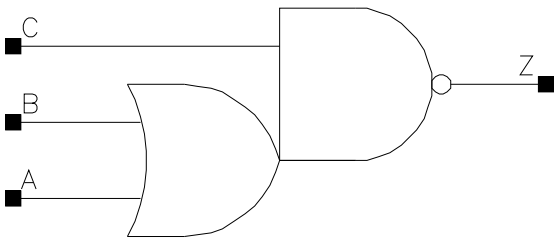
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	1.468e-07	1.704e-07	2.391e-07
B (output stable)	2.027e-06	2.182e-06	4.025e-06
C (output stable)	1.268e-07	1.666e-07	1.323e-07
D (output stable)	1.994e-06	2.156e-06	4.036e-06
E (output stable)	-1.202e-07	1.274e-07	-2.828e-07
F (output stable)	1.950e-06	2.063e-06	3.572e-06
A to Z	2.907e-07	4.181e-07	1.403e-07
B to Z	2.250e-07	2.433e-08	2.764e-07
C to Z	-2.320e-08	-2.878e-08	-1.232e-07
D to Z	-5.168e-08	-1.883e-07	-4.294e-07
E to Z	3.027e-07	4.349e-07	6.148e-07
F to Z	6.093e-08	4.407e-08	1.721e-07

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X34_P4	1.200	2.720	3.2640
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X34_P4	X46_P4
A	0.0009	0.0027	0.0055	0.0072
B	0.0009	0.0025	0.0050	0.0069
C	0.0010	0.0029	0.0059	0.0077

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0092	0.0096	2.9213	0.9558
A to Z ↑	0.0131	0.0139	4.7815	1.6307
B to Z ↓	0.0070	0.0073	2.8598	0.9605
B to Z ↑	0.0134	0.0134	4.8095	1.6412
C to Z ↓	0.0080	0.0081	2.6399	0.8720
C to Z ↑	0.0131	0.0131	2.5667	0.8541
	X34_P4	**X46_P4**	**X34_P4**	**X46_P4**
A to Z ↓	0.0101	0.0101	0.4872	0.3722

A to Z ↑	0.0144	0.0142	0.8144	0.6264
B to Z ↓	0.0076	0.0077	0.4945	0.3794
B to Z ↑	0.0136	0.0137	0.8191	0.6304
C to Z ↓	0.0085	0.0085	0.4471	0.3421
C to Z ↑	0.0133	0.0132	0.4273	0.3269

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P4	1.714e-05	1.145e-09
X17_P4	4.720e-05	2.139e-09
X34_P4	9.351e-05	3.795e-09
X46_P4	1.225e-04	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	7.755e-05	2.804e-04	5.902e-04	7.245e-04
B (output stable)	8.812e-05	3.097e-04	6.714e-04	8.137e-04
C (output stable)	8.162e-05	2.718e-04	5.618e-04	7.163e-04
A to Z	1.820e-03	5.771e-03	1.191e-02	1.544e-02
B to Z	1.480e-03	4.442e-03	9.097e-03	1.189e-02
C to Z	2.175e-03	6.679e-03	1.372e-02	1.787e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

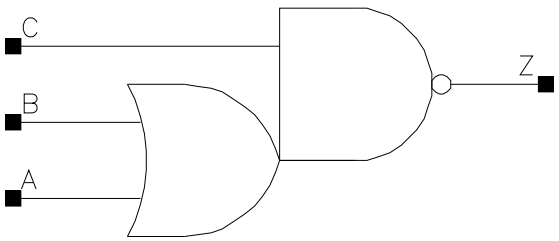
Pin Cycle (vdds)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	1.261e-07	1.006e-07	1.212e-07	2.239e-07
B (output stable)	1.640e-06	1.537e-05	4.199e-05	4.271e-05
C (output stable)	7.231e-08	-3.920e-08	-1.240e-07	-2.088e-07
A to Z	5.750e-07	1.297e-06	2.887e-06	3.020e-06
B to Z	9.198e-07	2.619e-06	3.888e-06	4.901e-06
C to Z	1.164e-06	9.140e-07	2.069e-06	6.893e-07

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.544	0.6528
X11_P4	1.200	0.952	1.1424
X17_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X17_P4	X23_P4
A	0.0009	0.0018	0.0028	0.0038
B	0.0009	0.0019	0.0027	0.0035
C	0.0009	0.0019	0.0027	0.0038
	X46_P4			
A	0.0076			
B	0.0071			
C	0.0077			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0089	0.0091	2.9443	1.3736
A to Z ↑	0.0164	0.0166	5.0294	2.3845
B to Z ↓	0.0071	0.0072	2.8929	1.3372

B to Z ↑	0.0170	0.0171	5.0537	2.3965
C to Z ↓	0.0072	0.0072	2.7716	1.2876
C to Z ↑	0.0100	0.0100	2.7477	1.2941
	X17_P4	**X23_P4**	**X17_P4**	**X23_P4**
A to Z ↓	0.0087	0.0093	0.9534	0.7067
A to Z ↑	0.0157	0.0172	1.5803	1.2078
B to Z ↓	0.0068	0.0071	0.9509	0.7077
B to Z ↑	0.0161	0.0168	1.5881	1.2136
C to Z ↓	0.0070	0.0072	0.9034	0.6693
C to Z ↑	0.0093	0.0096	0.8608	0.6554
	X46_P4		**X46_P4**	
A to Z ↓	0.0092		0.3690	
A to Z ↑	0.0169		0.6114	
B to Z ↓	0.0070		0.3656	
B to Z ↑	0.0165		0.6145	
C to Z ↓	0.0074		0.3479	
C to Z ↑	0.0094		0.3315	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P4	1.730e-05	1.145e-09
X11_P4	3.391e-05	1.642e-09
X17_P4	4.917e-05	2.139e-09
X23_P4	6.679e-05	2.801e-09
X46_P4	1.266e-04	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	3.693e-05	8.059e-05	1.168e-04	2.079e-04
B (output stable)	4.032e-05	9.316e-05	1.338e-04	2.529e-04
C (output stable)	2.126e-04	5.081e-04	6.280e-04	9.629e-04
A to Z	2.150e-03	4.619e-03	6.488e-03	9.541e-03
B to Z	1.786e-03	3.883e-03	5.315e-03	7.476e-03
C to Z	1.563e-03	3.380e-03	4.760e-03	6.700e-03
	X46_P4			
A (output stable)	3.975e-04			
B (output stable)	4.788e-04			
C (output stable)	1.760e-03			
A to Z	1.847e-02			
B to Z	1.437e-02			
C to Z	1.293e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	1.594e-07	2.456e-07	2.567e-07	5.858e-07
B (output stable)	1.652e-06	3.834e-06	5.682e-06	3.221e-05
C (output stable)	5.740e-08	-4.420e-08	-9.350e-08	-1.790e-07
A to Z	5.920e-07	1.161e-06	9.200e-07	1.703e-06
B to Z	7.332e-07	3.910e-07	4.790e-07	-1.094e-06
C to Z	8.537e-07	2.726e-06	2.871e-06	3.127e-06

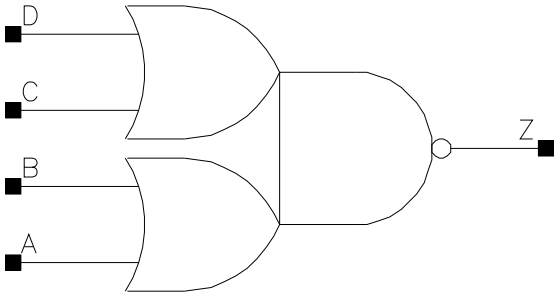
	X46_P4			
A (output stable)	9.114e-07			
B (output stable)	5.275e-05			
C (output stable)	-4.641e-07			
A to Z	3.740e-06			
B to Z	9.340e-07			
C to Z	9.755e-06			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0010	0.0019	0.0027	0.0038
B	0.0009	0.0017	0.0025	0.0035
C	0.0009	0.0018	0.0027	0.0037
D	0.0009	0.0017	0.0025	0.0035
	X42_P4			
A	0.0077			
B	0.0071			
C	0.0073			
D	0.0070			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0101	0.0110	2.6995	1.3438
A to Z ↑	0.0192	0.0193	5.2954	2.4385
B to Z ↓	0.0086	0.0090	2.6422	1.3490
B to Z ↑	0.0198	0.0188	5.3108	2.4498
C to Z ↓	0.0094	0.0103	2.7779	1.3712
C to Z ↑	0.0140	0.0148	5.1760	2.4468
D to Z ↓	0.0074	0.0078	2.7043	1.3808
D to Z ↑	0.0142	0.0135	5.2022	2.4637
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0105	0.0107	0.9191	0.6632
A to Z ↑	0.0182	0.0189	1.6416	1.2131
B to Z ↓	0.0088	0.0086	0.9226	0.6631
B to Z ↑	0.0182	0.0185	1.6504	1.2188
C to Z ↓	0.0100	0.0100	0.9401	0.6775
C to Z ↑	0.0139	0.0140	1.6479	1.2151
D to Z ↓	0.0078	0.0076	0.9488	0.6806
D to Z ↑	0.0132	0.0132	1.6603	1.2235
	X42_P4		**X42_P4**	
A to Z ↓	0.0110		0.3483	
A to Z ↑	0.0190		0.6186	
B to Z ↓	0.0090		0.3445	
B to Z ↑	0.0188		0.6214	
C to Z ↓	0.0108		0.3567	
C to Z ↑	0.0144		0.6152	
D to Z ↓	0.0082		0.3536	
D to Z ↑	0.0136		0.6195	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P4	2.006e-05	1.310e-09
X10_P4	4.066e-05	2.139e-09
X15_P4	5.666e-05	2.635e-09
X21_P4	7.617e-05	3.464e-09
X42_P4	1.470e-04	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	5.083e-05	1.557e-04	2.036e-04	2.952e-04
B (output stable)	6.110e-05	2.248e-04	2.648e-04	3.895e-04
C (output stable)	8.959e-05	2.434e-04	3.181e-04	4.506e-04
D (output stable)	1.037e-04	3.142e-04	3.743e-04	5.418e-04
A to Z	2.567e-03	5.759e-03	7.996e-03	1.123e-02
B to Z	2.214e-03	4.657e-03	6.537e-03	9.111e-03
C to Z	1.927e-03	4.419e-03	6.154e-03	8.444e-03
D to Z	1.606e-03	3.393e-03	4.784e-03	6.537e-03
	X42_P4			
A (output stable)	5.880e-04			
B (output stable)	7.643e-04			
C (output stable)	8.913e-04			
D (output stable)	1.081e-03			

A to Z	2.240e-02			
B to Z	1.822e-02			
C to Z	1.710e-02			
D to Z	1.329e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

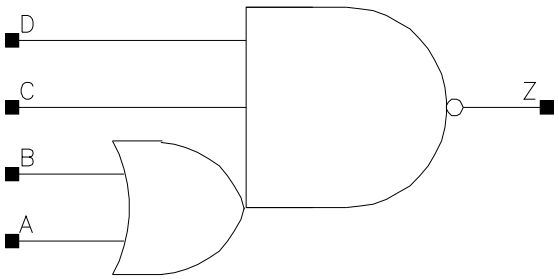
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	2.177e-07	4.512e-07	3.997e-07	7.901e-07
B (output stable)	3.625e-06	3.964e-05	2.455e-05	5.612e-05
C (output stable)	1.534e-07	3.015e-07	2.508e-07	5.327e-07
D (output stable)	3.032e-06	3.891e-05	2.366e-05	5.419e-05
A to Z	4.887e-07	2.855e-06	1.383e-06	4.804e-06
B to Z	7.360e-08	1.337e-06	1.721e-06	1.834e-06
C to Z	9.063e-07	3.271e-06	1.231e-06	2.643e-06
D to Z	5.055e-07	1.299e-06	3.071e-06	2.959e-06
	X42_P4			
A (output stable)	1.212e-06			
B (output stable)	9.793e-05			
C (output stable)	6.773e-07			
D (output stable)	9.747e-05			
A to Z	8.290e-06			
B to Z	5.789e-06			
C to Z	5.100e-06			
D to Z	3.129e-06			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X21_P4	1.200	2.448	2.9376
X31_P4	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X21_P4	X31_P4
A	0.0009	0.0017	0.0035	0.0053
B	0.0011	0.0017	0.0033	0.0049
C	0.0009	0.0019	0.0038	0.0058
D	0.0009	0.0018	0.0037	0.0055

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0138	0.0134	3.6358	1.9527
A to Z ↑	0.0175	0.0161	4.8092	2.4217
B to Z ↓	0.0119	0.0105	3.6940	1.9638
B to Z ↑	0.0178	0.0152	4.8485	2.4380
C to Z ↓	0.0117	0.0120	3.4253	1.8342

C to Z ↑	0.0159	0.0155	2.5075	1.2634
D to Z ↓	0.0128	0.0122	3.4489	1.8461
D to Z ↑	0.0150	0.0140	2.5410	1.2672
	X21_P4	**X31_P4**	**X21_P4**	**X31_P4**
A to Z ↓	0.0136	0.0138	1.0192	0.6924
A to Z ↑	0.0157	0.0158	1.2103	0.8127
B to Z ↓	0.0107	0.0109	1.0259	0.6995
B to Z ↑	0.0150	0.0149	1.2182	0.8189
C to Z ↓	0.0119	0.0120	0.9586	0.6523
C to Z ↑	0.0152	0.0152	0.6406	0.4325
D to Z ↓	0.0123	0.0126	0.9645	0.6563
D to Z ↑	0.0138	0.0139	0.6416	0.4322

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P4	1.566e-05	1.476e-09
X10_P4	2.905e-05	2.139e-09
X21_P4	5.415e-05	3.464e-09
X31_P4	7.931e-05	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	1.555e-04	3.375e-04	6.221e-04	9.248e-04
B (output stable)	1.586e-04	3.502e-04	6.458e-04	9.520e-04
C (output stable)	5.087e-05	1.436e-04	2.750e-04	4.112e-04
D (output stable)	6.945e-05	2.402e-04	4.445e-04	6.450e-04
A to Z	2.566e-03	4.556e-03	8.865e-03	1.320e-02
B to Z	2.055e-03	3.499e-03	6.788e-03	1.013e-02
C to Z	3.071e-03	5.862e-03	1.130e-02	1.683e-02
D to Z	2.782e-03	5.051e-03	9.749e-03	1.452e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

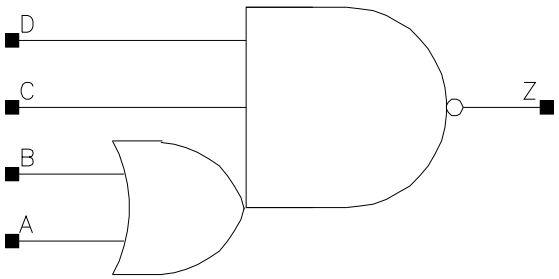
Pin Cycle (vdds)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	-1.851e-07	-4.315e-07	-1.111e-06	-1.507e-06
B (output stable)	5.176e-06	8.123e-06	1.238e-05	1.703e-05
C (output stable)	6.396e-08	3.868e-08	-5.280e-08	-1.334e-07
D (output stable)	4.501e-08	-6.742e-08	-3.155e-07	-4.707e-07
A to Z	6.610e-07	1.361e-06	1.657e-06	2.830e-06
B to Z	2.980e-07	8.300e-08	-1.440e-06	-2.293e-06
C to Z	1.423e-06	9.430e-07	3.305e-06	4.667e-06
D to Z	1.114e-06	9.080e-07	2.045e-06	2.617e-06

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0010	0.0019	0.0029	0.0038
B	0.0009	0.0018	0.0026	0.0035
C	0.0009	0.0018	0.0028	0.0037
D	0.0009	0.0018	0.0027	0.0036

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0120	0.0130	3.7033	1.9390
A to Z ↑	0.0192	0.0208	4.6610	2.3800
B to Z ↓	0.0101	0.0107	3.6335	1.9420
B to Z ↑	0.0199	0.0205	4.6811	2.3905
C to Z ↓	0.0100	0.0112	3.5051	1.8527

C to Z ↑	0.0125	0.0132	2.5535	1.2912
D to Z ↓	0.0103	0.0109	3.5330	1.8657
D to Z ↑	0.0109	0.0110	2.5721	1.3017
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0128	0.0129	1.3341	1.0076
A to Z ↑	0.0200	0.0204	1.6052	1.2179
B to Z ↓	0.0107	0.0106	1.3286	1.0062
B to Z ↑	0.0200	0.0205	1.6131	1.2232
C to Z ↓	0.0109	0.0111	1.2705	0.9602
C to Z ↑	0.0125	0.0128	0.8621	0.6481
D to Z ↓	0.0108	0.0111	1.2795	0.9664
D to Z ↑	0.0106	0.0108	0.8684	0.6528

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P4	1.560e-05	1.476e-09
X10_P4	3.027e-05	2.139e-09
X15_P4	4.176e-05	2.635e-09
X21_P4	5.725e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	3.134e-05	7.046e-05	1.040e-04	1.351e-04
B (output stable)	3.192e-05	8.486e-05	1.167e-04	1.553e-04
C (output stable)	7.197e-05	1.690e-04	2.526e-04	3.370e-04
D (output stable)	1.253e-04	4.237e-04	5.154e-04	7.513e-04
A to Z	2.866e-03	6.190e-03	8.809e-03	1.200e-02
B to Z	2.444e-03	5.057e-03	7.179e-03	9.819e-03
C to Z	2.103e-03	4.559e-03	6.402e-03	8.771e-03
D to Z	1.858e-03	3.831e-03	5.492e-03	7.416e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

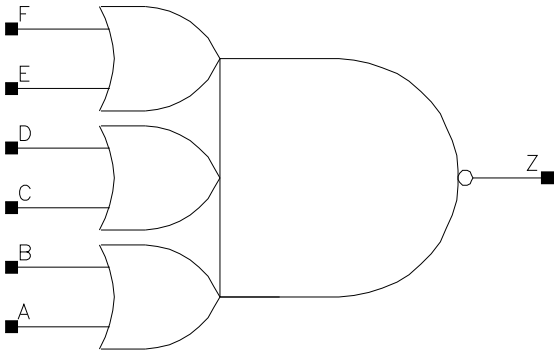
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	1.405e-07	3.477e-07	2.800e-07	4.028e-07
B (output stable)	8.513e-07	9.686e-06	7.602e-06	1.445e-05
C (output stable)	6.553e-08	1.747e-08	-6.052e-08	-8.528e-08
D (output stable)	6.756e-08	-1.543e-07	-2.106e-07	-3.398e-07
A to Z	7.200e-07	1.097e-06	1.637e-06	3.102e-06
B to Z	2.920e-07	-3.580e-07	3.510e-07	3.980e-07
C to Z	6.043e-07	1.069e-06	2.460e-06	3.447e-06
D to Z	4.883e-07	1.405e-06	1.314e-06	2.144e-06

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	1.088	1.3056
X9_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X9_P4
A	0.0008	0.0019
B	0.0008	0.0018
C	0.0008	0.0019
D	0.0007	0.0017
E	0.0008	0.0018
F	0.0008	0.0017

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X9_P4	X3_P4	X9_P4
A to Z ↓	0.0157	0.0169	4.2295	1.7638
A to Z ↑	0.0260	0.0249	6.4750	2.3958
B to Z ↓	0.0145	0.0147	4.2662	1.7672
B to Z ↑	0.0276	0.0248	6.4957	2.4043
C to Z ↓	0.0155	0.0163	4.2752	1.7766
C to Z ↑	0.0224	0.0214	6.5005	2.3928
D to Z ↓	0.0139	0.0140	4.3152	1.7827
D to Z ↑	0.0237	0.0211	6.5274	2.4038
E to Z ↓	0.0136	0.0148	4.3293	1.7886
E to Z ↑	0.0172	0.0167	6.5285	2.3977
F to Z ↓	0.0121	0.0121	4.3746	1.7946
F to Z ↑	0.0182	0.0158	6.5715	2.4139

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P4	1.920e-05	1.807e-09
X9_P4	4.708e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P4	X9_P4
A (output stable)	4.312e-05	1.462e-04
B (output stable)	4.764e-05	1.894e-04
C (output stable)	6.629e-05	1.949e-04
D (output stable)	7.082e-05	2.442e-04
E (output stable)	1.719e-04	4.376e-04
F (output stable)	1.786e-04	4.750e-04
A to Z	3.274e-03	8.473e-03
B to Z	2.978e-03	7.281e-03
C to Z	2.691e-03	6.959e-03
D to Z	2.412e-03	5.906e-03
E to Z	2.041e-03	5.508e-03
F to Z	1.793e-03	4.474e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

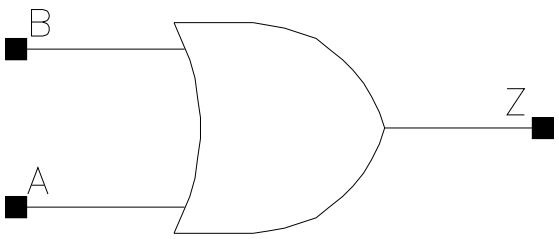
Pin Cycle (vdds)	X3_P4	X9_P4
A (output stable)	1.637e-07	4.221e-07
B (output stable)	1.994e-06	2.639e-05
C (output stable)	1.092e-07	1.989e-07
D (output stable)	2.095e-06	2.465e-05
E (output stable)	-4.532e-08	-2.272e-07
F (output stable)	1.800e-06	2.513e-05
A to Z	6.213e-07	2.746e-06
B to Z	3.583e-07	1.331e-06
C to Z	1.598e-07	2.469e-06
D to Z	-2.093e-07	9.122e-07
E to Z	6.996e-07	3.667e-06
F to Z	2.956e-07	1.787e-06

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X33_P4	1.200	1.360	1.6320
X50_P4	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P4	X16_P4	X33_P4	X50_P4
A	0.0008	0.0010	0.0020	0.0021
B	0.0007	0.0010	0.0021	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0282	0.0257	1.6585	0.8346
A to Z ↑	0.0171	0.0185	2.4929	1.2564
B to Z ↓	0.0293	0.0267	1.6573	0.8341
B to Z ↑	0.0159	0.0170	2.4922	1.2564
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0266	0.0315	0.4131	0.2835
A to Z ↑	0.0183	0.0183	0.6134	0.4144
B to Z ↓	0.0265	0.0320	0.4130	0.2838
B to Z ↑	0.0165	0.0169	0.6125	0.4147

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	2.541e-05	1.145e-09
X16_P4	4.492e-05	1.310e-09
X33_P4	8.796e-05	2.139e-09
X50_P4	1.179e-04	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	3.339e-05	6.148e-05	1.931e-04	1.829e-04
B (output stable)	4.302e-05	8.004e-05	3.150e-04	2.967e-04
A to Z	3.488e-03	5.893e-03	1.228e-02	1.731e-02
B to Z	3.295e-03	5.576e-03	1.127e-02	1.640e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

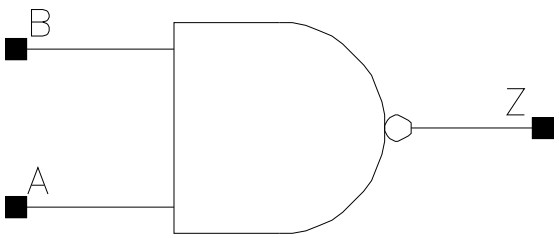
Pin Cycle (vdds)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	2.086e-07	2.966e-07	4.566e-07	5.292e-07
B (output stable)	5.069e-06	5.740e-06	6.418e-05	5.951e-05
A to Z	1.834e-07	2.248e-07	1.062e-06	7.360e-07
B to Z	1.465e-06	6.911e-07	1.530e-06	1.182e-06

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X16_P4	1.200	0.952	1.1424
X24_P4	1.200	1.088	1.3056
X32_P4	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P4	X16_P4	X24_P4	X32_P4
A	0.0011	0.0011	0.0011	0.0011
B	0.0011	0.0012	0.0012	0.0012

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0226	0.0237	1.6083	0.8351
A to Z ↑	0.0268	0.0277	2.5274	1.2880
B to Z ↓	0.0238	0.0250	1.6087	0.8353
B to Z ↑	0.0254	0.0259	2.5264	1.2872
	X24_P4	**X32_P4**	**X24_P4**	**X32_P4**
A to Z ↓	0.0264	0.0270	0.5641	0.4225
A to Z ↑	0.0297	0.0302	0.8609	0.6425
B to Z ↓	0.0276	0.0285	0.5645	0.4225
B to Z ↑	0.0278	0.0289	0.8612	0.6426

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	4.318e-05	1.476e-09
X16_P4	5.864e-05	1.642e-09
X24_P4	7.296e-05	1.807e-09
X32_P4	9.068e-05	1.973e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	3.290e-05	3.300e-05	3.308e-05	3.559e-05
B (output stable)	4.460e-05	4.488e-05	4.506e-05	4.493e-05
A to Z	6.416e-03	7.636e-03	9.746e-03	1.276e-02
B to Z	6.174e-03	7.407e-03	9.524e-03	1.252e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

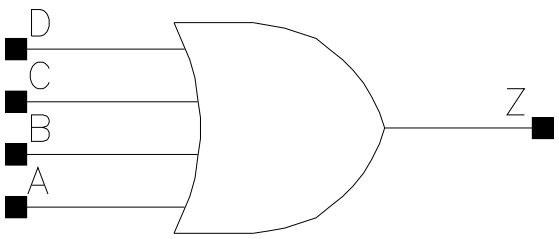
Pin Cycle (vdds)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	6.339e-08	6.617e-08	6.587e-08	7.059e-08
B (output stable)	7.061e-08	7.024e-08	7.063e-08	7.391e-08
A to Z	1.235e-06	7.827e-07	6.920e-07	4.400e-08
B to Z	2.583e-07	9.580e-08	-5.000e-09	-1.520e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P4	1.200	2.176	2.6112
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P4	X27_P4
A	0.0018	0.0021
B	0.0017	0.0021
C	0.0018	0.0021
D	0.0017	0.0022

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P4	X27_P4	X20_P4	X27_P4
A to Z ↓	0.0289	0.0303	0.9300	0.6947
A to Z ↑	0.0189	0.0182	0.8227	0.6135
B to Z ↓	0.0291	0.0302	0.9297	0.6955
B to Z ↑	0.0175	0.0165	0.8224	0.6130
C to Z ↓	0.0283	0.0300	0.9290	0.6951
C to Z ↑	0.0179	0.0178	0.8234	0.6149
D to Z ↓	0.0286	0.0302	0.9289	0.6944
D to Z ↑	0.0166	0.0163	0.8228	0.6142

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X20_P4	6.696e-05	3.132e-09
X27_P4	9.250e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X20_P4	X27_P4
A (output stable)	2.509e-03	3.447e-03
B (output stable)	2.218e-03	3.041e-03
C (output stable)	2.215e-03	3.142e-03
D (output stable)	1.919e-03	2.783e-03
A to Z	1.058e-02	1.475e-02
B to Z	9.837e-03	1.364e-02
C to Z	9.562e-03	1.330e-02
D to Z	8.832e-03	1.233e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

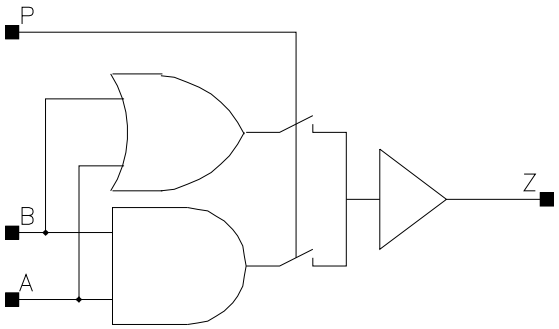
Pin Cycle (vdds)	X20_P4	X27_P4
A (output stable)	2.260e-07	5.608e-07
B (output stable)	1.590e-05	3.700e-05
C (output stable)	5.157e-07	9.783e-07
D (output stable)	1.579e-05	4.081e-05
A to Z	1.950e-06	9.834e-07
B to Z	2.586e-06	5.670e-06
C to Z	2.256e-06	1.071e-06
D to Z	3.024e-06	4.793e-06

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X16_P4	1.200	1.224	1.4688
X25_P4	1.200	2.040	2.4480
X33_P4	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0013	0.0019	0.0034	0.0034
B	0.0013	0.0019	0.0039	0.0039
P	0.0007	0.0011	0.0020	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0342	0.0316	1.6888	0.8259
A to Z ↑	0.0225	0.0214	2.5306	1.2646
B to Z ↓	0.0345	0.0321	1.6973	0.8307
B to Z ↑	0.0235	0.0224	2.5317	1.2664
P to Z ↓	0.0323	0.0304	1.6962	0.8303
P to Z ↑	0.0230	0.0221	2.5300	1.2644
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**

A to Z ↓	0.0303	0.0326	0.5607	0.4240
A to Z ↑	0.0212	0.0226	0.8514	0.6375
B to Z ↓	0.0306	0.0326	0.5636	0.4258
B to Z ↑	0.0225	0.0237	0.8520	0.6377
P to Z ↓	0.0294	0.0317	0.5635	0.4259
P to Z ↑	0.0217	0.0231	0.8501	0.6363

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	2.456e-05	1.642e-09
X16_P4	4.853e-05	1.973e-09
X25_P4	7.956e-05	2.967e-09
X33_P4	9.111e-05	3.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	6.909e-05	1.121e-04	2.448e-04	2.453e-04
B (output stable)	7.748e-05	1.409e-04	3.505e-04	3.540e-04
P (output stable)	1.615e-04	3.005e-04	4.991e-04	5.105e-04
A to Z	4.022e-03	7.092e-03	1.190e-02	1.436e-02
B to Z	3.925e-03	6.972e-03	1.149e-02	1.396e-02
P to Z	3.675e-03	6.628e-03	1.106e-02	1.351e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

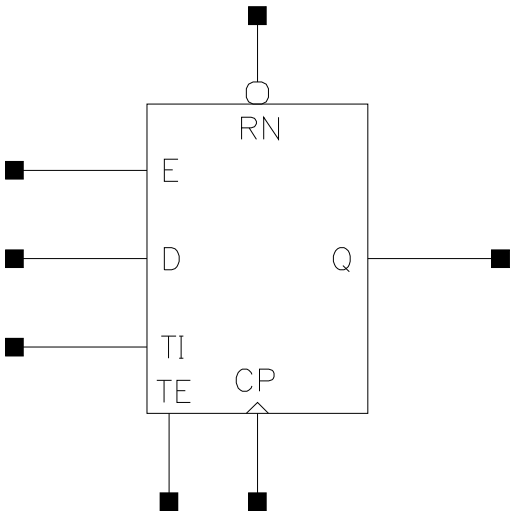
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	1.313e-07	2.741e-07	4.668e-07	4.796e-07
B (output stable)	2.677e-06	2.758e-06	1.267e-05	1.275e-05
P (output stable)	1.564e-05	2.100e-05	2.207e-05	2.181e-05
A to Z	1.003e-07	3.382e-07	1.750e-07	4.550e-08
B to Z	1.615e-08	1.785e-07	-1.949e-07	-2.327e-07
P to Z	7.235e-08	1.901e-07	2.405e-07	3.162e-07

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.488	5.3856
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0011	0.0011
RN	0.0009	0.0007	0.0008	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.0599	0.0331	3.4837	1.6433
CP to Q ↑	0.0506	0.0433	4.9506	2.5041
RN to Q ↓	0.0436	0.0513	3.1111	1.5989
	X17_P4	X33_P4	X17_P4	X33_P4
CP to Q ↓	0.0575	0.0608	0.8001	0.4191
CP to Q ↑	0.0700	0.0735	1.2297	0.6272
RN to Q ↓	0.0698	0.0739	0.8001	0.4192

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0799	0.0552	0.0552	0.0552
CP ↑	min_pulse_width to CP	0.0531	0.0290	0.0242	0.0242
D ↓	hold_rising to CP	-0.0841	-0.0385	-0.0385	-0.0385
D ↑	hold_rising to CP	-0.0505	-0.0116	-0.0116	-0.0116
D ↓	setup_rising to CP	0.1186	0.0752	0.0752	0.0752
D ↑	setup_rising to CP	0.0773	0.0419	0.0419	0.0419
E ↓	hold_rising to CP	-0.0579	-0.0576	-0.0576	-0.0576
E ↑	hold_rising to CP	-0.0459	-0.0120	-0.0120	-0.0120
E ↓	setup_rising to CP	0.1018	0.1044	0.1048	0.1044
E ↑	setup_rising to CP	0.1103	0.0779	0.0779	0.0779
RN ↓	min_pulse_width to RN	0.0588	0.0637	0.0566	0.0566
RN ↑	recovery_rising to CP	0.0149	0.0127	0.0127	0.0127
RN ↑	removal_rising to CP	-0.0101	-0.0027	-0.0027	-0.0027
TE ↓	hold_rising to CP	-0.0328	-0.0230	-0.0230	-0.0230
TE ↑	hold_rising to CP	-0.0309	-0.0184	-0.0184	-0.0184
TE ↓	setup_rising to CP	0.0751	0.0631	0.0631	0.0631
TE ↑	setup_rising to CP	0.1393	0.0950	0.0950	0.0950
TI ↓	hold_rising to CP	-0.1077	-0.0514	-0.0514	-0.0514
TI ↑	hold_rising to CP	-0.0369	-0.0187	-0.0187	-0.0187
TI ↓	setup_rising to CP	0.1430	0.0916	0.0916	0.0916
TI ↑	setup_rising to CP	0.0671	0.0445	0.0445	0.0445

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	9.154e-05	6.340e-09
X8_P4	9.839e-05	5.948e-09
X17_P4	1.198e-04	6.279e-09
X33_P4	1.440e-04	6.611e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

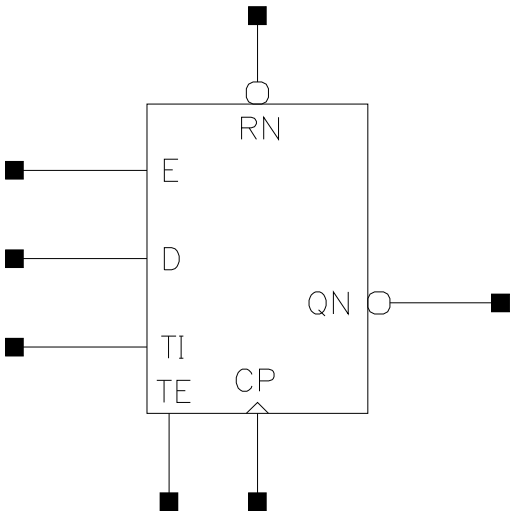
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.837e-03	5.871e-03	5.879e-03	5.883e-03
Clock 100Mhz Data 25Mhz	9.780e-03	9.826e-03	1.075e-02	1.200e-02
Clock 100Mhz Data 50Mhz	1.372e-02	1.378e-02	1.562e-02	1.811e-02
Clock = 0 Data 100Mhz	9.052e-03	8.559e-03	8.397e-03	8.317e-03
Clock = 1 Data 100Mhz	3.103e-03	3.170e-03	3.194e-03	3.206e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.624	5.5488
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0011	0.0011
RN	0.0009	0.0009	0.0009	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.0618	0.0579	2.9531	1.5885
CP to QN ↑	0.0675	0.0446	4.8521	2.4345
RN to QN ↑	0.0546	0.0579	4.8463	2.4365
	X17_P4	X33_P4	X17_P4	X33_P4
CP to QN ↓	0.0559	0.0595	0.8004	0.4184
CP to QN ↑	0.0465	0.0508	1.2311	0.6276
RN to QN ↑	0.0633	0.0665	1.2285	0.6269

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0799	0.0557	0.0552	0.0552
CP ↑	min_pulse_width to CP	0.0386	0.0242	0.0253	0.0290
D ↓	hold_rising to CP	-0.0838	-0.0385	-0.0385	-0.0385
D ↑	hold_rising to CP	-0.0505	-0.0116	-0.0116	-0.0116
D ↓	setup_rising to CP	0.1186	0.0752	0.0752	0.0752
D ↑	setup_rising to CP	0.0773	0.0419	0.0419	0.0419
E ↓	hold_rising to CP	-0.0576	-0.0576	-0.0576	-0.0576
E ↑	hold_rising to CP	-0.0459	-0.0120	-0.0120	-0.0120
E ↓	setup_rising to CP	0.1048	0.1048	0.1044	0.1044
E ↑	setup_rising to CP	0.1103	0.0779	0.0779	0.0779
RN ↓	min_pulse_width to RN	0.0540	0.0566	0.0637	0.0708
RN ↑	recovery_rising to CP	0.0149	0.0124	0.0127	0.0127
RN ↑	removal_rising to CP	-0.0101	-0.0052	-0.0027	-0.0027
TE ↓	hold_rising to CP	-0.0358	-0.0230	-0.0230	-0.0234
TE ↑	hold_rising to CP	-0.0309	-0.0184	-0.0184	-0.0159
TE ↓	setup_rising to CP	0.0751	0.0631	0.0631	0.0631
TE ↑	setup_rising to CP	0.1393	0.0950	0.0950	0.0950
TI ↓	hold_rising to CP	-0.1077	-0.0514	-0.0514	-0.0514
TI ↑	hold_rising to CP	-0.0369	-0.0187	-0.0187	-0.0187
TI ↓	setup_rising to CP	0.1430	0.0916	0.0916	0.0916
TI ↑	setup_rising to CP	0.0671	0.0445	0.0445	0.0445

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	9.548e-05	6.340e-09
X8_P4	1.040e-04	6.114e-09
X17_P4	1.260e-04	6.279e-09
X33_P4	1.549e-04	6.611e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

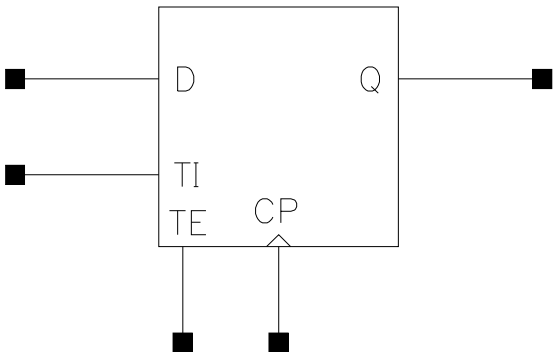
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.835e-03	5.869e-03	5.874e-03	5.877e-03
Clock 100Mhz Data 25Mhz	9.616e-03	9.854e-03	1.072e-02	1.198e-02
Clock 100Mhz Data 50Mhz	1.340e-02	1.384e-02	1.556e-02	1.809e-02
Clock = 0 Data 100Mhz	9.057e-03	8.563e-03	8.402e-03	8.321e-03
Clock = 1 Data 100Mhz	3.100e-03	3.171e-03	3.197e-03	3.210e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.400	4.0800
X8_P4	1.200	3.128	3.7536
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0009	0.0009
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0495	0.0308	3.3015	1.6456
CP to Q ↑	0.0455	0.0394	4.9769	2.4732
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0476	0.0522	0.7869	0.4123
CP to Q ↑	0.0674	0.0716	1.2280	0.6264

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0745	0.0789	0.0789	0.0789
CP ↑	min_pulse_width to CP	0.0386	0.0242	0.0205	0.0205
D ↓	hold_rising to CP	-0.0527	-0.0184	-0.0215	-0.0215
D ↑	hold_rising to CP	-0.0159	0.0057	0.0027	0.0027
D ↓	setup_rising to CP	0.0826	0.0561	0.0561	0.0561
D ↑	setup_rising to CP	0.0407	0.0221	0.0221	0.0221
TE ↓	hold_rising to CP	-0.0279	-0.0166	-0.0166	-0.0166
TE ↑	hold_rising to CP	-0.0208	-0.0088	-0.0088	-0.0088
TE ↓	setup_rising to CP	0.0681	0.0514	0.0512	0.0512
TE ↑	setup_rising to CP	0.1242	0.1024	0.1024	0.1024
TI ↓	hold_rising to CP	-0.1028	-0.0630	-0.0630	-0.0630
TI ↑	hold_rising to CP	-0.0256	-0.0098	-0.0098	-0.0098
TI ↓	setup_rising to CP	0.1327	0.1026	0.1026	0.1026
TI ↑	setup_rising to CP	0.0520	0.0386	0.0386	0.0386

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	7.271e-05	4.623e-09
X8_P4	8.096e-05	4.292e-09
X17_P4	1.107e-04	4.789e-09
X33_P4	1.336e-04	5.120e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

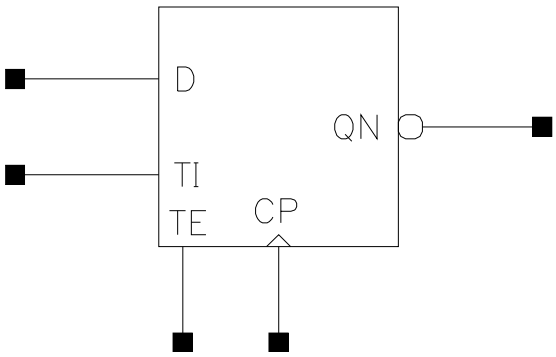
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.318e-03	5.357e-03	5.366e-03	5.371e-03
Clock 100Mhz Data 25Mhz	8.106e-03	8.132e-03	9.093e-03	1.016e-02
Clock 100Mhz Data 50Mhz	1.089e-02	1.091e-02	1.282e-02	1.496e-02
Clock = 0 Data 100Mhz	7.106e-03	6.594e-03	6.423e-03	6.339e-03
Clock = 1 Data 100Mhz	1.764e-03	9.144e-04	6.313e-04	4.898e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.536	4.2432
X8_P4	1.200	3.264	3.9168
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0009	0.0009
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0578	0.0606	3.3747	1.6353
CP to QN ↑	0.0541	0.0410	4.9427	2.4416
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0481	0.0532	0.7884	0.4123
CP to QN ↑	0.0407	0.0452	1.2293	0.6256

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0745	0.0789	0.0789	0.0789
CP ↑	min_pulse_width to CP	0.0290	0.0242	0.0242	0.0253
D ↓	hold_rising to CP	-0.0527	-0.0215	-0.0159	-0.0163
D ↑	hold_rising to CP	-0.0159	0.0057	0.0057	0.0057
D ↓	setup_rising to CP	0.0826	0.0561	0.0561	0.0561
D ↑	setup_rising to CP	0.0407	0.0221	0.0221	0.0221
TE ↓	hold_rising to CP	-0.0279	-0.0166	-0.0166	-0.0166
TE ↑	hold_rising to CP	-0.0208	-0.0088	-0.0088	-0.0088
TE ↓	setup_rising to CP	0.0681	0.0512	0.0512	0.0512
TE ↑	setup_rising to CP	0.1246	0.1024	0.1024	0.1024
TI ↓	hold_rising to CP	-0.1028	-0.0630	-0.0631	-0.0631
TI ↑	hold_rising to CP	-0.0271	-0.0098	-0.0098	-0.0098
TI ↓	setup_rising to CP	0.1327	0.1026	0.1026	0.1026
TI ↑	setup_rising to CP	0.0561	0.0386	0.0386	0.0386

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	7.382e-05	4.789e-09
X8_P4	8.185e-05	4.457e-09
X17_P4	1.097e-04	4.789e-09
X33_P4	1.326e-04	5.120e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

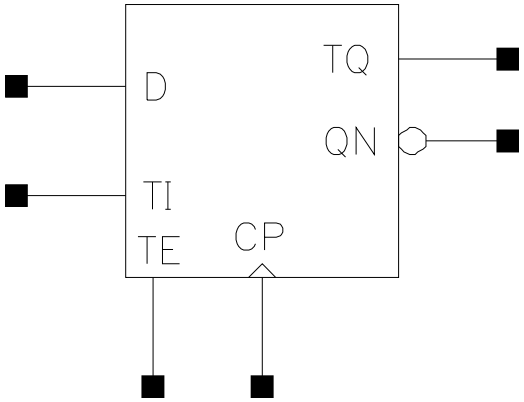
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.264e-03	5.327e-03	5.348e-03	5.358e-03
Clock 100Mhz Data 25Mhz	8.016e-03	8.258e-03	9.023e-03	1.012e-02
Clock 100Mhz Data 50Mhz	1.077e-02	1.119e-02	1.270e-02	1.489e-02
Clock = 0 Data 100Mhz	7.140e-03	6.607e-03	6.433e-03	6.345e-03
Clock = 1 Data 100Mhz	1.753e-03	9.092e-04	6.280e-04	4.874e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.536	4.2432
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0013	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0640	0.0553	3.0636	1.6039
CP to QN ↑	0.0655	0.0428	4.8841	2.4557
CP to TQ ↓	0.0450	0.0282	4.1579	2.9607
CP to TQ ↑	0.0466	0.0391	8.9936	6.5253
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0529	0.0579	0.8062	0.4221
CP to QN ↑	0.0444	0.0481	1.2447	0.6394
CP to TQ ↓	0.0293	0.0304	3.8687	3.8881
CP to TQ ↑	0.0398	0.0409	8.3724	8.8347

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0745	0.0789	0.0789	0.0789
CP ↑	min_pulse_width to CP	0.0386	0.0242	0.0242	0.0253
D ↓	hold_rising to CP	-0.0527	-0.0163	-0.0163	-0.0163
D ↑	hold_rising to CP	-0.0163	0.0057	0.0057	0.0057
D ↓	setup_rising to CP	0.0826	0.0564	0.0564	0.0564
D ↑	setup_rising to CP	0.0407	0.0221	0.0221	0.0221
TE ↓	hold_rising to CP	-0.0279	-0.0141	-0.0141	-0.0141
TE ↑	hold_rising to CP	-0.0208	-0.0088	-0.0088	-0.0088
TE ↓	setup_rising to CP	0.0681	0.0512	0.0512	0.0512
TE ↑	setup_rising to CP	0.1249	0.1002	0.1028	0.1028
TI ↓	hold_rising to CP	-0.1028	-0.0631	-0.0631	-0.0631
TI ↑	hold_rising to CP	-0.0256	-0.0098	-0.0098	-0.0098
TI ↓	setup_rising to CP	0.1332	0.1026	0.1026	0.1026
TI ↑	setup_rising to CP	0.0520	0.0386	0.0386	0.0386

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	8.162e-05	5.131e-09
X8_P4	9.138e-05	4.789e-09
X17_P4	1.057e-04	4.954e-09
X33_P4	1.330e-04	5.286e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4

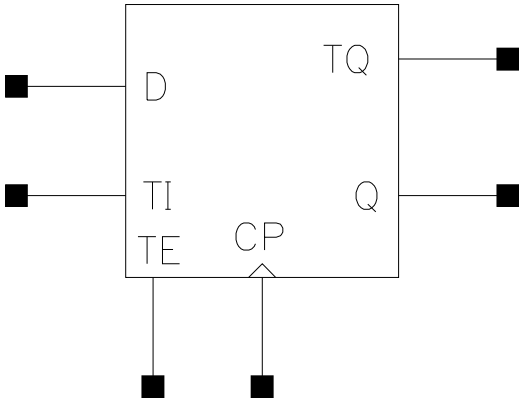
Clock 100Mhz Data 0Mhz	5.393e-03	5.394e-03	5.394e-03	5.395e-03
Clock 100Mhz Data 25Mhz	8.452e-03	8.623e-03	9.085e-03	1.041e-02
Clock 100Mhz Data 50Mhz	1.151e-02	1.185e-02	1.278e-02	1.542e-02
Clock = 0 Data 100Mhz	7.136e-03	6.615e-03	6.444e-03	6.358e-03
Clock = 1 Data 100Mhz	1.764e-03	9.143e-04	6.312e-04	4.898e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.400	4.0800
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0009	0.0009	0.0009
D	0.0010	0.0008	0.0008	0.0008

TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0657	0.0346	3.4606	1.6391
CP to Q ↑	0.0524	0.0421	5.0436	2.4880
CP to TQ ↓	0.0620	0.0355	3.4673	3.9815
CP to TQ ↑	0.0537	0.0458	6.5841	8.9806
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0488	0.0536	0.8086	0.4203
CP to Q ↑	0.0686	0.0729	1.2556	0.6298
CP to TQ ↓	0.0505	0.0559	3.7998	3.8746
CP to TQ ↑	0.0726	0.0784	8.6577	8.7597

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0745	0.0789	0.0789	0.0789
CP ↑	min_pulse_width to CP	0.0579	0.0253	0.0205	0.0223
D ↓	hold_rising to CP	-0.0527	-0.0163	-0.0215	-0.0215
D ↑	hold_rising to CP	-0.0159	0.0057	0.0027	0.0027
D ↓	setup_rising to CP	0.0826	0.0561	0.0561	0.0561
D ↑	setup_rising to CP	0.0407	0.0221	0.0221	0.0221
TE ↓	hold_rising to CP	-0.0279	-0.0141	-0.0166	-0.0166
TE ↑	hold_rising to CP	-0.0208	-0.0088	-0.0088	-0.0088
TE ↓	setup_rising to CP	0.0681	0.0512	0.0512	0.0512
TE ↑	setup_rising to CP	0.1242	0.1028	0.1024	0.1024
TI ↓	hold_rising to CP	-0.1028	-0.0631	-0.0630	-0.0630
TI ↑	hold_rising to CP	-0.0256	-0.0098	-0.0098	-0.0098
TI ↓	setup_rising to CP	0.1327	0.1026	0.1026	0.1026
TI ↑	setup_rising to CP	0.0520	0.0386	0.0386	0.0386

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	8.124e-05	4.954e-09
X8_P4	8.674e-05	4.623e-09
X17_P4	1.153e-04	4.954e-09
X33_P4	1.380e-04	5.286e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

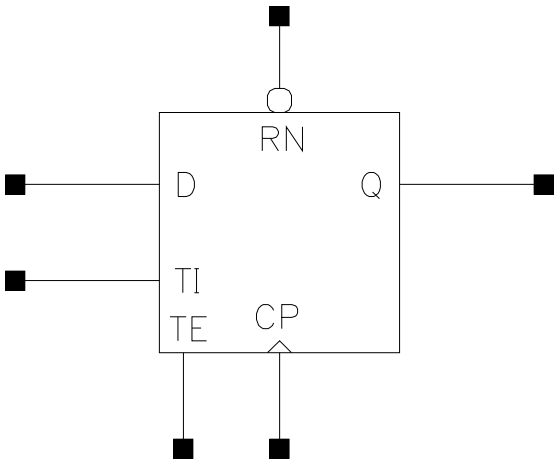
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.296e-03	5.342e-03	5.356e-03	5.363e-03
Clock 100Mhz Data 25Mhz	8.747e-03	8.471e-03	9.346e-03	1.051e-02
Clock 100Mhz Data 50Mhz	1.220e-02	1.160e-02	1.334e-02	1.566e-02
Clock = 0 Data 100Mhz	7.096e-03	6.586e-03	6.420e-03	6.337e-03
Clock = 1 Data 100Mhz	1.751e-03	9.079e-04	6.272e-04	4.868e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.672	4.4064
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0007	0.0007	0.0007
RN	0.0009	0.0007	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0595	0.0330	3.5238	1.6470
CP to Q ↑	0.0502	0.0425	4.9796	2.5036
RN to Q ↓	0.0433	0.0514	3.1265	1.6031
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0497	0.0547	0.7955	0.4183
CP to Q ↑	0.0624	0.0664	1.2265	0.6262
RN to Q ↓	0.0622	0.0672	0.7948	0.4183

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0818	0.0789	0.0818	0.0818
CP ↑	min_pulse_width to CP	0.0531	0.0253	0.0242	0.0242
D ↓	hold_rising to CP	-0.0481	-0.0117	-0.0117	-0.0117
D ↑	hold_rising to CP	-0.0212	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0796	0.0512	0.0512	0.0512
D ↑	setup_rising to CP	0.0512	0.0270	0.0295	0.0295
RN ↓	min_pulse_width to RN	0.0540	0.0588	0.0544	0.0544
RN ↑	recovery_rising to CP	0.0149	0.0127	0.0127	0.0127
RN ↑	removal_rising to CP	-0.0101	-0.0052	-0.0052	-0.0052
TE ↓	hold_rising to CP	-0.0335	-0.0095	-0.0095	-0.0095
TE ↑	hold_rising to CP	-0.0312	-0.0168	-0.0193	-0.0193
TE ↓	setup_rising to CP	0.0681	0.0512	0.0512	0.0512
TE ↑	setup_rising to CP	0.1194	0.0957	0.0957	0.0957
TI ↓	hold_rising to CP	-0.0931	-0.0478	-0.0519	-0.0519
TI ↑	hold_rising to CP	-0.0318	-0.0202	-0.0200	-0.0200
TI ↓	setup_rising to CP	0.1278	0.0924	0.0964	0.0964
TI ↑	setup_rising to CP	0.0617	0.0443	0.0458	0.0458

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	8.051e-05	5.286e-09
X8_P4	8.657e-05	4.954e-09
X17_P4	1.138e-04	5.451e-09
X33_P4	1.332e-04	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.835e-03	5.859e-03	5.893e-03	5.910e-03

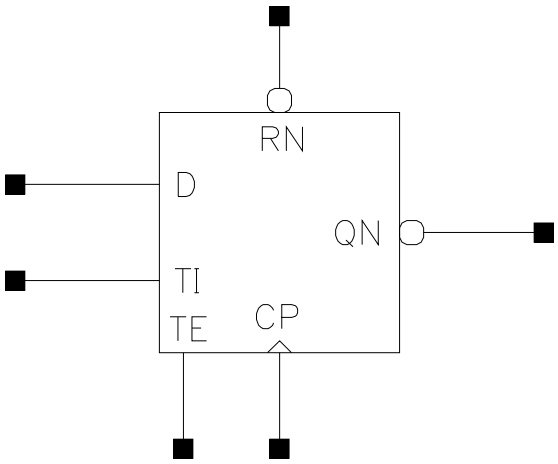
Clock 100Mhz Data 25Mhz	9.043e-03	8.851e-03	9.885e-03	1.100e-02
Clock 100Mhz Data 50Mhz	1.225e-02	1.184e-02	1.388e-02	1.609e-02
Clock = 0 Data 100Mhz	7.103e-03	6.495e-03	6.296e-03	6.196e-03
Clock = 1 Data 100Mhz	1.793e-03	9.313e-04	6.440e-04	5.005e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	3.944	4.7328
X33_P4	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0007	0.0007	0.0007
RN	0.0009	0.0009	0.0009	0.0009
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0560	0.0520	2.9062	1.5551
CP to QN ↑	0.0615	0.0402	4.8571	2.4229
RN to QN ↑	0.0494	0.0531	4.8462	2.4259
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0521	0.0573	0.7951	0.4176
CP to QN ↑	0.0445	0.0492	1.2377	0.6342
RN to QN ↑	0.0620	0.0662	1.2351	0.6329

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0818	0.0789	0.0789	0.0789
CP ↑	min_pulse_width to CP	0.0386	0.0242	0.0253	0.0290
D ↓	hold_rising to CP	-0.0478	-0.0117	-0.0117	-0.0117
D ↑	hold_rising to CP	-0.0212	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0796	0.0512	0.0512	0.0512
D ↑	setup_rising to CP	0.0512	0.0270	0.0270	0.0295
RN ↓	min_pulse_width to RN	0.0540	0.0544	0.0637	0.0659
RN ↑	recovery_rising to CP	0.0149	0.0149	0.0124	0.0124
RN ↑	removal_rising to CP	-0.0101	-0.0076	-0.0052	-0.0052
TE ↓	hold_rising to CP	-0.0335	-0.0095	-0.0095	-0.0095
TE ↑	hold_rising to CP	-0.0309	-0.0168	-0.0168	-0.0168
TE ↓	setup_rising to CP	0.0681	0.0512	0.0512	0.0512
TE ↑	setup_rising to CP	0.1194	0.0957	0.0957	0.0957
TI ↓	hold_rising to CP	-0.0931	-0.0519	-0.0478	-0.0478
TI ↑	hold_rising to CP	-0.0359	-0.0200	-0.0202	-0.0202
TI ↓	setup_rising to CP	0.1278	0.0924	0.0965	0.0965
TI ↑	setup_rising to CP	0.0617	0.0443	0.0443	0.0443

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	8.502e-05	5.347e-09
X8_P4	9.217e-05	5.120e-09
X17_P4	1.169e-04	5.286e-09
X33_P4	1.426e-04	5.617e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.791e-03	5.836e-03	5.850e-03	5.857e-03

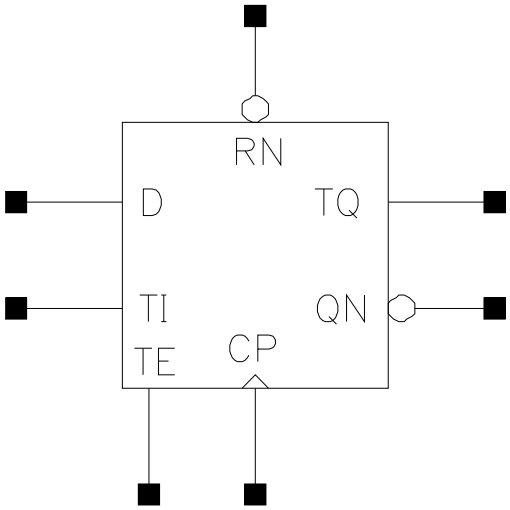
Clock 100Mhz Data 25Mhz	8.767e-03	8.810e-03	9.763e-03	1.087e-02
Clock 100Mhz Data 50Mhz	1.174e-02	1.178e-02	1.368e-02	1.589e-02
Clock = 0 Data 100Mhz	7.104e-03	6.494e-03	6.297e-03	6.198e-03
Clock = 1 Data 100Mhz	1.792e-03	9.307e-04	6.436e-04	5.001e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0007	0.0007	0.0007

RN	0.0011	0.0008	0.0009	0.0009
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0625	0.0542	2.9131	1.6367
CP to QN ↑	0.0802	0.0450	4.3639	2.5184
CP to TQ ↓	0.0557	0.0300	3.7365	3.0627
CP to TQ ↑	0.0519	0.0427	7.3712	6.8449
RN to QN ↑	0.0576	0.0629	4.4265	2.5208
RN to TQ ↓	0.0428	0.0498	3.2809	2.9880
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0563	0.0615	0.8127	0.4274
CP to QN ↑	0.0458	0.0487	1.2615	0.6361
CP to TQ ↓	0.0313	0.0323	3.7868	3.7156
CP to TQ ↑	0.0426	0.0437	6.4496	6.5519
RN to QN ↑	0.0634	0.0655	1.2619	0.6364
RN to TQ ↓	0.0508	0.0513	3.7099	3.6288

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0818	0.0789	0.0818	0.0818
CP ↑	min_pulse_width to CP	0.0531	0.0242	0.0242	0.0253
D ↓	hold_rising to CP	-0.0481	-0.0117	-0.0117	-0.0117
D ↑	hold_rising to CP	-0.0212	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0796	0.0512	0.0512	0.0512
D ↑	setup_rising to CP	0.0512	0.0270	0.0295	0.0295
RN ↓	min_pulse_width to RN	0.0588	0.0588	0.0588	0.0637
RN ↑	recovery_rising to CP	0.0145	0.0124	0.0124	0.0124
RN ↑	removal_rising to CP	-0.0100	-0.0052	-0.0052	-0.0052
TE ↓	hold_rising to CP	-0.0335	-0.0095	-0.0095	-0.0095
TE ↑	hold_rising to CP	-0.0309	-0.0168	-0.0193	-0.0193
TE ↓	setup_rising to CP	0.0681	0.0512	0.0512	0.0512
TE ↑	setup_rising to CP	0.1194	0.0957	0.0957	0.0957
TI ↓	hold_rising to CP	-0.0931	-0.0478	-0.0478	-0.0478
TI ↑	hold_rising to CP	-0.0359	-0.0202	-0.0200	-0.0200
TI ↓	setup_rising to CP	0.1278	0.0924	0.0924	0.0924
TI ↑	setup_rising to CP	0.0617	0.0443	0.0443	0.0443

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	8.993e-05	5.451e-09
X8_P4	9.699e-05	5.120e-09
X17_P4	1.149e-04	5.451e-09
X33_P4	1.441e-04	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

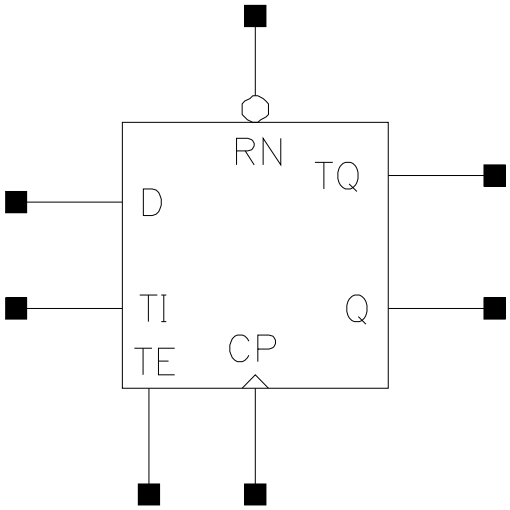
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.791e-03	5.834e-03	5.875e-03	5.897e-03
Clock 100Mhz Data 25Mhz	9.196e-03	9.059e-03	9.643e-03	1.100e-02
Clock 100Mhz Data 50Mhz	1.260e-02	1.228e-02	1.341e-02	1.611e-02
Clock = 0 Data 100Mhz	7.098e-03	6.491e-03	6.286e-03	6.185e-03
Clock = 1 Data 100Mhz	1.792e-03	9.305e-04	6.434e-04	4.999e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0007	0.0007	0.0007

RN	0.0009	0.0009	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0676	0.0360	3.7326	1.6917
CP to Q ↑	0.0538	0.0445	5.1788	2.5936
CP to TQ ↓	0.0633	0.0357	4.6541	4.0160
CP to TQ ↑	0.0557	0.0466	9.7868	8.9382
RN to Q ↓	0.0470	0.0539	3.2839	1.6413
RN to TQ ↓	0.0447	0.0537	4.1494	3.9169
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0512	0.0566	0.8053	0.4235
CP to Q ↑	0.0629	0.0672	1.2317	0.6284
CP to TQ ↓	0.0530	0.0595	3.8186	3.8952
CP to TQ ↑	0.0666	0.0732	8.7652	8.8072
RN to Q ↓	0.0634	0.0688	0.8050	0.4235
RN to TQ ↓	0.0651	0.0717	3.8205	3.8952

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0818	0.0789	0.0789	0.0789
CP ↑	min_pulse_width to CP	0.0590	0.0290	0.0242	0.0242
D ↓	hold_rising to CP	-0.0481	-0.0117	-0.0117	-0.0117
D ↑	hold_rising to CP	-0.0212	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0796	0.0512	0.0512	0.0512
D ↑	setup_rising to CP	0.0512	0.0270	0.0270	0.0270
RN ↓	min_pulse_width to RN	0.0588	0.0686	0.0544	0.0544
RN ↑	recovery_rising to CP	0.0149	0.0149	0.0127	0.0127
RN ↑	removal_rising to CP	-0.0076	-0.0048	-0.0052	-0.0052
TE ↓	hold_rising to CP	-0.0335	-0.0064	-0.0095	-0.0095
TE ↑	hold_rising to CP	-0.0312	-0.0168	-0.0168	-0.0168
TE ↓	setup_rising to CP	0.0681	0.0512	0.0512	0.0512
TE ↑	setup_rising to CP	0.1194	0.0957	0.0957	0.0957
TI ↓	hold_rising to CP	-0.0931	-0.0480	-0.0519	-0.0519
TI ↑	hold_rising to CP	-0.0318	-0.0202	-0.0200	-0.0200
TI ↓	setup_rising to CP	0.1278	0.0924	0.0924	0.0924
TI ↑	setup_rising to CP	0.0617	0.0443	0.0443	0.0443

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	8.374e-05	5.451e-09
X8_P4	9.022e-05	5.120e-09
X17_P4	1.160e-04	5.451e-09
X33_P4	1.354e-04	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

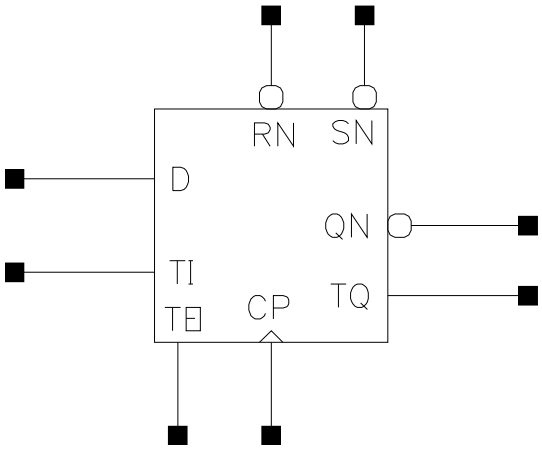
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.826e-03	5.853e-03	5.861e-03	5.865e-03
Clock 100Mhz Data 25Mhz	9.376e-03	9.107e-03	1.006e-02	1.127e-02
Clock 100Mhz Data 50Mhz	1.292e-02	1.236e-02	1.427e-02	1.667e-02
Clock = 0 Data 100Mhz	7.103e-03	6.495e-03	6.292e-03	6.191e-03
Clock = 1 Data 100Mhz	1.794e-03	9.315e-04	6.441e-04	5.006e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.352	5.2224
X17_P4	1.200	4.488	5.3856
X33_P4	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0009

SN	0.0014	0.0014	0.0014
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
CP to QN ↓	0.0602	0.0643	1.5847	0.8160
CP to QN ↑	0.0463	0.0489	2.4398	1.2350
CP to TQ ↓	0.0347	0.0347	4.6882	4.6921
CP to TQ ↑	0.0498	0.0498	11.2218	11.2391
RN to QN ↓	0.0550	0.0599	1.5922	0.8180
RN to QN ↑	0.0546	0.0568	2.4363	1.2349
RN to TQ ↓	0.0442	0.0442	4.6188	4.6204
RN to TQ ↑	0.0436	0.0435	11.3356	11.3463
SN to QN ↓	0.0615	0.0655	1.5854	0.8166
SN to TQ ↑	0.0513	0.0514	11.2115	11.2240
	X33_P4		X33_P4	
CP to QN ↓	0.0741		0.4325	
CP to QN ↑	0.0550		0.6326	
CP to TQ ↓	0.0348		4.7009	
CP to TQ ↑	0.0499		11.2577	
RN to QN ↓	0.0708		0.4325	
RN to QN ↑	0.0624		0.6322	
RN to TQ ↓	0.0443		4.6269	
RN to TQ ↑	0.0436		11.3856	
SN to QN ↓	0.0752		0.4329	
SN to TQ ↑	0.0515		11.2497	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0842	0.0842	0.0842
CP ↑	min_pulse_width to CP	0.0253	0.0253	0.0290
D ↓	hold_rising to CP	-0.0117	-0.0117	-0.0117
D ↑	hold_rising to CP	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0561	0.0561	0.0561
D ↑	setup_rising to CP	0.0295	0.0295	0.0295
RN ↓	min_pulse_width to RN	0.0637	0.0659	0.0708
RN ↑	non_seq_hold_rising to SN	-0.0237	-0.0237	-0.0237
RN ↑	non_seq_setup_rising to SN	0.0571	0.0571	0.0571
RN ↑	recovery_rising to CP	0.0216	0.0216	0.0216
RN ↑	removal_rising to CP	-0.0149	-0.0149	-0.0149
SN ↓	min_pulse_width to SN	0.0544	0.0571	0.0598
SN ↑	recovery_rising to CP	0.0029	0.0029	0.0029
SN ↑	removal_rising to CP	0.0287	0.0287	0.0287

TE ↓	hold_rising to CP	-0.0095	-0.0095	-0.0095
TE ↑	hold_rising to CP	-0.0168	-0.0168	-0.0168
TE ↓	setup_rising to CP	0.0539	0.0536	0.0536
TE ↑	setup_rising to CP	0.1006	0.1006	0.1006
TI ↓	hold_rising to CP	-0.0534	-0.0534	-0.0534
TI ↑	hold_rising to CP	-0.0202	-0.0202	-0.0202
TI ↓	setup_rising to CP	0.1013	0.1013	0.1013
TI ↑	setup_rising to CP	0.0499	0.0499	0.0499

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	1.067e-04	5.800e-09
X17_P4	1.209e-04	5.966e-09
X33_P4	1.457e-04	6.297e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

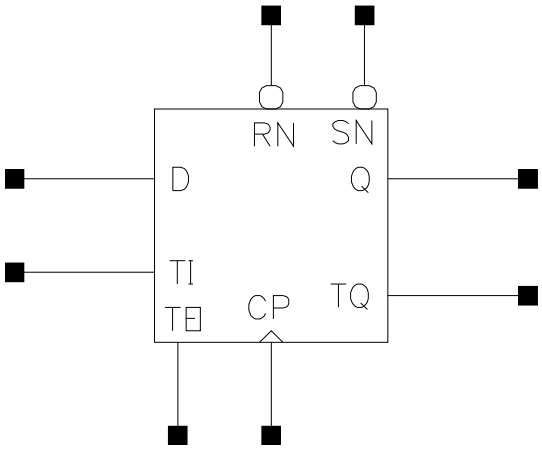
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	6.170e-03	6.171e-03	6.172e-03
Clock 100Mhz Data 25Mhz	9.419e-03	9.979e-03	1.153e-02
Clock 100Mhz Data 50Mhz	1.267e-02	1.379e-02	1.689e-02
Clock = 0 Data 100Mhz	6.077e-03	6.075e-03	6.076e-03
Clock = 1 Data 100Mhz	6.981e-05	6.986e-05	6.997e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.216	5.0592
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010
D	0.0006	0.0006	0.0006
RN	0.0010	0.0009	0.0009

SN	0.0014	0.0014	0.0014
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
CP to Q ↓	0.0390	0.0441	1.6454	0.8528
CP to Q ↑	0.0491	0.0523	2.4971	1.2712
CP to TQ ↓	0.0393	0.0444	4.7780	4.8525
CP to TQ ↑	0.0536	0.0592	11.0921	11.1757
RN to Q ↓	0.0466	0.0496	1.5942	0.8223
RN to Q ↑	0.0518	0.0541	2.4840	1.2624
RN to TQ ↓	0.0470	0.0501	4.6779	4.7230
RN to TQ ↑	0.0559	0.0602	11.0436	11.1148
SN to Q ↑	0.0503	0.0529	2.4858	1.2623
SN to TQ ↑	0.0543	0.0588	11.0585	11.1314
	X33_P4		X33_P4	
CP to Q ↓	0.0566		0.4576	
CP to Q ↑	0.0606		0.6580	
CP to TQ ↓	0.0537		5.0525	
CP to TQ ↑	0.0696		11.3140	
RN to Q ↓	0.0574		0.4370	
RN to Q ↑	0.0604		0.6504	
RN to TQ ↓	0.0557		4.8578	
RN to TQ ↑	0.0680		11.2333	
SN to Q ↑	0.0595		0.6507	
SN to TQ ↑	0.0669		11.2533	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0842	0.0842	0.0842
CP ↑	min_pulse_width to CP	0.0290	0.0349	0.0483
D ↓	hold_rising to CP	-0.0117	-0.0117	-0.0117
D ↑	hold_rising to CP	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0561	0.0561	0.0561
D ↑	setup_rising to CP	0.0295	0.0295	0.0295
RN ↓	min_pulse_width to RN	0.0735	0.0854	0.1099
RN ↑	non_seq_hold_rising to SN	-0.0235	-0.0335	-0.0432
RN ↑	non_seq_setup_rising to SN	0.0523	0.0523	0.0676
RN ↑	recovery_rising to CP	0.0197	0.0197	0.0197
RN ↑	removal_rising to CP	-0.0100	-0.0100	-0.0100
SN ↓	min_pulse_width to SN	0.0598	0.0696	0.0842
SN ↑	recovery_rising to CP	0.0029	0.0029	0.0029
SN ↑	removal_rising to CP	0.0287	0.0287	0.0287

TE ↓	hold_rising to CP	-0.0095	-0.0095	-0.0095
TE ↑	hold_rising to CP	-0.0168	-0.0168	-0.0137
TE ↓	setup_rising to CP	0.0509	0.0536	0.0536
TE ↑	setup_rising to CP	0.1006	0.1006	0.1006
TI ↓	hold_rising to CP	-0.0519	-0.0519	-0.0519
TI ↑	hold_rising to CP	-0.0202	-0.0187	-0.0146
TI ↓	setup_rising to CP	0.0972	0.1013	0.1013
TI ↑	setup_rising to CP	0.0499	0.0499	0.0499

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P4	1.024e-04	5.628e-09
X17_P4	1.142e-04	5.794e-09
X33_P4	1.353e-04	6.125e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

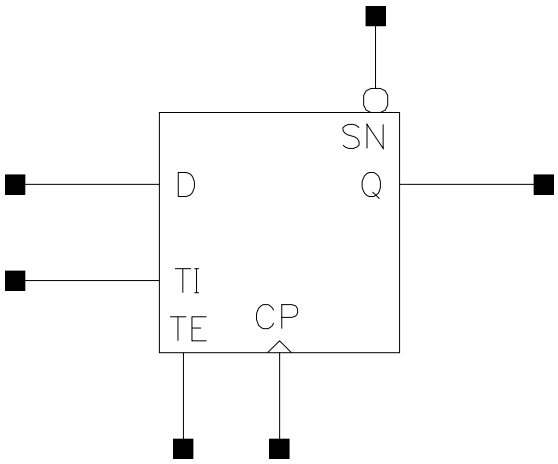
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	6.162e-03	6.163e-03	6.164e-03
Clock 100Mhz Data 25Mhz	9.397e-03	1.020e-02	1.243e-02
Clock 100Mhz Data 50Mhz	1.263e-02	1.424e-02	1.870e-02
Clock = 0 Data 100Mhz	6.074e-03	6.075e-03	6.074e-03
Clock = 1 Data 100Mhz	6.954e-05	6.976e-05	6.986e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005
SN	0.0015	0.0015	0.0015	0.0015
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0010			
D	0.0005			
SN	0.0015			
TE	0.0011			
TI	0.0004			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.0596	0.0341	3.5323	1.6355
CP to Q ↑	0.0524	0.0447	5.0091	2.4860
SN to Q ↑	0.0366	0.0385	4.8851	2.4638
	X17_P4	X25_P4	X17_P4	X25_P4
CP to Q ↓	0.0488	0.0514	0.7953	0.5503
CP to Q ↑	0.0628	0.0650	1.2262	0.8310
SN to Q ↑	0.0571	0.0593	1.2257	0.8322
	X33_P4		X33_P4	
CP to Q ↓	0.0538		0.4184	
CP to Q ↑	0.0667		0.6261	
SN to Q ↑	0.0611		0.6252	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.0847	0.0847	0.0847	0.0847
CP ↑	min_pulse_width to CP	0.0531	0.0242	0.0205	0.0205
D ↓	hold_rising to CP	-0.0478	-0.0166	-0.0166	-0.0166
D ↑	hold_rising to CP	-0.0184	0.0027	0.0027	0.0027
D ↓	setup_rising to CP	0.0823	0.0561	0.0561	0.0561
D ↑	setup_rising to CP	0.0463	0.0242	0.0242	0.0242
SN ↓	min_pulse_width to SN	0.0403	0.0474	0.0425	0.0425
SN ↑	recovery_rising to CP	0.0029	0.0029	0.0029	0.0029
SN ↑	removal_rising to CP	0.0187	0.0263	0.0267	0.0267
TE ↓	hold_rising to CP	-0.0331	-0.0117	-0.0117	-0.0117
TE ↑	hold_rising to CP	-0.0261	-0.0144	-0.0144	-0.0144
TE ↓	setup_rising to CP	0.0674	0.0539	0.0539	0.0539
TE ↑	setup_rising to CP	0.1246	0.1054	0.1054	0.1054
TI ↓	hold_rising to CP	-0.0985	-0.0583	-0.0583	-0.0583
TI ↑	hold_rising to CP	-0.0310	-0.0152	-0.0152	-0.0152
TI ↓	setup_rising to CP	0.1327	0.1026	0.1026	0.1026
TI ↑	setup_rising to CP	0.0609	0.0394	0.0394	0.0394
		X33_P4			

CP ↓	min_pulse_width to CP	0.0847			
CP ↑	min_pulse_width to CP	0.0205			
D ↓	hold_rising to CP	-0.0166			
D ↑	hold_rising to CP	0.0027			
D ↓	setup_rising to CP	0.0561			
D ↑	setup_rising to CP	0.0242			
SN ↓	min_pulse_width to SN	0.0425			
SN ↑	recovery_rising to CP	0.0029			
SN ↑	removal_rising to CP	0.0263			
TE ↓	hold_rising to CP	-0.0117			
TE ↑	hold_rising to CP	-0.0144			
TE ↓	setup_rising to CP	0.0539			
TE ↑	setup_rising to CP	0.1054			
TI ↓	hold_rising to CP	-0.0583			
TI ↑	hold_rising to CP	-0.0152			
TI ↓	setup_rising to CP	0.1026			
TI ↑	setup_rising to CP	0.0394			

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	8.510e-05	5.286e-09
X8_P4	9.310e-05	5.120e-09
X17_P4	1.181e-04	5.451e-09
X25_P4	1.310e-04	5.617e-09
X33_P4	1.437e-04	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	5.688e-03	5.808e-03	5.848e-03	5.868e-03
Clock 100Mhz Data 25Mhz	8.881e-03	8.903e-03	9.824e-03	1.038e-02
Clock 100Mhz Data 50Mhz	1.207e-02	1.200e-02	1.380e-02	1.490e-02
Clock = 0 Data 100Mhz	6.819e-03	6.379e-03	6.233e-03	6.159e-03
Clock = 1 Data 100Mhz	1.794e-03	9.313e-04	6.440e-04	5.004e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	5.880e-03			

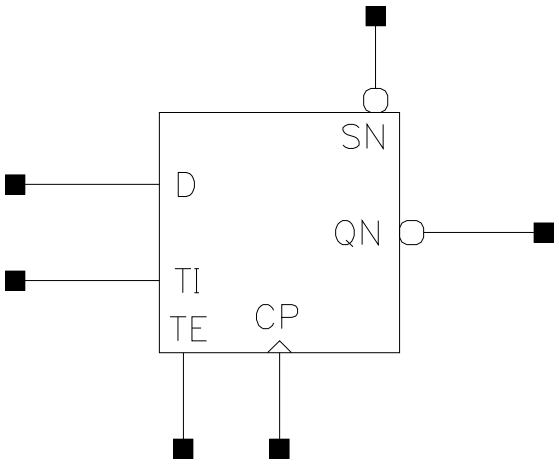
Clock 100Mhz Data 25Mhz	1.096e-02			
Clock 100Mhz Data 50Mhz	1.603e-02			
Clock = 0 Data 100Mhz	6.115e-03			
Clock = 1 Data 100Mhz	4.142e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005
SN	0.0015	0.0015	0.0015	0.0015
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0010			
D	0.0005			
SN	0.0015			
TE	0.0011			
TI	0.0004			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.0583	0.0527	2.9065	1.5558
CP to QN ↑	0.0615	0.0397	4.8458	2.4327
SN to QN ↓	0.0441	0.0470	2.9000	1.5570
	X17_P4	X25_P4	X17_P4	X25_P4
CP to QN ↓	0.0556	0.0587	0.7977	0.5521
CP to QN ↑	0.0468	0.0497	1.2274	0.8324
SN to QN ↓	0.0485	0.0515	0.7976	0.5516
	X33_P4		X33_P4	
CP to QN ↓	0.0614		0.4192	
CP to QN ↑	0.0519		0.6267	
SN to QN ↓	0.0539		0.4186	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.0847	0.0847	0.0866	0.0866
CP ↑	min_pulse_width to CP	0.0386	0.0205	0.0253	0.0290
D ↓	hold_rising to CP	-0.0474	-0.0166	-0.0166	-0.0166
D ↑	hold_rising to CP	-0.0184	0.0027	0.0027	0.0027
D ↓	setup_rising to CP	0.0823	0.0561	0.0561	0.0561
D ↑	setup_rising to CP	0.0463	0.0242	0.0242	0.0242
SN ↓	min_pulse_width to SN	0.0376	0.0425	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0029	0.0029	0.0029	0.0029
SN ↑	removal_rising to CP	0.0187	0.0263	0.0267	0.0263
TE ↓	hold_rising to CP	-0.0331	-0.0117	-0.0117	-0.0117
TE ↑	hold_rising to CP	-0.0261	-0.0144	-0.0144	-0.0144
TE ↓	setup_rising to CP	0.0674	0.0539	0.0539	0.0539
TE ↑	setup_rising to CP	0.1246	0.1054	0.1054	0.1054
TI ↓	hold_rising to CP	-0.0985	-0.0583	-0.0583	-0.0583
TI ↑	hold_rising to CP	-0.0310	-0.0152	-0.0152	-0.0152
TI ↓	setup_rising to CP	0.1327	0.1026	0.1026	0.1026
TI ↑	setup_rising to CP	0.0609	0.0394	0.0394	0.0394
		X33_P4			

CP ↓	min_pulse_width to CP	0.0866			
CP ↑	min_pulse_width to CP	0.0290			
D ↓	hold_rising to CP	-0.0166			
D ↑	hold_rising to CP	0.0027			
D ↓	setup_rising to CP	0.0561			
D ↑	setup_rising to CP	0.0242			
SN ↓	min_pulse_width to SN	0.0474			
SN ↑	recovery_rising to CP	0.0029			
SN ↑	removal_rising to CP	0.0263			
TE ↓	hold_rising to CP	-0.0117			
TE ↑	hold_rising to CP	-0.0144			
TE ↓	setup_rising to CP	0.0537			
TE ↑	setup_rising to CP	0.1054			
TI ↓	hold_rising to CP	-0.0583			
TI ↑	hold_rising to CP	-0.0152			
TI ↓	setup_rising to CP	0.1026			
TI ↑	setup_rising to CP	0.0394			

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	8.173e-05	5.286e-09
X8_P4	8.768e-05	5.120e-09
X17_P4	1.138e-04	5.451e-09
X25_P4	1.234e-04	5.617e-09
X33_P4	1.331e-04	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	5.686e-03	5.816e-03	5.854e-03	5.873e-03
Clock 100Mhz Data 25Mhz	8.594e-03	8.776e-03	9.944e-03	1.053e-02
Clock 100Mhz Data 50Mhz	1.150e-02	1.174e-02	1.403e-02	1.519e-02
Clock = 0 Data 100Mhz	6.819e-03	6.383e-03	6.236e-03	6.161e-03
Clock = 1 Data 100Mhz	1.793e-03	9.312e-04	6.439e-04	5.002e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	5.885e-03			

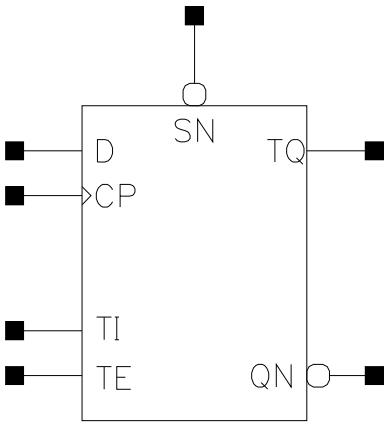
Clock 100Mhz Data 25Mhz	1.111e-02			
Clock 100Mhz Data 50Mhz	1.633e-02			
Clock = 0 Data 100Mhz	6.117e-03			
Clock = 1 Data 100Mhz	4.141e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.216	5.0592
X8_P4	1.200	4.080	4.8960
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005

SN	0.0016	0.0017	0.0016	0.0016
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0667	0.0550	2.9058	1.5664
CP to QN ↑	0.0794	0.0449	4.7908	2.4830
CP to TQ ↓	0.0571	0.0302	4.1814	3.5318
CP to TQ ↑	0.0520	0.0417	6.5718	6.4182
SN to QN ↓	0.0465	0.0482	2.8980	1.5647
SN to TQ ↑	0.0333	0.0345	6.4725	6.4313
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0555	0.0616	0.8184	0.4156
CP to QN ↑	0.0503	0.0560	1.2390	0.6314
CP to TQ ↓	0.0374	0.0373	3.6770	3.6791
CP to TQ ↑	0.0468	0.0469	6.4633	6.4773
SN to QN ↓	0.0498	0.0555	0.8176	0.4153
SN to TQ ↑	0.0355	0.0408	6.4027	6.4658

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0847	0.0847	0.0866	0.0866
CP ↑	min_pulse_width to CP	0.0531	0.0242	0.0290	0.0301
D ↓	hold_rising to CP	-0.0478	-0.0166	-0.0166	-0.0166
D ↑	hold_rising to CP	-0.0184	0.0027	0.0027	0.0027
D ↓	setup_rising to CP	0.0823	0.0561	0.0561	0.0561
D ↑	setup_rising to CP	0.0463	0.0242	0.0242	0.0242
SN ↓	min_pulse_width to SN	0.0354	0.0376	0.0403	0.0403
SN ↑	recovery_rising to CP	0.0029	0.0029	0.0029	0.0029
SN ↑	removal_rising to CP	0.0187	0.0263	0.0263	0.0263
TE ↓	hold_rising to CP	-0.0331	-0.0117	-0.0117	-0.0117
TE ↑	hold_rising to CP	-0.0261	-0.0144	-0.0144	-0.0144
TE ↓	setup_rising to CP	0.0674	0.0539	0.0537	0.0537
TE ↑	setup_rising to CP	0.1246	0.1054	0.1054	0.1054
TI ↓	hold_rising to CP	-0.0985	-0.0583	-0.0583	-0.0583
TI ↑	hold_rising to CP	-0.0310	-0.0152	-0.0152	-0.0152
TI ↓	setup_rising to CP	0.1327	0.1026	0.1026	0.1026
TI ↑	setup_rising to CP	0.0609	0.0394	0.0394	0.0394

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	9.183e-05	5.617e-09
X8_P4	9.771e-05	5.451e-09
X17_P4	1.239e-04	5.782e-09
X33_P4	1.432e-04	6.114e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

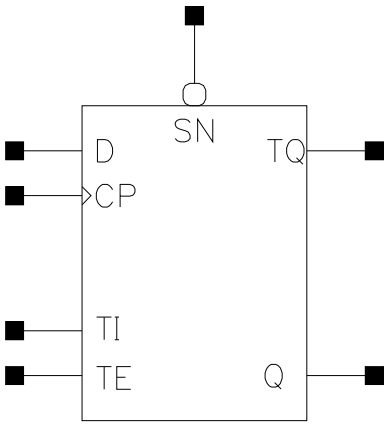
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.691e-03	5.815e-03	5.857e-03	5.878e-03
Clock 100Mhz Data 25Mhz	9.154e-03	9.117e-03	1.022e-02	1.141e-02
Clock 100Mhz Data 50Mhz	1.262e-02	1.242e-02	1.459e-02	1.695e-02
Clock = 0 Data 100Mhz	6.832e-03	6.392e-03	6.245e-03	6.171e-03
Clock = 1 Data 100Mhz	1.794e-03	9.316e-04	6.442e-04	5.006e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.944	4.7328
X17_P4	1.200	4.216	5.0592
X33_P4	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005

SN	0.0016	0.0015	0.0015	0.0014
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0685	0.0368	3.6264	1.6701
CP to Q ↑	0.0559	0.0467	5.0392	2.5183
CP to TQ ↓	0.0688	0.0376	5.1534	4.0396
CP to TQ ↑	0.0549	0.0510	6.6161	9.0279
SN to Q ↑	0.0357	0.0398	4.9139	2.4906
SN to TQ ↑	0.0348	0.0433	6.4938	8.9862
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0499	0.0550	0.8162	0.4256
CP to Q ↑	0.0637	0.0677	1.2329	0.6290
CP to TQ ↓	0.0517	0.0581	3.8173	3.8875
CP to TQ ↑	0.0676	0.0738	8.7678	8.8209
SN to Q ↑	0.0581	0.0621	1.2325	0.6279
SN to TQ ↑	0.0619	0.0681	8.7702	8.8127

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0847	0.0847	0.0847	0.0847
CP ↑	min_pulse_width to CP	0.0627	0.0290	0.0205	0.0223
D ↓	hold_rising to CP	-0.0478	-0.0166	-0.0166	-0.0166
D ↑	hold_rising to CP	-0.0184	0.0027	0.0027	0.0027
D ↓	setup_rising to CP	0.0823	0.0561	0.0561	0.0561
D ↑	setup_rising to CP	0.0463	0.0242	0.0242	0.0242
SN ↓	min_pulse_width to SN	0.0354	0.0474	0.0425	0.0425
SN ↑	recovery_rising to CP	0.0029	0.0029	0.0029	0.0029
SN ↑	removal_rising to CP	0.0187	0.0263	0.0263	0.0267
TE ↓	hold_rising to CP	-0.0331	-0.0117	-0.0117	-0.0117
TE ↑	hold_rising to CP	-0.0261	-0.0144	-0.0144	-0.0144
TE ↓	setup_rising to CP	0.0674	0.0539	0.0539	0.0539
TE ↑	setup_rising to CP	0.1246	0.1054	0.1054	0.1054
TI ↓	hold_rising to CP	-0.0985	-0.0583	-0.0583	-0.0583
TI ↑	hold_rising to CP	-0.0310	-0.0152	-0.0152	-0.0152
TI ↓	setup_rising to CP	0.1327	0.1026	0.1026	0.1026
TI ↑	setup_rising to CP	0.0609	0.0394	0.0394	0.0394

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	9.200e-05	5.451e-09
X8_P4	9.863e-05	5.286e-09
X17_P4	1.237e-04	5.617e-09
X33_P4	1.492e-04	5.948e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

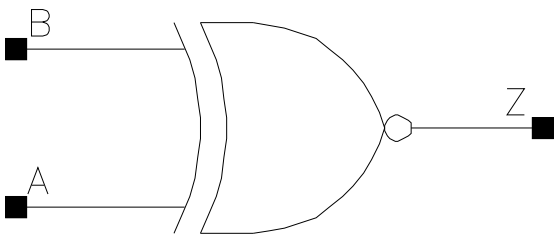
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	5.689e-03	5.810e-03	5.849e-03	5.869e-03
Clock 100Mhz Data 25Mhz	9.318e-03	9.211e-03	1.008e-02	1.129e-02
Clock 100Mhz Data 50Mhz	1.295e-02	1.261e-02	1.431e-02	1.671e-02
Clock = 0 Data 100Mhz	6.833e-03	6.385e-03	6.237e-03	6.162e-03
Clock = 1 Data 100Mhz	1.794e-03	9.316e-04	6.442e-04	5.006e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P4	X8_P4	X17_P4	X25_P4
A	0.0017	0.0007	0.0010	0.0016
B	0.0016	0.0015	0.0019	0.0026
	X33_P4			
A	0.0018			
B	0.0030			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X8_P4**	**X6_P4**	**X8_P4**
A to Z ↓	0.0165	0.0360	2.7359	1.6922
A to Z ↑	0.0174	0.0339	3.8050	2.5662
B to Z ↓	0.0154	0.0253	2.7351	1.6750
B to Z ↑	0.0182	0.0244	3.8138	2.5571
	X17_P4	**X25_P4**	**X17_P4**	**X25_P4**
A to Z ↓	0.0347	0.0351	0.8313	0.5710
A to Z ↑	0.0317	0.0317	1.2587	0.8386

B to Z ↓	0.0262	0.0253	0.8276	0.5686
B to Z ↑	0.0249	0.0239	1.2551	0.8369
	X33_P4		**X33_P4**	
A to Z ↓	0.0335		0.4279	
A to Z ↑	0.0310		0.6305	
B to Z ↓	0.0245		0.4266	
B to Z ↑	0.0239		0.6294	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P4	3.660e-05	1.642e-09
X8_P4	5.520e-05	2.139e-09
X17_P4	8.223e-05	2.304e-09
X25_P4	1.321e-04	3.298e-09
X33_P4	1.676e-04	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	3.670e-03	6.903e-03	1.034e-02	1.630e-02
B to Z	3.590e-03	4.988e-03	8.180e-03	1.258e-02
	X33_P4			
A to Z	2.011e-02			
B to Z	1.602e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

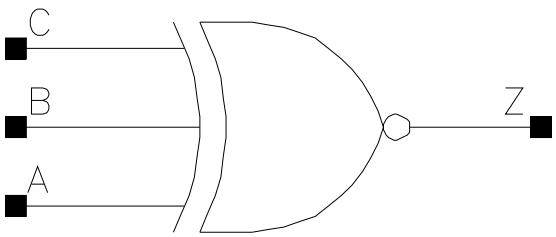
Pin Cycle (vdds)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	1.263e-06	2.233e-07	8.516e-07	-1.983e-07
B to Z	3.244e-07	1.002e-06	1.180e-06	9.046e-07
	X33_P4			
A to Z	8.035e-07			
B to Z	4.118e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	2.176	2.6112
X16_P4	1.200	2.720	3.2640
X25_P4	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X16_P4	X25_P4
A	0.0030	0.0025	0.0031	0.0046
B	0.0033	0.0023	0.0030	0.0042
C	0.0021	0.0007	0.0007	0.0008

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0255	0.0426	3.2136	1.7773
A to Z ↑	0.0252	0.0393	5.4193	2.5414
B to Z ↓	0.0263	0.0430	3.2190	1.7775
B to Z ↑	0.0255	0.0398	5.4191	2.5409
C to Z ↓	0.0261	0.0570	3.2257	1.7772
C to Z ↑	0.0248	0.0534	5.4220	2.5406
	X16_P4	**X25_P4**	**X16_P4**	**X25_P4**
A to Z ↓	0.0433	0.0438	0.9111	0.5837
A to Z ↑	0.0427	0.0431	1.3291	0.8405
B to Z ↓	0.0439	0.0449	0.9115	0.5836

B to Z ↑	0.0433	0.0443	1.3296	0.8408
C to Z ↓	0.0608	0.0654	0.9107	0.5833
C to Z ↑	0.0597	0.0645	1.3295	0.8410

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	3.986e-05	2.967e-09
X8_P4	4.690e-05	3.132e-09
X16_P4	7.407e-05	3.795e-09
X25_P4	1.044e-04	5.286e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	3.832e-03	5.423e-03	9.112e-03	1.401e-02
B to Z	3.815e-03	5.365e-03	9.092e-03	1.406e-02
C to Z	3.722e-03	8.036e-03	1.226e-02	1.870e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

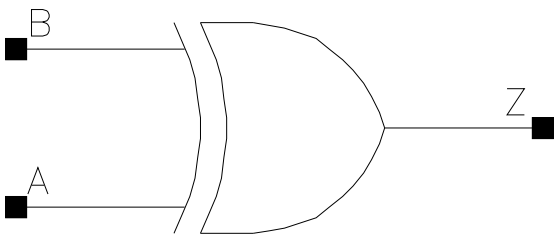
Pin Cycle (vdds)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	5.561e-07	7.874e-08	7.216e-08	-9.698e-08
B to Z	1.386e-05	5.275e-06	6.981e-06	1.139e-05
C to Z	2.620e-05	1.256e-05	1.555e-05	2.203e-05

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.224	1.4688
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.224	1.4688
X16_P4	1.200	1.360	1.6320
X25_P4	1.200	2.176	2.6112
X31_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X16_P4
A	0.0008	0.0016	0.0011	0.0012
B	0.0013	0.0015	0.0015	0.0017
	X25_P4	X31_P4		
A	0.0016	0.0020		
B	0.0027	0.0035		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0326	0.0161	2.9676	2.1573
A to Z ↑	0.0317	0.0186	4.7474	4.8062
B to Z ↓	0.0239	0.0169	2.9442	2.1760
B to Z ↑	0.0239	0.0173	4.7411	4.8036
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0294	0.0311	1.6541	0.8536

A to Z ↑	0.0278	0.0295	2.5012	1.2600
B to Z ↓	0.0231	0.0242	1.6437	0.8495
B to Z ↑	0.0222	0.0238	2.4971	1.2589
	X25_P4	**X31_P4**	**X25_P4**	**X31_P4**
A to Z ↓	0.0331	0.0314	0.5670	0.4530
A to Z ↑	0.0312	0.0299	0.8371	0.6731
B to Z ↓	0.0249	0.0235	0.5666	0.4527
B to Z ↑	0.0238	0.0229	0.8369	0.6727

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	4.668e-05	1.973e-09
X6_P4	3.921e-05	1.642e-09
X8_P4	6.624e-05	1.973e-09
X16_P4	9.013e-05	2.139e-09
X25_P4	1.289e-04	3.132e-09
X31_P4	1.640e-04	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	5.162e-03	3.645e-03	6.421e-03	9.615e-03
B to Z	4.084e-03	3.496e-03	5.414e-03	8.178e-03
	X25_P4	X31_P4		
A to Z	1.529e-02	1.881e-02		
B to Z	1.176e-02	1.450e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

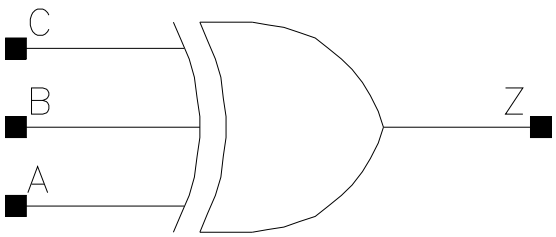
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	2.199e-07	9.430e-07	7.838e-07	5.069e-07
B to Z	5.573e-07	3.122e-06	1.504e-06	1.652e-06
	X25_P4	X31_P4		
A to Z	5.833e-07	1.671e-06		
B to Z	-9.350e-08	-3.080e-07		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X24_P4	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X24_P4
A	0.0026	0.0025	0.0031	0.0055
B	0.0026	0.0023	0.0029	0.0046
C	0.0008	0.0017	0.0023	0.0035

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0259	0.0426	3.3899	1.7761
A to Z ↑	0.0254	0.0392	5.9144	2.5382
B to Z ↓	0.0264	0.0430	3.3943	1.7776
B to Z ↑	0.0257	0.0398	5.9121	2.5383
C to Z ↓	0.0453	0.0422	3.3714	1.7768
C to Z ↑	0.0447	0.0389	5.8872	2.5383
	X17_P4	**X24_P4**	**X17_P4**	**X24_P4**
A to Z ↓	0.0399	0.0462	0.8495	0.6120
A to Z ↑	0.0393	0.0356	1.2396	0.8435
B to Z ↓	0.0402	0.0467	0.8492	0.6120

B to Z ↑	0.0398	0.0359	1.2410	0.8443
C to Z ↓	0.0399	0.0455	0.8497	0.6119
C to Z ↑	0.0395	0.0358	1.2409	0.8441

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P4	4.679e-05	2.967e-09
X8_P4	3.854e-05	2.801e-09
X17_P4	6.445e-05	2.967e-09
X24_P4	1.121e-04	5.120e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	3.634e-03	5.420e-03	8.793e-03	1.476e-02
B to Z	3.655e-03	5.360e-03	8.750e-03	1.464e-02
C to Z	7.180e-03	5.250e-03	8.694e-03	1.445e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	4.262e-07	6.050e-08	1.675e-08	1.598e-07
B to Z	7.571e-06	5.382e-06	7.389e-06	1.559e-05
C to Z	1.873e-05	1.466e-05	1.806e-05	4.442e-05

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