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Technology	cmos028fdsoi
Design rule manual	0.4.8
Design Kit	1.2
Previous Design Kit	1.1
AMS Version	2018.3
Maturity DMS reference	8356769-core/DM00388089-RF

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File name	Description
28FDSOI_Model_Reference_Guide.pdf	General description of models and usage
28FD_MOS_mismatch_model_doc.pdf	mismatch usage documentation in DK environnement
CMOM_with_and_wo_via.pdf	CMOM model description
EGLVTPS_Analog_Report.pdf	EG LVT PowerSwitch Comparison to previous DK - focus on analog performance
EGLVTPS_Standard_Report.pdf	EG LVT PowerSwitch Comparison to previous DK
EGLVTV_Analog_Report.pdf	EGV LVT Comparison to previous DK - focus on analog performance
EGLVTV_Standard_Report.pdf	EGV LVT Comparison to previous DK
EGLVT_Analog_Report.pdf	EG LVT Comparison to previous DK - focus on analog performance
EGLVT_RF_Report.pdf	EGLVT RF compared to EGLVTRF and EGLVT RFSEG
EGLVT_Standard_Report.pdf	EG LVT Comparison to previous DK
EGRVTV_Analog_Report.pdf	EGV RVT Comparison to previous DK - focus on analog performance
EGRVTV_Standard_Report.pdf	EGV RVT Comparison to previous DK
EGRVT_Analog_Report.pdf	EG RVT Comparison to previous DK - focus on analog performance
EGRVT_Standard_Report.pdf	EG RVT Comparison to previous DK
EG_LVT_vs_RVT_Analog_Report.pdf	EG LVT compared to EG RVT - focus on analog performance
EG_LVT_vs_RVT_Standard_Report.pdf	EG LVT compared to EG RVT
EG_Mismatch_Report.pdf	EG LVT and EG RVT Comparison to previous DK - focus on mismatch
EG_cpoly.pdf	EG_cpoly
ESD_Diodes.pdf	ESD_Diodes model description
ESD_NMOS.pdf	ESD_NMOS model description
LLE_LOD_EG.pdf	LOD bench report for EG
LLE_LOD_SG.pdf	LOD bench report for SG
LLE_PCPASTRX_SG.pdf	PCPASTRX bench report for SG
LLE_WPE_EG.pdf	WPE bench report for EG
LLE_WPE_SG.pdf	WPE bench report for SG
LVT_Analog_Report.pdf	SG LVT Comparison to previous DK - focus on analog performance
LVT_Biasing_Report.pdf	SG LVT Comparison to previous DK - focus on Vdd/Vbs variations
LVT_RO.pdf	SG LVT Comparison to previous DK for pre-layout ring oscillators
LVT_Standard_Report.pdf	SG LVT Comparison to previous DK
RVT_Analog_Report.pdf	SG RVT Comparison to previous DK - focus on analog performance
RVT_Biasing_Report.pdf	SG RVT Comparison to previous DK - focus on Vdd/Vbs variations
RVT_RO.pdf	SG RVT Comparison to previous DK for pre-layout ring oscillators
RVT_Standard_Report.pdf	SG RVT Comparison to previous DK
SG_LVT_vs_RVT_Analog_Report.pdf	SG LVT compared to SG RVT - focus on analog performance
SG_LVT_vs_RVT_RF_Report.pdf	SG LVT RF compared to SG RVT RF
SG_LVT_vs_RVT_Standard_Report.pdf	SG LVT compared to SG RVT
SG_Mismatch_Report.pdf	SG LVT and SG RVT Comparison to previous DK - focus on mismatch
SG_RF_Report.bch	SG RF compared to SG and SG RFSEG (both LVT and RVT)
SOA_usage.pdf	SOA user's manual
UTSOI210_documentation.pdf	UTSOI2.1.0 user's manual
UTSOI220_documentation_for_PDK.pdf	UTSOI 2.2 model documentation
ageing_WiCkeD.pdf	--

ageing_modelstatus.pdf	--
cmim.pdf	Comparison to previous DK
cmim_c0.pdf	Comparison to previous DK based on C0
cmim_leakage.pdf	omparison to previous DK based on leeakage current
cmim_matching.pdf	Comparison to previous DK
cmom_rf_custom.pdf	Comparison to previous DK and to usual cmom
differential_tline.pdf	Differential transmission line model description
diode.pdf	Comparaison to previous DK
esd_lowcap.pdf	esd_lowcap model description
esd_nfet_eg_hb.pdf	esd_nfet_eg_hb model description
esd_nfet_rvt_hb.pdf	esd_nfet_rvt_hb model description
esd_ppp.pdf	esd_ppp model description
ind_hq.pdf	HQ inductor model description
indsym_lohq.pdf	LoHQ inductor model description
indsym_lohq_high_perf.pdf	LoHQ high Perf inductor model description
microstrip_tline.pdf	Microstrip transmission line model description
modelstatus.pdf	Summary of model versions and changes wrt. previous DK
mos_psp_dr18otp.pdf	mos_psp_dr18otp model description
mos_psp_ext18hv.pdf	mos_psp_ext18hv model description
nwres.pdf	Comparison to previous DK
resistor.pdf	Poly resistors and opndres - Comparison to previous DK
soa_documentation.pdf	Summary of Safe Operating Area warnings
varmos1V0.pdf	SG MOS varactor model description
varmos1V8.pdf	EG MOS varactor model description

Library	Description	Release	Previous
common_beol	--	1.1	1.1
common_cmim16acc	--	1.0	1.0
common_esd	--	1.1	1.1
common_feol	--	1.1	1.1
common_fet	--	1.3	1.3
common_varactor	--	0.1	0.1
common_varind	--	2.0	2.0

cmim16acc **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cmim16acc	cmim16acc	1.0	MIM capacitor 16fF um2 without shield	■	■	■	■		■
cmim16acc_2p	cmim16acc_2p	1.0	2 pins capacitor 16fF um2 with shield	■	■	■	■		■
cmim16acc_2p	cmim16acc_2p_acc	1.0	2 pins capacitor 16fF um2 with shield	■	■	■	■		■
cmim16acc	cmim16acc_acc	1.0	MIM capacitor 16fF um2 without shield	■	■	■	■		■
cmim16acc_sh	cmim16acc_sh	1.0	MIM capacitor 16fF um2 with shield	■	■	■	■		■
cmim16acc_sh	cmim16acc_sh_acc	1.0	MIM capacitor 16fF um2 with shield	■	■	■	■		■

cmom_5u1x_1t8x_lb **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cmom_5U1x_1T8x_LB_2p	cmom_5U1x_1T8x_LB_2p	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_5U1x_1T8x_LB_2p	cmom_5U1x_1T8x_LB_2p_acc	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_5U1x_1T8x_LB_sh	cmom_5U1x_1T8x_LB_sh	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■
cmom_5U1x_1T8x_LB_sh	cmom_5U1x_1T8x_LB_sh_acc	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■

cmom_5u1x_1t8x_lb_wo_via **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cmom_5U1x_1T8x_LB_wo_via_2p	cmom_5U1x_1T8x_LB_wo_via_2p	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_5U1x_1T8x_LB_wo_via_2p	cmom_5U1x_1T8x_LB_wo_via_2p_acc	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_5U1x_1T8x_LB_wo_via_sh	cmom_5U1x_1T8x_LB_wo_via_sh	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■
cmom_5U1x_1T8x_LB_wo_via_sh	cmom_5U1x_1T8x_LB_wo_via_sh_acc	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■

cmom_5u1x_2t8x_lb **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cmom_5U1x_2T8x_LB_2p	cmom_5U1x_2T8x_LB_2p	0.1	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_5U1x_2T8x_LB_2p	cmom_5U1x_2T8x_LB_2p_acc	0.1	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_5U1x_2T8x_LB_sh	cmom_5U1x_2T8x_LB_sh	0.1	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■
cmom_5U1x_2T8x_LB_sh	cmom_5U1x_2T8x_LB_sh_acc	0.1	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■

cmom_5u1x_2t8x_lb_wo_via **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cmom_5U1x_2T8x_LB_wo_via_2p	cmom_5U1x_2T8x_LB_wo_via_2p	0.1	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_5U1x_2T8x_LB_wo_via_2p	cmom_5U1x_2T8x_LB_wo_via_2p_acc	0.1	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_5U1x_2T8x_LB_wo_via_sh	cmom_5U1x_2T8x_LB_wo_via_sh	0.1	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■
cmom_5U1x_2T8x_LB_wo_via_sh	cmom_5U1x_2T8x_LB_wo_via_sh_acc	0.1	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■

cmom_6u1x_2t8x_lb **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cmom_6U1x_2T8x_LB_2p	cmom_6U1x_2T8x_LB_2p	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_6U1x_2T8x_LB_2p	cmom_6U1x_2T8x_LB_2p_acc	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_6U1x_2T8x_LB_sh	cmom_6U1x_2T8x_LB_sh	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■
cmom_6U1x_2T8x_LB_sh	cmom_6U1x_2T8x_LB_sh_acc	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■

cmom_6u1x_2t8x_lb_wo_via **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cmom_6U1x_2T8x_LB_wo_via_2p	cmom_6U1x_2T8x_LB_wo_via_2p	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_6U1x_2T8x_LB_wo_via_2p	cmom_6U1x_2T8x_LB_wo_via_2p_acc	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_6U1x_2T8x_LB_wo_via_sh	cmom_6U1x_2T8x_LB_wo_via_sh	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■
cmom_6U1x_2T8x_LB_wo_via_sh	cmom_6U1x_2T8x_LB_wo_via_sh_acc	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■

cmom_6u1x_2u2x_2t8x_lb **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cmom_6U1x_2U2x_2T8x_LB_2p	cmom_6U1x_2U2x_2T8x_LB_2p	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_6U1x_2U2x_2T8x_LB_2p	cmom_6U1x_2U2x_2T8x_LB_2p_acc	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_6U1x_2U2x_2T8x_LB_sh	cmom_6U1x_2U2x_2T8x_LB_sh	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■
cmom_6U1x_2U2x_2T8x_LB_sh	cmom_6U1x_2U2x_2T8x_LB_sh_acc	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■

cmom_6u1x_2u2x_2t8x_lb_wo_via **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cmom_6U1x_2U2x_2T8x_LB_wo_via_2p	cmom_6U1x_2U2x_2T8x_LB_wo_via_2p	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_6U1x_2U2x_2T8x_LB_wo_via_2p	cmom_6U1x_2U2x_2T8x_LB_wo_via_2p_acc	1.0	2 pins Stacked Fringe Capacitance without shield	■	■	■	■		■
cmom_6U1x_2U2x_2T8x_LB_wo_via_sh	cmom_6U1x_2U2x_2T8x_LB_wo_via_sh	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■
cmom_6U1x_2U2x_2T8x_LB_wo_via_sh	cmom_6U1x_2U2x_2T8x_LB_wo_via_sh_acc	1.0	Stacked Fringe Capacitance with OD Poly shield	■	■	■	■		■

cmom_rf_custom **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cmom_rf_10f_100n	cmom_rf_10f_100n	1.1	cmom rf 10f 100n	■	■	■	■		■
cmom_rf_10f_80n	cmom_rf_10f_80n	1.1	cmom rf 10f 80n	■	■	■	■		■
cmom_rf_150f_100n	cmom_rf_150f_100n	1.1	cmom rf 150f 100n	■	■	■	■		■
cmom_rf_150f_80n	cmom_rf_150f_80n	1.1	cmom rf 150f 80n	■	■	■	■		■
cmom_rf_50f_100n	cmom_rf_50f_100n	1.1	cmom rf 50f 100n	■	■	■	■		■
cmom_rf_50f_80n	cmom_rf_50f_80n	1.1	cmom rf 50f 80n	■	■	■	■		■

cvar_eg **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cvar_eg	cvar_eg	2.1.a	varactor NMOS G02 single 1V8	■	■	■			
cvar_eg_atto	cvar_eg_atto	0.1.a	Varactor attofarad G02 diff	■	■	■			
cvar_eg_diff	cvar_eg_diff	2.1.a	varactor NMOS GO2 diff 1V8	■	■	■			

Device update for cvar_eg

DK name	Model name	Release	Previous	Change description
cvar_eg	cvar_eg	2.1.a	2.1	rpoly spread align to drm
cvar_eg_atto	cvar_eg_atto	0.1.a	0.1	Fix for multisim capability
cvar_eg_diff	cvar_eg_diff	2.1.a	2.1	rpoly spread align to drm

cvar_sg **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
cvar_sg	cvar_sg	2.0	varactor NMOS G01 single 1V0						

Device update for cvar_sg

DK name	Model name	Release	Previous	Change description
cvar_sg	cvar_sg	2.0	0.1	production model

differential_tline_6U1x_2T8x_LB **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
differential_tline_6U1x_2T8x_LB	differential_tline_6U1x_2T8x_LB	0.1	differential microstrip transmission line						

diode **ST Confidential**

DK Name	Model name	Release	Description	Model features				
				Process variations				
				Pre-defined corners	User-defined corners	Statistical models	LPE	SOA
diodenwx	diodenwx	1.1	Nwell/Psub Junction diode	■				■
diodenwx_lvs	diodenwx_lvs	1.1	Nwell/Psub Junction diode	■				■
diodenx	diodenx	1.1	Nplus/Psub Junction diode	■				■
diodepnw	diodepnw	1.1	Pplus/Nwell Junction diode	■				■
diodepwtw	diodepwtw	1.2.a	Pwell/Niso Junction diode	■				■
diodepwtw_lvs	diodepwtw_lvs	1.1	Pwell/Niso Junction diode	■				■
diodetwx	diodetwx	1.2.a	Niso/Psub Junction diode	■				■
diodetwx_lvs	diodetwx_lvs	1.1	Niso/Psub Junction diode	■				■
egdiodenx	egdiodenx	1.1	Pplus/Nwell Junction diode	■				■
egdiodepnw	egdiodepnw	1.1	Nplus/Psub Junction diode	■				■
egtdndsx	egtdndsx	1.1	EG N+ Floating Gate Tie-Down	■				■
egtdpdnw	egtdpdnw	1.1	EG P+ Floating Gate Tie-Down	■				■

driftotp **ST Confidential**

DK Name	Model name	Release	Description	Model features																				
				Process			Mismatch			Post-Layout														
										LPE														
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	Resistance	Capacitance	DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
ndriftotp	ndriftotp	1.2.b	Drift OTP	■	■	■	■	■	■	■	■									■

dsv **ST Confidential**

DK Name	Model name	Release	Description	Model features																		
				Process			Mismatch			Post-Layout												
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	LPE		DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
										Resistance	Capacitance										
dsvnfetpd	dsvnfetpd	1.0.g	Dense Cell 0.120 Single Well PD NFET	■	■	■	■	■	■	■	■										■
dsvnfetwl	dsvnfetwl	1.0.g	Dense Cell 0.120 Single Well PG NFET	■	■	■	■	■	■	■	■										■
dsvpfetpu	dsvpfetpu	1.0.g	Dense Cell 0.120 Single Well PU PFET	■	■	■	■	■	■	■	■										■

Device update for dsv

DK name	Model name	Release	Previous	Change description
dsvnfetpd	dsvnfetpd	1.0.g	1.0.f	Syntax update. No electrical change
dsvnfetwl	dsvnfetwl	1.0.g	1.0.f	Syntax update. No electrical change
dsvpfetpu	dsvpfetpu	1.0.g	1.0.f	Syntax update. No electrical change

dsw **ST Confidential**

DK Name	Model name	Release	Description	Model features																		
				Process			Mismatch			Post-Layout												
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	LPE		DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
										Resistance	Capacitance										
dswnfetpd	dswnfetpd	1.0.g	Dense Cell 0.120 PD NFET (SP0120LL / D120)	■	■	■	■	■	■	■	■										■
dswnfetwl	dswnfetwl	1.0.g	Dense Cell 0.120 PG NFET (SP0120LL / D120)	■	■	■	■	■	■	■	■										■
dswpfetpu	dswpfetpu	1.0.g	Dense Cell 0.120 PU PFET (SP0120LL / D120)	■	■	■	■	■	■	■	■										■

Device update for dsw

DK name	Model name	Release	Previous	Change description
dswnfetpd	dswnfetpd	1.0.g	1.0.f	Syntax update. No electrical change
dswnfetwl	dswnfetwl	1.0.g	1.0.f	Syntax update. No electrical change
dswpfetpu	dswpfetpu	1.0.g	1.0.f	Syntax update. No electrical change

dsx **ST Confidential**

DK Name	Model name	Release	Description	Model features																		
				Process			Mismatch			Post-Layout												
										LPE												
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	Resistance	Capacitance	DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
dsxnfetpd	dsxnfetpd	0.09.a	Dense Cell 0.126 Single Well PD NFET	■	■	■	■	■	■	■	■									■
dsxnfetwl	dsxnfetwl	0.09.a	Dense Cell 0.126 Single Well PD NFET	■	■	■	■	■	■	■	■									■
dsxpfetpu	dsxpfetpu	0.09.a	Dense Cell 0.126 Single Well PU PFET	■	■	■	■	■	■	■	■									■

Device update for dsx

DK name	Model name	Release	Previous	Change description
dsxnfetpd	dsxnfetpd	0.09.a	0.09	Syntax update. No electrical change
dsxnfetwl	dsxnfetwl	0.09.a	0.09	Syntax update. No electrical change
dsxpfetpu	dsxpfetpu	0.09.a	0.09	Syntax update. No electrical change

eg **ST Confidential**

DK Name	Model name	Release	Description	Model features																		
				Process			Mismatch			Post-Layout												
										LPE												
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	Resistance	Capacitance	DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
egnfet	egnfet_acc	1.2.c	Accurate 1.8V IO Nfet 28A	■	■	■	■	■	■	■	■	■	■							■
egpfet	egpfet_acc	1.2.c	Accurate 1.8V IO Pfet 28A	■	■	■	■	■	■	■	■	■	■	■						■
egvnfet	egvnfet_acc	1.2.c	Accurate 1.5V IO Nfet 28A	■	■	■	■	■	■	■	■	■	■							■
egvpfet	egvpfet_acc	1.2.c	Accurate 1.5V IO Pfet 28A	■	■	■	■	■	■	■	■	■	■	■						■

Device update for eg

DK name	Model name	Release	Previous	Change description
egnfet	egnfet_acc	1.2.c	1.2.b	Add dev=4 and Syntax update. No electrical change
egpfet	egpfet_acc	1.2.c	1.2.b	Add dev=4 and Syntax update. No electrical change
egvnfet	egvnfet_acc	1.2.c	1.2.b	Add dev=4 and Syntax update. No electrical change
egvpfet	egvpfet_acc	1.2.c	1.2.b	Add dev=4 and Syntax update. No electrical change

egext **ST Confidential**

DK Name	Model name	Release	Description	Model features																				
				Process			Mismatch			Post-Layout														
										LPE														
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	Resistance	Capacitance	DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
egnexti	egnexti	0.1	Extended Drain MOS	■		■	■	■	■	■	■									■
egpext	egpext	0.1	Extended Drain MOS	■		■	■	■	■	■	■									■

eglvt **ST Confidential**

DK Name	Model name	Release	Description	Model features																		
				Process			Mismatch			Post-Layout												
										LPE												
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	Resistance	Capacitance	DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
eglvtnfet	eglvtnfet_acc	1.2.e	Accurate 1.8V IO low Vt Nfet 28A	■	■	■	■	■	■	■	■	■		■						■
eglvtnfet_rf	eglvtnfet_rf	1.0.e	RF 1.8V IO low Vt Nfet 28A	■	■	■	■	■	■	■	■	■		■						■
eglvtnfet_rf	eglvtnfet_rfseg	1.0.e	NQS RF 1.8V IO low Vt Nfet 28A	■	■	■	■	■	■	■	■		■	■						■
eglvtpfet	eglvtpfet_acc	1.2.e	Accurate 1.8V IO low Vt Pfet 28A	■	■	■	■	■	■	■	■	■	■							■
eglvtpfet_rf	eglvtpfet_rf	1.0.e	RF 1.8V IO low Vt Pfet 28A	■	■	■	■	■	■	■	■	■	■							■
eglvtpfet_rf	eglvtpfet_rfseg	1.0.e	NQS RF 1.8V IO low Vt Pfet 28A	■	■	■	■	■	■	■	■	■	■							■
eglvtpspfet	eglvtpspfet	1.2.d	1.8V IO low Vt Pfet 28A	■	■	■	■	■	■	■	■	■	■							■
egvlvtnfet	eglvtvnfet_acc	1.2.e	Accurate 1.5V IO Nfet 28A	■	■	■	■	■	■	■	■			■						■
egvlvtpfet	eglvtvpfet_acc	1.2.e	Accurate 1.5V IO Pfet 28A	■	■	■	■	■	■	■	■	■								■
egvlvtnfet_rf	egvlvtnfet_rf	1.0.e	RF 1.5V IO low Vt Nfet 28A	■	■	■	■	■	■	■	■			■						■
egvlvtnfet_rf	egvlvtnfet_rfseg	1.0.e	NQS RF 1.5V IO low Vt Nfet 28A	■	■	■	■	■	■	■	■			■						■
egvlvtpfet_rf	egvlvtpfet_rf	1.0.e	RF 1.5V IO low Vt Pfet 28A	■	■	■	■	■	■	■	■	■								■
egvlvtpfet_rf	egvlvtpfet_rfseg	1.0.e	NQS RF 1.5V IO low Vt Pfet 28A	■	■	■	■	■	■	■	■	■								■

Device update for eglvt

DK name	Model name	Release	Previous	Change description
eglvtnfet	eglvtnfet_acc	1.2.e	1.2.d	Add dev=4 and Syntax update. No electrical change
eglvtnfet_rf	eglvtnfet_rf	1.0.e	1.0.d	Add dev=4 and Syntax update. No electrical change
eglvtnfet_rf	eglvtnfet_rfseg	1.0.e	1.0.d	Add dev=4 and Syntax update. No electrical change
eglvtpfet	eglvtpfet_acc	1.2.e	1.2.d	Add dev=4 and Syntax update. No electrical change
eglvtpfet_rf	eglvtpfet_rf	1.0.e	1.0.d	Add dev=4 and Syntax update. No electrical change
eglvtpfet_rf	eglvtpfet_rfseg	1.0.e	1.0.d	Add dev=4 and Syntax update. No electrical change
eglvtpspfet	eglvtpspfet	1.2.d	1.2.c	Syntax update. No electrical change
egvlvtnfet	eglvtvnfet_acc	1.2.e	1.2.d	Add dev=4 and Syntax update. No electrical change
egvlvtpfet	eglvtvpfet_acc	1.2.e	1.2.d	Add dev=4 and Syntax update. No electrical change
egvlvtnfet_rf	egvlvtnfet_rf	1.0.e	1.0.d	Add dev=4 and Syntax update. No electrical change
egvlvtnfet_rf	egvlvtnfet_rfseg	1.0.e	1.0.d	Add dev=4 and Syntax update. No electrical change
egvlvtpfet_rf	egvlvtpfet_rf	1.0.e	1.0.d	Add dev=4 and Syntax update. No electrical change
egvlvtpfet_rf	egvlvtpfet_rfseg	1.0.e	1.0.d	Add dev=4 and Syntax update. No electrical change

egncap **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
egncap	egncap	1.2	EG POLY N+ Nwell capacitor						

egnfetsb **ST Confidential**

DK Name	Model name	Release	Description	Model features																		
				Process			Mismatch			Post-Layout												
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	LPE		DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
										Resistance	Capacitance										
esdegnfet	esdegnfet	1.1	EG NFET	■		■	■	■	■												■
esdegnfet	esdegnfet_nova	1.1	EG NFET	■		■	■	■	■												■
esdegnfet	esdegnfet_va	1.1	EG NFET	■		■	■	■	■												■

egpcap **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
egpcap	egpcap	1.2	EG POLY P+ Pwell capacitor	■	■	■			■

esd_lowcap **ST Confidential**

DK Name	Model name	Release	Description	Model features				
				Process variations				
				Pre-defined corners	User-defined corners	Statistical models	LPE	SOA
esd_lowcap	esd_lowcap	0.1.a	ESD LOW CAP	■		■		■

Device update for esd_lowcap

DK name	Model name	Release	Previous	Change description
esd_lowcap	esd_lowcap	0.1.a	0.1	Fix on capacitance

esd_ulc_eg **ST Confidential**

DK Name	Model name	Release	Description	Model features				
				Process variations				
				Pre-defined corners	User-defined corners	Statistical models	LPE	SOA
esd_ulc_eg	esd_ulc_eg	0.1	ESD Ultra Low Cap EG	■		■		■

Device update for esd_ulc_eg

DK name	Model name	Release	Previous	Change description
esd_ulc_eg	esd_ulc_eg	0.1	0.01	Preliminary model

esd_ulc_rvt **ST Confidential**

DK Name	Model name	Release	Description	Model features				
				Process variations				
				Pre-defined corners	User-defined corners	Statistical models	LPE	SOA
esd_ulc_rvt	esd_ulc_rvt	0.1	ESD Ultra Low Cap RVT	■		■		■

Device update for esd_ulc_rvt

DK name	Model name	Release	Previous	Change description
esd_ulc_rvt	esd_ulc_rvt	0.1	0.01	Preliminary model

grhcdgated **ST Confidential**

DK Name	Model name	Release	Description	Model features				
				Process variations				
				Pre-defined corners	User-defined corners	Statistical models	LPE	SOA
esdvnpn_eg	esdvnpn_eg	1.2.a	Poly bounded TW N+/PW ESD Diode - EG version	■		■		■
esdvnpn_eg	esdvnpn_eg_nova	1.2.a	Poly bounded TW N+/PW ESD Diode - EG version	■		■		■
esdvnpn_eg	esdvnpn_eg_va	1.2.a	Poly bounded TW N+/PW ESD Diode - EG version	■		■		■
esdvpnp_eg	esdvpnp_eg	1.2.a	Poly bounded DW P+/NW ESD Diode - EG version	■		■		■
esdvpnp_eg	esdvpnp_eg_nova	1.2.a	Poly bounded DW P+/NW ESD Diode - EG version	■		■		■
esdvpnp_eg	esdvpnp_eg_va	1.2.a	Poly bounded DW P+/NW ESD Diode - EG version	■		■		■

Device update for grhcdgated

DK name	Model name	Release	Previous	Change description
esdvnpn_eg	esdvnpn_eg	1.2.a	1.2	SOA change
esdvnpn_eg	esdvnpn_eg_nova	1.2.a	1.2	SOA change
esdvnpn_eg	esdvnpn_eg_va	1.2.a	1.2	SOA change
esdvpnp_eg	esdvpnp_eg	1.2.a	1.2	SOA change
esdvpnp_eg	esdvpnp_eg_nova	1.2.a	1.2	SOA change
esdvpnp_eg	esdvpnp_eg_va	1.2.a	1.2	SOA change

grhcdsti **ST Confidential**

DK Name	Model name	Release	Description	Model features				
				Process variations				
				Pre-defined corners	User-defined corners	Statistical models	LPE	SOA
esdvnpn	esdvnpn	1.2.a	N+/PW Diode/Vertical NPN Bipolar (TW)	■		■		■
esdvnpn	esdvnpn_nova	1.2.a	N+/PW Diode/Vertical NPN Bipolar (TW)	■		■		■
esdvnpn	esdvnpn_va	1.2.a	N+/PW Diode/Vertical NPN Bipolar (TW)	■		■		■
esdvpnp	esdvpnp	1.2.a	P+/NW Diode/Vertical PNP Bipolar	■		■		■
esdvpnp	esdvpnp_nova	1.2.a	P+/NW Diode/Vertical PNP Bipolar	■		■		■
esdvpnp	esdvpnp_va	1.2.a	P+/NW Diode/Vertical PNP Bipolar	■		■		■

Device update for grhcdsti

DK name	Model name	Release	Previous	Change description
esdvnpn	esdvnpn	1.2.a	1.2	SOA change
esdvnpn	esdvnpn_nova	1.2.a	1.2	SOA change
esdvnpn	esdvnpn_va	1.2.a	1.2	SOA change
esdvpnp	esdvpnp	1.2.a	1.2	SOA change
esdvpnp	esdvpnp_nova	1.2.a	1.2	SOA change
esdvpnp	esdvpnp_va	1.2.a	1.2	SOA change

hcdgated **ST Confidential**

DK Name	Model name	Release	Description	Model features				
				Process variations				
				Pre-defined corners	User-defined corners	Statistical models	LPE	SOA
esdndsx_eg	esdndsx_eg	1.2.a	Poly bounded DW N+/PW ESD Diode - EG version	■		■		■
esdndsx_eg	esdndsx_eg_nova	1.2.a	Poly bounded DW N+/PW ESD Diode - EG version	■		■		■
esdndsx_eg	esdndsx_eg_va	1.2.a	Poly bounded DW N+/PW ESD Diode - EG version	■		■		■

Device update for hcdgated

DK name	Model name	Release	Previous	Change description
esdndsx_eg	esdndsx_eg	1.2.a	1.2	SOA change
esdndsx_eg	esdndsx_eg_nova	1.2.a	1.2	SOA change
esdndsx_eg	esdndsx_eg_va	1.2.a	1.2	SOA change

hcdsti **ST Confidential**

DK Name	Model name	Release	Description	Model features				
				Process variations				
				Pre-defined corners	User-defined corners	Statistical models	LPE	SOA
esdndsx	esdndsx	1.2.a	N+/PW Diode (DW) (ESD N+ Junction)	■		■		■
esdndsx	esdndsx_nova	1.2.a	N+/PW Diode (DW) (ESD N+ Junction)	■		■		■
esdndsx	esdndsx_va	1.2.a	N+/PW Diode (DW) (ESD N+ Junction)	■		■		■

Device update for hcdsti

DK name	Model name	Release	Previous	Change description
esdndsx	esdndsx	1.2.a	1.2	SOA change
esdndsx	esdndsx_nova	1.2.a	1.2	SOA change
esdndsx	esdndsx_va	1.2.a	1.2	SOA change

hlvt **ST Confidential**

DK Name	Model name	Release	Description	Model features																		
				Process			Mismatch			Post-Layout												
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	LPE		DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
										Resistance	Capacitance										
hlvtnfet	hlvtnfet	0.01.a	High Low Vt Nfet	■	■	■	■	■	■	■	■			■						■
hlvtpfet	hlvtpfet	0.01.a	High Low Vt Pfet	■	■	■	■	■	■	■	■		■							■

Device update for hlvt

DK name	Model name	Release	Previous	Change description
hlvtnfet	hlvtnfet	0.01.a	0.01	Syntax change, no electrical change
hlvtpfet	hlvtpfet	0.01.a	0.01	Syntax change, no electrical change

ind_hq_5U1x_2T8x_LB **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
ind_hq_5U1x_2T8x_LB	ind_hq_5U1x_2T8x_LB	0.03	Thick copper symmetrical HQ inductors with patterned GND shield	■	■	■			
inddif_hq_5U1x_2T8x_LB	inddif_hq_5U1x_2T8x_LB	0.03	Thick copper differential HQ inductors with patterned GND shield	■	■	■			

ind_hq_6U1x_2T8x_LB **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
ind_hq_6U1x_2T8x_LB	ind_hq_6U1x_2T8x_LB	2.0	Thick copper symmetrical HQ inductors with patterned GND shield	■	■	■			
inddif_hq_6U1x_2T8x_LB	inddif_hq_6U1x_2T8x_LB	2.0	Thick copper differential HQ inductors with patterned GND shield	■	■	■			

ind_hq_6U1x_2U2x_2T8x_LB **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
ind_hq_6U1x_2U2x_2T8x_LB	ind_hq_6U1x_2U2x_2T8x_LB	0.03	Thick copper symmetrical HQ inductors with patterned GND shield						
inddif_hq_6U1x_2U2x_2T8x_LB	inddif_hq_6U1x_2U2x_2T8x_LB	0.03	Thick copper differential HQ inductors with patterned GND shield						

ind_lohq_5U1x_2T8x_LB **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
ind_lohq_5U1x_2T8x_LB	ind_lohq_5U1x_2T8x_LB	0.03	Thick copper symmetrical low HQ inductors with patterned GND shield	■	■	■			
inddif_lohq_5U1x_2T8x_LB	inddif_lohq_5U1x_2T8x_LB	0.03	Thick copper differential low HQ inductors with patterned GND shield	■	■	■			

ind_lohq_6U1x_2T8x_LB **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
ind_lohq_6U1x_2T8x_LB	ind_lohq_6U1x_2T8x_LB	2.0	Thick copper symmetrical low HQ inductors with patterned GND shield	■	■	■			
inddif_lohq_6U1x_2T8x_LB	inddif_lohq_6U1x_2T8x_LB	2.0	Thick copper differential low HQ inductors with patterned GND shield	■	■	■			

ind_lohq_6U1x_2U2x_2T8x_LB **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
ind_lohq_6U1x_2U2x_2T8x_LB	ind_lohq_6U1x_2U2x_2T8x_LB	2.0	Thick copper symmetrical low HQ inductors with patterned GND shield	■	■	■			
inddif_lohq_6U1x_2U2x_2T8x_LB	inddif_lohq_6U1x_2U2x_2T8x_LB	2.0	Thick copper differential low HQ inductors with patterned GND shield	■	■	■			

ind_lohq_high_perf_6U1x_2T8x_LB **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
ind_lohq_high_perf_6U1x_2T8x_LB	ind_lohq_high_perf_6U1x_2T8x_LB	2.0	Thick copper symmetrical low HQ high perf inductors with patterned GND shield						
inddif_lohq_high_perf_6U1x_2T8x_LB	inddif_lohq_high_perf_6U1x_2T8x_LB	2.0	Thick copper differential low HQ high perf inductors with patterned GND shield						

lsd **ST Confidential**

DK Name	Model name	Release	Description	Model features																		
				Process			Mismatch			Post-Layout												
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	LPE		DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
										Resistance	Capacitance										
lsdnfetpd	lsdnfetpd	1.0.e	High Performance Cell 0.316 PD NFET (DP0316SW)	■	■	■	■	■	■	■	■										■
lsdnfetwl	lsdnfetwl	1.0.e	High Performance Cell 0.316 PG NFET (DP0316SW)	■	■	■	■	■	■	■	■										■
lsdpfetpu	lsdpfetpu	1.0.e	High Performance Cell 0.316 PU PFET (DP0316SW)	■	■	■	■	■	■	■	■										■

Device update for lsd

DK name	Model name	Release	Previous	Change description
lsdnfetpd	lsdnfetpd	1.0.e	1.0.d	Syntax update, no electrical change
lsdnfetwl	lsdnfetwl	1.0.e	1.0.d	Syntax update, no electrical change
lsdpfetpu	lsdpfetpu	1.0.e	1.0.d	Syntax update, no electrical change

lsl **ST Confidential**

DK Name	Model name	Release	Description	Model features																		
				Process			Mismatch			Post-Layout												
										LPE												
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	Resistance	Capacitance	DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
lslnfet	lslnfet	1.0.g	2-Port 0.251 Regular-Vt NFET (TP251)	■	■	■	■	■	■	■	■									■

Device update for lsl

DK name	Model name	Release	Previous	Change description
lslnfet	lslnfet	1.0.g	1.0.f	Syntax update, no electrical change

lsp **ST Confidential**

DK Name	Model name	Release	Description	Model features																		
				Process			Mismatch			Post-Layout												
										LPE												
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	Resistance	Capacitance	DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
lspnfetpd	lspnfetpd	1.0.f	2-Port 0.251 Single Well Pull Down NFET	■	■	■	■	■	■	■	■									■
lspnfetwl	lspnfetwl	1.0.f	2-Port 0.251 Single Well Pass Gate NFET	■	■	■	■	■	■	■	■									■
lsppfetpu	lsppfetpu	1.0.f	2-Port 0.251 Single Well Pull Up PFET	■	■	■	■	■	■	■	■									■

Device update for lsp

DK name	Model name	Release	Previous	Change description
lspnfetpd	lspnfetpd	1.0.f	1.0.e	Syntax update, no electrical change
lspnfetwl	lspnfetwl	1.0.f	1.0.e	Syntax update, no electrical change
lsppfetpu	lsppfetpu	1.0.f	1.0.e	Syntax update, no electrical change

lsv **ST Confidential**

DK Name	Model name	Release	Description	Model features																
				Process			Mismatch			Post-Layout										
										LPE										
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	Resistance	Capacitance	DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
lsvnfetpd	lsvnfetpd	1.0.g	Dense Cell 0.197 PD NFET (SP0197LL / B197)	■	■	■	■	■	■	■	■									■
lsvnfetwl	lsvnfetwl	1.0.g	Dense Cell 0.197 PG NFET (SP0197LL / B197)	■	■	■	■	■	■	■	■									■
lsvpfetpu	lsvpfetpu	1.0.g	Dense Cell 0.120 PU PFET (SP0197LL / B197)	■	■	■	■	■	■	■	■									■

Device update for lsv

DK name	Model name	Release	Previous	Change description
lsvnfetpd	lsvnfetpd	1.0.g	1.0.f	Syntax update, no electrical change
lsvnfetwl	lsvnfetwl	1.0.g	1.0.f	Syntax update, no electrical change
lsvpfetpu	lsvpfetpu	1.0.g	1.0.f	Syntax update, no electrical change

lvsres **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
lvsres	lvsres	0.01	LVSRES						

lvt **ST Confidential**

DK Name	Model name	Release	Description	Model features																
				Process			Mismatch			Post-Layout										
										LPE										
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	Resistance	Capacitance	DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
lvtnfet	lvtnfet_acc	1.3.e	Accurate Low Vt Nfet	■	■	■	■	■	■	■	■	■		■	■					■
lvtnfet_rf	lvtnfet_rf	1.0.e	RF Low Vt Nfet	■	■	■	■	■	■	■	■	■		■	■					■
lvtnfet_rf	lvtnfet_rfseg	1.0.e	NQS RF Low Vt Nfet	■	■	■	■	■	■	■	■	■		■	■					■
lvtpfet	lvtpfet_acc	1.3.e	Accurate Low Vt Pfet	■	■	■	■	■	■	■	■	■	■	■	■					■
lvtpfet_rf	lvtpfet_rf	1.0.e	RF Low Vt Pfet	■	■	■	■	■	■	■	■	■	■	■	■					■
lvtpfet_rf	lvtpfet_rfseg	1.0.e	NQS RF Low Vt Pfet	■	■	■	■	■	■	■	■	■	■	■	■					■

Device update for lvt

DK name	Model name	Release	Previous	Change description
lvtnfet	lvtnfet_acc	1.3.e	1.3.d	Add dev=4 and Syntax update, no electrical change
lvtnfet_rf	lvtnfet_rf	1.0.e	1.0.d	Add dev=4 and Syntax update, no electrical change
lvtnfet_rf	lvtnfet_rfseg	1.0.e	1.0.d	Add dev=4 and Syntax update, no electrical change
lvtpfet	lvtpfet_acc	1.3.e	1.3.d	Add dev=4 and Syntax update, no electrical change
lvtpfet_rf	lvtpfet_rf	1.0.e	1.0.d	Add dev=4 and Syntax update, no electrical change
lvtpfet_rf	lvtpfet_rfseg	1.0.e	1.0.d	Add dev=4 and Syntax update, no electrical change

microstrip_tline_6U1x_2T8x_LB **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
microstrip_tline_6U1x_2T8x_LB	microstrip_tline_6U1x_2T8x_LB	0.1	microstrip transmission line						

rndiff **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
opndres	opndres	1.3	Model for Unsilicided P+ Active Res.	■	■	■	■		■
opndres	opndres_std	1.3	Simple Model for Unsilicided P+ Active Res.	■	■	■	■		■

rnwell **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
nwres	nwres	1.3.a	Model for Nwell Res.	■	■	■	■		■
nwres	nwres_std	1.3.a	Simple Model for Nwell Res.	■	■	■	■		■

rpolyh **ST Confidential**

DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
opreres	opreres	1.3	Model for Unsilicided Re P+ Poly Res.	■	■	■	■		■
opreres	opreres_std	1.3	Simple Model for Unsilicided Re P+ Poly Res.	■	■	■	■		■

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DK Name	Model name	Release	Description	Model features					
				Process					
				Pre-defined corners	User-defined corners	Statistical models	Mismatch MC	LPE	SOA
opppcres	opppcres	1.3	Model for Unsilicided P+ Poly Res.	■	■	■	■		■
opppcres_lc	opppcres_lc	1.3	Model for Unsilicided P+ Poly Res.	■	■	■	■		■
opppcres_lc	opppcres_lc_std	1.3	Simple Model for Unsilicided P+ Poly Res.	■	■	■	■		■
opppcres	opppcres_std	1.3	Simple Model for Unsilicided P+ Poly Res.	■	■	■	■		■

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DK Name	Model name	Release	Description	Model features																		
				Process			Mismatch			Post-Layout												
										LPE												
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	Resistance	Capacitance	DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
nfet	nfet_acc	1.2.d	Accurate Regular Vt Nfet	■	■	■	■	■	■	■	■	■	■	■	■					■
nfet_rf	nfet_rf	1.0.c	RF Regular Vt nfet	■	■	■	■	■	■	■	■	■	■	■	■					■
nfet_rf	nfet_rfseg	1.0.c	NQS RF Regular Vt nfet	■	■	■	■	■	■	■	■	■	■	■	■					■
pfet	pfet_acc	1.2.d	Accurate Regular Vt Pfet	■	■	■	■	■	■	■	■	■	■	■	■					■
pfet_rf	pfet_rf	1.0.c	RF Regular Vt pfet	■	■	■	■	■	■	■	■	■	■	■	■					■
pfet_rf	pfet_rfseg	1.0.c	NQS RF Regular Vt pfet	■	■	■	■	■	■	■	■	■	■	■	■					■

Device update for rvt

DK name	Model name	Release	Previous	Change description
nfet	nfet_acc	1.2.d	1.2.c	Add dev=4 and Syntax update, no electrical change
nfet_rf	nfet_rf	1.0.c	1.0.b	Add dev=4 and Syntax update, no electrical change
nfet_rf	nfet_rfseg	1.0.c	1.0.b	Add dev=4 and Syntax update, no electrical change
pfet	pfet_acc	1.2.d	1.2.c	Add dev=4 and Syntax update, no electrical change
pfet_rf	pfet_rf	1.0.c	1.0.b	Add dev=4 and Syntax update, no electrical change
pfet_rf	pfet_rfseg	1.0.c	1.0.b	Add dev=4 and Syntax update, no electrical change

rvtnfetsb **ST Confidential**

DK Name	Model name	Release	Description	Model features																				
				Process			Mismatch			Post-Layout															
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte Carlo	LPE		DNW	WPE	LOD	PCPASTRX	POLYPITCH	RXRX	PGPROX	NRS-NRD	SOA
										Resistance	Capacitance										
esdnfet	esdnfet	1.1	SG NFET	■		■	■	■	■												■
esdnfet	esdnfet_nova	1.1	SG NFET	■		■	■	■	■												■
esdnfet	esdnfet_va	1.1	SG NFET	■		■	■	■	■												■