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C28SOI_SC_8_CORE_LL Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells

Overview

- C28SOI_SC_8_CORE_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

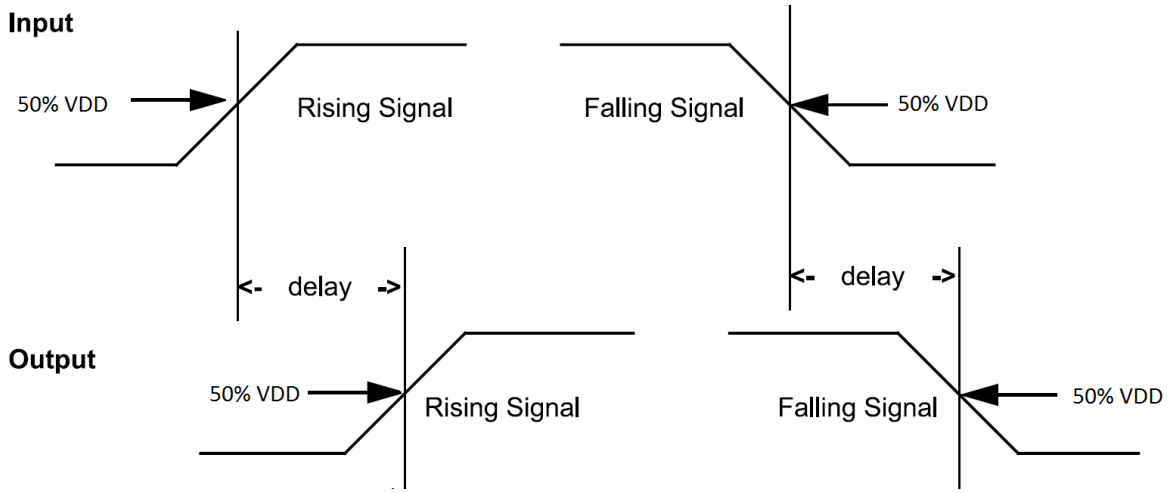


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

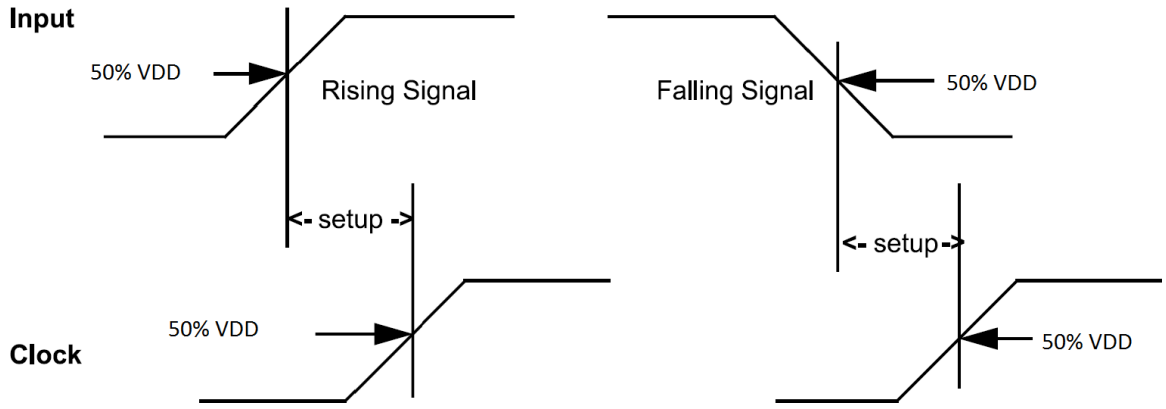


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

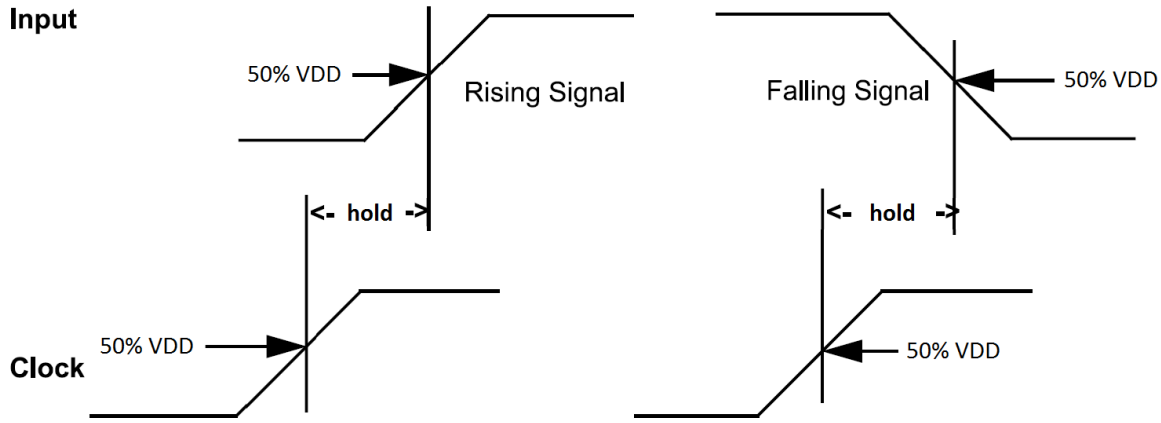


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

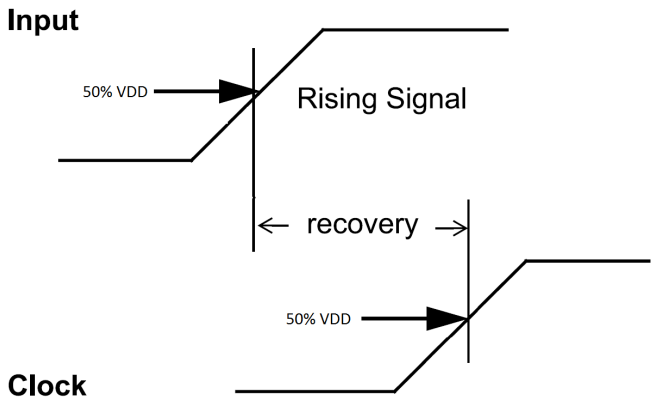


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

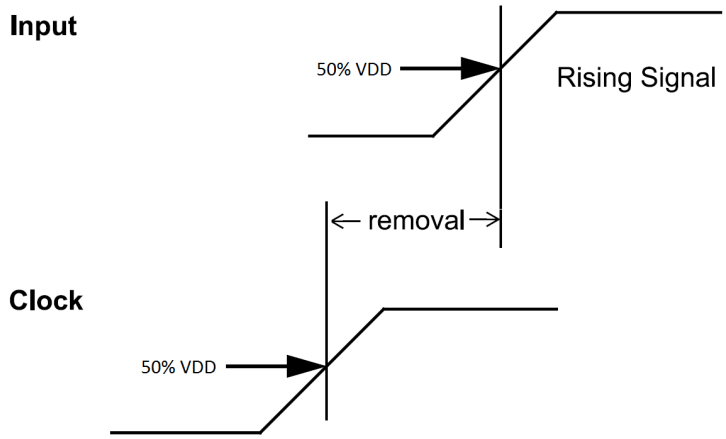


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

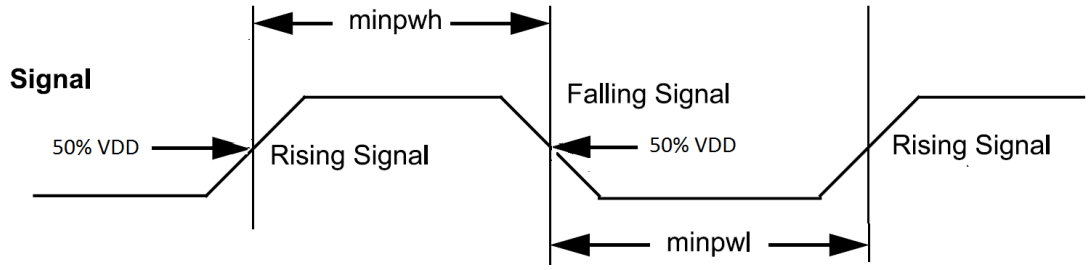


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

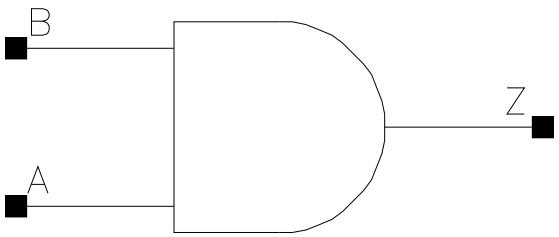
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.544	0.4352
X10_P0	0.800	0.680	0.5440
X11_P0	1.600	0.544	0.8704
X19_P0	0.800	1.224	0.9792
X24_P0	0.800	1.360	1.0880
X29_P0	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X11_P0	X19_P0
A	0.0004	0.0006	0.0008	0.0012
B	0.0004	0.0006	0.0008	0.0011
	X24_P0	X29_P0		
A	0.0012	0.0012		
B	0.0011	0.0010		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0289	0.0229	3.7758	1.7970
A to Z ↑	0.0234	0.0212	5.5090	2.6287
B to Z ↓	0.0279	0.0216	3.7706	1.7935
B to Z ↑	0.0250	0.0224	5.5005	2.6293
	X11_P0	**X19_P0**	**X11_P0**	**X19_P0**

A to Z ↓	0.0249	0.0224	1.3818	0.9216
A to Z ↑	0.0194	0.0207	2.5338	1.3246
B to Z ↓	0.0234	0.0215	1.3796	0.9223
B to Z ↑	0.0206	0.0222	2.5347	1.3238
	X24_P0	**X29_P0**	**X24_P0**	**X29_P0**
A to Z ↓	0.0242	0.0256	0.7493	0.6240
A to Z ↑	0.0226	0.0241	1.0625	0.8823
B to Z ↓	0.0235	0.0249	0.7486	0.6243
B to Z ↑	0.0243	0.0259	1.0615	0.8821

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	3.970e-05	1.000e-20
X10_P0	9.207e-05	1.000e-20
X11_P0	1.049e-04	1.000e-20
X19_P0	1.748e-04	1.000e-20
X24_P0	2.027e-04	1.000e-20
X29_P0	2.306e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X11_P0	X19_P0
A (output stable)	6.009e-06	1.234e-05	1.660e-05	2.315e-05
B (output stable)	1.125e-05	2.125e-05	2.925e-05	4.306e-05
A to Z	1.229e-03	2.073e-03	2.478e-03	4.082e-03
B to Z	1.191e-03	2.012e-03	2.365e-03	3.940e-03
	X24_P0	X29_P0		
A (output stable)	2.296e-05	2.305e-05		
B (output stable)	4.295e-05	4.286e-05		
A to Z	4.974e-03	5.808e-03		
B to Z	4.842e-03	5.690e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

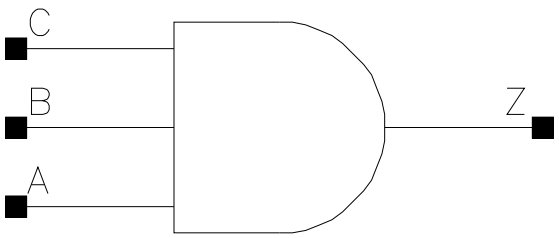
Pin Cycle (vdds)	X5_P0	X10_P0	X11_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P0	X29_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.680	0.5440
X10_P0	0.800	0.816	0.6528
X14_P0	0.800	1.360	1.0880
X19_P0	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0006	0.0011	0.0013
B	0.0004	0.0006	0.0009	0.0011
C	0.0004	0.0006	0.0008	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0325	0.0256	3.8158	1.8071
A to Z ↑	0.0321	0.0283	5.5772	2.6563
B to Z ↓	0.0317	0.0245	3.8200	1.8064
B to Z ↑	0.0335	0.0293	5.5630	2.6553
C to Z ↓	0.0308	0.0235	3.8119	1.8043
C to Z ↑	0.0348	0.0300	5.5747	2.6551
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0261	0.0245	1.2440	0.9260

A to Z ↑	0.0275	0.0266	1.8016	1.3359
B to Z ↓	0.0249	0.0234	1.2432	0.9246
B to Z ↑	0.0286	0.0278	1.8001	1.3366
C to Z ↓	0.0239	0.0224	1.2421	0.9243
C to Z ↑	0.0295	0.0286	1.8036	1.3356

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	3.758e-05	1.000e-20
X10_P0	8.732e-05	1.000e-20
X14_P0	1.215e-04	1.000e-20
X19_P0	1.679e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	6.711e-06	1.403e-05	1.873e-05	2.550e-05
B (output stable)	8.700e-06	1.652e-05	2.316e-05	3.229e-05
C (output stable)	1.879e-05	3.545e-05	5.096e-05	7.535e-05
A to Z	1.443e-03	2.417e-03	3.562e-03	4.650e-03
B to Z	1.399e-03	2.337e-03	3.429e-03	4.474e-03
C to Z	1.367e-03	2.269e-03	3.329e-03	4.318e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

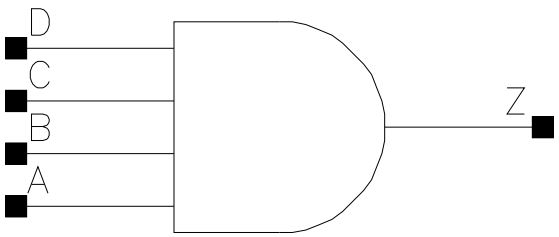
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.088	0.8704
X3_P0	0.800	1.088	0.8704
X10_P0	0.800	2.176	1.7408
X13_P0	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P0	X3_P0	X10_P0	X13_P0
A	0.0004	0.0004	0.0009	0.0010
B	0.0004	0.0004	0.0009	0.0010
C	0.0004	0.0004	0.0009	0.0010
D	0.0004	0.0004	0.0009	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	X3_P0	X2_P0	X3_P0
A to Z ↓	0.0255	0.0272	7.2897	4.6684
A to Z ↑	0.0271	0.0268	20.4809	10.7142
B to Z ↓	0.0242	0.0263	7.2915	4.6691
B to Z ↑	0.0284	0.0283	20.5008	10.7187
C to Z ↓	0.0263	0.0281	7.2797	4.6435
C to Z ↑	0.0273	0.0269	20.5132	10.7271

D to Z ↓	0.0252	0.0279	7.2821	4.6382
D to Z ↑	0.0291	0.0297	20.5081	10.7234
	X10_P0	**X13_P0**	**X10_P0**	**X13_P0**
A to Z ↓	0.0253	0.0253	1.5963	1.1880
A to Z ↑	0.0250	0.0271	3.5259	2.7052
B to Z ↓	0.0243	0.0233	1.5957	1.1871
B to Z ↑	0.0264	0.0277	3.5253	2.7029
C to Z ↓	0.0254	0.0242	1.5838	1.1889
C to Z ↑	0.0241	0.0236	3.5223	2.7010
D to Z ↓	0.0232	0.0222	1.5797	1.1880
D to Z ↑	0.0245	0.0240	3.5224	2.7008

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P0	3.132e-05	1.000e-20
X3_P0	4.253e-05	1.000e-20
X10_P0	1.329e-04	1.000e-20
X13_P0	1.843e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P0	X3_P0	X10_P0	X13_P0
A (output stable)	2.565e-04	2.999e-04	7.812e-04	1.076e-03
B (output stable)	2.422e-04	2.835e-04	7.396e-04	1.006e-03
C (output stable)	2.665e-04	2.916e-04	7.588e-04	9.636e-04
D (output stable)	2.520e-04	2.839e-04	7.033e-04	8.915e-04
A to Z	9.505e-04	1.259e-03	3.520e-03	4.808e-03
B to Z	9.110e-04	1.214e-03	3.406e-03	4.531e-03
C to Z	9.843e-04	1.276e-03	3.200e-03	4.044e-03
D to Z	9.461e-04	1.255e-03	2.969e-03	3.774e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

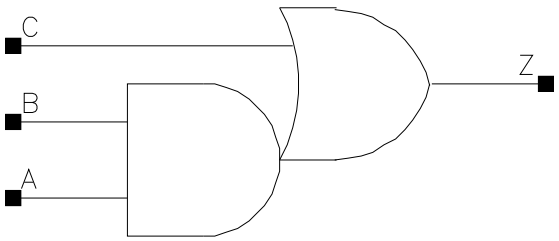
Pin Cycle (vdds)	X2_P0	X3_P0	X10_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	0.952	0.7616
X19_P0	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0004	0.0005	0.0011
B	0.0004	0.0006	0.0009
C	0.0004	0.0006	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0395	0.0339	3.6038	1.8076
A to Z ↑	0.0264	0.0233	5.1308	2.6068
B to Z ↓	0.0375	0.0321	3.5927	1.8029
B to Z ↑	0.0284	0.0251	5.1218	2.6028
C to Z ↓	0.0403	0.0332	3.5864	1.8003
C to Z ↑	0.0243	0.0214	5.0910	2.5877
	X19_P0		**X19_P0**	
A to Z ↓	0.0325		0.9373	
A to Z ↑	0.0257		1.3150	

B to Z ↓	0.0314		0.9376	
B to Z ↑	0.0275		1.3151	
C to Z ↓	0.0322		0.9356	
C to Z ↑	0.0230		1.3028	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	4.533e-05	1.000e-20
X10_P0	9.218e-05	1.000e-20
X19_P0	1.667e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	2.324e-05	3.096e-05	6.892e-05
B (output stable)	2.467e-05	3.616e-05	7.653e-05
C (output stable)	3.228e-05	4.417e-05	1.040e-04
A to Z	1.454e-03	2.410e-03	4.639e-03
B to Z	1.412e-03	2.334e-03	4.545e-03
C to Z	1.564e-03	2.520e-03	4.865e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

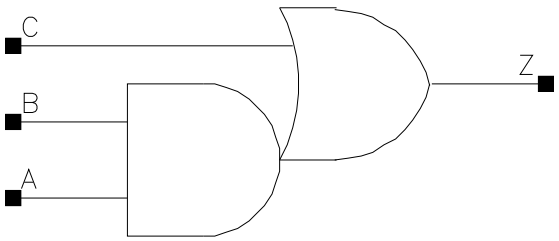
Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	0.952	0.7616
X14_P0	0.800	1.632	1.3056
X19_P0	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0005	0.0011	0.0011
B	0.0004	0.0005	0.0011	0.0011
C	0.0004	0.0006	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0412	0.0350	3.5919	1.8213
A to Z ↑	0.0287	0.0257	5.2216	2.6219
B to Z ↓	0.0400	0.0336	3.5829	1.8160
B to Z ↑	0.0313	0.0275	5.2238	2.6254
C to Z ↓	0.0361	0.0316	3.5698	1.8124
C to Z ↑	0.0212	0.0186	5.1538	2.5978
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0317	0.0339	1.2393	0.9323

A to Z ↑	0.0234	0.0248	1.7772	1.3269
B to Z ↓	0.0289	0.0313	1.2346	0.9288
B to Z ↑	0.0243	0.0260	1.7755	1.3274
C to Z ↓	0.0264	0.0288	1.2317	0.9260
C to Z ↑	0.0162	0.0174	1.7601	1.3128

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	4.548e-05	1.000e-20
X10_P0	8.824e-05	1.000e-20
X14_P0	1.566e-04	1.000e-20
X19_P0	1.799e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	8.644e-06	1.127e-05	3.874e-05	3.861e-05
B (output stable)	1.109e-05	1.402e-05	6.036e-05	6.009e-05
C (output stable)	1.006e-04	1.138e-04	3.332e-04	3.331e-04
A to Z	1.588e-03	2.465e-03	4.215e-03	5.055e-03
B to Z	1.550e-03	2.392e-03	3.925e-03	4.778e-03
C to Z	1.353e-03	2.144e-03	3.445e-03	4.214e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

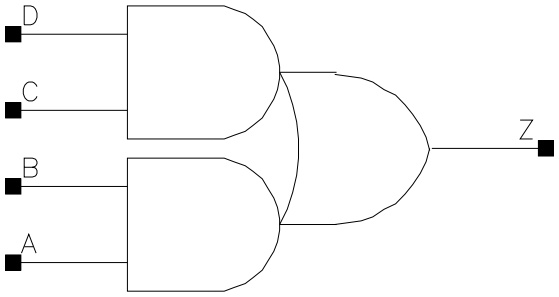
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.088	0.8704
X10_P0	0.800	1.088	0.8704
X14_P0	0.800	1.768	1.4144
X19_P0	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0006	0.0011	0.0011
B	0.0004	0.0008	0.0010	0.0010
C	0.0004	0.0005	0.0012	0.0012
D	0.0004	0.0006	0.0010	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0421	0.0347	3.6112	1.8159
A to Z ↑	0.0300	0.0268	5.2520	2.6059
B to Z ↓	0.0390	0.0318	3.5910	1.8058

B to Z ↑	0.0309	0.0278	5.2484	2.6032
C to Z ↓	0.0377	0.0315	3.5949	1.8089
C to Z ↑	0.0255	0.0225	5.2379	2.5972
D to Z ↓	0.0365	0.0302	3.5898	1.8062
D to Z ↑	0.0277	0.0243	5.2367	2.5974
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0312	0.0337	1.2385	0.9355
A to Z ↑	0.0240	0.0257	1.7838	1.3359
B to Z ↓	0.0295	0.0320	1.2365	0.9340
B to Z ↑	0.0256	0.0274	1.7833	1.3358
C to Z ↓	0.0287	0.0312	1.2358	0.9331
C to Z ↑	0.0206	0.0223	1.7765	1.3317
D to Z ↓	0.0271	0.0297	1.2342	0.9322
D to Z ↑	0.0219	0.0237	1.7766	1.3311

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	5.244e-05	1.000e-20
X10_P0	1.058e-04	1.000e-20
X14_P0	1.757e-04	1.000e-20
X19_P0	2.014e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	2.176e-05	2.831e-05	3.420e-05	3.395e-05
B (output stable)	6.686e-05	6.779e-05	4.307e-05	4.296e-05
C (output stable)	2.405e-05	3.056e-05	7.307e-05	7.340e-05
D (output stable)	2.604e-05	3.747e-05	8.592e-05	8.628e-05
A to Z	1.799e-03	2.749e-03	4.390e-03	5.325e-03
B to Z	1.650e-03	2.529e-03	4.200e-03	5.137e-03
C to Z	1.553e-03	2.388e-03	3.758e-03	4.666e-03
D to Z	1.504e-03	2.321e-03	3.607e-03	4.510e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

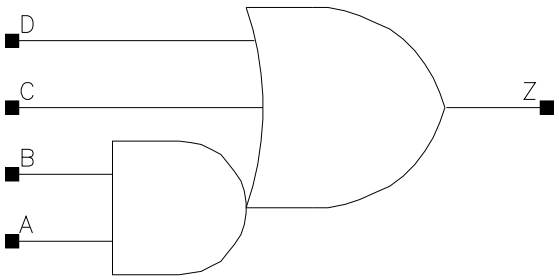
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	1.088	0.8704
X19_P0	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0004	0.0005	0.0010
B	0.0004	0.0005	0.0010
C	0.0004	0.0005	0.0011
D	0.0004	0.0005	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0495	0.0408	4.0116	1.8776
A to Z ↑	0.0275	0.0226	5.4666	2.6138
B to Z ↓	0.0483	0.0385	4.0035	1.8699
B to Z ↑	0.0296	0.0243	5.4667	2.6140
C to Z ↓	0.0522	0.0428	3.9949	1.8697
C to Z ↑	0.0247	0.0304	5.4197	2.6197

D to Z ↓	0.0519	0.0434	3.9968	1.8706
D to Z ↑	0.0245	0.0300	5.4208	2.6174
	X19_P0		**X19_P0**	
A to Z ↓	0.0404		0.9708	
A to Z ↑	0.0250		1.3033	
B to Z ↓	0.0370		0.9659	
B to Z ↑	0.0257		1.3021	
C to Z ↓	0.0415		0.9660	
C to Z ↑	0.0246		1.2966	
D to Z ↓	0.0409		0.9665	
D to Z ↑	0.0242		1.2953	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	3.661e-05	1.000e-20
X10_P0	8.104e-05	1.000e-20
X19_P0	1.496e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	2.930e-05	5.707e-05	9.454e-05
B (output stable)	2.847e-05	5.677e-05	1.063e-04
C (output stable)	1.465e-05	2.706e-05	5.739e-05
D (output stable)	1.903e-05	3.570e-05	6.605e-05
A to Z	1.555e-03	2.562e-03	5.017e-03
B to Z	1.519e-03	2.474e-03	4.715e-03
C to Z	1.695e-03	2.909e-03	5.480e-03
D to Z	1.631e-03	2.798e-03	5.214e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

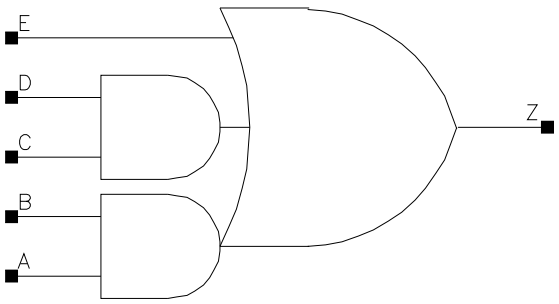
Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.088	0.8704
X10_P0	0.800	1.224	0.9792
X19_P0	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0003	0.0005	0.0010
B	0.0004	0.0005	0.0009
C	0.0004	0.0007	0.0011
D	0.0004	0.0005	0.0009
E	0.0004	0.0005	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0619	0.0473	3.7706	1.8659
A to Z ↑	0.0350	0.0284	5.3063	2.6290

B to Z ↓	0.0618	0.0456	3.7594	1.8629
B to Z ↑	0.0382	0.0302	5.3068	2.6283
C to Z ↓	0.0550	0.0424	3.7603	1.8629
C to Z ↑	0.0309	0.0243	5.2655	2.6113
D to Z ↓	0.0523	0.0390	3.7474	1.8554
D to Z ↑	0.0331	0.0256	5.2666	2.6094
E to Z ↓	0.0556	0.0422	3.7397	1.8556
E to Z ↑	0.0266	0.0218	5.2149	2.5942
	X19_P0		**X19_P0**	
A to Z ↓	0.0456		0.9602	
A to Z ↑	0.0295		1.3222	
B to Z ↓	0.0437		0.9590	
B to Z ↑	0.0316		1.3217	
C to Z ↓	0.0395		0.9580	
C to Z ↑	0.0245		1.3115	
D to Z ↓	0.0377		0.9553	
D to Z ↑	0.0263		1.3102	
E to Z ↓	0.0404		0.9549	
E to Z ↑	0.0276		1.3076	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	4.524e-05	1.000e-20
X10_P0	9.714e-05	1.000e-20
X19_P0	1.741e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	8.548e-06	1.538e-05	3.071e-05
B (output stable)	1.219e-05	1.683e-05	3.126e-05
C (output stable)	3.631e-05	4.363e-05	9.523e-05
D (output stable)	3.765e-05	5.237e-05	1.011e-04
E (output stable)	5.172e-05	7.549e-05	1.572e-04
A to Z	2.102e-03	3.188e-03	6.120e-03
B to Z	2.080e-03	3.096e-03	5.935e-03
C to Z	1.800e-03	2.682e-03	5.052e-03
D to Z	1.748e-03	2.573e-03	4.912e-03
E to Z	1.841e-03	2.784e-03	5.364e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

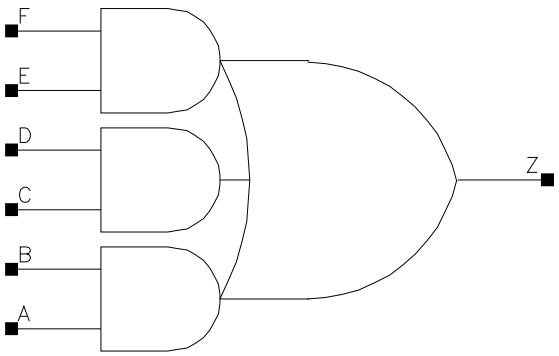
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.360	1.0880
X5_P0	0.800	1.360	1.0880
X10_P0	0.800	1.632	1.3056
X19_P0	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P0	X5_P0	X10_P0	X19_P0
A	0.0004	0.0004	0.0006	0.0010

B	0.0004	0.0004	0.0007	0.0009
C	0.0006	0.0006	0.0005	0.0010
D	0.0004	0.0004	0.0005	0.0009
E	0.0006	0.0006	0.0005	0.0011
F	0.0005	0.0005	0.0005	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X5_P0**	**X2_P0**	**X5_P0**
A to Z ↓	0.0471	0.0484	7.4746	3.8802
A to Z ↑	0.0342	0.0334	10.6444	5.5712
B to Z ↓	0.0454	0.0467	7.4526	3.8690
B to Z ↑	0.0368	0.0360	10.6358	5.5707
C to Z ↓	0.0441	0.0455	7.4685	3.8784
C to Z ↑	0.0318	0.0311	10.5423	5.5264
D to Z ↓	0.0407	0.0421	7.4492	3.8677
D to Z ↑	0.0334	0.0327	10.5325	5.5229
E to Z ↓	0.0368	0.0380	7.4446	3.8670
E to Z ↑	0.0265	0.0258	10.4702	5.4971
F to Z ↓	0.0342	0.0357	7.4264	3.8574
F to Z ↑	0.0278	0.0274	10.4676	5.4957
	X10_P0	**X19_P0**	**X10_P0**	**X19_P0**
A to Z ↓	0.0516	0.0473	1.8712	0.9588
A to Z ↑	0.0352	0.0319	2.6488	1.3280
B to Z ↓	0.0489	0.0458	1.8597	0.9570
B to Z ↑	0.0366	0.0341	2.6494	1.3267
C to Z ↓	0.0472	0.0439	1.8654	0.9579
C to Z ↑	0.0315	0.0294	2.6341	1.3193
D to Z ↓	0.0458	0.0426	1.8606	0.9563
D to Z ↑	0.0337	0.0315	2.6348	1.3183
E to Z ↓	0.0416	0.0399	1.8607	0.9558
E to Z ↑	0.0270	0.0257	2.6223	1.3148
F to Z ↓	0.0395	0.0378	1.8552	0.9533
F to Z ↑	0.0288	0.0276	2.6222	1.3145

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P0	4.843e-05	1.000e-20
X5_P0	6.274e-05	1.000e-20
X10_P0	1.062e-04	1.000e-20
X19_P0	2.024e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P0	X5_P0	X10_P0	X19_P0
A (output stable)	1.868e-05	1.869e-05	3.010e-05	4.270e-05
B (output stable)	1.953e-05	1.958e-05	5.080e-05	4.570e-05
C (output stable)	2.750e-05	2.760e-05	2.803e-05	5.733e-05
D (output stable)	3.101e-05	3.110e-05	3.224e-05	6.715e-05
E (output stable)	6.196e-05	6.219e-05	7.963e-05	1.251e-04
F (output stable)	6.769e-05	6.792e-05	7.999e-05	1.325e-04

A to Z	1.898e-03	2.226e-03	3.598e-03	6.564e-03
B to Z	1.835e-03	2.160e-03	3.397e-03	6.389e-03
C to Z	1.603e-03	1.923e-03	3.197e-03	5.863e-03
D to Z	1.525e-03	1.842e-03	3.125e-03	5.731e-03
E to Z	1.287e-03	1.590e-03	2.812e-03	5.273e-03
F to Z	1.230e-03	1.532e-03	2.736e-03	5.114e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

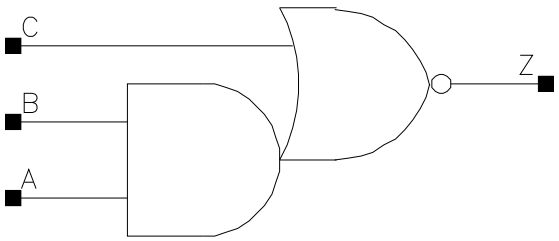
Pin Cycle (vdds)	X2_P0	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X10_P0	0.800	1.360	1.0880
X19_P0	0.800	2.584	2.0672
X25_P0	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P0	X10_P0	X19_P0	X25_P0
A	0.0005	0.0013	0.0025	0.0033
B	0.0004	0.0011	0.0023	0.0031
C	0.0005	0.0013	0.0025	0.0034

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X10_P0**	**X3_P0**	**X10_P0**
A to Z ↓	0.0086	0.0091	6.1472	2.2076
A to Z ↑	0.0164	0.0167	10.1710	3.4683
B to Z ↓	0.0092	0.0095	6.1908	2.2262
B to Z ↑	0.0142	0.0137	10.0012	3.4586
C to Z ↓	0.0088	0.0089	3.6871	1.2838
C to Z ↑	0.0164	0.0165	9.2998	3.1961
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0096	0.0095	1.1236	0.8554

A to Z ↑	0.0173	0.0169	1.7691	1.3194
B to Z ↓	0.0095	0.0095	1.1337	0.8633
B to Z ↑	0.0139	0.0139	1.7663	1.3311
C to Z ↓	0.0106	0.0107	0.7815	0.6012
C to Z ↑	0.0167	0.0166	1.6324	1.2235

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	3.865e-05	1.000e-20
X10_P0	1.023e-04	1.000e-20
X19_P0	1.945e-04	1.000e-20
X25_P0	2.579e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X10_P0	X19_P0	X25_P0
A (output stable)	3.030e-05	1.095e-04	2.206e-04	2.904e-04
B (output stable)	3.840e-05	1.340e-04	2.730e-04	3.522e-04
C (output stable)	4.629e-05	1.503e-04	2.946e-04	4.022e-04
A to Z	6.331e-04	1.947e-03	4.008e-03	5.237e-03
B to Z	5.678e-04	1.619e-03	3.287e-03	4.350e-03
C to Z	8.308e-04	2.461e-03	4.867e-03	6.479e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

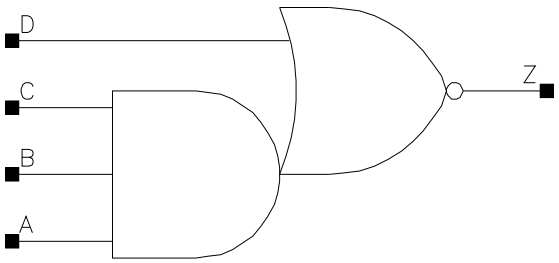
Pin Cycle (vdds)	X3_P0	X10_P0	X19_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X17_P0	0.800	3.536	2.8288
X22_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X17_P0	X22_P0
A	0.0004	0.0025	0.0034
B	0.0004	0.0024	0.0032
C	0.0006	0.0022	0.0031
D	0.0005	0.0026	0.0034

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X17_P0	X3_P0	X17_P0
A to Z ↓	0.0134	0.0142	8.6861	1.6316
A to Z ↑	0.0213	0.0205	10.1630	1.7168
B to Z ↓	0.0143	0.0145	8.7106	1.6375
B to Z ↑	0.0195	0.0186	10.1716	1.7375
C to Z ↓	0.0157	0.0139	8.7458	1.6419
C to Z ↑	0.0189	0.0157	10.2131	1.7449
D to Z ↓	0.0111	0.0127	3.6025	0.7715

D to Z ↑	0.0211	0.0194	8.7550	1.4892
	X22_P0		**X22_P0**	
A to Z ↓	0.0140		1.2381	
A to Z ↑	0.0202		1.2852	
B to Z ↓	0.0142		1.2428	
B to Z ↑	0.0182		1.3040	
C to Z ↓	0.0138		1.2467	
C to Z ↑	0.0155		1.3127	
D to Z ↓	0.0133		0.6404	
D to Z ↑	0.0187		1.1153	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	4.050e-05	1.000e-20
X17_P0	1.879e-04	1.000e-20
X22_P0	2.425e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X17_P0	X22_P0
A (output stable)	2.510e-05	1.595e-04	2.103e-04
B (output stable)	2.623e-05	1.715e-04	2.228e-04
C (output stable)	3.197e-05	2.667e-04	3.453e-04
D (output stable)	7.259e-05	4.358e-04	5.730e-04
A to Z	9.232e-04	5.238e-03	6.815e-03
B to Z	8.355e-04	4.509e-03	5.847e-03
C to Z	7.721e-04	3.817e-03	4.961e-03
D to Z	1.172e-03	6.190e-03	8.013e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

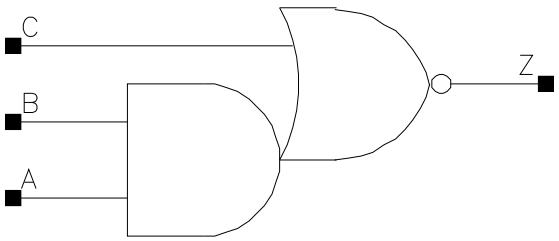
Pin Cycle (vdds)	X3_P0	X17_P0	X22_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X6_P0	0.800	1.088	0.8704
X9_P0	0.800	1.360	1.0880
X12_P0	0.800	1.904	1.5232
X25_P0	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X9_P0	X12_P0
A	0.0004	0.0009	0.0014	0.0019
B	0.0004	0.0009	0.0013	0.0017
C	0.0005	0.0008	0.0011	0.0016
	X25_P0			
A	0.0037			
B	0.0034			
C	0.0031			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0120	0.0115	8.2240	3.2204
A to Z ↑	0.0180	0.0190	11.6650	5.1656
B to Z ↓	0.0136	0.0117	8.2603	3.2435

B to Z ↑	0.0166	0.0161	11.5325	5.1776
C to Z ↓	0.0076	0.0065	4.9813	2.3374
C to Z ↑	0.0147	0.0133	10.6822	4.7615
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0109	0.0114	2.2127	1.6595
A to Z ↑	0.0176	0.0180	3.4591	2.5658
B to Z ↓	0.0115	0.0114	2.2295	1.6726
B to Z ↑	0.0147	0.0149	3.4567	2.5928
C to Z ↓	0.0065	0.0064	1.6037	1.1925
C to Z ↑	0.0126	0.0128	3.1883	2.3797
	X25_P0		**X25_P0**	
A to Z ↓	0.0111		0.8625	
A to Z ↑	0.0174		1.3006	
B to Z ↓	0.0115		0.8686	
B to Z ↑	0.0144		1.3043	
C to Z ↓	0.0063		0.6068	
C to Z ↑	0.0123		1.2026	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	3.023e-05	1.000e-20
X6_P0	7.229e-05	1.000e-20
X9_P0	1.007e-04	1.000e-20
X12_P0	1.357e-04	1.000e-20
X25_P0	2.630e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	1.117e-05	3.797e-05	4.912e-05	7.255e-05
B (output stable)	1.369e-05	5.915e-05	6.855e-05	1.093e-04
C (output stable)	1.219e-04	3.233e-04	3.923e-04	5.506e-04
A to Z	7.292e-04	1.783e-03	2.433e-03	3.368e-03
B to Z	6.714e-04	1.520e-03	2.059e-03	2.802e-03
C to Z	5.115e-04	1.127e-03	1.556e-03	2.153e-03
	X25_P0			
A (output stable)	1.383e-04			
B (output stable)	1.911e-04			
C (output stable)	1.024e-03			
A to Z	6.406e-03			
B to Z	5.407e-03			
C to Z	4.084e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

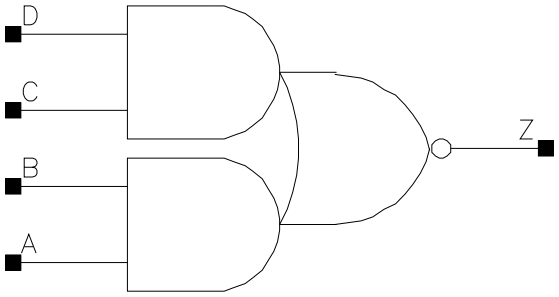
	X25_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.680	0.5440
X6_P0	0.800	1.224	0.9792
X9_P0	0.800	1.768	1.4144
X12_P0	0.800	2.448	1.9584
X24_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P0	X6_P0	X9_P0	X12_P0
A	0.0004	0.0010	0.0014	0.0018
B	0.0004	0.0008	0.0013	0.0019
C	0.0004	0.0010	0.0013	0.0017
D	0.0004	0.0008	0.0012	0.0016
	X24_P0			
A	0.0036			
B	0.0036			
C	0.0034			
D	0.0032			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X6_P0**	**X2_P0**	**X6_P0**
A to Z ↓	0.0120	0.0123	8.3554	3.1269
A to Z ↑	0.0231	0.0196	14.7417	4.7193
B to Z ↓	0.0133	0.0135	8.4051	3.1435
B to Z ↑	0.0210	0.0177	14.7047	4.8011
C to Z ↓	0.0086	0.0086	8.3620	3.1353
C to Z ↑	0.0185	0.0160	14.6427	4.6886
D to Z ↓	0.0095	0.0094	8.4313	3.1590
D to Z ↑	0.0163	0.0143	14.5926	4.8039
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0132	0.0137	2.2137	1.6653
A to Z ↑	0.0207	0.0211	3.1722	2.3842
B to Z ↓	0.0143	0.0144	2.2277	1.6754
B to Z ↑	0.0182	0.0186	3.1737	2.3612
C to Z ↓	0.0093	0.0099	2.2098	1.6654
C to Z ↑	0.0169	0.0174	3.1545	2.3574
D to Z ↓	0.0100	0.0099	2.2277	1.6806
D to Z ↑	0.0143	0.0145	3.1513	2.3632
	X24_P0		**X24_P0**	
A to Z ↓	0.0136		0.8558	
A to Z ↑	0.0207		1.2030	
B to Z ↓	0.0145		0.8615	
B to Z ↑	0.0182		1.1955	
C to Z ↓	0.0099		0.8408	
C to Z ↑	0.0174		1.1932	
D to Z ↓	0.0100		0.8484	
D to Z ↑	0.0145		1.1958	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P0	2.694e-05	1.000e-20
X6_P0	8.651e-05	1.000e-20
X9_P0	1.217e-04	1.000e-20
X12_P0	1.624e-04	1.000e-20
X24_P0	3.144e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P0	X6_P0	X9_P0	X12_P0
A (output stable)	1.319e-05	3.365e-05	6.614e-05	9.780e-05
B (output stable)	1.549e-05	4.312e-05	1.084e-04	1.726e-04
C (output stable)	3.166e-05	7.070e-05	1.280e-04	1.851e-04
D (output stable)	3.690e-05	8.549e-05	1.662e-04	2.540e-04
A to Z	7.495e-04	1.984e-03	3.109e-03	4.269e-03
B to Z	6.773e-04	1.788e-03	2.743e-03	3.768e-03
C to Z	4.857e-04	1.339e-03	2.121e-03	2.953e-03
D to Z	4.289e-04	1.189e-03	1.806e-03	2.471e-03
	X24_P0			
A (output stable)	1.786e-04			
B (output stable)	2.845e-04			
C (output stable)	3.533e-04			
D (output stable)	4.793e-04			

A to Z	8.257e-03			
B to Z	7.299e-03			
C to Z	5.769e-03			
D to Z	4.869e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

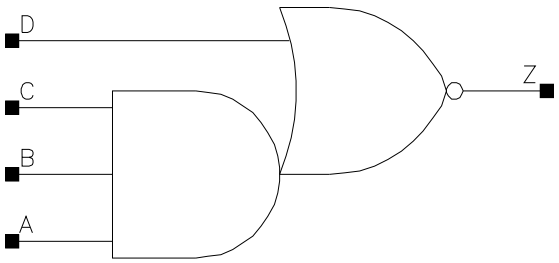
Pin Cycle (vdds)	X2_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X12_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X12_P0
A	0.0005	0.0018
B	0.0005	0.0017
C	0.0007	0.0016
D	0.0005	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X12_P0	X3_P0	X12_P0
A to Z ↓	0.0154	0.0157	8.7084	2.4252
A to Z ↑	0.0224	0.0211	9.9967	2.5966
B to Z ↓	0.0168	0.0160	8.7299	2.4311
B to Z ↑	0.0212	0.0191	10.1059	2.5965
C to Z ↓	0.0190	0.0157	8.7616	2.4359
C to Z ↑	0.0211	0.0163	10.1608	2.6091
D to Z ↓	0.0070	0.0058	3.6643	0.9937
D to Z ↑	0.0158	0.0133	8.5989	2.2143

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	4.122e-05	1.000e-20
X12_P0	1.366e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X12_P0
A (output stable)	9.457e-06	5.454e-05
B (output stable)	1.090e-05	6.637e-05
C (output stable)	2.166e-05	1.186e-04
D (output stable)	2.369e-04	7.926e-04
A to Z	1.129e-03	4.112e-03
B to Z	1.043e-03	3.564e-03
C to Z	9.926e-04	3.073e-03
D to Z	7.229e-04	2.373e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

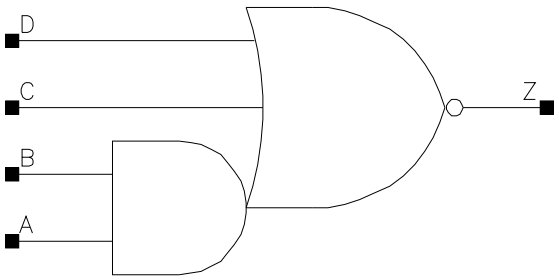
Pin Cycle (vdds)	X3_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X20_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P0	X20_P0
A	0.0004	0.0033
B	0.0004	0.0031
C	0.0005	0.0033
D	0.0005	0.0030

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X20_P0	X3_P0	X20_P0
A to Z ↓	0.0102	0.0113	6.0225	0.9672
A to Z ↑	0.0225	0.0210	14.8490	1.9203
B to Z ↓	0.0113	0.0116	6.0676	0.9757
B to Z ↑	0.0205	0.0175	14.9516	1.9204
C to Z ↓	0.0107	0.0151	3.6493	0.7639
C to Z ↑	0.0259	0.0240	14.1614	1.8208
D to Z ↓	0.0104	0.0139	3.6497	0.7623

D to Z ↑	0.0263	0.0226	14.1833	1.8254

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	3.401e-05	1.000e-20
X20_P0	2.010e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X20_P0
A (output stable)	5.625e-05	3.832e-04
B (output stable)	6.056e-05	4.076e-04
C (output stable)	2.724e-05	2.961e-04
D (output stable)	3.542e-05	3.818e-04
A to Z	7.994e-04	5.457e-03
B to Z	7.283e-04	4.615e-03
C to Z	1.146e-03	8.176e-03
D to Z	1.035e-03	6.747e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

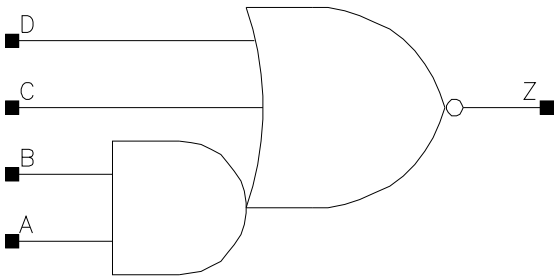
Pin Cycle (vdds)	X3_P0	X20_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.816	0.6528
X10_P0	0.800	2.448	1.9584
X19_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P0	X10_P0	X19_P0
A	0.0005	0.0017	0.0035
B	0.0004	0.0016	0.0033
C	0.0005	0.0015	0.0029
D	0.0004	0.0014	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	X10_P0	X2_P0	X10_P0
A to Z ↓	0.0133	0.0134	7.2140	1.9064
A to Z ↑	0.0265	0.0242	15.7515	3.8240
B to Z ↓	0.0149	0.0140	7.2544	1.9181
B to Z ↑	0.0243	0.0209	15.7998	3.8347
C to Z ↓	0.0124	0.0112	6.3994	1.6074
C to Z ↑	0.0204	0.0179	14.9611	3.6258

D to Z ↓	0.0107	0.0086	6.4297	1.6186
D to Z ↑	0.0191	0.0154	14.9533	3.6294
	X19_P0		**X19_P0**	
A to Z ↓	0.0131		0.9745	
A to Z ↑	0.0235		1.9376	
B to Z ↓	0.0139		0.9808	
B to Z ↑	0.0202		1.9368	
C to Z ↓	0.0116		0.8454	
C to Z ↑	0.0172		1.8350	
D to Z ↓	0.0089		0.8517	
D to Z ↑	0.0146		1.8372	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P0	2.736e-05	1.000e-20
X10_P0	1.101e-04	1.000e-20
X19_P0	2.158e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P0	X10_P0	X19_P0
A (output stable)	1.314e-05	5.560e-05	1.097e-04
B (output stable)	1.280e-05	7.366e-05	1.365e-04
C (output stable)	3.336e-05	1.632e-04	3.256e-04
D (output stable)	7.420e-05	3.723e-04	7.133e-04
A to Z	1.064e-03	3.957e-03	7.593e-03
B to Z	9.815e-04	3.443e-03	6.645e-03
C to Z	7.041e-04	2.672e-03	5.048e-03
D to Z	6.065e-04	2.053e-03	3.837e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

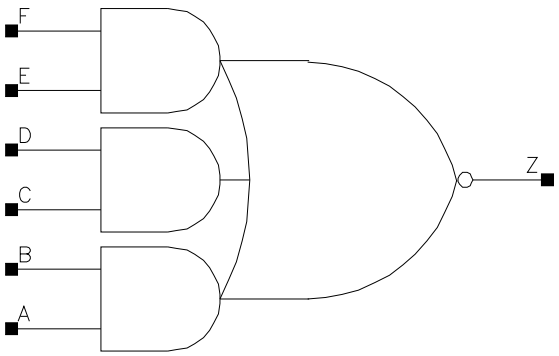
Pin Cycle (vdds)	X2_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.088	0.8704
X5_P0	0.800	2.040	1.6320
X7_P0	0.800	2.720	2.1760
X9_P0	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P0	X5_P0	X7_P0	X9_P0
A	0.0004	0.0008	0.0013	0.0017

B	0.0004	0.0009	0.0012	0.0016
C	0.0004	0.0008	0.0012	0.0019
D	0.0004	0.0009	0.0011	0.0016
E	0.0006	0.0009	0.0012	0.0015
F	0.0004	0.0007	0.0011	0.0015

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X5_P0**	**X2_P0**	**X5_P0**
A to Z ↓	0.0145	0.0179	6.3763	3.6483
A to Z ↑	0.0342	0.0319	15.2530	6.8858
B to Z ↓	0.0162	0.0199	6.4141	3.6596
B to Z ↑	0.0317	0.0304	15.3016	6.8401
C to Z ↓	0.0135	0.0162	6.4329	3.6312
C to Z ↑	0.0300	0.0286	15.3271	6.8992
D to Z ↓	0.0150	0.0180	6.4819	3.6470
D to Z ↑	0.0276	0.0272	15.3078	6.8690
E to Z ↓	0.0105	0.0127	6.4543	3.5823
E to Z ↑	0.0240	0.0236	15.2425	6.8269
F to Z ↓	0.0112	0.0137	6.5167	3.6011
F to Z ↑	0.0209	0.0213	15.1928	6.8434
	X7_P0	**X9_P0**	**X7_P0**	**X9_P0**
A to Z ↓	0.0175	0.0179	2.5206	1.9165
A to Z ↑	0.0309	0.0317	4.5311	3.4220
B to Z ↓	0.0188	0.0190	2.5302	1.9239
B to Z ↑	0.0284	0.0289	4.6081	3.4628
C to Z ↓	0.0158	0.0164	2.5304	1.9060
C to Z ↑	0.0278	0.0292	4.6016	3.4656
D to Z ↓	0.0172	0.0168	2.5433	1.9138
D to Z ↑	0.0251	0.0254	4.5703	3.4425
E to Z ↓	0.0118	0.0118	2.5265	1.9060
E to Z ↑	0.0221	0.0222	4.5410	3.4328
F to Z ↓	0.0128	0.0121	2.5454	1.9207
F to Z ↑	0.0195	0.0190	4.5684	3.4277

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P0	4.686e-05	1.000e-20
X5_P0	9.725e-05	1.000e-20
X7_P0	1.412e-04	1.000e-20
X9_P0	1.807e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

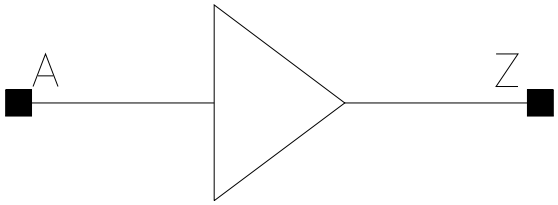
Pin Cycle (vdd)	X2_P0	X5_P0	X7_P0	X9_P0
A (output stable)	2.173e-05	4.064e-05	7.225e-05	1.011e-04
B (output stable)	2.325e-05	5.040e-05	9.263e-05	1.471e-04
C (output stable)	3.550e-05	6.666e-05	9.791e-05	1.415e-04
D (output stable)	3.932e-05	7.522e-05	1.254e-04	1.805e-04
E (output stable)	6.439e-05	1.395e-04	2.082e-04	3.063e-04
F (output stable)	7.832e-05	1.473e-04	2.326e-04	3.469e-04

A to Z	1.428e-03	2.929e-03	4.238e-03	5.785e-03
B to Z	1.332e-03	2.815e-03	3.893e-03	5.272e-03
C to Z	1.103e-03	2.336e-03	3.355e-03	4.561e-03
D to Z	1.019e-03	2.228e-03	3.053e-03	4.112e-03
E to Z	7.661e-04	1.768e-03	2.427e-03	3.209e-03
F to Z	6.930e-04	1.626e-03	2.154e-03	2.783e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X2_P0	X5_P0	X7_P0	X9_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.544	0.4352
X5_P0	0.800	0.544	0.4352
X9_P0	0.800	0.680	0.5440
X11_P0	1.600	0.408	0.6528
X13_P0	0.800	0.680	0.5440
X19_P0	0.800	0.952	0.7616
X23_P0	1.600	0.544	0.8704
X24_P0	0.800	1.088	0.8704
X29_P0	0.800	1.224	0.9792
X34_P0	1.600	0.680	1.0880
X38_P0	0.800	1.632	1.3056
X46_P0	1.600	0.952	1.5232
X57_P0	0.800	2.312	1.8496
X68_P0	1.600	1.224	1.9584
X91_P0	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P0	X5_P0	X9_P0	X11_P0
A	0.0005	0.0005	0.0005	0.0007
	X13_P0	X19_P0	X23_P0	X24_P0
A	0.0006	0.0008	0.0010	0.0010
	X29_P0	X34_P0	X38_P0	X46_P0
A	0.0011	0.0013	0.0017	0.0017
	X57_P0	X68_P0	X91_P0	
A	0.0022	0.0023	0.0031	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X5_P0**	**X2_P0**	**X5_P0**
A to Z ↓	0.0241	0.0244	7.2261	3.7271
A to Z ↑	0.0188	0.0184	10.3806	5.4065
	X9_P0	**X11_P0**	**X9_P0**	**X11_P0**
A to Z ↓	0.0287	0.0267	1.9027	1.3857
A to Z ↑	0.0218	0.0192	2.6909	2.5315
	X13_P0	**X19_P0**	**X13_P0**	**X19_P0**
A to Z ↓	0.0251	0.0253	1.3003	0.9189
A to Z ↑	0.0201	0.0188	1.8533	1.3059
	X23_P0	**X24_P0**	**X23_P0**	**X24_P0**
A to Z ↓	0.0253	0.0248	0.6705	0.7482
A to Z ↑	0.0181	0.0193	1.2722	1.0470
	X29_P0	**X34_P0**	**X29_P0**	**X34_P0**
A to Z ↓	0.0236	0.0249	0.6201	0.4605
A to Z ↑	0.0188	0.0184	0.8787	0.8672
	X38_P0	**X46_P0**	**X38_P0**	**X46_P0**
A to Z ↓	0.0232	0.0244	0.4688	0.3467
A to Z ↑	0.0186	0.0177	0.6489	0.6532
	X57_P0	**X68_P0**	**X57_P0**	**X68_P0**
A to Z ↓	0.0241	0.0241	0.3149	0.2350
A to Z ↑	0.0193	0.0178	0.4350	0.4369
	X91_P0		**X91_P0**	
A to Z ↓	0.0255		0.1808	
A to Z ↑	0.0187		0.3283	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P0	2.479e-05	1.000e-20
X5_P0	4.110e-05	1.000e-20
X9_P0	7.048e-05	1.000e-20
X11_P0	9.148e-05	1.000e-20
X13_P0	1.086e-04	1.000e-20
X19_P0	1.390e-04	1.000e-20
X23_P0	1.798e-04	1.000e-20
X24_P0	1.748e-04	1.000e-20
X29_P0	2.119e-04	1.000e-20
X34_P0	2.564e-04	1.000e-20
X38_P0	2.862e-04	1.000e-20
X46_P0	3.292e-04	1.000e-20
X57_P0	4.102e-04	1.000e-20
X68_P0	4.880e-04	1.000e-20
X91_P0	6.234e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P0	X5_P0	X9_P0	X11_P0
A to Z	8.831e-04	1.139e-03	1.852e-03	2.214e-03
	X13_P0	X19_P0	X23_P0	X24_P0
A to Z	2.687e-03	3.640e-03	4.065e-03	4.527e-03
	X29_P0	X34_P0	X38_P0	X46_P0

A to Z	5.247e-03	6.073e-03	7.193e-03	7.794e-03
	X57_P0	X68_P0	X91_P0	
A to Z	1.064e-02	1.154e-02	1.562e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

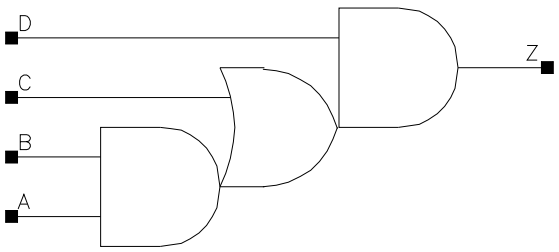
Pin Cycle (vdds)	X2_P0	X5_P0	X9_P0	X11_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P0	X19_P0	X23_P0	X24_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P0	X34_P0	X38_P0	X46_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P0	X68_P0	X91_P0	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.952	0.7616
X10_P0	0.800	1.632	1.3056
X14_P0	0.800	1.768	1.4144
X19_P0	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0005	0.0011	0.0011	0.0011
B	0.0006	0.0010	0.0010	0.0010
C	0.0006	0.0013	0.0013	0.0013
D	0.0009	0.0011	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0314	0.0285	3.8045	1.7938
A to Z ↑	0.0302	0.0273	5.5260	2.6264
B to Z ↓	0.0296	0.0266	3.7961	1.7928
B to Z ↑	0.0311	0.0278	5.5236	2.6254
C to Z ↓	0.0274	0.0246	3.7889	1.7898
C to Z ↑	0.0226	0.0200	5.4705	2.5988

D to Z ↓	0.0264	0.0224	3.7654	1.7776
D to Z ↑	0.0260	0.0218	5.4831	2.6041
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0318	0.0339	1.2455	0.9354
A to Z ↑	0.0304	0.0324	1.7659	1.3228
B to Z ↓	0.0300	0.0322	1.2434	0.9340
B to Z ↑	0.0310	0.0331	1.7645	1.3244
C to Z ↓	0.0277	0.0299	1.2404	0.9309
C to Z ↑	0.0225	0.0241	1.7416	1.3063
D to Z ↓	0.0245	0.0257	1.2279	0.9200
D to Z ↑	0.0242	0.0256	1.7452	1.3089

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	6.583e-05	1.000e-20
X10_P0	1.316e-04	1.000e-20
X14_P0	1.587e-04	1.000e-20
X19_P0	1.859e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	2.500e-05	4.707e-05	4.799e-05	4.826e-05
B (output stable)	3.049e-05	5.619e-05	5.737e-05	5.748e-05
C (output stable)	1.074e-04	1.733e-04	1.744e-04	1.754e-04
D (output stable)	5.880e-05	8.933e-05	9.049e-05	9.081e-05
A to Z	1.843e-03	3.367e-03	4.400e-03	5.327e-03
B to Z	1.762e-03	3.164e-03	4.194e-03	5.119e-03
C to Z	1.538e-03	2.707e-03	3.649e-03	4.474e-03
D to Z	1.879e-03	3.296e-03	4.196e-03	4.949e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

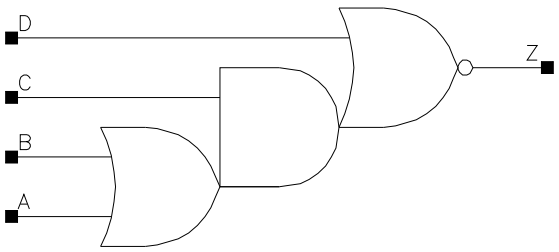
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X6_P0	0.800	1.496	1.1968
X9_P0	0.800	1.768	1.4144
X12_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X9_P0	X12_P0
A	0.0005	0.0009	0.0014	0.0018
B	0.0005	0.0009	0.0014	0.0018
C	0.0005	0.0009	0.0013	0.0017
D	0.0006	0.0009	0.0012	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X6_P0**	**X3_P0**	**X6_P0**
A to Z ↓	0.0137	0.0124	6.2411	3.1899
A to Z ↑	0.0277	0.0270	14.9147	7.7813
B to Z ↓	0.0131	0.0123	6.0906	3.2073
B to Z ↑	0.0278	0.0262	14.9204	7.7890
C to Z ↓	0.0124	0.0115	5.7584	2.9843
C to Z ↑	0.0179	0.0167	10.2011	5.2422

D to Z ↓	0.0072	0.0054	3.6934	1.8824
D to Z ↑	0.0177	0.0150	10.8361	5.5898
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0124	0.0128	2.1899	1.6941
A to Z ↑	0.0248	0.0263	5.0496	3.8748
B to Z ↓	0.0119	0.0121	2.2073	1.6931
B to Z ↑	0.0250	0.0255	5.0554	3.8799
C to Z ↓	0.0117	0.0117	2.0602	1.5811
C to Z ↑	0.0159	0.0161	3.4316	2.6042
D to Z ↓	0.0056	0.0056	1.3059	0.9977
D to Z ↑	0.0140	0.0138	3.6479	2.7776

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	4.035e-05	1.000e-20
X6_P0	7.651e-05	1.000e-20
X9_P0	1.066e-04	1.000e-20
X12_P0	1.398e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	1.083e-05	2.681e-05	3.217e-05	5.511e-05
B (output stable)	1.266e-05	2.972e-05	4.039e-05	7.141e-05
C (output stable)	3.848e-05	8.611e-05	1.166e-04	1.600e-04
D (output stable)	1.287e-04	3.428e-04	4.700e-04	7.154e-04
A to Z	1.156e-03	2.184e-03	3.024e-03	4.202e-03
B to Z	1.035e-03	1.858e-03	2.679e-03	3.590e-03
C to Z	8.813e-04	1.606e-03	2.291e-03	3.116e-03
D to Z	6.822e-04	1.166e-03	1.637e-03	2.150e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

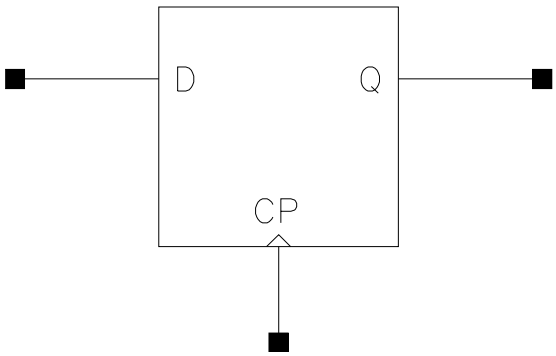
Pin Cycle (vdds)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	1.600	1.496	2.3936
X19_P0	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P0	X19_P0
CP	0.0007	0.0007
D	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	X19_P0	X10_P0	X19_P0
CP to Q ↓	0.0469	0.0631	1.8503	0.9928
CP to Q ↑	0.0557	0.0639	2.5949	1.3289

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P0	X19_P0
CP ↓	min_pulse_width to CP	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0411	0.0565
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0224	0.0224
D ↑	setup_rising to CP	0.0141	0.0141

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P0	1.944e-04	1.000e-20
X19_P0	2.446e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

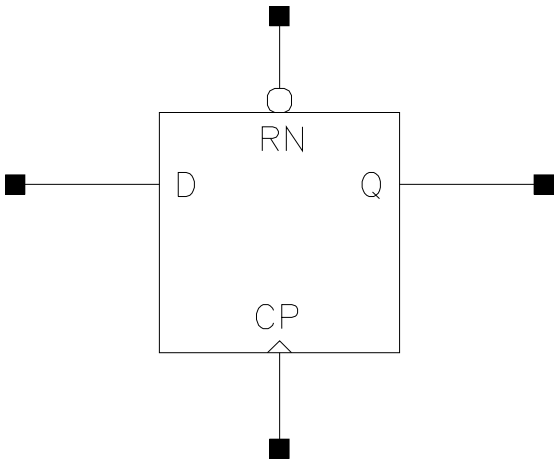
Pin Cycle	X10_P0	X19_P0
Clock 100Mhz Data 0Mhz	5.835e-03	5.840e-03
Clock 100Mhz Data 25Mhz	7.140e-03	8.769e-03
Clock 100Mhz Data 50Mhz	8.446e-03	1.170e-02
Clock = 0 Data 100Mhz	2.298e-03	2.299e-03
Clock = 1 Data 100Mhz	1.538e-05	1.562e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	1.600	1.768	2.8288
X19_P0	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P0	X19_P0
CP	0.0007	0.0007
D	0.0006	0.0006
RN	0.0007	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	X19_P0	X10_P0	X19_P0
CP to Q ↓	0.0513	0.0652	1.8758	0.9811
CP to Q ↑	0.0582	0.0660	2.5879	1.3166
RN to Q ↓	0.0529	0.0671	1.8403	0.9453

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P0	X19_P0
CP ↓	min_pulse_width to CP	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0410	0.0551
D ↓	hold_rising to CP	0.0178	0.0173
D ↑	hold_rising to CP	0.0107	0.0107
D ↓	setup_rising to CP	0.0198	0.0224
D ↑	setup_rising to CP	0.0200	0.0200
RN ↓	min_pulse_width to RN	0.0637	0.0806
RN ↑	recovery_rising to CP	0.0076	0.0076
RN ↑	removal_rising to CP	-0.0033	-0.0033

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P0	2.233e-04	1.000e-20
X19_P0	2.867e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

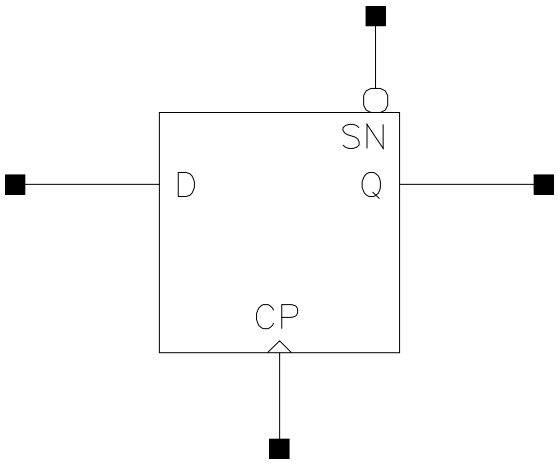
Pin Cycle	X10_P0	X19_P0
Clock 100Mhz Data 0Mhz	5.916e-03	5.916e-03
Clock 100Mhz Data 25Mhz	7.347e-03	8.950e-03
Clock 100Mhz Data 50Mhz	8.778e-03	1.198e-02
Clock = 0 Data 100Mhz	2.296e-03	2.297e-03
Clock = 1 Data 100Mhz	1.552e-05	1.557e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	1.600	1.768	2.8288
X19_P0	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P0	X19_P0
CP	0.0007	0.0007
D	0.0006	0.0006
SN	0.0009	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	X19_P0	X10_P0	X19_P0
CP to Q ↓	0.0482	0.0635	1.8601	0.9750
CP to Q ↑	0.0576	0.0661	2.5830	1.3183
SN to Q ↑	0.0354	0.0401	2.5381	1.2841

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P0	X19_P0
CP ↓	min_pulse_width to CP	0.0491	0.0491
CP ↑	min_pulse_width to CP	0.0411	0.0551
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0224	0.0224
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0398	0.0425
SN ↑	recovery_rising to CP	-0.0017	0.0010
SN ↑	removal_rising to CP	0.0281	0.0313

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P0	2.260e-04	1.000e-20
X19_P0	2.817e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

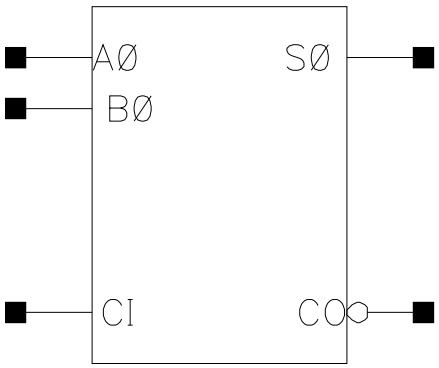
Pin Cycle	X10_P0	X19_P0
Clock 100Mhz Data 0Mhz	5.805e-03	5.808e-03
Clock 100Mhz Data 25Mhz	7.178e-03	8.839e-03
Clock 100Mhz Data 50Mhz	8.550e-03	1.187e-02
Clock = 0 Data 100Mhz	2.198e-03	2.198e-03
Clock = 1 Data 100Mhz	1.561e-05	1.561e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_P0	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_P0	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_P0	1.600	2.720	4.3520
C8T28SOIDV_LLS1_FA1X4_P0	1.600	2.040	3.2640
C8T28SOIDV_LLS1_FA1X9_P0	1.600	3.128	5.0048
C8T28SOIDV_LLS1_FA1X18_P0	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P0	C8T28SOIDV_LL_-FA1X9_P0	C8T28SOIDV_LL_-FA1X14_P0	C8T28SOIDV_LL_-FA1X19_P0
A0	0.0019	0.0020	0.0032	0.0034
B0	0.0016	0.0017	0.0029	0.0031
CI	0.0012	0.0012	0.0022	0.0024
	C8T28SOIDV_LLS1_-FA1X4_P0	C8T28SOIDV_LLS1_-FA1X9_P0	C8T28SOIDV_LLS1_-FA1X18_P0	
A0	0.0019	0.0025	0.0027	
B0	0.0018	0.0029	0.0032	
CI	0.0014	0.0021	0.0024	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P0	**C8T28SOIDV_LL_-FA1X9_P0**	**C8T28SOIDV_LL_-FA1X5_P0**	**C8T28SOIDV_LL_-FA1X9_P0**
A0 to CO ↓	0.0412	0.0439	3.8528	1.9773
A0 to CO ↑	0.0315	0.0335	5.1375	2.6269
A0 to S0 ↓	0.0450	0.0485	3.8107	1.9613
A0 to S0 ↑	0.0468	0.0498	5.1448	2.5842
B0 to CO ↓	0.0412	0.0441	3.8623	1.9859
B0 to CO ↑	0.0325	0.0345	5.1381	2.6287
B0 to S0 ↓	0.0455	0.0491	3.8124	1.9630
B0 to S0 ↑	0.0474	0.0507	5.1478	2.5856
CI to CO ↓	0.0391	0.0416	3.8597	1.9828
CI to CO ↑	0.0318	0.0336	5.1305	2.6236
CI to S0 ↓	0.0451	0.0488	3.8117	1.9628
CI to S0 ↑	0.0470	0.0502	5.1440	2.5862
	C8T28SOIDV_LL_-FA1X14_P0	**C8T28SOIDV_LL_-FA1X19_P0**	**C8T28SOIDV_LL_-FA1X14_P0**	**C8T28SOIDV_LL_-FA1X19_P0**
A0 to CO ↓	0.0418	0.0457	1.2809	0.9748
A0 to CO ↑	0.0319	0.0330	1.7966	1.3428
A0 to S0 ↓	0.0515	0.0517	1.2774	0.9505
A0 to S0 ↑	0.0534	0.0546	1.7448	1.3028
B0 to CO ↓	0.0410	0.0449	1.2836	0.9766
B0 to CO ↑	0.0323	0.0333	1.7957	1.3416
B0 to S0 ↓	0.0518	0.0520	1.2774	0.9515
B0 to S0 ↑	0.0537	0.0548	1.7464	1.3044
CI to CO ↓	0.0390	0.0427	1.2807	0.9745
CI to CO ↑	0.0315	0.0325	1.7949	1.3412
CI to S0 ↓	0.0511	0.0515	1.2770	0.9512
CI to S0 ↑	0.0527	0.0541	1.7458	1.3036
	C8T28SOIDV_-LLS1_FA1X4_P0	**C8T28SOIDV_-LLS1_FA1X9_P0**	**C8T28SOIDV_-LLS1_FA1X4_P0**	**C8T28SOIDV_-LLS1_FA1X9_P0**
A0 to CO ↓	0.0282	0.0257	7.3715	2.3724
A0 to CO ↑	0.0251	0.0237	5.1804	2.6209
A0 to S0 ↓	0.0610	0.0660	4.0861	1.4379
A0 to S0 ↑	0.0579	0.0569	5.4534	2.5702
B0 to CO ↓	0.0267	0.0265	7.3611	2.3739
B0 to CO ↑	0.0215	0.0224	5.1653	2.6197
B0 to S0 ↓	0.0619	0.0688	4.0866	1.4376
B0 to S0 ↑	0.0589	0.0597	5.4541	2.5710
CI to CO ↓	0.0272	0.0368	7.3628	2.3885
CI to CO ↑	0.0233	0.0215	5.1833	2.6381

CI to S0 ↓	0.0343	0.0402	4.0914	1.4399
CI to S0 ↑	0.0306	0.0306	5.4538	2.5716
	C8T28SOIDV_-LLS1_FA1X18_P0		**C8T28SOIDV_-LLS1_FA1X18_P0**	
A0 to CO ↓	0.0326		1.2384	
A0 to CO ↑	0.0245		1.2873	
A0 to S0 ↓	0.0695		0.7415	
A0 to S0 ↑	0.0571		1.2881	
B0 to CO ↓	0.0339		1.2392	
B0 to CO ↑	0.0232		1.2865	
B0 to S0 ↓	0.0708		0.7413	
B0 to S0 ↑	0.0585		1.2882	
CI to CO ↓	0.0455		1.2480	
CI to CO ↑	0.0256		1.2893	
CI to S0 ↓	0.0408		0.7417	
CI to S0 ↑	0.0278		1.2883	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P0	1.570e-04	1.000e-20
C8T28SOIDV_LL_FA1X9_P0	2.170e-04	1.000e-20
C8T28SOIDV_LL_FA1X14_P0	3.226e-04	1.000e-20
C8T28SOIDV_LL_FA1X19_P0	4.037e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P0	3.459e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P0	5.122e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P0	7.774e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P0	C8T28SOIDV_LL_-FA1X9_P0	C8T28SOIDV_LL_-FA1X14_P0	C8T28SOIDV_LL_-FA1X19_P0
A0 to CO	2.044e-03	2.948e-03	4.843e-03	5.972e-03
A0 to S0	2.076e-03	2.880e-03	4.942e-03	6.065e-03
B0 to CO	2.062e-03	2.987e-03	4.876e-03	6.032e-03
B0 to S0	2.060e-03	2.881e-03	4.929e-03	6.054e-03
CI to CO	2.063e-03	2.967e-03	4.931e-03	6.117e-03
CI to S0	2.059e-03	2.884e-03	4.932e-03	6.054e-03
	C8T28SOIDV_LLS1_-FA1X4_P0	C8T28SOIDV_LLS1_-FA1X9_P0	C8T28SOIDV_LLS1_-FA1X18_P0	
A0 to CO	3.171e-03	4.895e-03	7.824e-03	
A0 to S0	4.287e-03	6.326e-03	9.738e-03	
B0 to CO	3.358e-03	4.965e-03	7.853e-03	
B0 to S0	4.606e-03	6.471e-03	9.838e-03	
CI to CO	2.294e-03	4.052e-03	6.945e-03	
CI to S0	2.586e-03	4.506e-03	7.505e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P0	C8T28SOIDV_LL_-FA1X9_P0	C8T28SOIDV_LL_-FA1X14_P0	C8T28SOIDV_LL_-FA1X19_P0
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P0	C8T28SOIDV_LLS1_-FA1X9_P0	C8T28SOIDV_LLS1_-FA1X18_P0	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P0	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P0	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P0	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P0	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P0	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P0	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P0	C8T28SOI_LL_-HA1X9_P0	C8T28SOI_LLS1_-HA1X5_P0	C8T28SOIDV_LL_-HA1X14_P0
A0	0.0006	0.0009	0.0011	0.0013
B0	0.0006	0.0010	0.0010	0.0011
	C8T28SOIDV_LL_-HA1X19_P0	C8T28SOIDV_LLS1_-HA1X11_P0		
A0	0.0015	0.0016		
B0	0.0013	0.0016		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P0	**C8T28SOI_LL_-HA1X9_P0**	**C8T28SOI_LL_-HA1X5_P0**	**C8T28SOI_LL_-HA1X9_P0**
A0 to CO ↓	0.0327	0.0271	3.8278	1.8726
A0 to CO ↑	0.0312	0.0263	5.4981	2.6362
A0 to S0 ↓	0.0423	0.0374	3.6872	1.8579
A0 to S0 ↑	0.0401	0.0358	5.3561	2.6306
B0 to CO ↓	0.0320	0.0266	3.8307	1.8738
B0 to CO ↑	0.0333	0.0285	5.4980	2.6365
B0 to S0 ↓	0.0438	0.0383	3.6871	1.8579
B0 to S0 ↑	0.0397	0.0353	5.3513	2.6319
	C8T28SOI_LLS1_-HA1X5_P0	**C8T28SOIDV_LL_-HA1X14_P0**	**C8T28SOI_LLS1_-HA1X5_P0**	**C8T28SOIDV_LL_-HA1X14_P0**
A0 to CO ↓	0.0261	0.0281	3.7602	1.2572
A0 to CO ↑	0.0246	0.0258	5.4344	1.7661
A0 to S0 ↓	0.0369	0.0418	3.7458	1.2667
A0 to S0 ↑	0.0419	0.0397	5.4695	1.7437
B0 to CO ↓	0.0250	0.0261	3.7582	1.2530
B0 to CO ↑	0.0261	0.0265	5.4322	1.7657
B0 to S0 ↓	0.0388	0.0414	3.7481	1.2664
B0 to S0 ↑	0.0415	0.0380	5.4686	1.7439
	C8T28SOIDV_LL_-HA1X19_P0	**C8T28SOIDV_-LLS1_HA1X11_P0**	**C8T28SOIDV_LL_-HA1X19_P0**	**C8T28SOIDV_-LLS1_HA1X11_P0**
A0 to CO ↓	0.0259	0.0248	0.9199	1.3108
A0 to CO ↑	0.0246	0.0261	1.3343	2.5957
A0 to S0 ↓	0.0378	0.0322	0.9143	1.3306
A0 to S0 ↑	0.0364	0.0345	1.3087	2.6198
B0 to CO ↓	0.0242	0.0236	0.9179	1.3100
B0 to CO ↑	0.0256	0.0279	1.3348	2.5956
B0 to S0 ↓	0.0381	0.0333	0.9148	1.3283
B0 to S0 ↑	0.0350	0.0344	1.3095	2.6176

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_HA1X5_P0	8.895e-05	1.000e-20
C8T28SOI_LL_HA1X9_P0	2.015e-04	1.000e-20
C8T28SOI_LLS1_HA1X5_P0	1.094e-04	1.000e-20
C8T28SOIDV_LL_HA1X14_P0	2.899e-04	1.000e-20
C8T28SOIDV_LL_HA1X19_P0	4.033e-04	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P0	2.711e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

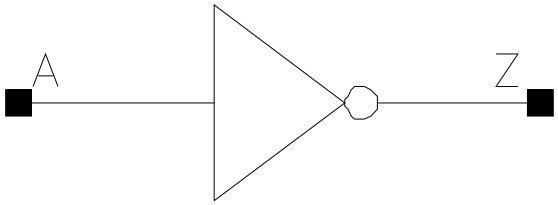
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P0	C8T28SOI_LL_-HA1X9_P0	C8T28SOI_LLS1_-HA1X5_P0	C8T28SOIDV_LL_-HA1X14_P0
A0 to CO	1.549e-03	2.499e-03	1.853e-03	4.044e-03
A0 to S0	1.415e-03	2.449e-03	1.656e-03	4.149e-03
B0 to CO	1.571e-03	2.604e-03	1.890e-03	4.063e-03
B0 to S0	1.404e-03	2.419e-03	1.631e-03	4.055e-03
	C8T28SOIDV_LL_-HA1X19_P0	C8T28SOIDV_LLS1_-HA1X11_P0		
A0 to CO	4.884e-03	3.559e-03		
A0 to S0	4.992e-03	3.281e-03		

B0 to CO	4.902e-03	3.311e-03		
B0 to S0	4.906e-03	3.340e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P0	C8T28SOI_LL_-HA1X9_P0	C8T28SOI_LLS1_-HA1X5_P0	C8T28SOIDV_LL_-HA1X14_P0
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P0	C8T28SOIDV_LLS1_-HA1X11_P0		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P0	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P0	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P0	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P0	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P0	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P0	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P0	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P0	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P0	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P0	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P0	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P0	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P0	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P0	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P0	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P0	C8T28SOI_LL_IVX3_-P0	C8T28SOI_LL_IVX5_-P0	C8T28SOI_LL_-IVX10_P0

A	0.0003	0.0004	0.0005	0.0009
	C8T28SOI_LL_-IVX14_P0	C8T28SOI_LL_-IVX19_P0	C8T28SOI_LL_-IVX29_P0	C8T28SOI_LL_-IVX34_P0
A	0.0013	0.0017	0.0026	0.0030
	C8T28SOI_LL_-IVX38_P0	C8T28SOIDV_LL_-IVX11_P0	C8T28SOIDV_LL_-IVX23_P0	C8T28SOIDV_LL_-IVX34_P0
A	0.0034	0.0010	0.0019	0.0027
	C8T28SOIDV_LL_-IVX46_P0	C8T28SOIDV_LL_-IVX68_P0	C8T28SOIDV_LL_-IVX91_P0	
A	0.0037	0.0056	0.0078	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P0	**C8T28SOI_LL_-IVX3_P0**	**C8T28SOI_LL_-IVX2_P0**	**C8T28SOI_LL_-IVX3_P0**
A to Z ↓	0.0067	0.0063	7.4159	5.6348
A to Z ↑	0.0130	0.0117	10.5976	7.9860
	C8T28SOI_LL_-IVX5_P0	**C8T28SOI_LL_-IVX10_P0**	**C8T28SOI_LL_-IVX5_P0**	**C8T28SOI_LL_-IVX10_P0**
A to Z ↓	0.0057	0.0043	3.8263	1.8311
A to Z ↑	0.0104	0.0086	5.5273	2.6281
	C8T28SOI_LL_-IVX14_P0	**C8T28SOI_LL_-IVX19_P0**	**C8T28SOI_LL_-IVX14_P0**	**C8T28SOI_LL_-IVX19_P0**
A to Z ↓	0.0045	0.0049	1.2643	0.9639
A to Z ↑	0.0086	0.0088	1.7663	1.3511
	C8T28SOI_LL_-IVX29_P0	**C8T28SOI_LL_-IVX34_P0**	**C8T28SOI_LL_-IVX29_P0**	**C8T28SOI_LL_-IVX34_P0**
A to Z ↓	0.0048	0.0045	0.6459	0.5513
A to Z ↑	0.0085	0.0081	0.8949	0.7645
	C8T28SOI_LL_-IVX38_P0	**C8T28SOIDV_LL_-IVX11_P0**	**C8T28SOI_LL_-IVX38_P0**	**C8T28SOIDV_LL_-IVX11_P0**
A to Z ↓	0.0047	0.0041	0.4880	1.4185
A to Z ↑	0.0083	0.0102	0.6767	2.6698
	C8T28SOIDV_LL_-IVX23_P0	**C8T28SOIDV_LL_-IVX34_P0**	**C8T28SOIDV_LL_-IVX23_P0**	**C8T28SOIDV_LL_-IVX34_P0**
A to Z ↓	0.0032	0.0037	0.6922	0.4732
A to Z ↑	0.0090	0.0092	1.3013	0.8726
	C8T28SOIDV_LL_-IVX46_P0	**C8T28SOIDV_LL_-IVX68_P0**	**C8T28SOIDV_LL_-IVX46_P0**	**C8T28SOIDV_LL_-IVX68_P0**
A to Z ↓	0.0035	0.0036	0.3567	0.2429
A to Z ↑	0.0089	0.0087	0.6540	0.4387
	C8T28SOIDV_LL_-IVX91_P0		**C8T28SOIDV_LL_-IVX91_P0**	
A to Z ↓	0.0040		0.1875	
A to Z ↑	0.0090		0.3329	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_IVX2_P0	1.298e-05	1.000e-20
C8T28SOI_LL_IVX3_P0	1.849e-05	1.000e-20
C8T28SOI_LL_IVX5_P0	2.790e-05	1.000e-20
C8T28SOI_LL_IVX10_P0	5.926e-05	1.000e-20

C8T28SOI_LL_IVX14_P0	8.438e-05	1.000e-20
C8T28SOI_LL_IVX19_P0	1.091e-04	1.000e-20
C8T28SOI_LL_IVX29_P0	1.586e-04	1.000e-20
C8T28SOI_LL_IVX34_P0	1.834e-04	1.000e-20
C8T28SOI_LL_IVX38_P0	2.081e-04	1.000e-20
C8T28SOIDV_LL_IVX11_P0	6.976e-05	1.000e-20
C8T28SOIDV_LL_IVX23_P0	1.395e-04	1.000e-20
C8T28SOIDV_LL_IVX34_P0	2.002e-04	1.000e-20
C8T28SOIDV_LL_IVX46_P0	2.598e-04	1.000e-20
C8T28SOIDV_LL_IVX68_P0	3.787e-04	1.000e-20
C8T28SOIDV_LL_IVX91_P0	4.977e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P0	C8T28SOI_LL_IVX3_-P0	C8T28SOI_LL_IVX5_-P0	C8T28SOI_LL_-IVX10_P0
A to Z	3.192e-04	3.966e-04	5.142e-04	9.790e-04
	C8T28SOI_LL_-IVX14_P0	C8T28SOI_LL_-IVX19_P0	C8T28SOI_LL_-IVX29_P0	C8T28SOI_LL_-IVX34_P0
A to Z	1.489e-03	2.007e-03	2.926e-03	3.312e-03
	C8T28SOI_LL_-IVX38_P0	C8T28SOIDV_LL_-IVX11_P0	C8T28SOIDV_LL_-IVX23_P0	C8T28SOIDV_LL_-IVX34_P0
A to Z	3.821e-03	1.156e-03	2.163e-03	3.272e-03
	C8T28SOIDV_LL_-IVX46_P0	C8T28SOIDV_LL_-IVX68_P0	C8T28SOIDV_LL_-IVX91_P0	
A to Z	4.194e-03	6.209e-03	8.311e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

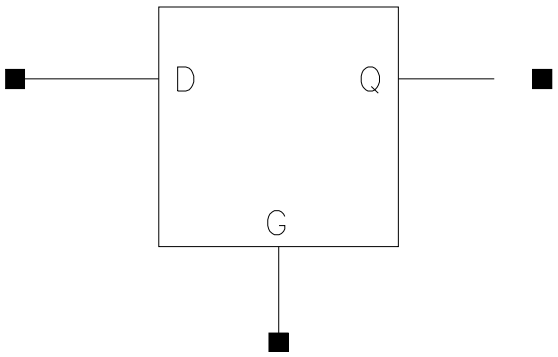
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P0	C8T28SOI_LL_IVX3_-P0	C8T28SOI_LL_IVX5_-P0	C8T28SOI_LL_-IVX10_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P0	C8T28SOI_LL_-IVX19_P0	C8T28SOI_LL_-IVX29_P0	C8T28SOI_LL_-IVX34_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P0	C8T28SOIDV_LL_-IVX11_P0	C8T28SOIDV_LL_-IVX23_P0	C8T28SOIDV_LL_-IVX34_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P0	C8T28SOIDV_LL_-IVX68_P0	C8T28SOIDV_LL_-IVX91_P0	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.360	1.0880
X9_P0	1.600	0.952	1.5232
X19_P0	1.600	1.224	1.9584
X28_P0	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0	X28_P0
D	0.0003	0.0006	0.0008	0.0013
G	0.0008	0.0008	0.0015	0.0015

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D to Q ↓	0.0466	0.0445	3.8563	1.9189
D to Q ↑	0.0267	0.0318	5.2985	2.5867
G to Q ↓	0.0501	0.0471	3.8472	1.9150

G to Q ↑	0.0260	0.0294	5.3075	2.5901
	X19_P0	**X28_P0**	**X19_P0**	**X28_P0**
D to Q ↓	0.0355	0.0375	0.9228	0.6222
D to Q ↑	0.0268	0.0271	1.3043	0.8732
G to Q ↓	0.0406	0.0363	0.9203	0.6208
G to Q ↑	0.0245	0.0247	1.3047	0.8741

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P0	X9_P0	X19_P0	X28_P0
D ↓	hold_falling to G	-0.0013	-0.0045	0.0052	0.0036
D ↑	hold_falling to G	0.0066	0.0018	0.0068	0.0068
D ↓	setup_falling to G	0.0417	0.0418	0.0321	0.0311
D ↑	setup_falling to G	0.0281	0.0328	0.0306	0.0306
G ↑	min_pulse_width to G	0.0411	0.0378	0.0318	0.0318

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	7.241e-05	1.000e-20
X9_P0	1.188e-04	1.000e-20
X19_P0	2.039e-04	1.000e-20
X28_P0	2.768e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	7.689e-06	2.234e-05	2.467e-05	6.798e-05
G (output stable)	6.439e-04	7.646e-04	1.280e-03	1.210e-03
D to Q	2.397e-03	3.836e-03	5.694e-03	8.255e-03
G to Q	2.318e-03	3.697e-03	5.375e-03	7.315e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

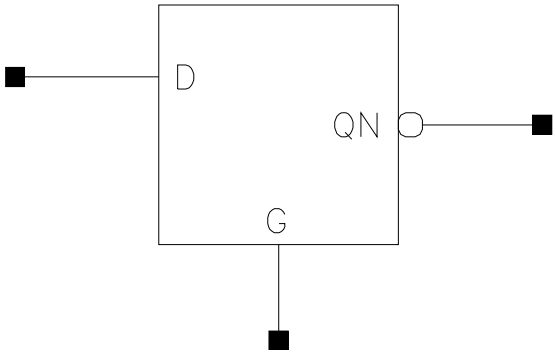
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P0
D	0.0003
G	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P0	X10_P0
D to QN ↓	0.0409	1.7958
D to QN ↑	0.0557	2.5802
G to QN ↓	0.0400	1.7961
G to QN ↑	0.0588	2.5808

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P0
D ↓	hold_falling to G	-0.0143
D ↑	hold_falling to G	-0.0014
D ↓	setup_falling to G	0.0418
D ↑	setup_falling to G	0.0286
G ↑	min_pulse_width to G	0.0377

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P0	1.096e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X10_P0
D (output stable)	7.355e-06
G (output stable)	7.130e-04
D to QN	3.080e-03
G to QN	3.007e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

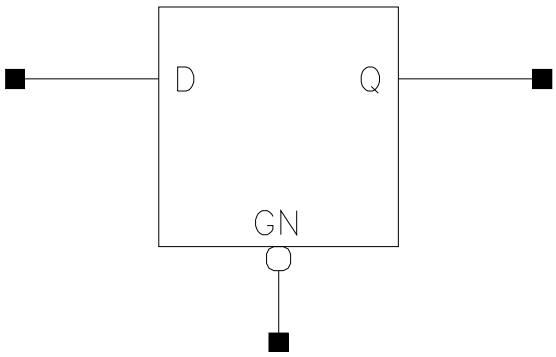
Pin Cycle (vdds)	X10_P0
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.360	1.0880
X9_P0	1.600	0.952	1.5232
X19_P0	1.600	1.224	1.9584
X28_P0	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0	X28_P0
D	0.0003	0.0006	0.0008	0.0012
GN	0.0007	0.0008	0.0011	0.0015

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D to Q ↓	0.0471	0.0438	3.8611	1.9237
D to Q ↑	0.0268	0.0316	5.2918	2.5939
GN to Q ↓	0.0426	0.0416	3.8611	1.9247

GN to Q ↑	0.0478	0.0452	5.2883	2.5826
	X19_P0	**X28_P0**	**X19_P0**	**X28_P0**
D to Q ↓	0.0362	0.0358	0.9199	0.6199
D to Q ↑	0.0282	0.0275	1.2930	0.8651
GN to Q ↓	0.0319	0.0303	0.9208	0.6198
GN to Q ↑	0.0400	0.0396	1.2891	0.8643

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P0	X9_P0	X19_P0	X28_P0
D ↓	hold_rising to GN	-0.0101	-0.0052	0.0002	-0.0003
D ↑	hold_rising to GN	0.0105	0.0052	0.0106	0.0106
D ↓	setup_rising to GN	0.0519	0.0445	0.0396	0.0401
D ↑	setup_rising to GN	0.0249	0.0293	0.0239	0.0249
GN ↓	min_pulse_width to GN	0.0585	0.0511	0.0439	0.0396

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	6.938e-05	1.000e-20
X9_P0	1.175e-04	1.000e-20
X19_P0	2.119e-04	1.000e-20
X28_P0	2.811e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	7.598e-06	1.266e-05	2.449e-05	5.798e-05
GN (output stable)	6.433e-04	7.624e-04	1.121e-03	1.209e-03
D to Q	2.402e-03	3.860e-03	5.913e-03	8.083e-03
GN to Q	3.553e-03	5.112e-03	7.479e-03	9.497e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

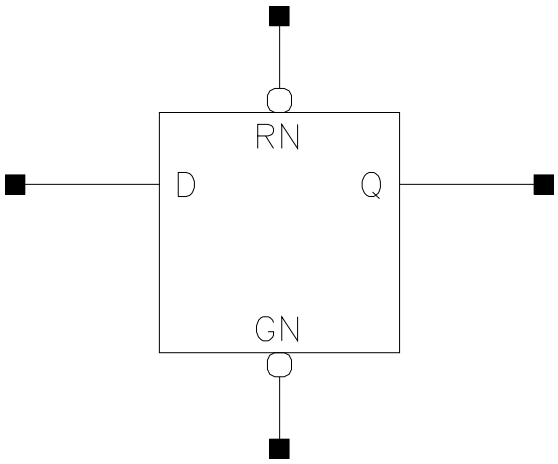
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.632	1.3056
X9_P0	1.600	1.224	1.9584
X19_P0	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0
D	0.0003	0.0005	0.0010
GN	0.0009	0.0009	0.0013
RN	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D to Q ↓	0.0488	0.0460	3.7954	1.8756

D to Q ↑	0.0457	0.0502	5.4926	2.6796
GN to Q ↓	0.0451	0.0426	3.7939	1.8770
GN to Q ↑	0.0634	0.0596	5.4944	2.6861
RN to Q ↓	0.0394	0.0494	3.6663	1.8742
RN to Q ↑	0.0495	0.0535	5.4910	2.6813
	X19_P0		**X19_P0**	
D to Q ↓	0.0376		0.9273	
D to Q ↑	0.0531		1.3527	
GN to Q ↓	0.0339		0.9281	
GN to Q ↑	0.0565		1.3553	
RN to Q ↓	0.0625		0.9853	
RN to Q ↑	0.0582		1.3523	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P0	X9_P0	X19_P0
D ↓	hold_rising to GN	-0.0101	-0.0074	-0.0030
D ↑	hold_rising to GN	-0.0039	-0.0088	-0.0137
D ↓	setup_rising to GN	0.0542	0.0494	0.0397
D ↑	setup_rising to GN	0.0460	0.0508	0.0588
GN ↓	min_pulse_width to GN	0.0617	0.0587	0.0588
RN ↓	min_pulse_width to RN	0.0496	0.0566	0.0735
RN ↑	recovery_rising to GN	0.0519	0.0558	0.0660
RN ↑	removal_rising to GN	-0.0292	-0.0337	-0.0413

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	7.052e-05	1.000e-20
X9_P0	1.144e-04	1.000e-20
X19_P0	1.991e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0
D (output stable)	3.205e-05	2.358e-05	3.526e-05
GN (output stable)	6.951e-04	7.221e-04	9.126e-04
RN (output stable)	3.005e-05	3.855e-05	5.243e-05
D to Q	3.102e-03	4.448e-03	6.912e-03
GN to Q	4.346e-03	5.669e-03	8.353e-03
RN to Q	2.243e-03	3.309e-03	5.565e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

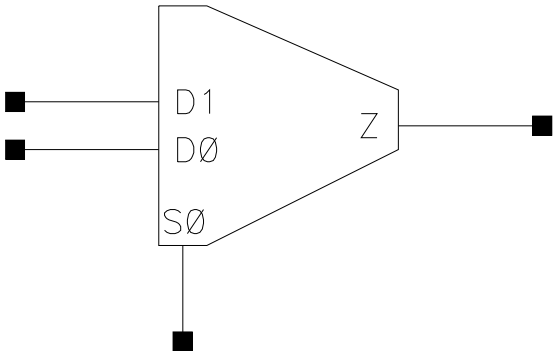
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.360	1.0880
X9_P0	0.800	1.496	1.1968
X14_P0	0.800	2.176	1.7408
X19_P0	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P0	X9_P0	X14_P0	X19_P0
D0	0.0005	0.0006	0.0008	0.0010
D1	0.0004	0.0006	0.0008	0.0010
S0	0.0009	0.0008	0.0011	0.0013

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D0 to Z ↓	0.0355	0.0327	3.8623	1.9439
D0 to Z ↑	0.0286	0.0273	5.4552	2.7547
D1 to Z ↓	0.0356	0.0316	3.8569	1.9406
D1 to Z ↑	0.0280	0.0257	5.4632	2.7477
S0 to Z ↓	0.0336	0.0285	3.8482	1.9346
S0 to Z ↑	0.0323	0.0287	5.4610	2.7496

	X14_P0	X19_P0	X14_P0	X19_P0
D0 to Z ↓	0.0356	0.0310	1.3384	0.9664
D0 to Z ↑	0.0290	0.0263	1.8583	1.3503
D1 to Z ↓	0.0358	0.0317	1.3369	0.9663
D1 to Z ↑	0.0277	0.0255	1.8590	1.3468
S0 to Z ↓	0.0342	0.0311	1.3332	0.9633
S0 to Z ↑	0.0338	0.0303	1.8595	1.3483

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	8.504e-05	1.000e-20
X9_P0	1.478e-04	1.000e-20
X14_P0	1.976e-04	1.000e-20
X19_P0	2.903e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X9_P0	X14_P0	X19_P0
D0 (output stable)	4.891e-04	8.914e-04	1.024e-03	1.323e-03
D1 (output stable)	4.648e-04	7.622e-04	1.065e-03	1.394e-03
S0 (output stable)	6.773e-04	6.092e-04	9.571e-04	1.153e-03
D0 to Z	1.770e-03	2.818e-03	4.486e-03	5.461e-03
D1 to Z	1.722e-03	2.622e-03	4.357e-03	5.416e-03
S0 to Z	2.166e-03	2.742e-03	4.899e-03	5.885e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

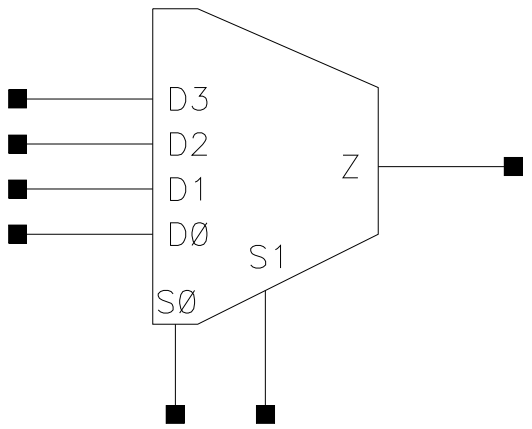
Pin Cycle (vdds)	X5_P0	X9_P0	X14_P0	X19_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.600	1.496	2.3936
X9_P0	1.600	1.768	2.8288
X13_P0	1.600	2.312	3.6992
X18_P0	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P0	X9_P0	X13_P0	X18_P0
D0	0.0004	0.0006	0.0008	0.0008
D1	0.0003	0.0004	0.0008	0.0008
D2	0.0003	0.0006	0.0008	0.0008
D3	0.0003	0.0005	0.0008	0.0008
S0	0.0011	0.0015	0.0018	0.0019
S1	0.0007	0.0007	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X9_P0**	**X4_P0**	**X9_P0**
D0 to Z ↓	0.0768	0.0625	4.1880	2.0534
D0 to Z ↑	0.0495	0.0434	5.6217	2.7741
D1 to Z ↓	0.0756	0.0620	4.1830	2.0555
D1 to Z ↑	0.0494	0.0430	5.6122	2.7724
D2 to Z ↓	0.0703	0.0629	4.1378	2.0595
D2 to Z ↑	0.0474	0.0429	5.5779	2.7685
D3 to Z ↓	0.0712	0.0620	4.1504	2.0598
D3 to Z ↑	0.0481	0.0429	5.5778	2.7675
S0 to Z ↓	0.0796	0.0690	4.1673	2.0573
S0 to Z ↑	0.0581	0.0537	5.6124	2.7759
S1 to Z ↓	0.0508	0.0468	4.1617	2.0570
S1 to Z ↑	0.0452	0.0420	5.6009	2.7710
	X13_P0	**X18_P0**	**X13_P0**	**X18_P0**
D0 to Z ↓	0.0601	0.0650	1.4321	1.0695
D0 to Z ↑	0.0390	0.0421	1.8550	1.4023
D1 to Z ↓	0.0607	0.0656	1.4341	1.0709
D1 to Z ↑	0.0400	0.0432	1.8551	1.4020
D2 to Z ↓	0.0556	0.0601	1.4168	1.0571
D2 to Z ↑	0.0387	0.0418	1.8475	1.3982
D3 to Z ↓	0.0555	0.0599	1.4165	1.0568
D3 to Z ↑	0.0391	0.0421	1.8480	1.3967
S0 to Z ↓	0.0642	0.0690	1.4245	1.0639
S0 to Z ↑	0.0486	0.0518	1.8546	1.4019
S1 to Z ↓	0.0447	0.0495	1.4247	1.0634
S1 to Z ↑	0.0380	0.0411	1.8530	1.4012

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	8.098e-05	1.000e-20
X9_P0	1.324e-04	1.000e-20
X13_P0	2.217e-04	1.000e-20
X18_P0	2.503e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X9_P0	X13_P0	X18_P0
D0 (output stable)	3.229e-05	3.642e-05	7.175e-05	7.164e-05
D1 (output stable)	4.639e-05	4.709e-05	6.773e-05	6.768e-05
D2 (output stable)	4.137e-05	4.744e-05	6.668e-05	6.666e-05
D3 (output stable)	3.496e-05	4.781e-05	6.194e-05	6.219e-05
S0 (output stable)	8.208e-04	9.755e-04	1.561e-03	1.562e-03
S1 (output stable)	9.812e-04	1.095e-03	1.708e-03	1.713e-03
D0 to Z	2.327e-03	3.430e-03	5.412e-03	6.790e-03
D1 to Z	2.294e-03	3.415e-03	5.479e-03	6.864e-03
D2 to Z	2.175e-03	3.420e-03	5.177e-03	6.491e-03
D3 to Z	2.203e-03	3.423e-03	5.198e-03	6.510e-03
S0 to Z	3.189e-03	4.547e-03	7.085e-03	8.447e-03
S1 to Z	2.720e-03	3.851e-03	5.979e-03	7.313e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

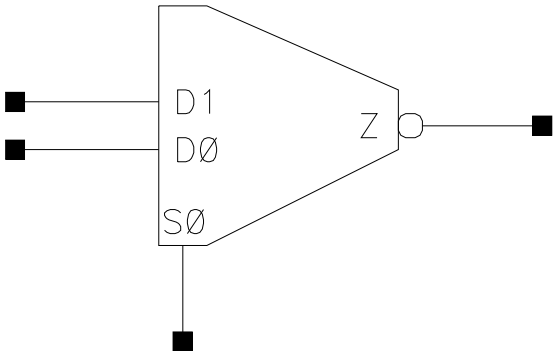
Pin Cycle (vdds)	X4_P0	X9_P0	X13_P0	X18_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P0	0.800	0.952	0.7616
X2_P0	0.800	0.952	0.7616
X6_P0	0.800	1.904	1.5232
X9_P0	0.800	2.448	1.9584
X12_P0	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P0	X2_P0	X6_P0	X9_P0
D0	0.0003	0.0004	0.0009	0.0014
D1	0.0003	0.0004	0.0009	0.0014
S0	0.0009	0.0012	0.0016	0.0023
	X12_P0			
D0	0.0018			
D1	0.0018			
S0	0.0026			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P0	**X2_P0**	**X1_P0**	**X2_P0**
D0 to Z ↓	0.0121	0.0111	11.1204	7.3335

D0 to Z ↑	0.0248	0.0187	23.6158	12.5027
D1 to Z ↓	0.0115	0.0106	10.9799	7.2165
D1 to Z ↑	0.0250	0.0191	23.6784	12.6823
S0 to Z ↓	0.0227	0.0154	10.9807	7.2517
S0 to Z ↑	0.0263	0.0168	23.5628	12.5562
	X6_P0	**X9_P0**	**X6_P0**	**X9_P0**
D0 to Z ↓	0.0126	0.0116	3.2441	2.1889
D0 to Z ↑	0.0196	0.0184	5.1570	3.5929
D1 to Z ↓	0.0123	0.0117	3.1993	2.1958
D1 to Z ↑	0.0207	0.0189	5.3165	3.4991
S0 to Z ↓	0.0179	0.0152	3.2115	2.1850
S0 to Z ↑	0.0192	0.0169	5.2203	3.5396
	X12_P0		**X12_P0**	
D0 to Z ↓	0.0121		1.6734	
D0 to Z ↑	0.0185		2.7067	
D1 to Z ↓	0.0117		1.6641	
D1 to Z ↑	0.0187		2.6357	
S0 to Z ↓	0.0165		1.6626	
S0 to Z ↑	0.0178		2.6668	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X1_P0	2.903e-05	1.000e-20
X2_P0	5.988e-05	1.000e-20
X6_P0	1.182e-04	1.000e-20
X9_P0	1.837e-04	1.000e-20
X12_P0	2.217e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X1_P0	X2_P0	X6_P0	X9_P0
D0 (output stable)	7.409e-06	1.792e-05	5.432e-05	7.812e-05
D1 (output stable)	7.154e-06	1.836e-05	5.923e-05	8.429e-05
S0 (output stable)	6.682e-04	7.844e-04	1.275e-03	2.014e-03
D0 to Z	5.471e-04	7.169e-04	1.880e-03	2.549e-03
D1 to Z	5.455e-04	7.096e-04	1.908e-03	2.599e-03
S0 to Z	1.151e-03	1.302e-03	2.665e-03	3.809e-03
	X12_P0			
D0 (output stable)	1.017e-04			
D1 (output stable)	1.054e-04			
S0 (output stable)	2.275e-03			
D0 to Z	3.445e-03			
D1 to Z	3.433e-03			
S0 to Z	4.725e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X1_P0	X2_P0	X6_P0	X9_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

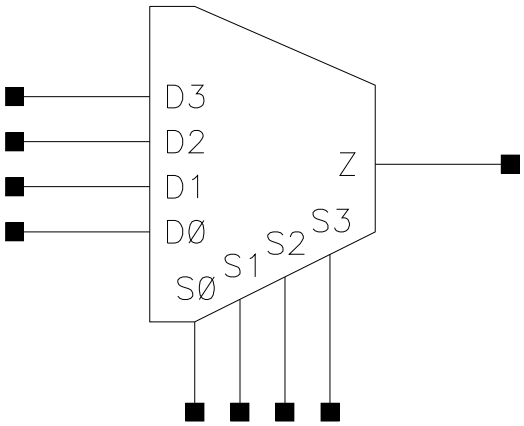
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P0			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.600	0.952	1.5232
X15_P0	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P0	X15_P0
D0	0.0005	0.0012
D1	0.0005	0.0010
D2	0.0005	0.0012
D3	0.0005	0.0010
S0	0.0005	0.0011
S1	0.0005	0.0013
S2	0.0005	0.0011
S3	0.0005	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X15_P0	X4_P0	X15_P0
D0 to Z ↓	0.0393	0.0413	6.2787	1.6504
D0 to Z ↑	0.0333	0.0312	5.1399	1.2973
D1 to Z ↓	0.0362	0.0372	6.2723	1.6496
D1 to Z ↑	0.0290	0.0271	5.1077	1.2908
D2 to Z ↓	0.0385	0.0405	6.2822	1.6516
D2 to Z ↑	0.0327	0.0300	5.1540	1.3030
D3 to Z ↓	0.0350	0.0366	6.2756	1.6496
D3 to Z ↑	0.0282	0.0262	5.1202	1.2966
S0 to Z ↓	0.0377	0.0378	6.2742	1.6485
S0 to Z ↑	0.0354	0.0316	5.1372	1.2975
S1 to Z ↓	0.0343	0.0344	6.2729	1.6477
S1 to Z ↑	0.0306	0.0278	5.1089	1.2889
S2 to Z ↓	0.0374	0.0373	6.2819	1.6489
S2 to Z ↑	0.0348	0.0307	5.1544	1.3035
S3 to Z ↓	0.0344	0.0338	6.2745	1.6467
S3 to Z ↑	0.0305	0.0267	5.1221	1.2957

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	1.012e-04	1.000e-20
X15_P0	2.969e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X15_P0
D0 (output stable)	2.910e-04	8.074e-04
D1 (output stable)	2.492e-04	6.769e-04
D2 (output stable)	2.884e-04	7.972e-04
D3 (output stable)	2.482e-04	6.712e-04
S0 (output stable)	2.793e-04	7.696e-04
S1 (output stable)	2.410e-04	6.620e-04
S2 (output stable)	2.832e-04	7.701e-04
S3 (output stable)	2.438e-04	6.612e-04
D0 to Z	2.252e-03	6.441e-03
D1 to Z	1.949e-03	5.590e-03
D2 to Z	2.101e-03	5.940e-03
D3 to Z	1.807e-03	5.119e-03
S0 to Z	2.185e-03	6.064e-03
S1 to Z	1.892e-03	5.284e-03
S2 to Z	2.054e-03	5.597e-03
S3 to Z	1.768e-03	4.787e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

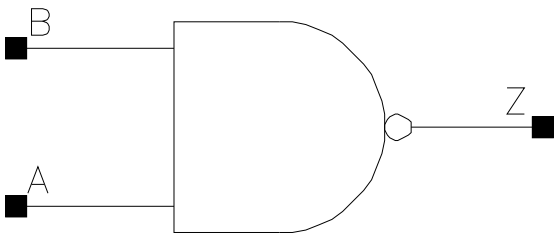
Pin Cycle (vdds)	X4_P0	X15_P0
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P0	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P0	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P0	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P0	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P0	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P0	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P0	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P0	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P0	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P0	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P0	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P0	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P0	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P0	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P0	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P0	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P0	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P0	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P0	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P0	C8T28SOI_LL_-NAND2X4_P0	C8T28SOI_LL_-NAND2X8_P0	C8T28SOI_LL_-NAND2X12_P0
A	0.0003	0.0004	0.0009	0.0013
B	0.0003	0.0004	0.0008	0.0012
	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X24_P0	C8T28SOI_-LLBR0P8_-NAND2X4_P0
A	0.0017	0.0022	0.0006	0.0006
B	0.0016	0.0021	0.0006	0.0005
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	C8T28SOI_-LLBR0P8_-NAND2X12_P0	C8T28SOI_-LLBR0P8_-NAND2X16_P0	C8T28SOI_LLS_-NAND2X8_P0
A	0.0009	0.0014	0.0018	0.0009
B	0.0008	0.0012	0.0016	0.0008
	C8T28SOI_LLS_-NAND2X15_P0	C8T28SOI_LLS_-NAND2X23_P0	C8T28SOI_LLS_-NAND2X31_P0	C8T28SOIDV_LL_-NAND2X9_P0
A	0.0018	0.0027	0.0036	0.0009
B	0.0016	0.0025	0.0034	0.0010
	C8T28SOIDV_LL_-NAND2X18_P0	C8T28SOIDV_LL_-NAND2X27_P0	C8T28SOIDV_LL_-NAND2X36_P0	
A	0.0019	0.0028	0.0038	
B	0.0018	0.0027	0.0035	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND2X2_P0	**C8T28SOI_LL_-NAND2X4_P0**	**C8T28SOI_LL_-NAND2X2_P0**	**C8T28SOI_LL_-NAND2X4_P0**
A to Z ↓	0.0093	0.0080	12.0711	6.3789
A to Z ↑	0.0146	0.0119	10.5467	5.5017
B to Z ↓	0.0110	0.0091	12.1377	6.4203
B to Z ↑	0.0138	0.0108	10.5811	5.5753
	C8T28SOI_LL_-NAND2X8_P0	**C8T28SOI_LL_-NAND2X12_P0**	**C8T28SOI_LL_-NAND2X8_P0**	**C8T28SOI_LL_-NAND2X12_P0**
A to Z ↓	0.0088	0.0084	3.2028	2.1885
A to Z ↑	0.0120	0.0117	2.6254	1.7861
B to Z ↓	0.0083	0.0087	3.2243	2.2035
B to Z ↑	0.0095	0.0097	2.6390	1.8056

	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0
A to Z ↓	0.0086	0.0085	1.6585	1.3382
A to Z ↑	0.0117	0.0117	1.3442	1.0866
B to Z ↓	0.0084	0.0088	1.6710	1.3484
B to Z ↑	0.0093	0.0096	1.3577	1.0982
	C8T28SOI_LL_-NAND2X24_P0	**C8T28SOI_-LLBR0P8_-NAND2X4_P0**	**C8T28SOI_LL_-NAND2X24_P0**	**C8T28SOI_-LLBR0P8_-NAND2X4_P0**
A to Z ↓	0.0330	0.0061	0.7489	4.4522
A to Z ↑	0.0338	0.0156	1.0666	7.0365
B to Z ↓	0.0341	0.0064	0.7484	4.4980
B to Z ↑	0.0325	0.0136	1.0678	7.0227
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	**C8T28SOI_-LLBR0P8_-NAND2X12_P0**	**C8T28SOI_-LLBR0P8_-NAND2X8_P0**	**C8T28SOI_-LLBR0P8_-NAND2X12_P0**
A to Z ↓	0.0066	0.0066	2.4269	1.6553
A to Z ↑	0.0156	0.0156	3.5407	2.3941
B to Z ↓	0.0054	0.0062	2.4556	1.6754
B to Z ↑	0.0119	0.0125	3.5557	2.4066
	C8T28SOI_-LLBR0P8_-NAND2X16_P0	**C8T28SOI_LLS_-NAND2X8_P0**	**C8T28SOI_-LLBR0P8_-NAND2X16_P0**	**C8T28SOI_LLS_-NAND2X8_P0**
A to Z ↓	0.0063	0.0088	1.2633	3.1982
A to Z ↑	0.0150	0.0121	1.7927	2.6529
B to Z ↓	0.0053	0.0083	1.2790	3.2189
B to Z ↑	0.0114	0.0096	1.8076	2.6822
	C8T28SOI_LLS_-NAND2X15_P0	**C8T28SOI_LLS_-NAND2X23_P0**	**C8T28SOI_LLS_-NAND2X15_P0**	**C8T28SOI_LLS_-NAND2X23_P0**
A to Z ↓	0.0087	0.0087	1.6559	1.1167
A to Z ↑	0.0117	0.0116	1.3266	0.8851
B to Z ↓	0.0085	0.0087	1.6680	1.1249
B to Z ↑	0.0093	0.0093	1.3347	0.8905
	C8T28SOI_LLS_-NAND2X31_P0	**C8T28SOIDV_LL_-NAND2X9_P0**	**C8T28SOI_LLS_-NAND2X31_P0**	**C8T28SOIDV_LL_-NAND2X9_P0**
A to Z ↓	0.0087	0.0072	0.8443	2.4151
A to Z ↑	0.0116	0.0126	0.6661	2.5692
B to Z ↓	0.0088	0.0078	0.8508	2.4342
B to Z ↑	0.0094	0.0111	0.6701	2.6120
	C8T28SOIDV_LL_-NAND2X18_P0	**C8T28SOIDV_LL_-NAND2X27_P0**	**C8T28SOIDV_LL_-NAND2X18_P0**	**C8T28SOIDV_LL_-NAND2X27_P0**
A to Z ↓	0.0077	0.0078	1.2234	0.8316
A to Z ↑	0.0129	0.0129	1.2929	0.8714
B to Z ↓	0.0070	0.0078	1.2331	0.8390
B to Z ↑	0.0102	0.0108	1.3001	0.8761
	C8T28SOIDV_LL_-NAND2X36_P0		**C8T28SOIDV_LL_-NAND2X36_P0**	
A to Z ↓	0.0078		0.6273	
A to Z ↑	0.0128		0.6530	
B to Z ↓	0.0073		0.6329	
B to Z ↑	0.0101		0.6571	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P0	1.274e-05	1.000e-20
C8T28SOI_LL_NAND2X4_P0	2.890e-05	1.000e-20
C8T28SOI_LL_NAND2X8_P0	5.789e-05	1.000e-20
C8T28SOI_LL_NAND2X12_P0	8.320e-05	1.000e-20
C8T28SOI_LL_NAND2X15_P0	1.086e-04	1.000e-20
C8T28SOI_LL_NAND2X19_P0	1.340e-04	1.000e-20
C8T28SOI_LL_NAND2X24_P0	2.071e-04	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P0	3.008e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P0	5.397e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_P0	7.682e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_P0	9.975e-05	1.000e-20
C8T28SOI_LLS_NAND2X8_P0	5.789e-05	1.000e-20
C8T28SOI_LLS_NAND2X15_P0	1.086e-04	1.000e-20
C8T28SOI_LLS_NAND2X23_P0	1.594e-04	1.000e-20
C8T28SOI_LLS_NAND2X31_P0	2.102e-04	1.000e-20
C8T28SOIDV_LL_NAND2X9_P0	7.130e-05	1.000e-20
C8T28SOIDV_LL_NAND2X18_P0	1.364e-04	1.000e-20
C8T28SOIDV_LL_NAND2X27_P0	1.978e-04	1.000e-20
C8T28SOIDV_LL_NAND2X36_P0	2.592e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P0	C8T28SOI_LL_-NAND2X4_P0	C8T28SOI_LL_-NAND2X8_P0	C8T28SOI_LL_-NAND2X12_P0
A (output stable)	5.655e-06	1.064e-05	5.168e-05	6.286e-05
B (output stable)	9.629e-06	1.822e-05	1.265e-04	1.295e-04
A to Z	3.778e-04	6.065e-04	1.310e-03	1.891e-03
B to Z	3.447e-04	5.348e-04	1.043e-03	1.594e-03
	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X24_P0	C8T28SOI_-LLBR0P8_-NAND2X4_P0
A (output stable)	9.436e-05	1.041e-04	1.257e-05	1.561e-05
B (output stable)	2.169e-04	2.026e-04	2.093e-05	2.566e-05
A to Z	2.528e-03	3.119e-03	5.475e-03	6.607e-04
B to Z	2.045e-03	2.620e-03	5.412e-03	5.676e-04
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	C8T28SOI_-LLBR0P8_-NAND2X12_P0	C8T28SOI_-LLBR0P8_-NAND2X16_P0	C8T28SOI_LLS_-NAND2X8_P0
A (output stable)	6.202e-05	7.414e-05	1.177e-04	5.210e-05
B (output stable)	1.513e-04	1.551e-04	2.595e-04	1.318e-04
A to Z	1.333e-03	1.983e-03	2.516e-03	1.316e-03
B to Z	9.790e-04	1.562e-03	1.872e-03	1.050e-03
	C8T28SOI_LLS_-NAND2X15_P0	C8T28SOI_LLS_-NAND2X23_P0	C8T28SOI_LLS_-NAND2X31_P0	C8T28SOIDV_LL_-NAND2X9_P0
A (output stable)	1.000e-04	1.433e-04	1.853e-04	2.792e-05
B (output stable)	2.258e-04	3.015e-04	3.791e-04	4.695e-05
A to Z	2.558e-03	3.801e-03	5.041e-03	1.434e-03
B to Z	2.067e-03	3.112e-03	4.151e-03	1.253e-03
	C8T28SOIDV_LL_-NAND2X18_P0	C8T28SOIDV_LL_-NAND2X27_P0	C8T28SOIDV_LL_-NAND2X36_P0	
A (output stable)	1.120e-04	1.305e-04	2.242e-04	
B (output stable)	3.026e-04	2.507e-04	5.733e-04	
A to Z	2.933e-03	4.351e-03	5.763e-03	

B to Z	2.332e-03	3.693e-03	4.607e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

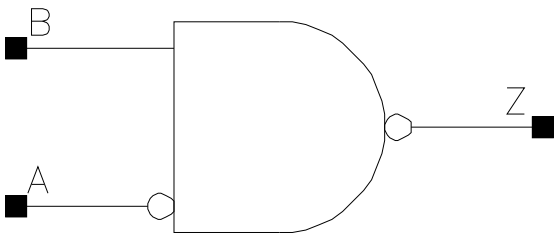
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P0	C8T28SOI_LL_-NAND2X4_P0	C8T28SOI_LL_-NAND2X8_P0	C8T28SOI_LL_-NAND2X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X24_P0	C8T28SOI_-LLBR0P8_-NAND2X4_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	C8T28SOI_-LLBR0P8_-NAND2X12_P0	C8T28SOI_-LLBR0P8_-NAND2X16_P0	C8T28SOI_LLS_-NAND2X8_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P0	C8T28SOI_LLS_-NAND2X23_P0	C8T28SOI_LLS_-NAND2X31_P0	C8T28SOIDV_LL_-NAND2X9_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P0	C8T28SOIDV_LL_-NAND2X27_P0	C8T28SOIDV_LL_-NAND2X36_P0	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.544	0.4352
X4_P0	0.800	0.680	0.5440
X9_P0	1.600	0.544	0.8704
X13_P0	1.600	0.816	1.3056
X17_P0	1.600	0.816	1.3056
X23_P0	0.800	2.312	1.8496
X27_P0	1.600	1.088	1.7408
X31_P0	0.800	2.992	2.3936
X36_P0	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P0	X4_P0	X9_P0	X13_P0
A	0.0005	0.0005	0.0008	0.0008
B	0.0003	0.0004	0.0009	0.0014
	X17_P0	X23_P0	X27_P0	X31_P0
A	0.0008	0.0016	0.0013	0.0022
B	0.0017	0.0025	0.0027	0.0032
	X36_P0			
A	0.0013			
B	0.0035			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X4_P0**	**X2_P0**	**X4_P0**
A to Z ↓	0.0254	0.0258	12.1186	6.4201
A to Z ↑	0.0192	0.0193	10.3418	5.3572
B to Z ↓	0.0113	0.0092	12.3077	6.5323
B to Z ↑	0.0139	0.0107	10.5847	5.5713
	X9_P0	**X13_P0**	**X9_P0**	**X13_P0**
A to Z ↓	0.0251	0.0303	2.4484	1.5688
A to Z ↑	0.0183	0.0223	2.5316	1.7119
B to Z ↓	0.0080	0.0078	2.5032	1.6025
B to Z ↑	0.0111	0.0114	2.6220	1.7927
	X17_P0	**X23_P0**	**X17_P0**	**X23_P0**
A to Z ↓	0.0327	0.0240	1.2247	1.1047
A to Z ↑	0.0231	0.0189	1.2984	0.8821
B to Z ↓	0.0075	0.0085	1.2497	1.1277
B to Z ↑	0.0107	0.0093	1.3660	0.9114
	X27_P0	**X31_P0**	**X27_P0**	**X31_P0**
A to Z ↓	0.0277	0.0240	0.8246	0.8351
A to Z ↑	0.0205	0.0188	0.8618	0.6474
B to Z ↓	0.0074	0.0087	0.8437	0.8518
B to Z ↑	0.0103	0.0094	0.8799	0.6858
	X36_P0		**X36_P0**	
A to Z ↓	0.0317		0.6235	
A to Z ↑	0.0234		0.6454	
B to Z ↓	0.0073		0.6360	
B to Z ↑	0.0100		0.6607	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P0	2.356e-05	1.000e-20
X4_P0	4.151e-05	1.000e-20
X9_P0	1.055e-04	1.000e-20
X13_P0	1.274e-04	1.000e-20
X17_P0	1.641e-04	1.000e-20
X23_P0	2.423e-04	1.000e-20
X27_P0	2.636e-04	1.000e-20
X31_P0	3.179e-04	1.000e-20
X36_P0	3.269e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P0	X4_P0	X9_P0	X13_P0
A (output stable)	5.365e-04	6.530e-04	1.258e-03	1.755e-03
B (output stable)	9.645e-06	1.851e-05	4.985e-05	1.386e-04
A to Z	8.899e-04	1.192e-03	2.557e-03	3.995e-03
B to Z	3.461e-04	5.310e-04	1.265e-03	1.907e-03
	X17_P0	X23_P0	X27_P0	X31_P0
A (output stable)	1.937e-03	3.229e-03	3.109e-03	4.275e-03
B (output stable)	1.659e-04	2.652e-04	2.615e-04	3.508e-04
A to Z	4.789e-03	6.773e-03	7.021e-03	9.037e-03
B to Z	2.394e-03	3.112e-03	3.539e-03	4.136e-03
	X36_P0			
A (output stable)	3.968e-03			

B (output stable)	4.227e-04			
A to Z	9.357e-03			
B to Z	4.572e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

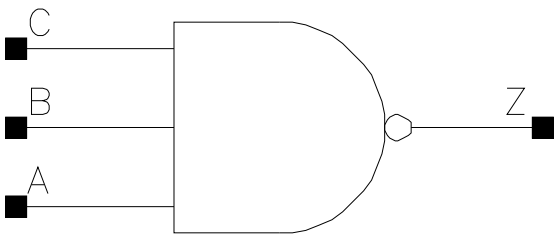
Pin Cycle (vdds)	X2_P0	X4_P0	X9_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P0	X23_P0	X27_P0	X31_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P0	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P0	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P0	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P0	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P0	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P0	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P0	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P0	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P0	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P0	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P0	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P0	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P0	C8T28SOI_LL_-NAND3X7_P0	C8T28SOI_LL_-NAND3X10_P0	C8T28SOI_LL_-NAND3X14_P0
A	0.0004	0.0009	0.0013	0.0017
B	0.0004	0.0009	0.0013	0.0016
C	0.0005	0.0008	0.0012	0.0016
	C8T28SOI_LL_-NAND3X20_P0	C8T28SOI_LL_-NAND3X27_P0	C8T28SOI_-LLBR0P6_-NAND3X3_P0	C8T28SOI_-LLBR0P6_-NAND3X7_P0
A	0.0026	0.0036	0.0006	0.0009
B	0.0025	0.0034	0.0004	0.0009
C	0.0024	0.0032	0.0005	0.0008
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	C8T28SOI_-LLBR0P6_-NAND3X14_P0	C8T28SOI_-LLBR0P6_-NAND3X20_P0	C8T28SOI_-LLBR0P6_-NAND3X27_P0
A	0.0013	0.0018	0.0027	0.0035
B	0.0012	0.0016	0.0024	0.0033
C	0.0012	0.0016	0.0024	0.0032

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-NAND3X3_P0	**C8T28SOI_LL_-NAND3X7_P0**	**C8T28SOI_LL_-NAND3X3_P0**	**C8T28SOI_LL_-NAND3X7_P0**
A to Z ↓	0.0124	0.0138	9.2646	4.6083
A to Z ↑	0.0147	0.0151	5.5366	2.7054
B to Z ↓	0.0133	0.0139	9.2916	4.6245
B to Z ↑	0.0137	0.0139	5.5631	2.7104
C to Z ↓	0.0139	0.0130	9.3137	4.6310
C to Z ↑	0.0126	0.0116	5.6231	2.6413
	C8T28SOI_LL_-NAND3X10_P0	**C8T28SOI_LL_-NAND3X14_P0**	**C8T28SOI_LL_-NAND3X10_P0**	**C8T28SOI_LL_-NAND3X14_P0**
A to Z ↓	0.0131	0.0134	3.1757	2.3958
A to Z ↑	0.0142	0.0145	1.7581	1.3648
B to Z ↓	0.0136	0.0135	3.1877	2.4033
B to Z ↑	0.0131	0.0132	1.8045	1.3649
C to Z ↓	0.0130	0.0129	3.1937	2.4078
C to Z ↑	0.0112	0.0111	1.8145	1.3545
	C8T28SOI_LL_-NAND3X20_P0	**C8T28SOI_LL_-NAND3X27_P0**	**C8T28SOI_LL_-NAND3X20_P0**	**C8T28SOI_LL_-NAND3X27_P0**
A to Z ↓	0.0131	0.0132	1.6280	1.2362
A to Z ↑	0.0140	0.0140	0.8859	0.6683
B to Z ↓	0.0136	0.0136	1.6338	1.2409
B to Z ↑	0.0128	0.0128	0.8862	0.6670
C to Z ↓	0.0129	0.0131	1.6374	1.2430
C to Z ↑	0.0109	0.0109	0.9062	0.6824
	C8T28SOI_-LLBR0P6_-NAND3X3_P0	**C8T28SOI_-LLBR0P6_-NAND3X7_P0**	**C8T28SOI_-LLBR0P6_-NAND3X3_P0**	**C8T28SOI_-LLBR0P6_-NAND3X7_P0**
A to Z ↓	0.0082	0.0104	5.7297	3.1594
A to Z ↑	0.0209	0.0226	8.3373	4.2393
B to Z ↓	0.0083	0.0097	5.7790	3.1819
B to Z ↑	0.0186	0.0198	8.3037	4.2494

C to Z ↓	0.0080	0.0080	5.8248	3.2029
C to Z ↑	0.0162	0.0158	8.3501	4.2165
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	**C8T28SOI_-LLBR0P6_-NAND3X14_P0**	**C8T28SOI_-LLBR0P6_-NAND3X10_P0**	**C8T28SOI_-LLBR0P6_-NAND3X14_P0**
A to Z ↓	0.0092	0.0098	2.1197	1.6076
A to Z ↑	0.0211	0.0217	2.8327	2.1445
B to Z ↓	0.0088	0.0089	2.1377	1.6207
B to Z ↑	0.0183	0.0187	2.8384	2.1475
C to Z ↓	0.0075	0.0072	2.1535	1.6335
C to Z ↑	0.0149	0.0147	2.8543	2.1419
	C8T28SOI_-LLBR0P6_-NAND3X20_P0	**C8T28SOI_-LLBR0P6_-NAND3X27_P0**	**C8T28SOI_-LLBR0P6_-NAND3X20_P0**	**C8T28SOI_-LLBR0P6_-NAND3X27_P0**
A to Z ↓	0.0093	0.0094	1.0871	0.8312
A to Z ↑	0.0212	0.0211	1.4289	1.0779
B to Z ↓	0.0088	0.0087	1.0961	0.8377
B to Z ↑	0.0184	0.0182	1.4298	1.0765
C to Z ↓	0.0072	0.0073	1.1049	0.8445
C to Z ↑	0.0144	0.0143	1.4358	1.0803

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P0	2.243e-05	1.000e-20
C8T28SOI_LL_NAND3X7_P0	4.655e-05	1.000e-20
C8T28SOI_LL_NAND3X10_P0	6.460e-05	1.000e-20
C8T28SOI_LL_NAND3X14_P0	8.655e-05	1.000e-20
C8T28SOI_LL_NAND3X20_P0	1.265e-04	1.000e-20
C8T28SOI_LL_NAND3X27_P0	1.665e-04	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P0	2.346e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P0	4.485e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_P0	6.015e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_P0	8.149e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_P0	1.180e-04	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_P0	1.546e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P0	C8T28SOI_LL_-NAND3X7_P0	C8T28SOI_LL_-NAND3X10_P0	C8T28SOI_LL_-NAND3X14_P0
A (output stable)	1.183e-05	5.088e-05	6.404e-05	9.393e-05
B (output stable)	1.480e-05	6.289e-05	8.243e-05	1.120e-04
C (output stable)	3.147e-05	1.494e-04	1.788e-04	2.680e-04
A to Z	8.088e-04	1.804e-03	2.508e-03	3.402e-03
B to Z	7.300e-04	1.554e-03	2.148e-03	2.909e-03
C to Z	6.604e-04	1.319e-03	1.846e-03	2.477e-03
	C8T28SOI_LL_-NAND3X20_P0	C8T28SOI_LL_-NAND3X27_P0	C8T28SOI_-LLBR0P6_-NAND3X3_P0	C8T28SOI_-LLBR0P6_-NAND3X7_P0
A (output stable)	1.309e-04	1.743e-04	1.991e-05	6.791e-05
B (output stable)	1.650e-04	2.133e-04	2.277e-05	8.107e-05
C (output stable)	3.965e-04	5.077e-04	5.065e-05	2.001e-04

A to Z	4.952e-03	6.567e-03	8.478e-04	1.928e-03
B to Z	4.259e-03	5.634e-03	7.207e-04	1.556e-03
C to Z	3.563e-03	4.753e-03	5.984e-04	1.185e-03
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	C8T28SOI_-LLBR0P6_-NAND3X14_P0	C8T28SOI_-LLBR0P6_-NAND3X20_P0	C8T28SOI_-LLBR0P6_-NAND3X27_P0
A (output stable)	8.594e-05	1.376e-04	1.795e-04	2.429e-04
B (output stable)	1.041e-04	1.607e-04	2.213e-04	2.830e-04
C (output stable)	2.440e-04	3.674e-04	5.358e-04	6.860e-04
A to Z	2.597e-03	3.604e-03	5.191e-03	6.862e-03
B to Z	2.051e-03	2.827e-03	4.091e-03	5.374e-03
C to Z	1.604e-03	2.117e-03	3.048e-03	4.042e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

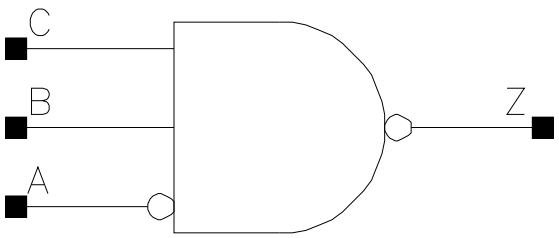
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P0	C8T28SOI_LL_-NAND3X7_P0	C8T28SOI_LL_-NAND3X10_P0	C8T28SOI_LL_-NAND3X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P0	C8T28SOI_LL_-NAND3X27_P0	C8T28SOI_-LLBR0P6_-NAND3X3_P0	C8T28SOI_-LLBR0P6_-NAND3X7_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	C8T28SOI_-LLBR0P6_-NAND3X14_P0	C8T28SOI_-LLBR0P6_-NAND3X20_P0	C8T28SOI_-LLBR0P6_-NAND3X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X7_P0	0.800	1.360	1.0880
X10_P0	0.800	1.632	1.3056
X14_P0	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X10_P0	X14_P0
A	0.0006	0.0008	0.0007	0.0007
B	0.0004	0.0009	0.0013	0.0017
C	0.0005	0.0008	0.0012	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0314	0.0301	9.2727	4.6338
A to Z ↑	0.0220	0.0220	5.3614	2.5840
B to Z ↓	0.0129	0.0135	9.3479	4.6688
B to Z ↑	0.0132	0.0133	5.5700	2.6499
C to Z ↓	0.0135	0.0125	9.3722	4.6766
C to Z ↑	0.0121	0.0110	5.6216	2.6458
	X10_P0	**X14_P0**	**X10_P0**	**X14_P0**
A to Z ↓	0.0328	0.0355	3.1655	2.4039

A to Z ↑	0.0242	0.0266	1.7606	1.3193
B to Z ↓	0.0136	0.0131	3.1886	2.4204
B to Z ↑	0.0130	0.0127	1.8064	1.3526
C to Z ↓	0.0129	0.0125	3.1943	2.4250
C to Z ↑	0.0112	0.0106	1.8177	1.3556

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	3.352e-05	1.000e-20
X7_P0	7.483e-05	1.000e-20
X10_P0	9.440e-05	1.000e-20
X14_P0	1.164e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	6.574e-04	1.221e-03	1.493e-03	1.798e-03
B (output stable)	1.505e-05	5.282e-05	8.400e-05	1.029e-04
C (output stable)	3.158e-05	1.558e-04	1.846e-04	2.617e-04
A to Z	1.390e-03	2.932e-03	4.025e-03	5.168e-03
B to Z	6.955e-04	1.486e-03	2.147e-03	2.803e-03
C to Z	6.242e-04	1.233e-03	1.838e-03	2.358e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

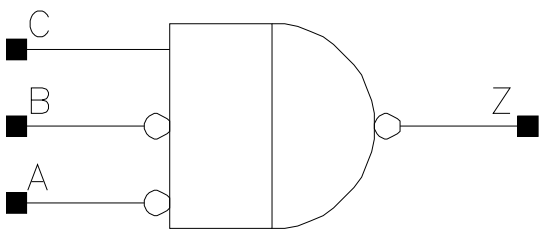
Pin Cycle (vdds)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	0.816	0.6528
X8_P0	0.800	1.088	0.8704
X12_P0	0.800	1.632	1.3056
X15_P0	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X12_P0	X15_P0
A	0.0006	0.0006	0.0011	0.0010
B	0.0006	0.0006	0.0011	0.0010
C	0.0004	0.0008	0.0012	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0278	0.0336	5.9922	3.1842
A to Z ↑	0.0184	0.0212	5.1286	2.5616
B to Z ↓	0.0287	0.0345	5.9982	3.1839
B to Z ↑	0.0173	0.0202	5.1228	2.5574
C to Z ↓	0.0093	0.0085	6.0871	3.2222
C to Z ↑	0.0109	0.0097	5.1657	2.6590
	X12_P0	**X15_P0**	**X12_P0**	**X15_P0**
A to Z ↓	0.0308	0.0333	2.1671	1.6487
A to Z ↑	0.0197	0.0232	1.7108	1.2911
B to Z ↓	0.0299	0.0324	2.1669	1.6503

B to Z ↑	0.0178	0.0213	1.7093	1.2878
C to Z ↓	0.0093	0.0085	2.1988	1.6744
C to Z ↑	0.0102	0.0092	1.8023	1.3323

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	5.653e-05	1.000e-20
X8_P0	7.552e-05	1.000e-20
X12_P0	1.195e-04	1.000e-20
X15_P0	1.341e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	3.606e-04	4.715e-04	8.053e-04	8.984e-04
B (output stable)	3.369e-04	4.461e-04	7.457e-04	8.369e-04
C (output stable)	2.046e-05	1.256e-04	1.324e-04	2.100e-04
A to Z	1.659e-03	2.697e-03	4.258e-03	5.129e-03
B to Z	1.563e-03	2.596e-03	3.884e-03	4.755e-03
C to Z	5.980e-04	1.067e-03	1.687e-03	2.078e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

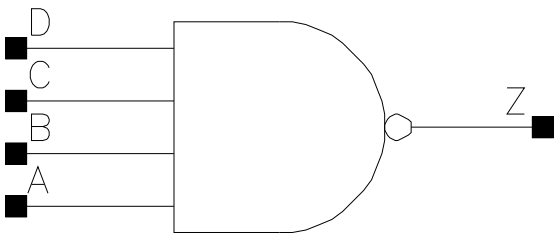
Pin Cycle (vdds)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.224	0.9792
X10_P0	0.800	1.360	1.0880
X14_P0	0.800	1.904	1.5232
X18_P0	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X18_P0
A	0.0004	0.0004	0.0005	0.0005
B	0.0004	0.0004	0.0005	0.0007
C	0.0004	0.0004	0.0004	0.0005
D	0.0004	0.0004	0.0005	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0457	0.0420	3.6054	1.8196
A to Z ↑	0.0373	0.0375	5.1784	2.6199
B to Z ↓	0.0477	0.0442	3.6064	1.8182
B to Z ↑	0.0365	0.0371	5.1784	2.6228
C to Z ↓	0.0482	0.0438	3.6012	1.8194
C to Z ↑	0.0394	0.0401	5.1727	2.6213

D to Z ↓	0.0508	0.0462	3.6029	1.8171
D to Z ↑	0.0393	0.0400	5.1730	2.6182
	X14_P0	**X18_P0**	**X14_P0**	**X18_P0**
A to Z ↓	0.0450	0.0415	1.2504	1.0128
A to Z ↑	0.0372	0.0361	1.7900	1.4138
B to Z ↓	0.0471	0.0432	1.2504	1.0129
B to Z ↑	0.0363	0.0356	1.7895	1.4133
C to Z ↓	0.0440	0.0383	1.2487	1.0125
C to Z ↑	0.0379	0.0356	1.7857	1.4097
D to Z ↓	0.0462	0.0398	1.2489	1.0124
D to Z ↑	0.0374	0.0345	1.7858	1.4115

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	5.826e-05	1.000e-20
X10_P0	9.238e-05	1.000e-20
X14_P0	1.323e-04	1.000e-20
X18_P0	1.791e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	2.616e-04	3.097e-04	4.528e-04	5.035e-04
B (output stable)	2.509e-04	2.974e-04	4.352e-04	4.869e-04
C (output stable)	2.896e-04	3.170e-04	4.757e-04	4.887e-04
D (output stable)	2.775e-04	3.050e-04	4.557e-04	4.652e-04
A to Z	2.024e-03	2.873e-03	4.464e-03	5.173e-03
B to Z	1.993e-03	2.840e-03	4.411e-03	5.126e-03
C to Z	2.160e-03	2.966e-03	4.279e-03	4.845e-03
D to Z	2.141e-03	2.941e-03	4.238e-03	4.783e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

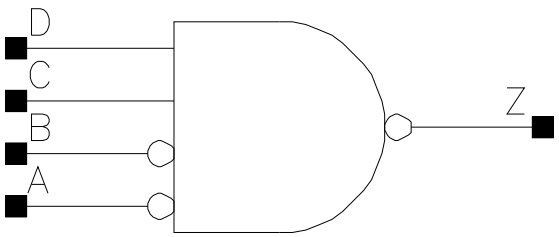
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.952	0.7616
X7_P0	0.800	1.360	1.0880
X10_P0	0.800	2.040	1.6320
X14_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P0	X7_P0	X10_P0	X14_P0
A	0.0006	0.0006	0.0011	0.0009
B	0.0006	0.0006	0.0011	0.0010
C	0.0006	0.0009	0.0013	0.0017
D	0.0004	0.0008	0.0012	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X7_P0	X3_P0	X7_P0
A to Z ↓	0.0319	0.0370	8.8041	4.6368
A to Z ↑	0.0200	0.0230	5.1554	2.5928
B to Z ↓	0.0323	0.0376	8.8057	4.6383
B to Z ↑	0.0188	0.0217	5.1547	2.5913
C to Z ↓	0.0134	0.0134	8.8802	4.6661
C to Z ↑	0.0137	0.0132	5.3353	2.6529

D to Z ↓	0.0133	0.0125	8.8884	4.6725
D to Z ↑	0.0121	0.0109	5.3115	2.6462
	X10_P0	**X14_P0**	**X10_P0**	**X14_P0**
A to Z ↓	0.0348	0.0377	3.1636	2.4109
A to Z ↑	0.0212	0.0266	1.7476	1.2984
B to Z ↓	0.0337	0.0371	3.1634	2.4101
B to Z ↑	0.0194	0.0250	1.7440	1.2948
C to Z ↓	0.0135	0.0131	3.1833	2.4242
C to Z ↑	0.0130	0.0128	1.8072	1.3541
D to Z ↓	0.0128	0.0125	3.1896	2.4289
D to Z ↑	0.0111	0.0107	1.8182	1.3577

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	4.954e-05	1.000e-20
X7_P0	6.306e-05	1.000e-20
X10_P0	1.034e-04	1.000e-20
X14_P0	1.105e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	4.423e-04	5.747e-04	1.028e-03	1.168e-03
B (output stable)	4.102e-04	5.415e-04	9.272e-04	1.077e-03
C (output stable)	2.503e-05	5.473e-05	8.356e-05	1.063e-04
D (output stable)	6.481e-05	1.654e-04	2.003e-04	2.835e-04
A to Z	1.900e-03	3.060e-03	4.822e-03	6.047e-03
B to Z	1.813e-03	2.970e-03	4.452e-03	5.703e-03
C to Z	7.489e-04	1.478e-03	2.130e-03	2.805e-03
D to Z	6.840e-04	1.226e-03	1.824e-03	2.367e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

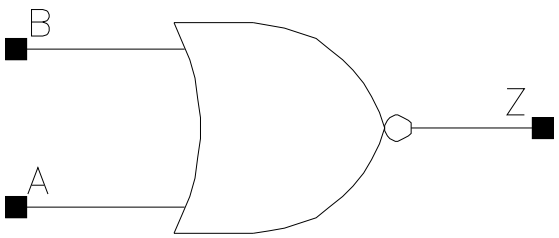
Pin Cycle (vdds)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.408	0.3264
X4_P0	0.800	0.408	0.3264
X8_P0	0.800	0.680	0.5440
X9_P0	1.600	0.408	0.6528
X12_P0	0.800	0.952	0.7616
X16_P0	0.800	1.224	0.9792
X19_P0	1.600	0.680	1.0880
X20_P0	0.800	1.496	1.1968
X23_P0	0.800	1.496	1.1968
X24_P0	0.800	1.768	1.4144
X27_P0	0.800	1.632	1.3056
X29_P0	1.600	0.952	1.5232
X31_P0	0.800	2.312	1.8496
X34_P0	0.800	2.040	1.6320
X38_P0	0.800	2.176	1.7408
X39_P0	1.600	1.224	1.9584
X46_P0	1.600	1.224	1.9584
X57_P0	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P0	X4_P0	X8_P0	X9_P0
A	0.0003	0.0004	0.0009	0.0009
B	0.0003	0.0004	0.0008	0.0009
	X12_P0	X16_P0	X19_P0	X20_P0

A	0.0014	0.0017	0.0019	0.0023
B	0.0012	0.0016	0.0018	0.0020
	X23_P0	X24_P0	X27_P0	X29_P0
A	0.0007	0.0027	0.0007	0.0029
B	0.0006	0.0025	0.0006	0.0027
	X31_P0	X34_P0	X38_P0	X39_P0
A	0.0035	0.0006	0.0007	0.0038
B	0.0033	0.0006	0.0006	0.0036
	X46_P0	X57_P0		
A	0.0006	0.0006		
B	0.0007	0.0007		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X4_P0**	**X2_P0**	**X4_P0**
A to Z ↓	0.0082	0.0077	7.4119	3.8465
A to Z ↑	0.0171	0.0151	20.5695	10.9957
B to Z ↓	0.0074	0.0066	7.4485	3.8747
B to Z ↑	0.0181	0.0157	20.6049	11.0108
	X8_P0	**X9_P0**	**X8_P0**	**X9_P0**
A to Z ↓	0.0070	0.0061	1.8568	1.4350
A to Z ↑	0.0138	0.0140	5.1576	4.9586
B to Z ↓	0.0048	0.0051	1.8588	1.4793
B to Z ↑	0.0121	0.0146	5.1639	4.9654
	X12_P0	**X16_P0**	**X12_P0**	**X16_P0**
A to Z ↓	0.0072	0.0072	1.2689	0.9466
A to Z ↑	0.0134	0.0137	3.3978	2.5884
B to Z ↓	0.0053	0.0051	1.2784	0.9544
B to Z ↑	0.0125	0.0123	3.4061	2.5942
	X19_P0	**X20_P0**	**X19_P0**	**X20_P0**
A to Z ↓	0.0067	0.0074	0.7212	0.7740
A to Z ↑	0.0155	0.0136	2.5283	2.0596
B to Z ↓	0.0051	0.0055	0.7268	0.7803
B to Z ↑	0.0144	0.0126	2.5312	2.0643
	X23_P0	**X24_P0**	**X23_P0**	**X24_P0**
A to Z ↓	0.0296	0.0072	0.7865	0.6423
A to Z ↑	0.0413	0.0135	1.0793	1.7341
B to Z ↓	0.0280	0.0052	0.7861	0.6480
B to Z ↑	0.0416	0.0123	1.0795	1.7372
	X27_P0	**X29_P0**	**X27_P0**	**X29_P0**
A to Z ↓	0.0309	0.0063	0.6557	0.4789
A to Z ↑	0.0426	0.0145	0.9016	1.6956
B to Z ↓	0.0293	0.0048	0.6554	0.4822
B to Z ↑	0.0430	0.0140	0.9009	1.6985
	X31_P0	**X34_P0**	**X31_P0**	**X34_P0**
A to Z ↓	0.0074	0.0323	0.4814	0.5368
A to Z ↑	0.0136	0.0479	1.3009	0.7411
B to Z ↓	0.0054	0.0309	0.4854	0.5364
B to Z ↑	0.0125	0.0485	1.3033	0.7409
	X38_P0	**X39_P0**	**X38_P0**	**X39_P0**
A to Z ↓	0.0333	0.0065	0.4684	0.3644
A to Z ↑	0.0488	0.0148	0.6489	1.2738

B to Z ↓	0.0317	0.0049	0.4676	0.3681
B to Z ↑	0.0493	0.0138	0.6501	1.2754
	X46_P0	**X57_P0**	**X46_P0**	**X57_P0**
A to Z ↓	0.0379	0.0408	0.3476	0.2837
A to Z ↑	0.0511	0.0534	0.6441	0.5167
B to Z ↓	0.0368	0.0396	0.3474	0.2836
B to Z ↑	0.0525	0.0548	0.6440	0.5178

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P0	1.277e-05	1.000e-20
X4_P0	2.853e-05	1.000e-20
X8_P0	5.920e-05	1.000e-20
X9_P0	7.176e-05	1.000e-20
X12_P0	8.524e-05	1.000e-20
X16_P0	1.114e-04	1.000e-20
X19_P0	1.376e-04	1.000e-20
X20_P0	1.375e-04	1.000e-20
X23_P0	2.213e-04	1.000e-20
X24_P0	1.636e-04	1.000e-20
X27_P0	2.500e-04	1.000e-20
X29_P0	1.998e-04	1.000e-20
X31_P0	2.159e-04	1.000e-20
X34_P0	3.070e-04	1.000e-20
X38_P0	3.349e-04	1.000e-20
X39_P0	2.622e-04	1.000e-20
X46_P0	3.617e-04	1.000e-20
X57_P0	4.244e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P0	X4_P0	X8_P0	X9_P0
A (output stable)	8.917e-06	1.576e-05	6.416e-05	3.530e-05
B (output stable)	1.538e-05	2.738e-05	1.525e-04	6.269e-05
A to Z	3.820e-04	6.506e-04	1.291e-03	1.376e-03
B to Z	3.355e-04	5.585e-04	9.576e-04	1.193e-03
	X12_P0	X16_P0	X19_P0	X20_P0
A (output stable)	8.946e-05	1.272e-04	1.359e-04	1.500e-04
B (output stable)	1.880e-04	2.854e-04	3.505e-04	2.962e-04
A to Z	1.906e-03	2.558e-03	2.960e-03	3.192e-03
B to Z	1.496e-03	1.942e-03	2.382e-03	2.491e-03
	X23_P0	X24_P0	X27_P0	X29_P0
A (output stable)	1.786e-05	1.843e-04	1.755e-05	1.738e-04
B (output stable)	3.018e-05	3.827e-04	3.132e-05	3.534e-04
A to Z	5.456e-03	3.777e-03	6.146e-03	4.158e-03
B to Z	5.365e-03	2.899e-03	6.057e-03	3.416e-03
	X31_P0	X34_P0	X38_P0	X39_P0
A (output stable)	2.470e-04	1.855e-05	1.905e-05	2.607e-04
B (output stable)	5.157e-04	3.300e-05	3.332e-05	5.861e-04
A to Z	5.043e-03	8.180e-03	8.962e-03	5.626e-03
B to Z	3.900e-03	8.081e-03	8.853e-03	4.523e-03
	X46_P0	X57_P0		

A (output stable)	1.905e-05	1.905e-05		
B (output stable)	3.350e-05	3.368e-05		
A to Z	1.003e-02	1.230e-02		
B to Z	9.957e-03	1.222e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

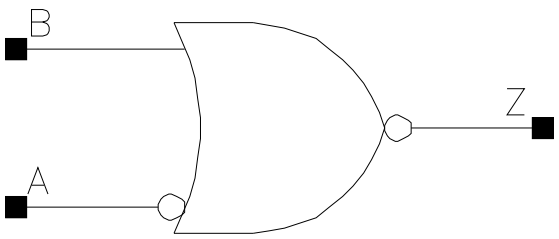
Pin Cycle (vdds)	X2_P0	X4_P0	X8_P0	X9_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P0	X16_P0	X19_P0	X20_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P0	X24_P0	X27_P0	X29_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P0	X34_P0	X38_P0	X39_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P0	X57_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.544	0.4352
X3_P0	0.800	0.544	0.4352
X4_P0	0.800	0.544	0.4352
X10_P0	1.600	0.544	0.8704
X14_P0	1.600	0.816	1.3056
X19_P0	1.600	0.816	1.3056
X29_P0	1.600	1.088	1.7408
X39_P0	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P0	X3_P0	X4_P0	X10_P0
A	0.0005	0.0005	0.0005	0.0008
B	0.0003	0.0003	0.0004	0.0009
	X14_P0	X19_P0	X29_P0	X39_P0
A	0.0008	0.0008	0.0013	0.0013
B	0.0014	0.0017	0.0027	0.0035

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	X3_P0	X2_P0	X3_P0
A to Z ↓	0.0240	0.0241	7.2370	5.3271
A to Z ↑	0.0223	0.0221	20.4497	17.2505
B to Z ↓	0.0071	0.0060	7.4997	5.5158

B to Z ↑	0.0172	0.0165	20.5879	17.3432
	X4_P0	**X10_P0**	**X4_P0**	**X10_P0**
A to Z ↓	0.0247	0.0239	4.0140	1.3839
A to Z ↑	0.0219	0.0208	12.4067	4.8979
B to Z ↓	0.0057	0.0051	4.1598	1.4103
B to Z ↑	0.0148	0.0150	12.4726	4.9263
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0288	0.0302	0.8910	0.6895
A to Z ↑	0.0242	0.0246	3.3492	2.4595
B to Z ↓	0.0046	0.0044	0.9772	0.7587
B to Z ↑	0.0140	0.0129	3.3725	2.4782
	X29_P0	**X39_P0**	**X29_P0**	**X39_P0**
A to Z ↓	0.0264	0.0304	0.4654	0.3495
A to Z ↑	0.0234	0.0253	1.6927	1.2494
B to Z ↓	0.0048	0.0043	0.4834	0.3765
B to Z ↑	0.0139	0.0128	1.7041	1.2582

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P0	2.420e-05	1.000e-20
X3_P0	2.865e-05	1.000e-20
X4_P0	3.762e-05	1.000e-20
X10_P0	1.083e-04	1.000e-20
X14_P0	1.284e-04	1.000e-20
X19_P0	1.728e-04	1.000e-20
X29_P0	2.658e-04	1.000e-20
X39_P0	3.339e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P0	X3_P0	X4_P0	X10_P0
A (output stable)	5.381e-04	5.767e-04	6.339e-04	1.282e-03
B (output stable)	1.552e-05	1.806e-05	2.540e-05	6.616e-05
A to Z	8.974e-04	9.827e-04	1.137e-03	2.594e-03
B to Z	3.164e-04	3.652e-04	4.563e-04	1.245e-03
	X14_P0	X19_P0	X29_P0	X39_P0
A (output stable)	1.828e-03	2.012e-03	3.158e-03	4.015e-03
B (output stable)	9.946e-05	1.328e-04	3.545e-04	2.562e-04
A to Z	3.780e-03	4.537e-03	7.158e-03	9.073e-03
B to Z	1.676e-03	2.120e-03	3.386e-03	4.185e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

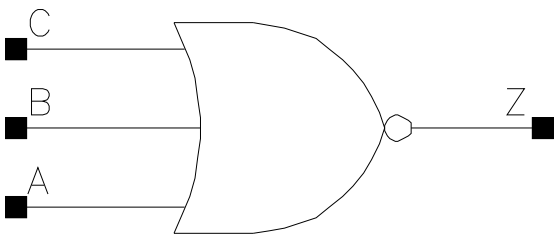
Pin Cycle (vdds)	X2_P0	X3_P0	X4_P0	X10_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P0	X19_P0	X29_P0	X39_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description
3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.544	0.4352
X7_P0	0.800	0.952	0.7616
X11_P0	0.800	1.360	1.0880
X14_P0	0.800	1.768	1.4144
X21_P0	0.800	2.584	2.0672
X29_P0	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X11_P0	X14_P0
A	0.0005	0.0008	0.0013	0.0018
B	0.0005	0.0010	0.0013	0.0019
C	0.0005	0.0008	0.0012	0.0016
	X21_P0	X29_P0		
A	0.0029	0.0037		
B	0.0028	0.0037		
C	0.0024	0.0032		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X7_P0	X3_P0	X7_P0
A to Z ↓	0.0087	0.0087	3.9064	2.0379
A to Z ↑	0.0195	0.0199	15.4631	7.9127

B to Z ↓	0.0082	0.0080	3.9268	1.9727
B to Z ↑	0.0192	0.0201	15.4855	7.9238
C to Z ↓	0.0072	0.0057	3.9769	1.9927
C to Z ↑	0.0189	0.0159	15.4908	7.9188
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0087	0.0087	1.2784	0.9775
A to Z ↑	0.0203	0.0196	5.1843	3.7920
B to Z ↓	0.0082	0.0080	1.2915	0.9526
B to Z ↑	0.0189	0.0196	5.1911	3.7979
C to Z ↓	0.0063	0.0059	1.2866	0.9688
C to Z ↑	0.0173	0.0160	5.1897	3.7958
	X21_P0	**X29_P0**	**X21_P0**	**X29_P0**
A to Z ↓	0.0086	0.0087	0.6512	0.4890
A to Z ↑	0.0194	0.0195	2.5436	1.9123
B to Z ↓	0.0080	0.0081	0.6415	0.4847
B to Z ↑	0.0193	0.0193	2.5469	1.9145
C to Z ↓	0.0062	0.0062	0.6534	0.4934
C to Z ↑	0.0162	0.0162	2.5467	1.9148

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	2.349e-05	1.000e-20
X7_P0	4.607e-05	1.000e-20
X11_P0	6.863e-05	1.000e-20
X14_P0	9.389e-05	1.000e-20
X21_P0	1.375e-04	1.000e-20
X29_P0	1.821e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	1.822e-05	4.446e-05	8.079e-05	9.196e-05
B (output stable)	2.017e-05	6.333e-05	8.483e-05	1.260e-04
C (output stable)	4.853e-05	1.853e-04	2.157e-04	3.644e-04
A to Z	7.794e-04	1.567e-03	2.471e-03	3.227e-03
B to Z	6.738e-04	1.385e-03	2.010e-03	2.840e-03
C to Z	5.778e-04	1.001e-03	1.662e-03	2.102e-03
	X21_P0	X29_P0		
A (output stable)	1.340e-04	1.787e-04		
B (output stable)	1.817e-04	2.462e-04		
C (output stable)	5.064e-04	6.791e-04		
A to Z	4.782e-03	6.383e-03		
B to Z	4.168e-03	5.564e-03		
C to Z	3.145e-03	4.202e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

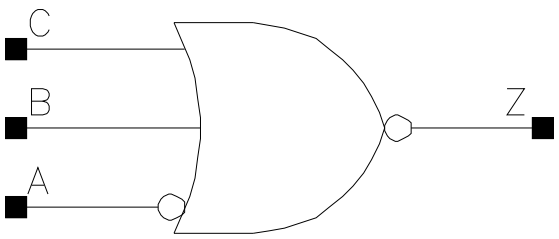
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P0	X29_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X7_P0	0.800	1.360	1.0880
X11_P0	0.800	1.632	1.3056
X14_P0	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X11_P0	X14_P0
A	0.0006	0.0006	0.0008	0.0011
B	0.0005	0.0009	0.0012	0.0017
C	0.0005	0.0008	0.0012	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0265	0.0234	3.7725	1.7735
A to Z ↑	0.0293	0.0288	15.5146	7.5374
B to Z ↓	0.0082	0.0081	3.9436	1.8692
B to Z ↑	0.0191	0.0199	15.5715	7.5656
C to Z ↓	0.0072	0.0061	3.9849	1.8785
C to Z ↑	0.0188	0.0166	15.5789	7.5600
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0284	0.0226	1.2467	0.9232

A to Z ↑	0.0321	0.0281	5.1848	3.8418
B to Z ↓	0.0081	0.0079	1.2929	0.9654
B to Z ↑	0.0187	0.0189	5.2038	3.8576
C to Z ↓	0.0061	0.0059	1.2884	0.9731
C to Z ↑	0.0169	0.0162	5.2028	3.8565

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	3.577e-05	1.000e-20
X7_P0	8.172e-05	1.000e-20
X11_P0	9.657e-05	1.000e-20
X14_P0	1.469e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	6.766e-04	1.181e-03	1.525e-03	2.165e-03
B (output stable)	2.078e-05	7.061e-05	8.902e-05	1.342e-04
C (output stable)	4.883e-05	2.040e-04	2.170e-04	3.520e-04
A to Z	1.439e-03	2.974e-03	4.018e-03	5.574e-03
B to Z	6.665e-04	1.443e-03	2.002e-03	2.712e-03
C to Z	5.722e-04	1.102e-03	1.628e-03	2.095e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

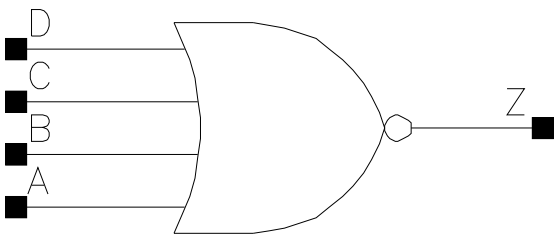
Pin Cycle (vdds)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.224	0.9792
X10_P0	0.800	1.632	1.3056
X14_P0	0.800	1.904	1.5232
X18_P0	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X18_P0
A	0.0004	0.0003	0.0004	0.0005
B	0.0005	0.0005	0.0006	0.0006
C	0.0004	0.0004	0.0004	0.0005
D	0.0005	0.0004	0.0005	0.0005

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0287	0.0334	3.7505	1.7958
A to Z ↑	0.0489	0.0544	5.4526	2.6208
B to Z ↓	0.0280	0.0336	3.7464	1.7955
B to Z ↑	0.0501	0.0574	5.4537	2.6206
C to Z ↓	0.0301	0.0342	3.7487	1.7905
C to Z ↑	0.0528	0.0592	5.4447	2.6184

D to Z ↓	0.0299	0.0331	3.7414	1.7916
D to Z ↑	0.0549	0.0599	5.4473	2.6189
	X14_P0	**X18_P0**	**X14_P0**	**X18_P0**
A to Z ↓	0.0316	0.0331	1.2337	0.9808
A to Z ↑	0.0487	0.0472	1.7953	1.3567
B to Z ↓	0.0312	0.0321	1.2322	0.9810
B to Z ↑	0.0506	0.0481	1.7952	1.3571
C to Z ↓	0.0308	0.0332	1.2296	0.9781
C to Z ↑	0.0490	0.0482	1.7930	1.3543
D to Z ↓	0.0299	0.0319	1.2280	0.9780
D to Z ↑	0.0501	0.0489	1.7904	1.3527

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	7.007e-05	1.000e-20
X10_P0	1.058e-04	1.000e-20
X14_P0	1.587e-04	1.000e-20
X18_P0	2.117e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	2.790e-04	3.538e-04	4.368e-04	5.439e-04
B (output stable)	2.627e-04	3.443e-04	4.175e-04	5.109e-04
C (output stable)	3.039e-04	3.489e-04	4.501e-04	5.673e-04
D (output stable)	2.910e-04	3.315e-04	4.259e-04	5.325e-04
A to Z	1.980e-03	3.152e-03	4.376e-03	5.578e-03
B to Z	1.932e-03	3.114e-03	4.311e-03	5.492e-03
C to Z	2.074e-03	3.131e-03	4.144e-03	5.317e-03
D to Z	2.044e-03	3.082e-03	4.082e-03	5.222e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

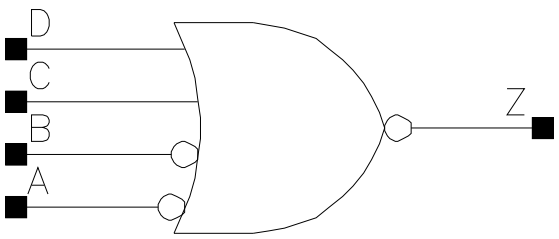
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	1.224	0.9792
X7_P0	0.800	1.496	1.1968
X11_P0	0.800	2.040	1.6320
X14_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P0	X7_P0	X11_P0	X14_P0
A	0.0006	0.0006	0.0011	0.0011
B	0.0006	0.0006	0.0011	0.0011
C	0.0004	0.0009	0.0012	0.0017
D	0.0004	0.0008	0.0012	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X7_P0	X4_P0	X7_P0
A to Z ↓	0.0265	0.0270	3.5012	1.8069
A to Z ↑	0.0369	0.0354	14.8416	7.6224
B to Z ↓	0.0247	0.0251	3.4992	1.8045
B to Z ↑	0.0373	0.0358	14.8430	7.6240
C to Z ↓	0.0084	0.0080	3.6055	1.8844
C to Z ↑	0.0203	0.0197	14.8730	7.6530

D to Z ↓	0.0074	0.0060	3.6232	1.8807
D to Z ↑	0.0199	0.0167	14.8751	7.6475
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0245	0.0268	1.2329	0.9298
A to Z ↑	0.0326	0.0355	5.1375	3.8316
B to Z ↓	0.0223	0.0249	1.2305	0.9277
B to Z ↑	0.0329	0.0363	5.1384	3.8322
C to Z ↓	0.0081	0.0082	1.2921	0.9662
C to Z ↑	0.0187	0.0191	5.1542	3.8442
D to Z ↓	0.0062	0.0061	1.2888	0.9657
D to Z ↑	0.0170	0.0164	5.1538	3.8429

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	5.279e-05	1.000e-20
X7_P0	6.961e-05	1.000e-20
X11_P0	1.110e-04	1.000e-20
X14_P0	1.272e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X7_P0	X11_P0	X14_P0
A (output stable)	5.637e-04	6.276e-04	1.024e-03	1.208e-03
B (output stable)	5.322e-04	5.958e-04	9.486e-04	1.142e-03
C (output stable)	4.437e-05	6.931e-05	1.007e-04	1.442e-04
D (output stable)	8.542e-05	2.047e-04	2.474e-04	3.957e-04
A to Z	2.392e-03	3.179e-03	4.875e-03	6.284e-03
B to Z	2.248e-03	3.037e-03	4.584e-03	6.006e-03
C to Z	7.566e-04	1.422e-03	2.010e-03	2.748e-03
D to Z	6.664e-04	1.097e-03	1.640e-03	2.144e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

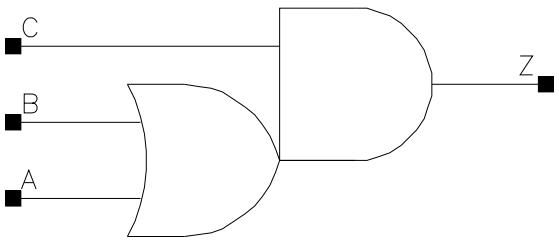
Pin Cycle (vdds)	X4_P0	X7_P0	X11_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.680	0.5440
X10_P0	0.800	0.952	0.7616
X19_P0	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0005	0.0005	0.0010
B	0.0005	0.0006	0.0012
C	0.0006	0.0008	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0260	0.0292	3.6031	1.8008
A to Z ↑	0.0213	0.0252	5.9832	2.6138
B to Z ↓	0.0269	0.0301	3.6040	1.8023
B to Z ↑	0.0198	0.0234	5.9893	2.6149
C to Z ↓	0.0236	0.0254	3.5698	1.7782
C to Z ↑	0.0204	0.0235	5.9839	2.6128
	X19_P0		**X19_P0**	
A to Z ↓	0.0303		0.9358	
A to Z ↑	0.0264		1.3335	

B to Z ↓	0.0312		0.9360	
B to Z ↑	0.0244		1.3310	
C to Z ↓	0.0254		0.9214	
C to Z ↑	0.0237		1.3311	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	5.853e-05	1.000e-20
X10_P0	9.878e-05	1.000e-20
X19_P0	1.858e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	3.079e-05	3.156e-05	6.603e-05
B (output stable)	3.596e-05	3.803e-05	7.506e-05
C (output stable)	3.469e-05	3.574e-05	7.036e-05
A to Z	1.389e-03	2.355e-03	4.769e-03
B to Z	1.306e-03	2.253e-03	4.583e-03
C to Z	1.510e-03	2.385e-03	4.754e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

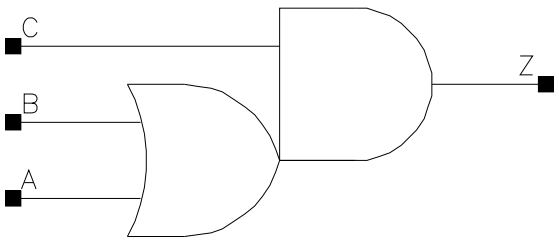
Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	1.360	1.0880
X14_P0	0.800	1.496	1.1968
X19_P0	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0005	0.0011	0.0011	0.0011
B	0.0005	0.0010	0.0010	0.0010
C	0.0006	0.0011	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0320	0.0263	3.5320	1.7874
A to Z ↑	0.0221	0.0201	5.1960	2.5583
B to Z ↓	0.0328	0.0268	3.5323	1.7904
B to Z ↑	0.0206	0.0187	5.1873	2.5524
C to Z ↓	0.0220	0.0178	3.4669	1.7646
C to Z ↑	0.0206	0.0184	5.1872	2.5502
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0294	0.0319	1.2398	0.9364

A to Z ↑	0.0222	0.0239	1.7285	1.2985
B to Z ↓	0.0299	0.0326	1.2396	0.9366
B to Z ↑	0.0209	0.0227	1.7277	1.2960
C to Z ↓	0.0201	0.0219	1.2184	0.9173
C to Z ↑	0.0207	0.0226	1.7248	1.2949

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	6.574e-05	1.000e-20
X10_P0	1.335e-04	1.000e-20
X14_P0	1.601e-04	1.000e-20
X19_P0	1.865e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	1.285e-05	2.666e-05	2.676e-05	2.677e-05
B (output stable)	1.586e-05	3.667e-05	3.691e-05	3.720e-05
C (output stable)	1.061e-04	2.144e-04	2.148e-04	2.161e-04
A to Z	1.744e-03	3.069e-03	4.000e-03	4.909e-03
B to Z	1.646e-03	2.833e-03	3.764e-03	4.679e-03
C to Z	1.473e-03	2.539e-03	3.376e-03	4.174e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

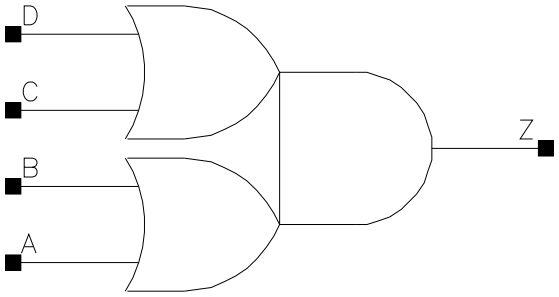
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.952	0.7616
X10_P0	0.800	1.088	0.8704
X14_P0	0.800	1.904	1.5232
X19_P0	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0005	0.0010	0.0010
B	0.0004	0.0006	0.0010	0.0010
C	0.0004	0.0006	0.0011	0.0011
D	0.0004	0.0006	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0454	0.0355	3.6456	1.8201
A to Z ↑	0.0313	0.0262	5.2238	2.6065
B to Z ↓	0.0463	0.0364	3.6470	1.8200

B to Z ↑	0.0301	0.0249	5.2188	2.6016
C to Z ↓	0.0390	0.0316	3.6136	1.8093
C to Z ↑	0.0304	0.0262	5.2181	2.6027
D to Z ↓	0.0398	0.0322	3.6134	1.8100
D to Z ↑	0.0288	0.0245	5.2147	2.6023
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0340	0.0357	1.2554	0.9431
A to Z ↑	0.0249	0.0259	1.7351	1.3025
B to Z ↓	0.0335	0.0352	1.2554	0.9433
B to Z ↑	0.0230	0.0240	1.7305	1.3005
C to Z ↓	0.0290	0.0310	1.2467	0.9374
C to Z ↑	0.0243	0.0254	1.7320	1.3016
D to Z ↓	0.0283	0.0303	1.2479	0.9374
D to Z ↑	0.0220	0.0232	1.7287	1.2980

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	4.813e-05	1.000e-20
X10_P0	1.039e-04	1.000e-20
X14_P0	1.714e-04	1.000e-20
X19_P0	1.955e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	1.260e-05	1.912e-05	5.605e-05	5.510e-05
B (output stable)	1.601e-05	2.599e-05	1.159e-04	1.153e-04
C (output stable)	3.206e-05	4.021e-05	9.660e-05	9.728e-05
D (output stable)	3.685e-05	4.827e-05	1.502e-04	1.512e-04
A to Z	1.806e-03	2.792e-03	4.662e-03	5.406e-03
B to Z	1.745e-03	2.673e-03	4.315e-03	5.057e-03
C to Z	1.587e-03	2.521e-03	4.098e-03	4.836e-03
D to Z	1.531e-03	2.416e-03	3.756e-03	4.484e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

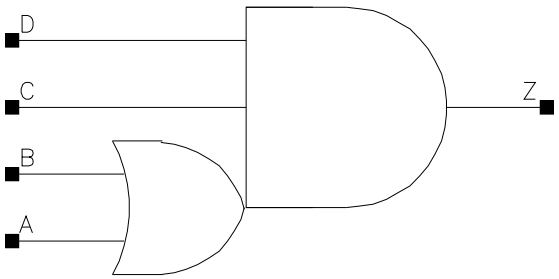
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	0.816	0.6528
X10_P0	0.800	1.088	0.8704
X14_P0	0.800	1.904	1.5232
X19_P0	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0008	0.0009	0.0010
B	0.0004	0.0006	0.0009	0.0011
C	0.0004	0.0006	0.0009	0.0011
D	0.0004	0.0006	0.0009	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X10_P0	X4_P0	X10_P0
A to Z ↓	0.0384	0.0364	3.9809	1.8475
A to Z ↑	0.0353	0.0362	5.5490	2.6514
B to Z ↓	0.0400	0.0344	3.9842	1.8467
B to Z ↑	0.0342	0.0316	5.5485	2.6404
C to Z ↓	0.0318	0.0278	3.8912	1.8163

C to Z ↑	0.0333	0.0316	5.5367	2.6420
D to Z ↓	0.0312	0.0269	3.8915	1.8143
D to Z ↑	0.0352	0.0329	5.5393	2.6421
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0357	0.0336	1.2557	0.9365
A to Z ↑	0.0345	0.0349	1.7678	1.3232
B to Z ↓	0.0348	0.0330	1.2558	0.9362
B to Z ↑	0.0316	0.0319	1.7607	1.3189
C to Z ↓	0.0291	0.0276	1.2340	0.9213
C to Z ↑	0.0316	0.0315	1.7603	1.3190
D to Z ↓	0.0277	0.0263	1.2310	0.9199
D to Z ↑	0.0322	0.0322	1.7610	1.3191

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	4.149e-05	1.000e-20
X10_P0	9.324e-05	1.000e-20
X14_P0	1.366e-04	1.000e-20
X19_P0	1.801e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X10_P0	X14_P0	X19_P0
A (output stable)	3.019e-05	4.576e-05	7.300e-05	8.059e-05
B (output stable)	2.864e-05	5.102e-05	8.733e-05	9.794e-05
C (output stable)	1.090e-05	2.100e-05	5.349e-05	5.918e-05
D (output stable)	1.493e-05	2.480e-05	8.551e-05	9.291e-05
A to Z	1.540e-03	2.826e-03	4.311e-03	5.379e-03
B to Z	1.496e-03	2.597e-03	4.008e-03	5.000e-03
C to Z	1.612e-03	2.789e-03	4.430e-03	5.460e-03
D to Z	1.562e-03	2.704e-03	4.189e-03	5.193e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

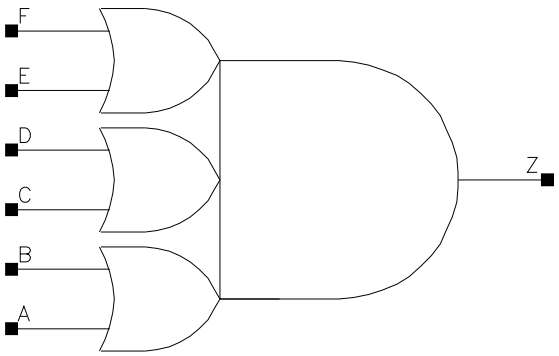
Pin Cycle (vdds)	X4_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	1.360	1.0880
X9_P0	0.800	1.496	1.1968
X19_P0	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P0	X9_P0	X19_P0
A	0.0004	0.0005	0.0009
B	0.0006	0.0008	0.0011
C	0.0004	0.0005	0.0009
D	0.0004	0.0005	0.0011
E	0.0004	0.0005	0.0009
F	0.0004	0.0005	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X9_P0**	**X4_P0**	**X9_P0**
A to Z ↓	0.0537	0.0432	4.0558	1.9933
A to Z ↑	0.0411	0.0375	5.6954	2.7787
B to Z ↓	0.0563	0.0453	4.0556	1.9936
B to Z ↑	0.0411	0.0366	5.6970	2.7770
C to Z ↓	0.0495	0.0395	4.0257	1.9824
C to Z ↑	0.0418	0.0370	5.7014	2.7786
D to Z ↓	0.0502	0.0402	4.0242	1.9813
D to Z ↑	0.0398	0.0350	5.6953	2.7740
E to Z ↓	0.0425	0.0351	3.9797	1.9685
E to Z ↑	0.0382	0.0350	5.6959	2.7764
F to Z ↓	0.0440	0.0363	3.9816	1.9686
F to Z ↑	0.0371	0.0336	5.6896	2.7721
	X19_P0		**X19_P0**	
A to Z ↓	0.0418		0.9536	
A to Z ↑	0.0356		1.3222	
B to Z ↓	0.0432		0.9539	
B to Z ↑	0.0335		1.3188	
C to Z ↓	0.0387		0.9480	
C to Z ↑	0.0357		1.3216	
D to Z ↓	0.0399		0.9479	
D to Z ↑	0.0339		1.3186	
E to Z ↓	0.0343		0.9422	
E to Z ↑	0.0340		1.3211	
F to Z ↓	0.0356		0.9419	
F to Z ↑	0.0322		1.3169	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	4.810e-05	1.000e-20
X9_P0	1.060e-04	1.000e-20
X19_P0	2.069e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X9_P0	X19_P0
A (output stable)	1.193e-05	1.922e-05	3.442e-05
B (output stable)	1.774e-05	2.650e-05	4.457e-05
C (output stable)	1.982e-05	2.686e-05	5.295e-05
D (output stable)	2.358e-05	3.181e-05	6.351e-05
E (output stable)	5.055e-05	6.274e-05	1.178e-04
F (output stable)	5.063e-05	6.798e-05	1.260e-04
A to Z	2.122e-03	3.352e-03	6.528e-03
B to Z	2.086e-03	3.266e-03	6.307e-03
C to Z	1.945e-03	3.091e-03	6.064e-03
D to Z	1.880e-03	2.972e-03	5.840e-03
E to Z	1.703e-03	2.810e-03	5.517e-03
F to Z	1.657e-03	2.716e-03	5.324e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

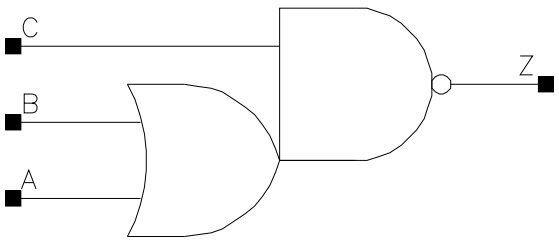
Pin Cycle (vdds)	X4_P0	X9_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.544	0.4352
X10_P0	0.800	1.360	1.0880
X20_P0	0.800	2.720	2.1760
X26_P0	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P0	X10_P0	X20_P0	X26_P0
A	0.0004	0.0013	0.0025	0.0033
B	0.0004	0.0011	0.0023	0.0031
C	0.0004	0.0013	0.0027	0.0036

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X10_P0**	**X3_P0**	**X10_P0**
A to Z ↓	0.0105	0.0117	7.1429	2.2207
A to Z ↑	0.0150	0.0149	12.4807	3.4346
B to Z ↓	0.0089	0.0096	7.0254	2.2326
B to Z ↑	0.0154	0.0140	12.5077	3.4450
C to Z ↓	0.0099	0.0104	6.5228	2.0454
C to Z ↑	0.0146	0.0134	6.5229	1.8090
	X20_P0	**X26_P0**	**X20_P0**	**X26_P0**
A to Z ↓	0.0123	0.0124	1.1327	0.8572

A to Z ↑	0.0156	0.0155	1.7522	1.3182
B to Z ↓	0.0101	0.0102	1.1409	0.8665
B to Z ↑	0.0147	0.0147	1.7574	1.3218
C to Z ↓	0.0111	0.0111	1.0447	0.7916
C to Z ↑	0.0138	0.0137	0.8941	0.6722

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	2.991e-05	1.000e-20
X10_P0	1.025e-04	1.000e-20
X20_P0	2.008e-04	1.000e-20
X26_P0	2.641e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X10_P0	X20_P0	X26_P0
A (output stable)	2.700e-05	1.021e-04	2.074e-04	2.682e-04
B (output stable)	3.233e-05	1.324e-04	2.733e-04	3.537e-04
C (output stable)	3.124e-05	1.077e-04	2.290e-04	2.955e-04
A to Z	5.557e-04	2.080e-03	4.291e-03	5.697e-03
B to Z	4.797e-04	1.636e-03	3.462e-03	4.615e-03
C to Z	6.862e-04	2.377e-03	4.967e-03	6.549e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

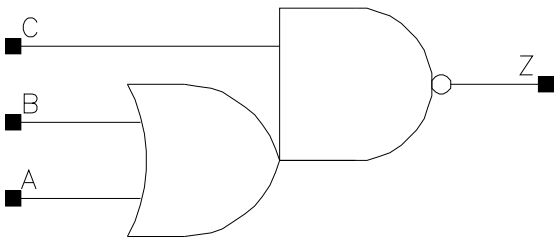
Pin Cycle (vdds)	X3_P0	X10_P0	X20_P0	X26_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X7_P0	0.800	0.952	0.7616
X10_P0	0.800	1.360	1.0880
X13_P0	0.800	1.904	1.5232
X26_P0	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X10_P0	X13_P0
A	0.0005	0.0008	0.0014	0.0018
B	0.0005	0.0009	0.0013	0.0016
C	0.0006	0.0008	0.0012	0.0017
	X26_P0			
A	0.0036			
B	0.0032			
C	0.0033			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X7_P0	X3_P0	X7_P0
A to Z ↓	0.0129	0.0114	6.2160	3.2285
A to Z ↑	0.0202	0.0174	9.9438	5.0848
B to Z ↓	0.0114	0.0095	6.2269	3.1521

B to Z ↑	0.0207	0.0177	9.9615	5.0943
C to Z ↓	0.0112	0.0094	5.8421	2.9843
C to Z ↑	0.0127	0.0106	5.3344	2.7603
	X10_P0	**X13_P0**	**X10_P0**	**X13_P0**
A to Z ↓	0.0109	0.0117	2.1786	1.6596
A to Z ↑	0.0168	0.0183	3.3680	2.5832
B to Z ↓	0.0093	0.0094	2.1710	1.6613
B to Z ↑	0.0170	0.0172	3.3747	2.5888
C to Z ↓	0.0091	0.0092	2.0392	1.5503
C to Z ↑	0.0100	0.0100	1.8259	1.3822
	X26_P0		**X26_P0**	
A to Z ↓	0.0116		0.8543	
A to Z ↑	0.0179		1.3018	
B to Z ↓	0.0093		0.8516	
B to Z ↑	0.0168		1.3053	
C to Z ↓	0.0094		0.7966	
C to Z ↑	0.0098		0.6968	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	3.983e-05	1.000e-20
X7_P0	7.246e-05	1.000e-20
X10_P0	1.053e-04	1.000e-20
X13_P0	1.390e-04	1.000e-20
X26_P0	2.668e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X7_P0	X10_P0	X13_P0
A (output stable)	1.495e-05	2.711e-05	3.946e-05	7.242e-05
B (output stable)	1.816e-05	3.502e-05	5.090e-05	1.186e-04
C (output stable)	1.051e-04	2.112e-04	2.804e-04	4.084e-04
A to Z	1.002e-03	1.618e-03	2.348e-03	3.379e-03
B to Z	8.854e-04	1.412e-03	2.016e-03	2.708e-03
C to Z	7.281e-04	1.232e-03	1.756e-03	2.431e-03
	X26_P0			
A (output stable)	1.399e-04			
B (output stable)	2.149e-04			
C (output stable)	7.342e-04			
A to Z	6.529e-03			
B to Z	5.198e-03			
C to Z	4.687e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P0	X7_P0	X10_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

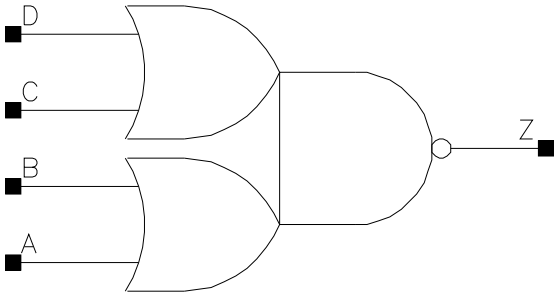
	X26_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X6_P0	0.800	1.360	1.0880
X8_P0	0.800	1.768	1.4144
X11_P0	0.800	2.448	1.9584
X24_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X8_P0	X11_P0
A	0.0004	0.0009	0.0013	0.0017
B	0.0004	0.0008	0.0012	0.0016
C	0.0004	0.0008	0.0012	0.0017
D	0.0004	0.0007	0.0011	0.0015
	X24_P0			
A	0.0037			
B	0.0033			
C	0.0035			
D	0.0032			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X6_P0**	**X3_P0**	**X6_P0**
A to Z ↓	0.0117	0.0141	5.8345	3.1851
A to Z ↑	0.0221	0.0217	12.3876	5.3714
B to Z ↓	0.0106	0.0120	5.7954	3.1920
B to Z ↑	0.0227	0.0206	12.3900	5.3804
C to Z ↓	0.0099	0.0124	5.9006	3.1936
C to Z ↑	0.0157	0.0164	12.4114	5.3960
D to Z ↓	0.0085	0.0099	5.8600	3.2182
D to Z ↑	0.0161	0.0145	12.4281	5.4096
	X8_P0	**X11_P0**	**X8_P0**	**X11_P0**
A to Z ↓	0.0133	0.0135	2.1740	1.6454
A to Z ↑	0.0202	0.0204	3.5958	2.6997
B to Z ↓	0.0116	0.0115	2.1867	1.6469
B to Z ↑	0.0196	0.0196	3.6040	2.7058
C to Z ↓	0.0120	0.0124	2.1882	1.6557
C to Z ↑	0.0151	0.0156	3.5920	2.7157
D to Z ↓	0.0101	0.0100	2.2120	1.6602
D to Z ↑	0.0143	0.0143	3.6041	2.7246
	X24_P0		**X24_P0**	
A to Z ↓	0.0137		0.8017	
A to Z ↑	0.0204		1.3036	
B to Z ↓	0.0117		0.7965	
B to Z ↑	0.0198		1.3069	
C to Z ↓	0.0128		0.8075	
C to Z ↑	0.0156		1.3046	
D to Z ↓	0.0103		0.8044	
D to Z ↑	0.0145		1.3091	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	3.814e-05	1.000e-20
X6_P0	8.594e-05	1.000e-20
X8_P0	1.237e-04	1.000e-20
X11_P0	1.665e-04	1.000e-20
X24_P0	3.219e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X6_P0	X8_P0	X11_P0
A (output stable)	1.708e-05	5.778e-05	7.205e-05	1.019e-04
B (output stable)	2.266e-05	1.180e-04	1.246e-04	1.974e-04
C (output stable)	3.716e-05	9.708e-05	1.239e-04	1.718e-04
D (output stable)	4.527e-05	1.523e-04	1.769e-04	2.653e-04
A to Z	8.979e-04	2.102e-03	2.896e-03	3.916e-03
B to Z	8.011e-04	1.749e-03	2.420e-03	3.263e-03
C to Z	6.198e-04	1.586e-03	2.187e-03	3.025e-03
D to Z	5.424e-04	1.241e-03	1.764e-03	2.412e-03
	X24_P0			
A (output stable)	2.093e-04			
B (output stable)	3.670e-04			
C (output stable)	3.330e-04			
D (output stable)	4.913e-04			

A to Z	8.058e-03			
B to Z	6.724e-03			
C to Z	6.228e-03			
D to Z	4.994e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

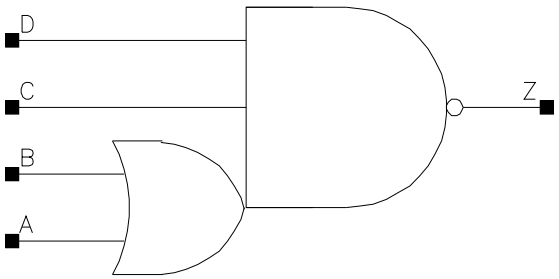
Pin Cycle (vdds)	X3_P0	X6_P0	X8_P0	X11_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X6_P0	0.800	1.360	1.0880
X12_P0	0.800	2.448	1.9584
X18_P0	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X12_P0	X18_P0
A	0.0006	0.0008	0.0016	0.0024
B	0.0004	0.0008	0.0015	0.0023
C	0.0005	0.0009	0.0017	0.0027
D	0.0005	0.0009	0.0017	0.0025

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0201	0.0166	8.7723	4.6693
A to Z ↑	0.0222	0.0178	10.2226	5.1403
B to Z ↓	0.0152	0.0136	8.7587	4.6819
B to Z ↑	0.0193	0.0164	10.2175	5.1553
C to Z ↓	0.0161	0.0158	8.2730	4.4183

C to Z ↑	0.0172	0.0163	5.1606	2.6550
D to Z ↓	0.0176	0.0159	8.3076	4.4345
D to Z ↑	0.0167	0.0150	5.2734	2.6602
	X12_P0	**X18_P0**	**X12_P0**	**X18_P0**
A to Z ↓	0.0169	0.0171	2.4233	1.6377
A to Z ↑	0.0175	0.0174	2.5826	1.7301
B to Z ↓	0.0138	0.0141	2.4319	1.6454
B to Z ↑	0.0161	0.0163	2.5908	1.7367
C to Z ↓	0.0156	0.0158	2.2929	1.5506
C to Z ↑	0.0159	0.0158	1.3525	0.8938
D to Z ↓	0.0159	0.0160	2.3014	1.5560
D to Z ↑	0.0146	0.0146	1.3485	0.9016

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	3.224e-05	1.000e-20
X6_P0	5.916e-05	1.000e-20
X12_P0	1.110e-04	1.000e-20
X18_P0	1.630e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X6_P0	X12_P0	X18_P0
A (output stable)	4.544e-05	8.895e-05	1.660e-04	2.295e-04
B (output stable)	5.123e-05	1.029e-04	1.854e-04	2.568e-04
C (output stable)	1.856e-05	5.740e-05	1.054e-04	1.669e-04
D (output stable)	2.472e-05	8.852e-05	1.499e-04	2.304e-04
A to Z	1.049e-03	1.674e-03	3.273e-03	4.879e-03
B to Z	8.276e-04	1.341e-03	2.599e-03	3.910e-03
C to Z	1.174e-03	2.151e-03	4.085e-03	6.114e-03
D to Z	1.098e-03	1.867e-03	3.571e-03	5.300e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

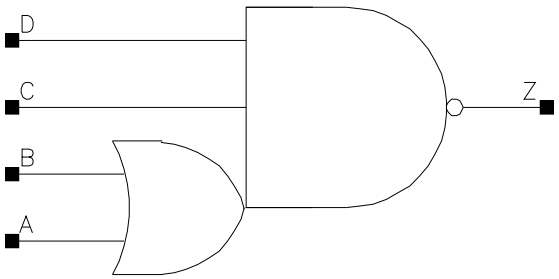
Pin Cycle (vdds)	X3_P0	X6_P0	X12_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X6_P0	0.800	1.360	1.0880
X9_P0	0.800	1.768	1.4144
X12_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X9_P0	X12_P0
A	0.0005	0.0009	0.0014	0.0018
B	0.0004	0.0008	0.0012	0.0019
C	0.0004	0.0008	0.0013	0.0017
D	0.0004	0.0008	0.0012	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0159	0.0164	9.4897	4.6396
A to Z ↑	0.0209	0.0220	10.4372	5.1440
B to Z ↓	0.0140	0.0138	9.3443	4.6536
B to Z ↑	0.0213	0.0211	10.4607	5.1536
C to Z ↓	0.0132	0.0139	8.9602	4.4205

C to Z ↑	0.0133	0.0135	5.5662	2.7391
D to Z ↓	0.0138	0.0135	8.9844	4.4311
D to Z ↑	0.0122	0.0116	5.6177	2.7536
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0165	0.0166	3.1817	2.4129
A to Z ↑	0.0214	0.0217	3.4052	2.6347
B to Z ↓	0.0142	0.0142	3.1818	2.4167
B to Z ↑	0.0207	0.0214	3.4119	2.6417
C to Z ↓	0.0138	0.0139	3.0248	2.2952
C to Z ↑	0.0130	0.0132	1.8135	1.3743
D to Z ↓	0.0137	0.0135	3.0324	2.3011
D to Z ↑	0.0114	0.0111	1.8237	1.3850

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	2.864e-05	1.000e-20
X6_P0	5.991e-05	1.000e-20
X9_P0	8.423e-05	1.000e-20
X12_P0	1.121e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	1.081e-05	2.472e-05	3.901e-05	4.944e-05
B (output stable)	1.165e-05	3.611e-05	4.956e-05	6.769e-05
C (output stable)	2.704e-05	6.522e-05	9.530e-05	1.247e-04
D (output stable)	4.558e-05	1.677e-04	1.868e-04	2.975e-04
A to Z	9.976e-04	2.166e-03	3.148e-03	4.213e-03
B to Z	8.790e-04	1.800e-03	2.609e-03	3.488e-03
C to Z	7.366e-04	1.615e-03	2.300e-03	3.122e-03
D to Z	6.642e-04	1.391e-03	2.021e-03	2.671e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

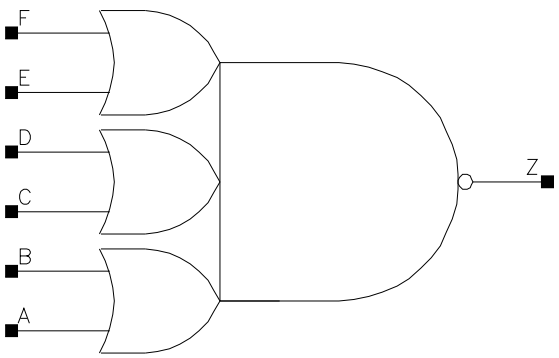
Pin Cycle (vdds)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.224	0.9792
X3_P0	0.800	1.224	0.9792
X5_P0	0.800	2.040	1.6320
X8_P0	0.800	2.720	2.1760
X10_P0	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P0	X3_P0	X5_P0	X8_P0
A	0.0004	0.0005	0.0009	0.0014
B	0.0004	0.0005	0.0008	0.0012
C	0.0004	0.0005	0.0009	0.0013
D	0.0004	0.0004	0.0008	0.0012

E	0.0004	0.0005	0.0008	0.0012
F	0.0003	0.0004	0.0008	0.0012
	X10_P0			
A	0.0018			
B	0.0017			
C	0.0017			
D	0.0016			
E	0.0016			
F	0.0015			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X3_P0**	**X2_P0**	**X3_P0**
A to Z ↓	0.0211	0.0200	10.4580	8.0082
A to Z ↑	0.0307	0.0264	14.3006	9.8515
B to Z ↓	0.0198	0.0187	10.4774	8.0416
B to Z ↑	0.0318	0.0275	14.3093	9.8638
C to Z ↓	0.0208	0.0201	10.5169	8.0406
C to Z ↑	0.0270	0.0237	14.3115	9.9685
D to Z ↓	0.0201	0.0182	10.5863	8.1114
D to Z ↑	0.0290	0.0242	14.3428	9.9760
E to Z ↓	0.0181	0.0176	10.5247	8.0409
E to Z ↑	0.0216	0.0190	14.3080	9.9891
F to Z ↓	0.0170	0.0160	10.5797	8.1148
F to Z ↑	0.0227	0.0195	14.3391	10.0019
	X5_P0	**X8_P0**	**X5_P0**	**X8_P0**
A to Z ↓	0.0212	0.0208	4.2360	2.8876
A to Z ↑	0.0272	0.0262	5.1463	3.4134
B to Z ↓	0.0188	0.0186	4.2523	2.8889
B to Z ↑	0.0263	0.0260	5.1514	3.4181
C to Z ↓	0.0197	0.0202	4.2617	2.9062
C to Z ↑	0.0230	0.0227	5.1835	3.4736
D to Z ↓	0.0174	0.0178	4.2700	2.9061
D to Z ↑	0.0225	0.0228	5.1922	3.4784
E to Z ↓	0.0184	0.0182	4.2730	2.9086
E to Z ↑	0.0190	0.0182	5.1897	3.4808
F to Z ↓	0.0158	0.0157	4.2845	2.9029
F to Z ↑	0.0179	0.0180	5.2002	3.4904
	X10_P0		**X10_P0**	
A to Z ↓	0.0213		2.1882	
A to Z ↑	0.0265		2.5884	
B to Z ↓	0.0189		2.1909	
B to Z ↑	0.0260		2.5926	
C to Z ↓	0.0199		2.1994	
C to Z ↑	0.0227		2.6256	
D to Z ↓	0.0176		2.2027	
D to Z ↑	0.0224		2.6318	
E to Z ↓	0.0185		2.2008	
E to Z ↑	0.0185		2.6216	
F to Z ↓	0.0162		2.2092	
F to Z ↑	0.0179		2.6290	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P0	3.414e-05	1.000e-20
X3_P0	5.399e-05	1.000e-20
X5_P0	9.971e-05	1.000e-20
X8_P0	1.417e-04	1.000e-20
X10_P0	1.877e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P0	X3_P0	X5_P0	X8_P0
A (output stable)	1.531e-05	1.913e-05	5.349e-05	7.142e-05
B (output stable)	1.865e-05	2.440e-05	9.134e-05	1.073e-04
C (output stable)	2.315e-05	2.919e-05	6.850e-05	9.335e-05
D (output stable)	2.729e-05	3.368e-05	1.042e-04	1.228e-04
E (output stable)	5.482e-05	6.894e-05	1.239e-04	1.824e-04
F (output stable)	5.965e-05	7.560e-05	1.598e-04	2.146e-04
A to Z	1.225e-03	1.491e-03	3.004e-03	4.307e-03
B to Z	1.143e-03	1.379e-03	2.621e-03	3.790e-03
C to Z	1.027e-03	1.270e-03	2.434e-03	3.555e-03
D to Z	9.643e-04	1.154e-03	2.125e-03	3.152e-03
E to Z	8.078e-04	1.011e-03	2.023e-03	2.863e-03
F to Z	7.445e-04	9.142e-04	1.710e-03	2.493e-03
	X10_P0			
A (output stable)	1.015e-04			
B (output stable)	1.656e-04			
C (output stable)	1.275e-04			
D (output stable)	1.906e-04			
E (output stable)	2.344e-04			
F (output stable)	2.932e-04			
A to Z	5.817e-03			
B to Z	5.081e-03			
C to Z	4.748e-03			
D to Z	4.154e-03			
E to Z	3.906e-03			
F to Z	3.353e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X2_P0	X3_P0	X5_P0	X8_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P0			

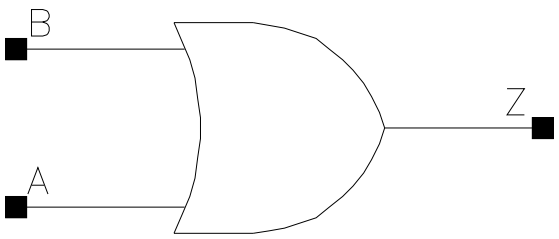
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.544	0.4352
X9_P0	0.800	0.680	0.5440
X19_P0	0.800	1.360	1.0880
X29_P0	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0	X29_P0
A	0.0005	0.0006	0.0010	0.0010
B	0.0004	0.0005	0.0010	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X9_P0**	**X5_P0**	**X9_P0**
A to Z ↓	0.0339	0.0288	3.8311	1.9247
A to Z ↑	0.0205	0.0212	5.4052	2.7115
B to Z ↓	0.0344	0.0289	3.8328	1.9242
B to Z ↑	0.0196	0.0198	5.4093	2.7144
	X19_P0	**X29_P0**	**X19_P0**	**X29_P0**
A to Z ↓	0.0292	0.0343	0.9213	0.6293
A to Z ↑	0.0210	0.0240	1.2923	0.8667
B to Z ↓	0.0282	0.0334	0.9215	0.6291
B to Z ↑	0.0191	0.0221	1.2914	0.8654

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	3.885e-05	1.000e-20
X9_P0	7.778e-05	1.000e-20
X19_P0	1.555e-04	1.000e-20
X29_P0	1.989e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0	X29_P0
A (output stable)	9.555e-06	1.849e-05	6.808e-05	6.812e-05
B (output stable)	1.817e-05	3.064e-05	1.711e-04	1.719e-04
A to Z	1.299e-03	2.089e-03	4.422e-03	6.342e-03
B to Z	1.245e-03	1.997e-03	4.069e-03	5.967e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

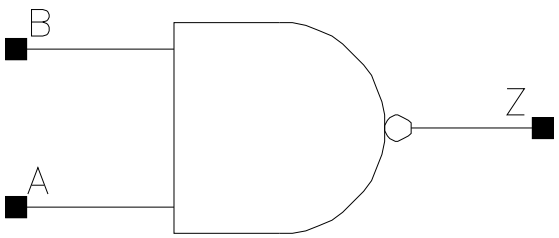
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0	X29_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X9_P0	0.800	0.952	0.7616
X14_P0	0.800	1.088	0.8704
X18_P0	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P0	X9_P0	X14_P0	X18_P0
A	0.0006	0.0005	0.0005	0.0005
B	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X9_P0**	**X5_P0**	**X9_P0**
A to Z ↓	0.0265	0.0303	3.4552	1.8913
A to Z ↑	0.0286	0.0316	5.1672	2.7220
B to Z ↓	0.0275	0.0321	3.4564	1.8931
B to Z ↑	0.0271	0.0307	5.1699	2.7228
	X14_P0	**X18_P0**	**X14_P0**	**X18_P0**
A to Z ↓	0.0334	0.0356	1.3013	0.9869
A to Z ↑	0.0339	0.0348	1.7999	1.3886
B to Z ↓	0.0351	0.0371	1.3021	0.9878
B to Z ↑	0.0330	0.0339	1.8000	1.3875

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	9.409e-05	1.000e-20
X9_P0	1.133e-04	1.000e-20
X14_P0	1.366e-04	1.000e-20
X18_P0	1.483e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X9_P0	X14_P0	X18_P0
A (output stable)	1.201e-05	1.073e-05	1.118e-05	1.115e-05
B (output stable)	2.103e-05	1.908e-05	1.905e-05	1.801e-05
A to Z	2.281e-03	2.938e-03	3.792e-03	4.314e-03
B to Z	2.214e-03	2.879e-03	3.734e-03	4.255e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

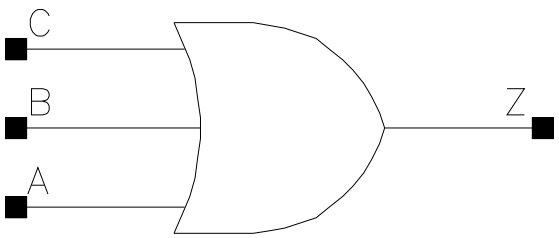
Pin Cycle (vdds)	X5_P0	X9_P0	X14_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.680	0.5440
X10_P0	0.800	0.952	0.7616
X14_P0	0.800	1.496	1.1968
X19_P0	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0006	0.0009	0.0015
B	0.0004	0.0006	0.0011	0.0015
C	0.0004	0.0006	0.0010	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0451	0.0390	3.9581	1.8712
A to Z ↑	0.0241	0.0204	5.4367	2.5747
B to Z ↓	0.0447	0.0387	3.9581	1.8727
B to Z ↑	0.0236	0.0195	5.4384	2.5738
C to Z ↓	0.0451	0.0382	3.9604	1.8726
C to Z ↑	0.0228	0.0183	5.4342	2.5715
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0364	0.0355	1.2517	0.9558

A to Z ↑	0.0188	0.0188	1.7508	1.3403
B to Z ↓	0.0370	0.0347	1.2525	0.9563
B to Z ↑	0.0178	0.0182	1.7474	1.3382
C to Z ↓	0.0334	0.0332	1.2519	0.9560
C to Z ↑	0.0161	0.0165	1.7469	1.3363

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	3.520e-05	1.000e-20
X10_P0	7.419e-05	1.000e-20
X14_P0	1.221e-04	1.000e-20
X19_P0	1.643e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	1.106e-05	2.088e-05	4.463e-05	8.104e-05
B (output stable)	1.256e-05	2.222e-05	6.237e-05	8.521e-05
C (output stable)	2.911e-05	5.290e-05	1.912e-04	2.105e-04
A to Z	1.549e-03	2.557e-03	4.135e-03	5.904e-03
B to Z	1.483e-03	2.441e-03	3.946e-03	5.440e-03
C to Z	1.433e-03	2.341e-03	3.550e-03	5.051e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

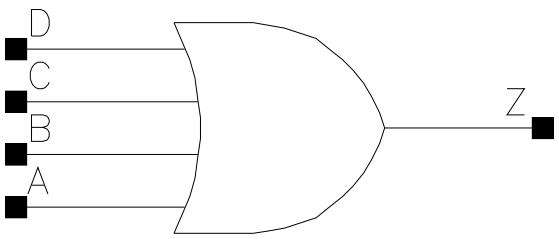
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	1.224	0.9792
X8_P0	0.800	1.496	1.1968
X12_P0	0.800	2.176	1.7408
X15_P0	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X12_P0	X15_P0
A	0.0004	0.0005	0.0010	0.0010
B	0.0004	0.0006	0.0009	0.0011
C	0.0004	0.0005	0.0009	0.0011
D	0.0004	0.0006	0.0009	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0351	0.0328	6.0391	3.1872
A to Z ↑	0.0209	0.0211	5.0350	2.6685
B to Z ↓	0.0365	0.0339	6.0381	3.1871
B to Z ↑	0.0201	0.0202	5.0395	2.6662
C to Z ↓	0.0380	0.0323	6.0500	3.1812
C to Z ↑	0.0220	0.0207	5.1664	2.6798

D to Z ↓	0.0399	0.0336	6.0461	3.1788
D to Z ↑	0.0215	0.0199	5.1635	2.6738
	X12_P0	**X15_P0**	**X12_P0**	**X15_P0**
A to Z ↓	0.0332	0.0334	2.1927	1.6477
A to Z ↑	0.0216	0.0205	1.7226	1.3173
B to Z ↓	0.0330	0.0327	2.1930	1.6465
B to Z ↑	0.0204	0.0189	1.7195	1.3159
C to Z ↓	0.0322	0.0321	2.1895	1.6447
C to Z ↑	0.0205	0.0195	1.7168	1.3251
D to Z ↓	0.0320	0.0316	2.1881	1.6433
D to Z ↑	0.0193	0.0180	1.7144	1.3209

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	4.357e-05	1.000e-20
X8_P0	9.524e-05	1.000e-20
X12_P0	1.203e-04	1.000e-20
X15_P0	1.748e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	3.136e-04	5.582e-04	8.492e-04	1.174e-03
B (output stable)	2.983e-04	5.250e-04	7.837e-04	1.075e-03
C (output stable)	3.168e-04	5.354e-04	7.874e-04	1.084e-03
D (output stable)	3.024e-04	5.029e-04	7.239e-04	1.005e-03
A to Z	1.380e-03	2.719e-03	3.832e-03	5.139e-03
B to Z	1.337e-03	2.627e-03	3.618e-03	4.774e-03
C to Z	1.438e-03	2.479e-03	3.493e-03	4.524e-03
D to Z	1.400e-03	2.394e-03	3.289e-03	4.222e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

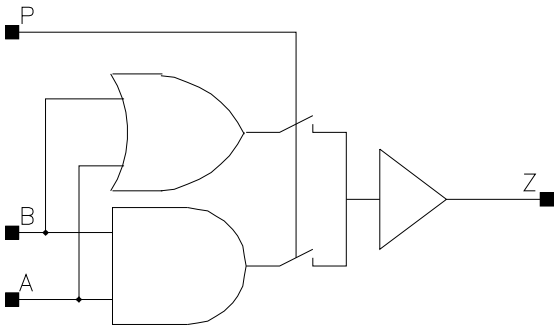
Pin Cycle (vdds)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.952	0.7616
X10_P0	1.600	0.816	1.3056
X14_P0	1.600	1.224	1.9584
X19_P0	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0008	0.0009	0.0018	0.0018
B	0.0008	0.0010	0.0019	0.0019
P	0.0004	0.0006	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0418	0.0372	3.9021	1.8077
A to Z ↑	0.0235	0.0275	5.4448	2.5956
B to Z ↓	0.0416	0.0380	3.9065	1.8139
B to Z ↑	0.0245	0.0288	5.4486	2.5962
P to Z ↓	0.0379	0.0360	3.8998	1.8123
P to Z ↑	0.0233	0.0280	5.4403	2.5956
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**

A to Z ↓	0.0341	0.0364	1.2404	0.9139
A to Z ↑	0.0261	0.0273	1.7716	1.3224
B to Z ↓	0.0324	0.0346	1.2497	0.9195
B to Z ↑	0.0259	0.0273	1.7727	1.3220
P to Z ↓	0.0318	0.0343	1.2519	0.9207
P to Z ↑	0.0260	0.0277	1.7712	1.3220

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	4.924e-05	1.000e-20
X10_P0	1.121e-04	1.000e-20
X14_P0	1.812e-04	1.000e-20
X19_P0	2.137e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	2.731e-05	4.079e-05	1.143e-04	1.087e-04
B (output stable)	3.532e-05	5.870e-05	2.291e-04	2.210e-04
P (output stable)	9.371e-05	1.480e-04	2.863e-04	2.609e-04
A to Z	1.548e-03	2.966e-03	4.698e-03	5.639e-03
B to Z	1.513e-03	2.944e-03	4.456e-03	5.398e-03
P to Z	1.383e-03	2.785e-03	4.392e-03	5.382e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

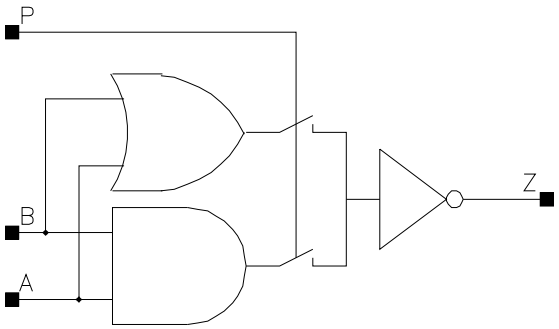
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.600	0.544	0.8704
X10_P0	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P0	X10_P0
A	0.0008	0.0016
B	0.0008	0.0015
P	0.0006	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0141	0.0129	6.0791	3.1721
A to Z ↑	0.0224	0.0205	9.9599	5.0495
B to Z ↓	0.0149	0.0125	6.0275	3.1804
B to Z ↑	0.0225	0.0185	9.9361	5.1013
P to Z ↓	0.0149	0.0120	6.1434	3.2043
P to Z ↑	0.0215	0.0170	10.0078	5.0772

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	5.090e-05	1.000e-20
X10_P0	9.378e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0
A (output stable)	3.832e-05	1.137e-04
B (output stable)	5.266e-05	2.225e-04
P (output stable)	1.279e-04	2.910e-04
A to Z	1.137e-03	1.999e-03
B to Z	1.086e-03	1.728e-03
P to Z	9.478e-04	1.568e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

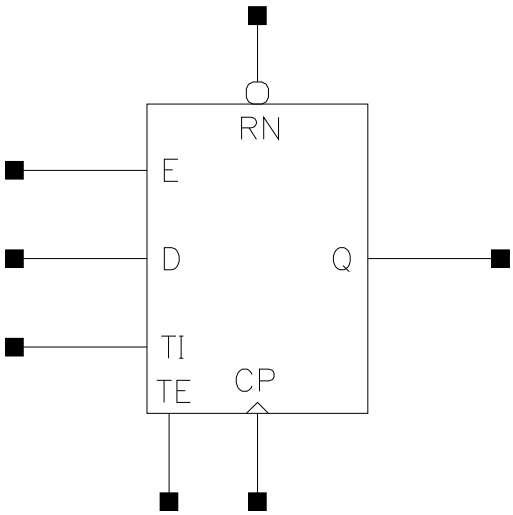
Pin Cycle (vdds)	X5_P0	X10_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.600	2.992	4.7872
X10_P0	1.600	3.128	5.0048
X19_P0	1.600	3.264	5.2224
X23_P0	1.600	3.264	5.2224
X29_P0	1.600	3.536	5.6576
X34_P0	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0	X23_P0
CP	0.0004	0.0005	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
E	0.0010	0.0010	0.0010	0.0010

RN	0.0008	0.0008	0.0008	0.0008
TE	0.0008	0.0008	0.0008	0.0008
TI	0.0003	0.0003	0.0003	0.0003
	X29_P0	X34_P0		
CP	0.0004	0.0004		
D	0.0004	0.0004		
E	0.0010	0.0010		
RN	0.0008	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
CP to Q ↓	0.0533	0.0873	3.5386	1.7752
CP to Q ↑	0.0744	0.1158	5.1091	2.5929
RN to Q ↓	0.0446	0.0838	3.5402	1.7753
	X19_P0	**X23_P0**	**X19_P0**	**X23_P0**
CP to Q ↓	0.0943	0.0950	0.9097	0.6746
CP to Q ↑	0.1203	0.1184	1.3014	1.2786
RN to Q ↓	0.0853	0.0862	0.9061	0.6724
	X29_P0	**X34_P0**	**X29_P0**	**X34_P0**
CP to Q ↓	0.0783	0.0774	0.5932	0.4642
CP to Q ↑	0.0965	0.0972	0.8651	0.8644
RN to Q ↓	0.0708	0.0698	0.5933	0.4642

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P0	X10_P0	X19_P0	X23_P0
CP ↓	min_pulse_width to CP	0.0681	0.0681	0.0681	0.0681
CP ↑	min_pulse_width to CP	0.0488	0.0488	0.0488	0.0488
D ↓	hold_rising to CP	-0.0413	-0.0413	-0.0413	-0.0413
D ↑	hold_rising to CP	-0.0147	-0.0147	-0.0147	-0.0147
D ↓	setup_rising to CP	0.0786	0.0786	0.0786	0.0786
D ↑	setup_rising to CP	0.0422	0.0422	0.0422	0.0422
E ↓	hold_rising to CP	-0.0435	-0.0435	-0.0435	-0.0435
E ↑	hold_rising to CP	-0.0143	-0.0143	-0.0143	-0.0143
E ↓	setup_rising to CP	0.1100	0.1100	0.1100	0.1100
E ↑	setup_rising to CP	0.0786	0.0786	0.0786	0.0786
RN ↓	min_pulse_width to RN	0.0615	0.0544	0.0588	0.0588
RN ↑	recovery_rising to CP	-0.0044	-0.0044	-0.0044	-0.0044
RN ↑	removal_rising to CP	0.0140	0.0140	0.0140	0.0140
TE ↓	hold_rising to CP	-0.0240	-0.0240	-0.0240	-0.0240

TE ↑	hold_rising to CP	-0.0088	-0.0088	-0.0088	-0.0088
TE ↓	setup_rising to CP	0.0635	0.0635	0.0635	0.0635
TE ↑	setup_rising to CP	0.0786	0.0786	0.0786	0.0781
TI ↓	hold_rising to CP	-0.0391	-0.0383	-0.0383	-0.0383
TI ↑	hold_rising to CP	-0.0092	-0.0092	-0.0092	-0.0092
TI ↓	setup_rising to CP	0.0773	0.0770	0.0772	0.0770
TI ↑	setup_rising to CP	0.0332	0.0332	0.0332	0.0332
		X29_P0	X34_P0		
CP ↓	min_pulse_width to CP	0.0681	0.0681		
CP ↑	min_pulse_width to CP	0.0487	0.0487		
D ↓	hold_rising to CP	-0.0413	-0.0413		
D ↑	hold_rising to CP	-0.0121	-0.0147		
D ↓	setup_rising to CP	0.0786	0.0786		
D ↑	setup_rising to CP	0.0422	0.0422		
E ↓	hold_rising to CP	-0.0435	-0.0435		
E ↑	hold_rising to CP	-0.0143	-0.0143		
E ↓	setup_rising to CP	0.1100	0.1100		
E ↑	setup_rising to CP	0.0786	0.0786		
RN ↓	min_pulse_width to RN	0.0588	0.0615		
RN ↑	recovery_rising to CP	-0.0044	-0.0044		
RN ↑	removal_rising to CP	0.0140	0.0140		
TE ↓	hold_rising to CP	-0.0214	-0.0214		
TE ↑	hold_rising to CP	-0.0061	-0.0061		
TE ↓	setup_rising to CP	0.0635	0.0635		
TE ↑	setup_rising to CP	0.0781	0.0781		
TI ↓	hold_rising to CP	-0.0391	-0.0391		
TI ↑	hold_rising to CP	-0.0092	-0.0092		
TI ↓	setup_rising to CP	0.0770	0.0770		
TI ↑	setup_rising to CP	0.0332	0.0332		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	1.977e-04	1.000e-20
X10_P0	2.440e-04	1.000e-20
X19_P0	3.256e-04	1.000e-20
X23_P0	3.411e-04	1.000e-20

X29_P0	4.307e-04	1.000e-20
X34_P0	4.536e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

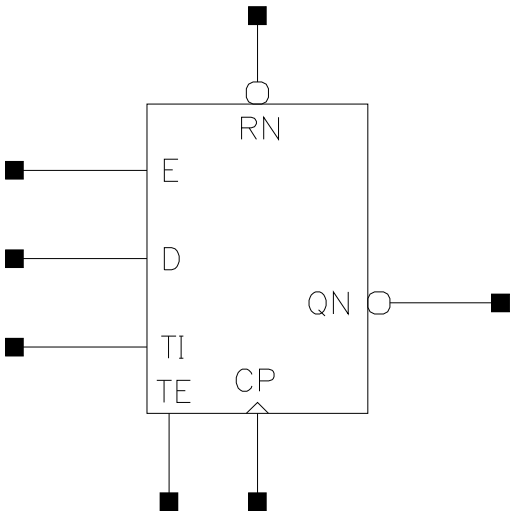
Pin Cycle	X5_P0	X10_P0	X19_P0	X23_P0
Clock 100Mhz Data 0Mhz	6.002e-03	5.993e-03	5.999e-03	6.001e-03
Clock 100Mhz Data 25Mhz	6.225e-03	6.567e-03	7.154e-03	7.198e-03
Clock 100Mhz Data 50Mhz	6.449e-03	7.141e-03	8.310e-03	8.394e-03
Clock = 0 Data 100Mhz	3.498e-03	3.498e-03	3.496e-03	3.496e-03
Clock = 1 Data 100Mhz	1.383e-03	1.382e-03	1.381e-03	1.381e-03
	X29_P0	X34_P0		
Clock 100Mhz Data 0Mhz	6.001e-03	6.002e-03		
Clock 100Mhz Data 25Mhz	7.669e-03	7.821e-03		
Clock 100Mhz Data 50Mhz	9.336e-03	9.640e-03		
Clock = 0 Data 100Mhz	3.496e-03	3.496e-03		
Clock = 1 Data 100Mhz	1.381e-03	1.381e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.600	2.992	4.7872
X10_P0	1.600	3.128	5.0048
X19_P0	1.600	3.264	5.2224
X23_P0	1.600	3.264	5.2224
X29_P0	1.600	3.536	5.6576
X34_P0	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0	X23_P0
CP	0.0004	0.0004	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
E	0.0010	0.0011	0.0011	0.0011

RN	0.0008	0.0007	0.0008	0.0008
TE	0.0008	0.0008	0.0008	0.0008
TI	0.0003	0.0003	0.0003	0.0003
	X29_P0	X34_P0		
CP	0.0005	0.0005		
D	0.0004	0.0004		
E	0.0011	0.0010		
RN	0.0008	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
CP to QN ↓	0.1022	0.0880	3.5545	1.7711
CP to QN ↑	0.0742	0.0672	5.1040	2.5921
RN to QN ↑	0.0704	0.0596	5.1015	2.5904
	X19_P0	**X23_P0**	**X19_P0**	**X23_P0**
CP to QN ↓	0.0919	0.0930	0.9027	0.6747
CP to QN ↑	0.0727	0.0709	1.3031	1.2806
RN to QN ↑	0.0653	0.0633	1.3027	1.2795
	X29_P0	**X34_P0**	**X29_P0**	**X34_P0**
CP to QN ↓	0.1259	0.1231	0.5937	0.4587
CP to QN ↑	0.0975	0.0962	0.8666	0.8633
RN to QN ↑	0.0934	0.0928	0.8646	0.8637

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P0	X10_P0	X19_P0	X23_P0
CP ↓	min_pulse_width to CP	0.0681	0.0681	0.0681	0.0681
CP ↑	min_pulse_width to CP	0.0488	0.0487	0.0487	0.0487
D ↓	hold_rising to CP	-0.0413	-0.0413	-0.0413	-0.0413
D ↑	hold_rising to CP	-0.0147	-0.0147	-0.0121	-0.0121
D ↓	setup_rising to CP	0.0786	0.0786	0.0786	0.0786
D ↑	setup_rising to CP	0.0422	0.0422	0.0422	0.0422
E ↓	hold_rising to CP	-0.0435	-0.0435	-0.0435	-0.0435
E ↑	hold_rising to CP	-0.0143	-0.0143	-0.0143	-0.0143
E ↓	setup_rising to CP	0.1100	0.1100	0.1100	0.1100
E ↑	setup_rising to CP	0.0786	0.0786	0.0786	0.0786
RN ↓	min_pulse_width to RN	0.0566	0.0588	0.0637	0.0637
RN ↑	recovery_rising to CP	-0.0044	-0.0044	-0.0044	-0.0044
RN ↑	removal_rising to CP	0.0140	0.0140	0.0140	0.0140
TE ↓	hold_rising to CP	-0.0240	-0.0214	-0.0214	-0.0214

TE ↑	hold_rising to CP	-0.0088	-0.0088	-0.0061	-0.0061
TE ↓	setup_rising to CP	0.0635	0.0635	0.0635	0.0635
TE ↑	setup_rising to CP	0.0786	0.0781	0.0781	0.0781
TI ↓	hold_rising to CP	-0.0391	-0.0391	-0.0391	-0.0391
TI ↑	hold_rising to CP	-0.0092	-0.0092	-0.0092	-0.0092
TI ↓	setup_rising to CP	0.0770	0.0770	0.0770	0.0770
TI ↑	setup_rising to CP	0.0332	0.0332	0.0332	0.0332
		X29_P0	X34_P0		
CP ↓	min_pulse_width to CP	0.0681	0.0681		
CP ↑	min_pulse_width to CP	0.0488	0.0488		
D ↓	hold_rising to CP	-0.0413	-0.0413		
D ↑	hold_rising to CP	-0.0147	-0.0147		
D ↓	setup_rising to CP	0.0786	0.0786		
D ↑	setup_rising to CP	0.0422	0.0422		
E ↓	hold_rising to CP	-0.0435	-0.0435		
E ↑	hold_rising to CP	-0.0143	-0.0143		
E ↓	setup_rising to CP	0.1100	0.1100		
E ↑	setup_rising to CP	0.0786	0.0786		
RN ↓	min_pulse_width to RN	0.0566	0.0566		
RN ↑	recovery_rising to CP	-0.0040	-0.0040		
RN ↑	removal_rising to CP	0.0140	0.0140		
TE ↓	hold_rising to CP	-0.0240	-0.0240		
TE ↑	hold_rising to CP	-0.0088	-0.0088		
TE ↓	setup_rising to CP	0.0635	0.0635		
TE ↑	setup_rising to CP	0.0786	0.0786		
TI ↓	hold_rising to CP	-0.0426	-0.0383		
TI ↑	hold_rising to CP	-0.0092	-0.0092		
TI ↓	setup_rising to CP	0.0770	0.0770		
TI ↑	setup_rising to CP	0.0332	0.0332		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	1.970e-04	1.000e-20
X10_P0	2.389e-04	1.000e-20
X19_P0	3.191e-04	1.000e-20
X23_P0	3.441e-04	1.000e-20

X29_P0	4.146e-04	1.000e-20
X34_P0	4.511e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

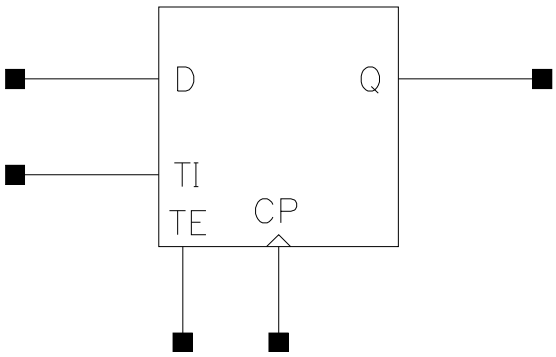
Pin Cycle	X5_P0	X10_P0	X19_P0	X23_P0
Clock 100Mhz Data 0Mhz	5.991e-03	5.998e-03	6.001e-03	6.001e-03
Clock 100Mhz Data 25Mhz	6.263e-03	6.538e-03	7.132e-03	7.202e-03
Clock 100Mhz Data 50Mhz	6.534e-03	7.078e-03	8.264e-03	8.402e-03
Clock = 0 Data 100Mhz	3.498e-03	3.497e-03	3.496e-03	3.495e-03
Clock = 1 Data 100Mhz	1.382e-03	1.381e-03	1.380e-03	1.380e-03
	X29_P0	X34_P0		
Clock 100Mhz Data 0Mhz	6.002e-03	6.003e-03		
Clock 100Mhz Data 25Mhz	7.708e-03	7.847e-03		
Clock 100Mhz Data 50Mhz	9.413e-03	9.690e-03		
Clock = 0 Data 100Mhz	3.495e-03	3.495e-03		
Clock = 1 Data 100Mhz	1.380e-03	1.380e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P0	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P0	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P0	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P0	C8T28SOI_LLHF_-SDFPQX3_P0	C8T28SOIDV_LL_-SDFPQX5_P0	C8T28SOIDV_LL_-SDFPQX10_P0
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P0	C8T28SOIDV_LL_-SDFPQX23_P0	C8T28SOIDV_LL_-SDFPQX29_P0	
CP	0.0004	0.0004	0.0004	
D	0.0004	0.0004	0.0004	
TE	0.0008	0.0008	0.0008	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P0	**C8T28SOI_LLHF_-SDFPQX3_P0**	**C8T28SOI_LL_-SDFPQX5_P0**	**C8T28SOI_LLHF_-SDFPQX3_P0**
CP to Q ↓	0.0561	0.0474	3.7309	5.8482
CP to Q ↑	0.0533	0.0621	5.1682	7.9043
	C8T28SOIDV_LL_-SDFPQX5_P0	**C8T28SOIDV_LL_-SDFPQX10_P0**	**C8T28SOIDV_LL_-SDFPQX5_P0**	**C8T28SOIDV_LL_-SDFPQX10_P0**
CP to Q ↓	0.0494	0.0698	3.5354	1.7261
CP to Q ↑	0.0625	0.0895	5.1102	2.5624
	C8T28SOIDV_LL_-SDFPQX19_P0	**C8T28SOIDV_LL_-SDFPQX23_P0**	**C8T28SOIDV_LL_-SDFPQX19_P0**	**C8T28SOIDV_LL_-SDFPQX23_P0**
CP to Q ↓	0.0754	0.0781	0.8925	0.6703
CP to Q ↑	0.0949	0.0975	1.2913	1.2824
	C8T28SOIDV_LL_-SDFPQX29_P0		**C8T28SOIDV_LL_-SDFPQX29_P0**	
CP to Q ↓	0.0737		0.6010	
CP to Q ↑	0.0899		0.8575	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P0	C8T28SOI_-LLHF_-SDFPQX3_P0	C8T28SOIDV_-LL_SDFPQX5_-P0	C8T28SOIDV_-LL_SDFPQX10_-P0
CP ↓	min_pulse_width to CP	0.0930	0.0902	0.0768	0.0768
CP ↑	min_pulse_width to CP	0.0456	0.0365	0.0408	0.0394
D ↓	hold_rising to CP	-0.0413	-0.0897	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0094	-0.0069	-0.0001	-0.0001
D ↓	setup_rising to CP	0.0759	0.1342	0.0467	0.0467
D ↑	setup_rising to CP	0.0363	0.0395	0.0249	0.0249
TE ↓	hold_rising to CP	-0.0262	-0.0279	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0072	-0.0063	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0738	0.1072	0.0446	0.0446
TE ↑	setup_rising to CP	0.0911	0.1248	0.0911	0.0884

TI ↓	hold_rising to CP	-0.0573	-0.0846	-0.0475	-0.0475
TI ↑	hold_rising to CP	-0.0092	-0.0035	-0.0092	-0.0092
TI ↓	setup_rising to CP	0.0919	0.1209	0.0870	0.0870
TI ↑	setup_rising to CP	0.0332	0.0326	0.0348	0.0348
		C8T28SOIDV_-LL_SDFPQX19_-P0	C8T28SOIDV_-LL_SDFPQX23_-P0	C8T28SOIDV_-LL_SDFPQX29_-P0	
CP ↓	min_pulse_width to CP	0.0768	0.0768	0.0768	
CP ↑	min_pulse_width to CP	0.0394	0.0408	0.0408	
D ↓	hold_rising to CP	-0.0072	-0.0072	-0.0072	
D ↑	hold_rising to CP	-0.0001	-0.0001	-0.0001	
D ↓	setup_rising to CP	0.0467	0.0467	0.0467	
D ↑	setup_rising to CP	0.0249	0.0249	0.0249	
TE ↓	hold_rising to CP	-0.0023	-0.0023	-0.0023	
TE ↑	hold_rising to CP	-0.0071	-0.0071	-0.0071	
TE ↓	setup_rising to CP	0.0446	0.0446	0.0442	
TE ↑	setup_rising to CP	0.0884	0.0884	0.0937	
TI ↓	hold_rising to CP	-0.0475	-0.0475	-0.0473	
TI ↑	hold_rising to CP	-0.0092	-0.0092	-0.0092	
TI ↓	setup_rising to CP	0.0870	0.0870	0.0883	
TI ↑	setup_rising to CP	0.0348	0.0348	0.0348	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P0	1.640e-04	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P0	1.457e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P0	1.555e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P0	2.153e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P0	2.685e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P0	2.894e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P0	3.545e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P0	C8T28SOI_LLHF_-SDFPQX3_P0	C8T28SOIDV_LL_-SDFPQX5_P0	C8T28SOIDV_LL_-SDFPQX10_P0
Clock 100Mhz Data 0Mhz	5.786e-03	5.575e-03	5.312e-03	5.177e-03
Clock 100Mhz Data 25Mhz	5.613e-03	5.401e-03	5.228e-03	5.434e-03
Clock 100Mhz Data 50Mhz	5.440e-03	5.227e-03	5.143e-03	5.691e-03

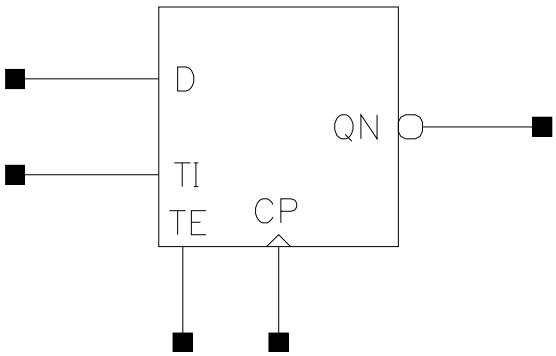
Clock = 0 Data 100Mhz	2.857e-03	3.014e-03	2.813e-03	2.709e-03
Clock = 1 Data 100Mhz	2.770e-05	3.703e-04	2.569e-04	2.003e-04
	C8T28SOIDV_LL_-SDFPQX19_P0	C8T28SOIDV_LL_-SDFPQX23_P0	C8T28SOIDV_LL_-SDFPQX29_P0	
Clock 100Mhz Data 0Mhz	5.099e-03	5.047e-03	5.011e-03	
Clock 100Mhz Data 25Mhz	5.835e-03	5.870e-03	6.242e-03	
Clock 100Mhz Data 50Mhz	6.571e-03	6.692e-03	7.473e-03	
Clock = 0 Data 100Mhz	2.645e-03	2.603e-03	2.574e-03	
Clock = 1 Data 100Mhz	1.664e-04	1.437e-04	1.275e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P0	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P0	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P0	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P0	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P0	C8T28SOI_LLHF_-SDFPQNX3_P0	C8T28SOIDV_LL_-SDFPQNX5_P0	C8T28SOIDV_LL_-SDFPQNX10_P0

CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P0	C8T28SOIDV_LL_-SDFPQNX29_P0		
CP	0.0004	0.0004		
D	0.0004	0.0004		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P0	**C8T28SOI_LLHF_-SDFPQNX3_P0**	**C8T28SOI_LL_-SDFPQNX5_P0**	**C8T28SOI_LLHF_-SDFPQNX3_P0**
CP to QN ↓	0.0692	0.0742	3.6084	5.5487
CP to QN ↑	0.0621	0.0590	5.5966	7.7224
	C8T28SOIDV_LL_-SDFPQNX5_P0	**C8T28SOIDV_LL_-SDFPQNX10_P0**	**C8T28SOIDV_LL_-SDFPQNX5_P0**	**C8T28SOIDV_LL_-SDFPQNX10_P0**
CP to QN ↓	0.0767	0.0721	3.4747	1.7406
CP to QN ↑	0.0569	0.0603	5.0570	2.5621
	C8T28SOIDV_LL_-SDFPQNX19_P0	**C8T28SOIDV_LL_-SDFPQNX29_P0**	**C8T28SOIDV_LL_-SDFPQNX19_P0**	**C8T28SOIDV_LL_-SDFPQNX29_P0**
CP to QN ↓	0.0807	0.0938	0.9005	0.5971
CP to QN ↑	0.0712	0.0801	1.3092	0.8597

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P0	C8T28SOI_-LLHF_-SDFPQNX3_P0	C8T28SOIDV_-LL_SDFPQNX5_-P0	C8T28SOIDV_-LL_-SDFPQNX10_P0
CP ↓	min_pulse_width to CP	0.0913	0.0895	0.0768	0.0768
CP ↑	min_pulse_width to CP	0.0361	0.0364	0.0394	0.0408
D ↓	hold_rising to CP	-0.0413	-0.0897	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0094	-0.0096	-0.0001	-0.0001
D ↓	setup_rising to CP	0.0759	0.1283	0.0467	0.0467
D ↑	setup_rising to CP	0.0363	0.0395	0.0249	0.0249
TE ↓	hold_rising to CP	-0.0262	-0.0279	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0072	-0.0063	-0.0043	-0.0071
TE ↓	setup_rising to CP	0.0738	0.1077	0.0446	0.0446
TE ↑	setup_rising to CP	0.0911	0.1253	0.0911	0.0916
TI ↓	hold_rising to CP	-0.0573	-0.0854	-0.0475	-0.0475
TI ↑	hold_rising to CP	-0.0092	-0.0035	-0.0034	-0.0092
TI ↓	setup_rising to CP	0.0919	0.1193	0.0870	0.0870
TI ↑	setup_rising to CP	0.0332	0.0326	0.0342	0.0348

		C8T28SOIDV_-LL_-SDFPQNX19_P0	C8T28SOIDV_-LL_-SDFPQNX29_P0		
CP ↓	min_pulse_width to CP	0.0768	0.0768		
CP ↑	min_pulse_width to CP	0.0454	0.0394		
D ↓	hold_rising to CP	-0.0072	-0.0072		
D ↑	hold_rising to CP	-0.0001	-0.0001		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0249	0.0249		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0071	-0.0071		
TE ↓	setup_rising to CP	0.0446	0.0446		
TE ↑	setup_rising to CP	0.0916	0.0916		
TI ↓	hold_rising to CP	-0.0475	-0.0475		
TI ↑	hold_rising to CP	-0.0092	-0.0092		
TI ↓	setup_rising to CP	0.0870	0.0870		
TI ↑	setup_rising to CP	0.0348	0.0348		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P0	1.626e-04	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P0	1.478e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P0	1.567e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P0	2.115e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P0	2.694e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P0	4.157e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P0	C8T28SOI_LLHF_-SDFPQNX3_P0	C8T28SOIDV_LL_-SDFPQNX5_P0	C8T28SOIDV_LL_-SDFPQNX10_P0
Clock 100Mhz Data 0Mhz	5.785e-03	5.639e-03	5.359e-03	5.210e-03
Clock 100Mhz Data 25Mhz	5.550e-03	5.454e-03	5.189e-03	5.422e-03
Clock 100Mhz Data 50Mhz	5.315e-03	5.268e-03	5.019e-03	5.633e-03
Clock = 0 Data 100Mhz	2.857e-03	3.029e-03	2.827e-03	2.720e-03
Clock = 1 Data 100Mhz	2.759e-05	3.738e-04	2.592e-04	2.018e-04
	C8T28SOIDV_LL_-SDFPQNX19_P0	C8T28SOIDV_LL_-SDFPQNX29_P0		
Clock 100Mhz Data 0Mhz	5.124e-03	5.065e-03		

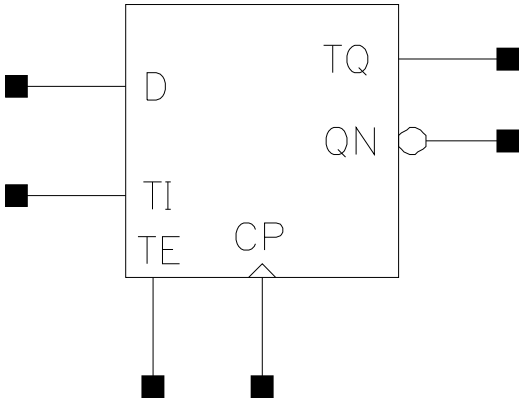
Clock 100Mhz Data 25Mhz	5.948e-03	6.611e-03		
Clock 100Mhz Data 50Mhz	6.772e-03	8.156e-03		
Clock = 0 Data 100Mhz	2.653e-03	2.611e-03		
Clock = 1 Data 100Mhz	1.675e-04	1.447e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P0	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P0	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P0	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P0	C8T28SOI_LLHF_-SDFPQNTX3_P0	C8T28SOIDV_LL_-SDFPQNTX5_P0	C8T28SOIDV_LL_-SDFPQNTX10_P0
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P0	C8T28SOIDV_LL_-SDFPQNTX29_P0		
CP	0.0004	0.0004		
D	0.0004	0.0004		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNTX5_P0	**C8T28SOI_LLHF_-SDFPQNTX3_P0**	**C8T28SOI_LL_-SDFPQNTX5_P0**	**C8T28SOI_LLHF_-SDFPQNTX3_P0**
CP to QN ↓	0.0783	0.0812	3.7368	5.6512
CP to QN ↑	0.0782	0.0719	5.6237	7.7541
CP to TQ ↓	0.0655	0.0501	10.1482	6.6280
CP to TQ ↑	0.0678	0.0612	26.8241	14.1078
	C8T28SOIDV_LL_-SDFPQNTX5_P0	**C8T28SOIDV_LL_-SDFPQNTX10_P0**	**C8T28SOIDV_LL_-SDFPQNTX5_P0**	**C8T28SOIDV_LL_-SDFPQNTX10_P0**
CP to QN ↓	0.0826	0.0799	3.4277	1.7515
CP to QN ↑	0.0665	0.0662	5.0636	2.5654
CP to TQ ↓	0.0464	0.0483	6.6746	6.9010
CP to TQ ↑	0.0626	0.0641	11.1153	11.5161
	C8T28SOIDV_LL_-SDFPQNTX19_P0	**C8T28SOIDV_LL_-SDFPQNTX29_P0**	**C8T28SOIDV_LL_-SDFPQNTX19_P0**	**C8T28SOIDV_LL_-SDFPQNTX29_P0**
CP to QN ↓	0.0819	0.0961	0.8979	0.6011
CP to QN ↑	0.0716	0.0849	1.3032	0.8600
CP to TQ ↓	0.0502	0.0485	6.8196	6.9710
CP to TQ ↑	0.0663	0.0670	11.9066	15.0968

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_P0	C8T28SOI_-LLHF_-SDFPQNTX3_P0	C8T28SOIDV_-LL_-SDFPQNTX5_P0	C8T28SOIDV_-LL_-SDFPQNTX10_-P0
CP ↓	min_pulse_width to CP	0.0930	0.0895	0.0768	0.0768
CP ↑	min_pulse_width to CP	0.0502	0.0423	0.0408	0.0441
D ↓	hold_rising to CP	-0.0413	-0.0897	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0094	-0.0096	-0.0001	-0.0001
D ↓	setup_rising to CP	0.0759	0.1283	0.0467	0.0467

D ↑	setup_rising to CP	0.0363	0.0395	0.0249	0.0249
TE ↓	hold_rising to CP	-0.0230	-0.0279	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0072	-0.0063	-0.0043	-0.0071
TE ↓	setup_rising to CP	0.0738	0.1077	0.0446	0.0446
TE ↑	setup_rising to CP	0.0911	0.1253	0.0911	0.0916
TI ↓	hold_rising to CP	-0.0573	-0.0854	-0.0473	-0.0475
TI ↑	hold_rising to CP	-0.0092	-0.0035	-0.0034	-0.0092
TI ↓	setup_rising to CP	0.0919	0.1193	0.0870	0.0870
TI ↑	setup_rising to CP	0.0332	0.0326	0.0342	0.0348
		C8T28SOIDV_-LL_-SDFPQNTX19_-P0	C8T28SOIDV_-LL_-SDFPQNTX29_-P0		
CP ↓	min_pulse_width to CP	0.0768	0.0768		
CP ↑	min_pulse_width to CP	0.0454	0.0408		
D ↓	hold_rising to CP	-0.0072	-0.0072		
D ↑	hold_rising to CP	-0.0001	-0.0001		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0249	0.0249		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0071	-0.0071		
TE ↓	setup_rising to CP	0.0446	0.0446		
TE ↑	setup_rising to CP	0.0916	0.0911		
TI ↓	hold_rising to CP	-0.0475	-0.0475		
TI ↑	hold_rising to CP	-0.0092	-0.0092		
TI ↓	setup_rising to CP	0.0870	0.0870		
TI ↑	setup_rising to CP	0.0348	0.0348		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P0	1.618e-04	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P0	1.579e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P0	1.676e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P0	2.001e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P0	2.667e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P0	4.158e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

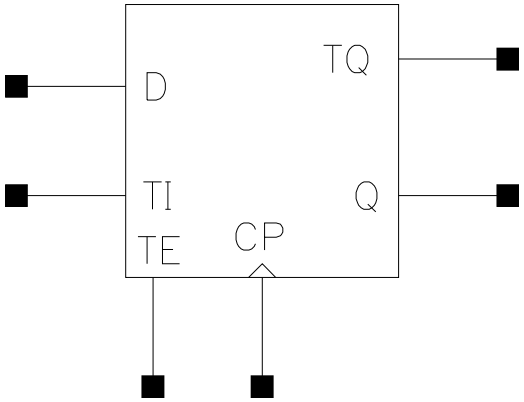
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P0	C8T28SOI_LLHF_-SDFPQNTX3_P0	C8T28SOIDV_LL_-SDFPQNTX5_P0	C8T28SOIDV_LL_-SDFPQNTX10_P0
Clock 100Mhz Data 0Mhz	5.792e-03	5.641e-03	5.358e-03	5.210e-03
Clock 100Mhz Data 25Mhz	5.780e-03	5.637e-03	5.364e-03	5.428e-03
Clock 100Mhz Data 50Mhz	5.768e-03	5.633e-03	5.370e-03	5.645e-03
Clock = 0 Data 100Mhz	2.857e-03	3.032e-03	2.829e-03	2.722e-03
Clock = 1 Data 100Mhz	2.750e-05	3.758e-04	2.607e-04	2.030e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P0	C8T28SOIDV_LL_-SDFPQNTX29_P0		
Clock 100Mhz Data 0Mhz	5.122e-03	5.061e-03		
Clock 100Mhz Data 25Mhz	5.891e-03	6.757e-03		
Clock 100Mhz Data 50Mhz	6.659e-03	8.453e-03		
Clock = 0 Data 100Mhz	2.657e-03	2.614e-03		
Clock = 1 Data 100Mhz	1.686e-04	1.455e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P0	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P0	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P0	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P0	C8T28SOI_LLHF_-SDFPQTX3_P0	C8T28SOIDV_LL_-SDFPQTX5_P0	C8T28SOIDV_LL_-SDFPQTX10_P0
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P0	C8T28SOIDV_LL_-SDFPQTX29_P0		
CP	0.0004	0.0004		
D	0.0004	0.0004		
TE	0.0008	0.0008		
TI	0.0002	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQTX5_P0	**C8T28SOI_LLHF_-SDFPQTX3_P0**	**C8T28SOI_LL_-SDFPQTX5_P0**	**C8T28SOI_LLHF_-SDFPQTX3_P0**
CP to Q ↓	0.0657	0.0612	3.9183	6.0328
CP to Q ↑	0.0577	0.0620	5.1985	8.0123
CP to TQ ↓	0.0791	0.0591	11.0765	6.7931
CP to TQ ↑	0.0749	0.0661	27.2474	14.2987
	C8T28SOIDV_LL_-SDFPQTX5_P0	**C8T28SOIDV_LL_-SDFPQTX10_P0**	**C8T28SOIDV_LL_-SDFPQTX5_P0**	**C8T28SOIDV_LL_-SDFPQTX10_P0**
CP to Q ↓	0.0534	0.0715	3.6108	1.7329
CP to Q ↑	0.0646	0.0911	5.1729	2.5622
CP to TQ ↓	0.0528	0.0737	6.8314	7.0200
CP to TQ ↑	0.0669	0.0949	12.1913	11.9797
	C8T28SOIDV_LL_-SDFPQTX19_P0	**C8T28SOIDV_LL_-SDFPQTX29_P0**	**C8T28SOIDV_LL_-SDFPQTX19_P0**	**C8T28SOIDV_LL_-SDFPQTX29_P0**
CP to Q ↓	0.0769	0.0833	0.8948	0.5857
CP to Q ↑	0.0955	0.0940	1.2973	0.8552
CP to TQ ↓	0.0802	0.0518	7.0697	7.1967
CP to TQ ↑	0.1013	0.0686	12.0128	15.1028

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P0	C8T28SOI_-LLHF_-SDFPQTX3_P0	C8T28SOIDV_-LL_SDFPQTX5_-P0	C8T28SOIDV_-LL_-SDFPQTX10_P0
CP ↓	min_pulse_width to CP	0.0930	0.0895	0.0768	0.0768
CP ↑	min_pulse_width to CP	0.0549	0.0471	0.0455	0.0394
D ↓	hold_rising to CP	-0.0413	-0.0897	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0094	-0.0096	-0.0001	-0.0001
D ↓	setup_rising to CP	0.0759	0.1283	0.0467	0.0467

D ↑	setup_rising to CP	0.0363	0.0395	0.0249	0.0249
TE ↓	hold_rising to CP	-0.0262	-0.0279	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0072	-0.0063	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0738	0.1050	0.0446	0.0446
TE ↑	setup_rising to CP	0.0906	0.1253	0.0911	0.0884
TI ↓	hold_rising to CP	-0.0573	-0.0854	-0.0475	-0.0475
TI ↑	hold_rising to CP	-0.0092	-0.0035	-0.0092	-0.0092
TI ↓	setup_rising to CP	0.0919	0.1200	0.0870	0.0870
TI ↑	setup_rising to CP	0.0332	0.0326	0.0348	0.0348
		C8T28SOIDV_-LL_-SDFPQTX19_P0	C8T28SOIDV_-LL_-SDFPQTX29_P0		
CP ↓	min_pulse_width to CP	0.0768	0.0768		
CP ↑	min_pulse_width to CP	0.0394	0.0454		
D ↓	hold_rising to CP	-0.0072	-0.0072		
D ↑	hold_rising to CP	-0.0001	-0.0001		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0249	0.0249		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0071	-0.0071		
TE ↓	setup_rising to CP	0.0446	0.0442		
TE ↑	setup_rising to CP	0.0884	0.0911		
TI ↓	hold_rising to CP	-0.0475	-0.0475		
TI ↑	hold_rising to CP	-0.0092	-0.0092		
TI ↓	setup_rising to CP	0.0870	0.0883		
TI ↑	setup_rising to CP	0.0348	0.0348		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P0	1.651e-04	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P0	1.579e-04	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P0	1.668e-04	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P0	2.260e-04	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P0	2.817e-04	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P0	3.732e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

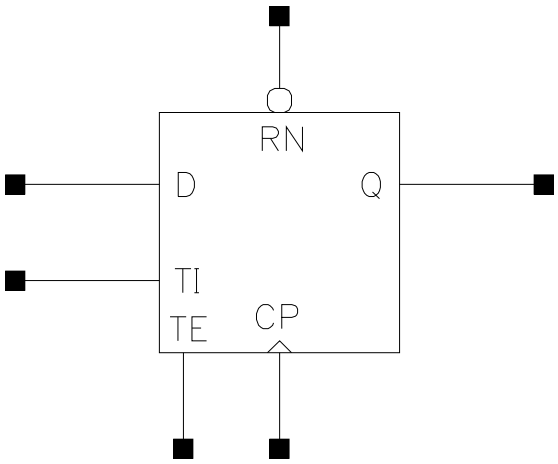
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P0	C8T28SOI_LLHF_-SDFPQTX3_P0	C8T28SOIDV_LL_-SDFPQTX5_P0	C8T28SOIDV_LL_-SDFPQTX10_P0
Clock 100Mhz Data 0Mhz	5.789e-03	5.646e-03	5.360e-03	5.214e-03
Clock 100Mhz Data 25Mhz	5.835e-03	5.665e-03	5.406e-03	5.583e-03
Clock 100Mhz Data 50Mhz	5.881e-03	5.685e-03	5.452e-03	5.951e-03
Clock = 0 Data 100Mhz	2.866e-03	3.033e-03	2.826e-03	2.719e-03
Clock = 1 Data 100Mhz	2.735e-05	3.738e-04	2.592e-04	2.018e-04
	C8T28SOIDV_LL_-SDFPQTX19_P0	C8T28SOIDV_LL_-SDFPQTX29_P0		
Clock 100Mhz Data 0Mhz	5.128e-03	5.074e-03		
Clock 100Mhz Data 25Mhz	6.009e-03	6.466e-03		
Clock 100Mhz Data 50Mhz	6.890e-03	7.858e-03		
Clock = 0 Data 100Mhz	2.653e-03	2.613e-03		
Clock = 1 Data 100Mhz	1.676e-04	1.448e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P0	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P0	C8T28SOI_LLHF_-SDFPRQX3_P0	C8T28SOIDV_LL_-SDFPRQX5_P0	C8T28SOIDV_LL_-SDFPRQX10_P0
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
RN	0.0007	0.0007	0.0008	0.0008
TE	0.0009	0.0009	0.0007	0.0007
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P0	C8T28SOIDV_LL_-SDFPRQX29_P0		
CP	0.0004	0.0004		
D	0.0004	0.0004		
RN	0.0008	0.0008		
TE	0.0007	0.0007		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P0	**C8T28SOI_LLHF_-SDFPRQX3_P0**	**C8T28SOI_LL_-SDFPRQX5_P0**	**C8T28SOI_LLHF_-SDFPRQX3_P0**
CP to Q ↓	0.0645	0.0585	3.7550	5.8936
CP to Q ↑	0.0557	0.0621	5.1726	7.8484
RN to Q ↓	0.0569	0.0558	3.5081	5.5774
	C8T28SOIDV_LL_-SDFPRQX5_P0	**C8T28SOIDV_LL_-SDFPRQX10_P0**	**C8T28SOIDV_LL_-SDFPRQX5_P0**	**C8T28SOIDV_LL_-SDFPRQX10_P0**
CP to Q ↓	0.0500	0.0714	3.5298	1.7457
CP to Q ↑	0.0655	0.0933	5.1054	2.5670
RN to Q ↓	0.0464	0.0724	3.4974	1.7452
	C8T28SOIDV_LL_-SDFPRQX19_P0	**C8T28SOIDV_LL_-SDFPRQX29_P0**	**C8T28SOIDV_LL_-SDFPRQX19_P0**	**C8T28SOIDV_LL_-SDFPRQX29_P0**
CP to Q ↓	0.0762	0.0775	0.8937	0.6111
CP to Q ↑	0.0980	0.1015	1.3097	0.8893
RN to Q ↓	0.0774	0.0788	0.8944	0.6108

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P0	C8T28SOI_-LLHF_-SDFPRQX3_P0	C8T28SOIDV_-LL_SDFPRQX5_-P0	C8T28SOIDV_-LL_-SDFPRQX10_P0
CP ↓	min_pulse_width to CP	0.0930	0.0854	0.0786	0.0786
CP ↑	min_pulse_width to CP	0.0502	0.0457	0.0408	0.0408
D ↓	hold_rising to CP	-0.0387	-0.0848	-0.0077	-0.0077
D ↑	hold_rising to CP	-0.0088	-0.0090	0.0009	0.0009
D ↓	setup_rising to CP	0.0759	0.1293	0.0467	0.0467
D ↑	setup_rising to CP	0.0391	0.0386	0.0266	0.0266
RN ↓	min_pulse_width to RN	0.0620	0.0593	0.0540	0.0518
RN ↑	recovery_rising to CP	0.0032	0.0005	0.0005	0.0005
RN ↑	removal_rising to CP	0.0090	0.0091	0.0091	0.0091

TE ↓	hold_rising to CP	-0.0289	-0.0333	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0093	-0.0063	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0738	0.1024	0.0442	0.0442
TE ↑	setup_rising to CP	0.0906	0.1199	0.0884	0.0884
TI ↓	hold_rising to CP	-0.0557	-0.0798	-0.0439	-0.0439
TI ↑	hold_rising to CP	-0.0092	-0.0078	-0.0098	-0.0098
TI ↓	setup_rising to CP	0.0919	0.1203	0.0870	0.0870
TI ↑	setup_rising to CP	0.0391	0.0332	0.0404	0.0404
		C8T28SOIDV_-LL_-SDFPRQX19_P0	C8T28SOIDV_-LL_-SDFPRQX29_P0		
CP ↓	min_pulse_width to CP	0.0786	0.0786		
CP ↑	min_pulse_width to CP	0.0409	0.0408		
D ↓	hold_rising to CP	-0.0072	-0.0072		
D ↑	hold_rising to CP	0.0009	0.0009		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0266	0.0266		
RN ↓	min_pulse_width to RN	0.0518	0.0518		
RN ↑	recovery_rising to CP	0.0005	-0.0021		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0092	-0.0092		
TE ↓	setup_rising to CP	0.0442	0.0442		
TE ↑	setup_rising to CP	0.0884	0.0884		
TI ↓	hold_rising to CP	-0.0439	-0.0439		
TI ↑	hold_rising to CP	-0.0141	-0.0141		
TI ↓	setup_rising to CP	0.0870	0.0870		
TI ↑	setup_rising to CP	0.0404	0.0404		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P0	1.737e-04	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P0	1.583e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P0	1.668e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P0	2.225e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQX19_P0	2.822e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P0	3.584e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

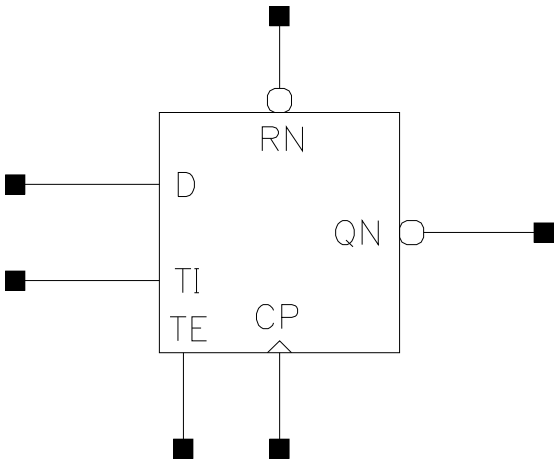
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P0	C8T28SOI_LLHF_-SDFPRQX3_P0	C8T28SOIDV_LL_-SDFPRQX5_P0	C8T28SOIDV_LL_-SDFPRQX10_P0
Clock 100Mhz Data 0Mhz	6.038e-03	5.823e-03	5.522e-03	5.373e-03
Clock 100Mhz Data 25Mhz	5.833e-03	5.645e-03	5.358e-03	5.593e-03
Clock 100Mhz Data 50Mhz	5.628e-03	5.468e-03	5.195e-03	5.812e-03
Clock = 0 Data 100Mhz	2.684e-03	2.877e-03	2.736e-03	2.665e-03
Clock = 1 Data 100Mhz	2.745e-05	3.766e-04	2.607e-04	2.027e-04
	C8T28SOIDV_LL_-SDFPRQX19_P0	C8T28SOIDV_LL_-SDFPRQX29_P0		
Clock 100Mhz Data 0Mhz	5.282e-03	5.223e-03		
Clock 100Mhz Data 25Mhz	5.986e-03	6.553e-03		
Clock 100Mhz Data 50Mhz	6.690e-03	7.884e-03		
Clock = 0 Data 100Mhz	2.623e-03	2.596e-03		
Clock = 1 Data 100Mhz	1.681e-04	1.450e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P0	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P0	C8T28SOI_LLHF_-SDFPRQNX3_P0	C8T28SOIDV_LL_-SDFPRQNX5_P0	C8T28SOIDV_LL_-SDFPRQNX10_P0
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
RN	0.0007	0.0007	0.0008	0.0007
TE	0.0009	0.0009	0.0007	0.0007
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P0	C8T28SOIDV_LL_-SDFPRQNX29_P0		
CP	0.0004	0.0004		
D	0.0004	0.0004		
RN	0.0006	0.0006		
TE	0.0007	0.0007		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNX5_P0	**C8T28SOI_LLHF_-SDFPRQNX3_P0**	**C8T28SOI_LL_-SDFPRQNX5_P0**	**C8T28SOI_LLHF_-SDFPRQNX3_P0**
CP to QN ↓	0.0734	0.0781	3.7103	5.5617
CP to QN ↑	0.0691	0.0646	5.3403	7.7294
RN to QN ↑	0.0674	0.0661	5.3381	7.7103
	C8T28SOIDV_LL_-SDFPRQNX5_P0	**C8T28SOIDV_LL_-SDFPRQNX10_P0**	**C8T28SOIDV_LL_-SDFPRQNX5_P0**	**C8T28SOIDV_LL_-SDFPRQNX10_P0**
CP to QN ↓	0.0838	0.0754	3.4145	1.7452
CP to QN ↑	0.0637	0.0610	5.0519	2.5675
RN to QN ↑	0.0638	0.0575	5.0349	2.5666
	C8T28SOIDV_LL_-SDFPRQNX19_P0	**C8T28SOIDV_LL_-SDFPRQNX29_P0**	**C8T28SOIDV_LL_-SDFPRQNX19_P0**	**C8T28SOIDV_LL_-SDFPRQNX29_P0**
CP to QN ↓	0.0839	0.0899	0.9160	0.6149
CP to QN ↑	0.0677	0.0759	1.3163	0.8858
RN to QN ↑	0.0623	0.0723	1.3147	0.8855

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P0	C8T28SOI_-LLHF_-SDFPRQNX3_-P0	C8T28SOIDV_-LL_-SDFPRQNX5_-P0	C8T28SOIDV_-LL_-SDFPRQNX10_-P0
CP ↓	min_pulse_width to CP	0.0930	0.0854	0.0786	0.0786
CP ↑	min_pulse_width to CP	0.0408	0.0365	0.0408	0.0407
D ↓	hold_rising to CP	-0.0387	-0.0848	-0.0072	-0.0045
D ↑	hold_rising to CP	-0.0088	-0.0090	0.0009	0.0009
D ↓	setup_rising to CP	0.0759	0.1234	0.0467	0.0467
D ↑	setup_rising to CP	0.0391	0.0412	0.0239	0.0266
RN ↓	min_pulse_width to RN	0.0620	0.0593	0.0518	0.0540
RN ↑	recovery_rising to CP	0.0032	0.0005	0.0005	0.0005

RN ↑	removal_rising to CP	0.0090	0.0096	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0289	-0.0333	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0093	-0.0095	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0738	0.1024	0.0442	0.0442
TE ↑	setup_rising to CP	0.0906	0.1204	0.0884	0.0884
TI ↓	hold_rising to CP	-0.0573	-0.0798	-0.0439	-0.0439
TI ↑	hold_rising to CP	-0.0085	-0.0078	-0.0098	-0.0098
TI ↓	setup_rising to CP	0.0919	0.1187	0.0870	0.0870
TI ↑	setup_rising to CP	0.0391	0.0332	0.0388	0.0388
		C8T28SOIDV_-LL_-SDFPRQNX19_-P0	C8T28SOIDV_-LL_-SDFPRQNX29_-P0		
CP ↓	min_pulse_width to CP	0.0799	0.0816		
CP ↑	min_pulse_width to CP	0.0441	0.0500		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0004	-0.0000		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0240	0.0240		
RN ↓	min_pulse_width to RN	0.0588	0.0708		
RN ↑	recovery_rising to CP	-0.0021	-0.0017		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0001	-0.0001		
TE ↑	hold_rising to CP	-0.0092	-0.0092		
TE ↓	setup_rising to CP	0.0442	0.0442		
TE ↑	setup_rising to CP	0.0884	0.0884		
TI ↓	hold_rising to CP	-0.0424	-0.0426		
TI ↑	hold_rising to CP	-0.0098	-0.0098		
TI ↓	setup_rising to CP	0.0870	0.0870		
TI ↑	setup_rising to CP	0.0388	0.0388		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P0	1.716e-04	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P0	1.604e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P0	1.659e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P0	2.203e-04	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P0	2.653e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P0	3.429e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

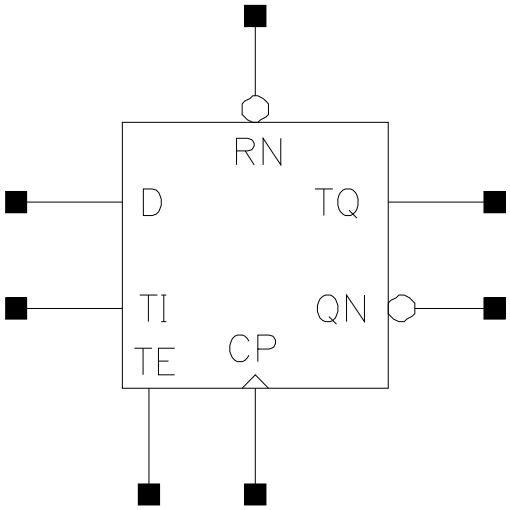
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P0	C8T28SOI_LLHF_-SDFPRQNX3_P0	C8T28SOIDV_LL_-SDFPRQNX5_P0	C8T28SOIDV_LL_-SDFPRQNX10_P0
Clock 100Mhz Data 0Mhz	6.031e-03	5.807e-03	5.513e-03	5.366e-03
Clock 100Mhz Data 25Mhz	5.754e-03	5.597e-03	5.371e-03	5.587e-03
Clock 100Mhz Data 50Mhz	5.476e-03	5.387e-03	5.229e-03	5.808e-03
Clock = 0 Data 100Mhz	2.683e-03	2.875e-03	2.737e-03	2.664e-03
Clock = 1 Data 100Mhz	2.731e-05	3.762e-04	2.604e-04	2.026e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P0	C8T28SOIDV_LL_-SDFPRQNX29_P0		
Clock 100Mhz Data 0Mhz	5.320e-03	5.307e-03		
Clock 100Mhz Data 25Mhz	6.046e-03	6.787e-03		
Clock 100Mhz Data 50Mhz	6.773e-03	8.266e-03		
Clock = 0 Data 100Mhz	2.621e-03	2.592e-03		
Clock = 1 Data 100Mhz	1.679e-04	1.448e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P0	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P0	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P0	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P0	C8T28SOI_LLHF_-SDFPRQNTX3_P0	C8T28SOIDV_LL_-SDFPRQNTX5_P0	C8T28SOIDV_LL_-SDFPRQNTX10_P0
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
RN	0.0007	0.0007	0.0008	0.0008
TE	0.0009	0.0009	0.0007	0.0007
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P0	C8T28SOIDV_LL_-SDFPRQNTX29_P0		
CP	0.0004	0.0004		
D	0.0004	0.0004		
RN	0.0007	0.0006		
TE	0.0007	0.0007		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNTX5_P0	**C8T28SOI_LLHF_-SDFPRQNTX3_P0**	**C8T28SOI_LL_-SDFPRQNTX5_P0**	**C8T28SOI_LLHF_-SDFPRQNTX3_P0**
CP to QN ↓	0.0814	0.0852	3.6288	5.6432
CP to QN ↑	0.0852	0.0783	5.6232	7.7468
CP to TQ ↓	0.0731	0.0562	10.6000	6.6817
CP to TQ ↑	0.0693	0.0648	26.8062	14.1318
RN to QN ↑	0.0737	0.0713	5.6223	7.7776
RN to TQ ↓	0.0634	0.0551	10.3063	6.4232
	C8T28SOIDV_LL_-SDFPRQNTX5_P0	**C8T28SOIDV_LL_-SDFPRQNTX10_P0**	**C8T28SOIDV_LL_-SDFPRQNTX5_P0**	**C8T28SOIDV_LL_-SDFPRQNTX10_P0**
CP to QN ↓	0.0879	0.0928	3.4584	1.7976
CP to QN ↑	0.0690	0.0730	5.0389	2.5635
CP to TQ ↓	0.0476	0.0483	6.6768	6.7343
CP to TQ ↑	0.0665	0.0665	11.1226	11.1247
RN to QN ↑	0.0652	0.0698	5.0487	2.5629
RN to TQ ↓	0.0427	0.0438	6.6812	6.7357
	C8T28SOIDV_LL_-SDFPRQNTX19_P0	**C8T28SOIDV_LL_-SDFPRQNTX29_P0**	**C8T28SOIDV_LL_-SDFPRQNTX19_P0**	**C8T28SOIDV_LL_-SDFPRQNTX29_P0**
CP to QN ↓	0.0878	0.0895	0.9036	0.6151
CP to QN ↑	0.0739	0.0816	1.2952	0.8791
CP to TQ ↓	0.0520	0.0624	6.7787	7.6376
CP to TQ ↑	0.0711	0.0790	11.1459	12.6739
RN to QN ↑	0.0685	0.0769	1.2944	0.8772
RN to TQ ↓	0.0453	0.0568	6.7649	7.5342

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P0	C8T28SOI_-LLHF_-SDFPRQNTX3_-P0	C8T28SOIDV_-LL_-SDFPRQNTX5_-P0	C8T28SOIDV_-LL_SDF-PRQNTX10_P0
CP ↓	min_pulse_width to CP	0.0930	0.0854	0.0785	0.0786
CP ↑	min_pulse_width to CP	0.0549	0.0470	0.0441	0.0456
D ↓	hold_rising to CP	-0.0360	-0.0848	-0.0072	-0.0077
D ↑	hold_rising to CP	-0.0088	-0.0090	0.0009	0.0009
D ↓	setup_rising to CP	0.0759	0.1293	0.0467	0.0467
D ↑	setup_rising to CP	0.0391	0.0412	0.0266	0.0266
RN ↓	min_pulse_width to RN	0.0615	0.0615	0.0588	0.0615
RN ↑	recovery_rising to CP	0.0028	-0.0000	0.0005	0.0005
RN ↑	removal_rising to CP	0.0096	0.0096	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0289	-0.0333	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0093	-0.0095	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0738	0.1024	0.0442	0.0442
TE ↑	setup_rising to CP	0.0911	0.1199	0.0884	0.0884
TI ↓	hold_rising to CP	-0.0521	-0.0798	-0.0439	-0.0439
TI ↑	hold_rising to CP	-0.0092	-0.0078	-0.0098	-0.0098
TI ↓	setup_rising to CP	0.0919	0.1203	0.0870	0.0870
TI ↑	setup_rising to CP	0.0391	0.0332	0.0388	0.0404
		C8T28SOIDV_-LL_SDF-PRQNTX19_P0	C8T28SOIDV_-LL_SDF-PRQNTX29_P0		
CP ↓	min_pulse_width to CP	0.0799	0.0799		
CP ↑	min_pulse_width to CP	0.0455	0.0546		
D ↓	hold_rising to CP	-0.0023	-0.0019		
D ↑	hold_rising to CP	0.0004	0.0004		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0266	0.0266		
RN ↓	min_pulse_width to RN	0.0637	0.0757		
RN ↑	recovery_rising to CP	-0.0021	0.0005		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0001	-0.0001		
TE ↑	hold_rising to CP	-0.0092	-0.0092		

TE ↓	setup_rising to CP	0.0442	0.0442		
TE ↑	setup_rising to CP	0.0884	0.0884		
TI ↓	hold_rising to CP	-0.0424	-0.0424		
TI ↑	hold_rising to CP	-0.0098	-0.0098		
TI ↓	setup_rising to CP	0.0870	0.0870		
TI ↑	setup_rising to CP	0.0388	0.0388		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P0	1.707e-04	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P0	1.684e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P0	1.767e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_-P0	2.000e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_-P0	2.653e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_-P0	3.516e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

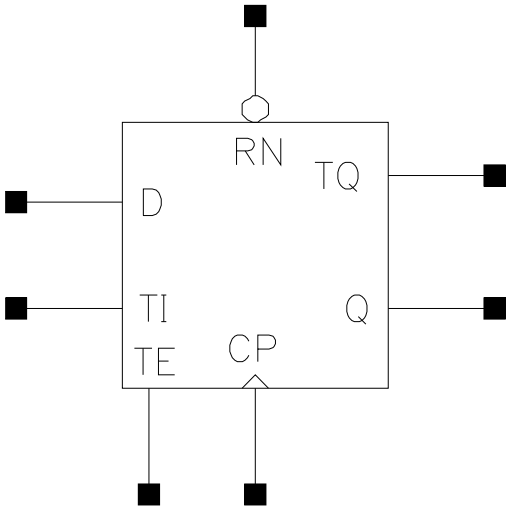
Pin Cycle	C8T28SOI_LL_-SDFPRQNTX5_P0	C8T28SOI_LLHF_-SDFPRQNTX3_P0	C8T28SOIDV_LL_-SDFPRQNTX5_P0	C8T28SOIDV_LL_-SDFPRQNTX10_P0
Clock 100Mhz Data 0Mhz	6.037e-03	5.810e-03	5.524e-03	5.374e-03
Clock 100Mhz Data 25Mhz	5.966e-03	5.784e-03	5.520e-03	5.642e-03
Clock 100Mhz Data 50Mhz	5.896e-03	5.759e-03	5.516e-03	5.909e-03
Clock = 0 Data 100Mhz	2.668e-03	2.872e-03	2.737e-03	2.666e-03
Clock = 1 Data 100Mhz	2.710e-05	3.778e-04	2.615e-04	2.035e-04
	C8T28SOIDV_LL_-SDFPRQNTX19_P0	C8T28SOIDV_LL_-SDFPRQNTX29_P0		
Clock 100Mhz Data 0Mhz	5.327e-03	5.289e-03		
Clock 100Mhz Data 25Mhz	6.064e-03	6.935e-03		
Clock 100Mhz Data 50Mhz	6.800e-03	8.581e-03		
Clock = 0 Data 100Mhz	2.623e-03	2.595e-03		
Clock = 1 Data 100Mhz	1.687e-04	1.454e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P0	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P0	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P0	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P0	C8T28SOI_LLHF_-SDFPRQTX3_P0	C8T28SOIDV_LL_-SDFPRQTX5_P0	C8T28SOIDV_LL_-SDFPRQTX10_P0
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
RN	0.0007	0.0007	0.0008	0.0007
TE	0.0009	0.0009	0.0007	0.0007
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P0	C8T28SOIDV_LL_-SDFPRQTX29_P0		
CP	0.0004	0.0004		
D	0.0004	0.0004		
RN	0.0008	0.0008		
TE	0.0007	0.0007		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQTX5_P0	**C8T28SOI_LLHF_-SDFPRQTX3_P0**	**C8T28SOI_LL_-SDFPRQTX5_P0**	**C8T28SOI_LLHF_-SDFPRQTX3_P0**
CP to Q ↓	0.0748	0.0651	3.9777	6.0657
CP to Q ↑	0.0598	0.0648	5.2027	8.0120
CP to TQ ↓	0.0884	0.0628	11.1575	6.8302
CP to TQ ↑	0.0766	0.0687	26.8533	14.3053
RN to Q ↓	0.0599	0.0585	3.6685	5.7138
RN to TQ ↓	0.0693	0.0580	10.7820	6.5334
	C8T28SOIDV_LL_-SDFPRQTX5_P0	**C8T28SOIDV_LL_-SDFPRQTX10_P0**	**C8T28SOIDV_LL_-SDFPRQTX5_P0**	**C8T28SOIDV_LL_-SDFPRQTX10_P0**
CP to Q ↓	0.0539	0.0727	3.6275	1.7706
CP to Q ↑	0.0676	0.0947	5.1464	2.5663
CP to TQ ↓	0.0541	0.0754	6.8250	6.7294
CP to TQ ↑	0.0703	0.0987	11.2611	11.1941
RN to Q ↓	0.0510	0.0745	3.5808	1.7672
RN to TQ ↓	0.0511	0.0772	6.7751	6.7284
	C8T28SOIDV_LL_-SDFPRQTX19_P0	**C8T28SOIDV_LL_-SDFPRQTX29_P0**	**C8T28SOIDV_LL_-SDFPRQTX19_P0**	**C8T28SOIDV_LL_-SDFPRQTX29_P0**
CP to Q ↓	0.0811	0.0776	0.9264	0.6210
CP to Q ↑	0.1011	0.1012	1.3022	0.8849
CP to TQ ↓	0.0848	0.0798	6.7903	6.6198
CP to TQ ↑	0.1069	0.1065	11.1847	11.4400
RN to Q ↓	0.0818	0.0789	0.9268	0.6207
RN to TQ ↓	0.0855	0.0811	6.7914	6.6193

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_P0	C8T28SOI_-LLHF_-SDFPRQTX3_P0	C8T28SOIDV_-LL_-SDFPRQTX5_P0	C8T28SOIDV_-LL_-SDFPRQTX10_-P0
CP ↓	min_pulse_width to CP	0.0930	0.0854	0.0786	0.0786
CP ↑	min_pulse_width to CP	0.0644	0.0504	0.0455	0.0409
D ↓	hold_rising to CP	-0.0360	-0.0848	-0.0077	-0.0077
D ↑	hold_rising to CP	-0.0088	-0.0090	0.0009	0.0009
D ↓	setup_rising to CP	0.0759	0.1267	0.0467	0.0467
D ↑	setup_rising to CP	0.0391	0.0444	0.0266	0.0266
RN ↓	min_pulse_width to RN	0.0659	0.0615	0.0588	0.0518
RN ↑	recovery_rising to CP	0.0028	-0.0000	0.0005	-0.0021
RN ↑	removal_rising to CP	0.0090	0.0100	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0289	-0.0333	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0093	-0.0095	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0738	0.1024	0.0442	0.0442
TE ↑	setup_rising to CP	0.0906	0.1204	0.0884	0.0884
TI ↓	hold_rising to CP	-0.0521	-0.0798	-0.0439	-0.0439
TI ↑	hold_rising to CP	-0.0092	-0.0078	-0.0098	-0.0141
TI ↓	setup_rising to CP	0.0919	0.1203	0.0870	0.0870
TI ↑	setup_rising to CP	0.0391	0.0332	0.0404	0.0404
		C8T28SOIDV_-LL_-SDFPRQTX19_-P0	C8T28SOIDV_-LL_-SDFPRQTX29_-P0		
CP ↓	min_pulse_width to CP	0.0786	0.0786		
CP ↑	min_pulse_width to CP	0.0408	0.0408		
D ↓	hold_rising to CP	-0.0077	-0.0072		
D ↑	hold_rising to CP	0.0009	0.0009		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0266	0.0266		
RN ↓	min_pulse_width to RN	0.0518	0.0518		
RN ↑	recovery_rising to CP	0.0005	-0.0021		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0092	-0.0092		

TE ↓	setup_rising to CP	0.0442	0.0442		
TE ↑	setup_rising to CP	0.0884	0.0884		
TI ↓	hold_rising to CP	-0.0439	-0.0439		
TI ↑	hold_rising to CP	-0.0098	-0.0141		
TI ↓	setup_rising to CP	0.0870	0.0870		
TI ↑	setup_rising to CP	0.0404	0.0404		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P0	1.750e-04	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P0	1.672e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P0	1.777e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P0	2.314e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P0	2.854e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P0	3.672e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

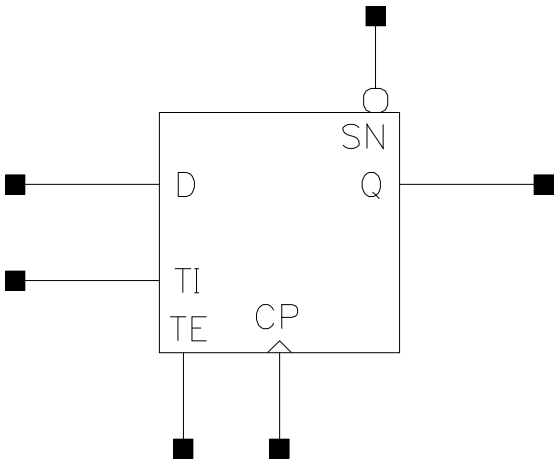
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P0	C8T28SOI_LLHF_-SDFPRQTX3_P0	C8T28SOIDV_LL_-SDFPRQTX5_P0	C8T28SOIDV_LL_-SDFPRQTX10_P0
Clock 100Mhz Data 0Mhz	6.039e-03	5.814e-03	5.518e-03	5.370e-03
Clock 100Mhz Data 25Mhz	6.052e-03	5.802e-03	5.503e-03	5.748e-03
Clock 100Mhz Data 50Mhz	6.064e-03	5.789e-03	5.489e-03	6.126e-03
Clock = 0 Data 100Mhz	2.674e-03	2.875e-03	2.735e-03	2.665e-03
Clock = 1 Data 100Mhz	2.715e-05	3.782e-04	2.619e-04	2.037e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P0	C8T28SOIDV_LL_-SDFPRQTX29_P0		
Clock 100Mhz Data 0Mhz	5.281e-03	5.222e-03		
Clock 100Mhz Data 25Mhz	6.158e-03	6.610e-03		
Clock 100Mhz Data 50Mhz	7.036e-03	7.998e-03		
Clock = 0 Data 100Mhz	2.623e-03	2.596e-03		
Clock = 1 Data 100Mhz	1.689e-04	1.456e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P0	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P0	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P0	C8T28SOI_LLHF_-SDFPSQX3_P0	C8T28SOIDV_LL_-SDFPSQX5_P0	C8T28SOIDV_LL_-SDFPSQX10_P0
CP	0.0006	0.0006	0.0004	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0012	0.0012	0.0008	0.0009
TE	0.0009	0.0009	0.0008	0.0009
TI	0.0003	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQX14_P0	C8T28SOIDV_LL_-SDFPSQX19_P0	C8T28SOIDV_LL_-SDFPSQX29_P0	
CP	0.0005	0.0005	0.0005	
D	0.0003	0.0003	0.0003	
SN	0.0009	0.0009	0.0009	
TE	0.0009	0.0009	0.0009	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P0	**C8T28SOI_LLHF_-SDFPSQX3_P0**	**C8T28SOI_LL_-SDFPSQX5_P0**	**C8T28SOI_LLHF_-SDFPSQX3_P0**
CP to Q ↓	0.0676	0.0594	3.8466	5.9860
CP to Q ↑	0.0576	0.0637	5.2045	7.8744
SN to Q ↑	0.0480	0.0438	5.1424	7.7846
	C8T28SOIDV_LL_-SDFPSQX5_P0	**C8T28SOIDV_LL_-SDFPSQX10_P0**	**C8T28SOIDV_LL_-SDFPSQX5_P0**	**C8T28SOIDV_LL_-SDFPSQX10_P0**
CP to Q ↓	0.0493	0.0726	3.5216	1.7141
CP to Q ↑	0.0621	0.1002	5.0968	2.5546
SN to Q ↑	0.0433	0.0789	5.0837	2.5573
	C8T28SOIDV_LL_-SDFPSQX14_P0	**C8T28SOIDV_LL_-SDFPSQX19_P0**	**C8T28SOIDV_LL_-SDFPSQX14_P0**	**C8T28SOIDV_LL_-SDFPSQX19_P0**
CP to Q ↓	0.0725	0.0771	1.1527	0.8784
CP to Q ↑	0.0997	0.1035	1.7111	1.2876
SN to Q ↑	0.0779	0.0817	1.7118	1.2890
	C8T28SOIDV_LL_-SDFPSQX29_P0		**C8T28SOIDV_LL_-SDFPSQX29_P0**	
CP to Q ↓	0.0768		0.5966	
CP to Q ↑	0.1075		0.8571	
SN to Q ↑	0.0858		0.8562	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P0	C8T28SOI_-LLHF_-SDFPSQX3_P0	C8T28SOIDV_-LL_SDFPSQX5_-P0	C8T28SOIDV_-LL_-SDFPSQX10_P0
CP ↓	min_pulse_width to CP	0.1024	0.1030	0.0857	0.0864
CP ↑	min_pulse_width to CP	0.0597	0.0457	0.0408	0.0408
D ↓	hold_rising to CP	-0.0462	-0.0946	-0.0116	-0.0191
D ↑	hold_rising to CP	-0.0098	-0.0041	0.0009	0.0009
D ↓	setup_rising to CP	0.0857	0.1435	0.0590	0.0613
D ↑	setup_rising to CP	0.0363	0.0395	0.0266	0.0298

SN ↓	min_pulse_width to SN	0.0474	0.0403	0.0403	0.0425
SN ↑	recovery_rising to CP	0.0031	0.0080	-0.0017	-0.0070
SN ↑	removal_rising to CP	0.0238	0.0310	0.0331	0.0357
TE ↓	hold_rising to CP	-0.0230	-0.0279	-0.0099	-0.0147
TE ↑	hold_rising to CP	-0.0072	-0.0046	0.0031	-0.0044
TE ↓	setup_rising to CP	0.0808	0.1170	0.0565	0.0592
TE ↑	setup_rising to CP	0.1004	0.1341	0.0933	0.0884
TI ↓	hold_rising to CP	-0.0621	-0.0911	-0.0439	-0.0424
TI ↑	hold_rising to CP	-0.0034	-0.0022	0.0027	-0.0034
TI ↓	setup_rising to CP	0.1016	0.1349	0.0918	0.0870
TI ↑	setup_rising to CP	0.0332	0.0326	0.0237	0.0340
		C8T28SOIDV_-LL_-SDFPSQX14_P0	C8T28SOIDV_-LL_-SDFPSQX19_P0	C8T28SOIDV_-LL_-SDFPSQX29_P0	
CP ↓	min_pulse_width to CP	0.0864	0.0864	0.0864	
CP ↑	min_pulse_width to CP	0.0408	0.0409	0.0409	
D ↓	hold_rising to CP	-0.0191	-0.0191	-0.0191	
D ↑	hold_rising to CP	0.0009	0.0009	0.0009	
D ↓	setup_rising to CP	0.0613	0.0613	0.0613	
D ↑	setup_rising to CP	0.0298	0.0298	0.0298	
SN ↓	min_pulse_width to SN	0.0403	0.0425	0.0425	
SN ↑	recovery_rising to CP	-0.0066	-0.0066	-0.0066	
SN ↑	removal_rising to CP	0.0357	0.0357	0.0357	
TE ↓	hold_rising to CP	-0.0147	-0.0147	-0.0147	
TE ↑	hold_rising to CP	-0.0044	-0.0044	-0.0044	
TE ↓	setup_rising to CP	0.0592	0.0592	0.0592	
TE ↑	setup_rising to CP	0.0884	0.0884	0.0884	
TI ↓	hold_rising to CP	-0.0424	-0.0424	-0.0424	
TI ↑	hold_rising to CP	-0.0049	-0.0049	-0.0049	
TI ↓	setup_rising to CP	0.0870	0.0870	0.0870	
TI ↑	setup_rising to CP	0.0342	0.0342	0.0342	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQX5_P0	1.761e-04	1.000e-20

C8T28SOI_LLHF_SDFPSQX3_P0	1.642e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P0	1.687e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P0	2.275e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P0	2.596e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P0	2.959e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P0	3.677e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

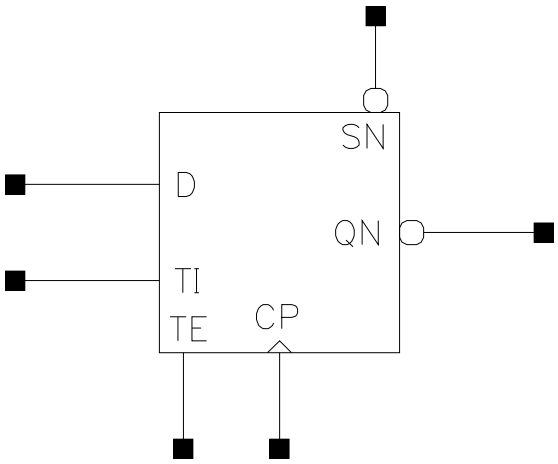
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P0	C8T28SOI_LLHF_-SDFPSQX3_P0	C8T28SOIDV_LL_-SDFPSQX5_P0	C8T28SOIDV_LL_-SDFPSQX10_P0
Clock 100Mhz Data 0Mhz	5.919e-03	5.642e-03	5.367e-03	5.237e-03
Clock 100Mhz Data 25Mhz	5.871e-03	5.563e-03	5.229e-03	5.566e-03
Clock 100Mhz Data 50Mhz	5.823e-03	5.485e-03	5.090e-03	5.895e-03
Clock = 0 Data 100Mhz	2.769e-03	2.967e-03	2.850e-03	2.815e-03
Clock = 1 Data 100Mhz	2.735e-05	3.744e-04	2.594e-04	2.021e-04
	C8T28SOIDV_LL_-SDFPSQX14_P0	C8T28SOIDV_LL_-SDFPSQX19_P0	C8T28SOIDV_LL_-SDFPSQX29_P0	
Clock 100Mhz Data 0Mhz	5.159e-03	5.108e-03	5.071e-03	
Clock 100Mhz Data 25Mhz	5.682e-03	5.986e-03	6.386e-03	
Clock 100Mhz Data 50Mhz	6.205e-03	6.865e-03	7.702e-03	
Clock = 0 Data 100Mhz	2.794e-03	2.780e-03	2.770e-03	
Clock = 1 Data 100Mhz	1.677e-04	1.449e-04	1.285e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P0	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P0	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P0	C8T28SOI_LLHF_-SDFPSQNX3_P0	C8T28SOIDV_LL_-SDFPSQNX5_P0	C8T28SOIDV_LL_-SDFPSQNX10_P0
CP	0.0006	0.0006	0.0004	0.0004
D	0.0003	0.0004	0.0003	0.0003
SN	0.0012	0.0011	0.0009	0.0009
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNX14_P0	C8T28SOIDV_LL_-SDFPSQNX19_P0	C8T28SOIDV_LL_-SDFPSQNX23_P0	C8T28SOIDV_LL_-SDFPSQNX29_P0
CP	0.0004	0.0004	0.0004	0.0004
D	0.0003	0.0003	0.0003	0.0003
SN	0.0009	0.0009	0.0009	0.0008
TE	0.0008	0.0008	0.0008	0.0008
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNX5_P0	**C8T28SOI_LLHF_-SDFPSQNX3_P0**	**C8T28SOI_LL_-SDFPSQNX5_P0**	**C8T28SOI_LLHF_-SDFPSQNX3_P0**
CP to QN ↓	0.0778	0.0785	3.7990	5.5443
CP to QN ↑	0.0740	0.0677	5.4020	7.7301
SN to QN ↓	0.0692	0.0591	3.7999	5.5368
	C8T28SOIDV_LL_-SDFPSQNX5_P0	**C8T28SOIDV_LL_-SDFPSQNX10_P0**	**C8T28SOIDV_LL_-SDFPSQNX5_P0**	**C8T28SOIDV_LL_-SDFPSQNX10_P0**
CP to QN ↓	0.0833	0.0776	3.4027	1.6862
CP to QN ↑	0.0670	0.0669	5.0578	2.5318
SN to QN ↓	0.0637	0.0564	3.4015	1.6832
	C8T28SOIDV_LL_-SDFPSQNX14_P0	**C8T28SOIDV_LL_-SDFPSQNX19_P0**	**C8T28SOIDV_LL_-SDFPSQNX14_P0**	**C8T28SOIDV_LL_-SDFPSQNX19_P0**
CP to QN ↓	0.0803	0.0821	1.1551	0.8810
CP to QN ↑	0.0685	0.0707	1.7009	1.2800
SN to QN ↓	0.0576	0.0602	1.1543	0.8792
	C8T28SOIDV_LL_-SDFPSQNX23_P0	**C8T28SOIDV_LL_-SDFPSQNX29_P0**	**C8T28SOIDV_LL_-SDFPSQNX23_P0**	**C8T28SOIDV_LL_-SDFPSQNX29_P0**
CP to QN ↓	0.0836	0.0799	0.6801	0.5902
CP to QN ↑	0.0707	0.0714	1.2748	0.8557
SN to QN ↓	0.0623	0.0619	0.6790	0.5900

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P0	C8T28SOI_-LLHF_-SDFPSQNX3_-P0	C8T28SOIDV_-LL_-SDFPSQNX5_-P0	C8T28SOIDV_-LL_-SDFPSQNX10_-P0
CP ↓	min_pulse_width to CP	0.1024	0.1030	0.0857	0.0887
CP ↑	min_pulse_width to CP	0.0455	0.0411	0.0408	0.0454
D ↓	hold_rising to CP	-0.0462	-0.0941	-0.0116	-0.0120
D ↑	hold_rising to CP	-0.0098	-0.0069	0.0009	0.0009
D ↓	setup_rising to CP	0.0857	0.1435	0.0586	0.0590

D ↑	setup_rising to CP	0.0363	0.0395	0.0266	0.0266
SN ↓	min_pulse_width to SN	0.0447	0.0376	0.0403	0.0403
SN ↑	recovery_rising to CP	0.0031	0.0048	-0.0044	-0.0017
SN ↑	removal_rising to CP	0.0238	0.0310	0.0335	0.0357
TE ↓	hold_rising to CP	-0.0230	-0.0279	-0.0099	-0.0104
TE ↑	hold_rising to CP	-0.0072	-0.0041	0.0031	0.0031
TE ↓	setup_rising to CP	0.0808	0.1170	0.0565	0.0565
TE ↑	setup_rising to CP	0.1004	0.1341	0.0933	0.0933
TI ↓	hold_rising to CP	-0.0621	-0.0911	-0.0482	-0.0439
TI ↑	hold_rising to CP	-0.0077	-0.0038	0.0027	0.0027
TI ↓	setup_rising to CP	0.1016	0.1349	0.0918	0.0918
TI ↑	setup_rising to CP	0.0332	0.0326	0.0237	0.0237
		C8T28SOIDV_-LL_-SDFPSQNX14_-P0	C8T28SOIDV_-LL_-SDFPSQNX19_-P0	C8T28SOIDV_-LL_-SDFPSQNX23_-P0	C8T28SOIDV_-LL_-SDFPSQNX29_-P0
CP ↓	min_pulse_width to CP	0.0887	0.0887	0.0887	0.0857
CP ↑	min_pulse_width to CP	0.0454	0.0454	0.0454	0.0487
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120	-0.0116
D ↑	hold_rising to CP	0.0009	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0590	0.0590	0.0590	0.0586
D ↑	setup_rising to CP	0.0266	0.0266	0.0266	0.0266
SN ↓	min_pulse_width to SN	0.0403	0.0425	0.0425	0.0452
SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0357	0.0357	0.0357	0.0331
TE ↓	hold_rising to CP	-0.0104	-0.0104	-0.0104	-0.0099
TE ↑	hold_rising to CP	0.0031	0.0031	0.0031	0.0031
TE ↓	setup_rising to CP	0.0565	0.0565	0.0565	0.0565
TE ↑	setup_rising to CP	0.0933	0.0933	0.0933	0.0933
TI ↓	hold_rising to CP	-0.0439	-0.0439	-0.0439	-0.0439
TI ↑	hold_rising to CP	0.0027	0.0027	0.0027	0.0027
TI ↓	setup_rising to CP	0.0925	0.0918	0.0918	0.0918
TI ↑	setup_rising to CP	0.0237	0.0237	0.0237	0.0237

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P0	1.762e-04	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P0	1.632e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P0	1.712e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P0	2.372e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P0	2.613e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P0	2.958e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P0	3.128e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P0	3.850e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

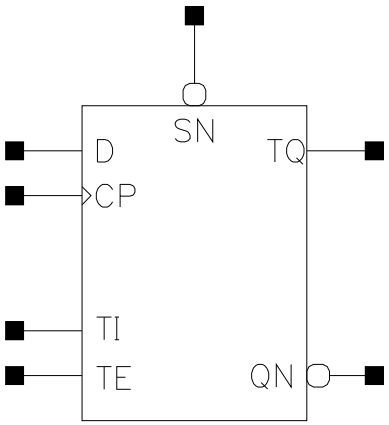
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P0	C8T28SOI_LLHF_-SDFPSQNX3_P0	C8T28SOIDV_LL_-SDFPSQNX5_P0	C8T28SOIDV_LL_-SDFPSQNX10_P0
Clock 100Mhz Data 0Mhz	5.906e-03	5.635e-03	5.361e-03	5.283e-03
Clock 100Mhz Data 25Mhz	5.755e-03	5.505e-03	5.302e-03	5.657e-03
Clock 100Mhz Data 50Mhz	5.604e-03	5.375e-03	5.243e-03	6.031e-03
Clock = 0 Data 100Mhz	2.769e-03	2.969e-03	2.853e-03	2.792e-03
Clock = 1 Data 100Mhz	2.731e-05	3.757e-04	2.603e-04	2.026e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P0	C8T28SOIDV_LL_-SDFPSQNX19_P0	C8T28SOIDV_LL_-SDFPSQNX23_P0	C8T28SOIDV_LL_-SDFPSQNX29_P0
Clock 100Mhz Data 0Mhz	5.235e-03	5.204e-03	5.181e-03	5.137e-03
Clock 100Mhz Data 25Mhz	5.813e-03	5.997e-03	6.101e-03	6.484e-03
Clock 100Mhz Data 50Mhz	6.390e-03	6.790e-03	7.021e-03	7.830e-03
Clock = 0 Data 100Mhz	2.756e-03	2.732e-03	2.715e-03	2.704e-03
Clock = 1 Data 100Mhz	1.680e-04	1.449e-04	1.284e-04	1.162e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P0	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P0	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P0	C8T28SOI_LLHF_-SDFPSQNTX3_P0	C8T28SOIDV_LL_-SDFPSQNTX5_P0	C8T28SOIDV_LL_-SDFPSQNTX10_P0
CP	0.0006	0.0006	0.0004	0.0004
D	0.0003	0.0004	0.0003	0.0003
SN	0.0011	0.0011	0.0008	0.0008
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNTX19_P0	C8T28SOIDV_LL_-SDFPSQNTX23_P0	C8T28SOIDV_LL_-SDFPSQNTX29_P0	
CP	0.0004	0.0004	0.0004	
D	0.0003	0.0003	0.0003	
SN	0.0008	0.0008	0.0008	
TE	0.0008	0.0008	0.0008	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P0	**C8T28SOI_LLHF_-SDFPSQNTX3_P0**	**C8T28SOI_LL_-SDFPSQNTX5_P0**	**C8T28SOI_LLHF_-SDFPSQNTX3_P0**
CP to QN ↓	0.0846	0.0844	3.8606	5.6132
CP to QN ↑	0.0846	0.0797	5.3667	7.7684
CP to TQ ↓	0.0712	0.0569	10.4424	6.7289
CP to TQ ↑	0.0713	0.0663	26.8287	14.1464
SN to QN ↓	0.0734	0.0633	3.8586	5.6136
SN to TQ ↑	0.0605	0.0460	26.7659	14.0955
	C8T28SOIDV_LL_-SDFPSQNTX5_P0	**C8T28SOIDV_LL_-SDFPSQNTX10_P0**	**C8T28SOIDV_LL_-SDFPSQNTX5_P0**	**C8T28SOIDV_LL_-SDFPSQNTX10_P0**
CP to QN ↓	0.0830	0.0774	3.4647	1.6767
CP to QN ↑	0.0682	0.0711	5.0564	2.5423
CP to TQ ↓	0.0481	0.0550	6.7382	6.8132
CP to TQ ↑	0.0637	0.0667	12.0698	12.1301
SN to QN ↓	0.0626	0.0587	3.4701	1.6779
SN to TQ ↑	0.0432	0.0480	12.0497	12.0811
	C8T28SOIDV_LL_-SDFPSQNTX19_P0	**C8T28SOIDV_LL_-SDFPSQNTX23_P0**	**C8T28SOIDV_LL_-SDFPSQNTX19_P0**	**C8T28SOIDV_LL_-SDFPSQNTX23_P0**
CP to QN ↓	0.0819	0.0841	0.8751	0.6783
CP to QN ↑	0.0756	0.0747	1.2826	1.2763
CP to TQ ↓	0.0548	0.0558	6.8024	6.8413
CP to TQ ↑	0.0666	0.0673	12.1348	12.1423
SN to QN ↓	0.0629	0.0651	0.8746	0.6778
SN to TQ ↑	0.0477	0.0485	12.0828	12.0902
	C8T28SOIDV_LL_-SDFPSQNTX29_P0		**C8T28SOIDV_LL_-SDFPSQNTX29_P0**	
CP to QN ↓	0.0833		0.5919	
CP to QN ↑	0.0768		0.8558	

CP to TQ ↓	0.0578		6.9661	
CP to TQ ↑	0.0718		14.0474	
SN to QN ↓	0.0645		0.5917	
SN to TQ ↑	0.0531		13.9762	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P0	C8T28SOI_-LLHF_-SDFPSQNTX3_-P0	C8T28SOIDV_-LL_-SDFPSQNTX5_-P0	C8T28SOIDV_-LL_SDFP-SQNTX10_P0
CP ↓	min_pulse_width to CP	0.1024	0.1030	0.0840	0.0857
CP ↑	min_pulse_width to CP	0.0549	0.0470	0.0441	0.0453
D ↓	hold_rising to CP	-0.0462	-0.0946	-0.0116	-0.0116
D ↑	hold_rising to CP	-0.0066	-0.0041	0.0009	0.0009
D ↓	setup_rising to CP	0.0857	0.1435	0.0590	0.0586
D ↑	setup_rising to CP	0.0363	0.0395	0.0266	0.0266
SN ↓	min_pulse_width to SN	0.0496	0.0425	0.0403	0.0425
SN ↑	recovery_rising to CP	0.0080	0.0080	-0.0044	-0.0017
SN ↑	removal_rising to CP	0.0212	0.0310	0.0331	0.0331
TE ↓	hold_rising to CP	-0.0230	-0.0279	-0.0099	-0.0099
TE ↑	hold_rising to CP	-0.0072	-0.0046	0.0031	0.0031
TE ↓	setup_rising to CP	0.0857	0.1170	0.0565	0.0565
TE ↑	setup_rising to CP	0.1057	0.1367	0.0933	0.0933
TI ↓	hold_rising to CP	-0.0621	-0.0911	-0.0439	-0.0439
TI ↑	hold_rising to CP	-0.0034	-0.0022	0.0027	0.0027
TI ↓	setup_rising to CP	0.1065	0.1349	0.0918	0.0918
TI ↑	setup_rising to CP	0.0332	0.0326	0.0237	0.0237
		C8T28SOIDV_-LL_SDFP-SQNTX19_P0	C8T28SOIDV_-LL_SDFP-SQNTX23_P0	C8T28SOIDV_-LL_SDFP-SQNTX29_P0	
CP ↓	min_pulse_width to CP	0.0857	0.0857	0.0857	
CP ↑	min_pulse_width to CP	0.0487	0.0487	0.0500	
D ↓	hold_rising to CP	-0.0116	-0.0116	-0.0116	
D ↑	hold_rising to CP	0.0009	0.0009	0.0009	
D ↓	setup_rising to CP	0.0586	0.0586	0.0586	
D ↑	setup_rising to CP	0.0266	0.0266	0.0266	
SN ↓	min_pulse_width to SN	0.0452	0.0452	0.0452	

SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	
SN ↑	removal_rising to CP	0.0331	0.0331	0.0335	
TE ↓	hold_rising to CP	-0.0099	-0.0099	-0.0099	
TE ↑	hold_rising to CP	0.0031	0.0031	0.0031	
TE ↓	setup_rising to CP	0.0565	0.0565	0.0565	
TE ↑	setup_rising to CP	0.0933	0.0933	0.0933	
TI ↓	hold_rising to CP	-0.0439	-0.0439	-0.0439	
TI ↑	hold_rising to CP	0.0027	0.0027	0.0027	
TI ↓	setup_rising to CP	0.0918	0.0918	0.0918	
TI ↑	setup_rising to CP	0.0237	0.0237	0.0237	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P0	1.750e-04	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P0	1.752e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P0	1.861e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_P0	2.497e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_P0	3.098e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_P0	3.286e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_P0	3.968e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

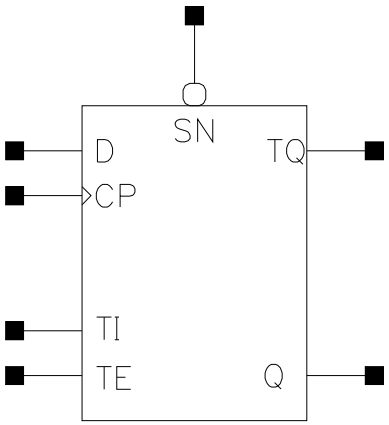
Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P0	C8T28SOI_LLHF_-SDFPSQNTX3_P0	C8T28SOIDV_LL_-SDFPSQNTX5_P0	C8T28SOIDV_LL_-SDFPSQNTX10_P0
Clock 100Mhz Data 0Mhz	5.730e-03	5.546e-03	5.306e-03	5.185e-03
Clock 100Mhz Data 25Mhz	5.803e-03	5.629e-03	5.340e-03	5.704e-03
Clock 100Mhz Data 50Mhz	5.876e-03	5.711e-03	5.375e-03	6.223e-03
Clock = 0 Data 100Mhz	2.764e-03	2.964e-03	2.848e-03	2.790e-03
Clock = 1 Data 100Mhz	2.715e-05	3.735e-04	2.588e-04	2.016e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P0	C8T28SOIDV_LL_-SDFPSQNTX23_P0	C8T28SOIDV_LL_-SDFPSQNTX29_P0	
Clock 100Mhz Data 0Mhz	5.113e-03	5.064e-03	5.030e-03	
Clock 100Mhz Data 25Mhz	6.067e-03	6.160e-03	6.586e-03	
Clock 100Mhz Data 50Mhz	7.020e-03	7.255e-03	8.142e-03	
Clock = 0 Data 100Mhz	2.756e-03	2.733e-03	2.717e-03	
Clock = 1 Data 100Mhz	1.672e-04	1.443e-04	1.279e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P0	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P0	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P0	C8T28SOI_LLHF_-SDFPSQTX3_P0	C8T28SOIDV_LL_-SDFPSQTX5_P0	C8T28SOIDV_LL_-SDFPSQTX10_P0
CP	0.0006	0.0006	0.0004	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0012	0.0012	0.0008	0.0009
TE	0.0009	0.0009	0.0008	0.0009
TI	0.0003	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQTX19_P0	C8T28SOIDV_LL_-SDFPSQTX29_P0		
CP	0.0005	0.0005		
D	0.0003	0.0003		
SN	0.0009	0.0009		
TE	0.0009	0.0009		
TI	0.0004	0.0004		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQTX5_P0	**C8T28SOI_LLHF_-SDFPSQTX3_P0**	**C8T28SOI_LL_-SDFPSQTX5_P0**	**C8T28SOI_LLHF_-SDFPSQTX3_P0**
CP to Q ↓	0.0718	0.0658	4.0045	6.1377
CP to Q ↑	0.0604	0.0662	5.2105	8.0328
CP to TQ ↓	0.0852	0.0633	11.0034	6.8840
CP to TQ ↑	0.0778	0.0701	26.8421	14.3217
SN to Q ↑	0.0498	0.0456	5.1336	7.9265
SN to TQ ↑	0.0651	0.0490	26.7507	14.2454
	C8T28SOIDV_LL_-SDFPSQTX5_P0	**C8T28SOIDV_LL_-SDFPSQTX10_P0**	**C8T28SOIDV_LL_-SDFPSQTX5_P0**	**C8T28SOIDV_LL_-SDFPSQTX10_P0**
CP to Q ↓	0.0550	0.0713	3.6137	1.7550
CP to Q ↑	0.0646	0.0987	5.1567	2.5736
CP to TQ ↓	0.0554	0.0734	6.8269	6.9762
CP to TQ ↑	0.0669	0.1029	12.1926	11.9670
SN to Q ↑	0.0457	0.0770	5.1438	2.5745
SN to TQ ↑	0.0480	0.0812	12.1384	11.9664
	C8T28SOIDV_LL_-SDFPSQTX19_P0	**C8T28SOIDV_LL_-SDFPSQTX29_P0**	**C8T28SOIDV_LL_-SDFPSQTX19_P0**	**C8T28SOIDV_LL_-SDFPSQTX29_P0**
CP to Q ↓	0.0767	0.0864	0.9027	0.5836
CP to Q ↑	0.1036	0.1123	1.3145	0.8729
CP to TQ ↓	0.0769	0.0491	5.8856	6.0960
CP to TQ ↑	0.1085	0.0709	13.9697	14.0782
SN to Q ↑	0.0818	0.0905	1.3146	0.8730
SN to TQ ↑	0.0867	0.0495	13.9708	14.0616

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_P0	C8T28SOI_-LLHF_-SDFPSQTX3_P0	C8T28SOIDV_-LL_-SDFPSQTX5_P0	C8T28SOIDV_-LL_-SDFPSQTX10_-P0
CP ↓	min_pulse_width to CP	0.1024	0.1030	0.0857	0.0864
CP ↑	min_pulse_width to CP	0.0644	0.0518	0.0455	0.0408
D ↓	hold_rising to CP	-0.0462	-0.0946	-0.0116	-0.0191
D ↑	hold_rising to CP	-0.0066	-0.0041	0.0009	0.0009
D ↓	setup_rising to CP	0.0857	0.1435	0.0586	0.0613
D ↑	setup_rising to CP	0.0363	0.0395	0.0266	0.0298
SN ↓	min_pulse_width to SN	0.0522	0.0425	0.0425	0.0425
SN ↑	recovery_rising to CP	0.0080	0.0080	-0.0017	-0.0070
SN ↑	removal_rising to CP	0.0212	0.0310	0.0331	0.0357
TE ↓	hold_rising to CP	-0.0230	-0.0279	-0.0099	-0.0143
TE ↑	hold_rising to CP	-0.0040	-0.0046	0.0031	-0.0044
TE ↓	setup_rising to CP	0.0857	0.1170	0.0565	0.0592
TE ↑	setup_rising to CP	0.1057	0.1367	0.0933	0.0911
TI ↓	hold_rising to CP	-0.0621	-0.0911	-0.0439	-0.0424
TI ↑	hold_rising to CP	-0.0034	-0.0022	0.0027	-0.0049
TI ↓	setup_rising to CP	0.1065	0.1349	0.0918	0.0870
TI ↑	setup_rising to CP	0.0332	0.0326	0.0237	0.0340
		C8T28SOIDV_-LL_-SDFPSQTX19_-P0	C8T28SOIDV_-LL_-SDFPSQTX29_-P0		
CP ↓	min_pulse_width to CP	0.0864	0.0864		
CP ↑	min_pulse_width to CP	0.0409	0.0456		
D ↓	hold_rising to CP	-0.0191	-0.0191		
D ↑	hold_rising to CP	0.0009	0.0009		
D ↓	setup_rising to CP	0.0613	0.0613		
D ↑	setup_rising to CP	0.0298	0.0298		
SN ↓	min_pulse_width to SN	0.0425	0.0500		
SN ↑	recovery_rising to CP	-0.0066	-0.0070		
SN ↑	removal_rising to CP	0.0357	0.0357		
TE ↓	hold_rising to CP	-0.0147	-0.0147		
TE ↑	hold_rising to CP	-0.0044	-0.0044		

TE ↓	setup_rising to CP	0.0592	0.0592		
TE ↑	setup_rising to CP	0.0884	0.0911		
TI ↓	hold_rising to CP	-0.0424	-0.0424		
TI ↑	hold_rising to CP	-0.0049	-0.0034		
TI ↓	setup_rising to CP	0.0870	0.0870		
TI ↑	setup_rising to CP	0.0342	0.0342		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P0	1.757e-04	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P0	1.761e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P0	1.841e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P0	2.412e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P0	2.963e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P0	3.898e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

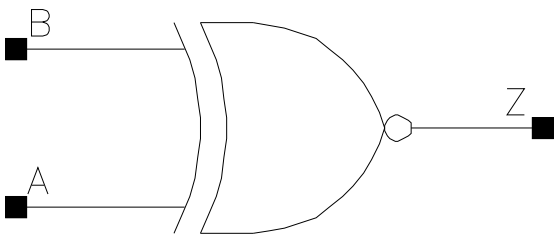
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P0	C8T28SOI_LLHF_-SDFPSQTX3_P0	C8T28SOIDV_LL_-SDFPSQTX5_P0	C8T28SOIDV_LL_-SDFPSQTX10_P0
Clock 100Mhz Data 0Mhz	5.737e-03	5.551e-03	5.310e-03	5.194e-03
Clock 100Mhz Data 25Mhz	5.869e-03	5.663e-03	5.369e-03	5.620e-03
Clock 100Mhz Data 50Mhz	6.001e-03	5.776e-03	5.428e-03	6.045e-03
Clock = 0 Data 100Mhz	2.762e-03	2.964e-03	2.847e-03	2.821e-03
Clock = 1 Data 100Mhz	2.714e-05	3.737e-04	2.589e-04	2.019e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P0	C8T28SOIDV_LL_-SDFPSQTX29_P0		
Clock 100Mhz Data 0Mhz	5.125e-03	5.079e-03		
Clock 100Mhz Data 25Mhz	6.034e-03	6.577e-03		
Clock 100Mhz Data 50Mhz	6.943e-03	8.074e-03		
Clock = 0 Data 100Mhz	2.799e-03	2.784e-03		
Clock = 1 Data 100Mhz	1.677e-04	1.450e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.600	0.544	0.8704
X5_P0	0.800	1.496	1.1968
X8_P0	1.600	1.088	1.7408
X9_P0	0.800	1.632	1.3056
X11_P0	1.600	1.360	2.1760
X14_P0	0.800	2.312	1.8496
X15_P0	1.600	1.904	3.0464
X19_P0	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P0	X5_P0	X8_P0	X9_P0
A	0.0008	0.0005	0.0014	0.0006
B	0.0008	0.0009	0.0012	0.0011
	X11_P0	X14_P0	X15_P0	X19_P0
A	0.0021	0.0008	0.0024	0.0010
B	0.0019	0.0013	0.0022	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X5_P0	X4_P0	X5_P0
A to Z ↓	0.0162	0.0479	4.8292	3.6796
A to Z ↑	0.0188	0.0444	7.4318	5.5049
B to Z ↓	0.0154	0.0354	4.8296	3.6642
B to Z ↑	0.0199	0.0333	7.4383	5.4950

	X8_P0	X9_P0	X8_P0	X9_P0
A to Z ↓	0.0194	0.0441	2.5425	1.8891
A to Z ↑	0.0228	0.0417	3.9290	2.8043
B to Z ↓	0.0186	0.0332	2.5422	1.8852
B to Z ↑	0.0230	0.0320	3.9297	2.8012
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0181	0.0415	1.7728	1.2777
A to Z ↑	0.0207	0.0384	2.5739	1.7951
B to Z ↓	0.0167	0.0309	1.7719	1.2730
B to Z ↑	0.0207	0.0296	2.5755	1.7921
	X15_P0	**X19_P0**	**X15_P0**	**X19_P0**
A to Z ↓	0.0201	0.0381	1.3411	0.9531
A to Z ↑	0.0229	0.0363	1.9559	1.3360
B to Z ↓	0.0186	0.0292	1.3401	0.9502
B to Z ↑	0.0230	0.0284	1.9574	1.3357

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	9.033e-05	1.000e-20
X5_P0	9.670e-05	1.000e-20
X8_P0	1.420e-04	1.000e-20
X9_P0	1.592e-04	1.000e-20
X11_P0	2.160e-04	1.000e-20
X14_P0	2.428e-04	1.000e-20
X15_P0	2.715e-04	1.000e-20
X19_P0	3.403e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X5_P0	X8_P0	X9_P0
A to Z	1.296e-03	2.817e-03	2.512e-03	4.022e-03
B to Z	1.293e-03	2.279e-03	2.506e-03	3.279e-03
	X11_P0	X14_P0	X15_P0	X19_P0
A to Z	3.587e-03	6.259e-03	4.863e-03	7.574e-03
B to Z	3.535e-03	4.990e-03	4.800e-03	6.181e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

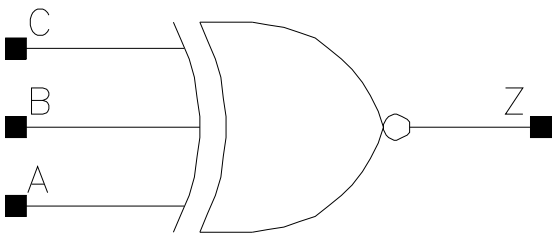
Pin Cycle (vdds)	X4_P0	X5_P0	X8_P0	X9_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P0	X14_P0	X15_P0	X19_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P0	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P0	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P0	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P0	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P0	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P0	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P0	C8T28SOIDV_LL_-XNOR3X4_P0	C8T28SOIDV_LL_-XNOR3X9_P0	C8T28SOIDV_LL_-XNOR3X13_P0
A	0.0013	0.0013	0.0017	0.0022
B	0.0013	0.0012	0.0016	0.0022
C	0.0006	0.0006	0.0006	0.0005
	C8T28SOIDV_LLS_-XNOR3X1_P0	C8T28SOIDV_LLS_-XNOR3X2_P0	C8T28SOIDV_LLS_-XNOR3X5_P0	C8T28SOIDV_LLS_-XNOR3X7_P0

A	0.0013	0.0014	0.0031	0.0047
B	0.0013	0.0015	0.0029	0.0044
C	0.0009	0.0011	0.0021	0.0030

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XNOR3X2_P0	**C8T28SOIDV_LL_-XNOR3X4_P0**	**C8T28SOIDV_LL_-XNOR3X2_P0**	**C8T28SOIDV_LL_-XNOR3X4_P0**
A to Z ↓	0.0491	0.0517	7.7757	3.9941
A to Z ↑	0.0476	0.0481	10.2405	5.5774
B to Z ↓	0.0498	0.0525	7.7764	3.9932
B to Z ↑	0.0484	0.0490	10.2421	5.5756
C to Z ↓	0.0664	0.0701	7.7733	3.9918
C to Z ↑	0.0650	0.0664	10.2316	5.5756
	C8T28SOIDV_LL_-XNOR3X9_P0	**C8T28SOIDV_LL_-XNOR3X13_P0**	**C8T28SOIDV_LL_-XNOR3X9_P0**	**C8T28SOIDV_LL_-XNOR3X13_P0**
A to Z ↓	0.0435	0.0508	2.0086	1.3716
A to Z ↑	0.0461	0.0531	2.7223	1.8848
B to Z ↓	0.0444	0.0517	2.0094	1.3726
B to Z ↑	0.0473	0.0544	2.7223	1.8843
C to Z ↓	0.0632	0.0772	2.0095	1.3726
C to Z ↑	0.0655	0.0799	2.7209	1.8848
	C8T28SOIDV_LLS_-XNOR3X1_P0	**C8T28SOIDV_LLS_-XNOR3X2_P0**	**C8T28SOIDV_LLS_-XNOR3X1_P0**	**C8T28SOIDV_LLS_-XNOR3X2_P0**
A to Z ↓	0.0297	0.0331	14.2145	7.5315
A to Z ↑	0.0314	0.0308	22.5349	11.7251
B to Z ↓	0.0307	0.0343	14.2320	7.5377
B to Z ↑	0.0322	0.0318	22.5354	11.7196
C to Z ↓	0.0296	0.0322	14.2324	7.5504
C to Z ↑	0.0315	0.0304	22.5111	11.7170
	C8T28SOIDV_LLS_-XNOR3X5_P0	**C8T28SOIDV_LLS_-XNOR3X7_P0**	**C8T28SOIDV_LLS_-XNOR3X5_P0**	**C8T28SOIDV_LLS_-XNOR3X7_P0**
A to Z ↓	0.0337	0.0282	3.5834	2.4751
A to Z ↑	0.0327	0.0276	5.7347	3.8348
B to Z ↓	0.0332	0.0274	3.5907	2.4817
B to Z ↑	0.0323	0.0272	5.7380	3.8369
C to Z ↓	0.0316	0.0265	3.5867	2.4824
C to Z ↑	0.0308	0.0260	5.7277	3.8328

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P0	6.485e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P0	7.857e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P0	1.407e-04	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P0	2.008e-04	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P0	4.210e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P0	7.544e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P0	1.802e-04	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P0	2.757e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P0	C8T28SOIDV_LL_-XNOR3X4_P0	C8T28SOIDV_LL_-XNOR3X9_P0	C8T28SOIDV_LL_-XNOR3X13_P0
A to Z	1.673e-03	2.030e-03	3.053e-03	5.190e-03
B to Z	1.667e-03	2.027e-03	3.078e-03	5.233e-03
C to Z	2.621e-03	3.019e-03	4.275e-03	7.097e-03
	C8T28SOIDV_LLS_-XNOR3X1_P0	C8T28SOIDV_LLS_-XNOR3X2_P0	C8T28SOIDV_LLS_-XNOR3X5_P0	C8T28SOIDV_LLS_-XNOR3X7_P0
A to Z	9.724e-04	1.441e-03	3.190e-03	4.302e-03
B to Z	9.743e-04	1.469e-03	3.248e-03	4.284e-03
C to Z	9.634e-04	1.458e-03	3.247e-03	4.289e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

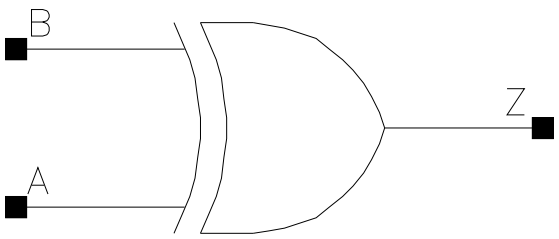
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P0	C8T28SOIDV_LL_-XNOR3X4_P0	C8T28SOIDV_LL_-XNOR3X9_P0	C8T28SOIDV_LL_-XNOR3X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P0	C8T28SOIDV_LLS_-XNOR3X2_P0	C8T28SOIDV_LLS_-XNOR3X5_P0	C8T28SOIDV_LLS_-XNOR3X7_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.360	1.0880
X4_P0	1.600	0.544	0.8704
X5_P0	0.800	1.360	1.0880
X8_P0	1.600	1.088	1.7408
X9_P0	0.800	1.496	1.1968
X12_P0	1.600	1.360	2.1760
X13_P0	0.800	2.176	1.7408
X15_P0	1.600	1.904	3.0464
X17_P0	0.800	2.312	1.8496
X18_P0	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P0	X4_P0	X5_P0	X8_P0
A	0.0004	0.0008	0.0006	0.0013
B	0.0009	0.0008	0.0010	0.0014
	X9_P0	X12_P0	X13_P0	X15_P0
A	0.0006	0.0022	0.0010	0.0025
B	0.0012	0.0016	0.0019	0.0021
	X17_P0	X18_P0		
A	0.0010	0.0014		
B	0.0019	0.0016		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X4_P0**	**X2_P0**	**X4_P0**
A to Z ↓	0.0408	0.0166	7.3994	3.6982
A to Z ↑	0.0402	0.0206	10.5141	9.8949
B to Z ↓	0.0317	0.0171	7.3609	3.7171
B to Z ↑	0.0330	0.0194	10.5164	9.8899
	X5_P0	**X8_P0**	**X5_P0**	**X8_P0**
A to Z ↓	0.0378	0.0215	3.8039	1.9880
A to Z ↑	0.0352	0.0247	5.3778	5.1526
B to Z ↓	0.0290	0.0227	3.7858	2.0017
B to Z ↑	0.0286	0.0236	5.3674	5.1507
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0366	0.0193	1.9909	1.3386
A to Z ↑	0.0352	0.0220	2.7847	3.4475
B to Z ↓	0.0282	0.0188	1.9835	1.3482
B to Z ↑	0.0280	0.0202	2.7818	3.4476
	X13_P0	**X15_P0**	**X13_P0**	**X15_P0**
A to Z ↓	0.0335	0.0210	1.3550	1.0370
A to Z ↑	0.0322	0.0256	1.9247	3.0673
B to Z ↓	0.0234	0.0204	1.3511	1.0440
B to Z ↑	0.0227	0.0235	1.9210	3.0641
	X17_P0	**X18_P0**	**X17_P0**	**X18_P0**
A to Z ↓	0.0353	0.0393	1.0260	1.0352
A to Z ↑	0.0335	0.0363	1.4411	1.3987
B to Z ↓	0.0252	0.0307	1.0238	1.0341
B to Z ↑	0.0242	0.0283	1.4381	1.3977

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P0	7.438e-05	1.000e-20
X4_P0	9.032e-05	1.000e-20
X5_P0	1.186e-04	1.000e-20
X8_P0	1.429e-04	1.000e-20
X9_P0	1.961e-04	1.000e-20
X12_P0	2.192e-04	1.000e-20
X13_P0	3.167e-04	1.000e-20
X15_P0	2.629e-04	1.000e-20
X17_P0	3.415e-04	1.000e-20
X18_P0	3.350e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P0	X4_P0	X5_P0	X8_P0
A to Z	2.022e-03	1.312e-03	2.581e-03	2.588e-03
B to Z	1.800e-03	1.294e-03	2.255e-03	2.601e-03
	X9_P0	X12_P0	X13_P0	X15_P0
A to Z	3.761e-03	3.629e-03	6.100e-03	4.721e-03
B to Z	3.347e-03	3.538e-03	4.260e-03	4.625e-03
	X17_P0	X18_P0		
A to Z	6.929e-03	7.694e-03		
B to Z	5.061e-03	6.130e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

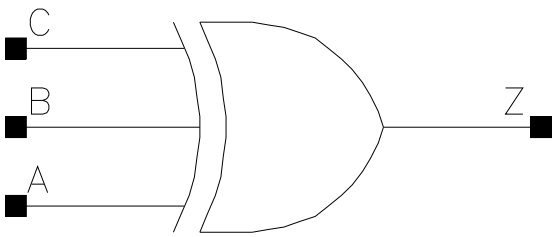
Pin Cycle (vdds)	X2_P0	X4_P0	X5_P0	X8_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P0	X12_P0	X13_P0	X15_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P0	X18_P0		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P0	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P0	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P0	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P0	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P0	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P0	C8T28SOIDV_LL_-XOR3X4_P0	C8T28SOIDV_LL_-XOR3X9_P0	C8T28SOIDV_LL_-XOR3X13_P0
A	0.0014	0.0013	0.0015	0.0022
B	0.0013	0.0014	0.0016	0.0021
C	0.0008	0.0008	0.0011	0.0018
	C8T28SOIDV_LLS_-XOR3X1_P0	C8T28SOIDV_LLS_-XOR3X2_P0	C8T28SOIDV_LLS_-XOR3X5_P0	C8T28SOIDV_LLS_-XOR3X7_P0

A	0.0014	0.0015	0.0025	0.0038
B	0.0015	0.0015	0.0025	0.0040
C	0.0005	0.0005	0.0005	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P0	**C8T28SOIDV_LL_-XOR3X4_P0**	**C8T28SOIDV_LL_-XOR3X2_P0**	**C8T28SOIDV_LL_-XOR3X4_P0**
A to Z ↓	0.0475	0.0522	7.8204	4.0075
A to Z ↑	0.0462	0.0497	10.5121	5.5739
B to Z ↓	0.0480	0.0533	7.8207	4.0083
B to Z ↑	0.0469	0.0510	10.5173	5.5730
C to Z ↓	0.0474	0.0525	7.8231	4.0093
C to Z ↑	0.0460	0.0497	10.5188	5.5771
	C8T28SOIDV_LL_-XOR3X9_P0	**C8T28SOIDV_LL_-XOR3X13_P0**	**C8T28SOIDV_LL_-XOR3X9_P0**	**C8T28SOIDV_LL_-XOR3X13_P0**
A to Z ↓	0.0465	0.0523	1.9941	1.3272
A to Z ↑	0.0476	0.0542	2.7334	1.8399
B to Z ↓	0.0477	0.0532	1.9951	1.3276
B to Z ↑	0.0489	0.0555	2.7348	1.8400
C to Z ↓	0.0464	0.0526	1.9955	1.3283
C to Z ↑	0.0470	0.0550	2.7361	1.8403
	C8T28SOIDV_LLS_-XOR3X1_P0	**C8T28SOIDV_LLS_-XOR3X2_P0**	**C8T28SOIDV_LLS_-XOR3X1_P0**	**C8T28SOIDV_LLS_-XOR3X2_P0**
A to Z ↓	0.0311	0.0346	9.8595	7.6986
A to Z ↑	0.0315	0.0308	16.1711	11.1773
B to Z ↓	0.0321	0.0353	9.8831	7.7055
B to Z ↑	0.0325	0.0315	16.1760	11.1726
C to Z ↓	0.0491	0.0529	9.8422	7.6704
C to Z ↑	0.0504	0.0500	16.1505	11.1335
	C8T28SOIDV_LLS_-XOR3X5_P0	**C8T28SOIDV_LLS_-XOR3X7_P0**	**C8T28SOIDV_LLS_-XOR3X5_P0**	**C8T28SOIDV_LLS_-XOR3X7_P0**
A to Z ↓	0.0464	0.0393	3.9583	2.7398
A to Z ↑	0.0392	0.0334	5.7811	3.8979
B to Z ↓	0.0440	0.0389	3.9706	2.7446
B to Z ↑	0.0383	0.0335	5.7859	3.9014
C to Z ↓	0.0736	0.0607	3.9697	2.7363
C to Z ↑	0.0684	0.0555	5.7719	3.8870

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P0	5.223e-05	1.000e-20
C8T28SOIDV_LL_XOR3X4_P0	6.764e-05	1.000e-20
C8T28SOIDV_LL_XOR3X9_P0	1.268e-04	1.000e-20
C8T28SOIDV_LL_XOR3X13_P0	1.888e-04	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P0	7.547e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P0	9.030e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P0	1.536e-04	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P0	2.305e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P0	C8T28SOIDV_LL_-XOR3X4_P0	C8T28SOIDV_LL_-XOR3X9_P0	C8T28SOIDV_LL_-XOR3X13_P0
A to Z	1.575e-03	2.031e-03	3.085e-03	5.478e-03
B to Z	1.567e-03	2.037e-03	3.115e-03	5.513e-03
C to Z	1.558e-03	2.021e-03	3.105e-03	5.528e-03
	C8T28SOIDV_LLS_-XOR3X1_P0	C8T28SOIDV_LLS_-XOR3X2_P0	C8T28SOIDV_LLS_-XOR3X5_P0	C8T28SOIDV_LLS_-XOR3X7_P0
A to Z	1.210e-03	1.487e-03	3.051e-03	4.189e-03
B to Z	1.217e-03	1.509e-03	3.115e-03	4.281e-03
C to Z	2.275e-03	2.617e-03	5.019e-03	6.870e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P0	C8T28SOIDV_LL_-XOR3X4_P0	C8T28SOIDV_LL_-XOR3X9_P0	C8T28SOIDV_LL_-XOR3X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P0	C8T28SOIDV_LLS_-XOR3X2_P0	C8T28SOIDV_LLS_-XOR3X5_P0	C8T28SOIDV_LLS_-XOR3X7_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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