C28SOI_IO_EXT_CSF_BASIC_EG User's Manual

Basic IO library in compatible standard frame designed in 28 nm FDSOI CMOS technology

Overview

The C28SOI_IO_EXT_CSF_BASIC_EG library includes supply, filler, fillercut, and corner cells in linear and two rows compatible standard frame.

Features

- Uses the standard process option and 28 Å gate oxide.
- Supports both single and 2 rows configurations for an IO ring[1].
- FC (Flip-chip) and CL (Cluster) frames provided

Application

These cells are used in 1.8 V IO ring.

Information Snapshot

Process Options

- GO1: SVT
- GO2: 28 Å

Packaging

- Flip-chip

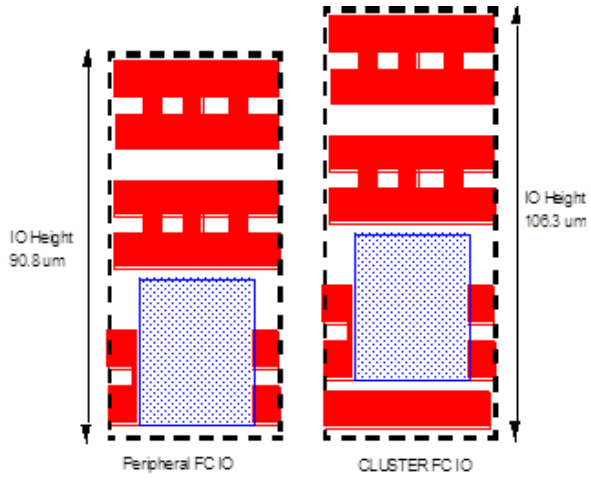
Table 1 : Operating Values

Symbol	Parameter	Min	Typ	Max	Unit
vdd	Supply voltage for 1.0 V node	*	1.0	1.1	V
vdde	Supply voltage for 1.8 V IO ring	*	1.8	1.95	V
$T_{junction}$	Operating junction temperature	-40	25	125	°C

* As per Design Platform specification

For more details about electrical specifications, please refer to *Section 3: Electrical Specifications*.

Figure 1 : Compatible standard frame topology



[1] Single row configuration is also called linear configuration.

1. Quick References

	*The document uses the following convention to indicate logic levels:* *L indicates logic low.* *H indicates logic high.* *X indicates don't care state.* *Z indicates high impedance state.* *'-' (Hyphen) indicates 'No activity'.*

	** suffixed in library name indicates multiple metallization options.* *** suffixed in cell name indicates multiple packages / configurations.*

1.1 Metal Stacking Convention

The metallization options supported by this library can be referred from its product package. The following is the convention that can be used to decode the segment in the library name:

- 7 metal option (5U1X2T8XLB) known as 5002 refers as follows:
  - 5U1X refers to the first 5 levels with 1X pitch (thin) metal.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 8 metal option (6U1X2T8XLB) known as 6002 refers as follows:
  - 6U1X refers to the first 6 levels with 1X pitch (thin) metal in ultra-low K.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 10 metal option (6U1X2U2X2T8XLB) known as 6202 refers as follows:
  - 6U1X refers to the first 6 levels with 1X pitch (thin) metal in ultra-low K.
  - 2U2X refers to the next 2 levels with 2X pitch (thin) metal in ultra-low K.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap

1.2 Reference Documentation

For details on the following topics:

- Power Sequencing Recommendation in IOs
- Specifications and Analysis of Overshoots and Undershoots
- SSN Application Notes
- ESD qualification
- Latch-up qualification
- Maturity information
- RDL recommended rules
  - ST users, refer to the IO Reference catalog
  - (http://ccds.st.com/cps/sections/library/io/io_reference_catalog/downloadFile/file/IO_Helpdesk_Solutions.pdf).
  - Non-ST users, contact Customer Support personnel

1.3 Reference Library

The C28SOI_IO_EXT_CSF_BASIC_EG library refers to some cells from 28nm FDSOI libraries listed below. For a correct usage, these libraries are mandatory:

- C28SOI_IO_ALLF_FRAMEKIT_EG
- C28SOI_IO_ALLF_IOSUPPLYKIT_EG

1.4 Acronyms and Abbreviations Used

Table 2 : Acronyms and Abbreviations

Acronym/Abbreviation	Description
B2B	Back-to-Back
CDM	Charge Device Model
DC	Direct Current
DRM	Design Rule Manual
ESD	Electrostatic Discharge
HBM	Human Body Model
FC	Flip-chip
CL	Cluster
MM	Machine Model
RMS	Root Mean Square
SVT	Standard V_T
2ROWS	Two rows

2.Functional Specifications

The C28SOI_IO_EXT_CSF_BASIC_EG library includes 82 top cells.

Table 3 : Cell List

Cell Name	Width x Height (µm)	Cell Description
Supply cells - linear compatible standard frame, FC view		
VDDE_EXT_CSF_FC_LIN	40 X 90.8	Linear power supply for IO ring
GNDE_EXT_CSF_FC_LIN	40 X 90.8	Linear ground supply for IO ring
VDD_EXT_CSF_FC_LIN	40 X 90.8	Linear power supply for core
GND_EXT_CSF_FC_LIN	40 X 90.8	Linear ground supply for core
Supply cells - linear compatible standard frame, CL view		
VDDE_EXT_CSF_CL_LIN	40 X 106.3	Linear power supply for IO cluster
GNDE_EXT_CSF_CL_LIN	40 X 106.3	Linear ground supply for IO cluster
VDD_EXT_CSF_CL_LIN	40 X 106.3	Linear power supply for core
GND_EXT_CSF_CL_LIN	40 X 106.3	Linear ground supply for core
Supply cells – 2ROWS compatible standard frame, FC view		
GND_VDD_EXT_CSF_FC_2ROWS	45 X 184.6	2ROWS power and ground supplies for core
VDD_GND_EXT_CSF_FC_2ROWS	45 X 184.6	2ROWS power and ground supplies for core
Supply cells – INNER compatible standard frame, FC view		
GNDE_EXT_CSF_FC_INNER	40 X 90.8	Inner ground supply for IO ring
VDDE_EXT_CSF_FC_INNER	40 X 90.8	Inner power supply for IO ring
Supply cells – OUTER compatible standard frame, FC view		
GNDE_EXT_CSF_FC_OUTER	45 X 184.6	Inner ground supply for IO ring
VDDE_EXT_CSF_FC_OUTER	45 X 184.6	Inner power supply for IO ring
Analog input cells – linear compatible standard frame, FC view		
WIRECELL_EXT_CSF_FC_LIN	40 X 90.8	Analog input IO pad for IO ring
WIRECELL_50OHM_EXT_CSF_FC_LIN	40 X 90.8	Analog input IO pad with 50ohms serial resistor for IO ring
Analog input cells – linear compatible standard frame, CL view		
WIRECELL_EXT_CSF_CL_LIN	40 X 106.3	Analog input IO pad for IO cluster
WIRECELL_50OHMS_EXT_CSF_CL_LIN	40 X 106.3	Analog input IO pad with 50ohms serial resistor for IO cluster

Table 3 : Cell List

Cell Name	Width x Height (µm)	Cell Description
Analog input cells – INNER compatible standard frame, FC view		
WIRECELL_EXT_CSF_FC_INNER	40 X 90.8	Analog input IO pad for IO ring
WIRECELL_50OHMS_EXT_CSF_FC_INNER	40 X 90.8	Analog input IO pad with 50ohms serial resistor for IO ring
Filler cells - linear compatible standard frame, FC view		
FILLCELL_1GRID_EXT_CSF_FC_LIN	0.1 X 90.8	1 placement grid filler
FILLCELL_1UM_EXT_CSF_FC_LIN	1 X 90.8	1 µm pitch filler
FILLCELL_5UM_EXT_CSF_FC_LIN	5 X 90.8	5 µm pitch filler
FILLCELL_10UM_EXT_CSF_FC_LIN	10 X 90.8	10 µm pitch filler
FILLCELL_REFASRC_EXT_CSF_FC_LIN	8.5 X 90.8	Connector for compensation cell.
FILLCELL_VDDE_GNDE_EXT_CSF_FC_LIN	8.5 X 90.8	Filler cell giving access to vdde and gnde at core side
FILLCELL_END_LEFT_EXT_CSF_FC_LIN	17 X 90.8	Filler closes left
FILLCELL_END_RIGHT_EXT_CSF_FC_LIN	17 X 90.8	Filler closes right
Filler cells - INNER compatible standard frame, FC view		
FILLCELL_1GRID_EXT_CSF_FC_INNER	0.1 X 90.8	1 placement grid filler
FILLCELL_1UM_EXT_CSF_FC_INNER	1 X 90.8	1 µm pitch filler
FILLCELL_5UM_EXT_CSF_FC_INNER	5 X 90.8	5 µm pitch filler
FILLCELL_10UM_EXT_CSF_FC_INNER	10 X 90.8	10 µm pitch filler
EMPTYCELL_EXT_CSF_FC_INNER	40 X 90.8	Empty IO cell including ESD protection
FILLCELL_END_LEFT_EXT_CSF_FC_INNER	17 X 90.8	Filler closes left
FILLCELL_END_RIGHT_EXT_CSF_FC_INNER	17 X 90.8	Filler closes right
Filler cells - OUTER compatible standard frame, FC view		
FILLCELL_1GRID_EXT_CSF_FC_OUTER	0.1 X 93.8	1 placement grid filler
FILLCELL_1UM_EXT_CSF_FC_OUTER	1 X 93.8	1 µm pitch filler
FILLCELL_5UM_EXT_CSF_FC_OUTER	5 X 93.8	5 µm pitch filler
FILLCELL_10UM_EXT_CSF_FC_OUTER	10 X 93.8	10 µm pitch filler
EMPTYCELL_EXT_CSF_FC_OUTER	45 X 184.6	Empty IO cell including ESD protection
Filler cells – 2ROWS compatible standard frame, FC view		
FILLCELL_1GRID_EXT_CSF_FC_2ROWS	0.1 X 184.6	1 placement grid filler
FILLCELL_1UM_EXT_CSF_FC_2ROWS	1 X 184.6	1 µm pitch filler
FILLCELL_5UM_EXT_CSF_FC_2ROWS	5 X 184.6	5 µm pitch filler

Table 3 : Cell List

Cell Name	Width x Height (µm)	Cell Description
FILLCELL_10UM_EXT_CSF_FC_2ROWS	10 X 184.6	10 µm pitch filler
FILLCELL_REFASRC_EXT_CSF_FC_2ROWS	8.5 X 184.6	Connector for compensation cell.
FILLCELL_VDDE_GNDE_EXT_CSF_FC_2ROWS	8.5 X 184.6	Filler cell giving access to vdde and gnde at core side
FILLCELL_END_LEFT_EXT_CSF_FC_2ROWS	21 X 184.6	Filler closes left
FILLCELL_END_RIGHT_EXT_CSF_FC_2ROWS	21 X 184.6	Filler closes right
Filler cells - linear compatible standard frame, CL view		
FILLCELL_1GRID_EXT_CSF_CL_LIN	0.1 X 106.3	1 placement grid filler cell.
FILLCELL_1UM_EXT_CSF_CL_LIN	1 X 106.3	1 µm pitch filler cell.
FILLCELL_5UM_EXT_CSF_CL_LIN	5 X 106.3	5 µm pitch filler
FILLCELL_10UM_EXT_CSF_CL_LIN	10 X 106.3	10 µm pitch filler
FILLCELL_REFASRC_EXT_CSF_CL_LIN	8.5 X 106.3	Connector for compensation cell.
FILLCELL_VDDE_GNDE_EXT_CSF_CL_LIN	8.5 X 106.3	Filler cell giving access to vdde and gnde at core side
FILLCELL_FEEDTHROUGH_40UM_EXT_CSF_CL_LIN	40 X 106.3	Filler cell giving possibility to route through an IO cluster
FILLCELL_END_LEFT_EXT_CSF_CL_LIN	17 X 106.3	Filler closes left
FILLCELL_END_RIGHT_EXT_CSF_CL_LIN	17 X 106.3	Filler closes right
Fillercut cells - linear compatible standard frame, FC view		
FILLCUTCELL_ALL_EXT_CSF_FC_LIN	14 X 90.8	Cuts all nodes
FILLCUTCELL_VDDE_EXT_CSF_FC_LIN	1.6 X 90.8	Cuts vdde node
FILLCUTCELL_VDDE_GNDE_EXT_CSF_FC_LIN	1.6 X 90.8	Cuts vdde and gnde nodes
FILLCUTCELL_GNDE_EXT_CSF_FC_LIN	1.6 X 90.8	Cuts gnde node
FILLCUTCELL_REFASRC_EXT_CSF_FC_LIN	1.6 X 90.8	Cuts ASRC and REF rails
FILLCUTCELL_VDD_EXT_CSF_FC_LIN	1.6 X 90.8	Cuts vdd node
Fillercut cells – 2ROWS compatible standard frame, FC view		
FILLCUTCELL_ALL_EXT_CSF_FC_2ROWS	14 X 184.6	Cuts all nodes
FILLCUTCELL_VDDE_EXT_CSF_FC_2ROWS	1.6 X 184.6	Cuts vdde node
FILLCUTCELL_VDDE_GNDE_EXT_CSF_FC_2ROWS	1.6 X 184.6	Cuts vdde and gnde nodes
FILLCUTCELL_GNDE_EXT_CSF_FC_2ROWS	1.6 X 184.6	Cuts gnde node
FILLCUTCELL_REFASRC_EXT_CSF_FC_2ROWS	1.6 X 184.6	Cuts ASRC and REF rails
FILLCUTCELL_VDD_EXT_CSF_FC_2ROWS	1.6 X 184.6	Cuts vdd node.
Fillercut cells - linear compatible standard frame, CL view		

Table 3 : Cell List

Cell Name	Width x Height (µm)	Cell Description
FILLCUTCELL_VDDE_EXT_CSF_CL_LIN	3.5 X 106.3	Cuts vdde node
FILLCUTCELL_VDDE_GNDE_EXT_CSF_CL_LIN	3.5 X 106.3	Cuts vdde and gnde nodes
FILLCUTCELL_GNDE_EXT_CSF_CL_LIN	1.6 X 106.3	Cuts gnde node
FILLCUTCELL_REFASRC_EXT_CSF_CL_LIN	1.6 X 106.3	Cuts ASRC and REF rails
FILLCUTCELL_VDD_EXT_CSF_CL_LIN	1.6 X 106.3	Cuts vdd node
Corner cells - linear compatible standard frame, FC view		
RTCORNERCELL_EXT_CSF_FC_LIN	90.8 X 90.8	Right-top corner
LTCORNERCELL_EXT_CSF_FC_LIN	90.8 X 90.8	Left-top corner
RBCORNERCELL_EXT_CSF_FC_LIN	90.8 X 90.8	Right-bottom corner
LBCORNERCELL_EXT_CSF_FC_LIN	90.8 X 90.8	Left-bottom corner
Corner cells – 2ROWS compatible standard frame, FC view		
RTCORNERCELL_EXT_CSF_FC_2ROWS	184.6 X 184.6	Right-top corner
LTCORNERCELL_EXT_CSF_FC_2ROWS	184.6 X 184.6	Left-top corner
RBCORNERCELL_EXT_CSF_FC_2ROWS	184.6 X 184.6	Right-bottom corner
LBCORNERCELL_EXT_CSF_FC_2ROWS	184.6 X 184.6	Left-bottom corner

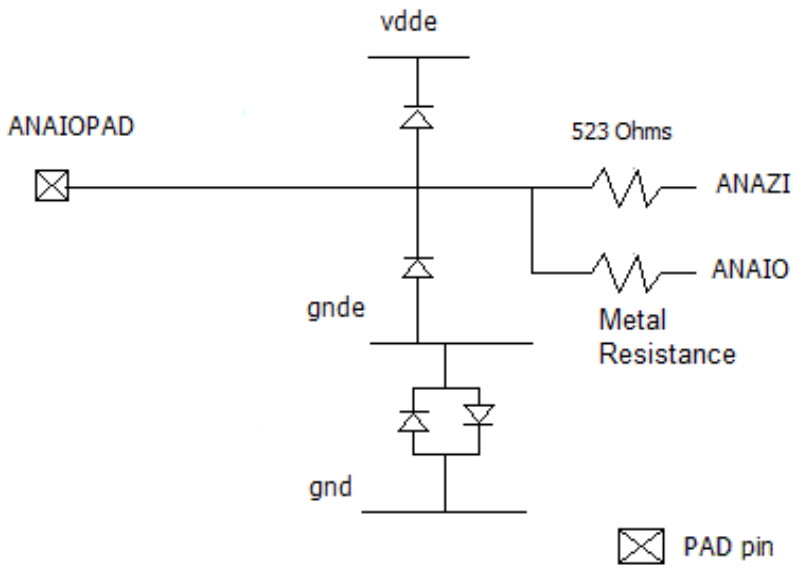
The ALLCELLS cells are not considered part of the Deliverable. These cells are specifically for QA check and hence subject to change, without prior notice.

2.1 Analog input cells

2.1.1 WIRECELL_EXT_CSF_FC_LIN / CL_LIN / FC_INNER

2.1.1.1. Functional Diagram

Figure 2 : Block Diagram



2.1.1.2. Interface Description

Table 4 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
ANAIOPAD	Input / Output	0 to vdde	Analog node without series resistor, pad side
Logic core pins			
ANAIO	Input / Output	0 to vdde	Analog node without series resistor, core side
ANAZI	Input / Output	0 to vdde	Input node varying between vdde and gnde without series resistor, core side
Track pins			
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.1.1.3. Cell Information

Table 5 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdde node)	-	-	22	nA
		Fast Process, Max voltage, 125˚C (vdde node)	-	-	24	
I_{DC}	DC current Pad to core [1]	110˚C (ANAIO node)	-	-	49	mA
		125˚C (ANAIO node)	-	-	17	
		110˚C (ANAZI node)	-	-	0.77	
		125˚C (ANAZI node)	-	-	0.27	
	DC current Pad to core [2]	110˚C (ANAIO node)	-	-	38	
		125˚C (ANAIO node)	-	-	17	
		110˚C (ANAZI node)	-	-	0.77	
		125˚C (ANAZI node)	-	-	0.27	
I_{RMS}	RMS current Pad to core [1]	100˚C (ANAIO node)	-	-	135	mA
		100˚C (ANAZI node)	-	-	5	
	RMS current Pad to core [2]	100˚C (ANAIO node)	-	-	103	
		100˚C (ANAZI node)	-	-	5	
$R_{PadToCore}$	Resistance Pad to core	25˚C (ANAIO node)	-	-	460	mΩ
		25˚C (ANAZI node)	-	-	523	Ω
C_{Par}	Parasitic capacitance (without Bump)	Corner TT, 125˚C (ANAIOPAD node)	-	-	1380	fF
	Parasitic capacitance (with BUMP_FC61A_96X96)	Corner TT, 125˚C (ANAIOPAD node)	-	-	1460 [3]	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

[3] The parasitic capacitance value depends on the type and the position of bump.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

2.1.1.4. Functional Description

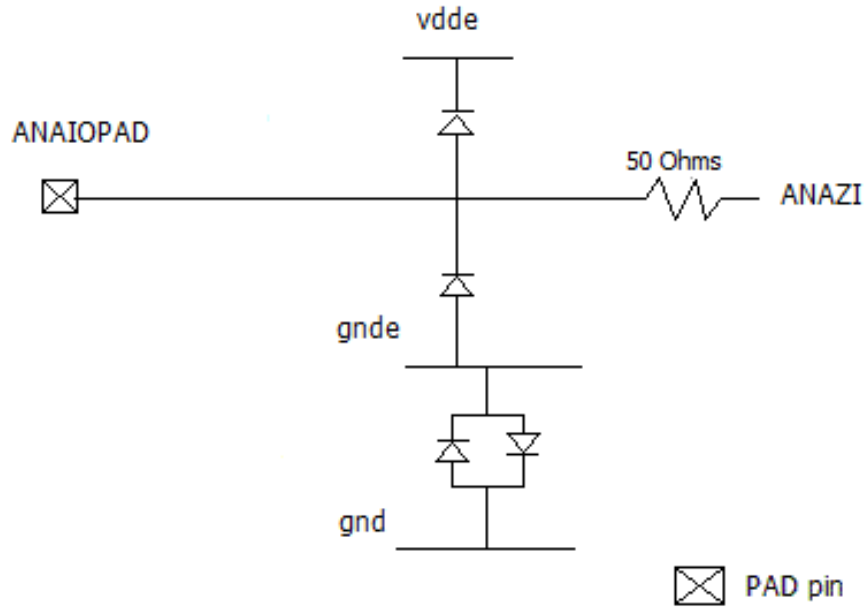
This cell is designed to interface analog signals between the core and the external domain. The analog signal to the core can be tapped at two pins, ANAZI and ANAIOPAD. The ANAZI pin connects the pad pin to the core through a 523 Ohm series resistor. It is mandatory to connect an input buffer or a transistor gate to this resistor.
If the current has to flow in the analog interface from core to external circuit, the ANAIO pin should be used.

For 2ROWS sections WIRECELL is not provided in outer row, it is not compatible with pad to core current specification of the cell

2.1.2 WIRECELL_50OHMS_EXT_CSF_FC_LIN / CL_LIN / FC_INNER

2.1.2.1. Functional Diagram

Figure 3 : Block Diagram



2.1.2.2. Interface Description

Table 6 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
ANAIOPAD	Input / Output	0 to vdde	Analog node without series resistor, pad side
Logic core pins			
ANAZI	Input / Output	0 to vdde	Input node varying between vdde and gnde with 50 ohms series resistor, core side
Track pins			
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.1.2.3. Cell Information

Table 7 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdde node)	-	-	22	nA
		Fast Process, Max voltage, 125˚C (vdde node)	-	-	24	
I_{DC}	DC current Pad to core [1]	110˚C (ANAZI node)	-	-	0.77	mA
		125˚C (ANAZI node)	-	-	0.27	
	DC current Pad to core [2]	100˚C (ANAZI node)	-	-	0.77	
		100˚C (ANAZI node)	-	-	0.27	
I_{RMS}	RMS current Pad to core [1]	100˚C (ANAZI node)	-	-	5	mA
	RMS current Pad to core	100˚C (ANAZI node)	-	-	5	
$R_{PadToCore}$	Resistance Pad to core [2]	25˚C (ANAZI node)	-	-	50	Ω
C_{Par}	Parasitic capacitance (without Bump)	Corner TT, 125˚C (ANAIOPAD node)	-	-	1380	fF
	Parasitic capacitance (with BUMP_FC61A_96X96)	Corner TT, 125˚C (ANAIOPAD node)	-	-	1460 [3]	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

[3] The parasitic capacitance value depends on the type and the position of bump.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

2.1.2.4. Functional Description

This cell is designed to interface analog signals between the core and the external domain. The analog signal to the core is connected to ANAIO pin through a 50 ohms resistor.

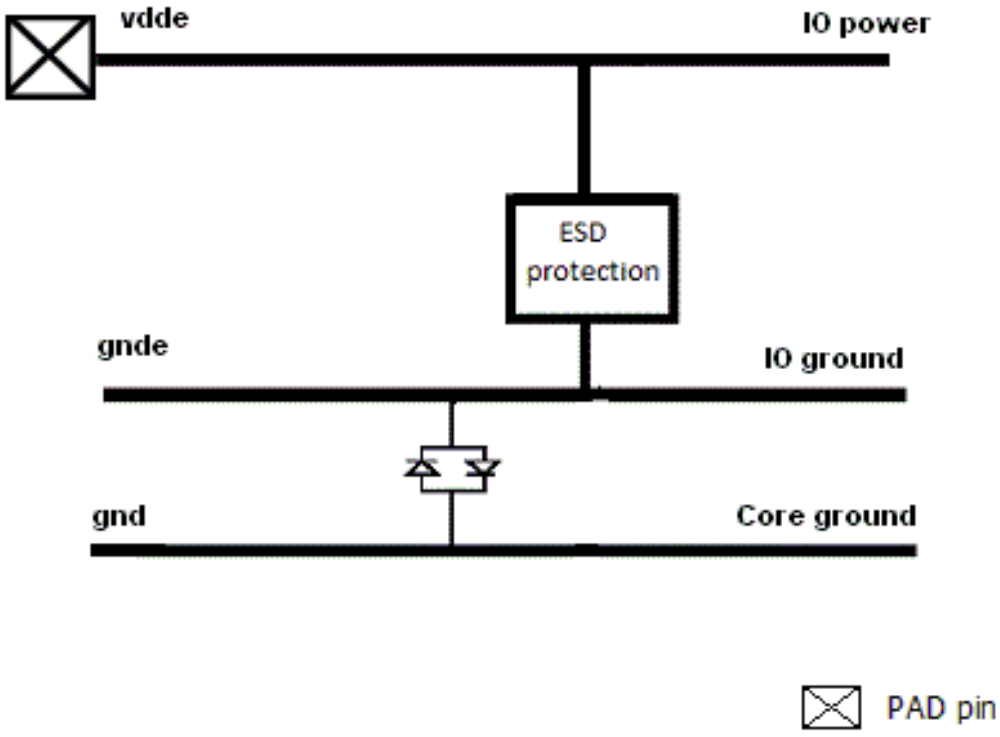
For 2ROWS sections WIRECELL is not provided in outer row, it is not compatible with pad to core current specification of the cell

2.2 Supply Cells

2.2.1 VDDE_EXT_CSF_FC_LIN / CL_LIN / FC_INNER / FC_OUTER

2.2.1.1. Functional Diagram

Figure 4 : Block Diagram



2.2.1.2. Interface Description

Table 8 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vdde	Input / Output	vdde	IO power node, pad side
Track pins			
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.2.1.3. Cell Information

Table 9 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdde node)	-	-	309	nA
		Fast Process, Max voltage, 125˚C (vdde node)	-	-	2.5	µA
I_{DC}	DC current Pad to rails [2]	110°C (vdde node) [1]	-	-	179	mA
		125°C (vdde node) [1]	-	-	64	
	DC current Pad to rails [3]	110°C (vdde node) [1]	-	-	38	
		125°C (vdde node) [1]	-	-	22	
I_{RMS}	RMS current Pad to rails [2]	100°C (vdde node) [1]	-	-	236	mA
	RMS current Pad to rails [3]	100°C (vdde node) [1]	-	-	103	

[1] Propagated through track pins.

[2] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[3] Considering min RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [3].
DC/RMS current values of RDL should be checked accordingly at chip level.

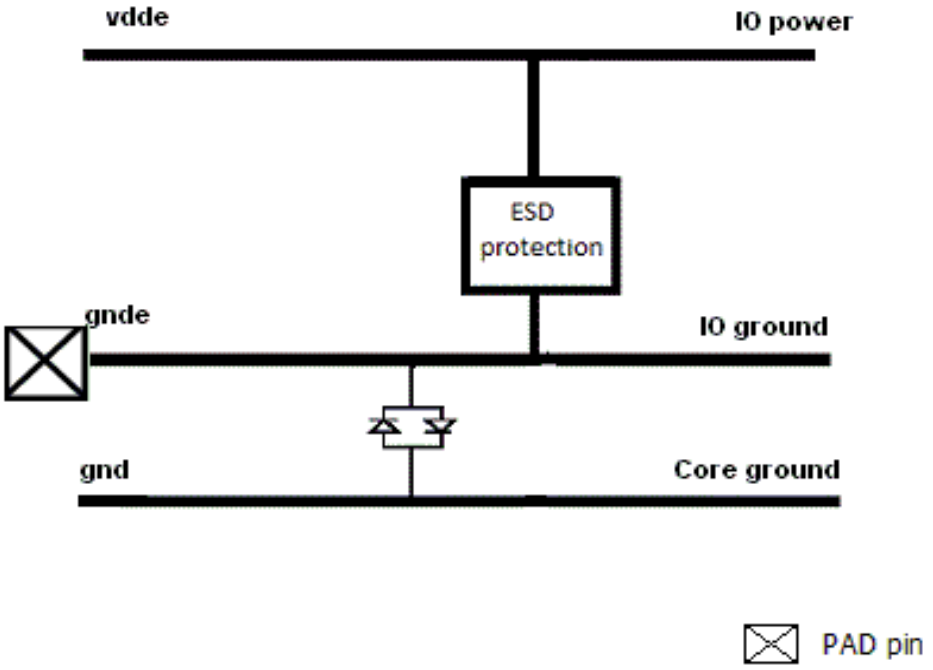
2.2.1.4. Functional Description

These cells provide vdde supply connections used for IOs cells in the pad ring.

2.2.2 GNDE_EXT_CSF_FC_LIN / CL_LIN / FC_INNER / FC_OUTER

2.2.2.1. Functional Diagram

Figure 5 : Functional Diagram



2.2.2.2. Interface Description

Table 10 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
gnde	Input / Output	0	IO ground node, pad side
Track pins			
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.2.2.3. Cell Information

Table 11 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdde node)	-	-	309	nA
		Fast Process, Max voltage, 125˚C (vdde node)	-	-	2.5	µA
I_{DC}	DC current Pad to rails [2]	110°C (gnde node) [1]	-	-	178	mA
		125°C (gnde node) [1]	-	-	64	
	DC current Pad to rails [3]	110°C (gnde node) [1]	-	-	38	
		125°C (gnde node) [1]	-	-	22	
I_{RMS}	RMS current Pad to rails [2]	100°C (gnde node) [1]	-	-	195	mA
	RMS current Pad to rails [3]	100°C (gnde node) [1]	-	-	103	

[1] Propagated through track pins.

[2] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[3] Considering min RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [3].
DC/RMS current values of RDL should be checked accordingly at chip level.

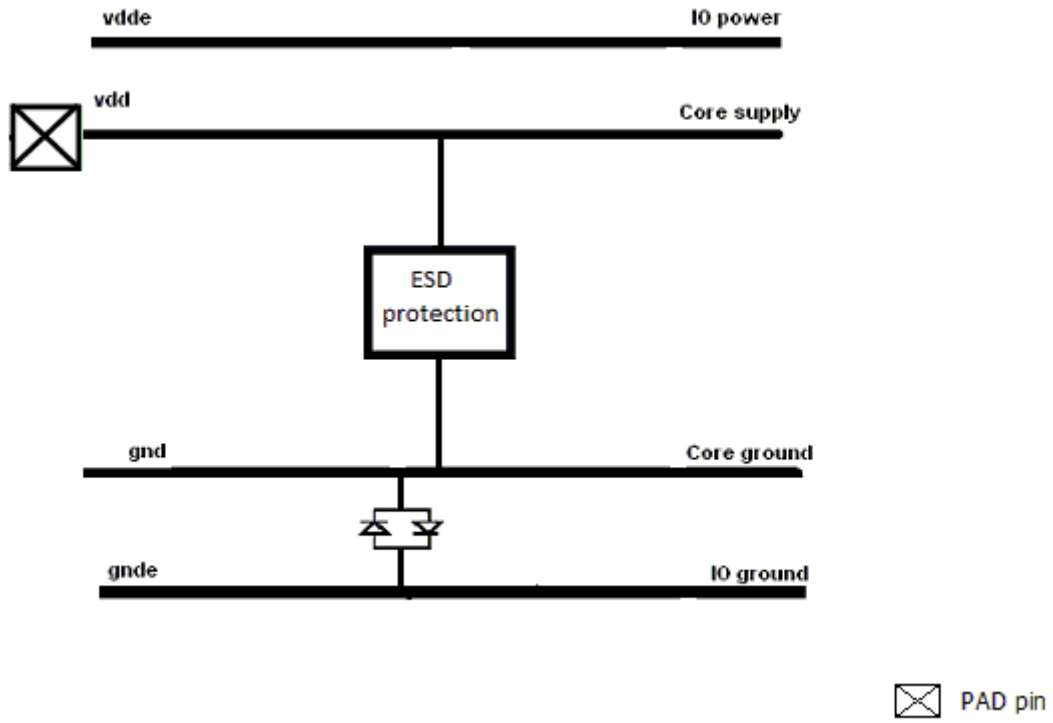
2.2.2.4. Functional Description

These cells provide gnde ground connections used for IOs cells in the pad ring.

2.2.3 VDD_EXT_CSF_FC_LIN / CL_LIN

2.2.3.1. Functional Diagram

Figure 6 : Functional Diagram



2.2.3.2. Interface Description

Table 12 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vdd	Input / Output	vdd	Core power node, pad side
Track pins			
vdde	Input / Output	vdde	IO power node
vdd	Input / Output	vdd	Core power node
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.2.3.3. Cell Information

Table 13 : Cell Information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdd node)	-	-	22	nA
		Fast Process, Max voltage, 125˚C (vdd node)	-	-	3.9	µA
I_{DC}	DC current Pad to core [1]	110°C (vdd node)	-	-	117	mA
		125°C (vdd node)	-	-	41	
	DC current Pad to core [2]	110°C (vdd node)	-	-	38	
		125°C (vdd node)	-	-	22	
I_{RMS}	RMS current Pad to core [1]	100°C (vdd node)	-	-	128	mA
	RMS current Pad to core [2]	100°C (vdd node)	-	-	103	
$R_{PadToCore}$	Pad to core resistance	25°C (Pad vdd to IA core pin)	-	-	85	mΩ

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints

[2] Considering min RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

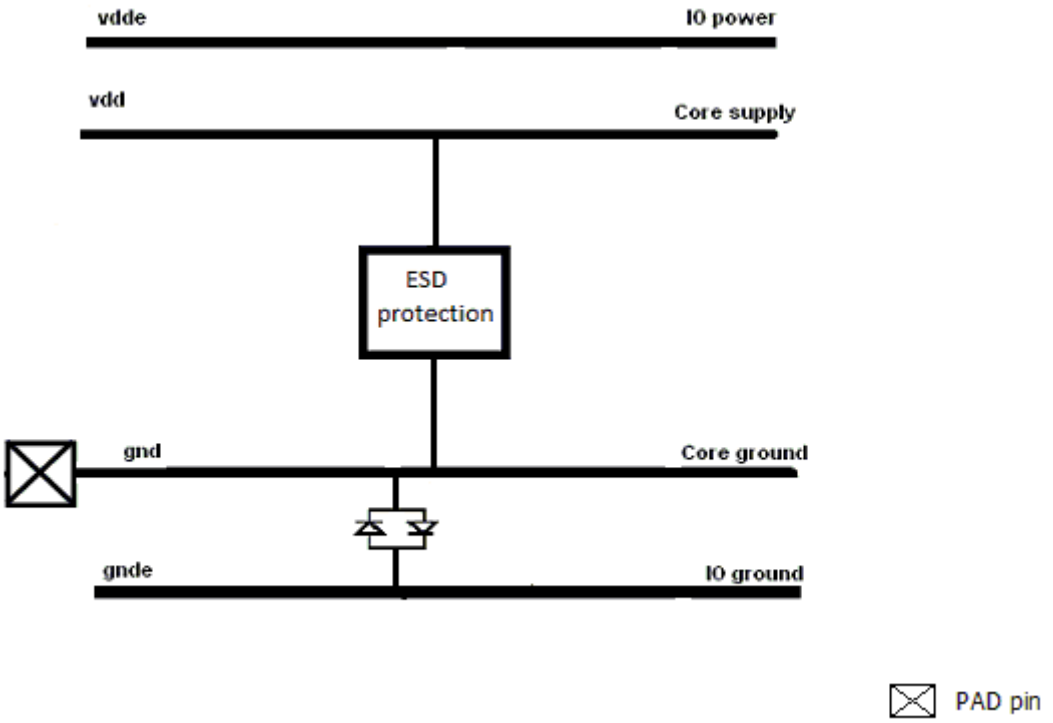
2.2.3.4. Functional Description

These cells provide power (vdd) connections, to the core and to the pad ring.

2.2.4 GND_EXT_CSF_FC_LIN / CL_LIN

2.2.4.1. Functional Diagram

Figure 7 : Functional Diagram



2.2.4.2. Interface Description

Table 14 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
gnd	Input / Output	0	Core and substrate ground node, pad side
Track pins			
vdde	Input / Output	vdde	IO power node
vdd	Input / Output	vdd	Core power node
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.2.4.3. Cell Information

Table 15 : Cell Information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdd node)	-	-	22	nA
		Fast Process, Max voltage, 125˚C (vdd node)	-	-	3.9	µA
I_{DC}	DC current Pad to core [1]	110°C (gnd node)	-	-	107	mA
		125°C (gnd node)	-	-	38	
	DC current Pad to core [2]	110°C (gnd node)	-	-	38	
		125°C (gnd node)	-	-	22	
I_{RMS}	RMS current Pad to core [1]	100°C (gnd node)	-	-	137	mA
	RMS current Pad to core [2]	100°C (gnd node)	-	-	103	
$R_{PadToCore}$	Pad to core resistance	25°C (Pad gnd to IB core pin)	-	-	85	mΩ

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints

[2] Considering min RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

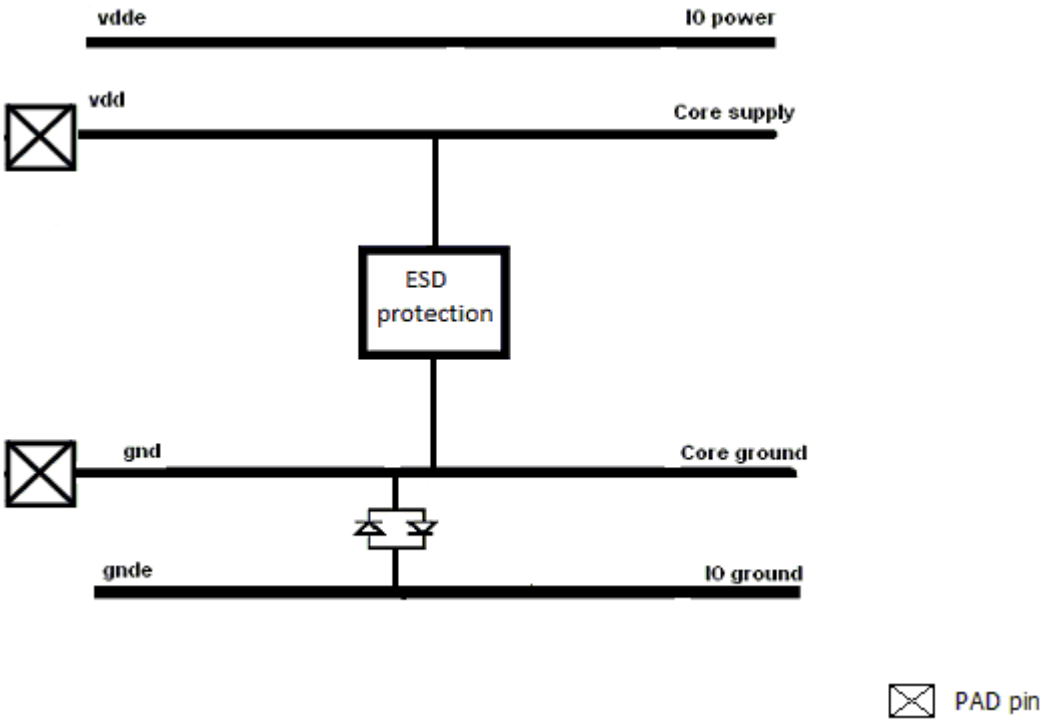
2.2.4.4. Functional Description

These cells provide ground (gnd) connections, to the core and to the pad ring.

2.2.5 GND_VDD_EXT_CSF_FC_2ROWS and VDD_GND_EXT_CSF_FC_2ROWS

2.2.5.1. Functional Diagram

Figure 8 : Functional Diagram



2.2.5.2. Interface Description

Table 16 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vdd	Input / Output	vdd	Core power node, pad side
gnd	Input / Output	0	Core and substrate ground node, pad side
Track pins			
vdde	Input / Output	vdde	IO power node
vdd	Input / Output	vdd	Core power node
gnde	Input / Output	0	IO ground node
gnd	Input / Output	0	Core and substrate ground node

2.2.5.3. Cell Information

Table 17 : Cell Information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdd node)	-	-	44	nA
		Fast Process, Max voltage, 125˚C (vdd node)	-	-	7.8	µA
I_{DC}	DC current Pad to core [1] VDD_GND_EXT_CSF_FC _2ROWS	110°C (vdd node)	-	-	91	mA
		110°C (gnd node)	-	-	114	
		125°C (vdd node)	-	-	32	
		125°C (gnd node)	-	-	40	
	DC current Pad to core [1] GND_VDD_EXT_CSF_FC _2ROWS	110°C (vdd node)	-	-	91	mA
		110°C (gnd node)	-	-	114	
		125°C (vdd node)	-	-	32	
		125°C (gnd node)	-	-	40	
	DC current Pad to core [2]	110°C (vdd / gnd node)	-	-	38	mA
		125°C (vdd / gnd node)	-	-	22	
I_{RMS}	RMS current Pad to core [1] VDD_GND_EXT_CSF_FC _2ROWS	100°C (vdd node)	-	-	99	mA
		100°C (gnd node)			123	
	RMS current Pad to core [1] GND_VDD_EXT_CSF_FC _2ROWS	100°C (vdd node)			119	mA
		100°C (gnd node)			125	
	RMS current Pad to core [2]	100°C (vdd / gnd node)	-	-	103	mA
$R_{PadToCore}$	Pad to core resistance VDD_GND_EXT_CSF_FC _2ROWS	25°C (Pad vdd to IA core pin)	-	-	403	mΩ
		25°C (Pad gnd to IB core pin)	-	-	115	
	Pad to core resistance GND_VDD_EXT_CSF_FC _2ROWS	25°C (Pad vdd to IA core pin)	-	-	408	
		25°C (Pad gnd to IB core pin)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints

[2] Considering min RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

2.2.5.4. Functional Description

These cells provide power and ground (vdd and gnd) connections, to the core and to the pad ring.

2.3 FILLER CELLS

2.3.1 FILLCELL_1GRID / 1UM / 5UM / 10UM_EXT_CSF_FC_LIN / FC_INNER / FC_OUTER / CL_LIN

2.3.1.1. Functional Description

These cells are used as a filler cells.

2.3.2 FILLCELL_VDDE_GNDE_EXT_CSF_FC_LIN / CL_LIN / FC_2ROWS

2.3.2.1. Cell information

Table 18 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
I_{DC}	DC current Rails to core	110°C (vdde / gnde node)	-	-	11	mA
		125°C (vdde / gnde node)	-	-	4	
I_{RMS}	RMS current Rails to core	100°C (vdde / gnde node)	-	-	22	mA
$R_{Rails\ to\ core}$	Rails to core resistance	25°C (gnde node)	-	-	300	mΩ
		25°C (vdde node)	-	-	500	mΩ

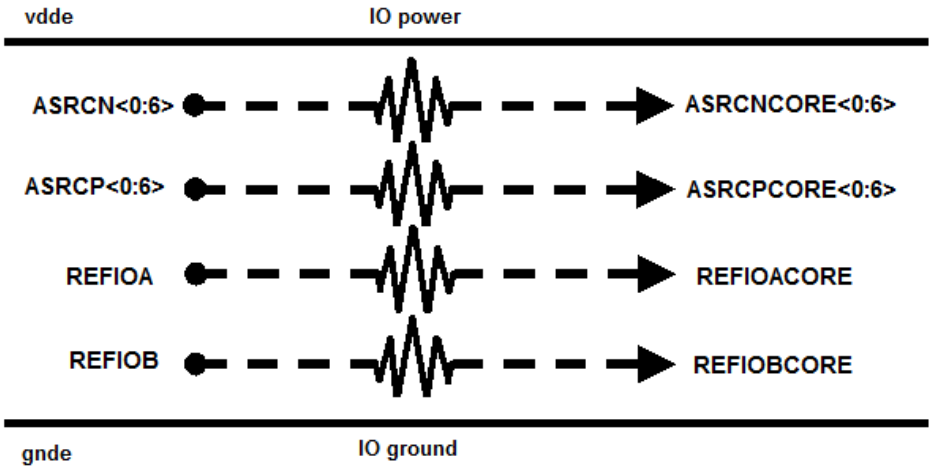
2.3.2.2. Functional Description

This cell is used as a filler cell. It cuts the ‘gnd’ core pin to provide both ‘vdde’ and ‘gnde’ access to core in thick metal ‘IB’. It should be placed once for every compensation cell placed on the chip.

2.3.3 FILLCELL_REFASRC_EXT_CSF_FC_LIN / CL_LIN / FC_2ROWS

2.3.3.1. Functional Diagram

Figure 9 : Block Diagram



2.3.3.2. Interface Description

Table 19 : Pin Description

Pin	Type	Voltage Level (V)	Description
Logic pins [1]			
ASRCN<0:6>	Input/Output	0 or vdde	ASRCN <0:6> signal nodes
ASRCNCORE<0:6>	Input/Output	0 or vdde	ASRCN <0:6> signal nodes, core side
ASRCP<0:6>	Input/Output	0 or vdde	ASRCP <0:6> signal nodes
ASRCPCORE<0:6>	Input/Output	0 or vdde	ASRCP <0:6> signal nodes, core side
REFIOA	Input/Output	Vref	REFIOA reference node
REFIOACORE	Input/Output	Vref	REFIOA reference node, core side
REFIOB	Input/Output	Vref	REFIOB reference node
REFIOBCORE	Input/Output	Vref	REFIOB reference node, core side
Track pins			
gnde	Input/Output	0	IO ground node
vdde	Input/Output	vdde	IO power node

[1] Logic pins are digital. Hence, ensure that all the input pins are either tied to ground or to their respective supply levels depending upon the mode of operation of the IO cell. Floating input pins are not allowed.

2.3.3.3. Cell Information

Table 20 : Cell Information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdde node)	-	-	< 150	pA
		Fast Process, Max voltage, 125˚C (vdde node)	-	-	< 150	

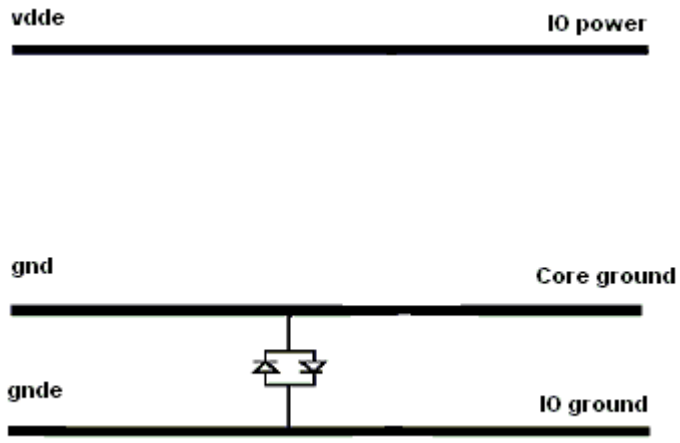
2.3.3.4. Functional Description

The FILLCELL_REFASRC_EXT_CSF_FC_LIN/CL_LIN cells are designed to act as the ASRCN <0:6>, ASRCP <0:6>, REFIOA, and REFIOB signal connector to core compensation cell and reference cell.

2.3.4 EMPTYCELL_EXT_CSF_FC_INNER / OUTER

2.3.4.1. Functional Diagram

Figure 10 : Block Diagram



2.3.4.2. Interface Description

Table 21 : Pin Description

Pin	Type	Voltage Level (V)	Description
Track pins			
vdde	Input / Output	vdde	IO power node
gnd	Input / Output	0	Core and substrate ground node
gnde	Input / Output	0	IO ground node

2.3.4.3. Cell Information

Table 22 : Cell Information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdde node)	-	-	< 150	pA
		Fast Process, Max voltage, 125˚C (vdde node)	-	-	< 150	

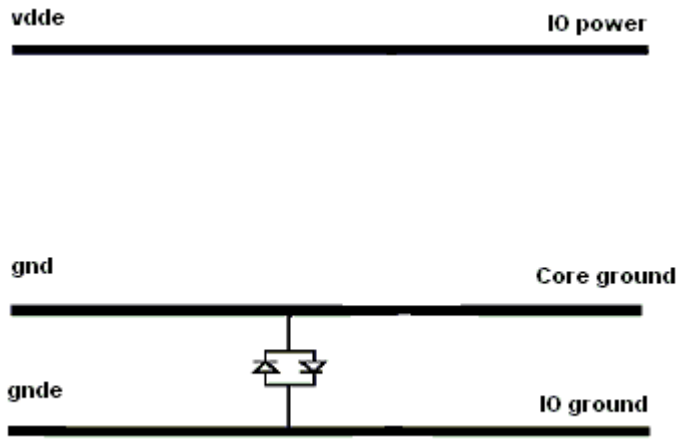
2.3.4.4. Functional Description

EMPTYCELLs are IO supply cells without pad. They aim at filling a row (inner or outer) of a double row ring, instead of an IO, and providing signal connection between the two rows, in the same way as IO cells do.

2.3.5 FILLCELL_FEEDTHROUGH_40UM_EXT_CSF_CL_LIN

2.3.5.1. Functional Diagram

Figure 11 : Block Diagram



2.3.5.2. Interface Description

Table 23 : Pin Description

Pin	Type	Voltage Level (V)	Description
Track pins			
vdde	Input / Output	vdde	IO power node
gnd	Input / Output	0	Core and substrate ground node
gnde	Input / Output	0	IO ground node

2.3.5.3. Cell Information

Table 24 : Cell Information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdde node)	-	-	< 150	pA
		Fast Process, Max voltage, 125˚C (vdde node)	-	-	< 150	

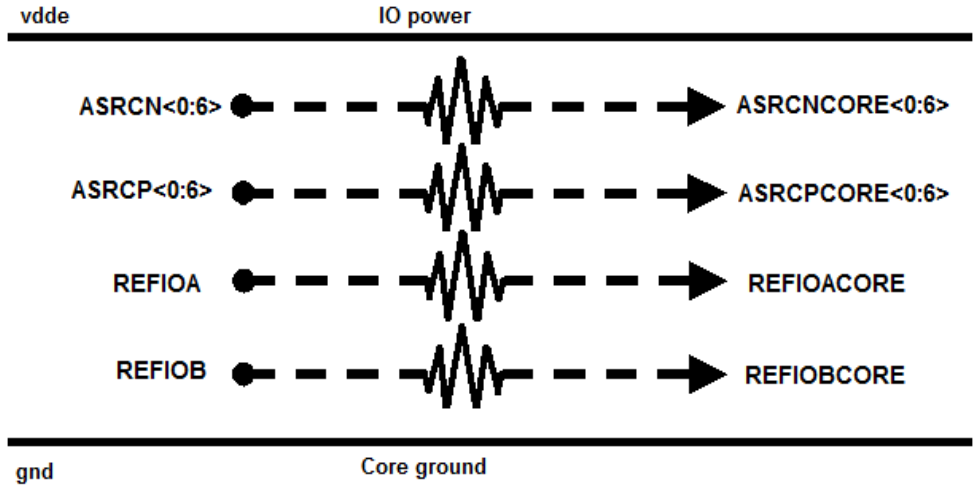
2.3.5.4. Functional Description

This cell is provided only on CL view. It provides routing possibility through the IO cluster with M2, M3 and M4.

2.3.6 FILLCELL_END_LEFT /RIGHT_EXT_CSF_FC / CL_LIN / FC_INNER / FC_2ROWS

2.3.6.1. Functional Diagram

Figure 12 : Block Diagram



2.3.6.2. Interface Description

Table 25 : Pin Description for CORNER Cells

Pin	Type	Voltage Level (V)	Description
Logic pins [1]			
ASRCN<0:6>	Input/Output	0 or vdde	ASRCN <0:6> signal nodes
ASRCNCORE<0:6>	Input/Output	0 or vdde	ASRCN <0:6> signal nodes, core side
ASRCP<0:6>	Input/Output	0 or vdde	ASRCP <0:6> signal nodes
ASRCPCORE<0:6>	Input/Output	0 or vdde	ASRCP <0:6> signal nodes, core side
REFIOA	Input/Output	Vref	REFIOA reference node
REFIOACORE	Input/Output	Vref	REFIOA reference node, core side
REFIOB	Input/Output	Vref	REFIOB reference node
REFIOBCORE	Input/Output	Vref	REFIOB reference node, core side
Track pins			
gnd	Input/Output	0	Core and substrate ground node
vdde	Input/Output	vdde	IO power node

[1] Logic pins are digital. Hence, ensure that all the input pins are either tied to ground or to their respective supply levels depending upon the mode of operation of the IO cell. Floating input pins are not allowed.

2.3.6.3. Cell Information

Table 26 : Cell Information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdde node)	-	-	< 150	pA
		Fast Process, Max voltage, 125˚C (vdde node)	-	-	< 150	

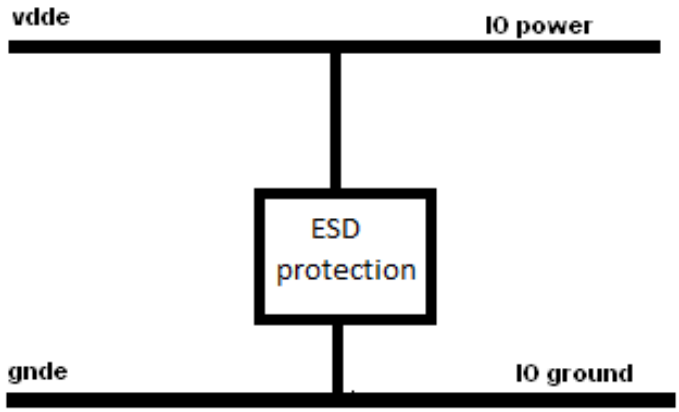
2.3.6.4. Functional Description

The purpose of FILLCELL_END_LEFT_EXT_CSF_** and FILLCELL_END_RIGHT_EXT_CSF_** is to provide a latch-up guard ring, to hang to the power core grid on right and left sides and to allow compensation cell placement beside . It provides core pins for vdd, gnd, ASRCNCORE<0:6>, ASRCPCORE<0:6>, REFIOACORE, and REFIOBCORE.

2.4 LB/LT/RB/RTCORNERCELL_EXT_CSF_FC_LIN / FC_2ROWS

2.4.1 Functional Diagram

Figure 13 : Block Diagram



2.4.2 Interface Description

Table 27 : Pin Description

Pin	Type	Voltage Level (V)	Description
Track pins			
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node

2.4.3 Cell Specifications

Table 28 : Cell Specifications for LB/LT/RB/RTCORNERCELL_EXT_CSF_FC_LIN

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current for *CORNERCELL_*_LIN cells	Fast Process, Max voltage, 25˚C (vdde node)	-	-	318	nA
		Fast Process, Max voltage, 125˚C (vdde node)	-	-	2.5	µA
	Leakage current for *CORNERCELL_*_2ROWS cells	Fast Process, Max voltage, 25˚C (vdde node)	-	-	636	nA
		Fast Process, Max voltage, 125˚C (vdde node)	-	-	5	µA

2.4.4 Functional Description

The corner cell is used to maintain rails continuity in the IO ring at chip corners. The following table lists the type of corner cells along with their position in the IO ring. Corner includes the full clamp.

Table 29 : Corner Cell Usage

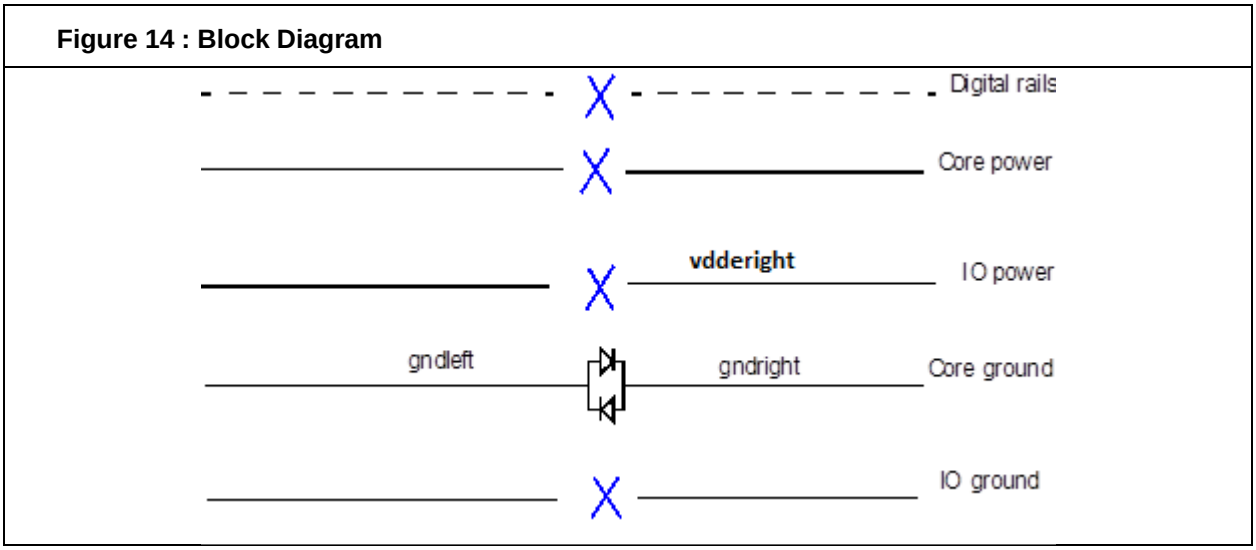
Type	Description
LBCORNERCELL	Left bottom corner
LTCORNERCELL	Left top corner
RBCORNERCELL	Right bottom corner
RTCORNERCELL	Right top corner

2.5 FILLERCUT CELLS

2.5.1 FILLCUTCELL_ALL_EXT_CSF_FC_LIN / FC_2ROWS

2.5.1.1. Functional Diagram

Figure 14 : Block Diagram



2.5.1.2. Interface Description

Table 30 : Pin Description

Pin	Type	Voltage Level (V)	Description
Track pins			
vdderight	Input / Output	vdde	IO power node on right side
gndright	Input / Output	0	Core and substrate ground node on right side
gndleft	Input / Output	0	Core and substrate ground node on left side

2.5.1.3. Cell Information

Table 31 : Cell Information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25˚C (vdderight node)	-	-	< 150	pA
		Fast Process, Max voltage, 125˚C (vdderight node)	-	-	< 150	

2.5.1.4. Functional Description

The FILLCUTCELL_ALL_EXT_CSF_FC_LIN / FC_2ROWS cell is designed to cut the following nodes in the IO ring:

- vdde
- gnde

- vdd
- gnd (through B2B diodes for ESD continuity)
- ASRCN<0:6> and ASRCP<0:6>
- REFIOA
- REFIOB

2.5.2 FILLCUTCELL_GNDE_EXT_CSF_FC_LIN / CL_LIN / FC_2ROWS

2.5.2.1. Functional Description

The FILLCUT_GNDE_EXT_CSF_FC / CL_LIN / FC_2ROWS filler is designed to cut the gnde node in the IO ring

2.5.3 FILLCUTCELL_REFASRC_EXT_CSF_FC_LIN / CL_LIN / FC_2ROWS

2.5.3.1. Functional Description

The FILLCUT_REFASRC_EXT_CSF_FC / CL_LIN / FC_2ROWS filler is designed to cut ASRCN<0:6>, ASRCP<0:6>, REFIOA and REFIOB signal rails in the IO ring.

2.5.4 FILLCUTCELL_VDDE_GNDE_EXT_CSF_FC_LIN / CL_LIN / FC_2ROWS

2.5.4.1. Functional Description

The FILLCUT_VDDE_GNDE_EXT_CSF_FC / CL_LIN / FC_2ROWS filler is designed to cut vdde and gnde nodes in the IO ring.

2.5.5 FILLCUTCELL_VDDE_EXT_CSF_FC_LIN / CL_LIN / FC_2ROWS

2.5.5.1. Functional Description

The FILLCUT_VDDE_EXT_CSF_FC / CL_LIN / FC_2ROWS filler is designed to cut vdde node in the IO ring.

2.5.6 FILLCUTCELL_VDD_EXT_CSF_FC_LIN / CL_LIN / FC_2ROWS

2.5.6.1. Functional Description

The FILLCUT_VDD_EXT_CSF_FC / CL_LIN / FC_2ROWS filler is designed to cut vdd node in the IO ring.

3.Electrical Specifications

3.1 ESD and Latch-up Characteristics

Table 32 : ESD and Latch-up Characteristics

Symbol	Parameter	Condition	Target	Unit
V_{ESD}	Electrostatic discharge voltage	Human Body Model (HBM) [1]	2000	V
		Machine Model (MM) [1]	100	V
		Charge Device Model (CDM) [1]	500V JEDEC	V
$I_{latch-up}$	Injection current	Maximum operating junction temperature 125°C [2]	100	mA
	Over-voltage stress		1.5* vdde	V

[1] ESD qualification: According to electrostatic discharge sensitivity measurement
[2] Latch-up qualification: According to latch-up sensitivity measurement.

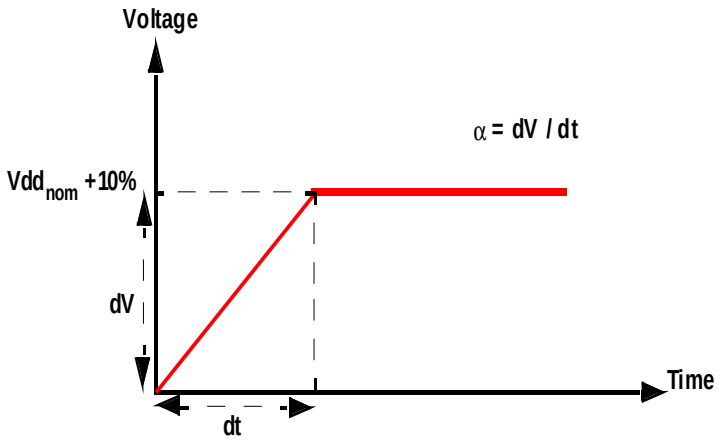
The level of CDM current seen at a given pre-charge voltage varies significantly with the chip size and package type. For instance, larger dies/packages generates higher CDM current.

However, this package size dependence has been considered during IO qualification, so that the above CDM commitment remains valid for any die/package size (even for large die/package sizes of hundreds of mm^2).

3.2 ESD Clamps power-up sensitivity

For correct power-up sequence without parasitic clamp switch-on, it is necessary to limit the power rise time as per next table.

Figure 15 : ESD Clamp Power-up Sensitivity



Power Ramp-Up should be equal or slower than 0.5V/us.

4. Usage Guidelines

4.1 Design Requirements

The C28SOI_IO_EXT_CSF_BASIC_EG library supports the construction of an IO ring in single row or double rows configuration.

4.2 Physical implementation

4.2.1 General placement rules

All cells in this library have their origin at (0, 0) and the ‘pr boundary’ abutted to the origin axes. The strategy to build the IO pad ring or the IO cluster is to abut laterally ‘pr boundary’ layers.

	*The rails of the IO pad ring should not be modified. Only the appropriate filler cut cells supplied within the library should be used. Non-compliance of this constraint disengages the responsibility of the IO supplier and prevents final implementation for full solution / services and support that could be provided for this deliverable.*

4.2.2 Filler cells placement rules

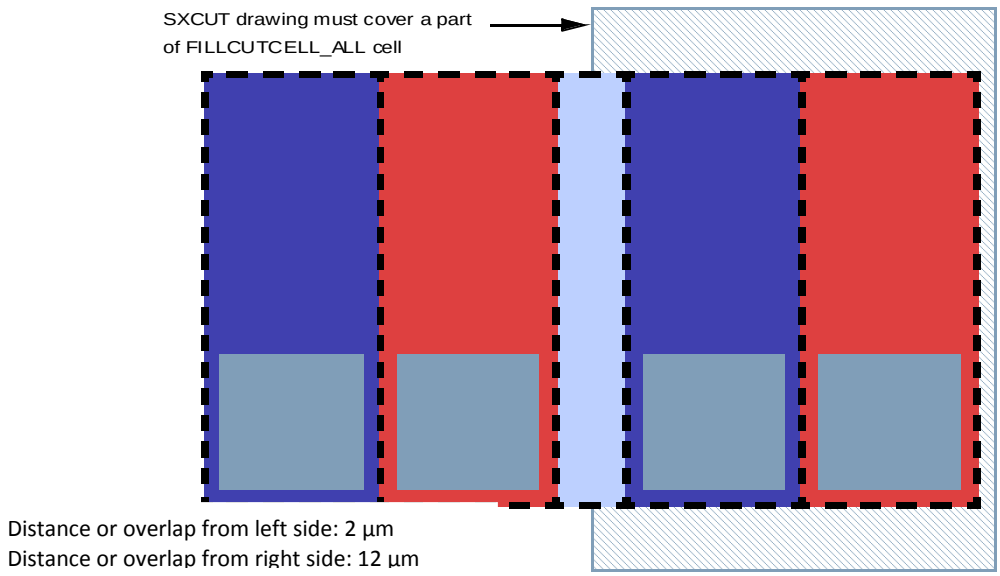
Following rule should be strictly followed when constructing a pad ring.

	*All spaces between IOs should be filled by the larger filler cells available or if needed, FILLCELL_REFASRC_EXT_CSF_**, FILLCELL_VDDE_GNDE_EXT_CSF_** cells.* *FILLCELL_1GRID_EXT_CSF_** and FILLCELL_1UM_EXT_CSF_** cells must not be used to fill in gaps larger than 5 µm.*

4.2.3 FILLCUTCELL_ALL usage

When using FILLCUTCELL_ALL_EXT_CSF_FC_LIN cell, please consider that the substrate node on the right side (gndright) is “virtually” different from the substrate node on the left side (gndleft). Therefore, one of the substrate polarization must be isolated using the marker layer, SXCUT drawing. *Figure 16: Using SXCUT Drawing with FILLCUTCELL_ALL_EXT_CSF_FC_LIN Cell* shows the way to use this layer.

Figure 16 : Using SXCUT Drawing with FILLCUTCELL_ALL_EXT_CSF_FC_LIN Cell



4.2.4 Guidelines for 2ROWS sections construction

4.2.4.1. Generalities

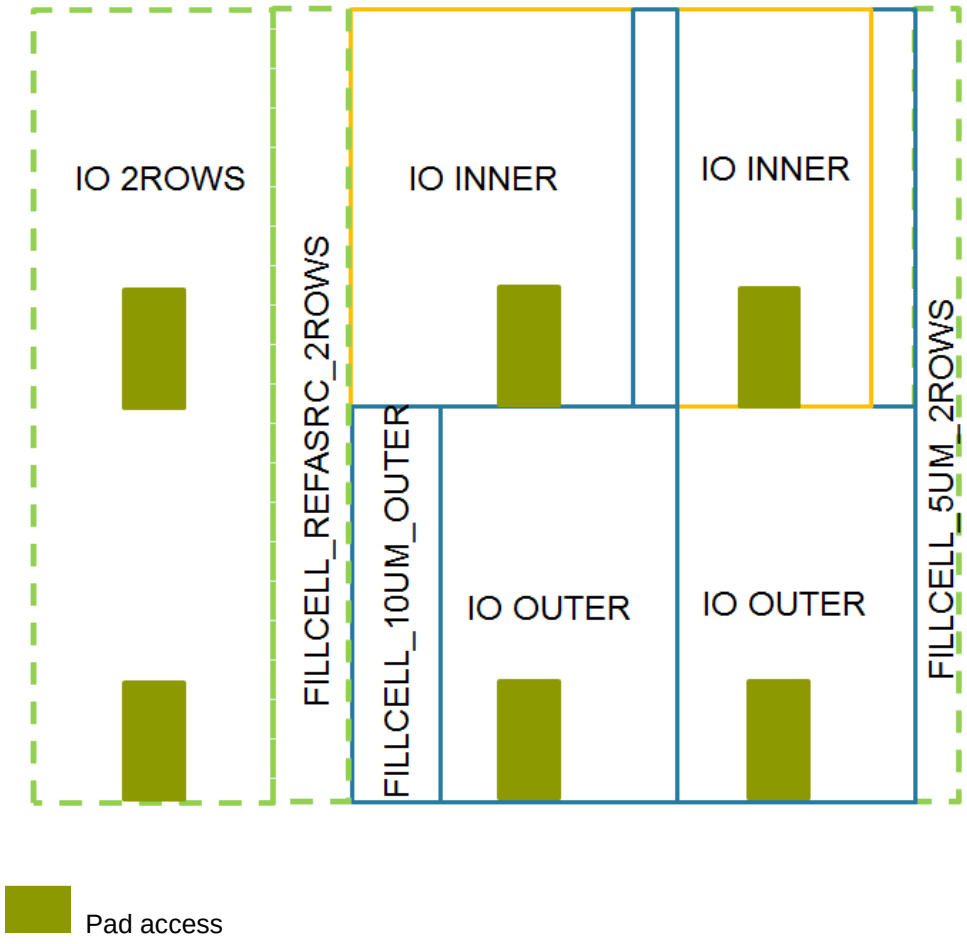
The double row IO ring is built by using 2ROWS, OUTER and INNER IOs.

- OUTER cells are filling in one IO slot and these cells are ‘L-shape’ to allow signal routing from IO cell to core.
- INNER IO is the same as a linear one and it is used only in the inner row.
- 2ROWS cells fill both inner and outer rows.

To differentiate IO cells dedicated for 2ROWS usage from linear ones, the following nomenclature is used

- **_INNER**: for inner row IO cells
- **_OUTER:** for outer row IO cells
- **_2ROWS:** for IO with inner and outer pads in the same frame

Figure 17 : Example of macro assembly of IO_INNER, IO_OUTER and IO_2ROWS in 2ROWS configuration

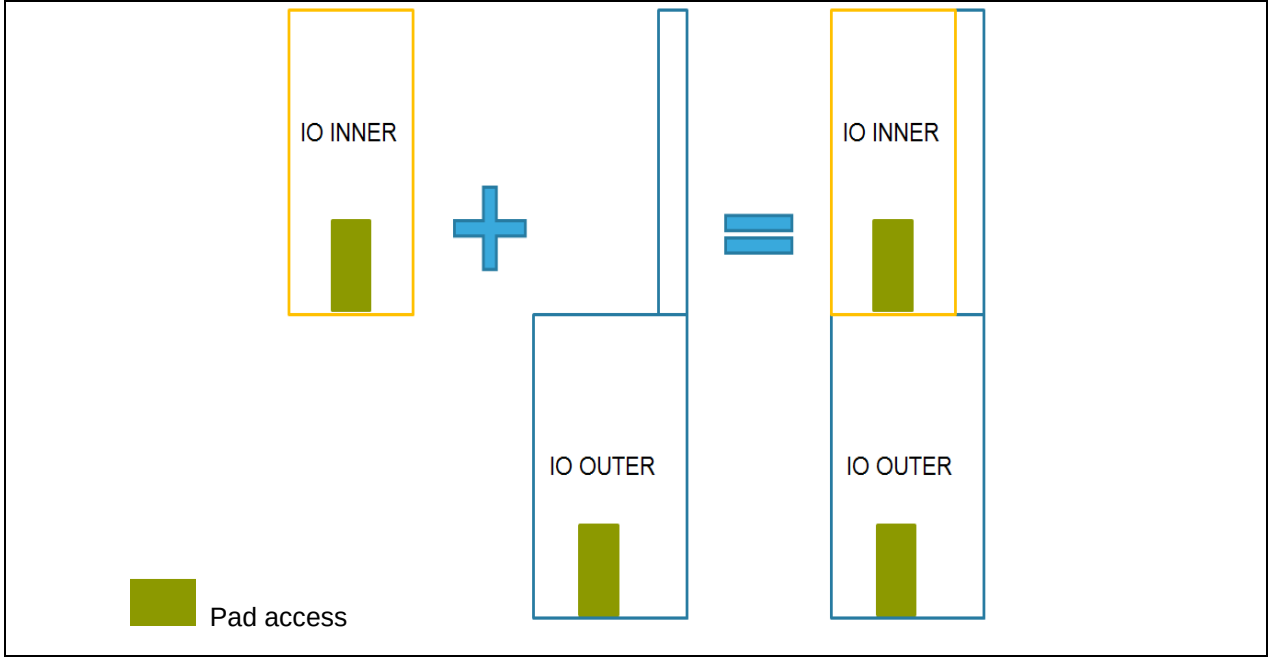


4.2.4.2. Assembly of INNER and OUTER IOs

Three different configurations can occur when abutting INNER and OUTER IO cells.

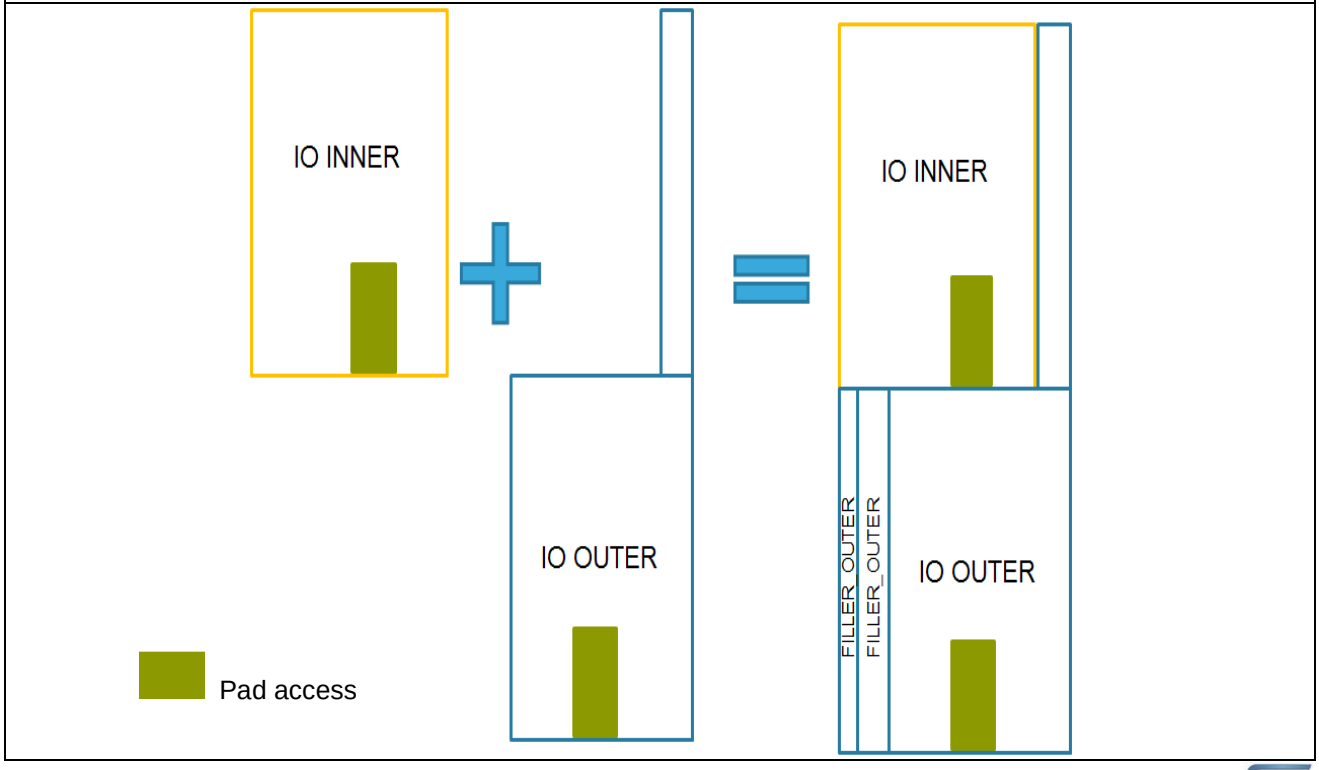
- **Case 1:** Inner IO is aligned on term of width to the outer one. In this case as shown in the figure below no filler is need to abut these two cells.

Figure 18 : Assembly of IO_INNER and IO_OUTER having aligned width



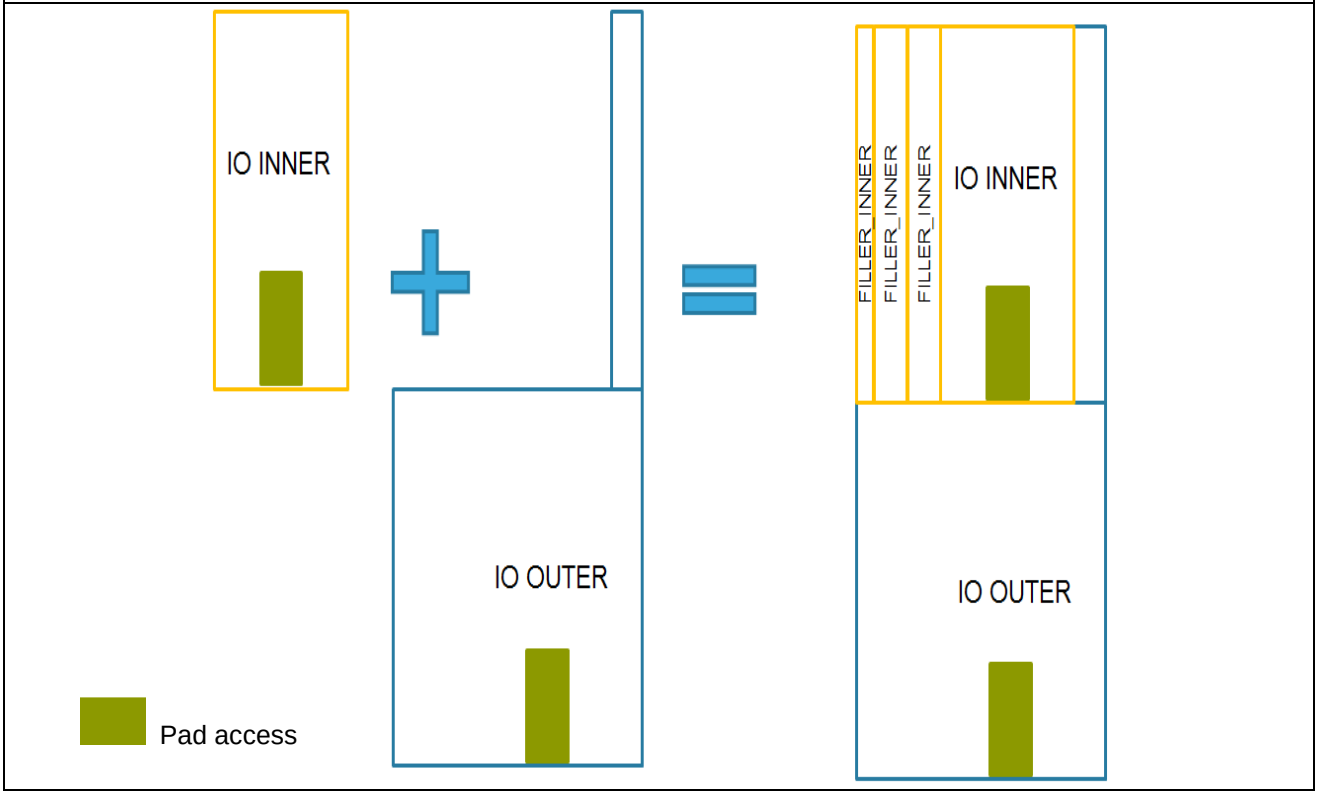
- **Case 2:** Inner IO is larger than the outer one to be placed with. In this case OUTER fillers are needed to fill in the free space in the outer row

Figure 19 : Assembly of an IO_INNER larger than the IO_OUTER



- **Case 3:** Outer IO is larger than the INNER one to be placed with. In this case INNER fillers are needed to fill in the free space in the inner row

Figure 20 : Assembly of an IO_OUTER larger than the IO_INNER



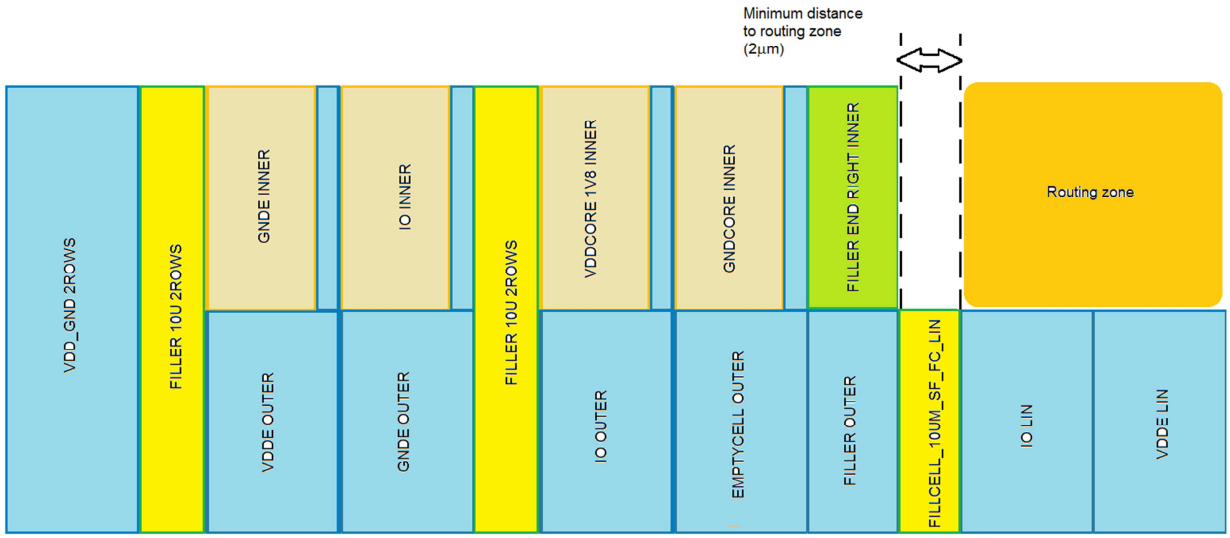
	Only these three placement configurations are allowed to abut INNER and OUTER cells

	For OUTER and INNER FILLERs placement same fillers placement rules described in the previous chapter have to be respected

4.2.5 Guidelines for switching between single and 2ROWS configuration

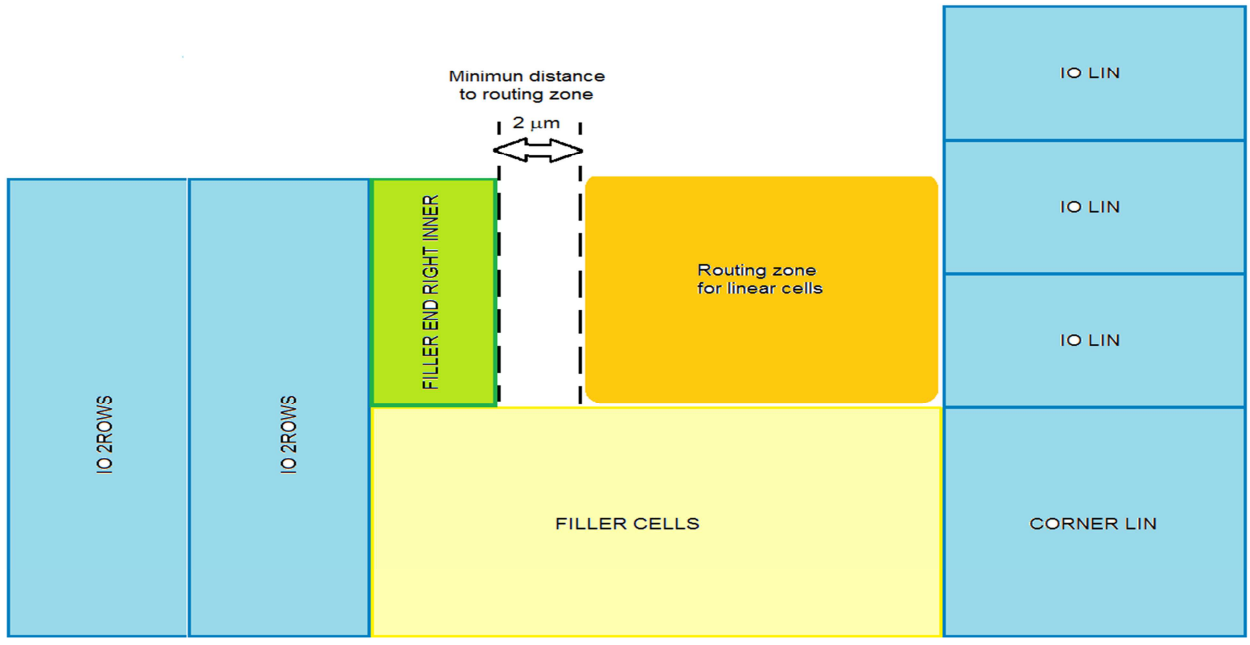
In case of switching between single and double row configuration, a minimum distance of 2 µm must be maintained between FILLCELL_END_*_FC_LIN_INNER and the routing zone of LIN IO ring.

Figure 21 : Example of switching from LIN to 2ROWS configuration



In case of starting a 2ROWS configuration ring after a linear corner, a minimum distance must be maintained in order to route the linear IOs.

Figure 22 : Example of switching from LIN to 2ROWS configuration near a linear corner

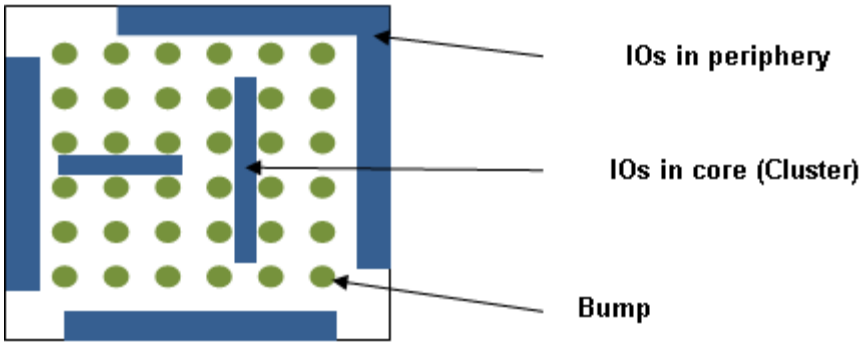


4.2.6 Flip-chip Architecture

4.2.6.1. Principles of Flip-chip Architecture

The use of a flip-chip package allows IOs placement not only in the periphery, but also in the core.

Figure 23 : Flip-Chip Possibilities



4.2.6.2. Peripheral Flip-chip

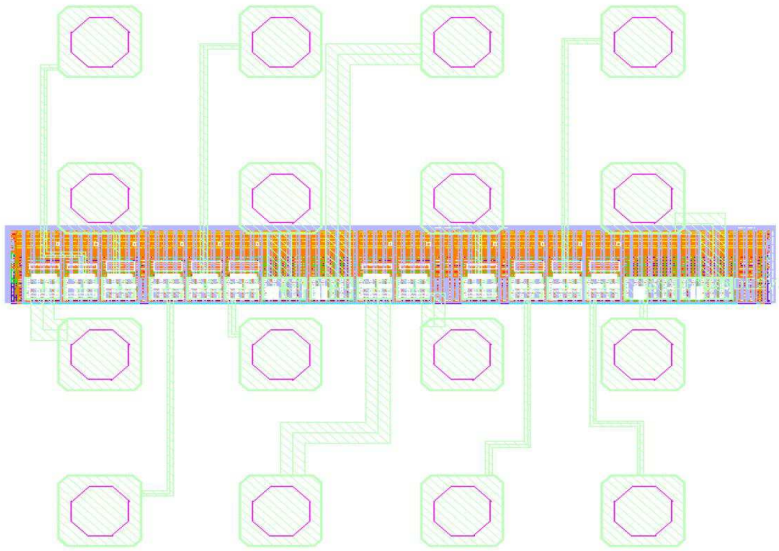
Peripheral flip-chip architecture is quite similar to a wirebond pad. IOs can be put in an L-shaped ring or in a line on the sides of the chip. IO pins are redistributed to the bump by Alucap. The characteristics of the developed solution are:

- Flexible IO cell versus bump placement.
- Fixed IO height.
- Flexible IO width (multiple of routing grid).

4.2.6.3. Flip-chip Cluster

- In the core, IOs are arranged in a line. A linear group of several IOs is named as Cluster (CL)
- IO pins are redistributed to the bump by Alucap.
- A cluster can be integrated everywhere in the chip. However, as it contains Alucap pins, it must be placed between Alucap bump rows (or columns) to avoid shorts.

Figure 24 : Cluster Macro Overview



- Note: The cluster cells ensure latch-up free configuration when placed in the core. It also provides a core power grid continuity in the 2 axis

4.3 Information on Power Cells

4.3.1 ESD Protection Nomenclature

For a better understanding of the ESD placement rules, the following definition of ESD protection devices is proposed:

- CVDDE refers to the full VDDE/GNDE ESD clamp. It is embedded in VDDE_EXT_CSF_**, GNDE_EXT_CSF_** and **CORNERCELL_EXT_CSF_** cells.
- CVDD refers to the VDD/GND ESD clamp. It is embedded in VDD_EXT_CSF_**, GND_EXT_CSF_** and each time in VDD_GND/GND_VDD_EXT_CSF_FC_2ROWS supply cells.
-

4.3.2 IO Supply Placement Rules (VDDE/GNDE)

4.3.2.1. IO Supply Number

The number of IO supplies required in an IO ring is defined by three main parameters:

- Current capability of the cell
- Minimum number of VDDE/GNDE ESD clamps
- Simultaneous switching noise concept: limitation of the power/ground bounce, in order to maintain correct signal integrity.
-

	***Number of vdde / gnde supplies:*** *The number of IO supplies required for each type of IO is described in the User Manual of each IO library. It includes two constraints, the current capability of the cell and the simultaneous switching noise concerns.*

	***CVDDE.r1:*** *For any IO ring section delimited by vdde and/or gnde cut, at least two CVDDE clamps are required.*

4.3.2.2. IO Supply Distance

	***CVDDE.r2:*** *The maximum distance between two CVDDE ESD clamps is 1 mm.*

4.3.3 Core Supply Placement Rules (VDD/GND)

4.3.3.1. Core Supply Number

The number of core supplies required in an IO ring is defined by the current capability of the cell.

	***Number of vdd / gnd supplies:*** *The number of core supplies required to supply the core is under chip designer responsibility.*

Note: Using a homogenous power grid and supply distribution always has a positive impact in term of voltage drop.

On each vdd section of the IO ring, a VDD_EXT_CSF_** and a GND_EXT_CSF_** or a VDD_GND/GND_VDD_EXT_CSF_FC_2ROWS power cell is mandatory to supply the vdd and gnd nodes. This cell embeds its own vdd / gnd ESD clamp (CVDD).

	***CVDD.r1:*** *vdd and gnd rails must always be polarized by appropriate supply cells. For any IO ring section delimited by vdd and/or gnd cut, at least two CVDD clamps are required.*

	*Vdd and gnd core nodes supplied by core supply BUMP can be protected also by the 1V0 CORECLAMP provided by the C28SOI_IO_EXT_ALLF_CORESUPPLY_EG library. You can refer to C28SOI_IO_EXT_ALLF_CORESUPPLY_EG library UM for usage guidelines.*

	*If vdd and gnd core nodes are protected only through 1V0 CORE CLAMP, provided by the C28SOI_IO_EXT_ALLF_CORESUPPLY_EG library, a support has to be requested.*

4.3.3.2. Core Supply Distance

To prevent any dangerous voltage difference between vdd and gnd rails during an ESD event, the following rule must be respected.

	***CVDD.r2:*** *Maximum distance between two 1V0 ESD clamps (CVDD) is 640 µm.*

4.3.4 Fillercut Cells

4.3.4.1. Cutting Pad Ring Rails

Cutting vdde and/or gnde rails

Following rule has to be respected when cutting vdde and/or gnde rails to ensure the performance of ESD network.

	***CVDDE.r3:*** *In case of cut VDDE and/or GNDE (FILLCUTCELL_ALL_**, FILLCUT_GNDE_**, FILLCELL_END_**, FILLCUT_VDDE_** and FILLCUT_VDDE_GNDE_** cells), IO near the cuts must be at less than 250 µm distance from CVDDE ESD clamp.*

	***CVDDE.r4:*** *When vdde node is cut: if the two adjacent IOring sections are not powered at the same time (one side of the cut is vdde ON and the other one is vdde OFF), ASRC and REF nodes have to be cut by using FILLCUTCELL_REFASRC_EXT_CSF * filler.*

Cutting gnd rail (FILLCUTCELL_ALL_ and FILLCELL_END_** cells)**

Gnd node is the global ESD reference node for ESD protection. As a consequence, this node should be continuous through the entire chip. When gnd node is cut, this continuity is ensured by the use of a back-to-back diode that is present inside FILLCUTCELL_ALL** cell between left and right track pins. Please refer to *Section 2.5.1 FILLCUTCELL_ALL_EXT_CSF_FC_LIN / FC_2ROWS* for details.

Due to the presence of these diodes on the global ESD reference node, a restriction of three 'gnd' cuts is mandatory on a chip, to avoid an overvoltage of the stressed pad during an ESD event. This is specified in the following rule.

	***GND.r1:*** *A maximum of three cuts of 'gnd' node (FILLCUTCELL_ALL_** and FILLCELL_END_** cells) are allowed per chip. Between two different IOs sections, only one back-to-back diode has to be present between two gnd nodes.*

	*If cut of gnd node is needed for more than three times in a chip, please refer to the C28SOI_IO_EXT_ALLF_ESDHUB_EG library user's manual*

Cutting vdd rail

	***VDD.r1:*** *Maximum distance between a clamp and a cut (FILLCUTCELL_ALL_**, FILLCELL_END_** and FILLCUT_VDD_** cells) is 400 µm.*

Summary

Table 33 : Cutting Rails

Cells	Cut vdde Rails	Cut gnde Rails	Cut vdd Rails	Cut gnd Rails	Rules
FILLCUTCELL_ALL_EXT_CSF_**	X	X	X	X	CVDDE.r1, CVDDE.r2, CVDDE.r3, CVDDE.r4, CVDD.r1, CVDD.r2, GND.r1, VDD.r1
FILLCUT_GNDE_EXT_CSF_*	-	X	-	-	CVDDE.r1, CVDDE.r2, CVDDE.r3
FILLCUT_VDDE_EXT_CSF_*	X	-	-	-	CVDDE.r1, CVDDE.r2, CVDDE.r3, CVDDE.r4
FILLCUT_VDDE_GNDE_EXT_CSF_*	X	X	-	-	CVDDE.r1, CVDDE.r2, CVDDE.r3, CVDDE.r4
FILLCUT_VDD_EXT_CSF_*	-	-	X	-	CVDD.r1, CVDD.r2, VDD.r1
FILLCELL_END_LEFT/RIGHT_EXT_CSF_*	X	X	X	X	CVDDE.r1, CVDDE.r2, CVDDE.r3, CVDD.r1, CVDD.r2, GND.r1, VDD.r1

‘X’ indicates the cut rails of the cells.
‘-’ indicates the non-cut rails of the cells.

4.3.5 WIRECELL Placement Rules

	*To connect an input buffer or a transistor gate to IO pad It is mandatory to use RES pin (series resistor pin on IO signal) and a CDM secondary protection*

5.Contact Information

ST users, login to **HELPDESK**. (http://col2.cro.st.com/helpdesk) for submitting queries or support requests.

Non-ST users, contact Customer Support personnel.

Appendix A: Cell Naming Convention

Table 34 : Naming Convention for Top Cells

Segment Name	Description
Cell type	Refers to the type of cell. It can have either of the following values: - VDDE/GNDE: IO power supply cell - FILLCELL: filler cells - FILLCUTCELL: fillercut cell
1st suffix	Refers to the cell offer. It can have either of the following values: - <none> - EXT: extended CDM specification offer
2nd suffix	Refers to the type of frame. It can have any of the following values: - CSF: refers to compatible standard frame
3rd suffix	Refers to the layout view of the cell. It can have any of the following values: - FC: represents flip-chip configuration - CL: represents cluster configuration
4th suffix	Refers to the type of IO ring configuration: - LIN: represents single row (linear) configuration - 2ROWS: represents double row configuration

Table 35 : Example: Segments in Name of VDDE_EXT_CSF_FC_LIN Cell

Segment Name	Segment Value	Description
Cell type	VDDE	VDDE power supply cell
1st suffix	EXT	Extended CDM specification
2nd suffix	CSF	Uses compatible standard frame
3rd suffix	FC	Flip-chip configuration
4th suffix	LIN	Linear layout configuration

Appendix B: Document Revision History

Table 36 : Revision History

Date	Document Version	Comments
11-February-2016	1.4	• Reference Library added • Alignment to ESD/LU guidelines • Table 2 “Acronyms/Abbreviations” added • Leakage current for Wirecells updated • Functional diagrams of FILLER_END and REFASRC fillers updated
09-July-2015	1.3	• “ Pin description” tables improved • “ Cell Information“ tables updated • DC current for WIRECELL cells corrected
04-June-2015	1.2	• DC and RMS currents updated for supply cells
06-November-2014	1.1	• DC current Pad to core updated for GND and VDD FC LIN cells • Rails to core resistance added for FILLCELL_VDDE_GNDE_* cells
22-September-2014	1.0	• First release

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