

# Analog Flow 28 UTBB-FDSOI Process Design Kit

## Module 0- PDK Presentation

**FD-SOI**



life.augmented

Company Confidential

CMOS & Derivative PDK



*At the end of this course, you will be able to*

- **Recall** the available Design Kit and choose among the options
- **Identify** where and how to get a Design Kit related information and support
- **Configure** the CAD tools
- **Run all the steps of the analog flow**



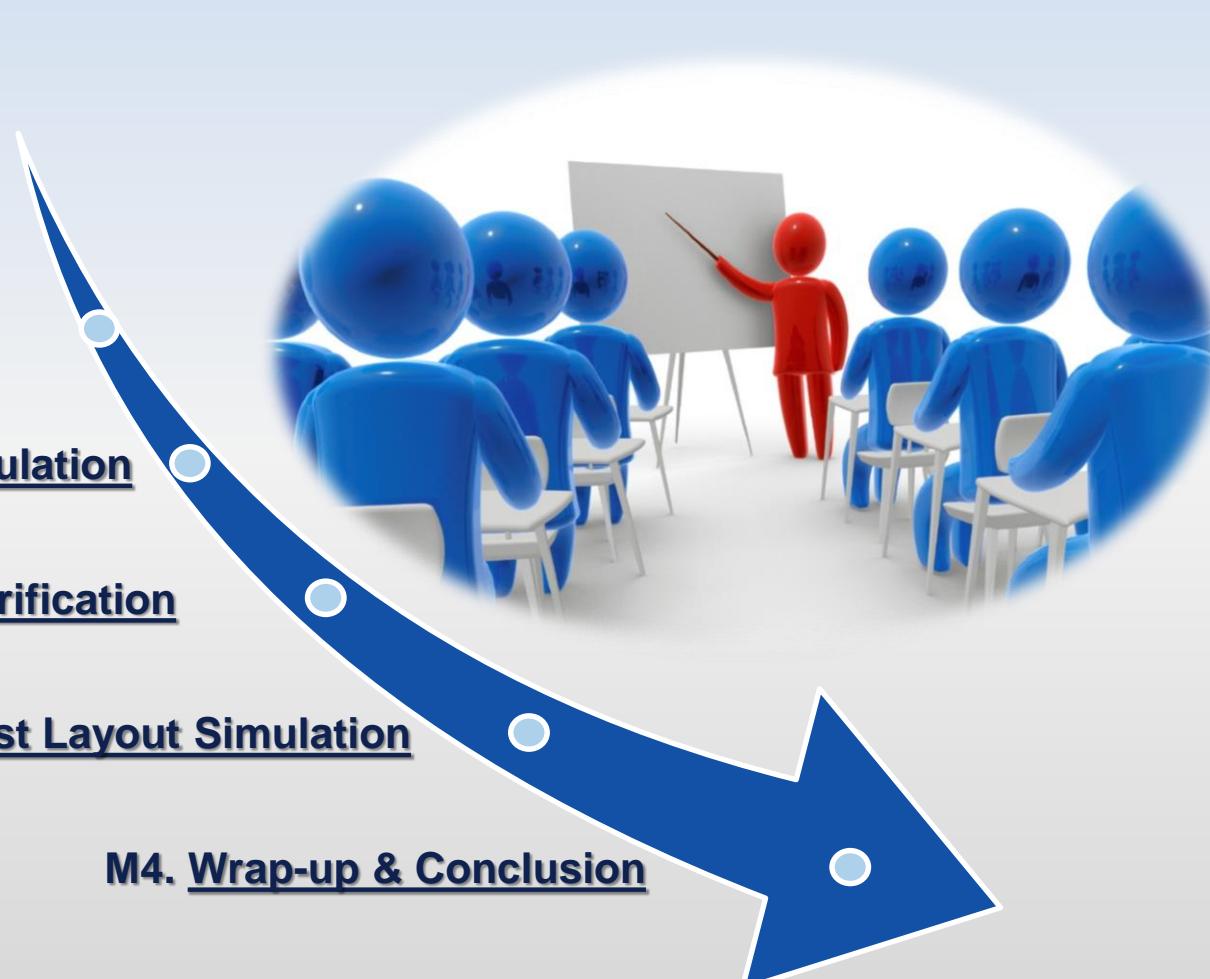
**M0. Design Kit Overview**

**M1. Schematic and Simulation**

**M2. Layout Verification**

**M3. Post Layout Simulation**

**M4. Wrap-up & Conclusion**

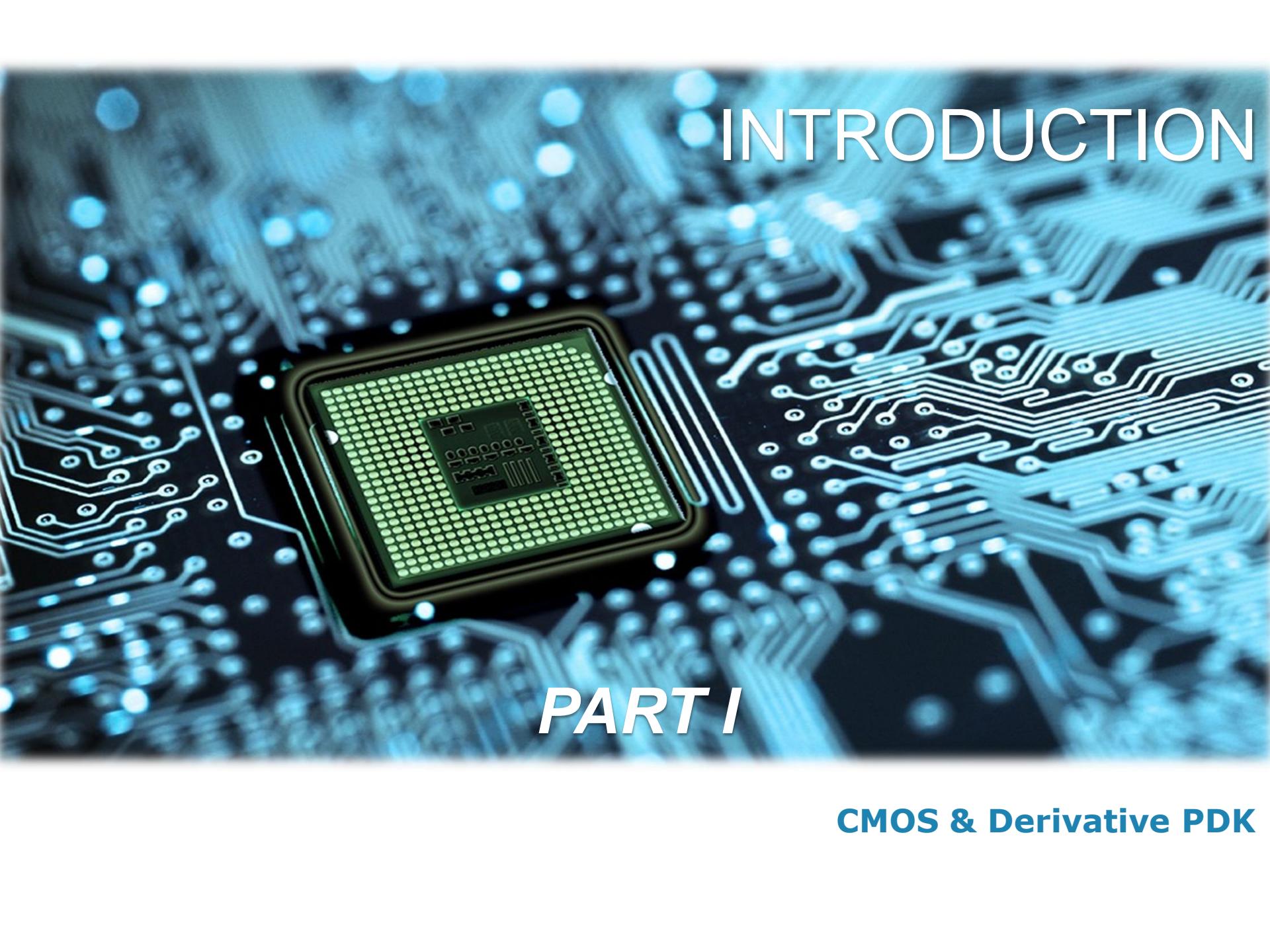




- Recall the available Design Kit and choose among the options
- Identify where and how to get a Design Kit related information and support
- Identify the supported flow

# AGENDA





# INTRODUCTION

## PART I

**CMOS & Derivative PDK**

## Introduction

Technology Overview



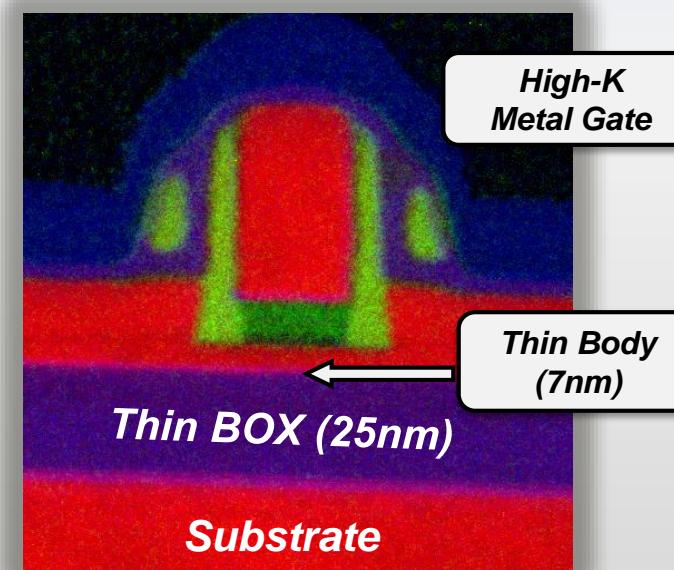
Design-Kit Contents

Roadmap

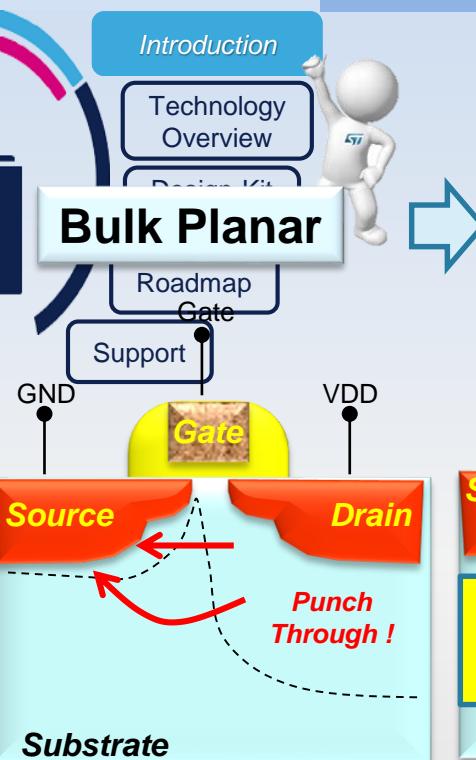
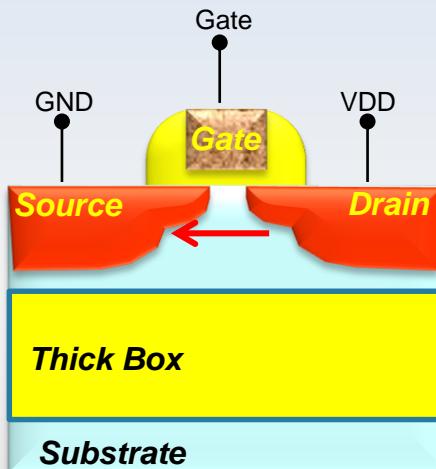
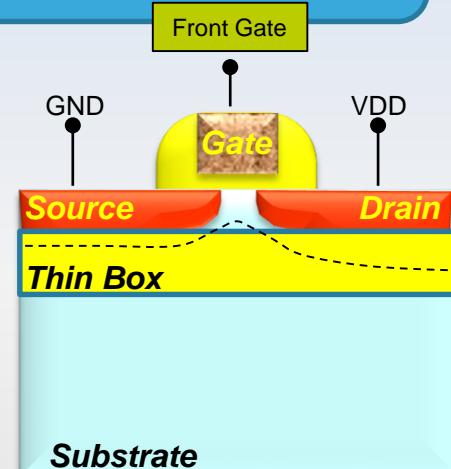
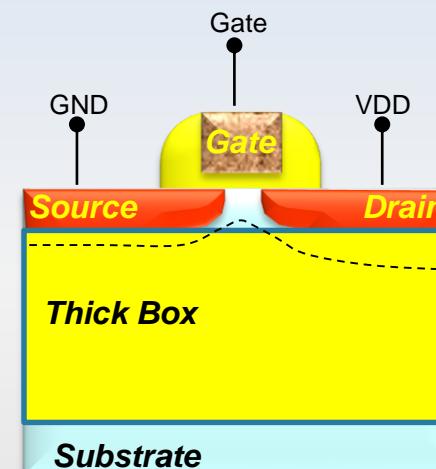
Support

- 28FDSOI (Fully Depleted Silicon on Insulator) is a new technology, targeted as Low Power to serve battery operated and wireless applications, relying on an ultra-thin layer of silicon over a Buried Oxide (BOX) acting as an insulator.
  - The top silicon layer is fully depleted, which means, it doesn't have any intrinsic charge carriers

- ✓ Ultra Thin Silicon film is 7nm
- ✓ Ultra Thin BOX (25nm) made by oxydation
- ✓ High-k dielectric and Metal Gate electrode ( HKMG )
- ✓ Source and Drain : epitaxy raised.
- ✓ Thin SD silicidation
- ✓ No memory effect compared to partially depleted
- ✓ Undoped channel (Analog, variability)
- ✓ Bulk / SOI co-integration ( hybrid ) : easy



Ultra Thin Body &amp; BOX Fully Depleted SOI transistor

Partially Depleted SOI  
**PDSOI**Extremely Thin SOI  
**ETSOI****Performance summary**

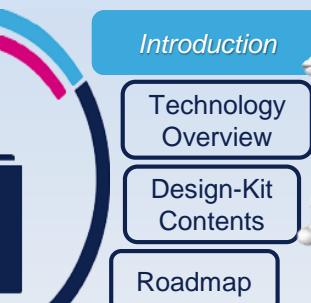
DIBL*	150mV/V
Sub-VT slope	95mV/Dec
History effect	No effect
Self heating	Low
FBB efficiency	25mV/V

\* DIBL: Drain Induced Barrier Lowering

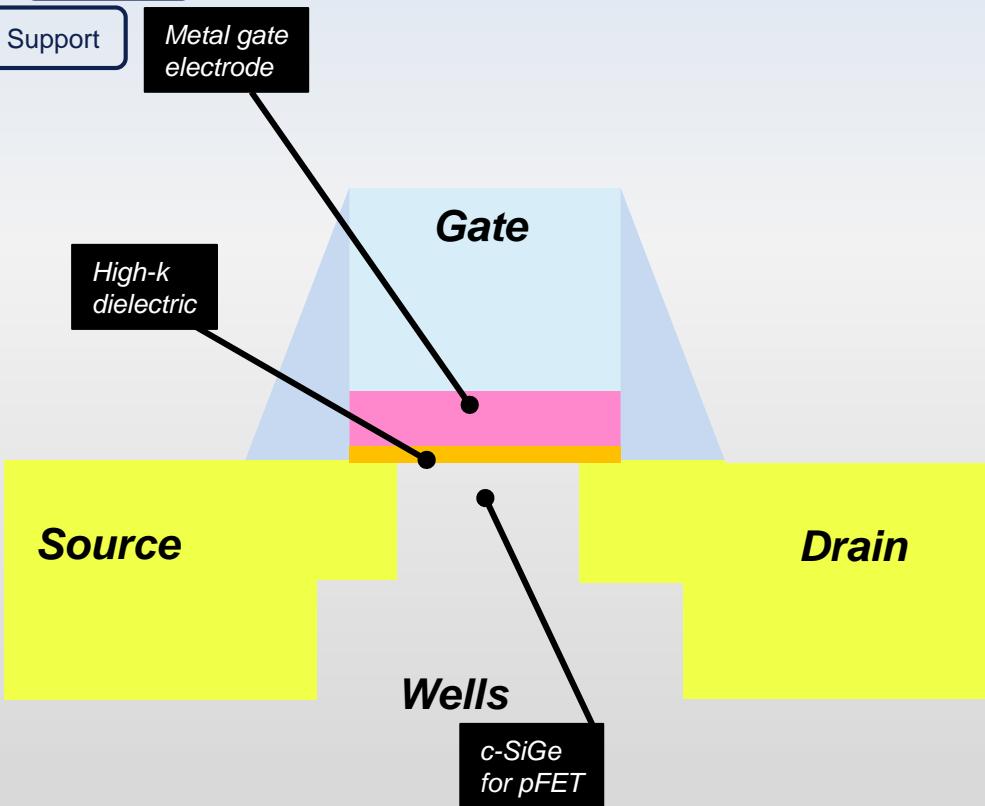
DIBL*	150mV/V
Sub-VT slope	95mV/Dec
History effect	Yes
Self heating	High (fat box)
FBB efficiency	No FBB

DIBL*	95mV/V
Sub-VT slope	78mV/Dec
History effect	No effect
Self heating	High
FBB efficiency	No FBB

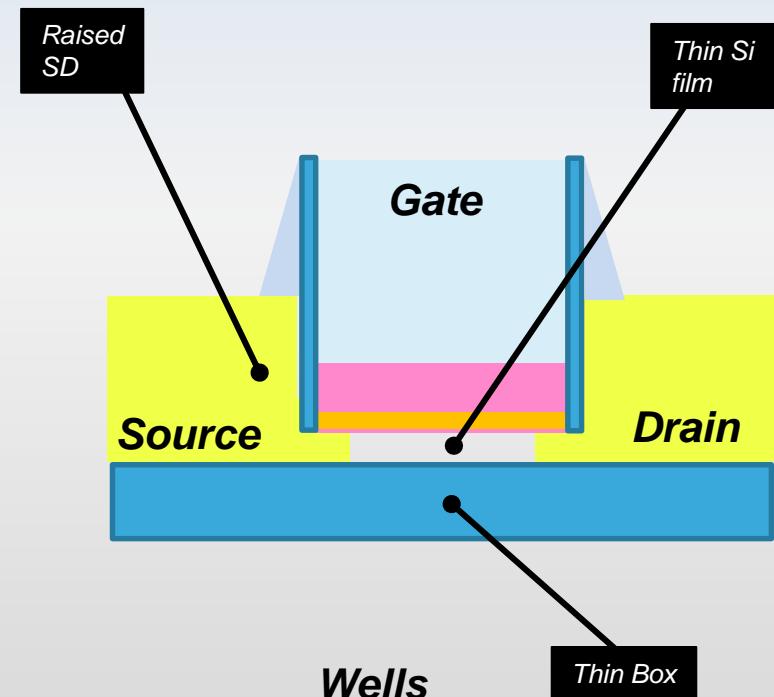
Back Gate	
DIBL*	95mV/V
Sub-VT slope	78mV/Dec
History effect	No effect
Self heating	Low (thin box hybrid zones)
FBB efficiency	80mV/V

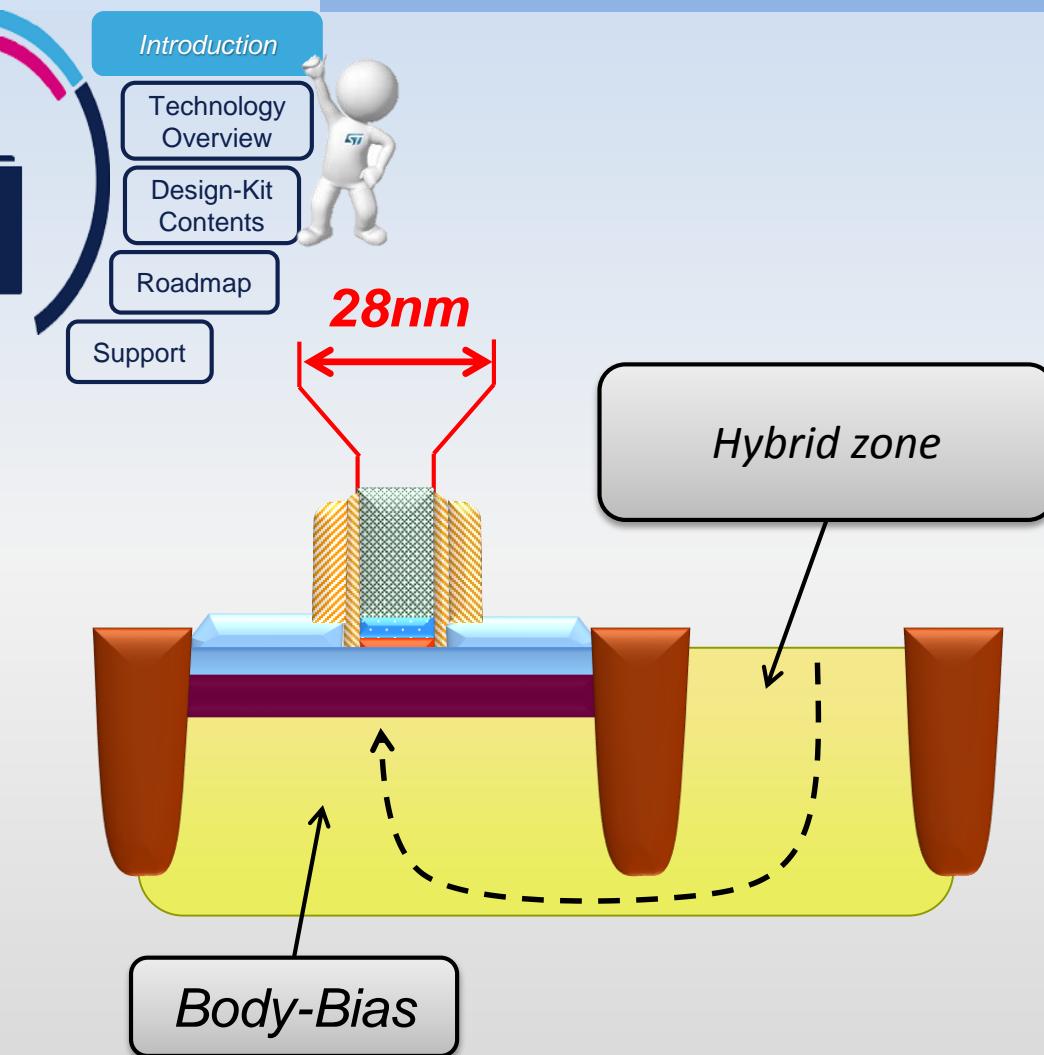


### 28LP Bulk Technology



### 28FDSOI Technology





- **Shorter channel length**
  - 28nm technology !
- **Better electrostatics**
  - Faster operation
  - Low voltage
  - Reduced variability
- **Total dielectric isolation**
  - Latch up immunity
- **Lower leakage current**
  - Less sensitive to temperature

**Introduction**

Technology Overview

Design-Kit Contents

Roadmap

Support

**Faster****Puts more powerful devices in the hands of the end user**

Transistors at max frequencies are up to 30% faster than bulk CMOS, enabling faster processors

**Cooler****End-user devices run cooler and last longer**

Transistors are significantly more power efficient than bulk CMOS devices with lower leakage and much wider range of operation points down to lower voltages

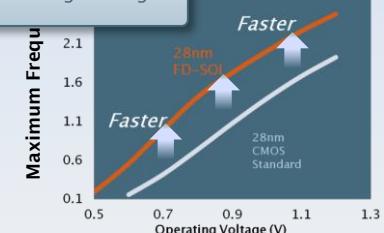
**Simpler****Much simpler manufacturing process**

Extensive use of existing fab infrastructure  
Design porting from bulk is simple and fast

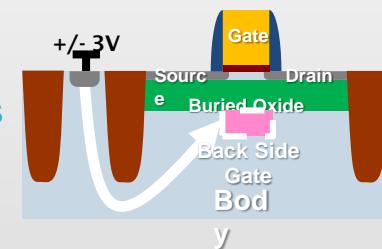


- FD-SOI enables better transistor electrostatics
  - Improving transistor parasitics
  - Improving transistor behavior, especially at low supply
  - Reducing transistor variability sources

>x2 Performance at low voltage  
>35% Performance increase at nominal and high voltage



- FD-SOI enables usage of body bias techniques
  - Transistor is ideally controlled through two independent gates
  - Allowing dynamically modulating transistor threshold voltage





- FD-SOI enables very low voltage operation

- And is extremely fast at low voltage, allowing running with better energy efficiency

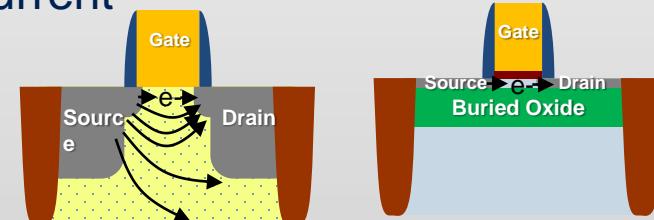
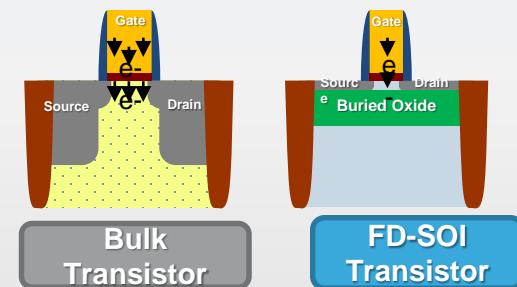
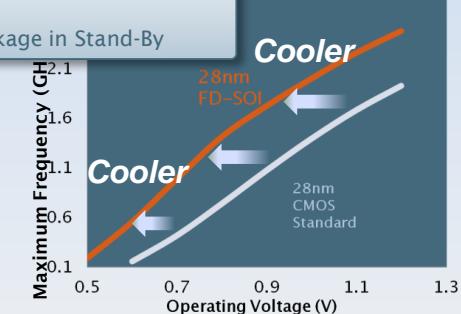
- FD-SOI has lower gate leakage current

- Thicker gate dielectric → reduced gate leakage
  - Ultra low power SRAM memories
  - Leakage current is less sensitive to temperature with FD-SOI

- FD-SOI has lower channel leakage current

- Carriers are efficiently confined from source to drain

~35% Less Power at Highest Performance  
-35% Power Leakage in Stand-By





## 28nm FD-SOI Process versus Bulk 28LP



Interconnect Process

**Same**

Process complexity

**15% fewer steps in FD-SOI**

Device Process

**80% common, 20% specific**

Process development

**Only 20% Front-End steps to develop**

Lead time

**10% Better**

CAPEX

**Same equipment as bulk**

Scalability

**Down to 10nm**

# TECHNOLOGY OVERVIEW

- General Features

**PART II**

**CMOS & Derivative PDK**



Introduction

Technology Overview

Design-Kit Contents

Roadmap

Support

-  • FULLY-DEPLETED SOI devices, with ULTRATHIN BOX and GROUND PLANE
-  • Thick Gate Oxide for IO compatibility
-  • COINTEGRATION with BULK devices.
-  • TRIPLE WELL (Deep N-WELL) allows isolating PWELL from the substrate
-  • SHALLOW TRENCH ISOLATION (STI)
-  • Dual Damascene COPPER interconnects.
-  • Self-aligned SILICIDED DRAIN, SOURCE AND GATE
  - drastically reduces gate and S/D series resistance.

Introduction

Technology Overview

Design-Kit Contents

Roadmap

Support



Device family	Nominal power supply voltage	Maximum power supply voltage
<b>Thin oxide GO1 SG MOS (RVT/LVT)</b>	0.9V (overdrive 1.1V)	1.155V
<b>Thick oxide GO2 MOS (EG)</b>	1.8V	1.98V
<b>Thick oxide GO2 MOS (EGV)</b>	1.5V	1.65V
<b>MOM capacitor (with via)</b>	<ul style="list-style-type: none"> <li>- min pitch finger W=S=0.050um: 1.1V</li> <li>- relaxed finger pitch W=S&gt;=0.060um: 1.8V</li> </ul>	1.155V  1.98V
<b>MOM capacitor (without via)</b>	1.8V	1.98V
<b>OTP drift</b>	6V ( $ V_d - V_s  \leq 6V$ on the drain)	6.6V
<b>MIM capacitor</b>	1.1V	1.155V

# TECHNOLOGY OVERVIEW

- Metal Stack

PART II

CMOS & Derivative PDK



- The naming convention  $xU1x-yU2x-zT8x$  shows three information for each configuration of the stack description:

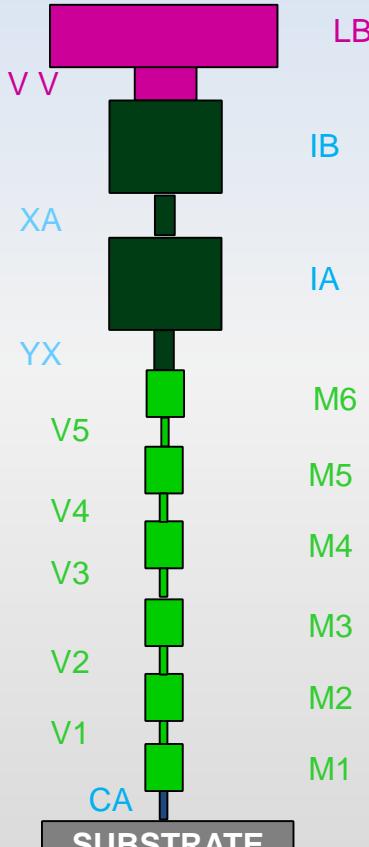
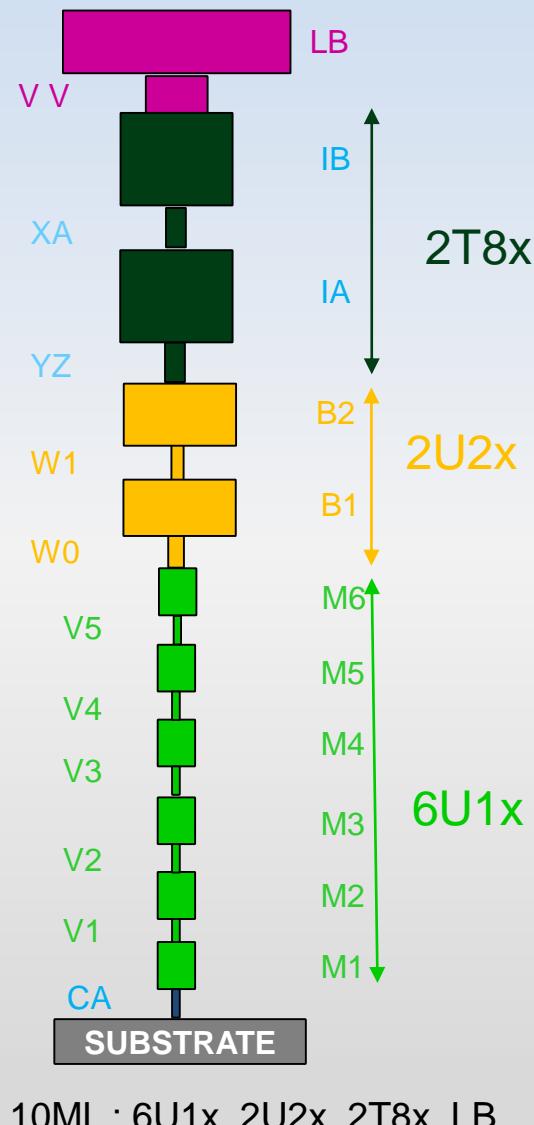
- Number of metal levels in this configuration
- The oxide type
- Metal thickness



- And in the different configurations:

- The dielectric type can be:
  - L for Low-k material
  - U for Ultra low-k dielectric
  - T for TEOS/FTEOS \*
- The metal thickness is represented by the number of 'x'
  - For example: 1x, 1p3x (1.3x), 2x, 8x...

\* TEOS: tetraethylorthosilicate  
FTEOS: fluorinated TEOS

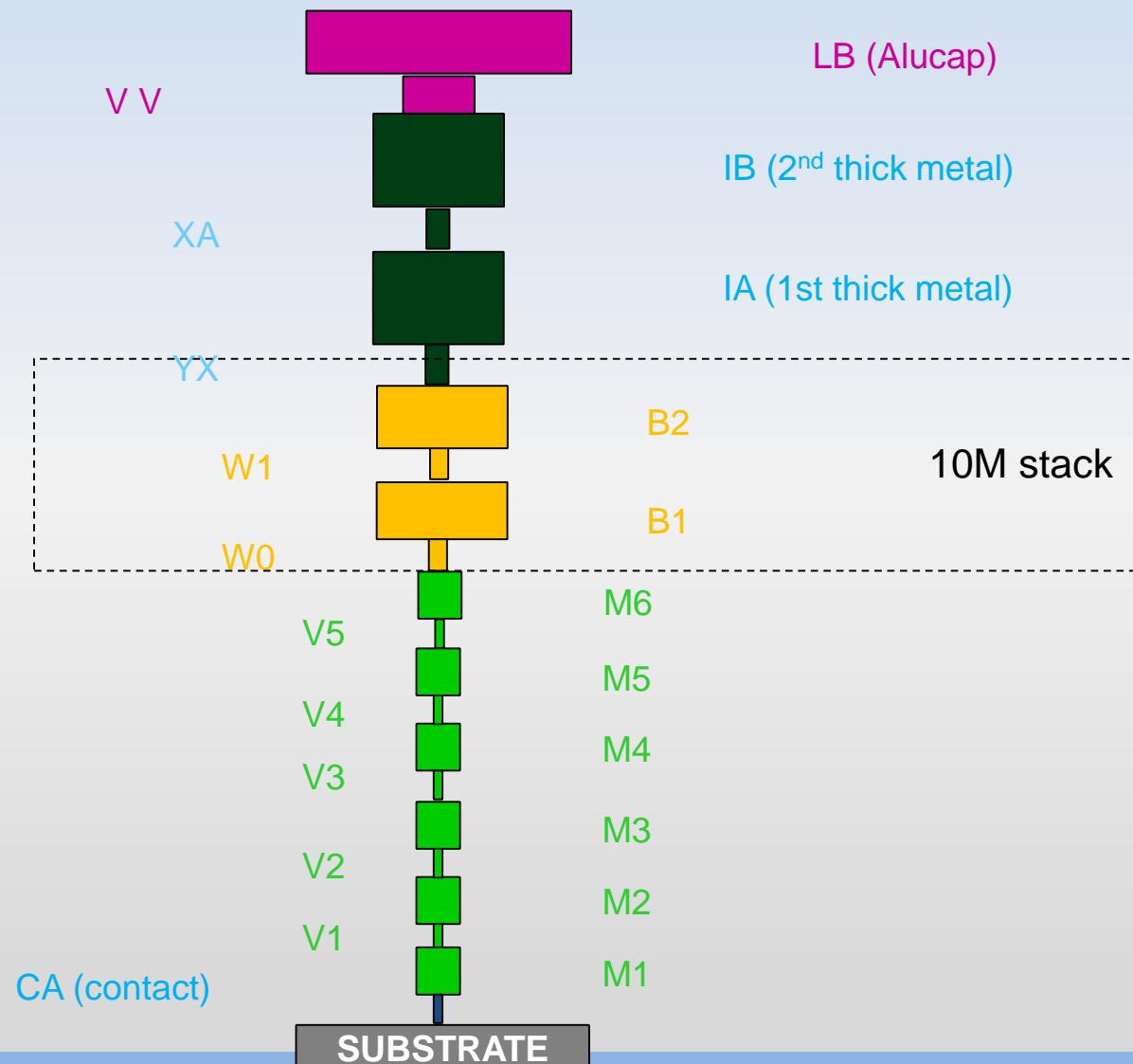


# TECHNOLOGY OVERVIEW

- Layers

PART II

CMOS & Derivative PDK



Introduction

Technology Overview

Design-Kit Contents

Roadmap

Support



## Names of the most used front end layers

cmos28FDSOI layer name	Description
<b>RX</b>	Definition of active area
<b>T3</b>	Used to obtain isolated PW
<b>NW</b>	Definition of N-Well area
<b>LVT</b>	Low-VT devices
<b>RVT</b>	Regular-VT devices
<b>EG</b>	GO <sub>2</sub> medium oxide (28Å)
<b>BP</b>	Definition of P-type implant
<b>PC</b>	Definition of Gate Poly an interconnect Poly
<b>OP</b>	Unsalicided areas
<b>CA</b>	square connection between either RX or PC to M1



names of the most used back end layers, with basic DRM rules:

cmos28FDSOI layer name	Description
<b>Vx</b>	Via between Mx and Mx+1
<b>Mx</b>	Metal levels from 1 to 6 (or 5)
<b>Vxbar</b>	Rectangular via for connecting Mx to Mx+1
<b>VxLGR</b>	Large square via between Mx and Mx+1
<b>W0</b>	Square via for connecting M6 to B1
<b>W1</b>	Square via for connecting B1 to B2
<b>B1</b>	first-level 2x metal line (for a trench in ultralow-k dielectric)
<b>B2</b>	second-level 2x metal line (for a trench in ultralow-k dielectric)
<b>YX</b>	square via for connecting MLAST1X to IA.
<b>YZ</b>	square via for connecting B2 to IA
<b>IA</b>	First level 8x metal line (in oxide)
<b>XA</b>	Square Via between thick IA and IB
<b>IB</b>	Second level 8x metal line (in oxide)
<b>VV</b>	Padopen (square via for connecting the last copper metal to LB)
<b>LB</b>	Alucap

# TECHNOLOGY OVERVIEW

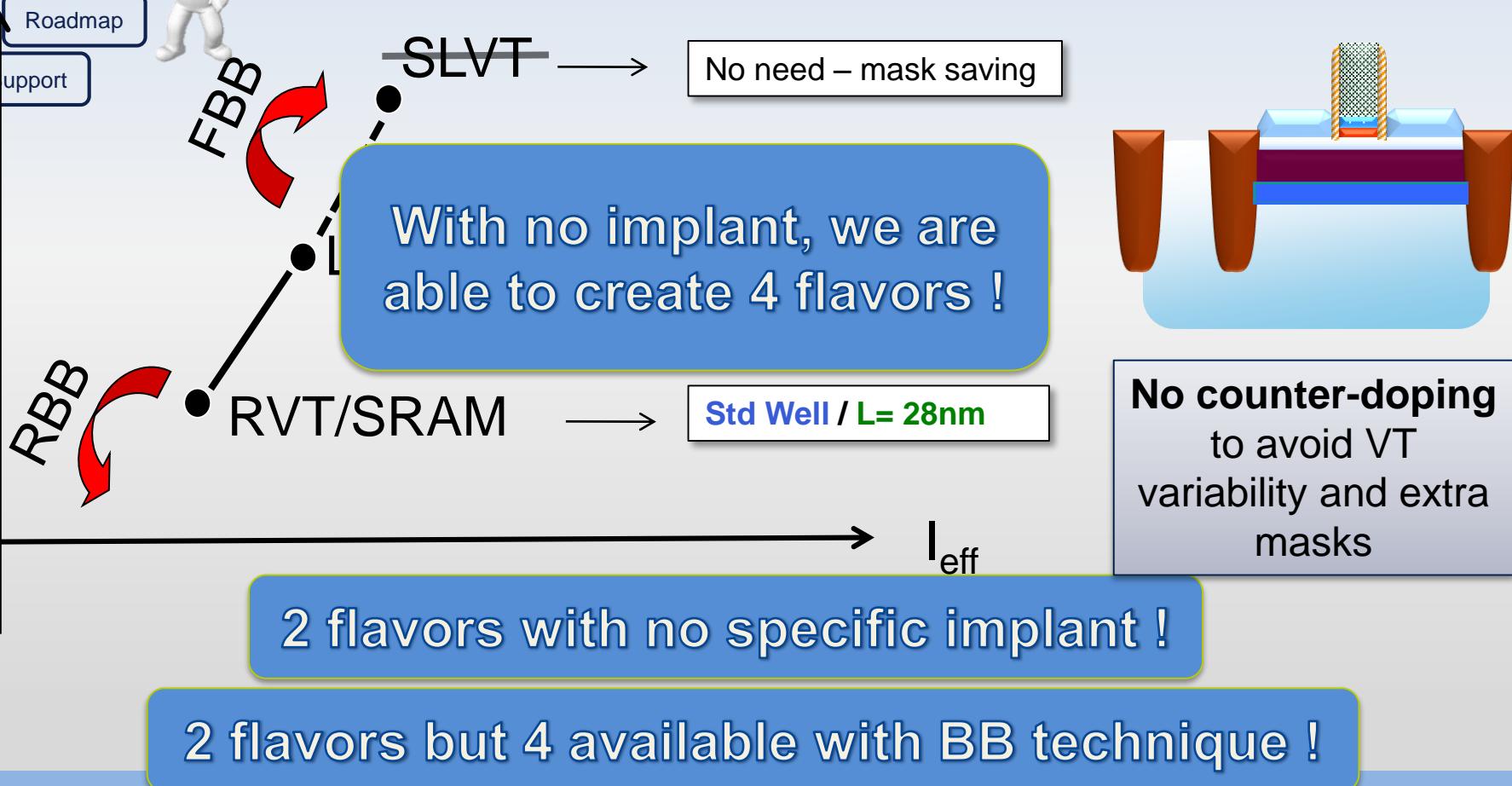
- **28UTBB-FDSOI Strategy:** The VT offer

**PART II**

**CMOS & Derivative PDK**



- 4 sources of V<sub>th</sub> modulation for FDSOI : Gate Oxide, Well type, Poly Biasing, Body Biasing



# TECHNOLOGY OVERVIEW

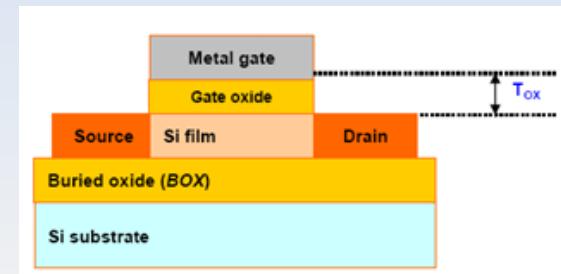
- **28UTBB-FDSOI Strategy:** Gate oxide option

**PART II**

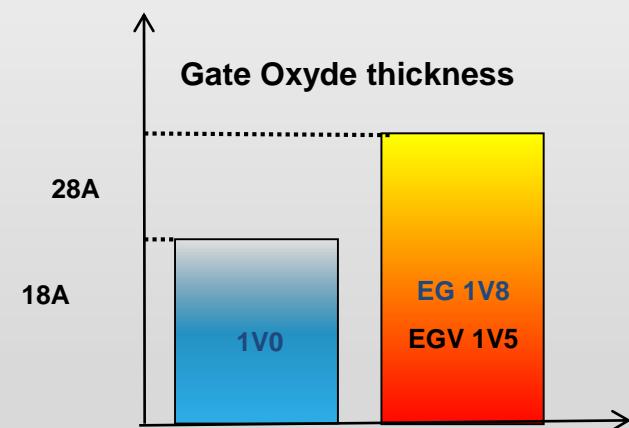
**CMOS & Derivative PDK**



- CMOS28FDSOI is a low power technology process for applications with a single IO oxide + single core oxide double-Vt process.
- It gives access to :
  - 1.0V Low  $V_{TH}$  transistors (LVT)
  - 1.0V Regular  $V_{TH}$  transistors (RVT)
  - 1.5V and 1.8V IO transistors using IO oxide.
  - Low leakage (high density) SRAM using LP core oxide



	<b>Thin</b>	<b>Medium EGV/EG</b>
<b>Thickness</b>	18A	28A
<b>Nominal Voltage</b>	1V0	1V5/1V8



Source: cmos028 FDSOI Design Manual

# TECHNOLOGY OVERVIEW

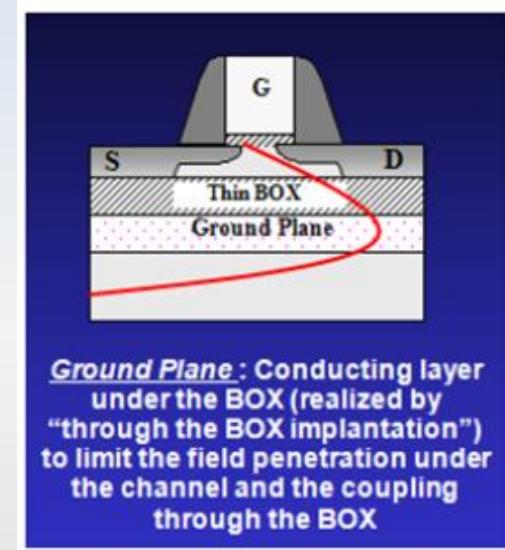
- **28UTBB-FDSOI Strategy:** GP option & Flipwell approach

**PART II**

**CMOS & Derivative PDK**



Ground Plane implant?	
Bulk	No. → Channel doping and gate oxide thickness to modulate the threshold voltage
FDSOI	Yes. → Suppress the depletion depth below the BOX for better DIBL → Improve the effect of the body biasing → Ground plane affects the electrostatic of the channel → V <sub>th</sub> shift of around 80 mV



No new CAD layer, because the ground plane implant is the same as the well

Introduction

Technology Overview

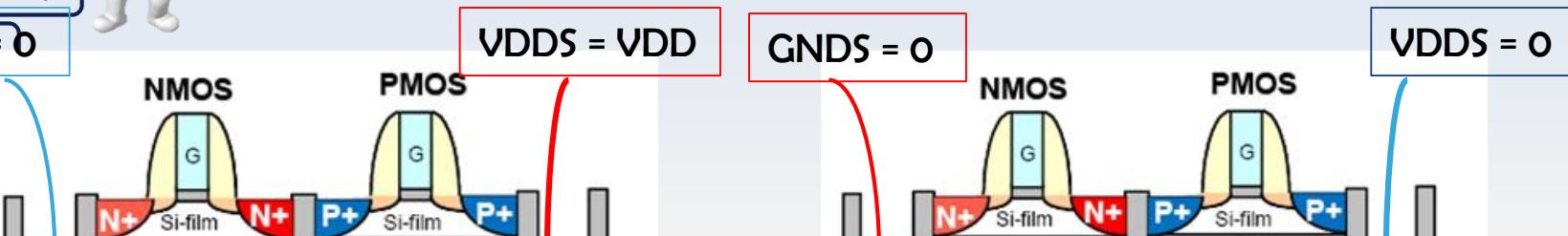
Design-Kit Contents

Roadmap

GNDS = 0



- Use of ground plane (GP) implant for VT adjustment



**Front end Structure is the same for RVT and LVT : no doping**

RVT Flavor – Standard well & GP

LVT Flavor – Flipped well & GP

pLVT already in FBB  
to reach the spec.

- Ground Plane is defined by the implant under the box :  
nLVT is NMOS with N-type Ground Plane →  $V_{th\_lin} \sim 400$  mV (Flip Well  $w=0.21\mu$   $l=30n$ )  
nRVT is NMOS with P-type Ground Plane →  $V_{th\_lin} \sim 480$  mV (Std Well  $w=0.21\mu$   $l=30n$ )

# TECHNOLOGY OVERVIEW

- **28UTBB-FDSOI Strategy: Poly Biasing**

**PART II**

**CMOS & Derivative PDK**

Introduction

Technology Overview

Design-Kit Contents

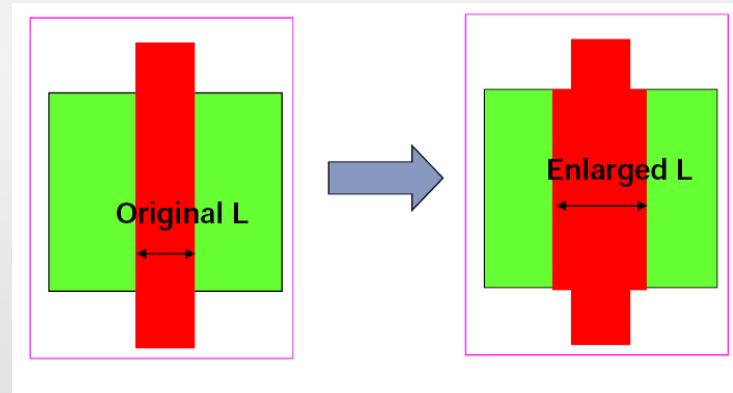
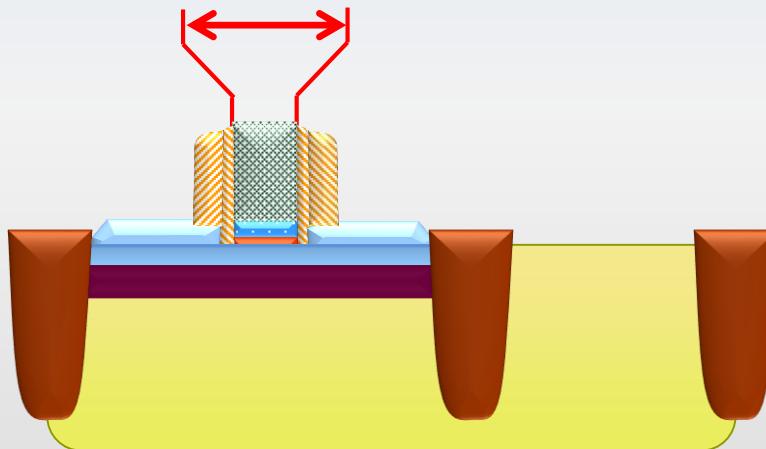
Roadmap

Support



- UTBB FD-SOI enables shorter channel length
- Enabling wider transistor effective gate length modulation

***From 28nm (PB0) up to 44nm (PB16)***

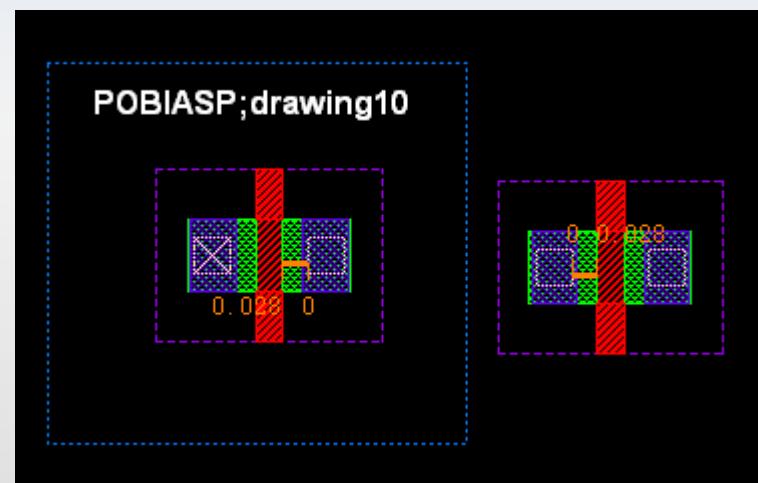


- CPP (Drawn) = 136 nm (relaxed, min is 126nm)



PolyBiasing layers	Note
POBIASP;drawing4 or 6 (wimpy)	Increase by 4 (2nm each edge), etc ..
POBIASP;drawing10 or 16	Increase by 10 (5nm each edge), etc ..

- The gate length increases with POBIASP, But not the active area (in green)
  - Perimeter and area of source and drain decrease.
  - Impact on the Poly rounding effect
  - Small impact on Cgs / Cgd



Used in the ST standard cells to change the performance of the cell.  
Wider range than in bulk : L vary from 28 ( nominal ) to 44 ( 28 +16 ) nm

# TECHNOLOGY OVERVIEW

- **28UTBB-FDSOI Strategy: Body Biasing**

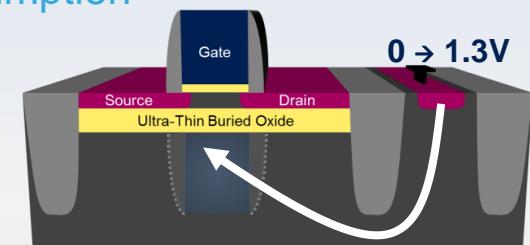
**PART II**

**CMOS & Derivative PDK**

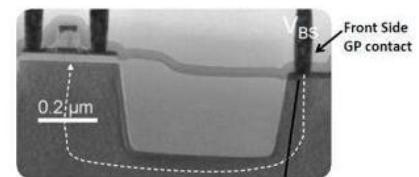
[Introduction](#)[Technology Overview](#)[Design-Kit Contents](#)[Roadmap](#)[Support](#)

## A very reasonable effort for extremely worthwhile benefits

- An **extremely powerful** and flexible concept in FD-SOI to :
  - Boost performance
  - Optimize passive and dynamic power consumption
  - Cancel out process variations and extract optimal behavior from all parts
- Comparatively **easy to implement**
  - No area penalty compared to Bulk
  - Reuse of Bulk design techniques
  - Speed/Power control

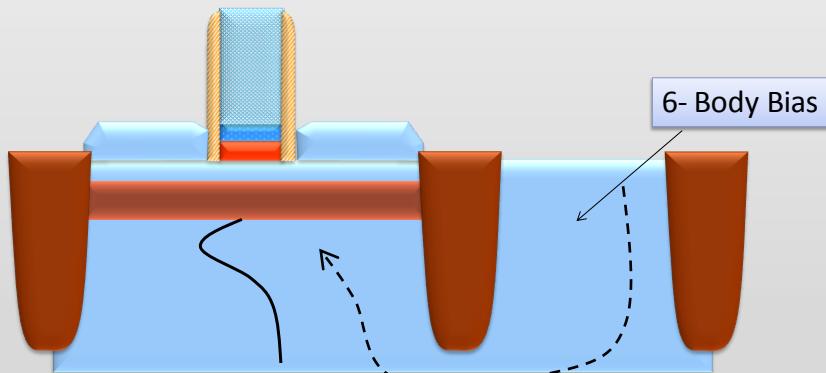
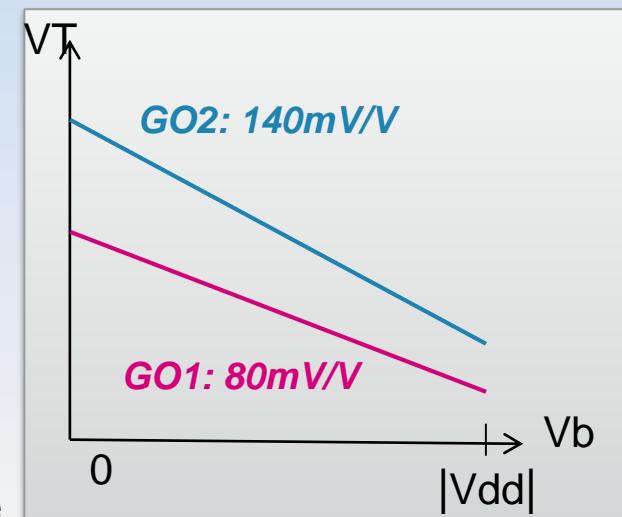


### Back-gate contact





- Create an own  $V_t$  with Body Biasing
  - consists of applying a voltage just under the BOX of target transistors
  - connecting the transistor bodies to a bias network in the circuit layout rather than to power or ground.
- Changes the electrostatic control of the transistors and shifts their threshold voltage
  - **Forward body bias (FBB):** lowers the threshold voltage by applying a positive body-to-source voltage to a n transistor (transistor both faster and leakier )
  - **Reverse body bias (RBB):** involves applying a negative body-to-source voltage to an n transistor, raises the threshold voltage (transistor both slower and less leaky)



Effects depends  
on flavors and n/p  
mos

Only 25mV/V in  
bulk technology +  
limited to 0.3V

Introduction

Technology Overview

Design-Kit Contents

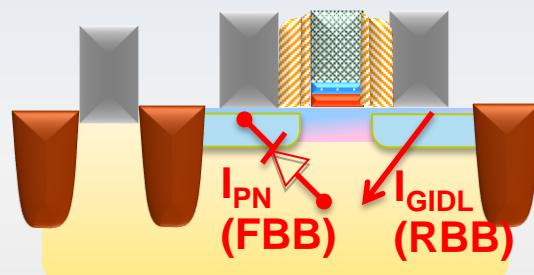
Roadmap

Support

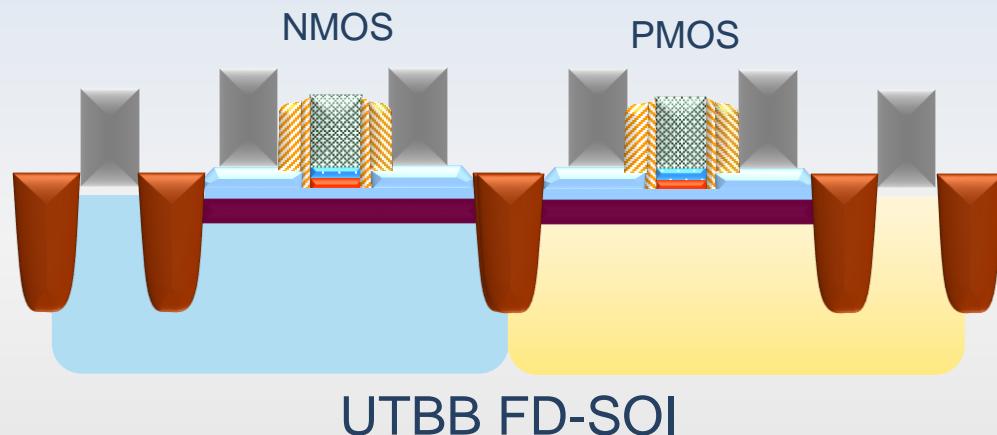


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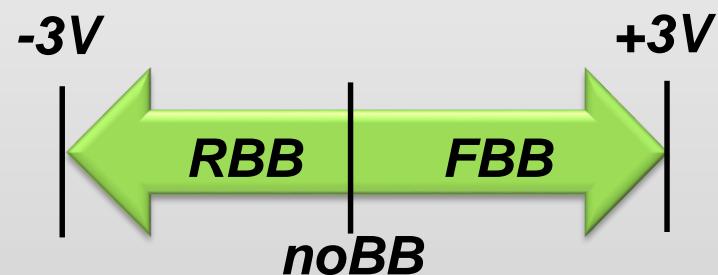
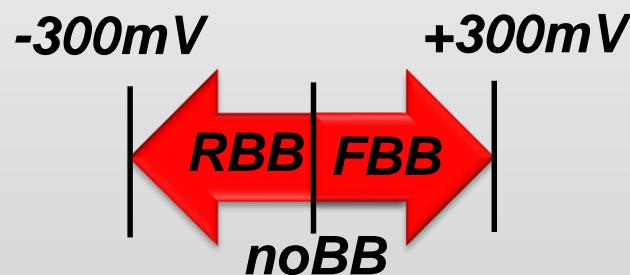
## Efficient knob for speed/leakage optimization



BULK



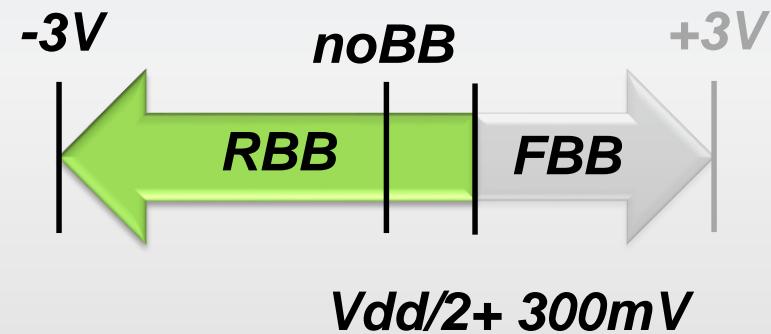
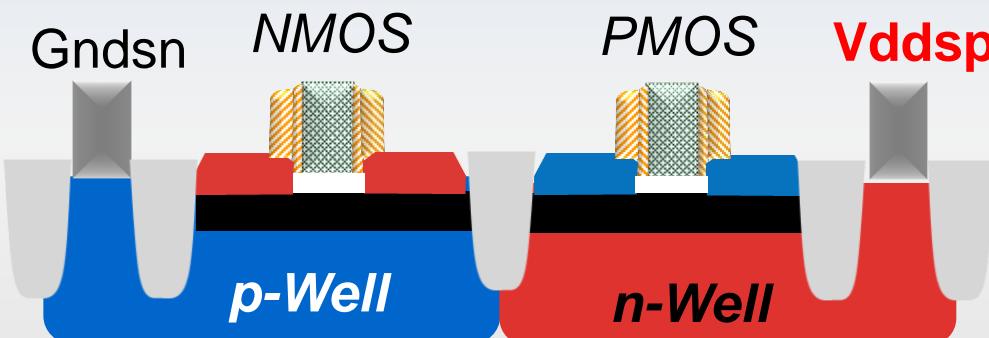
UTBB FD-SOI





## Conventional Well (CW) - RBB

RVT structure is RBB-oriented.  
Models are qualified up to -1.3V

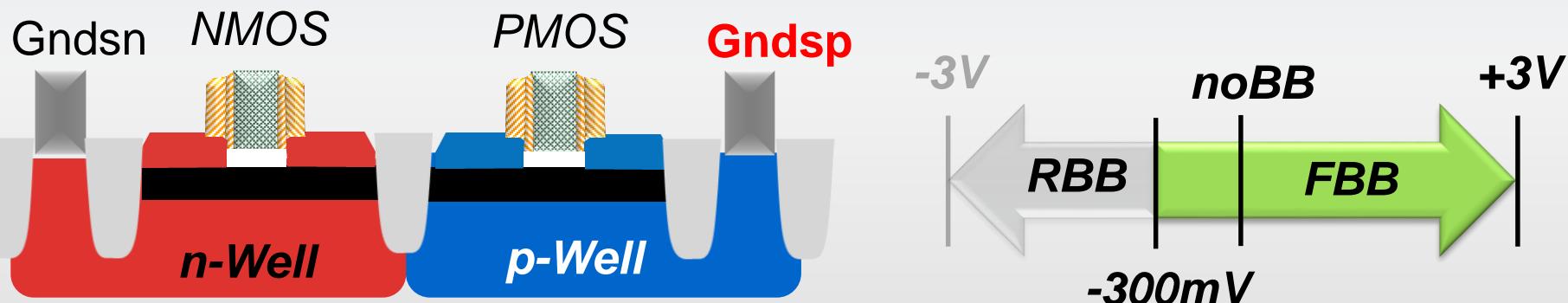


Efficient knob for speed/leakage optimization

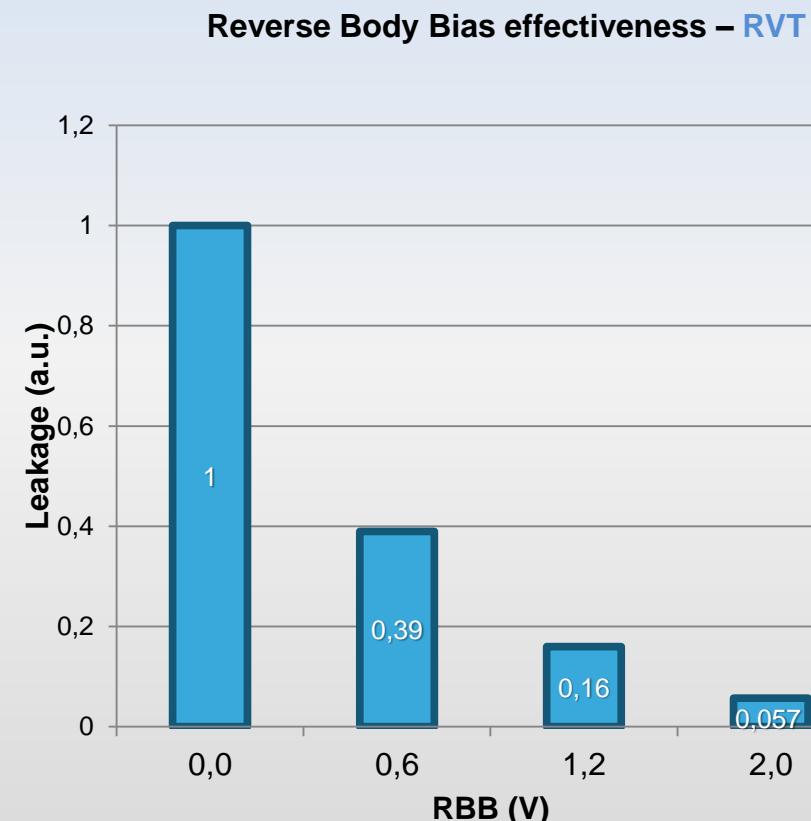
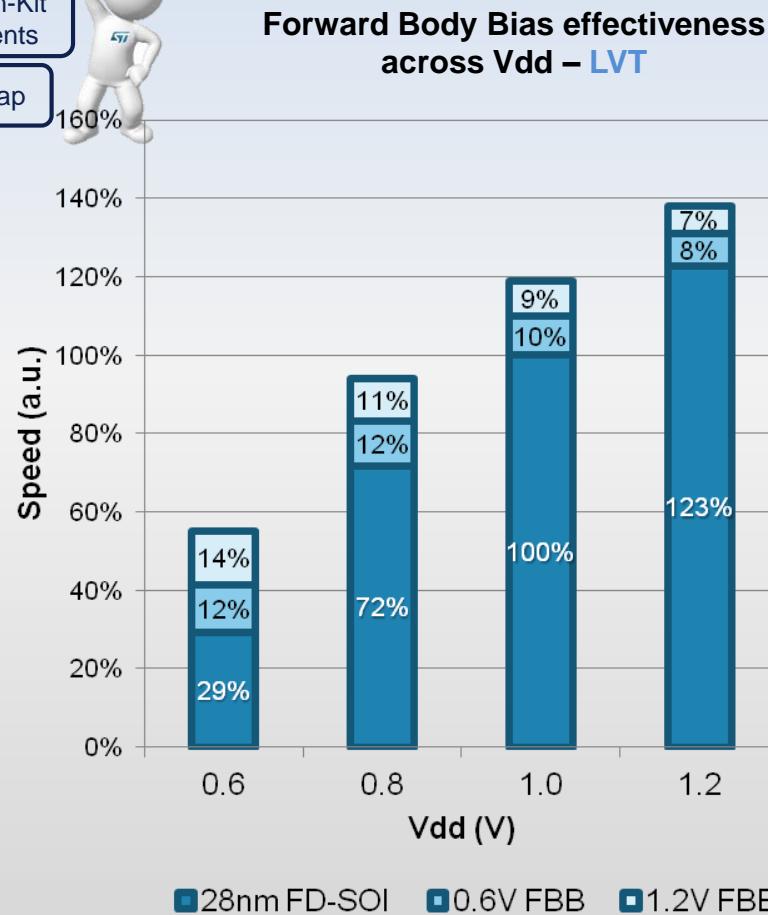


## Flip Well (FW) - FBB

LVT structure is FBB-oriented. Models are qualified up to +1.3V



Efficient knob for speed/leakage optimization



Introduction

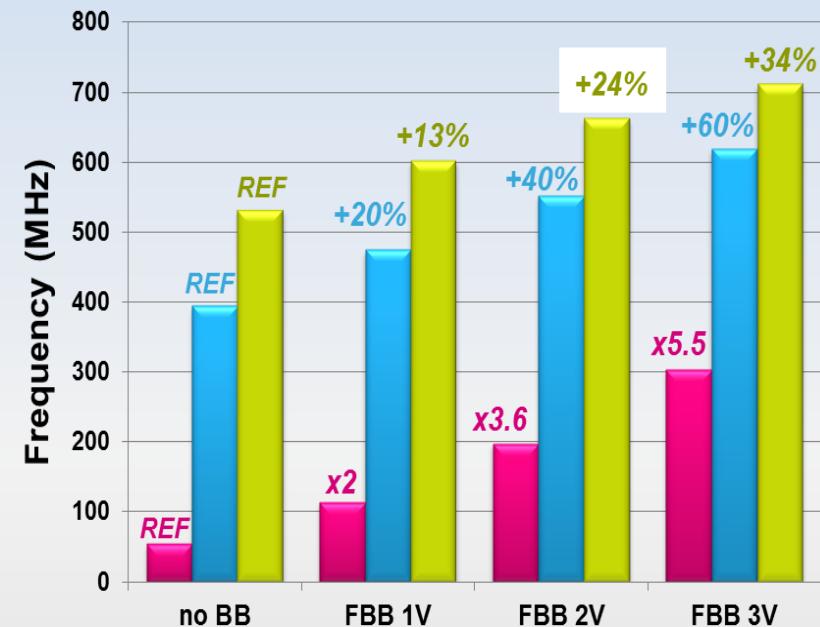
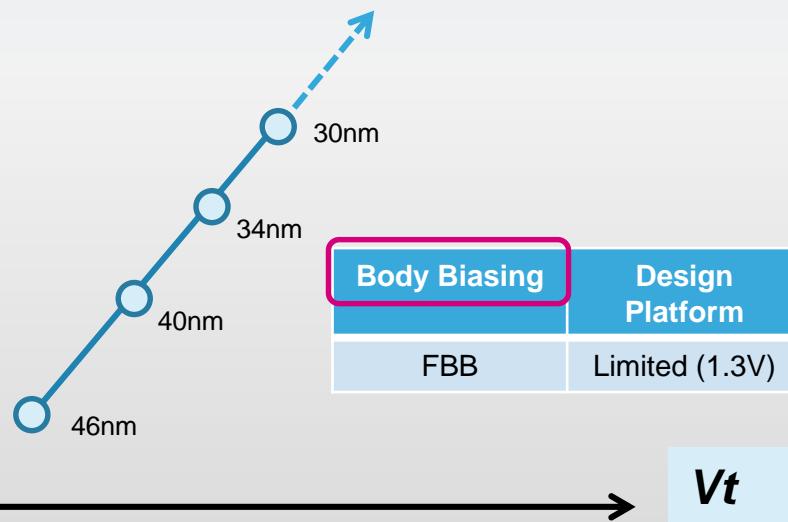
## High Performance optimization

Roadmap

Support

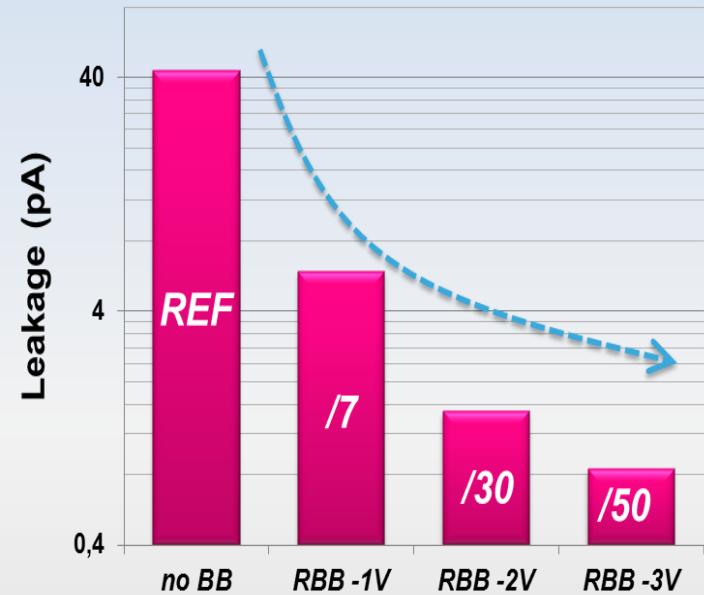
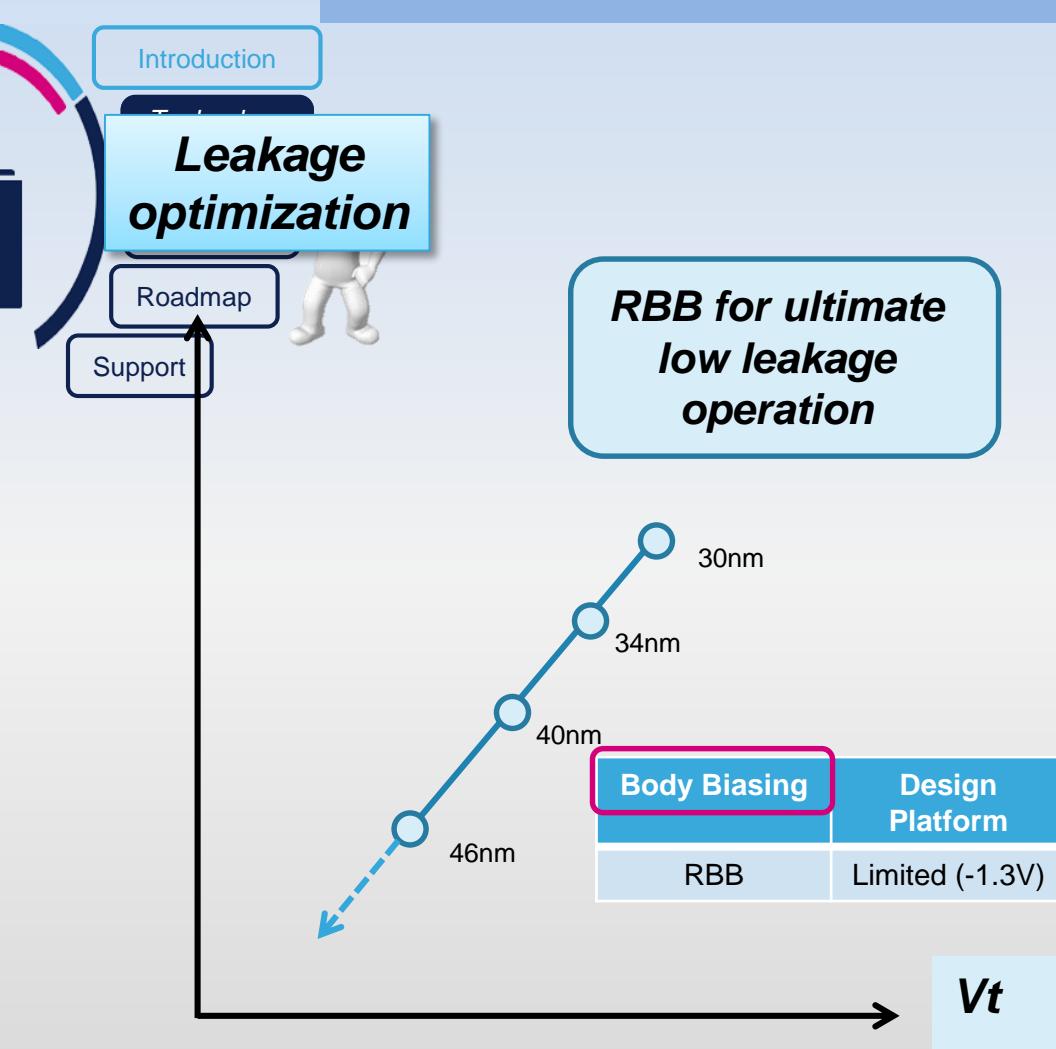


**FBB to reach  
desperate speed  
design zone**



**Ultra low  $V_t$  flavor  
created by design**

Applicable to products targeting ultimate frequencies (Servers)  
when speed cannot be achieved in the standard ( $V_{dd}$ ,  $P_b$ ) space



**Ultra high  $V_t$  flavor**  
**created by design**

Applicable to products targeting ultra low leakage (Internet of Things, Medical)  
when static consumption cannot be achieved in the standard ( $V_{dd}$ ,  $P_b$ ) space

# TECHNOLOGY OVERVIEW

- **28UTBB-FDSOI Strategy:** Usage & Limitation and Solutions

**PART II**

**CMOS & Derivative PDK**

Introduction

Technology Overview

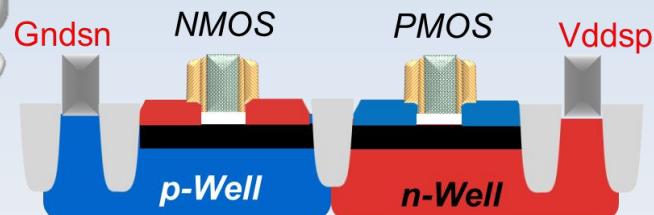
Design-Kit Contents

Roadmap

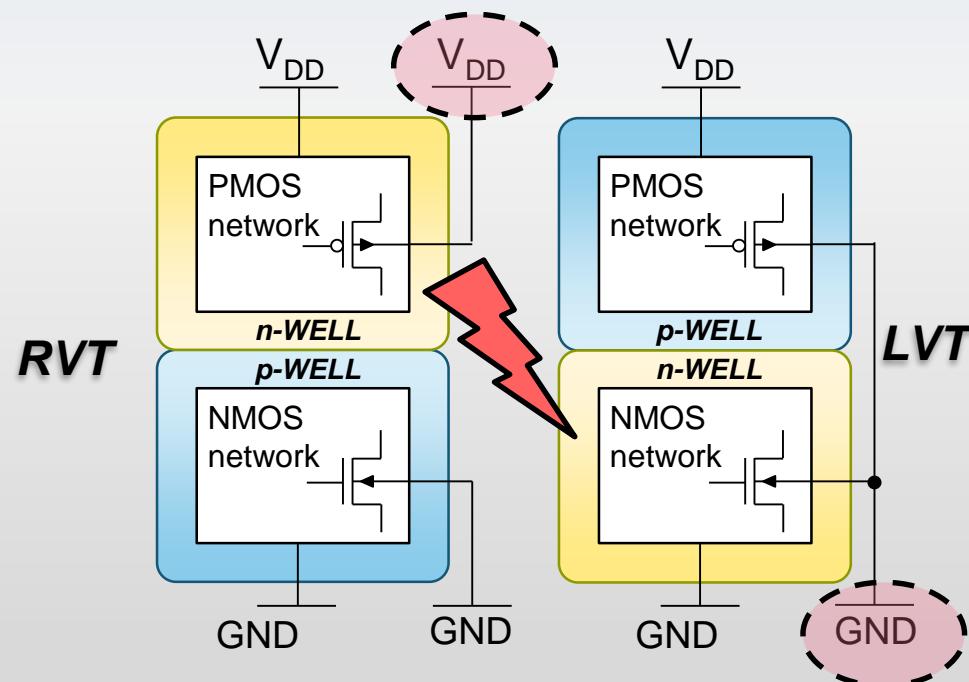
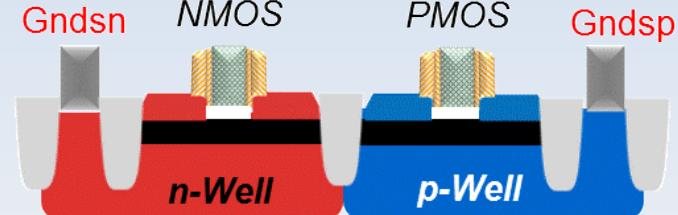
Support



- **RVT: Conventional Well (CW)**



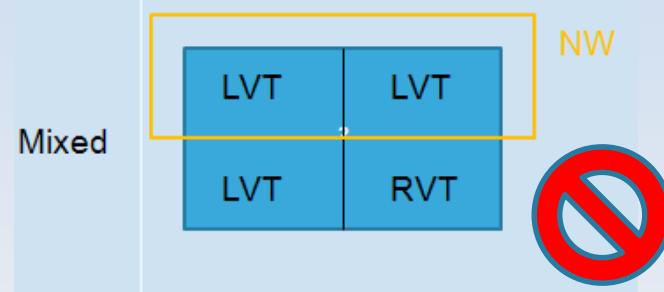
- **LVT: Flip Well (FW)**



**Well bias conflict when co-integrating standard LVT & RVT flavors**



- LVT and RVT cannot be mixed
  - nLVT mos are now in n-well !
- Solution :  
→ LVT and RVT blocks can be mixed
  - With the guard-ring protection ( Triple-well spacing rule : 3.5 um)



→To adjust speed and leakage target, it is needed no more to play with LVT/RVT, but

- Poly bias: PB4, ..., PB16
- Voltage: 0.8V, 1V, overdrive...
- Body Bias techniques: FBB, Full FBB and RBB.
- Explore possibilities of the technology ( single well approach ...)

# TECHNOLOGY OVERVIEW

- 28UTBB-FDSOI Required Layers

PART II

CMOS & Derivative PDK



- Specific layers & markers to define FDSOI & Bulk area

Name	Number	Description
<b>MKR;FDSOI</b>	202; 46	Marker layer to cover FDSOI contributions <i>(included in sealring pCell)</i>
<b>MKR;HSSOI</b>	204;56	layer to identify flipwell area (cover LVT devices)
<b>HYBRID</b>	201;122	Defines areas with NOSOI opening
<b>POBIASP;drawingX</b>	204;57	retarget all nominal gate length by + X nm within std cells ( X = 4, 6 ... 16nm )

Source: 28FDSOI Technology Design Manual

Introduction

Technology Overview

Design-Kit Contents

Roadmap

Support

**Requisite for 28FD technology:**

- Provide high performance at low voltage (key for mobile systems)
- Improve Switching Energy Efficient (key for mobile systems)
- Reduce the process cost thanks to process complexity contraction
- Guaranty IPs/design porting from 28LP bulk technology



**Diode-based devices have to be kept inside a bulk area**  
→ Co-integration (bulk/SOI)

**Devices list  
inside bulk area**

**Back-biasing solution:**

Wells taps

**Diodes suite:**

Regular diode

ESD diode

Antenna diode

**Bipolar:**

Vertical PNP bipolar

**Varactors:**

EG NCAP / EG PCAP

SG NCAP

**Resistors:**

Nwell resistance

Unsilicided diffusion resistance

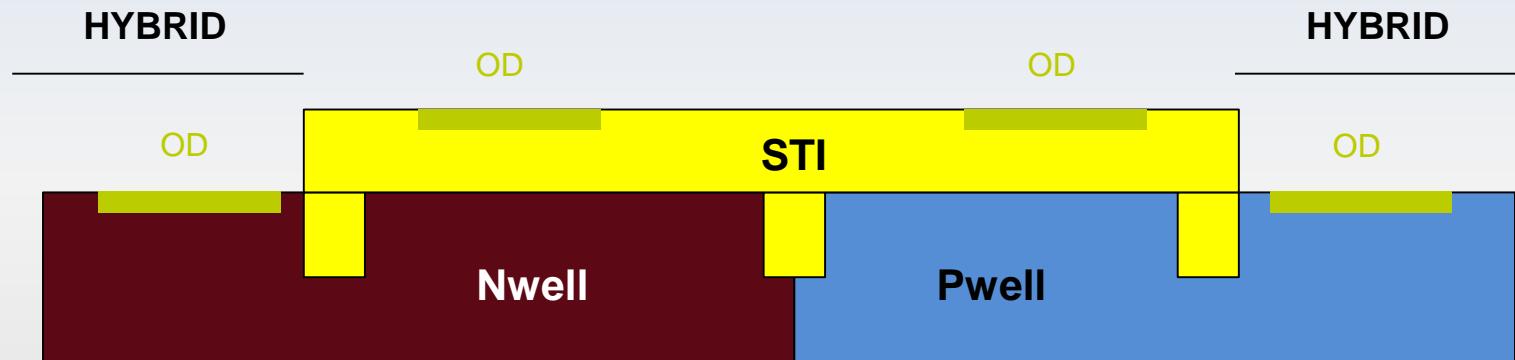
**MOSFETs:**

Unsilicided nMOS SG/EG transistor (ESD protection)

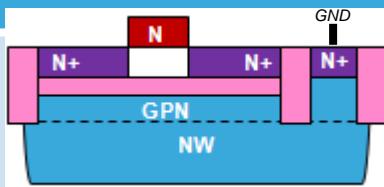
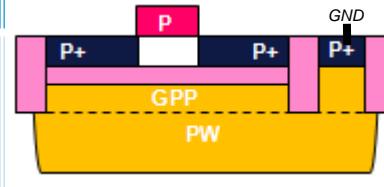
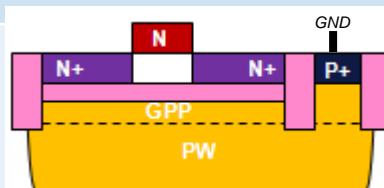
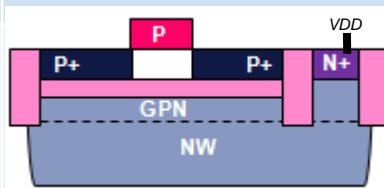
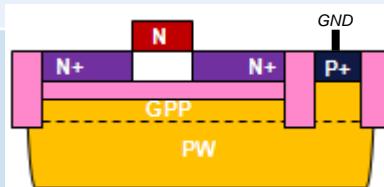
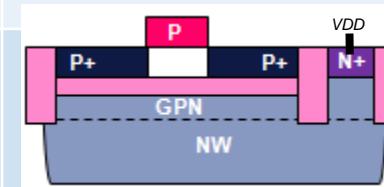
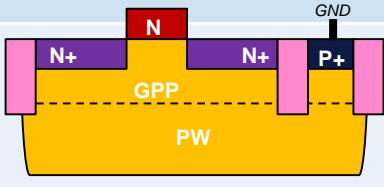
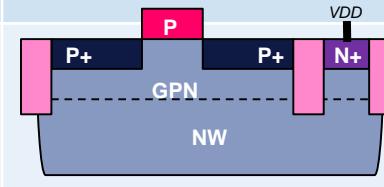


## • Layer (HYBRID ; drawing):

- This layer must be used to open bulk areas on SOI wafers
- Remove the silicon film and the Buried oxide (BOX) layer.



- This layer must be placed on diodes and substrate plugs (ntap / ptap and ncap or pcap) → Body biasing uses.
- Also used for specific devices : Vertical bipolar, ESD,drift MOS

Category	Architecture	NMOS	PMOS	Devices
LVT MOS devices <i>(HSSOI)</i>	Flip well (In Flip-Well area NW drawn reversed)			- LVT GO1/GO2 - ESD LVT MOS on SOI
RVT MOS devices	Flip GP			- RVT GO1/GO2 - ESD RVT MOS on SOI
SRAM array	Flip GP			- SRAM LL
Hybrid devices	Flip GP (Do not draw nominal gates on HYBRID (Lmin=48nm))			- ESD MOS on Bulk
<b><u>Note: FW &amp; non-FW area must be clearly separated (no mix of LVT &amp; RVT devices)</u></b>				

# DESIGN-KIT CONTENTS

- 28UTBB-FDSOI Devices Library

## PART III

CMOS & Derivative PDK

## Introduction

**MOSFETs devices**Thin oxide transistors suite:SG NMOS ( $V_{dd}^{nom}=1V$ ) RVT & LVTSG PMOS ( $V_{dd}^{nom}=1V$ ) RVT & LVTThick oxide transistors suite:EG NMOS ( $V_{dd}^{nom}=1.8V$ ) **RVT** & LVTEG PMOS ( $V_{dd}^{nom}=1.8V$ ) **RVT** & LVTEGV NMOS ( $V_{dd}^{nom}=1.5V$ ) **RVT** & LVTEGV PMOS ( $V_{dd}^{nom}=1.5V$ ) **RVT** & LVT

Power switch (EG PMOS RVT)

**RF MOSFETs devices**Thin oxide transistors suite:SG NMOS ( $V_{dd}^{nom}=1V$ ) RVT & LVTSG PMOS ( $V_{dd}^{nom}=1V$ ) RVT & LVTThick oxide transistors suite:EG NMOS ( $V_{dd}^{nom}=1.8V$ ) LVTEG PMOS ( $V_{dd}^{nom}=1.8V$ ) LVTEGV NMOS ( $V_{dd}^{nom}=1.5V$ ) LVTEGV PMOS ( $V_{dd}^{nom}=1.5V$ ) LVT**SRAM devices**HD cell / Single Port  $0.120\mu m^2$ HS cell / Single Port  $0.152\mu m^2$ RF cell / Dual Port  $0.298\mu m^2$ **ESD devices**

STI diodes / N+ on Pwell and P+ on Nwell

Transistors suite:

Unsilicided EG NMOS on bulk (RVT)

Unsilicided SG NMOS on bulk (RVT)

Unsilicided SG NMOS on SOI (RVT/LVT)

**OTP devices**

Cell capacitance / SG oxide on SOI

Drift transistor / EG NMOS RVT

**Analog devices**

Vertical bipolar device (PNP/NPN)

Varactor capacitance EG N/PCAP

MoM capacitor /  $2fF/\mu m^2$  min pitchResistances suite:

P+ poly unsilicided R

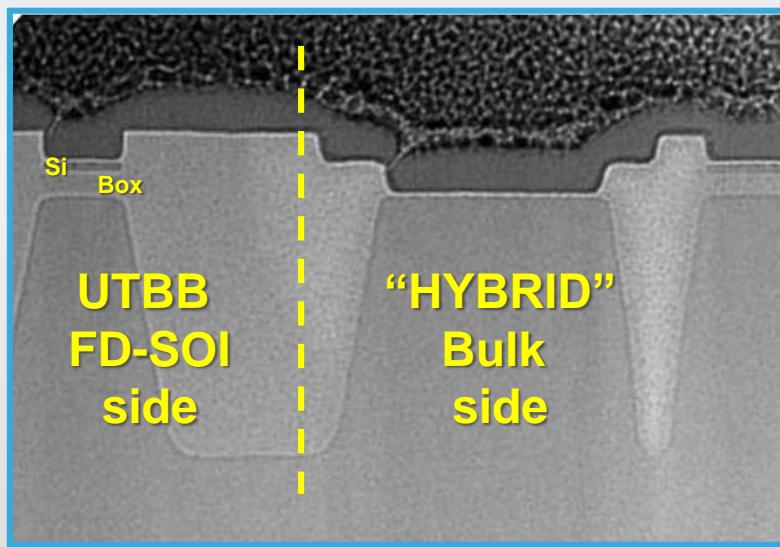
P+ poly unsilicided high precision R

N+ diffusion unsilicided R

N well R

**Decoupling devices**MiM capacitance /  $20fF/\mu m^2$  with Ta<sub>2</sub>O<sub>5</sub>**Devices break-down**

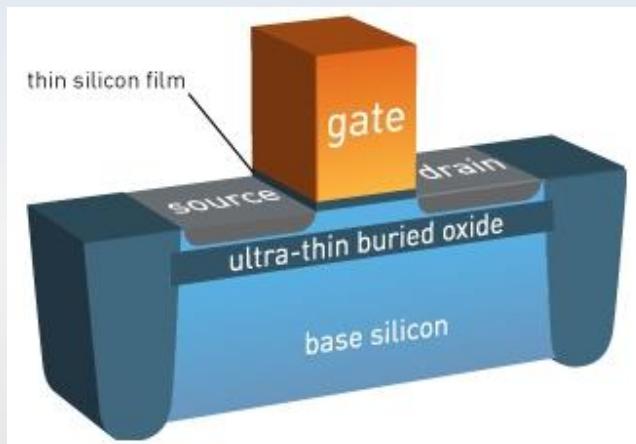
Device Type	SOI part	BULK part
MOSFET	All transistors (SG/EG)	
SRAM	All bit-cells (SP/DP/RF)	
Drift transistor		EG NMOS
Vertical Bipolar		PNP/NPN
Varactors		EG NCAP
Resistors	P+ Poly (on FO)	N+ diffusion / N well
Diodes suite		N+/Pw & P+/Nw
ESD Devices	SG/EG NMOS	SG NMOS



Device Type	UTBB FD-SOI	BULK
Logic	2Vt / PB0-16nm*	
SRAM	✓	
Capacitance	✓	
Varactor		✓
Drift MOS (OTP)		✓
Digital I/O	✓	
Resistors	✓ (Poly)	✓ (Active)
Diodes (antenna)		✓
ESD Devices	✓ (FET)	✓ (FET, diode, SCR)
Vertical Bipolar		✓

(\*) **PB = Poly Bias**

28nm UTBB technology allows for modulating logic transistor effective gate length in the range 24-40nm for the authorized poly/contact pitch. The bias number (PB) indicates the additional value to the minimal length (24nm).



## 28UTBB-FDSOI Mosfets



Show Categories

### Library

cmos32lp  
AMSBElib  
C28FDSOI\_MMW\_8ML  
MentorObserverLib  
ST\_C32\_addon\_AMS  
ST\_C32\_addon\_DP  
STlib  
aamix  
**Flipwell : LVT flavor**  
**GPF : RVT flavor**  
**mosRF : RF flavor**  
aatest  
adsLib  
analog  
artistkit\_addon  
basic  
cdsDefTechLib  
cmos28\_emetro  
**cmos32lp**  
cmos32lp\_Tech  
goldenGateLib  
lib\_test\_28  
mgcLib  
sbilib

### Category

Flipwell  
Everything  
Uncategorized  
BIPOLARS  
CAPACITORS  
DIODES  
DoNotUse  
ESD  
ESD\_Hierarchical\_Cells  
MOSFETS  
Flipwell  
GPF  
mosRF  
RESISTORS  
SRAM  
Wire\_Models

### Cell

eglvttnfet  
eglvttnfet\_b  
eglvttnfetnp  
eglvtppfet  
eglvtppfet\_b  
eglvtppfetw  
eglvtppspfet  
eglvtppspfet\_b  
eglvtppspfetw  
eglvttnfet  
eglvttnfet\_b  
eglvttnfetnp  
eglvtppfet  
eglvtppfet\_b  
eglvtppfetw  
lvtnfet  
lvtnfet\_b  
lvtnfetnp  
lvtpfet  
lvtpfet\_b  
lvtpfetw

- EG devices : 1.8V**
- w/o bulk connexion
  - tw/np suffix : body biasing use
  - spfet : power switch fet

- EGV devices : 1.5V**
- w/o bulk connexion \_b
  - tw/np suffix : body biasing use

- GO1 LVT fet : 1.0V**
- w/o bulk connexion \_b
  - tw/np suffix : body biasing use



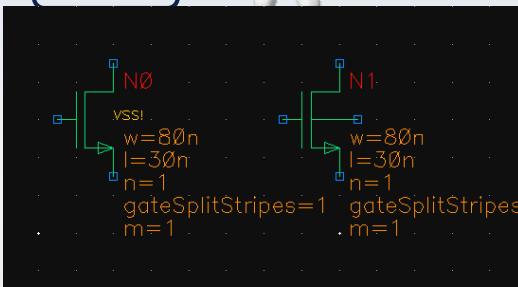
Introduction

Technology Overview

Design-Kit Contents

Roadmap

Support



## Geometrical range

L [ 30nm\* to 2 um ]

W [ 0.08 to 2um ]

- 1.0V low V<sub>t</sub> ( LVT ) and Regular V<sub>t</sub> ( RVT ) transistors ( GO1 = 18A )
- Cadence device name is the name of the model

DEVICES	DEVICES IN OPUS	MODEL NAME
NFET LVT	lvtnfet, lvtnfet_b**, lvtnfetnp	lvtnfet
PFET LVT	lvtpfet, lvtpfet_b**, lvtpfettw	lvtpfet
NFET RVT	nfet, nfet_b**, nfettw	nfet
PFET RVT	pfet, pfet_b**, pfetnp	pfet
NFET HLVT	hlvtnfet, hlvtnfet_b**, hlvtnfetnp	hlvtnfet
PFET HLVT	hlvtpfet, hlvtppfet_b**, hlvtppfettw	hlvtpfet

\* : At the mask data preparation, PC compensation shrinks the length by 6nm → 24nm is the effective length

\*\* : Regular devices have an inherited connection to bulk ( global VSS! Pin created ) \*b → 4 pins  
(Inherited Connections to minimize the amount of power supply wiring in schematics)



Introduction

Technology Overview

Design-Kit Contents

Roadmap

Support



- 1.8V Low V<sub>t</sub> EG and 1.5V EGV transistors  
→ For IO use ( G<sub>O2</sub> = 28A ).
- Cadence device name is the name of the model
  - Exception: eglvtnfet device has egltvnfet model. Same for pmos

DEVICES	DEVICES IN OPUS	MODEL NAME
28A LVT NFET 1.8V	eglvtfnfet, eglvtfnfet_b, eglvtfnfetnp	eglvtfnfet
28A LVT PFET 1.8V	eglvtvpfet, eglvtvpfet_b, eglvtvpfettw	eglvtvpfet
28A NFET 1.8V	egnfet, egnfet_b, egnfettw	egnfet
28A PFET 1.8V	egpfet, egpfet_b, egpfetnp	egpfet

**EG offer :**  
**L [ 0.15 to 2um ]**  
**W [ 0.08 to 2um ]**

**EGV offer :**  
**L [ 0.1 to 2um ]**  
**W [ 0.16 to 2 um ]**

DEVICES	DEVICES IN OPUS	MODEL NAME
28A LVT NFET 1.5V	eglvtfnfet, eglvtfnfet_b, eglvtfnfetnp	egltvnfet
28A LVT PFET 1.5V	eglvtvpfet, eglvtvpfet_b, eglvtvpfettw	eglvtvpfet
28A NFET 1.5V	egvnfet, egvnfet_b, egvnfettw	egvnfet
28A PFET 1.5V	egvpfet, egvpfet_b, egvpfetnp	egvpfet



Introduction

Technology Overview

Design-Kit Contents

Roadmap

Support

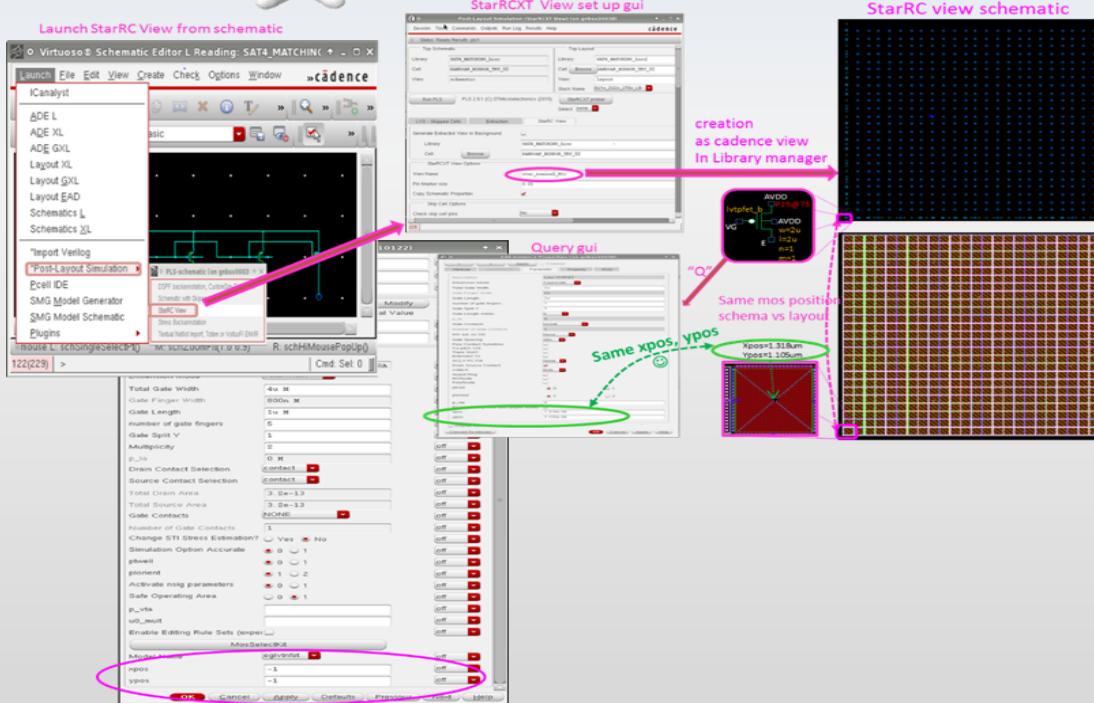


- RF MOS:
  - Specific MOS optimized for RF designs
  - Layout of the gate contact and guardring are different
  - Specific parameters on source and drain contacts for more accurate designs
- Cadence device name is the name of the model

DEVICES	DEVICES IN OPUS	MODEL NAME
18A LVT NFET 1.0V	lvtnfet_rf	lvtnfet_rf
18A LVT PFET 1.0V	lvtpfet_rf	lvtpfet_rf
18A RVT NFET 1.0V	nfet_rf	nfet_rf
18A RVT PFET 1.0V	pfet_rf	pfet_rf
28A LVT NFET 1.8V	eglvtfnfet_rf	eglvtfnfet_rf
28A LVT PFET 1.8V	eglvtfpfet_rf	eglvtfpfet_rf
28A LVT NFET 1.5V	egvlvtfnfet_rf	egvlvtfnfet_rf
28A LVT PFET 1.5V	egvlvtpfet_rf	egvlvtpfet_rf



- CAD solution for matching effect for all transistors (Core + RF)
  - New simulation level « Accurate » (enabled by default for new designs)
  - New instance parameters (xpos/ypos/plorient) available for schematic and post-layout simulations



See documentation

**\$PDKITROOT/doc/TRAININGS  
/New\_Matching\_Flow\_With\_St  
arRC\_TR.pdf**



- Mos active instance parameters

- Schematic/ Layout related parameters
- Impact in the simulation

- Mos inactive instance parameters

- No impact on the simulation

MosSelectKit

Robust Rules	<input type="radio"/> 0 <input checked="" type="radio"/> 1
Dimension Mode	TotalWidth <input type="button" value="▼"/>
Total Gate Width	80n M
Gate Finger Width	80n M
Gate Length	30n M
number of gate fingers	1
Gate Split Y	1
Multiplicity	1
Gate Length Adder	0 <input type="button" value="▼"/>
p_ia	0 M
Drain Contact Selection	contact <input type="button" value="▼"/>
Source Contact Selection	contact <input type="button" value="▼"/>
Total Drain Area	6.08E
Total Source Area	6.08E
Gate Contacts	NONE <input type="button" value="▼"/>
Number of Gate Contacts	1
Change STI Stress Estimation?	<input type="radio"/> Yes <input checked="" type="radio"/> No
Simulation Option Expert	<input checked="" type="radio"/> 0 <input type="radio"/> 1
Gate Spacing	96n <input type="button" value="▼"/>
Poly Contact Symetries	<input type="checkbox"/>
M1Route	<input type="checkbox"/>
PolyRoute	<input type="checkbox"/>
ptwell	<input checked="" type="radio"/> 0 <input type="radio"/> 1
Activate nsig parameters	<input checked="" type="radio"/> 0 <input type="radio"/> 1
Safe Operating Area	<input type="radio"/> 0 <input checked="" type="radio"/> 1
X-coordinate of gate	-1 M
Y-coordinate of gate	-1 M
plorient	<input checked="" type="radio"/> 1 <input type="radio"/> 2
Enable Editing Rule Sets (experimental)	<input type="checkbox"/>
Bulk	vss!
Source First	<input checked="" type="checkbox"/>

Parameters to manage device dimension

Parameters which have influence on both schematic and layout

Simulation parameters

Specific parameters



- **STI estimation**

- sa, sb ,sd, schematic only
- give access to the parameter for customization.

Change STI Stress Estimation?  Yes  No

STI Compression (sa) 1.8u M

STI Compression (sb) 1.8u M

- **Accurate switches**

- enable features as accurate simulation level, gate resistance...
- **Only** for LVT, RVT, EGLVT and EG LVT mosfets



- **Swrg** (Activate Gate Resistance modeling)
  - swrg=0: no gate resistance
  - swrg=1 (default): gate resistance activated (recommended)
- **Swshe** (Activate Self Heating)
  - swshe=0 (default): self-heating deactivated
  - swshe=1: self-heating activated
- **Mismatch**
  - 1 (default): mismatch is enabled if it is activated by ArtistKit
  - 0: disabled mismatch locally



cdf	Values	Meaning
swrg	0	Simulation standard
	1 (default)	Simulation Accurate
Self heating	0 (default)	Use self heating: No
	1	Use self heating : Yes
Mismatch	0	Use self mismatch: No
	1 (default)	Use self mismatch :Yes



Introduction

Technology Overview

Design-Kit Contents

Roadmap

Support



- **SOA (Safe Operating Area)**
  - To check if the device conditions of use are in safe mode
    - 1 (default): checks available if it is activated by ArtistKit
    - 0: disabled SOA locally
- **Multiplicity**
  - schematic only : number of device in parallel. On the layout side : always equal to one.



Drain Contact Selection	<input type="button" value="contact"/>
Source Contact Selection	<input type="button" value="contact"/>
Total Drain Area	6.08f
Total Source Area	6.08f
Total Drain Periphery	312n
Total Source Periphery	312n

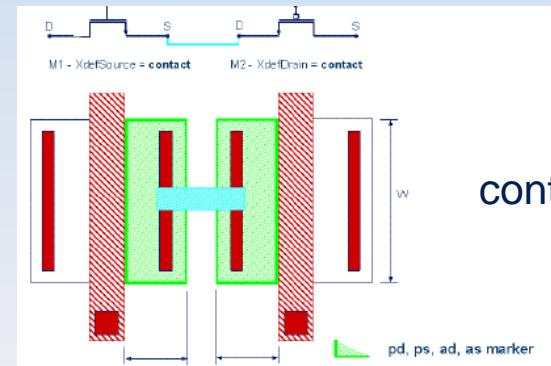
- **Drain/Source contact Selection :**
  - Describe layout configuration in schematic to be as closed as possible than the physical design.
  - Impact on sa/sd & pa/pd.
  - value are editable only if USER mode is chosen, if not parameters are automatically calculated.
  - **Values:**

**contact:** No butting to other source/drain region

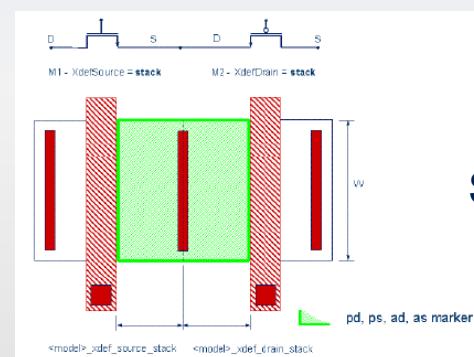
**stack:** Drain will be abutted to another source/drain keeping contacts

**noStack:** Drain will be abutted to another source/drain, no contacts are kept

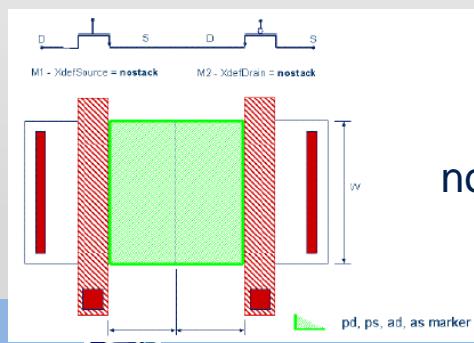
- **user:** User have to specify ad and pd



contact



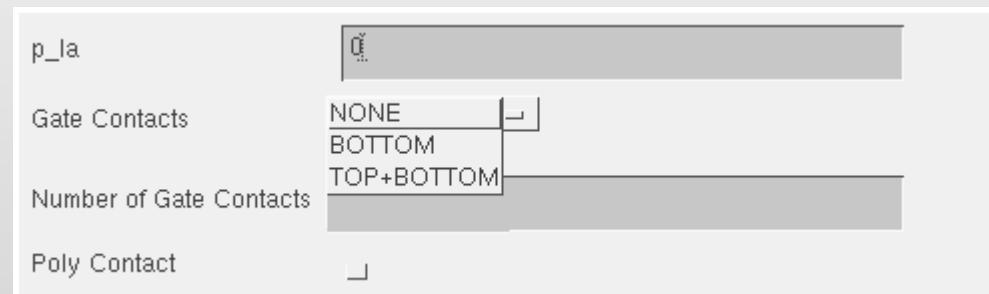
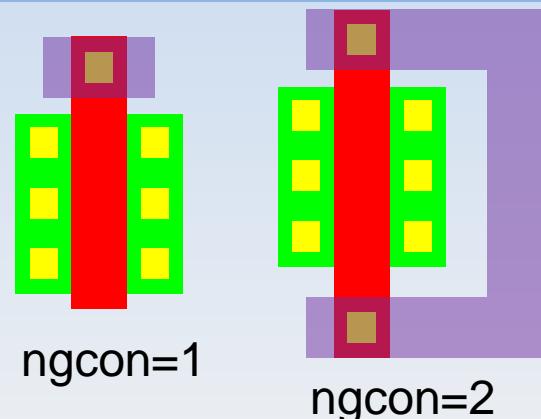
Stack



noStack



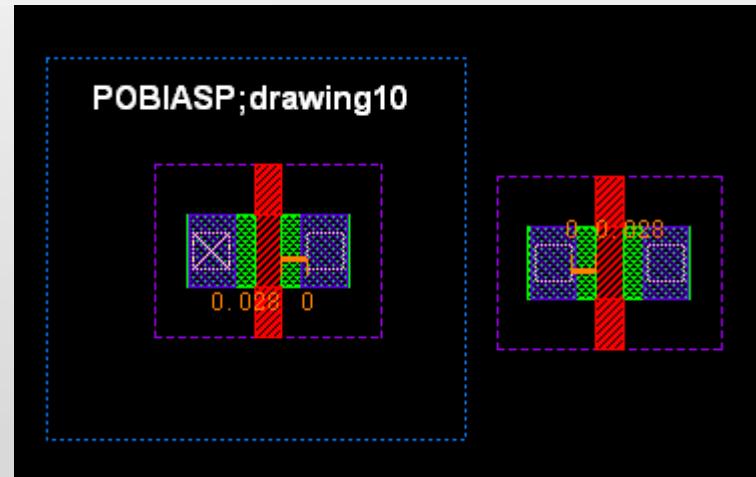
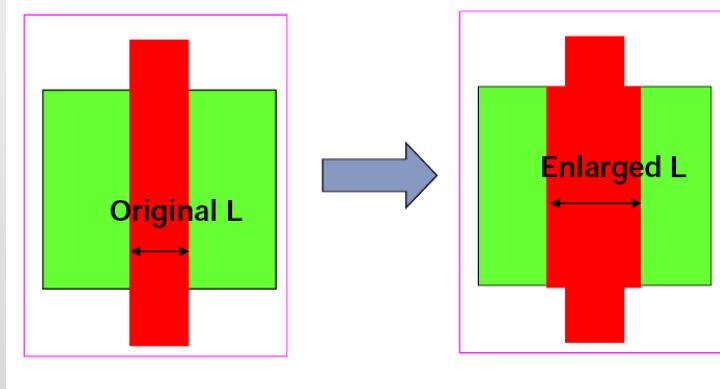
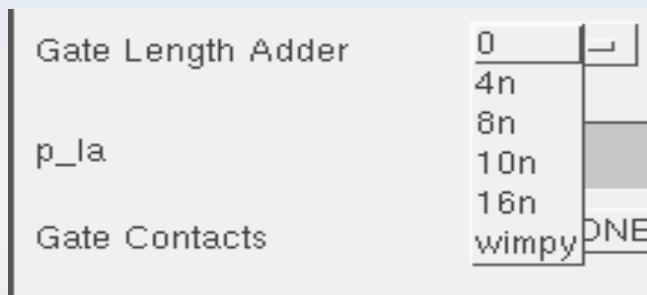
- **Number of gate contact ngcon**
  - Values [1,2]
  - Default value 1
  - Ngcon is extracted from the layout
  - Used in RF when we measure the gate resistance  
( param SWRG=1 ) NGCON will impact this gate resistance.
- can be modified in schematic because users can decide to take into account the effect during pre-layout simulation





## • Gate Length Adder (*parameter p\_la*)

- increase the gate length without changing L (also called polybiasing)
- can modify the length of the pcell by adding some markers.





Introduction  
Technology Overview  
**Design-Kit Contents**  
Roadmap  
Support



- Mos active instance parameters

- Schematic/ Layout related parameters
- Impact in the simulation

- Mos inactive instance parameters

- No impact on the simulation

Dimension Mode	TotalWidth
Total Gate Width	1u M
Gate Finger Width	1u M
Gate Length	30n M
number of gate fingers	1
Drain Contact Selection	Contact
Source Contact Selection	contact
Total Drain Area	87f
Total Source Area	87f
Total Drain Periphery	1.174u
Total Source Periphery	1.174u
Number of gate accesses	1
Change STI Stress Estimation?	<input type="radio"/> Yes <input checked="" type="radio"/> No
Average Poly Spacing	106n
Simulation Option Expert	<input checked="" type="radio"/> 0 <input type="radio"/> 1
Safe Operating Area	<input type="radio"/> 0 <input checked="" type="radio"/> 1
X-coordinate of gate	-1 M
Y-coordinate of gate	-1 M
Orientation of the transistor	<input checked="" type="radio"/> 1 <input type="radio"/> 2
Number of gate contact rows	2
Number of contact rows on inner	1
Number of contact rows on inner	1
Number of contacts per row or	10
Distance contacts to gate on s	33n
Number of contacts per row or	10
Distance contacts to gate on d	33n
Guardring Segments	TB
Netlisted Strap	2
Presence of deep nwell	<input checked="" type="radio"/> 0 <input type="radio"/> 1
Activate nsig parameters	<input checked="" type="radio"/> 0 <input type="radio"/> 1
Strap width	160n M
Distance strap to RX	347n M

Parameters to manage device dimension

Parameters which have influence on both schematic and layout

Simulation parameters



Introduction

Technology Overview

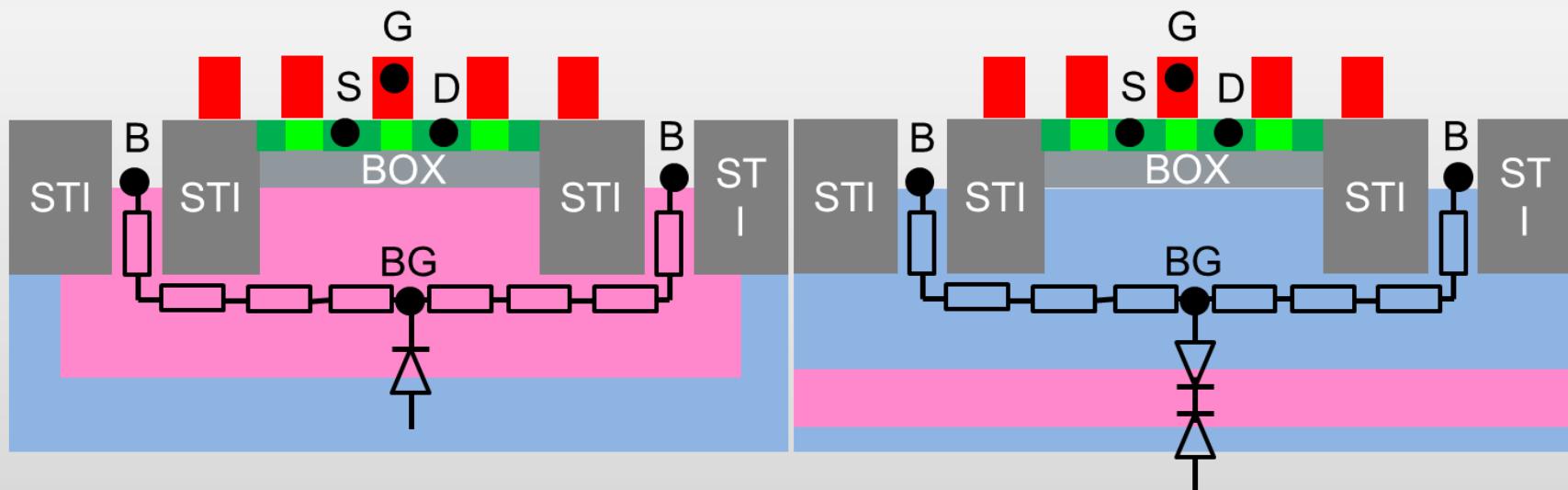
Design-Kit Contents

Roadmap

Support



- Fifth pin available for isolated configuration to properly describe HF behavior of substrate regions
- In standard MOS transistors, when substrate diodes (PW/NW, PW/DNW, etc.) are extracted, they are connected to B terminal of MOS.
- For RF MOS, they are connected to BG terminal





## 28UTBB-FDSOI Mosfets pcell features: layout

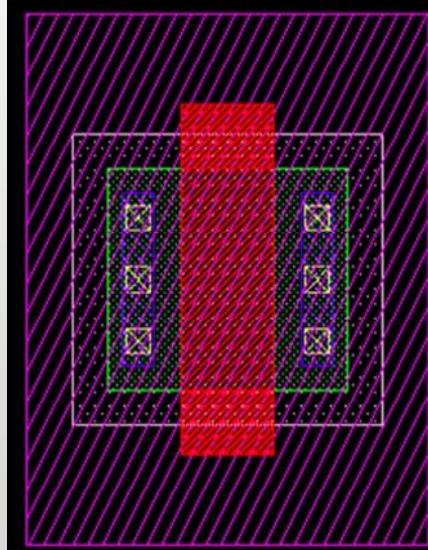


- **Robust rules:** applies some DFM rules to be compliant with the SRD DFM checker

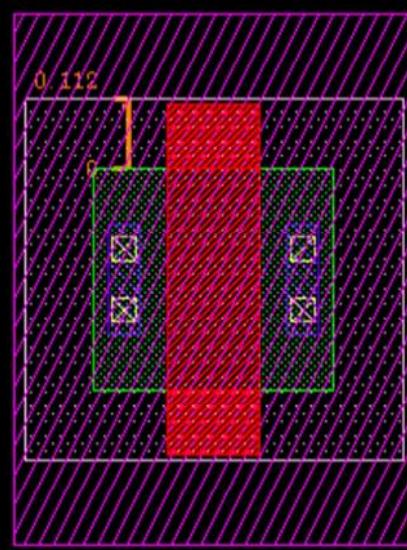
- Switch activated by default for new devices
- Only for core mosfets
- BP enclosure  $0.112\mu\text{m}$
- Vertical RX enclosure on CA  $0.03\mu\text{m}$

Ex: egpfet

Non DFM pcell



DFM pcell





Introduction

Technology Overview

Design-Kit Contents

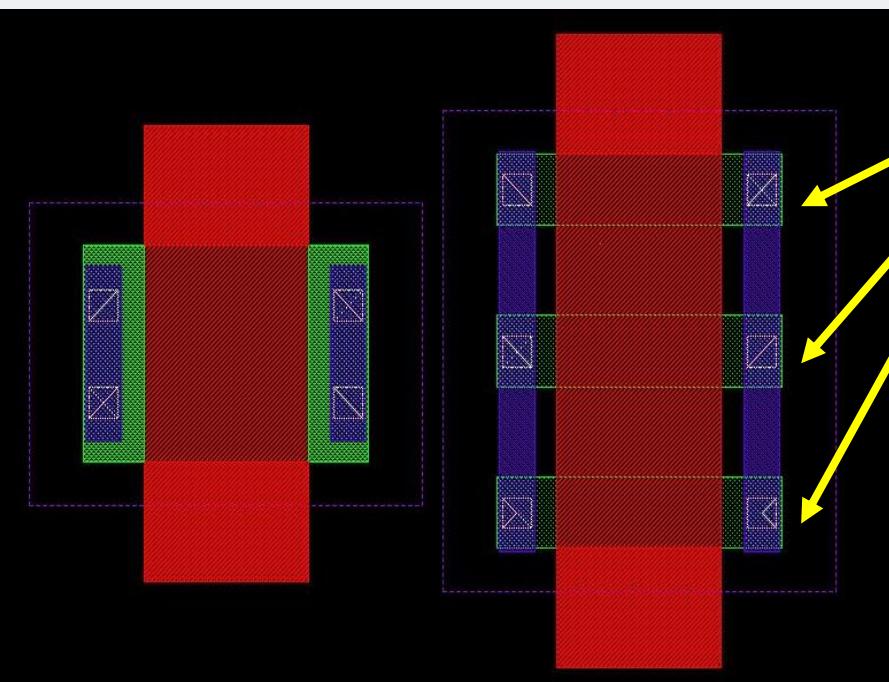
Roadmap

Support



- **gateSplitStripes Y pCell parameter:**

- Number of gate splits in Y-direction.
- Produces individual RX shapes in device layout.
- Influences pd (drain perimeter) and ps (source perimeter) calculation.



Gate Split Y=3

CDF Parameter	Value
Description	UTSOI model
Dimension Mode	TotalWidth
Total Gate Width	80n M
Gate Finger Width	80n M
Gate Length	30.00n M
number of gate fingers	1
Gate Split Y	1

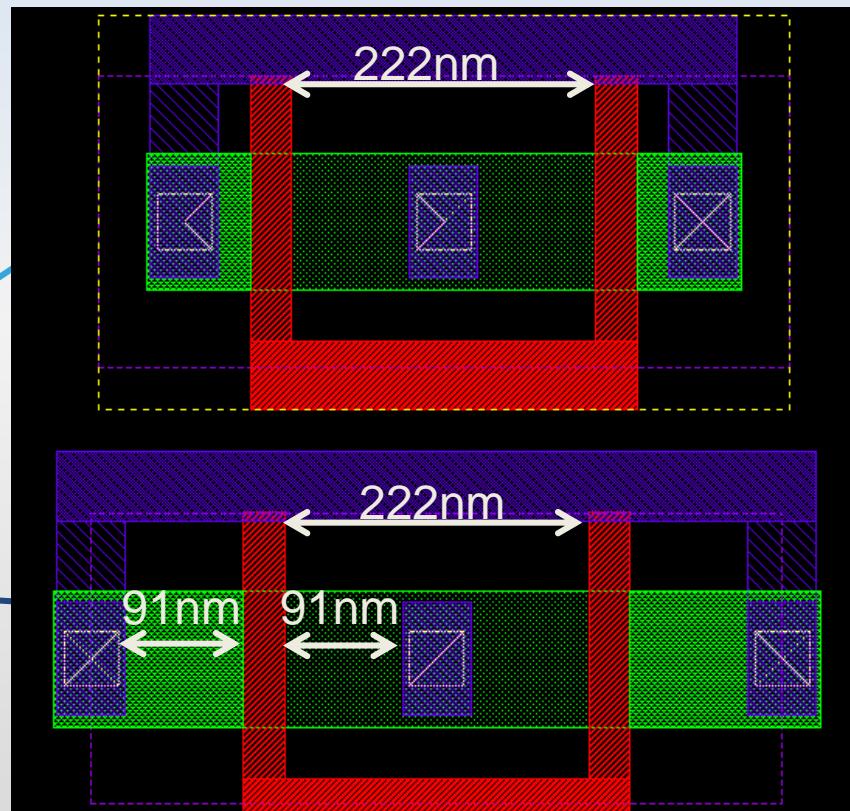


- Introduction
- Technology Overview
- Design-Kit Contents**
- Roadmap
- Support



- **Gate spacing (case 1) :** switch to change the distance between the fingers of the transistor.
- **Poly Contact Symmetries (case 2) :** switch to enable symmetries around the gate i.e. the contacts are at the same distance to the gate.

Gate Spacing	<input type="button" value="222n"/>
Poly Contact Symmetries	<input checked="" type="checkbox"/>
Triple Well?	<input type="checkbox"/>
ACLV PC Fill	<input type="button" value="None"/>
Drain Source Contact	<input checked="" type="checkbox"/>
cntBLR	<input type="button" value="Both"/>
Guard Ring	<input type="checkbox"/>



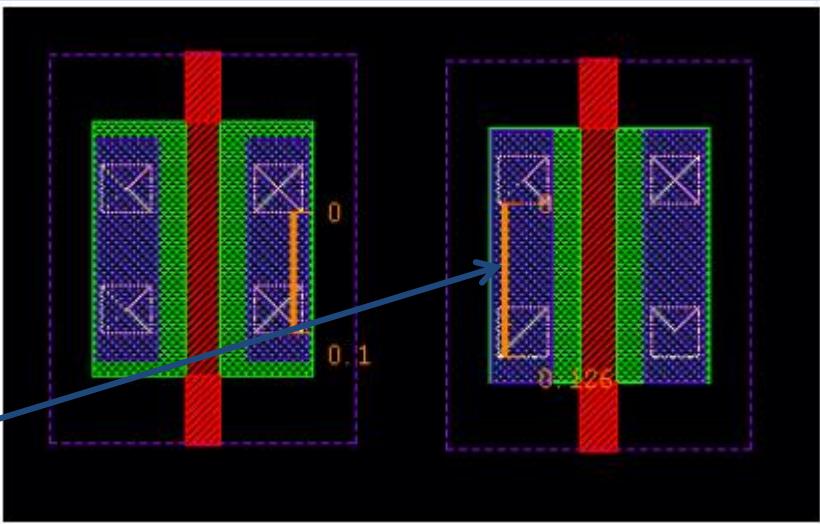
Helps to reduce the capacitance between the gate and the source/drain contacts.



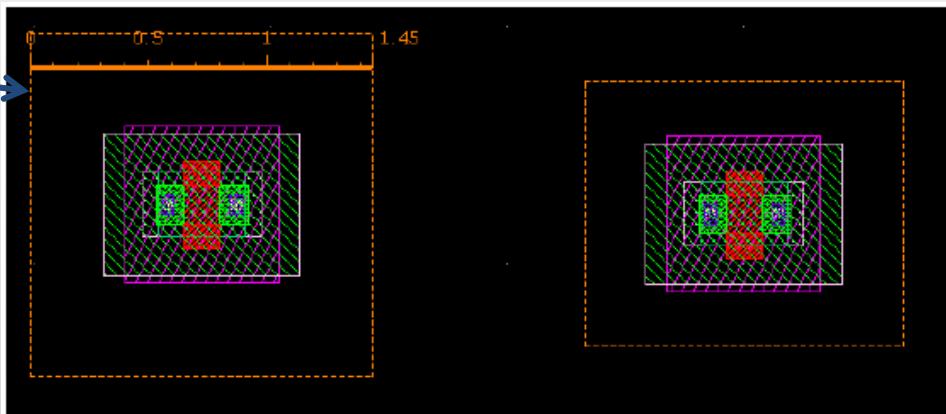
Gate Spacing 96n

- Custom Gate Spacing
- Poly Contact Symmetries
- Ca pitch 126
- Triple Well?

- **Ca pitch 126** : switch to choose between 2 values of spacing for CA (100 or 126n)



- **Extended T3** : gives the possibility to extend T3





Introduction

# MOS Layout Parameters

77

**Gate Contact:** add contact on the gate automatically.

Overview

**Triple well:** add the minimum t-well around the mos.

**ACLV PC Fill : Option Right :** add a dummy poly on the right of the gate's transistor. ( both sides possible)

**Drain Source Contact :Option Left :** add only contact on the left side on the structure ( Right/both options are available)

Gate Contacts **TOP+BOTTOM**

Number of Gate Contacts **2**

NW ext. on OD **None**

Gate Spacing **96n**

Custom Gate Spacing

Poly Contact Symmetries

Ca pitch 126

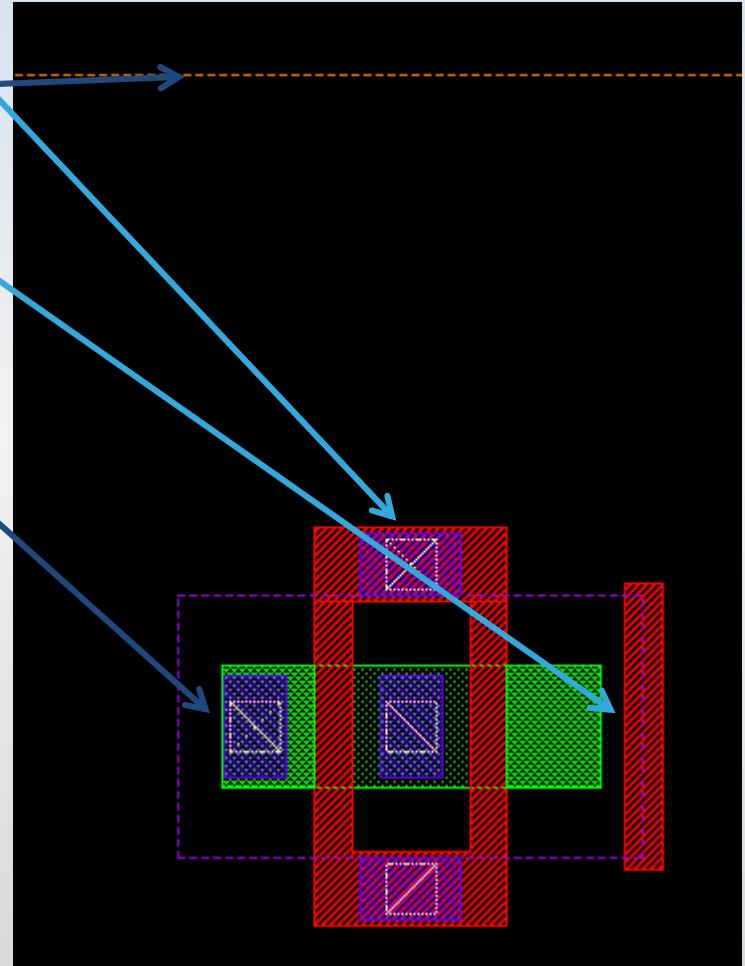
Triple Well?

ACLV PC Fill **Right**

Drain Source Contact

cntBLR **Left**

Guard Ring





Introduction

Technology Overview

Design-Kit Contents

Roadmap

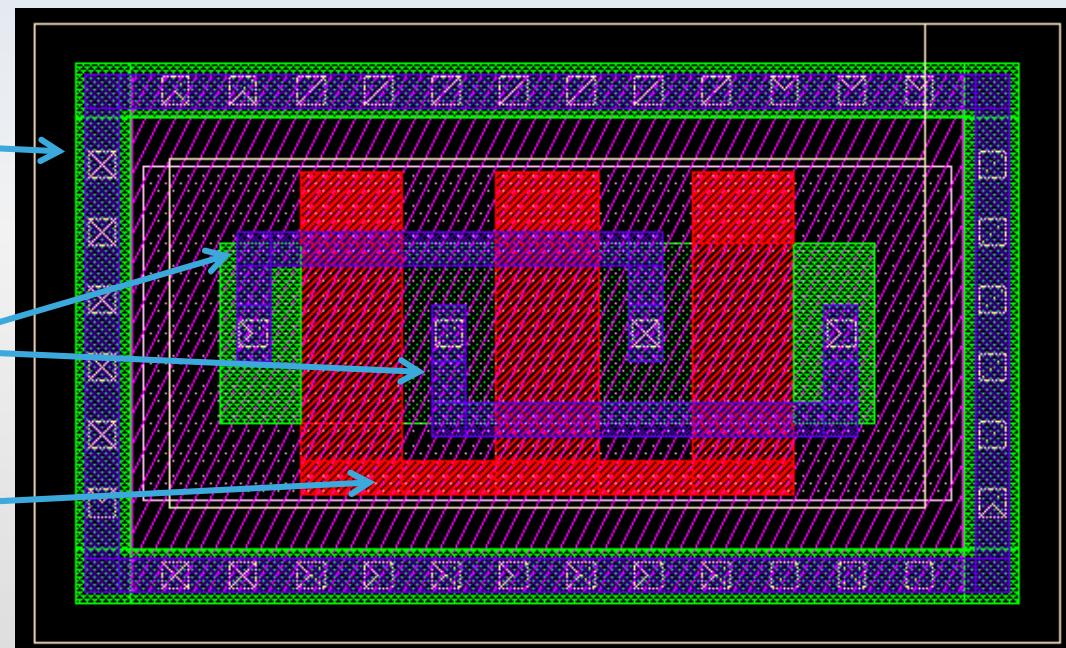
Support



**Guard ring** : enables guard ring around the device

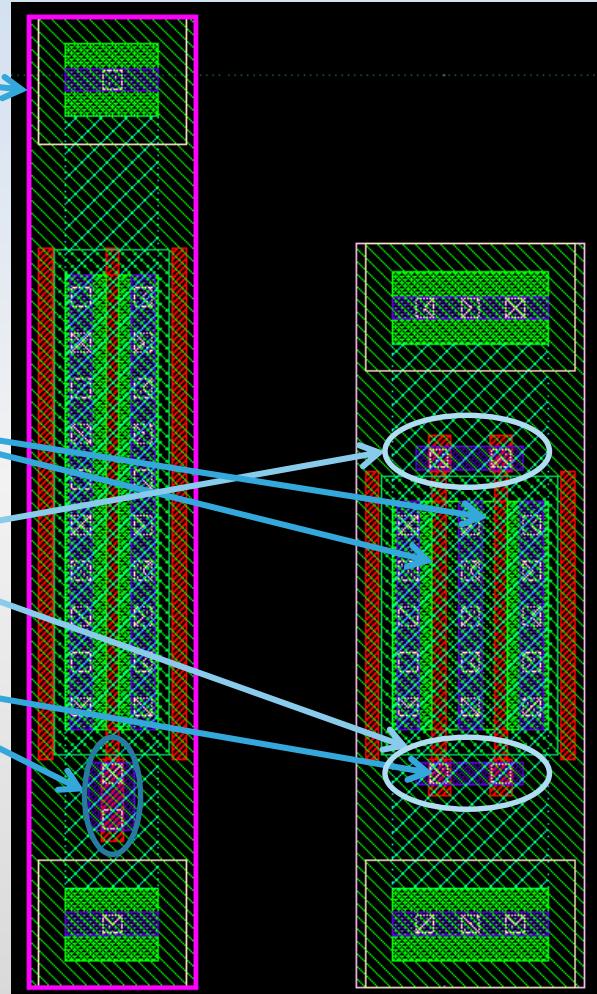
**M1Route** : Enables M1 routing of source/drain regions for multi-finger devices

**PolyRoute** : Enables PC routing of gates for multi-finger devices

Guard Ring M1Route   
PolyRoute 



Default layout of  
lvtnfet\_rf



**n:** number of gate fingers

**ngcon :** number of gate accesses (*bottom* or *bottom and top*)

**ncrg :** number of gate contact rows (1 or 2)

number of gate fingers

1

Number of gate accesses

1

Average Poly Spacing

106n

Number of gate contact rows

2



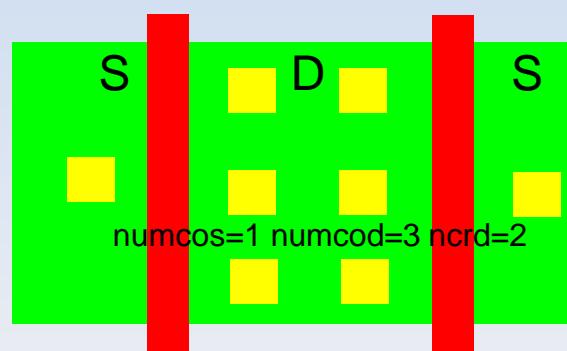
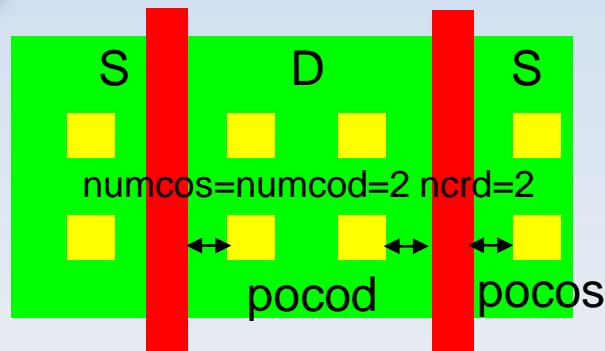
Introduction

Technology Overview

Design-Kit Contents

Roadmap

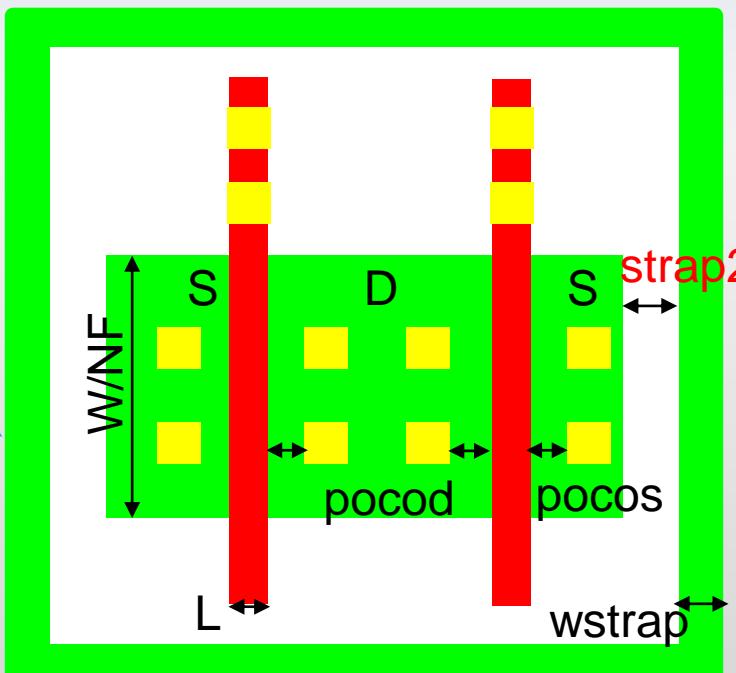
Support

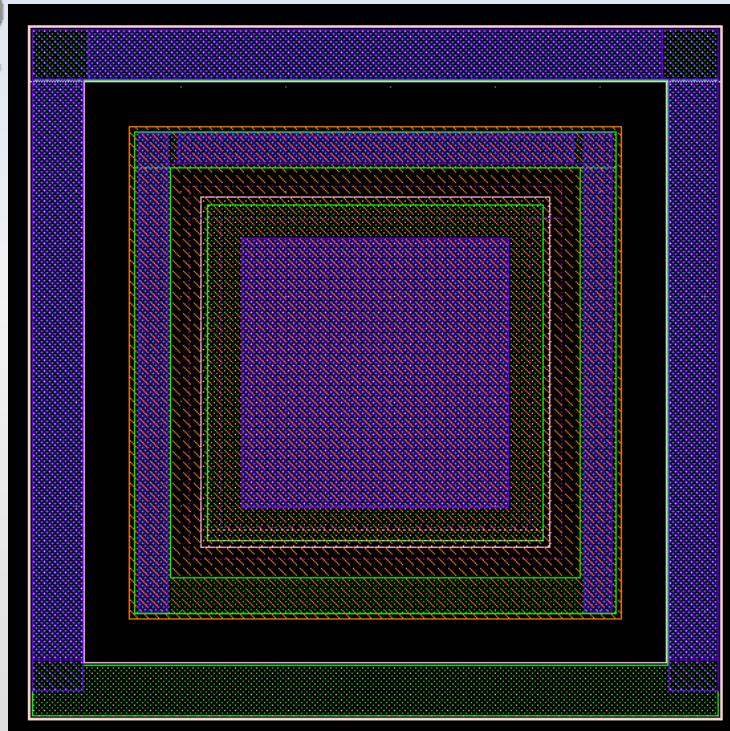


<b>ncrs</b>	Number of contact rows on inner source	2
<b>ncrd</b>	Number of contact rows on inner drain	1
<b>numcos</b>	Number of contacts per row on source	4
<b>pocos</b>	Distance contacts to gate on source	5.1e-08
<b>numcod</b>	Number of contacts per row on drain	5
<b>pocod</b>	Distance contacts to gate on drain	4.1e-08
<b>grStubs</b>	Guardring Segments	LTBR
	Netlisted Strap	0
	Presence of deep nwell	<input checked="" type="radio"/> 0
<b>wstrap</b>	Strap width	100n
<b>strap2rx</b>	Distance strap to RX	347.00n

- LTBR
- L
  - R
  - LR
  - T
  - B
  - TB
  - LTR
  - LBR
  - LTB
  - TBR
  - LTBR

Default value is TB





## 28FDSOI Vertical Bipolar



Introduction

Technology Overview

Design-Kit Contents

Roadmap

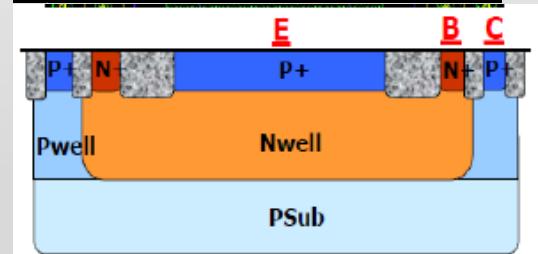
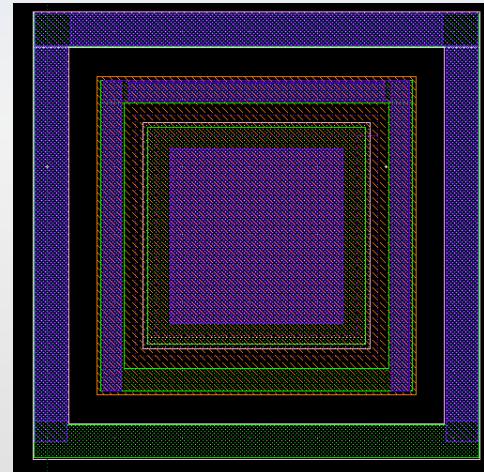
Support



- VPPNP device

- 1 geometry is recommended: **(3.2um)<sup>2</sup>**
  - Characterizations have only been made and ensured for the default specific geometry (3.2x3.2 um)
  - For the others, process does not guarantee the behavior of the device.
  - 10.24μm<sup>2</sup> is C032 dimensions, shrinked by 0.81x in C028 ( 0.83um<sup>2</sup> on silicon)

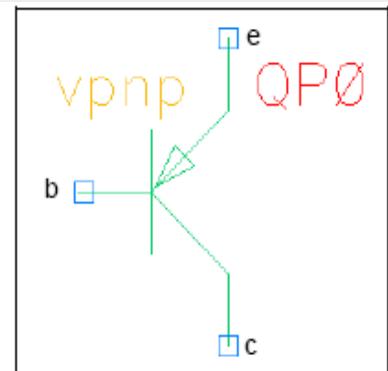
DEVICES	DEVICES IN OPUS	MODEL NAME	SOI/BULK
P+/Nwell/Psub b sign emitter bipolar E:3.2x3.2	vppnp	vppnp	BULK



Used in bandgap circuit application



- Introduction
- Technology Overview
- Design-Kit Contents
- Roadmap
- Support



- Netlisting:
  - Terminal order c b e
  - Netlisted as XQP
- This VPPNP model is accurate only for DC simulation.
- AC and capacitance parameters are given only for consistency in circuit simulation
- The default pCell is recommended.
  - Only nfinger=1 is supported today
- diodes included:
  - diodenwx, diodepnw
- Corners available
  - TYP, Imin, Imax, Bmin, Bmax
  - Stat ( MC simulation)

Device	Emitter Dimension ( $\mu\text{m}^2$ )	BETA	BVceo (V)	VBE (V)
VPPNP	3.2x3.2	0.9	9.75	0.762



Introduction

Technology Overview

Design-Kit Contents

Roadmap

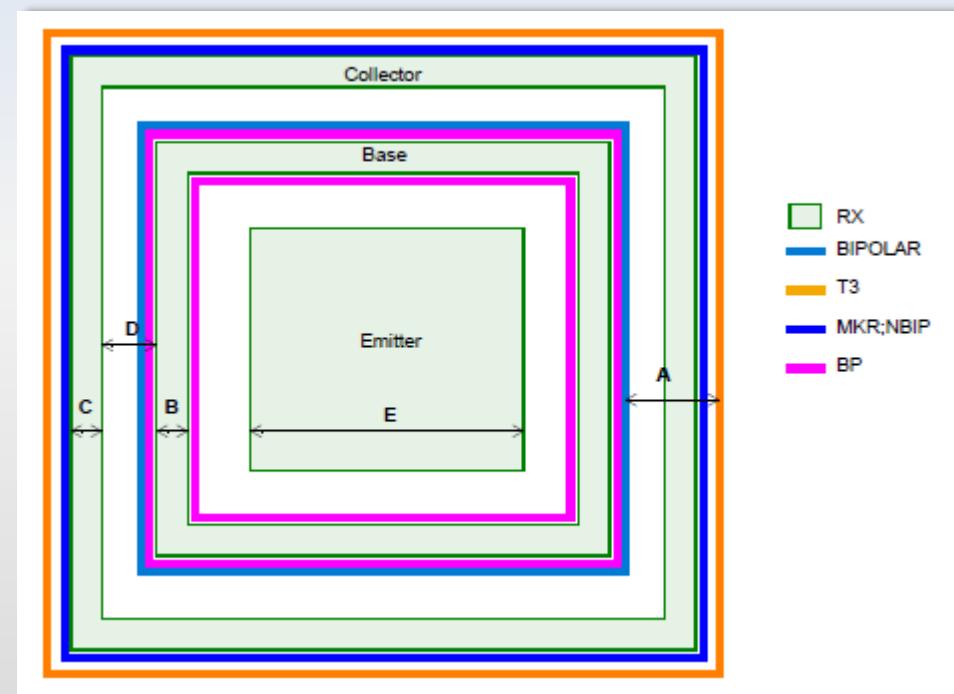
Support

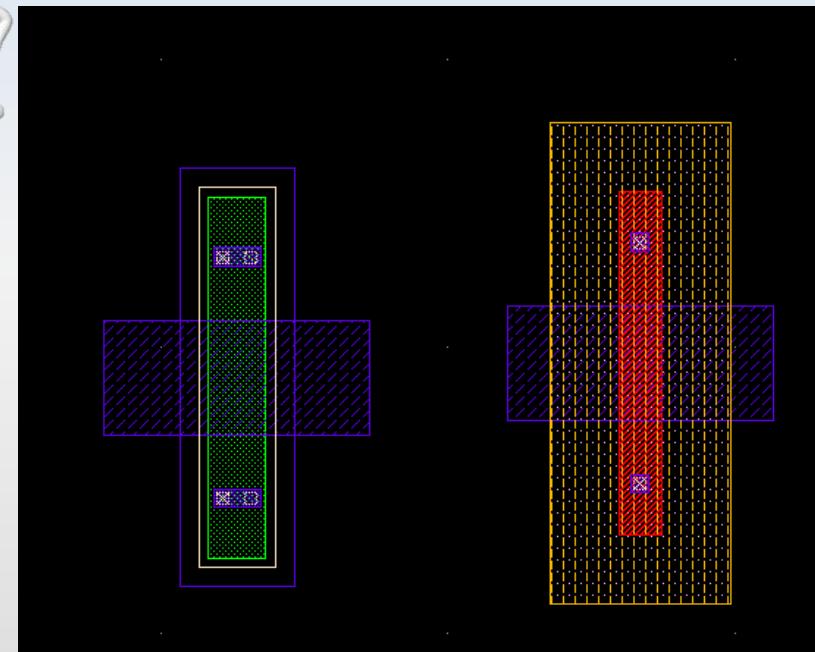


- VNPN device
  - other sizes than 3.2x3.2um and 6.4x6.4um are forbidden

DEVICES	DEVICES IN OPUS	MODEL NAME	SOI/BULK
P+/Nwell/P sub signe emitter bipolar E:3.2x3.2	vnpn	vnpn	BULK

Used in bandgap circuit  
application





## 28FDSOI Resistors

Guard Ring

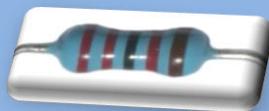


M1Route



PolyRoute





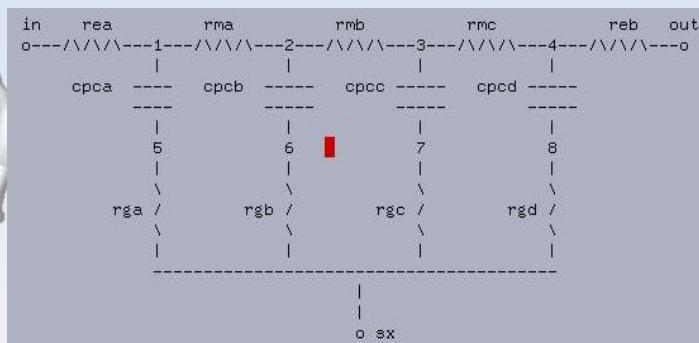
DEVICES	DEVICES IN OPUS	MODEL NAME	SOI / Bulk	Rs min (Ω/sq)	Rs typ (Ω/sq)	Rs max (Ω/sq)
Poly High precision non-silicided	opreres, opreres_b	opreres	SOI	872	1036	1199
P+ Poly non-silicided	oppres, oppres_b	oppres	SOI	390	439	490
P+ Poly non-silicided	oppres_lc, oppres_lc_b	oppres_lc	SOI	316	370	426
N+ Diffusion non-silicided	opndres, opndres_b	opndres	bulk	115	140	166
NW Resistor	nwres, nwres_b	nwres	bulk	528	749	977

The screenshot shows the Opus software interface with the following details:

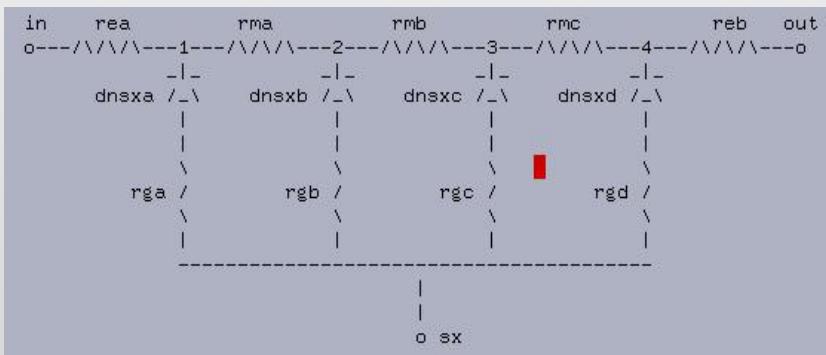
- Left Panel:** A tree view of libraries. The "cmos32lp" library is expanded, showing sub-libraries like "analogLib", "basic", "cdsDefTechLib", "cmos28\_emetro", and "cmos32lp".
- Middle Panel:** A list of components under the "RESISTORS" category. The list includes:
  - Do\_Not\_Use
  - ESD
  - ESD\_Hierarchical\_Cell
  - MOSFETS
  - Miscellaneous
  - RESISTORS
  - SRAM
  - Wire Models
- Right Panel:** A list of models for the selected "RESISTORS" component. The list includes:
  - nwres
  - nwres\_b
  - opndres
  - opndres\_b
  - oppres
  - oppres\_b
  - opreres
  - opreres\_b
- Bottom Right Panel:** A table with columns "View", "Lock", and "DM state". The "View" column lists "auCdl", "auLvs", "eldoD", "hspiceD", "layout", "spectre", and "symbol". The "Lock" and "DM state" columns are mostly empty.



## POLY resistor

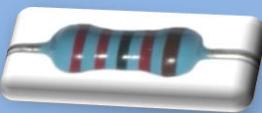


## Diffusion and N-WELL resistors

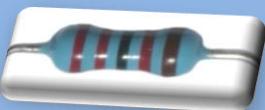


- Netlisting:

- Terminal order: p n b (for plus negative bulk)
- Netlisted as a subckt in eldo:
  - XR
- non linearity voltage support
- Model supports only rectangular shape with contact at each side of the resistor.



- Models include following features:
  - Multiple lumped element R-C sub circuit for better accuracy at higher frequencies (**Accurate models in ST**)
  - Separate body and end resistance temp coefficients
  - Parasitic capacitance between the resistor and substrate
  - Self heating and back-bias effects: activated by default
- CA resistance is included in the Rend distribution
- TYP, RMIN, RMAX and stat corners.
- Accurate models are selected by default.



Add Instance (on gnx894)

Library	cmos32lp	Browse	
Cell	opreres		
View	symbol		
Names			
Array	Rows 1	Columns 1	
Description	ion OP P+ Poly resistor		
Dimension by Geometry	<input type="checkbox"/>		
value	3.7664K Ohms		
Stripe Width	150n M		
Stripe Length	400n M		
Series Stripes	1		
Parallel Stripes	1		
Stripe Distance	0 M		
Sized Up			
Bulk	[@lSup :%:vss!]		
Temperature Deviation			
Substrate Resistance	50 Ohms		
Self Heating	1		
Backplane Designation	PW		
bp	3		
Guard Ring	<input type="checkbox"/>		
Create Dummies	<input type="checkbox"/>		
Routing Width	0 M		
Contact Rows	1		
<input type="button" value="Select Path Data"/> <input type="button" value="Hide"/> <input type="button" value="Cancel"/> <input type="button" value="Defaults"/> <input type="button" value="Help"/>			

CDS params	Models params	Parameter Description
value	r	Resistance value
Stripe width	w	Width of Polysilicon, RX or NW
Stripe length	l	Length
Series stripes	s	Number of series bars
Parallel stripes	pbar	Number of parallel bars
Temp deviation	dtemp	Device Temp. Rise above ambient
Self heating	sh	Self-heating switch
Backplane designation	bp (only for P+ op)	Backplane designation
	pCells params	Parameter description
Strip distance		Distance between stripes
Guard ring		Guard ring
Create dummies		Dummies
Routing width		Width of routing for stripes
Contact rows		Number of contact rows

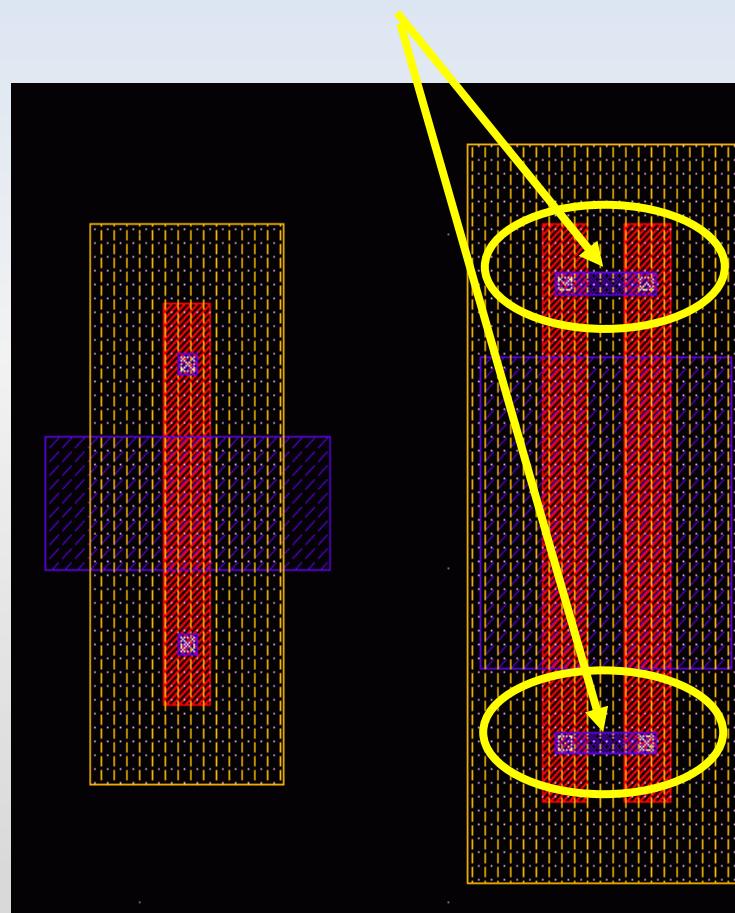


## Management of “par” and “s” for resistor

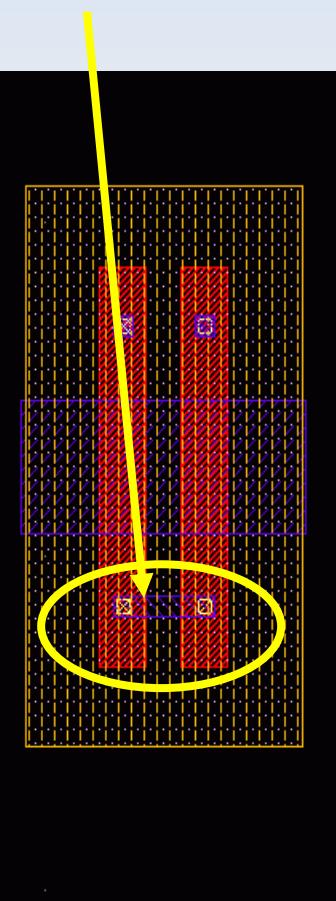
- “par”
  - number of paralleled POLY shapes
  - netlisted as “pbar”
- “ser”
  - number of POLY shapes in series
- This 2 cdf give the possibility to duplicate the resistive part of the resistance in 2 different ways.

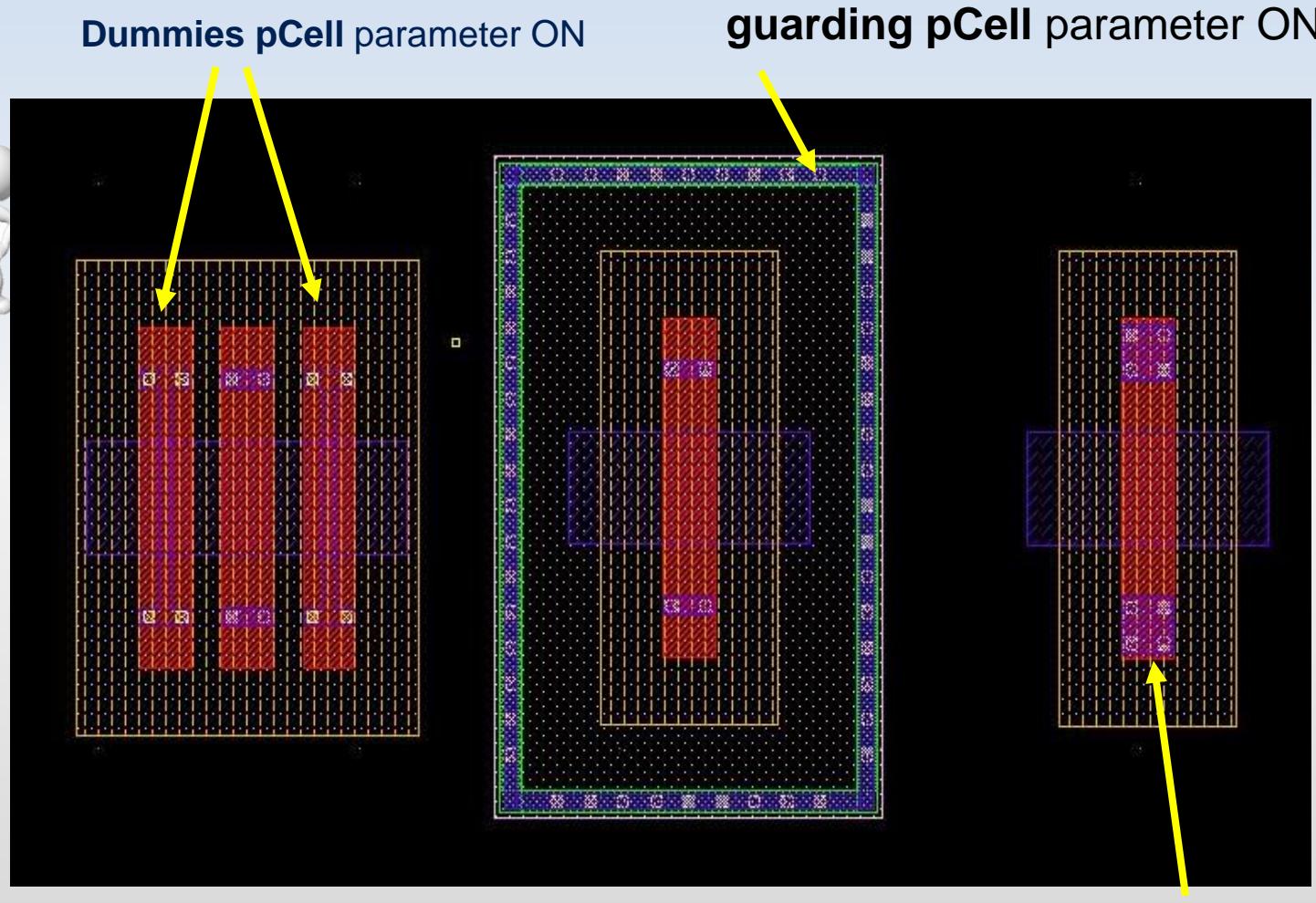


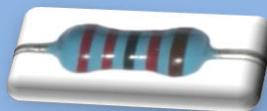
### Parallel Pcell parameter set to 2



### Series Pcell parameter set to 2





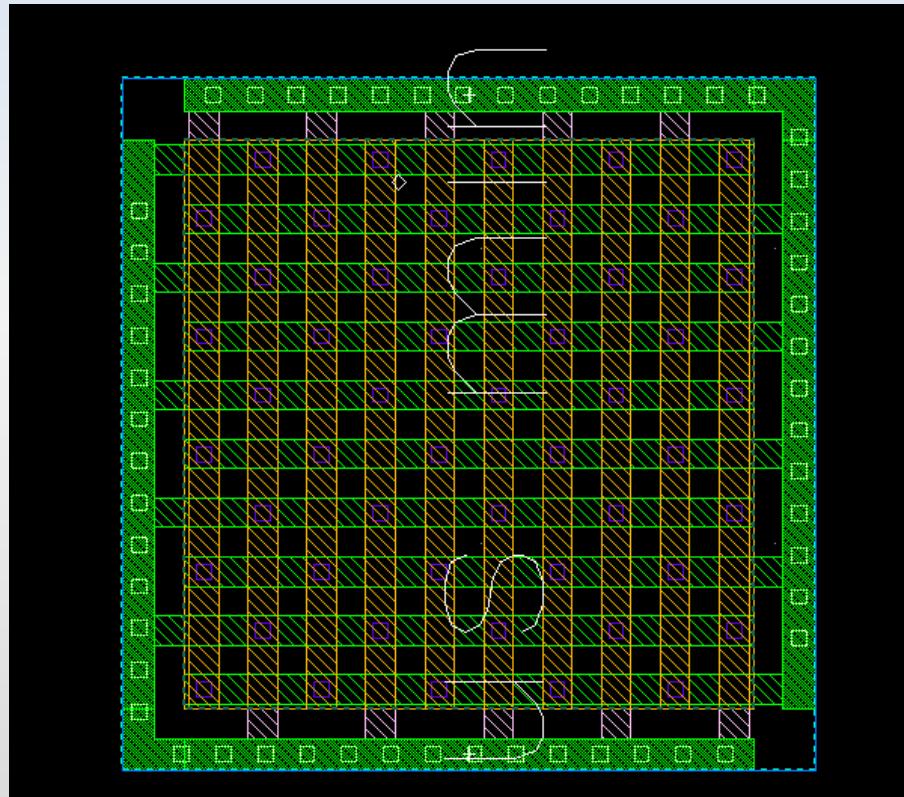


DEVICES	DEVICES IN OPUS	DK 8ML	DK 10ML
Metal1 to metal6	rm1x	X	X
Metal B1 & B2	rm2x	X	X
Metal IA & IB	rm8x	X	X
Metal LB	rmlb	X	X

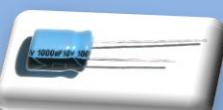
**r** : Total nominal resistance  
**w** : Width of one resistor stripe  
**I** : Length of one resistor stripe  
**metal** : Select the metal level  
**dimensionMode** : allow to define (value and I or w), or (w & I)

Description	Metal
Resistance Value	0.241
Width (m)	2e-6
Length (m)	2e-6
Metal position	M1
pre_layout_local	
Dimension by Geometry	

A dropdown menu is open under the 'Metal' entry, showing options M1, M2, M3, M4, M5, and M6. M1 is selected.



28-FDSOI Capacitors  
egncap/egpcap  
MOM capacitor  
MIM capacitor



**Edit Object Properties**

Apply To: only current instance

Show: system user CDF

Browse Reset Instance Labels Display

Property	Value	Display
Library Name	cmos32lp	off
Cell Name	egncap_b	value
View Name	symbol	off
Instance Name	C0	off

Add Delete Modify

CDF Parameter

Description	Value	Display
POLY N+ Nwell capacitor	1	off
Multiplicity	1	off
Dimension by Geometry	✓	off
Value at 1.8V	8.6449f F	off
Value (depletion) at -1.8V	2.8649f F	off
I	1u M	off
w	1u M	off
Number of Gates	1	off
Number of RX Shapes	1	off
Resistance	-2 Ohms	off
Inductance	-2 H	off
Guard Ring	✓	off
M1 Routing?	✓	off
M1 Rails?	✓	off
Create Pins w/o Routing?	✓	off

Select Rule Sets

Rule Sets	DFM_RULES	Display
Enable ROD Objects?	✓	off
Safe Operating Area	0 1	off
Substrate Resistance	50	off

OK Cancel Apply Defaults Previous Next Help

Netlisting Params	Parameter Description
w	Width of the capacitor (diffusion width)
l	Length of the capacitor (polysilicon width)
nf	Number of gates per individual RX diffusion
nrep	Number of individual RX diffusion shapes
setind	switch to use internal calculation for M1 wiring inductance or user-defined value
setres	switch to use internal calculation for M1 wiring resistance or user-defined value
m	Number of devices in parallel
soa	Check if the condition of use are in safe area
pCells params	
guardring	guardring
M1 routing	M1 routing present in pCell
M1 rails	M1 rails creation for pins
Create pins wo routing	Pins creation without routing



Introduction

Technology Overview

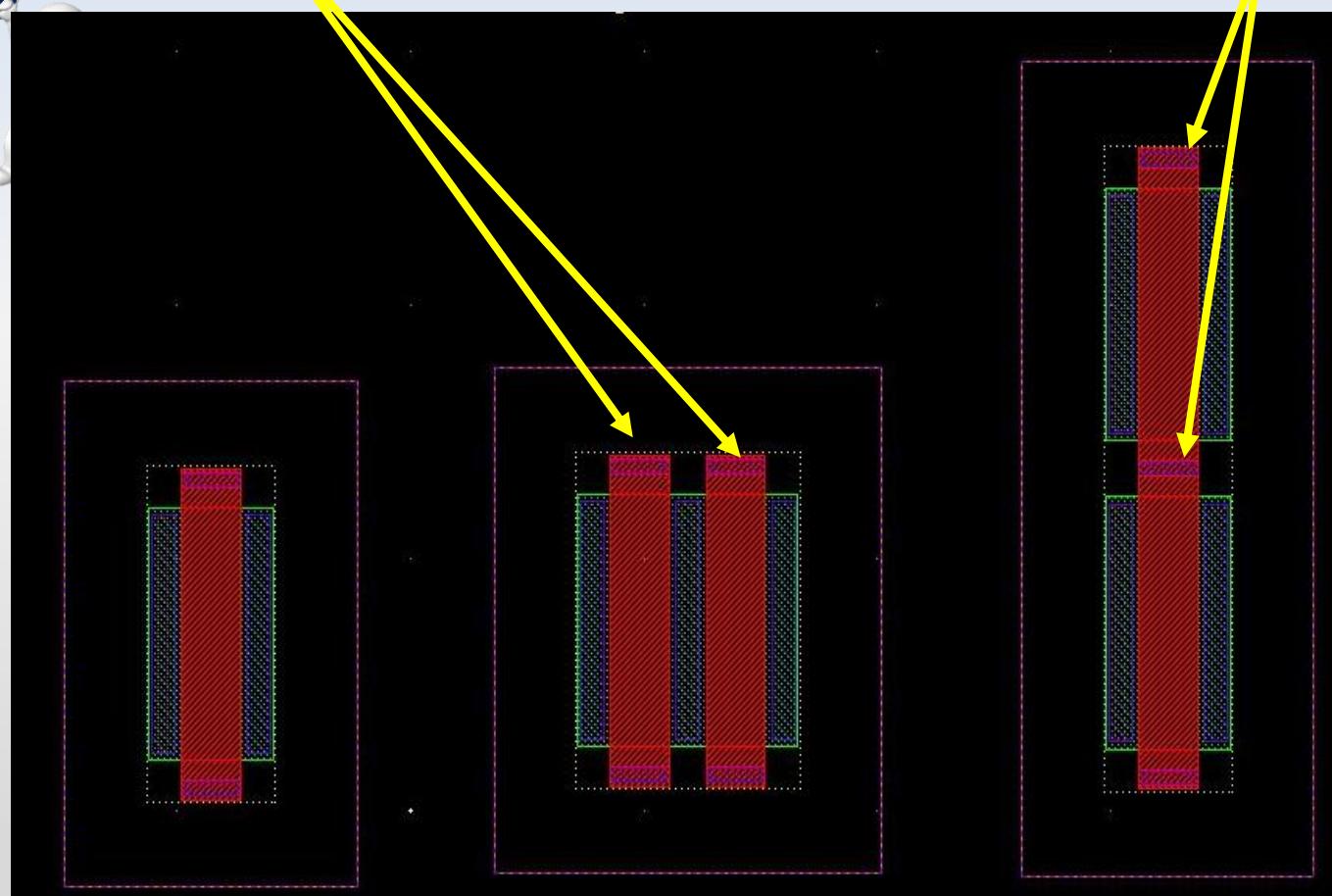
Design-Kit Contents

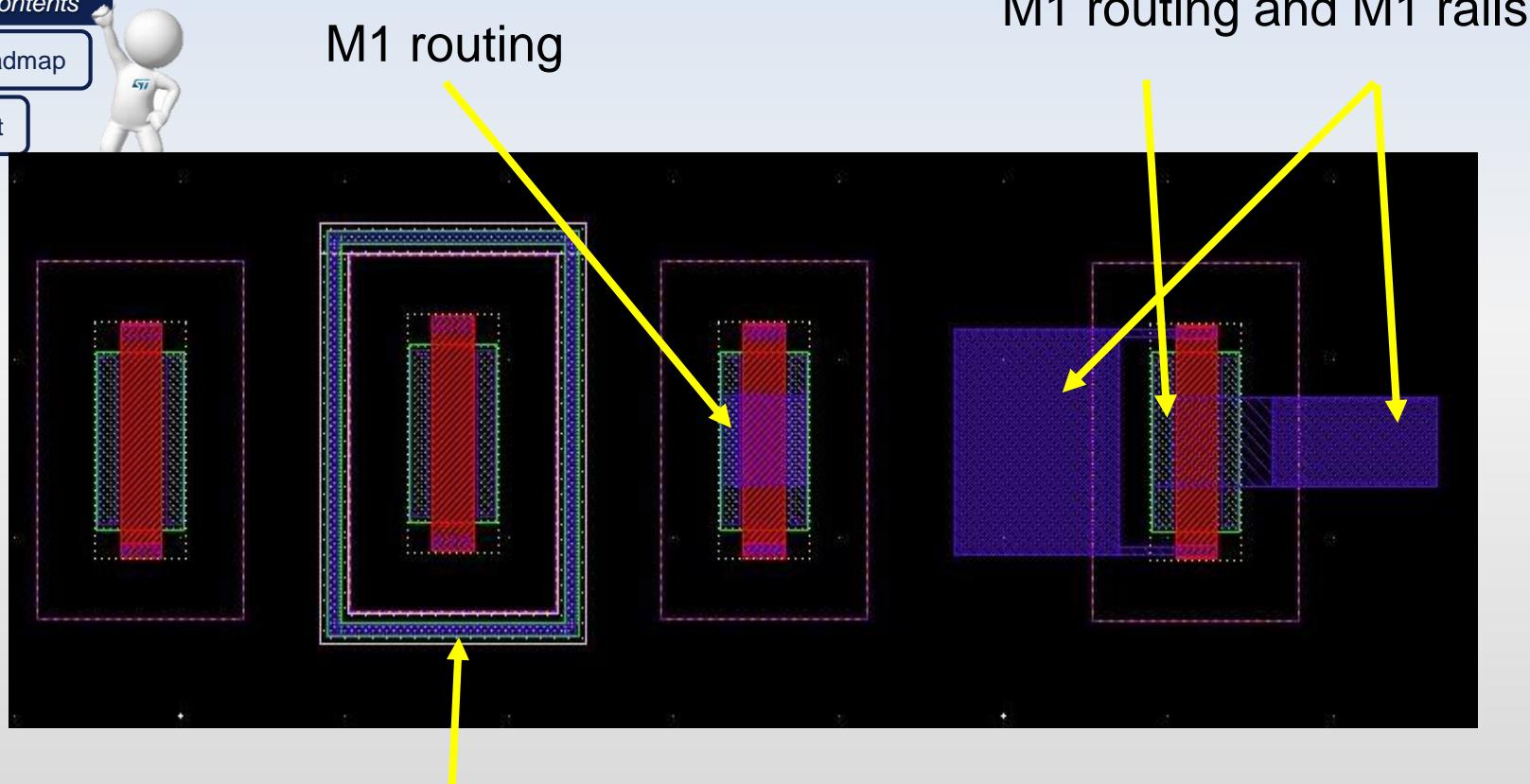
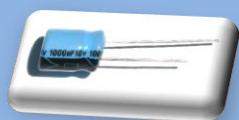
Roadmap

Support

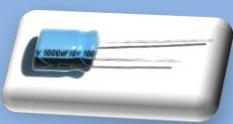
Number of gates set to 2

Number of RX shapes set to 2





Guardring



Introduction

Technology Overview

Design-Kit Contents

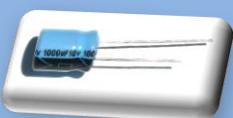
Roadmap

Support



- Models include following features:
  - Gate leakage
- Models don't include:
  - Parasitic inductance introduced by the metal lines
  - Temperature variation of the gate leakage

parasitics included in model	NW-to-substrate diode
	resistance of pcell wiring when setres=-2
	Fringe cap between pcell wiring and diffusion
	Fringe cap between pcell wiring and STI
	metal-to-metal capacitance due to pcell wiring



- Same free capacitor using up to M1-M6 fingers metal layers, scalable.
- Same models offer:
  - 2 pins MOM without Poly/active shield (std & acc)
  - 4 pins MOM with Poly/active shield (std & acc)
  - Preliminary models
  - Corner variation depends on number of levels used (spread is higher for small nb of levels)

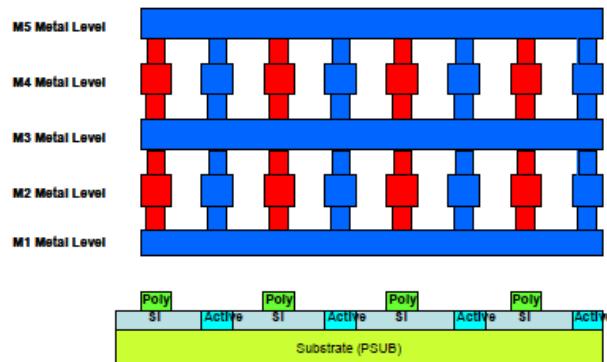
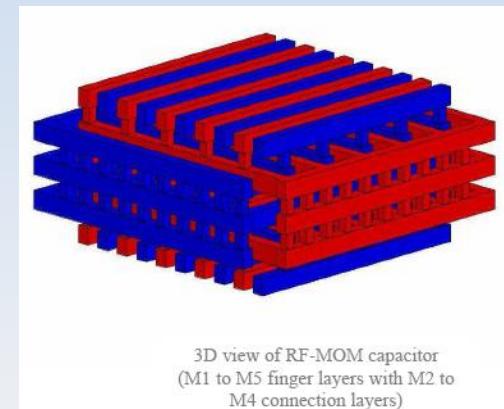


Figure 2: Cross section of MOM capacitor (Shield + M1 to M5 layers)

M1-M5 RF MOM with VIA	Pitch/Vmax	C028FDSOI ( M1-M5 value) ...
C (fF/ $\mu\text{m}^2$ )	100nm/1.15V 160nm/1.98V 200nm/1.98V	6.45fF/ $\mu\text{m}^2$ 2.59fF/ $\mu\text{m}^2$ 1.76fF/ $\mu\text{m}^2$
Raccess (ohm)	100nm/1.1V 160nm/1.15V 200nm/1.98V	~1 ~0.95 ~0.93

The poly/active shield under the cmom  
→ No extra parasitic capacitance from the bulk

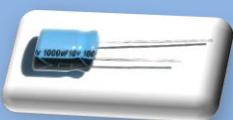
Different options available M1-M2, M1-M3 ...  
Density decrease without via (~ -15%)



DEVICES	DEVICES IN OPUS	MODEL NAME
RFMOM with OD/PO shield	cmom_6U1x_2U2x_2T8x_LB_wo_via_sh	cmom_6U1x_2U2x_2T8x_LB_wo_via_sh
		cmom_6U1x_2U2x_2T8x_LB_wo_via_sh_acc
	cmom_6U1x_2U2x_2T8x_LB_sh	cmom_6U1x_2U2x_2T8x_LB_sh
		cmom_6U1x_2U2x_2T8x_LB_sh_acc
2 pins RFMOM	cmom_6U1x_2U2x_2T8x_LB_wo_via_2p	cmom_6U1x_2U2x_2T8x_LB_wo_via_2p
		cmom_6U1x_2U2x_2T8x_LB_wo_via_2p_acc
	cmom_6U1x_2U2x_2T8x_LB_2p	cmom_6U1x_2U2x_2T8x_LB_2p
		cmom_6U1x_2U2x_2T8x_LB_2p_acc

DEVICES	DEVICES IN OPUS	MODEL NAME
N+ Poly / GO2 28A / NWELL	egncap	egncap
	egncap_b	
P+ Poly / GO2 28A / PWELL	egpcap	egpcap
	egpcap_b	

Hybrid ( bulk ) devices

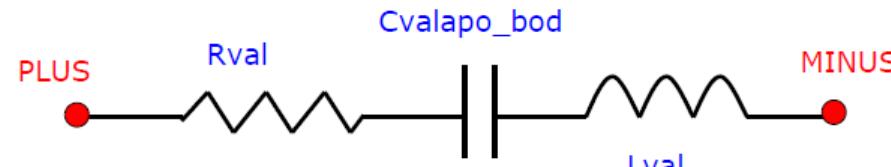
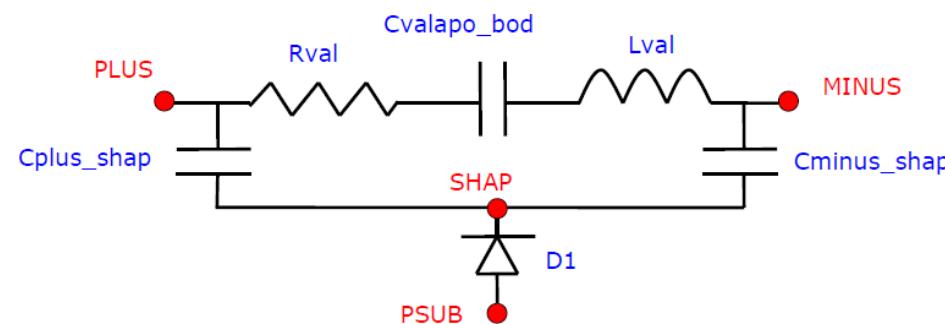


Introduction

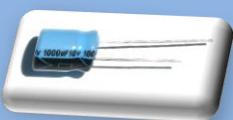
Technology Overview

Design-Kit  
Contents

Standard models are C model based, whereas the \_acc models ( for accuracy ) are RLC model based.

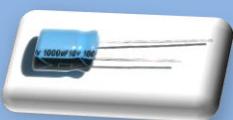

**cmom\_6U1x\_2U2x\_2T8x\_LB\_2p\_acc**

**cmom\_6U1x\_2U2x\_2T8x\_LB\_sh\_acc**

More detail in the CMOM\_with\_&\_wo\_via.pdf file in the documentation

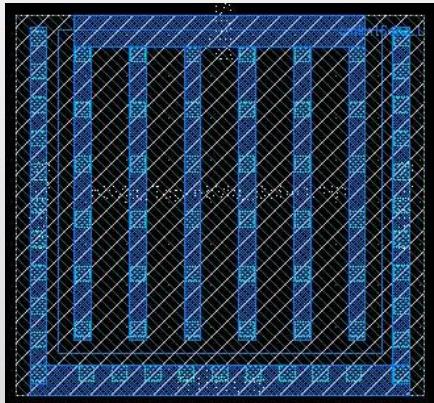
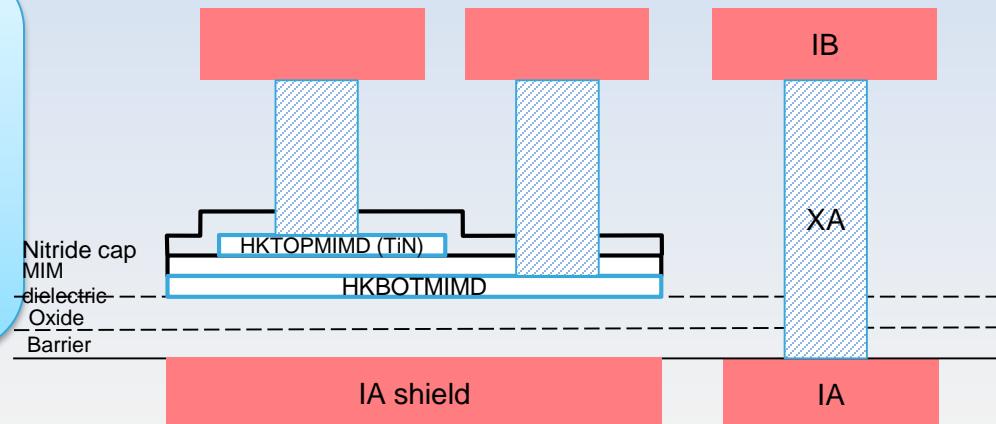


## Planar decoupling MiM capacitor (DECAP)

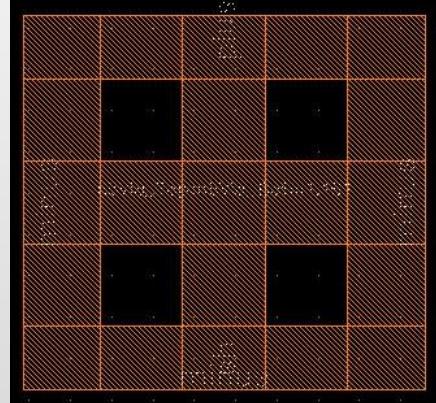
- targeted for nominal power supply voltages of 1.1V
  - max power supply of 1.155V
- located between the first and the second 8x metallization levels (IA and IB respectively).
  - The capacitance is connected through the via (XA) and metal level above the MIM (IB).
- Typical density 20fF/um<sup>2</sup>
- Leakage (1.2V/125C) 3\*10e-2 A/cm<sup>2</sup>.
- ST/Crolles dielectrics used : Ta<sub>2</sub>O<sub>5</sub> (16.2 fF/um<sup>2</sup> +/-15 )



- Planar architecture
- Capacitor between IA & IB
- 3 additional masks for MIM option : BOTMIM, TOPMIM, SPMIM
- Connection with XA
- No constraint on IA or IB routing & placement

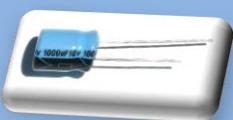


cmim16acc layout  
Connection to IB with XA vias



cmim16acc\_sh IA shield pattern

- Shielded capacitor available
- Avoid uncontrolled parasitic capacitance with lower levels (metals, poly, substrate)
- Slotted structure to respect density rules

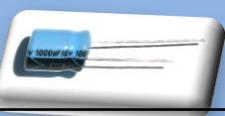


DEVICES	DEVICES IN OPUS	MODEL NAME
RF MIM capacitor	cmim16acc	cmim16acc
		cmim16acc_acc
RF MIM capacitor 2 pins	cmim16acc_2p	cmim16acc_2p
		cmim16acc_2p_acc
RF MIM capacitor shield	cmim16_acc_sh	cmim16_acc_sh
		cmim16_acc_sh_acc

Parameters	Specifications		
	LOW	TYP	HIGH
Capacitance (fF/ $\mu\text{m}^2$ )	-15% (13.8)	16.2	+15% (18.6)
Leakage current @1.1V (A/cm <sup>2</sup> ) @25°C			<10 <sup>-5</sup>
Leakage current @1.1V (A/cm <sup>2</sup> ) @125°C			<2.10 <sup>-3</sup>
Voltage (V) for 4 years lifetime (0.1% failure, S=10mm <sup>2</sup> , 105°C)	< 1.4 V		
Voltage (V) for 10 years lifetime (0.1% failure, S=10mm <sup>2</sup> , 125°C)	< 1.155 V		

- 2 pin model definitions (2 pins; 3pins)
- 2 simulation levels : name & name\_acc
- Models functionalities :
  - C corners
  - SOQ limits
  - Post layout simulation (not for 2 pins cmim)
  - Mismatch
  - Monte Carlo
- Accurate models functionnalities:
  - R access
  - Linearity coefficients \*
  - Leakage \*
  - Relaxation \*

\* No cmos28FDSOI silicone based values (cmos065)



Introduction

Technology Overview

Design-Kit Contents

Roadmap

Support

Netlisting Params	Parameter Description
w	Width of the capacitor (diffusion width)
l	Length of the capacitor (polysilicon width)
nf	Number of gates per individual RX diffusion
nrep	Number of individual RX diffusion shapes
setind	switch to use internal calculation for M1 wiring inductance or user-defined value
setres	switch to use internal calculation for M1 wiring resistance or user-defined value
m	Number of devices in parallel
soa	Check if the condition of use are in safe area
pCells params	
guardring	guardring
M1 routing	M1 routing present in pCell
M1 rails	M1 rails creation for pins
Create pins wo routing	Pins creation without routing

Edit Object Properties (on gnx894)

Apply To: only current instance  
Show: system user CDF

Browse Reset Instance Labels Display

Property	Value	Display
Library Name	cmos32lp1	off
Cell Name	ncap_b	off
View Name	symbol	off
Instance Name	c0	off

Add Delete Modify

CDF Parameter	Value	Display
Description	Thin Oxide NCAP	off
Dimension by Geometry	<input checked="" type="checkbox"/>	off
value	20.4955f F	off
value (depletion)	1.44434f F	off
l	1u M	off
w	1u M	off
Number of Gates	1	off
Number of RX Shapes	1	off
Temperature Deviation		off
Sized Up		off
Substrate Resistance	50 Ohms	off
Resistance	-2 Ohms	off
Inductance	-2 H	off
Guard Ring	<input type="checkbox"/>	off
M1 Routing?	<input checked="" type="checkbox"/>	off
M1 Rails?	<input checked="" type="checkbox"/>	off
Create Pins w/o Routing?	<input checked="" type="checkbox"/>	off

Select Rule Sets

Rule Sets	Value	Display
Enable ROD Objects?	<input type="checkbox"/>	off
Multiplicity	1	off

OK Cancel Apply Defaults Previous Next Help



- No model available
- Only for LVS

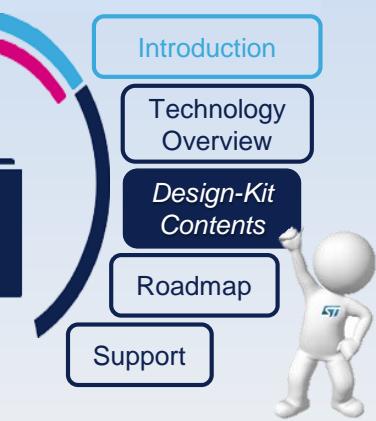
DEVICES	DEVICES IN OPUS	DK 8ML	DK 10ML
Metal1 to metal6	cfrm1x	X	X
Metal B1 & B2	cfrm2x	X	X
Metal IA & IB	cfrm8x	X	X
Metal LB	cfrmlb	X	X

I : Length of the capacitor

fs : Metal spacing

metal : Select the metal level

Length (m)	0.05e-6
Finger space (m)	0.05e-6
Metal position	<div style="border: 1px solid black; padding: 2px; display: inline-block;">M1</div> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-left: 10px;">M1</div> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-left: 10px;">M2</div> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-left: 10px;">M3</div> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-left: 10px;">M4</div> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-left: 10px;">M5</div> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-left: 10px;">M6</div>



## 28FDSOI Diodes

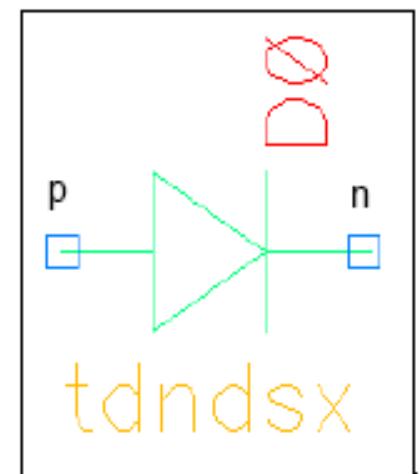


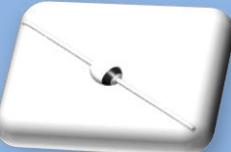
DEVICES	DEVICES IN OPUS	MODEL NAME
GO1 N+/Pwell	tdndsx	tdndsx
GO1 P+/Nwell	tdpdnw	tdpdnw
GO2 N+/Pwell	egtdndsx	egtdndsx
GO2 P+/Nwell	egtdpdnw	egtdptnw

tdndsx	p ( psub ) and n ( n+ )	antenna protection for mos in pwell : nRVT and pLVT
tdpdnw	p ( BP ) and n ( nwell )	antenna protection for mos in nwell : pRVT but not nLVT 

See next

- G02 devices : same as G01 + EG layers
  - Used with G02 devices
- Diode models include junction capacitance and forward bias current parameters





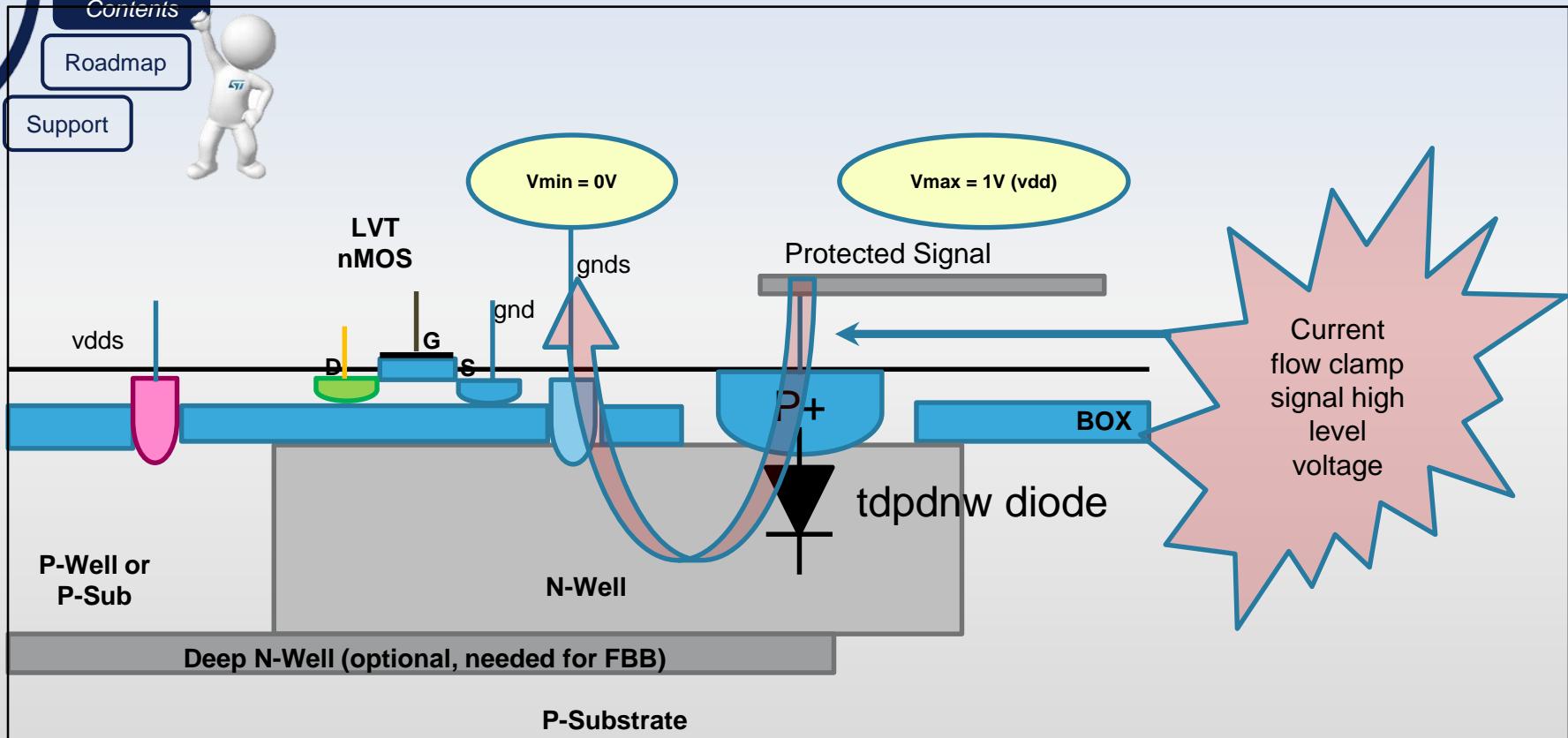
Introduction

Technology Overview

Design-Kit Contents

Roadmap

Support





Introduction

Technology Overview

Design-Kit Contents

Roadmap

Support



- In Front-End, area/peri and width/height can be used
  - Skill callbacks exist to manage indifferently the 2 ways
  - Only area/peri are netlisted
- In layout, only width/height has an impact on pCell
  - If area/peri is used, default pCell values are used!

Parameter	Prompt	Unit	Description
area	Area	m <sup>2</sup>	Area of the diode.
perimeter	Perimeter	m	Perimeter of the diode.
trise	Device Temperature Deviation	°C	Deviation of device temperature from ambient
width	Width	m	PCell parameter: Width of diode
height	Height	m	PCell parameter: Height of diode

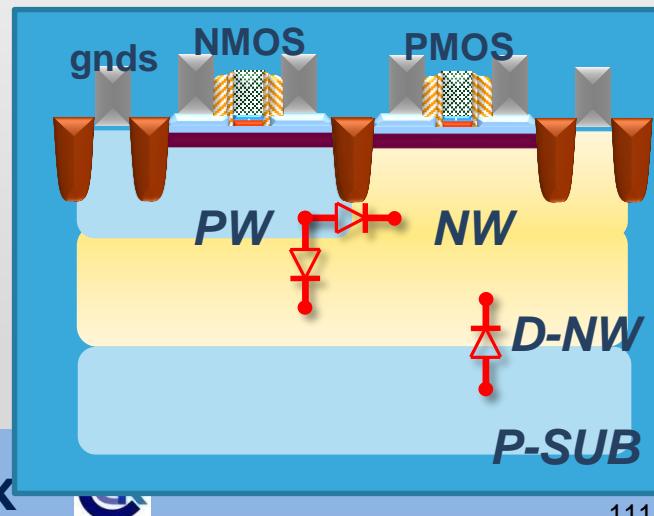


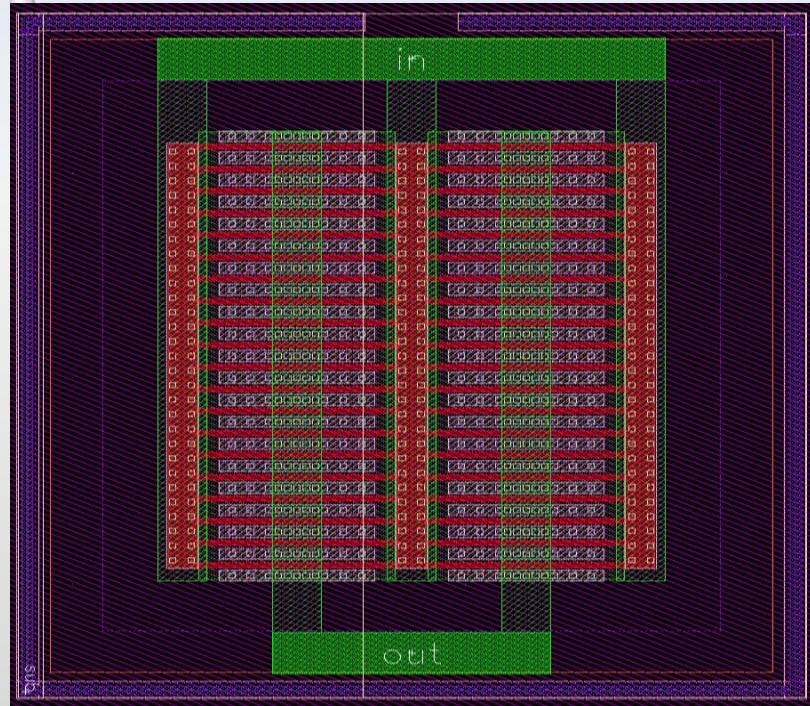
- Introduction
- Technology Overview
- Design-Kit Contents**
- Roadmap
- Support



DEVICES	DEVICES IN OPUS / MODEL NAME
Niso/Psub	diodetwx_lvs, diodetwx
Pwell/Niso	diodepwtw_lvs, diodepwtw
Nwell/Psub	diodenwx_lvs, diodenwx
N+ to Substrate	diodenx
P+ diff to Nwell	diodepnw
EG N+ to Substrate	egdiodenx
EG P+ diff to Nwell	egdiodepnw

- Parasitic diodes have no layout pCells and some are not verified by LVS (\_lvs in the device name is for devices with negative bias).
- These devices can be used in 2 ways:
  - Manually placed in schematic for parasitic effect estimation
  - Placed by the parasitic extraction flow in the extracted view

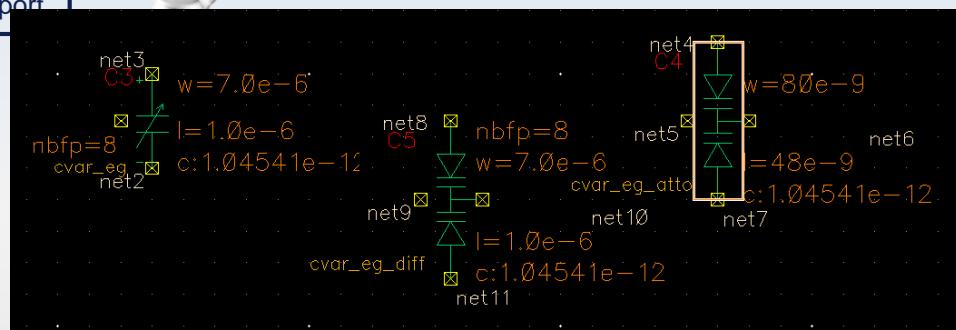




## 28FDSOI Varactors

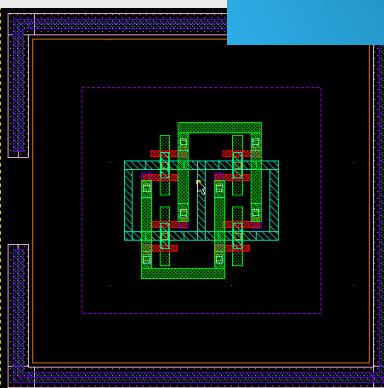
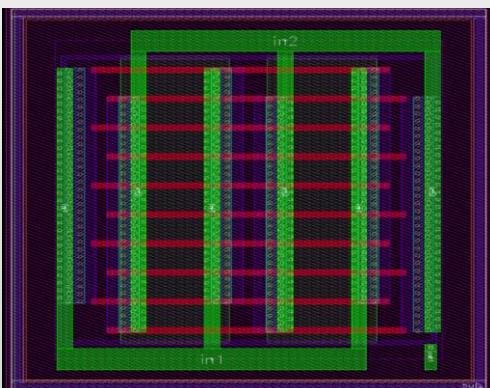
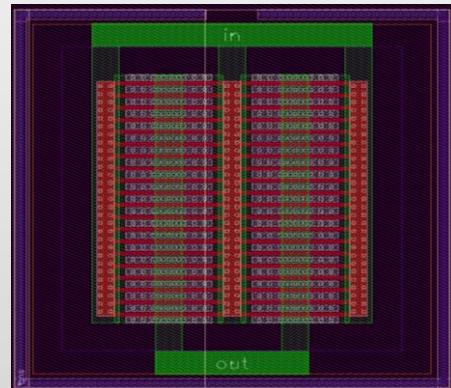


DEVICES	DEVICES IN OPUS	MODEL NAME
Single EG NMOS Varactor	cvar_eg	cvar_eg
Differential EG NMOS Varactor	cvar_eg_diff	cvar_eg_diff
Attofarad EG NMOS Varactor	cvar_eg_atto	cvar_eg_atto



N+poly/N-Well varactors

No additional mask / processing



Hybrid (bulk ) devices

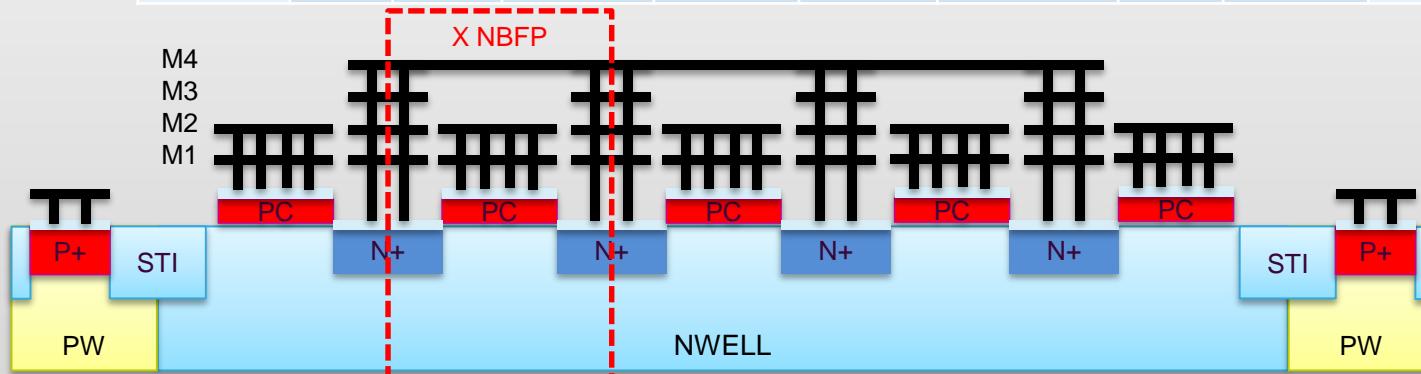
Varactor single layout

Varactor diff. layout

Varactor atto layout



Varactor MOS		Cap. (F)	Gate Length ( $\mu\text{m}$ )	Gate Width ( $\mu\text{m}$ )	Nbfp	Ncell	Bias	Tuning Ratio	Worst Case & Min/max	Model frequency validity
GO2 single	Min	20 f	0.048	1	1	1	-1,8V	1.5	Yes	110 GHz
	Max	10 p	2	10	50	10	1,8V	3		
GO2 diff	Min	20 f	0.049	1.5	1	1	-1,8V	1.5	Yes	110 GHz
	Max	10 p	2	10	50	5	1,8V	2		
			Length ( $\mu\text{m}$ )	Finger Width ( $\mu\text{m}$ )	Nbline	Nbcolumn				
GO2 attofarad	Min		0.048	0.08	1	1				
	Max		0.048	0.5	10	10				



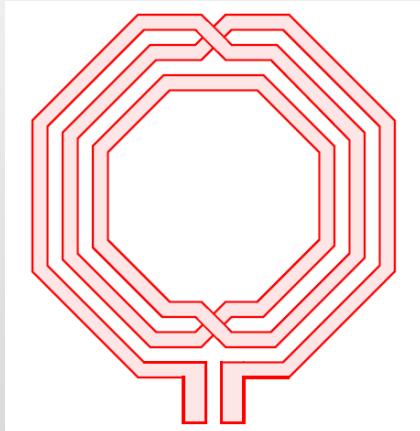
Cross section of the N+ poly/NWELL MOS varactor Pcell



## 28FDSOI Inductors

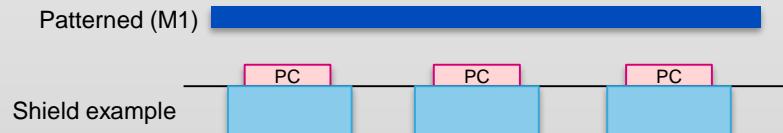
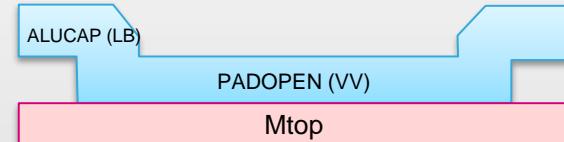


DEVICES	DEVICES IN OPUS	MODEL NAME
Low Value High Q inductor	ind_lohq_<metal_option>	ind_lohq_<metal_option>
Differential Low Value High Q inductor	Inddif_lohq_<metal_option>	inddif_lohq_<metal_option>
Low Value High Q High Performance inductor	ind_lohq_high_perf_<metal_option>	ind_lohq_high_perf_<metal_option>
Differential Low Value High Q High Performance inductor	Inddif_lohq_high_perf_<metal_option>	inddif_lohq_high_perf_<metal_option>
High Q inductor	ind_hq_<metal_option>	ind_hq_<metal_option>
Differential High Q inductor	Inddif_hq_<metal_option>	inddif_hq_<metal_option>



Inductor Top View

Imported from 28lp technology. Same behavior expected

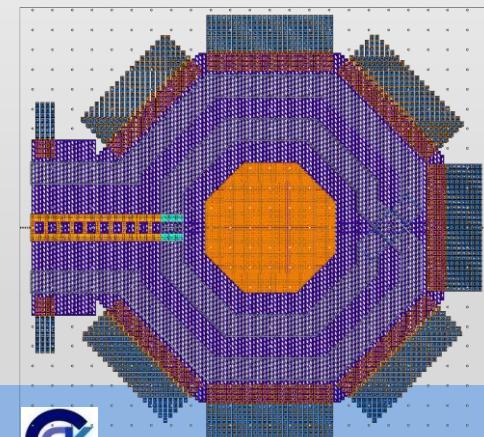
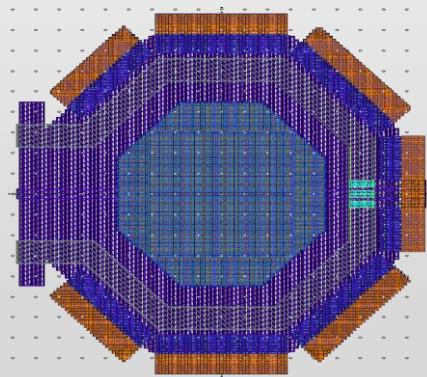


Inductor x-section



Instance parameter	Inductor LoHQ	Inductor HQ
Nbturns	Fixed to 1	2 – 3
d (internal diameter)	44 – 440 µm	88 – 440 µm
W (coil width)	5.5 – 32,99 µm	11 – 32.99 µm
Is (inductance value)	0.062 – 1.112 nH	0.549 – 7.794 nH
mpout (middle point output orientation)	short / long	short / long
wmp (middle point width)	5.5 - 41.16 µm	11 - 63.52 µm

Stack	Inductor LoHQ	Inductor HQ
	Coil in IB+LB middle point in M2 to M6	Coil in IB+LB middle point in M2 to IA
	Pattern shield in M1	Pattern shield in M1



# DESIGN-KIT CONTENTS

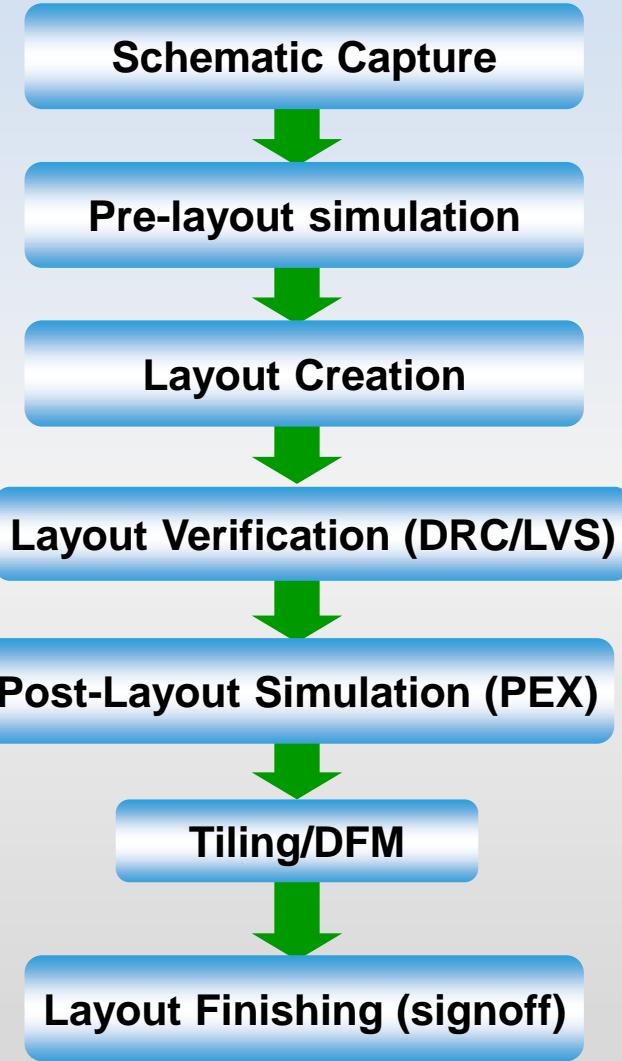
- Analog Design Flow

## PART III

CMOS & Derivative PDK



- A **PDK** is basically a collection of modules & technological files like spice models, physical layout verification decks including device-library with CAD flow oriented files adapted to a target and given technology
- **ST PDKs** also enable the **glue** between the CAD tools, providing a **design flow** with graphical interfaces and methodologies in order to ease and speed-up the design activity to be First-Time-Silicon-Success.
- **ST PDKs** support broad range of major EDA (Electronics Design Automation) companies in the open CAD market such as :



Introduction

Technology Overview

Design-Kit  
Contents

Roadmap

Support



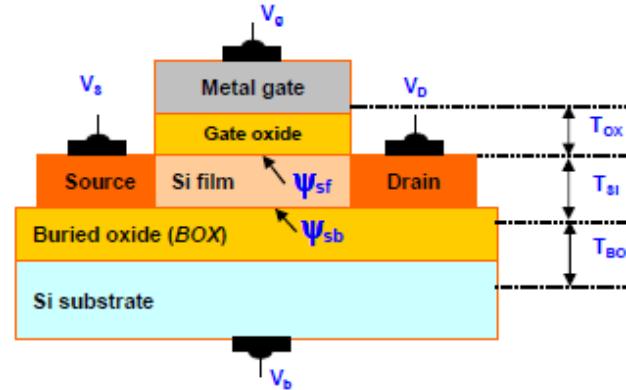
Cadence framework is to be used with Design Kits

Analog Flow uses EDA tools from several CAD vendors:





- UTSOI2 is used to describe 28FDSOI MOSFETs
  - ST – LETI Co-development



- Bulk-referenced model / PSP based
- Equations adapted from PSP formalism to specific FDSOI topology
  - 4-terminal transistor model + facultative 5th thermal node
  - ELDO, HSPICE, XA, SPECTRE, ADS, GoldenGate, AFS, finesim



# Maturity

ST Models have different maturity level, device by device

- Devices Maturity available in  
\$DKITROOT/doc/TECHNOLOGY/DEVICE\_LIST



## Production

**Model revision format : 2.x**

mat 30

Based silicon model representative of mat 30 technology



## Pre-production

**Model revision format : 1.x**

mat 20

Based silicon model representative of mat 20 technology



## Preliminary

**Model revision format : 0.x**

mat 10

Based silicon model representative of mat 10 technology

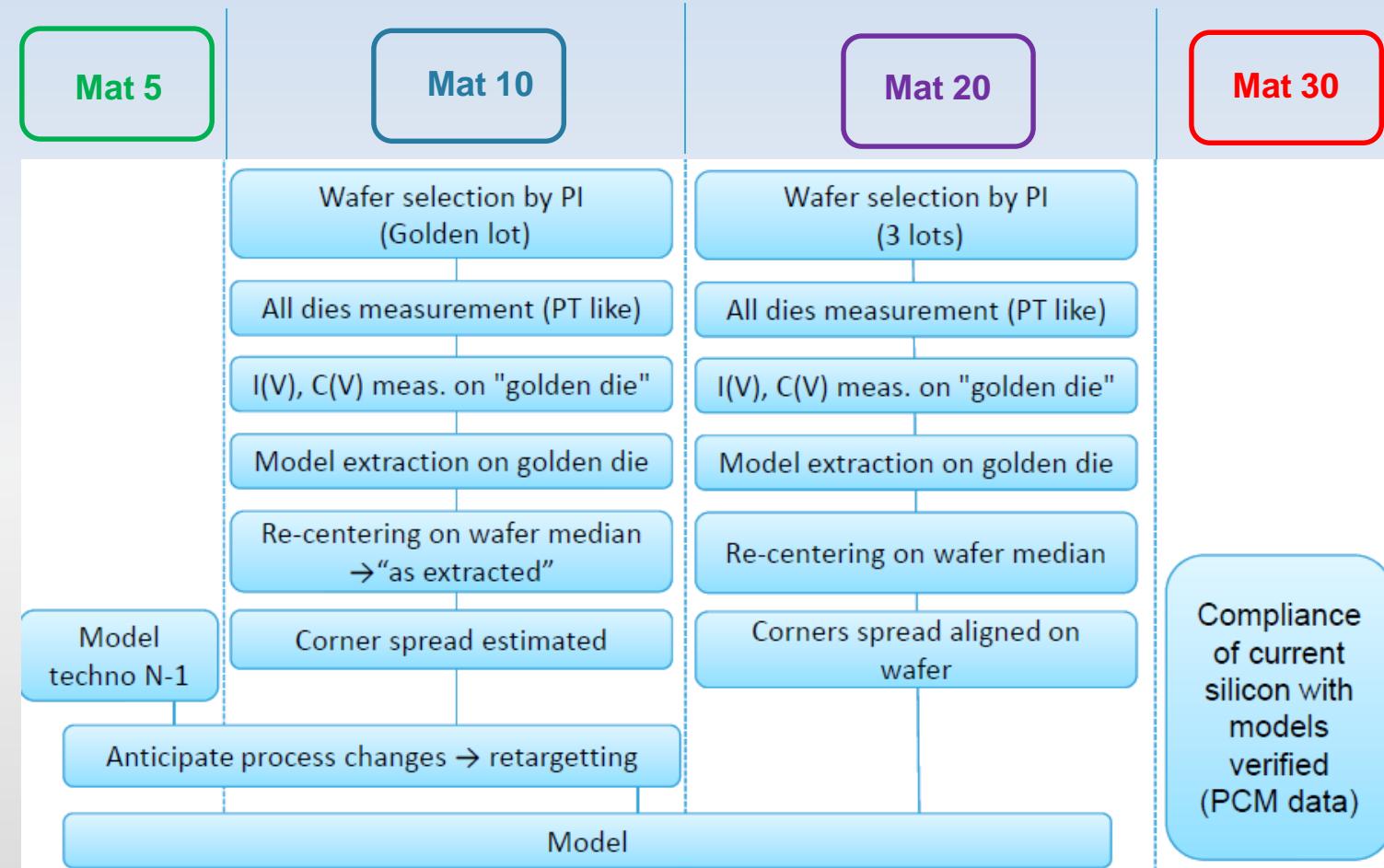


## Tentative

**Model revision format : 0.0x**

mat 5

Prediction models based on early silicon results, TCAD simulation and previous technology models



Introduction

Technology Overview

Design-Kit  
Contents

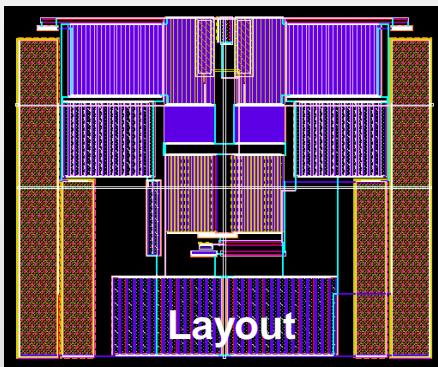
Roadmap

Support



*Does my layout fulfill  
the Design Rule Manual requirements?*

DRC, Design Rule Check, will tell me!

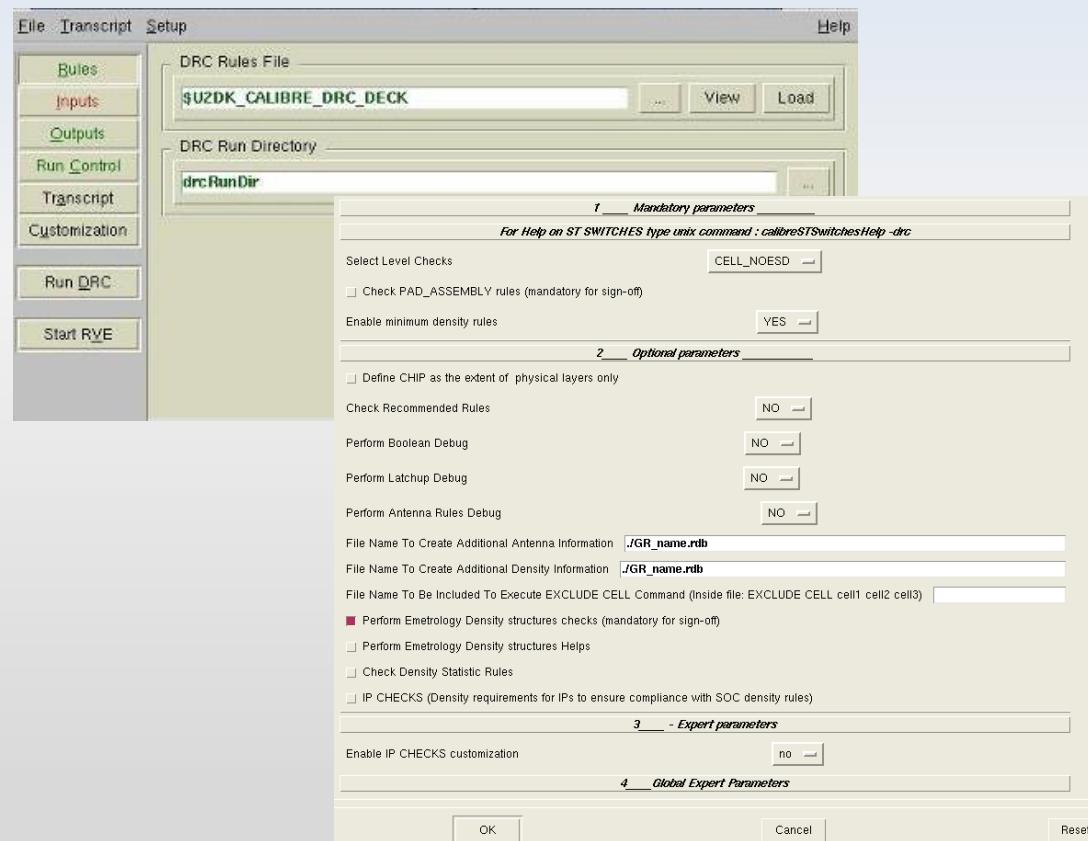


**Process Rules**





- Use calibre
  - launch calibre gui: `calibre -gui -drc`



Introduction

Technology  
OverviewDesign-Kit  
Contents

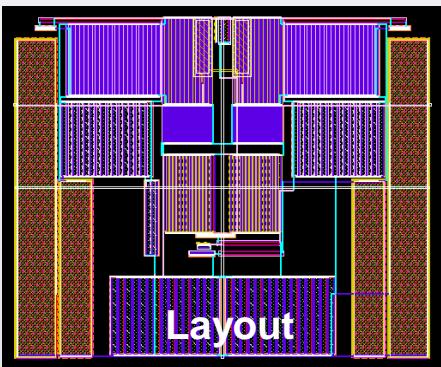
Roadmap

Support



*Does my preliminary layout fulfill  
the Design Rule Manual requirements ?*

**PVS DRC** will help me!

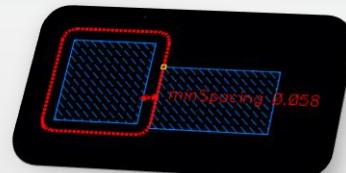


**Process Rules**

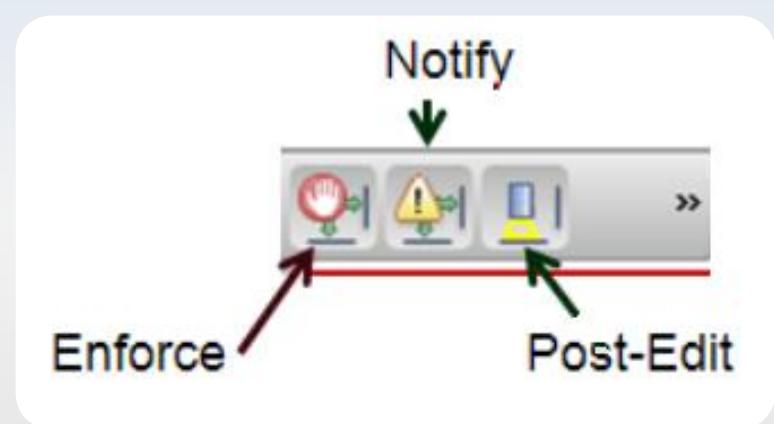
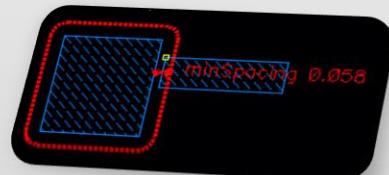


- Run PVS on In Design mode
  - PVS is activated by default in your environment
  - DRD Edit toolbar visible with 3 modes

**Enforce mode** : cannot draw if rule not respected



**Notify mode** : drawing possible if rule not respected



**Post-Edit mode** : Errors are output once you have modifying an existing layout.



File Preferences Toolbars Help **cadence**

Run Data Rules Input Output DRC Options

**Rules**

Tech&Rules Configurator  Use Configurator

Input Technology GuiConfig is used

**Config Options**

1 \_\_\_\_\_ Mandatory parameters \_\_\_\_\_

Select Level Checks CHIP\_NOESD

Check PAD\_ASSEMBLY rules (mandatory for sign-off)

ClassPAD (mandatory and design dependant) ClassFC44S

Enable minimum density rules YES

DB Format GDSII

GOLDEN INCLUDE FILE CATION\_FINISHING/MODULES/CADENCE/pvs\_pack/drc\_cmos028FDSoI/golden\_file.txt

2 \_\_\_\_\_ Optional parameters \_\_\_\_\_

Define CHIP as the extent of physical layers only

Check Recommended Rules NO

Perform Boolean Debug NO

Perform Latchup Debug NO

Perform Antenna Rules Debug NO

File Name Included To Execute The EXCLUDE none

CELL Command

Perform Emetrology Density structures checks (mandatory for sign-off)

Perform Emetrology Density structures Helps

IP CHECKS (Density requirements for IPs to ensure compliance with SOC density rules)

Start DRC DE

**Cancel** **Apply** **Submit**

Introduction

Technology Overview

Design-Kit Contents

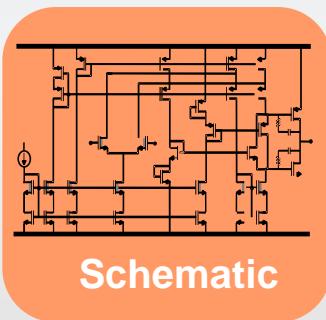
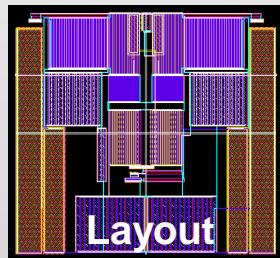
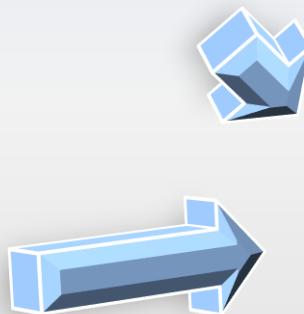
Roadmap

Support



*Is my layout equivalent to the schematic?*

LVS, Layout Versus Schematic, will tell me!

**LVS Options****Schematic****Layout****Process Rules,  
Devices description**

Introduction

Technology Overview

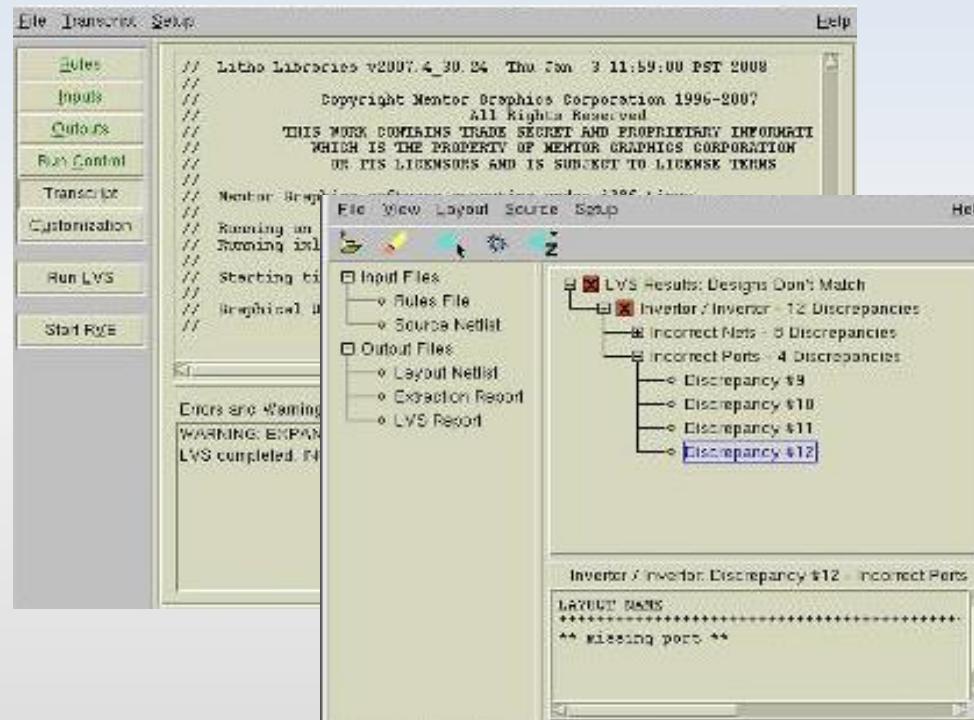
Design-Kit Contents

Roadmap

Support



## Launch **calibre** LVS unix



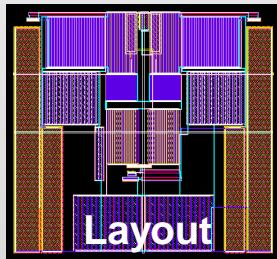
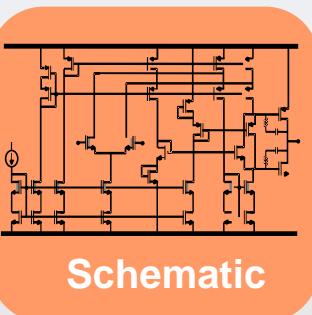
Introduction

Technology Overview

Design-Kit Contents

Roadmap

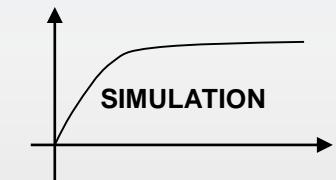
Support



*How to take interconnects and layout effects  
into account during simulation?*



**Extraction  
Options**



**Simulable Netlist**

**with parasitics**



**Devices description,  
Interconnects description**

Introduction

Technology Overview

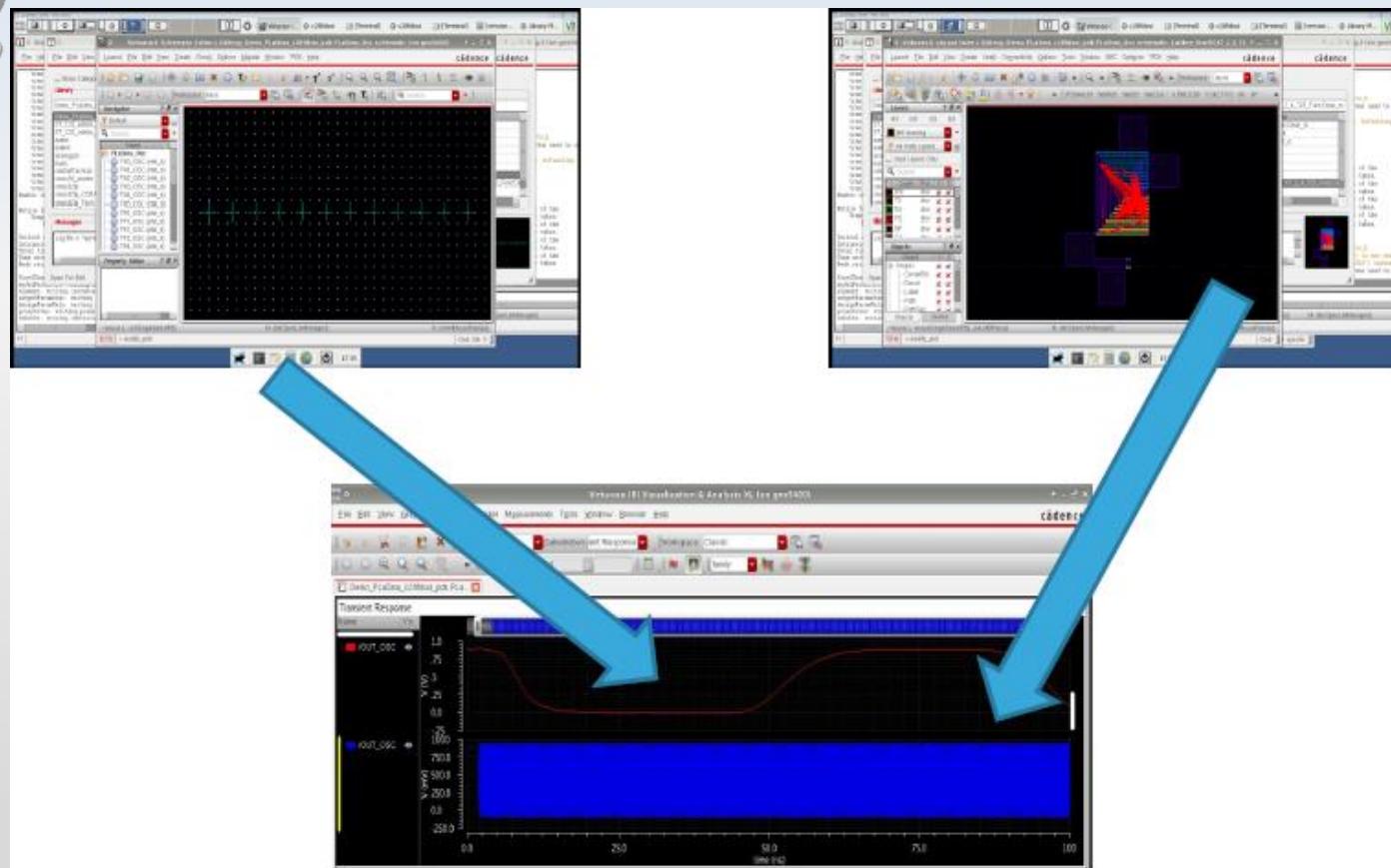
Design-Kit Contents

Roadmap

Support



- Use **PLaSma** stands for : **[P]ost [La]ayout [S]imulation**
  - simple user-friendly methodology for Post-Layout simulation using calibre and StarRCXT.



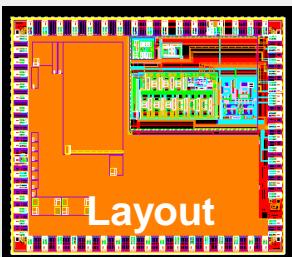
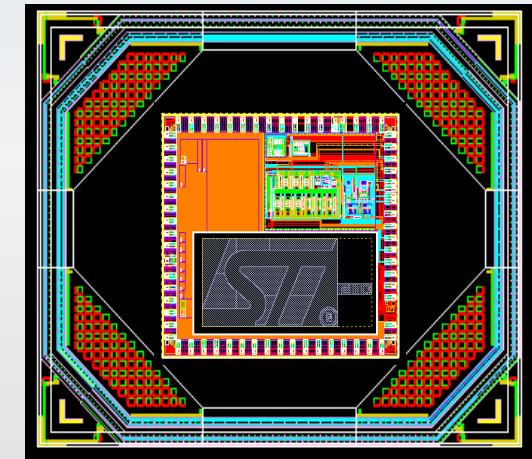
Introduction

Technology Overview

Design-Kit Contents

Roadmap

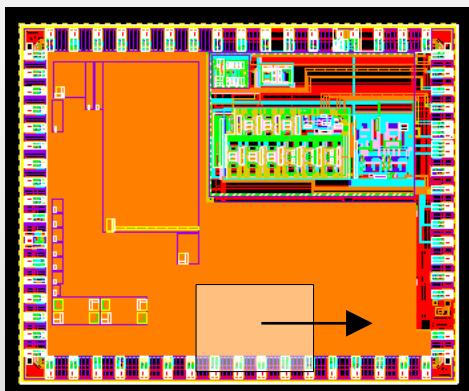
Support

Design Kit  
PCells

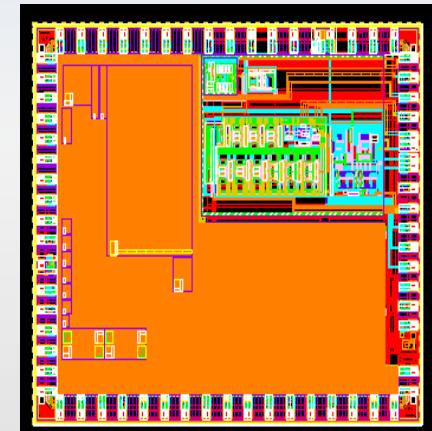
Process Rules



## Tiling Options



## Process Rules





- The Tiling step is done by Designer at chip finishing
  - Possibility to use “noTiles” layer to prevent tiles generation
- Protect your sensitive devices with dummies exclusion layers (PCEXCLUD, RXEXCLUD, Mx;exclude)
- Because, traditional tiling with calibre DRC has become now obsolete, ST has its own tiling solution: **SmartTiling (SMT)**, provided in DK (via-tiling)
  - requires an extra calyieldenhance (YE) license.



# PART IV DOCUMENTATION

**CMOS & Derivative PDK**

Introduction

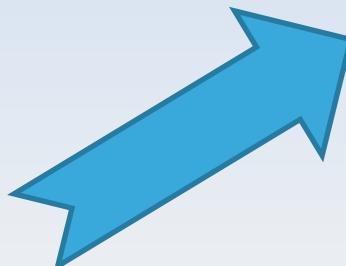
Technology Overview

Design-Kit Contents

Roadmap

Support

Design Rule Manuals available at  
**\$PDK/doc/TECHNOLOGY/DRM path :**

ADCS : 8343474 : 28FDSOI**Additional PC Design Rules in STMicroelectronics technology**

ST_102_or	One of the following rules must be met {102, 102peri, 102s, 102t, 102u, 102mb, CT01b}.		
ST_105_or	Gate with channel length < 0.048 um must meet ST_105a, ST_105b or ST_105c		
ST_105a	(Gate with channel length < 0.048 um) maximum space to PC in Gate side direction on both sides of the gate, with an exception for a single run-length with length < 10% of the device width	0.146	
ST_105b	(Gate with channel length < 0.048 um) exact space to PC in Gate side direction on both sides of the gate, with an exception for a single run-length with length < 10% of the device width	0.222	
ST_105c	(Gate with channel length < 0.048 um) exact space to PC in Gate side direction on both sides of the gate, with an exception for a single run-length with length < 10% of the device width	0.242	
ST_107a	Orientation-restricted gates (Gate over CELLSNR or HVT or PCCRIT or PCORIENT or MKR,srmperi) must have the gate width aligned along the X-axis <sup>a</sup>		
PC.D.1	Distance of U-shape PC <sup>bcd</sup> to RX <sup>f</sup> .	A	0.029

a.DRC implementation is: RX edges cutting PC must be aligned along the Y-axis

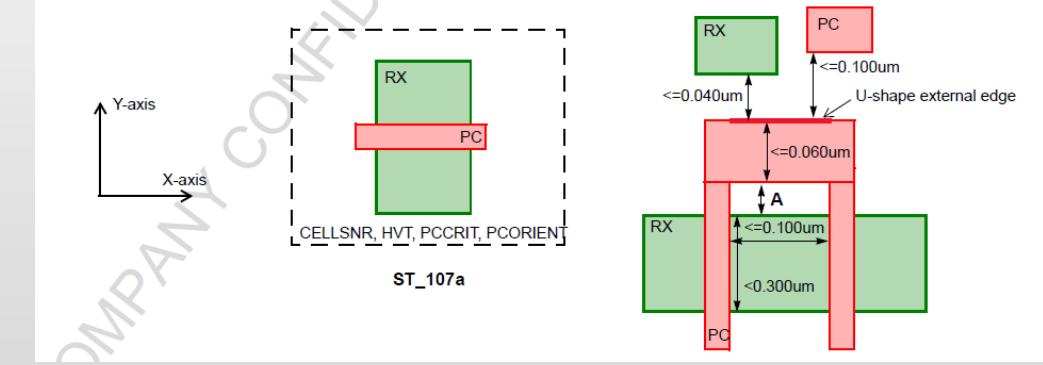
b.This rule does not apply to U-shape PC with PC notch length &gt; 0.100um

c.This rule does not apply to U-shape PC with PC head width &gt; 0.060um

d.This rule does not apply to U-shape PC with U-shape external edge distance to PC &gt; 0.100um

e.This rule does not apply to U-shape PC with U-shape external edge distance to RX &gt; 0.040um

f.This rule does not apply to RX with width &gt;= 0.300um





- In the 28FDSOI PDK, you could find:
  - A README file for each analog flow step (**SIMULATION, DRC/LVS/PEX...**)
  - Releases Notes (RN) and Known problems and solutions (KPS)
  - Spice models documents



*At the end of this course, you will be able to*

- **Recall** the available Design Kit and choose among the options
- **Identify** where and how to get a Design Kit related information and support
- **Configure** the CAD tools
- **Run all the steps of the analog flow**





Thanks for your attention