C28SOI_IO_EXT_CSF_BASIC_EG_6U1X2T8XLB

Release Notes and Known Problems and Solutions

1. Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library Name	C28SOI_IO_EXT_CSF_BASIC_EG_6U1X2T8XLB
Library Version	7.0
Library Type	IO Cells
Technology	CMOS028_FDSOI
DK Version	DK_cmos28FDSOI_RF_6U1x_2T8x_LB 2.8.c-08

1.2 Impact of Product Release

For latest information, please refer to LYS *(http://col2.cro.st.com/libyield).*

1.3 Related Documentation

- **C28SOI_IO_EXT_CSF_BASIC_EG_7.0 User Manual**
- **C28SOI_IO_EXT_CSF_BASIC_EG_7.0 Release Notes and Known Problems and Solutions**
- **C28SOI_IO_EXT_CSF_BASIC_EG_7.0 HDL MODELS model usage guidelines**
- **C28SOI_IO_EXT_CSF_BASIC_EG_ff28_1.05V_1.95V_125C_7y50kR_ss28_1.10V_1.65V_m40C_7y50kR_7.0 DataBook**
- **C28SOI_IO_EXT_CSF_BASIC_EG_ff28_1.10V_1.95V_m40C_tt28_1.00V_1.80V_25C_ss28_0.90V_1.65V_125C_-7.0 DataBook**
- **C28SOI_IO_EXT_CSF_BASIC_EG_ff28_0.90V_1.95V_125C_2ey_ss28_0.90V_1.65V_m40C_2ey_7.0 Data-Book**

- **C28SOI_IO_EXT_CSF_BASIC_EG_ff28_0.90V_1.95V_m40C_2ey_ss28_0.90V_1.65V_125C_2ey_7.0 DataBook**
- **C28SOI_IO_EXT_CSF_BASIC_EG_ff28_1.10V_1.95V_125C_ss28_0.90V_1.65V_m40C_7.0 DataBook**
- **C28SOI_IO_EXT_CSF_BASIC_EG_ff28_1.10V_1.95V_m40C_7y50kR_ss28_1.10V_1.65V_125C_7y50kR_7.0 DataBook**

2. Changes with respect to all Previous Versions

2.1 Changes in Version 7.0-02 w.r.t Version 7.0-01

A. STF are Characterized with SPICE DK_cmos28FDSOI_RF_6U1x_2U2x_2T8x_LB 2.8.c-08

B. 86 corners are added in this release

No Update

2.2 Changes in Version 7.0-01 w.r.t Version 6.0.b

A. This is the Final release

B. Major content of packages are

(1) HDL Models:

(a) Emulator (_emul.v), Tetramax(_tmax.v),Verilog(.v), Power Verilog (_allpins.v), MENTOR

(2) STF View contains 51 corners

(3) Physical Views (Layout ,Signoff LEF , CADENCE LEF ,Schematic, CDL, GDS, SPI, Abstract , Synopsys Layout)

(4) Other views(ADMS, NOVAS, CPF, IODA, VOLTUS etc.)

First release

2.3 Changes in Version 6.0.b w.r.t Version 6.0

Physical views of this package updated CDL , GDS and SYNOPSYS LAYOUT & FRAM.

2.4 Version 6.0

A. This is the Final release.

B. This package contains Verilog, libs, Cadence LEF, SIGNOFF LEF, SIP, SIGNOFF GDS, CDL and SYNOPSYS LAYOUT & FRAM.

(1) Verilog Models:

I. Verilog (.v) model : Compliance with power aware flow.

II. In VERILOG Pin name, Pin direction and functionality is aligned with Usermanual .

(2) Liberty NLDM (STF) :

I. STF view is compliance with UPF flow .

3. Known Problems and Solutions of this release

This document is compatible for viewing with acroread 7.0 and later versions. If opened with a lower version of acroread, there might be some color display problem.

DRC Errors:

EMET.DEN.1 - All topcells - Corrected at chip level
EMET.DEN.2 - All topcells - Corrected at chip level
EMET.DEN.3 - All topcells - Corrected at chip level
EMET.DEN.4 - All topcells - Corrected at chip level
EMET.DEN.5 - All topcells - Corrected at chip level
EMET.DEN.6 - All topcells - Corrected at chip level
EMET.DEN.7 - All topcells - Corrected at chip level
EMET.DEN.8 - All topcells - Corrected at chip level
EMET.DEN.9 - All topcells - Corrected at chip level
EMET.DEN.10 - All topcells - Corrected at chip level
EMET.DEN.11 - All topcells - Corrected at chip level
EMET.DEN.12 - All topcells - Corrected at chip level
RX.DEN.1 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles
PC.DEN.1 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles
M1.DEN.1 - GNDE/VDDE_EXT_CSF_FC_OUTER, *CORNER_EXT_CSF_FC_2ROWS and EMPTYCELL_EXT_CSF_FC_INNER/OUTER - Corrected by tiles
M2.DEN.1 - EMPTYCELL_EXT_CSF_FC_OUTER, *CORNER_EXT_CSF_FC_2ROWS, GNDE/VDDE_EXT_CSF_FC_OUTER, FILLCELL_FEEDTHROUGH_40UM_EXT_CSF_CL_LIN - Corrected by tiles
M3.DEN.1 - EMPTYCELL_EXT_CSF_FC_OUTER, *CORNER_EXT_CSF_FC_2ROWS, GNDE/VDDE_EXT_CSF_FC_OUTER, FILLCELL_FEEDTHROUGH_40UM_EXT_CSF_CL_LIN - Corrected by tiles
M4.DEN.1 - EMPTYCELL_EXT_CSF_FC_OUTER, *CORNER_EXT_CSF_FC_2ROWS, GNDE/VDDE_EXT_CSF_FC_OUTER, FILLCELL_FEEDTHROUGH_40UM_EXT_CSF_CL_LIN - Corrected by tiles
M5.DEN.1 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles
M6.DEN.1 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles
B1.DEN.1 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

B2.DEN.1 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

IA.DEN.1 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

IB.DEN.1 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

GR8x00_IA - all FILLCELL_1GRID_EXT_CSF* - Corrected by abutment

GR8x01a_IA - all FILLCELL_1GRID_EXT_CSF* - Corrected by abutment

GR601a_M5 - all FILLCELL_1GRID_EXT_CSF* - Corrected by abutment

GR601aSE_M5 - all FILLCELL_1GRID_EXT_CSF* - Corrected by abutment

HYBRID.W.1 - all FILLCELL_1GRID_EXT_CSF* - Corrected by abutment

GR8x00_IB - all FILLCELL_1GRID_EXT_CSF* - Corrected by abutment

GR8x01a_IB - all FILLCELL_1GRID_EXT_CSF* - Corrected by abutment

GRB_N301 - FILLCELL_1UM_EXT_CSF_CL_LIN - Corrected by abutment

GR3T02 - FILLCELL_1UM_EXT_CSF_CL_LIN and FILLCELL_1GRID_EXT_CSF_CL_LIN - Corrected by abutment

GR3T05 - FILLCELL_1GRID_EXT_CSF_CL_LIN - Corrected by abutment

ST_B_BP01a - FILLCELL_1GRID_EXT_CSF_CL_LIN - Corrected by abutment

GR350a - FILLCELL_1GRID_EXT_CSF_CL_LIN - Corrected by abutment

PLDDSOI.B.1.2 - FILLCELL_1GRID_EXT_CSF_CL_LIN - Corrected by abutment

NLDDSOI.B.1.2 - FILLCELL_1GRID_EXT_CSF_CL_LIN - Corrected by abutment

ST_B_BN01a - FILLCELL_1GRID_EXT_CSF_CL_LIN - Corrected by abutment

RX.DEN.8 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

PC.DEN.8 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

M1.DEN.8 - GNDE/VDDE_EXT_CSF_FC_OUTER, *CORNER_EXT_CSF_FC_2ROWS and EMPTYCELL_EXT_CSF_FC_INNER/OUTER - Corrected by tiles

M2.DEN.8 - EMPTYCELL_EXT_CSF_FC_OUTER, *CORNER_EXT_CSF_FC_2ROWS, GNDE/VDDE_EXT_CSF_FC_OUTER, FILLCELL_FEEDTHROUGH_40UM_EXT_CSF_CL_LIN - Corrected by tiles

M3.DEN.8 - EMPTYCELL_EXT_CSF_FC_OUTER, *CORNER_EXT_CSF_FC_2ROWS, GNDE/VDDE_EXT_CSF_FC_OUTER, FILLCELL_FEEDTHROUGH_40UM_EXT_CSF_CL_LIN - Corrected by tiles

M4.DEN.8 - EMPTYCELL_EXT_CSF_FC_OUTER, *CORNER_EXT_CSF_FC_2ROWS, GNDE/VDDE_EXT_CSF_FC_OUTER, FILLCELL_FEEDTHROUGH_40UM_EXT_CSF_CL_LIN - Corrected by tiles

M5.DEN.8 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

M6.DEN.8 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

B1.DEN.8 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

B2.DEN.8 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

IA.DEN.8 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

	IB.DEN.8 - EMPTYCELL_EXT_CSF_FC_OUTER and GNDE/VDDE_EXT_CSF_FC_OUTER - Corrected by tiles

	**LVS/ERC Errors** **Comparison : nothing in layout - All topcells with empty schematic - Corrected at chip level** **ERC1a - all Filler Cut cells and all 1Grid cells - Corrected at chip level** **ERC2_ST - FILLCELL_1GRID_EXT_CSF_CL_LIN - Corrected at chip level** **ERC3_ST - FILLCELL_1GRID_EXT_CSF_CL_LIN - Corrected at chip level** **SOFTCHECK: stamping conflict - FILLCUTCELL_ALL_EXT_CSF_FC_2ROWS and FILLCUTCELL_ALL_EXT_CSF_FC_LIN - Corrected by abutment**

4. Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact HELPDESK (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.

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