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C28SOI_SC_12_CORE_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells

Overview

- C28SOI_SC_12_CORE_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

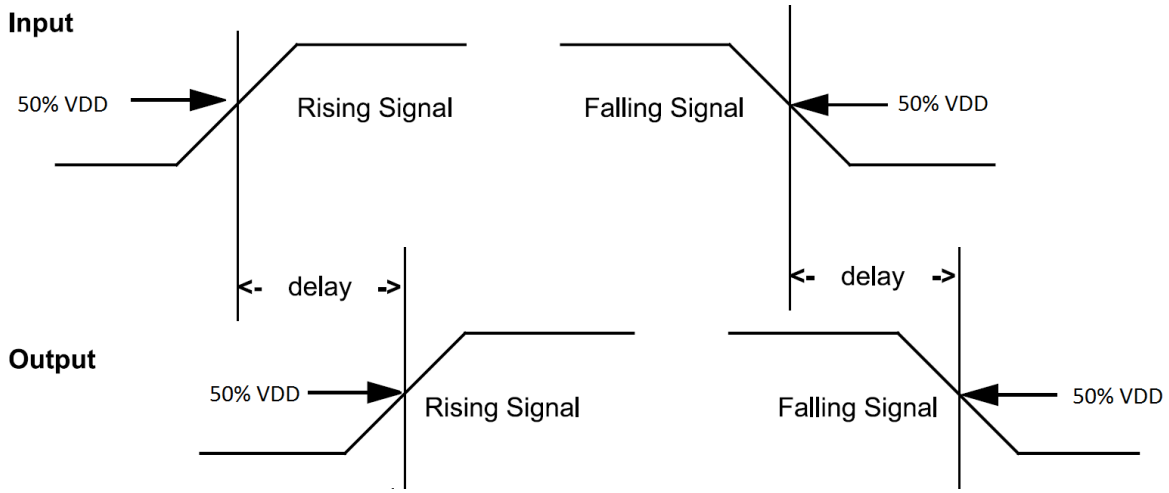


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

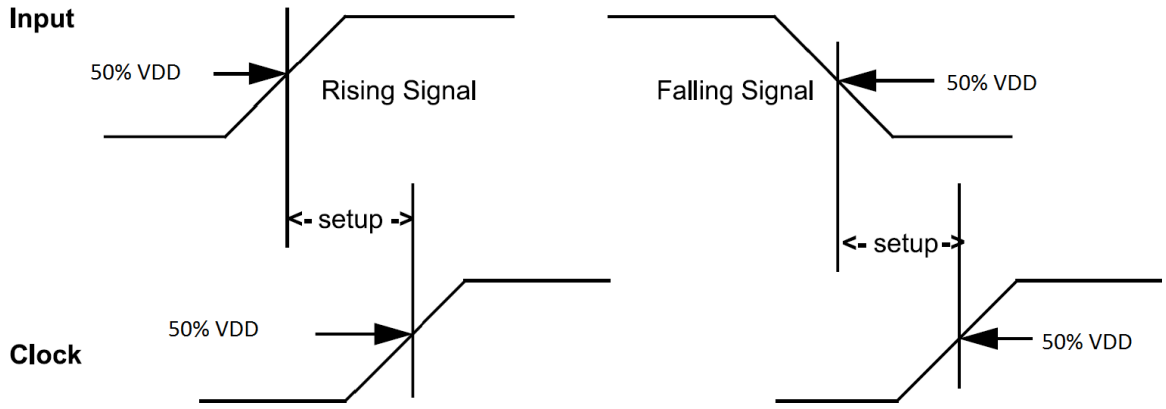


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

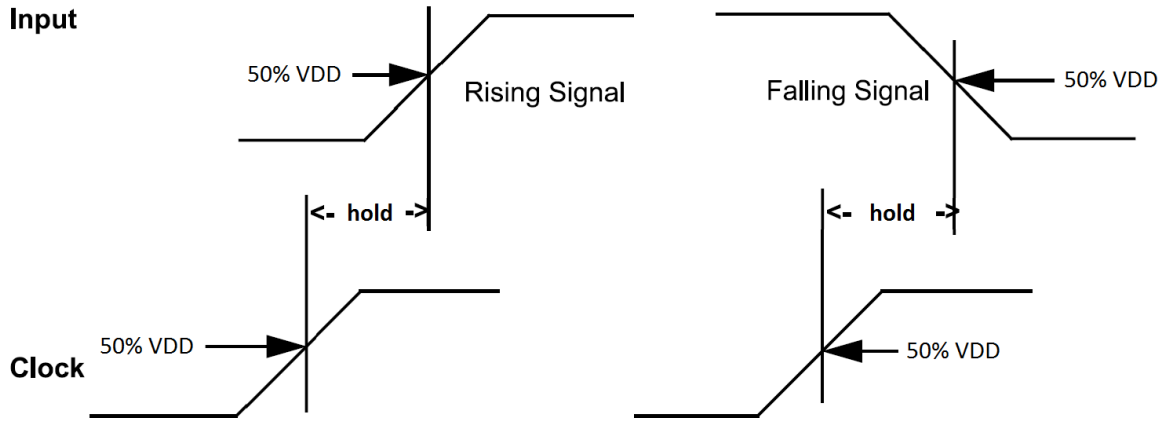


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

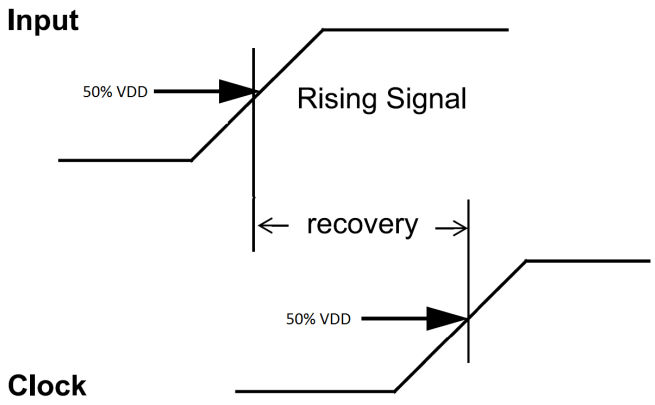


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

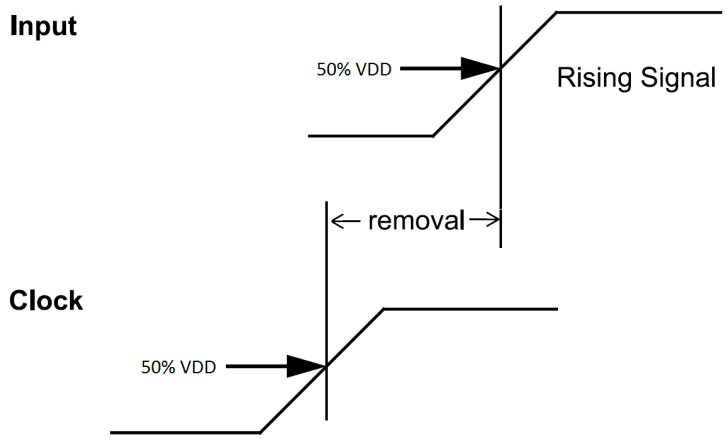


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

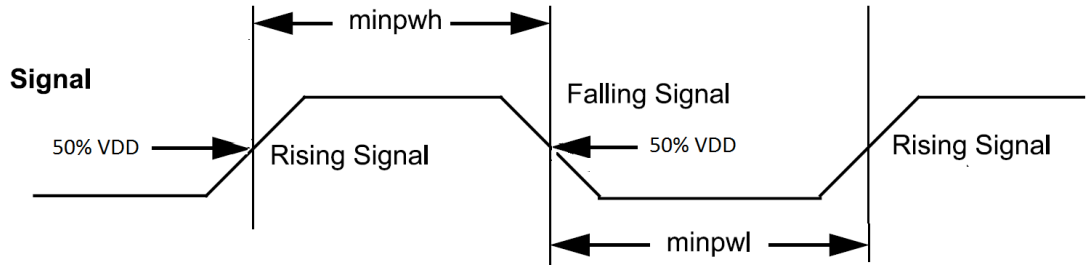


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

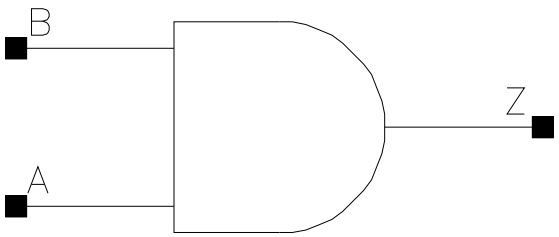
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X25_P0	1.200	1.088	1.3056
X33_P0	1.200	1.360	1.6320
X42_P0	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0007	0.0010	0.0015	0.0018
B	0.0006	0.0009	0.0014	0.0018
	X42_P0			
A	0.0018			
B	0.0018			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0274	0.0219	2.0474	1.0389
A to Z ↑	0.0223	0.0207	3.0598	1.4864
B to Z ↓	0.0261	0.0207	2.0475	1.0372
B to Z ↑	0.0237	0.0219	3.0623	1.4862
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0226	0.0217	0.6850	0.5110

A to Z ↑	0.0202	0.0207	0.9799	0.7393
B to Z ↓	0.0215	0.0198	0.6852	0.5100
B to Z ↑	0.0214	0.0213	0.9806	0.7401
	X42_P0		**X42_P0**	
A to Z ↓	0.0236		0.4145	
A to Z ↑	0.0227		0.5930	
B to Z ↓	0.0218		0.4135	
B to Z ↑	0.0234		0.5925	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	9.381e-05	1.000e-20
X16_P0	2.081e-04	1.000e-20
X25_P0	3.008e-04	1.000e-20
X33_P0	4.138e-04	1.000e-20
X42_P0	4.825e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	1.048e-05	2.025e-05	3.123e-05	8.000e-05
B (output stable)	1.883e-05	3.398e-05	5.336e-05	2.054e-04
A to Z	2.064e-03	3.508e-03	5.354e-03	7.024e-03
B to Z	1.999e-03	3.401e-03	5.184e-03	6.596e-03
	X42_P0			
A (output stable)	8.114e-05			
B (output stable)	2.034e-04			
A to Z	8.581e-03			
B to Z	8.139e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

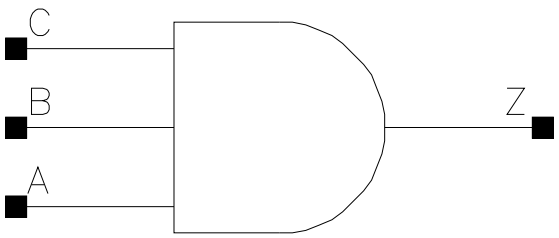
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X25_P0	1.200	1.360	1.6320
X33_P0	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0006	0.0010	0.0016	0.0019
B	0.0005	0.0009	0.0014	0.0017
C	0.0006	0.0009	0.0013	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0294	0.0241	2.0714	1.0120
A to Z ↑	0.0286	0.0268	3.0945	1.4734
B to Z ↓	0.0285	0.0232	2.0706	1.0108
B to Z ↑	0.0298	0.0279	3.0902	1.4737
C to Z ↓	0.0275	0.0221	2.0680	1.0097
C to Z ↑	0.0308	0.0284	3.0920	1.4743
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0243	0.0227	0.6929	0.5186

A to Z ↑	0.0260	0.0248	1.0036	0.7513
B to Z ↓	0.0234	0.0216	0.6926	0.5184
B to Z ↑	0.0272	0.0259	1.0048	0.7515
C to Z ↓	0.0221	0.0206	0.6916	0.5175
C to Z ↑	0.0278	0.0266	1.0045	0.7528

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	9.235e-05	1.000e-20
X17_P0	2.067e-04	1.000e-20
X25_P0	2.931e-04	1.000e-20
X33_P0	4.032e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	1.181e-05	2.435e-05	3.233e-05	4.485e-05
B (output stable)	1.437e-05	2.785e-05	4.035e-05	5.458e-05
C (output stable)	3.165e-05	6.061e-05	9.015e-05	1.277e-04
A to Z	2.290e-03	4.107e-03	5.919e-03	7.547e-03
B to Z	2.213e-03	3.969e-03	5.704e-03	7.258e-03
C to Z	2.155e-03	3.848e-03	5.512e-03	6.998e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

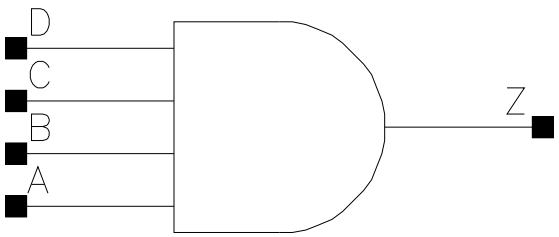
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X6_P0	1.200	1.088	1.3056
X20_P0	1.200	2.312	2.7744
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P0	X6_P0	X20_P0	X27_P0
A	0.0005	0.0007	0.0016	0.0018
B	0.0005	0.0007	0.0016	0.0018
C	0.0004	0.0007	0.0015	0.0018
D	0.0005	0.0007	0.0016	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X6_P0	X4_P0	X6_P0
A to Z ↓	0.0309	0.0265	3.9209	2.5266
A to Z ↑	0.0300	0.0228	10.7486	5.6925
B to Z ↓	0.0300	0.0251	3.9182	2.5256
B to Z ↑	0.0316	0.0236	10.7496	5.6953
C to Z ↓	0.0322	0.0288	3.8843	2.5337
C to Z ↑	0.0305	0.0231	10.7554	5.6999

D to Z ↓	0.0315	0.0270	3.8832	2.5316
D to Z ↑	0.0329	0.0242	10.7568	5.6974
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0253	0.0233	0.7322	0.5172
A to Z ↑	0.0232	0.0263	1.8962	1.4415
B to Z ↓	0.0231	0.0214	0.7302	0.5160
B to Z ↑	0.0235	0.0269	1.8963	1.4406
C to Z ↓	0.0248	0.0226	0.7363	0.5181
C to Z ↑	0.0210	0.0233	1.8953	1.4397
D to Z ↓	0.0225	0.0209	0.7334	0.5168
D to Z ↑	0.0213	0.0241	1.8935	1.4393

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	3.989e-05	1.000e-20
X6_P0	1.081e-04	1.000e-20
X20_P0	3.368e-04	1.000e-20
X27_P0	4.397e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	3.283e-04	5.281e-04	1.544e-03	1.892e-03
B (output stable)	3.113e-04	4.929e-04	1.430e-03	1.774e-03
C (output stable)	3.268e-04	5.557e-04	1.391e-03	1.727e-03
D (output stable)	3.134e-04	5.184e-04	1.268e-03	1.605e-03
A to Z	1.388e-03	2.181e-03	6.539e-03	8.508e-03
B to Z	1.342e-03	2.087e-03	6.093e-03	8.055e-03
C to Z	1.418e-03	2.295e-03	5.824e-03	7.375e-03
D to Z	1.372e-03	2.195e-03	5.378e-03	6.952e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

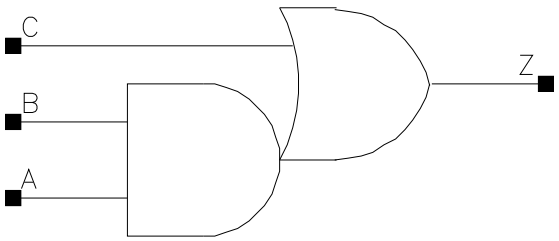
Pin Cycle (vdds)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0019
B	0.0006	0.0009	0.0017
C	0.0007	0.0010	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0341	0.0298	2.0929	1.0248
A to Z ↑	0.0230	0.0205	2.9852	1.4608
B to Z ↓	0.0319	0.0277	2.0889	1.0214
B to Z ↑	0.0246	0.0220	2.9850	1.4616
C to Z ↓	0.0333	0.0289	2.0864	1.0208
C to Z ↑	0.0210	0.0196	2.9667	1.4528
	X33_P0		**X33_P0**	
A to Z ↓	0.0298		0.5199	
A to Z ↑	0.0209		0.7358	

B to Z ↓	0.0279		0.5188	
B to Z ↑	0.0220		0.7361	
C to Z ↓	0.0291		0.5182	
C to Z ↑	0.0194		0.7323	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	8.910e-05	1.000e-20
X17_P0	1.957e-04	1.000e-20
X33_P0	3.849e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	3.501e-05	5.488e-05	1.295e-04
B (output stable)	3.870e-05	6.284e-05	1.588e-04
C (output stable)	4.513e-05	7.719e-05	1.775e-04
A to Z	2.166e-03	3.826e-03	7.610e-03
B to Z	2.087e-03	3.677e-03	7.262e-03
C to Z	2.293e-03	4.033e-03	8.058e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

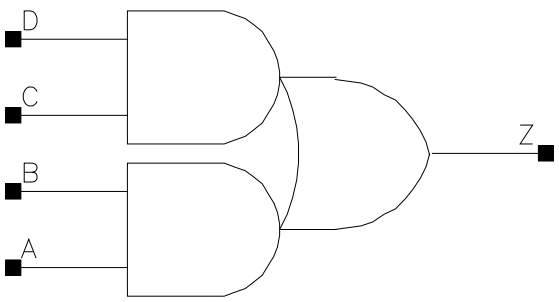
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0017
B	0.0006	0.0009	0.0016
C	0.0005	0.0008	0.0018
D	0.0006	0.0009	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0389	0.0334	2.0186	1.0196
A to Z ↑	0.0296	0.0269	2.9383	1.4640
B to Z ↓	0.0363	0.0312	2.0099	1.0163
B to Z ↑	0.0306	0.0283	2.9383	1.4637

C to Z ↓	0.0352	0.0311	2.0126	1.0175
C to Z ↑	0.0252	0.0232	2.9314	1.4579
D to Z ↓	0.0340	0.0298	2.0074	1.0151
D to Z ↑	0.0272	0.0248	2.9293	1.4584
	X33_P0		**X33_P0**	
A to Z ↓	0.0312		0.5200	
A to Z ↑	0.0244		0.7396	
B to Z ↓	0.0296		0.5193	
B to Z ↑	0.0259		0.7390	
C to Z ↓	0.0288		0.5189	
C to Z ↑	0.0210		0.7366	
D to Z ↓	0.0273		0.5181	
D to Z ↑	0.0223		0.7366	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.078e-04	1.000e-20
X17_P0	2.320e-04	1.000e-20
X33_P0	4.495e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	2.952e-05	4.123e-05	5.654e-05
B (output stable)	8.407e-05	1.088e-04	7.232e-05
C (output stable)	3.293e-05	5.371e-05	1.248e-04
D (output stable)	3.644e-05	6.209e-05	1.464e-04
A to Z	2.805e-03	4.834e-03	8.752e-03
B to Z	2.623e-03	4.594e-03	8.449e-03
C to Z	2.450e-03	4.282e-03	7.625e-03
D to Z	2.384e-03	4.152e-03	7.361e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

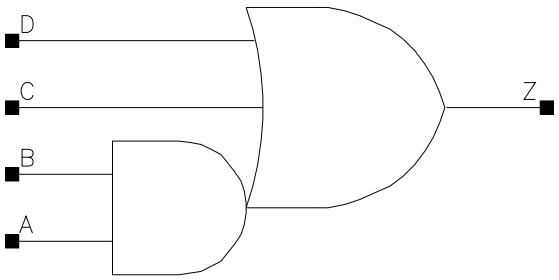
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	0.952	1.1424
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0016
B	0.0006	0.0009	0.0017
C	0.0006	0.0009	0.0017
D	0.0006	0.0009	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0447	0.0384	2.1770	1.0713
A to Z ↑	0.0249	0.0225	2.9784	1.5111
B to Z ↓	0.0432	0.0362	2.1715	1.0690
B to Z ↑	0.0267	0.0235	2.9728	1.5099
C to Z ↓	0.0460	0.0390	2.1671	1.0677
C to Z ↑	0.0228	0.0210	2.9557	1.5024

D to Z ↓	0.0459	0.0394	2.1670	1.0683
D to Z ↑	0.0224	0.0208	2.9543	1.5010
	X33_P0		**X33_P0**	
A to Z ↓	0.0392		0.5372	
A to Z ↑	0.0225		0.7375	
B to Z ↓	0.0355		0.5343	
B to Z ↑	0.0232		0.7363	
C to Z ↓	0.0405		0.5342	
C to Z ↑	0.0208		0.7340	
D to Z ↓	0.0398		0.5347	
D to Z ↑	0.0200		0.7322	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	7.594e-05	1.000e-20
X17_P0	1.676e-04	1.000e-20
X33_P0	3.326e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	4.291e-05	7.651e-05	1.805e-04
B (output stable)	4.280e-05	7.443e-05	1.996e-04
C (output stable)	2.264e-05	4.306e-05	1.235e-04
D (output stable)	2.925e-05	5.485e-05	1.933e-04
A to Z	2.479e-03	4.267e-03	8.649e-03
B to Z	2.413e-03	4.112e-03	8.103e-03
C to Z	2.699e-03	4.636e-03	9.543e-03
D to Z	2.587e-03	4.454e-03	8.963e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

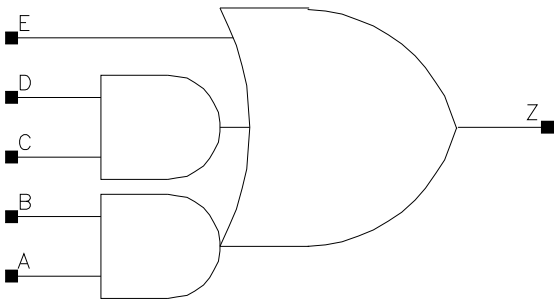
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.088	1.3056
X17_P0	1.200	1.224	1.4688
X33_P0	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0008	0.0017
B	0.0006	0.0009	0.0016
C	0.0007	0.0011	0.0018
D	0.0006	0.0009	0.0017
E	0.0006	0.0009	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0537	0.0444	2.0708	1.0420
A to Z ↑	0.0312	0.0269	2.9207	1.4698

B to Z ↓	0.0522	0.0426	2.0635	1.0393
B to Z ↑	0.0334	0.0285	2.9193	1.4682
C to Z ↓	0.0463	0.0400	2.0646	1.0398
C to Z ↑	0.0265	0.0228	2.8956	1.4595
D to Z ↓	0.0435	0.0368	2.0558	1.0347
D to Z ↑	0.0282	0.0241	2.8962	1.4583
E to Z ↓	0.0478	0.0398	2.0535	1.0349
E to Z ↑	0.0240	0.0209	2.8716	1.4511
	X33_P0		**X33_P0**	
A to Z ↓	0.0442		0.5364	
A to Z ↑	0.0278		0.7423	
B to Z ↓	0.0417		0.5351	
B to Z ↑	0.0294		0.7429	
C to Z ↓	0.0387		0.5354	
C to Z ↑	0.0228		0.7362	
D to Z ↓	0.0359		0.5332	
D to Z ↑	0.0241		0.7366	
E to Z ↓	0.0392		0.5333	
E to Z ↑	0.0209		0.7319	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	9.481e-05	1.000e-20
X17_P0	2.035e-04	1.000e-20
X33_P0	3.853e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	1.488e-05	2.396e-05	5.497e-05
B (output stable)	1.904e-05	2.688e-05	6.733e-05
C (output stable)	5.073e-05	6.891e-05	1.750e-04
D (output stable)	6.027e-05	8.420e-05	1.936e-04
E (output stable)	8.720e-05	1.144e-04	2.666e-04
A to Z	3.273e-03	5.339e-03	1.058e-02
B to Z	3.201e-03	5.175e-03	1.014e-02
C to Z	2.699e-03	4.507e-03	8.743e-03
D to Z	2.608e-03	4.322e-03	8.334e-03
E to Z	2.846e-03	4.688e-03	9.135e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

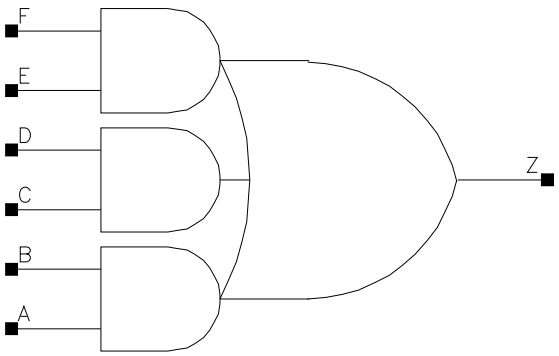
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.360	1.6320
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
A	0.0006	0.0006	0.0008	0.0017

B	0.0006	0.0007	0.0012	0.0016
C	0.0005	0.0006	0.0008	0.0017
D	0.0006	0.0007	0.0008	0.0016
E	0.0006	0.0007	0.0009	0.0018
F	0.0006	0.0007	0.0009	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0543	0.0510	4.0633	2.0788
A to Z ↑	0.0335	0.0319	5.8580	2.9761
B to Z ↓	0.0500	0.0473	4.0329	2.0653
B to Z ↑	0.0342	0.0329	5.8541	2.9744
C to Z ↓	0.0493	0.0468	4.0483	2.0721
C to Z ↑	0.0303	0.0289	5.8220	2.9587
D to Z ↓	0.0475	0.0451	4.0359	2.0656
D to Z ↑	0.0324	0.0309	5.8185	2.9563
E to Z ↓	0.0415	0.0406	4.0343	2.0660
E to Z ↑	0.0256	0.0246	5.7870	2.9419
F to Z ↓	0.0392	0.0383	4.0209	2.0588
F to Z ↑	0.0272	0.0262	5.7867	2.9431
	X17_P0	X33_P0	X17_P0	X33_P0
A to Z ↓	0.0479	0.0458	1.0473	0.5347
A to Z ↑	0.0296	0.0295	1.4741	0.7452
B to Z ↓	0.0452	0.0434	1.0405	0.5332
B to Z ↑	0.0313	0.0311	1.4740	0.7447
C to Z ↓	0.0446	0.0427	1.0443	0.5343
C to Z ↑	0.0270	0.0273	1.4670	0.7407
D to Z ↓	0.0424	0.0405	1.0405	0.5330
D to Z ↑	0.0288	0.0288	1.4669	0.7401
E to Z ↓	0.0385	0.0389	1.0409	0.5331
E to Z ↑	0.0227	0.0237	1.4606	0.7381
F to Z ↓	0.0363	0.0362	1.0372	0.5312
F to Z ↑	0.0242	0.0252	1.4600	0.7383

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	7.245e-05	1.000e-20
X8_P0	1.305e-04	1.000e-20
X17_P0	2.398e-04	1.000e-20
X33_P0	4.518e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	3.000e-05	3.473e-05	4.401e-05	7.891e-05
B (output stable)	6.807e-05	7.605e-05	7.953e-05	1.028e-04
C (output stable)	3.106e-05	3.718e-05	4.724e-05	1.073e-04
D (output stable)	3.513e-05	4.268e-05	5.319e-05	1.397e-04
E (output stable)	8.724e-05	1.060e-04	1.320e-04	2.219e-04
F (output stable)	8.863e-05	1.058e-04	1.382e-04	2.470e-04

A to Z	2.747e-03	3.801e-03	5.946e-03	1.124e-02
B to Z	2.540e-03	3.558e-03	5.615e-03	1.080e-02
C to Z	2.364e-03	3.342e-03	5.325e-03	1.008e-02
D to Z	2.286e-03	3.242e-03	5.163e-03	9.690e-03
E to Z	1.963e-03	2.885e-03	4.627e-03	9.055e-03
F to Z	1.887e-03	2.783e-03	4.466e-03	8.672e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

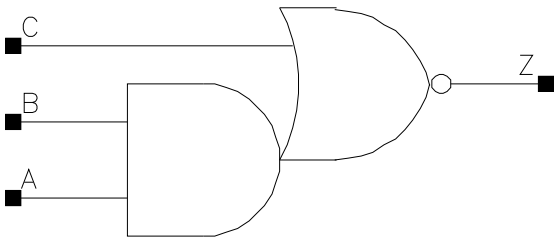
Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008
X44_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X33_P0	X44_P0
A	0.0007	0.0021	0.0041	0.0056
B	0.0007	0.0019	0.0038	0.0051
C	0.0007	0.0022	0.0043	0.0056

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0088	0.0090	3.6857	1.2472
A to Z ↑	0.0156	0.0157	5.8016	1.9344
B to Z ↓	0.0092	0.0092	3.7087	1.2575
B to Z ↑	0.0131	0.0127	5.7192	1.9331
C to Z ↓	0.0088	0.0088	2.1055	0.7198
C to Z ↑	0.0154	0.0150	5.3150	1.7858
	X33_P0	**X44_P0**	**X33_P0**	**X44_P0**
A to Z ↓	0.0093	0.0093	0.6337	0.4806

A to Z ↑	0.0159	0.0158	0.9695	0.7353
B to Z ↓	0.0094	0.0094	0.6389	0.4848
B to Z ↑	0.0128	0.0128	0.9669	0.7312
C to Z ↓	0.0105	0.0105	0.4283	0.3329
C to Z ↑	0.0154	0.0151	0.8941	0.6769

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P0	8.001e-05	1.000e-20
X17_P0	2.304e-04	1.000e-20
X33_P0	4.420e-04	1.000e-20
X44_P0	5.877e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	5.668e-05	1.658e-04	3.785e-04	4.700e-04
B (output stable)	6.183e-05	2.075e-04	4.599e-04	5.641e-04
C (output stable)	7.635e-05	2.288e-04	5.074e-04	6.405e-04
A to Z	1.087e-03	3.347e-03	6.793e-03	8.970e-03
B to Z	9.667e-04	2.796e-03	5.679e-03	7.483e-03
C to Z	1.405e-03	4.117e-03	8.348e-03	1.087e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

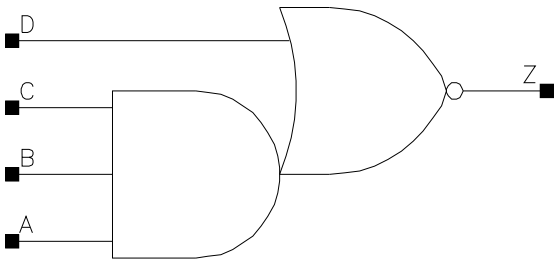
Pin Cycle (vdds)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X29_P0	1.200	3.536	4.2432
X38_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X29_P0	X38_P0
A	0.0007	0.0042	0.0055
B	0.0007	0.0041	0.0052
C	0.0007	0.0038	0.0050
D	0.0008	0.0044	0.0054

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X29_P0	X5_P0	X29_P0
A to Z ↓	0.0134	0.0140	5.2722	0.9070
A to Z ↑	0.0198	0.0195	5.7986	0.9604
B to Z ↓	0.0140	0.0141	5.2864	0.9107
B to Z ↑	0.0178	0.0175	5.7930	0.9661
C to Z ↓	0.0140	0.0136	5.2952	0.9130
C to Z ↑	0.0156	0.0148	5.7226	0.9714
D to Z ↓	0.0108	0.0126	2.1438	0.4316

D to Z ↑	0.0180	0.0181	4.9622	0.8304
	X38_P0		**X38_P0**	
A to Z ↓	0.0135		0.6997	
A to Z ↑	0.0188		0.7241	
B to Z ↓	0.0136		0.7029	
B to Z ↑	0.0168		0.7298	
C to Z ↓	0.0131		0.7047	
C to Z ↑	0.0141		0.7365	
D to Z ↓	0.0133		0.3603	
D to Z ↑	0.0174		0.6271	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	7.867e-05	1.000e-20
X29_P0	4.302e-04	1.000e-20
X38_P0	5.593e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X29_P0	X38_P0
A (output stable)	3.184e-05	2.728e-04	3.480e-04
B (output stable)	3.503e-05	2.868e-04	3.708e-04
C (output stable)	4.868e-05	4.472e-04	5.705e-04
D (output stable)	9.715e-05	7.168e-04	9.433e-04
A to Z	1.451e-03	8.955e-03	1.125e-02
B to Z	1.307e-03	7.712e-03	9.689e-03
C to Z	1.181e-03	6.586e-03	8.191e-03
D to Z	1.754e-03	1.052e-02	1.337e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

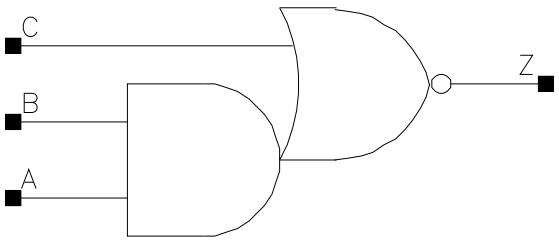
Pin Cycle (vdds)	X5_P0	X29_P0	X38_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X11_P0	1.200	1.088	1.3056
X16_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X11_P0	X16_P0	X23_P0
A	0.0008	0.0015	0.0022	0.0030
B	0.0008	0.0014	0.0021	0.0027
C	0.0007	0.0013	0.0020	0.0028
	X46_P0			
A	0.0057			
B	0.0054			
C	0.0055			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X11_P0	X6_P0	X11_P0
A to Z ↓	0.0105	0.0113	3.5844	1.8129
A to Z ↑	0.0165	0.0173	5.8043	2.8324
B to Z ↓	0.0114	0.0115	3.6045	1.8246

B to Z ↑	0.0145	0.0147	5.7380	2.8390
C to Z ↓	0.0061	0.0067	2.1597	1.2743
C to Z ↑	0.0130	0.0125	5.3183	2.6161
	X16_P0	**X23_P0**	**X16_P0**	**X23_P0**
A to Z ↓	0.0107	0.0111	1.2472	0.9382
A to Z ↑	0.0159	0.0165	1.9058	1.4411
B to Z ↓	0.0113	0.0113	1.2564	0.9447
B to Z ↑	0.0133	0.0137	1.9042	1.4451
C to Z ↓	0.0068	0.0057	0.8878	0.5516
C to Z ↑	0.0118	0.0125	1.7583	1.3305
	X46_P0		**X46_P0**	
A to Z ↓	0.0106		0.4802	
A to Z ↑	0.0156		0.7449	
B to Z ↓	0.0110		0.4839	
B to Z ↑	0.0128		0.7430	
C to Z ↓	0.0058		0.2825	
C to Z ↑	0.0124		0.6865	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P0	7.969e-05	1.000e-20
X11_P0	1.605e-04	1.000e-20
X16_P0	2.272e-04	1.000e-20
X23_P0	3.145e-04	1.000e-20
X46_P0	6.110e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	2.027e-05	5.934e-05	7.270e-05	1.090e-04
B (output stable)	2.570e-05	9.891e-05	1.047e-04	1.641e-04
C (output stable)	2.063e-04	5.246e-04	5.730e-04	8.352e-04
A to Z	1.379e-03	2.971e-03	4.046e-03	5.567e-03
B to Z	1.245e-03	2.567e-03	3.473e-03	4.742e-03
C to Z	9.850e-04	1.983e-03	2.745e-03	3.900e-03
	X46_P0			
A (output stable)	1.938e-04			
B (output stable)	2.780e-04			
C (output stable)	1.383e-03			
A to Z	1.031e-02			
B to Z	8.792e-03			
C to Z	7.394e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

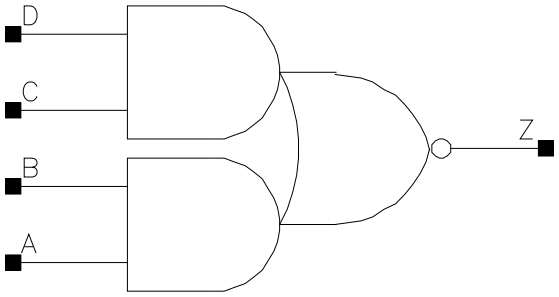
	X46_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P0	X10_P0	X16_P0	X21_P0
A	0.0006	0.0015	0.0023	0.0029
B	0.0006	0.0014	0.0021	0.0028
C	0.0006	0.0015	0.0021	0.0028
D	0.0006	0.0013	0.0019	0.0026
	X42_P0			
A	0.0058			
B	0.0054			
C	0.0055			
D	0.0052			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X10_P0**	**X4_P0**	**X10_P0**
A to Z ↓	0.0120	0.0119	4.4782	1.7542
A to Z ↑	0.0222	0.0181	8.0226	2.6141
B to Z ↓	0.0130	0.0131	4.5046	1.7655
B to Z ↑	0.0200	0.0165	7.9984	2.6691
C to Z ↓	0.0088	0.0086	4.5593	1.7608
C to Z ↑	0.0181	0.0153	7.9825	2.6156
D to Z ↓	0.0095	0.0093	4.5938	1.7757
D to Z ↑	0.0158	0.0134	7.9550	2.6486
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0129	0.0127	1.2520	0.9412
A to Z ↑	0.0189	0.0187	1.7616	1.3565
B to Z ↓	0.0137	0.0133	1.2596	0.9470
B to Z ↑	0.0164	0.0162	1.7617	1.3579
C to Z ↓	0.0090	0.0094	1.2509	0.9413
C to Z ↑	0.0156	0.0162	1.7554	1.3504
D to Z ↓	0.0095	0.0094	1.2614	0.9490
D to Z ↑	0.0130	0.0134	1.7562	1.3509
	X42_P0		**X42_P0**	
A to Z ↓	0.0133		0.4869	
A to Z ↑	0.0189		0.6818	
B to Z ↓	0.0137		0.4899	
B to Z ↑	0.0162		0.6788	
C to Z ↓	0.0098		0.4829	
C to Z ↑	0.0163		0.6796	
D to Z ↓	0.0099		0.4868	
D to Z ↑	0.0136		0.6772	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	5.961e-05	1.000e-20
X10_P0	1.948e-04	1.000e-20
X16_P0	2.736e-04	1.000e-20
X21_P0	3.658e-04	1.000e-20
X42_P0	7.155e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	2.318e-05	5.402e-05	1.062e-04	1.464e-04
B (output stable)	2.913e-05	7.145e-05	1.771e-04	2.562e-04
C (output stable)	5.476e-05	1.223e-04	2.144e-04	2.739e-04
D (output stable)	6.297e-05	1.450e-04	2.851e-04	3.821e-04
A to Z	1.344e-03	3.339e-03	5.171e-03	6.678e-03
B to Z	1.217e-03	3.034e-03	4.543e-03	5.875e-03
C to Z	9.046e-04	2.368e-03	3.571e-03	4.860e-03
D to Z	8.006e-04	2.101e-03	3.024e-03	4.090e-03
	X42_P0			
A (output stable)	2.800e-04			
B (output stable)	4.578e-04			
C (output stable)	5.266e-04			
D (output stable)	7.049e-04			

A to Z	1.318e-02			
B to Z	1.159e-02			
C to Z	9.513e-03			
D to Z	8.091e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

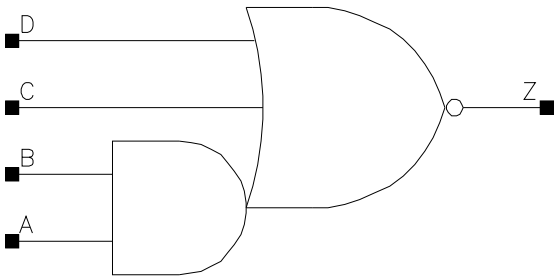
Pin Cycle (vdds)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X35_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P0	X35_P0
A	0.0007	0.0054
B	0.0007	0.0049
C	0.0007	0.0052
D	0.0007	0.0048

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X35_P0	X5_P0	X35_P0
A to Z ↓	0.0105	0.0108	3.7240	0.5453
A to Z ↑	0.0211	0.0195	8.5382	1.0873
B to Z ↓	0.0111	0.0111	3.7495	0.5501
B to Z ↑	0.0182	0.0162	8.4826	1.0857
C to Z ↓	0.0108	0.0145	2.2184	0.4282
C to Z ↑	0.0225	0.0215	8.0787	1.0304
D to Z ↓	0.0104	0.0134	2.2398	0.4275

D to Z ↑	0.0224	0.0204	8.0888	1.0331

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	6.586e-05	1.000e-20
X35_P0	4.728e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X35_P0
A (output stable)	7.276e-05	5.867e-04
B (output stable)	7.337e-05	6.255e-04
C (output stable)	4.086e-05	4.479e-04
D (output stable)	5.288e-05	5.904e-04
A to Z	1.246e-03	9.008e-03
B to Z	1.110e-03	7.656e-03
C to Z	1.753e-03	1.316e-02
D to Z	1.547e-03	1.100e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

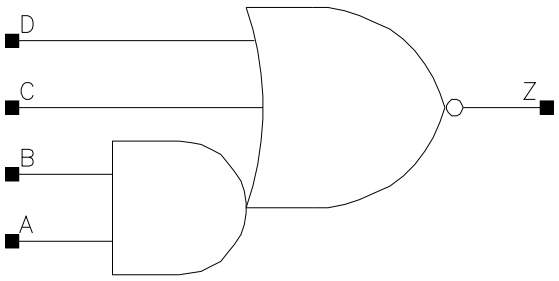
Pin Cycle (vdds)	X5_P0	X35_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X17_P0	1.200	2.448	2.9376
X34_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P0	X17_P0	X34_P0
A	0.0007	0.0029	0.0058
B	0.0007	0.0028	0.0055
C	0.0006	0.0025	0.0049
D	0.0007	0.0023	0.0045

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X17_P0	X4_P0	X17_P0
A to Z ↓	0.0123	0.0133	4.0607	1.0629
A to Z ↑	0.0218	0.0229	8.5957	2.1163
B to Z ↓	0.0135	0.0138	4.0864	1.0693
B to Z ↑	0.0194	0.0195	8.5146	2.1186
C to Z ↓	0.0116	0.0114	3.6170	0.8770
C to Z ↑	0.0162	0.0170	8.1104	2.0070

D to Z ↓	0.0099	0.0088	3.6770	0.8804
D to Z ↑	0.0156	0.0143	8.1186	2.0088
	X34_P0		**X34_P0**	
A to Z ↓	0.0131		0.5437	
A to Z ↑	0.0223		1.0767	
B to Z ↓	0.0138		0.5472	
B to Z ↑	0.0191		1.0727	
C to Z ↓	0.0117		0.4621	
C to Z ↑	0.0164		1.0195	
D to Z ↓	0.0091		0.4651	
D to Z ↑	0.0139		1.0205	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	6.122e-05	1.000e-20
X17_P0	2.436e-04	1.000e-20
X34_P0	4.775e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X17_P0	X34_P0
A (output stable)	1.838e-05	9.220e-05	1.796e-04
B (output stable)	2.002e-05	1.182e-04	2.219e-04
C (output stable)	5.695e-05	3.026e-04	5.826e-04
D (output stable)	1.026e-04	6.825e-04	1.268e-03
A to Z	1.584e-03	6.776e-03	1.306e-02
B to Z	1.447e-03	5.923e-03	1.148e-02
C to Z	1.080e-03	4.623e-03	8.786e-03
D to Z	9.044e-04	3.502e-03	6.681e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

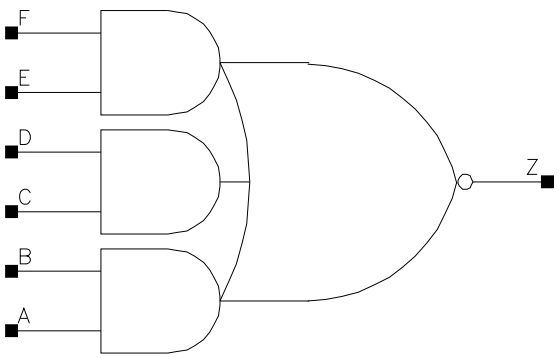
Pin Cycle (vdds)	X4_P0	X17_P0	X34_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X8_P0	1.200	2.176	2.6112
X13_P0	1.200	2.720	3.2640
X17_P0	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P0	X8_P0	X13_P0	X17_P0
A	0.0007	0.0014	0.0022	0.0029

B	0.0007	0.0013	0.0020	0.0027
C	0.0007	0.0014	0.0021	0.0027
D	0.0007	0.0013	0.0019	0.0025
E	0.0009	0.0013	0.0020	0.0026
F	0.0007	0.0013	0.0018	0.0024

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0150	0.0180	3.5807	2.0656
A to Z ↑	0.0323	0.0316	8.2597	3.8072
B to Z ↓	0.0165	0.0190	3.5991	2.0737
B to Z ↑	0.0297	0.0287	8.2492	3.8135
C to Z ↓	0.0135	0.0161	3.5558	2.0753
C to Z ↑	0.0283	0.0286	8.2979	3.8218
D to Z ↓	0.0148	0.0172	3.5800	2.0861
D to Z ↑	0.0258	0.0256	8.2570	3.8188
E to Z ↓	0.0102	0.0123	3.5028	2.0759
E to Z ↑	0.0228	0.0228	8.2038	3.7899
F to Z ↓	0.0109	0.0128	3.5371	2.0931
F to Z ↑	0.0203	0.0195	8.2475	3.7914
	X13_P0	**X17_P0**	**X13_P0**	**X17_P0**
A to Z ↓	0.0171	0.0173	1.4014	1.0674
A to Z ↑	0.0291	0.0293	2.5197	1.9244
B to Z ↓	0.0184	0.0182	1.4067	1.0713
B to Z ↑	0.0266	0.0263	2.5263	1.9243
C to Z ↓	0.0154	0.0154	1.4101	1.0587
C to Z ↑	0.0259	0.0263	2.5317	1.9357
D to Z ↓	0.0166	0.0161	1.4174	1.0644
D to Z ↑	0.0234	0.0233	2.5339	1.9319
E to Z ↓	0.0117	0.0116	1.4065	1.0601
E to Z ↑	0.0210	0.0211	2.5162	1.9168
F to Z ↓	0.0124	0.0118	1.4168	1.0681
F to Z ↑	0.0182	0.0181	2.5180	1.9227

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	1.035e-04	1.000e-20
X8_P0	2.148e-04	1.000e-20
X13_P0	3.060e-04	1.000e-20
X17_P0	4.076e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

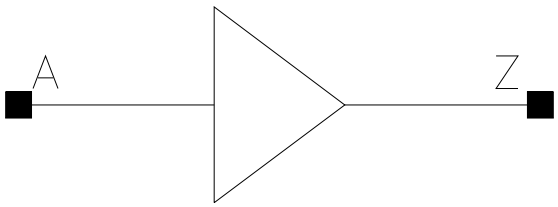
Pin Cycle (vdd)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	3.626e-05	8.707e-05	1.190e-04	1.624e-04
B (output stable)	3.997e-05	1.316e-04	1.548e-04	2.345e-04
C (output stable)	5.673e-05	1.232e-04	1.586e-04	2.194e-04
D (output stable)	6.197e-05	1.774e-04	1.998e-04	2.904e-04
E (output stable)	1.129e-04	2.804e-04	3.579e-04	4.852e-04
F (output stable)	1.309e-04	3.316e-04	4.007e-04	5.541e-04

A to Z	2.476e-03	5.192e-03	7.155e-03	9.506e-03
B to Z	2.308e-03	4.758e-03	6.596e-03	8.639e-03
C to Z	1.920e-03	4.195e-03	5.632e-03	7.509e-03
D to Z	1.776e-03	3.798e-03	5.130e-03	6.746e-03
E to Z	1.392e-03	3.096e-03	4.150e-03	5.507e-03
F to Z	1.264e-03	2.696e-03	3.654e-03	4.783e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X6_P0	1.200	0.408	0.4896
X8_P0	1.200	0.408	0.4896
X13_P0	1.200	0.544	0.6528
X16_P0	1.200	0.544	0.6528
X21_P0	1.200	0.680	0.8160
X25_P0	1.200	0.680	0.8160
X29_P0	1.200	0.952	1.1424
X33_P0	1.200	0.952	1.1424
X42_P0	1.200	1.088	1.3056
X50_P0	1.200	1.224	1.4688
X58_P0	1.200	1.496	1.7952
X67_P0	1.200	1.632	1.9584
X75_P0	1.200	1.768	2.1216
X84_P0	1.200	1.904	2.2848
X100_P0	1.200	2.312	2.7744
X134_P0	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0007	0.0007	0.0007	0.0007
	X16_P0	X21_P0	X25_P0	X29_P0
A	0.0007	0.0010	0.0010	0.0014
	X33_P0	X42_P0	X50_P0	X58_P0
A	0.0013	0.0015	0.0018	0.0027

	X67_P0	X75_P0	X84_P0	X100_P0
A	0.0027	0.0026	0.0026	0.0035
	X134_P0			
A	0.0044			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0219	0.0220	3.8494	2.7633
A to Z ↑	0.0174	0.0172	5.7283	4.1884
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0228	0.0254	2.0269	1.3150
A to Z ↑	0.0178	0.0201	2.9758	1.9514
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0275	0.0225	1.0363	0.8054
A to Z ↑	0.0213	0.0184	1.4904	1.1707
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0236	0.0228	0.6866	0.5815
A to Z ↑	0.0191	0.0175	0.9789	0.8350
	X33_P0	**X42_P0**	**X33_P0**	**X42_P0**
A to Z ↓	0.0238	0.0230	0.5148	0.4172
A to Z ↑	0.0182	0.0185	0.7322	0.5886
	X50_P0	**X58_P0**	**X50_P0**	**X58_P0**
A to Z ↓	0.0224	0.0208	0.3467	0.2987
A to Z ↑	0.0181	0.0171	0.4887	0.4205
	X67_P0	**X75_P0**	**X67_P0**	**X75_P0**
A to Z ↓	0.0218	0.0230	0.2625	0.2359
A to Z ↑	0.0178	0.0188	0.3678	0.3293
	X84_P0	**X100_P0**	**X84_P0**	**X100_P0**
A to Z ↓	0.0240	0.0225	0.2132	0.1791
A to Z ↑	0.0196	0.0184	0.2971	0.2484
	X134_P0		**X134_P0**	
A to Z ↓	0.0238		0.1381	
A to Z ↑	0.0197		0.1897	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	5.314e-05	1.000e-20
X6_P0	6.885e-05	1.000e-20
X8_P0	9.082e-05	1.000e-20
X13_P0	1.162e-04	1.000e-20
X16_P0	1.549e-04	1.000e-20
X21_P0	2.169e-04	1.000e-20
X25_P0	2.505e-04	1.000e-20
X29_P0	2.801e-04	1.000e-20
X33_P0	3.085e-04	1.000e-20
X42_P0	3.930e-04	1.000e-20
X50_P0	4.794e-04	1.000e-20
X58_P0	5.939e-04	1.000e-20
X67_P0	6.512e-04	1.000e-20
X75_P0	7.085e-04	1.000e-20

X84_P0	7.659e-04	1.000e-20
X100_P0	9.378e-04	1.000e-20
X134_P0	1.224e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	1.425e-03	1.602e-03	1.909e-03	2.574e-03
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	3.207e-03	4.204e-03	4.764e-03	5.379e-03
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	5.973e-03	7.478e-03	8.824e-03	1.069e-02
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	1.192e-02	1.342e-02	1.480e-02	1.750e-02
	X134_P0			
A to Z	2.416e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

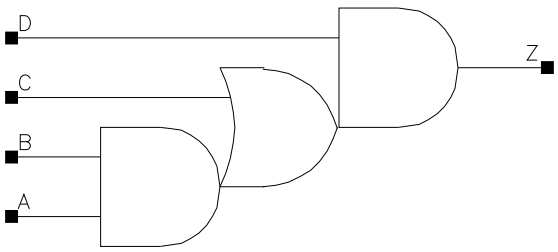
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P0			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.632	1.9584
X25_P0	1.200	1.768	2.1216
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0008	0.0019	0.0018	0.0018
B	0.0009	0.0016	0.0016	0.0016
C	0.0009	0.0021	0.0021	0.0021
D	0.0014	0.0017	0.0017	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0286	0.0268	2.0675	1.0231
A to Z ↑	0.0279	0.0261	3.0211	1.4703
B to Z ↓	0.0266	0.0245	2.0597	1.0214
B to Z ↑	0.0284	0.0261	3.0197	1.4686
C to Z ↓	0.0249	0.0229	2.0580	1.0198
C to Z ↑	0.0209	0.0190	2.9902	1.4547

D to Z ↓	0.0243	0.0211	2.0445	1.0134
D to Z ↑	0.0240	0.0207	2.9951	1.4571
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0295	0.0311	0.6934	0.5221
A to Z ↑	0.0287	0.0302	0.9946	0.7465
B to Z ↓	0.0273	0.0294	0.6927	0.5219
B to Z ↑	0.0288	0.0308	0.9924	0.7452
C to Z ↓	0.0257	0.0277	0.6911	0.5203
C to Z ↑	0.0212	0.0226	0.9823	0.7366
D to Z ↓	0.0229	0.0241	0.6853	0.5147
D to Z ↑	0.0228	0.0240	0.9841	0.7384

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.524e-04	1.000e-20
X17_P0	2.999e-04	1.000e-20
X25_P0	3.658e-04	1.000e-20
X33_P0	4.317e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	4.014e-05	8.379e-05	8.420e-05	7.373e-05
B (output stable)	4.936e-05	1.019e-04	1.025e-04	8.955e-05
C (output stable)	1.688e-04	2.628e-04	2.648e-04	2.578e-04
D (output stable)	9.539e-05	1.410e-04	1.424e-04	1.402e-04
A to Z	3.066e-03	5.620e-03	7.226e-03	8.681e-03
B to Z	2.909e-03	5.214e-03	6.808e-03	8.352e-03
C to Z	2.559e-03	4.503e-03	5.986e-03	7.335e-03
D to Z	3.133e-03	5.491e-03	6.887e-03	8.122e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

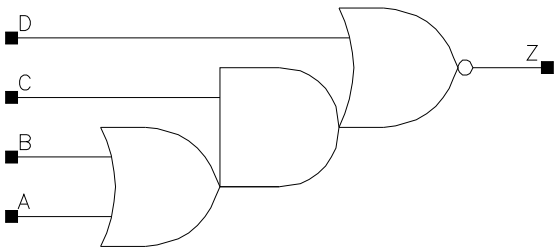
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.952	1.1424
X11_P0	1.200	1.496	1.7952
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X16_P0	X21_P0
A	0.0008	0.0014	0.0022	0.0029
B	0.0008	0.0014	0.0022	0.0028
C	0.0007	0.0014	0.0021	0.0028
D	0.0010	0.0014	0.0021	0.0028

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0131	0.0123	3.5070	1.8380
A to Z ↑	0.0270	0.0246	8.4059	4.3587
B to Z ↓	0.0125	0.0119	3.4368	1.8136
B to Z ↑	0.0259	0.0241	8.4177	4.3646
C to Z ↓	0.0120	0.0114	3.2343	1.6997
C to Z ↑	0.0168	0.0152	5.6823	2.9104

D to Z ↓	0.0069	0.0056	2.0792	1.0538
D to Z ↑	0.0162	0.0141	6.0632	3.1119
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0122	0.0125	1.2422	0.9527
A to Z ↑	0.0226	0.0240	2.8124	2.1665
B to Z ↓	0.0115	0.0118	1.2482	0.9542
B to Z ↑	0.0226	0.0233	2.8156	2.1689
C to Z ↓	0.0114	0.0115	1.1650	0.8897
C to Z ↑	0.0144	0.0146	1.9274	1.4472
D to Z ↓	0.0056	0.0057	0.7324	0.5579
D to Z ↑	0.0131	0.0130	2.0451	1.5476

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	8.922e-05	1.000e-20
X11_P0	1.698e-04	1.000e-20
X16_P0	2.409e-04	1.000e-20
X21_P0	3.183e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	2.268e-05	4.059e-05	5.284e-05	8.817e-05
B (output stable)	2.881e-05	4.858e-05	6.535e-05	1.097e-04
C (output stable)	6.542e-05	1.313e-04	1.786e-04	2.504e-04
D (output stable)	2.609e-04	5.440e-04	7.695e-04	1.098e-03
A to Z	2.039e-03	3.558e-03	4.955e-03	6.936e-03
B to Z	1.718e-03	3.048e-03	4.377e-03	5.898e-03
C to Z	1.538e-03	2.685e-03	3.815e-03	5.213e-03
D to Z	1.153e-03	2.045e-03	2.836e-03	3.772e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

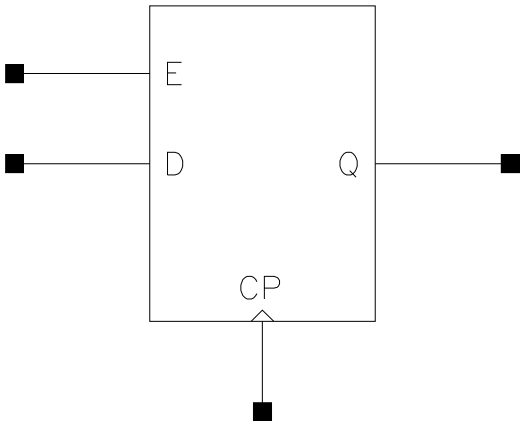
Pin Cycle (vdds)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.128	3.7536
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0010	0.0010	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0345	0.0394	2.0337	1.0457
CP to Q ↑	0.0437	0.0467	3.0066	1.5081
	X33_P0		**X33_P0**	
CP to Q ↓	0.0600		0.5210	
CP to Q ↑	0.0742		0.7471	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0478	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0284	0.0330	0.0271
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0463	0.0463	0.0463
D ↑	setup_rising to CP	0.0293	0.0293	0.0293
E ↓	hold_rising to CP	-0.0093	-0.0093	-0.0093
E ↑	hold_rising to CP	-0.0012	-0.0012	-0.0012
E ↓	setup_rising to CP	0.0537	0.0505	0.0537
E ↑	setup_rising to CP	0.0484	0.0484	0.0484

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	3.280e-04	1.000e-20
X17_P0	3.876e-04	1.000e-20
X33_P0	5.821e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

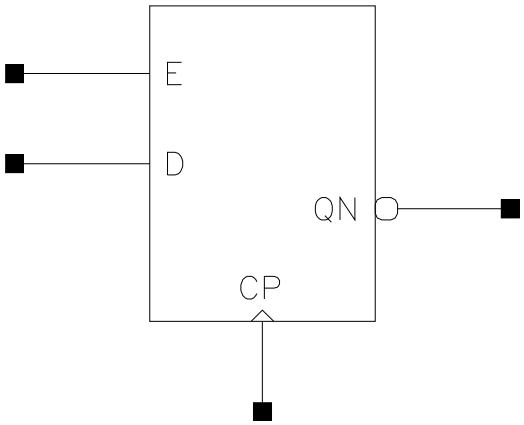
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	6.358e-03	6.358e-03	6.365e-03
Clock 100Mhz Data 25Mhz	8.391e-03	9.175e-03	1.125e-02
Clock 100Mhz Data 50Mhz	1.043e-02	1.199e-02	1.613e-02
Clock = 0 Data 100Mhz	4.051e-03	4.050e-03	4.050e-03
Clock = 1 Data 100Mhz	1.144e-03	1.144e-03	1.144e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.264	3.9168
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0010	0.0010	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0608	0.0572	2.1001	1.0076
CP to QN ↑	0.0473	0.0479	3.0613	1.4692
	X33_P0		**X33_P0**	
CP to QN ↓	0.0610		0.5221	
CP to QN ↑	0.0524		0.7498	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0478	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0271	0.0271	0.0318
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0463	0.0463	0.0463
D ↑	setup_rising to CP	0.0293	0.0293	0.0293
E ↓	hold_rising to CP	-0.0093	-0.0093	-0.0093
E ↑	hold_rising to CP	-0.0012	-0.0012	-0.0012
E ↓	setup_rising to CP	0.0537	0.0537	0.0505
E ↑	setup_rising to CP	0.0484	0.0484	0.0484

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	3.251e-04	1.000e-20
X17_P0	4.305e-04	1.000e-20
X33_P0	5.669e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

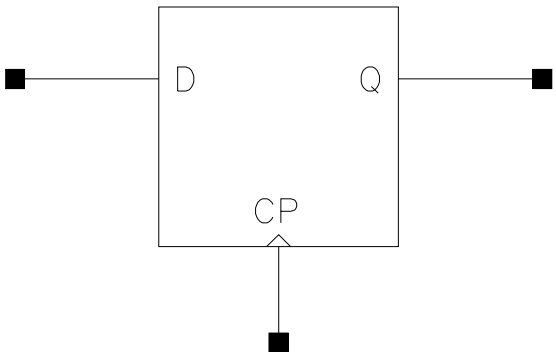
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	6.358e-03	6.357e-03	6.358e-03
Clock 100Mhz Data 25Mhz	8.400e-03	9.386e-03	1.124e-02
Clock 100Mhz Data 50Mhz	1.044e-02	1.242e-02	1.612e-02
Clock = 0 Data 100Mhz	4.050e-03	4.050e-03	4.050e-03
Clock = 1 Data 100Mhz	1.144e-03	1.144e-03	1.144e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.176	2.6112
X17_P0	1.200	2.448	2.9376
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0361	0.0395	2.0226	1.0381
CP to Q ↑	0.0445	0.0494	2.9229	1.4844
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to Q ↓	0.0494	0.0516	0.6106	0.5528
CP to Q ↑	0.0562	0.0573	0.8341	0.7589

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0431	0.0431	0.0431	0.0431
CP ↑	min_pulse_width to CP	0.0271	0.0318	0.0412	0.0424
D ↓	hold_rising to CP	0.0124	0.0124	0.0124	0.0124
D ↑	hold_rising to CP	0.0129	0.0129	0.0129	0.0129
D ↓	setup_rising to CP	0.0224	0.0219	0.0219	0.0214
D ↑	setup_rising to CP	0.0146	0.0146	0.0146	0.0146

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	2.559e-04	1.000e-20
X17_P0	3.226e-04	1.000e-20
X30_P0	4.203e-04	1.000e-20
X33_P0	4.388e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

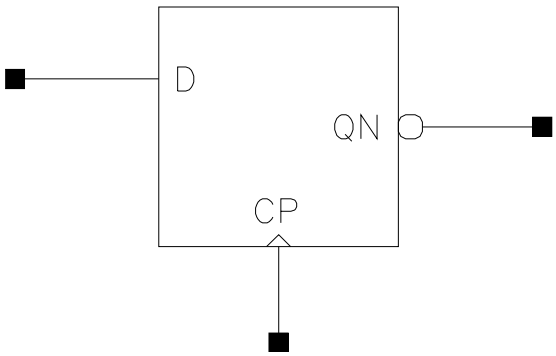
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	6.647e-03	6.677e-03	6.687e-03	6.692e-03
Clock 100Mhz Data 25Mhz	7.679e-03	8.733e-03	1.065e-02	1.112e-02
Clock 100Mhz Data 50Mhz	8.712e-03	1.079e-02	1.461e-02	1.555e-02
Clock = 0 Data 100Mhz	2.615e-03	2.695e-03	2.719e-03	2.732e-03
Clock = 1 Data 100Mhz	1.761e-05	1.799e-05	1.825e-05	1.840e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0349	0.0407	2.0753	1.0652
CP to QN ↑	0.0374	0.0398	2.9193	1.4823
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to QN ↓	0.0612	0.0614	0.5752	0.5202
CP to QN ↑	0.0491	0.0563	0.8092	0.7483

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0384	0.0417	0.0431	0.0431
CP ↑	min_pulse_width to CP	0.0271	0.0318	0.0271	0.0330
D ↓	hold_rising to CP	0.0146	0.0178	0.0124	0.0124
D ↑	hold_rising to CP	0.0151	0.0151	0.0129	0.0123
D ↓	setup_rising to CP	0.0175	0.0170	0.0219	0.0224
D ↑	setup_rising to CP	0.0146	0.0146	0.0146	0.0146

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	2.409e-04	1.000e-20
X17_P0	3.012e-04	1.000e-20
X30_P0	4.710e-04	1.000e-20
X33_P0	4.953e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

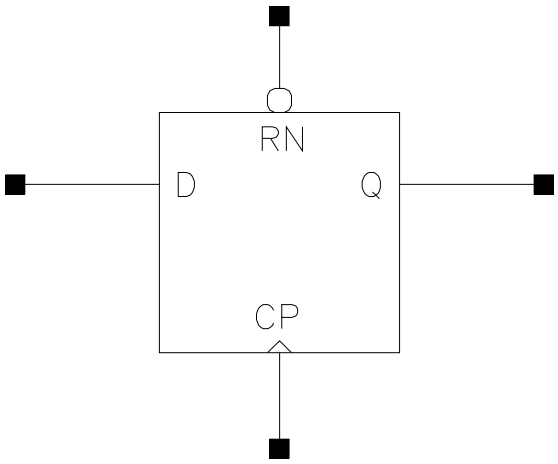
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	6.405e-03	6.407e-03	6.503e-03	6.544e-03
Clock 100Mhz Data 25Mhz	7.348e-03	8.205e-03	9.901e-03	1.053e-02
Clock 100Mhz Data 50Mhz	8.292e-03	1.000e-02	1.330e-02	1.451e-02
Clock = 0 Data 100Mhz	2.360e-03	2.361e-03	2.498e-03	2.528e-03
Clock = 1 Data 100Mhz	1.746e-05	1.786e-05	1.808e-05	1.815e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0006	0.0006
RN	0.0008	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0413	0.0512	1.0480	0.6177
CP to Q ↑	0.0511	0.0573	1.4892	0.8375
RN to Q ↓	0.0690	0.0904	1.0837	0.6355

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0331	0.0424
D ↓	hold_rising to CP	0.0124	0.0124
D ↑	hold_rising to CP	0.0102	0.0102
D ↓	setup_rising to CP	0.0272	0.0272
D ↑	setup_rising to CP	0.0174	0.0174
RN ↓	min_pulse_width to RN	0.0854	0.1050
RN ↑	recovery_rising to CP	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0001	-0.0001

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P0	3.592e-04	1.000e-20
X30_P0	4.672e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

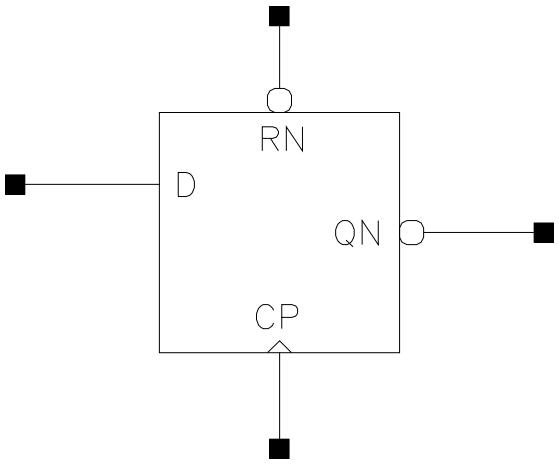
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	7.098e-03	7.097e-03
Clock 100Mhz Data 25Mhz	9.306e-03	1.119e-02
Clock 100Mhz Data 50Mhz	1.151e-02	1.529e-02
Clock = 0 Data 100Mhz	3.217e-03	3.220e-03
Clock = 1 Data 100Mhz	1.836e-05	1.861e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0006	0.0006
RN	0.0008	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0593	0.0639	1.0012	0.5769
CP to QN ↑	0.0476	0.0514	1.4570	0.8126
RN to QN ↑	0.0711	0.0761	1.4607	0.8148

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0271	0.0318
D ↓	hold_rising to CP	0.0124	0.0124
D ↑	hold_rising to CP	0.0102	0.0102
D ↓	setup_rising to CP	0.0272	0.0272
D ↑	setup_rising to CP	0.0174	0.0174
RN ↓	min_pulse_width to RN	0.0708	0.0708
RN ↑	recovery_rising to CP	0.0125	0.0125
RN ↑	removal_rising to CP	-0.0001	-0.0006

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P0	3.971e-04	1.000e-20
X30_P0	4.814e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

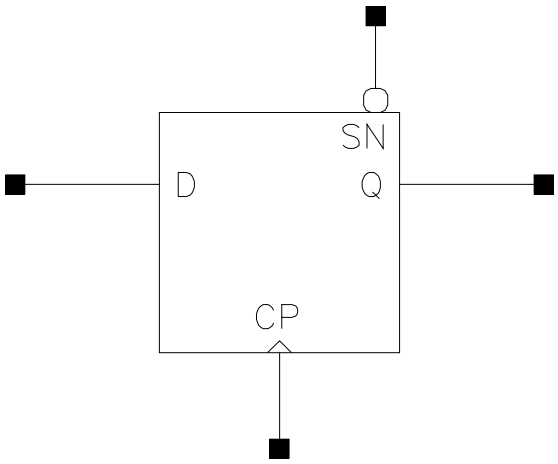
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	7.098e-03	7.090e-03
Clock 100Mhz Data 25Mhz	9.451e-03	1.068e-02
Clock 100Mhz Data 50Mhz	1.180e-02	1.428e-02
Clock = 0 Data 100Mhz	3.258e-03	3.248e-03
Clock = 1 Data 100Mhz	1.820e-05	1.841e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0006	0.0006
SN	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0416	0.0521	1.0488	0.6158
CP to Q ↑	0.0507	0.0572	1.4902	0.8369
SN to Q ↑	0.0525	0.0612	1.4941	0.8377

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0491	0.0491
CP ↑	min_pulse_width to CP	0.0331	0.0424
D ↓	hold_rising to CP	0.0129	0.0129
D ↑	hold_rising to CP	0.0102	0.0129
D ↓	setup_rising to CP	0.0295	0.0262
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0527	0.0625
SN ↑	recovery_rising to CP	0.0032	0.0028
SN ↑	removal_rising to CP	0.0265	0.0265

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P0	3.389e-04	1.000e-20
X30_P0	4.256e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

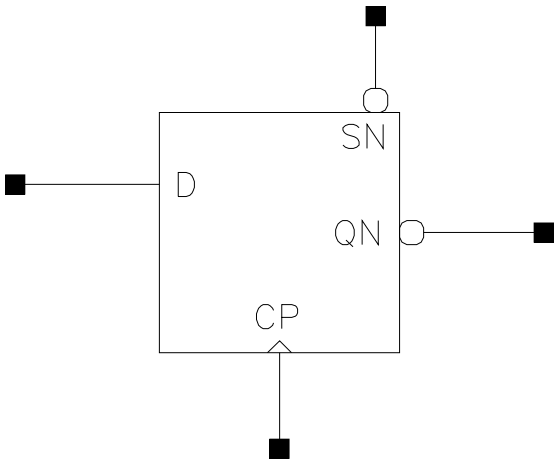
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	7.172e-03	7.158e-03
Clock 100Mhz Data 25Mhz	9.378e-03	1.127e-02
Clock 100Mhz Data 50Mhz	1.158e-02	1.539e-02
Clock = 0 Data 100Mhz	3.186e-03	3.186e-03
Clock = 1 Data 100Mhz	1.852e-05	1.852e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0006	0.0006
SN	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0588	0.0633	1.0045	0.5775
CP to QN ↑	0.0480	0.0517	1.4545	0.8110
SN to QN ↓	0.0598	0.0643	1.0046	0.5770

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0491	0.0491
CP ↑	min_pulse_width to CP	0.0271	0.0318
D ↓	hold_rising to CP	0.0134	0.0134
D ↑	hold_rising to CP	0.0102	0.0102
D ↓	setup_rising to CP	0.0295	0.0295
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0425	0.0452
SN ↑	recovery_rising to CP	0.0032	0.0032
SN ↑	removal_rising to CP	0.0265	0.0265

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P0	4.084e-04	1.000e-20
X30_P0	5.136e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

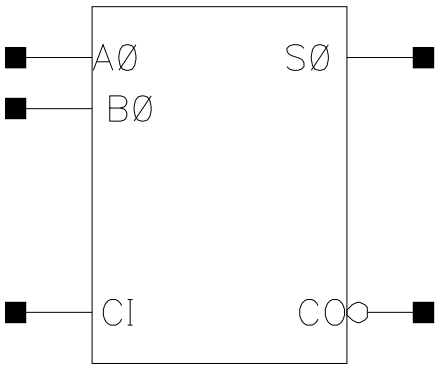
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	7.171e-03	7.166e-03
Clock 100Mhz Data 25Mhz	9.503e-03	1.070e-02
Clock 100Mhz Data 50Mhz	1.184e-02	1.423e-02
Clock = 0 Data 100Mhz	3.186e-03	3.187e-03
Clock = 1 Data 100Mhz	1.820e-05	1.820e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_P0	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_-P0	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_-P0	1.200	3.672	4.4064
C12T28SOI_LLS1_-FA1X33_P0	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0	0.0028	0.0058	0.0026	0.0052
B0	0.0026	0.0057	0.0028	0.0049
CI	0.0019	0.0043	0.0020	0.0035

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0
A0 to CO ↓	0.0382	0.0412	2.1095	0.5518
A0 to CO ↑	0.0298	0.0308	3.0174	0.7728
A0 to S0 ↓	0.0403	0.0507	2.1007	0.5415
A0 to S0 ↑	0.0416	0.0508	2.9915	0.7647
B0 to CO ↓	0.0377	0.0416	2.1148	0.5541
B0 to CO ↑	0.0306	0.0319	3.0176	0.7704
B0 to S0 ↓	0.0407	0.0516	2.1012	0.5418
B0 to S0 ↑	0.0419	0.0516	2.9937	0.7650
CI to CO ↓	0.0368	0.0409	2.1145	0.5518
CI to CO ↑	0.0303	0.0308	3.0141	0.7721
CI to S0 ↓	0.0403	0.0509	2.1029	0.5416
CI to S0 ↑	0.0418	0.0517	2.9928	0.7645
	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0 to CO ↓	0.0255	0.0310	4.1751	0.7196
A0 to CO ↑	0.0224	0.0253	3.0548	0.7641
A0 to S0 ↓	0.0549	0.0670	2.2569	0.5630
A0 to S0 ↑	0.0507	0.0543	3.1103	0.7749
B0 to CO ↓	0.0264	0.0321	4.1746	0.7198
B0 to CO ↑	0.0209	0.0243	3.0507	0.7642
B0 to S0 ↓	0.0548	0.0683	2.2564	0.5630
B0 to S0 ↑	0.0506	0.0555	3.1103	0.7751
CI to CO ↓	0.0264	0.0449	4.1669	0.7270
CI to CO ↑	0.0232	0.0277	3.1208	0.7697
CI to S0 ↓	0.0313	0.0402	2.2592	0.5634
CI to S0 ↑	0.0269	0.0268	3.1108	0.7752

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_FA1X8_P0	3.309e-04	1.000e-20
C12T28SOI_LL_FA1X33_P0	8.957e-04	1.000e-20
C12T28SOI_LLS1_FA1X8_P0	7.288e-04	1.000e-20
C12T28SOI_LLS1_FA1X33_P0	1.509e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0 to CO	3.224e-03	9.832e-03	4.877e-03	1.238e-02
A0 to S0	3.209e-03	1.015e-02	6.522e-03	1.525e-02
B0 to CO	3.266e-03	1.004e-02	4.890e-03	1.249e-02
B0 to S0	3.197e-03	1.017e-02	6.583e-03	1.547e-02
CI to CO	3.319e-03	1.019e-02	3.506e-03	1.133e-02
CI to S0	3.203e-03	1.019e-02	3.971e-03	1.213e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00

A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X33_P0	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X33_P0
A0	0.0010	0.0029
B0	0.0009	0.0025

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
A0 to CO ↓	0.0295	0.0263	2.1023	0.5197
A0 to CO ↑	0.0276	0.0249	2.9939	0.7654
A0 to S0 ↓	0.0384	0.0356	2.0627	0.5198
A0 to S0 ↑	0.0369	0.0409	2.9576	0.7574
B0 to CO ↓	0.0287	0.0244	2.0991	0.5162
B0 to CO ↑	0.0296	0.0260	2.9934	0.7653
B0 to S0 ↓	0.0399	0.0357	2.0628	0.5195
B0 to S0 ↑	0.0364	0.0393	2.9567	0.7575

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	2.025e-04	1.000e-20
X33_P0	8.752e-04	1.000e-20

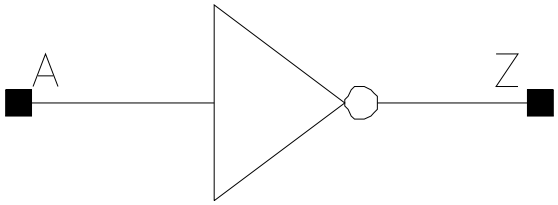
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X33_P0
A0 to CO	2.470e-03	8.350e-03
A0 to S0	2.322e-03	8.333e-03
B0 to CO	2.518e-03	8.577e-03
B0 to S0	2.306e-03	8.145e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X8_P0	X33_P0
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.272	0.3264
X6_P0	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X13_P0	1.200	0.408	0.4896
X17_P0	1.200	0.408	0.4896
X21_P0	1.200	0.544	0.6528
X25_P0	1.200	0.544	0.6528
X29_P0	1.200	0.680	0.8160
X33_P0	1.200	0.680	0.8160
X50_P0	1.200	0.952	1.1424
X58_P0	1.200	1.088	1.3056
X67_P0	1.200	1.224	1.4688
X75_P0	1.200	1.360	1.6320
X84_P0	1.200	1.496	1.7952
X100_P0	1.200	1.768	2.1216
X134_P0	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0005	0.0006	0.0008	0.0011
	X17_P0	X21_P0	X25_P0	X29_P0
A	0.0014	0.0019	0.0021	0.0025
	X33_P0	X50_P0	X58_P0	X67_P0
A	0.0028	0.0042	0.0049	0.0057
	X75_P0	X84_P0	X100_P0	X134_P0

A	0.0065	0.0074	0.0090	0.0125

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0061	0.0058	4.0151	3.0618
A to Z ↑	0.0113	0.0101	5.8599	4.3973
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0052	0.0042	2.0728	1.3510
A to Z ↑	0.0091	0.0083	3.0266	1.9976
	X17_P0	**X21_P0**	**X17_P0**	**X21_P0**
A to Z ↓	0.0043	0.0046	1.0277	0.8306
A to Z ↑	0.0078	0.0083	1.4852	1.1989
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0046	0.0043	0.7029	0.5980
A to Z ↑	0.0079	0.0077	0.9990	0.8561
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0043	0.0044	0.5292	0.3573
A to Z ↑	0.0073	0.0073	0.7497	0.5016
	X58_P0	**X67_P0**	**X58_P0**	**X67_P0**
A to Z ↓	0.0048	0.0047	0.3094	0.2718
A to Z ↑	0.0076	0.0074	0.4324	0.3791
	X75_P0	**X84_P0**	**X75_P0**	**X84_P0**
A to Z ↓	0.0051	0.0052	0.2446	0.2215
A to Z ↑	0.0079	0.0079	0.3392	0.3066
	X100_P0	**X134_P0**	**X100_P0**	**X134_P0**
A to Z ↓	0.0058	0.0065	0.1880	0.1459
A to Z ↑	0.0084	0.0091	0.2585	0.1983

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.754e-05	1.000e-20
X6_P0	3.962e-05	1.000e-20
X8_P0	6.370e-05	1.000e-20
X13_P0	9.102e-05	1.000e-20
X17_P0	1.301e-04	1.000e-20
X21_P0	1.535e-04	1.000e-20
X25_P0	1.881e-04	1.000e-20
X29_P0	2.156e-04	1.000e-20
X33_P0	2.454e-04	1.000e-20
X50_P0	3.597e-04	1.000e-20
X58_P0	4.170e-04	1.000e-20
X67_P0	4.742e-04	1.000e-20
X75_P0	5.314e-04	1.000e-20
X84_P0	5.887e-04	1.000e-20
X100_P0	7.032e-04	1.000e-20
X134_P0	9.321e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0

A to Z	5.328e-04	6.751e-04	9.287e-04	1.331e-03
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	1.754e-03	2.265e-03	2.666e-03	3.008e-03
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	3.350e-03	4.970e-03	5.925e-03	6.624e-03
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	7.612e-03	8.379e-03	1.022e-02	1.397e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

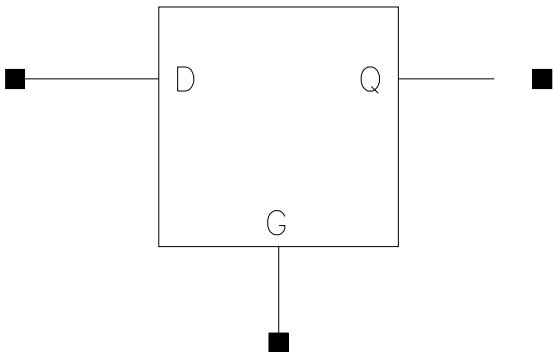
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X23_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P0	X23_P0
D	0.0005	0.0012
G	0.0011	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X23_P0	X8_P0	X23_P0
D to Q ↓	0.0437	0.0336	2.1021	1.0239
D to Q ↑	0.0294	0.0289	2.9425	0.7813
G to Q ↓	0.0462	0.0365	2.0951	1.0227
G to Q ↑	0.0285	0.0251	2.9426	0.7820

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X23_P0
D ↓	hold_falling to G	-0.0013	0.0058
D ↑	hold_falling to G	0.0045	0.0041
D ↓	setup_falling to G	0.0414	0.0296
D ↑	setup_falling to G	0.0334	0.0353
G ↑	min_pulse_width to G	0.0409	0.0399

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.443e-04	1.000e-20
X23_P0	3.645e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X23_P0
D (output stable)	1.248e-05	5.436e-05
G (output stable)	8.716e-04	1.751e-03
D to Q	4.137e-03	7.980e-03
G to Q	4.001e-03	7.468e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

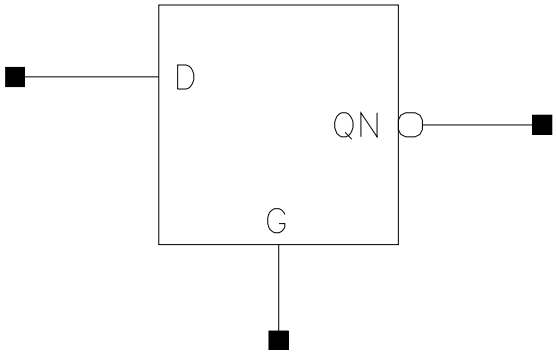
Pin Cycle (vdds)	X8_P0	X23_P0
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P0
D	0.0005
G	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P0	X17_P0
D to QN ↓	0.0382	1.0056
D to QN ↑	0.0487	1.4455
G to QN ↓	0.0369	1.0047
G to QN ↑	0.0494	1.4468

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P0
D ↓	hold_falling to G	-0.0062
D ↑	hold_falling to G	0.0019
D ↓	setup_falling to G	0.0370
D ↑	setup_falling to G	0.0290
G ↑	min_pulse_width to G	0.0317

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P0	2.369e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X17_P0
D (output stable)	1.234e-05
G (output stable)	1.065e-03
D to QN	4.931e-03
G to QN	4.828e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

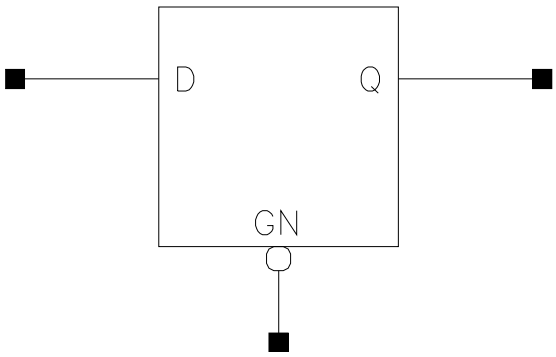
Pin Cycle (vdds)	X17_P0
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
D	0.0005	0.0007	0.0016
GN	0.0010	0.0013	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D to Q ↓	0.0443	0.0375	2.1058	1.0432
D to Q ↑	0.0299	0.0280	2.9474	1.5082
GN to Q ↓	0.0404	0.0333	2.1085	1.0439
GN to Q ↑	0.0440	0.0420	2.9429	1.5072

	X33_P0		X33_P0	
D to Q ↓	0.0362		0.5336	
D to Q ↑	0.0235		0.7550	
GN to Q ↓	0.0313		0.5335	
GN to Q ↑	0.0319		0.7547	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X17_P0	X33_P0
D ↓	hold_rising to GN	-0.0042	-0.0030	-0.0030
D ↑	hold_rising to GN	0.0057	0.0074	0.0105
D ↓	setup_rising to GN	0.0497	0.0455	0.0400
D ↑	setup_rising to GN	0.0298	0.0239	0.0191
GN ↓	min_pulse_width to GN	0.0554	0.0468	0.0440

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.430e-04	1.000e-20
X17_P0	2.401e-04	1.000e-20
X33_P0	4.241e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
D (output stable)	1.244e-05	2.070e-05	5.936e-05
GN (output stable)	8.669e-04	1.195e-03	1.570e-03
D to Q	4.166e-03	5.963e-03	9.596e-03
GN to Q	5.727e-03	7.907e-03	1.176e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

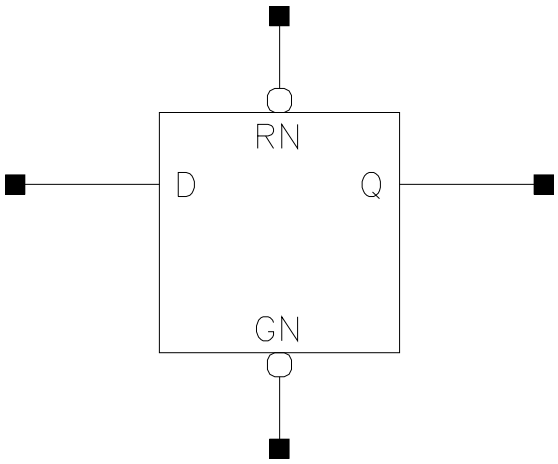
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.496	1.7952
X33_P0	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X33_P0
D	0.0005	0.0012
GN	0.0012	0.0022
RN	0.0005	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
D to Q ↓	0.0411	0.0364	2.0649	0.5359
D to Q ↑	0.0388	0.0501	2.9987	0.7772

GN to Q ↓	0.0378	0.0337	2.0661	0.5366
GN to Q ↑	0.0506	0.0527	2.9991	0.7767
RN to Q ↓	0.0338	0.0629	2.0099	0.5694
RN to Q ↑	0.0405	0.0552	2.9999	0.7778

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X33_P0
D ↓	hold_rising to GN	-0.0052	0.0023
D ↑	hold_rising to GN	0.0010	-0.0137
D ↓	setup_rising to GN	0.0449	0.0402
D ↑	setup_rising to GN	0.0362	0.0556
GN ↓	min_pulse_width to GN	0.0511	0.0542
RN ↓	min_pulse_width to RN	0.0398	0.0735
RN ↑	recovery_rising to GN	0.0389	0.0611
RN ↑	removal_rising to GN	-0.0244	-0.0385

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.601e-04	1.000e-20
X33_P0	4.276e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X33_P0
D (output stable)	3.536e-05	5.817e-05
GN (output stable)	9.628e-04	1.538e-03
RN (output stable)	4.020e-05	7.850e-05
D to Q	4.193e-03	1.172e-02
GN to Q	5.886e-03	1.434e-02
RN to Q	3.046e-03	9.498e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

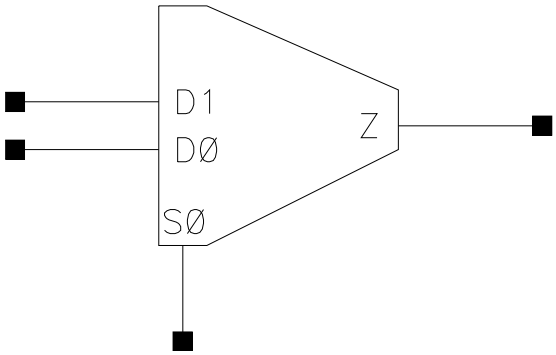
Pin Cycle (vdds)	X8_P0	X33_P0
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
D0	0.0007	0.0010	0.0013	0.0018
D1	0.0007	0.0010	0.0013	0.0017
S0	0.0012	0.0013	0.0015	0.0023

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D0 to Z ↓	0.0342	0.0299	2.0921	1.0238
D0 to Z ↑	0.0278	0.0251	3.0203	1.4754
D1 to Z ↓	0.0322	0.0292	2.0843	1.0225
D1 to Z ↑	0.0252	0.0236	3.0135	1.4735
S0 to Z ↓	0.0294	0.0281	2.0820	1.0204
S0 to Z ↑	0.0281	0.0279	3.0159	1.4720

	X25_P0	X33_P0	X25_P0	X33_P0
D0 to Z ↓	0.0322	0.0287	0.7019	0.5268
D0 to Z ↑	0.0268	0.0247	0.9914	0.7426
D1 to Z ↓	0.0341	0.0296	0.7039	0.5269
D1 to Z ↑	0.0259	0.0240	0.9902	0.7416
S0 to Z ↓	0.0323	0.0293	0.7005	0.5262
S0 to Z ↑	0.0310	0.0281	0.9898	0.7426

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.699e-04	1.000e-20
X17_P0	3.361e-04	1.000e-20
X25_P0	4.341e-04	1.000e-20
X33_P0	6.623e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	8.363e-04	1.338e-03	1.517e-03	2.192e-03
D1 (output stable)	7.194e-04	1.281e-03	1.637e-03	2.256e-03
S0 (output stable)	1.012e-03	1.128e-03	1.439e-03	1.844e-03
D0 to Z	2.792e-03	4.714e-03	7.303e-03	9.190e-03
D1 to Z	2.573e-03	4.570e-03	7.366e-03	9.120e-03
S0 to Z	3.203e-03	4.976e-03	8.100e-03	9.917e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

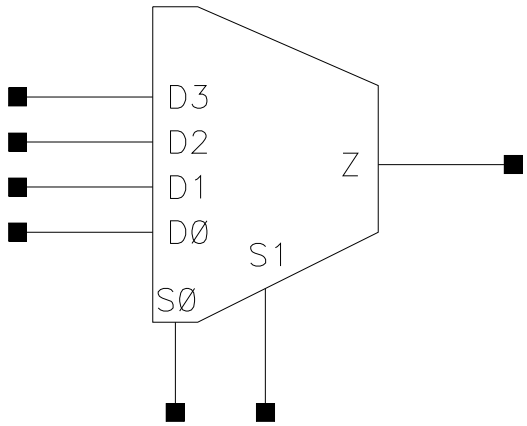
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.312	2.7744
X31_P0	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P0	X31_P0
D0	0.0005	0.0013
D1	0.0005	0.0013
D2	0.0005	0.0013
D3	0.0005	0.0013
S0	0.0017	0.0034
S1	0.0011	0.0022

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X31_P0	X8_P0	X31_P0

D0 to Z ↓	0.0575	0.0578	2.1769	0.5995
D0 to Z ↑	0.0399	0.0416	3.0475	0.8178
D1 to Z ↓	0.0570	0.0580	2.1744	0.5995
D1 to Z ↑	0.0401	0.0415	3.0481	0.8182
D2 to Z ↓	0.0619	0.0539	2.1895	0.5942
D2 to Z ↑	0.0425	0.0384	3.0588	0.8119
D3 to Z ↓	0.0617	0.0535	2.1892	0.5932
D3 to Z ↑	0.0421	0.0394	3.0553	0.8144
S0 to Z ↓	0.0634	0.0629	2.1805	0.5962
S0 to Z ↑	0.0491	0.0505	3.0539	0.8168
S1 to Z ↓	0.0465	0.0448	2.1824	0.5965
S1 to Z ↑	0.0388	0.0396	3.0524	0.8164

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.635e-04	1.000e-20
X31_P0	5.383e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X31_P0
D0 (output stable)	1.982e-05	1.053e-04
D1 (output stable)	1.956e-05	9.615e-05
D2 (output stable)	2.255e-05	9.975e-05
D3 (output stable)	2.245e-05	9.906e-05
S0 (output stable)	1.368e-03	3.005e-03
S1 (output stable)	1.201e-03	2.595e-03
D0 to Z	3.156e-03	1.112e-02
D1 to Z	3.144e-03	1.118e-02
D2 to Z	3.381e-03	1.036e-02
D3 to Z	3.370e-03	1.039e-02
S0 to Z	4.660e-03	1.403e-02
S1 to Z	3.901e-03	1.170e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

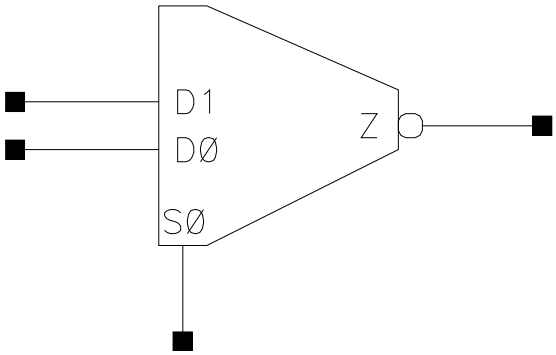
Pin Cycle (vdds)	X8_P0	X31_P0
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.816	0.9792
X5_P0	1.200	0.952	1.1424
X10_P0	1.200	1.768	2.1216
X16_P0	1.200	2.448	2.9376
X21_P0	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P0	X5_P0	X10_P0	X16_P0
D0	0.0005	0.0007	0.0015	0.0022
D1	0.0005	0.0007	0.0014	0.0022
S0	0.0011	0.0018	0.0024	0.0035
	X21_P0			
D0	0.0029			
D1	0.0029			
S0	0.0040			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X5_P0	X3_P0	X5_P0
D0 to Z ↓	0.0116	0.0116	6.8506	4.1116

D0 to Z ↑	0.0198	0.0172	12.4591	6.2957
D1 to Z ↓	0.0115	0.0113	6.8000	3.9426
D1 to Z ↑	0.0204	0.0177	12.4828	6.5115
S0 to Z ↓	0.0183	0.0151	6.7979	4.0148
S0 to Z ↑	0.0199	0.0164	12.4463	6.3884
	X10_P0	**X16_P0**	**X10_P0**	**X16_P0**
D0 to Z ↓	0.0132	0.0122	1.9310	1.2626
D0 to Z ↑	0.0188	0.0176	2.9219	1.9249
D1 to Z ↓	0.0120	0.0118	1.8780	1.2396
D1 to Z ↑	0.0186	0.0180	2.9642	1.9438
S0 to Z ↓	0.0184	0.0157	1.8962	1.2465
S0 to Z ↑	0.0195	0.0167	2.9347	1.9302
	X21_P0		**X21_P0**	
D0 to Z ↓	0.0120		0.9622	
D0 to Z ↑	0.0172		1.4571	
D1 to Z ↓	0.0118		0.9398	
D1 to Z ↑	0.0179		1.4520	
S0 to Z ↓	0.0165		0.9476	
S0 to Z ↑	0.0171		1.4501	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	5.783e-05	1.000e-20
X5_P0	1.444e-04	1.000e-20
X10_P0	2.580e-04	1.000e-20
X16_P0	4.103e-04	1.000e-20
X21_P0	5.027e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	1.237e-05	3.008e-05	8.750e-05	1.351e-04
D1 (output stable)	1.235e-05	3.041e-05	7.261e-05	1.288e-04
S0 (output stable)	8.739e-04	1.383e-03	2.154e-03	3.546e-03
D0 to Z	7.756e-04	1.330e-03	3.265e-03	4.593e-03
D1 to Z	7.777e-04	1.317e-03	3.114e-03	4.541e-03
S0 to Z	1.497e-03	2.366e-03	4.601e-03	6.790e-03
	X21_P0			
D0 (output stable)	1.727e-04			
D1 (output stable)	1.725e-04			
S0 (output stable)	3.863e-03			
D0 to Z	5.933e-03			
D1 to Z	5.990e-03			
S0 to Z	8.195e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

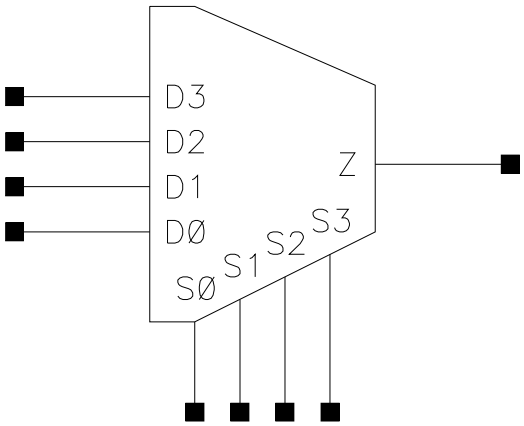
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P0			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	1.768	2.1216
X27_P0	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P0	X27_P0
D0	0.0006	0.0018
D1	0.0006	0.0019
D2	0.0006	0.0018
D3	0.0006	0.0018
S0	0.0006	0.0017
S1	0.0007	0.0017
S2	0.0006	0.0017
S3	0.0006	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	X27_P0	X7_P0	X27_P0
D0 to Z ↓	0.0450	0.0361	3.4503	0.9374
D0 to Z ↑	0.0334	0.0276	2.9650	0.7397
D1 to Z ↓	0.0415	0.0335	3.4466	0.9368
D1 to Z ↑	0.0300	0.0241	2.9526	0.7362
D2 to Z ↓	0.0458	0.0350	3.4537	0.9373
D2 to Z ↑	0.0330	0.0262	2.9765	0.7418
D3 to Z ↓	0.0424	0.0324	3.4475	0.9361
D3 to Z ↑	0.0296	0.0226	2.9626	0.7380
S0 to Z ↓	0.0437	0.0342	3.4493	0.9372
S0 to Z ↑	0.0356	0.0291	2.9659	0.7391
S1 to Z ↓	0.0405	0.0316	3.4470	0.9368
S1 to Z ↑	0.0320	0.0252	2.9526	0.7361
S2 to Z ↓	0.0445	0.0330	3.4528	0.9364
S2 to Z ↑	0.0352	0.0276	2.9747	0.7411
S3 to Z ↓	0.0415	0.0305	3.4471	0.9353
S3 to Z ↑	0.0316	0.0238	2.9629	0.7377

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X7_P0	1.537e-04	1.000e-20
X27_P0	6.656e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X7_P0	X27_P0
D0 (output stable)	3.939e-04	1.236e-03
D1 (output stable)	3.523e-04	1.064e-03
D2 (output stable)	3.712e-04	1.163e-03
D3 (output stable)	3.294e-04	9.905e-04
S0 (output stable)	3.858e-04	1.184e-03
S1 (output stable)	3.433e-04	1.022e-03
S2 (output stable)	3.632e-04	1.110e-03
S3 (output stable)	3.205e-04	9.518e-04
D0 to Z	3.319e-03	1.013e-02
D1 to Z	2.983e-03	8.953e-03
D2 to Z	3.283e-03	9.247e-03
D3 to Z	2.952e-03	8.075e-03
S0 to Z	3.258e-03	9.741e-03
S1 to Z	2.925e-03	8.600e-03
S2 to Z	3.220e-03	8.830e-03
S3 to Z	2.893e-03	7.726e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

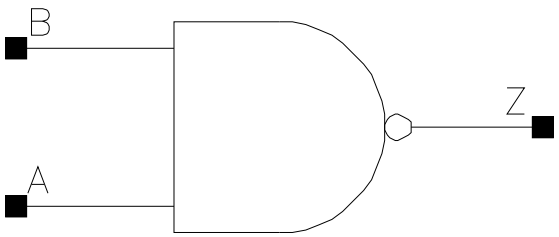
Pin Cycle (vdds)	X7_P0	X27_P0
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P0	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P0	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P0	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P0	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P0	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P0	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P0	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P0	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P0	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P0	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P0	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P0	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P0	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P0	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P0	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P0	C12T28SOI_LL_-NAND2X5_P0	C12T28SOI_LL_-NAND2X7_P0	C12T28SOI_LL_-NAND2X10_P0
A	0.0005	0.0006	0.0007	0.0012
B	0.0005	0.0006	0.0007	0.0011
	C12T28SOI_LL_-NAND2X13_P0	C12T28SOI_LL_-NAND2X17_P0	C12T28SOI_LL_-NAND2X20_P0	C12T28SOI_LL_-NAND2X24_P0
A	0.0015	0.0019	0.0022	0.0026
B	0.0014	0.0018	0.0020	0.0024
	C12T28SOI_LL_-NAND2X27_P0	C12T28SOI_LL_-NAND2X42_P0	C12T28SOI_LL_-NAND2X47_P0	C12T28SOI_LL_-NAND2X50_P0
A	0.0029	0.0009	0.0009	0.0009
B	0.0027	0.0010	0.0010	0.0010
	C12T28SOI_LL_-NAND2X58_P0	C12T28SOI_LL_-NAND2X67_P0	C12T28SOI_-LLBR0D8_-NAND2X7_P0	C12T28SOI_-LLBR0D8_-NAND2X14_P0
A	0.0009	0.0009	0.0007	0.0014
B	0.0010	0.0010	0.0007	0.0013
	C12T28SOI_LLS_-NAND2X40_P0	C12T28SOI_LLS_-NAND2X54_P0		
A	0.0044	0.0058		
B	0.0040	0.0054		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P0	**C12T28SOI_LL_-NAND2X5_P0**	**C12T28SOI_LL_-NAND2X3_P0**	**C12T28SOI_LL_-NAND2X5_P0**
A to Z ↓	0.0088	0.0080	6.6808	4.2551
A to Z ↑	0.0131	0.0116	5.8816	3.7373
B to Z ↓	0.0100	0.0088	6.7295	4.2860
B to Z ↑	0.0119	0.0102	5.9127	3.7564
	C12T28SOI_LL_-NAND2X7_P0	**C12T28SOI_LL_-NAND2X10_P0**	**C12T28SOI_LL_-NAND2X7_P0**	**C12T28SOI_LL_-NAND2X10_P0**
A to Z ↓	0.0080	0.0089	3.5570	2.3634
A to Z ↑	0.0111	0.0121	3.0058	1.9822
B to Z ↓	0.0088	0.0086	3.5808	2.3802
B to Z ↑	0.0097	0.0096	3.0332	1.9947
	C12T28SOI_LL_-NAND2X13_P0	**C12T28SOI_LL_-NAND2X17_P0**	**C12T28SOI_LL_-NAND2X13_P0**	**C12T28SOI_LL_-NAND2X17_P0**
A to Z ↓	0.0086	0.0085	1.8099	1.4430

A to Z ↑	0.0112	0.0113	1.4801	1.1962
B to Z ↓	0.0084	0.0087	1.8214	1.4529
B to Z ↑	0.0088	0.0094	1.4898	1.2021
	C12T28SOI_LL_-NAND2X20_P0	**C12T28SOI_LL_-NAND2X24_P0**	**C12T28SOI_LL_-NAND2X20_P0**	**C12T28SOI_LL_-NAND2X24_P0**
A to Z ↓	0.0084	0.0086	1.2334	1.0510
A to Z ↑	0.0109	0.0112	0.9954	0.8528
B to Z ↓	0.0088	0.0085	1.2411	1.0573
B to Z ↑	0.0090	0.0089	1.0027	0.8571
	C12T28SOI_LL_-NAND2X27_P0	**C12T28SOI_LL_-NAND2X42_P0**	**C12T28SOI_LL_-NAND2X27_P0**	**C12T28SOI_LL_-NAND2X42_P0**
A to Z ↓	0.0085	0.0318	0.9364	0.4194
A to Z ↑	0.0108	0.0321	0.7471	0.5869
B to Z ↓	0.0084	0.0330	0.9423	0.4195
B to Z ↑	0.0085	0.0309	0.7520	0.5882
	C12T28SOI_LL_-NAND2X47_P0	**C12T28SOI_LL_-NAND2X50_P0**	**C12T28SOI_LL_-NAND2X47_P0**	**C12T28SOI_LL_-NAND2X50_P0**
A to Z ↓	0.0326	0.0328	0.3728	0.3496
A to Z ↑	0.0325	0.0327	0.5107	0.4899
B to Z ↓	0.0337	0.0340	0.3727	0.3496
B to Z ↑	0.0313	0.0316	0.5107	0.4901
	C12T28SOI_LL_-NAND2X58_P0	**C12T28SOI_LL_-NAND2X67_P0**	**C12T28SOI_LL_-NAND2X58_P0**	**C12T28SOI_LL_-NAND2X67_P0**
A to Z ↓	0.0343	0.0357	0.3028	0.2661
A to Z ↑	0.0339	0.0349	0.4213	0.3704
B to Z ↓	0.0355	0.0369	0.3029	0.2661
B to Z ↑	0.0327	0.0338	0.4222	0.3702
	C12T28SOI_-LLBR0D8_-NAND2X7_P0	**C12T28SOI_-LLBR0D8_-NAND2X14_P0**	**C12T28SOI_-LLBR0D8_-NAND2X7_P0**	**C12T28SOI_-LLBR0D8_-NAND2X14_P0**
A to Z ↓	0.0057	0.0064	2.6769	1.3976
A to Z ↑	0.0142	0.0144	3.9997	1.9536
B to Z ↓	0.0059	0.0053	2.7042	1.4139
B to Z ↑	0.0122	0.0109	4.1231	1.9859
	C12T28SOI_LLS_-NAND2X40_P0	**C12T28SOI_LLS_-NAND2X54_P0**	**C12T28SOI_LLS_-NAND2X40_P0**	**C12T28SOI_LLS_-NAND2X54_P0**
A to Z ↓	0.0084	0.0085	0.6335	0.4790
A to Z ↑	0.0106	0.0107	0.5008	0.3773
B to Z ↓	0.0084	0.0086	0.6377	0.4824
B to Z ↑	0.0084	0.0085	0.5041	0.3802

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P0	2.732e-05	1.000e-20
C12T28SOI_LL_NAND2X5_P0	5.090e-05	1.000e-20
C12T28SOI_LL_NAND2X7_P0	6.501e-05	1.000e-20
C12T28SOI_LL_NAND2X10_P0	8.906e-05	1.000e-20
C12T28SOI_LL_NAND2X13_P0	1.280e-04	1.000e-20
C12T28SOI_LL_NAND2X17_P0	1.517e-04	1.000e-20
C12T28SOI_LL_NAND2X20_P0	1.863e-04	1.000e-20
C12T28SOI_LL_NAND2X24_P0	2.145e-04	1.000e-20
C12T28SOI_LL_NAND2X27_P0	2.448e-04	1.000e-20

C12T28SOI_LL_NAND2X42_P0	4.517e-04	1.000e-20
C12T28SOI_LL_NAND2X47_P0	4.947e-04	1.000e-20
C12T28SOI_LL_NAND2X50_P0	4.977e-04	1.000e-20
C12T28SOI_LL_NAND2X58_P0	5.438e-04	1.000e-20
C12T28SOI_LL_NAND2X67_P0	5.898e-04	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_P0	5.932e-05	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_P0	1.145e-04	1.000e-20
C12T28SOI_LLS_NAND2X40_P0	3.617e-04	1.000e-20
C12T28SOI_LLS_NAND2X54_P0	4.787e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_NAND2X3_P0	C12T28SOI_LL_NAND2X5_P0	C12T28SOI_LL_NAND2X7_P0	C12T28SOI_LL_NAND2X10_P0
A (output stable)	1.040e-05	1.623e-05	1.910e-05	6.608e-05
B (output stable)	1.638e-05	2.546e-05	3.129e-05	1.690e-04
A to Z	6.350e-04	9.041e-04	1.097e-03	1.793e-03
B to Z	5.723e-04	8.072e-04	9.731e-04	1.458e-03
	C12T28SOI_LL_NAND2X13_P0	C12T28SOI_LL_NAND2X17_P0	C12T28SOI_LL_NAND2X20_P0	C12T28SOI_LL_NAND2X24_P0
A (output stable)	7.865e-05	9.024e-05	1.001e-04	1.422e-04
B (output stable)	1.956e-04	1.950e-04	2.107e-04	3.174e-04
A to Z	2.272e-03	2.822e-03	3.281e-03	3.933e-03
B to Z	1.873e-03	2.401e-03	2.806e-03	3.260e-03
	C12T28SOI_LL_NAND2X27_P0	C12T28SOI_LL_NAND2X42_P0	C12T28SOI_LL_NAND2X47_P0	C12T28SOI_LL_NAND2X50_P0
A (output stable)	1.530e-04	2.186e-05	2.186e-05	2.136e-05
B (output stable)	3.352e-04	3.386e-05	3.468e-05	3.386e-05
A to Z	4.338e-03	9.330e-03	1.012e-02	1.043e-02
B to Z	3.595e-03	9.219e-03	1.001e-02	1.032e-02
	C12T28SOI_LL_NAND2X58_P0	C12T28SOI_LL_NAND2X67_P0	C12T28SOI_LLBR0D8_NAND2X7_P0	C12T28SOI_LLBR0D8_NAND2X14_P0
A (output stable)	2.136e-05	2.136e-05	2.519e-05	9.708e-05
B (output stable)	3.468e-05	3.468e-05	4.134e-05	2.429e-04
A to Z	1.201e-02	1.337e-02	1.093e-03	2.273e-03
B to Z	1.189e-02	1.326e-02	9.166e-04	1.725e-03
	C12T28SOI_LLS_NAND2X40_P0	C12T28SOI_LLS_NAND2X54_P0		
A (output stable)	2.206e-04	2.811e-04		
B (output stable)	4.629e-04	6.023e-04		
A to Z	6.390e-03	8.516e-03		
B to Z	5.345e-03	7.142e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_NAND2X3_P0	C12T28SOI_LL_NAND2X5_P0	C12T28SOI_LL_NAND2X7_P0	C12T28SOI_LL_NAND2X10_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

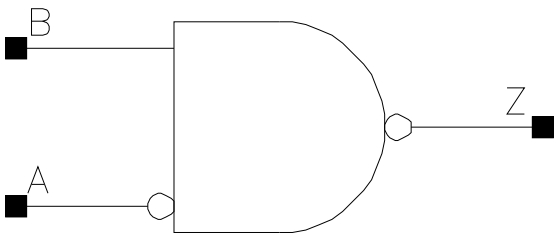
	C12T28SOI_LL_-NAND2X13_P0	C12T28SOI_LL_-NAND2X17_P0	C12T28SOI_LL_-NAND2X20_P0	C12T28SOI_LL_-NAND2X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P0	C12T28SOI_LL_-NAND2X42_P0	C12T28SOI_LL_-NAND2X47_P0	C12T28SOI_LL_-NAND2X50_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P0	C12T28SOI_LL_-NAND2X67_P0	C12T28SOI_-LLBR0D8_-NAND2X7_P0	C12T28SOI_-LLBR0D8_-NAND2X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P0	C12T28SOI_LLS_-NAND2X54_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X7_P0	1.200	0.544	0.6528
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X40_P0	1.200	2.312	2.7744
X54_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P0	X7_P0	X13_P0	X27_P0
A	0.0007	0.0007	0.0010	0.0018
B	0.0005	0.0007	0.0013	0.0027
	X40_P0	X54_P0		
A	0.0027	0.0035		
B	0.0040	0.0054		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0239	0.0252	6.6566	3.5435
A to Z ↑	0.0186	0.0193	5.7099	2.9651
B to Z ↓	0.0103	0.0089	6.7938	3.6087
B to Z ↑	0.0120	0.0096	5.9148	3.0568
	X13_P0	**X27_P0**	**X13_P0**	**X27_P0**

A to Z ↓	0.0228	0.0221	1.8780	0.9332
A to Z ↑	0.0182	0.0177	1.5209	0.7370
B to Z ↓	0.0083	0.0082	1.9170	0.9526
B to Z ↑	0.0088	0.0084	1.5246	0.7528
	X40_P0	**X54_P0**	**X40_P0**	**X54_P0**
A to Z ↓	0.0223	0.0223	0.6232	0.4723
A to Z ↑	0.0180	0.0180	0.4911	0.3705
B to Z ↓	0.0083	0.0084	0.6362	0.4823
B to Z ↑	0.0084	0.0084	0.5057	0.3817

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	5.215e-05	1.000e-20
X7_P0	8.908e-05	1.000e-20
X13_P0	1.945e-04	1.000e-20
X27_P0	3.729e-04	1.000e-20
X40_P0	5.473e-04	1.000e-20
X54_P0	7.217e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	9.068e-04	1.089e-03	1.836e-03	3.584e-03
B (output stable)	1.690e-05	3.140e-05	1.794e-04	3.019e-04
A to Z	1.495e-03	2.047e-03	3.781e-03	7.390e-03
B to Z	5.756e-04	9.645e-04	1.845e-03	3.618e-03
	X40_P0	X54_P0		
A (output stable)	5.424e-03	7.133e-03		
B (output stable)	4.388e-04	5.616e-04		
A to Z	1.108e-02	1.466e-02		
B to Z	5.348e-03	7.103e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

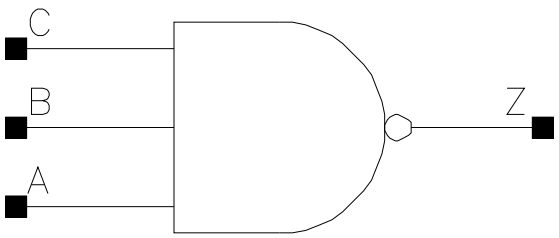
Pin Cycle (vdds)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P0	X54_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P0	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P0	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P0	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P0	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P0	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P0	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P0	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P0	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P0	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P0	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P0	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P0	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P0	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P0	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P0	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A	0.0006	0.0007	0.0012	0.0015
B	0.0006	0.0008	0.0011	0.0014
C	0.0006	0.0007	0.0011	0.0014
	C12T28SOI_LL_-NAND3X15_P0	C12T28SOI_LL_-NAND3X18_P0	C12T28SOI_LL_-NAND3X21_P0	C12T28SOI_LL_-NAND3X24_P0
A	0.0019	0.0021	0.0026	0.0029
B	0.0018	0.0021	0.0025	0.0028
C	0.0017	0.0020	0.0024	0.0027
	C12T28SOI_LL_-NAND3X35_P0	C12T28SOI_LL_-NAND3X47_P0	C12T28SOI_-LLBR0P6_-NAND3X6_P0	C12T28SOI_-LLBR0P6_-NAND3X12_P0
A	0.0044	0.0059	0.0007	0.0015
B	0.0041	0.0056	0.0008	0.0014
C	0.0040	0.0054	0.0007	0.0013
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	C12T28SOI_-LLBR0P6_-NAND3X24_P0	C12T28SOI_-LLBR0P6_-NAND3X35_P0	C12T28SOI_-LLBR0P6_-NAND3X47_P0
A	0.0022	0.0029	0.0043	0.0058
B	0.0020	0.0027	0.0040	0.0054
C	0.0019	0.0026	0.0039	0.0052
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0			
A	0.0023			
B	0.0022			
C	0.0020			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0
A to Z ↓	0.0147	0.0133	6.9284	4.9241
A to Z ↑	0.0164	0.0145	4.2618	2.9215
B to Z ↓	0.0160	0.0142	6.9516	4.9392
B to Z ↑	0.0158	0.0137	4.2702	2.9276
C to Z ↓	0.0148	0.0134	6.9602	4.9465
C to Z ↑	0.0137	0.0118	4.2697	2.9423

	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A to Z ↓	0.0144	0.0136	3.3592	2.5945
A to Z ↑	0.0153	0.0141	1.9934	1.4935
B to Z ↓	0.0142	0.0134	3.3695	2.6024
B to Z ↑	0.0139	0.0128	1.9970	1.4961
C to Z ↓	0.0132	0.0127	3.3758	2.6069
C to Z ↑	0.0118	0.0108	1.9911	1.4861
	C12T28SOI_LL_-NAND3X15_P0	**C12T28SOI_LL_-NAND3X18_P0**	**C12T28SOI_LL_-NAND3X15_P0**	**C12T28SOI_LL_-NAND3X18_P0**
A to Z ↓	0.0128	0.0125	2.0987	1.7886
A to Z ↑	0.0138	0.0132	1.1956	0.9938
B to Z ↓	0.0133	0.0131	2.1062	1.7946
B to Z ↑	0.0124	0.0119	1.1988	0.9964
C to Z ↓	0.0127	0.0125	2.1099	1.7978
C to Z ↑	0.0107	0.0101	1.2053	1.0018
	C12T28SOI_LL_-NAND3X21_P0	**C12T28SOI_LL_-NAND3X24_P0**	**C12T28SOI_LL_-NAND3X21_P0**	**C12T28SOI_LL_-NAND3X24_P0**
A to Z ↓	0.0133	0.0131	1.5131	1.3505
A to Z ↑	0.0138	0.0135	0.8565	0.7518
B to Z ↓	0.0133	0.0132	1.5178	1.3551
B to Z ↑	0.0126	0.0122	0.8581	0.7531
C to Z ↓	0.0128	0.0126	1.5206	1.3575
C to Z ↑	0.0107	0.0103	0.8590	0.7534
	C12T28SOI_LL_-NAND3X35_P0	**C12T28SOI_LL_-NAND3X47_P0**	**C12T28SOI_LL_-NAND3X35_P0**	**C12T28SOI_LL_-NAND3X47_P0**
A to Z ↓	0.0124	0.0126	0.9200	0.6994
A to Z ↑	0.0130	0.0131	0.5045	0.3814
B to Z ↓	0.0128	0.0129	0.9233	0.7016
B to Z ↑	0.0117	0.0117	0.5045	0.3801
C to Z ↓	0.0123	0.0124	0.9250	0.7031
C to Z ↑	0.0097	0.0096	0.5066	0.3815
	C12T28SOI_-LLBR0P6_-NAND3X6_P0	**C12T28SOI_-LLBR0P6_-NAND3X12_P0**	**C12T28SOI_-LLBR0P6_-NAND3X6_P0**	**C12T28SOI_-LLBR0P6_-NAND3X12_P0**
A to Z ↓	0.0095	0.0099	3.3140	1.7481
A to Z ↑	0.0213	0.0209	4.6083	2.3539
B to Z ↓	0.0097	0.0089	3.3370	1.7623
B to Z ↑	0.0195	0.0182	4.6141	2.3581
C to Z ↓	0.0079	0.0069	3.3589	1.7743
C to Z ↑	0.0157	0.0142	4.6304	2.3626
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	**C12T28SOI_-LLBR0P6_-NAND3X24_P0**	**C12T28SOI_-LLBR0P6_-NAND3X18_P0**	**C12T28SOI_-LLBR0P6_-NAND3X24_P0**
A to Z ↓	0.0089	0.0095	1.2081	0.9133
A to Z ↑	0.0197	0.0201	1.5678	1.1843
B to Z ↓	0.0086	0.0087	1.2183	0.9208
B to Z ↑	0.0170	0.0174	1.5720	1.1862
C to Z ↓	0.0071	0.0070	1.2255	0.9268
C to Z ↑	0.0136	0.0136	1.5801	1.1854
	C12T28SOI_-LLBR0P6_-NAND3X35_P0	**C12T28SOI_-LLBR0P6_-NAND3X47_P0**	**C12T28SOI_-LLBR0P6_-NAND3X35_P0**	**C12T28SOI_-LLBR0P6_-NAND3X47_P0**

A to Z ↓	0.0090	0.0090	0.6240	0.4761
A to Z ↑	0.0200	0.0199	0.8117	0.6135
B to Z ↓	0.0086	0.0085	0.6295	0.4802
B to Z ↑	0.0172	0.0171	0.8121	0.6135
C to Z ↓	0.0069	0.0070	0.6338	0.4834
C to Z ↑	0.0133	0.0133	0.8169	0.6148
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P0**	
A to Z ↓	0.0100		1.1668	
A to Z ↑	0.0199		1.4707	
B to Z ↓	0.0089		1.1758	
B to Z ↑	0.0173		1.4735	
C to Z ↓	0.0070		1.1834	
C to Z ↑	0.0133		1.4635	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P0	3.387e-05	1.000e-20
C12T28SOI_LL_NAND3X6_P0	5.502e-05	1.000e-20
C12T28SOI_LL_NAND3X9_P0	7.131e-05	1.000e-20
C12T28SOI_LL_NAND3X12_P0	1.018e-04	1.000e-20
C12T28SOI_LL_NAND3X15_P0	1.176e-04	1.000e-20
C12T28SOI_LL_NAND3X18_P0	1.440e-04	1.000e-20
C12T28SOI_LL_NAND3X21_P0	1.696e-04	1.000e-20
C12T28SOI_LL_NAND3X24_P0	1.932e-04	1.000e-20
C12T28SOI_LL_NAND3X35_P0	2.845e-04	1.000e-20
C12T28SOI_LL_NAND3X47_P0	3.758e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_P0	5.000e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P0	9.011e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P0	1.232e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P0	1.669e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P0	2.435e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P0	3.200e-04	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P0	1.584e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A (output stable)	2.220e-05	2.956e-05	7.139e-05	8.315e-05
B (output stable)	3.190e-05	3.981e-05	8.910e-05	1.042e-04
C (output stable)	1.153e-04	1.399e-04	2.130e-04	2.479e-04
A to Z	1.268e-03	1.611e-03	2.521e-03	3.059e-03
B to Z	1.174e-03	1.469e-03	2.155e-03	2.641e-03
C to Z	1.000e-03	1.269e-03	1.834e-03	2.264e-03

	C12T28SOI_LL_-NAND3X15_P0	C12T28SOI_LL_-NAND3X18_P0	C12T28SOI_LL_-NAND3X21_P0	C12T28SOI_LL_-NAND3X24_P0
A (output stable)	8.789e-05	9.970e-05	1.424e-04	1.529e-04
B (output stable)	1.110e-04	1.263e-04	1.693e-04	1.855e-04
C (output stable)	2.569e-04	2.903e-04	3.924e-04	4.330e-04
A to Z	3.655e-03	4.194e-03	5.208e-03	5.740e-03
B to Z	3.150e-03	3.615e-03	4.486e-03	4.962e-03
C to Z	2.747e-03	3.148e-03	3.863e-03	4.272e-03
	C12T28SOI_LL_-NAND3X35_P0	C12T28SOI_LL_-NAND3X47_P0	C12T28SOI_-LLBR0P6_-NAND3X6_P0	C12T28SOI_-LLBR0P6_-NAND3X12_P0
A (output stable)	2.081e-04	2.715e-04	4.227e-05	1.176e-04
B (output stable)	2.521e-04	3.305e-04	5.598e-05	1.510e-04
C (output stable)	6.234e-04	7.928e-04	1.850e-04	3.483e-04
A to Z	8.212e-03	1.087e-02	1.668e-03	3.227e-03
B to Z	7.035e-03	9.321e-03	1.442e-03	2.573e-03
C to Z	5.990e-03	7.930e-03	1.120e-03	1.933e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	C12T28SOI_-LLBR0P6_-NAND3X24_P0	C12T28SOI_-LLBR0P6_-NAND3X35_P0	C12T28SOI_-LLBR0P6_-NAND3X47_P0
A (output stable)	1.421e-04	2.150e-04	2.902e-04	3.821e-04
B (output stable)	1.754e-04	2.692e-04	3.573e-04	4.746e-04
C (output stable)	3.885e-04	6.186e-04	8.993e-04	1.150e-03
A to Z	4.354e-03	6.010e-03	8.704e-03	1.133e-02
B to Z	3.468e-03	4.801e-03	6.926e-03	9.042e-03
C to Z	2.724e-03	3.645e-03	5.198e-03	6.768e-03
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0			
A (output stable)	1.731e-04			
B (output stable)	2.250e-04			
C (output stable)	4.994e-04			
A to Z	4.856e-03			
B to Z	3.896e-03			
C to Z	2.956e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P0	C12T28SOI_LL_-NAND3X18_P0	C12T28SOI_LL_-NAND3X21_P0	C12T28SOI_LL_-NAND3X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

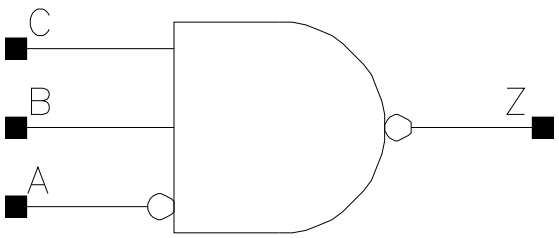
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P0	C12T28SOI_LL_-NAND3X47_P0	C12T28SOI_-LLBR0P6_-NAND3X6_P0	C12T28SOI_-LLBR0P6_-NAND3X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	C12T28SOI_-LLBR0P6_-NAND3X24_P0	C12T28SOI_-LLBR0P6_-NAND3X35_P0	C12T28SOI_-LLBR0P6_-NAND3X47_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.816	0.9792
X12_P0	1.200	1.224	1.4688
X18_P0	1.200	1.496	1.7952
X24_P0	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0007	0.0010	0.0010	0.0018
B	0.0007	0.0014	0.0021	0.0028
C	0.0007	0.0014	0.0020	0.0026

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X12_P0**	**X6_P0**	**X12_P0**
A to Z ↓	0.0285	0.0269	4.9353	2.6142
A to Z ↑	0.0205	0.0199	2.8734	1.4443
B to Z ↓	0.0125	0.0126	4.9738	2.6353
B to Z ↑	0.0122	0.0119	2.9382	1.4823
C to Z ↓	0.0128	0.0117	4.9854	2.6401
C to Z ↑	0.0109	0.0097	2.9514	1.4917
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0309	0.0262	1.7877	1.3525

A to Z ↑	0.0231	0.0189	0.9715	0.7292
B to Z ↓	0.0130	0.0126	1.8004	1.3635
B to Z ↑	0.0119	0.0116	0.9976	0.7506
C to Z ↓	0.0126	0.0119	1.8033	1.3659
C to Z ↑	0.0102	0.0095	1.0030	0.7551

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P0	7.767e-05	1.000e-20
X12_P0	1.669e-04	1.000e-20
X18_P0	2.083e-04	1.000e-20
X24_P0	3.235e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	1.057e-03	1.932e-03	2.496e-03	3.658e-03
B (output stable)	2.710e-05	8.719e-05	1.328e-04	1.976e-04
C (output stable)	5.972e-05	2.497e-04	2.915e-04	4.492e-04
A to Z	2.382e-03	4.675e-03	6.675e-03	9.014e-03
B to Z	1.262e-03	2.439e-03	3.618e-03	4.688e-03
C to Z	1.144e-03	2.034e-03	3.151e-03	3.936e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

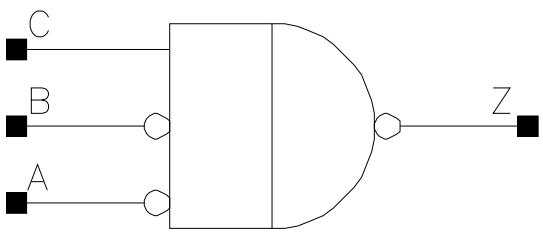
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	0.816	0.9792
X13_P0	1.200	1.088	1.3056
X20_P0	1.200	1.632	1.9584
X27_P0	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P0	X13_P0	X20_P0	X27_P0
A	0.0009	0.0009	0.0017	0.0016
B	0.0010	0.0010	0.0018	0.0017
C	0.0007	0.0014	0.0020	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	**X13_P0**	**X7_P0**	**X13_P0**
A to Z ↓	0.0260	0.0315	3.3984	1.7987
A to Z ↑	0.0177	0.0205	2.8579	1.4387
B to Z ↓	0.0269	0.0326	3.3967	1.7978
B to Z ↑	0.0166	0.0195	2.8536	1.4369
C to Z ↓	0.0087	0.0082	3.4553	1.8243
C to Z ↑	0.0096	0.0086	2.9391	1.4889
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0284	0.0313	1.2233	0.9288
A to Z ↑	0.0189	0.0230	0.9695	0.7291
B to Z ↓	0.0276	0.0309	1.2227	0.9288

B to Z ↑	0.0171	0.0217	0.9680	0.7277
C to Z ↓	0.0091	0.0087	1.2423	0.9425
C to Z ↑	0.0092	0.0089	1.0023	0.7526

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X7_P0	1.186e-04	1.000e-20
X13_P0	1.592e-04	1.000e-20
X20_P0	2.597e-04	1.000e-20
X27_P0	2.903e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	6.126e-04	7.853e-04	1.333e-03	1.531e-03
B (output stable)	5.713e-04	7.429e-04	1.243e-03	1.456e-03
C (output stable)	3.410e-05	2.050e-04	2.018e-04	2.480e-04
A to Z	2.762e-03	4.501e-03	6.968e-03	8.736e-03
B to Z	2.595e-03	4.339e-03	6.351e-03	8.189e-03
C to Z	1.012e-03	1.856e-03	2.902e-03	3.839e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

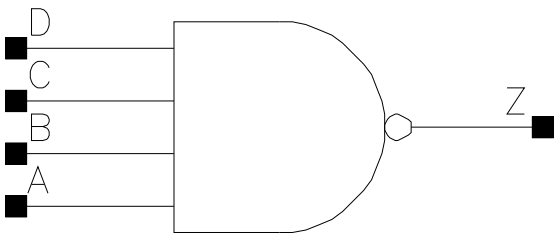
Pin Cycle (vdds)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0006	0.0006	0.0007	0.0009
B	0.0006	0.0006	0.0008	0.0010
C	0.0006	0.0007	0.0008	0.0009
D	0.0006	0.0006	0.0008	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0422	0.0412	2.0349	1.0185
A to Z ↑	0.0342	0.0367	2.9234	1.4488
B to Z ↓	0.0436	0.0433	2.0351	1.0196
B to Z ↑	0.0330	0.0363	2.9226	1.4482
C to Z ↓	0.0432	0.0417	2.0346	1.0187
C to Z ↑	0.0354	0.0384	2.9225	1.4485

D to Z ↓	0.0450	0.0431	2.0337	1.0189
D to Z ↑	0.0347	0.0371	2.9226	1.4477
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0429	0.0397	0.7006	0.5248
A to Z ↑	0.0348	0.0341	0.9766	0.7333
B to Z ↓	0.0445	0.0409	0.7008	0.5248
B to Z ↑	0.0339	0.0330	0.9767	0.7328
C to Z ↓	0.0405	0.0371	0.7006	0.5242
C to Z ↑	0.0354	0.0342	0.9744	0.7316
D to Z ↓	0.0420	0.0384	0.7000	0.5248
D to Z ↑	0.0341	0.0331	0.9750	0.7304

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.191e-04	1.000e-20
X17_P0	1.931e-04	1.000e-20
X25_P0	2.786e-04	1.000e-20
X33_P0	3.926e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	4.300e-04	5.217e-04	7.494e-04	9.226e-04
B (output stable)	4.074e-04	5.019e-04	7.158e-04	8.777e-04
C (output stable)	4.409e-04	5.221e-04	7.742e-04	9.116e-04
D (output stable)	4.164e-04	4.955e-04	7.351e-04	8.650e-04
A to Z	3.275e-03	5.003e-03	7.583e-03	9.349e-03
B to Z	3.211e-03	4.946e-03	7.483e-03	9.228e-03
C to Z	3.381e-03	4.996e-03	7.222e-03	8.809e-03
D to Z	3.324e-03	4.926e-03	7.120e-03	8.684e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

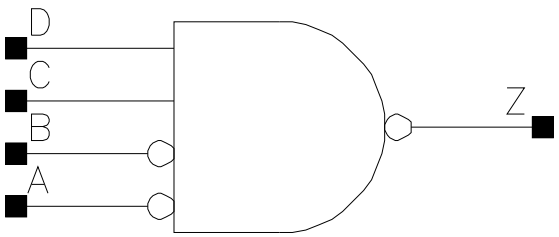
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X12_P0	1.200	1.496	1.7952
X18_P0	1.200	2.040	2.4480
X24_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0009	0.0009	0.0017	0.0016
B	0.0009	0.0014	0.0018	0.0017
C	0.0007	0.0014	0.0020	0.0028
D	0.0007	0.0014	0.0020	0.0028

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X12_P0	X6_P0	X12_P0
A to Z ↓	0.0278	0.0369	5.0598	2.6188
A to Z ↑	0.0186	0.0229	2.8524	1.4400
B to Z ↓	0.0282	0.0373	5.0624	2.6180
B to Z ↑	0.0170	0.0216	2.8491	1.4387
C to Z ↓	0.0126	0.0126	5.0992	2.6351
C to Z ↑	0.0122	0.0119	3.0873	1.4819

D to Z ↓	0.0127	0.0116	5.1101	2.6393
D to Z ↑	0.0109	0.0097	3.1015	1.4910
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0316	0.0356	1.7843	1.3539
A to Z ↑	0.0199	0.0260	0.9692	0.7289
B to Z ↓	0.0309	0.0350	1.7844	1.3538
B to Z ↑	0.0182	0.0244	0.9670	0.7276
C to Z ↓	0.0125	0.0131	1.7964	1.3617
C to Z ↑	0.0115	0.0120	1.0013	0.7482
D to Z ↓	0.0121	0.0125	1.7997	1.3644
D to Z ↑	0.0098	0.0100	1.0188	0.7535

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P0	1.015e-04	1.000e-20
X12_P0	1.369e-04	1.000e-20
X18_P0	2.262e-04	1.000e-20
X24_P0	2.436e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	6.997e-04	1.097e-03	1.685e-03	1.966e-03
B (output stable)	6.467e-04	1.028e-03	1.527e-03	1.823e-03
C (output stable)	2.919e-05	9.015e-05	1.277e-04	1.789e-04
D (output stable)	6.676e-05	2.584e-04	3.023e-04	4.640e-04
A to Z	2.853e-03	5.267e-03	7.708e-03	1.020e-02
B to Z	2.711e-03	4.997e-03	7.125e-03	9.620e-03
C to Z	1.226e-03	2.432e-03	3.473e-03	4.903e-03
D to Z	1.108e-03	2.026e-03	3.035e-03	4.171e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

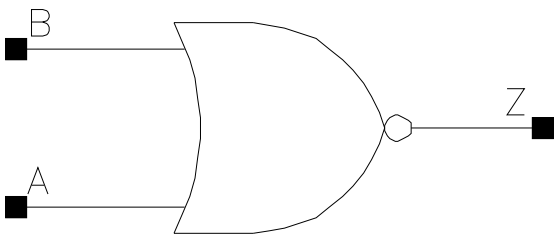
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.408	0.4896
X5_P0	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X10_P0	1.200	0.680	0.8160
X14_P0	1.200	0.680	0.8160
X17_P0	1.200	0.952	1.1424
X21_P0	1.200	0.952	1.1424
X24_P0	1.200	1.224	1.4688
X27_P0	1.200	1.224	1.4688
X34_P0	1.200	1.496	1.7952
X40_P0	1.200	1.360	1.6320
X41_P0	1.200	1.768	2.1216
X49_P0	1.200	1.496	1.7952
X53_P0	1.200	1.904	2.2848
X55_P0	1.200	2.312	2.7744
X57_P0	1.200	1.904	2.2848
X65_P0	1.200	2.040	2.4480
X84_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P0	X5_P0	X7_P0	X10_P0
A	0.0005	0.0006	0.0007	0.0012
B	0.0005	0.0006	0.0008	0.0011
	X14_P0	X17_P0	X21_P0	X24_P0

A	0.0015	0.0019	0.0022	0.0026
B	0.0014	0.0017	0.0020	0.0024
	X27_P0	X34_P0	X40_P0	X41_P0
A	0.0029	0.0036	0.0008	0.0044
B	0.0027	0.0034	0.0010	0.0041
	X49_P0	X53_P0	X55_P0	X57_P0
A	0.0009	0.0009	0.0059	0.0009
B	0.0010	0.0008	0.0055	0.0008
	X65_P0	X84_P0		
A	0.0009	0.0010		
B	0.0008	0.0009		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X5_P0**	**X3_P0**	**X5_P0**
A to Z ↓	0.0076	0.0071	4.0346	2.8867
A to Z ↑	0.0149	0.0136	11.2427	8.1383
B to Z ↓	0.0067	0.0060	4.1088	2.9045
B to Z ↑	0.0156	0.0141	11.2794	8.1529
	X7_P0	**X10_P0**	**X7_P0**	**X10_P0**
A to Z ↓	0.0070	0.0072	2.1028	1.3743
A to Z ↑	0.0125	0.0139	5.7040	3.8322
B to Z ↓	0.0058	0.0050	2.1282	1.3865
B to Z ↑	0.0129	0.0121	5.7163	3.8381
	X14_P0	**X17_P0**	**X14_P0**	**X17_P0**
A to Z ↓	0.0072	0.0072	1.0405	0.8376
A to Z ↑	0.0128	0.0130	2.8235	2.2885
B to Z ↓	0.0050	0.0055	1.0501	0.8440
B to Z ↑	0.0114	0.0123	2.8294	2.2929
	X21_P0	**X24_P0**	**X21_P0**	**X24_P0**
A to Z ↓	0.0072	0.0070	0.7090	0.6054
A to Z ↑	0.0123	0.0126	1.8967	1.6584
B to Z ↓	0.0056	0.0051	0.7143	0.6107
B to Z ↑	0.0119	0.0117	1.9005	1.6621
	X27_P0	**X34_P0**	**X27_P0**	**X34_P0**
A to Z ↓	0.0070	0.0074	0.5369	0.4329
A to Z ↑	0.0120	0.0124	1.4551	1.1592
B to Z ↓	0.0050	0.0055	0.5420	0.4364
B to Z ↑	0.0112	0.0118	1.4580	1.1614
	X40_P0	**X41_P0**	**X40_P0**	**X41_P0**
A to Z ↓	0.0280	0.0071	0.4287	0.3610
A to Z ↑	0.0379	0.0120	0.5999	0.9610
B to Z ↓	0.0269	0.0051	0.4283	0.3643
B to Z ↑	0.0391	0.0112	0.6000	0.9627
	X49_P0	**X53_P0**	**X49_P0**	**X53_P0**
A to Z ↓	0.0292	0.0306	0.3570	0.3280
A to Z ↑	0.0391	0.0444	0.4984	0.4618
B to Z ↓	0.0281	0.0294	0.3570	0.3280
B to Z ↑	0.0402	0.0451	0.4987	0.4616
	X55_P0	**X57_P0**	**X55_P0**	**X57_P0**
A to Z ↓	0.0072	0.0308	0.2727	0.3072
A to Z ↑	0.0120	0.0446	0.7237	0.4289

B to Z ↓	0.0053	0.0296	0.2756	0.3074
B to Z ↑	0.0113	0.0453	0.7255	0.4282
	X65_P0	**X84_P0**	**X65_P0**	**X84_P0**
A to Z ↓	0.0318	0.0331	0.2693	0.2132
A to Z ↑	0.0456	0.0462	0.3751	0.2977
B to Z ↓	0.0306	0.0320	0.2692	0.2131
B to Z ↑	0.0464	0.0471	0.3753	0.2978

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	2.773e-05	1.000e-20
X5_P0	4.322e-05	1.000e-20
X7_P0	6.693e-05	1.000e-20
X10_P0	9.158e-05	1.000e-20
X14_P0	1.323e-04	1.000e-20
X17_P0	1.565e-04	1.000e-20
X21_P0	1.929e-04	1.000e-20
X24_P0	2.216e-04	1.000e-20
X27_P0	2.537e-04	1.000e-20
X34_P0	3.145e-04	1.000e-20
X40_P0	5.161e-04	1.000e-20
X41_P0	3.753e-04	1.000e-20
X49_P0	5.865e-04	1.000e-20
X53_P0	6.718e-04	1.000e-20
X55_P0	4.969e-04	1.000e-20
X57_P0	7.182e-04	1.000e-20
X65_P0	7.888e-04	1.000e-20
X84_P0	9.156e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	1.568e-05	2.101e-05	2.926e-05	9.044e-05
B (output stable)	2.711e-05	3.559e-05	4.943e-05	2.226e-04
A to Z	6.263e-04	7.967e-04	1.089e-03	1.770e-03
B to Z	5.454e-04	6.884e-04	9.267e-04	1.318e-03
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	1.059e-04	1.242e-04	1.389e-04	1.716e-04
B (output stable)	2.589e-04	2.646e-04	2.752e-04	3.715e-04
A to Z	2.263e-03	2.815e-03	3.277e-03	3.844e-03
B to Z	1.723e-03	2.260e-03	2.656e-03	3.018e-03
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	1.884e-04	2.210e-04	2.973e-05	2.892e-04
B (output stable)	3.999e-04	4.162e-04	4.950e-05	6.177e-04
A to Z	4.236e-03	5.391e-03	9.099e-03	6.389e-03
B to Z	3.314e-03	4.356e-03	8.950e-03	4.979e-03
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	3.073e-05	3.073e-05	3.668e-04	3.073e-05
B (output stable)	4.968e-05	5.318e-05	7.320e-04	5.318e-05
A to Z	1.033e-02	1.282e-02	8.394e-03	1.328e-02
B to Z	1.018e-02	1.265e-02	6.631e-03	1.312e-02
	X65_P0	X84_P0		

A (output stable)	3.073e-05	3.423e-05		
B (output stable)	5.400e-05	5.418e-05		
A to Z	1.455e-02	1.752e-02		
B to Z	1.438e-02	1.732e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

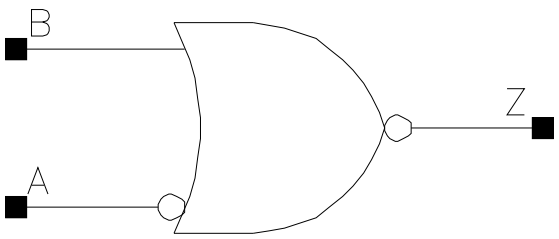
Pin Cycle (vdds)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P0	X84_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X7_P0	1.200	0.680	0.8160
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X41_P0	1.200	2.312	2.7744
X55_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X7_P0	X13_P0
A	0.0007	0.0007	0.0007	0.0010
B	0.0005	0.0008	0.0007	0.0013
	X27_P0	X41_P0	X55_P0	
A	0.0018	0.0027	0.0035	
B	0.0027	0.0041	0.0054	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0222	0.0244	3.8852	2.4952
A to Z ↑	0.0211	0.0210	11.1420	5.6633
B to Z ↓	0.0069	0.0072	4.0877	2.6379
B to Z ↑	0.0158	0.0126	11.2584	5.7345

	X7_P0	X13_P0	X7_P0	X13_P0
A to Z ↓	0.0247	0.0215	1.9678	1.0646
A to Z ↑	0.0231	0.0216	5.5944	2.9644
B to Z ↓	0.0062	0.0053	2.0311	1.0974
B to Z ↑	0.0141	0.0125	5.6377	2.9909
	X27_P0	**X41_P0**	**X27_P0**	**X41_P0**
A to Z ↓	0.0208	0.0213	0.5130	0.3471
A to Z ↑	0.0207	0.0210	1.4231	0.9548
B to Z ↓	0.0052	0.0053	0.5431	0.3660
B to Z ↑	0.0118	0.0116	1.4369	0.9638
	X55_P0		**X55_P0**	
A to Z ↓	0.0209		0.2624	
A to Z ↑	0.0206		0.7201	
B to Z ↓	0.0053		0.2772	
B to Z ↑	0.0116		0.7270	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	5.261e-05	1.000e-20
X6_P0	8.875e-05	1.000e-20
X7_P0	1.001e-04	1.000e-20
X13_P0	1.956e-04	1.000e-20
X27_P0	3.815e-04	1.000e-20
X41_P0	5.606e-04	1.000e-20
X55_P0	7.395e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	8.958e-04	1.067e-03	1.132e-03	1.860e-03
B (output stable)	2.695e-05	4.925e-05	1.280e-04	2.244e-04
A to Z	1.486e-03	2.013e-03	2.340e-03	3.918e-03
B to Z	5.517e-04	8.859e-04	1.068e-03	1.806e-03
	X27_P0	X41_P0	X55_P0	
A (output stable)	3.675e-03	5.562e-03	7.255e-03	
B (output stable)	4.356e-04	6.144e-04	7.566e-04	
A to Z	7.783e-03	1.164e-02	1.523e-02	
B to Z	3.535e-03	5.195e-03	6.841e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

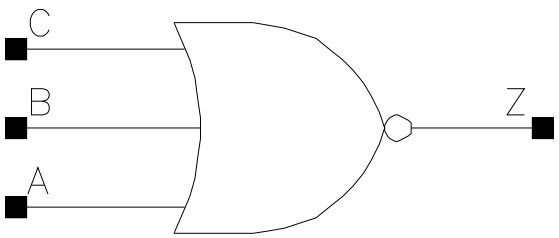
Pin Cycle (vdds)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X41_P0	X55_P0	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X9_P0	1.200	0.952	1.1424
X13_P0	1.200	0.952	1.1424
X16_P0	1.200	1.360	1.6320
X19_P0	1.200	1.496	1.7952
X22_P0	1.200	1.768	2.1216
X25_P0	1.200	1.904	2.2848
X37_P0	1.200	2.584	3.1008
X49_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P0	X6_P0	X9_P0	X13_P0
A	0.0006	0.0007	0.0011	0.0014
B	0.0006	0.0007	0.0013	0.0015
C	0.0006	0.0007	0.0011	0.0013
	X16_P0	X19_P0	X22_P0	X25_P0
A	0.0019	0.0022	0.0026	0.0029
B	0.0019	0.0026	0.0028	0.0035
C	0.0017	0.0020	0.0024	0.0026
	X37_P0	X49_P0		
A	0.0043	0.0059		
B	0.0045	0.0060		

C	0.0039	0.0054		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0089	0.0085	2.9178	2.1310
A to Z ↑	0.0200	0.0179	12.0658	8.4562
B to Z ↓	0.0083	0.0079	2.9236	2.1361
B to Z ↑	0.0196	0.0174	12.0737	8.4632
C to Z ↓	0.0073	0.0067	2.9398	2.1551
C to Z ↑	0.0194	0.0171	12.0810	8.4695
	X9_P0	**X13_P0**	**X9_P0**	**X13_P0**
A to Z ↓	0.0088	0.0086	1.4103	1.0765
A to Z ↑	0.0197	0.0180	5.6586	4.1870
B to Z ↓	0.0081	0.0077	1.3802	1.0378
B to Z ↑	0.0199	0.0177	5.6668	4.1943
C to Z ↓	0.0060	0.0057	1.3896	1.0553
C to Z ↑	0.0160	0.0147	5.6616	4.1911
	X16_P0	**X19_P0**	**X16_P0**	**X19_P0**
A to Z ↓	0.0087	0.0085	0.8417	0.7075
A to Z ↑	0.0188	0.0183	3.3988	2.8005
B to Z ↓	0.0082	0.0081	0.8444	0.6953
B to Z ↑	0.0186	0.0186	3.4042	2.8057
C to Z ↓	0.0063	0.0063	0.8479	0.7200
C to Z ↑	0.0165	0.0156	3.4029	2.8042
	X22_P0	**X25_P0**	**X22_P0**	**X25_P0**
A to Z ↓	0.0086	0.0086	0.6156	0.5387
A to Z ↑	0.0184	0.0182	2.4247	2.1069
B to Z ↓	0.0080	0.0079	0.6066	0.5215
B to Z ↑	0.0183	0.0184	2.4280	2.1104
C to Z ↓	0.0059	0.0059	0.6117	0.5401
C to Z ↑	0.0154	0.0148	2.4273	2.1092
	X37_P0	**X49_P0**	**X37_P0**	**X49_P0**
A to Z ↓	0.0086	0.0087	0.3706	0.2803
A to Z ↑	0.0176	0.0176	1.4114	1.0625
B to Z ↓	0.0080	0.0080	0.3673	0.2781
B to Z ↑	0.0173	0.0173	1.4136	1.0640
C to Z ↓	0.0062	0.0063	0.3710	0.2809
C to Z ↑	0.0149	0.0151	1.4131	1.0640

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	3.422e-05	1.000e-20
X6_P0	5.406e-05	1.000e-20
X9_P0	7.338e-05	1.000e-20
X13_P0	1.085e-04	1.000e-20
X16_P0	1.262e-04	1.000e-20
X19_P0	1.628e-04	1.000e-20
X22_P0	1.795e-04	1.000e-20
X25_P0	2.144e-04	1.000e-20
X37_P0	3.151e-04	1.000e-20

X49_P0	4.185e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	2.308e-05	3.181e-05	6.030e-05	7.798e-05
B (output stable)	2.531e-05	3.546e-05	8.416e-05	1.009e-04
C (output stable)	5.883e-05	8.351e-05	2.612e-04	3.135e-04
A to Z	1.032e-03	1.341e-03	2.193e-03	2.732e-03
B to Z	8.948e-04	1.156e-03	1.934e-03	2.373e-03
C to Z	7.857e-04	9.944e-04	1.436e-03	1.798e-03
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	9.201e-05	1.114e-04	1.335e-04	1.560e-04
B (output stable)	1.232e-04	1.649e-04	1.850e-04	2.263e-04
C (output stable)	3.206e-04	4.266e-04	5.101e-04	6.179e-04
A to Z	3.497e-03	4.174e-03	4.814e-03	5.519e-03
B to Z	3.040e-03	3.678e-03	4.201e-03	4.851e-03
C to Z	2.467e-03	2.842e-03	3.254e-03	3.619e-03
	X37_P0	X49_P0		
A (output stable)	2.245e-04	2.972e-04		
B (output stable)	2.956e-04	3.876e-04		
C (output stable)	8.077e-04	1.050e-03		
A to Z	7.998e-03	1.064e-02		
B to Z	6.909e-03	9.179e-03		
C to Z	5.344e-03	7.142e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

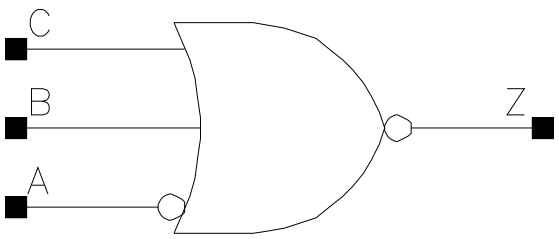
Pin Cycle (vdds)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P0	X49_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.680	0.8160
X13_P0	1.200	1.224	1.4688
X19_P0	1.200	1.496	1.7952
X25_P0	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0007	0.0010	0.0010	0.0018
B	0.0007	0.0015	0.0022	0.0029
C	0.0008	0.0013	0.0020	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X13_P0**	**X6_P0**	**X13_P0**
A to Z ↓	0.0245	0.0231	2.0528	1.1163
A to Z ↑	0.0274	0.0268	8.5426	4.1788
B to Z ↓	0.0080	0.0077	2.1451	1.0426
B to Z ↑	0.0177	0.0178	8.5718	4.1949
C to Z ↓	0.0069	0.0057	2.1558	1.0559
C to Z ↑	0.0174	0.0147	8.5766	4.1915
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0258	0.0228	0.6915	0.5246

A to Z ↑	0.0291	0.0267	2.8078	2.1078
B to Z ↓	0.0081	0.0078	0.7217	0.5390
B to Z ↑	0.0174	0.0172	2.8196	2.1158
C to Z ↓	0.0062	0.0058	0.7209	0.5428
C to Z ↑	0.0157	0.0148	2.8199	2.1161

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P0	7.989e-05	1.000e-20
X13_P0	1.781e-04	1.000e-20
X19_P0	2.244e-04	1.000e-20
X25_P0	3.416e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	1.094e-03	2.010e-03	2.457e-03	3.891e-03
B (output stable)	3.602e-05	1.023e-04	1.414e-04	1.964e-04
C (output stable)	8.249e-05	3.199e-04	3.662e-04	5.488e-04
A to Z	2.404e-03	4.799e-03	6.455e-03	9.210e-03
B to Z	1.161e-03	2.393e-03	3.472e-03	4.609e-03
C to Z	1.004e-03	1.803e-03	2.827e-03	3.574e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

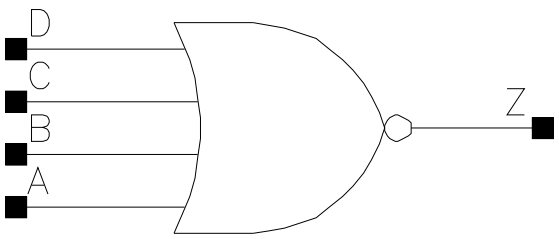
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	1.904	2.2848
X32_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X32_P0
A	0.0006	0.0006	0.0007	0.0008
B	0.0007	0.0006	0.0008	0.0010
C	0.0005	0.0005	0.0007	0.0008
D	0.0006	0.0006	0.0007	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0294	0.0289	2.0171	0.9905
A to Z ↑	0.0434	0.0461	2.9798	1.4687
B to Z ↓	0.0281	0.0280	2.0166	0.9907
B to Z ↑	0.0441	0.0470	2.9809	1.4700
C to Z ↓	0.0290	0.0291	2.0138	0.9884
C to Z ↑	0.0445	0.0477	2.9800	1.4689

D to Z ↓	0.0284	0.0286	2.0140	0.9884
D to Z ↑	0.0456	0.0490	2.9771	1.4668
	X25_P0	**X32_P0**	**X25_P0**	**X32_P0**
A to Z ↓	0.0297	0.0316	0.6867	0.5398
A to Z ↑	0.0445	0.0430	1.0025	0.7597
B to Z ↓	0.0288	0.0305	0.6863	0.5402
B to Z ↑	0.0458	0.0438	1.0017	0.7596
C to Z ↓	0.0288	0.0313	0.6836	0.5386
C to Z ↑	0.0446	0.0436	0.9996	0.7594
D to Z ↓	0.0278	0.0297	0.6837	0.5379
D to Z ↑	0.0456	0.0443	1.0014	0.7602

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.445e-04	1.000e-20
X17_P0	2.439e-04	1.000e-20
X25_P0	3.736e-04	1.000e-20
X32_P0	4.970e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	4.251e-04	5.039e-04	7.020e-04	8.944e-04
B (output stable)	3.938e-04	4.714e-04	6.603e-04	8.329e-04
C (output stable)	4.080e-04	4.720e-04	7.202e-04	9.143e-04
D (output stable)	3.773e-04	4.429e-04	6.754e-04	8.528e-04
A to Z	3.038e-03	4.731e-03	7.122e-03	8.982e-03
B to Z	2.949e-03	4.649e-03	7.001e-03	8.830e-03
C to Z	3.097e-03	4.778e-03	6.810e-03	8.656e-03
D to Z	3.004e-03	4.700e-03	6.697e-03	8.488e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

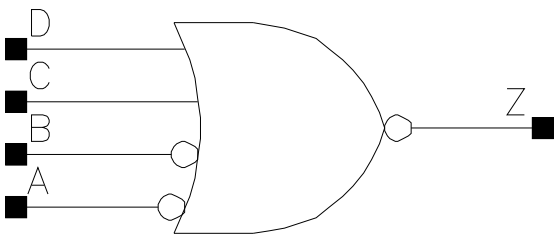
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X13_P0	1.200	1.496	1.7952
X19_P0	1.200	2.040	2.4480
X25_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0009	0.0009	0.0018	0.0017
B	0.0009	0.0014	0.0018	0.0018
C	0.0007	0.0014	0.0021	0.0028
D	0.0007	0.0013	0.0020	0.0026

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X13_P0	X6_P0	X13_P0
A to Z ↓	0.0209	0.0260	1.9994	1.0023
A to Z ↑	0.0276	0.0340	8.2192	4.2401
B to Z ↓	0.0196	0.0250	1.9967	1.0002
B to Z ↑	0.0282	0.0351	8.2201	4.2410
C to Z ↓	0.0084	0.0079	2.1572	1.0440
C to Z ↑	0.0178	0.0181	8.2518	4.2577

D to Z ↓	0.0070	0.0059	2.1534	1.0524
D to Z ↑	0.0172	0.0153	8.2516	4.2540
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0228	0.0249	0.6852	0.5169
A to Z ↑	0.0304	0.0330	2.8123	2.1253
B to Z ↓	0.0208	0.0233	0.6842	0.5159
B to Z ↑	0.0307	0.0337	2.8133	2.1250
C to Z ↓	0.0082	0.0080	0.7231	0.5425
C to Z ↑	0.0173	0.0173	2.8233	2.1320
D to Z ↓	0.0062	0.0059	0.7215	0.5428
D to Z ↑	0.0157	0.0148	2.8227	2.1316

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P0	1.107e-04	1.000e-20
X13_P0	1.550e-04	1.000e-20
X19_P0	2.545e-04	1.000e-20
X25_P0	2.945e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	7.011e-04	1.087e-03	1.685e-03	1.989e-03
B (output stable)	6.578e-04	1.032e-03	1.565e-03	1.894e-03
C (output stable)	3.997e-05	1.176e-04	1.663e-04	2.254e-04
D (output stable)	9.803e-05	3.354e-04	4.160e-04	6.232e-04
A to Z	2.953e-03	5.355e-03	8.000e-03	1.020e-02
B to Z	2.833e-03	5.137e-03	7.550e-03	9.793e-03
C to Z	1.205e-03	2.406e-03	3.446e-03	4.559e-03
D to Z	1.046e-03	1.864e-03	2.826e-03	3.557e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

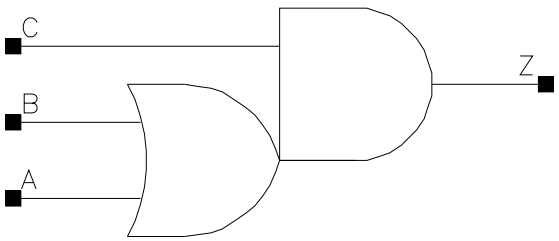
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0009	0.0009	0.0016
B	0.0010	0.0010	0.0019
C	0.0009	0.0010	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0230	0.0265	2.0729	1.0314
A to Z ↑	0.0209	0.0232	2.9967	1.4717
B to Z ↓	0.0236	0.0274	2.0763	1.0316
B to Z ↑	0.0190	0.0216	2.9885	1.4688
C to Z ↓	0.0210	0.0230	2.0548	1.0187
C to Z ↑	0.0196	0.0218	2.9909	1.4704
	X33_P0		**X33_P0**	
A to Z ↓	0.0277		0.5215	
A to Z ↑	0.0249		0.7380	

B to Z ↓	0.0285		0.5216	
B to Z ↑	0.0228		0.7377	
C to Z ↓	0.0235		0.5136	
C to Z ↑	0.0225		0.7368	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.442e-04	1.000e-20
X17_P0	2.166e-04	1.000e-20
X33_P0	4.255e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	5.197e-05	5.240e-05	1.091e-04
B (output stable)	6.136e-05	6.184e-05	1.244e-04
C (output stable)	5.913e-05	6.185e-05	1.175e-04
A to Z	2.420e-03	3.740e-03	7.818e-03
B to Z	2.242e-03	3.553e-03	7.454e-03
C to Z	2.593e-03	3.780e-03	7.781e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

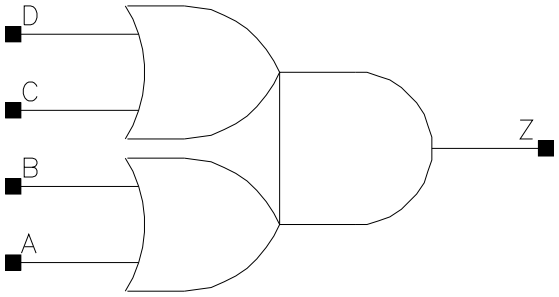
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0008	0.0017
B	0.0006	0.0009	0.0017
C	0.0006	0.0009	0.0017
D	0.0006	0.0009	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0399	0.0332	2.0102	1.0218
A to Z ↑	0.0286	0.0251	2.9311	1.4668
B to Z ↓	0.0411	0.0342	2.0102	1.0225
B to Z ↑	0.0276	0.0239	2.9266	1.4644

C to Z ↓	0.0349	0.0294	1.9937	1.0162
C to Z ↑	0.0278	0.0252	2.9268	1.4666
D to Z ↓	0.0353	0.0300	1.9925	1.0161
D to Z ↑	0.0262	0.0232	2.9242	1.4635
	X33_P0		**X33_P0**	
A to Z ↓	0.0336		0.5246	
A to Z ↑	0.0252		0.7372	
B to Z ↓	0.0334		0.5251	
B to Z ↑	0.0233		0.7352	
C to Z ↓	0.0293		0.5216	
C to Z ↑	0.0248		0.7363	
D to Z ↓	0.0287		0.5218	
D to Z ↑	0.0226		0.7348	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.044e-04	1.000e-20
X17_P0	2.265e-04	1.000e-20
X33_P0	4.342e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	1.961e-05	3.195e-05	9.160e-05
B (output stable)	2.557e-05	4.302e-05	1.963e-04
C (output stable)	4.814e-05	6.623e-05	1.576e-04
D (output stable)	5.499e-05	7.851e-05	2.625e-04
A to Z	2.844e-03	4.691e-03	9.216e-03
B to Z	2.743e-03	4.491e-03	8.641e-03
C to Z	2.513e-03	4.250e-03	8.318e-03
D to Z	2.411e-03	4.052e-03	7.719e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

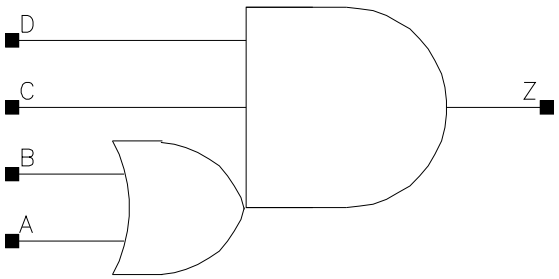
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	1.088	1.3056
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0006	0.0009	0.0014	0.0017
B	0.0006	0.0009	0.0015	0.0018
C	0.0006	0.0009	0.0015	0.0017
D	0.0006	0.0009	0.0015	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0338	0.0311	2.1137	1.0303
A to Z ↑	0.0340	0.0317	3.0436	1.4733
B to Z ↓	0.0348	0.0311	2.1143	1.0307
B to Z ↑	0.0323	0.0291	3.0339	1.4699
C to Z ↓	0.0283	0.0257	2.0741	1.0146

C to Z ↑	0.0315	0.0291	3.0366	1.4694
D to Z ↓	0.0275	0.0249	2.0724	1.0136
D to Z ↑	0.0331	0.0305	3.0371	1.4681
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0326	0.0311	0.6992	0.5238
A to Z ↑	0.0323	0.0328	0.9971	0.7483
B to Z ↓	0.0323	0.0308	0.6995	0.5241
B to Z ↑	0.0297	0.0300	0.9943	0.7460
C to Z ↓	0.0272	0.0258	0.6885	0.5159
C to Z ↑	0.0298	0.0296	0.9947	0.7457
D to Z ↓	0.0259	0.0248	0.6866	0.5153
D to Z ↑	0.0303	0.0305	0.9955	0.7458

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	9.854e-05	1.000e-20
X17_P0	2.179e-04	1.000e-20
X25_P0	3.219e-04	1.000e-20
X33_P0	4.270e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	3.545e-05	6.679e-05	1.165e-04	1.289e-04
B (output stable)	3.742e-05	7.944e-05	1.404e-04	1.543e-04
C (output stable)	1.616e-05	3.325e-05	8.229e-05	9.076e-05
D (output stable)	2.139e-05	4.113e-05	1.298e-04	1.436e-04
A to Z	2.460e-03	4.483e-03	7.115e-03	8.971e-03
B to Z	2.367e-03	4.234e-03	6.660e-03	8.369e-03
C to Z	2.522e-03	4.548e-03	7.361e-03	9.094e-03
D to Z	2.447e-03	4.403e-03	6.967e-03	8.700e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

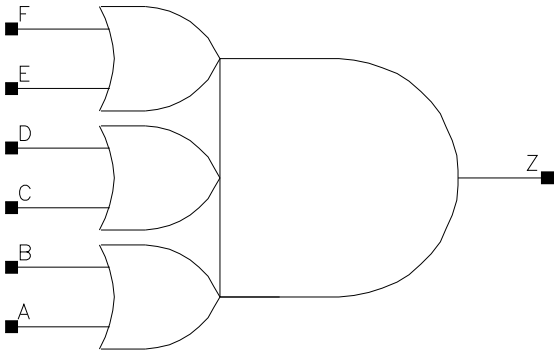
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0015
B	0.0006	0.0009	0.0017
C	0.0006	0.0009	0.0015
D	0.0006	0.0009	0.0017
E	0.0006	0.0009	0.0015
F	0.0006	0.0009	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0454	0.0381	2.1521	1.0457
A to Z ↑	0.0365	0.0333	3.0192	1.4846
B to Z ↓	0.0463	0.0392	2.1530	1.0459
B to Z ↑	0.0351	0.0320	3.0191	1.4832
C to Z ↓	0.0419	0.0361	2.1388	1.0430
C to Z ↑	0.0372	0.0334	3.0213	1.4843
D to Z ↓	0.0430	0.0371	2.1385	1.0432
D to Z ↑	0.0355	0.0318	3.0179	1.4841
E to Z ↓	0.0366	0.0319	2.1221	1.0372
E to Z ↑	0.0346	0.0318	3.0182	1.4838
F to Z ↓	0.0379	0.0328	2.1226	1.0373
F to Z ↑	0.0331	0.0301	3.0150	1.4812
	X33_P0		X33_P0	
A to Z ↓	0.0382		0.5328	
A to Z ↑	0.0339		0.7477	
B to Z ↓	0.0395		0.5329	
B to Z ↑	0.0318		0.7462	
C to Z ↓	0.0354		0.5299	
C to Z ↑	0.0340		0.7474	
D to Z ↓	0.0365		0.5301	
D to Z ↑	0.0320		0.7459	
E to Z ↓	0.0313		0.5268	
E to Z ↑	0.0324		0.7468	
F to Z ↓	0.0324		0.5271	
F to Z ↑	0.0303		0.7447	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.101e-04	1.000e-20
X17_P0	2.480e-04	1.000e-20
X33_P0	4.710e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	1.800e-05	3.128e-05	5.828e-05
B (output stable)	2.226e-05	4.232e-05	7.609e-05
C (output stable)	2.735e-05	4.436e-05	8.885e-05
D (output stable)	3.296e-05	5.384e-05	1.068e-04
E (output stable)	7.099e-05	1.037e-04	1.941e-04
F (output stable)	7.339e-05	1.106e-04	2.113e-04
A to Z	3.252e-03	5.512e-03	1.083e-02
B to Z	3.140e-03	5.318e-03	1.042e-02
C to Z	3.003e-03	5.167e-03	1.007e-02
D to Z	2.898e-03	4.970e-03	9.659e-03
E to Z	2.683e-03	4.714e-03	9.177e-03
F to Z	2.593e-03	4.530e-03	8.801e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

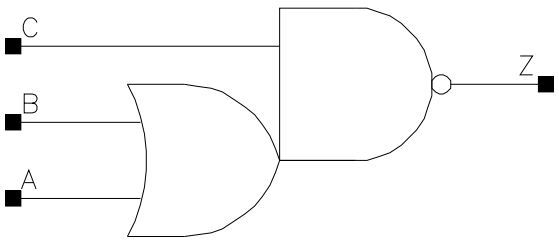
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X34_P0	1.200	2.720	3.2640
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X34_P0	X46_P0
A	0.0007	0.0021	0.0042	0.0055
B	0.0007	0.0019	0.0039	0.0052
C	0.0007	0.0022	0.0045	0.0058

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0111	0.0116	3.8363	1.2568
A to Z ↑	0.0131	0.0138	5.6878	1.9225
B to Z ↓	0.0092	0.0096	3.7662	1.2633
B to Z ↑	0.0134	0.0133	5.7043	1.9285
C to Z ↓	0.0104	0.0105	3.5042	1.1582
C to Z ↑	0.0129	0.0127	3.0263	1.0030
	X34_P0	**X46_P0**	**X34_P0**	**X46_P0**
A to Z ↓	0.0122	0.0121	0.6398	0.4876

A to Z ↑	0.0144	0.0141	0.9607	0.7360
B to Z ↓	0.0099	0.0100	0.6466	0.4943
B to Z ↑	0.0136	0.0136	0.9634	0.7380
C to Z ↓	0.0109	0.0108	0.5915	0.4513
C to Z ↑	0.0129	0.0128	0.5021	0.3834

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P0	7.893e-05	1.000e-20
X17_P0	2.316e-04	1.000e-20
X34_P0	4.578e-04	1.000e-20
X46_P0	6.046e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	4.631e-05	1.600e-04	3.417e-04	4.153e-04
B (output stable)	5.583e-05	2.059e-04	4.561e-04	5.322e-04
C (output stable)	5.416e-05	1.729e-04	3.673e-04	4.607e-04
A to Z	1.128e-03	3.557e-03	7.379e-03	9.548e-03
B to Z	9.663e-04	2.895e-03	5.941e-03	7.769e-03
C to Z	1.348e-03	4.112e-03	8.472e-03	1.097e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

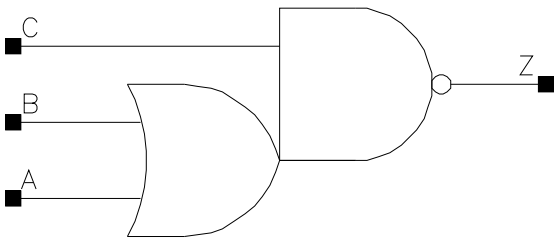
Pin Cycle (vdds)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.544	0.6528
X11_P0	1.200	0.952	1.1424
X17_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X17_P0	X23_P0
A	0.0007	0.0014	0.0022	0.0030
B	0.0007	0.0015	0.0021	0.0027
C	0.0007	0.0014	0.0020	0.0028
	X46_P0			
A	0.0060			
B	0.0055			
C	0.0056			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0113	0.0115	3.9107	1.8274
A to Z ↑	0.0166	0.0164	5.9949	2.8232
B to Z ↓	0.0097	0.0096	3.8543	1.7861

B to Z ↑	0.0170	0.0168	6.0118	2.8307
C to Z ↓	0.0094	0.0094	3.6307	1.6890
C to Z ↑	0.0100	0.0098	3.2308	1.5158
	X17_P0	**X23_P0**	**X17_P0**	**X23_P0**
A to Z ↓	0.0109	0.0117	1.2592	0.9353
A to Z ↑	0.0154	0.0171	1.8738	1.4276
B to Z ↓	0.0092	0.0096	1.2556	0.9351
B to Z ↑	0.0157	0.0164	1.8783	1.4317
C to Z ↓	0.0090	0.0093	1.1768	0.8728
C to Z ↑	0.0090	0.0094	1.0089	0.7671
	X46_P0		**X46_P0**	
A to Z ↓	0.0115		0.4855	
A to Z ↑	0.0166		0.7215	
B to Z ↓	0.0093		0.4815	
B to Z ↑	0.0160		0.7235	
C to Z ↓	0.0094		0.4518	
C to Z ↑	0.0091		0.3878	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	7.640e-05	1.000e-20
X11_P0	1.606e-04	1.000e-20
X17_P0	2.359e-04	1.000e-20
X23_P0	3.139e-04	1.000e-20
X46_P0	6.096e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	2.060e-05	4.448e-05	6.395e-05	1.185e-04
B (output stable)	2.519e-05	5.872e-05	8.301e-05	1.992e-04
C (output stable)	1.484e-04	3.567e-04	4.289e-04	6.772e-04
A to Z	1.319e-03	2.803e-03	3.927e-03	5.768e-03
B to Z	1.142e-03	2.457e-03	3.372e-03	4.720e-03
C to Z	9.988e-04	2.174e-03	3.040e-03	4.297e-03
	X46_P0			
A (output stable)	2.249e-04			
B (output stable)	3.620e-04			
C (output stable)	1.211e-03			
A to Z	1.113e-02			
B to Z	9.062e-03			
C to Z	8.263e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

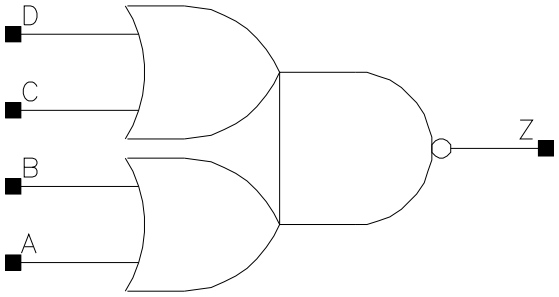
	X46_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0008	0.0015	0.0021	0.0030
B	0.0007	0.0013	0.0019	0.0027
C	0.0007	0.0014	0.0021	0.0029
D	0.0007	0.0013	0.0019	0.0026
	X42_P0			
A	0.0060			
B	0.0054			
C	0.0057			
D	0.0053			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0124	0.0135	3.5649	1.7897
A to Z ↑	0.0196	0.0194	6.3002	2.8929
B to Z ↓	0.0110	0.0115	3.5049	1.7934
B to Z ↑	0.0198	0.0186	6.3066	2.9008
C to Z ↓	0.0112	0.0124	3.6050	1.7969
C to Z ↑	0.0143	0.0149	6.1751	2.9000
D to Z ↓	0.0095	0.0099	3.5270	1.8043
D to Z ↑	0.0144	0.0135	6.1898	2.9109
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0127	0.0131	1.2221	0.8789
A to Z ↑	0.0180	0.0188	1.9455	1.4341
B to Z ↓	0.0111	0.0110	1.2267	0.8781
B to Z ↑	0.0177	0.0182	1.9504	1.4373
C to Z ↓	0.0117	0.0120	1.2289	0.8840
C to Z ↑	0.0135	0.0140	1.9513	1.4356
D to Z ↓	0.0097	0.0097	1.2398	0.8859
D to Z ↑	0.0128	0.0131	1.9583	1.4404
	X42_P0		**X42_P0**	
A to Z ↓	0.0132		0.4584	
A to Z ↑	0.0187		0.7292	
B to Z ↓	0.0112		0.4540	
B to Z ↑	0.0182		0.7305	
C to Z ↓	0.0125		0.4624	
C to Z ↑	0.0142		0.7251	
D to Z ↓	0.0101		0.4582	
D to Z ↑	0.0133		0.7279	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	9.056e-05	1.000e-20
X10_P0	1.950e-04	1.000e-20
X15_P0	2.833e-04	1.000e-20
X21_P0	3.788e-04	1.000e-20
X42_P0	7.420e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	2.813e-05	8.842e-05	1.125e-04	1.648e-04
B (output stable)	3.987e-05	1.888e-04	1.886e-04	3.121e-04
C (output stable)	5.409e-05	1.489e-04	1.854e-04	2.691e-04
D (output stable)	6.778e-05	2.488e-04	2.622e-04	4.087e-04
A to Z	1.550e-03	3.461e-03	4.735e-03	6.712e-03
B to Z	1.376e-03	2.899e-03	3.991e-03	5.650e-03
C to Z	1.179e-03	2.727e-03	3.672e-03	5.190e-03
D to Z	1.023e-03	2.174e-03	2.995e-03	4.206e-03
	X42_P0			
A (output stable)	3.262e-04			
B (output stable)	5.972e-04			
C (output stable)	5.246e-04			
D (output stable)	7.980e-04			

A to Z	1.323e-02			
B to Z	1.111e-02			
C to Z	1.034e-02			
D to Z	8.357e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

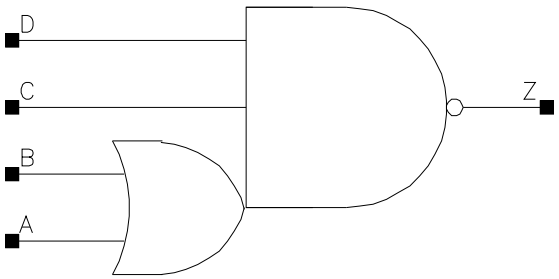
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X21_P0	1.200	2.448	2.9376
X31_P0	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X21_P0	X31_P0
A	0.0007	0.0013	0.0027	0.0041
B	0.0009	0.0013	0.0025	0.0037
C	0.0007	0.0015	0.0029	0.0044
D	0.0007	0.0014	0.0028	0.0042

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0170	0.0161	4.9615	2.6320
A to Z ↑	0.0181	0.0163	5.6712	2.8547
B to Z ↓	0.0152	0.0132	5.0051	2.6408
B to Z ↑	0.0183	0.0153	5.6981	2.8636
C to Z ↓	0.0150	0.0153	4.7026	2.4904

C to Z ↑	0.0157	0.0152	2.9401	1.4835
D to Z ↓	0.0162	0.0153	4.7229	2.5009
D to Z ↑	0.0150	0.0138	2.9730	1.4854
	X21_P0	**X31_P0**	**X21_P0**	**X31_P0**
A to Z ↓	0.0164	0.0165	1.3676	0.9267
A to Z ↑	0.0159	0.0159	1.4266	0.9575
B to Z ↓	0.0134	0.0136	1.3734	0.9331
B to Z ↑	0.0149	0.0149	1.4315	0.9610
C to Z ↓	0.0152	0.0152	1.2945	0.8783
C to Z ↑	0.0148	0.0148	0.7516	0.5071
D to Z ↓	0.0154	0.0156	1.2998	0.8817
D to Z ↑	0.0135	0.0136	0.7523	0.5063

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	6.919e-05	1.000e-20
X10_P0	1.309e-04	1.000e-20
X21_P0	2.504e-04	1.000e-20
X31_P0	3.701e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	6.771e-05	1.438e-04	2.570e-04	3.738e-04
B (output stable)	7.677e-05	1.640e-04	2.910e-04	4.230e-04
C (output stable)	3.127e-05	9.317e-05	1.757e-04	2.561e-04
D (output stable)	3.998e-05	1.449e-04	2.500e-04	3.537e-04
A to Z	1.610e-03	2.838e-03	5.492e-03	8.165e-03
B to Z	1.343e-03	2.279e-03	4.404e-03	6.580e-03
C to Z	1.877e-03	3.588e-03	6.870e-03	1.018e-02
D to Z	1.735e-03	3.123e-03	6.009e-03	8.933e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

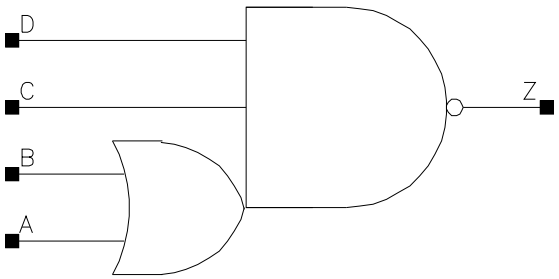
Pin Cycle (vdds)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0008	0.0015	0.0023	0.0030
B	0.0007	0.0014	0.0020	0.0028
C	0.0007	0.0014	0.0021	0.0028
D	0.0007	0.0014	0.0020	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0151	0.0164	5.0596	2.6269
A to Z ↑	0.0191	0.0208	5.5271	2.8159
B to Z ↓	0.0132	0.0139	4.9851	2.6285
B to Z ↑	0.0195	0.0201	5.5387	2.8219
C to Z ↓	0.0126	0.0141	4.7784	2.5005

C to Z ↑	0.0122	0.0129	2.9880	1.5106
D to Z ↓	0.0129	0.0137	4.7932	2.5062
D to Z ↑	0.0109	0.0110	3.0035	1.5191
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0160	0.0162	1.8027	1.3582
A to Z ↑	0.0198	0.0203	1.8954	1.4352
B to Z ↓	0.0138	0.0137	1.7975	1.3561
B to Z ↑	0.0194	0.0199	1.9002	1.4386
C to Z ↓	0.0137	0.0140	1.7118	1.2906
C to Z ↑	0.0122	0.0125	1.0091	0.7589
D to Z ↓	0.0133	0.0138	1.7158	1.2935
D to Z ↑	0.0104	0.0108	1.0141	0.7630

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	6.865e-05	1.000e-20
X10_P0	1.323e-04	1.000e-20
X15_P0	1.892e-04	1.000e-20
X21_P0	2.545e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	1.815e-05	4.007e-05	5.922e-05	7.690e-05
B (output stable)	1.959e-05	6.345e-05	7.569e-05	1.120e-04
C (output stable)	4.554e-05	1.052e-04	1.530e-04	2.085e-04
D (output stable)	7.739e-05	2.654e-04	3.085e-04	4.673e-04
A to Z	1.720e-03	3.717e-03	5.237e-03	7.190e-03
B to Z	1.512e-03	3.108e-03	4.407e-03	6.032e-03
C to Z	1.303e-03	2.837e-03	3.956e-03	5.477e-03
D to Z	1.183e-03	2.471e-03	3.489e-03	4.780e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

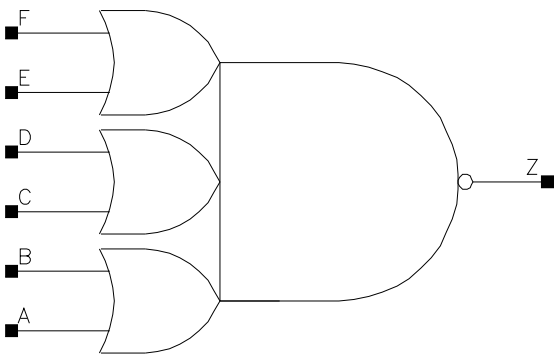
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	1.088	1.3056
X9_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X9_P0
A	0.0006	0.0015
B	0.0006	0.0014
C	0.0006	0.0015
D	0.0006	0.0013
E	0.0006	0.0014
F	0.0006	0.0013

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X9_P0	X3_P0	X9_P0
A to Z ↓	0.0192	0.0206	5.8592	2.3811
A to Z ↑	0.0268	0.0252	7.8372	2.8335
B to Z ↓	0.0180	0.0183	5.8959	2.3833
B to Z ↑	0.0279	0.0247	7.8427	2.8368
C to Z ↓	0.0188	0.0196	5.9126	2.3954
C to Z ↑	0.0233	0.0217	7.8573	2.8271
D to Z ↓	0.0173	0.0173	5.9454	2.4001
D to Z ↑	0.0242	0.0212	7.8662	2.8329
E to Z ↓	0.0163	0.0175	5.9211	2.3904
E to Z ↑	0.0183	0.0172	7.8726	2.8317
F to Z ↓	0.0150	0.0148	5.9544	2.3943
F to Z ↑	0.0191	0.0160	7.8985	2.8403

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P0	7.552e-05	1.000e-20
X9_P0	2.232e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P0	X9_P0
A (output stable)	2.474e-05	8.583e-05
B (output stable)	3.032e-05	1.508e-04
C (output stable)	3.847e-05	1.126e-04
D (output stable)	4.389e-05	1.797e-04
E (output stable)	8.846e-05	2.288e-04
F (output stable)	9.523e-05	2.903e-04
A to Z	1.917e-03	5.035e-03
B to Z	1.775e-03	4.424e-03
C to Z	1.598e-03	4.185e-03
D to Z	1.467e-03	3.649e-03
E to Z	1.242e-03	3.388e-03
F to Z	1.127e-03	2.834e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

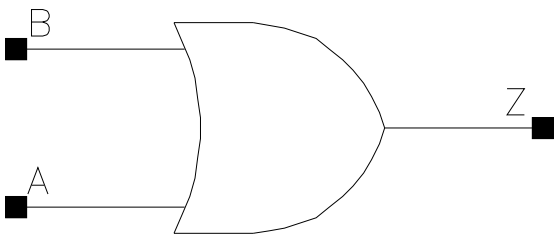
Pin Cycle (vdds)	X3_P0	X9_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X33_P0	1.200	1.360	1.6320
X50_P0	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P0	X16_P0	X33_P0	X50_P0
A	0.0007	0.0009	0.0016	0.0017
B	0.0006	0.0009	0.0017	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0307	0.0263	2.0762	1.0456
A to Z ↑	0.0195	0.0205	2.9521	1.4892
B to Z ↓	0.0312	0.0269	2.0760	1.0442
B to Z ↑	0.0184	0.0191	2.9588	1.4884
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0272	0.0321	0.5166	0.3536
A to Z ↑	0.0204	0.0202	0.7258	0.4895
B to Z ↓	0.0266	0.0319	0.5161	0.3537
B to Z ↑	0.0185	0.0187	0.7253	0.4899

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	8.154e-05	1.000e-20
X16_P0	1.662e-04	1.000e-20
X33_P0	3.307e-04	1.000e-20
X50_P0	4.306e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	1.625e-05	3.159e-05	1.057e-04	1.007e-04
B (output stable)	2.990e-05	5.231e-05	2.679e-04	2.497e-04
A to Z	2.140e-03	3.563e-03	7.430e-03	1.052e-02
B to Z	2.050e-03	3.404e-03	6.863e-03	1.001e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

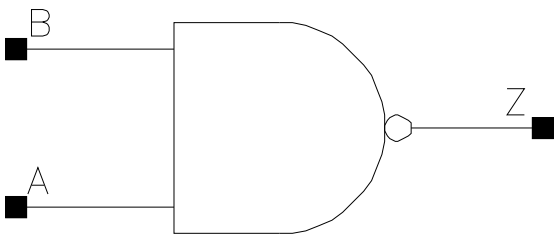
Pin Cycle (vdds)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X16_P0	1.200	0.952	1.1424
X24_P0	1.200	1.088	1.3056
X32_P0	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P0	X16_P0	X24_P0	X32_P0
A	0.0009	0.0009	0.0009	0.0009
B	0.0010	0.0010	0.0010	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0267	0.0274	2.0259	1.0502
A to Z ↑	0.0282	0.0287	2.9861	1.5201
B to Z ↓	0.0279	0.0287	2.0261	1.0513
B to Z ↑	0.0269	0.0271	2.9903	1.5205
	X24_P0	**X32_P0**	**X24_P0**	**X32_P0**
A to Z ↓	0.0301	0.0311	0.7091	0.5328
A to Z ↑	0.0307	0.0313	1.0164	0.7591
B to Z ↓	0.0314	0.0326	0.7081	0.5327
B to Z ↑	0.0291	0.0302	1.0163	0.7599

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	1.902e-04	1.000e-20
X16_P0	2.409e-04	1.000e-20
X24_P0	2.892e-04	1.000e-20
X32_P0	3.975e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	1.989e-05	2.044e-05	2.036e-05	2.086e-05
B (output stable)	3.040e-05	3.096e-05	3.036e-05	3.068e-05
A to Z	3.937e-03	4.593e-03	5.854e-03	7.722e-03
B to Z	3.825e-03	4.483e-03	5.756e-03	7.620e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

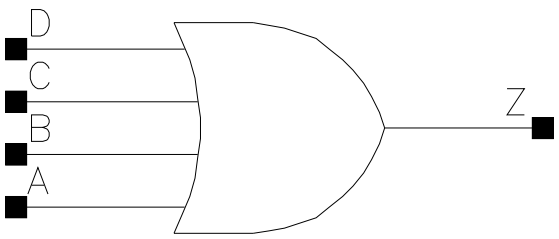
Pin Cycle (vdds)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X27_P0
A	0.0015	0.0017
B	0.0014	0.0018
C	0.0015	0.0018
D	0.0014	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	X27_P0	X20_P0	X27_P0
A to Z ↓	0.0307	0.0320	1.2367	0.9253
A to Z ↑	0.0209	0.0202	0.9713	0.7248
B to Z ↓	0.0305	0.0314	1.2365	0.9254
B to Z ↑	0.0197	0.0186	0.9703	0.7231
C to Z ↓	0.0298	0.0314	1.2345	0.9238
C to Z ↑	0.0199	0.0199	0.9728	0.7261
D to Z ↓	0.0296	0.0309	1.2333	0.9237
D to Z ↑	0.0187	0.0184	0.9719	0.7259

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X20_P0	2.614e-04	1.000e-20
X27_P0	3.803e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X20_P0	X27_P0
A (output stable)	1.417e-03	1.971e-03
B (output stable)	1.297e-03	1.805e-03
C (output stable)	1.293e-03	1.872e-03
D (output stable)	1.172e-03	1.736e-03
A to Z	6.342e-03	8.884e-03
B to Z	5.953e-03	8.276e-03
C to Z	5.801e-03	8.078e-03
D to Z	5.427e-03	7.541e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

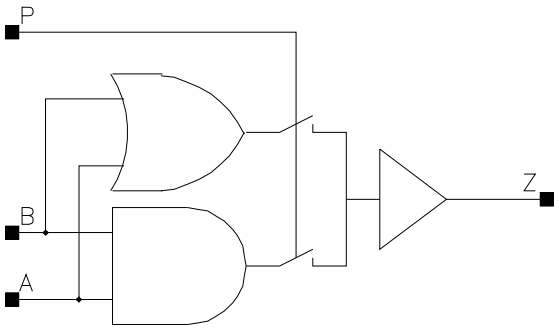
Pin Cycle (vdds)	X20_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X16_P0	1.200	1.224	1.4688
X25_P0	1.200	2.040	2.4480
X33_P0	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0011	0.0016	0.0028	0.0028
B	0.0010	0.0016	0.0032	0.0032
P	0.0006	0.0009	0.0016	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0373	0.0333	2.1158	1.0327
A to Z ↑	0.0266	0.0250	3.0050	1.4992
B to Z ↓	0.0373	0.0335	2.1205	1.0359
B to Z ↑	0.0275	0.0258	3.0054	1.5012
P to Z ↓	0.0344	0.0313	2.1178	1.0352
P to Z ↑	0.0264	0.0249	3.0014	1.4983
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**

A to Z ↓	0.0316	0.0338	0.7013	0.5298
A to Z ↑	0.0244	0.0259	1.0076	0.7546
B to Z ↓	0.0317	0.0336	0.7037	0.5317
B to Z ↑	0.0256	0.0268	1.0080	0.7553
P to Z ↓	0.0303	0.0324	0.7025	0.5311
P to Z ↑	0.0244	0.0258	1.0069	0.7533

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	9.947e-05	1.000e-20
X16_P0	2.226e-04	1.000e-20
X25_P0	3.735e-04	1.000e-20
X33_P0	4.334e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	3.773e-05	6.180e-05	1.353e-04	1.357e-04
B (output stable)	4.802e-05	8.596e-05	2.283e-04	2.268e-04
P (output stable)	1.312e-04	2.285e-04	3.421e-04	3.508e-04
A to Z	2.470e-03	4.360e-03	7.237e-03	8.732e-03
B to Z	2.428e-03	4.315e-03	7.054e-03	8.555e-03
P to Z	2.264e-03	4.084e-03	6.797e-03	8.290e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

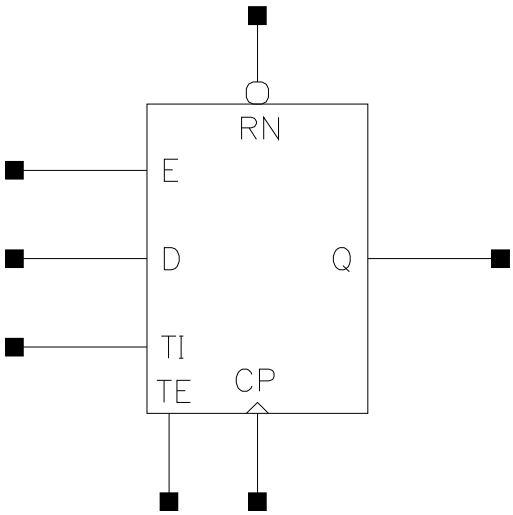
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.488	5.3856
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
E	0.0008	0.0010	0.0010	0.0010
RN	0.0008	0.0006	0.0007	0.0008
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
CP to Q ↓	0.0709	0.0371	4.4943	2.0421
CP to Q ↑	0.0598	0.0501	6.1221	2.9587
RN to Q ↓	0.0592	0.0511	3.9906	2.1195
	X17_P0	X33_P0	X17_P0	X33_P0
CP to Q ↓	0.0659	0.0690	1.0044	0.5242
CP to Q ↑	0.0813	0.0850	1.4526	0.7399
RN to Q ↓	0.0870	0.0901	1.0033	0.5239

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0926	0.0620	0.0620	0.0620
CP ↑	min_pulse_width to CP	0.0658	0.0318	0.0284	0.0318
D ↓	hold_rising to CP	-0.0936	-0.0408	-0.0440	-0.0440
D ↑	hold_rising to CP	-0.0621	-0.0191	-0.0191	-0.0191
D ↓	setup_rising to CP	0.1388	0.0831	0.0831	0.0831
D ↑	setup_rising to CP	0.0974	0.0488	0.0488	0.0488
E ↓	hold_rising to CP	-0.0724	-0.0750	-0.0745	-0.0745
E ↑	hold_rising to CP	-0.0604	-0.0193	-0.0193	-0.0193
E ↓	setup_rising to CP	0.1220	0.1197	0.1197	0.1197
E ↑	setup_rising to CP	0.1297	0.0879	0.0879	0.0879
RN ↓	min_pulse_width to RN	0.0637	0.0686	0.0615	0.0615
RN ↑	recovery_rising to CP	0.0151	0.0125	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0104	-0.0030	-0.0030	-0.0030
TE ↓	hold_rising to CP	-0.0435	-0.0262	-0.0262	-0.0262
TE ↑	hold_rising to CP	-0.0409	-0.0262	-0.0262	-0.0262
TE ↓	setup_rising to CP	0.0900	0.0749	0.0749	0.0749
TE ↑	setup_rising to CP	0.1714	0.1204	0.1171	0.1204
TI ↓	hold_rising to CP	-0.1240	-0.0627	-0.0627	-0.0627
TI ↑	hold_rising to CP	-0.0524	-0.0244	-0.0244	-0.0287
TI ↓	setup_rising to CP	0.1677	0.1071	0.1078	0.1071
TI ↑	setup_rising to CP	0.0820	0.0584	0.0584	0.0584

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.827e-04	1.000e-20
X8_P0	3.301e-04	1.000e-20
X17_P0	4.328e-04	1.000e-20
X33_P0	5.846e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

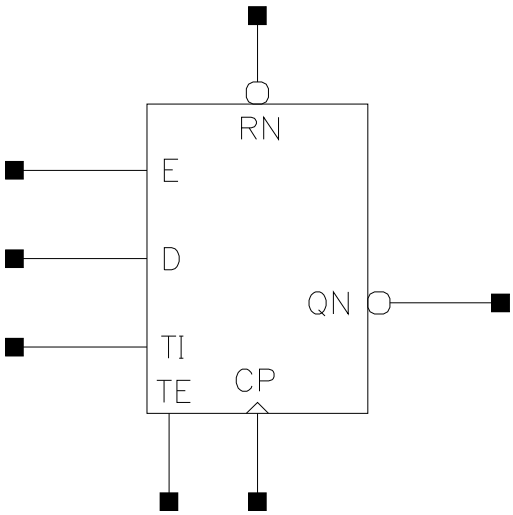
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	7.194e-03	7.227e-03	7.234e-03	7.237e-03
Clock 100Mhz Data 25Mhz	7.867e-03	7.849e-03	8.405e-03	9.180e-03
Clock 100Mhz Data 50Mhz	8.541e-03	8.472e-03	9.577e-03	1.112e-02
Clock = 0 Data 100Mhz	5.676e-03	5.244e-03	5.099e-03	5.027e-03
Clock = 1 Data 100Mhz	1.850e-03	1.882e-03	1.893e-03	1.899e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.624	5.5488
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
E	0.0008	0.0010	0.0010	0.0010
RN	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
CP to QN ↓	0.0734	0.0682	3.9289	1.9889
CP to QN ↑	0.0802	0.0507	5.9994	2.8858
RN to QN ↑	0.0737	0.0734	5.9794	2.8845
	X17_P0	X33_P0	X17_P0	X33_P0
CP to QN ↓	0.0644	0.0677	1.0041	0.5240
CP to QN ↑	0.0514	0.0557	1.4538	0.7410
RN to QN ↑	0.0708	0.0779	1.4567	0.7423

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0926	0.0620	0.0620	0.0620
CP ↑	min_pulse_width to CP	0.0488	0.0284	0.0318	0.0318
D ↓	hold_rising to CP	-0.0936	-0.0440	-0.0408	-0.0408
D ↑	hold_rising to CP	-0.0621	-0.0191	-0.0191	-0.0191
D ↓	setup_rising to CP	0.1388	0.0831	0.0831	0.0831
D ↑	setup_rising to CP	0.0974	0.0488	0.0488	0.0488
E ↓	hold_rising to CP	-0.0724	-0.0745	-0.0750	-0.0750
E ↑	hold_rising to CP	-0.0604	-0.0193	-0.0193	-0.0193
E ↓	setup_rising to CP	0.1220	0.1197	0.1197	0.1197
E ↑	setup_rising to CP	0.1297	0.0879	0.0879	0.0879
RN ↓	min_pulse_width to RN	0.0588	0.0615	0.0708	0.0757
RN ↑	recovery_rising to CP	0.0151	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0104	-0.0056	-0.0030	-0.0030
TE ↓	hold_rising to CP	-0.0425	-0.0262	-0.0262	-0.0262
TE ↑	hold_rising to CP	-0.0409	-0.0262	-0.0262	-0.0262
TE ↓	setup_rising to CP	0.0900	0.0749	0.0749	0.0749
TE ↑	setup_rising to CP	0.1714	0.1204	0.1204	0.1204
TI ↓	hold_rising to CP	-0.1240	-0.0627	-0.0627	-0.0627
TI ↑	hold_rising to CP	-0.0524	-0.0244	-0.0244	-0.0244
TI ↓	setup_rising to CP	0.1677	0.1071	0.1071	0.1071
TI ↑	setup_rising to CP	0.0820	0.0584	0.0584	0.0584

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.835e-04	1.000e-20
X8_P0	3.204e-04	1.000e-20
X17_P0	4.128e-04	1.000e-20
X33_P0	5.430e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

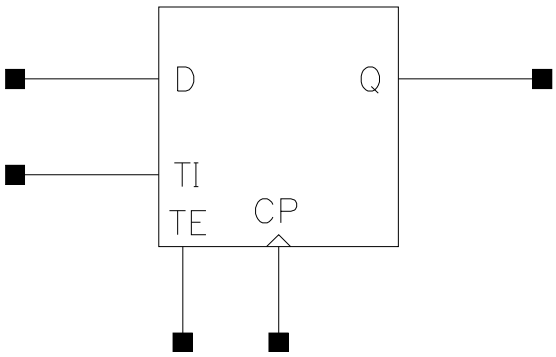
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	7.193e-03	7.226e-03	7.228e-03	7.229e-03
Clock 100Mhz Data 25Mhz	7.749e-03	7.870e-03	8.381e-03	9.158e-03
Clock 100Mhz Data 50Mhz	8.305e-03	8.515e-03	9.533e-03	1.109e-02
Clock = 0 Data 100Mhz	5.680e-03	5.246e-03	5.101e-03	5.030e-03
Clock = 1 Data 100Mhz	1.848e-03	1.882e-03	1.894e-03	1.901e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.400	4.0800
X8_P0	1.200	3.128	3.7536
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0581	0.0346	4.2345	2.0416
CP to Q ↑	0.0533	0.0452	6.1558	2.9245
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0534	0.0582	0.9887	0.5163
CP to Q ↑	0.0771	0.0815	1.4531	0.7400

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0856	0.0906	0.0905	0.0905
CP ↑	min_pulse_width to CP	0.0471	0.0271	0.0271	0.0271
D ↓	hold_rising to CP	-0.0577	-0.0218	-0.0218	-0.0218
D ↑	hold_rising to CP	-0.0234	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0927	0.0613	0.0586	0.0613
D ↑	setup_rising to CP	0.0514	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0376	-0.0169	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0311	-0.0195	-0.0195	-0.0195
TE ↓	setup_rising to CP	0.0782	0.0564	0.0564	0.0564
TE ↑	setup_rising to CP	0.1487	0.1204	0.1204	0.1204
TI ↓	hold_rising to CP	-0.1191	-0.0732	-0.0732	-0.0732
TI ↑	hold_rising to CP	-0.0377	-0.0203	-0.0203	-0.0203
TI ↓	setup_rising to CP	0.1579	0.1176	0.1176	0.1176
TI ↑	setup_rising to CP	0.0674	0.0459	0.0459	0.0459

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.306e-04	1.000e-20
X8_P0	2.803e-04	1.000e-20
X17_P0	4.143e-04	1.000e-20
X33_P0	5.298e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

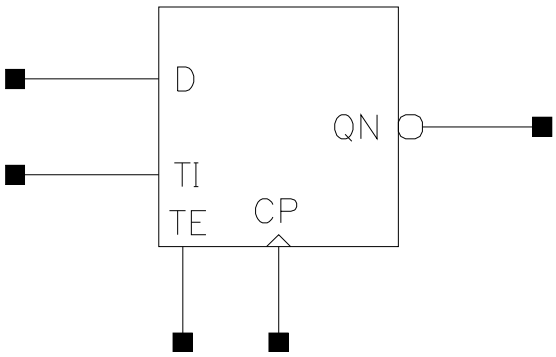
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	6.481e-03	6.509e-03	6.514e-03	6.516e-03
Clock 100Mhz Data 25Mhz	6.573e-03	6.575e-03	7.142e-03	7.805e-03
Clock 100Mhz Data 50Mhz	6.665e-03	6.641e-03	7.770e-03	9.094e-03
Clock = 0 Data 100Mhz	4.347e-03	3.994e-03	3.877e-03	3.820e-03
Clock = 1 Data 100Mhz	1.051e-03	5.443e-04	3.755e-04	2.911e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.536	4.2432
X8_P0	1.200	3.264	3.9168
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0680	0.0710	4.4895	2.0347
CP to QN ↑	0.0633	0.0467	6.1101	2.8896
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0544	0.0598	0.9894	0.5165
CP to QN ↑	0.0448	0.0495	1.4522	0.7396

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0856	0.0905	0.0906	0.0906
CP ↑	min_pulse_width to CP	0.0377	0.0271	0.0271	0.0271
D ↓	hold_rising to CP	-0.0577	-0.0218	-0.0218	-0.0218
D ↑	hold_rising to CP	-0.0234	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0895	0.0586	0.0613	0.0613
D ↑	setup_rising to CP	0.0514	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0376	-0.0169	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0332	-0.0195	-0.0195	-0.0195
TE ↓	setup_rising to CP	0.0756	0.0537	0.0564	0.0564
TE ↑	setup_rising to CP	0.1492	0.1204	0.1204	0.1204
TI ↓	hold_rising to CP	-0.1191	-0.0732	-0.0732	-0.0732
TI ↑	hold_rising to CP	-0.0367	-0.0203	-0.0203	-0.0203
TI ↓	setup_rising to CP	0.1536	0.1176	0.1176	0.1176
TI ↑	setup_rising to CP	0.0674	0.0459	0.0459	0.0459

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.336e-04	1.000e-20
X8_P0	2.820e-04	1.000e-20
X17_P0	4.107e-04	1.000e-20
X33_P0	5.261e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

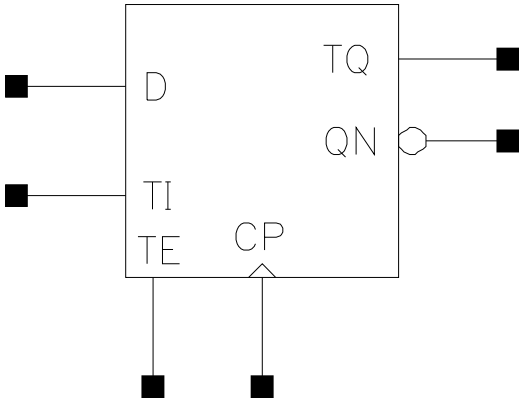
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	6.417e-03	6.475e-03	6.492e-03	6.501e-03
Clock 100Mhz Data 25Mhz	6.496e-03	6.659e-03	7.088e-03	7.774e-03
Clock 100Mhz Data 50Mhz	6.575e-03	6.843e-03	7.684e-03	9.047e-03
Clock = 0 Data 100Mhz	4.374e-03	4.006e-03	3.885e-03	3.825e-03
Clock = 1 Data 100Mhz	1.044e-03	5.409e-04	3.731e-04	2.893e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.536	4.2432
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0011	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0009

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0756	0.0639	4.0405	1.9999
CP to QN ↑	0.0760	0.0475	5.9908	2.8984
CP to TQ ↓	0.0529	0.0316	5.5416	3.8283
CP to TQ ↑	0.0551	0.0452	11.4800	8.1507
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0600	0.0645	1.0077	0.5257
CP to QN ↑	0.0487	0.0520	1.4690	0.7520
CP to TQ ↓	0.0326	0.0338	5.2338	5.2315
CP to TQ ↑	0.0460	0.0473	10.6288	11.2598

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0856	0.0906	0.0906	0.0906
CP ↑	min_pulse_width to CP	0.0471	0.0271	0.0271	0.0318
D ↓	hold_rising to CP	-0.0577	-0.0218	-0.0218	-0.0218
D ↑	hold_rising to CP	-0.0234	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0895	0.0554	0.0586	0.0586
D ↑	setup_rising to CP	0.0514	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0376	-0.0169	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0332	-0.0195	-0.0195	-0.0195
TE ↓	setup_rising to CP	0.0724	0.0537	0.0537	0.0537
TE ↑	setup_rising to CP	0.1492	0.1204	0.1204	0.1204
TI ↓	hold_rising to CP	-0.1191	-0.0732	-0.0732	-0.0732
TI ↑	hold_rising to CP	-0.0374	-0.0203	-0.0203	-0.0203
TI ↓	setup_rising to CP	0.1536	0.1176	0.1176	0.1176
TI ↑	setup_rising to CP	0.0674	0.0459	0.0459	0.0459

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.482e-04	1.000e-20
X8_P0	3.122e-04	1.000e-20
X17_P0	3.856e-04	1.000e-20
X33_P0	5.213e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0

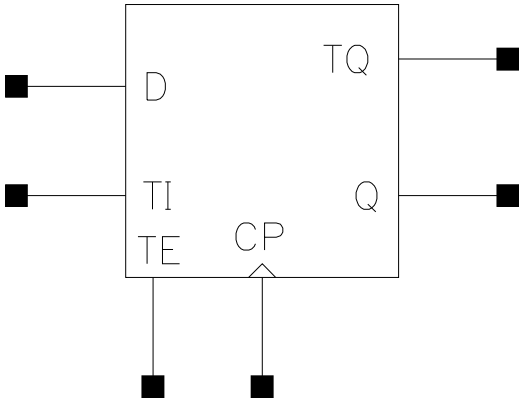
Clock 100Mhz Data 0Mhz	6.582e-03	6.562e-03	6.555e-03	6.553e-03
Clock 100Mhz Data 25Mhz	6.808e-03	6.892e-03	7.153e-03	7.929e-03
Clock 100Mhz Data 50Mhz	7.034e-03	7.222e-03	7.751e-03	9.305e-03
Clock = 0 Data 100Mhz	4.369e-03	4.011e-03	3.892e-03	3.833e-03
Clock = 1 Data 100Mhz	1.051e-03	5.443e-04	3.755e-04	2.910e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.400	4.0800
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006

TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0775	0.0388	4.4378	2.0325
CP to Q ↑	0.0616	0.0481	6.2175	2.9414
CP to TQ ↓	0.0727	0.0395	4.4312	5.3423
CP to TQ ↑	0.0635	0.0535	8.2283	11.4734
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0547	0.0597	1.0126	0.5251
CP to Q ↑	0.0785	0.0828	1.4808	0.7431
CP to TQ ↓	0.0566	0.0620	5.1706	5.2476
CP to TQ ↑	0.0838	0.0901	11.0735	11.1867

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0856	0.0906	0.0905	0.0905
CP ↑	min_pulse_width to CP	0.0693	0.0318	0.0271	0.0271
D ↓	hold_rising to CP	-0.0577	-0.0192	-0.0218	-0.0218
D ↑	hold_rising to CP	-0.0234	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0927	0.0586	0.0613	0.0586
D ↑	setup_rising to CP	0.0514	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0376	-0.0143	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0332	-0.0196	-0.0195	-0.0195
TE ↓	setup_rising to CP	0.0782	0.0537	0.0564	0.0537
TE ↑	setup_rising to CP	0.1513	0.1204	0.1204	0.1204
TI ↓	hold_rising to CP	-0.1191	-0.0732	-0.0732	-0.0732
TI ↑	hold_rising to CP	-0.0374	-0.0203	-0.0203	-0.0203
TI ↓	setup_rising to CP	0.1579	0.1176	0.1176	0.1176
TI ↑	setup_rising to CP	0.0674	0.0459	0.0459	0.0459

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.526e-04	1.000e-20
X8_P0	2.935e-04	1.000e-20
X17_P0	4.245e-04	1.000e-20
X33_P0	5.396e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

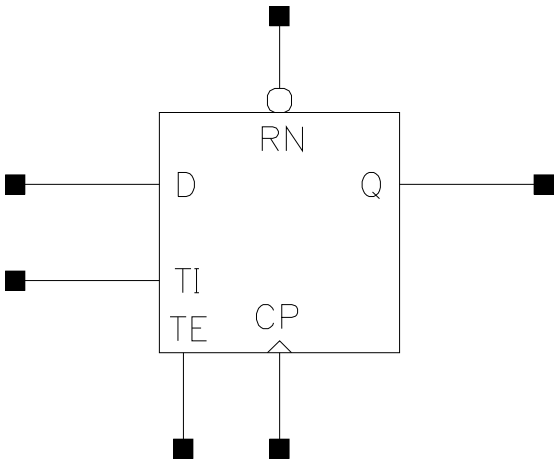
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	6.457e-03	6.497e-03	6.505e-03	6.510e-03
Clock 100Mhz Data 25Mhz	6.986e-03	6.784e-03	7.299e-03	8.020e-03
Clock 100Mhz Data 50Mhz	7.515e-03	7.072e-03	8.093e-03	9.529e-03
Clock = 0 Data 100Mhz	4.345e-03	3.992e-03	3.877e-03	3.819e-03
Clock = 1 Data 100Mhz	1.041e-03	5.396e-04	3.723e-04	2.886e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.672	4.4064
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
RN	0.0008	0.0006	0.0007	0.0007
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0703	0.0370	4.5490	2.0468
CP to Q ↑	0.0591	0.0490	6.1561	2.9576
RN to Q ↓	0.0586	0.0521	4.0404	2.1028
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0558	0.0610	0.9988	0.5230
CP to Q ↑	0.0715	0.0757	1.4504	0.7389
RN to Q ↓	0.0774	0.0827	0.9971	0.5219

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0951	0.0912	0.0911	0.0911
CP ↑	min_pulse_width to CP	0.0611	0.0283	0.0271	0.0271
D ↓	hold_rising to CP	-0.0501	-0.0094	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0283	-0.0045	-0.0040	-0.0040
D ↓	setup_rising to CP	0.0901	0.0564	0.0564	0.0564
D ↑	setup_rising to CP	0.0579	0.0347	0.0347	0.0347
RN ↓	min_pulse_width to RN	0.0588	0.0637	0.0593	0.0615
RN ↑	recovery_rising to CP	0.0146	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0104	-0.0056	-0.0029	-0.0029
TE ↓	hold_rising to CP	-0.0328	-0.0071	-0.0066	-0.0066
TE ↑	hold_rising to CP	-0.0409	-0.0235	-0.0293	-0.0293
TE ↓	setup_rising to CP	0.0749	0.0586	0.0586	0.0586
TE ↑	setup_rising to CP	0.1444	0.1102	0.1128	0.1128
TI ↓	hold_rising to CP	-0.1085	-0.0527	-0.0570	-0.0570
TI ↑	hold_rising to CP	-0.0475	-0.0260	-0.0300	-0.0300
TI ↓	setup_rising to CP	0.1530	0.1078	0.1078	0.1078
TI ↑	setup_rising to CP	0.0771	0.0599	0.0597	0.0597

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.620e-04	1.000e-20
X8_P0	3.014e-04	1.000e-20
X17_P0	4.287e-04	1.000e-20
X33_P0	5.579e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	7.194e-03	7.201e-03	7.238e-03	7.257e-03

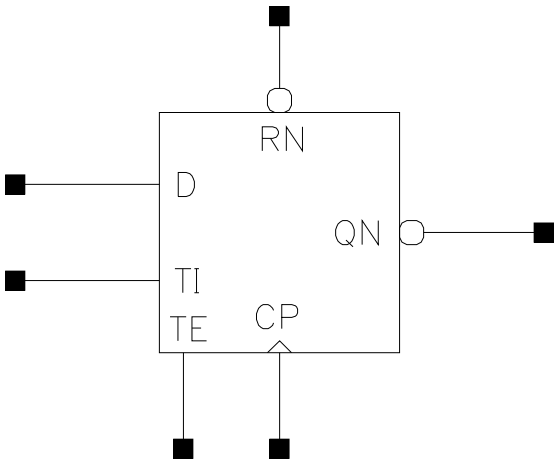
Clock 100Mhz Data 25Mhz	7.390e-03	7.230e-03	7.831e-03	8.531e-03
Clock 100Mhz Data 50Mhz	7.585e-03	7.258e-03	8.425e-03	9.804e-03
Clock = 0 Data 100Mhz	4.333e-03	3.916e-03	3.782e-03	3.715e-03
Clock = 1 Data 100Mhz	1.070e-03	5.553e-04	3.837e-04	2.978e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	3.944	4.7328
X33_P0	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0659	0.0605	3.8563	1.9475
CP to QN ↑	0.0726	0.0451	5.9927	2.8714
RN to QN ↑	0.0676	0.0685	5.9616	2.8648
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0593	0.0650	1.0005	0.5226
CP to QN ↑	0.0487	0.0539	1.4627	0.7461
RN to QN ↑	0.0690	0.0756	1.4652	0.7471

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0944	0.0912	0.0912	0.0912
CP ↑	min_pulse_width to CP	0.0458	0.0271	0.0318	0.0318
D ↓	hold_rising to CP	-0.0501	-0.0120	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0283	-0.0045	-0.0045	-0.0045
D ↓	setup_rising to CP	0.0901	0.0564	0.0564	0.0564
D ↑	setup_rising to CP	0.0579	0.0347	0.0347	0.0347
RN ↓	min_pulse_width to RN	0.0588	0.0593	0.0708	0.0708
RN ↑	recovery_rising to CP	0.0151	0.0146	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0104	-0.0051	-0.0056	-0.0056
TE ↓	hold_rising to CP	-0.0360	-0.0066	-0.0071	-0.0071
TE ↑	hold_rising to CP	-0.0409	-0.0235	-0.0235	-0.0235
TE ↓	setup_rising to CP	0.0749	0.0586	0.0586	0.0586
TE ↑	setup_rising to CP	0.1444	0.1102	0.1128	0.1128
TI ↓	hold_rising to CP	-0.1085	-0.0570	-0.0530	-0.0530
TI ↑	hold_rising to CP	-0.0475	-0.0260	-0.0260	-0.0260
TI ↓	setup_rising to CP	0.1530	0.1078	0.1078	0.1078
TI ↑	setup_rising to CP	0.0771	0.0557	0.0599	0.0599

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.651e-04	1.000e-20
X8_P0	2.916e-04	1.000e-20
X17_P0	4.155e-04	1.000e-20
X33_P0	5.153e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	7.128e-03	7.167e-03	7.179e-03	7.185e-03

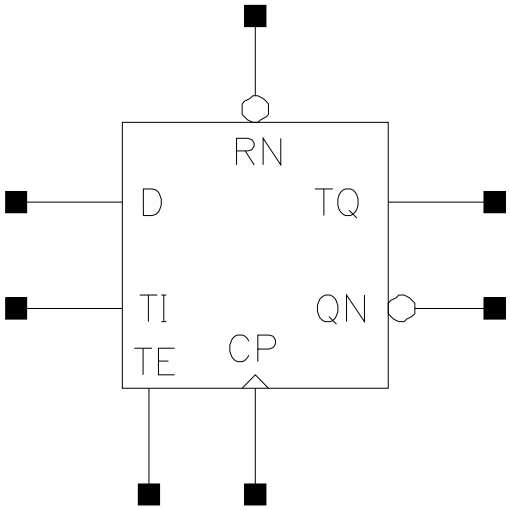
Clock 100Mhz Data 25Mhz	7.170e-03	7.184e-03	7.750e-03	8.456e-03
Clock 100Mhz Data 50Mhz	7.212e-03	7.200e-03	8.321e-03	9.726e-03
Clock = 0 Data 100Mhz	4.327e-03	3.912e-03	3.778e-03	3.712e-03
Clock = 1 Data 100Mhz	1.069e-03	5.544e-04	3.829e-04	2.973e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006

RN	0.0009	0.0006	0.0007	0.0007
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0735	0.0626	3.8685	2.0514
CP to QN ↑	0.0936	0.0501	5.3655	2.9767
CP to TQ ↓	0.0659	0.0336	4.8604	4.0164
CP to TQ ↑	0.0617	0.0498	9.2907	8.5963
RN to QN ↑	0.0663	0.0662	5.4058	2.9701
RN to TQ ↓	0.0454	0.0446	4.4381	4.1587
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0644	0.0691	1.0158	0.5319
CP to QN ↑	0.0503	0.0530	1.4855	0.7493
CP to TQ ↓	0.0350	0.0361	5.0694	4.9568
CP to TQ ↑	0.0497	0.0508	8.0492	8.1583
RN to QN ↑	0.0681	0.0724	1.4826	0.7474
RN to TQ ↓	0.0480	0.0499	5.2042	5.1102

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0944	0.0912	0.0911	0.0911
CP ↑	min_pulse_width to CP	0.0646	0.0284	0.0284	0.0318
D ↓	hold_rising to CP	-0.0501	-0.0094	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0283	-0.0045	-0.0045	-0.0045
D ↓	setup_rising to CP	0.0901	0.0564	0.0564	0.0564
D ↑	setup_rising to CP	0.0579	0.0347	0.0347	0.0347
RN ↓	min_pulse_width to RN	0.0637	0.0637	0.0659	0.0708
RN ↑	recovery_rising to CP	0.0200	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0119	-0.0056	-0.0056	-0.0056
TE ↓	hold_rising to CP	-0.0328	-0.0071	-0.0071	-0.0071
TE ↑	hold_rising to CP	-0.0409	-0.0235	-0.0235	-0.0235
TE ↓	setup_rising to CP	0.0749	0.0586	0.0586	0.0586
TE ↑	setup_rising to CP	0.1444	0.1102	0.1128	0.1128
TI ↓	hold_rising to CP	-0.1085	-0.0527	-0.0527	-0.0530
TI ↑	hold_rising to CP	-0.0475	-0.0260	-0.0257	-0.0260
TI ↓	setup_rising to CP	0.1530	0.1078	0.1078	0.1078
TI ↑	setup_rising to CP	0.0764	0.0599	0.0597	0.0597

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.930e-04	1.000e-20
X8_P0	3.081e-04	1.000e-20
X17_P0	3.791e-04	1.000e-20
X33_P0	5.004e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

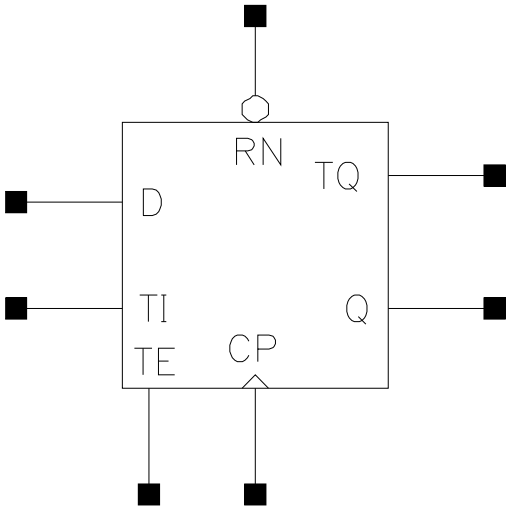
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	7.133e-03	7.168e-03	7.217e-03	7.242e-03
Clock 100Mhz Data 25Mhz	7.455e-03	7.332e-03	7.697e-03	8.512e-03
Clock 100Mhz Data 50Mhz	7.777e-03	7.496e-03	8.176e-03	9.783e-03
Clock = 0 Data 100Mhz	4.327e-03	3.912e-03	3.775e-03	3.707e-03
Clock = 1 Data 100Mhz	1.069e-03	5.544e-04	3.831e-04	2.975e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006

RN	0.0008	0.0008	0.0007	0.0007
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0789	0.0401	4.7543	2.0941
CP to Q ↑	0.0631	0.0512	6.3651	3.0482
CP to TQ ↓	0.0728	0.0392	6.0779	5.3639
CP to TQ ↑	0.0660	0.0544	12.5437	11.3813
RN to Q ↓	0.0604	0.0590	4.1945	2.1560
RN to TQ ↓	0.0587	0.0559	5.4404	5.5188
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0580	0.0632	1.0116	0.5294
CP to Q ↑	0.0725	0.0766	1.4579	0.7418
CP to TQ ↓	0.0599	0.0661	5.2015	5.2712
CP to TQ ↑	0.0776	0.0842	11.1961	11.2409
RN to Q ↓	0.0797	0.0848	1.0106	0.5287
RN to TQ ↓	0.0816	0.0878	5.1962	5.2682

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0951	0.0912	0.0912	0.0912
CP ↑	min_pulse_width to CP	0.0705	0.0318	0.0271	0.0271
D ↓	hold_rising to CP	-0.0501	-0.0094	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0283	-0.0045	-0.0045	-0.0045
D ↓	setup_rising to CP	0.0901	0.0564	0.0564	0.0564
D ↑	setup_rising to CP	0.0579	0.0347	0.0347	0.0347
RN ↓	min_pulse_width to RN	0.0637	0.0735	0.0593	0.0615
RN ↑	recovery_rising to CP	0.0151	0.0146	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0104	-0.0056	-0.0056	-0.0056
TE ↓	hold_rising to CP	-0.0328	-0.0045	-0.0066	-0.0066
TE ↑	hold_rising to CP	-0.0409	-0.0235	-0.0235	-0.0235
TE ↓	setup_rising to CP	0.0749	0.0586	0.0586	0.0586
TE ↑	setup_rising to CP	0.1444	0.1102	0.1102	0.1102
TI ↓	hold_rising to CP	-0.1085	-0.0530	-0.0570	-0.0570
TI ↑	hold_rising to CP	-0.0475	-0.0260	-0.0260	-0.0260
TI ↓	setup_rising to CP	0.1530	0.1078	0.1078	0.1078
TI ↑	setup_rising to CP	0.0771	0.0599	0.0557	0.0557

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.711e-04	1.000e-20
X8_P0	3.130e-04	1.000e-20
X17_P0	4.350e-04	1.000e-20
X33_P0	5.644e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

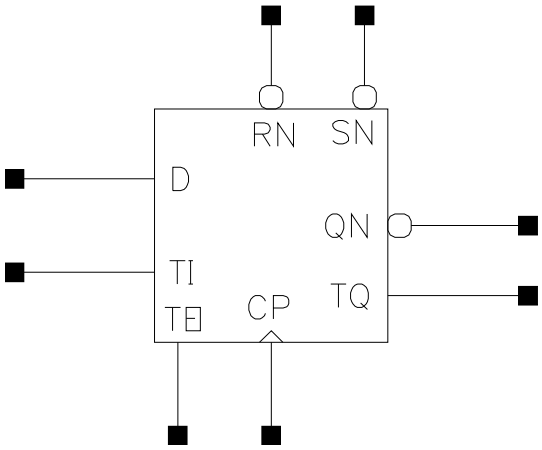
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	7.181e-03	7.193e-03	7.195e-03	7.197e-03
Clock 100Mhz Data 25Mhz	7.593e-03	7.381e-03	7.964e-03	8.682e-03
Clock 100Mhz Data 50Mhz	8.005e-03	7.570e-03	8.733e-03	1.017e-02
Clock = 0 Data 100Mhz	4.333e-03	3.916e-03	3.778e-03	3.709e-03
Clock = 1 Data 100Mhz	1.070e-03	5.554e-04	3.837e-04	2.978e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.352	5.2224
X17_P0	1.200	4.488	5.3856
X33_P0	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0005	0.0005	0.0005
RN	0.0007	0.0007	0.0007

SN	0.0012	0.0012	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0698	0.0738	1.9816	1.0190
CP to QN ↑	0.0519	0.0544	2.8889	1.4629
CP to TQ ↓	0.0395	0.0394	6.5536	6.5520
CP to TQ ↑	0.0587	0.0586	14.7026	14.7145
RN to QN ↓	0.0763	0.0803	1.9810	1.0191
RN to QN ↑	0.0737	0.0773	2.8889	1.4652
RN to TQ ↓	0.0559	0.0556	6.9154	6.9208
RN to TQ ↑	0.0654	0.0654	14.6863	14.6927
SN to QN ↓	0.0823	0.0872	1.9891	1.0228
SN to TQ ↑	0.0700	0.0698	14.8691	14.8727
	X33_P0		**X33_P0**	
CP to QN ↓	0.0840		0.5372	
CP to QN ↑	0.0609		0.7476	
CP to TQ ↓	0.0395		6.5591	
CP to TQ ↑	0.0588		14.7513	
RN to QN ↓	0.0903		0.5373	
RN to QN ↑	0.0858		0.7473	
RN to TQ ↓	0.0555		6.9282	
RN to TQ ↑	0.0656		14.7152	
SN to QN ↓	0.0987		0.5376	
SN to TQ ↑	0.0698		14.9147	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0966	0.0966	0.0966
CP ↑	min_pulse_width to CP	0.0318	0.0318	0.0330
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0045	-0.0045	-0.0045
D ↓	setup_rising to CP	0.0613	0.0613	0.0613
D ↑	setup_rising to CP	0.0343	0.0343	0.0343
RN ↓	min_pulse_width to RN	0.0708	0.0708	0.0757
RN ↑	non_seq_hold_rising to SN	-0.0286	-0.0286	-0.0286
RN ↑	non_seq_setup_rising to SN	0.0622	0.0622	0.0622
RN ↑	recovery_rising to CP	0.0248	0.0248	0.0244
RN ↑	removal_rising to CP	-0.0152	-0.0152	-0.0152
SN ↓	min_pulse_width to SN	0.0598	0.0647	0.0674
SN ↑	recovery_rising to CP	0.0048	0.0048	0.0048
SN ↑	removal_rising to CP	0.0308	0.0308	0.0308

TE ↓	hold_rising to CP	-0.0098	-0.0098	-0.0098
TE ↑	hold_rising to CP	-0.0235	-0.0240	-0.0240
TE ↓	setup_rising to CP	0.0613	0.0613	0.0613
TE ↑	setup_rising to CP	0.1177	0.1177	0.1177
TI ↓	hold_rising to CP	-0.0586	-0.0586	-0.0586
TI ↑	hold_rising to CP	-0.0251	-0.0251	-0.0251
TI ↓	setup_rising to CP	0.1163	0.1163	0.1163
TI ↑	setup_rising to CP	0.0597	0.0597	0.0597

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	3.406e-04	1.000e-20
X17_P0	3.978e-04	1.000e-20
X33_P0	5.044e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

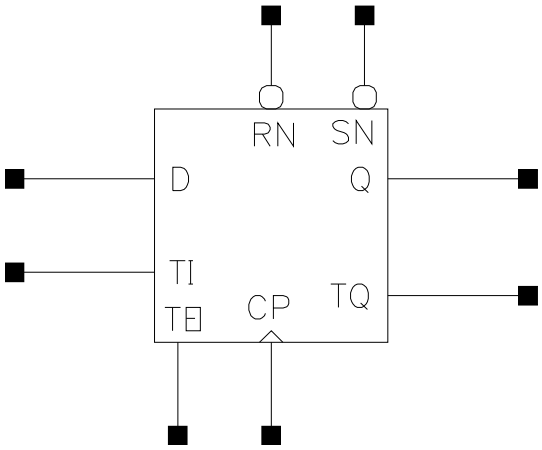
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	7.596e-03	7.596e-03	7.597e-03
Clock 100Mhz Data 25Mhz	7.666e-03	8.010e-03	8.995e-03
Clock 100Mhz Data 50Mhz	7.736e-03	8.423e-03	1.039e-02
Clock = 0 Data 100Mhz	3.613e-03	3.614e-03	3.614e-03
Clock = 1 Data 100Mhz	4.009e-05	3.997e-05	4.020e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.216	5.0592
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0005	0.0005	0.0005
RN	0.0007	0.0007	0.0007

SN	0.0012	0.0012	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0439	0.0490	2.0395	1.0547
CP to Q ↑	0.0564	0.0595	2.9553	1.5031
CP to TQ ↓	0.0440	0.0492	6.6323	6.6974
CP to TQ ↑	0.0629	0.0692	14.4551	14.5462
RN to Q ↓	0.0671	0.0777	2.2471	1.1636
RN to Q ↑	0.0520	0.0592	3.0509	1.5553
RN to TQ ↓	0.0642	0.0737	7.0588	7.1924
RN to TQ ↑	0.0629	0.0755	14.5719	14.6551
SN to Q ↑	0.0695	0.0765	3.0521	1.5542
SN to TQ ↑	0.0804	0.0927	14.5819	14.6551
	X33_P0		**X33_P0**	
CP to Q ↓	0.0617		0.5617	
CP to Q ↑	0.0682		0.7765	
CP to TQ ↓	0.0584		6.8864	
CP to TQ ↑	0.0814		14.6754	
RN to Q ↓	0.1029		0.6271	
RN to Q ↑	0.0769		0.8091	
RN to TQ ↓	0.0909		7.5372	
RN to TQ ↑	0.1003		14.7932	
SN to Q ↑	0.0939		0.8094	
SN to TQ ↑	0.1173		14.7944	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0966	0.0983	0.0983
CP ↑	min_pulse_width to CP	0.0330	0.0412	0.0518
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0094
D ↑	hold_rising to CP	-0.0045	-0.0050	-0.0050
D ↓	setup_rising to CP	0.0613	0.0613	0.0613
D ↑	setup_rising to CP	0.0343	0.0343	0.0343
RN ↓	min_pulse_width to RN	0.0806	0.0952	0.1196
RN ↑	non_seq_hold_rising to SN	-0.0286	-0.0334	-0.0481
RN ↑	non_seq_setup_rising to SN	0.0571	0.0594	0.0845
RN ↑	recovery_rising to CP	0.0191	0.0191	0.0217
RN ↑	removal_rising to CP	-0.0103	-0.0103	-0.0103
SN ↓	min_pulse_width to SN	0.0696	0.0793	0.1016
SN ↑	recovery_rising to CP	0.0048	0.0048	0.0048
SN ↑	removal_rising to CP	0.0308	0.0308	0.0308

TE ↓	hold_rising to CP	-0.0066	-0.0071	-0.0071
TE ↑	hold_rising to CP	-0.0240	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.0613	0.0608	0.0608
TE ↑	setup_rising to CP	0.1177	0.1177	0.1171
TI ↓	hold_rising to CP	-0.0570	-0.0570	-0.0530
TI ↑	hold_rising to CP	-0.0251	-0.0251	-0.0251
TI ↓	setup_rising to CP	0.1163	0.1163	0.1160
TI ↑	setup_rising to CP	0.0597	0.0597	0.0597

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	3.459e-04	1.000e-20
X17_P0	4.109e-04	1.000e-20
X33_P0	5.359e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

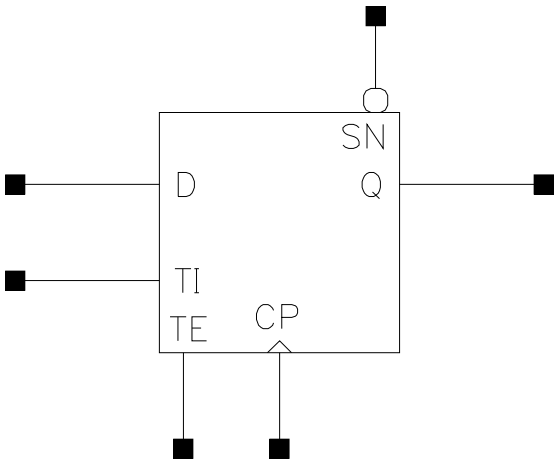
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	7.586e-03	7.587e-03	7.587e-03
Clock 100Mhz Data 25Mhz	7.661e-03	8.163e-03	9.576e-03
Clock 100Mhz Data 50Mhz	7.736e-03	8.740e-03	1.157e-02
Clock = 0 Data 100Mhz	3.613e-03	3.613e-03	3.615e-03
Clock = 1 Data 100Mhz	4.009e-05	4.017e-05	4.045e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004
SN	0.0013	0.0013	0.0013	0.0013
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0008			
D	0.0004			
SN	0.0013			
TE	0.0009			
TI	0.0004			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0707	0.0385	4.5569	2.0334
CP to Q ↑	0.0621	0.0516	6.2025	2.9422
SN to Q ↑	0.0471	0.0540	6.0452	2.9357
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
CP to Q ↓	0.0552	0.0577	0.9996	0.6891
CP to Q ↑	0.0722	0.0743	1.4504	0.9813
SN to Q ↑	0.0738	0.0760	1.4496	0.9821
	X33_P0		**X33_P0**	
CP to Q ↓	0.0600		0.5238	
CP to Q ↑	0.0760		0.7394	
SN to Q ↑	0.0776		0.7394	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.0998	0.0999	0.0999	0.0999
CP ↑	min_pulse_width to CP	0.0646	0.0283	0.0271	0.0271
D ↓	hold_rising to CP	-0.0528	-0.0143	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0262	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0949	0.0613	0.0613	0.0613
D ↑	setup_rising to CP	0.0558	0.0294	0.0294	0.0294
SN ↓	min_pulse_width to SN	0.0425	0.0522	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0081	0.0048	0.0048	0.0048
SN ↑	removal_rising to CP	0.0238	0.0309	0.0309	0.0309
TE ↓	hold_rising to CP	-0.0386	-0.0094	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0381	-0.0186	-0.0186	-0.0186
TE ↓	setup_rising to CP	0.0773	0.0589	0.0589	0.0589
TE ↑	setup_rising to CP	0.1513	0.1226	0.1226	0.1226
TI ↓	hold_rising to CP	-0.1133	-0.0634	-0.0634	-0.0634
TI ↑	hold_rising to CP	-0.0423	-0.0211	-0.0209	-0.0209
TI ↓	setup_rising to CP	0.1579	0.1176	0.1176	0.1176
TI ↑	setup_rising to CP	0.0713	0.0508	0.0508	0.0508
		X33_P0			

CP ↓	min_pulse_width to CP	0.0999			
CP ↑	min_pulse_width to CP	0.0271			
D ↓	hold_rising to CP	-0.0169			
D ↑	hold_rising to CP	0.0009			
D ↓	setup_rising to CP	0.0613			
D ↑	setup_rising to CP	0.0294			
SN ↓	min_pulse_width to SN	0.0474			
SN ↑	recovery_rising to CP	0.0048			
SN ↑	removal_rising to CP	0.0309			
TE ↓	hold_rising to CP	-0.0120			
TE ↑	hold_rising to CP	-0.0186			
TE ↓	setup_rising to CP	0.0589			
TE ↑	setup_rising to CP	0.1199			
TI ↓	hold_rising to CP	-0.0634			
TI ↑	hold_rising to CP	-0.0209			
TI ↓	setup_rising to CP	0.1176			
TI ↑	setup_rising to CP	0.0508			

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.542e-04	1.000e-20
X8_P0	3.010e-04	1.000e-20
X17_P0	4.232e-04	1.000e-20
X25_P0	4.732e-04	1.000e-20
X33_P0	5.230e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	6.992e-03	7.136e-03	7.185e-03	7.208e-03
Clock 100Mhz Data 25Mhz	7.225e-03	7.245e-03	7.799e-03	8.135e-03
Clock 100Mhz Data 50Mhz	7.458e-03	7.354e-03	8.413e-03	9.062e-03
Clock = 0 Data 100Mhz	4.113e-03	3.820e-03	3.724e-03	3.675e-03
Clock = 1 Data 100Mhz	1.070e-03	5.551e-04	3.835e-04	2.976e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	7.223e-03			

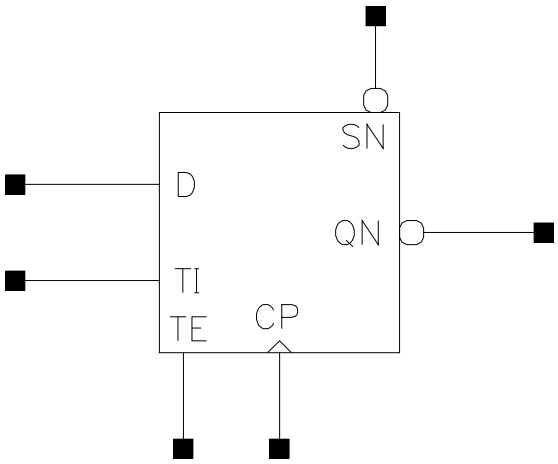
Clock 100Mhz Data 25Mhz	8.475e-03			
Clock 100Mhz Data 50Mhz	9.726e-03			
Clock = 0 Data 100Mhz	3.646e-03			
Clock = 1 Data 100Mhz	2.461e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004
SN	0.0012	0.0013	0.0013	0.0013
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0008			
D	0.0004			
SN	0.0013			
TE	0.0009			
TI	0.0004			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0691	0.0611	3.8543	1.9466
CP to QN ↑	0.0734	0.0447	5.9706	2.8800
SN to QN ↓	0.0553	0.0625	3.8417	1.9473
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
CP to QN ↓	0.0636	0.0669	1.0030	0.6915
CP to QN ↑	0.0521	0.0551	1.4498	0.9834
SN to QN ↓	0.0666	0.0700	1.0026	0.6915
	X33_P0		**X33_P0**	
CP to QN ↓	0.0694		0.5248	
CP to QN ↑	0.0572		0.7394	
SN to QN ↓	0.0724		0.5240	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.0998	0.0999	0.0999	0.0999
CP ↑	min_pulse_width to CP	0.0471	0.0271	0.0318	0.0318
D ↓	hold_rising to CP	-0.0528	-0.0169	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0262	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0949	0.0613	0.0613	0.0613
D ↑	setup_rising to CP	0.0558	0.0294	0.0294	0.0294
SN ↓	min_pulse_width to SN	0.0425	0.0474	0.0522	0.0522
SN ↑	recovery_rising to CP	0.0048	0.0048	0.0048	0.0048
SN ↑	removal_rising to CP	0.0238	0.0309	0.0309	0.0309
TE ↓	hold_rising to CP	-0.0386	-0.0120	-0.0094	-0.0094
TE ↑	hold_rising to CP	-0.0381	-0.0186	-0.0186	-0.0186
TE ↓	setup_rising to CP	0.0778	0.0589	0.0589	0.0589
TE ↑	setup_rising to CP	0.1513	0.1226	0.1226	0.1226
TI ↓	hold_rising to CP	-0.1133	-0.0634	-0.0634	-0.0634
TI ↑	hold_rising to CP	-0.0416	-0.0209	-0.0195	-0.0195
TI ↓	setup_rising to CP	0.1579	0.1176	0.1176	0.1176
TI ↑	setup_rising to CP	0.0713	0.0508	0.0508	0.0508
		X33_P0			

CP ↓	min_pulse_width to CP	0.0999			
CP ↑	min_pulse_width to CP	0.0318			
D ↓	hold_rising to CP	-0.0143			
D ↑	hold_rising to CP	0.0009			
D ↓	setup_rising to CP	0.0613			
D ↑	setup_rising to CP	0.0294			
SN ↓	min_pulse_width to SN	0.0522			
SN ↑	recovery_rising to CP	0.0048			
SN ↑	removal_rising to CP	0.0309			
TE ↓	hold_rising to CP	-0.0094			
TE ↑	hold_rising to CP	-0.0186			
TE ↓	setup_rising to CP	0.0589			
TE ↑	setup_rising to CP	0.1226			
TI ↓	hold_rising to CP	-0.0634			
TI ↑	hold_rising to CP	-0.0195			
TI ↓	setup_rising to CP	0.1176			
TI ↑	setup_rising to CP	0.0508			

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.544e-04	1.000e-20
X8_P0	3.111e-04	1.000e-20
X17_P0	4.365e-04	1.000e-20
X25_P0	5.010e-04	1.000e-20
X33_P0	5.657e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	6.991e-03	7.148e-03	7.192e-03	7.215e-03
Clock 100Mhz Data 25Mhz	7.021e-03	7.152e-03	7.892e-03	8.260e-03
Clock 100Mhz Data 50Mhz	7.050e-03	7.157e-03	8.592e-03	9.305e-03
Clock = 0 Data 100Mhz	4.114e-03	3.824e-03	3.726e-03	3.678e-03
Clock = 1 Data 100Mhz	1.069e-03	5.546e-04	3.833e-04	2.975e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	7.229e-03			

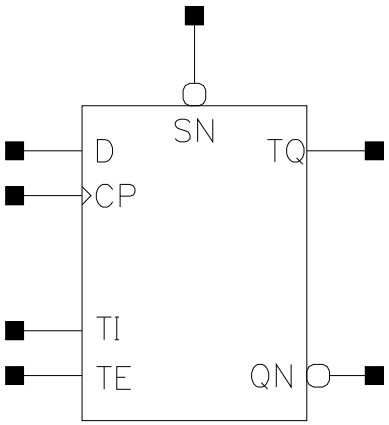
Clock 100Mhz Data 25Mhz	8.609e-03			
Clock 100Mhz Data 50Mhz	9.990e-03			
Clock = 0 Data 100Mhz	3.648e-03			
Clock = 1 Data 100Mhz	2.461e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.216	5.0592
X8_P0	1.200	4.080	4.8960
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004

SN	0.0014	0.0015	0.0014	0.0014
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0795	0.0640	3.8562	1.9585
CP to QN ↑	0.0940	0.0503	5.9075	2.9293
CP to TQ ↓	0.0677	0.0342	5.4904	4.7347
CP to TQ ↑	0.0619	0.0487	8.2261	8.0039
SN to QN ↓	0.0527	0.0493	3.8512	1.9598
SN to TQ ↑	0.0372	0.0352	8.0754	7.9775
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0634	0.0694	1.0286	0.5200
CP to QN ↑	0.0556	0.0612	1.4633	0.7446
CP to TQ ↓	0.0419	0.0418	4.8810	4.8769
CP to TQ ↑	0.0548	0.0548	8.0805	8.0966
SN to QN ↓	0.0555	0.0614	1.0272	0.5192
SN to TQ ↑	0.0467	0.0465	8.0669	8.0872

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0998	0.0999	0.0999	0.0999
CP ↑	min_pulse_width to CP	0.0645	0.0284	0.0331	0.0365
D ↓	hold_rising to CP	-0.0528	-0.0169	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0262	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0949	0.0613	0.0613	0.0613
D ↑	setup_rising to CP	0.0558	0.0294	0.0294	0.0294
SN ↓	min_pulse_width to SN	0.0354	0.0403	0.0403	0.0430
SN ↑	recovery_rising to CP	0.0048	0.0054	0.0054	0.0054
SN ↑	removal_rising to CP	0.0238	0.0309	0.0309	0.0309
TE ↓	hold_rising to CP	-0.0386	-0.0120	-0.0094	-0.0094
TE ↑	hold_rising to CP	-0.0381	-0.0186	-0.0186	-0.0186
TE ↓	setup_rising to CP	0.0773	0.0589	0.0589	0.0589
TE ↑	setup_rising to CP	0.1513	0.1226	0.1226	0.1226
TI ↓	hold_rising to CP	-0.1133	-0.0634	-0.0634	-0.0634
TI ↑	hold_rising to CP	-0.0416	-0.0211	-0.0195	-0.0195
TI ↓	setup_rising to CP	0.1579	0.1176	0.1176	0.1176
TI ↑	setup_rising to CP	0.0728	0.0508	0.0508	0.0508

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.894e-04	1.000e-20
X8_P0	3.454e-04	1.000e-20
X17_P0	4.708e-04	1.000e-20
X33_P0	6.000e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

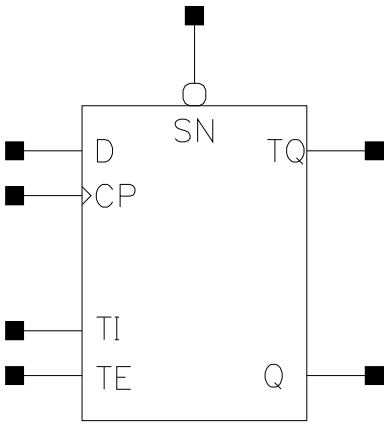
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	6.999e-03	7.145e-03	7.194e-03	7.219e-03
Clock 100Mhz Data 25Mhz	7.394e-03	7.364e-03	8.061e-03	8.785e-03
Clock 100Mhz Data 50Mhz	7.788e-03	7.583e-03	8.927e-03	1.035e-02
Clock = 0 Data 100Mhz	4.124e-03	3.830e-03	3.733e-03	3.684e-03
Clock = 1 Data 100Mhz	1.070e-03	5.551e-04	3.835e-04	2.977e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.944	4.7328
X17_P0	1.200	4.216	5.0592
X33_P0	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004

SN	0.0014	0.0013	0.0013	0.0013
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0802	0.0414	4.6514	2.0659
CP to Q ↑	0.0660	0.0534	6.2276	2.9753
CP to TQ ↓	0.0796	0.0419	6.9577	5.4062
CP to TQ ↑	0.0648	0.0595	8.2839	11.5260
SN to Q ↑	0.0396	0.0564	6.0449	2.9715
SN to TQ ↑	0.0387	0.0635	8.1001	11.4923
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0561	0.0614	1.0226	0.5314
CP to Q ↑	0.0729	0.0771	1.4581	0.7420
CP to TQ ↓	0.0579	0.0642	5.1949	5.2625
CP to TQ ↑	0.0779	0.0846	11.1998	11.2478
SN to Q ↑	0.0744	0.0786	1.4552	0.7413
SN to TQ ↑	0.0794	0.0861	11.2027	11.2484

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0998	0.0999	0.0999	0.0999
CP ↑	min_pulse_width to CP	0.0740	0.0318	0.0271	0.0271
D ↓	hold_rising to CP	-0.0528	-0.0110	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0262	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0949	0.0613	0.0613	0.0613
D ↑	setup_rising to CP	0.0558	0.0294	0.0294	0.0294
SN ↓	min_pulse_width to SN	0.0354	0.0571	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0080	0.0048	0.0048	0.0048
SN ↑	removal_rising to CP	0.0238	0.0309	0.0309	0.0309
TE ↓	hold_rising to CP	-0.0386	-0.0094	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0381	-0.0186	-0.0186	-0.0186
TE ↓	setup_rising to CP	0.0773	0.0589	0.0589	0.0589
TE ↑	setup_rising to CP	0.1513	0.1226	0.1226	0.1226
TI ↓	hold_rising to CP	-0.1133	-0.0634	-0.0634	-0.0634
TI ↑	hold_rising to CP	-0.0416	-0.0195	-0.0209	-0.0209
TI ↓	setup_rising to CP	0.1579	0.1176	0.1176	0.1176
TI ↑	setup_rising to CP	0.0728	0.0508	0.0508	0.0508

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	2.827e-04	1.000e-20
X8_P0	3.132e-04	1.000e-20
X17_P0	4.343e-04	1.000e-20
X33_P0	5.340e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

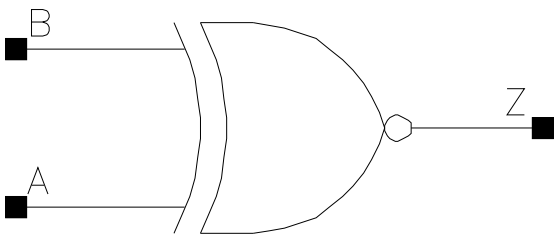
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	6.992e-03	7.137e-03	7.185e-03	7.209e-03
Clock 100Mhz Data 25Mhz	7.499e-03	7.428e-03	7.939e-03	8.691e-03
Clock 100Mhz Data 50Mhz	8.006e-03	7.719e-03	8.692e-03	1.017e-02
Clock = 0 Data 100Mhz	4.123e-03	3.826e-03	3.728e-03	3.679e-03
Clock = 1 Data 100Mhz	1.070e-03	5.549e-04	3.834e-04	2.976e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P0	X8_P0	X17_P0	X25_P0
A	0.0014	0.0006	0.0008	0.0013
B	0.0014	0.0013	0.0017	0.0022
	X33_P0			
A	0.0015			
B	0.0026			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X8_P0**	**X6_P0**	**X8_P0**
A to Z ↓	0.0184	0.0415	3.6502	2.1085
A to Z ↑	0.0192	0.0385	4.4908	3.0473
B to Z ↓	0.0175	0.0282	3.6483	2.0917
B to Z ↑	0.0199	0.0271	4.4927	3.0363
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
A to Z ↓	0.0389	0.0391	1.0345	0.7096
A to Z ↑	0.0350	0.0349	1.4869	0.9913

B to Z ↓	0.0288	0.0278	1.0308	0.7076
B to Z ↑	0.0269	0.0258	1.4829	0.9884
	X33_P0		**X33_P0**	
A to Z ↓	0.0370		0.5330	
A to Z ↑	0.0339		0.7454	
B to Z ↓	0.0267		0.5318	
B to Z ↑	0.0256		0.7440	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P0	1.764e-04	1.000e-20
X8_P0	1.986e-04	1.000e-20
X17_P0	3.508e-04	1.000e-20
X25_P0	5.385e-04	1.000e-20
X33_P0	7.585e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	2.264e-03	4.314e-03	6.445e-03	1.004e-02
B to Z	2.236e-03	3.084e-03	5.087e-03	7.752e-03
	X33_P0			
A to Z	1.242e-02			
B to Z	9.957e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

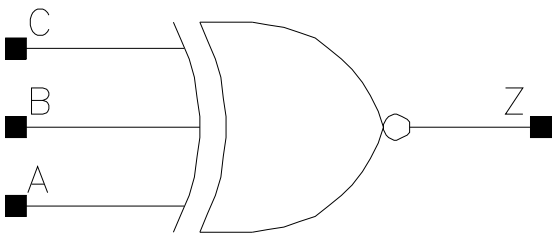
Pin Cycle (vdds)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	2.176	2.6112
X16_P0	1.200	2.720	3.2640
X25_P0	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X16_P0	X25_P0
A	0.0024	0.0021	0.0026	0.0038
B	0.0028	0.0019	0.0026	0.0035
C	0.0017	0.0006	0.0006	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0288	0.0480	4.3044	2.2080
A to Z ↑	0.0272	0.0447	6.3898	3.0176
B to Z ↓	0.0297	0.0483	4.3060	2.2100
B to Z ↑	0.0276	0.0452	6.3908	3.0173
C to Z ↓	0.0291	0.0638	4.3103	2.2090
C to Z ↑	0.0267	0.0602	6.3899	3.0178
	X16_P0	**X25_P0**	**X16_P0**	**X25_P0**
A to Z ↓	0.0479	0.0482	1.1359	0.7245
A to Z ↑	0.0481	0.0477	1.5809	0.9944
B to Z ↓	0.0484	0.0494	1.1370	0.7249

B to Z ↑	0.0486	0.0491	1.5804	0.9946
C to Z ↓	0.0670	0.0715	1.1366	0.7248
C to Z ↑	0.0662	0.0707	1.5812	0.9946

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	1.718e-04	1.000e-20
X8_P0	1.753e-04	1.000e-20
X16_P0	3.102e-04	1.000e-20
X25_P0	4.460e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	2.293e-03	3.319e-03	5.603e-03	8.590e-03
B to Z	2.349e-03	3.310e-03	5.626e-03	8.684e-03
C to Z	2.335e-03	4.890e-03	7.474e-03	1.140e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

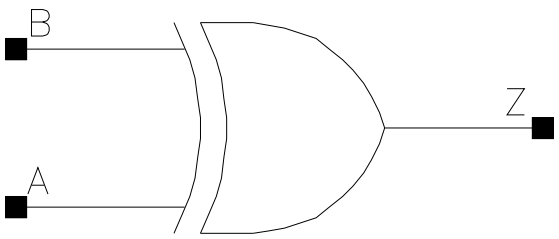
Pin Cycle (vdds)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.224	1.4688
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.224	1.4688
X16_P0	1.200	1.360	1.6320
X25_P0	1.200	2.176	2.6112
X31_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X16_P0
A	0.0007	0.0013	0.0009	0.0010
B	0.0011	0.0013	0.0013	0.0015
	X25_P0	X31_P0		
A	0.0013	0.0017		
B	0.0023	0.0030		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0369	0.0180	3.9086	2.8242
A to Z ↑	0.0359	0.0199	5.8400	5.7160
B to Z ↓	0.0265	0.0187	3.8878	2.8356
B to Z ↑	0.0269	0.0188	5.8299	5.7121
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0328	0.0342	2.0641	1.0653

A to Z ↑	0.0305	0.0321	2.9687	1.4937
B to Z ↓	0.0254	0.0261	2.0572	1.0614
B to Z ↑	0.0243	0.0256	2.9644	1.4927
	X25_P0	**X31_P0**	**X25_P0**	**X31_P0**
A to Z ↓	0.0365	0.0341	0.7039	0.5660
A to Z ↑	0.0339	0.0319	0.9878	0.7984
B to Z ↓	0.0269	0.0251	0.7033	0.5654
B to Z ↑	0.0253	0.0239	0.9881	0.7969

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	1.578e-04	1.000e-20
X6_P0	1.681e-04	1.000e-20
X8_P0	2.606e-04	1.000e-20
X16_P0	4.072e-04	1.000e-20
X25_P0	5.352e-04	1.000e-20
X31_P0	7.608e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	3.126e-03	2.221e-03	3.896e-03	5.916e-03
B to Z	2.490e-03	2.168e-03	3.336e-03	5.090e-03
	X25_P0	X31_P0		
A to Z	9.370e-03	1.148e-02		
B to Z	7.242e-03	8.919e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

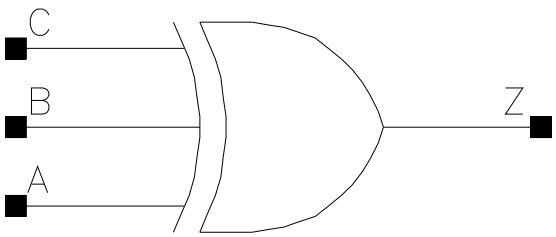
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P0	X31_P0		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X24_P0	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X24_P0
A	0.0020	0.0021	0.0026	0.0046
B	0.0021	0.0019	0.0024	0.0038
C	0.0007	0.0014	0.0020	0.0030

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0292	0.0480	4.5003	2.2076
A to Z ↑	0.0277	0.0447	6.9818	3.0146
B to Z ↓	0.0299	0.0483	4.5033	2.2089
B to Z ↑	0.0282	0.0452	6.9827	3.0158
C to Z ↓	0.0507	0.0471	4.4804	2.2105
C to Z ↑	0.0494	0.0438	6.9578	3.0162
	X17_P0	**X24_P0**	**X17_P0**	**X24_P0**
A to Z ↓	0.0435	0.0509	1.0573	0.7616
A to Z ↑	0.0438	0.0388	1.4677	0.9969
B to Z ↓	0.0437	0.0512	1.0577	0.7614

B to Z ↑	0.0442	0.0391	1.4692	0.9974
C to Z ↓	0.0431	0.0497	1.0580	0.7615
C to Z ↑	0.0435	0.0386	1.4689	0.9973

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	1.878e-04	1.000e-20
X8_P0	1.483e-04	1.000e-20
X17_P0	2.969e-04	1.000e-20
X24_P0	4.627e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	2.186e-03	3.318e-03	5.369e-03	9.037e-03
B to Z	2.232e-03	3.310e-03	5.383e-03	9.054e-03
C to Z	4.338e-03	3.271e-03	5.393e-03	9.067e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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