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C28SOI_SC_12_COREPBP16_LR Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 16 nm

Overview

- C28SOI_SC_12_COREPBP16_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

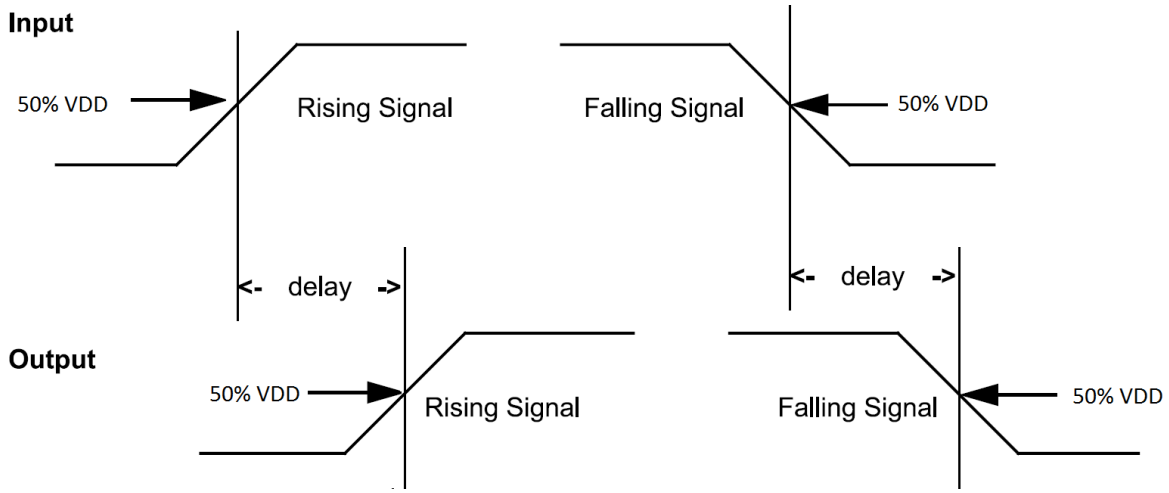


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

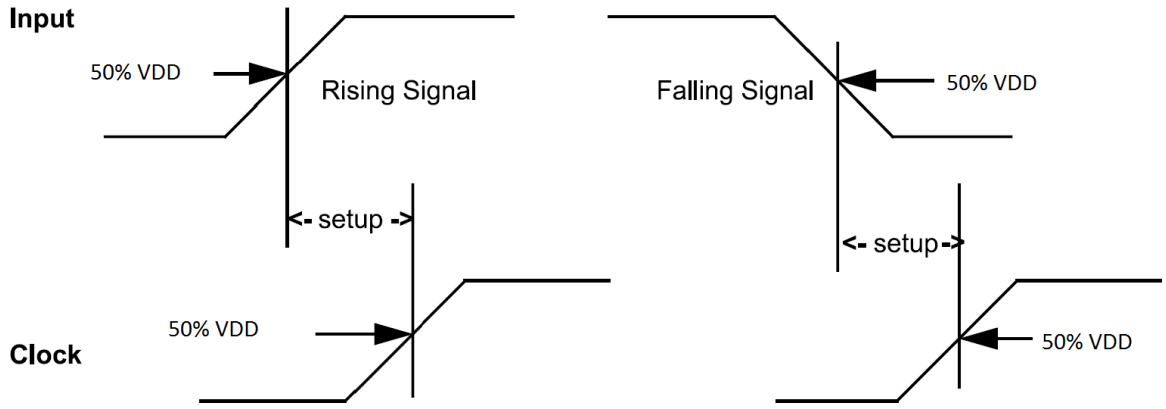


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

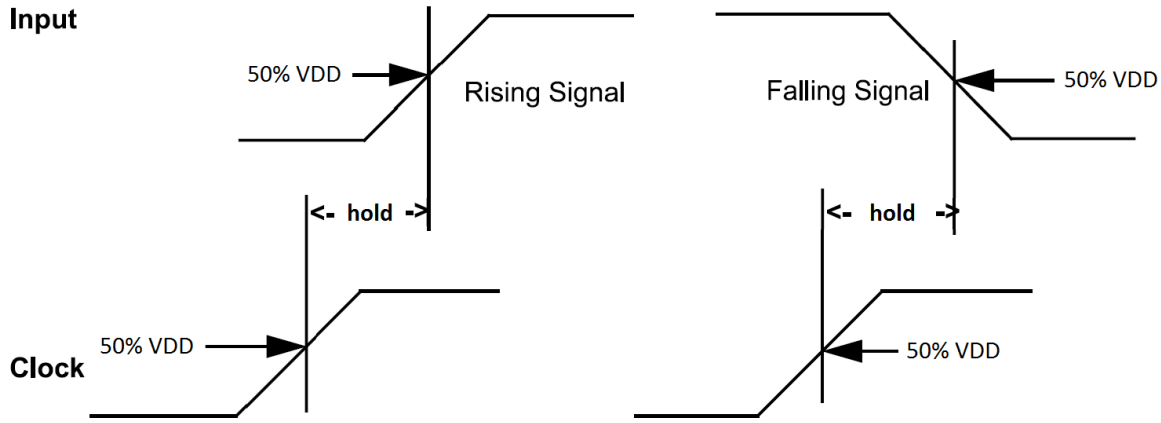


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

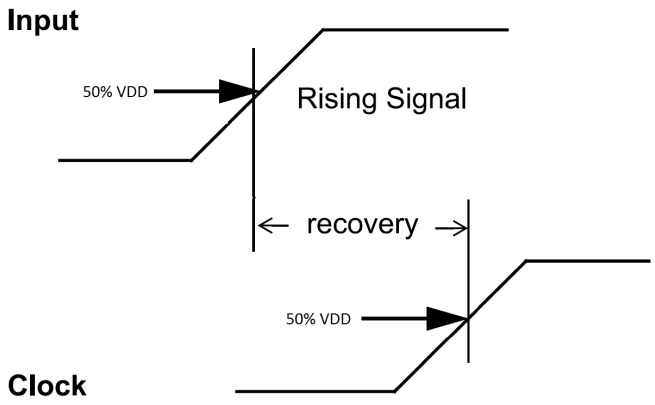


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

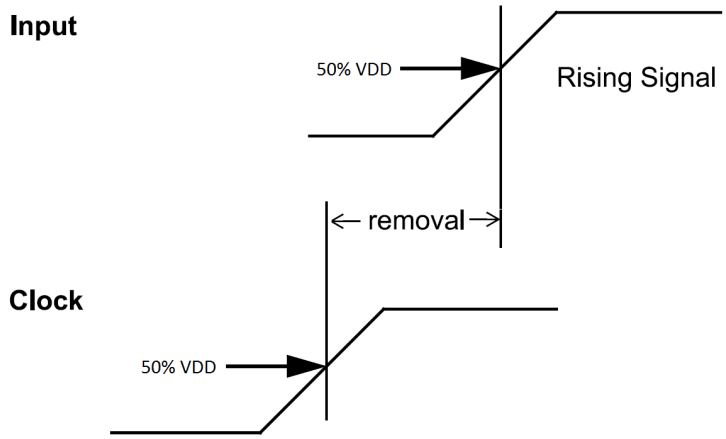


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

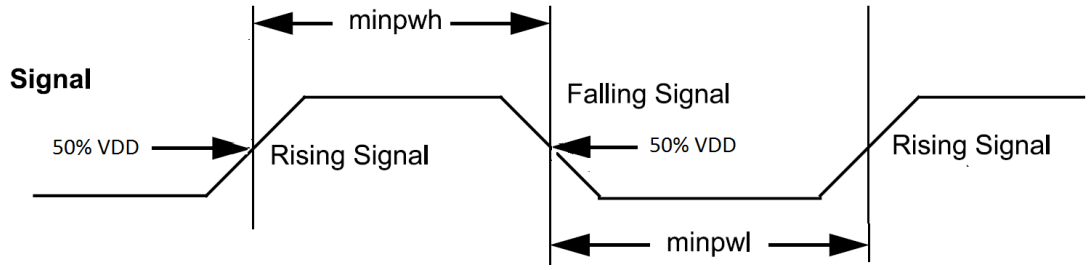


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

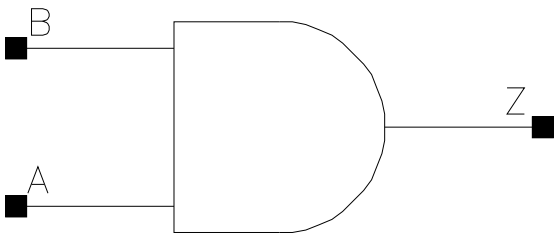
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X25_P16	1.200	1.088	1.3056
X33_P16	1.200	1.360	1.6320
X42_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0008	0.0011	0.0016	0.0020
B	0.0006	0.0010	0.0016	0.0021
	X42_P16			
A	0.0020			
B	0.0020			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0552	0.0442	3.0211	1.5385
A to Z ↑	0.0448	0.0396	5.6688	2.7666
B to Z ↓	0.0527	0.0418	3.0226	1.5368
B to Z ↑	0.0460	0.0407	5.6691	2.7672
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0459	0.0441	1.0198	0.7550

A to Z ↑	0.0397	0.0402	1.8196	1.3700
B to Z ↓	0.0436	0.0408	1.0182	0.7540
B to Z ↑	0.0408	0.0399	1.8211	1.3709
	X42_P16		**X42_P16**	
A to Z ↓	0.0473		0.6141	
A to Z ↑	0.0433		1.0984	
B to Z ↓	0.0440		0.6134	
B to Z ↑	0.0432		1.0977	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	3.303e-07	8.218e-10
X16_P16	6.022e-07	9.409e-10
X25_P16	8.773e-07	1.298e-09
X33_P16	1.216e-06	1.536e-09
X42_P16	1.360e-06	1.655e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	1.002e-05	1.983e-05	3.027e-05	6.795e-05
B (output stable)	2.983e-05	5.710e-05	8.828e-05	3.331e-04
A to Z	1.921e-03	3.071e-03	4.792e-03	6.303e-03
B to Z	1.806e-03	2.862e-03	4.471e-03	5.616e-03
	X42_P16			
A (output stable)	6.891e-05			
B (output stable)	3.297e-04			
A to Z	7.445e-03			
B to Z	6.766e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

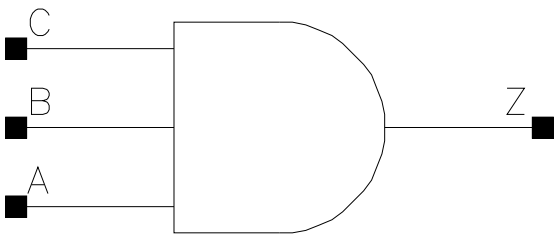
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	3.886e-08	-1.859e-08	-8.320e-08	-1.351e-07
B (output stable)	1.870e-08	-4.100e-08	-6.680e-08	-1.500e-07
A to Z	-3.414e-07	-2.334e-07	-5.785e-07	-1.108e-06
B to Z	-1.016e-07	-3.107e-07	-4.528e-07	-4.204e-07
	X42_P16			
A (output stable)	-1.300e-07			
B (output stable)	-1.703e-07			
A to Z	-1.548e-06			
B to Z	-8.004e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X25_P16	1.200	1.360	1.6320
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0007	0.0011	0.0017	0.0021
B	0.0006	0.0010	0.0015	0.0020
C	0.0006	0.0010	0.0014	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0595	0.0487	3.0637	1.4993
A to Z ↑	0.0605	0.0535	5.7197	2.7344
B to Z ↓	0.0577	0.0465	3.0609	1.4968
B to Z ↑	0.0597	0.0531	5.7208	2.7358
C to Z ↓	0.0555	0.0444	3.0611	1.4955
C to Z ↑	0.0605	0.0528	5.7245	2.7368
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0492	0.0463	1.0292	0.7704

A to Z ↑	0.0537	0.0504	1.8570	1.3911
B to Z ↓	0.0473	0.0442	1.0290	0.7689
B to Z ↑	0.0533	0.0501	1.8605	1.3937
C to Z ↓	0.0449	0.0421	1.0273	0.7686
C to Z ↑	0.0530	0.0499	1.8605	1.3937

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	2.576e-07	9.409e-10
X17_P16	4.940e-07	1.060e-09
X25_P16	7.073e-07	1.536e-09
X33_P16	9.388e-07	1.655e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	9.137e-06	1.841e-05	2.462e-05	3.385e-05
B (output stable)	3.037e-05	6.197e-05	8.675e-05	1.195e-04
C (output stable)	6.206e-05	1.166e-04	1.738e-04	2.362e-04
A to Z	2.103e-03	3.602e-03	5.265e-03	6.671e-03
B to Z	1.986e-03	3.393e-03	4.953e-03	6.251e-03
C to Z	1.899e-03	3.187e-03	4.640e-03	5.829e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

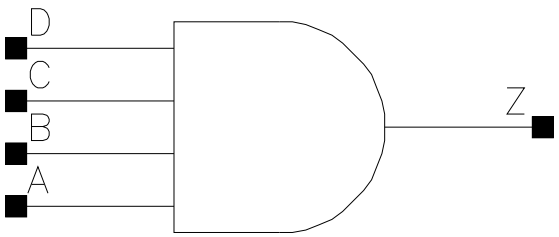
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	4.496e-08	-6.827e-09	-5.107e-08	-1.193e-07
B (output stable)	4.160e-08	-1.520e-08	-5.437e-08	-1.122e-07
C (output stable)	1.940e-08	-2.907e-08	-7.693e-08	-1.454e-07
A to Z	-3.617e-07	-8.502e-07	-6.606e-07	-1.348e-06
B to Z	-1.290e-07	-2.672e-07	-5.133e-07	-8.307e-07
C to Z	-8.081e-08	-3.204e-07	-3.473e-07	-6.980e-07

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X6_P16	1.200	1.088	1.3056
X20_P16	1.200	2.312	2.7744
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P16	X6_P16	X20_P16	X27_P16
A	0.0005	0.0008	0.0018	0.0020
B	0.0005	0.0007	0.0018	0.0020
C	0.0005	0.0008	0.0017	0.0020
D	0.0005	0.0007	0.0018	0.0020

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X6_P16	X4_P16	X6_P16
A to Z ↓	0.0657	0.0532	5.8408	3.7413
A to Z ↑	0.0671	0.0486	22.7298	11.8609
B to Z ↓	0.0642	0.0502	5.8441	3.7395
B to Z ↑	0.0684	0.0493	22.7582	11.8744
C to Z ↓	0.0683	0.0569	5.8397	3.7688
C to Z ↑	0.0652	0.0464	22.7704	11.8926

D to Z ↓	0.0665	0.0530	5.8398	3.7631
D to Z ↑	0.0678	0.0472	22.7887	11.8967
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0504	0.0471	1.0839	0.7653
A to Z ↑	0.0487	0.0542	3.9283	2.9687
B to Z ↓	0.0463	0.0438	1.0820	0.7639
B to Z ↑	0.0483	0.0542	3.9285	2.9680
C to Z ↓	0.0493	0.0454	1.0952	0.7712
C to Z ↑	0.0419	0.0452	3.9306	2.9694
D to Z ↓	0.0449	0.0421	1.0925	0.7687
D to Z ↑	0.0414	0.0451	3.9316	2.9701

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	2.332e-07	1.298e-09
X6_P16	5.061e-07	1.298e-09
X20_P16	1.380e-06	2.370e-09
X27_P16	1.542e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	3.558e-04	5.451e-04	1.591e-03	1.971e-03
B (output stable)	3.329e-04	4.946e-04	1.470e-03	1.836e-03
C (output stable)	3.398e-04	5.521e-04	1.391e-03	1.708e-03
D (output stable)	3.202e-04	4.932e-04	1.207e-03	1.486e-03
A to Z	1.438e-03	2.216e-03	6.613e-03	8.577e-03
B to Z	1.367e-03	2.066e-03	6.008e-03	7.944e-03
C to Z	1.389e-03	2.202e-03	5.512e-03	6.820e-03
D to Z	1.324e-03	2.044e-03	4.881e-03	6.177e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

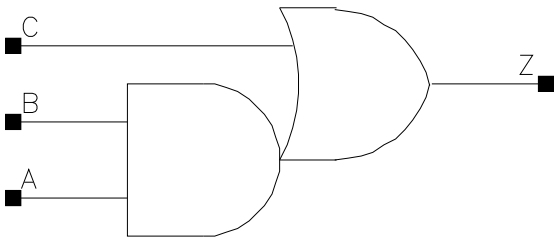
Pin Cycle (vdds)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	-8.100e-07	-1.192e-06	-7.398e-06	-1.411e-05
B (output stable)	-7.854e-07	-1.161e-06	-7.201e-06	-1.460e-05
C (output stable)	4.477e-06	7.958e-06	2.819e-05	4.758e-05
D (output stable)	2.636e-06	5.344e-06	1.248e-05	2.006e-05
A to Z	-8.495e-07	-1.314e-06	-6.735e-06	-1.142e-05
B to Z	-7.284e-07	-1.206e-06	-6.403e-06	-1.106e-05
C to Z	-1.054e-07	-2.019e-07	-1.058e-06	-1.280e-06
D to Z	-1.664e-07	-2.405e-07	-9.109e-07	-1.092e-06

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0006	0.0009	0.0020
B	0.0006	0.0010	0.0018
C	0.0007	0.0011	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0744	0.0646	3.1442	1.5394
A to Z ↑	0.0464	0.0398	5.5556	2.7105
B to Z ↓	0.0693	0.0600	3.1369	1.5346
B to Z ↑	0.0480	0.0416	5.5536	2.7098
C to Z ↓	0.0753	0.0660	3.1264	1.5306
C to Z ↑	0.0393	0.0359	5.5196	2.6974
	X33_P16		**X33_P16**	
A to Z ↓	0.0647		0.7787	
A to Z ↑	0.0406		1.3656	

B to Z ↓	0.0595		0.7777	
B to Z ↑	0.0411		1.3632	
C to Z ↓	0.0653		0.7754	
C to Z ↑	0.0351		1.3581	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	4.751e-07	9.409e-10
X17_P16	8.794e-07	1.060e-09
X33_P16	1.773e-06	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	4.783e-06	9.357e-06	2.558e-05
B (output stable)	1.798e-05	2.864e-05	1.066e-04
C (output stable)	5.436e-05	9.325e-05	2.136e-04
A to Z	1.929e-03	3.234e-03	6.419e-03
B to Z	1.821e-03	3.028e-03	5.870e-03
C to Z	2.175e-03	3.677e-03	7.230e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

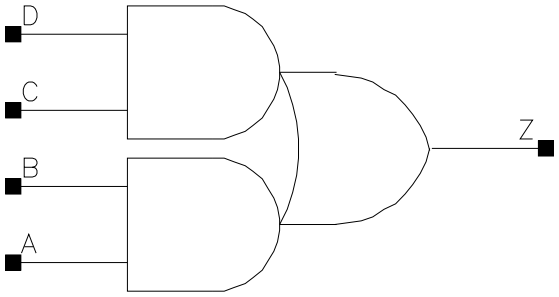
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	1.966e-06	5.617e-06	7.888e-06
B (output stable)	1.215e-05	2.098e-05	3.925e-05
C (output stable)	-6.650e-06	-9.269e-06	-1.808e-05
A to Z	-2.489e-07	-4.117e-07	-3.230e-07
B to Z	-7.870e-08	-2.545e-07	-7.245e-07
C to Z	-4.994e-06	-5.636e-06	-1.185e-05

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0006	0.0009	0.0019
B	0.0007	0.0010	0.0018
C	0.0006	0.0009	0.0019
D	0.0006	0.0010	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0877	0.0741	3.0181	1.5154
A to Z ↑	0.0578	0.0501	5.4655	2.7161
B to Z ↓	0.0821	0.0692	3.0048	1.5105
B to Z ↑	0.0581	0.0509	5.4618	2.7167

C to Z ↓	0.0762	0.0655	3.0044	1.5095
C to Z ↑	0.0500	0.0433	5.4500	2.7095
D to Z ↓	0.0730	0.0622	2.9959	1.5075
D to Z ↑	0.0523	0.0451	5.4530	2.7084
	X33_P16		**X33_P16**	
A to Z ↓	0.0708		0.7787	
A to Z ↑	0.0463		1.3711	
B to Z ↓	0.0671		0.7780	
B to Z ↑	0.0480		1.3710	
C to Z ↓	0.0623		0.7770	
C to Z ↑	0.0408		1.3659	
D to Z ↓	0.0586		0.7762	
D to Z ↑	0.0421		1.3661	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	4.962e-07	1.179e-09
X17_P16	9.350e-07	1.298e-09
X33_P16	1.695e-06	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.688e-05	3.834e-05	6.486e-05
B (output stable)	1.014e-04	1.510e-04	1.056e-04
C (output stable)	8.737e-06	1.704e-05	3.112e-05
D (output stable)	2.027e-05	3.917e-05	7.902e-05
A to Z	2.578e-03	4.226e-03	7.916e-03
B to Z	2.383e-03	3.919e-03	7.475e-03
C to Z	2.140e-03	3.519e-03	6.492e-03
D to Z	2.048e-03	3.329e-03	6.075e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

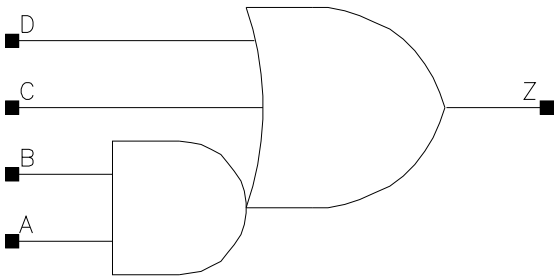
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-5.512e-07	-1.253e-06	-3.592e-06
B (output stable)	-1.687e-06	-1.298e-06	-3.626e-06
C (output stable)	1.048e-06	4.016e-06	8.357e-06
D (output stable)	1.347e-06	4.154e-06	7.782e-06
A to Z	-2.566e-06	-3.285e-06	-1.064e-05
B to Z	-2.821e-06	-3.534e-06	-1.068e-05
C to Z	-2.182e-07	-2.883e-07	-4.410e-07
D to Z	-2.056e-07	-3.343e-07	-7.335e-07

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	0.952	1.1424
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0006	0.0009	0.0017
B	0.0006	0.0009	0.0018
C	0.0007	0.0009	0.0018
D	0.0006	0.0010	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.1025	0.0859	3.3486	1.6377
A to Z ↑	0.0498	0.0428	5.5377	2.7887
B to Z ↓	0.0980	0.0799	3.3440	1.6331
B to Z ↑	0.0519	0.0440	5.5434	2.7904
C to Z ↓	0.1125	0.0948	3.3369	1.6323
C to Z ↑	0.0421	0.0379	5.5080	2.7759

D to Z ↓	0.1089	0.0930	3.3347	1.6321
D to Z ↑	0.0419	0.0377	5.5033	2.7739
	X33_P16		**X33_P16**	
A to Z ↓	0.0867		0.8188	
A to Z ↑	0.0427		1.3669	
B to Z ↓	0.0772		0.8143	
B to Z ↑	0.0427		1.3669	
C to Z ↓	0.0960		0.8149	
C to Z ↑	0.0370		1.3599	
D to Z ↓	0.0921		0.8151	
D to Z ↑	0.0360		1.3568	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	4.925e-07	1.060e-09
X17_P16	9.338e-07	1.179e-09
X33_P16	1.926e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.330e-06	4.715e-06	1.457e-05
B (output stable)	6.485e-06	1.224e-05	6.194e-05
C (output stable)	9.272e-05	1.647e-04	4.754e-04
D (output stable)	8.054e-06	1.298e-05	3.030e-05
A to Z	2.097e-03	3.422e-03	6.846e-03
B to Z	2.010e-03	3.211e-03	6.176e-03
C to Z	2.476e-03	4.107e-03	8.315e-03
D to Z	2.320e-03	3.843e-03	7.567e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

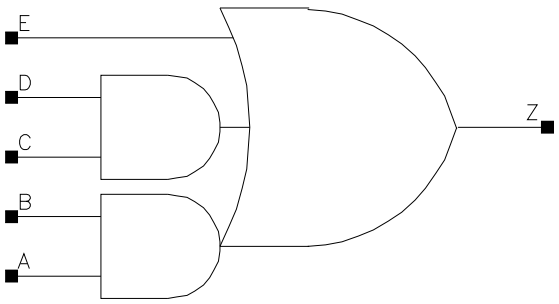
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	1.610e-06	3.961e-06	5.991e-06
B (output stable)	5.671e-06	1.158e-05	1.986e-05
C (output stable)	-1.662e-05	-2.795e-05	-7.789e-05
D (output stable)	4.126e-06	9.890e-06	2.705e-05
A to Z	-2.181e-07	-6.677e-07	-1.217e-06
B to Z	-1.187e-07	-3.234e-07	-6.746e-07
C to Z	-6.388e-06	-9.286e-06	-2.292e-05
D to Z	-4.322e-06	-5.797e-06	-1.109e-05

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.088	1.3056
X17_P16	1.200	1.224	1.4688
X33_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0006	0.0009	0.0019
B	0.0006	0.0009	0.0017
C	0.0007	0.0011	0.0019
D	0.0006	0.0009	0.0018
E	0.0006	0.0010	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.1302	0.1068	3.1955	1.5819
A to Z ↑	0.0605	0.0502	5.4423	2.7307

B to Z ↓	0.1258	0.1018	3.1833	1.5782
B to Z ↑	0.0632	0.0522	5.4412	2.7293
C to Z ↓	0.1064	0.0885	3.1760	1.5746
C to Z ↑	0.0526	0.0433	5.3899	2.7140
D to Z ↓	0.0990	0.0806	3.1594	1.5668
D to Z ↑	0.0543	0.0446	5.3923	2.7128
E to Z ↓	0.1132	0.0928	3.1535	1.5664
E to Z ↑	0.0441	0.0375	5.3522	2.6956
	X33_P16		**X33_P16**	
A to Z ↓	0.1048		0.8173	
A to Z ↑	0.0517		1.3772	
B to Z ↓	0.0980		0.8151	
B to Z ↑	0.0528		1.3771	
C to Z ↓	0.0853		0.8133	
C to Z ↑	0.0434		1.3661	
D to Z ↓	0.0778		0.8098	
D to Z ↑	0.0443		1.3658	
E to Z ↓	0.0899		0.8097	
E to Z ↑	0.0373		1.3572	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	5.798e-07	1.298e-09
X17_P16	1.081e-06	1.417e-09
X33_P16	1.959e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.007e-05	3.468e-05	7.927e-05
B (output stable)	4.714e-05	5.595e-05	1.451e-04
C (output stable)	1.006e-05	1.339e-05	3.567e-05
D (output stable)	1.054e-05	2.135e-05	6.311e-05
E (output stable)	7.440e-05	8.401e-05	2.194e-04
A to Z	2.938e-03	4.626e-03	9.091e-03
B to Z	2.861e-03	4.424e-03	8.525e-03
C to Z	2.264e-03	3.576e-03	6.931e-03
D to Z	2.152e-03	3.342e-03	6.386e-03
E to Z	2.540e-03	3.986e-03	7.687e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-2.667e-06	-4.562e-06	-1.001e-05
B (output stable)	-6.926e-06	-7.577e-06	-1.699e-05
C (output stable)	5.491e-06	1.012e-05	2.151e-05
D (output stable)	3.430e-06	1.110e-05	1.845e-05
E (output stable)	-7.249e-07	3.809e-06	-7.237e-07
A to Z	-7.921e-06	-9.133e-06	-1.913e-05
B to Z	-8.259e-06	-9.163e-06	-1.956e-05
C to Z	-2.782e-07	-6.221e-07	-7.860e-07
D to Z	-2.312e-07	-3.364e-07	-7.442e-07

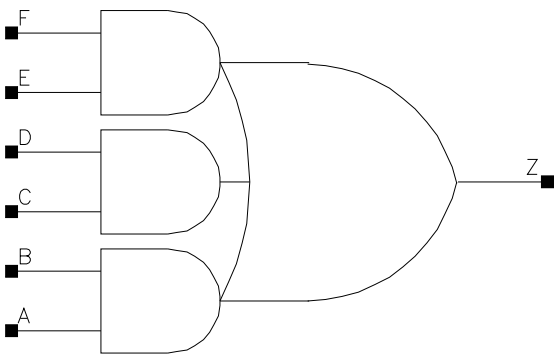
E to Z	-4.566e-06	-5.214e-06	-1.140e-05

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.360	1.6320
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
A	0.0006	0.0007	0.0009	0.0019

B	0.0006	0.0007	0.0012	0.0017
C	0.0006	0.0007	0.0009	0.0018
D	0.0006	0.0007	0.0009	0.0017
E	0.0006	0.0007	0.0009	0.0019
F	0.0006	0.0007	0.0009	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.1300	0.1202	6.1941	3.1483
A to Z ↑	0.0642	0.0601	11.1815	5.5159
B to Z ↓	0.1198	0.1117	6.1567	3.1327
B to Z ↑	0.0638	0.0604	11.1781	5.5127
C to Z ↓	0.1170	0.1092	6.1726	3.1378
C to Z ↑	0.0588	0.0550	11.1126	5.4809
D to Z ↓	0.1119	0.1044	6.1496	3.1269
D to Z ↑	0.0611	0.0574	11.1167	5.4804
E to Z ↓	0.0942	0.0899	6.1321	3.1214
E to Z ↑	0.0509	0.0479	11.0525	5.4551
F to Z ↓	0.0878	0.0838	6.1102	3.1101
F to Z ↑	0.0524	0.0494	11.0545	5.4533
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
A to Z ↓	0.1138	0.1086	1.5873	0.8171
A to Z ↑	0.0546	0.0553	2.7379	1.3822
B to Z ↓	0.1074	0.1023	1.5770	0.8151
B to Z ↑	0.0563	0.0564	2.7384	1.3826
C to Z ↓	0.1043	0.1006	1.5815	0.8160
C to Z ↑	0.0502	0.0518	2.7244	1.3736
D to Z ↓	0.0988	0.0945	1.5754	0.8136
D to Z ↑	0.0522	0.0530	2.7241	1.3740
E to Z ↓	0.0856	0.0868	1.5735	0.8125
E to Z ↑	0.0433	0.0457	2.7137	1.3690
F to Z ↓	0.0799	0.0801	1.5681	0.8095
F to Z ↑	0.0450	0.0470	2.7132	1.3698

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	4.493e-07	1.536e-09
X8_P16	6.807e-07	1.536e-09
X17_P16	1.133e-06	1.655e-09
X33_P16	1.992e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	5.220e-05	6.403e-05	8.296e-05	1.706e-04
B (output stable)	1.815e-04	2.104e-04	2.459e-04	4.202e-04
C (output stable)	2.707e-05	3.288e-05	4.272e-05	7.077e-05
D (output stable)	3.655e-05	4.587e-05	5.966e-05	1.394e-04
E (output stable)	2.296e-05	2.555e-05	3.134e-05	4.555e-05
F (output stable)	2.528e-05	3.026e-05	4.228e-05	9.908e-05

A to Z	2.760e-03	3.555e-03	5.205e-03	9.908e-03
B to Z	2.549e-03	3.312e-03	4.895e-03	9.350e-03
C to Z	2.322e-03	3.036e-03	4.512e-03	8.615e-03
D to Z	2.231e-03	2.917e-03	4.314e-03	8.103e-03
E to Z	1.840e-03	2.498e-03	3.720e-03	7.372e-03
F to Z	1.734e-03	2.356e-03	3.510e-03	6.869e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

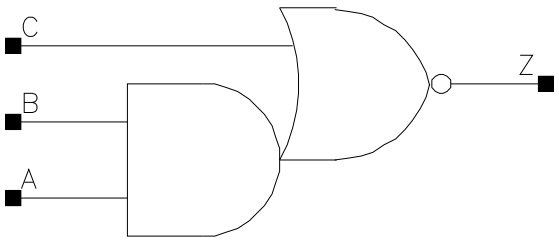
Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	-6.261e-06	-7.669e-06	-1.021e-05	-2.134e-05
B (output stable)	-1.742e-05	-2.023e-05	-2.440e-05	-5.247e-05
C (output stable)	-2.196e-06	-2.289e-06	-1.660e-06	1.431e-06
D (output stable)	-9.432e-07	-5.699e-07	2.572e-07	1.104e-05
E (output stable)	1.347e-05	1.714e-05	2.533e-05	4.517e-05
F (output stable)	1.036e-05	1.355e-05	2.046e-05	3.977e-05
A to Z	-9.797e-06	-1.113e-05	-1.302e-05	-2.400e-05
B to Z	-1.003e-05	-1.123e-05	-1.330e-05	-2.487e-05
C to Z	-5.698e-06	-6.131e-06	-7.036e-06	-7.730e-06
D to Z	-5.458e-06	-5.881e-06	-6.679e-06	-8.000e-06
E to Z	-3.339e-07	-3.686e-07	-4.643e-07	-1.258e-06
F to Z	-2.328e-07	-3.418e-07	-5.137e-07	-9.579e-07

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008
X44_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X33_P16	X44_P16
A	0.0008	0.0023	0.0046	0.0062
B	0.0008	0.0021	0.0042	0.0056
C	0.0009	0.0025	0.0048	0.0063

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0170	0.0180	5.7926	1.9699
A to Z ↑	0.0314	0.0322	11.9943	3.9702
B to Z ↓	0.0167	0.0171	5.8291	1.9846
B to Z ↑	0.0260	0.0259	11.8876	3.9751
C to Z ↓	0.0166	0.0169	3.0305	1.0364
C to Z ↑	0.0343	0.0343	10.9982	3.6611
	X33_P16	**X44_P16**	**X33_P16**	**X44_P16**
A to Z ↓	0.0184	0.0183	0.9957	0.7535

A to Z ↑	0.0323	0.0323	1.9857	1.5004
B to Z ↓	0.0169	0.0168	1.0037	0.7595
B to Z ↑	0.0256	0.0254	1.9860	1.4977
C to Z ↓	0.0187	0.0189	0.6182	0.4830
C to Z ↑	0.0349	0.0347	1.8287	1.3799

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P16	3.457e-07	8.218e-10
X17_P16	9.288e-07	1.536e-09
X33_P16	1.722e-06	2.608e-09
X44_P16	2.253e-06	3.323e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	9.325e-06	3.764e-05	8.137e-05	1.086e-04
B (output stable)	3.021e-05	1.439e-04	3.277e-04	4.234e-04
C (output stable)	9.166e-05	2.871e-04	6.299e-04	8.334e-04
A to Z	8.713e-04	2.824e-03	5.721e-03	7.560e-03
B to Z	6.581e-04	1.940e-03	3.846e-03	5.060e-03
C to Z	1.290e-03	3.880e-03	7.986e-03	1.052e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

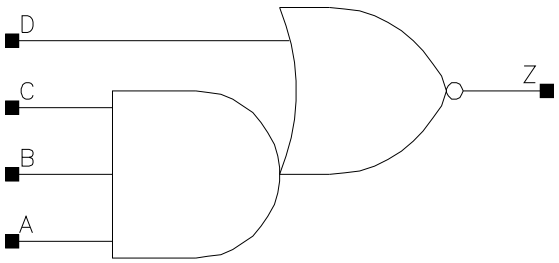
Pin Cycle (vdds)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	4.320e-06	1.246e-05	2.124e-05	2.864e-05
B (output stable)	1.925e-05	4.573e-05	9.975e-05	1.274e-04
C (output stable)	-8.634e-06	-2.030e-05	-4.602e-05	-5.817e-05
A to Z	-2.349e-07	-1.317e-06	-3.589e-06	-4.760e-06
B to Z	1.220e-08	-5.150e-07	-7.900e-08	-3.500e-08
C to Z	-5.255e-06	-1.297e-05	-3.024e-05	-3.743e-05

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X29_P16	1.200	3.536	4.2432
X38_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X29_P16	X38_P16
A	0.0008	0.0047	0.0061
B	0.0008	0.0045	0.0059
C	0.0008	0.0042	0.0056
D	0.0009	0.0048	0.0060

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X29_P16	X5_P16	X29_P16
A to Z ↓	0.0252	0.0269	8.6036	1.4703
A to Z ↑	0.0402	0.0403	11.9837	1.9713
B to Z ↓	0.0246	0.0254	8.6109	1.4716
B to Z ↑	0.0359	0.0355	11.9811	1.9801
C to Z ↓	0.0234	0.0228	8.6270	1.4762
C to Z ↑	0.0308	0.0295	11.8926	1.9914
D to Z ↓	0.0194	0.0216	3.0834	0.6247

D to Z ↑	0.0391	0.0398	10.2347	1.6966
	X38_P16		**X38_P16**	
A to Z ↓	0.0264		1.1257	
A to Z ↑	0.0393		1.4828	
B to Z ↓	0.0252		1.1281	
B to Z ↑	0.0348		1.4921	
C to Z ↓	0.0224		1.1318	
C to Z ↑	0.0287		1.5055	
D to Z ↓	0.0225		0.5190	
D to Z ↑	0.0388		1.2772	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P16	3.514e-07	9.409e-10
X29_P16	1.743e-06	3.442e-09
X38_P16	2.191e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P16	X29_P16	X38_P16
A (output stable)	1.090e-05	1.001e-04	1.213e-04
B (output stable)	2.558e-05	2.336e-04	2.972e-04
C (output stable)	5.283e-05	5.580e-04	7.068e-04
D (output stable)	3.894e-04	3.040e-03	3.965e-03
A to Z	1.356e-03	8.694e-03	1.104e-02
B to Z	1.149e-03	6.964e-03	8.913e-03
C to Z	9.328e-04	5.105e-03	6.442e-03
D to Z	1.707e-03	1.056e-02	1.354e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

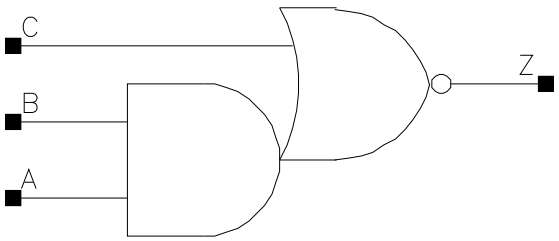
Pin Cycle (vdds)	X5_P16	X29_P16	X38_P16
A (output stable)	9.222e-06	6.488e-05	8.366e-05
B (output stable)	2.134e-06	1.210e-05	1.542e-05
C (output stable)	2.457e-06	9.577e-06	1.172e-05
D (output stable)	-4.901e-05	-4.287e-04	-5.409e-04
A to Z	-7.310e-08	-1.041e-06	-1.279e-06
B to Z	-3.064e-07	-3.071e-06	-3.870e-06
C to Z	-6.480e-08	-1.305e-06	-1.921e-06
D to Z	-5.264e-06	-4.633e-05	-5.863e-05

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X11_P16	1.200	1.088	1.3056
X16_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X11_P16	X16_P16	X23_P16
A	0.0009	0.0017	0.0026	0.0034
B	0.0009	0.0016	0.0024	0.0031
C	0.0008	0.0015	0.0022	0.0031
	X46_P16			
A	0.0065			
B	0.0060			
C	0.0059			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X11_P16	X6_P16	X11_P16
A to Z ↓	0.0195	0.0211	5.6467	2.8409
A to Z ↑	0.0373	0.0394	11.9793	5.8480
B to Z ↓	0.0202	0.0204	5.6716	2.8563

B to Z ↑	0.0329	0.0337	11.9010	5.8613
C to Z ↓	0.0126	0.0132	3.1019	1.8290
C to Z ↑	0.0256	0.0251	10.9131	5.3464
	X16_P16	**X23_P16**	**X16_P16**	**X23_P16**
A to Z ↓	0.0204	0.0208	1.9669	1.4729
A to Z ↑	0.0372	0.0378	3.9216	2.9620
B to Z ↓	0.0203	0.0201	1.9781	1.4812
B to Z ↑	0.0316	0.0319	3.9217	2.9696
C to Z ↓	0.0133	0.0120	1.2880	0.7907
C to Z ↑	0.0243	0.0246	3.5835	2.7118
	X46_P16		**X46_P16**	
A to Z ↓	0.0203		0.7538	
A to Z ↑	0.0365		1.5154	
B to Z ↓	0.0197		0.7582	
B to Z ↑	0.0306		1.5141	
C to Z ↓	0.0122		0.4063	
C to Z ↑	0.0244		1.3866	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P16	3.453e-07	8.218e-10
X11_P16	6.692e-07	1.298e-09
X16_P16	8.669e-07	1.536e-09
X23_P16	1.296e-06	2.013e-09
X46_P16	2.433e-06	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	2.811e-05	7.395e-05	9.795e-05	1.345e-04
B (output stable)	1.042e-04	3.201e-04	3.622e-04	5.121e-04
C (output stable)	3.846e-05	1.009e-04	1.344e-04	2.090e-04
A to Z	1.342e-03	3.020e-03	4.099e-03	5.597e-03
B to Z	1.129e-03	2.383e-03	3.203e-03	4.331e-03
C to Z	6.292e-04	1.277e-03	1.757e-03	2.398e-03
	X46_P16			
A (output stable)	2.421e-04			
B (output stable)	8.385e-04			
C (output stable)	3.111e-04			
A to Z	1.030e-02			
B to Z	7.892e-03			
C to Z	4.493e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	-2.177e-06	-5.909e-06	-5.591e-06	-7.686e-06
B (output stable)	-1.486e-05	-4.251e-05	-3.785e-05	-5.286e-05
C (output stable)	5.521e-05	1.448e-04	1.395e-04	1.920e-04
A to Z	-2.691e-06	-1.048e-05	-8.738e-06	-1.186e-05
B to Z	-3.054e-06	-8.721e-06	-7.502e-06	-1.083e-05
C to Z	-4.817e-08	-2.688e-07	-5.802e-07	-8.183e-07

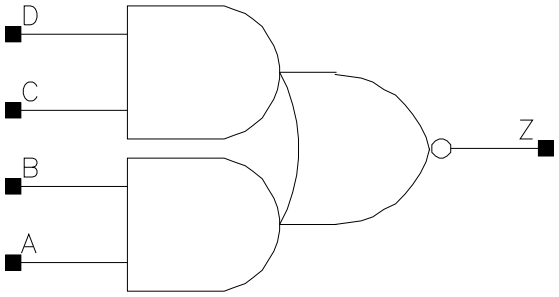
	X46_P16			
A (output stable)	-1.243e-05			
B (output stable)	-8.002e-05			
C (output stable)	3.231e-04			
A to Z	-1.906e-05			
B to Z	-1.416e-05			
C to Z	-1.202e-06			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P16	X10_P16	X16_P16	X21_P16
A	0.0007	0.0018	0.0026	0.0033
B	0.0007	0.0015	0.0024	0.0031
C	0.0006	0.0017	0.0023	0.0031
D	0.0007	0.0014	0.0022	0.0029
	X42_P16			
A	0.0066			
B	0.0062			
C	0.0062			
D	0.0057			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X10_P16**	**X4_P16**	**X10_P16**
A to Z ↓	0.0218	0.0215	7.1266	2.7648
A to Z ↑	0.0478	0.0405	16.7156	5.3946
B to Z ↓	0.0229	0.0227	7.1552	2.7779
B to Z ↑	0.0429	0.0370	16.6937	5.4809
C to Z ↓	0.0175	0.0166	7.2280	2.7708
C to Z ↑	0.0363	0.0314	16.5346	5.3454
D to Z ↓	0.0177	0.0167	7.2662	2.7879
D to Z ↑	0.0311	0.0269	16.5139	5.3990
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0234	0.0234	1.9775	1.4784
A to Z ↑	0.0423	0.0423	3.6217	2.7735
B to Z ↓	0.0237	0.0231	1.9864	1.4856
B to Z ↑	0.0373	0.0369	3.6214	2.7762
C to Z ↓	0.0181	0.0185	1.9709	1.4770
C to Z ↑	0.0326	0.0334	3.5790	2.7373
D to Z ↓	0.0172	0.0168	1.9887	1.4898
D to Z ↑	0.0269	0.0272	3.5833	2.7437
	X42_P16		**X42_P16**	
A to Z ↓	0.0240		0.7626	
A to Z ↑	0.0424		1.3885	
B to Z ↓	0.0237		0.7661	
B to Z ↑	0.0370		1.3847	
C to Z ↓	0.0190		0.7542	
C to Z ↑	0.0335		1.3729	
D to Z ↓	0.0175		0.7609	
D to Z ↑	0.0275		1.3713	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	3.346e-07	9.409e-10
X10_P16	8.648e-07	1.536e-09
X16_P16	1.156e-06	1.894e-09
X21_P16	1.578e-06	2.489e-09
X42_P16	3.023e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	2.584e-05	6.191e-05	1.171e-04	1.556e-04
B (output stable)	4.235e-05	1.051e-04	2.805e-04	4.118e-04
C (output stable)	1.047e-05	2.976e-05	6.251e-05	9.399e-05
D (output stable)	2.848e-05	7.586e-05	2.228e-04	3.467e-04
A to Z	1.389e-03	3.370e-03	5.375e-03	7.046e-03
B to Z	1.209e-03	2.930e-03	4.485e-03	5.801e-03
C to Z	7.917e-04	1.926e-03	3.126e-03	4.251e-03
D to Z	6.241e-04	1.495e-03	2.231e-03	2.966e-03
	X42_P16			
A (output stable)	2.992e-04			
B (output stable)	7.280e-04			
C (output stable)	1.785e-04			
D (output stable)	6.183e-04			

A to Z	1.381e-02			
B to Z	1.146e-02			
C to Z	8.321e-03			
D to Z	5.920e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

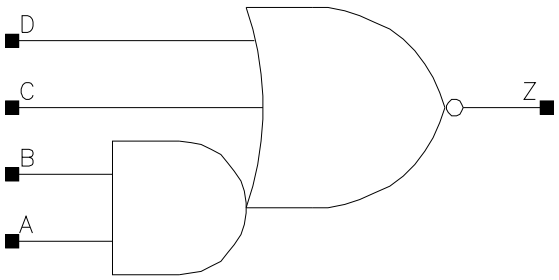
Pin Cycle (vdds)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	-1.854e-06	-3.599e-06	-5.227e-06	-6.346e-06
B (output stable)	-1.827e-06	-3.634e-06	-5.408e-06	-7.826e-06
C (output stable)	1.848e-06	8.293e-06	1.049e-05	1.617e-05
D (output stable)	1.736e-06	7.727e-06	1.063e-05	1.420e-05
A to Z	-6.334e-06	-1.023e-05	-1.524e-05	-1.923e-05
B to Z	-6.304e-06	-9.974e-06	-1.466e-05	-1.706e-05
C to Z	-3.107e-07	-5.193e-07	-1.529e-06	-2.501e-06
D to Z	-9.973e-08	-3.032e-07	-6.607e-07	-8.863e-07
	X42_P16			
A (output stable)	-1.158e-05			
B (output stable)	-1.451e-05			
C (output stable)	3.082e-05			
D (output stable)	2.784e-05			
A to Z	-3.387e-05			
B to Z	-3.149e-05			
C to Z	-5.183e-06			
D to Z	-2.118e-06			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X35_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P16	X35_P16
A	0.0008	0.0059
B	0.0008	0.0054
C	0.0008	0.0059
D	0.0008	0.0055

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X35_P16	X5_P16	X35_P16
A to Z ↓	0.0193	0.0202	5.8757	0.8511
A to Z ↑	0.0422	0.0397	18.3232	2.2988
B to Z ↓	0.0195	0.0193	5.9061	0.8595
B to Z ↑	0.0351	0.0315	18.2600	2.2980
C to Z ↓	0.0193	0.0240	3.2083	0.6209
C to Z ↑	0.0524	0.0513	17.3197	2.1752
D to Z ↓	0.0188	0.0227	3.2337	0.6181

D to Z ↑	0.0499	0.0473	17.3176	2.1776

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P16	2.748e-07	9.409e-10
X35_P16	1.615e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P16	X35_P16
A (output stable)	4.564e-06	5.357e-05
B (output stable)	1.221e-05	1.630e-04
C (output stable)	1.601e-04	1.690e-03
D (output stable)	1.226e-05	1.281e-04
A to Z	1.075e-03	7.904e-03
B to Z	8.638e-04	5.697e-03
C to Z	1.772e-03	1.402e-02
D to Z	1.493e-03	1.104e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

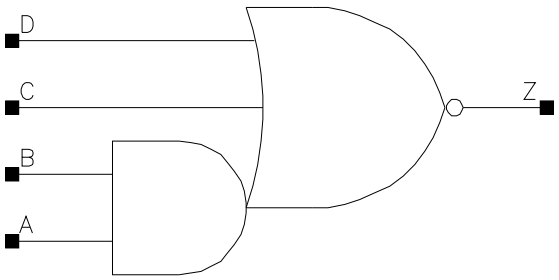
Pin Cycle (vdds)	X5_P16	X35_P16
A (output stable)	4.245e-06	2.917e-05
B (output stable)	1.091e-05	6.753e-05
C (output stable)	-2.697e-05	-2.232e-04
D (output stable)	9.483e-06	7.287e-05
A to Z	-3.331e-07	-5.118e-06
B to Z	-2.738e-07	-2.271e-06
C to Z	-8.747e-06	-6.477e-05
D to Z	-5.407e-06	-3.428e-05

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X17_P16	1.200	2.448	2.9376
X34_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P16	X17_P16	X34_P16
A	0.0008	0.0033	0.0067
B	0.0008	0.0031	0.0063
C	0.0007	0.0028	0.0056
D	0.0007	0.0026	0.0050

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X17_P16	X4_P16	X17_P16
A to Z ↓	0.0224	0.0242	6.4379	1.6882
A to Z ↑	0.0517	0.0548	18.3460	4.4998
B to Z ↓	0.0238	0.0242	6.4629	1.6944
B to Z ↑	0.0459	0.0469	18.2510	4.5043
C to Z ↓	0.0208	0.0205	5.2887	1.2963
C to Z ↑	0.0384	0.0409	17.2546	4.2497

D to Z ↓	0.0179	0.0162	5.4221	1.3019
D to Z ↑	0.0324	0.0297	17.2906	4.2605
	X34_P16		**X34_P16**	
A to Z ↓	0.0240		0.8623	
A to Z ↑	0.0538		2.2771	
B to Z ↓	0.0242		0.8655	
B to Z ↑	0.0461		2.2727	
C to Z ↓	0.0206		0.6763	
C to Z ↑	0.0397		2.1464	
D to Z ↓	0.0162		0.6819	
D to Z ↑	0.0290		2.1478	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	2.144e-07	9.409e-10
X17_P16	8.164e-07	2.489e-09
X34_P16	1.549e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P16	X17_P16	X34_P16
A (output stable)	3.314e-05	1.504e-04	3.028e-04
B (output stable)	5.060e-05	2.747e-04	5.226e-04
C (output stable)	4.221e-05	3.849e-04	7.027e-04
D (output stable)	7.617e-06	9.799e-05	1.744e-04
A to Z	1.686e-03	7.414e-03	1.433e-02
B to Z	1.495e-03	6.230e-03	1.210e-02
C to Z	1.013e-03	4.462e-03	8.471e-03
D to Z	6.936e-04	2.551e-03	4.833e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

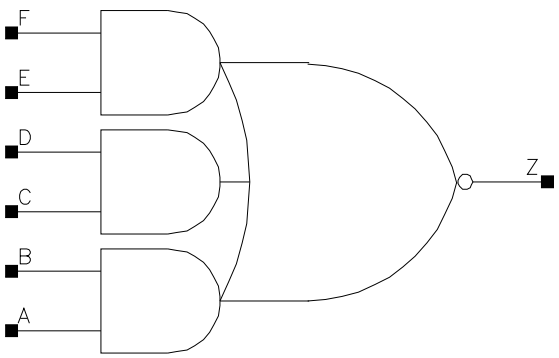
Pin Cycle (vdds)	X4_P16	X17_P16	X34_P16
A (output stable)	-4.320e-06	-1.539e-05	-3.002e-05
B (output stable)	-7.396e-06	-2.660e-05	-5.119e-05
C (output stable)	6.751e-06	-2.056e-05	-2.509e-05
D (output stable)	2.215e-05	9.686e-05	1.772e-04
A to Z	-5.011e-06	-2.430e-05	-4.576e-05
B to Z	-4.980e-06	-2.407e-05	-4.444e-05
C to Z	-1.200e-06	-1.194e-05	-2.058e-05
D to Z	-2.444e-07	-1.467e-06	-3.045e-06

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X8_P16	1.200	2.176	2.6112
X13_P16	1.200	2.720	3.2640
X17_P16	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P16	X8_P16	X13_P16	X17_P16
A	0.0008	0.0016	0.0026	0.0033

B	0.0008	0.0015	0.0023	0.0031
C	0.0008	0.0016	0.0024	0.0030
D	0.0008	0.0015	0.0022	0.0029
E	0.0010	0.0015	0.0022	0.0029
F	0.0008	0.0014	0.0021	0.0027

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0252	0.0305	5.6879	3.2864
A to Z ↑	0.0739	0.0724	17.6168	8.0796
B to Z ↓	0.0272	0.0308	5.7035	3.2935
B to Z ↑	0.0679	0.0653	17.6185	8.0919
C to Z ↓	0.0237	0.0282	5.6216	3.2714
C to Z ↑	0.0644	0.0646	17.6454	8.0890
D to Z ↓	0.0252	0.0286	5.6468	3.2837
D to Z ↑	0.0584	0.0577	17.6021	8.0861
E to Z ↓	0.0186	0.0221	5.4735	3.2615
E to Z ↑	0.0462	0.0463	17.4693	8.0175
F to Z ↓	0.0192	0.0216	5.5181	3.2860
F to Z ↑	0.0398	0.0391	17.5558	8.0271
	X13_P16	**X17_P16**	**X13_P16**	**X17_P16**
A to Z ↓	0.0294	0.0294	2.2340	1.6998
A to Z ↑	0.0676	0.0677	5.3540	4.0711
B to Z ↓	0.0304	0.0298	2.2384	1.7037
B to Z ↑	0.0614	0.0606	5.3668	4.0731
C to Z ↓	0.0274	0.0272	2.2499	1.6795
C to Z ↑	0.0597	0.0599	5.3636	4.0765
D to Z ↓	0.0282	0.0271	2.2577	1.6864
D to Z ↑	0.0536	0.0530	5.3745	4.0765
E to Z ↓	0.0214	0.0213	2.2384	1.6787
E to Z ↑	0.0434	0.0434	5.3230	4.0352
F to Z ↓	0.0211	0.0200	2.2560	1.6912
F to Z ↑	0.0370	0.0362	5.3308	4.0474

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	5.118e-07	1.298e-09
X8_P16	9.547e-07	2.251e-09
X13_P16	1.267e-06	2.727e-09
X17_P16	1.702e-06	3.561e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

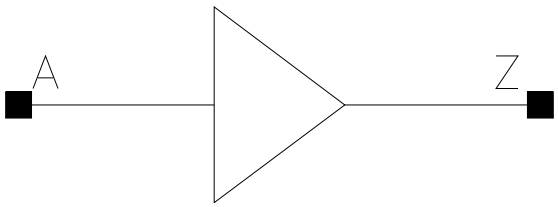
Pin Cycle (vdd)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	8.267e-05	1.850e-04	2.591e-04	3.376e-04
B (output stable)	2.168e-04	5.170e-04	6.543e-04	8.789e-04
C (output stable)	3.880e-05	8.964e-05	1.189e-04	1.657e-04
D (output stable)	5.696e-05	1.971e-04	2.191e-04	3.432e-04
E (output stable)	2.089e-05	5.372e-05	7.852e-05	1.081e-04
F (output stable)	3.392e-05	1.411e-04	1.689e-04	2.661e-04

A to Z	2.695e-03	5.719e-03	7.922e-03	1.045e-02
B to Z	2.483e-03	5.121e-03	7.165e-03	9.294e-03
C to Z	2.017e-03	4.464e-03	5.997e-03	7.967e-03
D to Z	1.814e-03	3.906e-03	5.277e-03	6.861e-03
E to Z	1.242e-03	2.869e-03	3.850e-03	5.095e-03
F to Z	1.038e-03	2.300e-03	3.082e-03	3.938e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	-1.250e-05	-2.712e-05	-3.086e-05	-4.109e-05
B (output stable)	-3.466e-05	-6.900e-05	-7.594e-05	-1.001e-04
C (output stable)	-2.007e-06	-5.422e-06	-3.021e-06	-4.928e-06
D (output stable)	3.146e-06	1.520e-06	4.681e-06	2.923e-06
E (output stable)	2.753e-05	6.272e-05	7.108e-05	9.699e-05
F (output stable)	2.405e-05	5.339e-05	6.137e-05	8.242e-05
A to Z	-1.666e-05	-3.490e-05	-3.696e-05	-5.000e-05
B to Z	-1.730e-05	-3.420e-05	-3.613e-05	-4.914e-05
C to Z	-7.079e-06	-1.633e-05	-1.536e-05	-2.259e-05
D to Z	-6.460e-06	-1.516e-05	-1.514e-05	-2.092e-05
E to Z	-6.189e-07	-1.679e-06	-2.035e-06	-3.310e-06
F to Z	-3.476e-07	-1.132e-06	-1.365e-06	-1.999e-06

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.408	0.4896
X6_P16	1.200	0.408	0.4896
X8_P16	1.200	0.408	0.4896
X13_P16	1.200	0.544	0.6528
X16_P16	1.200	0.544	0.6528
X21_P16	1.200	0.680	0.8160
X25_P16	1.200	0.680	0.8160
X29_P16	1.200	0.952	1.1424
X33_P16	1.200	0.952	1.1424
X42_P16	1.200	1.088	1.3056
X50_P16	1.200	1.224	1.4688
X58_P16	1.200	1.496	1.7952
X67_P16	1.200	1.632	1.9584
X75_P16	1.200	1.768	2.1216
X84_P16	1.200	1.904	2.2848
X100_P16	1.200	2.312	2.7744
X134_P16	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0008	0.0008	0.0008	0.0008
	X16_P16	X21_P16	X25_P16	X29_P16
A	0.0008	0.0011	0.0011	0.0015
	X33_P16	X42_P16	X50_P16	X58_P16
A	0.0015	0.0017	0.0020	0.0030

	X67_P16	X75_P16	X84_P16	X100_P16
A	0.0030	0.0029	0.0029	0.0039
	X134_P16			
A	0.0048			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0441	0.0441	5.6948	4.0766
A to Z ↑	0.0340	0.0333	10.9656	7.8674
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0458	0.0518	2.9714	1.9566
A to Z ↑	0.0341	0.0380	5.5253	3.6536
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0557	0.0456	1.5402	1.1940
A to Z ↑	0.0401	0.0341	2.7736	2.1807
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0474	0.0458	1.0191	0.8693
A to Z ↑	0.0350	0.0331	1.8144	1.5561
	X33_P16	**X42_P16**	**X33_P16**	**X42_P16**
A to Z ↓	0.0481	0.0466	0.7673	0.6220
A to Z ↑	0.0345	0.0345	1.3568	1.0910
	X50_P16	**X58_P16**	**X50_P16**	**X58_P16**
A to Z ↓	0.0454	0.0421	0.5171	0.4457
A to Z ↑	0.0335	0.0316	0.9065	0.7793
	X67_P16	**X75_P16**	**X67_P16**	**X75_P16**
A to Z ↓	0.0443	0.0465	0.3921	0.3538
A to Z ↑	0.0330	0.0345	0.6819	0.6107
	X84_P16	**X100_P16**	**X84_P16**	**X100_P16**
A to Z ↓	0.0485	0.0456	0.3203	0.2689
A to Z ↑	0.0358	0.0340	0.5506	0.4608
	X134_P16		**X134_P16**	
A to Z ↓	0.0476		0.2090	
A to Z ↑	0.0357		0.3509	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	2.912e-07	7.027e-10
X6_P16	3.550e-07	7.027e-10
X8_P16	4.293e-07	7.027e-10
X13_P16	5.484e-07	8.218e-10
X16_P16	6.645e-07	8.218e-10
X21_P16	8.852e-07	9.409e-10
X25_P16	9.778e-07	9.409e-10
X29_P16	1.151e-06	1.179e-09
X33_P16	1.226e-06	1.179e-09
X42_P16	1.501e-06	1.298e-09
X50_P16	1.796e-06	1.417e-09
X58_P16	2.206e-06	1.655e-09
X67_P16	2.411e-06	1.775e-09
X75_P16	2.616e-06	1.894e-09

X84_P16	2.821e-06	2.013e-09
X100_P16	3.436e-06	2.370e-09
X134_P16	4.462e-06	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	1.339e-03	1.487e-03	1.752e-03	2.284e-03
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	2.696e-03	3.704e-03	4.083e-03	4.585e-03
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	5.050e-03	6.391e-03	7.476e-03	9.173e-03
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	1.019e-02	1.135e-02	1.235e-02	1.477e-02
	X134_P16			
A to Z	1.977e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

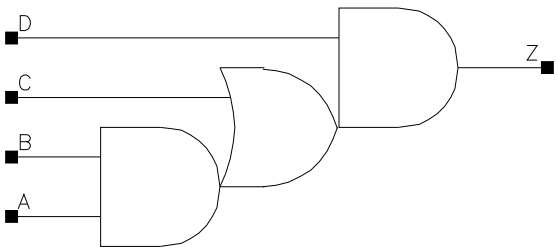
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	-2.024e-07	-2.430e-07	-2.664e-07	-6.461e-08
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	-1.950e-07	-4.777e-07	-5.404e-07	-6.973e-07
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	-5.646e-07	-7.778e-07	-7.795e-07	-1.686e-06
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	-1.435e-06	-1.564e-06	-1.159e-06	-1.816e-06
	X134_P16			
A to Z	-1.563e-06			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.632	1.9584
X25_P16	1.200	1.768	2.1216
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0009	0.0020	0.0020	0.0020
B	0.0010	0.0018	0.0018	0.0017
C	0.0010	0.0022	0.0022	0.0021
D	0.0015	0.0020	0.0020	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0645	0.0606	3.0530	1.5179
A to Z ↑	0.0531	0.0497	5.6018	2.7208
B to Z ↓	0.0598	0.0552	3.0480	1.5166
B to Z ↑	0.0527	0.0480	5.5995	2.7227
C to Z ↓	0.0525	0.0478	3.0391	1.5122
C to Z ↑	0.0392	0.0352	5.5472	2.6966

D to Z ↓	0.0481	0.0420	3.0036	1.4974
D to Z ↑	0.0466	0.0401	5.5575	2.7010
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0672	0.0715	1.0378	0.7859
A to Z ↑	0.0549	0.0578	1.8404	1.3833
B to Z ↓	0.0619	0.0670	1.0362	0.7852
B to Z ↑	0.0534	0.0570	1.8390	1.3830
C to Z ↓	0.0542	0.0590	1.0318	0.7811
C to Z ↑	0.0393	0.0421	1.8212	1.3668
D to Z ↓	0.0457	0.0482	1.0170	0.7666
D to Z ↑	0.0441	0.0464	1.8238	1.3694

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	5.820e-07	1.179e-09
X17_P16	1.062e-06	1.775e-09
X25_P16	1.220e-06	1.894e-09
X33_P16	1.379e-06	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	8.056e-05	1.563e-04	1.568e-04	1.548e-04
B (output stable)	1.026e-04	2.164e-04	2.167e-04	1.889e-04
C (output stable)	2.486e-04	4.224e-04	4.240e-04	4.032e-04
D (output stable)	6.972e-05	9.073e-05	9.081e-05	9.080e-05
A to Z	2.959e-03	5.378e-03	6.648e-03	7.531e-03
B to Z	2.740e-03	4.802e-03	6.067e-03	7.042e-03
C to Z	2.260e-03	3.799e-03	5.068e-03	6.031e-03
D to Z	3.071e-03	5.161e-03	6.423e-03	7.313e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

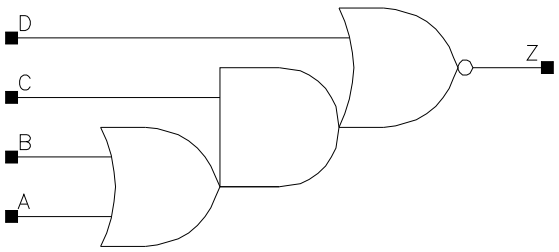
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	-2.144e-06	-4.128e-06	-4.131e-06	-3.976e-06
B (output stable)	-2.184e-06	-4.126e-06	-4.122e-06	-3.992e-06
C (output stable)	1.146e-06	1.553e-06	1.544e-06	1.999e-06
D (output stable)	5.452e-07	7.636e-07	7.935e-07	5.858e-07
A to Z	-3.906e-06	-6.922e-06	-7.392e-06	-7.064e-06
B to Z	-3.675e-06	-6.504e-06	-7.193e-06	-7.436e-06
C to Z	-3.800e-07	-5.145e-07	-4.995e-07	-5.781e-07
D to Z	-8.764e-07	-1.817e-06	-2.123e-06	-2.123e-06

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.952	1.1424
X11_P16	1.200	1.496	1.7952
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X16_P16	X21_P16
A	0.0009	0.0017	0.0025	0.0033
B	0.0009	0.0016	0.0025	0.0033
C	0.0008	0.0016	0.0024	0.0032
D	0.0011	0.0016	0.0023	0.0030

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0235	0.0225	5.4823	2.8756
A to Z ↑	0.0630	0.0581	17.9266	9.2098
B to Z ↓	0.0230	0.0223	5.3784	2.8430
B to Z ↑	0.0588	0.0548	17.9290	9.2293
C to Z ↓	0.0210	0.0200	5.0130	2.6373
C to Z ↑	0.0372	0.0341	11.7280	5.9739

D to Z ↓	0.0140	0.0122	2.9421	1.4957
D to Z ↑	0.0315	0.0271	12.6114	6.4291
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0225	0.0229	1.9701	1.4981
A to Z ↑	0.0546	0.0573	6.0081	4.5760
B to Z ↓	0.0220	0.0223	1.9712	1.4954
B to Z ↑	0.0530	0.0539	5.9925	4.5892
C to Z ↓	0.0203	0.0203	1.8261	1.3833
C to Z ↑	0.0335	0.0338	3.9618	2.9709
D to Z ↓	0.0122	0.0122	1.0520	0.8022
D to Z ↑	0.0257	0.0256	4.2424	3.1970

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P16	4.035e-07	1.179e-09
X11_P16	7.350e-07	1.656e-09
X16_P16	9.404e-07	1.894e-09
X21_P16	1.270e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	4.046e-05	7.085e-05	8.868e-05	1.587e-04
B (output stable)	2.903e-05	6.240e-05	8.324e-05	1.230e-04
C (output stable)	2.129e-04	4.133e-04	5.629e-04	8.266e-04
D (output stable)	3.169e-05	6.494e-05	7.768e-05	1.333e-04
A to Z	2.179e-03	3.804e-03	5.323e-03	7.524e-03
B to Z	1.774e-03	3.127e-03	4.533e-03	6.134e-03
C to Z	1.462e-03	2.483e-03	3.598e-03	4.962e-03
D to Z	8.091e-04	1.311e-03	1.758e-03	2.340e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

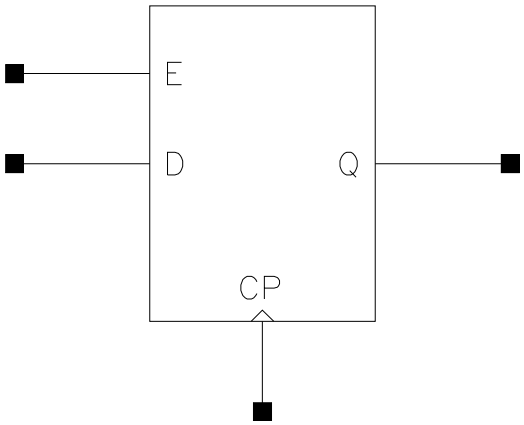
Pin Cycle (vdds)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	-5.852e-06	-8.293e-06	-1.008e-05	-1.910e-05
B (output stable)	1.704e-06	-1.298e-06	5.221e-06	2.930e-06
C (output stable)	-2.377e-05	-4.269e-05	-5.801e-05	-8.907e-05
D (output stable)	3.780e-05	8.155e-05	1.075e-04	1.550e-04
A to Z	-8.298e-06	-1.357e-05	-1.497e-05	-2.570e-05
B to Z	-3.216e-06	-7.073e-06	-7.778e-06	-1.083e-05
C to Z	-4.767e-06	-8.191e-06	-1.093e-05	-1.637e-05
D to Z	-3.063e-07	-4.249e-07	-3.011e-07	-6.829e-07

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.128	3.7536
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
E	0.0011	0.0011	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0748	0.0871	3.0667	1.6008
CP to Q ↑	0.0886	0.0945	5.5920	2.8048
	X33_P16		**X33_P16**	
CP to Q ↓	0.1281		0.7785	
CP to Q ↑	0.1545		1.3846	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1133	0.1133	0.1133
CP ↑	min_pulse_width to CP	0.0597	0.0742	0.0512
D ↓	hold_rising to CP	-0.0557	-0.0526	-0.0582
D ↑	hold_rising to CP	-0.0237	-0.0237	-0.0237
D ↓	setup_rising to CP	0.1222	0.1222	0.1222
D ↑	setup_rising to CP	0.0584	0.0584	0.0588
E ↓	hold_rising to CP	-0.0432	-0.0432	-0.0457
E ↑	hold_rising to CP	-0.0259	-0.0259	-0.0259
E ↓	setup_rising to CP	0.1063	0.1063	0.1063
E ↑	setup_rising to CP	0.1346	0.1346	0.1294

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	1.755e-06	2.966e-09
X17_P16	1.985e-06	3.085e-09
X33_P16	2.693e-06	3.561e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

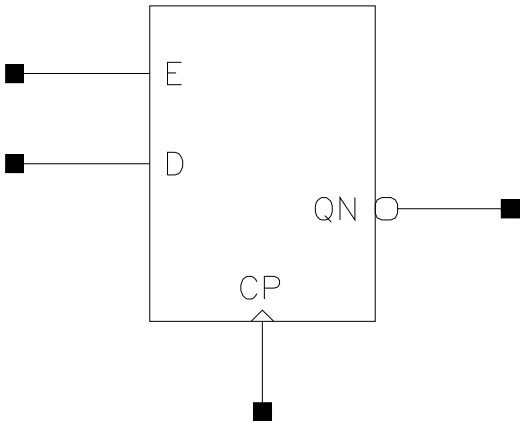
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.202e-03	3.202e-03	3.207e-03
Clock 100Mhz Data 25Mhz	6.800e-03	7.259e-03	9.443e-03
Clock 100Mhz Data 50Mhz	1.040e-02	1.132e-02	1.568e-02
Clock = 0 Data 100Mhz	4.052e-03	4.052e-03	4.053e-03
Clock = 1 Data 100Mhz	1.111e-03	1.111e-03	1.111e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.264	3.9168
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
E	0.0010	0.0010	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.1286	0.1188	3.1342	1.4987
CP to QN ↑	0.0994	0.1029	5.6560	2.7199
	X33_P16		**X33_P16**	
CP to QN ↓	0.1269		0.7829	
CP to QN ↑	0.1141		1.3871	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1133	0.1133	0.1133
CP ↑	min_pulse_width to CP	0.0512	0.0560	0.0645
D ↓	hold_rising to CP	-0.0582	-0.0557	-0.0557
D ↑	hold_rising to CP	-0.0237	-0.0237	-0.0237
D ↓	setup_rising to CP	0.1222	0.1222	0.1222
D ↑	setup_rising to CP	0.0588	0.0588	0.0588
E ↓	hold_rising to CP	-0.0457	-0.0432	-0.0432
E ↑	hold_rising to CP	-0.0259	-0.0259	-0.0259
E ↓	setup_rising to CP	0.1063	0.1063	0.1063
E ↑	setup_rising to CP	0.1346	0.1346	0.1346

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	1.741e-06	2.966e-09
X17_P16	2.101e-06	3.204e-09
X33_P16	2.633e-06	3.561e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

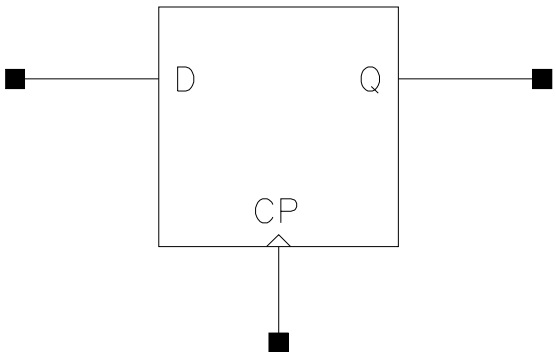
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.200e-03	3.201e-03	3.202e-03
Clock 100Mhz Data 25Mhz	6.851e-03	7.796e-03	9.238e-03
Clock 100Mhz Data 50Mhz	1.050e-02	1.239e-02	1.527e-02
Clock = 0 Data 100Mhz	4.056e-03	4.056e-03	4.057e-03
Clock = 1 Data 100Mhz	1.110e-03	1.110e-03	1.110e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.176	2.6112
X17_P16	1.200	2.448	2.9376
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0780	0.0862	3.0681	1.5870
CP to Q ↑	0.0904	0.1003	5.4444	2.7660
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to Q ↓	0.1108	0.1154	0.9618	0.8724
CP to Q ↑	0.1130	0.1152	1.5640	1.4198

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0999	0.1047	0.1036	0.1036
CP ↑	min_pulse_width to CP	0.0597	0.0731	0.0973	0.1033
D ↓	hold_rising to CP	-0.0020	-0.0045	-0.0045	-0.0045
D ↑	hold_rising to CP	0.0029	0.0029	0.0029	0.0029
D ↓	setup_rising to CP	0.0629	0.0685	0.0685	0.0685
D ↑	setup_rising to CP	0.0267	0.0292	0.0292	0.0292

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	1.441e-06	2.251e-09
X17_P16	1.678e-06	2.489e-09
X30_P16	2.033e-06	2.727e-09
X33_P16	2.098e-06	2.727e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

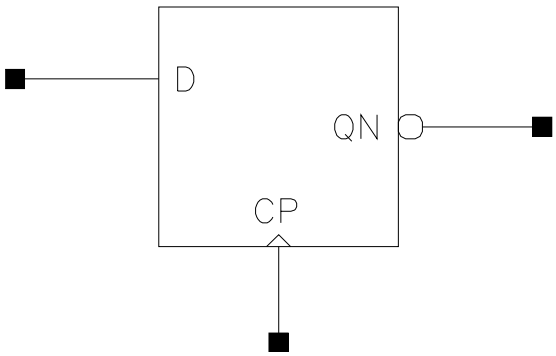
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.401e-03	3.424e-03	3.431e-03	3.435e-03
Clock 100Mhz Data 25Mhz	6.075e-03	6.844e-03	7.835e-03	8.040e-03
Clock 100Mhz Data 50Mhz	8.748e-03	1.026e-02	1.224e-02	1.265e-02
Clock = 0 Data 100Mhz	2.766e-03	2.861e-03	2.889e-03	2.904e-03
Clock = 1 Data 100Mhz	2.730e-05	2.729e-05	2.738e-05	2.739e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.0746	0.0904	3.1519	1.6467
CP to QN ↑	0.0797	0.0844	5.4299	2.7565
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to QN ↓	0.1283	0.1281	0.8644	0.7793
CP to QN ↑	0.1051	0.1233	1.5057	1.3877

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0816	0.0816	0.1036	0.0988
CP ↑	min_pulse_width to CP	0.0548	0.0731	0.0560	0.0731
D ↓	hold_rising to CP	0.0131	0.0127	-0.0041	-0.0020
D ↑	hold_rising to CP	0.0053	0.0078	0.0029	0.0029
D ↓	setup_rising to CP	0.0441	0.0441	0.0685	0.0636
D ↑	setup_rising to CP	0.0394	0.0372	0.0292	0.0267

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	1.330e-06	2.013e-09
X17_P16	1.567e-06	2.132e-09
X30_P16	2.177e-06	2.727e-09
X33_P16	2.320e-06	2.847e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

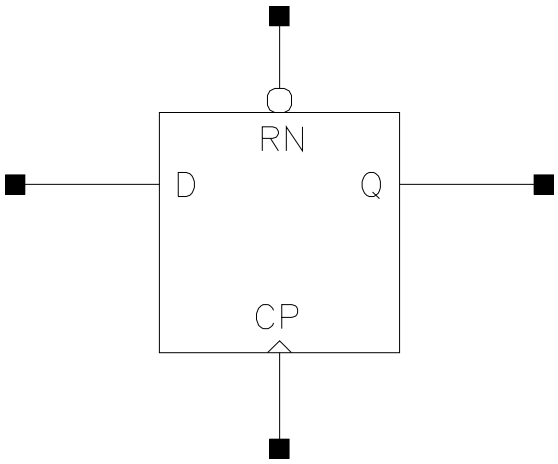
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.272e-03	3.272e-03	3.331e-03	3.354e-03
Clock 100Mhz Data 25Mhz	5.739e-03	6.241e-03	8.169e-03	8.484e-03
Clock 100Mhz Data 50Mhz	8.206e-03	9.210e-03	1.301e-02	1.361e-02
Clock = 0 Data 100Mhz	2.406e-03	2.406e-03	2.587e-03	2.633e-03
Clock = 1 Data 100Mhz	2.707e-05	2.711e-05	2.726e-05	2.735e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0007	0.0007
RN	0.0010	0.0010

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0900	0.1142	1.6036	0.9764
CP to Q ↑	0.1036	0.1159	2.7718	1.5692
RN to Q ↓	0.1514	0.2034	1.7749	1.0945

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.1133	0.1095
CP ↑	min_pulse_width to CP	0.0742	0.0984
D ↓	hold_rising to CP	-0.0045	-0.0045
D ↑	hold_rising to CP	0.0007	0.0007
D ↓	setup_rising to CP	0.0734	0.0734
D ↑	setup_rising to CP	0.0421	0.0421
RN ↓	min_pulse_width to RN	0.1897	0.2505
RN ↑	recovery_rising to CP	0.0419	0.0419
RN ↑	removal_rising to CP	-0.0149	-0.0149

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P16	1.746e-06	3.085e-09
X30_P16	2.025e-06	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

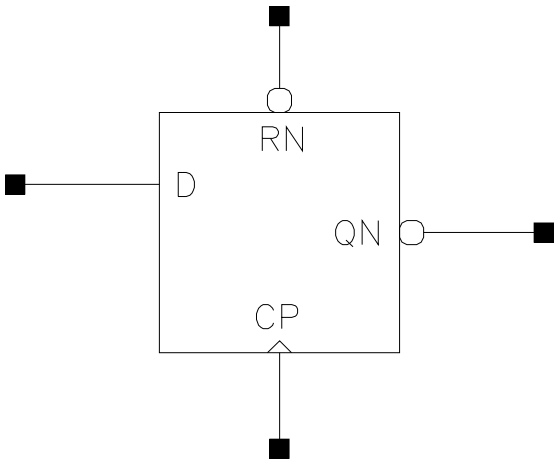
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	3.660e-03	3.660e-03
Clock 100Mhz Data 25Mhz	7.317e-03	8.284e-03
Clock 100Mhz Data 50Mhz	1.097e-02	1.291e-02
Clock = 0 Data 100Mhz	3.391e-03	3.394e-03
Clock = 1 Data 100Mhz	2.769e-05	2.775e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0007	0.0007
RN	0.0010	0.0010

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.1227	0.1326	1.4842	0.8674
CP to QN ↑	0.1024	0.1097	2.7046	1.5112
RN to QN ↑	0.1603	0.1701	2.7192	1.5182

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.1133	0.1095
CP ↑	min_pulse_width to CP	0.0597	0.0608
D ↓	hold_rising to CP	-0.0038	-0.0038
D ↑	hold_rising to CP	0.0007	0.0007
D ↓	setup_rising to CP	0.0731	0.0734
D ↑	setup_rising to CP	0.0394	0.0394
RN ↓	min_pulse_width to RN	0.1475	0.1523
RN ↑	recovery_rising to CP	0.0394	0.0367
RN ↑	removal_rising to CP	-0.0149	-0.0122

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P16	2.098e-06	3.085e-09
X30_P16	2.521e-06	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

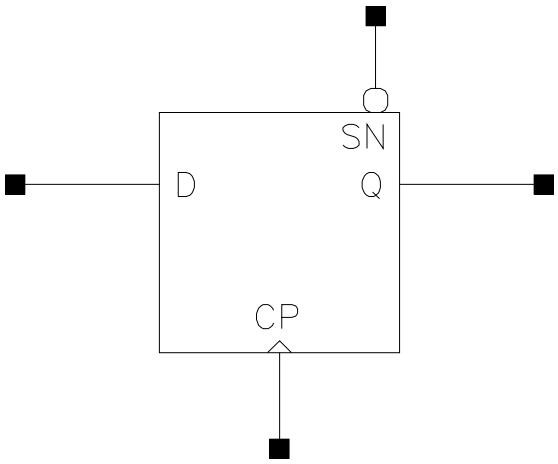
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	3.668e-03	3.666e-03
Clock 100Mhz Data 25Mhz	7.819e-03	8.767e-03
Clock 100Mhz Data 50Mhz	1.197e-02	1.387e-02
Clock = 0 Data 100Mhz	3.436e-03	3.422e-03
Clock = 1 Data 100Mhz	2.768e-05	2.773e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0905	0.1158	1.6077	0.9749
CP to Q ↑	0.1027	0.1155	2.7746	1.5682
SN to Q ↑	0.1043	0.1202	2.7907	1.5788

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.1181	0.1181
CP ↑	min_pulse_width to CP	0.0742	0.1021
D ↓	hold_rising to CP	-0.0045	-0.0045
D ↑	hold_rising to CP	0.0007	0.0007
D ↓	setup_rising to CP	0.0780	0.0783
D ↑	setup_rising to CP	0.0345	0.0345
SN ↓	min_pulse_width to SN	0.0984	0.1184
SN ↑	recovery_rising to CP	0.0225	0.0228
SN ↑	removal_rising to CP	0.0505	0.0505

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P16	1.925e-06	3.085e-09
X30_P16	2.345e-06	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

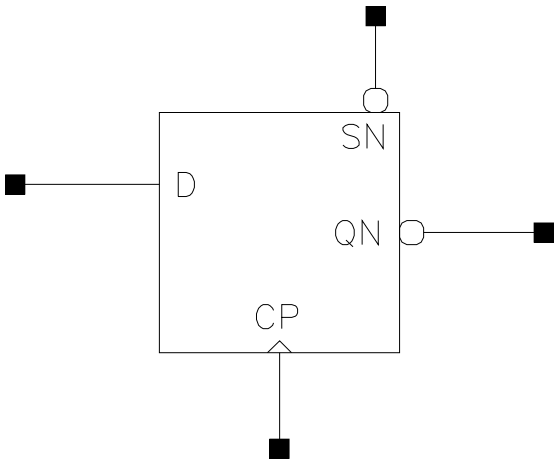
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	3.685e-03	3.678e-03
Clock 100Mhz Data 25Mhz	7.349e-03	8.323e-03
Clock 100Mhz Data 50Mhz	1.101e-02	1.297e-02
Clock = 0 Data 100Mhz	3.369e-03	3.369e-03
Clock = 1 Data 100Mhz	2.124e-05	2.132e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.1218	0.1318	1.4873	0.8691
CP to QN ↑	0.1033	0.1105	2.7007	1.5109
SN to QN ↓	0.1235	0.1339	1.4871	0.8703

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.1181	0.1181
CP ↑	min_pulse_width to CP	0.0596	0.0608
D ↓	hold_rising to CP	-0.0038	-0.0038
D ↑	hold_rising to CP	0.0007	0.0007
D ↓	setup_rising to CP	0.0810	0.0810
D ↑	setup_rising to CP	0.0345	0.0320
SN ↓	min_pulse_width to SN	0.0859	0.0886
SN ↑	recovery_rising to CP	0.0225	0.0228
SN ↑	removal_rising to CP	0.0505	0.0505

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P16	1.870e-06	3.085e-09
X30_P16	2.140e-06	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

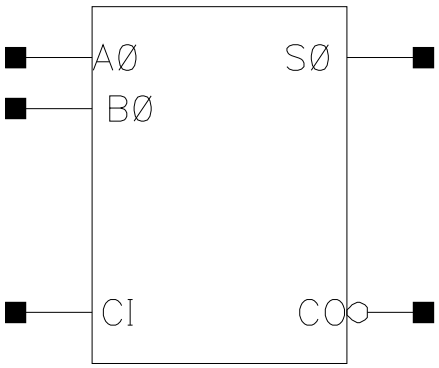
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	3.704e-03	3.702e-03
Clock 100Mhz Data 25Mhz	7.837e-03	8.791e-03
Clock 100Mhz Data 50Mhz	1.197e-02	1.388e-02
Clock = 0 Data 100Mhz	3.365e-03	3.365e-03
Clock = 1 Data 100Mhz	2.774e-05	2.779e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_-P16	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_-P16	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_-P16	1.200	3.672	4.4064
C12T28SOI_LRS1_-FA1X33_P16	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16
A0	0.0033	0.0066	0.0030	0.0058
B0	0.0030	0.0064	0.0032	0.0055
CI	0.0023	0.0050	0.0022	0.0039

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16
A0 to CO ↓	0.0877	0.0949	3.1865	0.8534
A0 to CO ↑	0.0577	0.0586	5.6116	1.4377
A0 to S0 ↓	0.0881	0.1106	3.1435	0.8314
A0 to S0 ↑	0.0901	0.1090	5.5456	1.4122
B0 to CO ↓	0.0854	0.0944	3.2034	0.8596
B0 to CO ↑	0.0589	0.0606	5.6150	1.4334
B0 to S0 ↓	0.0882	0.1119	3.1420	0.8309
B0 to S0 ↑	0.0894	0.1097	5.5463	1.4127
CI to CO ↓	0.0802	0.0895	3.2126	0.8598
CI to CO ↑	0.0573	0.0579	5.6124	1.4379
CI to S0 ↓	0.0865	0.1101	3.1392	0.8308
CI to S0 ↑	0.0881	0.1087	5.5459	1.4124
	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16
A0 to CO ↓	0.0534	0.0665	6.6720	1.1649
A0 to CO ↑	0.0420	0.0484	5.6404	1.4263
A0 to S0 ↓	0.1162	0.1428	3.3493	0.8608
A0 to S0 ↑	0.1039	0.1120	5.7845	1.4346
B0 to CO ↓	0.0535	0.0669	6.6731	1.1674
B0 to CO ↑	0.0399	0.0470	5.6359	1.4262
B0 to S0 ↓	0.1167	0.1459	3.3482	0.8606
B0 to S0 ↑	0.1044	0.1149	5.7859	1.4348
CI to CO ↓	0.0506	0.0887	6.6617	1.1848
CI to CO ↑	0.0447	0.0528	5.7560	1.4368
CI to S0 ↓	0.0637	0.0837	3.3505	0.8606
CI to S0 ↑	0.0531	0.0528	5.7790	1.4346

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_FA1X8_P16	1.364e-06	2.251e-09
C12T28SOI_LR_FA1X33_P16	3.519e-06	4.633e-09
C12T28SOI_LRS1_FA1X8_P16	2.944e-06	3.561e-09
C12T28SOI_LRS1_FA1X33_P16	6.142e-06	7.372e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16
A0 to CO	3.117e-03	8.328e-03	4.692e-03	1.140e-02
A0 to S0	3.136e-03	8.659e-03	6.305e-03	1.419e-02
B0 to CO	3.066e-03	8.301e-03	4.721e-03	1.155e-02
B0 to S0	2.972e-03	8.404e-03	6.398e-03	1.448e-02
CI to CO	3.046e-03	8.281e-03	3.309e-03	9.982e-03
CI to S0	2.957e-03	8.399e-03	3.756e-03	1.083e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16
A0 to CO	-1.537e-05	-3.004e-05	3.506e-06	7.558e-06
A0 to S0	-1.246e-05	-2.470e-05	5.375e-06	1.081e-05
B0 to CO	1.414e-06	2.974e-06	-1.765e-06	-3.911e-06
B0 to S0	9.123e-06	1.755e-05	-6.098e-07	-2.415e-06
CI to CO	1.301e-05	2.508e-05	-3.004e-07	-1.122e-06
CI to S0	6.673e-06	1.163e-05	-4.447e-07	-7.336e-07

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X33_P16	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X33_P16
A0	0.0011	0.0033
B0	0.0011	0.0030

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
A0 to CO ↓	0.0597	0.0529	3.1237	0.7722
A0 to CO ↑	0.0554	0.0474	5.5826	1.4227
A0 to S0 ↓	0.0839	0.0763	3.0610	0.7741
A0 to S0 ↑	0.0749	0.0796	5.5049	1.4072
B0 to CO ↓	0.0584	0.0493	3.1244	0.7670
B0 to CO ↑	0.0574	0.0477	5.5839	1.4228
B0 to S0 ↓	0.0843	0.0735	3.0612	0.7745
B0 to S0 ↑	0.0743	0.0766	5.5027	1.4074

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	7.892e-07	1.417e-09
X33_P16	2.868e-06	2.966e-09

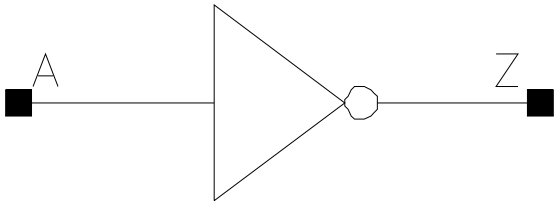
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X33_P16
A0 to CO	2.396e-03	7.724e-03
A0 to S0	2.173e-03	7.355e-03
B0 to CO	2.402e-03	7.547e-03
B0 to S0	2.119e-03	6.915e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X8_P16	X33_P16
A0 to CO	-2.074e-06	-2.302e-05
A0 to S0	-1.618e-06	-1.489e-05
B0 to CO	4.905e-06	3.027e-05
B0 to S0	2.361e-06	1.481e-05

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.272	0.3264
X6_P16	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X13_P16	1.200	0.408	0.4896
X17_P16	1.200	0.408	0.4896
X21_P16	1.200	0.544	0.6528
X25_P16	1.200	0.544	0.6528
X29_P16	1.200	0.680	0.8160
X33_P16	1.200	0.680	0.8160
X50_P16	1.200	0.952	1.1424
X58_P16	1.200	1.088	1.3056
X67_P16	1.200	1.224	1.4688
X75_P16	1.200	1.360	1.6320
X84_P16	1.200	1.496	1.7952
X100_P16	1.200	1.768	2.1216
X134_P16	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0005	0.0007	0.0008	0.0013
	X17_P16	X21_P16	X25_P16	X29_P16
A	0.0016	0.0021	0.0024	0.0028
	X33_P16	X50_P16	X58_P16	X67_P16
A	0.0031	0.0046	0.0054	0.0062
	X75_P16	X84_P16	X100_P16	X134_P16

A	0.0070	0.0079	0.0095	0.0132

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0136	0.0127	5.8023	4.4391
A to Z ↑	0.0221	0.0204	11.0663	8.1962
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0113	0.0102	2.9704	1.9462
A to Z ↑	0.0184	0.0171	5.5610	3.6988
	X17_P16	**X21_P16**	**X17_P16**	**X21_P16**
A to Z ↓	0.0098	0.0106	1.4743	1.1979
A to Z ↑	0.0162	0.0173	2.7259	2.2100
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0104	0.0099	1.0127	0.8672
A to Z ↑	0.0166	0.0160	1.8312	1.5738
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0098	0.0101	0.7639	0.5179
A to Z ↑	0.0157	0.0158	1.3719	0.9183
	X58_P16	**X67_P16**	**X58_P16**	**X67_P16**
A to Z ↓	0.0103	0.0102	0.4489	0.3937
A to Z ↑	0.0161	0.0158	0.7902	0.6914
	X75_P16	**X84_P16**	**X75_P16**	**X84_P16**
A to Z ↓	0.0107	0.0107	0.3543	0.3201
A to Z ↑	0.0163	0.0163	0.6183	0.5581
	X100_P16	**X134_P16**	**X100_P16**	**X134_P16**
A to Z ↓	0.0113	0.0120	0.2713	0.2095
A to Z ↑	0.0169	0.0175	0.4681	0.3568

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.553e-07	5.836e-10
X6_P16	1.964e-07	5.836e-10
X8_P16	2.875e-07	5.836e-10
X13_P16	4.286e-07	7.027e-10
X17_P16	5.506e-07	7.027e-10
X21_P16	6.618e-07	8.218e-10
X25_P16	7.654e-07	8.218e-10
X29_P16	8.819e-07	9.409e-10
X33_P16	9.702e-07	9.409e-10
X50_P16	1.379e-06	1.179e-09
X58_P16	1.584e-06	1.298e-09
X67_P16	1.789e-06	1.417e-09
X75_P16	1.994e-06	1.536e-09
X84_P16	2.199e-06	1.655e-09
X100_P16	2.609e-06	1.894e-09
X134_P16	3.430e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16

A to Z	3.358e-04	3.904e-04	4.638e-04	5.892e-04
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	7.155e-04	1.051e-03	1.175e-03	1.238e-03
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	1.354e-03	2.031e-03	2.517e-03	2.698e-03
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	3.148e-03	3.378e-03	4.041e-03	5.406e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

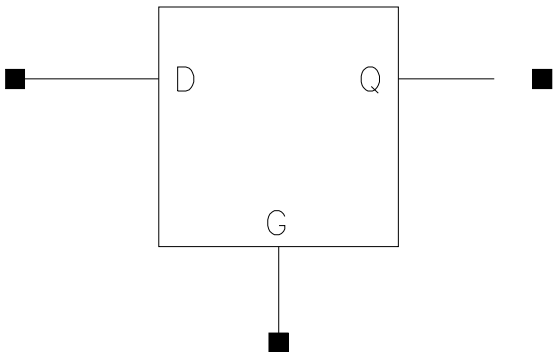
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	-1.810e-08	-1.890e-08	-2.901e-07	-1.530e-07
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	3.390e-08	-8.888e-07	2.975e-07	2.010e-08
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	3.172e-07	2.465e-07	3.480e-07	1.116e-06
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	9.390e-07	-9.470e-07	-1.810e-06	-5.457e-06

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X23_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P16	X23_P16
D	0.0006	0.0013
G	0.0013	0.0020

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X23_P16	X8_P16	X23_P16
D to Q ↓	0.1011	0.0768	3.2733	1.5574
D to Q ↑	0.0584	0.0579	5.5028	1.4513
G to Q ↓	0.1072	0.0780	3.2709	1.5581
G to Q ↑	0.0557	0.0501	5.5011	1.4509

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P16	X23_P16
D ↓	hold_falling to G	-0.0432	-0.0263
D ↑	hold_falling to G	-0.0167	-0.0167
D ↓	setup_falling to G	0.0974	0.0682
D ↑	setup_falling to G	0.0617	0.0666
G ↑	min_pulse_width to G	0.0926	0.0676

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	7.667e-07	1.417e-09
X23_P16	1.361e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X23_P16
D (output stable)	1.558e-05	7.028e-05
G (output stable)	7.876e-04	1.514e-03
D to Q	3.598e-03	6.934e-03
G to Q	3.295e-03	6.009e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

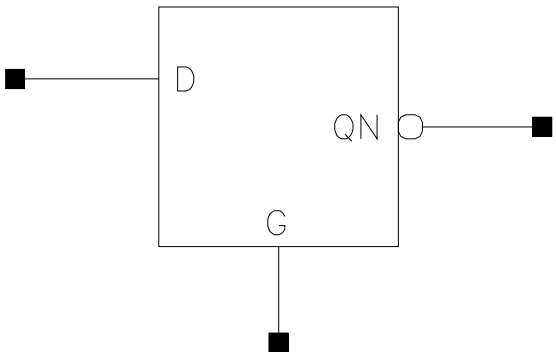
Pin Cycle (vdds)	X8_P16	X23_P16
D (output stable)	-1.233e-06	-4.893e-06
G (output stable)	2.941e-06	5.368e-06
D to Q	-2.567e-06	-5.426e-06
G to Q	2.398e-05	1.726e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P16
D	0.0006
G	0.0014

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P16	X17_P16
D to QN ↓	0.0799	1.4944
D to QN ↑	0.1099	2.6950
G to QN ↓	0.0767	1.4935
G to QN ↑	0.1118	2.6940

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P16
D ↓	hold_falling to G	-0.0533
D ↑	hold_falling to G	-0.0223
D ↓	setup_falling to G	0.0831
D ↑	setup_falling to G	0.0520
G ↑	min_pulse_width to G	0.0722

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P16	1.133e-06	1.536e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X17_P16
D (output stable)	2.417e-05
G (output stable)	8.552e-04
D to QN	4.638e-03
G to QN	4.190e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

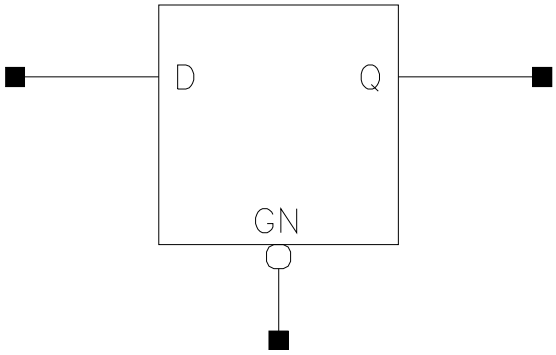
Pin Cycle (vdds)	X17_P16
D (output stable)	-4.207e-06
G (output stable)	6.199e-06
D to QN	-2.524e-06
G to QN	4.989e-05

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
D	0.0005	0.0008	0.0017
GN	0.0012	0.0015	0.0020

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D to Q ↓	0.1021	0.0854	3.2921	1.5973
D to Q ↑	0.0599	0.0541	5.5058	2.8128
GN to Q ↓	0.0893	0.0735	3.2890	1.5958
GN to Q ↑	0.0903	0.0832	5.5083	2.8112

	X33_P16		X33_P16	
D to Q ↓	0.0817		0.8112	
D to Q ↑	0.0457		1.4049	
GN to Q ↓	0.0680		0.8117	
GN to Q ↑	0.0634		1.4059	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P16	X17_P16	X33_P16
D ↓	hold_rising to GN	-0.0504	-0.0382	-0.0382
D ↑	hold_rising to GN	-0.0143	-0.0090	-0.0042
D ↓	setup_rising to GN	0.1149	0.0951	0.0902
D ↑	setup_rising to GN	0.0539	0.0487	0.0386
GN ↓	min_pulse_width to GN	0.1124	0.0970	0.0886

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	7.013e-07	1.417e-09
X17_P16	1.077e-06	1.655e-09
X33_P16	1.738e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
D (output stable)	1.763e-05	2.929e-05	8.156e-05
GN (output stable)	7.852e-04	1.073e-03	1.280e-03
D to Q	3.600e-03	5.000e-03	8.115e-03
GN to Q	5.189e-03	6.991e-03	1.015e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

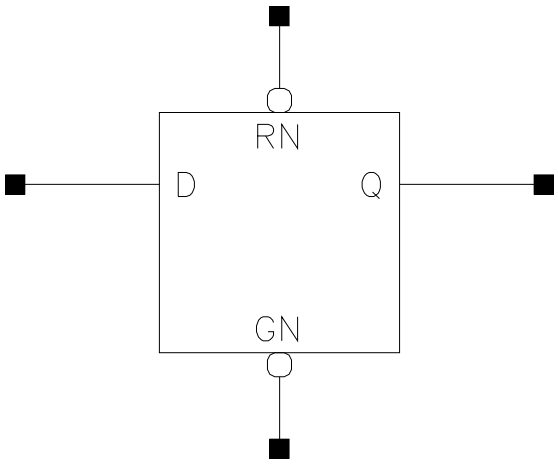
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
D (output stable)	-1.205e-06	-1.856e-06	-4.989e-06
GN (output stable)	2.677e-06	5.137e-06	5.502e-06
D to Q	-2.492e-06	-3.083e-06	-5.597e-06
GN to Q	-3.316e-05	-1.473e-05	-1.447e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.496	1.7952
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X33_P16
D	0.0006	0.0013
GN	0.0013	0.0025
RN	0.0006	0.0006

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
D to Q ↓	0.0948	0.0828	3.1705	0.8183
D to Q ↑	0.0782	0.0970	5.6166	1.4590

GN to Q ↓	0.0835	0.0743	3.1712	0.8192
GN to Q ↑	0.1042	0.1045	5.6137	1.4603
RN to Q ↓	0.0669	0.1260	3.0237	0.9159
RN to Q ↑	0.0846	0.1040	5.6167	1.4602

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P16	X33_P16
D ↓	hold_rising to GN	-0.0456	-0.0358
D ↑	hold_rising to GN	-0.0290	-0.0537
D ↓	setup_rising to GN	0.1003	0.0881
D ↑	setup_rising to GN	0.0734	0.1079
GN ↓	min_pulse_width to GN	0.0980	0.1049
RN ↓	min_pulse_width to RN	0.0823	0.1480
RN ↑	recovery_rising to GN	0.0835	0.1145
RN ↑	removal_rising to GN	-0.0534	-0.0777

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	6.234e-07	1.655e-09
X33_P16	1.361e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X33_P16
D (output stable)	6.597e-05	9.560e-05
GN (output stable)	9.169e-04	1.359e-03
RN (output stable)	2.045e-05	3.810e-05
D to Q	3.552e-03	8.685e-03
GN to Q	5.255e-03	1.120e-02
RN to Q	2.885e-03	6.514e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

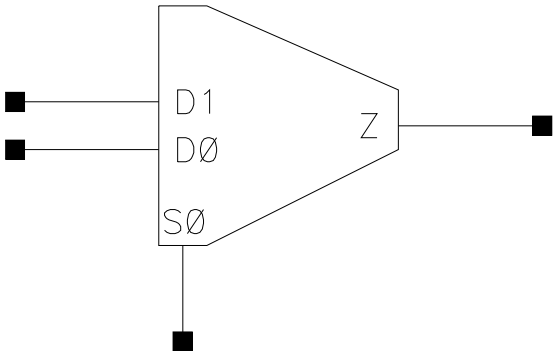
Pin Cycle (vdds)	X8_P16	X33_P16
D (output stable)	-3.101e-06	-7.442e-06
GN (output stable)	2.415e-06	7.372e-06
RN (output stable)	4.510e-07	7.160e-07
D to Q	-2.725e-06	-4.521e-06
GN to Q	-3.425e-05	4.435e-05
RN to Q	2.049e-06	-3.166e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
D0	0.0007	0.0011	0.0014	0.0020
D1	0.0007	0.0011	0.0014	0.0019
S0	0.0014	0.0015	0.0018	0.0026

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D0 to Z ↓	0.0724	0.0627	3.1249	1.5304
D0 to Z ↑	0.0544	0.0485	5.6079	2.7343
D1 to Z ↓	0.0693	0.0625	3.1123	1.5283
D1 to Z ↑	0.0495	0.0450	5.6003	2.7304
S0 to Z ↓	0.0620	0.0581	3.1133	1.5268
S0 to Z ↑	0.0569	0.0553	5.6041	2.7326

	X25_P16	X33_P16	X25_P16	X33_P16
D0 to Z ↓	0.0681	0.0606	1.0588	0.7916
D0 to Z ↑	0.0540	0.0483	1.8396	1.3764
D1 to Z ↓	0.0733	0.0635	1.0638	0.7934
D1 to Z ↑	0.0505	0.0458	1.8351	1.3736
S0 to Z ↓	0.0675	0.0608	1.0602	0.7918
S0 to Z ↑	0.0627	0.0561	1.8392	1.3762

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	8.595e-07	1.417e-09
X17_P16	1.424e-06	1.536e-09
X25_P16	1.983e-06	2.370e-09
X33_P16	2.690e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	6.828e-04	9.629e-04	1.014e-03	1.333e-03
D1 (output stable)	5.376e-04	8.711e-04	1.160e-03	1.414e-03
S0 (output stable)	9.485e-04	1.079e-03	1.403e-03	1.709e-03
D0 to Z	2.493e-03	3.954e-03	6.143e-03	7.678e-03
D1 to Z	2.291e-03	3.821e-03	6.195e-03	7.582e-03
S0 to Z	2.865e-03	4.241e-03	6.901e-03	8.426e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

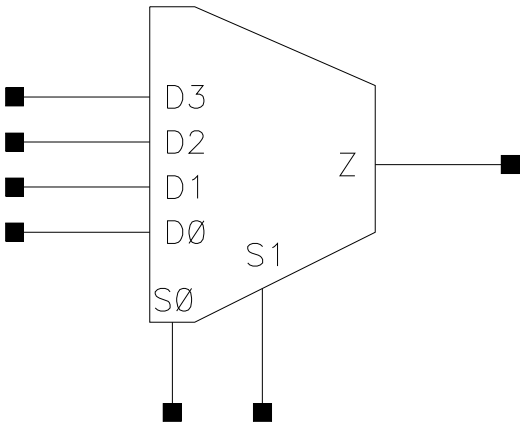
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	-1.489e-07	-5.975e-08	-1.790e-07	5.580e-08
D1 (output stable)	-9.115e-08	-1.672e-07	-2.435e-07	4.380e-07
S0 (output stable)	-6.205e-08	-5.995e-08	-1.629e-07	-1.824e-07
D0 to Z	-1.181e-07	-7.920e-08	-5.536e-07	-7.040e-07
D1 to Z	-1.823e-07	-3.210e-07	-5.613e-07	4.750e-08
S0 to Z	-1.547e-07	-2.349e-07	-5.670e-07	-6.068e-07

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.312	2.7744
X31_P16	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P16	X31_P16
D0	0.0005	0.0014
D1	0.0005	0.0014
D2	0.0005	0.0014
D3	0.0005	0.0014
S0	0.0019	0.0038
S1	0.0013	0.0025

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X31_P16	X8_P16	X31_P16

D0 to Z ↓	0.1380	0.1369	3.3508	0.9306
D0 to Z ↑	0.0797	0.0789	5.6678	1.5191
D1 to Z ↓	0.1371	0.1373	3.3498	0.9305
D1 to Z ↑	0.0803	0.0786	5.6704	1.5193
D2 to Z ↓	0.1488	0.1285	3.3783	0.9202
D2 to Z ↑	0.0839	0.0735	5.6897	1.5090
D3 to Z ↓	0.1483	0.1278	3.3775	0.9190
D3 to Z ↑	0.0828	0.0748	5.6877	1.5129
S0 to Z ↓	0.1512	0.1465	3.3584	0.9240
S0 to Z ↑	0.1013	0.1014	5.6832	1.5167
S1 to Z ↓	0.1090	0.1006	3.3644	0.9253
S1 to Z ↑	0.0753	0.0735	5.6736	1.5150

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	8.531e-07	2.370e-09
X31_P16	2.353e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X31_P16
D0 (output stable)	4.006e-05	1.835e-04
D1 (output stable)	3.940e-05	1.926e-04
D2 (output stable)	3.334e-05	9.901e-05
D3 (output stable)	3.606e-05	1.699e-04
S0 (output stable)	1.513e-03	3.562e-03
S1 (output stable)	9.833e-04	2.137e-03
D0 to Z	2.660e-03	8.833e-03
D1 to Z	2.654e-03	8.880e-03
D2 to Z	2.863e-03	8.302e-03
D3 to Z	2.855e-03	8.286e-03
S0 to Z	4.304e-03	1.243e-02
S1 to Z	2.982e-03	8.220e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

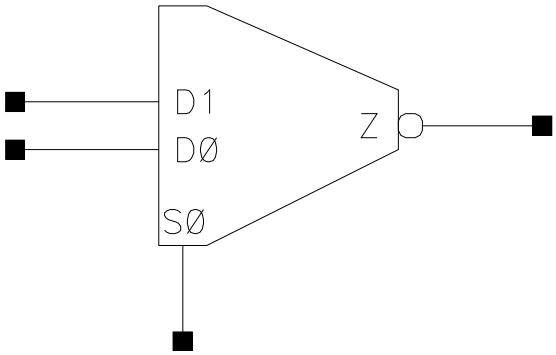
Pin Cycle (vdds)	X8_P16	X31_P16
D0 (output stable)	-3.841e-06	-1.593e-05
D1 (output stable)	-3.387e-06	-1.416e-05
D2 (output stable)	-3.363e-06	-5.266e-06
D3 (output stable)	-3.311e-06	-1.037e-05
S0 (output stable)	-1.874e-05	-6.649e-05
S1 (output stable)	1.826e-05	7.390e-05
D0 to Z	-4.146e-06	-1.497e-05
D1 to Z	-4.226e-06	-1.477e-05
D2 to Z	-4.723e-06	-1.248e-05
D3 to Z	-4.635e-06	-1.198e-05
S0 to Z	-1.665e-05	-5.587e-05
S1 to Z	2.281e-05	1.008e-04

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.816	0.9792
X5_P16	1.200	0.952	1.1424
X10_P16	1.200	1.768	2.1216
X16_P16	1.200	2.448	2.9376
X21_P16	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P16	X5_P16	X10_P16	X16_P16
D0	0.0005	0.0008	0.0017	0.0025
D1	0.0005	0.0008	0.0016	0.0025
S0	0.0012	0.0021	0.0028	0.0041
	X21_P16			
D0	0.0034			
D1	0.0033			
S0	0.0047			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X5_P16	X3_P16	X5_P16
D0 to Z ↓	0.0230	0.0224	11.1996	6.4343

D0 to Z ↑	0.0430	0.0380	26.6185	13.0875
D1 to Z ↓	0.0225	0.0210	11.0696	6.2145
D1 to Z ↑	0.0450	0.0399	26.6236	13.3972
S0 to Z ↓	0.0362	0.0289	11.1087	6.3162
S0 to Z ↑	0.0408	0.0323	26.5556	13.2292
	X10_P16	**X16_P16**	**X10_P16**	**X16_P16**
D0 to Z ↓	0.0252	0.0234	2.9916	1.9549
D0 to Z ↑	0.0413	0.0392	6.0277	3.9542
D1 to Z ↓	0.0222	0.0218	2.9225	1.9373
D1 to Z ↑	0.0419	0.0405	6.0913	3.9783
S0 to Z ↓	0.0351	0.0303	2.9484	1.9420
S0 to Z ↑	0.0380	0.0330	6.0512	3.9625
	X21_P16		**X21_P16**	
D0 to Z ↓	0.0232		1.4849	
D0 to Z ↑	0.0383		2.9859	
D1 to Z ↓	0.0217		1.4656	
D1 to Z ↑	0.0406		2.9725	
S0 to Z ↓	0.0314		1.4721	
S0 to Z ↑	0.0335		2.9779	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P16	3.321e-07	1.060e-09
X5_P16	6.560e-07	1.179e-09
X10_P16	1.137e-06	1.894e-09
X16_P16	1.723e-06	2.489e-09
X21_P16	2.107e-06	3.085e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	1.784e-05	3.637e-05	1.169e-04	1.877e-04
D1 (output stable)	2.426e-05	1.384e-04	1.460e-04	2.257e-04
S0 (output stable)	7.847e-04	1.102e-03	1.984e-03	3.000e-03
D0 to Z	7.764e-04	1.306e-03	3.270e-03	4.580e-03
D1 to Z	7.795e-04	1.297e-03	3.097e-03	4.512e-03
S0 to Z	1.357e-03	1.870e-03	4.001e-03	5.491e-03
	X21_P16			
D0 (output stable)	2.473e-04			
D1 (output stable)	3.474e-04			
S0 (output stable)	3.321e-03			
D0 to Z	5.860e-03			
D1 to Z	5.965e-03			
S0 to Z	6.688e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	-1.232e-06	-2.024e-06	-5.753e-06	-1.311e-05
D1 (output stable)	-4.439e-06	-2.802e-05	-1.946e-05	-3.298e-05
S0 (output stable)	6.056e-06	3.120e-05	2.322e-05	3.579e-05
D0 to Z	-6.403e-07	-8.066e-07	-3.327e-06	-8.617e-06

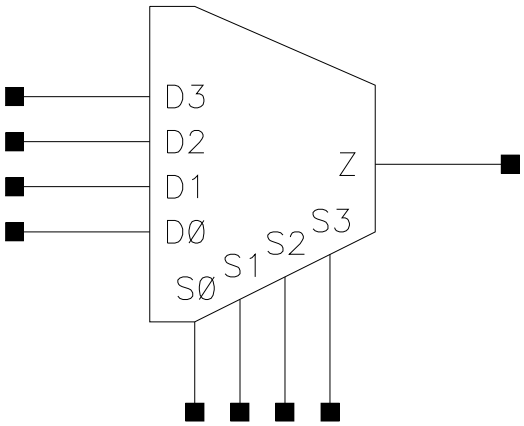
D1 to Z	-8.877e-07	-3.046e-06	-4.202e-06	-8.305e-06
S0 to Z	7.798e-06	1.698e-05	2.965e-05	5.927e-05
	X21_P16			
D0 (output stable)	-1.594e-05			
D1 (output stable)	-5.852e-05			
S0 (output stable)	5.960e-05			
D0 to Z	-8.825e-06			
D1 to Z	-1.198e-05			
S0 to Z	7.253e-05			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	1.768	2.1216
X27_P16	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P16	X27_P16
D0	0.0006	0.0020
D1	0.0006	0.0020
D2	0.0006	0.0019
D3	0.0006	0.0020
S0	0.0006	0.0018
S1	0.0007	0.0018
S2	0.0006	0.0018
S3	0.0007	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	X27_P16	X7_P16	X27_P16
D0 to Z ↓	0.0991	0.0812	5.5007	1.4931
D0 to Z ↑	0.0655	0.0534	5.5209	1.3688
D1 to Z ↓	0.0882	0.0724	5.4979	1.4917
D1 to Z ↑	0.0596	0.0476	5.4966	1.3630
D2 to Z ↓	0.1003	0.0770	5.5245	1.4962
D2 to Z ↑	0.0642	0.0497	5.5445	1.3747
D3 to Z ↓	0.0894	0.0684	5.5038	1.4930
D3 to Z ↑	0.0584	0.0440	5.5204	1.3694
S0 to Z ↓	0.0959	0.0765	5.4992	1.4923
S0 to Z ↑	0.0680	0.0545	5.5170	1.3684
S1 to Z ↓	0.0856	0.0675	5.4979	1.4913
S1 to Z ↑	0.0621	0.0482	5.4967	1.3634
S2 to Z ↓	0.0970	0.0724	5.5170	1.4930
S2 to Z ↑	0.0668	0.0508	5.5424	1.3749
S3 to Z ↓	0.0868	0.0636	5.5108	1.4927
S3 to Z ↑	0.0608	0.0447	5.5261	1.3703

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X7_P16	7.640e-07	1.894e-09
X27_P16	2.632e-06	3.561e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X7_P16	X27_P16
D0 (output stable)	4.404e-04	1.382e-03
D1 (output stable)	3.414e-04	1.043e-03
D2 (output stable)	4.309e-04	1.354e-03
D3 (output stable)	3.197e-04	9.908e-04
S0 (output stable)	4.526e-04	1.384e-03
S1 (output stable)	3.381e-04	1.020e-03
S2 (output stable)	4.098e-04	1.282e-03
S3 (output stable)	3.069e-04	9.499e-04
D0 to Z	3.274e-03	1.020e-02
D1 to Z	2.860e-03	8.753e-03
D2 to Z	3.150e-03	8.755e-03
D3 to Z	2.740e-03	7.323e-03
S0 to Z	3.194e-03	9.647e-03
S1 to Z	2.776e-03	8.205e-03
S2 to Z	3.069e-03	8.201e-03
S3 to Z	2.657e-03	6.786e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

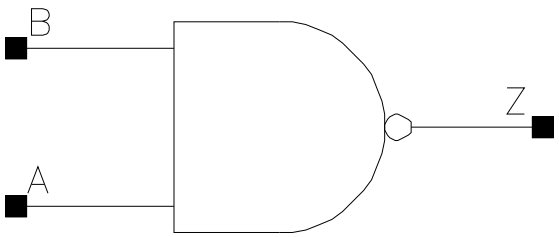
Pin Cycle (vdds)	X7_P16	X27_P16
D0 (output stable)	-3.130e-06	-7.013e-06
D1 (output stable)	6.126e-07	5.613e-06
D2 (output stable)	-6.282e-06	-1.350e-05
D3 (output stable)	6.071e-06	2.007e-05
S0 (output stable)	-6.404e-06	-1.479e-05
S1 (output stable)	5.983e-06	1.988e-05
S2 (output stable)	-3.687e-06	-7.421e-06
S3 (output stable)	2.764e-06	1.272e-05
D0 to Z	-5.902e-06	-1.120e-05
D1 to Z	-3.627e-07	-6.089e-07
D2 to Z	-5.274e-06	-1.050e-05
D3 to Z	-1.483e-07	-2.232e-07
S0 to Z	-5.930e-06	-1.139e-05
S1 to Z	-2.526e-07	-7.806e-07
S2 to Z	-5.293e-06	-1.065e-05
S3 to Z	-3.833e-09	-4.028e-07

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P16	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P16	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P16	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P16	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P16	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P16	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P16	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P16	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P16	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P16	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P16	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P16	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P16	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P16	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P16	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P16	C12T28SOI_LR_-NAND2X5_P16	C12T28SOI_LR_-NAND2X7_P16	C12T28SOI_LR_-NAND2X10_P16
A	0.0005	0.0007	0.0008	0.0013
B	0.0006	0.0007	0.0008	0.0012
	C12T28SOI_LR_-NAND2X13_P16	C12T28SOI_LR_-NAND2X17_P16	C12T28SOI_LR_-NAND2X20_P16	C12T28SOI_LR_-NAND2X24_P16
A	0.0016	0.0021	0.0024	0.0029
B	0.0015	0.0020	0.0022	0.0027
	C12T28SOI_LR_-NAND2X27_P16	C12T28SOI_LR_-NAND2X42_P16	C12T28SOI_LR_-NAND2X47_P16	C12T28SOI_LR_-NAND2X50_P16
A	0.0032	0.0010	0.0010	0.0010
B	0.0030	0.0011	0.0011	0.0011
	C12T28SOI_LR_-NAND2X58_P16	C12T28SOI_LR_-NAND2X67_P16	C12T28SOI_-LRBR0D8_-NAND2X7_P16	C12T28SOI_-LRBR0D8_-NAND2X14_P16
A	0.0010	0.0010	0.0008	0.0016
B	0.0011	0.0011	0.0008	0.0015
	C12T28SOI_LRS_-NAND2X40_P16	C12T28SOI_LRS_-NAND2X54_P16		
A	0.0049	0.0064		
B	0.0044	0.0059		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P16	**C12T28SOI_LR_-NAND2X5_P16**	**C12T28SOI_LR_-NAND2X3_P16**	**C12T28SOI_LR_-NAND2X5_P16**
A to Z ↓	0.0176	0.0157	10.7893	6.7023
A to Z ↑	0.0257	0.0233	11.0447	6.8770
B to Z ↓	0.0187	0.0160	10.8656	6.7590
B to Z ↑	0.0237	0.0206	11.1017	6.9120
	C12T28SOI_LR_-NAND2X7_P16	**C12T28SOI_LR_-NAND2X10_P16**	**C12T28SOI_LR_-NAND2X7_P16**	**C12T28SOI_LR_-NAND2X10_P16**
A to Z ↓	0.0154	0.0182	5.5784	3.7489
A to Z ↑	0.0226	0.0244	5.5271	3.6646
B to Z ↓	0.0156	0.0159	5.6139	3.7786
B to Z ↑	0.0199	0.0201	5.5727	3.6883
	C12T28SOI_LR_-NAND2X13_P16	**C12T28SOI_LR_-NAND2X17_P16**	**C12T28SOI_LR_-NAND2X13_P16**	**C12T28SOI_LR_-NAND2X17_P16**
A to Z ↓	0.0172	0.0172	2.8366	2.2801

A to Z ↑	0.0231	0.0234	2.7060	2.1973
B to Z ↓	0.0149	0.0156	2.8606	2.2952
B to Z ↑	0.0188	0.0195	2.7239	2.2111
	C12T28SOI_LR_-NAND2X20_P16	**C12T28SOI_LR_-NAND2X24_P16**	**C12T28SOI_LR_-NAND2X20_P16**	**C12T28SOI_LR_-NAND2X24_P16**
A to Z ↓	0.0168	0.0176	1.9363	1.6623
A to Z ↑	0.0227	0.0233	1.8189	1.5629
B to Z ↓	0.0154	0.0152	1.9532	1.6756
B to Z ↑	0.0190	0.0189	1.8332	1.5739
	C12T28SOI_LR_-NAND2X27_P16	**C12T28SOI_LR_-NAND2X42_P16**	**C12T28SOI_LR_-NAND2X27_P16**	**C12T28SOI_LR_-NAND2X42_P16**
A to Z ↓	0.0172	0.0642	1.4703	0.6257
A to Z ↑	0.0228	0.0647	1.3635	1.0902
B to Z ↓	0.0149	0.0654	1.4820	0.6256
B to Z ↑	0.0184	0.0624	1.3731	1.0903
	C12T28SOI_LR_-NAND2X47_P16	**C12T28SOI_LR_-NAND2X50_P16**	**C12T28SOI_LR_-NAND2X47_P16**	**C12T28SOI_LR_-NAND2X50_P16**
A to Z ↓	0.0663	0.0668	0.5589	0.5237
A to Z ↑	0.0659	0.0662	0.9503	0.9097
B to Z ↓	0.0675	0.0680	0.5593	0.5239
B to Z ↑	0.0636	0.0640	0.9498	0.9098
	C12T28SOI_LR_-NAND2X58_P16	**C12T28SOI_LR_-NAND2X67_P16**	**C12T28SOI_LR_-NAND2X58_P16**	**C12T28SOI_LR_-NAND2X67_P16**
A to Z ↓	0.0703	0.0728	0.4540	0.4006
A to Z ↑	0.0687	0.0702	0.7826	0.6874
B to Z ↓	0.0714	0.0739	0.4538	0.4006
B to Z ↑	0.0663	0.0679	0.7829	0.6873
	C12T28SOI_-LRBR0D8_-NAND2X7_P16	**C12T28SOI_-LRBR0D8_-NAND2X14_P16**	**C12T28SOI_-LRBR0D8_-NAND2X7_P16**	**C12T28SOI_-LRBR0D8_-NAND2X14_P16**
A to Z ↓	0.0133	0.0151	4.1370	2.1543
A to Z ↑	0.0269	0.0275	7.4736	3.6349
B to Z ↓	0.0129	0.0120	4.1703	2.1868
B to Z ↑	0.0225	0.0205	7.6746	3.6936
	C12T28SOI_LRS_-NAND2X40_P16	**C12T28SOI_LRS_-NAND2X54_P16**	**C12T28SOI_LRS_-NAND2X40_P16**	**C12T28SOI_LRS_-NAND2X54_P16**
A to Z ↓	0.0171	0.0171	0.9950	0.7523
A to Z ↑	0.0227	0.0226	0.9126	0.6870
B to Z ↓	0.0151	0.0152	1.0027	0.7597
B to Z ↑	0.0184	0.0185	0.9196	0.6928

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P16	1.658e-07	7.027e-10
C12T28SOI_LR_NAND2X5_P16	2.603e-07	7.027e-10
C12T28SOI_LR_NAND2X7_P16	3.092e-07	7.027e-10
C12T28SOI_LR_NAND2X10_P16	4.329e-07	9.409e-10
C12T28SOI_LR_NAND2X13_P16	5.600e-07	9.409e-10
C12T28SOI_LR_NAND2X17_P16	6.845e-07	1.179e-09
C12T28SOI_LR_NAND2X20_P16	7.936e-07	1.179e-09
C12T28SOI_LR_NAND2X24_P16	9.342e-07	1.417e-09
C12T28SOI_LR_NAND2X27_P16	1.028e-06	1.417e-09

C12T28SOI_LR_NAND2X42_P16	2.018e-06	1.536e-09
C12T28SOI_LR_NAND2X47_P16	2.233e-06	1.656e-09
C12T28SOI_LR_NAND2X50_P16	2.284e-06	1.656e-09
C12T28SOI_LR_NAND2X58_P16	2.550e-06	1.775e-09
C12T28SOI_LR_NAND2X67_P16	2.815e-06	1.894e-09
C12T28SOI_LRBR0D8_NAND2X7_-P16	3.777e-07	1.296e-09
C12T28SOI_LRBR0D8_NAND2X14_-P16	6.780e-07	1.549e-09
C12T28SOI_LRS_NAND2X40_P16	1.498e-06	1.894e-09
C12T28SOI_LRS_NAND2X54_P16	1.968e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P16	C12T28SOI_LR_-NAND2X5_P16	C12T28SOI_LR_-NAND2X7_P16	C12T28SOI_LR_-NAND2X10_P16
A (output stable)	9.958e-06	1.579e-05	1.898e-05	5.652e-05
B (output stable)	2.707e-05	4.257e-05	5.196e-05	2.747e-04
A to Z	5.144e-04	6.712e-04	7.911e-04	1.462e-03
B to Z	4.122e-04	4.987e-04	5.817e-04	9.034e-04
	C12T28SOI_LR_-NAND2X13_P16	C12T28SOI_LR_-NAND2X17_P16	C12T28SOI_LR_-NAND2X20_P16	C12T28SOI_LR_-NAND2X24_P16
A (output stable)	6.836e-05	8.641e-05	9.749e-05	1.293e-04
B (output stable)	3.132e-04	3.181e-04	3.517e-04	5.317e-04
A to Z	1.761e-03	2.218e-03	2.504e-03	3.108e-03
B to Z	1.065e-03	1.434e-03	1.619e-03	1.883e-03
	C12T28SOI_LR_-NAND2X27_P16	C12T28SOI_LR_-NAND2X42_P16	C12T28SOI_LR_-NAND2X47_P16	C12T28SOI_LR_-NAND2X50_P16
A (output stable)	1.361e-04	2.118e-05	2.126e-05	2.125e-05
B (output stable)	5.667e-04	5.782e-05	5.808e-05	5.793e-05
A to Z	3.389e-03	8.958e-03	9.581e-03	9.817e-03
B to Z	2.045e-03	8.753e-03	9.377e-03	9.611e-03
	C12T28SOI_LR_-NAND2X58_P16	C12T28SOI_LR_-NAND2X67_P16	C12T28SOI_-LRBR0D8_-NAND2X7_P16	C12T28SOI_-LRBR0D8_-NAND2X14_P16
A (output stable)	2.134e-05	2.139e-05	2.458e-05	8.501e-05
B (output stable)	5.804e-05	5.770e-05	6.922e-05	3.969e-04
A to Z	1.115e-02	1.209e-02	8.347e-04	1.855e-03
B to Z	1.094e-02	1.189e-02	5.489e-04	9.463e-04
	C12T28SOI_LRS_-NAND2X40_P16	C12T28SOI_LRS_-NAND2X54_P16		
A (output stable)	2.032e-04	2.627e-04		
B (output stable)	7.944e-04	1.007e-03		
A to Z	5.018e-03	6.620e-03		
B to Z	3.079e-03	4.100e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P16	C12T28SOI_LR_-NAND2X5_P16	C12T28SOI_LR_-NAND2X7_P16	C12T28SOI_LR_-NAND2X10_P16
A (output stable)	2.110e-08	-4.700e-09	-2.200e-08	-1.085e-07
B (output stable)	2.330e-08	-9.100e-09	-2.790e-08	-9.240e-08
A to Z	-1.086e-07	-1.108e-07	-1.590e-07	-6.448e-07

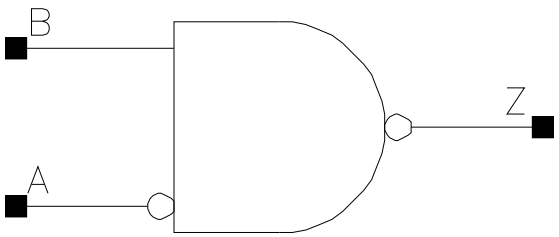
B to Z	4.410e-08	7.470e-08	2.595e-07	4.200e-09
	C12T28SOI_LR_-NAND2X13_P16	C12T28SOI_LR_-NAND2X17_P16	C12T28SOI_LR_-NAND2X20_P16	C12T28SOI_LR_-NAND2X24_P16
A (output stable)	-6.500e-08	-7.590e-08	-1.891e-07	-1.812e-07
B (output stable)	-2.004e-06	-1.832e-06	-2.849e-07	-3.674e-06
A to Z	-9.501e-07	-9.903e-07	-1.525e-06	-1.940e-06
B to Z	-3.435e-07	5.460e-07	1.140e-07	-6.520e-07
	C12T28SOI_LR_-NAND2X27_P16	C12T28SOI_LR_-NAND2X42_P16	C12T28SOI_LR_-NAND2X47_P16	C12T28SOI_LR_-NAND2X50_P16
A (output stable)	-2.516e-07	-1.431e-08	-1.386e-08	-1.392e-08
B (output stable)	-3.444e-06	-2.330e-08	-2.370e-08	-2.290e-08
A to Z	-2.014e-06	-8.460e-07	-8.779e-07	-6.206e-07
B to Z	-4.240e-07	-5.290e-07	-7.320e-07	-9.237e-07
	C12T28SOI_LR_-NAND2X58_P16	C12T28SOI_LR_-NAND2X67_P16	C12T28SOI_-LRBR0D8_-NAND2X7_P16	C12T28SOI_-LRBR0D8_-NAND2X14_P16
A (output stable)	-1.434e-08	-1.364e-08	7.420e-09	2.108e-07
B (output stable)	-2.300e-08	-2.350e-08	-5.000e-10	-7.462e-06
A to Z	-1.102e-06	-5.140e-07	-2.213e-07	-1.061e-06
B to Z	-1.254e-06	-1.199e-06	1.223e-07	-4.269e-07
	C12T28SOI_LRS_-NAND2X40_P16	C12T28SOI_LRS_-NAND2X54_P16		
A (output stable)	-3.533e-07	-4.707e-07		
B (output stable)	-4.569e-06	-6.024e-06		
A to Z	-3.105e-06	-4.580e-06		
B to Z	-5.450e-07	1.184e-06		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X7_P16	1.200	0.544	0.6528
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X40_P16	1.200	2.312	2.7744
X54_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P16	X7_P16	X13_P16	X27_P16
A	0.0008	0.0008	0.0011	0.0020
B	0.0006	0.0008	0.0015	0.0029
	X40_P16	X54_P16		
A	0.0030	0.0039		
B	0.0044	0.0058		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0476	0.0499	10.8579	5.6149
A to Z ↑	0.0365	0.0373	10.9359	5.5103
B to Z ↓	0.0191	0.0156	11.0079	5.6693
B to Z ↑	0.0238	0.0198	11.1055	5.6104
	X13_P16	**X27_P16**	**X13_P16**	**X27_P16**

A to Z ↓	0.0456	0.0439	2.9447	1.4678
A to Z ↑	0.0346	0.0334	2.8154	1.3645
B to Z ↓	0.0146	0.0146	2.9819	1.4879
B to Z ↑	0.0185	0.0182	2.7925	1.3748
	X40_P16	**X54_P16**	**X40_P16**	**X54_P16**
A to Z ↓	0.0446	0.0446	0.9870	0.7479
A to Z ↑	0.0340	0.0340	0.9089	0.6849
B to Z ↓	0.0145	0.0145	0.9971	0.7557
B to Z ↑	0.0179	0.0179	0.9227	0.6956

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P16	2.907e-07	8.218e-10
X7_P16	4.343e-07	8.218e-10
X13_P16	8.552e-07	1.179e-09
X27_P16	1.554e-06	1.775e-09
X40_P16	2.230e-06	2.370e-09
X54_P16	2.905e-06	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	8.490e-04	1.095e-03	1.746e-03	3.318e-03
B (output stable)	2.789e-05	5.249e-05	2.914e-04	5.185e-04
A to Z	1.449e-03	2.010e-03	3.674e-03	7.116e-03
B to Z	4.194e-04	5.768e-04	1.031e-03	2.040e-03
	X40_P16	X54_P16		
A (output stable)	5.136e-03	6.774e-03		
B (output stable)	7.647e-04	9.931e-04		
A to Z	1.070e-02	1.417e-02		
B to Z	2.920e-03	3.844e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

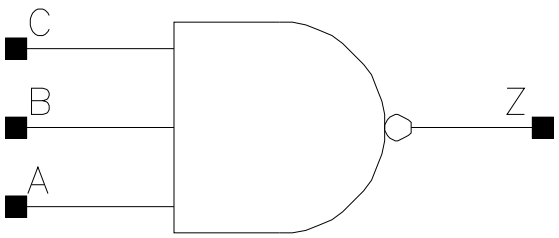
Pin Cycle (vdds)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	-1.060e-07	-8.780e-08	-2.790e-07	-5.356e-07
B (output stable)	2.480e-08	-2.710e-08	-1.599e-07	-2.377e-06
A to Z	-9.119e-08	-1.750e-08	-3.015e-07	-4.910e-07
B to Z	8.100e-09	5.220e-08	3.214e-07	4.720e-07
	X40_P16	X54_P16		
A (output stable)	-2.720e-07	-1.043e-06		
B (output stable)	-3.784e-06	-5.820e-06		
A to Z	-9.850e-07	-2.340e-07		
B to Z	-4.880e-07	-3.127e-06		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P16	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P16	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P16	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P16	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P16	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P16	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P16	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P16	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P16	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P16	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P16	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P16	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P16	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P16	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P16	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A	0.0007	0.0008	0.0013	0.0016
B	0.0007	0.0009	0.0013	0.0016
C	0.0006	0.0008	0.0012	0.0015
	C12T28SOI_LR_-NAND3X15_P16	C12T28SOI_LR_-NAND3X18_P16	C12T28SOI_LR_-NAND3X21_P16	C12T28SOI_LR_-NAND3X24_P16
A	0.0021	0.0024	0.0029	0.0032
B	0.0020	0.0023	0.0028	0.0031
C	0.0019	0.0021	0.0026	0.0029
	C12T28SOI_LR_-NAND3X35_P16	C12T28SOI_LR_-NAND3X47_P16	C12T28SOI_-LRBR0P6_-NAND3X6_P16	C12T28SOI_-LRBR0P6_-NAND3X12_P16
A	0.0048	0.0064	0.0008	0.0017
B	0.0046	0.0061	0.0009	0.0016
C	0.0044	0.0058	0.0008	0.0015
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	C12T28SOI_-LRBR0P6_-NAND3X24_P16	C12T28SOI_-LRBR0P6_-NAND3X35_P16	C12T28SOI_-LRBR0P6_-NAND3X47_P16
A	0.0024	0.0032	0.0048	0.0064
B	0.0023	0.0031	0.0045	0.0060
C	0.0021	0.0028	0.0042	0.0056
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16			
A	0.0025			
B	0.0024			
C	0.0022			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16
A to Z ↓	0.0280	0.0249	11.3588	7.9397
A to Z ↑	0.0318	0.0287	7.9057	5.3644
B to Z ↓	0.0290	0.0254	11.3853	7.9514
B to Z ↑	0.0306	0.0273	7.9118	5.3733
C to Z ↓	0.0248	0.0219	11.3982	7.9769
C to Z ↑	0.0266	0.0236	7.9145	5.3990

	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A to Z ↓	0.0279	0.0257	5.4805	4.1749
A to Z ↑	0.0304	0.0284	3.6856	2.7318
B to Z ↓	0.0261	0.0241	5.4867	4.1790
B to Z ↑	0.0278	0.0259	3.6891	2.7346
C to Z ↓	0.0222	0.0206	5.5073	4.1932
C to Z ↑	0.0237	0.0219	3.6798	2.7173
	C12T28SOI_LR_-NAND3X15_P16	**C12T28SOI_LR_-NAND3X18_P16**	**C12T28SOI_LR_-NAND3X15_P16**	**C12T28SOI_LR_-NAND3X18_P16**
A to Z ↓	0.0254	0.0246	3.4250	2.9011
A to Z ↑	0.0281	0.0271	2.1955	1.8160
B to Z ↓	0.0244	0.0237	3.4297	2.9057
B to Z ↑	0.0257	0.0249	2.1991	1.8192
C to Z ↓	0.0214	0.0204	3.4442	2.9143
C to Z ↑	0.0222	0.0211	2.2116	1.8300
	C12T28SOI_LR_-NAND3X21_P16	**C12T28SOI_LR_-NAND3X24_P16**	**C12T28SOI_LR_-NAND3X21_P16**	**C12T28SOI_LR_-NAND3X24_P16**
A to Z ↓	0.0259	0.0251	2.4603	2.1778
A to Z ↑	0.0281	0.0275	1.5700	1.3715
B to Z ↓	0.0244	0.0238	2.4634	2.1813
B to Z ↑	0.0258	0.0251	1.5719	1.3731
C to Z ↓	0.0210	0.0204	2.4710	2.1866
C to Z ↑	0.0219	0.0212	1.5729	1.3728
	C12T28SOI_LR_-NAND3X35_P16	**C12T28SOI_LR_-NAND3X47_P16**	**C12T28SOI_LR_-NAND3X35_P16**	**C12T28SOI_LR_-NAND3X47_P16**
A to Z ↓	0.0246	0.0248	1.4825	1.1257
A to Z ↑	0.0270	0.0271	0.9164	0.6913
B to Z ↓	0.0235	0.0235	1.4858	1.1281
B to Z ↑	0.0246	0.0246	0.9165	0.6897
C to Z ↓	0.0203	0.0204	1.4901	1.1309
C to Z ↑	0.0208	0.0208	0.9202	0.6925
	C12T28SOI_-LRBR0P6_-NAND3X6_P16	**C12T28SOI_-LRBR0P6_-NAND3X12_P16**	**C12T28SOI_-LRBR0P6_-NAND3X6_P16**	**C12T28SOI_-LRBR0P6_-NAND3X12_P16**
A to Z ↓	0.0199	0.0208	5.2829	2.7698
A to Z ↑	0.0397	0.0396	8.6933	4.4187
B to Z ↓	0.0200	0.0188	5.2991	2.7769
B to Z ↑	0.0361	0.0340	8.7118	4.4259
C to Z ↓	0.0158	0.0143	5.3375	2.7977
C to Z ↑	0.0281	0.0254	8.7564	4.4368
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	**C12T28SOI_-LRBR0P6_-NAND3X24_P16**	**C12T28SOI_-LRBR0P6_-NAND3X18_P16**	**C12T28SOI_-LRBR0P6_-NAND3X24_P16**
A to Z ↓	0.0198	0.0202	1.9218	1.4401
A to Z ↑	0.0377	0.0382	2.9396	2.2171
B to Z ↓	0.0183	0.0183	1.9294	1.4464
B to Z ↑	0.0324	0.0328	2.9466	2.2210
C to Z ↓	0.0145	0.0141	1.9422	1.4561
C to Z ↑	0.0247	0.0245	2.9655	2.2249
	C12T28SOI_-LRBR0P6_-NAND3X35_P16	**C12T28SOI_-LRBR0P6_-NAND3X47_P16**	**C12T28SOI_-LRBR0P6_-NAND3X35_P16**	**C12T28SOI_-LRBR0P6_-NAND3X47_P16**

A to Z ↓	0.0198	0.0200	0.9823	0.7467
A to Z ↑	0.0380	0.0380	1.5125	1.1413
B to Z ↓	0.0182	0.0183	0.9867	0.7502
B to Z ↑	0.0325	0.0325	1.5143	1.1422
C to Z ↓	0.0141	0.0144	0.9941	0.7552
C to Z ↑	0.0242	0.0245	1.5287	1.1468
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P16**	
A to Z ↓	0.0203		1.8095	
A to Z ↑	0.0374		2.7159	
B to Z ↓	0.0181		1.8156	
B to Z ↑	0.0320		2.7201	
C to Z ↓	0.0135		1.8306	
C to Z ↑	0.0235		2.7048	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P16	2.117e-07	9.409e-10
C12T28SOI_LR_NAND3X6_P16	2.955e-07	9.409e-10
C12T28SOI_LR_NAND3X9_P16	4.076e-07	1.298e-09
C12T28SOI_LR_NAND3X12_P16	5.244e-07	1.298e-09
C12T28SOI_LR_NAND3X15_P16	5.944e-07	1.536e-09
C12T28SOI_LR_NAND3X18_P16	6.901e-07	1.536e-09
C12T28SOI_LR_NAND3X21_P16	8.633e-07	2.013e-09
C12T28SOI_LR_NAND3X24_P16	9.500e-07	2.013e-09
C12T28SOI_LR_NAND3X35_P16	1.376e-06	2.727e-09
C12T28SOI_LR_NAND3X47_P16	1.799e-06	3.442e-09
C12T28SOI_LRBR0P6_NAND3X6_-P16	3.900e-07	1.615e-09
C12T28SOI_LRBR0P6_NAND3X12_-P16	7.087e-07	2.005e-09
C12T28SOI_LRBR0P6_NAND3X18_-P16	9.351e-07	2.266e-09
C12T28SOI_LRBR0P6_NAND3X24_-P16	1.312e-06	2.786e-09
C12T28SOI_LRBR0P6_NAND3X35_-P16	1.919e-06	3.566e-09
C12T28SOI_LRBR0P6_NAND3X47_-P16	2.522e-06	4.346e-09
C12T28SOIDV_LRBR0P6_-NAND3X18_P16	1.135e-06	1.874e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A (output stable)	1.156e-05	1.686e-05	4.117e-05	4.964e-05
B (output stable)	5.793e-05	7.358e-05	1.620e-04	1.930e-04
C (output stable)	1.810e-04	2.224e-04	3.324e-04	3.934e-04
A to Z	1.213e-03	1.473e-03	2.447e-03	2.868e-03
B to Z	1.089e-03	1.280e-03	1.950e-03	2.276e-03
C to Z	8.083e-04	9.404e-04	1.376e-03	1.589e-03

	C12T28SOI_LR_-NAND3X15_P16	C12T28SOI_LR_-NAND3X18_P16	C12T28SOI_LR_-NAND3X21_P16	C12T28SOI_LR_-NAND3X24_P16
A (output stable)	5.908e-05	6.517e-05	8.672e-05	9.484e-05
B (output stable)	2.224e-04	2.555e-04	3.280e-04	3.615e-04
C (output stable)	4.320e-04	4.948e-04	6.356e-04	6.844e-04
A to Z	3.451e-03	3.893e-03	4.918e-03	5.351e-03
B to Z	2.751e-03	3.100e-03	3.901e-03	4.241e-03
C to Z	1.983e-03	2.180e-03	2.737e-03	2.955e-03
	C12T28SOI_LR_-NAND3X35_P16	C12T28SOI_LR_-NAND3X47_P16	C12T28SOI_-LRBR0P6_-NAND3X6_P16	C12T28SOI_-LRBR0P6_-NAND3X12_P16
A (output stable)	1.276e-04	1.709e-04	2.360e-05	6.986e-05
B (output stable)	5.050e-04	6.617e-04	1.077e-04	2.827e-04
C (output stable)	1.018e-03	1.302e-03	3.052e-04	5.677e-04
A to Z	7.710e-03	1.019e-02	1.607e-03	3.183e-03
B to Z	6.086e-03	8.020e-03	1.315e-03	2.322e-03
C to Z	4.179e-03	5.575e-03	8.154e-04	1.292e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	C12T28SOI_-LRBR0P6_-NAND3X24_P16	C12T28SOI_-LRBR0P6_-NAND3X35_P16	C12T28SOI_-LRBR0P6_-NAND3X47_P16
A (output stable)	9.052e-05	1.361e-04	1.823e-04	2.381e-04
B (output stable)	3.675e-04	5.237e-04	7.369e-04	9.513e-04
C (output stable)	7.088e-04	1.018e-03	1.528e-03	1.967e-03
A to Z	4.313e-03	5.929e-03	8.579e-03	1.125e-02
B to Z	3.131e-03	4.302e-03	6.190e-03	8.188e-03
C to Z	1.815e-03	2.393e-03	3.392e-03	4.510e-03
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16			
A (output stable)	1.021e-04			
B (output stable)	4.279e-04			
C (output stable)	8.484e-04			
A to Z	4.660e-03			
B to Z	3.380e-03			
C to Z	1.826e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A (output stable)	8.267e-09	-6.200e-09	1.801e-07	-1.111e-07
B (output stable)	1.944e-08	-8.150e-09	-3.248e-07	-1.210e-07
C (output stable)	-2.783e-08	-5.843e-08	-2.116e-06	-1.632e-07
A to Z	4.880e-08	-1.880e-07	4.000e-09	-1.020e-07
B to Z	2.590e-08	2.950e-07	2.420e-07	-5.700e-07
C to Z	1.515e-07	2.000e-08	4.000e-08	1.170e-07
	C12T28SOI_LR_-NAND3X15_P16	C12T28SOI_LR_-NAND3X18_P16	C12T28SOI_LR_-NAND3X21_P16	C12T28SOI_LR_-NAND3X24_P16
A (output stable)	5.103e-08	-9.267e-09	1.786e-07	9.907e-08
B (output stable)	-4.873e-07	-5.369e-07	-7.947e-07	-8.177e-07
C (output stable)	-1.955e-06	-1.901e-06	-3.868e-06	-3.548e-06
A to Z	1.550e-07	5.700e-08	-3.360e-07	-1.270e-07
B to Z	-6.930e-07	-9.570e-07	-8.050e-07	-1.285e-06

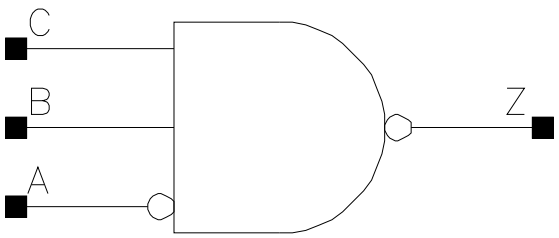
C to Z	1.060e-07	6.600e-08	1.600e-08	-1.115e-06
	C12T28SOI_LR_-NAND3X35_P16	C12T28SOI_LR_-NAND3X47_P16	C12T28SOI_-LRBR0P6_-NAND3X6_P16	C12T28SOI_-LRBR0P6_-NAND3X12_P16
A (output stable)	1.342e-07	1.645e-07	3.727e-07	8.294e-07
B (output stable)	-1.383e-06	-1.761e-06	-7.660e-07	-2.722e-06
C (output stable)	-5.499e-06	-6.738e-06	-4.728e-06	-6.356e-06
A to Z	-2.300e-08	3.040e-07	-3.229e-07	-3.900e-08
B to Z	-1.861e-06	-2.293e-06	2.086e-07	-8.990e-07
C to Z	-2.720e-07	-3.110e-07	-7.220e-08	2.730e-07
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	C12T28SOI_-LRBR0P6_-NAND3X24_P16	C12T28SOI_-LRBR0P6_-NAND3X35_P16	C12T28SOI_-LRBR0P6_-NAND3X47_P16
A (output stable)	-9.940e-08	9.833e-07	4.233e-07	6.611e-07
B (output stable)	-1.197e-07	-3.202e-06	-1.379e-06	-1.987e-06
C (output stable)	-2.359e-07	-7.986e-06	-6.722e-06	-9.292e-06
A to Z	-5.720e-07	-2.730e-07	-6.660e-07	4.280e-07
B to Z	-1.582e-06	-1.812e-06	-2.541e-06	-3.128e-06
C to Z	2.930e-07	-5.120e-07	-7.170e-07	-9.670e-07
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16			
A (output stable)	-9.367e-08			
B (output stable)	-1.664e-07			
C (output stable)	-2.561e-07			
A to Z	-3.740e-07			
B to Z	-1.957e-06			
C to Z	-2.590e-07			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.816	0.9792
X12_P16	1.200	1.224	1.4688
X18_P16	1.200	1.496	1.7952
X24_P16	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0008	0.0011	0.0011	0.0020
B	0.0008	0.0016	0.0023	0.0031
C	0.0008	0.0015	0.0021	0.0029

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X12_P16**	**X6_P16**	**X12_P16**
A to Z ↓	0.0569	0.0538	8.0848	4.2282
A to Z ↑	0.0405	0.0382	5.3533	2.6840
B to Z ↓	0.0220	0.0231	8.1109	4.2398
B to Z ↑	0.0249	0.0248	5.3837	2.7052
C to Z ↓	0.0214	0.0194	8.1313	4.2573
C to Z ↑	0.0224	0.0207	5.4082	2.7215
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0616	0.0517	2.9096	2.1877

A to Z ↑	0.0437	0.0361	1.8059	1.3517
B to Z ↓	0.0236	0.0229	2.9156	2.1937
B to Z ↑	0.0248	0.0243	1.8196	1.3659
C to Z ↓	0.0205	0.0192	2.9247	2.2016
C to Z ↑	0.0212	0.0202	1.8301	1.3746

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P16	3.890e-07	1.060e-09
X12_P16	7.741e-07	1.417e-09
X18_P16	9.273e-07	1.655e-09
X24_P16	1.504e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	1.069e-03	1.848e-03	2.551e-03	3.376e-03
B (output stable)	5.870e-05	1.243e-04	1.933e-04	2.802e-04
C (output stable)	1.230e-04	4.465e-04	5.494e-04	8.409e-04
A to Z	2.450e-03	4.808e-03	6.943e-03	9.086e-03
B to Z	1.045e-03	2.086e-03	3.100e-03	3.945e-03
C to Z	8.256e-04	1.388e-03	2.179e-03	2.594e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

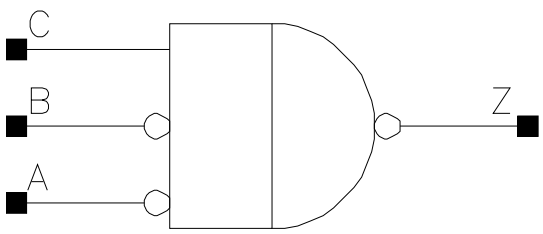
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	-9.583e-08	-1.505e-07	-3.114e-07	-1.542e-07
B (output stable)	-1.594e-08	-1.907e-07	-2.167e-07	-1.324e-06
C (output stable)	-2.163e-08	-2.012e-06	-2.479e-07	-3.865e-06
A to Z	-1.419e-07	-3.381e-07	-4.750e-07	-3.500e-08
B to Z	5.460e-08	-5.350e-07	-1.086e-06	-1.168e-06
C to Z	7.400e-08	1.270e-07	1.330e-07	2.030e-07

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	0.816	0.9792
X13_P16	1.200	1.088	1.3056
X20_P16	1.200	1.632	1.9584
X27_P16	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P16	X13_P16	X20_P16	X27_P16
A	0.0010	0.0010	0.0019	0.0018
B	0.0011	0.0010	0.0020	0.0018
C	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	**X13_P16**	**X7_P16**	**X13_P16**
A to Z ↓	0.0569	0.0705	5.3851	2.8595
A to Z ↑	0.0332	0.0381	5.3184	2.6723
B to Z ↓	0.0551	0.0689	5.3800	2.8556
B to Z ↑	0.0316	0.0366	5.3191	2.6718
C to Z ↓	0.0154	0.0145	5.4179	2.8645
C to Z ↑	0.0197	0.0184	5.4074	2.7229
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0631	0.0701	1.9450	1.4698
A to Z ↑	0.0353	0.0422	1.7987	1.3507
B to Z ↓	0.0576	0.0659	1.9387	1.4683

B to Z ↑	0.0328	0.0403	1.7970	1.3503
C to Z ↓	0.0158	0.0152	1.9531	1.4748
C to Z ↑	0.0194	0.0188	1.8325	1.3751

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X7_P16	6.047e-07	1.060e-09
X13_P16	8.384e-07	1.298e-09
X20_P16	1.284e-06	1.775e-09
X27_P16	1.432e-06	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	6.101e-04	8.250e-04	1.406e-03	1.661e-03
B (output stable)	4.852e-04	7.041e-04	1.020e-03	1.315e-03
C (output stable)	5.575e-05	3.325e-04	3.452e-04	4.564e-04
A to Z	2.672e-03	4.401e-03	7.004e-03	8.667e-03
B to Z	2.376e-03	4.118e-03	6.046e-03	7.873e-03
C to Z	5.969e-04	1.029e-03	1.743e-03	2.236e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

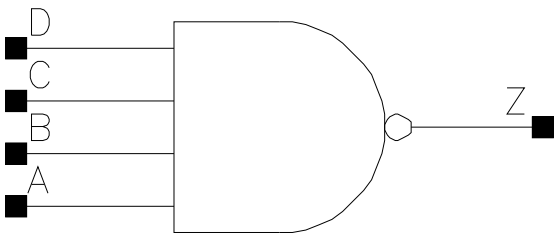
Pin Cycle (vdds)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	-2.298e-06	-2.328e-06	-1.008e-05	-9.861e-06
B (output stable)	9.234e-06	9.298e-06	1.904e-05	1.801e-05
C (output stable)	-2.730e-07	-3.757e-07	-8.705e-07	-9.542e-07
A to Z	-1.513e-06	-1.675e-06	-7.596e-06	-7.475e-06
B to Z	-3.177e-07	-3.845e-07	-7.690e-07	-5.860e-07
C to Z	1.372e-07	1.498e-07	1.079e-06	-2.830e-07

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0007	0.0007	0.0008	0.0010
B	0.0007	0.0007	0.0009	0.0011
C	0.0007	0.0007	0.0009	0.0010
D	0.0007	0.0007	0.0009	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0952	0.0915	3.0527	1.5259
A to Z ↑	0.0687	0.0731	5.4073	2.6953
B to Z ↓	0.0968	0.0944	3.0538	1.5267
B to Z ↑	0.0664	0.0726	5.4158	2.6957
C to Z ↓	0.0951	0.0894	3.0544	1.5273
C to Z ↑	0.0706	0.0765	5.4140	2.6927

D to Z ↓	0.0971	0.0907	3.0561	1.5248
D to Z ↑	0.0693	0.0738	5.4046	2.6908
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0955	0.0862	1.0544	0.7899
A to Z ↑	0.0702	0.0679	1.8106	1.3584
B to Z ↓	0.0974	0.0876	1.0544	0.7898
B to Z ↑	0.0687	0.0659	1.8115	1.3598
C to Z ↓	0.0868	0.0788	1.0529	0.7898
C to Z ↑	0.0714	0.0689	1.8107	1.3580
D to Z ↓	0.0882	0.0802	1.0538	0.7895
D to Z ↑	0.0689	0.0666	1.8101	1.3577

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	8.003e-07	1.417e-09
X17_P16	1.225e-06	1.655e-09
X25_P16	1.730e-06	2.013e-09
X33_P16	2.193e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	4.295e-04	5.394e-04	7.979e-04	9.251e-04
B (output stable)	3.967e-04	5.173e-04	7.500e-04	8.632e-04
C (output stable)	4.254e-04	5.229e-04	7.877e-04	8.928e-04
D (output stable)	3.906e-04	4.797e-04	6.940e-04	7.839e-04
A to Z	3.144e-03	4.701e-03	7.330e-03	8.850e-03
B to Z	3.037e-03	4.614e-03	7.187e-03	8.647e-03
C to Z	3.223e-03	4.621e-03	6.818e-03	8.219e-03
D to Z	3.128e-03	4.508e-03	6.657e-03	8.019e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

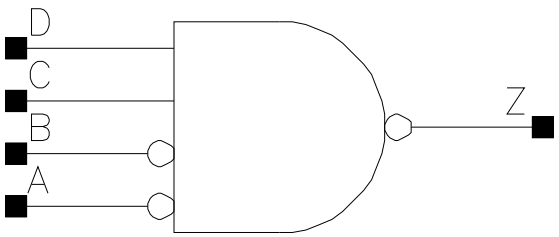
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	-7.819e-07	-1.247e-06	-9.354e-06	-8.312e-06
B (output stable)	-7.932e-07	-1.197e-06	-7.932e-06	-8.047e-06
C (output stable)	3.920e-06	8.022e-06	2.071e-05	2.553e-05
D (output stable)	2.279e-06	5.326e-06	7.782e-06	1.105e-05
A to Z	-1.028e-06	-1.577e-06	-6.132e-06	-6.874e-06
B to Z	-9.315e-07	-1.389e-06	-6.206e-06	-6.760e-06
C to Z	-3.557e-07	-5.145e-07	-4.294e-07	-8.816e-07
D to Z	-1.005e-07	-1.582e-07	-6.841e-07	-5.651e-07

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X12_P16	1.200	1.496	1.7952
X18_P16	1.200	2.040	2.4480
X24_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0010	0.0010	0.0019	0.0018
B	0.0010	0.0014	0.0019	0.0018
C	0.0008	0.0016	0.0023	0.0031
D	0.0008	0.0015	0.0021	0.0030

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X12_P16	X6_P16	X12_P16
A to Z ↓	0.0606	0.0822	8.2998	4.2442
A to Z ↑	0.0355	0.0428	5.3145	2.6777
B to Z ↓	0.0577	0.0792	8.3066	4.2431
B to Z ↑	0.0328	0.0409	5.3146	2.6737
C to Z ↓	0.0221	0.0231	8.3194	4.2366
C to Z ↑	0.0250	0.0248	5.6539	2.7048

D to Z ↓	0.0211	0.0193	8.3486	4.2522
D to Z ↑	0.0223	0.0206	5.6848	2.7211
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0701	0.0791	2.9029	2.1984
A to Z ↑	0.0380	0.0483	1.8004	1.3537
B to Z ↓	0.0649	0.0748	2.9033	2.1998
B to Z ↑	0.0355	0.0461	1.7978	1.3511
C to Z ↓	0.0231	0.0237	2.9048	2.1962
C to Z ↑	0.0246	0.0249	1.8254	1.3649
D to Z ↓	0.0203	0.0205	2.9147	2.2037
D to Z ↑	0.0211	0.0211	1.8566	1.3743

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P16	4.691e-07	1.179e-09
X12_P16	7.499e-07	1.655e-09
X18_P16	1.126e-06	2.132e-09
X24_P16	1.200e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	6.917e-04	1.178e-03	1.766e-03	2.145e-03
B (output stable)	5.372e-04	9.636e-04	1.319e-03	1.720e-03
C (output stable)	7.176e-05	1.807e-04	2.695e-04	3.577e-04
D (output stable)	1.369e-04	4.524e-04	5.445e-04	7.877e-04
A to Z	2.875e-03	5.516e-03	8.145e-03	1.069e-02
B to Z	2.572e-03	5.114e-03	7.251e-03	9.871e-03
C to Z	1.011e-03	2.080e-03	3.006e-03	4.194e-03
D to Z	7.870e-04	1.378e-03	2.139e-03	2.888e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

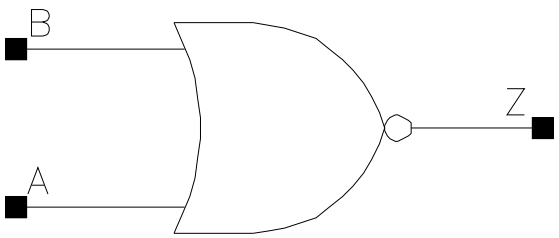
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	-2.202e-06	-6.826e-06	-9.740e-06	-9.827e-06
B (output stable)	8.366e-06	1.113e-05	2.048e-05	1.953e-05
C (output stable)	-7.759e-08	-5.248e-07	-9.025e-07	-1.048e-06
D (output stable)	-1.529e-07	-2.386e-06	-2.297e-06	-4.769e-06
A to Z	-1.268e-06	-5.457e-06	-7.760e-06	-7.619e-06
B to Z	-1.286e-07	-4.224e-07	-8.620e-07	-5.910e-07
C to Z	-2.239e-07	-6.130e-07	-1.073e-06	-1.200e-06
D to Z	3.840e-08	1.200e-07	2.160e-07	2.210e-07

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.408	0.4896
X5_P16	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X10_P16	1.200	0.680	0.8160
X14_P16	1.200	0.680	0.8160
X17_P16	1.200	0.952	1.1424
X21_P16	1.200	0.952	1.1424
X24_P16	1.200	1.224	1.4688
X27_P16	1.200	1.224	1.4688
X34_P16	1.200	1.496	1.7952
X40_P16	1.200	1.360	1.6320
X41_P16	1.200	1.768	2.1216
X49_P16	1.200	1.496	1.7952
X53_P16	1.200	1.904	2.2848
X55_P16	1.200	2.312	2.7744
X57_P16	1.200	1.904	2.2848
X65_P16	1.200	2.040	2.4480
X84_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P16	X5_P16	X7_P16	X10_P16
A	0.0006	0.0007	0.0008	0.0014
B	0.0005	0.0006	0.0008	0.0012
	X14_P16	X17_P16	X21_P16	X24_P16

A	0.0017	0.0022	0.0025	0.0029
B	0.0015	0.0019	0.0023	0.0027
	X27_P16	X34_P16	X40_P16	X41_P16
A	0.0032	0.0041	0.0009	0.0050
B	0.0030	0.0037	0.0010	0.0045
	X49_P16	X53_P16	X55_P16	X57_P16
A	0.0010	0.0010	0.0066	0.0010
B	0.0010	0.0009	0.0060	0.0009
	X65_P16	X84_P16		
A	0.0010	0.0012		
B	0.0009	0.0010		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X5_P16**	**X3_P16**	**X5_P16**
A to Z ↓	0.0161	0.0150	5.8063	4.1493
A to Z ↑	0.0324	0.0297	23.7645	16.9928
B to Z ↓	0.0147	0.0132	5.9215	4.1819
B to Z ↑	0.0303	0.0270	23.8265	17.0394
	X7_P16	**X10_P16**	**X7_P16**	**X10_P16**
A to Z ↓	0.0144	0.0151	3.0122	1.9844
A to Z ↑	0.0280	0.0319	11.8480	7.9539
B to Z ↓	0.0125	0.0119	3.0483	2.0032
B to Z ↑	0.0250	0.0236	11.8851	7.9785
	X14_P16	**X17_P16**	**X14_P16**	**X17_P16**
A to Z ↓	0.0146	0.0150	1.4944	1.2092
A to Z ↑	0.0298	0.0302	5.8336	4.7352
B to Z ↓	0.0114	0.0123	1.5098	1.2203
B to Z ↑	0.0222	0.0240	5.8542	4.7463
	X21_P16	**X24_P16**	**X21_P16**	**X24_P16**
A to Z ↓	0.0148	0.0147	1.0234	0.8774
A to Z ↑	0.0292	0.0296	3.9111	3.4110
B to Z ↓	0.0122	0.0118	1.0321	0.8861
B to Z ↑	0.0232	0.0230	3.9238	3.4208
	X27_P16	**X34_P16**	**X27_P16**	**X34_P16**
A to Z ↓	0.0146	0.0150	0.7741	0.6256
A to Z ↑	0.0289	0.0292	2.9777	2.3779
B to Z ↓	0.0117	0.0121	0.7823	0.6316
B to Z ↑	0.0224	0.0231	2.9916	2.3842
	X40_P16	**X41_P16**	**X40_P16**	**X41_P16**
A to Z ↓	0.0553	0.0148	0.6399	0.5215
A to Z ↑	0.0858	0.0291	1.1153	1.9722
B to Z ↓	0.0535	0.0118	0.6404	0.5270
B to Z ↑	0.0844	0.0223	1.1159	1.9785
	X49_P16	**X53_P16**	**X49_P16**	**X53_P16**
A to Z ↓	0.0583	0.0599	0.5342	0.4904
A to Z ↑	0.0884	0.1027	0.9288	0.8592
B to Z ↓	0.0564	0.0581	0.5338	0.4897
B to Z ↑	0.0868	0.1001	0.9277	0.8600
	X55_P16	**X57_P16**	**X55_P16**	**X57_P16**
A to Z ↓	0.0149	0.0602	0.3941	0.4596
A to Z ↑	0.0291	0.1027	1.4836	0.7968

B to Z ↓	0.0119	0.0584	0.3988	0.4592
B to Z ↑	0.0224	0.1002	1.4885	0.7975
	X65_P16	**X84_P16**	**X65_P16**	**X84_P16**
A to Z ↓	0.0619	0.0645	0.4042	0.3214
A to Z ↑	0.1039	0.1036	0.6986	0.5525
B to Z ↓	0.0601	0.0629	0.4033	0.3213
B to Z ↑	0.1014	0.1018	0.6979	0.5526

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P16	1.515e-07	7.027e-10
X5_P16	2.086e-07	7.027e-10
X7_P16	2.823e-07	7.027e-10
X10_P16	3.971e-07	9.409e-10
X14_P16	5.142e-07	9.409e-10
X17_P16	6.308e-07	1.179e-09
X21_P16	7.306e-07	1.179e-09
X24_P16	8.594e-07	1.417e-09
X27_P16	9.479e-07	1.417e-09
X34_P16	1.165e-06	1.655e-09
X40_P16	1.552e-06	1.536e-09
X41_P16	1.383e-06	1.894e-09
X49_P16	1.697e-06	1.655e-09
X53_P16	2.161e-06	2.013e-09
X55_P16	1.818e-06	2.370e-09
X57_P16	2.233e-06	2.013e-09
X65_P16	2.377e-06	2.132e-09
X84_P16	2.687e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	2.231e-05	3.005e-05	4.250e-05	1.231e-04
B (output stable)	3.362e-06	4.030e-06	5.712e-06	4.740e-05
A to Z	5.455e-04	6.615e-04	8.660e-04	1.566e-03
B to Z	3.908e-04	4.449e-04	5.569e-04	7.648e-04
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	1.466e-04	1.757e-04	2.023e-04	2.422e-04
B (output stable)	5.340e-05	6.319e-05	6.660e-05	7.178e-05
A to Z	1.915e-03	2.414e-03	2.768e-03	3.265e-03
B to Z	9.334e-04	1.329e-03	1.502e-03	1.699e-03
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	2.641e-04	3.229e-04	4.293e-05	4.133e-04
B (output stable)	7.546e-05	8.602e-05	5.733e-06	1.267e-04
A to Z	3.598e-03	4.557e-03	8.713e-03	5.471e-03
B to Z	1.848e-03	2.484e-03	8.436e-03	2.768e-03
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	4.306e-05	4.354e-05	5.428e-04	4.355e-05
B (output stable)	5.690e-06	5.719e-06	1.646e-04	5.720e-06
A to Z	9.766e-03	1.213e-02	7.231e-03	1.237e-02
B to Z	9.487e-03	1.182e-02	3.691e-03	1.206e-02
	X65_P16	X84_P16		

A (output stable)	4.362e-05	4.455e-05		
B (output stable)	5.801e-06	6.487e-06		
A to Z	1.328e-02	1.563e-02		
B to Z	1.298e-02	1.526e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

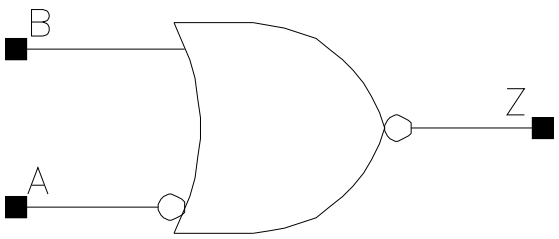
Pin Cycle (vdds)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	-1.603e-06	-2.009e-06	-2.711e-06	-1.054e-05
B (output stable)	9.947e-06	1.333e-05	1.799e-05	6.487e-05
A to Z	-6.090e-07	-9.982e-07	-1.605e-06	-6.203e-06
B to Z	5.240e-08	-1.529e-07	1.310e-07	-1.157e-07
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	-1.244e-05	-9.482e-06	-1.090e-05	-1.790e-05
B (output stable)	8.030e-05	5.877e-05	6.745e-05	1.085e-04
A to Z	-7.775e-06	-5.701e-06	-6.795e-06	-1.019e-05
B to Z	-3.262e-07	-7.770e-08	1.420e-08	-4.592e-07
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	-1.945e-05	-1.686e-05	-2.698e-06	-2.726e-05
B (output stable)	1.224e-04	1.024e-04	1.787e-05	1.643e-04
A to Z	-1.135e-05	-1.014e-05	-2.009e-06	-1.561e-05
B to Z	-1.577e-07	-1.170e-07	-4.400e-07	-2.100e-07
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	-2.696e-06	-2.667e-06	-3.429e-05	-2.667e-06
B (output stable)	1.779e-05	1.906e-05	2.060e-04	1.906e-05
A to Z	-1.911e-06	-2.943e-06	-1.915e-05	-2.267e-06
B to Z	-4.947e-07	-1.368e-06	-1.105e-06	-1.426e-06
	X65_P16	X84_P16		
A (output stable)	-2.665e-06	-2.725e-06		
B (output stable)	1.906e-05	1.952e-05		
A to Z	-2.919e-06	-2.753e-06		
B to Z	-1.253e-06	-1.383e-06		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X7_P16	1.200	0.680	0.8160
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X41_P16	1.200	2.312	2.7744
X55_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X7_P16	X13_P16
A	0.0008	0.0008	0.0008	0.0011
B	0.0005	0.0008	0.0008	0.0015
	X27_P16	X41_P16	X55_P16	
A	0.0021	0.0031	0.0040	
B	0.0030	0.0044	0.0059	

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0448	0.0491	5.7481	3.6647
A to Z ↑	0.0436	0.0425	23.6406	11.8129
B to Z ↓	0.0151	0.0142	5.9201	3.8159
B to Z ↑	0.0307	0.0252	23.8290	11.9054

	X7_P16	X13_P16	X7_P16	X13_P16
A to Z ↓	0.0495	0.0438	2.8772	1.5666
A to Z ↑	0.0464	0.0427	11.6271	6.1110
B to Z ↓	0.0129	0.0119	2.8996	1.5706
B to Z ↑	0.0264	0.0239	11.6769	6.1461
	X27_P16	**X41_P16**	**X27_P16**	**X41_P16**
A to Z ↓	0.0422	0.0430	0.7576	0.5129
A to Z ↑	0.0409	0.0413	2.9421	1.9700
B to Z ↓	0.0118	0.0117	0.7804	0.5273
B to Z ↑	0.0229	0.0226	2.9591	1.9801
	X55_P16		**X55_P16**	
A to Z ↓	0.0427		0.3880	
A to Z ↑	0.0411		1.4829	
B to Z ↓	0.0118		0.3995	
B to Z ↑	0.0225		1.4909	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P16	2.765e-07	8.218e-10
X6_P16	3.738e-07	8.218e-10
X7_P16	4.592e-07	9.409e-10
X13_P16	7.993e-07	1.179e-09
X27_P16	1.468e-06	1.775e-09
X41_P16	2.110e-06	2.370e-09
X55_P16	2.751e-06	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	8.398e-04	1.068e-03	1.141e-03	1.811e-03
B (output stable)	6.377e-06	1.613e-05	1.429e-05	2.978e-05
A to Z	1.451e-03	2.008e-03	2.348e-03	3.908e-03
B to Z	4.024e-04	5.569e-04	6.629e-04	1.039e-03
	X27_P16	X41_P16	X55_P16	
A (output stable)	3.511e-03	5.341e-03	7.051e-03	
B (output stable)	6.484e-05	9.638e-05	1.355e-04	
A to Z	7.708e-03	1.147e-02	1.521e-02	
B to Z	1.989e-03	2.890e-03	3.804e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

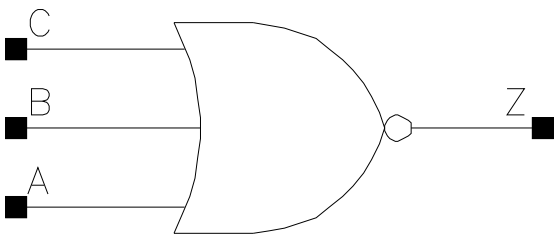
Pin Cycle (vdds)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	-1.658e-06	-2.541e-06	-6.551e-06	-1.106e-05
B (output stable)	3.488e-06	9.051e-06	8.385e-06	1.372e-05
A to Z	-8.233e-07	-1.191e-06	-3.781e-06	-6.075e-06
B to Z	-1.130e-07	7.190e-08	3.740e-08	-3.006e-07
	X27_P16	X41_P16	X55_P16	
A (output stable)	-1.871e-05	-2.581e-05	-3.271e-05	
B (output stable)	2.333e-05	3.424e-05	4.477e-05	
A to Z	-1.105e-05	-1.487e-05	-1.861e-05	
B to Z	-5.558e-07	-9.584e-07	-1.165e-06	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X9_P16	1.200	0.952	1.1424
X13_P16	1.200	0.952	1.1424
X16_P16	1.200	1.360	1.6320
X19_P16	1.200	1.496	1.7952
X22_P16	1.200	1.768	2.1216
X25_P16	1.200	1.904	2.2848
X37_P16	1.200	2.584	3.1008
X49_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P16	X6_P16	X9_P16	X13_P16
A	0.0007	0.0008	0.0013	0.0016
B	0.0007	0.0008	0.0015	0.0017
C	0.0007	0.0008	0.0012	0.0015
	X16_P16	X19_P16	X22_P16	X25_P16
A	0.0022	0.0025	0.0029	0.0032
B	0.0022	0.0029	0.0031	0.0038
C	0.0019	0.0022	0.0027	0.0029
	X37_P16	X49_P16		
A	0.0048	0.0065		
B	0.0050	0.0067		

C	0.0043	0.0059		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0176	0.0167	4.2175	3.0651
A to Z ↑	0.0468	0.0427	26.0160	18.1510
B to Z ↓	0.0169	0.0159	4.2120	3.0604
B to Z ↑	0.0434	0.0393	26.0656	18.1527
C to Z ↓	0.0154	0.0141	4.2410	3.0941
C to Z ↑	0.0378	0.0330	26.1310	18.1849
	X9_P16	**X13_P16**	**X9_P16**	**X13_P16**
A to Z ↓	0.0171	0.0166	2.0528	1.5606
A to Z ↑	0.0470	0.0437	12.1236	8.9552
B to Z ↓	0.0166	0.0158	1.9996	1.4987
B to Z ↑	0.0460	0.0420	12.1312	8.9356
C to Z ↓	0.0134	0.0128	2.0089	1.5175
C to Z ↑	0.0305	0.0284	12.1599	8.9747
	X16_P16	**X19_P16**	**X16_P16**	**X19_P16**
A to Z ↓	0.0170	0.0165	1.2231	1.0206
A to Z ↑	0.0451	0.0442	7.2568	5.9731
B to Z ↓	0.0167	0.0163	1.2245	0.9990
B to Z ↑	0.0430	0.0432	7.2584	5.9718
C to Z ↓	0.0138	0.0134	1.2254	1.0386
C to Z ↑	0.0319	0.0299	7.2851	5.9966
	X22_P16	**X25_P16**	**X22_P16**	**X25_P16**
A to Z ↓	0.0168	0.0165	0.8963	0.7783
A to Z ↑	0.0445	0.0442	5.1792	4.4861
B to Z ↓	0.0163	0.0161	0.8806	0.7503
B to Z ↑	0.0425	0.0433	5.1680	4.4950
C to Z ↓	0.0132	0.0130	0.8859	0.7789
C to Z ↑	0.0296	0.0284	5.1911	4.5032
	X37_P16	**X49_P16**	**X37_P16**	**X49_P16**
A to Z ↓	0.0167	0.0168	0.5372	0.4069
A to Z ↑	0.0429	0.0429	3.0055	2.2549
B to Z ↓	0.0161	0.0162	0.5308	0.4025
B to Z ↑	0.0407	0.0406	3.0004	2.2570
C to Z ↓	0.0133	0.0135	0.5361	0.4063
C to Z ↑	0.0285	0.0290	3.0061	2.2607

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.580e-07	8.218e-10
X6_P16	2.153e-07	8.218e-10
X9_P16	3.093e-07	1.179e-09
X13_P16	4.033e-07	1.179e-09
X16_P16	4.974e-07	1.536e-09
X19_P16	6.192e-07	1.656e-09
X22_P16	6.861e-07	1.894e-09
X25_P16	8.033e-07	2.013e-09
X37_P16	1.126e-06	2.608e-09

X49_P16	1.488e-06	3.323e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	1.118e-04	1.549e-04	3.325e-04	4.176e-04
B (output stable)	-1.719e-07	-2.666e-06	1.159e-04	1.165e-04
C (output stable)	2.732e-06	3.802e-06	2.171e-05	2.369e-05
A to Z	1.026e-03	1.304e-03	2.198e-03	2.715e-03
B to Z	8.238e-04	1.019e-03	1.834e-03	2.199e-03
C to Z	6.072e-04	7.048e-04	9.823e-04	1.177e-03
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	4.768e-04	6.011e-04	7.071e-04	8.366e-04
B (output stable)	9.630e-05	1.422e-04	1.815e-04	2.315e-04
C (output stable)	2.422e-05	2.907e-05	3.678e-05	4.179e-05
A to Z	3.488e-03	4.124e-03	4.786e-03	5.474e-03
B to Z	2.828e-03	3.399e-03	3.887e-03	4.521e-03
C to Z	1.726e-03	1.904e-03	2.162e-03	2.369e-03
	X37_P16	X49_P16		
A (output stable)	1.169e-03	1.548e-03		
B (output stable)	2.490e-04	3.168e-04		
C (output stable)	6.189e-05	8.025e-05		
A to Z	7.886e-03	1.051e-02		
B to Z	6.300e-03	8.380e-03		
C to Z	3.453e-03	4.683e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

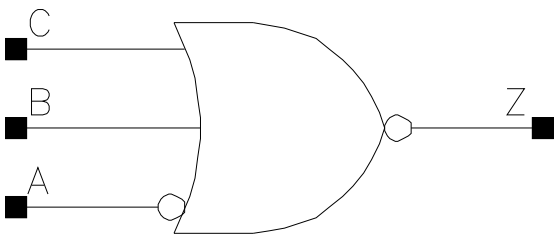
Pin Cycle (vdds)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	-1.693e-05	-2.288e-05	-5.364e-05	-6.691e-05
B (output stable)	8.231e-06	1.206e-05	5.295e-06	9.770e-06
C (output stable)	9.998e-06	1.416e-05	4.392e-05	5.505e-05
A to Z	-2.863e-06	-3.975e-06	-1.136e-05	-1.453e-05
B to Z	-9.139e-07	-1.251e-06	-6.894e-06	-7.457e-06
C to Z	-2.750e-08	-2.460e-07	-4.790e-07	-2.819e-07
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	-6.344e-05	-8.438e-05	-1.026e-04	-1.255e-04
B (output stable)	2.604e-05	3.499e-05	2.999e-05	4.116e-05
C (output stable)	4.145e-05	5.821e-05	7.404e-05	9.228e-05
A to Z	-1.240e-05	-1.663e-05	-2.195e-05	-2.736e-05
B to Z	-4.444e-06	-7.640e-06	-1.086e-05	-1.291e-05
C to Z	-7.608e-07	-9.434e-07	-4.176e-07	-5.315e-07
	X37_P16	X49_P16		
A (output stable)	-1.662e-04	-2.163e-04		
B (output stable)	5.811e-05	7.834e-05		
C (output stable)	1.165e-04	1.505e-04		
A to Z	-3.265e-05	-4.271e-05		
B to Z	-1.566e-05	-1.947e-05		
C to Z	-8.177e-07	-9.970e-07		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.680	0.8160
X13_P16	1.200	1.224	1.4688
X19_P16	1.200	1.496	1.7952
X25_P16	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0008	0.0011	0.0011	0.0021
B	0.0008	0.0017	0.0025	0.0033
C	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X13_P16**	**X6_P16**	**X13_P16**
A to Z ↓	0.0494	0.0459	3.0332	1.6648
A to Z ↑	0.0580	0.0565	18.3320	8.9274
B to Z ↓	0.0162	0.0158	3.0825	1.5058
B to Z ↑	0.0399	0.0420	18.3581	8.9384
C to Z ↓	0.0143	0.0128	3.1014	1.5186
C to Z ↑	0.0337	0.0283	18.3963	8.9703
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0527	0.0459	1.0324	0.7805

A to Z ↑	0.0601	0.0558	5.9847	4.4899
B to Z ↓	0.0163	0.0160	1.0467	0.7794
B to Z ↑	0.0405	0.0406	6.0085	4.4964
C to Z ↓	0.0133	0.0129	1.0401	0.7831
C to Z ↑	0.0300	0.0285	6.0189	4.5143

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P16	3.454e-07	9.409e-10
X13_P16	7.042e-07	1.417e-09
X19_P16	8.261e-07	1.655e-09
X25_P16	1.317e-06	2.251e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	1.224e-03	2.257e-03	3.026e-03	4.430e-03
B (output stable)	3.736e-06	4.487e-05	4.663e-05	7.602e-05
C (output stable)	5.737e-06	2.878e-05	2.524e-05	4.474e-05
A to Z	2.496e-03	4.909e-03	6.772e-03	9.483e-03
B to Z	1.032e-03	2.213e-03	3.156e-03	4.219e-03
C to Z	7.224e-04	1.179e-03	1.889e-03	2.332e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

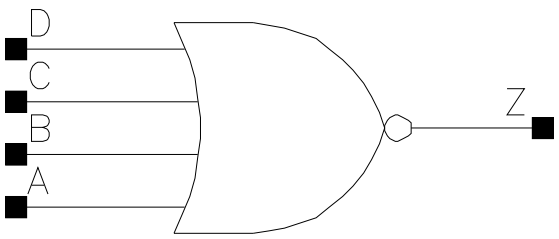
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	-2.563e-05	-6.906e-05	-8.373e-05	-1.238e-04
B (output stable)	1.395e-05	3.137e-05	5.062e-05	6.659e-05
C (output stable)	1.355e-05	3.292e-05	3.445e-05	5.389e-05
A to Z	-3.496e-06	-1.291e-05	-1.330e-05	-2.197e-05
B to Z	-1.213e-06	-6.901e-06	-5.644e-06	-1.069e-05
C to Z	-2.091e-07	-6.173e-07	-9.413e-07	-1.227e-06

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	1.904	2.2848
X32_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X32_P16
A	0.0007	0.0007	0.0008	0.0009
B	0.0007	0.0007	0.0009	0.0012
C	0.0006	0.0006	0.0008	0.0009
D	0.0006	0.0006	0.0008	0.0009

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0604	0.0584	2.9859	1.4647
A to Z ↑	0.0977	0.1040	5.5510	2.7217
B to Z ↓	0.0585	0.0571	2.9837	1.4653
B to Z ↑	0.0954	0.1020	5.5491	2.7216
C to Z ↓	0.0595	0.0583	2.9823	1.4640
C to Z ↑	0.0986	0.1066	5.5430	2.7234

D to Z ↓	0.0589	0.0577	2.9806	1.4650
D to Z ↑	0.0973	0.1055	5.5420	2.7228
	X25_P16	**X32_P16**	**X25_P16**	**X32_P16**
A to Z ↓	0.0595	0.0620	1.0179	0.8058
A to Z ↑	0.1011	0.0971	1.8546	1.4103
B to Z ↓	0.0582	0.0606	1.0175	0.8049
B to Z ↑	0.0996	0.0954	1.8547	1.4093
C to Z ↓	0.0570	0.0603	1.0139	0.8038
C to Z ↑	0.0996	0.0973	1.8512	1.4096
D to Z ↓	0.0554	0.0578	1.0137	0.8033
D to Z ↑	0.0978	0.0950	1.8512	1.4104

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	5.154e-07	1.417e-09
X17_P16	7.369e-07	1.536e-09
X25_P16	1.115e-06	2.013e-09
X32_P16	1.325e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	4.425e-04	5.475e-04	7.573e-04	9.561e-04
B (output stable)	3.645e-04	4.726e-04	6.626e-04	8.220e-04
C (output stable)	4.166e-04	5.059e-04	7.955e-04	1.019e-03
D (output stable)	3.377e-04	4.321e-04	6.810e-04	8.650e-04
A to Z	3.035e-03	4.556e-03	6.939e-03	8.757e-03
B to Z	2.875e-03	4.411e-03	6.725e-03	8.509e-03
C to Z	3.080e-03	4.538e-03	6.503e-03	8.239e-03
D to Z	2.919e-03	4.397e-03	6.298e-03	7.955e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

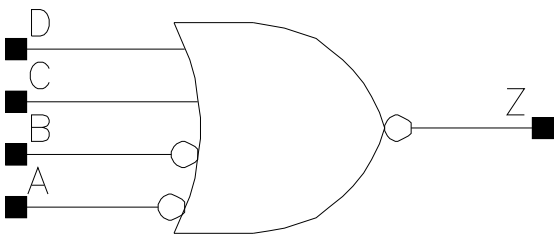
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	-1.318e-06	-1.224e-06	-1.631e-06	-2.120e-06
B (output stable)	3.547e-06	3.360e-06	5.484e-06	7.874e-06
C (output stable)	-2.332e-06	-2.297e-06	-2.916e-06	-3.566e-06
D (output stable)	4.646e-06	4.432e-06	6.855e-06	9.230e-06
A to Z	-8.587e-07	-1.032e-06	-1.521e-06	-1.781e-06
B to Z	4.820e-08	-2.042e-07	-2.056e-07	-2.576e-07
C to Z	-8.804e-07	-1.126e-06	-1.569e-06	-1.510e-06
D to Z	-7.970e-08	-1.757e-07	-4.561e-07	-4.892e-07

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X13_P16	1.200	1.496	1.7952
X19_P16	1.200	2.040	2.4480
X25_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0011	0.0011	0.0020	0.0019
B	0.0011	0.0015	0.0021	0.0020
C	0.0008	0.0016	0.0024	0.0032
D	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X13_P16	X6_P16	X13_P16
A to Z ↓	0.0415	0.0521	2.9699	1.4743
A to Z ↑	0.0581	0.0717	17.6496	9.0114
B to Z ↓	0.0387	0.0502	2.9669	1.4724
B to Z ↑	0.0584	0.0727	17.6539	9.0365
C to Z ↓	0.0167	0.0158	3.1205	1.4981
C to Z ↑	0.0401	0.0418	17.6866	9.0311

D to Z ↓	0.0144	0.0129	3.1125	1.5121
D to Z ↑	0.0332	0.0290	17.7116	9.0605
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0455	0.0499	1.0141	0.7666
A to Z ↑	0.0644	0.0696	5.9895	4.5123
B to Z ↓	0.0421	0.0468	1.0124	0.7654
B to Z ↑	0.0639	0.0695	6.0068	4.5133
C to Z ↓	0.0164	0.0160	1.0476	0.7858
C to Z ↑	0.0403	0.0402	6.0124	4.5170
D to Z ↓	0.0133	0.0128	1.0404	0.7826
D to Z ↑	0.0300	0.0278	6.0202	4.5350

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P16	4.117e-07	1.179e-09
X13_P16	5.913e-07	1.655e-09
X19_P16	9.383e-07	2.132e-09
X25_P16	1.056e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	7.045e-04	1.319e-03	1.949e-03	2.424e-03
B (output stable)	6.305e-04	1.266e-03	1.805e-03	2.295e-03
C (output stable)	2.194e-06	3.090e-05	5.079e-05	8.155e-05
D (output stable)	1.203e-05	5.170e-05	6.379e-05	1.101e-04
A to Z	2.941e-03	5.660e-03	8.399e-03	1.080e-02
B to Z	2.722e-03	5.368e-03	7.737e-03	1.018e-02
C to Z	1.077e-03	2.194e-03	3.142e-03	4.123e-03
D to Z	7.472e-04	1.212e-03	1.889e-03	2.233e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

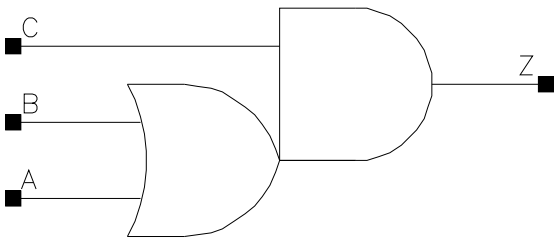
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	-1.219e-05	-3.579e-05	-4.456e-05	-6.414e-05
B (output stable)	-1.175e-05	-3.510e-05	-4.244e-05	-6.082e-05
C (output stable)	1.569e-05	2.412e-05	4.162e-05	5.265e-05
D (output stable)	2.188e-05	5.110e-05	5.943e-05	8.712e-05
A to Z	-3.508e-06	-1.467e-05	-1.614e-05	-2.521e-05
B to Z	-3.670e-06	-1.389e-05	-1.541e-05	-2.429e-05
C to Z	-8.694e-07	-6.536e-06	-5.604e-06	-1.072e-05
D to Z	-2.458e-07	-3.063e-07	-9.805e-07	-6.448e-07

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0010	0.0010	0.0018
B	0.0011	0.0010	0.0020
C	0.0011	0.0011	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0514	0.0604	3.0789	1.5379
A to Z ↑	0.0387	0.0431	5.5540	2.7228
B to Z ↓	0.0492	0.0588	3.0770	1.5364
B to Z ↑	0.0355	0.0404	5.5446	2.7204
C to Z ↓	0.0413	0.0460	3.0407	1.5039
C to Z ↑	0.0375	0.0414	5.5442	2.7191
	X33_P16		**X33_P16**	
A to Z ↓	0.0625		0.7822	
A to Z ↑	0.0456		1.3700	

B to Z ↓	0.0608		0.7813	
B to Z ↑	0.0422		1.3655	
C to Z ↓	0.0468		0.7623	
C to Z ↑	0.0426		1.3663	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	5.258e-07	9.409e-10
X17_P16	7.207e-07	1.060e-09
X33_P16	1.453e-06	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.041e-04	1.056e-04	2.081e-04
B (output stable)	8.885e-05	8.890e-05	1.755e-04
C (output stable)	4.480e-05	4.681e-05	8.799e-05
A to Z	2.207e-03	3.163e-03	6.550e-03
B to Z	1.908e-03	2.875e-03	5.983e-03
C to Z	2.435e-03	3.390e-03	6.933e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

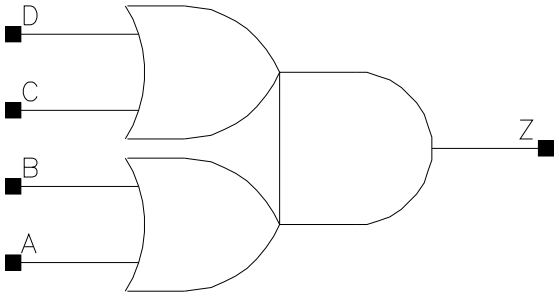
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-2.052e-06	-2.165e-06	-4.252e-06
B (output stable)	1.999e-06	2.009e-06	4.108e-06
C (output stable)	1.277e-07	1.962e-07	2.037e-07
A to Z	-1.388e-06	-1.644e-06	-3.609e-06
B to Z	-2.400e-07	-3.352e-07	-4.665e-07
C to Z	-6.302e-07	-1.078e-06	-1.596e-06

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0006	0.0009	0.0019
B	0.0007	0.0010	0.0018
C	0.0006	0.0010	0.0019
D	0.0006	0.0010	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0907	0.0743	3.0317	1.5280
A to Z ↑	0.0560	0.0469	5.4448	2.7189
B to Z ↓	0.0896	0.0726	3.0319	1.5289
B to Z ↑	0.0542	0.0447	5.4409	2.7150

C to Z ↓	0.0792	0.0654	3.0069	1.5196
C to Z ↑	0.0533	0.0459	5.4413	2.7165
D to Z ↓	0.0763	0.0628	3.0083	1.5205
D to Z ↑	0.0504	0.0426	5.4394	2.7150
	X33_P16		**X33_P16**	
A to Z ↓	0.0750		0.7904	
A to Z ↑	0.0469		1.3654	
B to Z ↓	0.0702		0.7910	
B to Z ↑	0.0436		1.3636	
C to Z ↓	0.0651		0.7853	
C to Z ↑	0.0449		1.3655	
D to Z ↓	0.0600		0.7862	
D to Z ↑	0.0414		1.3627	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	5.298e-07	1.179e-09
X17_P16	9.997e-07	1.298e-09
X33_P16	1.850e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.140e-05	3.789e-05	1.183e-04
B (output stable)	9.069e-06	1.319e-05	3.968e-05
C (output stable)	7.559e-05	1.112e-04	3.351e-04
D (output stable)	6.269e-05	7.874e-05	1.958e-04
A to Z	2.582e-03	4.080e-03	8.165e-03
B to Z	2.446e-03	3.792e-03	7.304e-03
C to Z	2.234e-03	3.563e-03	7.098e-03
D to Z	2.076e-03	3.262e-03	6.219e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

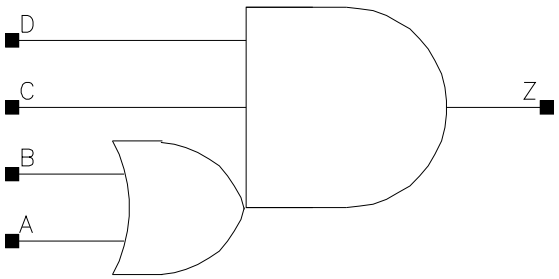
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-1.141e-06	-1.998e-06	-9.257e-06
B (output stable)	3.100e-06	7.154e-06	1.241e-05
C (output stable)	-3.076e-06	-3.936e-06	-2.731e-05
D (output stable)	3.938e-06	9.165e-06	2.873e-05
A to Z	-1.142e-06	-2.032e-06	-8.517e-06
B to Z	-3.656e-07	-5.932e-07	-2.510e-06
C to Z	-1.284e-06	-2.027e-06	-8.814e-06
D to Z	-3.599e-07	-7.836e-07	-3.010e-06

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	1.088	1.3056
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0006	0.0010	0.0015	0.0018
B	0.0006	0.0010	0.0015	0.0018
C	0.0007	0.0010	0.0016	0.0019
D	0.0006	0.0010	0.0016	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0768	0.0703	3.1836	1.5486
A to Z ↑	0.0665	0.0596	5.6565	2.7347
B to Z ↓	0.0753	0.0662	3.1856	1.5494
B to Z ↑	0.0630	0.0540	5.6455	2.7317
C to Z ↓	0.0565	0.0514	3.0760	1.5097

C to Z ↑	0.0658	0.0576	5.6387	2.7290
D to Z ↓	0.0551	0.0496	3.0759	1.5075
D to Z ↑	0.0662	0.0581	5.6393	2.7283
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0735	0.0694	1.0482	0.7869
A to Z ↑	0.0606	0.0601	1.8509	1.3852
B to Z ↓	0.0692	0.0655	1.0493	0.7866
B to Z ↑	0.0559	0.0553	1.8468	1.3832
C to Z ↓	0.0541	0.0512	1.0188	0.7655
C to Z ↑	0.0595	0.0580	1.8458	1.3821
D to Z ↓	0.0515	0.0491	1.0171	0.7635
D to Z ↑	0.0584	0.0575	1.8444	1.3828

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	2.994e-07	1.060e-09
X17_P16	5.885e-07	1.298e-09
X25_P16	9.572e-07	2.013e-09
X33_P16	1.186e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	7.099e-05	1.421e-04	2.510e-04	2.809e-04
B (output stable)	6.611e-05	1.307e-04	2.190e-04	2.417e-04
C (output stable)	9.736e-06	2.105e-05	5.086e-05	5.859e-05
D (output stable)	2.335e-05	5.197e-05	1.609e-04	1.722e-04
A to Z	2.132e-03	3.777e-03	6.072e-03	7.367e-03
B to Z	1.994e-03	3.359e-03	5.440e-03	6.595e-03
C to Z	2.358e-03	4.087e-03	6.736e-03	8.027e-03
D to Z	2.251e-03	3.887e-03	6.227e-03	7.504e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

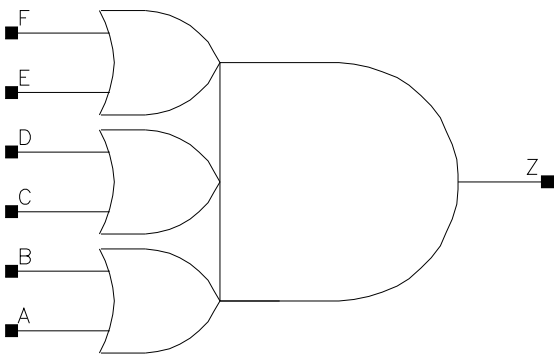
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	-1.382e-06	-4.036e-06	-4.462e-06	-5.207e-06
B (output stable)	3.444e-07	3.061e-06	3.402e-06	5.491e-06
C (output stable)	1.493e-07	2.173e-08	-1.620e-07	-2.978e-07
D (output stable)	1.732e-07	8.693e-08	-5.372e-08	-1.052e-07
A to Z	-1.023e-06	-4.688e-06	-6.659e-06	-7.096e-06
B to Z	-1.168e-07	-3.603e-07	-5.114e-07	-8.529e-07
C to Z	-3.502e-07	-1.392e-06	-2.057e-06	-2.108e-06
D to Z	-4.017e-07	-1.097e-06	-1.520e-06	-1.538e-06

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0009	0.0016
B	0.0006	0.0009	0.0018
C	0.0006	0.0009	0.0017
D	0.0006	0.0009	0.0018
E	0.0006	0.0009	0.0016
F	0.0006	0.0009	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.1037	0.0864	3.2799	1.5877
A to Z ↑	0.0749	0.0656	5.6187	2.7490
B to Z ↓	0.1015	0.0850	3.2793	1.5887
B to Z ↑	0.0722	0.0630	5.6183	2.7479
C to Z ↓	0.0950	0.0810	3.2556	1.5838
C to Z ↑	0.0737	0.0639	5.6188	2.7485
D to Z ↓	0.0937	0.0794	3.2557	1.5843
D to Z ↑	0.0707	0.0610	5.6138	2.7471
E to Z ↓	0.0817	0.0707	3.2269	1.5725
E to Z ↑	0.0669	0.0592	5.6162	2.7469
F to Z ↓	0.0809	0.0688	3.2277	1.5738
F to Z ↑	0.0641	0.0559	5.6094	2.7447
	X33_P16		**X33_P16**	
A to Z ↓	0.0864		0.8109	
A to Z ↑	0.0668		1.3871	
B to Z ↓	0.0856		0.8110	
B to Z ↑	0.0632		1.3840	
C to Z ↓	0.0796		0.8056	
C to Z ↑	0.0651		1.3861	
D to Z ↓	0.0784		0.8058	
D to Z ↑	0.0615		1.3836	
E to Z ↓	0.0698		0.8002	
E to Z ↑	0.0604		1.3849	
F to Z ↓	0.0685		0.8004	
F to Z ↑	0.0568		1.3825	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	4.979e-07	1.417e-09
X17_P16	9.224e-07	1.536e-09
X33_P16	1.749e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.656e-05	3.016e-05	5.656e-05
B (output stable)	8.059e-06	1.683e-05	2.747e-05
C (output stable)	4.694e-05	7.602e-05	1.570e-04
D (output stable)	3.607e-05	5.800e-05	1.231e-04
E (output stable)	1.027e-04	1.551e-04	2.965e-04
F (output stable)	1.101e-04	1.623e-04	3.131e-04
A to Z	2.969e-03	4.873e-03	9.428e-03
B to Z	2.817e-03	4.602e-03	8.945e-03
C to Z	2.697e-03	4.467e-03	8.610e-03
D to Z	2.560e-03	4.189e-03	8.098e-03
E to Z	2.330e-03	3.907e-03	7.561e-03
F to Z	2.201e-03	3.632e-03	7.061e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

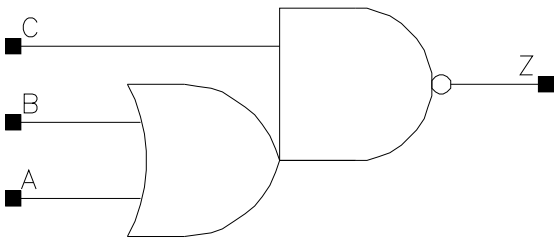
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-8.954e-07	-1.646e-06	-3.050e-06
B (output stable)	3.154e-06	6.597e-06	1.261e-05
C (output stable)	-1.804e-06	-2.908e-06	-6.266e-06
D (output stable)	2.868e-06	6.270e-06	1.117e-05
E (output stable)	-1.894e-06	-1.901e-06	-4.914e-06
F (output stable)	1.615e-06	5.265e-06	8.436e-06
A to Z	-1.614e-06	-2.435e-06	-4.864e-06
B to Z	-7.661e-07	-1.176e-06	-2.467e-06
C to Z	-1.696e-06	-2.699e-06	-5.448e-06
D to Z	-7.234e-07	-1.144e-06	-2.388e-06
E to Z	-1.753e-06	-2.718e-06	-5.377e-06
F to Z	-8.460e-07	-1.330e-06	-2.529e-06

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X34_P16	1.200	2.720	3.2640
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X34_P16	X46_P16
A	0.0008	0.0023	0.0048	0.0062
B	0.0008	0.0022	0.0042	0.0057
C	0.0008	0.0024	0.0049	0.0064

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0199	0.0208	5.9853	1.9664
A to Z ↑	0.0295	0.0317	11.8401	3.9601
B to Z ↓	0.0167	0.0173	5.9223	1.9928
B to Z ↑	0.0266	0.0267	11.8823	3.9738
C to Z ↓	0.0197	0.0200	5.4586	1.8101
C to Z ↑	0.0257	0.0255	5.5371	1.8250
	X34_P16	**X46_P16**	**X34_P16**	**X46_P16**
A to Z ↓	0.0216	0.0215	1.0006	0.7611

A to Z ↑	0.0327	0.0322	1.9746	1.5059
B to Z ↓	0.0175	0.0175	1.0113	0.7710
B to Z ↑	0.0270	0.0269	1.9826	1.5108
C to Z ↓	0.0206	0.0204	0.9204	0.7012
C to Z ↑	0.0259	0.0257	0.9117	0.6936

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P16	3.399e-07	8.218e-10
X17_P16	9.202e-07	1.536e-09
X34_P16	1.834e-06	2.727e-09
X46_P16	2.393e-06	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	9.424e-05	3.208e-04	6.785e-04	8.421e-04
B (output stable)	8.083e-05	2.586e-04	5.425e-04	6.777e-04
C (output stable)	4.083e-05	1.421e-04	2.974e-04	3.763e-04
A to Z	9.636e-04	3.198e-03	6.703e-03	8.607e-03
B to Z	6.566e-04	2.006e-03	4.165e-03	5.395e-03
C to Z	1.166e-03	3.616e-03	7.537e-03	9.700e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

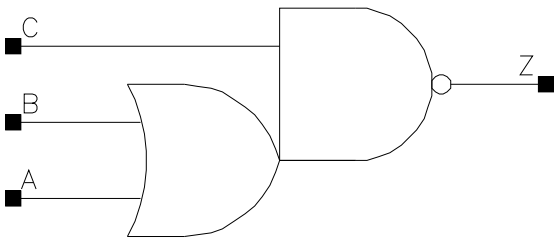
Pin Cycle (vdds)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	-1.537e-06	-7.219e-06	-1.817e-05	-2.148e-05
B (output stable)	2.526e-06	1.747e-06	1.334e-06	4.008e-06
C (output stable)	-5.900e-09	-4.290e-08	1.408e-07	5.980e-08
A to Z	-1.201e-06	-5.363e-06	-1.342e-05	-1.556e-05
B to Z	-4.920e-08	-6.930e-07	-9.460e-07	-1.339e-06
C to Z	-7.048e-07	-1.077e-06	-3.160e-06	-3.099e-06

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.544	0.6528
X11_P16	1.200	0.952	1.1424
X17_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X17_P16	X23_P16
A	0.0008	0.0016	0.0025	0.0034
B	0.0008	0.0017	0.0023	0.0031
C	0.0008	0.0015	0.0022	0.0030
	X46_P16			
A	0.0068			
B	0.0062			
C	0.0061			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0215	0.0219	6.1367	2.8673
A to Z ↑	0.0366	0.0369	12.4567	5.8408
B to Z ↓	0.0190	0.0193	6.0629	2.8053

B to Z ↑	0.0340	0.0345	12.4883	5.8569
C to Z ↓	0.0168	0.0167	5.6700	2.6381
C to Z ↑	0.0201	0.0199	5.8954	2.7590
	X17_P16	**X23_P16**	**X17_P16**	**X23_P16**
A to Z ↓	0.0211	0.0222	1.9773	1.4613
A to Z ↑	0.0350	0.0385	3.8790	2.9415
B to Z ↓	0.0183	0.0190	1.9769	1.4593
B to Z ↑	0.0321	0.0334	3.8879	2.9486
C to Z ↓	0.0161	0.0165	1.8374	1.3552
C to Z ↑	0.0188	0.0193	1.8356	1.3922
	X46_P16		**X46_P16**	
A to Z ↓	0.0220		0.7582	
A to Z ↑	0.0377		1.4807	
B to Z ↓	0.0187		0.7519	
B to Z ↑	0.0327		1.4841	
C to Z ↓	0.0165		0.7015	
C to Z ↑	0.0189		0.7017	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P16	3.381e-07	8.218e-10
X11_P16	6.587e-07	1.179e-09
X17_P16	9.514e-07	1.536e-09
X23_P16	1.316e-06	2.013e-09
X46_P16	2.465e-06	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	2.555e-05	5.464e-05	8.157e-05	1.669e-04
B (output stable)	1.133e-05	2.730e-05	3.701e-05	7.135e-05
C (output stable)	2.195e-04	5.141e-04	6.291e-04	9.748e-04
A to Z	1.282e-03	2.773e-03	3.811e-03	5.838e-03
B to Z	9.749e-04	2.137e-03	2.808e-03	4.074e-03
C to Z	6.604e-04	1.436e-03	1.929e-03	2.846e-03
	X46_P16			
A (output stable)	3.153e-04			
B (output stable)	1.363e-04			
C (output stable)	1.774e-03			
A to Z	1.121e-02			
B to Z	7.751e-03			
C to Z	5.442e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	-1.447e-06	-3.099e-06	-4.687e-06	-1.107e-05
B (output stable)	2.373e-06	5.224e-06	7.865e-06	2.115e-06
C (output stable)	-5.800e-08	-2.286e-06	-3.138e-07	-4.912e-06
A to Z	-1.054e-06	-3.997e-06	-3.088e-06	-1.318e-05
B to Z	4.100e-09	-1.506e-06	-1.540e-07	-2.801e-06
C to Z	-3.592e-07	-7.577e-07	-1.078e-06	-1.865e-06

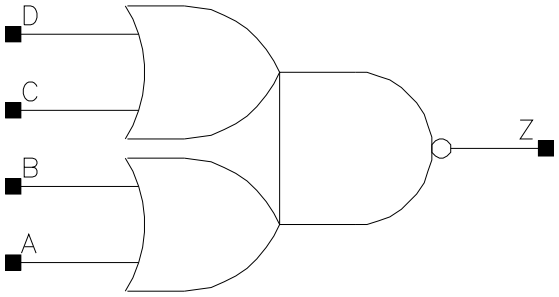
	X46_P16			
A (output stable)	-1.931e-05			
B (output stable)	4.851e-06			
C (output stable)	-9.213e-06			
A to Z	-2.059e-05			
B to Z	-5.473e-06			
C to Z	-3.929e-06			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0009	0.0017	0.0025	0.0034
B	0.0008	0.0015	0.0022	0.0030
C	0.0008	0.0016	0.0023	0.0032
D	0.0008	0.0014	0.0021	0.0029
	X42_P16			
A	0.0068			
B	0.0061			
C	0.0064			
D	0.0057			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0234	0.0248	5.5439	2.7909
A to Z ↑	0.0421	0.0427	13.0125	5.9786
B to Z ↓	0.0210	0.0217	5.4645	2.7899
B to Z ↑	0.0389	0.0370	13.0300	5.9903
C to Z ↓	0.0204	0.0220	5.5812	2.7943
C to Z ↑	0.0311	0.0335	12.8112	5.9876
D to Z ↓	0.0175	0.0180	5.4994	2.8072
D to Z ↑	0.0277	0.0264	12.8425	6.0099
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0240	0.0243	1.9140	1.3699
A to Z ↑	0.0404	0.0416	4.0094	2.9467
B to Z ↓	0.0215	0.0212	1.9230	1.3661
B to Z ↑	0.0360	0.0365	4.0193	2.9532
C to Z ↓	0.0215	0.0215	1.9148	1.3721
C to Z ↑	0.0316	0.0321	4.0179	2.9475
D to Z ↓	0.0181	0.0178	1.9451	1.3765
D to Z ↑	0.0259	0.0260	4.0339	2.9608
	X42_P16		**X42_P16**	
A to Z ↓	0.0247		0.7121	
A to Z ↑	0.0416		1.4908	
B to Z ↓	0.0216		0.7058	
B to Z ↑	0.0368		1.4941	
C to Z ↓	0.0223		0.7147	
C to Z ↑	0.0325		1.4855	
D to Z ↓	0.0183		0.7110	
D to Z ↑	0.0263		1.4919	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P16	3.905e-07	9.409e-10
X10_P16	7.804e-07	1.536e-09
X15_P16	1.060e-06	1.894e-09
X21_P16	1.478e-06	2.489e-09
X42_P16	2.836e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	3.387e-05	1.161e-04	1.506e-04	2.202e-04
B (output stable)	1.145e-05	3.737e-05	5.107e-05	6.941e-05
C (output stable)	9.635e-05	3.314e-04	3.869e-04	5.760e-04
D (output stable)	6.760e-05	1.779e-04	2.232e-04	3.201e-04
A to Z	1.563e-03	3.612e-03	4.950e-03	6.996e-03
B to Z	1.265e-03	2.694e-03	3.738e-03	5.263e-03
C to Z	1.050e-03	2.563e-03	3.487e-03	4.873e-03
D to Z	7.626e-04	1.625e-03	2.262e-03	3.136e-03
	X42_P16			
A (output stable)	4.315e-04			
B (output stable)	1.413e-04			
C (output stable)	1.134e-03			
D (output stable)	6.310e-04			

A to Z	1.388e-02			
B to Z	1.044e-02			
C to Z	9.788e-03			
D to Z	6.327e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

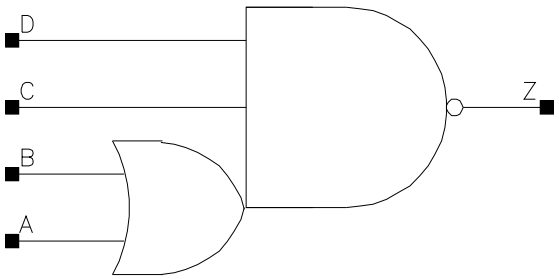
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	-1.845e-06	-9.101e-06	-8.039e-06	-1.431e-05
B (output stable)	6.685e-06	1.187e-05	1.469e-05	2.332e-05
C (output stable)	-3.717e-06	-2.900e-05	-2.098e-05	-4.072e-05
D (output stable)	8.406e-06	3.036e-05	2.622e-05	4.795e-05
A to Z	-1.894e-06	-8.422e-06	-7.846e-06	-1.329e-05
B to Z	-6.592e-07	-2.890e-06	-1.668e-06	-4.533e-06
C to Z	-1.533e-06	-7.998e-06	-6.921e-06	-1.227e-05
D to Z	-4.072e-07	-2.475e-06	-1.748e-06	-3.465e-06
	X42_P16			
A (output stable)	-2.542e-05			
B (output stable)	4.226e-05			
C (output stable)	-7.093e-05			
D (output stable)	8.417e-05			
A to Z	-2.456e-05			
B to Z	-7.754e-06			
C to Z	-2.221e-05			
D to Z	-5.697e-06			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X21_P16	1.200	2.448	2.9376
X31_P16	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X21_P16	X31_P16
A	0.0008	0.0015	0.0031	0.0047
B	0.0010	0.0014	0.0027	0.0041
C	0.0008	0.0017	0.0032	0.0048
D	0.0008	0.0016	0.0031	0.0046

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0288	0.0272	8.0785	4.2492
A to Z ↑	0.0392	0.0361	11.7230	5.8948
B to Z ↓	0.0256	0.0221	8.0680	4.2602
B to Z ↑	0.0360	0.0304	11.7781	5.9182
C to Z ↓	0.0279	0.0285	7.6155	4.0165

C to Z ↑	0.0307	0.0300	5.3745	2.7031
D to Z ↓	0.0286	0.0274	7.6282	4.0254
D to Z ↑	0.0293	0.0276	5.4227	2.7050
	X21_P16	**X31_P16**	**X21_P16**	**X31_P16**
A to Z ↓	0.0277	0.0279	2.2082	1.4946
A to Z ↑	0.0355	0.0355	2.9467	1.9729
B to Z ↓	0.0222	0.0224	2.2144	1.5021
B to Z ↑	0.0296	0.0298	2.9574	1.9812
C to Z ↓	0.0285	0.0286	2.0882	1.4150
C to Z ↑	0.0295	0.0295	1.3664	0.9184
D to Z ↓	0.0275	0.0277	2.0912	1.4170
D to Z ↑	0.0272	0.0273	1.3664	0.9168

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P16	3.290e-07	1.060e-09
X10_P16	6.089e-07	1.536e-09
X21_P16	1.120e-06	2.489e-09
X31_P16	1.633e-06	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	1.409e-04	2.972e-04	5.641e-04	8.325e-04
B (output stable)	1.324e-04	2.585e-04	4.809e-04	7.047e-04
C (output stable)	2.040e-05	5.816e-05	1.132e-04	1.655e-04
D (output stable)	5.268e-05	1.697e-04	2.967e-04	4.323e-04
A to Z	1.537e-03	2.655e-03	5.174e-03	7.682e-03
B to Z	1.113e-03	1.758e-03	3.366e-03	5.061e-03
C to Z	1.822e-03	3.487e-03	6.699e-03	9.965e-03
D to Z	1.637e-03	2.901e-03	5.583e-03	8.321e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

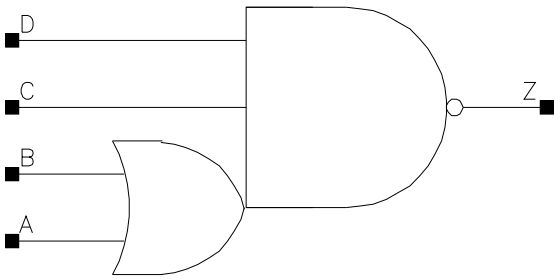
Pin Cycle (vdds)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	-4.456e-06	-6.539e-06	-1.161e-05	-1.595e-05
B (output stable)	2.310e-06	5.227e-06	7.738e-06	1.063e-05
C (output stable)	-3.228e-08	-1.166e-07	-7.822e-08	-1.771e-07
D (output stable)	5.772e-08	2.076e-07	4.485e-07	4.923e-07
A to Z	-4.421e-06	-6.294e-06	-1.115e-05	-1.376e-05
B to Z	-2.700e-08	-2.310e-07	-6.400e-07	-9.750e-07
C to Z	-1.180e-06	-1.773e-06	-2.807e-06	-4.061e-06
D to Z	-8.878e-07	-1.914e-06	-3.055e-06	-3.976e-06

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0009	0.0017	0.0026	0.0034
B	0.0008	0.0016	0.0023	0.0031
C	0.0008	0.0016	0.0024	0.0031
D	0.0008	0.0015	0.0022	0.0030

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0289	0.0312	8.2301	4.2448
A to Z ↑	0.0425	0.0461	11.5029	5.8304
B to Z ↓	0.0254	0.0269	8.1447	4.2416
B to Z ↑	0.0402	0.0414	11.5263	5.8398
C to Z ↓	0.0224	0.0253	7.7553	4.0170

C to Z ↑	0.0246	0.0260	5.4404	2.7471
D to Z ↓	0.0219	0.0225	7.7818	4.0323
D to Z ↑	0.0220	0.0222	5.4696	2.7649
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0308	0.0309	2.9195	2.1927
A to Z ↑	0.0445	0.0452	3.9117	2.9559
B to Z ↓	0.0266	0.0266	2.9171	2.1891
B to Z ↑	0.0403	0.0410	3.9202	2.9598
C to Z ↓	0.0247	0.0251	2.7619	2.0732
C to Z ↑	0.0250	0.0254	1.8302	1.3779
D to Z ↓	0.0223	0.0226	2.7723	2.0799
D to Z ↑	0.0215	0.0218	1.8422	1.3860

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P16	3.216e-07	1.060e-09
X10_P16	6.345e-07	1.536e-09
X15_P16	8.544e-07	1.894e-09
X21_P16	1.191e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	2.019e-05	5.670e-05	7.801e-05	1.067e-04
B (output stable)	1.295e-05	4.502e-05	5.466e-05	7.692e-05
C (output stable)	7.528e-05	1.521e-04	2.318e-04	3.079e-04
D (output stable)	1.347e-04	4.530e-04	5.476e-04	8.120e-04
A to Z	1.771e-03	3.920e-03	5.563e-03	7.564e-03
B to Z	1.446e-03	3.044e-03	4.297e-03	5.864e-03
C to Z	1.103e-03	2.550e-03	3.521e-03	4.870e-03
D to Z	8.813e-04	1.877e-03	2.637e-03	3.599e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

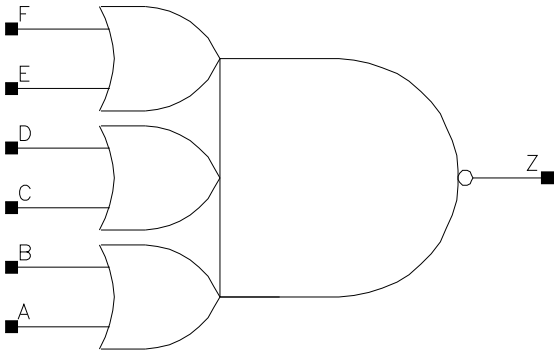
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	-1.182e-06	-5.521e-06	-5.115e-06	-9.016e-06
B (output stable)	1.979e-06	6.145e-06	6.080e-06	1.061e-05
C (output stable)	-6.810e-09	-4.046e-07	-1.125e-06	-9.349e-07
D (output stable)	-3.438e-08	-2.208e-06	-2.480e-06	-4.211e-06
A to Z	-1.134e-06	-6.063e-06	-5.465e-06	-1.012e-05
B to Z	-9.910e-08	-2.130e-07	-4.840e-07	-3.100e-07
C to Z	-4.274e-07	-2.330e-06	-2.565e-06	-4.119e-06
D to Z	-3.381e-07	-7.813e-07	-1.382e-06	-1.429e-06

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	1.088	1.3056
X9_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X9_P16
A	0.0007	0.0018
B	0.0007	0.0016
C	0.0007	0.0017
D	0.0006	0.0015
E	0.0007	0.0016
F	0.0007	0.0015

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X9_P16	X3_P16	X9_P16
A to Z ↓	0.0366	0.0377	9.5675	3.8295
A to Z ↑	0.0574	0.0540	16.3920	5.8537
B to Z ↓	0.0345	0.0336	9.6078	3.8276
B to Z ↑	0.0563	0.0492	16.4134	5.8626
C to Z ↓	0.0345	0.0349	9.6063	3.8352
C to Z ↑	0.0497	0.0468	16.3952	5.8393
D to Z ↓	0.0319	0.0308	9.6279	3.8372
D to Z ↑	0.0482	0.0416	16.4235	5.8509
E to Z ↓	0.0286	0.0297	9.6200	3.8273
E to Z ↑	0.0384	0.0371	16.4185	5.8396
F to Z ↓	0.0262	0.0250	9.6437	3.8302
F to Z ↑	0.0367	0.0309	16.4725	5.8603

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P16	3.862e-07	1.298e-09
X9_P16	9.527e-07	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P16	X9_P16
A (output stable)	2.276e-05	9.622e-05
B (output stable)	1.177e-05	5.482e-05
C (output stable)	6.507e-05	2.340e-04
D (output stable)	5.391e-05	1.601e-04
E (output stable)	1.381e-04	3.656e-04
F (output stable)	1.485e-04	3.555e-04
A to Z	2.075e-03	5.461e-03
B to Z	1.874e-03	4.566e-03
C to Z	1.688e-03	4.447e-03
D to Z	1.485e-03	3.600e-03
E to Z	1.202e-03	3.330e-03
F to Z	1.001e-03	2.440e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

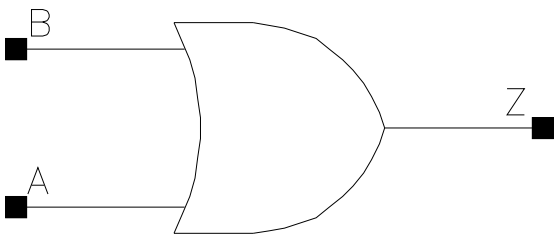
Pin Cycle (vdds)	X3_P16	X9_P16
A (output stable)	-1.261e-06	-7.510e-06
B (output stable)	4.502e-06	1.989e-05
C (output stable)	-2.297e-06	-1.628e-05
D (output stable)	4.437e-06	2.125e-05
E (output stable)	-1.492e-06	-1.400e-05
F (output stable)	3.533e-06	1.098e-05
A to Z	-1.562e-06	-9.991e-06
B to Z	-5.850e-07	-3.506e-06
C to Z	-1.651e-06	-1.041e-05
D to Z	-6.169e-07	-4.145e-06
E to Z	-1.569e-06	-1.022e-05
F to Z	-7.043e-07	-4.833e-06

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X33_P16	1.200	1.360	1.6320
X50_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P16	X16_P16	X33_P16	X50_P16
A	0.0008	0.0009	0.0018	0.0019
B	0.0006	0.0009	0.0018	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0703	0.0607	3.0965	1.5656
A to Z ↑	0.0371	0.0374	5.5046	2.7670
B to Z ↓	0.0670	0.0582	3.0998	1.5661
B to Z ↑	0.0354	0.0352	5.5058	2.7671
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0622	0.0733	0.7733	0.5343
A to Z ↑	0.0369	0.0366	1.3484	0.9089
B to Z ↓	0.0573	0.0686	0.7731	0.5349
B to Z ↑	0.0343	0.0345	1.3469	0.9072

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	5.020e-07	8.218e-10
X16_P16	8.648e-07	9.409e-10
X33_P16	1.722e-06	1.536e-09
X50_P16	2.327e-06	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	2.311e-05	4.365e-05	1.427e-04	1.337e-04
B (output stable)	3.749e-06	5.458e-06	7.646e-05	6.497e-05
A to Z	1.983e-03	3.123e-03	6.554e-03	8.681e-03
B to Z	1.811e-03	2.826e-03	5.679e-03	7.835e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

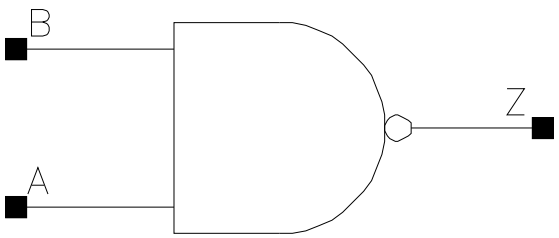
Pin Cycle (vdds)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	-1.613e-06	-2.690e-06	-1.178e-05	-1.150e-05
B (output stable)	1.052e-05	1.905e-05	7.492e-05	7.331e-05
A to Z	-9.391e-07	-1.532e-06	-7.774e-06	-7.639e-06
B to Z	-2.941e-07	-3.526e-07	-7.406e-07	-9.225e-07

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X16_P16	1.200	0.952	1.1424
X24_P16	1.200	1.088	1.3056
X32_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P16	X16_P16	X24_P16	X32_P16
A	0.0010	0.0010	0.0010	0.0009
B	0.0011	0.0011	0.0011	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0527	0.0549	2.9726	1.5449
A to Z ↑	0.0557	0.0569	5.5266	2.8107
B to Z ↓	0.0539	0.0563	2.9673	1.5436
B to Z ↑	0.0534	0.0540	5.5307	2.8116
	X24_P16	**X32_P16**	**X24_P16**	**X32_P16**
A to Z ↓	0.0612	0.0624	1.0518	0.7968
A to Z ↑	0.0610	0.0631	1.8797	1.4052
B to Z ↓	0.0626	0.0640	1.0520	0.7966
B to Z ↑	0.0581	0.0610	1.8808	1.4050

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	8.474e-07	1.060e-09
X16_P16	1.148e-06	1.179e-09
X24_P16	1.421e-06	1.295e-09
X32_P16	1.681e-06	1.417e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	1.919e-05	1.926e-05	1.934e-05	2.067e-05
B (output stable)	5.101e-05	5.120e-05	5.123e-05	5.282e-05
A to Z	3.867e-03	4.439e-03	5.570e-03	7.431e-03
B to Z	3.674e-03	4.258e-03	5.401e-03	7.255e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

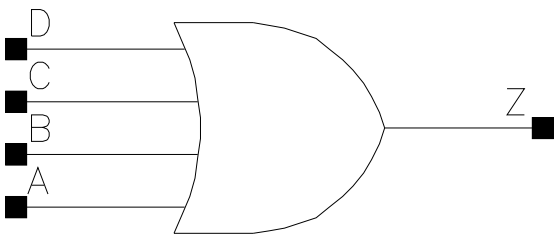
Pin Cycle (vdds)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	-1.479e-08	-1.246e-08	-1.197e-08	4.240e-09
B (output stable)	-2.610e-08	-2.640e-08	-2.540e-08	-2.430e-08
A to Z	-2.943e-07	-6.181e-07	-4.740e-07	-6.029e-07
B to Z	-2.048e-07	-3.773e-07	-3.491e-07	-5.169e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P16	1.200	2.176	2.6112
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P16	X27_P16
A	0.0017	0.0019
B	0.0015	0.0019
C	0.0017	0.0019
D	0.0015	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P16	X27_P16	X20_P16	X27_P16
A to Z ↓	0.0697	0.0720	1.9762	1.4789
A to Z ↑	0.0393	0.0375	1.8045	1.3462
B to Z ↓	0.0653	0.0668	1.9797	1.4778
B to Z ↑	0.0373	0.0351	1.8030	1.3450
C to Z ↓	0.0672	0.0694	1.9741	1.4783
C to Z ↑	0.0374	0.0362	1.8071	1.3509
D to Z ↓	0.0630	0.0648	1.9777	1.4787
D to Z ↑	0.0354	0.0342	1.8074	1.3489

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X20_P16	1.336e-06	2.251e-09
X27_P16	1.913e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X20_P16	X27_P16
A (output stable)	1.543e-03	2.123e-03
B (output stable)	1.234e-03	1.674e-03
C (output stable)	1.471e-03	2.128e-03
D (output stable)	1.120e-03	1.634e-03
A to Z	6.319e-03	8.860e-03
B to Z	5.703e-03	7.943e-03
C to Z	5.507e-03	7.570e-03
D to Z	4.891e-03	6.744e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

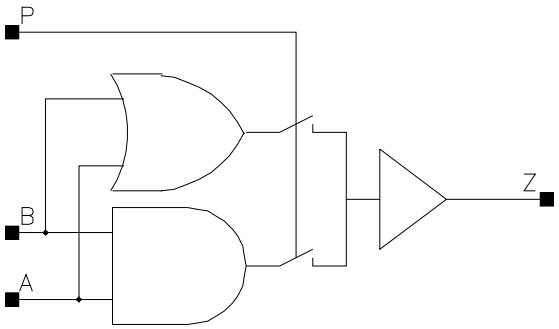
Pin Cycle (vdds)	X20_P16	X27_P16
A (output stable)	-4.559e-06	-9.977e-06
B (output stable)	9.905e-06	2.041e-05
C (output stable)	-1.055e-05	-2.656e-05
D (output stable)	1.420e-05	2.882e-05
A to Z	-3.740e-06	-7.688e-06
B to Z	-3.610e-07	-6.970e-07
C to Z	-3.184e-06	-7.308e-06
D to Z	-1.222e-07	-3.460e-07

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X16_P16	1.200	1.224	1.4688
X25_P16	1.200	2.040	2.4480
X33_P16	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0012	0.0018	0.0031	0.0031
B	0.0011	0.0017	0.0034	0.0034
P	0.0006	0.0009	0.0018	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0855	0.0755	3.1842	1.5519
A to Z ↑	0.0529	0.0474	5.5781	2.7868
B to Z ↓	0.0840	0.0743	3.2095	1.5660
B to Z ↑	0.0542	0.0487	5.5790	2.7879
P to Z ↓	0.0747	0.0665	3.2159	1.5682
P to Z ↑	0.0515	0.0464	5.5782	2.7865
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**

A to Z ↓	0.0718	0.0773	1.0550	0.8029
A to Z ↑	0.0470	0.0497	1.8691	1.4008
B to Z ↓	0.0705	0.0754	1.0618	0.8075
B to Z ↑	0.0486	0.0508	1.8699	1.4023
P to Z ↓	0.0642	0.0693	1.0643	0.8097
P to Z ↑	0.0458	0.0482	1.8682	1.4010

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	4.654e-07	1.179e-09
X16_P16	9.358e-07	1.417e-09
X25_P16	1.519e-06	2.132e-09
X33_P16	1.729e-06	2.251e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	4.564e-05	7.505e-05	1.640e-04	1.626e-04
B (output stable)	1.240e-04	2.036e-04	3.687e-04	3.712e-04
P (output stable)	1.033e-04	1.699e-04	2.955e-04	3.001e-04
A to Z	2.294e-03	3.834e-03	6.711e-03	7.688e-03
B to Z	2.227e-03	3.711e-03	6.446e-03	7.443e-03
P to Z	1.970e-03	3.329e-03	5.868e-03	6.847e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

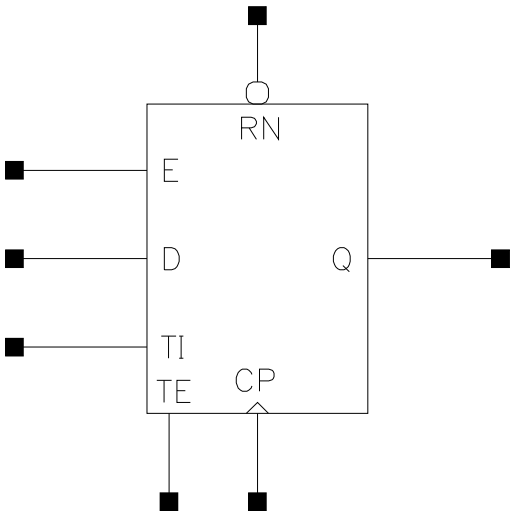
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	-3.236e-06	-4.805e-06	-7.973e-06	-7.944e-06
B (output stable)	-1.192e-05	-1.776e-05	-1.275e-05	-1.358e-05
P (output stable)	1.574e-05	3.034e-05	4.154e-05	4.213e-05
A to Z	-2.801e-06	-4.085e-06	-7.555e-06	-7.936e-06
B to Z	-2.519e-06	-3.501e-06	-5.961e-06	-5.968e-06
P to Z	-5.160e-07	-1.041e-06	-2.430e-06	-2.312e-06

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.488	5.3856
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0007	0.0007	0.0008
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to Q ↓	0.1787	0.0800	7.5373	3.0928
CP to Q ↑	0.1254	0.1018	11.8013	5.5097
RN to Q ↓	0.1346	0.1113	6.1191	3.3556
	X17_P16	X33_P16	X17_P16	X33_P16
CP to Q ↓	0.1391	0.1465	1.4859	0.7841
CP to Q ↑	0.1701	0.1783	2.7045	1.3727
RN to Q ↓	0.1894	0.1966	1.4821	0.7825

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2648	0.1744	0.1701	0.1695
CP ↑	min_pulse_width to CP	0.1699	0.0645	0.0549	0.0549
D ↓	hold_rising to CP	-0.2794	-0.1454	-0.1505	-0.1505
D ↑	hold_rising to CP	-0.1453	-0.0561	-0.0582	-0.0582
D ↓	setup_rising to CP	0.3734	0.2319	0.2326	0.2326
D ↑	setup_rising to CP	0.1951	0.1080	0.1031	0.1031
E ↓	hold_rising to CP	-0.1741	-0.1692	-0.1741	-0.1741
E ↑	hold_rising to CP	-0.1435	-0.0583	-0.0583	-0.0583
E ↓	setup_rising to CP	0.3288	0.3249	0.3249	0.3249
E ↑	setup_rising to CP	0.3593	0.2418	0.2394	0.2369
RN ↓	min_pulse_width to RN	0.1355	0.1480	0.1316	0.1338
RN ↑	recovery_rising to CP	0.0392	0.0416	0.0367	0.0367
RN ↑	removal_rising to CP	-0.0268	-0.0174	-0.0174	-0.0174
TE ↓	hold_rising to CP	-0.1332	-0.1021	-0.1014	-0.1045
TE ↑	hold_rising to CP	-0.1014	-0.0623	-0.0672	-0.0672
TE ↓	setup_rising to CP	0.2441	0.1904	0.1883	0.1883
TE ↑	setup_rising to CP	0.4734	0.3372	0.3352	0.3349
TI ↓	hold_rising to CP	-0.3674	-0.2052	-0.2141	-0.2140
TI ↑	hold_rising to CP	-0.1200	-0.0685	-0.0695	-0.0695
TI ↓	setup_rising to CP	0.4669	0.3074	0.3041	0.3041
TI ↑	setup_rising to CP	0.1659	0.1242	0.1193	0.1193

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.741e-06	4.557e-09
X8_P16	1.890e-06	4.276e-09
X17_P16	2.277e-06	4.514e-09
X33_P16	2.695e-06	4.752e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

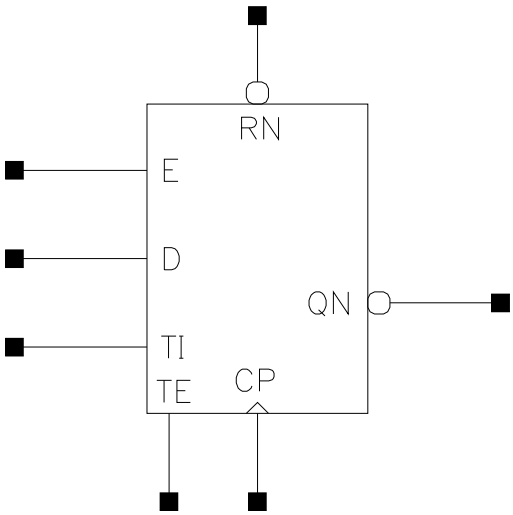
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.636e-03	3.668e-03	3.676e-03	3.680e-03
Clock 100Mhz Data 25Mhz	5.868e-03	6.021e-03	6.609e-03	7.267e-03
Clock 100Mhz Data 50Mhz	8.099e-03	8.375e-03	9.541e-03	1.085e-02
Clock = 0 Data 100Mhz	5.041e-03	4.968e-03	4.944e-03	4.934e-03
Clock = 1 Data 100Mhz	1.993e-03	2.024e-03	2.036e-03	2.041e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.624	5.5488
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to QN ↓	0.1569	0.1420	5.8894	2.9746
CP to QN ↑	0.1937	0.1054	11.5431	5.3810
RN to QN ↑	0.1619	0.1591	11.4966	5.3694
	X17_P16	X33_P16	X17_P16	X33_P16
CP to QN ↓	0.1336	0.1409	1.4891	0.7847
CP to QN ↑	0.1118	0.1215	2.7069	1.3751
RN to QN ↑	0.1598	0.1763	2.7162	1.3815

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2648	0.1744	0.1744	0.1701
CP ↑	min_pulse_width to CP	0.1215	0.0548	0.0645	0.0705
D ↓	hold_rising to CP	-0.2865	-0.1484	-0.1484	-0.1454
D ↑	hold_rising to CP	-0.1453	-0.0561	-0.0561	-0.0561
D ↓	setup_rising to CP	0.3731	0.2319	0.2319	0.2319
D ↑	setup_rising to CP	0.1954	0.1055	0.1054	0.1054
E ↓	hold_rising to CP	-0.1772	-0.1723	-0.1692	-0.1692
E ↑	hold_rising to CP	-0.1435	-0.0579	-0.0579	-0.0579
E ↓	setup_rising to CP	0.3337	0.3249	0.3249	0.3249
E ↑	setup_rising to CP	0.3590	0.2418	0.2418	0.2421
RN ↓	min_pulse_width to RN	0.1306	0.1343	0.1480	0.1599
RN ↑	recovery_rising to CP	0.0367	0.0415	0.0416	0.0419
RN ↑	removal_rising to CP	-0.0268	-0.0171	-0.0174	-0.0174
TE ↓	hold_rising to CP	-0.1358	-0.1014	-0.1021	-0.1021
TE ↑	hold_rising to CP	-0.1014	-0.0653	-0.0623	-0.0623
TE ↓	setup_rising to CP	0.2441	0.1904	0.1904	0.1904
TE ↑	setup_rising to CP	0.4734	0.3370	0.3370	0.3370
TI ↓	hold_rising to CP	-0.3723	-0.2100	-0.2092	-0.2092
TI ↑	hold_rising to CP	-0.1200	-0.0680	-0.0685	-0.0685
TI ↓	setup_rising to CP	0.4615	0.3074	0.3074	0.3080
TI ↑	setup_rising to CP	0.1659	0.1229	0.1228	0.1228

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.828e-06	4.557e-09
X8_P16	2.026e-06	4.395e-09
X17_P16	2.440e-06	4.514e-09
X33_P16	2.986e-06	4.752e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

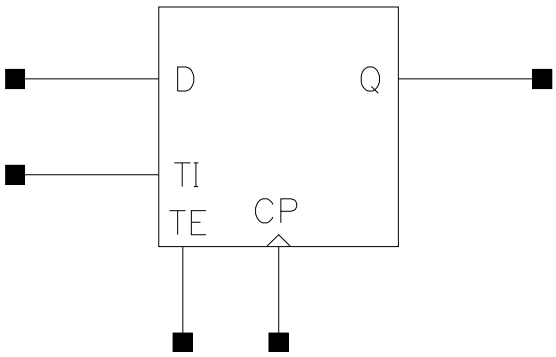
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.637e-03	3.669e-03	3.675e-03	3.679e-03
Clock 100Mhz Data 25Mhz	5.868e-03	6.066e-03	6.555e-03	7.170e-03
Clock 100Mhz Data 50Mhz	8.099e-03	8.463e-03	9.434e-03	1.066e-02
Clock = 0 Data 100Mhz	5.034e-03	4.962e-03	4.940e-03	4.928e-03
Clock = 1 Data 100Mhz	1.993e-03	2.026e-03	2.039e-03	2.045e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.400	4.0800
X8_P16	1.200	3.128	3.7536
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1425	0.0740	6.9824	3.0730
CP to Q ↑	0.1120	0.0919	11.8687	5.4465
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.1138	0.1251	1.4532	0.7695
CP to Q ↑	0.1724	0.1820	2.6962	1.3695

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2262	0.2359	0.2354	0.2330
CP ↑	min_pulse_width to CP	0.1167	0.0548	0.0512	0.0501
D ↓	hold_rising to CP	-0.1724	-0.0826	-0.0850	-0.0850
D ↑	hold_rising to CP	-0.0623	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.2365	0.1590	0.1594	0.1563
D ↑	setup_rising to CP	0.1002	0.0509	0.0484	0.0484
TE ↓	hold_rising to CP	-0.1057	-0.0750	-0.0743	-0.0743
TE ↑	hold_rising to CP	-0.0845	-0.0530	-0.0586	-0.0586
TE ↓	setup_rising to CP	0.2002	0.1539	0.1512	0.1515
TE ↑	setup_rising to CP	0.4179	0.3349	0.3297	0.3297
TI ↓	hold_rising to CP	-0.3445	-0.2204	-0.2267	-0.2267
TI ↑	hold_rising to CP	-0.0954	-0.0547	-0.0560	-0.0560
TI ↓	setup_rising to CP	0.4188	0.3185	0.3185	0.3151
TI ↑	setup_rising to CP	0.1361	0.0962	0.0947	0.0947

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.405e-06	3.323e-09
X8_P16	1.571e-06	3.085e-09
X17_P16	2.130e-06	3.442e-09
X33_P16	2.550e-06	3.680e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

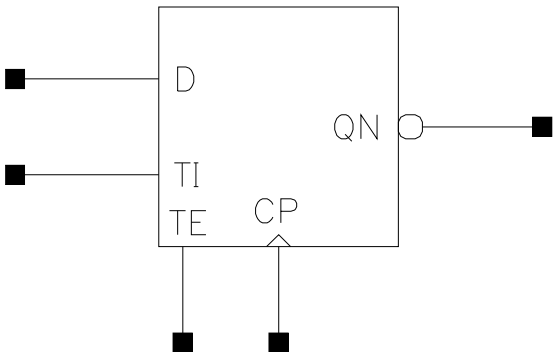
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.248e-03	3.276e-03	3.282e-03	3.286e-03
Clock 100Mhz Data 25Mhz	4.822e-03	4.930e-03	5.498e-03	6.010e-03
Clock 100Mhz Data 50Mhz	6.396e-03	6.584e-03	7.713e-03	8.734e-03
Clock = 0 Data 100Mhz	4.038e-03	3.854e-03	3.792e-03	3.761e-03
Clock = 1 Data 100Mhz	1.141e-03	6.003e-04	4.202e-04	3.301e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.536	4.2432
X8_P16	1.200	3.264	3.9168
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1498	0.1592	6.8101	3.1185
CP to QN ↑	0.1537	0.0974	11.7786	5.3902
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.1127	0.1246	1.4538	0.7710
CP to QN ↑	0.0969	0.1065	2.6929	1.3696

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2256	0.2359	0.2359	0.2359
CP ↑	min_pulse_width to CP	0.0925	0.0512	0.0560	0.0597
D ↓	hold_rising to CP	-0.1720	-0.0850	-0.0826	-0.0826
D ↑	hold_rising to CP	-0.0653	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.2316	0.1590	0.1590	0.1590
D ↑	setup_rising to CP	0.1002	0.0484	0.0509	0.0509
TE ↓	hold_rising to CP	-0.1057	-0.0743	-0.0750	-0.0750
TE ↑	hold_rising to CP	-0.0870	-0.0586	-0.0530	-0.0530
TE ↓	setup_rising to CP	0.1950	0.1508	0.1508	0.1508
TE ↑	setup_rising to CP	0.4127	0.3293	0.3349	0.3349
TI ↓	hold_rising to CP	-0.3494	-0.2267	-0.2204	-0.2203
TI ↑	hold_rising to CP	-0.0964	-0.0560	-0.0552	-0.0547
TI ↓	setup_rising to CP	0.4175	0.3185	0.3185	0.3185
TI ↑	setup_rising to CP	0.1361	0.0947	0.0962	0.0962

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.418e-06	3.442e-09
X8_P16	1.583e-06	3.204e-09
X17_P16	2.122e-06	3.442e-09
X33_P16	2.541e-06	3.680e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

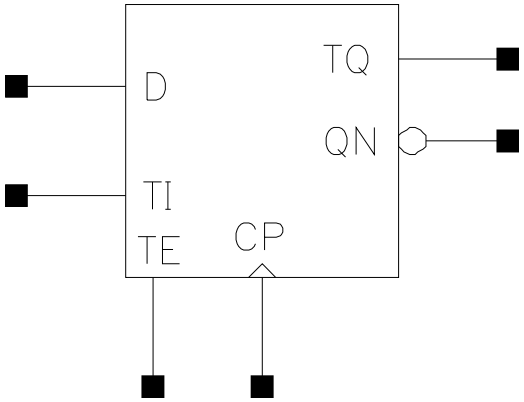
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.215e-03	3.280e-03	3.301e-03	3.311e-03
Clock 100Mhz Data 25Mhz	4.839e-03	5.014e-03	5.485e-03	5.996e-03
Clock 100Mhz Data 50Mhz	6.464e-03	6.748e-03	7.669e-03	8.680e-03
Clock = 0 Data 100Mhz	4.053e-03	3.865e-03	3.802e-03	3.771e-03
Clock = 1 Data 100Mhz	1.134e-03	6.076e-04	4.322e-04	3.446e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.536	4.2432
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1669	0.1356	6.0762	2.9780
CP to QN ↑	0.1897	0.1023	11.4759	5.3911
CP to TQ ↓	0.1318	0.0682	8.8489	5.8527
CP to TQ ↑	0.1162	0.0921	23.9404	16.3023
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.1252	0.1345	1.4920	0.7877
CP to QN ↑	0.1048	0.1116	2.7232	1.3915
CP to TQ ↓	0.0717	0.0752	7.9199	7.9501
CP to TQ ↑	0.0940	0.0967	21.7120	23.0573

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2262	0.2359	0.2359	0.2359
CP ↑	min_pulse_width to CP	0.1167	0.0549	0.0560	0.0608
D ↓	hold_rising to CP	-0.1727	-0.0826	-0.0826	-0.0801
D ↑	hold_rising to CP	-0.0623	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.2368	0.1563	0.1559	0.1559
D ↑	setup_rising to CP	0.1002	0.0509	0.0509	0.0509
TE ↓	hold_rising to CP	-0.1057	-0.0750	-0.0750	-0.0750
TE ↑	hold_rising to CP	-0.0849	-0.0555	-0.0530	-0.0530
TE ↓	setup_rising to CP	0.1975	0.1512	0.1512	0.1512
TE ↑	setup_rising to CP	0.4127	0.3297	0.3297	0.3297
TI ↓	hold_rising to CP	-0.3445	-0.2204	-0.2204	-0.2168
TI ↑	hold_rising to CP	-0.0956	-0.0547	-0.0547	-0.0547
TI ↓	setup_rising to CP	0.4188	0.3144	0.3185	0.3185
TI ↑	setup_rising to CP	0.1361	0.0962	0.0957	0.0962

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.561e-06	3.688e-09
X8_P16	1.773e-06	3.442e-09
X17_P16	2.044e-06	3.561e-09
X33_P16	2.558e-06	3.799e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16

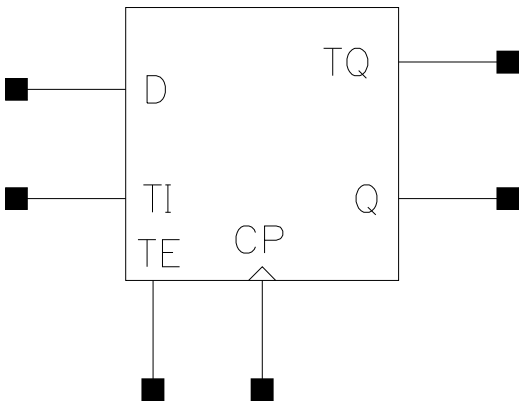
Clock 100Mhz Data 0Mhz	3.325e-03	3.313e-03	3.311e-03	3.311e-03
Clock 100Mhz Data 25Mhz	5.092e-03	5.252e-03	5.478e-03	6.057e-03
Clock 100Mhz Data 50Mhz	6.859e-03	7.191e-03	7.645e-03	8.803e-03
Clock = 0 Data 100Mhz	4.047e-03	3.861e-03	3.800e-03	3.769e-03
Clock = 1 Data 100Mhz	1.141e-03	5.891e-04	4.051e-04	3.131e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.400	4.0800
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007

TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1887	0.0833	7.5578	3.0901
CP to Q ↑	0.1294	0.0976	12.0217	5.4867
CP to TQ ↓	0.1845	0.0897	7.5171	8.0811
CP to TQ ↑	0.1337	0.1098	16.2951	23.3589
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.1169	0.1282	1.4924	0.7844
CP to Q ↑	0.1756	0.1847	2.7408	1.3752
CP to TQ ↓	0.1227	0.1372	7.6656	7.8029
CP to TQ ↑	0.1870	0.2001	22.5883	22.7704

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2256	0.2359	0.2335	0.2330
CP ↑	min_pulse_width to CP	0.1662	0.0645	0.0506	0.0501
D ↓	hold_rising to CP	-0.1724	-0.0801	-0.0850	-0.0850
D ↑	hold_rising to CP	-0.0653	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.2316	0.1559	0.1563	0.1563
D ↑	setup_rising to CP	0.1002	0.0509	0.0484	0.0484
TE ↓	hold_rising to CP	-0.1057	-0.0725	-0.0743	-0.0743
TE ↑	hold_rising to CP	-0.0867	-0.0530	-0.0586	-0.0583
TE ↓	setup_rising to CP	0.1953	0.1512	0.1512	0.1515
TE ↑	setup_rising to CP	0.4130	0.3297	0.3297	0.3297
TI ↓	hold_rising to CP	-0.3486	-0.2170	-0.2267	-0.2267
TI ↑	hold_rising to CP	-0.0964	-0.0552	-0.0560	-0.0560
TI ↓	setup_rising to CP	0.4175	0.3185	0.3185	0.3151
TI ↑	setup_rising to CP	0.1366	0.0962	0.0947	0.0947

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.564e-06	3.561e-09
X8_P16	1.679e-06	3.323e-09
X17_P16	2.214e-06	3.561e-09
X33_P16	2.628e-06	3.799e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

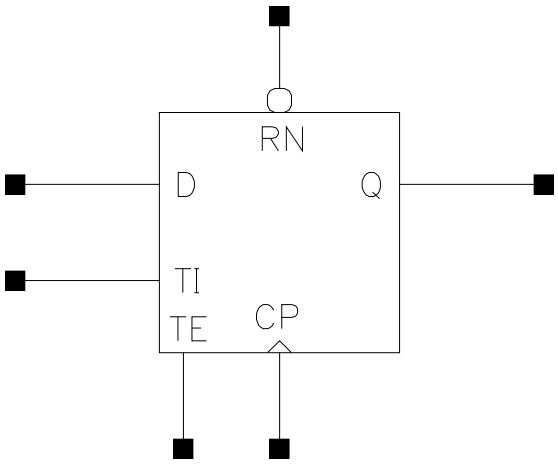
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.235e-03	3.270e-03	3.278e-03	3.283e-03
Clock 100Mhz Data 25Mhz	5.043e-03	5.102e-03	5.658e-03	6.198e-03
Clock 100Mhz Data 50Mhz	6.852e-03	6.934e-03	8.039e-03	9.112e-03
Clock = 0 Data 100Mhz	4.029e-03	3.847e-03	3.788e-03	3.758e-03
Clock = 1 Data 100Mhz	1.132e-03	5.845e-04	4.021e-04	3.109e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.672	4.4064
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
RN	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1743	0.0798	7.7184	3.1007
CP to Q ↑	0.1234	0.0997	11.8715	5.5054
RN to Q ↓	0.1325	0.1118	6.2447	3.3289
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.1191	0.1310	1.4769	0.7826
CP to Q ↑	0.1498	0.1583	2.6951	1.3710
RN to Q ↓	0.1701	0.1820	1.4693	0.7798

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2570	0.2450	0.2475	0.2475
CP ↑	min_pulse_width to CP	0.1517	0.0597	0.0512	0.0512
D ↓	hold_rising to CP	-0.1524	-0.0631	-0.0654	-0.0680
D ↑	hold_rising to CP	-0.0751	-0.0241	-0.0262	-0.0262
D ↓	setup_rising to CP	0.2368	0.1514	0.1514	0.1514
D ↑	setup_rising to CP	0.1170	0.0711	0.0686	0.0686
RN ↓	min_pulse_width to RN	0.1328	0.1382	0.1343	0.1321
RN ↑	recovery_rising to CP	0.0418	0.0468	0.0416	0.0419
RN ↑	removal_rising to CP	-0.0293	-0.0198	-0.0171	-0.0171
TE ↓	hold_rising to CP	-0.1164	-0.0609	-0.0631	-0.0631
TE ↑	hold_rising to CP	-0.1021	-0.0628	-0.0680	-0.0676
TE ↓	setup_rising to CP	0.2006	0.1459	0.1463	0.1466
TE ↑	setup_rising to CP	0.4127	0.3199	0.3255	0.3199
TI ↓	hold_rising to CP	-0.3186	-0.1875	-0.1959	-0.1959
TI ↑	hold_rising to CP	-0.1116	-0.0665	-0.0699	-0.0714
TI ↓	setup_rising to CP	0.4175	0.3087	0.3087	0.3092
TI ↑	setup_rising to CP	0.1610	0.1206	0.1206	0.1208

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.535e-06	3.799e-09
X8_P16	1.668e-06	3.561e-09
X17_P16	2.174e-06	3.918e-09
X33_P16	2.497e-06	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.644e-03	3.679e-03	3.706e-03	3.721e-03

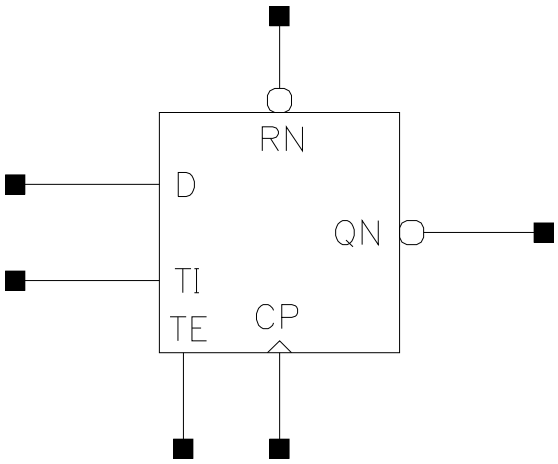
Clock 100Mhz Data 25Mhz	5.433e-03	5.459e-03	6.148e-03	6.714e-03
Clock 100Mhz Data 50Mhz	7.222e-03	7.238e-03	8.590e-03	9.708e-03
Clock = 0 Data 100Mhz	4.179e-03	3.921e-03	3.834e-03	3.791e-03
Clock = 1 Data 100Mhz	1.160e-03	6.390e-04	4.651e-04	3.784e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	3.944	4.7328
X33_P16	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1406	0.1260	5.7248	2.8815
CP to QN ↑	0.1770	0.0951	11.5236	5.3520
RN to QN ↑	0.1502	0.1500	11.4839	5.3356
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.1231	0.1361	1.4745	0.7827
CP to QN ↑	0.1069	0.1183	2.7082	1.3857
RN to QN ↑	0.1562	0.1728	2.7202	1.3892

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2570	0.2450	0.2450	0.2432
CP ↑	min_pulse_width to CP	0.1119	0.0511	0.0645	0.0693
D ↓	hold_rising to CP	-0.1577	-0.0654	-0.0627	-0.0658
D ↑	hold_rising to CP	-0.0751	-0.0237	-0.0241	-0.0237
D ↓	setup_rising to CP	0.2368	0.1514	0.1545	0.1514
D ↑	setup_rising to CP	0.1174	0.0686	0.0686	0.0686
RN ↓	min_pulse_width to RN	0.1306	0.1294	0.1475	0.1572
RN ↑	recovery_rising to CP	0.0388	0.0464	0.0468	0.0468
RN ↑	removal_rising to CP	-0.0268	-0.0223	-0.0198	-0.0198
TE ↓	hold_rising to CP	-0.1186	-0.0606	-0.0606	-0.0606
TE ↑	hold_rising to CP	-0.1020	-0.0653	-0.0627	-0.0653
TE ↓	setup_rising to CP	0.2006	0.1463	0.1490	0.1463
TE ↑	setup_rising to CP	0.4127	0.3199	0.3251	0.3199
TI ↓	hold_rising to CP	-0.3235	-0.1926	-0.1870	-0.1911
TI ↑	hold_rising to CP	-0.1111	-0.0660	-0.0665	-0.0660
TI ↓	setup_rising to CP	0.4175	0.3047	0.3087	0.3087
TI ↑	setup_rising to CP	0.1556	0.1208	0.1206	0.1206

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.634e-06	3.844e-09
X8_P16	1.805e-06	3.680e-09
X17_P16	2.261e-06	3.799e-09
X33_P16	2.755e-06	4.037e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.602e-03	3.631e-03	3.640e-03	3.644e-03

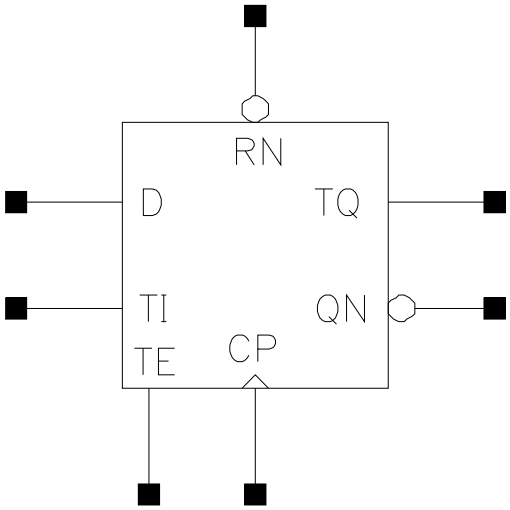
Clock 100Mhz Data 25Mhz	5.375e-03	5.465e-03	5.971e-03	6.499e-03
Clock 100Mhz Data 50Mhz	7.148e-03	7.299e-03	8.302e-03	9.353e-03
Clock = 0 Data 100Mhz	4.183e-03	3.927e-03	3.845e-03	3.804e-03
Clock = 1 Data 100Mhz	1.159e-03	6.139e-04	4.320e-04	3.413e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007

RN	0.0010	0.0007	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1588	0.1308	5.7363	3.0191
CP to QN ↑	0.2364	0.1088	10.1649	5.5374
CP to TQ ↓	0.1674	0.0732	8.0493	6.1240
CP to TQ ↑	0.1292	0.1015	18.6400	17.1065
RN to QN ↑	0.1505	0.1499	10.2971	5.5222
RN to TQ ↓	0.1020	0.1001	6.9131	6.5502
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.1344	0.1436	1.5019	0.7952
CP to QN ↑	0.1093	0.1145	2.7533	1.3844
CP to TQ ↓	0.0768	0.0802	7.6844	7.5267
CP to TQ ↑	0.1017	0.1043	15.9043	16.1142
RN to QN ↑	0.1539	0.1630	2.7489	1.3821
RN to TQ ↓	0.1076	0.1139	8.1274	8.0007

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2570	0.2450	0.2480	0.2480
CP ↑	min_pulse_width to CP	0.1651	0.0597	0.0597	0.0645
D ↓	hold_rising to CP	-0.1577	-0.0658	-0.0631	-0.0631
D ↑	hold_rising to CP	-0.0751	-0.0237	-0.0237	-0.0237
D ↓	setup_rising to CP	0.2368	0.1514	0.1511	0.1511
D ↑	setup_rising to CP	0.1170	0.0711	0.0711	0.0711
RN ↓	min_pulse_width to RN	0.1355	0.1355	0.1404	0.1501
RN ↑	recovery_rising to CP	0.0415	0.0468	0.0468	0.0468
RN ↑	removal_rising to CP	-0.0317	-0.0198	-0.0198	-0.0198
TE ↓	hold_rising to CP	-0.1190	-0.0606	-0.0606	-0.0582
TE ↑	hold_rising to CP	-0.1020	-0.0627	-0.0683	-0.0683
TE ↓	setup_rising to CP	0.2002	0.1463	0.1459	0.1459
TE ↑	setup_rising to CP	0.4127	0.3199	0.3195	0.3195
TI ↓	hold_rising to CP	-0.3201	-0.1870	-0.1870	-0.1875
TI ↑	hold_rising to CP	-0.1111	-0.0665	-0.0658	-0.0658
TI ↓	setup_rising to CP	0.4189	0.3047	0.3087	0.3087
TI ↑	setup_rising to CP	0.1610	0.1206	0.1206	0.1206

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.706e-06	3.918e-09
X8_P16	1.888e-06	3.680e-09
X17_P16	2.250e-06	3.918e-09
X33_P16	2.823e-06	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

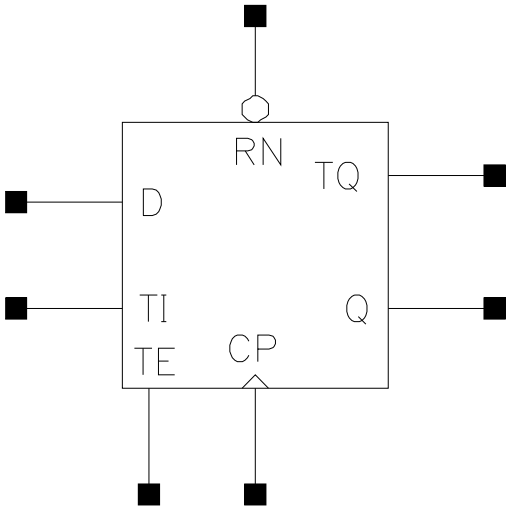
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.612e-03	3.658e-03	3.691e-03	3.708e-03
Clock 100Mhz Data 25Mhz	5.552e-03	5.623e-03	5.916e-03	6.515e-03
Clock 100Mhz Data 50Mhz	7.492e-03	7.589e-03	8.140e-03	9.323e-03
Clock = 0 Data 100Mhz	4.173e-03	3.916e-03	3.827e-03	3.783e-03
Clock = 1 Data 100Mhz	1.159e-03	6.277e-04	4.502e-04	3.616e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007

RN	0.0008	0.0008	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1970	0.0869	8.1714	3.1854
CP to Q ↑	0.1325	0.1039	12.2616	5.6686
CP to TQ ↓	0.1922	0.0903	10.1157	8.1734
CP to TQ ↑	0.1391	0.1118	25.8817	23.2456
RN to Q ↓	0.1377	0.1279	6.5343	3.4550
RN to TQ ↓	0.1363	0.1326	8.3731	8.6657
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.1228	0.1354	1.4955	0.7949
CP to Q ↑	0.1506	0.1596	2.7011	1.3742
CP to TQ ↓	0.1287	0.1459	7.7219	7.8454
CP to TQ ↑	0.1614	0.1758	22.7835	22.8637
RN to Q ↓	0.1741	0.1866	1.4912	0.7920
RN to TQ ↓	0.1799	0.1972	7.7165	7.8397

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2552	0.2450	0.2432	0.2421
CP ↑	min_pulse_width to CP	0.1758	0.0682	0.0511	0.0511
D ↓	hold_rising to CP	-0.1580	-0.0631	-0.0654	-0.0654
D ↑	hold_rising to CP	-0.0751	-0.0241	-0.0237	-0.0237
D ↓	setup_rising to CP	0.2316	0.1514	0.1514	0.1489
D ↑	setup_rising to CP	0.1171	0.0711	0.0686	0.0686
RN ↓	min_pulse_width to RN	0.1377	0.1550	0.1294	0.1294
RN ↑	recovery_rising to CP	0.0367	0.0464	0.0416	0.0416
RN ↑	removal_rising to CP	-0.0268	-0.0223	-0.0198	-0.0198
TE ↓	hold_rising to CP	-0.1164	-0.0582	-0.0631	-0.0631
TE ↑	hold_rising to CP	-0.1017	-0.0627	-0.0683	-0.0680
TE ↓	setup_rising to CP	0.1953	0.1463	0.1466	0.1466
TE ↑	setup_rising to CP	0.4130	0.3199	0.3199	0.3202
TI ↓	hold_rising to CP	-0.3201	-0.1862	-0.1919	-0.1959
TI ↑	hold_rising to CP	-0.1111	-0.0650	-0.0658	-0.0658
TI ↓	setup_rising to CP	0.4175	0.3087	0.3053	0.3053
TI ↑	setup_rising to CP	0.1595	0.1206	0.1193	0.1157

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.603e-06	3.918e-09
X8_P16	1.730e-06	3.680e-09
X17_P16	2.206e-06	3.918e-09
X33_P16	2.531e-06	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

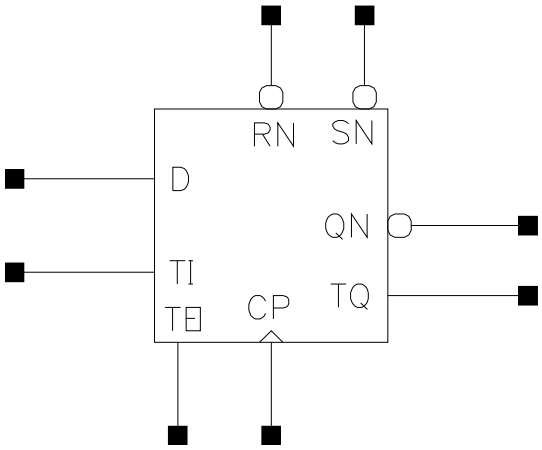
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.642e-03	3.677e-03	3.688e-03	3.693e-03
Clock 100Mhz Data 25Mhz	5.534e-03	5.573e-03	6.260e-03	6.844e-03
Clock 100Mhz Data 50Mhz	7.426e-03	7.469e-03	8.832e-03	9.995e-03
Clock = 0 Data 100Mhz	4.177e-03	3.920e-03	3.835e-03	3.792e-03
Clock = 1 Data 100Mhz	1.161e-03	6.012e-04	4.148e-04	3.216e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.352	5.2224
X17_P16	1.200	4.488	5.3856
X33_P16	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0008	0.0008	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.1444	0.1538	2.9334	1.5249
CP to QN ↑	0.1152	0.1205	5.3700	2.7140
CP to TQ ↓	0.0871	0.0870	9.9859	9.9765
CP to TQ ↑	0.1196	0.1198	31.7222	31.7363
RN to QN ↓	0.1627	0.1721	2.9296	1.5250
RN to QN ↑	0.1718	0.1804	5.3854	2.7196
RN to TQ ↓	0.1299	0.1295	10.9576	10.9562
RN to TQ ↑	0.1387	0.1388	31.6800	31.6514
SN to QN ↓	0.1757	0.1870	2.9522	1.5315
SN to TQ ↑	0.1481	0.1478	31.9812	32.0385
	X33_P16		**X33_P16**	
CP to QN ↓	0.1767		0.8244	
CP to QN ↑	0.1334		1.3872	
CP to TQ ↓	0.0871		9.9911	
CP to TQ ↑	0.1203		31.7473	
RN to QN ↓	0.1947		0.8254	
RN to QN ↑	0.1984		1.3901	
RN to TQ ↓	0.1296		10.9640	
RN to TQ ↑	0.1392		31.7244	
SN to QN ↓	0.2125		0.8253	
SN to TQ ↑	0.1483		32.0924	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2577	0.2577	0.2577
CP ↑	min_pulse_width to CP	0.0645	0.0693	0.0742
D ↓	hold_rising to CP	-0.0631	-0.0631	-0.0631
D ↑	hold_rising to CP	-0.0237	-0.0237	-0.0237
D ↓	setup_rising to CP	0.1612	0.1612	0.1612
D ↑	setup_rising to CP	0.0760	0.0760	0.0760
RN ↓	min_pulse_width to RN	0.1501	0.1572	0.1697
RN ↑	non_seq_hold_rising to SN	-0.0628	-0.0628	-0.0628
RN ↑	non_seq_setup_rising to SN	0.1394	0.1394	0.1394
RN ↑	recovery_rising to CP	0.0662	0.0662	0.0662
RN ↑	removal_rising to CP	-0.0366	-0.0366	-0.0366
SN ↓	min_pulse_width to SN	0.1206	0.1260	0.1357
SN ↑	recovery_rising to CP	0.0250	0.0250	0.0250
SN ↑	removal_rising to CP	0.0603	0.0603	0.0603

TE ↓	hold_rising to CP	-0.0579	-0.0609	-0.0579
TE ↑	hold_rising to CP	-0.0628	-0.0653	-0.0653
TE ↓	setup_rising to CP	0.1561	0.1561	0.1561
TE ↑	setup_rising to CP	0.3297	0.3297	0.3297
TI ↓	hold_rising to CP	-0.1870	-0.1870	-0.1870
TI ↑	hold_rising to CP	-0.0665	-0.0665	-0.0665
TI ↓	setup_rising to CP	0.3185	0.3185	0.3185
TI ↑	setup_rising to CP	0.1255	0.1255	0.1255

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	2.051e-06	4.169e-09
X17_P16	2.334e-06	4.288e-09
X33_P16	2.804e-06	4.527e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

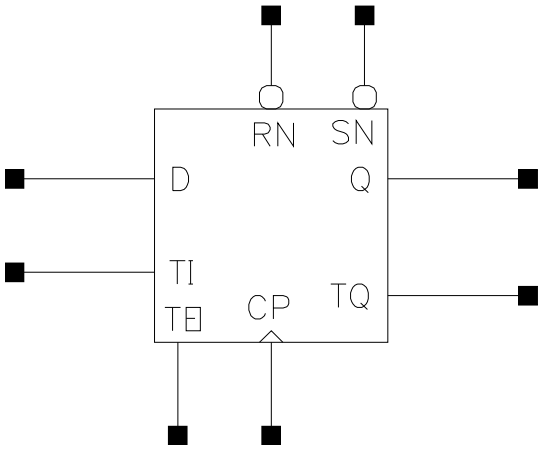
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.875e-03	3.875e-03	3.876e-03
Clock 100Mhz Data 25Mhz	5.894e-03	6.130e-03	6.713e-03
Clock 100Mhz Data 50Mhz	7.912e-03	8.386e-03	9.551e-03
Clock = 0 Data 100Mhz	3.816e-03	3.815e-03	3.816e-03
Clock = 1 Data 100Mhz	1.160e-04	1.158e-04	1.161e-04

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.216	5.0592
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0008	0.0008	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0955	0.1073	3.1137	1.6338
CP to Q ↑	0.1137	0.1192	5.4996	2.7971
CP to TQ ↓	0.1026	0.1206	10.1314	10.2491
CP to TQ ↑	0.1291	0.1424	30.4409	30.5973
RN to Q ↓	0.1481	0.1720	3.7201	1.9702
RN to Q ↑	0.1059	0.1184	5.7498	2.9447
RN to TQ ↓	0.1585	0.1913	11.2921	11.5778
RN to TQ ↑	0.1320	0.1577	30.7608	30.9707
SN to Q ↑	0.1433	0.1556	5.7526	2.9459
SN to TQ ↑	0.1694	0.1950	30.7693	30.9738
	X33_P16		**X33_P16**	
CP to Q ↓	0.1375		0.8963	
CP to Q ↑	0.1352		1.4500	
CP to TQ ↓	0.1526		10.6183	
CP to TQ ↑	0.1674		30.8910	
RN to Q ↓	0.2311		1.1113	
RN to Q ↑	0.1514		1.5487	
RN to TQ ↓	0.2482		12.3878	
RN to TQ ↑	0.2076		31.3716	
SN to Q ↑	0.1886		1.5493	
SN to TQ ↑	0.2449		31.3717	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2577	0.2571	0.2529
CP ↑	min_pulse_width to CP	0.0742	0.0887	0.1226
D ↓	hold_rising to CP	-0.0631	-0.0606	-0.0606
D ↑	hold_rising to CP	-0.0241	-0.0241	-0.0237
D ↓	setup_rising to CP	0.1612	0.1612	0.1594
D ↑	setup_rising to CP	0.0791	0.0760	0.0760
RN ↓	min_pulse_width to RN	0.1697	0.2039	0.2722
RN ↑	non_seq_hold_rising to SN	-0.0678	-0.0797	-0.1091
RN ↑	non_seq_setup_rising to SN	0.1323	0.1323	0.1726
RN ↑	recovery_rising to CP	0.0593	0.0593	0.0565
RN ↑	removal_rising to CP	-0.0295	-0.0295	-0.0295
SN ↓	min_pulse_width to SN	0.1379	0.1575	0.2041
SN ↑	recovery_rising to CP	0.0250	0.0250	0.0225
SN ↑	removal_rising to CP	0.0603	0.0603	0.0603

TE ↓	hold_rising to CP	-0.0582	-0.0582	-0.0582
TE ↑	hold_rising to CP	-0.0628	-0.0628	-0.0653
TE ↓	setup_rising to CP	0.1561	0.1564	0.1539
TE ↑	setup_rising to CP	0.3297	0.3297	0.3304
TI ↓	hold_rising to CP	-0.1862	-0.1821	-0.1821
TI ↑	hold_rising to CP	-0.0650	-0.0650	-0.0660
TI ↓	setup_rising to CP	0.3185	0.3190	0.3136
TI ↑	setup_rising to CP	0.1255	0.1255	0.1255

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P16	1.958e-06	4.046e-09
X17_P16	2.175e-06	4.165e-09
X33_P16	2.545e-06	4.403e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

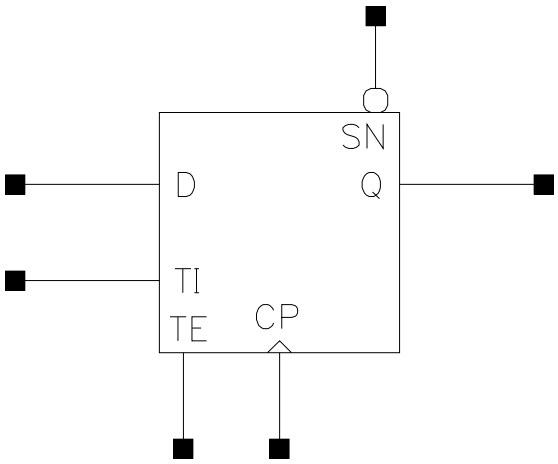
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.814e-03	3.815e-03	3.815e-03
Clock 100Mhz Data 25Mhz	5.741e-03	5.994e-03	6.621e-03
Clock 100Mhz Data 50Mhz	7.669e-03	8.173e-03	9.427e-03
Clock = 0 Data 100Mhz	3.811e-03	3.812e-03	3.811e-03
Clock = 1 Data 100Mhz	9.651e-05	9.672e-05	9.686e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0014	0.0014	0.0014	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P16			

CP	0.0009			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1756	0.0836	7.7453	3.0881
CP to Q ↑	0.1306	0.1044	11.9967	5.4836
SN to Q ↑	0.0972	0.1095	11.6624	5.5006
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to Q ↓	0.1179	0.1245	1.4780	1.0261
CP to Q ↑	0.1502	0.1553	2.6916	1.8238
SN to Q ↑	0.1553	0.1604	2.6954	1.8236
	X33_P16		**X33_P16**	
CP to Q ↓	0.1297		0.7830	
CP to Q ↑	0.1586		1.3734	
SN to Q ↑	0.1637		1.3716	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.2594	0.2577	0.2571	0.2552
CP ↑	min_pulse_width to CP	0.1554	0.0597	0.0512	0.0512
D ↓	hold_rising to CP	-0.1573	-0.0703	-0.0728	-0.0728
D ↑	hold_rising to CP	-0.0698	-0.0213	-0.0213	-0.0244
D ↓	setup_rising to CP	0.2364	0.1636	0.1612	0.1612
D ↑	setup_rising to CP	0.1100	0.0558	0.0561	0.0561
SN ↓	min_pulse_width to SN	0.0833	0.0979	0.0930	0.0930
SN ↑	recovery_rising to CP	0.0202	0.0250	0.0225	0.0225
SN ↑	removal_rising to CP	0.0432	0.0606	0.0606	0.0606
TE ↓	hold_rising to CP	-0.1137	-0.0654	-0.0680	-0.0680
TE ↑	hold_rising to CP	-0.0968	-0.0579	-0.0634	-0.0634
TE ↓	setup_rising to CP	0.2055	0.1587	0.1591	0.1561
TE ↑	setup_rising to CP	0.4179	0.3346	0.3346	0.3346
TI ↓	hold_rising to CP	-0.3201	-0.1967	-0.2057	-0.2057
TI ↑	hold_rising to CP	-0.1062	-0.0616	-0.0609	-0.0609
TI ↓	setup_rising to CP	0.4224	0.3234	0.3200	0.3200
TI ↑	setup_rising to CP	0.1512	0.1059	0.1046	0.1046
		X33_P16			

CP ↓	min_pulse_width to CP	0.2552			
CP ↑	min_pulse_width to CP	0.0501			
D ↓	hold_rising to CP	-0.0728			
D ↑	hold_rising to CP	-0.0241			
D ↓	setup_rising to CP	0.1612			
D ↑	setup_rising to CP	0.0561			
SN ↓	min_pulse_width to SN	0.0930			
SN ↑	recovery_rising to CP	0.0225			
SN ↑	removal_rising to CP	0.0606			
TE ↓	hold_rising to CP	-0.0679			
TE ↑	hold_rising to CP	-0.0634			
TE ↓	setup_rising to CP	0.1561			
TE ↑	setup_rising to CP	0.3349			
TI ↓	hold_rising to CP	-0.2057			
TI ↑	hold_rising to CP	-0.0609			
TI ↓	setup_rising to CP	0.3200			
TI ↑	setup_rising to CP	0.1046			

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.639e-06	3.799e-09
X8_P16	1.807e-06	3.680e-09
X17_P16	2.267e-06	3.918e-09
X25_P16	2.516e-06	4.038e-09
X33_P16	2.761e-06	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	3.536e-03	3.619e-03	3.647e-03	3.660e-03
Clock 100Mhz Data 25Mhz	5.308e-03	5.451e-03	6.090e-03	6.404e-03
Clock 100Mhz Data 50Mhz	7.080e-03	7.282e-03	8.534e-03	9.147e-03
Clock = 0 Data 100Mhz	4.060e-03	3.877e-03	3.817e-03	3.786e-03
Clock = 1 Data 100Mhz	1.160e-03	6.168e-04	4.356e-04	3.451e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	3.669e-03			

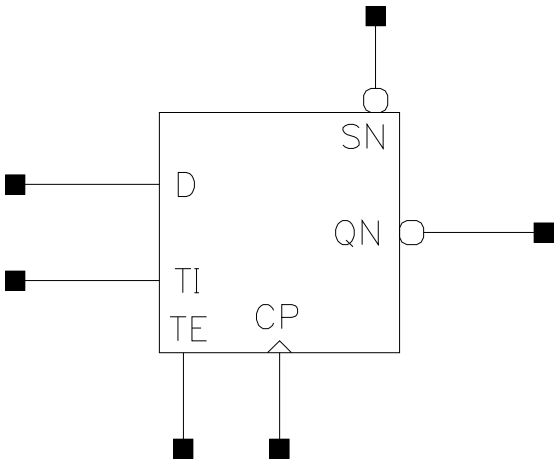
Clock 100Mhz Data 25Mhz	6.650e-03			
Clock 100Mhz Data 50Mhz	9.632e-03			
Clock = 0 Data 100Mhz	3.768e-03			
Clock = 1 Data 100Mhz	2.907e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0014	0.0013	0.0013	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P16			

CP	0.0009			
D	0.0004			
SN	0.0013			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1484	0.1273	5.7225	2.8808
CP to QN ↑	0.1799	0.0953	11.4978	5.3715
SN to QN ↓	0.1178	0.1319	5.6966	2.8801
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to QN ↓	0.1317	0.1393	1.4831	1.0293
CP to QN ↑	0.1151	0.1217	2.6967	1.8249
SN to QN ↓	0.1391	0.1470	1.4821	1.0296
	X33_P16		**X33_P16**	
CP to QN ↓	0.1453		0.7867	
CP to QN ↑	0.1263		1.3739	
SN to QN ↓	0.1529		0.7861	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.2594	0.2577	0.2571	0.2571
CP ↑	min_pulse_width to CP	0.1130	0.0512	0.0694	0.0694
D ↓	hold_rising to CP	-0.1573	-0.0728	-0.0703	-0.0703
D ↑	hold_rising to CP	-0.0724	-0.0213	-0.0213	-0.0213
D ↓	setup_rising to CP	0.2416	0.1636	0.1643	0.1612
D ↑	setup_rising to CP	0.1100	0.0558	0.0558	0.0558
SN ↓	min_pulse_width to SN	0.0833	0.0930	0.1055	0.1055
SN ↑	recovery_rising to CP	0.0202	0.0250	0.0250	0.0250
SN ↑	removal_rising to CP	0.0432	0.0610	0.0606	0.0606
TE ↓	hold_rising to CP	-0.1133	-0.0680	-0.0654	-0.0654
TE ↑	hold_rising to CP	-0.0968	-0.0604	-0.0579	-0.0604
TE ↓	setup_rising to CP	0.2055	0.1587	0.1587	0.1591
TE ↑	setup_rising to CP	0.4179	0.3346	0.3346	0.3346
TI ↓	hold_rising to CP	-0.3235	-0.2016	-0.2008	-0.2008
TI ↑	hold_rising to CP	-0.1062	-0.0611	-0.0596	-0.0611
TI ↓	setup_rising to CP	0.4189	0.3234	0.3200	0.3200
TI ↑	setup_rising to CP	0.1512	0.1045	0.1059	0.1046
		X33_P16			

CP ↓	min_pulse_width to CP	0.2552			
CP ↑	min_pulse_width to CP	0.0743			
D ↓	hold_rising to CP	-0.0703			
D ↑	hold_rising to CP	-0.0213			
D ↓	setup_rising to CP	0.1612			
D ↑	setup_rising to CP	0.0558			
SN ↓	min_pulse_width to SN	0.1082			
SN ↑	recovery_rising to CP	0.0225			
SN ↑	removal_rising to CP	0.0606			
TE ↓	hold_rising to CP	-0.0680			
TE ↑	hold_rising to CP	-0.0604			
TE ↓	setup_rising to CP	0.1561			
TE ↑	setup_rising to CP	0.3346			
TI ↓	hold_rising to CP	-0.2008			
TI ↑	hold_rising to CP	-0.0611			
TI ↓	setup_rising to CP	0.3200			
TI ↑	setup_rising to CP	0.1046			

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.561e-06	3.799e-09
X8_P16	1.667e-06	3.680e-09
X17_P16	2.153e-06	3.918e-09
X25_P16	2.313e-06	4.038e-09
X33_P16	2.476e-06	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	3.525e-03	3.610e-03	3.635e-03	3.647e-03
Clock 100Mhz Data 25Mhz	5.270e-03	5.440e-03	6.057e-03	6.361e-03
Clock 100Mhz Data 50Mhz	7.015e-03	7.269e-03	8.480e-03	9.074e-03
Clock = 0 Data 100Mhz	4.061e-03	3.881e-03	3.818e-03	3.787e-03
Clock = 1 Data 100Mhz	1.160e-03	6.236e-04	4.448e-04	3.555e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	3.654e-03			

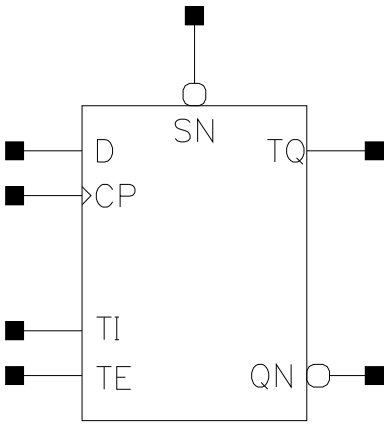
Clock 100Mhz Data 25Mhz	6.609e-03			
Clock 100Mhz Data 50Mhz	9.563e-03			
Clock = 0 Data 100Mhz	3.769e-03			
Clock = 1 Data 100Mhz	3.018e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.216	5.0592
X8_P16	1.200	4.080	4.8960
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0016	0.0015	0.0015
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1728	0.1348	5.6979	2.8885
CP to QN ↑	0.2389	0.1095	11.2900	5.4366
CP to TQ ↓	0.1710	0.0751	9.1831	7.1369
CP to TQ ↑	0.1311	0.1001	16.2747	15.8445
SN to QN ↓	0.1113	0.1148	5.6900	2.8878
SN to TQ ↑	0.0759	0.0784	15.9641	15.9042
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.1329	0.1470	1.5084	0.7776
CP to QN ↑	0.1246	0.1367	2.7040	1.3745
CP to TQ ↓	0.0952	0.0951	7.4812	7.4827
CP to TQ ↑	0.1129	0.1130	15.9470	15.9776
SN to QN ↓	0.1149	0.1290	1.5078	0.7757
SN to TQ ↑	0.0939	0.0940	15.9470	15.9921

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2594	0.2582	0.2577	0.2577
CP ↑	min_pulse_width to CP	0.1651	0.0597	0.0742	0.0828
D ↓	hold_rising to CP	-0.1573	-0.0703	-0.0703	-0.0703
D ↑	hold_rising to CP	-0.0724	-0.0213	-0.0188	-0.0188
D ↓	setup_rising to CP	0.2364	0.1636	0.1636	0.1636
D ↑	setup_rising to CP	0.1100	0.0558	0.0558	0.0558
SN ↓	min_pulse_width to SN	0.0762	0.0784	0.0811	0.0837
SN ↑	recovery_rising to CP	0.0228	0.0250	0.0250	0.0250
SN ↑	removal_rising to CP	0.0432	0.0606	0.0606	0.0606
TE ↓	hold_rising to CP	-0.1133	-0.0680	-0.0654	-0.0654
TE ↑	hold_rising to CP	-0.0968	-0.0579	-0.0579	-0.0579
TE ↓	setup_rising to CP	0.2051	0.1587	0.1587	0.1587
TE ↑	setup_rising to CP	0.4179	0.3346	0.3346	0.3346
TI ↓	hold_rising to CP	-0.3201	-0.2008	-0.1967	-0.1967
TI ↑	hold_rising to CP	-0.1062	-0.0596	-0.0601	-0.0601
TI ↓	setup_rising to CP	0.4224	0.3234	0.3234	0.3234
TI ↑	setup_rising to CP	0.1512	0.1059	0.1059	0.1059

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.741e-06	4.037e-09
X8_P16	1.845e-06	3.918e-09
X17_P16	2.332e-06	4.157e-09
X33_P16	2.655e-06	4.395e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

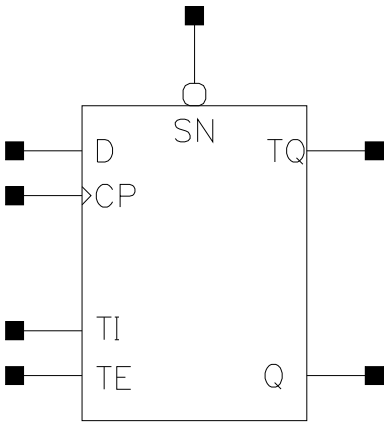
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.524e-03	3.610e-03	3.640e-03	3.654e-03
Clock 100Mhz Data 25Mhz	5.505e-03	5.634e-03	6.171e-03	6.713e-03
Clock 100Mhz Data 50Mhz	7.485e-03	7.657e-03	8.702e-03	9.772e-03
Clock = 0 Data 100Mhz	4.065e-03	3.882e-03	3.821e-03	3.790e-03
Clock = 1 Data 100Mhz	1.161e-03	6.011e-04	4.147e-04	3.215e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.944	4.7328
X17_P16	1.200	4.216	5.0592
X33_P16	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0014	0.0014	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.2031	0.0898	8.0387	3.1625
CP to Q ↑	0.1400	0.1081	12.0816	5.5411
CP to TQ ↓	0.2050	0.0968	11.6600	8.2078
CP to TQ ↑	0.1390	0.1219	16.3905	23.4331
SN to Q ↑	0.0807	0.1139	11.6907	5.5571
SN to TQ ↑	0.0798	0.1302	16.0000	23.4120
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.1207	0.1325	1.5138	0.7984
CP to Q ↑	0.1525	0.1607	2.7061	1.3780
CP to TQ ↓	0.1266	0.1428	7.7221	7.8338
CP to TQ ↑	0.1635	0.1767	22.7914	22.9002
SN to Q ↑	0.1574	0.1655	2.7050	1.3762
SN to TQ ↑	0.1684	0.1815	22.7933	22.8976

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.2576	0.2577	0.2571	0.2534
CP ↑	min_pulse_width to CP	0.1806	0.0683	0.0512	0.0501
D ↓	hold_rising to CP	-0.1573	-0.0676	-0.0728	-0.0728
D ↑	hold_rising to CP	-0.0724	-0.0213	-0.0244	-0.0241
D ↓	setup_rising to CP	0.2365	0.1636	0.1612	0.1612
D ↑	setup_rising to CP	0.1100	0.0589	0.0561	0.0561
SN ↓	min_pulse_width to SN	0.0708	0.1082	0.0930	0.0930
SN ↑	recovery_rising to CP	0.0202	0.0250	0.0225	0.0225
SN ↑	removal_rising to CP	0.0432	0.0606	0.0606	0.0606
TE ↓	hold_rising to CP	-0.1158	-0.0654	-0.0680	-0.0680
TE ↑	hold_rising to CP	-0.0965	-0.0579	-0.0634	-0.0634
TE ↓	setup_rising to CP	0.2002	0.1587	0.1591	0.1564
TE ↑	setup_rising to CP	0.4127	0.3346	0.3346	0.3349
TI ↓	hold_rising to CP	-0.3237	-0.1973	-0.2057	-0.2057
TI ↑	hold_rising to CP	-0.1062	-0.0601	-0.0609	-0.0609
TI ↓	setup_rising to CP	0.4175	0.3234	0.3200	0.3200
TI ↑	setup_rising to CP	0.1512	0.1059	0.1046	0.1046

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	1.743e-06	3.918e-09
X8_P16	1.921e-06	3.799e-09
X17_P16	2.369e-06	4.038e-09
X33_P16	2.861e-06	4.276e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

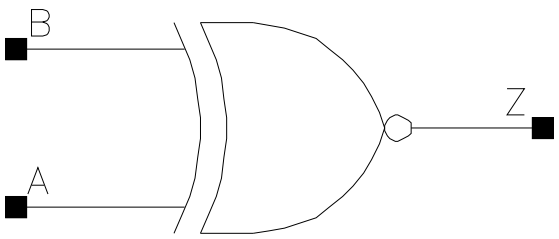
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	3.535e-03	3.634e-03	3.666e-03	3.683e-03
Clock 100Mhz Data 25Mhz	5.436e-03	5.596e-03	6.264e-03	6.841e-03
Clock 100Mhz Data 50Mhz	7.337e-03	7.558e-03	8.861e-03	9.999e-03
Clock = 0 Data 100Mhz	4.067e-03	3.878e-03	3.816e-03	3.784e-03
Clock = 1 Data 100Mhz	1.161e-03	6.011e-04	4.147e-04	3.215e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P16	X8_P16	X17_P16	X25_P16
A	0.0017	0.0007	0.0009	0.0014
B	0.0016	0.0015	0.0019	0.0025
	X33_P16			
A	0.0016			
B	0.0029			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X8_P16**	**X6_P16**	**X8_P16**
A to Z ↓	0.0351	0.0893	5.7383	3.1485
A to Z ↑	0.0393	0.0756	8.9581	5.6654
B to Z ↓	0.0333	0.0610	5.7275	3.1293
B to Z ↑	0.0383	0.0551	8.9745	5.6457
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
A to Z ↓	0.0836	0.0834	1.5586	1.0727
A to Z ↑	0.0684	0.0691	2.7667	1.8374

B to Z ↓	0.0627	0.0611	1.5561	1.0706
B to Z ↑	0.0540	0.0525	2.7603	1.8349
	X33_P16		**X33_P16**	
A to Z ↓	0.0777		0.8064	
A to Z ↑	0.0661		1.3792	
B to Z ↓	0.0581		0.8048	
B to Z ↑	0.0514		1.3776	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P16	7.079e-07	1.179e-09
X8_P16	1.024e-06	1.536e-09
X17_P16	1.534e-06	1.655e-09
X25_P16	2.428e-06	2.370e-09
X33_P16	3.092e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	2.207e-03	3.962e-03	5.502e-03	8.868e-03
B to Z	2.072e-03	2.710e-03	4.073e-03	6.413e-03
	X33_P16			
A to Z	1.075e-02			
B to Z	8.023e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

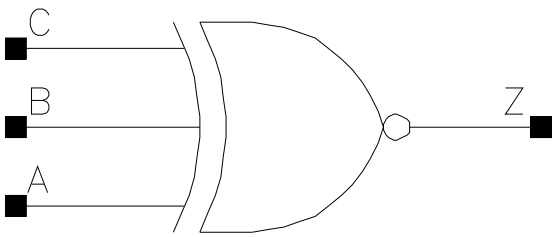
Pin Cycle (vdds)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	-2.707e-06	-1.844e-07	-2.406e-07	-6.604e-07
B to Z	9.077e-06	-2.543e-07	-1.238e-07	-7.739e-07
	X33_P16			
A to Z	-7.392e-07			
B to Z	-4.236e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	2.176	2.6112
X16_P16	1.200	2.720	3.2640
X25_P16	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X16_P16	X25_P16
A	0.0028	0.0024	0.0030	0.0044
B	0.0031	0.0022	0.0029	0.0040
C	0.0020	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0618	0.1096	6.9596	3.3679
A to Z ↑	0.0580	0.0976	13.3310	5.6124
B to Z ↓	0.0627	0.1092	6.9535	3.3649
B to Z ↑	0.0581	0.0971	13.3061	5.6094
C to Z ↓	0.0605	0.1416	6.9379	3.3651
C to Z ↑	0.0555	0.1281	13.2968	5.6150
	X16_P16	**X25_P16**	**X16_P16**	**X25_P16**
A to Z ↓	0.1074	0.1063	1.7330	1.1042
A to Z ↑	0.1035	0.1020	2.9429	1.8466
B to Z ↓	0.1074	0.1078	1.7328	1.1038

B to Z ↑	0.1032	0.1037	2.9442	1.8473
C to Z ↓	0.1465	0.1539	1.7323	1.1031
C to Z ↑	0.1403	0.1484	2.9446	1.8470

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	7.624e-07	2.132e-09
X8_P16	8.669e-07	2.251e-09
X16_P16	1.387e-06	2.727e-09
X25_P16	1.956e-06	3.799e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	2.485e-03	3.172e-03	5.051e-03	7.506e-03
B to Z	2.279e-03	3.097e-03	4.945e-03	7.412e-03
C to Z	2.249e-03	4.775e-03	7.007e-03	1.046e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

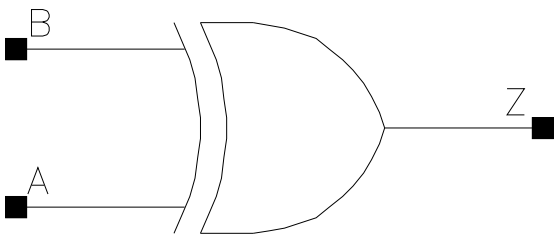
Pin Cycle (vdds)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	-2.981e-05	-9.932e-06	-1.451e-05	-2.251e-05
B to Z	1.395e-05	-8.574e-07	4.489e-06	8.039e-06
C to Z	1.378e-05	7.830e-06	1.164e-05	1.403e-05

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.224	1.4688
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.224	1.4688
X16_P16	1.200	1.360	1.6320
X25_P16	1.200	2.176	2.6112
X31_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X16_P16
A	0.0007	0.0016	0.0010	0.0011
B	0.0012	0.0015	0.0015	0.0017
	X25_P16	X31_P16		
A	0.0014	0.0019		
B	0.0026	0.0033		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0794	0.0388	5.8263	4.3474
A to Z ↑	0.0710	0.0394	11.1420	11.8746
B to Z ↓	0.0555	0.0379	5.8075	4.3646
B to Z ↑	0.0544	0.0376	11.1286	11.8677
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0700	0.0726	3.0539	1.5879

A to Z ↑	0.0599	0.0627	5.5247	2.7789
B to Z ↓	0.0533	0.0550	3.0479	1.5865
B to Z ↑	0.0488	0.0511	5.5189	2.7779
	X25_P16	**X31_P16**	**X25_P16**	**X31_P16**
A to Z ↓	0.0777	0.0723	1.0606	0.8590
A to Z ↑	0.0669	0.0630	1.8343	1.4796
B to Z ↓	0.0581	0.0545	1.0597	0.8586
B to Z ↑	0.0507	0.0482	1.8355	1.4801

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	8.420e-07	1.417e-09
X6_P16	7.495e-07	1.179e-09
X8_P16	1.244e-06	1.417e-09
X16_P16	1.674e-06	1.536e-09
X25_P16	2.381e-06	2.251e-09
X31_P16	2.987e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	3.041e-03	2.204e-03	3.622e-03	5.145e-03
B to Z	2.307e-03	2.016e-03	2.943e-03	4.230e-03
	X25_P16	X31_P16		
A to Z	7.951e-03	9.813e-03		
B to Z	5.479e-03	6.723e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

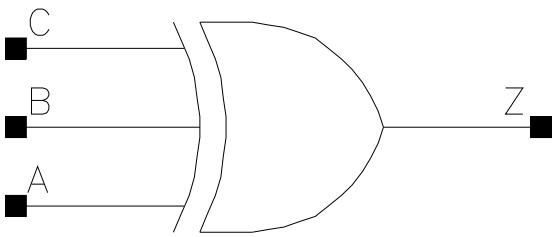
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	-2.140e-07	-9.400e-06	-2.915e-07	-3.425e-07
B to Z	-1.981e-07	6.270e-06	-1.537e-07	-1.932e-07
	X25_P16	X31_P16		
A to Z	-5.147e-07	-6.711e-07		
B to Z	-5.542e-07	-5.707e-07		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X24_P16	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X24_P16
A	0.0024	0.0024	0.0030	0.0053
B	0.0024	0.0022	0.0027	0.0044
C	0.0007	0.0016	0.0023	0.0036

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0623	0.1094	7.2615	3.3649
A to Z ↑	0.0583	0.0973	14.5446	5.6077
B to Z ↓	0.0624	0.1090	7.2583	3.3635
B to Z ↑	0.0587	0.0969	14.5252	5.6064
C to Z ↓	0.1050	0.1056	7.2465	3.3620
C to Z ↑	0.1011	0.0927	14.5065	5.6074
	X17_P16	**X24_P16**	**X17_P16**	**X24_P16**
A to Z ↓	0.0971	0.1139	1.6012	1.1623
A to Z ↑	0.0941	0.0826	2.7255	1.8478
B to Z ↓	0.0966	0.1140	1.5996	1.1602

B to Z ↑	0.0935	0.0822	2.7276	1.8477
C to Z ↓	0.0944	0.1096	1.5997	1.1588
C to Z ↑	0.0911	0.0797	2.7290	1.8472

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P16	8.806e-07	2.132e-09
X8_P16	7.134e-07	2.013e-09
X17_P16	1.198e-06	2.132e-09
X24_P16	2.163e-06	3.680e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	2.224e-03	3.195e-03	4.858e-03	8.364e-03
B to Z	2.166e-03	3.076e-03	4.664e-03	8.055e-03
C to Z	4.488e-03	2.976e-03	4.637e-03	7.833e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	-1.487e-05	-1.259e-05	-1.956e-05	-4.389e-05
B to Z	1.620e-06	2.712e-06	9.128e-06	-2.491e-06
C to Z	1.377e-05	5.129e-06	1.178e-05	2.903e-05

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