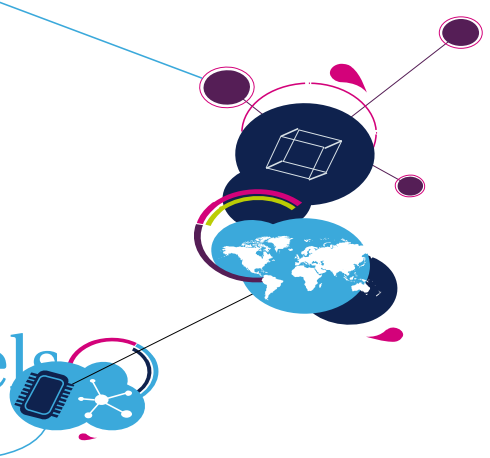
cmos028fdsoi Technology

PDC vs MC Noise report for EG models

DK1.2_RF_mmW



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General information on PDC vs MC Noise report for EG models

- Maximum supply voltage is 1.8 V.
- Validity domain is defined as follows:
  - ✔ Drawn gate length varies from 150nm to 10um.
  - ✔ Drawn transistor width varies from 0.16um to 10um.
  - ✔ Device temperature varies from -40 °C to 125 °C.

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Output parameters definitions

- Model(s): egnfet_acc, egpfet_acc

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egnfet_acc
Electrical characteristics per geometry

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egnfet_acc @ w=1.5e-6, l=0.15e-6, pre_layout_local=1, nf=2, sa=1.2e-07, sb=1.2e-07, devtype=PCELLwoWPE, as=9e-14, ad=9e-14, ps=1.74e-06, pd=1.74e-06, vbs=0, vdd=1.8, temp=25

	TT_Noisedev=4	TT_Noisedev=0	TT_Noisedev=2	PRO_MC_PARAM_TT_1_MC_AVG-3S	PRO_MC_PARAM_TT_1_MC_AVG	PRO_MC_PARAM_TT_1_MC_AVG+3S
logSi2@1Hz [log10(A²/Hz)]	-16.72	-15.66	-14.59	-16.73	-15.66	-14.59
logSi2ovId2@1Hz [log10(1/Hz)]	-8.12	-7.06	-5.99	-8.12	-7.06	-5.99
logSv2@1Hz [log10(V²/Hz)]	-10.01	-8.94	-7.87	-10.01	-8.94	-7.87

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egpfet_acc
Electrical characteristics per geometry

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egpfet_acc @ w=1.5e-6, l=0.15e-6, pre_layout_local=1, nf=2, sa=1.2e-07, sb=1.2e-07, devtype=PCELLwoWPE, as=9e-14, ad=9e-14, ps=1.74e-06, pd=1.74e-06, vbs=0, vdd=1.8, temp=25

	TT_Noisedev=4	TT_Noisedev=0	TT_Noisedev=2	PRO_MC_PARAM_TT_1_MC_AVG-3S	PRO_MC_PARAM_TT_1_MC_AVG	PRO_MC_PARAM_TT_1_MC_AVG+3S
logSi2@1Hz [log10(A²/Hz)]	-17.88	-16.98	-16.07	-17.88	-16.98	-16.07
logSi2ovId2@1Hz [log10(1/Hz)]	-8.48	-7.58	-6.68	-8.48	-7.58	-6.67
logSv2@1Hz [log10(V²/Hz)]	-10.1	-9.2	-8.3	-10.1	-9.2	-8.3

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egnfet_acc
Electrical characteristics scaling

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Scaling versus Length @ W/L=10&&W/nf<5um

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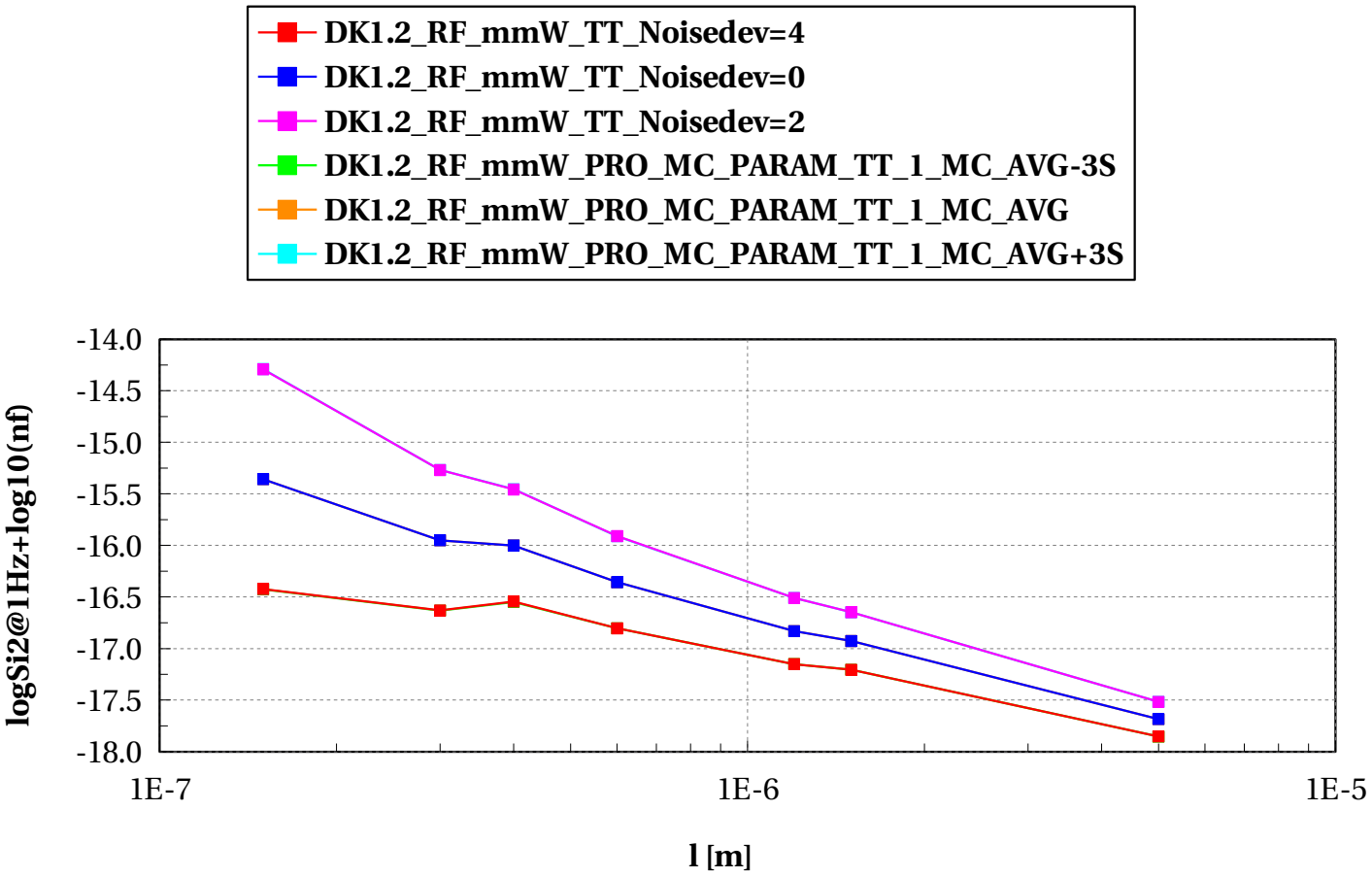
egnfet_acc, logSi2@1Hz+log10(nf) vs l [m]

W/L==10 and w/nf<5 and devType=="PCELLwoWPE"



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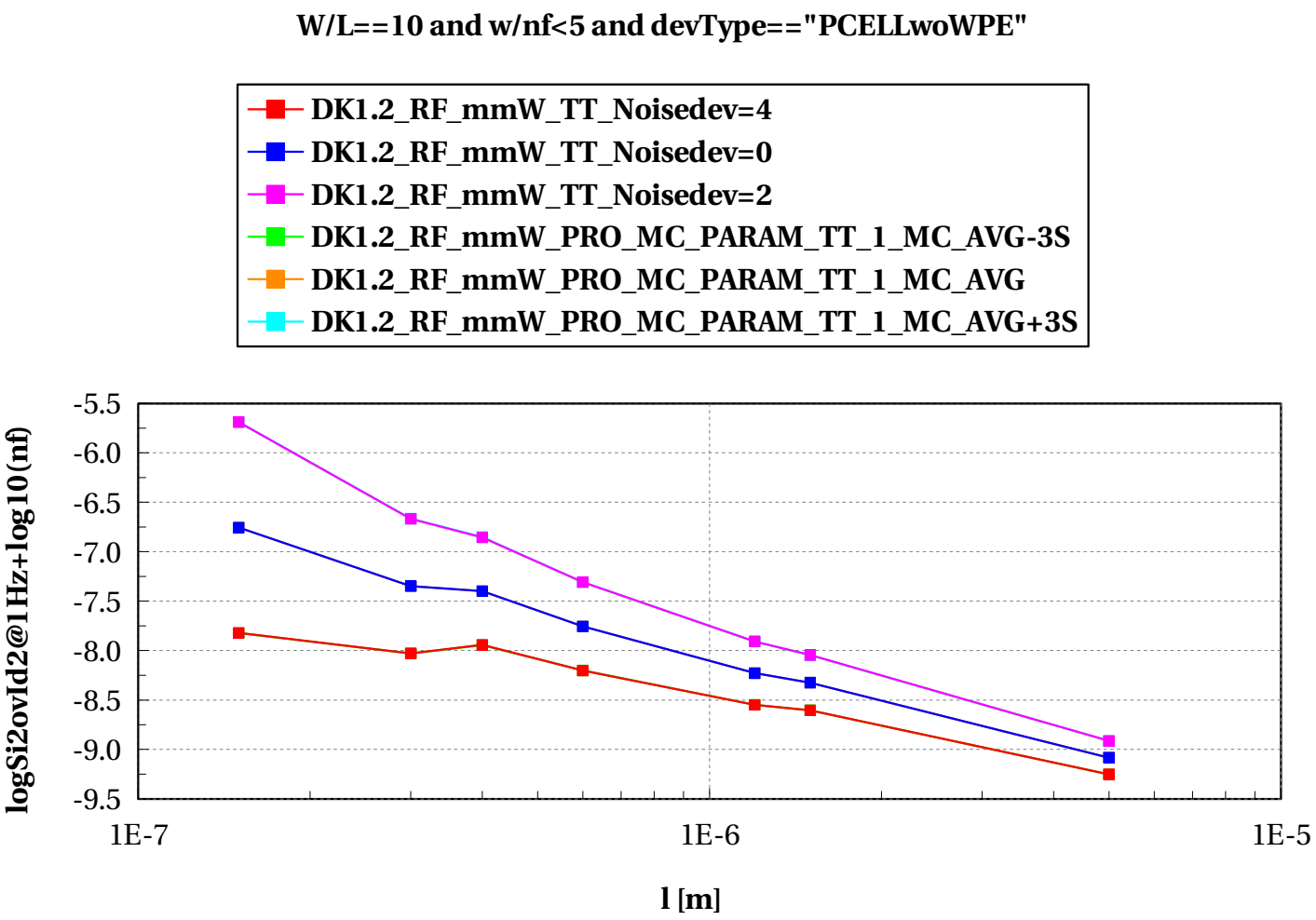
egnfet_acc, logSi2ovId2@1Hz+log10(nf) vs l [m]



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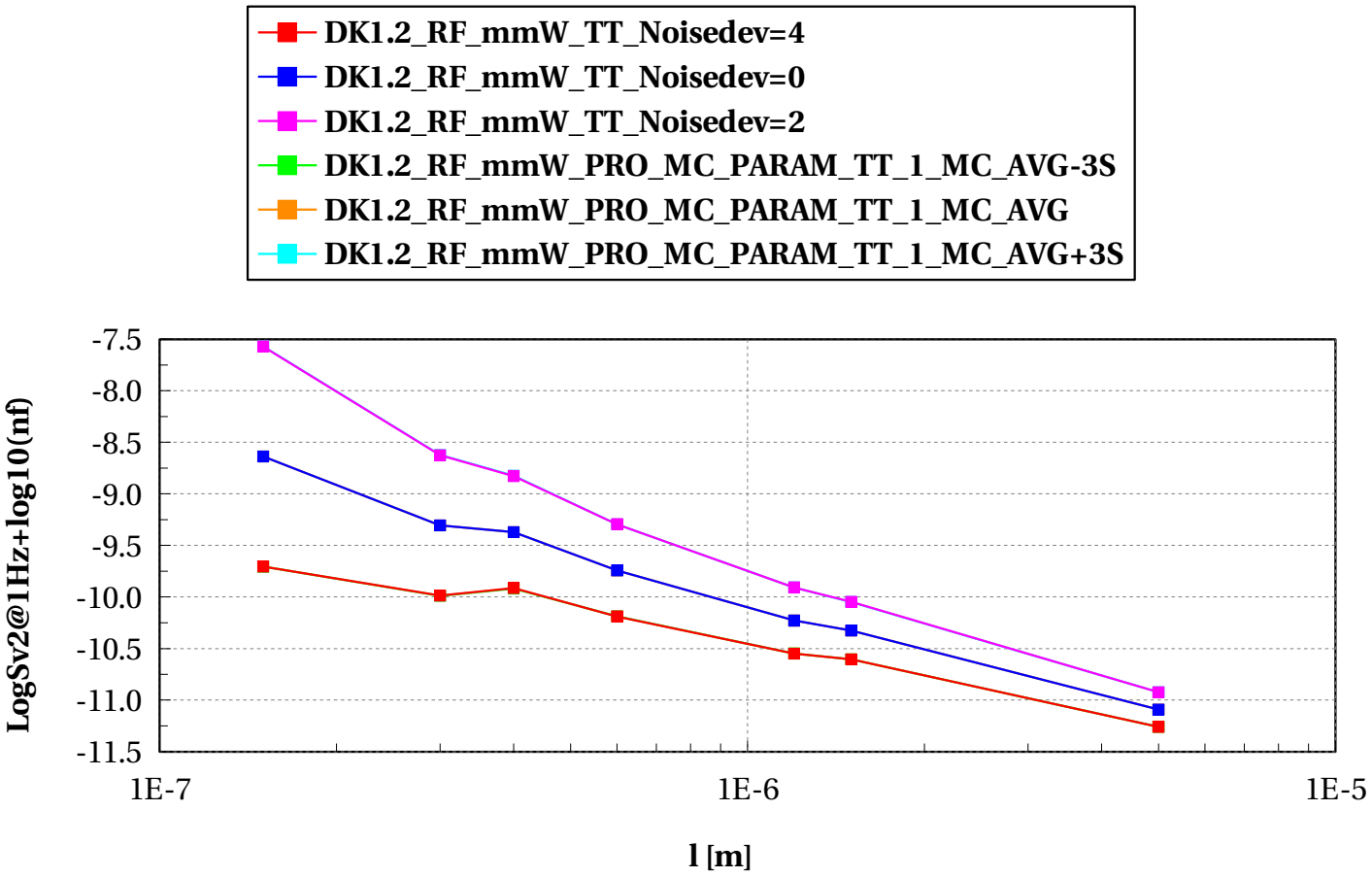
egnfet_acc, LogSv2@1Hz+log10(nf) vs l [m]

W/L==10 and w/nf<5 and devType=="PCELLwoWPE"



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egpfet_acc
Electrical characteristics scaling

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Scaling versus Length @ W/L=10&&W/nf<5um

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egpfet_acc, logSi2@1Hz+log10(nf) vs l [m]

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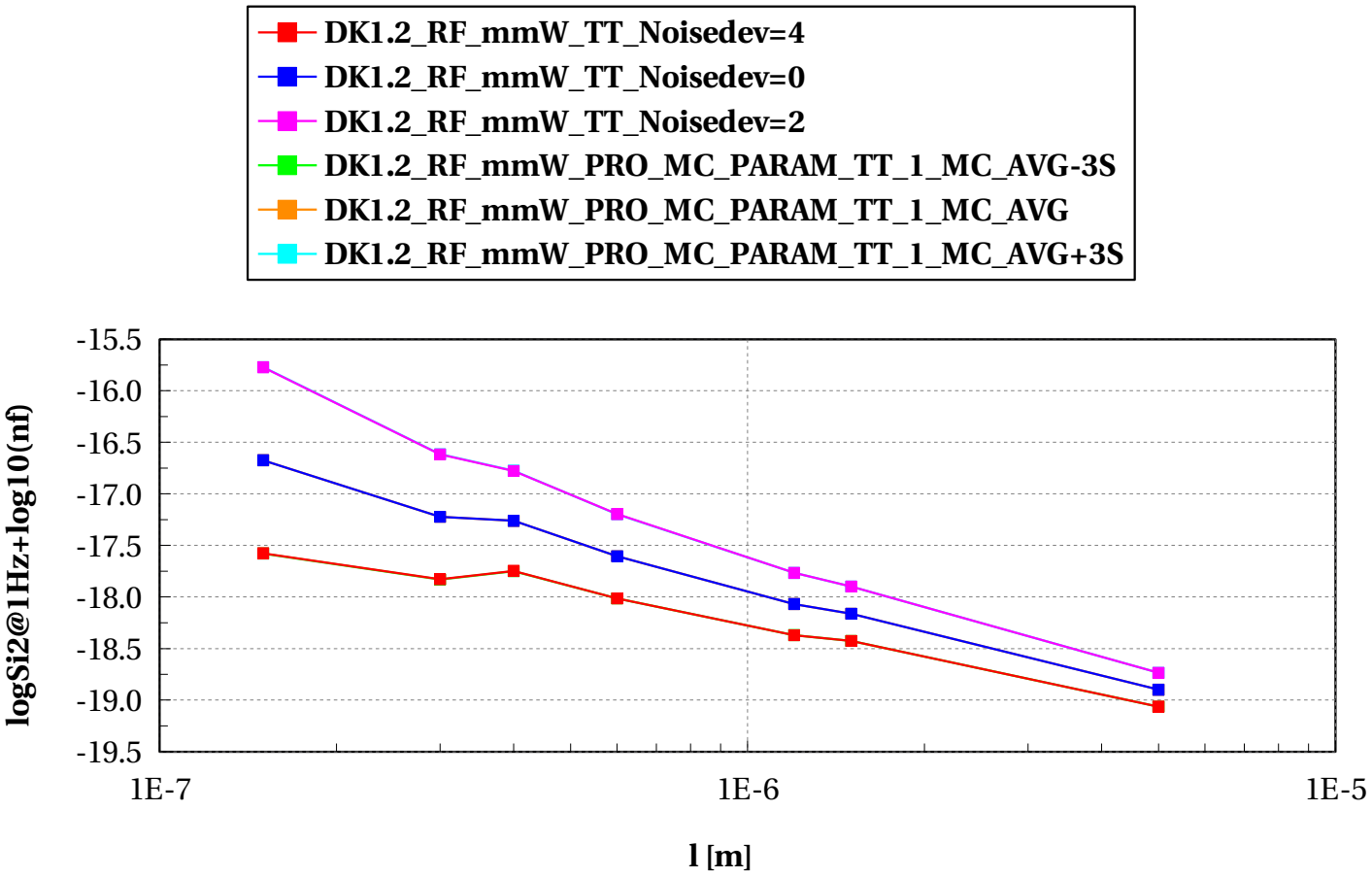

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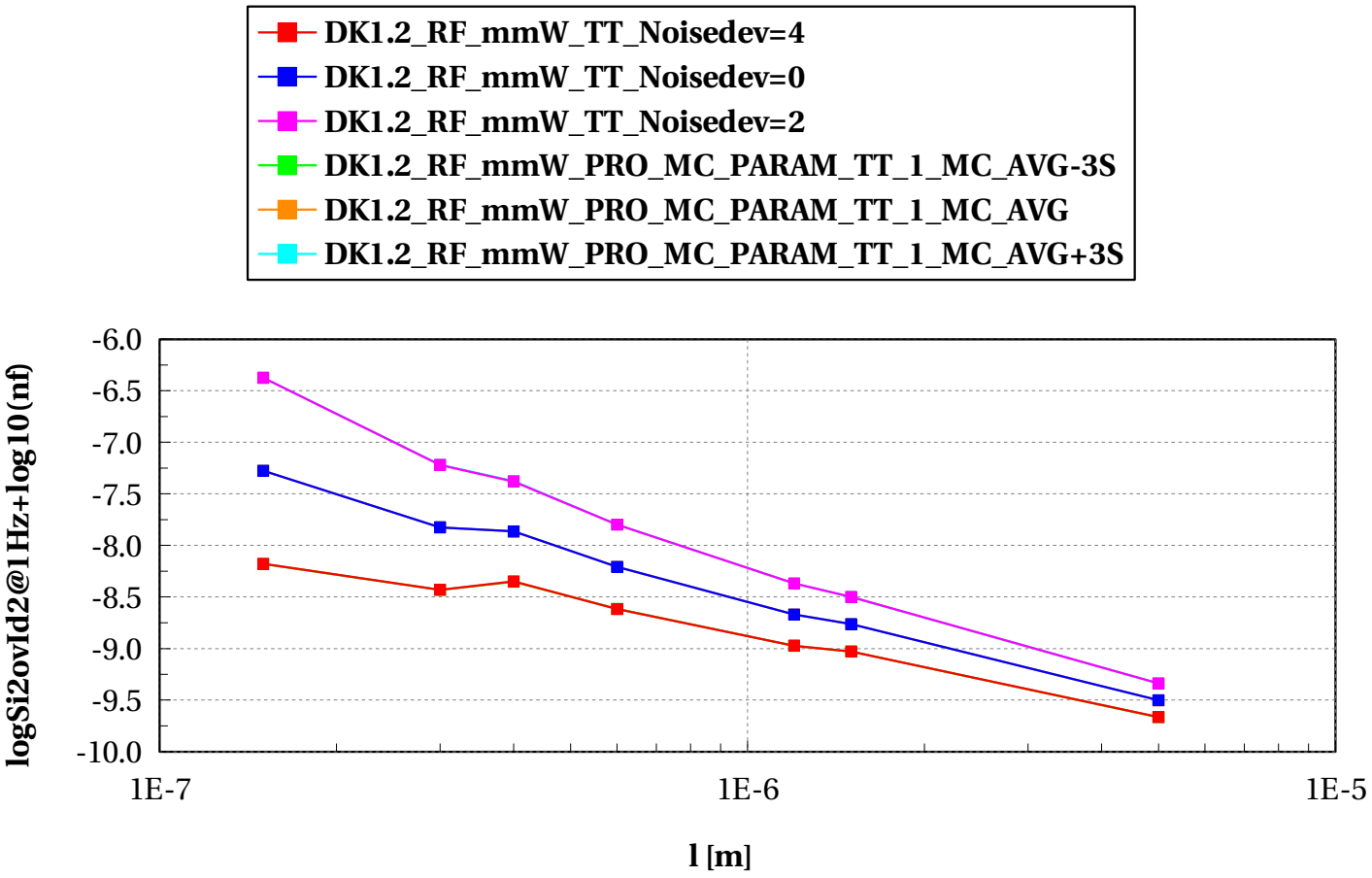
egpfet_acc, logSi2ovId2@1Hz+log10(nf) vs l [m]

W/L==10 and w/nf<5 and devType=="PCELLwoWPE"



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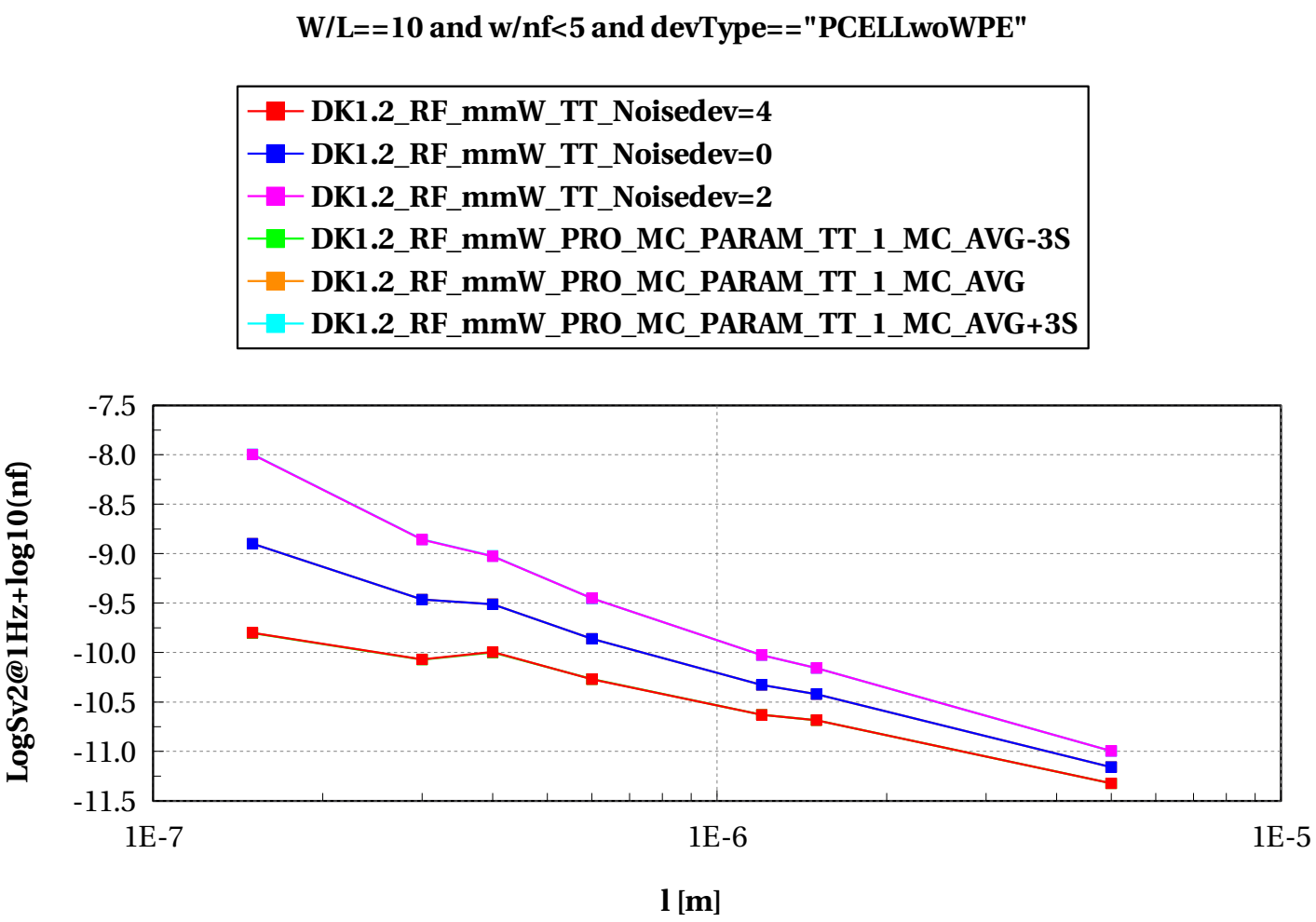
egpfet_acc, LogSv2@1Hz+log10(nf) vs l [m]



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Annex

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Conditions of simulations

The simulations were done with SBenchLSF Alpha using Eldo simulator 2018.3.

- Model egnfet_acc (DK1.2_RF_mmW)
  - ✔ Input Parameters
    - ✘ ams_release = 2018.3
    - ✘ mc_runs = 500
    - ✘ iana = 5e-6 A
    - ✘ temp = 25 °C
    - ✘ mc_sens = 0
    - ✘ f_ext = 100k Hz
    - ✘ sbenchlsf_release = Alpha
    - ✘ vbs = 0 V
    - ✘ model_version = 1.2.c
    - ✘ vds_ana = Vdd/4 V
    - ✘ mc_nsigma = 3
    - ✘ vdd = 1.8 V
  - ✔ Sweep Parameters
  - ✔ Extra parameters

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- ✘ eg_dev = 0

- ● Model egpfet_acc (DK1.2_RF_mmW)
  - ✔ Input Parameters
    - ✘ ams_release = 2018.3
    - ✘ mc_runs = 500
    - ✘ iana = 2e-6 A
    - ✘ temp = 25 °C
    - ✘ mc_sens = 0
    - ✘ f_ext = 100k Hz
    - ✘ sbenchlsf_release = Alpha
    - ✘ vbs = 0 V
    - ✘ model_version = 1.2.c
    - ✘ vds_ana = Vdd/4 V
    - ✘ mc_nsigma = 3
    - ✘ vdd = 1.8 V
  - ✔ Sweep Parameters
  - ✔ Extra parameters
    - ✘ eg_dev = 0

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