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C28SOI_SC_12_COREPBP4_LR Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 4 nm

Overview

- C28SOI_SC_12_COREPBP4_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

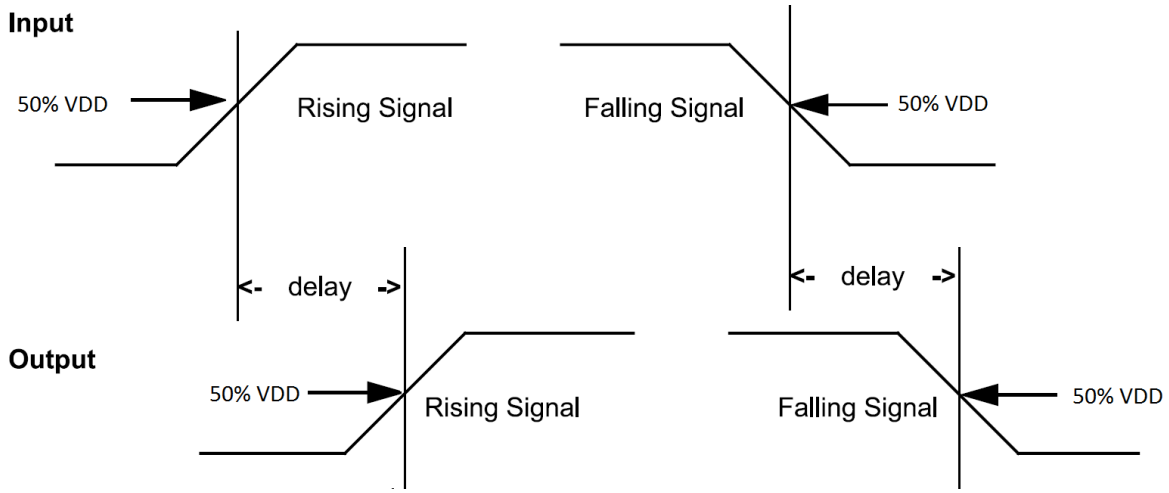


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

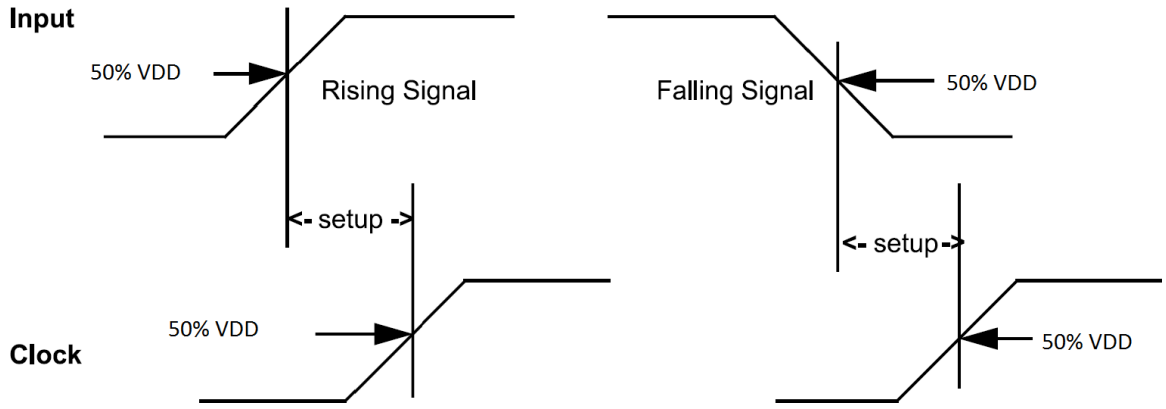


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

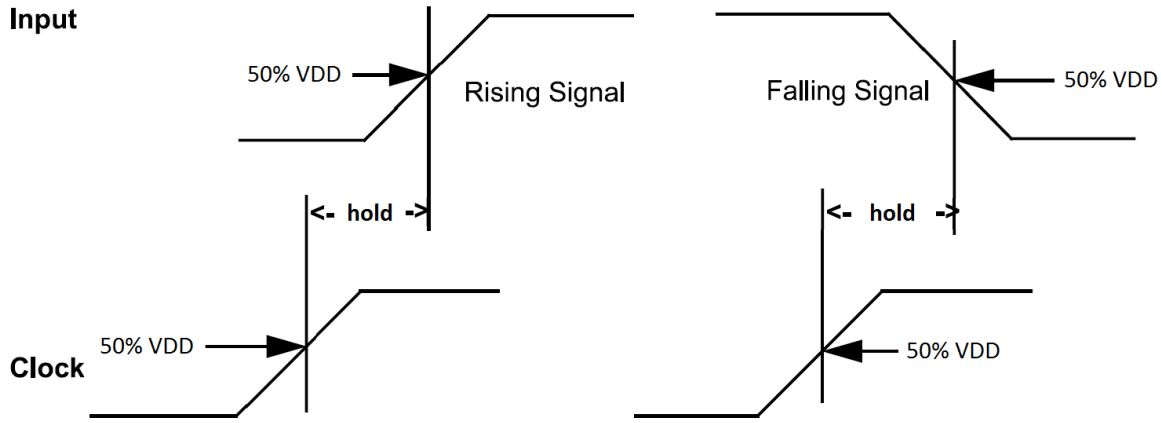


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

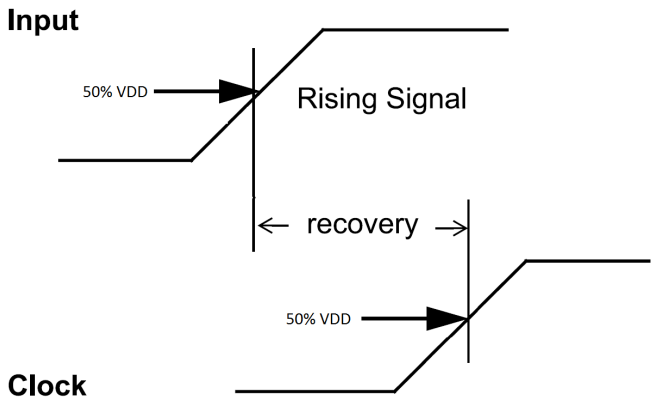


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

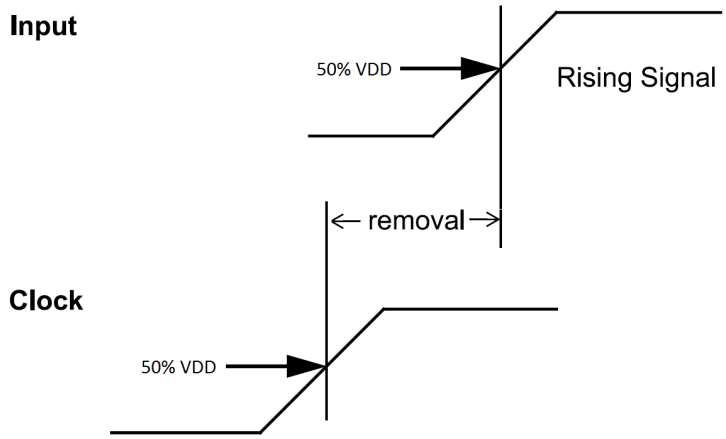


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

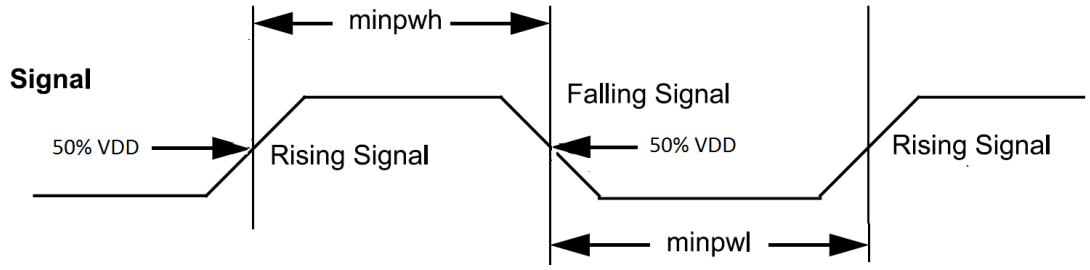


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

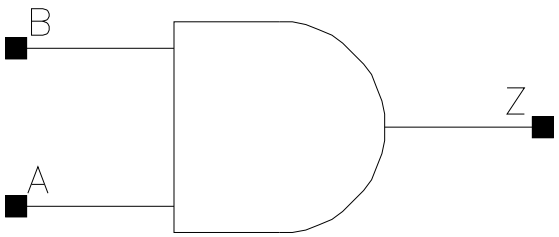
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X25_P4	1.200	1.088	1.3056
X33_P4	1.200	1.360	1.6320
X42_P4	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0007	0.0010	0.0015	0.0018
B	0.0006	0.0009	0.0014	0.0018
	X42_P4			
A	0.0018			
B	0.0018			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0412	0.0339	2.4623	1.2526
A to Z ↑	0.0336	0.0305	4.3305	2.1014
B to Z ↓	0.0394	0.0322	2.4645	1.2521
B to Z ↑	0.0346	0.0313	4.3294	2.1003
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0347	0.0336	0.8309	0.6164

A to Z ↑	0.0301	0.0306	1.3864	1.0458
B to Z ↓	0.0332	0.0312	0.8295	0.6156
B to Z ↑	0.0310	0.0305	1.3872	1.0453
	X42_P4		**X42_P4**	
A to Z ↓	0.0360		0.5017	
A to Z ↑	0.0330		0.8377	
B to Z ↓	0.0336		0.5006	
B to Z ↑	0.0330		0.8379	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	2.164e-06	8.218e-10
X16_P4	4.133e-06	9.409e-10
X25_P4	5.980e-06	1.298e-09
X33_P4	8.163e-06	1.536e-09
X42_P4	9.245e-06	1.655e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	1.186e-05	2.344e-05	3.626e-05	8.713e-05
B (output stable)	1.903e-05	3.773e-05	6.012e-05	2.852e-04
A to Z	1.796e-03	2.930e-03	4.495e-03	5.898e-03
B to Z	1.700e-03	2.757e-03	4.231e-03	5.324e-03
	X42_P4			
A (output stable)	8.762e-05			
B (output stable)	2.860e-04			
A to Z	7.042e-03			
B to Z	6.454e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

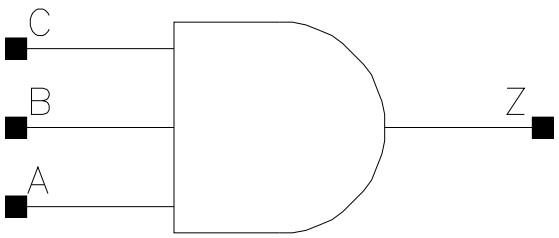
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	5.031e-08	3.097e-08	4.800e-09	-4.220e-09
B (output stable)	4.550e-08	2.793e-08	-1.530e-08	-3.830e-08
A to Z	-1.577e-07	-3.866e-07	-2.047e-07	-9.265e-07
B to Z	-5.260e-08	-2.375e-07	-2.759e-07	-7.490e-07
	X42_P4			
A (output stable)	-2.170e-09			
B (output stable)	-3.950e-08			
A to Z	-1.114e-06			
B to Z	-3.527e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X25_P4	1.200	1.360	1.6320
X33_P4	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0006	0.0010	0.0016	0.0019
B	0.0006	0.0009	0.0014	0.0018
C	0.0006	0.0009	0.0013	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0445	0.0369	2.4998	1.2215
A to Z ↑	0.0443	0.0398	4.3734	2.0819
B to Z ↓	0.0431	0.0355	2.4996	1.2209
B to Z ↑	0.0444	0.0401	4.3706	2.0844
C to Z ↓	0.0416	0.0339	2.4910	1.2198
C to Z ↑	0.0450	0.0398	4.3713	2.0844
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0369	0.0350	0.8392	0.6279

A to Z ↑	0.0391	0.0373	1.4200	1.0631
B to Z ↓	0.0356	0.0336	0.8389	0.6273
B to Z ↑	0.0395	0.0377	1.4201	1.0637
C to Z ↓	0.0339	0.0321	0.8377	0.6265
C to Z ↑	0.0394	0.0376	1.4203	1.0627

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	1.733e-06	9.409e-10
X17_P4	3.435e-06	1.060e-09
X25_P4	4.939e-06	1.536e-09
X33_P4	6.561e-06	1.655e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	1.287e-05	2.623e-05	3.509e-05	4.826e-05
B (output stable)	2.336e-05	4.988e-05	6.922e-05	9.683e-05
C (output stable)	4.934e-05	9.962e-05	1.443e-04	2.030e-04
A to Z	1.981e-03	3.399e-03	4.896e-03	6.258e-03
B to Z	1.882e-03	3.224e-03	4.634e-03	5.900e-03
C to Z	1.807e-03	3.046e-03	4.373e-03	5.540e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

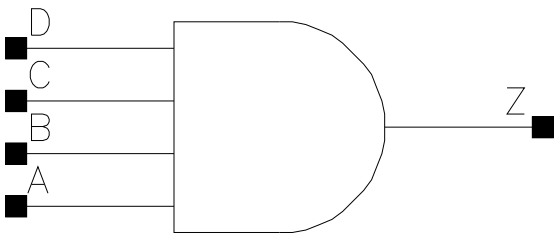
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	5.915e-08	3.200e-08	4.800e-09	-6.767e-09
B (output stable)	5.883e-08	2.655e-08	-4.233e-09	-3.190e-08
C (output stable)	4.610e-08	2.304e-08	-3.533e-09	-3.079e-08
A to Z	-6.965e-08	-2.656e-07	-3.971e-07	-4.122e-07
B to Z	1.395e-08	-1.572e-07	-5.415e-07	-5.081e-07
C to Z	-1.770e-07	-3.497e-07	-5.438e-07	-4.011e-07

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X6_P4	1.200	1.088	1.3056
X20_P4	1.200	2.312	2.7744
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P4	X6_P4	X20_P4	X27_P4
A	0.0005	0.0007	0.0016	0.0018
B	0.0005	0.0007	0.0016	0.0018
C	0.0004	0.0007	0.0016	0.0018
D	0.0005	0.0007	0.0016	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X6_P4	X4_P4	X6_P4
A to Z ↓	0.0483	0.0399	4.7124	3.0371
A to Z ↑	0.0493	0.0365	17.1931	9.1013
B to Z ↓	0.0471	0.0378	4.7138	3.0343
B to Z ↑	0.0504	0.0370	17.1953	9.0969
C to Z ↓	0.0502	0.0428	4.6844	3.0512
C to Z ↑	0.0482	0.0353	17.2007	9.1222

D to Z ↓	0.0490	0.0402	4.6849	3.0480
D to Z ↑	0.0504	0.0359	17.2159	9.1173
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0378	0.0356	0.8835	0.6250
A to Z ↑	0.0363	0.0405	3.0198	2.2868
B to Z ↓	0.0350	0.0332	0.8818	0.6239
B to Z ↑	0.0361	0.0406	3.0201	2.2881
C to Z ↓	0.0371	0.0347	0.8905	0.6277
C to Z ↑	0.0317	0.0346	3.0219	2.2882
D to Z ↓	0.0339	0.0323	0.8893	0.6265
D to Z ↑	0.0313	0.0346	3.0229	2.2862

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	1.420e-06	1.298e-09
X6_P4	3.060e-06	1.298e-09
X20_P4	8.347e-06	2.370e-09
X27_P4	9.532e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	3.263e-04	4.969e-04	1.444e-03	1.786e-03
B (output stable)	3.036e-04	4.494e-04	1.331e-03	1.658e-03
C (output stable)	3.199e-04	5.181e-04	1.294e-03	1.618e-03
D (output stable)	3.025e-04	4.674e-04	1.157e-03	1.478e-03
A to Z	1.344e-03	2.051e-03	6.066e-03	7.914e-03
B to Z	1.283e-03	1.929e-03	5.547e-03	7.365e-03
C to Z	1.318e-03	2.075e-03	5.125e-03	6.435e-03
D to Z	1.260e-03	1.944e-03	4.563e-03	5.876e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

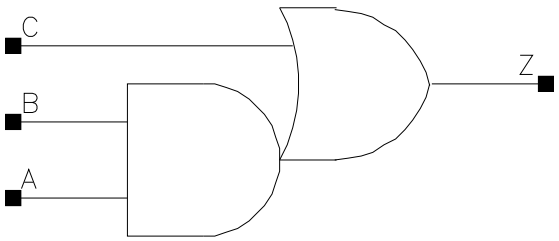
Pin Cycle (vdds)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	-5.277e-08	-8.109e-08	-1.127e-06	-2.129e-06
B (output stable)	-2.807e-08	-1.726e-08	-8.098e-07	-2.528e-06
C (output stable)	4.605e-06	7.650e-06	2.859e-05	5.238e-05
D (output stable)	4.592e-06	7.654e-06	2.804e-05	5.149e-05
A to Z	2.171e-07	3.226e-07	2.120e-07	8.310e-07
B to Z	2.260e-07	4.384e-07	8.650e-07	1.099e-06
C to Z	-1.189e-07	-2.896e-07	-1.198e-06	-1.682e-06
D to Z	-1.398e-07	-2.506e-07	-9.149e-07	-1.147e-06

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0019
B	0.0006	0.0009	0.0017
C	0.0007	0.0010	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0540	0.0472	2.5506	1.2482
A to Z ↑	0.0347	0.0301	4.2219	2.0639
B to Z ↓	0.0505	0.0442	2.5417	1.2439
B to Z ↑	0.0361	0.0316	4.2195	2.0673
C to Z ↓	0.0548	0.0483	2.5339	1.2414
C to Z ↑	0.0303	0.0278	4.1972	2.0568
	X33_P4		**X33_P4**	
A to Z ↓	0.0474		0.6331	
A to Z ↑	0.0308		1.0414	

B to Z ↓	0.0441		0.6319	
B to Z ↑	0.0314		1.0404	
C to Z ↓	0.0481		0.6301	
C to Z ↑	0.0273		1.0361	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	2.940e-06	9.409e-10
X17_P4	5.543e-06	1.060e-09
X33_P4	1.104e-05	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	1.538e-05	2.462e-05	6.784e-05
B (output stable)	1.851e-05	2.951e-05	1.080e-04
C (output stable)	5.187e-05	8.978e-05	2.059e-04
A to Z	1.825e-03	3.063e-03	6.086e-03
B to Z	1.732e-03	2.889e-03	5.632e-03
C to Z	2.040e-03	3.444e-03	6.793e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

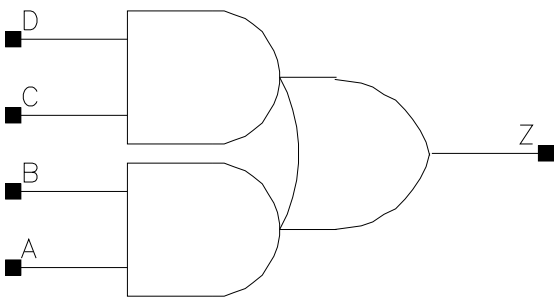
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	1.331e-05	2.205e-05	4.250e-05
B (output stable)	1.421e-05	2.218e-05	4.271e-05
C (output stable)	-2.540e-06	-2.801e-06	-5.955e-06
A to Z	-5.670e-08	-1.250e-07	-5.838e-07
B to Z	-5.170e-08	-2.727e-07	-5.080e-07
C to Z	-1.420e-07	7.590e-07	5.353e-07

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0017
B	0.0006	0.0009	0.0016
C	0.0005	0.0008	0.0018
D	0.0006	0.0009	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0635	0.0544	2.4503	1.2331
A to Z ↑	0.0433	0.0379	4.1607	2.0677
B to Z ↓	0.0597	0.0509	2.4398	1.2293
B to Z ↑	0.0439	0.0388	4.1606	2.0689

C to Z ↓	0.0556	0.0481	2.4411	1.2296
C to Z ↑	0.0376	0.0329	4.1495	2.0626
D to Z ↓	0.0535	0.0460	2.4344	1.2275
D to Z ↑	0.0395	0.0343	4.1529	2.0629
	X33_P4		**X33_P4**	
A to Z ↓	0.0518		0.6325	
A to Z ↑	0.0350		1.0460	
B to Z ↓	0.0493		0.6318	
B to Z ↑	0.0364		1.0462	
C to Z ↓	0.0456		0.6317	
C to Z ↑	0.0308		1.0411	
D to Z ↓	0.0431		0.6305	
D to Z ↑	0.0318		1.0422	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	3.094e-06	1.179e-09
X17_P4	5.856e-06	1.298e-09
X33_P4	1.081e-05	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	3.046e-05	4.448e-05	6.709e-05
B (output stable)	1.132e-04	1.430e-04	8.320e-05
C (output stable)	1.984e-05	3.287e-05	7.027e-05
D (output stable)	2.388e-05	4.179e-05	9.337e-05
A to Z	2.453e-03	4.001e-03	7.435e-03
B to Z	2.269e-03	3.717e-03	7.047e-03
C to Z	2.045e-03	3.346e-03	6.109e-03
D to Z	1.964e-03	3.185e-03	5.752e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

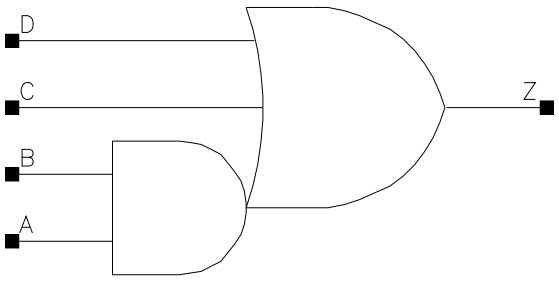
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	-1.841e-07	-2.094e-07	-8.686e-07
B (output stable)	-1.078e-06	-2.407e-07	-9.004e-07
C (output stable)	6.944e-06	1.144e-05	3.050e-05
D (output stable)	6.807e-06	1.123e-05	3.092e-05
A to Z	1.996e-07	6.303e-07	2.112e-06
B to Z	3.224e-07	8.833e-07	2.200e-06
C to Z	-1.829e-07	-2.704e-07	-4.824e-07
D to Z	-1.675e-07	-1.521e-07	-5.222e-07

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	0.952	1.1424
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0016
B	0.0006	0.0008	0.0017
C	0.0006	0.0009	0.0017
D	0.0006	0.0009	0.0016

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0727	0.0618	2.6952	1.3222
A to Z ↑	0.0374	0.0326	4.2091	2.1310
B to Z ↓	0.0700	0.0577	2.6887	1.3184
B to Z ↑	0.0390	0.0334	4.2065	2.1317
C to Z ↓	0.0798	0.0683	2.6812	1.3167
C to Z ↑	0.0327	0.0296	4.1817	2.1216

D to Z ↓	0.0777	0.0673	2.6803	1.3175
D to Z ↑	0.0323	0.0294	4.1782	2.1208
	X33_P4		**X33_P4**	
A to Z ↓	0.0620		0.6623	
A to Z ↑	0.0322		1.0422	
B to Z ↓	0.0561		0.6586	
B to Z ↑	0.0325		1.0423	
C to Z ↓	0.0691		0.6585	
C to Z ↑	0.0287		1.0371	
D to Z ↓	0.0666		0.6584	
D to Z ↑	0.0279		1.0354	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	2.958e-06	1.060e-09
X17_P4	5.683e-06	1.179e-09
X33_P4	1.153e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	9.647e-06	1.857e-05	6.046e-05
B (output stable)	1.184e-05	2.152e-05	9.521e-05
C (output stable)	3.895e-05	5.595e-05	1.676e-04
D (output stable)	1.450e-05	2.701e-05	7.162e-05
A to Z	2.017e-03	3.296e-03	6.526e-03
B to Z	1.940e-03	3.107e-03	5.953e-03
C to Z	2.350e-03	3.898e-03	7.840e-03
D to Z	2.210e-03	3.665e-03	7.184e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

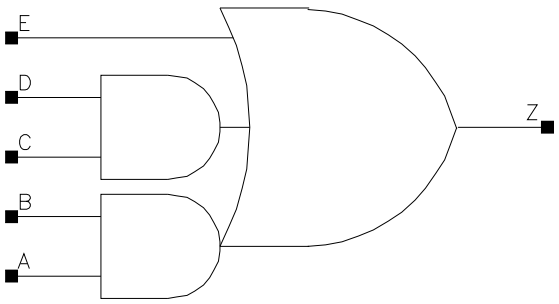
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	1.478e-05	3.058e-05	5.611e-05
B (output stable)	1.848e-05	3.493e-05	6.515e-05
C (output stable)	-4.652e-06	-4.330e-06	-1.416e-05
D (output stable)	7.460e-06	1.514e-05	5.051e-05
A to Z	-2.575e-07	-3.443e-07	-1.186e-06
B to Z	-1.494e-07	-3.317e-07	-6.301e-07
C to Z	-2.901e-07	3.553e-07	-5.790e-07
D to Z	-2.169e-07	3.477e-07	1.630e-07

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.088	1.3056
X17_P4	1.200	1.224	1.4688
X33_P4	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0008	0.0017
B	0.0006	0.0008	0.0016
C	0.0007	0.0011	0.0017
D	0.0006	0.0008	0.0016
E	0.0006	0.0009	0.0016

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0921	0.0770	2.5662	1.2784
A to Z ↑	0.0453	0.0383	4.1364	2.0803

B to Z ↓	0.0894	0.0737	2.5555	1.2756
B to Z ↑	0.0476	0.0399	4.1371	2.0798
C to Z ↓	0.0752	0.0639	2.5514	1.2746
C to Z ↑	0.0395	0.0331	4.0958	2.0654
D to Z ↓	0.0704	0.0588	2.5418	1.2686
D to Z ↑	0.0409	0.0343	4.0990	2.0631
E to Z ↓	0.0805	0.0675	2.5353	1.2677
E to Z ↑	0.0341	0.0294	4.0665	2.0530
	X33_P4		**X33_P4**	
A to Z ↓	0.0757		0.6614	
A to Z ↑	0.0392		1.0488	
B to Z ↓	0.0715		0.6594	
B to Z ↑	0.0405		1.0503	
C to Z ↓	0.0619		0.6589	
C to Z ↑	0.0331		1.0419	
D to Z ↓	0.0571		0.6561	
D to Z ↑	0.0340		1.0402	
E to Z ↓	0.0659		0.6554	
E to Z ↑	0.0293		1.0342	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	3.473e-06	1.298e-09
X17_P4	6.525e-06	1.417e-09
X33_P4	1.189e-05	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	1.797e-05	3.008e-05	6.804e-05
B (output stable)	2.356e-05	3.284e-05	8.874e-05
C (output stable)	2.192e-05	3.066e-05	7.712e-05
D (output stable)	2.651e-05	3.609e-05	1.027e-04
E (output stable)	4.960e-05	5.983e-05	1.441e-04
A to Z	2.807e-03	4.443e-03	8.717e-03
B to Z	2.736e-03	4.260e-03	8.231e-03
C to Z	2.176e-03	3.475e-03	6.729e-03
D to Z	2.079e-03	3.277e-03	6.266e-03
E to Z	2.421e-03	3.835e-03	7.414e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	-1.601e-06	-1.468e-06	-3.390e-06
B (output stable)	-1.661e-06	-1.615e-06	-3.787e-06
C (output stable)	1.420e-05	2.627e-05	5.759e-05
D (output stable)	1.719e-05	2.778e-05	5.999e-05
E (output stable)	1.375e-05	2.529e-05	5.179e-05
A to Z	-2.358e-07	1.059e-06	2.287e-06
B to Z	-2.921e-07	1.195e-06	2.318e-06
C to Z	-1.457e-07	-2.755e-07	-8.309e-07
D to Z	-1.026e-07	-2.349e-07	-7.222e-07

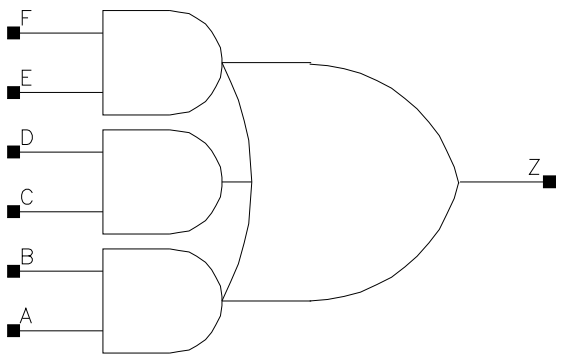
E to Z	-3.500e-07	3.271e-07	2.589e-07

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.360	1.6320
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
A	0.0006	0.0006	0.0008	0.0017

B	0.0006	0.0007	0.0011	0.0016
C	0.0005	0.0006	0.0008	0.0017
D	0.0006	0.0006	0.0008	0.0016
E	0.0006	0.0007	0.0008	0.0017
F	0.0006	0.0007	0.0009	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0930	0.0866	4.9444	2.5482
A to Z ↑	0.0482	0.0455	8.3777	4.2089
B to Z ↓	0.0864	0.0809	4.9105	2.5319
B to Z ↑	0.0484	0.0461	8.3711	4.2066
C to Z ↓	0.0840	0.0788	4.9245	2.5395
C to Z ↑	0.0444	0.0418	8.3225	4.1809
D to Z ↓	0.0808	0.0757	4.9071	2.5300
D to Z ↑	0.0463	0.0438	8.3218	4.1805
E to Z ↓	0.0674	0.0649	4.8995	2.5281
E to Z ↑	0.0383	0.0363	8.2758	4.1572
F to Z ↓	0.0633	0.0610	4.8822	2.5186
F to Z ↑	0.0396	0.0377	8.2736	4.1611
	X17_P4	X33_P4	X17_P4	X33_P4
A to Z ↓	0.0824	0.0782	1.2853	0.6597
A to Z ↑	0.0417	0.0416	2.0862	1.0537
B to Z ↓	0.0781	0.0742	1.2766	0.6576
B to Z ↑	0.0433	0.0430	2.0867	1.0535
C to Z ↓	0.0757	0.0723	1.2812	0.6588
C to Z ↑	0.0385	0.0391	2.0764	1.0474
D to Z ↓	0.0721	0.0687	1.2762	0.6569
D to Z ↑	0.0402	0.0404	2.0763	1.0473
E to Z ↓	0.0620	0.0625	1.2759	0.6567
E to Z ↑	0.0331	0.0345	2.0660	1.0441
F to Z ↓	0.0583	0.0580	1.2710	0.6541
F to Z ↑	0.0345	0.0357	2.0671	1.0440

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	2.703e-06	1.536e-09
X8_P4	4.095e-06	1.536e-09
X17_P4	6.869e-06	1.655e-09
X33_P4	1.225e-05	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	4.087e-05	4.495e-05	5.234e-05	9.811e-05
B (output stable)	9.696e-05	1.052e-04	1.090e-04	1.359e-04
C (output stable)	2.269e-05	2.594e-05	3.334e-05	6.276e-05
D (output stable)	2.756e-05	3.225e-05	4.059e-05	1.089e-04
E (output stable)	3.781e-05	4.324e-05	5.324e-05	7.876e-05
F (output stable)	3.784e-05	4.389e-05	5.728e-05	1.142e-04

A to Z	2.617e-03	3.393e-03	5.025e-03	9.428e-03
B to Z	2.423e-03	3.162e-03	4.729e-03	8.930e-03
C to Z	2.210e-03	2.907e-03	4.379e-03	8.225e-03
D to Z	2.129e-03	2.800e-03	4.201e-03	7.793e-03
E to Z	1.749e-03	2.395e-03	3.624e-03	7.076e-03
F to Z	1.659e-03	2.276e-03	3.442e-03	6.635e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

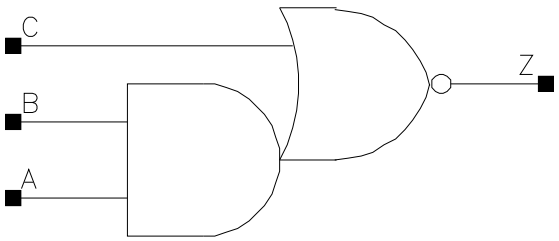
Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	-3.235e-06	-3.007e-06	-2.648e-06	-4.813e-06
B (output stable)	-3.790e-06	-2.922e-06	-1.590e-06	-4.780e-06
C (output stable)	4.375e-06	6.375e-06	1.019e-05	2.717e-05
D (output stable)	4.224e-06	6.081e-06	8.948e-06	2.521e-05
E (output stable)	2.126e-05	2.666e-05	3.710e-05	6.246e-05
F (output stable)	1.929e-05	2.442e-05	3.513e-05	6.134e-05
A to Z	-1.237e-06	-8.147e-07	3.336e-07	1.040e-06
B to Z	-1.116e-06	-5.149e-07	5.490e-07	1.572e-06
C to Z	-3.096e-07	3.517e-08	6.681e-07	1.303e-06
D to Z	-2.506e-07	5.518e-08	7.192e-07	1.350e-06
E to Z	-3.432e-07	-2.984e-07	-4.599e-07	-8.216e-07
F to Z	-3.119e-07	-3.316e-07	-4.182e-07	-7.283e-07

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008
X44_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X33_P4	X44_P4
A	0.0007	0.0021	0.0041	0.0056
B	0.0007	0.0019	0.0038	0.0051
C	0.0008	0.0022	0.0044	0.0057

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0137	0.0143	4.6920	1.5927
A to Z ↑	0.0243	0.0247	9.2413	3.0690
B to Z ↓	0.0132	0.0135	4.7207	1.6102
B to Z ↑	0.0205	0.0203	9.1352	3.0684
C to Z ↓	0.0131	0.0133	2.4991	0.8585
C to Z ↑	0.0266	0.0266	8.4560	2.8272
	X33_P4	**X44_P4**	**X33_P4**	**X44_P4**
A to Z ↓	0.0146	0.0146	0.8087	0.6130

A to Z ↑	0.0248	0.0248	1.5368	1.1629
B to Z ↓	0.0134	0.0134	0.8164	0.6181
B to Z ↑	0.0201	0.0200	1.5344	1.1585
C to Z ↓	0.0148	0.0150	0.5116	0.3987
C to Z ↑	0.0271	0.0269	1.4130	1.0679

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P4	2.138e-06	8.218e-10
X17_P4	5.753e-06	1.536e-09
X33_P4	1.066e-05	2.608e-09
X44_P4	1.417e-05	3.323e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	2.645e-05	8.421e-05	1.894e-04	2.481e-04
B (output stable)	3.127e-05	1.494e-04	3.272e-04	4.251e-04
C (output stable)	8.811e-05	2.741e-04	5.984e-04	7.816e-04
A to Z	8.486e-04	2.714e-03	5.496e-03	7.261e-03
B to Z	6.799e-04	2.000e-03	3.972e-03	5.233e-03
C to Z	1.225e-03	3.669e-03	7.510e-03	9.872e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

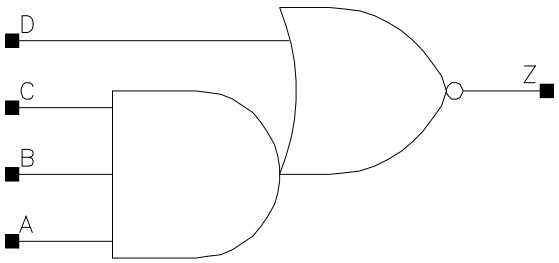
Pin Cycle (vdds)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	2.049e-05	4.983e-05	1.109e-04	1.414e-04
B (output stable)	2.046e-05	4.995e-05	1.102e-04	1.408e-04
C (output stable)	-2.664e-06	-6.284e-06	-1.506e-05	-1.899e-05
A to Z	1.900e-08	-1.111e-06	-4.031e-06	-5.491e-06
B to Z	-2.463e-07	-9.070e-07	-1.693e-06	-2.515e-06
C to Z	8.923e-07	2.236e-06	2.586e-06	4.333e-06

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X29_P4	1.200	3.536	4.2432
X38_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X29_P4	X38_P4
A	0.0007	0.0042	0.0055
B	0.0007	0.0040	0.0053
C	0.0007	0.0038	0.0051
D	0.0008	0.0044	0.0055

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X29_P4	X5_P4	X29_P4
A to Z ↓	0.0199	0.0212	6.9233	1.1883
A to Z ↑	0.0308	0.0307	9.2380	1.5242
B to Z ↓	0.0199	0.0204	6.9325	1.1912
B to Z ↑	0.0278	0.0274	9.2319	1.5330
C to Z ↓	0.0189	0.0185	6.9481	1.1958
C to Z ↑	0.0244	0.0233	9.1417	1.5405
D to Z ↓	0.0154	0.0173	2.5469	0.5163

D to Z ↑	0.0304	0.0308	7.8751	1.3112
	X38_P4		**X38_P4**	
A to Z ↓	0.0208		0.9138	
A to Z ↑	0.0300		1.1473	
B to Z ↓	0.0202		0.9156	
B to Z ↑	0.0269		1.1560	
C to Z ↓	0.0182		0.9193	
C to Z ↑	0.0227		1.1652	
D to Z ↓	0.0180		0.4289	
D to Z ↑	0.0301		0.9885	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P4	2.126e-06	9.409e-10
X29_P4	1.047e-05	3.442e-09
X38_P4	1.320e-05	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P4	X29_P4	X38_P4
A (output stable)	1.784e-05	1.556e-04	1.949e-04
B (output stable)	2.649e-05	2.666e-04	3.398e-04
C (output stable)	4.823e-05	5.402e-04	6.724e-04
D (output stable)	1.105e-04	9.092e-04	1.184e-03
A to Z	1.290e-03	8.199e-03	1.043e-02
B to Z	1.116e-03	6.712e-03	8.587e-03
C to Z	9.434e-04	5.188e-03	6.576e-03
D to Z	1.615e-03	9.913e-03	1.269e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

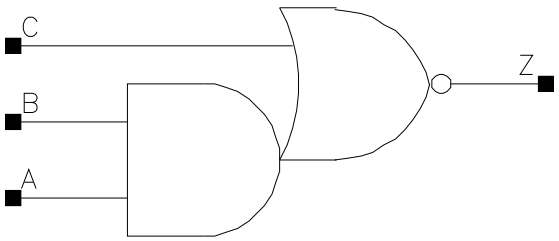
Pin Cycle (vdds)	X5_P4	X29_P4	X38_P4
A (output stable)	1.024e-05	7.494e-05	9.631e-05
B (output stable)	9.457e-06	7.179e-05	9.268e-05
C (output stable)	9.712e-06	7.136e-05	9.071e-05
D (output stable)	-2.933e-06	-4.427e-05	-5.369e-05
A to Z	4.500e-08	-5.085e-06	-1.562e-06
B to Z	-1.420e-07	-2.948e-06	-3.960e-06
C to Z	-6.600e-08	-1.332e-06	-1.610e-06
D to Z	-1.577e-07	-2.249e-06	-2.130e-06

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X11_P4	1.200	1.088	1.3056
X16_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X11_P4	X16_P4	X23_P4
A	0.0008	0.0015	0.0023	0.0030
B	0.0008	0.0015	0.0021	0.0028
C	0.0008	0.0013	0.0020	0.0028
	X46_P4			
A	0.0058			
B	0.0054			
C	0.0055			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X11_P4	X6_P4	X11_P4
A to Z ↓	0.0155	0.0167	4.5604	2.3051
A to Z ↑	0.0285	0.0301	9.2303	4.5082
B to Z ↓	0.0159	0.0161	4.5890	2.3214

B to Z ↑	0.0256	0.0262	9.1432	4.5158
C to Z ↓	0.0098	0.0102	2.5644	1.5083
C to Z ↑	0.0200	0.0194	8.4039	4.1278
	X16_P4	**X23_P4**	**X16_P4**	**X23_P4**
A to Z ↓	0.0161	0.0164	1.5945	1.1965
A to Z ↑	0.0283	0.0288	3.0264	2.2847
B to Z ↓	0.0159	0.0158	1.6076	1.2053
B to Z ↑	0.0244	0.0249	3.0231	2.2892
C to Z ↓	0.0103	0.0092	1.0598	0.6574
C to Z ↑	0.0187	0.0191	2.7700	2.0945
	X46_P4		**X46_P4**	
A to Z ↓	0.0159		0.6136	
A to Z ↑	0.0277		1.1739	
B to Z ↓	0.0154		0.6180	
B to Z ↑	0.0237		1.1710	
C to Z ↓	0.0093		0.3379	
C to Z ↑	0.0188		1.0752	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P4	2.118e-06	8.218e-10
X11_P4	4.146e-06	1.298e-09
X16_P4	5.471e-06	1.536e-09
X23_P4	7.959e-06	2.013e-09
X46_P4	1.503e-05	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	2.561e-05	7.099e-05	9.273e-05	1.322e-04
B (output stable)	3.141e-05	1.319e-04	1.451e-04	2.259e-04
C (output stable)	7.972e-05	1.871e-04	2.551e-04	3.682e-04
A to Z	1.256e-03	2.815e-03	3.804e-03	5.216e-03
B to Z	1.082e-03	2.282e-03	3.053e-03	4.150e-03
C to Z	6.420e-04	1.295e-03	1.784e-03	2.455e-03
	X46_P4			
A (output stable)	2.380e-04			
B (output stable)	3.957e-04			
C (output stable)	5.979e-04			
A to Z	9.557e-03			
B to Z	7.544e-03			
C to Z	4.552e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	-3.344e-07	-1.211e-06	-1.072e-06	-1.572e-06
B (output stable)	-3.829e-07	-1.274e-06	-1.115e-06	-2.012e-06
C (output stable)	5.357e-05	1.429e-04	1.387e-04	1.922e-04
A to Z	1.515e-06	9.060e-07	2.433e-06	4.233e-06
B to Z	1.212e-06	1.784e-06	2.869e-06	4.091e-06
C to Z	5.910e-08	-1.949e-07	1.509e-07	1.761e-07

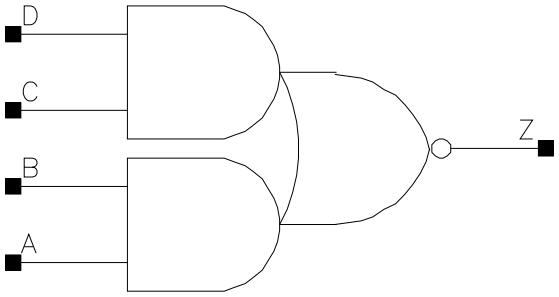
	X46_P4			
A (output stable)	-2.027e-06			
B (output stable)	-2.749e-06			
C (output stable)	3.165e-04			
A to Z	3.974e-06			
B to Z	7.408e-06			
C to Z	3.297e-07			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P4	X10_P4	X16_P4	X21_P4
A	0.0006	0.0016	0.0023	0.0029
B	0.0006	0.0014	0.0021	0.0028
C	0.0006	0.0015	0.0021	0.0028
D	0.0006	0.0013	0.0019	0.0026
	X42_P4			
A	0.0059			
B	0.0055			
C	0.0055			
D	0.0052			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X10_P4**	**X4_P4**	**X10_P4**
A to Z ↓	0.0174	0.0171	5.7196	2.2345
A to Z ↑	0.0363	0.0310	12.7551	4.1560
B to Z ↓	0.0181	0.0179	5.7524	2.2496
B to Z ↑	0.0330	0.0287	12.7237	4.2273
C to Z ↓	0.0140	0.0133	5.8177	2.2410
C to Z ↑	0.0277	0.0240	12.6062	4.1269
D to Z ↓	0.0140	0.0132	5.8697	2.2638
D to Z ↑	0.0242	0.0210	12.5731	4.1717
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0185	0.0184	1.6031	1.2016
A to Z ↑	0.0324	0.0320	2.7961	2.1446
B to Z ↓	0.0188	0.0182	1.6133	1.2096
B to Z ↑	0.0289	0.0284	2.7952	2.1453
C to Z ↓	0.0145	0.0145	1.5977	1.2000
C to Z ↑	0.0249	0.0252	2.7656	2.1196
D to Z ↓	0.0138	0.0132	1.6137	1.2120
D to Z ↑	0.0210	0.0210	2.7670	2.1214
	X42_P4		**X42_P4**	
A to Z ↓	0.0190		0.6217	
A to Z ↑	0.0322		1.0765	
B to Z ↓	0.0186		0.6259	
B to Z ↑	0.0283		1.0720	
C to Z ↓	0.0149		0.6152	
C to Z ↑	0.0253		1.0654	
D to Z ↓	0.0137		0.6204	
D to Z ↑	0.0211		1.0626	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	1.963e-06	9.409e-10
X10_P4	5.156e-06	1.536e-09
X16_P4	6.921e-06	1.894e-09
X21_P4	9.394e-06	2.489e-09
X42_P4	1.805e-05	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	2.705e-05	6.389e-05	1.264e-04	1.687e-04
B (output stable)	3.214e-05	8.057e-05	2.431e-04	3.508e-04
C (output stable)	2.700e-05	6.688e-05	1.256e-04	1.726e-04
D (output stable)	3.391e-05	8.601e-05	2.432e-04	3.556e-04
A to Z	1.302e-03	3.153e-03	5.003e-03	6.457e-03
B to Z	1.148e-03	2.784e-03	4.237e-03	5.422e-03
C to Z	7.553e-04	1.855e-03	2.974e-03	3.977e-03
D to Z	6.215e-04	1.514e-03	2.249e-03	2.933e-03
	X42_P4			
A (output stable)	3.229e-04			
B (output stable)	6.438e-04			
C (output stable)	3.286e-04			
D (output stable)	6.454e-04			

A to Z	1.266e-02			
B to Z	1.063e-02			
C to Z	7.744e-03			
D to Z	5.774e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

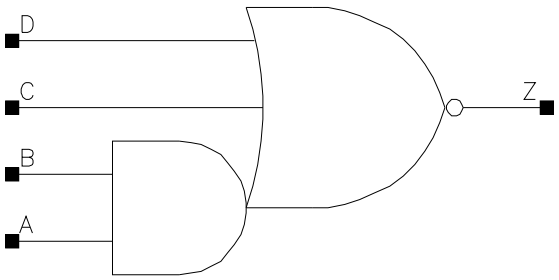
Pin Cycle (vdds)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	-6.144e-07	-8.575e-07	-1.398e-06	-1.533e-06
B (output stable)	-6.210e-07	-9.185e-07	-1.507e-06	-2.338e-06
C (output stable)	1.524e-05	3.046e-05	4.440e-05	5.481e-05
D (output stable)	1.533e-05	3.077e-05	4.463e-05	5.357e-05
A to Z	7.360e-07	2.896e-06	2.803e-06	3.492e-06
B to Z	7.483e-07	2.167e-06	2.839e-06	3.874e-06
C to Z	-1.924e-07	-2.071e-07	-7.983e-07	-2.517e-06
D to Z	-7.347e-08	-3.537e-07	-5.683e-07	-1.102e-06
	X42_P4			
A (output stable)	-2.881e-06			
B (output stable)	-4.880e-06			
C (output stable)	1.006e-04			
D (output stable)	9.909e-05			
A to Z	5.790e-06			
B to Z	4.820e-06			
C to Z	-3.695e-06			
D to Z	-2.173e-06			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X35_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P4	X35_P4
A	0.0007	0.0054
B	0.0007	0.0049
C	0.0007	0.0052
D	0.0008	0.0050

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X35_P4	X5_P4	X35_P4
A to Z ↓	0.0156	0.0162	4.7506	0.6939
A to Z ↑	0.0324	0.0305	14.1106	1.7798
B to Z ↓	0.0157	0.0155	4.7894	0.7011
B to Z ↑	0.0277	0.0250	14.0449	1.7786
C to Z ↓	0.0154	0.0194	2.6461	0.5129
C to Z ↑	0.0399	0.0388	13.3569	1.6855
D to Z ↓	0.0150	0.0182	2.6728	0.5114

D to Z ↑	0.0382	0.0361	13.3556	1.6866

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P4	1.658e-06	9.409e-10
X35_P4	9.967e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P4	X35_P4
A (output stable)	1.886e-05	1.960e-04
B (output stable)	2.230e-05	2.693e-04
C (output stable)	5.377e-05	6.078e-04
D (output stable)	2.605e-05	2.498e-04
A to Z	1.042e-03	7.622e-03
B to Z	8.715e-04	5.822e-03
C to Z	1.665e-03	1.295e-02
D to Z	1.417e-03	1.039e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

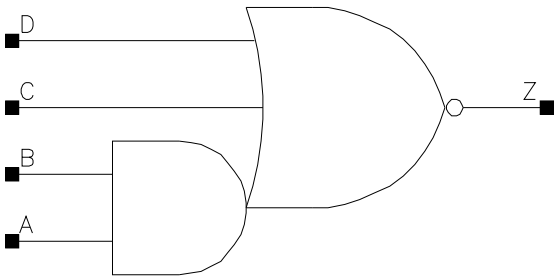
Pin Cycle (vdds)	X5_P4	X35_P4
A (output stable)	2.929e-05	1.866e-04
B (output stable)	3.344e-05	2.081e-04
C (output stable)	-4.277e-06	-3.848e-05
D (output stable)	1.437e-05	1.306e-04
A to Z	-1.109e-07	-5.604e-06
B to Z	-3.292e-07	-2.879e-06
C to Z	3.810e-07	7.833e-07
D to Z	3.493e-07	1.431e-06

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X17_P4	1.200	2.448	2.9376
X34_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P4	X17_P4	X34_P4
A	0.0007	0.0030	0.0060
B	0.0007	0.0028	0.0055
C	0.0006	0.0026	0.0050
D	0.0007	0.0023	0.0046

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X17_P4	X4_P4	X17_P4
A to Z ↓	0.0178	0.0191	5.1856	1.3633
A to Z ↑	0.0390	0.0410	14.1529	3.4797
B to Z ↓	0.0188	0.0191	5.2154	1.3712
B to Z ↑	0.0353	0.0357	14.0549	3.4829
C to Z ↓	0.0165	0.0161	4.3417	1.0575
C to Z ↑	0.0293	0.0309	13.2983	3.2815

D to Z ↓	0.0143	0.0129	4.4200	1.0621
D to Z ↑	0.0251	0.0228	13.3288	3.2907
	X34_P4		**X34_P4**	
A to Z ↓	0.0189		0.6977	
A to Z ↑	0.0402		1.7635	
B to Z ↓	0.0190		0.7016	
B to Z ↑	0.0351		1.7589	
C to Z ↓	0.0162		0.5544	
C to Z ↑	0.0300		1.6602	
D to Z ↓	0.0130		0.5583	
D to Z ↑	0.0224		1.6655	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	1.356e-06	9.409e-10
X17_P4	5.195e-06	2.489e-09
X34_P4	9.864e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P4	X17_P4	X34_P4
A (output stable)	2.527e-05	1.235e-04	2.439e-04
B (output stable)	2.689e-05	1.671e-04	3.164e-04
C (output stable)	2.083e-05	1.616e-04	3.017e-04
D (output stable)	2.984e-05	2.444e-04	4.391e-04
A to Z	1.567e-03	6.841e-03	1.317e-02
B to Z	1.406e-03	5.801e-03	1.124e-02
C to Z	9.610e-04	4.191e-03	7.947e-03
D to Z	6.899e-04	2.548e-03	4.845e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

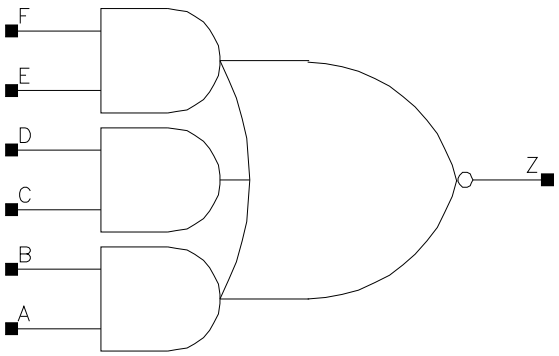
Pin Cycle (vdds)	X4_P4	X17_P4	X34_P4
A (output stable)	-1.231e-06	-5.910e-06	-1.120e-05
B (output stable)	-1.243e-06	-6.456e-06	-1.180e-05
C (output stable)	1.741e-05	5.407e-05	1.088e-04
D (output stable)	3.303e-05	1.865e-04	3.320e-04
A to Z	1.837e-06	4.286e-06	1.057e-05
B to Z	1.655e-06	5.614e-06	1.147e-05
C to Z	4.100e-08	1.391e-06	2.389e-06
D to Z	-3.148e-07	-9.101e-07	-2.062e-06

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X8_P4	1.200	2.176	2.6112
X13_P4	1.200	2.720	3.2640
X17_P4	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P4	X8_P4	X13_P4	X17_P4
A	0.0007	0.0015	0.0022	0.0029

B	0.0007	0.0014	0.0021	0.0027
C	0.0007	0.0014	0.0021	0.0027
D	0.0007	0.0013	0.0020	0.0026
E	0.0009	0.0014	0.0020	0.0026
F	0.0007	0.0013	0.0019	0.0025

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0204	0.0243	4.5836	2.6496
A to Z ↑	0.0551	0.0541	13.5733	6.2478
B to Z ↓	0.0219	0.0247	4.6039	2.6592
B to Z ↑	0.0513	0.0494	13.5585	6.2549
C to Z ↓	0.0191	0.0223	4.5394	2.6500
C to Z ↑	0.0481	0.0484	13.5976	6.2555
D to Z ↓	0.0201	0.0228	4.5694	2.6642
D to Z ↑	0.0442	0.0437	13.5459	6.2485
E to Z ↓	0.0150	0.0176	4.4370	2.6456
E to Z ↑	0.0349	0.0350	13.4379	6.1944
F to Z ↓	0.0153	0.0174	4.4815	2.6712
F to Z ↑	0.0307	0.0303	13.4984	6.1972
	X13_P4	X17_P4	X13_P4	X17_P4
A to Z ↓	0.0232	0.0234	1.8021	1.3727
A to Z ↑	0.0504	0.0507	4.1408	3.1502
B to Z ↓	0.0242	0.0239	1.8079	1.3778
B to Z ↑	0.0464	0.0460	4.1498	3.1494
C to Z ↓	0.0215	0.0215	1.8161	1.3587
C to Z ↑	0.0445	0.0450	4.1487	3.1589
D to Z ↓	0.0223	0.0215	1.8253	1.3663
D to Z ↑	0.0405	0.0403	4.1507	3.1535
E to Z ↓	0.0171	0.0170	1.8078	1.3582
E to Z ↑	0.0329	0.0329	4.1139	3.1233
F to Z ↓	0.0169	0.0161	1.8239	1.3712
F to Z ↑	0.0283	0.0281	4.1170	3.1314

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	2.965e-06	1.298e-09
X8_P4	5.650e-06	2.251e-09
X13_P4	7.622e-06	2.727e-09
X17_P4	1.023e-05	3.561e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	4.797e-05	1.107e-04	1.517e-04	2.030e-04
B (output stable)	5.259e-05	1.832e-04	2.113e-04	3.256e-04
C (output stable)	3.142e-05	7.383e-05	1.015e-04	1.450e-04
D (output stable)	3.863e-05	1.554e-04	1.710e-04	2.695e-04
E (output stable)	3.722e-05	9.412e-05	1.355e-04	1.844e-04
F (output stable)	4.285e-05	1.628e-04	1.999e-04	3.002e-04

A to Z	2.511e-03	5.295e-03	7.312e-03	9.690e-03
B to Z	2.326e-03	4.773e-03	6.653e-03	8.690e-03
C to Z	1.887e-03	4.156e-03	5.552e-03	7.408e-03
D to Z	1.720e-03	3.681e-03	4.949e-03	6.467e-03
E to Z	1.181e-03	2.716e-03	3.637e-03	4.819e-03
F to Z	1.020e-03	2.245e-03	3.006e-03	3.876e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

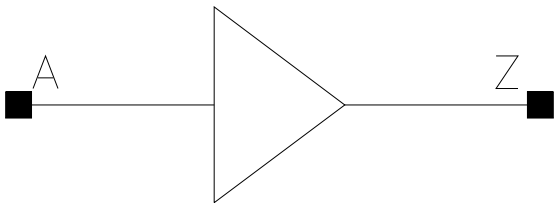
Pin Cycle (vdds)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	-3.790e-06	-7.689e-06	-7.993e-06	-1.032e-05
B (output stable)	-4.051e-06	-7.801e-06	-8.131e-06	-1.126e-05
C (output stable)	1.403e-05	2.654e-05	3.279e-05	4.285e-05
D (output stable)	1.323e-05	2.360e-05	3.029e-05	3.893e-05
E (output stable)	3.957e-05	8.901e-05	9.951e-05	1.356e-04
F (output stable)	3.821e-05	8.524e-05	9.635e-05	1.297e-04
A to Z	4.798e-07	4.087e-07	1.818e-06	1.358e-06
B to Z	6.687e-07	1.207e-06	2.154e-06	2.096e-06
C to Z	1.170e-06	1.717e-06	2.417e-06	2.144e-06
D to Z	9.836e-07	2.279e-06	2.772e-06	3.727e-06
E to Z	-4.978e-07	-1.858e-06	-2.367e-06	-3.519e-06
F to Z	-4.749e-07	-9.063e-07	-1.476e-06	-2.121e-06

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.408	0.4896
X6_P4	1.200	0.408	0.4896
X8_P4	1.200	0.408	0.4896
X13_P4	1.200	0.544	0.6528
X16_P4	1.200	0.544	0.6528
X21_P4	1.200	0.680	0.8160
X25_P4	1.200	0.680	0.8160
X29_P4	1.200	0.952	1.1424
X33_P4	1.200	0.952	1.1424
X42_P4	1.200	1.088	1.3056
X50_P4	1.200	1.224	1.4688
X58_P4	1.200	1.496	1.7952
X67_P4	1.200	1.632	1.9584
X75_P4	1.200	1.768	2.1216
X84_P4	1.200	1.904	2.2848
X100_P4	1.200	2.312	2.7744
X134_P4	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0007	0.0007	0.0007	0.0007
	X16_P4	X21_P4	X25_P4	X29_P4
A	0.0007	0.0010	0.0010	0.0014
	X33_P4	X42_P4	X50_P4	X58_P4
A	0.0013	0.0015	0.0018	0.0027

	X67_P4	X75_P4	X84_P4	X100_P4
A	0.0027	0.0027	0.0026	0.0035
	X134_P4			
A	0.0044			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0336	0.0335	4.5792	3.3022
A to Z ↑	0.0259	0.0255	8.2085	5.9479
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0347	0.0387	2.4299	1.5845
A to Z ↑	0.0262	0.0290	4.2112	2.7679
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0409	0.0345	1.2520	0.9703
A to Z ↑	0.0303	0.0262	2.1104	1.6581
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0360	0.0344	0.8310	0.7056
A to Z ↑	0.0271	0.0254	1.3862	1.1808
	X33_P4	**X42_P4**	**X33_P4**	**X42_P4**
A to Z ↓	0.0361	0.0348	0.6250	0.5067
A to Z ↑	0.0265	0.0264	1.0358	0.8332
	X50_P4	**X58_P4**	**X50_P4**	**X58_P4**
A to Z ↓	0.0342	0.0319	0.4215	0.3632
A to Z ↑	0.0257	0.0244	0.6911	0.5937
	X67_P4	**X75_P4**	**X67_P4**	**X75_P4**
A to Z ↓	0.0332	0.0351	0.3191	0.2880
A to Z ↑	0.0252	0.0266	0.5201	0.4657
	X84_P4	**X100_P4**	**X84_P4**	**X100_P4**
A to Z ↓	0.0365	0.0343	0.2609	0.2193
A to Z ↑	0.0275	0.0261	0.4201	0.3512
	X134_P4		**X134_P4**	
A to Z ↓	0.0359		0.1698	
A to Z ↑	0.0275		0.2682	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	1.883e-06	7.027e-10
X6_P4	2.282e-06	7.027e-10
X8_P4	2.733e-06	7.027e-10
X13_P4	3.570e-06	8.218e-10
X16_P4	4.334e-06	8.218e-10
X21_P4	5.849e-06	9.409e-10
X25_P4	6.384e-06	9.409e-10
X29_P4	7.661e-06	1.179e-09
X33_P4	7.995e-06	1.179e-09
X42_P4	9.850e-06	1.298e-09
X50_P4	1.180e-05	1.417e-09
X58_P4	1.452e-05	1.655e-09
X67_P4	1.588e-05	1.775e-09
X75_P4	1.724e-05	1.894e-09

X84_P4	1.860e-05	2.013e-09
X100_P4	2.267e-05	2.370e-09
X134_P4	2.947e-05	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	1.264e-03	1.400e-03	1.641e-03	2.139e-03
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	2.505e-03	3.463e-03	3.861e-03	4.304e-03
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	4.781e-03	5.941e-03	6.935e-03	8.594e-03
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	9.400e-03	1.064e-02	1.157e-02	1.376e-02
	X134_P4			
A to Z	1.854e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

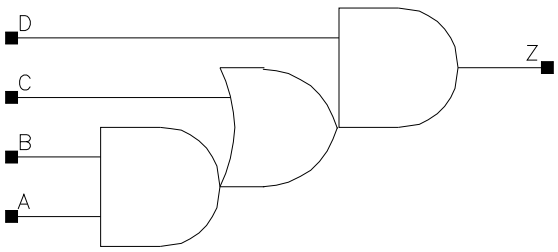
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	-1.805e-07	-2.539e-07	-1.817e-07	-1.305e-07
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	-1.307e-07	-3.068e-07	-1.003e-07	-2.501e-07
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	-4.932e-07	-4.200e-07	-1.029e-06	-3.876e-07
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	-8.171e-07	-1.220e-06	-8.970e-07	-9.380e-07
	X134_P4			
A to Z	-1.699e-06			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.632	1.9584
X25_P4	1.200	1.768	2.1216
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0008	0.0019	0.0018	0.0018
B	0.0009	0.0016	0.0016	0.0016
C	0.0009	0.0021	0.0021	0.0021
D	0.0014	0.0018	0.0018	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0478	0.0451	2.4896	1.2384
A to Z ↑	0.0403	0.0377	4.2636	2.0767
B to Z ↓	0.0447	0.0414	2.4831	1.2357
B to Z ↑	0.0401	0.0367	4.2593	2.0742
C to Z ↓	0.0395	0.0361	2.4769	1.2328
C to Z ↑	0.0301	0.0272	4.2252	2.0545

D to Z ↓	0.0367	0.0322	2.4507	1.2221
D to Z ↑	0.0355	0.0307	4.2303	2.0579
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0495	0.0522	0.8447	0.6381
A to Z ↑	0.0414	0.0433	1.4035	1.0548
B to Z ↓	0.0460	0.0495	0.8431	0.6369
B to Z ↑	0.0405	0.0432	1.4024	1.0543
C to Z ↓	0.0407	0.0438	0.8401	0.6345
C to Z ↑	0.0303	0.0322	1.3884	1.0413
D to Z ↓	0.0349	0.0366	0.8295	0.6241
D to Z ↑	0.0336	0.0352	1.3908	1.0431

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	3.641e-06	1.179e-09
X17_P4	6.726e-06	1.775e-09
X25_P4	7.873e-06	1.894e-09
X33_P4	9.024e-06	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	7.551e-05	1.561e-04	1.572e-04	1.424e-04
B (output stable)	8.667e-05	1.886e-04	1.900e-04	1.609e-04
C (output stable)	2.325e-04	3.731e-04	3.735e-04	3.561e-04
D (output stable)	9.485e-05	1.317e-04	1.322e-04	1.322e-04
A to Z	2.781e-03	5.059e-03	6.262e-03	7.148e-03
B to Z	2.594e-03	4.557e-03	5.760e-03	6.746e-03
C to Z	2.153e-03	3.632e-03	4.835e-03	5.770e-03
D to Z	2.863e-03	4.830e-03	6.007e-03	6.879e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

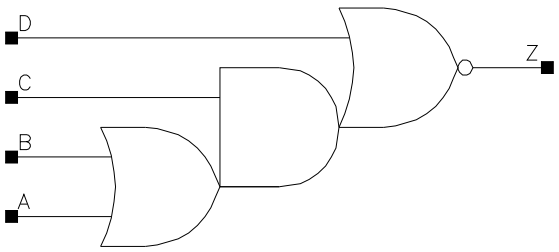
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	-5.870e-07	-1.134e-06	-1.145e-06	-1.025e-06
B (output stable)	-5.598e-07	-1.060e-06	-1.066e-06	-9.714e-07
C (output stable)	1.061e-05	1.822e-05	1.832e-05	1.842e-05
D (output stable)	8.334e-08	7.116e-08	8.407e-08	8.100e-08
A to Z	5.390e-07	1.353e-06	1.639e-06	1.378e-06
B to Z	9.270e-07	2.172e-06	1.895e-06	1.917e-06
C to Z	-2.883e-07	-3.879e-07	-4.916e-07	-4.438e-07
D to Z	-3.182e-07	7.854e-08	-1.064e-08	-2.365e-07

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.952	1.1424
X11_P4	1.200	1.496	1.7952
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X16_P4	X21_P4
A	0.0008	0.0015	0.0023	0.0029
B	0.0008	0.0014	0.0022	0.0029
C	0.0008	0.0014	0.0021	0.0029
D	0.0010	0.0014	0.0021	0.0028

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0187	0.0178	4.4399	2.3356
A to Z ↑	0.0472	0.0434	13.8579	7.1287
B to Z ↓	0.0182	0.0176	4.3511	2.3074
B to Z ↑	0.0443	0.0412	13.8578	7.1302
C to Z ↓	0.0167	0.0158	4.0736	2.1492
C to Z ↑	0.0290	0.0265	9.0312	4.6093

D to Z ↓	0.0109	0.0094	2.4443	1.2447
D to Z ↑	0.0247	0.0212	9.7239	4.9713
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0179	0.0182	1.5934	1.2163
A to Z ↑	0.0408	0.0428	4.6321	3.5471
B to Z ↓	0.0173	0.0177	1.5982	1.2172
B to Z ↑	0.0396	0.0405	4.6316	3.5475
C to Z ↓	0.0160	0.0160	1.4847	1.1291
C to Z ↑	0.0259	0.0262	3.0543	2.2917
D to Z ↓	0.0094	0.0094	0.8736	0.6665
D to Z ↑	0.0199	0.0199	3.2748	2.4726

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P4	2.415e-06	1.179e-09
X11_P4	4.412e-06	1.655e-09
X16_P4	5.778e-06	1.894e-09
X21_P4	7.723e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	3.026e-05	5.544e-05	7.150e-05	1.201e-04
B (output stable)	7.175e-06	1.353e-05	1.584e-05	2.598e-05
C (output stable)	8.256e-05	1.676e-04	2.301e-04	3.240e-04
D (output stable)	8.387e-05	1.719e-04	2.368e-04	3.402e-04
A to Z	2.026e-03	3.524e-03	4.927e-03	6.948e-03
B to Z	1.661e-03	2.915e-03	4.207e-03	5.717e-03
C to Z	1.397e-03	2.361e-03	3.408e-03	4.697e-03
D to Z	8.166e-04	1.347e-03	1.811e-03	2.413e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

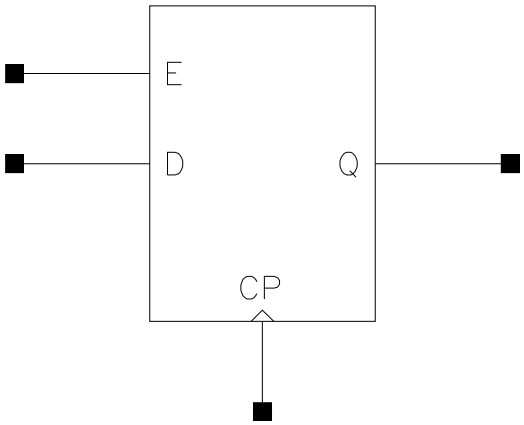
Pin Cycle (vdds)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	-1.777e-06	-2.444e-06	-2.642e-06	-5.707e-06
B (output stable)	1.065e-05	1.518e-05	2.239e-05	3.635e-05
C (output stable)	-1.980e-06	-3.355e-06	-4.695e-06	-7.539e-06
D (output stable)	6.699e-05	1.398e-04	1.912e-04	2.740e-04
A to Z	1.246e-06	1.063e-06	4.257e-06	5.643e-06
B to Z	4.760e-07	1.479e-06	2.424e-06	3.146e-06
C to Z	1.329e-06	2.486e-06	3.250e-06	7.411e-06
D to Z	-1.324e-07	4.119e-07	4.872e-07	5.900e-08

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.128	3.7536
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0011	0.0011	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0543	0.0623	2.4793	1.2891
CP to Q ↑	0.0652	0.0691	4.2620	2.1371
	X33_P4		**X33_P4**	
CP to Q ↓	0.0926		0.6338	
CP to Q ↑	0.1116		1.0583	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0798	0.0798	0.0798
CP ↑	min_pulse_width to CP	0.0443	0.0540	0.0406
D ↓	hold_rising to CP	-0.0364	-0.0364	-0.0361
D ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.0856	0.0856	0.0856
D ↑	setup_rising to CP	0.0436	0.0436	0.0439
E ↓	hold_rising to CP	-0.0263	-0.0263	-0.0263
E ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
E ↓	setup_rising to CP	0.0773	0.0773	0.0773
E ↑	setup_rising to CP	0.0932	0.0932	0.0932

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	1.083e-05	2.966e-09
X17_P4	1.231e-05	3.085e-09
X33_P4	1.705e-05	3.561e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

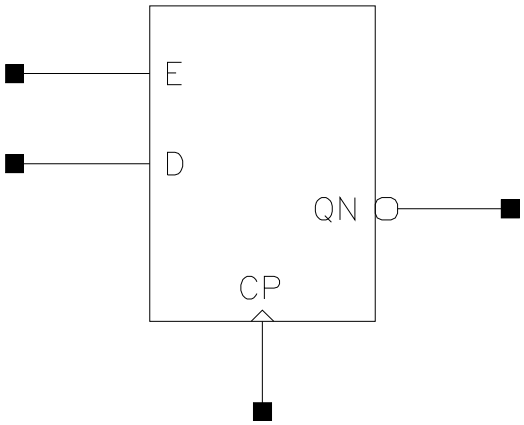
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.013e-03	3.013e-03	3.017e-03
Clock 100Mhz Data 25Mhz	6.407e-03	6.880e-03	8.923e-03
Clock 100Mhz Data 50Mhz	9.802e-03	1.075e-02	1.483e-02
Clock = 0 Data 100Mhz	3.816e-03	3.816e-03	3.817e-03
Clock = 1 Data 100Mhz	1.074e-03	1.074e-03	1.074e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.264	3.9168
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0011	0.0011	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0922	0.0861	2.5454	1.2189
CP to QN ↑	0.0728	0.0749	4.3221	2.0767
	X33_P4		**X33_P4**	
CP to QN ↓	0.0916		0.6360	
CP to QN ↑	0.0823		1.0617	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0798	0.0798	0.0798
CP ↑	min_pulse_width to CP	0.0369	0.0406	0.0491
D ↓	hold_rising to CP	-0.0361	-0.0364	-0.0364
D ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.0856	0.0856	0.0856
D ↑	setup_rising to CP	0.0436	0.0436	0.0436
E ↓	hold_rising to CP	-0.0263	-0.0263	-0.0263
E ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
E ↓	setup_rising to CP	0.0773	0.0773	0.0773
E ↑	setup_rising to CP	0.0932	0.0932	0.0932

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	1.077e-05	2.966e-09
X17_P4	1.315e-05	3.204e-09
X33_P4	1.666e-05	3.561e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

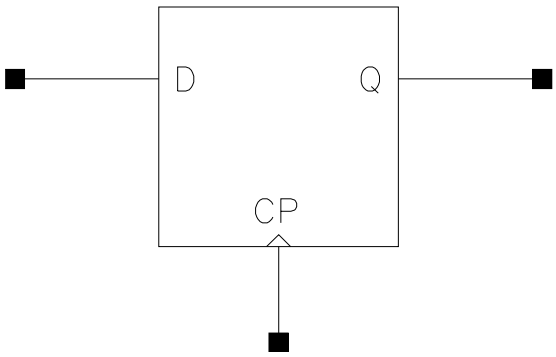
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.009e-03	3.010e-03	3.011e-03
Clock 100Mhz Data 25Mhz	6.452e-03	7.325e-03	8.733e-03
Clock 100Mhz Data 50Mhz	9.895e-03	1.164e-02	1.446e-02
Clock = 0 Data 100Mhz	3.817e-03	3.817e-03	3.816e-03
Clock = 1 Data 100Mhz	1.074e-03	1.074e-03	1.074e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.176	2.6112
X17_P4	1.200	2.448	2.9376
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0563	0.0618	2.4756	1.2807
CP to Q ↑	0.0664	0.0732	4.1422	2.1063
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to Q ↓	0.0781	0.0819	0.7677	0.6982
CP to Q ↑	0.0817	0.0840	1.1858	1.0796

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0701	0.0749	0.0749	0.0749
CP ↑	min_pulse_width to CP	0.0443	0.0502	0.0685	0.0733
D ↓	hold_rising to CP	0.0030	0.0030	0.0030	0.0030
D ↑	hold_rising to CP	0.0078	0.0082	0.0082	0.0078
D ↓	setup_rising to CP	0.0441	0.0462	0.0466	0.0462
D ↑	setup_rising to CP	0.0219	0.0219	0.0219	0.0219

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	8.803e-06	2.251e-09
X17_P4	1.039e-05	2.489e-09
X30_P4	1.291e-05	2.727e-09
X33_P4	1.316e-05	2.727e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

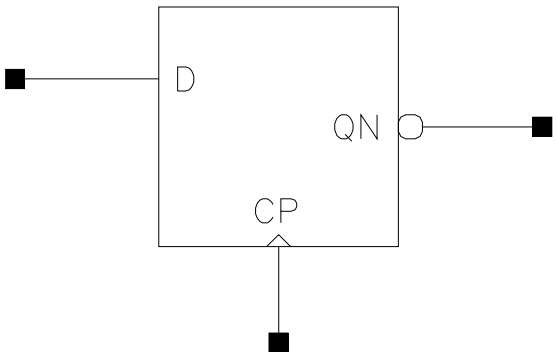
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.174e-03	3.194e-03	3.201e-03	3.205e-03
Clock 100Mhz Data 25Mhz	5.682e-03	6.443e-03	7.497e-03	7.760e-03
Clock 100Mhz Data 50Mhz	8.190e-03	9.693e-03	1.179e-02	1.231e-02
Clock = 0 Data 100Mhz	2.543e-03	2.628e-03	2.654e-03	2.667e-03
Clock = 1 Data 100Mhz	2.213e-05	2.225e-05	2.238e-05	2.242e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0539	0.0642	2.5466	1.3226
CP to QN ↑	0.0579	0.0611	4.1368	2.1006
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to QN ↓	0.0922	0.0923	0.7005	0.6344
CP to QN ↑	0.0761	0.0884	1.1460	1.0593

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0577	0.0615	0.0749	0.0701
CP ↑	min_pulse_width to CP	0.0406	0.0502	0.0417	0.0502
D ↓	hold_rising to CP	0.0097	0.0153	0.0034	0.0027
D ↑	hold_rising to CP	0.0103	0.0103	0.0082	0.0078
D ↓	setup_rising to CP	0.0319	0.0319	0.0462	0.0441
D ↑	setup_rising to CP	0.0268	0.0268	0.0219	0.0219

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	8.205e-06	2.013e-09
X17_P4	9.725e-06	2.132e-09
X30_P4	1.388e-05	2.727e-09
X33_P4	1.465e-05	2.847e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

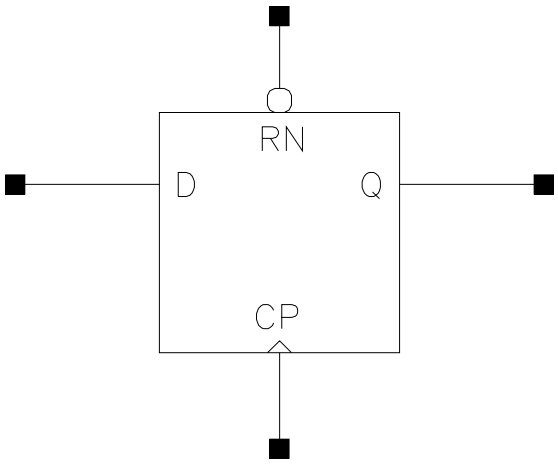
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.043e-03	3.044e-03	3.098e-03	3.121e-03
Clock 100Mhz Data 25Mhz	5.370e-03	5.888e-03	7.623e-03	8.002e-03
Clock 100Mhz Data 50Mhz	7.697e-03	8.732e-03	1.215e-02	1.288e-02
Clock = 0 Data 100Mhz	2.254e-03	2.253e-03	2.405e-03	2.440e-03
Clock = 1 Data 100Mhz	2.227e-05	2.218e-05	2.234e-05	2.246e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0006	0.0006
RN	0.0008	0.0008

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0647	0.0806	1.2947	0.7790
CP to Q ↑	0.0757	0.0839	2.1117	1.1900
RN to Q ↓	0.1041	0.1369	1.3951	0.8455

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0797	0.0797
CP ↑	min_pulse_width to CP	0.0540	0.0684
D ↓	hold_rising to CP	0.0033	0.0030
D ↑	hold_rising to CP	0.0029	0.0029
D ↓	setup_rising to CP	0.0514	0.0514
D ↑	setup_rising to CP	0.0324	0.0324
RN ↓	min_pulse_width to RN	0.1311	0.1653
RN ↑	recovery_rising to CP	0.0297	0.0293
RN ↑	removal_rising to CP	-0.0103	-0.0103

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P4	1.086e-05	3.085e-09
X30_P4	1.298e-05	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

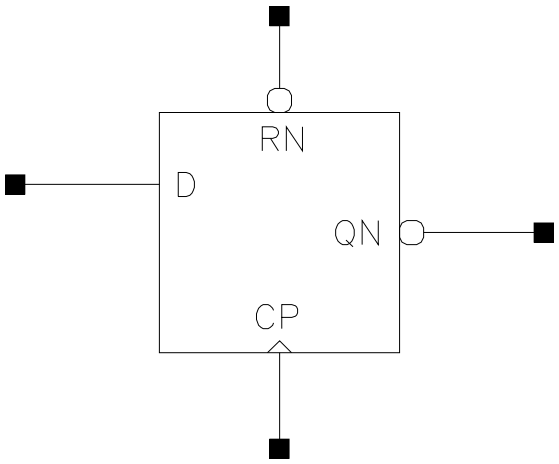
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	3.416e-03	3.414e-03
Clock 100Mhz Data 25Mhz	6.906e-03	7.934e-03
Clock 100Mhz Data 50Mhz	1.040e-02	1.245e-02
Clock = 0 Data 100Mhz	3.148e-03	3.150e-03
Clock = 1 Data 100Mhz	2.250e-05	2.259e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0006	0.0006
RN	0.0009	0.0009

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0891	0.0961	1.2099	0.7034
CP to QN ↑	0.0743	0.0802	2.0599	1.1507
RN to QN ↑	0.1118	0.1192	2.0714	1.1561

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0797	0.0797
CP ↑	min_pulse_width to CP	0.0417	0.0454
D ↓	hold_rising to CP	0.0033	0.0034
D ↑	hold_rising to CP	0.0029	0.0029
D ↓	setup_rising to CP	0.0514	0.0514
D ↑	setup_rising to CP	0.0268	0.0268
RN ↓	min_pulse_width to RN	0.1062	0.1089
RN ↑	recovery_rising to CP	0.0297	0.0272
RN ↑	removal_rising to CP	-0.0103	-0.0103

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P4	1.292e-05	3.085e-09
X30_P4	1.574e-05	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

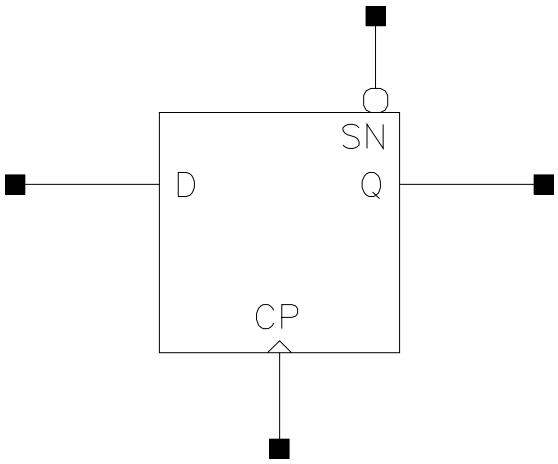
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	3.410e-03	3.413e-03
Clock 100Mhz Data 25Mhz	7.301e-03	8.250e-03
Clock 100Mhz Data 50Mhz	1.119e-02	1.309e-02
Clock = 0 Data 100Mhz	3.187e-03	3.176e-03
Clock = 1 Data 100Mhz	2.251e-05	2.256e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0011	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0653	0.0820	1.2963	0.7766
CP to Q ↑	0.0751	0.0837	2.1127	1.1904
SN to Q ↑	0.0772	0.0878	2.1236	1.1990

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0845	0.0845
CP ↑	min_pulse_width to CP	0.0539	0.0684
D ↓	hold_rising to CP	0.0033	0.0033
D ↑	hold_rising to CP	0.0054	0.0051
D ↓	setup_rising to CP	0.0563	0.0563
D ↑	setup_rising to CP	0.0275	0.0275
SN ↓	min_pulse_width to SN	0.0740	0.0864
SN ↑	recovery_rising to CP	0.0155	0.0155
SN ↑	removal_rising to CP	0.0357	0.0357

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P4	1.175e-05	3.085e-09
X30_P4	1.459e-05	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

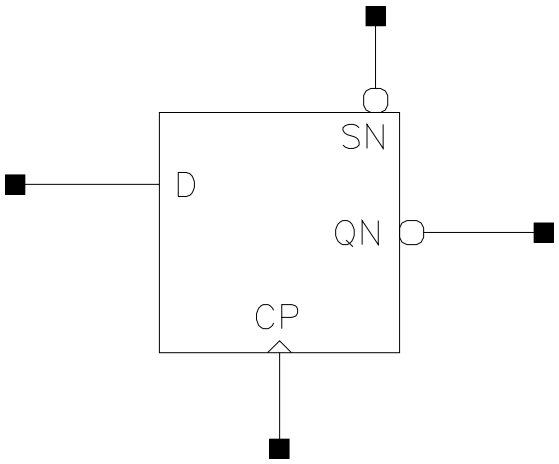
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	3.453e-03	3.446e-03
Clock 100Mhz Data 25Mhz	6.951e-03	7.987e-03
Clock 100Mhz Data 50Mhz	1.045e-02	1.253e-02
Clock = 0 Data 100Mhz	3.137e-03	3.136e-03
Clock = 1 Data 100Mhz	2.274e-05	2.279e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0011	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0885	0.0954	1.2125	0.7050
CP to QN ↑	0.0751	0.0806	2.0585	1.1494
SN to QN ↓	0.0906	0.0978	1.2117	0.7052

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0845	0.0845
CP ↑	min_pulse_width to CP	0.0454	0.0454
D ↓	hold_rising to CP	0.0034	0.0034
D ↑	hold_rising to CP	0.0029	0.0029
D ↓	setup_rising to CP	0.0563	0.0563
D ↑	setup_rising to CP	0.0275	0.0275
SN ↓	min_pulse_width to SN	0.0664	0.0664
SN ↑	recovery_rising to CP	0.0124	0.0124
SN ↑	removal_rising to CP	0.0357	0.0357

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P4	1.176e-05	3.085e-09
X30_P4	1.381e-05	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

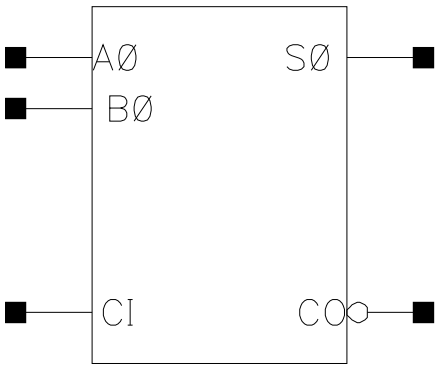
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	3.448e-03	3.448e-03
Clock 100Mhz Data 25Mhz	7.326e-03	8.258e-03
Clock 100Mhz Data 50Mhz	1.120e-02	1.307e-02
Clock = 0 Data 100Mhz	3.135e-03	3.136e-03
Clock = 1 Data 100Mhz	2.273e-05	2.279e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_P4	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_-P4	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_-P4	1.200	3.672	4.4064
C12T28SOI_LRS1_-FA1X33_P4	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_-FA1X8_P4	C12T28SOI_LR_-FA1X33_P4	C12T28SOI_LRS1_-FA1X8_P4	C12T28SOI_LRS1_-FA1X33_P4
A0	0.0029	0.0059	0.0027	0.0053
B0	0.0027	0.0058	0.0029	0.0050
CI	0.0020	0.0045	0.0020	0.0035

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P4	C12T28SOI_LR_-FA1X33_P4	C12T28SOI_LR_-FA1X8_P4	C12T28SOI_LR_-FA1X33_P4
A0 to CO ↓	0.0636	0.0681	2.5743	0.6859
A0 to CO ↑	0.0435	0.0439	4.2674	1.0956
A0 to S0 ↓	0.0643	0.0801	2.5518	0.6718
A0 to S0 ↑	0.0659	0.0790	4.2235	1.0792
B0 to CO ↓	0.0615	0.0677	2.5828	0.6897
B0 to CO ↑	0.0441	0.0453	4.2691	1.0916
B0 to S0 ↓	0.0642	0.0809	2.5521	0.6714
B0 to S0 ↑	0.0653	0.0796	4.2255	1.0800
CI to CO ↓	0.0586	0.0645	2.5924	0.6893
CI to CO ↑	0.0433	0.0434	4.2665	1.0952
CI to S0 ↓	0.0630	0.0796	2.5510	0.6713
CI to S0 ↑	0.0647	0.0790	4.2251	1.0795
	C12T28SOI_LRS1_-FA1X8_P4	C12T28SOI_LRS1_-FA1X33_P4	C12T28SOI_LRS1_-FA1X8_P4	C12T28SOI_LRS1_-FA1X33_P4
A0 to CO ↓	0.0405	0.0493	5.3406	0.9308
A0 to CO ↑	0.0322	0.0365	4.3095	1.0837
A0 to S0 ↓	0.0855	0.1038	2.7283	0.6972
A0 to S0 ↑	0.0775	0.0830	4.3999	1.0963
B0 to CO ↓	0.0408	0.0498	5.3411	0.9318
B0 to CO ↑	0.0306	0.0354	4.3055	1.0835
B0 to S0 ↓	0.0857	0.1061	2.7268	0.6971
B0 to S0 ↑	0.0777	0.0851	4.3996	1.0963
CI to CO ↓	0.0392	0.0654	5.3345	0.9455
CI to CO ↑	0.0344	0.0400	4.4062	1.0910
CI to S0 ↓	0.0478	0.0613	2.7310	0.6975
CI to S0 ↑	0.0405	0.0401	4.3989	1.0969

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_FA1X8_P4	8.540e-06	2.251e-09
C12T28SOI_LR_FA1X33_P4	2.239e-05	4.633e-09
C12T28SOI_LRS1_FA1X8_P4	1.926e-05	3.561e-09
C12T28SOI_LRS1_FA1X33_P4	3.976e-05	7.372e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P4	C12T28SOI_LR_-FA1X33_P4	C12T28SOI_LRS1_-FA1X8_P4	C12T28SOI_LRS1_-FA1X33_P4
A0 to CO	2.867e-03	7.860e-03	4.462e-03	1.080e-02
A0 to S0	2.912e-03	8.247e-03	5.994e-03	1.345e-02
B0 to CO	2.877e-03	7.965e-03	4.481e-03	1.094e-02
B0 to S0	2.810e-03	8.111e-03	6.069e-03	1.373e-02
CI to CO	2.845e-03	7.921e-03	3.163e-03	9.541e-03
CI to S0	2.788e-03	8.064e-03	3.559e-03	1.027e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P4	C12T28SOI_LR_-FA1X33_P4	C12T28SOI_LRS1_-FA1X8_P4	C12T28SOI_LRS1_-FA1X33_P4
A0 to CO	-6.295e-07	-9.497e-07	2.653e-06	6.282e-06

A0 to S0	-8.192e-07	-1.436e-06	4.027e-06	8.661e-06
B0 to CO	3.027e-06	5.821e-06	-1.541e-07	9.750e-09
B0 to S0	1.370e-05	2.634e-05	3.453e-06	6.849e-06
CI to CO	1.824e-05	3.489e-05	-5.175e-08	-7.871e-07
CI to S0	2.022e-05	3.237e-05	-2.625e-07	-8.528e-07

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X33_P4	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X33_P4
A0	0.0010	0.0029
B0	0.0009	0.0026

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
A0 to CO ↓	0.0444	0.0400	2.5407	0.6301
A0 to CO ↑	0.0411	0.0360	4.2354	1.0830
A0 to S0 ↓	0.0601	0.0555	2.4925	0.6311
A0 to S0 ↑	0.0553	0.0591	4.1784	1.0714
B0 to CO ↓	0.0434	0.0374	2.5413	0.6261
B0 to CO ↑	0.0428	0.0366	4.2355	1.0829
B0 to S0 ↓	0.0607	0.0538	2.4922	0.6313
B0 to S0 ↑	0.0548	0.0569	4.1776	1.0709

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	5.162e-06	1.417e-09
X33_P4	1.914e-05	2.966e-09

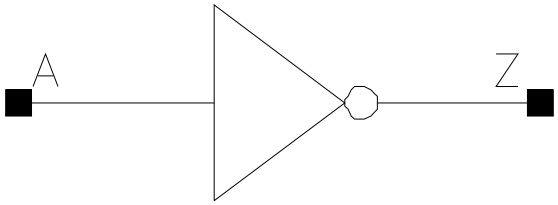
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X33_P4
A0 to CO	2.218e-03	7.120e-03
A0 to S0	2.035e-03	6.877e-03
B0 to CO	2.239e-03	7.122e-03
B0 to S0	1.988e-03	6.545e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X8_P4	X33_P4
A0 to CO	-1.345e-07	-7.987e-07
A0 to S0	-1.123e-07	-3.143e-07
B0 to CO	3.952e-06	2.895e-05
B0 to S0	1.903e-06	1.420e-05

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.272	0.3264
X6_P4	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X13_P4	1.200	0.408	0.4896
X17_P4	1.200	0.408	0.4896
X21_P4	1.200	0.544	0.6528
X25_P4	1.200	0.544	0.6528
X29_P4	1.200	0.680	0.8160
X33_P4	1.200	0.680	0.8160
X50_P4	1.200	0.952	1.1424
X58_P4	1.200	1.088	1.3056
X67_P4	1.200	1.224	1.4688
X75_P4	1.200	1.360	1.6320
X84_P4	1.200	1.496	1.7952
X100_P4	1.200	1.768	2.1216
X134_P4	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0005	0.0006	0.0008	0.0011
	X17_P4	X21_P4	X25_P4	X29_P4
A	0.0014	0.0019	0.0021	0.0025
	X33_P4	X50_P4	X58_P4	X67_P4
A	0.0028	0.0043	0.0050	0.0057
	X75_P4	X84_P4	X100_P4	X134_P4

A	0.0064	0.0072	0.0088	0.0124

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0104	0.0097	4.7353	3.6364
A to Z ↑	0.0174	0.0160	8.3447	6.2241
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0086	0.0075	2.4542	1.6003
A to Z ↑	0.0145	0.0132	4.2576	2.8238
	X17_P4	**X21_P4**	**X17_P4**	**X21_P4**
A to Z ↓	0.0073	0.0079	1.2199	0.9861
A to Z ↑	0.0126	0.0134	2.0932	1.6908
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0078	0.0073	0.8379	0.7146
A to Z ↑	0.0129	0.0124	1.4070	1.2059
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0072	0.0074	0.6315	0.4277
A to Z ↑	0.0121	0.0120	1.0547	0.7062
	X58_P4	**X67_P4**	**X58_P4**	**X67_P4**
A to Z ↓	0.0078	0.0076	0.3707	0.3258
A to Z ↑	0.0125	0.0121	0.6083	0.5324
	X75_P4	**X84_P4**	**X75_P4**	**X84_P4**
A to Z ↓	0.0081	0.0080	0.2937	0.2657
A to Z ↑	0.0126	0.0125	0.4759	0.4306
	X100_P4	**X134_P4**	**X100_P4**	**X134_P4**
A to Z ↓	0.0086	0.0093	0.2254	0.1750
A to Z ↑	0.0130	0.0136	0.3626	0.2777

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	9.971e-07	5.836e-10
X6_P4	1.256e-06	5.836e-10
X8_P4	1.814e-06	5.836e-10
X13_P4	2.771e-06	7.027e-10
X17_P4	3.517e-06	7.027e-10
X21_P4	4.337e-06	8.218e-10
X25_P4	4.924e-06	8.218e-10
X29_P4	5.835e-06	9.409e-10
X33_P4	6.282e-06	9.409e-10
X50_P4	8.993e-06	1.179e-09
X58_P4	1.035e-05	1.298e-09
X67_P4	1.171e-05	1.417e-09
X75_P4	1.307e-05	1.536e-09
X84_P4	1.443e-05	1.655e-09
X100_P4	1.715e-05	1.894e-09
X134_P4	2.258e-05	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4

A to Z	3.446e-04	4.081e-04	5.002e-04	6.552e-04
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	8.154e-04	1.158e-03	1.309e-03	1.407e-03
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	1.527e-03	2.259e-03	2.841e-03	2.980e-03
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	3.562e-03	3.743e-03	4.517e-03	6.098e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

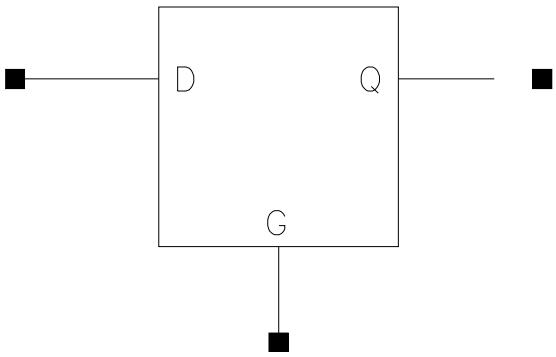
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	-2.410e-08	-1.330e-08	6.897e-07	9.567e-07
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	1.191e-06	1.611e-07	2.470e-07	2.721e-07
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	2.956e-07	1.730e-07	5.090e-07	3.510e-07
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	3.930e-07	5.091e-06	3.660e-06	3.975e-06

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X23_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P4	X23_P4
D	0.0005	0.0012
G	0.0011	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X23_P4	X8_P4	X23_P4
D to Q ↓	0.0716	0.0552	2.6221	1.2478
D to Q ↑	0.0434	0.0427	4.1771	1.1032
G to Q ↓	0.0751	0.0561	2.6184	1.2465
G to Q ↑	0.0415	0.0376	4.1763	1.1050

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P4	X23_P4
D ↓	hold_falling to G	-0.0267	-0.0113
D ↑	hold_falling to G	-0.0073	-0.0073
D ↓	setup_falling to G	0.0709	0.0459
D ↑	setup_falling to G	0.0474	0.0497
G ↑	min_pulse_width to G	0.0637	0.0524

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	4.797e-06	1.417e-09
X23_P4	9.098e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X23_P4
D (output stable)	1.573e-05	6.694e-05
G (output stable)	7.491e-04	1.459e-03
D to Q	3.438e-03	6.557e-03
G to Q	3.185e-03	5.778e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

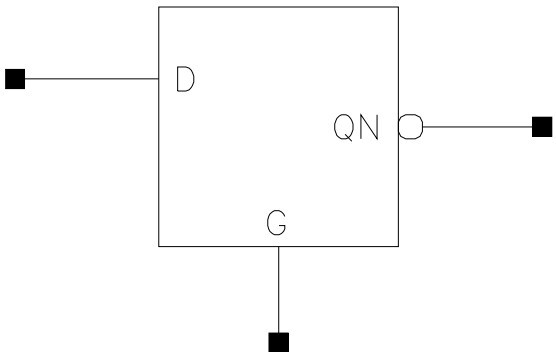
Pin Cycle (vdds)	X8_P4	X23_P4
D (output stable)	-1.563e-07	-1.120e-06
G (output stable)	9.649e-06	2.586e-05
D to Q	-5.447e-07	-1.593e-07
G to Q	3.407e-05	1.918e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P4
D	0.0005
G	0.0012

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P4	X17_P4
D to QN ↓	0.0576	1.2156
D to QN ↑	0.0788	2.0510
G to QN ↓	0.0552	1.2153
G to QN ↑	0.0790	2.0507

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P4
D ↓	hold_falling to G	-0.0315
D ↑	hold_falling to G	-0.0103
D ↓	setup_falling to G	0.0556
D ↑	setup_falling to G	0.0401
G ↑	min_pulse_width to G	0.0493

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P4	7.160e-06	1.536e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X17_P4
D (output stable)	1.603e-05
G (output stable)	8.248e-04
D to QN	4.339e-03
G to QN	3.969e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

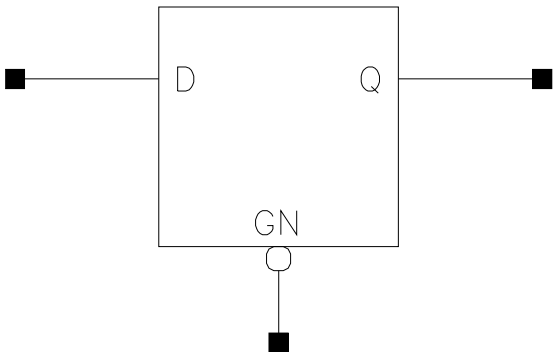
Pin Cycle (vdds)	X17_P4
D (output stable)	-1.263e-07
G (output stable)	9.508e-06
D to QN	-4.226e-07
G to QN	6.379e-05

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
D	0.0005	0.0007	0.0016
GN	0.0010	0.0013	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D to Q ↓	0.0724	0.0616	2.6324	1.2867
D to Q ↑	0.0443	0.0404	4.1819	2.1389
GN to Q ↓	0.0640	0.0534	2.6334	1.2875
GN to Q ↑	0.0662	0.0623	4.1757	2.1340

	X33_P4		X33_P4	
D to Q ↓	0.0592		0.6564	
D to Q ↑	0.0345		1.0704	
GN to Q ↓	0.0503		0.6573	
GN to Q ↑	0.0479		1.0694	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P4	X17_P4	X33_P4
D ↓	hold_rising to GN	-0.0287	-0.0185	-0.0189
D ↑	hold_rising to GN	-0.0042	-0.0019	0.0033
D ↓	setup_rising to GN	0.0784	0.0686	0.0634
D ↑	setup_rising to GN	0.0387	0.0365	0.0316
GN ↓	min_pulse_width to GN	0.0827	0.0722	0.0675

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	4.416e-06	1.417e-09
X17_P4	6.808e-06	1.655e-09
X33_P4	1.110e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
D (output stable)	1.592e-05	2.669e-05	7.366e-05
GN (output stable)	7.484e-04	1.032e-03	1.237e-03
D to Q	3.450e-03	4.795e-03	7.786e-03
GN to Q	4.933e-03	6.668e-03	9.733e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

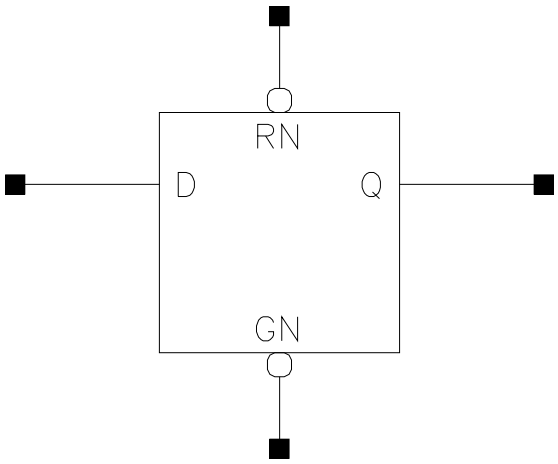
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
D (output stable)	-1.604e-07	-1.409e-07	-9.197e-07
GN (output stable)	9.545e-06	1.338e-05	2.531e-05
D to Q	-4.908e-07	-6.364e-07	-7.126e-07
GN to Q	-3.769e-05	-2.120e-05	-2.812e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.496	1.7952
X33_P4	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X33_P4
D	0.0005	0.0012
GN	0.0012	0.0022
RN	0.0005	0.0006

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
D to Q ↓	0.0675	0.0596	2.5484	0.6623
D to Q ↑	0.0571	0.0704	4.2571	1.1082

GN to Q ↓	0.0601	0.0545	2.5478	0.6625
GN to Q ↑	0.0759	0.0764	4.2524	1.1080
RN to Q ↓	0.0498	0.0902	2.4454	0.7270
RN to Q ↑	0.0611	0.0764	4.2593	1.1087

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P4	X33_P4
D ↓	hold_rising to GN	-0.0238	-0.0164
D ↑	hold_rising to GN	-0.0139	-0.0312
D ↓	setup_rising to GN	0.0682	0.0638
D ↑	setup_rising to GN	0.0536	0.0780
GN ↓	min_pulse_width to GN	0.0732	0.0761
RN ↓	min_pulse_width to RN	0.0583	0.1067
RN ↑	recovery_rising to GN	0.0585	0.0850
RN ↑	removal_rising to GN	-0.0388	-0.0557

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	4.026e-06	1.655e-09
X33_P4	9.029e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X33_P4
D (output stable)	6.789e-05	1.185e-04
GN (output stable)	8.680e-04	1.295e-03
RN (output stable)	3.460e-05	6.125e-05
D to Q	3.397e-03	8.469e-03
GN to Q	4.997e-03	1.087e-02
RN to Q	2.684e-03	6.545e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

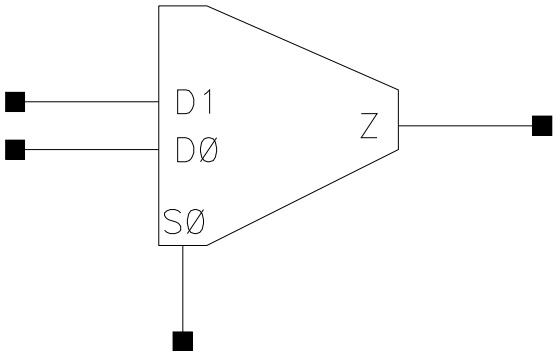
Pin Cycle (vdds)	X8_P4	X33_P4
D (output stable)	-5.770e-07	-8.043e-07
GN (output stable)	4.721e-06	9.515e-06
RN (output stable)	1.077e-07	1.781e-07
D to Q	-5.635e-07	-8.329e-07
GN to Q	-3.741e-05	3.099e-05
RN to Q	2.968e-06	-2.014e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
D0	0.0007	0.0010	0.0013	0.0018
D1	0.0007	0.0010	0.0013	0.0017
S0	0.0012	0.0014	0.0015	0.0023

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D0 to Z ↓	0.0535	0.0470	2.5347	1.2443
D0 to Z ↑	0.0410	0.0367	4.2681	2.0859
D1 to Z ↓	0.0510	0.0466	2.5273	1.2428
D1 to Z ↑	0.0375	0.0344	4.2583	2.0828
S0 to Z ↓	0.0457	0.0434	2.5246	1.2412
S0 to Z ↑	0.0426	0.0417	4.2635	2.0842

	X25_P4	X33_P4	X25_P4	X33_P4
D0 to Z ↓	0.0502	0.0451	0.8596	0.6442
D0 to Z ↑	0.0402	0.0364	1.4042	1.0500
D1 to Z ↓	0.0537	0.0470	0.8629	0.6442
D1 to Z ↑	0.0381	0.0347	1.4002	1.0478
S0 to Z ↓	0.0498	0.0452	0.8587	0.6429
S0 to Z ↑	0.0468	0.0423	1.4016	1.0494

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	5.510e-06	1.417e-09
X17_P4	9.206e-06	1.536e-09
X25_P4	1.278e-05	2.370e-09
X33_P4	1.738e-05	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	6.868e-04	9.861e-04	1.054e-03	1.408e-03
D1 (output stable)	5.481e-04	9.008e-04	1.194e-03	1.485e-03
S0 (output stable)	9.034e-04	1.019e-03	1.316e-03	1.606e-03
D0 to Z	2.391e-03	3.818e-03	5.897e-03	7.364e-03
D1 to Z	2.185e-03	3.690e-03	5.947e-03	7.272e-03
S0 to Z	2.741e-03	4.075e-03	6.616e-03	8.059e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

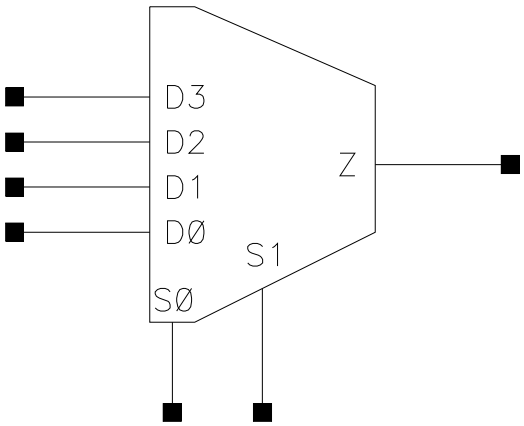
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	-9.935e-08	-3.095e-07	2.940e-07	2.102e-07
D1 (output stable)	-3.375e-07	3.449e-07	-1.713e-07	4.960e-07
S0 (output stable)	-1.220e-08	5.380e-08	-7.640e-08	-1.201e-07
D0 to Z	-1.397e-07	-3.092e-07	-3.594e-07	-6.320e-07
D1 to Z	-1.629e-07	-2.291e-07	-2.394e-07	-6.295e-07
S0 to Z	-2.005e-07	-9.165e-08	-3.252e-07	-1.856e-07

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.312	2.7744
X31_P4	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P4	X31_P4
D0	0.0005	0.0013
D1	0.0005	0.0013
D2	0.0005	0.0013
D3	0.0005	0.0013
S0	0.0018	0.0035
S1	0.0011	0.0022

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X31_P4	X8_P4	X31_P4

D0 to Z ↓	0.0976	0.0977	2.6959	0.7479
D0 to Z ↑	0.0588	0.0587	4.3068	1.1565
D1 to Z ↓	0.0968	0.0980	2.6938	0.7479
D1 to Z ↑	0.0592	0.0585	4.3118	1.1569
D2 to Z ↓	0.1052	0.0912	2.7165	0.7396
D2 to Z ↑	0.0620	0.0545	4.3271	1.1494
D3 to Z ↓	0.1049	0.0906	2.7155	0.7385
D3 to Z ↑	0.0613	0.0556	4.3240	1.1528
S0 to Z ↓	0.1070	0.1043	2.7006	0.7427
S0 to Z ↑	0.0740	0.0741	4.3210	1.1555
S1 to Z ↓	0.0768	0.0715	2.7041	0.7436
S1 to Z ↑	0.0572	0.0566	4.3157	1.1543

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	5.231e-06	2.370e-09
X31_P4	1.461e-05	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X31_P4
D0 (output stable)	1.361e-05	7.475e-05
D1 (output stable)	1.748e-05	1.004e-04
D2 (output stable)	1.793e-05	7.130e-05
D3 (output stable)	2.270e-05	1.003e-04
S0 (output stable)	1.332e-03	2.995e-03
S1 (output stable)	1.000e-03	2.134e-03
D0 to Z	2.573e-03	8.603e-03
D1 to Z	2.566e-03	8.631e-03
D2 to Z	2.773e-03	8.039e-03
D3 to Z	2.765e-03	8.008e-03
S0 to Z	4.042e-03	1.163e-02
S1 to Z	2.958e-03	8.165e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

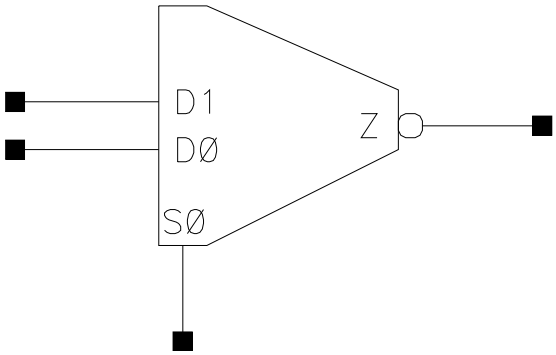
Pin Cycle (vdds)	X8_P4	X31_P4
D0 (output stable)	3.038e-06	1.092e-05
D1 (output stable)	2.873e-06	9.708e-06
D2 (output stable)	2.552e-06	1.294e-05
D3 (output stable)	1.855e-06	1.206e-05
S0 (output stable)	-4.066e-06	-1.031e-05
S1 (output stable)	4.791e-05	1.743e-04
D0 to Z	1.017e-06	1.332e-06
D1 to Z	6.252e-07	5.300e-06
D2 to Z	1.728e-06	1.819e-06
D3 to Z	1.873e-06	4.522e-06
S0 to Z	-2.020e-07	-4.142e-06
S1 to Z	4.387e-05	1.669e-04

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.816	0.9792
X5_P4	1.200	0.952	1.1424
X10_P4	1.200	1.768	2.1216
X16_P4	1.200	2.448	2.9376
X21_P4	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P4	X5_P4	X10_P4	X16_P4
D0	0.0005	0.0007	0.0015	0.0023
D1	0.0005	0.0008	0.0014	0.0022
S0	0.0011	0.0019	0.0025	0.0036
	X21_P4			
D0	0.0030			
D1	0.0030			
S0	0.0042			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X5_P4	X3_P4	X5_P4
D0 to Z ↓	0.0181	0.0176	8.8815	5.2300

D0 to Z ↑	0.0326	0.0291	20.0305	10.0421
D1 to Z ↓	0.0178	0.0168	8.7833	5.0257
D1 to Z ↑	0.0339	0.0305	20.0484	10.3158
S0 to Z ↓	0.0276	0.0224	8.8124	5.1265
S0 to Z ↑	0.0308	0.0248	20.0007	10.1685
	X10_P4	**X16_P4**	**X10_P4**	**X16_P4**
D0 to Z ↓	0.0196	0.0182	2.4405	1.5976
D0 to Z ↑	0.0317	0.0301	4.6439	3.0541
D1 to Z ↓	0.0177	0.0174	2.3777	1.5757
D1 to Z ↑	0.0319	0.0309	4.6987	3.0771
S0 to Z ↓	0.0271	0.0235	2.4043	1.5841
S0 to Z ↑	0.0292	0.0253	4.6652	3.0633
	X21_P4		**X21_P4**	
D0 to Z ↓	0.0181		1.2162	
D0 to Z ↑	0.0295		2.3084	
D1 to Z ↓	0.0174		1.1946	
D1 to Z ↑	0.0310		2.2983	
S0 to Z ↓	0.0245		1.2026	
S0 to Z ↑	0.0259		2.3018	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P4	2.055e-06	1.060e-09
X5_P4	4.060e-06	1.179e-09
X10_P4	6.939e-06	1.894e-09
X16_P4	1.054e-05	2.489e-09
X21_P4	1.285e-05	3.085e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	1.606e-05	3.610e-05	1.073e-04	1.676e-04
D1 (output stable)	1.558e-05	3.871e-05	8.967e-05	1.544e-04
S0 (output stable)	7.447e-04	1.055e-03	1.891e-03	2.911e-03
D0 to Z	7.341e-04	1.230e-03	3.068e-03	4.284e-03
D1 to Z	7.364e-04	1.223e-03	2.908e-03	4.236e-03
S0 to Z	1.306e-03	1.842e-03	3.890e-03	5.395e-03
	X21_P4			
D0 (output stable)	2.203e-04			
D1 (output stable)	2.087e-04			
S0 (output stable)	3.229e-03			
D0 to Z	5.480e-03			
D1 to Z	5.591e-03			
S0 to Z	6.604e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	-1.458e-07	-1.323e-07	-1.143e-06	-2.664e-06
D1 (output stable)	-1.470e-07	-1.078e-06	-9.549e-07	-2.155e-06
S0 (output stable)	9.900e-06	3.515e-05	4.336e-05	8.063e-05
D0 to Z	2.513e-07	5.469e-07	1.383e-06	1.945e-06

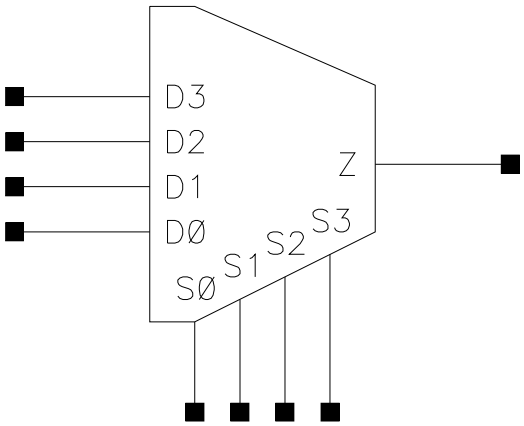
D1 to Z	4.035e-08	5.085e-07	1.775e-06	5.630e-07
S0 to Z	8.341e-06	2.964e-05	3.303e-05	6.644e-05
	X21_P4			
D0 (output stable)	-3.405e-06			
D1 (output stable)	-3.978e-06			
S0 (output stable)	1.135e-04			
D0 to Z	5.401e-06			
D1 to Z	2.650e-06			
S0 to Z	8.798e-05			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	1.768	2.1216
X27_P4	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P4	X27_P4
D0	0.0006	0.0018
D1	0.0006	0.0018
D2	0.0006	0.0018
D3	0.0006	0.0018
S0	0.0006	0.0017
S1	0.0007	0.0017
S2	0.0006	0.0016
S3	0.0006	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	X27_P4	X7_P4	X27_P4
D0 to Z ↓	0.0728	0.0596	4.4276	1.2073
D0 to Z ↑	0.0491	0.0400	4.1965	1.0439
D1 to Z ↓	0.0650	0.0534	4.4244	1.2066
D1 to Z ↑	0.0447	0.0357	4.1771	1.0394
D2 to Z ↓	0.0733	0.0566	4.4403	1.2095
D2 to Z ↑	0.0484	0.0375	4.2109	1.0481
D3 to Z ↓	0.0657	0.0503	4.4352	1.2069
D3 to Z ↑	0.0440	0.0332	4.1980	1.0430
S0 to Z ↓	0.0707	0.0566	4.4256	1.2062
S0 to Z ↑	0.0512	0.0412	4.1947	1.0445
S1 to Z ↓	0.0634	0.0502	4.4226	1.2055
S1 to Z ↑	0.0467	0.0364	4.1809	1.0397
S2 to Z ↓	0.0712	0.0534	4.4297	1.2069
S2 to Z ↑	0.0505	0.0385	4.2112	1.0485
S3 to Z ↓	0.0640	0.0472	4.4279	1.2054
S3 to Z ↑	0.0460	0.0340	4.1991	1.0435

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X7_P4	4.604e-06	1.894e-09
X27_P4	1.617e-05	3.561e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X7_P4	X27_P4
D0 (output stable)	4.040e-04	1.256e-03
D1 (output stable)	3.269e-04	9.847e-04
D2 (output stable)	3.779e-04	1.198e-03
D3 (output stable)	3.010e-04	9.205e-04
S0 (output stable)	3.955e-04	1.209e-03
S1 (output stable)	3.149e-04	9.460e-04
S2 (output stable)	3.679e-04	1.150e-03
S3 (output stable)	2.882e-04	8.815e-04
D0 to Z	3.094e-03	9.400e-03
D1 to Z	2.706e-03	8.078e-03
D2 to Z	3.009e-03	8.196e-03
D3 to Z	2.627e-03	6.858e-03
S0 to Z	3.022e-03	8.926e-03
S1 to Z	2.633e-03	7.632e-03
S2 to Z	2.936e-03	7.706e-03
S3 to Z	2.552e-03	6.407e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

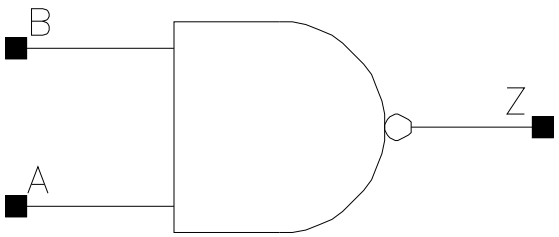
Pin Cycle (vdds)	X7_P4	X27_P4
D0 (output stable)	-5.202e-07	-3.334e-07
D1 (output stable)	8.814e-06	2.462e-05
D2 (output stable)	-5.213e-07	-3.159e-07
D3 (output stable)	8.926e-06	2.443e-05
S0 (output stable)	-7.400e-07	-2.870e-07
S1 (output stable)	9.199e-06	2.464e-05
S2 (output stable)	-4.784e-07	-3.217e-07
S3 (output stable)	8.930e-06	2.438e-05
D0 to Z	-2.018e-07	1.182e-06
D1 to Z	-2.267e-07	-7.801e-07
D2 to Z	7.978e-08	2.167e-06
D3 to Z	-6.412e-08	-5.103e-07
S0 to Z	-1.950e-07	1.399e-06
S1 to Z	-1.986e-07	-7.145e-07
S2 to Z	1.730e-07	2.005e-06
S3 to Z	-1.418e-08	-2.991e-07

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P4	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P4	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P4	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P4	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P4	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P4	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P4	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P4	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P4	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P4	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P4	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P4	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P4	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P4	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P4	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P4	C12T28SOI_LR_-NAND2X5_P4	C12T28SOI_LR_-NAND2X7_P4	C12T28SOI_LR_-NAND2X10_P4
A	0.0005	0.0006	0.0007	0.0012
B	0.0005	0.0006	0.0007	0.0011
	C12T28SOI_LR_-NAND2X13_P4	C12T28SOI_LR_-NAND2X17_P4	C12T28SOI_LR_-NAND2X20_P4	C12T28SOI_LR_-NAND2X24_P4
A	0.0015	0.0019	0.0022	0.0026
B	0.0014	0.0018	0.0020	0.0024
	C12T28SOI_LR_-NAND2X27_P4	C12T28SOI_LR_-NAND2X42_P4	C12T28SOI_LR_-NAND2X47_P4	C12T28SOI_LR_-NAND2X50_P4
A	0.0029	0.0009	0.0009	0.0009
B	0.0027	0.0010	0.0010	0.0010
	C12T28SOI_LR_-NAND2X58_P4	C12T28SOI_LR_-NAND2X67_P4	C12T28SOI_-LRBR0D8_-NAND2X7_P4	C12T28SOI_-LRBR0D8_-NAND2X14_P4
A	0.0009	0.0009	0.0007	0.0014
B	0.0010	0.0010	0.0007	0.0013
	C12T28SOI_LRS_-NAND2X40_P4	C12T28SOI_LRS_-NAND2X54_P4		
A	0.0043	0.0058		
B	0.0040	0.0054		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P4	**C12T28SOI_LR_-NAND2X5_P4**	**C12T28SOI_LR_-NAND2X3_P4**	**C12T28SOI_LR_-NAND2X5_P4**
A to Z ↓	0.0140	0.0125	8.5949	5.4046
A to Z ↑	0.0201	0.0182	8.3473	5.2549
B to Z ↓	0.0146	0.0125	8.6497	5.4520
B to Z ↑	0.0187	0.0164	8.3893	5.2825
	C12T28SOI_LR_-NAND2X7_P4	**C12T28SOI_LR_-NAND2X10_P4**	**C12T28SOI_LR_-NAND2X7_P4**	**C12T28SOI_LR_-NAND2X10_P4**
A to Z ↓	0.0123	0.0142	4.5141	3.0236
A to Z ↑	0.0176	0.0190	4.2294	2.7917
B to Z ↓	0.0123	0.0124	4.5513	3.0472
B to Z ↑	0.0157	0.0157	4.2648	2.8105
	C12T28SOI_LR_-NAND2X13_P4	**C12T28SOI_LR_-NAND2X17_P4**	**C12T28SOI_LR_-NAND2X13_P4**	**C12T28SOI_LR_-NAND2X17_P4**
A to Z ↓	0.0136	0.0136	2.3054	1.8426

A to Z ↑	0.0179	0.0181	2.0777	1.6794
B to Z ↓	0.0118	0.0123	2.3218	1.8533
B to Z ↑	0.0148	0.0154	2.0921	1.6906
	C12T28SOI_LR_-NAND2X20_P4	**C12T28SOI_LR_-NAND2X24_P4**	**C12T28SOI_LR_-NAND2X20_P4**	**C12T28SOI_LR_-NAND2X24_P4**
A to Z ↓	0.0133	0.0137	1.5743	1.3446
A to Z ↑	0.0176	0.0179	1.3978	1.1963
B to Z ↓	0.0121	0.0119	1.5858	1.3563
B to Z ↑	0.0150	0.0148	1.4074	1.2039
	C12T28SOI_LR_-NAND2X27_P4	**C12T28SOI_LR_-NAND2X42_P4**	**C12T28SOI_LR_-NAND2X27_P4**	**C12T28SOI_LR_-NAND2X42_P4**
A to Z ↓	0.0134	0.0471	1.1970	0.5096
A to Z ↑	0.0174	0.0485	1.0483	0.8310
B to Z ↓	0.0116	0.0479	1.2044	0.5095
B to Z ↑	0.0142	0.0469	1.0548	0.8320
	C12T28SOI_LR_-NAND2X47_P4	**C12T28SOI_LR_-NAND2X50_P4**	**C12T28SOI_LR_-NAND2X47_P4**	**C12T28SOI_LR_-NAND2X50_P4**
A to Z ↓	0.0482	0.0486	0.4538	0.4260
A to Z ↑	0.0491	0.0493	0.7239	0.6936
B to Z ↓	0.0491	0.0496	0.4537	0.4260
B to Z ↑	0.0475	0.0478	0.7226	0.6944
	C12T28SOI_LR_-NAND2X58_P4	**C12T28SOI_LR_-NAND2X67_P4**	**C12T28SOI_LR_-NAND2X58_P4**	**C12T28SOI_LR_-NAND2X67_P4**
A to Z ↓	0.0509	0.0525	0.3690	0.3253
A to Z ↑	0.0511	0.0519	0.5965	0.5240
B to Z ↓	0.0519	0.0533	0.3688	0.3251
B to Z ↑	0.0495	0.0503	0.5969	0.5248
	C12T28SOI_-LRBR0D8_-NAND2X7_P4	**C12T28SOI_-LRBR0D8_-NAND2X14_P4**	**C12T28SOI_-LRBR0D8_-NAND2X7_P4**	**C12T28SOI_-LRBR0D8_-NAND2X14_P4**
A to Z ↓	0.0105	0.0117	3.3659	1.7613
A to Z ↑	0.0209	0.0213	5.6798	2.7725
B to Z ↓	0.0099	0.0091	3.4100	1.7901
B to Z ↑	0.0180	0.0163	5.8480	2.8214
	C12T28SOI_LRS_-NAND2X40_P4	**C12T28SOI_LRS_-NAND2X54_P4**	**C12T28SOI_LRS_-NAND2X40_P4**	**C12T28SOI_LRS_-NAND2X54_P4**
A to Z ↓	0.0133	0.0134	0.8089	0.6124
A to Z ↑	0.0173	0.0174	0.7022	0.5292
B to Z ↓	0.0117	0.0119	0.8156	0.6181
B to Z ↑	0.0142	0.0144	0.7071	0.5330

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P4	9.904e-07	7.027e-10
C12T28SOI_LR_NAND2X5_P4	1.557e-06	7.027e-10
C12T28SOI_LR_NAND2X7_P4	1.839e-06	7.027e-10
C12T28SOI_LR_NAND2X10_P4	2.638e-06	9.409e-10
C12T28SOI_LR_NAND2X13_P4	3.378e-06	9.409e-10
C12T28SOI_LR_NAND2X17_P4	4.220e-06	1.179e-09
C12T28SOI_LR_NAND2X20_P4	4.809e-06	1.179e-09
C12T28SOI_LR_NAND2X24_P4	5.794e-06	1.417e-09
C12T28SOI_LR_NAND2X27_P4	6.245e-06	1.417e-09

C12T28SOI_LR_NAND2X42_P4	1.282e-05	1.536e-09
C12T28SOI_LR_NAND2X47_P4	1.444e-05	1.655e-09
C12T28SOI_LR_NAND2X50_P4	1.446e-05	1.655e-09
C12T28SOI_LR_NAND2X58_P4	1.609e-05	1.775e-09
C12T28SOI_LR_NAND2X67_P4	1.773e-05	1.894e-09
C12T28SOI_LRBR0D8_NAND2X7_P4	2.120e-06	1.296e-09
C12T28SOI_LRBR0D8_NAND2X14_-P4	3.852e-06	1.549e-09
C12T28SOI_LRS_NAND2X40_P4	9.120e-06	1.894e-09
C12T28SOI_LRS_NAND2X54_P4	1.200e-05	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P4	C12T28SOI_LR_-NAND2X5_P4	C12T28SOI_LR_-NAND2X7_P4	C12T28SOI_LR_-NAND2X10_P4
A (output stable)	1.163e-05	1.854e-05	2.240e-05	7.182e-05
B (output stable)	1.613e-05	2.547e-05	3.162e-05	2.372e-04
A to Z	4.985e-04	6.544e-04	7.746e-04	1.403e-03
B to Z	4.172e-04	5.224e-04	6.095e-04	9.388e-04
	C12T28SOI_LR_-NAND2X13_P4	C12T28SOI_LR_-NAND2X17_P4	C12T28SOI_LR_-NAND2X20_P4	C12T28SOI_LR_-NAND2X24_P4
A (output stable)	8.548e-05	1.036e-04	1.157e-04	1.560e-04
B (output stable)	2.691e-04	2.647e-04	3.029e-04	4.505e-04
A to Z	1.697e-03	2.135e-03	2.413e-03	2.972e-03
B to Z	1.135e-03	1.507e-03	1.715e-03	1.997e-03
	C12T28SOI_LR_-NAND2X27_P4	C12T28SOI_LR_-NAND2X42_P4	C12T28SOI_LR_-NAND2X47_P4	C12T28SOI_LR_-NAND2X50_P4
A (output stable)	1.701e-04	2.485e-05	2.495e-05	2.490e-05
B (output stable)	4.843e-04	3.843e-05	3.854e-05	3.855e-05
A to Z	3.193e-03	8.249e-03	8.878e-03	9.083e-03
B to Z	2.113e-03	8.076e-03	8.710e-03	8.918e-03
	C12T28SOI_LR_-NAND2X58_P4	C12T28SOI_LR_-NAND2X67_P4	C12T28SOI_-LRBR0D8_-NAND2X7_P4	C12T28SOI_-LRBR0D8_-NAND2X14_P4
A (output stable)	2.500e-05	2.510e-05	2.950e-05	1.072e-04
B (output stable)	3.868e-05	3.871e-05	4.246e-05	3.441e-04
A to Z	1.031e-02	1.119e-02	8.045e-04	1.764e-03
B to Z	1.014e-02	1.102e-02	5.761e-04	1.013e-03
	C12T28SOI_LRS_-NAND2X40_P4	C12T28SOI_LRS_-NAND2X54_P4		
A (output stable)	2.504e-04	3.228e-04		
B (output stable)	6.657e-04	8.624e-04		
A to Z	4.722e-03	6.271e-03		
B to Z	3.147e-03	4.240e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P4	C12T28SOI_LR_-NAND2X5_P4	C12T28SOI_LR_-NAND2X7_P4	C12T28SOI_LR_-NAND2X10_P4
A (output stable)	4.130e-08	3.465e-08	3.593e-08	7.100e-09
B (output stable)	3.410e-08	2.063e-08	1.093e-08	-1.220e-06
A to Z	1.440e-08	-1.220e-08	-2.036e-07	-6.320e-08
B to Z	3.630e-08	-1.310e-07	4.990e-08	1.700e-09

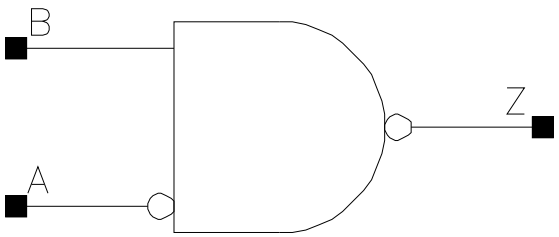
	C12T28SOI_LR_-NAND2X13_P4	C12T28SOI_LR_-NAND2X17_P4	C12T28SOI_LR_-NAND2X20_P4	C12T28SOI_LR_-NAND2X24_P4
A (output stable)	-1.390e-08	-4.350e-08	-7.030e-08	-8.210e-08
B (output stable)	-1.176e-06	-9.583e-07	-9.560e-08	-2.172e-06
A to Z	4.275e-07	-8.760e-07	5.610e-07	-7.850e-07
B to Z	-4.488e-07	-1.000e-09	-7.000e-07	-9.830e-07
	C12T28SOI_LR_-NAND2X27_P4	C12T28SOI_LR_-NAND2X42_P4	C12T28SOI_LR_-NAND2X47_P4	C12T28SOI_LR_-NAND2X50_P4
A (output stable)	-1.097e-07	3.070e-08	3.123e-08	3.138e-08
B (output stable)	-2.035e-06	1.478e-08	1.534e-08	1.525e-08
A to Z	-2.078e-06	-3.360e-07	-3.420e-07	-7.520e-07
B to Z	2.370e-07	-3.070e-07	-3.980e-07	-5.200e-07
	C12T28SOI_LR_-NAND2X58_P4	C12T28SOI_LR_-NAND2X67_P4	C12T28SOI_-LRBR0D8_-NAND2X7_P4	C12T28SOI_-LRBR0D8_-NAND2X14_P4
A (output stable)	3.169e-08	3.205e-08	5.114e-08	1.170e-08
B (output stable)	1.552e-08	1.605e-08	2.497e-08	-4.509e-06
A to Z	-7.590e-07	-6.390e-07	1.635e-07	-2.386e-07
B to Z	-2.390e-07	-5.880e-07	1.193e-07	8.127e-07
	C12T28SOI_LRS_-NAND2X40_P4	C12T28SOI_LRS_-NAND2X54_P4		
A (output stable)	-2.389e-07	-2.658e-07		
B (output stable)	-2.600e-06	-3.733e-06		
A to Z	-1.383e-06	-1.469e-06		
B to Z	7.600e-08	1.190e-07		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X7_P4	1.200	0.544	0.6528
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X40_P4	1.200	2.312	2.7744
X54_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P4	X7_P4	X13_P4	X27_P4
A	0.0007	0.0008	0.0010	0.0018
B	0.0005	0.0007	0.0013	0.0027
	X40_P4	X54_P4		
A	0.0027	0.0036		
B	0.0040	0.0053		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0364	0.0380	8.6118	4.5278
A to Z ↑	0.0276	0.0283	8.1795	4.2008
B to Z ↓	0.0150	0.0123	8.7496	4.5983
B to Z ↑	0.0188	0.0157	8.3901	4.2975
	X13_P4	**X27_P4**	**X13_P4**	**X27_P4**

A to Z ↓	0.0347	0.0338	2.3896	1.1940
A to Z ↑	0.0262	0.0256	2.1507	1.0423
B to Z ↓	0.0115	0.0114	2.4278	1.2119
B to Z ↑	0.0146	0.0142	2.1419	1.0573
	X40_P4	**X54_P4**	**X40_P4**	**X54_P4**
A to Z ↓	0.0343	0.0340	0.7995	0.6063
A to Z ↑	0.0261	0.0258	0.6944	0.5239
B to Z ↓	0.0114	0.0115	0.8149	0.6171
B to Z ↑	0.0141	0.0141	0.7094	0.5353

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P4	1.822e-06	8.218e-10
X7_P4	2.652e-06	8.218e-10
X13_P4	5.305e-06	1.179e-09
X27_P4	9.619e-06	1.775e-09
X40_P4	1.386e-05	2.370e-09
X54_P4	1.810e-05	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	7.905e-04	9.946e-04	1.586e-03	3.080e-03
B (output stable)	1.704e-05	3.275e-05	2.470e-04	4.364e-04
A to Z	1.359e-03	1.862e-03	3.391e-03	6.626e-03
B to Z	4.232e-04	6.047e-04	1.103e-03	2.141e-03
	X40_P4	X54_P4		
A (output stable)	4.735e-03	6.105e-03		
B (output stable)	6.393e-04	8.478e-04		
A to Z	9.953e-03	1.300e-02		
B to Z	3.120e-03	4.139e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

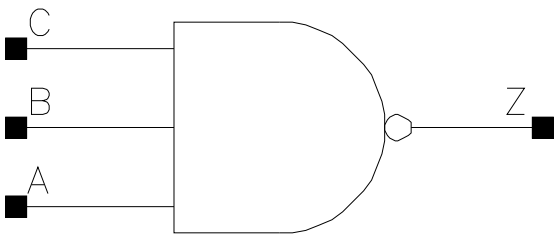
Pin Cycle (vdds)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	-7.770e-08	9.600e-09	-1.320e-07	-3.332e-07
B (output stable)	3.270e-08	5.980e-09	-3.430e-08	-1.305e-06
A to Z	7.210e-08	-1.720e-08	-1.713e-07	-3.920e-07
B to Z	6.780e-08	3.270e-08	8.220e-08	1.700e-08
	X40_P4	X54_P4		
A (output stable)	-6.880e-07	-8.720e-07		
B (output stable)	-2.040e-06	-3.281e-06		
A to Z	-8.060e-07	-1.010e-06		
B to Z	-9.190e-07	-1.492e-06		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P4	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P4	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P4	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P4	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P4	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P4	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P4	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P4	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P4	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P4	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P4	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P4	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P4	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P4	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P4	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A	0.0006	0.0007	0.0012	0.0015
B	0.0006	0.0008	0.0011	0.0014
C	0.0006	0.0007	0.0011	0.0014
	C12T28SOI_LR_-NAND3X15_P4	C12T28SOI_LR_-NAND3X18_P4	C12T28SOI_LR_-NAND3X21_P4	C12T28SOI_LR_-NAND3X24_P4
A	0.0019	0.0022	0.0026	0.0029
B	0.0018	0.0021	0.0025	0.0027
C	0.0017	0.0020	0.0024	0.0027
	C12T28SOI_LR_-NAND3X35_P4	C12T28SOI_LR_-NAND3X47_P4	C12T28SOI_-LRBR0P6_-NAND3X6_P4	C12T28SOI_-LRBR0P6_-NAND3X12_P4
A	0.0044	0.0057	0.0007	0.0015
B	0.0041	0.0056	0.0008	0.0014
C	0.0040	0.0053	0.0007	0.0013
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	C12T28SOI_-LRBR0P6_-NAND3X24_P4	C12T28SOI_-LRBR0P6_-NAND3X35_P4	C12T28SOI_-LRBR0P6_-NAND3X47_P4
A	0.0022	0.0029	0.0043	0.0058
B	0.0020	0.0027	0.0040	0.0054
C	0.0019	0.0026	0.0038	0.0051
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4			
A	0.0023			
B	0.0022			
C	0.0020			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4
A to Z ↓	0.0219	0.0196	9.0890	6.4044
A to Z ↑	0.0249	0.0225	6.0099	4.1090
B to Z ↓	0.0229	0.0202	9.1056	6.4152
B to Z ↑	0.0241	0.0215	6.0207	4.1180
C to Z ↓	0.0199	0.0176	9.1315	6.4364
C to Z ↑	0.0211	0.0188	6.0216	4.1397

	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A to Z ↓	0.0218	0.0203	4.3990	3.3777
A to Z ↑	0.0237	0.0222	2.8080	2.0977
B to Z ↓	0.0207	0.0193	4.4101	3.3852
B to Z ↑	0.0218	0.0203	2.8138	2.1021
C to Z ↓	0.0178	0.0167	4.4230	3.3973
C to Z ↑	0.0188	0.0175	2.8048	2.0869
	C12T28SOI_LR_-NAND3X15_P4	**C12T28SOI_LR_-NAND3X18_P4**	**C12T28SOI_LR_-NAND3X15_P4**	**C12T28SOI_LR_-NAND3X18_P4**
A to Z ↓	0.0197	0.0192	2.7496	2.3431
A to Z ↑	0.0217	0.0211	1.6793	1.3947
B to Z ↓	0.0193	0.0189	2.7566	2.3514
B to Z ↑	0.0200	0.0194	1.6835	1.3982
C to Z ↓	0.0171	0.0166	2.7655	2.3593
C to Z ↑	0.0175	0.0168	1.6943	1.4069
	C12T28SOI_LR_-NAND3X21_P4	**C12T28SOI_LR_-NAND3X24_P4**	**C12T28SOI_LR_-NAND3X21_P4**	**C12T28SOI_LR_-NAND3X24_P4**
A to Z ↓	0.0202	0.0198	1.9843	1.7630
A to Z ↑	0.0219	0.0214	1.2024	1.0546
B to Z ↓	0.0194	0.0190	1.9906	1.7687
B to Z ↑	0.0201	0.0196	1.2047	1.0565
C to Z ↓	0.0169	0.0167	1.9979	1.7753
C to Z ↑	0.0174	0.0170	1.2060	1.0567
	C12T28SOI_LR_-NAND3X35_P4	**C12T28SOI_LR_-NAND3X47_P4**	**C12T28SOI_LR_-NAND3X35_P4**	**C12T28SOI_LR_-NAND3X47_P4**
A to Z ↓	0.0191	0.0195	1.2034	0.9141
A to Z ↑	0.0209	0.0211	0.7062	0.5329
B to Z ↓	0.0186	0.0189	1.2062	0.9162
B to Z ↑	0.0191	0.0193	0.7064	0.5319
C to Z ↓	0.0162	0.0166	1.2111	0.9197
C to Z ↑	0.0163	0.0165	0.7101	0.5342
	C12T28SOI_-LRBR0P6_-NAND3X6_P4	**C12T28SOI_-LRBR0P6_-NAND3X12_P4**	**C12T28SOI_-LRBR0P6_-NAND3X6_P4**	**C12T28SOI_-LRBR0P6_-NAND3X12_P4**
A to Z ↓	0.0157	0.0163	4.2983	2.2552
A to Z ↑	0.0305	0.0303	6.5773	3.3525
B to Z ↓	0.0158	0.0148	4.3177	2.2663
B to Z ↑	0.0280	0.0263	6.5943	3.3594
C to Z ↓	0.0124	0.0112	4.3463	2.2854
C to Z ↑	0.0226	0.0204	6.6233	3.3665
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	**C12T28SOI_-LRBR0P6_-NAND3X24_P4**	**C12T28SOI_-LRBR0P6_-NAND3X18_P4**	**C12T28SOI_-LRBR0P6_-NAND3X24_P4**
A to Z ↓	0.0153	0.0158	1.5627	1.1749
A to Z ↑	0.0287	0.0292	2.2304	1.6840
B to Z ↓	0.0143	0.0143	1.5735	1.1810
B to Z ↑	0.0250	0.0254	2.2369	1.6878
C to Z ↓	0.0113	0.0110	1.5834	1.1903
C to Z ↑	0.0198	0.0197	2.2503	1.6895
	C12T28SOI_-LRBR0P6_-NAND3X35_P4	**C12T28SOI_-LRBR0P6_-NAND3X47_P4**	**C12T28SOI_-LRBR0P6_-NAND3X35_P4**	**C12T28SOI_-LRBR0P6_-NAND3X47_P4**

A to Z ↓	0.0154	0.0156	0.8013	0.6095
A to Z ↑	0.0290	0.0291	1.1527	0.8718
B to Z ↓	0.0143	0.0144	0.8057	0.6135
B to Z ↑	0.0252	0.0252	1.1542	0.8717
C to Z ↓	0.0110	0.0113	0.8123	0.6183
C to Z ↑	0.0194	0.0197	1.1638	0.8745
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P4**	
A to Z ↓	0.0160		1.4805	
A to Z ↑	0.0288		2.0774	
B to Z ↓	0.0143		1.4888	
B to Z ↑	0.0251		2.0807	
C to Z ↓	0.0106		1.5013	
C to Z ↑	0.0191		2.0658	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P4	1.166e-06	9.409e-10
C12T28SOI_LR_NAND3X6_P4	1.635e-06	9.409e-10
C12T28SOI_LR_NAND3X9_P4	2.280e-06	1.298e-09
C12T28SOI_LR_NAND3X12_P4	2.901e-06	1.298e-09
C12T28SOI_LR_NAND3X15_P4	3.395e-06	1.536e-09
C12T28SOI_LR_NAND3X18_P4	3.873e-06	1.536e-09
C12T28SOI_LR_NAND3X21_P4	4.910e-06	2.013e-09
C12T28SOI_LR_NAND3X24_P4	5.291e-06	2.013e-09
C12T28SOI_LR_NAND3X35_P4	7.674e-06	2.727e-09
C12T28SOI_LR_NAND3X47_P4	1.005e-05	3.442e-09
C12T28SOI_LRBR0P6_NAND3X6_P4	2.006e-06	1.615e-09
C12T28SOI_LRBR0P6_NAND3X12_-P4	3.648e-06	2.005e-09
C12T28SOI_LRBR0P6_NAND3X18_-P4	4.860e-06	2.266e-09
C12T28SOI_LRBR0P6_NAND3X24_-P4	6.792e-06	2.786e-09
C12T28SOI_LRBR0P6_NAND3X35_-P4	9.943e-06	3.566e-09
C12T28SOI_LRBR0P6_NAND3X47_-P4	1.309e-05	4.346e-09
C12T28SOIDV_LRBR0P6_-NAND3X18_P4	5.896e-06	1.874e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A (output stable)	2.055e-05	2.848e-05	6.848e-05	8.097e-05
B (output stable)	4.873e-05	6.250e-05	1.525e-04	1.801e-04
C (output stable)	1.871e-04	2.212e-04	3.657e-04	4.215e-04
A to Z	1.152e-03	1.397e-03	2.305e-03	2.709e-03
B to Z	1.046e-03	1.235e-03	1.872e-03	2.199e-03
C to Z	8.076e-04	9.544e-04	1.396e-03	1.639e-03

	C12T28SOI_LR_-NAND3X15_P4	C12T28SOI_LR_-NAND3X18_P4	C12T28SOI_LR_-NAND3X21_P4	C12T28SOI_LR_-NAND3X24_P4
A (output stable)	9.160e-05	1.041e-04	1.420e-04	1.531e-04
B (output stable)	2.007e-04	2.308e-04	3.088e-04	3.359e-04
C (output stable)	4.551e-04	5.116e-04	6.916e-04	7.410e-04
A to Z	3.243e-03	3.662e-03	4.633e-03	5.053e-03
B to Z	2.643e-03	2.984e-03	3.759e-03	4.091e-03
C to Z	2.029e-03	2.262e-03	2.816e-03	3.063e-03
	C12T28SOI_LR_-NAND3X35_P4	C12T28SOI_LR_-NAND3X47_P4	C12T28SOI_-LRBR0P6_-NAND3X6_P4	C12T28SOI_-LRBR0P6_-NAND3X12_P4
A (output stable)	2.105e-04	2.779e-04	4.123e-05	1.162e-04
B (output stable)	4.692e-04	6.150e-04	9.172e-05	2.640e-04
C (output stable)	1.094e-03	1.378e-03	3.038e-04	6.090e-04
A to Z	7.161e-03	9.608e-03	1.497e-03	2.944e-03
B to Z	5.751e-03	7.758e-03	1.246e-03	2.198e-03
C to Z	4.167e-03	5.791e-03	8.278e-04	1.338e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	C12T28SOI_-LRBR0P6_-NAND3X24_P4	C12T28SOI_-LRBR0P6_-NAND3X35_P4	C12T28SOI_-LRBR0P6_-NAND3X47_P4
A (output stable)	1.492e-04	2.186e-04	3.017e-04	3.986e-04
B (output stable)	3.299e-04	4.856e-04	6.576e-04	8.774e-04
C (output stable)	7.056e-04	1.085e-03	1.556e-03	2.018e-03
A to Z	3.935e-03	5.470e-03	7.895e-03	1.041e-02
B to Z	2.936e-03	4.068e-03	5.846e-03	7.738e-03
C to Z	1.884e-03	2.493e-03	3.537e-03	4.719e-03
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4			
A (output stable)	1.707e-04			
B (output stable)	3.949e-04			
C (output stable)	8.721e-04			
A to Z	4.316e-03			
B to Z	3.211e-03			
C to Z	1.926e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A (output stable)	4.167e-08	3.332e-08	4.967e-08	-7.367e-09
B (output stable)	3.831e-08	2.748e-08	-3.003e-07	-2.505e-08
C (output stable)	4.377e-08	3.710e-08	-1.830e-06	-1.670e-08
A to Z	-2.670e-07	4.120e-07	-8.810e-07	-1.359e-06
B to Z	-1.650e-07	-4.570e-07	1.470e-07	-4.490e-07
C to Z	2.560e-07	3.030e-07	4.810e-07	6.260e-07
	C12T28SOI_LR_-NAND3X15_P4	C12T28SOI_LR_-NAND3X18_P4	C12T28SOI_LR_-NAND3X21_P4	C12T28SOI_LR_-NAND3X24_P4
A (output stable)	-1.140e-08	-1.750e-08	2.797e-08	-1.777e-08
B (output stable)	-3.735e-07	-3.942e-07	-1.387e-06	-7.034e-07
C (output stable)	-1.538e-06	-1.452e-06	-3.853e-06	-2.866e-06
A to Z	5.630e-07	5.220e-07	-2.274e-06	-2.410e-06
B to Z	-4.250e-07	-6.360e-07	-5.950e-07	-8.920e-07

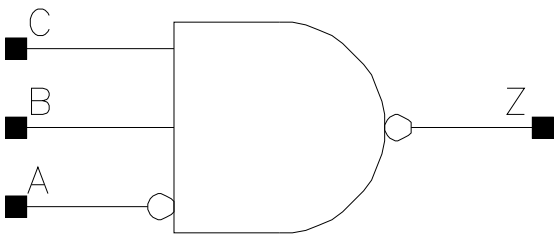
C to Z	2.880e-07	-2.730e-07	9.110e-07	-4.640e-07
	C12T28SOI_LR_-NAND3X35_P4	C12T28SOI_LR_-NAND3X47_P4	C12T28SOI_-LRBR0P6_-NAND3X6_P4	C12T28SOI_-LRBR0P6_-NAND3X12_P4
A (output stable)	-9.887e-08	-1.231e-07	1.140e-07	1.793e-07
B (output stable)	-1.165e-06	-2.306e-06	-6.223e-07	-2.064e-06
C (output stable)	-4.504e-06	-6.216e-06	-3.793e-06	-5.569e-06
A to Z	8.760e-07	1.515e-06	1.870e-07	-2.315e-06
B to Z	-1.338e-06	-1.405e-06	-4.775e-07	-1.047e-06
C to Z	1.509e-06	1.496e-06	3.740e-08	5.690e-07
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	C12T28SOI_-LRBR0P6_-NAND3X24_P4	C12T28SOI_-LRBR0P6_-NAND3X35_P4	C12T28SOI_-LRBR0P6_-NAND3X47_P4
A (output stable)	-1.467e-09	1.456e-07	5.410e-08	7.350e-08
B (output stable)	-2.720e-08	-2.563e-06	-1.375e-06	-1.816e-06
C (output stable)	-2.243e-08	-6.854e-06	-5.693e-06	-7.247e-06
A to Z	-2.098e-06	-4.782e-06	-2.700e-08	4.930e-07
B to Z	-1.539e-06	-2.208e-06	-2.985e-06	-3.926e-06
C to Z	7.580e-07	2.440e-07	5.930e-07	-7.300e-07
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4			
A (output stable)	-2.050e-08			
B (output stable)	-2.983e-08			
C (output stable)	-3.400e-08			
A to Z	-3.152e-06			
B to Z	-1.875e-06			
C to Z	-2.530e-07			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.816	0.9792
X12_P4	1.200	1.224	1.4688
X18_P4	1.200	1.496	1.7952
X24_P4	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0007	0.0010	0.0010	0.0018
B	0.0007	0.0014	0.0021	0.0028
C	0.0007	0.0014	0.0020	0.0026

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X12_P4**	**X6_P4**	**X12_P4**
A to Z ↓	0.0430	0.0408	6.4885	3.4137
A to Z ↑	0.0305	0.0287	4.0758	2.0451
B to Z ↓	0.0178	0.0183	6.5222	3.4357
B to Z ↑	0.0196	0.0192	4.1308	2.0791
C to Z ↓	0.0172	0.0155	6.5398	3.4467
C to Z ↑	0.0179	0.0162	4.1494	2.0931
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0468	0.0396	2.3479	1.7690

A to Z ↑	0.0331	0.0274	1.3764	1.0317
B to Z ↓	0.0189	0.0183	2.3581	1.7789
B to Z ↑	0.0193	0.0190	1.3994	1.0513
C to Z ↓	0.0166	0.0156	2.3681	1.7874
C to Z ↑	0.0169	0.0160	1.4079	1.0585

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P4	2.302e-06	1.060e-09
X12_P4	4.559e-06	1.417e-09
X18_P4	5.476e-06	1.655e-09
X24_P4	8.814e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	9.661e-04	1.696e-03	2.322e-03	3.115e-03
B (output stable)	4.660e-05	1.564e-04	2.443e-04	3.471e-04
C (output stable)	9.577e-05	4.239e-04	5.194e-04	7.836e-04
A to Z	2.260e-03	4.393e-03	6.392e-03	8.419e-03
B to Z	1.016e-03	1.979e-03	2.981e-03	3.818e-03
C to Z	8.457e-04	1.401e-03	2.253e-03	2.721e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

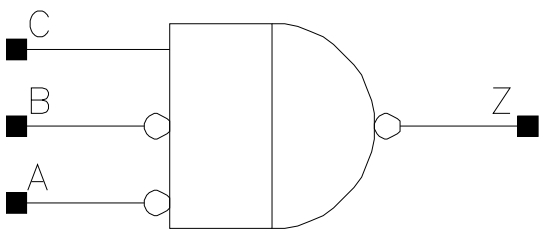
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	-2.600e-09	-1.240e-07	-9.223e-08	-1.453e-07
B (output stable)	2.259e-08	-3.253e-07	-8.327e-08	-1.309e-06
C (output stable)	2.459e-08	-1.617e-06	-6.183e-08	-3.004e-06
A to Z	-3.430e-08	-1.780e-07	-1.080e-07	-1.480e-07
B to Z	1.500e-07	-5.030e-07	-6.260e-07	-1.115e-06
C to Z	3.480e-07	2.550e-07	8.710e-07	-3.750e-07

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	0.816	0.9792
X13_P4	1.200	1.088	1.3056
X20_P4	1.200	1.632	1.9584
X27_P4	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P4	X13_P4	X20_P4	X27_P4
A	0.0009	0.0009	0.0017	0.0016
B	0.0010	0.0010	0.0018	0.0017
C	0.0007	0.0014	0.0020	0.0027

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	**X13_P4**	**X7_P4**	**X13_P4**
A to Z ↓	0.0428	0.0518	4.3260	2.3065
A to Z ↑	0.0256	0.0290	4.0479	2.0354
B to Z ↓	0.0418	0.0510	4.3390	2.3063
B to Z ↑	0.0243	0.0278	4.0449	2.0348
C to Z ↓	0.0122	0.0115	4.3950	2.3240
C to Z ↑	0.0156	0.0145	4.1395	2.0902
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0471	0.0519	1.5673	1.1909
A to Z ↑	0.0271	0.0323	1.3725	1.0311
B to Z ↓	0.0434	0.0490	1.5704	1.1918

B to Z ↑	0.0251	0.0308	1.3705	1.0287
C to Z ↓	0.0126	0.0121	1.5863	1.2003
C to Z ↑	0.0153	0.0149	1.4071	1.0571

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X7_P4	3.583e-06	1.060e-09
X13_P4	4.909e-06	1.298e-09
X20_P4	7.595e-06	1.775e-09
X27_P4	8.462e-06	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	5.649e-04	7.489e-04	1.285e-03	1.514e-03
B (output stable)	4.660e-04	6.517e-04	1.001e-03	1.251e-03
C (output stable)	3.554e-05	2.889e-04	2.883e-04	3.686e-04
A to Z	2.492e-03	4.070e-03	6.480e-03	8.041e-03
B to Z	2.234e-03	3.819e-03	5.638e-03	7.314e-03
C to Z	6.265e-04	1.104e-03	1.832e-03	2.374e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

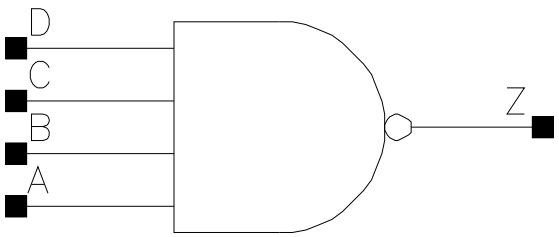
Pin Cycle (vdds)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	-1.926e-07	-2.734e-07	-1.991e-06	-1.950e-06
B (output stable)	1.167e-05	1.168e-05	5.249e-05	5.184e-05
C (output stable)	2.147e-08	-3.513e-08	-8.687e-08	-1.751e-07
A to Z	5.340e-08	-1.922e-07	8.843e-07	7.320e-07
B to Z	-2.712e-07	-2.259e-07	-4.440e-07	-3.260e-07
C to Z	3.320e-08	-4.806e-07	-1.900e-08	-1.038e-06

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0006	0.0006	0.0007	0.0009
B	0.0007	0.0007	0.0008	0.0010
C	0.0006	0.0007	0.0008	0.0009
D	0.0006	0.0006	0.0008	0.0010

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0680	0.0659	2.4777	1.2390
A to Z ↑	0.0513	0.0546	4.1286	2.0525
B to Z ↓	0.0692	0.0680	2.4772	1.2371
B to Z ↑	0.0498	0.0541	4.1268	2.0526
C to Z ↓	0.0684	0.0645	2.4801	1.2374
C to Z ↑	0.0531	0.0570	4.1241	2.0504

D to Z ↓	0.0700	0.0656	2.4788	1.2374
D to Z ↑	0.0522	0.0551	4.1332	2.0489
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0686	0.0627	0.8559	0.6407
A to Z ↑	0.0525	0.0511	1.3810	1.0350
B to Z ↓	0.0701	0.0637	0.8566	0.6413
B to Z ↑	0.0513	0.0497	1.3820	1.0364
C to Z ↓	0.0629	0.0574	0.8557	0.6414
C to Z ↑	0.0535	0.0517	1.3795	1.0350
D to Z ↓	0.0641	0.0585	0.8566	0.6412
D to Z ↑	0.0517	0.0501	1.3819	1.0353

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	4.754e-06	1.417e-09
X17_P4	7.330e-06	1.655e-09
X25_P4	1.033e-05	2.013e-09
X33_P4	1.325e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	3.973e-04	4.996e-04	7.133e-04	8.486e-04
B (output stable)	3.656e-04	4.746e-04	6.697e-04	7.879e-04
C (output stable)	4.034e-04	4.924e-04	7.394e-04	8.438e-04
D (output stable)	3.717e-04	4.560e-04	6.849e-04	7.784e-04
A to Z	2.964e-03	4.402e-03	6.897e-03	8.329e-03
B to Z	2.878e-03	4.325e-03	6.773e-03	8.163e-03
C to Z	3.054e-03	4.333e-03	6.445e-03	7.720e-03
D to Z	2.977e-03	4.238e-03	6.309e-03	7.549e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

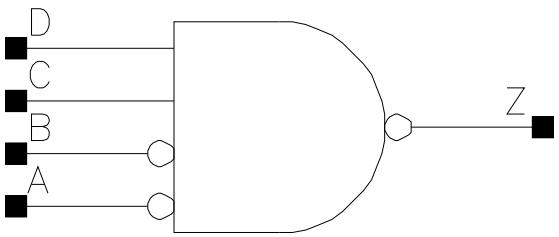
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	-7.242e-08	-5.000e-11	-1.321e-06	-1.245e-06
B (output stable)	-5.287e-08	-1.490e-08	-1.222e-06	-1.111e-06
C (output stable)	4.189e-06	7.736e-06	2.321e-05	2.791e-05
D (output stable)	4.237e-06	7.736e-06	2.321e-05	2.807e-05
A to Z	1.461e-07	4.131e-07	3.959e-07	3.781e-07
B to Z	1.505e-07	1.633e-07	5.948e-07	9.390e-07
C to Z	-9.210e-08	-2.783e-07	-3.910e-07	-2.490e-07
D to Z	-1.120e-07	-3.070e-07	-3.050e-07	-4.281e-07

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X12_P4	1.200	1.496	1.7952
X18_P4	1.200	2.040	2.4480
X24_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0009	0.0009	0.0017	0.0016
B	0.0009	0.0013	0.0018	0.0017
C	0.0007	0.0014	0.0021	0.0028
D	0.0007	0.0014	0.0020	0.0027

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X12_P4	X6_P4	X12_P4
A to Z ↓	0.0454	0.0605	6.6595	3.4256
A to Z ↑	0.0270	0.0326	4.0459	2.0386
B to Z ↓	0.0436	0.0586	6.6589	3.4253
B to Z ↑	0.0248	0.0310	4.0434	2.0368
C to Z ↓	0.0179	0.0182	6.6947	3.4370
C to Z ↑	0.0196	0.0192	4.3454	2.0787

D to Z ↓	0.0170	0.0154	6.7137	3.4450
D to Z ↑	0.0178	0.0162	4.3671	2.0925
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0523	0.0587	2.3437	1.7768
A to Z ↑	0.0290	0.0367	1.3728	1.0322
B to Z ↓	0.0487	0.0557	2.3417	1.7752
B to Z ↑	0.0270	0.0350	1.3707	1.0300
C to Z ↓	0.0185	0.0189	2.3499	1.7811
C to Z ↑	0.0192	0.0195	1.4044	1.0494
D to Z ↓	0.0164	0.0165	2.3603	1.7878
D to Z ↑	0.0167	0.0167	1.4299	1.0573

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P4	2.792e-06	1.179e-09
X12_P4	4.200e-06	1.655e-09
X18_P4	6.461e-06	2.132e-09
X24_P4	6.834e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	6.345e-04	1.078e-03	1.624e-03	1.967e-03
B (output stable)	5.122e-04	9.043e-04	1.266e-03	1.629e-03
C (output stable)	5.672e-05	1.753e-04	2.539e-04	3.602e-04
D (output stable)	1.160e-04	4.573e-04	5.463e-04	8.447e-04
A to Z	2.664e-03	5.061e-03	7.524e-03	9.890e-03
B to Z	2.406e-03	4.694e-03	6.723e-03	9.143e-03
C to Z	9.854e-04	1.969e-03	2.894e-03	4.036e-03
D to Z	8.106e-04	1.390e-03	2.216e-03	2.981e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

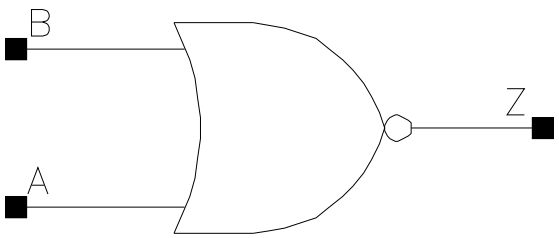
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	-2.751e-07	-1.339e-06	-1.679e-06	-1.847e-06
B (output stable)	1.053e-05	2.751e-05	4.490e-05	4.671e-05
C (output stable)	3.269e-08	-4.302e-07	-4.971e-07	-1.066e-06
D (output stable)	3.391e-08	-1.760e-06	-1.515e-06	-3.837e-06
A to Z	1.902e-07	2.665e-07	6.651e-07	9.240e-07
B to Z	-1.859e-07	-3.260e-07	-3.710e-07	-2.620e-07
C to Z	1.560e-07	-4.380e-07	-6.020e-07	-9.990e-07
D to Z	3.260e-07	2.620e-07	1.548e-06	6.020e-07

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.408	0.4896
X5_P4	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X10_P4	1.200	0.680	0.8160
X14_P4	1.200	0.680	0.8160
X17_P4	1.200	0.952	1.1424
X21_P4	1.200	0.952	1.1424
X24_P4	1.200	1.224	1.4688
X27_P4	1.200	1.224	1.4688
X34_P4	1.200	1.496	1.7952
X40_P4	1.200	1.360	1.6320
X41_P4	1.200	1.768	2.1216
X49_P4	1.200	1.496	1.7952
X53_P4	1.200	1.904	2.2848
X55_P4	1.200	2.312	2.7744
X57_P4	1.200	1.904	2.2848
X65_P4	1.200	2.040	2.4480
X84_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P4	X5_P4	X7_P4	X10_P4
A	0.0005	0.0006	0.0007	0.0012
B	0.0005	0.0006	0.0008	0.0011
	X14_P4	X17_P4	X21_P4	X24_P4

A	0.0015	0.0020	0.0023	0.0026
B	0.0014	0.0018	0.0020	0.0024
	X27_P4	X34_P4	X40_P4	X41_P4
A	0.0029	0.0037	0.0008	0.0045
B	0.0027	0.0033	0.0010	0.0041
	X49_P4	X53_P4	X55_P4	X57_P4
A	0.0009	0.0009	0.0059	0.0009
B	0.0010	0.0008	0.0055	0.0008
	X65_P4	X84_P4		
A	0.0009	0.0010		
B	0.0008	0.0009		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X5_P4**	**X3_P4**	**X5_P4**
A to Z ↓	0.0124	0.0116	4.7436	3.4124
A to Z ↑	0.0250	0.0231	17.9667	12.9552
B to Z ↓	0.0113	0.0102	4.8442	3.4331
B to Z ↑	0.0237	0.0213	18.0310	13.0013
	X7_P4	**X10_P4**	**X7_P4**	**X10_P4**
A to Z ↓	0.0111	0.0117	2.4893	1.6307
A to Z ↑	0.0217	0.0245	9.1089	6.0774
B to Z ↓	0.0097	0.0090	2.5214	1.6444
B to Z ↑	0.0197	0.0184	9.1359	6.1066
	X14_P4	**X17_P4**	**X14_P4**	**X17_P4**
A to Z ↓	0.0113	0.0115	1.2353	0.9948
A to Z ↑	0.0231	0.0232	4.4905	3.6324
B to Z ↓	0.0087	0.0094	1.2470	1.0038
B to Z ↑	0.0174	0.0187	4.5118	3.6449
	X21_P4	**X24_P4**	**X21_P4**	**X24_P4**
A to Z ↓	0.0114	0.0114	0.8458	0.7229
A to Z ↑	0.0224	0.0228	3.0167	2.6247
B to Z ↓	0.0093	0.0089	0.8538	0.7304
B to Z ↑	0.0182	0.0179	3.0271	2.6345
	X27_P4	**X34_P4**	**X27_P4**	**X34_P4**
A to Z ↓	0.0112	0.0117	0.6405	0.5173
A to Z ↑	0.0221	0.0225	2.3018	1.8367
B to Z ↓	0.0087	0.0093	0.6475	0.5226
B to Z ↑	0.0172	0.0181	2.3131	1.8432
	X40_P4	**X41_P4**	**X40_P4**	**X41_P4**
A to Z ↓	0.0410	0.0113	0.5210	0.4313
A to Z ↑	0.0624	0.0222	0.8500	1.5217
B to Z ↓	0.0396	0.0088	0.5206	0.4363
B to Z ↑	0.0618	0.0171	0.8496	1.5294
	X49_P4	**X53_P4**	**X49_P4**	**X53_P4**
A to Z ↓	0.0425	0.0444	0.4340	0.3980
A to Z ↑	0.0636	0.0734	0.7071	0.6547
B to Z ↓	0.0411	0.0429	0.4339	0.3981
B to Z ↑	0.0629	0.0720	0.7073	0.6550
	X55_P4	**X57_P4**	**X55_P4**	**X57_P4**
A to Z ↓	0.0114	0.0446	0.3261	0.3733
A to Z ↑	0.0220	0.0736	1.1458	0.6072

B to Z ↓	0.0089	0.0432	0.3304	0.3734
B to Z ↑	0.0173	0.0722	1.1513	0.6076
	X65_P4	**X84_P4**	**X65_P4**	**X84_P4**
A to Z ↓	0.0455	0.0475	0.3276	0.2610
A to Z ↑	0.0739	0.0747	0.5315	0.4217
B to Z ↓	0.0440	0.0461	0.3278	0.2609
B to Z ↑	0.0726	0.0736	0.5320	0.4211

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P4	9.580e-07	7.027e-10
X5_P4	1.319e-06	7.027e-10
X7_P4	1.779e-06	7.027e-10
X10_P4	2.559e-06	9.409e-10
X14_P4	3.279e-06	9.409e-10
X17_P4	4.109e-06	1.179e-09
X21_P4	4.674e-06	1.179e-09
X24_P4	5.630e-06	1.417e-09
X27_P4	6.075e-06	1.417e-09
X34_P4	7.477e-06	1.655e-09
X40_P4	1.084e-05	1.536e-09
X41_P4	8.879e-06	1.894e-09
X49_P4	1.196e-05	1.655e-09
X53_P4	1.487e-05	2.013e-09
X55_P4	1.168e-05	2.370e-09
X57_P4	1.546e-05	2.013e-09
X65_P4	1.658e-05	2.132e-09
X84_P4	1.849e-05	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	2.125e-05	2.861e-05	3.943e-05	1.152e-04
B (output stable)	1.026e-05	1.429e-05	2.117e-05	7.788e-05
A to Z	5.262e-04	6.391e-04	8.372e-04	1.489e-03
B to Z	3.955e-04	4.594e-04	5.812e-04	8.073e-04
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	1.357e-04	1.646e-04	1.855e-04	2.284e-04
B (output stable)	9.305e-05	1.097e-04	1.125e-04	1.379e-04
A to Z	1.829e-03	2.304e-03	2.625e-03	3.120e-03
B to Z	1.001e-03	1.395e-03	1.588e-03	1.801e-03
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	2.447e-04	2.976e-04	3.981e-05	3.864e-04
B (output stable)	1.472e-04	1.683e-04	2.115e-05	2.355e-04
A to Z	3.383e-03	4.350e-03	8.098e-03	5.141e-03
B to Z	1.912e-03	2.630e-03	7.850e-03	2.851e-03
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	3.995e-05	4.126e-05	4.936e-04	4.133e-05
B (output stable)	2.105e-05	2.228e-05	2.884e-04	2.229e-05
A to Z	8.963e-03	1.133e-02	6.689e-03	1.160e-02
B to Z	8.714e-03	1.105e-02	3.824e-03	1.133e-02
	X65_P4	X84_P4		

A (output stable)	4.138e-05	4.275e-05		
B (output stable)	2.235e-05	2.268e-05		
A to Z	1.238e-02	1.464e-02		
B to Z	1.211e-02	1.431e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

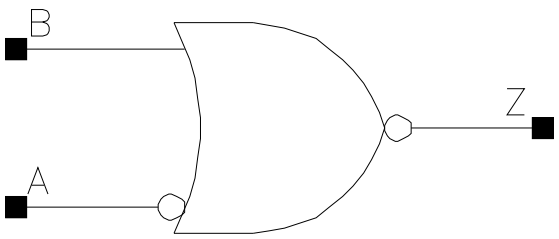
Pin Cycle (vdds)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	-2.630e-07	-2.965e-07	-2.908e-07	-3.570e-06
B (output stable)	1.034e-05	1.307e-05	1.692e-05	7.013e-05
A to Z	-4.820e-08	3.611e-07	4.924e-07	1.455e-06
B to Z	-1.465e-07	-3.550e-08	1.650e-07	7.350e-08
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	-3.435e-06	-2.789e-06	-2.851e-06	-5.255e-06
B (output stable)	8.436e-05	6.504e-05	6.706e-05	1.159e-04
A to Z	2.038e-06	1.767e-06	2.141e-06	2.961e-06
B to Z	2.906e-07	5.257e-07	7.563e-07	5.498e-07
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	-5.124e-06	-4.272e-06	-2.751e-07	-7.708e-06
B (output stable)	1.273e-04	1.112e-04	1.681e-05	1.769e-04
A to Z	3.107e-06	2.888e-06	-4.700e-07	4.332e-06
B to Z	9.157e-07	6.410e-07	-5.250e-07	1.258e-06
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	-2.813e-07	-3.527e-07	-8.601e-06	-3.525e-07
B (output stable)	1.675e-05	1.802e-05	1.966e-04	1.802e-05
A to Z	-8.480e-07	-6.780e-07	5.054e-06	-4.330e-07
B to Z	-2.200e-08	-9.010e-07	1.440e-06	-6.990e-07
	X65_P4	X84_P4		
A (output stable)	-3.522e-07	-3.623e-07		
B (output stable)	1.801e-05	1.860e-05		
A to Z	-3.650e-07	-1.358e-06		
B to Z	-1.278e-06	-6.700e-07		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X7_P4	1.200	0.680	0.8160
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X41_P4	1.200	2.312	2.7744
X55_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X7_P4	X13_P4
A	0.0007	0.0007	0.0007	0.0010
B	0.0005	0.0008	0.0007	0.0013
	X27_P4	X41_P4	X55_P4	
A	0.0018	0.0027	0.0036	
B	0.0027	0.0041	0.0055	

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0339	0.0369	4.6286	2.9845
A to Z ↑	0.0328	0.0323	17.8453	9.0619
B to Z ↓	0.0116	0.0110	4.8272	3.1403
B to Z ↑	0.0240	0.0197	18.0031	9.1522

	X7_P4	X13_P4	X7_P4	X13_P4
A to Z ↓	0.0373	0.0331	2.3558	1.2806
A to Z ↑	0.0351	0.0324	8.9400	4.7054
B to Z ↓	0.0100	0.0091	2.3983	1.3016
B to Z ↑	0.0208	0.0188	8.9958	4.7425
	X27_P4	**X41_P4**	**X27_P4**	**X41_P4**
A to Z ↓	0.0322	0.0328	0.6189	0.4196
A to Z ↑	0.0313	0.0317	2.2637	1.5182
B to Z ↓	0.0089	0.0090	0.6469	0.4374
B to Z ↑	0.0179	0.0178	2.2849	1.5306
	X55_P4		**X55_P4**	
A to Z ↓	0.0321		0.3174	
A to Z ↑	0.0310		1.1428	
B to Z ↓	0.0090		0.3315	
B to Z ↑	0.0177		1.1533	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P4	1.786e-06	8.218e-10
X6_P4	2.438e-06	8.218e-10
X7_P4	2.916e-06	9.409e-10
X13_P4	5.124e-06	1.179e-09
X27_P4	9.430e-06	1.775e-09
X41_P4	1.360e-05	2.370e-09
X55_P4	1.777e-05	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	7.799e-04	9.731e-04	1.038e-03	1.642e-03
B (output stable)	2.232e-05	4.176e-05	8.402e-05	1.750e-04
A to Z	1.361e-03	1.866e-03	2.178e-03	3.621e-03
B to Z	4.057e-04	5.736e-04	6.846e-04	1.097e-03
	X27_P4	X41_P4	X55_P4	
A (output stable)	3.218e-03	4.924e-03	6.322e-03	
B (output stable)	3.579e-04	5.225e-04	6.397e-04	
A to Z	7.183e-03	1.072e-02	1.386e-02	
B to Z	2.112e-03	3.083e-03	4.059e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

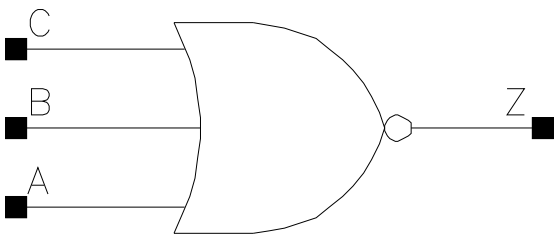
Pin Cycle (vdds)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	-2.858e-07	-1.048e-07	-1.325e-06	-2.394e-06
B (output stable)	1.010e-05	1.669e-05	4.488e-05	7.454e-05
A to Z	1.794e-07	4.246e-07	7.570e-07	1.226e-06
B to Z	-1.308e-07	-3.066e-07	-1.051e-07	1.447e-07
	X27_P4	X41_P4	X55_P4	
A (output stable)	-4.055e-06	-5.858e-06	-7.112e-06	
B (output stable)	1.249e-04	1.731e-04	1.964e-04	
A to Z	1.608e-06	2.085e-06	2.626e-06	
B to Z	5.680e-07	8.870e-07	1.195e-06	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X9_P4	1.200	0.952	1.1424
X13_P4	1.200	0.952	1.1424
X16_P4	1.200	1.360	1.6320
X19_P4	1.200	1.496	1.7952
X22_P4	1.200	1.768	2.1216
X25_P4	1.200	1.904	2.2848
X37_P4	1.200	2.584	3.1008
X49_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P4	X6_P4	X9_P4	X13_P4
A	0.0006	0.0007	0.0011	0.0014
B	0.0006	0.0007	0.0013	0.0016
C	0.0006	0.0008	0.0011	0.0013
	X16_P4	X19_P4	X22_P4	X25_P4
A	0.0019	0.0022	0.0026	0.0029
B	0.0020	0.0026	0.0028	0.0035
C	0.0017	0.0020	0.0024	0.0026
	X37_P4	X49_P4		
A	0.0044	0.0059		
B	0.0045	0.0060		

C	0.0039	0.0054		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0138	0.0131	3.4618	2.5292
A to Z ↑	0.0355	0.0326	19.8874	13.9863
B to Z ↓	0.0132	0.0124	3.4653	2.5326
B to Z ↑	0.0332	0.0302	19.8999	13.9966
C to Z ↓	0.0120	0.0110	3.4874	2.5567
C to Z ↑	0.0295	0.0260	19.9416	14.0213
	X9_P4	**X13_P4**	**X9_P4**	**X13_P4**
A to Z ↓	0.0134	0.0131	1.6847	1.2889
A to Z ↑	0.0355	0.0332	9.2975	6.9023
B to Z ↓	0.0128	0.0122	1.6414	1.2363
B to Z ↑	0.0348	0.0317	9.3028	6.9004
C to Z ↓	0.0104	0.0098	1.6502	1.2537
C to Z ↑	0.0239	0.0220	9.3140	6.9185
	X16_P4	**X19_P4**	**X16_P4**	**X19_P4**
A to Z ↓	0.0134	0.0131	1.0037	0.8434
A to Z ↑	0.0342	0.0337	5.5819	4.6111
B to Z ↓	0.0129	0.0127	1.0068	0.8262
B to Z ↑	0.0328	0.0332	5.5844	4.6164
C to Z ↓	0.0107	0.0105	1.0069	0.8581
C to Z ↑	0.0249	0.0235	5.5952	4.6248
	X22_P4	**X25_P4**	**X22_P4**	**X25_P4**
A to Z ↓	0.0132	0.0130	0.7379	0.6437
A to Z ↑	0.0336	0.0334	3.9804	3.4681
B to Z ↓	0.0126	0.0124	0.7252	0.6200
B to Z ↑	0.0325	0.0327	3.9813	3.4688
C to Z ↓	0.0102	0.0099	0.7299	0.6440
C to Z ↑	0.0232	0.0221	3.9909	3.4765
	X37_P4	**X49_P4**	**X37_P4**	**X49_P4**
A to Z ↓	0.0131	0.0132	0.4431	0.3360
A to Z ↑	0.0326	0.0326	2.3199	1.7453
B to Z ↓	0.0124	0.0125	0.4383	0.3327
B to Z ↑	0.0309	0.0308	2.3207	1.7463
C to Z ↓	0.0102	0.0104	0.4433	0.3363
C to Z ↑	0.0221	0.0225	2.3262	1.7501

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	9.701e-07	8.218e-10
X6_P4	1.326e-06	8.218e-10
X9_P4	1.927e-06	1.179e-09
X13_P4	2.504e-06	1.179e-09
X16_P4	3.118e-06	1.536e-09
X19_P4	3.815e-06	1.655e-09
X22_P4	4.316e-06	1.894e-09
X25_P4	4.959e-06	2.013e-09
X37_P4	7.077e-06	2.608e-09

X49_P4	9.363e-06	3.323e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	3.352e-05	4.478e-05	1.169e-04	1.289e-04
B (output stable)	-6.362e-07	-1.097e-06	2.779e-05	2.699e-05
C (output stable)	1.232e-05	1.823e-05	5.573e-05	6.798e-05
A to Z	9.692e-04	1.230e-03	2.059e-03	2.532e-03
B to Z	7.900e-04	9.810e-04	1.738e-03	2.068e-03
C to Z	6.089e-04	7.180e-04	1.009e-03	1.183e-03
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	1.430e-04	1.767e-04	2.160e-04	2.573e-04
B (output stable)	2.619e-05	3.575e-05	4.660e-05	5.512e-05
C (output stable)	7.674e-05	9.563e-05	1.121e-04	1.303e-04
A to Z	3.268e-03	3.874e-03	4.479e-03	5.085e-03
B to Z	2.691e-03	3.246e-03	3.706e-03	4.244e-03
C to Z	1.767e-03	1.967e-03	2.237e-03	2.399e-03
	X37_P4	X49_P4		
A (output stable)	3.480e-04	4.579e-04		
B (output stable)	6.117e-05	7.706e-05		
C (output stable)	1.917e-04	2.497e-04		
A to Z	7.353e-03	9.812e-03		
B to Z	5.935e-03	7.902e-03		
C to Z	3.499e-03	4.747e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

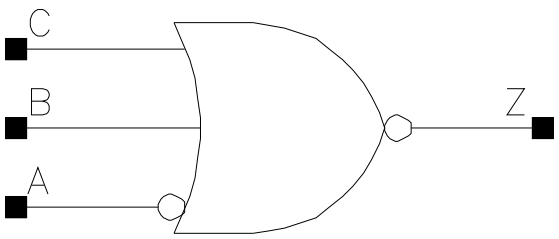
Pin Cycle (vdds)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	-2.016e-06	-2.306e-06	-1.282e-05	-1.186e-05
B (output stable)	1.244e-05	1.710e-05	2.977e-05	3.766e-05
C (output stable)	2.394e-05	3.268e-05	8.593e-05	1.108e-04
A to Z	5.620e-07	1.082e-06	8.350e-07	2.326e-06
B to Z	1.120e-08	4.000e-08	4.480e-07	1.344e-06
C to Z	-2.452e-07	-3.570e-07	-2.284e-07	-2.015e-07
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	-9.804e-06	-1.309e-05	-1.742e-05	-2.214e-05
B (output stable)	4.431e-05	6.259e-05	6.750e-05	8.835e-05
C (output stable)	9.802e-05	1.351e-04	1.637e-04	2.035e-04
A to Z	1.398e-06	2.156e-06	2.596e-06	3.721e-06
B to Z	5.610e-07	8.710e-07	1.317e-06	3.734e-06
C to Z	-1.713e-07	-3.341e-07	-5.595e-07	-5.031e-07
	X37_P4	X49_P4		
A (output stable)	-2.519e-05	-3.219e-05		
B (output stable)	1.101e-04	1.439e-04		
C (output stable)	2.646e-04	3.412e-04		
A to Z	4.562e-06	6.720e-06		
B to Z	3.270e-06	4.763e-06		
C to Z	-7.450e-07	-1.368e-06		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.680	0.8160
X13_P4	1.200	1.224	1.4688
X19_P4	1.200	1.496	1.7952
X25_P4	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0008	0.0010	0.0010	0.0018
B	0.0007	0.0016	0.0023	0.0030
C	0.0008	0.0014	0.0020	0.0027

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X13_P4**	**X6_P4**	**X13_P4**
A to Z ↓	0.0372	0.0348	2.4725	1.3597
A to Z ↑	0.0437	0.0424	14.1288	6.8906
B to Z ↓	0.0126	0.0122	2.5483	1.2424
B to Z ↑	0.0307	0.0319	14.1591	6.9069
C to Z ↓	0.0112	0.0098	2.5600	1.2544
C to Z ↑	0.0265	0.0221	14.1851	6.9183
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0398	0.0348	0.8403	0.6366

A to Z ↑	0.0455	0.0419	4.6247	3.4688
B to Z ↓	0.0128	0.0124	0.8640	0.6439
B to Z ↑	0.0311	0.0309	4.6348	3.4781
C to Z ↓	0.0104	0.0099	0.8591	0.6476
C to Z ↑	0.0237	0.0222	4.6445	3.4848

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P4	2.184e-06	9.409e-10
X13_P4	4.440e-06	1.417e-09
X19_P4	5.250e-06	1.655e-09
X25_P4	8.284e-06	2.251e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	1.004e-03	1.773e-03	2.341e-03	3.480e-03
B (output stable)	1.309e-05	6.512e-05	7.048e-05	1.110e-04
C (output stable)	2.927e-05	1.216e-04	1.302e-04	2.026e-04
A to Z	2.308e-03	4.543e-03	6.269e-03	8.735e-03
B to Z	9.930e-04	2.086e-03	3.017e-03	3.972e-03
C to Z	7.333e-04	1.195e-03	1.955e-03	2.387e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

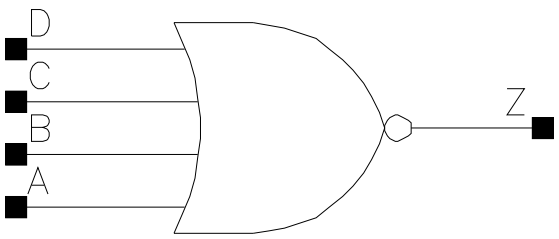
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	-2.102e-06	-8.150e-06	-9.262e-06	-1.534e-05
B (output stable)	1.691e-05	3.501e-05	5.260e-05	7.090e-05
C (output stable)	3.231e-05	1.129e-04	1.189e-04	1.872e-04
A to Z	8.500e-07	1.793e-06	2.588e-06	3.790e-06
B to Z	2.900e-08	1.203e-06	8.210e-07	3.505e-06
C to Z	-9.910e-08	-2.168e-07	-3.155e-07	-4.683e-07

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	1.904	2.2848
X32_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X32_P4
A	0.0006	0.0006	0.0007	0.0008
B	0.0007	0.0006	0.0008	0.0010
C	0.0005	0.0005	0.0007	0.0009
D	0.0006	0.0006	0.0007	0.0008

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0441	0.0429	2.4250	1.1948
A to Z ↑	0.0707	0.0747	4.2106	2.0759
B to Z ↓	0.0425	0.0418	2.4258	1.1947
B to Z ↑	0.0695	0.0737	4.2092	2.0767
C to Z ↓	0.0436	0.0432	2.4190	1.1910
C to Z ↑	0.0718	0.0770	4.2144	2.0760

D to Z ↓	0.0430	0.0426	2.4217	1.1912
D to Z ↑	0.0712	0.0767	4.2105	2.0768
	X25_P4	**X32_P4**	**X25_P4**	**X32_P4**
A to Z ↓	0.0435	0.0459	0.8312	0.6548
A to Z ↑	0.0725	0.0703	1.4154	1.0749
B to Z ↓	0.0424	0.0444	0.8308	0.6547
B to Z ↑	0.0719	0.0692	1.4141	1.0745
C to Z ↓	0.0422	0.0449	0.8283	0.6525
C to Z ↑	0.0720	0.0707	1.4132	1.0750
D to Z ↓	0.0409	0.0429	0.8273	0.6521
D to Z ↑	0.0711	0.0694	1.4132	1.0751

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	3.401e-06	1.417e-09
X17_P4	4.927e-06	1.536e-09
X25_P4	7.458e-06	2.013e-09
X32_P4	9.106e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	4.078e-04	4.951e-04	6.820e-04	8.750e-04
B (output stable)	3.425e-04	4.320e-04	5.994e-04	7.578e-04
C (output stable)	3.844e-04	4.585e-04	7.189e-04	9.231e-04
D (output stable)	3.222e-04	3.993e-04	6.294e-04	8.025e-04
A to Z	2.827e-03	4.226e-03	6.431e-03	8.096e-03
B to Z	2.686e-03	4.099e-03	6.234e-03	7.857e-03
C to Z	2.884e-03	4.243e-03	6.069e-03	7.659e-03
D to Z	2.739e-03	4.112e-03	5.886e-03	7.408e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

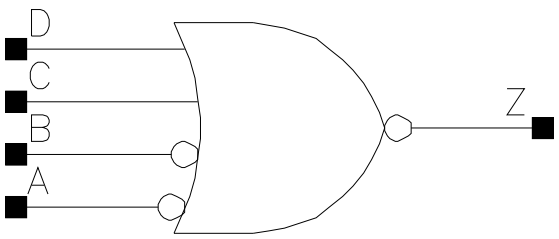
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	-1.823e-07	-1.656e-07	-2.019e-07	-1.287e-07
B (output stable)	5.575e-06	5.322e-06	7.829e-06	1.039e-05
C (output stable)	-1.250e-07	-1.877e-07	-2.190e-07	-2.396e-07
D (output stable)	5.990e-06	5.791e-06	7.960e-06	1.008e-05
A to Z	-1.571e-07	-1.896e-07	-4.758e-07	-4.534e-07
B to Z	-5.870e-08	-2.047e-07	-8.050e-08	-3.289e-07
C to Z	-2.209e-07	-1.514e-07	6.400e-08	-2.144e-07
D to Z	-1.603e-07	-1.607e-07	-1.919e-07	-3.579e-07

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X13_P4	1.200	1.496	1.7952
X19_P4	1.200	2.040	2.4480
X25_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0009	0.0010	0.0018	0.0017
B	0.0010	0.0014	0.0018	0.0018
C	0.0008	0.0015	0.0021	0.0029
D	0.0007	0.0014	0.0020	0.0026

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X13_P4	X6_P4	X13_P4
A to Z ↓	0.0319	0.0395	2.4178	1.2047
A to Z ↑	0.0439	0.0535	13.6061	6.9655
B to Z ↓	0.0300	0.0382	2.4154	1.2028
B to Z ↑	0.0441	0.0545	13.6104	6.9685
C to Z ↓	0.0131	0.0124	2.5773	1.2392
C to Z ↑	0.0310	0.0320	13.6365	6.9818

D to Z ↓	0.0112	0.0100	2.5672	1.2495
D to Z ↑	0.0262	0.0229	13.6641	6.9966
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0346	0.0378	0.8278	0.6253
A to Z ↑	0.0481	0.0518	4.6285	3.4928
B to Z ↓	0.0320	0.0358	0.8265	0.6244
B to Z ↑	0.0477	0.0521	4.6305	3.4894
C to Z ↓	0.0128	0.0125	0.8657	0.6491
C to Z ↑	0.0308	0.0309	4.6378	3.4961
D to Z ↓	0.0104	0.0100	0.8598	0.6475
D to Z ↑	0.0236	0.0221	4.6484	3.5047

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P4	2.543e-06	1.179e-09
X13_P4	3.552e-06	1.655e-09
X19_P4	5.682e-06	2.132e-09
X25_P4	6.392e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	6.074e-04	1.063e-03	1.575e-03	1.928e-03
B (output stable)	5.430e-04	1.012e-03	1.440e-03	1.823e-03
C (output stable)	6.211e-06	4.683e-05	6.233e-05	9.829e-05
D (output stable)	3.348e-05	1.394e-04	1.672e-04	2.746e-04
A to Z	2.739e-03	5.225e-03	7.707e-03	9.915e-03
B to Z	2.570e-03	4.967e-03	7.133e-03	9.406e-03
C to Z	1.037e-03	2.099e-03	2.989e-03	3.935e-03
D to Z	7.610e-04	1.261e-03	1.954e-03	2.354e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

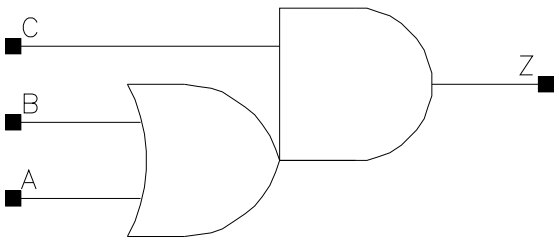
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	-1.010e-06	-6.549e-06	-6.595e-06	-1.039e-05
B (output stable)	-9.200e-07	-7.636e-06	-6.860e-06	-1.133e-05
C (output stable)	2.300e-05	4.430e-05	6.750e-05	8.718e-05
D (output stable)	3.951e-05	1.230e-04	1.365e-04	2.103e-04
A to Z	8.270e-07	7.740e-07	1.848e-06	1.324e-06
B to Z	1.027e-06	1.275e-06	1.874e-06	1.471e-06
C to Z	-5.900e-08	1.792e-06	8.350e-07	1.524e-06
D to Z	-4.714e-07	-4.286e-07	-3.510e-07	-2.976e-07

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0009	0.0009	0.0016
B	0.0010	0.0010	0.0018
C	0.0010	0.0010	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0387	0.0446	2.5054	1.2507
A to Z ↑	0.0299	0.0330	4.2298	2.0791
B to Z ↓	0.0375	0.0437	2.5070	1.2521
B to Z ↑	0.0276	0.0309	4.2264	2.0741
C to Z ↓	0.0320	0.0350	2.4775	1.2275
C to Z ↑	0.0291	0.0317	4.2245	2.0754
	X33_P4		**X33_P4**	
A to Z ↓	0.0460		0.6350	
A to Z ↑	0.0349		1.0444	

B to Z ↓	0.0450		0.6358	
B to Z ↑	0.0322		1.0425	
C to Z ↓	0.0356		0.6216	
C to Z ↑	0.0326		1.0420	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	3.395e-06	9.409e-10
X17_P4	4.775e-06	1.060e-09
X33_P4	9.487e-06	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	8.200e-05	8.315e-05	1.701e-04
B (output stable)	7.884e-05	8.031e-05	1.558e-04
C (output stable)	5.862e-05	6.102e-05	1.165e-04
A to Z	2.109e-03	3.028e-03	6.240e-03
B to Z	1.853e-03	2.772e-03	5.732e-03
C to Z	2.299e-03	3.188e-03	6.491e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

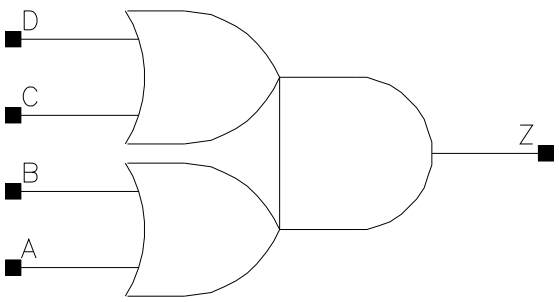
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	-4.506e-07	-4.859e-07	-1.078e-06
B (output stable)	5.383e-06	5.464e-06	1.165e-05
C (output stable)	4.128e-08	5.441e-08	6.585e-08
A to Z	-2.200e-08	-4.330e-08	-8.500e-08
B to Z	-2.663e-07	-1.333e-07	-2.105e-07
C to Z	-6.405e-08	-2.012e-07	-1.571e-07

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0008	0.0017
B	0.0006	0.0009	0.0017
C	0.0006	0.0009	0.0017
D	0.0006	0.0009	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0652	0.0546	2.4515	1.2432
A to Z ↑	0.0422	0.0360	4.1508	2.0728
B to Z ↓	0.0649	0.0538	2.4539	1.2436
B to Z ↑	0.0409	0.0344	4.1408	2.0709

C to Z ↓	0.0574	0.0487	2.4308	1.2352
C to Z ↑	0.0403	0.0354	4.1460	2.0734
D to Z ↓	0.0558	0.0472	2.4330	1.2365
D to Z ↑	0.0382	0.0330	4.1421	2.0698
	X33_P4		**X33_P4**	
A to Z ↓	0.0550		0.6417	
A to Z ↑	0.0359		1.0422	
B to Z ↓	0.0519		0.6428	
B to Z ↑	0.0335		1.0391	
C to Z ↓	0.0483		0.6374	
C to Z ↑	0.0345		1.0412	
D to Z ↓	0.0447		0.6387	
D to Z ↑	0.0318		1.0390	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	3.273e-06	1.179e-09
X17_P4	6.206e-06	1.298e-09
X33_P4	1.153e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.289e-05	3.818e-05	1.119e-04
B (output stable)	1.515e-05	2.540e-05	9.240e-05
C (output stable)	6.676e-05	8.872e-05	2.092e-04
D (output stable)	5.953e-05	7.584e-05	2.032e-04
A to Z	2.459e-03	3.910e-03	7.747e-03
B to Z	2.333e-03	3.647e-03	6.973e-03
C to Z	2.133e-03	3.452e-03	6.774e-03
D to Z	1.992e-03	3.184e-03	5.976e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

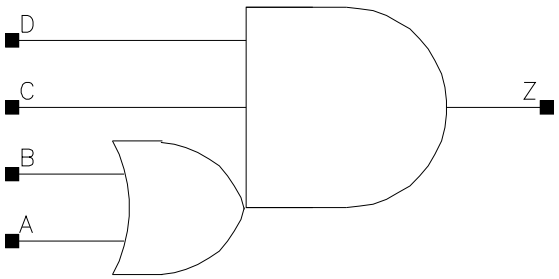
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	-1.624e-07	-1.994e-07	-2.438e-06
B (output stable)	6.114e-06	1.054e-05	5.097e-05
C (output stable)	-5.605e-07	-1.933e-07	-2.787e-06
D (output stable)	6.026e-06	1.102e-05	4.601e-05
A to Z	-1.098e-07	-2.198e-07	2.350e-06
B to Z	-1.661e-07	-1.480e-08	-5.583e-08
C to Z	-8.557e-08	1.190e-07	3.145e-06
D to Z	-8.881e-08	2.756e-08	2.955e-07

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	1.088	1.3056
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0006	0.0009	0.0014	0.0017
B	0.0006	0.0009	0.0015	0.0018
C	0.0007	0.0009	0.0015	0.0018
D	0.0006	0.0010	0.0015	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0557	0.0516	2.5771	1.2560
A to Z ↑	0.0494	0.0447	4.3006	2.0809
B to Z ↓	0.0552	0.0490	2.5803	1.2561
B to Z ↑	0.0469	0.0407	4.2953	2.0745
C to Z ↓	0.0426	0.0387	2.5047	1.2277

C to Z ↑	0.0483	0.0428	4.2896	2.0760
D to Z ↓	0.0415	0.0376	2.5046	1.2264
D to Z ↑	0.0492	0.0437	4.2890	2.0757
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0538	0.0522	0.8526	0.6404
A to Z ↑	0.0455	0.0462	1.4093	1.0568
B to Z ↓	0.0510	0.0495	0.8532	0.6404
B to Z ↑	0.0421	0.0426	1.4082	1.0557
C to Z ↓	0.0408	0.0393	0.8322	0.6248
C to Z ↑	0.0441	0.0439	1.4067	1.0542
D to Z ↓	0.0389	0.0378	0.8302	0.6236
D to Z ↑	0.0438	0.0441	1.4061	1.0548

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	1.998e-06	1.060e-09
X17_P4	3.987e-06	1.298e-09
X25_P4	6.324e-06	2.013e-09
X33_P4	7.893e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	6.772e-05	1.302e-04	2.210e-04	2.428e-04
B (output stable)	6.701e-05	1.264e-04	2.208e-04	2.395e-04
C (output stable)	1.519e-05	3.120e-05	7.780e-05	8.687e-05
D (output stable)	3.044e-05	6.327e-05	2.011e-04	2.131e-04
A to Z	2.045e-03	3.588e-03	5.806e-03	7.260e-03
B to Z	1.920e-03	3.230e-03	5.247e-03	6.552e-03
C to Z	2.216e-03	3.812e-03	6.312e-03	7.685e-03
D to Z	2.126e-03	3.640e-03	5.858e-03	7.242e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

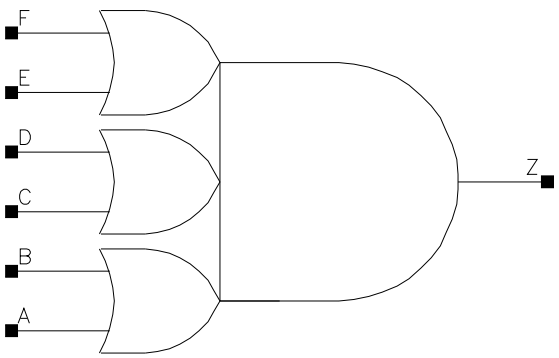
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	-6.141e-07	-1.281e-06	-1.886e-06	-1.179e-06
B (output stable)	9.866e-07	5.935e-06	7.757e-06	1.040e-05
C (output stable)	8.331e-08	6.653e-08	8.308e-08	2.286e-08
D (output stable)	-4.048e-08	-9.987e-08	-1.679e-07	-1.286e-08
A to Z	-9.630e-08	3.770e-07	3.700e-08	2.700e-08
B to Z	-6.126e-08	-2.486e-07	-2.433e-07	-4.046e-07
C to Z	-8.490e-08	1.500e-06	2.321e-06	2.066e-06
D to Z	-3.783e-08	1.233e-06	2.235e-06	2.484e-06

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0008	0.0015
B	0.0006	0.0009	0.0017
C	0.0006	0.0009	0.0015
D	0.0006	0.0009	0.0017
E	0.0006	0.0009	0.0015
F	0.0006	0.0009	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0744	0.0619	2.6474	1.2830
A to Z ↑	0.0552	0.0483	4.2682	2.0956
B to Z ↓	0.0735	0.0616	2.6486	1.2832
B to Z ↑	0.0533	0.0466	4.2685	2.0951
C to Z ↓	0.0684	0.0587	2.6279	1.2798
C to Z ↑	0.0548	0.0477	4.2702	2.0955
D to Z ↓	0.0680	0.0580	2.6287	1.2801
D to Z ↑	0.0526	0.0455	4.2663	2.0940
E to Z ↓	0.0594	0.0518	2.6051	1.2705
E to Z ↑	0.0500	0.0444	4.2685	2.0943
F to Z ↓	0.0593	0.0506	2.6046	1.2718
F to Z ↑	0.0479	0.0418	4.2634	2.0909
	X33_P4		X33_P4	
A to Z ↓	0.0621		0.6560	
A to Z ↑	0.0493		1.0564	
B to Z ↓	0.0619		0.6558	
B to Z ↑	0.0465		1.0547	
C to Z ↓	0.0576		0.6517	
C to Z ↑	0.0484		1.0567	
D to Z ↓	0.0570		0.6519	
D to Z ↑	0.0457		1.0542	
E to Z ↓	0.0507		0.6470	
E to Z ↑	0.0450		1.0556	
F to Z ↓	0.0502		0.6474	
F to Z ↑	0.0422		1.0534	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	3.069e-06	1.417e-09
X17_P4	5.828e-06	1.536e-09
X33_P4	1.104e-05	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	1.947e-05	3.382e-05	6.349e-05
B (output stable)	1.381e-05	2.867e-05	4.877e-05
C (output stable)	3.836e-05	6.274e-05	1.276e-04
D (output stable)	3.411e-05	5.464e-05	1.124e-04
E (output stable)	1.083e-04	1.573e-04	3.034e-04
F (output stable)	1.001e-04	1.458e-04	2.866e-04
A to Z	2.825e-03	4.587e-03	8.894e-03
B to Z	2.687e-03	4.343e-03	8.432e-03
C to Z	2.571e-03	4.231e-03	8.135e-03
D to Z	2.444e-03	3.979e-03	7.654e-03
E to Z	2.232e-03	3.733e-03	7.153e-03
F to Z	2.114e-03	3.476e-03	6.693e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

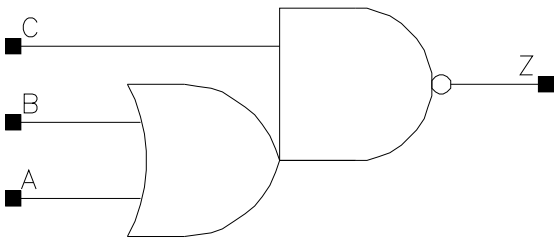
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	-8.485e-08	-9.514e-08	-2.917e-07
B (output stable)	4.027e-06	7.347e-06	1.390e-05
C (output stable)	-1.573e-07	-1.362e-07	-6.767e-07
D (output stable)	3.953e-06	7.331e-06	1.359e-05
E (output stable)	-7.371e-07	-1.746e-07	-1.514e-06
F (output stable)	3.669e-06	7.243e-06	1.265e-05
A to Z	5.866e-08	2.212e-07	-3.111e-08
B to Z	8.333e-10	2.417e-07	3.163e-07
C to Z	-1.343e-07	-2.496e-07	-5.833e-07
D to Z	-8.680e-08	-1.667e-07	-3.321e-07
E to Z	5.218e-08	1.430e-07	2.633e-08
F to Z	9.712e-08	3.678e-08	1.567e-08

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X34_P4	1.200	2.720	3.2640
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X34_P4	X46_P4
A	0.0007	0.0021	0.0043	0.0056
B	0.0007	0.0019	0.0038	0.0052
C	0.0008	0.0022	0.0045	0.0058

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0157	0.0163	4.8722	1.6021
A to Z ↑	0.0231	0.0245	9.0936	3.0529
B to Z ↓	0.0133	0.0137	4.7931	1.6171
B to Z ↑	0.0210	0.0210	9.1241	3.0657
C to Z ↓	0.0157	0.0159	4.4297	1.4731
C to Z ↑	0.0201	0.0199	4.2455	1.4053
	X34_P4	**X46_P4**	**X34_P4**	**X46_P4**
A to Z ↓	0.0170	0.0169	0.8159	0.6218

A to Z ↑	0.0254	0.0251	1.5254	1.1646
B to Z ↓	0.0140	0.0140	0.8245	0.6302
B to Z ↑	0.0213	0.0213	1.5311	1.1691
C to Z ↓	0.0165	0.0163	0.7511	0.5730
C to Z ↑	0.0202	0.0201	0.7025	0.5361

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P4	2.074e-06	8.218e-10
X17_P4	5.670e-06	1.536e-09
X34_P4	1.124e-05	2.727e-09
X46_P4	1.470e-05	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	7.254e-05	2.540e-04	5.348e-04	6.591e-04
B (output stable)	7.052e-05	2.278e-04	4.943e-04	6.023e-04
C (output stable)	5.390e-05	1.842e-04	3.821e-04	4.837e-04
A to Z	9.351e-04	3.055e-03	6.425e-03	8.266e-03
B to Z	6.790e-04	2.063e-03	4.276e-03	5.560e-03
C to Z	1.110e-03	3.412e-03	7.118e-03	9.183e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

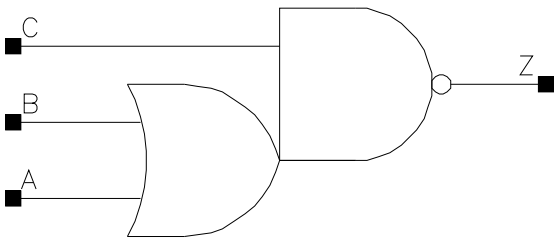
Pin Cycle (vdds)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	-1.354e-07	-2.016e-06	-5.388e-06	-6.253e-06
B (output stable)	5.770e-06	2.279e-05	5.522e-05	6.304e-05
C (output stable)	4.537e-08	-2.000e-08	-9.410e-08	-1.235e-07
A to Z	1.717e-07	9.100e-07	2.988e-06	2.629e-06
B to Z	-1.091e-07	4.700e-08	-1.213e-06	-1.595e-06
C to Z	-2.343e-07	1.660e-06	5.024e-06	4.741e-06

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.544	0.6528
X11_P4	1.200	0.952	1.1424
X17_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X17_P4	X23_P4
A	0.0007	0.0014	0.0022	0.0030
B	0.0007	0.0015	0.0021	0.0027
C	0.0007	0.0014	0.0020	0.0028
	X46_P4			
A	0.0060			
B	0.0055			
C	0.0056			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0170	0.0173	4.9728	2.3275
A to Z ↑	0.0280	0.0282	9.5629	4.5009
B to Z ↓	0.0150	0.0153	4.8969	2.2741

B to Z ↑	0.0262	0.0265	9.5967	4.5149
C to Z ↓	0.0132	0.0131	4.6059	2.1459
C to Z ↑	0.0159	0.0157	4.5279	2.1254
	X17_P4	**X23_P4**	**X17_P4**	**X23_P4**
A to Z ↓	0.0166	0.0175	1.6057	1.1896
A to Z ↑	0.0267	0.0293	2.9867	2.2701
B to Z ↓	0.0146	0.0151	1.6016	1.1890
B to Z ↑	0.0247	0.0257	2.9969	2.2777
C to Z ↓	0.0127	0.0130	1.4962	1.1063
C to Z ↑	0.0149	0.0153	1.4140	1.0747
	X46_P4		**X46_P4**	
A to Z ↓	0.0174		0.6186	
A to Z ↑	0.0288		1.1444	
B to Z ↓	0.0149		0.6139	
B to Z ↑	0.0251		1.1481	
C to Z ↓	0.0131		0.5735	
C to Z ↑	0.0150		0.5426	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P4	2.067e-06	8.218e-10
X11_P4	4.040e-06	1.179e-09
X17_P4	5.844e-06	1.536e-09
X23_P4	7.968e-06	2.013e-09
X46_P4	1.503e-05	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	2.494e-05	5.394e-05	7.978e-05	1.474e-04
B (output stable)	1.695e-05	4.044e-05	5.656e-05	1.055e-04
C (output stable)	1.789e-04	4.406e-04	5.343e-04	8.377e-04
A to Z	1.199e-03	2.590e-03	3.561e-03	5.420e-03
B to Z	9.303e-04	2.042e-03	2.694e-03	3.901e-03
C to Z	6.716e-04	1.461e-03	1.986e-03	2.884e-03
	X46_P4			
A (output stable)	2.828e-04			
B (output stable)	2.006e-04			
C (output stable)	1.525e-03			
A to Z	1.043e-02			
B to Z	7.421e-03			
C to Z	5.537e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	-1.025e-07	-2.899e-07	-4.898e-07	-2.729e-06
B (output stable)	5.567e-06	1.224e-05	1.832e-05	4.138e-05
C (output stable)	1.156e-08	-1.787e-06	-1.154e-06	-2.513e-06
A to Z	8.470e-08	-1.297e-06	-2.320e-07	-1.125e-06
B to Z	-1.823e-07	-5.020e-07	-8.360e-07	-1.039e-06
C to Z	1.721e-07	7.250e-07	-6.000e-08	4.185e-06

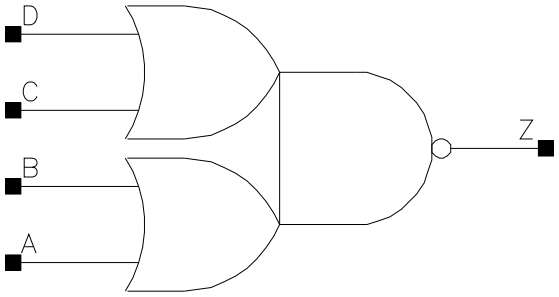
	X46_P4			
A (output stable)	-4.524e-06			
B (output stable)	7.135e-05			
C (output stable)	-4.135e-06			
A to Z	2.932e-06			
B to Z	-2.551e-06			
C to Z	5.151e-06			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0008	0.0015	0.0022	0.0030
B	0.0008	0.0013	0.0020	0.0027
C	0.0007	0.0014	0.0021	0.0029
D	0.0007	0.0013	0.0019	0.0026
	X42_P4			
A	0.0061			
B	0.0055			
C	0.0057			
D	0.0053			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0185	0.0196	4.5113	2.2668
A to Z ↑	0.0322	0.0326	10.0095	4.6050
B to Z ↓	0.0168	0.0173	4.4374	2.2693
B to Z ↑	0.0300	0.0285	10.0264	4.6199
C to Z ↓	0.0161	0.0173	4.5524	2.2746
C to Z ↑	0.0244	0.0261	9.8301	4.6107
D to Z ↓	0.0138	0.0142	4.4712	2.2851
D to Z ↑	0.0220	0.0209	9.8636	4.6342
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0189	0.0192	1.5537	1.1165
A to Z ↑	0.0306	0.0316	3.0906	2.2763
B to Z ↓	0.0170	0.0167	1.5614	1.1141
B to Z ↑	0.0276	0.0279	3.1007	2.2839
C to Z ↓	0.0168	0.0167	1.5595	1.1213
C to Z ↑	0.0244	0.0247	3.0949	2.2765
D to Z ↓	0.0142	0.0138	1.5793	1.1241
D to Z ↑	0.0204	0.0201	3.1111	2.2888
	X42_P4		**X42_P4**	
A to Z ↓	0.0196		0.5825	
A to Z ↑	0.0318		1.1540	
B to Z ↓	0.0172		0.5767	
B to Z ↑	0.0283		1.1574	
C to Z ↓	0.0175		0.5860	
C to Z ↑	0.0253		1.1483	
D to Z ↓	0.0145		0.5815	
D to Z ↑	0.0209		1.1537	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P4	2.386e-06	9.409e-10
X10_P4	4.842e-06	1.536e-09
X15_P4	6.697e-06	1.894e-09
X21_P4	9.044e-06	2.489e-09
X42_P4	1.740e-05	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	3.409e-05	1.089e-04	1.417e-04	2.080e-04
B (output stable)	2.251e-05	8.850e-05	1.035e-04	1.484e-04
C (output stable)	7.309e-05	1.976e-04	2.593e-04	3.718e-04
D (output stable)	6.446e-05	1.799e-04	2.188e-04	3.141e-04
A to Z	1.461e-03	3.349e-03	4.555e-03	6.446e-03
B to Z	1.201e-03	2.540e-03	3.512e-03	4.910e-03
C to Z	1.013e-03	2.433e-03	3.290e-03	4.545e-03
D to Z	7.702e-04	1.628e-03	2.256e-03	3.048e-03
	X42_P4			
A (output stable)	4.104e-04			
B (output stable)	2.981e-04			
C (output stable)	7.331e-04			
D (output stable)	6.255e-04			

A to Z	1.287e-02			
B to Z	9.849e-03			
C to Z	9.274e-03			
D to Z	6.342e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

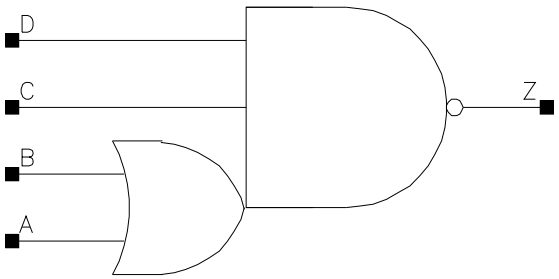
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	-2.003e-07	-2.393e-06	-1.808e-06	-3.635e-06
B (output stable)	1.048e-05	4.949e-05	3.919e-05	7.638e-05
C (output stable)	-3.918e-07	-2.972e-06	-2.364e-06	-4.436e-06
D (output stable)	1.001e-05	4.821e-05	3.781e-05	7.416e-05
A to Z	-2.410e-07	2.683e-06	7.437e-07	2.805e-06
B to Z	-4.315e-07	-3.963e-07	-7.650e-07	-1.343e-06
C to Z	2.303e-07	3.682e-06	2.433e-06	4.800e-06
D to Z	-1.470e-08	6.523e-07	1.144e-06	9.130e-07
	X42_P4			
A (output stable)	-6.280e-06			
B (output stable)	1.354e-04			
C (output stable)	-8.159e-06			
D (output stable)	1.332e-04			
A to Z	4.468e-06			
B to Z	-1.913e-06			
C to Z	9.565e-06			
D to Z	2.804e-06			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X21_P4	1.200	2.448	2.9376
X31_P4	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X21_P4	X31_P4
A	0.0007	0.0014	0.0028	0.0042
B	0.0009	0.0013	0.0025	0.0037
C	0.0007	0.0015	0.0029	0.0044
D	0.0007	0.0014	0.0028	0.0042

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0230	0.0217	6.5062	3.4435
A to Z ↑	0.0307	0.0282	9.0415	4.5419
B to Z ↓	0.0207	0.0179	6.5165	3.4466
B to Z ↑	0.0287	0.0241	9.0899	4.5644
C to Z ↓	0.0221	0.0225	6.1380	3.2497

C to Z ↑	0.0241	0.0235	4.1253	2.0776
D to Z ↓	0.0229	0.0218	6.1545	3.2594
D to Z ↑	0.0231	0.0217	4.1704	2.0800
	X21_P4	**X31_P4**	**X21_P4**	**X31_P4**
A to Z ↓	0.0220	0.0223	1.7921	1.2146
A to Z ↑	0.0277	0.0277	2.2702	1.5217
B to Z ↓	0.0181	0.0182	1.7981	1.2196
B to Z ↑	0.0236	0.0236	2.2815	1.5296
C to Z ↓	0.0224	0.0226	1.6928	1.1483
C to Z ↑	0.0230	0.0231	1.0519	0.7086
D to Z ↓	0.0220	0.0222	1.6972	1.1512
D to Z ↑	0.0214	0.0214	1.0527	0.7076

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P4	1.889e-06	1.060e-09
X10_P4	3.482e-06	1.536e-09
X21_P4	6.440e-06	2.489e-09
X31_P4	9.406e-06	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	1.275e-04	2.712e-04	5.019e-04	7.445e-04
B (output stable)	1.223e-04	2.658e-04	4.899e-04	7.203e-04
C (output stable)	3.014e-05	8.787e-05	1.681e-04	2.526e-04
D (output stable)	5.814e-05	2.214e-04	4.057e-04	5.855e-04
A to Z	1.487e-03	2.567e-03	4.976e-03	7.410e-03
B to Z	1.119e-03	1.789e-03	3.438e-03	5.154e-03
C to Z	1.719e-03	3.278e-03	6.279e-03	9.355e-03
D to Z	1.561e-03	2.762e-03	5.311e-03	7.915e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

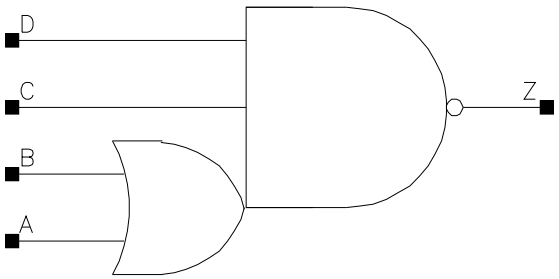
Pin Cycle (vdds)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	-1.394e-06	-2.104e-06	-4.148e-06	-5.488e-06
B (output stable)	5.677e-06	9.747e-06	1.499e-05	2.108e-05
C (output stable)	5.869e-08	4.882e-08	2.826e-08	-1.864e-08
D (output stable)	-9.848e-08	-2.299e-07	-6.350e-07	-8.755e-07
A to Z	9.570e-07	1.619e-06	2.354e-06	3.304e-06
B to Z	-3.290e-08	-2.710e-07	-6.110e-07	-8.270e-07
C to Z	1.364e-06	1.138e-06	9.673e-07	1.579e-06
D to Z	1.696e-06	9.167e-07	1.602e-06	1.989e-06

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0008	0.0015	0.0023	0.0030
B	0.0007	0.0014	0.0021	0.0028
C	0.0007	0.0014	0.0022	0.0028
D	0.0007	0.0014	0.0020	0.0027

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0224	0.0242	6.6380	3.4343
A to Z ↑	0.0323	0.0349	8.8447	4.4890
B to Z ↓	0.0200	0.0211	6.5438	3.4307
B to Z ↑	0.0308	0.0317	8.8653	4.5027
C to Z ↓	0.0180	0.0201	6.2410	3.2524

C to Z ↑	0.0194	0.0204	4.1884	2.1167
D to Z ↓	0.0175	0.0181	6.2696	3.2662
D to Z ↑	0.0176	0.0177	4.2092	2.1284
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0238	0.0240	2.3616	1.7789
A to Z ↑	0.0336	0.0343	3.0181	2.2827
B to Z ↓	0.0209	0.0209	2.3554	1.7717
B to Z ↑	0.0307	0.0314	3.0260	2.2878
C to Z ↓	0.0197	0.0200	2.2360	1.6815
C to Z ↑	0.0196	0.0199	1.4104	1.0624
D to Z ↓	0.0178	0.0182	2.2453	1.6879
D to Z ↑	0.0171	0.0174	1.4182	1.0690

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P4	1.842e-06	1.060e-09
X10_P4	3.573e-06	1.536e-09
X15_P4	4.871e-06	1.894e-09
X21_P4	6.707e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	2.054e-05	4.839e-05	7.092e-05	9.282e-05
B (output stable)	1.611e-05	4.183e-05	5.718e-05	7.545e-05
C (output stable)	6.342e-05	1.429e-04	2.198e-04	2.856e-04
D (output stable)	1.038e-04	3.878e-04	4.666e-04	6.854e-04
A to Z	1.653e-03	3.643e-03	5.138e-03	7.028e-03
B to Z	1.364e-03	2.860e-03	4.022e-03	5.517e-03
C to Z	1.065e-03	2.427e-03	3.359e-03	4.638e-03
D to Z	8.902e-04	1.876e-03	2.646e-03	3.607e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

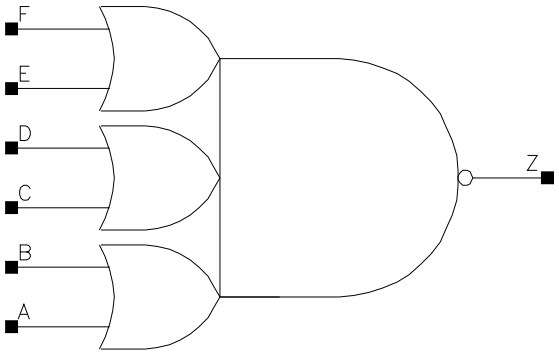
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	-3.809e-08	-1.077e-06	-9.334e-07	-1.696e-06
B (output stable)	2.600e-06	1.111e-05	1.041e-05	1.794e-05
C (output stable)	3.207e-08	-1.441e-07	-5.208e-07	-3.775e-07
D (output stable)	1.335e-08	-1.403e-06	-1.560e-06	-2.583e-06
A to Z	3.940e-07	1.685e-06	1.683e-06	2.795e-06
B to Z	-2.500e-08	-3.220e-07	-3.230e-07	-6.100e-07
C to Z	1.977e-07	1.832e-06	1.182e-06	2.719e-06
D to Z	4.323e-07	3.088e-06	2.034e-06	4.596e-06

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	1.088	1.3056
X9_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X9_P4
A	0.0006	0.0015
B	0.0006	0.0014
C	0.0006	0.0015
D	0.0006	0.0013
E	0.0006	0.0014
F	0.0006	0.0013

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X9_P4	X3_P4	X9_P4
A to Z ↓	0.0283	0.0294	7.6744	3.1037
A to Z ↑	0.0431	0.0409	12.5102	4.5148
B to Z ↓	0.0268	0.0264	7.7103	3.1019
B to Z ↑	0.0427	0.0376	12.5298	4.5251
C to Z ↓	0.0271	0.0275	7.7182	3.1133
C to Z ↑	0.0378	0.0358	12.5253	4.5061
D to Z ↓	0.0251	0.0245	7.7418	3.1153
D to Z ↑	0.0370	0.0322	12.5498	4.5185
E to Z ↓	0.0226	0.0235	7.7326	3.1069
E to Z ↑	0.0299	0.0290	12.5391	4.5071
F to Z ↓	0.0207	0.0200	7.7567	3.1093
F to Z ↑	0.0290	0.0246	12.5877	4.5257

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P4	2.247e-06	1.298e-09
X9_P4	5.575e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P4	X9_P4
A (output stable)	2.646e-05	9.642e-05
B (output stable)	2.055e-05	8.197e-05
C (output stable)	5.416e-05	1.605e-04
D (output stable)	4.768e-05	1.507e-04
E (output stable)	1.401e-04	3.475e-04
F (output stable)	1.354e-04	3.300e-04
A to Z	1.937e-03	5.049e-03
B to Z	1.752e-03	4.252e-03
C to Z	1.588e-03	4.125e-03
D to Z	1.405e-03	3.393e-03
E to Z	1.154e-03	3.153e-03
F to Z	9.800e-04	2.384e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

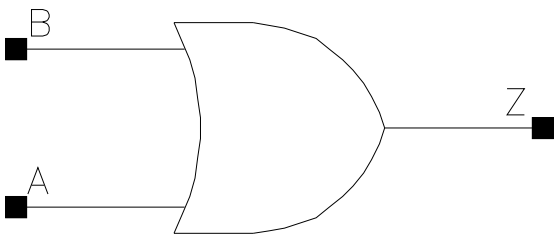
Pin Cycle (vdds)	X3_P4	X9_P4
A (output stable)	-7.156e-08	-1.682e-06
B (output stable)	5.340e-06	3.237e-05
C (output stable)	-1.522e-07	-1.785e-06
D (output stable)	5.515e-06	3.075e-05
E (output stable)	-6.490e-07	-2.994e-06
F (output stable)	4.879e-06	3.036e-05
A to Z	5.111e-07	7.430e-06
B to Z	2.906e-07	4.298e-06
C to Z	5.789e-08	6.431e-06
D to Z	-1.201e-07	1.885e-06
E to Z	5.317e-07	6.245e-06
F to Z	2.610e-07	3.376e-06

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X33_P4	1.200	1.360	1.6320
X50_P4	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P4	X16_P4	X33_P4	X50_P4
A	0.0007	0.0009	0.0017	0.0017
B	0.0006	0.0009	0.0017	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0509	0.0447	2.5126	1.2701
A to Z ↑	0.0285	0.0290	4.1815	2.1038
B to Z ↓	0.0490	0.0432	2.5160	1.2701
B to Z ↑	0.0271	0.0273	4.1841	2.1070
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0458	0.0533	0.6282	0.4337
A to Z ↑	0.0286	0.0283	1.0262	0.6920
B to Z ↓	0.0425	0.0505	0.6285	0.4340
B to Z ↑	0.0265	0.0267	1.0265	0.6921

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	3.063e-06	8.218e-10
X16_P4	5.442e-06	9.409e-10
X33_P4	1.069e-05	1.536e-09
X50_P4	1.432e-05	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	2.211e-05	4.174e-05	1.340e-04	1.270e-04
B (output stable)	1.142e-05	2.106e-05	1.135e-04	1.032e-04
A to Z	1.862e-03	2.969e-03	6.207e-03	8.262e-03
B to Z	1.714e-03	2.711e-03	5.429e-03	7.532e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

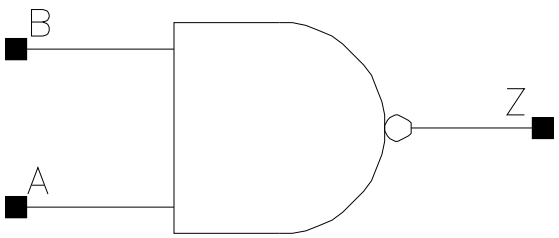
Pin Cycle (vdds)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	-2.675e-07	-3.921e-07	-3.583e-06	-3.405e-06
B (output stable)	1.091e-05	1.830e-05	7.961e-05	7.753e-05
A to Z	-1.455e-07	-2.990e-08	1.085e-06	8.328e-07
B to Z	-1.547e-07	-1.011e-07	-6.558e-07	-6.156e-07

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X16_P4	1.200	0.952	1.1424
X24_P4	1.200	1.088	1.3056
X32_P4	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P4	X16_P4	X24_P4	X32_P4
A	0.0009	0.0009	0.0009	0.0009
B	0.0010	0.0010	0.0010	0.0010

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0394	0.0407	2.4248	1.2625
A to Z ↑	0.0424	0.0431	4.2226	2.1483
B to Z ↓	0.0404	0.0418	2.4253	1.2617
B to Z ↑	0.0408	0.0411	4.2153	2.1519
	X24_P4	**X32_P4**	**X24_P4**	**X32_P4**
A to Z ↓	0.0448	0.0453	0.8574	0.6470
A to Z ↑	0.0460	0.0469	1.4356	1.0716
B to Z ↓	0.0459	0.0466	0.8559	0.6469
B to Z ↑	0.0439	0.0453	1.4368	1.0739

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	5.288e-06	1.060e-09
X16_P4	7.166e-06	1.179e-09
X24_P4	8.893e-06	1.298e-09
X32_P4	1.094e-05	1.417e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	2.278e-05	2.286e-05	2.293e-05	2.421e-05
B (output stable)	3.096e-05	3.116e-05	3.123e-05	3.469e-05
A to Z	3.604e-03	4.132e-03	5.192e-03	6.809e-03
B to Z	3.448e-03	3.987e-03	5.055e-03	6.654e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

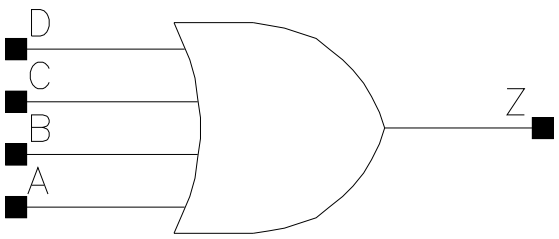
Pin Cycle (vdds)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	3.776e-08	4.020e-08	4.039e-08	3.439e-08
B (output stable)	1.470e-08	1.443e-08	1.483e-08	1.552e-08
A to Z	-4.045e-07	-3.370e-07	-3.566e-07	-4.911e-07
B to Z	-3.859e-07	-1.266e-07	-3.461e-07	-3.020e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P4	1.200	2.176	2.6112
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P4	X27_P4
A	0.0015	0.0017
B	0.0014	0.0017
C	0.0015	0.0018
D	0.0014	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P4	X27_P4	X20_P4	X27_P4
A to Z ↓	0.0512	0.0531	1.5916	1.1941
A to Z ↑	0.0301	0.0289	1.3753	1.0247
B to Z ↓	0.0484	0.0496	1.5918	1.1912
B to Z ↑	0.0285	0.0270	1.3726	1.0234
C to Z ↓	0.0491	0.0514	1.5922	1.1926
C to Z ↑	0.0286	0.0282	1.3769	1.0291
D to Z ↓	0.0462	0.0484	1.5940	1.1927
D to Z ↑	0.0271	0.0266	1.3757	1.0276

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X20_P4	7.990e-06	2.251e-09
X27_P4	1.121e-05	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X20_P4	X27_P4
A (output stable)	1.402e-03	1.934e-03
B (output stable)	1.151e-03	1.576e-03
C (output stable)	1.290e-03	1.865e-03
D (output stable)	1.031e-03	1.538e-03
A to Z	5.831e-03	8.192e-03
B to Z	5.283e-03	7.371e-03
C to Z	5.134e-03	7.147e-03
D to Z	4.582e-03	6.415e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

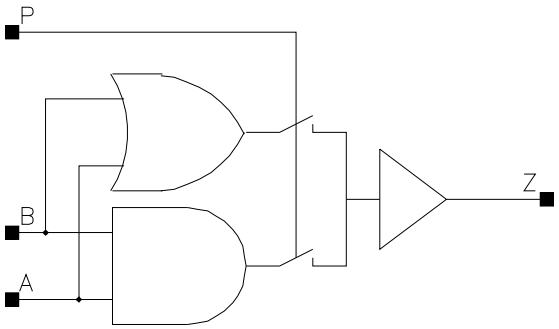
Pin Cycle (vdds)	X20_P4	X27_P4
A (output stable)	-7.985e-07	-1.627e-06
B (output stable)	2.211e-05	4.663e-05
C (output stable)	-8.297e-07	-2.555e-06
D (output stable)	2.210e-05	4.774e-05
A to Z	1.058e-07	1.423e-06
B to Z	-1.260e-07	-4.510e-07
C to Z	5.592e-07	1.649e-06
D to Z	-1.150e-07	-1.500e-07

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X16_P4	1.200	1.224	1.4688
X25_P4	1.200	2.040	2.4480
X33_P4	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0011	0.0016	0.0028	0.0028
B	0.0010	0.0016	0.0032	0.0032
P	0.0006	0.0009	0.0016	0.0016

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0615	0.0549	2.5790	1.2582
A to Z ↑	0.0396	0.0359	4.2460	2.1210
B to Z ↓	0.0605	0.0542	2.5935	1.2680
B to Z ↑	0.0405	0.0367	4.2521	2.1213
P to Z ↓	0.0542	0.0491	2.5972	1.2693
P to Z ↑	0.0386	0.0353	4.2396	2.1201
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**

A to Z ↓	0.0526	0.0560	0.8559	0.6495
A to Z ↑	0.0356	0.0374	1.4261	1.0674
B to Z ↓	0.0517	0.0547	0.8610	0.6524
B to Z ↑	0.0368	0.0381	1.4252	1.0676
P to Z ↓	0.0475	0.0508	0.8623	0.6544
P to Z ↑	0.0348	0.0364	1.4230	1.0660

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	2.885e-06	1.179e-09
X16_P4	5.832e-06	1.417e-09
X25_P4	9.502e-06	2.132e-09
X33_P4	1.089e-05	2.251e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	4.616e-05	7.450e-05	1.651e-04	1.655e-04
B (output stable)	4.452e-05	8.056e-05	2.103e-04	2.132e-04
P (output stable)	1.008e-04	1.728e-04	2.966e-04	3.028e-04
A to Z	2.167e-03	3.634e-03	6.308e-03	7.256e-03
B to Z	2.099e-03	3.519e-03	6.046e-03	6.995e-03
P to Z	1.873e-03	3.194e-03	5.563e-03	6.499e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

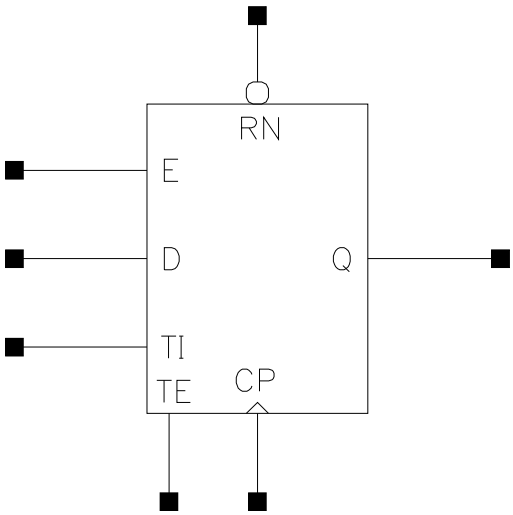
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	-9.708e-07	-9.910e-07	-1.764e-06	-1.773e-06
B (output stable)	4.485e-06	7.900e-06	1.996e-05	2.005e-05
P (output stable)	1.737e-05	3.050e-05	4.158e-05	4.196e-05
A to Z	-5.700e-08	2.251e-07	-5.750e-07	-4.540e-07
B to Z	-9.565e-08	-3.010e-08	-5.213e-07	-6.559e-07
P to Z	-3.436e-08	-9.145e-08	-1.940e-07	-2.059e-07

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.488	5.3856
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
E	0.0008	0.0010	0.0010	0.0010
RN	0.0007	0.0006	0.0007	0.0007
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.1212	0.0581	5.8361	2.5008
CP to Q ↑	0.0908	0.0747	8.8085	4.1991
RN to Q ↓	0.0940	0.0778	4.8585	2.6660
	X17_P4	X33_P4	X17_P4	X33_P4
CP to Q ↓	0.1008	0.1053	1.2121	0.6391
CP to Q ↑	0.1230	0.1279	2.0585	1.0490
RN to Q ↓	0.1345	0.1387	1.2087	0.6362

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1751	0.1166	0.1185	0.1166
CP ↑	min_pulse_width to CP	0.1120	0.0491	0.0406	0.0406
D ↓	hold_rising to CP	-0.1866	-0.0943	-0.0973	-0.0973
D ↑	hold_rising to CP	-0.1013	-0.0361	-0.0361	-0.0361
D ↓	setup_rising to CP	0.2560	0.1584	0.1584	0.1584
D ↑	setup_rising to CP	0.1439	0.0759	0.0759	0.0759
E ↓	hold_rising to CP	-0.1209	-0.1182	-0.1209	-0.1209
E ↑	hold_rising to CP	-0.0991	-0.0383	-0.0383	-0.0383
E ↓	setup_rising to CP	0.2190	0.2169	0.2169	0.2169
E ↑	setup_rising to CP	0.2442	0.1660	0.1660	0.1660
RN ↓	min_pulse_width to RN	0.0969	0.1067	0.0974	0.0974
RN ↑	recovery_rising to CP	0.0297	0.0297	0.0297	0.0297
RN ↑	removal_rising to CP	-0.0197	-0.0099	-0.0096	-0.0096
TE ↓	hold_rising to CP	-0.0889	-0.0654	-0.0650	-0.0650
TE ↑	hold_rising to CP	-0.0698	-0.0454	-0.0454	-0.0454
TE ↓	setup_rising to CP	0.1658	0.1291	0.1291	0.1291
TE ↑	setup_rising to CP	0.3175	0.2225	0.2250	0.2250
TI ↓	hold_rising to CP	-0.2391	-0.1347	-0.1342	-0.1340
TI ↑	hold_rising to CP	-0.0804	-0.0472	-0.0472	-0.0472
TI ↓	setup_rising to CP	0.3136	0.2035	0.2035	0.2035
TI ↑	setup_rising to CP	0.1213	0.0881	0.0881	0.0881

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	1.062e-05	4.557e-09
X8_P4	1.154e-05	4.276e-09
X17_P4	1.412e-05	4.514e-09
X33_P4	1.704e-05	4.752e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

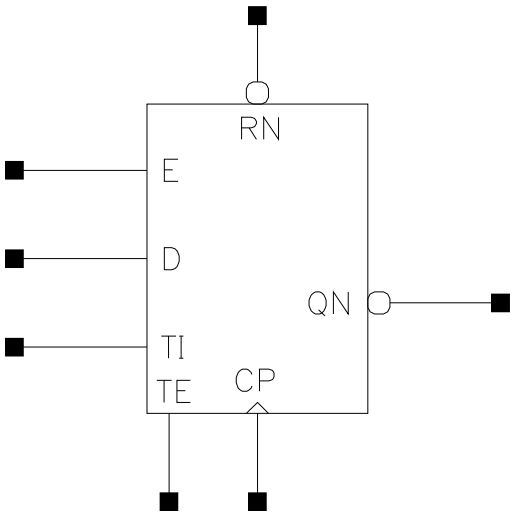
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.424e-03	3.448e-03	3.454e-03	3.457e-03
Clock 100Mhz Data 25Mhz	5.591e-03	5.700e-03	6.237e-03	6.828e-03
Clock 100Mhz Data 50Mhz	7.758e-03	7.953e-03	9.020e-03	1.020e-02
Clock = 0 Data 100Mhz	4.909e-03	4.762e-03	4.714e-03	4.691e-03
Clock = 1 Data 100Mhz	1.903e-03	1.926e-03	1.935e-03	1.939e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.624	5.5488
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
E	0.0008	0.0010	0.0010	0.0010
RN	0.0007	0.0007	0.0007	0.0007
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.1129	0.1025	4.7205	2.4119
CP to QN ↑	0.1347	0.0776	8.6183	4.0908
RN to QN ↑	0.1148	0.1137	8.5915	4.0833
	X17_P4	X33_P4	X17_P4	X33_P4
CP to QN ↓	0.0967	0.1016	1.2138	0.6385
CP to QN ↑	0.0812	0.0875	2.0582	1.0509
RN to QN ↑	0.1114	0.1217	2.0663	1.0546

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1751	0.1166	0.1166	0.1166
CP ↑	min_pulse_width to CP	0.0830	0.0406	0.0465	0.0502
D ↓	hold_rising to CP	-0.1889	-0.0943	-0.0943	-0.0943
D ↑	hold_rising to CP	-0.1044	-0.0361	-0.0361	-0.0361
D ↓	setup_rising to CP	0.2557	0.1584	0.1584	0.1584
D ↑	setup_rising to CP	0.1442	0.0759	0.0755	0.0755
E ↓	hold_rising to CP	-0.1209	-0.1209	-0.1182	-0.1182
E ↑	hold_rising to CP	-0.0991	-0.0383	-0.0383	-0.0383
E ↓	setup_rising to CP	0.2239	0.2169	0.2169	0.2169
E ↑	setup_rising to CP	0.2442	0.1660	0.1660	0.1660
RN ↓	min_pulse_width to RN	0.0969	0.1001	0.1067	0.1165
RN ↑	recovery_rising to CP	0.0297	0.0290	0.0293	0.0293
RN ↑	removal_rising to CP	-0.0197	-0.0151	-0.0096	-0.0096
TE ↓	hold_rising to CP	-0.0889	-0.0650	-0.0623	-0.0623
TE ↑	hold_rising to CP	-0.0698	-0.0454	-0.0454	-0.0458
TE ↓	setup_rising to CP	0.1658	0.1291	0.1291	0.1295
TE ↑	setup_rising to CP	0.3178	0.2250	0.2250	0.2250
TI ↓	hold_rising to CP	-0.2442	-0.1342	-0.1306	-0.1306
TI ↑	hold_rising to CP	-0.0802	-0.0472	-0.0472	-0.0477
TI ↓	setup_rising to CP	0.3136	0.2035	0.2030	0.2030
TI ↑	setup_rising to CP	0.1198	0.0881	0.0881	0.0881

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	1.111e-05	4.557e-09
X8_P4	1.225e-05	4.395e-09
X17_P4	1.490e-05	4.514e-09
X33_P4	1.842e-05	4.752e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

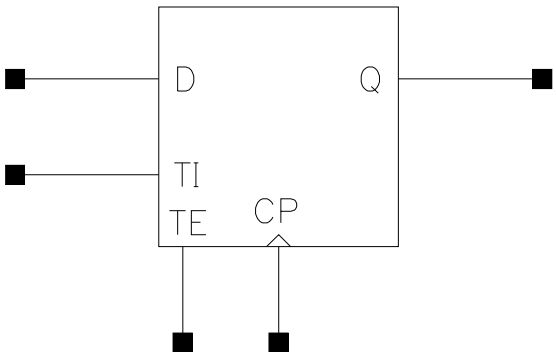
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.422e-03	3.447e-03	3.451e-03	3.453e-03
Clock 100Mhz Data 25Mhz	5.571e-03	5.737e-03	6.194e-03	6.776e-03
Clock 100Mhz Data 50Mhz	7.719e-03	8.027e-03	8.938e-03	1.010e-02
Clock = 0 Data 100Mhz	4.907e-03	4.762e-03	4.715e-03	4.692e-03
Clock = 1 Data 100Mhz	1.902e-03	1.927e-03	1.937e-03	1.942e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.400	4.0800
X8_P4	1.200	3.128	3.7536
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0979	0.0539	5.4454	2.4916
CP to Q ↑	0.0811	0.0674	8.8689	4.1449
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0826	0.0896	1.1860	0.6266
CP to Q ↑	0.1207	0.1267	2.0539	1.0460

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1552	0.1620	0.1615	0.1615
CP ↑	min_pulse_width to CP	0.0782	0.0406	0.0407	0.0407
D ↓	hold_rising to CP	-0.1164	-0.0504	-0.0534	-0.0534
D ↑	hold_rising to CP	-0.0405	-0.0090	-0.0086	-0.0086
D ↓	setup_rising to CP	0.1657	0.1100	0.1100	0.1100
D ↑	setup_rising to CP	0.0752	0.0387	0.0387	0.0387
TE ↓	hold_rising to CP	-0.0690	-0.0455	-0.0480	-0.0480
TE ↑	hold_rising to CP	-0.0552	-0.0361	-0.0361	-0.0361
TE ↓	setup_rising to CP	0.1392	0.1048	0.1048	0.1048
TE ↑	setup_rising to CP	0.2780	0.2195	0.2195	0.2195
TI ↓	hold_rising to CP	-0.2294	-0.1458	-0.1453	-0.1453
TI ↑	hold_rising to CP	-0.0643	-0.0352	-0.0387	-0.0387
TI ↓	setup_rising to CP	0.2837	0.2146	0.2146	0.2146
TI ↑	setup_rising to CP	0.1005	0.0699	0.0699	0.0699

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	8.510e-06	3.323e-09
X8_P4	9.592e-06	3.085e-09
X17_P4	1.322e-05	3.442e-09
X33_P4	1.599e-05	3.680e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

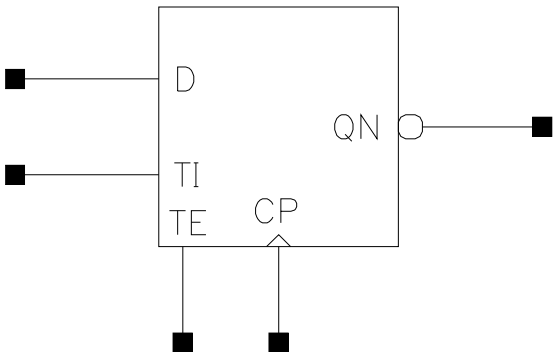
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.068e-03	3.100e-03	3.108e-03	3.112e-03
Clock 100Mhz Data 25Mhz	4.574e-03	4.651e-03	5.186e-03	5.664e-03
Clock 100Mhz Data 50Mhz	6.081e-03	6.201e-03	7.264e-03	8.217e-03
Clock = 0 Data 100Mhz	3.862e-03	3.651e-03	3.581e-03	3.546e-03
Clock = 1 Data 100Mhz	1.086e-03	5.639e-04	3.899e-04	3.029e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.536	4.2432
X8_P4	1.200	3.264	3.9168
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.1063	0.1108	5.4533	2.5067
CP to QN ↑	0.1072	0.0715	8.7849	4.0971
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0817	0.0895	1.1880	0.6273
CP to QN ↑	0.0702	0.0767	2.0541	1.0450

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1510	0.1615	0.1615	0.1615
CP ↑	min_pulse_width to CP	0.0637	0.0406	0.0406	0.0454
D ↓	hold_rising to CP	-0.1164	-0.0534	-0.0504	-0.0504
D ↑	hold_rising to CP	-0.0402	-0.0086	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1630	0.1100	0.1100	0.1100
D ↑	setup_rising to CP	0.0752	0.0387	0.0387	0.0387
TE ↓	hold_rising to CP	-0.0720	-0.0480	-0.0455	-0.0455
TE ↑	hold_rising to CP	-0.0548	-0.0361	-0.0361	-0.0361
TE ↓	setup_rising to CP	0.1392	0.1048	0.1048	0.1048
TE ↑	setup_rising to CP	0.2784	0.2195	0.2195	0.2195
TI ↓	hold_rising to CP	-0.2294	-0.1453	-0.1458	-0.1458
TI ↑	hold_rising to CP	-0.0658	-0.0347	-0.0352	-0.0352
TI ↓	setup_rising to CP	0.2843	0.2146	0.2146	0.2146
TI ↑	setup_rising to CP	0.1005	0.0699	0.0699	0.0699

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	8.636e-06	3.442e-09
X8_P4	9.698e-06	3.204e-09
X17_P4	1.311e-05	3.442e-09
X33_P4	1.587e-05	3.680e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

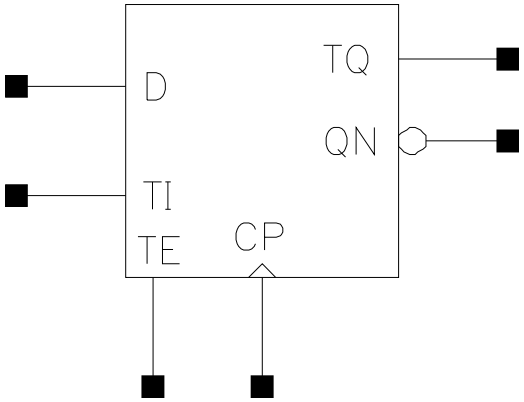
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.031e-03	3.081e-03	3.097e-03	3.105e-03
Clock 100Mhz Data 25Mhz	4.571e-03	4.718e-03	5.138e-03	5.625e-03
Clock 100Mhz Data 50Mhz	6.111e-03	6.356e-03	7.179e-03	8.145e-03
Clock = 0 Data 100Mhz	3.871e-03	3.654e-03	3.583e-03	3.547e-03
Clock = 1 Data 100Mhz	1.079e-03	5.622e-04	3.898e-04	3.037e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.536	4.2432
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0011	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.1178	0.0966	4.8738	2.4200
CP to QN ↑	0.1302	0.0744	8.6278	4.1076
CP to TQ ↓	0.0907	0.0501	6.9386	4.7077
CP to TQ ↑	0.0840	0.0674	17.4116	12.0489
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0900	0.0969	1.2153	0.6416
CP to QN ↑	0.0760	0.0811	2.0783	1.0647
CP to TQ ↓	0.0523	0.0546	6.3749	6.3941
CP to TQ ↑	0.0688	0.0707	16.0346	17.0584

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1552	0.1615	0.1615	0.1615
CP ↑	min_pulse_width to CP	0.0782	0.0406	0.0406	0.0454
D ↓	hold_rising to CP	-0.1133	-0.0511	-0.0511	-0.0511
D ↑	hold_rising to CP	-0.0405	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1630	0.1075	0.1075	0.1075
D ↑	setup_rising to CP	0.0752	0.0387	0.0387	0.0387
TE ↓	hold_rising to CP	-0.0694	-0.0455	-0.0455	-0.0455
TE ↑	hold_rising to CP	-0.0552	-0.0361	-0.0361	-0.0361
TE ↓	setup_rising to CP	0.1362	0.1048	0.1048	0.1048
TE ↑	setup_rising to CP	0.2784	0.2198	0.2198	0.2198
TI ↓	hold_rising to CP	-0.2296	-0.1458	-0.1458	-0.1419
TI ↑	hold_rising to CP	-0.0658	-0.0352	-0.0352	-0.0352
TI ↓	setup_rising to CP	0.2843	0.2148	0.2148	0.2146
TI ↑	setup_rising to CP	0.1005	0.0699	0.0699	0.0699

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	9.546e-06	3.688e-09
X8_P4	1.083e-05	3.442e-09
X17_P4	1.259e-05	3.561e-09
X33_P4	1.593e-05	3.799e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4

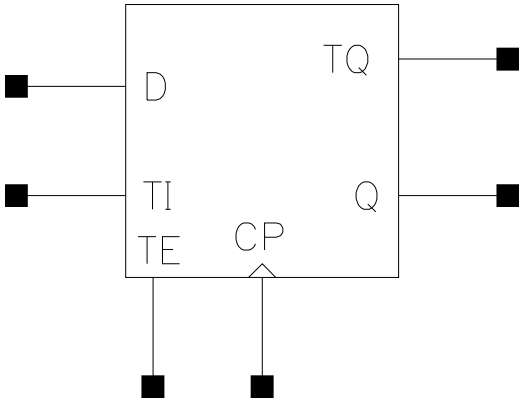
Clock 100Mhz Data 0Mhz	3.126e-03	3.128e-03	3.129e-03	3.130e-03
Clock 100Mhz Data 25Mhz	4.812e-03	4.947e-03	5.158e-03	5.737e-03
Clock 100Mhz Data 50Mhz	6.497e-03	6.767e-03	7.188e-03	8.344e-03
Clock = 0 Data 100Mhz	3.870e-03	3.658e-03	3.589e-03	3.554e-03
Clock = 1 Data 100Mhz	1.086e-03	5.636e-04	3.896e-04	3.027e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.400	4.0800
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006

TE	0.0009	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.1294	0.0606	5.8179	2.4955
CP to Q ↑	0.0931	0.0715	8.9970	4.1670
CP to TQ ↓	0.1253	0.0648	5.8011	6.5358
CP to TQ ↑	0.0962	0.0800	12.1421	17.3349
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0844	0.0919	1.2192	0.6400
CP to Q ↑	0.1225	0.1287	2.0928	1.0518
CP to TQ ↓	0.0884	0.0979	6.2018	6.3164
CP to TQ ↑	0.1305	0.1397	16.6454	16.8026

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1528	0.1615	0.1615	0.1615
CP ↑	min_pulse_width to CP	0.1120	0.0454	0.0407	0.0407
D ↓	hold_rising to CP	-0.1164	-0.0511	-0.0534	-0.0534
D ↑	hold_rising to CP	-0.0398	-0.0090	-0.0086	-0.0086
D ↓	setup_rising to CP	0.1630	0.1075	0.1100	0.1100
D ↑	setup_rising to CP	0.0752	0.0387	0.0387	0.0387
TE ↓	hold_rising to CP	-0.0720	-0.0455	-0.0480	-0.0480
TE ↑	hold_rising to CP	-0.0545	-0.0361	-0.0361	-0.0361
TE ↓	setup_rising to CP	0.1362	0.1048	0.1048	0.1048
TE ↑	setup_rising to CP	0.2762	0.2198	0.2195	0.2195
TI ↓	hold_rising to CP	-0.2296	-0.1404	-0.1453	-0.1453
TI ↑	hold_rising to CP	-0.0658	-0.0352	-0.0387	-0.0387
TI ↓	setup_rising to CP	0.2843	0.2146	0.2146	0.2146
TI ↑	setup_rising to CP	0.1005	0.0699	0.0699	0.0699

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	9.509e-06	3.561e-09
X8_P4	1.026e-05	3.323e-09
X17_P4	1.373e-05	3.561e-09
X33_P4	1.647e-05	3.799e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

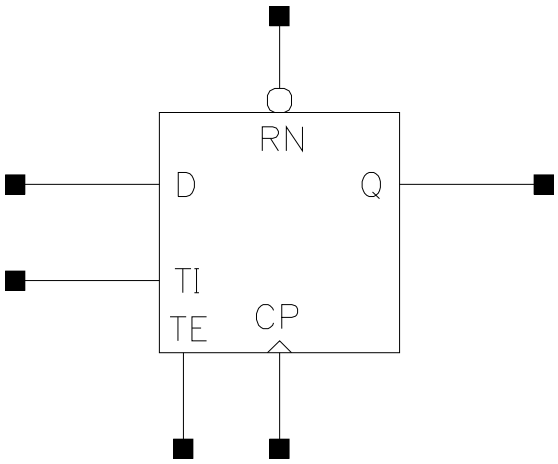
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.054e-03	3.090e-03	3.101e-03	3.106e-03
Clock 100Mhz Data 25Mhz	4.819e-03	4.818e-03	5.325e-03	5.846e-03
Clock 100Mhz Data 50Mhz	6.585e-03	6.545e-03	7.550e-03	8.586e-03
Clock = 0 Data 100Mhz	3.854e-03	3.646e-03	3.578e-03	3.544e-03
Clock = 1 Data 100Mhz	1.078e-03	5.597e-04	3.871e-04	3.008e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.672	4.4064
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
RN	0.0007	0.0006	0.0007	0.0007
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.1189	0.0579	5.9547	2.5058
CP to Q ↑	0.0894	0.0731	8.8750	4.1949
RN to Q ↓	0.0927	0.0786	4.9496	2.6435
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0866	0.0942	1.2041	0.6379
CP to Q ↑	0.1084	0.1140	2.0523	1.0461
RN to Q ↓	0.1208	0.1284	1.2006	0.6353

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1727	0.1674	0.1698	0.1698
CP ↑	min_pulse_width to CP	0.1024	0.0454	0.0406	0.0406
D ↓	hold_rising to CP	-0.1014	-0.0388	-0.0413	-0.0413
D ↑	hold_rising to CP	-0.0503	-0.0139	-0.0170	-0.0170
D ↓	setup_rising to CP	0.1630	0.1051	0.1047	0.1047
D ↑	setup_rising to CP	0.0850	0.0515	0.0541	0.0515
RN ↓	min_pulse_width to RN	0.0942	0.0996	0.0979	0.0979
RN ↑	recovery_rising to CP	0.0297	0.0290	0.0293	0.0293
RN ↑	removal_rising to CP	-0.0193	-0.0151	-0.0151	-0.0151
TE ↓	hold_rising to CP	-0.0770	-0.0364	-0.0360	-0.0360
TE ↑	hold_rising to CP	-0.0701	-0.0432	-0.0488	-0.0488
TE ↓	setup_rising to CP	0.1392	0.1027	0.1027	0.1027
TE ↑	setup_rising to CP	0.2762	0.2153	0.2153	0.2153
TI ↓	hold_rising to CP	-0.2100	-0.1214	-0.1223	-0.1223
TI ↑	hold_rising to CP	-0.0755	-0.0451	-0.0490	-0.0490
TI ↓	setup_rising to CP	0.2803	0.2043	0.2058	0.2058
TI ↑	setup_rising to CP	0.1152	0.0886	0.0901	0.0886

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	9.379e-06	3.799e-09
X8_P4	1.019e-05	3.561e-09
X17_P4	1.350e-05	3.918e-09
X33_P4	1.582e-05	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.425e-03	3.448e-03	3.473e-03	3.485e-03

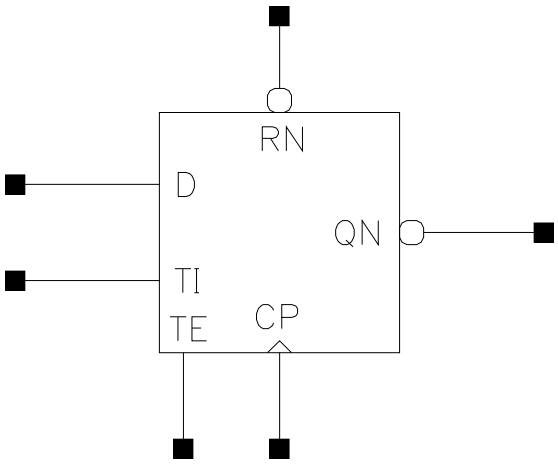
Clock 100Mhz Data 25Mhz	5.159e-03	5.133e-03	5.772e-03	6.287e-03
Clock 100Mhz Data 50Mhz	6.893e-03	6.818e-03	8.072e-03	9.088e-03
Clock = 0 Data 100Mhz	3.983e-03	3.706e-03	3.615e-03	3.570e-03
Clock = 1 Data 100Mhz	1.106e-03	5.785e-04	4.028e-04	3.150e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	3.944	4.7328
X33_P4	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.1014	0.0910	4.5911	2.3411
CP to QN ↑	0.1229	0.0698	8.6134	4.0670
RN to QN ↑	0.1062	0.1068	8.5913	4.0633
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0895	0.0975	1.2040	0.6367
CP to QN ↑	0.0774	0.0844	2.0671	1.0589
RN to QN ↑	0.1085	0.1182	2.0742	1.0603

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1727	0.1674	0.1693	0.1693
CP ↑	min_pulse_width to CP	0.0781	0.0406	0.0454	0.0502
D ↓	hold_rising to CP	-0.1036	-0.0388	-0.0357	-0.0357
D ↑	hold_rising to CP	-0.0503	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1630	0.1051	0.1051	0.1051
D ↑	setup_rising to CP	0.0850	0.0515	0.0515	0.0515
RN ↓	min_pulse_width to RN	0.0942	0.0952	0.1040	0.1111
RN ↑	recovery_rising to CP	0.0297	0.0346	0.0321	0.0346
RN ↑	removal_rising to CP	-0.0193	-0.0144	-0.0151	-0.0151
TE ↓	hold_rising to CP	-0.0770	-0.0364	-0.0364	-0.0364
TE ↑	hold_rising to CP	-0.0698	-0.0432	-0.0432	-0.0432
TE ↓	setup_rising to CP	0.1392	0.0999	0.1027	0.1027
TE ↑	setup_rising to CP	0.2762	0.2153	0.2153	0.2153
TI ↓	hold_rising to CP	-0.2098	-0.1208	-0.1214	-0.1214
TI ↑	hold_rising to CP	-0.0755	-0.0449	-0.0451	-0.0451
TI ↓	setup_rising to CP	0.2803	0.2048	0.2043	0.2043
TI ↑	setup_rising to CP	0.1150	0.0886	0.0886	0.0886

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	9.942e-06	3.844e-09
X8_P4	1.090e-05	3.680e-09
X17_P4	1.390e-05	3.799e-09
X33_P4	1.700e-05	4.037e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.394e-03	3.429e-03	3.440e-03	3.446e-03

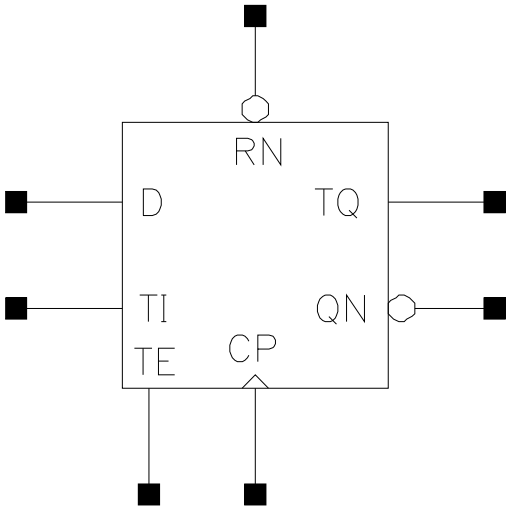
Clock 100Mhz Data 25Mhz	5.083e-03	5.149e-03	5.636e-03	6.124e-03
Clock 100Mhz Data 50Mhz	6.773e-03	6.868e-03	7.832e-03	8.802e-03
Clock = 0 Data 100Mhz	3.982e-03	3.705e-03	3.616e-03	3.572e-03
Clock = 1 Data 100Mhz	1.105e-03	5.751e-04	3.984e-04	3.102e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006

RN	0.0010	0.0006	0.0007	0.0008
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.1137	0.0944	4.6167	2.4635
CP to QN ↑	0.1613	0.0789	7.6645	4.2181
CP to TQ ↓	0.1142	0.0535	6.2772	4.8967
CP to TQ ↑	0.0938	0.0743	13.8502	12.7068
RN to QN ↑	0.1055	0.1049	7.7433	4.2123
RN to TQ ↓	0.0719	0.0707	5.4720	5.1654
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0968	0.1039	1.2243	0.6485
CP to QN ↑	0.0790	0.0830	2.1044	1.0601
CP to TQ ↓	0.0560	0.0581	6.1804	6.0645
CP to TQ ↑	0.0744	0.0762	11.8579	12.0406
RN to QN ↑	0.1072	0.1137	2.1037	1.0595
RN to TQ ↓	0.0759	0.0794	6.4557	6.3734

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1727	0.1674	0.1698	0.1698
CP ↑	min_pulse_width to CP	0.1120	0.0454	0.0454	0.0454
D ↓	hold_rising to CP	-0.1014	-0.0388	-0.0357	-0.0357
D ↑	hold_rising to CP	-0.0503	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1630	0.1051	0.1051	0.1051
D ↑	setup_rising to CP	0.0849	0.0515	0.0541	0.0541
RN ↓	min_pulse_width to RN	0.0991	0.1018	0.1018	0.1067
RN ↑	recovery_rising to CP	0.0314	0.0290	0.0321	0.0321
RN ↑	removal_rising to CP	-0.0249	-0.0151	-0.0151	-0.0151
TE ↓	hold_rising to CP	-0.0770	-0.0364	-0.0364	-0.0339
TE ↑	hold_rising to CP	-0.0698	-0.0432	-0.0463	-0.0463
TE ↓	setup_rising to CP	0.1392	0.0999	0.1027	0.1027
TE ↑	setup_rising to CP	0.2762	0.2153	0.2153	0.2153
TI ↓	hold_rising to CP	-0.2100	-0.1214	-0.1214	-0.1214
TI ↑	hold_rising to CP	-0.0755	-0.0451	-0.0449	-0.0449
TI ↓	setup_rising to CP	0.2843	0.2043	0.2043	0.2043
TI ↑	setup_rising to CP	0.1150	0.0886	0.0901	0.0901

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	1.050e-05	3.918e-09
X8_P4	1.144e-05	3.680e-09
X17_P4	1.365e-05	3.918e-09
X33_P4	1.722e-05	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

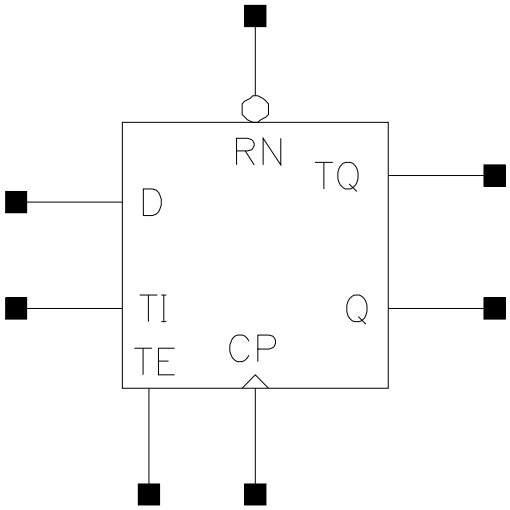
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.394e-03	3.431e-03	3.461e-03	3.477e-03
Clock 100Mhz Data 25Mhz	5.262e-03	5.283e-03	5.555e-03	6.162e-03
Clock 100Mhz Data 50Mhz	7.130e-03	7.135e-03	7.650e-03	8.848e-03
Clock = 0 Data 100Mhz	3.978e-03	3.703e-03	3.609e-03	3.562e-03
Clock = 1 Data 100Mhz	1.105e-03	5.780e-04	4.024e-04	3.147e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006

RN	0.0008	0.0008	0.0007	0.0007
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.1340	0.0629	6.3133	2.5780
CP to Q ↑	0.0955	0.0761	9.2021	4.3229
CP to TQ ↓	0.1290	0.0646	7.9266	6.5908
CP to TQ ↑	0.1000	0.0812	19.1136	17.2229
RN to Q ↓	0.0960	0.0890	5.1981	2.7382
RN to TQ ↓	0.0948	0.0907	6.7236	6.9024
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0889	0.0972	1.2194	0.6457
CP to Q ↑	0.1087	0.1149	2.0617	1.0497
CP to TQ ↓	0.0928	0.1042	6.2444	6.3438
CP to TQ ↑	0.1160	0.1264	16.8112	16.8873
RN to Q ↓	0.1232	0.1315	1.2165	0.6443
RN to TQ ↓	0.1271	0.1385	6.2406	6.3441

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1721	0.1674	0.1674	0.1668
CP ↑	min_pulse_width to CP	0.1180	0.0491	0.0406	0.0406
D ↓	hold_rising to CP	-0.1014	-0.0357	-0.0388	-0.0388
D ↑	hold_rising to CP	-0.0503	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1633	0.1051	0.1051	0.1051
D ↑	setup_rising to CP	0.0850	0.0515	0.0515	0.0515
RN ↓	min_pulse_width to RN	0.0991	0.1116	0.0952	0.0952
RN ↑	recovery_rising to CP	0.0297	0.0346	0.0290	0.0290
RN ↑	removal_rising to CP	-0.0197	-0.0148	-0.0151	-0.0151
TE ↓	hold_rising to CP	-0.0748	-0.0339	-0.0364	-0.0360
TE ↑	hold_rising to CP	-0.0698	-0.0432	-0.0432	-0.0432
TE ↓	setup_rising to CP	0.1362	0.0999	0.1027	0.1030
TE ↑	setup_rising to CP	0.2735	0.2153	0.2153	0.2153
TI ↓	hold_rising to CP	-0.2059	-0.1214	-0.1208	-0.1208
TI ↑	hold_rising to CP	-0.0755	-0.0436	-0.0449	-0.0449
TI ↓	setup_rising to CP	0.2793	0.2043	0.2043	0.2043
TI ↑	setup_rising to CP	0.1152	0.0886	0.0886	0.0886

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	9.742e-06	3.918e-09
X8_P4	1.059e-05	3.680e-09
X17_P4	1.371e-05	3.918e-09
X33_P4	1.604e-05	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

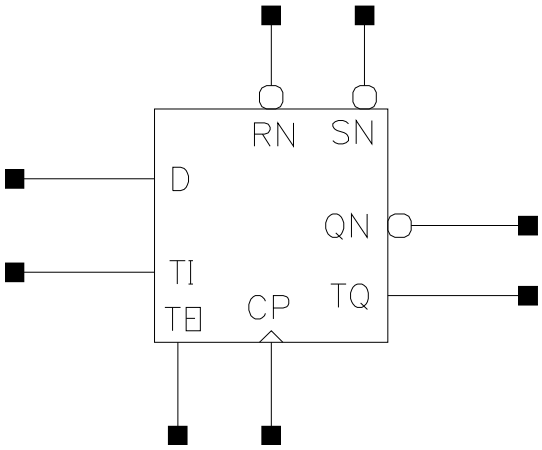
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.419e-03	3.444e-03	3.452e-03	3.455e-03
Clock 100Mhz Data 25Mhz	5.269e-03	5.247e-03	5.865e-03	6.414e-03
Clock 100Mhz Data 50Mhz	7.118e-03	7.050e-03	8.279e-03	9.374e-03
Clock = 0 Data 100Mhz	3.981e-03	3.706e-03	3.614e-03	3.568e-03
Clock = 1 Data 100Mhz	1.106e-03	5.754e-04	3.987e-04	3.104e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.352	5.2224
X17_P4	1.200	4.488	5.3856
X33_P4	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008
D	0.0005	0.0005	0.0005
RN	0.0007	0.0007	0.0007

SN	0.0012	0.0012	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
CP to QN ↓	0.1047	0.1108	2.3876	1.2384
CP to QN ↑	0.0837	0.0871	4.0895	2.0684
CP to TQ ↓	0.0637	0.0637	7.9131	7.9214
CP to TQ ↑	0.0877	0.0877	22.7301	22.7607
RN to QN ↓	0.1171	0.1230	2.3873	1.2393
RN to QN ↑	0.1191	0.1245	4.1031	2.0776
RN to TQ ↓	0.0902	0.0899	8.5785	8.5838
RN to TQ ↑	0.1003	0.1004	22.6770	22.7116
SN to QN ↓	0.1262	0.1335	2.4032	1.2438
SN to TQ ↑	0.1070	0.1068	22.9632	22.9605
	X33_P4		X33_P4	
CP to QN ↓	0.1257		0.6639	
CP to QN ↑	0.0960		1.0600	
CP to TQ ↓	0.0638		7.9236	
CP to TQ ↑	0.0880		22.7471	
RN to QN ↓	0.1376		0.6645	
RN to QN ↑	0.1369		1.0614	
RN to TQ ↓	0.0899		8.6008	
RN to TQ ↑	0.1007		22.7541	
SN to QN ↓	0.1504		0.6659	
SN to TQ ↑	0.1070		23.0367	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1765	0.1765	0.1765
CP ↑	min_pulse_width to CP	0.0502	0.0502	0.0540
D ↓	hold_rising to CP	-0.0388	-0.0388	-0.0388
D ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1096	0.1096	0.1096
D ↑	setup_rising to CP	0.0567	0.0567	0.0567
RN ↓	min_pulse_width to RN	0.1089	0.1138	0.1213
RN ↑	non_seq_hold_rising to SN	-0.0430	-0.0430	-0.0430
RN ↑	non_seq_setup_rising to SN	0.1008	0.1008	0.1008
RN ↑	recovery_rising to CP	0.0491	0.0461	0.0461
RN ↑	removal_rising to CP	-0.0267	-0.0267	-0.0267
SN ↓	min_pulse_width to SN	0.0913	0.0940	0.0989
SN ↑	recovery_rising to CP	0.0177	0.0177	0.0177
SN ↑	removal_rising to CP	0.0432	0.0432	0.0432

TE ↓	hold_rising to CP	-0.0364	-0.0364	-0.0364
TE ↑	hold_rising to CP	-0.0432	-0.0432	-0.0432
TE ↓	setup_rising to CP	0.1101	0.1101	0.1101
TE ↑	setup_rising to CP	0.2195	0.2195	0.2195
TI ↓	hold_rising to CP	-0.1214	-0.1214	-0.1214
TI ↑	hold_rising to CP	-0.0451	-0.0451	-0.0436
TI ↓	setup_rising to CP	0.2146	0.2146	0.2146
TI ↑	setup_rising to CP	0.0935	0.0935	0.0935

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	1.250e-05	4.169e-09
X17_P4	1.424e-05	4.288e-09
X33_P4	1.724e-05	4.527e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

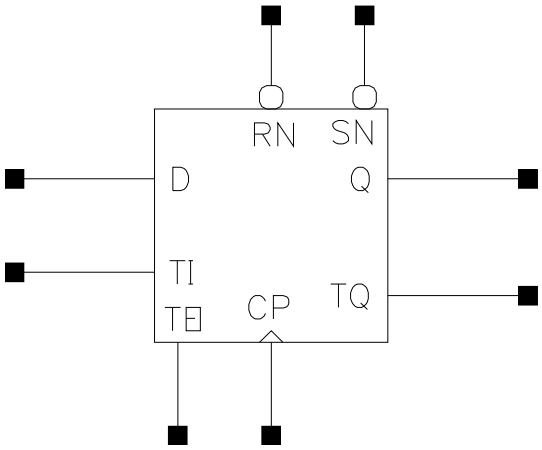
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.663e-03	3.663e-03	3.664e-03
Clock 100Mhz Data 25Mhz	5.558e-03	5.789e-03	6.382e-03
Clock 100Mhz Data 50Mhz	7.453e-03	7.915e-03	9.101e-03
Clock = 0 Data 100Mhz	3.578e-03	3.577e-03	3.577e-03
Clock = 1 Data 100Mhz	5.243e-05	5.246e-05	5.252e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.216	5.0592
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008
D	0.0005	0.0005	0.0005
RN	0.0007	0.0007	0.0007

SN	0.0012	0.0012	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
CP to Q ↓	0.0692	0.0770	2.5101	1.3128
CP to Q ↑	0.0835	0.0871	4.1888	2.1322
CP to TQ ↓	0.0731	0.0838	8.0391	8.1360
CP to TQ ↑	0.0939	0.1029	22.3082	22.4419
RN to Q ↓	0.1018	0.1171	2.9115	1.5291
RN to Q ↑	0.0768	0.0853	4.3561	2.2294
RN to TQ ↓	0.1062	0.1246	8.8245	9.0419
RN to TQ ↑	0.0942	0.1115	22.5309	22.6836
SN to Q ↑	0.1037	0.1120	4.3548	2.2325
SN to TQ ↑	0.1210	0.1382	22.5279	22.6859
	X33_P4		X33_P4	
CP to Q ↓	0.0971		0.7147	
CP to Q ↑	0.0980		1.1062	
CP to TQ ↓	0.1030		8.4259	
CP to TQ ↑	0.1199		22.6588	
RN to Q ↓	0.1546		0.8515	
RN to Q ↑	0.1076		1.1714	
RN to TQ ↓	0.1571		9.6228	
RN to TQ ↑	0.1450		22.9562	
SN to Q ↑	0.1341		1.1717	
SN to TQ ↑	0.1715		22.9675	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1746	0.1746	0.1747
CP ↑	min_pulse_width to CP	0.0539	0.0636	0.0830
D ↓	hold_rising to CP	-0.0357	-0.0361	-0.0364
D ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1096	0.1096	0.1096
D ↑	setup_rising to CP	0.0567	0.0567	0.0564
RN ↓	min_pulse_width to RN	0.1213	0.1431	0.1848
RN ↑	non_seq_hold_rising to SN	-0.0479	-0.0579	-0.0746
RN ↑	non_seq_setup_rising to SN	0.0960	0.0960	0.1214
RN ↑	recovery_rising to CP	0.0418	0.0418	0.0418
RN ↑	removal_rising to CP	-0.0193	-0.0193	-0.0193
SN ↓	min_pulse_width to SN	0.0989	0.1135	0.1428
SN ↑	recovery_rising to CP	0.0177	0.0177	0.0177
SN ↑	removal_rising to CP	0.0432	0.0432	0.0432

TE ↓	hold_rising to CP	-0.0339	-0.0339	-0.0339
TE ↑	hold_rising to CP	-0.0432	-0.0432	-0.0432
TE ↓	setup_rising to CP	0.1101	0.1101	0.1101
TE ↑	setup_rising to CP	0.2198	0.2195	0.2195
TI ↓	hold_rising to CP	-0.1215	-0.1160	-0.1160
TI ↑	hold_rising to CP	-0.0436	-0.0436	-0.0436
TI ↓	setup_rising to CP	0.2146	0.2146	0.2146
TI ↑	setup_rising to CP	0.0935	0.0935	0.0935

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P4	1.198e-05	4.046e-09
X17_P4	1.342e-05	4.165e-09
X33_P4	1.596e-05	4.403e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

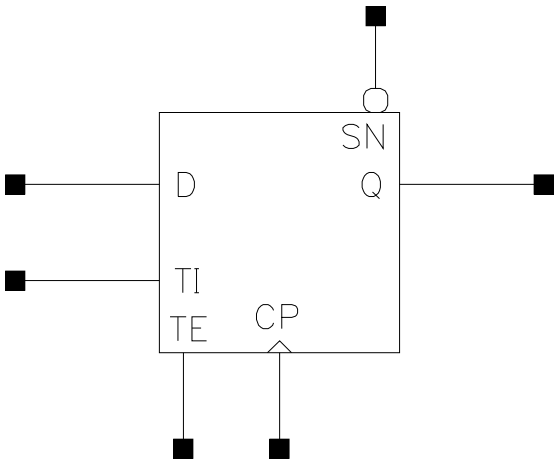
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.645e-03	3.645e-03	3.646e-03
Clock 100Mhz Data 25Mhz	5.456e-03	5.724e-03	6.414e-03
Clock 100Mhz Data 50Mhz	7.267e-03	7.803e-03	9.183e-03
Clock = 0 Data 100Mhz	3.576e-03	3.577e-03	3.576e-03
Clock = 1 Data 100Mhz	5.223e-05	5.231e-05	5.240e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004
SN	0.0013	0.0012	0.0013	0.0013
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0008			
D	0.0004			
SN	0.0012			
TE	0.0009			
TI	0.0004			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.1200	0.0607	5.9729	2.4926
CP to Q ↑	0.0943	0.0767	8.9594	4.1664
SN to Q ↑	0.0712	0.0805	8.7167	4.1788
	X17_P4	X25_P4	X17_P4	X25_P4
CP to Q ↓	0.0855	0.0897	1.2032	0.8351
CP to Q ↑	0.1088	0.1120	2.0491	1.3896
SN to Q ↑	0.1128	0.1160	2.0521	1.3910
	X33_P4		X33_P4	
CP to Q ↓	0.0932		0.6379	
CP to Q ↑	0.1144		1.0454	
SN to Q ↑	0.1183		1.0466	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.1770	0.1783	0.1783	0.1783
CP ↑	min_pulse_width to CP	0.1061	0.0455	0.0406	0.0406
D ↓	hold_rising to CP	-0.1066	-0.0437	-0.0462	-0.0462
D ↑	hold_rising to CP	-0.0451	-0.0117	-0.0117	-0.0117
D ↓	setup_rising to CP	0.1679	0.1123	0.1123	0.1123
D ↑	setup_rising to CP	0.0801	0.0439	0.0439	0.0439
SN ↓	min_pulse_width to SN	0.0637	0.0735	0.0713	0.0713
SN ↑	recovery_rising to CP	0.0155	0.0177	0.0177	0.0177
SN ↑	removal_rising to CP	0.0339	0.0433	0.0433	0.0433
TE ↓	hold_rising to CP	-0.0770	-0.0413	-0.0409	-0.0409
TE ↑	hold_rising to CP	-0.0650	-0.0383	-0.0414	-0.0414
TE ↓	setup_rising to CP	0.1441	0.1097	0.1097	0.1097
TE ↑	setup_rising to CP	0.2814	0.2250	0.2250	0.2250
TI ↓	hold_rising to CP	-0.2098	-0.1311	-0.1306	-0.1306
TI ↑	hold_rising to CP	-0.0707	-0.0401	-0.0401	-0.0401
TI ↓	setup_rising to CP	0.2852	0.2156	0.2156	0.2156
TI ↑	setup_rising to CP	0.1103	0.0788	0.0788	0.0788
		X33_P4			

CP ↓	min_pulse_width to CP	0.1784			
CP ↑	min_pulse_width to CP	0.0407			
D ↓	hold_rising to CP	-0.0462			
D ↑	hold_rising to CP	-0.0117			
D ↓	setup_rising to CP	0.1149			
D ↑	setup_rising to CP	0.0439			
SN ↓	min_pulse_width to SN	0.0713			
SN ↑	recovery_rising to CP	0.0177			
SN ↑	removal_rising to CP	0.0433			
TE ↓	hold_rising to CP	-0.0409			
TE ↑	hold_rising to CP	-0.0414			
TE ↓	setup_rising to CP	0.1097			
TE ↑	setup_rising to CP	0.2250			
TI ↓	hold_rising to CP	-0.1306			
TI ↑	hold_rising to CP	-0.0401			
TI ↓	setup_rising to CP	0.2156			
TI ↑	setup_rising to CP	0.0788			

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	9.915e-06	3.799e-09
X8_P4	1.097e-05	3.680e-09
X17_P4	1.399e-05	3.918e-09
X25_P4	1.555e-05	4.038e-09
X33_P4	1.710e-05	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	3.319e-03	3.406e-03	3.434e-03	3.449e-03
Clock 100Mhz Data 25Mhz	5.041e-03	5.144e-03	5.727e-03	6.011e-03
Clock 100Mhz Data 50Mhz	6.764e-03	6.883e-03	8.019e-03	8.574e-03
Clock = 0 Data 100Mhz	3.854e-03	3.654e-03	3.588e-03	3.555e-03
Clock = 1 Data 100Mhz	1.106e-03	5.754e-04	3.986e-04	3.103e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	3.457e-03			

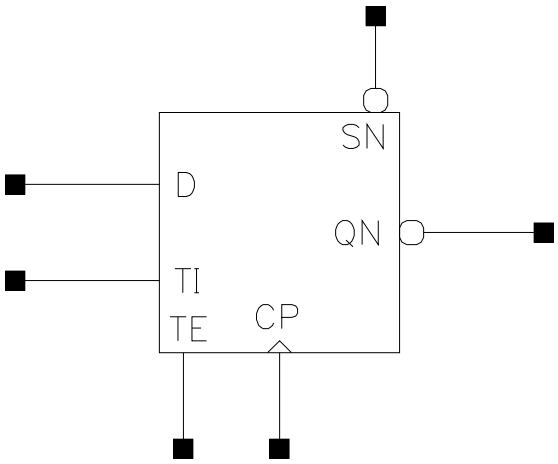
Clock 100Mhz Data 25Mhz	6.254e-03			
Clock 100Mhz Data 50Mhz	9.050e-03			
Clock = 0 Data 100Mhz	3.535e-03			
Clock = 1 Data 100Mhz	2.573e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004
SN	0.0013	0.0012	0.0013	0.0013
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0008			
D	0.0004			
SN	0.0013			
TE	0.0009			
TI	0.0004			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.1067	0.0921	4.5953	2.3454
CP to QN ↑	0.1247	0.0699	8.6040	4.0831
SN to QN ↓	0.0854	0.0958	4.5788	2.3460
	X17_P4	X25_P4	X17_P4	X25_P4
CP to QN ↓	0.0956	0.1006	1.2086	0.8398
CP to QN ↑	0.0831	0.0876	2.0558	1.3942
SN to QN ↓	0.1011	0.1062	1.2107	0.8389
	X33_P4		X33_P4	
CP to QN ↓	0.1045		0.6403	
CP to QN ↑	0.0906		1.0486	
SN to QN ↓	0.1101		0.6398	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.1770	0.1783	0.1789	0.1789
CP ↑	min_pulse_width to CP	0.0782	0.0406	0.0502	0.0502
D ↓	hold_rising to CP	-0.1066	-0.0462	-0.0406	-0.0406
D ↑	hold_rising to CP	-0.0451	-0.0117	-0.0117	-0.0117
D ↓	setup_rising to CP	0.1679	0.1149	0.1149	0.1149
D ↑	setup_rising to CP	0.0801	0.0439	0.0439	0.0439
SN ↓	min_pulse_width to SN	0.0615	0.0713	0.0762	0.0789
SN ↑	recovery_rising to CP	0.0155	0.0177	0.0177	0.0177
SN ↑	removal_rising to CP	0.0339	0.0433	0.0433	0.0433
TE ↓	hold_rising to CP	-0.0770	-0.0409	-0.0413	-0.0413
TE ↑	hold_rising to CP	-0.0650	-0.0383	-0.0383	-0.0383
TE ↓	setup_rising to CP	0.1411	0.1097	0.1097	0.1097
TE ↑	setup_rising to CP	0.2784	0.2250	0.2250	0.2250
TI ↓	hold_rising to CP	-0.2113	-0.1306	-0.1311	-0.1313
TI ↑	hold_rising to CP	-0.0705	-0.0401	-0.0386	-0.0386
TI ↓	setup_rising to CP	0.2842	0.2156	0.2197	0.2197
TI ↑	setup_rising to CP	0.1103	0.0788	0.0788	0.0788
		X33_P4			

CP ↓	min_pulse_width to CP	0.1784			
CP ↑	min_pulse_width to CP	0.0540			
D ↓	hold_rising to CP	-0.0406			
D ↑	hold_rising to CP	-0.0117			
D ↓	setup_rising to CP	0.1149			
D ↑	setup_rising to CP	0.0439			
SN ↓	min_pulse_width to SN	0.0811			
SN ↑	recovery_rising to CP	0.0177			
SN ↑	removal_rising to CP	0.0433			
TE ↓	hold_rising to CP	-0.0413			
TE ↑	hold_rising to CP	-0.0383			
TE ↓	setup_rising to CP	0.1097			
TE ↑	setup_rising to CP	0.2250			
TI ↓	hold_rising to CP	-0.1311			
TI ↑	hold_rising to CP	-0.0386			
TI ↓	setup_rising to CP	0.2197			
TI ↑	setup_rising to CP	0.0788			

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	9.492e-06	3.799e-09
X8_P4	1.027e-05	3.680e-09
X17_P4	1.345e-05	3.918e-09
X25_P4	1.460e-05	4.038e-09
X33_P4	1.577e-05	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	3.318e-03	3.408e-03	3.435e-03	3.448e-03
Clock 100Mhz Data 25Mhz	4.977e-03	5.124e-03	5.718e-03	6.001e-03
Clock 100Mhz Data 50Mhz	6.635e-03	6.840e-03	8.001e-03	8.554e-03
Clock = 0 Data 100Mhz	3.854e-03	3.657e-03	3.590e-03	3.556e-03
Clock = 1 Data 100Mhz	1.106e-03	5.755e-04	3.987e-04	3.103e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	3.456e-03			

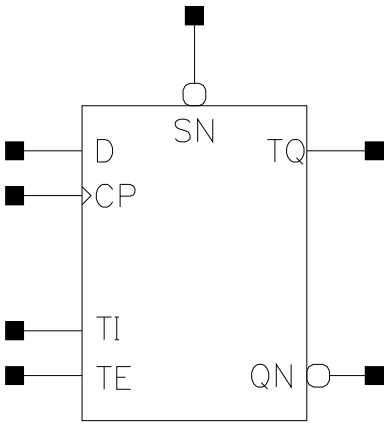
Clock 100Mhz Data 25Mhz	6.229e-03			
Clock 100Mhz Data 50Mhz	9.002e-03			
Clock = 0 Data 100Mhz	3.536e-03			
Clock = 1 Data 100Mhz	2.573e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.216	5.0592
X8_P4	1.200	4.080	4.8960
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004

SN	0.0014	0.0015	0.0014	0.0015
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.1233	0.0969	4.5881	2.3538
CP to QN ↑	0.1626	0.0794	8.4866	4.1495
CP to TQ ↓	0.1166	0.0548	7.1264	5.7417
CP to TQ ↑	0.0946	0.0733	12.1277	11.8133
SN to QN ↓	0.0805	0.0829	4.5765	2.3517
SN to TQ ↑	0.0560	0.0582	11.9023	11.8486
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0961	0.1055	1.2351	0.6332
CP to QN ↑	0.0893	0.0978	2.0674	1.0524
CP to TQ ↓	0.0683	0.0681	5.9861	5.9866
CP to TQ ↑	0.0821	0.0821	11.8783	11.9023
SN to QN ↓	0.0833	0.0927	1.2365	0.6335
SN to TQ ↑	0.0687	0.0686	11.8758	11.9078

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1770	0.1789	0.1789	0.1789
CP ↑	min_pulse_width to CP	0.1120	0.0454	0.0540	0.0588
D ↓	hold_rising to CP	-0.1036	-0.0437	-0.0406	-0.0406
D ↑	hold_rising to CP	-0.0451	-0.0117	-0.0117	-0.0117
D ↓	setup_rising to CP	0.1679	0.1149	0.1149	0.1149
D ↑	setup_rising to CP	0.0826	0.0439	0.0439	0.0439
SN ↓	min_pulse_width to SN	0.0566	0.0588	0.0593	0.0620
SN ↑	recovery_rising to CP	0.0180	0.0177	0.0177	0.0177
SN ↑	removal_rising to CP	0.0339	0.0433	0.0433	0.0433
TE ↓	hold_rising to CP	-0.0770	-0.0413	-0.0413	-0.0413
TE ↑	hold_rising to CP	-0.0650	-0.0383	-0.0383	-0.0383
TE ↓	setup_rising to CP	0.1441	0.1097	0.1097	0.1097
TE ↑	setup_rising to CP	0.2814	0.2250	0.2246	0.2250
TI ↓	hold_rising to CP	-0.2098	-0.1311	-0.1311	-0.1313
TI ↑	hold_rising to CP	-0.0707	-0.0401	-0.0386	-0.0386
TI ↓	setup_rising to CP	0.2852	0.2197	0.2197	0.2197
TI ↑	setup_rising to CP	0.1101	0.0788	0.0788	0.0788

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	1.069e-05	4.038e-09
X8_P4	1.146e-05	3.918e-09
X17_P4	1.464e-05	4.157e-09
X33_P4	1.695e-05	4.395e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

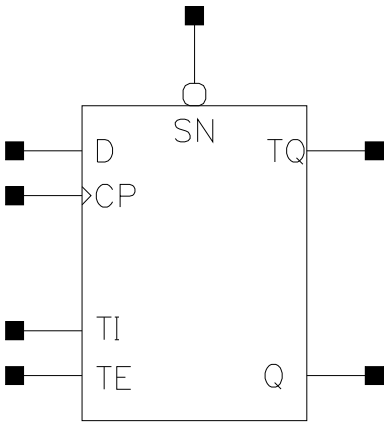
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.322e-03	3.411e-03	3.441e-03	3.456e-03
Clock 100Mhz Data 25Mhz	5.226e-03	5.314e-03	5.840e-03	6.365e-03
Clock 100Mhz Data 50Mhz	7.129e-03	7.217e-03	8.239e-03	9.274e-03
Clock = 0 Data 100Mhz	3.864e-03	3.663e-03	3.597e-03	3.563e-03
Clock = 1 Data 100Mhz	1.106e-03	5.757e-04	3.988e-04	3.105e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.944	4.7328
X17_P4	1.200	4.216	5.0592
X33_P4	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004

SN	0.0014	0.0013	0.0013	0.0013
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.1372	0.0651	6.1666	2.5516
CP to Q ↑	0.1005	0.0793	9.0187	4.2187
CP to TQ ↓	0.1378	0.0695	9.0047	6.6310
CP to TQ ↑	0.0994	0.0889	12.2222	17.4003
SN to Q ↑	0.0593	0.0837	8.7458	4.2269
SN to TQ ↑	0.0583	0.0949	11.9351	17.3815
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0872	0.0950	1.2368	0.6502
CP to Q ↑	0.1101	0.1158	2.0620	1.0496
CP to TQ ↓	0.0911	0.1022	6.2456	6.3377
CP to TQ ↑	0.1176	0.1272	16.8192	16.8967
SN to Q ↑	0.1139	0.1196	2.0618	1.0510
SN to TQ ↑	0.1215	0.1310	16.8168	16.8912

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1770	0.1783	0.1783	0.1784
CP ↑	min_pulse_width to CP	0.1217	0.0491	0.0406	0.0407
D ↓	hold_rising to CP	-0.1036	-0.0406	-0.0462	-0.0462
D ↑	hold_rising to CP	-0.0476	-0.0117	-0.0117	-0.0117
D ↓	setup_rising to CP	0.1657	0.1123	0.1149	0.1123
D ↑	setup_rising to CP	0.0826	0.0439	0.0439	0.0439
SN ↓	min_pulse_width to SN	0.0540	0.0811	0.0713	0.0713
SN ↑	recovery_rising to CP	0.0155	0.0177	0.0177	0.0177
SN ↑	removal_rising to CP	0.0339	0.0433	0.0433	0.0433
TE ↓	hold_rising to CP	-0.0770	-0.0388	-0.0409	-0.0409
TE ↑	hold_rising to CP	-0.0650	-0.0383	-0.0414	-0.0414
TE ↓	setup_rising to CP	0.1411	0.1097	0.1097	0.1097
TE ↑	setup_rising to CP	0.2787	0.2250	0.2250	0.2250
TI ↓	hold_rising to CP	-0.2098	-0.1272	-0.1306	-0.1306
TI ↑	hold_rising to CP	-0.0755	-0.0401	-0.0401	-0.0401
TI ↓	setup_rising to CP	0.2843	0.2156	0.2156	0.2156
TI ↑	setup_rising to CP	0.1101	0.0788	0.0788	0.0748

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	1.070e-05	3.918e-09
X8_P4	1.161e-05	3.799e-09
X17_P4	1.462e-05	4.038e-09
X33_P4	1.771e-05	4.276e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

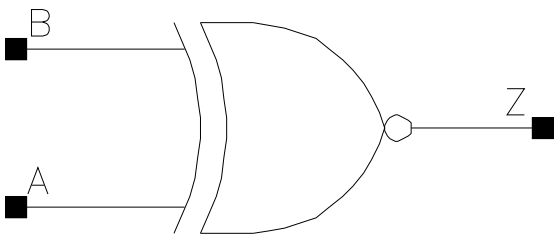
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.319e-03	3.406e-03	3.435e-03	3.449e-03
Clock 100Mhz Data 25Mhz	5.185e-03	5.280e-03	5.870e-03	6.420e-03
Clock 100Mhz Data 50Mhz	7.052e-03	7.155e-03	8.305e-03	9.390e-03
Clock = 0 Data 100Mhz	3.865e-03	3.659e-03	3.591e-03	3.557e-03
Clock = 1 Data 100Mhz	1.106e-03	5.757e-04	3.989e-04	3.105e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P4	X8_P4	X17_P4	X25_P4
A	0.0015	0.0006	0.0008	0.0013
B	0.0014	0.0013	0.0017	0.0022
	X33_P4			
A	0.0015			
B	0.0026			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X8_P4**	**X6_P4**	**X8_P4**
A to Z ↓	0.0273	0.0649	4.6511	2.5571
A to Z ↑	0.0301	0.0569	6.8723	4.3065
B to Z ↓	0.0260	0.0446	4.6445	2.5412
B to Z ↑	0.0295	0.0413	6.8823	4.2924
	X17_P4	**X25_P4**	**X17_P4**	**X25_P4**
A to Z ↓	0.0609	0.0607	1.2643	0.8699
A to Z ↑	0.0515	0.0518	2.1064	1.4024

B to Z ↓	0.0458	0.0444	1.2606	0.8684
B to Z ↑	0.0405	0.0392	2.1031	1.3991
	X33_P4		**X33_P4**	
A to Z ↓	0.0568		0.6539	
A to Z ↑	0.0497		1.0534	
B to Z ↓	0.0424		0.6527	
B to Z ↑	0.0385		1.0518	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P4	4.456e-06	1.179e-09
X8_P4	6.587e-06	1.536e-09
X17_P4	9.960e-06	1.655e-09
X25_P4	1.585e-05	2.370e-09
X33_P4	2.033e-05	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	2.068e-03	3.809e-03	5.324e-03	8.488e-03
B to Z	1.971e-03	2.595e-03	3.945e-03	6.145e-03
	X33_P4			
A to Z	1.028e-02			
B to Z	7.680e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

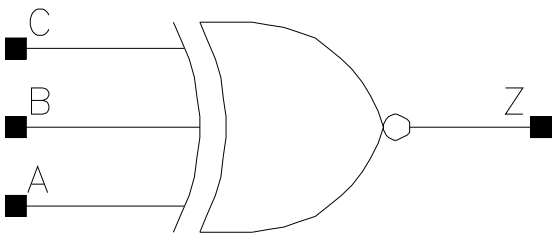
Pin Cycle (vdds)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	2.192e-07	-1.888e-07	-2.508e-07	-3.848e-07
B to Z	6.004e-06	-3.757e-08	-3.006e-07	-4.424e-07
	X33_P4			
A to Z	-1.562e-07			
B to Z	-4.671e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	2.176	2.6112
X16_P4	1.200	2.720	3.2640
X25_P4	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X16_P4	X25_P4
A	0.0025	0.0021	0.0027	0.0039
B	0.0029	0.0020	0.0027	0.0036
C	0.0018	0.0006	0.0006	0.0007

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0455	0.0781	5.5939	2.7204
A to Z ↑	0.0436	0.0707	10.2742	4.2690
B to Z ↓	0.0461	0.0777	5.5930	2.7201
B to Z ↑	0.0435	0.0705	10.2669	4.2697
C to Z ↓	0.0447	0.1006	5.5953	2.7188
C to Z ↑	0.0416	0.0927	10.2680	4.2713
	X16_P4	**X25_P4**	**X16_P4**	**X25_P4**
A to Z ↓	0.0773	0.0773	1.3989	0.8946
A to Z ↑	0.0753	0.0749	2.2386	1.4081
B to Z ↓	0.0773	0.0785	1.3984	0.8946

B to Z ↑	0.0752	0.0763	2.2381	1.4082
C to Z ↓	0.1046	0.1109	1.3977	0.8943
C to Z ↑	0.1013	0.1081	2.2391	1.4087

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	4.595e-06	2.132e-09
X8_P4	5.395e-06	2.251e-09
X16_P4	8.699e-06	2.727e-09
X25_P4	1.224e-05	3.799e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	2.218e-03	2.973e-03	4.772e-03	7.206e-03
B to Z	2.148e-03	2.909e-03	4.710e-03	7.186e-03
C to Z	2.074e-03	4.446e-03	6.548e-03	9.894e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

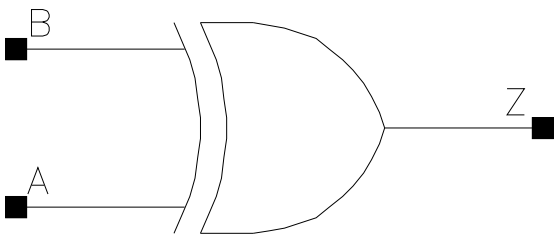
Pin Cycle (vdds)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	-1.727e-06	-9.975e-07	-1.162e-06	-1.604e-06
B to Z	2.065e-05	8.343e-06	1.304e-05	2.005e-05
C to Z	3.373e-05	1.644e-05	2.299e-05	3.394e-05

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.224	1.4688
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.224	1.4688
X16_P4	1.200	1.360	1.6320
X25_P4	1.200	2.176	2.6112
X31_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X16_P4
A	0.0007	0.0014	0.0009	0.0010
B	0.0011	0.0013	0.0013	0.0015
	X25_P4	X31_P4		
A	0.0013	0.0017		
B	0.0023	0.0030		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0583	0.0292	4.6742	3.5231
A to Z ↑	0.0534	0.0303	8.3460	9.1283
B to Z ↓	0.0414	0.0287	4.6572	3.5415
B to Z ↑	0.0408	0.0288	8.3454	9.1148
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0513	0.0530	2.4849	1.2883

A to Z ↑	0.0452	0.0471	4.1927	2.1150
B to Z ↓	0.0397	0.0404	2.4780	1.2872
B to Z ↑	0.0368	0.0382	4.1940	2.1100
	X25_P4	**X31_P4**	**X25_P4**	**X31_P4**
A to Z ↓	0.0572	0.0531	0.8621	0.6950
A to Z ↑	0.0505	0.0474	1.4006	1.1276
B to Z ↓	0.0430	0.0401	0.8615	0.6945
B to Z ↑	0.0383	0.0361	1.3987	1.1268

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	5.489e-06	1.417e-09
X6_P4	4.741e-06	1.179e-09
X8_P4	8.006e-06	1.417e-09
X16_P4	1.097e-05	1.536e-09
X25_P4	1.552e-05	2.251e-09
X31_P4	1.988e-05	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	2.896e-03	2.041e-03	3.436e-03	4.890e-03
B to Z	2.197e-03	1.910e-03	2.800e-03	4.017e-03
	X25_P4	X31_P4		
A to Z	7.726e-03	9.403e-03		
B to Z	5.416e-03	6.546e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

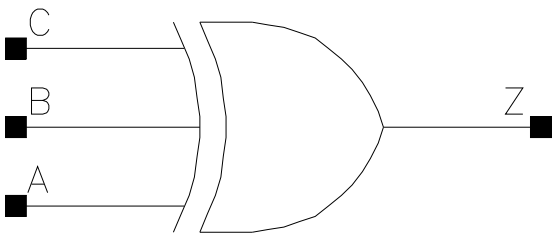
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	-1.918e-07	-5.225e-08	-2.261e-07	-1.674e-07
B to Z	-2.134e-07	8.408e-06	-1.939e-07	7.415e-08
	X25_P4	X31_P4		
A to Z	-3.837e-07	-4.241e-07		
B to Z	3.675e-08	3.129e-07		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X24_P4	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X24_P4
A	0.0021	0.0021	0.0026	0.0047
B	0.0022	0.0020	0.0025	0.0039
C	0.0007	0.0015	0.0020	0.0031

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0461	0.0780	5.8467	2.7180
A to Z ↑	0.0439	0.0706	11.1932	4.2639
B to Z ↓	0.0463	0.0777	5.8479	2.7188
B to Z ↑	0.0441	0.0704	11.1816	4.2655
C to Z ↓	0.0768	0.0754	5.8361	2.7181
C to Z ↑	0.0745	0.0677	11.1620	4.2654
	X17_P4	**X24_P4**	**X17_P4**	**X24_P4**
A to Z ↓	0.0703	0.0815	1.2973	0.9387
A to Z ↑	0.0685	0.0609	2.0776	1.4099
B to Z ↓	0.0699	0.0815	1.2965	0.9374

B to Z ↑	0.0682	0.0607	2.0780	1.4101
C to Z ↓	0.0684	0.0784	1.2963	0.9372
C to Z ↑	0.0666	0.0593	2.0778	1.4105

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P4	5.394e-06	2.132e-09
X8_P4	4.411e-06	2.013e-09
X17_P4	7.549e-06	2.132e-09
X24_P4	1.323e-05	3.680e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	2.068e-03	2.975e-03	4.552e-03	7.764e-03
B to Z	2.044e-03	2.908e-03	4.464e-03	7.620e-03
C to Z	4.128e-03	2.813e-03	4.410e-03	7.453e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	-1.110e-06	-1.086e-06	-1.117e-06	-3.360e-06
B to Z	1.331e-05	8.421e-06	1.396e-05	2.083e-05
C to Z	2.623e-05	1.877e-05	2.662e-05	5.473e-05

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