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C28SOI_SC_12_COREPBP16_LR Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 16 nm

Overview

- C28SOI_SC_12_COREPBP16_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

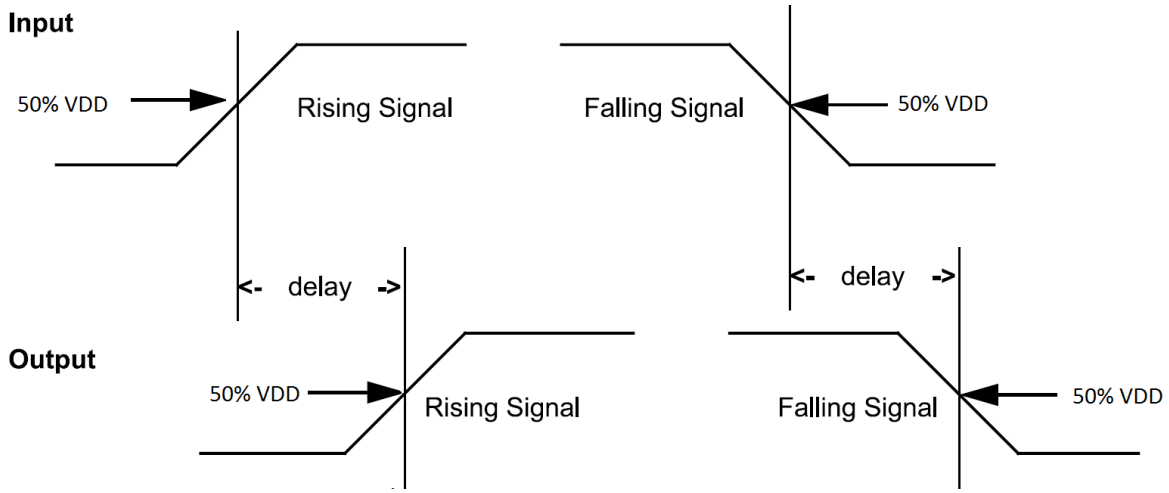


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

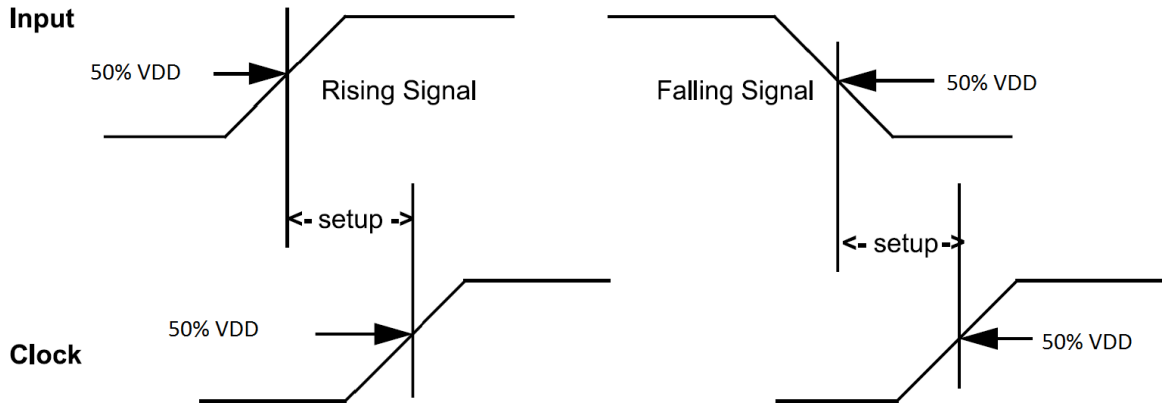


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

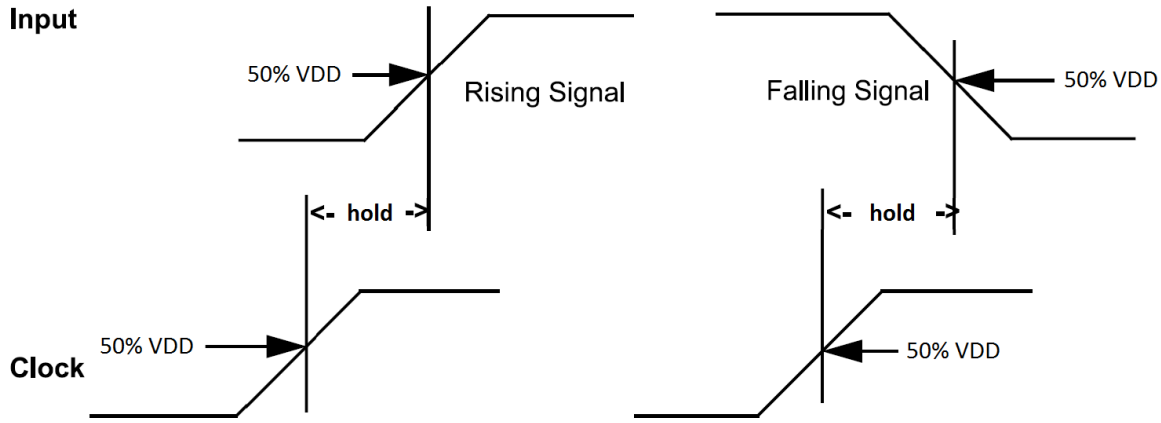


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

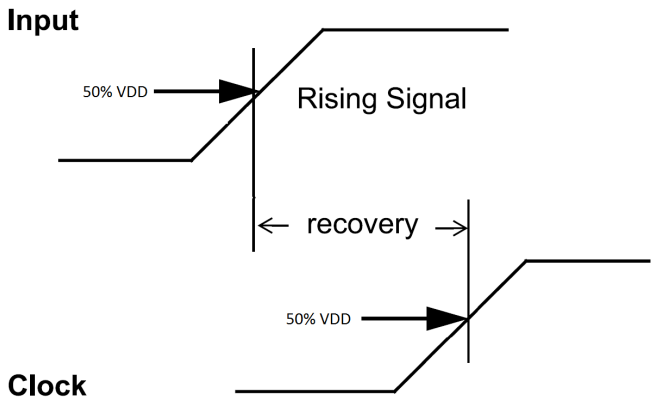


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

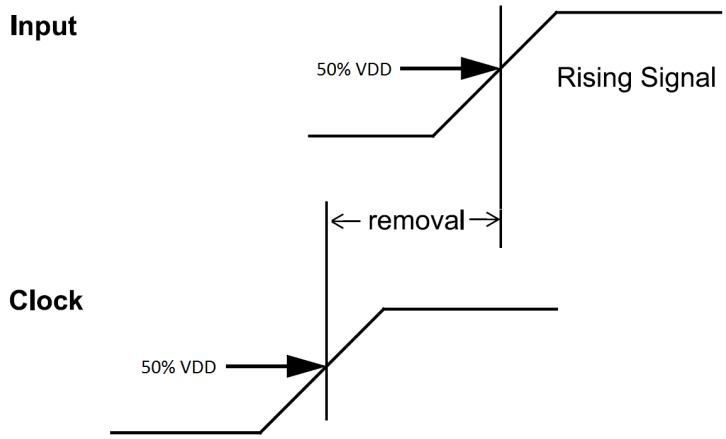


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

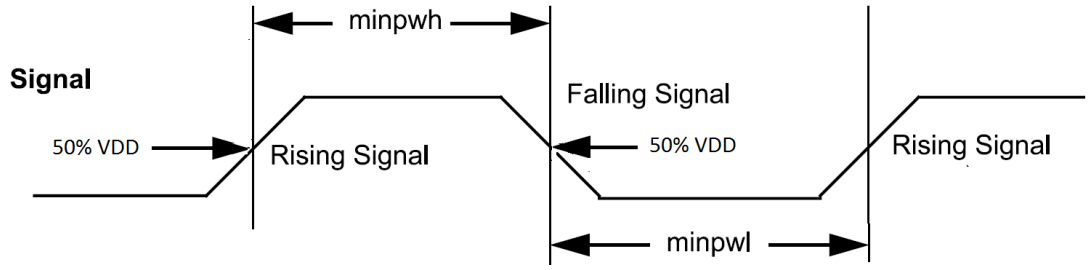


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

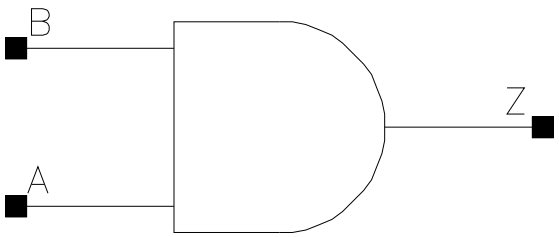
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X25_P16	1.200	1.088	1.3056
X33_P16	1.200	1.360	1.6320
X42_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0009	0.0013	0.0020	0.0025
B	0.0008	0.0013	0.0020	0.0025
	X42_P16			
A	0.0025			
B	0.0025			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0344	0.0289	1.9232	0.9726
A to Z ↑	0.0253	0.0235	3.4020	1.6575
B to Z ↓	0.0324	0.0271	1.9236	0.9719
B to Z ↑	0.0271	0.0251	3.4038	1.6584
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0299	0.0291	0.6443	0.4795

A to Z ↑	0.0234	0.0242	1.0943	0.8257
B to Z ↓	0.0281	0.0266	0.6448	0.4785
B to Z ↑	0.0249	0.0251	1.0945	0.8247
	X42_P16		**X42_P16**	
A to Z ↓	0.0314		0.3893	
A to Z ↑	0.0264		0.6604	
B to Z ↓	0.0289		0.3891	
B to Z ↑	0.0275		0.6611	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	3.499e-06	1.145e-09
X16_P16	6.368e-06	1.310e-09
X25_P16	9.526e-06	1.807e-09
X33_P16	1.296e-05	2.139e-09
X42_P16	1.463e-05	2.304e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	1.543e-05	2.833e-05	4.586e-05	1.061e-04
B (output stable)	3.280e-05	6.392e-05	1.023e-04	4.712e-04
A to Z	3.383e-03	5.647e-03	8.797e-03	1.166e-02
B to Z	3.176e-03	5.293e-03	8.240e-03	1.054e-02
	X42_P16			
A (output stable)	1.070e-04			
B (output stable)	4.662e-04			
A to Z	1.400e-02			
B to Z	1.288e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

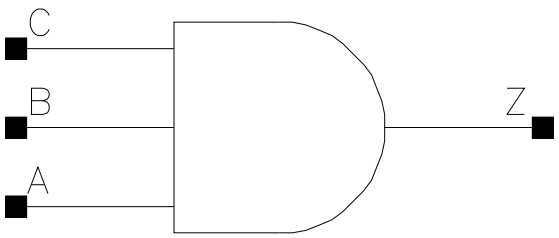
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	5.980e-08	-2.705e-08	-8.190e-08	-8.130e-08
B (output stable)	7.100e-08	2.170e-08	-2.020e-08	-8.870e-08
A to Z	-9.570e-08	-3.365e-07	3.400e-09	-6.979e-07
B to Z	-4.240e-08	6.220e-08	-2.025e-07	-2.828e-07
	X42_P16			
A (output stable)	-7.630e-08			
B (output stable)	-9.600e-08			
A to Z	-7.866e-07			
B to Z	-5.998e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X25_P16	1.200	1.360	1.6320
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0008	0.0013	0.0021	0.0026
B	0.0007	0.0013	0.0019	0.0024
C	0.0008	0.0013	0.0018	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0373	0.0320	1.9460	0.9493
A to Z ↑	0.0327	0.0306	3.4278	1.6419
B to Z ↓	0.0359	0.0304	1.9459	0.9479
B to Z ↑	0.0334	0.0313	3.4298	1.6419
C to Z ↓	0.0340	0.0286	1.9430	0.9477
C to Z ↑	0.0346	0.0320	3.4308	1.6423
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0322	0.0307	0.6514	0.4866

A to Z ↑	0.0304	0.0291	1.1191	0.8385
B to Z ↓	0.0307	0.0291	0.6506	0.4856
B to Z ↑	0.0311	0.0298	1.1186	0.8384
C to Z ↓	0.0288	0.0274	0.6503	0.4852
C to Z ↑	0.0319	0.0307	1.1188	0.8384

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	3.221e-06	1.310e-09
X17_P16	6.150e-06	1.476e-09
X25_P16	9.018e-06	2.139e-09
X33_P16	1.193e-05	2.304e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	1.846e-05	3.595e-05	4.869e-05	6.679e-05
B (output stable)	5.372e-05	1.069e-04	1.506e-04	2.056e-04
C (output stable)	1.049e-04	2.020e-04	2.980e-04	4.082e-04
A to Z	3.771e-03	6.678e-03	9.807e-03	1.258e-02
B to Z	3.560e-03	6.295e-03	9.226e-03	1.180e-02
C to Z	3.370e-03	5.917e-03	8.652e-03	1.104e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

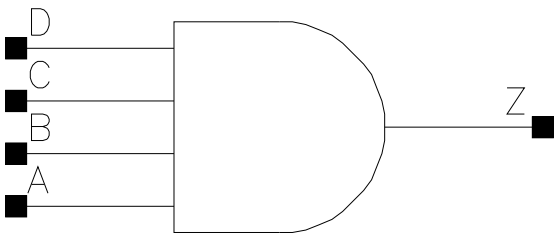
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	6.122e-08	-4.567e-09	-6.470e-08	-1.071e-07
B (output stable)	6.423e-08	3.620e-09	-6.757e-08	-1.088e-07
C (output stable)	7.920e-08	2.983e-08	-3.457e-08	-6.993e-08
A to Z	-1.762e-07	-2.094e-07	-2.785e-07	-4.965e-07
B to Z	-1.677e-07	-2.870e-07	-5.521e-07	-5.940e-07
C to Z	-2.960e-08	-5.020e-08	-4.141e-07	-3.114e-07

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X6_P16	1.200	1.088	1.3056
X20_P16	1.200	2.312	2.7744
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P16	X6_P16	X20_P16	X27_P16
A	0.0006	0.0010	0.0022	0.0025
B	0.0006	0.0009	0.0022	0.0025
C	0.0006	0.0010	0.0022	0.0025
D	0.0006	0.0009	0.0022	0.0025

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X6_P16	X4_P16	X6_P16
A to Z ↓	0.0390	0.0341	3.5291	2.3339
A to Z ↑	0.0353	0.0273	11.3440	6.1881
B to Z ↓	0.0375	0.0316	3.5306	2.3315
B to Z ↑	0.0373	0.0285	11.3483	6.1898
C to Z ↓	0.0397	0.0357	3.5124	2.3521
C to Z ↑	0.0345	0.0262	11.3543	6.2006

D to Z ↓	0.0382	0.0328	3.5105	2.3531
D to Z ↑	0.0371	0.0275	11.3654	6.2019
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0332	0.0312	0.6846	0.4846
A to Z ↑	0.0283	0.0318	2.0646	1.5673
B to Z ↓	0.0301	0.0286	0.6830	0.4836
B to Z ↑	0.0289	0.0328	2.0654	1.5671
C to Z ↓	0.0323	0.0299	0.6901	0.4875
C to Z ↑	0.0247	0.0270	2.0660	1.5663
D to Z ↓	0.0290	0.0275	0.6893	0.4865
D to Z ↑	0.0251	0.0280	2.0661	1.5662

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	3.218e-06	1.807e-09
X6_P16	5.945e-06	1.807e-09
X20_P16	1.692e-05	3.298e-09
X27_P16	1.996e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	6.162e-04	9.608e-04	2.820e-03	3.495e-03
B (output stable)	5.678e-04	8.617e-04	2.589e-03	3.247e-03
C (output stable)	5.702e-04	9.320e-04	2.423e-03	2.982e-03
D (output stable)	5.261e-04	8.246e-04	2.136e-03	2.664e-03
A to Z	2.481e-03	3.852e-03	1.163e-02	1.510e-02
B to Z	2.351e-03	3.593e-03	1.062e-02	1.406e-02
C to Z	2.375e-03	3.773e-03	9.780e-03	1.224e-02
D to Z	2.246e-03	3.494e-03	8.738e-03	1.121e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

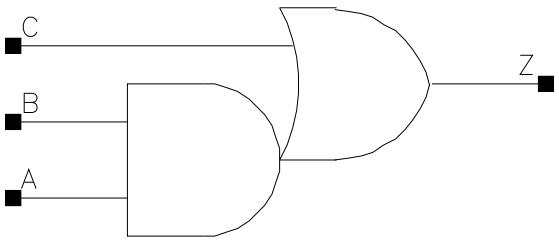
Pin Cycle (vdds)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	-3.663e-07	-3.426e-07	-2.994e-06	-5.757e-06
B (output stable)	-3.253e-07	-3.272e-07	-2.787e-06	-6.551e-06
C (output stable)	6.078e-06	1.088e-05	3.995e-05	6.790e-05
D (output stable)	5.954e-06	1.087e-05	3.343e-05	5.311e-05
A to Z	-9.060e-08	5.409e-07	-1.620e-07	-2.859e-06
B to Z	7.400e-09	4.332e-07	-8.380e-07	-1.853e-06
C to Z	-2.053e-07	-2.501e-07	-1.139e-06	-1.569e-06
D to Z	-2.393e-07	-2.880e-07	-9.483e-07	-1.441e-06

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0008	0.0012	0.0025
B	0.0008	0.0013	0.0024
C	0.0009	0.0014	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0440	0.0401	1.9916	0.9732
A to Z ↑	0.0264	0.0238	3.3240	1.6296
B to Z ↓	0.0405	0.0368	1.9837	0.9680
B to Z ↑	0.0284	0.0258	3.3241	1.6298
C to Z ↓	0.0427	0.0391	1.9801	0.9680
C to Z ↑	0.0249	0.0235	3.3046	1.6203
	X33_P16		**X33_P16**	
A to Z ↓	0.0401		0.4939	
A to Z ↑	0.0242		0.8201	

B to Z ↓	0.0370		0.4923	
B to Z ↑	0.0257		0.8204	
C to Z ↓	0.0392		0.4917	
C to Z ↑	0.0232		0.8162	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	4.602e-06	1.310e-09
X17_P16	8.452e-06	1.476e-09
X33_P16	1.699e-05	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.271e-05	2.244e-05	6.289e-05
B (output stable)	2.646e-05	3.947e-05	1.609e-04
C (output stable)	7.842e-05	1.315e-04	3.023e-04
A to Z	3.515e-03	6.179e-03	1.230e-02
B to Z	3.298e-03	5.771e-03	1.133e-02
C to Z	3.853e-03	6.763e-03	1.345e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

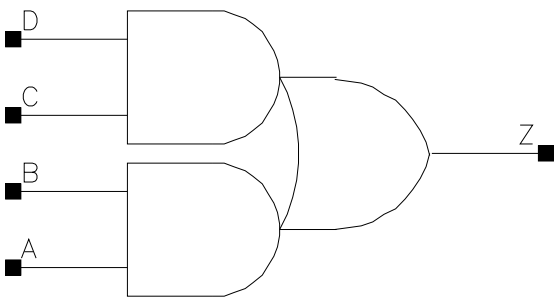
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	9.226e-06	2.071e-05	3.449e-05
B (output stable)	2.018e-05	3.292e-05	6.122e-05
C (output stable)	-4.899e-06	-6.303e-06	-1.245e-05
A to Z	-1.262e-07	-2.457e-07	-5.981e-07
B to Z	-1.159e-07	-2.622e-07	-1.141e-06
C to Z	-1.995e-06	-2.522e-06	-4.761e-06

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0008	0.0012	0.0024
B	0.0009	0.0013	0.0023
C	0.0007	0.0012	0.0025
D	0.0008	0.0013	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0499	0.0442	1.9288	0.9677
A to Z ↑	0.0339	0.0309	3.2754	1.6317
B to Z ↓	0.0461	0.0409	1.9174	0.9628
B to Z ↑	0.0355	0.0329	3.2790	1.6308

C to Z ↓	0.0450	0.0406	1.9199	0.9642
C to Z ↑	0.0286	0.0260	3.2696	1.6250
D to Z ↓	0.0427	0.0382	1.9124	0.9607
D to Z ↑	0.0309	0.0281	3.2698	1.6258
	X33_P16		**X33_P16**	
A to Z ↓	0.0428		0.4945	
A to Z ↑	0.0286		0.8237	
B to Z ↓	0.0402		0.4936	
B to Z ↑	0.0308		0.8238	
C to Z ↓	0.0391		0.4930	
C to Z ↑	0.0244		0.8215	
D to Z ↓	0.0367		0.4919	
D to Z ↑	0.0263		0.8214	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	5.117e-06	1.642e-09
X17_P16	9.493e-06	1.807e-09
X33_P16	1.774e-05	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	3.983e-05	5.882e-05	9.343e-05
B (output stable)	1.817e-04	2.282e-04	1.328e-04
C (output stable)	1.959e-05	3.459e-05	7.156e-05
D (output stable)	3.058e-05	5.665e-05	1.202e-04
A to Z	4.668e-03	7.903e-03	1.489e-02
B to Z	4.280e-03	7.308e-03	1.404e-02
C to Z	3.919e-03	6.687e-03	1.247e-02
D to Z	3.721e-03	6.312e-03	1.170e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

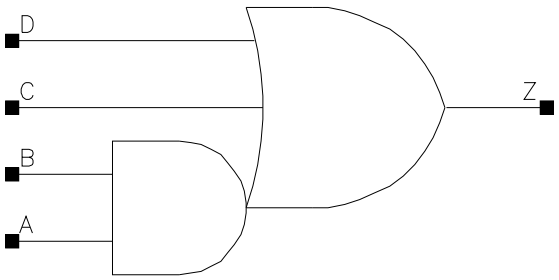
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-4.777e-07	-7.140e-07	-2.388e-06
B (output stable)	-1.928e-06	-7.595e-07	-2.391e-06
C (output stable)	5.683e-06	1.409e-05	3.384e-05
D (output stable)	5.957e-06	1.417e-05	3.323e-05
A to Z	-1.002e-06	-1.317e-06	-2.636e-06
B to Z	-8.476e-07	-9.577e-07	-2.934e-06
C to Z	-2.178e-07	-2.967e-07	-5.510e-07
D to Z	-2.812e-07	-2.721e-07	-6.438e-07

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	0.952	1.1424
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0008	0.0012	0.0022
B	0.0008	0.0012	0.0023
C	0.0008	0.0012	0.0024
D	0.0008	0.0012	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0572	0.0509	2.1028	1.0340
A to Z ↑	0.0283	0.0258	3.3165	1.6824
B to Z ↓	0.0542	0.0472	2.0931	1.0293
B to Z ↑	0.0305	0.0274	3.3133	1.6815
C to Z ↓	0.0603	0.0536	2.0937	1.0291
C to Z ↑	0.0269	0.0251	3.2959	1.6725

D to Z ↓	0.0595	0.0533	2.0935	1.0300
D to Z ↑	0.0265	0.0250	3.2930	1.6718
	X33_P16		**X33_P16**	
A to Z ↓	0.0518		0.5182	
A to Z ↑	0.0258		0.8217	
B to Z ↓	0.0462		0.5140	
B to Z ↑	0.0269		0.8215	
C to Z ↓	0.0552		0.5152	
C to Z ↑	0.0248		0.8177	
D to Z ↓	0.0535		0.5152	
D to Z ↑	0.0239		0.8166	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	4.909e-06	1.476e-09
X17_P16	9.139e-06	1.642e-09
X33_P16	1.873e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	6.976e-06	1.319e-05	4.556e-05
B (output stable)	1.196e-05	2.162e-05	1.121e-04
C (output stable)	1.280e-04	2.123e-04	5.698e-04
D (output stable)	1.323e-05	2.081e-05	5.607e-05
A to Z	3.917e-03	6.705e-03	1.351e-02
B to Z	3.715e-03	6.290e-03	1.227e-02
C to Z	4.512e-03	7.765e-03	1.580e-02
D to Z	4.241e-03	7.295e-03	1.452e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

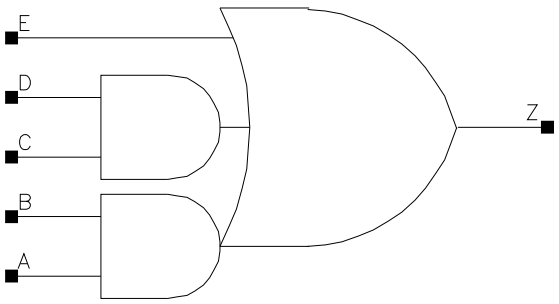
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	9.106e-06	2.010e-05	3.362e-05
B (output stable)	1.582e-05	3.202e-05	5.275e-05
C (output stable)	-1.626e-05	-2.500e-05	-6.590e-05
D (output stable)	9.638e-06	1.976e-05	5.811e-05
A to Z	-1.756e-07	-5.094e-07	-1.162e-06
B to Z	-2.407e-07	-4.023e-07	-1.047e-06
C to Z	-3.011e-06	-3.528e-06	-9.126e-06
D to Z	-1.758e-06	-1.906e-06	-3.940e-06

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.088	1.3056
X17_P16	1.200	1.224	1.4688
X33_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0008	0.0012	0.0024
B	0.0008	0.0012	0.0023
C	0.0009	0.0014	0.0024
D	0.0008	0.0012	0.0023
E	0.0008	0.0012	0.0022

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0707	0.0618	2.0202	1.0085
A to Z ↑	0.0357	0.0311	3.2552	1.6387

B to Z ↓	0.0678	0.0585	2.0088	1.0037
B to Z ↑	0.0386	0.0336	3.2549	1.6392
C to Z ↓	0.0593	0.0532	2.0082	1.0033
C to Z ↑	0.0300	0.0259	3.2318	1.6294
D to Z ↓	0.0548	0.0482	1.9943	0.9963
D to Z ↑	0.0321	0.0277	3.2327	1.6290
E to Z ↓	0.0617	0.0540	1.9944	0.9980
E to Z ↑	0.0281	0.0247	3.2076	1.6188
	X33_P16		**X33_P16**	
A to Z ↓	0.0606		0.5179	
A to Z ↑	0.0321		0.8270	
B to Z ↓	0.0566		0.5156	
B to Z ↑	0.0343		0.8261	
C to Z ↓	0.0513		0.5154	
C to Z ↑	0.0261		0.8215	
D to Z ↓	0.0469		0.5120	
D to Z ↑	0.0278		0.8213	
E to Z ↓	0.0526		0.5128	
E to Z ↑	0.0248		0.8161	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	5.870e-06	1.807e-09
X17_P16	1.078e-05	1.973e-09
X33_P16	2.009e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	3.266e-05	5.243e-05	1.188e-04
B (output stable)	5.143e-05	6.208e-05	1.693e-04
C (output stable)	2.092e-05	2.884e-05	7.639e-05
D (output stable)	2.648e-05	4.151e-05	1.257e-04
E (output stable)	9.219e-05	9.479e-05	2.442e-04
A to Z	5.441e-03	8.929e-03	1.750e-02
B to Z	5.237e-03	8.491e-03	1.640e-02
C to Z	4.244e-03	7.070e-03	1.368e-02
D to Z	4.007e-03	6.606e-03	1.266e-02
E to Z	4.640e-03	7.624e-03	1.474e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-3.096e-06	-4.263e-06	-9.650e-06
B (output stable)	-5.098e-06	-4.569e-06	-1.111e-05
C (output stable)	1.156e-05	2.430e-05	5.218e-05
D (output stable)	1.479e-05	3.191e-05	6.518e-05
E (output stable)	1.022e-05	2.487e-05	4.408e-05
A to Z	-3.274e-06	-2.204e-06	-5.578e-06
B to Z	-3.098e-06	-2.460e-06	-4.595e-06
C to Z	-2.292e-07	-4.454e-07	-7.680e-07
D to Z	-1.770e-07	-4.062e-07	-9.902e-07

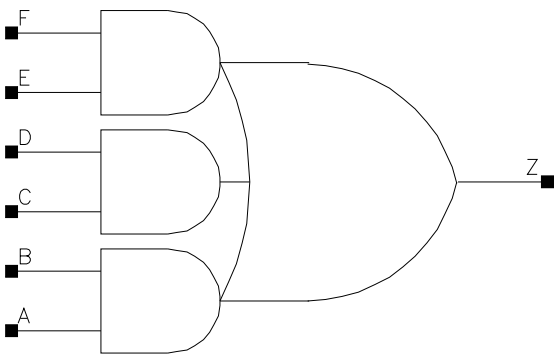
E to Z	-1.791e-06	-1.553e-06	-4.094e-06

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.360	1.6320
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
A	0.0008	0.0009	0.0012	0.0024

B	0.0008	0.0009	0.0016	0.0022
C	0.0007	0.0009	0.0011	0.0023
D	0.0008	0.0009	0.0012	0.0022
E	0.0008	0.0009	0.0012	0.0024
F	0.0008	0.0009	0.0012	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0702	0.0669	3.7577	2.0097
A to Z ↑	0.0374	0.0364	6.2772	3.3103
B to Z ↓	0.0643	0.0618	3.7217	1.9922
B to Z ↑	0.0388	0.0381	6.2763	3.3087
C to Z ↓	0.0637	0.0612	3.7414	2.0015
C to Z ↑	0.0338	0.0329	6.2399	3.2898
D to Z ↓	0.0603	0.0581	3.7201	1.9905
D to Z ↑	0.0364	0.0355	6.2377	3.2908
E to Z ↓	0.0524	0.0517	3.7157	1.9901
E to Z ↑	0.0283	0.0276	6.2104	3.2757
F to Z ↓	0.0485	0.0479	3.6947	1.9791
F to Z ↑	0.0302	0.0297	6.2092	3.2767
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
A to Z ↓	0.0653	0.0631	1.0121	0.5170
A to Z ↑	0.0341	0.0345	1.6429	0.8298
B to Z ↓	0.0613	0.0594	1.0030	0.5150
B to Z ↑	0.0367	0.0367	1.6429	0.8296
C to Z ↓	0.0606	0.0586	1.0085	0.5165
C to Z ↑	0.0310	0.0320	1.6345	0.8254
D to Z ↓	0.0569	0.0551	1.0025	0.5143
D to Z ↑	0.0335	0.0341	1.6345	0.8253
E to Z ↓	0.0513	0.0520	1.0025	0.5143
E to Z ↑	0.0261	0.0275	1.6291	0.8233
F to Z ↓	0.0477	0.0480	0.9971	0.5114
F to Z ↑	0.0281	0.0296	1.6286	0.8231

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	5.147e-06	2.139e-09
X8_P16	7.276e-06	2.139e-09
X17_P16	1.173e-05	2.304e-09
X33_P16	2.138e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	8.704e-05	1.029e-04	1.280e-04	2.523e-04
B (output stable)	2.445e-04	2.644e-04	2.743e-04	4.293e-04
C (output stable)	3.946e-05	4.639e-05	5.697e-05	9.101e-05
D (output stable)	5.259e-05	6.285e-05	7.568e-05	1.852e-04
E (output stable)	4.485e-05	5.025e-05	6.037e-05	8.452e-05
F (output stable)	4.697e-05	5.392e-05	6.935e-05	1.512e-04

A to Z	4.813e-03	6.439e-03	9.906e-03	1.897e-02
B to Z	4.408e-03	5.958e-03	9.249e-03	1.790e-02
C to Z	4.048e-03	5.524e-03	8.676e-03	1.667e-02
D to Z	3.844e-03	5.258e-03	8.242e-03	1.568e-02
E to Z	3.214e-03	4.572e-03	7.295e-03	1.445e-02
F to Z	3.007e-03	4.295e-03	6.876e-03	1.351e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

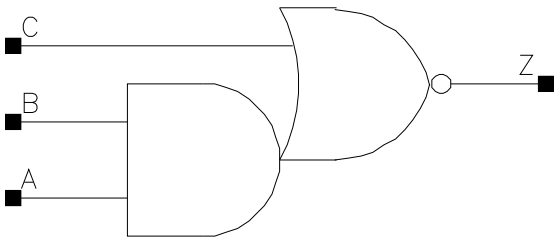
Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	-7.827e-06	-9.077e-06	-1.121e-05	-2.174e-05
B (output stable)	-1.567e-05	-1.649e-05	-1.505e-05	-3.610e-05
C (output stable)	3.941e-08	1.518e-06	6.347e-06	2.115e-05
D (output stable)	3.156e-06	4.745e-06	7.536e-06	2.848e-05
E (output stable)	2.448e-05	3.118e-05	4.467e-05	7.510e-05
F (output stable)	2.158e-05	2.752e-05	3.954e-05	6.874e-05
A to Z	-4.952e-06	-4.660e-06	-4.575e-06	-8.550e-06
B to Z	-4.717e-06	-4.352e-06	-4.178e-06	-7.964e-06
C to Z	-2.292e-06	-2.100e-06	-2.147e-06	-2.148e-06
D to Z	-2.221e-06	-2.057e-06	-1.980e-06	-1.861e-06
E to Z	-3.480e-07	-3.935e-07	-4.558e-07	-8.720e-07
F to Z	-3.648e-07	-3.919e-07	-5.621e-07	-7.821e-07

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008
X44_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X33_P16	X44_P16
A	0.0010	0.0030	0.0060	0.0081
B	0.0010	0.0028	0.0056	0.0075
C	0.0011	0.0032	0.0062	0.0082

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0089	0.0094	3.3014	1.1189
A to Z ↑	0.0204	0.0210	6.3084	2.1068
B to Z ↓	0.0092	0.0095	3.3435	1.1363
B to Z ↑	0.0163	0.0162	6.2351	2.1101
C to Z ↓	0.0100	0.0103	1.9665	0.6723
C to Z ↑	0.0207	0.0208	5.7525	1.9364
	X33_P16	**X44_P16**	**X33_P16**	**X44_P16**
A to Z ↓	0.0097	0.0096	0.5693	0.4314

A to Z ↑	0.0209	0.0210	1.0541	0.7990
B to Z ↓	0.0095	0.0094	0.5782	0.4382
B to Z ↑	0.0161	0.0160	1.0539	0.7967
C to Z ↓	0.0118	0.0120	0.3998	0.3106
C to Z ↑	0.0212	0.0211	0.9671	0.7318

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P16	3.838e-06	1.145e-09
X17_P16	1.083e-05	2.139e-09
X33_P16	2.030e-05	3.629e-09
X44_P16	2.670e-05	4.623e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	2.347e-05	8.158e-05	1.764e-04	2.321e-04
B (output stable)	4.242e-05	2.160e-04	4.952e-04	6.384e-04
C (output stable)	1.297e-04	4.038e-04	8.846e-04	1.160e-03
A to Z	1.567e-03	4.987e-03	1.004e-02	1.328e-02
B to Z	1.218e-03	3.596e-03	7.160e-03	9.466e-03
C to Z	2.253e-03	6.781e-03	1.381e-02	1.822e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

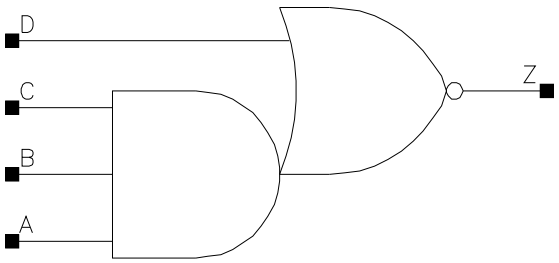
Pin Cycle (vdds)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	1.785e-05	4.539e-05	9.079e-05	1.174e-04
B (output stable)	2.997e-05	7.097e-05	1.563e-04	1.990e-04
C (output stable)	-5.835e-06	-1.354e-05	-3.181e-05	-4.013e-05
A to Z	4.162e-07	1.011e-06	2.081e-06	2.785e-06
B to Z	1.788e-07	2.090e-07	-6.000e-09	-2.494e-06
C to Z	-1.244e-06	-3.126e-06	-8.486e-06	-9.033e-06

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X29_P16	1.200	3.536	4.2432
X38_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X29_P16	X38_P16
A	0.0010	0.0061	0.0079
B	0.0010	0.0058	0.0076
C	0.0009	0.0055	0.0073
D	0.0011	0.0062	0.0077

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X29_P16	X5_P16	X29_P16
A to Z ↓	0.0136	0.0148	4.6647	0.8066
A to Z ↑	0.0261	0.0263	6.3072	1.0448
B to Z ↓	0.0138	0.0142	4.6795	0.8106
B to Z ↑	0.0230	0.0229	6.3119	1.0518
C to Z ↓	0.0137	0.0136	4.7055	0.8160
C to Z ↑	0.0192	0.0185	6.2434	1.0602
D to Z ↓	0.0123	0.0142	2.0044	0.4024

D to Z ↑	0.0239	0.0245	5.3630	0.8966
	X38_P16		**X38_P16**	
A to Z ↓	0.0145		0.6229	
A to Z ↑	0.0258		0.7869	
B to Z ↓	0.0141		0.6263	
B to Z ↑	0.0225		0.7943	
C to Z ↓	0.0134		0.6306	
C to Z ↑	0.0181		0.8032	
D to Z ↓	0.0151		0.3334	
D to Z ↑	0.0241		0.6766	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P16	4.249e-06	1.310e-09
X29_P16	2.274e-05	4.789e-09
X38_P16	2.909e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P16	X29_P16	X38_P16
A (output stable)	2.203e-05	1.998e-04	2.486e-04
B (output stable)	4.705e-05	4.414e-04	5.628e-04
C (output stable)	8.890e-05	9.172e-04	1.166e-03
D (output stable)	4.488e-04	3.674e-03	4.779e-03
A to Z	2.326e-03	1.482e-02	1.897e-02
B to Z	1.955e-03	1.180e-02	1.518e-02
C to Z	1.597e-03	8.904e-03	1.135e-02
D to Z	2.939e-03	1.809e-02	2.334e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

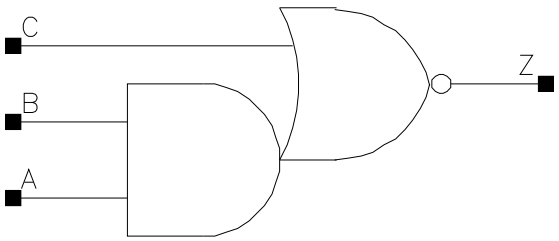
Pin Cycle (vdds)	X5_P16	X29_P16	X38_P16
A (output stable)	1.520e-05	1.099e-04	1.416e-04
B (output stable)	8.537e-06	5.905e-05	7.519e-05
C (output stable)	9.229e-06	5.669e-05	7.208e-05
D (output stable)	-4.136e-05	-4.033e-04	-5.048e-04
A to Z	-1.770e-07	-3.039e-06	-1.561e-06
B to Z	-4.810e-07	-3.303e-06	-4.419e-06
C to Z	-4.840e-07	1.429e-06	1.723e-06
D to Z	-1.286e-06	-1.762e-05	-2.387e-05

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X11_P16	1.200	1.088	1.3056
X16_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X11_P16	X16_P16	X23_P16
A	0.0011	0.0022	0.0033	0.0043
B	0.0011	0.0021	0.0030	0.0040
C	0.0011	0.0020	0.0029	0.0041
	X46_P16			
A	0.0084			
B	0.0079			
C	0.0080			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X11_P16	X6_P16	X11_P16
A to Z ↓	0.0112	0.0122	3.1959	1.6210
A to Z ↑	0.0228	0.0241	6.2893	3.0743
B to Z ↓	0.0122	0.0125	3.2310	1.6416

B to Z ↑	0.0194	0.0199	6.2244	3.0855
C to Z ↓	0.0063	0.0069	2.0257	1.1885
C to Z ↑	0.0163	0.0160	5.7917	2.8537
	X16_P16	**X23_P16**	**X16_P16**	**X23_P16**
A to Z ↓	0.0117	0.0119	1.1187	0.8411
A to Z ↑	0.0228	0.0231	2.0673	1.5656
B to Z ↓	0.0124	0.0123	1.1333	0.8517
B to Z ↑	0.0186	0.0189	2.0690	1.5722
C to Z ↓	0.0070	0.0059	0.8251	0.5194
C to Z ↑	0.0154	0.0159	1.9174	1.4530
	X46_P16		**X46_P16**	
A to Z ↓	0.0116		0.4318	
A to Z ↑	0.0224		0.8098	
B to Z ↓	0.0121		0.4371	
B to Z ↑	0.0181		0.8088	
C to Z ↓	0.0063		0.2654	
C to Z ↑	0.0160		0.7499	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P16	3.940e-06	1.145e-09
X11_P16	7.691e-06	1.807e-09
X16_P16	1.053e-05	2.139e-09
X23_P16	1.529e-05	2.801e-09
X46_P16	2.942e-05	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	3.824e-05	1.026e-04	1.340e-04	1.867e-04
B (output stable)	7.425e-05	3.064e-04	3.075e-04	4.645e-04
C (output stable)	7.573e-05	1.906e-04	2.565e-04	3.862e-04
A to Z	2.304e-03	5.103e-03	7.024e-03	9.557e-03
B to Z	1.925e-03	4.040e-03	5.508e-03	7.452e-03
C to Z	1.227e-03	2.483e-03	3.455e-03	4.820e-03
	X46_P16			
A (output stable)	3.368e-04			
B (output stable)	7.149e-04			
C (output stable)	6.029e-04			
A to Z	1.782e-02			
B to Z	1.380e-02			
C to Z	9.220e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	-1.264e-06	-3.774e-06	-3.331e-06	-4.661e-06
B (output stable)	-5.252e-06	-2.151e-05	-1.311e-05	-2.012e-05
C (output stable)	7.912e-05	2.104e-04	1.989e-04	2.730e-04
A to Z	-2.920e-07	-1.259e-06	-8.820e-07	-1.516e-06
B to Z	1.900e-08	-8.050e-07	-3.230e-07	-1.107e-06
C to Z	1.019e-06	6.932e-07	1.036e-06	-9.200e-07

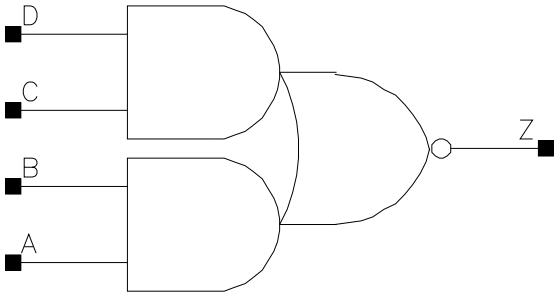
	X46_P16			
A (output stable)	-6.815e-06			
B (output stable)	-1.775e-05			
C (output stable)	4.508e-04			
A to Z	-3.638e-06			
B to Z	5.840e-07			
C to Z	-1.901e-06			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P16	X10_P16	X16_P16	X21_P16
A	0.0009	0.0022	0.0033	0.0042
B	0.0009	0.0020	0.0030	0.0040
C	0.0008	0.0021	0.0030	0.0041
D	0.0008	0.0019	0.0028	0.0038
	X42_P16			
A	0.0085			
B	0.0080			
C	0.0081			
D	0.0076			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X10_P16**	**X4_P16**	**X10_P16**
A to Z ↓	0.0129	0.0128	3.9552	1.5622
A to Z ↑	0.0293	0.0252	8.5183	2.8329
B to Z ↓	0.0142	0.0143	4.0016	1.5815
B to Z ↑	0.0258	0.0225	8.5070	2.8973
C to Z ↓	0.0092	0.0087	4.0429	1.5713
C to Z ↑	0.0235	0.0206	8.5300	2.8543
D to Z ↓	0.0098	0.0094	4.1055	1.5975
D to Z ↑	0.0196	0.0172	8.5213	2.8951
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0140	0.0140	1.1236	0.8441
A to Z ↑	0.0263	0.0263	1.9079	1.4719
B to Z ↓	0.0152	0.0148	1.1357	0.8536
B to Z ↑	0.0227	0.0224	1.9096	1.4754
C to Z ↓	0.0096	0.0098	1.1233	0.8449
C to Z ↑	0.0214	0.0219	1.9126	1.4732
D to Z ↓	0.0099	0.0096	1.1408	0.8586
D to Z ↑	0.0172	0.0175	1.9173	1.4775
	X42_P16		**X42_P16**	
A to Z ↓	0.0148		0.4375	
A to Z ↑	0.0267		0.7373	
B to Z ↓	0.0154		0.4423	
B to Z ↑	0.0226		0.7355	
C to Z ↓	0.0105		0.4331	
C to Z ↑	0.0221		0.7392	
D to Z ↓	0.0104		0.4397	
D to Z ↑	0.0178		0.7385	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	3.806e-06	1.310e-09
X10_P16	9.775e-06	2.139e-09
X16_P16	1.367e-05	2.635e-09
X21_P16	1.848e-05	3.464e-09
X42_P16	3.601e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	3.811e-05	8.890e-05	1.683e-04	2.251e-04
B (output stable)	5.216e-05	1.298e-04	3.895e-04	5.809e-04
C (output stable)	2.446e-05	6.799e-05	1.277e-04	1.854e-04
D (output stable)	4.055e-05	1.112e-04	3.444e-04	5.332e-04
A to Z	2.368e-03	5.837e-03	9.185e-03	1.204e-02
B to Z	2.035e-03	5.033e-03	7.660e-03	9.937e-03
C to Z	1.401e-03	3.503e-03	5.531e-03	7.473e-03
D to Z	1.113e-03	2.780e-03	4.125e-03	5.521e-03
	X42_P16			
A (output stable)	4.341e-04			
B (output stable)	1.020e-03			
C (output stable)	3.542e-04			
D (output stable)	9.485e-04			

A to Z	2.371e-02			
B to Z	1.970e-02			
C to Z	1.471e-02			
D to Z	1.101e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

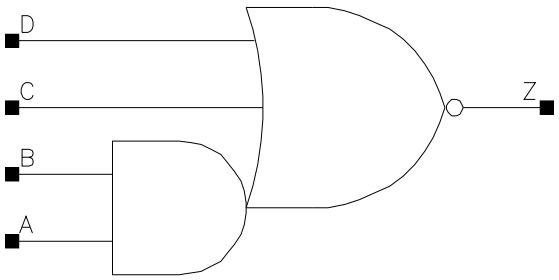
Pin Cycle (vdds)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	-1.417e-06	-2.420e-06	-3.637e-06	-4.121e-06
B (output stable)	-1.423e-06	-2.384e-06	-3.673e-06	-5.536e-06
C (output stable)	1.161e-05	3.341e-05	4.533e-05	6.185e-05
D (output stable)	1.134e-05	3.285e-05	4.547e-05	5.986e-05
A to Z	-1.919e-06	-1.678e-06	-3.735e-06	-4.300e-06
B to Z	-1.563e-06	-1.725e-06	-1.847e-06	-1.253e-06
C to Z	-2.463e-08	-3.330e-07	-7.720e-07	7.890e-07
D to Z	6.247e-08	6.733e-08	2.093e-07	-2.417e-07
	X42_P16			
A (output stable)	-7.482e-06			
B (output stable)	-1.005e-05			
C (output stable)	1.146e-04			
D (output stable)	1.117e-04			
A to Z	-6.263e-06			
B to Z	-4.520e-06			
C to Z	1.601e-06			
D to Z	-9.300e-08			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X35_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P16	X35_P16
A	0.0010	0.0077
B	0.0010	0.0071
C	0.0011	0.0075
D	0.0011	0.0070

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X35_P16	X5_P16	X35_P16
A to Z ↓	0.0106	0.0111	3.3360	0.4906
A to Z ↑	0.0266	0.0251	9.2673	1.1812
B to Z ↓	0.0112	0.0114	3.3822	0.4984
B to Z ↑	0.0216	0.0195	9.2174	1.1821
C to Z ↓	0.0124	0.0165	2.0915	0.3996
C to Z ↑	0.0303	0.0302	8.7445	1.1160
D to Z ↓	0.0118	0.0152	2.1044	0.3986

D to Z ↑	0.0294	0.0281	8.7500	1.1185

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P16	3.898e-06	1.310e-09
X35_P16	2.393e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P16	X35_P16
A (output stable)	1.347e-05	1.472e-04
B (output stable)	2.209e-05	2.987e-04
C (output stable)	2.070e-04	2.088e-03
D (output stable)	1.998e-05	2.204e-04
A to Z	1.857e-03	1.360e-02
B to Z	1.497e-03	1.021e-02
C to Z	3.046e-03	2.403e-02
D to Z	2.550e-03	1.892e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

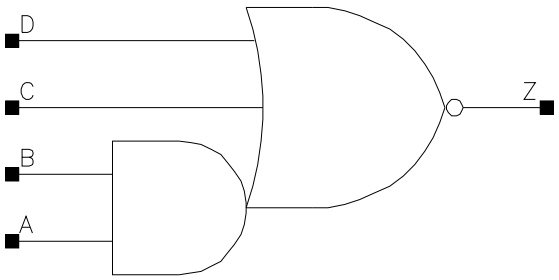
Pin Cycle (vdds)	X5_P16	X35_P16
A (output stable)	1.960e-05	1.264e-04
B (output stable)	2.989e-05	1.839e-04
C (output stable)	-2.414e-05	-1.906e-04
D (output stable)	1.887e-05	1.497e-04
A to Z	-2.462e-07	-1.978e-06
B to Z	-2.803e-07	-3.366e-06
C to Z	-2.838e-06	-2.470e-05
D to Z	-1.436e-06	-1.067e-05

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X17_P16	1.200	2.448	2.9376
X34_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P16	X17_P16	X34_P16
A	0.0010	0.0042	0.0086
B	0.0010	0.0040	0.0081
C	0.0009	0.0036	0.0071
D	0.0009	0.0034	0.0065

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X17_P16	X4_P16	X17_P16
A to Z ↓	0.0133	0.0146	3.6234	0.9556
A to Z ↑	0.0311	0.0328	9.3085	2.2950
B to Z ↓	0.0150	0.0155	3.6657	0.9656
B to Z ↑	0.0269	0.0274	9.2406	2.3007
C to Z ↓	0.0131	0.0130	3.2778	0.8017
C to Z ↑	0.0225	0.0240	8.7789	2.1735

D to Z ↓	0.0104	0.0094	3.3712	0.8082
D to Z ↑	0.0198	0.0185	8.8139	2.1828
	X34_P16		**X34_P16**	
A to Z ↓	0.0144		0.4895	
A to Z ↑	0.0323		1.1671	
B to Z ↓	0.0156		0.4946	
B to Z ↑	0.0270		1.1650	
C to Z ↓	0.0132		0.4263	
C to Z ↑	0.0234		1.1035	
D to Z ↓	0.0096		0.4314	
D to Z ↑	0.0181		1.1082	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	3.275e-06	1.310e-09
X17_P16	1.284e-05	3.464e-09
X34_P16	2.456e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P16	X17_P16	X34_P16
A (output stable)	5.166e-05	2.375e-04	4.758e-04
B (output stable)	5.627e-05	3.355e-04	6.345e-04
C (output stable)	5.280e-05	4.133e-04	7.639e-04
D (output stable)	2.220e-05	2.426e-04	4.324e-04
A to Z	2.907e-03	1.264e-02	2.451e-02
B to Z	2.548e-03	1.060e-02	2.063e-02
C to Z	1.759e-03	7.689e-03	1.469e-02
D to Z	1.238e-03	4.730e-03	9.031e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

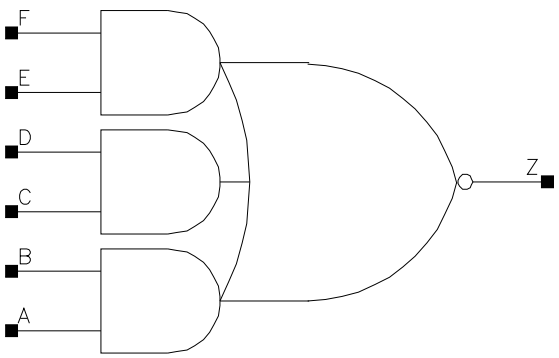
Pin Cycle (vdds)	X4_P16	X17_P16	X34_P16
A (output stable)	-3.920e-06	-1.565e-05	-2.986e-05
B (output stable)	-4.266e-06	-1.990e-05	-3.695e-05
C (output stable)	1.491e-05	1.741e-05	4.338e-05
D (output stable)	4.206e-05	2.156e-04	3.874e-04
A to Z	-8.080e-07	-3.607e-06	-6.710e-06
B to Z	-5.200e-07	-1.131e-06	-3.260e-06
C to Z	-2.550e-07	-3.180e-06	-6.039e-06
D to Z	-6.460e-08	-3.316e-07	-1.230e-06

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X8_P16	1.200	2.176	2.6112
X13_P16	1.200	2.720	3.2640
X17_P16	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P16	X8_P16	X13_P16	X17_P16
A	0.0011	0.0021	0.0032	0.0042

B	0.0010	0.0020	0.0030	0.0039
C	0.0010	0.0020	0.0030	0.0039
D	0.0010	0.0019	0.0028	0.0037
E	0.0012	0.0020	0.0029	0.0038
F	0.0010	0.0018	0.0027	0.0035

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0158	0.0194	3.2104	1.8555
A to Z ↑	0.0442	0.0434	8.9111	4.1320
B to Z ↓	0.0180	0.0208	3.2428	1.8695
B to Z ↑	0.0399	0.0387	8.9150	4.1444
C to Z ↓	0.0144	0.0173	3.1773	1.8643
C to Z ↑	0.0387	0.0388	8.9481	4.1437
D to Z ↓	0.0161	0.0188	3.2186	1.8834
D to Z ↑	0.0344	0.0342	8.9192	4.1471
E to Z ↓	0.0103	0.0125	3.1354	1.8676
E to Z ↑	0.0295	0.0294	8.8804	4.1238
F to Z ↓	0.0112	0.0131	3.1939	1.8968
F to Z ↑	0.0250	0.0245	8.9450	4.1330
	X13_P16	**X17_P16**	**X13_P16**	**X17_P16**
A to Z ↓	0.0186	0.0187	1.2613	0.9608
A to Z ↑	0.0407	0.0408	2.7316	2.0877
B to Z ↓	0.0205	0.0202	1.2701	0.9678
B to Z ↑	0.0366	0.0361	2.7430	2.0904
C to Z ↓	0.0167	0.0167	1.2662	0.9499
C to Z ↑	0.0360	0.0364	2.7431	2.0988
D to Z ↓	0.0184	0.0178	1.2782	0.9595
D to Z ↑	0.0318	0.0317	2.7492	2.0970
E to Z ↓	0.0120	0.0120	1.2629	0.9523
E to Z ↑	0.0277	0.0278	2.7342	2.0837
F to Z ↓	0.0127	0.0121	1.2817	0.9666
F to Z ↑	0.0232	0.0229	2.7416	2.0944

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	6.426e-06	1.807e-09
X8_P16	1.208e-05	3.132e-09
X13_P16	1.684e-05	3.795e-09
X17_P16	2.255e-05	4.954e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

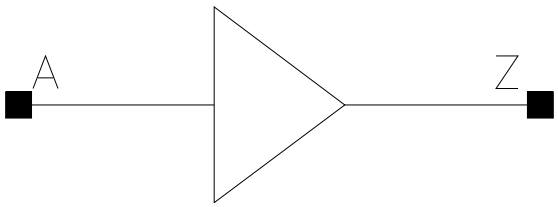
Pin Cycle (vdd)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	1.247e-04	2.783e-04	3.869e-04	5.072e-04
B (output stable)	2.224e-04	5.568e-04	6.797e-04	9.308e-04
C (output stable)	5.183e-05	1.182e-04	1.568e-04	2.193e-04
D (output stable)	7.119e-05	2.717e-04	2.966e-04	4.698e-04
E (output stable)	4.011e-05	1.013e-04	1.466e-04	2.003e-04
F (output stable)	5.158e-05	2.260e-04	2.694e-04	4.209e-04

A to Z	4.583e-03	9.658e-03	1.353e-02	1.784e-02
B to Z	4.165e-03	8.610e-03	1.216e-02	1.581e-02
C to Z	3.427e-03	7.463e-03	1.016e-02	1.350e-02
D to Z	3.045e-03	6.508e-03	8.895e-03	1.163e-02
E to Z	2.177e-03	4.840e-03	6.594e-03	8.717e-03
F to Z	1.820e-03	3.934e-03	5.359e-03	6.938e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	-1.402e-05	-2.988e-05	-3.264e-05	-4.332e-05
B (output stable)	-2.786e-05	-5.195e-05	-5.427e-05	-7.014e-05
C (output stable)	7.700e-06	1.401e-05	2.176e-05	2.928e-05
D (output stable)	1.426e-05	2.203e-05	2.895e-05	3.475e-05
E (output stable)	5.008e-05	1.116e-04	1.223e-04	1.677e-04
F (output stable)	4.454e-05	9.989e-05	1.104e-04	1.501e-04
A to Z	-6.158e-06	-1.226e-05	-1.218e-05	-1.519e-05
B to Z	-5.621e-06	-1.127e-05	-1.117e-05	-1.357e-05
C to Z	-2.033e-06	-5.198e-06	-4.398e-06	-6.848e-06
D to Z	-1.785e-06	-4.505e-06	-3.074e-06	-4.712e-06
E to Z	-5.435e-07	-1.204e-06	-1.213e-06	-1.684e-06
F to Z	-3.163e-07	-1.197e-06	-8.518e-07	-1.559e-06

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.408	0.4896
X6_P16	1.200	0.408	0.4896
X8_P16	1.200	0.408	0.4896
X13_P16	1.200	0.544	0.6528
X16_P16	1.200	0.544	0.6528
X21_P16	1.200	0.680	0.8160
X25_P16	1.200	0.680	0.8160
X29_P16	1.200	0.952	1.1424
X33_P16	1.200	0.952	1.1424
X42_P16	1.200	1.088	1.3056
X50_P16	1.200	1.224	1.4688
X58_P16	1.200	1.496	1.7952
X67_P16	1.200	1.632	1.9584
X75_P16	1.200	1.768	2.1216
X84_P16	1.200	1.904	2.2848
X100_P16	1.200	2.312	2.7744
X134_P16	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0009	0.0010	0.0010	0.0010
	X16_P16	X21_P16	X25_P16	X29_P16
A	0.0010	0.0014	0.0014	0.0018
	X33_P16	X42_P16	X50_P16	X58_P16
A	0.0018	0.0021	0.0025	0.0037

	X67_P16	X75_P16	X84_P16	X100_P16
A	0.0037	0.0037	0.0037	0.0048
	X134_P16			
A	0.0060			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0269	0.0272	3.4380	2.5433
A to Z ↑	0.0199	0.0198	6.1488	4.5813
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0285	0.0326	1.8998	1.2223
A to Z ↑	0.0207	0.0237	3.3133	2.1439
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0354	0.0297	0.9788	0.7502
A to Z ↑	0.0254	0.0218	1.6613	1.2924
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0312	0.0297	0.6469	0.5459
A to Z ↑	0.0226	0.0210	1.0917	0.9257
	X33_P16	**X42_P16**	**X33_P16**	**X42_P16**
A to Z ↓	0.0312	0.0307	0.4852	0.3933
A to Z ↑	0.0221	0.0224	0.8168	0.6567
	X50_P16	**X58_P16**	**X50_P16**	**X58_P16**
A to Z ↓	0.0301	0.0278	0.3265	0.2814
A to Z ↑	0.0219	0.0204	0.5457	0.4688
	X67_P16	**X75_P16**	**X67_P16**	**X75_P16**
A to Z ↓	0.0294	0.0310	0.2473	0.2235
A to Z ↑	0.0215	0.0227	0.4107	0.3673
	X84_P16	**X100_P16**	**X84_P16**	**X100_P16**
A to Z ↓	0.0324	0.0303	0.2027	0.1703
A to Z ↑	0.0237	0.0223	0.3318	0.2778
	X134_P16		**X134_P16**	
A to Z ↓	0.0319		0.1329	
A to Z ↑	0.0237		0.2126	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	2.686e-06	9.792e-10
X6_P16	3.204e-06	9.792e-10
X8_P16	3.818e-06	9.792e-10
X13_P16	4.992e-06	1.145e-09
X16_P16	5.955e-06	1.145e-09
X21_P16	8.034e-06	1.310e-09
X25_P16	8.869e-06	1.310e-09
X29_P16	1.066e-05	1.642e-09
X33_P16	1.138e-05	1.642e-09
X42_P16	1.393e-05	1.807e-09
X50_P16	1.666e-05	1.973e-09
X58_P16	2.055e-05	2.304e-09
X67_P16	2.250e-05	2.470e-09
X75_P16	2.445e-05	2.635e-09

X84_P16	2.640e-05	2.801e-09
X100_P16	3.226e-05	3.298e-09
X134_P16	4.201e-05	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	2.258e-03	2.548e-03	3.051e-03	4.179e-03
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	5.093e-03	6.787e-03	7.620e-03	8.653e-03
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	9.646e-03	1.212e-02	1.431e-02	1.718e-02
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	1.932e-02	2.171e-02	2.402e-02	2.845e-02
	X134_P16			
A to Z	3.933e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

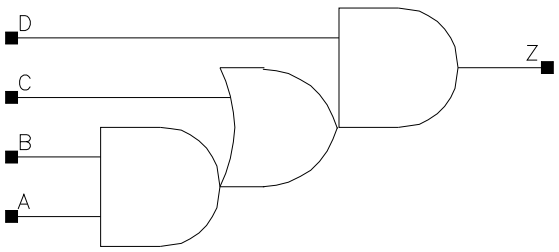
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	1.532e-07	-8.870e-08	-7.080e-08	9.120e-08
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	-2.707e-07	-1.691e-07	-1.450e-07	-1.929e-07
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	-2.366e-07	-2.590e-07	-6.790e-07	2.190e-07
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	-9.284e-07	-7.000e-07	-7.660e-07	-1.042e-06
	X134_P16			
A to Z	-1.300e-06			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.632	1.9584
X25_P16	1.200	1.768	2.1216
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0012	0.0025	0.0025	0.0025
B	0.0012	0.0023	0.0023	0.0023
C	0.0013	0.0027	0.0027	0.0027
D	0.0018	0.0025	0.0025	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0379	0.0361	1.9491	0.9635
A to Z ↑	0.0316	0.0299	3.3554	1.6335
B to Z ↓	0.0345	0.0325	1.9418	0.9616
B to Z ↑	0.0321	0.0299	3.3574	1.6346
C to Z ↓	0.0319	0.0297	1.9359	0.9596
C to Z ↑	0.0236	0.0216	3.3297	1.6215

D to Z ↓	0.0312	0.0278	1.9137	0.9491
D to Z ↑	0.0271	0.0237	3.3331	1.6240
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0400	0.0427	0.6567	0.4959
A to Z ↑	0.0333	0.0354	1.1067	0.8314
B to Z ↓	0.0365	0.0398	0.6552	0.4950
B to Z ↑	0.0334	0.0360	1.1062	0.8309
C to Z ↓	0.0337	0.0369	0.6534	0.4930
C to Z ↑	0.0245	0.0266	1.0952	0.8220
D to Z ↓	0.0304	0.0321	0.6437	0.4840
D to Z ↑	0.0263	0.0280	1.0971	0.8236

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	6.293e-06	1.642e-09
X17_P16	1.192e-05	2.470e-09
X25_P16	1.365e-05	2.635e-09
X33_P16	1.539e-05	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	1.451e-04	2.976e-04	2.997e-04	2.777e-04
B (output stable)	1.644e-04	3.577e-04	3.591e-04	3.084e-04
C (output stable)	3.936e-04	6.659e-04	6.688e-04	6.374e-04
D (output stable)	1.177e-04	1.708e-04	1.722e-04	1.720e-04
A to Z	5.168e-03	9.574e-03	1.215e-02	1.435e-02
B to Z	4.744e-03	8.539e-03	1.109e-02	1.341e-02
C to Z	3.986e-03	6.971e-03	9.424e-03	1.159e-02
D to Z	5.246e-03	9.215e-03	1.159e-02	1.356e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

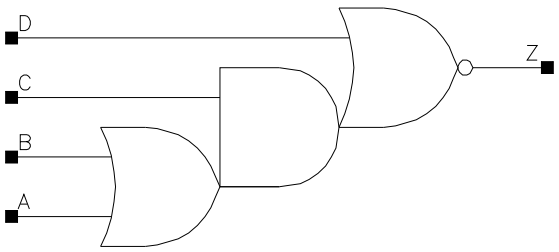
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	-1.580e-06	-3.032e-06	-3.016e-06	-2.804e-06
B (output stable)	-1.458e-06	-2.804e-06	-2.809e-06	-2.665e-06
C (output stable)	1.257e-05	2.141e-05	2.148e-05	2.198e-05
D (output stable)	9.430e-08	-1.210e-08	1.237e-08	4.070e-08
A to Z	-9.100e-07	-1.970e-06	-2.394e-06	-2.402e-06
B to Z	-5.890e-07	-1.401e-06	-1.161e-06	-2.050e-06
C to Z	-2.227e-07	-2.941e-07	-5.826e-07	-6.503e-07
D to Z	-3.592e-07	-2.776e-07	-4.486e-07	-3.304e-07

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.952	1.1424
X11_P16	1.200	1.496	1.7952
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X16_P16	X21_P16
A	0.0011	0.0021	0.0032	0.0042
B	0.0011	0.0020	0.0032	0.0041
C	0.0011	0.0021	0.0031	0.0042
D	0.0014	0.0021	0.0031	0.0041

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0139	0.0133	3.1514	1.6552
A to Z ↑	0.0369	0.0346	9.1284	4.7491
B to Z ↓	0.0133	0.0130	3.0723	1.6236
B to Z ↑	0.0349	0.0332	9.1386	4.7535
C to Z ↓	0.0129	0.0123	2.9295	1.5395
C to Z ↑	0.0221	0.0205	6.1798	3.1715

D to Z ↓	0.0072	0.0059	1.9594	0.9899
D to Z ↑	0.0196	0.0174	6.6165	3.4016
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0133	0.0137	1.1151	0.8585
A to Z ↑	0.0323	0.0342	3.0525	2.3531
B to Z ↓	0.0126	0.0130	1.1203	0.8588
B to Z ↑	0.0317	0.0325	3.0555	2.3550
C to Z ↓	0.0125	0.0126	1.0556	0.8082
C to Z ↑	0.0199	0.0201	2.0970	1.5731
D to Z ↓	0.0059	0.0060	0.6892	0.5251
D to Z ↑	0.0164	0.0163	2.2309	1.6870

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P16	5.056e-06	1.642e-09
X11_P16	9.566e-06	2.304e-09
X16_P16	1.305e-05	2.635e-09
X21_P16	1.758e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	6.128e-05	1.112e-04	1.436e-04	2.393e-04
B (output stable)	6.104e-06	1.567e-05	9.183e-06	2.984e-05
C (output stable)	2.684e-04	5.206e-04	6.988e-04	1.042e-03
D (output stable)	7.356e-05	1.499e-04	1.921e-04	2.990e-04
A to Z	3.660e-03	6.498e-03	9.165e-03	1.287e-02
B to Z	2.946e-03	5.285e-03	7.676e-03	1.037e-02
C to Z	2.456e-03	4.276e-03	6.198e-03	8.497e-03
D to Z	1.474e-03	2.547e-03	3.497e-03	4.651e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

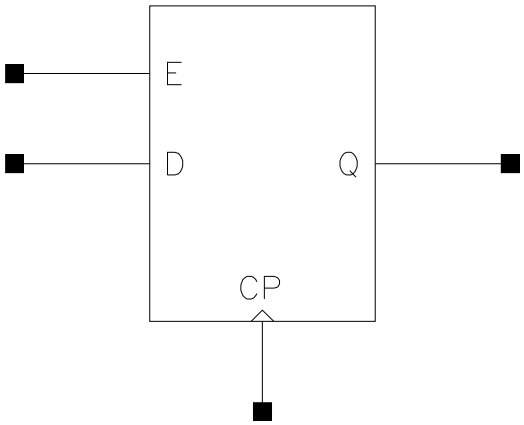
Pin Cycle (vdds)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	-5.215e-06	-7.553e-06	-9.138e-06	-1.679e-05
B (output stable)	1.339e-05	1.691e-05	2.897e-05	4.185e-05
C (output stable)	-2.136e-05	-3.660e-05	-4.798e-05	-7.778e-05
D (output stable)	7.217e-05	1.563e-04	2.124e-04	2.981e-04
A to Z	-2.588e-06	-4.056e-06	-2.520e-06	-6.799e-06
B to Z	-7.400e-07	-9.760e-07	-8.740e-07	-1.952e-06
C to Z	-6.617e-07	-4.737e-07	-7.983e-07	1.472e-06
D to Z	2.141e-06	-2.360e-08	-1.156e-07	-1.123e-06

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.128	3.7536
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008
E	0.0013	0.0013	0.0010

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0431	0.0505	1.9509	1.0112
CP to Q ↑	0.0527	0.0568	3.3609	1.6821
	X33_P16		**X33_P16**	
CP to Q ↓	0.0765		0.4922	
CP to Q ↑	0.0923		0.8331	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0604	0.0604	0.0604
CP ↑	min_pulse_width to CP	0.0349	0.0434	0.0301
D ↓	hold_rising to CP	-0.0237	-0.0212	-0.0237
D ↑	hold_rising to CP	-0.0039	-0.0043	-0.0039
D ↓	setup_rising to CP	0.0610	0.0610	0.0610
D ↑	setup_rising to CP	0.0313	0.0313	0.0313
E ↓	hold_rising to CP	-0.0161	-0.0161	-0.0161
E ↑	hold_rising to CP	-0.0043	-0.0043	-0.0043
E ↓	setup_rising to CP	0.0601	0.0601	0.0601
E ↑	setup_rising to CP	0.0637	0.0637	0.0637

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	1.735e-05	4.126e-09
X17_P16	1.947e-05	4.292e-09
X33_P16	2.604e-05	4.954e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

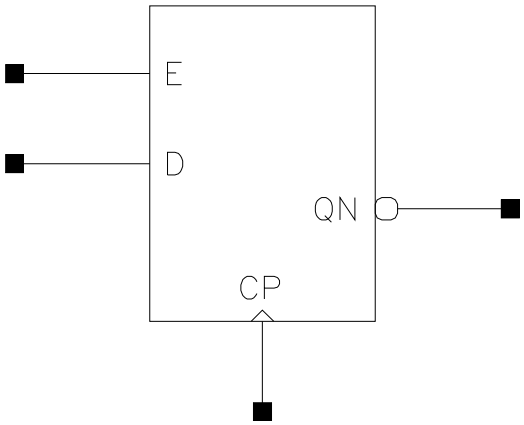
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.400e-03	5.401e-03	5.408e-03
Clock 100Mhz Data 25Mhz	1.162e-02	1.279e-02	1.655e-02
Clock 100Mhz Data 50Mhz	1.785e-02	2.019e-02	2.769e-02
Clock = 0 Data 100Mhz	7.101e-03	7.102e-03	7.103e-03
Clock = 1 Data 100Mhz	1.898e-03	1.898e-03	1.898e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.264	3.9168
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008
E	0.0010	0.0013	0.0013

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.0744	0.0703	1.9975	0.9511
CP to QN ↑	0.0580	0.0599	3.3991	1.6371
	X33_P16		**X33_P16**	
CP to QN ↓	0.0761		0.4935	
CP to QN ↑	0.0670		0.8351	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0604	0.0604	0.0604
CP ↑	min_pulse_width to CP	0.0301	0.0301	0.0349
D ↓	hold_rising to CP	-0.0237	-0.0237	-0.0237
D ↑	hold_rising to CP	-0.0039	-0.0039	-0.0043
D ↓	setup_rising to CP	0.0610	0.0610	0.0610
D ↑	setup_rising to CP	0.0344	0.0313	0.0313
E ↓	hold_rising to CP	-0.0161	-0.0161	-0.0161
E ↑	hold_rising to CP	-0.0068	-0.0043	-0.0043
E ↓	setup_rising to CP	0.0601	0.0601	0.0601
E ↑	setup_rising to CP	0.0637	0.0637	0.0637

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	1.722e-05	4.126e-09
X17_P16	2.046e-05	4.457e-09
X33_P16	2.554e-05	4.954e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

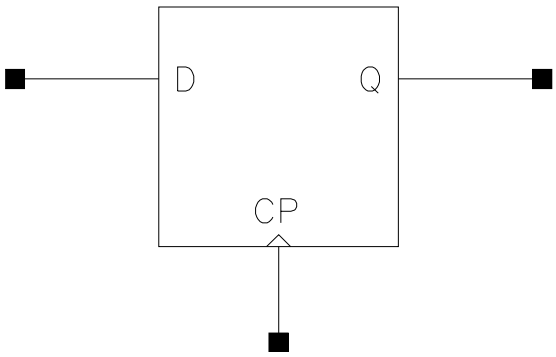
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.394e-03	5.396e-03	5.397e-03
Clock 100Mhz Data 25Mhz	1.167e-02	1.338e-02	1.631e-02
Clock 100Mhz Data 50Mhz	1.795e-02	2.137e-02	2.722e-02
Clock = 0 Data 100Mhz	7.102e-03	7.102e-03	7.103e-03
Clock = 1 Data 100Mhz	1.898e-03	1.898e-03	1.898e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.176	2.6112
X17_P16	1.200	2.448	2.9376
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0012	0.0012	0.0012	0.0012
D	0.0009	0.0009	0.0009	0.0009

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0450	0.0505	1.9460	1.0017
CP to Q ↑	0.0531	0.0594	3.2654	1.6562
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to Q ↓	0.0654	0.0682	0.5978	0.5440
CP to Q ↑	0.0679	0.0695	0.9288	0.8489

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0556	0.0556	0.0556	0.0556
CP ↑	min_pulse_width to CP	0.0338	0.0397	0.0531	0.0579
D ↓	hold_rising to CP	0.0078	0.0053	0.0053	0.0053
D ↑	hold_rising to CP	0.0103	0.0103	0.0103	0.0103
D ↓	setup_rising to CP	0.0317	0.0339	0.0339	0.0339
D ↑	setup_rising to CP	0.0145	0.0145	0.0145	0.0145

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	1.396e-05	3.132e-09
X17_P16	1.617e-05	3.464e-09
X30_P16	1.953e-05	3.795e-09
X33_P16	2.015e-05	3.795e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

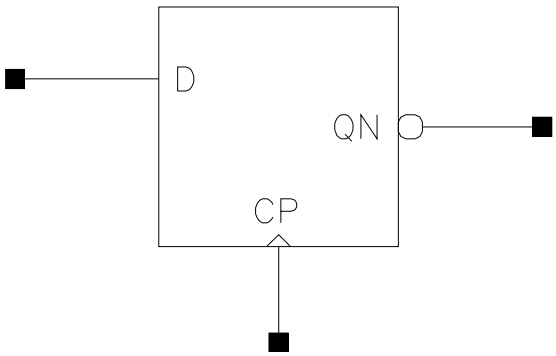
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.652e-03	5.691e-03	5.705e-03	5.710e-03
Clock 100Mhz Data 25Mhz	1.029e-02	1.190e-02	1.462e-02	1.530e-02
Clock 100Mhz Data 50Mhz	1.492e-02	1.811e-02	2.353e-02	2.488e-02
Clock = 0 Data 100Mhz	4.827e-03	4.973e-03	5.018e-03	5.040e-03
Clock = 1 Data 100Mhz	3.209e-05	3.192e-05	3.203e-05	3.203e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0012	0.0012	0.0012	0.0012
D	0.0009	0.0009	0.0009	0.0009

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.0437	0.0513	2.0024	1.0386
CP to QN ↑	0.0460	0.0494	3.2619	1.6563
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to QN ↓	0.0758	0.0762	0.5434	0.4928
CP to QN ↑	0.0621	0.0716	0.8987	0.8339

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0470	0.0507	0.0556	0.0556
CP ↑	min_pulse_width to CP	0.0301	0.0386	0.0338	0.0397
D ↓	hold_rising to CP	0.0127	0.0127	0.0056	0.0078
D ↑	hold_rising to CP	0.0124	0.0124	0.0103	0.0103
D ↓	setup_rising to CP	0.0245	0.0242	0.0339	0.0317
D ↑	setup_rising to CP	0.0175	0.0175	0.0145	0.0145

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	1.279e-05	2.801e-09
X17_P16	1.495e-05	2.967e-09
X30_P16	2.083e-05	3.795e-09
X33_P16	2.220e-05	3.961e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

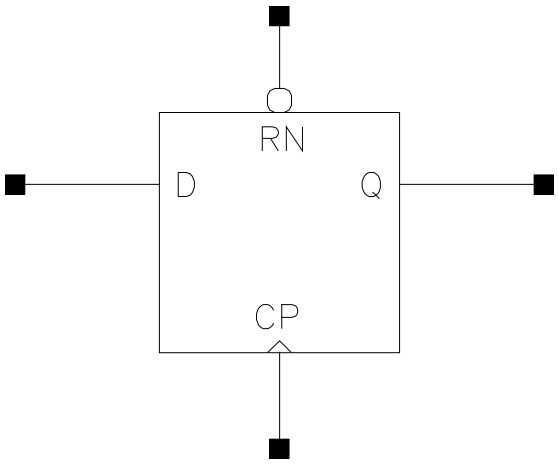
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.463e-03	5.463e-03	5.549e-03	5.582e-03
Clock 100Mhz Data 25Mhz	9.763e-03	1.101e-02	1.421e-02	1.495e-02
Clock 100Mhz Data 50Mhz	1.406e-02	1.655e-02	2.286e-02	2.432e-02
Clock = 0 Data 100Mhz	4.162e-03	4.162e-03	4.478e-03	4.567e-03
Clock = 1 Data 100Mhz	3.203e-05	3.207e-05	3.222e-05	3.240e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0012	0.0012
D	0.0009	0.0009
RN	0.0011	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0527	0.0674	1.0110	0.6071
CP to Q ↑	0.0610	0.0694	1.6603	0.9323
RN to Q ↓	0.0699	0.0792	0.9751	0.5792

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0604	0.0604
CP ↑	min_pulse_width to CP	0.0434	0.0542
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0104	0.0104
D ↓	setup_rising to CP	0.0366	0.0366
D ↑	setup_rising to CP	0.0197	0.0197
RN ↓	min_pulse_width to RN	0.1072	0.1365
RN ↑	recovery_rising to CP	0.0197	0.0197
RN ↑	removal_rising to CP	-0.0049	-0.0049

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P16	1.772e-05	4.292e-09
X30_P16	2.068e-05	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

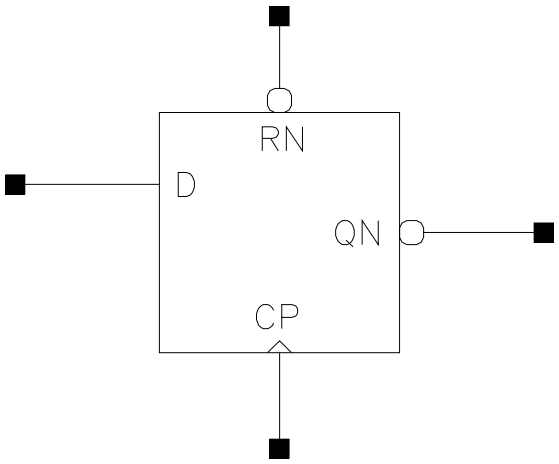
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	6.032e-03	6.031e-03
Clock 100Mhz Data 25Mhz	1.263e-02	1.530e-02
Clock 100Mhz Data 50Mhz	1.923e-02	2.457e-02
Clock = 0 Data 100Mhz	5.817e-03	5.820e-03
Clock = 1 Data 100Mhz	3.262e-05	3.265e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0012	0.0012
D	0.0009	0.0009
RN	0.0011	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.0716	0.0781	0.9419	0.5450
CP to QN ↑	0.0596	0.0646	1.6248	0.9011
RN to QN ↑	0.0797	0.0841	1.6240	0.9005

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0604	0.0604
CP ↑	min_pulse_width to CP	0.0349	0.0349
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0107	0.0107
D ↓	setup_rising to CP	0.0366	0.0366
D ↑	setup_rising to CP	0.0197	0.0197
RN ↓	min_pulse_width to RN	0.0850	0.0876
RN ↑	recovery_rising to CP	0.0201	0.0201
RN ↑	removal_rising to CP	-0.0049	-0.0049

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P16	2.003e-05	4.292e-09
X30_P16	2.370e-05	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

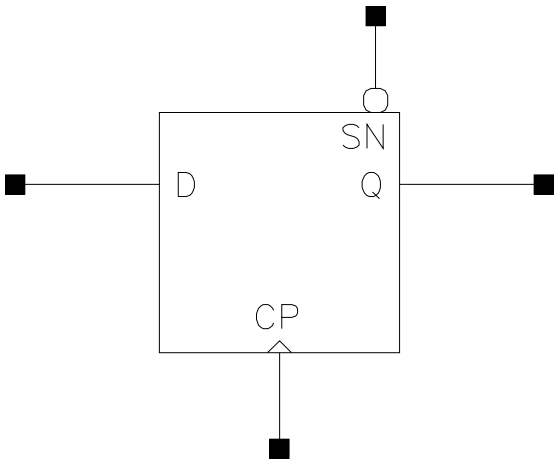
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	6.030e-03	6.029e-03
Clock 100Mhz Data 25Mhz	1.316e-02	1.512e-02
Clock 100Mhz Data 50Mhz	2.030e-02	2.422e-02
Clock = 0 Data 100Mhz	5.886e-03	5.865e-03
Clock = 1 Data 100Mhz	3.217e-05	3.249e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0012	0.0012
D	0.0009	0.0009
SN	0.0015	0.0015

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0526	0.0680	1.0115	0.6043
CP to Q ↑	0.0605	0.0692	1.6619	0.9323
SN to Q ↑	0.0496	0.0549	1.6416	0.9155

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0653	0.0653
CP ↑	min_pulse_width to CP	0.0434	0.0579
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0104	0.0104
D ↓	setup_rising to CP	0.0419	0.0419
D ↑	setup_rising to CP	0.0172	0.0172
SN ↓	min_pulse_width to SN	0.0598	0.0723
SN ↑	recovery_rising to CP	0.0082	0.0082
SN ↑	removal_rising to CP	0.0312	0.0312

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P16	1.890e-05	4.292e-09
X30_P16	2.257e-05	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

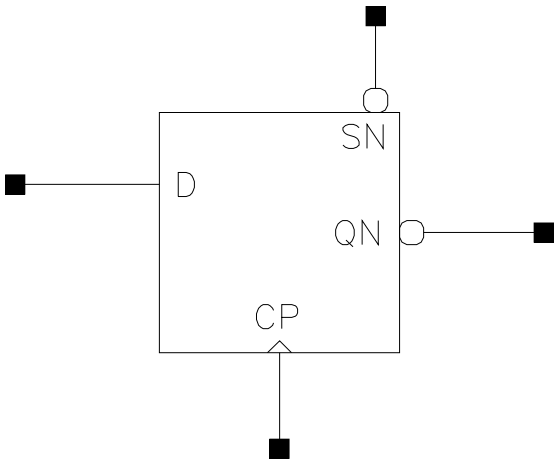
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	6.090e-03	6.076e-03
Clock 100Mhz Data 25Mhz	1.269e-02	1.537e-02
Clock 100Mhz Data 50Mhz	1.928e-02	2.466e-02
Clock = 0 Data 100Mhz	5.751e-03	5.751e-03
Clock = 1 Data 100Mhz	3.187e-05	3.194e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0012	0.0012
D	0.0009	0.0009
SN	0.0015	0.0015

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.0709	0.0775	0.9435	0.5460
CP to QN ↑	0.0598	0.0647	1.6232	0.9007
SN to QN ↓	0.0609	0.0672	0.9431	0.5456

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0653	0.0653
CP ↑	min_pulse_width to CP	0.0349	0.0349
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0104	0.0104
D ↓	setup_rising to CP	0.0419	0.0419
D ↑	setup_rising to CP	0.0172	0.0172
SN ↓	min_pulse_width to SN	0.0522	0.0522
SN ↑	recovery_rising to CP	0.0085	0.0082
SN ↑	removal_rising to CP	0.0312	0.0312

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P16	1.920e-05	4.292e-09
X30_P16	2.212e-05	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

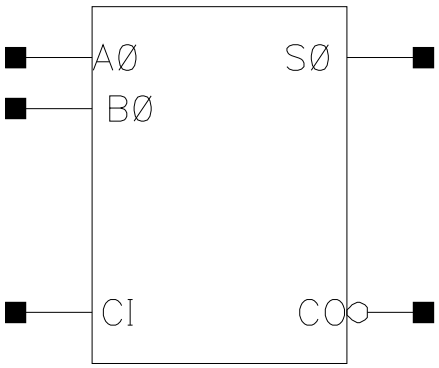
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	6.088e-03	6.083e-03
Clock 100Mhz Data 25Mhz	1.319e-02	1.516e-02
Clock 100Mhz Data 50Mhz	2.028e-02	2.423e-02
Clock = 0 Data 100Mhz	5.752e-03	5.752e-03
Clock = 1 Data 100Mhz	3.246e-05	3.258e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_-P16	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_-P16	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_-P16	1.200	3.672	4.4064
C12T28SOI_LRS1_-FA1X33_P16	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16
A0	0.0040	0.0082	0.0035	0.0068
B0	0.0036	0.0077	0.0038	0.0066
CI	0.0027	0.0059	0.0026	0.0047

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16
A0 to CO ↓	0.0501	0.0555	2.0324	0.5345
A0 to CO ↑	0.0341	0.0360	3.3624	0.8622
A0 to S0 ↓	0.0509	0.0648	1.9900	0.5195
A0 to S0 ↑	0.0524	0.0646	3.3271	0.8483
B0 to CO ↓	0.0495	0.0558	2.0414	0.5381
B0 to CO ↑	0.0354	0.0378	3.3652	0.8597
B0 to S0 ↓	0.0514	0.0660	1.9893	0.5194
B0 to S0 ↑	0.0525	0.0655	3.3281	0.8491
CI to CO ↓	0.0476	0.0543	2.0450	0.5374
CI to CO ↑	0.0352	0.0370	3.3634	0.8625
CI to S0 ↓	0.0508	0.0653	1.9893	0.5194
CI to S0 ↑	0.0524	0.0657	3.3271	0.8487
	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16
A0 to CO ↓	0.0320	0.0398	3.7148	0.6446
A0 to CO ↑	0.0259	0.0302	3.3973	0.8431
A0 to S0 ↓	0.0655	0.0817	2.1426	0.5422
A0 to S0 ↑	0.0603	0.0660	3.4568	0.8630
B0 to CO ↓	0.0329	0.0413	3.7184	0.6459
B0 to CO ↑	0.0238	0.0287	3.3947	0.8432
B0 to S0 ↓	0.0661	0.0841	2.1419	0.5422
B0 to S0 ↑	0.0610	0.0683	3.4553	0.8627
CI to CO ↓	0.0325	0.0578	3.7100	0.6578
CI to CO ↑	0.0261	0.0326	3.4753	0.8496
CI to S0 ↓	0.0369	0.0490	2.1448	0.5430
CI to S0 ↑	0.0321	0.0326	3.4556	0.8631

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_FA1X8_P16	1.591e-05	3.132e-09
C12T28SOI_LR_FA1X33_P16	3.946e-05	6.445e-09
C12T28SOI_LRS1_FA1X8_P16	2.697e-05	4.954e-09
C12T28SOI_LRS1_FA1X33_P16	6.190e-05	1.025e-08

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16
A0 to CO	5.501e-03	1.596e-02	8.055e-03	2.059e-02
A0 to S0	5.531e-03	1.654e-02	1.081e-02	2.560e-02
B0 to CO	5.479e-03	1.607e-02	8.155e-03	2.097e-02
B0 to S0	5.279e-03	1.612e-02	1.105e-02	2.628e-02
CI to CO	5.446e-03	1.607e-02	5.756e-03	1.875e-02
CI to S0	5.230e-03	1.604e-02	6.542e-03	2.014e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16
A0 to CO	-9.859e-06	-1.909e-05	5.045e-06	1.136e-05
A0 to S0	-7.665e-06	-1.458e-05	7.776e-06	1.558e-05
B0 to CO	4.695e-06	8.943e-06	-5.501e-07	-8.471e-07
B0 to S0	1.975e-05	3.847e-05	4.543e-06	7.921e-06
CI to CO	2.328e-05	4.501e-05	-3.244e-07	-1.205e-06
CI to S0	2.235e-05	3.913e-05	-4.420e-07	-1.196e-06

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X33_P16	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X33_P16
A0	0.0014	0.0040
B0	0.0012	0.0034

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
A0 to CO ↓	0.0375	0.0350	1.9864	0.4912
A0 to CO ↑	0.0316	0.0286	3.3344	0.8551
A0 to S0 ↓	0.0474	0.0459	1.9422	0.4910
A0 to S0 ↑	0.0451	0.0509	3.2957	0.8441
B0 to CO ↓	0.0363	0.0322	1.9818	0.4870
B0 to CO ↑	0.0341	0.0301	3.3346	0.8551
B0 to S0 ↓	0.0491	0.0457	1.9439	0.4911
B0 to S0 ↑	0.0443	0.0487	3.2936	0.8444

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	7.996e-06	1.973e-09
X33_P16	2.840e-05	4.126e-09

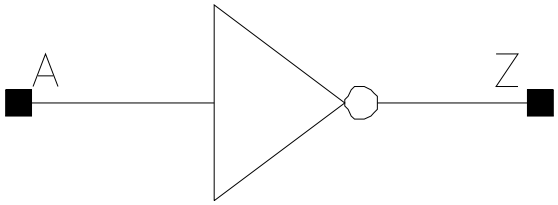
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X33_P16
A0 to CO	4.194e-03	1.399e-02
A0 to S0	3.865e-03	1.366e-02
B0 to CO	4.229e-03	1.397e-02
B0 to S0	3.767e-03	1.305e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X8_P16	X33_P16
A0 to CO	-3.575e-07	-3.641e-06
A0 to S0	-3.768e-07	-3.368e-06
B0 to CO	6.328e-06	4.305e-05
B0 to S0	3.032e-06	2.103e-05

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.272	0.3264
X6_P16	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X13_P16	1.200	0.408	0.4896
X17_P16	1.200	0.408	0.4896
X21_P16	1.200	0.544	0.6528
X25_P16	1.200	0.544	0.6528
X29_P16	1.200	0.680	0.8160
X33_P16	1.200	0.680	0.8160
X50_P16	1.200	0.952	1.1424
X58_P16	1.200	1.088	1.3056
X67_P16	1.200	1.224	1.4688
X75_P16	1.200	1.360	1.6320
X84_P16	1.200	1.496	1.7952
X100_P16	1.200	1.768	2.1216
X134_P16	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0007	0.0008	0.0011	0.0017
	X17_P16	X21_P16	X25_P16	X29_P16
A	0.0021	0.0027	0.0032	0.0037
	X33_P16	X50_P16	X58_P16	X67_P16
A	0.0041	0.0063	0.0073	0.0085
	X75_P16	X84_P16	X100_P16	X134_P16

A	0.0096	0.0109	0.0132	0.0182

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0065	0.0060	3.6136	2.8177
A to Z ↑	0.0135	0.0125	6.2844	4.7933
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0051	0.0043	1.9437	1.2496
A to Z ↑	0.0115	0.0107	3.3612	2.1895
	X17_P16	**X21_P16**	**X17_P16**	**X21_P16**
A to Z ↓	0.0042	0.0047	0.9630	0.7720
A to Z ↑	0.0102	0.0108	1.6523	1.3220
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0046	0.0043	0.6595	0.5589
A to Z ↑	0.0104	0.0101	1.1111	0.9453
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0042	0.0045	0.4953	0.3346
A to Z ↑	0.0099	0.0100	0.8321	0.5571
	X58_P16	**X67_P16**	**X58_P16**	**X67_P16**
A to Z ↓	0.0047	0.0047	0.2902	0.2549
A to Z ↑	0.0102	0.0101	0.4799	0.4204
	X75_P16	**X84_P16**	**X75_P16**	**X84_P16**
A to Z ↓	0.0052	0.0054	0.2300	0.2082
A to Z ↑	0.0105	0.0107	0.3763	0.3402
	X100_P16	**X134_P16**	**X100_P16**	**X134_P16**
A to Z ↓	0.0063	0.0071	0.1771	0.1381
A to Z ↑	0.0115	0.0123	0.2863	0.2194

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.410e-06	8.135e-10
X6_P16	1.749e-06	8.135e-10
X8_P16	2.491e-06	8.135e-10
X13_P16	3.818e-06	9.792e-10
X17_P16	4.848e-06	9.792e-10
X21_P16	5.956e-06	1.145e-09
X25_P16	6.869e-06	1.145e-09
X29_P16	8.009e-06	1.310e-09
X33_P16	8.820e-06	1.310e-09
X50_P16	1.271e-05	1.642e-09
X58_P16	1.466e-05	1.807e-09
X67_P16	1.661e-05	1.973e-09
X75_P16	1.856e-05	2.139e-09
X84_P16	2.051e-05	2.304e-09
X100_P16	2.441e-05	2.635e-09
X134_P16	3.221e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16

A to Z	6.403e-04	7.815e-04	1.015e-03	1.404e-03
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	1.789e-03	2.424e-03	2.790e-03	3.095e-03
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	3.445e-03	5.165e-03	6.150e-03	6.826e-03
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	7.902e-03	8.709e-03	1.078e-02	1.504e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

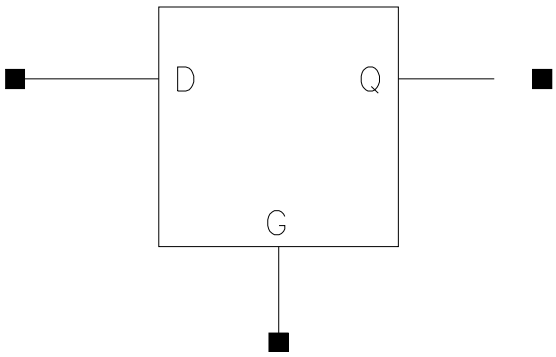
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	1.088e-06	1.444e-06	-7.790e-08	3.264e-07
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	-1.365e-07	-3.336e-07	-7.620e-07	-8.914e-07
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	-8.134e-07	-5.200e-08	-7.360e-07	3.044e-06
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	2.375e-06	3.640e-06	-2.910e-07	1.472e-05

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X23_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P16	X23_P16
D	0.0007	0.0017
G	0.0014	0.0022

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X23_P16	X8_P16	X23_P16
D to Q ↓	0.0567	0.0461	2.0534	0.9312
D to Q ↑	0.0341	0.0344	3.2858	0.8688
G to Q ↓	0.0579	0.0460	2.0504	0.9310
G to Q ↑	0.0332	0.0305	3.2870	0.8693

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P16	X23_P16
D ↓	hold_falling to G	-0.0140	-0.0069
D ↑	hold_falling to G	-0.0002	-0.0032
D ↓	setup_falling to G	0.0590	0.0419
D ↑	setup_falling to G	0.0348	0.0397
G ↑	min_pulse_width to G	0.0531	0.0420

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	7.387e-06	1.973e-09
X23_P16	1.319e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X23_P16
D (output stable)	2.286e-05	9.832e-05
G (output stable)	1.325e-03	2.612e-03
D to Q	6.753e-03	1.322e-02
G to Q	6.132e-03	1.161e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

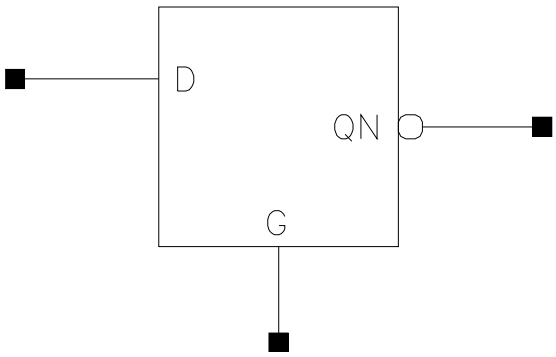
Pin Cycle (vdds)	X8_P16	X23_P16
D (output stable)	-5.992e-07	-2.829e-06
G (output stable)	1.139e-05	2.395e-05
D to Q	-1.284e-06	-2.888e-06
G to Q	3.889e-05	2.546e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P16
D	0.0007
G	0.0016

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P16	X17_P16
D to QN ↓	0.0468	0.9486
D to QN ↑	0.0635	1.6158
G to QN ↓	0.0452	0.9486
G to QN ↑	0.0624	1.6161

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P16
D ↓	hold_falling to G	-0.0219
D ↑	hold_falling to G	-0.0033
D ↓	setup_falling to G	0.0467
D ↑	setup_falling to G	0.0307
G ↑	min_pulse_width to G	0.0387

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P16	1.060e-05	2.139e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X17_P16
D (output stable)	2.542e-05
G (output stable)	1.501e-03
D to QN	8.484e-03
G to QN	7.694e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

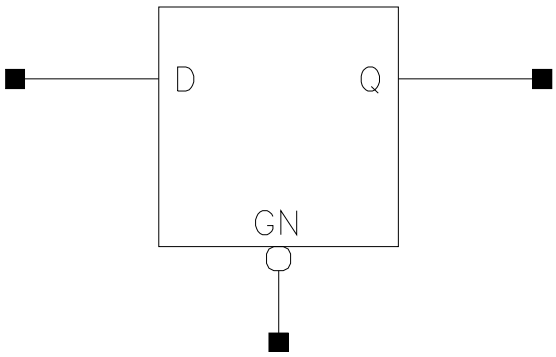
Pin Cycle (vdds)	X17_P16
D (output stable)	-1.162e-06
G (output stable)	1.211e-05
D to QN	-1.180e-06
G to QN	7.974e-05

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
D	0.0007	0.0010	0.0022
GN	0.0013	0.0017	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D to Q ↓	0.0572	0.0501	2.0626	1.0062
D to Q ↑	0.0348	0.0327	3.2865	1.6811
GN to Q ↓	0.0509	0.0440	2.0608	1.0083
GN to Q ↑	0.0532	0.0507	3.2860	1.6801

	X33_P16		X33_P16	
D to Q ↓	0.0485		0.5119	
D to Q ↑	0.0281		0.8436	
GN to Q ↓	0.0413		0.5127	
GN to Q ↑	0.0400		0.8420	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P16	X17_P16	X33_P16
D ↓	hold_rising to GN	-0.0163	-0.0115	-0.0118
D ↑	hold_rising to GN	0.0002	0.0058	0.0057
D ↓	setup_rising to GN	0.0667	0.0566	0.0545
D ↑	setup_rising to GN	0.0313	0.0292	0.0239
GN ↓	min_pulse_width to GN	0.0683	0.0626	0.0569

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	7.061e-06	1.973e-09
X17_P16	1.046e-05	2.304e-09
X33_P16	1.702e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
D (output stable)	2.413e-05	3.890e-05	1.081e-04
GN (output stable)	1.320e-03	1.781e-03	2.265e-03
D to Q	6.775e-03	9.683e-03	1.576e-02
GN to Q	9.392e-03	1.293e-02	1.928e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

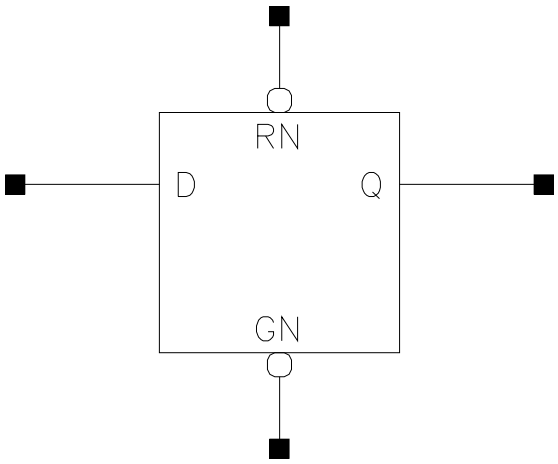
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
D (output stable)	-5.968e-07	-8.079e-07	-2.775e-06
GN (output stable)	1.121e-05	1.679e-05	2.677e-05
D to Q	-1.221e-06	-1.388e-06	-2.477e-06
GN to Q	-4.780e-05	-2.321e-05	-2.830e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.496	1.7952
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X33_P16
D	0.0007	0.0018
GN	0.0015	0.0027
RN	0.0007	0.0008

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
D to Q ↓	0.0535	0.0490	2.0030	0.5150
D to Q ↑	0.0451	0.0585	3.3449	0.8664

GN to Q ↓	0.0481	0.0444	2.0026	0.5156
GN to Q ↑	0.0605	0.0633	3.3465	0.8675
RN to Q ↓	0.0418	0.0729	1.8879	0.5296
RN to Q ↑	0.0477	0.0640	3.3468	0.8676

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P16	X33_P16
D ↓	hold_rising to GN	-0.0142	-0.0096
D ↑	hold_rising to GN	-0.0064	-0.0211
D ↓	setup_rising to GN	0.0563	0.0515
D ↑	setup_rising to GN	0.0441	0.0636
GN ↓	min_pulse_width to GN	0.0625	0.0644
RN ↓	min_pulse_width to RN	0.0518	0.0952
RN ↑	recovery_rising to GN	0.0468	0.0680
RN ↑	removal_rising to GN	-0.0291	-0.0486

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	6.952e-06	2.304e-09
X33_P16	1.488e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X33_P16
D (output stable)	1.263e-04	2.162e-04
GN (output stable)	1.554e-03	2.373e-03
RN (output stable)	4.713e-05	8.207e-05
D to Q	6.787e-03	1.797e-02
GN to Q	9.601e-03	2.214e-02
RN to Q	5.342e-03	1.458e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

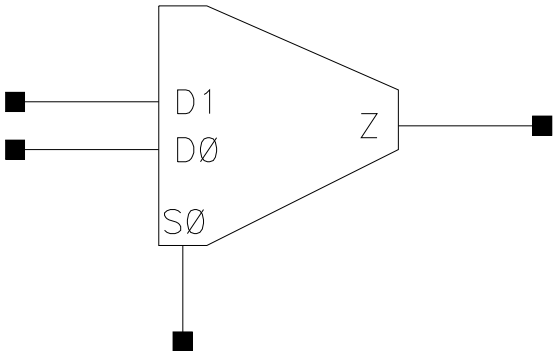
Pin Cycle (vdds)	X8_P16	X33_P16
D (output stable)	-1.572e-06	-2.332e-06
GN (output stable)	5.924e-06	1.248e-05
RN (output stable)	1.364e-07	2.899e-07
D to Q	-1.417e-06	-2.235e-06
GN to Q	-4.918e-05	5.856e-05
RN to Q	5.250e-06	-3.559e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
D0	0.0009	0.0013	0.0018	0.0024
D1	0.0009	0.0013	0.0018	0.0024
S0	0.0016	0.0017	0.0020	0.0030

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D0 to Z ↓	0.0412	0.0375	1.9927	0.9748
D0 to Z ↑	0.0320	0.0295	3.3621	1.6445
D1 to Z ↓	0.0396	0.0370	1.9893	0.9731
D1 to Z ↑	0.0294	0.0277	3.3547	1.6420
S0 to Z ↓	0.0354	0.0348	1.9813	0.9691
S0 to Z ↑	0.0339	0.0344	3.3571	1.6422

	X25_P16	X33_P16	X25_P16	X33_P16
D0 to Z ↓	0.0399	0.0362	0.6725	0.5024
D0 to Z ↑	0.0320	0.0293	1.1060	0.8278
D1 to Z ↓	0.0427	0.0377	0.6753	0.5040
D1 to Z ↑	0.0307	0.0283	1.1042	0.8275
S0 to Z ↓	0.0393	0.0360	0.6716	0.5017
S0 to Z ↑	0.0384	0.0352	1.1047	0.8275

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	7.839e-06	1.973e-09
X17_P16	1.277e-05	2.139e-09
X25_P16	1.808e-05	3.298e-09
X33_P16	2.432e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	1.138e-03	1.706e-03	1.904e-03	2.601e-03
D1 (output stable)	9.487e-04	1.596e-03	2.101e-03	2.712e-03
S0 (output stable)	1.563e-03	1.799e-03	2.365e-03	2.925e-03
D0 to Z	4.474e-03	7.449e-03	1.163e-02	1.463e-02
D1 to Z	4.165e-03	7.238e-03	1.175e-02	1.456e-02
S0 to Z	5.069e-03	7.887e-03	1.288e-02	1.581e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

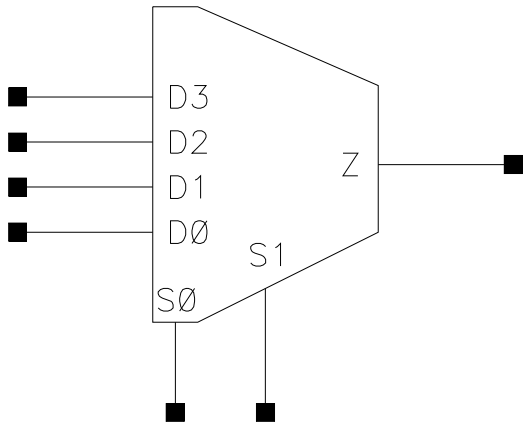
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	6.764e-07	9.650e-08	1.448e-06	1.597e-06
D1 (output stable)	1.151e-06	1.944e-06	3.082e-06	3.931e-06
S0 (output stable)	-1.200e-09	-7.640e-08	2.555e-07	-4.590e-08
D0 to Z	-1.400e-07	9.500e-09	2.815e-07	-6.695e-07
D1 to Z	-1.369e-07	2.270e-07	-3.910e-07	-4.045e-07
S0 to Z	1.159e-09	-1.961e-07	-2.691e-07	-1.248e-07

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.312	2.7744
X31_P16	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P16	X31_P16
D0	0.0007	0.0019
D1	0.0007	0.0018
D2	0.0007	0.0019
D3	0.0007	0.0018
S0	0.0023	0.0047
S1	0.0014	0.0028

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X31_P16	X8_P16	X31_P16

D0 to Z ↓	0.0753	0.0783	2.1200	0.5853
D0 to Z ↑	0.0458	0.0488	3.3845	0.9072
D1 to Z ↓	0.0748	0.0783	2.1173	0.5856
D1 to Z ↑	0.0461	0.0486	3.3858	0.9069
D2 to Z ↓	0.0805	0.0740	2.1319	0.5789
D2 to Z ↑	0.0482	0.0449	3.3913	0.9018
D3 to Z ↓	0.0803	0.0734	2.1319	0.5777
D3 to Z ↑	0.0477	0.0467	3.3892	0.9049
S0 to Z ↓	0.0821	0.0848	2.1229	0.5817
S0 to Z ↑	0.0584	0.0628	3.3895	0.9058
S1 to Z ↓	0.0576	0.0576	2.1244	0.5815
S1 to Z ↑	0.0446	0.0475	3.3864	0.9053

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	9.770e-06	3.298e-09
X31_P16	2.732e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X31_P16
D0 (output stable)	5.442e-05	2.418e-04
D1 (output stable)	5.309e-05	2.646e-04
D2 (output stable)	3.489e-05	1.187e-04
D3 (output stable)	5.570e-05	2.306e-04
S0 (output stable)	2.521e-03	6.016e-03
S1 (output stable)	1.731e-03	3.704e-03
D0 to Z	5.082e-03	1.765e-02
D1 to Z	5.072e-03	1.770e-02
D2 to Z	5.417e-03	1.662e-02
D3 to Z	5.402e-03	1.665e-02
S0 to Z	7.890e-03	2.390e-02
S1 to Z	5.638e-03	1.664e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

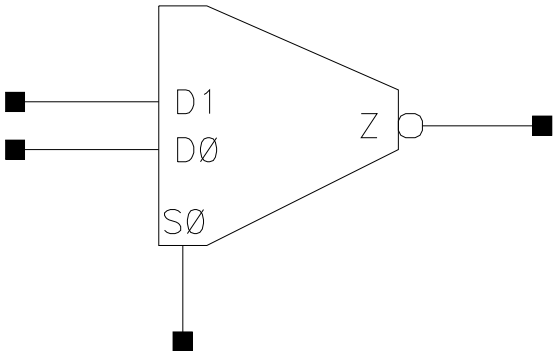
Pin Cycle (vdds)	X8_P16	X31_P16
D0 (output stable)	-1.246e-06	-8.890e-06
D1 (output stable)	-2.005e-07	-2.928e-06
D2 (output stable)	1.712e-06	1.120e-05
D3 (output stable)	-1.710e-06	1.953e-06
S0 (output stable)	-1.667e-05	-5.278e-05
S1 (output stable)	4.053e-05	1.599e-04
D0 to Z	-1.089e-06	-4.183e-06
D1 to Z	-1.861e-06	-3.720e-06
D2 to Z	-7.843e-07	-3.386e-06
D3 to Z	-6.212e-07	-1.840e-06
S0 to Z	-1.194e-05	-3.980e-05
S1 to Z	5.082e-05	2.052e-04

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.816	0.9792
X5_P16	1.200	0.952	1.1424
X10_P16	1.200	1.768	2.1216
X16_P16	1.200	2.448	2.9376
X21_P16	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P16	X5_P16	X10_P16	X16_P16
D0	0.0007	0.0010	0.0022	0.0032
D1	0.0007	0.0011	0.0021	0.0032
S0	0.0014	0.0024	0.0031	0.0047
	X21_P16			
D0	0.0043			
D1	0.0042			
S0	0.0053			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X5_P16	X3_P16	X5_P16
D0 to Z ↓	0.0127	0.0126	5.9267	3.7125

D0 to Z ↑	0.0252	0.0228	13.0975	6.8067
D1 to Z ↓	0.0124	0.0120	5.8791	3.5236
D1 to Z ↑	0.0262	0.0240	13.1049	7.0444
S0 to Z ↓	0.0211	0.0176	5.8957	3.6212
S0 to Z ↑	0.0235	0.0196	13.0740	6.9162
	X10_P16	**X16_P16**	**X10_P16**	**X16_P16**
D0 to Z ↓	0.0142	0.0131	1.7474	1.1409
D0 to Z ↑	0.0247	0.0236	3.1762	2.0929
D1 to Z ↓	0.0126	0.0124	1.6883	1.1134
D1 to Z ↑	0.0252	0.0245	3.2239	2.1124
S0 to Z ↓	0.0219	0.0188	1.7159	1.1262
S0 to Z ↑	0.0234	0.0202	3.1973	2.1022
	X21_P16		**X21_P16**	
D0 to Z ↓	0.0130		0.8717	
D0 to Z ↑	0.0231		1.5849	
D1 to Z ↓	0.0124		0.8444	
D1 to Z ↑	0.0247		1.5769	
S0 to Z ↓	0.0198		0.8575	
S0 to Z ↑	0.0208		1.5791	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P16	3.609e-06	1.476e-09
X5_P16	6.558e-06	1.642e-09
X10_P16	1.167e-05	2.635e-09
X16_P16	1.805e-05	3.464e-09
X21_P16	2.239e-05	4.292e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	2.432e-05	5.055e-05	1.555e-04	2.474e-04
D1 (output stable)	2.530e-05	1.355e-04	1.454e-04	2.443e-04
S0 (output stable)	1.315e-03	1.951e-03	3.392e-03	5.335e-03
D0 to Z	1.331e-03	2.221e-03	5.463e-03	7.741e-03
D1 to Z	1.329e-03	2.210e-03	5.204e-03	7.633e-03
S0 to Z	2.268e-03	3.305e-03	6.826e-03	9.723e-03
	X21_P16			
D0 (output stable)	3.196e-04			
D1 (output stable)	3.739e-04			
S0 (output stable)	5.907e-03			
D0 to Z	9.972e-03			
D1 to Z	1.012e-02			
S0 to Z	1.187e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	-6.036e-07	-8.817e-07	-3.199e-06	-7.766e-06
D1 (output stable)	-1.314e-06	-2.024e-05	-7.318e-06	-1.384e-05
S0 (output stable)	1.204e-05	4.906e-05	4.953e-05	8.864e-05
D0 to Z	-8.550e-08	8.045e-07	0.000e+00	-1.302e-06

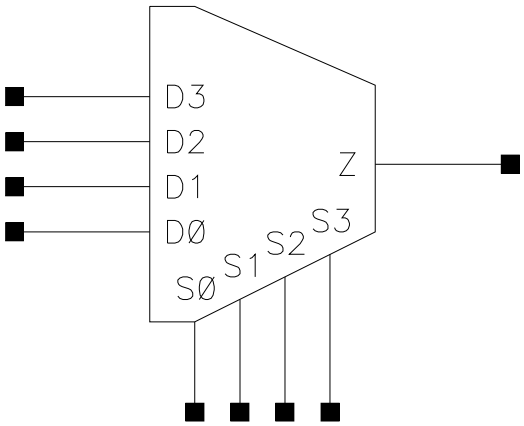
D1 to Z	-1.889e-07	-1.335e-06	3.950e-08	-1.275e-06
S0 to Z	1.243e-05	4.394e-05	5.122e-05	1.084e-04
	X21_P16			
D0 (output stable)	-9.429e-06			
D1 (output stable)	-3.114e-05			
S0 (output stable)	1.312e-04			
D0 to Z	1.979e-06			
D1 to Z	-8.600e-07			
S0 to Z	1.425e-04			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	1.768	2.1216
X27_P16	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P16	X27_P16
D0	0.0008	0.0025
D1	0.0008	0.0025
D2	0.0008	0.0025
D3	0.0008	0.0025
S0	0.0008	0.0024
S1	0.0009	0.0024
S2	0.0008	0.0024
S3	0.0009	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	X27_P16	X7_P16	X27_P16
D0 to Z ↓	0.0558	0.0480	3.1110	0.8487
D0 to Z ↑	0.0381	0.0329	3.3063	0.8237
D1 to Z ↓	0.0509	0.0441	3.1071	0.8480
D1 to Z ↑	0.0339	0.0286	3.2945	0.8213
D2 to Z ↓	0.0569	0.0466	3.1262	0.8508
D2 to Z ↑	0.0371	0.0305	3.3205	0.8275
D3 to Z ↓	0.0520	0.0428	3.1186	0.8490
D3 to Z ↑	0.0329	0.0263	3.3081	0.8245
S0 to Z ↓	0.0535	0.0450	3.1071	0.8482
S0 to Z ↑	0.0409	0.0349	3.3048	0.8242
S1 to Z ↓	0.0489	0.0410	3.1037	0.8472
S1 to Z ↑	0.0364	0.0301	3.2951	0.8212
S2 to Z ↓	0.0545	0.0435	3.1225	0.8495
S2 to Z ↑	0.0398	0.0325	3.3184	0.8274
S3 to Z ↓	0.0501	0.0397	3.1157	0.8478
S3 to Z ↑	0.0354	0.0279	3.3091	0.8244

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X7_P16	8.493e-06	2.635e-09
X27_P16	2.962e-05	4.954e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X7_P16	X27_P16
D0 (output stable)	7.474e-04	2.397e-03
D1 (output stable)	5.899e-04	1.867e-03
D2 (output stable)	6.948e-04	2.228e-03
D3 (output stable)	5.307e-04	1.691e-03
S0 (output stable)	7.424e-04	2.326e-03
S1 (output stable)	5.672e-04	1.788e-03
S2 (output stable)	6.545e-04	2.111e-03
S3 (output stable)	4.982e-04	1.602e-03
D0 to Z	5.660e-03	1.799e-02
D1 to Z	4.938e-03	1.551e-02
D2 to Z	5.423e-03	1.579e-02
D3 to Z	4.710e-03	1.334e-02
S0 to Z	5.474e-03	1.699e-02
S1 to Z	4.752e-03	1.458e-02
S2 to Z	5.234e-03	1.476e-02
S3 to Z	4.526e-03	1.240e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

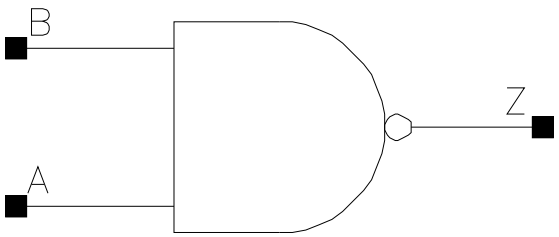
Pin Cycle (vdds)	X7_P16	X27_P16
D0 (output stable)	-2.082e-06	-3.653e-06
D1 (output stable)	5.350e-06	2.529e-05
D2 (output stable)	-4.127e-06	-6.018e-06
D3 (output stable)	1.127e-05	3.450e-05
S0 (output stable)	-5.427e-06	-8.804e-06
S1 (output stable)	1.148e-05	3.461e-05
S2 (output stable)	-1.922e-06	-3.251e-06
S3 (output stable)	8.756e-06	3.154e-05
D0 to Z	-2.536e-06	-3.191e-06
D1 to Z	-1.169e-07	-4.333e-07
D2 to Z	-2.201e-06	-2.694e-06
D3 to Z	-1.242e-07	-4.241e-07
S0 to Z	-2.508e-06	-2.816e-06
S1 to Z	-6.462e-08	-4.696e-07
S2 to Z	-2.191e-06	-2.369e-06
S3 to Z	-6.338e-08	-4.854e-07

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P16	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P16	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P16	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P16	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P16	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P16	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P16	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P16	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P16	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P16	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P16	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P16	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P16	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P16	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P16	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P16	C12T28SOI_LR_-NAND2X5_P16	C12T28SOI_LR_-NAND2X7_P16	C12T28SOI_LR_-NAND2X10_P16
A	0.0007	0.0009	0.0011	0.0017
B	0.0007	0.0009	0.0010	0.0016
	C12T28SOI_LR_-NAND2X13_P16	C12T28SOI_LR_-NAND2X17_P16	C12T28SOI_LR_-NAND2X20_P16	C12T28SOI_LR_-NAND2X24_P16
A	0.0021	0.0027	0.0031	0.0039
B	0.0020	0.0026	0.0030	0.0036
	C12T28SOI_LR_-NAND2X27_P16	C12T28SOI_LR_-NAND2X42_P16	C12T28SOI_LR_-NAND2X47_P16	C12T28SOI_LR_-NAND2X50_P16
A	0.0043	0.0013	0.0013	0.0013
B	0.0040	0.0013	0.0013	0.0013
	C12T28SOI_LR_-NAND2X58_P16	C12T28SOI_LR_-NAND2X67_P16	C12T28SOI_-LRBR0D8_-NAND2X7_P16	C12T28SOI_-LRBR0D8_-NAND2X14_P16
A	0.0013	0.0013	0.0010	0.0021
B	0.0013	0.0013	0.0010	0.0020
	C12T28SOI_LRS_-NAND2X40_P16	C12T28SOI_LRS_-NAND2X54_P16		
A	0.0064	0.0085		
B	0.0059	0.0080		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P16	**C12T28SOI_LR_-NAND2X5_P16**	**C12T28SOI_LR_-NAND2X3_P16**	**C12T28SOI_LR_-NAND2X5_P16**
A to Z ↓	0.0090	0.0079	5.7848	3.7676
A to Z ↑	0.0166	0.0152	6.2859	4.1017
B to Z ↓	0.0100	0.0085	5.8749	3.8205
B to Z ↑	0.0145	0.0128	6.3349	4.1336
	C12T28SOI_LR_-NAND2X7_P16	**C12T28SOI_LR_-NAND2X10_P16**	**C12T28SOI_LR_-NAND2X7_P16**	**C12T28SOI_LR_-NAND2X10_P16**
A to Z ↓	0.0078	0.0093	3.1711	2.0965
A to Z ↑	0.0148	0.0160	3.3449	2.1722
B to Z ↓	0.0084	0.0085	3.2114	2.1264
B to Z ↑	0.0124	0.0124	3.3769	2.1901
	C12T28SOI_LR_-NAND2X13_P16	**C12T28SOI_LR_-NAND2X17_P16**	**C12T28SOI_LR_-NAND2X13_P16**	**C12T28SOI_LR_-NAND2X17_P16**
A to Z ↓	0.0088	0.0087	1.6190	1.2830

A to Z ↑	0.0151	0.0153	1.6439	1.3163
B to Z ↓	0.0081	0.0085	1.6421	1.3001
B to Z ↑	0.0117	0.0122	1.6572	1.3258
	C12T28SOI_LR_-NAND2X20_P16	**C12T28SOI_LR_-NAND2X24_P16**	**C12T28SOI_LR_-NAND2X20_P16**	**C12T28SOI_LR_-NAND2X24_P16**
A to Z ↓	0.0085	0.0089	1.1067	0.9413
A to Z ↑	0.0148	0.0152	1.1056	0.9406
B to Z ↓	0.0085	0.0082	1.1226	0.9544
B to Z ↑	0.0119	0.0118	1.1152	0.9474
	C12T28SOI_LR_-NAND2X27_P16	**C12T28SOI_LR_-NAND2X42_P16**	**C12T28SOI_LR_-NAND2X27_P16**	**C12T28SOI_LR_-NAND2X42_P16**
A to Z ↓	0.0087	0.0391	0.8395	0.3949
A to Z ↑	0.0149	0.0427	0.8290	0.6555
B to Z ↓	0.0082	0.0407	0.8514	0.3954
B to Z ↑	0.0115	0.0407	0.8355	0.6555
	C12T28SOI_LR_-NAND2X47_P16	**C12T28SOI_LR_-NAND2X50_P16**	**C12T28SOI_LR_-NAND2X47_P16**	**C12T28SOI_LR_-NAND2X50_P16**
A to Z ↓	0.0405	0.0409	0.3513	0.3301
A to Z ↑	0.0435	0.0438	0.5697	0.5469
B to Z ↓	0.0422	0.0425	0.3514	0.3302
B to Z ↑	0.0416	0.0419	0.5698	0.5475
	C12T28SOI_LR_-NAND2X58_P16	**C12T28SOI_LR_-NAND2X67_P16**	**C12T28SOI_LR_-NAND2X58_P16**	**C12T28SOI_LR_-NAND2X67_P16**
A to Z ↓	0.0432	0.0450	0.2866	0.2526
A to Z ↑	0.0455	0.0467	0.4708	0.4137
B to Z ↓	0.0448	0.0466	0.2866	0.2524
B to Z ↑	0.0435	0.0447	0.4711	0.4140
	C12T28SOI_-LRBR0D8_-NAND2X7_P16	**C12T28SOI_-LRBR0D8_-NAND2X14_P16**	**C12T28SOI_-LRBR0D8_-NAND2X7_P16**	**C12T28SOI_-LRBR0D8_-NAND2X14_P16**
A to Z ↓	0.0060	0.0071	2.3967	1.2608
A to Z ↑	0.0181	0.0186	4.3919	2.1484
B to Z ↓	0.0059	0.0055	2.4452	1.2886
B to Z ↑	0.0145	0.0133	4.5257	2.1894
	C12T28SOI_LRS_-NAND2X40_P16	**C12T28SOI_LRS_-NAND2X54_P16**	**C12T28SOI_LRS_-NAND2X40_P16**	**C12T28SOI_LRS_-NAND2X54_P16**
A to Z ↓	0.0087	0.0087	0.5686	0.4307
A to Z ↑	0.0148	0.0148	0.5551	0.4181
B to Z ↓	0.0083	0.0085	0.5769	0.4365
B to Z ↑	0.0115	0.0116	0.5597	0.4216

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P16	1.689e-06	9.792e-10
C12T28SOI_LR_NAND2X5_P16	2.549e-06	9.792e-10
C12T28SOI_LR_NAND2X7_P16	3.007e-06	9.792e-10
C12T28SOI_LR_NAND2X10_P16	4.426e-06	1.310e-09
C12T28SOI_LR_NAND2X13_P16	5.671e-06	1.310e-09
C12T28SOI_LR_NAND2X17_P16	7.063e-06	1.642e-09
C12T28SOI_LR_NAND2X20_P16	8.190e-06	1.642e-09
C12T28SOI_LR_NAND2X24_P16	9.685e-06	1.973e-09
C12T28SOI_LR_NAND2X27_P16	1.072e-05	1.973e-09

C12T28SOI_LR_NAND2X42_P16	1.811e-05	2.139e-09
C12T28SOI_LR_NAND2X47_P16	1.989e-05	2.304e-09
C12T28SOI_LR_NAND2X50_P16	2.034e-05	2.304e-09
C12T28SOI_LR_NAND2X58_P16	2.257e-05	2.470e-09
C12T28SOI_LR_NAND2X67_P16	2.481e-05	2.635e-09
C12T28SOI_LRBR0D8_NAND2X7_-P16	3.570e-06	1.804e-09
C12T28SOI_LRBR0D8_NAND2X14_-P16	6.674e-06	2.156e-09
C12T28SOI_LRS_NAND2X40_P16	1.577e-05	2.635e-09
C12T28SOI_LRS_NAND2X54_P16	2.082e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P16	C12T28SOI_LR_-NAND2X5_P16	C12T28SOI_LR_-NAND2X7_P16	C12T28SOI_LR_-NAND2X10_P16
A (output stable)	1.527e-05	2.298e-05	2.756e-05	8.719e-05
B (output stable)	2.740e-05	4.298e-05	5.303e-05	3.886e-04
A to Z	9.219e-04	1.247e-03	1.486e-03	2.598e-03
B to Z	7.366e-04	9.628e-04	1.140e-03	1.761e-03
	C12T28SOI_LR_-NAND2X13_P16	C12T28SOI_LR_-NAND2X17_P16	C12T28SOI_LR_-NAND2X20_P16	C12T28SOI_LR_-NAND2X24_P16
A (output stable)	1.038e-04	1.273e-04	1.425e-04	1.948e-04
B (output stable)	4.410e-04	4.406e-04	4.846e-04	7.548e-04
A to Z	3.179e-03	4.020e-03	4.580e-03	5.592e-03
B to Z	2.171e-03	2.843e-03	3.269e-03	3.823e-03
	C12T28SOI_LR_-NAND2X27_P16	C12T28SOI_LR_-NAND2X42_P16	C12T28SOI_LR_-NAND2X47_P16	C12T28SOI_LR_-NAND2X50_P16
A (output stable)	2.032e-04	3.113e-05	3.114e-05	3.121e-05
B (output stable)	8.030e-04	6.565e-05	6.578e-05	6.576e-05
A to Z	6.150e-03	1.623e-02	1.760e-02	1.818e-02
B to Z	4.209e-03	1.588e-02	1.724e-02	1.782e-02
	C12T28SOI_LR_-NAND2X58_P16	C12T28SOI_LR_-NAND2X67_P16	C12T28SOI_-LRBR0D8_-NAND2X7_P16	C12T28SOI_-LRBR0D8_-NAND2X14_P16
A (output stable)	3.130e-05	3.141e-05	3.527e-05	1.297e-04
B (output stable)	6.592e-05	6.583e-05	7.082e-05	5.605e-04
A to Z	2.079e-02	2.307e-02	1.553e-03	3.352e-03
B to Z	2.044e-02	2.272e-02	1.081e-03	1.974e-03
	C12T28SOI_LRS_-NAND2X40_P16	C12T28SOI_LRS_-NAND2X54_P16		
A (output stable)	2.982e-04	3.921e-04		
B (output stable)	1.122e-03	1.416e-03		
A to Z	9.118e-03	1.207e-02		
B to Z	6.304e-03	8.375e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P16	C12T28SOI_LR_-NAND2X5_P16	C12T28SOI_LR_-NAND2X7_P16	C12T28SOI_LR_-NAND2X10_P16
A (output stable)	3.020e-08	-9.000e-10	-1.590e-08	-6.000e-08
B (output stable)	3.470e-08	1.580e-08	3.400e-09	-7.090e-08
A to Z	2.448e-07	1.768e-07	-5.900e-08	3.521e-07

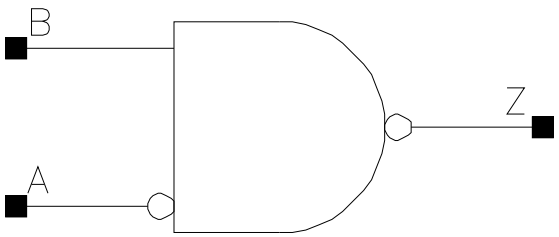
B to Z	2.228e-07	3.323e-07	5.339e-07	8.986e-07
	C12T28SOI_LR_-NAND2X13_P16	C12T28SOI_LR_-NAND2X17_P16	C12T28SOI_LR_-NAND2X20_P16	C12T28SOI_LR_-NAND2X24_P16
A (output stable)	-1.130e-07	-1.642e-07	-2.027e-07	-2.624e-07
B (output stable)	-2.051e-06	-1.746e-06	-1.935e-07	-3.812e-06
A to Z	1.323e-06	-6.210e-07	4.900e-08	1.521e-06
B to Z	-1.130e-07	1.788e-06	1.406e-06	2.128e-06
	C12T28SOI_LR_-NAND2X27_P16	C12T28SOI_LR_-NAND2X42_P16	C12T28SOI_LR_-NAND2X47_P16	C12T28SOI_LR_-NAND2X50_P16
A (output stable)	-3.263e-07	-8.530e-09	-7.540e-09	-7.590e-09
B (output stable)	-3.521e-06	2.580e-08	2.580e-08	2.680e-08
A to Z	1.744e-06	-2.710e-07	-8.030e-07	-6.750e-07
B to Z	3.530e-06	-4.630e-07	-5.330e-07	-5.280e-07
	C12T28SOI_LR_-NAND2X58_P16	C12T28SOI_LR_-NAND2X67_P16	C12T28SOI_-LRBR0D8_-NAND2X7_P16	C12T28SOI_-LRBR0D8_-NAND2X14_P16
A (output stable)	-7.360e-09	-6.020e-09	2.020e-08	-7.460e-08
B (output stable)	2.650e-08	2.710e-08	2.720e-08	-7.844e-06
A to Z	-6.970e-07	-6.090e-07	1.996e-07	1.088e-06
B to Z	-4.910e-07	-4.240e-07	9.558e-07	4.413e-07
	C12T28SOI_LRS_-NAND2X40_P16	C12T28SOI_LRS_-NAND2X54_P16		
A (output stable)	-5.091e-07	-6.573e-07		
B (output stable)	-4.594e-06	-5.982e-06		
A to Z	2.777e-06	3.282e-06		
B to Z	5.122e-06	3.020e-07		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X7_P16	1.200	0.544	0.6528
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X40_P16	1.200	2.312	2.7744
X54_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P16	X7_P16	X13_P16	X27_P16
A	0.0010	0.0010	0.0013	0.0025
B	0.0007	0.0010	0.0019	0.0039
	X40_P16	X54_P16		
A	0.0037	0.0049		
B	0.0058	0.0079		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0288	0.0309	5.7507	3.1511
A to Z ↑	0.0219	0.0231	6.1394	3.3042
B to Z ↓	0.0103	0.0084	5.9228	3.2320
B to Z ↑	0.0146	0.0123	6.3359	3.4023
	X13_P16	**X27_P16**	**X13_P16**	**X27_P16**

A to Z ↓	0.0293	0.0284	1.6946	0.8403
A to Z ↑	0.0223	0.0216	1.6922	0.8213
B to Z ↓	0.0080	0.0080	1.7403	0.8636
B to Z ↑	0.0116	0.0114	1.6956	0.8368
	X40_P16	**X54_P16**	**X40_P16**	**X54_P16**
A to Z ↓	0.0288	0.0288	0.5610	0.4255
A to Z ↑	0.0221	0.0220	0.5470	0.4127
B to Z ↓	0.0079	0.0080	0.5765	0.4369
B to Z ↑	0.0113	0.0113	0.5614	0.4233

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P16	2.888e-06	1.145e-09
X7_P16	4.219e-06	1.145e-09
X13_P16	8.160e-06	1.642e-09
X27_P16	1.539e-05	2.470e-09
X40_P16	2.241e-05	3.298e-09
X54_P16	2.941e-05	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	1.483e-03	1.924e-03	3.224e-03	6.236e-03
B (output stable)	2.940e-05	5.505e-05	4.053e-04	7.230e-04
A to Z	2.474e-03	3.469e-03	6.435e-03	1.259e-02
B to Z	7.465e-04	1.130e-03	2.116e-03	4.213e-03
	X40_P16	X54_P16		
A (output stable)	9.580e-03	1.267e-02		
B (output stable)	1.068e-03	1.394e-03		
A to Z	1.893e-02	2.509e-02		
B to Z	6.112e-03	8.069e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

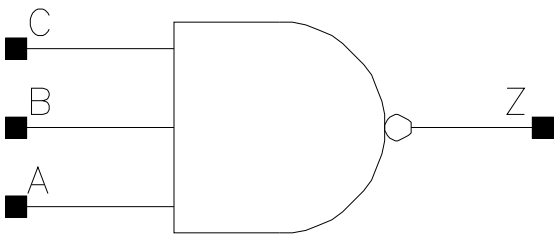
Pin Cycle (vdds)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	-2.360e-08	3.900e-08	1.540e-07	4.190e-08
B (output stable)	3.620e-08	3.400e-09	-9.070e-08	-2.313e-06
A to Z	-5.209e-08	5.700e-09	2.110e-08	7.400e-07
B to Z	3.730e-08	5.229e-07	9.480e-07	1.930e-07
	X40_P16	X54_P16		
A (output stable)	-1.430e-07	-4.600e-07		
B (output stable)	-3.680e-06	-5.693e-06		
A to Z	8.040e-07	1.264e-06		
B to Z	7.162e-06	8.620e-06		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P16	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P16	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P16	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P16	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P16	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P16	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P16	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P16	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P16	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P16	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P16	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P16	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P16	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P16	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P16	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A	0.0008	0.0011	0.0017	0.0021
B	0.0009	0.0011	0.0016	0.0020
C	0.0008	0.0010	0.0016	0.0020
	C12T28SOI_LR_-NAND3X15_P16	C12T28SOI_LR_-NAND3X18_P16	C12T28SOI_LR_-NAND3X21_P16	C12T28SOI_LR_-NAND3X24_P16
A	0.0027	0.0031	0.0038	0.0042
B	0.0026	0.0030	0.0036	0.0040
C	0.0025	0.0028	0.0035	0.0038
	C12T28SOI_LR_-NAND3X35_P16	C12T28SOI_LR_-NAND3X47_P16	C12T28SOI_-LRBR0P6_-NAND3X6_P16	C12T28SOI_-LRBR0P6_-NAND3X12_P16
A	0.0063	0.0085	0.0011	0.0021
B	0.0060	0.0080	0.0011	0.0020
C	0.0058	0.0078	0.0010	0.0019
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	C12T28SOI_-LRBR0P6_-NAND3X24_P16	C12T28SOI_-LRBR0P6_-NAND3X35_P16	C12T28SOI_-LRBR0P6_-NAND3X47_P16
A	0.0031	0.0042	0.0063	0.0084
B	0.0030	0.0040	0.0060	0.0080
C	0.0028	0.0038	0.0056	0.0076
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16			
A	0.0032			
B	0.0031			
C	0.0029			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16
A to Z ↓	0.0149	0.0134	6.0604	4.3531
A to Z ↑	0.0210	0.0192	4.6507	3.2544
B to Z ↓	0.0159	0.0139	6.0821	4.3682
B to Z ↑	0.0198	0.0178	4.6617	3.2619
C to Z ↓	0.0143	0.0127	6.1185	4.3940
C to Z ↑	0.0166	0.0149	4.6679	3.2836

	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A to Z ↓	0.0151	0.0140	2.9480	2.3019
A to Z ↑	0.0202	0.0190	2.1856	1.6604
B to Z ↓	0.0143	0.0133	2.9587	2.3108
B to Z ↑	0.0181	0.0170	2.1892	1.6631
C to Z ↓	0.0128	0.0120	2.9760	2.3248
C to Z ↑	0.0149	0.0138	2.1856	1.6534
	C12T28SOI_LR_-NAND3X15_P16	**C12T28SOI_LR_-NAND3X18_P16**	**C12T28SOI_LR_-NAND3X15_P16**	**C12T28SOI_LR_-NAND3X18_P16**
A to Z ↓	0.0136	0.0132	1.8447	1.5893
A to Z ↑	0.0187	0.0182	1.3161	1.1038
B to Z ↓	0.0133	0.0131	1.8537	1.5955
B to Z ↑	0.0168	0.0163	1.3186	1.1065
C to Z ↓	0.0123	0.0119	1.8651	1.6046
C to Z ↑	0.0138	0.0133	1.3285	1.1140
	C12T28SOI_LR_-NAND3X21_P16	**C12T28SOI_LR_-NAND3X24_P16**	**C12T28SOI_LR_-NAND3X21_P16**	**C12T28SOI_LR_-NAND3X24_P16**
A to Z ↓	0.0140	0.0137	1.3441	1.2014
A to Z ↑	0.0188	0.0184	0.9454	0.8344
B to Z ↓	0.0134	0.0131	1.3496	1.2066
B to Z ↑	0.0169	0.0165	0.9467	0.8356
C to Z ↓	0.0122	0.0120	1.3574	1.2138
C to Z ↑	0.0138	0.0134	0.9489	0.8365
	C12T28SOI_LR_-NAND3X35_P16	**C12T28SOI_LR_-NAND3X47_P16**	**C12T28SOI_LR_-NAND3X35_P16**	**C12T28SOI_LR_-NAND3X47_P16**
A to Z ↓	0.0132	0.0135	0.8183	0.6227
A to Z ↑	0.0181	0.0183	0.5580	0.4214
B to Z ↓	0.0130	0.0130	0.8223	0.6255
B to Z ↑	0.0161	0.0162	0.5582	0.4205
C to Z ↓	0.0119	0.0121	0.8274	0.6293
C to Z ↑	0.0131	0.0131	0.5617	0.4226
	C12T28SOI_-LRBR0P6_-NAND3X6_P16	**C12T28SOI_-LRBR0P6_-NAND3X12_P16**	**C12T28SOI_-LRBR0P6_-NAND3X6_P16**	**C12T28SOI_-LRBR0P6_-NAND3X12_P16**
A to Z ↓	0.0103	0.0109	2.9584	1.5617
A to Z ↑	0.0273	0.0273	5.0269	2.5613
B to Z ↓	0.0103	0.0096	2.9820	1.5758
B to Z ↑	0.0241	0.0229	5.0461	2.5679
C to Z ↓	0.0080	0.0071	3.0233	1.5990
C to Z ↑	0.0181	0.0165	5.0742	2.5774
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	**C12T28SOI_-LRBR0P6_-NAND3X24_P16**	**C12T28SOI_-LRBR0P6_-NAND3X18_P16**	**C12T28SOI_-LRBR0P6_-NAND3X24_P16**
A to Z ↓	0.0101	0.0105	1.0791	0.8158
A to Z ↑	0.0260	0.0264	1.7036	1.2860
B to Z ↓	0.0093	0.0093	1.0885	0.8231
B to Z ↑	0.0219	0.0222	1.7095	1.2895
C to Z ↓	0.0072	0.0070	1.1033	0.8349
C to Z ↑	0.0160	0.0159	1.7232	1.2925
	C12T28SOI_-LRBR0P6_-NAND3X35_P16	**C12T28SOI_-LRBR0P6_-NAND3X47_P16**	**C12T28SOI_-LRBR0P6_-NAND3X35_P16**	**C12T28SOI_-LRBR0P6_-NAND3X47_P16**

A to Z ↓	0.0101	0.0103	0.5571	0.4254
A to Z ↑	0.0264	0.0265	0.8804	0.6655
B to Z ↓	0.0092	0.0093	0.5626	0.4294
B to Z ↑	0.0221	0.0221	0.8825	0.6660
C to Z ↓	0.0070	0.0074	0.5707	0.4352
C to Z ↑	0.0158	0.0162	0.8927	0.6697
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P16**	
A to Z ↓	0.0108		1.0521	
A to Z ↑	0.0263		1.6398	
B to Z ↓	0.0093		1.0610	
B to Z ↑	0.0220		1.6436	
C to Z ↓	0.0068		1.0762	
C to Z ↑	0.0157		1.6354	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P16	2.368e-06	1.310e-09
C12T28SOI_LR_NAND3X6_P16	3.253e-06	1.310e-09
C12T28SOI_LR_NAND3X9_P16	4.721e-06	1.807e-09
C12T28SOI_LR_NAND3X12_P16	6.051e-06	1.807e-09
C12T28SOI_LR_NAND3X15_P16	7.227e-06	2.139e-09
C12T28SOI_LR_NAND3X18_P16	8.428e-06	2.139e-09
C12T28SOI_LR_NAND3X21_P16	1.029e-05	2.801e-09
C12T28SOI_LR_NAND3X24_P16	1.143e-05	2.801e-09
C12T28SOI_LR_NAND3X35_P16	1.686e-05	3.795e-09
C12T28SOI_LR_NAND3X47_P16	2.222e-05	4.789e-09
C12T28SOI_LRBR0P6_NAND3X6_-P16	4.036e-06	2.248e-09
C12T28SOI_LRBR0P6_NAND3X12_-P16	7.592e-06	2.790e-09
C12T28SOI_LRBR0P6_NAND3X18_-P16	1.055e-05	3.151e-09
C12T28SOI_LRBR0P6_NAND3X24_-P16	1.449e-05	3.874e-09
C12T28SOI_LRBR0P6_NAND3X35_-P16	2.148e-05	4.958e-09
C12T28SOI_LRBR0P6_NAND3X47_-P16	2.838e-05	6.042e-09
C12T28SOIDV_LRBR0P6_-NAND3X18_P16	1.187e-05	2.606e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A (output stable)	2.824e-05	3.859e-05	9.026e-05	1.072e-04
B (output stable)	9.348e-05	1.215e-04	2.885e-04	3.420e-04
C (output stable)	3.318e-04	3.976e-04	6.614e-04	7.639e-04
A to Z	2.040e-03	2.524e-03	4.140e-03	4.929e-03
B to Z	1.786e-03	2.149e-03	3.276e-03	3.894e-03
C to Z	1.350e-03	1.637e-03	2.417e-03	2.885e-03

	C12T28SOI_LR_-NAND3X15_P16	C12T28SOI_LR_-NAND3X18_P16	C12T28SOI_LR_-NAND3X21_P16	C12T28SOI_LR_-NAND3X24_P16
A (output stable)	1.230e-04	1.365e-04	1.851e-04	2.010e-04
B (output stable)	3.912e-04	4.493e-04	5.845e-04	6.417e-04
C (output stable)	8.348e-04	9.542e-04	1.268e-03	1.373e-03
A to Z	5.968e-03	6.777e-03	8.464e-03	9.268e-03
B to Z	4.734e-03	5.372e-03	6.697e-03	7.326e-03
C to Z	3.577e-03	4.011e-03	4.960e-03	5.405e-03
	C12T28SOI_LR_-NAND3X35_P16	C12T28SOI_LR_-NAND3X47_P16	C12T28SOI_-LRBR0P6_-NAND3X6_P16	C12T28SOI_-LRBR0P6_-NAND3X12_P16
A (output stable)	2.722e-04	3.650e-04	5.487e-05	1.525e-04
B (output stable)	8.926e-04	1.176e-03	1.767e-04	4.957e-04
C (output stable)	1.993e-03	2.579e-03	5.450e-04	1.099e-03
A to Z	1.344e-02	1.778e-02	2.792e-03	5.537e-03
B to Z	1.061e-02	1.398e-02	2.224e-03	4.014e-03
C to Z	7.748e-03	1.032e-02	1.433e-03	2.415e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	C12T28SOI_-LRBR0P6_-NAND3X24_P16	C12T28SOI_-LRBR0P6_-NAND3X35_P16	C12T28SOI_-LRBR0P6_-NAND3X47_P16
A (output stable)	1.928e-04	2.885e-04	3.916e-04	5.088e-04
B (output stable)	6.406e-04	9.223e-04	1.286e-03	1.663e-03
C (output stable)	1.357e-03	2.006e-03	2.922e-03	3.759e-03
A to Z	7.617e-03	1.042e-02	1.517e-02	1.996e-02
B to Z	5.499e-03	7.532e-03	1.092e-02	1.447e-02
C to Z	3.419e-03	4.537e-03	6.480e-03	8.667e-03
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16			
A (output stable)	2.204e-04			
B (output stable)	7.413e-04			
C (output stable)	1.583e-03			
A to Z	8.147e-03			
B to Z	5.898e-03			
C to Z	3.541e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A (output stable)	3.267e-08	3.167e-09	3.247e-08	-7.303e-08
B (output stable)	4.650e-08	2.465e-08	-6.117e-07	-8.487e-08
C (output stable)	5.997e-08	4.620e-08	-2.918e-06	-5.903e-08
A to Z	5.550e-07	4.030e-07	-5.650e-07	-9.660e-07
B to Z	-2.000e-08	-1.720e-07	-6.100e-07	-3.480e-07
C to Z	5.590e-07	1.271e-06	8.970e-07	-1.204e-06
	C12T28SOI_LR_-NAND3X15_P16	C12T28SOI_LR_-NAND3X18_P16	C12T28SOI_LR_-NAND3X21_P16	C12T28SOI_LR_-NAND3X24_P16
A (output stable)	-8.627e-08	-1.362e-07	-1.031e-07	-1.625e-07
B (output stable)	-7.612e-07	-7.719e-07	-1.395e-06	-1.343e-06
C (output stable)	-2.426e-06	-2.336e-06	-5.086e-06	-4.605e-06
A to Z	3.470e-07	8.580e-07	1.254e-06	1.365e-06
B to Z	-5.560e-07	-1.730e-07	-4.210e-07	-2.490e-07

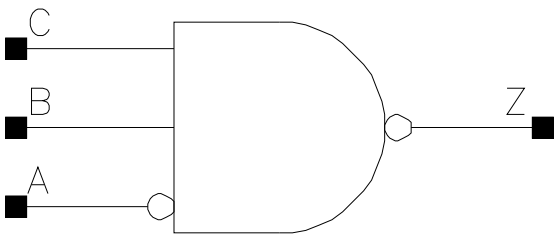
C to Z	-9.250e-07	-6.550e-07	1.000e-09	-1.930e-07
	C12T28SOI_LR_-NAND3X35_P16	C12T28SOI_LR_-NAND3X47_P16	C12T28SOI_-LRBR0P6_-NAND3X6_P16	C12T28SOI_-LRBR0P6_-NAND3X12_P16
A (output stable)	-2.898e-07	-3.211e-07	1.561e-07	2.326e-07
B (output stable)	-2.215e-06	-2.686e-06	-1.288e-06	-3.939e-06
C (output stable)	-7.028e-06	-8.497e-06	-6.172e-06	-8.979e-06
A to Z	1.578e-06	1.605e-06	1.430e-07	1.028e-06
B to Z	-1.488e-06	5.720e-07	4.690e-07	1.041e-06
C to Z	-7.810e-07	-9.660e-07	6.870e-07	2.798e-06
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	C12T28SOI_-LRBR0P6_-NAND3X24_P16	C12T28SOI_-LRBR0P6_-NAND3X35_P16	C12T28SOI_-LRBR0P6_-NAND3X47_P16
A (output stable)	-8.147e-08	1.748e-07	-6.140e-08	-1.117e-08
B (output stable)	-8.567e-08	-4.668e-06	-2.397e-06	-3.389e-06
C (output stable)	-4.833e-08	-1.100e-05	-8.553e-06	-1.157e-05
A to Z	1.940e-07	-1.894e-06	-1.140e-07	1.600e-07
B to Z	8.230e-07	8.190e-07	1.182e-06	1.550e-06
C to Z	3.708e-06	6.434e-06	8.580e-06	1.680e-07
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16			
A (output stable)	-8.850e-08			
B (output stable)	-6.500e-08			
C (output stable)	-6.497e-08			
A to Z	3.600e-07			
B to Z	8.380e-07			
C to Z	3.618e-06			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.816	0.9792
X12_P16	1.200	1.224	1.4688
X18_P16	1.200	1.496	1.7952
X24_P16	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0009	0.0014	0.0014	0.0025
B	0.0010	0.0020	0.0030	0.0040
C	0.0010	0.0020	0.0028	0.0038

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X12_P16**	**X6_P16**	**X12_P16**
A to Z ↓	0.0348	0.0340	4.3494	2.3177
A to Z ↑	0.0254	0.0248	3.2177	1.6140
B to Z ↓	0.0121	0.0127	4.3898	2.3390
B to Z ↑	0.0163	0.0163	3.2684	1.6446
C to Z ↓	0.0122	0.0113	4.4177	2.3525
C to Z ↑	0.0140	0.0130	3.2899	1.6565
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0392	0.0330	1.5884	1.2019

A to Z ↑	0.0288	0.0236	1.0870	0.8137
B to Z ↓	0.0130	0.0126	1.5998	1.2127
B to Z ↑	0.0162	0.0159	1.1069	0.8319
C to Z ↓	0.0121	0.0113	1.6081	1.2200
C to Z ↑	0.0134	0.0127	1.1147	0.8378

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P16	4.241e-06	1.476e-09
X12_P16	8.323e-06	1.973e-09
X18_P16	1.058e-05	2.304e-09
X24_P16	1.634e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	1.895e-03	3.415e-03	4.664e-03	6.395e-03
B (output stable)	1.028e-04	2.996e-04	4.693e-04	6.513e-04
C (output stable)	1.991e-04	7.634e-04	9.628e-04	1.426e-03
A to Z	4.223e-03	8.336e-03	1.200e-02	1.597e-02
B to Z	1.831e-03	3.623e-03	5.370e-03	6.907e-03
C to Z	1.471e-03	2.597e-03	4.009e-03	4.930e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

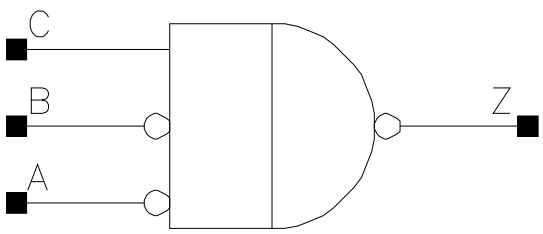
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	4.037e-08	5.300e-08	-6.277e-08	2.042e-07
B (output stable)	6.997e-09	-6.623e-07	-1.761e-07	-2.462e-06
C (output stable)	3.043e-08	-2.625e-06	-1.302e-07	-4.809e-06
A to Z	1.080e-07	4.310e-07	1.740e-07	2.200e-08
B to Z	-4.610e-07	-9.600e-08	-1.140e-07	3.540e-07
C to Z	-3.200e-08	-6.360e-07	-8.820e-07	-4.030e-07

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	0.816	0.9792
X13_P16	1.200	1.088	1.3056
X20_P16	1.200	1.632	1.9584
X27_P16	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P16	X13_P16	X20_P16	X27_P16
A	0.0012	0.0012	0.0024	0.0023
B	0.0013	0.0013	0.0025	0.0023
C	0.0010	0.0020	0.0029	0.0039

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	**X13_P16**	**X7_P16**	**X13_P16**
A to Z ↓	0.0328	0.0407	3.0357	1.6186
A to Z ↑	0.0213	0.0250	3.1954	1.6069
B to Z ↓	0.0331	0.0413	3.0396	1.6181
B to Z ↑	0.0197	0.0236	3.1930	1.6046
C to Z ↓	0.0082	0.0078	3.1052	1.6442
C to Z ↑	0.0123	0.0115	3.2838	1.6561
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0373	0.0411	1.1008	0.8378
A to Z ↑	0.0231	0.0279	1.0824	0.8129
B to Z ↓	0.0354	0.0400	1.1008	0.8380

B to Z ↑	0.0209	0.0261	1.0797	0.8112
C to Z ↓	0.0088	0.0083	1.1221	0.8523
C to Z ↑	0.0122	0.0118	1.1146	0.8369

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X7_P16	5.873e-06	1.476e-09
X13_P16	8.149e-06	1.807e-09
X20_P16	1.296e-05	2.470e-09
X27_P16	1.432e-05	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	1.059e-03	1.452e-03	2.465e-03	2.910e-03
B (output stable)	8.674e-04	1.262e-03	1.915e-03	2.392e-03
C (output stable)	5.946e-05	4.694e-04	4.699e-04	6.252e-04
A to Z	4.636e-03	7.687e-03	1.215e-02	1.518e-02
B to Z	4.158e-03	7.219e-03	1.065e-02	1.385e-02
C to Z	1.174e-03	2.125e-03	3.437e-03	4.483e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

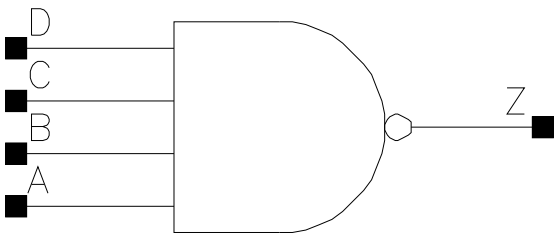
Pin Cycle (vdds)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	-8.936e-07	-9.040e-07	-6.040e-06	-6.041e-06
B (output stable)	1.670e-05	1.659e-05	5.885e-05	5.706e-05
C (output stable)	2.000e-09	-1.121e-07	-1.264e-06	-1.392e-06
A to Z	2.230e-08	-7.512e-08	-2.508e-06	-3.160e-06
B to Z	2.355e-07	-2.013e-07	8.460e-07	-4.890e-07
C to Z	3.204e-07	1.480e-07	1.207e-06	1.470e-07

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0008	0.0008	0.0010	0.0012
B	0.0009	0.0009	0.0010	0.0013
C	0.0008	0.0009	0.0011	0.0013
D	0.0008	0.0008	0.0011	0.0013

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0512	0.0512	1.9372	0.9667
A to Z ↑	0.0430	0.0469	3.2518	1.6191
B to Z ↓	0.0529	0.0537	1.9374	0.9670
B to Z ↑	0.0410	0.0458	3.2514	1.6182
C to Z ↓	0.0509	0.0500	1.9380	0.9667
C to Z ↑	0.0437	0.0482	3.2543	1.6165

D to Z ↓	0.0529	0.0518	1.9382	0.9656
D to Z ↑	0.0422	0.0461	3.2504	1.6169
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0544	0.0500	0.6654	0.4977
A to Z ↑	0.0458	0.0450	1.0896	0.8174
B to Z ↓	0.0564	0.0516	0.6656	0.4978
B to Z ↑	0.0441	0.0432	1.0896	0.8170
C to Z ↓	0.0496	0.0459	0.6652	0.4978
C to Z ↑	0.0458	0.0450	1.0874	0.8151
D to Z ↓	0.0515	0.0476	0.6652	0.4978
D to Z ↑	0.0438	0.0430	1.0878	0.8157

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	7.673e-06	1.973e-09
X17_P16	1.125e-05	2.304e-09
X25_P16	1.650e-05	2.801e-09
X33_P16	2.033e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	7.513e-04	9.492e-04	1.393e-03	1.643e-03
B (output stable)	6.812e-04	8.870e-04	1.296e-03	1.517e-03
C (output stable)	7.260e-04	8.767e-04	1.343e-03	1.532e-03
D (output stable)	6.519e-04	7.993e-04	1.196e-03	1.367e-03
A to Z	5.548e-03	8.565e-03	1.328e-02	1.625e-02
B to Z	5.358e-03	8.384e-03	1.301e-02	1.590e-02
C to Z	5.607e-03	8.332e-03	1.237e-02	1.509e-02
D to Z	5.424e-03	8.130e-03	1.208e-02	1.473e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

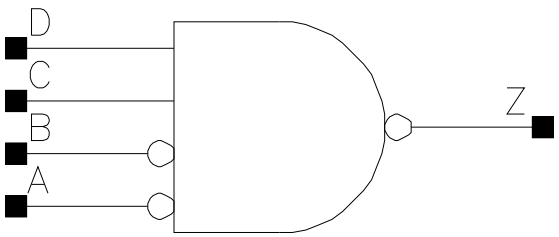
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	-3.069e-07	-4.874e-07	-3.168e-06	-3.286e-06
B (output stable)	-2.400e-07	-4.535e-07	-3.214e-06	-3.100e-06
C (output stable)	5.550e-06	1.087e-05	3.050e-05	3.729e-05
D (output stable)	5.366e-06	1.085e-05	2.088e-05	2.861e-05
A to Z	1.461e-07	-2.191e-07	-2.434e-06	-1.796e-06
B to Z	1.144e-07	-6.610e-08	-2.326e-06	-1.272e-06
C to Z	-1.612e-07	-4.580e-07	-6.790e-07	-5.610e-07
D to Z	4.760e-08	-4.177e-07	-5.200e-07	-7.400e-07

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X12_P16	1.200	1.496	1.7952
X18_P16	1.200	2.040	2.4480
X24_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0013	0.0013	0.0024	0.0022
B	0.0013	0.0017	0.0025	0.0023
C	0.0010	0.0020	0.0030	0.0041
D	0.0010	0.0020	0.0028	0.0040

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X12_P16	X6_P16	X12_P16
A to Z ↓	0.0351	0.0474	4.4834	2.3267
A to Z ↑	0.0231	0.0283	3.1933	1.6096
B to Z ↓	0.0349	0.0469	4.4849	2.3269
B to Z ↑	0.0208	0.0266	3.1940	1.6081
C to Z ↓	0.0122	0.0127	4.5212	2.3374
C to Z ↑	0.0165	0.0163	3.4502	1.6443

D to Z ↓	0.0121	0.0113	4.5488	2.3510
D to Z ↑	0.0140	0.0130	3.4730	1.6562
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0413	0.0462	1.5860	1.2060
A to Z ↑	0.0251	0.0321	1.0826	0.8135
B to Z ↓	0.0395	0.0448	1.5862	1.2066
B to Z ↑	0.0229	0.0301	1.0814	0.8131
C to Z ↓	0.0127	0.0130	1.5954	1.2115
C to Z ↑	0.0161	0.0163	1.1106	0.8302
D to Z ↓	0.0118	0.0119	1.6049	1.2187
D to Z ↑	0.0133	0.0132	1.1320	0.8368

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P16	5.226e-06	1.642e-09
X12_P16	8.102e-06	2.304e-09
X18_P16	1.271e-05	2.967e-09
X24_P16	1.375e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	1.226e-03	2.047e-03	3.128e-03	3.779e-03
B (output stable)	9.948e-04	1.714e-03	2.467e-03	3.116e-03
C (output stable)	1.291e-04	3.543e-04	5.200e-04	7.229e-04
D (output stable)	2.407e-04	8.414e-04	1.042e-03	1.570e-03
A to Z	5.005e-03	9.484e-03	1.413e-02	1.847e-02
B to Z	4.551e-03	8.818e-03	1.272e-02	1.707e-02
C to Z	1.773e-03	3.610e-03	5.239e-03	7.256e-03
D to Z	1.414e-03	2.584e-03	3.951e-03	5.319e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

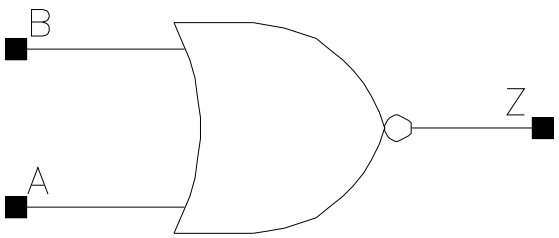
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	-7.938e-07	-4.493e-06	-5.676e-06	-6.295e-06
B (output stable)	1.495e-05	3.000e-05	5.066e-05	4.997e-05
C (output stable)	2.553e-08	-1.019e-06	-1.043e-06	-2.233e-06
D (output stable)	3.020e-08	-3.290e-06	-3.232e-06	-6.780e-06
A to Z	4.233e-07	-2.515e-06	-2.445e-06	-3.665e-06
B to Z	1.648e-07	-1.950e-07	1.098e-06	-3.250e-07
C to Z	3.150e-07	-7.400e-08	-6.700e-08	-2.280e-07
D to Z	3.800e-07	-5.240e-07	-6.950e-07	-9.650e-07

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.408	0.4896
X5_P16	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X10_P16	1.200	0.680	0.8160
X14_P16	1.200	0.680	0.8160
X17_P16	1.200	0.952	1.1424
X21_P16	1.200	0.952	1.1424
X24_P16	1.200	1.224	1.4688
X27_P16	1.200	1.224	1.4688
X34_P16	1.200	1.496	1.7952
X40_P16	1.200	1.360	1.6320
X41_P16	1.200	1.768	2.1216
X49_P16	1.200	1.496	1.7952
X53_P16	1.200	1.904	2.2848
X55_P16	1.200	2.312	2.7744
X57_P16	1.200	1.904	2.2848
X65_P16	1.200	2.040	2.4480
X84_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P16	X5_P16	X7_P16	X10_P16
A	0.0007	0.0008	0.0010	0.0018
B	0.0007	0.0008	0.0011	0.0016
	X14_P16	X17_P16	X21_P16	X24_P16

A	0.0022	0.0028	0.0033	0.0038
B	0.0020	0.0026	0.0030	0.0036
	X27_P16	X34_P16	X40_P16	X41_P16
A	0.0042	0.0054	0.0012	0.0065
B	0.0040	0.0049	0.0013	0.0060
	X49_P16	X53_P16	X55_P16	X57_P16
A	0.0012	0.0013	0.0087	0.0013
B	0.0013	0.0012	0.0081	0.0012
	X65_P16	X84_P16		
A	0.0012	0.0013		
B	0.0012	0.0012		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X5_P16**	**X3_P16**	**X5_P16**
A to Z ↓	0.0089	0.0083	3.6130	2.6520
A to Z ↑	0.0186	0.0173	11.8341	8.6965
B to Z ↓	0.0073	0.0064	3.7040	2.6806
B to Z ↑	0.0184	0.0168	11.9036	8.7320
	X7_P16	**X10_P16**	**X7_P16**	**X10_P16**
A to Z ↓	0.0080	0.0084	1.9656	1.2662
A to Z ↑	0.0164	0.0187	6.1896	4.1042
B to Z ↓	0.0060	0.0055	1.9946	1.2836
B to Z ↑	0.0157	0.0149	6.2190	4.1281
	X14_P16	**X17_P16**	**X14_P16**	**X17_P16**
A to Z ↓	0.0082	0.0084	0.9701	0.7750
A to Z ↑	0.0175	0.0177	3.0650	2.4641
B to Z ↓	0.0053	0.0059	0.9839	0.7847
B to Z ↑	0.0141	0.0151	3.0822	2.4786
	X21_P16	**X24_P16**	**X21_P16**	**X24_P16**
A to Z ↓	0.0083	0.0082	0.6622	0.5633
A to Z ↑	0.0171	0.0174	2.0610	1.7907
B to Z ↓	0.0059	0.0055	0.6699	0.5710
B to Z ↑	0.0147	0.0146	2.0725	1.8008
	X27_P16	**X34_P16**	**X27_P16**	**X34_P16**
A to Z ↓	0.0082	0.0085	0.5005	0.4041
A to Z ↑	0.0170	0.0171	1.5801	1.2583
B to Z ↓	0.0055	0.0058	0.5078	0.4094
B to Z ↑	0.0142	0.0146	1.5890	1.2651
	X40_P16	**X41_P16**	**X40_P16**	**X41_P16**
A to Z ↓	0.0356	0.0083	0.4036	0.3366
A to Z ↑	0.0515	0.0170	0.6697	1.0422
B to Z ↓	0.0340	0.0056	0.4040	0.3412
B to Z ↑	0.0522	0.0141	0.6696	1.0484
	X49_P16	**X53_P16**	**X49_P16**	**X53_P16**
A to Z ↓	0.0375	0.0387	0.3361	0.3067
A to Z ↑	0.0531	0.0609	0.5571	0.5137
B to Z ↓	0.0359	0.0372	0.3362	0.3064
B to Z ↑	0.0538	0.0613	0.5563	0.5133
	X55_P16	**X57_P16**	**X55_P16**	**X57_P16**
A to Z ↓	0.0085	0.0390	0.2543	0.2888
A to Z ↑	0.0171	0.0610	0.7850	0.4785

B to Z ↓	0.0057	0.0375	0.2582	0.2889
B to Z ↑	0.0142	0.0614	0.7901	0.4783
	X65_P16	**X84_P16**	**X65_P16**	**X84_P16**
A to Z ↓	0.0402	0.0422	0.2537	0.2025
A to Z ↑	0.0620	0.0626	0.4192	0.3324
B to Z ↓	0.0386	0.0407	0.2538	0.2023
B to Z ↑	0.0624	0.0633	0.4188	0.3324

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P16	1.704e-06	9.792e-10
X5_P16	2.267e-06	9.792e-10
X7_P16	3.007e-06	9.792e-10
X10_P16	4.458e-06	1.310e-09
X14_P16	5.700e-06	1.310e-09
X17_P16	7.128e-06	1.642e-09
X21_P16	8.252e-06	1.642e-09
X24_P16	9.757e-06	1.973e-09
X27_P16	1.081e-05	1.973e-09
X34_P16	1.337e-05	2.304e-09
X40_P16	1.581e-05	2.139e-09
X41_P16	1.593e-05	2.635e-09
X49_P16	1.745e-05	2.304e-09
X53_P16	2.144e-05	2.801e-09
X55_P16	2.105e-05	3.298e-09
X57_P16	2.216e-05	2.801e-09
X65_P16	2.381e-05	2.967e-09
X84_P16	2.751e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	3.371e-05	4.360e-05	6.028e-05	1.740e-04
B (output stable)	7.962e-06	1.027e-05	1.480e-05	8.482e-05
A to Z	9.545e-04	1.180e-03	1.561e-03	2.729e-03
B to Z	7.021e-04	8.416e-04	1.092e-03	1.561e-03
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	2.045e-04	2.466e-04	2.846e-04	3.389e-04
B (output stable)	9.732e-05	1.150e-04	1.234e-04	1.355e-04
A to Z	3.381e-03	4.280e-03	4.936e-03	5.807e-03
B to Z	1.965e-03	2.673e-03	3.078e-03	3.508e-03
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	3.697e-04	4.594e-04	6.111e-05	5.793e-04
B (output stable)	1.441e-04	1.660e-04	1.489e-05	2.369e-04
A to Z	6.429e-03	8.104e-03	1.587e-02	9.735e-03
B to Z	3.873e-03	5.061e-03	1.542e-02	5.800e-03
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	6.135e-05	6.202e-05	7.608e-04	6.206e-05
B (output stable)	1.479e-05	1.505e-05	3.092e-04	1.511e-05
A to Z	1.806e-02	2.214e-02	1.289e-02	2.271e-02
B to Z	1.761e-02	2.165e-02	7.723e-03	2.222e-02
	X65_P16	X84_P16		

A (output stable)	6.215e-05	6.360e-05		
B (output stable)	1.513e-05	1.614e-05		
A to Z	2.469e-02	2.965e-02		
B to Z	2.420e-02	2.907e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

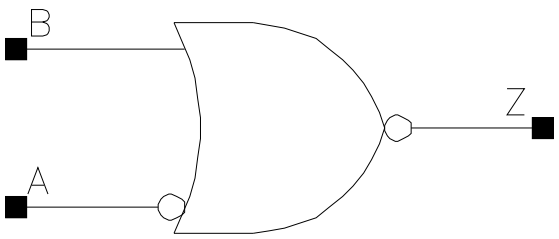
Pin Cycle (vdds)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	-8.535e-07	-9.945e-07	-1.357e-06	-7.804e-06
B (output stable)	1.362e-05	1.810e-05	2.436e-05	9.589e-05
A to Z	2.863e-07	5.449e-07	1.030e-07	-2.511e-06
B to Z	5.671e-07	1.305e-06	1.656e-06	-2.945e-07
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	-8.244e-06	-6.341e-06	-7.025e-06	-1.203e-05
B (output stable)	1.167e-04	8.409e-05	9.611e-05	1.573e-04
A to Z	-1.893e-06	-8.900e-07	-6.540e-07	-2.876e-06
B to Z	-8.520e-08	-3.310e-08	-1.740e-07	-6.471e-07
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	-1.280e-05	-1.061e-05	-1.337e-06	-1.767e-05
B (output stable)	1.758e-04	1.446e-04	2.425e-05	2.365e-04
A to Z	-2.368e-06	-6.340e-07	-5.030e-07	-3.956e-06
B to Z	-6.736e-07	-4.440e-07	-4.490e-07	-5.040e-07
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	-1.339e-06	-1.322e-06	-2.183e-05	-1.322e-06
B (output stable)	2.413e-05	2.555e-05	2.965e-04	2.561e-05
A to Z	-8.190e-07	-7.240e-07	-5.876e-06	-9.240e-07
B to Z	-3.920e-07	-8.180e-07	-7.080e-07	-7.510e-07
	X65_P16	X84_P16		
A (output stable)	-1.320e-06	-1.347e-06		
B (output stable)	2.555e-05	2.622e-05		
A to Z	-7.240e-07	-1.047e-06		
B to Z	-8.250e-07	-3.850e-07		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X7_P16	1.200	0.680	0.8160
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X41_P16	1.200	2.312	2.7744
X55_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X7_P16	X13_P16
A	0.0009	0.0009	0.0009	0.0014
B	0.0007	0.0010	0.0010	0.0020
	X27_P16	X41_P16	X55_P16	
A	0.0025	0.0037	0.0049	
B	0.0040	0.0060	0.0080	

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0277	0.0310	3.4562	2.3032
A to Z ↑	0.0251	0.0253	11.7297	6.1525
B to Z ↓	0.0076	0.0073	3.6787	2.4565
B to Z ↑	0.0186	0.0155	11.8817	6.2300

	X7_P16	X13_P16	X7_P16	X13_P16
A to Z ↓	0.0313	0.0288	1.8459	1.0008
A to Z ↑	0.0277	0.0265	6.0908	3.2274
B to Z ↓	0.0063	0.0056	1.9118	1.0325
B to Z ↑	0.0166	0.0153	6.1501	3.2648
	X27_P16	**X41_P16**	**X27_P16**	**X41_P16**
A to Z ↓	0.0280	0.0285	0.4792	0.3240
A to Z ↑	0.0253	0.0257	1.5473	1.0375
B to Z ↓	0.0055	0.0056	0.5101	0.3433
B to Z ↑	0.0145	0.0143	1.5655	1.0498
	X55_P16		**X55_P16**	
A to Z ↓	0.0283		0.2450	
A to Z ↑	0.0255		0.7823	
B to Z ↓	0.0056		0.2598	
B to Z ↑	0.0143		0.7917	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P16	2.897e-06	1.145e-09
X6_P16	3.851e-06	1.145e-09
X7_P16	4.602e-06	1.310e-09
X13_P16	8.138e-06	1.642e-09
X27_P16	1.549e-05	2.470e-09
X41_P16	2.257e-05	3.298e-09
X55_P16	2.964e-05	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	1.470e-03	1.879e-03	2.006e-03	3.319e-03
B (output stable)	3.017e-05	5.717e-05	8.465e-05	1.770e-04
A to Z	2.494e-03	3.478e-03	4.011e-03	6.845e-03
B to Z	7.146e-04	1.063e-03	1.250e-03	2.103e-03
	X27_P16	X41_P16	X55_P16	
A (output stable)	6.517e-03	9.865e-03	1.305e-02	
B (output stable)	3.793e-04	5.490e-04	7.587e-04	
A to Z	1.360e-02	2.029e-02	2.693e-02	
B to Z	4.083e-03	5.981e-03	7.882e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

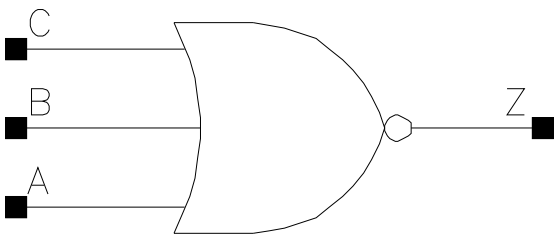
Pin Cycle (vdds)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	-2.381e-07	-1.019e-06	-3.719e-06	-6.693e-06
B (output stable)	1.244e-05	2.384e-05	4.384e-05	7.266e-05
A to Z	9.562e-07	6.400e-08	-4.100e-07	-7.170e-07
B to Z	1.948e-07	-1.646e-07	1.905e-06	-5.360e-07
	X27_P16	X41_P16	X55_P16	
A (output stable)	-9.283e-06	-1.300e-05	-1.616e-05	
B (output stable)	1.216e-04	1.720e-04	2.209e-04	
A to Z	2.493e-06	-2.831e-06	-2.921e-06	
B to Z	-5.200e-07	-6.840e-07	-7.730e-07	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X9_P16	1.200	0.952	1.1424
X13_P16	1.200	0.952	1.1424
X16_P16	1.200	1.360	1.6320
X19_P16	1.200	1.496	1.7952
X22_P16	1.200	1.768	2.1216
X25_P16	1.200	1.904	2.2848
X37_P16	1.200	2.584	3.1008
X49_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P16	X6_P16	X9_P16	X13_P16
A	0.0009	0.0011	0.0017	0.0021
B	0.0008	0.0010	0.0018	0.0022
C	0.0008	0.0011	0.0016	0.0020
	X16_P16	X19_P16	X22_P16	X25_P16
A	0.0028	0.0032	0.0038	0.0042
B	0.0028	0.0036	0.0039	0.0048
C	0.0026	0.0029	0.0036	0.0038
	X37_P16	X49_P16		
A	0.0063	0.0086		
B	0.0064	0.0086		

C	0.0058	0.0079		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0105	0.0099	2.6897	1.9931
A to Z ↑	0.0267	0.0246	12.8805	9.1560
B to Z ↓	0.0098	0.0091	2.6912	1.9938
B to Z ↑	0.0249	0.0227	12.8964	9.1684
C to Z ↓	0.0081	0.0072	2.7162	2.0187
C to Z ↑	0.0227	0.0202	12.9266	9.1895
	X9_P16	**X13_P16**	**X9_P16**	**X13_P16**
A to Z ↓	0.0102	0.0101	1.3047	1.0075
A to Z ↑	0.0269	0.0254	6.0584	4.5399
B to Z ↓	0.0095	0.0090	1.2735	0.9693
B to Z ↑	0.0263	0.0242	6.0652	4.5465
C to Z ↓	0.0067	0.0064	1.2870	0.9871
C to Z ↑	0.0190	0.0179	6.0768	4.5545
	X16_P16	**X19_P16**	**X16_P16**	**X19_P16**
A to Z ↓	0.0102	0.0100	0.7808	0.6625
A to Z ↑	0.0259	0.0255	3.6603	3.0399
B to Z ↓	0.0096	0.0094	0.7820	0.6495
B to Z ↑	0.0248	0.0250	3.6636	3.0438
C to Z ↓	0.0070	0.0068	0.7883	0.6755
C to Z ↑	0.0197	0.0187	3.6722	3.0503
	X22_P16	**X25_P16**	**X22_P16**	**X25_P16**
A to Z ↓	0.0101	0.0100	0.5741	0.5041
A to Z ↑	0.0256	0.0255	2.6147	2.2840
B to Z ↓	0.0093	0.0092	0.5648	0.4870
B to Z ↑	0.0246	0.0251	2.6178	2.2864
C to Z ↓	0.0066	0.0065	0.5719	0.5056
C to Z ↑	0.0184	0.0179	2.6239	2.2916
	X37_P16	**X49_P16**	**X37_P16**	**X49_P16**
A to Z ↓	0.0101	0.0102	0.3458	0.2621
A to Z ↑	0.0248	0.0249	1.5305	1.1524
B to Z ↓	0.0092	0.0094	0.3422	0.2596
B to Z ↑	0.0236	0.0235	1.5321	1.1537
C to Z ↓	0.0069	0.0070	0.3473	0.2632
C to Z ↑	0.0180	0.0182	1.5360	1.1567

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	2.313e-06	1.145e-09
X6_P16	3.071e-06	1.145e-09
X9_P16	4.663e-06	1.642e-09
X13_P16	5.978e-06	1.642e-09
X16_P16	7.527e-06	2.139e-09
X19_P16	9.094e-06	2.304e-09
X22_P16	1.040e-05	2.635e-09
X25_P16	1.194e-05	2.801e-09
X37_P16	1.708e-05	3.629e-09

X49_P16	2.266e-05	4.623e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	1.588e-04	2.122e-04	4.723e-04	5.787e-04
B (output stable)	-1.781e-05	-2.672e-05	1.008e-04	7.496e-05
C (output stable)	7.031e-06	1.012e-05	4.338e-05	4.996e-05
A to Z	1.774e-03	2.275e-03	3.801e-03	4.729e-03
B to Z	1.411e-03	1.773e-03	3.114e-03	3.784e-03
C to Z	1.060e-03	1.286e-03	1.855e-03	2.284e-03
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	6.690e-04	8.304e-04	9.876e-04	1.158e-03
B (output stable)	3.706e-05	6.569e-05	1.089e-04	1.401e-04
C (output stable)	5.312e-05	6.492e-05	7.915e-05	9.126e-05
A to Z	6.055e-03	7.166e-03	8.336e-03	9.507e-03
B to Z	4.854e-03	5.820e-03	6.691e-03	7.751e-03
C to Z	3.193e-03	3.596e-03	4.128e-03	4.576e-03
	X37_P16	X49_P16		
A (output stable)	1.619e-03	2.141e-03		
B (output stable)	9.912e-05	1.132e-04		
C (output stable)	1.356e-04	1.765e-04		
A to Z	1.379e-02	1.837e-02		
B to Z	1.093e-02	1.452e-02		
C to Z	6.709e-03	9.028e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

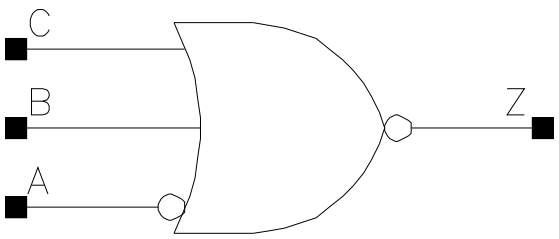
Pin Cycle (vdds)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	-1.610e-05	-2.107e-05	-5.652e-05	-6.788e-05
B (output stable)	1.657e-05	2.338e-05	2.610e-05	3.883e-05
C (output stable)	2.008e-05	2.949e-05	7.559e-05	9.773e-05
A to Z	-6.660e-07	-6.560e-07	-4.687e-06	-4.242e-06
B to Z	7.920e-08	4.610e-07	-1.220e-06	1.800e-07
C to Z	9.770e-08	1.240e-06	8.139e-07	1.697e-07
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	-6.278e-05	-8.347e-05	-1.035e-04	-1.267e-04
B (output stable)	5.468e-05	7.486e-05	7.552e-05	9.985e-05
C (output stable)	7.718e-05	1.091e-04	1.352e-04	1.696e-04
A to Z	-3.058e-06	-4.682e-06	-6.815e-06	-7.435e-06
B to Z	-4.810e-07	-6.800e-08	-1.670e-07	4.280e-07
C to Z	2.654e-06	1.777e-06	1.030e-06	4.990e-07
	X37_P16	X49_P16		
A (output stable)	-1.645e-04	-2.134e-04		
B (output stable)	1.355e-04	1.794e-04		
C (output stable)	2.178e-04	2.814e-04		
A to Z	-9.160e-06	-1.122e-05		
B to Z	7.270e-07	8.800e-07		
C to Z	1.721e-06	2.053e-06		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.680	0.8160
X13_P16	1.200	1.224	1.4688
X19_P16	1.200	1.496	1.7952
X25_P16	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0010	0.0013	0.0014	0.0025
B	0.0010	0.0022	0.0032	0.0043
C	0.0011	0.0020	0.0029	0.0039

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X13_P16**	**X6_P16**	**X13_P16**
A to Z ↓	0.0313	0.0305	1.9224	1.0633
A to Z ↑	0.0341	0.0338	9.2440	4.5338
B to Z ↓	0.0093	0.0091	2.0018	0.9743
B to Z ↑	0.0230	0.0242	9.2783	4.5454
C to Z ↓	0.0074	0.0064	2.0203	0.9879
C to Z ↑	0.0207	0.0178	9.3004	4.5545
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0349	0.0304	0.6514	0.4930

A to Z ↑	0.0369	0.0338	3.0503	2.2875
B to Z ↓	0.0095	0.0092	0.6749	0.5036
B to Z ↑	0.0235	0.0236	3.0612	2.2955
C to Z ↓	0.0068	0.0064	0.6766	0.5086
C to Z ↑	0.0187	0.0179	3.0684	2.3006

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P16	4.302e-06	1.310e-09
X13_P16	8.572e-06	1.973e-09
X19_P16	1.097e-05	2.304e-09
X25_P16	1.646e-05	3.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	2.086e-03	3.933e-03	5.221e-03	7.746e-03
B (output stable)	3.732e-06	6.399e-05	6.081e-05	1.041e-04
C (output stable)	2.089e-05	8.860e-05	9.396e-05	1.500e-04
A to Z	4.324e-03	8.603e-03	1.191e-02	1.670e-02
B to Z	1.787e-03	3.807e-03	5.466e-03	7.313e-03
C to Z	1.307e-03	2.286e-03	3.570e-03	4.516e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

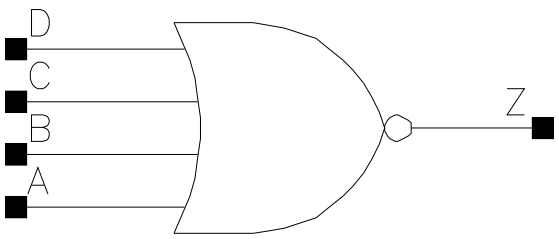
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	-2.050e-05	-5.846e-05	-7.174e-05	-1.070e-04
B (output stable)	2.226e-05	4.747e-05	7.251e-05	9.777e-05
C (output stable)	3.097e-05	8.963e-05	9.649e-05	1.505e-04
A to Z	3.300e-08	-1.835e-06	-3.137e-06	-2.729e-06
B to Z	4.080e-07	-2.480e-07	1.260e-07	5.510e-07
C to Z	1.087e-06	-5.201e-07	-2.880e-07	1.570e-07

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	1.904	2.2848
X32_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X32_P16
A	0.0008	0.0008	0.0009	0.0011
B	0.0009	0.0008	0.0010	0.0014
C	0.0007	0.0007	0.0010	0.0012
D	0.0008	0.0007	0.0010	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0361	0.0363	1.8956	0.9301
A to Z ↑	0.0541	0.0588	3.3172	1.6367
B to Z ↓	0.0344	0.0352	1.8944	0.9308
B to Z ↑	0.0543	0.0593	3.3171	1.6368
C to Z ↓	0.0352	0.0361	1.8899	0.9285
C to Z ↑	0.0552	0.0608	3.3154	1.6359

D to Z ↓	0.0343	0.0354	1.8893	0.9287
D to Z ↑	0.0559	0.0619	3.3164	1.6357
	X25_P16	**X32_P16**	**X25_P16**	**X32_P16**
A to Z ↓	0.0374	0.0397	0.6457	0.5078
A to Z ↑	0.0585	0.0568	1.1170	0.8471
B to Z ↓	0.0362	0.0384	0.6457	0.5072
B to Z ↑	0.0593	0.0573	1.1164	0.8470
C to Z ↓	0.0360	0.0388	0.6417	0.5050
C to Z ↑	0.0583	0.0575	1.1153	0.8462
D to Z ↓	0.0345	0.0366	0.6421	0.5052
D to Z ↑	0.0589	0.0578	1.1159	0.8462

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	6.076e-06	1.973e-09
X17_P16	8.692e-06	2.139e-09
X25_P16	1.287e-05	2.801e-09
X32_P16	1.532e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	7.660e-04	9.567e-04	1.353e-03	1.699e-03
B (output stable)	6.394e-04	8.327e-04	1.185e-03	1.469e-03
C (output stable)	6.998e-04	8.452e-04	1.326e-03	1.692e-03
D (output stable)	5.749e-04	7.251e-04	1.149e-03	1.457e-03
A to Z	5.277e-03	8.224e-03	1.249e-02	1.577e-02
B to Z	5.012e-03	7.981e-03	1.213e-02	1.535e-02
C to Z	5.287e-03	8.118e-03	1.171e-02	1.490e-02
D to Z	5.016e-03	7.877e-03	1.137e-02	1.443e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

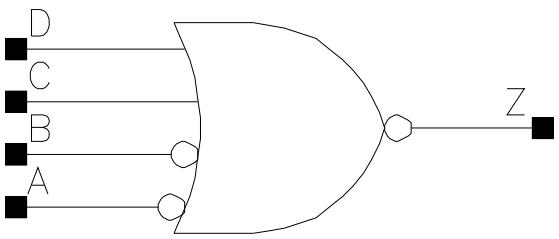
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	-4.632e-07	-5.418e-07	-6.644e-07	-7.967e-07
B (output stable)	7.152e-06	6.847e-06	1.066e-05	1.450e-05
C (output stable)	-5.974e-07	-6.331e-07	-6.322e-07	-7.059e-07
D (output stable)	7.742e-06	7.402e-06	1.098e-05	1.443e-05
A to Z	-9.800e-08	-3.794e-07	-3.460e-07	-4.844e-07
B to Z	1.810e-07	-1.832e-07	-2.474e-07	-2.353e-07
C to Z	-1.810e-07	-1.202e-07	-4.060e-07	-4.410e-07
D to Z	1.013e-07	9.500e-09	-2.344e-07	-3.267e-07

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X13_P16	1.200	1.496	1.7952
X19_P16	1.200	2.040	2.4480
X25_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0013	0.0013	0.0025	0.0024
B	0.0013	0.0018	0.0025	0.0025
C	0.0011	0.0021	0.0031	0.0041
D	0.0010	0.0020	0.0029	0.0039

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X13_P16	X6_P16	X13_P16
A to Z ↓	0.0274	0.0344	1.8711	0.9391
A to Z ↑	0.0332	0.0415	8.9161	4.6000
B to Z ↓	0.0251	0.0327	1.8695	0.9378
B to Z ↑	0.0341	0.0431	8.9173	4.6017
C to Z ↓	0.0097	0.0091	2.0307	0.9731
C to Z ↑	0.0232	0.0243	8.9550	4.6165

D to Z ↓	0.0075	0.0065	2.0387	0.9851
D to Z ↑	0.0204	0.0183	8.9738	4.6239
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0304	0.0333	0.6422	0.4843
A to Z ↑	0.0375	0.0406	3.0512	2.3044
B to Z ↓	0.0276	0.0308	0.6413	0.4837
B to Z ↑	0.0381	0.0416	3.0513	2.3044
C to Z ↓	0.0095	0.0093	0.6745	0.5056
C to Z ↑	0.0234	0.0234	3.0607	2.3103
D to Z ↓	0.0068	0.0064	0.6768	0.5083
D to Z ↑	0.0187	0.0176	3.0670	2.3155

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P16	5.446e-06	1.642e-09
X13_P16	8.468e-06	2.304e-09
X19_P16	1.339e-05	2.967e-09
X25_P16	1.587e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	1.233e-03	2.199e-03	3.316e-03	4.093e-03
B (output stable)	1.100e-03	2.089e-03	3.065e-03	3.860e-03
C (output stable)	6.319e-07	5.281e-05	8.023e-05	1.329e-04
D (output stable)	3.226e-05	1.414e-04	1.708e-04	2.938e-04
A to Z	5.156e-03	9.753e-03	1.461e-02	1.875e-02
B to Z	4.807e-03	9.247e-03	1.355e-02	1.772e-02
C to Z	1.854e-03	3.785e-03	5.450e-03	7.176e-03
D to Z	1.350e-03	2.334e-03	3.574e-03	4.389e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

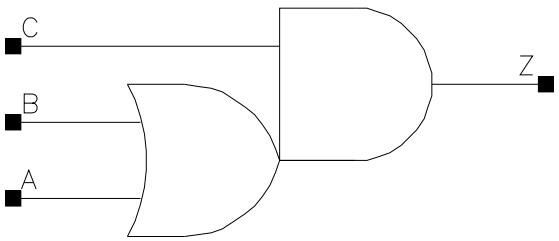
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	-9.324e-06	-3.372e-05	-3.870e-05	-5.680e-05
B (output stable)	-9.490e-06	-3.343e-05	-3.795e-05	-5.500e-05
C (output stable)	2.497e-05	4.437e-05	6.804e-05	8.881e-05
D (output stable)	4.425e-05	1.233e-04	1.352e-04	2.071e-04
A to Z	9.610e-07	-4.963e-06	-3.863e-06	-7.830e-06
B to Z	3.370e-07	-4.616e-06	-3.708e-06	-7.877e-06
C to Z	2.330e-07	-1.940e-07	-4.700e-08	4.970e-07
D to Z	1.273e-06	4.397e-07	1.804e-06	3.473e-07

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0012	0.0012	0.0023
B	0.0013	0.0013	0.0026
C	0.0013	0.0013	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0298	0.0356	1.9493	0.9726
A to Z ↑	0.0241	0.0275	3.3328	1.6387
B to Z ↓	0.0299	0.0362	1.9500	0.9737
B to Z ↑	0.0213	0.0251	3.3281	1.6374
C to Z ↓	0.0270	0.0304	1.9229	0.9534
C to Z ↑	0.0221	0.0251	3.3262	1.6365
	X33_P16		**X33_P16**	
A to Z ↓	0.0369		0.4952	
A to Z ↑	0.0294		0.8237	

B to Z ↓	0.0374		0.4954	
B to Z ↑	0.0265		0.8213	
C to Z ↓	0.0310		0.4839	
C to Z ↑	0.0261		0.8221	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	5.474e-06	1.310e-09
X17_P16	7.474e-06	1.476e-09
X33_P16	1.503e-05	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.371e-04	1.397e-04	2.833e-04
B (output stable)	1.264e-04	1.286e-04	2.482e-04
C (output stable)	7.473e-05	7.770e-05	1.441e-04
A to Z	3.896e-03	6.012e-03	1.251e-02
B to Z	3.409e-03	5.518e-03	1.152e-02
C to Z	4.263e-03	6.246e-03	1.288e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

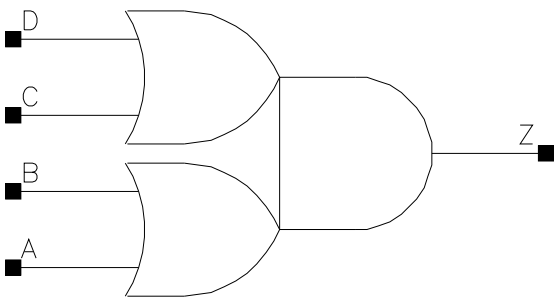
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-1.212e-06	-1.313e-06	-2.704e-06
B (output stable)	7.355e-06	7.482e-06	1.564e-05
C (output stable)	4.240e-08	5.382e-08	-7.480e-08
A to Z	-4.388e-07	-3.685e-07	-9.180e-07
B to Z	-1.085e-07	-1.913e-07	-7.668e-07
C to Z	-2.736e-07	-2.391e-07	-8.925e-07

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0008	0.0012	0.0024
B	0.0008	0.0013	0.0024
C	0.0008	0.0013	0.0024
D	0.0008	0.0012	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0507	0.0438	1.9306	0.9741
A to Z ↑	0.0330	0.0290	3.2663	1.6342
B to Z ↓	0.0517	0.0446	1.9315	0.9741
B to Z ↑	0.0314	0.0272	3.2635	1.6329

C to Z ↓	0.0437	0.0383	1.9097	0.9671
C to Z ↑	0.0323	0.0295	3.2657	1.6347
D to Z ↓	0.0440	0.0385	1.9107	0.9668
D to Z ↑	0.0301	0.0268	3.2629	1.6319
	X33_P16		**X33_P16**	
A to Z ↓	0.0449		0.5010	
A to Z ↑	0.0294		0.8215	
B to Z ↓	0.0437		0.5015	
B to Z ↑	0.0269		0.8199	
C to Z ↓	0.0387		0.4968	
C to Z ↑	0.0292		0.8204	
D to Z ↓	0.0372		0.4973	
D to Z ↑	0.0264		0.8193	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	5.306e-06	1.642e-09
X17_P16	9.857e-06	1.807e-09
X33_P16	1.875e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	3.328e-05	5.439e-05	1.649e-04
B (output stable)	1.598e-05	2.454e-05	9.130e-05
C (output stable)	1.116e-04	1.465e-04	3.922e-04
D (output stable)	9.412e-05	1.144e-04	2.961e-04
A to Z	4.704e-03	7.715e-03	1.536e-02
B to Z	4.437e-03	7.196e-03	1.391e-02
C to Z	4.037e-03	6.747e-03	1.338e-02
D to Z	3.771e-03	6.246e-03	1.197e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

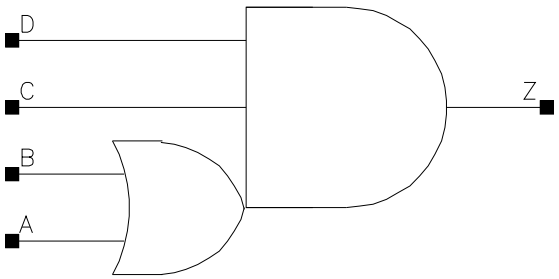
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-5.721e-07	-9.317e-07	-5.963e-06
B (output stable)	7.598e-06	1.490e-05	5.131e-05
C (output stable)	-1.449e-06	-1.007e-06	-1.489e-05
D (output stable)	7.293e-06	1.538e-05	5.290e-05
A to Z	-2.303e-07	-5.543e-07	-1.661e-06
B to Z	4.383e-08	-4.031e-07	-7.714e-07
C to Z	-3.701e-07	-3.505e-07	-6.440e-07
D to Z	-1.431e-07	-2.498e-07	-9.020e-07

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	1.088	1.3056
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0008	0.0013	0.0020	0.0024
B	0.0008	0.0013	0.0021	0.0025
C	0.0009	0.0013	0.0021	0.0025
D	0.0008	0.0013	0.0021	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0427	0.0409	2.0050	0.9780
A to Z ↑	0.0388	0.0367	3.3787	1.6413
B to Z ↓	0.0434	0.0402	2.0073	0.9779
B to Z ↑	0.0363	0.0329	3.3726	1.6389
C to Z ↓	0.0359	0.0339	1.9505	0.9553

C to Z ↑	0.0359	0.0334	3.3728	1.6369
D to Z ↓	0.0346	0.0325	1.9485	0.9533
D to Z ↑	0.0373	0.0346	3.3727	1.6372
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0425	0.0409	0.6652	0.4978
A to Z ↑	0.0373	0.0379	1.1107	0.8322
B to Z ↓	0.0414	0.0400	0.6656	0.4976
B to Z ↑	0.0339	0.0343	1.1080	0.8305
C to Z ↓	0.0354	0.0341	0.6501	0.4861
C to Z ↑	0.0344	0.0344	1.1088	0.8308
D to Z ↓	0.0334	0.0324	0.6479	0.4852
D to Z ↑	0.0346	0.0349	1.1093	0.8312

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	3.674e-06	1.476e-09
X17_P16	7.030e-06	1.807e-09
X25_P16	1.134e-05	2.801e-09
X33_P16	1.416e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	1.250e-04	2.379e-04	4.066e-04	4.481e-04
B (output stable)	1.218e-04	2.286e-04	3.996e-04	4.361e-04
C (output stable)	2.107e-05	4.155e-05	1.015e-04	1.138e-04
D (output stable)	6.057e-05	1.207e-04	3.596e-04	3.880e-04
A to Z	3.884e-03	7.098e-03	1.131e-02	1.406e-02
B to Z	3.629e-03	6.409e-03	1.023e-02	1.272e-02
C to Z	4.212e-03	7.534e-03	1.232e-02	1.500e-02
D to Z	4.008e-03	7.149e-03	1.139e-02	1.402e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

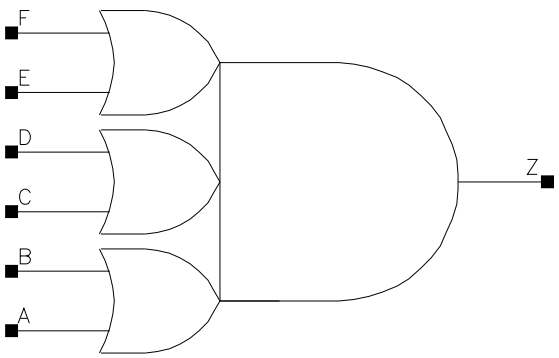
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	-1.269e-06	-2.946e-06	-2.865e-06	-3.134e-06
B (output stable)	9.077e-07	7.302e-06	1.028e-05	1.277e-05
C (output stable)	8.942e-08	4.147e-08	-2.150e-08	-4.254e-08
D (output stable)	-1.547e-07	-2.350e-07	-2.122e-08	-5.460e-08
A to Z	-2.087e-07	-1.970e-06	-2.697e-06	-3.516e-06
B to Z	-7.994e-08	-2.552e-07	-2.519e-07	-4.810e-07
C to Z	-1.195e-07	8.972e-07	1.700e-06	2.660e-06
D to Z	-2.608e-07	7.014e-07	2.106e-06	2.527e-06

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0009	0.0012	0.0021
B	0.0008	0.0012	0.0023
C	0.0008	0.0012	0.0022
D	0.0008	0.0012	0.0023
E	0.0008	0.0012	0.0022
F	0.0008	0.0012	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0580	0.0510	2.0738	1.0043
A to Z ↑	0.0425	0.0393	3.3585	1.6521
B to Z ↓	0.0588	0.0519	2.0748	1.0045
B to Z ↑	0.0407	0.0376	3.3600	1.6522
C to Z ↓	0.0528	0.0478	2.0563	1.0011
C to Z ↑	0.0428	0.0391	3.3605	1.6519
D to Z ↓	0.0538	0.0484	2.0569	1.0009
D to Z ↑	0.0405	0.0368	3.3574	1.6513
E to Z ↓	0.0452	0.0414	2.0331	0.9917
E to Z ↑	0.0400	0.0373	3.3569	1.6505
F to Z ↓	0.0464	0.0419	2.0339	0.9923
F to Z ↑	0.0377	0.0349	3.3542	1.6493
	X33_P16		**X33_P16**	
A to Z ↓	0.0515		0.5131	
A to Z ↑	0.0406		0.8334	
B to Z ↓	0.0526		0.5132	
B to Z ↑	0.0376		0.8315	
C to Z ↓	0.0470		0.5091	
C to Z ↑	0.0401		0.8332	
D to Z ↓	0.0479		0.5091	
D to Z ↑	0.0373		0.8312	
E to Z ↓	0.0410		0.5047	
E to Z ↑	0.0385		0.8318	
F to Z ↓	0.0417		0.5048	
F to Z ↑	0.0355		0.8303	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	5.708e-06	1.973e-09
X17_P16	1.036e-05	2.139e-09
X33_P16	1.983e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.855e-05	4.877e-05	9.223e-05
B (output stable)	1.683e-05	3.236e-05	5.573e-05
C (output stable)	6.879e-05	1.092e-04	2.212e-04
D (output stable)	5.725e-05	8.896e-05	1.832e-04
E (output stable)	1.937e-04	2.840e-04	5.431e-04
F (output stable)	1.779e-04	2.592e-04	5.026e-04
A to Z	5.468e-03	9.281e-03	1.826e-02
B to Z	5.186e-03	8.784e-03	1.727e-02
C to Z	4.943e-03	8.496e-03	1.659e-02
D to Z	4.676e-03	7.987e-03	1.561e-02
E to Z	4.263e-03	7.453e-03	1.463e-02
F to Z	4.019e-03	6.973e-03	1.370e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

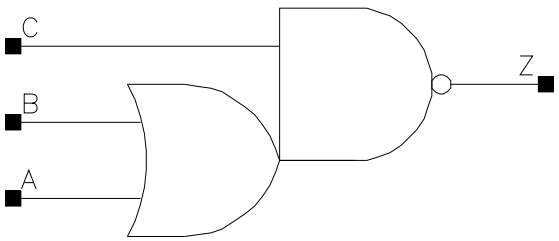
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-4.428e-07	-7.055e-07	-1.435e-06
B (output stable)	5.136e-06	1.015e-05	1.929e-05
C (output stable)	-6.791e-07	-7.619e-07	-2.286e-06
D (output stable)	4.920e-06	1.014e-05	1.847e-05
E (output stable)	-1.501e-06	-8.220e-07	-3.464e-06
F (output stable)	4.256e-06	1.004e-05	1.718e-05
A to Z	-2.766e-07	8.867e-08	-5.730e-07
B to Z	-1.035e-07	2.277e-07	1.679e-07
C to Z	-5.481e-07	-5.110e-07	-1.330e-06
D to Z	-2.092e-07	-3.247e-07	-9.493e-07
E to Z	-3.248e-07	-2.217e-07	-6.692e-07
F to Z	-2.602e-07	-2.101e-07	-5.760e-07

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X34_P16	1.200	2.720	3.2640
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X34_P16	X46_P16
A	0.0010	0.0030	0.0062	0.0081
B	0.0010	0.0028	0.0056	0.0075
C	0.0011	0.0032	0.0066	0.0086

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0122	0.0127	3.4728	1.1343
A to Z ↑	0.0174	0.0187	6.1898	2.0954
B to Z ↓	0.0093	0.0097	3.4180	1.1423
B to Z ↑	0.0166	0.0167	6.2216	2.1089
C to Z ↓	0.0108	0.0110	3.1399	1.0346
C to Z ↑	0.0171	0.0171	3.3544	1.1106
	X34_P16	**X46_P16**	**X34_P16**	**X46_P16**
A to Z ↓	0.0132	0.0132	0.5775	0.4403

A to Z ↑	0.0193	0.0191	1.0451	0.8012
B to Z ↓	0.0100	0.0101	0.5856	0.4481
B to Z ↑	0.0169	0.0170	1.0512	0.8062
C to Z ↓	0.0114	0.0113	0.5291	0.4041
C to Z ↑	0.0174	0.0172	0.5551	0.4230

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P16	3.598e-06	1.145e-09
X17_P16	1.020e-05	2.139e-09
X34_P16	2.036e-05	3.795e-09
X46_P16	2.678e-05	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	1.204e-04	4.237e-04	8.902e-04	1.109e-03
B (output stable)	1.112e-04	3.584e-04	7.738e-04	9.497e-04
C (output stable)	6.764e-05	2.294e-04	4.783e-04	6.016e-04
A to Z	1.695e-03	5.526e-03	1.148e-02	1.481e-02
B to Z	1.218e-03	3.684e-03	7.601e-03	9.897e-03
C to Z	2.063e-03	6.400e-03	1.322e-02	1.712e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

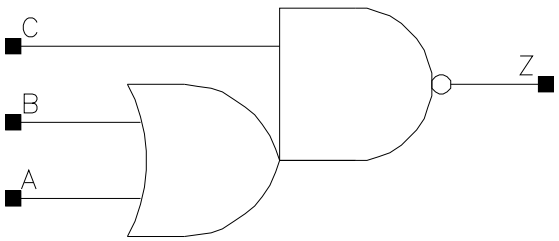
Pin Cycle (vdds)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	-6.640e-07	-4.636e-06	-1.224e-05	-1.428e-05
B (output stable)	8.001e-06	2.189e-05	4.899e-05	6.168e-05
C (output stable)	2.670e-08	-1.502e-07	-4.026e-07	-6.330e-07
A to Z	-1.020e-07	-1.220e-06	-4.610e-06	-5.060e-06
B to Z	-1.081e-07	2.850e-07	1.830e-07	6.960e-07
C to Z	2.416e-07	1.981e-06	3.415e-06	5.194e-06

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.544	0.6528
X11_P16	1.200	0.952	1.1424
X17_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X17_P16	X23_P16
A	0.0010	0.0021	0.0032	0.0044
B	0.0010	0.0022	0.0030	0.0040
C	0.0010	0.0021	0.0030	0.0041
	X46_P16			
A	0.0087			
B	0.0080			
C	0.0083			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0123	0.0125	3.5098	1.6347
A to Z ↑	0.0222	0.0225	6.4972	3.0710
B to Z ↓	0.0100	0.0101	3.4549	1.5942

B to Z ↑	0.0219	0.0221	6.5272	3.0856
C to Z ↓	0.0095	0.0095	3.2995	1.5300
C to Z ↑	0.0126	0.0126	3.5829	1.6860
	X17_P16	**X23_P16**	**X17_P16**	**X23_P16**
A to Z ↓	0.0120	0.0127	1.1347	0.8393
A to Z ↑	0.0213	0.0236	2.0361	1.5513
B to Z ↓	0.0095	0.0100	1.1320	0.8398
B to Z ↑	0.0207	0.0216	2.0458	1.5577
C to Z ↓	0.0092	0.0094	1.0734	0.7929
C to Z ↑	0.0118	0.0122	1.1204	0.8509
	X46_P16		**X46_P16**	
A to Z ↓	0.0126		0.4367	
A to Z ↑	0.0231		0.7830	
B to Z ↓	0.0098		0.4330	
B to Z ↑	0.0213		0.7867	
C to Z ↓	0.0095		0.4112	
C to Z ↑	0.0120		0.4293	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P16	3.820e-06	1.145e-09
X11_P16	7.684e-06	1.642e-09
X17_P16	1.126e-05	2.139e-09
X23_P16	1.536e-05	2.801e-09
X46_P16	2.956e-05	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	3.504e-05	7.564e-05	1.109e-04	2.180e-04
B (output stable)	1.793e-05	4.243e-05	5.842e-05	1.120e-04
C (output stable)	3.050e-04	7.326e-04	8.871e-04	1.390e-03
A to Z	2.188e-03	4.735e-03	6.579e-03	9.896e-03
B to Z	1.679e-03	3.663e-03	4.935e-03	7.034e-03
C to Z	1.268e-03	2.756e-03	3.820e-03	5.485e-03
	X46_P16			
A (output stable)	4.152e-04			
B (output stable)	2.169e-04			
C (output stable)	2.532e-03			
A to Z	1.911e-02			
B to Z	1.349e-02			
C to Z	1.057e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	-6.139e-07	-1.458e-06	-2.206e-06	-6.866e-06
B (output stable)	7.676e-06	1.680e-05	2.511e-05	3.537e-05
C (output stable)	1.990e-08	-2.191e-06	-2.464e-07	-4.667e-06
A to Z	-2.540e-07	-9.380e-07	-5.400e-07	-5.094e-06
B to Z	1.488e-07	-9.360e-07	1.209e-06	-1.742e-06
C to Z	5.086e-07	1.263e-06	1.103e-06	4.486e-06

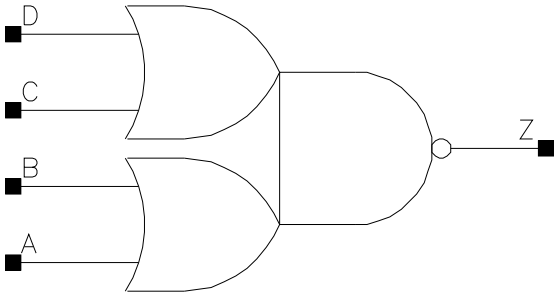
	X46_P16			
A (output stable)	-1.136e-05			
B (output stable)	6.386e-05			
C (output stable)	-8.587e-06			
A to Z	-8.060e-06			
B to Z	-3.433e-06			
C to Z	3.711e-06			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0011	0.0021	0.0031	0.0043
B	0.0010	0.0019	0.0029	0.0039
C	0.0010	0.0020	0.0030	0.0041
D	0.0010	0.0019	0.0027	0.0038
	X42_P16			
A	0.0087			
B	0.0080			
C	0.0083			
D	0.0077			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0138	0.0149	3.2008	1.5934
A to Z ↑	0.0259	0.0264	6.8244	3.1417
B to Z ↓	0.0117	0.0122	3.1385	1.5982
B to Z ↑	0.0254	0.0242	6.8428	3.1557
C to Z ↓	0.0126	0.0137	3.2876	1.6247
C to Z ↑	0.0184	0.0199	6.6887	3.1527
D to Z ↓	0.0100	0.0105	3.2100	1.6364
D to Z ↑	0.0175	0.0167	6.7207	3.1749
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0143	0.0145	1.0904	0.7845
A to Z ↑	0.0250	0.0259	2.1118	1.5563
B to Z ↓	0.0120	0.0118	1.0948	0.7843
B to Z ↑	0.0236	0.0240	2.1222	1.5630
C to Z ↓	0.0135	0.0134	1.1132	0.8002
C to Z ↑	0.0187	0.0191	2.1206	1.5598
D to Z ↓	0.0105	0.0104	1.1260	0.8042
D to Z ↑	0.0163	0.0165	2.1359	1.5707
	X42_P16		**X42_P16**	
A to Z ↓	0.0148		0.4108	
A to Z ↑	0.0259		0.7910	
B to Z ↓	0.0122		0.4068	
B to Z ↑	0.0242		0.7946	
C to Z ↓	0.0142		0.4198	
C to Z ↑	0.0194		0.7886	
D to Z ↓	0.0108		0.4171	
D to Z ↑	0.0168		0.7939	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P16	4.622e-06	1.310e-09
X10_P16	9.228e-06	2.139e-09
X15_P16	1.300e-05	2.635e-09
X21_P16	1.816e-05	3.464e-09
X42_P16	3.543e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	4.838e-05	1.612e-04	2.110e-04	3.028e-04
B (output stable)	2.114e-05	8.640e-05	1.087e-04	1.483e-04
C (output stable)	1.206e-04	3.777e-04	4.563e-04	6.657e-04
D (output stable)	9.699e-05	2.651e-04	3.277e-04	4.640e-04
A to Z	2.678e-03	6.104e-03	8.479e-03	1.194e-02
B to Z	2.185e-03	4.618e-03	6.476e-03	9.102e-03
C to Z	1.839e-03	4.365e-03	6.040e-03	8.396e-03
D to Z	1.389e-03	2.961e-03	4.157e-03	5.776e-03
	X42_P16			
A (output stable)	6.013e-04			
B (output stable)	3.034e-04			
C (output stable)	1.324e-03			
D (output stable)	9.299e-04			

A to Z	2.371e-02			
B to Z	1.808e-02			
C to Z	1.685e-02			
D to Z	1.159e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

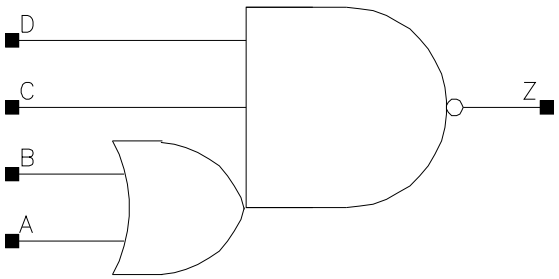
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	-8.825e-07	-5.874e-06	-4.892e-06	-9.113e-06
B (output stable)	1.431e-05	5.000e-05	4.692e-05	8.216e-05
C (output stable)	-9.398e-07	-1.582e-05	-9.893e-06	-2.072e-05
D (output stable)	1.421e-05	5.642e-05	4.923e-05	8.929e-05
A to Z	-1.267e-07	-9.153e-07	-2.122e-06	-2.834e-06
B to Z	-2.379e-07	-1.897e-07	3.960e-07	5.987e-07
C to Z	8.667e-09	5.193e-07	6.187e-07	9.427e-07
D to Z	1.862e-07	3.583e-07	1.096e-06	2.521e-06
	X42_P16			
A (output stable)	-1.552e-05			
B (output stable)	1.440e-04			
C (output stable)	-3.604e-05			
D (output stable)	1.565e-04			
A to Z	-6.087e-06			
B to Z	7.910e-07			
C to Z	2.317e-06			
D to Z	1.465e-06			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X21_P16	1.200	2.448	2.9376
X31_P16	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X21_P16	X31_P16
A	0.0010	0.0020	0.0040	0.0060
B	0.0012	0.0018	0.0035	0.0054
C	0.0010	0.0022	0.0043	0.0064
D	0.0010	0.0020	0.0040	0.0060

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0176	0.0170	4.3913	2.3438
A to Z ↑	0.0231	0.0214	6.1780	3.1126
B to Z ↓	0.0149	0.0131	4.4471	2.3572
B to Z ↑	0.0222	0.0190	6.2297	3.1318
C to Z ↓	0.0156	0.0161	4.1345	2.2031

C to Z ↑	0.0209	0.0204	3.2701	1.6454
D to Z ↓	0.0164	0.0157	4.1551	2.2145
D to Z ↑	0.0196	0.0184	3.3063	1.6495
	X21_P16	**X31_P16**	**X21_P16**	**X31_P16**
A to Z ↓	0.0173	0.0175	1.2209	0.8284
A to Z ↑	0.0210	0.0210	1.5557	1.0438
B to Z ↓	0.0133	0.0134	1.2288	0.8365
B to Z ↑	0.0187	0.0187	1.5650	1.0506
C to Z ↓	0.0160	0.0161	1.1491	0.7807
C to Z ↑	0.0201	0.0201	0.8318	0.5601
D to Z ↓	0.0159	0.0161	1.1543	0.7844
D to Z ↑	0.0182	0.0182	0.8333	0.5600

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P16	3.789e-06	1.476e-09
X10_P16	7.245e-06	2.139e-09
X21_P16	1.381e-05	3.464e-09
X31_P16	2.039e-05	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	2.321e-04	4.896e-04	9.225e-04	1.360e-03
B (output stable)	2.212e-04	4.748e-04	8.901e-04	1.310e-03
C (output stable)	4.026e-05	1.140e-04	2.197e-04	3.223e-04
D (output stable)	1.129e-04	3.934e-04	7.216e-04	1.060e-03
A to Z	2.528e-03	4.453e-03	8.688e-03	1.293e-02
B to Z	1.844e-03	3.062e-03	5.921e-03	8.858e-03
C to Z	3.123e-03	6.004e-03	1.159e-02	1.726e-02
D to Z	2.756e-03	4.972e-03	9.628e-03	1.435e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

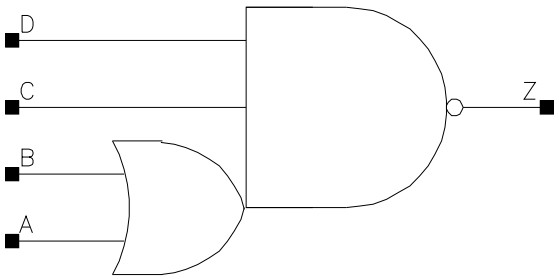
Pin Cycle (vdds)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	-3.295e-06	-4.735e-06	-8.811e-06	-1.193e-05
B (output stable)	6.890e-06	1.190e-05	1.815e-05	2.470e-05
C (output stable)	2.552e-08	-2.260e-08	-1.117e-07	-2.107e-07
D (output stable)	-2.376e-07	-4.880e-07	-1.208e-06	-1.660e-06
A to Z	-1.592e-06	-1.921e-06	-2.978e-06	-4.494e-06
B to Z	2.600e-08	5.790e-07	-1.280e-07	1.651e-06
C to Z	2.084e-06	8.910e-07	2.051e-06	3.048e-06
D to Z	1.417e-06	6.320e-07	6.180e-07	4.703e-07

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0011	0.0022	0.0033	0.0044
B	0.0010	0.0020	0.0030	0.0040
C	0.0010	0.0020	0.0031	0.0041
D	0.0010	0.0020	0.0030	0.0039

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0164	0.0178	4.4698	2.3292
A to Z ↑	0.0261	0.0285	6.0219	3.0633
B to Z ↓	0.0138	0.0146	4.4007	2.3341
B to Z ↑	0.0261	0.0269	6.0430	3.0759
C to Z ↓	0.0127	0.0144	4.2314	2.2229

C to Z ↑	0.0162	0.0172	3.3209	1.6781
D to Z ↓	0.0128	0.0135	4.2647	2.2386
D to Z ↑	0.0139	0.0141	3.3471	1.6923
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0176	0.0177	1.6023	1.2078
A to Z ↑	0.0275	0.0280	2.0625	1.5625
B to Z ↓	0.0146	0.0145	1.5978	1.2071
B to Z ↑	0.0263	0.0268	2.0714	1.5676
C to Z ↓	0.0140	0.0142	1.5244	1.1500
C to Z ↑	0.0164	0.0167	1.1191	0.8412
D to Z ↓	0.0134	0.0137	1.5359	1.1577
D to Z ↑	0.0136	0.0138	1.1284	0.8481

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P16	4.189e-06	1.476e-09
X10_P16	8.338e-06	2.139e-09
X15_P16	1.176e-05	2.635e-09
X21_P16	1.616e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	2.964e-05	7.599e-05	1.101e-04	1.420e-04
B (output stable)	2.054e-05	5.875e-05	7.904e-05	1.037e-04
C (output stable)	1.158e-04	2.472e-04	3.776e-04	4.953e-04
D (output stable)	1.999e-04	6.880e-04	8.394e-04	1.243e-03
A to Z	3.034e-03	6.640e-03	9.476e-03	1.287e-02
B to Z	2.464e-03	5.142e-03	7.321e-03	9.972e-03
C to Z	1.958e-03	4.375e-03	6.112e-03	8.407e-03
D to Z	1.591e-03	3.346e-03	4.763e-03	6.465e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

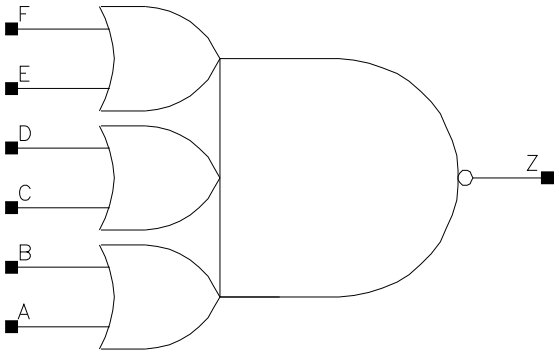
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	-4.302e-07	-3.230e-06	-2.832e-06	-5.087e-06
B (output stable)	3.475e-06	1.388e-05	1.214e-05	2.205e-05
C (output stable)	1.128e-08	-3.644e-07	-1.089e-06	-8.111e-07
D (output stable)	1.398e-08	-2.383e-06	-2.632e-06	-4.429e-06
A to Z	-2.570e-07	-3.192e-06	-2.731e-06	-4.764e-06
B to Z	1.470e-07	-1.873e-06	8.200e-08	-1.821e-06
C to Z	1.913e-07	1.597e-06	1.514e-06	2.255e-06
D to Z	2.780e-07	3.273e-06	1.592e-06	3.929e-06

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	1.088	1.3056
X9_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X9_P16
A	0.0009	0.0022
B	0.0009	0.0020
C	0.0009	0.0021
D	0.0008	0.0019
E	0.0008	0.0020
F	0.0008	0.0019

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X9_P16	X3_P16	X9_P16
A to Z ↓	0.0215	0.0228	5.1172	2.1121
A to Z ↑	0.0353	0.0340	8.4079	3.0856
B to Z ↓	0.0197	0.0197	5.1589	2.1164
B to Z ↑	0.0362	0.0325	8.4298	3.0954
C to Z ↓	0.0206	0.0214	5.1558	2.1233
C to Z ↑	0.0301	0.0289	8.4293	3.0802
D to Z ↓	0.0184	0.0182	5.2002	2.1305
D to Z ↑	0.0306	0.0271	8.4584	3.0938
E to Z ↓	0.0178	0.0190	5.2206	2.1377
E to Z ↑	0.0225	0.0222	8.4661	3.0877
F to Z ↓	0.0157	0.0155	5.2700	2.1450
F to Z ↑	0.0227	0.0196	8.5147	3.1070

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P16	4.926e-06	1.807e-09
X9_P16	1.226e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P16	X9_P16
A (output stable)	3.817e-05	1.444e-04
B (output stable)	2.406e-05	1.023e-04
C (output stable)	9.475e-05	3.145e-04
D (output stable)	7.973e-05	2.400e-04
E (output stable)	2.522e-04	6.238e-04
F (output stable)	2.397e-04	5.706e-04
A to Z	3.555e-03	9.264e-03
B to Z	3.170e-03	7.751e-03
C to Z	2.851e-03	7.469e-03
D to Z	2.478e-03	6.058e-03
E to Z	2.032e-03	5.593e-03
F to Z	1.692e-03	4.222e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

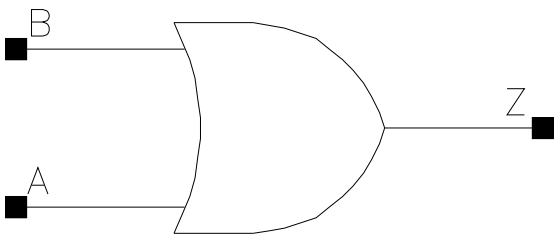
Pin Cycle (vdds)	X3_P16	X9_P16
A (output stable)	-5.542e-07	-4.782e-06
B (output stable)	7.136e-06	4.149e-05
C (output stable)	-6.195e-07	-1.038e-05
D (output stable)	7.350e-06	3.803e-05
E (output stable)	-6.450e-07	-7.251e-06
F (output stable)	7.158e-06	3.291e-05
A to Z	1.730e-07	3.414e-06
B to Z	2.962e-07	1.721e-06
C to Z	-4.470e-07	-2.419e-06
D to Z	-2.158e-07	-5.251e-07
E to Z	2.194e-07	6.828e-07
F to Z	1.656e-08	1.898e-07

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X33_P16	1.200	1.360	1.6320
X50_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P16	X16_P16	X33_P16	X50_P16
A	0.0009	0.0012	0.0023	0.0024
B	0.0008	0.0012	0.0023	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0392	0.0356	1.9674	0.9904
A to Z ↑	0.0231	0.0244	3.2961	1.6590
B to Z ↓	0.0393	0.0357	1.9671	0.9908
B to Z ↑	0.0217	0.0225	3.2937	1.6597
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0370	0.0440	0.4896	0.3376
A to Z ↑	0.0243	0.0244	0.8096	0.5462
B to Z ↓	0.0355	0.0430	0.4897	0.3374
B to Z ↑	0.0220	0.0225	0.8095	0.5461

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	4.463e-06	1.145e-09
X16_P16	7.573e-06	1.310e-09
X33_P16	1.521e-05	2.139e-09
X50_P16	2.050e-05	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	3.388e-05	6.190e-05	2.053e-04	1.924e-04
B (output stable)	8.813e-06	1.443e-05	1.326e-04	1.151e-04
A to Z	3.513e-03	5.830e-03	1.225e-02	1.709e-02
B to Z	3.246e-03	5.357e-03	1.086e-02	1.575e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

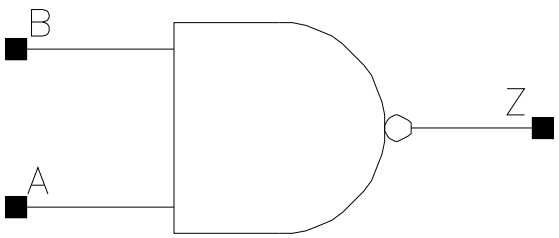
Pin Cycle (vdds)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	-8.824e-07	-1.387e-06	-8.099e-06	-7.692e-06
B (output stable)	1.434e-05	2.566e-05	1.085e-04	1.065e-04
A to Z	-2.332e-07	-1.940e-07	-3.168e-06	-3.205e-06
B to Z	-9.880e-08	-1.756e-07	-5.328e-07	-2.030e-07

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X16_P16	1.200	0.952	1.1424
X24_P16	1.200	1.088	1.3056
X32_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P16	X16_P16	X24_P16	X32_P16
A	0.0012	0.0012	0.0012	0.0012
B	0.0013	0.0013	0.0013	0.0013

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0308	0.0328	1.8906	0.9834
A to Z ↑	0.0358	0.0372	3.3211	1.6928
B to Z ↓	0.0322	0.0343	1.8919	0.9822
B to Z ↑	0.0338	0.0346	3.3168	1.6922
	X24_P16	**X32_P16**	**X24_P16**	**X32_P16**
A to Z ↓	0.0369	0.0377	0.6664	0.4999
A to Z ↑	0.0400	0.0415	1.1298	0.8440
B to Z ↓	0.0384	0.0396	0.6666	0.5000
B to Z ↑	0.0373	0.0396	1.1298	0.8446

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	7.750e-06	1.476e-09
X16_P16	1.018e-05	1.642e-09
X24_P16	1.245e-05	1.807e-09
X32_P16	1.536e-05	1.973e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	2.796e-05	2.812e-05	2.818e-05	3.028e-05
B (output stable)	5.200e-05	5.231e-05	5.238e-05	5.898e-05
A to Z	6.598e-03	7.877e-03	1.007e-02	1.346e-02
B to Z	6.259e-03	7.549e-03	9.754e-03	1.313e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

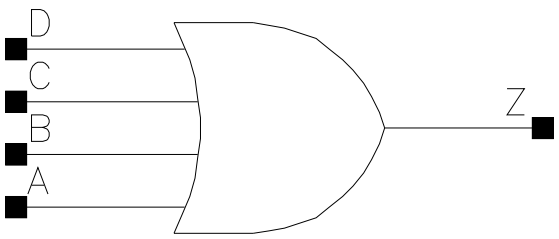
Pin Cycle (vdds)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	-3.770e-09	7.100e-10	1.760e-09	-1.490e-09
B (output stable)	4.000e-09	3.500e-09	5.000e-09	1.380e-08
A to Z	-2.634e-07	-2.165e-07	-1.550e-07	-4.323e-07
B to Z	-1.127e-07	2.810e-08	-8.890e-08	-4.538e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P16	1.200	2.176	2.6112
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P16	X27_P16
A	0.0021	0.0024
B	0.0019	0.0024
C	0.0021	0.0025
D	0.0020	0.0025

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P16	X27_P16	X20_P16	X27_P16
A to Z ↓	0.0401	0.0419	1.1192	0.8362
A to Z ↑	0.0255	0.0245	1.0863	0.8103
B to Z ↓	0.0391	0.0404	1.1193	0.8364
B to Z ↑	0.0238	0.0224	1.0849	0.8088
C to Z ↓	0.0395	0.0412	1.1177	0.8354
C to Z ↑	0.0242	0.0237	1.0876	0.8120
D to Z ↓	0.0386	0.0400	1.1185	0.8353
D to Z ↑	0.0225	0.0218	1.0864	0.8121

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X20_P16	1.449e-05	3.132e-09
X27_P16	2.033e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X20_P16	X27_P16
A (output stable)	2.726e-03	3.735e-03
B (output stable)	2.249e-03	3.067e-03
C (output stable)	2.451e-03	3.490e-03
D (output stable)	1.945e-03	2.817e-03
A to Z	1.113e-02	1.549e-02
B to Z	1.014e-02	1.404e-02
C to Z	9.817e-03	1.349e-02
D to Z	8.832e-03	1.217e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

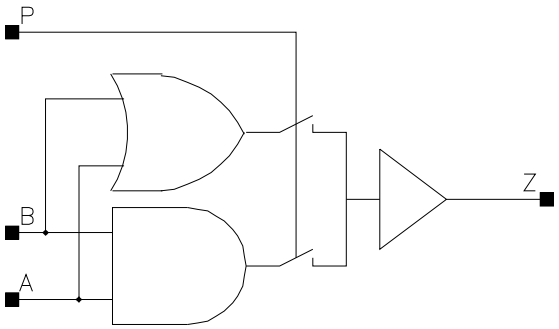
Pin Cycle (vdds)	X20_P16	X27_P16
A (output stable)	-2.727e-06	-6.017e-06
B (output stable)	2.371e-05	5.090e-05
C (output stable)	-4.706e-06	-1.423e-05
D (output stable)	2.620e-05	5.724e-05
A to Z	-1.475e-06	-2.587e-06
B to Z	1.060e-07	8.150e-07
C to Z	-1.109e-06	-2.886e-06
D to Z	3.480e-07	5.510e-07

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X16_P16	1.200	1.224	1.4688
X25_P16	1.200	2.040	2.4480
X33_P16	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0015	0.0022	0.0040	0.0040
B	0.0014	0.0022	0.0045	0.0045
P	0.0008	0.0012	0.0023	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0480	0.0442	2.0089	0.9824
A to Z ↑	0.0304	0.0287	3.3415	1.6709
B to Z ↓	0.0478	0.0443	2.0213	0.9903
B to Z ↑	0.0318	0.0300	3.3431	1.6746
P to Z ↓	0.0437	0.0409	2.0238	0.9907
P to Z ↑	0.0309	0.0293	3.3419	1.6714
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**

A to Z ↓	0.0422	0.0456	0.6663	0.5055
A to Z ↑	0.0284	0.0304	1.1220	0.8414
B to Z ↓	0.0419	0.0451	0.6709	0.5085
B to Z ↑	0.0300	0.0318	1.1238	0.8425
P to Z ↓	0.0393	0.0427	0.6715	0.5090
P to Z ↑	0.0288	0.0307	1.1219	0.8401

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	5.253e-06	1.642e-09
X16_P16	1.000e-05	1.973e-09
X25_P16	1.697e-05	2.967e-09
X33_P16	1.901e-05	3.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	6.730e-05	1.071e-04	2.382e-04	2.351e-04
B (output stable)	1.330e-04	1.862e-04	3.564e-04	3.576e-04
P (output stable)	1.553e-04	2.573e-04	4.406e-04	4.491e-04
A to Z	4.111e-03	7.150e-03	1.217e-02	1.449e-02
B to Z	3.980e-03	6.950e-03	1.162e-02	1.397e-02
P to Z	3.632e-03	6.437e-03	1.090e-02	1.322e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

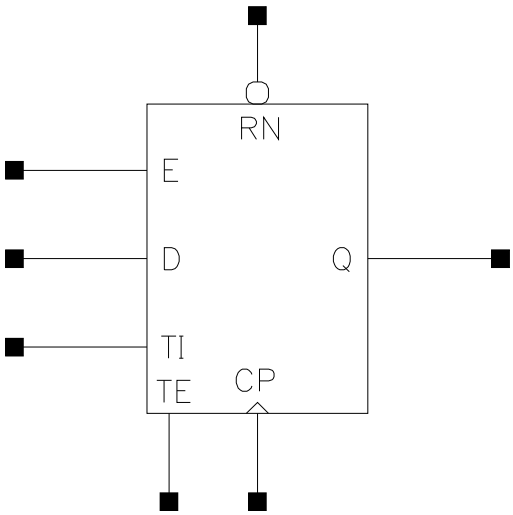
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	-2.268e-06	-2.950e-06	-4.797e-06	-4.678e-06
B (output stable)	-6.450e-06	-2.624e-06	1.765e-05	1.692e-05
P (output stable)	2.398e-05	4.379e-05	5.917e-05	5.994e-05
A to Z	-1.228e-06	-1.791e-06	-3.752e-06	-3.566e-06
B to Z	-1.057e-06	-1.156e-06	-3.188e-06	-3.157e-06
P to Z	-1.996e-07	-2.965e-07	-1.068e-06	-1.067e-06

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.488	5.3856
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0008	0.0008	0.0008
E	0.0011	0.0013	0.0013	0.0013
RN	0.0010	0.0009	0.0009	0.0010
TE	0.0011	0.0011	0.0011	0.0011

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to Q ↓	0.0862	0.0462	4.3321	1.9630
CP to Q ↑	0.0699	0.0594	6.5703	3.3063
RN to Q ↓	0.0602	0.0712	3.7852	1.8986
	X17_P16	X33_P16	X17_P16	X33_P16
CP to Q ↓	0.0799	0.0854	0.9446	0.4957
CP to Q ↑	0.0972	0.1029	1.6222	0.8252
RN to Q ↓	0.0968	0.1033	0.9444	0.4965

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1166	0.0780	0.0779	0.0779
CP ↑	min_pulse_width to CP	0.0801	0.0386	0.0301	0.0301
D ↓	hold_rising to CP	-0.1277	-0.0672	-0.0703	-0.0703
D ↑	hold_rising to CP	-0.0725	-0.0242	-0.0238	-0.0238
D ↓	setup_rising to CP	0.1726	0.1116	0.1147	0.1147
D ↑	setup_rising to CP	0.1073	0.0566	0.0566	0.0566
E ↓	hold_rising to CP	-0.0845	-0.0842	-0.0842	-0.0842
E ↑	hold_rising to CP	-0.0676	-0.0242	-0.0242	-0.0242
E ↓	setup_rising to CP	0.1482	0.1536	0.1536	0.1536
E ↑	setup_rising to CP	0.1614	0.1147	0.1147	0.1147
RN ↓	min_pulse_width to RN	0.0779	0.0876	0.0735	0.0757
RN ↑	recovery_rising to CP	0.0197	0.0197	0.0197	0.0197
RN ↑	removal_rising to CP	-0.0153	-0.0105	-0.0105	-0.0105
TE ↓	hold_rising to CP	-0.0601	-0.0429	-0.0429	-0.0454
TE ↑	hold_rising to CP	-0.0481	-0.0286	-0.0279	-0.0279
TE ↓	setup_rising to CP	0.1022	0.0897	0.0897	0.0897
TE ↑	setup_rising to CP	0.2053	0.1442	0.1442	0.1467
TI ↓	hold_rising to CP	-0.1668	-0.0874	-0.0874	-0.0874
TI ↑	hold_rising to CP	-0.0569	-0.0299	-0.0297	-0.0297
TI ↓	setup_rising to CP	0.2079	0.1319	0.1319	0.1319
TI ↑	setup_rising to CP	0.0881	0.0610	0.0610	0.0610

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.871e-05	6.340e-09
X8_P16	1.984e-05	5.948e-09
X17_P16	2.343e-05	6.279e-09
X33_P16	2.767e-05	6.611e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

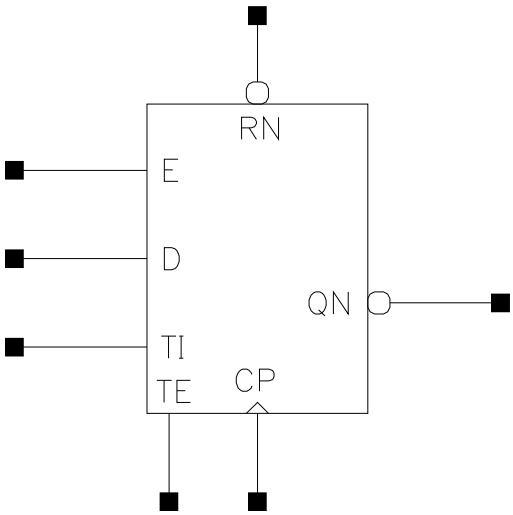
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.985e-03	6.041e-03	6.055e-03	6.062e-03
Clock 100Mhz Data 25Mhz	9.986e-03	1.016e-02	1.117e-02	1.249e-02
Clock 100Mhz Data 50Mhz	1.399e-02	1.427e-02	1.628e-02	1.891e-02
Clock = 0 Data 100Mhz	9.203e-03	8.900e-03	8.799e-03	8.751e-03
Clock = 1 Data 100Mhz	3.319e-03	3.405e-03	3.435e-03	3.450e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.624	5.5488
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0008	0.0008	0.0008
E	0.0011	0.0013	0.0013	0.0013
RN	0.0010	0.0010	0.0010	0.0010
TE	0.0011	0.0011	0.0011	0.0011

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to QN ↓	0.0862	0.0804	3.5303	1.8916
CP to QN ↑	0.0953	0.0609	6.4294	3.2219
RN to QN ↑	0.0749	0.0791	6.4133	3.2303
	X17_P16	X33_P16	X17_P16	X33_P16
CP to QN ↓	0.0779	0.0834	0.9450	0.4960
CP to QN ↑	0.0648	0.0713	1.6234	0.8266
RN to QN ↑	0.0879	0.0925	1.6217	0.8253

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1160	0.0779	0.0780	0.0780
CP ↑	min_pulse_width to CP	0.0579	0.0301	0.0349	0.0397
D ↓	hold_rising to CP	-0.1333	-0.0672	-0.0672	-0.0676
D ↑	hold_rising to CP	-0.0725	-0.0238	-0.0242	-0.0242
D ↓	setup_rising to CP	0.1748	0.1147	0.1147	0.1147
D ↑	setup_rising to CP	0.1073	0.0566	0.0566	0.0566
E ↓	hold_rising to CP	-0.0845	-0.0842	-0.0842	-0.0845
E ↑	hold_rising to CP	-0.0676	-0.0242	-0.0242	-0.0242
E ↓	setup_rising to CP	0.1509	0.1536	0.1536	0.1536
E ↑	setup_rising to CP	0.1614	0.1147	0.1147	0.1147
RN ↓	min_pulse_width to RN	0.0752	0.0735	0.0876	0.0947
RN ↑	recovery_rising to CP	0.0197	0.0223	0.0197	0.0197
RN ↑	removal_rising to CP	-0.0153	-0.0101	-0.0105	-0.0105
TE ↓	hold_rising to CP	-0.0601	-0.0429	-0.0429	-0.0429
TE ↑	hold_rising to CP	-0.0481	-0.0279	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1022	0.0897	0.0897	0.0897
TE ↑	setup_rising to CP	0.2053	0.1467	0.1467	0.1467
TI ↓	hold_rising to CP	-0.1683	-0.0874	-0.0874	-0.0876
TI ↑	hold_rising to CP	-0.0569	-0.0297	-0.0299	-0.0299
TI ↓	setup_rising to CP	0.2079	0.1319	0.1319	0.1319
TI ↑	setup_rising to CP	0.0881	0.0610	0.0610	0.0610

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.918e-05	6.340e-09
X8_P16	2.051e-05	6.114e-09
X17_P16	2.425e-05	6.279e-09
X33_P16	2.907e-05	6.611e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

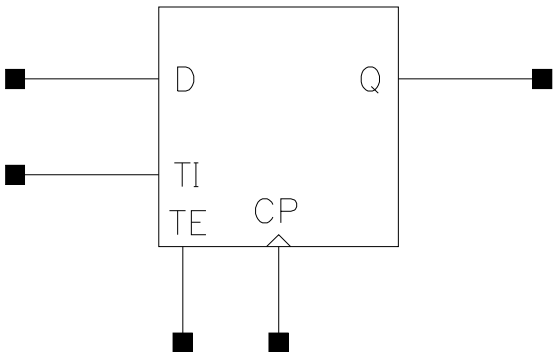
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.985e-03	6.041e-03	6.054e-03	6.061e-03
Clock 100Mhz Data 25Mhz	9.887e-03	1.021e-02	1.111e-02	1.238e-02
Clock 100Mhz Data 50Mhz	1.379e-02	1.438e-02	1.616e-02	1.871e-02
Clock = 0 Data 100Mhz	9.203e-03	8.901e-03	8.803e-03	8.753e-03
Clock = 1 Data 100Mhz	3.317e-03	3.407e-03	3.439e-03	3.455e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.400	4.0800
X8_P16	1.200	3.128	3.7536
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0011	0.0009	0.0009	0.0009
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0705	0.0428	4.0686	1.9558
CP to Q ↑	0.0630	0.0543	6.5950	3.2685
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0664	0.0737	0.9280	0.4879
CP to Q ↑	0.0960	0.1024	1.6188	0.8246

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1069	0.1137	0.1137	0.1137
CP ↑	min_pulse_width to CP	0.0579	0.0301	0.0301	0.0301
D ↓	hold_rising to CP	-0.0845	-0.0365	-0.0365	-0.0365
D ↑	hold_rising to CP	-0.0286	-0.0016	-0.0016	-0.0047
D ↓	setup_rising to CP	0.1193	0.0809	0.0809	0.0809
D ↑	setup_rising to CP	0.0560	0.0295	0.0295	0.0295
TE ↓	hold_rising to CP	-0.0503	-0.0282	-0.0307	-0.0307
TE ↑	hold_rising to CP	-0.0383	-0.0211	-0.0211	-0.0211
TE ↓	setup_rising to CP	0.0942	0.0757	0.0757	0.0757
TE ↑	setup_rising to CP	0.1858	0.1538	0.1538	0.1538
TI ↓	hold_rising to CP	-0.1584	-0.1000	-0.1000	-0.1000
TI ↑	hold_rising to CP	-0.0421	-0.0213	-0.0208	-0.0208
TI ↓	setup_rising to CP	0.1930	0.1493	0.1493	0.1493
TI ↑	setup_rising to CP	0.0720	0.0512	0.0512	0.0512

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.475e-05	4.623e-09
X8_P16	1.596e-05	4.292e-09
X17_P16	2.086e-05	4.789e-09
X33_P16	2.484e-05	5.120e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

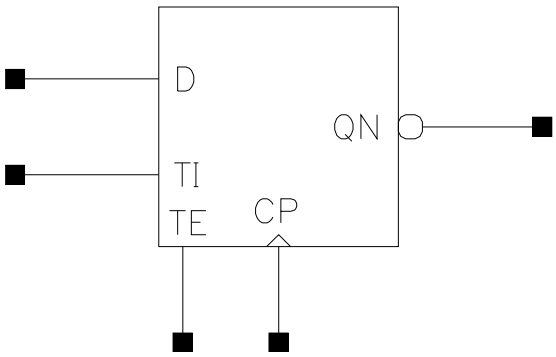
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.437e-03	5.509e-03	5.528e-03	5.538e-03
Clock 100Mhz Data 25Mhz	8.283e-03	8.419e-03	9.444e-03	1.054e-02
Clock 100Mhz Data 50Mhz	1.113e-02	1.133e-02	1.336e-02	1.554e-02
Clock = 0 Data 100Mhz	7.313e-03	6.873e-03	6.723e-03	6.649e-03
Clock = 1 Data 100Mhz	1.877e-03	9.700e-04	6.677e-04	5.166e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.536	4.2432
X8_P16	1.200	3.264	3.9168
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0011	0.0009	0.0009	0.0009
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0813	0.0862	4.0304	1.9596
CP to QN ↑	0.0763	0.0561	6.5522	3.2329
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0673	0.0751	0.9284	0.4886
CP to QN ↑	0.0571	0.0635	1.6199	0.8240

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1039	0.1156	0.1156	0.1156
CP ↑	min_pulse_width to CP	0.0434	0.0301	0.0301	0.0349
D ↓	hold_rising to CP	-0.0845	-0.0361	-0.0365	-0.0365
D ↑	hold_rising to CP	-0.0282	-0.0047	-0.0016	-0.0016
D ↓	setup_rising to CP	0.1168	0.0809	0.0809	0.0809
D ↑	setup_rising to CP	0.0560	0.0295	0.0295	0.0295
TE ↓	hold_rising to CP	-0.0503	-0.0307	-0.0282	-0.0282
TE ↑	hold_rising to CP	-0.0383	-0.0211	-0.0211	-0.0211
TE ↓	setup_rising to CP	0.0946	0.0757	0.0757	0.0757
TE ↑	setup_rising to CP	0.1832	0.1538	0.1569	0.1569
TI ↓	hold_rising to CP	-0.1586	-0.1000	-0.1000	-0.1000
TI ↑	hold_rising to CP	-0.0431	-0.0208	-0.0213	-0.0213
TI ↓	setup_rising to CP	0.1932	0.1493	0.1493	0.1493
TI ↑	setup_rising to CP	0.0735	0.0512	0.0512	0.0512

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.485e-05	4.789e-09
X8_P16	1.604e-05	4.457e-09
X17_P16	2.080e-05	4.789e-09
X33_P16	2.478e-05	5.120e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

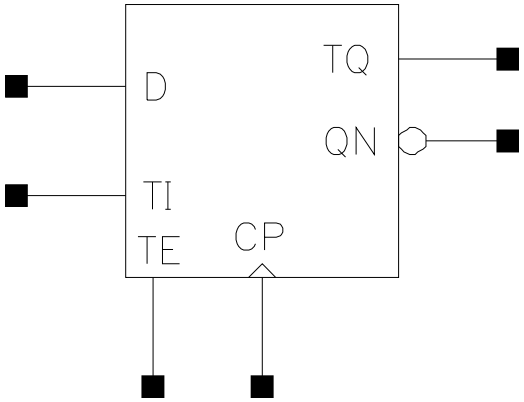
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.387e-03	5.503e-03	5.542e-03	5.561e-03
Clock 100Mhz Data 25Mhz	8.242e-03	8.565e-03	9.414e-03	1.051e-02
Clock 100Mhz Data 50Mhz	1.110e-02	1.163e-02	1.329e-02	1.547e-02
Clock = 0 Data 100Mhz	7.340e-03	6.884e-03	6.733e-03	6.657e-03
Clock = 1 Data 100Mhz	1.866e-03	9.880e-04	6.953e-04	5.490e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.536	4.2432
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0014	0.0011	0.0011	0.0011
D	0.0011	0.0009	0.0009	0.0009
TE	0.0010	0.0012	0.0012	0.0012

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0904	0.0780	3.6613	1.8999
CP to QN ↑	0.0942	0.0595	6.4443	3.2418
CP to TQ ↓	0.0640	0.0390	5.0831	3.5385
CP to TQ ↑	0.0646	0.0540	11.9364	8.6560
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0743	0.0813	0.9526	0.5007
CP to QN ↑	0.0618	0.0668	1.6384	0.8395
CP to TQ ↓	0.0408	0.0426	4.6040	4.6266
CP to TQ ↑	0.0548	0.0565	11.0105	11.5891

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1045	0.1137	0.1137	0.1137
CP ↑	min_pulse_width to CP	0.0579	0.0301	0.0338	0.0349
D ↓	hold_rising to CP	-0.0820	-0.0365	-0.0365	-0.0365
D ↑	hold_rising to CP	-0.0286	-0.0016	-0.0016	-0.0016
D ↓	setup_rising to CP	0.1137	0.0809	0.0809	0.0809
D ↑	setup_rising to CP	0.0560	0.0295	0.0295	0.0295
TE ↓	hold_rising to CP	-0.0503	-0.0282	-0.0282	-0.0282
TE ↑	hold_rising to CP	-0.0383	-0.0211	-0.0211	-0.0211
TE ↓	setup_rising to CP	0.0946	0.0757	0.0757	0.0757
TE ↑	setup_rising to CP	0.1802	0.1541	0.1538	0.1541
TI ↓	hold_rising to CP	-0.1586	-0.0985	-0.0985	-0.0985
TI ↑	hold_rising to CP	-0.0436	-0.0213	-0.0213	-0.0213
TI ↓	setup_rising to CP	0.1932	0.1478	0.1478	0.1478
TI ↑	setup_rising to CP	0.0735	0.0512	0.0512	0.0512

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.614e-05	5.131e-09
X8_P16	1.778e-05	4.789e-09
X17_P16	2.020e-05	4.954e-09
X33_P16	2.493e-05	5.286e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16

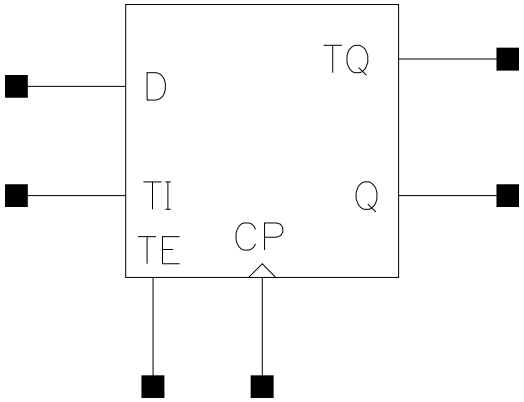
Clock 100Mhz Data 0Mhz	5.520e-03	5.551e-03	5.560e-03	5.565e-03
Clock 100Mhz Data 25Mhz	8.664e-03	8.949e-03	9.431e-03	1.070e-02
Clock 100Mhz Data 50Mhz	1.181e-02	1.235e-02	1.330e-02	1.583e-02
Clock = 0 Data 100Mhz	7.336e-03	6.888e-03	6.742e-03	6.667e-03
Clock = 1 Data 100Mhz	1.878e-03	9.690e-04	6.661e-04	5.147e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.400	4.0800
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0011	0.0009	0.0009	0.0009

TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0937	0.0480	4.3270	1.9610
CP to Q ↑	0.0725	0.0578	6.6726	3.2898
CP to TQ ↓	0.0893	0.0497	4.3353	4.7337
CP to TQ ↑	0.0742	0.0631	8.6849	11.7503
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0683	0.0757	0.9538	0.4981
CP to Q ↑	0.0980	0.1041	1.6498	0.8282
CP to TQ ↓	0.0710	0.0794	4.4871	4.5795
CP to TQ ↑	0.1035	0.1118	11.3788	11.4927

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1069	0.1137	0.1156	0.1156
CP ↑	min_pulse_width to CP	0.0820	0.0349	0.0301	0.0301
D ↓	hold_rising to CP	-0.0845	-0.0365	-0.0361	-0.0361
D ↑	hold_rising to CP	-0.0286	-0.0016	-0.0047	-0.0047
D ↓	setup_rising to CP	0.1193	0.0809	0.0809	0.0809
D ↑	setup_rising to CP	0.0560	0.0295	0.0295	0.0295
TE ↓	hold_rising to CP	-0.0503	-0.0282	-0.0307	-0.0307
TE ↑	hold_rising to CP	-0.0383	-0.0211	-0.0211	-0.0241
TE ↓	setup_rising to CP	0.0942	0.0757	0.0757	0.0757
TE ↑	setup_rising to CP	0.1858	0.1538	0.1538	0.1538
TI ↓	hold_rising to CP	-0.1586	-0.0986	-0.1000	-0.1000
TI ↑	hold_rising to CP	-0.0421	-0.0213	-0.0208	-0.0208
TI ↓	setup_rising to CP	0.1930	0.1478	0.1493	0.1493
TI ↑	setup_rising to CP	0.0720	0.0512	0.0512	0.0512

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.617e-05	4.954e-09
X8_P16	1.698e-05	4.623e-09
X17_P16	2.173e-05	4.954e-09
X33_P16	2.566e-05	5.286e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

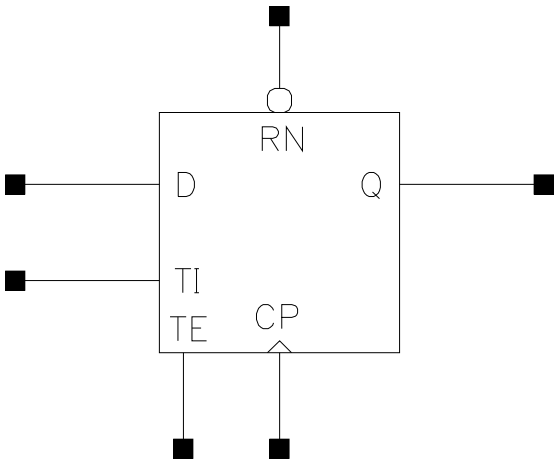
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.417e-03	5.498e-03	5.522e-03	5.533e-03
Clock 100Mhz Data 25Mhz	8.838e-03	8.749e-03	9.732e-03	1.088e-02
Clock 100Mhz Data 50Mhz	1.226e-02	1.200e-02	1.394e-02	1.623e-02
Clock = 0 Data 100Mhz	7.299e-03	6.860e-03	6.716e-03	6.645e-03
Clock = 1 Data 100Mhz	1.864e-03	9.618e-04	6.613e-04	5.111e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.672	4.4064
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0011	0.0008	0.0008	0.0008
RN	0.0010	0.0009	0.0009	0.0009
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0852	0.0461	4.3922	1.9669
CP to Q ↑	0.0692	0.0584	6.5999	3.3069
RN to Q ↓	0.0597	0.0712	3.8065	1.9040
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0694	0.0772	0.9364	0.4946
CP to Q ↑	0.0870	0.0928	1.6173	0.8238
RN to Q ↓	0.0864	0.0942	0.9361	0.4948

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1185	0.1156	0.1185	0.1185
CP ↑	min_pulse_width to CP	0.0724	0.0349	0.0301	0.0301
D ↓	hold_rising to CP	-0.0747	-0.0268	-0.0268	-0.0268
D ↑	hold_rising to CP	-0.0331	-0.0065	-0.0095	-0.0095
D ↓	setup_rising to CP	0.1193	0.0756	0.0756	0.0756
D ↑	setup_rising to CP	0.0658	0.0362	0.0393	0.0393
RN ↓	min_pulse_width to RN	0.0752	0.0828	0.0735	0.0735
RN ↑	recovery_rising to CP	0.0223	0.0197	0.0197	0.0197
RN ↑	removal_rising to CP	-0.0149	-0.0101	-0.0105	-0.0105
TE ↓	hold_rising to CP	-0.0552	-0.0215	-0.0215	-0.0215
TE ↑	hold_rising to CP	-0.0481	-0.0290	-0.0312	-0.0312
TE ↓	setup_rising to CP	0.0946	0.0731	0.0730	0.0730
TE ↑	setup_rising to CP	0.1809	0.1467	0.1467	0.1467
TI ↓	hold_rising to CP	-0.1488	-0.0840	-0.0840	-0.0840
TI ↑	hold_rising to CP	-0.0519	-0.0312	-0.0311	-0.0311
TI ↓	setup_rising to CP	0.1932	0.1432	0.1430	0.1430
TI ↑	setup_rising to CP	0.0832	0.0623	0.0623	0.0623

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.663e-05	5.286e-09
X8_P16	1.763e-05	4.954e-09
X17_P16	2.215e-05	5.451e-09
X33_P16	2.564e-05	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.997e-03	6.071e-03	6.118e-03	6.142e-03

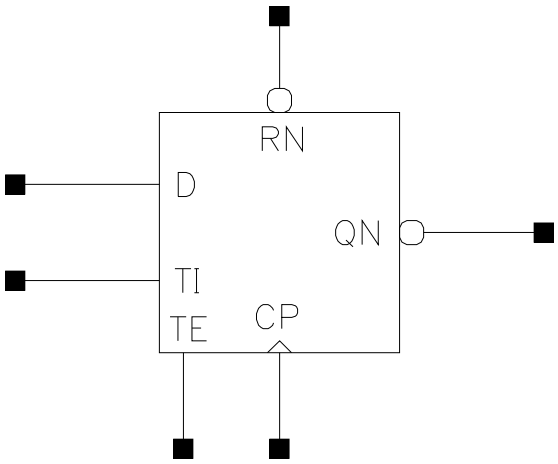
Clock 100Mhz Data 25Mhz	9.247e-03	9.205e-03	1.034e-02	1.151e-02
Clock 100Mhz Data 50Mhz	1.250e-02	1.234e-02	1.457e-02	1.687e-02
Clock = 0 Data 100Mhz	7.423e-03	6.868e-03	6.682e-03	6.589e-03
Clock = 1 Data 100Mhz	1.907e-03	1.017e-03	7.201e-04	5.719e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	3.944	4.7328
X33_P16	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0011	0.0008	0.0008	0.0008
RN	0.0010	0.0010	0.0010	0.0010
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0781	0.0725	3.4605	1.8411
CP to QN ↑	0.0873	0.0553	6.4267	3.2050
RN to QN ↑	0.0678	0.0730	6.4097	3.2128
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0724	0.0809	0.9365	0.4947
CP to QN ↑	0.0623	0.0697	1.6274	0.8333
RN to QN ↑	0.0862	0.0926	1.6272	0.8324

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1166	0.1156	0.1156	0.1156
CP ↑	min_pulse_width to CP	0.0531	0.0301	0.0349	0.0397
D ↓	hold_rising to CP	-0.0747	-0.0268	-0.0237	-0.0237
D ↑	hold_rising to CP	-0.0331	-0.0095	-0.0065	-0.0065
D ↓	setup_rising to CP	0.1193	0.0756	0.0756	0.0756
D ↑	setup_rising to CP	0.0658	0.0366	0.0362	0.0393
RN ↓	min_pulse_width to RN	0.0730	0.0735	0.0850	0.0898
RN ↑	recovery_rising to CP	0.0223	0.0219	0.0197	0.0197
RN ↑	removal_rising to CP	-0.0149	-0.0123	-0.0101	-0.0101
TE ↓	hold_rising to CP	-0.0552	-0.0215	-0.0215	-0.0215
TE ↑	hold_rising to CP	-0.0481	-0.0290	-0.0290	-0.0290
TE ↓	setup_rising to CP	0.0946	0.0731	0.0730	0.0730
TE ↑	setup_rising to CP	0.1809	0.1467	0.1467	0.1467
TI ↓	hold_rising to CP	-0.1488	-0.0840	-0.0840	-0.0840
TI ↑	hold_rising to CP	-0.0519	-0.0312	-0.0312	-0.0312
TI ↓	setup_rising to CP	0.1917	0.1437	0.1430	0.1430
TI ↑	setup_rising to CP	0.0832	0.0623	0.0623	0.0623

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.719e-05	5.347e-09
X8_P16	1.829e-05	5.120e-09
X17_P16	2.249e-05	5.286e-09
X33_P16	2.679e-05	5.617e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.947e-03	6.017e-03	6.041e-03	6.052e-03

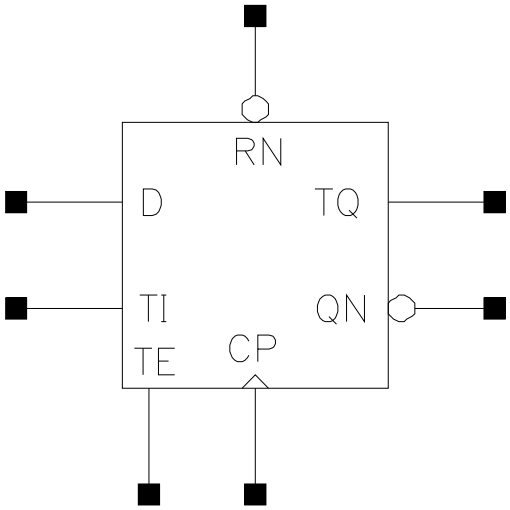
Clock 100Mhz Data 25Mhz	9.040e-03	9.179e-03	1.014e-02	1.128e-02
Clock 100Mhz Data 50Mhz	1.213e-02	1.234e-02	1.424e-02	1.652e-02
Clock = 0 Data 100Mhz	7.416e-03	6.863e-03	6.686e-03	6.597e-03
Clock = 1 Data 100Mhz	1.905e-03	9.866e-04	6.804e-04	5.274e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0011	0.0008	0.0008	0.0008

RN	0.0012	0.0009	0.0010	0.0010
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0875	0.0757	3.4632	1.9297
CP to QN ↑	0.1152	0.0628	5.7654	3.3248
CP to TQ ↓	0.0799	0.0417	4.6165	3.6716
CP to TQ ↑	0.0713	0.0586	9.7053	9.0178
RN to QN ↑	0.0796	0.0872	5.8530	3.3277
RN to TQ ↓	0.0588	0.0691	3.9389	3.5685
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0789	0.0859	0.9596	0.5065
CP to QN ↑	0.0641	0.0680	1.6585	0.8342
CP to TQ ↓	0.0437	0.0454	4.5110	4.4228
CP to TQ ↑	0.0587	0.0603	8.5008	8.6145
RN to QN ↑	0.0880	0.0908	1.6597	0.8350
RN to TQ ↓	0.0704	0.0712	4.3981	4.2987

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1166	0.1156	0.1185	0.1185
CP ↑	min_pulse_width to CP	0.0772	0.0349	0.0349	0.0349
D ↓	hold_rising to CP	-0.0747	-0.0268	-0.0237	-0.0237
D ↑	hold_rising to CP	-0.0331	-0.0065	-0.0095	-0.0095
D ↓	setup_rising to CP	0.1193	0.0756	0.0756	0.0756
D ↑	setup_rising to CP	0.0658	0.0362	0.0393	0.0393
RN ↓	min_pulse_width to RN	0.0779	0.0779	0.0828	0.0876
RN ↑	recovery_rising to CP	0.0219	0.0197	0.0197	0.0197
RN ↑	removal_rising to CP	-0.0171	-0.0101	-0.0101	-0.0101
TE ↓	hold_rising to CP	-0.0552	-0.0215	-0.0215	-0.0215
TE ↑	hold_rising to CP	-0.0481	-0.0290	-0.0290	-0.0290
TE ↓	setup_rising to CP	0.0946	0.0731	0.0731	0.0731
TE ↑	setup_rising to CP	0.1809	0.1467	0.1467	0.1467
TI ↓	hold_rising to CP	-0.1488	-0.0840	-0.0840	-0.0840
TI ↑	hold_rising to CP	-0.0519	-0.0312	-0.0312	-0.0312
TI ↓	setup_rising to CP	0.1917	0.1432	0.1430	0.1430
TI ↑	setup_rising to CP	0.0830	0.0623	0.0623	0.0623

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.802e-05	5.451e-09
X8_P16	1.921e-05	5.120e-09
X17_P16	2.219e-05	5.451e-09
X33_P16	2.721e-05	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

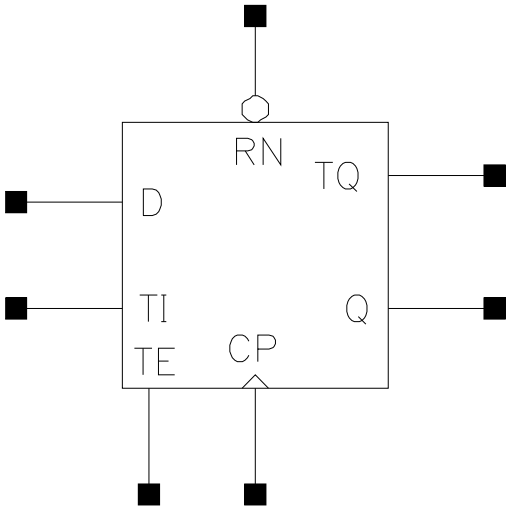
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.951e-03	6.040e-03	6.096e-03	6.125e-03
Clock 100Mhz Data 25Mhz	9.426e-03	9.453e-03	1.005e-02	1.134e-02
Clock 100Mhz Data 50Mhz	1.290e-02	1.287e-02	1.401e-02	1.655e-02
Clock = 0 Data 100Mhz	7.410e-03	6.859e-03	6.670e-03	6.576e-03
Clock = 1 Data 100Mhz	1.906e-03	1.017e-03	7.208e-04	5.728e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0011	0.0008	0.0008	0.0008

RN	0.0010	0.0010	0.0009	0.0009
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0974	0.0504	4.6571	2.0241
CP to Q ↑	0.0743	0.0611	6.8298	3.4131
CP to TQ ↓	0.0922	0.0505	5.7255	4.7895
CP to TQ ↑	0.0770	0.0643	12.8142	11.7035
RN to Q ↓	0.0650	0.0744	3.9911	1.9501
RN to TQ ↓	0.0625	0.0747	4.9816	4.6454
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0717	0.0799	0.9487	0.5016
CP to Q ↑	0.0879	0.0938	1.6235	0.8274
CP to TQ ↓	0.0745	0.0846	4.5122	4.6058
CP to TQ ↑	0.0932	0.1022	11.4968	11.5487
RN to Q ↓	0.0883	0.0967	0.9496	0.5018
RN to TQ ↓	0.0911	0.1013	4.5117	4.6058

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1185	0.1156	0.1156	0.1156
CP ↑	min_pulse_width to CP	0.0868	0.0386	0.0301	0.0301
D ↓	hold_rising to CP	-0.0747	-0.0237	-0.0268	-0.0268
D ↑	hold_rising to CP	-0.0331	-0.0065	-0.0095	-0.0095
D ↓	setup_rising to CP	0.1193	0.0756	0.0756	0.0756
D ↑	setup_rising to CP	0.0658	0.0362	0.0362	0.0362
RN ↓	min_pulse_width to RN	0.0806	0.0925	0.0735	0.0735
RN ↑	recovery_rising to CP	0.0197	0.0223	0.0197	0.0197
RN ↑	removal_rising to CP	-0.0153	-0.0101	-0.0101	-0.0101
TE ↓	hold_rising to CP	-0.0552	-0.0215	-0.0215	-0.0215
TE ↑	hold_rising to CP	-0.0481	-0.0290	-0.0290	-0.0290
TE ↓	setup_rising to CP	0.0946	0.0731	0.0731	0.0731
TE ↑	setup_rising to CP	0.1809	0.1467	0.1467	0.1467
TI ↓	hold_rising to CP	-0.1488	-0.0840	-0.0840	-0.0840
TI ↑	hold_rising to CP	-0.0519	-0.0312	-0.0312	-0.0312
TI ↓	setup_rising to CP	0.1917	0.1432	0.1432	0.1432
TI ↑	setup_rising to CP	0.0832	0.0623	0.0623	0.0623

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.742e-05	5.451e-09
X8_P16	1.835e-05	5.120e-09
X17_P16	2.268e-05	5.451e-09
X33_P16	2.618e-05	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

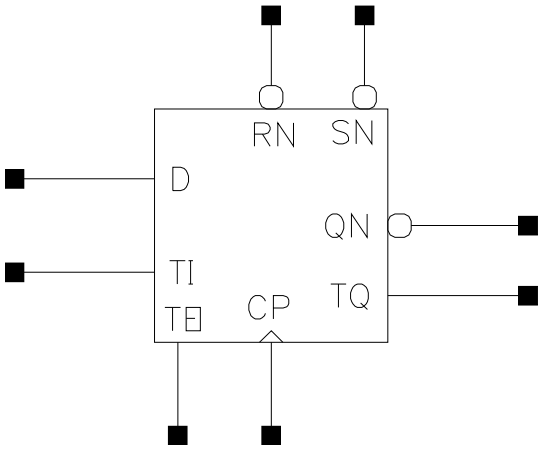
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.989e-03	6.064e-03	6.086e-03	6.098e-03
Clock 100Mhz Data 25Mhz	9.540e-03	9.445e-03	1.056e-02	1.177e-02
Clock 100Mhz Data 50Mhz	1.309e-02	1.283e-02	1.502e-02	1.745e-02
Clock = 0 Data 100Mhz	7.419e-03	6.866e-03	6.681e-03	6.589e-03
Clock = 1 Data 100Mhz	1.908e-03	9.867e-04	6.797e-04	5.263e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.352	5.2224
X17_P16	1.200	4.488	5.3856
X33_P16	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011
D	0.0007	0.0007	0.0007
RN	0.0010	0.0011	0.0011

SN	0.0015	0.0015	0.0015
TE	0.0013	0.0013	0.0013
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
CP to QN ↓	0.0833	0.0897	1.8750	0.9691
CP to QN ↑	0.0644	0.0681	3.2204	1.6275
CP to TQ ↓	0.0481	0.0480	5.6317	5.6357
CP to TQ ↑	0.0680	0.0681	14.9266	14.9411
RN to QN ↓	0.0761	0.0836	1.8848	0.9717
RN to QN ↑	0.0750	0.0782	3.2188	1.6268
RN to TQ ↓	0.0606	0.0606	5.5287	5.5299
RN to TQ ↑	0.0592	0.0591	15.0867	15.1073
SN to QN ↓	0.0842	0.0905	1.8763	0.9696
SN to TQ ↑	0.0694	0.0695	14.9177	14.9202
	X33_P16		X33_P16	
CP to QN ↓	0.1047		0.5186	
CP to QN ↑	0.0766		0.8319	
CP to TQ ↓	0.0481		5.6416	
CP to TQ ↑	0.0683		14.9648	
RN to QN ↓	0.1001		0.5191	
RN to QN ↑	0.0860		0.8320	
RN to TQ ↓	0.0606		5.5384	
RN to TQ ↑	0.0593		15.1468	
SN to QN ↓	0.1053		0.5196	
SN to TQ ↑	0.0697		14.9519	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1234	0.1234	0.1234
CP ↑	min_pulse_width to CP	0.0349	0.0349	0.0397
D ↓	hold_rising to CP	-0.0268	-0.0268	-0.0268
D ↑	hold_rising to CP	-0.0095	-0.0095	-0.0095
D ↓	setup_rising to CP	0.0830	0.0830	0.0830
D ↑	setup_rising to CP	0.0393	0.0393	0.0393
RN ↓	min_pulse_width to RN	0.0850	0.0898	0.0974
RN ↑	non_seq_hold_rising to SN	-0.0337	-0.0337	-0.0337
RN ↑	non_seq_setup_rising to SN	0.0789	0.0789	0.0789
RN ↑	recovery_rising to CP	0.0317	0.0317	0.0317
RN ↑	removal_rising to CP	-0.0171	-0.0171	-0.0201
SN ↓	min_pulse_width to SN	0.0740	0.0767	0.0793
SN ↑	recovery_rising to CP	0.0078	0.0078	0.0078
SN ↑	removal_rising to CP	0.0360	0.0360	0.0360

TE ↓	hold_rising to CP	-0.0215	-0.0215	-0.0215
TE ↑	hold_rising to CP	-0.0290	-0.0290	-0.0290
TE ↓	setup_rising to CP	0.0810	0.0810	0.0810
TE ↑	setup_rising to CP	0.1541	0.1541	0.1541
TI ↓	hold_rising to CP	-0.0840	-0.0840	-0.0840
TI ↑	hold_rising to CP	-0.0312	-0.0312	-0.0312
TI ↓	setup_rising to CP	0.1479	0.1479	0.1479
TI ↑	setup_rising to CP	0.0659	0.0659	0.0659

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	2.142e-05	5.800e-09
X17_P16	2.384e-05	5.966e-09
X33_P16	2.805e-05	6.297e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

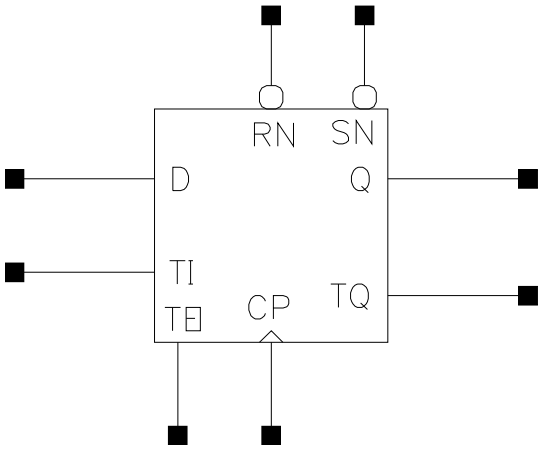
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	6.420e-03	6.420e-03	6.420e-03
Clock 100Mhz Data 25Mhz	9.855e-03	1.040e-02	1.185e-02
Clock 100Mhz Data 50Mhz	1.329e-02	1.438e-02	1.728e-02
Clock = 0 Data 100Mhz	6.526e-03	6.524e-03	6.526e-03
Clock = 1 Data 100Mhz	1.298e-04	1.297e-04	1.299e-04

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.216	5.0592
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011
D	0.0007	0.0007	0.0007
RN	0.0011	0.0011	0.0011

SN	0.0015	0.0015	0.0015
TE	0.0013	0.0013	0.0013
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0542	0.0618	1.9744	1.0279
CP to Q ↑	0.0668	0.0712	3.3044	1.6794
CP to TQ ↓	0.0557	0.0640	5.7558	5.8656
CP to TQ ↑	0.0735	0.0815	14.5280	14.6301
RN to Q ↓	0.0637	0.0682	1.8958	0.9823
RN to Q ↑	0.0712	0.0745	3.2865	1.6666
RN to TQ ↓	0.0651	0.0703	5.6072	5.6778
RN to TQ ↑	0.0774	0.0837	14.4647	14.5513
SN to Q ↑	0.0678	0.0713	3.2899	1.6681
SN to TQ ↑	0.0737	0.0803	14.4923	14.5757
	X33_P16		**X33_P16**	
CP to Q ↓	0.0806		0.5577	
CP to Q ↑	0.0827		0.8680	
CP to TQ ↓	0.0790		6.1585	
CP to TQ ↑	0.0964		14.8156	
RN to Q ↓	0.0800		0.5260	
RN to Q ↑	0.0833		0.8586	
RN to TQ ↓	0.0795		5.8719	
RN to TQ ↑	0.0950		14.7042	
SN to Q ↑	0.0805		0.8592	
SN to TQ ↑	0.0920		14.7275	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1234	0.1234	0.1234
CP ↑	min_pulse_width to CP	0.0397	0.0494	0.0687
D ↓	hold_rising to CP	-0.0268	-0.0237	-0.0237
D ↑	hold_rising to CP	-0.0095	-0.0065	-0.0065
D ↓	setup_rising to CP	0.0805	0.0830	0.0830
D ↑	setup_rising to CP	0.0393	0.0393	0.0393
RN ↓	min_pulse_width to RN	0.0996	0.1191	0.1533
RN ↑	non_seq_hold_rising to SN	-0.0385	-0.0455	-0.0601
RN ↑	non_seq_setup_rising to SN	0.0717	0.0717	0.0973
RN ↑	recovery_rising to CP	0.0268	0.0268	0.0299
RN ↑	removal_rising to CP	-0.0149	-0.0149	-0.0149
SN ↓	min_pulse_width to SN	0.0793	0.0891	0.1162
SN ↑	recovery_rising to CP	0.0078	0.0078	0.0078
SN ↑	removal_rising to CP	0.0360	0.0360	0.0360

TE ↓	hold_rising to CP	-0.0215	-0.0215	-0.0215
TE ↑	hold_rising to CP	-0.0290	-0.0290	-0.0290
TE ↓	setup_rising to CP	0.0810	0.0810	0.0810
TE ↑	setup_rising to CP	0.1516	0.1541	0.1541
TI ↓	hold_rising to CP	-0.0840	-0.0840	-0.0845
TI ↑	hold_rising to CP	-0.0312	-0.0312	-0.0312
TI ↓	setup_rising to CP	0.1479	0.1479	0.1479
TI ↑	setup_rising to CP	0.0659	0.0659	0.0659

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P16	2.079e-05	5.628e-09
X17_P16	2.289e-05	5.794e-09
X33_P16	2.663e-05	6.125e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

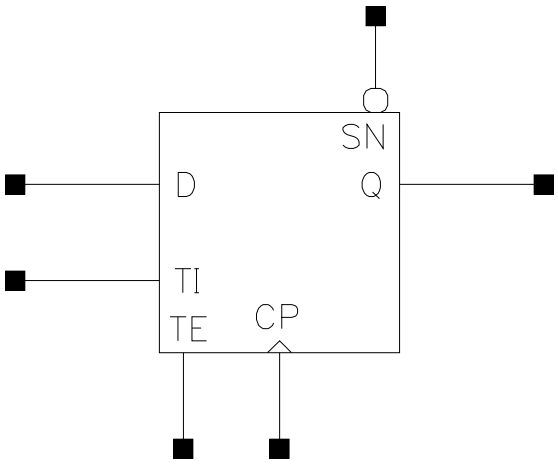
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	6.353e-03	6.354e-03	6.355e-03
Clock 100Mhz Data 25Mhz	9.721e-03	1.043e-02	1.236e-02
Clock 100Mhz Data 50Mhz	1.309e-02	1.451e-02	1.837e-02
Clock = 0 Data 100Mhz	6.522e-03	6.523e-03	6.522e-03
Clock = 1 Data 100Mhz	1.288e-04	1.291e-04	1.293e-04

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0005	0.0005	0.0005
SN	0.0017	0.0016	0.0016	0.0016
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005
	X33_P16			

CP	0.0011			
D	0.0005			
SN	0.0016			
TE	0.0012			
TI	0.0005			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0852	0.0474	4.4095	1.9568
CP to Q ↑	0.0722	0.0611	6.6415	3.2861
SN to Q ↑	0.0492	0.0515	6.4705	3.2572
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to Q ↓	0.0683	0.0725	0.9379	0.6506
CP to Q ↑	0.0874	0.0907	1.6170	1.0963
SN to Q ↑	0.0787	0.0820	1.6176	1.0960
	X33_P16		**X33_P16**	
CP to Q ↓	0.0760		0.4954	
CP to Q ↑	0.0931		0.8249	
SN to Q ↑	0.0844		0.8250	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.1214	0.1233	0.1233	0.1233
CP ↑	min_pulse_width to CP	0.0729	0.0349	0.0301	0.0301
D ↓	hold_rising to CP	-0.0771	-0.0286	-0.0316	-0.0316
D ↑	hold_rising to CP	-0.0309	-0.0044	-0.0044	-0.0044
D ↓	setup_rising to CP	0.1190	0.0830	0.0830	0.0830
D ↑	setup_rising to CP	0.0609	0.0313	0.0313	0.0313
SN ↓	min_pulse_width to SN	0.0522	0.0593	0.0544	0.0544
SN ↑	recovery_rising to CP	0.0078	0.0078	0.0078	0.0078
SN ↑	removal_rising to CP	0.0263	0.0361	0.0361	0.0361
TE ↓	hold_rising to CP	-0.0496	-0.0264	-0.0264	-0.0264
TE ↑	hold_rising to CP	-0.0432	-0.0241	-0.0238	-0.0238
TE ↓	setup_rising to CP	0.0995	0.0810	0.0806	0.0806
TE ↑	setup_rising to CP	0.1858	0.1565	0.1565	0.1565
TI ↓	hold_rising to CP	-0.1486	-0.0887	-0.0902	-0.0902
TI ↑	hold_rising to CP	-0.0485	-0.0262	-0.0262	-0.0262
TI ↓	setup_rising to CP	0.1930	0.1534	0.1534	0.1534
TI ↑	setup_rising to CP	0.0782	0.0561	0.0561	0.0561
		X33_P16			

CP ↓	min_pulse_width to CP	0.1233			
CP ↑	min_pulse_width to CP	0.0301			
D ↓	hold_rising to CP	-0.0316			
D ↑	hold_rising to CP	-0.0044			
D ↓	setup_rising to CP	0.0830			
D ↑	setup_rising to CP	0.0313			
SN ↓	min_pulse_width to SN	0.0544			
SN ↑	recovery_rising to CP	0.0078			
SN ↑	removal_rising to CP	0.0361			
TE ↓	hold_rising to CP	-0.0264			
TE ↑	hold_rising to CP	-0.0238			
TE ↓	setup_rising to CP	0.0806			
TE ↑	setup_rising to CP	0.1565			
TI ↓	hold_rising to CP	-0.0902			
TI ↑	hold_rising to CP	-0.0262			
TI ↓	setup_rising to CP	0.1534			
TI ↑	setup_rising to CP	0.0561			

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.746e-05	5.286e-09
X8_P16	1.868e-05	5.120e-09
X17_P16	2.294e-05	5.451e-09
X25_P16	2.510e-05	5.617e-09
X33_P16	2.724e-05	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	5.839e-03	6.003e-03	6.056e-03	6.083e-03
Clock 100Mhz Data 25Mhz	9.056e-03	9.213e-03	1.027e-02	1.087e-02
Clock 100Mhz Data 50Mhz	1.227e-02	1.242e-02	1.448e-02	1.566e-02
Clock = 0 Data 100Mhz	7.137e-03	6.747e-03	6.618e-03	6.553e-03
Clock = 1 Data 100Mhz	1.907e-03	9.872e-04	6.806e-04	5.273e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	6.100e-03			

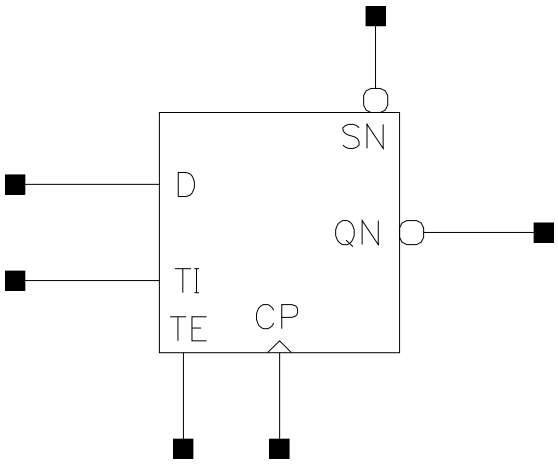
Clock 100Mhz Data 25Mhz	1.142e-02			
Clock 100Mhz Data 50Mhz	1.675e-02			
Clock = 0 Data 100Mhz	6.514e-03			
Clock = 1 Data 100Mhz	4.354e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0005	0.0005	0.0005
SN	0.0017	0.0016	0.0017	0.0017
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005
	X33_P16			

CP	0.0011			
D	0.0005			
SN	0.0016			
TE	0.0012			
TI	0.0005			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0814	0.0733	3.4620	1.8407
CP to QN ↑	0.0874	0.0548	6.4206	3.2200
SN to QN ↓	0.0603	0.0645	3.4542	1.8422
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to QN ↓	0.0771	0.0820	0.9413	0.6526
CP to QN ↑	0.0656	0.0699	1.6202	1.0965
SN to QN ↓	0.0663	0.0708	0.9391	0.6512
	X33_P16		**X33_P16**	
CP to QN ↓	0.0861		0.4969	
CP to QN ↑	0.0731		0.8266	
SN to QN ↓	0.0746		0.4964	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.1214	0.1233	0.1233	0.1239
CP ↑	min_pulse_width to CP	0.0531	0.0301	0.0349	0.0386
D ↓	hold_rising to CP	-0.0771	-0.0316	-0.0286	-0.0286
D ↑	hold_rising to CP	-0.0309	-0.0044	-0.0044	-0.0044
D ↓	setup_rising to CP	0.1190	0.0830	0.0830	0.0830
D ↑	setup_rising to CP	0.0609	0.0313	0.0313	0.0313
SN ↓	min_pulse_width to SN	0.0496	0.0544	0.0620	0.0620
SN ↑	recovery_rising to CP	0.0078	0.0078	0.0078	0.0078
SN ↑	removal_rising to CP	0.0263	0.0361	0.0361	0.0361
TE ↓	hold_rising to CP	-0.0496	-0.0264	-0.0264	-0.0264
TE ↑	hold_rising to CP	-0.0432	-0.0238	-0.0241	-0.0241
TE ↓	setup_rising to CP	0.0998	0.0806	0.0806	0.0806
TE ↑	setup_rising to CP	0.1858	0.1565	0.1565	0.1565
TI ↓	hold_rising to CP	-0.1486	-0.0902	-0.0887	-0.0887
TI ↑	hold_rising to CP	-0.0485	-0.0262	-0.0264	-0.0264
TI ↓	setup_rising to CP	0.1931	0.1534	0.1534	0.1534
TI ↑	setup_rising to CP	0.0782	0.0561	0.0561	0.0561
		X33_P16			

CP ↓	min_pulse_width to CP	0.1239			
CP ↑	min_pulse_width to CP	0.0397			
D ↓	hold_rising to CP	-0.0286			
D ↑	hold_rising to CP	-0.0044			
D ↓	setup_rising to CP	0.0830			
D ↑	setup_rising to CP	0.0313			
SN ↓	min_pulse_width to SN	0.0620			
SN ↑	recovery_rising to CP	0.0078			
SN ↑	removal_rising to CP	0.0361			
TE ↓	hold_rising to CP	-0.0264			
TE ↑	hold_rising to CP	-0.0241			
TE ↓	setup_rising to CP	0.0806			
TE ↑	setup_rising to CP	0.1565			
TI ↓	hold_rising to CP	-0.0887			
TI ↑	hold_rising to CP	-0.0264			
TI ↓	setup_rising to CP	0.1534			
TI ↑	setup_rising to CP	0.0561			

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.707e-05	5.286e-09
X8_P16	1.798e-05	5.120e-09
X17_P16	2.238e-05	5.451e-09
X25_P16	2.412e-05	5.617e-09
X33_P16	2.588e-05	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	5.835e-03	5.989e-03	6.035e-03	6.058e-03
Clock 100Mhz Data 25Mhz	8.858e-03	9.131e-03	1.030e-02	1.090e-02
Clock 100Mhz Data 50Mhz	1.188e-02	1.227e-02	1.456e-02	1.574e-02
Clock = 0 Data 100Mhz	7.137e-03	6.752e-03	6.619e-03	6.554e-03
Clock = 1 Data 100Mhz	1.907e-03	1.007e-03	7.067e-04	5.568e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	6.072e-03			

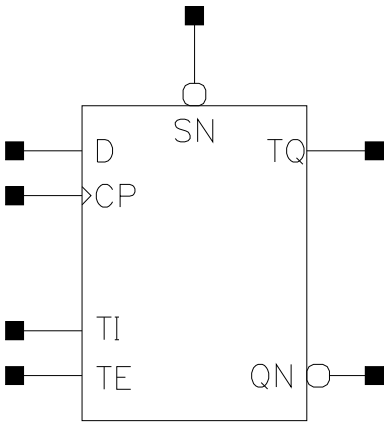
Clock 100Mhz Data 25Mhz	1.148e-02			
Clock 100Mhz Data 50Mhz	1.688e-02			
Clock = 0 Data 100Mhz	6.515e-03			
Clock = 1 Data 100Mhz	4.667e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.216	5.0592
X8_P16	1.200	4.080	4.8960
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0005	0.0005	0.0005

SN	0.0018	0.0019	0.0018	0.0018
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0935	0.0771	3.4576	1.8478
CP to QN ↑	0.1145	0.0626	6.3217	3.2703
CP to TQ ↓	0.0818	0.0421	5.1784	4.2111
CP to TQ ↑	0.0719	0.0574	8.6609	8.4514
SN to QN ↓	0.0593	0.0665	3.4635	1.8477
SN to TQ ↑	0.0418	0.0463	8.4922	8.4748
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0776	0.0867	0.9620	0.4919
CP to QN ↑	0.0710	0.0791	1.6270	0.8281
CP to TQ ↓	0.0527	0.0526	4.4266	4.4251
CP to TQ ↑	0.0648	0.0649	8.5243	8.5442
SN to QN ↓	0.0597	0.0679	0.9606	0.4916
SN to TQ ↑	0.0481	0.0482	8.4428	8.4655

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1214	0.1233	0.1239	0.1239
CP ↑	min_pulse_width to CP	0.0772	0.0338	0.0397	0.0434
D ↓	hold_rising to CP	-0.0771	-0.0286	-0.0286	-0.0286
D ↑	hold_rising to CP	-0.0309	-0.0044	-0.0047	-0.0047
D ↓	setup_rising to CP	0.1190	0.0830	0.0830	0.0830
D ↑	setup_rising to CP	0.0609	0.0313	0.0313	0.0313
SN ↓	min_pulse_width to SN	0.0447	0.0496	0.0522	0.0522
SN ↑	recovery_rising to CP	0.0078	0.0078	0.0078	0.0078
SN ↑	removal_rising to CP	0.0263	0.0361	0.0361	0.0361
TE ↓	hold_rising to CP	-0.0496	-0.0264	-0.0264	-0.0264
TE ↑	hold_rising to CP	-0.0432	-0.0241	-0.0241	-0.0241
TE ↓	setup_rising to CP	0.0995	0.0806	0.0806	0.0806
TE ↑	setup_rising to CP	0.1858	0.1565	0.1565	0.1565
TI ↓	hold_rising to CP	-0.1486	-0.0902	-0.0887	-0.0887
TI ↑	hold_rising to CP	-0.0485	-0.0262	-0.0264	-0.0264
TI ↓	setup_rising to CP	0.1930	0.1534	0.1534	0.1534
TI ↑	setup_rising to CP	0.0782	0.0561	0.0561	0.0561

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.856e-05	5.617e-09
X8_P16	1.947e-05	5.451e-09
X17_P16	2.387e-05	5.782e-09
X33_P16	2.736e-05	6.114e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

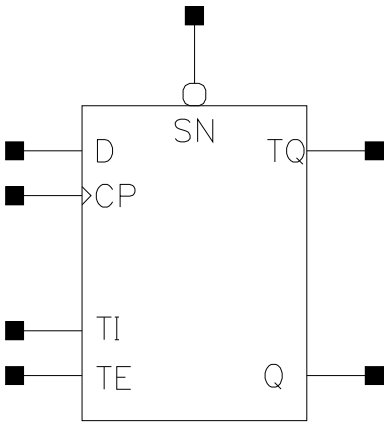
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.840e-03	6.008e-03	6.065e-03	6.094e-03
Clock 100Mhz Data 25Mhz	9.363e-03	9.489e-03	1.057e-02	1.174e-02
Clock 100Mhz Data 50Mhz	1.289e-02	1.297e-02	1.508e-02	1.739e-02
Clock = 0 Data 100Mhz	7.151e-03	6.760e-03	6.629e-03	6.564e-03
Clock = 1 Data 100Mhz	1.908e-03	9.866e-04	6.796e-04	5.262e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.944	4.7328
X17_P16	1.200	4.216	5.0592
X33_P16	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0005	0.0005	0.0005

SN	0.0018	0.0016	0.0016	0.0016
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0992	0.0513	4.5561	2.0021
CP to Q ↑	0.0774	0.0637	6.6927	3.3248
CP to TQ ↓	0.0999	0.0530	6.3988	4.8132
CP to TQ ↑	0.0763	0.0697	8.7246	11.8055
SN to Q ↑	0.0442	0.0533	6.4838	3.2920
SN to TQ ↑	0.0433	0.0581	8.5174	11.7464
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0701	0.0779	0.9616	0.5044
CP to Q ↑	0.0889	0.0945	1.6235	0.8280
CP to TQ ↓	0.0729	0.0825	4.5110	4.5947
CP to TQ ↑	0.0944	0.1027	11.5040	11.5678
SN to Q ↑	0.0801	0.0858	1.6245	0.8283
SN to TQ ↑	0.0856	0.0940	11.5026	11.5686

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1209	0.1233	0.1233	0.1233
CP ↑	min_pulse_width to CP	0.0879	0.0386	0.0301	0.0301
D ↓	hold_rising to CP	-0.0771	-0.0286	-0.0316	-0.0316
D ↑	hold_rising to CP	-0.0309	-0.0044	-0.0044	-0.0044
D ↓	setup_rising to CP	0.1190	0.0830	0.0830	0.0830
D ↑	setup_rising to CP	0.0609	0.0313	0.0313	0.0313
SN ↓	min_pulse_width to SN	0.0447	0.0620	0.0544	0.0544
SN ↑	recovery_rising to CP	0.0078	0.0078	0.0078	0.0078
SN ↑	removal_rising to CP	0.0263	0.0361	0.0361	0.0361
TE ↓	hold_rising to CP	-0.0496	-0.0264	-0.0264	-0.0264
TE ↑	hold_rising to CP	-0.0432	-0.0241	-0.0238	-0.0238
TE ↓	setup_rising to CP	0.0995	0.0810	0.0806	0.0810
TE ↑	setup_rising to CP	0.1858	0.1565	0.1565	0.1565
TI ↓	hold_rising to CP	-0.1486	-0.0889	-0.0902	-0.0902
TI ↑	hold_rising to CP	-0.0485	-0.0264	-0.0262	-0.0262
TI ↓	setup_rising to CP	0.1930	0.1534	0.1534	0.1534
TI ↑	setup_rising to CP	0.0782	0.0561	0.0561	0.0561

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.842e-05	5.451e-09
X8_P16	1.969e-05	5.286e-09
X17_P16	2.388e-05	5.617e-09
X33_P16	2.816e-05	5.948e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

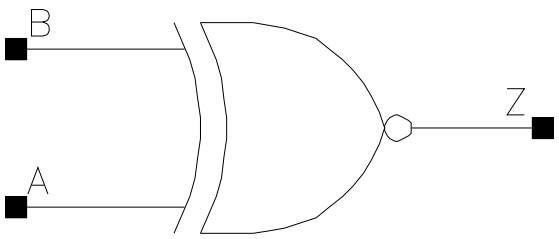
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	5.841e-03	6.009e-03	6.064e-03	6.091e-03
Clock 100Mhz Data 25Mhz	9.433e-03	9.504e-03	1.056e-02	1.176e-02
Clock 100Mhz Data 50Mhz	1.302e-02	1.300e-02	1.506e-02	1.743e-02
Clock = 0 Data 100Mhz	7.151e-03	6.754e-03	6.622e-03	6.556e-03
Clock = 1 Data 100Mhz	1.908e-03	9.866e-04	6.797e-04	5.263e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P16	X8_P16	X17_P16	X25_P16
A	0.0020	0.0008	0.0011	0.0018
B	0.0018	0.0017	0.0021	0.0030
	X33_P16			
A	0.0021			
B	0.0035			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X8_P16**	**X6_P16**	**X8_P16**
A to Z ↓	0.0218	0.0491	3.2711	2.0119
A to Z ↑	0.0234	0.0451	4.9440	3.3886
B to Z ↓	0.0202	0.0341	3.2659	1.9904
B to Z ↑	0.0236	0.0328	4.9554	3.3779
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
A to Z ↓	0.0477	0.0480	0.9917	0.6803
A to Z ↑	0.0421	0.0424	1.6624	1.1045

B to Z ↓	0.0354	0.0343	0.9867	0.6775
B to Z ↑	0.0333	0.0322	1.6601	1.1033
	X33_P16		**X33_P16**	
A to Z ↓	0.0459		0.5098	
A to Z ↑	0.0413		0.8307	
B to Z ↓	0.0332		0.5083	
B to Z ↑	0.0320		0.8287	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P16	7.035e-06	1.642e-09
X8_P16	8.904e-06	2.139e-09
X17_P16	1.334e-05	2.304e-09
X25_P16	2.142e-05	3.298e-09
X33_P16	2.696e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	3.711e-03	6.911e-03	1.019e-02	1.625e-02
B to Z	3.504e-03	4.858e-03	7.810e-03	1.216e-02
	X33_P16			
A to Z	2.002e-02			
B to Z	1.548e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

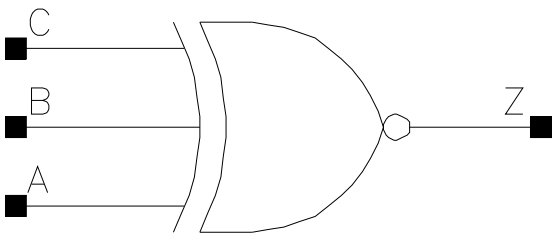
Pin Cycle (vdds)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	-6.361e-07	4.105e-08	-5.314e-08	5.430e-08
B to Z	1.162e-05	3.401e-07	3.422e-07	1.113e-06
	X33_P16			
A to Z	-1.128e-07			
B to Z	3.878e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	2.176	2.6112
X16_P16	1.200	2.720	3.2640
X25_P16	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X16_P16	X25_P16
A	0.0035	0.0029	0.0036	0.0053
B	0.0037	0.0026	0.0035	0.0048
C	0.0024	0.0008	0.0008	0.0009

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0353	0.0601	3.8806	2.1245
A to Z ↑	0.0343	0.0545	6.9639	3.3586
B to Z ↓	0.0361	0.0603	3.8844	2.1253
B to Z ↑	0.0346	0.0547	6.9576	3.3589
C to Z ↓	0.0354	0.0801	3.8849	2.1239
C to Z ↑	0.0334	0.0738	6.9611	3.3589
	X16_P16	**X25_P16**	**X16_P16**	**X25_P16**
A to Z ↓	0.0606	0.0607	1.0905	0.6969
A to Z ↑	0.0590	0.0591	1.7583	1.1091
B to Z ↓	0.0611	0.0619	1.0905	0.6966

B to Z ↑	0.0593	0.0603	1.7588	1.1090
C to Z ↓	0.0853	0.0910	1.0902	0.6962
C to Z ↑	0.0826	0.0888	1.7589	1.1093

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.013e-05	2.967e-09
X8_P16	1.031e-05	3.132e-09
X16_P16	1.571e-05	3.795e-09
X25_P16	2.255e-05	5.286e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	4.190e-03	5.637e-03	9.288e-03	1.405e-02
B to Z	3.901e-03	5.493e-03	9.122e-03	1.387e-02
C to Z	3.807e-03	8.393e-03	1.269e-02	1.913e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

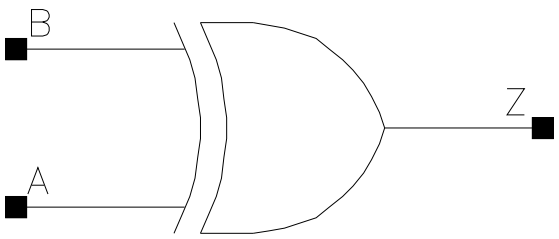
Pin Cycle (vdds)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	-2.171e-05	-6.965e-06	-9.041e-06	-1.459e-05
B to Z	2.834e-05	7.180e-06	1.526e-05	2.540e-05
C to Z	3.530e-05	1.759e-05	2.686e-05	3.640e-05

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.224	1.4688
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.224	1.4688
X16_P16	1.200	1.360	1.6320
X25_P16	1.200	2.176	2.6112
X31_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X16_P16
A	0.0009	0.0019	0.0012	0.0013
B	0.0014	0.0017	0.0018	0.0020
	X25_P16	X31_P16		
A	0.0018	0.0023		
B	0.0031	0.0040		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0445	0.0223	3.5482	2.5639
A to Z ↑	0.0422	0.0246	6.2718	6.2066
B to Z ↓	0.0319	0.0227	3.5186	2.5837
B to Z ↑	0.0321	0.0228	6.2651	6.2032
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0405	0.0429	1.9602	1.0157

A to Z ↑	0.0371	0.0395	3.3083	1.6675
B to Z ↓	0.0310	0.0328	1.9493	1.0114
B to Z ↑	0.0297	0.0320	3.3049	1.6663
	X25_P16	**X31_P16**	**X25_P16**	**X31_P16**
A to Z ↓	0.0451	0.0430	0.6745	0.5404
A to Z ↑	0.0415	0.0399	1.1031	0.8880
B to Z ↓	0.0333	0.0317	0.6738	0.5400
B to Z ↑	0.0315	0.0304	1.1031	0.8877

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	7.479e-06	1.973e-09
X6_P16	7.285e-06	1.642e-09
X8_P16	1.069e-05	1.973e-09
X16_P16	1.436e-05	2.139e-09
X25_P16	2.098e-05	3.132e-09
X31_P16	2.623e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	5.224e-03	3.721e-03	6.475e-03	9.621e-03
B to Z	4.005e-03	3.456e-03	5.276e-03	7.971e-03
	X25_P16	X31_P16		
A to Z	1.494e-02	1.848e-02		
B to Z	1.086e-02	1.344e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

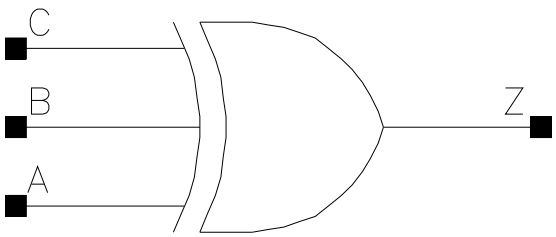
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	-2.299e-07	-1.512e-06	1.672e-08	5.820e-08
B to Z	1.399e-07	1.115e-05	9.445e-08	3.527e-07
	X25_P16	X31_P16		
A to Z	-1.235e-07	-4.964e-07		
B to Z	4.935e-07	4.083e-07		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X24_P16	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X24_P16
A	0.0030	0.0029	0.0036	0.0063
B	0.0030	0.0026	0.0033	0.0053
C	0.0009	0.0019	0.0027	0.0041

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0356	0.0600	4.0898	2.1242
A to Z ↑	0.0344	0.0545	7.6033	3.3538
B to Z ↓	0.0358	0.0603	4.0935	2.1239
B to Z ↑	0.0348	0.0547	7.5965	3.3570
C to Z ↓	0.0619	0.0588	4.0775	2.1238
C to Z ↑	0.0609	0.0531	7.5801	3.3554
	X17_P16	**X24_P16**	**X17_P16**	**X24_P16**
A to Z ↓	0.0558	0.0649	1.0129	0.7330
A to Z ↑	0.0545	0.0490	1.6375	1.1106
B to Z ↓	0.0561	0.0654	1.0126	0.7324

B to Z ↑	0.0546	0.0491	1.6383	1.1107
C to Z ↓	0.0553	0.0634	1.0130	0.7319
C to Z ↑	0.0539	0.0484	1.6379	1.1116

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P16	1.110e-05	2.967e-09
X8_P16	8.912e-06	2.801e-09
X17_P16	1.425e-05	2.967e-09
X24_P16	2.491e-05	5.120e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	3.846e-03	5.658e-03	9.010e-03	1.531e-02
B to Z	3.734e-03	5.471e-03	8.751e-03	1.481e-02
C to Z	7.632e-03	5.326e-03	8.670e-03	1.451e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	-9.236e-06	-8.877e-06	-1.227e-05	-3.558e-05
B to Z	1.305e-05	1.067e-05	2.006e-05	2.186e-05
C to Z	3.095e-05	1.683e-05	2.904e-05	6.287e-05

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