C28SOI_SC_12_PR_LR

Release Notes and Known Problems and Solutions

12 track Standard Cell Library comprising Place and Route cells

1 Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library name	C28SOI_SC_12_PR_LR
Library version	5.3.a
Library type	Standard Cells
Technology	CMOS028_FDSOI

1.2 Related Documentation

- StandardCell_Notes.pdf Present in Design Package
- User Manual C28SOI_SC_12_PR_LR_um.pdf present in doc directory of Product itself.
- Capacitance Value Decap_Info.csv present in doc directory of Product itself.

2 Release Details

2.1 Current Release Details, Version 5.3.a

- Below cells have been updated for Robustness relative to contact punch through effect.. There is no change in Cell Area and Abstract because of contact robustness update.
  - Updated cells are -
    - C12T28SOI_LR_DECAPXT4
    - C12T28SOI_LR_DECAPXT8
    - C12T28SOI_LR_DECAPXT16
- The product remains aligned to DP28FDSOI 2.5 specifications.

2.2 Version 5.3

- Previously the PC was cut asymmetric due to which some cells of this library were producing DRC errors with other cells in some configurations. Now this has been corrected in this release. PC on Boundary has been now cut symmetric to NW (45nm both sides) keeping PC to PC space of 90 nm. To support this PC cut, mos sizes have been altered too but all these moses are dummy mos. There is no change in Area or Abstract or characterized data for any Cell. Only change is in PC and RX layers for corrected cells.
  - Corrected cells are 6 cells as below -
    - C12T28SOI_LR_FILLERPFOP16
    - C12T28SOI_LR_FILLERPFOP2
    - C12T28SOI_LR_FILLERPFOP32
    - C12T28SOI_LR_FILLERPFOP4
    - C12T28SOI_LR_FILLERPFOP64
    - C12T28SOI_LR_FILLERPFOP8
- For Below cells RVT layer was missing in Previous release, so these cells have been updated.
  - C12T28SOI_LREGLV_DECAPXT12
  - C12T28SOI_LREGLV_DECAPXT16
  - C12T28SOI_LREGLV_DECAPXT32
  - C12T28SOI_LREGLV_DECAPXT64
  - C12T28SOI_LREGLV_DECAPXT9
- The product remains aligned to DP28FDSOI 2.5.

2.3 Version 5.2

- In previous Library release, there was an issue with PCEND cells, Poly Shape got extended at left and right side of cells boundary, which can create shorts in P&R. Now in this release, this issue has been corrected. Below cells have been updated for the same -

C12T28SOI_RVTFILLERPCENDB1	C12T28SOI_RVTFILLERPCENDB16
C12T28SOI_RVTFILLERPCENDB2	C12T28SOI_RVTFILLERPCENDB32
C12T28SOI_RVTFILLERPCENDB4	C12T28SOI_RVTFILLERPCENDB64

C12T28SOI_RVTFILLERPCENDB8	C12T28SOI_RVTFILLERPCENDBL1
C12T28SOI_RVTFILLERPCENDBR1	C12T28SOI_RVTFILLERPCENDT1
C12T28SOI_RVTFILLERPCENDT16	C12T28SOI_RVTFILLERPCENDT2
C12T28SOI_RVTFILLERPCENDT32	C12T28SOI_RVTFILLERPCENDT4
C12T28SOI_RVTFILLERPCENDT64	C12T28SOI_RVTFILLERPCENDT8
C12T28SOI_RVTFILLERPCENDTB1	C12T28SOI_RVTFILLERPCENDTB16
C12T28SOI_RVTFILLERPCENDTB2	C12T28SOI_RVTFILLERPCENDTB32
C12T28SOI_RVTFILLERPCENDTB4	C12T28SOI_RVTFILLERPCENDTB64
C12T28SOI_RVTFILLERPCENDTB8	C12T28SOI_RVTFILLERPCENDTBL1
C12T28SOI_RVTFILLERPCENDTBR1	C12T28SOI_RVTFILLERPCENDTL1
C12T28SOI_RVTFILLERPCENDTR1	

- There is no change in characterized data timing/power/leakage with respect to previous version.
- The product remains aligned to DP28FDSOI 2.5.

2.4 Version 5.1

- Dummy Poly in layout across various cells has been cut for DFM robustness.
- Below cells have been updated to fix SRD violations related to HYBRID.Details are as below -

Cells	Change in Abstract	Change in Diode Sizes
C12T28SOI_LR_ANTPROT3	No	Yes
C12T28SOI_LR_ANTPROT4	No	Yes
C12T28SOI_LR_ANTPROTGVFILLERSNPW8	Yes	Yes
C12T28SOI_LR_FILLERNPW4	Yes	No
C12T28SOI_LR_FILLERSNPW4	Yes	No

- Below cell have been updated for Robustness relative to contact punch through effect. Minimum Enclosure of 20nm for RX/CA has been ensured.There is no change in Cell Area and Abstract because of contact robustness update.
  - Updated cells are -
    - C12T28SOI_LR_DECAPXT4
    - C12T28SOI_LREGLV_DECAPXT12
    - C12T28SOI_LREGLV_DECAPXT16
    - C12T28SOI_LREGLV_DECAPXT32
    - C12T28SOI_LREGLV_DECAPXT64
    - C12T28SOI_LREGLV_DECAPXT9
- To enable support for Cadence Voltus Flow, CCS-Power has been added.
- Cells has been characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.
- The product has been aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Global Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.5 Version 4.0

- TIE High/Low cells have been added :
  - C12T28SOI_LR_TOHX8
  - C12T28SOI_LR_TOLX8
- Split Filler Cells with Antenna Diode has been added:
  - C12T28SOI_LR_ANTPROTGVFILLERSNPW8
- The product is aligned to DP28FDSOI 2.4 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.6 Version 4.0

- Cells have been updated to have better design manufacturability without any change in Abstract and Area.
- The product is aligned to DP28FDSOI 2.3 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.7 Version 2.0

- The Product is aligned to DP28FDSOI_7ML 1.0. Refer to Design Package Documents for more details.
- For Standard Cell Library Specific Features, Refer to StandardCell_Notes.pdf Present in Design Package.

3 Known Problems and Solutions

3.1 DP related Generic Problems

■ For Generic Standard cell Library related problem for this DP, please refer to KPS section inside StandardCell_Notes.pdf Present in Design Package.

3.2 Dont_use and dont_touch cells

➥ Specific attributes dont_use and dont_touch in Synopsys Technology File

☞ The “dont_touch” and “dont_use” attributes are defined in the Synopsys Technology Files for few cells. Reason can be -

a) Cell has some specific custom feature. Therefore We want to ensure that Either these cells are not automatically picked during Synthesis unless the designer wishes to specically use them in the design or those are not replaced during Design Optimization.

b) Cell’s functionality is not properly understood by tools.

Cells with such attributes are as following:

– C12T28SOI_LR_ANTPROT3

– C12T28SOI_LR_ANTPROT4

3.3 C12T28SOI_LR_ANTPROT3 is not Standalone DRC clean.

■ C12T28SOI_LR_ANTPROT3 is not standalone DRC clean, had to keep other cell on surroundings. To overcome this issue, there is another ANTPROT cell “C12T28SOI_LR_ANTPROT4” which is standalone DRC clean for fully isolated Designs

3.4 FILLERFLPCHKAE* cells have intentional DRC error.

■ FILLERFLPCHKAE* cells have intentional DRC error : DRC : GR11

– This is to ensure detection & Removal of these cells during final floor plan.

4 Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.

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