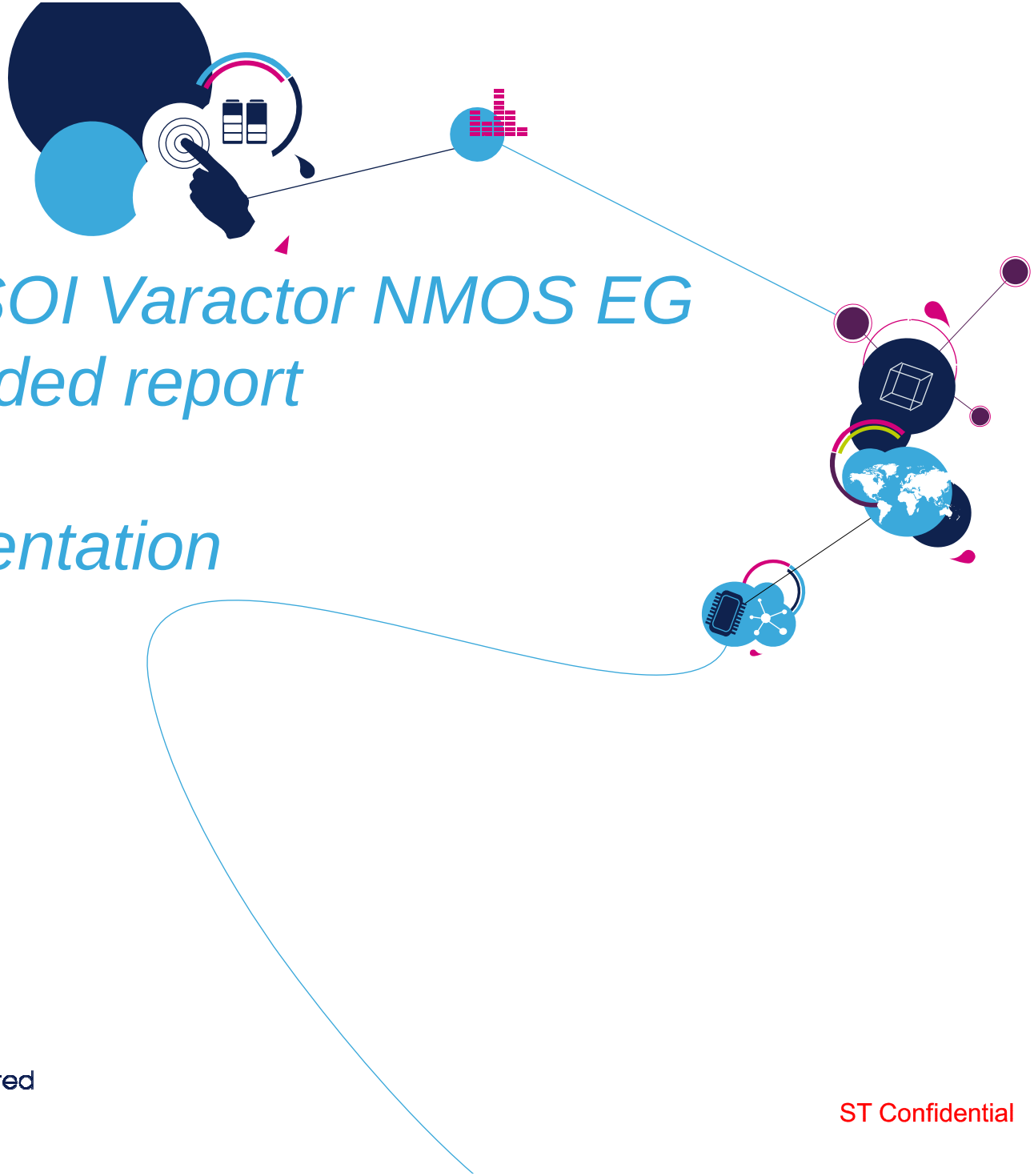


CMOS 28FDSOI Varactor NMOS EG single, diff. ended report

Model documentation

Florence SONNERAT
Cédric DURAND

October 2nd, 2017

life.augmented

Outline

- Devices presentation
- Varactor EG NMOS Single Ended (SE) Cross Section & Layout
- Varactor EG NMOS SE model performances
- Varactor EG NMOS diff. Cross Section & Layout
- Varactor EG NMOS diff. model performances
- Conclusion

Devices presentation

- Devices name and maturity:
  - Varactor single ended EG: cvar_eg, MAT. 30.
  - Varactor differential ended EG: cvar_eg_diff, MAT. 30.

- Silicon characteristics and measurements details:
  - De-embedding technique: PAD-THRU.
  - Single :
    - MPW C281608, Lot Q618020, wafer 8, die 71.
    - Measurements setup: 2 ports S parameters 100 MHz up to 110 GHz.
    - 3 temperatures have been measured : -40 °C, 25 °C and 125°C.
  - Diff
    - MPW C281348, Lot Q511109, wafer 13, die 60.
    - Measurements setup: 4 ports S parameters 100 MHz up to 67 GHz.
    - No temperature measurements available : coefficients will be inherited from the single model.

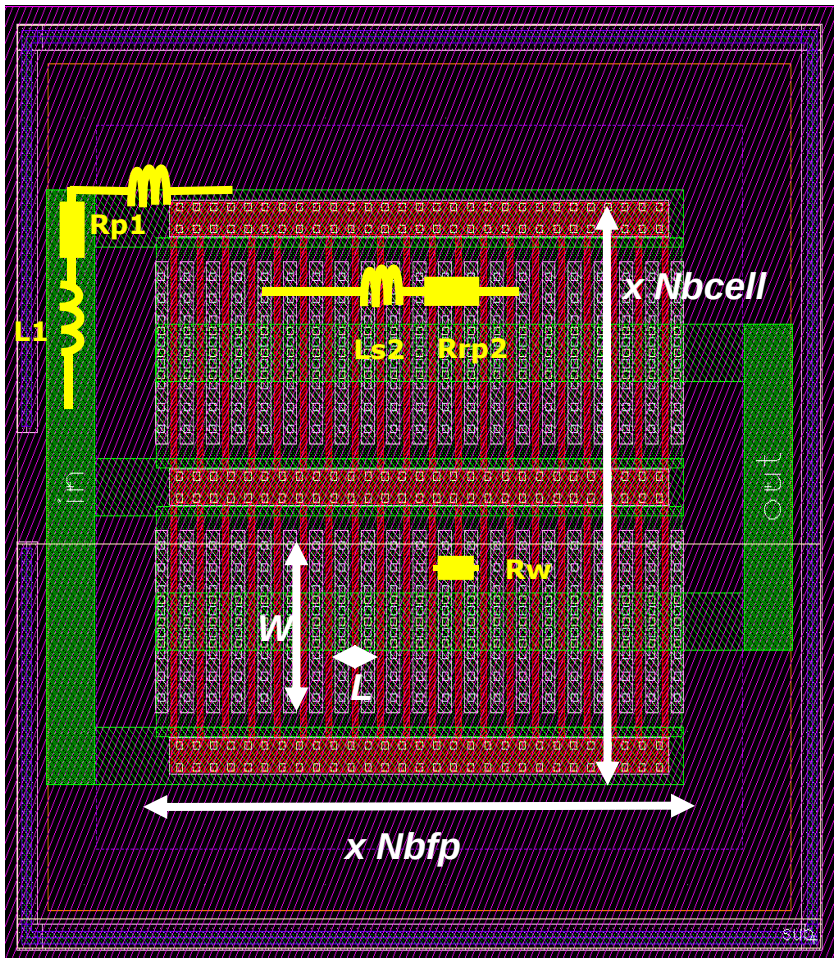
Devices presentation

Varactor MOS EG	Simulation with temperature	Worst case & Min/max	Pcell available	Model Si-based
Cvar_eg	Yes	Yes	Yes	Yes, up to 110 GHz
Cvar_eg_diff	Yes	Yes	Yes	Yes, up to 67 GHz

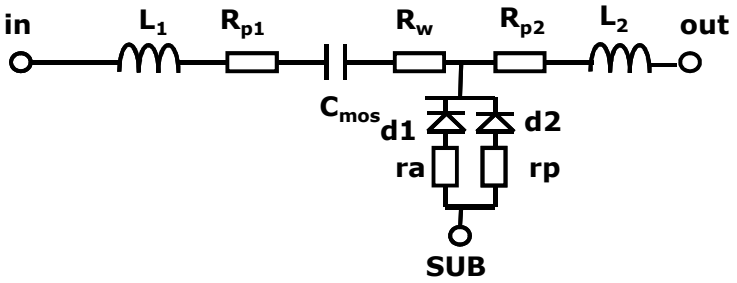
- Best/worst case
  - Statistical and Best/Worst case simulations are available
  - The criteria is the capacitance. Best/Worst are constructed with DRM value and mapping on one wafer. So statistical simulations concern mainly observed variations on intrinsic serial capacitance and back-end variation extracted from DRM

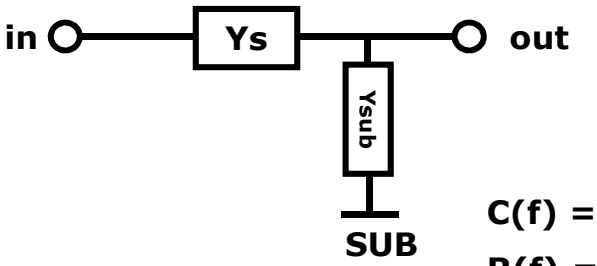
Varactor NMOS EG SE layout

Layout varactor NMOS Single Ended



Equivalent circuit





$C(f) = [-imag(1/Ys)]/(2\pi f)$

$R(f) = real(1/Ys)$

$Q(f) = imag(Ys)/real(Ys)$

Varactor NMOS EG SE parameters

- Varactor NMOS EG single in CMOS 28FDSOI

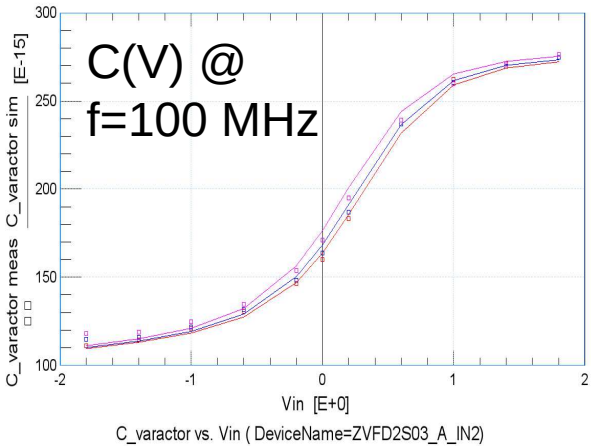
Varactor MOS **Cvar_eg**	**Cap. (F)**	**Gate Length (µm)**	**Gate Width (µm)**	**Nbfp**	**Ncell**	**Bias (V)**	**TR**	**Worst Case & Min/max**
Min	20 f	0.048	1	1	1	-1.8	1.5	Yes
Max	10 p	2	10	50	10	1.8	3	

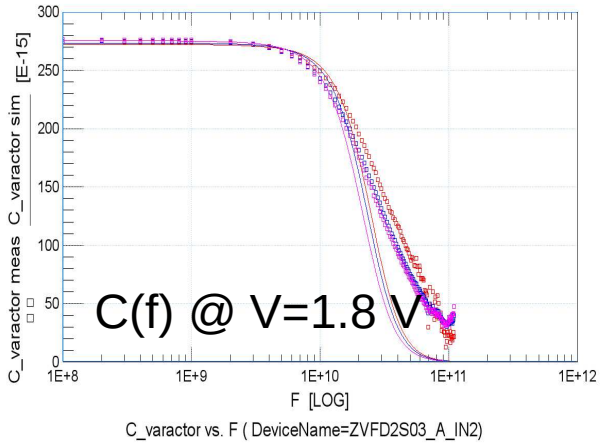
- Model maturity vs DK
  - Tentative: DK < 2.5
  - Preliminary: 2.5 < DK 2.8
  - Prod: since DK 0.9_RF_mmW

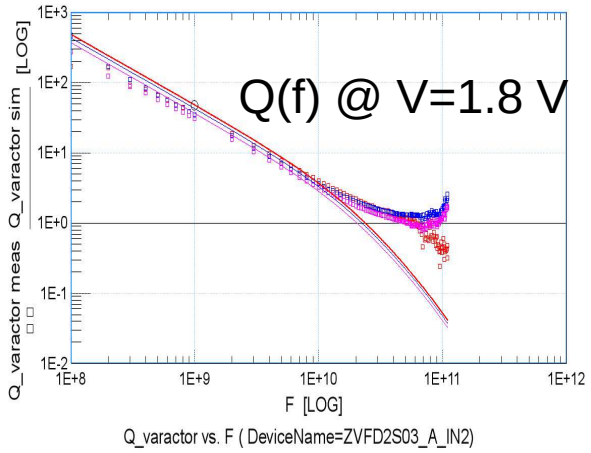
SE Varactor measured and simulated performances

▬ model □□ meas | **-40 °C 25°C 125°C**

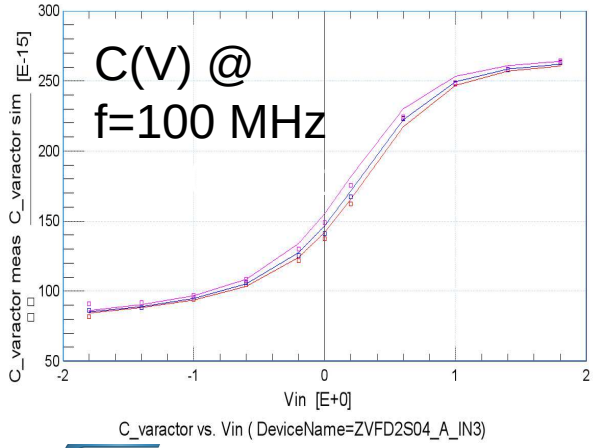
- **Varactor EG, C=274 fF (w=10 µm, l=0,25 µm, Nbfp=3, Nbcell=4)**

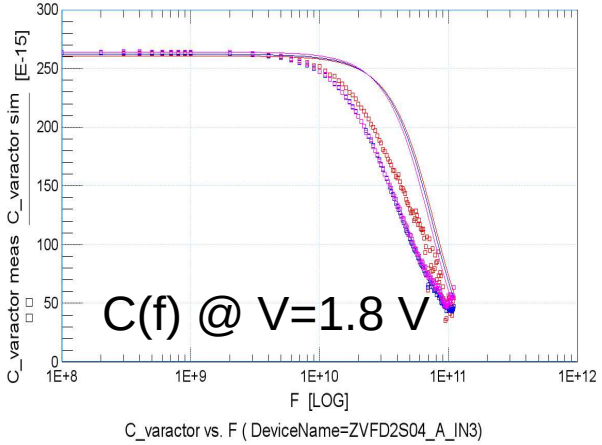


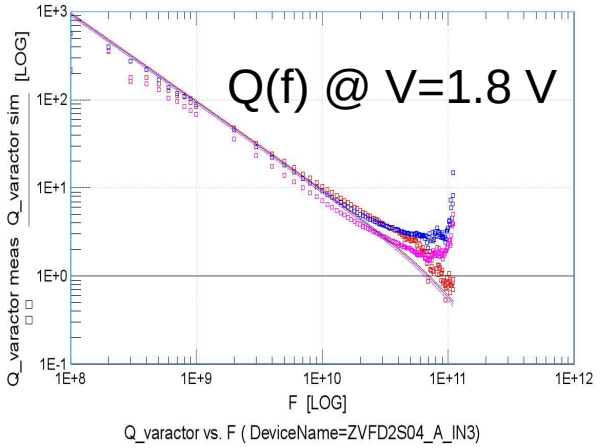




- **Varactor EG, C=262 fF (w=2 µm, l=1 µm, Nbfp=4, Nbcell=4)**





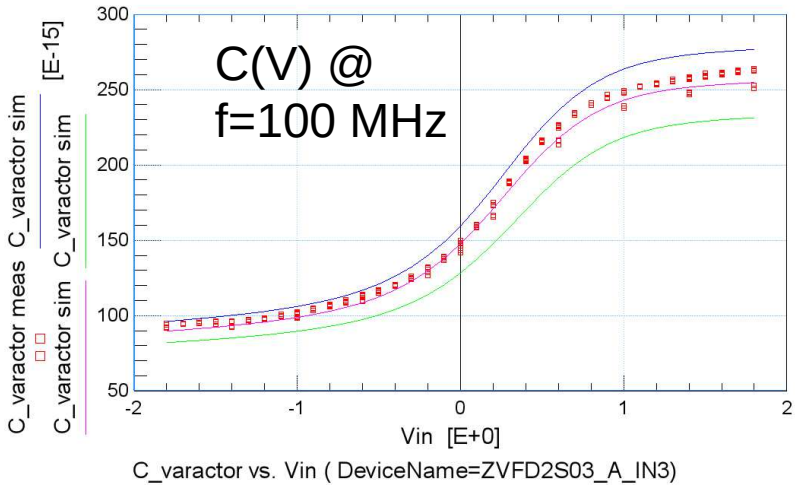


life.augmented

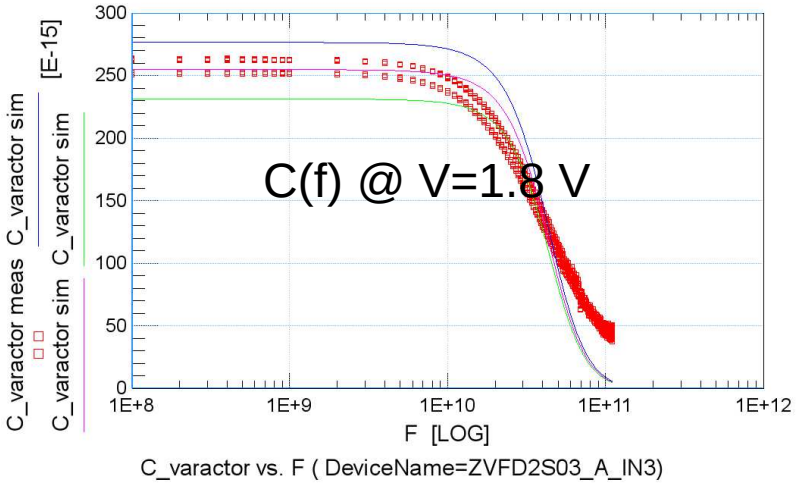
▬ model (min-typ-max) □□ meas

S.E varactors Corners

- **Varactor EG, C=255 fF (w=5 µm, l=0,5 µm, Nbfp=12, Nbcell=1)**

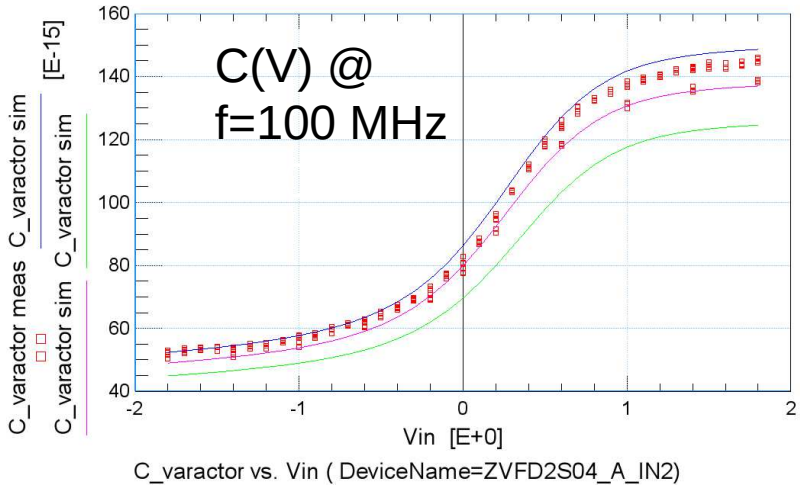


C_varactor vs. Vin (DeviceName=ZVFD2S03_A_IN3)

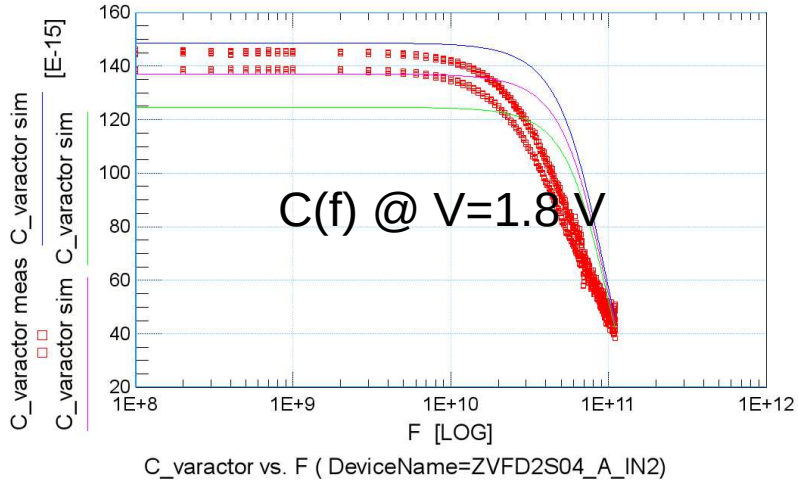


C_varactor vs. F (DeviceName=ZVFD2S03_A_IN3)

- **Varactor EG, C=131 fF (w=2 µm, l=0.5 µm, Nbfp=4, Nbcell=4)**



C_varactor vs. Vin (DeviceName=ZVFD2S04_A_IN2)



C_varactor vs. F (DeviceName=ZVFD2S04_A_IN2)

Measurements come from 2 lots :

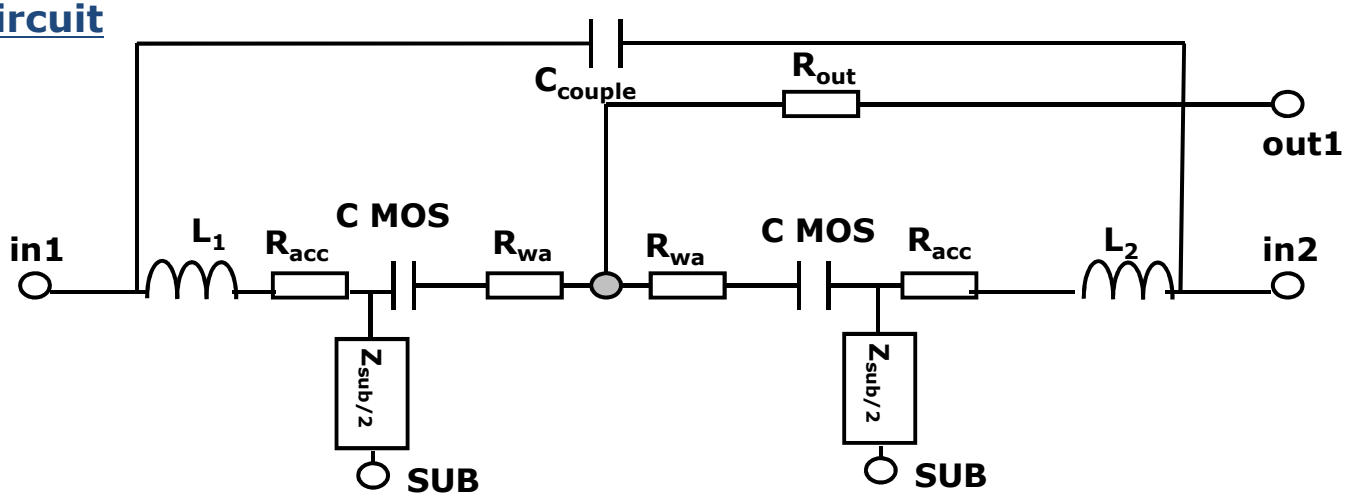
MPW C281348, Lot Q511109, wafer 13, die 34,48,68,72,100

MPW C281608, Lot Q618020, wafer 8, die 47, 71, 97

life.augmented

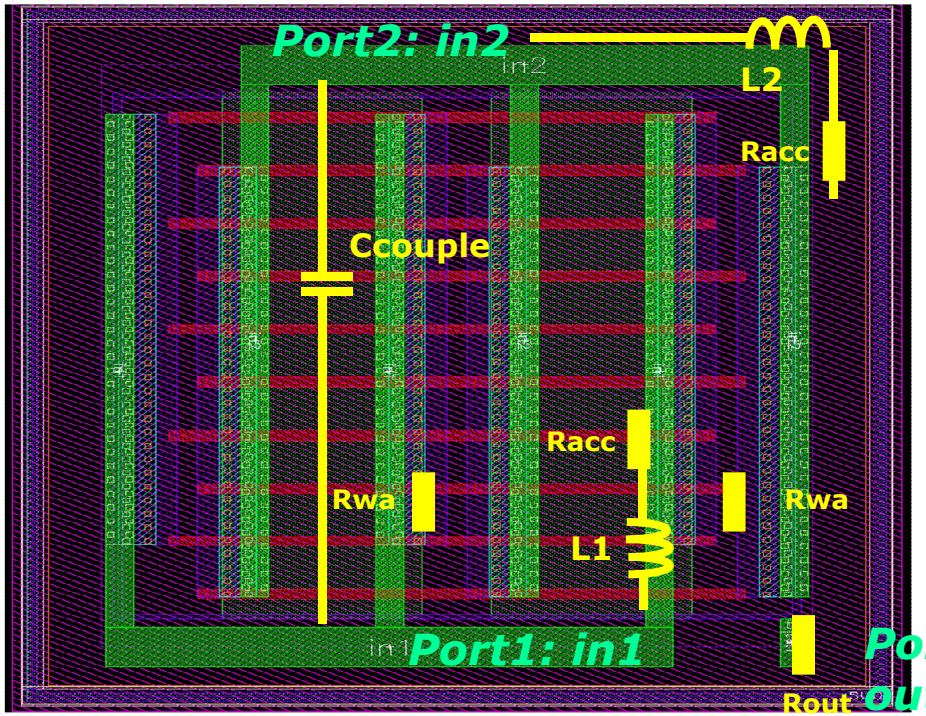
Varactor NMOS EG diff. layout

Equivalent Circuit



Layout varactor

NMOS Diff. Ended



Varactor NMOS EG diff. parameters

- Varactor NMOS EG diff. in CMOS28FDSOI

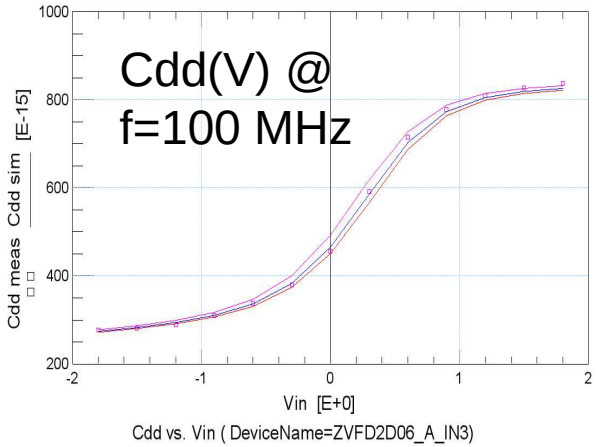
Varactor MOSEG diff	Cap. (F)	Gate Length (µm)	Gate Width (µm)	Nbfp	Ncell	Bias (V)	TR	Worst Case & Min/max
Min	20 f	0.049	1.5	1	1	-1.8	1.5	Yes
Max	10 p	2	10	50	5	1.8	3	

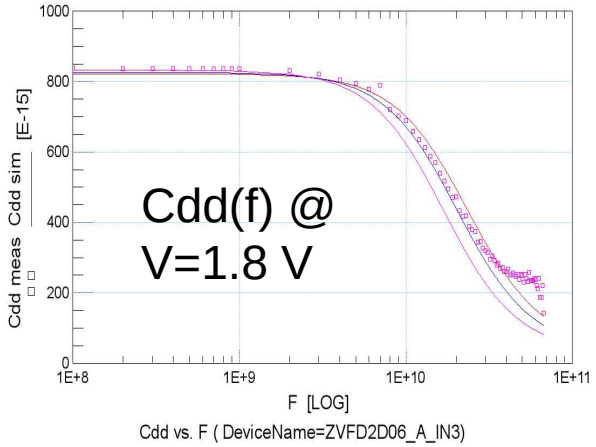
- Model maturity vs DK
  - Tentative: DK < 2.8
  - Prod: since DK 0.9_RF_mmW

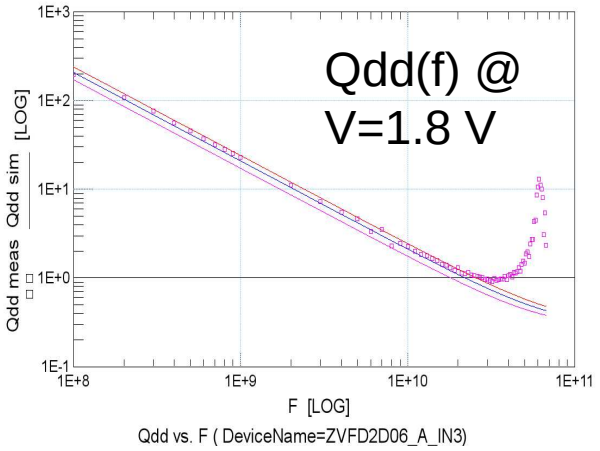
Diff. Varactor measured and simulated performances

Model : -40 °C 25°C 125°C Mes : □□ 25°C

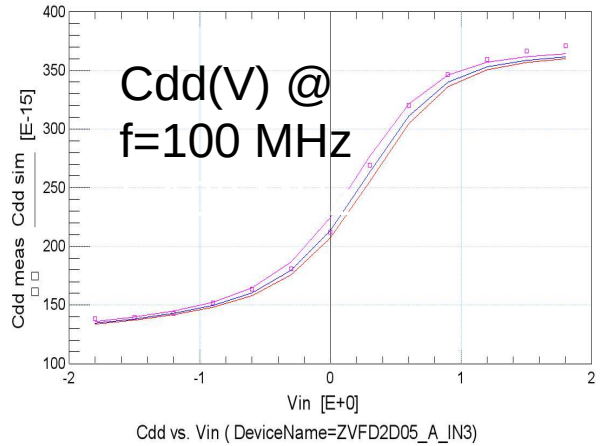
- **Varactor EG, C=362 fF (w=5 µm, l=0,83 µm, Nbfp=10, Nbcell=2)**

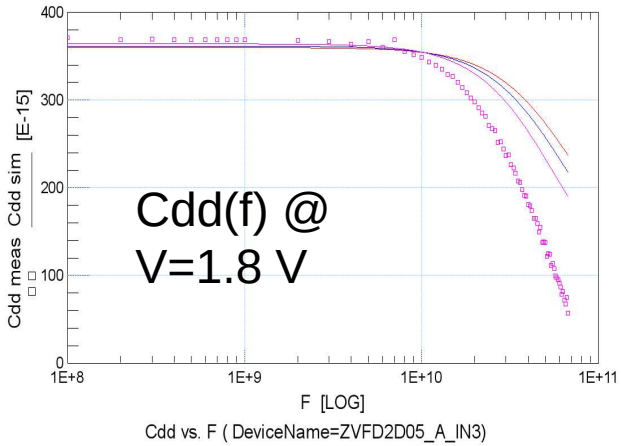


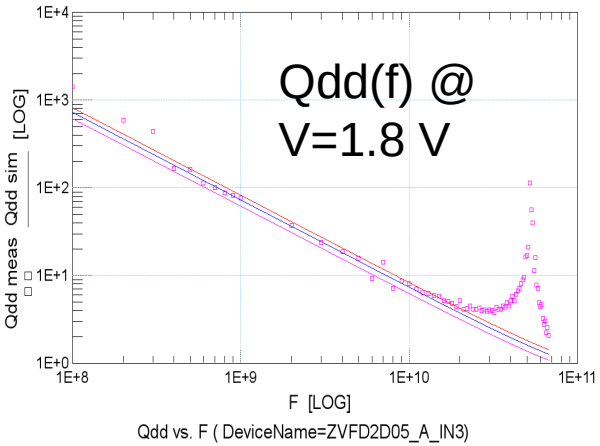




- **Varactor EG, C=826 fF (w=10 µm, l=2 µm, Nbfp=10, Nbcell=1)**





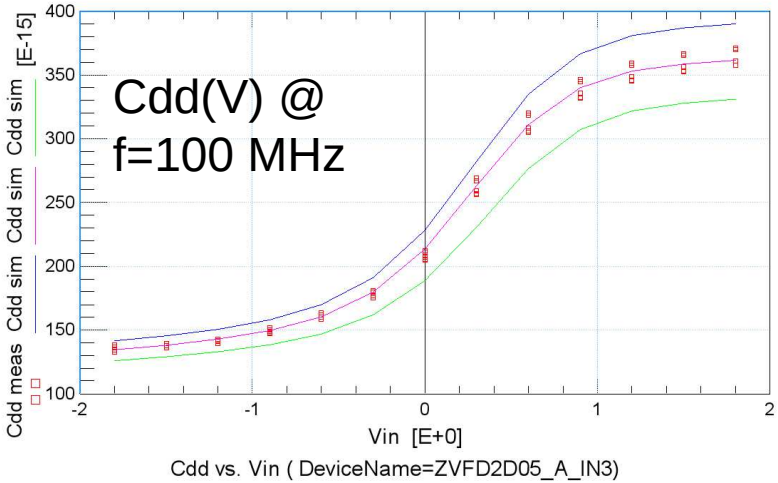


life.augmented

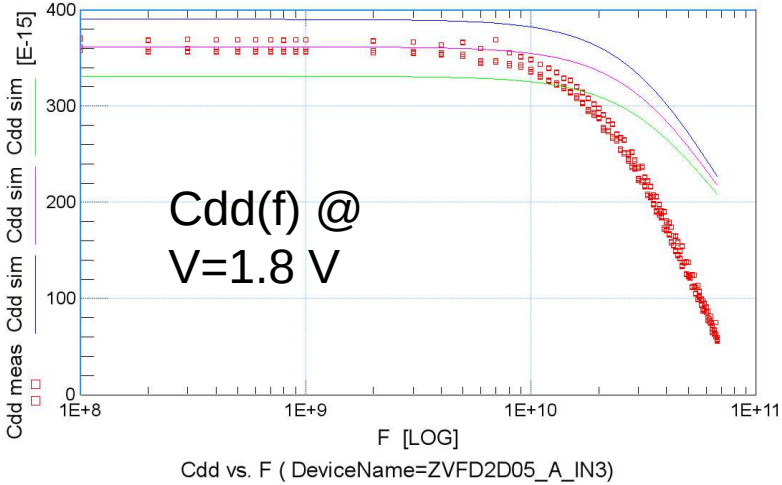
▬ model (min-typ-max) □□ meas

Diff. Varactor Corners

- **Varactor EG, C=371 fF (w=5 µm, l=0,83 µm, Nbfp=10, Nbcell=2)**

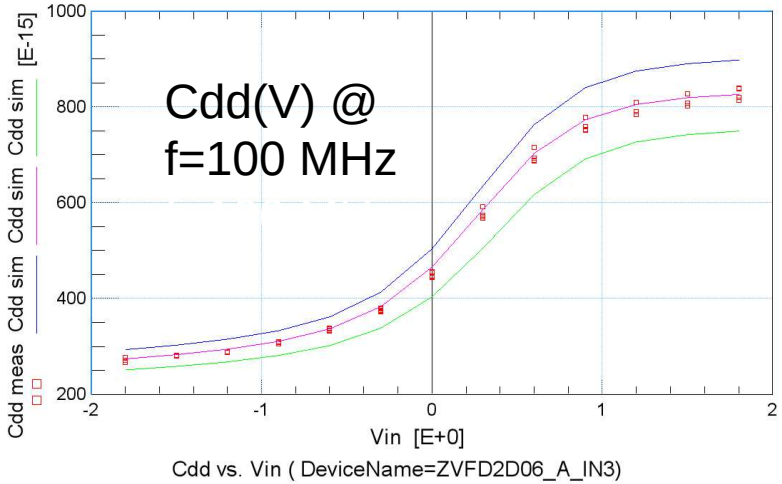


Cdd vs. Vin (DeviceName=ZVFD2D05_A_IN3)

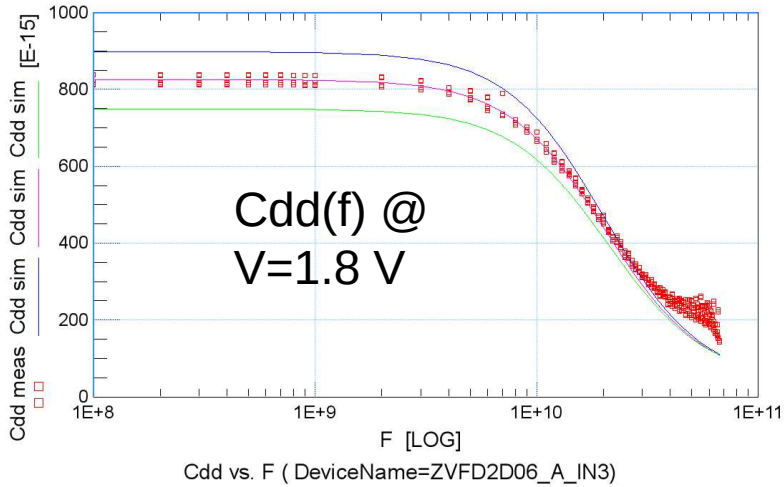


Cdd vs. F (DeviceName=ZVFD2D05_A_IN3)

- **Varactor EG, C=826 fF (w=10 µm, l=2 µm, Nbfp=10, Nbcell=1)**



Cdd vs. Vin (DeviceName=ZVFD2D06_A_IN3)



Cdd vs. F (DeviceName=ZVFD2D06_A_IN3)

Measurements come from 2 lots :

MPW C281348, Lot Q511109, wafer 13, die 47, 60

MPW C281608, Lot Q618020, wafer 8, die 34, 61,96

life.augmented

Conclusions

- Cvar_eg model is MAT 30 (silicon-based).
- Cvar_eg_diff is MAT 30 (silicon-based).
- Frequency use recommendations:
  - We recommend not to use the varactors at frequencies higher than the frequency for which the varactor Q factors falls below 5. For higher frequencies, the model accuracy is decreased.
  - We better recommend varactors use at frequencies below 20GHz. Performances and model are limited at higher frequencies.
- Please note that when using Spectre (version 16.10.387) in Transient and PSS (Periodic Steady State) simulations, the frequency dependency of varactors resistances is ignored, i.e. only DC resistance (constant) is simulated.