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C28SOI_SC_12_CORE_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells

Overview

- C28SOI_SC_12_CORE_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

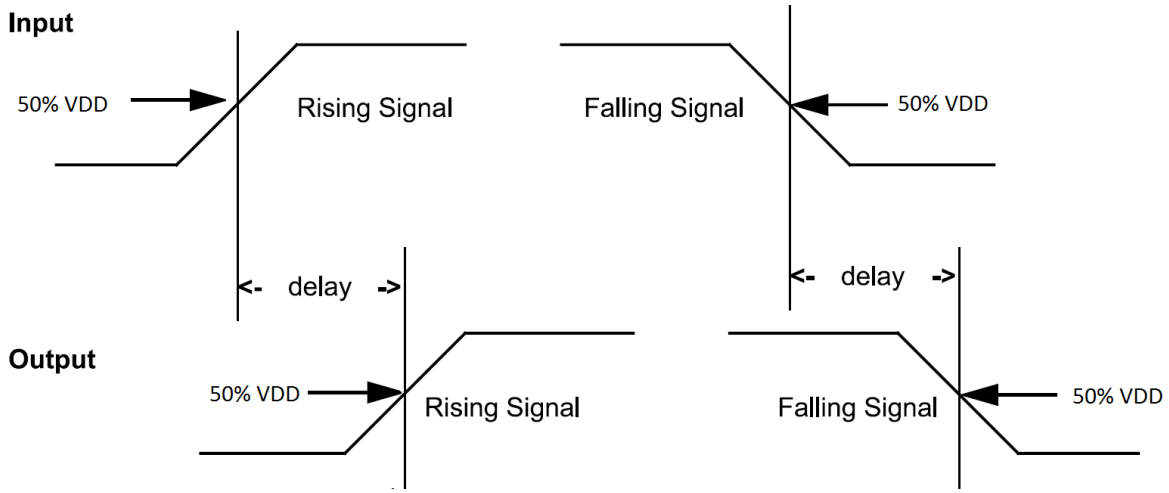


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

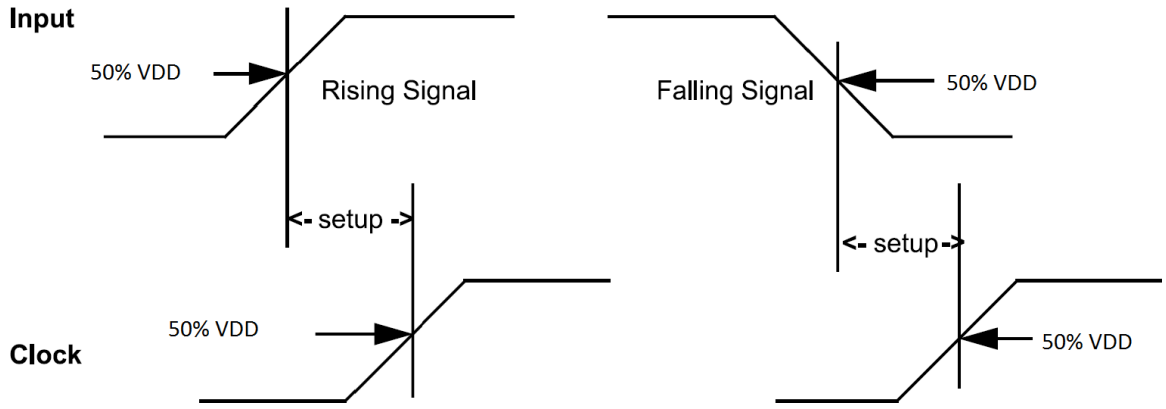


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

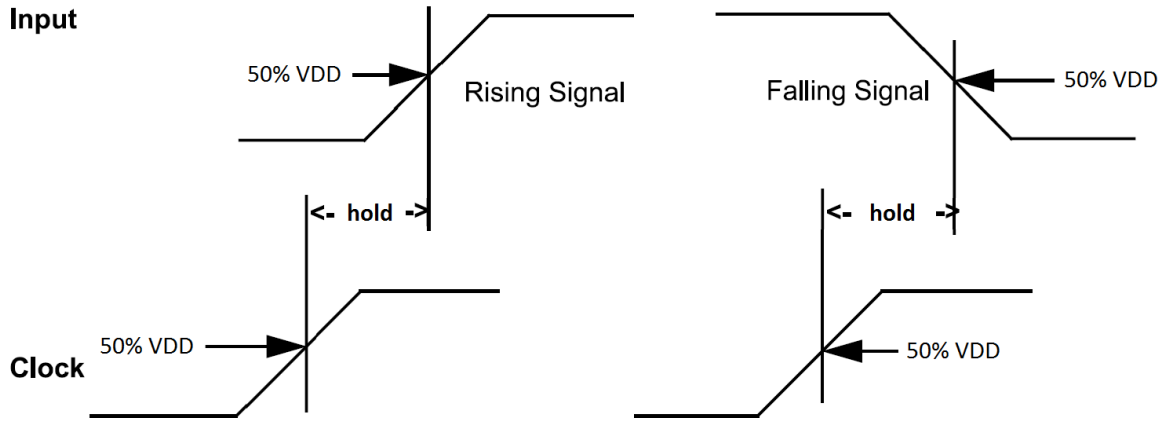


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

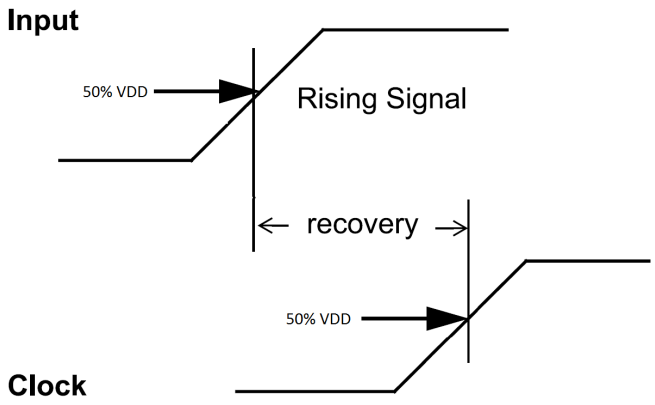


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

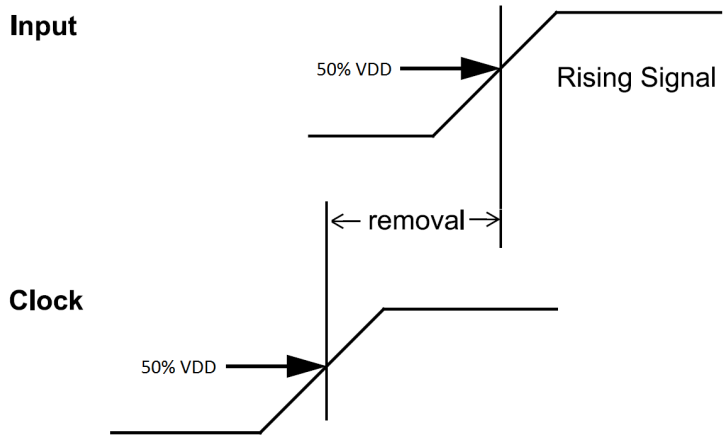


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

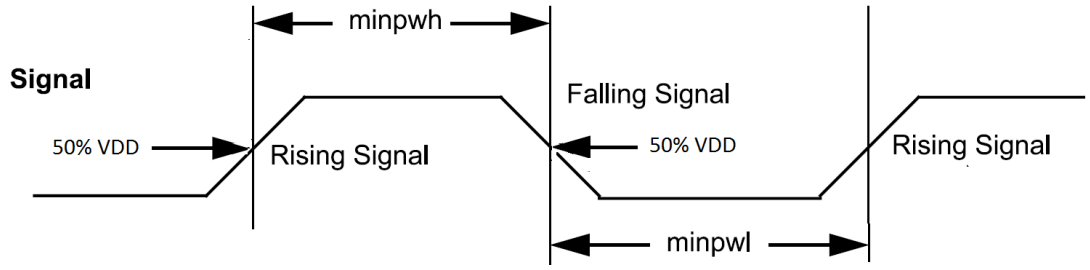


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

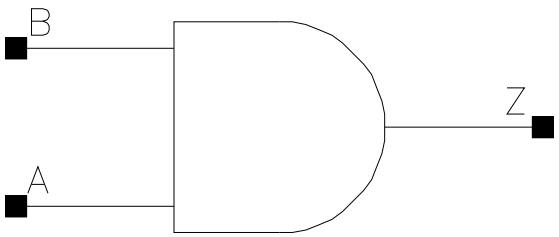
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X25_P0	1.200	1.088	1.3056
X33_P0	1.200	1.360	1.6320
X42_P0	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0007	0.0010	0.0016	0.0019
B	0.0006	0.0010	0.0015	0.0019
	X42_P0			
A	0.0019			
B	0.0019			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0230	0.0187	1.5642	0.7931
A to Z ↑	0.0184	0.0176	2.2665	1.0931
B to Z ↓	0.0218	0.0177	1.5631	0.7932
B to Z ↑	0.0197	0.0186	2.2645	1.0932
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0193	0.0186	0.5253	0.3914

A to Z ↑	0.0171	0.0177	0.7222	0.5468
B to Z ↓	0.0184	0.0169	0.5251	0.3909
B to Z ↑	0.0182	0.0183	0.7223	0.5470
	X42_P0		**X42_P0**	
A to Z ↓	0.0202		0.3181	
A to Z ↑	0.0194		0.4380	
B to Z ↓	0.0186		0.3174	
B to Z ↑	0.0201		0.4383	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.779e-05	1.000e-20
X16_P0	4.250e-05	1.000e-20
X25_P0	6.003e-05	1.000e-20
X33_P0	8.255e-05	1.000e-20
X42_P0	9.687e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	1.700e-05	3.206e-05	5.082e-05	1.184e-04
B (output stable)	3.479e-05	6.283e-05	1.016e-04	3.896e-04
A to Z	2.589e-03	4.421e-03	6.759e-03	8.874e-03
B to Z	2.497e-03	4.278e-03	6.525e-03	8.318e-03
	X42_P0			
A (output stable)	1.198e-04			
B (output stable)	3.908e-04			
A to Z	1.079e-02			
B to Z	1.023e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

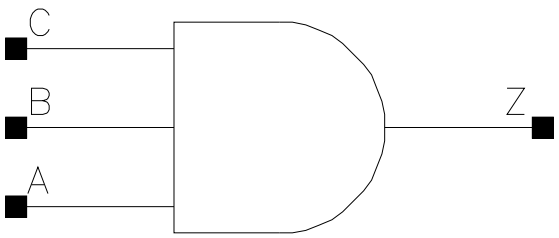
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X25_P0	1.200	1.360	1.6320
X33_P0	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0007	0.0010	0.0017	0.0020
B	0.0006	0.0010	0.0015	0.0019
C	0.0006	0.0010	0.0014	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0248	0.0207	1.5799	0.7743
A to Z ↑	0.0231	0.0222	2.2885	1.0830
B to Z ↓	0.0240	0.0198	1.5798	0.7730
B to Z ↑	0.0244	0.0233	2.2862	1.0840
C to Z ↓	0.0230	0.0188	1.5783	0.7714
C to Z ↑	0.0253	0.0238	2.2873	1.0825
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0208	0.0195	0.5322	0.3977

A to Z ↑	0.0214	0.0207	0.7443	0.5564
B to Z ↓	0.0200	0.0186	0.5321	0.3970
B to Z ↑	0.0227	0.0219	0.7439	0.5569
C to Z ↓	0.0189	0.0176	0.5320	0.3969
C to Z ↑	0.0233	0.0225	0.7431	0.5559

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.874e-05	1.000e-20
X17_P0	4.378e-05	1.000e-20
X25_P0	6.119e-05	1.000e-20
X33_P0	8.487e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	1.796e-05	3.597e-05	4.864e-05	6.604e-05
B (output stable)	4.020e-05	7.921e-05	1.142e-04	1.543e-04
C (output stable)	7.543e-05	1.448e-04	2.143e-04	2.961e-04
A to Z	2.853e-03	5.135e-03	7.418e-03	9.488e-03
B to Z	2.747e-03	4.952e-03	7.125e-03	9.096e-03
C to Z	2.664e-03	4.789e-03	6.868e-03	8.750e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

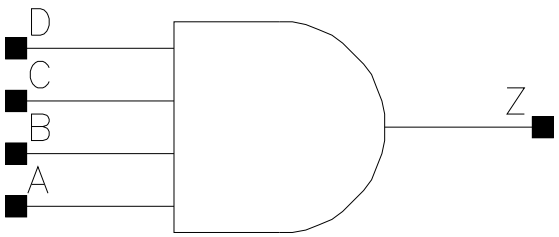
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X6_P0	1.200	1.088	1.3056
X20_P0	1.200	2.312	2.7744
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P0	X6_P0	X20_P0	X27_P0
A	0.0005	0.0008	0.0017	0.0019
B	0.0005	0.0007	0.0017	0.0019
C	0.0005	0.0008	0.0017	0.0019
D	0.0005	0.0007	0.0017	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X6_P0	X4_P0	X6_P0
A to Z ↓	0.0255	0.0224	2.9331	1.9124
A to Z ↑	0.0242	0.0191	7.8247	4.1988
B to Z ↓	0.0247	0.0210	2.9321	1.9123
B to Z ↑	0.0257	0.0198	7.8242	4.2006
C to Z ↓	0.0264	0.0241	2.8935	1.9184
C to Z ↑	0.0244	0.0192	7.8301	4.2038

D to Z ↓	0.0257	0.0225	2.8960	1.9156
D to Z ↑	0.0264	0.0201	7.8314	4.2041
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0215	0.0199	0.5602	0.3966
A to Z ↑	0.0196	0.0222	1.4101	1.0745
B to Z ↓	0.0197	0.0183	0.5592	0.3961
B to Z ↑	0.0201	0.0230	1.4103	1.0751
C to Z ↓	0.0211	0.0193	0.5631	0.3979
C to Z ↑	0.0179	0.0198	1.4094	1.0731
D to Z ↓	0.0191	0.0178	0.5618	0.3972
D to Z ↑	0.0182	0.0205	1.4094	1.0733

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	5.461e-06	1.000e-20
X6_P0	1.727e-05	1.000e-20
X20_P0	5.750e-05	1.000e-20
X27_P0	7.926e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	4.354e-04	6.961e-04	2.043e-03	2.507e-03
B (output stable)	4.128e-04	6.504e-04	1.945e-03	2.407e-03
C (output stable)	4.280e-04	7.207e-04	1.825e-03	2.273e-03
D (output stable)	4.083e-04	6.716e-04	1.715e-03	2.168e-03
A to Z	1.786e-03	2.804e-03	8.404e-03	1.089e-02
B to Z	1.720e-03	2.667e-03	7.813e-03	1.031e-02
C to Z	1.796e-03	2.901e-03	7.409e-03	9.365e-03
D to Z	1.730e-03	2.763e-03	6.817e-03	8.806e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

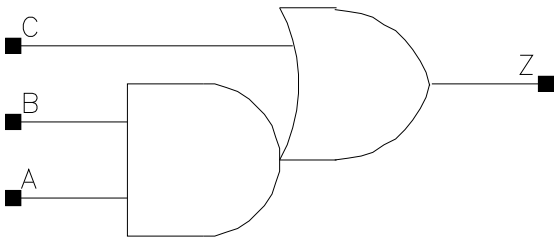
Pin Cycle (vdds)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0020
B	0.0007	0.0010	0.0018
C	0.0007	0.0010	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0286	0.0254	1.5954	0.7827
A to Z ↑	0.0190	0.0173	2.1911	1.0762
B to Z ↓	0.0265	0.0235	1.5926	0.7803
B to Z ↑	0.0205	0.0187	2.1870	1.0762
C to Z ↓	0.0275	0.0243	1.5894	0.7798
C to Z ↑	0.0178	0.0169	2.1755	1.0701
	X33_P0		**X33_P0**	
A to Z ↓	0.0255		0.3982	
A to Z ↑	0.0178		0.5430	

B to Z ↓	0.0239		0.3975	
B to Z ↑	0.0188		0.5424	
C to Z ↓	0.0246		0.3969	
C to Z ↑	0.0168		0.5404	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.378e-05	1.000e-20
X17_P0	3.311e-05	1.000e-20
X33_P0	6.417e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	4.588e-05	8.665e-05	1.987e-04
B (output stable)	5.263e-05	1.007e-04	2.591e-04
C (output stable)	6.467e-05	1.075e-04	2.451e-04
A to Z	2.697e-03	4.782e-03	9.514e-03
B to Z	2.589e-03	4.583e-03	9.064e-03
C to Z	2.879e-03	5.075e-03	1.015e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

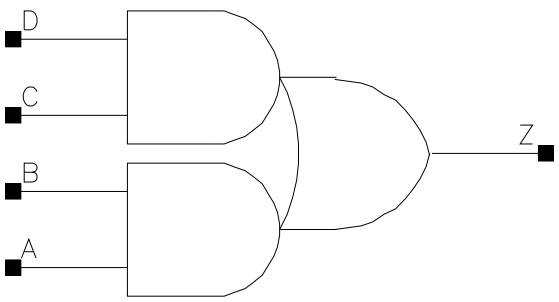
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0019
B	0.0007	0.0010	0.0017
C	0.0006	0.0009	0.0019
D	0.0007	0.0010	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0322	0.0281	1.5428	0.7806
A to Z ↑	0.0244	0.0228	2.1630	1.0755
B to Z ↓	0.0300	0.0262	1.5381	0.7785
B to Z ↑	0.0255	0.0242	2.1604	1.0753

C to Z ↓	0.0295	0.0264	1.5378	0.7789
C to Z ↑	0.0208	0.0196	2.1548	1.0709
D to Z ↓	0.0283	0.0252	1.5363	0.7773
D to Z ↑	0.0225	0.0210	2.1552	1.0712
	X33_P0		**X33_P0**	
A to Z ↓	0.0265		0.3985	
A to Z ↑	0.0207		0.5450	
B to Z ↓	0.0250		0.3982	
B to Z ↑	0.0221		0.5450	
C to Z ↓	0.0247		0.3976	
C to Z ↑	0.0178		0.5430	
D to Z ↓	0.0234		0.3975	
D to Z ↑	0.0190		0.5429	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.835e-05	1.000e-20
X17_P0	4.186e-05	1.000e-20
X33_P0	8.220e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	4.145e-05	6.019e-05	8.964e-05
B (output stable)	1.454e-04	1.847e-04	1.249e-04
C (output stable)	4.831e-05	8.228e-05	1.872e-04
D (output stable)	5.656e-05	9.974e-05	2.326e-04
A to Z	3.485e-03	6.025e-03	1.097e-02
B to Z	3.253e-03	5.720e-03	1.058e-02
C to Z	3.035e-03	5.329e-03	9.555e-03
D to Z	2.946e-03	5.158e-03	9.210e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

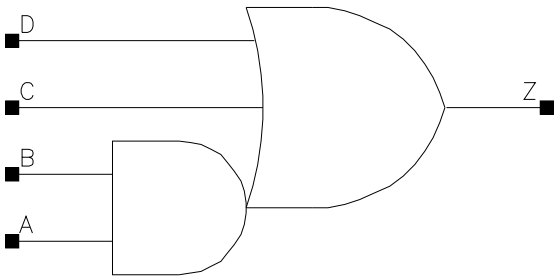
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	0.952	1.1424
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0010	0.0018
B	0.0006	0.0010	0.0018
C	0.0007	0.0009	0.0018
D	0.0006	0.0010	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0369	0.0324	1.6562	0.8208
A to Z ↑	0.0206	0.0192	2.1775	1.1229
B to Z ↓	0.0356	0.0305	1.6529	0.8202
B to Z ↑	0.0221	0.0201	2.1802	1.1233
C to Z ↓	0.0374	0.0323	1.6494	0.8195
C to Z ↑	0.0193	0.0181	2.1634	1.1177

D to Z ↓	0.0376	0.0329	1.6511	0.8200
D to Z ↑	0.0189	0.0180	2.1627	1.1174
	X33_P0		**X33_P0**	
A to Z ↓	0.0332		0.4110	
A to Z ↑	0.0192		0.5435	
B to Z ↓	0.0301		0.4094	
B to Z ↑	0.0199		0.5439	
C to Z ↓	0.0337		0.4097	
C to Z ↑	0.0180		0.5412	
D to Z ↓	0.0334		0.4099	
D to Z ↑	0.0173		0.5401	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.006e-05	1.000e-20
X17_P0	2.456e-05	1.000e-20
X33_P0	4.773e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	4.293e-05	9.962e-05	2.264e-04
B (output stable)	4.459e-05	9.978e-05	2.661e-04
C (output stable)	3.508e-05	6.457e-05	1.822e-04
D (output stable)	4.132e-05	8.202e-05	2.784e-04
A to Z	3.041e-03	5.259e-03	1.067e-02
B to Z	2.951e-03	5.061e-03	9.994e-03
C to Z	3.354e-03	5.778e-03	1.191e-02
D to Z	3.205e-03	5.535e-03	1.116e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

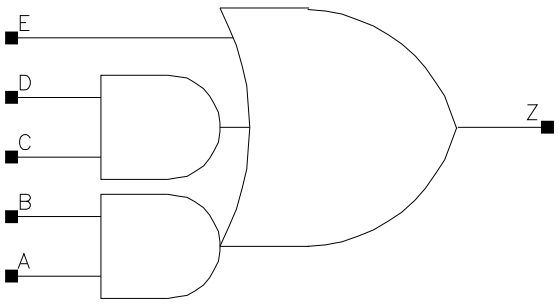
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.088	1.3056
X17_P0	1.200	1.224	1.4688
X33_P0	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0019
B	0.0006	0.0009	0.0017
C	0.0008	0.0012	0.0019
D	0.0007	0.0009	0.0018
E	0.0006	0.0010	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0438	0.0373	1.5750	0.7972
A to Z ↑	0.0257	0.0227	2.1378	1.0797

B to Z ↓	0.0424	0.0356	1.5708	0.7955
B to Z ↑	0.0277	0.0242	2.1370	1.0799
C to Z ↓	0.0383	0.0340	1.5710	0.7956
C to Z ↑	0.0218	0.0193	2.1212	1.0739
D to Z ↓	0.0358	0.0312	1.5650	0.7922
D to Z ↑	0.0233	0.0204	2.1202	1.0739
E to Z ↓	0.0391	0.0336	1.5633	0.7927
E to Z ↑	0.0202	0.0180	2.1035	1.0674
	X33_P0		**X33_P0**	
A to Z ↓	0.0370		0.4110	
A to Z ↑	0.0234		0.5471	
B to Z ↓	0.0349		0.4102	
B to Z ↑	0.0250		0.5466	
C to Z ↓	0.0329		0.4101	
C to Z ↑	0.0193		0.5427	
D to Z ↓	0.0305		0.4088	
D to Z ↑	0.0205		0.5428	
E to Z ↓	0.0331		0.4090	
E to Z ↑	0.0181		0.5391	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.356e-05	1.000e-20
X17_P0	3.177e-05	1.000e-20
X33_P0	6.094e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	2.478e-05	3.945e-05	8.929e-05
B (output stable)	3.246e-05	4.590e-05	1.193e-04
C (output stable)	5.997e-05	1.026e-04	2.505e-04
D (output stable)	6.975e-05	1.244e-04	2.885e-04
E (output stable)	1.125e-04	1.589e-04	3.688e-04
A to Z	4.035e-03	6.626e-03	1.313e-02
B to Z	3.938e-03	6.417e-03	1.258e-02
C to Z	3.303e-03	5.565e-03	1.080e-02
D to Z	3.183e-03	5.331e-03	1.029e-02
E to Z	3.520e-03	5.840e-03	1.138e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

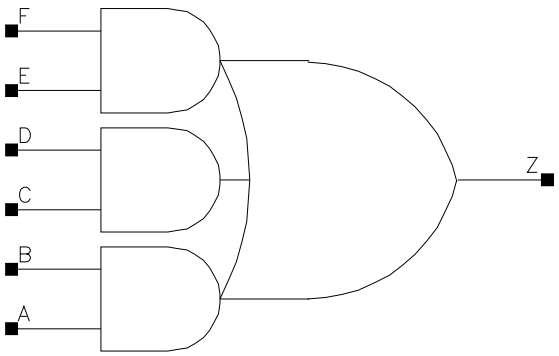
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.360	1.6320
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
A	0.0006	0.0007	0.0009	0.0019

B	0.0006	0.0007	0.0013	0.0017
C	0.0006	0.0007	0.0009	0.0018
D	0.0006	0.0007	0.0009	0.0017
E	0.0007	0.0008	0.0010	0.0019
F	0.0006	0.0007	0.0010	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0442	0.0420	3.0102	1.5866
A to Z ↑	0.0273	0.0265	4.2612	2.1924
B to Z ↓	0.0408	0.0389	2.9939	1.5789
B to Z ↑	0.0283	0.0277	4.2599	2.1913
C to Z ↓	0.0405	0.0389	3.0032	1.5831
C to Z ↑	0.0247	0.0239	4.2364	2.1793
D to Z ↓	0.0388	0.0373	2.9949	1.5788
D to Z ↑	0.0266	0.0258	4.2366	2.1786
E to Z ↓	0.0345	0.0340	2.9917	1.5782
E to Z ↑	0.0208	0.0203	4.2131	2.1696
F to Z ↓	0.0324	0.0319	2.9836	1.5736
F to Z ↑	0.0223	0.0218	4.2162	2.1699
	X17_P0	X33_P0	X17_P0	X33_P0
A to Z ↓	0.0398	0.0383	0.8005	0.4090
A to Z ↑	0.0249	0.0249	1.0843	0.5485
B to Z ↓	0.0375	0.0363	0.7965	0.4083
B to Z ↑	0.0266	0.0265	1.0841	0.5485
C to Z ↓	0.0375	0.0360	0.7989	0.4089
C to Z ↑	0.0227	0.0230	1.0788	0.5458
D to Z ↓	0.0355	0.0343	0.7964	0.4083
D to Z ↑	0.0243	0.0245	1.0783	0.5453
E to Z ↓	0.0327	0.0330	0.7959	0.4079
E to Z ↑	0.0191	0.0200	1.0747	0.5440
F to Z ↓	0.0307	0.0307	0.7935	0.4067
F to Z ↑	0.0205	0.0214	1.0750	0.5437

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	1.006e-05	1.000e-20
X8_P0	2.073e-05	1.000e-20
X17_P0	4.023e-05	1.000e-20
X33_P0	7.710e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	4.380e-05	5.147e-05	6.591e-05	1.214e-04
B (output stable)	1.151e-04	1.283e-04	1.409e-04	1.775e-04
C (output stable)	4.727e-05	5.857e-05	7.456e-05	1.670e-04
D (output stable)	5.457e-05	6.852e-05	8.700e-05	2.345e-04
E (output stable)	9.313e-05	1.244e-04	1.751e-04	3.009e-04
F (output stable)	9.772e-05	1.275e-04	1.868e-04	3.541e-04

A to Z	3.482e-03	4.742e-03	7.379e-03	1.398e-02
B to Z	3.215e-03	4.435e-03	6.973e-03	1.342e-02
C to Z	2.985e-03	4.149e-03	6.583e-03	1.248e-02
D to Z	2.878e-03	4.016e-03	6.375e-03	1.200e-02
E to Z	2.473e-03	3.572e-03	5.714e-03	1.119e-02
F to Z	2.367e-03	3.436e-03	5.510e-03	1.071e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

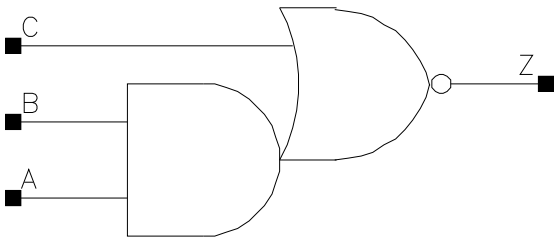
Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008
X44_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X33_P0	X44_P0
A	0.0008	0.0023	0.0046	0.0062
B	0.0007	0.0021	0.0042	0.0058
C	0.0008	0.0024	0.0048	0.0062

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0077	0.0078	2.8019	0.9519
A to Z ↑	0.0133	0.0135	4.3275	1.4563
B to Z ↓	0.0079	0.0080	2.8275	0.9641
B to Z ↑	0.0110	0.0108	4.2509	1.4548
C to Z ↓	0.0077	0.0078	1.6373	0.5649
C to Z ↑	0.0129	0.0127	3.9602	1.3445
	X33_P0	**X44_P0**	**X33_P0**	**X44_P0**
A to Z ↓	0.0081	0.0081	0.4858	0.3693

A to Z ↑	0.0136	0.0136	0.7302	0.5558
B to Z ↓	0.0082	0.0082	0.4919	0.3741
B to Z ↑	0.0109	0.0109	0.7276	0.5517
C to Z ↓	0.0093	0.0093	0.3354	0.2607
C to Z ↑	0.0130	0.0128	0.6731	0.5115

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P0	1.375e-05	1.000e-20
X17_P0	3.963e-05	1.000e-20
X33_P0	7.669e-05	1.000e-20
X44_P0	1.019e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	8.880e-05	2.618e-04	5.844e-04	7.334e-04
B (output stable)	9.950e-05	3.566e-04	7.821e-04	9.730e-04
C (output stable)	1.058e-04	3.195e-04	7.012e-04	8.920e-04
A to Z	1.387e-03	4.278e-03	8.665e-03	1.144e-02
B to Z	1.220e-03	3.519e-03	7.142e-03	9.417e-03
C to Z	1.787e-03	5.243e-03	1.064e-02	1.386e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

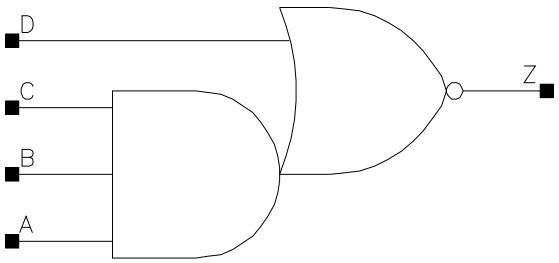
Pin Cycle (vdds)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X29_P0	1.200	3.536	4.2432
X38_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X29_P0	X38_P0
A	0.0008	0.0046	0.0061
B	0.0007	0.0045	0.0058
C	0.0007	0.0042	0.0056
D	0.0008	0.0048	0.0059

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X29_P0	X5_P0	X29_P0
A to Z ↓	0.0114	0.0120	3.9435	0.6875
A to Z ↑	0.0169	0.0168	4.3313	0.7212
B to Z ↓	0.0121	0.0122	3.9650	0.6923
B to Z ↑	0.0152	0.0150	4.3340	0.7276
C to Z ↓	0.0120	0.0118	3.9780	0.6958
C to Z ↑	0.0131	0.0125	4.2645	0.7330
D to Z ↓	0.0095	0.0111	1.6760	0.3376

D to Z ↑	0.0152	0.0153	3.7127	0.6267
	X38_P0		**X38_P0**	
A to Z ↓	0.0117		0.5344	
A to Z ↑	0.0163		0.5448	
B to Z ↓	0.0119		0.5386	
B to Z ↑	0.0144		0.5512	
C to Z ↓	0.0115		0.5413	
C to Z ↑	0.0120		0.5581	
D to Z ↓	0.0118		0.2818	
D to Z ↑	0.0148		0.4745	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.352e-05	1.000e-20
X29_P0	7.470e-05	1.000e-20
X38_P0	9.808e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X29_P0	X38_P0
A (output stable)	5.203e-05	3.967e-04	5.111e-04
B (output stable)	7.054e-05	5.671e-04	7.334e-04
C (output stable)	9.834e-05	9.061e-04	1.166e-03
D (output stable)	1.284e-04	9.518e-04	1.249e-03
A to Z	1.871e-03	1.157e-02	1.455e-02
B to Z	1.667e-03	9.864e-03	1.237e-02
C to Z	1.490e-03	8.301e-03	1.035e-02
D to Z	2.241e-03	1.342e-02	1.708e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

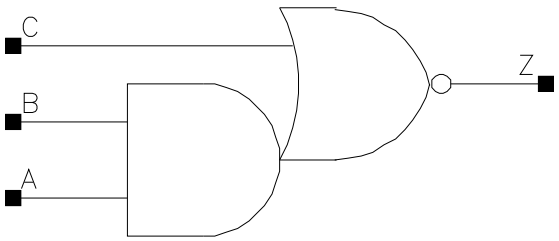
Pin Cycle (vdds)	X5_P0	X29_P0	X38_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X11_P0	1.200	1.088	1.3056
X16_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X11_P0	X16_P0	X23_P0
A	0.0008	0.0017	0.0024	0.0033
B	0.0008	0.0016	0.0023	0.0030
C	0.0008	0.0015	0.0022	0.0032
	X46_P0			
A	0.0063			
B	0.0060			
C	0.0062			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X11_P0	X6_P0	X11_P0
A to Z ↓	0.0093	0.0100	2.6993	1.3788
A to Z ↑	0.0140	0.0147	4.3245	2.1162
B to Z ↓	0.0099	0.0102	2.7257	1.3942

B to Z ↑	0.0122	0.0123	4.2598	2.1231
C to Z ↓	0.0052	0.0057	1.6892	0.9950
C to Z ↑	0.0110	0.0106	3.9628	1.9576
	X16_P0	**X23_P0**	**X16_P0**	**X23_P0**
A to Z ↓	0.0094	0.0098	0.9514	0.7174
A to Z ↑	0.0136	0.0140	1.4259	1.0812
B to Z ↓	0.0101	0.0101	0.9628	0.7248
B to Z ↑	0.0112	0.0115	1.4242	1.0854
C to Z ↓	0.0058	0.0049	0.6907	0.4366
C to Z ↑	0.0100	0.0106	1.3184	1.0006
	X46_P0		**X46_P0**	
A to Z ↓	0.0094		0.3689	
A to Z ↑	0.0134		0.5650	
B to Z ↓	0.0098		0.3731	
B to Z ↑	0.0109		0.5630	
C to Z ↓	0.0052		0.2236	
C to Z ↑	0.0107		0.5212	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P0	1.368e-05	1.000e-20
X11_P0	2.803e-05	1.000e-20
X16_P0	4.015e-05	1.000e-20
X23_P0	5.418e-05	1.000e-20
X46_P0	1.056e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	3.535e-05	9.849e-05	1.244e-04	1.815e-04
B (output stable)	4.612e-05	1.833e-04	2.006e-04	3.136e-04
C (output stable)	2.796e-04	7.051e-04	7.796e-04	1.132e-03
A to Z	1.769e-03	3.806e-03	5.201e-03	7.144e-03
B to Z	1.579e-03	3.256e-03	4.414e-03	6.017e-03
C to Z	1.247e-03	2.513e-03	3.485e-03	4.933e-03
	X46_P0			
A (output stable)	3.265e-04			
B (output stable)	5.414e-04			
C (output stable)	1.887e-03			
A to Z	1.326e-02			
B to Z	1.117e-02			
C to Z	9.367e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

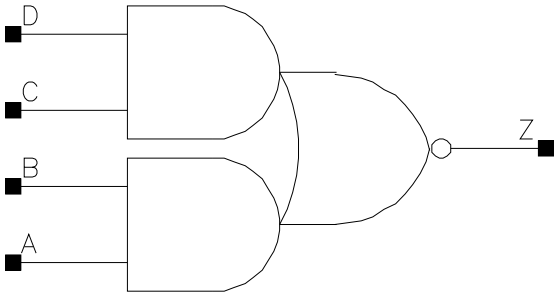
	X46_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P0	X10_P0	X16_P0	X21_P0
A	0.0007	0.0017	0.0025	0.0032
B	0.0007	0.0015	0.0023	0.0031
C	0.0006	0.0016	0.0023	0.0031
D	0.0007	0.0014	0.0022	0.0029
	X42_P0			
A	0.0064			
B	0.0060			
C	0.0061			
D	0.0058			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X10_P0**	**X4_P0**	**X10_P0**
A to Z ↓	0.0105	0.0104	3.3479	1.3224
A to Z ↑	0.0187	0.0154	5.9356	1.9590
B to Z ↓	0.0113	0.0114	3.3824	1.3369
B to Z ↑	0.0167	0.0140	5.9128	2.0118
C to Z ↓	0.0077	0.0074	3.4344	1.3315
C to Z ↑	0.0154	0.0132	5.9013	1.9614
D to Z ↓	0.0081	0.0080	3.4780	1.3493
D to Z ↑	0.0133	0.0114	5.8749	1.9926
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0113	0.0112	0.9551	0.7201
A to Z ↑	0.0161	0.0160	1.3220	1.0267
B to Z ↓	0.0121	0.0117	0.9653	0.7276
B to Z ↑	0.0139	0.0138	1.3214	1.0280
C to Z ↓	0.0079	0.0081	0.9549	0.7210
C to Z ↑	0.0135	0.0140	1.3167	1.0211
D to Z ↓	0.0083	0.0082	0.9682	0.7305
D to Z ↑	0.0111	0.0114	1.3172	1.0219
	X42_P0		**X42_P0**	
A to Z ↓	0.0119		0.3751	
A to Z ↑	0.0163		0.5165	
B to Z ↓	0.0123		0.3792	
B to Z ↑	0.0138		0.5137	
C to Z ↓	0.0087		0.3716	
C to Z ↑	0.0142		0.5150	
D to Z ↓	0.0088		0.3766	
D to Z ↑	0.0117		0.5126	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	8.916e-06	1.000e-20
X10_P0	3.356e-05	1.000e-20
X16_P0	4.701e-05	1.000e-20
X21_P0	6.243e-05	1.000e-20
X42_P0	1.222e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	3.625e-05	8.556e-05	1.642e-04	2.241e-04
B (output stable)	4.973e-05	1.217e-04	3.313e-04	4.784e-04
C (output stable)	7.676e-05	1.852e-04	3.208e-04	4.109e-04
D (output stable)	9.282e-05	2.291e-04	4.858e-04	6.647e-04
A to Z	1.734e-03	4.295e-03	6.660e-03	8.603e-03
B to Z	1.556e-03	3.870e-03	5.797e-03	7.507e-03
C to Z	1.163e-03	3.035e-03	4.576e-03	6.225e-03
D to Z	1.017e-03	2.664e-03	3.833e-03	5.179e-03
	X42_P0			
A (output stable)	4.294e-04			
B (output stable)	8.735e-04			
C (output stable)	7.928e-04			
D (output stable)	1.229e-03			

A to Z	1.699e-02			
B to Z	1.480e-02			
C to Z	1.220e-02			
D to Z	1.025e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

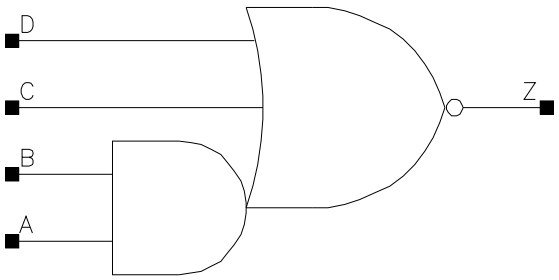
Pin Cycle (vdds)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X35_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P0	X35_P0
A	0.0008	0.0059
B	0.0008	0.0055
C	0.0008	0.0057
D	0.0008	0.0053

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X35_P0	X5_P0	X35_P0
A to Z ↓	0.0091	0.0094	2.8303	0.4197
A to Z ↑	0.0179	0.0167	6.3576	0.8227
B to Z ↓	0.0095	0.0097	2.8638	0.4258
B to Z ↑	0.0153	0.0137	6.3017	0.8211
C to Z ↓	0.0096	0.0129	1.7484	0.3350
C to Z ↑	0.0187	0.0181	6.0046	0.7784
D to Z ↓	0.0092	0.0118	1.7645	0.3350

D to Z ↑	0.0187	0.0173	6.0188	0.7818

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.088e-05	1.000e-20
X35_P0	8.151e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X35_P0
A (output stable)	9.470e-05	7.679e-04
B (output stable)	9.804e-05	8.611e-04
C (output stable)	6.144e-05	6.672e-04
D (output stable)	7.902e-05	8.625e-04
A to Z	1.588e-03	1.149e-02
B to Z	1.398e-03	9.624e-03
C to Z	2.247e-03	1.691e-02
D to Z	1.968e-03	1.402e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

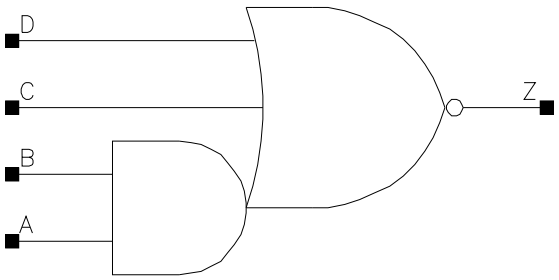
Pin Cycle (vdds)	X5_P0	X35_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X17_P0	1.200	2.448	2.9376
X34_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P0	X17_P0	X34_P0
A	0.0008	0.0032	0.0064
B	0.0008	0.0031	0.0061
C	0.0007	0.0028	0.0054
D	0.0007	0.0026	0.0050

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X17_P0	X4_P0	X17_P0
A to Z ↓	0.0109	0.0118	3.0544	0.8089
A to Z ↑	0.0185	0.0193	6.4128	1.5838
B to Z ↓	0.0119	0.0123	3.0860	0.8176
B to Z ↑	0.0163	0.0165	6.3314	1.5856
C to Z ↓	0.0101	0.0099	2.7626	0.6705
C to Z ↑	0.0138	0.0144	6.0499	1.5043

D to Z ↓	0.0084	0.0075	2.8119	0.6743
D to Z ↑	0.0132	0.0121	6.0631	1.5080
	X34_P0		**X34_P0**	
A to Z ↓	0.0116		0.4155	
A to Z ↑	0.0190		0.8104	
B to Z ↓	0.0124		0.4201	
B to Z ↑	0.0161		0.8063	
C to Z ↓	0.0103		0.3573	
C to Z ↑	0.0139		0.7678	
D to Z ↓	0.0079		0.3605	
D to Z ↑	0.0119		0.7699	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	1.078e-05	1.000e-20
X17_P0	4.251e-05	1.000e-20
X34_P0	8.347e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X17_P0	X34_P0
A (output stable)	3.232e-05	1.581e-04	3.092e-04
B (output stable)	3.564e-05	2.174e-04	4.105e-04
C (output stable)	8.378e-05	4.470e-04	8.603e-04
D (output stable)	1.422e-04	9.011e-04	1.684e-03
A to Z	2.056e-03	8.795e-03	1.698e-02
B to Z	1.867e-03	7.638e-03	1.479e-02
C to Z	1.377e-03	5.889e-03	1.120e-02
D to Z	1.146e-03	4.442e-03	8.468e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

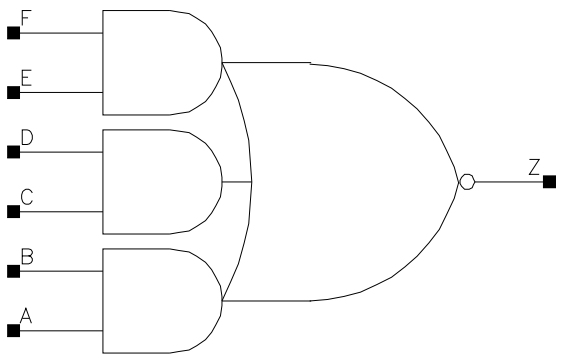
Pin Cycle (vdds)	X4_P0	X17_P0	X34_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X8_P0	1.200	2.176	2.6112
X13_P0	1.200	2.720	3.2640
X17_P0	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P0	X8_P0	X13_P0	X17_P0
A	0.0008	0.0016	0.0024	0.0032

B	0.0008	0.0015	0.0023	0.0030
C	0.0008	0.0015	0.0023	0.0029
D	0.0008	0.0014	0.0021	0.0028
E	0.0010	0.0015	0.0022	0.0029
F	0.0008	0.0014	0.0020	0.0027

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0131	0.0156	2.7047	1.5652
A to Z ↑	0.0270	0.0266	6.1609	2.8629
B to Z ↓	0.0145	0.0165	2.7319	1.5772
B to Z ↑	0.0248	0.0241	6.1479	2.8686
C to Z ↓	0.0117	0.0139	2.6901	1.5820
C to Z ↑	0.0239	0.0241	6.2035	2.8780
D to Z ↓	0.0128	0.0149	2.7233	1.5985
D to Z ↑	0.0216	0.0215	6.1612	2.8764
E to Z ↓	0.0088	0.0105	2.6622	1.5857
E to Z ↑	0.0194	0.0194	6.1150	2.8501
F to Z ↓	0.0092	0.0110	2.7058	1.6081
F to Z ↑	0.0172	0.0166	6.1585	2.8523
	X13_P0	**X17_P0**	**X13_P0**	**X17_P0**
A to Z ↓	0.0149	0.0151	1.0643	0.8127
A to Z ↑	0.0245	0.0247	1.8887	1.4509
B to Z ↓	0.0162	0.0160	1.0726	0.8192
B to Z ↑	0.0223	0.0221	1.8951	1.4505
C to Z ↓	0.0133	0.0133	1.0716	0.8067
C to Z ↑	0.0220	0.0224	1.9021	1.4633
D to Z ↓	0.0144	0.0140	1.0822	0.8146
D to Z ↑	0.0197	0.0198	1.9041	1.4593
E to Z ↓	0.0101	0.0100	1.0688	0.8088
E to Z ↑	0.0180	0.0181	1.8883	1.4456
F to Z ↓	0.0106	0.0102	1.0830	0.8194
F to Z ↑	0.0154	0.0154	1.8906	1.4517

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	1.675e-05	1.000e-20
X8_P0	3.631e-05	1.000e-20
X13_P0	5.195e-05	1.000e-20
X17_P0	6.884e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

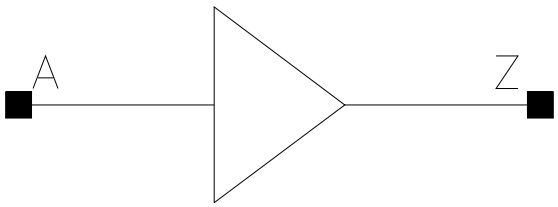
Pin Cycle (vdd)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	5.634e-05	1.322e-04	1.838e-04	2.494e-04
B (output stable)	6.499e-05	2.301e-04	2.713e-04	4.153e-04
C (output stable)	8.692e-05	1.889e-04	2.481e-04	3.408e-04
D (output stable)	9.801e-05	2.943e-04	3.393e-04	5.024e-04
E (output stable)	1.451e-04	3.590e-04	4.775e-04	6.462e-04
F (output stable)	1.678e-04	4.586e-04	5.710e-04	8.060e-04

A to Z	3.209e-03	6.736e-03	9.297e-03	1.236e-02
B to Z	2.977e-03	6.145e-03	8.529e-03	1.118e-02
C to Z	2.473e-03	5.392e-03	7.265e-03	9.695e-03
D to Z	2.270e-03	4.852e-03	6.572e-03	8.646e-03
E to Z	1.785e-03	3.957e-03	5.317e-03	7.060e-03
F to Z	1.604e-03	3.415e-03	4.636e-03	6.068e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X6_P0	1.200	0.408	0.4896
X8_P0	1.200	0.408	0.4896
X13_P0	1.200	0.544	0.6528
X16_P0	1.200	0.544	0.6528
X21_P0	1.200	0.680	0.8160
X25_P0	1.200	0.680	0.8160
X29_P0	1.200	0.952	1.1424
X33_P0	1.200	0.952	1.1424
X42_P0	1.200	1.088	1.3056
X50_P0	1.200	1.224	1.4688
X58_P0	1.200	1.496	1.7952
X67_P0	1.200	1.632	1.9584
X75_P0	1.200	1.768	2.1216
X84_P0	1.200	1.904	2.2848
X100_P0	1.200	2.312	2.7744
X134_P0	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0008	0.0008	0.0008	0.0008
	X16_P0	X21_P0	X25_P0	X29_P0
A	0.0008	0.0011	0.0011	0.0015
	X33_P0	X42_P0	X50_P0	X58_P0
A	0.0014	0.0016	0.0019	0.0029

	X67_P0	X75_P0	X84_P0	X100_P0
A	0.0029	0.0028	0.0028	0.0037
	X134_P0			
A	0.0047			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0182	0.0184	2.8501	2.0856
A to Z ↑	0.0145	0.0144	4.1627	3.0629
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0192	0.0215	1.5477	0.9976
A to Z ↑	0.0149	0.0169	2.1867	1.4327
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0232	0.0191	0.7931	0.6152
A to Z ↑	0.0180	0.0158	1.0960	0.8615
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0201	0.0194	0.5277	0.4442
A to Z ↑	0.0164	0.0150	0.7221	0.6156
	X33_P0	**X42_P0**	**X33_P0**	**X42_P0**
A to Z ↓	0.0203	0.0197	0.3948	0.3206
A to Z ↑	0.0156	0.0160	0.5393	0.4340
	X50_P0	**X58_P0**	**X50_P0**	**X58_P0**
A to Z ↓	0.0192	0.0179	0.2660	0.2299
A to Z ↑	0.0157	0.0149	0.3602	0.3101
	X67_P0	**X75_P0**	**X67_P0**	**X75_P0**
A to Z ↓	0.0188	0.0198	0.2018	0.1818
A to Z ↑	0.0155	0.0164	0.2720	0.2434
	X84_P0	**X100_P0**	**X84_P0**	**X100_P0**
A to Z ↓	0.0207	0.0193	0.1644	0.1382
A to Z ↑	0.0171	0.0161	0.2197	0.1841
	X134_P0		**X134_P0**	
A to Z ↓	0.0206		0.1070	
A to Z ↑	0.0172		0.1411	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	8.012e-06	1.000e-20
X6_P0	1.098e-05	1.000e-20
X8_P0	1.537e-05	1.000e-20
X13_P0	1.933e-05	1.000e-20
X16_P0	2.755e-05	1.000e-20
X21_P0	3.902e-05	1.000e-20
X25_P0	4.571e-05	1.000e-20
X29_P0	4.941e-05	1.000e-20
X33_P0	5.489e-05	1.000e-20
X42_P0	7.121e-05	1.000e-20
X50_P0	8.745e-05	1.000e-20
X58_P0	1.084e-04	1.000e-20
X67_P0	1.188e-04	1.000e-20
X75_P0	1.293e-04	1.000e-20

X84_P0	1.397e-04	1.000e-20
X100_P0	1.711e-04	1.000e-20
X134_P0	2.234e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	1.816e-03	2.034e-03	2.402e-03	3.242e-03
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	4.004e-03	5.315e-03	5.999e-03	6.811e-03
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	7.538e-03	9.450e-03	1.116e-02	1.357e-02
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	1.510e-02	1.699e-02	1.874e-02	2.219e-02
	X134_P0			
A to Z	3.095e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

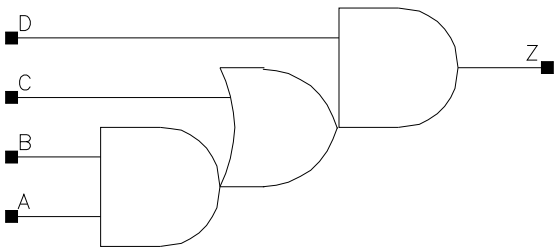
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P0			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.632	1.9584
X25_P0	1.200	1.768	2.1216
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0009	0.0020	0.0020	0.0019
B	0.0009	0.0018	0.0017	0.0017
C	0.0010	0.0022	0.0022	0.0022
D	0.0015	0.0019	0.0019	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0240	0.0226	1.5758	0.7832
A to Z ↑	0.0233	0.0221	2.2161	1.0794
B to Z ↓	0.0222	0.0207	1.5736	0.7823
B to Z ↑	0.0238	0.0222	2.2164	1.0794
C to Z ↓	0.0210	0.0196	1.5716	0.7811
C to Z ↑	0.0177	0.0163	2.1947	1.0695

D to Z ↓	0.0205	0.0181	1.5595	0.7754
D to Z ↑	0.0200	0.0175	2.1997	1.0714
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0249	0.0263	0.5321	0.3997
A to Z ↑	0.0242	0.0255	0.7321	0.5495
B to Z ↓	0.0231	0.0249	0.5318	0.3995
B to Z ↑	0.0244	0.0261	0.7320	0.5491
C to Z ↓	0.0219	0.0237	0.5302	0.3981
C to Z ↑	0.0181	0.0195	0.7246	0.5432
D to Z ↓	0.0196	0.0206	0.5251	0.3937
D to Z ↑	0.0192	0.0203	0.7257	0.5444

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	2.851e-05	1.000e-20
X17_P0	5.675e-05	1.000e-20
X25_P0	7.011e-05	1.000e-20
X33_P0	8.347e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	1.036e-04	2.117e-04	2.123e-04	1.968e-04
B (output stable)	1.171e-04	2.507e-04	2.514e-04	2.179e-04
C (output stable)	3.414e-04	5.561e-04	5.591e-04	5.416e-04
D (output stable)	1.195e-04	1.681e-04	1.688e-04	1.685e-04
A to Z	3.861e-03	7.109e-03	9.048e-03	1.078e-02
B to Z	3.649e-03	6.569e-03	8.504e-03	1.035e-02
C to Z	3.216e-03	5.688e-03	7.516e-03	9.174e-03
D to Z	3.967e-03	7.000e-03	8.725e-03	1.024e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

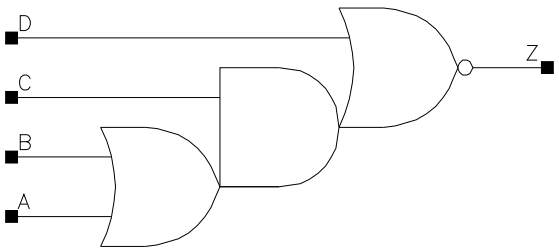
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.952	1.1424
X11_P0	1.200	1.496	1.7952
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X16_P0	X21_P0
A	0.0009	0.0016	0.0024	0.0032
B	0.0008	0.0015	0.0024	0.0031
C	0.0008	0.0015	0.0023	0.0031
D	0.0011	0.0016	0.0023	0.0031

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0115	0.0109	2.6700	1.4076
A to Z ↑	0.0225	0.0207	6.2850	3.2961
B to Z ↓	0.0108	0.0105	2.6009	1.3827
B to Z ↑	0.0217	0.0205	6.2997	3.3039
C to Z ↓	0.0105	0.0101	2.4717	1.3058
C to Z ↑	0.0141	0.0129	4.2471	2.1914

D to Z ↓	0.0058	0.0048	1.6404	0.8307
D to Z ↑	0.0136	0.0120	4.5416	2.3500
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0108	0.0112	0.9446	0.7309
A to Z ↑	0.0190	0.0203	2.1031	1.6335
B to Z ↓	0.0101	0.0105	0.9529	0.7339
B to Z ↑	0.0191	0.0198	2.1076	1.6379
C to Z ↓	0.0101	0.0102	0.8945	0.6880
C to Z ↑	0.0122	0.0124	1.4467	1.0870
D to Z ↓	0.0048	0.0049	0.5784	0.4416
D to Z ↑	0.0111	0.0111	1.5357	1.1658

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.508e-05	1.000e-20
X11_P0	2.878e-05	1.000e-20
X16_P0	4.162e-05	1.000e-20
X21_P0	5.437e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	3.835e-05	6.911e-05	9.174e-05	1.487e-04
B (output stable)	4.863e-05	8.531e-05	1.184e-04	1.886e-04
C (output stable)	1.120e-04	2.267e-04	3.113e-04	4.386e-04
D (output stable)	3.439e-04	7.260e-04	1.036e-03	1.452e-03
A to Z	2.630e-03	4.610e-03	6.437e-03	8.998e-03
B to Z	2.202e-03	3.925e-03	5.638e-03	7.594e-03
C to Z	1.953e-03	3.416e-03	4.859e-03	6.632e-03
D to Z	1.452e-03	2.579e-03	3.583e-03	4.760e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

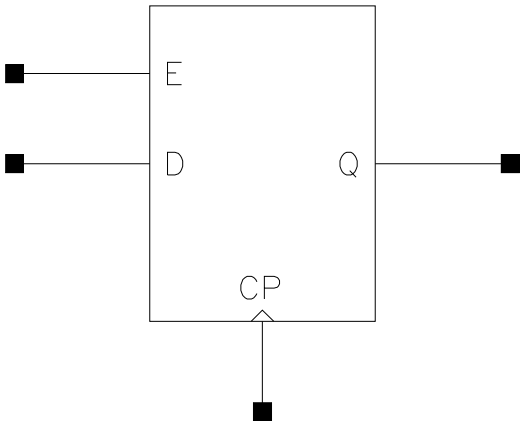
Pin Cycle (vdds)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.128	3.7536
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0011	0.0011	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0285	0.0326	1.5551	0.8003
CP to Q ↑	0.0358	0.0382	2.2324	1.1178
	X33_P0		**X33_P0**	
CP to Q ↓	0.0486		0.3995	
CP to Q ↑	0.0598		0.5539	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0387	0.0387	0.0387
CP ↑	min_pulse_width to CP	0.0237	0.0283	0.0224
D ↓	hold_rising to CP	-0.0071	-0.0071	-0.0071
D ↑	hold_rising to CP	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0366	0.0366	0.0366
D ↑	setup_rising to CP	0.0239	0.0239	0.0239
E ↓	hold_rising to CP	-0.0018	-0.0018	-0.0018
E ↑	hold_rising to CP	0.0036	0.0036	0.0036
E ↓	setup_rising to CP	0.0414	0.0414	0.0414
E ↑	setup_rising to CP	0.0390	0.0390	0.0390

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	5.075e-05	1.000e-20
X17_P0	6.140e-05	1.000e-20
X33_P0	9.733e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

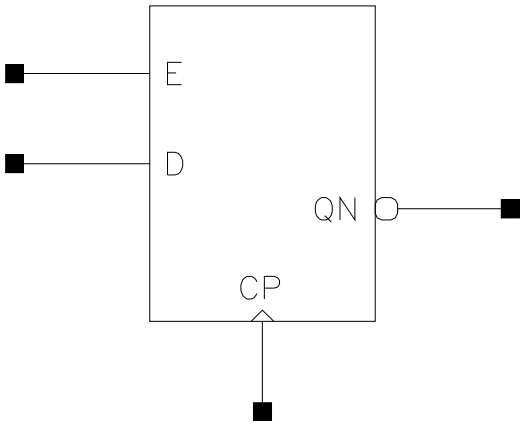
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	8.157e-03	8.158e-03	8.167e-03
Clock 100Mhz Data 25Mhz	1.070e-02	1.161e-02	1.427e-02
Clock 100Mhz Data 50Mhz	1.325e-02	1.507e-02	2.038e-02
Clock = 0 Data 100Mhz	5.141e-03	5.140e-03	5.140e-03
Clock = 1 Data 100Mhz	1.474e-03	1.474e-03	1.474e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.264	3.9168
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0008	0.0011	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0489	0.0463	1.6054	0.7704
CP to QN ↑	0.0383	0.0389	2.2702	1.0841
	X33_P0		**X33_P0**	
CP to QN ↓	0.0495		0.4010	
CP to QN ↑	0.0426		0.5569	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0387	0.0387	0.0387
CP ↑	min_pulse_width to CP	0.0224	0.0224	0.0271
D ↓	hold_rising to CP	-0.0071	-0.0071	-0.0071
D ↑	hold_rising to CP	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0366	0.0366	0.0366
D ↑	setup_rising to CP	0.0239	0.0239	0.0239
E ↓	hold_rising to CP	-0.0018	-0.0018	-0.0018
E ↑	hold_rising to CP	0.0036	0.0036	0.0036
E ↓	setup_rising to CP	0.0414	0.0414	0.0414
E ↑	setup_rising to CP	0.0396	0.0390	0.0390

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	5.034e-05	1.000e-20
X17_P0	7.056e-05	1.000e-20
X33_P0	9.453e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

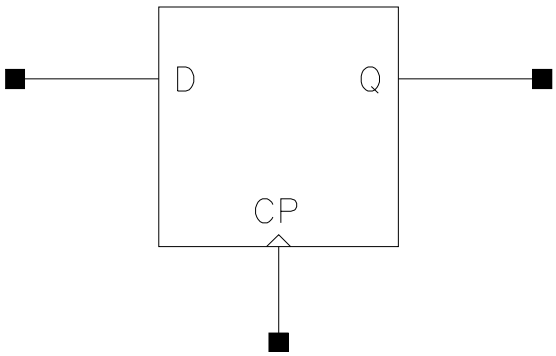
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	8.157e-03	8.158e-03	8.159e-03
Clock 100Mhz Data 25Mhz	1.073e-02	1.195e-02	1.419e-02
Clock 100Mhz Data 50Mhz	1.329e-02	1.574e-02	2.023e-02
Clock = 0 Data 100Mhz	5.140e-03	5.140e-03	5.141e-03
Clock = 1 Data 100Mhz	1.474e-03	1.474e-03	1.474e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.176	2.6112
X17_P0	1.200	2.448	2.9376
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0298	0.0328	1.5442	0.7939
CP to Q ↑	0.0361	0.0399	2.1515	1.0924
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to Q ↓	0.0408	0.0425	0.4674	0.4239
CP to Q ↑	0.0454	0.0462	0.6174	0.5615

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0339	0.0339	0.0339	0.0339
CP ↑	min_pulse_width to CP	0.0237	0.0271	0.0330	0.0365
D ↓	hold_rising to CP	0.0124	0.0124	0.0124	0.0124
D ↑	hold_rising to CP	0.0123	0.0123	0.0123	0.0123
D ↓	setup_rising to CP	0.0171	0.0171	0.0166	0.0166
D ↑	setup_rising to CP	0.0125	0.0125	0.0125	0.0125

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	3.866e-05	1.000e-20
X17_P0	5.081e-05	1.000e-20
X30_P0	6.896e-05	1.000e-20
X33_P0	7.180e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

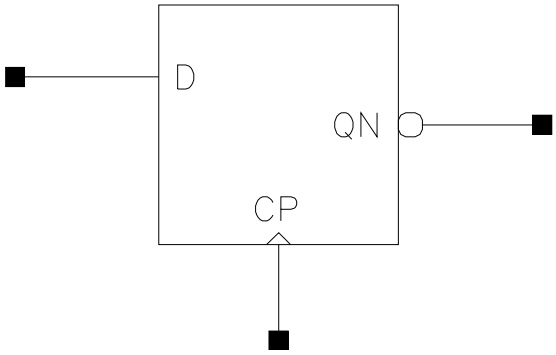
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	8.534e-03	8.576e-03	8.588e-03	8.595e-03
Clock 100Mhz Data 25Mhz	9.817e-03	1.107e-02	1.328e-02	1.381e-02
Clock 100Mhz Data 50Mhz	1.110e-02	1.357e-02	1.798e-02	1.903e-02
Clock = 0 Data 100Mhz	3.389e-03	3.489e-03	3.519e-03	3.534e-03
Clock = 1 Data 100Mhz	2.905e-05	2.908e-05	2.927e-05	2.939e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0290	0.0340	1.5954	0.8175
CP to QN ↑	0.0305	0.0325	2.1468	1.0962
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to QN ↓	0.0492	0.0494	0.4401	0.3997
CP to QN ↑	0.0401	0.0456	0.5974	0.5565

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0339	0.0339	0.0339	0.0339
CP ↑	min_pulse_width to CP	0.0224	0.0271	0.0237	0.0270
D ↓	hold_rising to CP	0.0146	0.0146	0.0124	0.0124
D ↑	hold_rising to CP	0.0151	0.0151	0.0123	0.0123
D ↓	setup_rising to CP	0.0149	0.0149	0.0171	0.0171
D ↑	setup_rising to CP	0.0120	0.0120	0.0125	0.0125

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	3.680e-05	1.000e-20
X17_P0	4.752e-05	1.000e-20
X30_P0	7.927e-05	1.000e-20
X33_P0	8.245e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

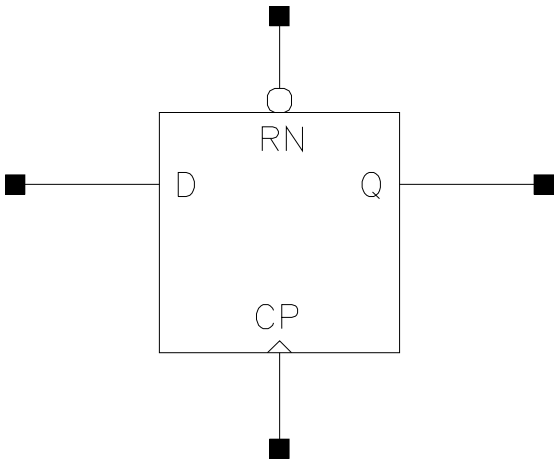
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	8.227e-03	8.230e-03	8.356e-03	8.410e-03
Clock 100Mhz Data 25Mhz	9.389e-03	1.040e-02	1.257e-02	1.329e-02
Clock 100Mhz Data 50Mhz	1.055e-02	1.257e-02	1.678e-02	1.817e-02
Clock = 0 Data 100Mhz	3.035e-03	3.036e-03	3.219e-03	3.262e-03
Clock = 1 Data 100Mhz	2.883e-05	2.905e-05	2.927e-05	2.942e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0342	0.0423	0.8017	0.4742
CP to Q ↑	0.0412	0.0462	1.0986	0.6195
RN to Q ↓	0.0545	0.0710	0.8267	0.4858

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0387	0.0387
CP ↑	min_pulse_width to CP	0.0284	0.0365
D ↓	hold_rising to CP	0.0124	0.0124
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0198	0.0198
D ↑	setup_rising to CP	0.0146	0.0146
RN ↓	min_pulse_width to RN	0.0686	0.0854
RN ↑	recovery_rising to CP	0.0097	0.0097
RN ↑	removal_rising to CP	-0.0028	-0.0028

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P0	5.888e-05	1.000e-20
X30_P0	8.125e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

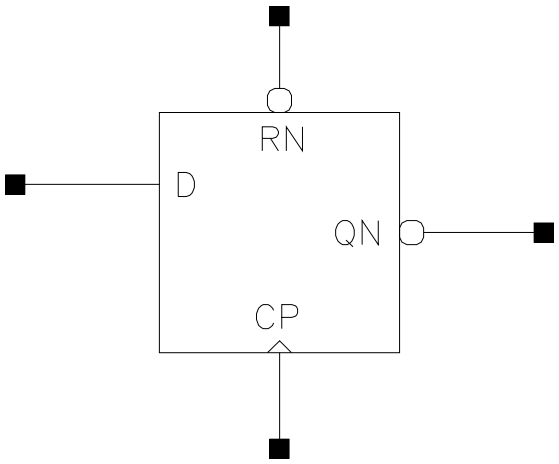
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	9.097e-03	9.094e-03
Clock 100Mhz Data 25Mhz	1.177e-02	1.395e-02
Clock 100Mhz Data 50Mhz	1.445e-02	1.881e-02
Clock = 0 Data 100Mhz	4.145e-03	4.149e-03
Clock = 1 Data 100Mhz	2.962e-05	2.966e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0010	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0475	0.0512	0.7663	0.4413
CP to QN ↑	0.0388	0.0418	1.0724	0.6004
RN to QN ↑	0.0559	0.0599	1.0770	0.6014

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0387	0.0386
CP ↑	min_pulse_width to CP	0.0236	0.0271
D ↓	hold_rising to CP	0.0124	0.0124
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0224	0.0224
D ↑	setup_rising to CP	0.0146	0.0146
RN ↓	min_pulse_width to RN	0.0540	0.0588
RN ↑	recovery_rising to CP	0.0097	0.0097
RN ↑	removal_rising to CP	-0.0028	-0.0028

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P0	6.252e-05	1.000e-20
X30_P0	7.594e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

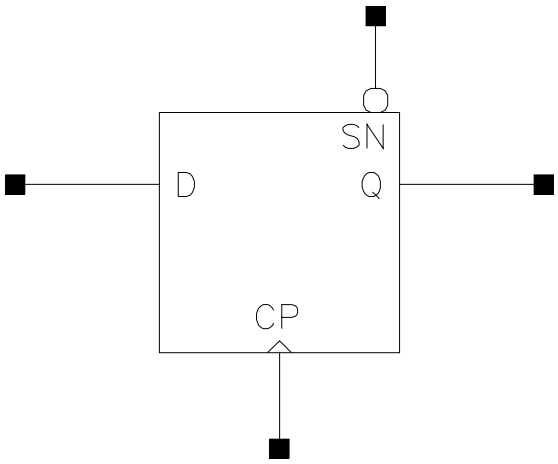
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	9.093e-03	9.083e-03
Clock 100Mhz Data 25Mhz	1.203e-02	1.353e-02
Clock 100Mhz Data 50Mhz	1.497e-02	1.798e-02
Clock = 0 Data 100Mhz	4.196e-03	4.183e-03
Clock = 1 Data 100Mhz	2.959e-05	2.964e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0343	0.0429	0.8018	0.4716
CP to Q ↑	0.0408	0.0461	1.0989	0.6206
SN to Q ↑	0.0419	0.0486	1.0997	0.6202

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0386	0.0386
CP ↑	min_pulse_width to CP	0.0284	0.0365
D ↓	hold_rising to CP	0.0129	0.0129
D ↑	hold_rising to CP	0.0124	0.0124
D ↓	setup_rising to CP	0.0220	0.0220
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0430	0.0479
SN ↑	recovery_rising to CP	0.0032	0.0032
SN ↑	removal_rising to CP	0.0189	0.0189

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P0	5.056e-05	1.000e-20
X30_P0	6.440e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

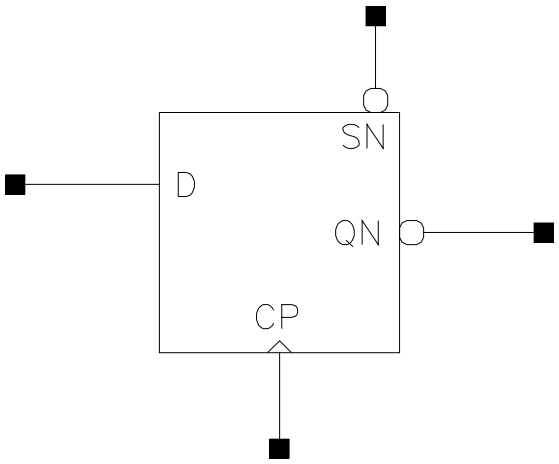
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	9.192e-03	9.173e-03
Clock 100Mhz Data 25Mhz	1.187e-02	1.405e-02
Clock 100Mhz Data 50Mhz	1.454e-02	1.892e-02
Clock = 0 Data 100Mhz	4.111e-03	4.111e-03
Clock = 1 Data 100Mhz	2.984e-05	2.982e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0471	0.0507	0.7681	0.4421
CP to QN ↑	0.0391	0.0420	1.0691	0.5991
SN to QN ↓	0.0476	0.0512	0.7674	0.4421

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0386	0.0386
CP ↑	min_pulse_width to CP	0.0237	0.0271
D ↓	hold_rising to CP	0.0129	0.0129
D ↑	hold_rising to CP	0.0124	0.0124
D ↓	setup_rising to CP	0.0220	0.0220
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0354	0.0354
SN ↑	recovery_rising to CP	0.0032	0.0032
SN ↑	removal_rising to CP	0.0189	0.0189

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P0	6.890e-05	1.000e-20
X30_P0	9.057e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

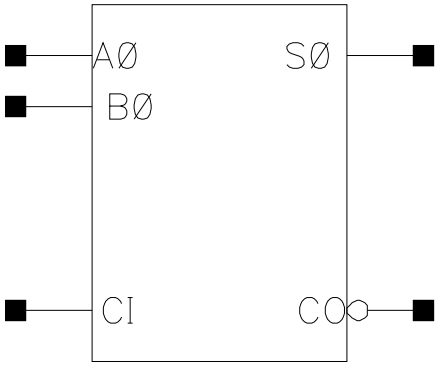
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	9.190e-03	9.184e-03
Clock 100Mhz Data 25Mhz	1.210e-02	1.355e-02
Clock 100Mhz Data 50Mhz	1.501e-02	1.792e-02
Clock = 0 Data 100Mhz	4.112e-03	4.112e-03
Clock = 1 Data 100Mhz	2.971e-05	2.990e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_P0	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_-P0	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_-P0	1.200	3.672	4.4064
C12T28SOI_LLS1_-FA1X33_P0	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0	0.0030	0.0062	0.0028	0.0055
B0	0.0028	0.0060	0.0030	0.0053
CI	0.0020	0.0045	0.0021	0.0038

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0
A0 to CO ↓	0.0317	0.0345	1.6141	0.4235
A0 to CO ↑	0.0247	0.0259	2.2225	0.5728
A0 to S0 ↓	0.0333	0.0420	1.6005	0.4140
A0 to S0 ↑	0.0342	0.0418	2.1979	0.5667
B0 to CO ↓	0.0313	0.0348	1.6186	0.4252
B0 to CO ↑	0.0254	0.0269	2.2240	0.5705
B0 to S0 ↓	0.0337	0.0429	1.6008	0.4141
B0 to S0 ↑	0.0344	0.0425	2.1995	0.5668
CI to CO ↓	0.0308	0.0346	1.6204	0.4240
CI to CO ↑	0.0253	0.0263	2.2221	0.5726
CI to S0 ↓	0.0334	0.0424	1.6010	0.4141
CI to S0 ↑	0.0346	0.0428	2.1990	0.5666
	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0 to CO ↓	0.0214	0.0261	3.1187	0.5371
A0 to CO ↑	0.0191	0.0217	2.2727	0.5654
A0 to S0 ↓	0.0447	0.0548	1.7349	0.4341
A0 to S0 ↑	0.0411	0.0444	2.2889	0.5773
B0 to CO ↓	0.0223	0.0271	3.1200	0.5378
B0 to CO ↑	0.0177	0.0207	2.2709	0.5658
B0 to S0 ↓	0.0448	0.0561	1.7350	0.4341
B0 to S0 ↑	0.0412	0.0456	2.2886	0.5774
CI to CO ↓	0.0221	0.0377	3.1139	0.5431
CI to CO ↑	0.0195	0.0236	2.3376	0.5702
CI to S0 ↓	0.0265	0.0341	1.7377	0.4346
CI to S0 ↑	0.0224	0.0227	2.2885	0.5775

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_FA1X8_P0	5.832e-05	1.000e-20
C12T28SOI_LL_FA1X33_P0	1.612e-04	1.000e-20
C12T28SOI_LLS1_FA1X8_P0	1.325e-04	1.000e-20
C12T28SOI_LLS1_FA1X33_P0	2.700e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0 to CO	4.011e-03	1.202e-02	6.184e-03	1.556e-02
A0 to S0	4.040e-03	1.249e-02	8.301e-03	1.927e-02
B0 to CO	4.053e-03	1.224e-02	6.218e-03	1.571e-02
B0 to S0	4.023e-03	1.251e-02	8.404e-03	1.957e-02
CI to CO	4.131e-03	1.247e-02	4.455e-03	1.422e-02
CI to S0	4.021e-03	1.251e-02	5.044e-03	1.529e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00

A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X33_P0	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X33_P0
A0	0.0011	0.0031
B0	0.0009	0.0027

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
A0 to CO ↓	0.0248	0.0227	1.6044	0.3998
A0 to CO ↑	0.0227	0.0210	2.1926	0.5677
A0 to S0 ↓	0.0313	0.0299	1.5724	0.3992
A0 to S0 ↑	0.0304	0.0343	2.1646	0.5594
B0 to CO ↓	0.0241	0.0208	1.6038	0.3961
B0 to CO ↑	0.0245	0.0222	2.1928	0.5675
B0 to S0 ↓	0.0327	0.0303	1.5718	0.3992
B0 to S0 ↑	0.0298	0.0328	2.1623	0.5594

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	3.655e-05	1.000e-20
X33_P0	1.716e-04	1.000e-20

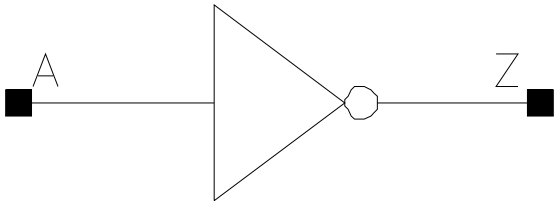
Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X33_P0
A0 to CO	3.083e-03	1.041e-02
A0 to S0	2.895e-03	1.036e-02
B0 to CO	3.137e-03	1.066e-02
B0 to S0	2.874e-03	1.016e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X8_P0	X33_P0
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.272	0.3264
X6_P0	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X13_P0	1.200	0.408	0.4896
X17_P0	1.200	0.408	0.4896
X21_P0	1.200	0.544	0.6528
X25_P0	1.200	0.544	0.6528
X29_P0	1.200	0.680	0.8160
X33_P0	1.200	0.680	0.8160
X50_P0	1.200	0.952	1.1424
X58_P0	1.200	1.088	1.3056
X67_P0	1.200	1.224	1.4688
X75_P0	1.200	1.360	1.6320
X84_P0	1.200	1.496	1.7952
X100_P0	1.200	1.768	2.1216
X134_P0	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0006	0.0007	0.0008	0.0013
	X17_P0	X21_P0	X25_P0	X29_P0
A	0.0016	0.0021	0.0024	0.0028
	X33_P0	X50_P0	X58_P0	X67_P0
A	0.0032	0.0048	0.0056	0.0064
	X75_P0	X84_P0	X100_P0	X134_P0

A	0.0074	0.0084	0.0102	0.0141

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0051	0.0048	3.0564	2.3409
A to Z ↑	0.0094	0.0084	4.3188	3.2605
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0044	0.0036	1.6114	1.0427
A to Z ↑	0.0076	0.0069	2.2483	1.4895
	X17_P0	**X21_P0**	**X17_P0**	**X21_P0**
A to Z ↓	0.0037	0.0040	0.8004	0.6447
A to Z ↑	0.0065	0.0069	1.1093	0.8955
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0040	0.0038	0.5490	0.4647
A to Z ↑	0.0066	0.0064	0.7471	0.6393
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0038	0.0039	0.4126	0.2788
A to Z ↑	0.0062	0.0061	0.5601	0.3754
	X58_P0	**X67_P0**	**X58_P0**	**X67_P0**
A to Z ↓	0.0042	0.0042	0.2419	0.2126
A to Z ↑	0.0064	0.0063	0.3238	0.2839
	X75_P0	**X84_P0**	**X75_P0**	**X84_P0**
A to Z ↓	0.0046	0.0048	0.1923	0.1740
A to Z ↑	0.0067	0.0068	0.2550	0.2313
	X100_P0	**X134_P0**	**X100_P0**	**X134_P0**
A to Z ↓	0.0055	0.0062	0.1485	0.1162
A to Z ↑	0.0075	0.0082	0.1954	0.1513

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	4.116e-06	1.000e-20
X6_P0	6.514e-06	1.000e-20
X8_P0	1.121e-05	1.000e-20
X13_P0	1.543e-05	1.000e-20
X17_P0	2.339e-05	1.000e-20
X21_P0	2.704e-05	1.000e-20
X25_P0	3.390e-05	1.000e-20
X29_P0	3.878e-05	1.000e-20
X33_P0	4.435e-05	1.000e-20
X50_P0	6.524e-05	1.000e-20
X58_P0	7.570e-05	1.000e-20
X67_P0	8.615e-05	1.000e-20
X75_P0	9.661e-05	1.000e-20
X84_P0	1.071e-04	1.000e-20
X100_P0	1.280e-04	1.000e-20
X134_P0	1.698e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0

A to Z	6.758e-04	8.577e-04	1.183e-03	1.708e-03
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	2.225e-03	2.891e-03	3.366e-03	3.858e-03
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	4.287e-03	6.361e-03	7.568e-03	8.498e-03
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	9.772e-03	1.081e-02	1.330e-02	1.839e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

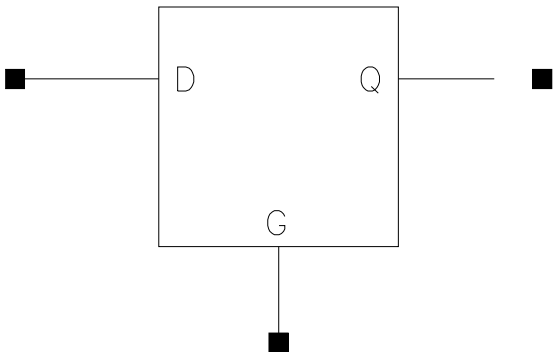
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X23_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P0	X23_P0
D	0.0005	0.0013
G	0.0011	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X23_P0	X8_P0	X23_P0
D to Q ↓	0.0360	0.0282	1.6058	0.7647
D to Q ↑	0.0243	0.0242	2.1595	0.5774
G to Q ↓	0.0369	0.0301	1.6005	0.7634
G to Q ↑	0.0236	0.0216	2.1618	0.5781

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X23_P0
D ↓	hold_falling to G	0.0004	0.0048
D ↑	hold_falling to G	0.0068	0.0068
D ↓	setup_falling to G	0.0370	0.0248
D ↑	setup_falling to G	0.0285	0.0304
G ↑	min_pulse_width to G	0.0317	0.0351

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	2.228e-05	1.000e-20
X23_P0	6.681e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X23_P0
D (output stable)	2.083e-05	8.428e-05
G (output stable)	1.126e-03	2.277e-03
D to Q	5.085e-03	9.937e-03
G to Q	4.865e-03	9.262e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

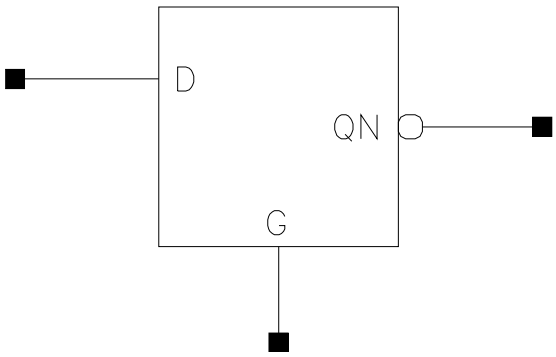
Pin Cycle (vdds)	X8_P0	X23_P0
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P0
D	0.0006
G	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P0	X17_P0
D to QN ↓	0.0312	0.7678
D to QN ↑	0.0397	1.0625
G to QN ↓	0.0301	0.7683
G to QN ↑	0.0394	1.0619

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P0
D ↓	hold_falling to G	-0.0013
D ↑	hold_falling to G	0.0036
D ↓	setup_falling to G	0.0295
D ↑	setup_falling to G	0.0235
G ↑	min_pulse_width to G	0.0269

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P0	3.926e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X17_P0
D (output stable)	2.113e-05
G (output stable)	1.372e-03
D to QN	6.180e-03
G to QN	6.003e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

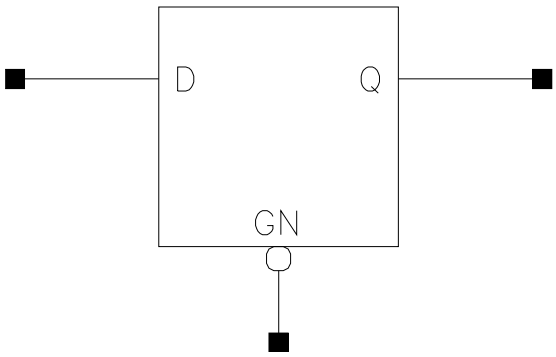
Pin Cycle (vdds)	X17_P0
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
D	0.0005	0.0008	0.0017
GN	0.0011	0.0014	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D to Q ↓	0.0364	0.0314	1.6081	0.7965
D to Q ↑	0.0247	0.0234	2.1589	1.1114
GN to Q ↓	0.0334	0.0282	1.6119	0.7989
GN to Q ↑	0.0354	0.0342	2.1574	1.1086

	X33_P0		X33_P0	
D to Q ↓	0.0305		0.4089	
D to Q ↑	0.0201		0.5580	
GN to Q ↓	0.0267		0.4096	
GN to Q ↑	0.0265		0.5564	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X33_P0
D ↓	hold_rising to GN	-0.0025	0.0023	0.0019
D ↑	hold_rising to GN	0.0107	0.0106	0.0128
D ↓	setup_rising to GN	0.0396	0.0348	0.0352
D ↑	setup_rising to GN	0.0245	0.0216	0.0191
GN ↓	min_pulse_width to GN	0.0463	0.0389	0.0360

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	2.298e-05	1.000e-20
X17_P0	4.114e-05	1.000e-20
X33_P0	7.509e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
D (output stable)	2.063e-05	3.368e-05	9.205e-05
GN (output stable)	1.120e-03	1.532e-03	2.059e-03
D to Q	5.115e-03	7.341e-03	1.192e-02
GN to Q	7.132e-03	9.857e-03	1.476e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

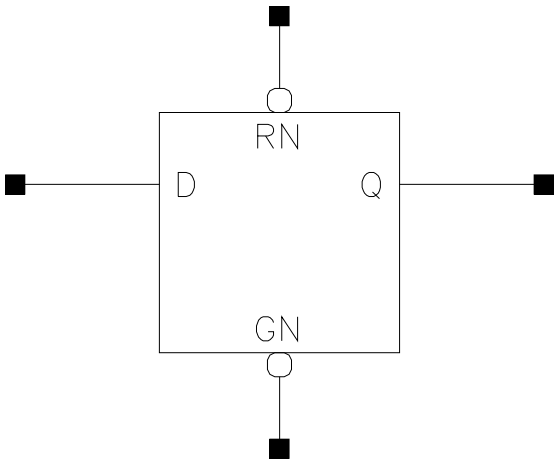
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.496	1.7952
X33_P0	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X33_P0
D	0.0006	0.0013
GN	0.0012	0.0023
RN	0.0005	0.0006

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
D to Q ↓	0.0341	0.0307	1.5746	0.4108
D to Q ↑	0.0317	0.0410	2.2026	0.5741

GN to Q ↓	0.0314	0.0286	1.5775	0.4114
GN to Q ↑	0.0402	0.0424	2.2000	0.5738
RN to Q ↓	0.0285	0.0524	1.5361	0.4358
RN to Q ↑	0.0325	0.0452	2.2007	0.5745

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X33_P0
D ↓	hold_rising to GN	0.0002	0.0019
D ↑	hold_rising to GN	0.0036	-0.0093
D ↓	setup_rising to GN	0.0348	0.0327
D ↑	setup_rising to GN	0.0314	0.0458
GN ↓	min_pulse_width to GN	0.0419	0.0450
RN ↓	min_pulse_width to RN	0.0327	0.0615
RN ↑	recovery_rising to GN	0.0346	0.0481
RN ↑	removal_rising to GN	-0.0195	-0.0310

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	2.871e-05	1.000e-20
X33_P0	8.198e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X33_P0
D (output stable)	9.260e-05	1.584e-04
GN (output stable)	1.297e-03	2.084e-03
RN (output stable)	4.260e-05	7.199e-05
D to Q	5.120e-03	1.405e-02
GN to Q	7.297e-03	1.742e-02
RN to Q	3.863e-03	1.143e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

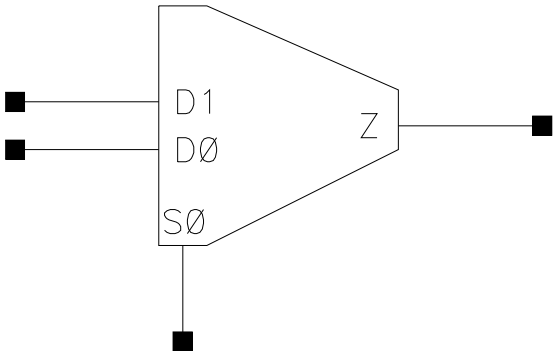
Pin Cycle (vdds)	X8_P0	X33_P0
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
D0	0.0007	0.0011	0.0014	0.0019
D1	0.0007	0.0010	0.0014	0.0019
S0	0.0013	0.0014	0.0016	0.0024

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D0 to Z ↓	0.0286	0.0253	1.5985	0.7839
D0 to Z ↑	0.0230	0.0212	2.2235	1.0875
D1 to Z ↓	0.0270	0.0248	1.5925	0.7824
D1 to Z ↑	0.0210	0.0200	2.2187	1.0864
S0 to Z ↓	0.0248	0.0239	1.5885	0.7803
S0 to Z ↑	0.0234	0.0235	2.2192	1.0867

	X25_P0	X33_P0	X25_P0	X33_P0
D0 to Z ↓	0.0272	0.0244	0.5390	0.4044
D0 to Z ↑	0.0225	0.0210	0.7318	0.5487
D1 to Z ↓	0.0290	0.0253	0.5404	0.4053
D1 to Z ↑	0.0218	0.0204	0.7313	0.5488
S0 to Z ↓	0.0276	0.0253	0.5378	0.4039
S0 to Z ↑	0.0261	0.0239	0.7310	0.5479

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	2.729e-05	1.000e-20
X17_P0	5.997e-05	1.000e-20
X25_P0	7.352e-05	1.000e-20
X33_P0	1.201e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	1.057e-03	1.688e-03	1.933e-03	2.791e-03
D1 (output stable)	9.145e-04	1.623e-03	2.074e-03	2.867e-03
S0 (output stable)	1.284e-03	1.437e-03	1.840e-03	2.354e-03
D0 to Z	3.488e-03	5.893e-03	9.081e-03	1.150e-02
D1 to Z	3.226e-03	5.717e-03	9.171e-03	1.142e-02
S0 to Z	4.013e-03	6.220e-03	1.008e-02	1.241e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

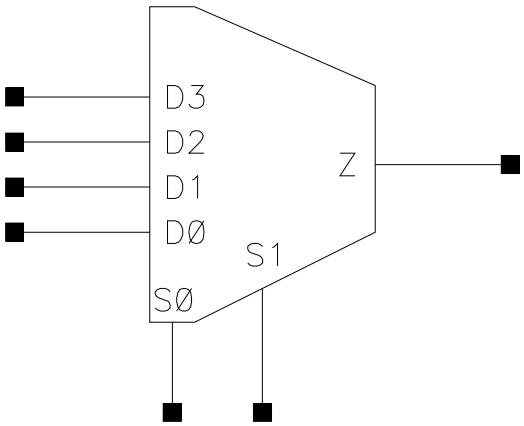
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.312	2.7744
X31_P0	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P0	X31_P0
D0	0.0005	0.0015
D1	0.0006	0.0014
D2	0.0005	0.0015
D3	0.0006	0.0014
S0	0.0019	0.0036
S1	0.0011	0.0023

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X31_P0	X8_P0	X31_P0

D0 to Z ↓	0.0471	0.0483	1.6522	0.4590
D0 to Z ↑	0.0325	0.0349	2.2333	0.6050
D1 to Z ↓	0.0467	0.0484	1.6510	0.4591
D1 to Z ↑	0.0327	0.0348	2.2333	0.6049
D2 to Z ↓	0.0504	0.0452	1.6599	0.4549
D2 to Z ↑	0.0345	0.0321	2.2400	0.6004
D3 to Z ↓	0.0502	0.0448	1.6598	0.4543
D3 to Z ↑	0.0341	0.0333	2.2395	0.6033
S0 to Z ↓	0.0513	0.0523	1.6528	0.4561
S0 to Z ↑	0.0394	0.0418	2.2376	0.6038
S1 to Z ↓	0.0377	0.0375	1.6550	0.4562
S1 to Z ↑	0.0312	0.0330	2.2361	0.6034

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	2.554e-05	1.000e-20
X31_P0	9.236e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X31_P0
D0 (output stable)	3.425e-05	1.807e-04
D1 (output stable)	3.451e-05	1.709e-04
D2 (output stable)	3.958e-05	1.731e-04
D3 (output stable)	3.753e-05	1.791e-04
S0 (output stable)	1.782e-03	3.960e-03
S1 (output stable)	1.587e-03	3.550e-03
D0 to Z	3.840e-03	1.355e-02
D1 to Z	3.824e-03	1.361e-02
D2 to Z	4.102e-03	1.264e-02
D3 to Z	4.089e-03	1.268e-02
S0 to Z	5.782e-03	1.740e-02
S1 to Z	4.679e-03	1.412e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

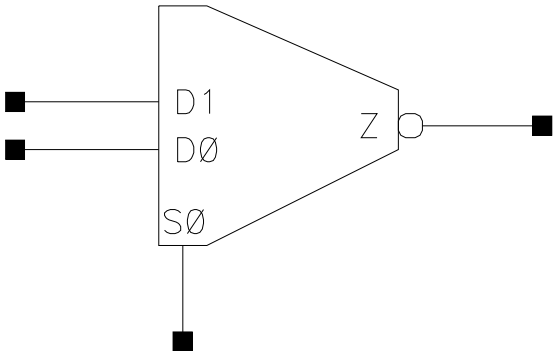
Pin Cycle (vdds)	X8_P0	X31_P0
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.816	0.9792
X5_P0	1.200	0.952	1.1424
X10_P0	1.200	1.768	2.1216
X16_P0	1.200	2.448	2.9376
X21_P0	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P0	X5_P0	X10_P0	X16_P0
D0	0.0005	0.0008	0.0016	0.0025
D1	0.0005	0.0008	0.0016	0.0024
S0	0.0011	0.0019	0.0025	0.0037
	X21_P0			
D0	0.0032			
D1	0.0032			
S0	0.0042			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X5_P0	X3_P0	X5_P0
D0 to Z ↓	0.0101	0.0101	5.0127	3.1577

D0 to Z ↑	0.0166	0.0146	9.0669	4.6705
D1 to Z ↓	0.0099	0.0099	4.9804	2.9849
D1 to Z ↑	0.0171	0.0150	9.0822	4.8832
S0 to Z ↓	0.0151	0.0127	4.9763	3.0620
S0 to Z ↑	0.0163	0.0136	9.0424	4.7580
	X10_P0	**X16_P0**	**X10_P0**	**X16_P0**
D0 to Z ↓	0.0114	0.0106	1.4930	0.9763
D0 to Z ↑	0.0158	0.0149	2.1873	1.4457
D1 to Z ↓	0.0105	0.0103	1.4393	0.9491
D1 to Z ↑	0.0157	0.0152	2.2289	1.4633
S0 to Z ↓	0.0155	0.0134	1.4610	0.9598
S0 to Z ↑	0.0163	0.0140	2.2014	1.4507
	X21_P0		**X21_P0**	
D0 to Z ↓	0.0106		0.7476	
D0 to Z ↑	0.0146		1.0977	
D1 to Z ↓	0.0104		0.7214	
D1 to Z ↑	0.0152		1.0921	
S0 to Z ↓	0.0141		0.7323	
S0 to Z ↑	0.0144		1.0911	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	8.130e-06	1.000e-20
X5_P0	2.453e-05	1.000e-20
X10_P0	4.420e-05	1.000e-20
X16_P0	7.048e-05	1.000e-20
X21_P0	8.603e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	2.068e-05	4.603e-05	1.331e-04	2.068e-04
D1 (output stable)	2.063e-05	4.848e-05	1.131e-04	1.967e-04
S0 (output stable)	1.132e-03	1.829e-03	2.909e-03	4.763e-03
D0 to Z	1.002e-03	1.701e-03	4.157e-03	5.864e-03
D1 to Z	1.004e-03	1.684e-03	3.978e-03	5.798e-03
S0 to Z	1.903e-03	3.001e-03	5.799e-03	8.583e-03
	X21_P0			
D0 (output stable)	2.661e-04			
D1 (output stable)	2.654e-04			
S0 (output stable)	5.252e-03			
D0 to Z	7.583e-03			
D1 to Z	7.652e-03			
S0 to Z	1.038e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

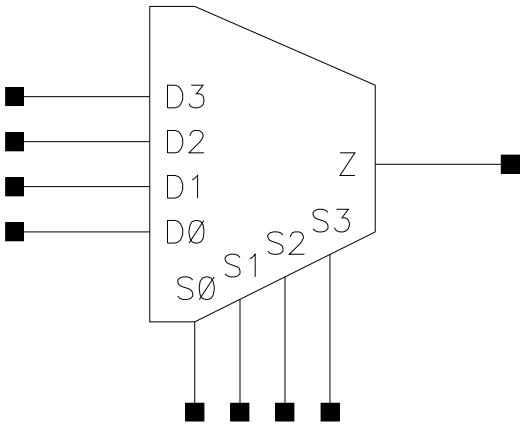
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P0			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	1.768	2.1216
X27_P0	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P0	X27_P0
D0	0.0006	0.0019
D1	0.0007	0.0020
D2	0.0006	0.0019
D3	0.0007	0.0020
S0	0.0007	0.0018
S1	0.0007	0.0018
S2	0.0007	0.0018
S3	0.0007	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	X27_P0	X7_P0	X27_P0
D0 to Z ↓	0.0370	0.0304	2.5832	0.7116
D0 to Z ↑	0.0272	0.0233	2.1769	0.5453
D1 to Z ↓	0.0344	0.0285	2.5813	0.7113
D1 to Z ↑	0.0245	0.0203	2.1673	0.5426
D2 to Z ↓	0.0375	0.0294	2.5873	0.7114
D2 to Z ↑	0.0268	0.0221	2.1841	0.5473
D3 to Z ↓	0.0349	0.0275	2.5823	0.7107
D3 to Z ↑	0.0241	0.0192	2.1739	0.5441
S0 to Z ↓	0.0358	0.0288	2.5827	0.7114
S0 to Z ↑	0.0292	0.0247	2.1752	0.5448
S1 to Z ↓	0.0334	0.0268	2.5811	0.7111
S1 to Z ↑	0.0262	0.0214	2.1672	0.5427
S2 to Z ↓	0.0362	0.0277	2.5856	0.7111
S2 to Z ↑	0.0288	0.0235	2.1830	0.5466
S3 to Z ↓	0.0340	0.0259	2.5823	0.7102
S3 to Z ↑	0.0259	0.0203	2.1750	0.5445

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X7_P0	2.530e-05	1.000e-20
X27_P0	1.197e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X7_P0	X27_P0
D0 (output stable)	5.171e-04	1.637e-03
D1 (output stable)	4.574e-04	1.420e-03
D2 (output stable)	4.864e-04	1.573e-03
D3 (output stable)	4.268e-04	1.356e-03
S0 (output stable)	5.078e-04	1.595e-03
S1 (output stable)	4.461e-04	1.392e-03
S2 (output stable)	4.774e-04	1.533e-03
S3 (output stable)	4.155e-04	1.331e-03
D0 to Z	4.163e-03	1.288e-02
D1 to Z	3.732e-03	1.139e-02
D2 to Z	4.083e-03	1.164e-02
D3 to Z	3.661e-03	1.016e-02
S0 to Z	4.076e-03	1.236e-02
S1 to Z	3.648e-03	1.091e-02
S2 to Z	3.994e-03	1.109e-02
S3 to Z	3.576e-03	9.692e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

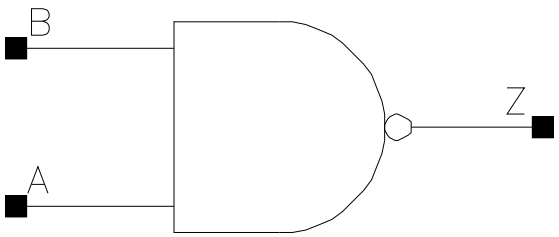
Pin Cycle (vdds)	X7_P0	X27_P0
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P0	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P0	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P0	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P0	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P0	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P0	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P0	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P0	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P0	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P0	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P0	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P0	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P0	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P0	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P0	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P0	C12T28SOI_LL_-NAND2X5_P0	C12T28SOI_LL_-NAND2X7_P0	C12T28SOI_LL_-NAND2X10_P0
A	0.0005	0.0007	0.0008	0.0013
B	0.0006	0.0007	0.0008	0.0012
	C12T28SOI_LL_-NAND2X13_P0	C12T28SOI_LL_-NAND2X17_P0	C12T28SOI_LL_-NAND2X20_P0	C12T28SOI_LL_-NAND2X24_P0
A	0.0016	0.0021	0.0024	0.0029
B	0.0015	0.0020	0.0023	0.0027
	C12T28SOI_LL_-NAND2X27_P0	C12T28SOI_LL_-NAND2X42_P0	C12T28SOI_LL_-NAND2X47_P0	C12T28SOI_LL_-NAND2X50_P0
A	0.0033	0.0010	0.0010	0.0010
B	0.0030	0.0010	0.0010	0.0010
	C12T28SOI_LL_-NAND2X58_P0	C12T28SOI_LL_-NAND2X67_P0	C12T28SOI_-LLBR0D8_-NAND2X7_P0	C12T28SOI_-LLBR0D8_-NAND2X14_P0
A	0.0010	0.0010	0.0008	0.0016
B	0.0010	0.0010	0.0008	0.0015
	C12T28SOI_LLS_-NAND2X40_P0	C12T28SOI_LLS_-NAND2X54_P0		
A	0.0049	0.0064		
B	0.0045	0.0061		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P0	**C12T28SOI_LL_-NAND2X5_P0**	**C12T28SOI_LL_-NAND2X3_P0**	**C12T28SOI_LL_-NAND2X5_P0**
A to Z ↓	0.0076	0.0070	4.9111	3.1930
A to Z ↑	0.0111	0.0099	4.3546	2.7900
B to Z ↓	0.0084	0.0075	4.9738	3.2299
B to Z ↑	0.0100	0.0086	4.3898	2.8102
	C12T28SOI_LL_-NAND2X7_P0	**C12T28SOI_LL_-NAND2X10_P0**	**C12T28SOI_LL_-NAND2X7_P0**	**C12T28SOI_LL_-NAND2X10_P0**
A to Z ↓	0.0070	0.0077	2.6813	1.7787
A to Z ↑	0.0095	0.0103	2.2430	1.4774
B to Z ↓	0.0075	0.0074	2.7070	1.7979
B to Z ↑	0.0081	0.0081	2.2648	1.4898
	C12T28SOI_LL_-NAND2X13_P0	**C12T28SOI_LL_-NAND2X17_P0**	**C12T28SOI_LL_-NAND2X13_P0**	**C12T28SOI_LL_-NAND2X17_P0**
A to Z ↓	0.0075	0.0074	1.3764	1.0917

A to Z ↑	0.0096	0.0097	1.1066	0.8941
B to Z ↓	0.0073	0.0076	1.3906	1.1029
B to Z ↑	0.0074	0.0079	1.1163	0.9011
	C12T28SOI_LL_-NAND2X20_P0	**C12T28SOI_LL_-NAND2X24_P0**	**C12T28SOI_LL_-NAND2X20_P0**	**C12T28SOI_LL_-NAND2X24_P0**
A to Z ↓	0.0073	0.0075	0.9407	0.7986
A to Z ↑	0.0093	0.0095	0.7461	0.6382
B to Z ↓	0.0077	0.0074	0.9507	0.8068
B to Z ↑	0.0076	0.0075	0.7534	0.6433
	C12T28SOI_LL_-NAND2X27_P0	**C12T28SOI_LL_-NAND2X42_P0**	**C12T28SOI_LL_-NAND2X27_P0**	**C12T28SOI_LL_-NAND2X42_P0**
A to Z ↓	0.0074	0.0266	0.7151	0.3228
A to Z ↑	0.0092	0.0270	0.5600	0.4331
B to Z ↓	0.0073	0.0276	0.7228	0.3227
B to Z ↑	0.0071	0.0259	0.5648	0.4333
	C12T28SOI_LL_-NAND2X47_P0	**C12T28SOI_LL_-NAND2X50_P0**	**C12T28SOI_LL_-NAND2X47_P0**	**C12T28SOI_LL_-NAND2X50_P0**
A to Z ↓	0.0272	0.0274	0.2861	0.2689
A to Z ↑	0.0274	0.0276	0.3775	0.3622
B to Z ↓	0.0282	0.0285	0.2862	0.2690
B to Z ↑	0.0263	0.0265	0.3777	0.3620
	C12T28SOI_LL_-NAND2X58_P0	**C12T28SOI_LL_-NAND2X67_P0**	**C12T28SOI_LL_-NAND2X58_P0**	**C12T28SOI_LL_-NAND2X67_P0**
A to Z ↓	0.0287	0.0298	0.2331	0.2047
A to Z ↑	0.0285	0.0294	0.3116	0.2740
B to Z ↓	0.0297	0.0309	0.2332	0.2046
B to Z ↑	0.0275	0.0284	0.3114	0.2739
	C12T28SOI_-LLBR0D8_-NAND2X7_P0	**C12T28SOI_-LLBR0D8_-NAND2X14_P0**	**C12T28SOI_-LLBR0D8_-NAND2X7_P0**	**C12T28SOI_-LLBR0D8_-NAND2X14_P0**
A to Z ↓	0.0050	0.0057	2.0386	1.0793
A to Z ↑	0.0121	0.0123	2.9593	1.4508
B to Z ↓	0.0050	0.0047	2.0708	1.0980
B to Z ↑	0.0103	0.0092	3.0681	1.4824
	C12T28SOI_LLS_-NAND2X40_P0	**C12T28SOI_LLS_-NAND2X54_P0**	**C12T28SOI_LLS_-NAND2X40_P0**	**C12T28SOI_LLS_-NAND2X54_P0**
A to Z ↓	0.0074	0.0075	0.4850	0.3671
A to Z ↑	0.0091	0.0092	0.3759	0.2836
B to Z ↓	0.0074	0.0076	0.4905	0.3715
B to Z ↑	0.0070	0.0072	0.3792	0.2864

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P0	4.006e-06	1.000e-20
C12T28SOI_LL_NAND2X5_P0	8.551e-06	1.000e-20
C12T28SOI_LL_NAND2X7_P0	1.144e-05	1.000e-20
C12T28SOI_LL_NAND2X10_P0	1.497e-05	1.000e-20
C12T28SOI_LL_NAND2X13_P0	2.286e-05	1.000e-20
C12T28SOI_LL_NAND2X17_P0	2.648e-05	1.000e-20
C12T28SOI_LL_NAND2X20_P0	3.331e-05	1.000e-20
C12T28SOI_LL_NAND2X24_P0	3.811e-05	1.000e-20
C12T28SOI_LL_NAND2X27_P0	4.378e-05	1.000e-20

C12T28SOI_LL_NAND2X42_P0	7.719e-05	1.000e-20
C12T28SOI_LL_NAND2X47_P0	8.434e-05	1.000e-20
C12T28SOI_LL_NAND2X50_P0	8.378e-05	1.000e-20
C12T28SOI_LL_NAND2X58_P0	9.036e-05	1.000e-20
C12T28SOI_LL_NAND2X67_P0	9.695e-05	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_P0	8.549e-06	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_-P0	1.681e-05	1.000e-20
C12T28SOI_LLS_NAND2X40_P0	6.473e-05	1.000e-20
C12T28SOI_LLS_NAND2X54_P0	8.568e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND2X3_P0	C12T28SOI_LL_-NAND2X5_P0	C12T28SOI_LL_-NAND2X7_P0	C12T28SOI_LL_-NAND2X10_P0
A (output stable)	1.661e-05	2.612e-05	3.085e-05	9.824e-05
B (output stable)	3.006e-05	4.497e-05	5.469e-05	3.264e-04
A to Z	8.164e-04	1.161e-03	1.404e-03	2.301e-03
B to Z	7.265e-04	1.025e-03	1.232e-03	1.855e-03
	C12T28SOI_LL_-NAND2X13_P0	C12T28SOI_LL_-NAND2X17_P0	C12T28SOI_LL_-NAND2X20_P0	C12T28SOI_LL_-NAND2X24_P0
A (output stable)	1.166e-04	1.390e-04	1.549e-04	2.154e-04
B (output stable)	3.780e-04	3.870e-04	4.191e-04	6.283e-04
A to Z	2.910e-03	3.624e-03	4.209e-03	5.057e-03
B to Z	2.386e-03	3.062e-03	3.572e-03	4.165e-03
	C12T28SOI_LL_-NAND2X27_P0	C12T28SOI_LL_-NAND2X42_P0	C12T28SOI_LL_-NAND2X47_P0	C12T28SOI_LL_-NAND2X50_P0
A (output stable)	2.324e-04	3.383e-05	3.395e-05	3.395e-05
B (output stable)	6.676e-04	6.449e-05	6.479e-05	6.459e-05
A to Z	5.574e-03	1.182e-02	1.281e-02	1.318e-02
B to Z	4.567e-03	1.167e-02	1.266e-02	1.303e-02
	C12T28SOI_LL_-NAND2X58_P0	C12T28SOI_LL_-NAND2X67_P0	C12T28SOI_-LLBR0D8_-NAND2X7_P0	C12T28SOI_-LLBR0D8_-NAND2X14_P0
A (output stable)	3.405e-05	3.415e-05	4.035e-05	1.461e-04
B (output stable)	6.479e-05	6.492e-05	7.112e-05	4.711e-04
A to Z	1.513e-02	1.681e-02	1.398e-03	2.907e-03
B to Z	1.498e-02	1.665e-02	1.154e-03	2.173e-03
	C12T28SOI_LLS_-NAND2X40_P0	C12T28SOI_LLS_-NAND2X54_P0		
A (output stable)	3.388e-04	4.281e-04		
B (output stable)	9.276e-04	1.215e-03		
A to Z	8.215e-03	1.094e-02		
B to Z	6.779e-03	9.055e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND2X3_P0	C12T28SOI_LL_-NAND2X5_P0	C12T28SOI_LL_-NAND2X7_P0	C12T28SOI_LL_-NAND2X10_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

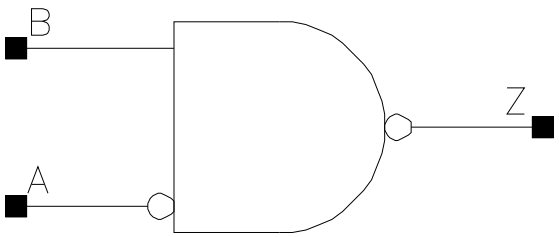
	C12T28SOI_LL_-NAND2X13_P0	C12T28SOI_LL_-NAND2X17_P0	C12T28SOI_LL_-NAND2X20_P0	C12T28SOI_LL_-NAND2X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P0	C12T28SOI_LL_-NAND2X42_P0	C12T28SOI_LL_-NAND2X47_P0	C12T28SOI_LL_-NAND2X50_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P0	C12T28SOI_LL_-NAND2X67_P0	C12T28SOI_-LLBR0D8_-NAND2X7_P0	C12T28SOI_-LLBR0D8_-NAND2X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P0	C12T28SOI_LLS_-NAND2X54_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X7_P0	1.200	0.544	0.6528
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X40_P0	1.200	2.312	2.7744
X54_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P0	X7_P0	X13_P0	X27_P0
A	0.0008	0.0008	0.0010	0.0019
B	0.0006	0.0008	0.0015	0.0030
	X40_P0	X54_P0		
A	0.0029	0.0038		
B	0.0045	0.0060		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0199	0.0211	4.8337	2.6468
A to Z ↑	0.0155	0.0162	4.1624	2.1829
B to Z ↓	0.0087	0.0076	5.0148	2.7252
B to Z ↑	0.0100	0.0081	4.3918	2.2868
	X13_P0	**X27_P0**	**X13_P0**	**X27_P0**

A to Z ↓	0.0193	0.0189	1.4345	0.7123
A to Z ↑	0.0156	0.0152	1.1303	0.5458
B to Z ↓	0.0072	0.0072	1.4797	0.7350
B to Z ↑	0.0073	0.0070	1.1437	0.5655
	X40_P0	**X54_P0**	**X40_P0**	**X54_P0**
A to Z ↓	0.0191	0.0191	0.4748	0.3603
A to Z ↑	0.0155	0.0155	0.3634	0.2746
B to Z ↓	0.0073	0.0074	0.4900	0.3718
B to Z ↑	0.0071	0.0071	0.3807	0.2879

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	7.834e-06	1.000e-20
X7_P0	1.497e-05	1.000e-20
X13_P0	3.511e-05	1.000e-20
X27_P0	6.690e-05	1.000e-20
X40_P0	9.832e-05	1.000e-20
X54_P0	1.297e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	1.173e-03	1.417e-03	2.404e-03	4.713e-03
B (output stable)	3.178e-05	5.687e-05	3.454e-04	6.050e-04
A to Z	1.930e-03	2.617e-03	4.853e-03	9.573e-03
B to Z	7.303e-04	1.224e-03	2.338e-03	4.584e-03
	X40_P0	X54_P0		
A (output stable)	7.131e-03	9.377e-03		
B (output stable)	8.892e-04	1.144e-03		
A to Z	1.425e-02	1.887e-02		
B to Z	6.780e-03	8.965e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

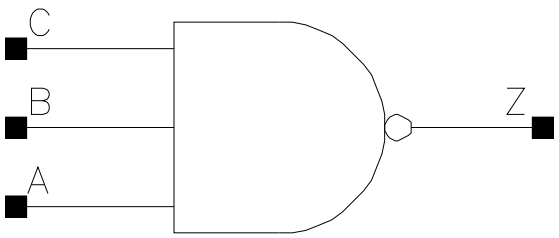
Pin Cycle (vdds)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P0	X54_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P0	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P0	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P0	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P0	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P0	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P0	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P0	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P0	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P0	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P0	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P0	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P0	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P0	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P0	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P0	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A	0.0007	0.0008	0.0013	0.0016
B	0.0007	0.0009	0.0013	0.0015
C	0.0006	0.0008	0.0012	0.0015
	C12T28SOI_LL_-NAND3X15_P0	C12T28SOI_LL_-NAND3X18_P0	C12T28SOI_LL_-NAND3X21_P0	C12T28SOI_LL_-NAND3X24_P0
A	0.0021	0.0024	0.0029	0.0032
B	0.0020	0.0023	0.0028	0.0031
C	0.0019	0.0022	0.0027	0.0030
	C12T28SOI_LL_-NAND3X35_P0	C12T28SOI_LL_-NAND3X47_P0	C12T28SOI_-LLBR0P6_-NAND3X6_P0	C12T28SOI_-LLBR0P6_-NAND3X12_P0
A	0.0049	0.0065	0.0008	0.0016
B	0.0046	0.0062	0.0009	0.0015
C	0.0045	0.0060	0.0008	0.0015
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	C12T28SOI_-LLBR0P6_-NAND3X24_P0	C12T28SOI_-LLBR0P6_-NAND3X35_P0	C12T28SOI_-LLBR0P6_-NAND3X47_P0
A	0.0024	0.0032	0.0048	0.0064
B	0.0022	0.0030	0.0045	0.0060
C	0.0021	0.0029	0.0043	0.0058
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0			
A	0.0025			
B	0.0024			
C	0.0022			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0
A to Z ↓	0.0123	0.0113	5.1168	3.6868
A to Z ↑	0.0140	0.0125	3.1708	2.1817
B to Z ↓	0.0135	0.0121	5.1461	3.7068
B to Z ↑	0.0133	0.0116	3.1790	2.1877
C to Z ↓	0.0125	0.0114	5.1630	3.7200
C to Z ↑	0.0114	0.0099	3.1840	2.2026

	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A to Z ↓	0.0123	0.0116	2.5030	1.9589
A to Z ↑	0.0131	0.0122	1.4890	1.1211
B to Z ↓	0.0122	0.0116	2.5164	1.9690
B to Z ↑	0.0119	0.0110	1.4924	1.1238
C to Z ↓	0.0113	0.0110	2.5261	1.9769
C to Z ↑	0.0099	0.0090	1.4859	1.1143
	C12T28SOI_LL_-NAND3X15_P0	**C12T28SOI_LL_-NAND3X18_P0**	**C12T28SOI_LL_-NAND3X15_P0**	**C12T28SOI_LL_-NAND3X18_P0**
A to Z ↓	0.0110	0.0108	1.5718	1.3513
A to Z ↑	0.0119	0.0115	0.8956	0.7453
B to Z ↓	0.0115	0.0114	1.5815	1.3591
B to Z ↑	0.0107	0.0102	0.8983	0.7477
C to Z ↓	0.0110	0.0109	1.5878	1.3639
C to Z ↑	0.0090	0.0085	0.9050	0.7534
	C12T28SOI_LL_-NAND3X21_P0	**C12T28SOI_LL_-NAND3X24_P0**	**C12T28SOI_LL_-NAND3X21_P0**	**C12T28SOI_LL_-NAND3X24_P0**
A to Z ↓	0.0114	0.0113	1.1418	1.0254
A to Z ↑	0.0120	0.0117	0.6431	0.5650
B to Z ↓	0.0116	0.0115	1.1480	1.0309
B to Z ↑	0.0108	0.0105	0.6445	0.5662
C to Z ↓	0.0111	0.0110	1.1524	1.0349
C to Z ↑	0.0090	0.0086	0.6456	0.5666
	C12T28SOI_LL_-NAND3X35_P0	**C12T28SOI_LL_-NAND3X47_P0**	**C12T28SOI_LL_-NAND3X35_P0**	**C12T28SOI_LL_-NAND3X47_P0**
A to Z ↓	0.0108	0.0110	0.7002	0.5338
A to Z ↑	0.0113	0.0114	0.3798	0.2878
B to Z ↓	0.0112	0.0113	0.7043	0.5369
B to Z ↑	0.0101	0.0101	0.3796	0.2865
C to Z ↓	0.0108	0.0108	0.7073	0.5392
C to Z ↑	0.0082	0.0081	0.3816	0.2877
	C12T28SOI_-LLBR0P6_-NAND3X6_P0	**C12T28SOI_-LLBR0P6_-NAND3X12_P0**	**C12T28SOI_-LLBR0P6_-NAND3X6_P0**	**C12T28SOI_-LLBR0P6_-NAND3X12_P0**
A to Z ↓	0.0083	0.0087	2.5124	1.3371
A to Z ↑	0.0181	0.0179	3.3948	1.7394
B to Z ↓	0.0085	0.0079	2.5416	1.3534
B to Z ↑	0.0164	0.0155	3.4062	1.7449
C to Z ↓	0.0069	0.0061	2.5685	1.3684
C to Z ↑	0.0131	0.0119	3.4250	1.7501
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	**C12T28SOI_-LLBR0P6_-NAND3X24_P0**	**C12T28SOI_-LLBR0P6_-NAND3X18_P0**	**C12T28SOI_-LLBR0P6_-NAND3X24_P0**
A to Z ↓	0.0079	0.0084	0.9256	0.7026
A to Z ↑	0.0168	0.0172	1.1573	0.8758
B to Z ↓	0.0076	0.0077	0.9367	0.7112
B to Z ↑	0.0144	0.0148	1.1616	0.8780
C to Z ↓	0.0063	0.0062	0.9457	0.7188
C to Z ↑	0.0114	0.0114	1.1698	0.8781
	C12T28SOI_-LLBR0P6_-NAND3X35_P0	**C12T28SOI_-LLBR0P6_-NAND3X47_P0**	**C12T28SOI_-LLBR0P6_-NAND3X35_P0**	**C12T28SOI_-LLBR0P6_-NAND3X47_P0**

A to Z ↓	0.0080	0.0081	0.4819	0.3691
A to Z ↑	0.0172	0.0171	0.6053	0.4594
B to Z ↓	0.0077	0.0077	0.4882	0.3738
B to Z ↑	0.0147	0.0146	0.6061	0.4589
C to Z ↓	0.0062	0.0064	0.4935	0.3775
C to Z ↑	0.0112	0.0113	0.6115	0.4600
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P0**	
A to Z ↓	0.0089		0.9092	
A to Z ↑	0.0171		1.0928	
B to Z ↓	0.0079		0.9194	
B to Z ↑	0.0147		1.0955	
C to Z ↓	0.0063		0.9290	
C to Z ↑	0.0111		1.0868	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P0	5.251e-06	1.000e-20
C12T28SOI_LL_NAND3X6_P0	9.493e-06	1.000e-20
C12T28SOI_LL_NAND3X9_P0	1.152e-05	1.000e-20
C12T28SOI_LL_NAND3X12_P0	1.750e-05	1.000e-20
C12T28SOI_LL_NAND3X15_P0	2.004e-05	1.000e-20
C12T28SOI_LL_NAND3X18_P0	2.511e-05	1.000e-20
C12T28SOI_LL_NAND3X21_P0	2.907e-05	1.000e-20
C12T28SOI_LL_NAND3X24_P0	3.338e-05	1.000e-20
C12T28SOI_LL_NAND3X35_P0	4.924e-05	1.000e-20
C12T28SOI_LL_NAND3X47_P0	6.512e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_P0	6.234e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P0	1.102e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P0	1.517e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P0	2.035e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P0	2.963e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P0	3.894e-05	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P0	2.204e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A (output stable)	2.854e-05	4.024e-05	9.233e-05	1.095e-04
B (output stable)	7.267e-05	9.388e-05	2.118e-04	2.514e-04
C (output stable)	2.491e-04	3.005e-04	4.903e-04	5.692e-04
A to Z	1.633e-03	2.070e-03	3.253e-03	3.950e-03
B to Z	1.491e-03	1.871e-03	2.755e-03	3.373e-03
C to Z	1.261e-03	1.603e-03	2.318e-03	2.864e-03

	C12T28SOI_LL_-NAND3X15_P0	C12T28SOI_LL_-NAND3X18_P0	C12T28SOI_LL_-NAND3X21_P0	C12T28SOI_LL_-NAND3X24_P0
A (output stable)	1.197e-04	1.362e-04	1.897e-04	2.031e-04
B (output stable)	2.884e-04	3.319e-04	4.279e-04	4.749e-04
C (output stable)	6.102e-04	6.909e-04	9.203e-04	1.016e-03
A to Z	4.742e-03	5.429e-03	6.748e-03	7.431e-03
B to Z	4.039e-03	4.625e-03	5.742e-03	6.337e-03
C to Z	3.481e-03	3.981e-03	4.889e-03	5.397e-03
	C12T28SOI_LL_-NAND3X35_P0	C12T28SOI_LL_-NAND3X47_P0	C12T28SOI_-LLBR0P6_-NAND3X6_P0	C12T28SOI_-LLBR0P6_-NAND3X12_P0
A (output stable)	2.803e-04	3.700e-04	5.798e-05	1.564e-04
B (output stable)	6.685e-04	8.935e-04	1.359e-04	3.691e-04
C (output stable)	1.460e-03	1.884e-03	4.084e-04	8.155e-04
A to Z	1.065e-02	1.409e-02	2.152e-03	4.174e-03
B to Z	9.005e-03	1.192e-02	1.837e-03	3.284e-03
C to Z	7.589e-03	1.004e-02	1.405e-03	2.427e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	C12T28SOI_-LLBR0P6_-NAND3X24_P0	C12T28SOI_-LLBR0P6_-NAND3X35_P0	C12T28SOI_-LLBR0P6_-NAND3X47_P0
A (output stable)	1.971e-04	2.889e-04	3.973e-04	5.248e-04
B (output stable)	4.681e-04	6.879e-04	9.505e-04	1.265e-03
C (output stable)	9.257e-04	1.457e-03	2.098e-03	2.713e-03
A to Z	5.647e-03	7.788e-03	1.128e-02	1.470e-02
B to Z	4.439e-03	6.138e-03	8.859e-03	1.156e-02
C to Z	3.416e-03	4.579e-03	6.519e-03	8.510e-03
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0			
A (output stable)	2.327e-04			
B (output stable)	5.525e-04			
C (output stable)	1.175e-03			
A to Z	6.253e-03			
B to Z	4.952e-03			
C to Z	3.698e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P0	C12T28SOI_LL_-NAND3X18_P0	C12T28SOI_LL_-NAND3X21_P0	C12T28SOI_LL_-NAND3X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

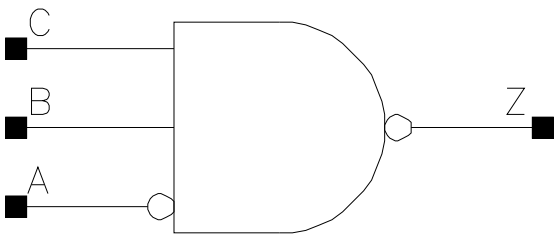
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P0	C12T28SOI_LL_-NAND3X47_P0	C12T28SOI_-LLBR0P6_-NAND3X6_P0	C12T28SOI_-LLBR0P6_-NAND3X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	C12T28SOI_-LLBR0P6_-NAND3X24_P0	C12T28SOI_-LLBR0P6_-NAND3X35_P0	C12T28SOI_-LLBR0P6_-NAND3X47_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.816	0.9792
X12_P0	1.200	1.224	1.4688
X18_P0	1.200	1.496	1.7952
X24_P0	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0008	0.0011	0.0011	0.0019
B	0.0008	0.0016	0.0023	0.0031
C	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X12_P0**	**X6_P0**	**X12_P0**
A to Z ↓	0.0238	0.0226	3.6564	1.9683
A to Z ↑	0.0172	0.0169	2.1182	1.0648
B to Z ↓	0.0108	0.0110	3.7075	1.9958
B to Z ↑	0.0104	0.0103	2.1974	1.1100
C to Z ↓	0.0109	0.0102	3.7230	2.0031
C to Z ↑	0.0092	0.0082	2.2115	1.1194
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0261	0.0222	1.3474	1.0243

A to Z ↑	0.0198	0.0162	0.7176	0.5382
B to Z ↓	0.0113	0.0110	1.3636	1.0377
B to Z ↑	0.0102	0.0100	0.7489	0.5636
C to Z ↓	0.0110	0.0104	1.3680	1.0415
C to Z ↑	0.0086	0.0080	0.7548	0.5680

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P0	1.305e-05	1.000e-20
X12_P0	2.964e-05	1.000e-20
X18_P0	3.717e-05	1.000e-20
X24_P0	5.676e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	1.376e-03	2.516e-03	3.269e-03	4.786e-03
B (output stable)	7.580e-05	2.233e-04	3.481e-04	4.896e-04
C (output stable)	1.408e-04	5.656e-04	7.015e-04	1.037e-03
A to Z	3.078e-03	6.056e-03	8.650e-03	1.178e-02
B to Z	1.611e-03	3.123e-03	4.629e-03	6.009e-03
C to Z	1.450e-03	2.579e-03	3.986e-03	4.970e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

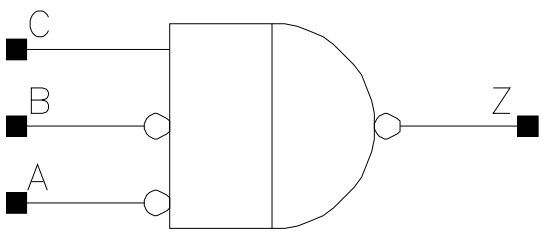
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	0.816	0.9792
X13_P0	1.200	1.088	1.3056
X20_P0	1.200	1.632	1.9584
X27_P0	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P0	X13_P0	X20_P0	X27_P0
A	0.0009	0.0009	0.0018	0.0017
B	0.0011	0.0010	0.0019	0.0018
C	0.0008	0.0015	0.0022	0.0030

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	**X13_P0**	**X7_P0**	**X13_P0**
A to Z ↓	0.0217	0.0264	2.5434	1.3576
A to Z ↑	0.0151	0.0175	2.0958	1.0560
B to Z ↓	0.0225	0.0274	2.5452	1.3577
B to Z ↑	0.0142	0.0166	2.0944	1.0561
C to Z ↓	0.0074	0.0071	2.6168	1.3917
C to Z ↑	0.0081	0.0072	2.1983	1.1152
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0239	0.0263	0.9257	0.7067
A to Z ↑	0.0162	0.0197	0.7138	0.5368
B to Z ↓	0.0234	0.0262	0.9262	0.7065

B to Z ↑	0.0147	0.0185	0.7131	0.5362
C to Z ↓	0.0079	0.0076	0.9514	0.7245
C to Z ↑	0.0078	0.0075	0.7531	0.5655

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X7_P0	1.932e-05	1.000e-20
X13_P0	2.546e-05	1.000e-20
X20_P0	4.187e-05	1.000e-20
X27_P0	4.705e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	7.960e-04	1.032e-03	1.755e-03	2.023e-03
B (output stable)	7.399e-04	9.740e-04	1.639e-03	1.923e-03
C (output stable)	5.970e-05	3.959e-04	4.017e-04	5.101e-04
A to Z	3.515e-03	5.728e-03	8.903e-03	1.113e-02
B to Z	3.316e-03	5.506e-03	8.155e-03	1.042e-02
C to Z	1.287e-03	2.361e-03	3.695e-03	4.868e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

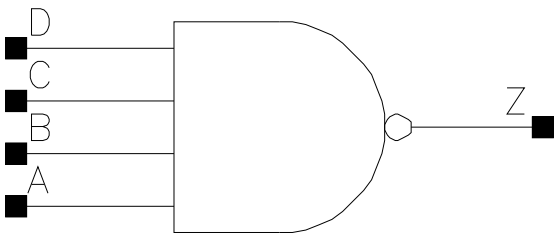
Pin Cycle (vdds)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0006	0.0006	0.0008	0.0009
B	0.0007	0.0007	0.0008	0.0010
C	0.0006	0.0007	0.0008	0.0010
D	0.0007	0.0007	0.0009	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0341	0.0337	1.5560	0.7791
A to Z ↑	0.0282	0.0306	2.1553	1.0662
B to Z ↓	0.0352	0.0355	1.5565	0.7792
B to Z ↑	0.0271	0.0300	2.1561	1.0648
C to Z ↓	0.0346	0.0338	1.5560	0.7783
C to Z ↑	0.0291	0.0318	2.1555	1.0649

D to Z ↓	0.0361	0.0351	1.5550	0.7793
D to Z ↑	0.0284	0.0306	2.1545	1.0632
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0354	0.0329	0.5381	0.4020
A to Z ↑	0.0292	0.0286	0.7196	0.5401
B to Z ↓	0.0367	0.0340	0.5381	0.4020
B to Z ↑	0.0283	0.0276	0.7195	0.5398
C to Z ↓	0.0333	0.0307	0.5381	0.4018
C to Z ↑	0.0295	0.0286	0.7188	0.5388
D to Z ↓	0.0346	0.0320	0.5376	0.4019
D to Z ↑	0.0285	0.0276	0.7183	0.5391

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.560e-05	1.000e-20
X17_P0	2.600e-05	1.000e-20
X25_P0	3.797e-05	1.000e-20
X33_P0	5.788e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	5.645e-04	6.857e-04	9.955e-04	1.220e-03
B (output stable)	5.351e-04	6.592e-04	9.519e-04	1.165e-03
C (output stable)	5.718e-04	6.761e-04	1.023e-03	1.191e-03
D (output stable)	5.385e-04	6.406e-04	9.697e-04	1.130e-03
A to Z	4.129e-03	6.283e-03	9.569e-03	1.180e-02
B to Z	4.034e-03	6.201e-03	9.430e-03	1.163e-02
C to Z	4.241e-03	6.247e-03	9.081e-03	1.109e-02
D to Z	4.156e-03	6.146e-03	8.940e-03	1.092e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

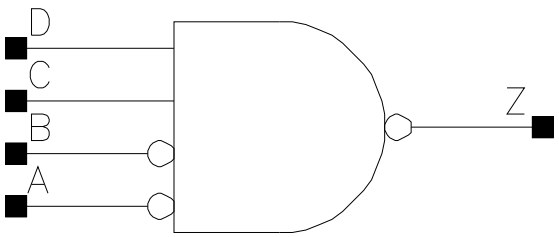
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X12_P0	1.200	1.496	1.7952
X18_P0	1.200	2.040	2.4480
X24_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0010	0.0010	0.0019	0.0017
B	0.0010	0.0014	0.0019	0.0018
C	0.0008	0.0016	0.0023	0.0031
D	0.0008	0.0015	0.0022	0.0031

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X12_P0	X6_P0	X12_P0
A to Z ↓	0.0231	0.0306	3.7691	1.9723
A to Z ↑	0.0159	0.0196	2.0992	1.0597
B to Z ↓	0.0236	0.0312	3.7701	1.9727
B to Z ↑	0.0144	0.0183	2.0988	1.0589
C to Z ↓	0.0109	0.0110	3.8198	1.9946
C to Z ↑	0.0105	0.0102	2.3463	1.1095

D to Z ↓	0.0108	0.0102	3.8340	2.0019
D to Z ↑	0.0092	0.0081	2.3607	1.1184
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0265	0.0297	1.3445	1.0239
A to Z ↑	0.0171	0.0221	0.7147	0.5372
B to Z ↓	0.0261	0.0295	1.3445	1.0240
B to Z ↑	0.0156	0.0207	0.7139	0.5360
C to Z ↓	0.0109	0.0114	1.3602	1.0346
C to Z ↑	0.0099	0.0103	0.7526	0.5612
D to Z ↓	0.0105	0.0109	1.3653	1.0388
D to Z ↑	0.0083	0.0084	0.7700	0.5666

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P0	1.709e-05	1.000e-20
X12_P0	2.181e-05	1.000e-20
X18_P0	3.676e-05	1.000e-20
X24_P0	4.003e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	9.092e-04	1.430e-03	2.204e-03	2.581e-03
B (output stable)	8.393e-04	1.337e-03	2.000e-03	2.390e-03
C (output stable)	9.185e-05	2.534e-04	3.725e-04	5.223e-04
D (output stable)	1.664e-04	6.058e-04	7.361e-04	1.128e-03
A to Z	3.678e-03	6.786e-03	9.968e-03	1.317e-02
B to Z	3.505e-03	6.423e-03	9.268e-03	1.240e-02
C to Z	1.564e-03	3.114e-03	4.450e-03	6.265e-03
D to Z	1.402e-03	2.570e-03	3.831e-03	5.255e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

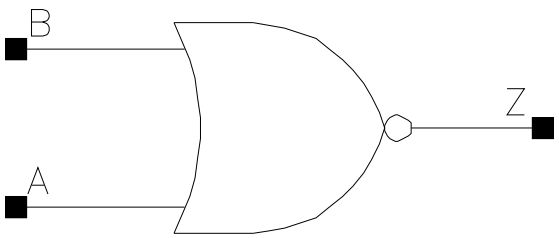
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.408	0.4896
X5_P0	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X10_P0	1.200	0.680	0.8160
X14_P0	1.200	0.680	0.8160
X17_P0	1.200	0.952	1.1424
X21_P0	1.200	0.952	1.1424
X24_P0	1.200	1.224	1.4688
X27_P0	1.200	1.224	1.4688
X34_P0	1.200	1.496	1.7952
X40_P0	1.200	1.360	1.6320
X41_P0	1.200	1.768	2.1216
X49_P0	1.200	1.496	1.7952
X53_P0	1.200	1.904	2.2848
X55_P0	1.200	2.312	2.7744
X57_P0	1.200	1.904	2.2848
X65_P0	1.200	2.040	2.4480
X84_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P0	X5_P0	X7_P0	X10_P0
A	0.0005	0.0006	0.0008	0.0013
B	0.0005	0.0006	0.0008	0.0012
	X14_P0	X17_P0	X21_P0	X24_P0

A	0.0017	0.0021	0.0025	0.0028
B	0.0015	0.0019	0.0023	0.0027
	X27_P0	X34_P0	X40_P0	X41_P0
A	0.0032	0.0040	0.0009	0.0049
B	0.0030	0.0038	0.0011	0.0046
	X49_P0	X53_P0	X55_P0	X57_P0
A	0.0009	0.0010	0.0065	0.0010
B	0.0011	0.0009	0.0061	0.0009
	X65_P0	X84_P0		
A	0.0010	0.0011		
B	0.0009	0.0010		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X5_P0**	**X3_P0**	**X5_P0**
A to Z ↓	0.0065	0.0062	3.0753	2.2254
A to Z ↑	0.0125	0.0114	8.2149	5.9948
B to Z ↓	0.0056	0.0050	3.1498	2.2419
B to Z ↑	0.0130	0.0118	8.2532	6.0136
	X7_P0	**X10_P0**	**X7_P0**	**X10_P0**
A to Z ↓	0.0061	0.0063	1.6388	1.0620
A to Z ↑	0.0105	0.0117	4.2233	2.8425
B to Z ↓	0.0049	0.0043	1.6607	1.0741
B to Z ↑	0.0108	0.0102	4.2393	2.8522
	X14_P0	**X17_P0**	**X14_P0**	**X17_P0**
A to Z ↓	0.0064	0.0063	0.8104	0.6507
A to Z ↑	0.0107	0.0109	2.1033	1.7034
B to Z ↓	0.0043	0.0048	0.8195	0.6568
B to Z ↑	0.0096	0.0104	2.1122	1.7099
	X21_P0	**X24_P0**	**X21_P0**	**X24_P0**
A to Z ↓	0.0064	0.0062	0.5541	0.4714
A to Z ↑	0.0104	0.0106	1.4161	1.2429
B to Z ↓	0.0048	0.0044	0.5594	0.4765
B to Z ↑	0.0101	0.0099	1.4222	1.2484
	X27_P0	**X34_P0**	**X27_P0**	**X34_P0**
A to Z ↓	0.0062	0.0066	0.4197	0.3389
A to Z ↑	0.0102	0.0104	1.0938	0.8699
B to Z ↓	0.0043	0.0048	0.4245	0.3424
B to Z ↑	0.0095	0.0100	1.0990	0.8739
	X40_P0	**X41_P0**	**X40_P0**	**X41_P0**
A to Z ↓	0.0238	0.0064	0.3289	0.2824
A to Z ↑	0.0315	0.0101	0.4425	0.7198
B to Z ↓	0.0227	0.0045	0.3289	0.2857
B to Z ↑	0.0327	0.0094	0.4427	0.7232
	X49_P0	**X53_P0**	**X49_P0**	**X53_P0**
A to Z ↓	0.0247	0.0259	0.2734	0.2507
A to Z ↑	0.0324	0.0368	0.3680	0.3404
B to Z ↓	0.0236	0.0249	0.2735	0.2508
B to Z ↑	0.0335	0.0376	0.3680	0.3403
	X55_P0	**X57_P0**	**X55_P0**	**X57_P0**
A to Z ↓	0.0065	0.0261	0.2137	0.2356
A to Z ↑	0.0101	0.0370	0.5431	0.3165

B to Z ↓	0.0046	0.0251	0.2165	0.2356
B to Z ↑	0.0095	0.0378	0.5458	0.3163
	X65_P0	**X84_P0**	**X65_P0**	**X84_P0**
A to Z ↓	0.0269	0.0281	0.2067	0.1639
A to Z ↑	0.0378	0.0383	0.2772	0.2206
B to Z ↓	0.0259	0.0270	0.2064	0.1639
B to Z ↑	0.0387	0.0393	0.2774	0.2204

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	3.978e-06	1.000e-20
X5_P0	6.778e-06	1.000e-20
X7_P0	1.135e-05	1.000e-20
X10_P0	1.490e-05	1.000e-20
X14_P0	2.275e-05	1.000e-20
X17_P0	2.631e-05	1.000e-20
X21_P0	3.316e-05	1.000e-20
X24_P0	3.787e-05	1.000e-20
X27_P0	4.359e-05	1.000e-20
X34_P0	5.402e-05	1.000e-20
X40_P0	1.019e-04	1.000e-20
X41_P0	6.445e-05	1.000e-20
X49_P0	1.171e-04	1.000e-20
X53_P0	1.307e-04	1.000e-20
X55_P0	8.531e-05	1.000e-20
X57_P0	1.416e-04	1.000e-20
X65_P0	1.569e-04	1.000e-20
X84_P0	1.789e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	2.615e-05	3.473e-05	4.714e-05	1.423e-04
B (output stable)	3.951e-05	5.199e-05	7.187e-05	3.021e-04
A to Z	8.014e-04	1.014e-03	1.379e-03	2.247e-03
B to Z	6.911e-04	8.698e-04	1.168e-03	1.669e-03
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	1.657e-04	1.961e-04	2.201e-04	2.704e-04
B (output stable)	3.646e-04	3.752e-04	3.914e-04	5.256e-04
A to Z	2.858e-03	3.567e-03	4.153e-03	4.865e-03
B to Z	2.177e-03	2.855e-03	3.341e-03	3.806e-03
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	2.972e-04	3.517e-04	4.751e-05	4.555e-04
B (output stable)	5.681e-04	5.933e-04	7.177e-05	8.768e-04
A to Z	5.364e-03	6.818e-03	1.150e-02	8.089e-03
B to Z	4.178e-03	5.478e-03	1.130e-02	6.275e-03
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	4.813e-05	4.921e-05	5.777e-04	4.911e-05
B (output stable)	7.165e-05	7.705e-05	1.042e-03	7.705e-05
A to Z	1.299e-02	1.608e-02	1.063e-02	1.664e-02
B to Z	1.279e-02	1.586e-02	8.352e-03	1.643e-02
	X65_P0	X84_P0		

A (output stable)	4.941e-05	5.119e-05		
B (output stable)	7.735e-05	7.818e-05		
A to Z	1.819e-02	2.185e-02		
B to Z	1.797e-02	2.160e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

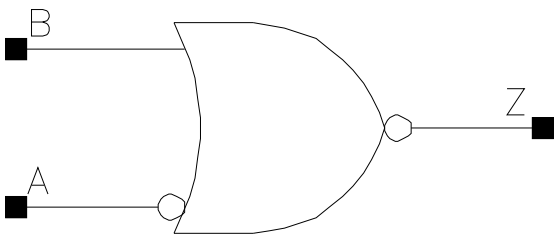
Pin Cycle (vdds)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P0	X84_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X7_P0	1.200	0.680	0.8160
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X41_P0	1.200	2.312	2.7744
X55_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X7_P0	X13_P0
A	0.0008	0.0008	0.0008	0.0011
B	0.0006	0.0008	0.0008	0.0015
	X27_P0	X41_P0	X55_P0	
A	0.0019	0.0029	0.0038	
B	0.0030	0.0046	0.0061	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0185	0.0205	2.8778	1.8956
A to Z ↑	0.0175	0.0175	8.0841	4.1728
B to Z ↓	0.0058	0.0061	3.1198	2.0538
B to Z ↑	0.0131	0.0105	8.2332	4.2565

	X7_P0	X13_P0	X7_P0	X13_P0
A to Z ↓	0.0207	0.0184	1.5116	0.8223
A to Z ↑	0.0191	0.0184	4.1470	2.2189
B to Z ↓	0.0052	0.0045	1.5893	0.8638
B to Z ↑	0.0118	0.0106	4.2091	2.2571
	X27_P0	**X41_P0**	**X27_P0**	**X41_P0**
A to Z ↓	0.0178	0.0182	0.3931	0.2665
A to Z ↑	0.0176	0.0179	1.0589	0.7113
B to Z ↓	0.0045	0.0046	0.4274	0.2881
B to Z ↑	0.0099	0.0098	1.0776	0.7243
	X55_P0		**X55_P0**	
A to Z ↓	0.0179		0.2020	
A to Z ↑	0.0176		0.5377	
B to Z ↓	0.0046		0.2185	
B to Z ↑	0.0097		0.5474	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	7.805e-06	1.000e-20
X6_P0	1.496e-05	1.000e-20
X7_P0	1.665e-05	1.000e-20
X13_P0	3.415e-05	1.000e-20
X27_P0	6.669e-05	1.000e-20
X41_P0	9.802e-05	1.000e-20
X55_P0	1.293e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	1.162e-03	1.393e-03	1.484e-03	2.454e-03
B (output stable)	3.941e-05	7.123e-05	1.818e-04	3.188e-04
A to Z	1.919e-03	2.573e-03	2.976e-03	5.026e-03
B to Z	6.986e-04	1.116e-03	1.340e-03	2.271e-03
	X27_P0	X41_P0	X55_P0	
A (output stable)	4.861e-03	7.344e-03	9.587e-03	
B (output stable)	6.190e-04	8.732e-04	1.076e-03	
A to Z	9.967e-03	1.491e-02	1.951e-02	
B to Z	4.449e-03	6.533e-03	8.608e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

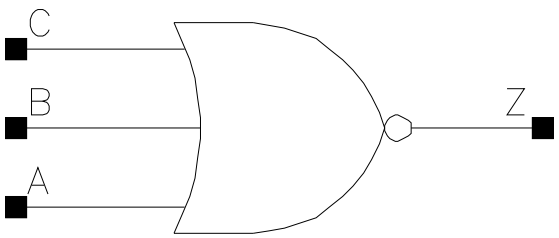
Pin Cycle (vdds)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X41_P0	X55_P0	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X9_P0	1.200	0.952	1.1424
X13_P0	1.200	0.952	1.1424
X16_P0	1.200	1.360	1.6320
X19_P0	1.200	1.496	1.7952
X22_P0	1.200	1.768	2.1216
X25_P0	1.200	1.904	2.2848
X37_P0	1.200	2.584	3.1008
X49_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P0	X6_P0	X9_P0	X13_P0
A	0.0007	0.0008	0.0012	0.0015
B	0.0006	0.0008	0.0014	0.0017
C	0.0007	0.0008	0.0012	0.0015
	X16_P0	X19_P0	X22_P0	X25_P0
A	0.0021	0.0024	0.0029	0.0032
B	0.0021	0.0028	0.0030	0.0038
C	0.0019	0.0022	0.0026	0.0029
	X37_P0	X49_P0		
A	0.0048	0.0065		
B	0.0049	0.0066		

C	0.0043	0.0060		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0079	0.0076	2.2549	1.6627
A to Z ↑	0.0165	0.0148	8.8718	6.2609
B to Z ↓	0.0072	0.0069	2.2643	1.6687
B to Z ↑	0.0163	0.0146	8.8908	6.2756
C to Z ↓	0.0062	0.0057	2.2817	1.6869
C to Z ↑	0.0161	0.0143	8.9003	6.2823
	X9_P0	**X13_P0**	**X9_P0**	**X13_P0**
A to Z ↓	0.0078	0.0077	1.0940	0.8434
A to Z ↑	0.0164	0.0151	4.1852	3.1203
B to Z ↓	0.0071	0.0067	1.0675	0.8084
B to Z ↑	0.0165	0.0148	4.1974	3.1283
C to Z ↓	0.0051	0.0048	1.0803	0.8255
C to Z ↑	0.0134	0.0124	4.1966	3.1289
	X16_P0	**X19_P0**	**X16_P0**	**X19_P0**
A to Z ↓	0.0077	0.0076	0.6541	0.5543
A to Z ↑	0.0156	0.0153	2.5281	2.0892
B to Z ↓	0.0072	0.0071	0.6567	0.5432
B to Z ↑	0.0156	0.0155	2.5341	2.0946
C to Z ↓	0.0054	0.0054	0.6617	0.5658
C to Z ↑	0.0139	0.0131	2.5350	2.0954
	X22_P0	**X25_P0**	**X22_P0**	**X25_P0**
A to Z ↓	0.0077	0.0077	0.4805	0.4226
A to Z ↑	0.0154	0.0152	1.8067	1.5727
B to Z ↓	0.0070	0.0069	0.4726	0.4070
B to Z ↑	0.0153	0.0154	1.8113	1.5771
C to Z ↓	0.0050	0.0051	0.4788	0.4237
C to Z ↑	0.0129	0.0125	1.8120	1.5773
	X37_P0	**X49_P0**	**X37_P0**	**X49_P0**
A to Z ↓	0.0078	0.0078	0.2906	0.2202
A to Z ↑	0.0147	0.0147	1.0556	0.7956
B to Z ↓	0.0070	0.0071	0.2876	0.2182
B to Z ↑	0.0144	0.0144	1.0583	0.7975
C to Z ↓	0.0054	0.0055	0.2915	0.2211
C to Z ↑	0.0126	0.0127	1.0585	0.7981

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	5.205e-06	1.000e-20
X6_P0	8.896e-06	1.000e-20
X9_P0	1.150e-05	1.000e-20
X13_P0	1.806e-05	1.000e-20
X16_P0	2.028e-05	1.000e-20
X19_P0	2.690e-05	1.000e-20
X22_P0	2.932e-05	1.000e-20
X25_P0	3.544e-05	1.000e-20
X37_P0	5.233e-05	1.000e-20

X49_P0	6.946e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	3.765e-05	5.091e-05	9.662e-05	1.241e-04
B (output stable)	4.080e-05	5.985e-05	1.252e-04	1.585e-04
C (output stable)	7.556e-05	1.156e-04	2.841e-04	3.756e-04
A to Z	1.325e-03	1.718e-03	2.813e-03	3.494e-03
B to Z	1.137e-03	1.466e-03	2.454e-03	3.008e-03
C to Z	9.904e-04	1.251e-03	1.814e-03	2.264e-03
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	1.477e-04	1.765e-04	2.130e-04	2.467e-04
B (output stable)	1.936e-04	2.597e-04	2.882e-04	3.503e-04
C (output stable)	3.930e-04	5.275e-04	6.100e-04	7.412e-04
A to Z	4.487e-03	5.345e-03	6.169e-03	7.059e-03
B to Z	3.858e-03	4.659e-03	5.331e-03	6.150e-03
C to Z	3.107e-03	3.577e-03	4.110e-03	4.556e-03
	X37_P0	X49_P0		
A (output stable)	3.560e-04	4.719e-04		
B (output stable)	4.702e-04	6.171e-04		
C (output stable)	1.005e-03	1.312e-03		
A to Z	1.024e-02	1.363e-02		
B to Z	8.744e-03	1.160e-02		
C to Z	6.722e-03	8.976e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

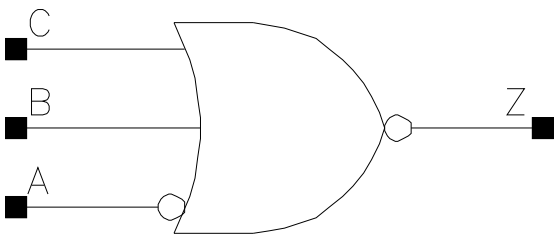
Pin Cycle (vdds)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P0	X49_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.680	0.8160
X13_P0	1.200	1.224	1.4688
X19_P0	1.200	1.496	1.7952
X25_P0	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0008	0.0010	0.0011	0.0020
B	0.0008	0.0017	0.0024	0.0032
C	0.0008	0.0015	0.0022	0.0030

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X13_P0**	**X6_P0**	**X13_P0**
A to Z ↓	0.0207	0.0197	1.5690	0.8751
A to Z ↑	0.0227	0.0225	6.3159	3.1079
B to Z ↓	0.0070	0.0068	1.6743	0.8131
B to Z ↑	0.0148	0.0149	6.3605	3.1296
C to Z ↓	0.0058	0.0048	1.6863	0.8259
C to Z ↑	0.0145	0.0124	6.3677	3.1291
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0221	0.0195	0.5308	0.4039

A to Z ↑	0.0246	0.0225	2.0944	1.5718
B to Z ↓	0.0072	0.0069	0.5654	0.4223
B to Z ↑	0.0145	0.0144	2.1104	1.5832
C to Z ↓	0.0053	0.0050	0.5665	0.4262
C to Z ↑	0.0132	0.0124	2.1114	1.5843

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P0	1.291e-05	1.000e-20
X13_P0	3.070e-05	1.000e-20
X19_P0	3.866e-05	1.000e-20
X25_P0	5.851e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	1.431e-03	2.641e-03	3.246e-03	5.112e-03
B (output stable)	6.110e-05	1.654e-04	2.319e-04	3.195e-04
C (output stable)	1.164e-04	4.080e-04	4.843e-04	7.111e-04
A to Z	3.103e-03	6.193e-03	8.326e-03	1.188e-02
B to Z	1.472e-03	3.033e-03	4.393e-03	5.832e-03
C to Z	1.263e-03	2.270e-03	3.555e-03	4.498e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

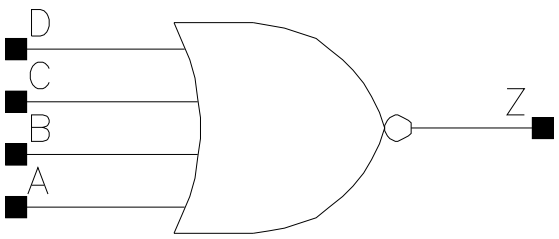
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	1.904	2.2848
X32_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X32_P0
A	0.0006	0.0007	0.0007	0.0009
B	0.0007	0.0007	0.0009	0.0011
C	0.0006	0.0006	0.0008	0.0009
D	0.0006	0.0006	0.0008	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0241	0.0241	1.5318	0.7552
A to Z ↑	0.0351	0.0376	2.1804	1.0814
B to Z ↓	0.0230	0.0232	1.5316	0.7548
B to Z ↑	0.0358	0.0386	2.1796	1.0816
C to Z ↓	0.0238	0.0242	1.5296	0.7538
C to Z ↑	0.0358	0.0387	2.1816	1.0820

D to Z ↓	0.0232	0.0237	1.5304	0.7545
D to Z ↑	0.0368	0.0400	2.1825	1.0831
	X25_P0	**X32_P0**	**X25_P0**	**X32_P0**
A to Z ↓	0.0249	0.0267	0.5263	0.4130
A to Z ↑	0.0368	0.0356	0.7435	0.5614
B to Z ↓	0.0241	0.0257	0.5259	0.4130
B to Z ↑	0.0380	0.0364	0.7438	0.5614
C to Z ↓	0.0242	0.0264	0.5240	0.4118
C to Z ↑	0.0367	0.0360	0.7430	0.5609
D to Z ↓	0.0233	0.0250	0.5241	0.4119
D to Z ↑	0.0377	0.0368	0.7428	0.5615

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	2.656e-05	1.000e-20
X17_P0	4.806e-05	1.000e-20
X25_P0	7.359e-05	1.000e-20
X32_P0	1.013e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	5.563e-04	6.622e-04	9.287e-04	1.176e-03
B (output stable)	5.132e-04	6.170e-04	8.755e-04	1.098e-03
C (output stable)	5.335e-04	6.192e-04	9.810e-04	1.249e-03
D (output stable)	4.899e-04	5.782e-04	9.210e-04	1.167e-03
A to Z	3.846e-03	5.947e-03	8.998e-03	1.132e-02
B to Z	3.727e-03	5.836e-03	8.826e-03	1.112e-02
C to Z	3.902e-03	5.972e-03	8.565e-03	1.087e-02
D to Z	3.775e-03	5.865e-03	8.413e-03	1.065e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

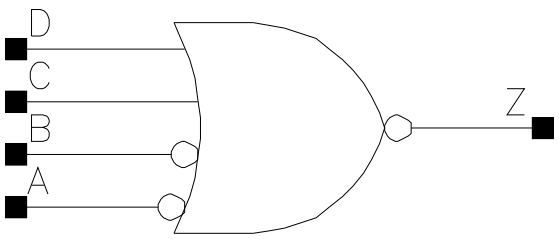
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X13_P0	1.200	1.496	1.7952
X19_P0	1.200	2.040	2.4480
X25_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0010	0.0010	0.0019	0.0019
B	0.0010	0.0015	0.0019	0.0019
C	0.0008	0.0016	0.0023	0.0031
D	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X13_P0	X6_P0	X13_P0
A to Z ↓	0.0178	0.0221	1.5261	0.7670
A to Z ↑	0.0229	0.0283	6.0796	3.1671
B to Z ↓	0.0166	0.0212	1.5252	0.7665
B to Z ↑	0.0236	0.0294	6.0810	3.1687
C to Z ↓	0.0074	0.0069	1.6984	0.8152
C to Z ↑	0.0149	0.0152	6.1297	3.1904

D to Z ↓	0.0060	0.0050	1.7022	0.8235
D to Z ↑	0.0144	0.0129	6.1320	3.1894
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0195	0.0213	0.5257	0.3963
A to Z ↑	0.0254	0.0276	2.0968	1.5875
B to Z ↓	0.0177	0.0199	0.5250	0.3959
B to Z ↑	0.0258	0.0284	2.0963	1.5877
C to Z ↓	0.0072	0.0071	0.5660	0.4242
C to Z ↑	0.0145	0.0145	2.1114	1.5984
D to Z ↓	0.0053	0.0051	0.5671	0.4259
D to Z ↑	0.0132	0.0125	2.1124	1.5983

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P0	1.978e-05	1.000e-20
X13_P0	2.670e-05	1.000e-20
X19_P0	4.414e-05	1.000e-20
X25_P0	5.071e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	9.157e-04	1.427e-03	2.219e-03	2.628e-03
B (output stable)	8.636e-04	1.385e-03	2.116e-03	2.550e-03
C (output stable)	6.885e-05	1.865e-04	2.685e-04	3.622e-04
D (output stable)	1.383e-04	4.139e-04	5.364e-04	7.907e-04
A to Z	3.809e-03	6.894e-03	1.034e-02	1.317e-02
B to Z	3.661e-03	6.602e-03	9.744e-03	1.262e-02
C to Z	1.527e-03	3.047e-03	4.358e-03	5.766e-03
D to Z	1.315e-03	2.343e-03	3.557e-03	4.476e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

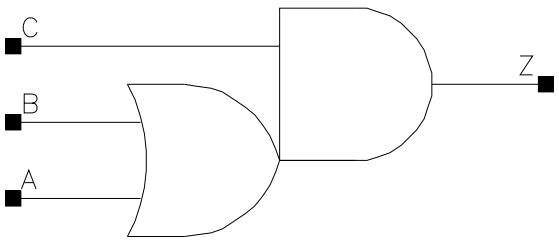
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0009	0.0009	0.0018
B	0.0010	0.0010	0.0020
C	0.0010	0.0010	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0193	0.0224	1.5807	0.7896
A to Z ↑	0.0178	0.0199	2.2026	1.0861
B to Z ↓	0.0199	0.0232	1.5837	0.7899
B to Z ↑	0.0161	0.0184	2.2008	1.0865
C to Z ↓	0.0178	0.0197	1.5663	0.7799
C to Z ↑	0.0166	0.0185	2.1986	1.0856
	X33_P0		**X33_P0**	
A to Z ↓	0.0234		0.4002	
A to Z ↑	0.0215		0.5437	

B to Z ↓	0.0242		0.4002	
B to Z ↑	0.0196		0.5436	
C to Z ↓	0.0201		0.3944	
C to Z ↑	0.0192		0.5432	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	2.693e-05	1.000e-20
X17_P0	4.159e-05	1.000e-20
X33_P0	8.051e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	1.075e-04	1.099e-04	2.219e-04
B (output stable)	1.198e-04	1.228e-04	2.388e-04
C (output stable)	7.636e-05	7.888e-05	1.509e-04
A to Z	3.057e-03	4.672e-03	9.744e-03
B to Z	2.829e-03	4.437e-03	9.284e-03
C to Z	3.300e-03	4.780e-03	9.822e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

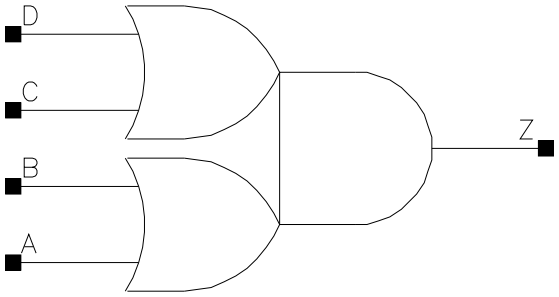
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0018
B	0.0007	0.0010	0.0019
C	0.0007	0.0010	0.0019
D	0.0006	0.0010	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0328	0.0278	1.5280	0.7808
A to Z ↑	0.0237	0.0213	2.1564	1.0792
B to Z ↓	0.0340	0.0289	1.5293	0.7815
B to Z ↑	0.0228	0.0202	2.1545	1.0778

C to Z ↓	0.0287	0.0247	1.5198	0.7781
C to Z ↑	0.0232	0.0216	2.1559	1.0788
D to Z ↓	0.0292	0.0253	1.5199	0.7781
D to Z ↑	0.0218	0.0198	2.1509	1.0761
	X33_P0		**X33_P0**	
A to Z ↓	0.0283		0.4018	
A to Z ↑	0.0215		0.5429	
B to Z ↓	0.0284		0.4020	
B to Z ↑	0.0199		0.5419	
C to Z ↓	0.0246		0.4000	
C to Z ↑	0.0214		0.5423	
D to Z ↓	0.0244		0.3999	
D to Z ↑	0.0194		0.5411	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.665e-05	1.000e-20
X17_P0	3.883e-05	1.000e-20
X33_P0	7.441e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	2.940e-05	4.811e-05	1.390e-04
B (output stable)	3.580e-05	6.133e-05	2.734e-04
C (output stable)	8.723e-05	1.178e-04	2.739e-04
D (output stable)	9.500e-05	1.324e-04	4.091e-04
A to Z	3.526e-03	5.845e-03	1.151e-02
B to Z	3.395e-03	5.591e-03	1.079e-02
C to Z	3.105e-03	5.287e-03	1.038e-02
D to Z	2.975e-03	5.037e-03	9.626e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

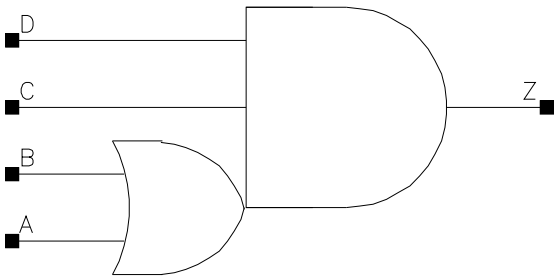
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	1.088	1.3056
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0006	0.0010	0.0016	0.0019
B	0.0006	0.0010	0.0016	0.0019
C	0.0007	0.0010	0.0016	0.0019
D	0.0006	0.0010	0.0016	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0279	0.0260	1.6102	0.7882
A to Z ↑	0.0279	0.0265	2.2341	1.0813
B to Z ↓	0.0289	0.0263	1.6118	0.7880
B to Z ↑	0.0266	0.0244	2.2327	1.0790
C to Z ↓	0.0239	0.0219	1.5817	0.7755

C to Z ↑	0.0254	0.0241	2.2308	1.0788
D to Z ↓	0.0232	0.0212	1.5804	0.7751
D to Z ↑	0.0271	0.0255	2.2296	1.0787
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0272	0.0262	0.5376	0.4022
A to Z ↑	0.0272	0.0279	0.7355	0.5514
B to Z ↓	0.0272	0.0261	0.5376	0.4022
B to Z ↑	0.0250	0.0255	0.7343	0.5498
C to Z ↓	0.0231	0.0221	0.5292	0.3958
C to Z ↑	0.0246	0.0247	0.7342	0.5498
D to Z ↓	0.0220	0.0212	0.5283	0.3956
D to Z ↑	0.0253	0.0257	0.7341	0.5499

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.938e-05	1.000e-20
X17_P0	4.474e-05	1.000e-20
X25_P0	6.421e-05	1.000e-20
X33_P0	8.636e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	8.943e-05	1.722e-04	2.918e-04	3.249e-04
B (output stable)	9.457e-05	1.900e-04	3.214e-04	3.569e-04
C (output stable)	1.974e-05	4.142e-05	1.028e-04	1.150e-04
D (output stable)	4.581e-05	9.118e-05	2.728e-04	3.000e-04
A to Z	3.021e-03	5.524e-03	8.774e-03	1.107e-02
B to Z	2.900e-03	5.219e-03	8.206e-03	1.032e-02
C to Z	3.155e-03	5.687e-03	9.222e-03	1.139e-02
D to Z	3.050e-03	5.492e-03	8.699e-03	1.086e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

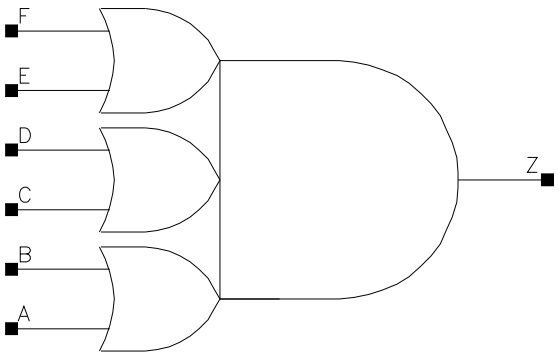
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0007	0.0009	0.0016
B	0.0006	0.0010	0.0018
C	0.0006	0.0009	0.0017
D	0.0007	0.0010	0.0019
E	0.0007	0.0009	0.0017
F	0.0007	0.0010	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0373	0.0319	1.6369	0.7980
A to Z ↑	0.0296	0.0277	2.2148	1.0948
B to Z ↓	0.0384	0.0331	1.6374	0.7981
B to Z ↑	0.0286	0.0268	2.2139	1.0949
C to Z ↓	0.0343	0.0303	1.6286	0.7968
C to Z ↑	0.0306	0.0281	2.2156	1.0948
D to Z ↓	0.0355	0.0313	1.6292	0.7972
D to Z ↑	0.0292	0.0267	2.2135	1.0942
E to Z ↓	0.0300	0.0268	1.6194	0.7936
E to Z ↑	0.0287	0.0270	2.2131	1.0938
F to Z ↓	0.0312	0.0277	1.6200	0.7936
F to Z ↑	0.0274	0.0255	2.2111	1.0927
	X33_P0		X33_P0	
A to Z ↓	0.0321		0.4078	
A to Z ↑	0.0284		0.5516	
B to Z ↓	0.0334		0.4080	
B to Z ↑	0.0264		0.5500	
C to Z ↓	0.0297		0.4060	
C to Z ↑	0.0287		0.5514	
D to Z ↓	0.0308		0.4063	
D to Z ↑	0.0269		0.5498	
E to Z ↓	0.0263		0.4042	
E to Z ↑	0.0277		0.5505	
F to Z ↓	0.0273		0.4044	
F to Z ↑	0.0257		0.5491	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.862e-05	1.000e-20
X17_P0	4.549e-05	1.000e-20
X33_P0	8.585e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	2.552e-05	4.408e-05	8.252e-05
B (output stable)	2.975e-05	5.786e-05	1.032e-04
C (output stable)	5.326e-05	8.510e-05	1.724e-04
D (output stable)	5.839e-05	9.614e-05	1.927e-04
E (output stable)	1.435e-04	2.093e-04	3.991e-04
F (output stable)	1.454e-04	2.163e-04	4.189e-04
A to Z	4.030e-03	6.840e-03	1.344e-02
B to Z	3.888e-03	6.601e-03	1.292e-02
C to Z	3.703e-03	6.396e-03	1.245e-02
D to Z	3.569e-03	6.146e-03	1.193e-02
E to Z	3.299e-03	5.823e-03	1.132e-02
F to Z	3.183e-03	5.595e-03	1.086e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

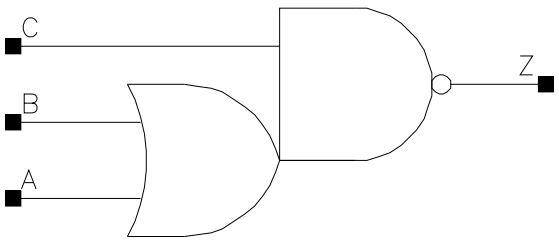
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X34_P0	1.200	2.720	3.2640
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X34_P0	X46_P0
A	0.0007	0.0023	0.0047	0.0061
B	0.0008	0.0021	0.0043	0.0058
C	0.0008	0.0024	0.0050	0.0065

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0099	0.0103	2.9521	0.9659
A to Z ↑	0.0110	0.0116	4.2218	1.4437
B to Z ↓	0.0080	0.0083	2.8820	0.9694
B to Z ↑	0.0112	0.0112	4.2408	1.4517
C to Z ↓	0.0091	0.0091	2.6851	0.8878
C to Z ↑	0.0110	0.0109	2.2555	0.7524
	X34_P0	**X46_P0**	**X34_P0**	**X46_P0**
A to Z ↓	0.0108	0.0108	0.4929	0.3769

A to Z ↑	0.0121	0.0119	0.7214	0.5560
B to Z ↓	0.0087	0.0087	0.5000	0.3840
B to Z ↑	0.0115	0.0116	0.7249	0.5593
C to Z ↓	0.0095	0.0095	0.4556	0.3489
C to Z ↑	0.0111	0.0110	0.3767	0.2892

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P0	1.386e-05	1.000e-20
X17_P0	4.112e-05	1.000e-20
X34_P0	8.069e-05	1.000e-20
X46_P0	1.067e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	9.769e-05	3.282e-04	6.941e-04	8.530e-04
B (output stable)	1.105e-04	3.856e-04	8.415e-04	1.001e-03
C (output stable)	7.116e-05	2.300e-04	4.826e-04	6.088e-04
A to Z	1.432e-03	4.515e-03	9.333e-03	1.210e-02
B to Z	1.219e-03	3.647e-03	7.481e-03	9.771e-03
C to Z	1.729e-03	5.276e-03	1.085e-02	1.407e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

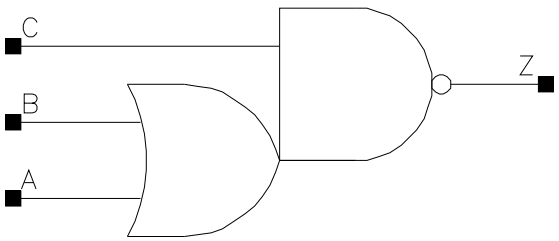
Pin Cycle (vdds)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.544	0.6528
X11_P0	1.200	0.952	1.1424
X17_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X17_P0	X23_P0
A	0.0008	0.0016	0.0024	0.0033
B	0.0008	0.0016	0.0023	0.0030
C	0.0008	0.0016	0.0023	0.0032
	X46_P0			
A	0.0066			
B	0.0061			
C	0.0064			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0099	0.0100	2.9811	1.3899
A to Z ↑	0.0141	0.0140	4.4570	2.1098
B to Z ↓	0.0084	0.0083	2.9257	1.3524

B to Z ↑	0.0144	0.0144	4.4737	2.1177
C to Z ↓	0.0081	0.0082	2.7816	1.2926
C to Z ↑	0.0083	0.0082	2.4315	1.1414
	X17_P0	**X23_P0**	**X17_P0**	**X23_P0**
A to Z ↓	0.0096	0.0103	0.9659	0.7169
A to Z ↑	0.0132	0.0145	1.3968	1.0696
B to Z ↓	0.0080	0.0083	0.9624	0.7164
B to Z ↑	0.0134	0.0140	1.4023	1.0733
C to Z ↓	0.0079	0.0082	0.9086	0.6731
C to Z ↑	0.0076	0.0079	0.7584	0.5786
	X46_P0		**X46_P0**	
A to Z ↓	0.0102		0.3746	
A to Z ↑	0.0141		0.5418	
B to Z ↓	0.0082		0.3706	
B to Z ↑	0.0137		0.5444	
C to Z ↓	0.0083		0.3504	
C to Z ↑	0.0076		0.2933	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.342e-05	1.000e-20
X11_P0	2.863e-05	1.000e-20
X17_P0	4.199e-05	1.000e-20
X23_P0	5.504e-05	1.000e-20
X46_P0	1.073e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	3.380e-05	7.252e-05	1.056e-04	1.890e-04
B (output stable)	3.876e-05	9.016e-05	1.281e-04	2.912e-04
C (output stable)	2.563e-04	6.175e-04	7.486e-04	1.179e-03
A to Z	1.695e-03	3.597e-03	5.053e-03	7.397e-03
B to Z	1.460e-03	3.147e-03	4.315e-03	6.033e-03
C to Z	1.269e-03	2.758e-03	3.866e-03	5.456e-03
	X46_P0			
A (output stable)	3.590e-04			
B (output stable)	5.357e-04			
C (output stable)	2.136e-03			
A to Z	1.427e-02			
B to Z	1.157e-02			
C to Z	1.047e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

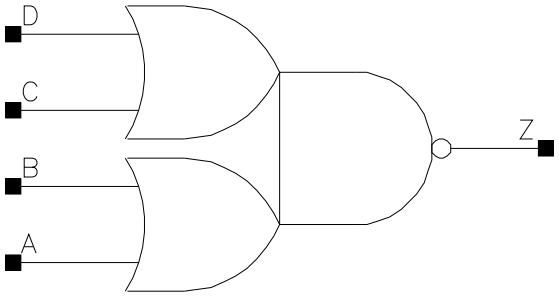
	X46_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0008	0.0016	0.0023	0.0033
B	0.0008	0.0015	0.0022	0.0030
C	0.0007	0.0015	0.0023	0.0032
D	0.0007	0.0014	0.0021	0.0029
	X42_P0			
A	0.0066			
B	0.0061			
C	0.0063			
D	0.0059			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0110	0.0118	2.7502	1.3688
A to Z ↑	0.0166	0.0164	4.7075	2.1584
B to Z ↓	0.0096	0.0100	2.6871	1.3730
B to Z ↑	0.0168	0.0158	4.7158	2.1670
C to Z ↓	0.0100	0.0109	2.7984	1.3800
C to Z ↑	0.0120	0.0125	4.5889	2.1669
D to Z ↓	0.0083	0.0087	2.7168	1.3879
D to Z ↑	0.0121	0.0114	4.6083	2.1796
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0112	0.0115	0.9367	0.6763
A to Z ↑	0.0153	0.0159	1.4557	1.0740
B to Z ↓	0.0097	0.0097	0.9395	0.6756
B to Z ↑	0.0151	0.0156	1.4621	1.0779
C to Z ↓	0.0104	0.0106	0.9471	0.6825
C to Z ↑	0.0114	0.0118	1.4618	1.0761
D to Z ↓	0.0085	0.0085	0.9546	0.6846
D to Z ↑	0.0108	0.0111	1.4709	1.0817
	X42_P0		**X42_P0**	
A to Z ↓	0.0117		0.3557	
A to Z ↑	0.0159		0.5489	
B to Z ↓	0.0099		0.3515	
B to Z ↑	0.0157		0.5510	
C to Z ↓	0.0112		0.3606	
C to Z ↑	0.0120		0.5451	
D to Z ↓	0.0089		0.3566	
D to Z ↑	0.0113		0.5485	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.518e-05	1.000e-20
X10_P0	3.400e-05	1.000e-20
X15_P0	5.001e-05	1.000e-20
X21_P0	6.496e-05	1.000e-20
X42_P0	1.272e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	4.336e-05	1.356e-04	1.735e-04	2.520e-04
B (output stable)	5.766e-05	2.660e-04	2.686e-04	4.427e-04
C (output stable)	9.903e-05	2.619e-04	3.362e-04	4.841e-04
D (output stable)	1.164e-04	3.920e-04	4.327e-04	6.659e-04
A to Z	1.996e-03	4.445e-03	6.104e-03	8.637e-03
B to Z	1.768e-03	3.718e-03	5.132e-03	7.264e-03
C to Z	1.499e-03	3.461e-03	4.677e-03	6.584e-03
D to Z	1.294e-03	2.747e-03	3.793e-03	5.313e-03
	X42_P0			
A (output stable)	4.971e-04			
B (output stable)	8.483e-04			
C (output stable)	9.479e-04			
D (output stable)	1.302e-03			

A to Z	1.703e-02			
B to Z	1.427e-02			
C to Z	1.312e-02			
D to Z	1.055e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

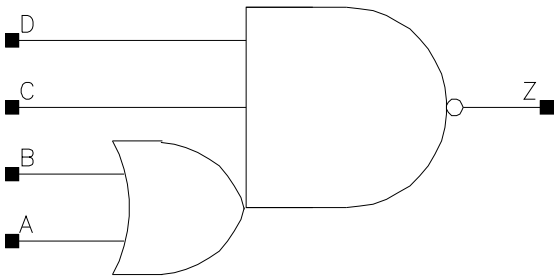
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X21_P0	1.200	2.448	2.9376
X31_P0	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X21_P0	X31_P0
A	0.0008	0.0015	0.0030	0.0045
B	0.0010	0.0014	0.0028	0.0042
C	0.0008	0.0017	0.0033	0.0049
D	0.0008	0.0016	0.0031	0.0047

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0146	0.0141	3.7113	1.9955
A to Z ↑	0.0151	0.0138	4.2528	2.1436
B to Z ↓	0.0128	0.0114	3.7702	2.0052
B to Z ↑	0.0153	0.0129	4.2820	2.1557
C to Z ↓	0.0128	0.0132	3.5154	1.8818

C to Z ↑	0.0134	0.0131	2.2044	1.1116
D to Z ↓	0.0139	0.0132	3.5388	1.8956
D to Z ↑	0.0127	0.0118	2.2388	1.1151
	X21_P0	**X31_P0**	**X21_P0**	**X31_P0**
A to Z ↓	0.0143	0.0145	1.0426	0.7087
A to Z ↑	0.0134	0.0134	1.0709	0.7199
B to Z ↓	0.0117	0.0119	1.0490	0.7155
B to Z ↑	0.0126	0.0126	1.0761	0.7239
C to Z ↓	0.0130	0.0131	0.9844	0.6700
C to Z ↑	0.0128	0.0128	0.5644	0.3823
D to Z ↓	0.0134	0.0136	0.9908	0.6746
D to Z ↑	0.0116	0.0116	0.5655	0.3819

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.218e-05	1.000e-20
X10_P0	2.284e-05	1.000e-20
X21_P0	4.377e-05	1.000e-20
X31_P0	6.472e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	1.688e-04	3.574e-04	6.648e-04	9.778e-04
B (output stable)	1.804e-04	3.835e-04	7.092e-04	1.043e-03
C (output stable)	4.021e-05	1.166e-04	2.228e-04	3.246e-04
D (output stable)	8.639e-05	3.019e-04	5.446e-04	7.860e-04
A to Z	2.036e-03	3.599e-03	6.975e-03	1.037e-02
B to Z	1.687e-03	2.876e-03	5.552e-03	8.294e-03
C to Z	2.415e-03	4.639e-03	8.886e-03	1.318e-02
D to Z	2.213e-03	4.006e-03	7.710e-03	1.146e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

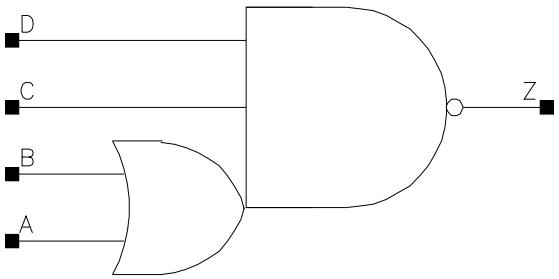
Pin Cycle (vdds)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0008	0.0017	0.0025	0.0033
B	0.0008	0.0015	0.0022	0.0031
C	0.0008	0.0016	0.0024	0.0032
D	0.0008	0.0015	0.0023	0.0030

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0129	0.0140	3.7870	1.9844
A to Z ↑	0.0163	0.0177	4.1116	2.1030
B to Z ↓	0.0114	0.0119	3.7109	1.9867
B to Z ↑	0.0167	0.0172	4.1237	2.1113
C to Z ↓	0.0110	0.0122	3.5812	1.8961

C to Z ↑	0.0104	0.0110	2.2532	1.1393
D to Z ↓	0.0111	0.0118	3.6004	1.9047
D to Z ↑	0.0091	0.0092	2.2702	1.1489
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0138	0.0139	1.3658	1.0317
A to Z ↑	0.0169	0.0173	1.4200	1.0786
B to Z ↓	0.0119	0.0118	1.3582	1.0302
B to Z ↑	0.0167	0.0172	1.4258	1.0822
C to Z ↓	0.0119	0.0122	1.2997	0.9831
C to Z ↑	0.0105	0.0107	0.7613	0.5719
D to Z ↓	0.0116	0.0120	1.3062	0.9876
D to Z ↑	0.0088	0.0091	0.7671	0.5764

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.219e-05	1.000e-20
X10_P0	2.298e-05	1.000e-20
X15_P0	3.319e-05	1.000e-20
X21_P0	4.418e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	2.872e-05	6.256e-05	9.161e-05	1.216e-04
B (output stable)	3.030e-05	9.297e-05	1.121e-04	1.656e-04
C (output stable)	9.257e-05	2.065e-04	3.072e-04	4.100e-04
D (output stable)	1.522e-04	5.270e-04	6.422e-04	9.399e-04
A to Z	2.236e-03	4.812e-03	6.805e-03	9.326e-03
B to Z	1.960e-03	4.024e-03	5.713e-03	7.812e-03
C to Z	1.670e-03	3.626e-03	5.068e-03	7.001e-03
D to Z	1.503e-03	3.125e-03	4.423e-03	6.045e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

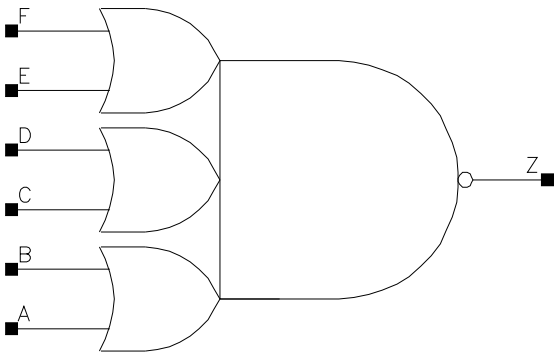
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	1.088	1.3056
X9_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X9_P0
A	0.0007	0.0017
B	0.0007	0.0015
C	0.0007	0.0016
D	0.0006	0.0015
E	0.0007	0.0015
F	0.0007	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X9_P0	X3_P0	X9_P0
A to Z ↓	0.0164	0.0177	4.3623	1.8094
A to Z ↑	0.0224	0.0212	5.7823	2.1156
B to Z ↓	0.0153	0.0158	4.3976	1.8119
B to Z ↑	0.0234	0.0210	5.7963	2.1220
C to Z ↓	0.0162	0.0171	4.4160	1.8255
C to Z ↑	0.0195	0.0182	5.8085	2.1123
D to Z ↓	0.0148	0.0150	4.4538	1.8306
D to Z ↑	0.0203	0.0179	5.8267	2.1213
E to Z ↓	0.0141	0.0153	4.4368	1.8243
E to Z ↑	0.0152	0.0143	5.8329	2.1180
F to Z ↓	0.0128	0.0129	4.4789	1.8293
F to Z ↑	0.0158	0.0135	5.8628	2.1300

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	1.185e-05	1.000e-20
X9_P0	3.809e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X9_P0
A (output stable)	3.481e-05	1.221e-04
B (output stable)	4.132e-05	2.064e-04
C (output stable)	7.398e-05	2.141e-04
D (output stable)	8.134e-05	3.016e-04
E (output stable)	1.852e-04	4.614e-04
F (output stable)	1.933e-04	5.409e-04
A to Z	2.499e-03	6.531e-03
B to Z	2.306e-03	5.734e-03
C to Z	2.063e-03	5.375e-03
D to Z	1.886e-03	4.675e-03
E to Z	1.585e-03	4.305e-03
F to Z	1.429e-03	3.585e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

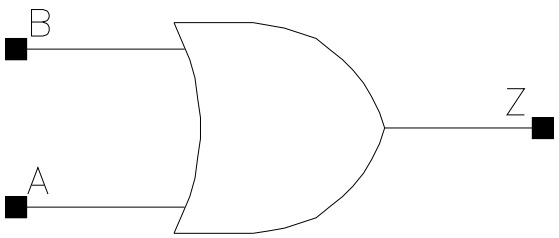
Pin Cycle (vdds)	X3_P0	X9_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X33_P0	1.200	1.360	1.6320
X50_P0	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P0	X16_P0	X33_P0	X50_P0
A	0.0008	0.0009	0.0018	0.0019
B	0.0006	0.0009	0.0018	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0254	0.0222	1.5841	0.7988
A to Z ↑	0.0164	0.0175	2.1667	1.0947
B to Z ↓	0.0260	0.0228	1.5838	0.7994
B to Z ↑	0.0154	0.0163	2.1666	1.0947
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0229	0.0272	0.3958	0.2716
A to Z ↑	0.0175	0.0175	0.5332	0.3616
B to Z ↓	0.0227	0.0273	0.3959	0.2716
B to Z ↑	0.0159	0.0162	0.5321	0.3607

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.151e-05	1.000e-20
X16_P0	2.598e-05	1.000e-20
X33_P0	5.113e-05	1.000e-20
X50_P0	6.493e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	2.716e-05	5.016e-05	1.653e-04	1.570e-04
B (output stable)	4.330e-05	7.571e-05	3.754e-04	3.504e-04
A to Z	2.673e-03	4.466e-03	9.326e-03	1.312e-02
B to Z	2.553e-03	4.265e-03	8.612e-03	1.249e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

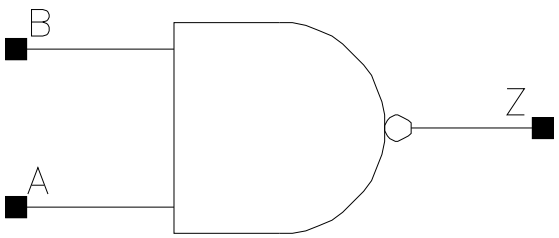
Pin Cycle (vdds)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X16_P0	1.200	0.952	1.1424
X24_P0	1.200	1.088	1.3056
X32_P0	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P0	X16_P0	X24_P0	X32_P0
A	0.0009	0.0009	0.0010	0.0009
B	0.0010	0.0010	0.0010	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0220	0.0227	1.5493	0.8074
A to Z ↑	0.0235	0.0242	2.2080	1.1281
B to Z ↓	0.0231	0.0239	1.5489	0.8071
B to Z ↑	0.0224	0.0226	2.2048	1.1293
	X24_P0	**X32_P0**	**X24_P0**	**X32_P0**
A to Z ↓	0.0249	0.0260	0.5449	0.4068
A to Z ↑	0.0258	0.0264	0.7551	0.5635
B to Z ↓	0.0260	0.0273	0.5445	0.4072
B to Z ↑	0.0242	0.0254	0.7542	0.5635

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	3.359e-05	1.000e-20
X16_P0	4.095e-05	1.000e-20
X24_P0	4.802e-05	1.000e-20
X32_P0	7.002e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	3.146e-05	3.154e-05	3.164e-05	3.288e-05
B (output stable)	5.406e-05	5.435e-05	5.445e-05	5.880e-05
A to Z	5.006e-03	5.848e-03	7.417e-03	9.810e-03
B to Z	4.846e-03	5.695e-03	7.275e-03	9.668e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

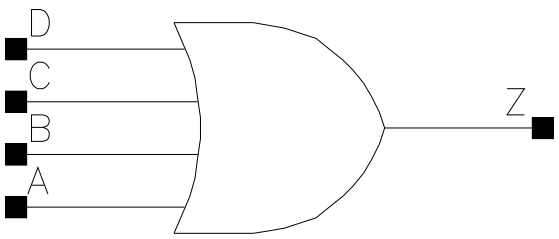
Pin Cycle (vdds)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X27_P0
A	0.0016	0.0019
B	0.0015	0.0019
C	0.0016	0.0019
D	0.0015	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	X27_P0	X20_P0	X27_P0
A to Z ↓	0.0257	0.0268	0.9352	0.6993
A to Z ↑	0.0179	0.0174	0.7155	0.5326
B to Z ↓	0.0258	0.0266	0.9362	0.6996
B to Z ↑	0.0169	0.0159	0.7157	0.5317
C to Z ↓	0.0249	0.0262	0.9341	0.6985
C to Z ↑	0.0171	0.0172	0.7169	0.5339
D to Z ↓	0.0249	0.0261	0.9337	0.6982
D to Z ↑	0.0160	0.0158	0.7154	0.5338

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X20_P0	4.045e-05	1.000e-20
X27_P0	6.018e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X20_P0	X27_P0
A (output stable)	1.872e-03	2.593e-03
B (output stable)	1.713e-03	2.381e-03
C (output stable)	1.744e-03	2.526e-03
D (output stable)	1.586e-03	2.353e-03
A to Z	8.093e-03	1.130e-02
B to Z	7.593e-03	1.052e-02
C to Z	7.333e-03	1.018e-02
D to Z	6.836e-03	9.491e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

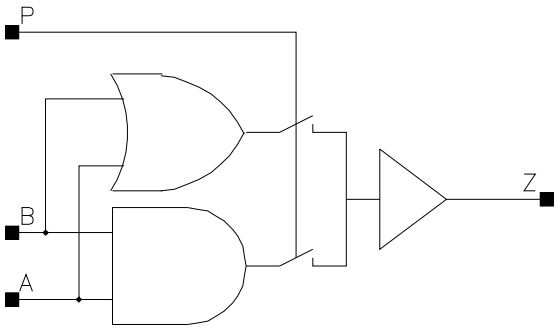
Pin Cycle (vdds)	X20_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X16_P0	1.200	1.224	1.4688
X25_P0	1.200	2.040	2.4480
X33_P0	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0012	0.0017	0.0030	0.0030
B	0.0011	0.0017	0.0035	0.0035
P	0.0006	0.0009	0.0018	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0308	0.0279	1.6090	0.7878
A to Z ↑	0.0219	0.0211	2.2067	1.1033
B to Z ↓	0.0308	0.0281	1.6155	0.7924
B to Z ↑	0.0227	0.0217	2.2091	1.1059
P to Z ↓	0.0286	0.0265	1.6140	0.7912
P to Z ↑	0.0221	0.0212	2.2064	1.1031
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**

A to Z ↓	0.0266	0.0285	0.5366	0.4055
A to Z ↑	0.0207	0.0220	0.7441	0.5563
B to Z ↓	0.0267	0.0284	0.5394	0.4071
B to Z ↑	0.0218	0.0229	0.7444	0.5571
P to Z ↓	0.0257	0.0276	0.5384	0.4068
P to Z ↑	0.0209	0.0221	0.7429	0.5555

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.633e-05	1.000e-20
X16_P0	3.923e-05	1.000e-20
X25_P0	6.600e-05	1.000e-20
X33_P0	7.733e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	6.479e-05	1.042e-04	2.246e-04	2.246e-04
B (output stable)	8.090e-05	1.424e-04	3.754e-04	3.752e-04
P (output stable)	1.896e-04	3.365e-04	5.262e-04	5.387e-04
A to Z	3.079e-03	5.431e-03	9.082e-03	1.088e-02
B to Z	3.010e-03	5.352e-03	8.798e-03	1.061e-02
P to Z	2.812e-03	5.080e-03	8.497e-03	1.031e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

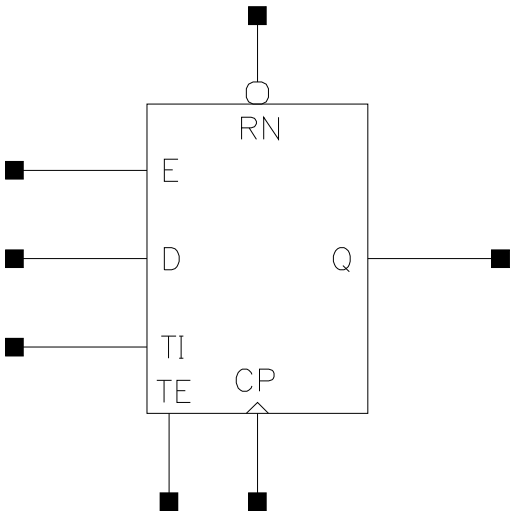
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.488	5.3856
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0006	0.0006	0.0006
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0007	0.0007	0.0008
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0543	0.0306	3.3150	1.5630
CP to Q ↑	0.0472	0.0405	4.4597	2.1839
RN to Q ↓	0.0476	0.0415	2.9565	1.6161
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0525	0.0552	0.7691	0.4033
CP to Q ↑	0.0648	0.0677	1.0701	0.5468
RN to Q ↓	0.0688	0.0714	0.7681	0.4030

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0717	0.0488	0.0488	0.0488
CP ↑	min_pulse_width to CP	0.0505	0.0271	0.0271	0.0271
D ↓	hold_rising to CP	-0.0750	-0.0310	-0.0310	-0.0310
D ↑	hold_rising to CP	-0.0484	-0.0120	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1096	0.0657	0.0657	0.0657
D ↑	setup_rising to CP	0.0724	0.0390	0.0390	0.0390
E ↓	hold_rising to CP	-0.0474	-0.0533	-0.0533	-0.0533
E ↑	hold_rising to CP	-0.0409	-0.0089	-0.0089	-0.0089
E ↓	setup_rising to CP	0.0918	0.0895	0.0895	0.0895
E ↑	setup_rising to CP	0.1004	0.0683	0.0683	0.0683
RN ↓	min_pulse_width to RN	0.0518	0.0566	0.0496	0.0496
RN ↑	recovery_rising to CP	0.0151	0.0097	0.0097	0.0097
RN ↑	removal_rising to CP	-0.0077	-0.0029	-0.0029	-0.0029
TE ↓	hold_rising to CP	-0.0337	-0.0186	-0.0186	-0.0186
TE ↑	hold_rising to CP	-0.0283	-0.0164	-0.0164	-0.0164
TE ↓	setup_rising to CP	0.0680	0.0582	0.0582	0.0582
TE ↑	setup_rising to CP	0.1248	0.0879	0.0879	0.0879
TI ↓	hold_rising to CP	-0.0941	-0.0475	-0.0475	-0.0475
TI ↑	hold_rising to CP	-0.0334	-0.0146	-0.0146	-0.0146
TI ↓	setup_rising to CP	0.1287	0.0820	0.0820	0.0820
TI ↑	setup_rising to CP	0.0617	0.0453	0.0453	0.0453

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.996e-05	1.000e-20
X8_P0	4.948e-05	1.000e-20
X17_P0	6.842e-05	1.000e-20
X33_P0	9.859e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

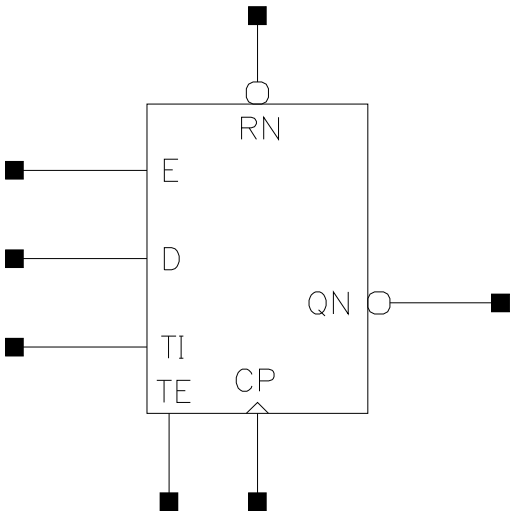
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	9.184e-03	9.231e-03	9.242e-03	9.248e-03
Clock 100Mhz Data 25Mhz	9.904e-03	9.962e-03	1.068e-02	1.162e-02
Clock 100Mhz Data 50Mhz	1.062e-02	1.069e-02	1.212e-02	1.400e-02
Clock = 0 Data 100Mhz	6.923e-03	6.522e-03	6.387e-03	6.321e-03
Clock = 1 Data 100Mhz	2.409e-03	2.449e-03	2.463e-03	2.470e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.624	5.5488
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0006	0.0006	0.0006
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
CP to QN ↓	0.0578	0.0545	2.9137	1.5150
CP to QN ↑	0.0613	0.0408	4.3651	2.1124
RN to QN ↑	0.0584	0.0584	4.3511	2.1120
	X17_P0	X33_P0	X17_P0	X33_P0
CP to QN ↓	0.0518	0.0546	0.7693	0.4022
CP to QN ↑	0.0418	0.0454	1.0691	0.5475
RN to QN ↑	0.0565	0.0621	1.0693	0.5470

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0717	0.0488	0.0488	0.0488
CP ↑	min_pulse_width to CP	0.0370	0.0271	0.0271	0.0271
D ↓	hold_rising to CP	-0.0750	-0.0310	-0.0310	-0.0310
D ↑	hold_rising to CP	-0.0484	-0.0120	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1096	0.0657	0.0657	0.0653
D ↑	setup_rising to CP	0.0724	0.0390	0.0390	0.0390
E ↓	hold_rising to CP	-0.0474	-0.0533	-0.0533	-0.0533
E ↑	hold_rising to CP	-0.0409	-0.0089	-0.0089	-0.0089
E ↓	setup_rising to CP	0.0950	0.0895	0.0895	0.0895
E ↑	setup_rising to CP	0.1004	0.0683	0.0683	0.0711
RN ↓	min_pulse_width to RN	0.0469	0.0496	0.0566	0.0588
RN ↑	recovery_rising to CP	0.0151	0.0125	0.0097	0.0097
RN ↑	removal_rising to CP	-0.0077	-0.0055	-0.0029	-0.0029
TE ↓	hold_rising to CP	-0.0337	-0.0186	-0.0186	-0.0191
TE ↑	hold_rising to CP	-0.0283	-0.0164	-0.0164	-0.0164
TE ↓	setup_rising to CP	0.0680	0.0582	0.0582	0.0582
TE ↑	setup_rising to CP	0.1248	0.0879	0.0879	0.0879
TI ↓	hold_rising to CP	-0.0941	-0.0475	-0.0475	-0.0475
TI ↑	hold_rising to CP	-0.0334	-0.0146	-0.0146	-0.0146
TI ↓	setup_rising to CP	0.1287	0.0820	0.0820	0.0820
TI ↑	setup_rising to CP	0.0624	0.0453	0.0453	0.0453

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.891e-05	1.000e-20
X8_P0	4.490e-05	1.000e-20
X17_P0	6.046e-05	1.000e-20
X33_P0	8.318e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

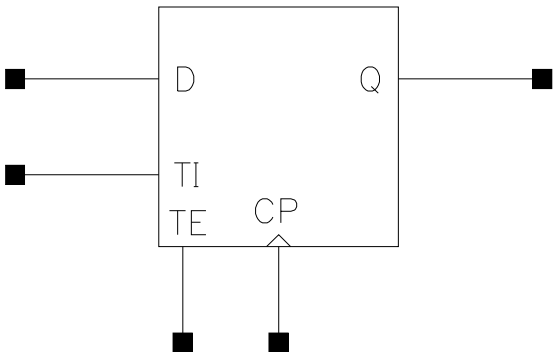
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	9.183e-03	9.229e-03	9.233e-03	9.235e-03
Clock 100Mhz Data 25Mhz	9.800e-03	9.994e-03	1.064e-02	1.158e-02
Clock 100Mhz Data 50Mhz	1.042e-02	1.076e-02	1.204e-02	1.392e-02
Clock = 0 Data 100Mhz	6.925e-03	6.523e-03	6.389e-03	6.324e-03
Clock = 1 Data 100Mhz	2.407e-03	2.449e-03	2.464e-03	2.473e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.400	4.0800
X8_P0	1.200	3.128	3.7536
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0450	0.0286	3.1503	1.5697
CP to Q ↑	0.0423	0.0369	4.4792	2.1519
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0431	0.0469	0.7567	0.3961
CP to Q ↑	0.0611	0.0646	1.0714	0.5477

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0647	0.0679	0.0679	0.0679
CP ↑	min_pulse_width to CP	0.0365	0.0224	0.0224	0.0224
D ↓	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0132	0.0058	0.0058	0.0058
D ↓	setup_rising to CP	0.0728	0.0467	0.0467	0.0467
D ↑	setup_rising to CP	0.0412	0.0217	0.0217	0.0249
TE ↓	hold_rising to CP	-0.0262	-0.0098	-0.0094	-0.0094
TE ↑	hold_rising to CP	-0.0213	-0.0093	-0.0088	-0.0088
TE ↓	setup_rising to CP	0.0610	0.0441	0.0441	0.0441
TE ↑	setup_rising to CP	0.1096	0.0911	0.0911	0.0911
TI ↓	hold_rising to CP	-0.0889	-0.0521	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0221	-0.0097	-0.0097	-0.0097
TI ↓	setup_rising to CP	0.1187	0.0884	0.0884	0.0884
TI ↑	setup_rising to CP	0.0527	0.0361	0.0361	0.0361

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.290e-05	1.000e-20
X8_P0	4.284e-05	1.000e-20
X17_P0	6.719e-05	1.000e-20
X33_P0	8.815e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

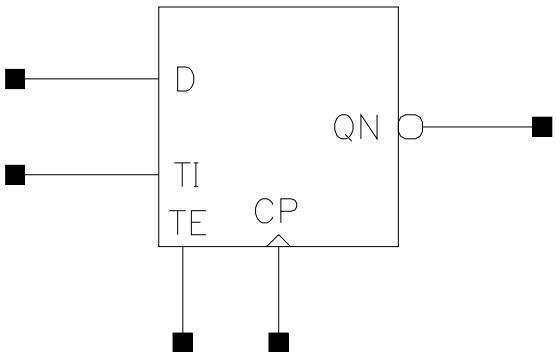
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	8.306e-03	8.407e-03	8.433e-03	8.447e-03
Clock 100Mhz Data 25Mhz	8.332e-03	8.435e-03	9.162e-03	9.973e-03
Clock 100Mhz Data 50Mhz	8.359e-03	8.463e-03	9.891e-03	1.150e-02
Clock = 0 Data 100Mhz	5.381e-03	4.989e-03	4.860e-03	4.797e-03
Clock = 1 Data 100Mhz	1.368e-03	7.130e-04	4.947e-04	3.855e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.536	4.2432
X8_P0	1.200	3.264	3.9168
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0534	0.0559	3.3096	1.5498
CP to QN ↑	0.0491	0.0376	4.4431	2.1195
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0443	0.0487	0.7573	0.3964
CP to QN ↑	0.0368	0.0406	1.0690	0.5467

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0630	0.0679	0.0679	0.0679
CP ↑	min_pulse_width to CP	0.0283	0.0224	0.0223	0.0254
D ↓	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0132	0.0058	0.0058	0.0058
D ↓	setup_rising to CP	0.0728	0.0467	0.0467	0.0467
D ↑	setup_rising to CP	0.0412	0.0217	0.0217	0.0217
TE ↓	hold_rising to CP	-0.0262	-0.0098	-0.0098	-0.0098
TE ↑	hold_rising to CP	-0.0213	-0.0088	-0.0088	-0.0088
TE ↓	setup_rising to CP	0.0578	0.0441	0.0441	0.0441
TE ↑	setup_rising to CP	0.1102	0.0911	0.0911	0.0911
TI ↓	hold_rising to CP	-0.0889	-0.0521	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0237	-0.0097	-0.0097	-0.0097
TI ↓	setup_rising to CP	0.1187	0.0884	0.0884	0.0884
TI ↑	setup_rising to CP	0.0527	0.0361	0.0361	0.0361

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.335e-05	1.000e-20
X8_P0	4.311e-05	1.000e-20
X17_P0	6.623e-05	1.000e-20
X33_P0	8.720e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

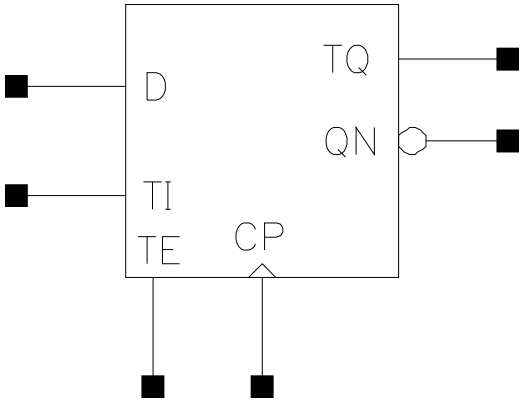
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	8.225e-03	8.364e-03	8.406e-03	8.427e-03
Clock 100Mhz Data 25Mhz	8.262e-03	8.527e-03	9.101e-03	9.941e-03
Clock 100Mhz Data 50Mhz	8.298e-03	8.689e-03	9.796e-03	1.146e-02
Clock = 0 Data 100Mhz	5.408e-03	5.001e-03	4.868e-03	4.802e-03
Clock = 1 Data 100Mhz	1.360e-03	7.088e-04	4.918e-04	3.834e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.536	4.2432
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0012	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010

TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0592	0.0514	3.0123	1.5321
CP to QN ↑	0.0590	0.0388	4.3776	2.1336
CP to TQ ↓	0.0416	0.0263	4.0421	2.8549
CP to TQ ↑	0.0435	0.0368	8.1524	5.8676
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0488	0.0526	0.7730	0.4049
CP to QN ↑	0.0399	0.0428	1.0848	0.5590
CP to TQ ↓	0.0271	0.0281	3.8096	3.8155
CP to TQ ↑	0.0374	0.0383	7.5738	7.9986

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0647	0.0679	0.0679	0.0679
CP ↑	min_pulse_width to CP	0.0365	0.0224	0.0236	0.0271
D ↓	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0132	0.0058	0.0058	0.0058
D ↓	setup_rising to CP	0.0728	0.0467	0.0467	0.0467
D ↑	setup_rising to CP	0.0416	0.0217	0.0217	0.0249
TE ↓	hold_rising to CP	-0.0230	-0.0098	-0.0098	-0.0098
TE ↑	hold_rising to CP	-0.0213	-0.0088	-0.0088	-0.0088
TE ↓	setup_rising to CP	0.0578	0.0441	0.0441	0.0441
TE ↑	setup_rising to CP	0.1102	0.0911	0.0911	0.0911
TI ↓	hold_rising to CP	-0.0889	-0.0521	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0221	-0.0097	-0.0097	-0.0097
TI ↓	setup_rising to CP	0.1189	0.0884	0.0884	0.0884
TI ↑	setup_rising to CP	0.0527	0.0361	0.0361	0.0361

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.520e-05	1.000e-20
X8_P0	4.718e-05	1.000e-20
X17_P0	6.084e-05	1.000e-20
X33_P0	8.533e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0

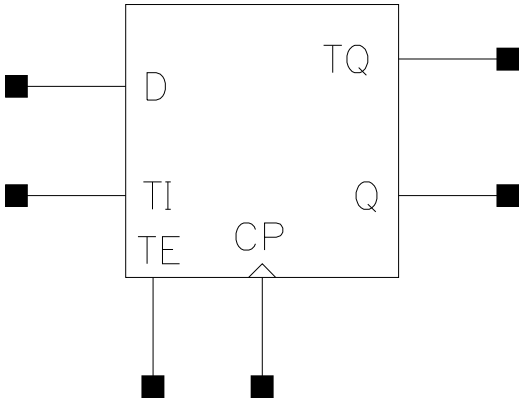
Clock 100Mhz Data 0Mhz	8.419e-03	8.466e-03	8.481e-03	8.490e-03
Clock 100Mhz Data 25Mhz	8.635e-03	8.835e-03	9.174e-03	1.013e-02
Clock 100Mhz Data 50Mhz	8.850e-03	9.203e-03	9.867e-03	1.177e-02
Clock = 0 Data 100Mhz	5.402e-03	5.008e-03	4.877e-03	4.812e-03
Clock = 1 Data 100Mhz	1.369e-03	7.136e-04	4.950e-04	3.858e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.400	4.0800
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007

TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0591	0.0320	3.2899	1.5549
CP to Q ↑	0.0485	0.0392	4.5378	2.1670
CP to TQ ↓	0.0561	0.0326	3.2751	3.9064
CP to TQ ↑	0.0497	0.0429	5.9547	8.1446
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0441	0.0481	0.7786	0.4045
CP to Q ↑	0.0622	0.0656	1.0968	0.5509
CP to TQ ↓	0.0456	0.0499	3.7932	3.8596
CP to TQ ↑	0.0660	0.0709	7.8880	7.9934

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0654	0.0679	0.0679	0.0679
CP ↑	min_pulse_width to CP	0.0518	0.0271	0.0224	0.0224
D ↓	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0132	0.0058	0.0058	0.0058
D ↓	setup_rising to CP	0.0728	0.0467	0.0467	0.0467
D ↑	setup_rising to CP	0.0412	0.0217	0.0217	0.0217
TE ↓	hold_rising to CP	-0.0262	-0.0098	-0.0094	-0.0094
TE ↑	hold_rising to CP	-0.0213	-0.0093	-0.0088	-0.0088
TE ↓	setup_rising to CP	0.0610	0.0441	0.0441	0.0441
TE ↑	setup_rising to CP	0.1096	0.0911	0.0911	0.0911
TI ↓	hold_rising to CP	-0.0889	-0.0521	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0221	-0.0097	-0.0097	-0.0097
TI ↓	setup_rising to CP	0.1187	0.0884	0.0884	0.0884
TI ↑	setup_rising to CP	0.0527	0.0361	0.0361	0.0361

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.575e-05	1.000e-20
X8_P0	4.418e-05	1.000e-20
X17_P0	6.801e-05	1.000e-20
X33_P0	8.894e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

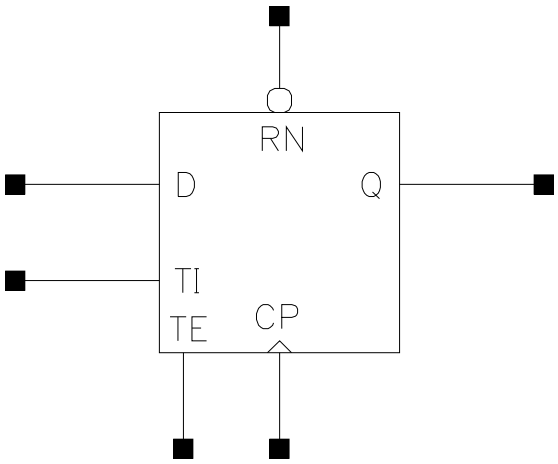
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	8.275e-03	8.388e-03	8.422e-03	8.440e-03
Clock 100Mhz Data 25Mhz	8.790e-03	8.688e-03	9.363e-03	1.024e-02
Clock 100Mhz Data 50Mhz	9.305e-03	8.989e-03	1.030e-02	1.203e-02
Clock = 0 Data 100Mhz	5.377e-03	4.987e-03	4.860e-03	4.796e-03
Clock = 1 Data 100Mhz	1.358e-03	7.078e-04	4.912e-04	3.829e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.672	4.4064
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
RN	0.0008	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0540	0.0305	3.3558	1.5677
CP to Q ↑	0.0469	0.0397	4.4764	2.1827
RN to Q ↓	0.0472	0.0422	2.9931	1.6072
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0450	0.0491	0.7646	0.4020
CP to Q ↑	0.0573	0.0607	1.0652	0.5450
RN to Q ↓	0.0617	0.0659	0.7633	0.4012

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0701	0.0696	0.0708	0.0708
CP ↑	min_pulse_width to CP	0.0471	0.0271	0.0224	0.0224
D ↓	hold_rising to CP	-0.0382	-0.0071	-0.0071	-0.0071
D ↑	hold_rising to CP	-0.0181	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0728	0.0409	0.0409	0.0409
D ↑	setup_rising to CP	0.0487	0.0266	0.0298	0.0298
RN ↓	min_pulse_width to RN	0.0469	0.0518	0.0474	0.0496
RN ↑	recovery_rising to CP	0.0151	0.0129	0.0129	0.0129
RN ↑	removal_rising to CP	-0.0104	-0.0029	-0.0029	-0.0029
TE ↓	hold_rising to CP	-0.0230	-0.0017	-0.0049	-0.0049
TE ↑	hold_rising to CP	-0.0288	-0.0142	-0.0163	-0.0163
TE ↓	setup_rising to CP	0.0577	0.0430	0.0430	0.0430
TE ↑	setup_rising to CP	0.1074	0.0830	0.0862	0.0862
TI ↓	hold_rising to CP	-0.0791	-0.0383	-0.0383	-0.0383
TI ↑	hold_rising to CP	-0.0328	-0.0162	-0.0162	-0.0162
TI ↓	setup_rising to CP	0.1131	0.0819	0.0835	0.0835
TI ↑	setup_rising to CP	0.0582	0.0450	0.0450	0.0450

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.808e-05	1.000e-20
X8_P0	4.603e-05	1.000e-20
X17_P0	6.934e-05	1.000e-20
X33_P0	9.534e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	9.180e-03	9.258e-03	9.324e-03	9.359e-03

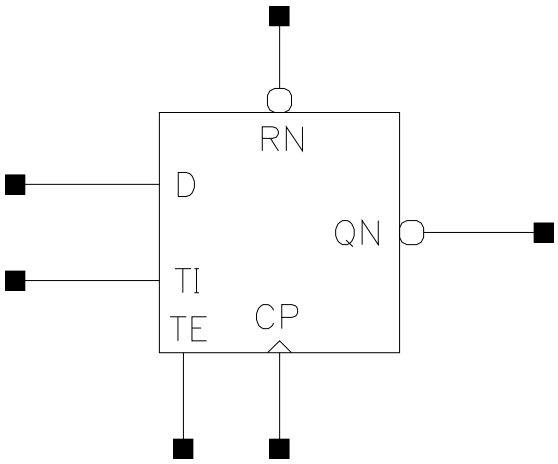
Clock 100Mhz Data 25Mhz	9.319e-03	9.245e-03	1.004e-02	1.090e-02
Clock 100Mhz Data 50Mhz	9.458e-03	9.232e-03	1.077e-02	1.244e-02
Clock = 0 Data 100Mhz	5.420e-03	4.950e-03	4.797e-03	4.721e-03
Clock = 1 Data 100Mhz	1.394e-03	7.276e-04	5.056e-04	3.948e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	3.944	4.7328
X33_P0	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0523	0.0486	2.8571	1.4835
CP to QN ↑	0.0557	0.0366	4.3593	2.1035
RN to QN ↑	0.0539	0.0547	4.3485	2.1014
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0480	0.0526	0.7649	0.4018
CP to QN ↑	0.0398	0.0440	1.0775	0.5535
RN to QN ↑	0.0553	0.0605	1.0813	0.5554

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0701	0.0679	0.0696	0.0696
CP ↑	min_pulse_width to CP	0.0364	0.0224	0.0271	0.0271
D ↓	hold_rising to CP	-0.0382	-0.0071	-0.0071	-0.0071
D ↑	hold_rising to CP	-0.0181	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0728	0.0414	0.0409	0.0409
D ↑	setup_rising to CP	0.0487	0.0266	0.0266	0.0266
RN ↓	min_pulse_width to RN	0.0469	0.0474	0.0566	0.0588
RN ↑	recovery_rising to CP	0.0151	0.0151	0.0125	0.0125
RN ↑	removal_rising to CP	-0.0077	-0.0055	-0.0055	-0.0055
TE ↓	hold_rising to CP	-0.0230	-0.0049	-0.0017	-0.0017
TE ↑	hold_rising to CP	-0.0288	-0.0137	-0.0137	-0.0137
TE ↓	setup_rising to CP	0.0577	0.0430	0.0430	0.0430
TE ↑	setup_rising to CP	0.1074	0.0830	0.0862	0.0862
TI ↓	hold_rising to CP	-0.0784	-0.0426	-0.0390	-0.0390
TI ↑	hold_rising to CP	-0.0326	-0.0162	-0.0162	-0.0162
TI ↓	setup_rising to CP	0.1131	0.0819	0.0835	0.0835
TI ↑	setup_rising to CP	0.0582	0.0450	0.0450	0.0450

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.745e-05	1.000e-20
X8_P0	4.145e-05	1.000e-20
X17_P0	6.467e-05	1.000e-20
X33_P0	8.043e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	9.101e-03	9.216e-03	9.253e-03	9.272e-03

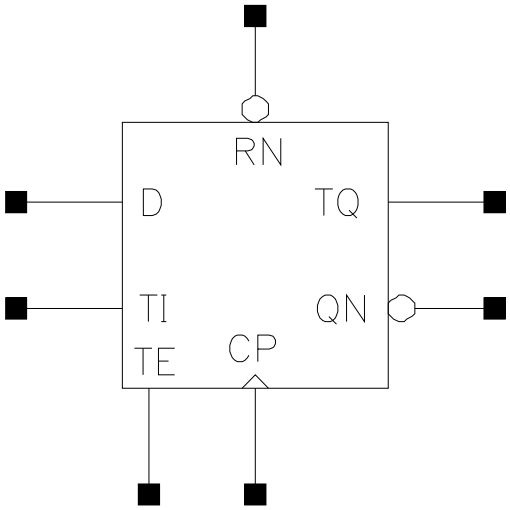
Clock 100Mhz Data 25Mhz	9.100e-03	9.210e-03	9.916e-03	1.077e-02
Clock 100Mhz Data 50Mhz	9.098e-03	9.205e-03	1.058e-02	1.228e-02
Clock = 0 Data 100Mhz	5.411e-03	4.944e-03	4.794e-03	4.719e-03
Clock = 1 Data 100Mhz	1.392e-03	7.265e-04	5.049e-04	3.941e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007

RN	0.0010	0.0007	0.0008	0.0008
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0581	0.0505	2.8667	1.5696
CP to QN ↑	0.0712	0.0406	3.9093	2.1955
CP to TQ ↓	0.0510	0.0278	3.5676	2.9811
CP to TQ ↑	0.0485	0.0401	6.6573	6.1831
RN to QN ↑	0.0529	0.0529	3.9371	2.1893
RN to TQ ↓	0.0370	0.0364	3.2811	3.0836
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0521	0.0561	0.7795	0.4105
CP to QN ↑	0.0410	0.0433	1.1005	0.5565
CP to TQ ↓	0.0289	0.0297	3.7254	3.6411
CP to TQ ↑	0.0400	0.0409	5.8096	5.8928
RN to QN ↑	0.0547	0.0582	1.0983	0.5554
RN to TQ ↓	0.0389	0.0404	3.8226	3.7527

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0701	0.0696	0.0708	0.0708
CP ↑	min_pulse_width to CP	0.0471	0.0236	0.0236	0.0271
D ↓	hold_rising to CP	-0.0382	-0.0071	-0.0071	-0.0071
D ↑	hold_rising to CP	-0.0181	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0728	0.0414	0.0409	0.0409
D ↑	setup_rising to CP	0.0487	0.0266	0.0298	0.0298
RN ↓	min_pulse_width to RN	0.0518	0.0518	0.0518	0.0566
RN ↑	recovery_rising to CP	0.0151	0.0129	0.0129	0.0129
RN ↑	removal_rising to CP	-0.0103	-0.0055	-0.0055	-0.0055
TE ↓	hold_rising to CP	-0.0230	-0.0017	-0.0017	-0.0017
TE ↑	hold_rising to CP	-0.0288	-0.0137	-0.0137	-0.0137
TE ↓	setup_rising to CP	0.0577	0.0430	0.0430	0.0430
TE ↑	setup_rising to CP	0.1074	0.0830	0.0830	0.0830
TI ↓	hold_rising to CP	-0.0784	-0.0390	-0.0383	-0.0383
TI ↑	hold_rising to CP	-0.0326	-0.0162	-0.0162	-0.0162
TI ↓	setup_rising to CP	0.1131	0.0819	0.0835	0.0835
TI ↑	setup_rising to CP	0.0582	0.0450	0.0450	0.0450

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	4.264e-05	1.000e-20
X8_P0	4.411e-05	1.000e-20
X17_P0	5.549e-05	1.000e-20
X33_P0	7.549e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

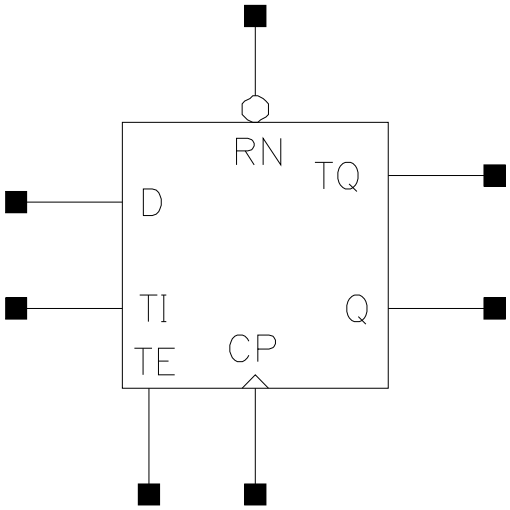
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	9.106e-03	9.215e-03	9.298e-03	9.340e-03
Clock 100Mhz Data 25Mhz	9.417e-03	9.394e-03	9.854e-03	1.086e-02
Clock 100Mhz Data 50Mhz	9.727e-03	9.573e-03	1.041e-02	1.237e-02
Clock = 0 Data 100Mhz	5.410e-03	4.944e-03	4.789e-03	4.711e-03
Clock = 1 Data 100Mhz	1.392e-03	7.266e-04	5.049e-04	3.941e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007

RN	0.0009	0.0008	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0605	0.0331	3.5353	1.6106
CP to Q ↑	0.0499	0.0415	4.6673	2.2727
CP to TQ ↓	0.0569	0.0325	4.4481	3.9400
CP to TQ ↑	0.0515	0.0435	8.9091	8.1180
RN to Q ↓	0.0486	0.0476	3.1372	1.6518
RN to TQ ↓	0.0475	0.0456	3.9981	4.0432
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0468	0.0509	0.7743	0.4073
CP to Q ↑	0.0582	0.0615	1.0723	0.5486
CP to TQ ↓	0.0483	0.0533	3.8190	3.8784
CP to TQ ↑	0.0619	0.0671	7.9984	8.0437
RN to Q ↓	0.0635	0.0675	0.7744	0.4072
RN to TQ ↓	0.0650	0.0700	3.8136	3.8792

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0701	0.0696	0.0696	0.0696
CP ↑	min_pulse_width to CP	0.0552	0.0271	0.0224	0.0224
D ↓	hold_rising to CP	-0.0382	-0.0071	-0.0071	-0.0071
D ↑	hold_rising to CP	-0.0181	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0728	0.0409	0.0414	0.0414
D ↑	setup_rising to CP	0.0487	0.0266	0.0266	0.0266
RN ↓	min_pulse_width to RN	0.0518	0.0588	0.0474	0.0496
RN ↑	recovery_rising to CP	0.0125	0.0125	0.0129	0.0129
RN ↑	removal_rising to CP	-0.0078	-0.0055	-0.0055	-0.0055
TE ↓	hold_rising to CP	-0.0230	-0.0017	-0.0049	-0.0049
TE ↑	hold_rising to CP	-0.0288	-0.0142	-0.0137	-0.0137
TE ↓	setup_rising to CP	0.0577	0.0430	0.0430	0.0430
TE ↑	setup_rising to CP	0.1074	0.0830	0.0830	0.0830
TI ↓	hold_rising to CP	-0.0791	-0.0390	-0.0383	-0.0383
TI ↑	hold_rising to CP	-0.0328	-0.0162	-0.0162	-0.0162
TI ↓	setup_rising to CP	0.1131	0.0819	0.0819	0.0819
TI ↑	setup_rising to CP	0.0582	0.0450	0.0450	0.0450

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.894e-05	1.000e-20
X8_P0	4.778e-05	1.000e-20
X17_P0	6.986e-05	1.000e-20
X33_P0	9.589e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

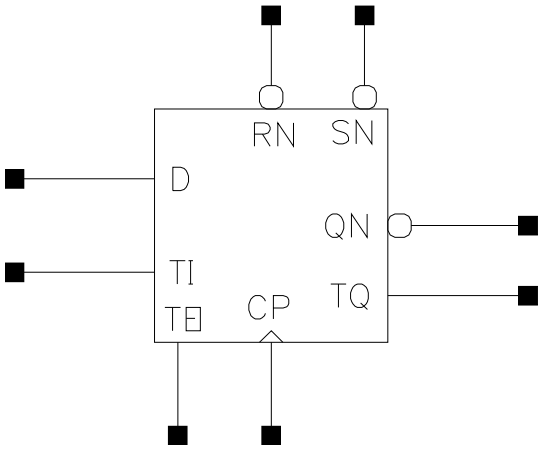
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	9.163e-03	9.244e-03	9.270e-03	9.283e-03
Clock 100Mhz Data 25Mhz	9.544e-03	9.428e-03	1.021e-02	1.109e-02
Clock 100Mhz Data 50Mhz	9.924e-03	9.612e-03	1.116e-02	1.289e-02
Clock = 0 Data 100Mhz	5.418e-03	4.949e-03	4.793e-03	4.715e-03
Clock = 1 Data 100Mhz	1.394e-03	7.276e-04	5.057e-04	3.947e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.352	5.2224
X17_P0	1.200	4.488	5.3856
X33_P0	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009
D	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
CP to QN ↓	0.0561	0.0594	1.5148	0.7791
CP to QN ↑	0.0419	0.0439	2.1187	1.0782
CP to TQ ↓	0.0323	0.0322	4.6995	4.7101
CP to TQ ↑	0.0467	0.0466	10.2276	10.2431
RN to QN ↓	0.0609	0.0641	1.5164	0.7798
RN to QN ↑	0.0584	0.0613	2.1216	1.0778
RN to TQ ↓	0.0451	0.0449	4.9667	4.9690
RN to TQ ↑	0.0516	0.0516	10.1982	10.2093
SN to QN ↓	0.0645	0.0685	1.5225	0.7822
SN to TQ ↑	0.0538	0.0537	10.3371	10.3554
	X33_P0		X33_P0	
CP to QN ↓	0.0677		0.4121	
CP to QN ↑	0.0490		0.5525	
CP to TQ ↓	0.0323		4.7149	
CP to TQ ↑	0.0468		10.2574	
RN to QN ↓	0.0722		0.4119	
RN to QN ↑	0.0679		0.5521	
RN to TQ ↓	0.0448		4.9827	
RN to TQ ↑	0.0518		10.2352	
SN to QN ↓	0.0778		0.4128	
SN to TQ ↑	0.0538		10.3948	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0743	0.0743	0.0743
CP ↑	min_pulse_width to CP	0.0271	0.0271	0.0270
D ↓	hold_rising to CP	-0.0071	-0.0071	-0.0071
D ↑	hold_rising to CP	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0467	0.0467	0.0467
D ↑	setup_rising to CP	0.0298	0.0298	0.0298
RN ↓	min_pulse_width to RN	0.0566	0.0588	0.0615
RN ↑	non_seq_hold_rising to SN	-0.0188	-0.0188	-0.0211
RN ↑	non_seq_setup_rising to SN	0.0496	0.0496	0.0496
RN ↑	recovery_rising to CP	0.0200	0.0200	0.0200
RN ↑	removal_rising to CP	-0.0119	-0.0119	-0.0119
SN ↓	min_pulse_width to SN	0.0500	0.0500	0.0527
SN ↑	recovery_rising to CP	0.0028	0.0028	0.0028
SN ↑	removal_rising to CP	0.0237	0.0237	0.0237

TE ↓	hold_rising to CP	-0.0049	-0.0049	-0.0049
TE ↑	hold_rising to CP	-0.0142	-0.0142	-0.0142
TE ↓	setup_rising to CP	0.0463	0.0463	0.0463
TE ↑	setup_rising to CP	0.0879	0.0879	0.0879
TI ↓	hold_rising to CP	-0.0426	-0.0426	-0.0426
TI ↑	hold_rising to CP	-0.0162	-0.0162	-0.0162
TI ↓	setup_rising to CP	0.0868	0.0868	0.0868
TI ↑	setup_rising to CP	0.0450	0.0450	0.0450

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	4.927e-05	1.000e-20
X17_P0	5.861e-05	1.000e-20
X33_P0	7.650e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

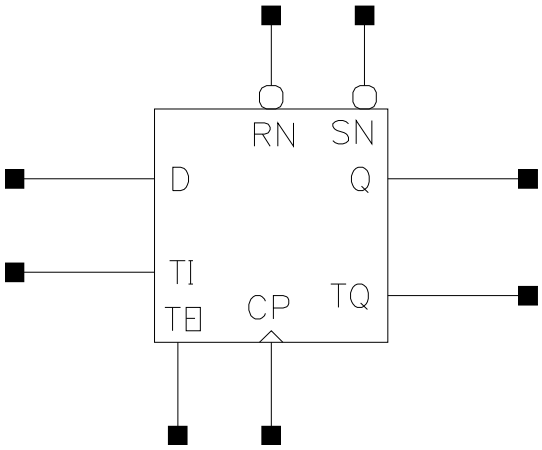
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	9.785e-03	9.785e-03	9.786e-03
Clock 100Mhz Data 25Mhz	9.844e-03	1.025e-02	1.140e-02
Clock 100Mhz Data 50Mhz	9.902e-03	1.072e-02	1.301e-02
Clock = 0 Data 100Mhz	4.637e-03	4.638e-03	4.638e-03
Clock = 1 Data 100Mhz	6.185e-05	6.196e-05	6.207e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.216	5.0592
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009
D	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
CP to Q ↓	0.0360	0.0402	1.5587	0.8076
CP to Q ↑	0.0456	0.0482	2.1761	1.1092
CP to TQ ↓	0.0360	0.0402	4.7697	4.8225
CP to TQ ↑	0.0500	0.0548	10.0994	10.1881
RN to Q ↓	0.0536	0.0619	1.7033	0.8822
RN to Q ↑	0.0416	0.0473	2.2442	1.1495
RN to TQ ↓	0.0520	0.0595	5.0693	5.1624
RN to TQ ↑	0.0483	0.0576	10.1922	10.2774
SN to Q ↑	0.0545	0.0601	2.2440	1.1492
SN to TQ ↑	0.0612	0.0702	10.2001	10.2767
	X33_P0		X33_P0	
CP to Q ↓	0.0507		0.4316	
CP to Q ↑	0.0555		0.5773	
CP to TQ ↓	0.0476		4.9803	
CP to TQ ↑	0.0639		10.3208	
RN to Q ↓	0.0814		0.4762	
RN to Q ↑	0.0613		0.6005	
RN to TQ ↓	0.0731		5.4213	
RN to TQ ↑	0.0755		10.4145	
SN to Q ↑	0.0737		0.6012	
SN to TQ ↑	0.0878		10.4199	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0743	0.0743	0.0725
CP ↑	min_pulse_width to CP	0.0283	0.0330	0.0424
D ↓	hold_rising to CP	-0.0071	-0.0071	-0.0071
D ↑	hold_rising to CP	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0467	0.0467	0.0467
D ↑	setup_rising to CP	0.0298	0.0298	0.0298
RN ↓	min_pulse_width to RN	0.0637	0.0735	0.0952
RN ↑	non_seq_hold_rising to SN	-0.0237	-0.0286	-0.0385
RN ↑	non_seq_setup_rising to SN	0.0474	0.0474	0.0650
RN ↑	recovery_rising to CP	0.0174	0.0174	0.0174
RN ↑	removal_rising to CP	-0.0103	-0.0103	-0.0103
SN ↓	min_pulse_width to SN	0.0527	0.0625	0.0771
SN ↑	recovery_rising to CP	0.0028	0.0028	0.0028
SN ↑	removal_rising to CP	0.0237	0.0237	0.0237

TE ↓	hold_rising to CP	-0.0049	-0.0049	-0.0049
TE ↑	hold_rising to CP	-0.0142	-0.0142	-0.0142
TE ↓	setup_rising to CP	0.0463	0.0463	0.0463
TE ↑	setup_rising to CP	0.0879	0.0879	0.0879
TI ↓	hold_rising to CP	-0.0426	-0.0426	-0.0383
TI ↑	hold_rising to CP	-0.0169	-0.0153	-0.0153
TI ↓	setup_rising to CP	0.0868	0.0868	0.0884
TI ↑	setup_rising to CP	0.0466	0.0466	0.0466

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	5.210e-05	1.000e-20
X17_P0	6.440e-05	1.000e-20
X33_P0	8.847e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

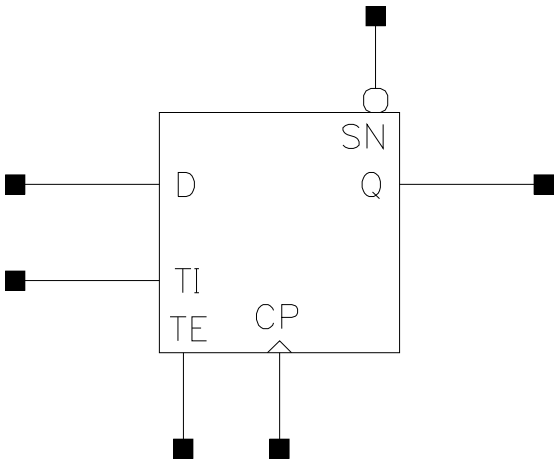
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	9.771e-03	9.771e-03	9.772e-03
Clock 100Mhz Data 25Mhz	9.804e-03	1.038e-02	1.201e-02
Clock 100Mhz Data 50Mhz	9.838e-03	1.099e-02	1.424e-02
Clock = 0 Data 100Mhz	4.636e-03	4.636e-03	4.637e-03
Clock = 1 Data 100Mhz	6.177e-05	6.183e-05	6.201e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004
SN	0.0014	0.0014	0.0014	0.0014
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0009			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0540	0.0316	3.3603	1.5516
CP to Q ↑	0.0486	0.0418	4.5146	2.1654
SN to Q ↑	0.0373	0.0429	4.4079	2.1634
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
CP to Q ↓	0.0445	0.0465	0.7647	0.5303
CP to Q ↑	0.0579	0.0597	1.0665	0.7251
SN to Q ↑	0.0585	0.0603	1.0666	0.7259
	X33_P0		**X33_P0**	
CP to Q ↓	0.0483		0.4024	
CP to Q ↑	0.0610		0.5462	
SN to Q ↑	0.0616		0.5457	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.0748	0.0749	0.0749	0.0749
CP ↑	min_pulse_width to CP	0.0471	0.0271	0.0224	0.0224
D ↓	hold_rising to CP	-0.0408	-0.0067	-0.0062	-0.0062
D ↑	hold_rising to CP	-0.0185	-0.0001	-0.0001	-0.0001
D ↓	setup_rising to CP	0.0755	0.0457	0.0457	0.0457
D ↑	setup_rising to CP	0.0432	0.0245	0.0245	0.0245
SN ↓	min_pulse_width to SN	0.0354	0.0403	0.0376	0.0376
SN ↑	recovery_rising to CP	0.0028	0.0028	0.0028	0.0028
SN ↑	removal_rising to CP	0.0163	0.0238	0.0238	0.0238
TE ↓	hold_rising to CP	-0.0289	-0.0045	-0.0045	-0.0045
TE ↑	hold_rising to CP	-0.0230	-0.0114	-0.0114	-0.0114
TE ↓	setup_rising to CP	0.0636	0.0441	0.0467	0.0467
TE ↑	setup_rising to CP	0.1123	0.0911	0.0911	0.0911
TI ↓	hold_rising to CP	-0.0843	-0.0432	-0.0475	-0.0475
TI ↑	hold_rising to CP	-0.0270	-0.0110	-0.0110	-0.0110
TI ↓	setup_rising to CP	0.1187	0.0877	0.0877	0.0877
TI ↑	setup_rising to CP	0.0576	0.0402	0.0402	0.0402
		X33_P0			

CP ↓	min_pulse_width to CP	0.0749			
CP ↑	min_pulse_width to CP	0.0224			
D ↓	hold_rising to CP	-0.0062			
D ↑	hold_rising to CP	-0.0001			
D ↓	setup_rising to CP	0.0457			
D ↑	setup_rising to CP	0.0245			
SN ↓	min_pulse_width to SN	0.0376			
SN ↑	recovery_rising to CP	0.0028			
SN ↑	removal_rising to CP	0.0238			
TE ↓	hold_rising to CP	-0.0045			
TE ↑	hold_rising to CP	-0.0114			
TE ↓	setup_rising to CP	0.0441			
TE ↑	setup_rising to CP	0.0911			
TI ↓	hold_rising to CP	-0.0432			
TI ↑	hold_rising to CP	-0.0110			
TI ↓	setup_rising to CP	0.0877			
TI ↑	setup_rising to CP	0.0402			

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.493e-05	1.000e-20
X8_P0	4.346e-05	1.000e-20
X17_P0	6.599e-05	1.000e-20
X25_P0	7.388e-05	1.000e-20
X33_P0	8.175e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	8.927e-03	9.170e-03	9.252e-03	9.292e-03
Clock 100Mhz Data 25Mhz	9.106e-03	9.253e-03	9.997e-03	1.042e-02
Clock 100Mhz Data 50Mhz	9.286e-03	9.336e-03	1.074e-02	1.154e-02
Clock = 0 Data 100Mhz	5.171e-03	4.840e-03	4.731e-03	4.677e-03
Clock = 1 Data 100Mhz	1.393e-03	7.271e-04	5.052e-04	3.943e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	9.316e-03			

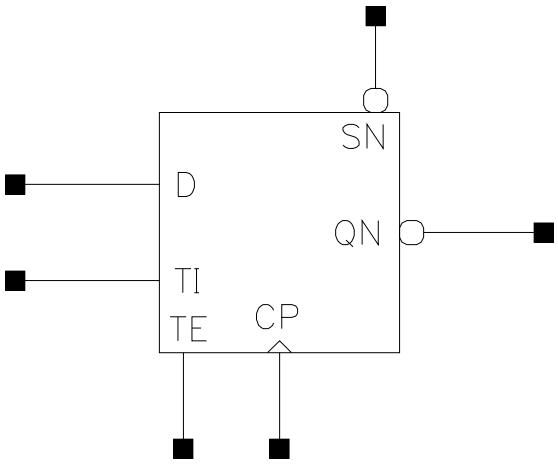
Clock 100Mhz Data 25Mhz	1.083e-02			
Clock 100Mhz Data 50Mhz	1.234e-02			
Clock = 0 Data 100Mhz	4.643e-03			
Clock = 1 Data 100Mhz	3.278e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004
SN	0.0014	0.0014	0.0014	0.0014
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0009			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0544	0.0491	2.8596	1.4860
CP to QN ↑	0.0560	0.0363	4.3446	2.1138
SN to QN ↓	0.0440	0.0497	2.8510	1.4862
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
CP to QN ↓	0.0514	0.0541	0.7668	0.5318
CP to QN ↑	0.0423	0.0447	1.0676	0.7266
SN to QN ↓	0.0530	0.0557	0.7674	0.5317
	X33_P0		**X33_P0**	
CP to QN ↓	0.0561		0.4033	
CP to QN ↑	0.0464		0.5467	
SN to QN ↓	0.0577		0.4031	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.0748	0.0749	0.0749	0.0749
CP ↑	min_pulse_width to CP	0.0365	0.0224	0.0271	0.0271
D ↓	hold_rising to CP	-0.0403	-0.0062	-0.0062	-0.0067
D ↑	hold_rising to CP	-0.0185	-0.0001	-0.0001	-0.0001
D ↓	setup_rising to CP	0.0755	0.0457	0.0457	0.0457
D ↑	setup_rising to CP	0.0432	0.0245	0.0245	0.0245
SN ↓	min_pulse_width to SN	0.0327	0.0376	0.0425	0.0425
SN ↑	recovery_rising to CP	0.0028	0.0028	0.0028	0.0028
SN ↑	removal_rising to CP	0.0163	0.0212	0.0238	0.0238
TE ↓	hold_rising to CP	-0.0289	-0.0071	-0.0045	-0.0045
TE ↑	hold_rising to CP	-0.0230	-0.0114	-0.0114	-0.0114
TE ↓	setup_rising to CP	0.0636	0.0441	0.0467	0.0467
TE ↑	setup_rising to CP	0.1123	0.0911	0.0906	0.0906
TI ↓	hold_rising to CP	-0.0843	-0.0475	-0.0432	-0.0432
TI ↑	hold_rising to CP	-0.0270	-0.0110	-0.0110	-0.0110
TI ↓	setup_rising to CP	0.1187	0.0877	0.0874	0.0874
TI ↑	setup_rising to CP	0.0576	0.0402	0.0402	0.0417
		X33_P0			

CP ↓	min_pulse_width to CP	0.0749			
CP ↑	min_pulse_width to CP	0.0271			
D ↓	hold_rising to CP	-0.0067			
D ↑	hold_rising to CP	-0.0001			
D ↓	setup_rising to CP	0.0457			
D ↑	setup_rising to CP	0.0245			
SN ↓	min_pulse_width to SN	0.0425			
SN ↑	recovery_rising to CP	0.0028			
SN ↑	removal_rising to CP	0.0238			
TE ↓	hold_rising to CP	-0.0045			
TE ↑	hold_rising to CP	-0.0114			
TE ↓	setup_rising to CP	0.0467			
TE ↑	setup_rising to CP	0.0906			
TI ↓	hold_rising to CP	-0.0432			
TI ↑	hold_rising to CP	-0.0110			
TI ↓	setup_rising to CP	0.0877			
TI ↑	setup_rising to CP	0.0417			

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.611e-05	1.000e-20
X8_P0	4.839e-05	1.000e-20
X17_P0	7.119e-05	1.000e-20
X25_P0	8.418e-05	1.000e-20
X33_P0	9.720e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	8.928e-03	9.184e-03	9.261e-03	9.300e-03
Clock 100Mhz Data 25Mhz	8.913e-03	9.164e-03	1.007e-02	1.053e-02
Clock 100Mhz Data 50Mhz	8.899e-03	9.145e-03	1.088e-02	1.175e-02
Clock = 0 Data 100Mhz	5.172e-03	4.845e-03	4.734e-03	4.679e-03
Clock = 1 Data 100Mhz	1.393e-03	7.270e-04	5.052e-04	3.943e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	9.324e-03			

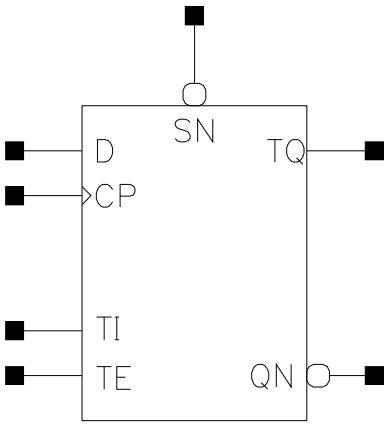
Clock 100Mhz Data 25Mhz	1.095e-02			
Clock 100Mhz Data 50Mhz	1.257e-02			
Clock = 0 Data 100Mhz	4.645e-03			
Clock = 1 Data 100Mhz	3.278e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.216	5.0592
X8_P0	1.200	4.080	4.8960
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004

SN	0.0014	0.0016	0.0015	0.0015
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0622	0.0512	2.8602	1.4976
CP to QN ↑	0.0713	0.0407	4.2947	2.1616
CP to TQ ↓	0.0519	0.0282	4.0161	3.4814
CP to TQ ↑	0.0483	0.0392	5.9435	5.7689
SN to QN ↓	0.0389	0.0398	2.8605	1.4975
SN to TQ ↑	0.0277	0.0288	5.8186	5.7482
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0512	0.0560	0.7915	0.3993
CP to QN ↑	0.0451	0.0496	1.0824	0.5529
CP to TQ ↓	0.0343	0.0342	3.5941	3.6018
CP to TQ ↑	0.0438	0.0438	5.8372	5.8502
SN to QN ↓	0.0386	0.0428	0.7911	0.3989
SN to TQ ↑	0.0368	0.0366	5.8273	5.8459

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0748	0.0749	0.0756	0.0756
CP ↑	min_pulse_width to CP	0.0471	0.0236	0.0284	0.0284
D ↓	hold_rising to CP	-0.0408	-0.0062	-0.0062	-0.0062
D ↑	hold_rising to CP	-0.0185	-0.0001	-0.0001	-0.0001
D ↓	setup_rising to CP	0.0755	0.0457	0.0457	0.0457
D ↑	setup_rising to CP	0.0465	0.0245	0.0245	0.0245
SN ↓	min_pulse_width to SN	0.0305	0.0305	0.0332	0.0332
SN ↑	recovery_rising to CP	0.0032	0.0032	0.0028	0.0028
SN ↑	removal_rising to CP	0.0163	0.0212	0.0212	0.0212
TE ↓	hold_rising to CP	-0.0289	-0.0071	-0.0045	-0.0045
TE ↑	hold_rising to CP	-0.0230	-0.0114	-0.0114	-0.0114
TE ↓	setup_rising to CP	0.0636	0.0441	0.0467	0.0467
TE ↑	setup_rising to CP	0.1123	0.0911	0.0906	0.0906
TI ↓	hold_rising to CP	-0.0843	-0.0475	-0.0432	-0.0432
TI ↑	hold_rising to CP	-0.0270	-0.0110	-0.0110	-0.0110
TI ↓	setup_rising to CP	0.1187	0.0877	0.0874	0.0874
TI ↑	setup_rising to CP	0.0576	0.0402	0.0402	0.0402

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	4.153e-05	1.000e-20
X8_P0	5.373e-05	1.000e-20
X17_P0	7.652e-05	1.000e-20
X33_P0	1.025e-04	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

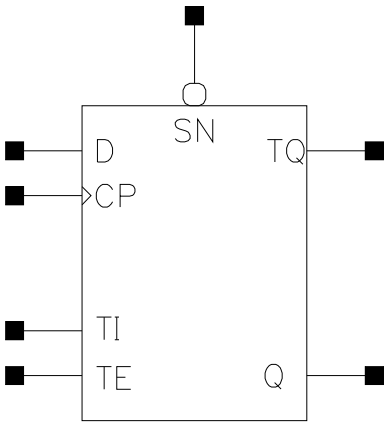
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	8.937e-03	9.183e-03	9.266e-03	9.309e-03
Clock 100Mhz Data 25Mhz	9.329e-03	9.428e-03	1.027e-02	1.115e-02
Clock 100Mhz Data 50Mhz	9.722e-03	9.672e-03	1.128e-02	1.299e-02
Clock = 0 Data 100Mhz	5.184e-03	4.852e-03	4.742e-03	4.687e-03
Clock = 1 Data 100Mhz	1.393e-03	7.272e-04	5.053e-04	3.944e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.944	4.7328
X17_P0	1.200	4.216	5.0592
X33_P0	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004

SN	0.0015	0.0014	0.0014	0.0014
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0613	0.0340	3.4307	1.5834
CP to Q ↑	0.0517	0.0434	4.5283	2.1976
CP to TQ ↓	0.0608	0.0345	5.0100	3.9583
CP to TQ ↑	0.0506	0.0476	5.9914	8.1972
SN to Q ↑	0.0292	0.0449	4.3893	2.1901
SN to TQ ↑	0.0284	0.0497	5.8432	8.1810
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0452	0.0494	0.7853	0.4094
CP to Q ↑	0.0585	0.0618	1.0709	0.5476
CP to TQ ↓	0.0467	0.0518	3.8148	3.8745
CP to TQ ↑	0.0622	0.0675	8.0031	8.0473
SN to Q ↑	0.0591	0.0624	1.0732	0.5487
SN to TQ ↑	0.0627	0.0680	8.0064	8.0495

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0748	0.0749	0.0749	0.0749
CP ↑	min_pulse_width to CP	0.0552	0.0271	0.0224	0.0224
D ↓	hold_rising to CP	-0.0408	-0.0067	-0.0062	-0.0062
D ↑	hold_rising to CP	-0.0185	-0.0001	-0.0001	-0.0001
D ↓	setup_rising to CP	0.0755	0.0457	0.0457	0.0457
D ↑	setup_rising to CP	0.0465	0.0245	0.0245	0.0245
SN ↓	min_pulse_width to SN	0.0305	0.0452	0.0376	0.0376
SN ↑	recovery_rising to CP	0.0032	0.0028	0.0028	0.0028
SN ↑	removal_rising to CP	0.0163	0.0238	0.0212	0.0238
TE ↓	hold_rising to CP	-0.0289	-0.0045	-0.0071	-0.0045
TE ↑	hold_rising to CP	-0.0230	-0.0114	-0.0114	-0.0114
TE ↓	setup_rising to CP	0.0636	0.0441	0.0441	0.0467
TE ↑	setup_rising to CP	0.1123	0.0911	0.0911	0.0911
TI ↓	hold_rising to CP	-0.0843	-0.0432	-0.0475	-0.0475
TI ↑	hold_rising to CP	-0.0270	-0.0110	-0.0110	-0.0110
TI ↓	setup_rising to CP	0.1187	0.0877	0.0877	0.0877
TI ↑	setup_rising to CP	0.0576	0.0417	0.0402	0.0402

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.976e-05	1.000e-20
X8_P0	4.454e-05	1.000e-20
X17_P0	6.683e-05	1.000e-20
X33_P0	8.258e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

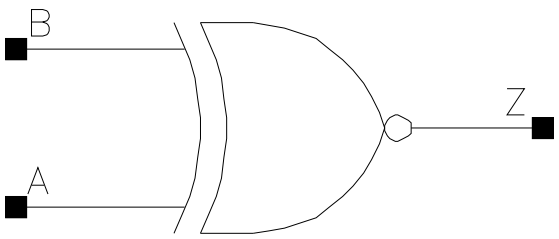
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	8.928e-03	9.175e-03	9.254e-03	9.294e-03
Clock 100Mhz Data 25Mhz	9.407e-03	9.477e-03	1.018e-02	1.109e-02
Clock 100Mhz Data 50Mhz	9.887e-03	9.779e-03	1.110e-02	1.289e-02
Clock = 0 Data 100Mhz	5.184e-03	4.848e-03	4.736e-03	4.680e-03
Clock = 1 Data 100Mhz	1.393e-03	7.272e-04	5.054e-04	3.945e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P0	X8_P0	X17_P0	X25_P0
A	0.0015	0.0007	0.0009	0.0014
B	0.0014	0.0014	0.0018	0.0024
	X33_P0			
A	0.0016			
B	0.0027			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X8_P0**	**X6_P0**	**X8_P0**
A to Z ↓	0.0157	0.0343	2.7622	1.6091
A to Z ↑	0.0161	0.0315	3.3609	2.2420
B to Z ↓	0.0148	0.0238	2.7628	1.5950
B to Z ↑	0.0167	0.0225	3.3673	2.2336
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
A to Z ↓	0.0326	0.0329	0.7905	0.5451
A to Z ↑	0.0290	0.0291	1.0982	0.7321

B to Z ↓	0.0246	0.0238	0.7876	0.5435
B to Z ↑	0.0226	0.0218	1.0956	0.7300
	X33_P0		**X33_P0**	
A to Z ↓	0.0313		0.4088	
A to Z ↑	0.0284		0.5505	
B to Z ↓	0.0230		0.4080	
B to Z ↑	0.0217		0.5494	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P0	3.251e-05	1.000e-20
X8_P0	3.159e-05	1.000e-20
X17_P0	6.064e-05	1.000e-20
X25_P0	9.034e-05	1.000e-20
X33_P0	1.351e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	2.888e-03	5.392e-03	8.015e-03	1.254e-02
B to Z	2.836e-03	3.867e-03	6.336e-03	9.702e-03
	X33_P0			
A to Z	1.553e-02			
B to Z	1.245e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

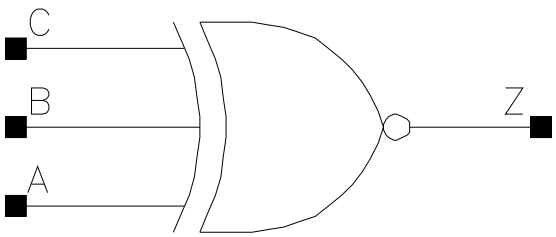
Pin Cycle (vdds)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	2.176	2.6112
X16_P0	1.200	2.720	3.2640
X25_P0	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X16_P0	X25_P0
A	0.0026	0.0022	0.0027	0.0040
B	0.0030	0.0021	0.0027	0.0037
C	0.0018	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0239	0.0390	3.2418	1.6956
A to Z ↑	0.0227	0.0361	4.7835	2.2169
B to Z ↓	0.0247	0.0393	3.2465	1.6961
B to Z ↑	0.0230	0.0365	4.7849	2.2178
C to Z ↓	0.0243	0.0515	3.2533	1.6944
C to Z ↑	0.0223	0.0483	4.7877	2.2157
	X16_P0	**X25_P0**	**X16_P0**	**X25_P0**
A to Z ↓	0.0392	0.0397	0.8700	0.5573
A to Z ↑	0.0392	0.0390	1.1643	0.7339
B to Z ↓	0.0397	0.0407	0.8702	0.5576

B to Z ↑	0.0396	0.0401	1.1640	0.7343
C to Z ↓	0.0545	0.0585	0.8695	0.5571
C to Z ↑	0.0536	0.0575	1.1642	0.7335

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	2.940e-05	1.000e-20
X8_P0	2.762e-05	1.000e-20
X16_P0	5.292e-05	1.000e-20
X25_P0	7.540e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	2.944e-03	4.137e-03	6.918e-03	1.060e-02
B to Z	3.000e-03	4.115e-03	6.938e-03	1.069e-02
C to Z	2.968e-03	6.159e-03	9.331e-03	1.420e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

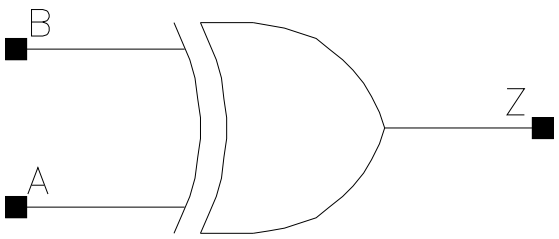
Pin Cycle (vdds)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.224	1.4688
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.224	1.4688
X16_P0	1.200	1.360	1.6320
X25_P0	1.200	2.176	2.6112
X31_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X16_P0
A	0.0007	0.0014	0.0010	0.0011
B	0.0012	0.0013	0.0014	0.0015
	X25_P0	X31_P0		
A	0.0014	0.0018		
B	0.0025	0.0032		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0307	0.0151	2.9003	2.1395
A to Z ↑	0.0295	0.0168	4.2671	4.2360
B to Z ↓	0.0223	0.0157	2.8866	2.1532
B to Z ↑	0.0223	0.0157	4.2646	4.2358
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0275	0.0289	1.5754	0.8143

A to Z ↑	0.0254	0.0270	2.1717	1.0988
B to Z ↓	0.0215	0.0225	1.5698	0.8121
B to Z ↑	0.0204	0.0217	2.1703	1.0970
	X25_P0	**X31_P0**	**X25_P0**	**X31_P0**
A to Z ↓	0.0308	0.0290	0.5409	0.4330
A to Z ↑	0.0283	0.0269	0.7299	0.5902
B to Z ↓	0.0234	0.0218	0.5405	0.4330
B to Z ↑	0.0215	0.0206	0.7291	0.5905

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	2.391e-05	1.000e-20
X6_P0	2.866e-05	1.000e-20
X8_P0	4.329e-05	1.000e-20
X16_P0	7.369e-05	1.000e-20
X25_P0	9.117e-05	1.000e-20
X31_P0	1.391e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	3.980e-03	2.831e-03	4.938e-03	7.430e-03
B to Z	3.168e-03	2.749e-03	4.214e-03	6.383e-03
	X25_P0	X31_P0		
A to Z	1.172e-02	1.442e-02		
B to Z	9.039e-03	1.118e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

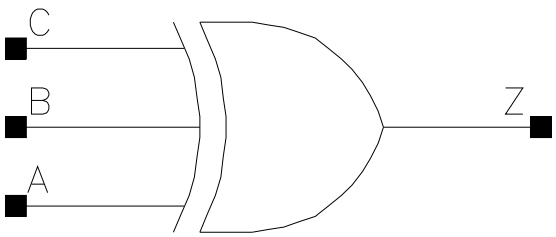
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P0	X31_P0		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X24_P0	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X24_P0
A	0.0022	0.0022	0.0027	0.0049
B	0.0023	0.0021	0.0025	0.0041
C	0.0007	0.0015	0.0021	0.0032

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0244	0.0390	3.4183	1.6950
A to Z ↑	0.0231	0.0361	5.2422	2.2138
B to Z ↓	0.0249	0.0393	3.4237	1.6960
B to Z ↑	0.0234	0.0365	5.2416	2.2141
C to Z ↓	0.0415	0.0384	3.3930	1.6952
C to Z ↑	0.0405	0.0355	5.2123	2.2148
	X17_P0	**X24_P0**	**X17_P0**	**X24_P0**
A to Z ↓	0.0359	0.0418	0.8118	0.5833
A to Z ↑	0.0359	0.0323	1.0798	0.7366
B to Z ↓	0.0361	0.0421	0.8119	0.5833

B to Z ↑	0.0362	0.0326	1.0801	0.7373
C to Z ↓	0.0358	0.0410	0.8122	0.5832
C to Z ↑	0.0358	0.0324	1.0799	0.7370

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	3.106e-05	1.000e-20
X8_P0	2.363e-05	1.000e-20
X17_P0	5.244e-05	1.000e-20
X24_P0	7.665e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	2.800e-03	4.137e-03	6.665e-03	1.121e-02
B to Z	2.852e-03	4.114e-03	6.671e-03	1.119e-02
C to Z	5.564e-03	4.055e-03	6.669e-03	1.114e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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