C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG User Manual

1.8 V IO general purpose library in standard frame designed using 28 nm FDSOI technology

Overview

The C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG library is designed using standard frame in 28 nm FDSOI technology.

All the bidirectional cells are PVT compensated and therefore, need the compensation cell, C28SOI_IO_EXT_CSF_COMPENSATION1V8_
LR_EG*, to compensate the IO for PVT variations in 1.8 V signaling environment. In 1.5/ 1.2 V signaling environment, compensation cell is not required but ASRC rails in IO ring need to be hardcoded at fixed logic.

Highlights

- General purpose 1.8 V/1.5 V full swing CMOS logic
- 1.2 V MDIO application
- Cells are designed to operate in 1.8 V and 1.5 V signaling environment complying with EIA/JESD8-7 standard
- Uses LVT# devices in GO1 and GO2
- Metallization option support as per product package

Product name contains LR due to legacy reasons although only LVT devices are used.

Information Snapshot

Process Options

- 16 Å GO1 oxide: LVT
- 28 Å GO2 oxide: LVT

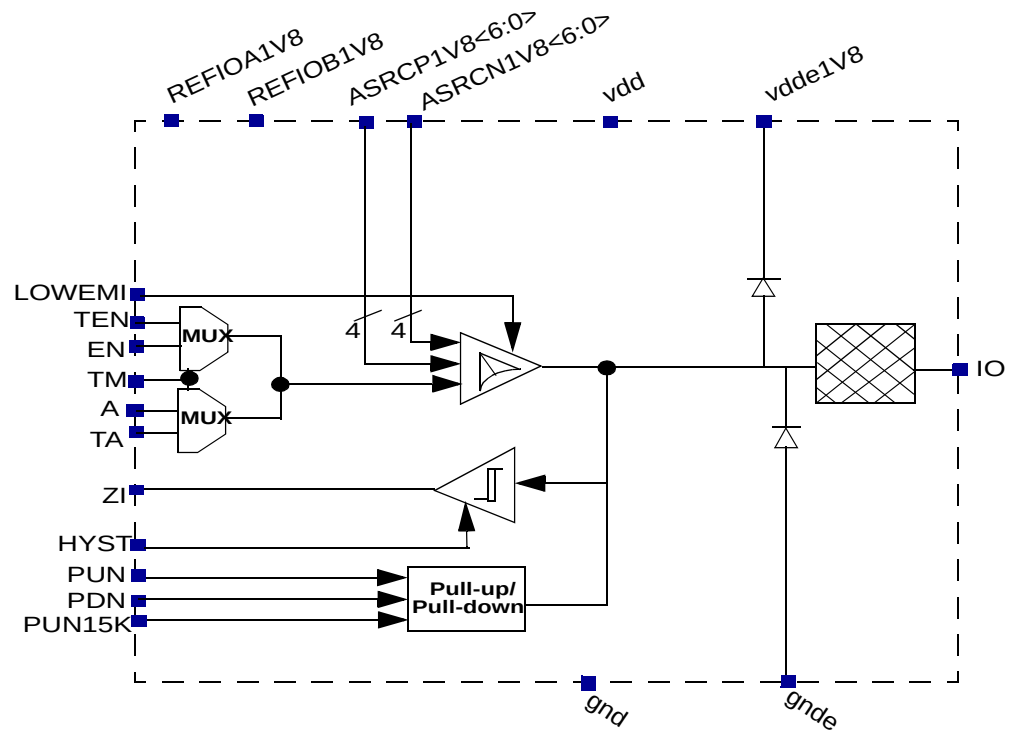
Packaging

- Flip-chip
- Cluster

Table 1. Operating conditions

Symbol	Para-meter	Con-dition	Value			Unit
			Min	Typ	Max	
$T_{junction}$	Temperature range	-	-40	25	125	°C
vdde1v8	IO PAD supply voltage range	1v8 operating range	1.65	1.8	1.95	V
		1v5 operating range	1.35	1.5	1.65	
		1v2 operating range	1.08	1.2	1.32	
vdd	Core supply voltage	Normal operating range	0.6	1.0	1.15	
V_i	Input voltage range of IO pin with respect to gnde	Input signal voltage operating range from device reliability perspective	-	-	1.95	

Figure 1. Block Diagram



1 Features

- Contains only digital cells
- 1.8 V signaling in Compensated mode and 1.5 V signaling in Non-compensated mode
- 1.2 V signaling in Non-compensated mode for MDIO applications (refer *Section 4.6: Usage of bidirectional IO for MDIO 1.2V application*)
- Compensated library with active slew rate control and with active impedance control
- Input with in-built programmable hysteresis
- Programmable slew and programmable drive
- Programmable pull-up, pull-down, and bus keeper features
- Scannable tristate output okk
- Antenna diode protection on core side input
- Test mode functionality
- Support for single row and double row configuration for an IO ring[a]
- No power sequence required for core and IO supplies[b]

a. Single row configuration is also called linear configuration and double row configuration is also called 2ROWS configuration.

b. Refer to *Section 3.2: Core-off and IO-off Functionality* for details.

2 Quick References

The document uses the following convention to indicate logic levels:

- *L indicates logic low.*
- *H indicates logic high.*
- *X indicates do not care state.*
- *Z indicates high impedance state.*
- *'-' (Hyphen) indicates 'No activity'.*

'' suffixed in library/cell name indicates multiple metallization options.*

2.1 Metal Stacking Convention

The metallization options supported by this library can be referred from its product package. The following is the convention that can be used to decode the segment in the library name:

- 7 metal option (5U1X2T8XLB) represents:
  - 5U1X refers to the first 5 levels with 1X pitch (thin) metal.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.
- 8 metal option (6U1X2T8XLB) represents:
  - 6U1X refers to the first 6 levels with 1X pitch (thin) metal in ultra low K.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.
- 10 metal option (6U1X2U2X2T8XLB) represents:
  - 6U1X refers to the first 6 levels with 1X pitch (thin) metal in ultra low K.
  - 2U2X refers to the next 2 levels with 2X pitch (thin) metal in ultra low K.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

2.2 Reference Documentation

This library is used with other cells of the 28 nm standard frame IO family. This family contains various cells: ESD protection, power supply, and place and route, which are used to construct an IO ring. To know more about these cells, refer the User Manuals of the following libraries:

- C28SOI_IO_EXT_CSF_BASIC_EG*
- C28SOI_IO_ALLF_IOSUPPLYKIT_EG*
- C28SOI_IO_ALLF_FRAMEKIT_EG*
- C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG*

For details on the following topics:

- Power Sequencing Recommendation in IOs
- Specifications and Analysis of Overshoots and Undershoots
- SSN Application Notes
- ESD qualification
- Latch-up qualification
- Maturity information
  - ST users, refer to the IO Reference catalog. (http://ccds.st.com/cps/sections/library/io/io_reference_catalog/downloadFile/file/IO_Helpdesk_Solutions.pdf)
  - Non-ST users, contact Customer Support personnel.

3 Functional Specifications

The library cell offer comprises bidirectional cells. The bidirectional cells have four variants, depending on the driving capability. The mode of operation and other features are the same across all the four different drives. However, the output DC/AC specifications of these IOs are different for different drives.

Table 2. Cell List

Cell Name	Width (µm)	Height (µm)	Pad Status in Core-off	Layout Configuration
Bidirectional IO 2 mA				
BD2SCARUDQPCZ_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	Tristate	Single row
BD2SCARUDQPCZ_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	Tristate	
BD2SCARUDQPCH_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	High	
BD2SCARUDQPCH_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	High	
BD2SCARUDQPCL_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	Low	
BD2SCARUDQPCL_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	Low	
BD2SCARUDQPCH_EXT_CSF_1V8_FC_INNER	40.0	90.8	High	Double row
BD2SCARUDQPCH_EXT_CSF_1V8_FC_OUTER	45.0	184.6	High	
BD2SCARUDQPCL_EXT_CSF_1V8_FC_INNER	40.0	90.8	Low	
BD2SCARUDQPCL_EXT_CSF_1V8_FC_OUTER	45.0	184.6	Low	
BD2SCARUDQPCZ_EXT_CSF_1V8_FC_INNER	40.0	90.8	Tristate	
BD2SCARUDQPCZ_EXT_CSF_1V8_FC_OUTER	45.0	184.6	Tristate	
Bidirectional IO 4 mA				
BD4SCARUDQPCZ_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	Tristate	Single row
BD4SCARUDQPCZ_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	Tristate	
BD4SCARUDQPCH_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	High	
BD4SCARUDQPCH_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	High	
BD4SCARUDQPCL_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	Low	
BD4SCARUDQPCL_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	Low	
BD4SCARUDQPCZ_IL_EXT_CSF_1V8_FC_LIN[1][3]	40.0	90.8	Tristate	
BD4SCARUDQPCZ_IL_EXT_CSF_1V8_CL_LIN[2][3]	40.0	106.3	Tristate	

Table 2. Cell List *(...continued)*

Cell Name	Width (µm)	Height (µm)	Pad Status in Core-off	Layout Configuration
BD4SCARUDQPCH_EXT_CSF_1V8_FC_INNER	40.0	90.8	High	Double row
BD4SCARUDQPCH_EXT_CSF_1V8_FC_OUTER	45.0	184.6	High	
BD4SCARUDQPCL_EXT_CSF_1V8_FC_INNER	40.0	90.8	Low	
BD4SCARUDQPCL_EXT_CSF_1V8_FC_OUTER	45.0	184.6	Low	
BD4SCARUDQPCZ_IL_EXT_CSF_1V8_FC_INNER	40.0	90.8	Tristate	
BD4SCARUDQPCZ_IL_EXT_CSF_1V8_FC_OUTER	45.0	184.6	Tristate	
BD4SCARUDQPCZ_EXT_CSF_1V8_FC_INNER	40.0	90.8	Tristate	
BD4SCARUDQPCZ_EXT_CSF_1V8_FC_OUTER	45.0	184.6	Tristate	
Bidirectional IO 6 mA				
BD6SCARUDQPCZ_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	Tristate	Single row
BD6SCARUDQPCZ_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	Tristate	
BD6SCARUDQPCH_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	High	
BD6SCARUDQPCH_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	High	
BD6SCARUDQPCL_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	Low	
BD6SCARUDQPCL_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	Low	
BD6SCARUDQPCH_EXT_CSF_1V8_FC_INNER	40.0	90.8|	High	Double row
BD6SCARUDQPCH_EXT_CSF_1V8_FC_OUTER	45.0	184.6|	High	
BD6SCARUDQPCL_EXT_CSF_1V8_FC_INNER	40.0	90.8|	Low	
BD6SCARUDQPCL_EXT_CSF_1V8_FC_OUTER	45.0	184.6|	Low	
BD6SCARUDQPCZ_EXT_CSF_1V8_FC_INNER	40.0	90.8|	Tristate	
BD6SCARUDQPCZ_EXT_CSF_1V8_FC_OUTER	45.0	184.6|	Tristate	
Bidirectional IO 8 mA				
BD8SCARUDQPCZ_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	Tristate	Single row
BD8SCARUDQPCZ_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	Tristate	
BD8SCARUDQPCH_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	High	
BD8SCARUDQPCH_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	High	
BD8SCARUDQPCL_EXT_CSF_1V8_FC_LIN[1]	40.0	90.8	Low	
BD8SCARUDQPCL_EXT_CSF_1V8_CL_LIN[2]	40.0	106.3	Low	
BD8SCARUDQPCH_EXT_CSF_1V8_FC_INNER	40.0	90.8|	High	Double row
BD8SCARUDQPCH_EXT_CSF_1V8_FC_OUTER	45.0	184.6|	High	
BD8SCARUDQPCL_EXT_CSF_1V8_FC_INNER	40.0	90.8|	Low	
BD8SCARUDQPCL_EXT_CSF_1V8_FC_OUTER	45.0	184.6|	Low	
BD8SCARUDQPCZ_EXT_CSF_1V8_FC_INNER	40.0	90.8|	Tristate	
BD8SCARUDQPCZ_EXT_CSF_1V8_FC_OUTER	45.0	184.6|	Tristate	

[1] These cells are integrated in linear flip-chip package.

[2] These cells are integrated in linear cluster package.

[3] Functionality/electrical specifications of *IL* cells are same as those of non *IL* cells, except the IO-off condition, where ZI = L at vdde1v8 = 0 V in *IL* cells.

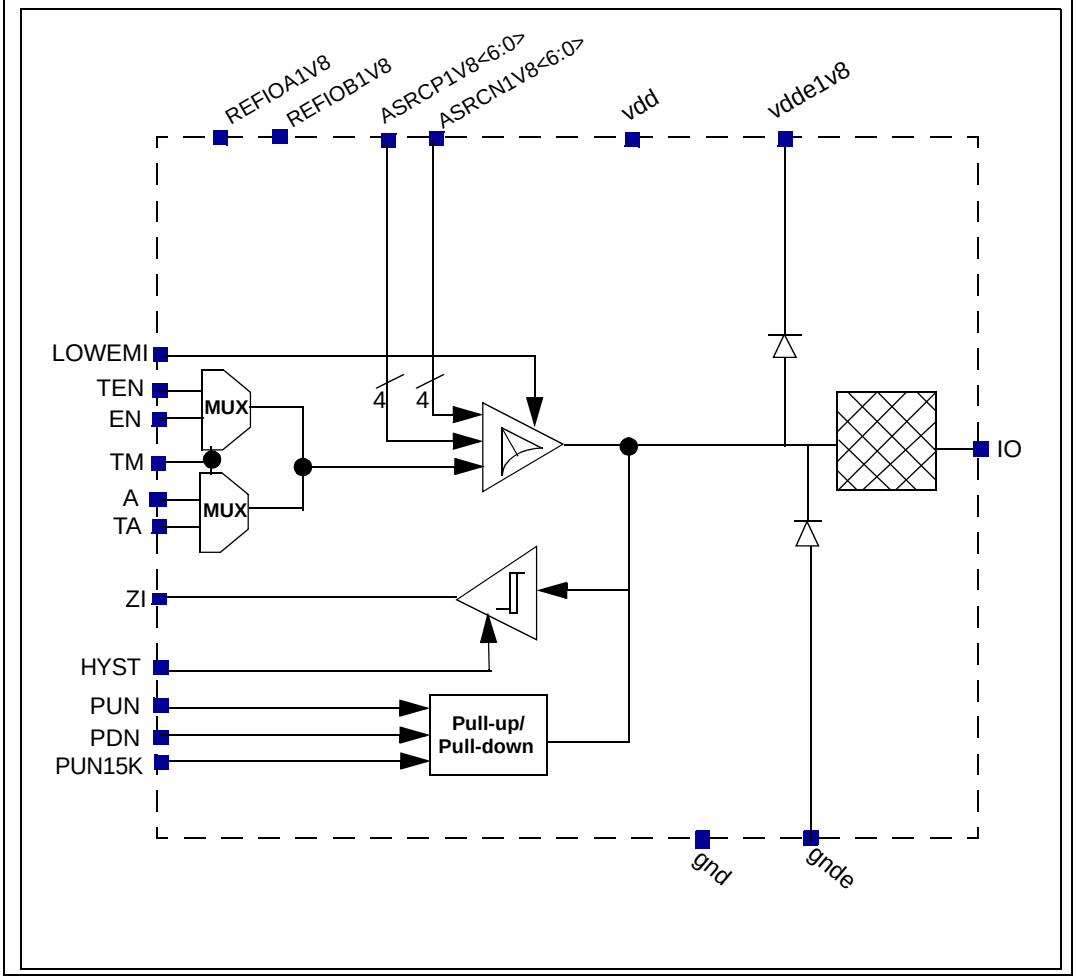
- *The Pad of cells carrying CZ in their name are in high impedance state in Core-off mode. Hence, in Core-off mode, the Pad of these cells must be driven externally.*
- *Drives (2 mA, 4 mA, 6 mA, and 8 mA) mentioned in cell names are guaranteed only for 1.8 V applications.*
- *For 1.5 V applications, drive is reduced. refer to Section 4.4: Static Characteristics (1.5 V applications) for more information.*

The ALLCELLS cells are not considered part of the deliverable. These cells are specifically for QA check and hence subject to change, without prior notice.

3.1 Bidirectional Cells

3.1.1 Functional Diagram

Figure 2. Programmable Bidirectional Buffer



3.1.2 Interface Description

Table 3. Pin Description

Pin	Type	Voltage Level	Description
Logic pins[1]			
A	Input	vdd	Driver input from core logic in Normal mode.
EN	Input	vdd	Enables output driver in Normal mode, active low.
TM	Input	vdd	For enabling Test mode, active high (TM = 'H' means Test mode, TM = 'L' means Normal mode).
TA	Input	vdd	Driver input from core login in Test mode.
TEN	Input	vdd	Enables output driver in Test mode, active low.
PUN	Input	vdd	Enables active pull-up, active low.
PDN	Input	vdd	Enables active pull-down, active low.
PUN15K	Input	vdd	Enables the additional pull-up of 15K (typical value, active low).
HYST	Input	vdd	Enables hysteresis, active high.
LOWEMI	Input	vdd	– Input from core logic to control output current slew rate. – When LOWEMI = 'H', the normal slew rate is slashed to half of its normal value. Thus, enabling Low EMI mode. – In normal case, LOWEMI = 'L'.
ZI	Output	vdd	Receiver output to core logic.
IO	Input/Output	vdde1v8	Bondpad.
Track pins			
ASRCN1V8<3:0>	Input/Output	vdde1v8	These pins are compensation bits used for slew rate/output drive control.
ASRCP1V8<3:0>			
vdde1v8	Input/Output	vdde1v8	External supply voltage.
vdd	Input/Output	vdd	Internal supply voltage.
gnde	Input/Output	Ground	External supply ground.
gnd	Input/Output	Ground	Internal supply ground.
Unused track pins			
ASRCN1V8<6:4>	Input/Output	0 or vdde1v8	Compensation bit track pins.
ASRCP1V8<6:4>			
REFIOA1V8			Reference signal track pins.
REFIOB1V8			

[1] Logic pins are digital. Hence, ensure that all the input pins are either tied to ground or to their respective supply levels depending upon the mode of operation of the IO cell. Floating input pins are not allowed.

3.1.3 Logic Behavior

Table 4. Input Cell Functional Table[1]

Input						Output	Mode
IO[2][3]	A	TA[3]	TM	EN	TEN	ZI[3]	
L	X	-	L	H	-	L	Simple input[4]
H	X	-	L	H	-	H	Simple input[4]
L	-	X	H	-	H	L	Simple input[5]
H	-	X	H	-	H	H	Simple input[4]

[1] For the combination EN/TEN = 'L', refer to *Table 5: Output Cell Functional Table*.

[2] IO is externally driven.

[3] Signal at A and ZI is at vdd level while IO is at vdde1v8 level.

[4] If weak pull-up is also switched on, then there is consumption from vdde1v8 to gnd through bidirectional cell driving it externally. However, the input works properly.

[5] If weak pull-down is also switched on, then there is consumption from vdde1v8 (IO supply of bidirectional cell) to gnd. However, the input works properly.

Table 5. Output Cell Functional Table

Input					Output	Mode
TM	EN	TEN	A	TA	IO	
L	L	X	L	X	L	Output[1]
L	L	X	H	X	H	
L	H	X	X	X	Z[2]	Input
H	X	L	X	L	L	Test mode output
H	X	L	X	H	H	
H	X	H	X	X	Z[2]	Test mode input

[1] IO is driven to the same logic level as that of 'A'.

[2] IO needs to be externally driven. In this case, pull-up and pull-down can be enabled or disabled depending upon PUN, and PDN. Refer to *Table 4: Input Cell Functional Table*[1].

The functionality for pin EN, which is used to enable output buffer for normal data path, in bidirectional buffers is not changed and is kept to active low, to keep it in line with the ST convention that is followed in all IO libraries.

3.1.3.1 Cell Behavior for Different Vdd Supply Operating Conditions

Table 6. Behavior in Different vdd Supply Operating Conditions

IOvdd[1]	Corevdd[2]	Description
0.6 V - 1.15 V	0.6 V - 1.15 V	IO works in Normal mode.
0	0	Cell works in Core-off mode. In this mode, IO keeps it's last state. Refer to *Section 3.2: Core-off and IO-off Functionality*.

[1] IOvdd refers to vdd supply used in IO ring.

[2] Corevdd refers to vdd supply used in core.

3.1.4 Functional Description

A bidirectional cell consists of a receiver and a driver. The receiver is programmed to incorporate hysteresis, which makes the receiver less sensitive to noisy input signals and/or noisy internal supply. The receiver is configured with three program bits, PUN, PUN15K, and PDN to switch on weak pull-up or pull-down transistors. During the IDDQ testing, the program bits can be used to disable both pull-up and pull-down transistors and cut the static current paths.

Table 7. Switching the Pull-up and Pull-down Transistors using PUN, PUN15K, and PDN

PUN	PDN	PUN15K	Description
L	L	H	Bus keeper[1]
L	H	H	Pull-up enabled [2]
H	L	H	Pull-down enabled[3]
H	H	H	Used in IDDQ mode [4]
L	L	L	Not allowed
L	H	L	Not allowed
H	L	L	Not allowed
H	H	L	15K pull-up enabled

[1] When PUN and PDN are low, IO is retained at its previous value using weak pull-up/pull-down and ZI is also driven to this IO value. However, the voltage levels are different. While ZI swings in logic voltage range 0 - vdd, IO swings in logic voltage range 0 - vdde1v8.

[2] Pull-up is implemented by a weak pull-up resistor of 50 kΩ (typical value).

[3] Pull-down is implemented by a weak pull-down resistor of 50 kΩ (typical value).

[4] IO is externally driven.

PUN = PDN = 'H' is prohibited, if the IO pin is tristated.

- *Pull-up/pull-down values of 50 K or 15 K in typical condition is applicable only for 1.8 V applications.*
- *For 1.5 V, these values are more. Refer to Section 4.4: Static Characteristics (1.5 V applications) for more information.*

To reduce EMI, when the buffer is operated at lower speed, a ‘LOWEMI’ pin is provided in bidirectional cells.

- *When LOWEMI = ‘H’, di/dt reduces to half of its value compared to the condition when LOWEMI = ‘L’.*
- *When LOWEMI = ‘H’, the maximum frequency of operation of output section is half of the frequency supported when LOWEMI = ‘L’.*

The driver is designed to source or sink the rated current (drive) within V_{OL} and V_{OH} specifications including margin for vdd or gnd noise. The three modes of operation of a bidirectional cell are:

- **Normal Mode**

A bidirectional cell is in Normal mode of operation when TM = ‘L’. In this mode, the cell can function as a driver or a receiver based on the logic condition of the EN pin.

- **Test Mode**

The cell is in Test mode, when TM = ‘H’. In this mode, functions of the TA and TEN pins are same as the functions of the A and EN pins in the Normal mode. Cell can function as both driver and receiver based on logic condition of the TEN pin.

- **IDDQ Mode**

The cell is in the IDDQ mode when PUN = PDN = ‘H’, which disconnects the pull-up and pull-down transistors, cutting off the static current consumption paths in the cell. In IDDQ mode, there should be no static current dissipation in the cell.

3.2 Core-off and IO-off Functionality

There is no power sequencing required for core and IO supplies. This means that core supply and IO supply can be switched ‘On’ or ‘Off’ independent of each other.

	*IO-off and core-off features are guaranteed only when the available supply is in the operating range. During transition or during voltage-ramp up, fixed logic state at output pins may not be ensured. There can be some glitch at the Pad during the transition phase of supplies, that is, vdd/vdde1v8.*

■ Core-off Mode

The bidirectional cells have no power sequencing requirement. This means that vdd and vdde1v8 can be switched ‘On’ or ‘Off’ independent of each other.

When vdde1v8 power is up, in the absence of core supply, cell goes in Core-off mode. In this mode, IO can be either low, high, or tristated, depending upon the cell name.

	● *Last state at IO is retained through weak pull-up/pull-down of 50 kΩ (typical).* ● *In this mode, there is no current consumption through weak pull-up/pull-down.*

■ IO-off Mode

The cell is in IO-off state when the core power supply is up in absence of IO power supply. In this mode, ZI is high.

	*If the vdde1v8 supply is powered down, the external activity at the 1.8 V/1.5 V interface is not allowed.*

4 Electrical Specifications

4.1 ESD and latch-up characteristics

Table 8. Library ESD targets

Symbol	Parameter	Condition	Target	Unit
V_{ESD}	Electronic discharge voltage	Human Body Model (HBM)	2000	V
		Machine Model (MM)	100	
		Charge Device Model (CDM)	500	
$P_{latch-up}$	Over-voltage stress	Maximum operating junction temperature 125 °C	1.5 * vdde1v8	
	Latch-up current[1]	Across temperature range	100	mA

[1] Specifications mentioned in the above table are valid for negative injection current only in case of Fail-safe/Tolerant IOs.

Warning for IO applications: ESD CDM

The level of CDM current seen at a given pre-charge voltage varies significantly with the chip size and package type. For instance, larger dies/packages generates higher CDM current.

However, this package size dependence has been considered during IO qualification, so that the above CDM commitment remains valid for any die/package size (even for large die/package sizes of hundreds of mm^2).

4.2 Static Characteristics (1.8 V applications)

4.2.1 Programmable Normal IO

Table 9. Static Characteristics of Bidirectional Cells

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
Receiver characteristics						
V_{IH} [1] [2]	High level input voltage	-	0.65 * vdde1v8	-	-	V
V_{IL} [1] [2]	Low level input voltage	-	-	-	0.35 * vdde1v8	V
V_{HYST}	Input hysteresis voltage	-	150	-	-	mV
Driver characteristics						
For 2 mA bidirectional cells						
I_{OL}	Static output low current	V_{OL} = 0.2 V	2	-	-	mA
I_{OH}	Static output high current	V_{OH} = vdde1v8 - 0.2 V	2	-	-	mA
For 4 mA bidirectional cells						
I_{OL}	Static output low current	V_{OL} = 0.2 V	4	-	-	mA
I_{OH}	Static output high current	V_{OH} = vdde1v8 - 0.2 V	4	-	-	mA
For 6 mA bidirectional cells						
I_{OL}	Static output low current	V_{OL} = 0.2 V	6	-	-	mA
I_{OH}	Static output high current	V_{OH} = vdde1v8 - 0.2 V	6	-	-	mA
For 8 mA bidirectional cells						
I_{OL}	Static output low current	V_{OL} = 0.2 V	8	-	-	mA
I_{OH}	Static output high current	V_{OH} = vdde1v8 - 0.2 V	8	-	-	mA
Weak input pull-up and pull-down characteristics						
I_{PU}	Pull-up current	V_I = 0 V (for 50 kΩ pull-up)	-	36	-	µA
I_{PD}	Pull-down current	V_I = vdde1v8	-	36	-	µA
I_{PU15K}	Pull-up current	V_I = 0 V (for 15 kΩ pull-up)	-	120	-	µA
R_{PU}	Equivalent pull-up resistance	V_I = 0 V	20	50	120	kΩ
R_{PD}	Equivalent pull-down resistance	V_I = vdde1v8	20	50	120	kΩ
R_{PU15K}	Equivalent pull-up resistance	V_I = 0 V	6	15	36	kΩ

[1] In Input mode of operation, the input signal on IO pad must be rail to rail (ground to supply level).

[2] In interchip communication, the maximum difference between the supply/ground of two chips must not be more than 300 mV.

4.3 Dynamic Characteristics (1.8 V applications)

4.3.1 Bidirectional Cells

4.3.1.1 Input Characteristics

Table 10. Dynamic Input Characteristics

vdd (V)	Symbol	Parameter	Condition	Value			Unit
				Min	Typ	Max	
0.6 - 1.15	C_{dty}	Duty cycle	Load at ZI = 0.2 pF	45	-	55	%
	F_{op}	Input frequency of operation		-	-	200	MHz

4.3.1.2 Output Characteristics

Table 11. Dynamic Characteristics of Output

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
C_{dty} [1] [2]	Duty cycle	-	40	-	60	%
f_{op}	Operating frequency	2 mA drive, Load = 15 pF, LOWEMI = 'L'	-	-	50	MHz
		2 mA drive, Load = 15 pF, LOWEMI = 'H'	-	-	25	MHz
		4 mA drive, Load = 15 pF, LOWEMI = 'L'	-	-	80	MHz
		4 mA drive, Load = 15 pF, LOWEMI = 'H'	-	-	40	MHz
		6 mA drive, Load = 15 pF, LOWEMI = 'L'	-	-	100	MHz
		6 mA drive, Load = 15 pF, LOWEMI = 'H'	-	-	50	MHz
		8 mA drive, Load = 15 pF, LOWEMI = 'L'	-	-	120	MHz
		8 mA drive, Load = 15 pF, LOWEMI = 'H'	-	-	60	MHz

[1] Externally driven by input A with 50% duty cycle.

[2] When compensation cell is working in Accurate mode.

4.4 Static Characteristics (1.5 V applications)

4.4.1 Programmable Normal IO

Table 12. Static Characteristics of Bidirectional Cells

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
Receiver characteristics						
V_{IH} [1] [2]	High level input voltage	-	0.7 * vdde1v8	-	-	V
V_{IL} [1] [2]	Low level input voltage	-	-	-	0.3 * vdde1v8	V
V_{HYST}	Input hysteresis voltage	-	50	-	-	mV
Driver characteristics						
For 2 mA bidirectional cells						
I_{OL}	Static output low current	V_{OL} = 0.2 V	1	-	-	mA
I_{OH}	Static output high current	V_{OH} = vdde1v8 - 0.2 V	1	-	-	mA
For 4 mA bidirectional cells						
I_{OL}	Static output low current	V_{OL} = 0.2 V	2	-	-	mA
I_{OH}	Static output high current	V_{OH} = vdde1v8 - 0.2 V	2	-	-	mA
For 6 mA bidirectional cells						
I_{OL}	Static output low current	V_{OL} = 0.2 V	3	-	-	mA
I_{OH}	Static output high current	V_{OH} = vdde1v8 - 0.2 V	3	-	-	mA

Table 12. Static Characteristics of Bidirectional Cells *(...continued)*

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
For 8 mA bidirectional cells						
I_{OL}	Static output low current	V_{OL} = 0.2 V	4	-	-	mA
I_{OH}	Static output high current	V_{OH} = vdde1v8 - 0.2 V	4	-	-	mA
Weak input pull-up and pull-down characteristics						
I_{PU}	Pull-up current	V_I = 0 V (for 75 kΩ pull-up)	-	24	-	µA
I_{PD}	Pull-down current	V_I = vdde1v8	-	24	-	µA
I_{PU15K}	Pull-up current	V_I = 0 V (for 20 kΩ pull-up)	-	90	-	µA
R_{PU}	Equivalent pull-up resistance	V_I = 0 V	25	-	160	kΩ
R_{PD}	Equivalent pull-down resistance	V_I = vdde1v8	25	-	160	kΩ
R_{PU15K}	Equivalent pull-up resistance	V_I = 0 V	8	-	50	kΩ

[1] In Input mode of operation, the input signal on IO pad must be rail to rail (ground to supply level).

[2] In interchip communication, the maximum difference between the supply/ground of two chips must not be more than 300 mV.

4.5 Dynamic Characteristics (1.5 V applications)

4.5.1 Bidirectional Cells

4.5.1.1 Input Characteristics

Table 13. Dynamic Input Characteristics

vdd (V)	Symbol	Parameter	Condition	Value			Unit
				Min	Typ	Max	
0.6 - 1.15	C_{dty}	Duty cycle	Load at ZI = 0.2 pF	45	-	55	%
	F_{op}	Input frequency of operation		-	-	100	MHz

4.5.1.2 Output Characteristics

Table 14. Dynamic Characteristics of Output

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
C_{dty} [1]	Duty cycle	-	40	-	60	%
f_{op}	Operating frequency	1 mA drive, Load = 15 pF, LOWEMI = 'L'	-	-	20	MHz
		1 mA drive, Load = 15 pF, LOWEMI = 'H'	-	-	10	MHz
		2 mA drive, Load = 15 pF, LOWEMI = 'L'	-	-	40	MHz
		2 mA drive, Load = 15 pF, LOWEMI = 'H'	-	-	20	MHz
		3 mA drive, Load = 15 pF, LOWEMI = 'L'	-	-	50	MHz
		3 mA drive, Load = 15 pF, LOWEMI = 'H'	-	-	25	MHz
		4 mA drive, Load = 15 pF, LOWEMI = 'L'	-	-	60	MHz
		4 mA drive, Load = 15 pF, LOWEMI = 'H'	-	-	30	MHz

[1] Externally driven by input A with 50% duty cycle.

4.6 Usage of bidirectional IO for MDIO 1.2V application

4.6.1 BD8SCARUDQPCZ_EXT_CSF_1V8* IO usage for 1.2 V application

The programmable IO are non-compensated bidirectional buffers in 1.2 V application. Connect ASRCP1V8<6:0>/ASRCN1V8<6:0> rails of the IO ring to fixed logic through FILLCELL_REFASRC_EXT_CSF_* cell. Please refer to *Figure 14: Constructing 1.5/ 1.2 V Normal IO Ring*.

4.6.2 Specification for MDIO 1.2 V application

Table 15. Static characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
Receiver characteristics						
V_{IH}	High level input voltage	-	0.84	-	vdde1v8 + 0.3	V
V_{IL}	Low level input voltage	-	-0.3	-	0.36	V
V_{HYST}	Input hysteresis voltage	-	100	-	-	mV
Driver characteristics						
I_{OL}	Static output low current	V_{OL} = 0.2 V	4	-	-	mA
I_{OH}	Static output high current	V_{OH} = vdde1v8 - 0.2	4	-	-	mA

Table 16. Dynamic input characteristics

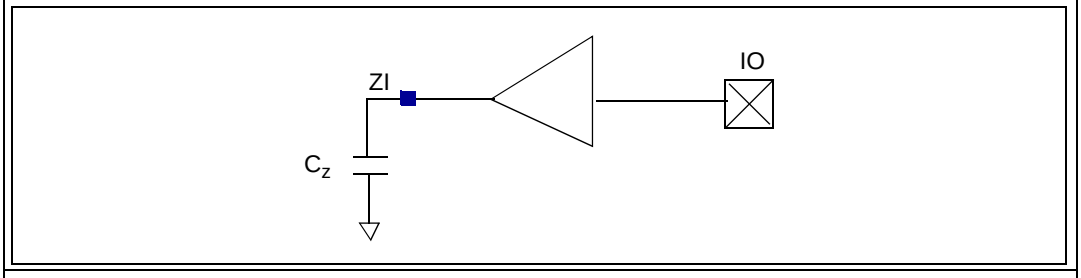
Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
C_{dty}	Duty cycle	-	45	-	55	%
f_{op}	Operating frequency	-	-	-	2.5	MHz

Table 17. Dynamic output characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
C_{dty}	High level input voltage	-	40	-	60	%
f_{op}	Low level input voltage	4 mA drive, Load = 470 pF, LOWEMI = 'L'	-	-	2.5	MHz
T_{low}	Low period	Measured between V_{IL} max and next rising	160	-	-	ns
T_{high}	High period	Measured between V_{IH} max and next rising	160	-	-	ns

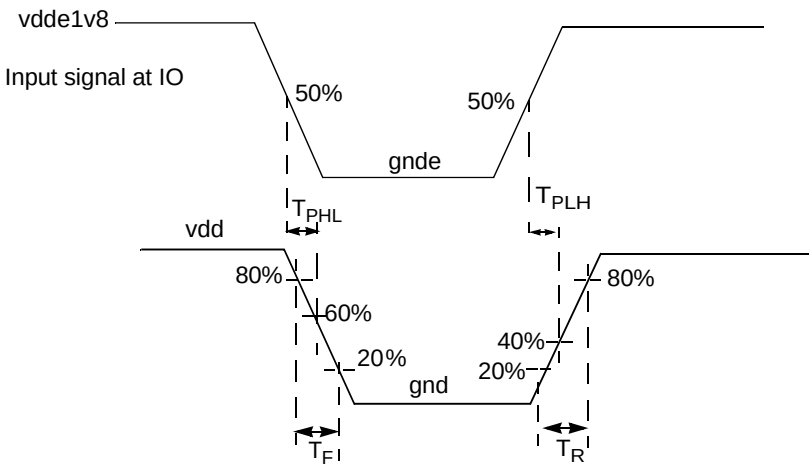
4.7 Measurement Setup

Figure 3. Input Test Setup



1. C_z = 0.2 pF

Figure 4. Input Timing Measurement Condition



1. T_R (from 20% to 80% of vdde1v8) and T_F (80% to 20% of vdde1v8) of input signal at IO is 1 ns.
2. Duty cycle of input signal at IO is 50%.

Figure 5. Output Test Setup

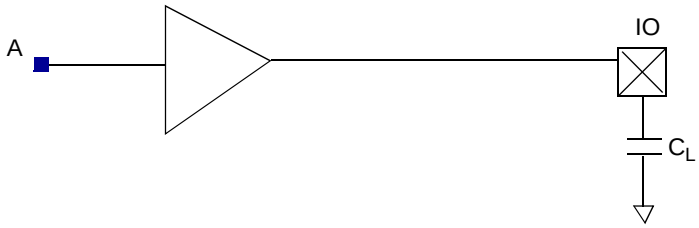
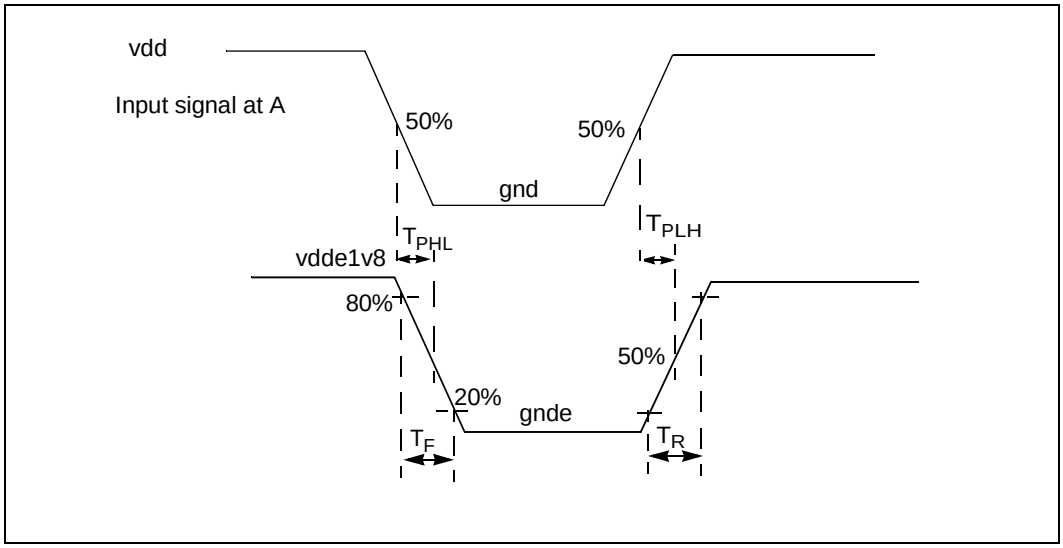
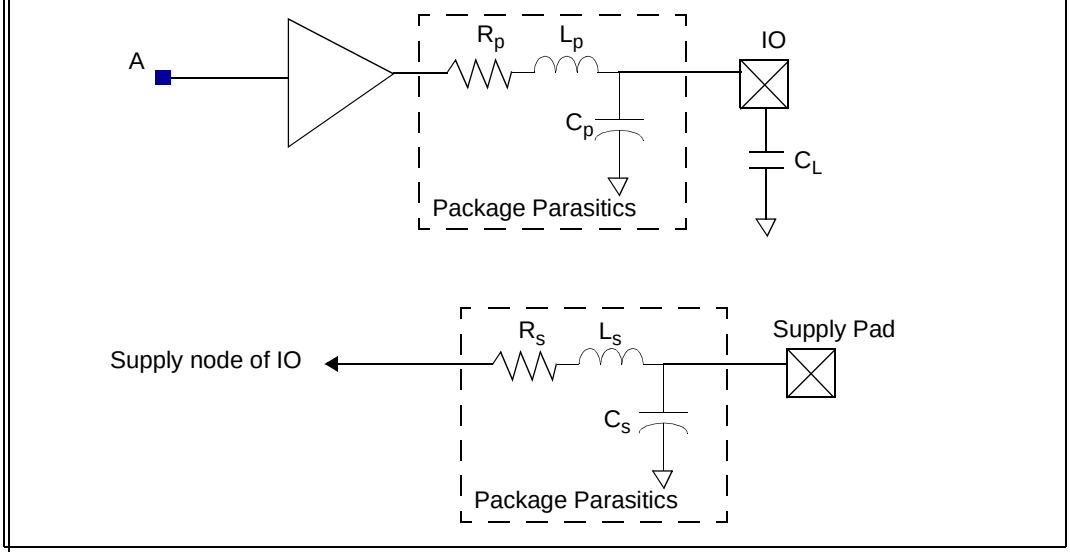


Figure 6. Output Timing Measurement Condition



1. T_R (from 0 to vdd) and T_F (vdd to 0) of input signal at A is 0.1 ns.
2. Duty cycle of input signal at A is 50%.

Figure 7. IO Supply Package Parasitics for SSN



1. $R_p = R_s = 200\ m\Omega$.
2. $L_p = 4.5$ nH.
3. $C_p = C_s = 2$ pF.
4. $L_s = 2$ nH.

- *The skew of any sort is not considered.*
- *Noise of any sort is not considered.*
- *All the applied input signals are jitter free.*
- *Jitter/Eye opening due to noise is not analyzed.*
- *No analysis for loopback timing is done.*
- *Board parasitics are not considered for simulations. All the simulations are done on the setups given in Figure 3: Input Test Setup and Figure 5: Output Test Setup.*

In all transient analysis, the output waveform is guaranteed to cross V_{OH} and V_{OL} levels.

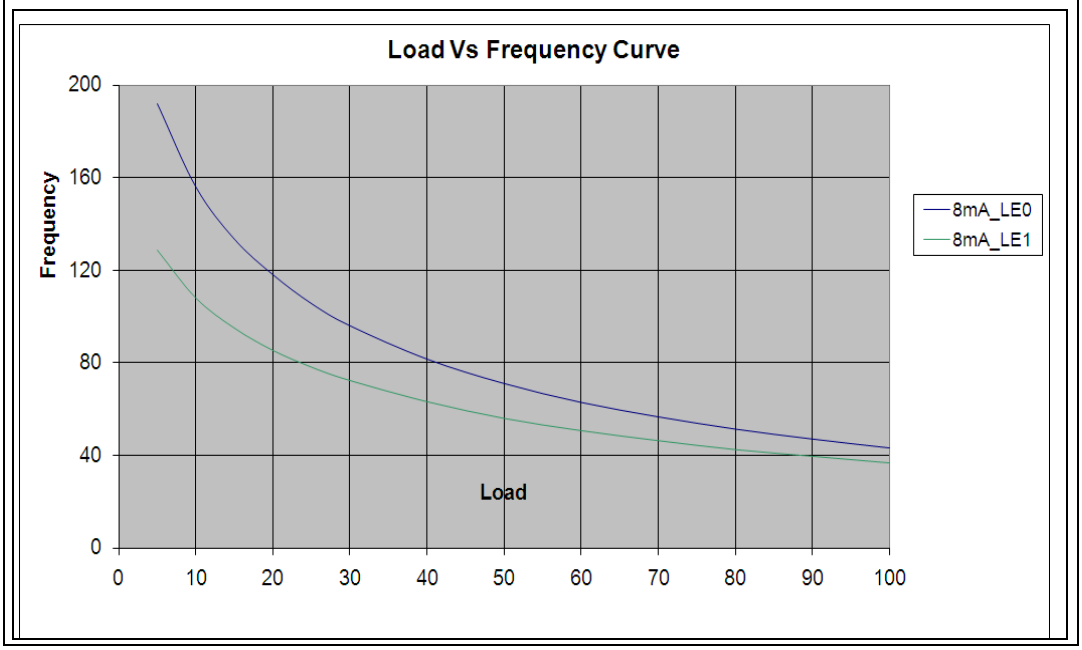
In characterization of library, to align IOs with other IPs:

- *vdde1v8 range is 1.65 V to 1.95 V.*
- *Coreside delay thresholds are 40% - 60%.*
- *Slope thresholds are 20% - 80%.*

4.8 Maximum Output Frequency versus Load

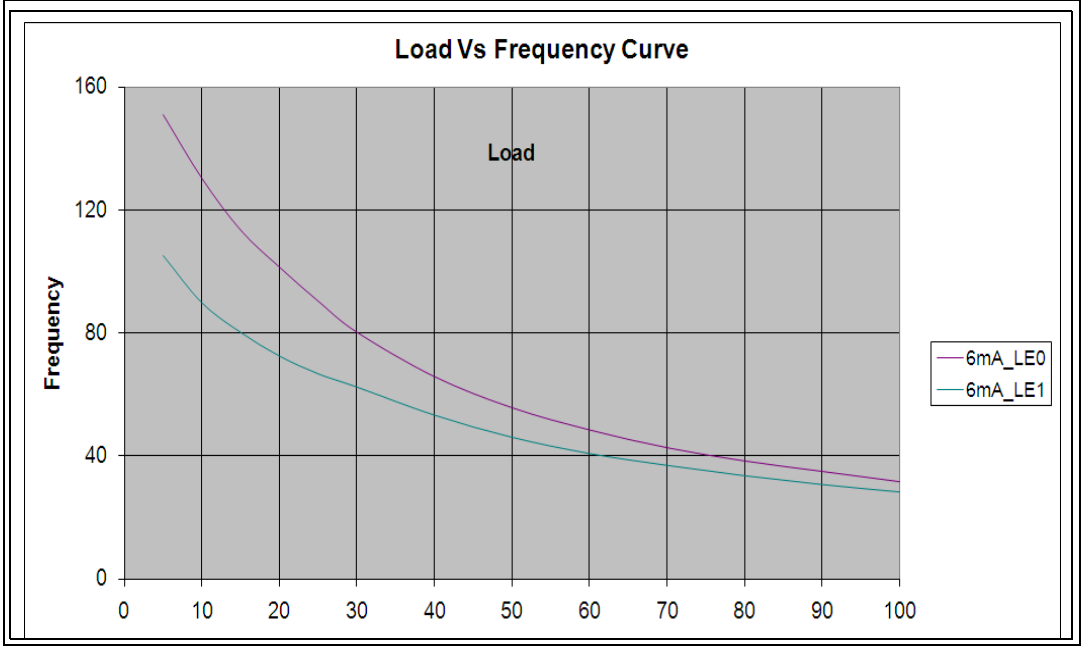
4.8.1 For 8 mA Bidirectional Cells (for 1.8 V application)

Figure 8. Output Frequency versus Load Characteristics for 8 mA Bidirectional Cells



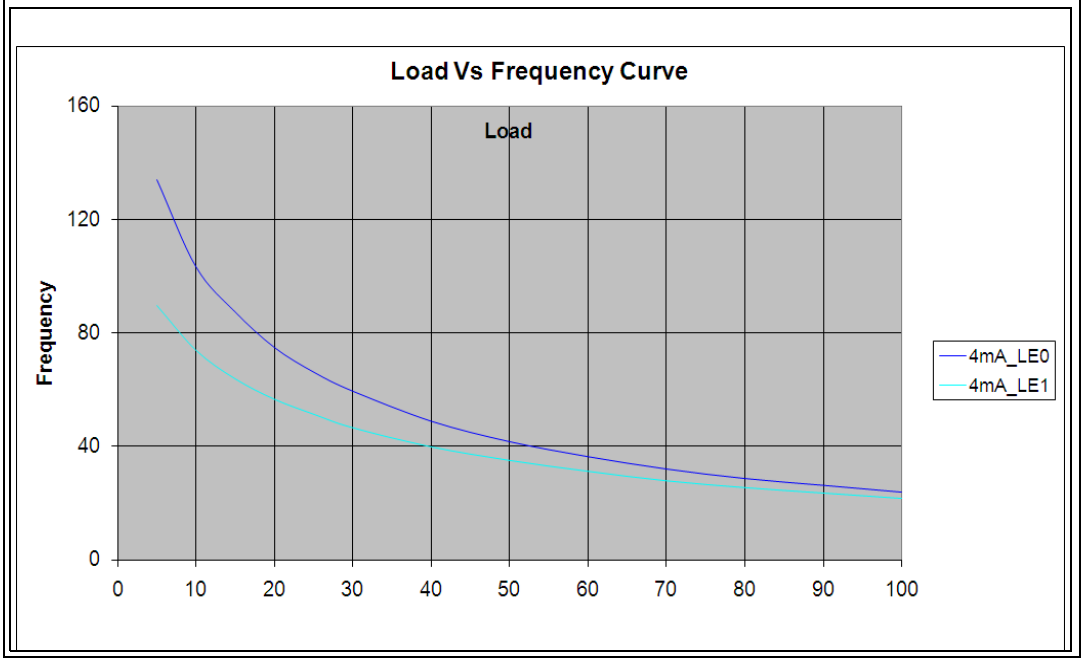
4.8.2 For 6 mA Bidirectional Cells (for 1.8 V application)

Figure 9. Output Frequency versus Load Characteristics for 6 mA Bidirectional Cells



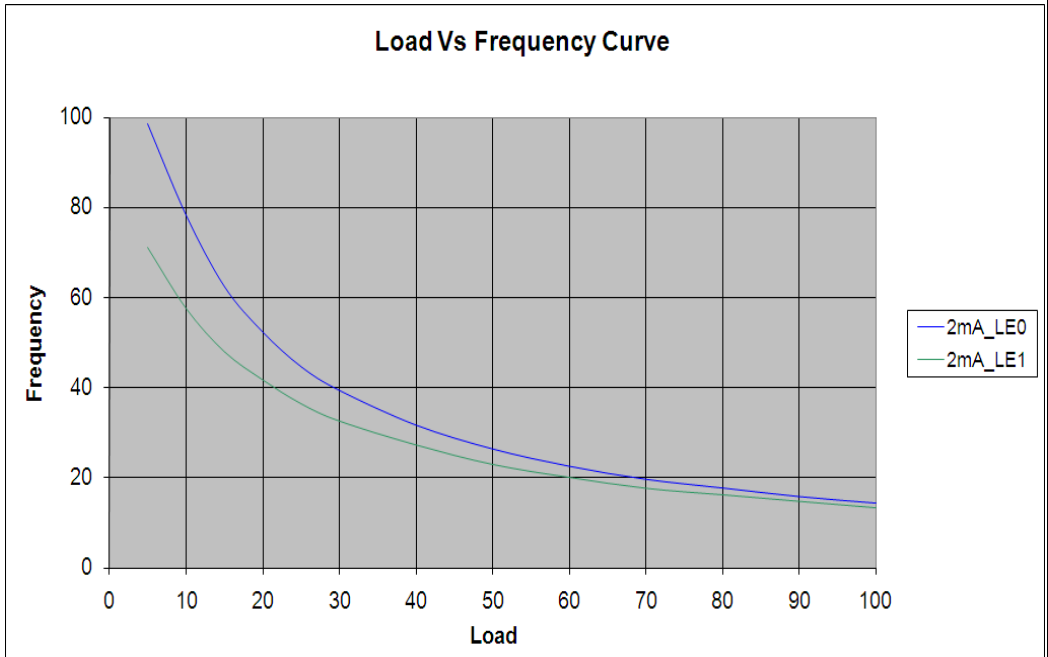
4.8.3 For 4 mA Bidirectional Cells (for 1.8 V application)

Figure 10. Output Frequency versus Load Characteristics for 4 mA Bidirectional Cells



4.8.4 For 2 mA Bidirectional Cells (for 1.8 V application)

Figure 11. Output Frequency versus Load Characteristics for 2 mA Bidirectional Cells



5 Usage Guidelines

5.1 IO Ring Development Guidelines

The C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG library supports the construction of an IO ring in single row configuration. To construct a 1.8 V IO ring in single row configuration, certain other libraries are required to be used with this library.

Table 18. Mandatory Cells

Library Name	Cell Type	Cell Name	Description
C28SOI_IO_EXT_CSF_BASIC_EG*	VDDE_EXT_CSF_FC_LIN	Supply cell	Contains ESD protection cells, supply cells, corners, and place and route cells.
	VDD_EXT_CSF_FC_LIN	Supply cell	
	GNDE_EXT_CSF_FC_LIN	Ground cell	
	GND_EXT_CSF_FC_LIN	Ground cell	
	VDDE_EXT_CSF_FC_INNER	Supply cell	
	GNDE_EXT_CSF_FC_INNER	Ground cell	
	VDDE_EXT_CSF_FC_OUTER	Supply cell	
	GNDE_EXT_CSF_FC_OUTER	Ground cell	
	GND_VDD_EXT_CSF_FC_2ROWS	Supply and Ground cell	
	WIRECELL_EXT_CSF_FC_LIN	Analog cell	
C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG*	COMPENSATION_EXT_1V8	Macro cell	– Contains one compensation cell. – For 1.8 V application, refer to the User Manual of the C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG* library to know more about the usage of the compensation cells and other requirements.
	COMPENSATION_EXT_CSF_1V8_FC _LIN	IO cell	

Table 18. Mandatory Cells *(...continued)*

Library Name	Cell Type	Cell Name	Description
C28SOI_IO_ALLF_IO SUPPLYKIT_EG*	-	-	Contains ESD protection cells, supply cells, corners, and place and route cells
C28SOI_IO_ALLF_F RAMEKIT_EG*	-	-	Contains leaf cells used by all other libraries, especially rail templates and bondpads.
For 1.5/ 1.2 V application C28SOI_IO_EXT_ CSF_ COMPENSATION1V 8 _LR_EG*	-	-	– Does not require any compensation cell. – ASRC rails in IO ring section are to be hardcoded at fixed logic. – Force ASRCN1V8<3:0> rails to logic high through 1.5 V supply and ASRCP1V8<3:0> rails to logic low through ground. – For more details, refer *Section 5.3.2: Usage of Bidirectional IOs (for 1.5/ 1.2 V application)*

5.2 Number of IOs per Supply

The number of IOs that can be driven by single supply pair (vdde and gnde), depends on the drive capability of the IOs. The number of IOs per supply for different drive capabilities is shown in the following table.

Table 19. Number of IOs per Supply for 1.8 V Application

Drive Capability	Condition	Number of IOs[1]
2 mA (BD2)	LOWEMI = ‘L’	16
4 mA (BD4)		10
6 mA (BD6)		8
8 mA (BD8)		6
2 mA (BD2)	LOWEMI = ‘H’	24
4 mA (BD4)		20
6 mA (BD6)		16
8 mA (BD8)		12

[1] The number of IOs per supply Pad is based on maximum number of IOs, which can switch simultaneously meeting dynamic specifications. These values are calculated assuming Package Parasitics as (R_S = 200 mΩ , L_S = 2 nH, and C_S = 2 pF) at supply Pad, as shown in *Figure 7: IO Supply Package Parasitics for SSN*.

Table 20. Number of IOs per Supply for 1.5 V Application

Drive Capability	Condition	Number of IOs[1]
1 mA (BD2)	LOWEMI = 'L'	6
2 mA (BD4)		5
3 mA (BD6)		4
4 mA (BD8)		3
1 mA (BD2)	LOWEMI = 'H'	8
2 mA (BD4)		6
3 mA (BD6)		5
4 mA (BD8)		4

[1] The number of IOs per supply Pad is based on maximum number of IOs, which can switch simultaneously meeting dynamic specifications. These values are calculated assuming Package Parasitics as (R_S = 200 mΩ , L_S = 2 nH, and C_S = 2 pF) at supply Pad, as shown in *Figure 7: IO Supply Package Parasitics for SSN*.

5.3 Place and Route Requirements

5.3.1 Usage of Bidirectional IOs (for 1.8 V application) with Compensation Cell

The programmable IOs are compensated bidirectional buffers and IO ring with these compensated IOs must be constructed in conjunction with the compensation cell. If the IO ring compensation cell is used, the ASRCN1V8<6:0> and ASRCP1V8<6:0> bits are directly tapped on the ASRCN1V8<6:0> and ASRCP1V8<6:0> rail, as shown in *Figure 12: Constructing 1.8 V Normal IO Ring using IO Ring Compensation Cell*.

Figure 12. Constructing 1.8 V Normal IO Ring using IO Ring Compensation Cell

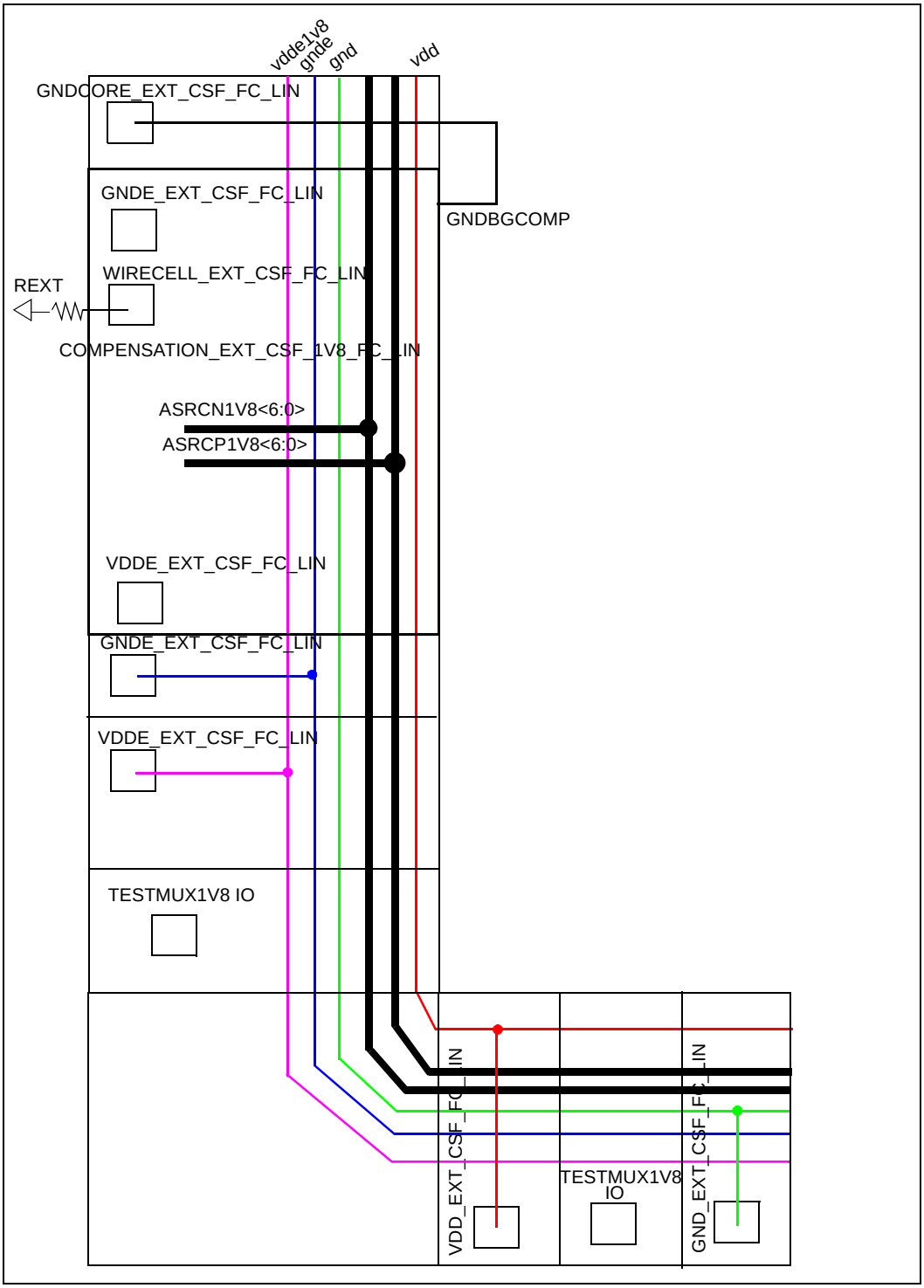
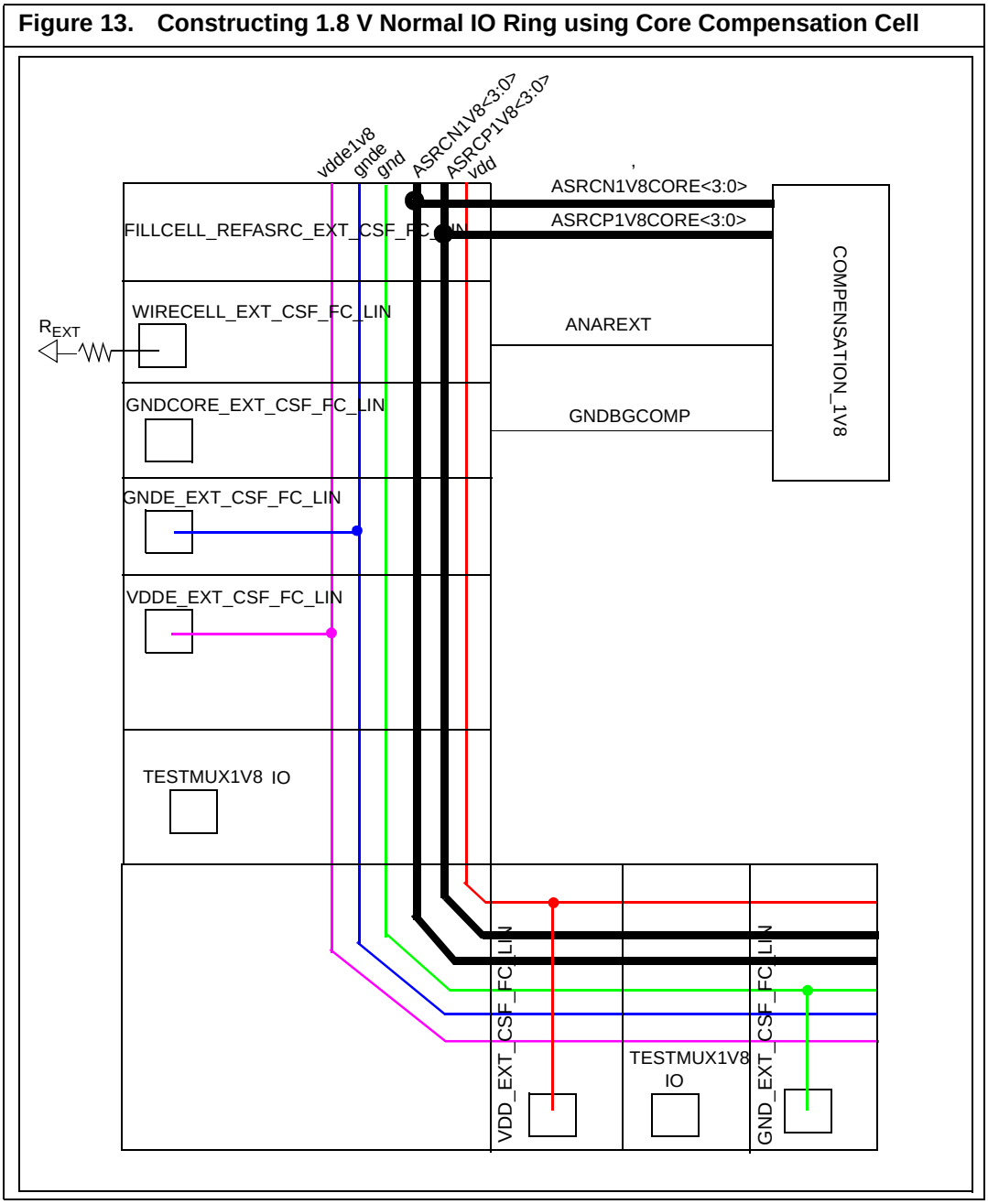


Figure 13. Constructing 1.8 V Normal IO Ring using Core Compensation Cell



5.3.2 Usage of Bidirectional IOs (for 1.5/ 1.2 V application)

The programmable IOs are non-compensated bidirectional buffers in 1.5/ 1.2 V application. Connect ASRCP1V8<3:0>/ASRCN1V8<3:0> rails of the IO ring to fixed logic through FILLCELL_REFASRC_EXT_CSF_* cell. Refer to *Figure 14: Constructing 1.5/ 1.2 V Normal IO Ring*.

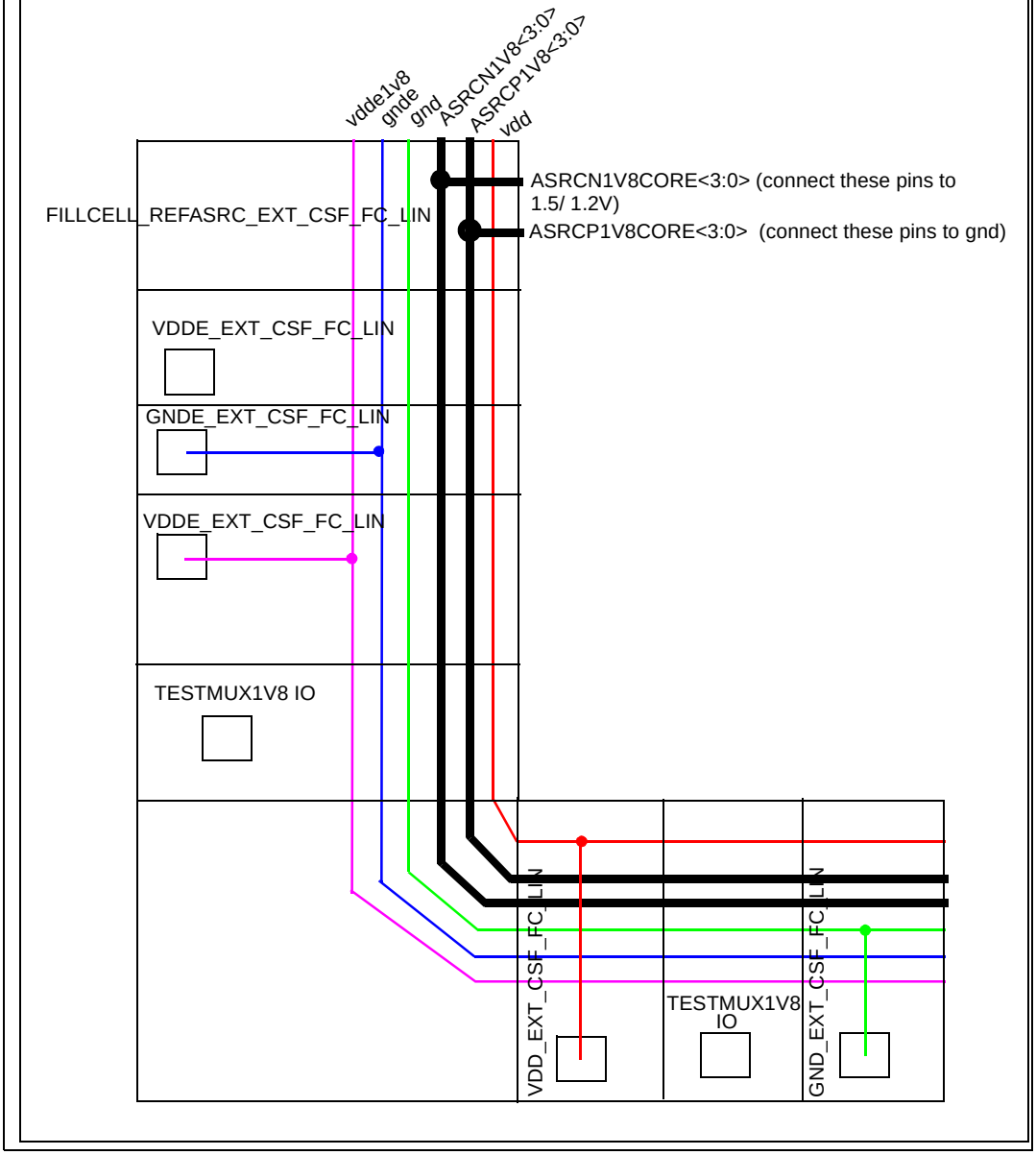
Table 21. Fixed Logic for ASRC rails in IO Ring

Library Name	Cell Name	Rail Pin	Core Pin[1]	Logic at Core Pin
C28SOI_IO_EXT_CSF_BASIC_EG*	FILLCELL_REFASRC_EXT_CSF_*	ASRCP1V8<0>	ASRCP1V8CORE<0>	gnd
		ASRCP1V8<1>	ASRCP1V8CORE<1>	
		ASRCP1V8<2>	ASRCP1V8CORE<2>	
		ASRCP1V8<3>	ASRCP1V8CORE<3>	
		ASRCN1V8<0>	ASRCN1V8CORE<0>	1.5/ 1.2 V supply voltage[2]
		ASRCN1V8<1>	ASRCN1V8CORE<1>	
		ASRCN1V8<2>	ASRCN1V8CORE<2>	
		ASRCN1V8<3>	ASRCN1V8CORE<3>	

[1] These pins are mapped according to the corresponding rail pins.

[2] 1.5/ 1.2 V supply voltage can be accessed through the core side vdde pin available in FILLCELL_VDDE_GNDE_EXT_CSF_* cell in the C28SOI_IO_EXT_CSF_BASIC_EG* library.

Figure 14. Constructing 1.5/ 1.2 V Normal IO Ring



6 Contact Information

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Appendix A Cell Naming Convention

Table 22. Naming Convention for Bidirectional Cells

Segment Name	Description
BD	Refers to the type of the cell. BD represents a bidirectional cell.
1st suffix	Indicates drive capability in mA. It can have either of the following values: – 2: represents 2 mA drive capability. – 4: represents 4 mA drive capability. – 6. represents 6 mA drive capability. – 8: represents 8 mA drive capability.
2nd suffix	Represents input type for a bidirectional cell. It can have the following value: – SC: refers to programmable Schmitt and non-Schmitt CMOS.
3rd suffix	Represents slew rate control. It can have the following value: – AR: indicates active slew rate control.
4th suffix	Represents active pull-up for a bidirectional cell. The value of this segment is U.
5th suffix	Represents active pull-down for a bidirectional cell. The value of this segment is D.
6th suffix	Refers to switch on pull-up or pull-down. The value of this segment is Q.
7th suffix	Refers to test pin block. The value of this segment is P.
8th suffix	Represents the status of Pad in Core-off mode. It can have either of the following values: – CZ: pad is tristated in Core-off mode. – CH: last value is retained at Pad. – CL: last value is retained at Pad.
9th suffix	Refers to the state of ZI pin in IO-off mode. The value of this segment is IL; ZI is low in IO-off mode.[1]
10th suffix	Refers to the size of the cell frame. It can have the following value: – EXT_CSF: represents a compatible standard frame.
11th suffix	Refers to the voltage level at Pad side. It can have the following value: – 1V8: represents 1.8 V Pad supply voltage.
12th suffix	Refers the type of cells (FC cells) based on packaging schemes. It can have either of the following values: – FC: indicates flip-chip cells package. – CL: indicates cluster cells package.
13th suffix	Refers to the configuration type of the IO ring. It can have either of the following values: – LIN: indicates single row configuration. – INNER indicates inner row in double row configuration. – OUTER indicates outer row in double row configuration.

[1] If this segment is not present in the name, it means that ZI is high in IO-off mode.

Table 23. Example: Segments in the Name of BD6SCARUDQPCZ_EXT_CSF_1V8_FC_LIN Cell

Segment Name	Segment Value	Description
BD	BD	Bidirectional cell
1st suffix	6	6 mA drive capability
2nd suffix	SC	Schmitt and non-Schmitt CMOS
3rd suffix	AR	Active slew rate control
4th suffix	U	Active pull-up
5th suffix	D	Active pull-down
6th suffix	Q	Switch on pull-up/pull-down
7th suffix	P	Test pin block present
8th suffix	CZ	Pad is tristated in Core-off mode
9th suffix	EXT_CSF	Compatible standard frame
10th suffix	1V8	1.8 V supply voltage
11th suffix	FC	Flip-chip type package
12th suffix	LIN	Single row configuration

Appendix B Document Revision History

Table 24. Document Revision History

Date	Document Version	Comments
09-Jun-2016	1.1	Updated: *Table 1: Operating conditions*, *Table 8: Library ESD targets*, *Table 10: Dynamic Input Characteristics* and *Table 13: Dynamic Input Characteristics*
11-Nov-2014	1.0	First release

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