C28SOI_SC_8_PR_LL
User Manual

8 track Standard Cells library comprising Place and Route cells

Overview

Features

- 8-track Standard Cells library
- The library consists of 69 cells
- Based on low power low V_T transistors

Applications

- These cells are used for Place and Route.

Library Architecture

In C28SOI_SC_8_PR_LL library, all pins are located on the vertical and horizontal pin grids. Although, only some place and route tools require all pins on grids, most of the tools work more efficiently with all pins on grids.

Figure 1. Layout for Single Height Cell

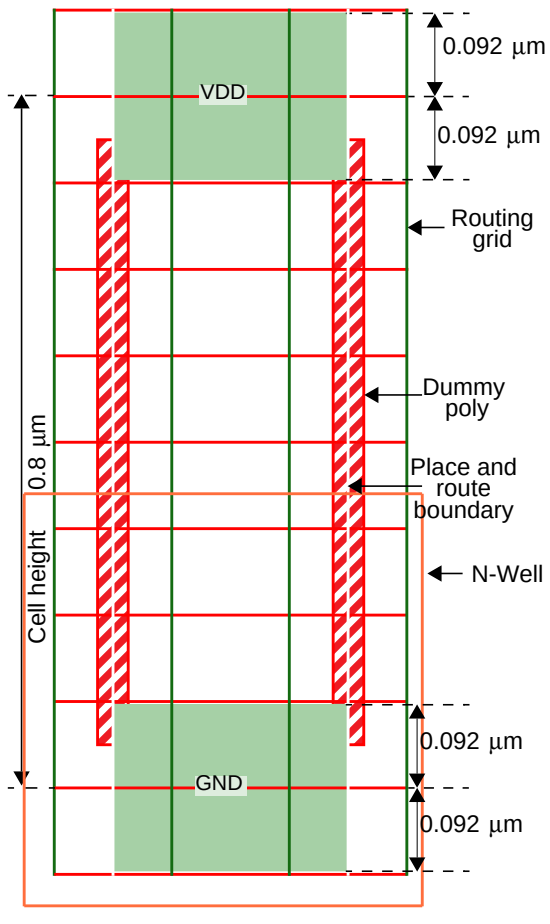
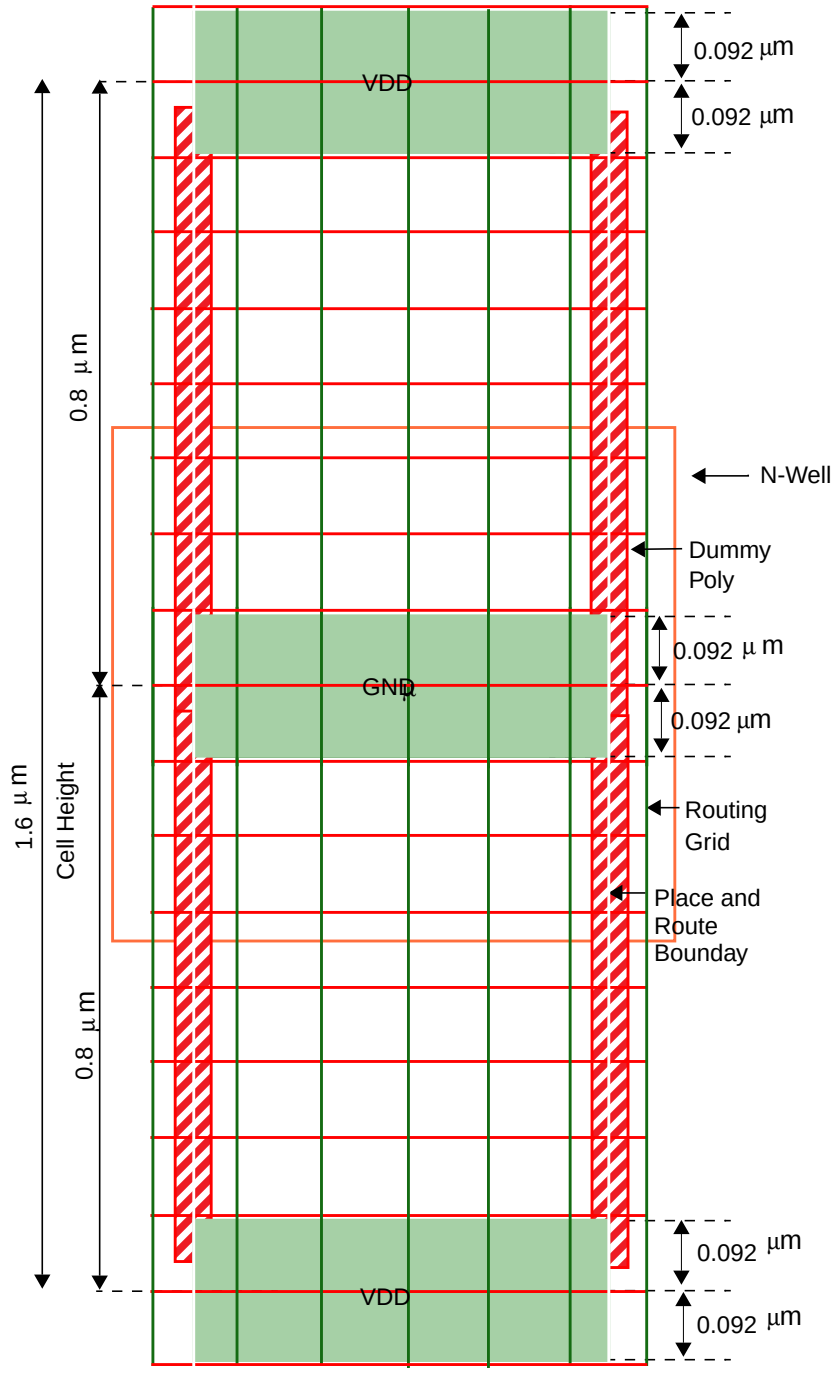


Table 1. Physical Specifications

Parameter	Measurement (µ m)
Drawn gate length	0.030
Layout grid	0.001
Vertical pin grid	0.100
Horizontal grid	0.136
Cell power and ground rail width	0.184
Single cell height	0.80
Double cell height	1.60

Figure 2. Layout for Double Height Cell with VDD Rail at Bottom



1 Quick References

This section provides reference information about the Standard Cell library.

	*This document is compatible for viewing with acroread 7.0 and higher versions. If opened with a lower version of acroread, there might be some color display problem.*

	*Please refer to the Naming Convention Document available in Design Package for more details regarding cell names.*

2 Functional Specifications

2.1 Cell List

The C28SOI_SC_8_PR_LL library consists of the following cells.

Table 2. Cell List

Cell Name	Number of Cells
ANTPROT	2
DECAP/PDECAP	11
FILLERPFOP	6
FILLERFLPCHKAE	6
FILLERCELL	7
FILLERSNPW/FILLERNPW	2
ANTPROTFILLERSNPW	3
ANTPROTGVFILLERNPW	2
ANTPROTGVFILLERSNPW	1
TOH/TOL	2
FILLERPCEND	27

3 Library Contents

This section describes the content of this library.

3.1 Library Description by Family

This section describes the library content by presenting all families of cells.

3.1.1 Antenna Diodes

This family of cells is completely compliant with CMOS028_FDSOI process.

The ANTPROT6 cell is a 6-grid cell with MINUS M1 pin. The library contains one ANTPROT6 cell:

- C8T28SOI_LL_ANTPROT6

The ANTPROT4 cell is 4-grid cell with MINUS M1 pin. The library contains one ANTPROT4 cell:

- C8T28SOI_LL_ANTPROT4

Caution: C8T28SOI_LL_ANTPROT4 is not standalone DRC clean, had to keep other cell on surroundings. To overcome this issue, there is another ANTPROT cell “C8T28SOI_LL_ANTPROT6” which is standalone DRC clean for fully isolated Designs

3.2 Supply Decoupling

Supply decoupling cells exist for users who want to discharge power nets.

Following are the decoupling cells with GO1 transistors.

- C8T28SOI_LLF_DECAPXT4
- C8T28SOI_LLF_DECAPXT8

Following are decoupling cells with large gate length (>30 nm) with GO1 transistors having only PMOS:

- C8T28SOI_LLL_PDECAP16
- C8T28SOI_LLL_PDECAP32
- C8T28SOI_LLL_PDECAP4
- C8T28SOI_LLL_PDECAP64
- C8T28SOI_LLL_PDECAP8

Following are decoupling cells with GO2 transistors.

- C8T28SOIDV_LLEGLV_DECAPXT11
- C8T28SOIDV_LLEGLV_DECAPXT16
- C8T28SOIDV_LLEGLV_DECAPXT32
- C8T28SOIDV_LLEGLV_DECAPXT64

3.3 TIE High/Low Cells

Following are Tie high and Tie low cells:

- C8T28SOI_LL_TOHX5
- C8T28SOI_LL_TOLX5

3.4 Filler Cells with Pattern Fill

3.4.1 Filler Cells with Pattern Fill for PC

This family of cells is completely compliant with CMOS028_FDSOI process. Poly rectangles (poly on boundary) are present to fill the poly density requirement. The following are the filler cells with pattern fill for PC:

- C8T28SOI_LL_FILLERCELL1
- C8T28SOI_LL_FILLERCELL2
- C8T28SOI_LL_FILLERCELL4
- C8T28SOI_LL_FILLERCELL8
- C8T28SOI_LL_FILLERCELL16
- C8T28SOI_LL_FILLERCELL32
- C8T28SOI_LL_FILLERCELL64

3.4.2 Filler Cells with Pattern Fill for PC and RX

This family of cells is completely compliant with CMOS028_FDSOI process. Poly rectangles are present to fill the PC density requirement. RX rectangles are present to satisfy the minimum RX density requirement. The following are the filler cells with pattern fill for PC and RX:

- C8T28SOI_LL_FILLERPFOP2
- C8T28SOI_LL_FILLERPFOP4
- C8T28SOI_LL_FILLERPFOP8
- C8T28SOI_LL_FILLERPFOP16
- C8T28SOI_LL_FILLERPFOP32
- C8T28SOI_LL_FILLERPFOP64

FILLERPFOP* cells are used at the top and bottom of the design.

Above cells have an endcap of 44nm and are standalone DRC clean and will not highlight the aggressive poly EndCap DRC violations at initial floorplan level.

For the above drawback we have added below cells :

- C8T28SOI_LL_FILLERPFLPCHKAE16
- C8T28SOI_LL_FILLERPFLPCHKAE2
- C8T28SOI_LL_FILLERPFLPCHKAE32
- C8T28SOI_LL_FILLERPFLPCHKAE4
- C8T28SOI_LL_FILLERPFLPCHKAE64
- C8T28SOI_LL_FILLERPFLPCHKAE8

These FILLERFLPCHKAE* cells when used during initial floor planning verification will represent real scenario of poly endcap(PCnes), helping designer to take corrective measure in the initial phase itself. These cells have an endcap of 37nm. Also These specific cells have intentional DRC error so that it can be checked that it does not remain in final GDS.

3.5 Filler Tie Cells with RX Well-straps with Pattern Fill for PC

The maximum distance from any point inside source/drain RX area to the nearest RX of a well tied within the same NW or PW is defined in DRM to ensure substrate polarization. RX well straps cells are necessary to satisfy this rule because there is no substrate strap in Standard Cells.

3.5.1 Non-split Filler Cells

This family of cells is completely compliant with CMOS028_FDSOI process. The FILLERNPW5 cells can be used to boost densities for RX and to improve the substrate polarization. The following filler cell with N-well and P-well straps, respectively is connected to abutting rails gnd and vdd:

- C8T28SOI_LL_FILLERNPW5

3.5.2 Split Filler Cells

This family of cells is completely compliant with CMOS028_FDSOI process. PC wires are present to fill the PO density requirement. The following filler cell with N-well and P-well straps, respectively is connected to internal pins, gnds and vdds, and with pattern fill for PC:

- C8T28SOI_LL_FILLERSNPW5

3.5.3 Non Split Cells with Antenna Diode

This family of cells is completely compliant with CMOS028_FDSOI process, PC wires are present to fill the PO density requirement. The following are the filler cells with Nwell and Pwell straps i.e. gnds and vdds internally tied to gnd, and with pattern fill for PC. An ANTENNA diode protection is connected between vdd and gnd to prevent from ANTENNA phenomena at process level.

- C8T28SOI_LL_ANTPROTGVFILLERNPW6
- C8T28SOI_LL_ANTPROTGVFILLERNPW8

3.5.4 Split Filler Cells with Antenna Diode

This family of cells is completely compliant with CMOS028_FDSOI process, PC wires are present to fill the PO density requirement. The following are the filler cells with N-well and P-well straps, respectively connected to internal pins, gnds and vdds, and with pattern fill for PC.

- C8T28SOI_LL_ANTPROTFILLERSNPW6
- C8T28SOI_LL_ANTPROTFILLERSNPW7
- C8T28SOI_LL_ANTPROTFILLERSNPW8
- C8T28SOI_LL_ANTPROTGVFILLERSNPW8

In cells C8T28SOI_LL_ANTPROTFILLERSNPW6/7/8, An ANTENNA diode protection is provided between gnd and gnds.

In cell C8T28SOI_LL_ANTPROTGVFILLERSNPW8, An ANTENNA diode protection is provided between gnd-gnds and vdd-vdds both in to prevent from ANTENNA phenomena at process level.

Caution: As ANTPROTFILLERSNPW* and ANTPROTGVFILLERSNPW*, both to be used for LVT FBB domains, so for deciding which one to use should be based on below remarks -

C8T28SOI_LL_ANTPROTGVFILLERSNPW* :

- Not to be used for extreme FBB domains as there is diode between vdd/vdds which may cause breakdown (Vb>2.6V)risk when used at Extreme FBB.

C8T28SOI_LL_ANTPROTFILLERSNPW* :

- To be used in case of very high difference of potential between vdd & vdds i.e., for LVT Extreme FBB domains and where antenna ratio are not violated at design level. As in

this cell, there is no diode between vdd-vdds, so no risk of huge potential difference in case of LVT Extreme FBB domains.

3.6 Filler Cell to Avoid the Aggressive end Capacitance Violation

They will be automatically inserted above last and first rows of all Standard Cells block to prevent DRC violation of aggressive PC end capacitance. Small poly rectangles are present to enlarge PC end capacitance at the top and/or at the bottom of first and last line.

- C8T28SOI_LVTFILLERPCENDB1
- C8T28SOI_LVTFILLERPCENDB16
- C8T28SOI_LVTFILLERPCENDB2
- C8T28SOI_LVTFILLERPCENDB32
- C8T28SOI_LVTFILLERPCENDB4
- C8T28SOI_LVTFILLERPCENDB64
- C8T28SOI_LVTFILLERPCENDB8
- C8T28SOI_LVTFILLERPCENDBL1
- C8T28SOI_LVTFILLERPCENDBR1
- C8T28SOI_LVTFILLERPCENDT1
- C8T28SOI_LVTFILLERPCENDT16
- C8T28SOI_LVTFILLERPCENDT2
- C8T28SOI_LVTFILLERPCENDT32
- C8T28SOI_LVTFILLERPCENDT4
- C8T28SOI_LVTFILLERPCENDT64
- C8T28SOI_LVTFILLERPCENDT8
- C8T28SOI_LVTFILLERPCENDTB1
- C8T28SOI_LVTFILLERPCENDTB16
- C8T28SOI_LVTFILLERPCENDTB2
- C8T28SOI_LVTFILLERPCENDTB32
- C8T28SOI_LVTFILLERPCENDTB4
- C8T28SOI_LVTFILLERPCENDTB64
- C8T28SOI_LVTFILLERPCENDTB8
- C8T28SOI_LVTFILLERPCENDTBL1
- C8T28SOI_LVTFILLERPCENDTBR1
- C8T28SOI_LVTFILLERPCENDTL1
- C8T28SOI_LVTFILLERPCENDTR1

3.7 Supported Flow Strategies

Different options are available for process, substrate connection, and V_T implant. For each parameter, the supported options are:

- Process options
  - Single CMOS028_FDSOI process
- Substrate connection options
  - No-split power with substrate straps connected to vdd and gnd
  - Split power with substrate straps connected to vdds and gnds
- V_T implants
  - Single V_T implant: only LVT

3.7.1 Single Process and Single V_T Implant

To illustrate the case of only one process (for example, CMOS028_FDSOI process) and only one V_T (for example, LVT implant), a possible strategy is discussed in further sections.

3.7.2 Gaps Filling

- C8T28SOI_LL_FILLERCELL1/2/4/8/16/32/64
- C8T28SOI_LL_FILLERPFOP2/4/8/16/32/64
- C8T28SOI_LL_FILLERPFOPAE2/4/8/16/32/64

3.7.3 Antenna Diodes

- C8T28SOI_LL_ANTPROT4/C8T28SOI_LL_ANTPROT6

3.7.4 Non-split Power Substrate Straps (OD well-straps connected to vdd/gnd)

- C8T28SOI_LL_FILLERNPW5

3.7.5 Split Power Substrate Straps (OD well-straps connected to vdds/gnds)

- C8T28SOI_LL_FILLERSNPW5

3.7.6 Split Power Substrate Straps (OD well-straps connected to vdds/gnds) with Antenna Protection Diode

- C8T28SOI_LL_ANTPROTFILLERSNPW6/7/8

3.7.7 Split Power Substrate Straps (OD Well-straps connected to vdds and gnds for Pwell and Nwell respectively) with Antenna Protecttion Diode

- C8T28SOI_LL_ANTPROTGVFILLERSNPW8

3.7.8 Non-Split Power Substrate Straps (OD Well-straps connected to gnd) with Antenna Protection Diode

- C8T28SOI_LL_ANTPROTGVFILLERNPW6/8

4 Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com