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C28SOI_SC_8_CORE_LL Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells

Overview

- C28SOI_SC_8_CORE_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

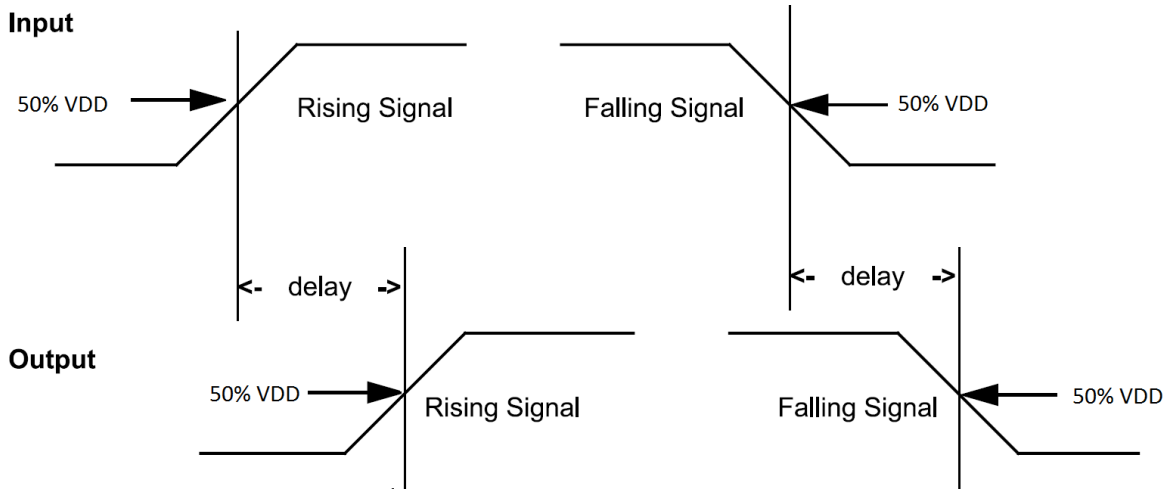


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

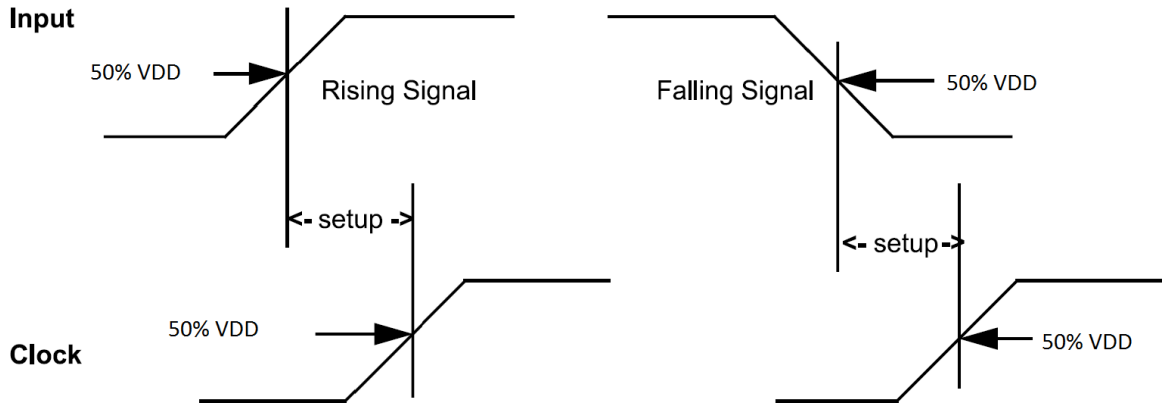


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

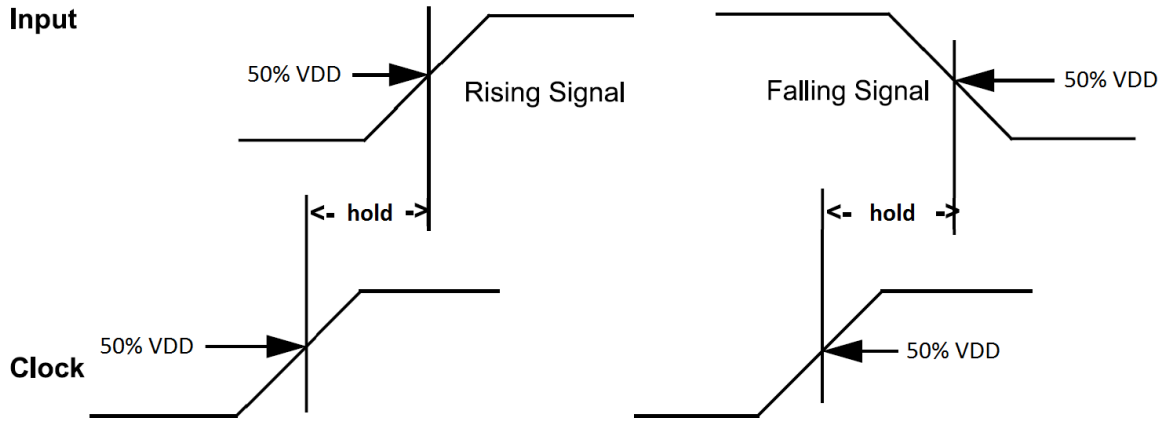


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

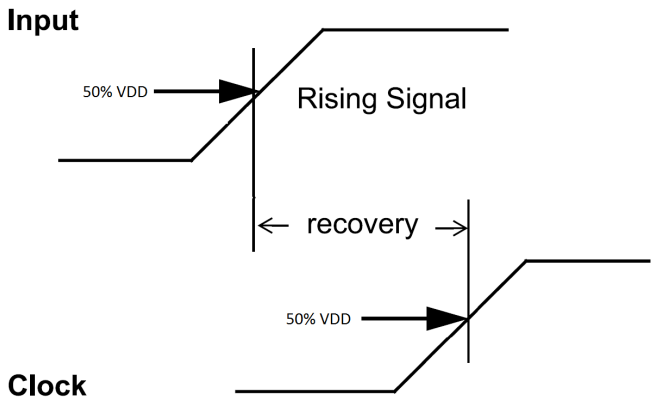


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

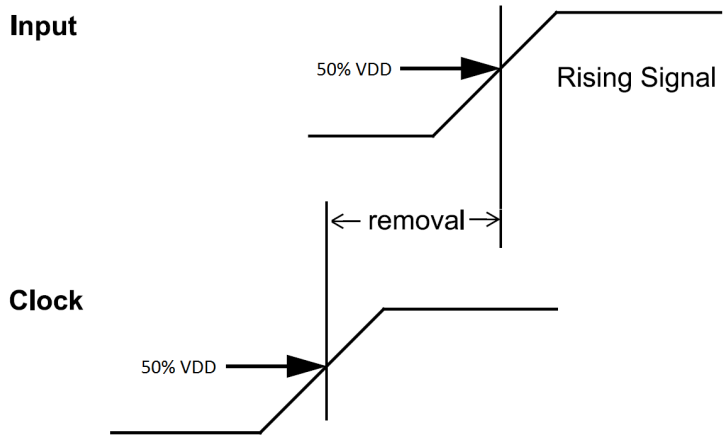


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

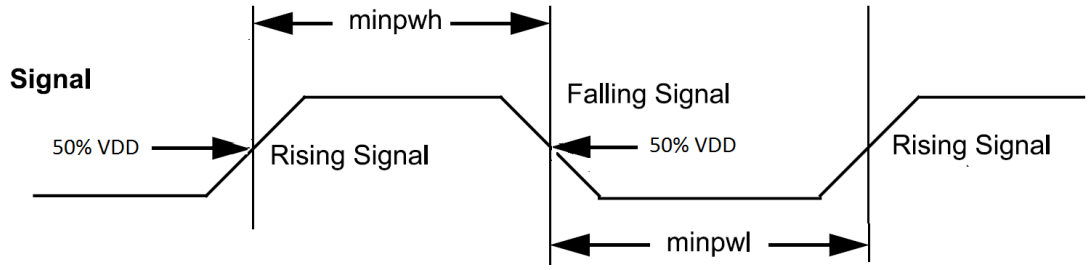


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

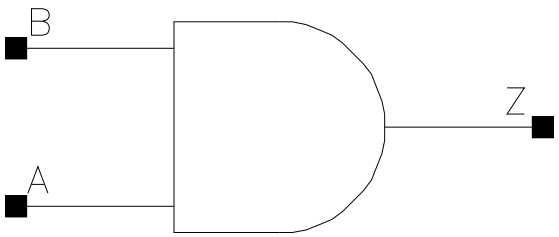
The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description	Logical Symbol
2 input AND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.544	0.4352
X10_P0	0.800	0.680	0.5440
X11_P0	1.600	0.544	0.8704
X19_P0	0.800	1.224	0.9792
X24_P0	0.800	1.360	1.0880
X29_P0	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X11_P0	X19_P0
A	0.0005	0.0006	0.0008	0.0013
B	0.0004	0.0006	0.0008	0.0012
	X24_P0	X29_P0		
A	0.0013	0.0013		
B	0.0012	0.0011		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0239	0.0196	2.8215	1.3490
A to Z ↑	0.0191	0.0178	4.0302	1.9333
B to Z ↓	0.0229	0.0184	2.8209	1.3491
B to Z ↑	0.0205	0.0190	4.0329	1.9322
	X11_P0	**X19_P0**	**X11_P0**	**X19_P0**

A to Z ↓	0.0212	0.0192	1.0632	0.6956
A to Z ↑	0.0163	0.0175	1.8450	0.9728
B to Z ↓	0.0199	0.0185	1.0628	0.6946
B to Z ↑	0.0174	0.0188	1.8455	0.9738
	X24_P0	**X29_P0**	**X24_P0**	**X29_P0**
A to Z ↓	0.0208	0.0220	0.5661	0.4713
A to Z ↑	0.0191	0.0204	0.7809	0.6480
B to Z ↓	0.0202	0.0215	0.5654	0.4716
B to Z ↑	0.0206	0.0220	0.7805	0.6477

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	6.386e-06	1.000e-20
X10_P0	1.620e-05	1.000e-20
X11_P0	1.776e-05	1.000e-20
X19_P0	3.048e-05	1.000e-20
X24_P0	3.552e-05	1.000e-20
X29_P0	4.056e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X11_P0	X19_P0
A (output stable)	1.012e-05	1.984e-05	2.658e-05	3.772e-05
B (output stable)	2.135e-05	4.015e-05	5.350e-05	8.146e-05
A to Z	1.558e-03	2.643e-03	3.137e-03	5.210e-03
B to Z	1.502e-03	2.559e-03	2.988e-03	5.013e-03
	X24_P0	X29_P0		
A (output stable)	3.749e-05	3.790e-05		
B (output stable)	8.185e-05	8.230e-05		
A to Z	6.315e-03	7.342e-03		
B to Z	6.132e-03	7.183e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

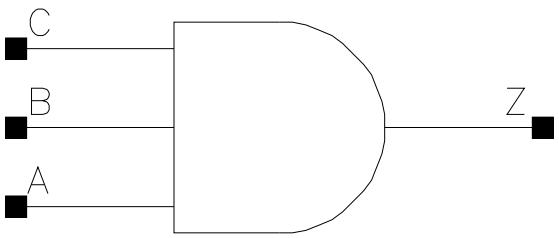
Pin Cycle (vdds)	X5_P0	X10_P0	X11_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P0	X29_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.680	0.5440
X10_P0	0.800	0.816	0.6528
X14_P0	0.800	1.360	1.0880
X19_P0	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0005	0.0007	0.0011	0.0013
B	0.0004	0.0006	0.0009	0.0012
C	0.0004	0.0006	0.0009	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0268	0.0219	2.8536	1.3576
A to Z ↑	0.0253	0.0232	4.0848	1.9531
B to Z ↓	0.0261	0.0209	2.8532	1.3582
B to Z ↑	0.0268	0.0243	4.0809	1.9565
C to Z ↓	0.0252	0.0200	2.8511	1.3564
C to Z ↑	0.0278	0.0249	4.0814	1.9537
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0222	0.0211	0.9403	0.6975

A to Z ↑	0.0224	0.0219	1.3295	0.9814
B to Z ↓	0.0212	0.0201	0.9402	0.6973
B to Z ↑	0.0236	0.0232	1.3294	0.9806
C to Z ↓	0.0202	0.0191	0.9395	0.6973
C to Z ↑	0.0245	0.0239	1.3292	0.9804

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	6.551e-06	1.000e-20
X10_P0	1.625e-05	1.000e-20
X14_P0	2.219e-05	1.000e-20
X19_P0	3.088e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	1.058e-05	2.095e-05	2.823e-05	3.825e-05
B (output stable)	2.427e-05	4.586e-05	6.550e-05	9.084e-05
C (output stable)	4.509e-05	8.457e-05	1.222e-04	1.752e-04
A to Z	1.810e-03	3.051e-03	4.500e-03	5.887e-03
B to Z	1.748e-03	2.942e-03	4.314e-03	5.647e-03
C to Z	1.698e-03	2.846e-03	4.173e-03	5.432e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

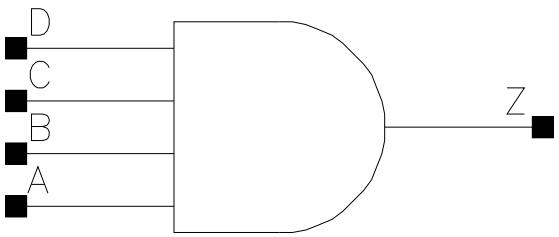
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.088	0.8704
X3_P0	0.800	1.088	0.8704
X10_P0	0.800	2.176	1.7408
X13_P0	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P0	X3_P0	X10_P0	X13_P0
A	0.0005	0.0005	0.0010	0.0011
B	0.0004	0.0004	0.0010	0.0011
C	0.0004	0.0004	0.0009	0.0011
D	0.0005	0.0005	0.0009	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	X3_P0	X2_P0	X3_P0
A to Z ↓	0.0212	0.0227	5.1656	3.4327
A to Z ↑	0.0219	0.0219	14.4610	7.8036
B to Z ↓	0.0200	0.0218	5.1598	3.4354
B to Z ↑	0.0231	0.0233	14.4698	7.8062
C to Z ↓	0.0218	0.0234	5.1563	3.4210
C to Z ↑	0.0218	0.0218	14.4778	7.8191

D to Z ↓	0.0208	0.0229	5.1574	3.4233
D to Z ↑	0.0233	0.0240	14.4836	7.8186
	X10_P0	**X13_P0**	**X10_P0**	**X13_P0**
A to Z ↓	0.0214	0.0215	1.1804	0.8797
A to Z ↑	0.0209	0.0228	2.6013	1.9971
B to Z ↓	0.0205	0.0198	1.1795	0.8784
B to Z ↑	0.0221	0.0234	2.6013	1.9974
C to Z ↓	0.0215	0.0206	1.1738	0.8804
C to Z ↑	0.0201	0.0199	2.6003	1.9947
D to Z ↓	0.0196	0.0189	1.1707	0.8801
D to Z ↑	0.0206	0.0204	2.6003	1.9933

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P0	4.054e-06	1.000e-20
X3_P0	6.051e-06	1.000e-20
X10_P0	2.032e-05	1.000e-20
X13_P0	2.913e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P0	X3_P0	X10_P0	X13_P0
A (output stable)	3.421e-04	4.005e-04	1.052e-03	1.443e-03
B (output stable)	3.229e-04	3.786e-04	9.978e-04	1.384e-03
C (output stable)	3.520e-04	3.849e-04	1.017e-03	1.299e-03
D (output stable)	3.311e-04	3.725e-04	9.738e-04	1.238e-03
A to Z	1.247e-03	1.632e-03	4.573e-03	6.221e-03
B to Z	1.189e-03	1.568e-03	4.410e-03	5.853e-03
C to Z	1.276e-03	1.633e-03	4.115e-03	5.204e-03
D to Z	1.219e-03	1.593e-03	3.806e-03	4.841e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

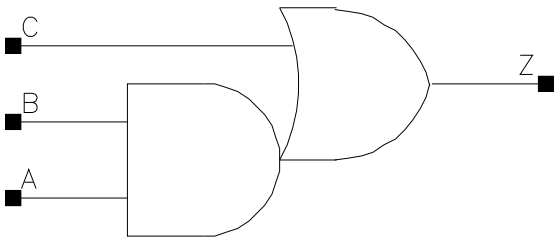
Pin Cycle (vdds)	X2_P0	X3_P0	X10_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	0.952	0.7616
X19_P0	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0004	0.0006	0.0012
B	0.0004	0.0006	0.0010
C	0.0005	0.0006	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0325	0.0288	2.7051	1.3563
A to Z ↑	0.0213	0.0195	3.7312	1.9018
B to Z ↓	0.0306	0.0271	2.6980	1.3519
B to Z ↑	0.0231	0.0211	3.7331	1.9051
C to Z ↓	0.0325	0.0278	2.6924	1.3503
C to Z ↑	0.0201	0.0183	3.7051	1.8905
	X19_P0		**X19_P0**	
A to Z ↓	0.0277		0.7073	
A to Z ↑	0.0213		0.9621	

B to Z ↓	0.0268		0.7079	
B to Z ↑	0.0230		0.9623	
C to Z ↓	0.0272		0.7062	
C to Z ↑	0.0196		0.9534	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	5.923e-06	1.000e-20
X10_P0	1.288e-05	1.000e-20
X19_P0	2.376e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	2.083e-05	4.373e-05	9.196e-05
B (output stable)	2.441e-05	5.179e-05	1.051e-04
C (output stable)	4.661e-05	6.219e-05	1.470e-04
A to Z	1.810e-03	3.021e-03	5.804e-03
B to Z	1.750e-03	2.918e-03	5.676e-03
C to Z	1.965e-03	3.187e-03	6.157e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

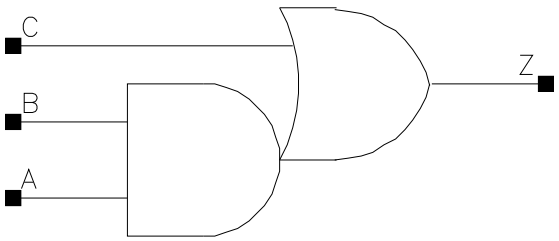
Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	0.952	0.7616
X14_P0	0.800	1.632	1.3056
X19_P0	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0006	0.0012	0.0012
B	0.0004	0.0006	0.0012	0.0012
C	0.0005	0.0006	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0335	0.0293	2.6952	1.3646
A to Z ↑	0.0232	0.0214	3.8099	1.9256
B to Z ↓	0.0322	0.0280	2.6881	1.3627
B to Z ↑	0.0254	0.0230	3.8152	1.9260
C to Z ↓	0.0295	0.0267	2.6805	1.3588
C to Z ↑	0.0175	0.0158	3.7727	1.9066
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0267	0.0286	0.9362	0.7021

A to Z ↑	0.0198	0.0210	1.3097	0.9752
B to Z ↓	0.0243	0.0264	0.9335	0.7005
B to Z ↑	0.0207	0.0221	1.3099	0.9752
C to Z ↓	0.0225	0.0246	0.9316	0.6986
C to Z ↑	0.0139	0.0149	1.2962	0.9637

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	5.962e-06	1.000e-20
X10_P0	1.246e-05	1.000e-20
X14_P0	2.215e-05	1.000e-20
X19_P0	2.534e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	1.535e-05	1.981e-05	6.389e-05	6.389e-05
B (output stable)	2.045e-05	2.596e-05	1.132e-04	1.117e-04
C (output stable)	1.003e-04	1.493e-04	4.171e-04	4.170e-04
A to Z	1.983e-03	3.089e-03	5.358e-03	6.382e-03
B to Z	1.925e-03	2.994e-03	4.973e-03	6.020e-03
C to Z	1.696e-03	2.709e-03	4.388e-03	5.352e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

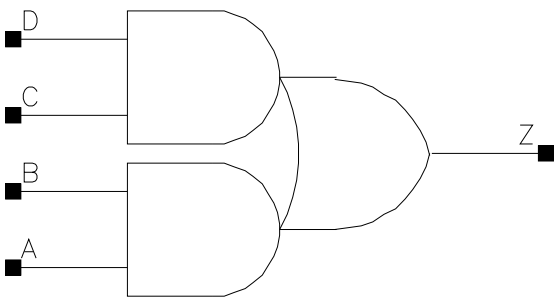
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.088	0.8704
X10_P0	0.800	1.088	0.8704
X14_P0	0.800	1.768	1.4144
X19_P0	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0005	0.0006	0.0012	0.0012
B	0.0005	0.0008	0.0011	0.0011
C	0.0004	0.0006	0.0013	0.0013
D	0.0005	0.0006	0.0011	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0344	0.0292	2.7088	1.3653
A to Z ↑	0.0245	0.0225	3.8466	1.9058
B to Z ↓	0.0317	0.0268	2.7000	1.3608

B to Z ↑	0.0254	0.0236	3.8473	1.9063
C to Z ↓	0.0312	0.0269	2.7001	1.3620
C to Z ↑	0.0208	0.0189	3.8387	1.9014
D to Z ↓	0.0300	0.0256	2.6972	1.3601
D to Z ↑	0.0226	0.0205	3.8413	1.8993
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0265	0.0285	0.9356	0.7056
A to Z ↑	0.0202	0.0216	1.3160	0.9839
B to Z ↓	0.0249	0.0271	0.9351	0.7050
B to Z ↑	0.0216	0.0232	1.3150	0.9833
C to Z ↓	0.0245	0.0267	0.9343	0.7043
C to Z ↑	0.0174	0.0188	1.3104	0.9804
D to Z ↓	0.0232	0.0254	0.9340	0.7041
D to Z ↑	0.0185	0.0201	1.3098	0.9799

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	7.594e-06	1.000e-20
X10_P0	1.648e-05	1.000e-20
X14_P0	2.744e-05	1.000e-20
X19_P0	3.156e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	2.992e-05	4.075e-05	5.425e-05	5.441e-05
B (output stable)	1.182e-04	1.267e-04	7.598e-05	7.623e-05
C (output stable)	3.365e-05	4.643e-05	1.069e-04	1.071e-04
D (output stable)	3.740e-05	6.027e-05	1.332e-04	1.344e-04
A to Z	2.261e-03	3.473e-03	5.595e-03	6.735e-03
B to Z	2.069e-03	3.192e-03	5.334e-03	6.483e-03
C to Z	1.943e-03	3.011e-03	4.780e-03	5.897e-03
D to Z	1.876e-03	2.919e-03	4.572e-03	5.686e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

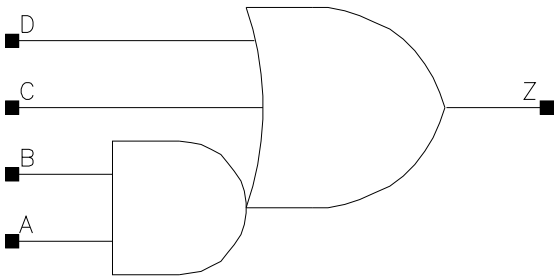
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	1.088	0.8704
X19_P0	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0004	0.0006	0.0011
B	0.0004	0.0006	0.0011
C	0.0005	0.0005	0.0012
D	0.0004	0.0006	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0402	0.0344	2.9929	1.4122
A to Z ↑	0.0223	0.0190	3.9907	1.9174
B to Z ↓	0.0390	0.0323	2.9891	1.4083
B to Z ↑	0.0240	0.0204	3.9918	1.9168
C to Z ↓	0.0415	0.0353	2.9826	1.4075
C to Z ↑	0.0206	0.0253	3.9599	1.9200

D to Z ↓	0.0417	0.0361	2.9828	1.4081
D to Z ↑	0.0204	0.0249	3.9592	1.9189
	X19_P0		**X19_P0**	
A to Z ↓	0.0342		0.7315	
A to Z ↑	0.0210		0.9525	
B to Z ↓	0.0313		0.7290	
B to Z ↑	0.0218		0.9522	
C to Z ↓	0.0344		0.7288	
C to Z ↑	0.0209		0.9464	
D to Z ↓	0.0343		0.7289	
D to Z ↑	0.0206		0.9467	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	4.127e-06	1.000e-20
X10_P0	1.023e-05	1.000e-20
X19_P0	1.883e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	2.295e-05	5.388e-05	1.052e-04
B (output stable)	2.391e-05	5.544e-05	1.283e-04
C (output stable)	2.323e-05	4.116e-05	8.822e-05
D (output stable)	2.462e-05	4.962e-05	9.494e-05
A to Z	1.919e-03	3.189e-03	6.243e-03
B to Z	1.866e-03	3.072e-03	5.863e-03
C to Z	2.121e-03	3.626e-03	6.895e-03
D to Z	2.033e-03	3.479e-03	6.542e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

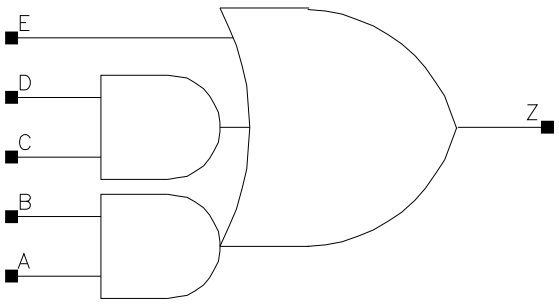
Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.088	0.8704
X10_P0	0.800	1.224	0.9792
X19_P0	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0004	0.0006	0.0011
B	0.0004	0.0006	0.0010
C	0.0004	0.0008	0.0012
D	0.0004	0.0006	0.0010
E	0.0004	0.0006	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0494	0.0393	2.8238	1.4046
A to Z ↑	0.0281	0.0238	3.8851	1.9253

B to Z ↓	0.0489	0.0378	2.8192	1.4031
B to Z ↑	0.0308	0.0255	3.8850	1.9268
C to Z ↓	0.0444	0.0359	2.8181	1.4026
C to Z ↑	0.0247	0.0203	3.8597	1.9152
D to Z ↓	0.0420	0.0328	2.8082	1.3969
D to Z ↑	0.0267	0.0216	3.8550	1.9146
E to Z ↓	0.0445	0.0353	2.8028	1.3974
E to Z ↑	0.0220	0.0187	3.8196	1.9006
	X19_P0		**X19_P0**	
A to Z ↓	0.0382		0.7249	
A to Z ↑	0.0245		0.9663	
B to Z ↓	0.0365		0.7241	
B to Z ↑	0.0265		0.9669	
C to Z ↓	0.0337		0.7228	
C to Z ↑	0.0205		0.9599	
D to Z ↓	0.0321		0.7215	
D to Z ↑	0.0221		0.9592	
E to Z ↓	0.0341		0.7211	
E to Z ↑	0.0231		0.9568	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	5.518e-06	1.000e-20
X10_P0	1.298e-05	1.000e-20
X19_P0	2.357e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	1.453e-05	2.574e-05	5.161e-05
B (output stable)	2.098e-05	2.911e-05	5.398e-05
C (output stable)	3.363e-05	5.668e-05	1.178e-04
D (output stable)	3.629e-05	6.741e-05	1.273e-04
E (output stable)	5.731e-05	1.035e-04	2.128e-04
A to Z	2.590e-03	3.992e-03	7.666e-03
B to Z	2.554e-03	3.869e-03	7.426e-03
C to Z	2.199e-03	3.340e-03	6.300e-03
D to Z	2.128e-03	3.196e-03	6.116e-03
E to Z	2.277e-03	3.498e-03	6.720e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

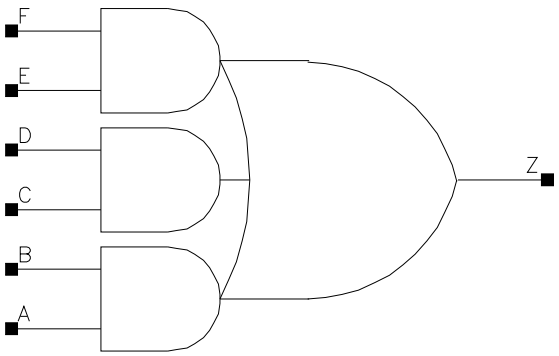
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.360	1.0880
X5_P0	0.800	1.360	1.0880
X10_P0	0.800	1.632	1.3056
X19_P0	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P0	X5_P0	X10_P0	X19_P0
A	0.0005	0.0005	0.0007	0.0011

B	0.0005	0.0005	0.0008	0.0010
C	0.0007	0.0007	0.0005	0.0011
D	0.0005	0.0005	0.0005	0.0010
E	0.0007	0.0007	0.0006	0.0012
F	0.0005	0.0005	0.0006	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X5_P0**	**X2_P0**	**X5_P0**
A to Z ↓	0.0389	0.0400	5.3219	2.9061
A to Z ↑	0.0275	0.0271	7.5880	4.0716
B to Z ↓	0.0372	0.0384	5.3062	2.8983
B to Z ↑	0.0298	0.0295	7.5845	4.0711
C to Z ↓	0.0365	0.0377	5.3210	2.9055
C to Z ↑	0.0256	0.0253	7.5235	4.0453
D to Z ↓	0.0336	0.0348	5.3054	2.8977
D to Z ↑	0.0271	0.0268	7.5186	4.0440
E to Z ↓	0.0308	0.0319	5.2998	2.8954
E to Z ↑	0.0213	0.0210	7.4757	4.0253
F to Z ↓	0.0285	0.0299	5.2873	2.8890
F to Z ↑	0.0226	0.0225	7.4787	4.0265
	X10_P0	**X19_P0**	**X10_P0**	**X19_P0**
A to Z ↓	0.0427	0.0397	1.4025	0.7223
A to Z ↑	0.0290	0.0264	1.9368	0.9706
B to Z ↓	0.0404	0.0383	1.3969	0.7217
B to Z ↑	0.0306	0.0285	1.9371	0.9704
C to Z ↓	0.0395	0.0371	1.3998	0.7219
C to Z ↑	0.0259	0.0244	1.9265	0.9654
D to Z ↓	0.0381	0.0360	1.3969	0.7214
D to Z ↑	0.0280	0.0264	1.9264	0.9650
E to Z ↓	0.0351	0.0340	1.3959	0.7201
E to Z ↑	0.0223	0.0214	1.9191	0.9620
F to Z ↓	0.0332	0.0322	1.3922	0.7188
F to Z ↑	0.0239	0.0231	1.9174	0.9621

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P0	6.479e-06	1.000e-20
X5_P0	8.730e-06	1.000e-20
X10_P0	1.530e-05	1.000e-20
X19_P0	2.970e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P0	X5_P0	X10_P0	X19_P0
A (output stable)	2.940e-05	2.940e-05	4.483e-05	6.737e-05
B (output stable)	3.229e-05	3.228e-05	9.319e-05	7.601e-05
C (output stable)	3.834e-05	3.840e-05	4.368e-05	8.691e-05
D (output stable)	4.366e-05	4.369e-05	5.161e-05	1.045e-04
E (output stable)	6.267e-05	6.278e-05	8.862e-05	1.469e-04
F (output stable)	7.008e-05	7.017e-05	9.215e-05	1.609e-04

A to Z	2.454e-03	2.826e-03	4.482e-03	8.230e-03
B to Z	2.362e-03	2.734e-03	4.233e-03	8.000e-03
C to Z	2.062e-03	2.429e-03	3.967e-03	7.325e-03
D to Z	1.955e-03	2.321e-03	3.873e-03	7.148e-03
E to Z	1.651e-03	2.004e-03	3.485e-03	6.571e-03
F to Z	1.571e-03	1.924e-03	3.386e-03	6.363e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

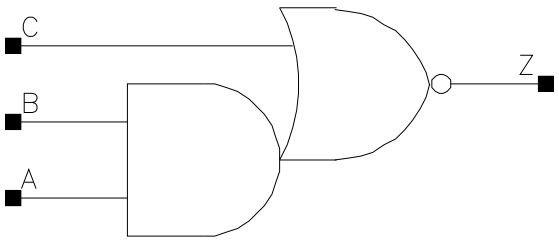
Pin Cycle (vdds)	X2_P0	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X10_P0	0.800	1.360	1.0880
X19_P0	0.800	2.584	2.0672
X25_P0	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P0	X10_P0	X19_P0	X25_P0
A	0.0006	0.0014	0.0028	0.0037
B	0.0005	0.0013	0.0026	0.0035
C	0.0005	0.0015	0.0028	0.0038

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X10_P0**	**X3_P0**	**X10_P0**
A to Z ↓	0.0075	0.0079	4.5764	1.6599
A to Z ↑	0.0141	0.0143	7.5339	2.5802
B to Z ↓	0.0078	0.0082	4.6330	1.6820
B to Z ↑	0.0119	0.0116	7.3744	2.5712
C to Z ↓	0.0077	0.0079	2.8436	0.9912
C to Z ↑	0.0137	0.0139	6.8720	2.3777
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0083	0.0083	0.8497	0.6491

A to Z ↑	0.0148	0.0146	1.3240	0.9854
B to Z ↓	0.0083	0.0083	0.8613	0.6582
B to Z ↑	0.0118	0.0117	1.3215	0.9977
C to Z ↓	0.0094	0.0094	0.6024	0.4607
C to Z ↑	0.0142	0.0140	1.2228	0.9160

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	5.783e-06	1.000e-20
X10_P0	1.500e-05	1.000e-20
X19_P0	2.867e-05	1.000e-20
X25_P0	3.796e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X10_P0	X19_P0	X25_P0
A (output stable)	4.490e-05	1.513e-04	3.031e-04	3.973e-04
B (output stable)	5.614e-05	2.083e-04	4.304e-04	5.535e-04
C (output stable)	6.557e-05	2.110e-04	4.185e-04	5.717e-04
A to Z	8.167e-04	2.512e-03	5.162e-03	6.757e-03
B to Z	7.222e-04	2.052e-03	4.156e-03	5.492e-03
C to Z	1.067e-03	3.160e-03	6.252e-03	8.325e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

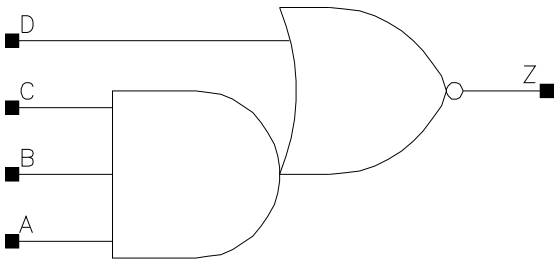
Pin Cycle (vdds)	X3_P0	X10_P0	X19_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X17_P0	0.800	3.536	2.8288
X22_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X17_P0	X22_P0
A	0.0005	0.0028	0.0038
B	0.0005	0.0026	0.0036
C	0.0006	0.0025	0.0035
D	0.0006	0.0030	0.0038

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X17_P0	X3_P0	X17_P0
A to Z ↓	0.0114	0.0122	6.3618	1.2255
A to Z ↑	0.0182	0.0176	7.5384	1.2725
B to Z ↓	0.0122	0.0126	6.3957	1.2336
B to Z ↑	0.0166	0.0159	7.5518	1.2942
C to Z ↓	0.0131	0.0121	6.4376	1.2402
C to Z ↑	0.0157	0.0132	7.5757	1.3020
D to Z ↓	0.0097	0.0112	2.7772	0.5937

D to Z ↑	0.0176	0.0163	6.5116	1.1103
	X22_P0		**X22_P0**	
A to Z ↓	0.0121		0.9320	
A to Z ↑	0.0174		0.9524	
B to Z ↓	0.0124		0.9389	
B to Z ↑	0.0155		0.9720	
C to Z ↓	0.0120		0.9443	
C to Z ↑	0.0131		0.9809	
D to Z ↓	0.0117		0.4919	
D to Z ↑	0.0158		0.8316	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	5.954e-06	1.000e-20
X17_P0	2.772e-05	1.000e-20
X22_P0	3.614e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X17_P0	X22_P0
A (output stable)	3.270e-05	2.025e-04	2.692e-04
B (output stable)	4.317e-05	3.081e-04	4.055e-04
C (output stable)	6.057e-05	5.140e-04	6.702e-04
D (output stable)	9.607e-05	5.817e-04	7.652e-04
A to Z	1.200e-03	6.833e-03	8.900e-03
B to Z	1.072e-03	5.808e-03	7.534e-03
C to Z	9.759e-04	4.839e-03	6.285e-03
D to Z	1.500e-03	7.972e-03	1.034e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

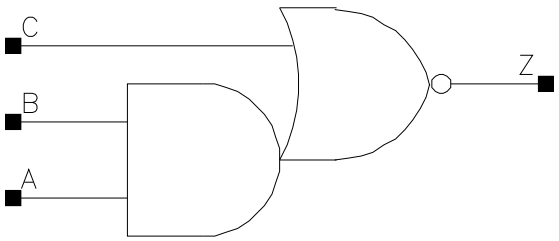
Pin Cycle (vdds)	X3_P0	X17_P0	X22_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X6_P0	0.800	1.088	0.8704
X9_P0	0.800	1.360	1.0880
X12_P0	0.800	1.904	1.5232
X25_P0	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X9_P0	X12_P0
A	0.0005	0.0010	0.0015	0.0021
B	0.0004	0.0010	0.0014	0.0019
C	0.0006	0.0009	0.0013	0.0018
	X25_P0			
A	0.0041			
B	0.0038			
C	0.0035			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0104	0.0101	5.9750	2.4184
A to Z ↑	0.0153	0.0162	8.5837	3.8357
B to Z ↓	0.0116	0.0103	6.0233	2.4466

B to Z ↑	0.0138	0.0135	8.4507	3.8482
C to Z ↓	0.0064	0.0055	3.7420	1.7852
C to Z ↑	0.0124	0.0113	7.8598	3.5436
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0096	0.0100	1.6635	1.2503
A to Z ↑	0.0150	0.0152	2.5682	1.8993
B to Z ↓	0.0102	0.0101	1.6851	1.2657
B to Z ↑	0.0124	0.0126	2.5683	1.9249
C to Z ↓	0.0055	0.0054	1.2189	0.9109
C to Z ↑	0.0107	0.0109	2.3750	1.7693
	X25_P0		**X25_P0**	
A to Z ↓	0.0099		0.6517	
A to Z ↑	0.0148		0.9657	
B to Z ↓	0.0102		0.6591	
B to Z ↑	0.0122		0.9699	
C to Z ↓	0.0054		0.4636	
C to Z ↑	0.0105		0.8966	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	4.535e-06	1.000e-20
X6_P0	1.081e-05	1.000e-20
X9_P0	1.516e-05	1.000e-20
X12_P0	2.018e-05	1.000e-20
X25_P0	3.902e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	1.997e-05	6.317e-05	8.366e-05	1.215e-04
B (output stable)	2.515e-05	1.118e-04	1.337e-04	2.117e-04
C (output stable)	1.580e-04	4.057e-04	5.153e-04	7.145e-04
A to Z	9.449e-04	2.310e-03	3.156e-03	4.361e-03
B to Z	8.591e-04	1.945e-03	2.635e-03	3.590e-03
C to Z	6.533e-04	1.437e-03	1.986e-03	2.747e-03
	X25_P0			
A (output stable)	2.341e-04			
B (output stable)	3.755e-04			
C (output stable)	1.338e-03			
A to Z	8.315e-03			
B to Z	6.918e-03			
C to Z	5.213e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

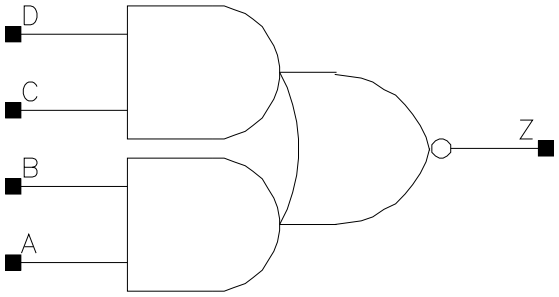
	X25_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.680	0.5440
X6_P0	0.800	1.224	0.9792
X9_P0	0.800	1.768	1.4144
X12_P0	0.800	2.448	1.9584
X24_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P0	X6_P0	X9_P0	X12_P0
A	0.0004	0.0011	0.0015	0.0020
B	0.0004	0.0009	0.0014	0.0021
C	0.0004	0.0011	0.0014	0.0019
D	0.0004	0.0009	0.0013	0.0018
	X24_P0			
A	0.0040			
B	0.0040			
C	0.0038			
D	0.0037			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X6_P0**	**X2_P0**	**X6_P0**
A to Z ↓	0.0104	0.0107	6.0866	2.3167
A to Z ↑	0.0194	0.0167	10.7213	3.5072
B to Z ↓	0.0115	0.0117	6.1557	2.3405
B to Z ↑	0.0175	0.0150	10.6845	3.5829
C to Z ↓	0.0075	0.0075	6.1120	2.3282
C to Z ↑	0.0158	0.0138	10.6497	3.4827
D to Z ↓	0.0081	0.0080	6.1979	2.3598
D to Z ↑	0.0137	0.0122	10.6023	3.5919
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0116	0.0119	1.6640	1.2547
A to Z ↑	0.0175	0.0179	2.3554	1.7712
B to Z ↓	0.0126	0.0126	1.6828	1.2682
B to Z ↑	0.0154	0.0156	2.3579	1.7489
C to Z ↓	0.0081	0.0086	1.6616	1.2580
C to Z ↑	0.0145	0.0149	2.3411	1.7474
D to Z ↓	0.0086	0.0085	1.6859	1.2758
D to Z ↑	0.0121	0.0123	2.3387	1.7527
	X24_P0		**X24_P0**	
A to Z ↓	0.0120		0.6486	
A to Z ↑	0.0176		0.8957	
B to Z ↓	0.0128		0.6556	
B to Z ↑	0.0153		0.8882	
C to Z ↓	0.0087		0.6342	
C to Z ↑	0.0150		0.8876	
D to Z ↓	0.0087		0.6441	
D to Z ↑	0.0123		0.8901	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P0	3.473e-06	1.000e-20
X6_P0	1.295e-05	1.000e-20
X9_P0	1.777e-05	1.000e-20
X12_P0	2.349e-05	1.000e-20
X24_P0	4.536e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P0	X6_P0	X9_P0	X12_P0
A (output stable)	2.103e-05	5.381e-05	1.036e-04	1.495e-04
B (output stable)	2.715e-05	7.613e-05	2.024e-04	3.226e-04
C (output stable)	3.857e-05	1.037e-04	1.806e-04	2.563e-04
D (output stable)	4.781e-05	1.325e-04	2.705e-04	4.189e-04
A to Z	9.802e-04	2.582e-03	4.040e-03	5.543e-03
B to Z	8.771e-04	2.306e-03	3.527e-03	4.843e-03
C to Z	6.364e-04	1.735e-03	2.745e-03	3.816e-03
D to Z	5.536e-04	1.517e-03	2.303e-03	3.148e-03
	X24_P0			
A (output stable)	2.758e-04			
B (output stable)	5.443e-04			
C (output stable)	4.963e-04			
D (output stable)	7.995e-04			

A to Z	1.074e-02			
B to Z	9.399e-03			
C to Z	7.459e-03			
D to Z	6.205e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

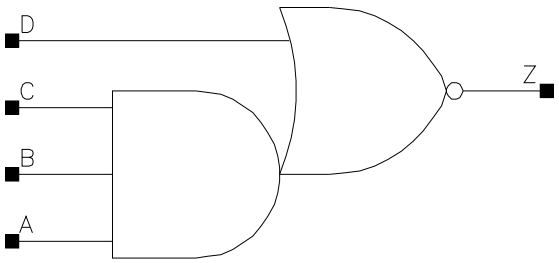
Pin Cycle (vdds)	X2_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X12_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X12_P0
A	0.0005	0.0020
B	0.0005	0.0019
C	0.0007	0.0018
D	0.0005	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X12_P0	X3_P0	X12_P0
A to Z ↓	0.0131	0.0136	6.3722	1.8179
A to Z ↑	0.0190	0.0181	7.3661	1.9286
B to Z ↓	0.0144	0.0140	6.4019	1.8268
B to Z ↑	0.0179	0.0163	7.4712	1.9295
C to Z ↓	0.0160	0.0139	6.4404	1.8348
C to Z ↑	0.0175	0.0138	7.5225	1.9423
D to Z ↓	0.0059	0.0050	2.8415	0.7741
D to Z ↑	0.0133	0.0114	6.3734	1.6509

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	6.221e-06	1.000e-20
X12_P0	2.025e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X12_P0
A (output stable)	1.628e-05	8.130e-05
B (output stable)	2.671e-05	1.565e-04
C (output stable)	4.790e-05	2.763e-04
D (output stable)	3.017e-04	1.021e-03
A to Z	1.473e-03	5.403e-03
B to Z	1.347e-03	4.637e-03
C to Z	1.269e-03	3.951e-03
D to Z	9.203e-04	3.029e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

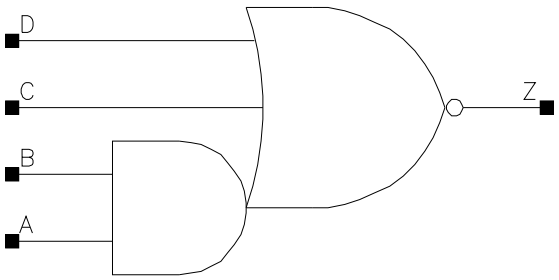
Pin Cycle (vdds)	X3_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X20_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P0	X20_P0
A	0.0005	0.0037
B	0.0005	0.0034
C	0.0005	0.0036
D	0.0005	0.0034

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X20_P0**	**X3_P0**	**X20_P0**
A to Z ↓	0.0088	0.0097	4.4882	0.7340
A to Z ↑	0.0190	0.0178	10.9349	1.4257
B to Z ↓	0.0096	0.0101	4.5451	0.7450
B to Z ↑	0.0171	0.0147	11.0351	1.4259
C to Z ↓	0.0095	0.0134	2.8148	0.5871
C to Z ↑	0.0213	0.0199	10.4345	1.3503
D to Z ↓	0.0091	0.0122	2.8182	0.5869

D to Z ↑	0.0218	0.0189	10.4620	1.3557

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	4.951e-06	1.000e-20
X20_P0	2.978e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X20_P0
A (output stable)	5.544e-05	3.974e-04
B (output stable)	6.004e-05	4.572e-04
C (output stable)	4.147e-05	4.464e-04
D (output stable)	4.979e-05	5.015e-04
A to Z	1.027e-03	7.007e-03
B to Z	9.227e-04	5.839e-03
C to Z	1.477e-03	1.057e-02
D to Z	1.324e-03	8.666e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

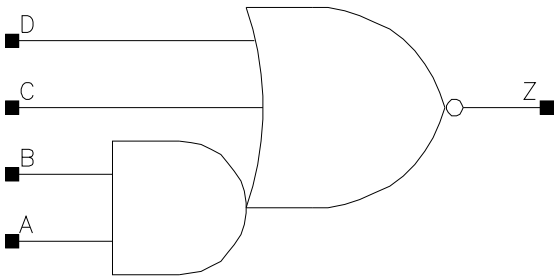
Pin Cycle (vdds)	X3_P0	X20_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.816	0.6528
X10_P0	0.800	2.448	1.9584
X19_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P0	X10_P0	X19_P0
A	0.0005	0.0019	0.0039
B	0.0005	0.0018	0.0037
C	0.0006	0.0016	0.0032
D	0.0004	0.0016	0.0030

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	X10_P0	X2_P0	X10_P0
A to Z ↓	0.0116	0.0118	5.3101	1.4208
A to Z ↑	0.0222	0.0204	11.5960	2.8411
B to Z ↓	0.0129	0.0124	5.3709	1.4364
B to Z ↑	0.0202	0.0176	11.6363	2.8484
C to Z ↓	0.0105	0.0096	4.7075	1.1836
C to Z ↑	0.0171	0.0151	11.0385	2.6971

D to Z ↓	0.0089	0.0072	4.7430	1.1960
D to Z ↑	0.0160	0.0131	11.0440	2.7043
	X19_P0		**X19_P0**	
A to Z ↓	0.0115		0.7295	
A to Z ↑	0.0199		1.4454	
B to Z ↓	0.0124		0.7384	
B to Z ↑	0.0170		1.4447	
C to Z ↓	0.0101		0.6370	
C to Z ↑	0.0146		1.3711	
D to Z ↓	0.0076		0.6440	
D to Z ↑	0.0125		1.3751	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P0	4.114e-06	1.000e-20
X10_P0	1.728e-05	1.000e-20
X19_P0	3.423e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P0	X10_P0	X19_P0
A (output stable)	2.296e-05	9.631e-05	1.902e-04
B (output stable)	2.282e-05	1.366e-04	2.549e-04
C (output stable)	4.405e-05	2.352e-04	4.728e-04
D (output stable)	8.566e-05	4.488e-04	8.691e-04
A to Z	1.389e-03	5.189e-03	9.965e-03
B to Z	1.270e-03	4.480e-03	8.643e-03
C to Z	9.026e-04	3.439e-03	6.501e-03
D to Z	7.715e-04	2.624e-03	4.906e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

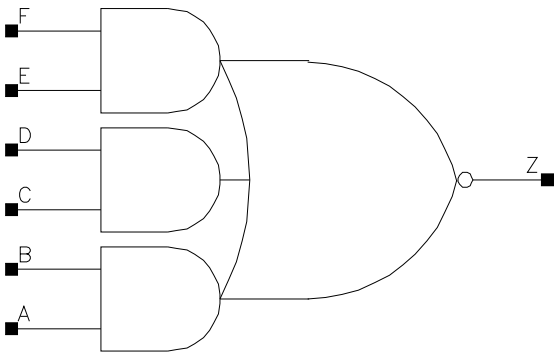
Pin Cycle (vdds)	X2_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.088	0.8704
X5_P0	0.800	2.040	1.6320
X7_P0	0.800	2.720	2.1760
X9_P0	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P0	X5_P0	X7_P0	X9_P0
A	0.0005	0.0009	0.0015	0.0019

B	0.0005	0.0010	0.0013	0.0018
C	0.0005	0.0009	0.0014	0.0021
D	0.0005	0.0010	0.0013	0.0017
E	0.0006	0.0010	0.0013	0.0017
F	0.0005	0.0008	0.0012	0.0017

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X5_P0**	**X2_P0**	**X5_P0**
A to Z ↓	0.0127	0.0154	4.7415	2.6937
A to Z ↑	0.0286	0.0268	11.2548	5.1354
B to Z ↓	0.0141	0.0171	4.7972	2.7126
B to Z ↑	0.0264	0.0253	11.2964	5.0923
C to Z ↓	0.0117	0.0139	4.7823	2.6844
C to Z ↑	0.0253	0.0242	11.3355	5.1513
D to Z ↓	0.0129	0.0153	4.8517	2.7083
D to Z ↑	0.0231	0.0228	11.3116	5.1241
E to Z ↓	0.0090	0.0107	4.8188	2.6367
E to Z ↑	0.0204	0.0201	11.2631	5.0868
F to Z ↓	0.0095	0.0116	4.8983	2.6643
F to Z ↑	0.0176	0.0180	11.2143	5.1051
	X7_P0	**X9_P0**	**X7_P0**	**X9_P0**
A to Z ↓	0.0150	0.0155	1.8756	1.4303
A to Z ↑	0.0259	0.0266	3.3661	2.5383
B to Z ↓	0.0164	0.0166	1.8915	1.4418
B to Z ↑	0.0239	0.0242	3.4411	2.5782
C to Z ↓	0.0136	0.0142	1.8830	1.4227
C to Z ↑	0.0236	0.0248	3.4375	2.5823
D to Z ↓	0.0148	0.0146	1.9028	1.4368
D to Z ↑	0.0211	0.0214	3.4052	2.5602
E to Z ↓	0.0101	0.0101	1.8815	1.4254
E to Z ↑	0.0189	0.0190	3.3818	2.5545
F to Z ↓	0.0109	0.0104	1.9078	1.4461
F to Z ↑	0.0166	0.0162	3.4099	2.5497

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P0	6.480e-06	1.000e-20
X5_P0	1.453e-05	1.000e-20
X7_P0	2.135e-05	1.000e-20
X9_P0	2.591e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

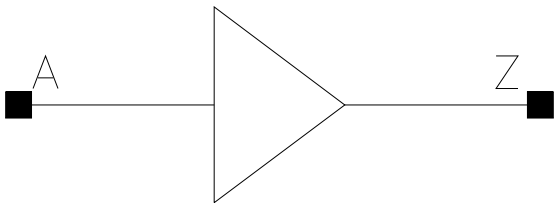
Pin Cycle (vdd)	X2_P0	X5_P0	X7_P0	X9_P0
A (output stable)	3.408e-05	6.412e-05	1.127e-04	1.561e-04
B (output stable)	3.814e-05	8.331e-05	1.656e-04	2.592e-04
C (output stable)	4.873e-05	9.740e-05	1.474e-04	2.088e-04
D (output stable)	5.694e-05	1.148e-04	2.085e-04	2.942e-04
E (output stable)	7.001e-05	1.584e-04	2.459e-04	3.394e-04
F (output stable)	8.467e-05	1.730e-04	2.985e-04	4.377e-04

A to Z	1.870e-03	3.830e-03	5.564e-03	7.590e-03
B to Z	1.733e-03	3.656e-03	5.083e-03	6.881e-03
C to Z	1.436e-03	3.033e-03	4.369e-03	5.938e-03
D to Z	1.315e-03	2.866e-03	3.944e-03	5.310e-03
E to Z	9.935e-04	2.277e-03	3.144e-03	4.160e-03
F to Z	8.894e-04	2.074e-03	2.757e-03	3.566e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P0	X5_P0	X7_P0	X9_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.544	0.4352
X5_P0	0.800	0.544	0.4352
X9_P0	0.800	0.680	0.5440
X11_P0	1.600	0.408	0.6528
X13_P0	0.800	0.680	0.5440
X19_P0	0.800	0.952	0.7616
X23_P0	1.600	0.544	0.8704
X24_P0	0.800	1.088	0.8704
X29_P0	0.800	1.224	0.9792
X34_P0	1.600	0.680	1.0880
X38_P0	0.800	1.632	1.3056
X46_P0	1.600	0.952	1.5232
X57_P0	0.800	2.312	1.8496
X68_P0	1.600	1.224	1.9584
X91_P0	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P0	X5_P0	X9_P0	X11_P0
A	0.0005	0.0005	0.0005	0.0007
	X13_P0	X19_P0	X23_P0	X24_P0
A	0.0007	0.0009	0.0011	0.0011
	X29_P0	X34_P0	X38_P0	X46_P0
A	0.0012	0.0014	0.0018	0.0018
	X57_P0	X68_P0	X91_P0	
A	0.0024	0.0025	0.0033	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X5_P0**	**X2_P0**	**X5_P0**
A to Z ↓	0.0197	0.0202	5.1197	2.7865
A to Z ↑	0.0153	0.0152	7.3971	3.9455
	X9_P0	**X11_P0**	**X9_P0**	**X11_P0**
A to Z ↓	0.0240	0.0225	1.4293	1.0677
A to Z ↑	0.0182	0.0162	1.9658	1.8420
	X13_P0	**X19_P0**	**X13_P0**	**X19_P0**
A to Z ↓	0.0214	0.0214	0.9806	0.6919
A to Z ↑	0.0172	0.0160	1.3703	0.9573
	X23_P0	**X24_P0**	**X23_P0**	**X24_P0**
A to Z ↓	0.0213	0.0211	0.5168	0.5654
A to Z ↑	0.0156	0.0165	0.9306	0.7672
	X29_P0	**X34_P0**	**X29_P0**	**X34_P0**
A to Z ↓	0.0203	0.0212	0.4680	0.3562
A to Z ↑	0.0162	0.0159	0.6445	0.6371
	X38_P0	**X46_P0**	**X38_P0**	**X46_P0**
A to Z ↓	0.0199	0.0207	0.3543	0.2677
A to Z ↑	0.0160	0.0152	0.4744	0.4789
	X57_P0	**X68_P0**	**X57_P0**	**X68_P0**
A to Z ↓	0.0208	0.0206	0.2384	0.1819
A to Z ↑	0.0167	0.0154	0.3187	0.3202
	X91_P0		**X91_P0**	
A to Z ↓	0.0217		0.1403	
A to Z ↑	0.0163		0.2411	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P0	3.157e-06	1.000e-20
X5_P0	5.866e-06	1.000e-20
X9_P0	1.071e-05	1.000e-20
X11_P0	1.346e-05	1.000e-20
X13_P0	1.701e-05	1.000e-20
X19_P0	2.099e-05	1.000e-20
X23_P0	2.692e-05	1.000e-20
X24_P0	2.685e-05	1.000e-20
X29_P0	3.281e-05	1.000e-20
X34_P0	3.833e-05	1.000e-20
X38_P0	4.425e-05	1.000e-20
X46_P0	4.887e-05	1.000e-20
X57_P0	6.332e-05	1.000e-20
X68_P0	7.309e-05	1.000e-20
X91_P0	9.260e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P0	X5_P0	X9_P0	X11_P0
A to Z	1.135e-03	1.446e-03	2.335e-03	2.786e-03
	X13_P0	X19_P0	X23_P0	X24_P0
A to Z	3.417e-03	4.633e-03	5.142e-03	5.763e-03
	X29_P0	X34_P0	X38_P0	X46_P0

A to Z	6.700e-03	7.682e-03	9.189e-03	9.858e-03
	X57_P0	X68_P0	X91_P0	
A to Z	1.361e-02	1.461e-02	1.975e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

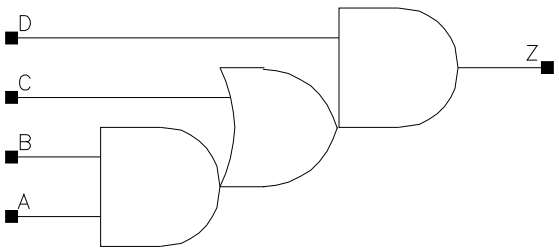
Pin Cycle (vdds)	X2_P0	X5_P0	X9_P0	X11_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P0	X19_P0	X23_P0	X24_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P0	X34_P0	X38_P0	X46_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P0	X68_P0	X91_P0	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.952	0.7616
X10_P0	0.800	1.632	1.3056
X14_P0	0.800	1.768	1.4144
X19_P0	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0006	0.0012	0.0012	0.0012
B	0.0006	0.0011	0.0011	0.0011
C	0.0006	0.0014	0.0014	0.0014
D	0.0009	0.0012	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0262	0.0240	2.8434	1.3445
A to Z ↑	0.0250	0.0229	4.0431	1.9231
B to Z ↓	0.0246	0.0223	2.8380	1.3416
B to Z ↑	0.0257	0.0233	4.0392	1.9208
C to Z ↓	0.0230	0.0209	2.8344	1.3399
C to Z ↑	0.0190	0.0170	4.0002	1.9042

D to Z ↓	0.0222	0.0191	2.8134	1.3302
D to Z ↑	0.0214	0.0182	4.0095	1.9076
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0267	0.0286	0.9386	0.7032
A to Z ↑	0.0254	0.0271	1.2928	0.9687
B to Z ↓	0.0252	0.0271	0.9383	0.7023
B to Z ↑	0.0260	0.0278	1.2917	0.9671
C to Z ↓	0.0236	0.0255	0.9348	0.7002
C to Z ↑	0.0191	0.0205	1.2751	0.9548
D to Z ↓	0.0209	0.0220	0.9250	0.6912
D to Z ↑	0.0202	0.0214	1.2785	0.9570

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.052e-05	1.000e-20
X10_P0	2.142e-05	1.000e-20
X14_P0	2.615e-05	1.000e-20
X19_P0	3.088e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	6.368e-05	1.224e-04	1.240e-04	1.244e-04
B (output stable)	7.093e-05	1.337e-04	1.358e-04	1.358e-04
C (output stable)	2.103e-04	3.505e-04	3.522e-04	3.534e-04
D (output stable)	7.280e-05	1.071e-04	1.083e-04	1.084e-04
A to Z	2.341e-03	4.297e-03	5.553e-03	6.667e-03
B to Z	2.225e-03	4.017e-03	5.273e-03	6.388e-03
C to Z	1.947e-03	3.447e-03	4.617e-03	5.638e-03
D to Z	2.400e-03	4.241e-03	5.358e-03	6.293e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

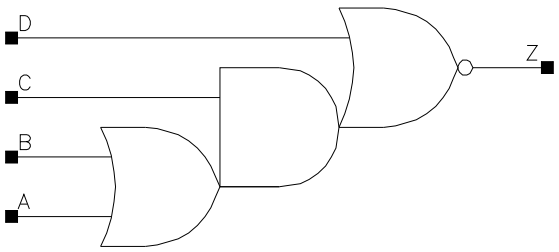
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X6_P0	0.800	1.496	1.1968
X9_P0	0.800	1.768	1.4144
X12_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X9_P0	X12_P0
A	0.0005	0.0010	0.0016	0.0020
B	0.0005	0.0009	0.0015	0.0020
C	0.0005	0.0010	0.0014	0.0019
D	0.0007	0.0010	0.0014	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0120	0.0109	4.6715	2.3945
A to Z ↑	0.0229	0.0226	10.9681	5.7992
B to Z ↓	0.0113	0.0108	4.5295	2.4102
B to Z ↑	0.0232	0.0222	10.9838	5.8138
C to Z ↓	0.0108	0.0101	4.3277	2.2540
C to Z ↑	0.0150	0.0140	7.5500	3.9128

D to Z ↓	0.0060	0.0046	2.8623	1.4602
D to Z ↑	0.0148	0.0127	8.0192	4.1779
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0110	0.0115	1.6410	1.2826
A to Z ↑	0.0208	0.0221	3.7317	2.8795
B to Z ↓	0.0104	0.0107	1.6589	1.2839
B to Z ↑	0.0211	0.0216	3.7400	2.8868
C to Z ↓	0.0104	0.0105	1.5590	1.2062
C to Z ↑	0.0134	0.0136	2.5431	1.9355
D to Z ↓	0.0048	0.0048	1.0154	0.7784
D to Z ↑	0.0118	0.0117	2.7051	2.0686

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	5.920e-06	1.000e-20
X6_P0	1.113e-05	1.000e-20
X9_P0	1.577e-05	1.000e-20
X12_P0	2.040e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	1.885e-05	4.584e-05	5.630e-05	9.461e-05
B (output stable)	2.225e-05	4.917e-05	6.974e-05	1.106e-04
C (output stable)	6.803e-05	1.504e-04	2.053e-04	2.837e-04
D (output stable)	1.594e-04	4.025e-04	5.604e-04	8.085e-04
A to Z	1.506e-03	2.855e-03	3.967e-03	5.501e-03
B to Z	1.337e-03	2.412e-03	3.483e-03	4.667e-03
C to Z	1.125e-03	2.055e-03	2.939e-03	3.995e-03
D to Z	8.631e-04	1.482e-03	2.081e-03	2.730e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

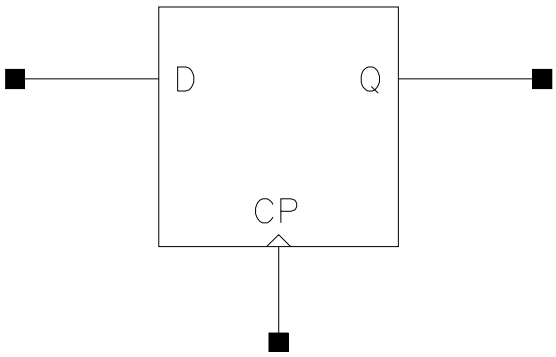
Pin Cycle (vdds)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	1.600	1.496	2.3936
X19_P0	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P0	X19_P0
CP	0.0008	0.0008
D	0.0006	0.0006

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	X19_P0	X10_P0	X19_P0
CP to Q ↓	0.0383	0.0513	1.3850	0.7458
CP to Q ↑	0.0446	0.0510	1.8928	0.9714

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P0	X19_P0
CP ↓	min_pulse_width to CP	0.0386	0.0386
CP ↑	min_pulse_width to CP	0.0329	0.0457
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0097	0.0097
D ↓	setup_rising to CP	0.0176	0.0176
D ↑	setup_rising to CP	0.0146	0.0146

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P0	2.690e-05	1.000e-20
X19_P0	3.455e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

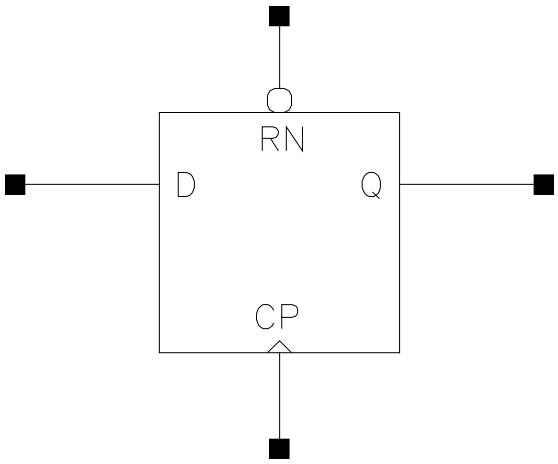
Pin Cycle	X10_P0	X19_P0
Clock 100Mhz Data 0Mhz	7.520e-03	7.528e-03
Clock 100Mhz Data 25Mhz	9.106e-03	1.098e-02
Clock 100Mhz Data 50Mhz	1.069e-02	1.443e-02
Clock = 0 Data 100Mhz	2.982e-03	2.982e-03
Clock = 1 Data 100Mhz	2.505e-05	2.515e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	1.600	1.768	2.8288
X19_P0	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P0	X19_P0
CP	0.0008	0.0008
D	0.0006	0.0006
RN	0.0008	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	X19_P0	X10_P0	X19_P0
CP to Q ↓	0.0417	0.0529	1.4081	0.7385
CP to Q ↑	0.0464	0.0525	1.8867	0.9646
RN to Q ↓	0.0427	0.0540	1.3787	0.7102

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P0	X19_P0
CP ↓	min_pulse_width to CP	0.0386	0.0386
CP ↑	min_pulse_width to CP	0.0363	0.0457
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0149	0.0176
D ↑	setup_rising to CP	0.0146	0.0146
RN ↓	min_pulse_width to RN	0.0518	0.0664
RN ↑	recovery_rising to CP	0.0081	0.0081
RN ↑	removal_rising to CP	-0.0033	-0.0033

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P0	3.289e-05	1.000e-20
X19_P0	4.450e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

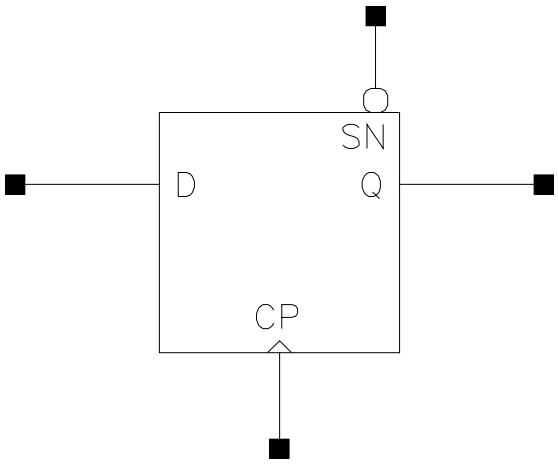
Pin Cycle	X10_P0	X19_P0
Clock 100Mhz Data 0Mhz	7.615e-03	7.615e-03
Clock 100Mhz Data 25Mhz	9.353e-03	1.119e-02
Clock 100Mhz Data 50Mhz	1.109e-02	1.477e-02
Clock = 0 Data 100Mhz	2.997e-03	2.997e-03
Clock = 1 Data 100Mhz	2.503e-05	2.516e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	1.600	1.768	2.8288
X19_P0	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P0	X19_P0
CP	0.0008	0.0008
D	0.0006	0.0006
SN	0.0010	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	X19_P0	X10_P0	X19_P0
CP to Q ↓	0.0393	0.0515	1.3944	0.7326
CP to Q ↑	0.0459	0.0525	1.8857	0.9656
SN to Q ↑	0.0291	0.0329	1.8518	0.9408

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P0	X19_P0
CP ↓	min_pulse_width to CP	0.0386	0.0386
CP ↑	min_pulse_width to CP	0.0329	0.0457
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0124	0.0124
D ↓	setup_rising to CP	0.0176	0.0176
D ↑	setup_rising to CP	0.0151	0.0151
SN ↓	min_pulse_width to SN	0.0327	0.0354
SN ↑	recovery_rising to CP	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0237	0.0237

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P0	3.057e-05	1.000e-20
X19_P0	3.809e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

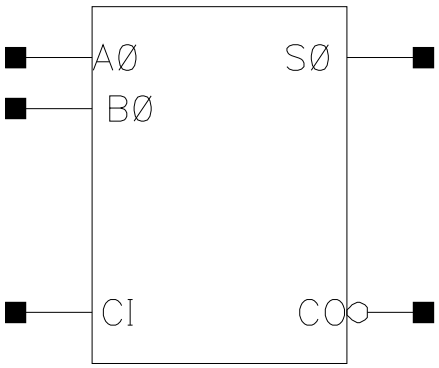
Pin Cycle	X10_P0	X19_P0
Clock 100Mhz Data 0Mhz	7.477e-03	7.481e-03
Clock 100Mhz Data 25Mhz	9.144e-03	1.105e-02
Clock 100Mhz Data 50Mhz	1.081e-02	1.462e-02
Clock = 0 Data 100Mhz	2.872e-03	2.873e-03
Clock = 1 Data 100Mhz	2.509e-05	2.519e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_P0	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_P0	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_P0	1.600	2.720	4.3520
C8T28SOIDV_LLS1_FA1X4_P0	1.600	2.040	3.2640
C8T28SOIDV_LLS1_FA1X9_P0	1.600	3.128	5.0048
C8T28SOIDV_LLS1_FA1X18_P0	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P0	C8T28SOIDV_LL_-FA1X9_P0	C8T28SOIDV_LL_-FA1X14_P0	C8T28SOIDV_LL_-FA1X19_P0
A0	0.0021	0.0022	0.0034	0.0037
B0	0.0017	0.0018	0.0032	0.0034
CI	0.0013	0.0013	0.0023	0.0025
	C8T28SOIDV_LLS1_-FA1X4_P0	C8T28SOIDV_LLS1_-FA1X9_P0	C8T28SOIDV_LLS1_-FA1X18_P0	
A0	0.0020	0.0027	0.0029	
B0	0.0019	0.0031	0.0035	
CI	0.0015	0.0022	0.0026	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P0	**C8T28SOIDV_LL_-FA1X9_P0**	**C8T28SOIDV_LL_-FA1X5_P0**	**C8T28SOIDV_LL_-FA1X9_P0**
A0 to CO ↓	0.0340	0.0365	2.8890	1.4791
A0 to CO ↑	0.0257	0.0276	3.7473	1.9168
A0 to S0 ↓	0.0367	0.0399	2.8464	1.4670
A0 to S0 ↑	0.0379	0.0407	3.7695	1.8877
B0 to CO ↓	0.0340	0.0367	2.8992	1.4842
B0 to CO ↑	0.0267	0.0285	3.7478	1.9187
B0 to S0 ↓	0.0372	0.0405	2.8481	1.4673
B0 to S0 ↑	0.0385	0.0415	3.7703	1.8878
CI to CO ↓	0.0326	0.0351	2.9006	1.4852
CI to CO ↑	0.0264	0.0283	3.7471	1.9165
CI to S0 ↓	0.0369	0.0404	2.8479	1.4671
CI to S0 ↑	0.0383	0.0413	3.7700	1.8871
	C8T28SOIDV_LL_-FA1X14_P0	**C8T28SOIDV_LL_-FA1X19_P0**	**C8T28SOIDV_LL_-FA1X14_P0**	**C8T28SOIDV_LL_-FA1X19_P0**
A0 to CO ↓	0.0348	0.0380	0.9687	0.7359
A0 to CO ↑	0.0264	0.0273	1.3230	0.9868
A0 to S0 ↓	0.0422	0.0426	0.9635	0.7154
A0 to S0 ↑	0.0432	0.0445	1.2748	0.9515
B0 to CO ↓	0.0342	0.0374	0.9710	0.7376
B0 to CO ↑	0.0267	0.0276	1.3222	0.9862
B0 to S0 ↓	0.0425	0.0429	0.9634	0.7154
B0 to S0 ↑	0.0435	0.0447	1.2759	0.9522
CI to CO ↓	0.0328	0.0359	0.9701	0.7367
CI to CO ↑	0.0263	0.0273	1.3226	0.9865
CI to S0 ↓	0.0420	0.0426	0.9633	0.7150
CI to S0 ↑	0.0429	0.0444	1.2750	0.9518
	C8T28SOIDV_-LLS1_FA1X4_P0	**C8T28SOIDV_-LLS1_FA1X9_P0**	**C8T28SOIDV_-LLS1_FA1X4_P0**	**C8T28SOIDV_-LLS1_FA1X9_P0**
A0 to CO ↓	0.0240	0.0216	5.3553	1.7864
A0 to CO ↑	0.0217	0.0199	3.8098	1.9194
A0 to S0 ↓	0.0496	0.0531	3.0394	1.1031
A0 to S0 ↑	0.0468	0.0455	3.9753	1.8768
B0 to CO ↓	0.0223	0.0223	5.3486	1.7880
B0 to CO ↑	0.0180	0.0187	3.7980	1.9179
B0 to S0 ↓	0.0498	0.0554	3.0372	1.1031
B0 to S0 ↑	0.0471	0.0478	3.9713	1.8768
CI to CO ↓	0.0228	0.0309	5.3498	1.7989
CI to CO ↑	0.0195	0.0179	3.8137	1.9341

CI to S0 ↓	0.0286	0.0337	3.0440	1.1056
CI to S0 ↑	0.0250	0.0252	3.9737	1.8765
	C8T28SOIDV_-LLS1_FA1X18_P0		**C8T28SOIDV_-LLS1_FA1X18_P0**	
A0 to CO ↓	0.0274		0.9470	
A0 to CO ↑	0.0206		0.9436	
A0 to S0 ↓	0.0564		0.5709	
A0 to S0 ↑	0.0462		0.9437	
B0 to CO ↓	0.0286		0.9479	
B0 to CO ↑	0.0195		0.9425	
B0 to S0 ↓	0.0576		0.5710	
B0 to S0 ↑	0.0475		0.9444	
CI to CO ↓	0.0382		0.9546	
CI to CO ↑	0.0215		0.9453	
CI to S0 ↓	0.0345		0.5713	
CI to S0 ↑	0.0233		0.9437	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P0	2.439e-05	1.000e-20
C8T28SOIDV_LL_FA1X9_P0	3.332e-05	1.000e-20
C8T28SOIDV_LL_FA1X14_P0	4.847e-05	1.000e-20
C8T28SOIDV_LL_FA1X19_P0	6.143e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P0	5.543e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P0	7.930e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P0	1.203e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P0	C8T28SOIDV_LL_-FA1X9_P0	C8T28SOIDV_LL_-FA1X14_P0	C8T28SOIDV_LL_-FA1X19_P0
A0 to CO	2.566e-03	3.648e-03	6.004e-03	7.349e-03
A0 to S0	2.634e-03	3.595e-03	6.158e-03	7.526e-03
B0 to CO	2.583e-03	3.689e-03	6.030e-03	7.405e-03
B0 to S0	2.609e-03	3.593e-03	6.120e-03	7.490e-03
CI to CO	2.584e-03	3.673e-03	6.071e-03	7.499e-03
CI to S0	2.599e-03	3.589e-03	6.101e-03	7.472e-03
	C8T28SOIDV_LLS1_-FA1X4_P0	C8T28SOIDV_LLS1_-FA1X9_P0	C8T28SOIDV_LLS1_-FA1X18_P0	
A0 to CO	4.058e-03	6.198e-03	9.834e-03	
A0 to S0	5.508e-03	8.042e-03	1.230e-02	
B0 to CO	4.291e-03	6.283e-03	9.885e-03	
B0 to S0	5.908e-03	8.228e-03	1.245e-02	
CI to CO	2.937e-03	5.131e-03	8.727e-03	
CI to S0	3.311e-03	5.711e-03	9.505e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P0	C8T28SOIDV_LL_-FA1X9_P0	C8T28SOIDV_LL_-FA1X14_P0	C8T28SOIDV_LL_-FA1X19_P0
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P0	C8T28SOIDV_LLS1_-FA1X9_P0	C8T28SOIDV_LLS1_-FA1X18_P0	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P0	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P0	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P0	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P0	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P0	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P0	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P0	C8T28SOI_LL_-HA1X9_P0	C8T28SOI_LLS1_-HA1X5_P0	C8T28SOIDV_LL_-HA1X14_P0
A0	0.0007	0.0010	0.0012	0.0014
B0	0.0006	0.0010	0.0011	0.0012
	C8T28SOIDV_LL_-HA1X19_P0	C8T28SOIDV_LLS1_-HA1X11_P0		
A0	0.0017	0.0017		
B0	0.0015	0.0017		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P0	**C8T28SOI_LL_-HA1X9_P0**	**C8T28SOI_LL_-HA1X5_P0**	**C8T28SOI_LL_-HA1X9_P0**
A0 to CO ↓	0.0271	0.0231	2.8635	1.4090
A0 to CO ↑	0.0251	0.0220	4.0099	1.9355
A0 to S0 ↓	0.0338	0.0310	2.7415	1.3946
A0 to S0 ↑	0.0326	0.0300	3.8903	1.9351
B0 to CO ↓	0.0264	0.0226	2.8648	1.4085
B0 to CO ↑	0.0270	0.0239	4.0119	1.9361
B0 to S0 ↓	0.0353	0.0320	2.7433	1.3943
B0 to S0 ↑	0.0320	0.0294	3.8908	1.9346
	C8T28SOI_LLS1_-HA1X5_P0	**C8T28SOIDV_LL_-HA1X14_P0**	**C8T28SOI_LLS1_-HA1X5_P0**	**C8T28SOIDV_LL_-HA1X14_P0**
A0 to CO ↓	0.0218	0.0239	2.8095	0.9584
A0 to CO ↑	0.0199	0.0216	3.9645	1.3013
A0 to S0 ↓	0.0296	0.0343	2.8021	0.9702
A0 to S0 ↑	0.0335	0.0330	3.9904	1.2816
B0 to CO ↓	0.0208	0.0222	2.8100	0.9543
B0 to CO ↑	0.0214	0.0223	3.9653	1.3025
B0 to S0 ↓	0.0312	0.0342	2.8029	0.9700
B0 to S0 ↑	0.0329	0.0314	3.9882	1.2821
	C8T28SOIDV_LL_-HA1X19_P0	**C8T28SOIDV_-LLS1_HA1X11_P0**	**C8T28SOIDV_LL_-HA1X19_P0**	**C8T28SOIDV_-LLS1_HA1X11_P0**
A0 to CO ↓	0.0223	0.0211	0.7054	1.0112
A0 to CO ↑	0.0209	0.0215	0.9870	1.9013
A0 to S0 ↓	0.0315	0.0267	0.7023	1.0250
A0 to S0 ↑	0.0306	0.0284	0.9618	1.9182
B0 to CO ↓	0.0208	0.0200	0.7041	1.0104
B0 to CO ↑	0.0219	0.0231	0.9867	1.9010
B0 to S0 ↓	0.0320	0.0275	0.7020	1.0243
B0 to S0 ↑	0.0293	0.0284	0.9619	1.9179

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_HA1X5_P0	1.354e-05	1.000e-20
C8T28SOI_LL_HA1X9_P0	3.378e-05	1.000e-20
C8T28SOI_LLS1_HA1X5_P0	1.681e-05	1.000e-20
C8T28SOIDV_LL_HA1X14_P0	4.883e-05	1.000e-20
C8T28SOIDV_LL_HA1X19_P0	6.856e-05	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P0	4.343e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

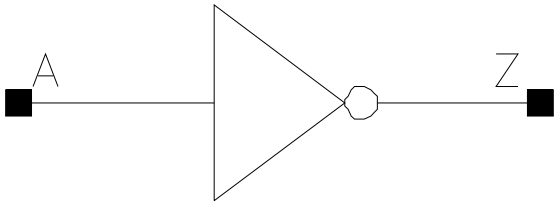
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P0	C8T28SOI_LL_-HA1X9_P0	C8T28SOI_LLS1_-HA1X5_P0	C8T28SOIDV_LL_-HA1X14_P0
A0 to CO	1.948e-03	3.154e-03	2.348e-03	5.082e-03
A0 to S0	1.779e-03	3.086e-03	2.095e-03	5.187e-03
B0 to CO	1.973e-03	3.274e-03	2.383e-03	5.073e-03
B0 to S0	1.765e-03	3.047e-03	2.059e-03	5.089e-03
	C8T28SOIDV_LL_-HA1X19_P0	C8T28SOIDV_LLS1_-HA1X11_P0		
A0 to CO	6.152e-03	4.453e-03		
A0 to S0	6.264e-03	4.101e-03		

B0 to CO	6.162e-03	4.156e-03		
B0 to S0	6.184e-03	4.192e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P0	C8T28SOI_LL_-HA1X9_P0	C8T28SOI_LLS1_-HA1X5_P0	C8T28SOIDV_LL_-HA1X14_P0
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P0	C8T28SOIDV_LLS1_-HA1X11_P0		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P0	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P0	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P0	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P0	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P0	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P0	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P0	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P0	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P0	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P0	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P0	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P0	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P0	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P0	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P0	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P0	C8T28SOI_LL_IVX3_-P0	C8T28SOI_LL_IVX5_-P0	C8T28SOI_LL_-IVX10_P0

A	0.0004	0.0004	0.0005	0.0010
	C8T28SOI_LL_-IVX14_P0	C8T28SOI_LL_-IVX19_P0	C8T28SOI_LL_-IVX29_P0	C8T28SOI_LL_-IVX34_P0
A	0.0015	0.0020	0.0029	0.0034
	C8T28SOI_LL_-IVX38_P0	C8T28SOIDV_LL_-IVX11_P0	C8T28SOIDV_LL_-IVX23_P0	C8T28SOIDV_LL_-IVX34_P0
A	0.0039	0.0011	0.0021	0.0031
	C8T28SOIDV_LL_-IVX46_P0	C8T28SOIDV_LL_-IVX68_P0	C8T28SOIDV_LL_-IVX91_P0	
A	0.0041	0.0063	0.0088	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P0	**C8T28SOI_LL_-IVX3_P0**	**C8T28SOI_LL_-IVX2_P0**	**C8T28SOI_LL_-IVX3_P0**
A to Z ↓	0.0056	0.0052	5.3822	4.1901
A to Z ↑	0.0107	0.0097	7.6869	5.8556
	C8T28SOI_LL_-IVX5_P0	**C8T28SOI_LL_-IVX10_P0**	**C8T28SOI_LL_-IVX5_P0**	**C8T28SOI_LL_-IVX10_P0**
A to Z ↓	0.0048	0.0036	2.9111	1.4014
A to Z ↑	0.0087	0.0072	4.0945	1.9478
	C8T28SOI_LL_-IVX14_P0	**C8T28SOI_LL_-IVX19_P0**	**C8T28SOI_LL_-IVX14_P0**	**C8T28SOI_LL_-IVX19_P0**
A to Z ↓	0.0039	0.0042	0.9753	0.7439
A to Z ↑	0.0071	0.0074	1.3091	1.0075
	C8T28SOI_LL_-IVX29_P0	**C8T28SOI_LL_-IVX34_P0**	**C8T28SOI_LL_-IVX29_P0**	**C8T28SOI_LL_-IVX34_P0**
A to Z ↓	0.0042	0.0039	0.4974	0.4238
A to Z ↑	0.0071	0.0068	0.6667	0.5690
	C8T28SOI_LL_-IVX38_P0	**C8T28SOIDV_LL_-IVX11_P0**	**C8T28SOI_LL_-IVX38_P0**	**C8T28SOIDV_LL_-IVX11_P0**
A to Z ↓	0.0041	0.0035	0.3761	1.1161
A to Z ↑	0.0070	0.0085	0.5050	1.9699
	C8T28SOIDV_LL_-IVX23_P0	**C8T28SOIDV_LL_-IVX34_P0**	**C8T28SOIDV_LL_-IVX23_P0**	**C8T28SOIDV_LL_-IVX34_P0**
A to Z ↓	0.0028	0.0032	0.5455	0.3740
A to Z ↑	0.0075	0.0077	0.9605	0.6448
	C8T28SOIDV_LL_-IVX46_P0	**C8T28SOIDV_LL_-IVX68_P0**	**C8T28SOIDV_LL_-IVX46_P0**	**C8T28SOIDV_LL_-IVX68_P0**
A to Z ↓	0.0032	0.0032	0.2815	0.1920
A to Z ↑	0.0075	0.0073	0.4841	0.3255
	C8T28SOIDV_LL_-IVX91_P0		**C8T28SOIDV_LL_-IVX91_P0**	
A to Z ↓	0.0037		0.1493	
A to Z ↑	0.0077		0.2481	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_IVX2_P0	1.637e-06	1.000e-20
C8T28SOI_LL_IVX3_P0	2.581e-06	1.000e-20
C8T28SOI_LL_IVX5_P0	4.130e-06	1.000e-20
C8T28SOI_LL_IVX10_P0	9.085e-06	1.000e-20

C8T28SOI_LL_IVX14_P0	1.292e-05	1.000e-20
C8T28SOI_LL_IVX19_P0	1.673e-05	1.000e-20
C8T28SOI_LL_IVX29_P0	2.435e-05	1.000e-20
C8T28SOI_LL_IVX34_P0	2.817e-05	1.000e-20
C8T28SOI_LL_IVX38_P0	3.198e-05	1.000e-20
C8T28SOIDV_LL_IVX11_P0	1.029e-05	1.000e-20
C8T28SOIDV_LL_IVX23_P0	2.093e-05	1.000e-20
C8T28SOIDV_LL_IVX34_P0	3.015e-05	1.000e-20
C8T28SOIDV_LL_IVX46_P0	3.926e-05	1.000e-20
C8T28SOIDV_LL_IVX68_P0	5.748e-05	1.000e-20
C8T28SOIDV_LL_IVX91_P0	7.571e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P0	C8T28SOI_LL_IVX3_-P0	C8T28SOI_LL_IVX5_-P0	C8T28SOI_LL_-IVX10_P0
A to Z	4.079e-04	5.066e-04	6.530e-04	1.265e-03
	C8T28SOI_LL_-IVX14_P0	C8T28SOI_LL_-IVX19_P0	C8T28SOI_LL_-IVX29_P0	C8T28SOI_LL_-IVX34_P0
A to Z	1.907e-03	2.564e-03	3.739e-03	4.224e-03
	C8T28SOI_LL_-IVX38_P0	C8T28SOIDV_LL_-IVX11_P0	C8T28SOIDV_LL_-IVX23_P0	C8T28SOIDV_LL_-IVX34_P0
A to Z	4.873e-03	1.466e-03	2.772e-03	4.186e-03
	C8T28SOIDV_LL_-IVX46_P0	C8T28SOIDV_LL_-IVX68_P0	C8T28SOIDV_LL_-IVX91_P0	
A to Z	5.387e-03	7.949e-03	1.068e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

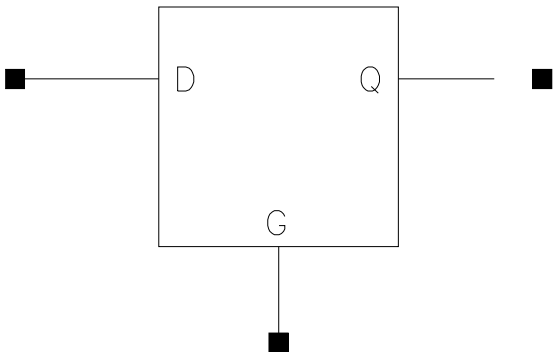
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P0	C8T28SOI_LL_IVX3_-P0	C8T28SOI_LL_IVX5_-P0	C8T28SOI_LL_-IVX10_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P0	C8T28SOI_LL_-IVX19_P0	C8T28SOI_LL_-IVX29_P0	C8T28SOI_LL_-IVX34_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P0	C8T28SOIDV_LL_-IVX11_P0	C8T28SOIDV_LL_-IVX23_P0	C8T28SOIDV_LL_-IVX34_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P0	C8T28SOIDV_LL_-IVX68_P0	C8T28SOIDV_LL_-IVX91_P0	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.360	1.0880
X9_P0	1.600	0.952	1.5232
X19_P0	1.600	1.224	1.9584
X28_P0	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0	X28_P0
D	0.0004	0.0006	0.0009	0.0015
G	0.0008	0.0008	0.0016	0.0016

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D to Q ↓	0.0377	0.0368	2.8951	1.4775
D to Q ↑	0.0221	0.0260	3.8929	1.8905
G to Q ↓	0.0393	0.0381	2.8875	1.4749

G to Q ↑	0.0216	0.0245	3.8949	1.8920
	X19_P0	**X28_P0**	**X19_P0**	**X28_P0**
D to Q ↓	0.0297	0.0312	0.7076	0.4774
D to Q ↑	0.0227	0.0230	0.9524	0.6411
G to Q ↓	0.0330	0.0298	0.7057	0.4757
G to Q ↑	0.0208	0.0210	0.9545	0.6407

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P0	X9_P0	X19_P0	X28_P0
D ↓	hold_falling to G	-0.0023	-0.0023	0.0080	0.0058
D ↑	hold_falling to G	0.0089	0.0068	0.0068	0.0068
D ↓	setup_falling to G	0.0369	0.0370	0.0273	0.0263
D ↑	setup_falling to G	0.0231	0.0279	0.0257	0.0257
G ↑	min_pulse_width to G	0.0330	0.0318	0.0271	0.0271

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	9.296e-06	1.000e-20
X9_P0	1.712e-05	1.000e-20
X19_P0	2.934e-05	1.000e-20
X28_P0	4.086e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	1.310e-05	3.348e-05	4.003e-05	1.051e-04
G (output stable)	8.342e-04	1.004e-03	1.645e-03	1.584e-03
D to Q	2.992e-03	4.744e-03	7.086e-03	1.028e-02
G to Q	2.850e-03	4.533e-03	6.637e-03	9.076e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

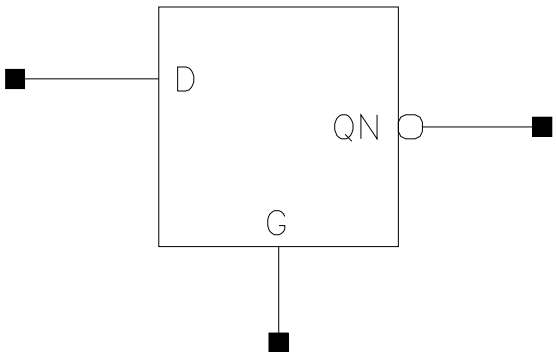
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P0
D	0.0004
G	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P0	X10_P0
D to QN ↓	0.0330	1.3490
D to QN ↑	0.0446	1.8909
G to QN ↓	0.0322	1.3491
G to QN ↑	0.0459	1.8888

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P0
D ↓	hold_falling to G	-0.0071
D ↑	hold_falling to G	0.0009
D ↓	setup_falling to G	0.0317
D ↑	setup_falling to G	0.0231
G ↑	min_pulse_width to G	0.0283

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P0	1.540e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X10_P0
D (output stable)	1.279e-05
G (output stable)	9.207e-04
D to QN	3.893e-03
G to QN	3.760e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

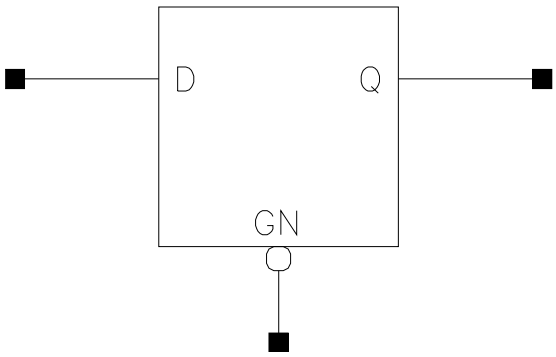
Pin Cycle (vdds)	X10_P0
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.360	1.0880
X9_P0	1.600	0.952	1.5232
X19_P0	1.600	1.224	1.9584
X28_P0	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0	X28_P0
D	0.0004	0.0006	0.0009	0.0013
GN	0.0008	0.0008	0.0012	0.0016

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D to Q ↓	0.0381	0.0363	2.9006	1.4823
D to Q ↑	0.0223	0.0259	3.8907	1.8926
GN to Q ↓	0.0346	0.0349	2.9046	1.4838

GN to Q ↑	0.0380	0.0363	3.8784	1.8834
	X19_P0	**X28_P0**	**X19_P0**	**X28_P0**
D to Q ↓	0.0303	0.0300	0.7035	0.4759
D to Q ↑	0.0238	0.0234	0.9466	0.6344
GN to Q ↓	0.0270	0.0259	0.7051	0.4764
GN to Q ↑	0.0327	0.0325	0.9438	0.6330

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P0	X9_P0	X19_P0	X28_P0
D ↓	hold_rising to GN	-0.0052	-0.0030	0.0019	0.0019
D ↑	hold_rising to GN	0.0106	0.0106	0.0107	0.0106
D ↓	setup_rising to GN	0.0422	0.0401	0.0352	0.0331
D ↑	setup_rising to GN	0.0190	0.0245	0.0217	0.0190
GN ↓	min_pulse_width to GN	0.0461	0.0433	0.0393	0.0349

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	9.343e-06	1.000e-20
X9_P0	1.768e-05	1.000e-20
X19_P0	3.328e-05	1.000e-20
X28_P0	4.418e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	1.289e-05	2.078e-05	4.014e-05	9.068e-05
GN (output stable)	8.331e-04	9.857e-04	1.439e-03	1.541e-03
D to Q	2.994e-03	4.765e-03	7.343e-03	1.009e-02
GN to Q	4.489e-03	6.391e-03	9.389e-03	1.195e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

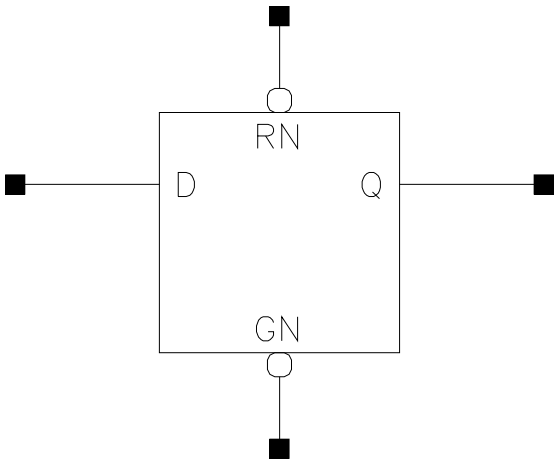
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.632	1.3056
X9_P0	1.600	1.224	1.9584
X19_P0	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0
D	0.0004	0.0005	0.0011
GN	0.0009	0.0010	0.0013
RN	0.0004	0.0005	0.0005

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D to Q ↓	0.0395	0.0378	2.8498	1.4336

D to Q ↑	0.0363	0.0397	4.0196	1.9548
GN to Q ↓	0.0366	0.0352	2.8510	1.4346
GN to Q ↑	0.0490	0.0462	4.0193	1.9573
RN to Q ↓	0.0326	0.0405	2.7544	1.4314
RN to Q ↑	0.0385	0.0419	4.0185	1.9558
	X19_P0		**X19_P0**	
D to Q ↓	0.0313		0.7089	
D to Q ↑	0.0421		0.9871	
GN to Q ↓	0.0284		0.7095	
GN to Q ↑	0.0442		0.9893	
RN to Q ↓	0.0513		0.7521	
RN to Q ↑	0.0464		0.9883	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P0	X9_P0	X19_P0
D ↓	hold_rising to GN	-0.0052	-0.0025	0.0019
D ↑	hold_rising to GN	0.0010	-0.0045	-0.0093
D ↓	setup_rising to GN	0.0445	0.0397	0.0353
D ↑	setup_rising to GN	0.0362	0.0416	0.0459
GN ↓	min_pulse_width to GN	0.0511	0.0481	0.0448
RN ↓	min_pulse_width to RN	0.0398	0.0469	0.0588
RN ↑	recovery_rising to GN	0.0389	0.0443	0.0514
RN ↑	removal_rising to GN	-0.0223	-0.0266	-0.0310

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.095e-05	1.000e-20
X9_P0	1.920e-05	1.000e-20
X19_P0	3.438e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0
D (output stable)	7.089e-05	6.933e-05	9.185e-05
GN (output stable)	9.341e-04	9.909e-04	1.254e-03
RN (output stable)	2.884e-05	3.798e-05	4.706e-05
D to Q	3.769e-03	5.368e-03	8.301e-03
GN to Q	5.373e-03	6.952e-03	1.017e-02
RN to Q	2.838e-03	4.093e-03	6.717e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

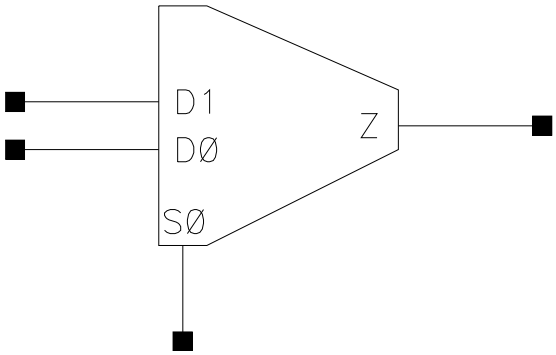
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.360	1.0880
X9_P0	0.800	1.496	1.1968
X14_P0	0.800	2.176	1.7408
X19_P0	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P0	X9_P0	X14_P0	X19_P0
D0	0.0005	0.0007	0.0009	0.0011
D1	0.0005	0.0006	0.0009	0.0011
S0	0.0009	0.0009	0.0011	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D0 to Z ↓	0.0293	0.0276	2.8891	1.4609
D0 to Z ↑	0.0233	0.0228	3.9832	2.0262
D1 to Z ↓	0.0295	0.0267	2.8859	1.4578
D1 to Z ↑	0.0228	0.0215	3.9860	2.0251
S0 to Z ↓	0.0278	0.0242	2.8764	1.4517
S0 to Z ↑	0.0262	0.0239	3.9867	2.0237

	X14_P0	X19_P0	X14_P0	X19_P0
D0 to Z ↓	0.0297	0.0263	1.0085	0.7286
D0 to Z ↑	0.0239	0.0221	1.3708	0.9907
D1 to Z ↓	0.0301	0.0270	1.0085	0.7290
D1 to Z ↑	0.0229	0.0215	1.3699	0.9916
S0 to Z ↓	0.0289	0.0267	1.0038	0.7262
S0 to Z ↑	0.0279	0.0255	1.3708	0.9902

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.146e-05	1.000e-20
X9_P0	2.246e-05	1.000e-20
X14_P0	2.879e-05	1.000e-20
X19_P0	4.416e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X9_P0	X14_P0	X19_P0
D0 (output stable)	6.263e-04	1.125e-03	1.310e-03	1.684e-03
D1 (output stable)	5.985e-04	9.661e-04	1.359e-03	1.770e-03
S0 (output stable)	8.695e-04	7.872e-04	1.231e-03	1.480e-03
D0 to Z	2.231e-03	3.549e-03	5.620e-03	6.884e-03
D1 to Z	2.174e-03	3.309e-03	5.464e-03	6.829e-03
S0 to Z	2.736e-03	3.469e-03	6.138e-03	7.415e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

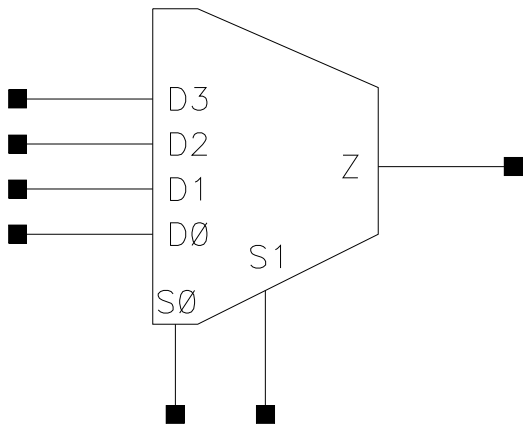
Pin Cycle (vdds)	X5_P0	X9_P0	X14_P0	X19_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.600	1.496	2.3936
X9_P0	1.600	1.768	2.8288
X13_P0	1.600	2.312	3.6992
X18_P0	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P0	X9_P0	X13_P0	X18_P0
D0	0.0004	0.0006	0.0009	0.0009
D1	0.0004	0.0005	0.0009	0.0009
D2	0.0004	0.0006	0.0009	0.0009
D3	0.0004	0.0005	0.0009	0.0009
S0	0.0012	0.0016	0.0020	0.0021
S1	0.0007	0.0008	0.0012	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X9_P0	X4_P0	X9_P0
D0 to Z ↓	0.0616	0.0513	3.1027	1.5252
D0 to Z ↑	0.0389	0.0354	4.0877	2.0247
D1 to Z ↓	0.0607	0.0510	3.0987	1.5263
D1 to Z ↑	0.0388	0.0351	4.0832	2.0233
D2 to Z ↓	0.0561	0.0517	3.0558	1.5287
D2 to Z ↑	0.0375	0.0351	4.0568	2.0208
D3 to Z ↓	0.0567	0.0509	3.0631	1.5283
D3 to Z ↑	0.0381	0.0351	4.0599	2.0216
S0 to Z ↓	0.0631	0.0561	3.0800	1.5249
S0 to Z ↑	0.0455	0.0433	4.0824	2.0255
S1 to Z ↓	0.0409	0.0385	3.0755	1.5251
S1 to Z ↑	0.0353	0.0340	4.0715	2.0211
	X13_P0	X18_P0	X13_P0	X18_P0
D0 to Z ↓	0.0508	0.0551	1.0741	0.8030
D0 to Z ↑	0.0321	0.0346	1.3566	1.0255
D1 to Z ↓	0.0512	0.0555	1.0751	0.8037
D1 to Z ↑	0.0330	0.0355	1.3573	1.0272
D2 to Z ↓	0.0462	0.0499	1.0577	0.7896
D2 to Z ↑	0.0321	0.0346	1.3531	1.0235
D3 to Z ↓	0.0459	0.0496	1.0575	0.7894
D3 to Z ↑	0.0323	0.0348	1.3527	1.0237
S0 to Z ↓	0.0535	0.0574	1.0654	0.7962
S0 to Z ↑	0.0397	0.0422	1.3555	1.0258
S1 to Z ↓	0.0376	0.0416	1.0654	0.7960
S1 to Z ↑	0.0311	0.0336	1.3545	1.0246

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	1.091e-05	1.000e-20
X9_P0	1.897e-05	1.000e-20
X13_P0	3.286e-05	1.000e-20
X18_P0	3.718e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X9_P0	X13_P0	X18_P0
D0 (output stable)	4.742e-05	5.584e-05	1.195e-04	1.189e-04
D1 (output stable)	6.118e-05	7.313e-05	1.061e-04	1.058e-04
D2 (output stable)	5.923e-05	7.431e-05	1.127e-04	1.125e-04
D3 (output stable)	4.715e-05	7.195e-05	1.022e-04	1.022e-04
S0 (output stable)	1.089e-03	1.300e-03	2.110e-03	2.111e-03
S1 (output stable)	1.172e-03	1.349e-03	2.172e-03	2.172e-03
D0 to Z	2.837e-03	4.199e-03	6.752e-03	8.377e-03
D1 to Z	2.802e-03	4.183e-03	6.829e-03	8.461e-03
D2 to Z	2.655e-03	4.176e-03	6.435e-03	7.970e-03
D3 to Z	2.684e-03	4.176e-03	6.454e-03	7.982e-03
S0 to Z	3.982e-03	5.662e-03	8.982e-03	1.058e-02
S1 to Z	3.095e-03	4.520e-03	7.172e-03	8.735e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

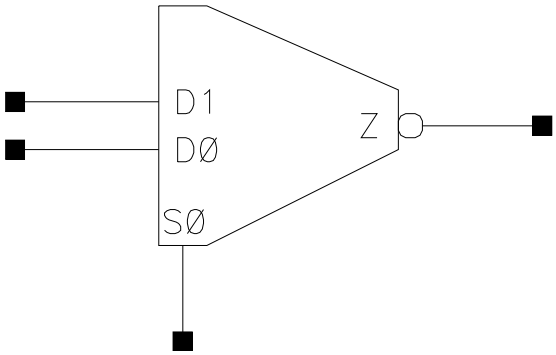
Pin Cycle (vdds)	X4_P0	X9_P0	X13_P0	X18_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P0	0.800	0.952	0.7616
X2_P0	0.800	0.952	0.7616
X6_P0	0.800	1.904	1.5232
X9_P0	0.800	2.448	1.9584
X12_P0	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P0	X2_P0	X6_P0	X9_P0
D0	0.0003	0.0005	0.0010	0.0015
D1	0.0003	0.0005	0.0010	0.0015
S0	0.0009	0.0012	0.0017	0.0024
	X12_P0			
D0	0.0020			
D1	0.0020			
S0	0.0027			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P0	X2_P0	X1_P0	X2_P0
D0 to Z ↓	0.0104	0.0096	7.9893	5.4428

D0 to Z ↑	0.0201	0.0158	16.6329	9.1441
D1 to Z ↓	0.0100	0.0093	7.8974	5.3151
D1 to Z ↑	0.0204	0.0161	16.6609	9.3147
S0 to Z ↓	0.0183	0.0129	7.8919	5.3609
S0 to Z ↑	0.0208	0.0139	16.5550	9.1876
	X6_P0	**X9_P0**	**X6_P0**	**X9_P0**
D0 to Z ↓	0.0110	0.0101	2.4593	1.6562
D0 to Z ↑	0.0165	0.0156	3.8243	2.6745
D1 to Z ↓	0.0106	0.0103	2.4106	1.6643
D1 to Z ↑	0.0174	0.0160	3.9564	2.6094
S0 to Z ↓	0.0152	0.0129	2.4284	1.6565
S0 to Z ↑	0.0160	0.0141	3.8775	2.6364
	X12_P0		**X12_P0**	
D0 to Z ↓	0.0106		1.2689	
D0 to Z ↑	0.0156		2.0185	
D1 to Z ↓	0.0102		1.2627	
D1 to Z ↑	0.0158		1.9690	
S0 to Z ↓	0.0140		1.2627	
S0 to Z ↑	0.0149		1.9896	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X1_P0	3.286e-06	1.000e-20
X2_P0	8.483e-06	1.000e-20
X6_P0	1.724e-05	1.000e-20
X9_P0	2.680e-05	1.000e-20
X12_P0	3.216e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X1_P0	X2_P0	X6_P0	X9_P0
D0 (output stable)	1.282e-05	2.749e-05	8.331e-05	1.207e-04
D1 (output stable)	1.229e-05	2.951e-05	8.765e-05	1.288e-04
S0 (output stable)	8.633e-04	1.039e-03	1.762e-03	2.741e-03
D0 to Z	7.137e-04	9.298e-04	2.429e-03	3.304e-03
D1 to Z	7.125e-04	9.185e-04	2.457e-03	3.368e-03
S0 to Z	1.465e-03	1.652e-03	3.385e-03	4.856e-03
	X12_P0			
D0 (output stable)	1.581e-04			
D1 (output stable)	1.614e-04			
S0 (output stable)	3.143e-03			
D0 to Z	4.459e-03			
D1 to Z	4.437e-03			
S0 to Z	6.026e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X1_P0	X2_P0	X6_P0	X9_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

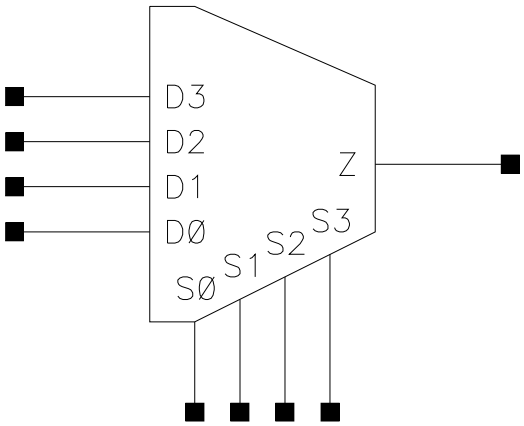
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P0			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.600	0.952	1.5232
X15_P0	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P0	X15_P0
D0	0.0005	0.0013
D1	0.0006	0.0011
D2	0.0005	0.0013
D3	0.0005	0.0011
S0	0.0005	0.0012
S1	0.0005	0.0014
S2	0.0005	0.0012
S3	0.0006	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X15_P0	X4_P0	X15_P0
D0 to Z ↓	0.0326	0.0346	4.6289	1.2239
D0 to Z ↑	0.0270	0.0261	3.7339	0.9479
D1 to Z ↓	0.0302	0.0315	4.6289	1.2230
D1 to Z ↑	0.0235	0.0228	3.7141	0.9425
D2 to Z ↓	0.0318	0.0338	4.6353	1.2252
D2 to Z ↑	0.0265	0.0251	3.7505	0.9528
D3 to Z ↓	0.0291	0.0309	4.6310	1.2232
D3 to Z ↑	0.0229	0.0220	3.7314	0.9468
S0 to Z ↓	0.0311	0.0317	4.6271	1.2227
S0 to Z ↑	0.0290	0.0267	3.7328	0.9462
S1 to Z ↓	0.0284	0.0291	4.6268	1.2221
S1 to Z ↑	0.0250	0.0234	3.7146	0.9421
S2 to Z ↓	0.0308	0.0311	4.6346	1.2236
S2 to Z ↑	0.0284	0.0259	3.7478	0.9521
S3 to Z ↓	0.0284	0.0285	4.6311	1.2221
S3 to Z ↑	0.0248	0.0226	3.7314	0.9475

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	1.547e-05	1.000e-20
X15_P0	4.555e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X15_P0
D0 (output stable)	3.856e-04	1.077e-03
D1 (output stable)	3.275e-04	8.975e-04
D2 (output stable)	3.890e-04	1.091e-03
D3 (output stable)	3.338e-04	9.172e-04
S0 (output stable)	3.710e-04	1.065e-03
S1 (output stable)	3.184e-04	9.135e-04
S2 (output stable)	3.836e-04	1.087e-03
S3 (output stable)	3.288e-04	9.392e-04
D0 to Z	2.895e-03	8.266e-03
D1 to Z	2.499e-03	7.176e-03
D2 to Z	2.675e-03	7.536e-03
D3 to Z	2.293e-03	6.483e-03
S0 to Z	2.799e-03	7.771e-03
S1 to Z	2.417e-03	6.762e-03
S2 to Z	2.605e-03	7.085e-03
S3 to Z	2.232e-03	6.051e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

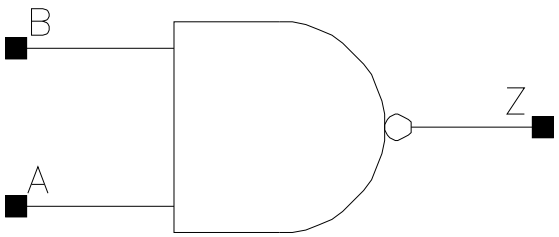
Pin Cycle (vdds)	X4_P0	X15_P0
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P0	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P0	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P0	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P0	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P0	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P0	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P0	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P0	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P0	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P0	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P0	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P0	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P0	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P0	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P0	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P0	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P0	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P0	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P0	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P0	C8T28SOI_LL_-NAND2X4_P0	C8T28SOI_LL_-NAND2X8_P0	C8T28SOI_LL_-NAND2X12_P0
A	0.0004	0.0005	0.0010	0.0015
B	0.0004	0.0005	0.0009	0.0014
	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X24_P0	C8T28SOI_-LLBR0P8_-NAND2X4_P0
A	0.0020	0.0025	0.0006	0.0006
B	0.0019	0.0023	0.0006	0.0005
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	C8T28SOI_-LLBR0P8_-NAND2X12_P0	C8T28SOI_-LLBR0P8_-NAND2X16_P0	C8T28SOI_LLS_-NAND2X8_P0
A	0.0010	0.0015	0.0020	0.0010
B	0.0009	0.0014	0.0018	0.0009
	C8T28SOI_LLS_-NAND2X15_P0	C8T28SOI_LLS_-NAND2X23_P0	C8T28SOI_LLS_-NAND2X31_P0	C8T28SOIDV_LL_-NAND2X9_P0
A	0.0021	0.0031	0.0041	0.0010
B	0.0019	0.0028	0.0038	0.0011
	C8T28SOIDV_LL_-NAND2X18_P0	C8T28SOIDV_LL_-NAND2X27_P0	C8T28SOIDV_LL_-NAND2X36_P0	
A	0.0021	0.0031	0.0042	
B	0.0020	0.0030	0.0039	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-NAND2X2_P0	**C8T28SOI_LL_-NAND2X4_P0**	**C8T28SOI_LL_-NAND2X2_P0**	**C8T28SOI_LL_-NAND2X4_P0**
A to Z ↓	0.0080	0.0069	8.5314	4.7009
A to Z ↑	0.0122	0.0102	7.6381	4.0881
B to Z ↓	0.0092	0.0077	8.6124	4.7484
B to Z ↑	0.0113	0.0091	7.6785	4.1434
	C8T28SOI_LL_-NAND2X8_P0	**C8T28SOI_LL_-NAND2X12_P0**	**C8T28SOI_LL_-NAND2X8_P0**	**C8T28SOI_LL_-NAND2X12_P0**
A to Z ↓	0.0076	0.0073	2.3999	1.6452
A to Z ↑	0.0103	0.0100	1.9492	1.3329
B to Z ↓	0.0072	0.0076	2.4248	1.6636
B to Z ↑	0.0079	0.0082	1.9644	1.3519

	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0
A to Z ↓	0.0075	0.0074	1.2488	1.0090
A to Z ↑	0.0100	0.0100	1.0046	0.8147
B to Z ↓	0.0073	0.0077	1.2634	1.0212
B to Z ↑	0.0078	0.0081	1.0179	0.8264
	C8T28SOI_LL_-NAND2X24_P0	**C8T28SOI_-LLBR0P8_-NAND2X4_P0**	**C8T28SOI_LL_-NAND2X24_P0**	**C8T28SOI_-LLBR0P8_-NAND2X4_P0**
A to Z ↓	0.0274	0.0053	0.5662	3.3430
A to Z ↑	0.0284	0.0133	0.7878	5.1532
B to Z ↓	0.0285	0.0055	0.5661	3.3977
B to Z ↑	0.0273	0.0114	0.7876	5.1732
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	**C8T28SOI_-LLBR0P8_-NAND2X12_P0**	**C8T28SOI_-LLBR0P8_-NAND2X8_P0**	**C8T28SOI_-LLBR0P8_-NAND2X12_P0**
A to Z ↓	0.0059	0.0058	1.8540	1.2683
A to Z ↑	0.0132	0.0132	2.5978	1.7614
B to Z ↓	0.0048	0.0054	1.8867	1.2917
B to Z ↑	0.0099	0.0104	2.6186	1.7738
	C8T28SOI_-LLBR0P8_-NAND2X16_P0	**C8T28SOI_LLS_-NAND2X8_P0**	**C8T28SOI_-LLBR0P8_-NAND2X16_P0**	**C8T28SOI_LLS_-NAND2X8_P0**
A to Z ↓	0.0056	0.0076	0.9706	2.3945
A to Z ↑	0.0128	0.0104	1.3176	1.9748
B to Z ↓	0.0047	0.0072	0.9880	2.4196
B to Z ↑	0.0095	0.0080	1.3327	2.0061
	C8T28SOI_LLS_-NAND2X15_P0	**C8T28SOI_LLS_-NAND2X23_P0**	**C8T28SOI_LLS_-NAND2X15_P0**	**C8T28SOI_LLS_-NAND2X23_P0**
A to Z ↓	0.0076	0.0076	1.2460	0.8415
A to Z ↑	0.0100	0.0099	0.9871	0.6586
B to Z ↓	0.0074	0.0076	1.2605	0.8513
B to Z ↑	0.0078	0.0078	0.9953	0.6645
	C8T28SOI_LLS_-NAND2X31_P0	**C8T28SOIDV_LL_-NAND2X9_P0**	**C8T28SOI_LLS_-NAND2X31_P0**	**C8T28SOIDV_LL_-NAND2X9_P0**
A to Z ↓	0.0076	0.0064	0.6375	1.8359
A to Z ↑	0.0099	0.0107	0.4962	1.8967
B to Z ↓	0.0077	0.0067	0.6449	1.8590
B to Z ↑	0.0079	0.0093	0.5004	1.9337
	C8T28SOIDV_LL_-NAND2X18_P0	**C8T28SOIDV_LL_-NAND2X27_P0**	**C8T28SOIDV_LL_-NAND2X18_P0**	**C8T28SOIDV_LL_-NAND2X27_P0**
A to Z ↓	0.0068	0.0069	0.9402	0.6412
A to Z ↑	0.0110	0.0110	0.9547	0.6451
B to Z ↓	0.0062	0.0069	0.9517	0.6492
B to Z ↑	0.0085	0.0090	0.9619	0.6496
	C8T28SOIDV_LL_-NAND2X36_P0		**C8T28SOIDV_LL_-NAND2X36_P0**	
A to Z ↓	0.0069		0.4833	
A to Z ↑	0.0109		0.4831	
B to Z ↓	0.0064		0.4895	
B to Z ↑	0.0084		0.4870	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P0	1.575e-06	1.000e-20
C8T28SOI_LL_NAND2X4_P0	4.302e-06	1.000e-20
C8T28SOI_LL_NAND2X8_P0	8.799e-06	1.000e-20
C8T28SOI_LL_NAND2X12_P0	1.261e-05	1.000e-20
C8T28SOI_LL_NAND2X15_P0	1.643e-05	1.000e-20
C8T28SOI_LL_NAND2X19_P0	2.026e-05	1.000e-20
C8T28SOI_LL_NAND2X24_P0	3.001e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P0	3.694e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P0	6.553e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_P0	9.253e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_P0	1.196e-05	1.000e-20
C8T28SOI_LLS_NAND2X8_P0	8.799e-06	1.000e-20
C8T28SOI_LLS_NAND2X15_P0	1.643e-05	1.000e-20
C8T28SOI_LLS_NAND2X23_P0	2.408e-05	1.000e-20
C8T28SOI_LLS_NAND2X31_P0	3.173e-05	1.000e-20
C8T28SOIDV_LL_NAND2X9_P0	1.053e-05	1.000e-20
C8T28SOIDV_LL_NAND2X18_P0	2.012e-05	1.000e-20
C8T28SOIDV_LL_NAND2X27_P0	2.924e-05	1.000e-20
C8T28SOIDV_LL_NAND2X36_P0	3.838e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P0	C8T28SOI_LL_-NAND2X4_P0	C8T28SOI_LL_-NAND2X8_P0	C8T28SOI_LL_-NAND2X12_P0
A (output stable)	9.665e-06	1.730e-05	7.604e-05	9.702e-05
B (output stable)	1.872e-05	3.315e-05	2.474e-04	2.604e-04
A to Z	4.931e-04	7.829e-04	1.693e-03	2.441e-03
B to Z	4.416e-04	6.811e-04	1.333e-03	2.031e-03
	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X24_P0	C8T28SOI_-LLBR0P8_-NAND2X4_P0
A (output stable)	1.417e-04	1.615e-04	2.046e-05	2.489e-05
B (output stable)	4.342e-04	4.163e-04	3.990e-05	4.649e-05
A to Z	3.261e-03	4.024e-03	7.018e-03	8.532e-04
B to Z	2.621e-03	3.338e-03	6.929e-03	7.212e-04
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	C8T28SOI_-LLBR0P8_-NAND2X12_P0	C8T28SOI_-LLBR0P8_-NAND2X16_P0	C8T28SOI_LLS_-NAND2X8_P0
A (output stable)	9.198e-05	1.143e-04	1.774e-04	7.698e-05
B (output stable)	2.951e-04	3.129e-04	5.195e-04	2.552e-04
A to Z	1.722e-03	2.560e-03	3.254e-03	1.700e-03
B to Z	1.243e-03	1.974e-03	2.371e-03	1.339e-03
	C8T28SOI_LLS_-NAND2X15_P0	C8T28SOI_LLS_-NAND2X23_P0	C8T28SOI_LLS_-NAND2X31_P0	C8T28SOIDV_LL_-NAND2X9_P0
A (output stable)	1.509e-04	2.175e-04	2.826e-04	4.532e-05
B (output stable)	4.506e-04	6.104e-04	7.737e-04	8.064e-05
A to Z	3.299e-03	4.907e-03	6.504e-03	1.834e-03
B to Z	2.650e-03	3.998e-03	5.298e-03	1.591e-03
	C8T28SOIDV_LL_-NAND2X18_P0	C8T28SOIDV_LL_-NAND2X27_P0	C8T28SOIDV_LL_-NAND2X36_P0	
A (output stable)	1.675e-04	2.036e-04	3.349e-04	
B (output stable)	5.657e-04	4.880e-04	1.101e-03	
A to Z	3.753e-03	5.569e-03	7.396e-03	

B to Z	2.965e-03	4.675e-03	5.835e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

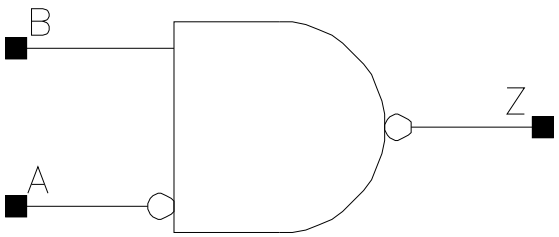
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P0	C8T28SOI_LL_-NAND2X4_P0	C8T28SOI_LL_-NAND2X8_P0	C8T28SOI_LL_-NAND2X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X24_P0	C8T28SOI_-LLBR0P8_-NAND2X4_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	C8T28SOI_-LLBR0P8_-NAND2X12_P0	C8T28SOI_-LLBR0P8_-NAND2X16_P0	C8T28SOI_LLS_-NAND2X8_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P0	C8T28SOI_LLS_-NAND2X23_P0	C8T28SOI_LLS_-NAND2X31_P0	C8T28SOIDV_LL_-NAND2X9_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P0	C8T28SOIDV_LL_-NAND2X27_P0	C8T28SOIDV_LL_-NAND2X36_P0	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.544	0.4352
X4_P0	0.800	0.680	0.5440
X9_P0	1.600	0.544	0.8704
X13_P0	1.600	0.816	1.3056
X17_P0	1.600	0.816	1.3056
X23_P0	0.800	2.312	1.8496
X27_P0	1.600	1.088	1.7408
X31_P0	0.800	2.992	2.3936
X36_P0	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P0	X4_P0	X9_P0	X13_P0
A	0.0005	0.0005	0.0009	0.0008
B	0.0004	0.0005	0.0010	0.0016
	X17_P0	X23_P0	X27_P0	X31_P0
A	0.0008	0.0018	0.0014	0.0024
B	0.0019	0.0028	0.0030	0.0036
	X36_P0			
A	0.0014			
B	0.0039			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X4_P0**	**X2_P0**	**X4_P0**
A to Z ↓	0.0209	0.0214	8.4683	4.7134
A to Z ↑	0.0157	0.0160	7.3811	3.9279
B to Z ↓	0.0095	0.0078	8.7098	4.8453
B to Z ↑	0.0114	0.0090	7.6832	4.1417
	X9_P0	**X13_P0**	**X9_P0**	**X13_P0**
A to Z ↓	0.0213	0.0256	1.8586	1.1793
A to Z ↑	0.0155	0.0189	1.8492	1.2426
B to Z ↓	0.0069	0.0068	1.9235	1.2214
B to Z ↑	0.0092	0.0095	1.9474	1.3252
	X17_P0	**X23_P0**	**X17_P0**	**X23_P0**
A to Z ↓	0.0277	0.0205	0.9295	0.8293
A to Z ↑	0.0197	0.0162	0.9472	0.6502
B to Z ↓	0.0066	0.0074	0.9599	0.8559
B to Z ↑	0.0090	0.0078	1.0174	0.6848
	X27_P0	**X31_P0**	**X27_P0**	**X31_P0**
A to Z ↓	0.0235	0.0204	0.6303	0.6276
A to Z ↑	0.0177	0.0161	0.6322	0.4741
B to Z ↓	0.0065	0.0076	0.6527	0.6471
B to Z ↑	0.0086	0.0080	0.6531	0.5154
	X36_P0		**X36_P0**	
A to Z ↓	0.0269		0.4763	
A to Z ↑	0.0201		0.4742	
B to Z ↓	0.0064		0.4916	
B to Z ↑	0.0084		0.4907	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P0	3.007e-06	1.000e-20
X4_P0	5.986e-06	1.000e-20
X9_P0	1.594e-05	1.000e-20
X13_P0	1.814e-05	1.000e-20
X17_P0	2.416e-05	1.000e-20
X23_P0	3.684e-05	1.000e-20
X27_P0	3.956e-05	1.000e-20
X31_P0	4.830e-05	1.000e-20
X36_P0	4.912e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P0	X4_P0	X9_P0	X13_P0
A (output stable)	7.051e-04	8.576e-04	1.650e-03	2.317e-03
B (output stable)	2.028e-05	3.398e-05	8.587e-05	2.624e-04
A to Z	1.166e-03	1.542e-03	3.297e-03	5.125e-03
B to Z	4.439e-04	6.754e-04	1.603e-03	2.425e-03
	X17_P0	X23_P0	X27_P0	X31_P0
A (output stable)	2.568e-03	4.276e-03	4.117e-03	5.671e-03
B (output stable)	3.088e-04	5.432e-04	5.148e-04	7.250e-04
A to Z	6.103e-03	8.795e-03	9.017e-03	1.172e-02
B to Z	3.032e-03	3.985e-03	4.484e-03	5.277e-03
	X36_P0			
A (output stable)	5.255e-03			

B (output stable)	8.065e-04			
A to Z	1.196e-02			
B to Z	5.797e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

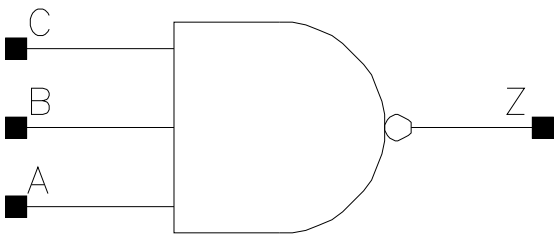
Pin Cycle (vdds)	X2_P0	X4_P0	X9_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P0	X23_P0	X27_P0	X31_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P0	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P0	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P0	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P0	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P0	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P0	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P0	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P0	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P0	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P0	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P0	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P0	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P0	C8T28SOI_LL_-NAND3X7_P0	C8T28SOI_LL_-NAND3X10_P0	C8T28SOI_LL_-NAND3X14_P0
A	0.0005	0.0010	0.0015	0.0020
B	0.0005	0.0010	0.0014	0.0019
C	0.0005	0.0009	0.0013	0.0018
	C8T28SOI_LL_-NAND3X20_P0	C8T28SOI_LL_-NAND3X27_P0	C8T28SOI_-LLBR0P6_-NAND3X3_P0	C8T28SOI_-LLBR0P6_-NAND3X7_P0
A	0.0030	0.0040	0.0006	0.0010
B	0.0028	0.0038	0.0005	0.0010
C	0.0027	0.0036	0.0005	0.0009
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	C8T28SOI_-LLBR0P6_-NAND3X14_P0	C8T28SOI_-LLBR0P6_-NAND3X20_P0	C8T28SOI_-LLBR0P6_-NAND3X27_P0
A	0.0015	0.0020	0.0030	0.0040
B	0.0014	0.0018	0.0027	0.0037
C	0.0014	0.0018	0.0027	0.0036

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-NAND3X3_P0	**C8T28SOI_LL_-NAND3X7_P0**	**C8T28SOI_LL_-NAND3X3_P0**	**C8T28SOI_LL_-NAND3X7_P0**
A to Z ↓	0.0105	0.0118	6.7534	3.4349
A to Z ↑	0.0127	0.0131	4.1322	2.0307
B to Z ↓	0.0114	0.0119	6.7924	3.4532
B to Z ↑	0.0116	0.0119	4.1629	2.0359
C to Z ↓	0.0118	0.0112	6.8225	3.4669
C to Z ↑	0.0106	0.0098	4.2084	1.9674
	C8T28SOI_LL_-NAND3X10_P0	**C8T28SOI_LL_-NAND3X14_P0**	**C8T28SOI_LL_-NAND3X10_P0**	**C8T28SOI_LL_-NAND3X14_P0**
A to Z ↓	0.0112	0.0116	2.3679	1.7941
A to Z ↑	0.0122	0.0126	1.3070	1.0251
B to Z ↓	0.0118	0.0117	2.3823	1.8038
B to Z ↑	0.0112	0.0113	1.3523	1.0253
C to Z ↓	0.0112	0.0112	2.3928	1.8119
C to Z ↑	0.0094	0.0094	1.3619	1.0148
	C8T28SOI_LL_-NAND3X20_P0	**C8T28SOI_LL_-NAND3X27_P0**	**C8T28SOI_LL_-NAND3X20_P0**	**C8T28SOI_LL_-NAND3X27_P0**
A to Z ↓	0.0112	0.0113	1.2219	0.9305
A to Z ↑	0.0121	0.0122	0.6598	0.4985
B to Z ↓	0.0118	0.0119	1.2293	0.9357
B to Z ↑	0.0110	0.0109	0.6599	0.4971
C to Z ↓	0.0112	0.0113	1.2349	0.9403
C to Z ↑	0.0091	0.0091	0.6797	0.5124
	C8T28SOI_-LLBR0P6_-NAND3X3_P0	**C8T28SOI_-LLBR0P6_-NAND3X7_P0**	**C8T28SOI_-LLBR0P6_-NAND3X3_P0**	**C8T28SOI_-LLBR0P6_-NAND3X7_P0**
A to Z ↓	0.0073	0.0091	4.2673	2.4227
A to Z ↑	0.0177	0.0191	6.0594	3.0882
B to Z ↓	0.0073	0.0086	4.3276	2.4483
B to Z ↑	0.0156	0.0166	6.0521	3.0997

C to Z ↓	0.0069	0.0071	4.3796	2.4759
C to Z ↑	0.0134	0.0131	6.0945	3.0695
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	**C8T28SOI_-LLBR0P6_-NAND3X14_P0**	**C8T28SOI_-LLBR0P6_-NAND3X10_P0**	**C8T28SOI_-LLBR0P6_-NAND3X14_P0**
A to Z ↓	0.0082	0.0087	1.6134	1.2310
A to Z ↑	0.0179	0.0184	2.0630	1.5649
B to Z ↓	0.0078	0.0079	1.6338	1.2454
B to Z ↑	0.0154	0.0158	2.0734	1.5686
C to Z ↓	0.0067	0.0064	1.6527	1.2609
C to Z ↑	0.0124	0.0122	2.0891	1.5660
	C8T28SOI_-LLBR0P6_-NAND3X20_P0	**C8T28SOI_-LLBR0P6_-NAND3X27_P0**	**C8T28SOI_-LLBR0P6_-NAND3X20_P0**	**C8T28SOI_-LLBR0P6_-NAND3X27_P0**
A to Z ↓	0.0083	0.0084	0.8326	0.6396
A to Z ↑	0.0180	0.0179	1.0420	0.7871
B to Z ↓	0.0079	0.0079	0.8428	0.6472
B to Z ↑	0.0155	0.0154	1.0437	0.7867
C to Z ↓	0.0064	0.0065	0.8531	0.6550
C to Z ↑	0.0119	0.0119	1.0510	0.7914

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P0	3.278e-06	1.000e-20
C8T28SOI_LL_NAND3X7_P0	6.786e-06	1.000e-20
C8T28SOI_LL_NAND3X10_P0	9.520e-06	1.000e-20
C8T28SOI_LL_NAND3X14_P0	1.261e-05	1.000e-20
C8T28SOI_LL_NAND3X20_P0	1.842e-05	1.000e-20
C8T28SOI_LL_NAND3X27_P0	2.425e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P0	2.500e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P0	4.629e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_P0	6.165e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_P0	8.269e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_P0	1.189e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_P0	1.553e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P0	C8T28SOI_LL_-NAND3X7_P0	C8T28SOI_LL_-NAND3X10_P0	C8T28SOI_LL_-NAND3X14_P0
A (output stable)	1.803e-05	6.587e-05	8.601e-05	1.210e-04
B (output stable)	4.124e-05	1.523e-04	2.136e-04	2.871e-04
C (output stable)	7.444e-05	3.420e-04	4.285e-04	6.329e-04
A to Z	1.055e-03	2.344e-03	3.277e-03	4.433e-03
B to Z	9.370e-04	1.994e-03	2.771e-03	3.747e-03
C to Z	8.361e-04	1.670e-03	2.346e-03	3.145e-03
	C8T28SOI_LL_-NAND3X20_P0	C8T28SOI_LL_-NAND3X27_P0	C8T28SOI_-LLBR0P6_-NAND3X3_P0	C8T28SOI_-LLBR0P6_-NAND3X7_P0
A (output stable)	1.724e-04	2.292e-04	2.989e-05	9.144e-05
B (output stable)	4.262e-04	5.593e-04	6.517e-05	2.039e-04
C (output stable)	9.300e-04	1.202e-03	1.202e-04	4.625e-04

A to Z	6.476e-03	8.588e-03	1.111e-03	2.515e-03
B to Z	5.496e-03	7.270e-03	9.306e-04	2.003e-03
C to Z	4.522e-03	6.022e-03	7.585e-04	1.499e-03
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	C8T28SOI_-LLBR0P6_-NAND3X14_P0	C8T28SOI_-LLBR0P6_-NAND3X20_P0	C8T28SOI_-LLBR0P6_-NAND3X27_P0
A (output stable)	1.182e-04	1.820e-04	2.429e-04	3.289e-04
B (output stable)	2.794e-04	4.124e-04	5.867e-04	7.725e-04
C (output stable)	5.764e-04	8.744e-04	1.257e-03	1.622e-03
A to Z	3.410e-03	4.719e-03	6.816e-03	9.003e-03
B to Z	2.652e-03	3.650e-03	5.292e-03	6.954e-03
C to Z	2.036e-03	2.687e-03	3.862e-03	5.120e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

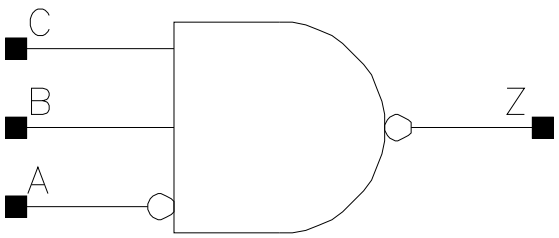
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P0	C8T28SOI_LL_-NAND3X7_P0	C8T28SOI_LL_-NAND3X10_P0	C8T28SOI_LL_-NAND3X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P0	C8T28SOI_LL_-NAND3X27_P0	C8T28SOI_-LLBR0P6_-NAND3X3_P0	C8T28SOI_-LLBR0P6_-NAND3X7_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	C8T28SOI_-LLBR0P6_-NAND3X14_P0	C8T28SOI_-LLBR0P6_-NAND3X20_P0	C8T28SOI_-LLBR0P6_-NAND3X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X7_P0	0.800	1.360	1.0880
X10_P0	0.800	1.632	1.3056
X14_P0	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X10_P0	X14_P0
A	0.0006	0.0009	0.0007	0.0007
B	0.0005	0.0010	0.0014	0.0019
C	0.0005	0.0009	0.0013	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0258	0.0253	6.7335	3.4430
A to Z ↑	0.0182	0.0186	3.9327	1.8964
B to Z ↓	0.0111	0.0117	6.8361	3.4876
B to Z ↑	0.0113	0.0113	4.1693	1.9762
C to Z ↓	0.0114	0.0108	6.8656	3.5008
C to Z ↑	0.0102	0.0093	4.2065	1.9714
	X10_P0	**X14_P0**	**X10_P0**	**X14_P0**
A to Z ↓	0.0277	0.0300	2.3519	1.7956

A to Z ↑	0.0206	0.0227	1.2992	0.9714
B to Z ↓	0.0117	0.0114	2.3808	1.8167
B to Z ↑	0.0111	0.0109	1.3542	1.0130
C to Z ↓	0.0112	0.0108	2.3909	1.8248
C to Z ↑	0.0094	0.0089	1.3650	1.0161

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	4.691e-06	1.000e-20
X7_P0	1.119e-05	1.000e-20
X10_P0	1.436e-05	1.000e-20
X14_P0	1.745e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	8.619e-04	1.595e-03	1.970e-03	2.385e-03
B (output stable)	4.193e-05	1.355e-04	2.183e-04	2.742e-04
C (output stable)	7.563e-05	3.496e-04	4.449e-04	6.135e-04
A to Z	1.815e-03	3.825e-03	5.280e-03	6.760e-03
B to Z	8.938e-04	1.914e-03	2.765e-03	3.613e-03
C to Z	7.919e-04	1.568e-03	2.334e-03	2.996e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

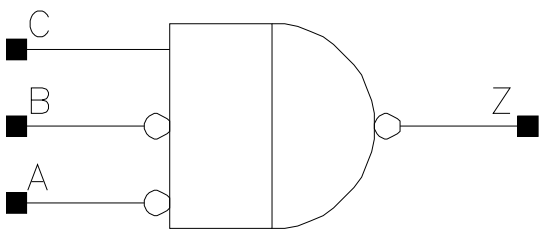
Pin Cycle (vdds)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	0.816	0.6528
X8_P0	0.800	1.088	0.8704
X12_P0	0.800	1.632	1.3056
X15_P0	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X12_P0	X15_P0
A	0.0006	0.0006	0.0012	0.0011
B	0.0007	0.0006	0.0012	0.0011
C	0.0005	0.0009	0.0014	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0231	0.0281	4.4174	2.3672
A to Z ↑	0.0157	0.0181	3.7508	1.8726
B to Z ↓	0.0240	0.0290	4.4153	2.3675
B to Z ↑	0.0147	0.0171	3.7472	1.8694
C to Z ↓	0.0079	0.0073	4.5346	2.4216
C to Z ↑	0.0091	0.0081	3.8342	1.9833
	X12_P0	**X15_P0**	**X12_P0**	**X15_P0**
A to Z ↓	0.0259	0.0280	1.6168	1.2340
A to Z ↑	0.0168	0.0197	1.2501	0.9428
B to Z ↓	0.0253	0.0275	1.6173	1.2344

B to Z ↑	0.0152	0.0180	1.2483	0.9410
C to Z ↓	0.0080	0.0074	1.6581	1.2663
C to Z ↑	0.0085	0.0077	1.3488	0.9929

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	7.944e-06	1.000e-20
X8_P0	1.033e-05	1.000e-20
X12_P0	1.632e-05	1.000e-20
X15_P0	1.857e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	4.736e-04	6.257e-04	1.072e-03	1.201e-03
B (output stable)	4.401e-04	5.896e-04	9.815e-04	1.110e-03
C (output stable)	3.782e-05	2.458e-04	2.655e-04	4.198e-04
A to Z	2.144e-03	3.469e-03	5.493e-03	6.615e-03
B to Z	2.014e-03	3.332e-03	5.030e-03	6.128e-03
C to Z	7.615e-04	1.361e-03	2.135e-03	2.667e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

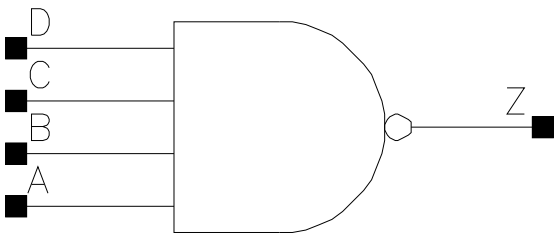
Pin Cycle (vdds)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.224	0.9792
X10_P0	0.800	1.360	1.0880
X14_P0	0.800	1.904	1.5232
X18_P0	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X18_P0
A	0.0004	0.0004	0.0005	0.0005
B	0.0005	0.0005	0.0005	0.0008
C	0.0004	0.0004	0.0005	0.0006
D	0.0005	0.0005	0.0005	0.0006

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0362	0.0341	2.7038	1.3642
A to Z ↑	0.0303	0.0309	3.7845	1.9281
B to Z ↓	0.0379	0.0359	2.7037	1.3638
B to Z ↑	0.0294	0.0304	3.7877	1.9259
C to Z ↓	0.0379	0.0352	2.7009	1.3641
C to Z ↑	0.0319	0.0329	3.7881	1.9223

D to Z ↓	0.0399	0.0372	2.6995	1.3643
D to Z ↑	0.0315	0.0325	3.7838	1.9233
	X14_P0	**X18_P0**	**X14_P0**	**X18_P0**
A to Z ↓	0.0367	0.0342	0.9413	0.7584
A to Z ↑	0.0310	0.0302	1.3227	1.0406
B to Z ↓	0.0385	0.0358	0.9412	0.7589
B to Z ↑	0.0301	0.0296	1.3221	1.0417
C to Z ↓	0.0359	0.0316	0.9411	0.7587
C to Z ↑	0.0316	0.0297	1.3178	1.0383
D to Z ↓	0.0377	0.0330	0.9412	0.7588
D to Z ↑	0.0310	0.0287	1.3191	1.0404

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	6.556e-06	1.000e-20
X10_P0	1.070e-05	1.000e-20
X14_P0	1.535e-05	1.000e-20
X18_P0	2.234e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	3.487e-04	4.134e-04	6.094e-04	6.742e-04
B (output stable)	3.335e-04	3.960e-04	5.841e-04	6.527e-04
C (output stable)	3.809e-04	4.162e-04	6.389e-04	6.528e-04
D (output stable)	3.635e-04	3.989e-04	6.113e-04	6.208e-04
A to Z	2.575e-03	3.653e-03	5.699e-03	6.614e-03
B to Z	2.525e-03	3.602e-03	5.621e-03	6.535e-03
C to Z	2.731e-03	3.746e-03	5.439e-03	6.181e-03
D to Z	2.695e-03	3.702e-03	5.374e-03	6.091e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

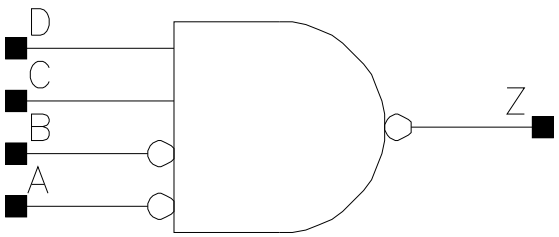
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.952	0.7616
X7_P0	0.800	1.360	1.0880
X10_P0	0.800	2.040	1.6320
X14_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P0	X7_P0	X10_P0	X14_P0
A	0.0006	0.0006	0.0012	0.0010
B	0.0006	0.0006	0.0012	0.0011
C	0.0006	0.0010	0.0014	0.0019
D	0.0005	0.0009	0.0013	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X7_P0	X3_P0	X7_P0
A to Z ↓	0.0264	0.0308	6.4767	3.4426
A to Z ↑	0.0170	0.0196	3.7936	1.9026
B to Z ↓	0.0268	0.0315	6.4806	3.4429
B to Z ↑	0.0158	0.0184	3.7950	1.9024
C to Z ↓	0.0114	0.0116	6.5813	3.4819
C to Z ↑	0.0117	0.0113	3.9936	1.9791

D to Z ↓	0.0113	0.0107	6.5996	3.4941
D to Z ↑	0.0102	0.0092	3.9881	1.9716
	X10_P0	**X14_P0**	**X10_P0**	**X14_P0**
A to Z ↓	0.0291	0.0316	2.3514	1.8006
A to Z ↑	0.0181	0.0224	1.2857	0.9500
B to Z ↓	0.0284	0.0313	2.3513	1.8008
B to Z ↑	0.0165	0.0211	1.2840	0.9477
C to Z ↓	0.0117	0.0115	2.3780	1.8192
C to Z ↑	0.0112	0.0109	1.3552	1.0145
D to Z ↓	0.0111	0.0109	2.3883	1.8273
D to Z ↑	0.0093	0.0090	1.3655	1.0186

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	7.067e-06	1.000e-20
X7_P0	8.742e-06	1.000e-20
X10_P0	1.426e-05	1.000e-20
X14_P0	1.534e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	5.791e-04	7.592e-04	1.357e-03	1.547e-03
B (output stable)	5.346e-04	7.124e-04	1.212e-03	1.414e-03
C (output stable)	8.495e-05	1.581e-04	2.415e-04	3.181e-04
D (output stable)	1.490e-04	3.870e-04	4.913e-04	6.891e-04
A to Z	2.479e-03	3.996e-03	6.296e-03	7.888e-03
B to Z	2.356e-03	3.861e-03	5.845e-03	7.433e-03
C to Z	9.590e-04	1.902e-03	2.742e-03	3.611e-03
D to Z	8.682e-04	1.558e-03	2.316e-03	3.008e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

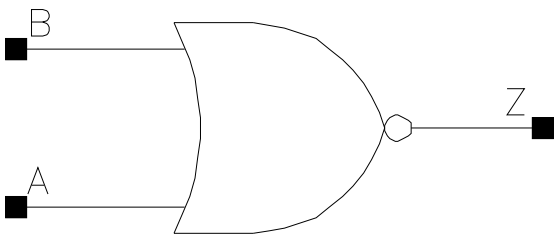
Pin Cycle (vdds)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.408	0.3264
X4_P0	0.800	0.408	0.3264
X8_P0	0.800	0.680	0.5440
X9_P0	1.600	0.408	0.6528
X12_P0	0.800	0.952	0.7616
X16_P0	0.800	1.224	0.9792
X19_P0	1.600	0.680	1.0880
X20_P0	0.800	1.496	1.1968
X23_P0	0.800	1.496	1.1968
X24_P0	0.800	1.768	1.4144
X27_P0	0.800	1.632	1.3056
X29_P0	1.600	0.952	1.5232
X31_P0	0.800	2.312	1.8496
X34_P0	0.800	2.040	1.6320
X38_P0	0.800	2.176	1.7408
X39_P0	1.600	1.224	1.9584
X46_P0	1.600	1.224	1.9584
X57_P0	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P0	X4_P0	X8_P0	X9_P0
A	0.0004	0.0005	0.0010	0.0010
B	0.0004	0.0005	0.0009	0.0010
	X12_P0	X16_P0	X19_P0	X20_P0

A	0.0015	0.0020	0.0021	0.0025
B	0.0014	0.0019	0.0020	0.0023
	X23_P0	X24_P0	X27_P0	X29_P0
A	0.0007	0.0030	0.0007	0.0032
B	0.0006	0.0028	0.0006	0.0030
	X31_P0	X34_P0	X38_P0	X39_P0
A	0.0039	0.0007	0.0007	0.0042
B	0.0037	0.0006	0.0006	0.0040
	X46_P0	X57_P0		
A	0.0007	0.0007		
B	0.0007	0.0007		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X4_P0**	**X2_P0**	**X4_P0**
A to Z ↓	0.0071	0.0067	5.3685	2.9423
A to Z ↑	0.0141	0.0127	14.5895	8.0406
B to Z ↓	0.0062	0.0055	5.4027	2.9670
B to Z ↑	0.0149	0.0131	14.6295	8.0633
	X8_P0	**X9_P0**	**X8_P0**	**X9_P0**
A to Z ↓	0.0062	0.0054	1.4231	1.1295
A to Z ↑	0.0117	0.0117	3.8234	3.6313
B to Z ↓	0.0041	0.0044	1.4239	1.1718
B to Z ↑	0.0103	0.0121	3.8382	3.6450
	X12_P0	**X16_P0**	**X12_P0**	**X16_P0**
A to Z ↓	0.0064	0.0064	0.9764	0.7259
A to Z ↑	0.0112	0.0115	2.5072	1.9200
B to Z ↓	0.0046	0.0044	0.9857	0.7335
B to Z ↑	0.0105	0.0103	2.5194	1.9284
	X19_P0	**X20_P0**	**X19_P0**	**X20_P0**
A to Z ↓	0.0060	0.0066	0.5716	0.5967
A to Z ↑	0.0129	0.0113	1.8636	1.5235
B to Z ↓	0.0045	0.0047	0.5769	0.6029
B to Z ↑	0.0120	0.0106	1.8689	1.5314
	X23_P0	**X24_P0**	**X23_P0**	**X24_P0**
A to Z ↓	0.0249	0.0064	0.5921	0.4942
A to Z ↑	0.0341	0.0113	0.7908	1.2863
B to Z ↓	0.0235	0.0044	0.5913	0.4998
B to Z ↑	0.0346	0.0103	0.7898	1.2928
	X27_P0	**X29_P0**	**X27_P0**	**X29_P0**
A to Z ↓	0.0260	0.0057	0.4936	0.3780
A to Z ↑	0.0352	0.0120	0.6605	1.2520
B to Z ↓	0.0246	0.0042	0.4934	0.3812
B to Z ↑	0.0357	0.0117	0.6604	1.2562
	X31_P0	**X34_P0**	**X31_P0**	**X34_P0**
A to Z ↓	0.0065	0.0273	0.3699	0.4054
A to Z ↑	0.0115	0.0396	0.9655	0.5420
B to Z ↓	0.0047	0.0260	0.3739	0.4055
B to Z ↑	0.0105	0.0404	0.9701	0.5411
	X38_P0	**X39_P0**	**X38_P0**	**X39_P0**
A to Z ↓	0.0281	0.0058	0.3528	0.2884
A to Z ↑	0.0403	0.0123	0.4753	0.9404

B to Z ↓	0.0267	0.0043	0.3532	0.2918
B to Z ↑	0.0411	0.0115	0.4746	0.9434
	X46_P0	**X57_P0**	**X46_P0**	**X57_P0**
A to Z ↓	0.0314	0.0336	0.2680	0.2194
A to Z ↑	0.0416	0.0435	0.4713	0.3794
B to Z ↓	0.0303	0.0326	0.2677	0.2194
B to Z ↑	0.0430	0.0448	0.4713	0.3792

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P0	1.555e-06	1.000e-20
X4_P0	4.026e-06	1.000e-20
X8_P0	8.743e-06	1.000e-20
X9_P0	1.043e-05	1.000e-20
X12_P0	1.253e-05	1.000e-20
X16_P0	1.633e-05	1.000e-20
X19_P0	1.996e-05	1.000e-20
X20_P0	2.014e-05	1.000e-20
X23_P0	3.792e-05	1.000e-20
X24_P0	2.394e-05	1.000e-20
X27_P0	4.341e-05	1.000e-20
X29_P0	2.902e-05	1.000e-20
X31_P0	3.155e-05	1.000e-20
X34_P0	5.034e-05	1.000e-20
X38_P0	5.538e-05	1.000e-20
X39_P0	3.809e-05	1.000e-20
X46_P0	6.088e-05	1.000e-20
X57_P0	7.241e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P0	X4_P0	X8_P0	X9_P0
A (output stable)	1.575e-05	2.652e-05	1.024e-04	5.825e-05
B (output stable)	2.088e-05	3.973e-05	1.975e-04	9.123e-05
A to Z	4.942e-04	8.312e-04	1.648e-03	1.748e-03
B to Z	4.297e-04	7.060e-04	1.216e-03	1.505e-03
	X12_P0	X16_P0	X19_P0	X20_P0
A (output stable)	1.434e-04	2.022e-04	2.160e-04	2.390e-04
B (output stable)	2.539e-04	3.681e-04	4.424e-04	3.999e-04
A to Z	2.432e-03	3.264e-03	3.745e-03	4.070e-03
B to Z	1.896e-03	2.463e-03	2.998e-03	3.150e-03
	X23_P0	X24_P0	X27_P0	X29_P0
A (output stable)	2.919e-05	2.936e-04	2.937e-05	2.772e-04
B (output stable)	4.472e-05	5.006e-04	4.484e-05	4.835e-04
A to Z	6.964e-03	4.816e-03	7.820e-03	5.272e-03
B to Z	6.843e-03	3.672e-03	7.700e-03	4.294e-03
	X31_P0	X34_P0	X38_P0	X39_P0
A (output stable)	3.930e-04	3.090e-05	3.099e-05	4.133e-04
B (output stable)	6.725e-04	4.769e-05	4.787e-05	7.617e-04
A to Z	6.434e-03	1.036e-02	1.133e-02	7.132e-03
B to Z	4.942e-03	1.023e-02	1.119e-02	5.691e-03
	X46_P0	X57_P0		

A (output stable)	3.150e-05	3.176e-05		
B (output stable)	4.900e-05	4.919e-05		
A to Z	1.242e-02	1.512e-02		
B to Z	1.232e-02	1.502e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

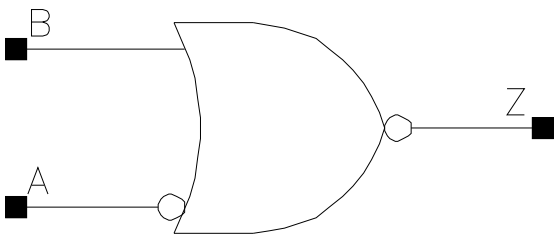
Pin Cycle (vdds)	X2_P0	X4_P0	X8_P0	X9_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P0	X16_P0	X19_P0	X20_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P0	X24_P0	X27_P0	X29_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P0	X34_P0	X38_P0	X39_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P0	X57_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.544	0.4352
X3_P0	0.800	0.544	0.4352
X4_P0	0.800	0.544	0.4352
X10_P0	1.600	0.544	0.8704
X14_P0	1.600	0.816	1.3056
X19_P0	1.600	0.816	1.3056
X29_P0	1.600	1.088	1.7408
X39_P0	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P0	X3_P0	X4_P0	X10_P0
A	0.0005	0.0005	0.0005	0.0009
B	0.0003	0.0004	0.0004	0.0010
	X14_P0	X19_P0	X29_P0	X39_P0
A	0.0009	0.0009	0.0014	0.0014
B	0.0016	0.0019	0.0030	0.0039

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	X3_P0	X2_P0	X3_P0
A to Z ↓	0.0198	0.0199	5.1210	3.8867
A to Z ↑	0.0182	0.0181	14.4525	12.3020
B to Z ↓	0.0060	0.0051	5.4365	4.1114

B to Z ↑	0.0142	0.0136	14.6205	12.4352
	X4_P0	**X10_P0**	**X4_P0**	**X10_P0**
A to Z ↓	0.0205	0.0204	2.9890	1.0835
A to Z ↑	0.0180	0.0175	8.9995	3.5648
B to Z ↓	0.0048	0.0044	3.1628	1.1167
B to Z ↑	0.0124	0.0124	9.1006	3.6080
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0245	0.0257	0.6814	0.5334
A to Z ↑	0.0204	0.0209	2.4203	1.7936
B to Z ↓	0.0041	0.0039	0.7734	0.6065
B to Z ↑	0.0116	0.0108	2.4521	1.8177
	X29_P0	**X39_P0**	**X29_P0**	**X39_P0**
A to Z ↓	0.0224	0.0258	0.3600	0.2700
A to Z ↑	0.0200	0.0217	1.2459	0.9151
B to Z ↓	0.0041	0.0039	0.3823	0.2997
B to Z ↑	0.0116	0.0106	1.2616	0.9271

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P0	3.047e-06	1.000e-20
X3_P0	3.664e-06	1.000e-20
X4_P0	5.153e-06	1.000e-20
X10_P0	1.606e-05	1.000e-20
X14_P0	1.814e-05	1.000e-20
X19_P0	2.552e-05	1.000e-20
X29_P0	3.933e-05	1.000e-20
X39_P0	4.967e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P0	X3_P0	X4_P0	X10_P0
A (output stable)	7.079e-04	7.590e-04	8.359e-04	1.688e-03
B (output stable)	2.305e-05	2.689e-05	3.720e-05	9.618e-05
A to Z	1.174e-03	1.281e-03	1.473e-03	3.342e-03
B to Z	4.063e-04	4.675e-04	5.812e-04	1.569e-03
	X14_P0	X19_P0	X29_P0	X39_P0
A (output stable)	2.411e-03	2.668e-03	4.202e-03	5.321e-03
B (output stable)	1.458e-04	1.922e-04	5.138e-04	3.714e-04
A to Z	4.860e-03	5.785e-03	9.199e-03	1.156e-02
B to Z	2.128e-03	2.680e-03	4.256e-03	5.286e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P0	X3_P0	X4_P0	X10_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P0	X19_P0	X29_P0	X39_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

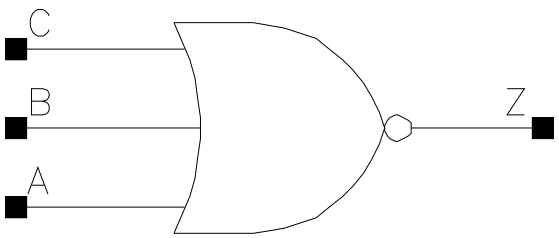
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.544	0.4352
X7_P0	0.800	0.952	0.7616
X11_P0	0.800	1.360	1.0880
X14_P0	0.800	1.768	1.4144
X21_P0	0.800	2.584	2.0672
X29_P0	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X11_P0	X14_P0
A	0.0005	0.0009	0.0015	0.0020
B	0.0005	0.0011	0.0014	0.0021
C	0.0005	0.0009	0.0014	0.0018
	X21_P0	X29_P0		
A	0.0032	0.0042		
B	0.0031	0.0042		
C	0.0027	0.0037		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0077	0.0078	2.9984	1.5677
A to Z ↑	0.0161	0.0166	11.2896	5.8294

B to Z ↓	0.0071	0.0070	3.0221	1.5081
B to Z ↑	0.0160	0.0168	11.3182	5.8451
C to Z ↓	0.0061	0.0049	3.0633	1.5291
C to Z ↑	0.0157	0.0134	11.3309	5.8448
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0078	0.0079	0.9858	0.7561
A to Z ↑	0.0169	0.0164	3.8558	2.7988
B to Z ↓	0.0072	0.0070	0.9951	0.7349
B to Z ↑	0.0159	0.0162	3.8662	2.8066
C to Z ↓	0.0054	0.0051	0.9946	0.7498
C to Z ↑	0.0145	0.0134	3.8678	2.8086
	X21_P0	**X29_P0**	**X21_P0**	**X29_P0**
A to Z ↓	0.0078	0.0079	0.5034	0.3781
A to Z ↑	0.0162	0.0164	1.8800	1.4142
B to Z ↓	0.0071	0.0072	0.4945	0.3743
B to Z ↑	0.0160	0.0161	1.8848	1.4178
C to Z ↓	0.0053	0.0054	0.5054	0.3821
C to Z ↑	0.0136	0.0137	1.8865	1.4194

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	3.336e-06	1.000e-20
X7_P0	6.714e-06	1.000e-20
X11_P0	9.759e-06	1.000e-20
X14_P0	1.358e-05	1.000e-20
X21_P0	1.974e-05	1.000e-20
X29_P0	2.612e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	2.995e-05	7.215e-05	1.294e-04	1.493e-04
B (output stable)	2.992e-05	8.767e-05	1.139e-04	1.725e-04
C (output stable)	5.649e-05	1.839e-04	2.216e-04	3.688e-04
A to Z	1.008e-03	2.024e-03	3.190e-03	4.171e-03
B to Z	8.617e-04	1.771e-03	2.569e-03	3.622e-03
C to Z	7.315e-04	1.272e-03	2.102e-03	2.663e-03
	X21_P0	X29_P0		
A (output stable)	2.175e-04	2.898e-04		
B (output stable)	2.508e-04	3.396e-04		
C (output stable)	5.227e-04	7.034e-04		
A to Z	6.175e-03	8.248e-03		
B to Z	5.323e-03	7.105e-03		
C to Z	3.983e-03	5.318e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

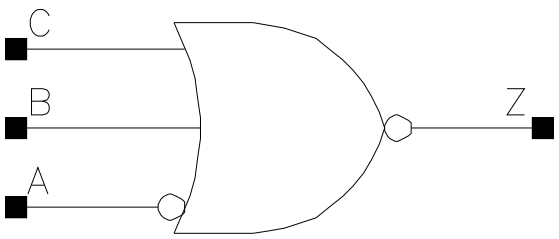
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P0	X29_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X7_P0	0.800	1.360	1.0880
X11_P0	0.800	1.632	1.3056
X14_P0	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X11_P0	X14_P0
A	0.0006	0.0006	0.0009	0.0012
B	0.0005	0.0010	0.0014	0.0019
C	0.0005	0.0009	0.0014	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0220	0.0199	2.8298	1.3360
A to Z ↑	0.0239	0.0238	11.3189	5.5416
B to Z ↓	0.0071	0.0071	3.0334	1.4378
B to Z ↑	0.0159	0.0165	11.4038	5.5802
C to Z ↓	0.0061	0.0052	3.0689	1.4494
C to Z ↑	0.0156	0.0140	11.4177	5.5818
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0241	0.0193	0.9422	0.6969

A to Z ↑	0.0269	0.0235	3.8529	2.8412
B to Z ↓	0.0071	0.0070	0.9963	0.7453
B to Z ↑	0.0158	0.0158	3.8779	2.8633
C to Z ↓	0.0053	0.0051	0.9961	0.7540
C to Z ↑	0.0143	0.0136	3.8805	2.8649

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	4.990e-06	1.000e-20
X7_P0	1.209e-05	1.000e-20
X11_P0	1.413e-05	1.000e-20
X14_P0	2.159e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	8.903e-04	1.571e-03	2.031e-03	2.894e-03
B (output stable)	3.262e-05	1.037e-04	1.343e-04	2.008e-04
C (output stable)	6.079e-05	2.206e-04	2.505e-04	3.887e-04
A to Z	1.878e-03	3.873e-03	5.230e-03	7.279e-03
B to Z	8.526e-04	1.842e-03	2.559e-03	3.462e-03
C to Z	7.245e-04	1.396e-03	2.057e-03	2.651e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

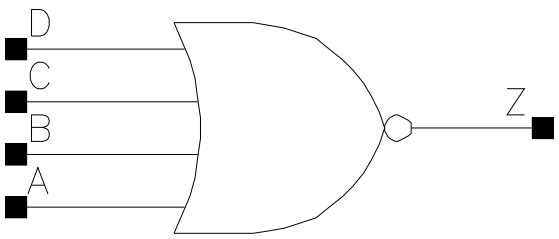
Pin Cycle (vdds)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.224	0.9792
X10_P0	0.800	1.632	1.3056
X14_P0	0.800	1.904	1.5232
X18_P0	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X18_P0
A	0.0004	0.0004	0.0004	0.0005
B	0.0005	0.0006	0.0006	0.0007
C	0.0004	0.0004	0.0005	0.0006
D	0.0005	0.0004	0.0005	0.0006

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0234	0.0274	2.8029	1.3493
A to Z ↑	0.0389	0.0435	3.9886	1.9239
B to Z ↓	0.0227	0.0274	2.8035	1.3482
B to Z ↑	0.0400	0.0459	3.9918	1.9210
C to Z ↓	0.0244	0.0279	2.8027	1.3469
C to Z ↑	0.0416	0.0468	3.9902	1.9229

D to Z ↓	0.0240	0.0269	2.7995	1.3468
D to Z ↑	0.0434	0.0477	3.9893	1.9211
	X14_P0	**X18_P0**	**X14_P0**	**X18_P0**
A to Z ↓	0.0263	0.0275	0.9300	0.7357
A to Z ↑	0.0398	0.0388	1.3244	0.9924
B to Z ↓	0.0258	0.0266	0.9298	0.7359
B to Z ↑	0.0415	0.0397	1.3253	0.9924
C to Z ↓	0.0256	0.0277	0.9277	0.7342
C to Z ↑	0.0399	0.0395	1.3254	0.9895
D to Z ↓	0.0248	0.0265	0.9273	0.7342
D to Z ↑	0.0410	0.0403	1.3243	0.9919

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.095e-05	1.000e-20
X10_P0	1.797e-05	1.000e-20
X14_P0	2.706e-05	1.000e-20
X18_P0	3.806e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	3.701e-04	4.672e-04	5.848e-04	7.221e-04
B (output stable)	3.450e-04	4.490e-04	5.577e-04	6.783e-04
C (output stable)	3.986e-04	4.563e-04	6.209e-04	7.853e-04
D (output stable)	3.778e-04	4.300e-04	5.867e-04	7.369e-04
A to Z	2.529e-03	3.976e-03	5.582e-03	7.101e-03
B to Z	2.465e-03	3.920e-03	5.485e-03	6.980e-03
C to Z	2.632e-03	3.925e-03	5.262e-03	6.733e-03
D to Z	2.585e-03	3.857e-03	5.177e-03	6.608e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

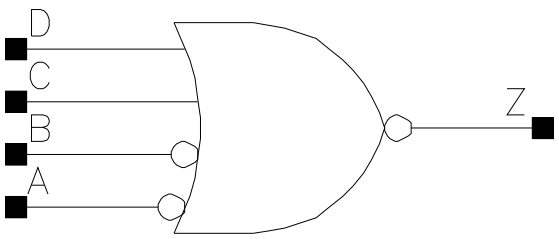
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	1.224	0.9792
X7_P0	0.800	1.496	1.1968
X11_P0	0.800	2.040	1.6320
X14_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P0	X7_P0	X11_P0	X14_P0
A	0.0007	0.0007	0.0012	0.0012
B	0.0007	0.0007	0.0012	0.0012
C	0.0005	0.0010	0.0014	0.0019
D	0.0005	0.0009	0.0014	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X7_P0	X4_P0	X7_P0
A to Z ↓	0.0222	0.0230	2.6292	1.3587
A to Z ↑	0.0299	0.0293	10.8657	5.6254
B to Z ↓	0.0206	0.0213	2.6280	1.3582
B to Z ↑	0.0304	0.0297	10.8751	5.6291
C to Z ↓	0.0073	0.0070	2.7693	1.4492
C to Z ↑	0.0169	0.0165	10.9226	5.6685

D to Z ↓	0.0062	0.0051	2.7864	1.4481
D to Z ↑	0.0165	0.0141	10.9293	5.6684
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0209	0.0229	0.9309	0.7010
A to Z ↑	0.0272	0.0295	3.8053	2.8299
B to Z ↓	0.0190	0.0212	0.9302	0.6995
B to Z ↑	0.0275	0.0303	3.8056	2.8295
C to Z ↓	0.0072	0.0072	0.9957	0.7435
C to Z ↑	0.0157	0.0160	3.8279	2.8486
D to Z ↓	0.0053	0.0052	0.9965	0.7469
D to Z ↑	0.0143	0.0138	3.8308	2.8502

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	8.016e-06	1.000e-20
X7_P0	1.051e-05	1.000e-20
X11_P0	1.662e-05	1.000e-20
X14_P0	1.891e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X7_P0	X11_P0	X14_P0
A (output stable)	7.358e-04	8.326e-04	1.363e-03	1.612e-03
B (output stable)	7.144e-04	8.113e-04	1.296e-03	1.558e-03
C (output stable)	7.211e-05	1.008e-04	1.523e-04	2.132e-04
D (output stable)	1.043e-04	2.149e-04	2.768e-04	4.215e-04
A to Z	3.079e-03	4.135e-03	6.360e-03	8.187e-03
B to Z	2.888e-03	3.947e-03	5.970e-03	7.805e-03
C to Z	9.648e-04	1.815e-03	2.571e-03	3.506e-03
D to Z	8.429e-04	1.389e-03	2.073e-03	2.710e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

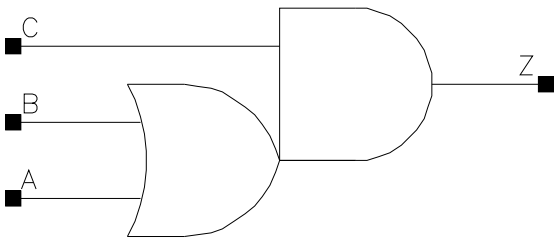
Pin Cycle (vdds)	X4_P0	X7_P0	X11_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.680	0.5440
X10_P0	0.800	0.952	0.7616
X19_P0	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0005	0.0006	0.0011
B	0.0006	0.0006	0.0013
C	0.0007	0.0008	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0217	0.0245	2.7031	1.3563
A to Z ↑	0.0181	0.0215	4.3832	1.9200
B to Z ↓	0.0225	0.0254	2.7054	1.3566
B to Z ↑	0.0166	0.0198	4.3730	1.9171
C to Z ↓	0.0200	0.0216	2.6775	1.3378
C to Z ↑	0.0171	0.0198	4.3775	1.9159
	X19_P0		**X19_P0**	
A to Z ↓	0.0255		0.7061	
A to Z ↑	0.0227		0.9812	

B to Z ↓	0.0264		0.7060	
B to Z ↑	0.0207		0.9802	
C to Z ↓	0.0218		0.6956	
C to Z ↑	0.0201		0.9799	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	9.001e-06	1.000e-20
X10_P0	1.602e-05	1.000e-20
X19_P0	3.015e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	6.383e-05	6.593e-05	1.345e-04
B (output stable)	7.041e-05	7.450e-05	1.449e-04
C (output stable)	4.502e-05	4.642e-05	9.184e-05
A to Z	1.774e-03	2.961e-03	5.994e-03
B to Z	1.659e-03	2.829e-03	5.749e-03
C to Z	1.943e-03	3.036e-03	6.053e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

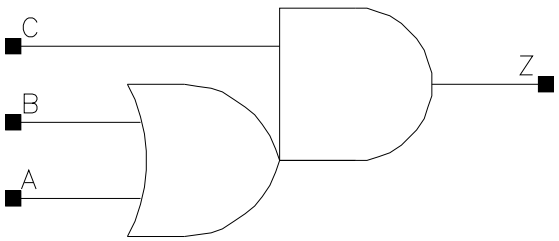
Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	1.360	1.0880
X14_P0	0.800	1.496	1.1968
X19_P0	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0005	0.0012	0.0012	0.0012
B	0.0006	0.0011	0.0011	0.0011
C	0.0006	0.0012	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0266	0.0222	2.6494	1.3455
A to Z ↑	0.0185	0.0171	3.8043	1.8618
B to Z ↓	0.0274	0.0227	2.6512	1.3446
B to Z ↑	0.0172	0.0159	3.7992	1.8601
C to Z ↓	0.0184	0.0151	2.6033	1.3277
C to Z ↑	0.0173	0.0156	3.7959	1.8587
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0247	0.0269	0.9374	0.7061

A to Z ↑	0.0188	0.0202	1.2628	0.9478
B to Z ↓	0.0254	0.0277	0.9369	0.7064
B to Z ↑	0.0177	0.0192	1.2619	0.9473
C to Z ↓	0.0171	0.0187	0.9219	0.6922
C to Z ↑	0.0176	0.0193	1.2592	0.9456

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.018e-05	1.000e-20
X10_P0	2.133e-05	1.000e-20
X14_P0	2.577e-05	1.000e-20
X19_P0	3.020e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	2.144e-05	4.353e-05	4.354e-05	4.355e-05
B (output stable)	2.441e-05	5.621e-05	5.627e-05	5.654e-05
C (output stable)	1.823e-04	3.684e-04	3.689e-04	3.694e-04
A to Z	2.220e-03	3.943e-03	5.094e-03	6.201e-03
B to Z	2.089e-03	3.629e-03	4.782e-03	5.899e-03
C to Z	1.872e-03	3.248e-03	4.310e-03	5.309e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

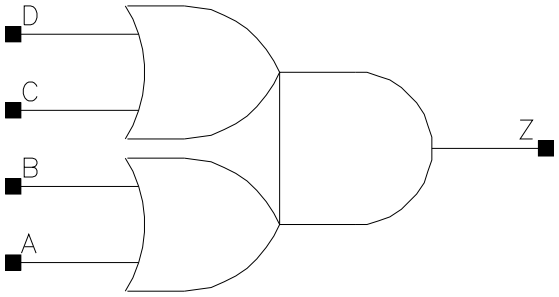
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.952	0.7616
X10_P0	0.800	1.088	0.8704
X14_P0	0.800	1.904	1.5232
X19_P0	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0006	0.0011	0.0011
B	0.0004	0.0006	0.0012	0.0011
C	0.0004	0.0006	0.0012	0.0012
D	0.0004	0.0006	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0366	0.0298	2.7345	1.3641
A to Z ↑	0.0254	0.0221	3.8215	1.9058
B to Z ↓	0.0377	0.0307	2.7337	1.3645

B to Z ↑	0.0244	0.0209	3.8185	1.9038
C to Z ↓	0.0314	0.0264	2.7166	1.3581
C to Z ↑	0.0248	0.0223	3.8171	1.9045
D to Z ↓	0.0323	0.0271	2.7152	1.3578
D to Z ↑	0.0235	0.0207	3.8128	1.9010
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0286	0.0301	0.9493	0.7111
A to Z ↑	0.0211	0.0220	1.2672	0.9523
B to Z ↓	0.0285	0.0301	0.9497	0.7114
B to Z ↑	0.0195	0.0204	1.2647	0.9499
C to Z ↓	0.0244	0.0261	0.9442	0.7078
C to Z ↑	0.0207	0.0218	1.2656	0.9511
D to Z ↓	0.0240	0.0258	0.9447	0.7079
D to Z ↑	0.0187	0.0198	1.2628	0.9490

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	6.540e-06	1.000e-20
X10_P0	1.526e-05	1.000e-20
X14_P0	2.501e-05	1.000e-20
X19_P0	2.851e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	1.882e-05	2.964e-05	8.506e-05	8.492e-05
B (output stable)	2.106e-05	3.707e-05	1.479e-04	1.471e-04
C (output stable)	5.748e-05	7.227e-05	1.706e-04	1.704e-04
D (output stable)	6.184e-05	8.157e-05	2.274e-04	2.274e-04
A to Z	2.248e-03	3.514e-03	5.922e-03	6.833e-03
B to Z	2.166e-03	3.361e-03	5.474e-03	6.388e-03
C to Z	1.965e-03	3.163e-03	5.186e-03	6.097e-03
D to Z	1.892e-03	3.029e-03	4.745e-03	5.654e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

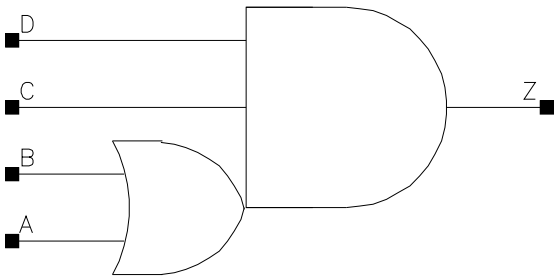
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	0.816	0.6528
X10_P0	0.800	1.088	0.8704
X14_P0	0.800	1.904	1.5232
X19_P0	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0009	0.0010	0.0011
B	0.0005	0.0006	0.0010	0.0012
C	0.0005	0.0006	0.0010	0.0012
D	0.0004	0.0006	0.0010	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X10_P0	X4_P0	X10_P0
A to Z ↓	0.0311	0.0301	2.9668	1.3903
A to Z ↑	0.0286	0.0298	4.0510	1.9426
B to Z ↓	0.0325	0.0290	2.9685	1.3898
B to Z ↑	0.0276	0.0262	4.0427	1.9380
C to Z ↓	0.0265	0.0237	2.8969	1.3642

C to Z ↑	0.0265	0.0258	4.0420	1.9357
D to Z ↓	0.0259	0.0229	2.8985	1.3631
D to Z ↑	0.0283	0.0272	4.0453	1.9352
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0296	0.0282	0.9497	0.7060
A to Z ↑	0.0288	0.0294	1.2923	0.9670
B to Z ↓	0.0292	0.0279	0.9505	0.7058
B to Z ↑	0.0263	0.0269	1.2882	0.9634
C to Z ↓	0.0248	0.0237	0.9331	0.6943
C to Z ↑	0.0258	0.0261	1.2878	0.9635
D to Z ↓	0.0235	0.0226	0.9308	0.6930
D to Z ↑	0.0266	0.0269	1.2878	0.9640

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	6.948e-06	1.000e-20
X10_P0	1.673e-05	1.000e-20
X14_P0	2.364e-05	1.000e-20
X19_P0	3.157e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X10_P0	X14_P0	X19_P0
A (output stable)	6.633e-05	1.079e-04	1.800e-04	2.012e-04
B (output stable)	7.081e-05	1.160e-04	1.935e-04	2.190e-04
C (output stable)	1.256e-05	2.603e-05	6.612e-05	7.408e-05
D (output stable)	3.150e-05	5.341e-05	1.746e-04	1.934e-04
A to Z	1.907e-03	3.498e-03	5.348e-03	6.686e-03
B to Z	1.847e-03	3.217e-03	4.970e-03	6.215e-03
C to Z	2.039e-03	3.512e-03	5.599e-03	6.904e-03
D to Z	1.968e-03	3.397e-03	5.273e-03	6.543e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

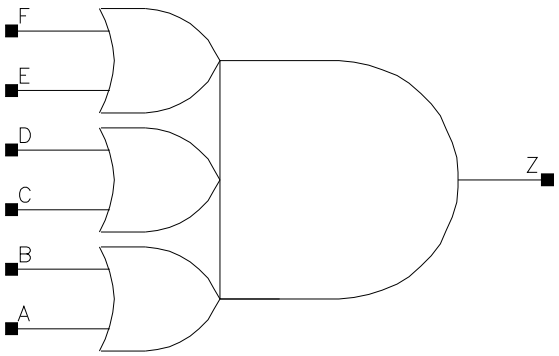
Pin Cycle (vdds)	X4_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	1.360	1.0880
X9_P0	0.800	1.496	1.1968
X19_P0	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P0	X9_P0	X19_P0
A	0.0005	0.0006	0.0010
B	0.0006	0.0008	0.0012
C	0.0004	0.0006	0.0010
D	0.0004	0.0005	0.0012
E	0.0005	0.0006	0.0010
F	0.0005	0.0006	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X9_P0**	**X4_P0**	**X9_P0**
A to Z ↓	0.0431	0.0359	3.0195	1.4913
A to Z ↑	0.0325	0.0307	4.1613	2.0412
B to Z ↓	0.0454	0.0378	3.0204	1.4925
B to Z ↑	0.0323	0.0298	4.1638	2.0395
C to Z ↓	0.0397	0.0328	3.0000	1.4838
C to Z ↑	0.0334	0.0306	4.1656	2.0404
D to Z ↓	0.0406	0.0337	3.0014	1.4846
D to Z ↑	0.0319	0.0290	4.1609	2.0380
E to Z ↓	0.0341	0.0292	2.9757	1.4757
E to Z ↑	0.0309	0.0292	4.1590	2.0386
F to Z ↓	0.0355	0.0303	2.9772	1.4773
F to Z ↑	0.0299	0.0280	4.1558	2.0358
	X19_P0		**X19_P0**	
A to Z ↓	0.0351		0.7170	
A to Z ↑	0.0296		0.9671	
B to Z ↓	0.0365		0.7173	
B to Z ↑	0.0276		0.9642	
C to Z ↓	0.0325		0.7133	
C to Z ↑	0.0299		0.9666	
D to Z ↓	0.0336		0.7137	
D to Z ↑	0.0283		0.9642	
E to Z ↓	0.0288		0.7096	
E to Z ↑	0.0288		0.9655	
F to Z ↓	0.0299		0.7102	
F to Z ↑	0.0270		0.9632	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	6.907e-06	1.000e-20
X9_P0	1.686e-05	1.000e-20
X19_P0	3.219e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X9_P0	X19_P0
A (output stable)	1.605e-05	2.702e-05	4.889e-05
B (output stable)	2.286e-05	3.601e-05	6.023e-05
C (output stable)	3.824e-05	5.321e-05	1.042e-04
D (output stable)	4.059e-05	5.889e-05	1.161e-04
E (output stable)	1.021e-04	1.294e-04	2.440e-04
F (output stable)	1.007e-04	1.350e-04	2.522e-04
A to Z	2.643e-03	4.184e-03	8.174e-03
B to Z	2.591e-03	4.071e-03	7.887e-03
C to Z	2.408e-03	3.847e-03	7.560e-03
D to Z	2.323e-03	3.695e-03	7.274e-03
E to Z	2.101e-03	3.487e-03	6.862e-03
F to Z	2.039e-03	3.366e-03	6.612e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

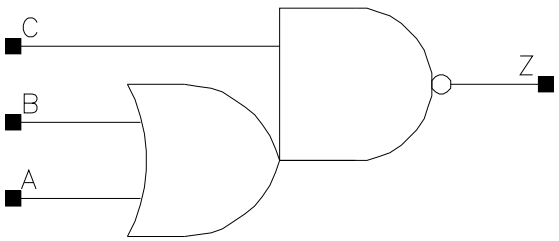
Pin Cycle (vdds)	X4_P0	X9_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.544	0.4352
X10_P0	0.800	1.360	1.0880
X20_P0	0.800	2.720	2.1760
X26_P0	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P0	X10_P0	X20_P0	X26_P0
A	0.0004	0.0014	0.0028	0.0037
B	0.0004	0.0013	0.0026	0.0035
C	0.0005	0.0015	0.0031	0.0041

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X10_P0**	**X3_P0**	**X10_P0**
A to Z ↓	0.0092	0.0103	5.3214	1.6815
A to Z ↑	0.0126	0.0126	9.1138	2.5473
B to Z ↓	0.0076	0.0083	5.2057	1.6878
B to Z ↑	0.0129	0.0118	9.1425	2.5596
C to Z ↓	0.0085	0.0091	4.8337	1.5443
C to Z ↑	0.0124	0.0115	4.8285	1.3543
	X20_P0	**X26_P0**	**X20_P0**	**X26_P0**
A to Z ↓	0.0109	0.0110	0.8606	0.6522

A to Z ↑	0.0131	0.0131	1.3079	0.9841
B to Z ↓	0.0087	0.0089	0.8694	0.6620
B to Z ↑	0.0124	0.0124	1.3140	0.9889
C to Z ↓	0.0096	0.0096	0.7930	0.6019
C to Z ↑	0.0118	0.0117	0.6669	0.5016

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	4.299e-06	1.000e-20
X10_P0	1.549e-05	1.000e-20
X20_P0	3.000e-05	1.000e-20
X26_P0	3.947e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X10_P0	X20_P0	X26_P0
A (output stable)	5.690e-05	2.097e-04	4.273e-04	5.541e-04
B (output stable)	6.369e-05	2.427e-04	4.980e-04	6.450e-04
C (output stable)	4.067e-05	1.422e-04	3.018e-04	3.877e-04
A to Z	7.173e-04	2.660e-03	5.480e-03	7.274e-03
B to Z	6.122e-04	2.074e-03	4.376e-03	5.829e-03
C to Z	8.933e-04	3.081e-03	6.422e-03	8.474e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

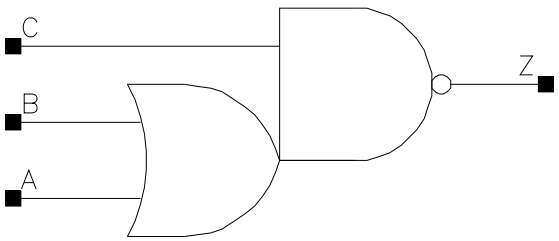
Pin Cycle (vdds)	X3_P0	X10_P0	X20_P0	X26_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X7_P0	0.800	0.952	0.7616
X10_P0	0.800	1.360	1.0880
X13_P0	0.800	1.904	1.5232
X26_P0	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X10_P0	X13_P0
A	0.0005	0.0009	0.0016	0.0020
B	0.0005	0.0010	0.0014	0.0018
C	0.0007	0.0009	0.0014	0.0019
	X26_P0			
A	0.0040			
B	0.0036			
C	0.0038			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X7_P0	X3_P0	X7_P0
A to Z ↓	0.0112	0.0100	4.6537	2.4221
A to Z ↑	0.0169	0.0149	7.3104	3.7613
B to Z ↓	0.0098	0.0082	4.6712	2.3498

B to Z ↑	0.0174	0.0151	7.3368	3.7740
C to Z ↓	0.0095	0.0081	4.4202	2.2476
C to Z ↑	0.0106	0.0089	3.9866	2.0823
	X10_P0	**X13_P0**	**X10_P0**	**X13_P0**
A to Z ↓	0.0096	0.0103	1.6369	1.2544
A to Z ↑	0.0143	0.0155	2.4847	1.9173
B to Z ↓	0.0080	0.0082	1.6283	1.2568
B to Z ↑	0.0145	0.0147	2.4933	1.9234
C to Z ↓	0.0079	0.0081	1.5435	1.1795
C to Z ↑	0.0084	0.0084	1.3721	1.0406
	X26_P0		**X26_P0**	
A to Z ↓	0.0102		0.6482	
A to Z ↑	0.0152		0.9682	
B to Z ↓	0.0081		0.6462	
B to Z ↑	0.0144		0.9722	
C to Z ↓	0.0083		0.6084	
C to Z ↑	0.0083		0.5257	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	5.957e-06	1.000e-20
X7_P0	1.108e-05	1.000e-20
X10_P0	1.603e-05	1.000e-20
X13_P0	2.071e-05	1.000e-20
X26_P0	3.977e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X7_P0	X10_P0	X13_P0
A (output stable)	2.460e-05	4.500e-05	6.561e-05	1.161e-04
B (output stable)	2.767e-05	5.341e-05	7.821e-05	1.611e-04
C (output stable)	1.907e-04	3.667e-04	4.969e-04	7.220e-04
A to Z	1.291e-03	2.102e-03	3.051e-03	4.377e-03
B to Z	1.135e-03	1.821e-03	2.608e-03	3.501e-03
C to Z	9.215e-04	1.571e-03	2.239e-03	3.093e-03
	X26_P0			
A (output stable)	2.253e-04			
B (output stable)	2.986e-04			
C (output stable)	1.320e-03			
A to Z	8.481e-03			
B to Z	6.715e-03			
C to Z	5.968e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P0	X7_P0	X10_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

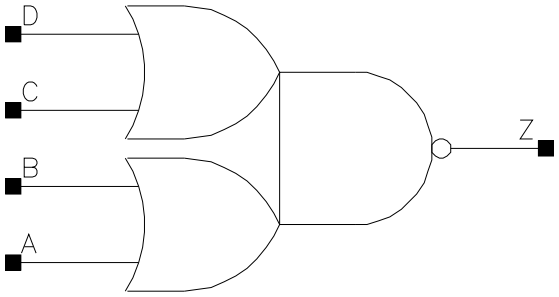
	X26_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X6_P0	0.800	1.360	1.0880
X8_P0	0.800	1.768	1.4144
X11_P0	0.800	2.448	1.9584
X24_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X8_P0	X11_P0
A	0.0005	0.0010	0.0015	0.0019
B	0.0005	0.0009	0.0013	0.0018
C	0.0005	0.0009	0.0014	0.0018
D	0.0004	0.0008	0.0013	0.0017
	X24_P0			
A	0.0042			
B	0.0038			
C	0.0039			
D	0.0036			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X6_P0**	**X3_P0**	**X6_P0**
A to Z ↓	0.0103	0.0123	4.3844	2.3862
A to Z ↑	0.0185	0.0183	8.9997	3.9770
B to Z ↓	0.0092	0.0104	4.3444	2.3932
B to Z ↑	0.0191	0.0175	9.0148	3.9874
C to Z ↓	0.0087	0.0109	4.4659	2.3982
C to Z ↑	0.0131	0.0137	9.0293	4.0019
D to Z ↓	0.0074	0.0085	4.4177	2.4242
D to Z ↑	0.0134	0.0122	9.0576	4.0214
	X8_P0	**X11_P0**	**X8_P0**	**X11_P0**
A to Z ↓	0.0117	0.0119	1.6330	1.2392
A to Z ↑	0.0171	0.0172	2.6656	2.0021
B to Z ↓	0.0101	0.0100	1.6421	1.2415
B to Z ↑	0.0167	0.0167	2.6782	2.0106
C to Z ↓	0.0106	0.0109	1.6529	1.2527
C to Z ↑	0.0127	0.0131	2.6648	2.0188
D to Z ↓	0.0088	0.0087	1.6709	1.2580
D to Z ↑	0.0120	0.0120	2.6812	2.0306
	X24_P0		**X24_P0**	
A to Z ↓	0.0120		0.6116	
A to Z ↑	0.0173		0.9688	
B to Z ↓	0.0102		0.6067	
B to Z ↑	0.0169		0.9729	
C to Z ↓	0.0113		0.6186	
C to Z ↑	0.0131		0.9697	
D to Z ↓	0.0090		0.6159	
D to Z ↑	0.0122		0.9756	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	5.261e-06	1.000e-20
X6_P0	1.289e-05	1.000e-20
X8_P0	1.880e-05	1.000e-20
X11_P0	2.519e-05	1.000e-20
X24_P0	4.694e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X6_P0	X8_P0	X11_P0
A (output stable)	2.645e-05	8.846e-05	1.120e-04	1.568e-04
B (output stable)	3.236e-05	1.507e-04	1.718e-04	2.635e-04
C (output stable)	6.919e-05	1.740e-04	2.253e-04	3.095e-04
D (output stable)	7.909e-05	2.326e-04	2.863e-04	4.117e-04
A to Z	1.173e-03	2.727e-03	3.773e-03	5.095e-03
B to Z	1.042e-03	2.265e-03	3.145e-03	4.233e-03
C to Z	7.998e-04	2.027e-03	2.806e-03	3.876e-03
D to Z	6.942e-04	1.582e-03	2.249e-03	3.072e-03
	X24_P0			
A (output stable)	3.220e-04			
B (output stable)	4.890e-04			
C (output stable)	6.091e-04			
D (output stable)	7.746e-04			

A to Z	1.049e-02			
B to Z	8.713e-03			
C to Z	7.971e-03			
D to Z	6.337e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

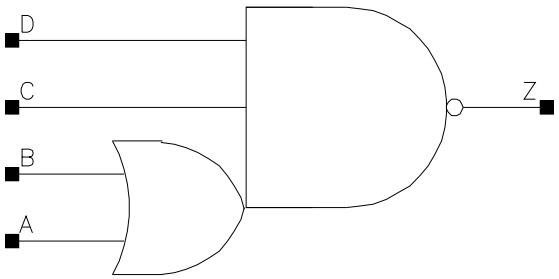
Pin Cycle (vdds)	X3_P0	X6_P0	X8_P0	X11_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X6_P0	0.800	1.360	1.0880
X12_P0	0.800	2.448	1.9584
X18_P0	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X12_P0	X18_P0
A	0.0007	0.0009	0.0018	0.0027
B	0.0005	0.0009	0.0017	0.0025
C	0.0005	0.0010	0.0020	0.0031
D	0.0005	0.0010	0.0019	0.0028

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0168	0.0145	6.4538	3.4937
A to Z ↑	0.0183	0.0149	7.5869	3.8228
B to Z ↓	0.0129	0.0117	6.4914	3.5085
B to Z ↑	0.0161	0.0138	7.5996	3.8384
C to Z ↓	0.0136	0.0135	6.0832	3.2946

C to Z ↑	0.0146	0.0141	3.8311	1.9796
D to Z ↓	0.0149	0.0137	6.1246	3.3157
D to Z ↑	0.0142	0.0128	3.9430	1.9875
	X12_P0	**X18_P0**	**X12_P0**	**X18_P0**
A to Z ↓	0.0148	0.0150	1.8229	1.2345
A to Z ↑	0.0147	0.0146	1.9193	1.2884
B to Z ↓	0.0119	0.0123	1.8325	1.2430
B to Z ↑	0.0136	0.0137	1.9294	1.2948
C to Z ↓	0.0134	0.0136	1.7193	1.1655
C to Z ↑	0.0138	0.0136	1.0123	0.6670
D to Z ↓	0.0138	0.0139	1.7306	1.1726
D to Z ↑	0.0125	0.0125	1.0091	0.6747

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	4.896e-06	1.000e-20
X6_P0	8.789e-06	1.000e-20
X12_P0	1.643e-05	1.000e-20
X18_P0	2.408e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X6_P0	X12_P0	X18_P0
A (output stable)	1.104e-04	2.220e-04	4.134e-04	5.922e-04
B (output stable)	1.166e-04	2.414e-04	4.436e-04	6.299e-04
C (output stable)	2.309e-05	6.974e-05	1.276e-04	2.072e-04
D (output stable)	5.297e-05	1.845e-04	3.282e-04	5.111e-04
A to Z	1.330e-03	2.141e-03	4.193e-03	6.248e-03
B to Z	1.046e-03	1.701e-03	3.295e-03	4.957e-03
C to Z	1.522e-03	2.803e-03	5.331e-03	7.981e-03
D to Z	1.408e-03	2.407e-03	4.615e-03	6.851e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

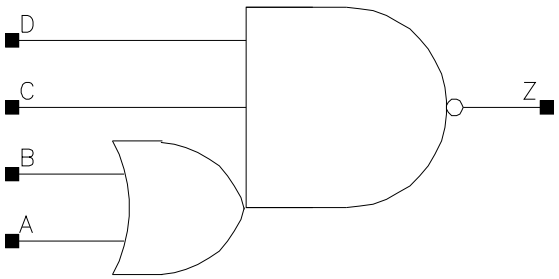
Pin Cycle (vdds)	X3_P0	X6_P0	X12_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X6_P0	0.800	1.360	1.0880
X9_P0	0.800	1.768	1.4144
X12_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X9_P0	X12_P0
A	0.0005	0.0010	0.0016	0.0020
B	0.0005	0.0009	0.0013	0.0021
C	0.0005	0.0009	0.0014	0.0019
D	0.0005	0.0009	0.0014	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0136	0.0140	6.9599	3.4511
A to Z ↑	0.0178	0.0188	7.6771	3.8218
B to Z ↓	0.0120	0.0119	6.8085	3.4663
B to Z ↑	0.0182	0.0182	7.6992	3.8312
C to Z ↓	0.0114	0.0120	6.5738	3.3023

C to Z ↑	0.0113	0.0116	4.1631	2.0633
D to Z ↓	0.0118	0.0116	6.6085	3.3190
D to Z ↑	0.0102	0.0098	4.1999	2.0790
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0142	0.0142	2.3734	1.8067
A to Z ↑	0.0182	0.0186	2.5199	1.9681
B to Z ↓	0.0122	0.0121	2.3714	1.8101
B to Z ↑	0.0178	0.0185	2.5287	1.9769
C to Z ↓	0.0120	0.0121	2.2630	1.7243
C to Z ↑	0.0112	0.0113	1.3622	1.0341
D to Z ↓	0.0119	0.0118	2.2748	1.7336
D to Z ↑	0.0096	0.0094	1.3719	1.0452

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P0	4.252e-06	1.000e-20
X6_P0	8.867e-06	1.000e-20
X9_P0	1.255e-05	1.000e-20
X12_P0	1.651e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	1.707e-05	3.801e-05	5.862e-05	7.509e-05
B (output stable)	1.769e-05	5.031e-05	7.019e-05	9.696e-05
C (output stable)	5.617e-05	1.290e-04	1.941e-04	2.541e-04
D (output stable)	9.002e-05	3.343e-04	3.893e-04	6.157e-04
A to Z	1.312e-03	2.836e-03	4.135e-03	5.531e-03
B to Z	1.151e-03	2.355e-03	3.419e-03	4.569e-03
C to Z	9.496e-04	2.082e-03	2.971e-03	4.032e-03
D to Z	8.460e-04	1.773e-03	2.577e-03	3.402e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

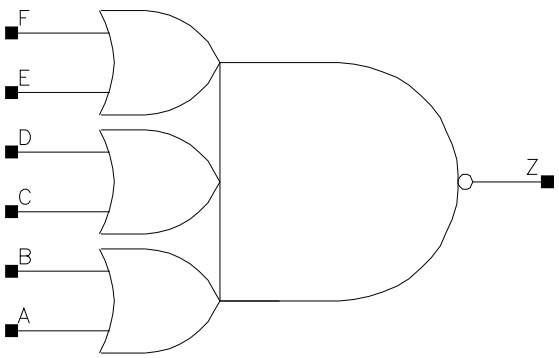
Pin Cycle (vdds)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.224	0.9792
X3_P0	0.800	1.224	0.9792
X5_P0	0.800	2.040	1.6320
X8_P0	0.800	2.720	2.1760
X10_P0	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P0	X3_P0	X5_P0	X8_P0
A	0.0004	0.0005	0.0010	0.0015
B	0.0004	0.0005	0.0009	0.0014
C	0.0004	0.0005	0.0010	0.0014
D	0.0005	0.0005	0.0009	0.0013

E	0.0004	0.0005	0.0009	0.0014
F	0.0004	0.0005	0.0009	0.0013
	X10_P0			
A	0.0020			
B	0.0018			
C	0.0019			
D	0.0018			
E	0.0018			
F	0.0017			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X3_P0**	**X2_P0**	**X3_P0**
A to Z ↓	0.0178	0.0170	7.6059	5.9353
A to Z ↑	0.0254	0.0220	10.3844	7.2175
B to Z ↓	0.0166	0.0158	7.6248	5.9683
B to Z ↑	0.0265	0.0231	10.4002	7.2357
C to Z ↓	0.0177	0.0173	7.6632	5.9659
C to Z ↑	0.0222	0.0198	10.3905	7.3433
D to Z ↓	0.0169	0.0156	7.7403	6.0456
D to Z ↑	0.0239	0.0203	10.4286	7.3595
E to Z ↓	0.0155	0.0152	7.6876	5.9776
E to Z ↑	0.0177	0.0158	10.4069	7.3630
F to Z ↓	0.0144	0.0137	7.7594	6.0647
F to Z ↑	0.0186	0.0162	10.4437	7.3906
	X5_P0	**X8_P0**	**X5_P0**	**X8_P0**
A to Z ↓	0.0182	0.0178	3.1808	2.1687
A to Z ↑	0.0229	0.0220	3.8175	2.5251
B to Z ↓	0.0161	0.0159	3.1983	2.1702
B to Z ↑	0.0224	0.0221	3.8275	2.5331
C to Z ↓	0.0170	0.0176	3.2094	2.1860
C to Z ↑	0.0194	0.0191	3.8570	2.5879
D to Z ↓	0.0150	0.0154	3.2191	2.1918
D to Z ↑	0.0190	0.0194	3.8721	2.5968
E to Z ↓	0.0161	0.0159	3.2292	2.1927
E to Z ↑	0.0158	0.0152	3.8648	2.5968
F to Z ↓	0.0137	0.0137	3.2430	2.1956
F to Z ↑	0.0150	0.0151	3.8835	2.6099
	X10_P0		**X10_P0**	
A to Z ↓	0.0182		1.6497	
A to Z ↑	0.0223		1.9209	
B to Z ↓	0.0162		1.6526	
B to Z ↑	0.0222		1.9275	
C to Z ↓	0.0173		1.6623	
C to Z ↑	0.0192		1.9605	
D to Z ↓	0.0153		1.6660	
D to Z ↑	0.0191		1.9689	
E to Z ↓	0.0162		1.6681	
E to Z ↑	0.0155		1.9564	
F to Z ↓	0.0141		1.6774	
F to Z ↑	0.0151		1.9674	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P0	4.594e-06	1.000e-20
X3_P0	8.137e-06	1.000e-20
X5_P0	1.459e-05	1.000e-20
X8_P0	2.077e-05	1.000e-20
X10_P0	2.732e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P0	X3_P0	X5_P0	X8_P0
A (output stable)	2.138e-05	2.712e-05	7.576e-05	1.015e-04
B (output stable)	2.494e-05	3.338e-05	1.156e-04	1.413e-04
C (output stable)	4.552e-05	5.648e-05	1.330e-04	1.834e-04
D (output stable)	5.071e-05	6.133e-05	1.724e-04	2.164e-04
E (output stable)	1.152e-04	1.403e-04	2.564e-04	3.841e-04
F (output stable)	1.207e-04	1.484e-04	2.951e-04	4.212e-04
A to Z	1.612e-03	1.954e-03	3.936e-03	5.656e-03
B to Z	1.497e-03	1.801e-03	3.434e-03	4.972e-03
C to Z	1.337e-03	1.647e-03	3.158e-03	4.623e-03
D to Z	1.245e-03	1.490e-03	2.748e-03	4.079e-03
E to Z	1.038e-03	1.297e-03	2.589e-03	3.670e-03
F to Z	9.487e-04	1.162e-03	2.177e-03	3.175e-03
	X10_P0			
A (output stable)	1.435e-04			
B (output stable)	2.112e-04			
C (output stable)	2.527e-04			
D (output stable)	3.221e-04			
E (output stable)	4.942e-04			
F (output stable)	5.579e-04			
A to Z	7.636e-03			
B to Z	6.662e-03			
C to Z	6.170e-03			
D to Z	5.376e-03			
E to Z	5.008e-03			
F to Z	4.265e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P0	X3_P0	X5_P0	X8_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P0			

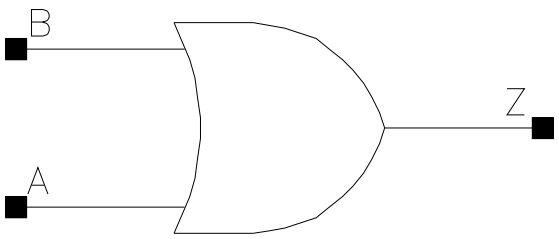
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.544	0.4352
X9_P0	0.800	0.680	0.5440
X19_P0	0.800	1.360	1.0880
X29_P0	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0	X29_P0
A	0.0005	0.0006	0.0011	0.0011
B	0.0004	0.0006	0.0011	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X9_P0**	**X5_P0**	**X9_P0**
A to Z ↓	0.0275	0.0242	2.8650	1.4435
A to Z ↑	0.0171	0.0180	3.9513	1.9887
B to Z ↓	0.0281	0.0245	2.8658	1.4425
B to Z ↑	0.0162	0.0168	3.9496	1.9881
	X19_P0	**X29_P0**	**X19_P0**	**X29_P0**
A to Z ↓	0.0246	0.0290	0.6936	0.4748
A to Z ↑	0.0179	0.0205	0.9434	0.6340
B to Z ↓	0.0241	0.0286	0.6929	0.4747
B to Z ↑	0.0163	0.0189	0.9428	0.6326

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	4.650e-06	1.000e-20
X9_P0	1.032e-05	1.000e-20
X19_P0	2.032e-05	1.000e-20
X29_P0	2.549e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0	X29_P0
A (output stable)	1.653e-05	3.047e-05	1.071e-04	1.075e-04
B (output stable)	2.490e-05	4.443e-05	2.145e-04	2.150e-04
A to Z	1.635e-03	2.644e-03	5.604e-03	7.956e-03
B to Z	1.563e-03	2.525e-03	5.157e-03	7.493e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

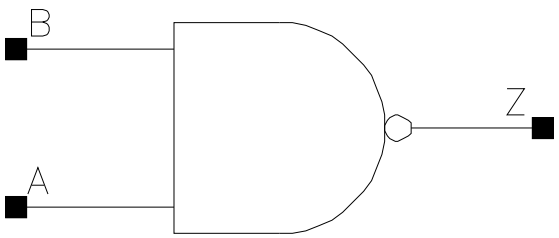
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0	X29_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X9_P0	0.800	0.952	0.7616
X14_P0	0.800	1.088	0.8704
X18_P0	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P0	X9_P0	X14_P0	X18_P0
A	0.0006	0.0006	0.0006	0.0005
B	0.0006	0.0007	0.0007	0.0006

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X9_P0**	**X5_P0**	**X9_P0**
A to Z ↓	0.0218	0.0249	2.5951	1.4177
A to Z ↑	0.0239	0.0264	3.7848	1.9980
B to Z ↓	0.0227	0.0264	2.5954	1.4175
B to Z ↑	0.0225	0.0254	3.7802	2.0004
	X14_P0	**X18_P0**	**X14_P0**	**X18_P0**
A to Z ↓	0.0274	0.0292	0.9808	0.7413
A to Z ↑	0.0281	0.0290	1.3190	1.0258
B to Z ↓	0.0288	0.0305	0.9811	0.7417
B to Z ↑	0.0272	0.0281	1.3184	1.0278

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	1.475e-05	1.000e-20
X9_P0	1.671e-05	1.000e-20
X14_P0	1.960e-05	1.000e-20
X18_P0	2.080e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X9_P0	X14_P0	X18_P0
A (output stable)	1.939e-05	1.764e-05	1.773e-05	1.848e-05
B (output stable)	3.914e-05	3.405e-05	3.417e-05	3.478e-05
A to Z	2.932e-03	3.765e-03	4.827e-03	5.475e-03
B to Z	2.838e-03	3.678e-03	4.740e-03	5.386e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

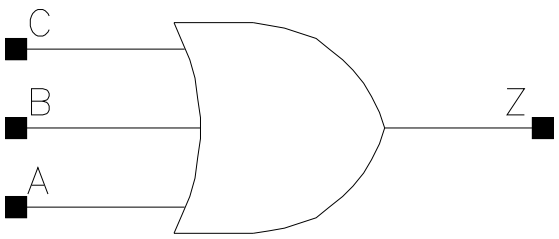
Pin Cycle (vdds)	X5_P0	X9_P0	X14_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.680	0.5440
X10_P0	0.800	0.952	0.7616
X14_P0	0.800	1.496	1.1968
X19_P0	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0005	0.0007	0.0010	0.0017
B	0.0004	0.0006	0.0013	0.0017
C	0.0005	0.0006	0.0011	0.0017

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0360	0.0321	2.9578	1.4068
A to Z ↑	0.0200	0.0176	3.9737	1.8820
B to Z ↓	0.0362	0.0322	2.9594	1.4082
B to Z ↑	0.0195	0.0168	3.9732	1.8812
C to Z ↓	0.0365	0.0319	2.9588	1.4061
C to Z ↑	0.0187	0.0156	3.9700	1.8796
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0303	0.0296	0.9443	0.7249

A to Z ↑	0.0163	0.0162	1.2880	0.9904
B to Z ↓	0.0309	0.0292	0.9456	0.7256
B to Z ↑	0.0153	0.0157	1.2849	0.9897
C to Z ↓	0.0282	0.0281	0.9441	0.7252
C to Z ↑	0.0139	0.0141	1.2820	0.9892

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	3.813e-06	1.000e-20
X10_P0	8.663e-06	1.000e-20
X14_P0	1.428e-05	1.000e-20
X19_P0	1.924e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	1.901e-05	3.412e-05	7.218e-05	1.298e-04
B (output stable)	1.611e-05	3.394e-05	8.865e-05	1.144e-04
C (output stable)	2.816e-05	6.288e-05	2.015e-04	2.168e-04
A to Z	1.936e-03	3.214e-03	5.241e-03	7.501e-03
B to Z	1.845e-03	3.061e-03	4.979e-03	6.877e-03
C to Z	1.775e-03	2.923e-03	4.486e-03	6.357e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

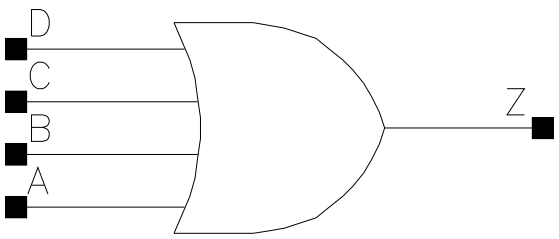
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	1.224	0.9792
X8_P0	0.800	1.496	1.1968
X12_P0	0.800	2.176	1.7408
X15_P0	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X12_P0	X15_P0
A	0.0004	0.0006	0.0010	0.0011
B	0.0004	0.0006	0.0010	0.0012
C	0.0004	0.0006	0.0010	0.0012
D	0.0005	0.0007	0.0009	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0287	0.0274	4.4470	2.3637
A to Z ↑	0.0175	0.0180	3.6771	1.9749
B to Z ↓	0.0299	0.0284	4.4447	2.3648
B to Z ↑	0.0167	0.0171	3.6730	1.9741
C to Z ↓	0.0307	0.0268	4.4522	2.3607
C to Z ↑	0.0183	0.0177	3.7790	1.9806

D to Z ↓	0.0323	0.0280	4.4511	2.3604
D to Z ↑	0.0177	0.0169	3.7760	1.9813
	X12_P0	**X15_P0**	**X12_P0**	**X15_P0**
A to Z ↓	0.0276	0.0281	1.6355	1.2285
A to Z ↑	0.0183	0.0176	1.2603	0.9702
B to Z ↓	0.0277	0.0278	1.6357	1.2283
B to Z ↑	0.0173	0.0161	1.2587	0.9691
C to Z ↓	0.0268	0.0269	1.6328	1.2267
C to Z ↑	0.0174	0.0168	1.2551	0.9750
D to Z ↓	0.0268	0.0268	1.6325	1.2262
D to Z ↑	0.0164	0.0155	1.2524	0.9733

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	5.094e-06	1.000e-20
X8_P0	1.310e-05	1.000e-20
X12_P0	1.582e-05	1.000e-20
X15_P0	2.349e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	4.180e-04	7.432e-04	1.136e-03	1.560e-03
B (output stable)	3.940e-04	6.966e-04	1.040e-03	1.421e-03
C (output stable)	4.183e-04	7.386e-04	1.078e-03	1.486e-03
D (output stable)	3.954e-04	6.929e-04	9.861e-04	1.372e-03
A to Z	1.769e-03	3.495e-03	4.945e-03	6.622e-03
B to Z	1.706e-03	3.370e-03	4.655e-03	6.144e-03
C to Z	1.815e-03	3.149e-03	4.456e-03	5.769e-03
D to Z	1.759e-03	3.031e-03	4.183e-03	5.372e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

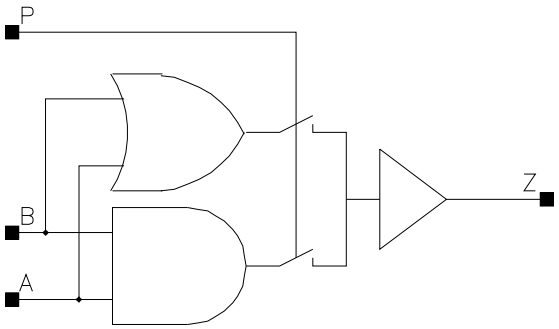
Pin Cycle (vdds)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.952	0.7616
X10_P0	1.600	0.816	1.3056
X14_P0	1.600	1.224	1.9584
X19_P0	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0009	0.0010	0.0019	0.0019
B	0.0008	0.0011	0.0020	0.0021
P	0.0005	0.0007	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0339	0.0310	2.9085	1.3543
A to Z ↑	0.0195	0.0228	3.9765	1.8971
B to Z ↓	0.0338	0.0316	2.9178	1.3603
B to Z ↑	0.0203	0.0239	3.9838	1.8983
P to Z ↓	0.0311	0.0302	2.9141	1.3598
P to Z ↑	0.0196	0.0235	3.9798	1.8966
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**

A to Z ↓	0.0287	0.0306	0.9358	0.6970
A to Z ↑	0.0221	0.0230	1.3031	0.9720
B to Z ↓	0.0274	0.0292	0.9437	0.7018
B to Z ↑	0.0219	0.0230	1.3039	0.9732
P to Z ↓	0.0270	0.0291	0.9459	0.7027
P to Z ↑	0.0222	0.0234	1.3034	0.9725

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	6.627e-06	1.000e-20
X10_P0	1.672e-05	1.000e-20
X14_P0	2.682e-05	1.000e-20
X19_P0	3.230e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	4.747e-05	6.878e-05	1.853e-04	1.768e-04
B (output stable)	5.954e-05	9.763e-05	3.576e-04	3.481e-04
P (output stable)	1.324e-04	2.159e-04	4.068e-04	3.806e-04
A to Z	1.960e-03	3.711e-03	5.952e-03	7.082e-03
B to Z	1.905e-03	3.668e-03	5.612e-03	6.743e-03
P to Z	1.745e-03	3.475e-03	5.532e-03	6.722e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

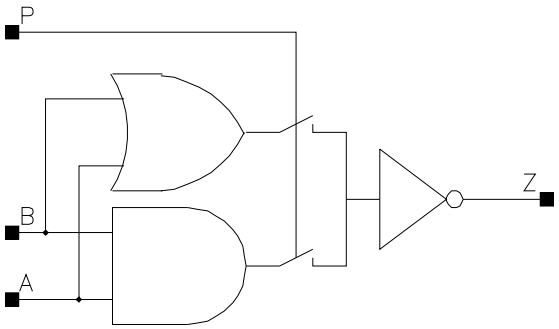
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.600	0.544	0.8704
X10_P0	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P0	X10_P0
A	0.0009	0.0018
B	0.0009	0.0016
P	0.0006	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0121	0.0113	4.5226	2.3714
A to Z ↑	0.0188	0.0173	7.3286	3.7260
B to Z ↓	0.0127	0.0109	4.4684	2.3787
B to Z ↑	0.0188	0.0158	7.2983	3.7761
P to Z ↓	0.0126	0.0105	4.5826	2.4019
P to Z ↑	0.0179	0.0145	7.3752	3.7498

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	7.467e-06	1.000e-20
X10_P0	1.363e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0
A (output stable)	6.551e-05	1.836e-04
B (output stable)	8.844e-05	3.474e-04
P (output stable)	1.896e-04	4.296e-04
A to Z	1.464e-03	2.592e-03
B to Z	1.382e-03	2.215e-03
P to Z	1.203e-03	2.007e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

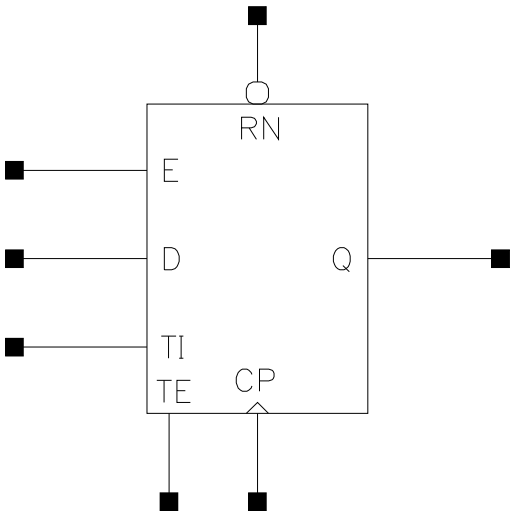
Pin Cycle (vdds)	X5_P0	X10_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.600	2.992	4.7872
X10_P0	1.600	3.128	5.0048
X19_P0	1.600	3.264	5.2224
X23_P0	1.600	3.264	5.2224
X29_P0	1.600	3.536	5.6576
X34_P0	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0	X23_P0
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0011	0.0011	0.0011	0.0011

RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P0	X34_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0011	0.0011		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
CP to Q ↓	0.0430	0.0685	2.6575	1.3354
CP to Q ↑	0.0581	0.0893	3.7264	1.9012
RN to Q ↓	0.0361	0.0660	2.6555	1.3354
	X19_P0	**X23_P0**	**X19_P0**	**X23_P0**
CP to Q ↓	0.0740	0.0744	0.6916	0.5201
CP to Q ↑	0.0930	0.0915	0.9577	0.9355
RN to Q ↓	0.0670	0.0675	0.6896	0.5184
	X29_P0	**X34_P0**	**X29_P0**	**X34_P0**
CP to Q ↓	0.0627	0.0621	0.4557	0.3599
CP to Q ↑	0.0756	0.0762	0.6352	0.6343
RN to Q ↓	0.0569	0.0563	0.4560	0.3600

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P0	X10_P0	X19_P0	X23_P0
CP ↓	min_pulse_width to CP	0.0549	0.0549	0.0549	0.0549
CP ↑	min_pulse_width to CP	0.0395	0.0394	0.0394	0.0394
D ↓	hold_rising to CP	-0.0289	-0.0289	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0072	-0.0072	-0.0072	-0.0072
D ↓	setup_rising to CP	0.0614	0.0614	0.0614	0.0614
D ↑	setup_rising to CP	0.0347	0.0347	0.0347	0.0347
E ↓	hold_rising to CP	-0.0283	-0.0283	-0.0283	-0.0283
E ↑	hold_rising to CP	-0.0066	-0.0066	-0.0066	-0.0066
E ↓	setup_rising to CP	0.0857	0.0857	0.0857	0.0857
E ↑	setup_rising to CP	0.0640	0.0640	0.0640	0.0640
RN ↓	min_pulse_width to RN	0.0496	0.0447	0.0447	0.0469
RN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
RN ↑	removal_rising to CP	0.0091	0.0091	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0110	-0.0110	-0.0110	-0.0110

TE ↑	hold_rising to CP	-0.0013	-0.0013	-0.0013	-0.0013
TE ↓	setup_rising to CP	0.0479	0.0479	0.0479	0.0479
TE ↑	setup_rising to CP	0.0591	0.0591	0.0591	0.0591
TI ↓	hold_rising to CP	-0.0280	-0.0280	-0.0280	-0.0280
TI ↑	hold_rising to CP	-0.0045	-0.0045	-0.0045	-0.0045
TI ↓	setup_rising to CP	0.0576	0.0576	0.0576	0.0576
TI ↑	setup_rising to CP	0.0293	0.0293	0.0293	0.0293
		X29_P0	X34_P0		
CP ↓	min_pulse_width to CP	0.0549	0.0549		
CP ↑	min_pulse_width to CP	0.0394	0.0394		
D ↓	hold_rising to CP	-0.0289	-0.0289		
D ↑	hold_rising to CP	-0.0072	-0.0072		
D ↓	setup_rising to CP	0.0614	0.0614		
D ↑	setup_rising to CP	0.0347	0.0347		
E ↓	hold_rising to CP	-0.0257	-0.0257		
E ↑	hold_rising to CP	-0.0066	-0.0066		
E ↓	setup_rising to CP	0.0857	0.0857		
E ↑	setup_rising to CP	0.0640	0.0640		
RN ↓	min_pulse_width to RN	0.0496	0.0496		
RN ↑	recovery_rising to CP	-0.0017	-0.0017		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0110	-0.0110		
TE ↑	hold_rising to CP	-0.0013	-0.0013		
TE ↓	setup_rising to CP	0.0479	0.0479		
TE ↑	setup_rising to CP	0.0591	0.0591		
TI ↓	hold_rising to CP	-0.0280	-0.0280		
TI ↑	hold_rising to CP	-0.0045	-0.0045		
TI ↓	setup_rising to CP	0.0576	0.0576		
TI ↑	setup_rising to CP	0.0293	0.0293		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	2.642e-05	1.000e-20
X10_P0	3.336e-05	1.000e-20
X19_P0	4.754e-05	1.000e-20
X23_P0	4.911e-05	1.000e-20

X29_P0	6.608e-05	1.000e-20
X34_P0	6.807e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

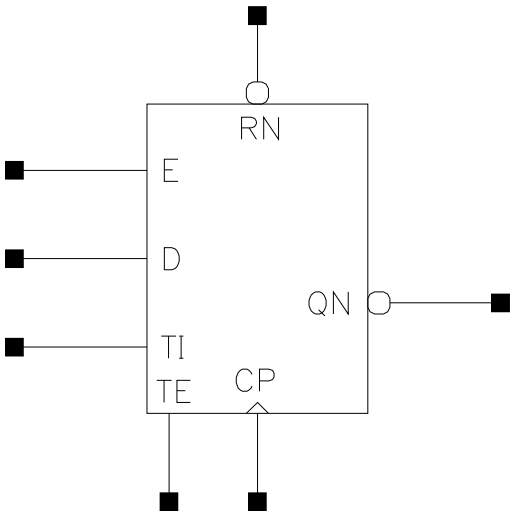
Pin Cycle	X5_P0	X10_P0	X19_P0	X23_P0
Clock 100Mhz Data 0Mhz	7.717e-03	7.708e-03	7.716e-03	7.719e-03
Clock 100Mhz Data 25Mhz	7.967e-03	8.400e-03	9.119e-03	9.161e-03
Clock 100Mhz Data 50Mhz	8.217e-03	9.093e-03	1.052e-02	1.060e-02
Clock = 0 Data 100Mhz	4.459e-03	4.459e-03	4.457e-03	4.457e-03
Clock = 1 Data 100Mhz	1.811e-03	1.811e-03	1.809e-03	1.810e-03
	X29_P0	X34_P0		
Clock 100Mhz Data 0Mhz	7.719e-03	7.719e-03		
Clock 100Mhz Data 25Mhz	9.806e-03	9.994e-03		
Clock 100Mhz Data 50Mhz	1.189e-02	1.227e-02		
Clock = 0 Data 100Mhz	4.456e-03	4.456e-03		
Clock = 1 Data 100Mhz	1.809e-03	1.809e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.600	2.992	4.7872
X10_P0	1.600	3.128	5.0048
X19_P0	1.600	3.264	5.2224
X23_P0	1.600	3.264	5.2224
X29_P0	1.600	3.536	5.6576
X34_P0	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0	X23_P0
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0011	0.0012	0.0012	0.0012

RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P0	X34_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0012	0.0011		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
CP to QN ↓	0.0787	0.0688	2.6577	1.3342
CP to QN ↑	0.0581	0.0538	3.7260	1.9002
RN to QN ↑	0.0554	0.0479	3.7244	1.9018
	X19_P0	**X23_P0**	**X19_P0**	**X23_P0**
CP to QN ↓	0.0721	0.0728	0.6851	0.5201
CP to QN ↑	0.0583	0.0568	0.9580	0.9367
RN to QN ↑	0.0526	0.0509	0.9581	0.9371
	X29_P0	**X34_P0**	**X29_P0**	**X34_P0**
CP to QN ↓	0.0975	0.0955	0.4559	0.3544
CP to QN ↑	0.0765	0.0755	0.6355	0.6337
RN to QN ↑	0.0736	0.0732	0.6357	0.6336

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P0	X10_P0	X19_P0	X23_P0
CP ↓	min_pulse_width to CP	0.0549	0.0549	0.0549	0.0549
CP ↑	min_pulse_width to CP	0.0394	0.0394	0.0393	0.0393
D ↓	hold_rising to CP	-0.0289	-0.0289	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0072	-0.0072	-0.0072	-0.0072
D ↓	setup_rising to CP	0.0614	0.0614	0.0614	0.0614
D ↑	setup_rising to CP	0.0347	0.0347	0.0347	0.0347
E ↓	hold_rising to CP	-0.0283	-0.0283	-0.0283	-0.0283
E ↑	hold_rising to CP	-0.0098	-0.0098	-0.0066	-0.0066
E ↓	setup_rising to CP	0.0857	0.0857	0.0857	0.0857
E ↑	setup_rising to CP	0.0640	0.0640	0.0640	0.0640
RN ↓	min_pulse_width to RN	0.0447	0.0469	0.0518	0.0518
RN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
RN ↑	removal_rising to CP	0.0091	0.0091	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0110	-0.0110	-0.0110	-0.0110

TE ↑	hold_rising to CP	-0.0013	-0.0013	-0.0013	-0.0013
TE ↓	setup_rising to CP	0.0479	0.0479	0.0479	0.0479
TE ↑	setup_rising to CP	0.0591	0.0586	0.0586	0.0586
TI ↓	hold_rising to CP	-0.0280	-0.0280	-0.0280	-0.0280
TI ↑	hold_rising to CP	-0.0043	-0.0045	-0.0045	-0.0045
TI ↓	setup_rising to CP	0.0576	0.0576	0.0576	0.0576
TI ↑	setup_rising to CP	0.0293	0.0293	0.0293	0.0293
		X29_P0	X34_P0		
CP ↓	min_pulse_width to CP	0.0549	0.0549		
CP ↑	min_pulse_width to CP	0.0394	0.0394		
D ↓	hold_rising to CP	-0.0289	-0.0289		
D ↑	hold_rising to CP	-0.0072	-0.0072		
D ↓	setup_rising to CP	0.0614	0.0614		
D ↑	setup_rising to CP	0.0347	0.0347		
E ↓	hold_rising to CP	-0.0283	-0.0283		
E ↑	hold_rising to CP	-0.0098	-0.0066		
E ↓	setup_rising to CP	0.0857	0.0857		
E ↑	setup_rising to CP	0.0640	0.0640		
RN ↓	min_pulse_width to RN	0.0447	0.0447		
RN ↑	recovery_rising to CP	-0.0017	-0.0017		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0110	-0.0110		
TE ↑	hold_rising to CP	-0.0013	-0.0013		
TE ↓	setup_rising to CP	0.0479	0.0479		
TE ↑	setup_rising to CP	0.0591	0.0591		
TI ↓	hold_rising to CP	-0.0280	-0.0280		
TI ↑	hold_rising to CP	-0.0045	-0.0045		
TI ↓	setup_rising to CP	0.0576	0.0576		
TI ↑	setup_rising to CP	0.0293	0.0293		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	2.483e-05	1.000e-20
X10_P0	3.081e-05	1.000e-20
X19_P0	4.260e-05	1.000e-20
X23_P0	4.521e-05	1.000e-20

X29_P0	5.722e-05	1.000e-20
X34_P0	6.046e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

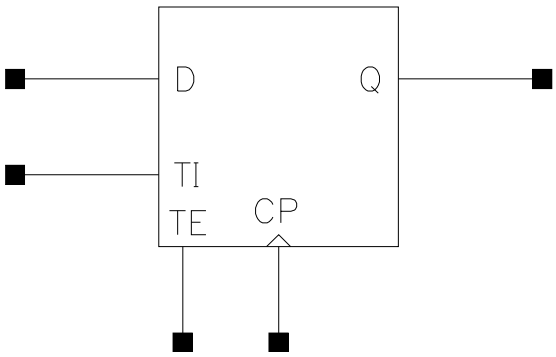
Pin Cycle	X5_P0	X10_P0	X19_P0	X23_P0
Clock 100Mhz Data 0Mhz	7.706e-03	7.714e-03	7.717e-03	7.717e-03
Clock 100Mhz Data 25Mhz	8.011e-03	8.369e-03	9.096e-03	9.165e-03
Clock 100Mhz Data 50Mhz	8.316e-03	9.023e-03	1.048e-02	1.061e-02
Clock = 0 Data 100Mhz	4.459e-03	4.458e-03	4.456e-03	4.455e-03
Clock = 1 Data 100Mhz	1.811e-03	1.809e-03	1.808e-03	1.808e-03
	X29_P0	X34_P0		
Clock 100Mhz Data 0Mhz	7.719e-03	7.719e-03		
Clock 100Mhz Data 25Mhz	9.851e-03	1.002e-02		
Clock 100Mhz Data 50Mhz	1.198e-02	1.233e-02		
Clock = 0 Data 100Mhz	4.455e-03	4.456e-03		
Clock = 1 Data 100Mhz	1.808e-03	1.809e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P0	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P0	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P0	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P0	C8T28SOI_LLHF_-SDFPQX3_P0	C8T28SOIDV_LL_-SDFPQX5_P0	C8T28SOIDV_LL_-SDFPQX10_P0
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P0	C8T28SOIDV_LL_-SDFPQX23_P0	C8T28SOIDV_LL_-SDFPQX29_P0	
CP	0.0005	0.0005	0.0005	
D	0.0005	0.0005	0.0005	
TE	0.0008	0.0008	0.0008	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P0	**C8T28SOI_LLHF_-SDFPQX3_P0**	**C8T28SOI_LL_-SDFPQX5_P0**	**C8T28SOI_LLHF_-SDFPQX3_P0**
CP to Q ↓	0.0443	0.0377	2.7847	4.2622
CP to Q ↑	0.0427	0.0488	3.7615	5.7291
	C8T28SOIDV_LL_-SDFPQX5_P0	**C8T28SOIDV_LL_-SDFPQX10_P0**	**C8T28SOIDV_LL_-SDFPQX5_P0**	**C8T28SOIDV_LL_-SDFPQX10_P0**
CP to Q ↓	0.0399	0.0554	2.6476	1.2938
CP to Q ↑	0.0493	0.0699	3.7233	1.8708
	C8T28SOIDV_LL_-SDFPQX19_P0	**C8T28SOIDV_LL_-SDFPQX23_P0**	**C8T28SOIDV_LL_-SDFPQX19_P0**	**C8T28SOIDV_LL_-SDFPQX23_P0**
CP to Q ↓	0.0598	0.0618	0.6726	0.5169
CP to Q ↑	0.0741	0.0758	0.9437	0.9364
	C8T28SOIDV_LL_-SDFPQX29_P0		**C8T28SOIDV_LL_-SDFPQX29_P0**	
CP to Q ↓	0.0589		0.4516	
CP to Q ↑	0.0708		0.6275	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P0	C8T28SOI_-LLHF_-SDFPQX3_P0	C8T28SOIDV_-LL_SDFPQX5_-P0	C8T28SOIDV_-LL_SDFPQX10_-P0
CP ↓	min_pulse_width to CP	0.0685	0.0681	0.0588	0.0575
CP ↑	min_pulse_width to CP	0.0362	0.0318	0.0362	0.0314
D ↓	hold_rising to CP	-0.0267	-0.0653	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0045	-0.0014	0.0058	0.0058
D ↓	setup_rising to CP	0.0581	0.0991	0.0370	0.0370
D ↑	setup_rising to CP	0.0294	0.0288	0.0191	0.0191
TE ↓	hold_rising to CP	-0.0165	-0.0181	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0023	-0.0014	-0.0023	-0.0023
TE ↓	setup_rising to CP	0.0565	0.0829	0.0345	0.0345
TE ↑	setup_rising to CP	0.0683	0.0927	0.0693	0.0667

TI ↓	hold_rising to CP	-0.0377	-0.0602	-0.0329	-0.0329
TI ↑	hold_rising to CP	-0.0043	0.0012	-0.0043	-0.0043
TI ↓	setup_rising to CP	0.0709	0.0944	0.0676	0.0683
TI ↑	setup_rising to CP	0.0291	0.0235	0.0291	0.0291
		C8T28SOIDV_-LL_SDFPQX19_-P0	C8T28SOIDV_-LL_SDFPQX23_-P0	C8T28SOIDV_-LL_SDFPQX29_-P0	
CP ↓	min_pulse_width to CP	0.0575	0.0575	0.0588	
CP ↑	min_pulse_width to CP	0.0314	0.0348	0.0348	
D ↓	hold_rising to CP	-0.0023	-0.0023	-0.0023	
D ↑	hold_rising to CP	0.0058	0.0058	0.0058	
D ↓	setup_rising to CP	0.0370	0.0370	0.0370	
D ↑	setup_rising to CP	0.0191	0.0191	0.0191	
TE ↓	hold_rising to CP	-0.0006	-0.0006	-0.0001	
TE ↑	hold_rising to CP	-0.0023	-0.0023	-0.0023	
TE ↓	setup_rising to CP	0.0345	0.0345	0.0345	
TE ↑	setup_rising to CP	0.0667	0.0667	0.0689	
TI ↓	hold_rising to CP	-0.0336	-0.0336	-0.0329	
TI ↑	hold_rising to CP	-0.0043	-0.0043	-0.0043	
TI ↓	setup_rising to CP	0.0683	0.0683	0.0676	
TI ↑	setup_rising to CP	0.0291	0.0291	0.0291	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P0	2.194e-05	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P0	1.799e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P0	2.055e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P0	2.968e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P0	3.806e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P0	4.061e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P0	5.242e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P0	C8T28SOI_LLHF_-SDFPQX3_P0	C8T28SOIDV_LL_-SDFPQX5_P0	C8T28SOIDV_LL_-SDFPQX10_P0
Clock 100Mhz Data 0Mhz	7.503e-03	7.190e-03	6.885e-03	6.729e-03
Clock 100Mhz Data 25Mhz	7.198e-03	6.900e-03	6.722e-03	7.013e-03
Clock 100Mhz Data 50Mhz	6.894e-03	6.611e-03	6.559e-03	7.298e-03

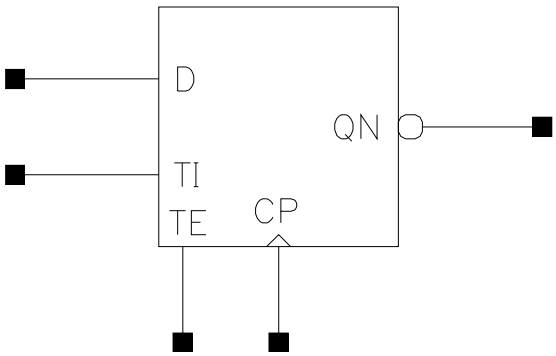
Clock = 0 Data 100Mhz	3.552e-03	3.725e-03	3.511e-03	3.401e-03
Clock = 1 Data 100Mhz	4.227e-05	4.853e-04	3.386e-04	2.653e-04
	C8T28SOIDV_LL_-SDFPQX19_P0	C8T28SOIDV_LL_-SDFPQX23_P0	C8T28SOIDV_LL_-SDFPQX29_P0	
Clock 100Mhz Data 0Mhz	6.637e-03	6.578e-03	6.536e-03	
Clock 100Mhz Data 25Mhz	7.510e-03	7.542e-03	8.050e-03	
Clock 100Mhz Data 50Mhz	8.383e-03	8.506e-03	9.564e-03	
Clock = 0 Data 100Mhz	3.333e-03	3.287e-03	3.257e-03	
Clock = 1 Data 100Mhz	2.214e-04	1.921e-04	1.712e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P0	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P0	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P0	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P0	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P0	C8T28SOI_LLHF_-SDFPQNX3_P0	C8T28SOIDV_LL_-SDFPQNX5_P0	C8T28SOIDV_LL_-SDFPQNX10_P0

CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P0	C8T28SOIDV_LL_-SDFPQNX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P0	**C8T28SOI_LLHF_-SDFPQNX3_P0**	**C8T28SOI_LL_-SDFPQNX5_P0**	**C8T28SOI_LLHF_-SDFPQNX3_P0**
CP to QN ↓	0.0546	0.0580	2.6897	4.0332
CP to QN ↑	0.0486	0.0462	4.0703	5.5793
	C8T28SOIDV_LL_-SDFPQNX5_P0	**C8T28SOIDV_LL_-SDFPQNX10_P0**	**C8T28SOIDV_LL_-SDFPQNX5_P0**	**C8T28SOIDV_LL_-SDFPQNX10_P0**
CP to QN ↓	0.0600	0.0570	2.6116	1.3041
CP to QN ↑	0.0454	0.0485	3.6812	1.8720
	C8T28SOIDV_LL_-SDFPQNX19_P0	**C8T28SOIDV_LL_-SDFPQNX29_P0**	**C8T28SOIDV_LL_-SDFPQNX19_P0**	**C8T28SOIDV_LL_-SDFPQNX29_P0**
CP to QN ↓	0.0636	0.0739	0.6788	0.4599
CP to QN ↑	0.0568	0.0639	0.9629	0.6315

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P0	C8T28SOI_-LLHF_-SDFPQNX3_P0	C8T28SOIDV_-LL_SDFPQNX5_-P0	C8T28SOIDV_-LL_-SDFPQNX10_P0
CP ↓	min_pulse_width to CP	0.0685	0.0668	0.0588	0.0575
CP ↑	min_pulse_width to CP	0.0315	0.0270	0.0315	0.0347
D ↓	hold_rising to CP	-0.0267	-0.0653	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0045	-0.0046	0.0058	0.0058
D ↓	setup_rising to CP	0.0581	0.0997	0.0370	0.0370
D ↑	setup_rising to CP	0.0294	0.0288	0.0191	0.0191
TE ↓	hold_rising to CP	-0.0165	-0.0181	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0023	-0.0018	0.0005	-0.0023
TE ↓	setup_rising to CP	0.0565	0.0771	0.0344	0.0345
TE ↑	setup_rising to CP	0.0683	0.0901	0.0693	0.0693
TI ↓	hold_rising to CP	-0.0377	-0.0602	-0.0329	-0.0329
TI ↑	hold_rising to CP	-0.0043	0.0012	0.0013	-0.0043
TI ↓	setup_rising to CP	0.0709	0.0901	0.0675	0.0676
TI ↑	setup_rising to CP	0.0291	0.0235	0.0250	0.0291

		C8T28SOIDV_-LL_-SDFPQNX19_P0	C8T28SOIDV_-LL_-SDFPQNX29_P0		
CP ↓	min_pulse_width to CP	0.0575	0.0575		
CP ↑	min_pulse_width to CP	0.0362	0.0314		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0058	0.0058		
D ↓	setup_rising to CP	0.0370	0.0370		
D ↑	setup_rising to CP	0.0191	0.0191		
TE ↓	hold_rising to CP	-0.0006	-0.0006		
TE ↑	hold_rising to CP	-0.0023	-0.0023		
TE ↓	setup_rising to CP	0.0345	0.0345		
TE ↑	setup_rising to CP	0.0693	0.0693		
TI ↓	hold_rising to CP	-0.0336	-0.0336		
TI ↑	hold_rising to CP	-0.0043	-0.0043		
TI ↓	setup_rising to CP	0.0676	0.0676		
TI ↑	setup_rising to CP	0.0291	0.0291		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P0	2.164e-05	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P0	1.820e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P0	2.076e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P0	2.927e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P0	3.831e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P0	6.343e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P0	C8T28SOI_LLHF_-SDFPQNX3_P0	C8T28SOIDV_LL_-SDFPQNX5_P0	C8T28SOIDV_LL_-SDFPQNX10_P0
Clock 100Mhz Data 0Mhz	7.502e-03	7.269e-03	6.945e-03	6.771e-03
Clock 100Mhz Data 25Mhz	7.139e-03	6.976e-03	6.687e-03	6.989e-03
Clock 100Mhz Data 50Mhz	6.777e-03	6.683e-03	6.430e-03	7.207e-03
Clock = 0 Data 100Mhz	3.553e-03	3.741e-03	3.527e-03	3.413e-03
Clock = 1 Data 100Mhz	4.232e-05	4.896e-04	3.416e-04	2.676e-04
	C8T28SOIDV_LL_-SDFPQNX19_P0	C8T28SOIDV_LL_-SDFPQNX29_P0		
Clock 100Mhz Data 0Mhz	6.671e-03	6.601e-03		

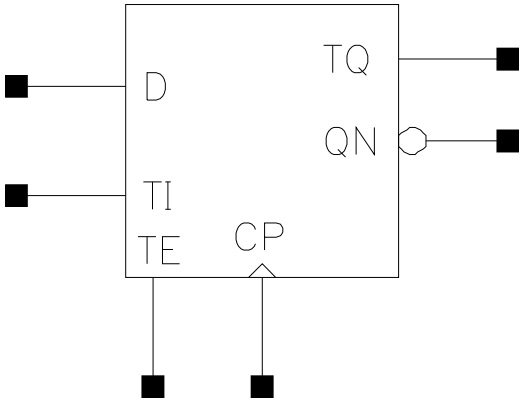
Clock 100Mhz Data 25Mhz	7.625e-03	8.511e-03		
Clock 100Mhz Data 50Mhz	8.580e-03	1.042e-02		
Clock = 0 Data 100Mhz	3.341e-03	3.297e-03		
Clock = 1 Data 100Mhz	2.232e-04	1.936e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P0	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P0	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P0	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P0	C8T28SOI_LLHF_-SDFPQNTX3_P0	C8T28SOIDV_LL_-SDFPQNTX5_P0	C8T28SOIDV_LL_-SDFPQNTX10_P0
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P0	C8T28SOIDV_LL_-SDFPQNTX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNTX5_P0	**C8T28SOI_LLHF_-SDFPQNTX3_P0**	**C8T28SOI_LL_-SDFPQNTX5_P0**	**C8T28SOI_LLHF_-SDFPQNTX3_P0**
CP to QN ↓	0.0615	0.0633	2.7958	4.1033
CP to QN ↑	0.0612	0.0562	4.0799	5.6088
CP to TQ ↓	0.0518	0.0398	7.2256	4.7567
CP to TQ ↑	0.0536	0.0480	18.5773	9.8434
	C8T28SOIDV_LL_-SDFPQNTX5_P0	**C8T28SOIDV_LL_-SDFPQNTX10_P0**	**C8T28SOIDV_LL_-SDFPQNTX5_P0**	**C8T28SOIDV_LL_-SDFPQNTX10_P0**
CP to QN ↓	0.0645	0.0629	2.5629	1.3104
CP to QN ↑	0.0529	0.0530	3.6849	1.8783
CP to TQ ↓	0.0375	0.0389	4.7666	4.9316
CP to TQ ↑	0.0492	0.0502	7.8850	8.1607
	C8T28SOIDV_LL_-SDFPQNTX19_P0	**C8T28SOIDV_LL_-SDFPQNTX29_P0**	**C8T28SOIDV_LL_-SDFPQNTX19_P0**	**C8T28SOIDV_LL_-SDFPQNTX29_P0**
CP to QN ↓	0.0647	0.0759	0.6759	0.4633
CP to QN ↑	0.0573	0.0679	0.9556	0.6303
CP to TQ ↓	0.0404	0.0393	4.8800	4.9700
CP to TQ ↑	0.0518	0.0520	8.4084	10.4454

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_P0	C8T28SOI_-LLHF_-SDFPQNTX3_P0	C8T28SOIDV_-LL_-SDFPQNTX5_P0	C8T28SOIDV_-LL_-SDFPQNTX10_-P0
CP ↓	min_pulse_width to CP	0.0685	0.0668	0.0588	0.0575
CP ↑	min_pulse_width to CP	0.0409	0.0364	0.0348	0.0362
D ↓	hold_rising to CP	-0.0267	-0.0653	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0045	-0.0046	0.0058	0.0058
D ↓	setup_rising to CP	0.0581	0.0997	0.0370	0.0370

D ↑	setup_rising to CP	0.0294	0.0288	0.0191	0.0191
TE ↓	hold_rising to CP	-0.0165	-0.0181	-0.0001	-0.0006
TE ↑	hold_rising to CP	-0.0023	-0.0013	0.0005	-0.0023
TE ↓	setup_rising to CP	0.0565	0.0771	0.0344	0.0345
TE ↑	setup_rising to CP	0.0683	0.0901	0.0689	0.0667
TI ↓	hold_rising to CP	-0.0377	-0.0605	-0.0329	-0.0336
TI ↑	hold_rising to CP	-0.0043	0.0014	0.0013	-0.0043
TI ↓	setup_rising to CP	0.0709	0.0901	0.0675	0.0676
TI ↑	setup_rising to CP	0.0291	0.0278	0.0250	0.0291
		C8T28SOIDV_-LL_-SDFPQNTX19_-P0	C8T28SOIDV_-LL_-SDFPQNTX29_-P0		
CP ↓	min_pulse_width to CP	0.0581	0.0575		
CP ↑	min_pulse_width to CP	0.0362	0.0347		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0058	0.0058		
D ↓	setup_rising to CP	0.0370	0.0370		
D ↑	setup_rising to CP	0.0191	0.0191		
TE ↓	hold_rising to CP	-0.0006	-0.0006		
TE ↑	hold_rising to CP	-0.0023	-0.0023		
TE ↓	setup_rising to CP	0.0345	0.0345		
TE ↑	setup_rising to CP	0.0693	0.0693		
TI ↓	hold_rising to CP	-0.0336	-0.0329		
TI ↑	hold_rising to CP	-0.0043	-0.0043		
TI ↓	setup_rising to CP	0.0676	0.0676		
TI ↑	setup_rising to CP	0.0291	0.0291		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P0	2.130e-05	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P0	1.930e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P0	2.202e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P0	2.704e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P0	3.777e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P0	6.210e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

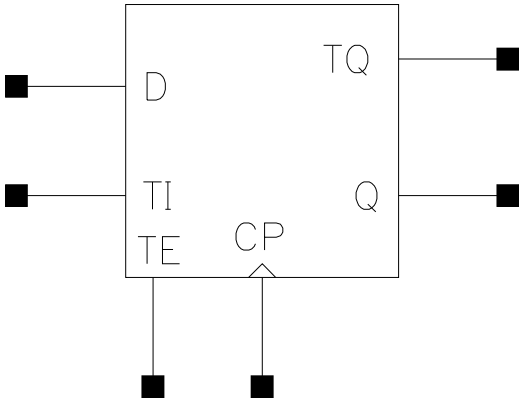
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P0	C8T28SOI_LLHF_-SDFPQNTX3_P0	C8T28SOIDV_LL_-SDFPQNTX5_P0	C8T28SOIDV_LL_-SDFPQNTX10_P0
Clock 100Mhz Data 0Mhz	7.510e-03	7.270e-03	6.943e-03	6.770e-03
Clock 100Mhz Data 25Mhz	7.433e-03	7.200e-03	6.904e-03	6.991e-03
Clock 100Mhz Data 50Mhz	7.356e-03	7.130e-03	6.865e-03	7.211e-03
Clock = 0 Data 100Mhz	3.553e-03	3.744e-03	3.529e-03	3.415e-03
Clock = 1 Data 100Mhz	4.210e-05	4.925e-04	3.436e-04	2.690e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P0	C8T28SOIDV_LL_-SDFPQNTX29_P0		
Clock 100Mhz Data 0Mhz	6.667e-03	6.595e-03		
Clock 100Mhz Data 25Mhz	7.556e-03	8.692e-03		
Clock 100Mhz Data 50Mhz	8.445e-03	1.079e-02		
Clock = 0 Data 100Mhz	3.346e-03	3.301e-03		
Clock = 1 Data 100Mhz	2.244e-04	1.946e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P0	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P0	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P0	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P0	C8T28SOI_LLHF_-SDFPQTX3_P0	C8T28SOIDV_LL_-SDFPQTX5_P0	C8T28SOIDV_LL_-SDFPQTX10_P0
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P0	C8T28SOIDV_LL_-SDFPQTX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQTX5_P0	**C8T28SOI_LLHF_-SDFPQTX3_P0**	**C8T28SOI_LL_-SDFPQTX5_P0**	**C8T28SOI_LLHF_-SDFPQTX3_P0**
CP to Q ↓	0.0518	0.0481	2.9478	4.4161
CP to Q ↑	0.0462	0.0491	3.7899	5.8303
CP to TQ ↓	0.0628	0.0470	7.9041	4.9017
CP to TQ ↑	0.0591	0.0518	18.8346	10.0125
	C8T28SOIDV_LL_-SDFPQTX5_P0	**C8T28SOIDV_LL_-SDFPQTX10_P0**	**C8T28SOIDV_LL_-SDFPQTX5_P0**	**C8T28SOIDV_LL_-SDFPQTX10_P0**
CP to Q ↓	0.0431	0.0567	2.7111	1.3001
CP to Q ↑	0.0509	0.0712	3.7800	1.8729
CP to TQ ↓	0.0429	0.0585	4.9117	4.9804
CP to TQ ↑	0.0524	0.0739	8.6310	8.4667
	C8T28SOIDV_LL_-SDFPQTX19_P0	**C8T28SOIDV_LL_-SDFPQTX29_P0**	**C8T28SOIDV_LL_-SDFPQTX19_P0**	**C8T28SOIDV_LL_-SDFPQTX29_P0**
CP to Q ↓	0.0611	0.0664	0.6744	0.4408
CP to Q ↑	0.0746	0.0740	0.9483	0.6245
CP to TQ ↓	0.0636	0.0416	5.0220	5.1254
CP to TQ ↑	0.0788	0.0533	8.4971	10.4609

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P0	C8T28SOI_-LLHF_-SDFPQTX3_P0	C8T28SOIDV_-LL_SDFPQTX5_-P0	C8T28SOIDV_-LL_-SDFPQTX10_P0
CP ↓	min_pulse_width to CP	0.0685	0.0668	0.0588	0.0575
CP ↑	min_pulse_width to CP	0.0456	0.0376	0.0362	0.0314
D ↓	hold_rising to CP	-0.0267	-0.0653	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0045	-0.0014	0.0058	0.0058
D ↓	setup_rising to CP	0.0581	0.0997	0.0370	0.0370

D ↑	setup_rising to CP	0.0294	0.0288	0.0191	0.0191
TE ↓	hold_rising to CP	-0.0165	-0.0181	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0023	-0.0018	-0.0023	-0.0023
TE ↓	setup_rising to CP	0.0565	0.0775	0.0345	0.0345
TE ↑	setup_rising to CP	0.0683	0.0901	0.0693	0.0693
TI ↓	hold_rising to CP	-0.0377	-0.0605	-0.0329	-0.0329
TI ↑	hold_rising to CP	-0.0043	0.0012	-0.0043	-0.0043
TI ↓	setup_rising to CP	0.0709	0.0901	0.0676	0.0683
TI ↑	setup_rising to CP	0.0291	0.0235	0.0291	0.0291
		C8T28SOIDV_-LL_-SDFPQTX19_P0	C8T28SOIDV_-LL_-SDFPQTX29_P0		
CP ↓	min_pulse_width to CP	0.0575	0.0588		
CP ↑	min_pulse_width to CP	0.0314	0.0394		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0058	0.0058		
D ↓	setup_rising to CP	0.0370	0.0370		
D ↑	setup_rising to CP	0.0191	0.0191		
TE ↓	hold_rising to CP	-0.0006	-0.0001		
TE ↑	hold_rising to CP	-0.0023	-0.0023		
TE ↓	setup_rising to CP	0.0345	0.0345		
TE ↑	setup_rising to CP	0.0667	0.0689		
TI ↓	hold_rising to CP	-0.0336	-0.0329		
TI ↑	hold_rising to CP	-0.0043	-0.0043		
TI ↓	setup_rising to CP	0.0683	0.0676		
TI ↑	setup_rising to CP	0.0291	0.0291		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P0	2.200e-05	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P0	1.929e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P0	2.187e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P0	3.095e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P0	3.932e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P0	5.433e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

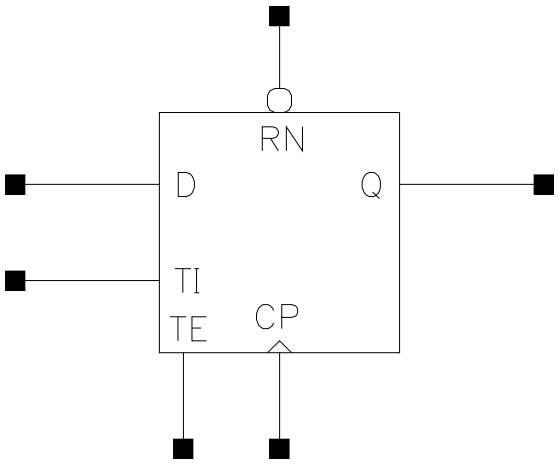
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P0	C8T28SOI_LLHF_-SDFPQTX3_P0	C8T28SOIDV_LL_-SDFPQTX5_P0	C8T28SOIDV_LL_-SDFPQTX10_P0
Clock 100Mhz Data 0Mhz	7.511e-03	7.278e-03	6.945e-03	6.774e-03
Clock 100Mhz Data 25Mhz	7.479e-03	7.221e-03	6.943e-03	7.203e-03
Clock 100Mhz Data 50Mhz	7.447e-03	7.164e-03	6.940e-03	7.633e-03
Clock = 0 Data 100Mhz	3.564e-03	3.746e-03	3.526e-03	3.412e-03
Clock = 1 Data 100Mhz	4.223e-05	4.895e-04	3.415e-04	2.675e-04
	C8T28SOIDV_LL_-SDFPQTX19_P0	C8T28SOIDV_LL_-SDFPQTX29_P0		
Clock 100Mhz Data 0Mhz	6.674e-03	6.612e-03		
Clock 100Mhz Data 25Mhz	7.729e-03	8.319e-03		
Clock 100Mhz Data 50Mhz	8.784e-03	1.003e-02		
Clock = 0 Data 100Mhz	3.342e-03	3.299e-03		
Clock = 1 Data 100Mhz	2.232e-04	1.937e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P0	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P0	C8T28SOI_LLHF_-SDFPRQX3_P0	C8T28SOIDV_LL_-SDFPRQX5_P0	C8T28SOIDV_LL_-SDFPRQX10_P0
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0009	0.0009
TE	0.0010	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P0	C8T28SOIDV_LL_-SDFPRQX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P0	**C8T28SOI_LLHF_-SDFPRQX3_P0**	**C8T28SOI_LL_-SDFPRQX5_P0**	**C8T28SOI_LLHF_-SDFPRQX3_P0**
CP to Q ↓	0.0504	0.0459	2.7978	4.2904
CP to Q ↑	0.0445	0.0490	3.7615	5.6688
RN to Q ↓	0.0455	0.0446	2.6175	4.0555
	C8T28SOIDV_LL_-SDFPRQX5_P0	**C8T28SOIDV_LL_-SDFPRQX10_P0**	**C8T28SOIDV_LL_-SDFPRQX5_P0**	**C8T28SOIDV_LL_-SDFPRQX10_P0**
CP to Q ↓	0.0404	0.0567	2.6435	1.3089
CP to Q ↑	0.0516	0.0727	3.7186	1.8764
RN to Q ↓	0.0375	0.0578	2.6194	1.3089
	C8T28SOIDV_LL_-SDFPRQX19_P0	**C8T28SOIDV_LL_-SDFPRQX29_P0**	**C8T28SOIDV_LL_-SDFPRQX19_P0**	**C8T28SOIDV_LL_-SDFPRQX29_P0**
CP to Q ↓	0.0605	0.0616	0.6736	0.4618
CP to Q ↑	0.0764	0.0792	0.9614	0.6552
RN to Q ↓	0.0618	0.0629	0.6737	0.4610

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P0	C8T28SOI_-LLHF_-SDFPRQX3_P0	C8T28SOIDV_-LL_SDFPRQX5_-P0	C8T28SOIDV_-LL_-SDFPRQX10_P0
CP ↓	min_pulse_width to CP	0.0685	0.0668	0.0589	0.0589
CP ↑	min_pulse_width to CP	0.0409	0.0364	0.0348	0.0348
D ↓	hold_rising to CP	-0.0267	-0.0594	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0045	-0.0046	0.0032	0.0032
D ↓	setup_rising to CP	0.0581	0.1001	0.0370	0.0370
D ↑	setup_rising to CP	0.0315	0.0347	0.0249	0.0249
RN ↓	min_pulse_width to RN	0.0474	0.0474	0.0447	0.0398
RN ↑	recovery_rising to CP	0.0028	0.0032	0.0032	0.0032
RN ↑	removal_rising to CP	0.0069	0.0069	0.0043	0.0043

TE ↓	hold_rising to CP	-0.0165	-0.0181	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0049	-0.0013	-0.0049	-0.0049
TE ↓	setup_rising to CP	0.0565	0.0781	0.0345	0.0345
TE ↑	setup_rising to CP	0.0683	0.0911	0.0667	0.0667
TI ↓	hold_rising to CP	-0.0377	-0.0596	-0.0277	-0.0277
TI ↑	hold_rising to CP	-0.0043	-0.0028	-0.0058	-0.0058
TI ↓	setup_rising to CP	0.0709	0.0909	0.0676	0.0676
TI ↑	setup_rising to CP	0.0299	0.0293	0.0299	0.0299
		C8T28SOIDV_-LL_-SDFPRQX19_P0	C8T28SOIDV_-LL_-SDFPRQX29_P0		
CP ↓	min_pulse_width to CP	0.0589	0.0589		
CP ↑	min_pulse_width to CP	0.0348	0.0348		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0032	0.0032		
D ↓	setup_rising to CP	0.0370	0.0370		
D ↑	setup_rising to CP	0.0249	0.0249		
RN ↓	min_pulse_width to RN	0.0398	0.0398		
RN ↑	recovery_rising to CP	0.0032	-0.0000		
RN ↑	removal_rising to CP	0.0043	0.0043		
TE ↓	hold_rising to CP	-0.0001	-0.0001		
TE ↑	hold_rising to CP	-0.0049	-0.0049		
TE ↓	setup_rising to CP	0.0345	0.0345		
TE ↑	setup_rising to CP	0.0667	0.0667		
TI ↓	hold_rising to CP	-0.0277	-0.0293		
TI ↑	hold_rising to CP	-0.0051	-0.0049		
TI ↓	setup_rising to CP	0.0676	0.0676		
TI ↑	setup_rising to CP	0.0299	0.0299		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P0	2.340e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P0	1.962e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P0	2.258e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P0	3.111e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX19_P0	4.153e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P0	5.367e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

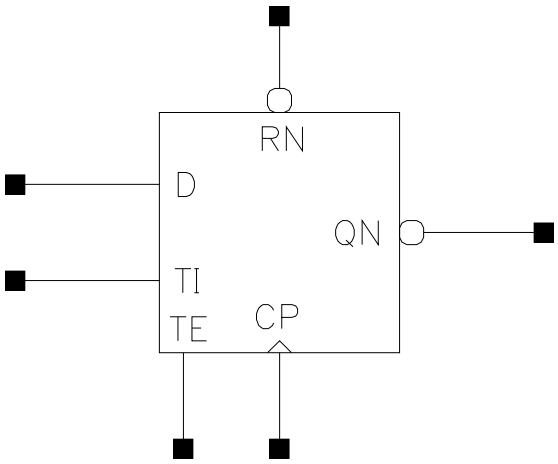
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P0	C8T28SOI_LLHF_-SDFPRQX3_P0	C8T28SOIDV_LL_-SDFPRQX5_P0	C8T28SOIDV_LL_-SDFPRQX10_P0
Clock 100Mhz Data 0Mhz	7.791e-03	7.483e-03	7.137e-03	6.964e-03
Clock 100Mhz Data 25Mhz	7.467e-03	7.206e-03	6.893e-03	7.217e-03
Clock 100Mhz Data 50Mhz	7.143e-03	6.930e-03	6.650e-03	7.469e-03
Clock = 0 Data 100Mhz	3.393e-03	3.606e-03	3.458e-03	3.384e-03
Clock = 1 Data 100Mhz	4.193e-05	4.928e-04	3.432e-04	2.684e-04
	C8T28SOIDV_LL_-SDFPRQX19_P0	C8T28SOIDV_LL_-SDFPRQX29_P0		
Clock 100Mhz Data 0Mhz	6.860e-03	6.793e-03		
Clock 100Mhz Data 25Mhz	7.704e-03	8.411e-03		
Clock 100Mhz Data 50Mhz	8.548e-03	1.003e-02		
Clock = 0 Data 100Mhz	3.340e-03	3.313e-03		
Clock = 1 Data 100Mhz	2.236e-04	1.938e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P0	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P0	C8T28SOI_LLHF_-SDFPRQNX3_P0	C8T28SOIDV_LL_-SDFPRQNX5_P0	C8T28SOIDV_LL_-SDFPRQNX10_P0
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P0	C8T28SOIDV_LL_-SDFPRQNX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0007	0.0007		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPRQNX5_P0	**C8T28SOI_LLHF_-SDFPRQNX3_P0**	**C8T28SOI_LL_-SDFPRQNX5_P0**	**C8T28SOI_LLHF_-SDFPRQNX3_P0**
CP to QN ↓	0.0576	0.0609	2.7584	4.0457
CP to QN ↑	0.0538	0.0504	3.8882	5.5769
RN to QN ↑	0.0533	0.0523	3.8824	5.5699
	C8T28SOIDV_LL_-SDFPRQNX5_P0	**C8T28SOIDV_LL_-SDFPRQNX10_P0**	**C8T28SOIDV_LL_-SDFPRQNX5_P0**	**C8T28SOIDV_LL_-SDFPRQNX10_P0**
CP to QN ↓	0.0651	0.0594	2.5522	1.3087
CP to QN ↑	0.0504	0.0491	3.6812	1.8761
RN to QN ↑	0.0509	0.0464	3.6684	1.8772
	C8T28SOIDV_LL_-SDFPRQNX19_P0	**C8T28SOIDV_LL_-SDFPRQNX29_P0**	**C8T28SOIDV_LL_-SDFPRQNX19_P0**	**C8T28SOIDV_LL_-SDFPRQNX29_P0**
CP to QN ↓	0.0660	0.0705	0.6901	0.4638
CP to QN ↑	0.0544	0.0608	0.9676	0.6520
RN to QN ↑	0.0503	0.0579	0.9661	0.6525

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P0	C8T28SOI_-LLHF_-SDFPRQNX3_-P0	C8T28SOIDV_-LL_-SDFPRQNX5_-P0	C8T28SOIDV_-LL_-SDFPRQNX10_-P0
CP ↓	min_pulse_width to CP	0.0685	0.0668	0.0589	0.0589
CP ↑	min_pulse_width to CP	0.0362	0.0317	0.0348	0.0348
D ↓	hold_rising to CP	-0.0267	-0.0599	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0045	-0.0041	0.0058	0.0058
D ↓	setup_rising to CP	0.0581	0.0942	0.0370	0.0370
D ↑	setup_rising to CP	0.0315	0.0347	0.0249	0.0249
RN ↓	min_pulse_width to RN	0.0474	0.0452	0.0398	0.0469
RN ↑	recovery_rising to CP	0.0032	0.0032	0.0032	0.0032

RN ↑	removal_rising to CP	0.0069	0.0042	0.0043	0.0043
TE ↓	hold_rising to CP	-0.0165	-0.0213	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0049	-0.0013	-0.0049	-0.0049
TE ↓	setup_rising to CP	0.0565	0.0781	0.0345	0.0345
TE ↑	setup_rising to CP	0.0683	0.0911	0.0667	0.0667
TI ↓	hold_rising to CP	-0.0377	-0.0596	-0.0277	-0.0277
TI ↑	hold_rising to CP	-0.0043	-0.0028	-0.0058	-0.0058
TI ↓	setup_rising to CP	0.0709	0.0909	0.0676	0.0676
TI ↑	setup_rising to CP	0.0299	0.0286	0.0299	0.0299
		C8T28SOIDV_-LL_-SDFPRQNX19_-P0	C8T28SOIDV_-LL_-SDFPRQNX29_-P0		
CP ↓	min_pulse_width to CP	0.0588	0.0605		
CP ↑	min_pulse_width to CP	0.0361	0.0407		
D ↓	hold_rising to CP	-0.0023	-0.0028		
D ↑	hold_rising to CP	0.0058	0.0058		
D ↓	setup_rising to CP	0.0370	0.0370		
D ↑	setup_rising to CP	0.0249	0.0249		
RN ↓	min_pulse_width to RN	0.0469	0.0588		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0043	0.0043		
TE ↓	hold_rising to CP	0.0026	0.0026		
TE ↑	hold_rising to CP	-0.0049	-0.0049		
TE ↓	setup_rising to CP	0.0345	0.0345		
TE ↑	setup_rising to CP	0.0667	0.0667		
TI ↓	hold_rising to CP	-0.0280	-0.0280		
TI ↑	hold_rising to CP	-0.0058	-0.0058		
TI ↓	setup_rising to CP	0.0676	0.0676		
TI ↑	setup_rising to CP	0.0299	0.0299		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P0	2.176e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P0	1.916e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P0	2.096e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P0	2.967e-05	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P0	3.570e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P0	4.715e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

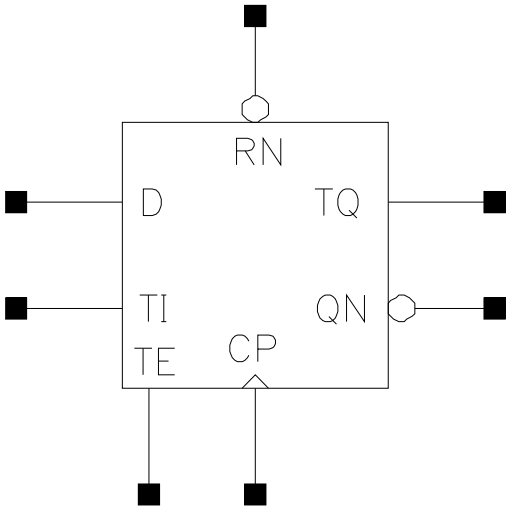
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P0	C8T28SOI_LLHF_-SDFPRQNX3_P0	C8T28SOIDV_LL_-SDFPRQNX5_P0	C8T28SOIDV_LL_-SDFPRQNX10_P0
Clock 100Mhz Data 0Mhz	7.786e-03	7.464e-03	7.126e-03	6.956e-03
Clock 100Mhz Data 25Mhz	7.393e-03	7.159e-03	6.916e-03	7.199e-03
Clock 100Mhz Data 50Mhz	7.000e-03	6.853e-03	6.706e-03	7.442e-03
Clock = 0 Data 100Mhz	3.391e-03	3.602e-03	3.459e-03	3.384e-03
Clock = 1 Data 100Mhz	4.195e-05	4.920e-04	3.427e-04	2.680e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P0	C8T28SOIDV_LL_-SDFPRQNX29_P0		
Clock 100Mhz Data 0Mhz	6.907e-03	6.897e-03		
Clock 100Mhz Data 25Mhz	7.763e-03	8.653e-03		
Clock 100Mhz Data 50Mhz	8.619e-03	1.041e-02		
Clock = 0 Data 100Mhz	3.338e-03	3.308e-03		
Clock = 1 Data 100Mhz	2.233e-04	1.935e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P0	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P0	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P0	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P0	C8T28SOI_LLHF_-SDFPRQNTX3_P0	C8T28SOIDV_LL_-SDFPRQNTX5_P0	C8T28SOIDV_LL_-SDFPRQNTX10_P0
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0008	0.0009
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P0	C8T28SOIDV_LL_-SDFPRQNTX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0007	0.0007		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNTX5_P0	**C8T28SOI_LLHF_-SDFPRQNTX3_P0**	**C8T28SOI_LL_-SDFPRQNTX5_P0**	**C8T28SOI_LLHF_-SDFPRQNTX3_P0**
CP to QN ↓	0.0638	0.0662	2.7185	4.0958
CP to QN ↑	0.0664	0.0610	4.0826	5.6131
CP to TQ ↓	0.0575	0.0443	7.5342	4.7925
CP to TQ ↑	0.0548	0.0506	18.5846	9.8599
RN to QN ↑	0.0582	0.0564	4.0802	5.6285
RN to TQ ↓	0.0506	0.0441	7.3245	4.6078
	C8T28SOIDV_LL_-SDFPRQNTX5_P0	**C8T28SOIDV_LL_-SDFPRQNTX10_P0**	**C8T28SOIDV_LL_-SDFPRQNTX5_P0**	**C8T28SOIDV_LL_-SDFPRQNTX10_P0**
CP to QN ↓	0.0684	0.0722	2.5907	1.3421
CP to QN ↑	0.0548	0.0579	3.6706	1.8683
CP to TQ ↓	0.0385	0.0391	4.7778	4.8142
CP to TQ ↑	0.0521	0.0521	7.8902	7.8949
RN to QN ↑	0.0518	0.0552	3.6751	1.8663
RN to TQ ↓	0.0346	0.0354	4.7789	4.8109
	C8T28SOIDV_LL_-SDFPRQNTX19_P0	**C8T28SOIDV_LL_-SDFPRQNTX29_P0**	**C8T28SOIDV_LL_-SDFPRQNTX19_P0**	**C8T28SOIDV_LL_-SDFPRQNTX29_P0**
CP to QN ↓	0.0690	0.0704	0.6779	0.4643
CP to QN ↑	0.0592	0.0655	0.9469	0.6461
CP to TQ ↓	0.0419	0.0504	4.8526	5.4495
CP to TQ ↑	0.0554	0.0613	7.9171	8.9464
RN to QN ↑	0.0549	0.0617	0.9448	0.6453
RN to TQ ↓	0.0368	0.0461	4.8387	5.3566

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P0	C8T28SOI_-LLHF_-SDFPRQNTX3_-P0	C8T28SOIDV_-LL_-SDFPRQNTX5_-P0	C8T28SOIDV_-LL_SDF-PRQNTX10_P0
CP ↓	min_pulse_width to CP	0.0685	0.0668	0.0589	0.0589
CP ↑	min_pulse_width to CP	0.0421	0.0363	0.0362	0.0362
D ↓	hold_rising to CP	-0.0267	-0.0594	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0045	-0.0041	0.0058	0.0032
D ↓	setup_rising to CP	0.0587	0.0975	0.0370	0.0370
D ↑	setup_rising to CP	0.0315	0.0347	0.0249	0.0249
RN ↓	min_pulse_width to RN	0.0496	0.0496	0.0469	0.0496
RN ↑	recovery_rising to CP	0.0028	0.0032	0.0032	0.0032
RN ↑	removal_rising to CP	0.0042	0.0042	0.0043	0.0043
TE ↓	hold_rising to CP	-0.0165	-0.0213	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0049	-0.0013	-0.0049	-0.0049
TE ↓	setup_rising to CP	0.0565	0.0781	0.0345	0.0345
TE ↑	setup_rising to CP	0.0689	0.0911	0.0667	0.0667
TI ↓	hold_rising to CP	-0.0377	-0.0596	-0.0293	-0.0277
TI ↑	hold_rising to CP	-0.0043	-0.0028	-0.0058	-0.0058
TI ↓	setup_rising to CP	0.0709	0.0909	0.0676	0.0676
TI ↑	setup_rising to CP	0.0299	0.0286	0.0299	0.0299
		C8T28SOIDV_-LL_SDF-PRQNTX19_P0	C8T28SOIDV_-LL_SDF-PRQNTX29_P0		
CP ↓	min_pulse_width to CP	0.0588	0.0588		
CP ↑	min_pulse_width to CP	0.0394	0.0454		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0058	0.0058		
D ↓	setup_rising to CP	0.0370	0.0370		
D ↑	setup_rising to CP	0.0249	0.0249		
RN ↓	min_pulse_width to RN	0.0518	0.0610		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0043	0.0043		
TE ↓	hold_rising to CP	0.0026	0.0026		
TE ↑	hold_rising to CP	-0.0049	-0.0049		

TE ↓	setup_rising to CP	0.0345	0.0345		
TE ↑	setup_rising to CP	0.0667	0.0667		
TI ↓	hold_rising to CP	-0.0280	-0.0280		
TI ↑	hold_rising to CP	-0.0058	-0.0058		
TI ↓	setup_rising to CP	0.0676	0.0676		
TI ↑	setup_rising to CP	0.0299	0.0299		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P0	2.143e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P0	2.020e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P0	2.250e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_P0	2.550e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_P0	3.543e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_P0	4.834e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

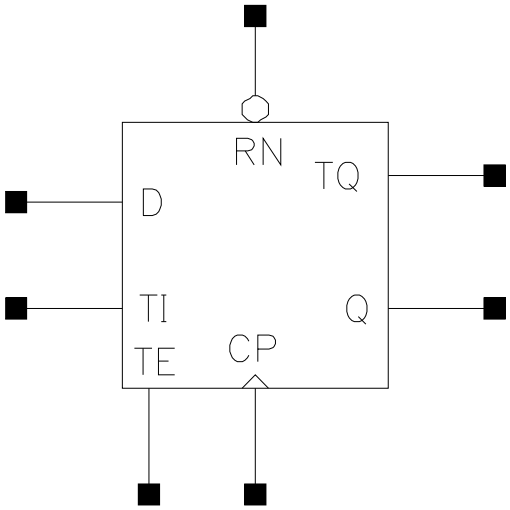
Pin Cycle	C8T28SOI_LL_SDFPRQNTX5_P0	C8T28SOI_LLHF_SDFPRQNTX3_P0	C8T28SOIDV_LL_SDFPRQNTX5_P0	C8T28SOIDV_LL_SDFPRQNTX10_P0
Clock 100Mhz Data 0Mhz	7.795e-03	7.469e-03	7.140e-03	6.967e-03
Clock 100Mhz Data 25Mhz	7.665e-03	7.387e-03	7.102e-03	7.245e-03
Clock 100Mhz Data 50Mhz	7.536e-03	7.305e-03	7.065e-03	7.523e-03
Clock = 0 Data 100Mhz	3.374e-03	3.599e-03	3.460e-03	3.386e-03
Clock = 1 Data 100Mhz	4.183e-05	4.948e-04	3.446e-04	2.695e-04
	C8T28SOIDV_LL_SDFPRQNTX19_P0	C8T28SOIDV_LL_SDFPRQNTX29_P0		
Clock 100Mhz Data 0Mhz	6.918e-03	6.876e-03		
Clock 100Mhz Data 25Mhz	7.778e-03	8.822e-03		
Clock 100Mhz Data 50Mhz	8.638e-03	1.077e-02		
Clock = 0 Data 100Mhz	3.341e-03	3.312e-03		
Clock = 1 Data 100Mhz	2.245e-04	1.945e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P0	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P0	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P0	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P0	C8T28SOI_LLHF_-SDFPRQTX3_P0	C8T28SOIDV_LL_-SDFPRQTX5_P0	C8T28SOIDV_LL_-SDFPRQTX10_P0
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0007	0.0009	0.0008
TE	0.0010	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P0	C8T28SOIDV_LL_-SDFPRQTX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQTX5_P0	**C8T28SOI_LLHF_-SDFPRQTX3_P0**	**C8T28SOI_LL_-SDFPRQTX5_P0**	**C8T28SOI_LLHF_-SDFPRQTX3_P0**
CP to Q ↓	0.0584	0.0511	2.9880	4.4381
CP to Q ↑	0.0478	0.0511	3.7959	5.8382
CP to TQ ↓	0.0697	0.0498	7.9591	4.9282
CP to TQ ↑	0.0604	0.0536	18.6075	10.0229
RN to Q ↓	0.0479	0.0468	2.7596	4.1815
RN to TQ ↓	0.0553	0.0465	7.6931	4.7137
	C8T28SOIDV_LL_-SDFPRQTX5_P0	**C8T28SOIDV_LL_-SDFPRQTX10_P0**	**C8T28SOIDV_LL_-SDFPRQTX5_P0**	**C8T28SOIDV_LL_-SDFPRQTX10_P0**
CP to Q ↓	0.0436	0.0578	2.7337	1.3313
CP to Q ↑	0.0533	0.0739	3.7598	1.8712
CP to TQ ↓	0.0439	0.0599	4.9134	4.8206
CP to TQ ↑	0.0550	0.0768	8.0283	7.9721
RN to Q ↓	0.0412	0.0594	2.6946	1.3319
RN to TQ ↓	0.0414	0.0615	4.8709	4.8194
	C8T28SOIDV_LL_-SDFPRQTX19_P0	**C8T28SOIDV_LL_-SDFPRQTX29_P0**	**C8T28SOIDV_LL_-SDFPRQTX19_P0**	**C8T28SOIDV_LL_-SDFPRQTX29_P0**
CP to Q ↓	0.0643	0.0618	0.7002	0.4706
CP to Q ↑	0.0788	0.0791	0.9527	0.6505
CP to TQ ↓	0.0672	0.0635	4.8678	4.7317
CP to TQ ↑	0.0830	0.0828	7.9706	8.1171
RN to Q ↓	0.0652	0.0631	0.6997	0.4702
RN to TQ ↓	0.0681	0.0648	4.8674	4.7307

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_P0	C8T28SOI_-LLHF_-SDFPRQTX3_P0	C8T28SOIDV_-LL_-SDFPRQTX5_P0	C8T28SOIDV_-LL_-SDFPRQTX10_-P0
CP ↓	min_pulse_width to CP	0.0685	0.0668	0.0589	0.0589
CP ↑	min_pulse_width to CP	0.0502	0.0411	0.0362	0.0348
D ↓	hold_rising to CP	-0.0267	-0.0594	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0045	-0.0041	0.0032	0.0032
D ↓	setup_rising to CP	0.0587	0.0975	0.0370	0.0370
D ↑	setup_rising to CP	0.0315	0.0343	0.0249	0.0249
RN ↓	min_pulse_width to RN	0.0540	0.0496	0.0496	0.0398
RN ↑	recovery_rising to CP	0.0028	0.0032	0.0032	-0.0000
RN ↑	removal_rising to CP	0.0069	0.0042	0.0043	0.0043
TE ↓	hold_rising to CP	-0.0165	-0.0213	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0049	-0.0013	-0.0049	-0.0049
TE ↓	setup_rising to CP	0.0565	0.0781	0.0345	0.0345
TE ↑	setup_rising to CP	0.0683	0.0911	0.0667	0.0667
TI ↓	hold_rising to CP	-0.0377	-0.0596	-0.0277	-0.0277
TI ↑	hold_rising to CP	-0.0043	-0.0028	-0.0058	-0.0051
TI ↓	setup_rising to CP	0.0709	0.0909	0.0676	0.0676
TI ↑	setup_rising to CP	0.0299	0.0286	0.0299	0.0299
		C8T28SOIDV_-LL_-SDFPRQTX19_-P0	C8T28SOIDV_-LL_-SDFPRQTX29_-P0		
CP ↓	min_pulse_width to CP	0.0589	0.0589		
CP ↑	min_pulse_width to CP	0.0348	0.0348		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0032	0.0032		
D ↓	setup_rising to CP	0.0370	0.0370		
D ↑	setup_rising to CP	0.0249	0.0249		
RN ↓	min_pulse_width to RN	0.0398	0.0398		
RN ↑	recovery_rising to CP	0.0032	0.0032		
RN ↑	removal_rising to CP	0.0043	0.0043		
TE ↓	hold_rising to CP	-0.0001	-0.0001		
TE ↑	hold_rising to CP	-0.0049	-0.0049		

TE ↓	setup_rising to CP	0.0345	0.0345		
TE ↑	setup_rising to CP	0.0667	0.0667		
TI ↓	hold_rising to CP	-0.0277	-0.0293		
TI ↑	hold_rising to CP	-0.0051	-0.0049		
TI ↓	setup_rising to CP	0.0676	0.0676		
TI ↑	setup_rising to CP	0.0299	0.0299		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P0	2.353e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P0	2.075e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P0	2.415e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P0	3.189e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P0	4.118e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P0	5.429e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

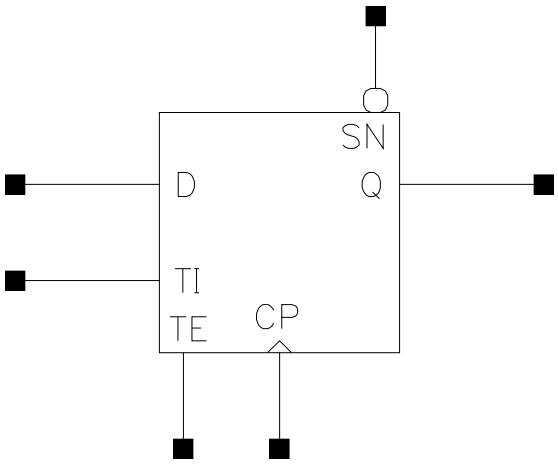
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P0	C8T28SOI_LLHF_-SDFPRQTX3_P0	C8T28SOIDV_LL_-SDFPRQTX5_P0	C8T28SOIDV_LL_-SDFPRQTX10_P0
Clock 100Mhz Data 0Mhz	7.796e-03	7.475e-03	7.133e-03	6.962e-03
Clock 100Mhz Data 25Mhz	7.741e-03	7.395e-03	7.072e-03	7.415e-03
Clock 100Mhz Data 50Mhz	7.686e-03	7.315e-03	7.010e-03	7.867e-03
Clock = 0 Data 100Mhz	3.381e-03	3.602e-03	3.457e-03	3.384e-03
Clock = 1 Data 100Mhz	4.189e-05	4.958e-04	3.452e-04	2.700e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P0	C8T28SOIDV_LL_-SDFPRQTX29_P0		
Clock 100Mhz Data 0Mhz	6.860e-03	6.792e-03		
Clock 100Mhz Data 25Mhz	7.917e-03	8.490e-03		
Clock 100Mhz Data 50Mhz	8.974e-03	1.019e-02		
Clock = 0 Data 100Mhz	3.341e-03	3.313e-03		
Clock = 1 Data 100Mhz	2.249e-04	1.949e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P0	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P0	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P0	C8T28SOI_LLHF_-SDFPSQX3_P0	C8T28SOIDV_LL_-SDFPSQX5_P0	C8T28SOIDV_LL_-SDFPSQX10_P0
CP	0.0007	0.0006	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0012	0.0013	0.0009	0.0010
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQX14_P0	C8T28SOIDV_LL_-SDFPSQX19_P0	C8T28SOIDV_LL_-SDFPSQX29_P0	
CP	0.0005	0.0005	0.0005	
D	0.0003	0.0003	0.0003	
SN	0.0010	0.0010	0.0010	
TE	0.0009	0.0009	0.0009	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P0	**C8T28SOI_LLHF_-SDFPSQX3_P0**	**C8T28SOI_LL_-SDFPSQX5_P0**	**C8T28SOI_LLHF_-SDFPSQX3_P0**
CP to Q ↓	0.0524	0.0466	2.8605	4.3617
CP to Q ↑	0.0458	0.0500	3.7932	5.6834
SN to Q ↑	0.0379	0.0349	3.7416	5.6273
	C8T28SOIDV_LL_-SDFPSQX5_P0	**C8T28SOIDV_LL_-SDFPSQX10_P0**	**C8T28SOIDV_LL_-SDFPSQX5_P0**	**C8T28SOIDV_LL_-SDFPSQX10_P0**
CP to Q ↓	0.0398	0.0572	2.6392	1.2790
CP to Q ↑	0.0490	0.0775	3.7191	1.8624
SN to Q ↑	0.0346	0.0612	3.7071	1.8614
	C8T28SOIDV_LL_-SDFPSQX14_P0	**C8T28SOIDV_LL_-SDFPSQX19_P0**	**C8T28SOIDV_LL_-SDFPSQX14_P0**	**C8T28SOIDV_LL_-SDFPSQX19_P0**
CP to Q ↓	0.0574	0.0609	0.8781	0.6773
CP to Q ↑	0.0773	0.0802	1.2531	0.9444
SN to Q ↑	0.0607	0.0636	1.2530	0.9440
	C8T28SOIDV_LL_-SDFPSQX29_P0		**C8T28SOIDV_LL_-SDFPSQX29_P0**	
CP to Q ↓	0.0607		0.4596	
CP to Q ↑	0.0832		0.6270	
SN to Q ↑	0.0667		0.6266	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P0	C8T28SOI_-LLHF_-SDFPSQX3_P0	C8T28SOIDV_-LL_SDFPSQX5_-P0	C8T28SOIDV_-LL_-SDFPSQX10_P0
CP ↓	min_pulse_width to CP	0.0767	0.0763	0.0629	0.0654
CP ↑	min_pulse_width to CP	0.0456	0.0364	0.0362	0.0314
D ↓	hold_rising to CP	-0.0316	-0.0701	-0.0072	-0.0120
D ↑	hold_rising to CP	-0.0017	0.0008	0.0032	0.0032
D ↓	setup_rising to CP	0.0662	0.1094	0.0467	0.0489
D ↑	setup_rising to CP	0.0294	0.0288	0.0249	0.0249

SN ↓	min_pulse_width to SN	0.0376	0.0332	0.0332	0.0354
SN ↑	recovery_rising to CP	0.0031	0.0031	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0163	0.0212	0.0260	0.0260
TE ↓	hold_rising to CP	-0.0165	-0.0181	-0.0050	-0.0072
TE ↑	hold_rising to CP	0.0009	-0.0018	0.0058	0.0005
TE ↓	setup_rising to CP	0.0608	0.0878	0.0451	0.0468
TE ↑	setup_rising to CP	0.0764	0.1008	0.0689	0.0689
TI ↓	hold_rising to CP	-0.0426	-0.0661	-0.0329	-0.0277
TI ↑	hold_rising to CP	-0.0000	0.0012	0.0061	-0.0000
TI ↓	setup_rising to CP	0.0773	0.1006	0.0675	0.0676
TI ↑	setup_rising to CP	0.0291	0.0235	0.0229	0.0293
		C8T28SOIDV_-LL_-SDFPSQX14_P0	C8T28SOIDV_-LL_-SDFPSQX19_P0	C8T28SOIDV_-LL_-SDFPSQX29_P0	
CP ↓	min_pulse_width to CP	0.0654	0.0654	0.0654	
CP ↑	min_pulse_width to CP	0.0314	0.0314	0.0348	
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120	
D ↑	hold_rising to CP	0.0032	0.0032	0.0032	
D ↓	setup_rising to CP	0.0489	0.0489	0.0489	
D ↑	setup_rising to CP	0.0249	0.0249	0.0249	
SN ↓	min_pulse_width to SN	0.0332	0.0332	0.0354	
SN ↑	recovery_rising to CP	-0.0049	-0.0049	-0.0017	
SN ↑	removal_rising to CP	0.0260	0.0260	0.0260	
TE ↓	hold_rising to CP	-0.0072	-0.0072	-0.0072	
TE ↑	hold_rising to CP	0.0005	0.0005	0.0005	
TE ↓	setup_rising to CP	0.0468	0.0468	0.0468	
TE ↑	setup_rising to CP	0.0689	0.0689	0.0689	
TI ↓	hold_rising to CP	-0.0277	-0.0280	-0.0277	
TI ↑	hold_rising to CP	-0.0000	-0.0000	-0.0000	
TI ↓	setup_rising to CP	0.0676	0.0676	0.0676	
TI ↑	setup_rising to CP	0.0293	0.0293	0.0293	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQX5_P0	2.295e-05	1.000e-20

C8T28SOI_LLHF_SDFPSQX3_P0	2.021e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P0	2.181e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P0	3.064e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P0	3.561e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P0	4.080e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P0	5.171e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

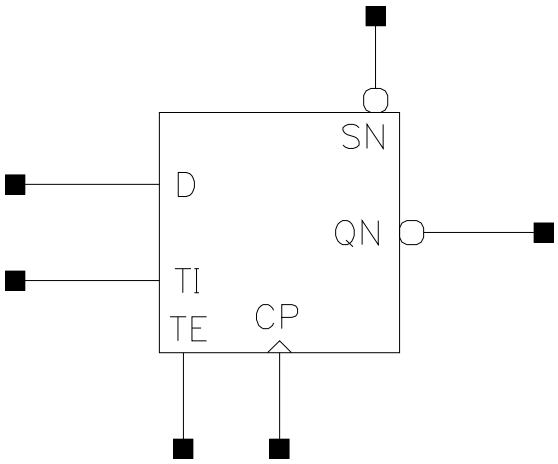
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P0	C8T28SOI_LLHF_-SDFPSQX3_P0	C8T28SOIDV_LL_-SDFPSQX5_P0	C8T28SOIDV_LL_-SDFPSQX10_P0
Clock 100Mhz Data 0Mhz	7.675e-03	7.277e-03	6.961e-03	6.804e-03
Clock 100Mhz Data 25Mhz	7.521e-03	7.105e-03	6.739e-03	7.178e-03
Clock 100Mhz Data 50Mhz	7.368e-03	6.933e-03	6.518e-03	7.552e-03
Clock = 0 Data 100Mhz	3.493e-03	3.706e-03	3.586e-03	3.553e-03
Clock = 1 Data 100Mhz	4.192e-05	4.908e-04	3.421e-04	2.683e-04
	C8T28SOIDV_LL_-SDFPSQX14_P0	C8T28SOIDV_LL_-SDFPSQX19_P0	C8T28SOIDV_LL_-SDFPSQX29_P0	
Clock 100Mhz Data 0Mhz	6.709e-03	6.647e-03	6.602e-03	
Clock 100Mhz Data 25Mhz	7.322e-03	7.688e-03	8.176e-03	
Clock 100Mhz Data 50Mhz	7.935e-03	8.728e-03	9.751e-03	
Clock = 0 Data 100Mhz	3.533e-03	3.519e-03	3.510e-03	
Clock = 1 Data 100Mhz	2.240e-04	1.944e-04	1.734e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P0	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P0	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P0	C8T28SOI_LLHF_-SDFPSQNX3_P0	C8T28SOIDV_LL_-SDFPSQNX5_P0	C8T28SOIDV_LL_-SDFPSQNX10_P0
CP	0.0007	0.0006	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0012	0.0013	0.0009	0.0010
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNX14_P0	C8T28SOIDV_LL_-SDFPSQNX19_P0	C8T28SOIDV_LL_-SDFPSQNX23_P0	C8T28SOIDV_LL_-SDFPSQNX29_P0
CP	0.0005	0.0005	0.0005	0.0005
D	0.0003	0.0003	0.0003	0.0003
SN	0.0010	0.0010	0.0010	0.0009
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPSQNX5_P0	**C8T28SOI_LLHF_-SDFPSQNX3_P0**	**C8T28SOI_LL_-SDFPSQNX5_P0**	**C8T28SOI_LLHF_-SDFPSQNX3_P0**
CP to QN ↓	0.0607	0.0611	2.8388	4.0301
CP to QN ↑	0.0572	0.0527	3.9537	5.5796
SN to QN ↓	0.0537	0.0465	2.8409	4.0263
	C8T28SOIDV_LL_-SDFPSQNX5_P0	**C8T28SOIDV_LL_-SDFPSQNX10_P0**	**C8T28SOIDV_LL_-SDFPSQNX5_P0**	**C8T28SOIDV_LL_-SDFPSQNX10_P0**
CP to QN ↓	0.0649	0.0611	2.5425	1.2926
CP to QN ↑	0.0529	0.0534	3.6804	1.8446
SN to QN ↓	0.0499	0.0448	2.5395	1.2921
	C8T28SOIDV_LL_-SDFPSQNX14_P0	**C8T28SOIDV_LL_-SDFPSQNX19_P0**	**C8T28SOIDV_LL_-SDFPSQNX14_P0**	**C8T28SOIDV_LL_-SDFPSQNX19_P0**
CP to QN ↓	0.0633	0.0648	0.8662	0.6620
CP to QN ↑	0.0549	0.0566	1.2419	0.9333
SN to QN ↓	0.0459	0.0480	0.8656	0.6607
	C8T28SOIDV_LL_-SDFPSQNX23_P0	**C8T28SOIDV_LL_-SDFPSQNX29_P0**	**C8T28SOIDV_LL_-SDFPSQNX23_P0**	**C8T28SOIDV_LL_-SDFPSQNX29_P0**
CP to QN ↓	0.0659	0.0632	0.5247	0.4539
CP to QN ↑	0.0566	0.0573	0.9302	0.6258
SN to QN ↓	0.0496	0.0493	0.5238	0.4538

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P0	C8T28SOI_-LLHF_-SDFPSQNX3_-P0	C8T28SOIDV_-LL_-SDFPSQNX5_-P0	C8T28SOIDV_-LL_-SDFPSQNX10_-P0
CP ↓	min_pulse_width to CP	0.0750	0.0763	0.0629	0.0660
CP ↑	min_pulse_width to CP	0.0362	0.0317	0.0348	0.0362
D ↓	hold_rising to CP	-0.0316	-0.0701	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0017	0.0008	0.0032	0.0032
D ↓	setup_rising to CP	0.0662	0.1094	0.0467	0.0467

D ↑	setup_rising to CP	0.0294	0.0288	0.0249	0.0249
SN ↓	min_pulse_width to SN	0.0354	0.0305	0.0332	0.0332
SN ↑	recovery_rising to CP	0.0031	0.0031	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0163	0.0212	0.0260	0.0260
TE ↓	hold_rising to CP	-0.0165	-0.0181	-0.0050	-0.0050
TE ↑	hold_rising to CP	0.0009	-0.0018	0.0058	0.0058
TE ↓	setup_rising to CP	0.0614	0.0878	0.0451	0.0451
TE ↑	setup_rising to CP	0.0764	0.1008	0.0689	0.0689
TI ↓	hold_rising to CP	-0.0426	-0.0654	-0.0329	-0.0293
TI ↑	hold_rising to CP	-0.0000	0.0012	0.0061	0.0061
TI ↓	setup_rising to CP	0.0773	0.1006	0.0675	0.0675
TI ↑	setup_rising to CP	0.0291	0.0235	0.0229	0.0229
		C8T28SOIDV_-LL_-SDFPSQNX14_-P0	C8T28SOIDV_-LL_-SDFPSQNX19_-P0	C8T28SOIDV_-LL_-SDFPSQNX23_-P0	C8T28SOIDV_-LL_-SDFPSQNX29_-P0
CP ↓	min_pulse_width to CP	0.0660	0.0660	0.0660	0.0629
CP ↑	min_pulse_width to CP	0.0362	0.0362	0.0362	0.0394
D ↓	hold_rising to CP	-0.0072	-0.0072	-0.0072	-0.0072
D ↑	hold_rising to CP	0.0032	0.0032	0.0032	0.0032
D ↓	setup_rising to CP	0.0467	0.0467	0.0467	0.0467
D ↑	setup_rising to CP	0.0249	0.0249	0.0249	0.0249
SN ↓	min_pulse_width to SN	0.0332	0.0332	0.0354	0.0381
SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0260	0.0260	0.0260	0.0260
TE ↓	hold_rising to CP	-0.0050	-0.0050	-0.0050	-0.0050
TE ↑	hold_rising to CP	0.0058	0.0058	0.0058	0.0058
TE ↓	setup_rising to CP	0.0451	0.0451	0.0451	0.0451
TE ↑	setup_rising to CP	0.0689	0.0689	0.0689	0.0689
TI ↓	hold_rising to CP	-0.0293	-0.0293	-0.0293	-0.0329
TI ↑	hold_rising to CP	0.0061	0.0061	0.0061	0.0061
TI ↓	setup_rising to CP	0.0675	0.0675	0.0675	0.0675
TI ↑	setup_rising to CP	0.0229	0.0229	0.0229	0.0229

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P0	2.440e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P0	2.087e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P0	2.363e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P0	3.385e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P0	3.828e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P0	4.407e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P0	4.579e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P0	6.032e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

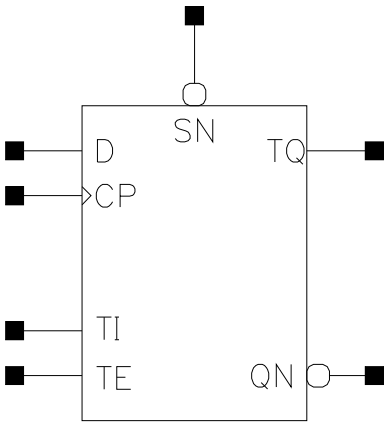
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P0	C8T28SOI_LLHF_-SDFPSQNX3_P0	C8T28SOIDV_LL_-SDFPSQNX5_P0	C8T28SOIDV_LL_-SDFPSQNX10_P0
Clock 100Mhz Data 0Mhz	7.659e-03	7.268e-03	6.953e-03	6.868e-03
Clock 100Mhz Data 25Mhz	7.406e-03	7.049e-03	6.837e-03	7.279e-03
Clock 100Mhz Data 50Mhz	7.152e-03	6.829e-03	6.721e-03	7.691e-03
Clock = 0 Data 100Mhz	3.494e-03	3.708e-03	3.589e-03	3.527e-03
Clock = 1 Data 100Mhz	4.188e-05	4.925e-04	3.434e-04	2.688e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P0	C8T28SOIDV_LL_-SDFPSQNX19_P0	C8T28SOIDV_LL_-SDFPSQNX23_P0	C8T28SOIDV_LL_-SDFPSQNX29_P0
Clock 100Mhz Data 0Mhz	6.814e-03	6.780e-03	6.756e-03	6.705e-03
Clock 100Mhz Data 25Mhz	7.480e-03	7.703e-03	7.818e-03	8.298e-03
Clock 100Mhz Data 50Mhz	8.145e-03	8.625e-03	8.879e-03	9.892e-03
Clock = 0 Data 100Mhz	3.490e-03	3.466e-03	3.449e-03	3.437e-03
Clock = 1 Data 100Mhz	2.241e-04	1.944e-04	1.731e-04	1.571e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P0	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P0	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P0	C8T28SOI_LLHF_-SDFPSQNTX3_P0	C8T28SOIDV_LL_-SDFPSQNTX5_P0	C8T28SOIDV_LL_-SDFPSQNTX10_P0
CP	0.0007	0.0006	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0013	0.0012	0.0009	0.0009
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNTX19_P0	C8T28SOIDV_LL_-SDFPSQNTX23_P0	C8T28SOIDV_LL_-SDFPSQNTX29_P0	
CP	0.0005	0.0005	0.0005	
D	0.0003	0.0003	0.0003	
SN	0.0009	0.0009	0.0009	
TE	0.0009	0.0009	0.0009	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P0	**C8T28SOI_LLHF_-SDFPSQNTX3_P0**	**C8T28SOI_LL_-SDFPSQNTX5_P0**	**C8T28SOI_LLHF_-SDFPSQNTX3_P0**
CP to QN ↓	0.0658	0.0656	2.8871	4.0784
CP to QN ↑	0.0658	0.0619	3.8959	5.6255
CP to TQ ↓	0.0559	0.0449	7.4382	4.8292
CP to TQ ↑	0.0559	0.0516	18.5680	9.8708
SN to QN ↓	0.0571	0.0497	2.8824	4.0724
SN to TQ ↑	0.0473	0.0363	18.5309	9.8289
	C8T28SOIDV_LL_-SDFPSQNTX5_P0	**C8T28SOIDV_LL_-SDFPSQNTX10_P0**	**C8T28SOIDV_LL_-SDFPSQNTX5_P0**	**C8T28SOIDV_LL_-SDFPSQNTX10_P0**
CP to QN ↓	0.0649	0.0614	2.5996	1.2850
CP to QN ↑	0.0542	0.0568	3.6915	1.8555
CP to TQ ↓	0.0389	0.0445	4.8290	4.8799
CP to TQ ↑	0.0499	0.0522	8.5122	8.5699
SN to QN ↓	0.0493	0.0469	2.6027	1.2838
SN to TQ ↑	0.0343	0.0378	8.4990	8.5301
	C8T28SOIDV_LL_-SDFPSQNTX19_P0	**C8T28SOIDV_LL_-SDFPSQNTX23_P0**	**C8T28SOIDV_LL_-SDFPSQNTX19_P0**	**C8T28SOIDV_LL_-SDFPSQNTX23_P0**
CP to QN ↓	0.0651	0.0667	0.6576	0.5234
CP to QN ↑	0.0606	0.0599	0.9381	0.9312
CP to TQ ↓	0.0444	0.0451	4.8778	4.9141
CP to TQ ↑	0.0521	0.0527	8.5722	8.5796
SN to QN ↓	0.0504	0.0520	0.6570	0.5230
SN to TQ ↑	0.0376	0.0382	8.5328	8.5430
	C8T28SOIDV_LL_-SDFPSQNTX29_P0		**C8T28SOIDV_LL_-SDFPSQNTX29_P0**	
CP to QN ↓	0.0663		0.4554	
CP to QN ↑	0.0617		0.6267	

CP to TQ ↓	0.0470		4.9945	
CP to TQ ↑	0.0558		9.8105	
SN to QN ↓	0.0517		0.4555	
SN to TQ ↑	0.0413		9.7570	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P0	C8T28SOI_-LLHF_-SDFPSQNTX3_-P0	C8T28SOIDV_-LL_-SDFPSQNTX5_-P0	C8T28SOIDV_-LL_SDFP-SQNTX10_P0
CP ↓	min_pulse_width to CP	0.0774	0.0763	0.0629	0.0629
CP ↑	min_pulse_width to CP	0.0422	0.0376	0.0362	0.0394
D ↓	hold_rising to CP	-0.0316	-0.0701	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0017	0.0008	0.0032	0.0032
D ↓	setup_rising to CP	0.0662	0.1094	0.0467	0.0467
D ↑	setup_rising to CP	0.0294	0.0288	0.0249	0.0249
SN ↓	min_pulse_width to SN	0.0403	0.0354	0.0332	0.0354
SN ↑	recovery_rising to CP	0.0031	0.0031	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0163	0.0212	0.0260	0.0260
TE ↓	hold_rising to CP	-0.0165	-0.0181	-0.0050	-0.0050
TE ↑	hold_rising to CP	0.0009	-0.0018	0.0058	0.0058
TE ↓	setup_rising to CP	0.0636	0.0878	0.0451	0.0445
TE ↑	setup_rising to CP	0.0760	0.1008	0.0689	0.0689
TI ↓	hold_rising to CP	-0.0426	-0.0661	-0.0329	-0.0329
TI ↑	hold_rising to CP	-0.0000	0.0012	0.0061	0.0061
TI ↓	setup_rising to CP	0.0771	0.1006	0.0675	0.0675
TI ↑	setup_rising to CP	0.0291	0.0235	0.0229	0.0229
		C8T28SOIDV_-LL_SDFP-SQNTX19_P0	C8T28SOIDV_-LL_SDFP-SQNTX23_P0	C8T28SOIDV_-LL_SDFP-SQNTX29_P0	
CP ↓	min_pulse_width to CP	0.0629	0.0629	0.0629	
CP ↑	min_pulse_width to CP	0.0407	0.0407	0.0407	
D ↓	hold_rising to CP	-0.0072	-0.0072	-0.0072	
D ↑	hold_rising to CP	0.0032	0.0032	0.0032	
D ↓	setup_rising to CP	0.0467	0.0467	0.0467	
D ↑	setup_rising to CP	0.0249	0.0249	0.0249	
SN ↓	min_pulse_width to SN	0.0354	0.0354	0.0381	

SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	
SN ↑	removal_rising to CP	0.0260	0.0260	0.0260	
TE ↓	hold_rising to CP	-0.0050	-0.0050	-0.0050	
TE ↑	hold_rising to CP	0.0058	0.0058	0.0058	
TE ↓	setup_rising to CP	0.0451	0.0451	0.0451	
TE ↑	setup_rising to CP	0.0689	0.0689	0.0689	
TI ↓	hold_rising to CP	-0.0329	-0.0329	-0.0329	
TI ↑	hold_rising to CP	0.0061	0.0061	0.0061	
TI ↓	setup_rising to CP	0.0675	0.0675	0.0675	
TI ↑	setup_rising to CP	0.0229	0.0229	0.0229	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P0	2.376e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P0	2.201e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P0	2.518e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_P0	3.500e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_P0	4.548e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_P0	4.737e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_P0	6.146e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

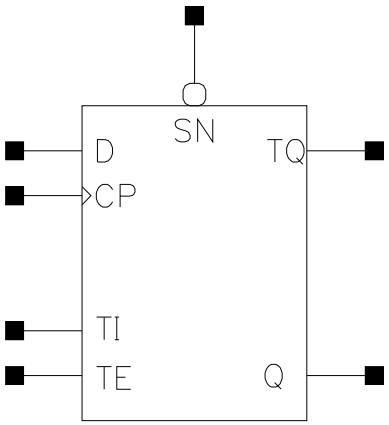
Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P0	C8T28SOI_LLHF_-SDFPSQNTX3_P0	C8T28SOIDV_LL_-SDFPSQNTX5_P0	C8T28SOIDV_LL_-SDFPSQNTX10_P0
Clock 100Mhz Data 0Mhz	7.417e-03	7.147e-03	6.876e-03	6.741e-03
Clock 100Mhz Data 25Mhz	7.457e-03	7.189e-03	6.883e-03	7.334e-03
Clock 100Mhz Data 50Mhz	7.497e-03	7.232e-03	6.889e-03	7.927e-03
Clock = 0 Data 100Mhz	3.486e-03	3.702e-03	3.584e-03	3.525e-03
Clock = 1 Data 100Mhz	4.195e-05	4.894e-04	3.413e-04	2.673e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P0	C8T28SOIDV_LL_-SDFPSQNTX23_P0	C8T28SOIDV_LL_-SDFPSQNTX29_P0	
Clock 100Mhz Data 0Mhz	6.660e-03	6.606e-03	6.567e-03	
Clock 100Mhz Data 25Mhz	7.781e-03	7.883e-03	8.414e-03	
Clock 100Mhz Data 50Mhz	8.902e-03	9.161e-03	1.026e-02	
Clock = 0 Data 100Mhz	3.490e-03	3.466e-03	3.451e-03	
Clock = 1 Data 100Mhz	2.229e-04	1.933e-04	1.722e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P0	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P0	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P0	C8T28SOI_LLHF_-SDFPSQTX3_P0	C8T28SOIDV_LL_-SDFPSQTX5_P0	C8T28SOIDV_LL_-SDFPSQTX10_P0
CP	0.0007	0.0006	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0013	0.0013	0.0009	0.0010
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQTX19_P0	C8T28SOIDV_LL_-SDFPSQTX29_P0		
CP	0.0005	0.0005		
D	0.0003	0.0003		
SN	0.0010	0.0010		
TE	0.0009	0.0009		
TI	0.0004	0.0004		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQTX5_P0	**C8T28SOI_LLHF_-SDFPSQTX3_P0**	**C8T28SOI_LL_-SDFPSQTX5_P0**	**C8T28SOI_LLHF_-SDFPSQTX3_P0**
CP to Q ↓	0.0561	0.0516	3.0102	4.4941
CP to Q ↑	0.0481	0.0520	3.7959	5.8447
CP to TQ ↓	0.0673	0.0502	7.8760	4.9691
CP to TQ ↑	0.0610	0.0545	18.5915	10.0329
SN to Q ↑	0.0396	0.0364	3.7440	5.7767
SN to TQ ↑	0.0509	0.0386	18.5280	9.9750
	C8T28SOIDV_LL_-SDFPSQTX5_P0	**C8T28SOIDV_LL_-SDFPSQTX10_P0**	**C8T28SOIDV_LL_-SDFPSQTX5_P0**	**C8T28SOIDV_LL_-SDFPSQTX10_P0**
CP to Q ↓	0.0443	0.0564	2.7176	1.3170
CP to Q ↑	0.0512	0.0766	3.7738	1.8822
CP to TQ ↓	0.0449	0.0581	4.9081	4.9562
CP to TQ ↑	0.0523	0.0796	8.6286	8.4571
SN to Q ↑	0.0366	0.0601	3.7644	1.8817
SN to TQ ↑	0.0378	0.0631	8.5928	8.4570
	C8T28SOIDV_LL_-SDFPSQTX19_P0	**C8T28SOIDV_LL_-SDFPSQTX29_P0**	**C8T28SOIDV_LL_-SDFPSQTX19_P0**	**C8T28SOIDV_LL_-SDFPSQTX29_P0**
CP to Q ↓	0.0607	0.0682	0.6821	0.4489
CP to Q ↑	0.0805	0.0870	0.9677	0.6411
CP to TQ ↓	0.0610	0.0393	4.2798	4.4221
CP to TQ ↑	0.0838	0.0551	9.7635	9.8513
SN to Q ↑	0.0639	0.0703	0.9671	0.6419
SN to TQ ↑	0.0672	0.0388	9.7694	9.8345

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_P0	C8T28SOI_-LLHF_-SDFPSQTX3_P0	C8T28SOIDV_-LL_-SDFPSQTX5_P0	C8T28SOIDV_-LL_-SDFPSQTX10_-P0
CP ↓	min_pulse_width to CP	0.0780	0.0763	0.0629	0.0654
CP ↑	min_pulse_width to CP	0.0502	0.0411	0.0362	0.0314
D ↓	hold_rising to CP	-0.0316	-0.0701	-0.0072	-0.0120
D ↑	hold_rising to CP	-0.0017	0.0008	0.0032	-0.0000
D ↓	setup_rising to CP	0.0662	0.1094	0.0467	0.0489
D ↑	setup_rising to CP	0.0294	0.0288	0.0249	0.0249
SN ↓	min_pulse_width to SN	0.0403	0.0354	0.0332	0.0332
SN ↑	recovery_rising to CP	0.0031	0.0058	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0163	0.0212	0.0260	0.0260
TE ↓	hold_rising to CP	-0.0165	-0.0181	-0.0050	-0.0066
TE ↑	hold_rising to CP	0.0009	-0.0018	0.0058	0.0010
TE ↓	setup_rising to CP	0.0636	0.0878	0.0451	0.0468
TE ↑	setup_rising to CP	0.0760	0.1008	0.0689	0.0689
TI ↓	hold_rising to CP	-0.0426	-0.0661	-0.0329	-0.0320
TI ↑	hold_rising to CP	-0.0000	0.0012	0.0061	-0.0000
TI ↓	setup_rising to CP	0.0771	0.1006	0.0675	0.0676
TI ↑	setup_rising to CP	0.0291	0.0235	0.0229	0.0293
		C8T28SOIDV_-LL_-SDFPSQTX19_-P0	C8T28SOIDV_-LL_-SDFPSQTX29_-P0		
CP ↓	min_pulse_width to CP	0.0654	0.0654		
CP ↑	min_pulse_width to CP	0.0314	0.0362		
D ↓	hold_rising to CP	-0.0120	-0.0120		
D ↑	hold_rising to CP	0.0032	0.0032		
D ↓	setup_rising to CP	0.0489	0.0489		
D ↑	setup_rising to CP	0.0249	0.0249		
SN ↓	min_pulse_width to SN	0.0332	0.0381		
SN ↑	recovery_rising to CP	-0.0017	-0.0017		
SN ↑	removal_rising to CP	0.0260	0.0260		
TE ↓	hold_rising to CP	-0.0072	-0.0072		
TE ↑	hold_rising to CP	0.0005	0.0005		

TE ↓	setup_rising to CP	0.0468	0.0468		
TE ↑	setup_rising to CP	0.0689	0.0689		
TI ↓	hold_rising to CP	-0.0277	-0.0277		
TI ↑	hold_rising to CP	-0.0000	-0.0003		
TI ↓	setup_rising to CP	0.0676	0.0676		
TI ↑	setup_rising to CP	0.0293	0.0293		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P0	2.280e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P0	2.134e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P0	2.343e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P0	3.255e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P0	3.978e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P0	5.425e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

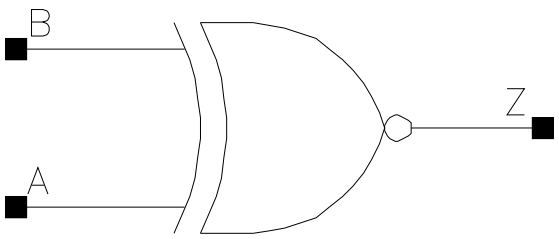
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P0	C8T28SOI_LLHF_-SDFPSQTX3_P0	C8T28SOIDV_LL_-SDFPSQTX5_P0	C8T28SOIDV_LL_-SDFPSQTX10_P0
Clock 100Mhz Data 0Mhz	7.427e-03	7.152e-03	6.882e-03	6.744e-03
Clock 100Mhz Data 25Mhz	7.510e-03	7.215e-03	6.904e-03	7.250e-03
Clock 100Mhz Data 50Mhz	7.593e-03	7.277e-03	6.926e-03	7.755e-03
Clock = 0 Data 100Mhz	3.485e-03	3.702e-03	3.583e-03	3.560e-03
Clock = 1 Data 100Mhz	4.200e-05	4.897e-04	3.415e-04	2.678e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P0	C8T28SOIDV_LL_-SDFPSQTX29_P0		
Clock 100Mhz Data 0Mhz	6.662e-03	6.608e-03		
Clock 100Mhz Data 25Mhz	7.758e-03	8.406e-03		
Clock 100Mhz Data 50Mhz	8.853e-03	1.020e-02		
Clock = 0 Data 100Mhz	3.539e-03	3.524e-03		
Clock = 1 Data 100Mhz	2.237e-04	1.942e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.600	0.544	0.8704
X5_P0	0.800	1.496	1.1968
X8_P0	1.600	1.088	1.7408
X9_P0	0.800	1.632	1.3056
X11_P0	1.600	1.360	2.1760
X14_P0	0.800	2.312	1.8496
X15_P0	1.600	1.904	3.0464
X19_P0	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P0	X5_P0	X8_P0	X9_P0
A	0.0009	0.0005	0.0015	0.0006
B	0.0008	0.0009	0.0012	0.0011
	X11_P0	X14_P0	X15_P0	X19_P0
A	0.0022	0.0009	0.0026	0.0011
B	0.0020	0.0015	0.0023	0.0017

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X5_P0	X4_P0	X5_P0
A to Z ↓	0.0139	0.0388	3.6243	2.7410
A to Z ↑	0.0157	0.0356	5.4357	4.0036
B to Z ↓	0.0130	0.0294	3.6246	2.7295
B to Z ↑	0.0166	0.0270	5.4424	4.0001

	X8_P0	X9_P0	X8_P0	X9_P0
A to Z ↓	0.0166	0.0364	1.9274	1.4116
A to Z ↑	0.0190	0.0339	2.9165	2.0451
B to Z ↓	0.0158	0.0281	1.9288	1.4094
B to Z ↑	0.0193	0.0263	2.9217	2.0457
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0157	0.0342	1.3529	0.9627
A to Z ↑	0.0174	0.0314	1.8984	1.3212
B to Z ↓	0.0143	0.0262	1.3536	0.9597
B to Z ↑	0.0175	0.0246	1.9034	1.3189
	X15_P0	**X19_P0**	**X15_P0**	**X19_P0**
A to Z ↓	0.0174	0.0319	1.0279	0.7172
A to Z ↑	0.0193	0.0300	1.4489	0.9827
B to Z ↓	0.0159	0.0251	1.0276	0.7154
B to Z ↑	0.0194	0.0239	1.4521	0.9818

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	1.437e-05	1.000e-20
X5_P0	1.256e-05	1.000e-20
X8_P0	2.192e-05	1.000e-20
X9_P0	2.280e-05	1.000e-20
X11_P0	3.374e-05	1.000e-20
X14_P0	3.479e-05	1.000e-20
X15_P0	4.184e-05	1.000e-20
X19_P0	5.185e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X5_P0	X8_P0	X9_P0
A to Z	1.670e-03	3.536e-03	3.215e-03	5.016e-03
B to Z	1.664e-03	2.860e-03	3.201e-03	4.092e-03
	X11_P0	X14_P0	X15_P0	X19_P0
A to Z	4.620e-03	7.859e-03	6.235e-03	9.540e-03
B to Z	4.566e-03	6.272e-03	6.164e-03	7.789e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

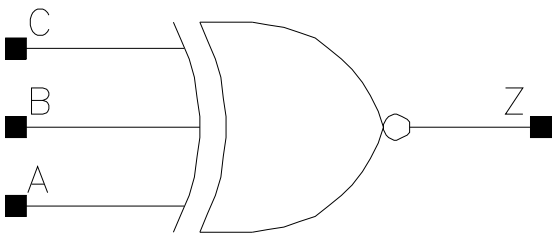
Pin Cycle (vdds)	X4_P0	X5_P0	X8_P0	X9_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P0	X14_P0	X15_P0	X19_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P0	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P0	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P0	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P0	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P0	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P0	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P0	C8T28SOIDV_LL_-XNOR3X4_P0	C8T28SOIDV_LL_-XNOR3X9_P0	C8T28SOIDV_LL_-XNOR3X13_P0
A	0.0014	0.0014	0.0018	0.0024
B	0.0014	0.0013	0.0017	0.0023
C	0.0007	0.0006	0.0006	0.0006
	C8T28SOIDV_LLS_-XNOR3X1_P0	C8T28SOIDV_LLS_-XNOR3X2_P0	C8T28SOIDV_LLS_-XNOR3X5_P0	C8T28SOIDV_LLS_-XNOR3X7_P0

A	0.0014	0.0015	0.0034	0.0051
B	0.0015	0.0016	0.0031	0.0048
C	0.0009	0.0012	0.0022	0.0033

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XNOR3X2_P0	**C8T28SOIDV_LL_-XNOR3X4_P0**	**C8T28SOIDV_LL_-XNOR3X2_P0**	**C8T28SOIDV_LL_-XNOR3X4_P0**
A to Z ↓	0.0393	0.0412	5.4925	2.9559
A to Z ↑	0.0375	0.0381	7.2875	4.0492
B to Z ↓	0.0399	0.0419	5.4953	2.9562
B to Z ↑	0.0382	0.0388	7.2934	4.0494
C to Z ↓	0.0527	0.0555	5.4899	2.9523
C to Z ↑	0.0510	0.0523	7.2861	4.0509
	C8T28SOIDV_LL_-XNOR3X9_P0	**C8T28SOIDV_LL_-XNOR3X13_P0**	**C8T28SOIDV_LL_-XNOR3X9_P0**	**C8T28SOIDV_LL_-XNOR3X13_P0**
A to Z ↓	0.0357	0.0411	1.4962	1.0288
A to Z ↑	0.0373	0.0430	1.9813	1.3859
B to Z ↓	0.0363	0.0419	1.4958	1.0285
B to Z ↑	0.0381	0.0440	1.9831	1.3864
C to Z ↓	0.0512	0.0619	1.4950	1.0277
C to Z ↑	0.0524	0.0640	1.9819	1.3850
	C8T28SOIDV_LLS_-XNOR3X1_P0	**C8T28SOIDV_LLS_-XNOR3X2_P0**	**C8T28SOIDV_LLS_-XNOR3X1_P0**	**C8T28SOIDV_LLS_-XNOR3X2_P0**
A to Z ↓	0.0243	0.0270	9.9706	5.5283
A to Z ↑	0.0255	0.0251	16.0182	8.5839
B to Z ↓	0.0250	0.0278	9.9956	5.5389
B to Z ↑	0.0261	0.0259	16.0184	8.5841
C to Z ↓	0.0243	0.0264	10.0073	5.5549
C to Z ↑	0.0256	0.0249	16.0086	8.5856
	C8T28SOIDV_LLS_-XNOR3X5_P0	**C8T28SOIDV_LLS_-XNOR3X7_P0**	**C8T28SOIDV_LLS_-XNOR3X5_P0**	**C8T28SOIDV_LLS_-XNOR3X7_P0**
A to Z ↓	0.0279	0.0239	2.6830	1.8577
A to Z ↑	0.0270	0.0233	4.2431	2.8425
B to Z ↓	0.0276	0.0232	2.6911	1.8646
B to Z ↑	0.0267	0.0229	4.2445	2.8437
C to Z ↓	0.0264	0.0226	2.6912	1.8669
C to Z ↑	0.0256	0.0219	4.2392	2.8428

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P0	8.299e-06	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P0	1.057e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P0	2.028e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P0	2.918e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P0	5.310e-06	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P0	1.103e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P0	2.689e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P0	4.185e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P0	C8T28SOIDV_LL_-XNOR3X4_P0	C8T28SOIDV_LL_-XNOR3X9_P0	C8T28SOIDV_LL_-XNOR3X13_P0
A to Z	2.162e-03	2.563e-03	3.840e-03	6.441e-03
B to Z	2.144e-03	2.547e-03	3.862e-03	6.475e-03
C to Z	3.388e-03	3.837e-03	5.424e-03	8.876e-03
	C8T28SOIDV_LLS_-XNOR3X1_P0	C8T28SOIDV_LLS_-XNOR3X2_P0	C8T28SOIDV_LLS_-XNOR3X5_P0	C8T28SOIDV_LLS_-XNOR3X7_P0
A to Z	1.285e-03	1.862e-03	4.093e-03	5.600e-03
B to Z	1.275e-03	1.887e-03	4.126e-03	5.532e-03
C to Z	1.251e-03	1.863e-03	4.066e-03	5.470e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

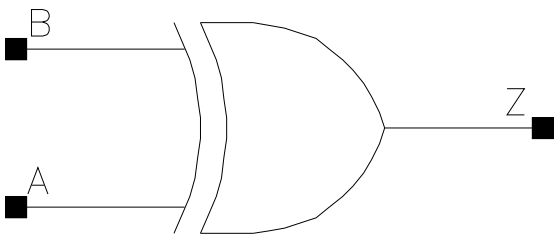
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P0	C8T28SOIDV_LL_-XNOR3X4_P0	C8T28SOIDV_LL_-XNOR3X9_P0	C8T28SOIDV_LL_-XNOR3X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P0	C8T28SOIDV_LLS_-XNOR3X2_P0	C8T28SOIDV_LLS_-XNOR3X5_P0	C8T28SOIDV_LLS_-XNOR3X7_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.360	1.0880
X4_P0	1.600	0.544	0.8704
X5_P0	0.800	1.360	1.0880
X8_P0	1.600	1.088	1.7408
X9_P0	0.800	1.496	1.1968
X12_P0	1.600	1.360	2.1760
X13_P0	0.800	2.176	1.7408
X15_P0	1.600	1.904	3.0464
X17_P0	0.800	2.312	1.8496
X18_P0	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P0	X4_P0	X5_P0	X8_P0
A	0.0005	0.0009	0.0006	0.0014
B	0.0009	0.0008	0.0010	0.0014
	X9_P0	X12_P0	X13_P0	X15_P0
A	0.0006	0.0023	0.0011	0.0027
B	0.0013	0.0017	0.0021	0.0022
	X17_P0	X18_P0		
A	0.0011	0.0015		
B	0.0021	0.0018		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X4_P0**	**X2_P0**	**X4_P0**
A to Z ↓	0.0333	0.0140	5.2583	2.7786
A to Z ↑	0.0321	0.0174	7.5034	7.2478
B to Z ↓	0.0261	0.0144	5.2257	2.8036
B to Z ↑	0.0264	0.0161	7.4912	7.2469
	X5_P0	**X8_P0**	**X5_P0**	**X8_P0**
A to Z ↓	0.0312	0.0181	2.8429	1.5189
A to Z ↑	0.0288	0.0209	3.9083	3.8227
B to Z ↓	0.0242	0.0191	2.8303	1.5357
B to Z ↑	0.0234	0.0197	3.9020	3.8213
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0307	0.0164	1.4876	1.0208
A to Z ↑	0.0291	0.0188	2.0452	2.5617
B to Z ↓	0.0239	0.0161	1.4826	1.0310
B to Z ↑	0.0233	0.0170	2.0420	2.5611
	X13_P0	**X15_P0**	**X13_P0**	**X15_P0**
A to Z ↓	0.0282	0.0179	1.0187	0.7981
A to Z ↑	0.0267	0.0217	1.4130	2.2879
B to Z ↓	0.0203	0.0174	1.0153	0.8066
B to Z ↑	0.0191	0.0196	1.4106	2.2874
	X17_P0	**X18_P0**	**X17_P0**	**X18_P0**
A to Z ↓	0.0297	0.0334	0.7702	0.7695
A to Z ↑	0.0278	0.0301	1.0566	1.0157
B to Z ↓	0.0219	0.0271	0.7687	0.7687
B to Z ↑	0.0204	0.0239	1.0561	1.0149

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P0	9.425e-06	1.000e-20
X4_P0	1.312e-05	1.000e-20
X5_P0	1.668e-05	1.000e-20
X8_P0	1.996e-05	1.000e-20
X9_P0	3.061e-05	1.000e-20
X12_P0	3.128e-05	1.000e-20
X13_P0	4.913e-05	1.000e-20
X15_P0	3.644e-05	1.000e-20
X17_P0	5.305e-05	1.000e-20
X18_P0	5.008e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P0	X4_P0	X5_P0	X8_P0
A to Z	2.598e-03	1.693e-03	3.287e-03	3.304e-03
B to Z	2.298e-03	1.658e-03	2.860e-03	3.295e-03
	X9_P0	X12_P0	X13_P0	X15_P0
A to Z	4.760e-03	4.673e-03	7.762e-03	6.053e-03
B to Z	4.224e-03	4.527e-03	5.423e-03	5.885e-03
	X17_P0	X18_P0		
A to Z	8.776e-03	9.781e-03		
B to Z	6.413e-03	7.779e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

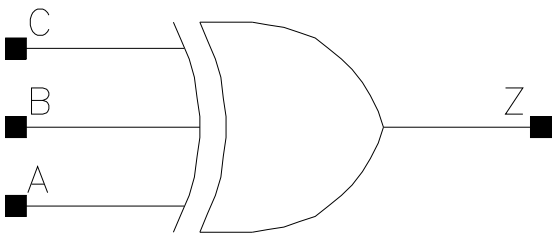
Pin Cycle (vdds)	X2_P0	X4_P0	X5_P0	X8_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P0	X12_P0	X13_P0	X15_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P0	X18_P0		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P0	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P0	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P0	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P0	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P0	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P0	C8T28SOIDV_LL_-XOR3X4_P0	C8T28SOIDV_LL_-XOR3X9_P0	C8T28SOIDV_LL_-XOR3X13_P0
A	0.0015	0.0014	0.0016	0.0024
B	0.0014	0.0015	0.0017	0.0023
C	0.0009	0.0009	0.0012	0.0019
	C8T28SOIDV_LLS_-XOR3X1_P0	C8T28SOIDV_LLS_-XOR3X2_P0	C8T28SOIDV_LLS_-XOR3X5_P0	C8T28SOIDV_LLS_-XOR3X7_P0

A	0.0015	0.0016	0.0027	0.0042
B	0.0016	0.0016	0.0027	0.0043
C	0.0005	0.0005	0.0005	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P0	**C8T28SOIDV_LL_-XOR3X4_P0**	**C8T28SOIDV_LL_-XOR3X2_P0**	**C8T28SOIDV_LL_-XOR3X4_P0**
A to Z ↓	0.0380	0.0416	5.5177	2.9676
A to Z ↑	0.0366	0.0393	7.5024	4.0580
B to Z ↓	0.0385	0.0425	5.5194	2.9685
B to Z ↑	0.0372	0.0404	7.4992	4.0588
C to Z ↓	0.0380	0.0418	5.5211	2.9687
C to Z ↑	0.0365	0.0395	7.4986	4.0582
	C8T28SOIDV_LL_-XOR3X9_P0	**C8T28SOIDV_LL_-XOR3X13_P0**	**C8T28SOIDV_LL_-XOR3X9_P0**	**C8T28SOIDV_LL_-XOR3X13_P0**
A to Z ↓	0.0379	0.0422	1.4830	1.0082
A to Z ↑	0.0383	0.0437	1.9972	1.3447
B to Z ↓	0.0388	0.0429	1.4838	1.0079
B to Z ↑	0.0393	0.0448	1.9982	1.3453
C to Z ↓	0.0379	0.0426	1.4832	1.0084
C to Z ↑	0.0380	0.0445	1.9981	1.3443
	C8T28SOIDV_LLS_-XOR3X1_P0	**C8T28SOIDV_LLS_-XOR3X2_P0**	**C8T28SOIDV_LLS_-XOR3X1_P0**	**C8T28SOIDV_LLS_-XOR3X2_P0**
A to Z ↓	0.0253	0.0280	7.1069	5.6436
A to Z ↑	0.0256	0.0251	11.6324	8.1995
B to Z ↓	0.0261	0.0286	7.1339	5.6528
B to Z ↑	0.0264	0.0257	11.6395	8.2005
C to Z ↓	0.0396	0.0426	7.0531	5.6009
C to Z ↑	0.0406	0.0405	11.5802	8.1455
	C8T28SOIDV_LLS_-XOR3X5_P0	**C8T28SOIDV_LLS_-XOR3X7_P0**	**C8T28SOIDV_LLS_-XOR3X5_P0**	**C8T28SOIDV_LLS_-XOR3X7_P0**
A to Z ↓	0.0371	0.0318	2.9367	2.0363
A to Z ↑	0.0315	0.0272	4.2778	2.8970
B to Z ↓	0.0353	0.0316	2.9467	2.0422
B to Z ↑	0.0309	0.0274	4.2827	2.8987
C to Z ↓	0.0589	0.0491	2.9368	2.0272
C to Z ↑	0.0549	0.0452	4.2612	2.8820

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P0	6.574e-06	1.000e-20
C8T28SOIDV_LL_XOR3X4_P0	9.245e-06	1.000e-20
C8T28SOIDV_LL_XOR3X9_P0	1.893e-05	1.000e-20
C8T28SOIDV_LL_XOR3X13_P0	2.784e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P0	1.063e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P0	1.336e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P0	2.266e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P0	3.390e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P0	C8T28SOIDV_LL_-XOR3X4_P0	C8T28SOIDV_LL_-XOR3X9_P0	C8T28SOIDV_LL_-XOR3X13_P0
A to Z	2.044e-03	2.563e-03	3.875e-03	6.776e-03
B to Z	2.021e-03	2.557e-03	3.899e-03	6.800e-03
C to Z	1.995e-03	2.523e-03	3.872e-03	6.799e-03
	C8T28SOIDV_LLS_-XOR3X1_P0	C8T28SOIDV_LLS_-XOR3X2_P0	C8T28SOIDV_LLS_-XOR3X5_P0	C8T28SOIDV_LLS_-XOR3X7_P0
A to Z	1.574e-03	1.915e-03	3.835e-03	5.340e-03
B to Z	1.571e-03	1.937e-03	3.881e-03	5.416e-03
C to Z	2.963e-03	3.395e-03	6.320e-03	8.813e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P0	C8T28SOIDV_LL_-XOR3X4_P0	C8T28SOIDV_LL_-XOR3X9_P0	C8T28SOIDV_LL_-XOR3X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P0	C8T28SOIDV_LLS_-XOR3X2_P0	C8T28SOIDV_LLS_-XOR3X5_P0	C8T28SOIDV_LLS_-XOR3X7_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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