C28SOI_IO_EXT_ANAF_ANA_EG User's Manual

Analog IO library in analog frame designed in 28nm FDSOI CMOS technology

Overview

The C28SOI_IO_EXT_ANAF_ANA_EG library is designed in 28nm FDSOI technology. This library provides all cells needed to make an analog IO ring or an analog IO cluster.

Features

- Uses the standard process option and 28 Å gate oxide.
- Supports single row configuration for an analog IO ring[1] or analog IO cluster.
- Provides 1.0 V, 1.8 V and 3.3 V supplies and dedicated supplies.
- Provides analog and analog UHF IO cells.
- Reduced noise propagation through the supply rails.

Applications

The cells provided in the library are used for constructing 1V0, 1V8, and 3V3 analog IO ring or IO cluster.

Information Snapshot

Process Options

- GO1: SVT
- GO2: 28 Å

Packaging

- Flip-chip

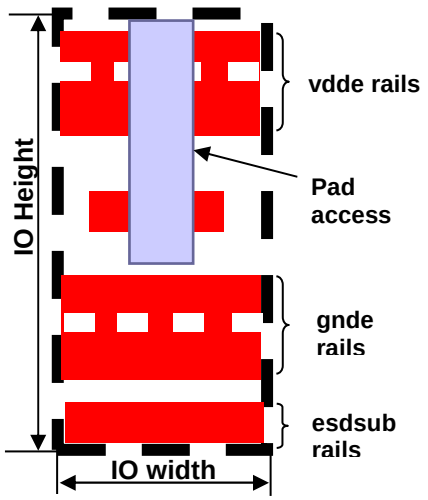
Table 1 : Operating values

Symbol	Parameter	Min	Typ	Max	Unit
vdde	Supply for 1.0, 1.8 or 3.3V IO ring	*	1.0	1.1	V
		*	1.8	1.95	V
		*	3.3	3.6	V
vdde1v0	Supply voltage for 1.0 V IO ring	*	1.0	1.1	V
vdde1v8	Supply voltage for 1.8 V IO ring	*	1.8	1.95	V
vdde3v3	Supply voltage for 3.3 V IO ring	*	3.3	3.6	V
vddcore1v0	Supply voltage for 1.0V node	*	1.0	1.1	V
vddcore1v8	Supply voltage for 1.8V node	*	1.8	1.95	V
vddcore3v3	Supply voltage for 3.3V node	*	3.3	3.6	V
$T_{junction}$	Operating junction temperature	-40	25	125	˚C

* As per Design Platform specification

For more details about electrical specifications, please refer to *Section 3: Electrical Specifications*.

Figure 1 : Flip-chip analog IO topology



[1] Single row configuration is also called linear configuration.

1. Quick References

	*The document uses the following convention to indicate logic levels:* *L indicates logic low.* *H indicates logic high.* *X indicates don't care state.* *Z indicates high impedance state.* *'-' (Hyphen) indicates 'No activity'.*

	** suffixed in library name indicates multiple metallization options.* *** suffixed in cell name indicates multiple packages / configurations.*

1.1 Metal Stacking Convention

The metallization options supported by this library can be referred from its product package. The following is the convention that can be used to decode the segment in the library name:

- 7 metal option (5U1X2T8XLB) known as 5002 refers as follows:
  - 5U1X refers to the first 5 levels with 1X pitch (thin) metal.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 8 metal option (6U1X2T8XLB) known as 6002 refers as follows:
  - 6U1X refers to the first 6 levels with 1X pitch (thin) metal in ultra-low K.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 10 metal option (6U1X2U2X2T8XLB) known as 6202 refers as follows:
  - 6U1X refers to the first 6 levels with 1x pitch (thin) metal in ultra-low K.
  - 2U2X refers to the next 2 levels with 2x pitch (thin) metal in ultra-low K.
  - 2T8X refers to 2 levels with 8x (thick) metal in oxide.
  - LB is the Alucap.

1.2 Reference Documentation

For details on the following topics:

- Power Sequencing Recommendation in IOs
- Specifications and Analysis of Overshoots and Undershoots
- SSN Application Notes
- ESD qualification
- Latch-up qualification
- Maturity information
- RDL recommended rules
  - ST users, refer to the IO Reference catalog

    (http://ccds.st.com/cps/sections/library/io/io_reference_catalog/downloadFile/file/IO_Helpdesk_Solutions.pdf).
  - Non-ST users, contact Customer Support personnel

1.3 Reference Library

The C28SOI_IO_EXT_ANAF_ANA_EG library refers to some cells from 28nm FDSOI libraries listed below. For a correct usage, these libraries are mandatory:

- C28SOI_IO_ALLF_FRAMEKIT_EG
- C28SOI_IO_ALLF_IOSUPPLYKIT_EG

1.4 Acronyms and Abbreviations Used

Table 2 : Acronyms and Abbreviations

Acronym/Abbreviation	Description
B2B	Back-to-Back
CDM	Charge Device Model
DC	Direct Current
DRM	Design Rule Manual
ESD	Electrostatic Discharge
HBM	Human Body Model
FC	Flip-chip
CL	Cluster
MM	Machine Model
RMS	Root Mean Square
SVT	Standard V_T
2ROWS	Two rows

2.Functional Specifications

The library cell offer comprises 1.0 V, 1.8 V, and 3.3 V analog IO cells in single layout configuration. Analog cells allow any voltage level between the rated minimum and maximum voltage specification.

The C28SOI_IO_EXT_ANAF_ANA_EG library includes 75 top cells.

Table 3 : Cell List

Cell Name	Width x Height (µm)	Cell Description
Input cells, FC views		
IO_20UM_EXT_ANA_FC_LIN	20 x 80	Signal Input/Output with series resistance dedicated to 1V0/1V8 ring section
IO_20UM_3V3_EXT_ANA_FC_LIN	20 x 80	Signal Input/Output with series resistance dedicated to 3V3 ring section
IO_20UM_50OHMS_EXT_ANA_FC_LIN	20 x 80	Analog IO cell with 50 Ohms series resistance
IO_20UM_3V3_50OHMS_EXT_ANA_FC_LIN	20 x 80	Analog IO cell with 50 Ohms series resistance
IO_UHF_EXT_ANA_FC_LIN	40 x 80	Signal Input/Output for RF application with series resistance
Input cells, CL views (cluster)		
IO_20UM_EXT_ANA_CL_LIN	20 x 80	Signal Input/Output with series resistance dedicated to 1V0/1V8 cluster section
IO_20UM_3V3_EXT_ANA_CL_LIN	20 x 80	Signal Input/Output with series resistance dedicated to 3V3 cluster section
IO_20UM_50OHMS_EXT_ANA_CL_LIN	20 x 80	Analog IO cell with 50 Ohms series resistance
IO_20UM_3V3_50OHMS_EXT_ANA_CL_LIN	20 x 80	Analog IO cell with 50 Ohms series resistance
IO_UHF_EXT_ANA_CL_LIN	40 x 80	Signal Input/Output for RF application with series resistance
Supply cells, FC views		
GNDE_ESD_1V0_EXT_ANA_FC_LIN	40 x 80	Ground supply with 1.0 V ESD protection
VDDE_ESD_1V0_EXT_ANA_FC_LIN	40 x 80	1.0 V power supply with 1.0 V ESD protection
GNDE_ESD_1V8_EXT_ANA_FC_LIN	40 x 80	Ground supply with 1.8 V ESD protection
VDDE_ESD_1V8_EXT_ANA_FC_LIN	40 x 80	1.8 V power supply with 1.8 V ESD protection
VDDE_GNDE_ESD_3V3_EXT_ANA_FC_LIN	100 x 80	3.3 V two slots power / ground supply with 3.3 V ESD protection
FILLCELL_ESD_1V0_EXT_ANA_FC_LIN	40 x 80	Filler including ESD protection for 1.0 V IO section
FILLCELL_ESD_1V8_EXT_ANA_FC_LIN	40 x 80	Filler including ESD protection for 1.8 V IO section
FILLCELL_ESD_3V3_EXT_ANA_FC_LIN	100 x 80	Filler including ESD protection for 3.3 V IO section
Supply cells, CL views (cluster)		

Table 3 : Cell List		
Cell Name	**Width x Height (µm)**	**Cell Description**
GNDE_ESD_1V0_EXT_ANA_CL_LIN	40 x 80	Ground supply with 1.0 V ESD protection
VDDE_ESD_1V0_EXT_ANA_ CL _LIN	40 x 80	1.0 V power supply with 1.0 V ESD protection
GNDE_ESD_1V8_EXT_ANA_ CL _LIN	40 x 80	Ground supply with 1.8 V ESD protection
VDDE_ESD_1V8_EXT_ANA_ CL _LIN	40 x 80	1.8 V power supply with 1.8 V ESD protection
VDDE_GNDE_ESD_3V3_EXT_ANA_ CL _LIN	100 x 80	3.3 V two slots power / ground supply with 3.3 V ESD protection
FILLCELL_ESD_1V0_EXT_ANA_ CL _LIN	40 x 80	Filler including ESD protection for 1.0 V IO section
FILLCELL_ESD_1V8_EXT_ANA_ CL _LIN	40 x 80	Filler including ESD protection for 1.8 V IO section
FILLCELL_ESD_3V3_EXT_ANA_ CL _LIN	100 x 80	Filler including ESD protection for 3.3 V IO section
Power cells, FC views		
ESDSUB_EXT_ANA_FC_LIN	40 x 80	Substrate and ESD reference ground supply
GNDE_NOESD_EXT_ANA_FC_LIN	40 x 80	Ground supply, pad to gnde without ESD protection
VDDE_NOESD_EXT_ANA_FC_LIN	40 x 80	Power supply, pad to vdde without ESD protection
Power cells, CL views (cluster)		
ESDSUB_EXT_ANA_CL_LIN	40 x 80	Substrate and ESD reference ground supply
GNDE_NOESD_EXT_ANA_CL_LIN	40 x 80	Ground supply, pad to gnde without ESD protection
VDDE_NOESD_EXT_ANA_CL_LIN	40 x 80	Power supply, pad to vdde without ESD protection
Dedicated supply cells, FC views		
GNDCORE_EXT_ANA_FC_LIN	30 x 80	Dedicated core ground supply
VDDCORE_1V0_GNDCORE_EXT_ANA_FC_LIN	70 x 80	Dedicated 1.0 V power supply referring to a dedicated ground node
VDDCORE_1V0_GNDE_EXT_ANA_FC_LIN	70 x 80	Dedicated 1.0 V power supply referring to gnde ground node
VDDCORE_1V0_ESDSUB_EXT_ANA_FC_LIN	70 x 80	Dedicated 1.0 V power supply referring to esdsub ground node
VDDCORE_1V8_GNDCORE_EXT_ANA_FC_LIN	70 x 80	Dedicated 1.8 V power supply referring to a dedicated ground node
VDDCORE_1V8_GNDE_EXT_ANA_FC_LIN	70 x 80	Dedicated 1.8 V power supply referring to gnde ground node
VDDCORE_1V8_ESDSUB_EXT_ANA_FC_LIN	70 x 80	Dedicated 1.8 V power supply referring to esdsub ground node
VDDCORE_3V3_GNDCORE_EXT_ANA_FC_LIN	100 x 80	Dedicated 3.3 V power supply referring to a dedicated ground node
VDDCORE_3V3_GNDE_EXT_ANA_FC_LIN	100 x 80	Dedicated 3.3 V power supply referring to gnde ground node

Table 3 : Cell List

Cell Name	Width x Height (µm)	Cell Description
VDDCORE_3V3_ESDSUB_EXT_ANA_FC_LIN	100 x 80	Dedicated 3.3 V power supply referring to esdsub ground node
Dedicated supply cells, CL views (cluster)		
GNDCORE_EXT_ANA_CL_LIN	30 x 80	Dedicated core ground supply
VDDCORE_1V0_GNDCORE_EXT_ANA_CL_LIN	70 x 80	Dedicated 1.0 V power supply referring to a dedicated ground node
VDDCORE_1V0_GNDE_EXT_ANA_CL_LIN	70 x 80	Dedicated 1.0 V power supply referring to gnde ground node
VDDCORE_1V0_ESDSUB_EXT_ANA_CL_LIN	70 x 80	Dedicated 1.0 V power supply referring to esdsub ground node
VDDCORE_1V8_GNDCORE_EXT_ANA_CL_LIN	70 x 80	Dedicated 1.8 V power supply referring to a dedicated ground node
VDDCORE_1V8_GNDE_EXT_ANA_CL_LIN	70 x 80	Dedicated 1.8 V power supply referring to gnde ground node
VDDCORE_1V8_ESDSUB_EXT_ANA_CL_LIN	70 x 80	Dedicated 1.8 V power supply referring to esdsub ground node
VDDCORE_3V3_GNDCORE_EXT_ANA_CL_LIN	100 x 80	Dedicated 3.3 V power supply referring to a dedicated ground node
VDDCORE_3V3_GNDE_EXT_ANA_CL_LIN	100 x 80	Dedicated 3.3 V power supply referring to gnde ground node
VDDCORE_3V3_ESDSUB_EXT_ANA_CL_LIN	100 x 80	Dedicated 3.3 V power supply referring to esdsub ground node
Filler cells, FC views		
FILLCELL_1GRID_EXT_ANA_FC_LIN	0.1 x 80	Analog IO filler
FILLCELL_1UM_EXT_ANA_ FC _LIN	1 x 80	Analog IO filler
FILLCELL_5UM_EXT_ANA_ FC _LIN	5 x 80	Analog IO filler
FILLCELL_10UM_EXT_ANA_ FC _LIN	10 x 80	Analog IO filler
CORNERCELL_EXT_ANA_ FC _LIN	80 x 80	Corner of the analog IO ring
FILLCELL_END_LEFT_EXT_ANA_ FC _LIN	18 x 80	Filler which closes left side of an IO ring section
FILLCELL_END_RIGHT_EXT_ANA_ FC _LIN	18 x 80	Filler which closes right side of an IO ring section
FILLCUTCELL_GNDE_EXT_ANA_ FC _LIN	1.6 x 80	Cuts gnde rails
FILLCUTCELL_VDDE_EXT_ANA_ FC _LIN	1.6 x 80	Cuts vdde rails
FILLCUTCELL_ALL_EXT_ANA_ FC _LIN	15.1 x 80	Cuts all rails. esdsub rail continuity ensured through back-to-back diodes
FILLCELL_STEP_BTB_EXT_ANAF_TO_CSF_FC_LIN	18.3 x 80	Allow transition between ANAF analog frame and CSF digital frame. Ground reference continuity ensured through back-to-back diodes
FILLCELL_STEP_EXT_ANAF_TO_CSF_FC_LIN	18.3 x 80	Allow transition between ANAF analog frame and CSF digital frame with a continuous ground reference node

Table 3 : Cell List		
Cell Name	**Width x Height (µm)**	**Cell Description**
FILLCELL_STEP_BTB_EXT_ANAF_TO_CSF_FC_2ROWS	18.3 x 80	Allow transition between ANAF analog frame and CSF 2ROWS digital frame. Ground reference continuity ensured through back-to-back diodes
FILLCELL_STEP_EXT_ANAF_TO_CSF_FC_2ROWS	18.3 x 80	Allow transition between ANAF analog frame and CSF 2ROWS digital frame with a continuous ground reference node
Filler cells, CL views (cluster)		
FILLCELL_1GRID_EXT_ANA_CL_LIN	0.1 x 80	Analog IO filler
FILLCELL_1UM_EXT_ANA_ CL _LIN	1 x 80	Analog IO filler
FILLCELL_5UM_EXT_ANA_ CL _LIN	5 x 80	Analog IO filler
FILLCELL_10UM_EXT_ANA_ CL _LIN	10 x 80	Analog IO filler
FILLCELL_FEEDTHROUGH_EXT_ANA_ CL _LIN	40 x 80	Filler allowing routing via M2 / M3 / M4 through an IO cluster
FILLCELL_END_LEFT_EXT_ANA_ CL _LIN	18 x 80	Filler which closes left side of an IO ring section
FILLCELL_END_RIGHT_EXT_ANA_ CL _LIN	18 x 80	Filler which closes right side of an IO ring section
FILLCUTCELL_GNDE_EXT_ANA_ CL _LIN	1.6 x 80	Cuts gnde rails
FILLCUTCELL_VDDE_EXT_ANA_ CL _LIN	1.6 x 80	Cuts vdde rails

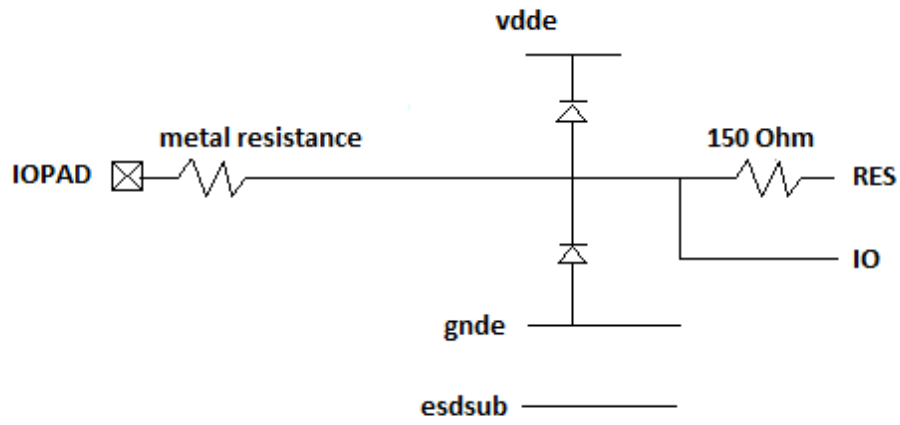
Please be aware that, for ANAF analog frame, there are no differences between FC cells and CL cells. Only their names are different.

The ALLCELLS cells are not considered part of the Deliverable. These cells are specifically for QA check and hence subject to change, without prior notice.

2.1 IO_20UM_EXT_ANA_FC_LIN / CL_LIN

2.1.1 Functional Diagram

Figure 2 : Block Diagram



2.1.2 Interface Description

Table 4 : Pin Description

Pin	Type	Voltage Level (V)	Description
Logic core pins			
RES	Input/Output	0 to vdde	Input node varying between vdde and gnde with series resistor, core side
IO	Input/Output	0 to vdde	Input node varying between vdde and gnde without series resistor, core side
Pad pin			
IOPAD	Input/Output	0 to vdde	Input node varying between vdde and gnde without series resistor, pad side
Track pins			
vdde	Input/Output	vdde	IO power node (1.0V or 1.8V)
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node

2.1.3 Cell Information

Table 5 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (IO node)	-	-	106	mΩ
		25 ˚C (RES node)	-	-	150	Ω
I_{DC}	DC current Pad To Core [2]	110 ˚C (IO node)	-	-	57	mA
		125 ˚C (IO node)	-	-	36	
		110 ˚C (RES node)	-	-	3	
		125 ˚C (RES node)	-	-	1	
	DC current Pad To Core [2]	110 ˚C (IO node)	-	-	38	
		125 ˚C (IO node)	-	-	22	
		110 ˚C (RES node)	-	-	3	
		125 ˚C (RES node)	-	-	1	
I_{RMS}	RMS current Pad To Core [1]	100 ˚C (IO node)	-	-	33	mA
		100 ˚C (RES node)	-	-	7	
	RMS current Pad To Core [2]	100 ˚C (IO node)	-	-	33	
		100 ˚C (RES node)	-	-	7	
C_{Par}	Parasitic capacitance (without Bump)	Corner TT, 125 ˚C (IO node)	-	-	637	fF
	Parasitic capacitance (with BUMP_FC61A_96X96)	Corner TT, 125 ˚C (IO node)	-	-	692 [3]	
$I_{leakage}$	Leakage current	Fast process, Max voltage, 25 ˚C (vdde node)	-	-	12	pA
		Fast process, Max voltage, 125 ˚C (vdde node)	-	-	56	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

[3] The parasitic capacitance value depends on the type and the position of bump.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

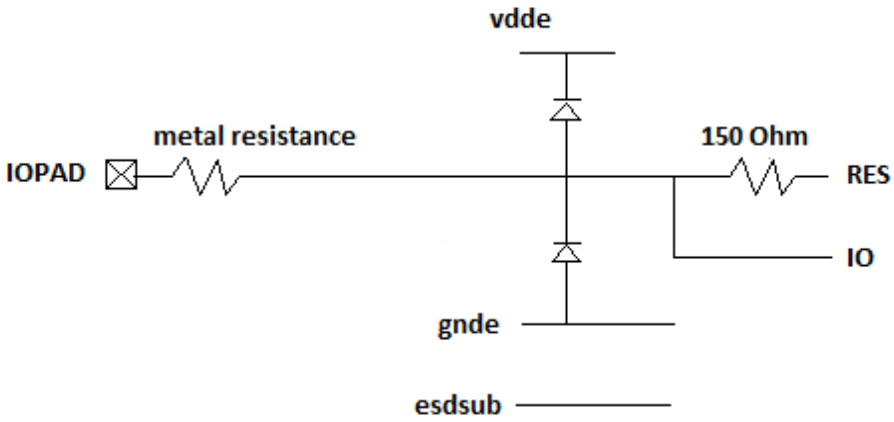
2.1.4 Functional Description

The IO_20UM_EXT_ANA_FC_LIN / CL_LIN cell is designed to interface 1V0/1V8 analog signals between the core and external domain.

2.2 IO_20UM_3V3_EXT_ANA_FC_LIN / CL_LIN

2.2.1 Functional Diagram

Figure 3 : Block Diagram



2.2.2 Interface Description

Table 6 : Pin Description

Pin	Type	Voltage Level (V)	Description
Logic core pins			
RES	Input/Output	0 to vdde	Input node varying between vdde and gnde with series resistor, core side
IO	Input/Output	0 to vdde	Input node varying between vdde and gnde without series resistor, core side
Pad pin			
IOPAD	Input/Output	0 to vdde	Input node varying between vdde and gnde without series resistor, pad side
Track pins			
vdde	Input/Output	vdde	IO power node (3.3V)
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node

2.2.3 Cell Information

Table 7 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (IO node)	-	-	106	mΩ
		25 ˚C (RES node)	-	-	150	Ω
I_{DC}	DC current Pad To Core [2]	110 ˚C (IO node)	-	-	57	mA
		125 ˚C (IO node)	-	-	36	
		110 ˚C (RES node)	-	-	3	
		125 ˚C (RES node)	-	-	1	
	DC current Pad To Core [2]	110 ˚C (IO node)	-	-	38	
		125 ˚C (IO node)	-	-	22	
		110 ˚C (RES node)	-	-	3	
		125 ˚C (RES node)	-	-	1	
I_{RMS}	RMS current Pad To Core [1]	100 ˚C (IO node)	-	-	33	mA
		100 ˚C (RES node)	-	-	7	
	RMS current Pad To Core [2]	100 ˚C (IO node)	-	-	33	
		100 ˚C (RES node)	-	-	7	
C_{Par}	Parasitic capacitance (without Bump)	Corner TT, 125 ˚C (IO node)	-	-	362	fF
	Parasitic capacitance (with BUMP_FC61A_96X96)	Corner TT, 125 ˚C (IO node)	-	-	413 [2]	
$I_{leakage}$	Leakage current	Fast process, Max voltage, 25 ˚C (vdde node)	-	-	27	pA
		Fast process, Max voltage, 125 ˚C (vdde node)	-	-	214	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

[3] The parasitic capacitance value depends on the type and the position of bump.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

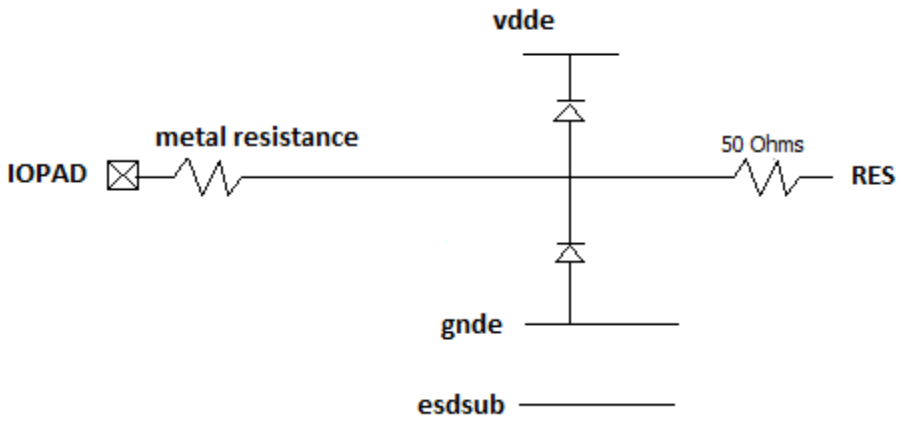
2.2.4 Functional Description

The IO_20UM_3V3_EXT_ANA_FC_LIN / CL_LIN cell is designed to interface 3V3 analog signals between the core and external domain.

2.3 IO_20UM_50OHMS_EXT_ANA_FC_LIN / CL_LIN

2.3.1 Functional Diagram

Figure 4 : Block Diagram



2.3.2 Interface Description

Table 8 : Pin Description

Pin	Type	Voltage Level (V)	Description
Logic core pins			
RES	Input/Output	0 to vdde	Input node varying between vdde and gnde with series resistor, core side
Pad pin			
IOPAD	Input/Output	0 to vdde	Input node varying between vdde and gnde without series resistor, pad side
Track pins			
vdde	Input/Output	vdde	IO power node (1.0V or 1.8V)
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node

2.3.3 Cell Information

Table 9 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (RES node)	-	-	50	Ω
I_{DC}	DC current Pad To Core [2]	110 ˚C (RES node)	-	-	3	mA
		125 ˚C (RES node)	-	-	1	
	DC current Pad To Core [2]	110 ˚C (RES node)	-	-	3	
		125 ˚C (RES node)	-	-	1	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (RES node)	-	-	7	mA
	RMS current Pad To Core [2]	100 ˚C (RES node)	-	-	7	
C_{Par}	Parasitic capacitance (without Bump)	Corner TT, 125 ˚C (IO node)	-	-	637	fF
	Parasitic capacitance (with BUMP_FC61A_96X96)	Corner TT, 125 ˚C (IO node)	-	-	692 [2]	
$I_{leakage}$	Leakage current	Fast process, Max voltage, 25 ˚C (vdde node)	-	-	12	pA
		Fast process, Max voltage, 125 ˚C (vdde node)	-	-	56	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

[3] The parasitic capacitance value depends on the type and the position of bump.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

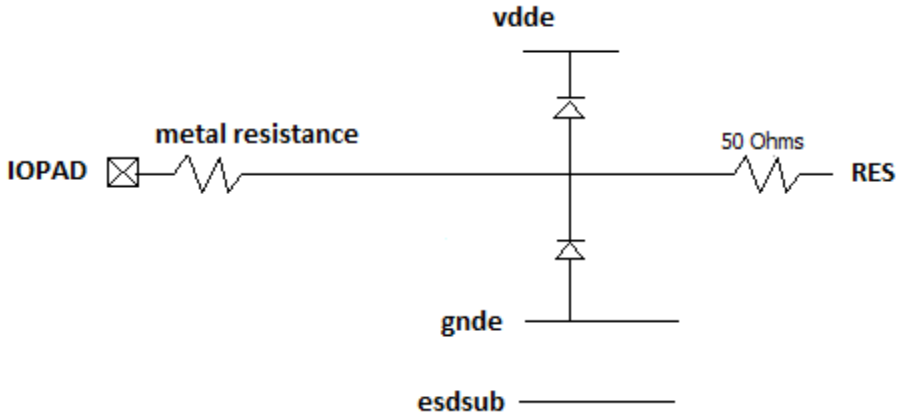
2.3.4 Functional Description

This cell is designed to interface analog signals between the core and the external domain. The analog signal to the core is connected to ANAIO pin through a 50 ohms resistor.

2.4 IO_20UM_3V3_50OHMS_EXT_ANA_FC_LIN / CL_LIN

2.4.1 Functional Diagram

Figure 5 : Block Diagram



2.4.2 Interface Description

Table 10 : Pin Description

Pin	Type	Voltage Level (V)	Description
Logic core pins			
RES	Input/Output	0 to vdde	Input node varying between vdde and gnde with series resistor, core side
Pad pin			
IOPAD	Input/Output	0 to vdde	Input node varying between vdde and gnde without series resistor, pad side
Track pins			
vdde	Input/Output	vdde	IO power node (3.3V)
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node

2.4.3 Cell Information

Table 11 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (RES node)	-	-	50	Ω
I_{DC}	DC current Pad To Core [1]	110 ˚C (RES node)	-	-	3	mA
		125 ˚C (RES node)	-	-	1	
	DC current Pad To Core [2]	110 ˚C (RES node)	-	-	3	
		125 ˚C (RES node)	-	-	1	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (RES node)	-	-	7	mA
	RMS current Pad To Core [2]	100 ˚C (RES node)	-	-	7	
C_{Par}	Parasitic capacitance (without Bump)	Corner TT, 125 ˚C (IO node)	-	-	362	fF
	Parasitic capacitance (with BUMP_FC61A_96X96)	Corner TT, 125 ˚C (IO node)	-	-	413 [2]	
$I_{leakage}$	Leakage current	Fast process, Max voltage, 25 ˚C (vdde node)	-	-	27	pA
		Fast process, Max voltage, 125 ˚C (vdde node)	-	-	214	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

[3] The parasitic capacitance value depends on the type and the position of bump.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

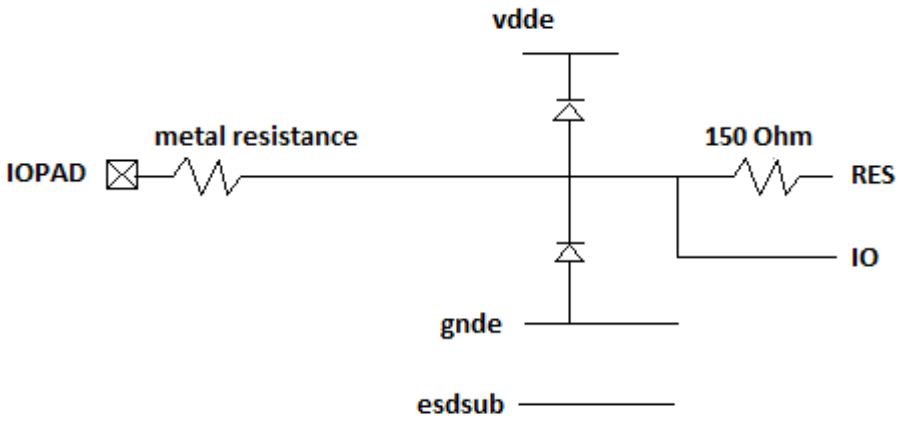
2.4.4 Functional Description

This cell is designed to interface analog signals between the core and the external domain. The analog signal to the core is connected to ANAIO pin through a 50 ohms resistor.

2.5 IO_UHF_EXT_ANA_FC_LIN / CL_LIN

2.5.1 Functional Diagram

Figure 6 : Block Diagram



2.5.2 Interface Description

Table 12 : Pin Description

Pin	Type	Voltage Level (V)	Description
Logic core pins			
RES	Input/Output	0 to vdde	Input node varying between vdde and gnde with series resistor, core side
IO	Input/Output	0 to vdde	Input node varying between vdde and gnde without series resistor, core side
Pad pin			
IOPAD	Input/Output	0 to vdde	Input node varying between vdde and gnde without series resistor, pad side
Track pins			
vdde	Input/Output	vdde	IO power node (1.8V or 3.3V)
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node

2.5.3 Cell Information

Table 13 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (IO node)	-	-	106	mΩ
		25 ˚C (RES node)	-	-	150	Ω
I_{DC}	DC current Pad To Core[1] [2]	110 ˚C (IO node)	-	-	57	mA
		125 ˚C (IO node)	-	-	33	
		110 ˚C (RES node)	-	-	3	
		125 ˚C (RES node)	-	-	1	
	DC current Pad To Core [2]	110 ˚C (IO node)	-	-	38	
		125 ˚C (IO node)	-	-	22	
		110 ˚C (RES node)	-	-	3	
		125 ˚C (RES node)	-	-	1	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (IO node)	-	-	33	mA
		100 ˚C (RES node)	-	-	7	
	RMS current Pad To Core [2]	100 ˚C (IO node)	-	-	33	
		100 ˚C (RES node)	-	-	7	
C_{Par}	Parasitic capacitance (without Bump)	Corner TT, PLS CMAX, 125 ˚C (IO node)	-	-	220	fF
	Parasitic capacitance (with BUMP_FC61A_96X96)	Corner TT, PLS CMAX, 125 ˚C (IO node)	-	-	287 [2]	
$I_{leakage}$	Leakage current	Fast process, Max voltage, 25 ˚C (vdde node)	-	-	27	pA
		Fast process, Max voltage, 125 ˚C (vdde node)	-	-	58	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

[3] The parasitic capacitance value depends of the type and the position of bump.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

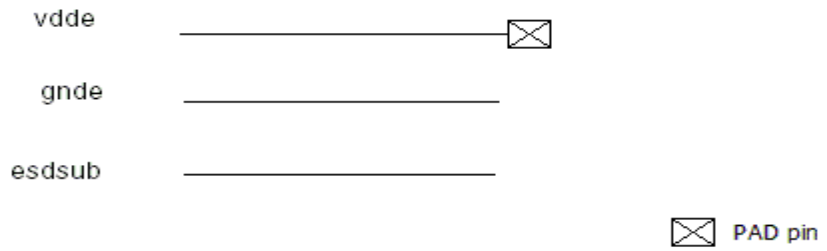
2.5.4 Functional Description

The IO_UHF_EXT_ANA_FC_LIN / CL_LIN cell is designed to interface ultra-high frequency analog signals between the core and external domain.

2.6 VDDE_NOESD_EXT_ANA_FC_LIN / CL_LIN

2.6.1 Functional Diagram

Figure 7 : Block Diagram



2.6.2 Interface Description

Table 14 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vdde	Input/Output	vdde	IO power node, pad side
Track and core pins			
vdde	Input/Output	vdde	IO power node
gnde	Input/Output	0	IO ground node, only track side
esdsub	Input/Output	0	Substrate ground node, only track side

2.6.3 Cell Information

Table 15 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to Core	25 ˚C (vdde node)	-	-	90	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vdde node)	-	-	145	mA
		125 ˚C (vdde node)	-	-	52	
	DC current Pad To Core [2]	110 ˚C (vdde node)	-	-	38	
		125 ˚C (vdde node)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (vdde node)	-	-	117	mA
	RMS current Pad To Core [2]	100 ˚C (vdde node)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

	DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2]. *DC/RMS current values of RDL should be checked accordingly at chip level.*

2.6.4 Functional Description

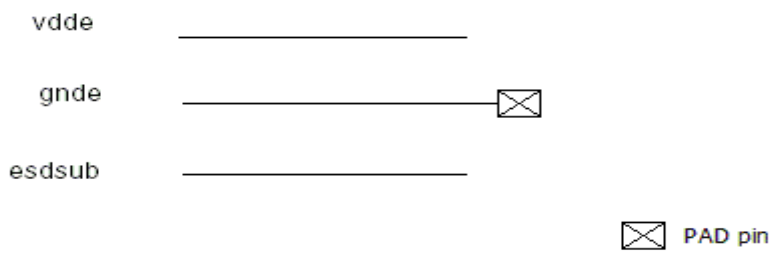
The VDDE_NOESD_EXT_ANA_FC_LIN / CL_LIN cell acts as a power pad, which provides bias to the power supply rail.

	The VDDE_NOESD_EXT_ANA_FC_LIN / CL_LIN cell does not contain ESD protection.

2.7 GNDE_NOESD_EXT_ANA_FC_LIN / CL_LIN

2.7.1 Functional Diagram

Figure 8 : Block Diagram



2.7.2 Interface Description

Table 16 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
gnde	Input/Output	0	IO ground node, pad side
Track and core pins			
vdde	Input/Output	vdde	IO power node
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node, only track side

2.7.3 Cell Information

Table 17 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to Core	25 ˚C (gnde node)	-	-	90	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (gnde node)	-	-	145	mA
		125 ˚C (gnde node)	-	-	52	
	DC current Pad To Core [2]	110 ˚C (gnde node)	-	-	38	
		125 ˚C (gnde node)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (gnde node)	-	-	117	mA
	RMS current Pad To Core [2]	100 ˚C (gnde node)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

2.7.4 Functional Description

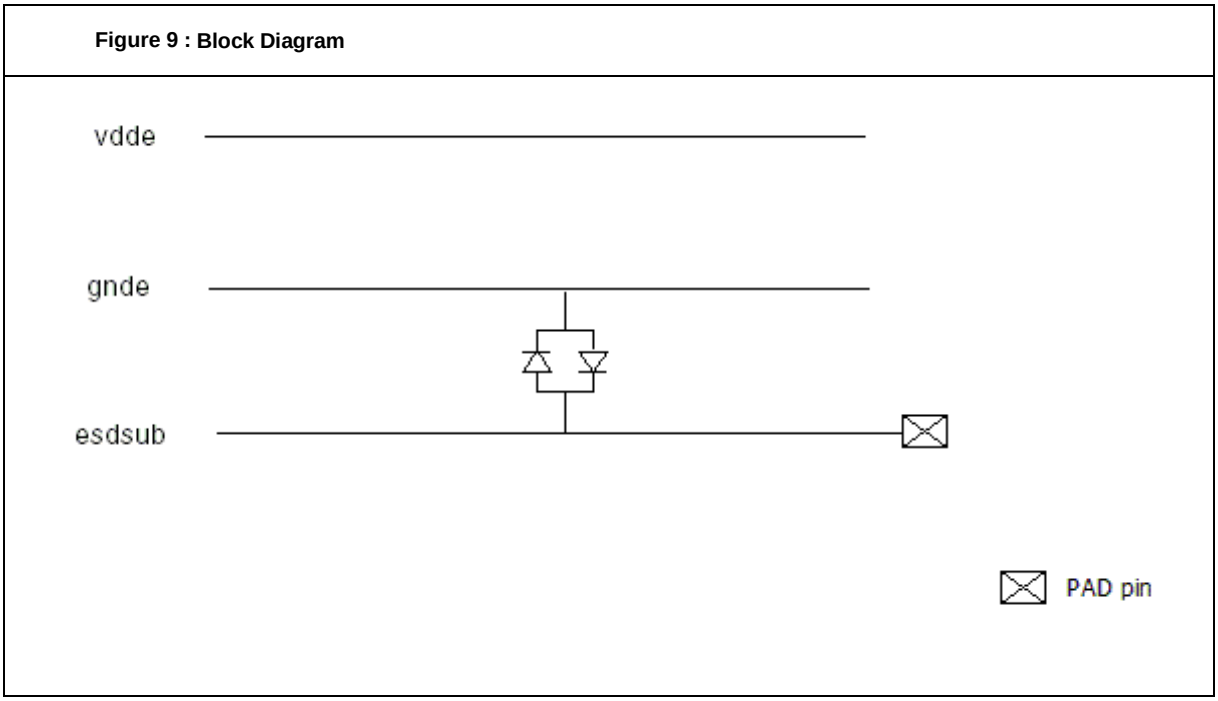
The GNDE_NOESD_EXT_ANA_FC_LIN / CL_LIN cell acts as a ground pad, which provides bias to the gnde ground supply rail.

The GNDE_NOESD_EXT_ANA_FC_LIN / CL_LIN cell does not contain ESD protection.

2.8 ESDSUB_EXT_ANA_FC_LIN / CL_LIN

2.8.1 Functional Diagram

Figure 9 : Block Diagram



2.8.2 Interface Description

Table 18 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
esdsub	Input/Output	0	Substrate ground node, pad side
Track and core pins			
vdde	Input/Output	vdde	IO power node, only track side
gnde	Input/Output	0	IO ground node, only track side
esdsub	Input/Output	0	Substrate ground node

2.8.3 Cell Information

Table 19 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (esdsub node)	-	-	90	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (esdsub node)	-	-	145	mA
		125 ˚C (esdsub node)	-	-	52	
	DC current Pad To Core [2]	110 ˚C (esdsub node)	-	-	38	
		125 ˚C (esdsub node)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (esdsub node)	-	-	117	mA
	RMS current Pad To Core [2]	100 ˚C (esdsub node)	-	-	103	
$I_{leakage}$	Leakage current	Fast process, Max voltage, 25 ˚C (vdde node)	-	-	< 150	pA
		Fast process, Max voltage, 125 °C (vdde node)	-	-	< 150	pA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

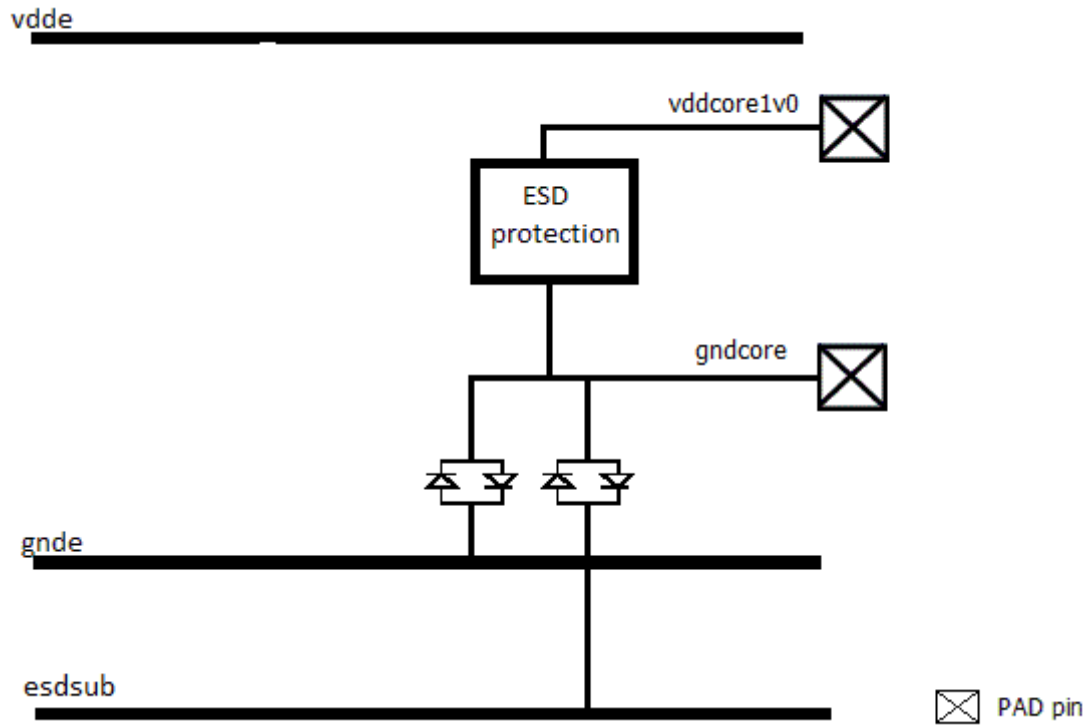
2.8.4 Functional Description

The ESDSUB_EXT_ANA_FC_LIN / CL_LIN cell acts as a ground pad, which provides bias to the esdsub ground supply rails and substrate.

2.9 VDDCORE_1V0_GNDCORE_EXT_ANA_FC_LIN / CL_LIN

2.9.1 Functional Diagram

Figure 10 : Block Diagram



2.9.2 Interface Description

Table 20 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, pad side
gndcore	Input / Output	0	Dedicated ground node, pad side
Track and core pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, only core side
gndcore	Input / Output	0	Dedicated ground node, only core side
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node, only track side
esdsub	Input / Output	0	Substrate ground node, only track side

2.9.3 Cell Information

Table 21 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vddcore1v0 and gndcore nodes)	-	-	54	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vddcore1v0 and gndcore nodes)	-	-	195	mA
		125 ˚C (vddcore1v0 and gndcore nodes)	-	-	71	
	DC current Pad To Core [2]	110 ˚C (vddcore1v0 and gndcore nodes)	-	-	38	mA
		125 ˚C (vddcore1v0 and gndcore nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (vddcore1v0 and gndcore nodes)	-	-	212	mA
	RMS current Pad To Core [2]	100 ˚C (vddcore1v0 and gndcore nodes)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v0 node)	-	-	64	nA
		Fast Process, Max voltage, 125 °C (vddcore1v0 node)	-	-	11	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

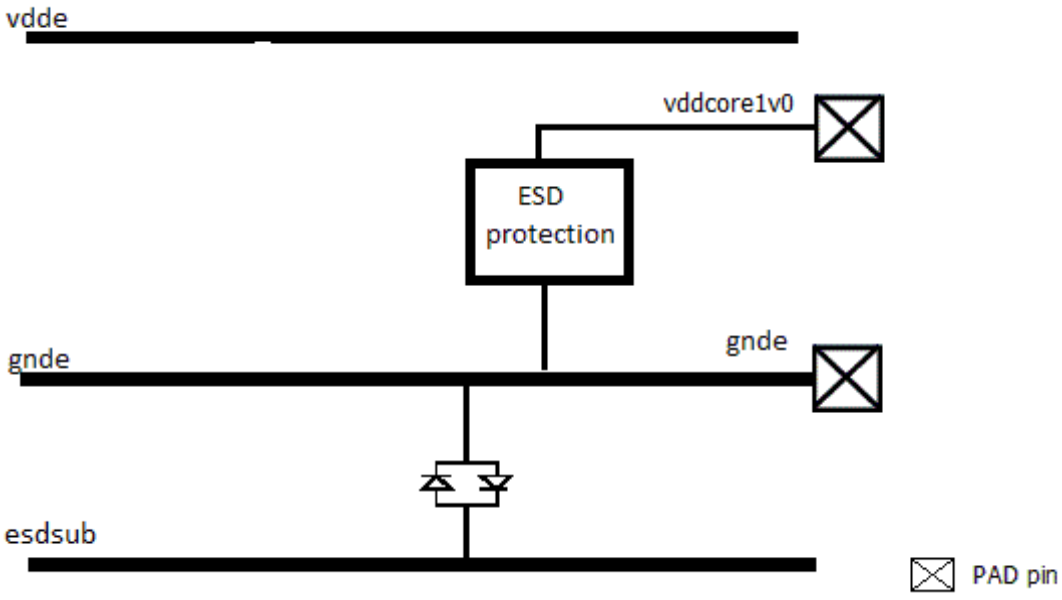
2.9.4 Functional Description

The VDDCORE_1V0_GNDCORE_EXT_ANA_FC_LIN / CL_LIN is a cell with dedicated 1.0 V power supply referring to a dedicated ground node

2.10 VDDCORE_1V0_GNDE_EXT_ANA_FC_LIN / CL_LIN

2.10.1 Functional Diagram

Figure 11 : Block Diagram



2.10.2 Interface Description

Table 22 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, pad side
gnde	Input / Output	0	IO ground node, pad side
Track and core pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node
esdsub	Input / Output	0	Substrate ground node, only track side

2.10.3 Cell Information

Table 23 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vddcore1v0 and gnde nodes)	-	-	54	mΩ
I_{DC}	DC current Pad To Core[2]	110 ˚C (vddcore1v0 and gnde nodes)	-	-	195	mA
		125 ˚C (vddcore1v0 and gnde nodes)	-	-	71	
	DC current Pad To Core [2]	110 ˚C (vddcore1v0 and gnde nodes)	-	-	38	mA
		125 ˚C (vddcore1v0 and gnde nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (vddcore1v0 and gnde nodes)	-	-	212	mA
	RMS current Pad To Core [2]	100 ˚C (vddcore1v0 and gnde nodes)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v0 node)	-	-	64	nA
		Fast Process, Max voltage, 125 °C (vddcore1v0 node)	-	-	11	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

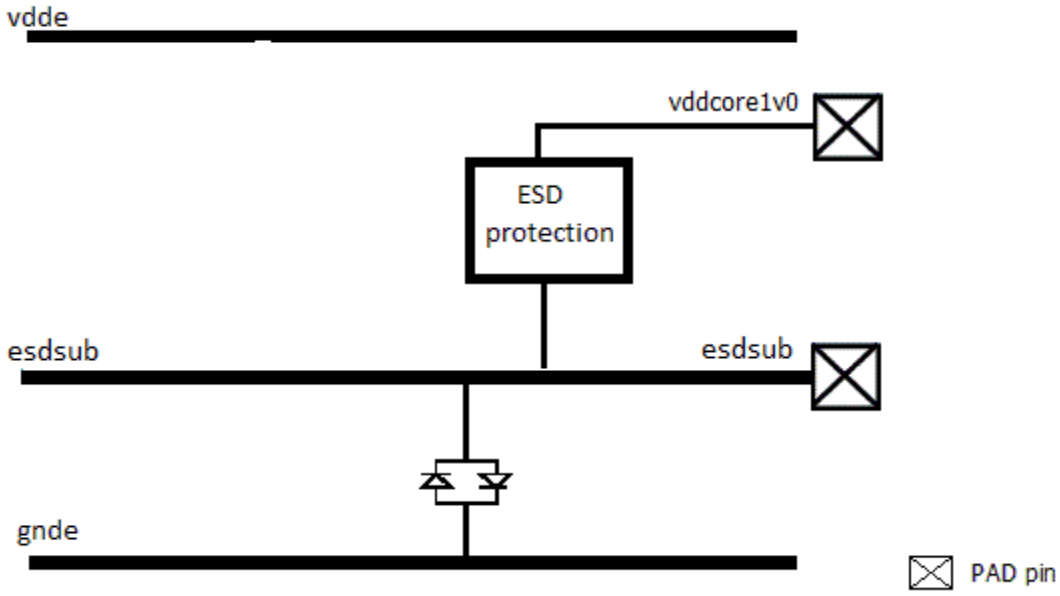
2.10.4 Functional Description

The VDDCORE_1V0_GNDE_EXT_ANA_FC_LIN / CL_LIN is a cell with dedicated 1.0 V power supply referring to gnde ground node

2.11 VDDCORE_1V0_ESDSUB_EXT_ANA_FC_LIN / CL_LIN

2.11.1 Functional Diagram

Figure 12 : Block Diagram



2.11.2 Interface Description

Table 24 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, pad side
esdsub	Input / Output	0	Substrate ground node, pad side
Track and core pins			
vddcore1v0	Input / Output	vddcore1v0	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node, only track side
esdsub	Input / Output	0	Substrate ground node

2.11.3 Cell Information

Table 25 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vddcore1v0 and esdsub nodes)	-	-	54	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vddcore1v0 and esdsub nodes)	-	-	195	mA
		125 ˚C (vddcore1v0 and esdsub nodes)	-	-	71	
	DC current Pad To Core [2]	110 ˚C (vddcore1v0 and esdsub nodes)	-	-	38	mA
		125 ˚C (vddcore1v0 and esdsub nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (vddcore1v0 and esdsub nodes)	-	-	212	mA
	RMS current Pad To Core [2]	100 ˚C (vddcore1v0 and esdsub nodes)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v0 node)	-	-	64	nA
		Fast Process, Max voltage, 125 °C (vddcore1v0 node)	-	-	11	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

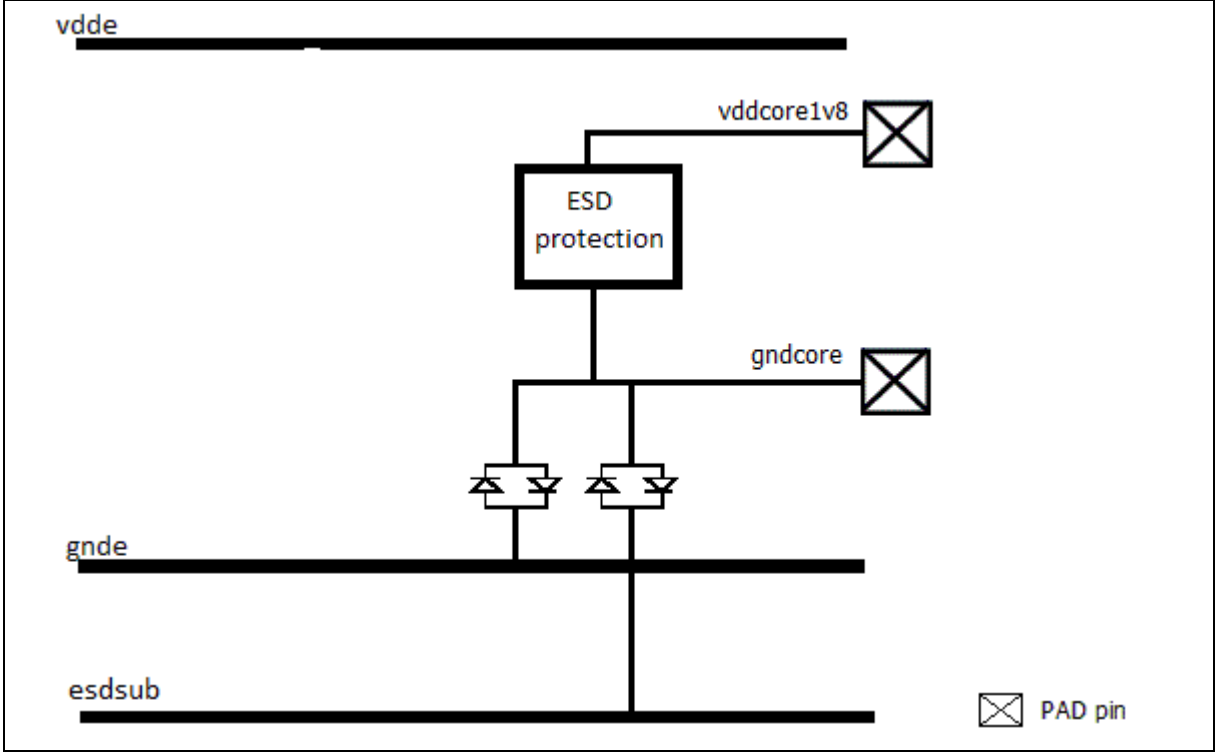
2.11.4 Functional Description

The VDDCORE_1V0_ESDSUB_EXT_ANA_FC_LIN / CL_LIN is a cell with dedicated 1.0 V power supply referring to esdsub ground node

2.12 VDDCORE_1V8_GNDCORE_EXT_ANA_FC_LIN / CL_LIN

2.12.1 Functional Diagram

Figure 13 : Block Diagram



2.12.2 Interface Description

Table 26 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, pad side
gndcore	Input / Output	0	Dedicated ground node, pad side
Track and core pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, only core side
gndcore	Input / Output	0	Dedicated ground node, only core side
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node, only track side
esdsub	Input / Output	0	Substrate ground node, only track side

2.12.3 Cell Information

Table 27 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vddcore1v8 and gndcore nodes)	-	-	54	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vddcore1v8 and gndcore nodes)	-	-	195	mA
		125 ˚C (vddcore1v8 and gndcore nodes)	-	-	71	
	DC current Pad To Core [2]	110 ˚C (vddcore1v8 and gndcore nodes)	-	-	38	mA
		125 ˚C (vddcore1v8 and gndcore nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (vddcore1v8 and gndcore nodes)	-	-	212	mA
	RMS current Pad To Core [2]	100 ˚C (vddcore1v8 and gndcore nodes)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v8 node)	-	-	495	nA
		Fast Process, Max voltage, 125 °C (vddcore1v8 node)	-	-	3.8	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

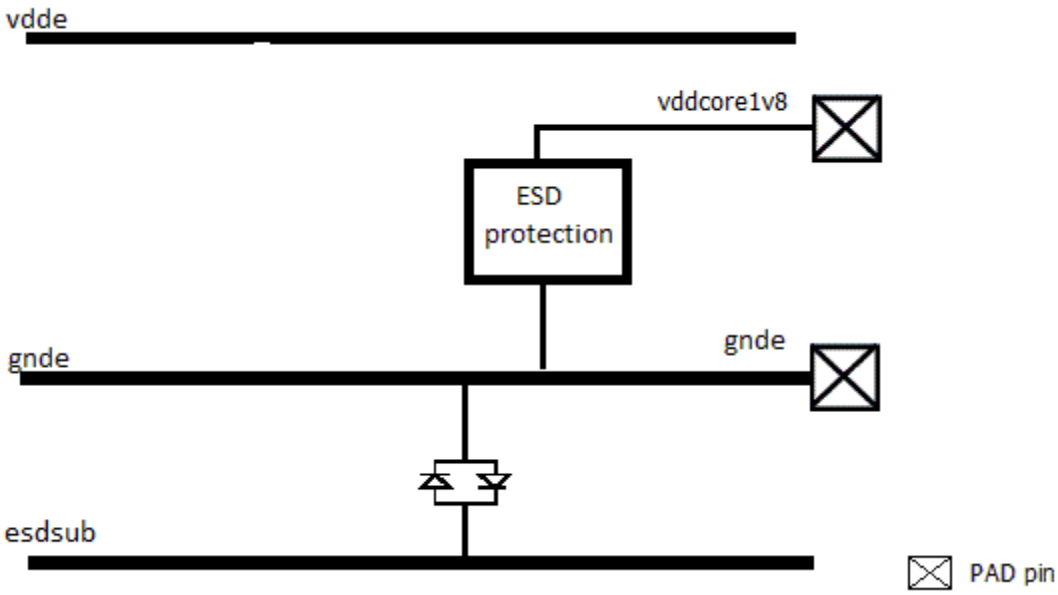
2.12.4 Functional Description

The VDDCORE_1V8_GNDCORE_EXT_ANA_FC_LIN / CL_LIN is a cell with dedicated 1.8 V power supply referring to a dedicated ground node

2.13 VDDCORE_1V8_GNDE_EXT_ANA_FC_LIN / CL_LIN

2.13.1 Functional Diagram

Figure 14 : Block Diagram



2.13.2 Interface Description

Table 28 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, pad side
gnde	Input / Output	0	IO ground node, pad side
Track and core pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node
esdsub	Input / Output	0	Substrate ground node, only track side

2.13.3 Cell Information

Table 29 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vddcore1v8 and gnde nodes)	-	-	54	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vddcore1v8 and gnde nodes)	-	-	195	mA
		125 ˚C (vddcore1v8 and gnde nodes)	-	-	71	
	DC current Pad To Core [2]	110 ˚C (vddcore1v8 and gnde nodes)	-	-	38	mA
		125 ˚C (vddcore1v8 and gnde nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (vddcore1v8 and gnde nodes)	-	-	212	mA
	RMS current Pad To Core [2]	100 ˚C (vddcore1v8 and gnde nodes)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v8 node)	-	-	495	nA
		Fast Process, Max voltage, 125 °C (vddcore1v8 node)	-	-	3.8	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

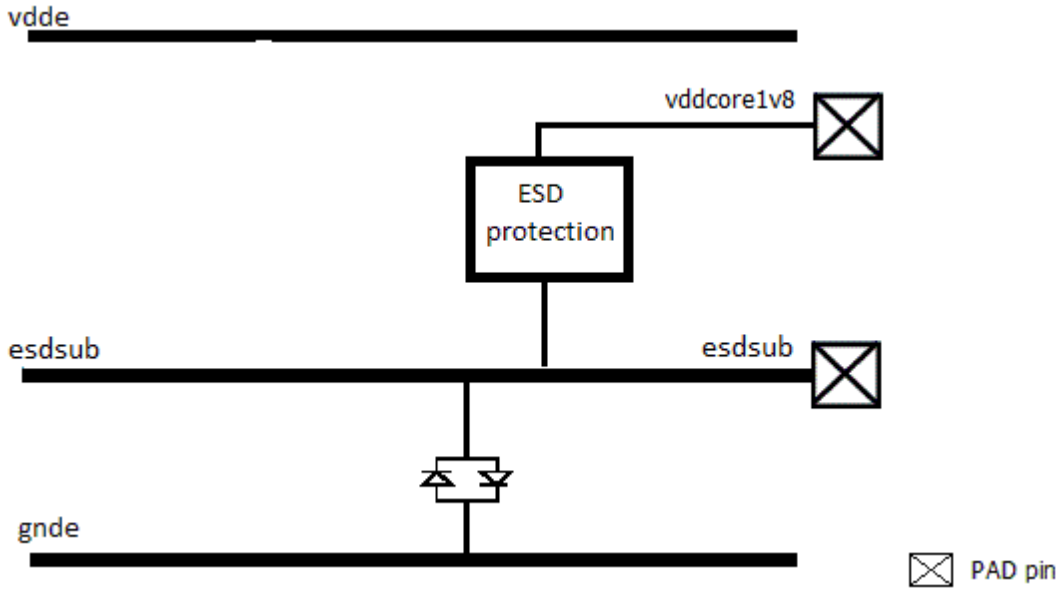
2.13.4 Functional Description

The VDDCORE_1V8_GNDE_EXT_ANA_FC_LIN / CL_LIN is a cell with dedicated 1.8 V power supply referring to gnde ground node

2.14 VDDCORE_1V8_ESDSUB_EXT_ANA_FC_LIN / CL_LIN

2.14.1 Functional Diagram

Figure 15 : Block Diagram



2.14.2 Interface Description

Table 30 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, pad side
esdsub	Input / Output	0	Common core ground node
Track and core pins			
vddcore1v8	Input / Output	vddcore1v8	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node, only track side
esdsub	Input / Output	0	Substrate ground node

2.14.3 Cell Information

Table 31 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vddcore1v8 and esdsub nodes)	-	-	54	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vddcore1v8 and esdsub nodes)	-	-	195	mA
		125 ˚C (vddcore1v8 and esdsub nodes)	-	-	71	
	DC current Pad To Core [2]	110 ˚C (vddcore1v8 and esdsub nodes)	-	-	38	mA
		125 ˚C (vddcore1v8 and esdsub nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (vddcore1v8 and esdsub nodes)	-	-	212	mA
	RMS current Pad To Core [2]	100 ˚C (vddcore1v8 and esdsub nodes)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore1v8 node)	-	-	495	nA
		Fast Process, Max voltage, 125 °C (vddcore1v8 node)	-	-	3.8	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

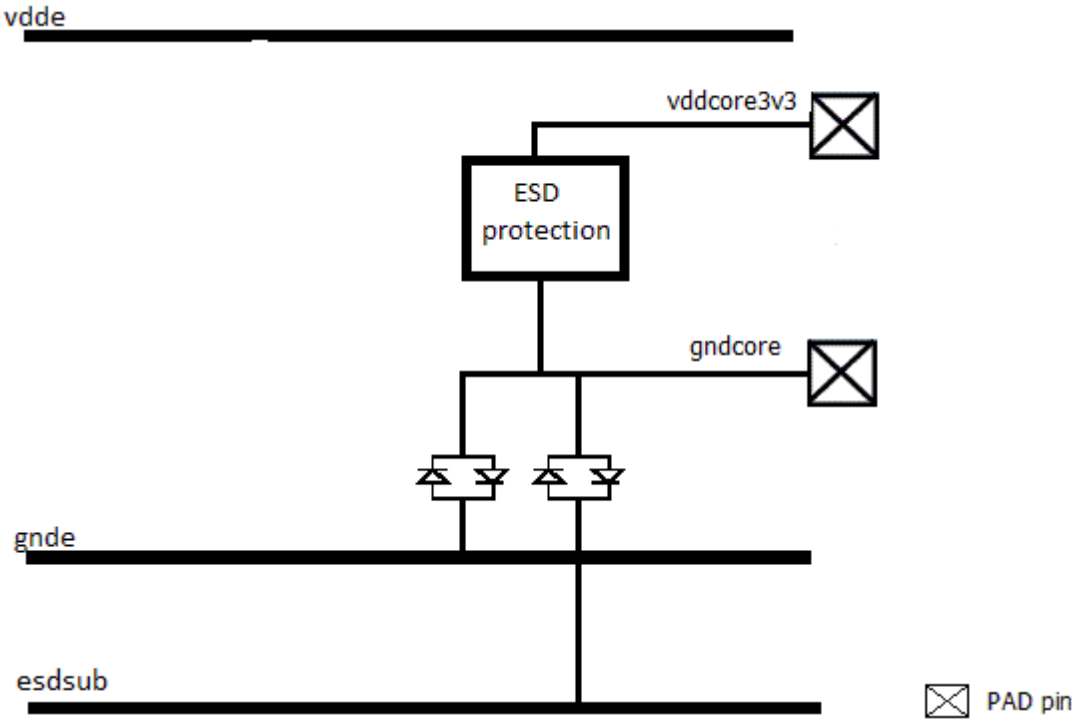
2.14.4 Functional Description

The VDDCORE_1V8_ESDSUB_EXT_ANA_FC_LIN / CL_LIN is a cell with dedicated 1.8 V power supply referring to esdsub ground node

2.15 VDDCORE_3V3_GNDCORE_EXT_ANA_FC_LIN / CL_LIN

2.15.1 Functional Diagram

Figure 16 : Block Diagram



2.15.2 Interface Description

Table 32 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, pad side
gndcore	Input / Output	0	Dedicated ground node, pad side
Track and core pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, only core side
gndcore	Input / Output	0	Dedicated ground node, only core side
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node, only track side
esdsub	Input / Output	0	Substrate ground node, only track side

2.15.3 Cell Information

Table 33 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vddcore3v3 and gndcore nodes)	-	-	47	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vddcore3v3 and gndcore nodes)	-	-	195	mA
		125 ˚C (vddcore3v3 and gndcore nodes)	-	-	75	
	DC current Pad To Core [2]	110 ˚C (vddcore3v3 and gndcore nodes)	-	-	38	mA
		125 ˚C (vddcore3v3 and gndcore nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (vddcore3v3 and gndcore nodes)	-	-	267	mA
	RMS current Pad To Core [2]	100 ˚C (vddcore3v3 and gndcore nodes)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vddcore3v3 node)	-	-	2.5	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

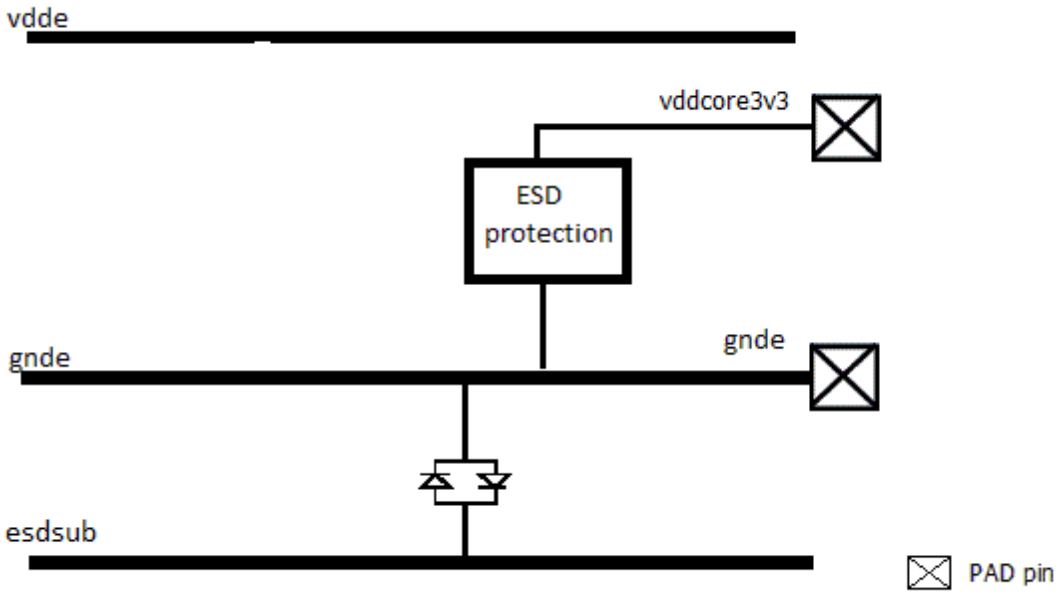
2.15.4 Functional Description

The VDDCORE_3V3_GNDCORE_EXT_ANA_FC_LIN / CL_LIN is a cell with dedicated 3.3 V power supply referring to a dedicated ground node

2.16 VDDCORE_3V3_GNDE_EXT_ANA_FC_LIN / CL_LIN

2.16.1 Functional Diagram

Figure 17 : Block Diagram



2.16.2 Interface Description

Table 34 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, pad side
gnde	Input / Output	0	IO ground node, pad side
Track and core pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node
esdsub	Input / Output	0	Substrate ground node, only track side

2.16.3 Cell Information

Table 35 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vddcore3v3 and gnde nodes)	-	-	47	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vddcore3v3 and gnde nodes)	-	-	195	mA
		125 ˚C (vddcore3v3 and gnde nodes)	-	-	75	
	DC current Pad To Core [2]	110 ˚C (vddcore3v3 and gnde nodes)	-	-	38	mA
		125 ˚C (vddcore3v3 and gnde nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (vddcore3v3 and gnde nodes)	-	-	267	mA
	RMS current Pad To Core [2]	100 ˚C (vddcore3v3 and gnde nodes)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vddcore3v3 node)	-	-	2.5	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

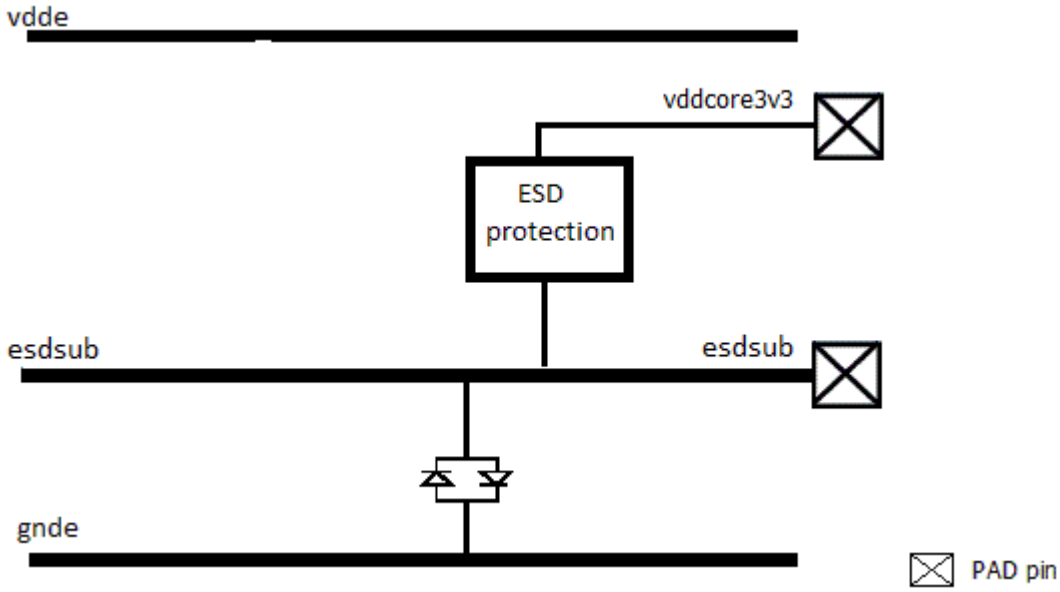
2.16.4 Functional Description

The VDDCORE_3V3_GNDE_EXT_ANA_FC_LIN / CL_LIN is a cell with dedicated 3.3 V power supply referring to gnde ground node

2.17 VDDCORE_3V3_ESDSUB_EXT_ANA_FC_LIN / CL_LIN

2.17.1 Functional Diagram

Figure 18 : Block Diagram



2.17.2 Interface Description

Table 36 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, pad side
esdsub	Input / Output	0	Substrate ground node, pad side
Track and core pins			
vddcore3v3	Input / Output	vddcore3v3	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node
gnde	Input / Output	0	IO ground node, only track side
esdsub	Input / Output	0	Substrate ground node

2.17.3 Cell Information

Table 37 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vddcore3v3 and esdsub nodes)	-	-	47	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vddcore3v3 and esdsub nodes)	-	-	195	mA
		125 ˚C (vddcore3v3 and esdsub nodes)	-	-	75	
	DC current Pad To Core [2]	110 ˚C (vddcore3v3 and esdsub nodes)	-	-	38	mA
		125 ˚C (vddcore3v3 and esdsub nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 ˚C (vddcore3v3 and esdsub nodes)	-	-	267	mA
	RMS current Pad To Core [2]	100 ˚C (vddcore3v3 and esdsub nodes)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vddcore3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vddcore3v3 node)	-	-	2.5	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

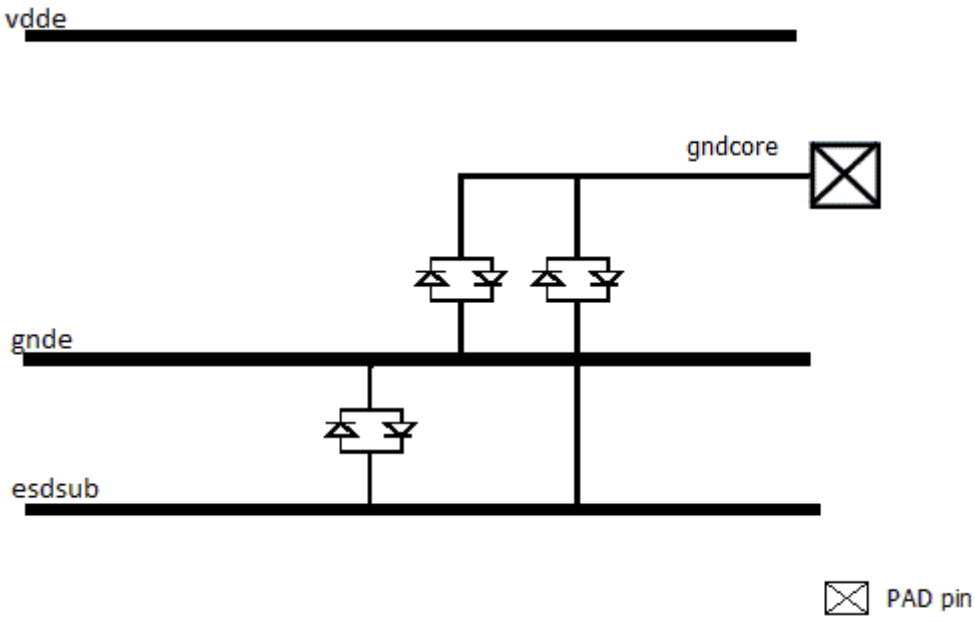
2.17.4 Functional Description

The VDDCORE_3V3_ESDSUB_EXT_ANA_FC_LIN / CL_LIN is a cell with dedicated 3.3 V power supply referring to esdsub ground node

2.18 GNDCORE_EXT_ANA_FC_LIN / CL_LIN

2.18.1 Functional Diagram

Figure 19 : Block Diagram



2.18.2 Interface Description

Table 38 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
gndcore	Input/Output	0	Dedicated ground node, pad side
Core pin			
gndcore	Input/Output	0	Dedicated ground node, core side
Track pins			
vdde	Input/Output	vdde	IO power node
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node

2.18.3 Cell Information

Table 39 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (gndcore node)	-	-	71	mΩ
I_{DC}	DC current Pad To Core[2]	110 ˚C (gndcore node)	-	-	115	mA
		125 ˚C (gndcore node)	-	-	41	
	DC current Pad To Core [2]	110 ˚C (gndcore node)	-	-	38	
		125 ˚C (gndcore node)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 °C (gndcore node)	-	-	103	mA
	RMS current Pad To Core [2]	100 ˚C (gndcore node)	-	-	103	
$I_{leakage}$	Leakage current	Fast process, Max voltage, 25 °C (vdde node)	-	-	< 150	pA
		Fast process, Max voltage, 125 ° C (vdde node)	-	-	< 150	pA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

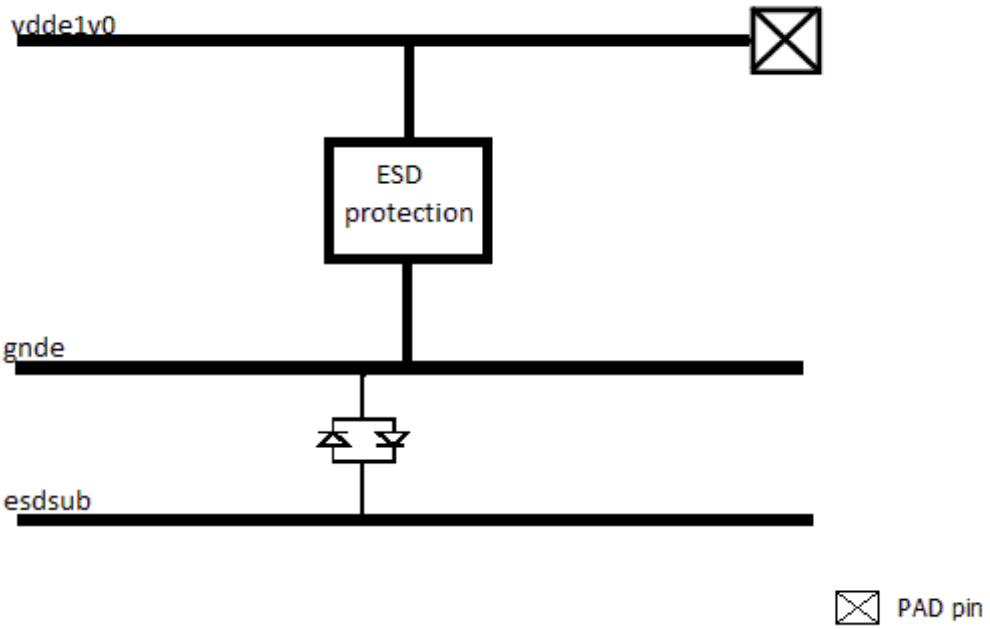
2.18.4 Functional Description

The GNDCORE_EXT_ANA_FC_LIN / CL_LIN dedicated ground supply cell can be used as separate core ground supply cell for core blocks requiring specific ground node.

2.19 VDDE_ESD_1V0_EXT_ANA_FC_LIN / CL_LIN

2.19.1 Functional Diagram

Figure 20 : Block Diagram



2.19.2 Interface Description

Table 40 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vdde1v0	Input/Output	vdde1v0	IO power node, pad side
Track and core pins			
vdde1v0	Input/Output	vdde1v0	IO power node
gnde	Input/Output	0	IO ground node, only track side
esdsub	Input/Output	0	Substrate ground node, only track side

2.19.3 Cell Information

Table 41 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vdde1v0 node)	-	-	90	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vdde1v0 node)	-	-	145	mA
		125 ˚C (vdde1v0 node)	-	-	52	
	DC current Pad To Core [2]	110 ˚C (vdde1v0 node)	-	-	38	
		125 ˚C (vdde1v0 node)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 °C (vdde1v0 node)	-	-	117	mA
	RMS current Pad To Core [2]	100 ˚C (vdde1v0 node)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vdde1v0 node)	-	-	22	nA
		Fast Process, Max voltage, 125 °C (vdde1v0 node)	-	-	3.9	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

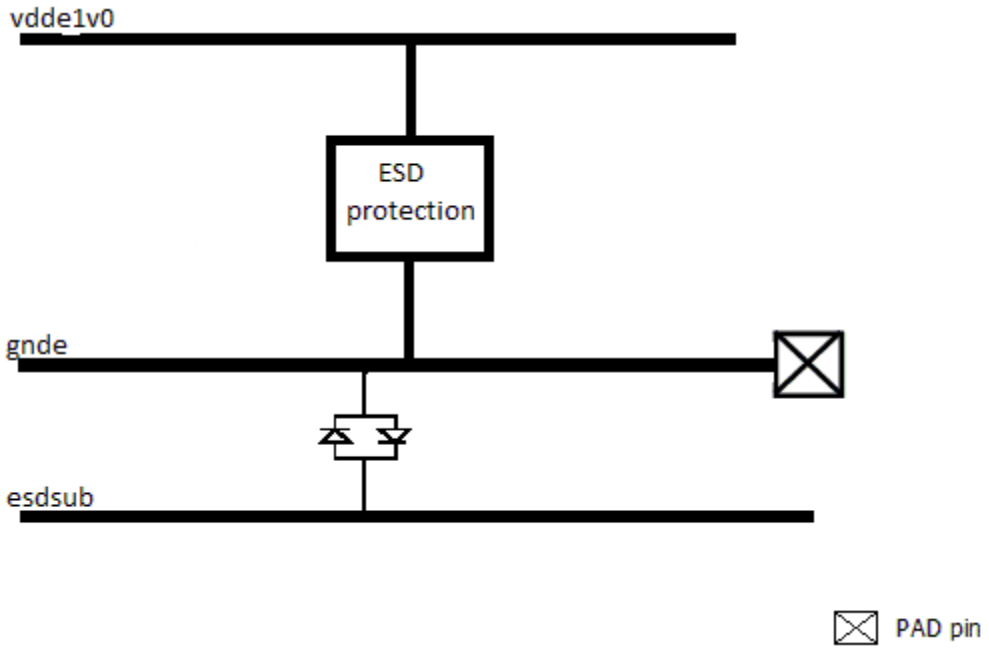
2.19.4 Functional Description

The VDDE_ESD_1V0_EXT_ANA_FC_LIN / CL_LIN cell acts as a power pad, which provides 1.0 V power supply to core, bias to the vdde1v0 power supply rails and ESD protection between vdde1v0 and gnde.

2.20 GNDE_ESD_1V0_EXT_ANA_FC_LIN / CL_LIN

2.20.1 Functional Diagram

Figure 21 : Block Diagram



2.20.2 Interface Description

Table 42 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
gnde	Input/Output	0	IO ground node, pad side
Track and core pins			
vdde1v0	Input/Output	vdde1v0	IO power node, only track side
gnde	Input/Output	0	IO ground supply node
esdsub	Input/Output	0	Substrate ground node, only track side

2.20.3 Cell Information

Table 43 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (gnde node)	-	-	90	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (gnde node)	-	-	145	mA
		125 ˚C (gnde node)	-	-	52	
	DC current Pad To Core [2]	110 ˚C (gnde node)	-	-	38	
		125 ˚C (gnde node)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 °C (gnde node)	-	-	117	mA
	RMS current Pad To Core [2]	100 ˚C (gnde node)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vdde1v0 node)	-	-	22	nA
		Fast Process, Max voltage, 125 °C (vdde1v0 node)	-	-	3.9	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

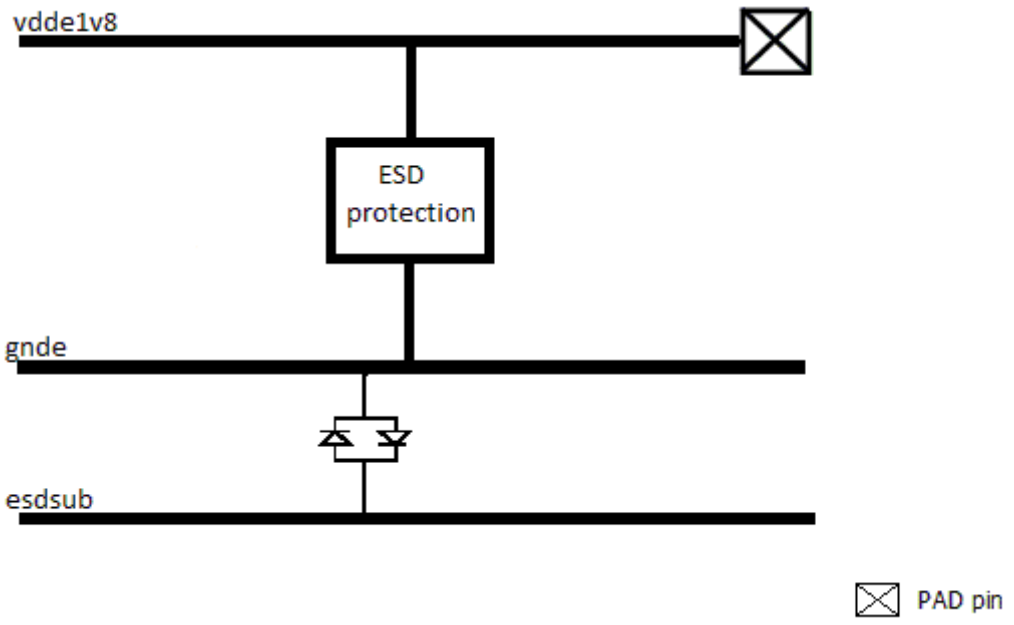
2.20.4 Functional Description

The GNDE_ESD_1V0_EXT_ANA_FC_LIN / CL_LIN cell acts as a ground pad, which provides ground supply to core, bias to the gnde ground supply rails and ESD protection between vdde1v0 and gnde.

2.21 VDDE_ESD_1V8_EXT_ANA_FC_LIN / CL_LIN

2.21.1 Functional Diagram

Figure 22 : Block Diagram



2.21.2 Interface Description

Table 44 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
vdde1v8	Input/Output	vdde1v8	IO power node, pad side
Track and core pin			
vdde1v8	Input/Output	vdde1v8	IO power node
gnde	Input/Output	0	IO ground node, only track side
esdsub	Input/Output	0	Substrate ground node, only track side

2.21.3 Cell Information

Table 45 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vdde1v8 node)	-	-	90	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vdde1v8 node)	-	-	145	mA
		125 ˚C (vdde1v8 node)	-	-	52	
	DC current Pad To Core [2]	110 ˚C (vdde1v8 node)	-	-	38	
		125 ˚C (vdde1v8 node)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 °C (vdde1v8 node)	-	-	117	mA
	RMS current Pad To Core [2]	100 ˚C (vdde1v8 node)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vdde1v8 node)	-	-	309	nA
		Fast Process, Max voltage, 125 °C (vdde1v8 node)	-	-	2.5	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

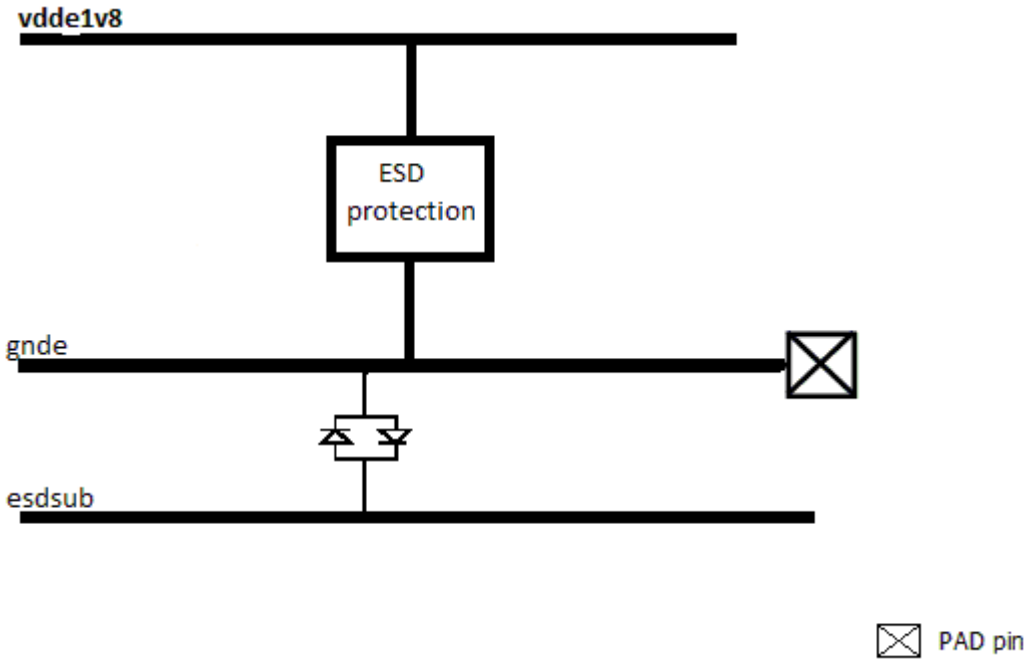
2.21.4 Functional Description

The VDDE_ESD_1V8_EXT_ANA_FC_LIN / CL_LIN cell acts as a power pad, which provides 1.8 V power supply to core, bias to the vdde1v8 power supply rail and ESD protection between vdde1v8 and gnde.

2.22 GNDE_ESD_1V8_EXT_ANA_FC_LIN / CL_LIN

2.22.1 Functional Diagram

Figure 23 : Block Diagram



2.22.2 Interface Description

Table 46 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pin			
gnde	Input/Output	0	IO ground node, pad side
Track and core pins			
vdde1v8	Input/Output	vdde1v8	IO power node, only track side
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node, only track side

2.22.3 Cell Information

Table 47 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (gnde node)	-	-	90	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (gnde node)	-	-	145	mA
		125 ˚C (gnde node)	-	-	52	
	DC current Pad To Core [2]	110 ˚C (gnde node)	-	-	38	
		125 ˚C (gnde node)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 °C (gnde node)	-	-	117	mA
	RMS current Pad To Core [2]	100 ˚C (gnde node)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vdde1v8 node)	-	-	309	nA
		Fast Process, Max voltage, 125 °C (vdde1v8 node)	-	-	2.5	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

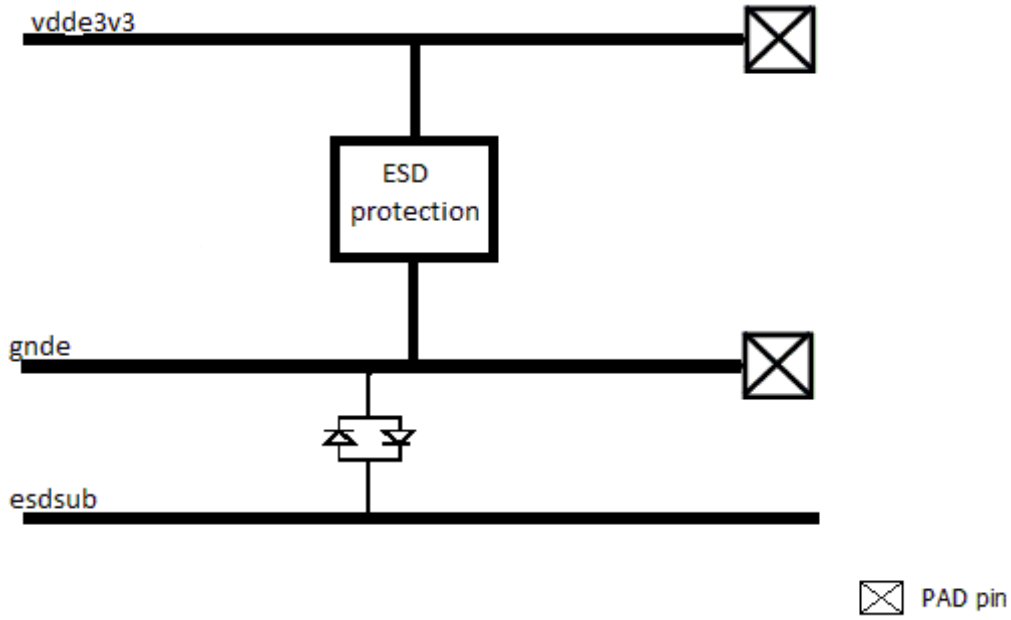
2.22.4 Functional Description

The GNDE_ESD_1V8_EXT_ANA_FC_LIN / CL_LIN cell acts as a ground pad, which provides ground supply to core, bias to the gnde ground supply rail and ESD protection between vdde1v8 and gnde.

2.23 VDDE_GNDE_ESD_3V3_EXT_ANA_FC_LIN / CL_LIN

2.23.1 Functional Diagram

Figure 24 : Block Diagram



2.23.2 Interface Description

Table 48 : Pin Description

Pin	Type	Voltage Level (V)	Description
Pad pins			
vdde3v3	Input/Output	vdde3v3	IO power node, pad side
gnde	Input/Output	0	IO ground node, pad side
Track and core pins			
vdde3v3	Input/Output	vdde3v3	IO power node
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node, only track side

2.23.3 Cell Information

Table 49 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$R_{PadToCore}$	Resistance Pad to core	25 ˚C (vdde3v3 node)	-	-	267	mΩ
I_{DC}	DC current Pad To Core [2]	110 ˚C (vdde3v3 and gnde nodes)	-	-	195	mA
		125 ˚C (vdde3v3 and gnde nodes)	-	-	75	
	DC current Pad To Core [2]	110 ˚C (vdde3v3 and gnde nodes)	-	-	38	
		125 ˚C (vdde3v3 and gnde nodes)	-	-	22	
I_{RMS}	RMS current Pad To Core [2]	100 °C (vdde3v3 and gnde nodes)	-	-	47	mA
	RMS current Pad To Core [2]	100 ˚C (vdde3v3 and gnde nodes)	-	-	103	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vdde3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vdde3v3 node)	-	-	2.5	µA

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].

DC/RMS current values of RDL should be checked accordingly at chip level.

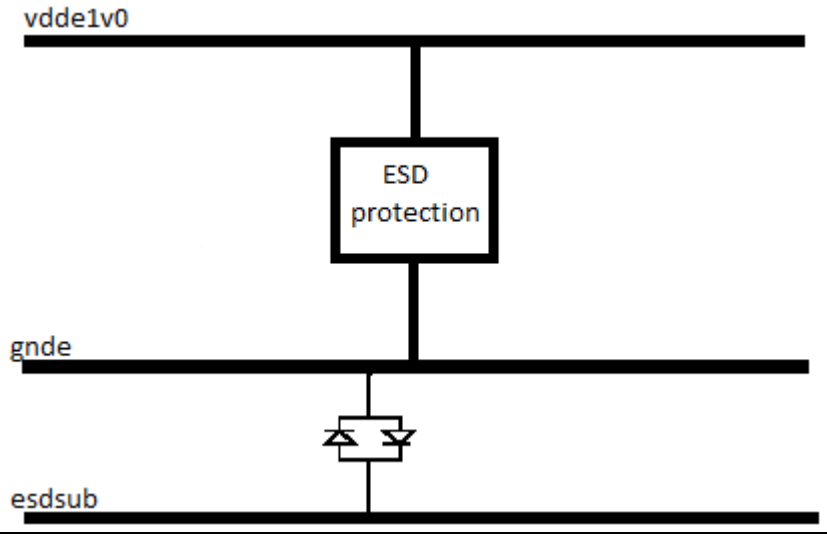
2.23.4 Functional Description

The VDDE_GNDE_ESD_3V3_EXT_ANA_FC_LIN / CL_LIN cell acts as a power and ground pad. It provides 3.3 V power supply and ground to core, and ESD protection between vdde3v3 and gnde.

2.24 FILLCELL_ESD_1V0_EXT_ANA_FC_LIN / CL_LIN

2.24.1 Functional Diagram

Figure 25 : Block Diagram



2.24.2 Interface Description

Table 50 : Pin Description

Pin	Type	Voltage Level (V)	Description
Track pins			
vdde1v0	Input/Output	vdde1v0	IO power node
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node

2.24.3 Cell Information

Table 51 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vdde1v0 node)	-	-	22	nA
		Fast Process, Max voltage, 125 °C (vdde1v0 node)	-	-	3.9	µA

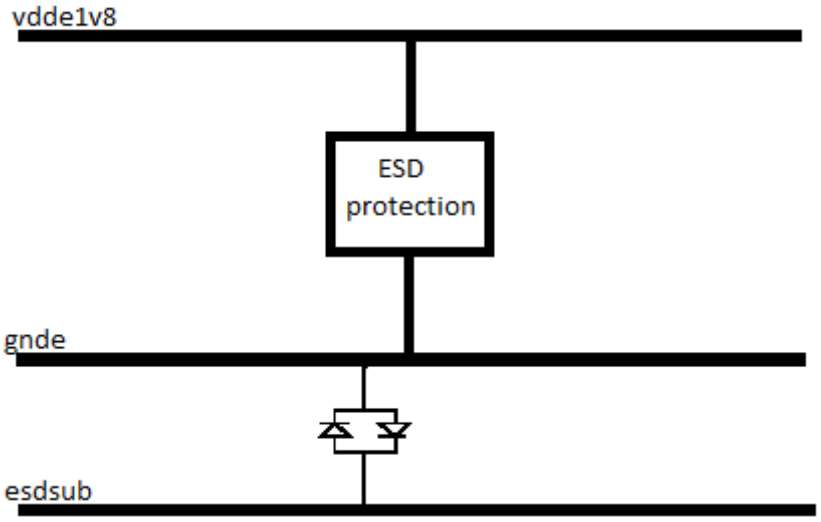
2.24.4 Functional Description

The FILLCELL_ESD_1V0_EXT_ANA_FC_LIN / CL_LIN cell is designed to provide ESD protection between vdde1v0 and gnde.

2.25 FILLCELL_ESD_1V8_EXT_ANA_FC_LIN / CL_LIN

2.25.1 Functional Diagram

Figure 26 : Block Diagram



2.25.2 Interface Description

Table 52 : Pin Description

Pin	Type	Voltage Level (V)	Description
Track pins			
vdde1v8	Input/Output	vdde1v8	IO power node
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node

2.25.3 Cell Information

Table 53 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vdde1v8 node)	-	-	309	nA
		Fast Process, Max voltage, 125 °C (vdde1v8 node)	-	-	2.5	µA

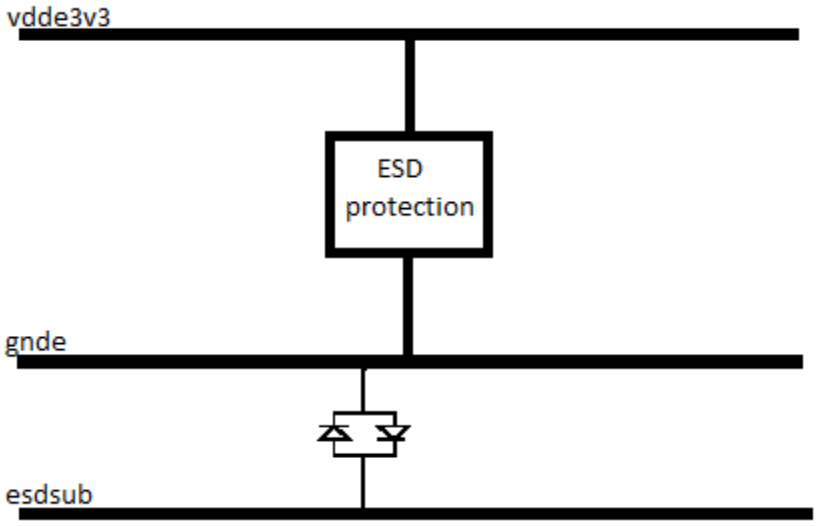
2.25.4 Functional Description

The FILLCELL_ESD_1V8_EXT_ANA_FC_LIN / CL_LIN cell is designed to provide ESD protection between vdde1v8 and gnde.

2.26 FILLCELL_ESD_3V3_EXT_ANA_FC_LIN / CL_LIN

2.26.1 Functional Diagram

Figure 27 : Block Diagram



2.26.2 Interface Description

Table 54 : Pin Description

Pin	Type	Voltage Level (V)	Description
Track pins			
vdde3v3	Input/Output	vdde3v3	IO power node
gnde	Input/Output	0	IO ground node
esdsub	Input/Output	0	Substrate ground node

2.26.3 Cell Information

Table 55 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (vdde3v3 node)	-	-	281	nA
		Fast Process, Max voltage, 125 °C (vdde3v3 node)	-	-	2.5	µA

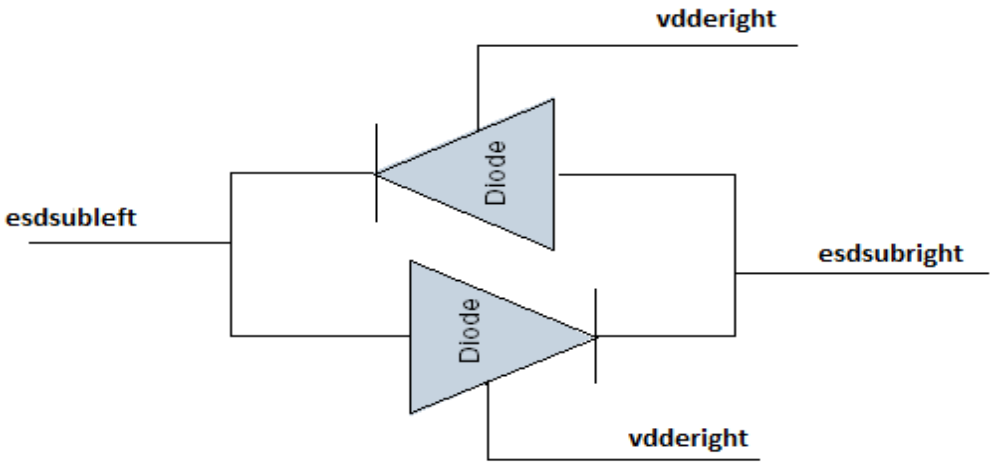
2.26.4 Functional Description

The FILLCELL_ESD_3V3_EXT_ANA_FC_LIN / CL_LIN cell is designed to provide ESD protection between vdde3v3 and gnde.

2.27 FILLCUTCELL_ALL_EXT_ANA_FC_LIN

2.27.1 Functional Diagram

Figure 28 : Block Diagram



2.27.2 Interface Description

Table 56 : Pin Description

Pin	Type	Voltage Level (V)	Description
esdsubleft	Input/Output	0	Substrate ground node on left side
esdsubright	Input/Output	0	Substrate ground node on right side
vdderight	Input/Output	vdde	IO power node on right side

2.27.3 Cell Information

Table 57 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 ˚C (vdderight node)	-	-	< 150	pA
		Fast Process, Max voltage, 125 ˚C (vdderight node)	-	-	< 150	

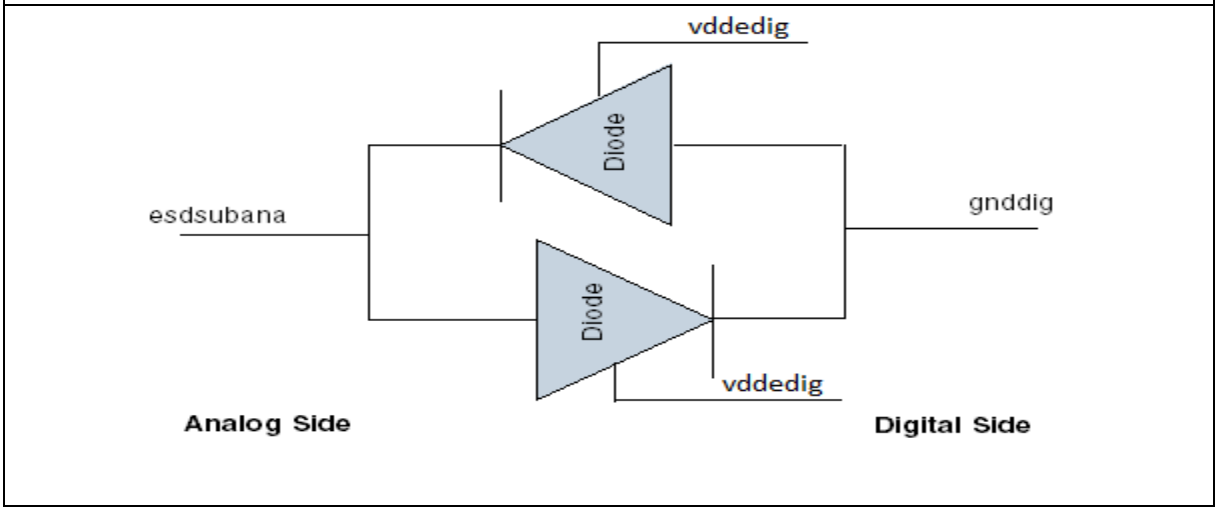
2.27.4 Functional Description

The FILLCUTCELL_ALL_EXT_ANA_FC_LIN cell is designed to cut all supply rails. ESD continuity is ensured through B2B diodes on the discontinued esdsub metal rail.

2.28 FILLCELL_STEP_BTB_EXT_ANAF_TO_CSF_FC_LIN

2.28.1 Functional Diagram

Figure 29 : Block Diagram



2.28.2 Interface Description

Table 58 : Pin Description

Pin	Type	Voltage Level (V)	Description
gnddig	Input/Output	0	Core, substrate ground and ESD reference node on digital side
esdsubana	Input/Output	0	Substrate ground and ESD reference node on analog side
vddedig	Input/Output	vdde	IO power node on digital side (1.2 V or 1.8 V)

2.28.3 Cell Information

Table 59 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 ˚C (vddedig node)	-	-	< 150	pA
		Fast Process, Max voltage, 125 ˚C (vddedig node)	-	-	< 150	

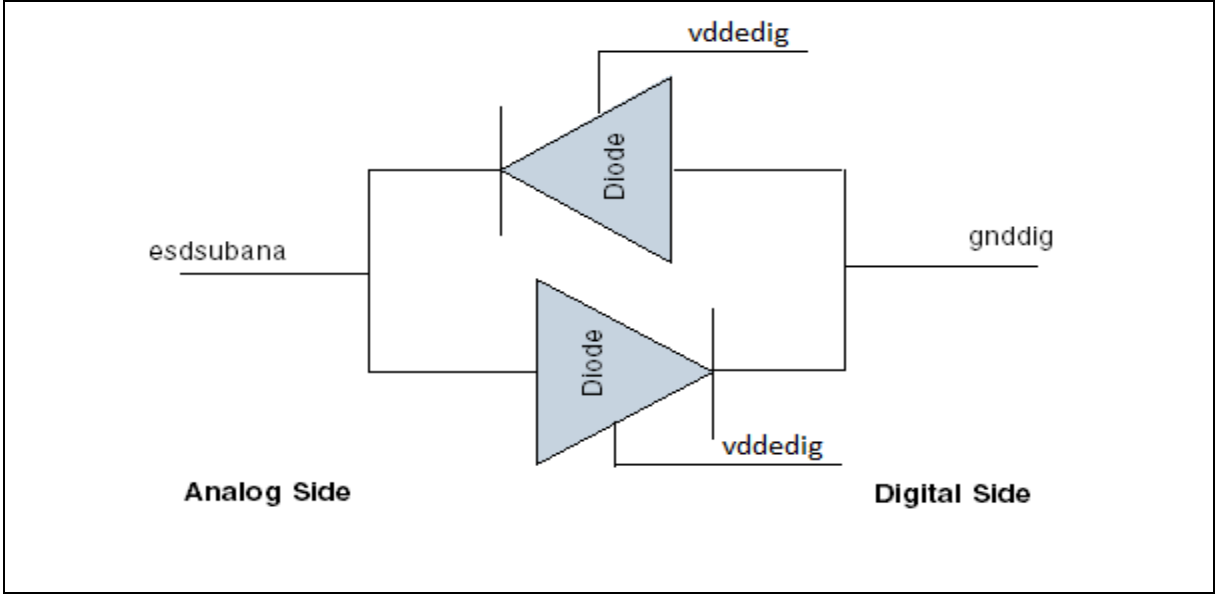
2.28.4 Functional Description

The FILLCELL_STEP_BTB_EXT_ANAF_TO_CSF_FC_LIN cuts all rails and ensures the ring transition from ANAF frame to CSF one. ESD continuity is ensured through B2B diodes between esdsub ground node from ANAF frame and gnd ground node from digital CSF frame.

2.29 FILLCELL_STEP_BTB_EXT_ANAF_TO_CSF_FC_2ROWS

2.29.1 Functional Diagram

Figure 30 : Block Diagram



2.29.2 Interface Description

Table 60 : Pin Description

Pin	Type	Voltage Level (V)	Description
gnddig	Input/Output	0	Core, substrate ground and ESD reference node on digital side
esdsubana	Input/Output	0	Substrate ground and ESD reference node on analog side
vddedig	Input/Output	vdde	IO power node on digital side (1.2V or 1.8V)

2.29.3 Cell Information

Table 61 : Cell Information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 ˚C (vddedig node)	-	-	< 150	pA
		Fast Process, Max voltage, 125 ˚C (vddedig node)	-	-	< 150	

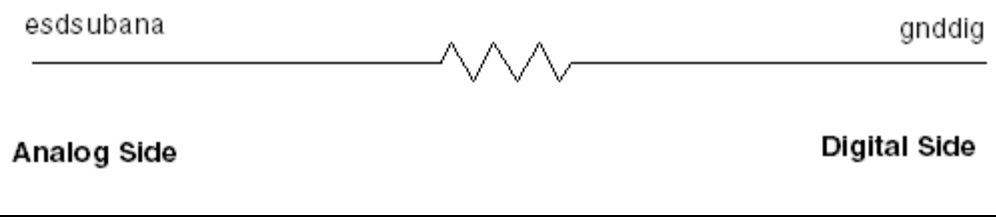
2.29.4 Functional Description

The FILLCELL_STEP_BTB_EXT_ANAF_TO_CSF_FC_2ROWS cuts all rails and ensures the ring transition from ANAF frame to CSF 2ROWS one. ESD continuity is ensured through B2B diodes between esdsub ground node from ANAF frame and gnd ground node from digital CSF frame.

2.30 FILLCELL_STEP_BTB_EXT_ANAF_TO_CSF_FC_LIN / 2ROWS

2.30.1 Functional Diagram

Figure 31 : Block Diagram



2.30.2 Interface Description

Table 62 : Pin Description

Pin Name	Type	Voltage Level (V)	Description
gnddig	Input/Output	0	Core, substrate ground and ESD reference node on digital side
esdsubana	Input/Output	0	Substrate ground and ESD reference node on analog side

2.30.3 Functional Description

The FILLCELL_STEP_BTB_EXT_ANAF_TO_CSF_FC_LIN / 2ROWS ensure the ring transition from ANAF frame to CSF/ CSF_2ROWS one. It cuts all rails and provides connection between esdsub ground node from ANAF frame and gnd ground node from CSF frame.

2.31 FILLCUTCELL_VDDE_EXT_ANA_FC_LIN / CL_LIN

2.31.1 Functional Description

The FILLCUTCELL_VDDE_EXT_ANA_FC_LIN / CL_LIN cell is designed to cut vdde rail only.

2.32 FILLCUTCELL_GNDE_EXT_ANA_FC_LIN / CL_LIN

2.32.1 Functional Description

The FILLCUTCELL_GNDE_EXT_ANA_FC_LIN / CL_LIN cell is designed to cut gnde rail only.

2.33 FILLCELL_1GRID / 1UM / 5UM / 10UM_EXT_ANA_FC_LIN / CL_LIN

2.33.1 Functional Description

The FILLCELL_1GRID / 1UM / 5UM / 10UM_EXT_ANA_FC_LIN / CL_LIN cells are designed to propagate supplies through the rails in the IO ring.

2.34 CORNERCELL_EXT_ANA_FC_LIN

2.34.1 Functional Description

The CORNERCELL_EXT_ANA_FC_LIN cell is instantiated at the corner of the chip in order to make the rails continuous. Same cell can be used for any CORNER of the chip.

2.35 FILLCELL_FEEDTHROUGH_EXT_ANA_CL_LIN

2.35.1 Functional Description

The FILLCELL_FEEDTHROUGH_EXT_ANA_CL_LIN cell is provided to allow routing through an analog IO cluster via M2/M3/M4

2.36 FILLCELL_END_LEFT / RIGHT_EXT_ANA_FC_LIN / CL_LIN

2.36.1 Functional Description

The purpose of FILLCELL_END_LEFT / RIGHT_EXT_ANA_FC_LIN / CL_LIN is to provide a latch-up guard ring. It provides pins for vdde and esdsub. These fillers are mandatory at the two edges of an analog IO cluster.

3.Electrical Specifications

3.1 ESD and Latch-up Characteristics

Table 63 : ESD and Latch-up Characteristics

Symbol	Parameter	Conditions	Target	Unit
V_{ESD}	Electrostatic discharge voltage	Human Body Model (HBM) [2]	2000	V
		Machine Model (MM) [2]	100	V
		Charge Device Model (CDM) [2] Full library except IO_UHF_XX / IO_20UM_XX[3] and 1V0 Dedicated supplies [4] (VDDCORE_1V0_XX)	500 V JEDEC	V
$I_{latchup}$	Injection current	Maximum operating junction temperature 125 ˚C [2]	200	mA
	Over-voltage stress		1.5 * vdde max	V

[1] ESD qualification: according to electrostatic discharge sensitivity measurement

[2] Latch-up qualification: according to latch-up sensitivity measurement

[3] For CDM target for IO_UHF_XX and IO_20UM_XX please refer to the table 65 ‘Supplies and IOs usage summary’ in the ‘IO placement’ section

[4] One VDDCORE_1V0_XX dedicated supply support 250 V CDM. For 500V CDM, 1V0 dedicated supply must be placed by pair. For such usage, please refer to the section ‘Dedicated supply Placement Rules’ below

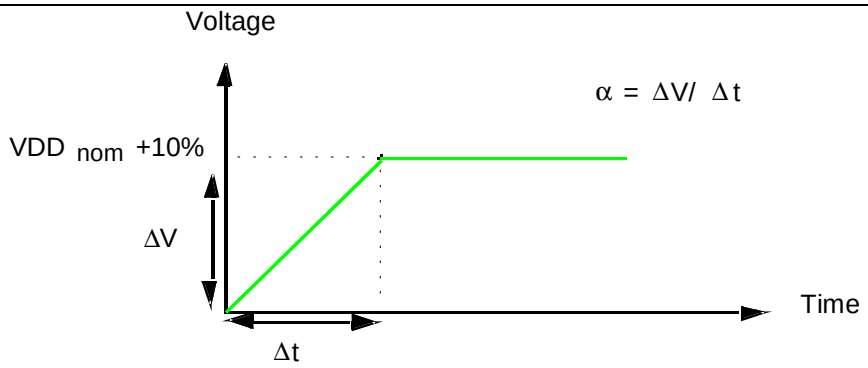
The level of CDM current seen at a given pre-charge voltage varies significantly with the chip size and package type. For instance, larger dies/packages generates higher CDM current.

However, this package size dependence has been considered during IO qualification, so that the above CDM commitment remains valid for any die/package size (even for large die/package sizes of hundreds of mm^2).

3.2 ESD Clamps Power-up Sensitivity

For correct power-up sequence without parasitic clamp switch-on, it is necessary to limit the power rise time as per next table.

Figure 32 : ESD Clamp Power Up Sensitivity



Power Ramp-Up should be equal or slower than 0.5V/us.

4.Usage Guidelines

4.1 Design Requirements

The C28SOI_IO_EXT_ANAF_ANA_EG library supports the construction of analog IO ring or analog IO cluster in single row configuration. Physical implementation

4.1.1 General placement rules

All cells in this library have their origin at (0, 0) and the 'PR boundary' abutted to the origin axes. The strategy to build the IO pad ring or the IO cluster is to abut laterally 'PR boundary' layers.

	*The rails of the IO pad ring should not be modified. Only the appropriate filler cut cells supplied within the library should be used. Non-compliance of this constraint disengages the responsibility of the IO supplier and prevents final implementation for full solution / services and support that could be provided for this deliverable.*
	*Please be aware that, for ANAF analog frame, there are no differences between FC cells and CL cells. Only their names are different.*

4.1.2 Constructing the Analog IO Ring

This library is self-sufficient for analog IO ring construction. It includes analog IOs, supplies, corners, fillers and fillercut cells required for this purpose.

4.1.3 Constructing the Analog IO cluster

The cells used at core side to construct an analog IO cluster section are CL_LIN cells. The only constraint is to place the FILLCELL_END_LEFT_EXT_ANA_CL_LIN and FILLCELL_END_RIGHT_EXT_ANA_CL_LIN respectively at the left and right edges of the analog IO cluster ring.

To route through the analog IO cluster only FILLCELL_FEEDTHROUGH_EXT_ANA_CL_LIN can be used.

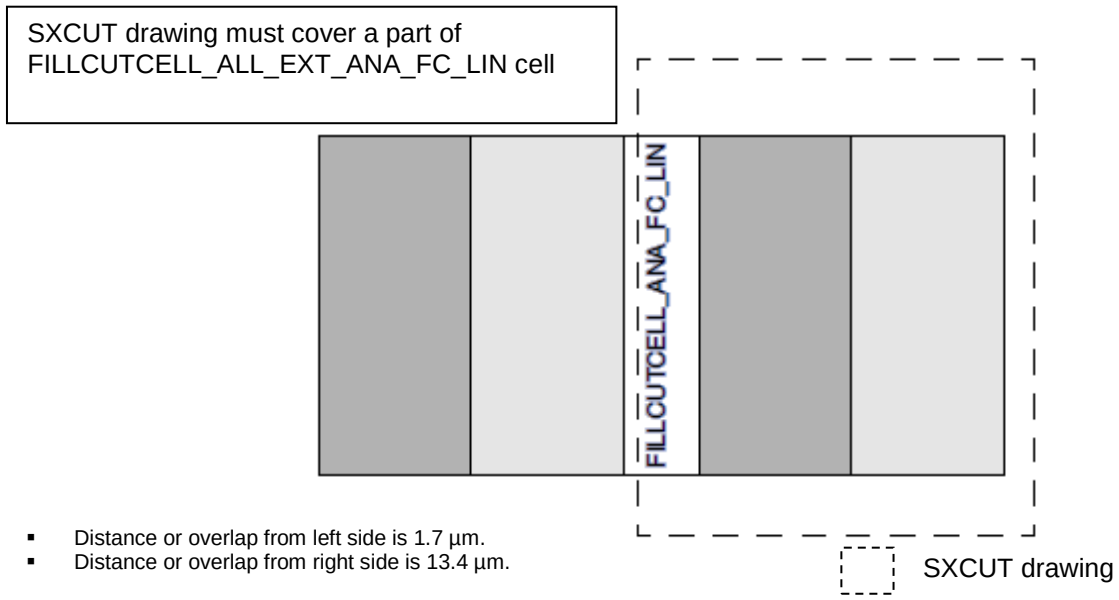
4.1.4 Filler cells usage

	*For tiling optimization reasons:* ▪ *All spaces between IOs should be filled by the larger filler cells available.* ▪ *FILLCELL_1GRID_EXT_ANA_FC_LIN / CL_LIN and FILLCELL_1UM_EXT_ANA_FC_LIN / CL_LIN cells must not be used to fill in gaps larger than 5 µm.*

4.1.5 FILLCUTCELL_ALL usage

When using FILLCUTCELL_ALL_EXT_ANA_FC_LIN cell, please consider that the substrate node on the right side (esdsubright) is different than the substrate node on the left side (esdsubleft). Therefore, one of the substrate polarization must be isolated using the marker layer, SXCUT drawing.

Figure 33 : Using SXCUT Drawing with FILLCUTCELL_ALL_EXT_ANA_FC_LIN cell

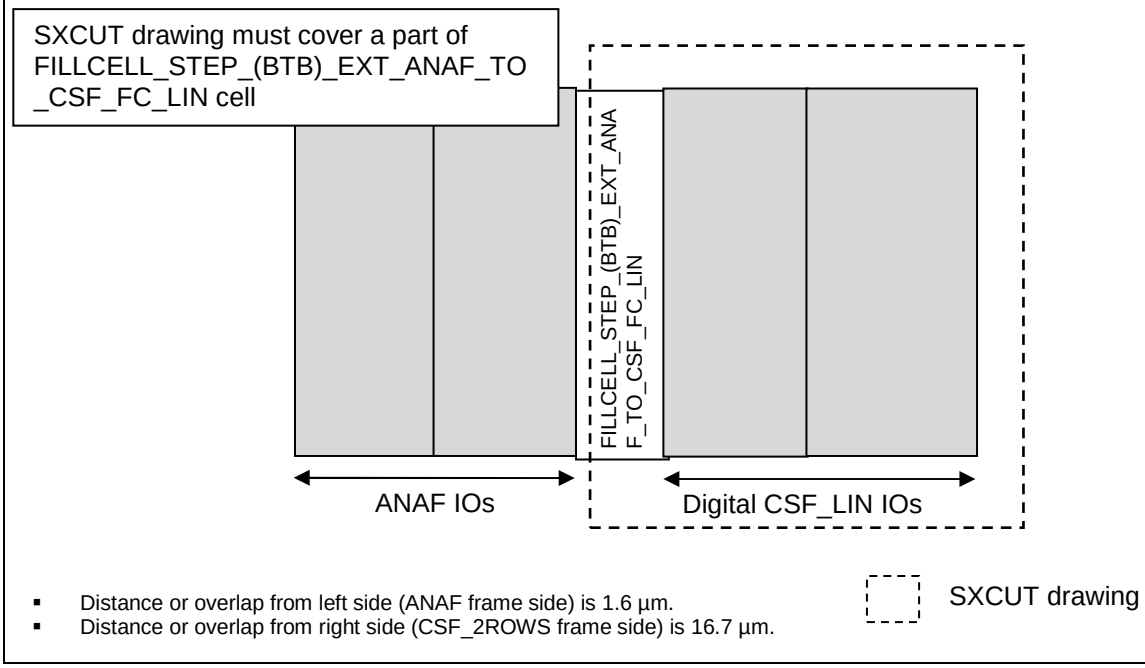


4.1.6 Step cells usage

When FILLCELL_STEP_(BTB)_EXT_ANAF_TO_CSF_FC_LIN step cells are used in R0 orientation they allow transition from analog frame to digital CSF frame. To allow the transition from digital CSF to analog section step filler must be flipped.

When using FILLCELL_STEP_(BTB)_EXT_ANAF_TO_CSF_FC_LIN step cells, please consider that the substrate node on the left side (gnddig) is different than the substrate node on the right side (esdsubana). Therefore, one of the substrate polarization must be isolated using the marker layer, SXCUT drawing.

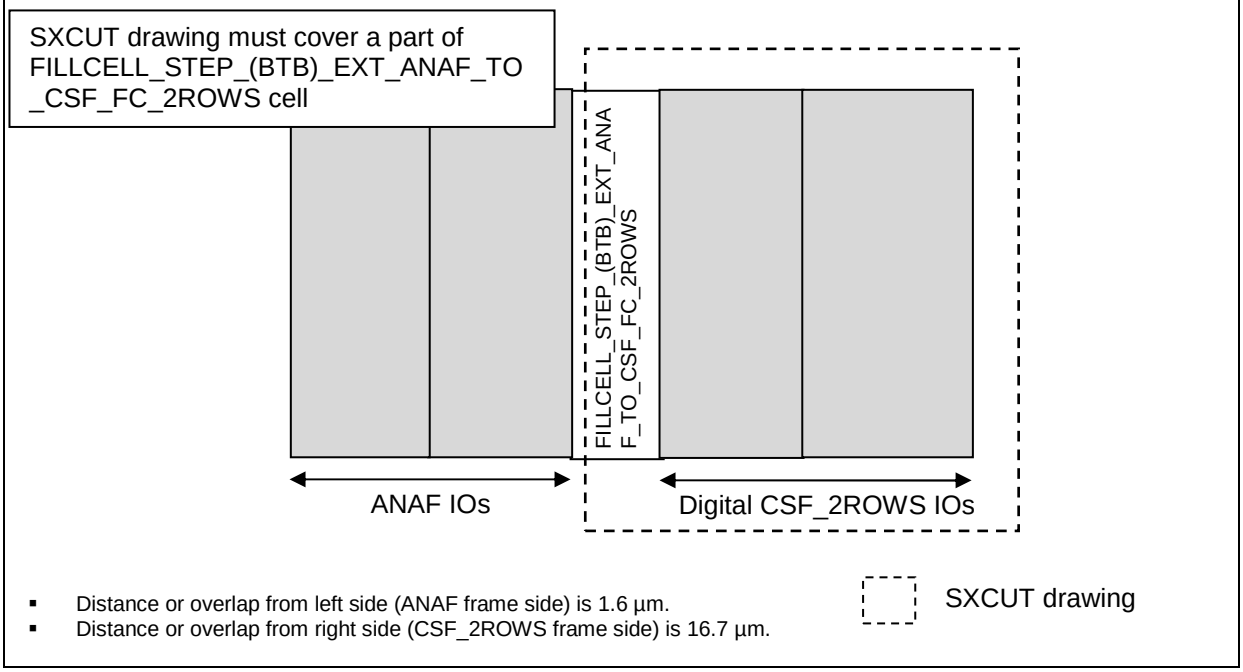
Figure 34 : Using SXCUT Drawing with FILLCELL_STEP_(BTB)_EXT_ANAF_TO_CSF_FC_LIN cell



When FILLCELL_STEP_(BTB)_EXT_ANAF_TO_CSF_FC_2ROWS step cells are used in R0 orientation they allow transition from analog frame to digital CSF_2ROWS frame. To allow the transition from digital CSF_2ROWS to analog section step filler must be flipped.

When using FILLCELL_STEP_(BTB)_EXT_ANAF_TO_CSF_FC_2ROWS step cells, please consider that the substrate node on the left side (esdsubana) is different than the substrate node on the right side (gnddig). Therefore, one of the substrate polarization must be isolated using the marker layer, SXCUT drawing.

Figure 35 : Using SXCUT Drawing with FILLCELL_STEP_(BTB)_EXT_ANAF_TO_CSF_FC_2ROWS cell



4.2 Placement rules

For this chapter a ‘section of analog IO ring’ is considered having a continuous vdde and gnde. A cut of vdde and/or gnde implies a change of ring section.

4.2.1 ESD Protection Nomenclature

For a better understanding of the ESD placement rules, the following definition of ESD protection devices is proposed:

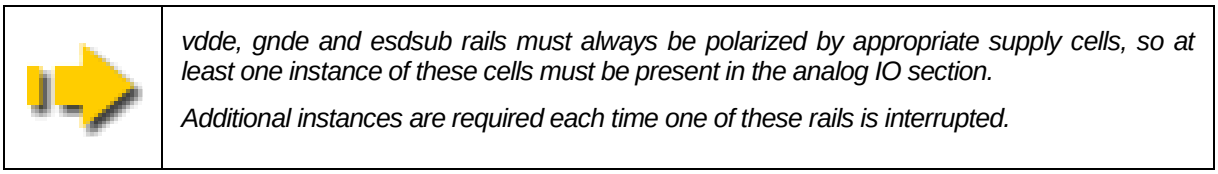
- CVDDE1V0 refers to the vdde1v0/gnde ESD clamp. It is embedded in VDDE/GNDE_ESD_1V0_EXT_ANA_** and FILLCELL_ESD_1V0_EXT_ANA_** cells.
- CVDDE1V8 refers to the vdde1v8/gnde ESD clamp. It is embedded in VDDE/GNDE_ESD_1V8_EXT_ANA_** and FILLCELL_ESD_1V8_EXT_ANA_** cells.
- CVDDE3V3 refers to the vdde3v3/gnde ESD clamp. It is embedded in VDDE/GNDE_ESD_3V3_EXT_ANA_** and FILLCELL_ESD_3V3_EXT_ANA_** cells.

4.2.2 Supply and power pad placement rules

ESD strategy for the C28SOI_IO_EXT_ANAF_ANA_EG library is based on a central clamp between vdde and gnde. In addition, there are diodes between the pad and vdde as well as between the pad and gnde, to forward the current through the ESD global protection.

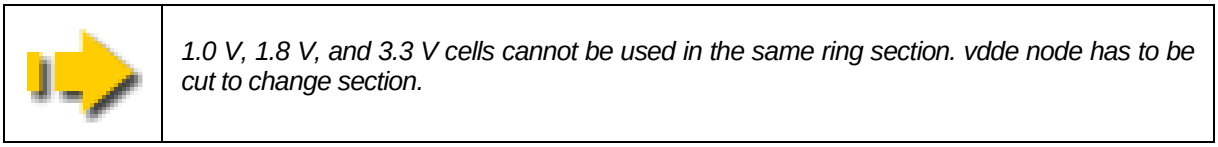
In order to protect the different sections together and also to have a common ESD reference, ‘esdsub’ rail must be kept continuous.

Rules listed below have to be respected to power and ground supplies within an analog IO section.

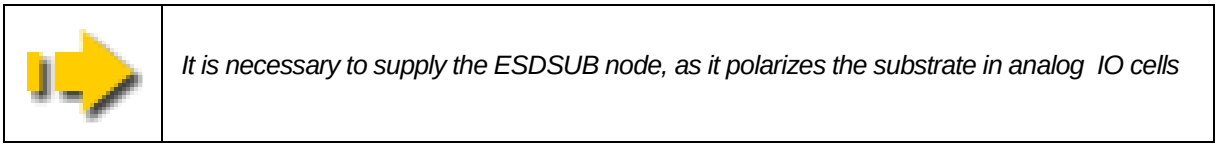


vdde, gnde and esdsub rails must always be polarized by appropriate supply cells, so at least one instance of these cells must be present in the analog IO section.

Additional instances are required each time one of these rails is interrupted.



1.0 V, 1.8 V, and 3.3 V cells cannot be used in the same ring section. vdde node has to be cut to change section.



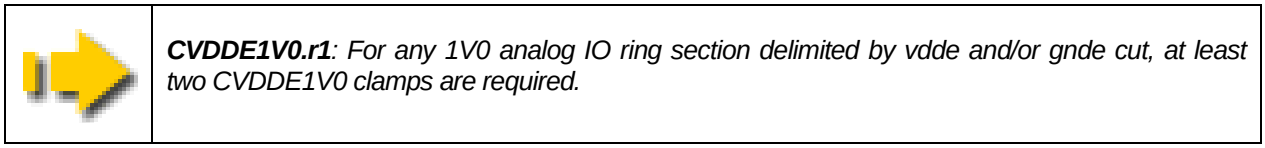
It is necessary to supply the ESDSUB node, as it polarizes the substrate in analog IO cells

4.2.2.1. IO Supply Number

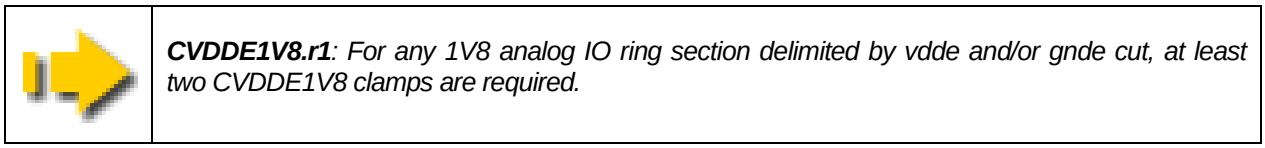
The number of IO supplies required in an IO ring is defined by two main parameters:

- Current capability of the cell
- Minimum number of VDDE/GNDE ESD clamps

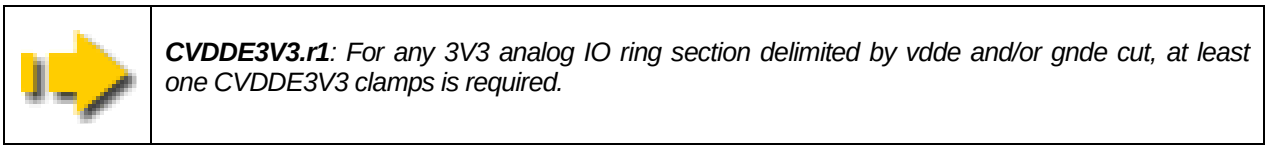
Below rules to be respected for different analog IO sections



***CVDDE1V0.r1**: For any 1V0 analog IO ring section delimited by vdde and/or gnde cut, at least two CVDDE1V0 clamps are required.*



***CVDDE1V8.r1**: For any 1V8 analog IO ring section delimited by vdde and/or gnde cut, at least two CVDDE1V8 clamps are required.*



***CVDDE3V3.r1**: For any 3V3 analog IO ring section delimited by vdde and/or gnde cut, at least one CVDDE3V3 clamps is required.*

4.2.2.2. IO Supply Distance

	***CVDDE1V0.r2**: The maximum distance between two CVDDE1V0 ESD clamps is 0.5 mm.*

	***CVDDE1V8.r2**: The maximum distance between two CVDDE1V8 ESD clamps is 1 mm.*

	***CVDDE3V3.r2**: The maximum distance between two CVDDE3V3 ESD clamps is 1 mm.*

	***ESDSUB.r1:** Maximum spacing between two ESDSUB cells must not exceed 1 mm to ensure correct substrate polarization.*

4.2.2.3. Protected loads

	Supply cells provided by C28SOI_IO_EXT_ANAF_ANA_EG library protect GO2 devices mounted on inverter, capacitor or single MOS

	Only VDDE/GNDE_ESD_1V0_EXT_ANA_FC_LIN / CL_LIN supply cells can protect NMOS, PMOS GO1 load mounted on inverter, capacitor or single MOS, except NMOS GO1 with gate connected to VDDE.

4.2.3 FILLERCUT Placement Rules:

Cutting vdde and/or gnde rails

	***CVDDE.r3:** In case of cut vdde and/or gnde nodes (FILLCUTCELL_*), it is necessary to have ESD protection according to the rail cut before and after this filler cut. The distance between the supply and the fillercut should not exceed 250 µm in the case of 1V8 or 3V3 IO ring section and 125 µm in the case of 1V0 IO ring section.*

Cutting esdsub rail (FILLCUTCELL_ALL_** and FILLCELL_END_** cells)

	*The maximum number of cut of ESD reference node on a whole chip (esdsub in analog section, gnd in digital ones) is three.*

	***ESDSUB.r2:*** *Each section cut by a FILLERCUT_ALL (FILLCUTCELL_ALL_EXT_ANA_FC_LIN) must contain at least one ESDSUB cell.*

	*If cut of esdsub node is needed for more than three times in a chip, please refer to the C28SOI_IO_EXT_ALLF_ESDHUB_EG library user's manual*

Summary

Table 64 : Cutting Rails

Cells	Cut vdde rails	Cut gnde rails	Cut esdsub rails	Rules
FILLCUTCELL_ALL_EXT_ANA_**	X	X	X	CVDDE1V0.r1, CVDDE1V8.r1, CVDDE3V3.r1, CVDDE1V0.r2, CVDDE1V8.r2, CVDDE3V3.r2, CVDDE.r3, ESDSUB.r1 ESDSUB.r2
FILLCUTCELL_GNDE_EXT_ANA_*	-	X	-	CVDDE1V0.r1, CVDDE1V8.r1, CVDDE3V3.r1, CVDDE1V0.r2, CVDDE1V8.r2, CVDDE3V3.r2, CVDDE.r3,
FILLCUTCELL_VDDE_EXT_ANA_*	X	-	-	CVDDE1V0.r1, CVDDE1V8.r1, CVDDE3V3.r1, CVDDE1V0.r2, CVDDE1V8.r2, CVDDE3V3.r2, CVDDE.r3,
FILLCELL_END_LEFT/RIGHT_*	X	X	X	CVDDE1V0.r1, CVDDE1V8.r1, CVDDE3V3.r1, CVDDE1V0.r2, CVDDE1V8.r2, CVDDE3V3.r2, CVDDE.r3, ESDSUB.r1 ESDSUB.r2

FILLCELL_STEP_EXT_ANAF_TO_CSF_*	X	X	-	CVDDE1V0.r1, CVDDE1V8.r1, CVDDE3V3.r1, CVDDE1V0.r2, CVDDE1V8.r2, CVDDE3V3.r2, CVDDE.r3
FILLCELL_STEP_BTB_EXT_ANAF_TO_CSF_*	X	X	X	CVDDE1V0.r1, CVDDE1V8.r1, CVDDE3V3.r1, CVDDE1V0.r2, CVDDE1V8.r2, CVDDE3V3.r2, CVDDE.r3, ESDSUB.r1 ESDSUB.r2

'X' indicates the cut rails of the cells.
'-' indicates the non-cut rails of the cells.

4.2.4 IO Placement Rules

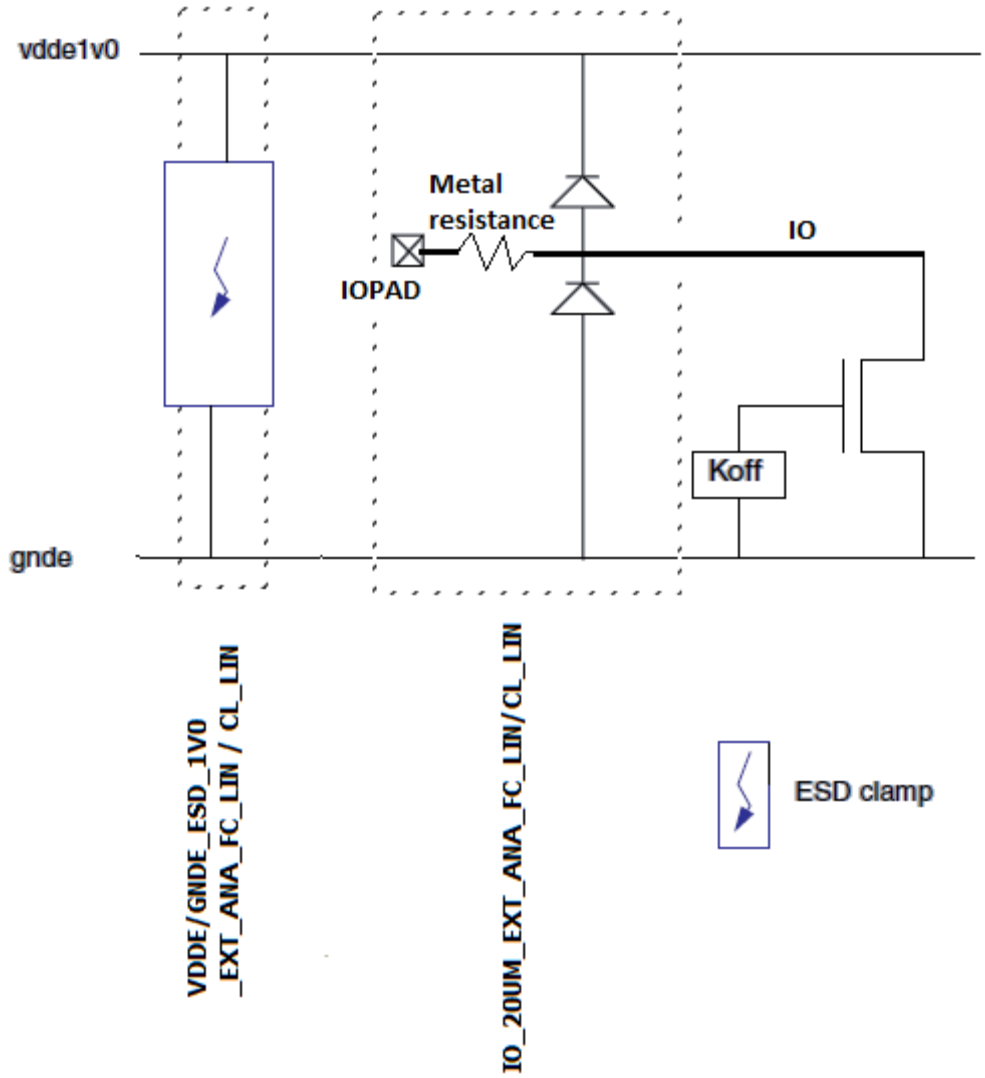
	*To connect an input buffer or a transistor gate to IO pad It is mandatory to use RES pin (series resistor pin on IO signal) and a CDM secondary protection*

	*Details on loads which can protected by IO_UHF_EXT_ANA_* and IO_20UM_*_EXT_ANA analog IO cells are provided in the next table 'Supplies and IOs usage summary'*

	*Please be aware that, for ANAF analog frame, there are no differences between FC cells and CL cells. Only their names are different.*

	*As indicated in the figure below, within an 1V0 analog section: when the drain of an NMOS GO1 is directly connected to pad, a specific keep-off structure is mandatory on gate (NMOS GO1 with gate 'on' cannot be efficiently protected)*

Figure 36 : GO1 Devices between analog IO signal and gnde



	A star routing between Bump, IO Signal ANA cells and macro is forbidden (see figure below)

Figure 37 : Forbidden configuration

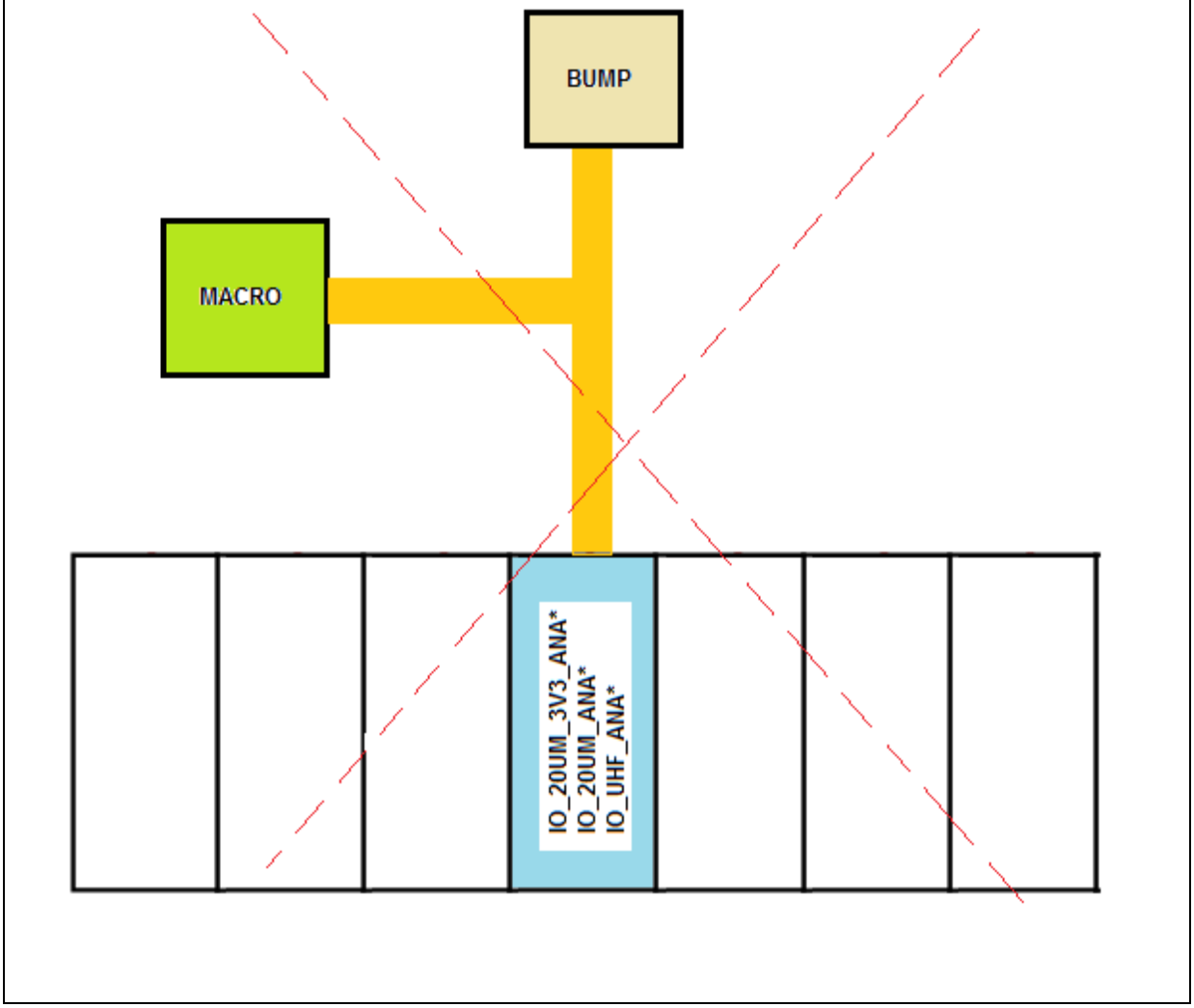


Table below summarizes allowed loads, ESD targets, maximum distances to respect between supplies / IO to supplies / cut filler to supplies for different configurations provided by the library.

Table 65 : Supplies and IOs usage summary

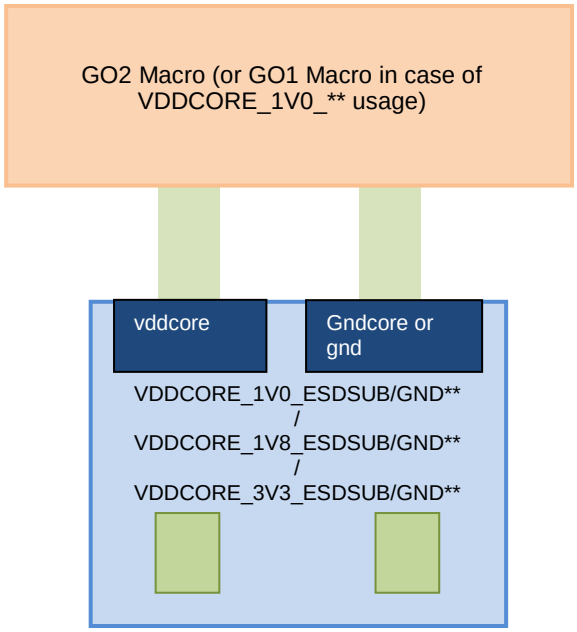
Configuration		Loads which can be protected	ESD target		Distance rules
ANA IO ring section	IO Cells		HBM	CDM	
1V0	IO_UHF_EXT_ANA_FC_LIN / CL_LIN	**FORBIDDEN**	-	-	-
	IO_20UM_EXT_ANA_FC_LIN / CL_LIN	GO1, RPO only(*)	2 kV	250 V	Supply to supply: 500 um IO to supply: 250 um Cut (ALL/GNDE/VDDE) to supply: 125 um
1V8	IO_UHF_EXT_ANA_FC_LIN / CL_LIN	GO2, RPO only(*)	2 kV	250 V	Supply to supply: 1 mm IO to supply: 500 um Cut (ALL/GNDE/VDDE) to supply: 250 um
	IO_20UM_EXT_ANA_FC_LIN / CL_LIN	GO2, No RPO	2kV	250 V	
	IO_20UM_EXT_ANA_FC_LIN / CL_LIN	GO2, RPO only(*)	2kV	500 V	
3V3	IO_UHF_EXT_ANA_FC_LIN / CL_LIN	Cascoded GO2, RPO only(*)	2 kV	250 V	Supply to supply: 1 mm IO to supply: 500 um Cut (ALL/GNDE/VDDE) to supply: 250 um
	IO_20UM_3V3_EXT_ANA_FC_LIN / CL_LIN	Cascoded GO2 (No RPO)	2kV	250 V	
	IO_20UM_3V3_EXT_ANA_FC_LIN / CL_LIN	Cascoded GO2, RPO only(*)	2kV	500 V	

(*): Silicide block (SBLK) overlap on drain and source must be minimum 0.3 um for both PMOS and NMOS on output buffer

4.2.5 Dedicated supply Placement Rules

As dedicated supply cells include their own ESD protection, analog macro can be powered directly by VDDCORE_xx supply cells.

Figure 38 : Macro connection to VDDCORE__GND** dedicated supplies**



Next table describes the cells usage correspondence:

Macro supply voltage level	Devices to protect	Macro ground	Cell to use
1V0	GO1/GO2 devices	Dedicated ground	VDDCORE_1V0_GNDCORE_**
1V0	GO1/GO2 devices	Shared IO ground	VDDCORE_1V0_GNDE_**
1V0	GO1/GO2 devices	Shared core ground	VDDCORE_1V0_ESDSUB_**
1V8	GO2 devices	Dedicated ground	VDDCORE_1V8_GNDCORE_**
1V8	GO2 devices	Shared IO ground	VDDCORE_1V8_GNDE_**
1V8	GO2 devices	Shared core ground	VDDCORE_1V8_ESDSUB_**
3V3	Cascaded GO2 devices	Dedicated ground	VDDCORE_3V3_GNDCORE_**
3V3	Cascaded GO2 devices	Shared IO ground	VDDCORE_3V3_GNDE_**
3V3	Cascaded GO2 devices	Shared core ground	VDDCORE_3V3_ESDSUB_**

	VDDCORE_1V0_** dedicated supply cannot be used to protect GO1 devices connected to IO signal as highlighted in the figure below

Figure 39 : Prohibited configuration

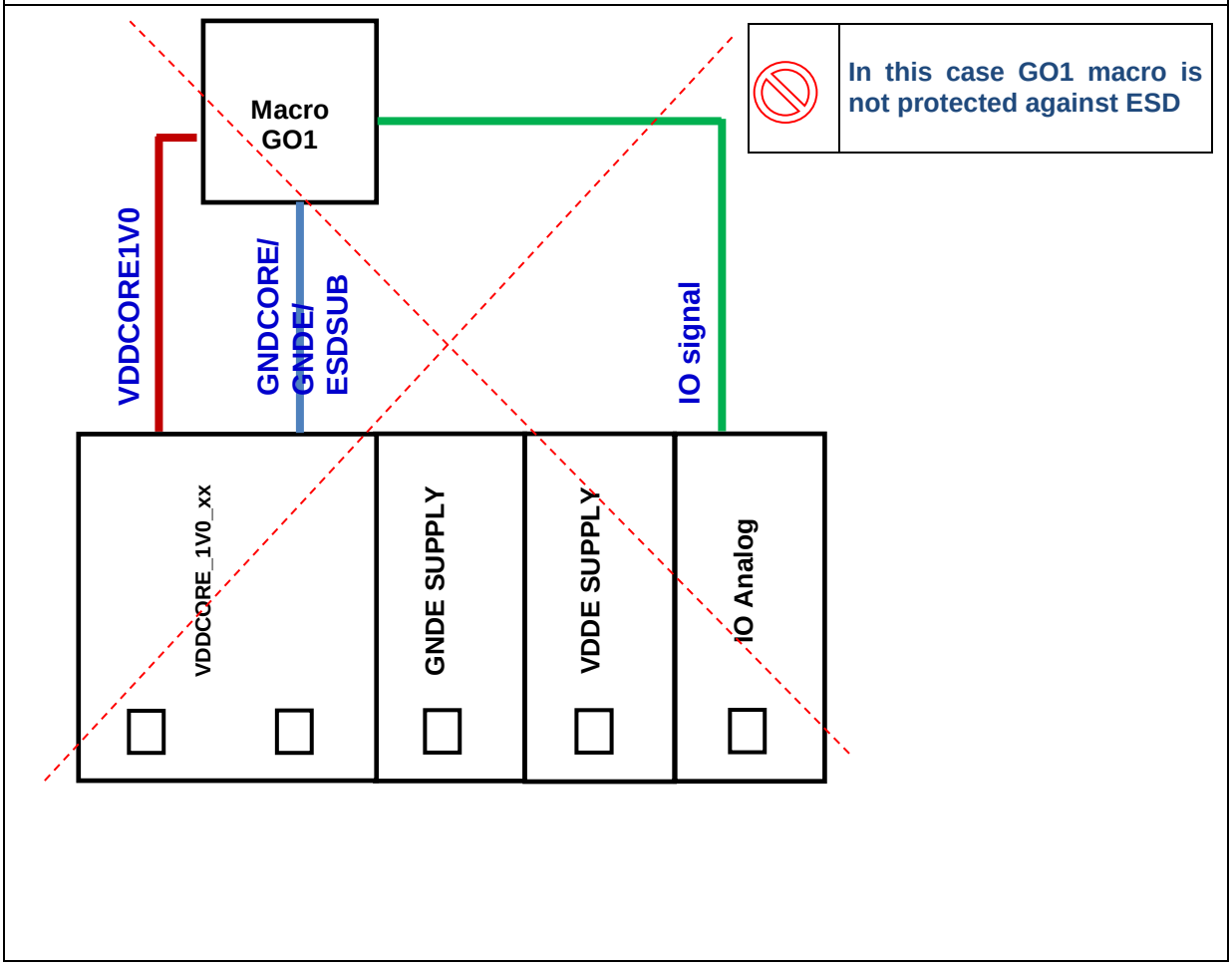
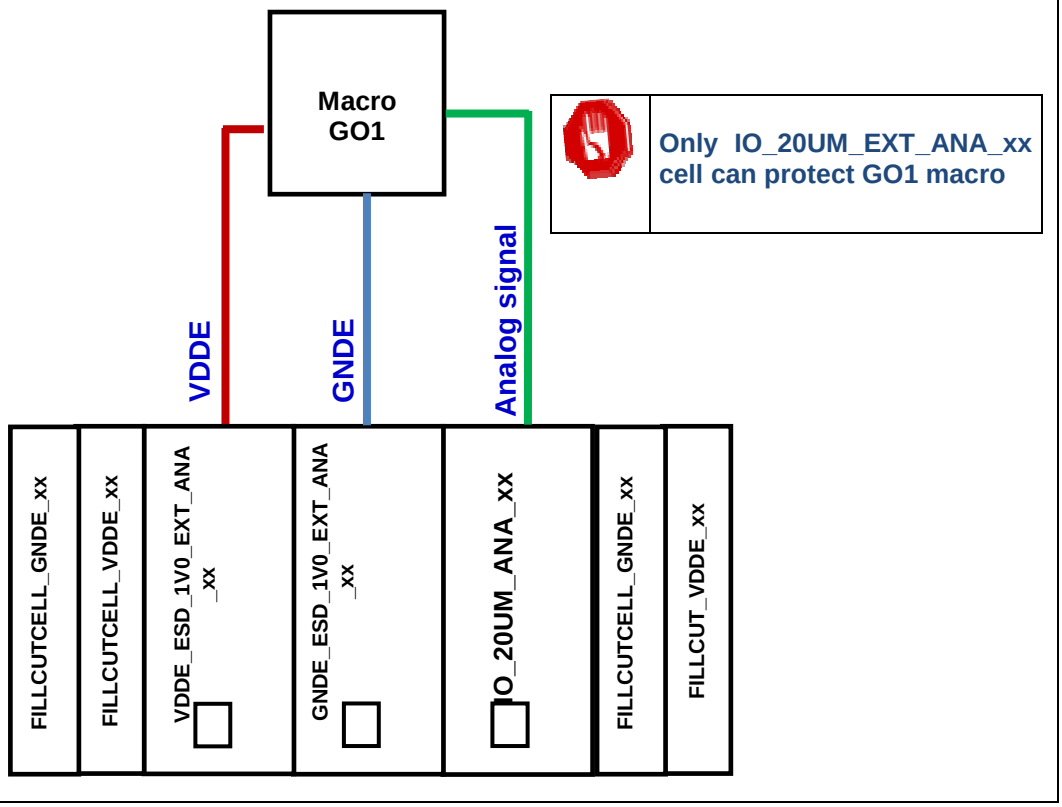


Figure 40 : Right configuration to protect a GO1 macro



A resistance constraint has to be respected when dedicated supplies are used. Figures below give more details about this constraint for different deployment cases.

Figure 41 : Dedicated supply cells used between BUMP and Macro

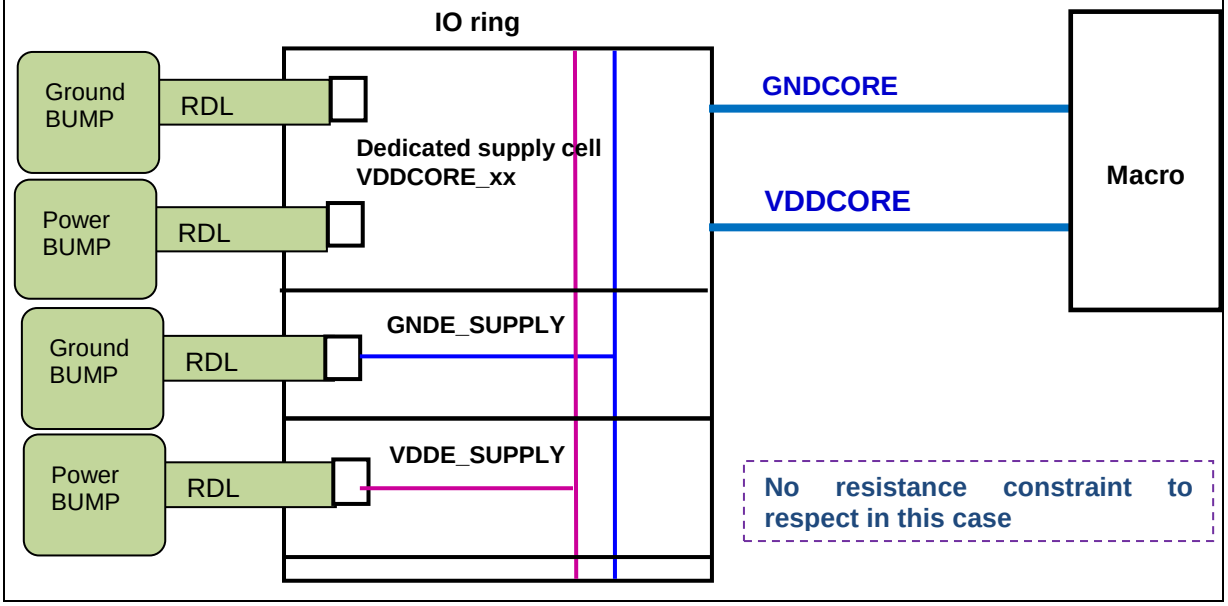


Figure 42 : Macro placed between BUMP and dedicated supply cells

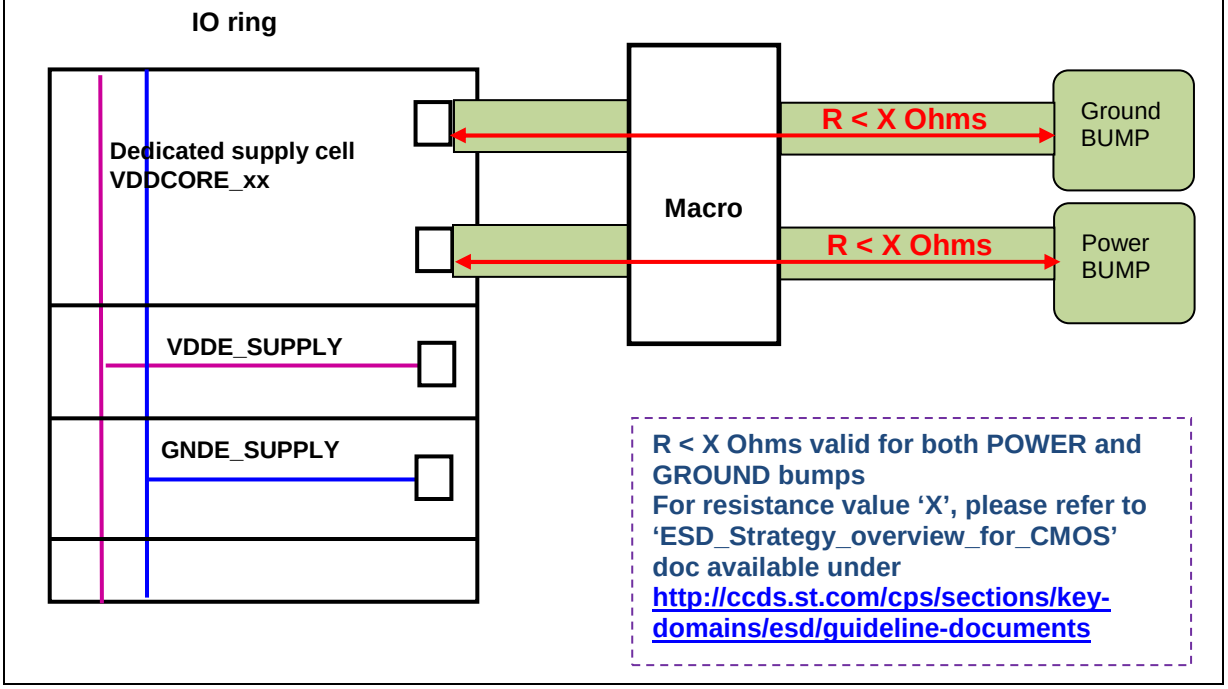
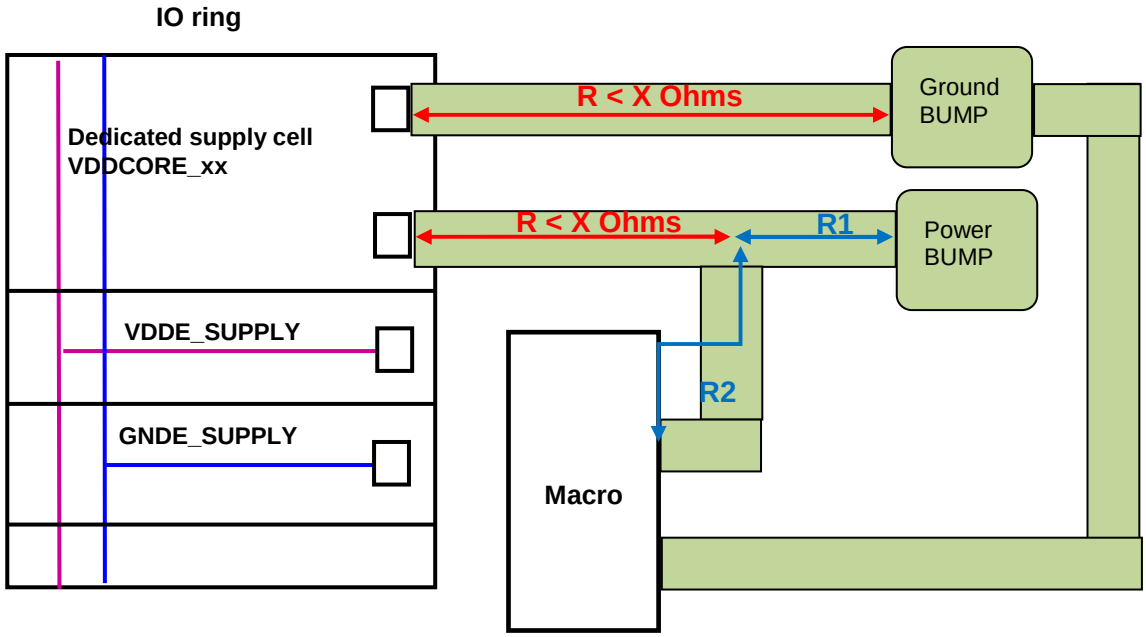


Figure 43 : Generic dedicated supply placement case



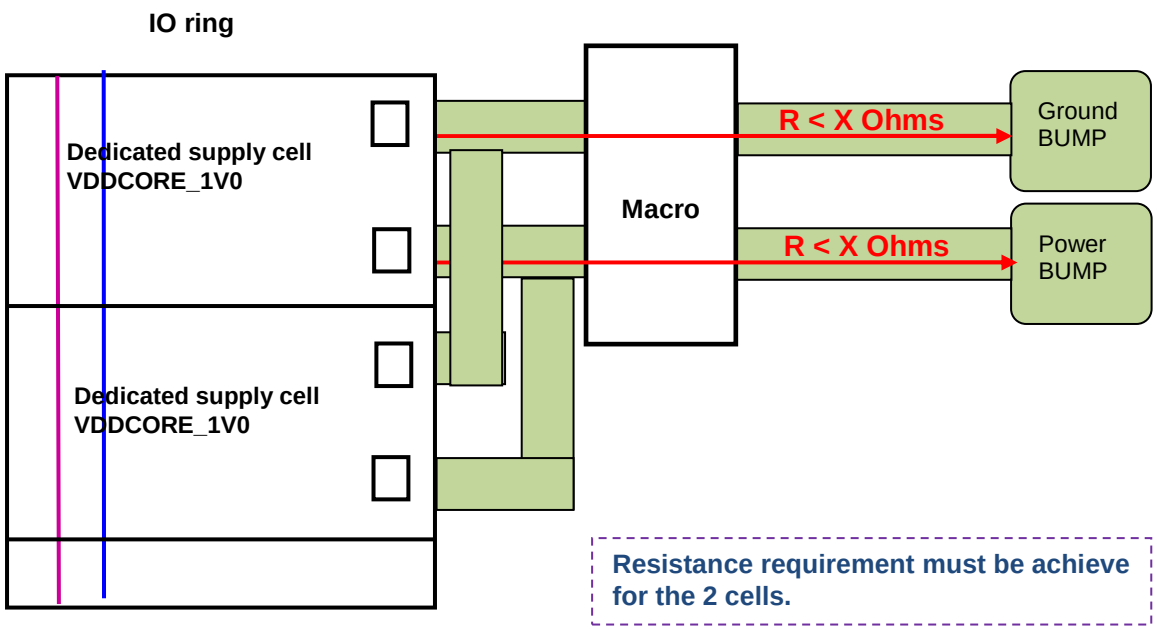
- **For resistance value 'X', please refer to 'ESD_Strategy_overview_for_CMOS' doc available under http://ccds.st.com/cps/sections/key-domains/esd/guideline-documents**
- **When we have a star routing, there are no resistance constraints for R1 and R2.**

Note: Star routing can be used also to connect ground BUMP.

One 1V0 dedicated supply support 250 V CDM.

For 500V CDM, 1V0 dedicated supply must be placed by pair

Figure 44 : Example of two dedicated 1V0 supplies connected on parallel



For more information about dedicated supply cells usage and for specific configuration not listed above, please ask support through helpdesk

When dedicated supply cells are used, It is necessary to supply all nodes having a pad connection.

5.Contact Information

ers, login to **HELPDESK**. (http://col2.cro.st.com/helpdesk) for submitting queries or support requests.

Non-ST users, contact Customer Support personnel.

Appendix A: Naming Convention

The names of C28SOI_IO_EXT_ANAF_ANA_EG library and comprising analog cells consist of multiple segments. Each segment in a naming convention represents a particular feature of the library or cell. However, a name contains only the segments that represent any function.

Table 66 : Naming Convention for C28SOI_IO_EXT_ANAF_ANA_EG Cells

Segment Name	Description
Cell type	Refers to the functionality of the cell. It can have either of the following values: - VDDE_ESD/GNDE_ESD: Supply/ground with ESD protection devices. - VDDE_NOESD/GNDE_NOESD: Supply/ground without ESD protection devices. - FILLCELL_ESD: Filler cells with ESD protection. - ESDSUB_: ESDSUB ground. - IO_20UM: Analog IO. - IO_UHF: Analog RF IO. - VDDCORE_ and GNDCORE_: Dedicated power/ground. - CORNERCELL: Corner cell - FILLCELL_1GRID_, FILLCELL_1UM, FILLCELL_5UM, FILLCELL_10UM: Filler cells - FILLCUTCELL_: Filler cut cell (followed by list of cut node) - FILLCELL_STEP_(BTB)_EXT_ANAF_TO_CSF_FC_*, Step filler to digital frame.
1st suffix	Refers to the voltage level at pad side. The value of this segment is 1V0, 1V8, or 3V3 and indicates the voltage at pad side.
2nd suffix	Refers to the cell offer. It can have either of the following values: - <none> - EXT: extended CDM specification offer
3rd suffix	Refers to the type of frame used. The value of this segment is ANA, which refers an analog frame.
4th suffix	Refers to the layout view of the cell. It can have any of the following values: - FC: represents flip-chip configuration - CL: represents cluster configuration
5th suffix	Indicates single (linear) row or double row (2ROWS) configurations for the cell.

Table 67 : Example: Segments in the Name of GNDE_ESD_1V8_EXT_ANA_FC_LIN Cell

Segment Name	Segment Value	Description
Cell type	GNDE_ESD	Refers to the GNDE_ESD functionality of the cell
1st suffix	1V8	1.8 V at the pad side
2nd suffix	EXT	extended CDM specification offer
3rd suffix	ANA	Analog cell
4th suffix	FC	Flip-chip configuration
5th suffix	LIN	Single row configuration

Appendix B: Document Revision Historyf

Table 68 : Document Revision History

Date	Document Version	Comments
-September-2016	1.3	• Usage guidelines and rules modified for substrate ground supply and IO_20UM_XX analog IO cells • Usage guidelines improved for 1V0 dedicated supplies
-January-2016	1.2	• Adding note about FC = CL • Reference library added • Table 2 “Acronyms and Abbreviations” added • Alignment to ESD/LU guidelines
10-July-2015	1.1	• Table 1 : vddcore* nodes added • “Pin description” tables improved • “Cell Information” tables improved
23-September-2014	1.0	• First release

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