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C28SOI_SC_8_COREPBP4_LL Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 4 nm

Overview

- C28SOI_SC_8_COREPBP4_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

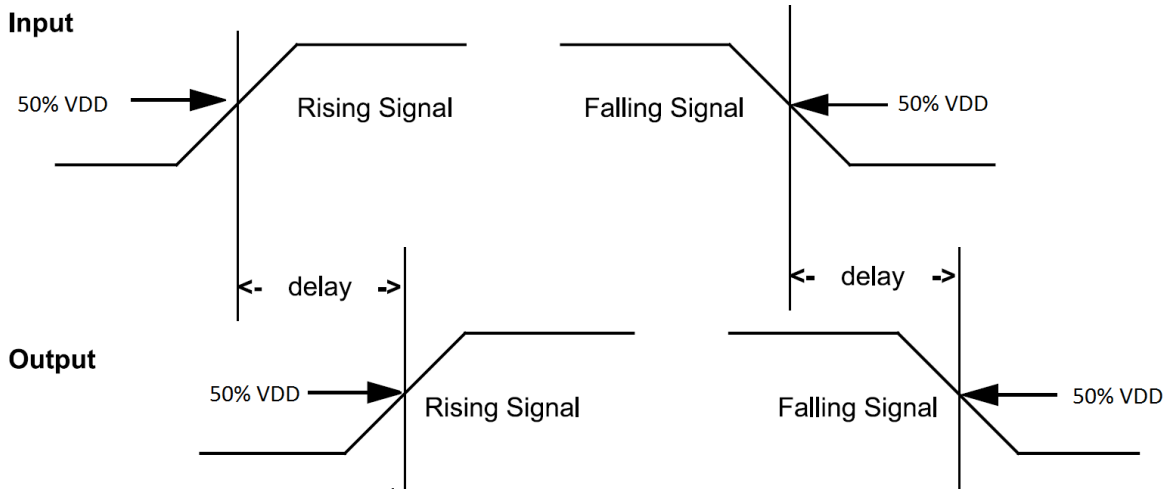


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

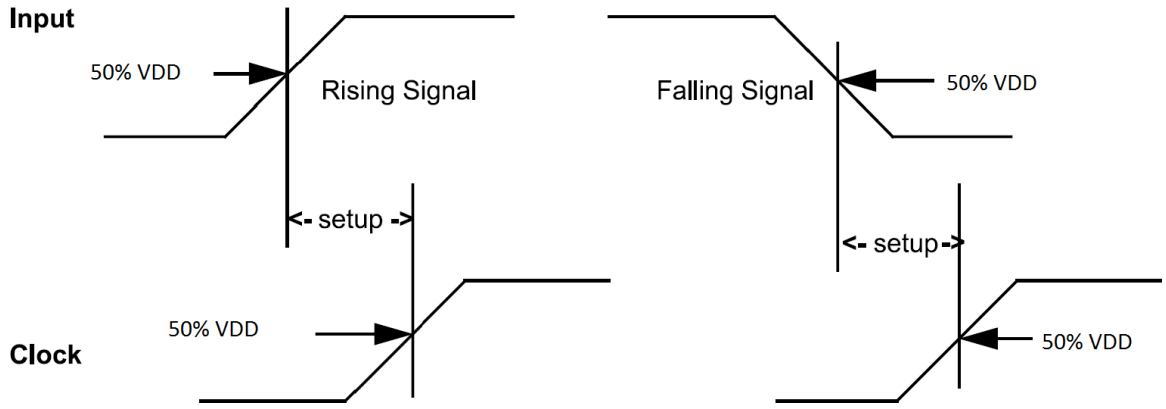


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

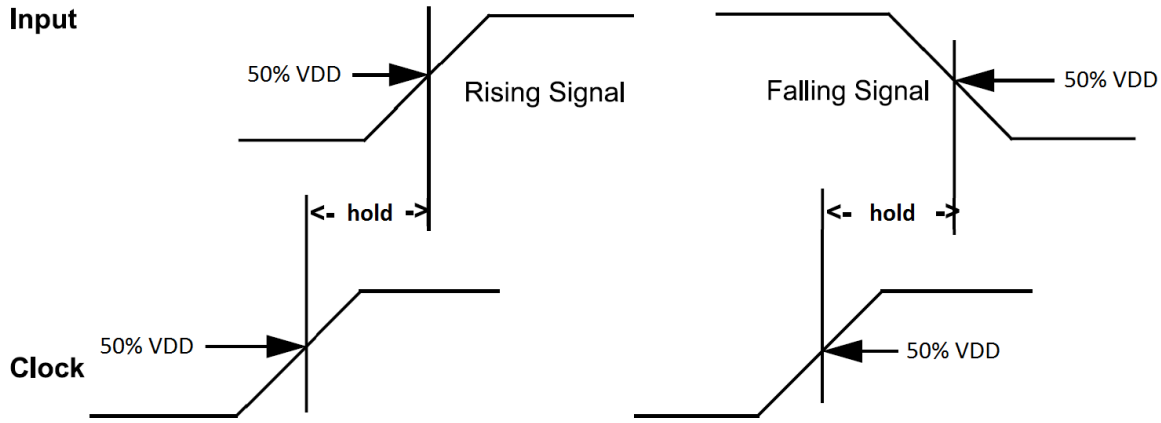


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

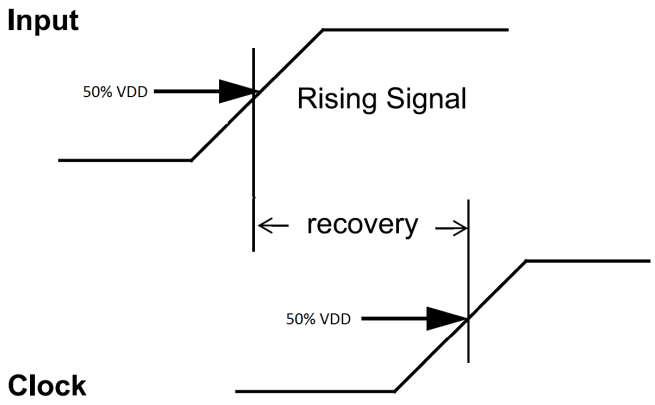


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

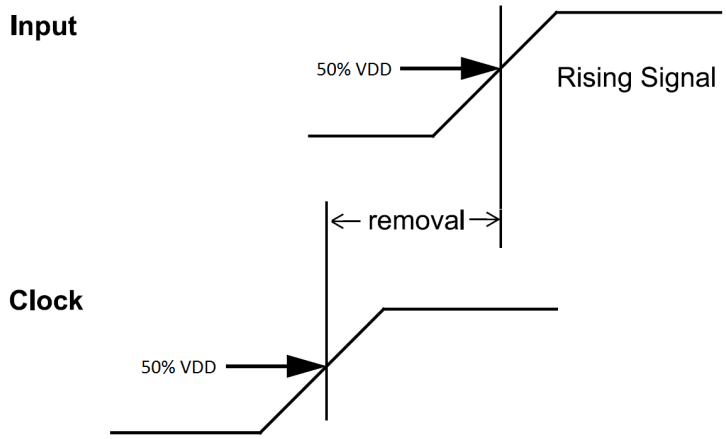


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

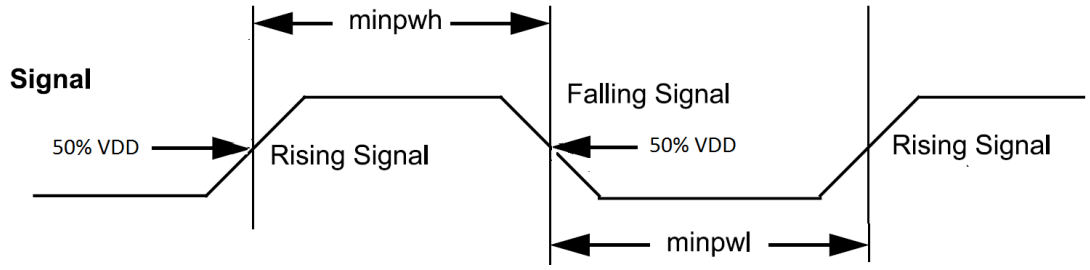


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

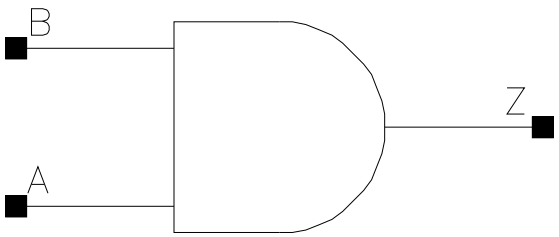
The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description	Logical Symbol
2 input AND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.544	0.4352
X10_P4	0.800	0.680	0.5440
X11_P4	1.600	0.544	0.8704
X19_P4	0.800	1.224	0.9792
X24_P4	0.800	1.360	1.0880
X29_P4	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X11_P4	X19_P4
A	0.0004	0.0006	0.0008	0.0013
B	0.0004	0.0006	0.0008	0.0011
	X24_P4	X29_P4		
A	0.0012	0.0012		
B	0.0011	0.0011		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0331	0.0262	4.0770	1.9407
A to Z ↑	0.0267	0.0240	6.1789	2.9519
B to Z ↓	0.0318	0.0247	4.0743	1.9390
B to Z ↑	0.0283	0.0253	6.1780	2.9489
	X11_P4	**X19_P4**	**X11_P4**	**X19_P4**

A to Z ↓	0.0287	0.0257	1.4970	0.9971
A to Z ↑	0.0224	0.0236	2.8573	1.4872
B to Z ↓	0.0269	0.0247	1.4950	0.9982
B to Z ↑	0.0237	0.0251	2.8580	1.4842
	X24_P4	**X29_P4**	**X24_P4**	**X29_P4**
A to Z ↓	0.0277	0.0295	0.8096	0.6756
A to Z ↑	0.0257	0.0275	1.1926	0.9908
B to Z ↓	0.0268	0.0287	0.8095	0.6755
B to Z ↑	0.0274	0.0294	1.1922	0.9909

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.416e-05	1.000e-20
X10_P4	3.213e-05	1.000e-20
X11_P4	3.695e-05	1.000e-20
X19_P4	6.118e-05	1.000e-20
X24_P4	7.085e-05	1.000e-20
X29_P4	8.053e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X11_P4	X19_P4
A (output stable)	5.204e-06	1.109e-05	1.495e-05	2.094e-05
B (output stable)	1.136e-05	2.166e-05	3.084e-05	4.357e-05
A to Z	1.197e-03	1.990e-03	2.426e-03	3.927e-03
B to Z	1.151e-03	1.914e-03	2.296e-03	3.754e-03
	X24_P4	X29_P4		
A (output stable)	2.099e-05	2.109e-05		
B (output stable)	4.397e-05	4.407e-05		
A to Z	4.781e-03	5.578e-03		
B to Z	4.615e-03	5.421e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

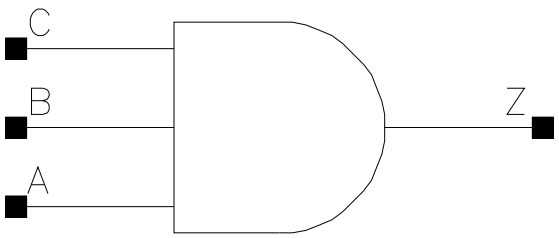
Pin Cycle (vdds)	X5_P4	X10_P4	X11_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P4	X29_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.680	0.5440
X10_P4	0.800	0.816	0.6528
X14_P4	0.800	1.360	1.0880
X19_P4	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0004	0.0007	0.0011	0.0013
B	0.0004	0.0006	0.0009	0.0012
C	0.0004	0.0006	0.0008	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0372	0.0294	4.1289	1.9546
A to Z ↑	0.0366	0.0322	6.2564	2.9820
B to Z ↓	0.0363	0.0280	4.1248	1.9508
B to Z ↑	0.0378	0.0330	6.2616	2.9827
C to Z ↓	0.0353	0.0269	4.1248	1.9504
C to Z ↑	0.0392	0.0337	6.2607	2.9834
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0296	0.0280	1.3449	1.0015

A to Z ↑	0.0311	0.0301	2.0246	1.4989
B to Z ↓	0.0283	0.0266	1.3422	0.9994
B to Z ↑	0.0319	0.0310	2.0220	1.5003
C to Z ↓	0.0271	0.0254	1.3425	0.9988
C to Z ↑	0.0330	0.0317	2.0240	1.5005

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.320e-05	1.000e-20
X10_P4	3.014e-05	1.000e-20
X14_P4	4.209e-05	1.000e-20
X19_P4	5.819e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	6.148e-06	1.317e-05	1.720e-05	2.375e-05
B (output stable)	8.126e-06	1.527e-05	2.150e-05	3.015e-05
C (output stable)	1.934e-05	3.649e-05	5.277e-05	7.751e-05
A to Z	1.406e-03	2.333e-03	3.393e-03	4.428e-03
B to Z	1.357e-03	2.240e-03	3.250e-03	4.228e-03
C to Z	1.319e-03	2.157e-03	3.132e-03	4.045e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

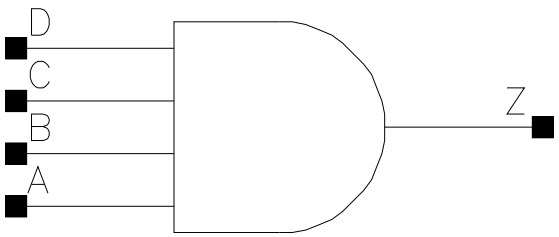
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.088	0.8704
X3_P4	0.800	1.088	0.8704
X10_P4	0.800	2.176	1.7408
X13_P4	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P4	X3_P4	X10_P4	X13_P4
A	0.0004	0.0005	0.0010	0.0011
B	0.0004	0.0004	0.0009	0.0011
C	0.0004	0.0004	0.0009	0.0011
D	0.0005	0.0005	0.0009	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	X3_P4	X2_P4	X3_P4
A to Z ↓	0.0292	0.0312	7.8648	5.0406
A to Z ↑	0.0310	0.0307	22.9102	11.8758
B to Z ↓	0.0276	0.0301	7.8688	5.0444
B to Z ↑	0.0324	0.0323	22.9185	11.8782
C to Z ↓	0.0300	0.0321	7.8553	5.0292
C to Z ↑	0.0309	0.0304	22.9442	11.8921

D to Z ↓	0.0288	0.0318	7.8480	5.0259
D to Z ↑	0.0329	0.0335	22.9416	11.8949
	X10_P4	**X13_P4**	**X10_P4**	**X13_P4**
A to Z ↓	0.0289	0.0289	1.7280	1.2860
A to Z ↑	0.0288	0.0311	3.8976	2.9903
B to Z ↓	0.0278	0.0266	1.7266	1.2844
B to Z ↑	0.0303	0.0315	3.8983	2.9907
C to Z ↓	0.0290	0.0277	1.7137	1.2887
C to Z ↑	0.0274	0.0268	3.8975	2.9888
D to Z ↓	0.0265	0.0254	1.7104	1.2861
D to Z ↑	0.0276	0.0271	3.8969	2.9894

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P4	1.157e-05	1.000e-20
X3_P4	1.549e-05	1.000e-20
X10_P4	4.758e-05	1.000e-20
X13_P4	6.583e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P4	X3_P4	X10_P4	X13_P4
A (output stable)	2.511e-04	2.982e-04	7.736e-04	1.069e-03
B (output stable)	2.352e-04	2.804e-04	7.277e-04	9.858e-04
C (output stable)	2.589e-04	2.856e-04	7.435e-04	9.433e-04
D (output stable)	2.428e-04	2.765e-04	6.759e-04	8.572e-04
A to Z	9.421e-04	1.253e-03	3.509e-03	4.800e-03
B to Z	8.966e-04	1.203e-03	3.382e-03	4.486e-03
C to Z	9.677e-04	1.248e-03	3.133e-03	3.953e-03
D to Z	9.242e-04	1.222e-03	2.871e-03	3.644e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

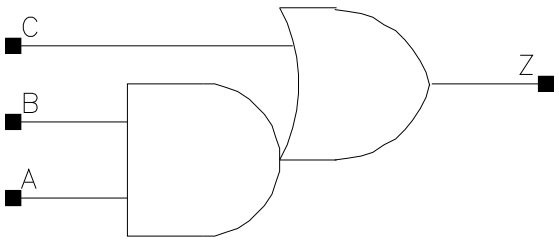
Pin Cycle (vdds)	X2_P4	X3_P4	X10_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	0.952	0.7616
X19_P4	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0004	0.0005	0.0011
B	0.0004	0.0006	0.0009
C	0.0004	0.0006	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0451	0.0385	3.9050	1.9549
A to Z ↑	0.0300	0.0264	5.7735	2.9263
B to Z ↓	0.0429	0.0364	3.8901	1.9499
B to Z ↑	0.0321	0.0284	5.7719	2.9251
C to Z ↓	0.0465	0.0381	3.8843	1.9478
C to Z ↑	0.0276	0.0243	5.7353	2.9099
	X19_P4		**X19_P4**	
A to Z ↓	0.0370		1.0158	
A to Z ↑	0.0291		1.4780	

B to Z ↓	0.0357		1.0152	
B to Z ↑	0.0310		1.4754	
C to Z ↓	0.0370		1.0126	
C to Z ↑	0.0261		1.4641	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.679e-05	1.000e-20
X10_P4	3.384e-05	1.000e-20
X19_P4	6.080e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	2.063e-05	2.990e-05	6.748e-05
B (output stable)	2.239e-05	3.555e-05	7.533e-05
C (output stable)	3.120e-05	4.159e-05	9.966e-05
A to Z	1.399e-03	2.290e-03	4.408e-03
B to Z	1.352e-03	2.205e-03	4.287e-03
C to Z	1.532e-03	2.439e-03	4.708e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

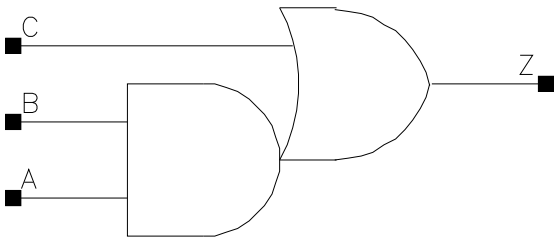
Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	0.952	0.7616
X14_P4	0.800	1.632	1.3056
X19_P4	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0004	0.0006	0.0011	0.0011
B	0.0004	0.0005	0.0011	0.0011
C	0.0004	0.0006	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0476	0.0404	3.8905	1.9718
A to Z ↑	0.0325	0.0292	5.8771	2.9485
B to Z ↓	0.0462	0.0387	3.8769	1.9699
B to Z ↑	0.0354	0.0311	5.8710	2.9453
C to Z ↓	0.0412	0.0358	3.8658	1.9622
C to Z ↑	0.0242	0.0213	5.8027	2.9190
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0365	0.0393	1.3400	1.0096

A to Z ↑	0.0266	0.0284	1.9952	1.4902
B to Z ↓	0.0333	0.0363	1.3335	1.0060
B to Z ↑	0.0275	0.0295	1.9954	1.4913
C to Z ↓	0.0299	0.0328	1.3322	1.0032
C to Z ↑	0.0186	0.0200	1.9754	1.4745

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.684e-05	1.000e-20
X10_P4	3.215e-05	1.000e-20
X14_P4	5.745e-05	1.000e-20
X19_P4	6.598e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	7.962e-06	1.036e-05	3.631e-05	3.641e-05
B (output stable)	1.072e-05	1.356e-05	5.958e-05	5.983e-05
C (output stable)	1.018e-04	1.161e-04	3.403e-04	3.408e-04
A to Z	1.549e-03	2.380e-03	4.142e-03	4.950e-03
B to Z	1.507e-03	2.296e-03	3.821e-03	4.634e-03
C to Z	1.302e-03	2.037e-03	3.279e-03	4.027e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

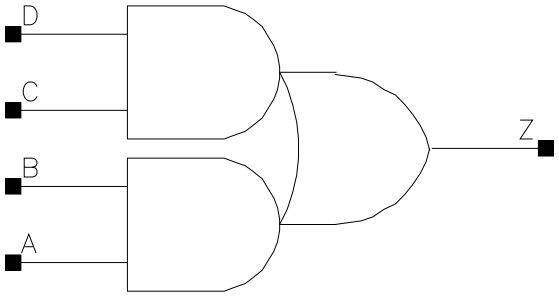
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.088	0.8704
X10_P4	0.800	1.088	0.8704
X14_P4	0.800	1.768	1.4144
X19_P4	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0004	0.0006	0.0011	0.0011
B	0.0004	0.0008	0.0010	0.0010
C	0.0004	0.0006	0.0012	0.0012
D	0.0004	0.0006	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0485	0.0399	3.9066	1.9648
A to Z ↑	0.0342	0.0306	5.9037	2.9302
B to Z ↓	0.0448	0.0366	3.8865	1.9537

B to Z ↑	0.0349	0.0315	5.9021	2.9272
C to Z ↓	0.0430	0.0360	3.8920	1.9565
C to Z ↑	0.0289	0.0256	5.8856	2.9232
D to Z ↓	0.0416	0.0344	3.8845	1.9527
D to Z ↑	0.0313	0.0275	5.8825	2.9190
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0360	0.0388	1.3388	1.0114
A to Z ↑	0.0272	0.0291	2.0027	1.5007
B to Z ↓	0.0339	0.0368	1.3369	1.0107
B to Z ↑	0.0289	0.0309	2.0023	1.4995
C to Z ↓	0.0326	0.0355	1.3358	1.0101
C to Z ↑	0.0234	0.0253	1.9952	1.4947
D to Z ↓	0.0307	0.0337	1.3341	1.0084
D to Z ↑	0.0248	0.0269	1.9939	1.4936

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.909e-05	1.000e-20
X10_P4	3.804e-05	1.000e-20
X14_P4	6.301e-05	1.000e-20
X19_P4	7.212e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.986e-05	2.613e-05	3.151e-05	3.158e-05
B (output stable)	6.887e-05	6.785e-05	4.219e-05	4.231e-05
C (output stable)	2.331e-05	3.003e-05	7.171e-05	7.192e-05
D (output stable)	2.597e-05	3.750e-05	8.626e-05	8.648e-05
A to Z	1.769e-03	2.680e-03	4.308e-03	5.179e-03
B to Z	1.610e-03	2.444e-03	4.090e-03	4.961e-03
C to Z	1.497e-03	2.282e-03	3.605e-03	4.462e-03
D to Z	1.445e-03	2.201e-03	3.431e-03	4.279e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

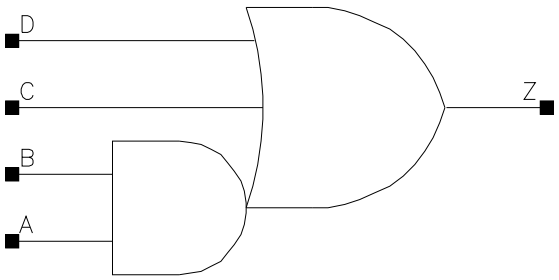
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	1.088	0.8704
X19_P4	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0004	0.0005	0.0010
B	0.0004	0.0006	0.0010
C	0.0004	0.0005	0.0011
D	0.0004	0.0005	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0566	0.0464	4.3574	2.0370
A to Z ↑	0.0312	0.0258	6.1465	2.9374
B to Z ↓	0.0550	0.0437	4.3474	2.0279
B to Z ↑	0.0335	0.0276	6.1459	2.9332
C to Z ↓	0.0605	0.0496	4.3388	2.0286
C to Z ↑	0.0281	0.0343	6.0972	2.9469

D to Z ↓	0.0599	0.0500	4.3381	2.0287
D to Z ↑	0.0279	0.0339	6.0945	2.9430
	X19_P4		**X19_P4**	
A to Z ↓	0.0460		1.0535	
A to Z ↑	0.0284		1.4664	
B to Z ↓	0.0421		1.0479	
B to Z ↑	0.0292		1.4663	
C to Z ↓	0.0480		1.0485	
C to Z ↑	0.0279		1.4582	
D to Z ↓	0.0471		1.0481	
D to Z ↑	0.0275		1.4569	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.381e-05	1.000e-20
X10_P4	3.014e-05	1.000e-20
X19_P4	5.552e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	2.401e-05	5.255e-05	9.100e-05
B (output stable)	2.390e-05	5.248e-05	1.029e-04
C (output stable)	1.401e-05	2.595e-05	5.533e-05
D (output stable)	1.832e-05	3.449e-05	6.420e-05
A to Z	1.490e-03	2.430e-03	4.769e-03
B to Z	1.449e-03	2.333e-03	4.446e-03
C to Z	1.659e-03	2.813e-03	5.320e-03
D to Z	1.587e-03	2.689e-03	5.028e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

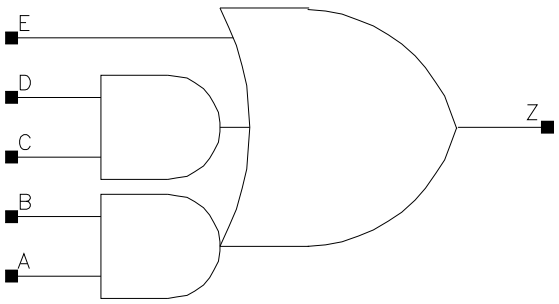
Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.088	0.8704
X10_P4	0.800	1.224	0.9792
X19_P4	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0003	0.0006	0.0011
B	0.0004	0.0006	0.0009
C	0.0004	0.0007	0.0011
D	0.0004	0.0006	0.0010
E	0.0004	0.0005	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0719	0.0548	4.0974	2.0232
A to Z ↑	0.0397	0.0322	5.9673	2.9578

B to Z ↓	0.0715	0.0527	4.0857	2.0189
B to Z ↑	0.0431	0.0343	5.9683	2.9558
C to Z ↓	0.0629	0.0482	4.0865	2.0180
C to Z ↑	0.0350	0.0276	5.9227	2.9363
D to Z ↓	0.0598	0.0443	4.0705	2.0105
D to Z ↑	0.0374	0.0290	5.9167	2.9360
E to Z ↓	0.0640	0.0485	4.0615	2.0101
E to Z ↑	0.0301	0.0248	5.8633	2.9170
	X19_P4		**X19_P4**	
A to Z ↓	0.0528		1.0421	
A to Z ↑	0.0335		1.4869	
B to Z ↓	0.0506		1.0397	
B to Z ↑	0.0357		1.4858	
C to Z ↓	0.0449		1.0386	
C to Z ↑	0.0278		1.4743	
D to Z ↓	0.0427		1.0361	
D to Z ↑	0.0298		1.4740	
E to Z ↓	0.0465		1.0354	
E to Z ↑	0.0311		1.4698	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.695e-05	1.000e-20
X10_P4	3.586e-05	1.000e-20
X19_P4	6.414e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	8.095e-06	1.451e-05	2.946e-05
B (output stable)	1.188e-05	1.618e-05	3.013e-05
C (output stable)	3.219e-05	4.338e-05	9.435e-05
D (output stable)	3.361e-05	5.212e-05	1.008e-04
E (output stable)	5.191e-05	7.576e-05	1.569e-04
A to Z	2.041e-03	3.094e-03	5.926e-03
B to Z	2.015e-03	2.990e-03	5.721e-03
C to Z	1.717e-03	2.545e-03	4.772e-03
D to Z	1.662e-03	2.424e-03	4.614e-03
E to Z	1.779e-03	2.681e-03	5.140e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

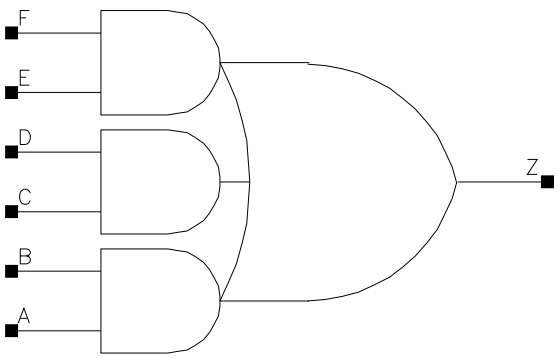
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.360	1.0880
X5_P4	0.800	1.360	1.0880
X10_P4	0.800	1.632	1.3056
X19_P4	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P4	X5_P4	X10_P4	X19_P4
A	0.0004	0.0004	0.0007	0.0011

B	0.0005	0.0004	0.0007	0.0009
C	0.0006	0.0006	0.0005	0.0010
D	0.0004	0.0004	0.0005	0.0009
E	0.0006	0.0006	0.0005	0.0011
F	0.0005	0.0005	0.0005	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X5_P4**	**X2_P4**	**X5_P4**
A to Z ↓	0.0544	0.0559	8.0745	4.1987
A to Z ↑	0.0388	0.0378	12.0269	6.2573
B to Z ↓	0.0523	0.0539	8.0474	4.1875
B to Z ↑	0.0415	0.0407	12.0223	6.2512
C to Z ↓	0.0506	0.0523	8.0649	4.1951
C to Z ↑	0.0361	0.0353	11.9120	6.2055
D to Z ↓	0.0467	0.0484	8.0427	4.1833
D to Z ↑	0.0377	0.0370	11.9049	6.2054
E to Z ↓	0.0417	0.0433	8.0377	4.1821
E to Z ↑	0.0300	0.0292	11.8284	6.1722
F to Z ↓	0.0387	0.0405	8.0172	4.1716
F to Z ↑	0.0314	0.0309	11.8338	6.1728
	X10_P4	**X19_P4**	**X10_P4**	**X19_P4**
A to Z ↓	0.0596	0.0547	2.0276	1.0399
A to Z ↑	0.0399	0.0362	2.9782	1.4928
B to Z ↓	0.0564	0.0529	2.0155	1.0383
B to Z ↑	0.0413	0.0385	2.9774	1.4923
C to Z ↓	0.0543	0.0505	2.0217	1.0387
C to Z ↑	0.0356	0.0333	2.9625	1.4827
D to Z ↓	0.0526	0.0489	2.0160	1.0372
D to Z ↑	0.0380	0.0356	2.9623	1.4826
E to Z ↓	0.0473	0.0454	2.0157	1.0365
E to Z ↑	0.0305	0.0291	2.9478	1.4776
F to Z ↓	0.0449	0.0429	2.0098	1.0339
F to Z ↑	0.0324	0.0311	2.9453	1.4754

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P4	1.787e-05	1.000e-20
X5_P4	2.311e-05	1.000e-20
X10_P4	3.891e-05	1.000e-20
X19_P4	7.356e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P4	X5_P4	X10_P4	X19_P4
A (output stable)	1.742e-05	1.743e-05	2.768e-05	4.006e-05
B (output stable)	1.868e-05	1.872e-05	5.020e-05	4.376e-05
C (output stable)	2.661e-05	2.665e-05	2.703e-05	5.583e-05
D (output stable)	3.071e-05	3.076e-05	3.152e-05	6.567e-05
E (output stable)	5.987e-05	5.998e-05	7.926e-05	1.259e-04
F (output stable)	6.564e-05	6.573e-05	8.034e-05	1.342e-04

A to Z	1.916e-03	2.213e-03	3.496e-03	6.374e-03
B to Z	1.848e-03	2.144e-03	3.287e-03	6.177e-03
C to Z	1.603e-03	1.895e-03	3.073e-03	5.634e-03
D to Z	1.518e-03	1.807e-03	2.993e-03	5.481e-03
E to Z	1.258e-03	1.536e-03	2.663e-03	4.994e-03
F to Z	1.194e-03	1.472e-03	2.579e-03	4.816e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

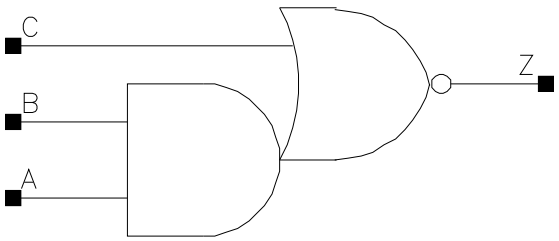
Pin Cycle (vdds)	X2_P4	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X10_P4	0.800	1.360	1.0880
X19_P4	0.800	2.584	2.0672
X25_P4	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P4	X10_P4	X19_P4	X25_P4
A	0.0005	0.0013	0.0026	0.0034
B	0.0004	0.0012	0.0024	0.0032
C	0.0005	0.0014	0.0026	0.0035

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X10_P4**	**X3_P4**	**X10_P4**
A to Z ↓	0.0099	0.0105	6.6737	2.3965
A to Z ↑	0.0183	0.0186	11.2603	3.8351
B to Z ↓	0.0105	0.0108	6.7294	2.4171
B to Z ↑	0.0157	0.0152	11.0969	3.8260
C to Z ↓	0.0103	0.0105	3.9665	1.3807
C to Z ↑	0.0188	0.0189	10.2861	3.5277
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0111	0.0111	1.2177	0.9273

A to Z ↑	0.0192	0.0189	1.9534	1.4573
B to Z ↓	0.0108	0.0109	1.2292	0.9354
B to Z ↑	0.0154	0.0154	1.9515	1.4700
C to Z ↓	0.0122	0.0123	0.8415	0.6483
C to Z ↑	0.0192	0.0191	1.7990	1.3480

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.396e-05	1.000e-20
X10_P4	3.730e-05	1.000e-20
X19_P4	7.089e-05	1.000e-20
X25_P4	9.366e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X10_P4	X19_P4	X25_P4
A (output stable)	2.944e-05	1.063e-04	2.148e-04	2.811e-04
B (output stable)	3.794e-05	1.333e-04	2.705e-04	3.503e-04
C (output stable)	4.405e-05	1.427e-04	2.835e-04	3.869e-04
A to Z	5.870e-04	1.824e-03	3.789e-03	4.933e-03
B to Z	5.074e-04	1.448e-03	2.950e-03	3.903e-03
C to Z	8.025e-04	2.388e-03	4.755e-03	6.328e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

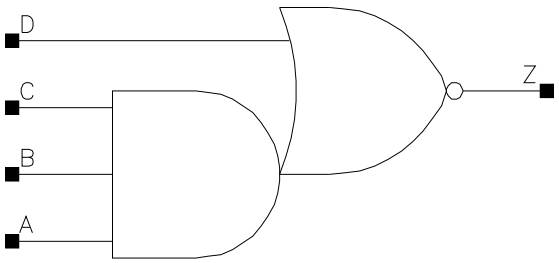
Pin Cycle (vdds)	X3_P4	X10_P4	X19_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X17_P4	0.800	3.536	2.8288
X22_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X17_P4	X22_P4
A	0.0005	0.0026	0.0035
B	0.0004	0.0024	0.0033
C	0.0006	0.0023	0.0031
D	0.0005	0.0027	0.0035

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X17_P4	X3_P4	X17_P4
A to Z ↓	0.0153	0.0162	9.4840	1.7746
A to Z ↑	0.0238	0.0230	11.2576	1.8988
B to Z ↓	0.0160	0.0162	9.5059	1.7803
B to Z ↑	0.0217	0.0207	11.2670	1.9205
C to Z ↓	0.0174	0.0153	9.5464	1.7858
C to Z ↑	0.0209	0.0174	11.3086	1.9290
D to Z ↓	0.0128	0.0144	3.8736	0.8301

D to Z ↑	0.0239	0.0222	9.6717	1.6412
	X22_P4		**X22_P4**	
A to Z ↓	0.0161		1.3456	
A to Z ↑	0.0227		1.4213	
B to Z ↓	0.0160		1.3508	
B to Z ↑	0.0203		1.4414	
C to Z ↓	0.0152		1.3553	
C to Z ↑	0.0171		1.4503	
D to Z ↓	0.0151		0.6889	
D to Z ↑	0.0215		1.2289	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.478e-05	1.000e-20
X17_P4	6.883e-05	1.000e-20
X22_P4	8.868e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X17_P4	X22_P4
A (output stable)	2.400e-05	1.530e-04	2.008e-04
B (output stable)	2.515e-05	1.659e-04	2.172e-04
C (output stable)	3.202e-05	2.759e-04	3.600e-04
D (output stable)	6.876e-05	4.188e-04	5.470e-04
A to Z	8.987e-04	5.144e-03	6.688e-03
B to Z	8.009e-04	4.338e-03	5.618e-03
C to Z	7.273e-04	3.535e-03	4.581e-03
D to Z	1.157e-03	6.153e-03	7.976e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

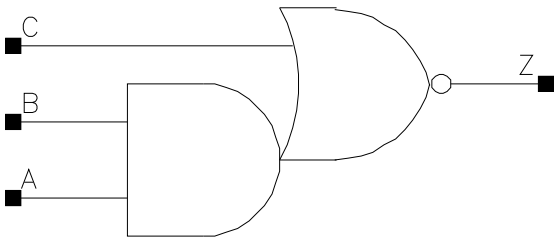
Pin Cycle (vdds)	X3_P4	X17_P4	X22_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X6_P4	0.800	1.088	0.8704
X9_P4	0.800	1.360	1.0880
X12_P4	0.800	1.904	1.5232
X25_P4	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X9_P4	X12_P4
A	0.0004	0.0010	0.0014	0.0020
B	0.0004	0.0009	0.0013	0.0018
C	0.0005	0.0008	0.0012	0.0016
	X25_P4			
A	0.0039			
B	0.0036			
C	0.0032			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0137	0.0133	8.9448	3.4971
A to Z ↑	0.0207	0.0219	12.9206	5.7098
B to Z ↓	0.0154	0.0133	8.9863	3.5209

B to Z ↑	0.0191	0.0186	12.7875	5.7231
C to Z ↓	0.0090	0.0077	5.3624	2.5154
C to Z ↑	0.0163	0.0148	11.8584	5.2705
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0126	0.0131	2.4024	1.8005
A to Z ↑	0.0204	0.0208	3.8216	2.8355
B to Z ↓	0.0131	0.0130	2.4208	1.8146
B to Z ↑	0.0171	0.0173	3.8221	2.8631
C to Z ↓	0.0077	0.0075	1.7271	1.2840
C to Z ↑	0.0139	0.0142	3.5289	2.6335
	X25_P4		**X25_P4**	
A to Z ↓	0.0129		0.9358	
A to Z ↑	0.0201		1.4349	
B to Z ↓	0.0131		0.9420	
B to Z ↑	0.0168		1.4394	
C to Z ↓	0.0074		0.6538	
C to Z ↑	0.0136		1.3303	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.088e-05	1.000e-20
X6_P4	2.624e-05	1.000e-20
X9_P4	3.637e-05	1.000e-20
X12_P4	4.924e-05	1.000e-20
X25_P4	9.524e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.045e-05	3.565e-05	4.631e-05	6.838e-05
B (output stable)	1.323e-05	5.873e-05	6.879e-05	1.089e-04
C (output stable)	1.243e-04	3.310e-04	4.008e-04	5.613e-04
A to Z	7.205e-04	1.778e-03	2.415e-03	3.349e-03
B to Z	6.539e-04	1.476e-03	1.989e-03	2.704e-03
C to Z	4.581e-04	9.995e-04	1.367e-03	1.899e-03
	X25_P4			
A (output stable)	1.299e-04			
B (output stable)	1.928e-04			
C (output stable)	1.042e-03			
A to Z	6.360e-03			
B to Z	5.207e-03			
C to Z	3.569e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

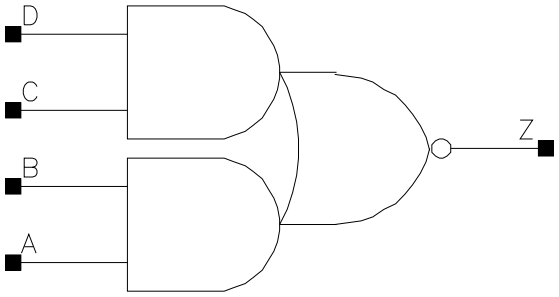
	X25_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.680	0.5440
X6_P4	0.800	1.224	0.9792
X9_P4	0.800	1.768	1.4144
X12_P4	0.800	2.448	1.9584
X24_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P4	X6_P4	X9_P4	X12_P4
A	0.0004	0.0010	0.0014	0.0019
B	0.0004	0.0009	0.0013	0.0019
C	0.0004	0.0010	0.0013	0.0018
D	0.0004	0.0008	0.0012	0.0017
	X24_P4			
A	0.0038			
B	0.0037			
C	0.0035			
D	0.0033			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X6_P4**	**X2_P4**	**X6_P4**
A to Z ↓	0.0137	0.0140	9.0815	3.4007
A to Z ↑	0.0264	0.0226	16.3726	5.2166
B to Z ↓	0.0151	0.0152	9.1392	3.4186
B to Z ↑	0.0239	0.0203	16.3348	5.3030
C to Z ↓	0.0100	0.0099	9.0888	3.4093
C to Z ↑	0.0206	0.0179	16.2988	5.1963
D to Z ↓	0.0109	0.0107	9.1646	3.4353
D to Z ↑	0.0181	0.0158	16.2532	5.3167
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0150	0.0155	2.4049	1.8066
A to Z ↑	0.0237	0.0242	3.5036	2.6318
B to Z ↓	0.0161	0.0162	2.4198	1.8181
B to Z ↑	0.0210	0.0214	3.5051	2.6085
C to Z ↓	0.0108	0.0114	2.3985	1.8073
C to Z ↑	0.0189	0.0195	3.4919	2.6095
D to Z ↓	0.0113	0.0111	2.4205	1.8239
D to Z ↑	0.0159	0.0161	3.4897	2.6165
	X24_P4		**X24_P4**	
A to Z ↓	0.0155		0.9281	
A to Z ↑	0.0238		1.3266	
B to Z ↓	0.0163		0.9340	
B to Z ↑	0.0210		1.3190	
C to Z ↓	0.0114		0.9112	
C to Z ↑	0.0194		1.3198	
D to Z ↓	0.0113		0.9206	
D to Z ↑	0.0161		1.3228	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P4	1.001e-05	1.000e-20
X6_P4	3.147e-05	1.000e-20
X9_P4	4.472e-05	1.000e-20
X12_P4	5.992e-05	1.000e-20
X24_P4	1.161e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.226e-05	3.133e-05	6.213e-05	9.215e-05
B (output stable)	1.515e-05	4.258e-05	1.087e-04	1.738e-04
C (output stable)	3.132e-05	6.983e-05	1.263e-04	1.816e-04
D (output stable)	3.715e-05	8.641e-05	1.687e-04	2.506e-04
A to Z	7.506e-04	1.979e-03	3.128e-03	4.302e-03
B to Z	6.699e-04	1.759e-03	2.712e-03	3.727e-03
C to Z	4.579e-04	1.242e-03	2.002e-03	2.808e-03
D to Z	3.936e-04	1.074e-03	1.644e-03	2.252e-03
	X24_P4			
A (output stable)	1.689e-04			
B (output stable)	2.911e-04			
C (output stable)	3.440e-04			
D (output stable)	4.912e-04			

A to Z	8.322e-03			
B to Z	7.240e-03			
C to Z	5.471e-03			
D to Z	4.439e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

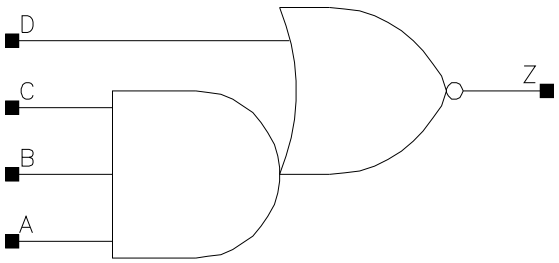
Pin Cycle (vdds)	X2_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X12_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X12_P4
A	0.0005	0.0019
B	0.0005	0.0018
C	0.0007	0.0017
D	0.0005	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X12_P4	X3_P4	X12_P4
A to Z ↓	0.0176	0.0181	9.5069	2.6381
A to Z ↑	0.0258	0.0244	11.0689	2.8688
B to Z ↓	0.0188	0.0181	9.5271	2.6447
B to Z ↑	0.0243	0.0220	11.1821	2.8684
C to Z ↓	0.0212	0.0175	9.5628	2.6503
C to Z ↑	0.0242	0.0189	11.2548	2.8821
D to Z ↓	0.0084	0.0070	3.9381	1.0688
D to Z ↑	0.0174	0.0148	9.5466	2.4520

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.497e-05	1.000e-20
X12_P4	4.993e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X12_P4
A (output stable)	9.006e-06	5.131e-05
B (output stable)	1.018e-05	6.420e-05
C (output stable)	2.183e-05	1.258e-04
D (output stable)	2.442e-04	8.146e-04
A to Z	1.141e-03	4.184e-03
B to Z	1.045e-03	3.576e-03
C to Z	9.854e-04	3.013e-03
D to Z	6.557e-04	2.108e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

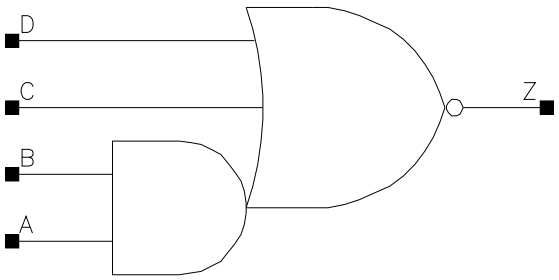
Pin Cycle (vdds)	X3_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X20_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P4	X20_P4
A	0.0004	0.0035
B	0.0004	0.0032
C	0.0005	0.0034
D	0.0005	0.0031

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X20_P4	X3_P4	X20_P4
A to Z ↓	0.0117	0.0128	6.5479	1.0485
A to Z ↑	0.0247	0.0233	16.3855	2.1140
B to Z ↓	0.0129	0.0131	6.5960	1.0580
B to Z ↑	0.0224	0.0192	16.4974	2.1149
C to Z ↓	0.0125	0.0170	3.9297	0.8226
C to Z ↑	0.0296	0.0277	15.5984	2.0009
D to Z ↓	0.0122	0.0157	3.9277	0.8210

D to Z ↑	0.0299	0.0258	15.6198	2.0046

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.235e-05	1.000e-20
X20_P4	7.341e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X20_P4
A (output stable)	5.237e-05	3.651e-04
B (output stable)	5.631e-05	3.916e-04
C (output stable)	2.610e-05	2.899e-04
D (output stable)	3.441e-05	3.766e-04
A to Z	7.644e-04	5.222e-03
B to Z	6.830e-04	4.267e-03
C to Z	1.148e-03	8.304e-03
D to Z	1.025e-03	6.737e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

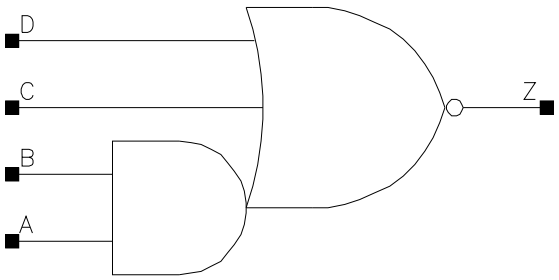
Pin Cycle (vdds)	X3_P4	X20_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.816	0.6528
X10_P4	0.800	2.448	1.9584
X19_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P4	X10_P4	X19_P4
A	0.0005	0.0018	0.0037
B	0.0005	0.0017	0.0034
C	0.0006	0.0015	0.0030
D	0.0004	0.0014	0.0028

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	X10_P4	X2_P4	X10_P4
A to Z ↓	0.0153	0.0155	7.8412	2.0722
A to Z ↑	0.0306	0.0281	17.3634	4.2101
B to Z ↓	0.0170	0.0160	7.8875	2.0854
B to Z ↑	0.0280	0.0243	17.4148	4.2211
C to Z ↓	0.0142	0.0128	6.8850	1.7331
C to Z ↑	0.0230	0.0207	16.4868	3.9914

D to Z ↓	0.0122	0.0100	6.9238	1.7457
D to Z ↑	0.0211	0.0170	16.4969	3.9996
	X19_P4		**X19_P4**	
A to Z ↓	0.0151		1.0598	
A to Z ↑	0.0274		2.1298	
B to Z ↓	0.0159		1.0668	
B to Z ↑	0.0235		2.1306	
C to Z ↓	0.0132		0.9125	
C to Z ↑	0.0199		2.0176	
D to Z ↓	0.0103		0.9193	
D to Z ↑	0.0162		2.0222	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P4	9.887e-06	1.000e-20
X10_P4	3.927e-05	1.000e-20
X19_P4	7.671e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P4	X10_P4	X19_P4
A (output stable)	1.246e-05	5.242e-05	1.056e-04
B (output stable)	1.243e-05	7.160e-05	1.324e-04
C (output stable)	3.303e-05	1.614e-04	3.206e-04
D (output stable)	7.655e-05	3.845e-04	7.315e-04
A to Z	1.084e-03	4.043e-03	7.762e-03
B to Z	9.923e-04	3.471e-03	6.677e-03
C to Z	6.854e-04	2.604e-03	4.923e-03
D to Z	5.674e-04	1.868e-03	3.481e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

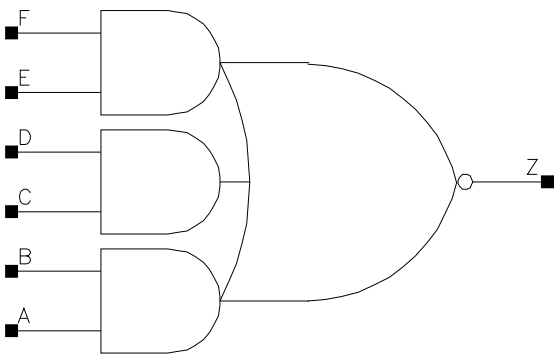
Pin Cycle (vdds)	X2_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.088	0.8704
X5_P4	0.800	2.040	1.6320
X7_P4	0.800	2.720	2.1760
X9_P4	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P4	X5_P4	X7_P4	X9_P4
A	0.0005	0.0008	0.0014	0.0018

B	0.0005	0.0010	0.0012	0.0016
C	0.0005	0.0008	0.0013	0.0019
D	0.0004	0.0009	0.0012	0.0016
E	0.0006	0.0009	0.0012	0.0016
F	0.0004	0.0007	0.0011	0.0015

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X5_P4**	**X2_P4**	**X5_P4**
A to Z ↓	0.0165	0.0202	6.9314	3.9717
A to Z ↑	0.0392	0.0366	16.8067	7.5751
B to Z ↓	0.0183	0.0224	6.9719	3.9845
B to Z ↑	0.0363	0.0348	16.8627	7.5300
C to Z ↓	0.0154	0.0183	6.9933	3.9499
C to Z ↑	0.0342	0.0325	16.8870	7.5907
D to Z ↓	0.0170	0.0202	7.0481	3.9682
D to Z ↑	0.0314	0.0309	16.8707	7.5609
E to Z ↓	0.0119	0.0143	7.0173	3.8980
E to Z ↑	0.0266	0.0262	16.8262	7.5277
F to Z ↓	0.0127	0.0154	7.0861	3.9185
F to Z ↑	0.0230	0.0235	16.7808	7.5448
	X7_P4	**X9_P4**	**X7_P4**	**X9_P4**
A to Z ↓	0.0197	0.0202	2.7421	2.0851
A to Z ↑	0.0355	0.0365	4.9880	3.7628
B to Z ↓	0.0212	0.0213	2.7525	2.0933
B to Z ↑	0.0327	0.0332	5.0696	3.8061
C to Z ↓	0.0179	0.0185	2.7535	2.0721
C to Z ↑	0.0318	0.0333	5.0616	3.8088
D to Z ↓	0.0193	0.0189	2.7675	2.0815
D to Z ↑	0.0287	0.0290	5.0292	3.7848
E to Z ↓	0.0134	0.0134	2.7476	2.0717
E to Z ↑	0.0246	0.0246	5.0064	3.7812
F to Z ↓	0.0143	0.0136	2.7700	2.0891
F to Z ↑	0.0216	0.0210	5.0372	3.7768

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P4	1.732e-05	1.000e-20
X5_P4	3.544e-05	1.000e-20
X7_P4	5.116e-05	1.000e-20
X9_P4	6.635e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P4	X5_P4	X7_P4	X9_P4
A (output stable)	2.025e-05	3.790e-05	6.836e-05	9.556e-05
B (output stable)	2.243e-05	4.883e-05	9.162e-05	1.455e-04
C (output stable)	3.475e-05	6.504e-05	9.528e-05	1.371e-04
D (output stable)	3.911e-05	7.448e-05	1.254e-04	1.788e-04
E (output stable)	6.432e-05	1.406e-04	2.101e-04	3.060e-04
F (output stable)	7.736e-05	1.494e-04	2.368e-04	3.514e-04

A to Z	1.464e-03	2.999e-03	4.355e-03	5.954e-03
B to Z	1.359e-03	2.869e-03	3.975e-03	5.386e-03
C to Z	1.115e-03	2.357e-03	3.395e-03	4.624e-03
D to Z	1.020e-03	2.231e-03	3.058e-03	4.121e-03
E to Z	7.369e-04	1.711e-03	2.346e-03	3.107e-03
F to Z	6.540e-04	1.552e-03	2.039e-03	2.623e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

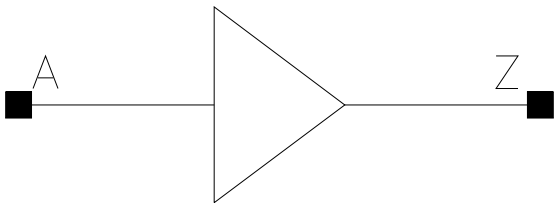
Pin Cycle (vdds)	X2_P4	X5_P4	X7_P4	X9_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.544	0.4352
X5_P4	0.800	0.544	0.4352
X9_P4	0.800	0.680	0.5440
X11_P4	1.600	0.408	0.6528
X13_P4	0.800	0.680	0.5440
X19_P4	0.800	0.952	0.7616
X23_P4	1.600	0.544	0.8704
X24_P4	0.800	1.088	0.8704
X29_P4	0.800	1.224	0.9792
X34_P4	1.600	0.680	1.0880
X38_P4	0.800	1.632	1.3056
X46_P4	1.600	0.952	1.5232
X57_P4	0.800	2.312	1.8496
X68_P4	1.600	1.224	1.9584
X91_P4	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P4	X5_P4	X9_P4	X11_P4
A	0.0005	0.0005	0.0005	0.0007
	X13_P4	X19_P4	X23_P4	X24_P4
A	0.0007	0.0009	0.0011	0.0010
	X29_P4	X34_P4	X38_P4	X46_P4
A	0.0012	0.0013	0.0018	0.0018
	X57_P4	X68_P4	X91_P4	
A	0.0023	0.0024	0.0033	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X5_P4**	**X2_P4**	**X5_P4**
A to Z ↓	0.0274	0.0279	7.7794	4.0277
A to Z ↑	0.0215	0.0211	11.7352	6.0822
	X9_P4	**X11_P4**	**X9_P4**	**X11_P4**
A to Z ↓	0.0329	0.0304	2.0602	1.5018
A to Z ↑	0.0249	0.0221	3.0257	2.8509
	X13_P4	**X19_P4**	**X13_P4**	**X19_P4**
A to Z ↓	0.0286	0.0287	1.4064	0.9944
A to Z ↑	0.0228	0.0214	2.0820	1.4682
	X23_P4	**X24_P4**	**X23_P4**	**X24_P4**
A to Z ↓	0.0291	0.0282	0.7276	0.8090
A to Z ↑	0.0209	0.0220	1.4339	1.1763
	X29_P4	**X34_P4**	**X29_P4**	**X34_P4**
A to Z ↓	0.0270	0.0286	0.6712	0.5001
A to Z ↑	0.0214	0.0212	0.9863	0.9763
	X38_P4	**X46_P4**	**X38_P4**	**X46_P4**
A to Z ↓	0.0264	0.0278	0.5078	0.3761
A to Z ↑	0.0211	0.0203	0.7298	0.7330
	X57_P4	**X68_P4**	**X57_P4**	**X68_P4**
A to Z ↓	0.0275	0.0273	0.3411	0.2548
A to Z ↑	0.0219	0.0202	0.4880	0.4902
	X91_P4		**X91_P4**	
A to Z ↓	0.0287		0.1959	
A to Z ↑	0.0212		0.3686	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P4	9.076e-06	1.000e-20
X5_P4	1.498e-05	1.000e-20
X9_P4	2.516e-05	1.000e-20
X11_P4	3.305e-05	1.000e-20
X13_P4	3.857e-05	1.000e-20
X19_P4	4.992e-05	1.000e-20
X23_P4	6.442e-05	1.000e-20
X24_P4	6.257e-05	1.000e-20
X29_P4	7.593e-05	1.000e-20
X34_P4	9.202e-05	1.000e-20
X38_P4	1.026e-04	1.000e-20
X46_P4	1.181e-04	1.000e-20
X57_P4	1.472e-04	1.000e-20
X68_P4	1.748e-04	1.000e-20
X91_P4	2.239e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P4	X5_P4	X9_P4	X11_P4
A to Z	8.528e-04	1.101e-03	1.770e-03	2.131e-03
	X13_P4	X19_P4	X23_P4	X24_P4
A to Z	2.561e-03	3.441e-03	3.902e-03	4.281e-03
	X29_P4	X34_P4	X38_P4	X46_P4

A to Z	4.987e-03	5.862e-03	6.832e-03	7.439e-03
	X57_P4	X68_P4	X91_P4	
A to Z	1.010e-02	1.087e-02	1.465e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

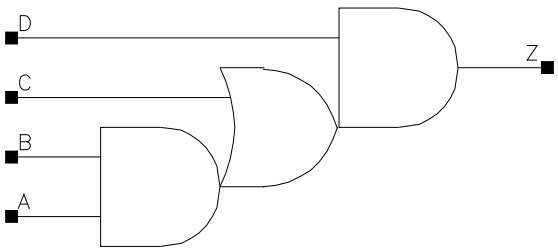
Pin Cycle (vdds)	X2_P4	X5_P4	X9_P4	X11_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P4	X19_P4	X23_P4	X24_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P4	X34_P4	X38_P4	X46_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P4	X68_P4	X91_P4	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.952	0.7616
X10_P4	0.800	1.632	1.3056
X14_P4	0.800	1.768	1.4144
X19_P4	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0005	0.0012	0.0012	0.0012
B	0.0006	0.0011	0.0010	0.0010
C	0.0006	0.0013	0.0013	0.0013
D	0.0009	0.0011	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0361	0.0327	4.1105	1.9390
A to Z ↑	0.0341	0.0306	6.2000	2.9517
B to Z ↓	0.0340	0.0304	4.0994	1.9384
B to Z ↑	0.0350	0.0311	6.2007	2.9461
C to Z ↓	0.0310	0.0276	4.0936	1.9353
C to Z ↑	0.0256	0.0225	6.1467	2.9197

D to Z ↓	0.0301	0.0254	4.0649	1.9217
D to Z ↑	0.0297	0.0247	6.1561	2.9256
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0364	0.0392	1.3465	1.0132
A to Z ↑	0.0341	0.0367	1.9815	1.4896
B to Z ↓	0.0342	0.0372	1.3446	1.0120
B to Z ↑	0.0347	0.0373	1.9827	1.4879
C to Z ↓	0.0311	0.0340	1.3412	1.0085
C to Z ↑	0.0252	0.0272	1.9556	1.4679
D to Z ↓	0.0277	0.0295	1.3267	0.9953
D to Z ↑	0.0273	0.0292	1.9610	1.4714

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.360e-05	1.000e-20
X10_P4	4.703e-05	1.000e-20
X14_P4	5.649e-05	1.000e-20
X19_P4	6.597e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	2.480e-05	4.690e-05	4.773e-05	4.803e-05
B (output stable)	3.226e-05	5.979e-05	6.132e-05	6.129e-05
C (output stable)	1.113e-04	1.793e-04	1.808e-04	1.814e-04
D (output stable)	5.472e-05	8.286e-05	8.402e-05	8.433e-05
A to Z	1.820e-03	3.277e-03	4.237e-03	5.141e-03
B to Z	1.727e-03	3.053e-03	4.007e-03	4.910e-03
C to Z	1.478e-03	2.550e-03	3.429e-03	4.249e-03
D to Z	1.855e-03	3.202e-03	4.048e-03	4.817e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

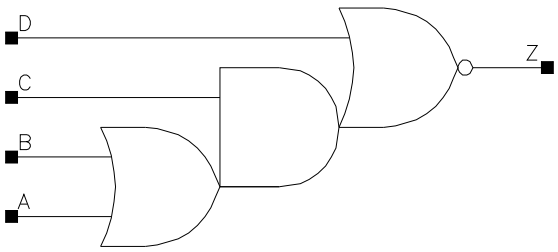
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X6_P4	0.800	1.496	1.1968
X9_P4	0.800	1.768	1.4144
X12_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X9_P4	X12_P4
A	0.0005	0.0010	0.0015	0.0019
B	0.0005	0.0009	0.0014	0.0019
C	0.0005	0.0009	0.0013	0.0018
D	0.0006	0.0009	0.0013	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0158	0.0144	6.7819	3.4638
A to Z ↑	0.0319	0.0311	16.4420	8.5570
B to Z ↓	0.0151	0.0142	6.6248	3.4832
B to Z ↑	0.0317	0.0299	16.4484	8.5663
C to Z ↓	0.0142	0.0131	6.2573	3.2374
C to Z ↑	0.0206	0.0192	11.2828	5.7930

D to Z ↓	0.0085	0.0067	3.9651	2.0196
D to Z ↑	0.0195	0.0164	11.9889	6.1743
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0144	0.0148	2.3821	1.8383
A to Z ↑	0.0287	0.0304	5.5617	4.2617
B to Z ↓	0.0139	0.0141	2.3968	1.8363
B to Z ↑	0.0287	0.0292	5.5666	4.2663
C to Z ↓	0.0133	0.0133	2.2369	1.7143
C to Z ↑	0.0184	0.0186	3.7904	2.8766
D to Z ↓	0.0069	0.0068	1.4042	1.0730
D to Z ↑	0.0153	0.0151	4.0321	3.0682

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.471e-05	1.000e-20
X6_P4	2.802e-05	1.000e-20
X9_P4	3.872e-05	1.000e-20
X12_P4	5.110e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.013e-05	2.548e-05	3.044e-05	5.225e-05
B (output stable)	1.176e-05	2.787e-05	3.743e-05	6.587e-05
C (output stable)	3.841e-05	8.556e-05	1.154e-04	1.580e-04
D (output stable)	1.336e-04	3.537e-04	4.850e-04	7.383e-04
A to Z	1.179e-03	2.225e-03	3.080e-03	4.296e-03
B to Z	1.043e-03	1.868e-03	2.694e-03	3.621e-03
C to Z	8.624e-04	1.563e-03	2.236e-03	3.041e-03
D to Z	6.197e-04	1.034e-03	1.440e-03	1.891e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

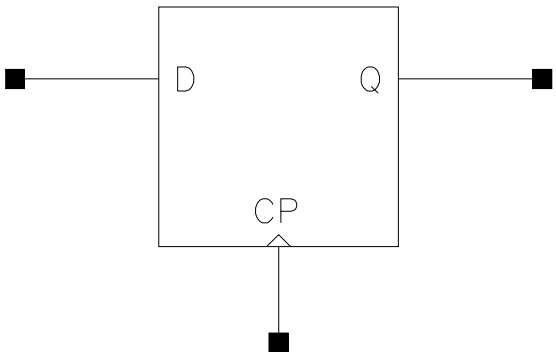
Pin Cycle (vdds)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	1.600	1.496	2.3936
X19_P4	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P4	X19_P4
CP	0.0008	0.0008
D	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P4	X19_P4	X10_P4	X19_P4
CP to Q ↓	0.0541	0.0729	2.0109	1.0863
CP to Q ↑	0.0637	0.0729	2.9234	1.4970

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P4	X19_P4
CP ↓	min_pulse_width to CP	0.0537	0.0537
CP ↑	min_pulse_width to CP	0.0456	0.0644
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0107	0.0107
D ↓	setup_rising to CP	0.0273	0.0273
D ↑	setup_rising to CP	0.0200	0.0200

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P4	7.113e-05	1.000e-20
X19_P4	8.915e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

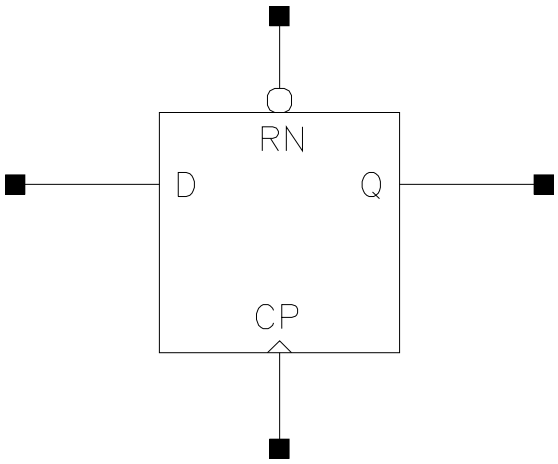
Pin Cycle	X10_P4	X19_P4
Clock 100Mhz Data 0Mhz	5.816e-03	5.820e-03
Clock 100Mhz Data 25Mhz	7.063e-03	8.512e-03
Clock 100Mhz Data 50Mhz	8.309e-03	1.120e-02
Clock = 0 Data 100Mhz	2.302e-03	2.301e-03
Clock = 1 Data 100Mhz	1.431e-05	1.440e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	1.600	1.768	2.8288
X19_P4	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P4	X19_P4
CP	0.0008	0.0008
D	0.0006	0.0006
RN	0.0007	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P4	X19_P4	X10_P4	X19_P4
CP to Q ↓	0.0592	0.0756	2.0435	1.0734
CP to Q ↑	0.0666	0.0755	2.9128	1.4840
RN to Q ↓	0.0610	0.0781	2.0058	1.0363

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P4	X19_P4
CP ↓	min_pulse_width to CP	0.0571	0.0571
CP ↑	min_pulse_width to CP	0.0468	0.0644
D ↓	hold_rising to CP	0.0173	0.0173
D ↑	hold_rising to CP	0.0049	0.0049
D ↓	setup_rising to CP	0.0273	0.0273
D ↑	setup_rising to CP	0.0200	0.0200
RN ↓	min_pulse_width to RN	0.0735	0.0925
RN ↑	recovery_rising to CP	0.0103	0.0103
RN ↑	removal_rising to CP	-0.0029	-0.0055

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P4	8.055e-05	1.000e-20
X19_P4	1.022e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

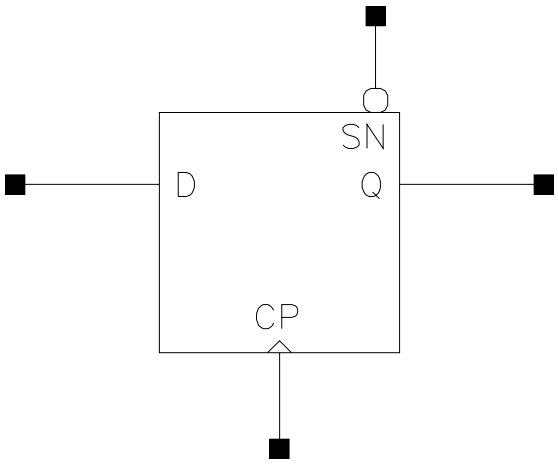
Pin Cycle	X10_P4	X19_P4
Clock 100Mhz Data 0Mhz	5.902e-03	5.903e-03
Clock 100Mhz Data 25Mhz	7.262e-03	8.695e-03
Clock 100Mhz Data 50Mhz	8.622e-03	1.149e-02
Clock = 0 Data 100Mhz	2.305e-03	2.306e-03
Clock = 1 Data 100Mhz	1.448e-05	1.449e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	1.600	1.768	2.8288
X19_P4	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P4	X19_P4
CP	0.0008	0.0008
D	0.0006	0.0006
SN	0.0009	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P4	X19_P4	X10_P4	X19_P4
CP to Q ↓	0.0556	0.0738	2.0241	1.0658
CP to Q ↑	0.0659	0.0757	2.9121	1.4884
SN to Q ↑	0.0401	0.0455	2.8585	1.4484

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P4	X19_P4
CP ↓	min_pulse_width to CP	0.0571	0.0571
CP ↑	min_pulse_width to CP	0.0456	0.0644
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0107	0.0103
D ↓	setup_rising to CP	0.0273	0.0273
D ↑	setup_rising to CP	0.0200	0.0200
SN ↓	min_pulse_width to SN	0.0447	0.0474
SN ↑	recovery_rising to CP	0.0032	0.0032
SN ↑	removal_rising to CP	0.0334	0.0334

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P4	8.267e-05	1.000e-20
X19_P4	1.030e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

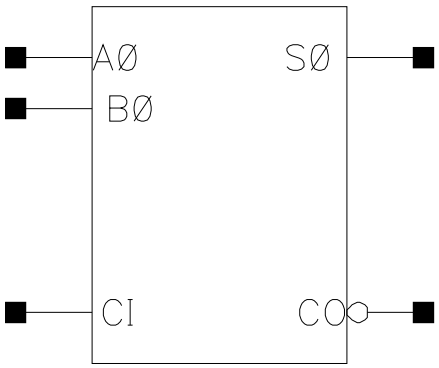
Pin Cycle	X10_P4	X19_P4
Clock 100Mhz Data 0Mhz	5.788e-03	5.791e-03
Clock 100Mhz Data 25Mhz	7.088e-03	8.581e-03
Clock 100Mhz Data 50Mhz	8.389e-03	1.137e-02
Clock = 0 Data 100Mhz	2.206e-03	2.206e-03
Clock = 1 Data 100Mhz	1.444e-05	1.445e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_-P4	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_-P4	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_-P4	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_-P4	1.600	2.720	4.3520
C8T28SOIDV_LLS1_-FA1X4_P4	1.600	2.040	3.2640
C8T28SOIDV_LLS1_-FA1X9_P4	1.600	3.128	5.0048
C8T28SOIDV_LLS1_-FA1X18_P4	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P4	C8T28SOIDV_LL_-FA1X9_P4	C8T28SOIDV_LL_-FA1X14_P4	C8T28SOIDV_LL_-FA1X19_P4
A0	0.0020	0.0021	0.0033	0.0036
B0	0.0017	0.0018	0.0031	0.0033
CI	0.0013	0.0013	0.0023	0.0025
	C8T28SOIDV_LLS1_-FA1X4_P4	C8T28SOIDV_LLS1_-FA1X9_P4	C8T28SOIDV_LLS1_-FA1X18_P4	
A0	0.0020	0.0026	0.0027	
B0	0.0019	0.0030	0.0033	
CI	0.0014	0.0021	0.0025	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P4	**C8T28SOIDV_LL_-FA1X9_P4**	**C8T28SOIDV_LL_-FA1X5_P4**	**C8T28SOIDV_LL_-FA1X9_P4**
A0 to CO ↓	0.0475	0.0505	4.1743	2.1459
A0 to CO ↑	0.0358	0.0379	5.7831	2.9558
A0 to S0 ↓	0.0519	0.0560	4.1291	2.1245
A0 to S0 ↑	0.0536	0.0573	5.7855	2.9059
B0 to CO ↓	0.0474	0.0505	4.1905	2.1539
B0 to CO ↑	0.0370	0.0390	5.7889	2.9570
B0 to S0 ↓	0.0522	0.0565	4.1259	2.1257
B0 to S0 ↑	0.0542	0.0581	5.7854	2.9070
CI to CO ↓	0.0448	0.0475	4.1877	2.1509
CI to CO ↑	0.0361	0.0379	5.7810	2.9517
CI to S0 ↓	0.0517	0.0561	4.1297	2.1242
CI to S0 ↑	0.0537	0.0575	5.7846	2.9068
	C8T28SOIDV_LL_-FA1X14_P4	**C8T28SOIDV_LL_-FA1X19_P4**	**C8T28SOIDV_LL_-FA1X14_P4**	**C8T28SOIDV_LL_-FA1X19_P4**
A0 to CO ↓	0.0481	0.0526	1.3887	1.0578
A0 to CO ↑	0.0362	0.0374	2.0172	1.5085
A0 to S0 ↓	0.0593	0.0595	1.3851	1.0304
A0 to S0 ↑	0.0611	0.0626	1.9618	1.4646
B0 to CO ↓	0.0472	0.0516	1.3935	1.0603
B0 to CO ↑	0.0366	0.0377	2.0164	1.5074
B0 to S0 ↓	0.0595	0.0598	1.3851	1.0312
B0 to S0 ↑	0.0613	0.0627	1.9621	1.4649
CI to CO ↓	0.0446	0.0488	1.3903	1.0588
CI to CO ↑	0.0356	0.0367	2.0157	1.5073
CI to S0 ↓	0.0586	0.0589	1.3845	1.0307
CI to S0 ↑	0.0602	0.0616	1.9612	1.4651
	C8T28SOIDV_-LLS1_FA1X4_P4	**C8T28SOIDV_-LLS1_FA1X9_P4**	**C8T28SOIDV_-LLS1_FA1X4_P4**	**C8T28SOIDV_-LLS1_FA1X9_P4**
A0 to CO ↓	0.0318	0.0293	8.0289	2.5887
A0 to CO ↑	0.0283	0.0269	5.8240	2.9498
A0 to S0 ↓	0.0694	0.0755	4.4254	1.5630
A0 to S0 ↑	0.0656	0.0647	6.1388	2.8928
B0 to CO ↓	0.0302	0.0301	8.0205	2.5904
B0 to CO ↑	0.0244	0.0255	5.8066	2.9476
B0 to S0 ↓	0.0706	0.0787	4.4253	1.5631
B0 to S0 ↑	0.0669	0.0679	6.1327	2.8931
CI to CO ↓	0.0308	0.0416	8.0214	2.6088
CI to CO ↑	0.0267	0.0248	5.8256	2.9679

CI to S0 ↓	0.0389	0.0459	4.4288	1.5649
CI to S0 ↑	0.0347	0.0348	6.1379	2.8940
	C8T28SOIDV_-LLS1_FA1X18_P4		**C8T28SOIDV_-LLS1_FA1X18_P4**	
A0 to CO ↓	0.0367		1.3477	
A0 to CO ↑	0.0277		1.4490	
A0 to S0 ↓	0.0795		0.8071	
A0 to S0 ↑	0.0650		1.4488	
B0 to CO ↓	0.0382		1.3500	
B0 to CO ↑	0.0264		1.4475	
B0 to S0 ↓	0.0812		0.8072	
B0 to S0 ↑	0.0667		1.4492	
CI to CO ↓	0.0516		1.3612	
CI to CO ↑	0.0292		1.4514	
CI to S0 ↓	0.0468		0.8074	
CI to S0 ↑	0.0317		1.4502	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P4	5.607e-05	1.000e-20
C8T28SOIDV_LL_FA1X9_P4	7.803e-05	1.000e-20
C8T28SOIDV_LL_FA1X14_P4	1.162e-04	1.000e-20
C8T28SOIDV_LL_FA1X19_P4	1.452e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P4	1.224e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P4	1.834e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P4	2.775e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P4	C8T28SOIDV_LL_-FA1X9_P4	C8T28SOIDV_LL_-FA1X14_P4	C8T28SOIDV_LL_-FA1X19_P4
A0 to CO	2.016e-03	2.847e-03	4.695e-03	5.733e-03
A0 to S0	2.053e-03	2.786e-03	4.790e-03	5.840e-03
B0 to CO	2.032e-03	2.881e-03	4.721e-03	5.786e-03
B0 to S0	2.030e-03	2.780e-03	4.771e-03	5.818e-03
CI to CO	2.032e-03	2.859e-03	4.774e-03	5.864e-03
CI to S0	2.026e-03	2.780e-03	4.765e-03	5.800e-03
	C8T28SOIDV_LLS1_-FA1X4_P4	C8T28SOIDV_LLS1_-FA1X9_P4	C8T28SOIDV_LLS1_-FA1X18_P4	
A0 to CO	3.130e-03	4.804e-03	7.621e-03	
A0 to S0	4.234e-03	6.209e-03	9.503e-03	
B0 to CO	3.321e-03	4.880e-03	7.666e-03	
B0 to S0	4.562e-03	6.372e-03	9.627e-03	
CI to CO	2.249e-03	3.968e-03	6.709e-03	
CI to S0	2.532e-03	4.407e-03	7.248e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P4	C8T28SOIDV_LL_-FA1X9_P4	C8T28SOIDV_LL_-FA1X14_P4	C8T28SOIDV_LL_-FA1X19_P4
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P4	C8T28SOIDV_LLS1_-FA1X9_P4	C8T28SOIDV_LLS1_-FA1X18_P4	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P4	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P4	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P4	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P4	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P4	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P4	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P4	C8T28SOI_LL_-HA1X9_P4	C8T28SOI_LLS1_-HA1X5_P4	C8T28SOIDV_LL_-HA1X14_P4
A0	0.0007	0.0010	0.0012	0.0013
B0	0.0006	0.0010	0.0011	0.0012
	C8T28SOIDV_LL_-HA1X19_P4	C8T28SOIDV_LLS1_-HA1X11_P4		
A0	0.0016	0.0017		
B0	0.0014	0.0017		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P4	**C8T28SOI_LL_-HA1X9_P4**	**C8T28SOI_LL_-HA1X5_P4**	**C8T28SOI_LL_-HA1X9_P4**
A0 to CO ↓	0.0374	0.0311	4.1465	2.0290
A0 to CO ↑	0.0353	0.0298	6.1820	2.9650
A0 to S0 ↓	0.0489	0.0431	3.9829	2.0115
A0 to S0 ↑	0.0458	0.0408	6.0300	2.9525
B0 to CO ↓	0.0366	0.0305	4.1423	2.0296
B0 to CO ↑	0.0375	0.0322	6.1814	2.9652
B0 to S0 ↓	0.0503	0.0438	3.9861	2.0116
B0 to S0 ↑	0.0453	0.0403	6.0283	2.9527
	C8T28SOI_LLS1_-HA1X5_P4	**C8T28SOIDV_LL_-HA1X14_P4**	**C8T28SOI_LLS1_-HA1X5_P4**	**C8T28SOIDV_LL_-HA1X14_P4**
A0 to CO ↓	0.0299	0.0321	4.0578	1.3654
A0 to CO ↑	0.0280	0.0294	6.1050	1.9846
A0 to S0 ↓	0.0424	0.0481	4.0498	1.3728
A0 to S0 ↑	0.0474	0.0451	6.1453	1.9631
B0 to CO ↓	0.0286	0.0299	4.0594	1.3608
B0 to CO ↑	0.0296	0.0300	6.1062	1.9836
B0 to S0 ↓	0.0443	0.0473	4.0503	1.3740
B0 to S0 ↑	0.0470	0.0432	6.1426	1.9631
	C8T28SOIDV_LL_-HA1X19_P4	**C8T28SOIDV_-LLS1_HA1X11_P4**	**C8T28SOIDV_LL_-HA1X19_P4**	**C8T28SOIDV_-LLS1_HA1X11_P4**
A0 to CO ↓	0.0298	0.0284	0.9980	1.4217
A0 to CO ↑	0.0282	0.0295	1.4992	2.9186
A0 to S0 ↓	0.0437	0.0368	0.9918	1.4408
A0 to S0 ↑	0.0415	0.0390	1.4722	2.9439
B0 to CO ↓	0.0278	0.0270	0.9949	1.4170
B0 to CO ↑	0.0290	0.0315	1.4993	2.9184
B0 to S0 ↓	0.0437	0.0383	0.9916	1.4402
B0 to S0 ↑	0.0399	0.0389	1.4725	2.9420

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_HA1X5_P4	3.200e-05	1.000e-20
C8T28SOI_LL_HA1X9_P4	7.084e-05	1.000e-20
C8T28SOI_LLS1_HA1X5_P4	3.930e-05	1.000e-20
C8T28SOIDV_LL_HA1X14_P4	1.011e-04	1.000e-20
C8T28SOIDV_LL_HA1X19_P4	1.408e-04	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P4	9.665e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

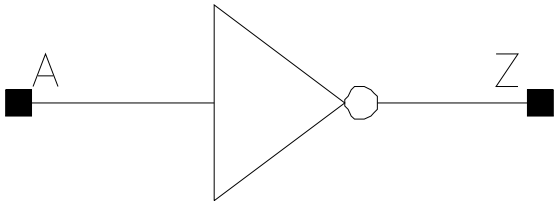
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P4	C8T28SOI_LL_-HA1X9_P4	C8T28SOI_LLS1_-HA1X5_P4	C8T28SOIDV_LL_-HA1X14_P4
A0 to CO	1.526e-03	2.446e-03	1.831e-03	3.953e-03
A0 to S0	1.383e-03	2.372e-03	1.624e-03	4.021e-03
B0 to CO	1.546e-03	2.548e-03	1.866e-03	3.965e-03
B0 to S0	1.368e-03	2.331e-03	1.593e-03	3.907e-03
	C8T28SOIDV_LL_-HA1X19_P4	C8T28SOIDV_LLS1_-HA1X11_P4		
A0 to CO	4.786e-03	3.493e-03		
A0 to S0	4.838e-03	3.183e-03		

B0 to CO	4.789e-03	3.227e-03		
B0 to S0	4.721e-03	3.254e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P4	C8T28SOI_LL_-HA1X9_P4	C8T28SOI_LLS1_-HA1X5_P4	C8T28SOIDV_LL_-HA1X14_P4
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P4	C8T28SOIDV_LLS1_-HA1X11_P4		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P4	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P4	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P4	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P4	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P4	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P4	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P4	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P4	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P4	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P4	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P4	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P4	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P4	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P4	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P4	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P4	C8T28SOI_LL_IVX3_-P4	C8T28SOI_LL_IVX5_-P4	C8T28SOI_LL_-IVX10_P4

A	0.0003	0.0004	0.0005	0.0009
	C8T28SOI_LL_-IVX14_P4	C8T28SOI_LL_-IVX19_P4	C8T28SOI_LL_-IVX29_P4	C8T28SOI_LL_-IVX34_P4
A	0.0014	0.0018	0.0026	0.0031
	C8T28SOI_LL_-IVX38_P4	C8T28SOIDV_LL_-IVX11_P4	C8T28SOIDV_LL_-IVX23_P4	C8T28SOIDV_LL_-IVX34_P4
A	0.0035	0.0010	0.0019	0.0028
	C8T28SOIDV_LL_-IVX46_P4	C8T28SOIDV_LL_-IVX68_P4	C8T28SOIDV_LL_-IVX91_P4	
A	0.0038	0.0058	0.0079	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P4	**C8T28SOI_LL_-IVX3_P4**	**C8T28SOI_LL_-IVX2_P4**	**C8T28SOI_LL_-IVX3_P4**
A to Z ↓	0.0080	0.0075	7.9600	6.0679
A to Z ↑	0.0146	0.0131	11.9629	8.9721
	C8T28SOI_LL_-IVX5_P4	**C8T28SOI_LL_-IVX10_P4**	**C8T28SOI_LL_-IVX5_P4**	**C8T28SOI_LL_-IVX10_P4**
A to Z ↓	0.0068	0.0053	4.1173	1.9703
A to Z ↑	0.0115	0.0096	6.2072	2.9507
	C8T28SOI_LL_-IVX14_P4	**C8T28SOI_LL_-IVX19_P4**	**C8T28SOI_LL_-IVX14_P4**	**C8T28SOI_LL_-IVX19_P4**
A to Z ↓	0.0055	0.0059	1.3613	1.0377
A to Z ↑	0.0096	0.0099	1.9792	1.5111
	C8T28SOI_LL_-IVX29_P4	**C8T28SOI_LL_-IVX34_P4**	**C8T28SOI_LL_-IVX29_P4**	**C8T28SOI_LL_-IVX34_P4**
A to Z ↓	0.0058	0.0055	0.6954	0.5938
A to Z ↑	0.0095	0.0091	1.0039	0.8581
	C8T28SOI_LL_-IVX38_P4	**C8T28SOIDV_LL_-IVX11_P4**	**C8T28SOI_LL_-IVX38_P4**	**C8T28SOIDV_LL_-IVX11_P4**
A to Z ↓	0.0056	0.0052	0.5257	1.5285
A to Z ↑	0.0093	0.0112	0.7569	2.9965
	C8T28SOIDV_LL_-IVX23_P4	**C8T28SOIDV_LL_-IVX34_P4**	**C8T28SOIDV_LL_-IVX23_P4**	**C8T28SOIDV_LL_-IVX34_P4**
A to Z ↓	0.0043	0.0047	0.7452	0.5104
A to Z ↑	0.0099	0.0101	1.4607	0.9794
	C8T28SOIDV_LL_-IVX46_P4	**C8T28SOIDV_LL_-IVX68_P4**	**C8T28SOIDV_LL_-IVX46_P4**	**C8T28SOIDV_LL_-IVX68_P4**
A to Z ↓	0.0045	0.0046	0.3848	0.2614
A to Z ↑	0.0098	0.0096	0.7334	0.4926
	C8T28SOIDV_LL_-IVX91_P4		**C8T28SOIDV_LL_-IVX91_P4**	
A to Z ↓	0.0050		0.2018	
A to Z ↑	0.0099		0.3733	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_IVX2_P4	4.781e-06	1.000e-20
C8T28SOI_LL_IVX3_P4	6.708e-06	1.000e-20
C8T28SOI_LL_IVX5_P4	1.019e-05	1.000e-20
C8T28SOI_LL_IVX10_P4	2.138e-05	1.000e-20

C8T28SOI_LL_IVX14_P4	3.045e-05	1.000e-20
C8T28SOI_LL_IVX19_P4	3.935e-05	1.000e-20
C8T28SOI_LL_IVX29_P4	5.714e-05	1.000e-20
C8T28SOI_LL_IVX34_P4	6.604e-05	1.000e-20
C8T28SOI_LL_IVX38_P4	7.494e-05	1.000e-20
C8T28SOIDV_LL_IVX11_P4	2.520e-05	1.000e-20
C8T28SOIDV_LL_IVX23_P4	5.017e-05	1.000e-20
C8T28SOIDV_LL_IVX34_P4	7.182e-05	1.000e-20
C8T28SOIDV_LL_IVX46_P4	9.297e-05	1.000e-20
C8T28SOIDV_LL_IVX68_P4	1.352e-04	1.000e-20
C8T28SOIDV_LL_IVX91_P4	1.775e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P4	C8T28SOI_LL_IVX3_-P4	C8T28SOI_LL_IVX5_-P4	C8T28SOI_LL_-IVX10_P4
A to Z	2.803e-04	3.418e-04	4.318e-04	7.880e-04
	C8T28SOI_LL_-IVX14_P4	C8T28SOI_LL_-IVX19_P4	C8T28SOI_LL_-IVX29_P4	C8T28SOI_LL_-IVX34_P4
A to Z	1.211e-03	1.649e-03	2.384e-03	2.664e-03
	C8T28SOI_LL_-IVX38_P4	C8T28SOIDV_LL_-IVX11_P4	C8T28SOIDV_LL_-IVX23_P4	C8T28SOIDV_LL_-IVX34_P4
A to Z	3.095e-03	9.512e-04	1.728e-03	2.642e-03
	C8T28SOIDV_LL_-IVX46_P4	C8T28SOIDV_LL_-IVX68_P4	C8T28SOIDV_LL_-IVX91_P4	
A to Z	3.342e-03	4.960e-03	6.631e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

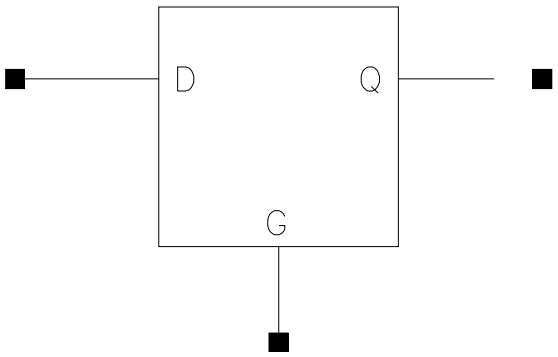
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P4	C8T28SOI_LL_IVX3_-P4	C8T28SOI_LL_IVX5_-P4	C8T28SOI_LL_-IVX10_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P4	C8T28SOI_LL_-IVX19_P4	C8T28SOI_LL_-IVX29_P4	C8T28SOI_LL_-IVX34_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P4	C8T28SOIDV_LL_-IVX11_P4	C8T28SOIDV_LL_-IVX23_P4	C8T28SOIDV_LL_-IVX34_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P4	C8T28SOIDV_LL_-IVX68_P4	C8T28SOIDV_LL_-IVX91_P4	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.360	1.0880
X9_P4	1.600	0.952	1.5232
X19_P4	1.600	1.224	1.9584
X28_P4	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4	X28_P4
D	0.0003	0.0006	0.0008	0.0014
G	0.0008	0.0008	0.0015	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D to Q ↓	0.0539	0.0510	4.1949	2.0886
D to Q ↑	0.0305	0.0362	5.9628	2.9174
G to Q ↓	0.0584	0.0542	4.1903	2.0852

G to Q ↑	0.0296	0.0336	5.9613	2.9185
	X19_P4	**X28_P4**	**X19_P4**	**X28_P4**
D to Q ↓	0.0410	0.0433	1.0025	0.6757
D to Q ↑	0.0305	0.0308	1.4668	0.9839
G to Q ↓	0.0468	0.0422	1.0007	0.6740
G to Q ↑	0.0281	0.0283	1.4687	0.9835

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P4	X9_P4	X19_P4	X28_P4
D ↓	hold_falling to G	-0.0094	-0.0088	0.0036	-0.0013
D ↑	hold_falling to G	0.0018	-0.0030	0.0019	0.0019
D ↓	setup_falling to G	0.0488	0.0467	0.0337	0.0365
D ↑	setup_falling to G	0.0334	0.0383	0.0355	0.0350
G ↑	min_pulse_width to G	0.0471	0.0424	0.0365	0.0399

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.673e-05	1.000e-20
X9_P4	4.304e-05	1.000e-20
X19_P4	7.367e-05	1.000e-20
X28_P4	9.954e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	7.084e-06	2.062e-05	2.279e-05	6.389e-05
G (output stable)	6.200e-04	7.295e-04	1.222e-03	1.152e-03
D to Q	2.317e-03	3.689e-03	5.476e-03	7.978e-03
G to Q	2.203e-03	3.495e-03	5.097e-03	6.962e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

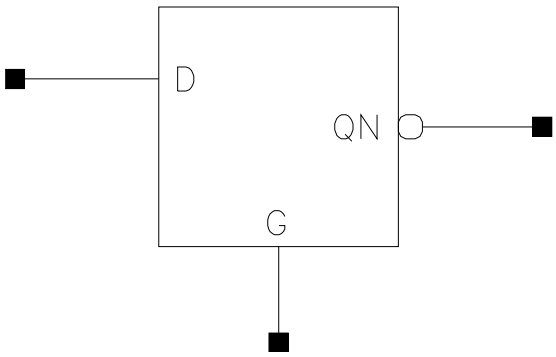
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P4
D	0.0004
G	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P4	X10_P4
D to QN ↓	0.0474	1.9440
D to QN ↑	0.0642	2.9070
G to QN ↓	0.0463	1.9457
G to QN ↑	0.0681	2.9056

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P4
D ↓	hold_falling to G	-0.0191
D ↑	hold_falling to G	-0.0030
D ↓	setup_falling to G	0.0467
D ↑	setup_falling to G	0.0335
G ↑	min_pulse_width to G	0.0424

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P4	3.992e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X10_P4
D (output stable)	6.999e-06
G (output stable)	6.696e-04
D to QN	3.033e-03
G to QN	2.896e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

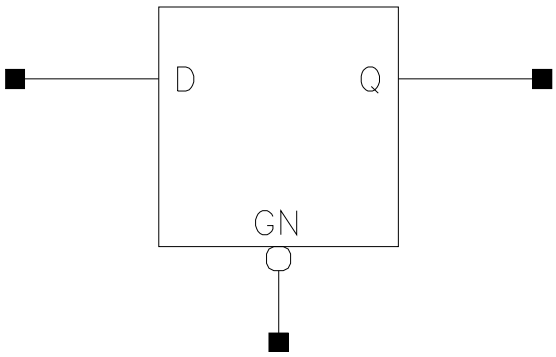
Pin Cycle (vdds)	X10_P4
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.360	1.0880
X9_P4	1.600	0.952	1.5232
X19_P4	1.600	1.224	1.9584
X28_P4	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4	X28_P4
D	0.0003	0.0006	0.0008	0.0012
GN	0.0008	0.0008	0.0012	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D to Q ↓	0.0544	0.0501	4.2016	2.0931
D to Q ↑	0.0307	0.0360	5.9563	2.9209
GN to Q ↓	0.0488	0.0473	4.2042	2.0920

GN to Q ↑	0.0543	0.0513	5.9504	2.9134
	X19_P4	**X28_P4**	**X19_P4**	**X28_P4**
D to Q ↓	0.0416	0.0414	1.0000	0.6733
D to Q ↑	0.0320	0.0314	1.4580	0.9741
GN to Q ↓	0.0367	0.0351	1.0009	0.6735
GN to Q ↑	0.0452	0.0449	1.4548	0.9723

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P4	X9_P4	X19_P4	X28_P4
D ↓	hold_rising to GN	-0.0145	-0.0096	-0.0052	-0.0052
D ↑	hold_rising to GN	0.0080	0.0032	0.0058	0.0052
D ↓	setup_rising to GN	0.0596	0.0520	0.0472	0.0445
D ↑	setup_rising to GN	0.0239	0.0314	0.0293	0.0265
GN ↓	min_pulse_width to GN	0.0631	0.0590	0.0517	0.0474

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.539e-05	1.000e-20
X9_P4	4.217e-05	1.000e-20
X19_P4	7.528e-05	1.000e-20
X28_P4	9.939e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	7.073e-06	1.172e-05	2.291e-05	5.395e-05
GN (output stable)	6.208e-04	7.279e-04	1.056e-03	1.162e-03
D to Q	2.318e-03	3.702e-03	5.661e-03	7.795e-03
GN to Q	3.470e-03	4.957e-03	7.233e-03	9.221e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

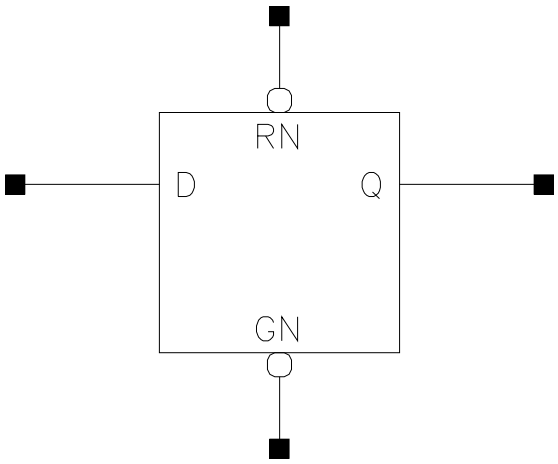
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.632	1.3056
X9_P4	1.600	1.224	1.9584
X19_P4	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4
D	0.0003	0.0005	0.0010
GN	0.0009	0.0009	0.0013
RN	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D to Q ↓	0.0561	0.0528	4.1301	2.0426

D to Q ↑	0.0515	0.0567	6.1796	3.0229
GN to Q ↓	0.0515	0.0488	4.1308	2.0418
GN to Q ↑	0.0717	0.0675	6.1752	3.0312
RN to Q ↓	0.0450	0.0568	3.9766	2.0423
RN to Q ↑	0.0564	0.0607	6.1778	3.0255
	X19_P4		**X19_P4**	
D to Q ↓	0.0434		1.0078	
D to Q ↑	0.0601		1.5264	
GN to Q ↓	0.0391		1.0088	
GN to Q ↑	0.0638		1.5293	
RN to Q ↓	0.0724		1.0790	
RN to Q ↑	0.0656		1.5254	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P4	X9_P4	X19_P4
D ↓	hold_rising to GN	-0.0145	-0.0149	-0.0046
D ↑	hold_rising to GN	-0.0094	-0.0142	-0.0186
D ↓	setup_rising to GN	0.0613	0.0570	0.0473
D ↑	setup_rising to GN	0.0508	0.0557	0.0658
GN ↓	min_pulse_width to GN	0.0698	0.0666	0.0668
RN ↓	min_pulse_width to RN	0.0566	0.0659	0.0828
RN ↑	recovery_rising to GN	0.0590	0.0660	0.0725
RN ↑	removal_rising to GN	-0.0347	-0.0418	-0.0462

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.520e-05	1.000e-20
X9_P4	4.012e-05	1.000e-20
X19_P4	6.930e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4
D (output stable)	3.823e-05	2.792e-05	4.195e-05
GN (output stable)	6.800e-04	6.984e-04	8.790e-04
RN (output stable)	2.698e-05	3.565e-05	4.877e-05
D to Q	2.957e-03	4.217e-03	6.482e-03
GN to Q	4.202e-03	5.425e-03	7.905e-03
RN to Q	2.196e-03	3.187e-03	5.226e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

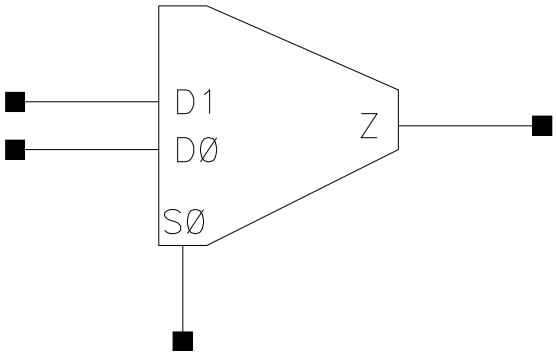
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.360	1.0880
X9_P4	0.800	1.496	1.1968
X14_P4	0.800	2.176	1.7408
X19_P4	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P4	X9_P4	X14_P4	X19_P4
D0	0.0005	0.0006	0.0008	0.0011
D1	0.0004	0.0006	0.0008	0.0011
S0	0.0009	0.0009	0.0011	0.0014

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D0 to Z ↓	0.0405	0.0373	4.1768	2.1066
D0 to Z ↑	0.0324	0.0309	6.1302	3.0922
D1 to Z ↓	0.0408	0.0361	4.1712	2.1026
D1 to Z ↑	0.0318	0.0291	6.1341	3.0905
S0 to Z ↓	0.0385	0.0325	4.1624	2.0987
S0 to Z ↑	0.0367	0.0326	6.1335	3.0897

	X14_P4	X19_P4	X14_P4	X19_P4
D0 to Z ↓	0.0406	0.0353	1.4506	1.0460
D0 to Z ↑	0.0330	0.0299	2.0910	1.5145
D1 to Z ↓	0.0410	0.0362	1.4497	1.0466
D1 to Z ↑	0.0313	0.0289	2.0869	1.5161
S0 to Z ↓	0.0390	0.0354	1.4452	1.0443
S0 to Z ↑	0.0384	0.0343	2.0887	1.5136

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	3.115e-05	1.000e-20
X9_P4	5.293e-05	1.000e-20
X14_P4	7.080e-05	1.000e-20
X19_P4	1.040e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X9_P4	X14_P4	X19_P4
D0 (output stable)	4.420e-04	8.206e-04	9.265e-04	1.163e-03
D1 (output stable)	4.199e-04	6.907e-04	9.689e-04	1.240e-03
S0 (output stable)	6.548e-04	5.845e-04	9.399e-04	1.115e-03
D0 to Z	1.717e-03	2.691e-03	4.292e-03	5.206e-03
D1 to Z	1.670e-03	2.508e-03	4.169e-03	5.155e-03
S0 to Z	2.103e-03	2.623e-03	4.710e-03	5.639e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

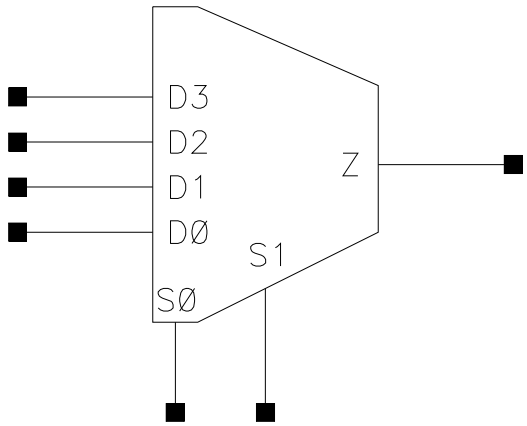
Pin Cycle (vdds)	X5_P4	X9_P4	X14_P4	X19_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.600	1.496	2.3936
X9_P4	1.600	1.768	2.8288
X13_P4	1.600	2.312	3.6992
X18_P4	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P4	X9_P4	X13_P4	X18_P4
D0	0.0004	0.0006	0.0008	0.0008
D1	0.0004	0.0005	0.0008	0.0008
D2	0.0003	0.0006	0.0008	0.0008
D3	0.0003	0.0005	0.0008	0.0008
S0	0.0011	0.0015	0.0019	0.0019
S1	0.0007	0.0008	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X9_P4**	**X4_P4**	**X9_P4**
D0 to Z ↓	0.0887	0.0721	4.5616	2.2337
D0 to Z ↑	0.0559	0.0492	6.3244	3.1190
D1 to Z ↓	0.0873	0.0716	4.5533	2.2354
D1 to Z ↑	0.0559	0.0488	6.3114	3.1192
D2 to Z ↓	0.0814	0.0725	4.5038	2.2406
D2 to Z ↑	0.0538	0.0487	6.2720	3.1172
D3 to Z ↓	0.0825	0.0715	4.5182	2.2393
D3 to Z ↑	0.0546	0.0487	6.2722	3.1162
S0 to Z ↓	0.0924	0.0800	4.5358	2.2368
S0 to Z ↑	0.0662	0.0615	6.3159	3.1248
S1 to Z ↓	0.0587	0.0539	4.5289	2.2358
S1 to Z ↑	0.0510	0.0475	6.3000	3.1178
	X13_P4	**X18_P4**	**X13_P4**	**X18_P4**
D0 to Z ↓	0.0689	0.0746	1.5530	1.1605
D0 to Z ↑	0.0443	0.0478	2.0868	1.5780
D1 to Z ↓	0.0695	0.0752	1.5559	1.1622
D1 to Z ↑	0.0455	0.0490	2.0868	1.5767
D2 to Z ↓	0.0639	0.0692	1.5367	1.1476
D2 to Z ↑	0.0439	0.0474	2.0799	1.5732
D3 to Z ↓	0.0637	0.0690	1.5355	1.1471
D3 to Z ↑	0.0442	0.0478	2.0800	1.5710
S0 to Z ↓	0.0741	0.0796	1.5452	1.1544
S0 to Z ↑	0.0557	0.0593	2.0860	1.5774
S1 to Z ↓	0.0510	0.0565	1.5445	1.1543
S1 to Z ↑	0.0429	0.0464	2.0825	1.5751

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	2.976e-05	1.000e-20
X9_P4	4.811e-05	1.000e-20
X13_P4	8.028e-05	1.000e-20
X18_P4	9.049e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X9_P4	X13_P4	X18_P4
D0 (output stable)	3.029e-05	3.464e-05	6.943e-05	6.873e-05
D1 (output stable)	4.264e-05	4.548e-05	6.502e-05	6.458e-05
D2 (output stable)	4.108e-05	4.598e-05	6.404e-05	6.393e-05
D3 (output stable)	3.282e-05	4.618e-05	5.946e-05	5.923e-05
S0 (output stable)	8.105e-04	9.815e-04	1.580e-03	1.581e-03
S1 (output stable)	8.906e-04	1.053e-03	1.660e-03	1.663e-03
D0 to Z	2.239e-03	3.270e-03	5.215e-03	6.435e-03
D1 to Z	2.209e-03	3.256e-03	5.281e-03	6.502e-03
D2 to Z	2.097e-03	3.258e-03	4.999e-03	6.176e-03
D3 to Z	2.125e-03	3.259e-03	5.021e-03	6.196e-03
S0 to Z	3.113e-03	4.419e-03	6.959e-03	8.172e-03
S1 to Z	2.521e-03	3.647e-03	5.712e-03	6.899e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

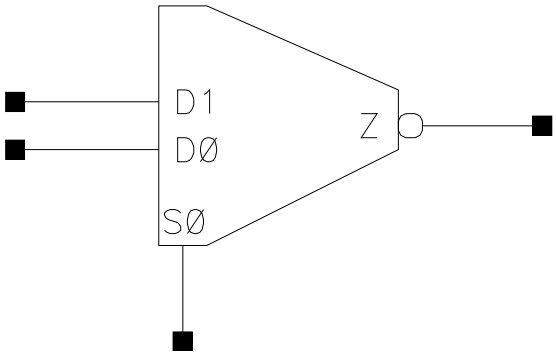
Pin Cycle (vdds)	X4_P4	X9_P4	X13_P4	X18_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P4	0.800	0.952	0.7616
X2_P4	0.800	0.952	0.7616
X6_P4	0.800	1.904	1.5232
X9_P4	0.800	2.448	1.9584
X12_P4	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P4	X2_P4	X6_P4	X9_P4
D0	0.0003	0.0004	0.0010	0.0014
D1	0.0003	0.0004	0.0009	0.0014
S0	0.0009	0.0012	0.0017	0.0024
	X12_P4			
D0	0.0019			
D1	0.0019			
S0	0.0027			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P4	X2_P4	X1_P4	X2_P4
D0 to Z ↓	0.0138	0.0129	12.0657	7.9627

D0 to Z ↑	0.0280	0.0211	26.4852	13.8767
D1 to Z ↓	0.0132	0.0122	11.9093	7.8394
D1 to Z ↑	0.0283	0.0219	26.5321	14.0440
S0 to Z ↓	0.0257	0.0175	11.9170	7.8863
S0 to Z ↑	0.0297	0.0188	26.4064	13.9380
	X6_P4	**X9_P4**	**X6_P4**	**X9_P4**
D0 to Z ↓	0.0146	0.0134	3.5160	2.3714
D0 to Z ↑	0.0222	0.0210	5.6995	3.9675
D1 to Z ↓	0.0142	0.0135	3.4667	2.3806
D1 to Z ↑	0.0236	0.0216	5.8772	3.8640
S0 to Z ↓	0.0204	0.0173	3.4826	2.3692
S0 to Z ↑	0.0216	0.0189	5.7756	3.9124
	X12_P4		**X12_P4**	
D0 to Z ↓	0.0140		1.8124	
D0 to Z ↑	0.0212		2.9898	
D1 to Z ↓	0.0134		1.8040	
D1 to Z ↑	0.0214		2.9099	
S0 to Z ↓	0.0188		1.8027	
S0 to Z ↑	0.0201		2.9466	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X1_P4	1.094e-05	1.000e-20
X2_P4	2.183e-05	1.000e-20
X6_P4	4.333e-05	1.000e-20
X9_P4	6.728e-05	1.000e-20
X12_P4	8.130e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X1_P4	X2_P4	X6_P4	X9_P4
D0 (output stable)	6.941e-06	1.654e-05	5.156e-05	7.339e-05
D1 (output stable)	6.622e-06	1.731e-05	5.577e-05	7.926e-05
S0 (output stable)	6.469e-04	7.282e-04	1.230e-03	1.896e-03
D0 to Z	5.401e-04	7.020e-04	1.863e-03	2.514e-03
D1 to Z	5.379e-04	6.968e-04	1.894e-03	2.571e-03
S0 to Z	1.123e-03	1.226e-03	2.577e-03	3.622e-03
	X12_P4			
D0 (output stable)	9.659e-05			
D1 (output stable)	9.929e-05			
S0 (output stable)	2.204e-03			
D0 to Z	3.404e-03			
D1 to Z	3.388e-03			
S0 to Z	4.564e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X1_P4	X2_P4	X6_P4	X9_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

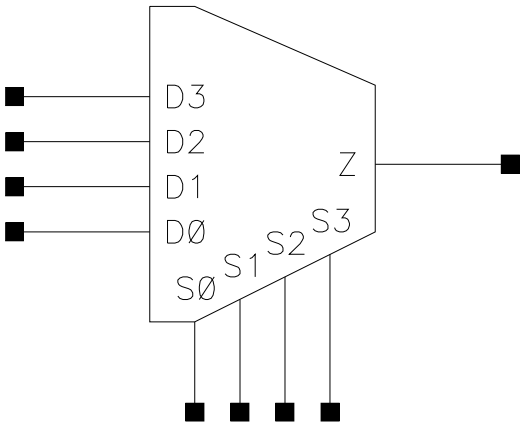
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P4			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.600	0.952	1.5232
X15_P4	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P4	X15_P4
D0	0.0005	0.0013
D1	0.0005	0.0010
D2	0.0005	0.0013
D3	0.0005	0.0010
S0	0.0005	0.0011
S1	0.0005	0.0013
S2	0.0005	0.0011
S3	0.0005	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X15_P4	X4_P4	X15_P4
D0 to Z ↓	0.0450	0.0473	6.8214	1.7935
D0 to Z ↑	0.0379	0.0354	5.7819	1.4595
D1 to Z ↓	0.0410	0.0421	6.8190	1.7921
D1 to Z ↑	0.0329	0.0308	5.7507	1.4515
D2 to Z ↓	0.0440	0.0458	6.8284	1.7949
D2 to Z ↑	0.0371	0.0337	5.7985	1.4669
D3 to Z ↓	0.0395	0.0409	6.8244	1.7926
D3 to Z ↑	0.0319	0.0294	5.7728	1.4573
S0 to Z ↓	0.0431	0.0433	6.8210	1.7911
S0 to Z ↑	0.0401	0.0357	5.7816	1.4597
S1 to Z ↓	0.0388	0.0389	6.8183	1.7900
S1 to Z ↑	0.0346	0.0314	5.7491	1.4518
S2 to Z ↓	0.0427	0.0422	6.8276	1.7926
S2 to Z ↑	0.0393	0.0342	5.8005	1.4660
S3 to Z ↓	0.0388	0.0375	6.8239	1.7901
S3 to Z ↑	0.0344	0.0297	5.7693	1.4580

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	3.658e-05	1.000e-20
X15_P4	1.078e-04	1.000e-20

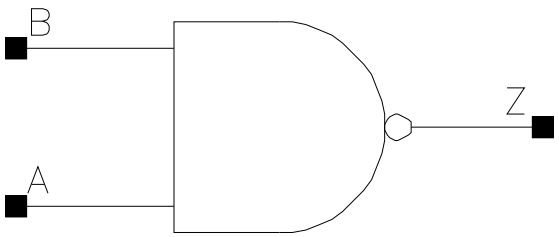
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X15_P4
D0 (output stable)	2.954e-04	8.222e-04
D1 (output stable)	2.476e-04	6.772e-04
D2 (output stable)	2.919e-04	8.037e-04
D3 (output stable)	2.459e-04	6.615e-04
S0 (output stable)	2.822e-04	7.799e-04
S1 (output stable)	2.385e-04	6.579e-04
S2 (output stable)	2.857e-04	7.732e-04
S3 (output stable)	2.406e-04	6.472e-04
D0 to Z	2.268e-03	6.420e-03
D1 to Z	1.939e-03	5.503e-03
D2 to Z	2.096e-03	5.780e-03
D3 to Z	1.775e-03	4.883e-03
S0 to Z	2.192e-03	6.005e-03
S1 to Z	1.874e-03	5.156e-03
S2 to Z	2.041e-03	5.404e-03
S3 to Z	1.728e-03	4.513e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X4_P4	X15_P4
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description	Logical Symbol
2 input NAND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P4	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P4	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P4	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P4	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P4	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P4	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P4	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P4	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P4	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P4	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P4	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P4	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P4	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P4	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P4	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P4	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P4	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P4	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P4	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P4	C8T28SOI_LL_-NAND2X4_P4	C8T28SOI_LL_-NAND2X8_P4	C8T28SOI_LL_-NAND2X12_P4
A	0.0003	0.0005	0.0009	0.0014
B	0.0003	0.0005	0.0009	0.0013
	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X24_P4	C8T28SOI_-LLBR0P8_-NAND2X4_P4
A	0.0018	0.0023	0.0006	0.0006
B	0.0017	0.0021	0.0006	0.0005
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	C8T28SOI_-LLBR0P8_-NAND2X12_P4	C8T28SOI_-LLBR0P8_-NAND2X16_P4	C8T28SOI_LLS_-NAND2X8_P4
A	0.0010	0.0014	0.0019	0.0009
B	0.0008	0.0013	0.0016	0.0008
	C8T28SOI_LLS_-NAND2X15_P4	C8T28SOI_LLS_-NAND2X23_P4	C8T28SOI_LLS_-NAND2X31_P4	C8T28SOIDV_LL_-NAND2X9_P4
A	0.0019	0.0028	0.0038	0.0010
B	0.0017	0.0026	0.0034	0.0010
	C8T28SOIDV_LL_-NAND2X18_P4	C8T28SOIDV_LL_-NAND2X27_P4	C8T28SOIDV_LL_-NAND2X36_P4	
A	0.0020	0.0029	0.0039	
B	0.0018	0.0027	0.0037	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-NAND2X2_P4	**C8T28SOI_LL_-NAND2X4_P4**	**C8T28SOI_LL_-NAND2X2_P4**	**C8T28SOI_LL_-NAND2X4_P4**
A to Z ↓	0.0106	0.0092	13.0940	6.9291
A to Z ↑	0.0164	0.0135	11.9023	6.1754
B to Z ↓	0.0124	0.0102	13.1749	6.9773
B to Z ↑	0.0155	0.0122	11.9466	6.2514
	C8T28SOI_LL_-NAND2X8_P4	**C8T28SOI_LL_-NAND2X12_P4**	**C8T28SOI_LL_-NAND2X8_P4**	**C8T28SOI_LL_-NAND2X12_P4**
A to Z ↓	0.0102	0.0098	3.4751	2.3738
A to Z ↑	0.0136	0.0133	2.9462	2.0016
B to Z ↓	0.0093	0.0098	3.5024	2.3918
B to Z ↑	0.0107	0.0110	2.9634	2.0234

	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4
A to Z ↓	0.0100	0.0099	1.7993	1.4511
A to Z ↑	0.0132	0.0132	1.5052	1.2168
B to Z ↓	0.0094	0.0099	1.8131	1.4629
B to Z ↑	0.0105	0.0109	1.5199	1.2295
	C8T28SOI_LL_-NAND2X24_P4	**C8T28SOI_-LLBR0P8_-NAND2X4_P4**	**C8T28SOI_LL_-NAND2X24_P4**	**C8T28SOI_-LLBR0P8_-NAND2X4_P4**
A to Z ↓	0.0377	0.0074	0.8104	4.8314
A to Z ↑	0.0385	0.0174	1.1957	7.8992
B to Z ↓	0.0389	0.0078	0.8105	4.8855
B to Z ↑	0.0369	0.0151	1.1971	7.9061
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	**C8T28SOI_-LLBR0P8_-NAND2X12_P4**	**C8T28SOI_-LLBR0P8_-NAND2X8_P4**	**C8T28SOI_-LLBR0P8_-NAND2X12_P4**
A to Z ↓	0.0082	0.0081	2.6280	1.7941
A to Z ↑	0.0174	0.0174	3.9700	2.6813
B to Z ↓	0.0066	0.0074	2.6619	1.8164
B to Z ↑	0.0131	0.0137	3.9941	2.6962
	C8T28SOI_-LLBR0P8_-NAND2X16_P4	**C8T28SOI_LLS_-NAND2X8_P4**	**C8T28SOI_-LLBR0P8_-NAND2X16_P4**	**C8T28SOI_LLS_-NAND2X8_P4**
A to Z ↓	0.0078	0.0102	1.3676	3.4703
A to Z ↑	0.0168	0.0137	2.0076	2.9754
B to Z ↓	0.0064	0.0094	1.3859	3.4958
B to Z ↑	0.0125	0.0108	2.0255	3.0058
	C8T28SOI_LLS_-NAND2X15_P4	**C8T28SOI_LLS_-NAND2X23_P4**	**C8T28SOI_LLS_-NAND2X15_P4**	**C8T28SOI_LLS_-NAND2X23_P4**
A to Z ↓	0.0101	0.0101	1.7955	1.2111
A to Z ↑	0.0133	0.0132	1.4859	0.9920
B to Z ↓	0.0095	0.0097	1.8098	1.2208
B to Z ↑	0.0105	0.0106	1.4951	0.9984
	C8T28SOI_LLS_-NAND2X31_P4	**C8T28SOIDV_LL_-NAND2X9_P4**	**C8T28SOI_LLS_-NAND2X31_P4**	**C8T28SOIDV_LL_-NAND2X9_P4**
A to Z ↓	0.0101	0.0085	0.9154	2.6256
A to Z ↑	0.0132	0.0141	0.7466	2.8867
B to Z ↓	0.0099	0.0089	0.9232	2.6486
B to Z ↑	0.0107	0.0123	0.7512	2.9309
	C8T28SOIDV_LL_-NAND2X18_P4	**C8T28SOIDV_LL_-NAND2X27_P4**	**C8T28SOIDV_LL_-NAND2X18_P4**	**C8T28SOIDV_LL_-NAND2X27_P4**
A to Z ↓	0.0092	0.0091	1.3281	0.9037
A to Z ↑	0.0145	0.0145	1.4500	0.9770
B to Z ↓	0.0081	0.0090	1.3408	0.9117
B to Z ↑	0.0113	0.0120	1.4589	0.9826
	C8T28SOIDV_LL_-NAND2X36_P4		**C8T28SOIDV_LL_-NAND2X36_P4**	
A to Z ↓	0.0093		0.6813	
A to Z ↑	0.0144		0.7318	
B to Z ↓	0.0083		0.6879	
B to Z ↑	0.0113		0.7368	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P4	4.790e-06	1.000e-20
C8T28SOI_LL_NAND2X4_P4	1.061e-05	1.000e-20
C8T28SOI_LL_NAND2X8_P4	2.112e-05	1.000e-20
C8T28SOI_LL_NAND2X12_P4	3.038e-05	1.000e-20
C8T28SOI_LL_NAND2X15_P4	3.966e-05	1.000e-20
C8T28SOI_LL_NAND2X19_P4	4.896e-05	1.000e-20
C8T28SOI_LL_NAND2X24_P4	7.512e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P4	1.140e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P4	2.043e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_P4	2.910e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_P4	3.780e-05	1.000e-20
C8T28SOI_LLS_NAND2X8_P4	2.112e-05	1.000e-20
C8T28SOI_LLS_NAND2X15_P4	3.966e-05	1.000e-20
C8T28SOI_LLS_NAND2X23_P4	5.825e-05	1.000e-20
C8T28SOI_LLS_NAND2X31_P4	7.684e-05	1.000e-20
C8T28SOIDV_LL_NAND2X9_P4	2.611e-05	1.000e-20
C8T28SOIDV_LL_NAND2X18_P4	4.970e-05	1.000e-20
C8T28SOIDV_LL_NAND2X27_P4	7.192e-05	1.000e-20
C8T28SOIDV_LL_NAND2X36_P4	9.419e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P4	C8T28SOI_LL_-NAND2X4_P4	C8T28SOI_LL_-NAND2X8_P4	C8T28SOI_LL_-NAND2X12_P4
A (output stable)	5.030e-06	9.429e-06	4.767e-05	5.828e-05
B (output stable)	9.879e-06	1.878e-05	1.280e-04	1.322e-04
A to Z	3.516e-04	5.453e-04	1.205e-03	1.726e-03
B to Z	3.137e-04	4.675e-04	8.900e-04	1.373e-03
	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X24_P4	C8T28SOI_-LLBR0P8_-NAND2X4_P4
A (output stable)	8.820e-05	9.639e-05	1.157e-05	1.411e-05
B (output stable)	2.206e-04	2.067e-04	2.161e-05	2.627e-05
A to Z	2.317e-03	2.846e-03	5.362e-03	6.116e-04
B to Z	1.751e-03	2.262e-03	5.283e-03	4.976e-04
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	C8T28SOI_-LLBR0P8_-NAND2X12_P4	C8T28SOI_-LLBR0P8_-NAND2X16_P4	C8T28SOI_LLS_-NAND2X8_P4
A (output stable)	5.741e-05	6.838e-05	1.098e-04	4.835e-05
B (output stable)	1.543e-04	1.581e-04	2.647e-04	1.332e-04
A to Z	1.250e-03	1.851e-03	2.346e-03	1.212e-03
B to Z	8.363e-04	1.356e-03	1.584e-03	8.979e-04
	C8T28SOI_LLS_-NAND2X15_P4	C8T28SOI_LLS_-NAND2X23_P4	C8T28SOI_LLS_-NAND2X31_P4	C8T28SOIDV_LL_-NAND2X9_P4
A (output stable)	9.238e-05	1.338e-04	1.749e-04	2.581e-05
B (output stable)	2.283e-04	3.062e-04	3.885e-04	4.860e-05
A to Z	2.344e-03	3.488e-03	4.623e-03	1.291e-03
B to Z	1.772e-03	2.676e-03	3.576e-03	1.083e-03
	C8T28SOIDV_LL_-NAND2X18_P4	C8T28SOIDV_LL_-NAND2X27_P4	C8T28SOIDV_LL_-NAND2X36_P4	
A (output stable)	1.027e-04	1.219e-04	2.082e-04	
B (output stable)	3.079e-04	2.637e-04	5.792e-04	
A to Z	2.691e-03	3.974e-03	5.302e-03	

B to Z	1.975e-03	3.182e-03	3.917e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

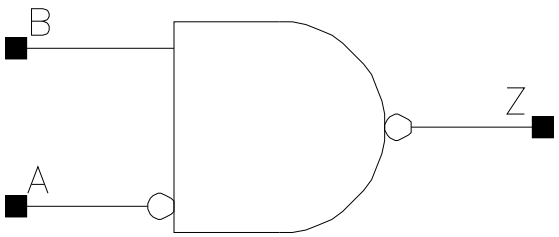
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P4	C8T28SOI_LL_-NAND2X4_P4	C8T28SOI_LL_-NAND2X8_P4	C8T28SOI_LL_-NAND2X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X24_P4	C8T28SOI_-LLBR0P8_-NAND2X4_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	C8T28SOI_-LLBR0P8_-NAND2X12_P4	C8T28SOI_-LLBR0P8_-NAND2X16_P4	C8T28SOI_LLS_-NAND2X8_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P4	C8T28SOI_LLS_-NAND2X23_P4	C8T28SOI_LLS_-NAND2X31_P4	C8T28SOIDV_LL_-NAND2X9_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P4	C8T28SOIDV_LL_-NAND2X27_P4	C8T28SOIDV_LL_-NAND2X36_P4	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.544	0.4352
X4_P4	0.800	0.680	0.5440
X9_P4	1.600	0.544	0.8704
X13_P4	1.600	0.816	1.3056
X17_P4	1.600	0.816	1.3056
X23_P4	0.800	2.312	1.8496
X27_P4	1.600	1.088	1.7408
X31_P4	0.800	2.992	2.3936
X36_P4	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P4	X4_P4	X9_P4	X13_P4
A	0.0005	0.0005	0.0008	0.0008
B	0.0003	0.0005	0.0009	0.0015
	X17_P4	X23_P4	X27_P4	X31_P4
A	0.0008	0.0017	0.0014	0.0023
B	0.0018	0.0025	0.0028	0.0033
	X36_P4			
A	0.0013			
B	0.0036			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X4_P4**	**X2_P4**	**X4_P4**
A to Z ↓	0.0287	0.0294	13.1533	6.9883
A to Z ↑	0.0221	0.0222	11.6873	6.0345
B to Z ↓	0.0128	0.0103	13.3579	7.0988
B to Z ↑	0.0156	0.0121	11.9499	6.2480
	X9_P4	**X13_P4**	**X9_P4**	**X13_P4**
A to Z ↓	0.0285	0.0345	2.6691	1.7099
A to Z ↑	0.0212	0.0257	2.8533	1.9283
B to Z ↓	0.0092	0.0089	2.7245	1.7441
B to Z ↑	0.0123	0.0127	2.9417	2.0103
	X17_P4	**X23_P4**	**X17_P4**	**X23_P4**
A to Z ↓	0.0374	0.0273	1.3374	1.2004
A to Z ↑	0.0266	0.0217	1.4639	0.9899
B to Z ↓	0.0087	0.0095	1.3606	1.2230
B to Z ↑	0.0120	0.0106	1.5299	1.0208
	X27_P4	**X31_P4**	**X27_P4**	**X31_P4**
A to Z ↓	0.0318	0.0273	0.8988	0.9074
A to Z ↑	0.0237	0.0216	0.9675	0.7273
B to Z ↓	0.0085	0.0097	0.9169	0.9239
B to Z ↑	0.0115	0.0106	0.9864	0.7678
	X36_P4		**X36_P4**	
A to Z ↓	0.0362		0.6796	
A to Z ↑	0.0268		0.7266	
B to Z ↓	0.0083		0.6918	
B to Z ↑	0.0112		0.7406	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P4	8.714e-06	1.000e-20
X4_P4	1.516e-05	1.000e-20
X9_P4	3.812e-05	1.000e-20
X13_P4	4.622e-05	1.000e-20
X17_P4	5.948e-05	1.000e-20
X23_P4	8.806e-05	1.000e-20
X27_P4	9.504e-05	1.000e-20
X31_P4	1.156e-04	1.000e-20
X36_P4	1.178e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P4	X4_P4	X9_P4	X13_P4
A (output stable)	5.143e-04	6.402e-04	1.229e-03	1.763e-03
B (output stable)	9.874e-06	1.905e-05	5.107e-05	1.410e-04
A to Z	8.673e-04	1.174e-03	2.518e-03	3.965e-03
B to Z	3.158e-04	4.627e-04	1.095e-03	1.656e-03
	X17_P4	X23_P4	X27_P4	X31_P4
A (output stable)	1.973e-03	3.145e-03	3.141e-03	4.196e-03
B (output stable)	1.691e-04	2.776e-04	2.643e-04	3.681e-04
A to Z	4.760e-03	6.680e-03	6.987e-03	8.926e-03
B to Z	2.060e-03	2.669e-03	3.019e-03	3.543e-03
	X36_P4			
A (output stable)	4.023e-03			

B (output stable)	4.358e-04			
A to Z	9.245e-03			
B to Z	3.875e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

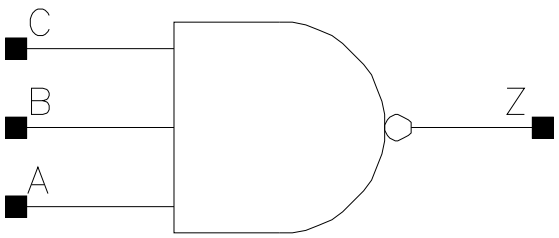
Pin Cycle (vdds)	X2_P4	X4_P4	X9_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P4	X23_P4	X27_P4	X31_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P4	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P4	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P4	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P4	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P4	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P4	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P4	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P4	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P4	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P4	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P4	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P4	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P4	C8T28SOI_LL_-NAND3X7_P4	C8T28SOI_LL_-NAND3X10_P4	C8T28SOI_LL_-NAND3X14_P4
A	0.0005	0.0009	0.0014	0.0018
B	0.0005	0.0009	0.0013	0.0017
C	0.0005	0.0008	0.0012	0.0017
	C8T28SOI_LL_-NAND3X20_P4	C8T28SOI_LL_-NAND3X27_P4	C8T28SOI_-LLBR0P6_-NAND3X3_P4	C8T28SOI_-LLBR0P6_-NAND3X7_P4
A	0.0027	0.0037	0.0006	0.0010
B	0.0026	0.0035	0.0005	0.0009
C	0.0024	0.0033	0.0005	0.0008
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	C8T28SOI_-LLBR0P6_-NAND3X14_P4	C8T28SOI_-LLBR0P6_-NAND3X20_P4	C8T28SOI_-LLBR0P6_-NAND3X27_P4
A	0.0014	0.0019	0.0027	0.0037
B	0.0013	0.0017	0.0025	0.0034
C	0.0013	0.0017	0.0025	0.0033

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND3X3_P4	**C8T28SOI_LL_-NAND3X7_P4**	**C8T28SOI_LL_-NAND3X3_P4**	**C8T28SOI_LL_-NAND3X7_P4**
A to Z ↓	0.0140	0.0158	10.1087	5.0142
A to Z ↑	0.0167	0.0171	6.2081	3.0299
B to Z ↓	0.0148	0.0155	10.1320	5.0281
B to Z ↑	0.0155	0.0157	6.2342	3.0327
C to Z ↓	0.0153	0.0142	10.1597	5.0400
C to Z ↑	0.0142	0.0132	6.2949	2.9578
	C8T28SOI_LL_-NAND3X10_P4	**C8T28SOI_LL_-NAND3X14_P4**	**C8T28SOI_LL_-NAND3X10_P4**	**C8T28SOI_LL_-NAND3X14_P4**
A to Z ↓	0.0149	0.0154	3.4578	2.6054
A to Z ↑	0.0161	0.0165	1.9683	1.5256
B to Z ↓	0.0152	0.0150	3.4677	2.6127
B to Z ↑	0.0149	0.0150	2.0174	1.5248
C to Z ↓	0.0142	0.0141	3.4777	2.6196
C to Z ↑	0.0127	0.0127	2.0282	1.5140
	C8T28SOI_LL_-NAND3X20_P4	**C8T28SOI_LL_-NAND3X27_P4**	**C8T28SOI_LL_-NAND3X20_P4**	**C8T28SOI_LL_-NAND3X27_P4**
A to Z ↓	0.0149	0.0150	1.7694	1.3438
A to Z ↑	0.0159	0.0160	0.9914	0.7475
B to Z ↓	0.0152	0.0151	1.7755	1.3474
B to Z ↑	0.0146	0.0145	0.9912	0.7458
C to Z ↓	0.0140	0.0142	1.7805	1.3515
C to Z ↑	0.0123	0.0124	1.0129	0.7623
	C8T28SOI_-LLBR0P6_-NAND3X3_P4	**C8T28SOI_-LLBR0P6_-NAND3X7_P4**	**C8T28SOI_-LLBR0P6_-NAND3X3_P4**	**C8T28SOI_-LLBR0P6_-NAND3X7_P4**
A to Z ↓	0.0099	0.0124	6.2512	3.4311
A to Z ↑	0.0235	0.0253	9.3825	4.7632
B to Z ↓	0.0099	0.0115	6.2991	3.4520
B to Z ↑	0.0208	0.0221	9.3423	4.7737

C to Z ↓	0.0095	0.0093	6.3515	3.4776
C to Z ↑	0.0178	0.0174	9.3961	4.7394
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	**C8T28SOI_-LLBR0P6_-NAND3X14_P4**	**C8T28SOI_-LLBR0P6_-NAND3X10_P4**	**C8T28SOI_-LLBR0P6_-NAND3X14_P4**
A to Z ↓	0.0111	0.0119	2.3057	1.7467
A to Z ↑	0.0237	0.0244	3.1810	2.4065
B to Z ↓	0.0105	0.0106	2.3231	1.7588
B to Z ↑	0.0204	0.0209	3.1920	2.4107
C to Z ↓	0.0089	0.0085	2.3424	1.7743
C to Z ↑	0.0164	0.0162	3.2110	2.4076
	C8T28SOI_-LLBR0P6_-NAND3X20_P4	**C8T28SOI_-LLBR0P6_-NAND3X27_P4**	**C8T28SOI_-LLBR0P6_-NAND3X20_P4**	**C8T28SOI_-LLBR0P6_-NAND3X27_P4**
A to Z ↓	0.0113	0.0114	1.1811	0.9025
A to Z ↑	0.0237	0.0237	1.6031	1.2081
B to Z ↓	0.0105	0.0104	1.1898	0.9091
B to Z ↑	0.0205	0.0203	1.6055	1.2084
C to Z ↓	0.0084	0.0085	1.2003	0.9168
C to Z ↑	0.0157	0.0157	1.6134	1.2141

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P4	8.344e-06	1.000e-20
C8T28SOI_LL_NAND3X7_P4	1.739e-05	1.000e-20
C8T28SOI_LL_NAND3X10_P4	2.399e-05	1.000e-20
C8T28SOI_LL_NAND3X14_P4	3.232e-05	1.000e-20
C8T28SOI_LL_NAND3X20_P4	4.725e-05	1.000e-20
C8T28SOI_LL_NAND3X27_P4	6.215e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P4	9.198e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P4	1.775e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_P4	2.368e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_P4	3.225e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_P4	4.673e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_P4	6.117e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P4	C8T28SOI_LL_-NAND3X7_P4	C8T28SOI_LL_-NAND3X10_P4	C8T28SOI_LL_-NAND3X14_P4
A (output stable)	1.112e-05	4.735e-05	6.041e-05	8.885e-05
B (output stable)	1.391e-05	6.103e-05	8.000e-05	1.085e-04
C (output stable)	3.298e-05	1.595e-04	1.877e-04	2.869e-04
A to Z	7.728e-04	1.755e-03	2.423e-03	3.299e-03
B to Z	6.846e-04	1.477e-03	2.034e-03	2.753e-03
C to Z	6.054e-04	1.194e-03	1.670e-03	2.237e-03
	C8T28SOI_LL_-NAND3X20_P4	C8T28SOI_LL_-NAND3X27_P4	C8T28SOI_-LLBR0P6_-NAND3X3_P4	C8T28SOI_-LLBR0P6_-NAND3X7_P4
A (output stable)	1.195e-04	1.622e-04	1.842e-05	6.372e-05
B (output stable)	1.574e-04	2.045e-04	2.113e-05	7.813e-05
C (output stable)	4.217e-04	5.442e-04	5.284e-05	2.061e-04

A to Z	4.786e-03	6.356e-03	8.303e-04	1.919e-03
B to Z	4.026e-03	5.320e-03	6.843e-04	1.503e-03
C to Z	3.203e-03	4.280e-03	5.415e-04	1.076e-03
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	C8T28SOI_-LLBR0P6_-NAND3X14_P4	C8T28SOI_-LLBR0P6_-NAND3X20_P4	C8T28SOI_-LLBR0P6_-NAND3X27_P4
A (output stable)	8.070e-05	1.303e-04	1.675e-04	2.288e-04
B (output stable)	9.937e-05	1.555e-04	2.111e-04	2.744e-04
C (output stable)	2.536e-04	3.903e-04	5.618e-04	7.223e-04
A to Z	2.571e-03	3.589e-03	5.145e-03	6.818e-03
B to Z	1.967e-03	2.721e-03	3.926e-03	5.155e-03
C to Z	1.438e-03	1.888e-03	2.707e-03	3.589e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

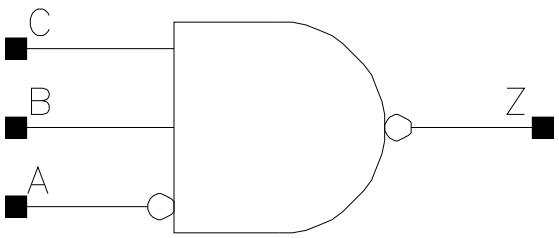
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P4	C8T28SOI_LL_-NAND3X7_P4	C8T28SOI_LL_-NAND3X10_P4	C8T28SOI_LL_-NAND3X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P4	C8T28SOI_LL_-NAND3X27_P4	C8T28SOI_-LLBR0P6_-NAND3X3_P4	C8T28SOI_-LLBR0P6_-NAND3X7_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	C8T28SOI_-LLBR0P6_-NAND3X14_P4	C8T28SOI_-LLBR0P6_-NAND3X20_P4	C8T28SOI_-LLBR0P6_-NAND3X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X7_P4	0.800	1.360	1.0880
X10_P4	0.800	1.632	1.3056
X14_P4	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X10_P4	X14_P4
A	0.0006	0.0009	0.0007	0.0007
B	0.0005	0.0009	0.0013	0.0017
C	0.0005	0.0009	0.0012	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0357	0.0342	10.1208	5.0430
A to Z ↑	0.0253	0.0252	6.0321	2.9066
B to Z ↓	0.0143	0.0152	10.1946	5.0781
B to Z ↑	0.0150	0.0151	6.2413	2.9665
C to Z ↓	0.0148	0.0137	10.2253	5.0908
C to Z ↑	0.0137	0.0125	6.2982	2.9625
	X10_P4	**X14_P4**	**X10_P4**	**X14_P4**
A to Z ↓	0.0376	0.0406	3.4490	2.6169

A to Z ↑	0.0279	0.0305	1.9787	1.4815
B to Z ↓	0.0151	0.0146	3.4703	2.6311
B to Z ↑	0.0148	0.0145	2.0191	1.5120
C to Z ↓	0.0141	0.0136	3.4786	2.6385
C to Z ↑	0.0127	0.0121	2.0303	1.5154

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.238e-05	1.000e-20
X7_P4	2.751e-05	1.000e-20
X10_P4	3.444e-05	1.000e-20
X14_P4	4.281e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	6.500e-04	1.198e-03	1.511e-03	1.821e-03
B (output stable)	1.423e-05	5.083e-05	8.159e-05	9.857e-05
C (output stable)	3.311e-05	1.670e-04	1.972e-04	2.767e-04
A to Z	1.389e-03	2.937e-03	4.080e-03	5.219e-03
B to Z	6.493e-04	1.407e-03	2.032e-03	2.640e-03
C to Z	5.681e-04	1.108e-03	1.658e-03	2.114e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

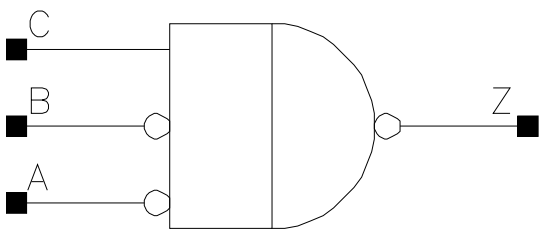
Pin Cycle (vdds)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	0.816	0.6528
X8_P4	0.800	1.088	0.8704
X12_P4	0.800	1.632	1.3056
X15_P4	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X12_P4	X15_P4
A	0.0006	0.0006	0.0011	0.0010
B	0.0007	0.0006	0.0011	0.0011
C	0.0005	0.0009	0.0013	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0315	0.0385	6.5263	3.4606
A to Z ↑	0.0211	0.0244	5.7700	2.8839
B to Z ↓	0.0322	0.0391	6.5234	3.4619
B to Z ↑	0.0200	0.0232	5.7680	2.8814
C to Z ↓	0.0105	0.0095	6.6169	3.4984
C to Z ↑	0.0123	0.0109	5.8122	2.9842
	X12_P4	**X15_P4**	**X12_P4**	**X15_P4**
A to Z ↓	0.0352	0.0385	2.3549	1.7943
A to Z ↑	0.0226	0.0267	1.9240	1.4514
B to Z ↓	0.0335	0.0370	2.3552	1.7931

B to Z ↑	0.0205	0.0245	1.9216	1.4490
C to Z ↓	0.0104	0.0095	2.3864	1.8167
C to Z ↑	0.0115	0.0105	2.0204	1.4925

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	2.085e-05	1.000e-20
X8_P4	2.806e-05	1.000e-20
X12_P4	4.442e-05	1.000e-20
X15_P4	4.969e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	3.533e-04	4.729e-04	8.043e-04	9.163e-04
B (output stable)	3.234e-04	4.413e-04	7.261e-04	8.380e-04
C (output stable)	2.092e-05	1.281e-04	1.358e-04	2.127e-04
A to Z	1.632e-03	2.679e-03	4.227e-03	5.133e-03
B to Z	1.516e-03	2.559e-03	3.793e-03	4.705e-03
C to Z	5.232e-04	9.147e-04	1.470e-03	1.781e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

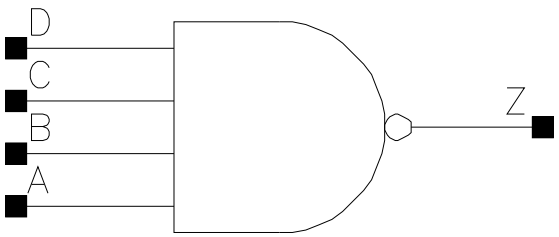
Pin Cycle (vdds)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.224	0.9792
X10_P4	0.800	1.360	1.0880
X14_P4	0.800	1.904	1.5232
X18_P4	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X18_P4
A	0.0004	0.0004	0.0005	0.0005
B	0.0004	0.0005	0.0005	0.0007
C	0.0004	0.0004	0.0005	0.0006
D	0.0004	0.0004	0.0005	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0529	0.0485	3.9040	1.9704
A to Z ↑	0.0425	0.0429	5.8135	2.9412
B to Z ↓	0.0550	0.0509	3.9045	1.9702
B to Z ↑	0.0415	0.0425	5.8183	2.9425
C to Z ↓	0.0553	0.0502	3.9053	1.9689
C to Z ↑	0.0448	0.0458	5.8078	2.9423

D to Z ↓	0.0580	0.0528	3.9034	1.9702
D to Z ↑	0.0446	0.0456	5.8114	2.9383
	X14_P4	**X18_P4**	**X14_P4**	**X18_P4**
A to Z ↓	0.0519	0.0478	1.3537	1.0972
A to Z ↑	0.0424	0.0413	2.0066	1.5889
B to Z ↓	0.0542	0.0498	1.3527	1.0974
B to Z ↑	0.0414	0.0406	2.0069	1.5874
C to Z ↓	0.0502	0.0439	1.3524	1.0979
C to Z ↑	0.0431	0.0406	2.0020	1.5837
D to Z ↓	0.0525	0.0456	1.3516	1.0980
D to Z ↑	0.0426	0.0393	2.0031	1.5851

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.208e-05	1.000e-20
X10_P4	3.492e-05	1.000e-20
X14_P4	4.984e-05	1.000e-20
X18_P4	6.607e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	2.569e-04	3.080e-04	4.524e-04	4.988e-04
B (output stable)	2.442e-04	2.947e-04	4.323e-04	4.790e-04
C (output stable)	2.822e-04	3.120e-04	4.700e-04	4.752e-04
D (output stable)	2.689e-04	2.986e-04	4.476e-04	4.486e-04
A to Z	1.995e-03	2.829e-03	4.392e-03	5.100e-03
B to Z	1.957e-03	2.791e-03	4.330e-03	5.041e-03
C to Z	2.121e-03	2.908e-03	4.178e-03	4.740e-03
D to Z	2.098e-03	2.876e-03	4.128e-03	4.668e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

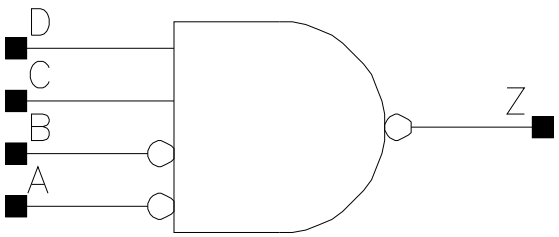
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.952	0.7616
X7_P4	0.800	1.360	1.0880
X10_P4	0.800	2.040	1.6320
X14_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P4	X7_P4	X10_P4	X14_P4
A	0.0006	0.0006	0.0011	0.0010
B	0.0006	0.0006	0.0012	0.0011
C	0.0006	0.0009	0.0013	0.0017
D	0.0005	0.0009	0.0012	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X7_P4	X3_P4	X7_P4
A to Z ↓	0.0363	0.0423	9.5973	5.0506
A to Z ↑	0.0231	0.0264	5.8071	2.9182
B to Z ↓	0.0364	0.0426	9.5977	5.0496
B to Z ↑	0.0217	0.0249	5.8022	2.9155
C to Z ↓	0.0148	0.0150	9.6742	5.0754
C to Z ↑	0.0155	0.0150	5.9765	2.9699

D to Z ↓	0.0146	0.0136	9.6884	5.0869
D to Z ↑	0.0137	0.0124	5.9565	2.9630
	X10_P4	**X14_P4**	**X10_P4**	**X14_P4**
A to Z ↓	0.0399	0.0433	3.4454	2.6239
A to Z ↑	0.0244	0.0304	1.9640	1.4595
B to Z ↓	0.0382	0.0422	3.4460	2.6241
B to Z ↑	0.0224	0.0286	1.9616	1.4574
C to Z ↓	0.0150	0.0147	3.4632	2.6358
C to Z ↑	0.0148	0.0145	2.0198	1.5136
D to Z ↓	0.0140	0.0137	3.4730	2.6427
D to Z ↑	0.0126	0.0122	2.0309	1.5173

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.824e-05	1.000e-20
X7_P4	2.351e-05	1.000e-20
X10_P4	3.857e-05	1.000e-20
X14_P4	4.129e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	4.338e-04	5.777e-04	1.032e-03	1.187e-03
B (output stable)	3.929e-04	5.360e-04	9.080e-04	1.076e-03
C (output stable)	2.376e-05	5.302e-05	8.068e-05	1.034e-04
D (output stable)	6.719e-05	1.807e-04	2.130e-04	3.054e-04
A to Z	1.897e-03	3.081e-03	4.873e-03	6.112e-03
B to Z	1.784e-03	2.970e-03	4.446e-03	5.722e-03
C to Z	7.008e-04	1.397e-03	2.011e-03	2.639e-03
D to Z	6.217e-04	1.099e-03	1.642e-03	2.126e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

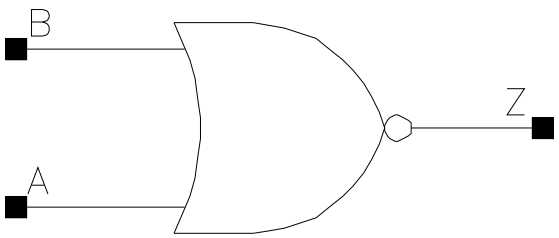
Pin Cycle (vdds)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.408	0.3264
X4_P4	0.800	0.408	0.3264
X8_P4	0.800	0.680	0.5440
X9_P4	1.600	0.408	0.6528
X12_P4	0.800	0.952	0.7616
X16_P4	0.800	1.224	0.9792
X19_P4	1.600	0.680	1.0880
X20_P4	0.800	1.496	1.1968
X23_P4	0.800	1.496	1.1968
X24_P4	0.800	1.768	1.4144
X27_P4	0.800	1.632	1.3056
X29_P4	1.600	0.952	1.5232
X31_P4	0.800	2.312	1.8496
X34_P4	0.800	2.040	1.6320
X38_P4	0.800	2.176	1.7408
X39_P4	1.600	1.224	1.9584
X46_P4	1.600	1.224	1.9584
X57_P4	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P4	X4_P4	X8_P4	X9_P4
A	0.0003	0.0005	0.0009	0.0010
B	0.0003	0.0005	0.0009	0.0010
	X12_P4	X16_P4	X19_P4	X20_P4

A	0.0014	0.0018	0.0020	0.0024
B	0.0013	0.0017	0.0019	0.0021
	X23_P4	X24_P4	X27_P4	X29_P4
A	0.0007	0.0028	0.0007	0.0030
B	0.0006	0.0025	0.0006	0.0028
	X31_P4	X34_P4	X38_P4	X39_P4
A	0.0037	0.0007	0.0007	0.0040
B	0.0034	0.0006	0.0006	0.0037
	X46_P4	X57_P4		
A	0.0006	0.0006		
B	0.0007	0.0007		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X4_P4**	**X2_P4**	**X4_P4**
A to Z ↓	0.0098	0.0092	7.9605	4.1429
A to Z ↑	0.0193	0.0170	22.9877	12.1806
B to Z ↓	0.0089	0.0080	7.9980	4.1701
B to Z ↑	0.0200	0.0172	23.0501	12.2043
	X8_P4	**X9_P4**	**X8_P4**	**X9_P4**
A to Z ↓	0.0085	0.0076	1.9975	1.5445
A to Z ↑	0.0159	0.0156	5.6987	5.4977
B to Z ↓	0.0060	0.0064	1.9982	1.5915
B to Z ↑	0.0132	0.0158	5.7140	5.5083
	X12_P4	**X16_P4**	**X12_P4**	**X16_P4**
A to Z ↓	0.0086	0.0086	1.3655	1.0187
A to Z ↑	0.0155	0.0158	3.7576	2.8597
B to Z ↓	0.0066	0.0063	1.3744	1.0262
B to Z ↑	0.0137	0.0134	3.7707	2.8698
	X19_P4	**X20_P4**	**X19_P4**	**X20_P4**
A to Z ↓	0.0082	0.0089	0.7757	0.8331
A to Z ↑	0.0176	0.0156	2.7993	2.2758
B to Z ↓	0.0065	0.0067	0.7823	0.8391
B to Z ↑	0.0157	0.0138	2.8032	2.2837
	X23_P4	**X24_P4**	**X23_P4**	**X24_P4**
A to Z ↓	0.0342	0.0087	0.8506	0.6913
A to Z ↑	0.0475	0.0156	1.2155	1.9147
B to Z ↓	0.0324	0.0064	0.8506	0.6969
B to Z ↑	0.0475	0.0133	1.2136	1.9211
	X27_P4	**X29_P4**	**X27_P4**	**X29_P4**
A to Z ↓	0.0359	0.0078	0.7104	0.5152
A to Z ↑	0.0491	0.0164	1.0148	1.8770
B to Z ↓	0.0340	0.0061	0.7097	0.5193
B to Z ↑	0.0491	0.0151	1.0132	1.8804
	X31_P4	**X34_P4**	**X31_P4**	**X34_P4**
A to Z ↓	0.0088	0.0373	0.5166	0.5806
A to Z ↑	0.0157	0.0552	1.4363	0.8328
B to Z ↓	0.0066	0.0356	0.5210	0.5803
B to Z ↑	0.0135	0.0555	1.4410	0.8328
	X38_P4	**X39_P4**	**X38_P4**	**X39_P4**
A to Z ↓	0.0381	0.0080	0.5069	0.3922
A to Z ↑	0.0558	0.0169	0.7296	1.4086

B to Z ↓	0.0365	0.0062	0.5068	0.3961
B to Z ↑	0.0561	0.0150	0.7297	1.4112
	X46_P4	**X57_P4**	**X46_P4**	**X57_P4**
A to Z ↓	0.0439	0.0475	0.3774	0.3085
A to Z ↑	0.0587	0.0615	0.7243	0.5819
B to Z ↓	0.0426	0.0461	0.3775	0.3082
B to Z ↑	0.0598	0.0626	0.7239	0.5821

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P4	4.715e-06	1.000e-20
X4_P4	1.037e-05	1.000e-20
X8_P4	2.142e-05	1.000e-20
X9_P4	2.593e-05	1.000e-20
X12_P4	3.089e-05	1.000e-20
X16_P4	4.039e-05	1.000e-20
X19_P4	4.954e-05	1.000e-20
X20_P4	4.990e-05	1.000e-20
X23_P4	7.670e-05	1.000e-20
X24_P4	5.941e-05	1.000e-20
X27_P4	8.642e-05	1.000e-20
X29_P4	7.189e-05	1.000e-20
X31_P4	7.843e-05	1.000e-20
X34_P4	1.087e-04	1.000e-20
X38_P4	1.184e-04	1.000e-20
X39_P4	9.428e-05	1.000e-20
X46_P4	1.265e-04	1.000e-20
X57_P4	1.480e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P4	X4_P4	X8_P4	X9_P4
A (output stable)	8.668e-06	1.530e-05	6.205e-05	3.395e-05
B (output stable)	1.497e-05	2.695e-05	1.532e-04	6.183e-05
A to Z	3.626e-04	6.093e-04	1.213e-03	1.258e-03
B to Z	3.069e-04	4.995e-04	8.140e-04	1.043e-03
	X12_P4	X16_P4	X19_P4	X20_P4
A (output stable)	8.733e-05	1.220e-04	1.303e-04	1.472e-04
B (output stable)	1.882e-04	2.876e-04	3.523e-04	2.986e-04
A to Z	1.787e-03	2.409e-03	2.779e-03	3.005e-03
B to Z	1.289e-03	1.663e-03	2.086e-03	2.154e-03
	X23_P4	X24_P4	X27_P4	X29_P4
A (output stable)	1.681e-05	1.795e-04	1.690e-05	1.684e-04
B (output stable)	3.025e-05	3.889e-04	3.047e-05	3.591e-04
A to Z	5.370e-03	3.555e-03	6.046e-03	3.870e-03
B to Z	5.257e-03	2.486e-03	5.934e-03	2.956e-03
	X31_P4	X34_P4	X38_P4	X39_P4
A (output stable)	2.432e-04	1.811e-05	1.853e-05	2.532e-04
B (output stable)	5.217e-04	3.222e-05	3.274e-05	5.874e-04
A to Z	4.750e-03	8.038e-03	8.730e-03	5.283e-03
B to Z	3.352e-03	7.914e-03	8.605e-03	3.917e-03
	X46_P4	X57_P4		

A (output stable)	1.836e-05	1.894e-05		
B (output stable)	3.304e-05	3.362e-05		
A to Z	9.766e-03	1.197e-02		
B to Z	9.670e-03	1.187e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

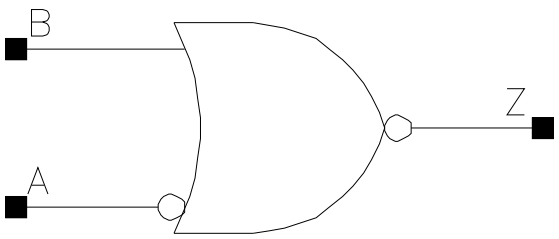
Pin Cycle (vdds)	X2_P4	X4_P4	X8_P4	X9_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P4	X16_P4	X19_P4	X20_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P4	X24_P4	X27_P4	X29_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P4	X34_P4	X38_P4	X39_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P4	X57_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.544	0.4352
X3_P4	0.800	0.544	0.4352
X4_P4	0.800	0.544	0.4352
X10_P4	1.600	0.544	0.8704
X14_P4	1.600	0.816	1.3056
X19_P4	1.600	0.816	1.3056
X29_P4	1.600	1.088	1.7408
X39_P4	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P4	X3_P4	X4_P4	X10_P4
A	0.0005	0.0005	0.0005	0.0009
B	0.0003	0.0003	0.0004	0.0009
	X14_P4	X19_P4	X29_P4	X39_P4
A	0.0009	0.0008	0.0013	0.0013
B	0.0015	0.0018	0.0028	0.0036

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	X3_P4	X2_P4	X3_P4
A to Z ↓	0.0274	0.0275	7.8070	5.7536
A to Z ↑	0.0257	0.0255	22.8850	19.2523
B to Z ↓	0.0086	0.0075	8.0568	5.9392

B to Z ↑	0.0191	0.0181	23.0341	19.3506
	X4_P4	**X10_P4**	**X4_P4**	**X10_P4**
A to Z ↓	0.0282	0.0274	4.3437	1.5007
A to Z ↑	0.0252	0.0240	13.7613	5.4338
B to Z ↓	0.0071	0.0065	4.4864	1.5177
B to Z ↑	0.0161	0.0162	13.8462	5.4666
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0331	0.0347	0.9678	0.7479
A to Z ↑	0.0278	0.0282	3.7222	2.7274
B to Z ↓	0.0059	0.0057	1.0525	0.8164
B to Z ↑	0.0152	0.0141	3.7486	2.7467
	X29_P4	**X39_P4**	**X29_P4**	**X39_P4**
A to Z ↓	0.0303	0.0346	0.5043	0.3792
A to Z ↑	0.0269	0.0287	1.8734	1.3836
B to Z ↓	0.0061	0.0056	0.5203	0.4055
B to Z ↑	0.0151	0.0138	1.8862	1.3938

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P4	8.841e-06	1.000e-20
X3_P4	1.047e-05	1.000e-20
X4_P4	1.364e-05	1.000e-20
X10_P4	3.885e-05	1.000e-20
X14_P4	4.608e-05	1.000e-20
X19_P4	6.184e-05	1.000e-20
X29_P4	9.512e-05	1.000e-20
X39_P4	1.191e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P4	X3_P4	X4_P4	X10_P4
A (output stable)	5.160e-04	5.571e-04	6.187e-04	1.252e-03
B (output stable)	1.510e-05	1.768e-05	2.497e-05	6.568e-05
A to Z	8.794e-04	9.671e-04	1.125e-03	2.567e-03
B to Z	2.880e-04	3.270e-04	4.011e-04	1.090e-03
	X14_P4	X19_P4	X29_P4	X39_P4
A (output stable)	1.842e-03	2.033e-03	3.155e-03	4.031e-03
B (output stable)	9.749e-05	1.312e-04	3.523e-04	2.511e-04
A to Z	3.755e-03	4.466e-03	7.132e-03	8.911e-03
B to Z	1.450e-03	1.826e-03	2.926e-03	3.554e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X2_P4	X3_P4	X4_P4	X10_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P4	X19_P4	X29_P4	X39_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

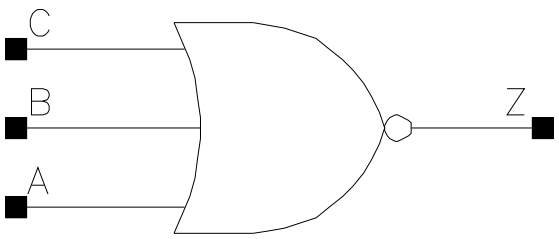
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.544	0.4352
X7_P4	0.800	0.952	0.7616
X11_P4	0.800	1.360	1.0880
X14_P4	0.800	1.768	1.4144
X21_P4	0.800	2.584	2.0672
X29_P4	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X11_P4	X14_P4
A	0.0005	0.0008	0.0014	0.0019
B	0.0005	0.0010	0.0013	0.0020
C	0.0005	0.0008	0.0012	0.0017
	X21_P4	X29_P4		
A	0.0030	0.0039		
B	0.0029	0.0039		
C	0.0025	0.0034		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X7_P4	X3_P4	X7_P4
A to Z ↓	0.0104	0.0104	4.2063	2.1966
A to Z ↑	0.0224	0.0230	17.0502	8.7165

B to Z ↓	0.0098	0.0097	4.2275	2.1238
B to Z ↑	0.0215	0.0231	17.0786	8.7272
C to Z ↓	0.0087	0.0071	4.2763	2.1445
C to Z ↑	0.0206	0.0172	17.0987	8.7310
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0104	0.0104	1.3756	1.0520
A to Z ↑	0.0234	0.0227	5.6985	4.1743
B to Z ↓	0.0098	0.0096	1.3890	1.0259
B to Z ↑	0.0214	0.0224	5.7070	4.1793
C to Z ↓	0.0077	0.0073	1.3835	1.0426
C to Z ↑	0.0187	0.0173	5.7093	4.1818
	X21_P4	**X29_P4**	**X21_P4**	**X29_P4**
A to Z ↓	0.0103	0.0104	0.7014	0.5269
A to Z ↑	0.0225	0.0226	2.7991	2.1038
B to Z ↓	0.0096	0.0097	0.6902	0.5217
B to Z ↑	0.0220	0.0221	2.8020	2.1060
C to Z ↓	0.0075	0.0076	0.7024	0.5302
C to Z ↑	0.0174	0.0176	2.8044	2.1084

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	8.537e-06	1.000e-20
X7_P4	1.658e-05	1.000e-20
X11_P4	2.505e-05	1.000e-20
X14_P4	3.399e-05	1.000e-20
X21_P4	4.995e-05	1.000e-20
X29_P4	6.618e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	1.785e-05	4.288e-05	7.993e-05	8.856e-05
B (output stable)	1.882e-05	6.009e-05	8.073e-05	1.184e-04
C (output stable)	4.957e-05	1.853e-04	2.198e-04	3.656e-04
A to Z	7.652e-04	1.552e-03	2.447e-03	3.191e-03
B to Z	6.427e-04	1.343e-03	1.929e-03	2.743e-03
C to Z	5.277e-04	8.875e-04	1.499e-03	1.877e-03
	X21_P4	X29_P4		
A (output stable)	1.309e-04	1.747e-04		
B (output stable)	1.729e-04	2.326e-04		
C (output stable)	5.144e-04	6.871e-04		
A to Z	4.727e-03	6.309e-03		
B to Z	4.026e-03	5.378e-03		
C to Z	2.807e-03	3.763e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

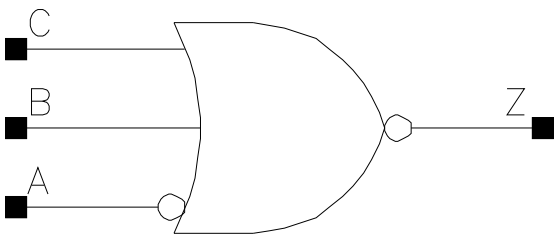
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P4	X29_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X7_P4	0.800	1.360	1.0880
X11_P4	0.800	1.632	1.3056
X14_P4	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X11_P4	X14_P4
A	0.0006	0.0006	0.0009	0.0012
B	0.0005	0.0009	0.0013	0.0017
C	0.0005	0.0009	0.0012	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0304	0.0267	4.0868	1.9152
A to Z ↑	0.0336	0.0331	17.0986	8.2984
B to Z ↓	0.0098	0.0097	4.2475	2.0093
B to Z ↑	0.0213	0.0226	17.1652	8.3269
C to Z ↓	0.0087	0.0075	4.2858	2.0215
C to Z ↑	0.0205	0.0180	17.1871	8.3288
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0325	0.0259	1.3492	0.9983

A to Z ↑	0.0367	0.0323	5.6993	4.2239
B to Z ↓	0.0097	0.0095	1.3905	1.0376
B to Z ↑	0.0212	0.0215	5.7192	4.2399
C to Z ↓	0.0075	0.0073	1.3856	1.0470
C to Z ↑	0.0183	0.0175	5.7238	4.2431

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.297e-05	1.000e-20
X7_P4	2.959e-05	1.000e-20
X11_P4	3.502e-05	1.000e-20
X14_P4	5.328e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	6.665e-04	1.148e-03	1.528e-03	2.114e-03
B (output stable)	1.956e-05	6.841e-05	8.549e-05	1.292e-04
C (output stable)	4.988e-05	2.053e-04	2.217e-04	3.573e-04
A to Z	1.447e-03	2.995e-03	4.072e-03	5.628e-03
B to Z	6.358e-04	1.396e-03	1.922e-03	2.612e-03
C to Z	5.221e-04	9.869e-04	1.462e-03	1.872e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

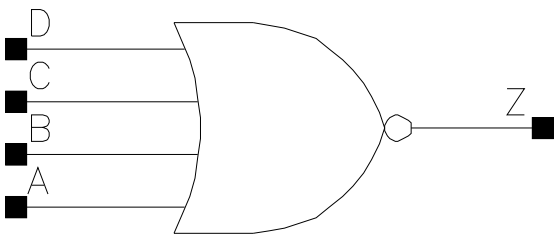
Pin Cycle (vdds)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.224	0.9792
X10_P4	0.800	1.632	1.3056
X14_P4	0.800	1.904	1.5232
X18_P4	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X18_P4
A	0.0004	0.0004	0.0004	0.0005
B	0.0005	0.0005	0.0006	0.0007
C	0.0004	0.0004	0.0005	0.0006
D	0.0005	0.0004	0.0005	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0335	0.0384	4.0610	1.9396
A to Z ↑	0.0557	0.0622	6.1271	2.9450
B to Z ↓	0.0327	0.0388	4.0613	1.9383
B to Z ↑	0.0567	0.0652	6.1270	2.9409
C to Z ↓	0.0349	0.0394	4.0565	1.9365
C to Z ↑	0.0599	0.0678	6.1253	2.9425

D to Z ↓	0.0347	0.0381	4.0542	1.9358
D to Z ↑	0.0619	0.0682	6.1211	2.9412
	X14_P4	**X18_P4**	**X14_P4**	**X18_P4**
A to Z ↓	0.0365	0.0382	1.3346	1.0616
A to Z ↑	0.0558	0.0542	2.0107	1.5233
B to Z ↓	0.0360	0.0369	1.3338	1.0609
B to Z ↑	0.0576	0.0548	2.0086	1.5255
C to Z ↓	0.0356	0.0381	1.3293	1.0570
C to Z ↑	0.0561	0.0552	2.0107	1.5231
D to Z ↓	0.0345	0.0366	1.3274	1.0579
D to Z ↑	0.0570	0.0556	2.0096	1.5235

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.493e-05	1.000e-20
X10_P4	3.727e-05	1.000e-20
X14_P4	5.581e-05	1.000e-20
X18_P4	7.351e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	2.749e-04	3.568e-04	4.393e-04	5.479e-04
B (output stable)	2.544e-04	3.439e-04	4.149e-04	5.075e-04
C (output stable)	2.983e-04	3.505e-04	4.488e-04	5.670e-04
D (output stable)	2.818e-04	3.293e-04	4.196e-04	5.245e-04
A to Z	1.959e-03	3.108e-03	4.334e-03	5.524e-03
B to Z	1.900e-03	3.060e-03	4.252e-03	5.420e-03
C to Z	2.046e-03	3.075e-03	4.085e-03	5.229e-03
D to Z	2.009e-03	3.017e-03	4.010e-03	5.116e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

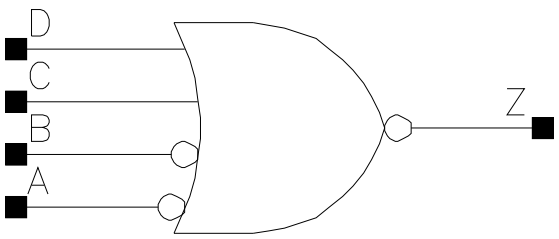
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	1.224	0.9792
X7_P4	0.800	1.496	1.1968
X11_P4	0.800	2.040	1.6320
X14_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P4	X7_P4	X11_P4	X14_P4
A	0.0006	0.0006	0.0012	0.0011
B	0.0006	0.0006	0.0012	0.0012
C	0.0005	0.0009	0.0013	0.0018
D	0.0005	0.0009	0.0013	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X7_P4	X4_P4	X7_P4
A to Z ↓	0.0302	0.0311	3.7855	1.9526
A to Z ↑	0.0421	0.0407	16.3551	8.3850
B to Z ↓	0.0280	0.0288	3.7830	1.9500
B to Z ↑	0.0423	0.0409	16.3631	8.3894
C to Z ↓	0.0100	0.0096	3.8795	2.0259
C to Z ↑	0.0226	0.0224	16.3941	8.4154

D to Z ↓	0.0089	0.0074	3.8992	2.0246
D to Z ↑	0.0216	0.0181	16.4028	8.4199
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0279	0.0307	1.3326	1.0045
A to Z ↑	0.0373	0.0407	5.6496	4.2147
B to Z ↓	0.0254	0.0286	1.3299	1.0020
B to Z ↑	0.0373	0.0413	5.6506	4.2142
C to Z ↓	0.0098	0.0098	1.3896	1.0389
C to Z ↑	0.0211	0.0217	5.6667	4.2259
D to Z ↓	0.0076	0.0074	1.3859	1.0391
D to Z ↑	0.0184	0.0177	5.6716	4.2292

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.914e-05	1.000e-20
X7_P4	2.522e-05	1.000e-20
X11_P4	4.039e-05	1.000e-20
X14_P4	4.635e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X7_P4	X11_P4	X14_P4
A (output stable)	5.546e-04	6.299e-04	1.012e-03	1.212e-03
B (output stable)	5.162e-04	5.900e-04	9.199e-04	1.132e-03
C (output stable)	4.340e-05	6.669e-05	9.666e-05	1.392e-04
D (output stable)	8.807e-05	2.073e-04	2.537e-04	4.009e-04
A to Z	2.405e-03	3.235e-03	4.912e-03	6.388e-03
B to Z	2.240e-03	3.070e-03	4.582e-03	6.073e-03
C to Z	7.230e-04	1.372e-03	1.931e-03	2.651e-03
D to Z	6.120e-04	9.813e-04	1.474e-03	1.919e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

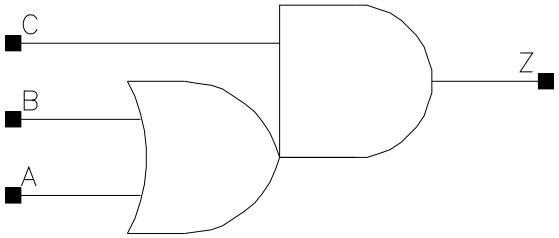
Pin Cycle (vdds)	X4_P4	X7_P4	X11_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.680	0.5440
X10_P4	0.800	0.952	0.7616
X19_P4	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0005	0.0006	0.0010
B	0.0006	0.0006	0.0012
C	0.0007	0.0008	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0296	0.0335	3.8964	1.9488
A to Z ↑	0.0242	0.0286	6.7357	2.9364
B to Z ↓	0.0303	0.0342	3.8948	1.9493
B to Z ↑	0.0226	0.0265	6.7252	2.9365
C to Z ↓	0.0269	0.0289	3.8607	1.9207
C to Z ↑	0.0233	0.0267	6.7281	2.9378
	X19_P4		**X19_P4**	
A to Z ↓	0.0346		1.0131	
A to Z ↑	0.0298		1.4958	

B to Z ↓	0.0355		1.0123	
B to Z ↑	0.0276		1.4932	
C to Z ↓	0.0290		0.9955	
C to Z ↑	0.0269		1.4938	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.095e-05	1.000e-20
X10_P4	3.521e-05	1.000e-20
X19_P4	6.620e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	3.014e-05	3.082e-05	6.474e-05
B (output stable)	3.532e-05	3.732e-05	7.367e-05
C (output stable)	3.179e-05	3.280e-05	6.422e-05
A to Z	1.348e-03	2.251e-03	4.562e-03
B to Z	1.249e-03	2.132e-03	4.337e-03
C to Z	1.479e-03	2.310e-03	4.599e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

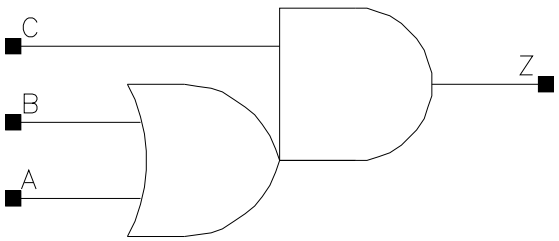
Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	1.360	1.0880
X14_P4	0.800	1.496	1.1968
X19_P4	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0005	0.0012	0.0012	0.0011
B	0.0006	0.0011	0.0011	0.0010
C	0.0006	0.0011	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0366	0.0302	3.8192	1.9330
A to Z ↑	0.0253	0.0230	5.8396	2.8765
B to Z ↓	0.0372	0.0303	3.8166	1.9329
B to Z ↑	0.0236	0.0214	5.8328	2.8725
C to Z ↓	0.0249	0.0203	3.7476	1.9051
C to Z ↑	0.0234	0.0208	5.8287	2.8707
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0334	0.0365	1.3403	1.0132

A to Z ↑	0.0252	0.0271	1.9415	1.4597
B to Z ↓	0.0337	0.0369	1.3410	1.0129
B to Z ↑	0.0236	0.0257	1.9407	1.4593
C to Z ↓	0.0226	0.0247	1.3152	0.9912
C to Z ↑	0.0231	0.0252	1.9397	1.4563

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.363e-05	1.000e-20
X10_P4	4.774e-05	1.000e-20
X14_P4	5.716e-05	1.000e-20
X19_P4	6.645e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.183e-05	2.473e-05	2.482e-05	2.493e-05
B (output stable)	1.493e-05	3.499e-05	3.504e-05	3.516e-05
C (output stable)	1.098e-04	2.203e-04	2.210e-04	2.217e-04
A to Z	1.716e-03	3.005e-03	3.848e-03	4.719e-03
B to Z	1.601e-03	2.730e-03	3.572e-03	4.449e-03
C to Z	1.414e-03	2.396e-03	3.163e-03	3.940e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

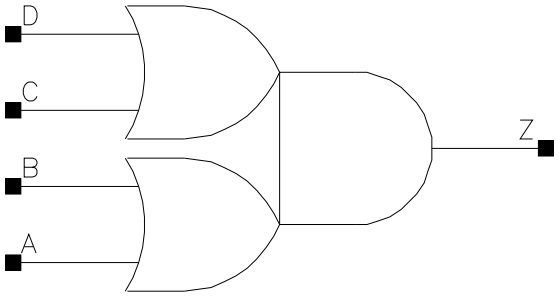
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.952	0.7616
X10_P4	0.800	1.088	0.8704
X14_P4	0.800	1.904	1.5232
X19_P4	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0004	0.0006	0.0011	0.0010
B	0.0004	0.0006	0.0011	0.0011
C	0.0004	0.0006	0.0011	0.0011
D	0.0004	0.0006	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0522	0.0407	3.9539	1.9687
A to Z ↑	0.0356	0.0298	5.8722	2.9298
B to Z ↓	0.0529	0.0414	3.9525	1.9687

B to Z ↑	0.0342	0.0283	5.8645	2.9264
C to Z ↓	0.0447	0.0362	3.9117	1.9568
C to Z ↑	0.0343	0.0297	5.8637	2.9277
D to Z ↓	0.0453	0.0365	3.9149	1.9562
D to Z ↑	0.0326	0.0278	5.8633	2.9240
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0387	0.0408	1.3578	1.0208
A to Z ↑	0.0282	0.0293	1.9505	1.4647
B to Z ↓	0.0377	0.0398	1.3585	1.0213
B to Z ↑	0.0260	0.0271	1.9438	1.4612
C to Z ↓	0.0331	0.0353	1.3484	1.0148
C to Z ↑	0.0273	0.0286	1.9465	1.4635
D to Z ↓	0.0317	0.0340	1.3496	1.0148
D to Z ↑	0.0247	0.0260	1.9426	1.4603

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.770e-05	1.000e-20
X10_P4	3.777e-05	1.000e-20
X14_P4	6.251e-05	1.000e-20
X19_P4	7.123e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.168e-05	1.773e-05	5.220e-05	5.214e-05
B (output stable)	1.494e-05	2.481e-05	1.142e-04	1.137e-04
C (output stable)	3.197e-05	3.991e-05	9.563e-05	9.573e-05
D (output stable)	3.667e-05	4.809e-05	1.505e-04	1.512e-04
A to Z	1.757e-03	2.706e-03	4.539e-03	5.217e-03
B to Z	1.688e-03	2.568e-03	4.141e-03	4.819e-03
C to Z	1.528e-03	2.416e-03	3.947e-03	4.610e-03
D to Z	1.464e-03	2.293e-03	3.548e-03	4.206e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

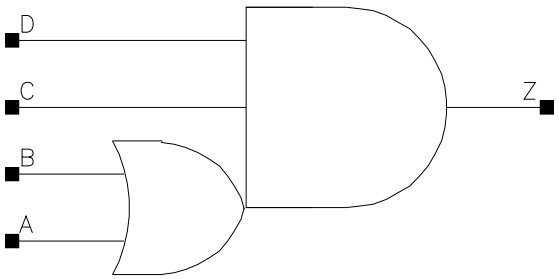
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	0.816	0.6528
X10_P4	0.800	1.088	0.8704
X14_P4	0.800	1.904	1.5232
X19_P4	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P4	X10_P4	X14_P4	X19_P4
A	0.0004	0.0008	0.0009	0.0011
B	0.0004	0.0006	0.0009	0.0011
C	0.0004	0.0006	0.0009	0.0011
D	0.0004	0.0006	0.0009	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X10_P4	X4_P4	X10_P4
A to Z ↓	0.0441	0.0418	4.3232	2.0017
A to Z ↑	0.0399	0.0408	6.2361	2.9783
B to Z ↓	0.0456	0.0391	4.3232	2.0017
B to Z ↑	0.0386	0.0355	6.2354	2.9711
C to Z ↓	0.0364	0.0318	4.2133	1.9642

C to Z ↑	0.0381	0.0360	6.2234	2.9686
D to Z ↓	0.0357	0.0308	4.2158	1.9620
D to Z ↑	0.0399	0.0372	6.2229	2.9708
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0409	0.0386	1.3595	1.0127
A to Z ↑	0.0389	0.0392	1.9838	1.4880
B to Z ↓	0.0396	0.0375	1.3599	1.0126
B to Z ↑	0.0356	0.0358	1.9762	1.4827
C to Z ↓	0.0332	0.0315	1.3343	0.9959
C to Z ↑	0.0360	0.0359	1.9776	1.4809
D to Z ↓	0.0315	0.0301	1.3314	0.9947
D to Z ↑	0.0363	0.0363	1.9794	1.4818

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.465e-05	1.000e-20
X10_P4	3.245e-05	1.000e-20
X14_P4	4.800e-05	1.000e-20
X19_P4	6.335e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X10_P4	X14_P4	X19_P4
A (output stable)	3.605e-05	5.320e-05	8.295e-05	8.880e-05
B (output stable)	3.405e-05	5.804e-05	9.766e-05	1.060e-04
C (output stable)	9.790e-06	1.926e-05	4.988e-05	5.542e-05
D (output stable)	1.467e-05	2.413e-05	8.578e-05	9.299e-05
A to Z	1.486e-03	2.708e-03	4.127e-03	5.135e-03
B to Z	1.433e-03	2.452e-03	3.794e-03	4.716e-03
C to Z	1.586e-03	2.709e-03	4.308e-03	5.297e-03
D to Z	1.530e-03	2.615e-03	4.043e-03	5.001e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

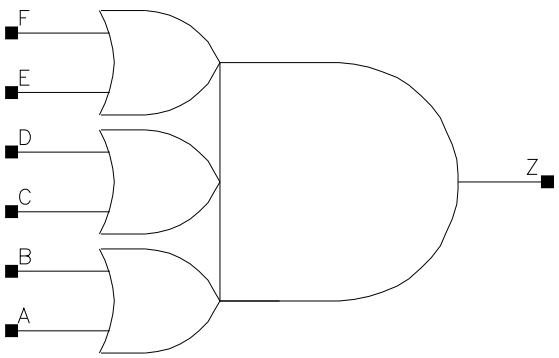
Pin Cycle (vdds)	X4_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	1.360	1.0880
X9_P4	0.800	1.496	1.1968
X19_P4	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P4	X9_P4	X19_P4
A	0.0004	0.0006	0.0009
B	0.0006	0.0008	0.0011
C	0.0004	0.0005	0.0009
D	0.0004	0.0005	0.0011
E	0.0004	0.0005	0.0009
F	0.0004	0.0006	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X9_P4	X4_P4	X9_P4
A to Z ↓	0.0619	0.0497	4.4011	2.1628
A to Z ↑	0.0470	0.0428	6.4016	3.1254
B to Z ↓	0.0644	0.0517	4.4008	2.1627
B to Z ↑	0.0469	0.0417	6.4025	3.1217
C to Z ↓	0.0570	0.0453	4.3683	2.1498
C to Z ↑	0.0473	0.0419	6.4065	3.1250
D to Z ↓	0.0574	0.0458	4.3693	2.1499
D to Z ↑	0.0451	0.0395	6.4019	3.1210
E to Z ↓	0.0488	0.0402	4.3185	2.1364
E to Z ↑	0.0431	0.0395	6.4011	3.1223
F to Z ↓	0.0502	0.0413	4.3214	2.1364
F to Z ↑	0.0418	0.0378	6.3927	3.1174
	X19_P4		X19_P4	
A to Z ↓	0.0480		1.0338	
A to Z ↑	0.0407		1.4864	
B to Z ↓	0.0493		1.0342	
B to Z ↑	0.0383		1.4826	
C to Z ↓	0.0445		1.0275	
C to Z ↑	0.0405		1.4863	
D to Z ↓	0.0454		1.0274	
D to Z ↑	0.0383		1.4823	
E to Z ↓	0.0393		1.0210	
E to Z ↑	0.0384		1.4849	
F to Z ↓	0.0404		1.0214	
F to Z ↑	0.0362		1.4811	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.754e-05	1.000e-20
X9_P4	3.768e-05	1.000e-20
X19_P4	7.424e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X9_P4	X19_P4
A (output stable)	1.083e-05	1.779e-05	3.200e-05
B (output stable)	1.638e-05	2.483e-05	4.174e-05
C (output stable)	1.940e-05	2.625e-05	5.174e-05
D (output stable)	2.308e-05	3.107e-05	6.213e-05
E (output stable)	5.402e-05	6.493e-05	1.214e-04
F (output stable)	5.359e-05	6.988e-05	1.292e-04
A to Z	2.078e-03	3.257e-03	6.330e-03
B to Z	2.035e-03	3.156e-03	6.082e-03
C to Z	1.894e-03	2.982e-03	5.842e-03
D to Z	1.822e-03	2.847e-03	5.589e-03
E to Z	1.643e-03	2.684e-03	5.262e-03
F to Z	1.590e-03	2.575e-03	5.039e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

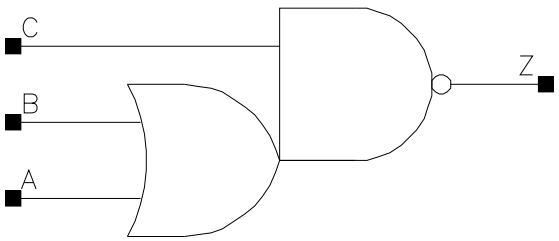
Pin Cycle (vdds)	X4_P4	X9_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.544	0.4352
X10_P4	0.800	1.360	1.0880
X20_P4	0.800	2.720	2.1760
X26_P4	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P4	X10_P4	X20_P4	X26_P4
A	0.0004	0.0013	0.0026	0.0035
B	0.0004	0.0012	0.0024	0.0032
C	0.0004	0.0014	0.0028	0.0038

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X10_P4**	**X3_P4**	**X10_P4**
A to Z ↓	0.0121	0.0133	7.7630	2.4076
A to Z ↑	0.0169	0.0171	13.8506	3.7979
B to Z ↓	0.0102	0.0109	7.6430	2.4234
B to Z ↑	0.0170	0.0155	13.8939	3.8130
C to Z ↓	0.0115	0.0120	7.0775	2.2158
C to Z ↑	0.0164	0.0151	7.3163	2.0218
	X20_P4	**X26_P4**	**X20_P4**	**X26_P4**
A to Z ↓	0.0140	0.0140	1.2275	0.9286

A to Z ↑	0.0178	0.0178	1.9364	1.4555
B to Z ↓	0.0114	0.0115	1.2363	0.9385
B to Z ↑	0.0162	0.0163	1.9430	1.4610
C to Z ↓	0.0127	0.0127	1.1305	0.8564
C to Z ↑	0.0156	0.0155	0.9990	0.7507

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.090e-05	1.000e-20
X10_P4	3.729e-05	1.000e-20
X20_P4	7.344e-05	1.000e-20
X26_P4	9.658e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X10_P4	X20_P4	X26_P4
A (output stable)	2.658e-05	1.006e-04	2.056e-04	2.646e-04
B (output stable)	3.188e-05	1.309e-04	2.710e-04	3.502e-04
C (output stable)	2.833e-05	1.005e-04	2.130e-04	2.794e-04
A to Z	5.229e-04	1.990e-03	4.126e-03	5.479e-03
B to Z	4.312e-04	1.468e-03	3.134e-03	4.181e-03
C to Z	6.528e-04	2.260e-03	4.746e-03	6.270e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

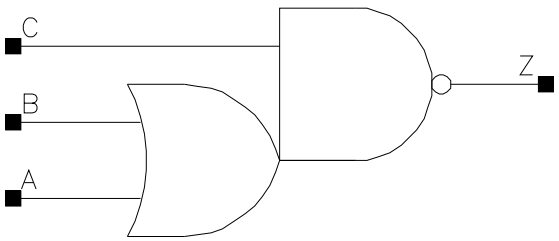
Pin Cycle (vdds)	X3_P4	X10_P4	X20_P4	X26_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X7_P4	0.800	0.952	0.7616
X10_P4	0.800	1.360	1.0880
X13_P4	0.800	1.904	1.5232
X26_P4	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X10_P4	X13_P4
A	0.0005	0.0009	0.0015	0.0019
B	0.0005	0.0009	0.0013	0.0017
C	0.0006	0.0008	0.0013	0.0017
	X26_P4			
A	0.0038			
B	0.0034			
C	0.0034			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X7_P4	X3_P4	X7_P4
A to Z ↓	0.0149	0.0132	6.7406	3.5043
A to Z ↑	0.0228	0.0198	11.0257	5.6308
B to Z ↓	0.0132	0.0112	6.7552	3.4216

B to Z ↑	0.0230	0.0198	11.0486	5.6454
C to Z ↓	0.0126	0.0106	6.3364	3.2403
C to Z ↑	0.0142	0.0119	5.9774	3.0851
	X10_P4	**X13_P4**	**X10_P4**	**X13_P4**
A to Z ↓	0.0128	0.0135	2.3632	1.7986
A to Z ↑	0.0191	0.0209	3.7297	2.8558
B to Z ↓	0.0109	0.0111	2.3564	1.8001
B to Z ↑	0.0190	0.0191	3.7391	2.8631
C to Z ↓	0.0103	0.0104	2.2133	1.6802
C to Z ↑	0.0113	0.0113	2.0406	1.5430
	X26_P4		**X26_P4**	
A to Z ↓	0.0134		0.9256	
A to Z ↑	0.0205		1.4384	
B to Z ↓	0.0109		0.9229	
B to Z ↑	0.0187		1.4425	
C to Z ↓	0.0106		0.8632	
C to Z ↑	0.0111		0.7779	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.458e-05	1.000e-20
X7_P4	2.622e-05	1.000e-20
X10_P4	3.819e-05	1.000e-20
X13_P4	5.087e-05	1.000e-20
X26_P4	9.757e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X7_P4	X10_P4	X13_P4
A (output stable)	1.386e-05	2.522e-05	3.639e-05	6.766e-05
B (output stable)	1.713e-05	3.317e-05	4.912e-05	1.163e-04
C (output stable)	1.107e-04	2.187e-04	2.892e-04	4.225e-04
A to Z	9.927e-04	1.588e-03	2.299e-03	3.351e-03
B to Z	8.545e-04	1.333e-03	1.897e-03	2.563e-03
C to Z	6.622e-04	1.096e-03	1.549e-03	2.157e-03
	X26_P4			
A (output stable)	1.318e-04			
B (output stable)	2.111e-04			
C (output stable)	7.592e-04			
A to Z	6.478e-03			
B to Z	4.901e-03			
C to Z	4.148e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P4	X7_P4	X10_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

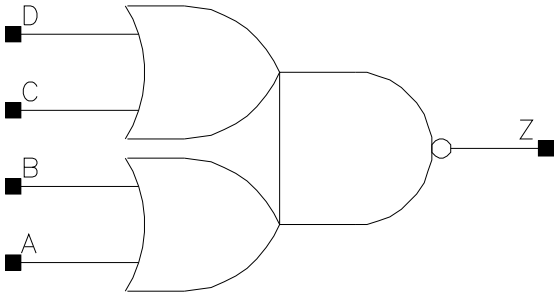
	X26_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X6_P4	0.800	1.360	1.0880
X8_P4	0.800	1.768	1.4144
X11_P4	0.800	2.448	1.9584
X24_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X8_P4	X11_P4
A	0.0005	0.0009	0.0014	0.0018
B	0.0004	0.0008	0.0012	0.0016
C	0.0004	0.0009	0.0013	0.0017
D	0.0004	0.0008	0.0012	0.0016
	X24_P4			
A	0.0039			
B	0.0035			
C	0.0036			
D	0.0033			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X6_P4**	**X3_P4**	**X6_P4**
A to Z ↓	0.0138	0.0162	6.3272	3.4545
A to Z ↑	0.0250	0.0248	13.7464	5.9445
B to Z ↓	0.0124	0.0139	6.2904	3.4612
B to Z ↑	0.0252	0.0229	13.7661	5.9582
C to Z ↓	0.0115	0.0142	6.4032	3.4684
C to Z ↑	0.0176	0.0187	13.7762	5.9681
D to Z ↓	0.0100	0.0113	6.3658	3.4951
D to Z ↑	0.0176	0.0160	13.8060	5.9899
	X8_P4	**X11_P4**	**X8_P4**	**X11_P4**
A to Z ↓	0.0154	0.0156	2.3591	1.7840
A to Z ↑	0.0231	0.0232	3.9799	2.9863
B to Z ↓	0.0135	0.0133	2.3723	1.7859
B to Z ↑	0.0218	0.0218	3.9905	2.9943
C to Z ↓	0.0137	0.0141	2.3766	1.7976
C to Z ↑	0.0174	0.0179	3.9748	3.0023
D to Z ↓	0.0116	0.0114	2.4047	1.8029
D to Z ↑	0.0157	0.0158	3.9920	3.0150
	X24_P4		**X24_P4**	
A to Z ↓	0.0157		0.8673	
A to Z ↑	0.0232		1.4402	
B to Z ↓	0.0134		0.8621	
B to Z ↑	0.0220		1.4441	
C to Z ↓	0.0145		0.8745	
C to Z ↑	0.0178		1.4410	
D to Z ↓	0.0117		0.8716	
D to Z ↑	0.0159		1.4474	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.395e-05	1.000e-20
X6_P4	3.102e-05	1.000e-20
X8_P4	4.437e-05	1.000e-20
X11_P4	5.984e-05	1.000e-20
X24_P4	1.180e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X6_P4	X8_P4	X11_P4
A (output stable)	1.589e-05	5.455e-05	6.933e-05	9.601e-05
B (output stable)	2.147e-05	1.167e-04	1.231e-04	1.939e-04
C (output stable)	3.712e-05	9.637e-05	1.231e-04	1.703e-04
D (output stable)	4.506e-05	1.535e-04	1.780e-04	2.670e-04
A to Z	8.982e-04	2.119e-03	2.907e-03	3.932e-03
B to Z	7.835e-04	1.706e-03	2.352e-03	3.168e-03
C to Z	5.875e-04	1.541e-03	2.111e-03	2.933e-03
D to Z	4.953e-04	1.138e-03	1.611e-03	2.206e-03
	X24_P4			
A (output stable)	1.988e-04			
B (output stable)	3.639e-04			
C (output stable)	3.324e-04			
D (output stable)	4.926e-04			

A to Z	8.098e-03			
B to Z	6.540e-03			
C to Z	6.045e-03			
D to Z	4.588e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

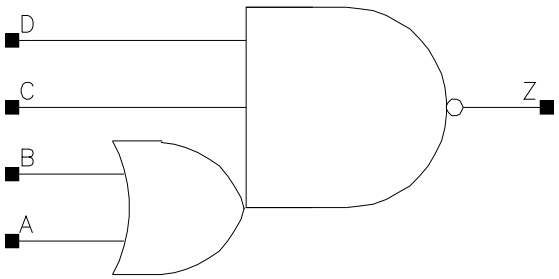
Pin Cycle (vdds)	X3_P4	X6_P4	X8_P4	X11_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X6_P4	0.800	1.360	1.0880
X12_P4	0.800	2.448	1.9584
X18_P4	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X12_P4	X18_P4
A	0.0007	0.0009	0.0017	0.0025
B	0.0004	0.0008	0.0016	0.0024
C	0.0005	0.0009	0.0018	0.0029
D	0.0005	0.0009	0.0017	0.0026

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0224	0.0185	9.5736	5.0844
A to Z ↑	0.0252	0.0202	11.3342	5.6959
B to Z ↓	0.0169	0.0150	9.5504	5.0984
B to Z ↑	0.0213	0.0182	11.3288	5.7130
C to Z ↓	0.0183	0.0181	9.0185	4.8062

C to Z ↑	0.0194	0.0185	5.7958	2.9731
D to Z ↓	0.0198	0.0179	9.0485	4.8220
D to Z ↑	0.0189	0.0170	5.9162	2.9793
	X12_P4	**X18_P4**	**X12_P4**	**X18_P4**
A to Z ↓	0.0188	0.0190	2.6364	1.7809
A to Z ↑	0.0199	0.0199	2.8580	1.9147
B to Z ↓	0.0152	0.0156	2.6459	1.7893
B to Z ↑	0.0178	0.0181	2.8685	1.9218
C to Z ↓	0.0178	0.0180	2.4924	1.6849
C to Z ↑	0.0180	0.0180	1.5115	0.9989
D to Z ↓	0.0178	0.0179	2.5006	1.6900
D to Z ↑	0.0165	0.0165	1.5080	1.0075

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.182e-05	1.000e-20
X6_P4	2.187e-05	1.000e-20
X12_P4	4.107e-05	1.000e-20
X18_P4	6.032e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X6_P4	X12_P4	X18_P4
A (output stable)	5.128e-05	1.036e-04	1.949e-04	2.708e-04
B (output stable)	5.681e-05	1.183e-04	2.138e-04	2.920e-04
C (output stable)	1.698e-05	5.376e-05	9.894e-05	1.567e-04
D (output stable)	2.412e-05	8.851e-05	1.504e-04	2.311e-04
A to Z	1.035e-03	1.628e-03	3.187e-03	4.758e-03
B to Z	7.815e-04	1.244e-03	2.406e-03	3.630e-03
C to Z	1.158e-03	2.127e-03	4.033e-03	6.047e-03
D to Z	1.074e-03	1.813e-03	3.463e-03	5.150e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

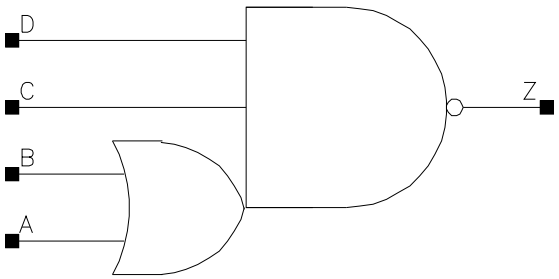
Pin Cycle (vdds)	X3_P4	X6_P4	X12_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X6_P4	0.800	1.360	1.0880
X9_P4	0.800	1.768	1.4144
X12_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X9_P4	X12_P4
A	0.0005	0.0010	0.0015	0.0019
B	0.0005	0.0009	0.0013	0.0020
C	0.0005	0.0009	0.0013	0.0017
D	0.0005	0.0008	0.0012	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0183	0.0188	10.3417	5.0481
A to Z ↑	0.0238	0.0252	11.5887	5.6949
B to Z ↓	0.0161	0.0159	10.1941	5.0639
B to Z ↑	0.0239	0.0237	11.6112	5.7069
C to Z ↓	0.0147	0.0156	9.7657	4.8065

C to Z ↑	0.0151	0.0153	6.2363	3.0618
D to Z ↓	0.0153	0.0148	9.7973	4.8224
D to Z ↑	0.0138	0.0130	6.2934	3.0784
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0190	0.0191	3.4629	2.6239
A to Z ↑	0.0244	0.0248	3.7688	2.9123
B to Z ↓	0.0162	0.0163	3.4634	2.6286
B to Z ↑	0.0232	0.0239	3.7787	2.9211
C to Z ↓	0.0155	0.0156	3.2913	2.4948
C to Z ↑	0.0148	0.0150	2.0275	1.5347
D to Z ↓	0.0150	0.0148	3.3015	2.5031
D to Z ↑	0.0128	0.0126	2.0391	1.5470

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.054e-05	1.000e-20
X6_P4	2.216e-05	1.000e-20
X9_P4	3.103e-05	1.000e-20
X12_P4	4.153e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.002e-05	2.276e-05	3.599e-05	4.580e-05
B (output stable)	1.089e-05	3.445e-05	4.721e-05	6.435e-05
C (output stable)	2.727e-05	6.402e-05	9.431e-05	1.232e-04
D (output stable)	4.778e-05	1.735e-04	1.938e-04	3.090e-04
A to Z	1.003e-03	2.191e-03	3.184e-03	4.267e-03
B to Z	8.645e-04	1.771e-03	2.567e-03	3.436e-03
C to Z	6.939e-04	1.542e-03	2.190e-03	2.983e-03
D to Z	6.122e-04	1.279e-03	1.857e-03	2.449e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

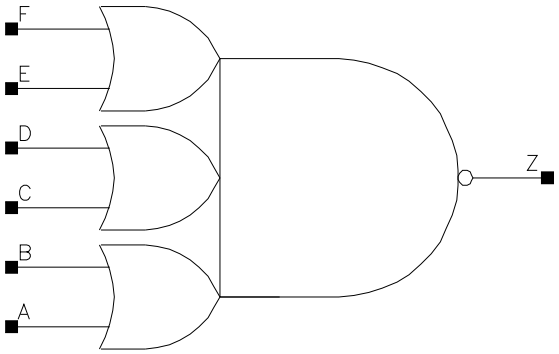
Pin Cycle (vdds)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.224	0.9792
X3_P4	0.800	1.224	0.9792
X5_P4	0.800	2.040	1.6320
X8_P4	0.800	2.720	2.1760
X10_P4	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P4	X3_P4	X5_P4	X8_P4
A	0.0004	0.0005	0.0010	0.0015
B	0.0004	0.0005	0.0009	0.0013
C	0.0004	0.0005	0.0009	0.0014
D	0.0004	0.0004	0.0009	0.0012

E	0.0004	0.0005	0.0009	0.0013
F	0.0004	0.0004	0.0008	0.0012
	X10_P4			
A	0.0019			
B	0.0017			
C	0.0018			
D	0.0016			
E	0.0017			
F	0.0016			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X3_P4**	**X2_P4**	**X3_P4**
A to Z ↓	0.0241	0.0229	11.3956	8.7239
A to Z ↑	0.0346	0.0298	15.9071	10.9377
B to Z ↓	0.0227	0.0214	11.4177	8.7616
B to Z ↑	0.0355	0.0307	15.9224	10.9539
C to Z ↓	0.0235	0.0228	11.4490	8.7544
C to Z ↑	0.0303	0.0268	15.9120	11.0635
D to Z ↓	0.0227	0.0206	11.5238	8.8293
D to Z ↑	0.0322	0.0270	15.9514	11.0726
E to Z ↓	0.0203	0.0197	11.4735	8.7665
E to Z ↑	0.0241	0.0213	15.9121	11.0794
F to Z ↓	0.0190	0.0178	11.5284	8.8422
F to Z ↑	0.0251	0.0216	15.9483	11.0998
	X5_P4	**X8_P4**	**X5_P4**	**X8_P4**
A to Z ↓	0.0242	0.0238	4.6065	3.1396
A to Z ↑	0.0308	0.0297	5.6969	3.7787
B to Z ↓	0.0215	0.0212	4.6234	3.1416
B to Z ↑	0.0294	0.0290	5.7059	3.7853
C to Z ↓	0.0222	0.0228	4.6301	3.1573
C to Z ↑	0.0260	0.0257	5.7333	3.8426
D to Z ↓	0.0195	0.0201	4.6394	3.1568
D to Z ↑	0.0249	0.0254	5.7501	3.8495
E to Z ↓	0.0206	0.0204	4.6468	3.1648
E to Z ↑	0.0214	0.0206	5.7404	3.8518
F to Z ↓	0.0176	0.0175	4.6595	3.1564
F to Z ↑	0.0196	0.0199	5.7583	3.8634
	X10_P4		**X10_P4**	
A to Z ↓	0.0243		2.3776	
A to Z ↑	0.0301		2.8635	
B to Z ↓	0.0215		2.3808	
B to Z ↑	0.0290		2.8695	
C to Z ↓	0.0225		2.3876	
C to Z ↑	0.0257		2.9030	
D to Z ↓	0.0198		2.3913	
D to Z ↑	0.0249		2.9108	
E to Z ↓	0.0206		2.3917	
E to Z ↑	0.0209		2.8976	
F to Z ↓	0.0179		2.4009	
F to Z ↑	0.0197		2.9083	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P4	1.266e-05	1.000e-20
X3_P4	1.965e-05	1.000e-20
X5_P4	3.672e-05	1.000e-20
X8_P4	5.213e-05	1.000e-20
X10_P4	6.924e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P4	X3_P4	X5_P4	X8_P4
A (output stable)	1.398e-05	1.743e-05	4.951e-05	6.762e-05
B (output stable)	1.742e-05	2.284e-05	8.857e-05	1.040e-04
C (output stable)	2.280e-05	2.854e-05	6.756e-05	9.196e-05
D (output stable)	2.686e-05	3.315e-05	1.038e-04	1.216e-04
E (output stable)	5.751e-05	7.170e-05	1.274e-04	1.892e-04
F (output stable)	6.232e-05	7.847e-05	1.640e-04	2.224e-04
A to Z	1.250e-03	1.520e-03	3.071e-03	4.405e-03
B to Z	1.155e-03	1.390e-03	2.641e-03	3.815e-03
C to Z	1.036e-03	1.280e-03	2.457e-03	3.589e-03
D to Z	9.623e-04	1.145e-03	2.100e-03	3.122e-03
E to Z	7.964e-04	9.907e-04	1.997e-03	2.820e-03
F to Z	7.210e-04	8.762e-04	1.636e-03	2.384e-03
	X10_P4			
A (output stable)	9.479e-05			
B (output stable)	1.612e-04			
C (output stable)	1.254e-04			
D (output stable)	1.900e-04			
E (output stable)	2.417e-04			
F (output stable)	3.020e-04			
A to Z	5.958e-03			
B to Z	5.126e-03			
C to Z	4.797e-03			
D to Z	4.112e-03			
E to Z	3.856e-03			
F to Z	3.212e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X2_P4	X3_P4	X5_P4	X8_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P4			

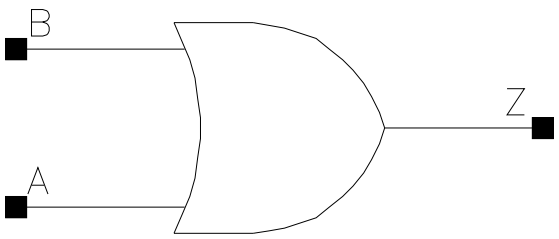
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.544	0.4352
X9_P4	0.800	0.680	0.5440
X19_P4	0.800	1.360	1.0880
X29_P4	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4	X29_P4
A	0.0005	0.0006	0.0010	0.0010
B	0.0004	0.0005	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X9_P4**	**X5_P4**	**X9_P4**
A to Z ↓	0.0389	0.0331	4.1474	2.0834
A to Z ↑	0.0235	0.0242	6.0752	3.0491
B to Z ↓	0.0391	0.0330	4.1474	2.0841
B to Z ↑	0.0225	0.0226	6.0785	3.0490
	X19_P4	**X29_P4**	**X19_P4**	**X29_P4**
A to Z ↓	0.0336	0.0396	0.9976	0.6812
A to Z ↑	0.0239	0.0273	1.4533	0.9757
B to Z ↓	0.0320	0.0381	0.9977	0.6813
B to Z ↑	0.0218	0.0251	1.4499	0.9744

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.456e-05	1.000e-20
X9_P4	2.844e-05	1.000e-20
X19_P4	5.748e-05	1.000e-20
X29_P4	7.376e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4	X29_P4
A (output stable)	9.149e-06	1.752e-05	6.515e-05	6.544e-05
B (output stable)	1.773e-05	3.027e-05	1.716e-04	1.723e-04
A to Z	1.264e-03	2.011e-03	4.257e-03	6.056e-03
B to Z	1.200e-03	1.895e-03	3.839e-03	5.621e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

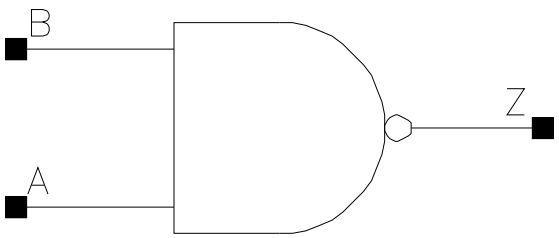
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4	X29_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X9_P4	0.800	0.952	0.7616
X14_P4	0.800	1.088	0.8704
X18_P4	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P4	X9_P4	X14_P4	X18_P4
A	0.0006	0.0006	0.0006	0.0005
B	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X9_P4**	**X5_P4**	**X9_P4**
A to Z ↓	0.0303	0.0349	3.7299	2.0445
A to Z ↑	0.0326	0.0360	5.8099	3.0569
B to Z ↓	0.0313	0.0367	3.7314	2.0470
B to Z ↑	0.0308	0.0349	5.8044	3.0571
	X14_P4	**X18_P4**	**X14_P4**	**X18_P4**
A to Z ↓	0.0385	0.0410	1.4086	1.0706
A to Z ↑	0.0385	0.0397	2.0279	1.5578
B to Z ↓	0.0403	0.0427	1.4100	1.0707
B to Z ↑	0.0375	0.0386	2.0276	1.5594

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	3.378e-05	1.000e-20
X9_P4	4.086e-05	1.000e-20
X14_P4	4.937e-05	1.000e-20
X18_P4	5.375e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X9_P4	X14_P4	X18_P4
A (output stable)	1.064e-05	1.004e-05	1.010e-05	1.042e-05
B (output stable)	2.148e-05	1.943e-05	1.955e-05	1.858e-05
A to Z	2.245e-03	2.895e-03	3.731e-03	4.227e-03
B to Z	2.165e-03	2.826e-03	3.661e-03	4.157e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

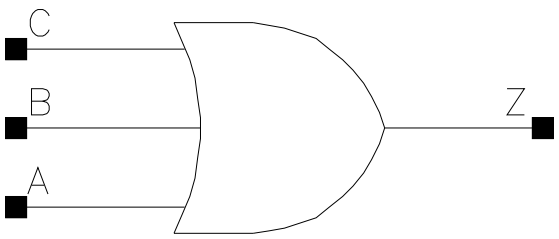
Pin Cycle (vdds)	X5_P4	X9_P4	X14_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.680	0.5440
X10_P4	0.800	0.952	0.7616
X14_P4	0.800	1.496	1.1968
X19_P4	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0004	0.0006	0.0010	0.0016
B	0.0004	0.0006	0.0012	0.0016
C	0.0004	0.0006	0.0011	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0522	0.0451	4.2927	2.0300
A to Z ↑	0.0274	0.0234	6.1018	2.8939
B to Z ↓	0.0513	0.0443	4.2883	2.0317
B to Z ↑	0.0269	0.0224	6.1046	2.8942
C to Z ↓	0.0513	0.0432	4.2937	2.0316
C to Z ↑	0.0260	0.0210	6.1074	2.8926
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0422	0.0408	1.3552	1.0344

A to Z ↑	0.0216	0.0214	1.9664	1.5041
B to Z ↓	0.0426	0.0394	1.3574	1.0352
B to Z ↑	0.0206	0.0207	1.9655	1.5010
C to Z ↓	0.0377	0.0369	1.3565	1.0348
C to Z ↑	0.0187	0.0188	1.9611	1.5003

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.338e-05	1.000e-20
X10_P4	2.776e-05	1.000e-20
X14_P4	4.598e-05	1.000e-20
X19_P4	6.195e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.085e-05	2.049e-05	4.298e-05	8.034e-05
B (output stable)	1.168e-05	2.070e-05	5.930e-05	8.092e-05
C (output stable)	2.945e-05	5.394e-05	1.918e-04	2.143e-04
A to Z	1.509e-03	2.467e-03	4.045e-03	5.740e-03
B to Z	1.433e-03	2.334e-03	3.833e-03	5.219e-03
C to Z	1.372e-03	2.210e-03	3.381e-03	4.749e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

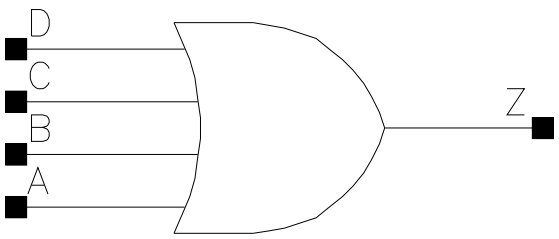
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	1.224	0.9792
X8_P4	0.800	1.496	1.1968
X12_P4	0.800	2.176	1.7408
X15_P4	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X12_P4	X15_P4
A	0.0004	0.0005	0.0010	0.0011
B	0.0004	0.0006	0.0009	0.0011
C	0.0004	0.0005	0.0010	0.0011
D	0.0004	0.0006	0.0009	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0402	0.0375	6.5797	3.4677
A to Z ↑	0.0240	0.0242	5.6797	2.9946
B to Z ↓	0.0415	0.0384	6.5819	3.4668
B to Z ↑	0.0232	0.0232	5.6856	2.9940
C to Z ↓	0.0433	0.0368	6.5936	3.4608
C to Z ↑	0.0251	0.0236	5.8157	3.0087

D to Z ↓	0.0451	0.0379	6.5935	3.4605
D to Z ↑	0.0245	0.0227	5.8116	3.0029
	X12_P4	**X15_P4**	**X12_P4**	**X15_P4**
A to Z ↓	0.0382	0.0385	2.3843	1.7910
A to Z ↑	0.0248	0.0235	1.9382	1.4784
B to Z ↓	0.0375	0.0371	2.3841	1.7916
B to Z ↑	0.0234	0.0217	1.9350	1.4769
C to Z ↓	0.0369	0.0367	2.3826	1.7872
C to Z ↑	0.0235	0.0223	1.9318	1.4871
D to Z ↓	0.0363	0.0357	2.3822	1.7881
D to Z ↑	0.0222	0.0207	1.9303	1.4855

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.654e-05	1.000e-20
X8_P4	3.529e-05	1.000e-20
X12_P4	4.453e-05	1.000e-20
X15_P4	6.520e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	3.164e-04	5.591e-04	8.605e-04	1.183e-03
B (output stable)	2.974e-04	5.185e-04	7.793e-04	1.061e-03
C (output stable)	3.154e-04	5.312e-04	7.877e-04	1.072e-03
D (output stable)	2.976e-04	4.909e-04	7.081e-04	9.758e-04
A to Z	1.361e-03	2.696e-03	3.807e-03	5.116e-03
B to Z	1.309e-03	2.589e-03	3.557e-03	4.695e-03
C to Z	1.405e-03	2.417e-03	3.419e-03	4.425e-03
D to Z	1.358e-03	2.314e-03	3.175e-03	4.082e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

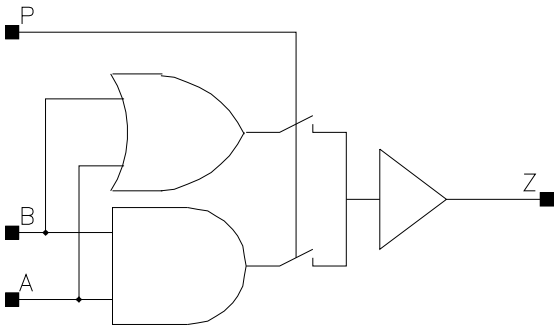
Pin Cycle (vdds)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.952	0.7616
X10_P4	1.600	0.816	1.3056
X14_P4	1.600	1.224	1.9584
X19_P4	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0008	0.0010	0.0019	0.0019
B	0.0008	0.0011	0.0019	0.0020
P	0.0004	0.0006	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0481	0.0427	4.2228	1.9566
A to Z ↑	0.0269	0.0311	6.1169	2.9179
B to Z ↓	0.0478	0.0435	4.2321	1.9636
B to Z ↑	0.0280	0.0327	6.1262	2.9232
P to Z ↓	0.0431	0.0409	4.2276	1.9636
P to Z ↑	0.0267	0.0316	6.1141	2.9191
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**

A to Z ↓	0.0392	0.0418	1.3418	0.9902
A to Z ↑	0.0296	0.0310	1.9888	1.4847
B to Z ↓	0.0371	0.0396	1.3522	0.9973
B to Z ↑	0.0292	0.0308	1.9894	1.4864
P to Z ↓	0.0359	0.0389	1.3553	0.9981
P to Z ↑	0.0292	0.0312	1.9892	1.4844

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.809e-05	1.000e-20
X10_P4	4.073e-05	1.000e-20
X14_P4	6.602e-05	1.000e-20
X19_P4	7.711e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	2.489e-05	3.670e-05	1.058e-04	1.006e-04
B (output stable)	3.334e-05	5.600e-05	2.250e-04	2.164e-04
P (output stable)	9.625e-05	1.518e-04	2.929e-04	2.664e-04
A to Z	1.520e-03	2.875e-03	4.596e-03	5.468e-03
B to Z	1.478e-03	2.844e-03	4.315e-03	5.190e-03
P to Z	1.334e-03	2.658e-03	4.198e-03	5.122e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

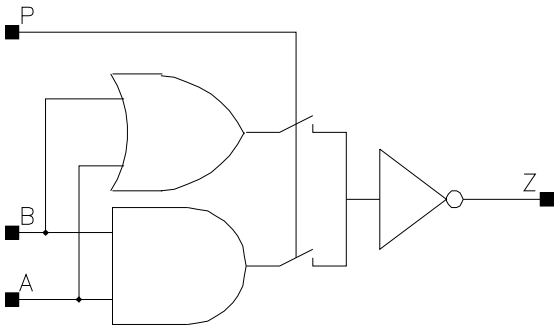
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.600	0.544	0.8704
X10_P4	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P4	X10_P4
A	0.0009	0.0017
B	0.0008	0.0016
P	0.0006	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0160	0.0148	6.6145	3.4457
A to Z ↑	0.0254	0.0234	11.0424	5.5899
B to Z ↓	0.0169	0.0142	6.5594	3.4559
B to Z ↑	0.0253	0.0209	11.0205	5.6461
P to Z ↓	0.0167	0.0134	6.6863	3.4820
P to Z ↑	0.0238	0.0187	11.1024	5.6204

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	1.862e-05	1.000e-20
X10_P4	3.439e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4
A (output stable)	3.510e-05	1.056e-04
B (output stable)	5.053e-05	2.197e-04
P (output stable)	1.308e-04	2.982e-04
A to Z	1.129e-03	1.992e-03
B to Z	1.067e-03	1.678e-03
P to Z	9.098e-04	1.482e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

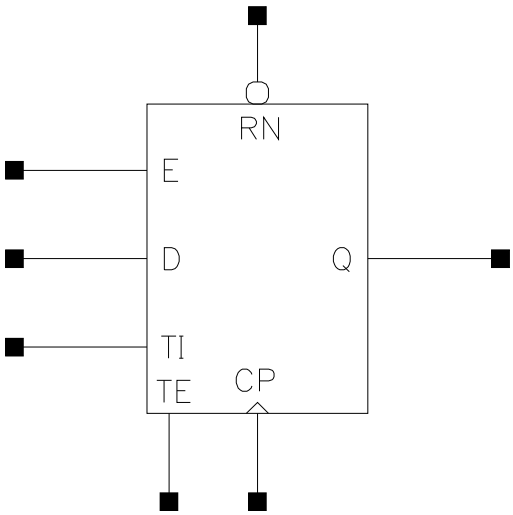
Pin Cycle (vdds)	X5_P4	X10_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.600	2.992	4.7872
X10_P4	1.600	3.128	5.0048
X19_P4	1.600	3.264	5.2224
X23_P4	1.600	3.264	5.2224
X29_P4	1.600	3.536	5.6576
X34_P4	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4	X23_P4
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0011	0.0011	0.0011	0.0011

RN	0.0008	0.0008	0.0008	0.0008
TE	0.0008	0.0008	0.0008	0.0008
TI	0.0003	0.0003	0.0003	0.0003
	X29_P4	X34_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0011	0.0011		
RN	0.0008	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
CP to Q ↓	0.0608	0.0994	3.8456	1.9187
CP to Q ↑	0.0848	0.1333	5.7645	2.9150
RN to Q ↓	0.0513	0.0960	3.8549	1.9190
	X19_P4	**X23_P4**	**X19_P4**	**X23_P4**
CP to Q ↓	0.1070	0.1081	0.9833	0.7325
CP to Q ↑	0.1380	0.1363	1.4647	1.4404
RN to Q ↓	0.0974	0.0987	0.9800	0.7293
	X29_P4	**X34_P4**	**X29_P4**	**X34_P4**
CP to Q ↓	0.0899	0.0892	0.6426	0.5038
CP to Q ↑	0.1107	0.1117	0.9717	0.9714
RN to Q ↓	0.0822	0.0813	0.6436	0.5036

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P4	X10_P4	X19_P4	X23_P4
CP ↓	min_pulse_width to CP	0.0798	0.0798	0.0798	0.0798
CP ↑	min_pulse_width to CP	0.0532	0.0533	0.0533	0.0533
D ↓	hold_rising to CP	-0.0511	-0.0511	-0.0511	-0.0511
D ↑	hold_rising to CP	-0.0196	-0.0196	-0.0196	-0.0196
D ↓	setup_rising to CP	0.0906	0.0906	0.0906	0.0906
D ↑	setup_rising to CP	0.0467	0.0435	0.0435	0.0435
E ↓	hold_rising to CP	-0.0474	-0.0533	-0.0474	-0.0474
E ↑	hold_rising to CP	-0.0192	-0.0192	-0.0192	-0.0192
E ↓	setup_rising to CP	0.1295	0.1295	0.1295	0.1295
E ↑	setup_rising to CP	0.0933	0.0933	0.0933	0.0933
RN ↓	min_pulse_width to RN	0.0686	0.0615	0.0659	0.0686
RN ↑	recovery_rising to CP	-0.0044	-0.0044	-0.0044	-0.0044
RN ↑	removal_rising to CP	0.0140	0.0140	0.0140	0.0140
TE ↓	hold_rising to CP	-0.0289	-0.0289	-0.0289	-0.0289

TE ↑	hold_rising to CP	-0.0116	-0.0142	-0.0116	-0.0116
TE ↓	setup_rising to CP	0.0732	0.0732	0.0732	0.0732
TE ↑	setup_rising to CP	0.0933	0.0933	0.0933	0.0933
TI ↓	hold_rising to CP	-0.0531	-0.0521	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0100	-0.0098	-0.0098	-0.0098
TI ↓	setup_rising to CP	0.0932	0.0932	0.0932	0.0932
TI ↑	setup_rising to CP	0.0404	0.0404	0.0404	0.0404
		X29_P4	X34_P4		
CP ↓	min_pulse_width to CP	0.0798	0.0798		
CP ↑	min_pulse_width to CP	0.0532	0.0532		
D ↓	hold_rising to CP	-0.0511	-0.0511		
D ↑	hold_rising to CP	-0.0196	-0.0196		
D ↓	setup_rising to CP	0.0906	0.0906		
D ↑	setup_rising to CP	0.0467	0.0467		
E ↓	hold_rising to CP	-0.0474	-0.0474		
E ↑	hold_rising to CP	-0.0192	-0.0192		
E ↓	setup_rising to CP	0.1295	0.1295		
E ↑	setup_rising to CP	0.0933	0.0933		
RN ↓	min_pulse_width to RN	0.0708	0.0708		
RN ↑	recovery_rising to CP	-0.0044	-0.0044		
RN ↑	removal_rising to CP	0.0140	0.0140		
TE ↓	hold_rising to CP	-0.0289	-0.0289		
TE ↑	hold_rising to CP	-0.0116	-0.0116		
TE ↓	setup_rising to CP	0.0732	0.0732		
TE ↑	setup_rising to CP	0.0933	0.0933		
TI ↓	hold_rising to CP	-0.0531	-0.0531		
TI ↑	hold_rising to CP	-0.0100	-0.0100		
TI ↓	setup_rising to CP	0.0932	0.0932		
TI ↑	setup_rising to CP	0.0404	0.0404		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	7.269e-05	1.000e-20
X10_P4	8.932e-05	1.000e-20
X19_P4	1.178e-04	1.000e-20
X23_P4	1.237e-04	1.000e-20

X29_P4	1.540e-04	1.000e-20
X34_P4	1.627e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

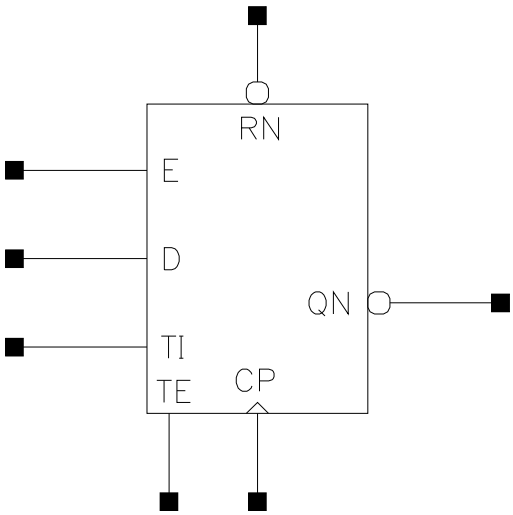
Pin Cycle	X5_P4	X10_P4	X19_P4	X23_P4
Clock 100Mhz Data 0Mhz	6.033e-03	6.026e-03	6.030e-03	6.033e-03
Clock 100Mhz Data 25Mhz	6.243e-03	6.585e-03	7.131e-03	7.187e-03
Clock 100Mhz Data 50Mhz	6.453e-03	7.144e-03	8.231e-03	8.341e-03
Clock = 0 Data 100Mhz	3.489e-03	3.489e-03	3.488e-03	3.488e-03
Clock = 1 Data 100Mhz	1.411e-03	1.411e-03	1.411e-03	1.411e-03
	X29_P4	X34_P4		
Clock 100Mhz Data 0Mhz	6.032e-03	6.033e-03		
Clock 100Mhz Data 25Mhz	7.692e-03	7.853e-03		
Clock 100Mhz Data 50Mhz	9.352e-03	9.673e-03		
Clock = 0 Data 100Mhz	3.489e-03	3.489e-03		
Clock = 1 Data 100Mhz	1.412e-03	1.412e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.600	2.992	4.7872
X10_P4	1.600	3.128	5.0048
X19_P4	1.600	3.264	5.2224
X23_P4	1.600	3.264	5.2224
X29_P4	1.600	3.536	5.6576
X34_P4	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4	X23_P4
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0011	0.0012	0.0012	0.0012

RN	0.0008	0.0008	0.0008	0.0008
TE	0.0008	0.0008	0.0008	0.0008
TI	0.0003	0.0003	0.0003	0.0003
	X29_P4	X34_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0012	0.0011		
RN	0.0008	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
CP to QN ↓	0.1177	0.1009	3.8633	1.9163
CP to QN ↑	0.0840	0.0767	5.7581	2.9130
RN to QN ↑	0.0802	0.0687	5.7581	2.9097
	X19_P4	**X23_P4**	**X19_P4**	**X23_P4**
CP to QN ↓	0.1057	0.1066	0.9771	0.7321
CP to QN ↑	0.0833	0.0810	1.4664	1.4418
RN to QN ↑	0.0757	0.0730	1.4659	1.4418
	X29_P4	**X34_P4**	**X29_P4**	**X34_P4**
CP to QN ↓	0.1454	0.1421	0.6427	0.4973
CP to QN ↑	0.1112	0.1095	0.9727	0.9712
RN to QN ↑	0.1071	0.1062	0.9737	0.9704

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P4	X10_P4	X19_P4	X23_P4
CP ↓	min_pulse_width to CP	0.0798	0.0798	0.0798	0.0798
CP ↑	min_pulse_width to CP	0.0532	0.0532	0.0532	0.0545
D ↓	hold_rising to CP	-0.0511	-0.0511	-0.0511	-0.0511
D ↑	hold_rising to CP	-0.0196	-0.0196	-0.0196	-0.0196
D ↓	setup_rising to CP	0.0906	0.0906	0.0906	0.0906
D ↑	setup_rising to CP	0.0435	0.0467	0.0467	0.0467
E ↓	hold_rising to CP	-0.0533	-0.0474	-0.0474	-0.0474
E ↑	hold_rising to CP	-0.0192	-0.0192	-0.0192	-0.0192
E ↓	setup_rising to CP	0.1295	0.1295	0.1295	0.1295
E ↑	setup_rising to CP	0.0933	0.0933	0.0933	0.0933
RN ↓	min_pulse_width to RN	0.0637	0.0659	0.0708	0.0708
RN ↑	recovery_rising to CP	-0.0044	-0.0044	-0.0044	-0.0044
RN ↑	removal_rising to CP	0.0140	0.0140	0.0140	0.0140
TE ↓	hold_rising to CP	-0.0289	-0.0289	-0.0289	-0.0289

TE ↑	hold_rising to CP	-0.0142	-0.0116	-0.0116	-0.0116
TE ↓	setup_rising to CP	0.0732	0.0732	0.0732	0.0732
TE ↑	setup_rising to CP	0.0933	0.0933	0.0933	0.0933
TI ↓	hold_rising to CP	-0.0521	-0.0531	-0.0531	-0.0531
TI ↑	hold_rising to CP	-0.0098	-0.0100	-0.0100	-0.0100
TI ↓	setup_rising to CP	0.0932	0.0932	0.0932	0.0932
TI ↑	setup_rising to CP	0.0404	0.0404	0.0404	0.0404
		X29_P4	X34_P4		
CP ↓	min_pulse_width to CP	0.0798	0.0798		
CP ↑	min_pulse_width to CP	0.0533	0.0533		
D ↓	hold_rising to CP	-0.0511	-0.0511		
D ↑	hold_rising to CP	-0.0196	-0.0196		
D ↓	setup_rising to CP	0.0906	0.0906		
D ↑	setup_rising to CP	0.0435	0.0435		
E ↓	hold_rising to CP	-0.0533	-0.0533		
E ↑	hold_rising to CP	-0.0192	-0.0192		
E ↓	setup_rising to CP	0.1295	0.1295		
E ↑	setup_rising to CP	0.0933	0.0933		
RN ↓	min_pulse_width to RN	0.0637	0.0615		
RN ↑	recovery_rising to CP	-0.0044	-0.0044		
RN ↑	removal_rising to CP	0.0140	0.0140		
TE ↓	hold_rising to CP	-0.0289	-0.0289		
TE ↑	hold_rising to CP	-0.0116	-0.0116		
TE ↓	setup_rising to CP	0.0732	0.0732		
TE ↑	setup_rising to CP	0.0933	0.0933		
TI ↓	hold_rising to CP	-0.0521	-0.0521		
TI ↑	hold_rising to CP	-0.0098	-0.0098		
TI ↓	setup_rising to CP	0.0932	0.0932		
TI ↑	setup_rising to CP	0.0404	0.0404		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	7.314e-05	1.000e-20
X10_P4	8.832e-05	1.000e-20
X19_P4	1.173e-04	1.000e-20
X23_P4	1.267e-04	1.000e-20

X29_P4	1.510e-04	1.000e-20
X34_P4	1.649e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

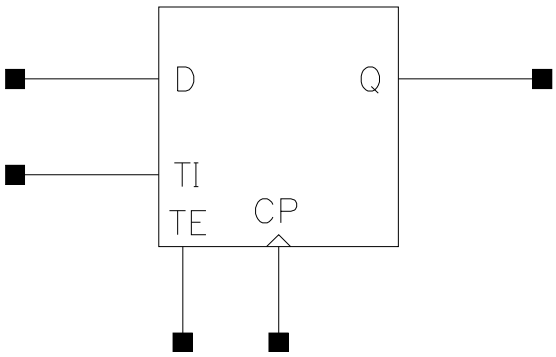
Pin Cycle	X5_P4	X10_P4	X19_P4	X23_P4
Clock 100Mhz Data 0Mhz	6.025e-03	6.032e-03	6.035e-03	6.036e-03
Clock 100Mhz Data 25Mhz	6.282e-03	6.558e-03	7.140e-03	7.184e-03
Clock 100Mhz Data 50Mhz	6.539e-03	7.084e-03	8.246e-03	8.332e-03
Clock = 0 Data 100Mhz	3.489e-03	3.489e-03	3.489e-03	3.489e-03
Clock = 1 Data 100Mhz	1.411e-03	1.411e-03	1.411e-03	1.412e-03
	X29_P4	X34_P4		
Clock 100Mhz Data 0Mhz	6.036e-03	6.035e-03		
Clock 100Mhz Data 25Mhz	7.733e-03	7.855e-03		
Clock 100Mhz Data 50Mhz	9.430e-03	9.674e-03		
Clock = 0 Data 100Mhz	3.490e-03	3.489e-03		
Clock = 1 Data 100Mhz	1.412e-03	1.412e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P4	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P4	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P4	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P4	C8T28SOI_LLHF_-SDFPQX3_P4	C8T28SOIDV_LL_-SDFPQX5_P4	C8T28SOIDV_LL_-SDFPQX10_P4
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P4	C8T28SOIDV_LL_-SDFPQX23_P4	C8T28SOIDV_LL_-SDFPQX29_P4	
CP	0.0004	0.0004	0.0004	
D	0.0004	0.0004	0.0004	
TE	0.0008	0.0008	0.0008	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P4	**C8T28SOI_LLHF_-SDFPQX3_P4**	**C8T28SOI_LL_-SDFPQX5_P4**	**C8T28SOI_LLHF_-SDFPQX3_P4**
CP to Q ↓	0.0645	0.0547	4.0583	6.3508
CP to Q ↑	0.0608	0.0714	5.8210	8.9211
	C8T28SOIDV_LL_-SDFPQX5_P4	**C8T28SOIDV_LL_-SDFPQX10_P4**	**C8T28SOIDV_LL_-SDFPQX5_P4**	**C8T28SOIDV_LL_-SDFPQX10_P4**
CP to Q ↓	0.0565	0.0797	3.8390	1.8660
CP to Q ↑	0.0716	0.1033	5.7595	2.8827
	C8T28SOIDV_LL_-SDFPQX19_P4	**C8T28SOIDV_LL_-SDFPQX23_P4**	**C8T28SOIDV_LL_-SDFPQX19_P4**	**C8T28SOIDV_LL_-SDFPQX23_P4**
CP to Q ↓	0.0864	0.0894	0.9667	0.7280
CP to Q ↑	0.1094	0.1124	1.4564	1.4422
	C8T28SOIDV_LL_-SDFPQX29_P4		**C8T28SOIDV_LL_-SDFPQX29_P4**	
CP to Q ↓	0.0847		0.6505	
CP to Q ↑	0.1039		0.9660	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P4	C8T28SOI_-LLHF_-SDFPQX3_P4	C8T28SOIDV_-LL_SDFPQX5_-P4	C8T28SOIDV_-LL_SDFPQX10_-P4
CP ↓	min_pulse_width to CP	0.1071	0.1042	0.0903	0.0903
CP ↑	min_pulse_width to CP	0.0500	0.0410	0.0486	0.0439
D ↓	hold_rising to CP	-0.0484	-0.1039	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0110	-0.0089	0.0010	-0.0017
D ↓	setup_rising to CP	0.0879	0.1537	0.0564	0.0564
D ↑	setup_rising to CP	0.0418	0.0444	0.0266	0.0266
TE ↓	hold_rising to CP	-0.0337	-0.0354	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0088	-0.0121	-0.0088	-0.0120
TE ↓	setup_rising to CP	0.0857	0.1213	0.0517	0.0517
TE ↑	setup_rising to CP	0.1079	0.1470	0.1079	0.1079

TI ↓	hold_rising to CP	-0.0684	-0.1009	-0.0586	-0.0586
TI ↑	hold_rising to CP	-0.0098	-0.0093	-0.0156	-0.0156
TI ↓	setup_rising to CP	0.1078	0.1411	0.1029	0.1029
TI ↑	setup_rising to CP	0.0404	0.0348	0.0404	0.0404
		C8T28SOIDV_-LL_SDFPQX19_-P4	C8T28SOIDV_-LL_SDFPQX23_-P4	C8T28SOIDV_-LL_SDFPQX29_-P4	
CP ↓	min_pulse_width to CP	0.0903	0.0903	0.0926	
CP ↑	min_pulse_width to CP	0.0439	0.0453	0.0453	
D ↓	hold_rising to CP	-0.0094	-0.0094	-0.0126	
D ↑	hold_rising to CP	-0.0017	0.0010	0.0009	
D ↓	setup_rising to CP	0.0564	0.0564	0.0564	
D ↑	setup_rising to CP	0.0266	0.0266	0.0266	
TE ↓	hold_rising to CP	-0.0072	-0.0072	-0.0072	
TE ↑	hold_rising to CP	-0.0088	-0.0088	-0.0088	
TE ↓	setup_rising to CP	0.0517	0.0517	0.0544	
TE ↑	setup_rising to CP	0.1079	0.1079	0.1079	
TI ↓	hold_rising to CP	-0.0586	-0.0586	-0.0586	
TI ↑	hold_rising to CP	-0.0156	-0.0156	-0.0156	
TI ↓	setup_rising to CP	0.1029	0.1029	0.1045	
TI ↑	setup_rising to CP	0.0404	0.0404	0.0404	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P4	6.068e-05	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P4	5.416e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P4	5.721e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P4	7.878e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P4	9.765e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P4	1.056e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P4	1.275e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P4	C8T28SOI_LLHF_-SDFPQX3_P4	C8T28SOIDV_LL_-SDFPQX5_P4	C8T28SOIDV_LL_-SDFPQX10_P4
Clock 100Mhz Data 0Mhz	5.764e-03	5.559e-03	5.307e-03	5.178e-03
Clock 100Mhz Data 25Mhz	5.567e-03	5.366e-03	5.206e-03	5.427e-03
Clock 100Mhz Data 50Mhz	5.370e-03	5.173e-03	5.104e-03	5.677e-03

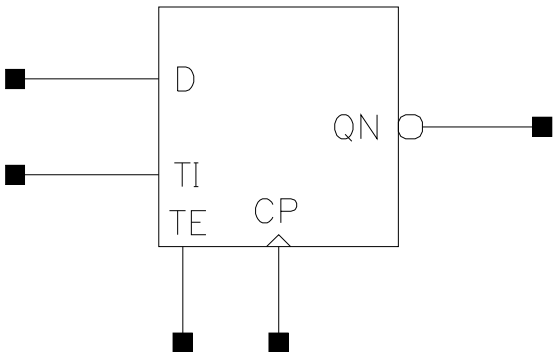
Clock = 0 Data 100Mhz	2.806e-03	2.941e-03	2.762e-03	2.670e-03
Clock = 1 Data 100Mhz	2.504e-05	3.720e-04	2.572e-04	1.998e-04
	C8T28SOIDV_LL_-SDFPQX19_P4	C8T28SOIDV_LL_-SDFPQX23_P4	C8T28SOIDV_LL_-SDFPQX29_P4	
Clock 100Mhz Data 0Mhz	5.102e-03	5.053e-03	5.018e-03	
Clock 100Mhz Data 25Mhz	5.819e-03	5.846e-03	6.233e-03	
Clock 100Mhz Data 50Mhz	6.536e-03	6.640e-03	7.449e-03	
Clock = 0 Data 100Mhz	2.614e-03	2.576e-03	2.551e-03	
Clock = 1 Data 100Mhz	1.654e-04	1.425e-04	1.261e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P4	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P4	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P4	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P4	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P4	C8T28SOI_LLHF_-SDFPQNX3_P4	C8T28SOIDV_LL_-SDFPQNX5_P4	C8T28SOIDV_LL_-SDFPQNX10_P4

CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P4	C8T28SOIDV_LL_-SDFPQNX29_P4		
CP	0.0004	0.0004		
D	0.0004	0.0004		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P4	**C8T28SOI_LLHF_-SDFPQNX3_P4**	**C8T28SOI_LL_-SDFPQNX5_P4**	**C8T28SOI_LLHF_-SDFPQNX3_P4**
CP to QN ↓	0.0800	0.0861	3.9091	5.9979
CP to QN ↑	0.0712	0.0675	6.3001	8.7199
	C8T28SOIDV_LL_-SDFPQNX5_P4	**C8T28SOIDV_LL_-SDFPQNX10_P4**	**C8T28SOIDV_LL_-SDFPQNX5_P4**	**C8T28SOIDV_LL_-SDFPQNX10_P4**
CP to QN ↓	0.0886	0.0829	3.7636	1.8819
CP to QN ↑	0.0647	0.0692	5.6970	2.8848
	C8T28SOIDV_LL_-SDFPQNX19_P4	**C8T28SOIDV_LL_-SDFPQNX29_P4**	**C8T28SOIDV_LL_-SDFPQNX19_P4**	**C8T28SOIDV_LL_-SDFPQNX29_P4**
CP to QN ↓	0.0931	0.1084	0.9751	0.6480
CP to QN ↑	0.0818	0.0921	1.4734	0.9684

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P4	C8T28SOI_-LLHF_-SDFPQNX3_P4	C8T28SOIDV_-LL_SDFPQNX5_-P4	C8T28SOIDV_-LL_-SDFPQNX10_P4
CP ↓	min_pulse_width to CP	0.1071	0.1029	0.0909	0.0903
CP ↑	min_pulse_width to CP	0.0440	0.0409	0.0439	0.0453
D ↓	hold_rising to CP	-0.0484	-0.1039	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0110	-0.0116	-0.0017	0.0010
D ↓	setup_rising to CP	0.0879	0.1478	0.0564	0.0564
D ↑	setup_rising to CP	0.0418	0.0444	0.0298	0.0266
TE ↓	hold_rising to CP	-0.0337	-0.0350	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0120	-0.0121	-0.0098	-0.0088
TE ↓	setup_rising to CP	0.0857	0.1219	0.0516	0.0517
TE ↑	setup_rising to CP	0.1079	0.1444	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0684	-0.1016	-0.0586	-0.0586
TI ↑	hold_rising to CP	-0.0098	-0.0093	-0.0105	-0.0156
TI ↓	setup_rising to CP	0.1078	0.1396	0.1029	0.1029
TI ↑	setup_rising to CP	0.0404	0.0348	0.0348	0.0404

		C8T28SOIDV_-LL_-SDFPQNX19_P4	C8T28SOIDV_-LL_-SDFPQNX29_P4		
CP ↓	min_pulse_width to CP	0.0903	0.0903		
CP ↑	min_pulse_width to CP	0.0532	0.0439		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	0.0010	-0.0017		
D ↓	setup_rising to CP	0.0564	0.0564		
D ↑	setup_rising to CP	0.0266	0.0266		
TE ↓	hold_rising to CP	-0.0072	-0.0072		
TE ↑	hold_rising to CP	-0.0088	-0.0088		
TE ↓	setup_rising to CP	0.0517	0.0517		
TE ↑	setup_rising to CP	0.1079	0.1079		
TI ↓	hold_rising to CP	-0.0586	-0.0586		
TI ↑	hold_rising to CP	-0.0098	-0.0156		
TI ↓	setup_rising to CP	0.1029	0.1029		
TI ↑	setup_rising to CP	0.0404	0.0404		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P4	6.009e-05	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P4	5.503e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P4	5.766e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P4	7.719e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P4	9.787e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P4	1.482e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P4	C8T28SOI_LLHF_-SDFPQNX3_P4	C8T28SOIDV_LL_-SDFPQNX5_P4	C8T28SOIDV_LL_-SDFPQNX10_P4
Clock 100Mhz Data 0Mhz	5.764e-03	5.622e-03	5.354e-03	5.211e-03
Clock 100Mhz Data 25Mhz	5.521e-03	5.428e-03	5.176e-03	5.409e-03
Clock 100Mhz Data 50Mhz	5.277e-03	5.234e-03	4.999e-03	5.606e-03
Clock = 0 Data 100Mhz	2.807e-03	2.953e-03	2.774e-03	2.680e-03
Clock = 1 Data 100Mhz	2.510e-05	3.744e-04	2.588e-04	2.010e-04
	C8T28SOIDV_LL_-SDFPQNX19_P4	C8T28SOIDV_LL_-SDFPQNX29_P4		
Clock 100Mhz Data 0Mhz	5.129e-03	5.072e-03		

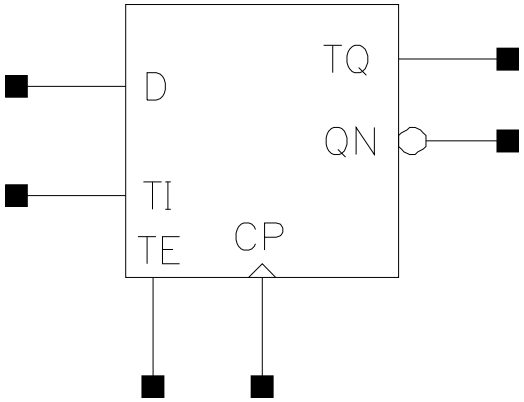
Clock 100Mhz Data 25Mhz	5.911e-03	6.623e-03		
Clock 100Mhz Data 50Mhz	6.693e-03	8.174e-03		
Clock = 0 Data 100Mhz	2.620e-03	2.584e-03		
Clock = 1 Data 100Mhz	1.664e-04	1.433e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P4	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P4	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P4	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P4	C8T28SOI_LLHF_-SDFPQNTX3_P4	C8T28SOIDV_LL_-SDFPQNTX5_P4	C8T28SOIDV_LL_-SDFPQNTX10_P4
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P4	C8T28SOIDV_LL_-SDFPQNTX29_P4		
CP	0.0004	0.0004		
D	0.0004	0.0004		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNTX5_P4	**C8T28SOI_LLHF_-SDFPQNTX3_P4**	**C8T28SOI_LL_-SDFPQNTX5_P4**	**C8T28SOI_LLHF_-SDFPQNTX3_P4**
CP to QN ↓	0.0904	0.0942	4.0441	6.1142
CP to QN ↑	0.0903	0.0831	6.3271	8.7340
CP to TQ ↓	0.0750	0.0578	11.0166	7.1668
CP to TQ ↑	0.0773	0.0705	30.1603	15.9836
	C8T28SOIDV_LL_-SDFPQNTX5_P4	**C8T28SOIDV_LL_-SDFPQNTX10_P4**	**C8T28SOIDV_LL_-SDFPQNTX5_P4**	**C8T28SOIDV_LL_-SDFPQNTX10_P4**
CP to QN ↓	0.0954	0.0920	3.7163	1.8973
CP to QN ↑	0.0760	0.0759	5.7016	2.8899
CP to TQ ↓	0.0529	0.0552	7.1920	7.4568
CP to TQ ↑	0.0717	0.0734	12.5590	13.0392
	C8T28SOIDV_LL_-SDFPQNTX19_P4	**C8T28SOIDV_LL_-SDFPQNTX29_P4**	**C8T28SOIDV_LL_-SDFPQNTX19_P4**	**C8T28SOIDV_LL_-SDFPQNTX29_P4**
CP to QN ↓	0.0946	0.1109	0.9725	0.6510
CP to QN ↑	0.0823	0.0976	1.4643	0.9679
CP to TQ ↓	0.0575	0.0556	7.3448	7.5226
CP to TQ ↑	0.0758	0.0768	13.4349	17.1672

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_P4	C8T28SOI_-LLHF_-SDFPQNTX3_P4	C8T28SOIDV_-LL_-SDFPQNTX5_P4	C8T28SOIDV_-LL_-SDFPQNTX10_-P4
CP ↓	min_pulse_width to CP	0.1071	0.1036	0.0909	0.0903
CP ↑	min_pulse_width to CP	0.0547	0.0502	0.0486	0.0485
D ↓	hold_rising to CP	-0.0484	-0.1043	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0110	-0.0116	-0.0017	0.0010
D ↓	setup_rising to CP	0.0879	0.1484	0.0564	0.0564

D ↑	setup_rising to CP	0.0418	0.0440	0.0298	0.0266
TE ↓	hold_rising to CP	-0.0337	-0.0350	-0.0072	-0.0077
TE ↑	hold_rising to CP	-0.0088	-0.0121	-0.0098	-0.0088
TE ↓	setup_rising to CP	0.0857	0.1219	0.0549	0.0517
TE ↑	setup_rising to CP	0.1079	0.1448	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0684	-0.1000	-0.0586	-0.0593
TI ↑	hold_rising to CP	-0.0098	-0.0093	-0.0105	-0.0156
TI ↓	setup_rising to CP	0.1078	0.1396	0.1029	0.1029
TI ↑	setup_rising to CP	0.0404	0.0391	0.0348	0.0404
		C8T28SOIDV_-LL_-SDFPQNTX19_-P4	C8T28SOIDV_-LL_-SDFPQNTX29_-P4		
CP ↓	min_pulse_width to CP	0.0903	0.0903		
CP ↑	min_pulse_width to CP	0.0533	0.0486		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	0.0010	0.0010		
D ↓	setup_rising to CP	0.0564	0.0564		
D ↑	setup_rising to CP	0.0266	0.0266		
TE ↓	hold_rising to CP	-0.0077	-0.0077		
TE ↑	hold_rising to CP	-0.0088	-0.0088		
TE ↓	setup_rising to CP	0.0517	0.0517		
TE ↑	setup_rising to CP	0.1079	0.1079		
TI ↓	hold_rising to CP	-0.0593	-0.0586		
TI ↑	hold_rising to CP	-0.0141	-0.0156		
TI ↓	setup_rising to CP	0.1029	0.1029		
TI ↑	setup_rising to CP	0.0404	0.0404		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P4	6.008e-05	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P4	5.881e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P4	6.168e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P4	7.335e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P4	9.704e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P4	1.494e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

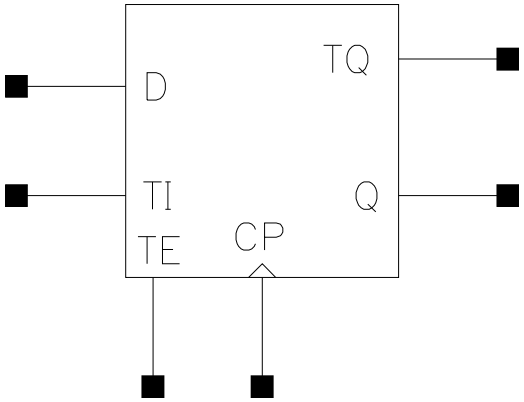
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P4	C8T28SOI_LLHF_-SDFPQNTX3_P4	C8T28SOIDV_LL_-SDFPQNTX5_P4	C8T28SOIDV_LL_-SDFPQNTX10_P4
Clock 100Mhz Data 0Mhz	5.768e-03	5.623e-03	5.353e-03	5.210e-03
Clock 100Mhz Data 25Mhz	5.748e-03	5.603e-03	5.346e-03	5.407e-03
Clock 100Mhz Data 50Mhz	5.728e-03	5.584e-03	5.339e-03	5.604e-03
Clock = 0 Data 100Mhz	2.807e-03	2.953e-03	2.775e-03	2.681e-03
Clock = 1 Data 100Mhz	2.505e-05	3.765e-04	2.602e-04	2.021e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P4	C8T28SOIDV_LL_-SDFPQNTX29_P4		
Clock 100Mhz Data 0Mhz	5.126e-03	5.067e-03		
Clock 100Mhz Data 25Mhz	5.854e-03	6.746e-03		
Clock 100Mhz Data 50Mhz	6.582e-03	8.425e-03		
Clock = 0 Data 100Mhz	2.624e-03	2.587e-03		
Clock = 1 Data 100Mhz	1.672e-04	1.440e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P4	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P4	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P4	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P4	C8T28SOI_LLHF_-SDFPQTX3_P4	C8T28SOIDV_LL_-SDFPQTX5_P4	C8T28SOIDV_LL_-SDFPQTX10_P4
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0004
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P4	C8T28SOIDV_LL_-SDFPQTX29_P4		
CP	0.0004	0.0004		
D	0.0004	0.0004		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQTX5_P4	**C8T28SOI_LLHF_-SDFPQTX3_P4**	**C8T28SOI_LL_-SDFPQTX5_P4**	**C8T28SOI_LLHF_-SDFPQTX3_P4**
CP to Q ↓	0.0759	0.0702	4.2756	6.5622
CP to Q ↑	0.0659	0.0712	5.8586	9.0266
CP to TQ ↓	0.0912	0.0683	12.0087	7.3512
CP to TQ ↑	0.0853	0.0759	30.5703	16.1780
	C8T28SOIDV_LL_-SDFPQTX5_P4	**C8T28SOIDV_LL_-SDFPQTX10_P4**	**C8T28SOIDV_LL_-SDFPQTX5_P4**	**C8T28SOIDV_LL_-SDFPQTX10_P4**
CP to Q ↓	0.0612	0.0817	3.9268	1.8729
CP to Q ↑	0.0739	0.1051	5.8208	2.8850
CP to TQ ↓	0.0606	0.0843	7.3677	7.5682
CP to TQ ↑	0.0766	0.1096	13.7764	13.5776
	C8T28SOIDV_LL_-SDFPQTX19_P4	**C8T28SOIDV_LL_-SDFPQTX29_P4**	**C8T28SOIDV_LL_-SDFPQTX19_P4**	**C8T28SOIDV_LL_-SDFPQTX29_P4**
CP to Q ↓	0.0883	0.0957	0.9694	0.6336
CP to Q ↑	0.1102	0.1084	1.4610	0.9636
CP to TQ ↓	0.0923	0.0592	7.6232	7.7657
CP to TQ ↑	0.1171	0.0786	13.6096	17.1820

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P4	C8T28SOI_-LLHF_-SDFPQTX3_P4	C8T28SOIDV_-LL_SDFPQTX5_-P4	C8T28SOIDV_-LL_-SDFPQTX10_P4
CP ↓	min_pulse_width to CP	0.1071	0.1029	0.0909	0.0903
CP ↑	min_pulse_width to CP	0.0642	0.0549	0.0499	0.0439
D ↓	hold_rising to CP	-0.0484	-0.1043	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0110	-0.0116	0.0010	-0.0017
D ↓	setup_rising to CP	0.0911	0.1484	0.0564	0.0564

D ↑	setup_rising to CP	0.0418	0.0444	0.0266	0.0266
TE ↓	hold_rising to CP	-0.0337	-0.0350	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0088	-0.0121	-0.0088	-0.0088
TE ↓	setup_rising to CP	0.0857	0.1219	0.0517	0.0517
TE ↑	setup_rising to CP	0.1079	0.1444	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0684	-0.1016	-0.0586	-0.0586
TI ↑	hold_rising to CP	-0.0098	-0.0093	-0.0156	-0.0156
TI ↓	setup_rising to CP	0.1078	0.1396	0.1029	0.1029
TI ↑	setup_rising to CP	0.0404	0.0348	0.0404	0.0404
		C8T28SOIDV_-LL_-SDFPQTX19_P4	C8T28SOIDV_-LL_-SDFPQTX29_P4		
CP ↓	min_pulse_width to CP	0.0903	0.0926		
CP ↑	min_pulse_width to CP	0.0439	0.0533		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	-0.0017	0.0004		
D ↓	setup_rising to CP	0.0564	0.0564		
D ↑	setup_rising to CP	0.0266	0.0266		
TE ↓	hold_rising to CP	-0.0072	-0.0072		
TE ↑	hold_rising to CP	-0.0120	-0.0088		
TE ↓	setup_rising to CP	0.0517	0.0517		
TE ↑	setup_rising to CP	0.1079	0.1079		
TI ↓	hold_rising to CP	-0.0586	-0.0586		
TI ↑	hold_rising to CP	-0.0156	-0.0156		
TI ↓	setup_rising to CP	0.1029	0.1045		
TI ↑	setup_rising to CP	0.0404	0.0404		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P4	6.118e-05	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P4	5.881e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P4	6.138e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P4	8.271e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P4	1.029e-04	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P4	1.349e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

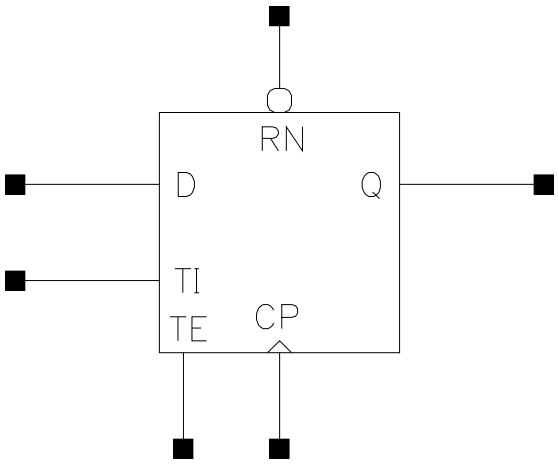
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P4	C8T28SOI_LLHF_-SDFPQTX3_P4	C8T28SOIDV_LL_-SDFPQTX5_P4	C8T28SOIDV_LL_-SDFPQTX10_P4
Clock 100Mhz Data 0Mhz	5.768e-03	5.627e-03	5.354e-03	5.213e-03
Clock 100Mhz Data 25Mhz	5.780e-03	5.614e-03	5.372e-03	5.574e-03
Clock 100Mhz Data 50Mhz	5.792e-03	5.601e-03	5.390e-03	5.936e-03
Clock = 0 Data 100Mhz	2.813e-03	2.958e-03	2.774e-03	2.679e-03
Clock = 1 Data 100Mhz	2.518e-05	3.756e-04	2.596e-04	2.017e-04
	C8T28SOIDV_LL_-SDFPQTX19_P4	C8T28SOIDV_LL_-SDFPQTX29_P4		
Clock 100Mhz Data 0Mhz	5.130e-03	5.079e-03		
Clock 100Mhz Data 25Mhz	5.986e-03	6.436e-03		
Clock 100Mhz Data 50Mhz	6.843e-03	7.792e-03		
Clock = 0 Data 100Mhz	2.621e-03	2.586e-03		
Clock = 1 Data 100Mhz	1.670e-04	1.439e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P4	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P4	C8T28SOI_LLHF_-SDFPRQX3_P4	C8T28SOIDV_LL_-SDFPRQX5_P4	C8T28SOIDV_LL_-SDFPRQX10_P4
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0005	0.0004	0.0004
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P4	C8T28SOIDV_LL_-SDFPRQX29_P4		
CP	0.0004	0.0004		
D	0.0004	0.0004		
RN	0.0008	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P4	**C8T28SOI_LLHF_-SDFPRQX3_P4**	**C8T28SOI_LL_-SDFPRQX5_P4**	**C8T28SOI_LLHF_-SDFPRQX3_P4**
CP to Q ↓	0.0743	0.0672	4.0935	6.4047
CP to Q ↑	0.0635	0.0712	5.8199	8.8445
RN to Q ↓	0.0655	0.0642	3.8024	6.0324
	C8T28SOIDV_LL_-SDFPRQX5_P4	**C8T28SOIDV_LL_-SDFPRQX10_P4**	**C8T28SOIDV_LL_-SDFPRQX5_P4**	**C8T28SOIDV_LL_-SDFPRQX10_P4**
CP to Q ↓	0.0571	0.0817	3.8272	1.8862
CP to Q ↑	0.0749	0.1077	5.7558	2.8884
RN to Q ↓	0.0534	0.0831	3.7988	1.8860
	C8T28SOIDV_LL_-SDFPRQX19_P4	**C8T28SOIDV_LL_-SDFPRQX29_P4**	**C8T28SOIDV_LL_-SDFPRQX19_P4**	**C8T28SOIDV_LL_-SDFPRQX29_P4**
CP to Q ↓	0.0872	0.0884	0.9689	0.6602
CP to Q ↑	0.1128	0.1169	1.4726	0.9990
RN to Q ↓	0.0890	0.0902	0.9680	0.6599

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P4	C8T28SOI_-LLHF_-SDFPRQX3_P4	C8T28SOIDV_-LL_SDFPRQX5_-P4	C8T28SOIDV_-LL_-SDFPRQX10_P4
CP ↓	min_pulse_width to CP	0.1071	0.0994	0.0933	0.0933
CP ↑	min_pulse_width to CP	0.0595	0.0502	0.0452	0.0453
D ↓	hold_rising to CP	-0.0484	-0.0990	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0142	-0.0143	-0.0049	-0.0049
D ↓	setup_rising to CP	0.0911	0.1488	0.0564	0.0564
D ↑	setup_rising to CP	0.0440	0.0461	0.0294	0.0294
RN ↓	min_pulse_width to RN	0.0713	0.0691	0.0637	0.0588
RN ↑	recovery_rising to CP	0.0054	0.0005	0.0005	0.0005
RN ↑	removal_rising to CP	0.0091	0.0091	0.0091	0.0091

TE ↓	hold_rising to CP	-0.0333	-0.0382	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0147	-0.0116	-0.0147	-0.0147
TE ↓	setup_rising to CP	0.0857	0.1165	0.0545	0.0545
TE ↑	setup_rising to CP	0.1079	0.1421	0.1089	0.1089
TI ↓	hold_rising to CP	-0.0668	-0.1003	-0.0550	-0.0550
TI ↑	hold_rising to CP	-0.0141	-0.0099	-0.0154	-0.0154
TI ↓	setup_rising to CP	0.1078	0.1363	0.1029	0.1029
TI ↑	setup_rising to CP	0.0453	0.0388	0.0453	0.0453
		C8T28SOIDV_-LL_-SDFPRQX19_P4	C8T28SOIDV_-LL_-SDFPRQX29_P4		
CP ↓	min_pulse_width to CP	0.0933	0.0933		
CP ↑	min_pulse_width to CP	0.0453	0.0453		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	-0.0049	-0.0049		
D ↓	setup_rising to CP	0.0564	0.0564		
D ↑	setup_rising to CP	0.0294	0.0294		
RN ↓	min_pulse_width to RN	0.0588	0.0588		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0072	-0.0072		
TE ↑	hold_rising to CP	-0.0147	-0.0147		
TE ↓	setup_rising to CP	0.0545	0.0566		
TE ↑	setup_rising to CP	0.1089	0.1079		
TI ↓	hold_rising to CP	-0.0550	-0.0593		
TI ↑	hold_rising to CP	-0.0154	-0.0154		
TI ↓	setup_rising to CP	0.1029	0.1029		
TI ↑	setup_rising to CP	0.0453	0.0453		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P4	6.405e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P4	5.887e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P4	6.097e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P4	8.098e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX19_P4	1.018e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P4	1.290e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

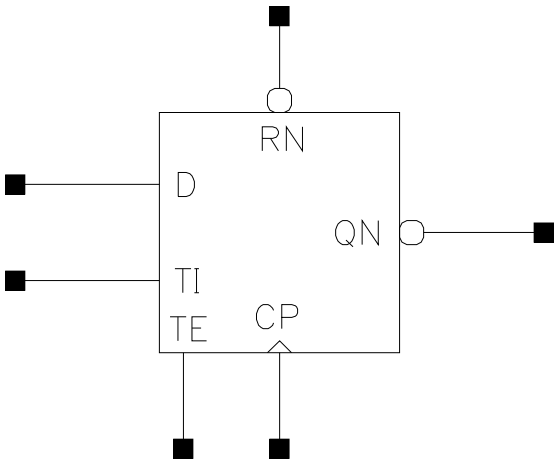
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P4	C8T28SOI_LLHF_-SDFPRQX3_P4	C8T28SOIDV_LL_-SDFPRQX5_P4	C8T28SOIDV_LL_-SDFPRQX10_P4
Clock 100Mhz Data 0Mhz	6.009e-03	5.801e-03	5.514e-03	5.370e-03
Clock 100Mhz Data 25Mhz	5.789e-03	5.614e-03	5.343e-03	5.593e-03
Clock 100Mhz Data 50Mhz	5.569e-03	5.427e-03	5.172e-03	5.815e-03
Clock = 0 Data 100Mhz	2.669e-03	2.839e-03	2.715e-03	2.653e-03
Clock = 1 Data 100Mhz	2.478e-05	3.779e-04	2.608e-04	2.022e-04
	C8T28SOIDV_LL_-SDFPRQX19_P4	C8T28SOIDV_LL_-SDFPRQX29_P4		
Clock 100Mhz Data 0Mhz	5.284e-03	5.227e-03		
Clock 100Mhz Data 25Mhz	5.969e-03	6.504e-03		
Clock 100Mhz Data 50Mhz	6.654e-03	7.781e-03		
Clock = 0 Data 100Mhz	2.616e-03	2.593e-03		
Clock = 1 Data 100Mhz	1.671e-04	1.438e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P4	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P4	C8T28SOI_LLHF_-SDFPRQNX3_P4	C8T28SOIDV_LL_-SDFPRQNX5_P4	C8T28SOIDV_LL_-SDFPRQNX10_P4
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0005	0.0004	0.0004
RN	0.0007	0.0007	0.0008	0.0008
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P4	C8T28SOIDV_LL_-SDFPRQNX29_P4		
CP	0.0004	0.0004		
D	0.0004	0.0004		
RN	0.0007	0.0007		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNX5_P4	**C8T28SOI_LLHF_-SDFPRQNX3_P4**	**C8T28SOI_LL_-SDFPRQNX5_P4**	**C8T28SOI_LLHF_-SDFPRQNX3_P4**
CP to QN ↓	0.0845	0.0902	4.0220	6.0209
CP to QN ↑	0.0792	0.0742	6.0170	8.7215
RN to QN ↑	0.0773	0.0758	6.0112	8.6926
	C8T28SOIDV_LL_-SDFPRQNX5_P4	**C8T28SOIDV_LL_-SDFPRQNX10_P4**	**C8T28SOIDV_LL_-SDFPRQNX5_P4**	**C8T28SOIDV_LL_-SDFPRQNX10_P4**
CP to QN ↓	0.0965	0.0866	3.7044	1.8872
CP to QN ↑	0.0725	0.0701	5.6823	2.8877
RN to QN ↑	0.0729	0.0665	5.6827	2.8867
	C8T28SOIDV_LL_-SDFPRQNX19_P4	**C8T28SOIDV_LL_-SDFPRQNX29_P4**	**C8T28SOIDV_LL_-SDFPRQNX19_P4**	**C8T28SOIDV_LL_-SDFPRQNX29_P4**
CP to QN ↓	0.0963	0.1032	0.9918	0.6650
CP to QN ↑	0.0775	0.0871	1.4781	0.9938
RN to QN ↑	0.0718	0.0835	1.4786	0.9943

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P4	C8T28SOI_-LLHF_-SDFPRQNX3_-P4	C8T28SOIDV_-LL_-SDFPRQNX5_-P4	C8T28SOIDV_-LL_-SDFPRQNX10_-P4
CP ↓	min_pulse_width to CP	0.1071	0.1012	0.0933	0.0933
CP ↑	min_pulse_width to CP	0.0487	0.0456	0.0453	0.0452
D ↓	hold_rising to CP	-0.0484	-0.0990	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0142	-0.0143	-0.0049	-0.0049
D ↓	setup_rising to CP	0.0879	0.1456	0.0564	0.0564
D ↑	setup_rising to CP	0.0440	0.0461	0.0294	0.0294
RN ↓	min_pulse_width to RN	0.0713	0.0691	0.0588	0.0659
RN ↑	recovery_rising to CP	0.0054	0.0005	0.0005	0.0005

RN ↑	removal_rising to CP	0.0091	0.0095	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0333	-0.0382	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0147	-0.0111	-0.0147	-0.0147
TE ↓	setup_rising to CP	0.0857	0.1170	0.0544	0.0545
TE ↑	setup_rising to CP	0.1079	0.1421	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0668	-0.0960	-0.0550	-0.0550
TI ↑	hold_rising to CP	-0.0141	-0.0099	-0.0154	-0.0154
TI ↓	setup_rising to CP	0.1078	0.1363	0.1029	0.1029
TI ↑	setup_rising to CP	0.0394	0.0397	0.0453	0.0453
		C8T28SOIDV_-LL_-SDFPRQNX19_-P4	C8T28SOIDV_-LL_-SDFPRQNX29_-P4		
CP ↓	min_pulse_width to CP	0.0950	0.0950		
CP ↑	min_pulse_width to CP	0.0500	0.0579		
D ↓	hold_rising to CP	-0.0072	-0.0072		
D ↑	hold_rising to CP	-0.0017	-0.0017		
D ↓	setup_rising to CP	0.0564	0.0564		
D ↑	setup_rising to CP	0.0294	0.0294		
RN ↓	min_pulse_width to RN	0.0659	0.0828		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0147	-0.0147		
TE ↓	setup_rising to CP	0.0545	0.0539		
TE ↑	setup_rising to CP	0.1089	0.1089		
TI ↓	hold_rising to CP	-0.0537	-0.0537		
TI ↑	hold_rising to CP	-0.0154	-0.0154		
TI ↓	setup_rising to CP	0.1029	0.1029		
TI ↑	setup_rising to CP	0.0453	0.0453		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P4	6.386e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P4	6.003e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P4	6.138e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P4	8.071e-05	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P4	9.721e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P4	1.253e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

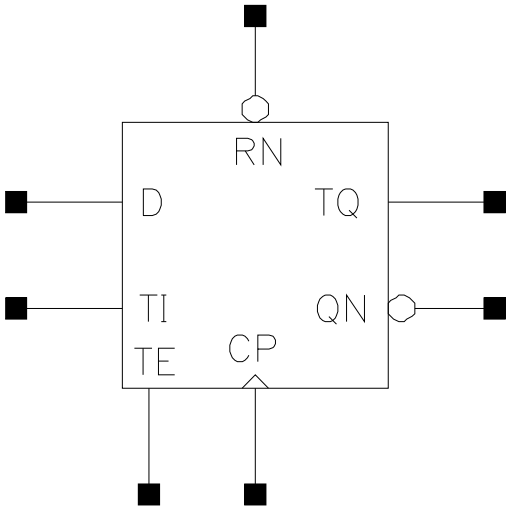
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P4	C8T28SOI_LLHF_-SDFPRQNX3_P4	C8T28SOIDV_LL_-SDFPRQNX5_P4	C8T28SOIDV_LL_-SDFPRQNX10_P4
Clock 100Mhz Data 0Mhz	6.003e-03	5.784e-03	5.503e-03	5.363e-03
Clock 100Mhz Data 25Mhz	5.727e-03	5.576e-03	5.363e-03	5.577e-03
Clock 100Mhz Data 50Mhz	5.451e-03	5.367e-03	5.223e-03	5.791e-03
Clock = 0 Data 100Mhz	2.666e-03	2.835e-03	2.715e-03	2.653e-03
Clock = 1 Data 100Mhz	2.481e-05	3.779e-04	2.607e-04	2.022e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P4	C8T28SOIDV_LL_-SDFPRQNX29_P4		
Clock 100Mhz Data 0Mhz	5.319e-03	5.310e-03		
Clock 100Mhz Data 25Mhz	6.009e-03	6.710e-03		
Clock 100Mhz Data 50Mhz	6.698e-03	8.111e-03		
Clock = 0 Data 100Mhz	2.615e-03	2.589e-03		
Clock = 1 Data 100Mhz	1.670e-04	1.437e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P4	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P4	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P4	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P4	C8T28SOI_LLHF_-SDFPRQNTX3_P4	C8T28SOIDV_LL_-SDFPRQNTX5_P4	C8T28SOIDV_LL_-SDFPRQNTX10_P4
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0005	0.0004	0.0004
RN	0.0007	0.0007	0.0008	0.0008
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P4	C8T28SOIDV_LL_-SDFPRQNTX29_P4		
CP	0.0004	0.0004		
D	0.0004	0.0004		
RN	0.0007	0.0007		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNTX5_P4	**C8T28SOI_LLHF_-SDFPRQNTX3_P4**	**C8T28SOI_LL_-SDFPRQNTX5_P4**	**C8T28SOI_LLHF_-SDFPRQNTX3_P4**
CP to QN ↓	0.0936	0.0984	3.9305	6.1027
CP to QN ↑	0.0984	0.0904	6.3300	8.7281
CP to TQ ↓	0.0837	0.0647	11.5321	7.2266
CP to TQ ↑	0.0788	0.0742	30.1536	16.0090
RN to QN ↑	0.0848	0.0820	6.3268	8.7716
RN to TQ ↓	0.0727	0.0634	11.2016	6.9382
	C8T28SOIDV_LL_-SDFPRQNTX5_P4	**C8T28SOIDV_LL_-SDFPRQNTX10_P4**	**C8T28SOIDV_LL_-SDFPRQNTX5_P4**	**C8T28SOIDV_LL_-SDFPRQNTX10_P4**
CP to QN ↓	0.1016	0.1073	3.7520	1.9482
CP to QN ↑	0.0790	0.0834	5.6804	2.8859
CP to TQ ↓	0.0543	0.0552	7.2037	7.2587
CP to TQ ↑	0.0760	0.0760	12.5648	12.5696
RN to QN ↑	0.0752	0.0802	5.6840	2.8802
RN to TQ ↓	0.0490	0.0503	7.2141	7.2774
	C8T28SOIDV_LL_-SDFPRQNTX19_P4	**C8T28SOIDV_LL_-SDFPRQNTX29_P4**	**C8T28SOIDV_LL_-SDFPRQNTX19_P4**	**C8T28SOIDV_LL_-SDFPRQNTX29_P4**
CP to QN ↓	0.1011	0.1029	0.9804	0.6659
CP to QN ↑	0.0847	0.0941	1.4569	0.9873
CP to TQ ↓	0.0595	0.0718	7.3210	8.2789
CP to TQ ↑	0.0812	0.0902	12.5922	14.3742
RN to QN ↑	0.0788	0.0892	1.4555	0.9856
RN to TQ ↓	0.0522	0.0656	7.3072	8.1712

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P4	C8T28SOI_-LLHF_-SDFPRQNTX3_-P4	C8T28SOIDV_-LL_-SDFPRQNTX5_-P4	C8T28SOIDV_-LL_SDF-PRQNTX10_P4
CP ↓	min_pulse_width to CP	0.1071	0.1012	0.0933	0.0933
CP ↑	min_pulse_width to CP	0.0642	0.0549	0.0486	0.0500
D ↓	hold_rising to CP	-0.0485	-0.0990	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0142	-0.0143	-0.0017	-0.0049
D ↓	setup_rising to CP	0.0879	0.1488	0.0564	0.0564
D ↑	setup_rising to CP	0.0440	0.0461	0.0294	0.0294
RN ↓	min_pulse_width to RN	0.0735	0.0713	0.0659	0.0708
RN ↑	recovery_rising to CP	0.0054	0.0005	0.0005	0.0005
RN ↑	removal_rising to CP	0.0095	0.0095	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0333	-0.0408	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0147	-0.0111	-0.0147	-0.0147
TE ↓	setup_rising to CP	0.0857	0.1170	0.0544	0.0539
TE ↑	setup_rising to CP	0.1079	0.1421	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0670	-0.0960	-0.0550	-0.0550
TI ↑	hold_rising to CP	-0.0141	-0.0099	-0.0154	-0.0154
TI ↓	setup_rising to CP	0.1078	0.1363	0.1029	0.1029
TI ↑	setup_rising to CP	0.0394	0.0397	0.0453	0.0453
		C8T28SOIDV_-LL_SDF-PRQNTX19_P4	C8T28SOIDV_-LL_SDF-PRQNTX29_P4		
CP ↓	min_pulse_width to CP	0.0950	0.0950		
CP ↑	min_pulse_width to CP	0.0532	0.0626		
D ↓	hold_rising to CP	-0.0072	-0.0072		
D ↑	hold_rising to CP	-0.0017	-0.0017		
D ↓	setup_rising to CP	0.0564	0.0591		
D ↑	setup_rising to CP	0.0294	0.0294		
RN ↓	min_pulse_width to RN	0.0708	0.0876		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0147	-0.0147		

TE ↓	setup_rising to CP	0.0566	0.0566		
TE ↑	setup_rising to CP	0.1085	0.1079		
TI ↓	hold_rising to CP	-0.0537	-0.0537		
TI ↑	hold_rising to CP	-0.0154	-0.0154		
TI ↓	setup_rising to CP	0.1029	0.1029		
TI ↑	setup_rising to CP	0.0453	0.0453		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P4	6.377e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P4	6.293e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P4	6.520e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_-P4	7.395e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_-P4	9.746e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_-P4	1.284e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

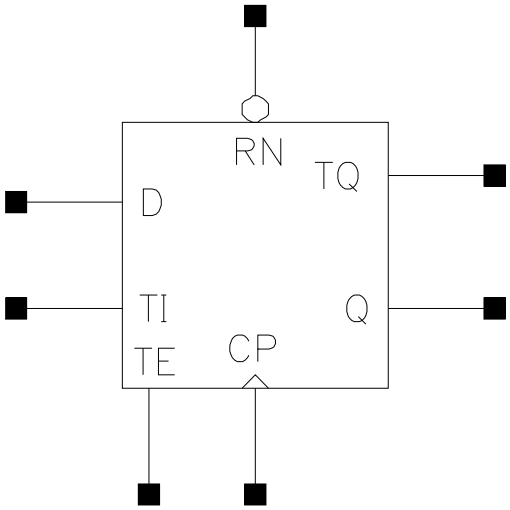
Pin Cycle	C8T28SOI_LL_-SDFPRQNTX5_P4	C8T28SOI_LLHF_-SDFPRQNTX3_P4	C8T28SOIDV_LL_-SDFPRQNTX5_P4	C8T28SOIDV_LL_-SDFPRQNTX10_P4
Clock 100Mhz Data 0Mhz	6.010e-03	5.789e-03	5.516e-03	5.372e-03
Clock 100Mhz Data 25Mhz	5.937e-03	5.754e-03	5.511e-03	5.617e-03
Clock 100Mhz Data 50Mhz	5.865e-03	5.719e-03	5.506e-03	5.862e-03
Clock = 0 Data 100Mhz	2.655e-03	2.833e-03	2.715e-03	2.654e-03
Clock = 1 Data 100Mhz	2.468e-05	3.796e-04	2.619e-04	2.031e-04
	C8T28SOIDV_LL_-SDFPRQNTX19_P4	C8T28SOIDV_LL_-SDFPRQNTX29_P4		
Clock 100Mhz Data 0Mhz	5.329e-03	5.293e-03		
Clock 100Mhz Data 25Mhz	6.027e-03	6.850e-03		
Clock 100Mhz Data 50Mhz	6.724e-03	8.407e-03		
Clock = 0 Data 100Mhz	2.617e-03	2.593e-03		
Clock = 1 Data 100Mhz	1.679e-04	1.444e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P4	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P4	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P4	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P4	C8T28SOI_LLHF_-SDFPRQTX3_P4	C8T28SOIDV_LL_-SDFPRQTX5_P4	C8T28SOIDV_LL_-SDFPRQTX10_P4
CP	0.0006	0.0006	0.0004	0.0004
D	0.0004	0.0005	0.0004	0.0004
RN	0.0007	0.0007	0.0008	0.0008
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P4	C8T28SOIDV_LL_-SDFPRQTX29_P4		
CP	0.0004	0.0004		
D	0.0004	0.0004		
RN	0.0008	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQTX5_P4	**C8T28SOI_LLHF_-SDFPRQTX3_P4**	**C8T28SOI_LL_-SDFPRQTX5_P4**	**C8T28SOI_LLHF_-SDFPRQTX3_P4**
CP to Q ↓	0.0864	0.0748	4.3424	6.5940
CP to Q ↑	0.0682	0.0742	5.8622	9.0294
CP to TQ ↓	0.1021	0.0727	12.1079	7.3924
CP to TQ ↑	0.0875	0.0787	30.1947	16.1920
RN to Q ↓	0.0691	0.0673	3.9803	6.1841
RN to TQ ↓	0.0798	0.0669	11.6733	7.0495
	C8T28SOIDV_LL_-SDFPRQTX5_P4	**C8T28SOIDV_LL_-SDFPRQTX10_P4**	**C8T28SOIDV_LL_-SDFPRQTX5_P4**	**C8T28SOIDV_LL_-SDFPRQTX10_P4**
CP to Q ↓	0.0618	0.0831	3.9358	1.9120
CP to Q ↑	0.0774	0.1089	5.7993	2.8832
CP to TQ ↓	0.0623	0.0863	7.3597	7.2270
CP to TQ ↑	0.0805	0.1136	12.7141	12.6286
RN to Q ↓	0.0587	0.0855	3.8946	1.9096
RN to TQ ↓	0.0591	0.0887	7.3097	7.2265
	C8T28SOIDV_LL_-SDFPRQTX19_P4	**C8T28SOIDV_LL_-SDFPRQTX29_P4**	**C8T28SOIDV_LL_-SDFPRQTX19_P4**	**C8T28SOIDV_LL_-SDFPRQTX29_P4**
CP to Q ↓	0.0929	0.0890	1.0017	0.6710
CP to Q ↑	0.1163	0.1169	1.4623	0.9937
CP to TQ ↓	0.0973	0.0916	7.2954	7.1366
CP to TQ ↑	0.1230	0.1230	12.6218	12.9604
RN to Q ↓	0.0941	0.0908	1.0036	0.6716
RN to TQ ↓	0.0985	0.0934	7.2988	7.1372

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_P4	C8T28SOI_-LLHF_-SDFPRQTX3_P4	C8T28SOIDV_-LL_-SDFPRQTX5_P4	C8T28SOIDV_-LL_-SDFPRQTX10_-P4
CP ↓	min_pulse_width to CP	0.1071	0.1012	0.0933	0.0933
CP ↑	min_pulse_width to CP	0.0737	0.0597	0.0500	0.0453
D ↓	hold_rising to CP	-0.0485	-0.0990	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0142	-0.0143	-0.0049	-0.0049
D ↓	setup_rising to CP	0.0879	0.1488	0.0564	0.0564
D ↑	setup_rising to CP	0.0440	0.0461	0.0294	0.0294
RN ↓	min_pulse_width to RN	0.0779	0.0713	0.0686	0.0588
RN ↑	recovery_rising to CP	0.0054	0.0001	0.0005	0.0005
RN ↑	removal_rising to CP	0.0095	0.0095	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0333	-0.0408	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0147	-0.0111	-0.0147	-0.0147
TE ↓	setup_rising to CP	0.0857	0.1165	0.0545	0.0545
TE ↑	setup_rising to CP	0.1079	0.1421	0.1085	0.1089
TI ↓	hold_rising to CP	-0.0670	-0.0960	-0.0550	-0.0550
TI ↑	hold_rising to CP	-0.0141	-0.0099	-0.0154	-0.0154
TI ↓	setup_rising to CP	0.1078	0.1355	0.1029	0.1029
TI ↑	setup_rising to CP	0.0394	0.0397	0.0453	0.0453
		C8T28SOIDV_-LL_-SDFPRQTX19_-P4	C8T28SOIDV_-LL_-SDFPRQTX29_-P4		
CP ↓	min_pulse_width to CP	0.0933	0.0933		
CP ↑	min_pulse_width to CP	0.0453	0.0453		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	-0.0049	-0.0049		
D ↓	setup_rising to CP	0.0564	0.0564		
D ↑	setup_rising to CP	0.0294	0.0294		
RN ↓	min_pulse_width to RN	0.0588	0.0588		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0072	-0.0072		
TE ↑	hold_rising to CP	-0.0147	-0.0147		

TE ↓	setup_rising to CP	0.0545	0.0566		
TE ↑	setup_rising to CP	0.1089	0.1079		
TI ↓	hold_rising to CP	-0.0550	-0.0593		
TI ↑	hold_rising to CP	-0.0154	-0.0154		
TI ↓	setup_rising to CP	0.1029	0.1029		
TI ↑	setup_rising to CP	0.0453	0.0453		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P4	6.460e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P4	6.206e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P4	6.486e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P4	8.465e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P4	1.036e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P4	1.326e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

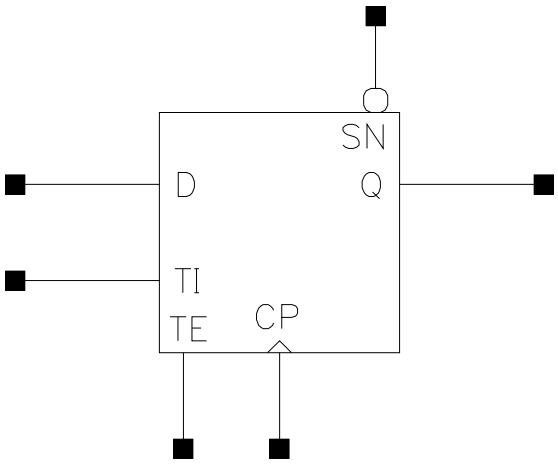
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P4	C8T28SOI_LLHF_-SDFPRQTX3_P4	C8T28SOIDV_LL_-SDFPRQTX5_P4	C8T28SOIDV_LL_-SDFPRQTX10_P4
Clock 100Mhz Data 0Mhz	6.013e-03	5.793e-03	5.510e-03	5.368e-03
Clock 100Mhz Data 25Mhz	5.999e-03	5.757e-03	5.478e-03	5.745e-03
Clock 100Mhz Data 50Mhz	5.986e-03	5.721e-03	5.446e-03	6.122e-03
Clock = 0 Data 100Mhz	2.658e-03	2.836e-03	2.714e-03	2.653e-03
Clock = 1 Data 100Mhz	2.481e-05	3.799e-04	2.621e-04	2.032e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P4	C8T28SOIDV_LL_-SDFPRQTX29_P4		
Clock 100Mhz Data 0Mhz	5.283e-03	5.226e-03		
Clock 100Mhz Data 25Mhz	6.136e-03	6.583e-03		
Clock 100Mhz Data 50Mhz	6.989e-03	7.941e-03		
Clock = 0 Data 100Mhz	2.616e-03	2.593e-03		
Clock = 1 Data 100Mhz	1.680e-04	1.445e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P4	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P4	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P4	C8T28SOI_LLHF_-SDFPSQX3_P4	C8T28SOIDV_LL_-SDFPSQX5_P4	C8T28SOIDV_LL_-SDFPSQX10_P4
CP	0.0006	0.0006	0.0004	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0012	0.0011	0.0009	0.0009
TE	0.0009	0.0009	0.0008	0.0009
TI	0.0003	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQX14_P4	C8T28SOIDV_LL_-SDFPSQX19_P4	C8T28SOIDV_LL_-SDFPSQX29_P4	
CP	0.0005	0.0005	0.0005	
D	0.0003	0.0003	0.0003	
SN	0.0009	0.0009	0.0009	
TE	0.0009	0.0009	0.0009	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P4	**C8T28SOI_LLHF_-SDFPSQX3_P4**	**C8T28SOI_LL_-SDFPSQX5_P4**	**C8T28SOI_LLHF_-SDFPSQX3_P4**
CP to Q ↓	0.0776	0.0683	4.1969	6.5102
CP to Q ↑	0.0655	0.0729	5.8639	8.8809
SN to Q ↑	0.0543	0.0494	5.7911	8.7696
	C8T28SOIDV_LL_-SDFPSQX5_P4	**C8T28SOIDV_LL_-SDFPSQX10_P4**	**C8T28SOIDV_LL_-SDFPSQX5_P4**	**C8T28SOIDV_LL_-SDFPSQX10_P4**
CP to Q ↓	0.0562	0.0831	3.8262	1.8519
CP to Q ↑	0.0712	0.1157	5.7481	2.8755
SN to Q ↑	0.0491	0.0908	5.7323	2.8775
	C8T28SOIDV_LL_-SDFPSQX14_P4	**C8T28SOIDV_LL_-SDFPSQX19_P4**	**C8T28SOIDV_LL_-SDFPSQX14_P4**	**C8T28SOIDV_LL_-SDFPSQX19_P4**
CP to Q ↓	0.0833	0.0885	1.2483	0.9535
CP to Q ↑	0.1153	0.1195	1.9276	1.4496
SN to Q ↑	0.0899	0.0941	1.9281	1.4485
	C8T28SOIDV_LL_-SDFPSQX29_P4		**C8T28SOIDV_LL_-SDFPSQX29_P4**	
CP to Q ↓	0.0881		0.6464	
CP to Q ↑	0.1247		0.9651	
SN to Q ↑	0.0995		0.9635	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P4	C8T28SOI_-LLHF_-SDFPSQX3_P4	C8T28SOIDV_-LL_SDFPSQX5_-P4	C8T28SOIDV_-LL_-SDFPSQX10_P4
CP ↓	min_pulse_width to CP	0.1165	0.1177	0.1004	0.0998
CP ↑	min_pulse_width to CP	0.0655	0.0516	0.0452	0.0454
D ↓	hold_rising to CP	-0.0533	-0.1088	-0.0192	-0.0240
D ↑	hold_rising to CP	-0.0114	-0.0089	-0.0049	-0.0045
D ↓	setup_rising to CP	0.0976	0.1657	0.0684	0.0737
D ↑	setup_rising to CP	0.0418	0.0440	0.0320	0.0320

SN ↓	min_pulse_width to SN	0.0522	0.0425	0.0452	0.0474
SN ↑	recovery_rising to CP	0.0080	0.0080	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0261	0.0359	0.0406	0.0406
TE ↓	hold_rising to CP	-0.0305	-0.0354	-0.0179	-0.0218
TE ↑	hold_rising to CP	-0.0093	-0.0062	-0.0023	-0.0098
TE ↓	setup_rising to CP	0.0955	0.1337	0.0662	0.0711
TE ↑	setup_rising to CP	0.1177	0.1594	0.1079	0.1057
TI ↓	hold_rising to CP	-0.0732	-0.1058	-0.0537	-0.0537
TI ↑	hold_rising to CP	-0.0098	-0.0093	-0.0044	-0.0105
TI ↓	setup_rising to CP	0.1176	0.1545	0.1072	0.1016
TI ↑	setup_rising to CP	0.0404	0.0391	0.0293	0.0388
		C8T28SOIDV_-LL_-SDFPSQX14_P4	C8T28SOIDV_-LL_-SDFPSQX19_P4	C8T28SOIDV_-LL_-SDFPSQX29_P4	
CP ↓	min_pulse_width to CP	0.0998	0.0998	0.0998	
CP ↑	min_pulse_width to CP	0.0454	0.0454	0.0454	
D ↓	hold_rising to CP	-0.0240	-0.0240	-0.0240	
D ↑	hold_rising to CP	-0.0045	-0.0045	-0.0045	
D ↓	setup_rising to CP	0.0737	0.0737	0.0737	
D ↑	setup_rising to CP	0.0320	0.0320	0.0320	
SN ↓	min_pulse_width to SN	0.0474	0.0474	0.0500	
SN ↑	recovery_rising to CP	-0.0044	-0.0044	-0.0012	
SN ↑	removal_rising to CP	0.0406	0.0406	0.0406	
TE ↓	hold_rising to CP	-0.0218	-0.0218	-0.0218	
TE ↑	hold_rising to CP	-0.0098	-0.0098	-0.0098	
TE ↓	setup_rising to CP	0.0711	0.0711	0.0711	
TE ↑	setup_rising to CP	0.1057	0.1057	0.1057	
TI ↓	hold_rising to CP	-0.0537	-0.0537	-0.0537	
TI ↑	hold_rising to CP	-0.0105	-0.0105	-0.0105	
TI ↓	setup_rising to CP	0.1024	0.1024	0.1016	
TI ↑	setup_rising to CP	0.0388	0.0346	0.0346	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQX5_P4	6.523e-05	1.000e-20

C8T28SOI_LLHF_SDFPSQX3_P4	6.103e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P4	6.230e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P4	8.375e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P4	9.491e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P4	1.079e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P4	1.332e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

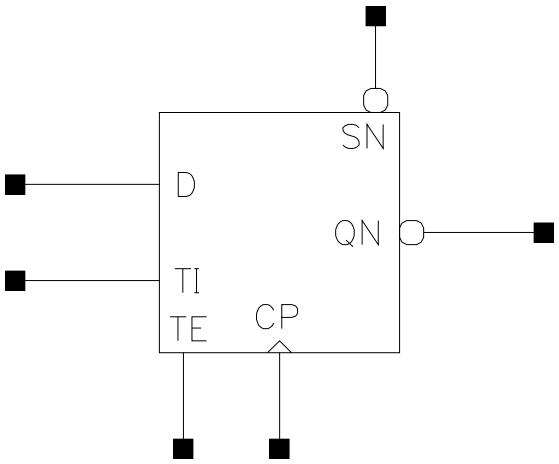
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P4	C8T28SOI_LLHF_-SDFPSQX3_P4	C8T28SOIDV_LL_-SDFPSQX5_P4	C8T28SOIDV_LL_-SDFPSQX10_P4
Clock 100Mhz Data 0Mhz	5.899e-03	5.628e-03	5.365e-03	5.240e-03
Clock 100Mhz Data 25Mhz	5.822e-03	5.529e-03	5.212e-03	5.563e-03
Clock 100Mhz Data 50Mhz	5.744e-03	5.430e-03	5.060e-03	5.885e-03
Clock = 0 Data 100Mhz	2.750e-03	2.922e-03	2.821e-03	2.793e-03
Clock = 1 Data 100Mhz	2.473e-05	3.756e-04	2.593e-04	2.014e-04
	C8T28SOIDV_LL_-SDFPSQX14_P4	C8T28SOIDV_LL_-SDFPSQX19_P4	C8T28SOIDV_LL_-SDFPSQX29_P4	
Clock 100Mhz Data 0Mhz	5.165e-03	5.115e-03	5.080e-03	
Clock 100Mhz Data 25Mhz	5.678e-03	5.971e-03	6.352e-03	
Clock 100Mhz Data 50Mhz	6.191e-03	6.826e-03	7.624e-03	
Clock = 0 Data 100Mhz	2.776e-03	2.765e-03	2.757e-03	
Clock = 1 Data 100Mhz	1.667e-04	1.436e-04	1.271e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P4	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P4	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P4	C8T28SOI_LLHF_-SDFPSQNX3_P4	C8T28SOIDV_LL_-SDFPSQNX5_P4	C8T28SOIDV_LL_-SDFPSQNX10_P4
CP	0.0006	0.0006	0.0004	0.0004
D	0.0003	0.0004	0.0003	0.0003
SN	0.0012	0.0012	0.0009	0.0010
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNX14_P4	C8T28SOIDV_LL_-SDFPSQNX19_P4	C8T28SOIDV_LL_-SDFPSQNX23_P4	C8T28SOIDV_LL_-SDFPSQNX29_P4
CP	0.0004	0.0004	0.0004	0.0004
D	0.0003	0.0003	0.0003	0.0003
SN	0.0009	0.0009	0.0010	0.0009
TE	0.0008	0.0008	0.0008	0.0008
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNX5_P4	**C8T28SOI_LLHF_-SDFPSQNX3_P4**	**C8T28SOI_LL_-SDFPSQNX5_P4**	**C8T28SOI_LLHF_-SDFPSQNX3_P4**
CP to QN ↓	0.0895	0.0906	4.1202	5.9975
CP to QN ↑	0.0848	0.0778	6.0804	8.7241
SN to QN ↓	0.0794	0.0677	4.1156	5.9883
	C8T28SOIDV_LL_-SDFPSQNX5_P4	**C8T28SOIDV_LL_-SDFPSQNX10_P4**	**C8T28SOIDV_LL_-SDFPSQNX5_P4**	**C8T28SOIDV_LL_-SDFPSQNX10_P4**
CP to QN ↓	0.0960	0.0892	3.6894	1.8262
CP to QN ↑	0.0761	0.0766	5.6909	2.8521
SN to QN ↓	0.0730	0.0644	3.6860	1.8271
	C8T28SOIDV_LL_-SDFPSQNX14_P4	**C8T28SOIDV_LL_-SDFPSQNX19_P4**	**C8T28SOIDV_LL_-SDFPSQNX14_P4**	**C8T28SOIDV_LL_-SDFPSQNX19_P4**
CP to QN ↓	0.0922	0.0947	1.2510	0.9533
CP to QN ↑	0.0783	0.0810	1.9141	1.4405
SN to QN ↓	0.0658	0.0690	1.2497	0.9521
	C8T28SOIDV_LL_-SDFPSQNX23_P4	**C8T28SOIDV_LL_-SDFPSQNX29_P4**	**C8T28SOIDV_LL_-SDFPSQNX23_P4**	**C8T28SOIDV_LL_-SDFPSQNX29_P4**
CP to QN ↓	0.0964	0.0920	0.7372	0.6400
CP to QN ↑	0.0811	0.0821	1.4344	0.9628
SN to QN ↓	0.0714	0.0708	0.7368	0.6396

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P4	C8T28SOI_-LLHF_-SDFPSQNX3_-P4	C8T28SOIDV_-LL_-SDFPSQNX5_-P4	C8T28SOIDV_-LL_-SDFPSQNX10_-P4
CP ↓	min_pulse_width to CP	0.1165	0.1177	0.1004	0.1021
CP ↑	min_pulse_width to CP	0.0500	0.0456	0.0453	0.0499
D ↓	hold_rising to CP	-0.0533	-0.1088	-0.0192	-0.0170
D ↑	hold_rising to CP	-0.0114	-0.0089	-0.0049	-0.0049
D ↓	setup_rising to CP	0.0976	0.1630	0.0684	0.0684

D ↑	setup_rising to CP	0.0418	0.0440	0.0320	0.0320
SN ↓	min_pulse_width to SN	0.0496	0.0447	0.0452	0.0474
SN ↑	recovery_rising to CP	0.0053	0.0080	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0261	0.0363	0.0406	0.0406
TE ↓	hold_rising to CP	-0.0337	-0.0354	-0.0175	-0.0121
TE ↑	hold_rising to CP	-0.0093	-0.0062	-0.0023	-0.0023
TE ↓	setup_rising to CP	0.0955	0.1337	0.0662	0.0662
TE ↑	setup_rising to CP	0.1177	0.1594	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0732	-0.1100	-0.0535	-0.0537
TI ↑	hold_rising to CP	-0.0098	-0.0093	-0.0044	-0.0028
TI ↓	setup_rising to CP	0.1176	0.1545	0.1064	0.1064
TI ↑	setup_rising to CP	0.0404	0.0391	0.0293	0.0293
		C8T28SOIDV_-LL_-SDFPSQNX14_-P4	C8T28SOIDV_-LL_-SDFPSQNX19_-P4	C8T28SOIDV_-LL_-SDFPSQNX23_-P4	C8T28SOIDV_-LL_-SDFPSQNX29_-P4
CP ↓	min_pulse_width to CP	0.1021	0.1022	0.1022	0.1004
CP ↑	min_pulse_width to CP	0.0500	0.0499	0.0532	0.0545
D ↓	hold_rising to CP	-0.0170	-0.0175	-0.0170	-0.0192
D ↑	hold_rising to CP	-0.0049	-0.0049	-0.0049	-0.0049
D ↓	setup_rising to CP	0.0684	0.0684	0.0684	0.0684
D ↑	setup_rising to CP	0.0320	0.0320	0.0320	0.0320
SN ↓	min_pulse_width to SN	0.0474	0.0474	0.0474	0.0500
SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0406	0.0406	0.0406	0.0406
TE ↓	hold_rising to CP	-0.0121	-0.0121	-0.0121	-0.0153
TE ↑	hold_rising to CP	-0.0023	-0.0023	-0.0023	-0.0023
TE ↓	setup_rising to CP	0.0662	0.0662	0.0662	0.0662
TE ↑	setup_rising to CP	0.1079	0.1079	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0537	-0.0537	-0.0537	-0.0537
TI ↑	hold_rising to CP	-0.0028	-0.0028	-0.0028	-0.0028
TI ↓	setup_rising to CP	0.1072	0.1072	0.1064	0.1080
TI ↑	setup_rising to CP	0.0293	0.0293	0.0293	0.0293

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P4	6.453e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P4	6.027e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P4	6.269e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P4	8.609e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P4	9.436e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P4	1.066e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P4	1.130e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P4	1.367e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

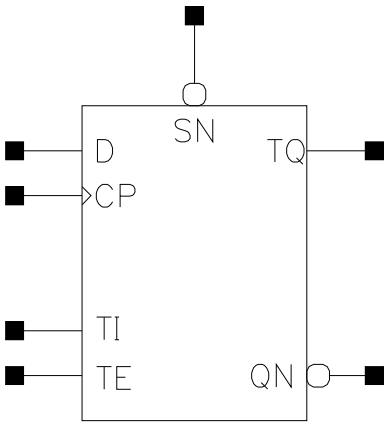
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P4	C8T28SOI_LLHF_-SDFPSQNX3_P4	C8T28SOIDV_LL_-SDFPSQNX5_P4	C8T28SOIDV_LL_-SDFPSQNX10_P4
Clock 100Mhz Data 0Mhz	5.887e-03	5.620e-03	5.358e-03	5.287e-03
Clock 100Mhz Data 25Mhz	5.728e-03	5.484e-03	5.294e-03	5.642e-03
Clock 100Mhz Data 50Mhz	5.570e-03	5.348e-03	5.230e-03	5.997e-03
Clock = 0 Data 100Mhz	2.749e-03	2.922e-03	2.822e-03	2.771e-03
Clock = 1 Data 100Mhz	2.483e-05	3.758e-04	2.595e-04	2.013e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P4	C8T28SOIDV_LL_-SDFPSQNX19_P4	C8T28SOIDV_LL_-SDFPSQNX23_P4	C8T28SOIDV_LL_-SDFPSQNX29_P4
Clock 100Mhz Data 0Mhz	5.243e-03	5.215e-03	5.195e-03	5.153e-03
Clock 100Mhz Data 25Mhz	5.781e-03	5.966e-03	6.057e-03	6.434e-03
Clock 100Mhz Data 50Mhz	6.320e-03	6.718e-03	6.919e-03	7.715e-03
Clock = 0 Data 100Mhz	2.740e-03	2.720e-03	2.706e-03	2.696e-03
Clock = 1 Data 100Mhz	1.665e-04	1.433e-04	1.267e-04	1.142e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P4	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P4	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P4	C8T28SOI_LLHF_-SDFPSQNTX3_P4	C8T28SOIDV_LL_-SDFPSQNTX5_P4	C8T28SOIDV_LL_-SDFPSQNTX10_P4
CP	0.0006	0.0006	0.0004	0.0004
D	0.0003	0.0004	0.0003	0.0003
SN	0.0013	0.0012	0.0009	0.0009
TE	0.0009	0.0009	0.0008	0.0008
TI	0.0003	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNTX19_P4	C8T28SOIDV_LL_-SDFPSQNTX23_P4	C8T28SOIDV_LL_-SDFPSQNTX29_P4	
CP	0.0004	0.0004	0.0004	
D	0.0003	0.0003	0.0003	
SN	0.0009	0.0009	0.0009	
TE	0.0008	0.0008	0.0008	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P4	**C8T28SOI_LLHF_-SDFPSQNTX3_P4**	**C8T28SOI_LL_-SDFPSQNTX5_P4**	**C8T28SOI_LLHF_-SDFPSQNTX3_P4**
CP to QN ↓	0.0975	0.0974	4.1805	6.0728
CP to QN ↑	0.0978	0.0919	6.0374	8.7478
CP to TQ ↓	0.0817	0.0655	11.3645	7.2855
CP to TQ ↑	0.0812	0.0760	30.1523	16.0170
SN to QN ↓	0.0844	0.0724	4.1770	6.0715
SN to TQ ↑	0.0687	0.0521	30.1033	15.9667
	C8T28SOIDV_LL_-SDFPSQNTX5_P4	**C8T28SOIDV_LL_-SDFPSQNTX10_P4**	**C8T28SOIDV_LL_-SDFPSQNTX5_P4**	**C8T28SOIDV_LL_-SDFPSQNTX10_P4**
CP to QN ↓	0.0958	0.0891	3.7520	1.8155
CP to QN ↑	0.0779	0.0817	5.7028	2.8638
CP to TQ ↓	0.0548	0.0631	7.2705	7.3596
CP to TQ ↑	0.0729	0.0765	13.6444	13.7159
SN to QN ↓	0.0718	0.0670	3.7536	1.8164
SN to TQ ↑	0.0489	0.0544	13.6309	13.6641
	C8T28SOIDV_LL_-SDFPSQNTX19_P4	**C8T28SOIDV_LL_-SDFPSQNTX23_P4**	**C8T28SOIDV_LL_-SDFPSQNTX19_P4**	**C8T28SOIDV_LL_-SDFPSQNTX23_P4**
CP to QN ↓	0.0945	0.0971	0.9473	0.7359
CP to QN ↑	0.0869	0.0860	1.4442	1.4349
CP to TQ ↓	0.0629	0.0639	7.3449	7.3919
CP to TQ ↑	0.0764	0.0773	13.7241	13.7301
SN to QN ↓	0.0721	0.0747	0.9470	0.7351
SN to TQ ↑	0.0541	0.0551	13.6580	13.6707
	C8T28SOIDV_LL_-SDFPSQNTX29_P4		**C8T28SOIDV_LL_-SDFPSQNTX29_P4**	
CP to QN ↓	0.0960		0.6418	
CP to QN ↑	0.0885		0.9632	

CP to TQ ↓	0.0667		7.5359	
CP to TQ ↑	0.0824		15.9109	
SN to QN ↓	0.0737		0.6413	
SN to TQ ↑	0.0603		15.8416	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P4	C8T28SOI_-LLHF_-SDFPSQNTX3_-P4	C8T28SOIDV_-LL_-SDFPSQNTX5_-P4	C8T28SOIDV_-LL_SDFP-SQNTX10_P4
CP ↓	min_pulse_width to CP	0.1189	0.1177	0.1004	0.1004
CP ↑	min_pulse_width to CP	0.0643	0.0549	0.0485	0.0532
D ↓	hold_rising to CP	-0.0565	-0.1088	-0.0192	-0.0192
D ↑	hold_rising to CP	-0.0114	-0.0089	-0.0049	-0.0049
D ↓	setup_rising to CP	0.1003	0.1656	0.0684	0.0716
D ↑	setup_rising to CP	0.0418	0.0440	0.0320	0.0320
SN ↓	min_pulse_width to SN	0.0571	0.0474	0.0452	0.0474
SN ↑	recovery_rising to CP	0.0080	0.0080	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0261	0.0363	0.0406	0.0378
TE ↓	hold_rising to CP	-0.0305	-0.0354	-0.0153	-0.0153
TE ↑	hold_rising to CP	-0.0093	-0.0062	-0.0023	-0.0023
TE ↓	setup_rising to CP	0.0977	0.1337	0.0662	0.0662
TE ↑	setup_rising to CP	0.1226	0.1594	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0775	-0.1100	-0.0537	-0.0537
TI ↑	hold_rising to CP	-0.0105	-0.0093	-0.0044	-0.0028
TI ↓	setup_rising to CP	0.1211	0.1545	0.1072	0.1080
TI ↑	setup_rising to CP	0.0404	0.0391	0.0293	0.0293
		C8T28SOIDV_-LL_SDFP-SQNTX19_P4	C8T28SOIDV_-LL_SDFP-SQNTX23_P4	C8T28SOIDV_-LL_SDFP-SQNTX29_P4	
CP ↓	min_pulse_width to CP	0.1004	0.1004	0.1004	
CP ↑	min_pulse_width to CP	0.0545	0.0545	0.0579	
D ↓	hold_rising to CP	-0.0192	-0.0192	-0.0192	
D ↑	hold_rising to CP	-0.0049	-0.0049	-0.0049	
D ↓	setup_rising to CP	0.0684	0.0716	0.0684	
D ↑	setup_rising to CP	0.0320	0.0320	0.0320	
SN ↓	min_pulse_width to SN	0.0500	0.0500	0.0522	

SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	
SN ↑	removal_rising to CP	0.0406	0.0406	0.0406	
TE ↓	hold_rising to CP	-0.0153	-0.0153	-0.0153	
TE ↑	hold_rising to CP	-0.0023	-0.0023	-0.0023	
TE ↓	setup_rising to CP	0.0662	0.0662	0.0662	
TE ↑	setup_rising to CP	0.1079	0.1079	0.1079	
TI ↓	hold_rising to CP	-0.0537	-0.0537	-0.0537	
TI ↑	hold_rising to CP	-0.0028	-0.0028	-0.0028	
TI ↓	setup_rising to CP	0.1080	0.1080	0.1080	
TI ↑	setup_rising to CP	0.0293	0.0293	0.0293	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P4	6.443e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P4	6.490e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P4	6.818e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_P4	9.090e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_P4	1.120e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_P4	1.191e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_P4	1.411e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

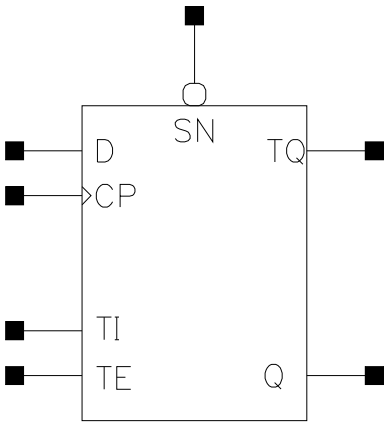
Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P4	C8T28SOI_LLHF_-SDFPSQNTX3_P4	C8T28SOIDV_LL_-SDFPSQNTX5_P4	C8T28SOIDV_LL_-SDFPSQNTX10_P4
Clock 100Mhz Data 0Mhz	5.703e-03	5.528e-03	5.301e-03	5.187e-03
Clock 100Mhz Data 25Mhz	5.770e-03	5.596e-03	5.329e-03	5.681e-03
Clock 100Mhz Data 50Mhz	5.837e-03	5.664e-03	5.357e-03	6.175e-03
Clock = 0 Data 100Mhz	2.745e-03	2.919e-03	2.820e-03	2.770e-03
Clock = 1 Data 100Mhz	2.482e-05	3.748e-04	2.589e-04	2.010e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P4	C8T28SOIDV_LL_-SDFPSQNTX23_P4	C8T28SOIDV_LL_-SDFPSQNTX29_P4	
Clock 100Mhz Data 0Mhz	5.118e-03	5.073e-03	5.041e-03	
Clock 100Mhz Data 25Mhz	6.022e-03	6.114e-03	6.517e-03	
Clock 100Mhz Data 50Mhz	6.925e-03	7.156e-03	7.992e-03	
Clock = 0 Data 100Mhz	2.740e-03	2.721e-03	2.708e-03	
Clock = 1 Data 100Mhz	1.663e-04	1.431e-04	1.265e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P4	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P4	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P4	C8T28SOI_LLHF_-SDFPSQTX3_P4	C8T28SOIDV_LL_-SDFPSQTX5_P4	C8T28SOIDV_LL_-SDFPSQTX10_P4
CP	0.0006	0.0006	0.0004	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0012	0.0012	0.0009	0.0009
TE	0.0009	0.0009	0.0008	0.0009
TI	0.0003	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQTX19_P4	C8T28SOIDV_LL_-SDFPSQTX29_P4		
CP	0.0005	0.0005		
D	0.0003	0.0003		
SN	0.0009	0.0009		
TE	0.0009	0.0009		
TI	0.0004	0.0004		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQTX5_P4	**C8T28SOI_LLHF_-SDFPSQTX3_P4**	**C8T28SOI_LL_-SDFPSQTX5_P4**	**C8T28SOI_LLHF_-SDFPSQTX3_P4**
CP to Q ↓	0.0830	0.0757	4.3763	6.6804
CP to Q ↑	0.0690	0.0758	5.8645	9.0504
CP to TQ ↓	0.0986	0.0733	11.9699	7.4545
CP to TQ ↑	0.0889	0.0803	30.1802	16.2056
SN to Q ↑	0.0566	0.0515	5.7879	8.9412
SN to TQ ↑	0.0740	0.0553	30.0846	16.1247
	C8T28SOIDV_LL_-SDFPSQTX5_P4	**C8T28SOIDV_LL_-SDFPSQTX10_P4**	**C8T28SOIDV_LL_-SDFPSQTX5_P4**	**C8T28SOIDV_LL_-SDFPSQTX10_P4**
CP to Q ↓	0.0629	0.0818	3.9272	1.8972
CP to Q ↑	0.0740	0.1140	5.8074	2.8952
CP to TQ ↓	0.0635	0.0842	7.3620	7.5183
CP to TQ ↑	0.0767	0.1189	13.7793	13.5503
SN to Q ↑	0.0516	0.0887	5.7912	2.8949
SN to TQ ↑	0.0544	0.0935	13.7196	13.5572
	C8T28SOIDV_LL_-SDFPSQTX19_P4	**C8T28SOIDV_LL_-SDFPSQTX29_P4**	**C8T28SOIDV_LL_-SDFPSQTX19_P4**	**C8T28SOIDV_LL_-SDFPSQTX29_P4**
CP to Q ↓	0.0882	0.0996	0.9789	0.6322
CP to Q ↑	0.1197	0.1304	1.4777	0.9817
CP to TQ ↓	0.0887	0.0563	6.3415	6.5759
CP to TQ ↑	0.1254	0.0810	15.8187	15.9302
SN to Q ↑	0.0943	0.1049	1.4766	0.9797
SN to TQ ↑	0.1000	0.0560	15.8208	15.9111

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_P4	C8T28SOI_-LLHF_-SDFPSQTX3_P4	C8T28SOIDV_-LL_-SDFPSQTX5_P4	C8T28SOIDV_-LL_-SDFPSQTX10_-P4
CP ↓	min_pulse_width to CP	0.1189	0.1177	0.1004	0.0998
CP ↑	min_pulse_width to CP	0.0738	0.0597	0.0499	0.0454
D ↓	hold_rising to CP	-0.0565	-0.1088	-0.0192	-0.0240
D ↑	hold_rising to CP	-0.0114	-0.0089	-0.0049	-0.0045
D ↓	setup_rising to CP	0.1003	0.1656	0.0684	0.0732
D ↑	setup_rising to CP	0.0418	0.0440	0.0320	0.0315
SN ↓	min_pulse_width to SN	0.0571	0.0474	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0080	0.0106	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0261	0.0363	0.0378	0.0406
TE ↓	hold_rising to CP	-0.0305	-0.0354	-0.0179	-0.0218
TE ↑	hold_rising to CP	-0.0093	-0.0062	-0.0023	-0.0098
TE ↓	setup_rising to CP	0.0977	0.1337	0.0662	0.0711
TE ↑	setup_rising to CP	0.1226	0.1594	0.1079	0.1079
TI ↓	hold_rising to CP	-0.0775	-0.1058	-0.0537	-0.0537
TI ↑	hold_rising to CP	-0.0105	-0.0093	-0.0028	-0.0098
TI ↓	setup_rising to CP	0.1211	0.1545	0.1064	0.1016
TI ↑	setup_rising to CP	0.0404	0.0391	0.0293	0.0404
		C8T28SOIDV_-LL_-SDFPSQTX19_-P4	C8T28SOIDV_-LL_-SDFPSQTX29_-P4		
CP ↓	min_pulse_width to CP	0.0998	0.0998		
CP ↑	min_pulse_width to CP	0.0454	0.0500		
D ↓	hold_rising to CP	-0.0240	-0.0240		
D ↑	hold_rising to CP	-0.0045	-0.0049		
D ↓	setup_rising to CP	0.0737	0.0732		
D ↑	setup_rising to CP	0.0320	0.0320		
SN ↓	min_pulse_width to SN	0.0474	0.0549		
SN ↑	recovery_rising to CP	-0.0044	-0.0017		
SN ↑	removal_rising to CP	0.0406	0.0406		
TE ↓	hold_rising to CP	-0.0218	-0.0192		
TE ↑	hold_rising to CP	-0.0098	-0.0098		

TE ↓	setup_rising to CP	0.0711	0.0711		
TE ↑	setup_rising to CP	0.1057	0.1085		
TI ↓	hold_rising to CP	-0.0537	-0.0537		
TI ↑	hold_rising to CP	-0.0105	-0.0105		
TI ↓	setup_rising to CP	0.1024	0.1016		
TI ↑	setup_rising to CP	0.0346	0.0388		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P4	6.519e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P4	6.557e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P4	6.811e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P4	8.845e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P4	1.088e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P4	1.415e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

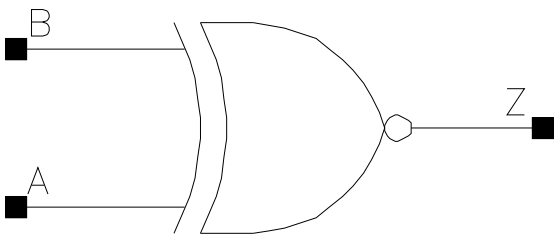
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P4	C8T28SOI_LLHF_-SDFPSQTX3_P4	C8T28SOIDV_LL_-SDFPSQTX5_P4	C8T28SOIDV_LL_-SDFPSQTX10_P4
Clock 100Mhz Data 0Mhz	5.711e-03	5.535e-03	5.306e-03	5.196e-03
Clock 100Mhz Data 25Mhz	5.813e-03	5.615e-03	5.342e-03	5.617e-03
Clock 100Mhz Data 50Mhz	5.914e-03	5.696e-03	5.377e-03	6.039e-03
Clock = 0 Data 100Mhz	2.745e-03	2.919e-03	2.819e-03	2.800e-03
Clock = 1 Data 100Mhz	2.487e-05	3.754e-04	2.592e-04	2.014e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P4	C8T28SOIDV_LL_-SDFPSQTX29_P4		
Clock 100Mhz Data 0Mhz	5.130e-03	5.087e-03		
Clock 100Mhz Data 25Mhz	6.016e-03	6.541e-03		
Clock 100Mhz Data 50Mhz	6.902e-03	7.995e-03		
Clock = 0 Data 100Mhz	2.782e-03	2.769e-03		
Clock = 1 Data 100Mhz	1.667e-04	1.436e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.600	0.544	0.8704
X5_P4	0.800	1.496	1.1968
X8_P4	1.600	1.088	1.7408
X9_P4	0.800	1.632	1.3056
X11_P4	1.600	1.360	2.1760
X14_P4	0.800	2.312	1.8496
X15_P4	1.600	1.904	3.0464
X19_P4	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P4	X5_P4	X8_P4	X9_P4
A	0.0009	0.0005	0.0015	0.0006
B	0.0008	0.0009	0.0012	0.0011
	X11_P4	X14_P4	X15_P4	X19_P4
A	0.0022	0.0008	0.0026	0.0010
B	0.0020	0.0014	0.0024	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X5_P4	X4_P4	X5_P4
A to Z ↓	0.0186	0.0551	5.2568	3.9906
A to Z ↑	0.0214	0.0501	8.2888	6.1953
B to Z ↓	0.0177	0.0406	5.2552	3.9749
B to Z ↑	0.0224	0.0378	8.2969	6.1899

	X8_P4	X9_P4	X8_P4	X9_P4
A to Z ↓	0.0221	0.0505	2.7578	2.0484
A to Z ↑	0.0260	0.0469	4.3667	3.1498
B to Z ↓	0.0213	0.0381	2.7584	2.0458
B to Z ↑	0.0259	0.0362	4.3693	3.1497
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0207	0.0478	1.9246	1.3862
A to Z ↑	0.0237	0.0434	2.8595	2.0141
B to Z ↓	0.0192	0.0354	1.9238	1.3808
B to Z ↑	0.0233	0.0336	2.8648	2.0111
	X15_P4	**X19_P4**	**X15_P4**	**X19_P4**
A to Z ↓	0.0228	0.0438	1.4548	1.0321
A to Z ↑	0.0262	0.0410	2.1722	1.4998
B to Z ↓	0.0212	0.0334	1.4532	1.0303
B to Z ↑	0.0258	0.0323	2.1756	1.4994

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	3.225e-05	1.000e-20
X5_P4	3.546e-05	1.000e-20
X8_P4	5.120e-05	1.000e-20
X9_P4	5.775e-05	1.000e-20
X11_P4	7.742e-05	1.000e-20
X14_P4	8.739e-05	1.000e-20
X15_P4	9.785e-05	1.000e-20
X19_P4	1.216e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X5_P4	X8_P4	X9_P4
A to Z	1.264e-03	2.746e-03	2.488e-03	3.864e-03
B to Z	1.254e-03	2.198e-03	2.464e-03	3.104e-03
	X11_P4	X14_P4	X15_P4	X19_P4
A to Z	3.545e-03	6.045e-03	4.803e-03	7.299e-03
B to Z	3.460e-03	4.748e-03	4.704e-03	5.868e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

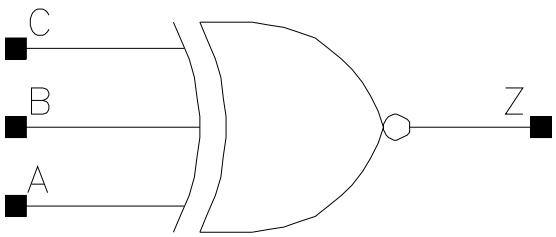
Pin Cycle (vdds)	X4_P4	X5_P4	X8_P4	X9_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P4	X14_P4	X15_P4	X19_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P4	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P4	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P4	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P4	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P4	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P4	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P4	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P4	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P4	C8T28SOIDV_LL_-XNOR3X4_P4	C8T28SOIDV_LL_-XNOR3X9_P4	C8T28SOIDV_LL_-XNOR3X13_P4
A	0.0014	0.0014	0.0017	0.0023
B	0.0014	0.0013	0.0017	0.0023
C	0.0006	0.0006	0.0006	0.0006
	C8T28SOIDV_LLS_-XNOR3X1_P4	C8T28SOIDV_LLS_-XNOR3X2_P4	C8T28SOIDV_LLS_-XNOR3X5_P4	C8T28SOIDV_LLS_-XNOR3X7_P4

A	0.0013	0.0015	0.0033	0.0049
B	0.0014	0.0016	0.0030	0.0046
C	0.0009	0.0011	0.0022	0.0031

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XNOR3X2_P4	**C8T28SOIDV_LL_-XNOR3X4_P4**	**C8T28SOIDV_LL_-XNOR3X2_P4**	**C8T28SOIDV_LL_-XNOR3X4_P4**
A to Z ↓	0.0566	0.0600	8.4074	4.3408
A to Z ↑	0.0544	0.0551	11.5592	6.2739
B to Z ↓	0.0573	0.0608	8.4094	4.3406
B to Z ↑	0.0552	0.0560	11.5712	6.2786
C to Z ↓	0.0764	0.0811	8.4056	4.3390
C to Z ↑	0.0743	0.0762	11.5602	6.2771
	C8T28SOIDV_LL_-XNOR3X9_P4	**C8T28SOIDV_LL_-XNOR3X13_P4**	**C8T28SOIDV_LL_-XNOR3X9_P4**	**C8T28SOIDV_LL_-XNOR3X13_P4**
A to Z ↓	0.0505	0.0585	2.1810	1.4890
A to Z ↑	0.0531	0.0605	3.0633	2.1154
B to Z ↓	0.0514	0.0594	2.1806	1.4891
B to Z ↑	0.0542	0.0618	3.0628	2.1150
C to Z ↓	0.0732	0.0888	2.1796	1.4892
C to Z ↑	0.0756	0.0913	3.0613	2.1153
	C8T28SOIDV_LLS_-XNOR3X1_P4	**C8T28SOIDV_LLS_-XNOR3X2_P4**	**C8T28SOIDV_LLS_-XNOR3X1_P4**	**C8T28SOIDV_LLS_-XNOR3X2_P4**
A to Z ↓	0.0341	0.0380	15.4878	8.2288
A to Z ↑	0.0358	0.0351	25.1699	12.9879
B to Z ↓	0.0350	0.0393	15.5014	8.2332
B to Z ↑	0.0367	0.0361	25.1619	12.9800
C to Z ↓	0.0338	0.0368	15.5014	8.2460
C to Z ↑	0.0359	0.0345	25.1368	12.9784
	C8T28SOIDV_LLS_-XNOR3X5_P4	**C8T28SOIDV_LLS_-XNOR3X7_P4**	**C8T28SOIDV_LLS_-XNOR3X5_P4**	**C8T28SOIDV_LLS_-XNOR3X7_P4**
A to Z ↓	0.0384	0.0322	3.8991	2.6960
A to Z ↑	0.0371	0.0315	6.3428	4.2397
B to Z ↓	0.0378	0.0311	3.9051	2.7019
B to Z ↑	0.0365	0.0310	6.3417	4.2394
C to Z ↓	0.0359	0.0300	3.9013	2.7024
C to Z ↑	0.0348	0.0294	6.3331	4.2359

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P4	2.377e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P4	2.860e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P4	5.075e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P4	7.228e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P4	1.558e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P4	2.733e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P4	6.575e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P4	9.960e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P4	C8T28SOIDV_LL_-XNOR3X4_P4	C8T28SOIDV_LL_-XNOR3X9_P4	C8T28SOIDV_LL_-XNOR3X13_P4
A to Z	1.666e-03	2.001e-03	2.985e-03	5.028e-03
B to Z	1.657e-03	1.994e-03	3.006e-03	5.065e-03
C to Z	2.626e-03	3.004e-03	4.241e-03	6.981e-03
	C8T28SOIDV_LLS_-XNOR3X1_P4	C8T28SOIDV_LLS_-XNOR3X2_P4	C8T28SOIDV_LLS_-XNOR3X5_P4	C8T28SOIDV_LLS_-XNOR3X7_P4
A to Z	9.801e-04	1.443e-03	3.197e-03	4.324e-03
B to Z	9.802e-04	1.470e-03	3.249e-03	4.287e-03
C to Z	9.669e-04	1.456e-03	3.238e-03	4.268e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

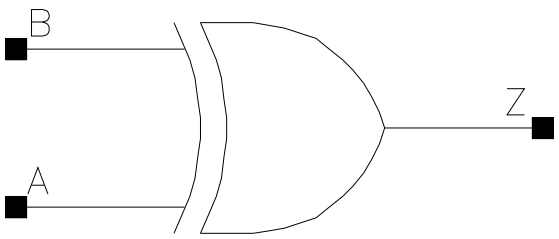
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P4	C8T28SOIDV_LL_-XNOR3X4_P4	C8T28SOIDV_LL_-XNOR3X9_P4	C8T28SOIDV_LL_-XNOR3X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P4	C8T28SOIDV_LLS_-XNOR3X2_P4	C8T28SOIDV_LLS_-XNOR3X5_P4	C8T28SOIDV_LLS_-XNOR3X7_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.360	1.0880
X4_P4	1.600	0.544	0.8704
X5_P4	0.800	1.360	1.0880
X8_P4	1.600	1.088	1.7408
X9_P4	0.800	1.496	1.1968
X12_P4	1.600	1.360	2.1760
X13_P4	0.800	2.176	1.7408
X15_P4	1.600	1.904	3.0464
X17_P4	0.800	2.312	1.8496
X18_P4	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P4	X4_P4	X5_P4	X8_P4
A	0.0005	0.0009	0.0006	0.0014
B	0.0009	0.0008	0.0010	0.0014
	X9_P4	X12_P4	X13_P4	X15_P4
A	0.0006	0.0023	0.0011	0.0027
B	0.0013	0.0018	0.0020	0.0022
	X17_P4	X18_P4		
A	0.0011	0.0014		
B	0.0020	0.0017		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X4_P4**	**X2_P4**	**X4_P4**
A to Z ↓	0.0470	0.0192	7.9980	4.0143
A to Z ↑	0.0456	0.0232	11.8904	10.9677
B to Z ↓	0.0360	0.0197	7.9454	4.0378
B to Z ↑	0.0374	0.0219	11.8819	10.9669
	X5_P4	**X8_P4**	**X5_P4**	**X8_P4**
A to Z ↓	0.0434	0.0250	4.1090	2.1558
A to Z ↑	0.0399	0.0279	6.0500	5.6990
B to Z ↓	0.0331	0.0260	4.0922	2.1705
B to Z ↑	0.0325	0.0266	6.0415	5.6948
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0420	0.0225	2.1556	1.4527
A to Z ↑	0.0398	0.0249	3.1281	3.8130
B to Z ↓	0.0321	0.0216	2.1498	1.4632
B to Z ↑	0.0317	0.0228	3.1224	3.8091
	X13_P4	**X15_P4**	**X13_P4**	**X15_P4**
A to Z ↓	0.0386	0.0244	1.4681	1.1227
A to Z ↑	0.0365	0.0287	2.1608	3.3847
B to Z ↓	0.0269	0.0233	1.4643	1.1315
B to Z ↑	0.0258	0.0264	2.1596	3.3809
	X17_P4	**X18_P4**	**X17_P4**	**X18_P4**
A to Z ↓	0.0407	0.0450	1.1126	1.1218
A to Z ↑	0.0380	0.0410	1.6191	1.5756
B to Z ↓	0.0290	0.0348	1.1100	1.1209
B to Z ↑	0.0275	0.0320	1.6175	1.5752

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P4	2.727e-05	1.000e-20
X4_P4	3.263e-05	1.000e-20
X5_P4	4.303e-05	1.000e-20
X8_P4	5.226e-05	1.000e-20
X9_P4	6.980e-05	1.000e-20
X12_P4	7.948e-05	1.000e-20
X13_P4	1.124e-04	1.000e-20
X15_P4	9.601e-05	1.000e-20
X17_P4	1.210e-04	1.000e-20
X18_P4	1.196e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P4	X4_P4	X5_P4	X8_P4
A to Z	1.991e-03	1.286e-03	2.526e-03	2.559e-03
B to Z	1.755e-03	1.254e-03	2.180e-03	2.561e-03
	X9_P4	X12_P4	X13_P4	X15_P4
A to Z	3.638e-03	3.589e-03	5.913e-03	4.685e-03
B to Z	3.195e-03	3.466e-03	3.967e-03	4.544e-03
	X17_P4	X18_P4		
A to Z	6.682e-03	7.399e-03		
B to Z	4.710e-03	5.744e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

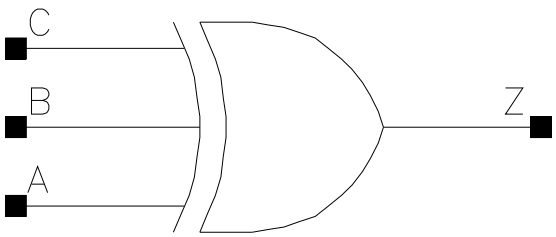
Pin Cycle (vdds)	X2_P4	X4_P4	X5_P4	X8_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P4	X12_P4	X13_P4	X15_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P4	X18_P4		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P4	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P4	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P4	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P4	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P4	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P4	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P4	C8T28SOIDV_LL_-XOR3X4_P4	C8T28SOIDV_LL_-XOR3X9_P4	C8T28SOIDV_LL_-XOR3X13_P4
A	0.0014	0.0013	0.0016	0.0023
B	0.0014	0.0014	0.0017	0.0022
C	0.0009	0.0009	0.0012	0.0019
	C8T28SOIDV_LLS_-XOR3X1_P4	C8T28SOIDV_LLS_-XOR3X2_P4	C8T28SOIDV_LLS_-XOR3X5_P4	C8T28SOIDV_LLS_-XOR3X7_P4

A	0.0014	0.0015	0.0026	0.0040
B	0.0015	0.0015	0.0026	0.0041
C	0.0005	0.0005	0.0005	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P4	**C8T28SOIDV_LL_-XOR3X4_P4**	**C8T28SOIDV_LL_-XOR3X2_P4**	**C8T28SOIDV_LL_-XOR3X4_P4**
A to Z ↓	0.0550	0.0604	8.4542	4.3547
A to Z ↑	0.0531	0.0569	11.8878	6.2729
B to Z ↓	0.0553	0.0615	8.4574	4.3561
B to Z ↑	0.0537	0.0583	11.8910	6.2732
C to Z ↓	0.0547	0.0605	8.4613	4.3577
C to Z ↑	0.0526	0.0567	11.8923	6.2741
	C8T28SOIDV_LL_-XOR3X9_P4	**C8T28SOIDV_LL_-XOR3X13_P4**	**C8T28SOIDV_LL_-XOR3X9_P4**	**C8T28SOIDV_LL_-XOR3X13_P4**
A to Z ↓	0.0537	0.0603	2.1658	1.4410
A to Z ↑	0.0546	0.0618	3.0761	2.0696
B to Z ↓	0.0549	0.0611	2.1664	1.4417
B to Z ↑	0.0561	0.0631	3.0766	2.0705
C to Z ↓	0.0534	0.0604	2.1658	1.4419
C to Z ↑	0.0539	0.0625	3.0780	2.0703
	C8T28SOIDV_LLS_-XOR3X1_P4	**C8T28SOIDV_LLS_-XOR3X2_P4**	**C8T28SOIDV_LLS_-XOR3X1_P4**	**C8T28SOIDV_LLS_-XOR3X2_P4**
A to Z ↓	0.0357	0.0396	10.7635	8.4117
A to Z ↑	0.0360	0.0351	17.9994	12.3820
B to Z ↓	0.0367	0.0403	10.7859	8.4179
B to Z ↑	0.0370	0.0358	18.0069	12.3763
C to Z ↓	0.0563	0.0608	10.7629	8.3920
C to Z ↑	0.0577	0.0572	17.9879	12.3411
	C8T28SOIDV_LLS_-XOR3X5_P4	**C8T28SOIDV_LLS_-XOR3X7_P4**	**C8T28SOIDV_LLS_-XOR3X5_P4**	**C8T28SOIDV_LLS_-XOR3X7_P4**
A to Z ↓	0.0532	0.0451	4.3161	2.9886
A to Z ↑	0.0445	0.0379	6.3958	4.3082
B to Z ↓	0.0503	0.0445	4.3288	2.9935
B to Z ↑	0.0434	0.0380	6.3995	4.3091
C to Z ↓	0.0845	0.0698	4.3333	2.9879
C to Z ↑	0.0779	0.0634	6.3864	4.2977

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P4	1.924e-05	1.000e-20
C8T28SOIDV_LL_XOR3X4_P4	2.461e-05	1.000e-20
C8T28SOIDV_LL_XOR3X9_P4	4.547e-05	1.000e-20
C8T28SOIDV_LL_XOR3X13_P4	6.785e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P4	2.742e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P4	3.258e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P4	5.598e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P4	8.374e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P4	C8T28SOIDV_LL_-XOR3X4_P4	C8T28SOIDV_LL_-XOR3X9_P4	C8T28SOIDV_LL_-XOR3X13_P4
A to Z	1.578e-03	1.998e-03	3.012e-03	5.327e-03
B to Z	1.566e-03	2.002e-03	3.038e-03	5.355e-03
C to Z	1.555e-03	1.982e-03	3.026e-03	5.368e-03
	C8T28SOIDV_LLS_-XOR3X1_P4	C8T28SOIDV_LLS_-XOR3X2_P4	C8T28SOIDV_LLS_-XOR3X5_P4	C8T28SOIDV_LLS_-XOR3X7_P4
A to Z	1.211e-03	1.486e-03	3.019e-03	4.162e-03
B to Z	1.217e-03	1.508e-03	3.076e-03	4.245e-03
C to Z	2.302e-03	2.649e-03	5.031e-03	6.925e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P4	C8T28SOIDV_LL_-XOR3X4_P4	C8T28SOIDV_LL_-XOR3X9_P4	C8T28SOIDV_LL_-XOR3X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P4	C8T28SOIDV_LLS_-XOR3X2_P4	C8T28SOIDV_LLS_-XOR3X5_P4	C8T28SOIDV_LLS_-XOR3X7_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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