C28SOI_SC_12_COREPBP10_LR Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 10 nm

Overview

- C28SOI_SC_12_COREPBP10_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

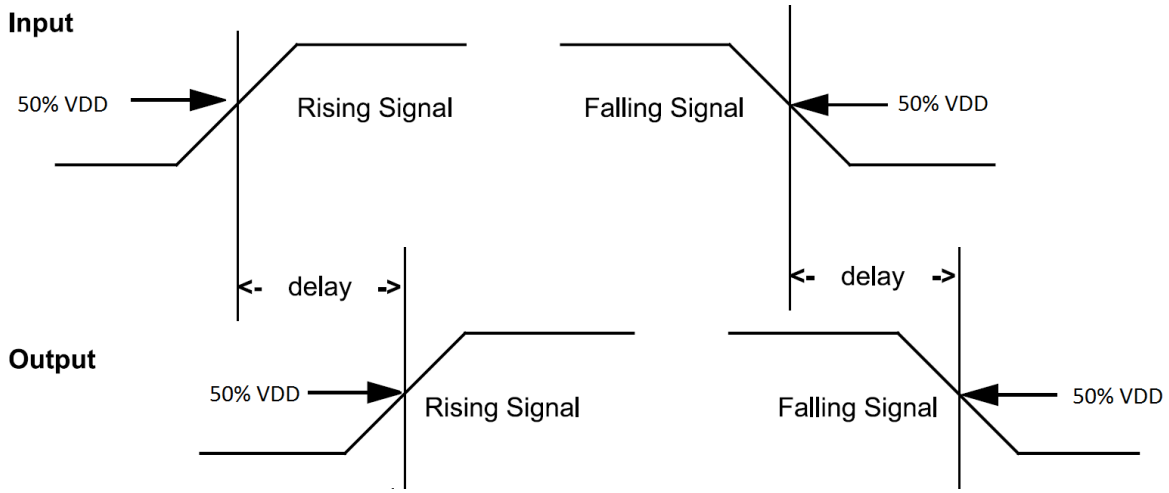


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

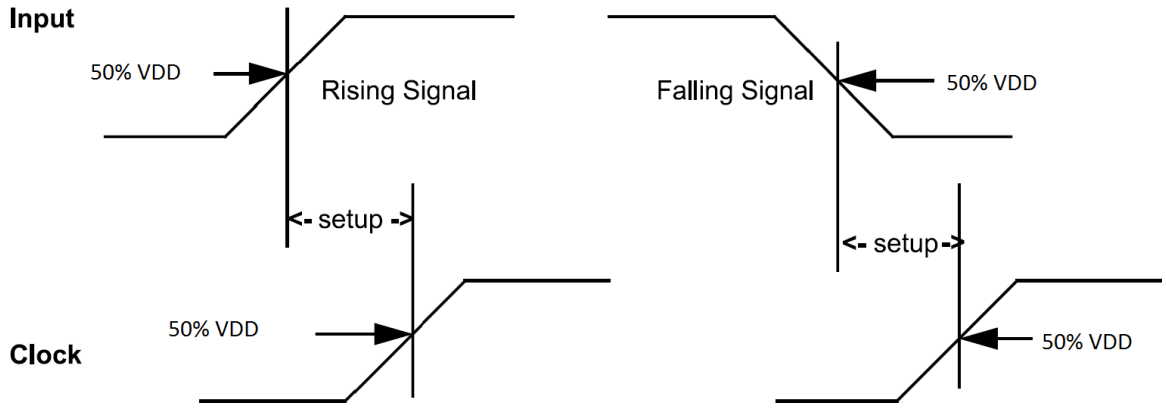


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

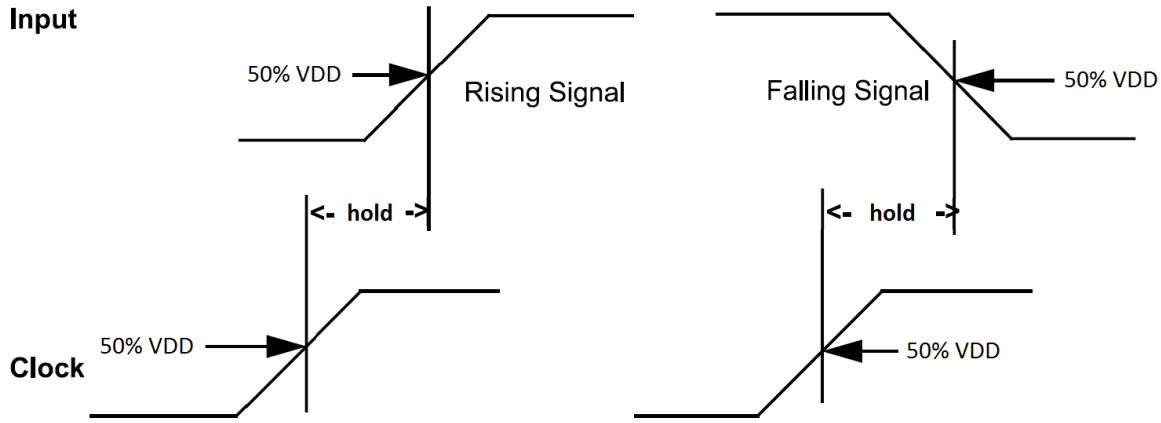


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

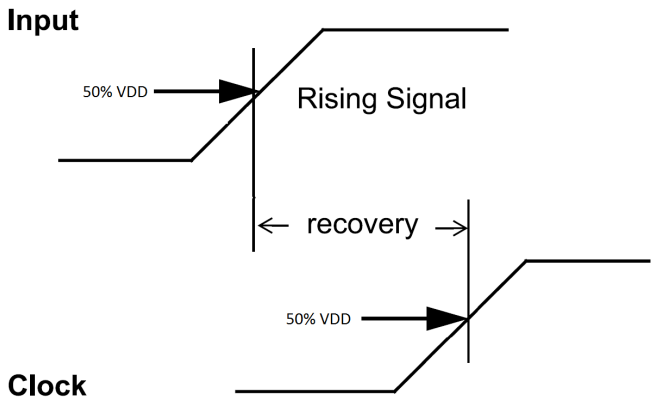


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

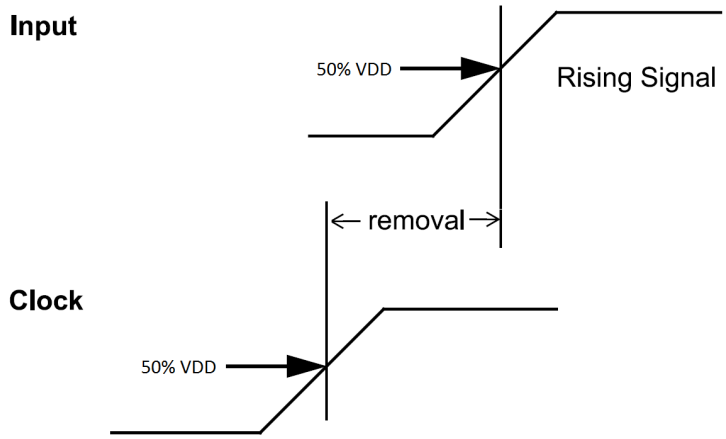


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

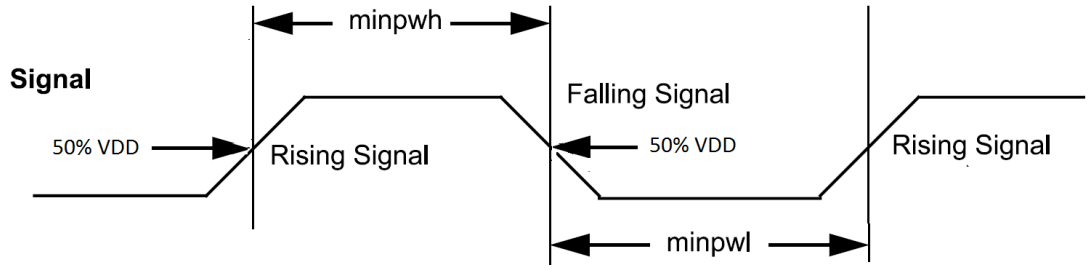


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

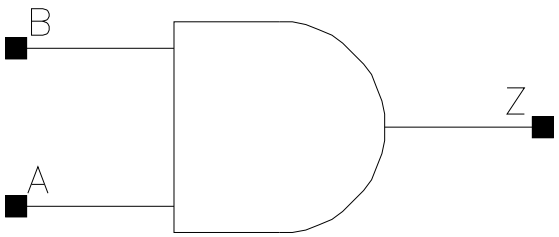
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X25_P10	1.200	1.088	1.3056
X33_P10	1.200	1.360	1.6320
X42_P10	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0009	0.0013	0.0019	0.0024
B	0.0008	0.0012	0.0018	0.0023
	X42_P10			
A	0.0023			
B	0.0023			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0300	0.0255	1.7848	0.9029
A to Z ↑	0.0220	0.0208	3.0057	1.4611
B to Z ↓	0.0284	0.0239	1.7836	0.9022
B to Z ↑	0.0237	0.0223	3.0025	1.4586
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0261	0.0254	0.5974	0.4451

A to Z ↑	0.0204	0.0211	0.9638	0.7280
B to Z ↓	0.0246	0.0232	0.5975	0.4444
B to Z ↑	0.0218	0.0220	0.9647	0.7271
	X42_P10		**X42_P10**	
A to Z ↓	0.0274		0.3611	
A to Z ↑	0.0231		0.5832	
B to Z ↓	0.0253		0.3607	
B to Z ↑	0.0242		0.5827	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	5.924e-06	1.145e-09
X16_P10	1.081e-05	1.310e-09
X25_P10	1.596e-05	1.807e-09
X33_P10	2.171e-05	2.139e-09
X42_P10	2.444e-05	2.304e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	1.637e-05	3.146e-05	4.873e-05	1.142e-04
B (output stable)	2.804e-05	4.917e-05	7.839e-05	3.996e-04
A to Z	3.321e-03	5.636e-03	8.630e-03	1.143e-02
B to Z	3.143e-03	5.331e-03	8.143e-03	1.048e-02
	X42_P10			
A (output stable)	1.145e-04			
B (output stable)	3.980e-04			
A to Z	1.381e-02			
B to Z	1.284e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

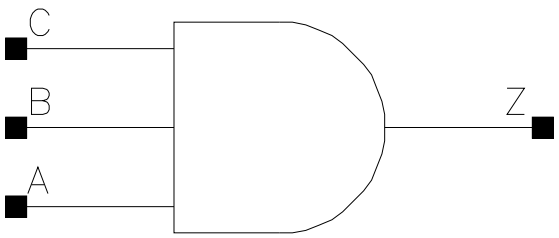
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	6.360e-08	3.036e-08	-2.860e-08	-1.510e-08
B (output stable)	8.280e-08	3.310e-08	8.600e-09	-1.360e-08
A to Z	-5.900e-09	-4.751e-08	-1.416e-07	-1.789e-07
B to Z	1.180e-08	-1.197e-08	2.261e-07	-1.532e-07
	X42_P10			
A (output stable)	-1.190e-08			
B (output stable)	-6.500e-09			
A to Z	-4.383e-07			
B to Z	-1.643e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X25_P10	1.200	1.360	1.6320
X33_P10	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0008	0.0012	0.0020	0.0024
B	0.0007	0.0012	0.0018	0.0023
C	0.0007	0.0012	0.0017	0.0022

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0325	0.0278	1.8043	0.8797
A to Z ↑	0.0283	0.0265	3.0278	1.4454
B to Z ↓	0.0313	0.0266	1.8038	0.8797
B to Z ↑	0.0292	0.0275	3.0278	1.4463
C to Z ↓	0.0297	0.0250	1.8012	0.8771
C to Z ↑	0.0303	0.0281	3.0260	1.4461
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0279	0.0268	0.6041	0.4513

A to Z ↑	0.0261	0.0253	0.9862	0.7389
B to Z ↓	0.0267	0.0255	0.6037	0.4506
B to Z ↑	0.0272	0.0263	0.9864	0.7393
C to Z ↓	0.0251	0.0241	0.6025	0.4504
C to Z ↑	0.0280	0.0272	0.9871	0.7394

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	4.960e-06	1.310e-09
X17_P10	9.451e-06	1.476e-09
X25_P10	1.377e-05	2.139e-09
X33_P10	1.817e-05	2.304e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	1.981e-05	3.939e-05	5.358e-05	7.179e-05
B (output stable)	4.396e-05	8.857e-05	1.252e-04	1.717e-04
C (output stable)	8.906e-05	1.728e-04	2.559e-04	3.525e-04
A to Z	3.702e-03	6.549e-03	9.624e-03	1.245e-02
B to Z	3.512e-03	6.219e-03	9.109e-03	1.176e-02
C to Z	3.346e-03	5.885e-03	8.602e-03	1.109e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

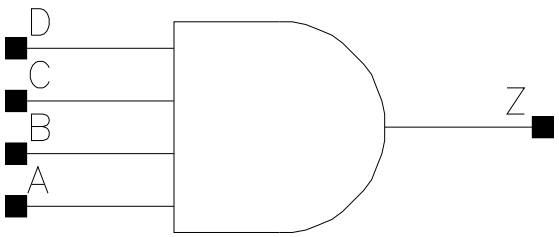
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	7.690e-08	4.185e-08	-1.303e-08	-4.420e-08
B (output stable)	8.898e-08	4.583e-08	6.033e-09	-2.040e-08
C (output stable)	8.407e-08	4.557e-08	2.653e-08	-9.867e-09
A to Z	-1.547e-07	-2.540e-08	-9.650e-08	3.149e-07
B to Z	-2.967e-08	7.710e-08	-3.737e-07	-3.963e-07
C to Z	-2.475e-07	-1.911e-07	-2.114e-07	-4.084e-07

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X6_P10	1.200	1.088	1.3056
X20_P10	1.200	2.312	2.7744
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P10	X6_P10	X20_P10	X27_P10
A	0.0006	0.0009	0.0021	0.0023
B	0.0006	0.0008	0.0020	0.0023
C	0.0005	0.0009	0.0020	0.0023
D	0.0006	0.0009	0.0020	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X6_P10	X4_P10	X6_P10
A to Z ↓	0.0339	0.0297	3.2641	2.1624
A to Z ↑	0.0306	0.0236	10.0405	5.4946
B to Z ↓	0.0327	0.0276	3.2663	2.1602
B to Z ↑	0.0324	0.0248	10.0483	5.4935
C to Z ↓	0.0346	0.0312	3.2445	2.1777
C to Z ↑	0.0301	0.0230	10.0505	5.5062

D to Z ↓	0.0334	0.0289	3.2406	2.1757
D to Z ↑	0.0325	0.0242	10.0616	5.5061
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0289	0.0272	0.6352	0.4498
A to Z ↑	0.0245	0.0277	1.8369	1.3956
B to Z ↓	0.0263	0.0250	0.6339	0.4489
B to Z ↑	0.0251	0.0287	1.8371	1.3961
C to Z ↓	0.0282	0.0261	0.6400	0.4520
C to Z ↑	0.0216	0.0236	1.8372	1.3952
D to Z ↓	0.0255	0.0240	0.6388	0.4511
D to Z ↑	0.0221	0.0246	1.8369	1.3953

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	4.856e-06	1.807e-09
X6_P10	9.345e-06	1.807e-09
X20_P10	2.573e-05	3.298e-09
X27_P10	2.958e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	5.921e-04	9.274e-04	2.718e-03	3.380e-03
B (output stable)	5.479e-04	8.370e-04	2.488e-03	3.138e-03
C (output stable)	5.559e-04	9.150e-04	2.376e-03	2.928e-03
D (output stable)	5.169e-04	8.198e-04	2.120e-03	2.664e-03
A to Z	2.406e-03	3.734e-03	1.124e-02	1.462e-02
B to Z	2.290e-03	3.507e-03	1.031e-02	1.370e-02
C to Z	2.329e-03	3.705e-03	9.591e-03	1.200e-02
D to Z	2.214e-03	3.460e-03	8.653e-03	1.105e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

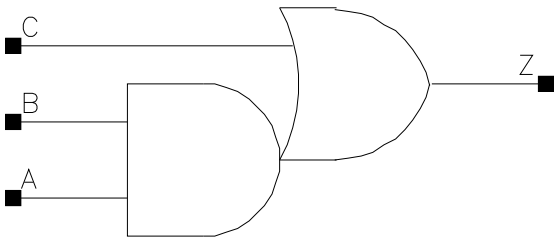
Pin Cycle (vdds)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	-1.481e-08	4.277e-07	5.603e-08	-1.960e-06
B (output stable)	-5.286e-10	2.596e-07	-2.902e-07	-2.172e-06
C (output stable)	5.899e-06	1.017e-05	3.694e-05	6.900e-05
D (output stable)	5.958e-06	1.011e-05	3.686e-05	6.850e-05
A to Z	2.887e-07	2.035e-06	4.487e-06	2.431e-06
B to Z	3.469e-07	1.355e-06	3.137e-06	1.207e-06
C to Z	-1.765e-07	-1.844e-07	-7.959e-07	-1.623e-06
D to Z	-1.501e-07	-2.664e-07	-1.193e-06	-1.546e-06

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0008	0.0011	0.0024
B	0.0008	0.0012	0.0022
C	0.0008	0.0013	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0382	0.0350	1.8406	0.8996
A to Z ↑	0.0230	0.0208	2.9293	1.4373
B to Z ↓	0.0353	0.0323	1.8321	0.8956
B to Z ↑	0.0249	0.0227	2.9297	1.4358
C to Z ↓	0.0368	0.0338	1.8299	0.8952
C to Z ↑	0.0219	0.0208	2.9110	1.4284
	X33_P10		**X33_P10**	
A to Z ↓	0.0348		0.4568	
A to Z ↑	0.0211		0.7239	

B to Z ↓	0.0323		0.4553	
B to Z ↑	0.0226		0.7239	
C to Z ↓	0.0338		0.4547	
C to Z ↑	0.0204		0.7197	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	8.223e-06	1.310e-09
X17_P10	1.510e-05	1.476e-09
X33_P10	3.027e-05	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.209e-05	3.538e-05	9.798e-05
B (output stable)	2.778e-05	4.228e-05	1.519e-04
C (output stable)	7.646e-05	1.301e-04	2.990e-04
A to Z	3.471e-03	6.149e-03	1.213e-02
B to Z	3.275e-03	5.787e-03	1.130e-02
C to Z	3.774e-03	6.655e-03	1.316e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

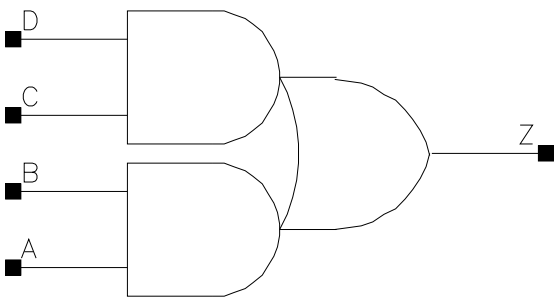
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	1.763e-05	3.141e-05	5.933e-05
B (output stable)	2.029e-05	3.165e-05	6.013e-05
C (output stable)	-2.809e-06	-3.082e-06	-6.771e-06
A to Z	-1.637e-07	-2.465e-07	-3.200e-07
B to Z	-3.550e-08	-1.317e-07	-5.613e-07
C to Z	-2.564e-07	3.863e-07	2.500e-08

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0011	0.0023
B	0.0008	0.0012	0.0021
C	0.0007	0.0011	0.0023
D	0.0008	0.0012	0.0022

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0429	0.0383	1.7825	0.8956
A to Z ↑	0.0296	0.0273	2.8876	1.4382
B to Z ↓	0.0398	0.0357	1.7726	0.8917
B to Z ↑	0.0311	0.0293	2.8879	1.4378

C to Z ↓	0.0392	0.0357	1.7748	0.8925
C to Z ↑	0.0250	0.0231	2.8808	1.4329
D to Z ↓	0.0372	0.0337	1.7682	0.8903
D to Z ↑	0.0272	0.0250	2.8817	1.4325
	X33_P10		**X33_P10**	
A to Z ↓	0.0366		0.4570	
A to Z ↑	0.0249		0.7262	
B to Z ↓	0.0345		0.4563	
B to Z ↑	0.0269		0.7264	
C to Z ↓	0.0340		0.4560	
C to Z ↑	0.0214		0.7244	
D to Z ↓	0.0320		0.4548	
D to Z ↑	0.0230		0.7242	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	8.770e-06	1.642e-09
X17_P10	1.621e-05	1.807e-09
X33_P10	2.999e-05	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	4.256e-05	6.184e-05	9.299e-05
B (output stable)	1.709e-04	2.079e-04	1.126e-04
C (output stable)	2.859e-05	4.578e-05	9.907e-05
D (output stable)	3.447e-05	5.765e-05	1.261e-04
A to Z	4.573e-03	7.817e-03	1.447e-02
B to Z	4.212e-03	7.313e-03	1.372e-02
C to Z	3.877e-03	6.717e-03	1.232e-02
D to Z	3.699e-03	6.380e-03	1.164e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

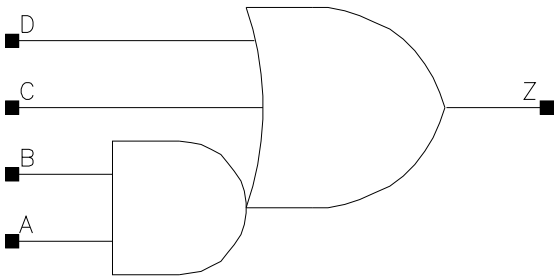
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-1.982e-07	-2.174e-07	-8.175e-07
B (output stable)	-1.292e-06	-2.477e-07	-8.503e-07
C (output stable)	9.430e-06	1.573e-05	3.856e-05
D (output stable)	9.322e-06	1.555e-05	3.889e-05
A to Z	-1.672e-07	-2.633e-08	-2.573e-07
B to Z	6.017e-08	1.543e-07	5.907e-07
C to Z	-1.442e-07	-2.427e-07	-1.919e-07
D to Z	-1.535e-07	-7.350e-08	-2.836e-07

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	0.952	1.1424
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0011	0.0021
B	0.0008	0.0011	0.0022
C	0.0008	0.0011	0.0022
D	0.0007	0.0012	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0495	0.0441	1.9339	0.9510
A to Z ↑	0.0247	0.0226	2.9175	1.4852
B to Z ↓	0.0471	0.0411	1.9256	0.9474
B to Z ↑	0.0267	0.0241	2.9196	1.4852
C to Z ↓	0.0515	0.0459	1.9239	0.9473
C to Z ↑	0.0237	0.0222	2.9004	1.4780

D to Z ↓	0.0512	0.0459	1.9250	0.9474
D to Z ↑	0.0234	0.0220	2.8998	1.4782
	X33_P10		**X33_P10**	
A to Z ↓	0.0448		0.4766	
A to Z ↑	0.0225		0.7246	
B to Z ↓	0.0403		0.4733	
B to Z ↑	0.0236		0.7247	
C to Z ↓	0.0471		0.4739	
C to Z ↑	0.0218		0.7211	
D to Z ↓	0.0460		0.4743	
D to Z ↑	0.0210		0.7202	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	8.609e-06	1.476e-09
X17_P10	1.613e-05	1.642e-09
X33_P10	3.295e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.364e-05	2.556e-05	8.429e-05
B (output stable)	1.698e-05	3.006e-05	1.365e-04
C (output stable)	8.095e-05	1.137e-04	3.226e-04
D (output stable)	1.875e-05	3.312e-05	9.186e-05
A to Z	3.887e-03	6.674e-03	1.343e-02
B to Z	3.707e-03	6.297e-03	1.230e-02
C to Z	4.429e-03	7.624e-03	1.548e-02
D to Z	4.179e-03	7.197e-03	1.431e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

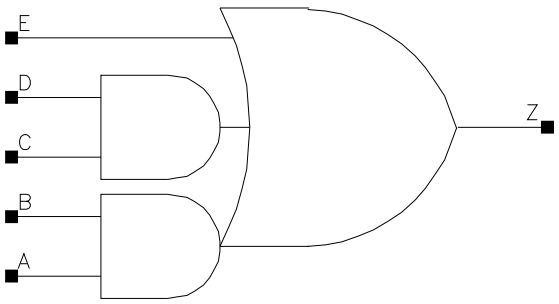
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	1.901e-05	3.897e-05	7.062e-05
B (output stable)	2.449e-05	4.651e-05	8.505e-05
C (output stable)	-8.462e-06	-9.212e-06	-2.624e-05
D (output stable)	1.123e-05	2.261e-05	7.464e-05
A to Z	-9.630e-08	-3.966e-07	-8.649e-07
B to Z	-2.405e-07	-1.714e-07	-8.361e-07
C to Z	-4.112e-07	4.567e-07	-6.360e-07
D to Z	-2.218e-07	2.000e-09	1.570e-07

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.088	1.3056
X17_P10	1.200	1.224	1.4688
X33_P10	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0011	0.0023
B	0.0008	0.0011	0.0021
C	0.0009	0.0014	0.0023
D	0.0008	0.0011	0.0022
E	0.0007	0.0011	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0604	0.0531	1.8528	0.9277
A to Z ↑	0.0312	0.0274	2.8659	1.4437

B to Z ↓	0.0581	0.0503	1.8444	0.9239
B to Z ↑	0.0339	0.0297	2.8643	1.4436
C to Z ↓	0.0513	0.0462	1.8442	0.9241
C to Z ↑	0.0262	0.0228	2.8450	1.4353
D to Z ↓	0.0476	0.0421	1.8324	0.9181
D to Z ↑	0.0282	0.0245	2.8434	1.4350
E to Z ↓	0.0530	0.0466	1.8326	0.9192
E to Z ↑	0.0248	0.0219	2.8252	1.4263
	X33_P10		**X33_P10**	
A to Z ↓	0.0518		0.4769	
A to Z ↑	0.0280		0.7291	
B to Z ↓	0.0486		0.4751	
B to Z ↑	0.0302		0.7288	
C to Z ↓	0.0445		0.4750	
C to Z ↑	0.0228		0.7240	
D to Z ↓	0.0408		0.4721	
D to Z ↑	0.0244		0.7236	
E to Z ↓	0.0455		0.4728	
E to Z ↑	0.0219		0.7196	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	1.014e-05	1.807e-09
X17_P10	1.865e-05	1.973e-09
X33_P10	3.431e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.892e-05	4.609e-05	1.027e-04
B (output stable)	3.555e-05	4.985e-05	1.313e-04
C (output stable)	3.149e-05	4.388e-05	1.111e-04
D (output stable)	3.892e-05	5.188e-05	1.459e-04
E (output stable)	7.564e-05	8.282e-05	2.051e-04
A to Z	5.346e-03	8.817e-03	1.718e-02
B to Z	5.159e-03	8.412e-03	1.620e-02
C to Z	4.210e-03	7.071e-03	1.359e-02
D to Z	3.994e-03	6.646e-03	1.267e-02
E to Z	4.570e-03	7.561e-03	1.457e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-2.045e-06	-1.866e-06	-4.566e-06
B (output stable)	-2.069e-06	-2.137e-06	-4.880e-06
C (output stable)	1.870e-05	3.538e-05	7.686e-05
D (output stable)	2.338e-05	3.870e-05	8.377e-05
E (output stable)	1.942e-05	3.654e-05	7.328e-05
A to Z	2.657e-07	1.014e-06	2.435e-06
B to Z	2.853e-07	1.032e-06	2.989e-06
C to Z	-1.024e-07	-2.402e-07	-7.126e-07
D to Z	-9.260e-08	-2.960e-07	-8.489e-07

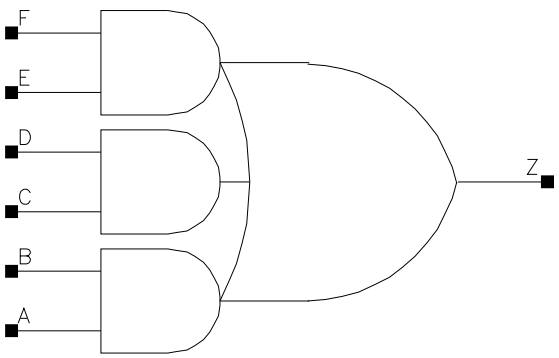
E to Z	-2.980e-07	-9.044e-08	-9.667e-09

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.360	1.6320
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
A	0.0007	0.0008	0.0011	0.0023

B	0.0008	0.0009	0.0014	0.0021
C	0.0007	0.0008	0.0011	0.0022
D	0.0007	0.0008	0.0011	0.0021
E	0.0008	0.0009	0.0011	0.0023
F	0.0008	0.0009	0.0012	0.0022

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0602	0.0575	3.4478	1.8506
A to Z ↑	0.0328	0.0320	5.5154	2.9182
B to Z ↓	0.0554	0.0533	3.4165	1.8360
B to Z ↑	0.0342	0.0338	5.5132	2.9177
C to Z ↓	0.0549	0.0528	3.4322	1.8436
C to Z ↑	0.0297	0.0289	5.4798	2.9006
D to Z ↓	0.0522	0.0503	3.4142	1.8352
D to Z ↑	0.0320	0.0314	5.4800	2.9012
E to Z ↓	0.0455	0.0450	3.4114	1.8346
E to Z ↑	0.0248	0.0243	5.4560	2.8893
F to Z ↓	0.0423	0.0419	3.3940	1.8251
F to Z ↑	0.0266	0.0262	5.4540	2.8889
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
A to Z ↓	0.0560	0.0537	0.9317	0.4755
A to Z ↑	0.0300	0.0301	1.4477	0.7313
B to Z ↓	0.0527	0.0507	0.9239	0.4738
B to Z ↑	0.0324	0.0322	1.4475	0.7309
C to Z ↓	0.0523	0.0502	0.9289	0.4750
C to Z ↑	0.0273	0.0279	1.4399	0.7274
D to Z ↓	0.0493	0.0474	0.9240	0.4733
D to Z ↑	0.0296	0.0299	1.4397	0.7274
E to Z ↓	0.0446	0.0449	0.9241	0.4732
E to Z ↑	0.0229	0.0239	1.4356	0.7257
F to Z ↓	0.0416	0.0415	0.9194	0.4708
F to Z ↑	0.0249	0.0259	1.4350	0.7256

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	8.403e-06	2.139e-09
X8_P10	1.209e-05	2.139e-09
X17_P10	1.974e-05	2.304e-09
X33_P10	3.548e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	6.945e-05	7.756e-05	8.991e-05	1.667e-04
B (output stable)	1.584e-04	1.713e-04	1.744e-04	2.185e-04
C (output stable)	3.503e-05	3.872e-05	4.713e-05	8.479e-05
D (output stable)	4.283e-05	4.852e-05	5.784e-05	1.492e-04
E (output stable)	5.585e-05	6.290e-05	7.651e-05	1.121e-04
F (output stable)	5.667e-05	6.484e-05	8.242e-05	1.543e-04

A to Z	4.683e-03	6.300e-03	9.765e-03	1.848e-02
B to Z	4.304e-03	5.848e-03	9.148e-03	1.750e-02
C to Z	3.958e-03	5.429e-03	8.596e-03	1.634e-02
D to Z	3.771e-03	5.186e-03	8.202e-03	1.547e-02
E to Z	3.168e-03	4.529e-03	7.284e-03	1.428e-02
F to Z	2.981e-03	4.282e-03	6.910e-03	1.343e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

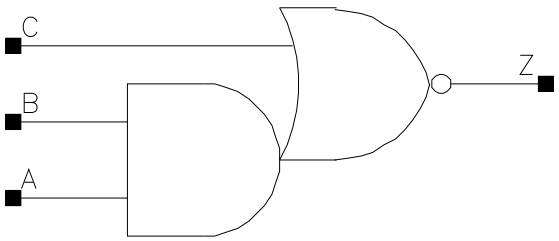
Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	-4.955e-06	-5.017e-06	-4.896e-06	-8.034e-06
B (output stable)	-5.213e-06	-4.998e-06	-3.368e-06	-8.098e-06
C (output stable)	6.183e-06	8.996e-06	1.513e-05	3.642e-05
D (output stable)	5.947e-06	8.508e-06	1.279e-05	3.231e-05
E (output stable)	2.921e-05	3.623e-05	5.035e-05	8.095e-05
F (output stable)	2.643e-05	3.303e-05	4.680e-05	7.753e-05
A to Z	-9.151e-07	-2.757e-07	6.021e-07	1.406e-06
B to Z	-7.167e-07	-1.032e-07	9.166e-07	1.850e-06
C to Z	-2.034e-07	1.469e-07	4.768e-07	2.820e-07
D to Z	-1.791e-07	2.228e-07	5.871e-07	3.217e-07
E to Z	-2.967e-07	-2.967e-07	-3.303e-07	-7.890e-07
F to Z	-3.249e-07	-3.409e-07	-3.541e-07	-7.715e-07

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008
X44_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X33_P10	X44_P10
A	0.0009	0.0028	0.0057	0.0076
B	0.0009	0.0027	0.0053	0.0072
C	0.0010	0.0030	0.0059	0.0077

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0078	0.0081	3.0431	1.0332
A to Z ↑	0.0182	0.0185	5.6165	1.8801
B to Z ↓	0.0081	0.0083	3.0828	1.0491
B to Z ↑	0.0148	0.0146	5.5406	1.8816
C to Z ↓	0.0087	0.0088	1.8379	0.6294
C to Z ↑	0.0182	0.0181	5.1217	1.7288
	X33_P10	**X44_P10**	**X33_P10**	**X44_P10**
A to Z ↓	0.0083	0.0082	0.5261	0.3988

A to Z ↑	0.0185	0.0185	0.9415	0.7144
B to Z ↓	0.0082	0.0082	0.5343	0.4053
B to Z ↑	0.0144	0.0144	0.9407	0.7117
C to Z ↓	0.0102	0.0104	0.3738	0.2902
C to Z ↑	0.0183	0.0182	0.8642	0.6546

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P10	6.242e-06	1.145e-09
X17_P10	1.717e-05	2.139e-09
X33_P10	3.191e-05	3.629e-09
X44_P10	4.216e-05	4.623e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	3.820e-05	1.196e-04	2.658e-04	3.459e-04
B (output stable)	4.482e-05	2.080e-04	4.732e-04	6.077e-04
C (output stable)	1.283e-04	3.976e-04	8.352e-04	1.117e-03
A to Z	1.609e-03	5.004e-03	1.001e-02	1.327e-02
B to Z	1.303e-03	3.759e-03	7.510e-03	9.935e-03
C to Z	2.238e-03	6.646e-03	1.334e-02	1.766e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

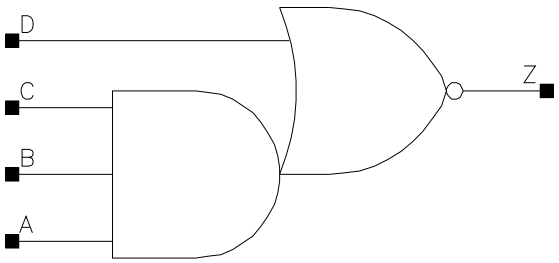
Pin Cycle (vdds)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	2.891e-05	6.880e-05	1.397e-04	1.804e-04
B (output stable)	2.904e-05	6.899e-05	1.401e-04	1.810e-04
C (output stable)	-2.868e-06	-6.576e-06	-1.459e-05	-1.860e-05
A to Z	2.303e-07	1.633e-06	3.113e-06	4.064e-06
B to Z	5.379e-07	1.653e-06	1.211e-06	-1.083e-06
C to Z	1.090e-06	1.582e-06	1.527e-06	1.393e-06

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X29_P10	1.200	3.536	4.2432
X38_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X29_P10	X38_P10
A	0.0010	0.0057	0.0075
B	0.0009	0.0055	0.0072
C	0.0009	0.0053	0.0069
D	0.0010	0.0060	0.0074

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X29_P10	X5_P10	X29_P10
A to Z ↓	0.0120	0.0129	4.2731	0.7411
A to Z ↑	0.0231	0.0233	5.6184	0.9321
B to Z ↓	0.0124	0.0127	4.2876	0.7449
B to Z ↑	0.0205	0.0204	5.6230	0.9391
C to Z ↓	0.0124	0.0122	4.3137	0.7504
C to Z ↑	0.0173	0.0168	5.5534	0.9463
D to Z ↓	0.0108	0.0126	1.8743	0.3760

D to Z ↑	0.0211	0.0213	4.7788	0.8019
	X38_P10		**X38_P10**	
A to Z ↓	0.0124		0.5732	
A to Z ↑	0.0225		0.7027	
B to Z ↓	0.0124		0.5765	
B to Z ↑	0.0198		0.7100	
C to Z ↓	0.0118		0.5808	
C to Z ↑	0.0160		0.7180	
D to Z ↓	0.0132		0.3117	
D to Z ↑	0.0207		0.6056	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P10	6.579e-06	1.310e-09
X29_P10	3.372e-05	4.789e-09
X38_P10	4.278e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P10	X29_P10	X38_P10
A (output stable)	2.667e-05	2.304e-04	2.953e-04
B (output stable)	4.515e-05	4.380e-04	5.554e-04
C (output stable)	8.224e-05	8.742e-04	1.121e-03
D (output stable)	1.757e-04	1.520e-03	1.939e-03
A to Z	2.304e-03	1.452e-02	1.819e-02
B to Z	1.973e-03	1.183e-02	1.485e-02
C to Z	1.660e-03	9.283e-03	1.144e-02
D to Z	2.893e-03	1.746e-02	2.225e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

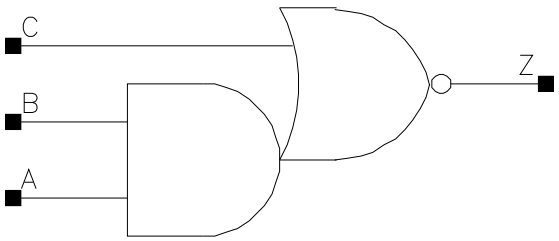
Pin Cycle (vdds)	X5_P10	X29_P10	X38_P10
A (output stable)	1.461e-05	9.971e-05	1.289e-04
B (output stable)	1.310e-05	8.961e-05	1.189e-04
C (output stable)	1.358e-05	9.018e-05	1.170e-04
D (output stable)	-5.133e-06	-7.955e-05	-9.685e-05
A to Z	1.560e-07	1.300e-08	-1.200e-07
B to Z	3.000e-08	-1.199e-06	-1.898e-06
C to Z	-8.100e-08	-1.311e-06	-1.489e-06
D to Z	5.516e-07	-3.500e-07	-1.934e-06

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X11_P10	1.200	1.088	1.3056
X16_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X11_P10	X16_P10	X23_P10
A	0.0010	0.0021	0.0030	0.0040
B	0.0010	0.0020	0.0029	0.0038
C	0.0010	0.0019	0.0027	0.0039
	X46_P10			
A	0.0078			
B	0.0075			
C	0.0076			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X11_P10	X6_P10	X11_P10
A to Z ↓	0.0098	0.0107	2.9421	1.4956
A to Z ↑	0.0198	0.0209	5.6017	2.7411
B to Z ↓	0.0107	0.0110	2.9778	1.5152

B to Z ↑	0.0170	0.0175	5.5384	2.7505
C to Z ↓	0.0053	0.0059	1.8935	1.1093
C to Z ↑	0.0148	0.0144	5.1544	2.5425
	X16_P10	**X23_P10**	**X16_P10**	**X23_P10**
A to Z ↓	0.0101	0.0104	1.0318	0.7766
A to Z ↑	0.0196	0.0199	1.8437	1.3970
B to Z ↓	0.0109	0.0108	1.0464	0.7866
B to Z ↑	0.0162	0.0164	1.8435	1.4024
C to Z ↓	0.0060	0.0050	0.7698	0.4860
C to Z ↑	0.0139	0.0143	1.7093	1.2952
	X46_P10		**X46_P10**	
A to Z ↓	0.0100		0.3988	
A to Z ↑	0.0193		0.7243	
B to Z ↓	0.0106		0.4043	
B to Z ↑	0.0157		0.7228	
C to Z ↓	0.0053		0.2487	
C to Z ↑	0.0143		0.6700	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P10	6.309e-06	1.145e-09
X11_P10	1.231e-05	1.807e-09
X16_P10	1.649e-05	2.139e-09
X23_P10	2.406e-05	2.801e-09
X46_P10	4.582e-05	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	3.695e-05	1.010e-04	1.315e-04	1.848e-04
B (output stable)	4.513e-05	1.897e-04	2.007e-04	3.188e-04
C (output stable)	1.134e-04	2.693e-04	3.478e-04	5.260e-04
A to Z	2.255e-03	4.961e-03	6.751e-03	9.223e-03
B to Z	1.922e-03	4.023e-03	5.437e-03	7.379e-03
C to Z	1.317e-03	2.645e-03	3.699e-03	5.175e-03
	X46_P10			
A (output stable)	3.399e-04			
B (output stable)	5.325e-04			
C (output stable)	8.717e-04			
A to Z	1.718e-02			
B to Z	1.373e-02			
C to Z	9.738e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	-3.925e-07	-1.434e-06	-9.734e-07	-1.510e-06
B (output stable)	-3.709e-07	-1.469e-06	-1.052e-06	-1.813e-06
C (output stable)	7.500e-05	2.015e-04	1.719e-04	2.406e-04
A to Z	1.667e-06	2.567e-06	3.739e-06	3.937e-06
B to Z	1.004e-06	1.642e-06	2.073e-06	2.666e-06
C to Z	6.711e-07	-3.023e-08	4.567e-07	6.157e-07

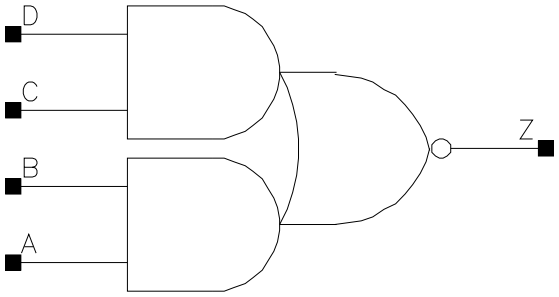
	X46_P10			
A (output stable)	-2.182e-06			
B (output stable)	-2.564e-06			
C (output stable)	4.304e-04			
A to Z	1.053e-05			
B to Z	5.640e-06			
C to Z	2.038e-06			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P10	X10_P10	X16_P10	X21_P10
A	0.0008	0.0021	0.0031	0.0040
B	0.0008	0.0019	0.0029	0.0038
C	0.0008	0.0020	0.0028	0.0038
D	0.0008	0.0018	0.0027	0.0036
	X42_P10			
A	0.0080			
B	0.0076			
C	0.0077			
D	0.0073			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X10_P10**	**X4_P10**	**X10_P10**
A to Z ↓	0.0113	0.0112	3.6329	1.4384
A to Z ↑	0.0256	0.0218	7.5764	2.5270
B to Z ↓	0.0126	0.0126	3.6798	1.4582
B to Z ↑	0.0226	0.0196	7.5595	2.5867
C to Z ↓	0.0080	0.0076	3.7199	1.4476
C to Z ↑	0.0209	0.0183	7.5795	2.5439
D to Z ↓	0.0086	0.0083	3.7796	1.4732
D to Z ↑	0.0176	0.0156	7.5634	2.5806
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0123	0.0122	1.0362	0.7791
A to Z ↑	0.0229	0.0227	1.7027	1.3155
B to Z ↓	0.0134	0.0129	1.0483	0.7888
B to Z ↑	0.0197	0.0194	1.7036	1.3182
C to Z ↓	0.0082	0.0083	1.0364	0.7802
C to Z ↑	0.0188	0.0192	1.7053	1.3154
D to Z ↓	0.0086	0.0084	1.0533	0.7935
D to Z ↑	0.0153	0.0155	1.7094	1.3186
	X42_P10		**X42_P10**	
A to Z ↓	0.0129		0.4045	
A to Z ↑	0.0232		0.6602	
B to Z ↓	0.0136		0.4095	
B to Z ↑	0.0197		0.6580	
C to Z ↓	0.0090		0.4003	
C to Z ↑	0.0194		0.6615	
D to Z ↓	0.0091		0.4069	
D to Z ↑	0.0158		0.6600	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	6.072e-06	1.310e-09
X10_P10	1.552e-05	2.139e-09
X16_P10	2.126e-05	2.635e-09
X21_P10	2.882e-05	3.464e-09
X42_P10	5.574e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	3.811e-05	8.922e-05	1.709e-04	2.285e-04
B (output stable)	4.585e-05	1.132e-04	3.363e-04	4.919e-04
C (output stable)	3.853e-05	9.691e-05	1.737e-04	2.312e-04
D (output stable)	4.886e-05	1.238e-04	3.348e-04	5.033e-04
A to Z	2.300e-03	5.607e-03	8.854e-03	1.144e-02
B to Z	2.002e-03	4.894e-03	7.465e-03	9.572e-03
C to Z	1.412e-03	3.563e-03	5.483e-03	7.357e-03
D to Z	1.159e-03	2.931e-03	4.233e-03	5.667e-03
	X42_P10			
A (output stable)	4.443e-04			
B (output stable)	8.923e-04			
C (output stable)	4.507e-04			
D (output stable)	9.107e-04			

A to Z	2.278e-02			
B to Z	1.912e-02			
C to Z	1.453e-02			
D to Z	1.127e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

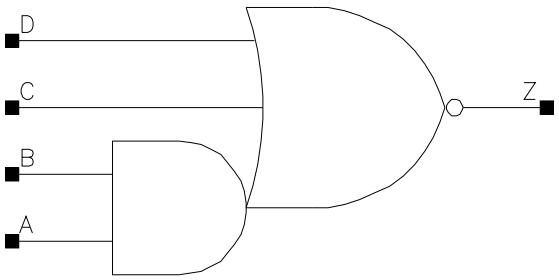
Pin Cycle (vdds)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	-7.258e-07	-8.817e-07	-1.615e-06	-1.675e-06
B (output stable)	-7.027e-07	-8.597e-07	-1.719e-06	-2.375e-06
C (output stable)	2.152e-05	3.817e-05	6.249e-05	7.569e-05
D (output stable)	2.158e-05	3.852e-05	6.250e-05	7.448e-05
A to Z	7.013e-07	1.984e-06	3.404e-06	3.306e-06
B to Z	8.267e-07	1.883e-06	3.445e-06	3.153e-06
C to Z	1.874e-07	4.803e-07	5.897e-07	9.023e-07
D to Z	1.433e-07	7.737e-07	1.181e-06	1.630e-06
	X42_P10			
A (output stable)	-3.398e-06			
B (output stable)	-4.751e-06			
C (output stable)	1.396e-04			
D (output stable)	1.383e-04			
A to Z	5.157e-06			
B to Z	4.433e-06			
C to Z	2.478e-06			
D to Z	2.065e-06			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X35_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P10	X35_P10
A	0.0009	0.0072
B	0.0009	0.0068
C	0.0010	0.0071
D	0.0010	0.0066

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X35_P10	X5_P10	X35_P10
A to Z ↓	0.0093	0.0098	3.0727	0.4533
A to Z ↑	0.0238	0.0225	8.2715	1.0589
B to Z ↓	0.0100	0.0102	3.1184	0.4611
B to Z ↑	0.0197	0.0179	8.2190	1.0587
C to Z ↓	0.0109	0.0147	1.9531	0.3731
C to Z ↑	0.0264	0.0261	7.8025	1.0003
D to Z ↓	0.0103	0.0134	1.9665	0.3726

D to Z ↑	0.0259	0.0245	7.8139	1.0030

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P10	5.568e-06	1.310e-09
X35_P10	3.343e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P10	X35_P10
A (output stable)	2.586e-05	2.658e-04
B (output stable)	3.125e-05	3.730e-04
C (output stable)	1.116e-04	1.169e-03
D (output stable)	3.200e-05	3.366e-04
A to Z	1.877e-03	1.373e-02
B to Z	1.556e-03	1.070e-02
C to Z	2.965e-03	2.297e-02
D to Z	2.506e-03	1.828e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

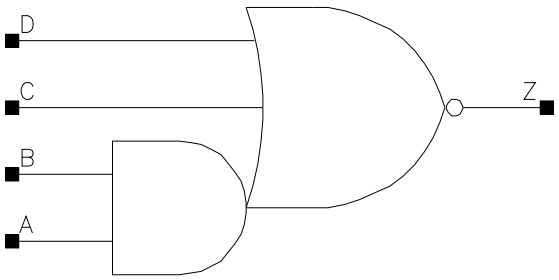
Pin Cycle (vdds)	X5_P10	X35_P10
A (output stable)	3.733e-05	2.323e-04
B (output stable)	4.428e-05	2.688e-04
C (output stable)	-9.092e-06	-7.157e-05
D (output stable)	2.160e-05	1.906e-04
A to Z	1.617e-07	1.218e-06
B to Z	-7.120e-08	-2.250e-07
C to Z	6.103e-07	-4.700e-07
D to Z	5.003e-07	4.077e-06

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X17_P10	1.200	2.448	2.9376
X34_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P10	X17_P10	X34_P10
A	0.0010	0.0040	0.0080
B	0.0010	0.0038	0.0076
C	0.0009	0.0034	0.0067
D	0.0009	0.0032	0.0063

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X17_P10	X4_P10	X17_P10
A to Z ↓	0.0117	0.0128	3.3327	0.8798
A to Z ↑	0.0269	0.0282	8.3124	2.0519
B to Z ↓	0.0132	0.0137	3.3764	0.8907
B to Z ↑	0.0234	0.0239	8.2402	2.0563
C to Z ↓	0.0116	0.0114	3.0609	0.7462
C to Z ↑	0.0197	0.0209	7.8381	1.9438

D to Z ↓	0.0092	0.0083	3.1364	0.7524
D to Z ↑	0.0179	0.0166	7.8660	1.9517
	X34_P10		**X34_P10**	
A to Z ↓	0.0126		0.4512	
A to Z ↑	0.0278		1.0452	
B to Z ↓	0.0138		0.4565	
B to Z ↑	0.0235		1.0423	
C to Z ↓	0.0117		0.3972	
C to Z ↑	0.0204		0.9881	
D to Z ↓	0.0085		0.4018	
D to Z ↑	0.0163		0.9923	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	4.602e-06	1.310e-09
X17_P10	1.785e-05	3.464e-09
X34_P10	3.389e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P10	X17_P10	X34_P10
A (output stable)	4.107e-05	1.967e-04	3.891e-04
B (output stable)	4.348e-05	2.631e-04	4.963e-04
C (output stable)	1.864e-05	2.047e-04	3.736e-04
D (output stable)	4.061e-05	3.455e-04	6.329e-04
A to Z	2.801e-03	1.210e-02	2.345e-02
B to Z	2.482e-03	1.027e-02	1.999e-02
C to Z	1.742e-03	7.557e-03	1.444e-02
D to Z	1.287e-03	4.939e-03	9.407e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

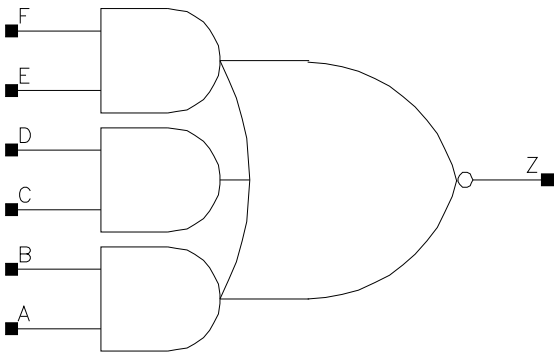
Pin Cycle (vdds)	X4_P10	X17_P10	X34_P10
A (output stable)	-1.704e-06	-7.916e-06	-1.497e-05
B (output stable)	-1.727e-06	-9.257e-06	-1.671e-05
C (output stable)	2.615e-05	7.608e-05	1.536e-04
D (output stable)	4.542e-05	2.512e-04	4.547e-04
A to Z	1.211e-06	6.101e-06	1.218e-05
B to Z	1.299e-06	6.008e-06	1.234e-05
C to Z	1.300e-07	8.920e-07	1.630e-06
D to Z	8.507e-08	4.627e-07	1.570e-06

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X8_P10	1.200	2.176	2.6112
X13_P10	1.200	2.720	3.2640
X17_P10	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P10	X8_P10	X13_P10	X17_P10
A	0.0010	0.0020	0.0030	0.0039

B	0.0010	0.0019	0.0028	0.0037
C	0.0010	0.0019	0.0028	0.0037
D	0.0009	0.0018	0.0027	0.0035
E	0.0011	0.0018	0.0027	0.0036
F	0.0009	0.0017	0.0026	0.0034

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0141	0.0173	2.9521	1.7064
A to Z ↑	0.0383	0.0377	7.9584	3.6958
B to Z ↓	0.0161	0.0186	2.9866	1.7210
B to Z ↑	0.0347	0.0338	7.9566	3.7058
C to Z ↓	0.0128	0.0153	2.9258	1.7181
C to Z ↑	0.0337	0.0338	7.9933	3.7071
D to Z ↓	0.0144	0.0168	2.9688	1.7377
D to Z ↑	0.0301	0.0299	7.9604	3.7083
E to Z ↓	0.0091	0.0111	2.8916	1.7208
E to Z ↑	0.0261	0.0260	7.9220	3.6859
F to Z ↓	0.0099	0.0118	2.9497	1.7501
F to Z ↑	0.0225	0.0220	7.9791	3.6928
	X13_P10	**X17_P10**	**X13_P10**	**X17_P10**
A to Z ↓	0.0165	0.0166	1.1599	0.8843
A to Z ↑	0.0351	0.0352	2.4431	1.8693
B to Z ↓	0.0183	0.0181	1.1695	0.8918
B to Z ↑	0.0316	0.0313	2.4527	1.8709
C to Z ↓	0.0147	0.0147	1.1656	0.8751
C to Z ↑	0.0312	0.0315	2.4543	1.8796
D to Z ↓	0.0164	0.0158	1.1781	0.8852
D to Z ↑	0.0278	0.0276	2.4588	1.8772
E to Z ↓	0.0107	0.0106	1.1628	0.8775
E to Z ↑	0.0246	0.0247	2.4445	1.8646
F to Z ↓	0.0115	0.0109	1.1811	0.8917
F to Z ↑	0.0208	0.0206	2.4503	1.8733

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	9.615e-06	1.807e-09
X8_P10	1.812e-05	3.132e-09
X13_P10	2.483e-05	3.795e-09
X17_P10	3.329e-05	4.954e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

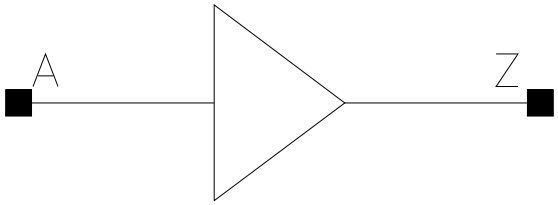
Pin Cycle (vdd)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	8.562e-05	1.922e-04	2.587e-04	3.424e-04
B (output stable)	9.427e-05	2.995e-04	3.412e-04	5.141e-04
C (output stable)	4.416e-05	1.010e-04	1.384e-04	1.975e-04
D (output stable)	5.522e-05	2.238e-04	2.329e-04	3.889e-04
E (output stable)	5.294e-05	1.309e-04	1.926e-04	2.624e-04
F (output stable)	6.168e-05	2.295e-04	2.764e-04	4.342e-04

A to Z	4.404e-03	9.248e-03	1.286e-02	1.698e-02
B to Z	4.028e-03	8.300e-03	1.162e-02	1.515e-02
C to Z	3.314e-03	7.186e-03	9.746e-03	1.291e-02
D to Z	2.974e-03	6.329e-03	8.624e-03	1.122e-02
E to Z	2.169e-03	4.794e-03	6.550e-03	8.653e-03
F to Z	1.856e-03	3.988e-03	5.448e-03	7.072e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	-6.594e-06	-1.359e-05	-1.292e-05	-1.714e-05
B (output stable)	-7.225e-06	-1.394e-05	-1.336e-05	-1.833e-05
C (output stable)	2.067e-05	3.942e-05	4.699e-05	6.273e-05
D (output stable)	1.958e-05	3.480e-05	4.222e-05	5.522e-05
E (output stable)	5.525e-05	1.227e-04	1.256e-04	1.733e-04
F (output stable)	5.182e-05	1.152e-04	1.193e-04	1.634e-04
A to Z	1.225e-06	2.703e-06	2.396e-06	3.994e-06
B to Z	1.344e-06	3.336e-06	4.033e-06	4.331e-06
C to Z	8.969e-07	1.182e-06	1.108e-06	2.064e-06
D to Z	9.376e-07	1.883e-06	2.528e-06	3.095e-06
E to Z	-2.155e-07	-2.246e-07	1.681e-07	4.367e-08
F to Z	-3.323e-07	-8.166e-07	-7.733e-07	-1.163e-06

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.408	0.4896
X6_P10	1.200	0.408	0.4896
X8_P10	1.200	0.408	0.4896
X13_P10	1.200	0.544	0.6528
X16_P10	1.200	0.544	0.6528
X21_P10	1.200	0.680	0.8160
X25_P10	1.200	0.680	0.8160
X29_P10	1.200	0.952	1.1424
X33_P10	1.200	0.952	1.1424
X42_P10	1.200	1.088	1.3056
X50_P10	1.200	1.224	1.4688
X58_P10	1.200	1.496	1.7952
X67_P10	1.200	1.632	1.9584
X75_P10	1.200	1.768	2.1216
X84_P10	1.200	1.904	2.2848
X100_P10	1.200	2.312	2.7744
X134_P10	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0009	0.0009	0.0009	0.0009
	X16_P10	X21_P10	X25_P10	X29_P10
A	0.0009	0.0013	0.0013	0.0017
	X33_P10	X42_P10	X50_P10	X58_P10
A	0.0017	0.0020	0.0023	0.0034

	X67_P10	X75_P10	X84_P10	X100_P10
A	0.0035	0.0034	0.0034	0.0045
	X134_P10			
A	0.0056			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0237	0.0239	3.1754	2.3563
A to Z ↑	0.0173	0.0174	5.4019	4.0274
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0250	0.0284	1.7644	1.1309
A to Z ↑	0.0182	0.0208	2.9171	1.8886
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0309	0.0260	0.9063	0.6950
A to Z ↑	0.0224	0.0191	1.4635	1.1391
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0275	0.0260	0.6001	0.5054
A to Z ↑	0.0201	0.0185	0.9628	0.8155
	X33_P10	**X42_P10**	**X33_P10**	**X42_P10**
A to Z ↓	0.0271	0.0267	0.4494	0.3644
A to Z ↑	0.0193	0.0196	0.7202	0.5792
	X50_P10	**X58_P10**	**X50_P10**	**X58_P10**
A to Z ↓	0.0261	0.0240	0.3024	0.2608
A to Z ↑	0.0191	0.0177	0.4810	0.4136
	X67_P10	**X75_P10**	**X67_P10**	**X75_P10**
A to Z ↓	0.0256	0.0268	0.2291	0.2069
A to Z ↑	0.0188	0.0198	0.3623	0.3242
	X84_P10	**X100_P10**	**X84_P10**	**X100_P10**
A to Z ↓	0.0281	0.0265	0.1873	0.1577
A to Z ↑	0.0207	0.0196	0.2929	0.2452
	X134_P10		**X134_P10**	
A to Z ↓	0.0277		0.1227	
A to Z ↑	0.0208		0.1876	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	5.084e-06	9.792e-10
X6_P10	6.066e-06	9.792e-10
X8_P10	7.187e-06	9.792e-10
X13_P10	9.407e-06	1.145e-09
X16_P10	1.123e-05	1.145e-09
X21_P10	1.509e-05	1.310e-09
X25_P10	1.649e-05	1.310e-09
X29_P10	1.992e-05	1.642e-09
X33_P10	2.095e-05	1.642e-09
X42_P10	2.564e-05	1.807e-09
X50_P10	3.064e-05	1.973e-09
X58_P10	3.772e-05	2.304e-09
X67_P10	4.127e-05	2.470e-09
X75_P10	4.482e-05	2.635e-09

X84_P10	4.836e-05	2.801e-09
X100_P10	5.900e-05	3.298e-09
X134_P10	7.673e-05	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	2.249e-03	2.534e-03	3.024e-03	4.139e-03
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	5.104e-03	6.720e-03	7.636e-03	8.628e-03
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	9.553e-03	1.197e-02	1.405e-02	1.673e-02
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	1.899e-02	2.127e-02	2.363e-02	2.831e-02
	X134_P10			
A to Z	3.889e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

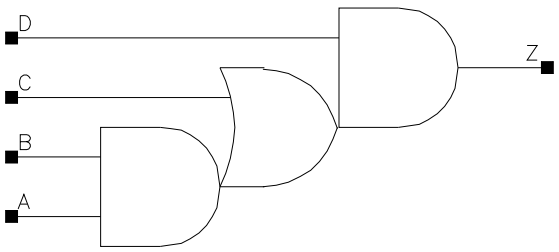
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	6.709e-07	6.152e-07	5.445e-07	3.849e-08
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	-6.000e-10	3.554e-07	2.742e-07	2.479e-07
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	2.051e-07	1.610e-07	1.370e-07	9.650e-07
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	1.886e-07	1.400e-07	7.200e-08	1.260e-07
	X134_P10			
A to Z	2.840e-07			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.632	1.9584
X25_P10	1.200	1.768	2.1216
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0011	0.0024	0.0024	0.0023
B	0.0011	0.0022	0.0022	0.0021
C	0.0012	0.0026	0.0026	0.0026
D	0.0017	0.0023	0.0023	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0327	0.0312	1.8039	0.8930
A to Z ↑	0.0277	0.0263	2.9562	1.4409
B to Z ↓	0.0300	0.0282	1.7985	0.8916
B to Z ↑	0.0283	0.0264	2.9552	1.4417
C to Z ↓	0.0281	0.0262	1.7957	0.8894
C to Z ↑	0.0208	0.0191	2.9329	1.4290

D to Z ↓	0.0273	0.0244	1.7763	0.8809
D to Z ↑	0.0237	0.0208	2.9376	1.4322
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0343	0.0365	0.6080	0.4586
A to Z ↑	0.0290	0.0307	0.9742	0.7328
B to Z ↓	0.0315	0.0342	0.6062	0.4579
B to Z ↑	0.0293	0.0315	0.9746	0.7324
C to Z ↓	0.0294	0.0321	0.6044	0.4558
C to Z ↑	0.0215	0.0233	0.9654	0.7250
D to Z ↓	0.0265	0.0279	0.5969	0.4483
D to Z ↑	0.0229	0.0244	0.9675	0.7263

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	1.035e-05	1.642e-09
X17_P10	1.928e-05	2.470e-09
X25_P10	2.221e-05	2.635e-09
X33_P10	2.514e-05	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	1.208e-04	2.509e-04	2.528e-04	2.282e-04
B (output stable)	1.478e-04	3.186e-04	3.206e-04	2.768e-04
C (output stable)	3.674e-04	5.969e-04	6.081e-04	5.711e-04
D (output stable)	1.293e-04	1.930e-04	1.945e-04	1.931e-04
A to Z	5.042e-03	9.365e-03	1.183e-02	1.405e-02
B to Z	4.665e-03	8.415e-03	1.085e-02	1.324e-02
C to Z	3.970e-03	6.979e-03	9.308e-03	1.149e-02
D to Z	5.114e-03	9.027e-03	1.128e-02	1.325e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

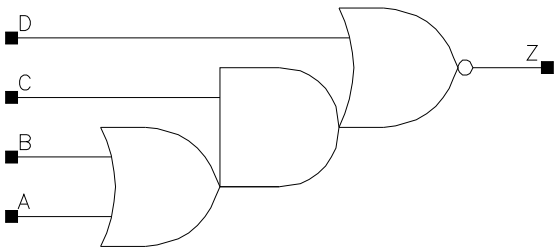
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	-7.062e-07	-1.387e-06	-1.393e-06	-1.217e-06
B (output stable)	-6.860e-07	-1.319e-06	-1.321e-06	-1.193e-06
C (output stable)	1.509e-05	2.558e-05	2.581e-05	2.595e-05
D (output stable)	5.827e-08	2.200e-09	1.307e-08	4.187e-08
A to Z	5.300e-08	-5.000e-08	-1.320e-07	-4.640e-07
B to Z	5.580e-07	3.900e-07	5.300e-07	5.510e-07
C to Z	6.403e-08	7.367e-08	-1.330e-07	-2.264e-07
D to Z	3.728e-08	4.099e-07	5.177e-08	2.075e-07

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.952	1.1424
X11_P10	1.200	1.496	1.7952
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X16_P10	X21_P10
A	0.0011	0.0020	0.0030	0.0040
B	0.0010	0.0019	0.0030	0.0039
C	0.0010	0.0019	0.0029	0.0039
D	0.0013	0.0020	0.0029	0.0039

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0123	0.0117	2.9054	1.5273
A to Z ↑	0.0320	0.0299	8.1575	4.2493
B to Z ↓	0.0117	0.0114	2.8298	1.4982
B to Z ↑	0.0304	0.0289	8.1668	4.2550
C to Z ↓	0.0114	0.0109	2.7068	1.4234
C to Z ↑	0.0194	0.0180	5.5067	2.8287

D to Z ↓	0.0061	0.0049	1.8372	0.9279
D to Z ↑	0.0178	0.0158	5.8968	3.0364
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0117	0.0120	1.0276	0.7920
A to Z ↑	0.0278	0.0293	2.7281	2.1065
B to Z ↓	0.0109	0.0114	1.0338	0.7934
B to Z ↑	0.0273	0.0283	2.7308	2.1090
C to Z ↓	0.0110	0.0112	0.9757	0.7479
C to Z ↑	0.0173	0.0176	1.8698	1.4033
D to Z ↓	0.0050	0.0050	0.6451	0.4915
D to Z ↑	0.0148	0.0148	1.9902	1.5065

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P10	7.659e-06	1.642e-09
X11_P10	1.424e-05	2.304e-09
X16_P10	1.899e-05	2.635e-09
X21_P10	2.553e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	4.859e-05	8.892e-05	1.159e-04	1.857e-04
B (output stable)	1.374e-06	1.808e-06	-7.713e-06	4.359e-07
C (output stable)	1.356e-04	2.683e-04	3.515e-04	5.231e-04
D (output stable)	1.194e-04	2.431e-04	3.293e-04	4.880e-04
A to Z	3.522e-03	6.237e-03	8.753e-03	1.223e-02
B to Z	2.859e-03	5.118e-03	7.347e-03	1.003e-02
C to Z	2.432e-03	4.241e-03	6.090e-03	8.366e-03
D to Z	1.557e-03	2.720e-03	3.761e-03	5.007e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

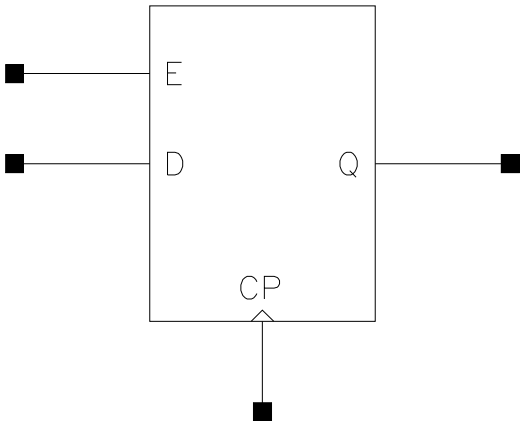
Pin Cycle (vdds)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	-2.299e-06	-3.299e-06	-3.536e-06	-6.951e-06
B (output stable)	1.632e-05	2.324e-05	3.340e-05	5.265e-05
C (output stable)	-4.166e-06	-6.414e-06	-6.909e-06	-1.385e-05
D (output stable)	9.096e-05	1.913e-04	2.413e-04	3.706e-04
A to Z	1.412e-06	2.314e-06	3.759e-06	4.873e-06
B to Z	4.650e-07	1.174e-06	6.490e-07	1.652e-06
C to Z	1.360e-06	2.773e-06	3.487e-06	8.894e-06
D to Z	3.205e-07	9.466e-07	1.144e-06	5.430e-07

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.128	3.7536
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008
E	0.0013	0.0013	0.0009

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0372	0.0433	1.7986	0.9299
CP to Q ↑	0.0456	0.0492	2.9647	1.4845
	X33_P10		**X33_P10**	
CP to Q ↓	0.0655		0.4555	
CP to Q ↑	0.0791		0.7359	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0508	0.0508	0.0508
CP ↑	min_pulse_width to CP	0.0301	0.0349	0.0253
D ↓	hold_rising to CP	-0.0166	-0.0166	-0.0166
D ↑	hold_rising to CP	-0.0016	0.0009	-0.0016
D ↓	setup_rising to CP	0.0512	0.0512	0.0512
D ↑	setup_rising to CP	0.0295	0.0295	0.0295
E ↓	hold_rising to CP	-0.0112	-0.0112	-0.0112
E ↑	hold_rising to CP	-0.0015	-0.0015	-0.0015
E ↓	setup_rising to CP	0.0531	0.0531	0.0531
E ↑	setup_rising to CP	0.0539	0.0539	0.0539

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	3.059e-05	4.126e-09
X17_P10	3.447e-05	4.292e-09
X33_P10	4.663e-05	4.954e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

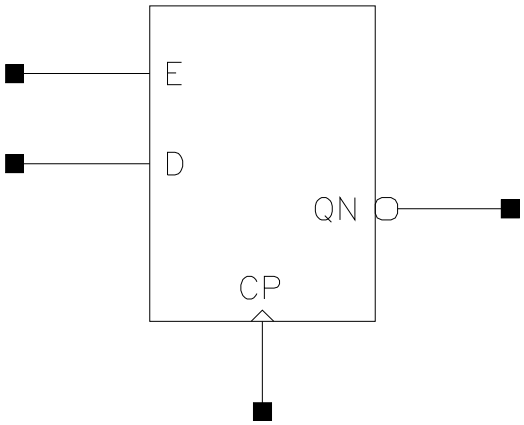
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.291e-03	5.292e-03	5.298e-03
Clock 100Mhz Data 25Mhz	1.136e-02	1.256e-02	1.612e-02
Clock 100Mhz Data 50Mhz	1.742e-02	1.982e-02	2.695e-02
Clock = 0 Data 100Mhz	6.888e-03	6.890e-03	6.890e-03
Clock = 1 Data 100Mhz	1.880e-03	1.880e-03	1.880e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.264	3.9168
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008
E	0.0009	0.0013	0.0013

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0637	0.0604	1.8447	0.8799
CP to QN ↑	0.0502	0.0517	2.9984	1.4439
	X33_P10		**X33_P10**	
CP to QN ↓	0.0651		0.4568	
CP to QN ↑	0.0575		0.7372	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0508	0.0508	0.0508
CP ↑	min_pulse_width to CP	0.0253	0.0290	0.0301
D ↓	hold_rising to CP	-0.0166	-0.0166	-0.0166
D ↑	hold_rising to CP	-0.0016	-0.0016	0.0009
D ↓	setup_rising to CP	0.0512	0.0512	0.0512
D ↑	setup_rising to CP	0.0295	0.0295	0.0295
E ↓	hold_rising to CP	-0.0112	-0.0112	-0.0112
E ↑	hold_rising to CP	-0.0015	-0.0015	-0.0015
E ↓	setup_rising to CP	0.0531	0.0531	0.0531
E ↑	setup_rising to CP	0.0539	0.0539	0.0539

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	3.039e-05	4.126e-09
X17_P10	3.639e-05	4.457e-09
X33_P10	4.568e-05	4.954e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

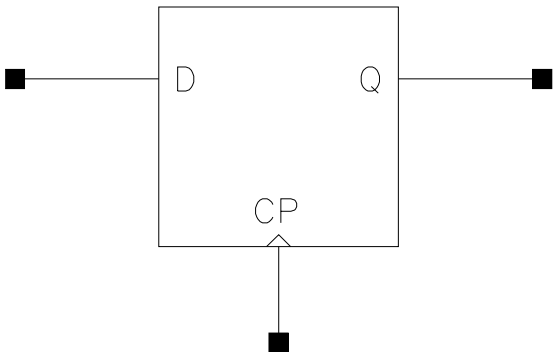
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.287e-03	5.288e-03	5.289e-03
Clock 100Mhz Data 25Mhz	1.140e-02	1.305e-02	1.596e-02
Clock 100Mhz Data 50Mhz	1.751e-02	2.081e-02	2.662e-02
Clock = 0 Data 100Mhz	6.890e-03	6.892e-03	6.892e-03
Clock = 1 Data 100Mhz	1.880e-03	1.880e-03	1.880e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.176	2.6112
X17_P10	1.200	2.448	2.9376
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0387	0.0433	1.7926	0.9222
CP to Q ↑	0.0459	0.0513	2.8756	1.4589
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to Q ↓	0.0558	0.0584	0.5478	0.4984
CP to Q ↑	0.0588	0.0600	0.8171	0.7478

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0460	0.0497	0.0508	0.0497
CP ↑	min_pulse_width to CP	0.0290	0.0338	0.0483	0.0483
D ↓	hold_rising to CP	0.0078	0.0078	0.0078	0.0078
D ↑	hold_rising to CP	0.0128	0.0128	0.0128	0.0128
D ↓	setup_rising to CP	0.0269	0.0269	0.0269	0.0269
D ↑	setup_rising to CP	0.0119	0.0119	0.0119	0.0119

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	2.481e-05	3.132e-09
X17_P10	2.889e-05	3.464e-09
X30_P10	3.527e-05	3.795e-09
X33_P10	3.613e-05	3.795e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

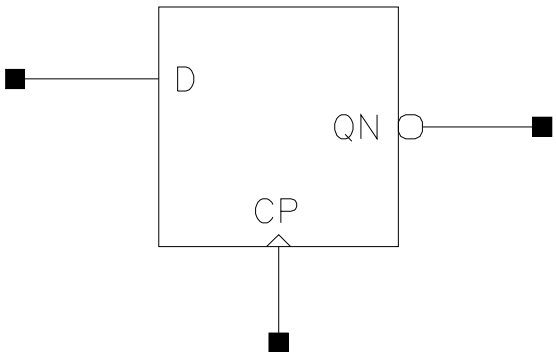
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.515e-03	5.547e-03	5.560e-03	5.565e-03
Clock 100Mhz Data 25Mhz	1.003e-02	1.165e-02	1.451e-02	1.520e-02
Clock 100Mhz Data 50Mhz	1.455e-02	1.776e-02	2.346e-02	2.484e-02
Clock = 0 Data 100Mhz	4.634e-03	4.773e-03	4.816e-03	4.838e-03
Clock = 1 Data 100Mhz	3.214e-05	3.221e-05	3.227e-05	3.233e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0375	0.0439	1.8457	0.9531
CP to QN ↑	0.0396	0.0425	2.8741	1.4591
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to QN ↓	0.0647	0.0650	0.5027	0.4555
CP to QN ↑	0.0533	0.0612	0.7919	0.7358

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0422	0.0422	0.0497	0.0460
CP ↑	min_pulse_width to CP	0.0290	0.0338	0.0290	0.0338
D ↓	hold_rising to CP	0.0127	0.0127	0.0078	0.0078
D ↑	hold_rising to CP	0.0121	0.0152	0.0128	0.0125
D ↓	setup_rising to CP	0.0220	0.0220	0.0269	0.0269
D ↑	setup_rising to CP	0.0145	0.0145	0.0119	0.0119

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	2.294e-05	2.801e-09
X17_P10	2.691e-05	2.967e-09
X30_P10	3.760e-05	3.795e-09
X33_P10	3.996e-05	3.961e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

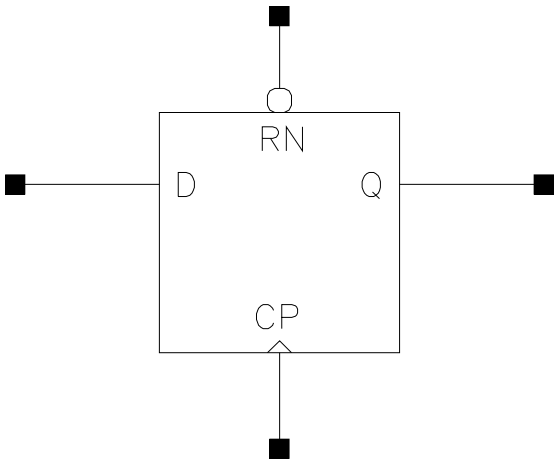
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.330e-03	5.332e-03	5.410e-03	5.443e-03
Clock 100Mhz Data 25Mhz	9.537e-03	1.081e-02	1.383e-02	1.460e-02
Clock 100Mhz Data 50Mhz	1.374e-02	1.628e-02	2.225e-02	2.376e-02
Clock = 0 Data 100Mhz	4.043e-03	4.044e-03	4.330e-03	4.408e-03
Clock = 1 Data 100Mhz	3.211e-05	3.216e-05	3.231e-05	3.243e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0011	0.0011
D	0.0008	0.0008
RN	0.0011	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0449	0.0578	0.9301	0.5567
CP to Q ↑	0.0528	0.0602	1.4638	0.8208
RN to Q ↓	0.0604	0.0683	0.9010	0.5329

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0508	0.0508
CP ↑	min_pulse_width to CP	0.0349	0.0483
D ↓	hold_rising to CP	0.0078	0.0078
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0317	0.0317
D ↑	setup_rising to CP	0.0175	0.0175
RN ↓	min_pulse_width to RN	0.0903	0.1169
RN ↑	recovery_rising to CP	0.0149	0.0149
RN ↑	removal_rising to CP	-0.0052	-0.0052

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P10	3.072e-05	4.292e-09
X30_P10	3.598e-05	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

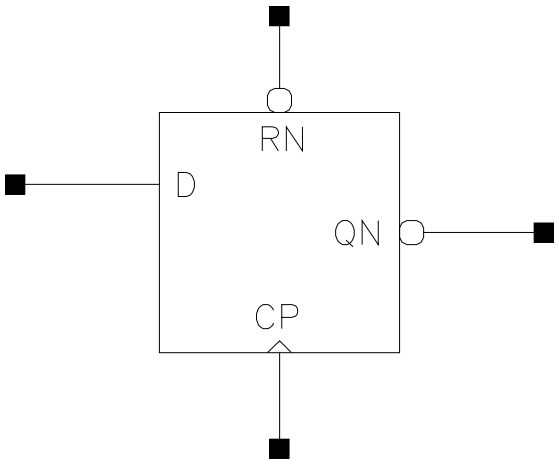
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	5.863e-03	5.871e-03
Clock 100Mhz Data 25Mhz	1.234e-02	1.522e-02
Clock 100Mhz Data 50Mhz	1.882e-02	2.457e-02
Clock = 0 Data 100Mhz	5.605e-03	5.609e-03
Clock = 1 Data 100Mhz	3.264e-05	3.275e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0011	0.0011
D	0.0008	0.0008
RN	0.0011	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.0615	0.0670	0.8721	0.5040
CP to QN ↑	0.0514	0.0559	1.4328	0.7951
RN to QN ↑	0.0690	0.0729	1.4314	0.7946

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0508	0.0508
CP ↑	min_pulse_width to CP	0.0301	0.0301
D ↓	hold_rising to CP	0.0078	0.0078
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0317	0.0317
D ↑	setup_rising to CP	0.0175	0.0175
RN ↓	min_pulse_width to RN	0.0730	0.0779
RN ↑	recovery_rising to CP	0.0149	0.0149
RN ↑	removal_rising to CP	-0.0052	-0.0052

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P10	3.591e-05	4.292e-09
X30_P10	4.318e-05	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

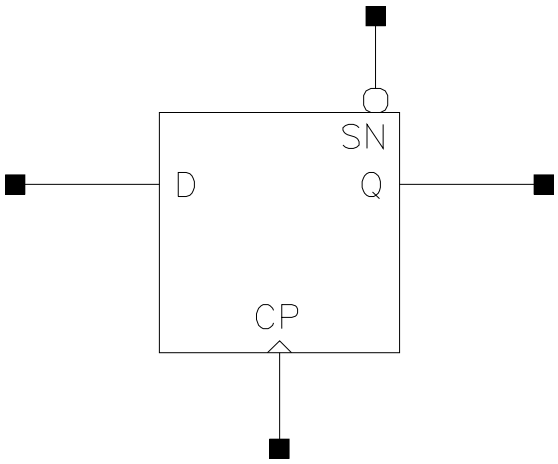
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	5.875e-03	5.874e-03
Clock 100Mhz Data 25Mhz	1.281e-02	1.479e-02
Clock 100Mhz Data 50Mhz	1.974e-02	2.371e-02
Clock = 0 Data 100Mhz	5.671e-03	5.652e-03
Clock = 1 Data 100Mhz	3.265e-05	3.272e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0011	0.0011
D	0.0008	0.0008
SN	0.0014	0.0014

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0452	0.0578	0.9310	0.5533
CP to Q ↑	0.0524	0.0596	1.4631	0.8202
SN to Q ↑	0.0434	0.0478	1.4479	0.8069

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0557	0.0557
CP ↑	min_pulse_width to CP	0.0349	0.0483
D ↓	hold_rising to CP	0.0078	0.0078
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0317	0.0317
D ↑	setup_rising to CP	0.0144	0.0145
SN ↓	min_pulse_width to SN	0.0549	0.0647
SN ↑	recovery_rising to CP	0.0029	0.0029
SN ↑	removal_rising to CP	0.0263	0.0263

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P10	3.338e-05	4.292e-09
X30_P10	4.067e-05	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

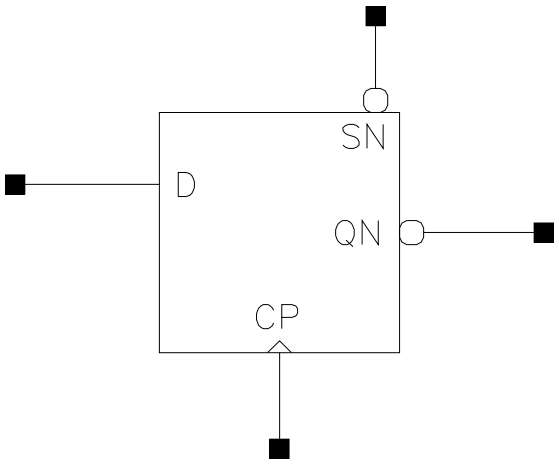
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	5.937e-03	5.925e-03
Clock 100Mhz Data 25Mhz	1.243e-02	1.519e-02
Clock 100Mhz Data 50Mhz	1.893e-02	2.445e-02
Clock = 0 Data 100Mhz	5.547e-03	5.547e-03
Clock = 1 Data 100Mhz	3.265e-05	3.269e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0011	0.0011
D	0.0008	0.0008
SN	0.0014	0.0014

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.0610	0.0666	0.8737	0.5053
CP to QN ↑	0.0516	0.0559	1.4302	0.7935
SN to QN ↓	0.0528	0.0582	0.8734	0.5051

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0557	0.0557
CP ↑	min_pulse_width to CP	0.0301	0.0301
D ↓	hold_rising to CP	0.0078	0.0078
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0317	0.0314
D ↑	setup_rising to CP	0.0144	0.0144
SN ↓	min_pulse_width to SN	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0029	0.0029
SN ↑	removal_rising to CP	0.0263	0.0263

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P10	3.307e-05	4.292e-09
X30_P10	3.820e-05	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

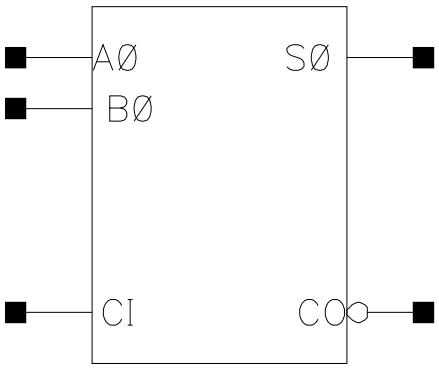
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	5.932e-03	5.927e-03
Clock 100Mhz Data 25Mhz	1.283e-02	1.483e-02
Clock 100Mhz Data 50Mhz	1.973e-02	2.373e-02
Clock = 0 Data 100Mhz	5.548e-03	5.548e-03
Clock = 1 Data 100Mhz	3.264e-05	3.270e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_-P10	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_-P10	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_-P10	1.200	3.672	4.4064
C12T28SOI_LRS1_-FA1X33_P10	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10
A0	0.0037	0.0077	0.0033	0.0064
B0	0.0034	0.0072	0.0035	0.0062
CI	0.0024	0.0055	0.0025	0.0044

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10
A0 to CO ↓	0.0431	0.0475	1.8718	0.4912
A0 to CO ↑	0.0298	0.0315	2.9619	0.7601
A0 to S0 ↓	0.0438	0.0558	1.8387	0.4786
A0 to S0 ↑	0.0451	0.0557	2.9317	0.7490
B0 to CO ↓	0.0427	0.0479	1.8786	0.4940
B0 to CO ↑	0.0310	0.0330	2.9634	0.7575
B0 to S0 ↓	0.0444	0.0569	1.8393	0.4785
B0 to S0 ↑	0.0453	0.0565	2.9342	0.7494
CI to CO ↓	0.0414	0.0470	1.8823	0.4933
CI to CO ↑	0.0309	0.0325	2.9618	0.7602
CI to S0 ↓	0.0439	0.0564	1.8384	0.4784
CI to S0 ↑	0.0454	0.0570	2.9336	0.7490
	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10
A0 to CO ↓	0.0281	0.0346	3.4023	0.5896
A0 to CO ↑	0.0228	0.0264	3.0007	0.7434
A0 to S0 ↓	0.0569	0.0707	1.9817	0.4995
A0 to S0 ↑	0.0527	0.0574	3.0458	0.7625
B0 to CO ↓	0.0291	0.0361	3.4052	0.5905
B0 to CO ↑	0.0209	0.0251	2.9993	0.7434
B0 to S0 ↓	0.0574	0.0728	1.9827	0.4995
B0 to S0 ↑	0.0532	0.0594	3.0469	0.7624
CI to CO ↓	0.0287	0.0502	3.3976	0.6003
CI to CO ↑	0.0230	0.0285	3.0730	0.7488
CI to S0 ↓	0.0326	0.0427	1.9849	0.5004
CI to S0 ↑	0.0282	0.0286	3.0472	0.7624

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_FA1X8_P10	2.545e-05	3.132e-09
C12T28SOI_LR_FA1X33_P10	6.471e-05	6.445e-09
C12T28SOI_LRS1_FA1X8_P10	4.999e-05	4.954e-09
C12T28SOI_LRS1_FA1X33_P10	1.084e-04	1.025e-08

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10
A0 to CO	5.303e-03	1.566e-02	7.913e-03	2.022e-02
A0 to S0	5.353e-03	1.628e-02	1.061e-02	2.508e-02
B0 to CO	5.344e-03	1.590e-02	7.999e-03	2.057e-02
B0 to S0	5.165e-03	1.598e-02	1.082e-02	2.571e-02
CI to CO	5.306e-03	1.592e-02	5.685e-03	1.855e-02
CI to S0	5.120e-03	1.592e-02	6.439e-03	1.980e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10
A0 to CO	-1.272e-06	-2.530e-06	4.221e-06	9.321e-06
A0 to S0	-1.587e-06	-2.887e-06	6.092e-06	1.285e-05
B0 to CO	4.228e-06	7.977e-06	6.704e-07	4.963e-07
B0 to S0	2.037e-05	3.951e-05	5.614e-06	9.470e-06
CI to CO	2.549e-05	4.903e-05	4.810e-08	-6.968e-07
CI to S0	2.800e-05	4.452e-05	-1.997e-07	-7.734e-07

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X33_P10	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X33_P10
A0	0.0013	0.0037
B0	0.0011	0.0031

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
A0 to CO ↓	0.0326	0.0304	1.8370	0.4551
A0 to CO ↑	0.0275	0.0250	2.9332	0.7535
A0 to S0 ↓	0.0406	0.0391	1.7999	0.4545
A0 to S0 ↑	0.0392	0.0440	2.9005	0.7439
B0 to CO ↓	0.0316	0.0280	1.8372	0.4509
B0 to CO ↑	0.0299	0.0266	2.9331	0.7533
B0 to S0 ↓	0.0424	0.0392	1.7997	0.4547
B0 to S0 ↑	0.0384	0.0420	2.9004	0.7435

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	1.400e-05	1.973e-09
X33_P10	4.993e-05	4.126e-09

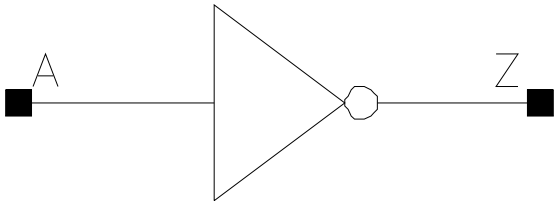
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X33_P10
A0 to CO	4.074e-03	1.355e-02
A0 to S0	3.781e-03	1.329e-02
B0 to CO	4.118e-03	1.363e-02
B0 to S0	3.699e-03	1.275e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X8_P10	X33_P10
A0 to CO	-8.325e-08	-5.325e-07
A0 to S0	-4.752e-08	-6.063e-07
B0 to CO	5.355e-06	4.029e-05
B0 to S0	2.514e-06	2.001e-05

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.272	0.3264
X6_P10	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X13_P10	1.200	0.408	0.4896
X17_P10	1.200	0.408	0.4896
X21_P10	1.200	0.544	0.6528
X25_P10	1.200	0.544	0.6528
X29_P10	1.200	0.680	0.8160
X33_P10	1.200	0.680	0.8160
X50_P10	1.200	0.952	1.1424
X58_P10	1.200	1.088	1.3056
X67_P10	1.200	1.224	1.4688
X75_P10	1.200	1.360	1.6320
X84_P10	1.200	1.496	1.7952
X100_P10	1.200	1.768	2.1216
X134_P10	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0007	0.0008	0.0010	0.0016
	X17_P10	X21_P10	X25_P10	X29_P10
A	0.0020	0.0026	0.0030	0.0035
	X33_P10	X50_P10	X58_P10	X67_P10
A	0.0039	0.0059	0.0070	0.0081
	X75_P10	X84_P10	X100_P10	X134_P10

A	0.0092	0.0103	0.0126	0.0173

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0055	0.0051	3.3642	2.6251
A to Z ↑	0.0123	0.0113	5.5445	4.2370
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0043	0.0035	1.8155	1.1653
A to Z ↑	0.0105	0.0097	2.9729	1.9368
	X17_P10	**X21_P10**	**X17_P10**	**X21_P10**
A to Z ↓	0.0034	0.0039	0.8994	0.7198
A to Z ↑	0.0093	0.0098	1.4625	1.1693
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0038	0.0035	0.6157	0.5214
A to Z ↑	0.0095	0.0092	0.9835	0.8355
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0034	0.0037	0.4626	0.3121
A to Z ↑	0.0089	0.0090	0.7362	0.4931
	X58_P10	**X67_P10**	**X58_P10**	**X67_P10**
A to Z ↓	0.0039	0.0039	0.2708	0.2380
A to Z ↑	0.0092	0.0090	0.4247	0.3722
	X75_P10	**X84_P10**	**X75_P10**	**X84_P10**
A to Z ↓	0.0043	0.0046	0.2150	0.1945
A to Z ↑	0.0094	0.0096	0.3338	0.3018
	X100_P10	**X134_P10**	**X100_P10**	**X134_P10**
A to Z ↓	0.0054	0.0063	0.1657	0.1294
A to Z ↑	0.0104	0.0112	0.2542	0.1953

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	2.685e-06	8.135e-10
X6_P10	3.313e-06	8.135e-10
X8_P10	4.700e-06	8.135e-10
X13_P10	7.235e-06	9.792e-10
X17_P10	9.094e-06	9.792e-10
X21_P10	1.123e-05	1.145e-09
X25_P10	1.277e-05	1.145e-09
X29_P10	1.505e-05	1.310e-09
X33_P10	1.632e-05	1.310e-09
X50_P10	2.339e-05	1.642e-09
X58_P10	2.694e-05	1.807e-09
X67_P10	3.048e-05	1.973e-09
X75_P10	3.403e-05	2.139e-09
X84_P10	3.757e-05	2.304e-09
X100_P10	4.467e-05	2.635e-09
X134_P10	5.885e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10

A to Z	7.078e-04	8.686e-04	1.150e-03	1.630e-03
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	2.090e-03	2.788e-03	3.226e-03	3.626e-03
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	3.981e-03	5.979e-03	7.167e-03	7.923e-03
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	9.093e-03	1.009e-02	1.251e-02	1.745e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

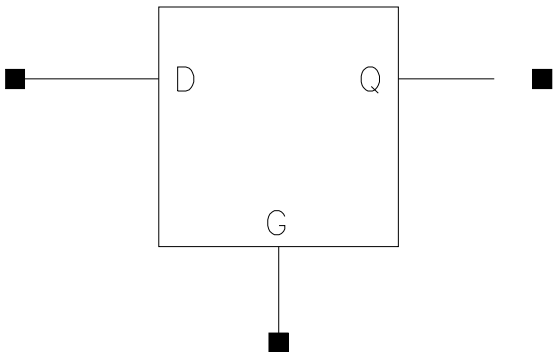
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	8.449e-07	1.069e-06	5.563e-07	6.948e-07
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	7.182e-07	1.270e-06	1.576e-06	2.620e-07
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	3.050e-07	2.910e-07	9.230e-07	4.640e-07
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	2.156e-06	3.503e-06	1.214e-06	3.544e-06

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X23_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P10	X23_P10
D	0.0006	0.0016
G	0.0013	0.0022

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X23_P10	X8_P10	X23_P10
D to Q ↓	0.0485	0.0398	1.8819	0.8586
D to Q ↑	0.0297	0.0302	2.8900	0.7664
G to Q ↓	0.0491	0.0398	1.8785	0.8573
G to Q ↑	0.0290	0.0268	2.8881	0.7670

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P10	X23_P10
D ↓	hold_falling to G	-0.0091	-0.0020
D ↑	hold_falling to G	0.0016	0.0020
D ↓	setup_falling to G	0.0485	0.0367
D ↑	setup_falling to G	0.0330	0.0379
G ↑	min_pulse_width to G	0.0435	0.0409

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	1.334e-05	1.973e-09
X23_P10	2.402e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X23_P10
D (output stable)	2.297e-05	9.525e-05
G (output stable)	1.334e-03	2.637e-03
D to Q	6.654e-03	1.317e-02
G to Q	6.148e-03	1.181e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

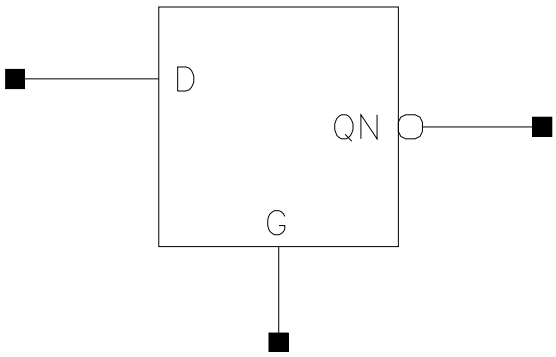
Pin Cycle (vdds)	X8_P10	X23_P10
D (output stable)	-1.596e-07	-1.054e-06
G (output stable)	1.235e-05	3.411e-05
D to Q	-3.298e-07	-7.966e-07
G to Q	4.574e-05	2.731e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P10
D	0.0007
G	0.0015

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P10	X17_P10
D to QN ↓	0.0401	0.8788
D to QN ↑	0.0546	1.4245
G to QN ↓	0.0387	0.8777
G to QN ↑	0.0532	1.4239

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P10
D ↓	hold_falling to G	-0.0140
D ↑	hold_falling to G	-0.0015
D ↓	setup_falling to G	0.0419
D ↑	setup_falling to G	0.0285
G ↑	min_pulse_width to G	0.0338

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P10	1.936e-05	2.139e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X17_P10
D (output stable)	2.361e-05
G (output stable)	1.551e-03
D to QN	8.284e-03
G to QN	7.673e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

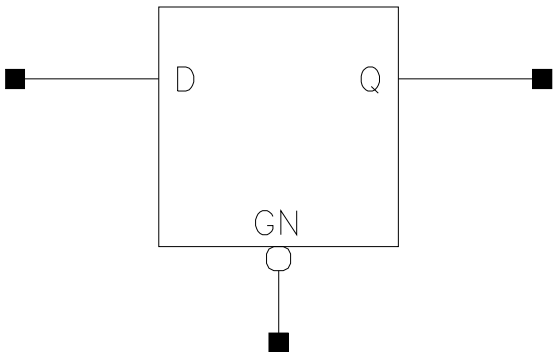
Pin Cycle (vdds)	X17_P10
D (output stable)	-1.288e-07
G (output stable)	1.231e-05
D to QN	-2.862e-07
G to QN	8.733e-05

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
D	0.0006	0.0009	0.0021
GN	0.0012	0.0016	0.0022

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D to Q ↓	0.0490	0.0430	1.8874	0.9261
D to Q ↑	0.0303	0.0286	2.8931	1.4816
GN to Q ↓	0.0442	0.0383	1.8906	0.9274
GN to Q ↑	0.0463	0.0445	2.8878	1.4795

	X33_P10		X33_P10	
D to Q ↓	0.0418		0.4723	
D to Q ↑	0.0245		0.7431	
GN to Q ↓	0.0360		0.4725	
GN to Q ↑	0.0352		0.7423	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P10	X17_P10	X33_P10
D ↓	hold_rising to GN	-0.0118	-0.0100	-0.0048
D ↑	hold_rising to GN	0.0058	0.0058	0.0106
D ↓	setup_rising to GN	0.0544	0.0496	0.0468
D ↑	setup_rising to GN	0.0295	0.0239	0.0221
GN ↓	min_pulse_width to GN	0.0625	0.0531	0.0511

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	1.241e-05	1.973e-09
X17_P10	1.858e-05	2.304e-09
X33_P10	3.006e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
D (output stable)	2.326e-05	3.823e-05	1.030e-04
GN (output stable)	1.329e-03	1.796e-03	2.291e-03
D to Q	6.684e-03	9.588e-03	1.562e-02
GN to Q	9.256e-03	1.277e-02	1.910e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

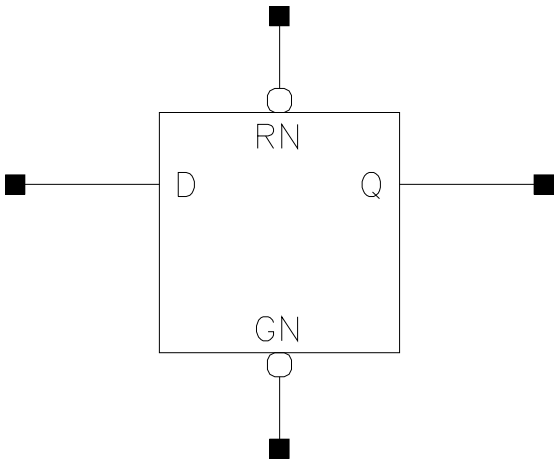
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
D (output stable)	-1.408e-07	-1.241e-07	-9.266e-07
GN (output stable)	1.218e-05	1.703e-05	3.424e-05
D to Q	-3.528e-07	-3.713e-07	-4.291e-07
GN to Q	-5.157e-05	-2.830e-05	-3.808e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.496	1.7952
X33_P10	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X33_P10
D	0.0007	0.0017
GN	0.0014	0.0026
RN	0.0007	0.0007

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
D to Q ↓	0.0458	0.0420	1.8402	0.4747
D to Q ↑	0.0391	0.0507	2.9417	0.7626

GN to Q ↓	0.0417	0.0386	1.8429	0.4750
GN to Q ↑	0.0526	0.0551	2.9430	0.7624
RN to Q ↓	0.0364	0.0629	1.7446	0.4856
RN to Q ↑	0.0410	0.0559	2.9422	0.7622

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P10	X33_P10
D ↓	hold_rising to GN	-0.0096	-0.0048
D ↑	hold_rising to GN	-0.0046	-0.0137
D ↓	setup_rising to GN	0.0496	0.0448
D ↑	setup_rising to GN	0.0392	0.0534
GN ↓	min_pulse_width to GN	0.0567	0.0559
RN ↓	min_pulse_width to RN	0.0469	0.0806
RN ↑	recovery_rising to GN	0.0388	0.0609
RN ↑	removal_rising to GN	-0.0242	-0.0412

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	1.150e-05	2.304e-09
X33_P10	2.470e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X33_P10
D (output stable)	1.140e-04	2.156e-04
GN (output stable)	1.560e-03	2.411e-03
RN (output stable)	5.541e-05	9.960e-05
D to Q	6.697e-03	1.800e-02
GN to Q	9.472e-03	2.214e-02
RN to Q	5.189e-03	1.471e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

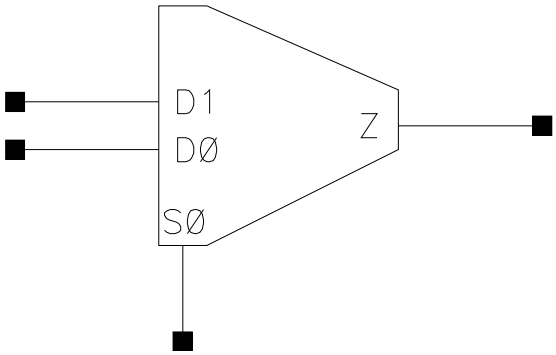
Pin Cycle (vdds)	X8_P10	X33_P10
D (output stable)	-7.466e-07	-1.110e-06
GN (output stable)	6.520e-06	1.245e-05
RN (output stable)	1.349e-07	1.897e-07
D to Q	-3.359e-07	-8.470e-07
GN to Q	-4.967e-05	4.914e-05
RN to Q	5.816e-06	-2.894e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
D0	0.0009	0.0013	0.0017	0.0023
D1	0.0008	0.0012	0.0017	0.0023
S0	0.0015	0.0016	0.0019	0.0028

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D0 to Z ↓	0.0361	0.0328	1.8430	0.8998
D0 to Z ↑	0.0281	0.0258	2.9621	1.4501
D1 to Z ↓	0.0346	0.0324	1.8378	0.8994
D1 to Z ↑	0.0258	0.0244	2.9586	1.4481
S0 to Z ↓	0.0310	0.0305	1.8292	0.8961
S0 to Z ↑	0.0297	0.0301	2.9586	1.4483

	X25_P10	X33_P10	X25_P10	X33_P10
D0 to Z ↓	0.0349	0.0316	0.6201	0.4645
D0 to Z ↑	0.0280	0.0257	0.9752	0.7303
D1 to Z ↓	0.0372	0.0327	0.6236	0.4658
D1 to Z ↑	0.0269	0.0247	0.9742	0.7300
S0 to Z ↓	0.0345	0.0315	0.6198	0.4637
S0 to Z ↑	0.0336	0.0308	0.9744	0.7302

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	1.474e-05	1.973e-09
X17_P10	2.393e-05	2.139e-09
X25_P10	3.376e-05	3.298e-09
X33_P10	4.518e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	1.194e-03	1.818e-03	2.061e-03	2.860e-03
D1 (output stable)	1.010e-03	1.715e-03	2.248e-03	2.966e-03
S0 (output stable)	1.569e-03	1.792e-03	2.336e-03	2.904e-03
D0 to Z	4.436e-03	7.397e-03	1.155e-02	1.450e-02
D1 to Z	4.117e-03	7.205e-03	1.167e-02	1.436e-02
S0 to Z	5.039e-03	7.836e-03	1.279e-02	1.564e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

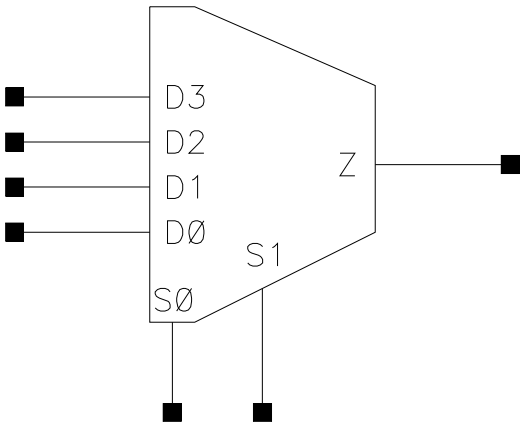
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	6.179e-07	2.732e-06	1.019e-06	3.366e-07
D1 (output stable)	1.320e-06	2.621e-06	7.460e-07	1.543e-06
S0 (output stable)	8.225e-08	1.495e-07	2.118e-07	5.055e-08
D0 to Z	3.310e-08	-1.400e-08	-2.423e-07	-2.735e-07
D1 to Z	9.945e-08	-2.230e-07	-2.095e-07	2.600e-07
S0 to Z	2.468e-07	1.703e-07	4.380e-08	5.845e-08

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.312	2.7744
X31_P10	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P10	X31_P10
D0	0.0006	0.0018
D1	0.0007	0.0017
D2	0.0006	0.0018
D3	0.0007	0.0018
S0	0.0022	0.0045
S1	0.0013	0.0027

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X31_P10	X8_P10	X31_P10

D0 to Z ↓	0.0645	0.0669	1.9449	0.5366
D0 to Z ↑	0.0398	0.0425	2.9796	0.7987
D1 to Z ↓	0.0640	0.0670	1.9435	0.5366
D1 to Z ↑	0.0400	0.0423	2.9783	0.7989
D2 to Z ↓	0.0690	0.0631	1.9565	0.5308
D2 to Z ↑	0.0420	0.0390	2.9857	0.7941
D3 to Z ↓	0.0687	0.0625	1.9563	0.5297
D3 to Z ↑	0.0415	0.0406	2.9831	0.7969
S0 to Z ↓	0.0701	0.0722	1.9477	0.5331
S0 to Z ↑	0.0505	0.0541	2.9830	0.7980
S1 to Z ↓	0.0495	0.0494	1.9491	0.5329
S1 to Z ↑	0.0394	0.0419	2.9816	0.7975

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	1.594e-05	3.298e-09
X31_P10	4.376e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X31_P10
D0 (output stable)	2.105e-05	1.138e-04
D1 (output stable)	2.805e-05	1.579e-04
D2 (output stable)	2.579e-05	9.258e-05
D3 (output stable)	3.760e-05	1.525e-04
S0 (output stable)	2.389e-03	5.532e-03
S1 (output stable)	1.765e-03	3.719e-03
D0 to Z	5.021e-03	1.751e-02
D1 to Z	5.009e-03	1.754e-02
D2 to Z	5.349e-03	1.642e-02
D3 to Z	5.332e-03	1.644e-02
S0 to Z	7.683e-03	2.322e-02
S1 to Z	5.698e-03	1.675e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

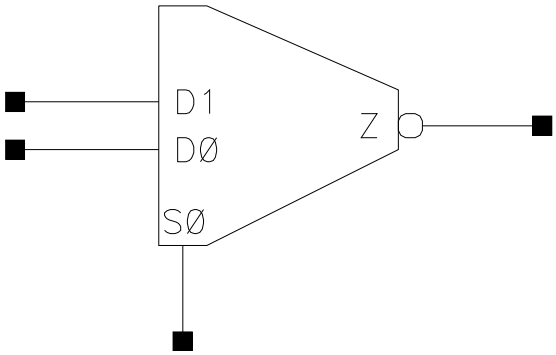
Pin Cycle (vdds)	X8_P10	X31_P10
D0 (output stable)	4.402e-06	1.508e-05
D1 (output stable)	4.212e-06	1.413e-05
D2 (output stable)	4.352e-06	2.041e-05
D3 (output stable)	2.977e-06	1.796e-05
S0 (output stable)	-6.612e-06	-1.623e-05
S1 (output stable)	6.265e-05	2.306e-04
D0 to Z	1.510e-06	2.398e-06
D1 to Z	7.920e-07	7.128e-06
D2 to Z	2.511e-06	2.772e-06
D3 to Z	2.888e-06	5.820e-06
S0 to Z	-1.226e-06	-6.769e-06
S1 to Z	6.079e-05	2.311e-04

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.816	0.9792
X5_P10	1.200	0.952	1.1424
X10_P10	1.200	1.768	2.1216
X16_P10	1.200	2.448	2.9376
X21_P10	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P10	X5_P10	X10_P10	X16_P10
D0	0.0006	0.0010	0.0020	0.0030
D1	0.0006	0.0010	0.0019	0.0030
S0	0.0013	0.0022	0.0029	0.0044
	X21_P10			
D0	0.0040			
D1	0.0040			
S0	0.0050			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X5_P10	X3_P10	X5_P10
D0 to Z ↓	0.0111	0.0110	5.4212	3.4253

D0 to Z ↑	0.0222	0.0200	11.6012	6.0497
D1 to Z ↓	0.0109	0.0106	5.3766	3.2448
D1 to Z ↑	0.0229	0.0210	11.6107	6.2823
S0 to Z ↓	0.0185	0.0156	5.3935	3.3367
S0 to Z ↑	0.0207	0.0174	11.5803	6.1563
	X10_P10	**X16_P10**	**X10_P10**	**X16_P10**
D0 to Z ↓	0.0124	0.0114	1.6152	1.0553
D0 to Z ↑	0.0217	0.0207	2.8299	1.8673
D1 to Z ↓	0.0112	0.0110	1.5586	1.0278
D1 to Z ↑	0.0220	0.0214	2.8759	1.8858
S0 to Z ↓	0.0192	0.0166	1.5854	1.0410
S0 to Z ↑	0.0208	0.0179	2.8494	1.8758
	X21_P10		**X21_P10**	
D0 to Z ↓	0.0113		0.8062	
D0 to Z ↑	0.0202		1.4149	
D1 to Z ↓	0.0110		0.7797	
D1 to Z ↑	0.0215		1.4078	
S0 to Z ↓	0.0175		0.7928	
S0 to Z ↑	0.0185		1.4092	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P10	6.126e-06	1.476e-09
X5_P10	1.131e-05	1.642e-09
X10_P10	1.965e-05	2.635e-09
X16_P10	3.006e-05	3.464e-09
X21_P10	3.695e-05	4.292e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	2.364e-05	5.064e-05	1.487e-04	2.330e-04
D1 (output stable)	2.280e-05	5.577e-05	1.254e-04	2.152e-04
S0 (output stable)	1.328e-03	1.987e-03	3.358e-03	5.370e-03
D0 to Z	1.310e-03	2.175e-03	5.328e-03	7.542e-03
D1 to Z	1.307e-03	2.169e-03	5.092e-03	7.466e-03
S0 to Z	2.292e-03	3.389e-03	6.873e-03	9.919e-03
	X21_P10			
D0 (output stable)	3.021e-04			
D1 (output stable)	2.885e-04			
S0 (output stable)	5.937e-03			
D0 to Z	9.722e-03			
D1 to Z	9.887e-03			
S0 to Z	1.210e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	-1.471e-07	-1.187e-07	-1.083e-06	-3.039e-06
D1 (output stable)	-1.740e-07	-1.193e-06	-9.796e-07	-2.199e-06
S0 (output stable)	1.287e-05	4.878e-05	5.681e-05	1.112e-04
D0 to Z	4.092e-07	1.805e-06	1.712e-06	3.697e-06

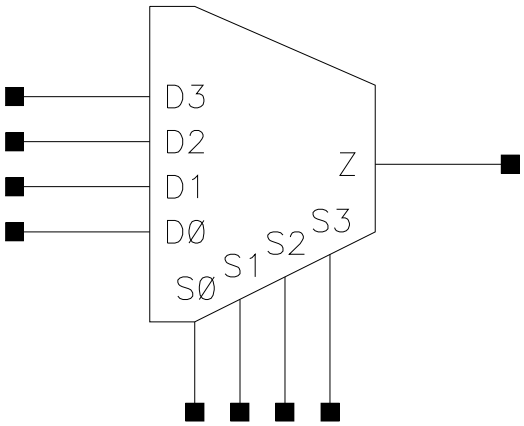
D1 to Z	3.553e-07	6.695e-07	2.857e-06	3.015e-06
S0 to Z	1.133e-05	4.207e-05	4.594e-05	9.294e-05
	X21_P10			
D0 (output stable)	-3.451e-06			
D1 (output stable)	-4.166e-06			
S0 (output stable)	1.553e-04			
D0 to Z	9.248e-06			
D1 to Z	7.863e-06			
S0 to Z	1.283e-04			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	1.768	2.1216
X27_P10	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P10	X27_P10
D0	0.0008	0.0023
D1	0.0008	0.0024
D2	0.0008	0.0023
D3	0.0008	0.0024
S0	0.0008	0.0022
S1	0.0008	0.0023
S2	0.0008	0.0022
S3	0.0008	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	X27_P10	X7_P10	X27_P10
D0 to Z ↓	0.0483	0.0413	2.8512	0.7797
D0 to Z ↑	0.0333	0.0285	2.9107	0.7270
D1 to Z ↓	0.0444	0.0383	2.8477	0.7791
D1 to Z ↑	0.0296	0.0248	2.9005	0.7245
D2 to Z ↓	0.0492	0.0402	2.8647	0.7814
D2 to Z ↑	0.0324	0.0266	2.9208	0.7296
D3 to Z ↓	0.0454	0.0373	2.8578	0.7801
D3 to Z ↑	0.0288	0.0230	2.9111	0.7270
S0 to Z ↓	0.0465	0.0388	2.8490	0.7791
S0 to Z ↑	0.0359	0.0305	2.9093	0.7269
S1 to Z ↓	0.0428	0.0357	2.8447	0.7786
S1 to Z ↑	0.0319	0.0262	2.9003	0.7244
S2 to Z ↓	0.0473	0.0376	2.8613	0.7803
S2 to Z ↑	0.0350	0.0285	2.9203	0.7294
S3 to Z ↓	0.0438	0.0348	2.8551	0.7790
S3 to Z ↑	0.0311	0.0245	2.9130	0.7269

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X7_P10	1.384e-05	2.635e-09
X27_P10	4.751e-05	4.954e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X7_P10	X27_P10
D0 (output stable)	7.119e-04	2.274e-03
D1 (output stable)	5.769e-04	1.808e-03
D2 (output stable)	6.516e-04	2.093e-03
D3 (output stable)	5.166e-04	1.634e-03
S0 (output stable)	6.900e-04	2.161e-03
S1 (output stable)	5.495e-04	1.710e-03
S2 (output stable)	6.240e-04	1.981e-03
S3 (output stable)	4.877e-04	1.540e-03
D0 to Z	5.508e-03	1.729e-02
D1 to Z	4.831e-03	1.499e-02
D2 to Z	5.308e-03	1.535e-02
D3 to Z	4.642e-03	1.311e-02
S0 to Z	5.342e-03	1.641e-02
S1 to Z	4.667e-03	1.416e-02
S2 to Z	5.140e-03	1.443e-02
S3 to Z	4.478e-03	1.228e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

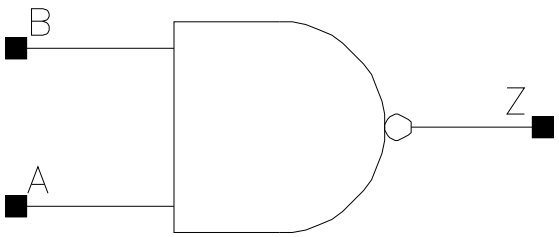
Pin Cycle (vdds)	X7_P10	X27_P10
D0 (output stable)	-7.303e-07	-7.529e-07
D1 (output stable)	1.163e-05	3.466e-05
D2 (output stable)	-8.533e-07	-7.204e-07
D3 (output stable)	1.257e-05	3.444e-05
S0 (output stable)	-1.439e-06	-5.963e-07
S1 (output stable)	1.289e-05	3.474e-05
S2 (output stable)	-6.440e-07	-4.470e-07
S3 (output stable)	1.229e-05	3.443e-05
D0 to Z	-1.384e-07	4.916e-07
D1 to Z	-3.526e-08	5.359e-08
D2 to Z	1.137e-07	5.715e-07
D3 to Z	-2.913e-08	2.052e-07
S0 to Z	-1.069e-07	8.354e-07
S1 to Z	-4.841e-08	-1.678e-08
S2 to Z	9.932e-08	1.587e-06
S3 to Z	-5.965e-08	1.006e-07

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P10	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P10	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P10	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P10	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P10	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P10	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P10	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P10	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P10	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P10	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P10	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P10	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P10	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P10	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P10	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P10	C12T28SOI_LR_-NAND2X5_P10	C12T28SOI_LR_-NAND2X7_P10	C12T28SOI_LR_-NAND2X10_P10
A	0.0006	0.0008	0.0010	0.0016
B	0.0007	0.0009	0.0010	0.0015
	C12T28SOI_LR_-NAND2X13_P10	C12T28SOI_LR_-NAND2X17_P10	C12T28SOI_LR_-NAND2X20_P10	C12T28SOI_LR_-NAND2X24_P10
A	0.0020	0.0026	0.0030	0.0036
B	0.0019	0.0025	0.0028	0.0034
	C12T28SOI_LR_-NAND2X27_P10	C12T28SOI_LR_-NAND2X42_P10	C12T28SOI_LR_-NAND2X47_P10	C12T28SOI_LR_-NAND2X50_P10
A	0.0040	0.0012	0.0012	0.0012
B	0.0038	0.0012	0.0012	0.0012
	C12T28SOI_LR_-NAND2X58_P10	C12T28SOI_LR_-NAND2X67_P10	C12T28SOI_-LRBR0D8_-NAND2X7_P10	C12T28SOI_-LRBR0D8_-NAND2X14_P10
A	0.0012	0.0012	0.0010	0.0020
B	0.0012	0.0012	0.0010	0.0019
	C12T28SOI_LRS_-NAND2X40_P10	C12T28SOI_LRS_-NAND2X54_P10		
A	0.0060	0.0080		
B	0.0056	0.0076		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P10	**C12T28SOI_LR_-NAND2X5_P10**	**C12T28SOI_LR_-NAND2X3_P10**	**C12T28SOI_LR_-NAND2X5_P10**
A to Z ↓	0.0079	0.0069	5.3010	3.4650
A to Z ↑	0.0148	0.0135	5.5591	3.6291
B to Z ↓	0.0088	0.0075	5.3848	3.5175
B to Z ↑	0.0130	0.0116	5.6022	3.6555
	C12T28SOI_LR_-NAND2X7_P10	**C12T28SOI_LR_-NAND2X10_P10**	**C12T28SOI_LR_-NAND2X7_P10**	**C12T28SOI_LR_-NAND2X10_P10**
A to Z ↓	0.0068	0.0080	2.9183	1.9296
A to Z ↑	0.0132	0.0141	2.9571	1.9197
B to Z ↓	0.0074	0.0076	2.9589	1.9574
B to Z ↑	0.0111	0.0112	2.9860	1.9347
	C12T28SOI_LR_-NAND2X13_P10	**C12T28SOI_LR_-NAND2X17_P10**	**C12T28SOI_LR_-NAND2X13_P10**	**C12T28SOI_LR_-NAND2X17_P10**
A to Z ↓	0.0075	0.0075	1.4942	1.1809

A to Z ↑	0.0134	0.0136	1.4546	1.1644
B to Z ↓	0.0071	0.0076	1.5156	1.1970
B to Z ↑	0.0104	0.0110	1.4664	1.1732
	C12T28SOI_LR_-NAND2X20_P10	**C12T28SOI_LR_-NAND2X24_P10**	**C12T28SOI_LR_-NAND2X20_P10**	**C12T28SOI_LR_-NAND2X24_P10**
A to Z ↓	0.0074	0.0077	1.0211	0.8677
A to Z ↑	0.0132	0.0134	0.9789	0.8323
B to Z ↓	0.0076	0.0073	1.0355	0.8797
B to Z ↑	0.0107	0.0106	0.9877	0.8384
	C12T28SOI_LR_-NAND2X27_P10	**C12T28SOI_LR_-NAND2X42_P10**	**C12T28SOI_LR_-NAND2X27_P10**	**C12T28SOI_LR_-NAND2X42_P10**
A to Z ↓	0.0074	0.0334	0.7752	0.3661
A to Z ↑	0.0131	0.0369	0.7345	0.5778
B to Z ↓	0.0072	0.0349	0.7860	0.3661
B to Z ↑	0.0103	0.0353	0.7400	0.5774
	C12T28SOI_LR_-NAND2X47_P10	**C12T28SOI_LR_-NAND2X50_P10**	**C12T28SOI_LR_-NAND2X47_P10**	**C12T28SOI_LR_-NAND2X50_P10**
A to Z ↓	0.0347	0.0350	0.3253	0.3056
A to Z ↑	0.0377	0.0380	0.5022	0.4823
B to Z ↓	0.0361	0.0365	0.3251	0.3054
B to Z ↑	0.0360	0.0364	0.5023	0.4825
	C12T28SOI_LR_-NAND2X58_P10	**C12T28SOI_LR_-NAND2X67_P10**	**C12T28SOI_LR_-NAND2X58_P10**	**C12T28SOI_LR_-NAND2X67_P10**
A to Z ↓	0.0369	0.0383	0.2653	0.2335
A to Z ↑	0.0394	0.0403	0.4151	0.3650
B to Z ↓	0.0384	0.0397	0.2653	0.2333
B to Z ↑	0.0378	0.0387	0.4152	0.3653
	C12T28SOI_-LRBR0D8_-NAND2X7_P10	**C12T28SOI_-LRBR0D8_-NAND2X14_P10**	**C12T28SOI_-LRBR0D8_-NAND2X7_P10**	**C12T28SOI_-LRBR0D8_-NAND2X14_P10**
A to Z ↓	0.0049	0.0059	2.2155	1.1668
A to Z ↑	0.0162	0.0165	3.8781	1.8976
B to Z ↓	0.0050	0.0046	2.2601	1.1928
B to Z ↑	0.0132	0.0121	4.0026	1.9339
	C12T28SOI_LRS_-NAND2X40_P10	**C12T28SOI_LRS_-NAND2X54_P10**	**C12T28SOI_LRS_-NAND2X40_P10**	**C12T28SOI_LRS_-NAND2X54_P10**
A to Z ↓	0.0074	0.0074	0.5251	0.3977
A to Z ↑	0.0130	0.0130	0.4920	0.3709
B to Z ↓	0.0073	0.0074	0.5327	0.4033
B to Z ↑	0.0102	0.0103	0.4960	0.3742

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P10	2.912e-06	9.792e-10
C12T28SOI_LR_NAND2X5_P10	4.404e-06	9.792e-10
C12T28SOI_LR_NAND2X7_P10	5.165e-06	9.792e-10
C12T28SOI_LR_NAND2X10_P10	7.545e-06	1.310e-09
C12T28SOI_LR_NAND2X13_P10	9.577e-06	1.310e-09
C12T28SOI_LR_NAND2X17_P10	1.199e-05	1.642e-09
C12T28SOI_LR_NAND2X20_P10	1.372e-05	1.642e-09
C12T28SOI_LR_NAND2X24_P10	1.640e-05	1.973e-09
C12T28SOI_LR_NAND2X27_P10	1.787e-05	1.973e-09

C12T28SOI_LR_NAND2X42_P10	3.384e-05	2.139e-09
C12T28SOI_LR_NAND2X47_P10	3.775e-05	2.304e-09
C12T28SOI_LR_NAND2X50_P10	3.820e-05	2.304e-09
C12T28SOI_LR_NAND2X58_P10	4.255e-05	2.470e-09
C12T28SOI_LR_NAND2X67_P10	4.691e-05	2.635e-09
C12T28SOI_LRBR0D8_NAND2X7_-P10	6.124e-06	1.804e-09
C12T28SOI_LRBR0D8_NAND2X14_-P10	1.126e-05	2.156e-09
C12T28SOI_LRS_NAND2X40_P10	2.618e-05	2.635e-09
C12T28SOI_LRS_NAND2X54_P10	3.450e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P10	C12T28SOI_LR_-NAND2X5_P10	C12T28SOI_LR_-NAND2X7_P10	C12T28SOI_LR_-NAND2X10_P10
A (output stable)	1.580e-05	2.481e-05	2.959e-05	9.347e-05
B (output stable)	2.499e-05	3.852e-05	4.727e-05	3.344e-04
A to Z	9.501e-04	1.297e-03	1.550e-03	2.646e-03
B to Z	7.887e-04	1.056e-03	1.251e-03	1.928e-03
	C12T28SOI_LR_-NAND2X13_P10	C12T28SOI_LR_-NAND2X17_P10	C12T28SOI_LR_-NAND2X20_P10	C12T28SOI_LR_-NAND2X24_P10
A (output stable)	1.119e-04	1.367e-04	1.494e-04	2.048e-04
B (output stable)	3.756e-04	3.620e-04	3.992e-04	6.371e-04
A to Z	3.245e-03	4.140e-03	4.728e-03	5.742e-03
B to Z	2.363e-03	3.129e-03	3.599e-03	4.221e-03
	C12T28SOI_LR_-NAND2X27_P10	C12T28SOI_LR_-NAND2X42_P10	C12T28SOI_LR_-NAND2X47_P10	C12T28SOI_LR_-NAND2X50_P10
A (output stable)	2.192e-04	3.341e-05	3.361e-05	3.355e-05
B (output stable)	6.734e-04	5.070e-05	5.059e-05	5.075e-05
A to Z	6.266e-03	1.563e-02	1.707e-02	1.762e-02
B to Z	4.600e-03	1.532e-02	1.676e-02	1.731e-02
	C12T28SOI_LR_-NAND2X58_P10	C12T28SOI_LR_-NAND2X67_P10	C12T28SOI_-LRBR0D8_-NAND2X7_P10	C12T28SOI_-LRBR0D8_-NAND2X14_P10
A (output stable)	3.370e-05	3.380e-05	3.821e-05	1.398e-04
B (output stable)	5.087e-05	5.095e-05	6.120e-05	4.781e-04
A to Z	2.019e-02	2.242e-02	1.603e-03	3.394e-03
B to Z	1.988e-02	2.212e-02	1.185e-03	2.202e-03
	C12T28SOI_LRS_-NAND2X40_P10	C12T28SOI_LRS_-NAND2X54_P10		
A (output stable)	3.170e-04	4.124e-04		
B (output stable)	9.261e-04	1.182e-03		
A to Z	9.278e-03	1.222e-02		
B to Z	6.853e-03	9.081e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P10	C12T28SOI_LR_-NAND2X5_P10	C12T28SOI_LR_-NAND2X7_P10	C12T28SOI_LR_-NAND2X10_P10
A (output stable)	3.780e-08	2.980e-08	1.880e-08	-3.910e-08
B (output stable)	7.270e-08	5.250e-08	4.570e-08	-1.137e-06
A to Z	3.159e-07	3.473e-07	7.559e-07	1.429e-06

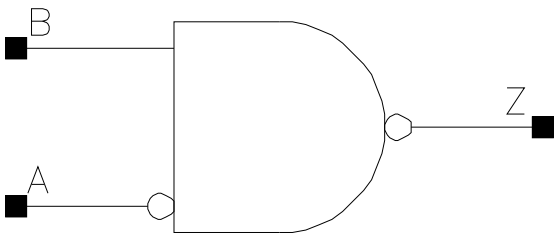
B to Z	2.512e-07	5.908e-07	1.173e-06	1.855e-06
	C12T28SOI_LR_-NAND2X13_P10	C12T28SOI_LR_-NAND2X17_P10	C12T28SOI_LR_-NAND2X20_P10	C12T28SOI_LR_-NAND2X24_P10
A (output stable)	-6.800e-08	-9.020e-08	-1.269e-07	-1.899e-07
B (output stable)	-1.045e-06	-7.634e-07	-9.840e-08	-2.078e-06
A to Z	1.435e-06	1.804e-06	2.936e-06	3.436e-06
B to Z	2.819e-06	3.188e-06	3.950e-06	4.631e-06
	C12T28SOI_LR_-NAND2X27_P10	C12T28SOI_LR_-NAND2X42_P10	C12T28SOI_LR_-NAND2X47_P10	C12T28SOI_LR_-NAND2X50_P10
A (output stable)	-2.356e-07	3.145e-08	3.271e-08	3.383e-08
B (output stable)	-1.899e-06	5.240e-08	5.410e-08	5.180e-08
A to Z	3.816e-06	-3.650e-07	-3.790e-07	-4.340e-07
B to Z	5.049e-06	-4.720e-07	-3.130e-07	-2.910e-07
	C12T28SOI_LR_-NAND2X58_P10	C12T28SOI_LR_-NAND2X67_P10	C12T28SOI_-LRBR0D8_-NAND2X7_P10	C12T28SOI_-LRBR0D8_-NAND2X14_P10
A (output stable)	3.362e-08	3.398e-08	4.283e-08	-3.910e-08
B (output stable)	5.120e-08	5.460e-08	6.180e-08	-4.056e-06
A to Z	-3.950e-07	-4.150e-07	4.316e-07	1.341e-06
B to Z	-5.460e-07	-4.360e-07	6.871e-07	4.260e-07
	C12T28SOI_LRS_-NAND2X40_P10	C12T28SOI_LRS_-NAND2X54_P10		
A (output stable)	-3.936e-07	-5.063e-07		
B (output stable)	-2.396e-06	-3.264e-06		
A to Z	5.895e-06	7.638e-06		
B to Z	7.312e-06	9.738e-06		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X7_P10	1.200	0.544	0.6528
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X40_P10	1.200	2.312	2.7744
X54_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P10	X7_P10	X13_P10	X27_P10
A	0.0009	0.0009	0.0012	0.0023
B	0.0007	0.0010	0.0018	0.0038
	X40_P10	X54_P10		
A	0.0035	0.0045		
B	0.0056	0.0076		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0254	0.0271	5.2417	2.8942
A to Z ↑	0.0191	0.0201	5.3973	2.9149
B to Z ↓	0.0091	0.0075	5.4267	2.9782
B to Z ↑	0.0131	0.0111	5.6030	3.0108
	X13_P10	**X27_P10**	**X13_P10**	**X27_P10**

A to Z ↓	0.0256	0.0249	1.5624	0.7744
A to Z ↑	0.0193	0.0188	1.4951	0.7254
B to Z ↓	0.0070	0.0070	1.6083	0.7981
B to Z ↑	0.0104	0.0101	1.4997	0.7411
	X40_P10	**X54_P10**	**X40_P10**	**X54_P10**
A to Z ↓	0.0255	0.0253	0.5165	0.3918
A to Z ↑	0.0194	0.0192	0.4829	0.3646
B to Z ↓	0.0071	0.0072	0.5323	0.4036
B to Z ↑	0.0101	0.0102	0.4978	0.3757

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P10	5.159e-06	1.145e-09
X7_P10	7.404e-06	1.145e-09
X13_P10	1.442e-05	1.642e-09
X27_P10	2.660e-05	2.470e-09
X40_P10	3.848e-05	3.298e-09
X54_P10	5.035e-05	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	1.474e-03	1.869e-03	3.125e-03	6.115e-03
B (output stable)	2.573e-05	4.728e-05	3.365e-04	5.944e-04
A to Z	2.441e-03	3.391e-03	6.221e-03	1.226e-02
B to Z	7.973e-04	1.240e-03	2.314e-03	4.598e-03
	X40_P10	X54_P10		
A (output stable)	9.409e-03	1.229e-02		
B (output stable)	8.628e-04	1.126e-03		
A to Z	1.859e-02	2.447e-02		
B to Z	6.829e-03	9.060e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

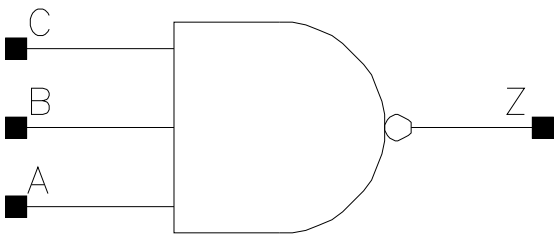
Pin Cycle (vdds)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	7.200e-08	1.231e-07	3.250e-08	-1.326e-07
B (output stable)	7.390e-08	4.820e-08	-1.450e-08	-1.135e-06
A to Z	3.444e-07	1.286e-07	8.695e-07	-1.630e-07
B to Z	1.120e-08	4.767e-07	-2.420e-07	-3.380e-07
	X40_P10	X54_P10		
A (output stable)	-2.140e-07	-4.800e-07		
B (output stable)	-1.841e-06	-2.803e-06		
A to Z	2.126e-06	3.649e-06		
B to Z	6.758e-06	8.649e-06		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P10	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P10	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P10	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P10	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P10	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P10	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P10	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P10	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P10	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P10	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P10	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P10	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P10	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P10	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P10	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A	0.0008	0.0010	0.0016	0.0020
B	0.0008	0.0010	0.0015	0.0019
C	0.0008	0.0010	0.0015	0.0019
	C12T28SOI_LR_-NAND3X15_P10	C12T28SOI_LR_-NAND3X18_P10	C12T28SOI_LR_-NAND3X21_P10	C12T28SOI_LR_-NAND3X24_P10
A	0.0026	0.0029	0.0036	0.0040
B	0.0025	0.0028	0.0034	0.0038
C	0.0024	0.0027	0.0033	0.0037
	C12T28SOI_LR_-NAND3X35_P10	C12T28SOI_LR_-NAND3X47_P10	C12T28SOI_-LRBR0P6_-NAND3X6_P10	C12T28SOI_-LRBR0P6_-NAND3X12_P10
A	0.0060	0.0080	0.0010	0.0020
B	0.0057	0.0077	0.0011	0.0019
C	0.0055	0.0075	0.0010	0.0019
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	C12T28SOI_-LRBR0P6_-NAND3X24_P10	C12T28SOI_-LRBR0P6_-NAND3X35_P10	C12T28SOI_-LRBR0P6_-NAND3X47_P10
A	0.0029	0.0039	0.0059	0.0079
B	0.0028	0.0038	0.0057	0.0077
C	0.0026	0.0036	0.0054	0.0073
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10			
A	0.0030			
B	0.0029			
C	0.0027			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10
A to Z ↓	0.0130	0.0117	5.5420	3.9910
A to Z ↑	0.0186	0.0170	4.1117	2.8789
B to Z ↓	0.0140	0.0124	5.5653	4.0082
B to Z ↑	0.0176	0.0158	4.1244	2.8876
C to Z ↓	0.0129	0.0115	5.5977	4.0322
C to Z ↑	0.0149	0.0134	4.1302	2.9057

	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A to Z ↓	0.0132	0.0122	2.6990	2.1138
A to Z ↑	0.0179	0.0168	1.9318	1.4703
B to Z ↓	0.0127	0.0119	2.7101	2.1229
B to Z ↑	0.0160	0.0151	1.9368	1.4741
C to Z ↓	0.0116	0.0110	2.7266	2.1357
C to Z ↑	0.0133	0.0124	1.9320	1.4654
	C12T28SOI_LR_-NAND3X15_P10	**C12T28SOI_LR_-NAND3X18_P10**	**C12T28SOI_LR_-NAND3X15_P10**	**C12T28SOI_LR_-NAND3X18_P10**
A to Z ↓	0.0118	0.0113	1.6899	1.4585
A to Z ↑	0.0165	0.0159	1.1650	0.9780
B to Z ↓	0.0119	0.0115	1.6978	1.4649
B to Z ↑	0.0148	0.0142	1.1690	0.9810
C to Z ↓	0.0112	0.0107	1.7085	1.4737
C to Z ↑	0.0124	0.0117	1.1778	0.9880
	C12T28SOI_LR_-NAND3X21_P10	**C12T28SOI_LR_-NAND3X24_P10**	**C12T28SOI_LR_-NAND3X21_P10**	**C12T28SOI_LR_-NAND3X24_P10**
A to Z ↓	0.0122	0.0119	1.2336	1.1044
A to Z ↑	0.0166	0.0163	0.8369	0.7394
B to Z ↓	0.0119	0.0118	1.2392	1.1094
B to Z ↑	0.0149	0.0146	0.8389	0.7413
C to Z ↓	0.0112	0.0110	1.2462	1.1159
C to Z ↑	0.0123	0.0121	0.8408	0.7422
	C12T28SOI_LR_-NAND3X35_P10	**C12T28SOI_LR_-NAND3X47_P10**	**C12T28SOI_LR_-NAND3X35_P10**	**C12T28SOI_LR_-NAND3X47_P10**
A to Z ↓	0.0112	0.0115	0.7529	0.5732
A to Z ↑	0.0158	0.0160	0.4954	0.3742
B to Z ↓	0.0114	0.0116	0.7566	0.5759
B to Z ↑	0.0141	0.0142	0.4960	0.3736
C to Z ↓	0.0107	0.0109	0.7613	0.5795
C to Z ↑	0.0116	0.0116	0.4992	0.3757
	C12T28SOI_-LRBR0P6_-NAND3X6_P10	**C12T28SOI_-LRBR0P6_-NAND3X12_P10**	**C12T28SOI_-LRBR0P6_-NAND3X6_P10**	**C12T28SOI_-LRBR0P6_-NAND3X12_P10**
A to Z ↓	0.0087	0.0093	2.7229	1.4392
A to Z ↑	0.0240	0.0240	4.4328	2.2632
B to Z ↓	0.0088	0.0082	2.7487	1.4537
B to Z ↑	0.0214	0.0203	4.4478	2.2689
C to Z ↓	0.0069	0.0061	2.7883	1.4758
C to Z ↑	0.0165	0.0151	4.4745	2.2770
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	**C12T28SOI_-LRBR0P6_-NAND3X24_P10**	**C12T28SOI_-LRBR0P6_-NAND3X18_P10**	**C12T28SOI_-LRBR0P6_-NAND3X24_P10**
A to Z ↓	0.0084	0.0089	0.9940	0.7522
A to Z ↑	0.0228	0.0232	1.5052	1.1369
B to Z ↓	0.0079	0.0079	1.0040	0.7598
B to Z ↑	0.0193	0.0197	1.5110	1.1401
C to Z ↓	0.0062	0.0061	1.0174	0.7709
C to Z ↑	0.0146	0.0146	1.5223	1.1429
	C12T28SOI_-LRBR0P6_-NAND3X35_P10	**C12T28SOI_-LRBR0P6_-NAND3X47_P10**	**C12T28SOI_-LRBR0P6_-NAND3X35_P10**	**C12T28SOI_-LRBR0P6_-NAND3X47_P10**

A to Z ↓	0.0084	0.0085	0.5141	0.3928
A to Z ↑	0.0231	0.0231	0.7796	0.5901
B to Z ↓	0.0077	0.0077	0.5199	0.3972
B to Z ↑	0.0195	0.0194	0.7817	0.5907
C to Z ↓	0.0059	0.0063	0.5276	0.4025
C to Z ↑	0.0142	0.0145	0.7904	0.5929
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P10**	
A to Z ↓	0.0091		0.9709	
A to Z ↑	0.0230		1.4495	
B to Z ↓	0.0078		0.9802	
B to Z ↑	0.0195		1.4532	
C to Z ↓	0.0057		0.9945	
C to Z ↑	0.0141		1.4445	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P10	3.714e-06	1.310e-09
C12T28SOI_LR_NAND3X6_P10	5.091e-06	1.310e-09
C12T28SOI_LR_NAND3X9_P10	7.308e-06	1.807e-09
C12T28SOI_LR_NAND3X12_P10	9.266e-06	1.807e-09
C12T28SOI_LR_NAND3X15_P10	1.098e-05	2.139e-09
C12T28SOI_LR_NAND3X18_P10	1.264e-05	2.139e-09
C12T28SOI_LR_NAND3X21_P10	1.573e-05	2.801e-09
C12T28SOI_LR_NAND3X24_P10	1.721e-05	2.801e-09
C12T28SOI_LR_NAND3X35_P10	2.519e-05	3.795e-09
C12T28SOI_LR_NAND3X47_P10	3.310e-05	4.789e-09
C12T28SOI_LRBR0P6_NAND3X6_-P10	6.361e-06	2.248e-09
C12T28SOI_LRBR0P6_NAND3X12_-P10	1.179e-05	2.790e-09
C12T28SOI_LRBR0P6_NAND3X18_-P10	1.607e-05	3.151e-09
C12T28SOI_LRBR0P6_NAND3X24_-P10	2.225e-05	3.874e-09
C12T28SOI_LRBR0P6_NAND3X35_-P10	3.281e-05	4.958e-09
C12T28SOI_LRBR0P6_NAND3X47_-P10	4.328e-05	6.042e-09
C12T28SOIDV_LRBR0P6_-NAND3X18_P10	1.856e-05	2.606e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A (output stable)	3.170e-05	4.308e-05	1.016e-04	1.200e-04
B (output stable)	8.300e-05	1.055e-04	2.561e-04	3.021e-04
C (output stable)	3.048e-04	3.599e-04	5.909e-04	6.818e-04
A to Z	2.016e-03	2.498e-03	4.071e-03	4.850e-03
B to Z	1.781e-03	2.168e-03	3.292e-03	3.934e-03
C to Z	1.408e-03	1.728e-03	2.545e-03	3.061e-03

	C12T28SOI_LR_-NAND3X15_P10	C12T28SOI_LR_-NAND3X18_P10	C12T28SOI_LR_-NAND3X21_P10	C12T28SOI_LR_-NAND3X24_P10
A (output stable)	1.364e-04	1.540e-04	2.086e-04	2.274e-04
B (output stable)	3.420e-04	3.942e-04	5.167e-04	5.709e-04
C (output stable)	7.393e-04	8.493e-04	1.140e-03	1.233e-03
A to Z	5.885e-03	6.602e-03	8.350e-03	9.177e-03
B to Z	4.793e-03	5.321e-03	6.766e-03	7.421e-03
C to Z	3.782e-03	4.154e-03	5.290e-03	5.784e-03
	C12T28SOI_LR_-NAND3X35_P10	C12T28SOI_LR_-NAND3X47_P10	C12T28SOI_-LRBR0P6_-NAND3X6_P10	C12T28SOI_-LRBR0P6_-NAND3X12_P10
A (output stable)	3.013e-04	3.966e-04	6.137e-05	1.695e-04
B (output stable)	7.602e-04	9.952e-04	1.538e-04	4.398e-04
C (output stable)	1.774e-03	2.284e-03	4.940e-04	9.796e-04
A to Z	1.302e-02	1.729e-02	2.718e-03	5.364e-03
B to Z	1.055e-02	1.404e-02	2.209e-03	3.996e-03
C to Z	8.053e-03	1.079e-02	1.519e-03	2.591e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	C12T28SOI_-LRBR0P6_-NAND3X24_P10	C12T28SOI_-LRBR0P6_-NAND3X35_P10	C12T28SOI_-LRBR0P6_-NAND3X47_P10
A (output stable)	2.113e-04	3.199e-04	4.342e-04	5.709e-04
B (output stable)	5.392e-04	8.160e-04	1.099e-03	1.453e-03
C (output stable)	1.142e-03	1.775e-03	2.583e-03	3.221e-03
A to Z	7.297e-03	1.009e-02	1.460e-02	1.906e-02
B to Z	5.439e-03	7.511e-03	1.080e-02	1.412e-02
C to Z	3.685e-03	4.907e-03	6.850e-03	9.105e-03
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10			
A (output stable)	2.457e-04			
B (output stable)	6.494e-04			
C (output stable)	1.405e-03			
A to Z	7.861e-03			
B to Z	5.841e-03			
C to Z	3.758e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A (output stable)	3.927e-08	3.450e-08	1.720e-08	-2.400e-08
B (output stable)	7.438e-08	4.922e-08	-4.721e-07	-1.310e-08
C (output stable)	7.437e-08	5.880e-08	-2.162e-06	-1.033e-09
A to Z	-4.150e-07	9.200e-07	4.600e-08	1.355e-06
B to Z	-1.950e-07	-1.220e-07	-1.220e-07	7.000e-07
C to Z	-4.210e-07	-2.250e-07	4.970e-07	1.020e-06
	C12T28SOI_LR_-NAND3X15_P10	C12T28SOI_LR_-NAND3X18_P10	C12T28SOI_LR_-NAND3X21_P10	C12T28SOI_LR_-NAND3X24_P10
A (output stable)	-7.150e-08	-1.050e-07	-1.121e-07	-1.407e-07
B (output stable)	-5.716e-07	-5.764e-07	-1.842e-06	-1.090e-06
C (output stable)	-1.692e-06	-1.641e-06	-4.690e-06	-3.436e-06
A to Z	1.890e-06	1.819e-06	2.226e-06	1.572e-06
B to Z	3.420e-07	1.635e-06	1.456e-06	2.839e-06

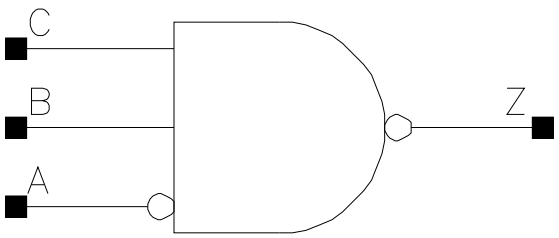
C to Z	9.020e-07	-1.800e-07	4.860e-07	-1.079e-06
	C12T28SOI_LR_-NAND3X35_P10	C12T28SOI_LR_-NAND3X47_P10	C12T28SOI_-LRBR0P6_-NAND3X6_P10	C12T28SOI_-LRBR0P6_-NAND3X12_P10
A (output stable)	-2.947e-07	-3.242e-07	7.780e-08	7.443e-08
B (output stable)	-1.795e-06	-2.292e-06	-8.551e-07	-2.719e-06
C (output stable)	-5.198e-06	-6.255e-06	-4.578e-06	-6.719e-06
A to Z	5.285e-06	6.427e-06	1.068e-06	1.608e-06
B to Z	4.800e-07	1.427e-06	4.100e-08	2.470e-07
C to Z	2.324e-06	3.095e-06	1.804e-06	7.430e-07
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	C12T28SOI_-LRBR0P6_-NAND3X24_P10	C12T28SOI_-LRBR0P6_-NAND3X35_P10	C12T28SOI_-LRBR0P6_-NAND3X47_P10
A (output stable)	-6.733e-09	-1.967e-09	-9.000e-08	-1.270e-07
B (output stable)	-2.129e-08	-3.448e-06	-2.139e-06	-9.595e-07
C (output stable)	-2.333e-10	-8.304e-06	-6.833e-06	-2.527e-06
A to Z	1.078e-06	2.179e-06	-6.930e-07	-6.770e-07
B to Z	1.963e-06	2.590e-06	3.159e-06	4.771e-06
C to Z	3.275e-06	4.968e-06	2.266e-06	8.667e-06
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10			
A (output stable)	-2.530e-08			
B (output stable)	-4.900e-09			
C (output stable)	-2.703e-08			
A to Z	1.883e-06			
B to Z	2.225e-06			
C to Z	3.338e-06			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.816	0.9792
X12_P10	1.200	1.224	1.4688
X18_P10	1.200	1.496	1.7952
X24_P10	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0009	0.0013	0.0013	0.0023
B	0.0010	0.0019	0.0029	0.0038
C	0.0010	0.0019	0.0027	0.0037

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X12_P10**	**X6_P10**	**X12_P10**
A to Z ↓	0.0305	0.0296	3.9765	2.1257
A to Z ↑	0.0220	0.0214	2.8355	1.4241
B to Z ↓	0.0109	0.0112	4.0189	2.1489
B to Z ↑	0.0145	0.0143	2.8958	1.4582
C to Z ↓	0.0111	0.0102	4.0457	2.1620
C to Z ↑	0.0126	0.0115	2.9143	1.4695
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0339	0.0290	1.4564	1.1034

A to Z ↑	0.0249	0.0204	0.9587	0.7183
B to Z ↓	0.0115	0.0112	1.4694	1.1151
B to Z ↑	0.0142	0.0141	0.9817	0.7378
C to Z ↓	0.0108	0.0103	1.4775	1.1219
C to Z ↑	0.0119	0.0114	0.9889	0.7438

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P10	6.914e-06	1.476e-09
X12_P10	1.352e-05	1.973e-09
X18_P10	1.670e-05	2.304e-09
X24_P10	2.637e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	1.834e-03	3.324e-03	4.451e-03	6.253e-03
B (output stable)	8.442e-05	2.596e-04	4.204e-04	5.774e-04
C (output stable)	1.681e-04	6.837e-04	8.632e-04	1.274e-03
A to Z	4.084e-03	7.982e-03	1.143e-02	1.538e-02
B to Z	1.868e-03	3.617e-03	5.356e-03	6.992e-03
C to Z	1.561e-03	2.737e-03	4.189e-03	5.283e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

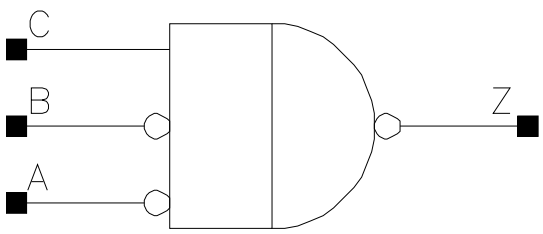
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	1.354e-07	5.143e-08	6.137e-08	-5.697e-08
B (output stable)	5.035e-08	-4.860e-07	-1.013e-07	-1.656e-06
C (output stable)	5.220e-08	-1.908e-06	-7.190e-08	-3.635e-06
A to Z	2.490e-07	1.143e-06	8.150e-07	2.735e-06
B to Z	3.360e-07	5.270e-07	2.141e-06	2.204e-06
C to Z	4.420e-07	5.900e-08	3.010e-07	3.040e-07

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	0.816	0.9792
X13_P10	1.200	1.088	1.3056
X20_P10	1.200	1.632	1.9584
X27_P10	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P10	X13_P10	X20_P10	X27_P10
A	0.0011	0.0011	0.0022	0.0021
B	0.0013	0.0012	0.0023	0.0022
C	0.0010	0.0019	0.0028	0.0037

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	**X13_P10**	**X7_P10**	**X13_P10**
A to Z ↓	0.0286	0.0350	2.7933	1.4870
A to Z ↑	0.0185	0.0216	2.8149	1.4160
B to Z ↓	0.0293	0.0360	2.7889	1.4872
B to Z ↑	0.0171	0.0204	2.8119	1.4157
C to Z ↓	0.0073	0.0068	2.8616	1.5171
C to Z ↑	0.0111	0.0102	2.9023	1.4658
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0322	0.0355	1.0125	0.7717
A to Z ↑	0.0201	0.0244	0.9541	0.7168
B to Z ↓	0.0311	0.0349	1.0111	0.7716

B to Z ↑	0.0181	0.0228	0.9532	0.7159
C to Z ↓	0.0079	0.0075	1.0353	0.7873
C to Z ↑	0.0110	0.0106	0.9871	0.7409

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X7_P10	1.014e-05	1.476e-09
X13_P10	1.404e-05	1.807e-09
X20_P10	2.195e-05	2.470e-09
X27_P10	2.438e-05	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	1.031e-03	1.383e-03	2.366e-03	2.775e-03
B (output stable)	8.702e-04	1.223e-03	1.910e-03	2.340e-03
C (output stable)	4.981e-05	4.066e-04	3.860e-04	4.322e-04
A to Z	4.521e-03	7.392e-03	1.174e-02	1.464e-02
B to Z	4.101e-03	6.987e-03	1.040e-02	1.345e-02
C to Z	1.290e-03	2.312e-03	3.763e-03	4.945e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

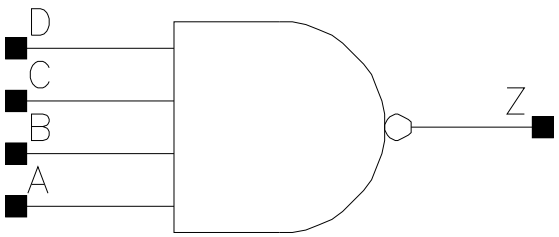
Pin Cycle (vdds)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	-1.272e-07	-1.367e-07	-2.130e-06	-2.283e-06
B (output stable)	1.558e-05	1.552e-05	7.169e-05	7.054e-05
C (output stable)	3.323e-08	-3.413e-08	-9.203e-08	-1.818e-07
A to Z	9.644e-07	6.554e-07	1.899e-06	1.875e-07
B to Z	1.009e-06	-3.140e-08	2.612e-06	-2.410e-07
C to Z	1.237e-06	2.620e-06	4.510e-06	4.320e-06

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0008	0.0007	0.0009	0.0011
B	0.0008	0.0008	0.0010	0.0012
C	0.0007	0.0008	0.0010	0.0012
D	0.0008	0.0008	0.0010	0.0012

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0438	0.0441	1.7908	0.8939
A to Z ↑	0.0375	0.0410	2.8723	1.4254
B to Z ↓	0.0453	0.0464	1.7893	0.8942
B to Z ↑	0.0359	0.0401	2.8700	1.4262
C to Z ↓	0.0438	0.0433	1.7908	0.8939
C to Z ↑	0.0383	0.0422	2.8719	1.4240

D to Z ↓	0.0457	0.0450	1.7902	0.8935
D to Z ↑	0.0370	0.0404	2.8699	1.4252
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0466	0.0431	0.6159	0.4604
A to Z ↑	0.0398	0.0393	0.9611	0.7206
B to Z ↓	0.0484	0.0445	0.6154	0.4600
B to Z ↑	0.0384	0.0377	0.9610	0.7204
C to Z ↓	0.0427	0.0396	0.6156	0.4603
C to Z ↑	0.0399	0.0392	0.9597	0.7198
D to Z ↓	0.0444	0.0412	0.6154	0.4604
D to Z ↑	0.0382	0.0375	0.9601	0.7199

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	1.367e-05	1.973e-09
X17_P10	2.054e-05	2.304e-09
X25_P10	2.940e-05	2.801e-09
X33_P10	3.682e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	7.335e-04	9.183e-04	1.343e-03	1.600e-03
B (output stable)	6.712e-04	8.603e-04	1.250e-03	1.480e-03
C (output stable)	7.199e-04	8.607e-04	1.316e-03	1.511e-03
D (output stable)	6.535e-04	7.914e-04	1.214e-03	1.387e-03
A to Z	5.425e-03	8.401e-03	1.297e-02	1.591e-02
B to Z	5.261e-03	8.246e-03	1.272e-02	1.560e-02
C to Z	5.499e-03	8.206e-03	1.209e-02	1.478e-02
D to Z	5.340e-03	8.030e-03	1.184e-02	1.447e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

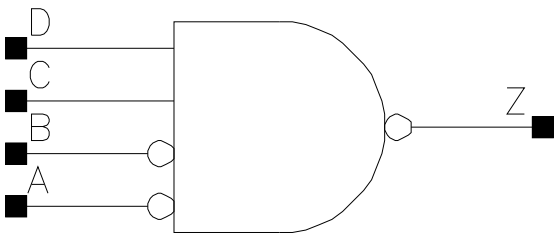
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	1.507e-07	9.569e-08	-1.312e-06	-9.610e-07
B (output stable)	1.276e-08	7.869e-08	-1.257e-06	-9.743e-07
C (output stable)	5.432e-06	1.016e-05	3.134e-05	3.750e-05
D (output stable)	5.456e-06	1.024e-05	3.139e-05	3.753e-05
A to Z	1.004e-06	7.608e-07	7.636e-07	2.305e-06
B to Z	3.367e-07	7.064e-07	5.755e-07	1.770e-06
C to Z	-2.666e-07	-2.454e-07	-5.570e-07	-9.550e-07
D to Z	-9.410e-08	-1.738e-07	-5.120e-07	-8.740e-07

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X12_P10	1.200	1.496	1.7952
X18_P10	1.200	2.040	2.4480
X24_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0012	0.0012	0.0023	0.0021
B	0.0012	0.0016	0.0023	0.0022
C	0.0010	0.0019	0.0028	0.0039
D	0.0009	0.0019	0.0027	0.0038

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X12_P10	X6_P10	X12_P10
A to Z ↓	0.0306	0.0408	4.0967	2.1336
A to Z ↑	0.0199	0.0246	2.8147	1.4184
B to Z ↓	0.0307	0.0409	4.0991	2.1340
B to Z ↑	0.0179	0.0230	2.8143	1.4179
C to Z ↓	0.0111	0.0112	4.1395	2.1481
C to Z ↑	0.0146	0.0143	3.0575	1.4581

D to Z ↓	0.0110	0.0101	4.1648	2.1606
D to Z ↑	0.0126	0.0115	3.0759	1.4690
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0354	0.0397	1.4535	1.1065
A to Z ↑	0.0215	0.0279	0.9551	0.7182
B to Z ↓	0.0344	0.0390	1.4537	1.1068
B to Z ↑	0.0196	0.0261	0.9538	0.7172
C to Z ↓	0.0112	0.0116	1.4655	1.1136
C to Z ↑	0.0140	0.0143	0.9852	0.7364
D to Z ↓	0.0106	0.0108	1.4742	1.1201
D to Z ↑	0.0117	0.0117	1.0047	0.7429

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P10	8.393e-06	1.642e-09
X12_P10	1.295e-05	2.304e-09
X18_P10	2.005e-05	2.967e-09
X24_P10	2.149e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	1.190e-03	1.956e-03	2.979e-03	3.591e-03
B (output stable)	9.970e-04	1.670e-03	2.418e-03	3.038e-03
C (output stable)	1.049e-04	2.998e-04	4.406e-04	6.227e-04
D (output stable)	2.069e-04	7.605e-04	9.301e-04	1.412e-03
A to Z	4.844e-03	9.082e-03	1.340e-02	1.761e-02
B to Z	4.459e-03	8.484e-03	1.213e-02	1.637e-02
C to Z	1.811e-03	3.622e-03	5.208e-03	7.260e-03
D to Z	1.504e-03	2.729e-03	4.134e-03	5.593e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

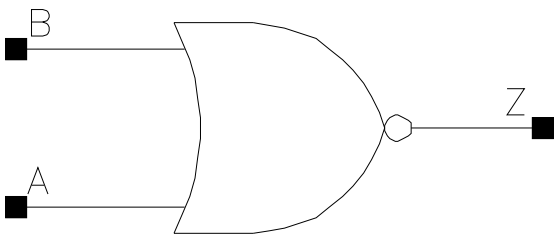
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	-4.725e-08	-1.704e-06	-1.613e-06	-2.229e-06
B (output stable)	1.420e-05	3.846e-05	6.142e-05	6.375e-05
C (output stable)	5.879e-08	-6.405e-07	-7.131e-07	-1.579e-06
D (output stable)	6.053e-08	-2.181e-06	-1.855e-06	-4.730e-06
A to Z	1.563e-06	1.784e-07	2.566e-06	3.900e-08
B to Z	1.685e-07	4.680e-07	2.408e-06	6.200e-08
C to Z	8.370e-07	5.390e-07	2.239e-06	1.068e-06
D to Z	4.380e-07	7.400e-08	1.250e-07	1.320e-07

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.408	0.4896
X5_P10	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X10_P10	1.200	0.680	0.8160
X14_P10	1.200	0.680	0.8160
X17_P10	1.200	0.952	1.1424
X21_P10	1.200	0.952	1.1424
X24_P10	1.200	1.224	1.4688
X27_P10	1.200	1.224	1.4688
X34_P10	1.200	1.496	1.7952
X40_P10	1.200	1.360	1.6320
X41_P10	1.200	1.768	2.1216
X49_P10	1.200	1.496	1.7952
X53_P10	1.200	1.904	2.2848
X55_P10	1.200	2.312	2.7744
X57_P10	1.200	1.904	2.2848
X65_P10	1.200	2.040	2.4480
X84_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P10	X5_P10	X7_P10	X10_P10
A	0.0007	0.0008	0.0010	0.0016
B	0.0007	0.0008	0.0010	0.0015
	X14_P10	X17_P10	X21_P10	X24_P10

A	0.0021	0.0026	0.0031	0.0036
B	0.0019	0.0024	0.0029	0.0034
	X27_P10	X34_P10	X40_P10	X41_P10
A	0.0040	0.0050	0.0011	0.0061
B	0.0038	0.0047	0.0012	0.0057
	X49_P10	X53_P10	X55_P10	X57_P10
A	0.0011	0.0012	0.0082	0.0012
B	0.0013	0.0011	0.0076	0.0011
	X65_P10	X84_P10		
A	0.0012	0.0013		
B	0.0011	0.0012		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X5_P10**	**X3_P10**	**X5_P10**
A to Z ↓	0.0076	0.0070	3.3722	2.4777
A to Z ↑	0.0165	0.0153	10.4946	7.7153
B to Z ↓	0.0061	0.0053	3.4564	2.5016
B to Z ↑	0.0167	0.0153	10.5505	7.7547
	X7_P10	**X10_P10**	**X7_P10**	**X10_P10**
A to Z ↓	0.0068	0.0071	1.8380	1.1828
A to Z ↑	0.0144	0.0164	5.5015	3.6522
B to Z ↓	0.0050	0.0045	1.8645	1.1976
B to Z ↑	0.0143	0.0136	5.5302	3.6727
	X14_P10	**X17_P10**	**X14_P10**	**X17_P10**
A to Z ↓	0.0069	0.0070	0.9074	0.7237
A to Z ↑	0.0154	0.0154	2.7287	2.1940
B to Z ↓	0.0043	0.0049	0.9195	0.7325
B to Z ↑	0.0129	0.0138	2.7459	2.2060
	X21_P10	**X24_P10**	**X21_P10**	**X24_P10**
A to Z ↓	0.0070	0.0069	0.6189	0.5264
A to Z ↑	0.0149	0.0151	1.8366	1.5961
B to Z ↓	0.0049	0.0046	0.6263	0.5334
B to Z ↑	0.0135	0.0132	1.8465	1.6056
	X27_P10	**X34_P10**	**X27_P10**	**X34_P10**
A to Z ↓	0.0068	0.0072	0.4685	0.3778
A to Z ↑	0.0145	0.0149	1.4103	1.1228
B to Z ↓	0.0044	0.0048	0.4750	0.3826
B to Z ↑	0.0128	0.0134	1.4188	1.1291
	X40_P10	**X41_P10**	**X40_P10**	**X41_P10**
A to Z ↓	0.0306	0.0069	0.3738	0.3148
A to Z ↑	0.0440	0.0146	0.5898	0.9300
B to Z ↓	0.0292	0.0045	0.3740	0.3192
B to Z ↑	0.0451	0.0127	0.5897	0.9356
	X49_P10	**X53_P10**	**X49_P10**	**X53_P10**
A to Z ↓	0.0323	0.0332	0.3110	0.2840
A to Z ↑	0.0457	0.0515	0.4909	0.4524
B to Z ↓	0.0309	0.0318	0.3113	0.2842
B to Z ↑	0.0469	0.0524	0.4910	0.4521
	X55_P10	**X57_P10**	**X55_P10**	**X57_P10**
A to Z ↓	0.0071	0.0335	0.2379	0.2676
A to Z ↑	0.0146	0.0517	0.7009	0.4219

B to Z ↓	0.0046	0.0321	0.2417	0.2677
B to Z ↑	0.0128	0.0526	0.7052	0.4220
	X65_P10	**X84_P10**	**X65_P10**	**X84_P10**
A to Z ↓	0.0346	0.0364	0.2350	0.1873
A to Z ↑	0.0527	0.0537	0.3695	0.2935
B to Z ↓	0.0332	0.0349	0.2351	0.1872
B to Z ↑	0.0536	0.0546	0.3694	0.2932

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P10	2.856e-06	9.792e-10
X5_P10	3.810e-06	9.792e-10
X7_P10	5.035e-06	9.792e-10
X10_P10	7.392e-06	1.310e-09
X14_P10	9.368e-06	1.310e-09
X17_P10	1.177e-05	1.642e-09
X21_P10	1.344e-05	1.642e-09
X24_P10	1.607e-05	1.973e-09
X27_P10	1.753e-05	1.973e-09
X34_P10	2.162e-05	2.304e-09
X40_P10	2.788e-05	2.139e-09
X41_P10	2.571e-05	2.635e-09
X49_P10	3.062e-05	2.304e-09
X53_P10	3.830e-05	2.801e-09
X55_P10	3.388e-05	3.298e-09
X57_P10	3.957e-05	2.801e-09
X65_P10	4.231e-05	2.967e-09
X84_P10	4.785e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	3.250e-05	4.256e-05	5.890e-05	1.676e-04
B (output stable)	1.431e-05	1.969e-05	2.889e-05	1.116e-04
A to Z	9.698e-04	1.201e-03	1.596e-03	2.740e-03
B to Z	7.496e-04	9.132e-04	1.192e-03	1.715e-03
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	1.967e-04	2.394e-04	2.698e-04	3.323e-04
B (output stable)	1.329e-04	1.562e-04	1.575e-04	1.931e-04
A to Z	3.414e-03	4.314e-03	4.973e-03	5.862e-03
B to Z	2.183e-03	2.922e-03	3.375e-03	3.876e-03
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	3.479e-04	4.351e-04	5.956e-05	5.455e-04
B (output stable)	2.052e-04	2.331e-04	2.907e-05	3.266e-04
A to Z	6.336e-03	8.152e-03	1.541e-02	9.608e-03
B to Z	4.212e-03	5.569e-03	1.502e-02	6.314e-03
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	5.973e-05	6.066e-05	7.225e-04	6.061e-05
B (output stable)	2.882e-05	2.995e-05	4.134e-04	2.987e-05
A to Z	1.759e-02	2.141e-02	1.272e-02	2.213e-02
B to Z	1.719e-02	2.099e-02	8.379e-03	2.171e-02
	X65_P10	X84_P10		

A (output stable)	6.071e-05	6.223e-05		
B (output stable)	2.997e-05	3.115e-05		
A to Z	2.416e-02	2.889e-02		
B to Z	2.374e-02	2.839e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

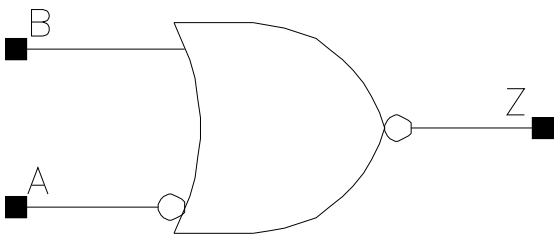
Pin Cycle (vdds)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	-3.273e-07	-2.986e-07	-3.807e-07	-3.916e-06
B (output stable)	1.330e-05	1.717e-05	2.261e-05	9.662e-05
A to Z	1.215e-07	1.502e-06	2.650e-06	2.895e-06
B to Z	1.436e-07	6.950e-07	1.013e-06	3.639e-07
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	-3.941e-06	-3.000e-06	-2.910e-06	-5.831e-06
B (output stable)	1.158e-04	8.591e-05	8.677e-05	1.559e-04
A to Z	3.972e-06	6.196e-06	7.688e-06	6.622e-06
B to Z	2.622e-07	1.149e-06	2.163e-06	4.190e-07
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	-4.815e-06	-4.606e-06	-3.605e-07	-7.130e-06
B (output stable)	1.452e-04	1.445e-04	2.245e-05	2.127e-04
A to Z	6.326e-06	1.144e-05	1.600e-08	9.212e-06
B to Z	1.178e-06	1.731e-06	-3.640e-07	1.594e-06
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	-3.661e-07	-3.244e-07	-9.038e-06	-3.245e-07
B (output stable)	2.236e-05	2.388e-05	2.644e-04	2.388e-05
A to Z	-1.140e-07	-3.030e-07	1.195e-05	-2.650e-07
B to Z	-1.680e-07	-3.570e-07	1.937e-06	-3.610e-07
	X65_P10	X84_P10		
A (output stable)	-3.234e-07	-3.411e-07		
B (output stable)	2.388e-05	2.457e-05		
A to Z	-2.790e-07	-5.090e-07		
B to Z	-4.070e-07	-5.740e-07		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X7_P10	1.200	0.680	0.8160
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X41_P10	1.200	2.312	2.7744
X55_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X7_P10	X13_P10
A	0.0009	0.0009	0.0009	0.0013
B	0.0007	0.0010	0.0010	0.0019
	X27_P10	X41_P10	X55_P10	
A	0.0024	0.0035	0.0046	
B	0.0038	0.0057	0.0076	

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0243	0.0271	3.1969	2.1363
A to Z ↑	0.0218	0.0220	10.3845	5.4627
B to Z ↓	0.0064	0.0063	3.4293	2.2923
B to Z ↑	0.0169	0.0140	10.5306	5.5428

	X7_P10	X13_P10	X7_P10	X13_P10
A to Z ↓	0.0273	0.0251	1.7157	0.9289
A to Z ↑	0.0241	0.0230	5.4179	2.8750
B to Z ↓	0.0052	0.0047	1.7875	0.9657
B to Z ↑	0.0151	0.0139	5.4780	2.9125
	X27_P10	**X41_P10**	**X27_P10**	**X41_P10**
A to Z ↓	0.0245	0.0247	0.4452	0.3010
A to Z ↑	0.0222	0.0222	1.3779	0.9247
B to Z ↓	0.0046	0.0045	0.4770	0.3214
B to Z ↑	0.0133	0.0129	1.3962	0.9370
	X55_P10		**X55_P10**	
A to Z ↓	0.0245		0.2277	
A to Z ↑	0.0220		0.6976	
B to Z ↓	0.0046		0.2432	
B to Z ↑	0.0129		0.7071	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P10	5.093e-06	1.145e-09
X6_P10	6.727e-06	1.145e-09
X7_P10	8.063e-06	1.310e-09
X13_P10	1.406e-05	1.642e-09
X27_P10	2.623e-05	2.470e-09
X41_P10	3.798e-05	3.298e-09
X55_P10	4.971e-05	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	1.463e-03	1.829e-03	1.948e-03	3.216e-03
B (output stable)	3.626e-05	6.601e-05	1.308e-04	2.754e-04
A to Z	2.458e-03	3.386e-03	3.895e-03	6.647e-03
B to Z	7.615e-04	1.148e-03	1.352e-03	2.300e-03
	X27_P10	X41_P10	X55_P10	
A (output stable)	6.403e-03	9.583e-03	1.261e-02	
B (output stable)	5.687e-04	7.809e-04	1.032e-03	
A to Z	1.332e-02	1.951e-02	2.575e-02	
B to Z	4.506e-03	6.469e-03	8.588e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

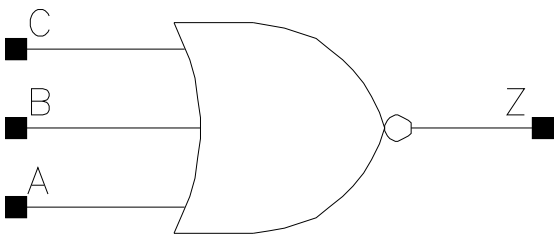
Pin Cycle (vdds)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	2.161e-07	9.188e-07	-4.489e-07	-8.176e-07
B (output stable)	1.305e-05	2.225e-05	6.150e-05	1.021e-04
A to Z	1.378e-06	2.044e-06	2.658e-06	4.629e-06
B to Z	1.339e-07	4.215e-07	4.344e-07	4.375e-07
	X27_P10	X41_P10	X55_P10	
A (output stable)	-4.042e-06	-9.920e-07	-6.424e-06	
B (output stable)	1.695e-04	2.030e-04	2.684e-04	
A to Z	2.491e-06	2.443e-06	3.643e-06	
B to Z	5.020e-07	6.490e-07	2.141e-06	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X9_P10	1.200	0.952	1.1424
X13_P10	1.200	0.952	1.1424
X16_P10	1.200	1.360	1.6320
X19_P10	1.200	1.496	1.7952
X22_P10	1.200	1.768	2.1216
X25_P10	1.200	1.904	2.2848
X37_P10	1.200	2.584	3.1008
X49_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P10	X6_P10	X9_P10	X13_P10
A	0.0008	0.0010	0.0016	0.0019
B	0.0008	0.0010	0.0017	0.0021
C	0.0008	0.0010	0.0015	0.0018
	X16_P10	X19_P10	X22_P10	X25_P10
A	0.0026	0.0030	0.0036	0.0040
B	0.0026	0.0034	0.0037	0.0046
C	0.0024	0.0028	0.0033	0.0037
	X37_P10	X49_P10		
A	0.0060	0.0081		
B	0.0060	0.0081		

C	0.0054	0.0075		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0090	0.0085	2.5116	1.8633
A to Z ↑	0.0232	0.0214	11.4664	8.1646
B to Z ↓	0.0083	0.0078	2.5165	1.8662
B to Z ↑	0.0220	0.0201	11.4823	8.1771
C to Z ↓	0.0068	0.0061	2.5403	1.8878
C to Z ↑	0.0207	0.0185	11.5066	8.1940
	X9_P10	**X13_P10**	**X9_P10**	**X13_P10**
A to Z ↓	0.0089	0.0087	1.2175	0.9416
A to Z ↑	0.0234	0.0220	5.3998	4.0549
B to Z ↓	0.0081	0.0076	1.1895	0.9066
B to Z ↑	0.0230	0.0211	5.4083	4.0614
C to Z ↓	0.0056	0.0053	1.2018	0.9233
C to Z ↑	0.0174	0.0163	5.4157	4.0663
	X16_P10	**X19_P10**	**X16_P10**	**X19_P10**
A to Z ↓	0.0088	0.0086	0.7287	0.6196
A to Z ↑	0.0225	0.0222	3.2654	2.7146
B to Z ↓	0.0082	0.0080	0.7307	0.6080
B to Z ↑	0.0218	0.0220	3.2705	2.7188
C to Z ↓	0.0059	0.0057	0.7359	0.6316
C to Z ↑	0.0180	0.0171	3.2762	2.7237
	X22_P10	**X25_P10**	**X22_P10**	**X25_P10**
A to Z ↓	0.0087	0.0086	0.5365	0.4715
A to Z ↑	0.0221	0.0221	2.3343	2.0410
B to Z ↓	0.0079	0.0078	0.5283	0.4558
B to Z ↑	0.0214	0.0219	2.3376	2.0442
C to Z ↓	0.0053	0.0053	0.5346	0.4731
C to Z ↑	0.0166	0.0162	2.3420	2.0474
	X37_P10	**X49_P10**	**X37_P10**	**X49_P10**
A to Z ↓	0.0086	0.0088	0.3232	0.2451
A to Z ↑	0.0215	0.0216	1.3678	1.0302
B to Z ↓	0.0078	0.0080	0.3201	0.2430
B to Z ↑	0.0204	0.0205	1.3703	1.0320
C to Z ↓	0.0057	0.0058	0.3250	0.2464
C to Z ↑	0.0163	0.0166	1.3727	1.0341

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	3.312e-06	1.145e-09
X6_P10	4.399e-06	1.145e-09
X9_P10	6.599e-06	1.642e-09
X13_P10	8.424e-06	1.642e-09
X16_P10	1.061e-05	2.139e-09
X19_P10	1.284e-05	2.304e-09
X22_P10	1.463e-05	2.635e-09
X25_P10	1.678e-05	2.801e-09
X37_P10	2.391e-05	3.629e-09

X49_P10	3.169e-05	4.623e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	7.807e-05	9.541e-05	2.677e-04	3.023e-04
B (output stable)	-1.115e-05	-1.610e-05	1.965e-05	1.002e-05
C (output stable)	1.644e-05	2.419e-05	7.555e-05	9.198e-05
A to Z	1.738e-03	2.232e-03	3.715e-03	4.616e-03
B to Z	1.407e-03	1.780e-03	3.085e-03	3.744e-03
C to Z	1.108e-03	1.358e-03	1.977e-03	2.427e-03
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	3.416e-04	4.215e-04	5.167e-04	6.064e-04
B (output stable)	-1.033e-06	1.682e-06	1.212e-05	1.545e-05
C (output stable)	1.028e-04	1.283e-04	1.510e-04	1.741e-04
A to Z	5.917e-03	7.004e-03	8.095e-03	9.263e-03
B to Z	4.826e-03	5.796e-03	6.583e-03	7.640e-03
C to Z	3.390e-03	3.840e-03	4.323e-03	4.797e-03
	X37_P10	X49_P10		
A (output stable)	8.190e-04	1.060e-03		
B (output stable)	-1.731e-06	-1.858e-05		
C (output stable)	2.581e-04	3.355e-04		
A to Z	1.339e-02	1.788e-02		
B to Z	1.075e-02	1.432e-02		
C to Z	7.058e-03	9.561e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

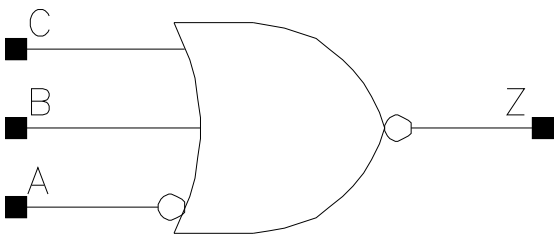
Pin Cycle (vdds)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	-5.361e-06	-5.710e-06	-2.710e-05	-2.818e-05
B (output stable)	1.817e-05	2.514e-05	4.552e-05	5.727e-05
C (output stable)	3.082e-05	4.319e-05	1.093e-04	1.421e-04
A to Z	4.090e-07	1.369e-06	3.730e-07	1.194e-06
B to Z	4.140e-07	3.480e-07	3.820e-07	3.402e-06
C to Z	1.138e-07	1.282e-07	1.790e-07	1.962e-07
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	-2.462e-05	-3.271e-05	-4.266e-05	-5.220e-05
B (output stable)	6.537e-05	9.133e-05	9.878e-05	1.311e-04
C (output stable)	1.204e-04	1.680e-04	2.063e-04	2.546e-04
A to Z	1.744e-06	4.423e-06	6.058e-06	6.714e-06
B to Z	5.960e-07	4.695e-06	-4.400e-08	6.419e-06
C to Z	6.930e-07	-6.030e-07	4.195e-07	6.450e-07
	X37_P10	X49_P10		
A (output stable)	-6.314e-05	-7.488e-05		
B (output stable)	1.636e-04	2.099e-04		
C (output stable)	3.329e-04	3.963e-04		
A to Z	1.040e-05	1.263e-05		
B to Z	8.917e-06	1.193e-05		
C to Z	8.090e-07	1.345e-06		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.680	0.8160
X13_P10	1.200	1.224	1.4688
X19_P10	1.200	1.496	1.7952
X25_P10	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0009	0.0012	0.0013	0.0024
B	0.0010	0.0021	0.0030	0.0040
C	0.0010	0.0019	0.0028	0.0037

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X13_P10**	**X6_P10**	**X13_P10**
A to Z ↓	0.0273	0.0265	1.7847	0.9851
A to Z ↑	0.0296	0.0293	8.2397	4.0470
B to Z ↓	0.0079	0.0077	1.8732	0.9114
B to Z ↑	0.0204	0.0211	8.2769	4.0621
C to Z ↓	0.0062	0.0051	1.8887	0.9244
C to Z ↑	0.0188	0.0161	8.2943	4.0667
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0303	0.0264	0.6038	0.4572

A to Z ↑	0.0321	0.0292	2.7241	2.0433
B to Z ↓	0.0081	0.0078	0.6311	0.4712
B to Z ↑	0.0206	0.0206	2.7363	2.0518
C to Z ↓	0.0057	0.0053	0.6325	0.4757
C to Z ↑	0.0172	0.0163	2.7410	2.0556

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P10	6.711e-06	1.310e-09
X13_P10	1.337e-05	1.973e-09
X19_P10	1.642e-05	2.304e-09
X25_P10	2.530e-05	3.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	1.916e-03	3.577e-03	4.614e-03	6.942e-03
B (output stable)	1.093e-05	8.084e-05	7.897e-05	1.314e-04
C (output stable)	4.309e-05	1.715e-04	1.888e-04	2.895e-04
A to Z	4.180e-03	8.309e-03	1.145e-02	1.604e-02
B to Z	1.792e-03	3.755e-03	5.445e-03	7.236e-03
C to Z	1.378e-03	2.399e-03	3.813e-03	4.786e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

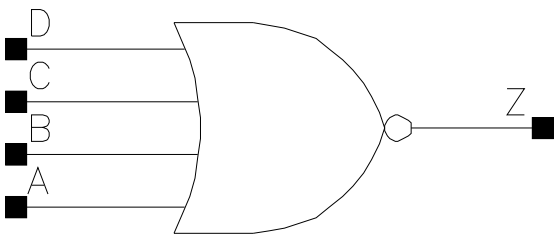
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	-4.585e-06	-2.205e-05	-2.348e-05	-3.994e-05
B (output stable)	2.495e-05	5.194e-05	7.627e-05	1.046e-04
C (output stable)	4.268e-05	1.453e-04	1.520e-04	2.430e-04
A to Z	2.716e-06	5.694e-06	4.590e-06	4.326e-06
B to Z	2.930e-07	3.254e-06	4.843e-06	7.052e-06
C to Z	1.735e-06	-1.385e-07	-6.490e-07	2.530e-07

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	1.904	2.2848
X32_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X32_P10
A	0.0008	0.0008	0.0009	0.0011
B	0.0008	0.0008	0.0010	0.0013
C	0.0007	0.0007	0.0009	0.0011
D	0.0007	0.0007	0.0010	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0309	0.0311	1.7544	0.8622
A to Z ↑	0.0466	0.0503	2.9197	1.4421
B to Z ↓	0.0294	0.0300	1.7553	0.8621
B to Z ↑	0.0472	0.0513	2.9188	1.4429
C to Z ↓	0.0302	0.0310	1.7514	0.8599
C to Z ↑	0.0477	0.0523	2.9215	1.4420

D to Z ↓	0.0294	0.0303	1.7514	0.8602
D to Z ↑	0.0487	0.0537	2.9212	1.4425
	X25_P10	**X32_P10**	**X25_P10**	**X32_P10**
A to Z ↓	0.0321	0.0343	0.5990	0.4699
A to Z ↑	0.0501	0.0489	0.9848	0.7472
B to Z ↓	0.0310	0.0331	0.5977	0.4702
B to Z ↑	0.0513	0.0497	0.9853	0.7468
C to Z ↓	0.0309	0.0335	0.5952	0.4681
C to Z ↑	0.0500	0.0493	0.9852	0.7462
D to Z ↓	0.0297	0.0316	0.5957	0.4682
D to Z ↑	0.0510	0.0500	0.9843	0.7459

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	9.821e-06	1.973e-09
X17_P10	1.385e-05	2.139e-09
X25_P10	2.067e-05	2.801e-09
X32_P10	2.461e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	7.411e-04	9.122e-04	1.288e-03	1.639e-03
B (output stable)	6.330e-04	8.054e-04	1.143e-03	1.435e-03
C (output stable)	6.848e-04	8.128e-04	1.261e-03	1.609e-03
D (output stable)	5.779e-04	7.097e-04	1.110e-03	1.407e-03
A to Z	5.110e-03	7.928e-03	1.208e-02	1.520e-02
B to Z	4.880e-03	7.716e-03	1.176e-02	1.482e-02
C to Z	5.139e-03	7.871e-03	1.136e-02	1.437e-02
D to Z	4.898e-03	7.656e-03	1.106e-02	1.396e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

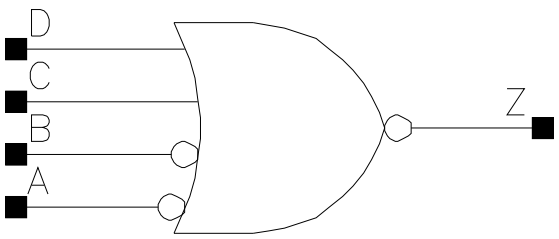
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	-1.296e-07	-7.121e-08	-9.128e-08	-5.839e-08
B (output stable)	7.309e-06	6.952e-06	1.031e-05	1.380e-05
C (output stable)	-5.158e-08	-4.653e-08	-2.875e-08	-1.199e-08
D (output stable)	7.806e-06	7.526e-06	1.058e-05	1.356e-05
A to Z	1.990e-07	1.870e-07	3.900e-08	9.740e-08
B to Z	3.923e-07	1.409e-07	4.044e-07	5.530e-08
C to Z	3.070e-07	3.652e-07	1.200e-07	1.740e-07
D to Z	4.201e-07	1.632e-07	-7.490e-08	1.644e-07

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X13_P10	1.200	1.496	1.7952
X19_P10	1.200	2.040	2.4480
X25_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0012	0.0012	0.0023	0.0023
B	0.0012	0.0017	0.0023	0.0024
C	0.0010	0.0020	0.0029	0.0038
D	0.0010	0.0019	0.0028	0.0037

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X13_P10	X6_P10	X13_P10
A to Z ↓	0.0241	0.0298	1.7356	0.8725
A to Z ↑	0.0290	0.0358	7.9468	4.1103
B to Z ↓	0.0222	0.0284	1.7351	0.8713
B to Z ↑	0.0299	0.0374	7.9482	4.1116
C to Z ↓	0.0084	0.0077	1.8971	0.9114
C to Z ↑	0.0205	0.0211	7.9902	4.1290

D to Z ↓	0.0064	0.0052	1.9027	0.9222
D to Z ↑	0.0187	0.0165	8.0024	4.1337
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0265	0.0290	0.5961	0.4495
A to Z ↑	0.0325	0.0352	2.7257	2.0600
B to Z ↓	0.0241	0.0270	0.5953	0.4490
B to Z ↑	0.0330	0.0363	2.7254	2.0599
C to Z ↓	0.0081	0.0079	0.6312	0.4730
C to Z ↑	0.0206	0.0205	2.7369	2.0671
D to Z ↓	0.0057	0.0053	0.6328	0.4755
D to Z ↑	0.0171	0.0162	2.7409	2.0702

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P10	8.028e-06	1.642e-09
X13_P10	1.189e-05	2.304e-09
X19_P10	1.890e-05	2.967e-09
X25_P10	2.186e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	1.173e-03	1.989e-03	3.007e-03	3.676e-03
B (output stable)	1.054e-03	1.881e-03	2.768e-03	3.473e-03
C (output stable)	-5.374e-07	6.521e-05	7.211e-05	1.315e-04
D (output stable)	5.050e-05	2.108e-04	2.474e-04	4.170e-04
A to Z	5.027e-03	9.325e-03	1.403e-02	1.797e-02
B to Z	4.731e-03	8.862e-03	1.309e-02	1.711e-02
C to Z	1.856e-03	3.708e-03	5.422e-03	7.129e-03
D to Z	1.426e-03	2.434e-03	3.816e-03	4.710e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

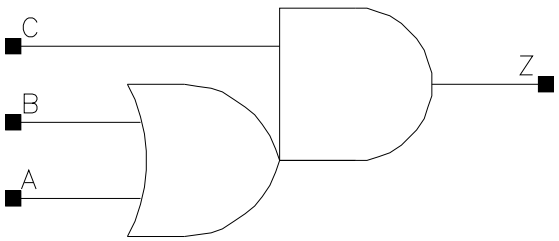
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	-1.941e-06	-1.379e-05	-1.411e-05	-2.239e-05
B (output stable)	-2.038e-06	-1.496e-05	-1.513e-05	-2.378e-05
C (output stable)	3.274e-05	6.130e-05	9.181e-05	1.186e-04
D (output stable)	5.260e-05	1.641e-04	1.762e-04	2.775e-04
A to Z	3.257e-06	9.680e-07	4.795e-06	2.514e-06
B to Z	2.633e-06	1.707e-06	3.977e-06	3.984e-06
C to Z	5.620e-07	3.327e-06	7.750e-07	6.749e-06
D to Z	1.137e-07	-2.220e-07	4.950e-07	5.850e-07

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0011	0.0011	0.0021
B	0.0012	0.0012	0.0024
C	0.0012	0.0012	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0261	0.0307	1.8067	0.9011
A to Z ↑	0.0213	0.0242	2.9352	1.4459
B to Z ↓	0.0265	0.0316	1.8088	0.9010
B to Z ↑	0.0189	0.0220	2.9340	1.4438
C to Z ↓	0.0238	0.0265	1.7852	0.8843
C to Z ↑	0.0196	0.0220	2.9340	1.4427
	X33_P10		**X33_P10**	
A to Z ↓	0.0320		0.4579	
A to Z ↑	0.0261		0.7262	

B to Z ↓	0.0328		0.4580	
B to Z ↑	0.0234		0.7244	
C to Z ↓	0.0273		0.4488	
C to Z ↑	0.0231		0.7241	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	9.315e-06	1.310e-09
X17_P10	1.282e-05	1.476e-09
X33_P10	2.568e-05	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.215e-04	1.227e-04	2.540e-04
B (output stable)	1.166e-04	1.181e-04	2.315e-04
C (output stable)	8.032e-05	8.331e-05	1.581e-04
A to Z	3.880e-03	5.945e-03	1.246e-02
B to Z	3.450e-03	5.504e-03	1.159e-02
C to Z	4.218e-03	6.113e-03	1.276e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

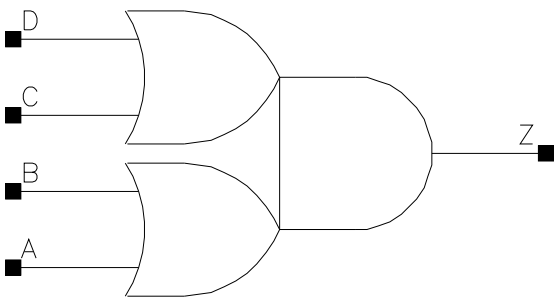
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-4.995e-07	-5.695e-07	-1.233e-06
B (output stable)	7.227e-06	7.349e-06	1.553e-05
C (output stable)	4.797e-08	5.965e-08	-3.440e-08
A to Z	2.074e-07	2.460e-07	2.000e-07
B to Z	9.510e-08	8.956e-08	4.510e-08
C to Z	-4.665e-08	-1.284e-07	-2.767e-07

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0011	0.0022
B	0.0008	0.0012	0.0022
C	0.0008	0.0012	0.0023
D	0.0008	0.0012	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0436	0.0379	1.7807	0.9003
A to Z ↑	0.0288	0.0256	2.8802	1.4408
B to Z ↓	0.0450	0.0391	1.7810	0.9005
B to Z ↑	0.0274	0.0240	2.8774	1.4392

C to Z ↓	0.0378	0.0334	1.7627	0.8942
C to Z ↑	0.0284	0.0262	2.8778	1.4407
D to Z ↓	0.0384	0.0340	1.7633	0.8945
D to Z ↑	0.0264	0.0238	2.8744	1.4381
	X33_P10		**X33_P10**	
A to Z ↓	0.0386		0.4627	
A to Z ↑	0.0257		0.7239	
B to Z ↓	0.0381		0.4631	
B to Z ↑	0.0235		0.7230	
C to Z ↓	0.0334		0.4592	
C to Z ↑	0.0256		0.7237	
D to Z ↓	0.0325		0.4592	
D to Z ↑	0.0232		0.7224	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	9.263e-06	1.642e-09
X17_P10	1.717e-05	1.807e-09
X33_P10	3.222e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	3.305e-05	5.430e-05	1.583e-04
B (output stable)	2.082e-05	3.431e-05	1.296e-04
C (output stable)	1.020e-04	1.315e-04	3.049e-04
D (output stable)	8.975e-05	1.101e-04	2.961e-04
A to Z	4.615e-03	7.641e-03	1.504e-02
B to Z	4.375e-03	7.179e-03	1.374e-02
C to Z	3.989e-03	6.769e-03	1.317e-02
D to Z	3.750e-03	6.314e-03	1.192e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

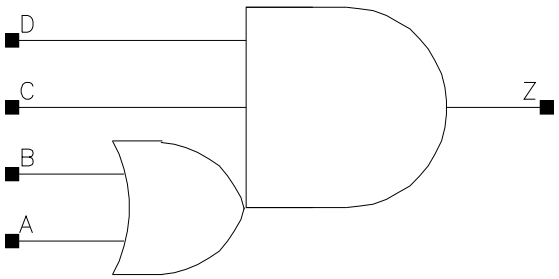
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-1.752e-07	-1.834e-07	-2.589e-06
B (output stable)	7.919e-06	1.404e-05	6.974e-05
C (output stable)	-6.502e-07	-2.504e-07	-2.981e-06
D (output stable)	7.755e-06	1.463e-05	6.254e-05
A to Z	-7.604e-08	-2.673e-07	3.271e-06
B to Z	-1.722e-07	-9.533e-08	8.528e-07
C to Z	1.876e-07	1.338e-07	3.997e-06
D to Z	1.570e-09	-1.232e-07	7.162e-07

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	1.088	1.3056
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0008	0.0012	0.0019	0.0023
B	0.0007	0.0012	0.0020	0.0023
C	0.0008	0.0012	0.0020	0.0023
D	0.0008	0.0012	0.0019	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0368	0.0350	1.8533	0.9027
A to Z ↑	0.0339	0.0319	2.9715	1.4434
B to Z ↓	0.0380	0.0347	1.8549	0.9030
B to Z ↑	0.0319	0.0286	2.9747	1.4410
C to Z ↓	0.0313	0.0292	1.8069	0.8840

C to Z ↑	0.0311	0.0287	2.9715	1.4415
D to Z ↓	0.0303	0.0281	1.8057	0.8834
D to Z ↑	0.0326	0.0300	2.9704	1.4417
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0367	0.0356	0.6151	0.4605
A to Z ↑	0.0328	0.0336	0.9793	0.7345
B to Z ↓	0.0362	0.0352	0.6154	0.4605
B to Z ↑	0.0299	0.0305	0.9778	0.7326
C to Z ↓	0.0308	0.0298	0.6020	0.4508
C to Z ↑	0.0299	0.0301	0.9779	0.7324
D to Z ↓	0.0292	0.0284	0.6008	0.4501
D to Z ↑	0.0303	0.0308	0.9774	0.7329

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	5.766e-06	1.476e-09
X17_P10	1.108e-05	1.807e-09
X25_P10	1.789e-05	2.801e-09
X33_P10	2.218e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	1.113e-04	2.100e-04	3.575e-04	3.961e-04
B (output stable)	1.098e-04	2.037e-04	3.577e-04	3.916e-04
C (output stable)	2.399e-05	4.791e-05	1.146e-04	1.276e-04
D (output stable)	5.099e-05	1.018e-04	3.211e-04	3.460e-04
A to Z	3.848e-03	6.904e-03	1.121e-02	1.410e-02
B to Z	3.621e-03	6.286e-03	1.023e-02	1.284e-02
C to Z	4.120e-03	7.259e-03	1.206e-02	1.485e-02
D to Z	3.938e-03	6.916e-03	1.121e-02	1.393e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

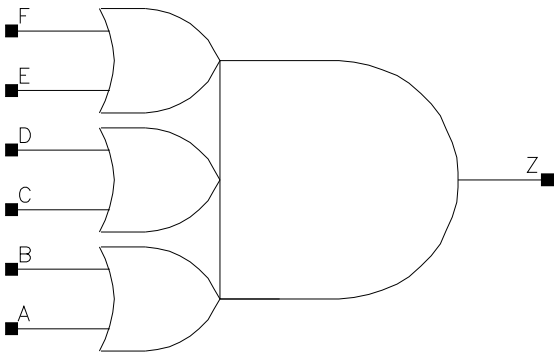
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	-8.047e-07	-1.522e-06	-2.193e-06	-1.259e-06
B (output stable)	1.257e-06	8.294e-06	1.076e-05	1.423e-05
C (output stable)	8.072e-08	5.664e-08	4.530e-08	1.208e-08
D (output stable)	-7.250e-08	-1.347e-07	-2.774e-07	1.030e-08
A to Z	1.844e-07	-1.010e-07	-3.110e-07	-9.960e-07
B to Z	-7.028e-08	-1.599e-07	-3.867e-07	-6.250e-07
C to Z	5.537e-08	1.921e-06	4.246e-06	3.275e-06
D to Z	-5.600e-09	1.670e-06	3.434e-06	3.027e-06

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0008	0.0011	0.0020
B	0.0008	0.0012	0.0022
C	0.0008	0.0011	0.0021
D	0.0008	0.0012	0.0022
E	0.0008	0.0011	0.0021
F	0.0008	0.0012	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0498	0.0433	1.9092	0.9241
A to Z ↑	0.0368	0.0338	2.9568	1.4549
B to Z ↓	0.0511	0.0447	1.9097	0.9243
B to Z ↑	0.0352	0.0323	2.9572	1.4561
C to Z ↓	0.0454	0.0408	1.8943	0.9210
C to Z ↑	0.0373	0.0339	2.9581	1.4553
D to Z ↓	0.0469	0.0418	1.8945	0.9217
D to Z ↑	0.0354	0.0319	2.9552	1.4554
E to Z ↓	0.0391	0.0356	1.8742	0.9138
E to Z ↑	0.0351	0.0326	2.9543	1.4545
F to Z ↓	0.0406	0.0363	1.8742	0.9142
F to Z ↑	0.0331	0.0304	2.9518	1.4532
	X33_P10		**X33_P10**	
A to Z ↓	0.0440		0.4725	
A to Z ↑	0.0350		0.7342	
B to Z ↓	0.0453		0.4725	
B to Z ↑	0.0323		0.7328	
C to Z ↓	0.0403		0.4689	
C to Z ↑	0.0349		0.7342	
D to Z ↓	0.0414		0.4692	
D to Z ↑	0.0324		0.7324	
E to Z ↓	0.0352		0.4654	
E to Z ↑	0.0337		0.7332	
F to Z ↓	0.0362		0.4655	
F to Z ↑	0.0309		0.7319	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	9.215e-06	1.973e-09
X17_P10	1.679e-05	2.139e-09
X33_P10	3.199e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.936e-05	5.072e-05	9.545e-05
B (output stable)	2.089e-05	4.114e-05	7.157e-05
C (output stable)	5.906e-05	9.576e-05	1.932e-04
D (output stable)	5.239e-05	8.288e-05	1.696e-04
E (output stable)	1.761e-04	2.546e-04	4.894e-04
F (output stable)	1.629e-04	2.365e-04	4.627e-04
A to Z	5.350e-03	9.004e-03	1.784e-02
B to Z	5.096e-03	8.551e-03	1.691e-02
C to Z	4.854e-03	8.283e-03	1.626e-02
D to Z	4.611e-03	7.824e-03	1.535e-02
E to Z	4.212e-03	7.330e-03	1.443e-02
F to Z	3.994e-03	6.886e-03	1.356e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

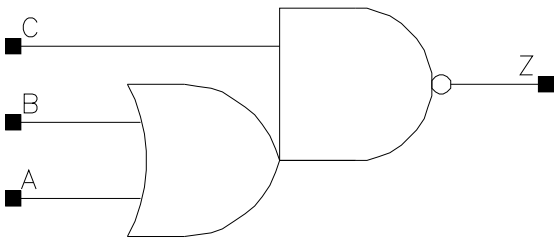
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-8.127e-08	-1.023e-07	-2.902e-07
B (output stable)	5.221e-06	9.718e-06	1.840e-05
C (output stable)	-1.816e-07	-1.294e-07	-7.681e-07
D (output stable)	5.095e-06	9.698e-06	1.807e-05
E (output stable)	-8.611e-07	-1.837e-07	-1.803e-06
F (output stable)	4.754e-06	9.623e-06	1.690e-05
A to Z	-9.343e-08	-4.150e-07	-8.990e-07
B to Z	-2.277e-07	-4.641e-07	-7.990e-07
C to Z	8.814e-08	-7.033e-08	9.744e-08
D to Z	-1.070e-07	-3.268e-07	-3.696e-07
E to Z	2.762e-07	2.780e-07	7.896e-07
F to Z	2.298e-07	2.036e-07	2.088e-07

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X34_P10	1.200	2.720	3.2640
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X34_P10	X46_P10
A	0.0009	0.0029	0.0059	0.0077
B	0.0009	0.0027	0.0053	0.0072
C	0.0010	0.0030	0.0062	0.0082

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0107	0.0110	3.2065	1.0485
A to Z ↑	0.0154	0.0161	5.5009	1.8685
B to Z ↓	0.0082	0.0084	3.1467	1.0550
B to Z ↑	0.0151	0.0149	5.5286	1.8798
C to Z ↓	0.0095	0.0095	2.8963	0.9560
C to Z ↑	0.0152	0.0150	2.9691	0.9856
	X34_P10	**X46_P10**	**X34_P10**	**X46_P10**
A to Z ↓	0.0117	0.0117	0.5338	0.4075

A to Z ↑	0.0170	0.0167	0.9323	0.7159
B to Z ↓	0.0089	0.0090	0.5416	0.4150
B to Z ↑	0.0154	0.0155	0.9380	0.7202
C to Z ↓	0.0100	0.0099	0.4893	0.3740
C to Z ↑	0.0154	0.0153	0.4927	0.3761

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P10	5.975e-06	1.145e-09
X17_P10	1.658e-05	2.139e-09
X34_P10	3.301e-05	3.795e-09
X46_P10	4.328e-05	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	1.051e-04	3.748e-04	7.898e-04	9.186e-04
B (output stable)	1.018e-04	3.395e-04	7.349e-04	8.365e-04
C (output stable)	7.292e-05	2.440e-04	5.081e-04	6.242e-04
A to Z	1.718e-03	5.396e-03	1.148e-02	1.478e-02
B to Z	1.300e-03	3.825e-03	8.090e-03	1.055e-02
C to Z	2.073e-03	6.305e-03	1.318e-02	1.699e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

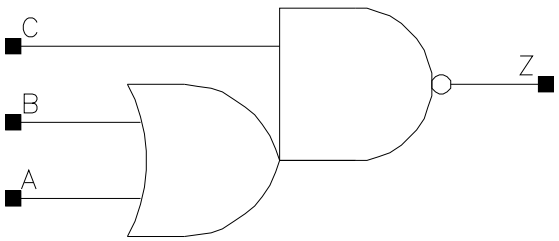
Pin Cycle (vdds)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	-1.386e-07	-2.111e-06	-6.238e-06	-5.241e-06
B (output stable)	7.653e-06	2.805e-05	7.541e-05	8.598e-05
C (output stable)	4.800e-08	-1.197e-07	-2.911e-07	-4.643e-07
A to Z	3.990e-07	1.344e-06	2.527e-06	1.480e-06
B to Z	5.755e-07	1.524e-06	1.413e-06	1.741e-06
C to Z	7.646e-07	2.699e-06	6.572e-06	7.058e-06

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.544	0.6528
X11_P10	1.200	0.952	1.1424
X17_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X17_P10	X23_P10
A	0.0010	0.0019	0.0030	0.0041
B	0.0009	0.0020	0.0028	0.0038
C	0.0010	0.0020	0.0029	0.0040
	X46_P10			
A	0.0082			
B	0.0076			
C	0.0079			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0107	0.0109	3.2330	1.5092
A to Z ↑	0.0194	0.0196	5.7777	2.7358
B to Z ↓	0.0086	0.0087	3.1815	1.4702

B to Z ↑	0.0195	0.0197	5.8050	2.7479
C to Z ↓	0.0084	0.0084	3.0450	1.4138
C to Z ↑	0.0114	0.0113	3.1748	1.4953
	X17_P10	**X23_P10**	**X17_P10**	**X23_P10**
A to Z ↓	0.0103	0.0111	1.0468	0.7753
A to Z ↑	0.0185	0.0206	1.8138	1.3828
B to Z ↓	0.0081	0.0086	1.0450	0.7759
B to Z ↑	0.0183	0.0193	1.8218	1.3897
C to Z ↓	0.0081	0.0084	0.9918	0.7333
C to Z ↑	0.0106	0.0110	0.9942	0.7558
	X46_P10		**X46_P10**	
A to Z ↓	0.0110		0.4040	
A to Z ↑	0.0201		0.6991	
B to Z ↓	0.0085		0.4003	
B to Z ↑	0.0189		0.7026	
C to Z ↓	0.0085		0.3807	
C to Z ↑	0.0108		0.3817	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P10	6.144e-06	1.145e-09
X11_P10	1.215e-05	1.642e-09
X17_P10	1.767e-05	2.139e-09
X23_P10	2.417e-05	2.801e-09
X46_P10	4.598e-05	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	3.462e-05	7.553e-05	1.092e-04	2.054e-04
B (output stable)	2.264e-05	5.345e-05	7.450e-05	1.451e-04
C (output stable)	2.472e-04	6.266e-04	7.023e-04	1.158e-03
A to Z	2.143e-03	4.617e-03	6.361e-03	9.628e-03
B to Z	1.695e-03	3.697e-03	4.928e-03	7.097e-03
C to Z	1.358e-03	2.947e-03	4.066e-03	5.846e-03
	X46_P10			
A (output stable)	3.908e-04			
B (output stable)	2.738e-04			
C (output stable)	2.152e-03			
A to Z	1.857e-02			
B to Z	1.362e-02			
C to Z	1.129e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	-9.974e-08	-3.049e-07	-5.049e-07	-2.707e-06
B (output stable)	7.350e-06	1.623e-05	2.420e-05	5.530e-05
C (output stable)	2.360e-08	-9.305e-07	-1.674e-07	-1.982e-06
A to Z	4.000e-08	4.190e-07	3.170e-07	-8.210e-07
B to Z	-1.342e-07	1.794e-06	1.920e-07	-1.202e-06
C to Z	1.263e-06	3.254e-06	2.880e-06	8.548e-06

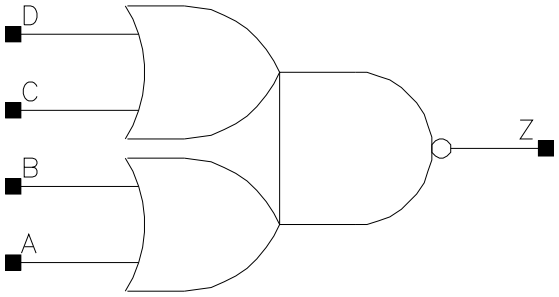
	X46_P10			
A (output stable)	-4.715e-06			
B (output stable)	9.598e-05			
C (output stable)	-3.666e-06			
A to Z	4.400e-07			
B to Z	-2.970e-06			
C to Z	8.952e-06			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0010	0.0020	0.0029	0.0041
B	0.0010	0.0018	0.0027	0.0038
C	0.0009	0.0019	0.0028	0.0040
D	0.0009	0.0018	0.0026	0.0037
	X42_P10			
A	0.0081			
B	0.0075			
C	0.0078			
D	0.0074			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0120	0.0130	2.9565	1.4722
A to Z ↑	0.0226	0.0230	6.0779	2.7972
B to Z ↓	0.0103	0.0107	2.8953	1.4775
B to Z ↑	0.0227	0.0215	6.0926	2.8105
C to Z ↓	0.0111	0.0121	3.0417	1.5024
C to Z ↑	0.0163	0.0176	5.9477	2.8065
D to Z ↓	0.0088	0.0092	2.9659	1.5134
D to Z ↑	0.0160	0.0152	5.9783	2.8270
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0124	0.0127	1.0073	0.7256
A to Z ↑	0.0216	0.0225	1.8821	1.3883
B to Z ↓	0.0104	0.0103	1.0115	0.7254
B to Z ↑	0.0209	0.0213	1.8918	1.3945
C to Z ↓	0.0117	0.0118	1.0302	0.7411
C to Z ↑	0.0162	0.0167	1.8897	1.3914
D to Z ↓	0.0091	0.0091	1.0411	0.7446
D to Z ↑	0.0147	0.0150	1.9040	1.4007
	X42_P10		**X42_P10**	
A to Z ↓	0.0129		0.3806	
A to Z ↑	0.0224		0.7069	
B to Z ↓	0.0105		0.3767	
B to Z ↑	0.0214		0.7102	
C to Z ↓	0.0123		0.3897	
C to Z ↑	0.0168		0.7039	
D to Z ↓	0.0094		0.3867	
D to Z ↑	0.0150		0.7089	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P10	7.248e-06	1.310e-09
X10_P10	1.452e-05	2.139e-09
X15_P10	2.020e-05	2.635e-09
X21_P10	2.787e-05	3.464e-09
X42_P10	5.397e-05	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	4.873e-05	1.548e-04	2.015e-04	2.922e-04
B (output stable)	3.036e-05	1.235e-04	1.445e-04	2.060e-04
C (output stable)	1.061e-04	2.871e-04	3.740e-04	5.375e-04
D (output stable)	9.179e-05	2.599e-04	3.201e-04	4.548e-04
A to Z	2.598e-03	5.892e-03	8.112e-03	1.149e-02
B to Z	2.167e-03	4.572e-03	6.349e-03	8.984e-03
C to Z	1.847e-03	4.333e-03	5.886e-03	8.307e-03
D to Z	1.454e-03	3.081e-03	4.257e-03	5.983e-03
	X42_P10			
A (output stable)	5.718e-04			
B (output stable)	4.151e-04			
C (output stable)	1.069e-03			
D (output stable)	9.123e-04			

A to Z	2.265e-02			
B to Z	1.763e-02			
C to Z	1.643e-02			
D to Z	1.181e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

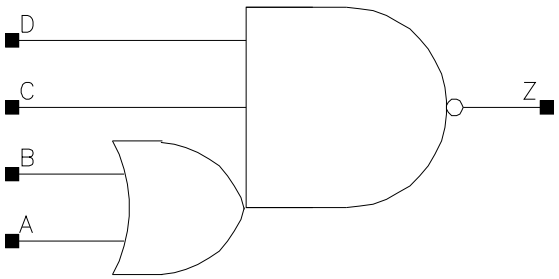
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	-1.798e-07	-2.571e-06	-1.883e-06	-3.742e-06
B (output stable)	1.373e-05	6.763e-05	5.360e-05	1.031e-04
C (output stable)	-3.937e-07	-3.118e-06	-2.345e-06	-4.825e-06
D (output stable)	1.332e-05	6.611e-05	5.077e-05	1.025e-04
A to Z	1.967e-07	3.865e-06	1.707e-06	5.081e-06
B to Z	1.287e-07	1.200e-06	1.720e-06	2.757e-06
C to Z	4.527e-07	4.490e-06	3.160e-06	6.672e-06
D to Z	5.277e-07	1.751e-06	2.963e-06	3.445e-06
	X42_P10			
A (output stable)	-6.370e-06			
B (output stable)	1.815e-04			
C (output stable)	-8.854e-06			
D (output stable)	1.785e-04			
A to Z	6.540e-06			
B to Z	5.112e-06			
C to Z	9.700e-06			
D to Z	6.223e-06			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X21_P10	1.200	2.448	2.9376
X31_P10	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X21_P10	X31_P10
A	0.0010	0.0018	0.0038	0.0056
B	0.0012	0.0017	0.0034	0.0051
C	0.0010	0.0020	0.0040	0.0061
D	0.0010	0.0019	0.0038	0.0057

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0158	0.0152	4.0249	2.1540
A to Z ↑	0.0204	0.0189	5.5108	2.7746
B to Z ↓	0.0135	0.0118	4.0816	2.1665
B to Z ↑	0.0201	0.0172	5.5516	2.7920
C to Z ↓	0.0137	0.0141	3.7894	2.0234

C to Z ↑	0.0185	0.0180	2.8977	1.4593
D to Z ↓	0.0147	0.0139	3.8118	2.0350
D to Z ↑	0.0174	0.0163	2.9328	1.4631
	X21_P10	**X31_P10**	**X21_P10**	**X31_P10**
A to Z ↓	0.0153	0.0155	1.1231	0.7625
A to Z ↑	0.0182	0.0182	1.3868	0.9311
B to Z ↓	0.0118	0.0118	1.1305	0.7703
B to Z ↑	0.0167	0.0165	1.3957	0.9372
C to Z ↓	0.0138	0.0139	1.0564	0.7184
C to Z ↑	0.0176	0.0176	0.7387	0.4981
D to Z ↓	0.0139	0.0141	1.0621	0.7222
D to Z ↑	0.0159	0.0159	0.7401	0.4980

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P10	5.905e-06	1.476e-09
X10_P10	1.110e-05	2.139e-09
X21_P10	2.086e-05	3.464e-09
X31_P10	3.064e-05	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	2.058e-04	4.361e-04	8.137e-04	1.206e-03
B (output stable)	1.969e-04	4.273e-04	7.924e-04	1.176e-03
C (output stable)	4.553e-05	1.293e-04	2.454e-04	3.651e-04
D (output stable)	9.427e-05	3.516e-04	6.508e-04	9.381e-04
A to Z	2.516e-03	4.440e-03	8.473e-03	1.256e-02
B to Z	1.908e-03	3.199e-03	6.045e-03	8.944e-03
C to Z	3.061e-03	5.861e-03	1.115e-02	1.655e-02
D to Z	2.731e-03	4.928e-03	9.372e-03	1.391e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

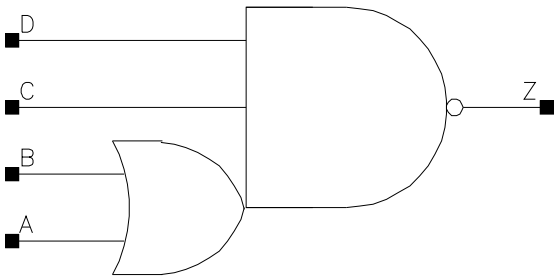
Pin Cycle (vdds)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	-1.667e-06	-2.420e-06	-4.876e-06	-6.596e-06
B (output stable)	8.042e-06	1.350e-05	2.074e-05	2.868e-05
C (output stable)	4.082e-08	-1.196e-08	-1.371e-07	-2.333e-07
D (output stable)	-1.124e-07	-3.834e-07	-1.005e-06	-1.543e-06
A to Z	5.130e-07	7.990e-07	1.743e-06	1.540e-06
B to Z	2.790e-07	-1.990e-07	-2.044e-06	-3.045e-06
C to Z	2.772e-06	2.704e-06	5.044e-06	5.773e-06
D to Z	2.525e-06	2.192e-06	3.817e-06	5.225e-06

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0010	0.0021	0.0031	0.0041
B	0.0010	0.0019	0.0028	0.0038
C	0.0010	0.0019	0.0030	0.0039
D	0.0010	0.0019	0.0028	0.0038

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0143	0.0155	4.0966	2.1391
A to Z ↑	0.0228	0.0248	5.3578	2.7299
B to Z ↓	0.0121	0.0128	4.0274	2.1426
B to Z ↑	0.0231	0.0238	5.3782	2.7397
C to Z ↓	0.0113	0.0128	3.8783	2.0427

C to Z ↑	0.0144	0.0153	2.9465	1.4897
D to Z ↓	0.0116	0.0122	3.9105	2.0578
D to Z ↑	0.0125	0.0126	2.9686	1.5019
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0152	0.0154	1.4714	1.1102
A to Z ↑	0.0238	0.0243	1.8389	1.3936
B to Z ↓	0.0128	0.0126	1.4665	1.1093
B to Z ↑	0.0233	0.0237	1.8472	1.3990
C to Z ↓	0.0125	0.0127	1.4006	1.0575
C to Z ↑	0.0146	0.0149	0.9931	0.7472
D to Z ↓	0.0121	0.0124	1.4115	1.0649
D to Z ↑	0.0122	0.0124	1.0009	0.7531

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P10	6.136e-06	1.476e-09
X10_P10	1.210e-05	2.139e-09
X15_P10	1.679e-05	2.635e-09
X21_P10	2.313e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	2.911e-05	6.971e-05	9.866e-05	1.316e-04
B (output stable)	2.266e-05	5.934e-05	8.210e-05	1.092e-04
C (output stable)	9.290e-05	2.107e-04	3.263e-04	4.164e-04
D (output stable)	1.690e-04	5.989e-04	7.149e-04	1.067e-03
A to Z	2.935e-03	6.388e-03	9.060e-03	1.238e-02
B to Z	2.426e-03	5.046e-03	7.181e-03	9.790e-03
C to Z	1.980e-03	4.373e-03	6.117e-03	8.412e-03
D to Z	1.671e-03	3.481e-03	4.964e-03	6.724e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

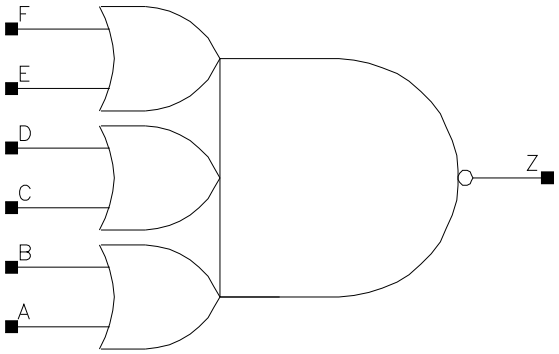
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	-1.313e-08	-1.166e-06	-8.348e-07	-1.722e-06
B (output stable)	3.483e-06	1.541e-05	1.230e-05	2.445e-05
C (output stable)	3.350e-08	-1.845e-07	-5.721e-07	-5.118e-07
D (output stable)	4.104e-08	-1.434e-06	-1.561e-06	-2.567e-06
A to Z	3.470e-07	7.270e-07	1.290e-06	2.118e-06
B to Z	1.650e-07	-1.960e-07	9.200e-08	-9.300e-08
C to Z	6.697e-07	3.990e-06	3.510e-06	7.315e-06
D to Z	4.640e-07	4.468e-06	2.527e-06	7.029e-06

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	1.088	1.3056
X9_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X9_P10
A	0.0008	0.0021
B	0.0008	0.0019
C	0.0008	0.0020
D	0.0008	0.0018
E	0.0008	0.0019
F	0.0008	0.0018

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X9_P10	X3_P10	X9_P10
A to Z ↓	0.0187	0.0199	4.6857	1.9422
A to Z ↑	0.0308	0.0295	7.4618	2.7480
B to Z ↓	0.0172	0.0173	4.7243	1.9460
B to Z ↑	0.0320	0.0287	7.4830	2.7571
C to Z ↓	0.0182	0.0190	4.7261	1.9538
C to Z ↑	0.0263	0.0253	7.4860	2.7440
D to Z ↓	0.0163	0.0162	4.7689	1.9606
D to Z ↑	0.0273	0.0242	7.5141	2.7564
E to Z ↓	0.0158	0.0170	4.7894	1.9684
E to Z ↑	0.0200	0.0196	7.5176	2.7498
F to Z ↓	0.0140	0.0139	4.8364	1.9752
F to Z ↑	0.0205	0.0178	7.5647	2.7680

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P10	7.387e-06	1.807e-09
X9_P10	1.815e-05	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P10	X9_P10
A (output stable)	3.981e-05	1.414e-04
B (output stable)	3.018e-05	1.191e-04
C (output stable)	8.262e-05	2.436e-04
D (output stable)	7.143e-05	2.268e-04
E (output stable)	2.265e-04	5.578e-04
F (output stable)	2.187e-04	5.300e-04
A to Z	3.413e-03	8.858e-03
B to Z	3.064e-03	7.473e-03
C to Z	2.761e-03	7.170e-03
D to Z	2.428e-03	5.927e-03
E to Z	2.015e-03	5.491e-03
F to Z	1.714e-03	4.262e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

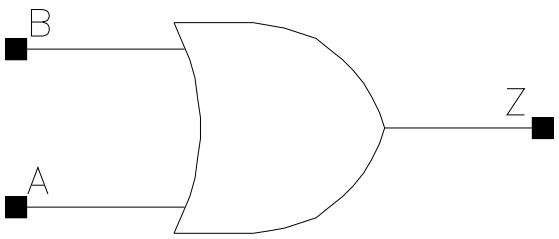
Pin Cycle (vdds)	X3_P10	X9_P10
A (output stable)	-7.663e-08	-1.905e-06
B (output stable)	7.005e-06	4.431e-05
C (output stable)	-1.811e-07	-2.011e-06
D (output stable)	7.200e-06	4.178e-05
E (output stable)	-7.418e-07	-3.388e-06
F (output stable)	6.451e-06	4.181e-05
A to Z	2.588e-07	7.919e-06
B to Z	1.444e-09	4.792e-06
C to Z	3.059e-07	7.886e-06
D to Z	-1.134e-07	2.965e-06
E to Z	8.036e-07	7.881e-06
F to Z	4.969e-07	5.283e-06

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X33_P10	1.200	1.360	1.6320
X50_P10	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P10	X16_P10	X33_P10	X50_P10
A	0.0009	0.0011	0.0022	0.0022
B	0.0008	0.0011	0.0022	0.0023

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0338	0.0305	1.8193	0.9155
A to Z ↑	0.0203	0.0214	2.9009	1.4600
B to Z ↓	0.0343	0.0310	1.8178	0.9158
B to Z ↑	0.0190	0.0197	2.9022	1.4618
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0319	0.0378	0.4533	0.3117
A to Z ↑	0.0214	0.0214	0.7140	0.4822
B to Z ↓	0.0310	0.0375	0.4534	0.3118
B to Z ↑	0.0193	0.0198	0.7134	0.4814

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	8.371e-06	1.145e-09
X16_P10	1.442e-05	1.310e-09
X33_P10	2.862e-05	2.139e-09
X50_P10	3.856e-05	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	3.377e-05	6.105e-05	1.981e-04	1.849e-04
B (output stable)	1.591e-05	2.885e-05	1.644e-04	1.483e-04
A to Z	3.449e-03	5.717e-03	1.209e-02	1.689e-02
B to Z	3.219e-03	5.302e-03	1.084e-02	1.572e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

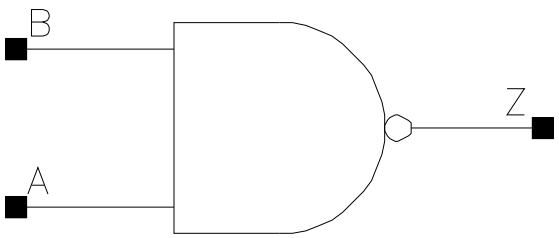
Pin Cycle (vdds)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	-2.906e-07	-3.499e-07	-3.852e-06	-3.452e-06
B (output stable)	1.404e-05	2.411e-05	1.086e-04	1.059e-04
A to Z	2.338e-07	1.134e-07	5.460e-07	4.835e-07
B to Z	5.980e-08	1.438e-07	-3.600e-08	9.500e-08

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X16_P10	1.200	0.952	1.1424
X24_P10	1.200	1.088	1.3056
X32_P10	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P10	X16_P10	X24_P10	X32_P10
A	0.0011	0.0011	0.0012	0.0011
B	0.0012	0.0013	0.0013	0.0013

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0267	0.0282	1.7569	0.9114
A to Z ↑	0.0314	0.0325	2.9325	1.4947
B to Z ↓	0.0281	0.0296	1.7563	0.9123
B to Z ↑	0.0297	0.0303	2.9306	1.4943
	X24_P10	**X32_P10**	**X24_P10**	**X32_P10**
A to Z ↓	0.0317	0.0323	0.6174	0.4631
A to Z ↑	0.0350	0.0359	0.9982	0.7460
B to Z ↓	0.0331	0.0340	0.6181	0.4627
B to Z ↑	0.0328	0.0342	0.9970	0.7458

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	1.409e-05	1.476e-09
X16_P10	1.897e-05	1.642e-09
X24_P10	2.349e-05	1.807e-09
X32_P10	2.865e-05	1.973e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	3.001e-05	3.013e-05	3.025e-05	3.252e-05
B (output stable)	4.589e-05	4.618e-05	4.630e-05	4.498e-05
A to Z	6.440e-03	7.652e-03	9.856e-03	1.297e-02
B to Z	6.146e-03	7.369e-03	9.585e-03	1.268e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

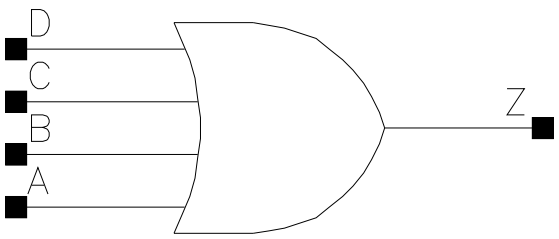
Pin Cycle (vdds)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	2.620e-08	2.915e-08	2.929e-08	3.389e-08
B (output stable)	5.070e-08	4.870e-08	5.040e-08	3.730e-08
A to Z	6.805e-07	3.416e-07	6.600e-08	-3.240e-07
B to Z	6.200e-08	-1.095e-07	-2.920e-07	-2.600e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P10	1.200	2.176	2.6112
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P10	X27_P10
A	0.0019	0.0023
B	0.0018	0.0023
C	0.0019	0.0023
D	0.0018	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P10	X27_P10	X20_P10	X27_P10
A to Z ↓	0.0343	0.0362	1.0265	0.7678
A to Z ↑	0.0221	0.0214	0.9573	0.7143
B to Z ↓	0.0339	0.0353	1.0267	0.7680
B to Z ↑	0.0206	0.0196	0.9569	0.7128
C to Z ↓	0.0337	0.0357	1.0257	0.7676
C to Z ↑	0.0210	0.0209	0.9584	0.7165
D to Z ↓	0.0334	0.0351	1.0261	0.7678
D to Z ↑	0.0195	0.0192	0.9578	0.7153

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X20_P10	2.388e-05	3.132e-09
X27_P10	3.340e-05	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X20_P10	X27_P10
A (output stable)	2.576e-03	3.563e-03
B (output stable)	2.165e-03	2.999e-03
C (output stable)	2.307e-03	3.291e-03
D (output stable)	1.886e-03	2.754e-03
A to Z	1.066e-02	1.496e-02
B to Z	9.765e-03	1.368e-02
C to Z	9.482e-03	1.320e-02
D to Z	8.615e-03	1.203e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

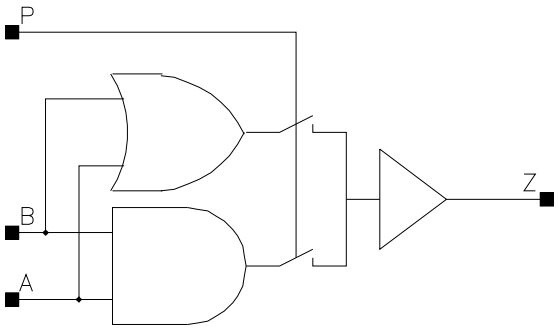
Pin Cycle (vdds)	X20_P10	X27_P10
A (output stable)	-8.050e-07	-1.888e-06
B (output stable)	2.907e-05	6.387e-05
C (output stable)	-7.850e-07	-2.620e-06
D (output stable)	2.920e-05	6.575e-05
A to Z	6.242e-07	1.134e-06
B to Z	8.990e-07	-4.700e-08
C to Z	7.311e-07	4.562e-07
D to Z	9.170e-07	1.600e-06

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X16_P10	1.200	1.224	1.4688
X25_P10	1.200	2.040	2.4480
X33_P10	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0014	0.0021	0.0037	0.0038
B	0.0014	0.0021	0.0042	0.0042
P	0.0008	0.0011	0.0022	0.0022

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0412	0.0381	1.8554	0.9078
A to Z ↑	0.0265	0.0252	2.9434	1.4726
B to Z ↓	0.0413	0.0384	1.8672	0.9146
B to Z ↑	0.0277	0.0264	2.9470	1.4754
P to Z ↓	0.0381	0.0359	1.8670	0.9138
P to Z ↑	0.0271	0.0260	2.9444	1.4721
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**

A to Z ↓	0.0363	0.0389	0.6159	0.4664
A to Z ↑	0.0248	0.0263	0.9899	0.7410
B to Z ↓	0.0363	0.0387	0.6195	0.4687
B to Z ↑	0.0263	0.0276	0.9906	0.7424
P to Z ↓	0.0344	0.0370	0.6198	0.4687
P to Z ↑	0.0253	0.0268	0.9886	0.7402

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	8.598e-06	1.642e-09
X16_P10	1.665e-05	1.973e-09
X25_P10	2.762e-05	2.967e-09
X33_P10	3.127e-05	3.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	6.625e-05	1.062e-04	2.348e-04	2.366e-04
B (output stable)	6.375e-05	1.112e-04	2.882e-04	2.919e-04
P (output stable)	1.466e-04	2.498e-04	4.194e-04	4.319e-04
A to Z	4.028e-03	7.075e-03	1.189e-02	1.412e-02
B to Z	3.907e-03	6.905e-03	1.139e-02	1.364e-02
P to Z	3.600e-03	6.471e-03	1.081e-02	1.303e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

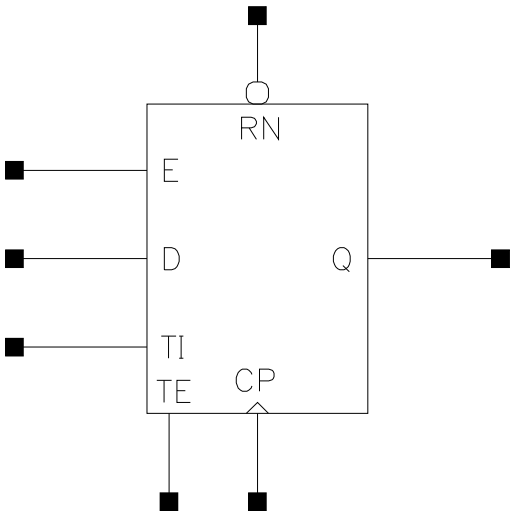
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	-1.113e-06	-1.207e-06	-1.799e-06	-1.803e-06
B (output stable)	5.783e-06	1.051e-05	2.643e-05	2.701e-05
P (output stable)	2.443e-05	4.247e-05	5.254e-05	5.402e-05
A to Z	-2.534e-07	-1.362e-07	-1.150e-06	-1.237e-06
B to Z	-1.244e-07	-3.204e-07	-1.094e-06	-1.104e-06
P to Z	-6.001e-08	-5.240e-08	-3.433e-07	1.113e-07

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.488	5.3856
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0010	0.0010	0.0010
D	0.0009	0.0008	0.0008	0.0008
E	0.0011	0.0012	0.0012	0.0012
RN	0.0010	0.0008	0.0009	0.0010
TE	0.0011	0.0011	0.0011	0.0011

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to Q ↓	0.0731	0.0397	3.9220	1.8094
CP to Q ↑	0.0604	0.0514	5.7641	2.9160
RN to Q ↓	0.0519	0.0613	3.4591	1.7548
	X17_P10	X33_P10	X17_P10	X33_P10
CP to Q ↓	0.0688	0.0730	0.8759	0.4588
CP to Q ↑	0.0838	0.0881	1.4304	0.7277
RN to Q ↓	0.0835	0.0885	0.8760	0.4595

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0973	0.0659	0.0659	0.0659
CP ↑	min_pulse_width to CP	0.0675	0.0338	0.0271	0.0290
D ↓	hold_rising to CP	-0.1089	-0.0557	-0.0557	-0.0557
D ↑	hold_rising to CP	-0.0627	-0.0189	-0.0189	-0.0189
D ↓	setup_rising to CP	0.1485	0.0951	0.0951	0.0951
D ↑	setup_rising to CP	0.0923	0.0490	0.0490	0.0490
E ↓	hold_rising to CP	-0.0698	-0.0691	-0.0722	-0.0722
E ↑	hold_rising to CP	-0.0554	-0.0194	-0.0194	-0.0194
E ↓	setup_rising to CP	0.1265	0.1292	0.1292	0.1292
E ↑	setup_rising to CP	0.1369	0.0979	0.0979	0.0979
RN ↓	min_pulse_width to RN	0.0686	0.0757	0.0637	0.0637
RN ↑	recovery_rising to CP	0.0171	0.0149	0.0149	0.0149
RN ↑	removal_rising to CP	-0.0098	-0.0052	-0.0052	-0.0052
TE ↓	hold_rising to CP	-0.0478	-0.0331	-0.0331	-0.0357
TE ↑	hold_rising to CP	-0.0379	-0.0233	-0.0233	-0.0233
TE ↓	setup_rising to CP	0.0875	0.0778	0.0778	0.0778
TE ↑	setup_rising to CP	0.1704	0.1198	0.1198	0.1223
TI ↓	hold_rising to CP	-0.1375	-0.0714	-0.0729	-0.0729
TI ↑	hold_rising to CP	-0.0472	-0.0251	-0.0251	-0.0251
TI ↓	setup_rising to CP	0.1771	0.1124	0.1124	0.1124
TI ↑	setup_rising to CP	0.0769	0.0548	0.0548	0.0548

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	3.182e-05	6.340e-09
X8_P10	3.397e-05	5.948e-09
X17_P10	4.063e-05	6.279e-09
X33_P10	4.804e-05	6.611e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

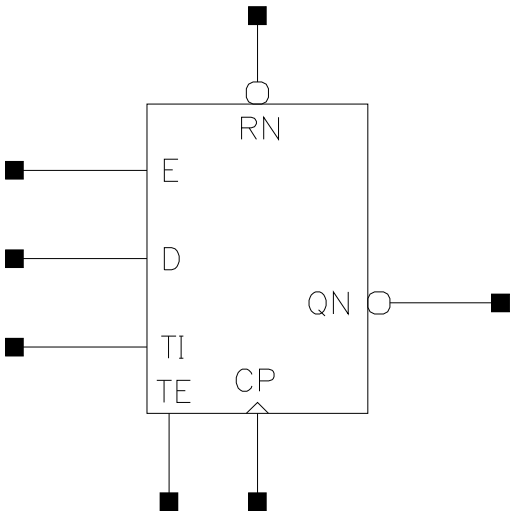
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.868e-03	5.913e-03	5.924e-03	5.930e-03
Clock 100Mhz Data 25Mhz	9.811e-03	9.928e-03	1.090e-02	1.215e-02
Clock 100Mhz Data 50Mhz	1.375e-02	1.394e-02	1.588e-02	1.838e-02
Clock = 0 Data 100Mhz	9.060e-03	8.686e-03	8.564e-03	8.503e-03
Clock = 1 Data 100Mhz	3.218e-03	3.294e-03	3.321e-03	3.335e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.624	5.5488
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0010	0.0010	0.0010
D	0.0009	0.0008	0.0008	0.0008
E	0.0011	0.0012	0.0012	0.0012
RN	0.0010	0.0009	0.0010	0.0010
TE	0.0011	0.0011	0.0011	0.0011

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to QN ↓	0.0741	0.0692	3.2548	1.7460
CP to QN ↑	0.0816	0.0529	5.6517	2.8370
RN to QN ↑	0.0649	0.0686	5.6349	2.8435
	X17_P10	X33_P10	X17_P10	X33_P10
CP to QN ↓	0.0670	0.0713	0.8761	0.4583
CP to QN ↑	0.0557	0.0609	1.4310	0.7286
RN to QN ↑	0.0756	0.0794	1.4260	0.7286

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0973	0.0659	0.0659	0.0659
CP ↑	min_pulse_width to CP	0.0483	0.0253	0.0301	0.0344
D ↓	hold_rising to CP	-0.1089	-0.0557	-0.0557	-0.0557
D ↑	hold_rising to CP	-0.0627	-0.0189	-0.0189	-0.0189
D ↓	setup_rising to CP	0.1482	0.0951	0.0951	0.0951
D ↑	setup_rising to CP	0.0926	0.0490	0.0490	0.0490
E ↓	hold_rising to CP	-0.0698	-0.0722	-0.0691	-0.0691
E ↑	hold_rising to CP	-0.0554	-0.0194	-0.0194	-0.0194
E ↓	setup_rising to CP	0.1262	0.1292	0.1292	0.1292
E ↑	setup_rising to CP	0.1369	0.0979	0.0979	0.0979
RN ↓	min_pulse_width to RN	0.0659	0.0637	0.0757	0.0828
RN ↑	recovery_rising to CP	0.0171	0.0174	0.0149	0.0149
RN ↑	removal_rising to CP	-0.0098	-0.0080	-0.0052	-0.0052
TE ↓	hold_rising to CP	-0.0478	-0.0331	-0.0331	-0.0331
TE ↑	hold_rising to CP	-0.0383	-0.0233	-0.0233	-0.0237
TE ↓	setup_rising to CP	0.0875	0.0778	0.0778	0.0778
TE ↑	setup_rising to CP	0.1704	0.1198	0.1223	0.1223
TI ↓	hold_rising to CP	-0.1375	-0.0714	-0.0714	-0.0714
TI ↑	hold_rising to CP	-0.0472	-0.0251	-0.0251	-0.0251
TI ↓	setup_rising to CP	0.1771	0.1124	0.1124	0.1124
TI ↑	setup_rising to CP	0.0769	0.0548	0.0548	0.0548

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	3.306e-05	6.340e-09
X8_P10	3.581e-05	6.114e-09
X17_P10	4.280e-05	6.279e-09
X33_P10	5.195e-05	6.611e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

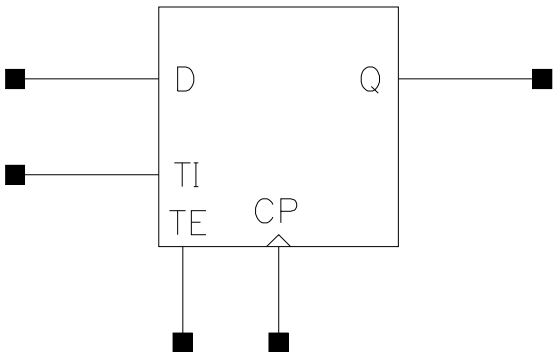
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.866e-03	5.910e-03	5.919e-03	5.923e-03
Clock 100Mhz Data 25Mhz	9.687e-03	9.969e-03	1.085e-02	1.210e-02
Clock 100Mhz Data 50Mhz	1.351e-02	1.403e-02	1.577e-02	1.828e-02
Clock = 0 Data 100Mhz	9.061e-03	8.690e-03	8.568e-03	8.507e-03
Clock = 1 Data 100Mhz	3.215e-03	3.296e-03	3.325e-03	3.339e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.400	4.0800
X8_P10	1.200	3.128	3.7536
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0600	0.0369	3.6959	1.8063
CP to Q ↑	0.0543	0.0470	5.7916	2.8767
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0569	0.0630	0.8604	0.4513
CP to Q ↑	0.0814	0.0868	1.4281	0.7268

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0895	0.0963	0.0963	0.0963
CP ↑	min_pulse_width to CP	0.0483	0.0290	0.0253	0.0253
D ↓	hold_rising to CP	-0.0698	-0.0264	-0.0264	-0.0264
D ↑	hold_rising to CP	-0.0212	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0991	0.0658	0.0658	0.0658
D ↑	setup_rising to CP	0.0481	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0405	-0.0237	-0.0237	-0.0237
TE ↑	hold_rising to CP	-0.0279	-0.0137	-0.0137	-0.0137
TE ↓	setup_rising to CP	0.0827	0.0660	0.0660	0.0660
TE ↑	setup_rising to CP	0.1539	0.1272	0.1272	0.1272
TI ↓	hold_rising to CP	-0.1326	-0.0825	-0.0840	-0.0840
TI ↑	hold_rising to CP	-0.0374	-0.0159	-0.0159	-0.0159
TI ↓	setup_rising to CP	0.1633	0.1270	0.1270	0.1270
TI ↑	setup_rising to CP	0.0617	0.0448	0.0448	0.0448

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	2.524e-05	4.623e-09
X8_P10	2.769e-05	4.292e-09
X17_P10	3.699e-05	4.789e-09
X33_P10	4.422e-05	5.120e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

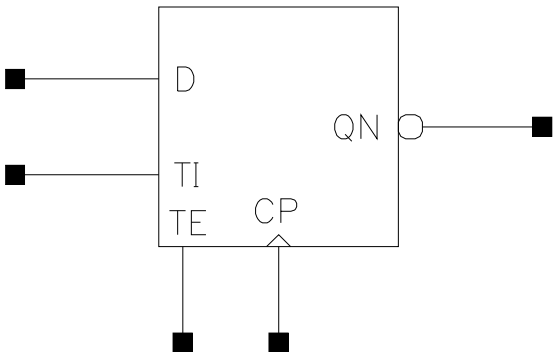
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.334e-03	5.404e-03	5.423e-03	5.433e-03
Clock 100Mhz Data 25Mhz	8.125e-03	8.228e-03	9.199e-03	1.029e-02
Clock 100Mhz Data 50Mhz	1.092e-02	1.105e-02	1.298e-02	1.514e-02
Clock = 0 Data 100Mhz	7.155e-03	6.685e-03	6.528e-03	6.450e-03
Clock = 1 Data 100Mhz	1.819e-03	9.399e-04	6.470e-04	5.006e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.536	4.2432
X8_P10	1.200	3.264	3.9168
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0695	0.0733	3.7153	1.8041
CP to QN ↑	0.0653	0.0487	5.7555	2.8457
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0576	0.0643	0.8605	0.4521
CP to QN ↑	0.0488	0.0546	1.4283	0.7274

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0895	0.0963	0.0963	0.0963
CP ↑	min_pulse_width to CP	0.0386	0.0253	0.0290	0.0301
D ↓	hold_rising to CP	-0.0698	-0.0289	-0.0264	-0.0264
D ↑	hold_rising to CP	-0.0208	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0995	0.0658	0.0658	0.0658
D ↑	setup_rising to CP	0.0481	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0405	-0.0237	-0.0240	-0.0240
TE ↑	hold_rising to CP	-0.0309	-0.0137	-0.0137	-0.0137
TE ↓	setup_rising to CP	0.0827	0.0660	0.0660	0.0660
TE ↑	setup_rising to CP	0.1539	0.1272	0.1272	0.1272
TI ↓	hold_rising to CP	-0.1286	-0.0840	-0.0825	-0.0825
TI ↑	hold_rising to CP	-0.0374	-0.0159	-0.0159	-0.0159
TI ↓	setup_rising to CP	0.1640	0.1270	0.1270	0.1270
TI ↑	setup_rising to CP	0.0617	0.0448	0.0448	0.0448

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	2.551e-05	4.789e-09
X8_P10	2.792e-05	4.457e-09
X17_P10	3.679e-05	4.789e-09
X33_P10	4.401e-05	5.120e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

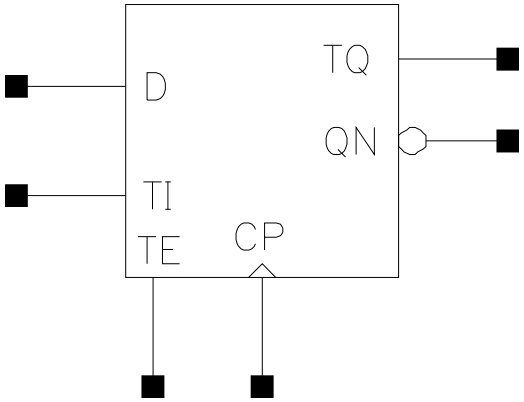
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.282e-03	5.380e-03	5.412e-03	5.428e-03
Clock 100Mhz Data 25Mhz	8.067e-03	8.360e-03	9.145e-03	1.027e-02
Clock 100Mhz Data 50Mhz	1.085e-02	1.134e-02	1.288e-02	1.512e-02
Clock = 0 Data 100Mhz	7.189e-03	6.705e-03	6.542e-03	6.460e-03
Clock = 1 Data 100Mhz	1.808e-03	9.402e-04	6.509e-04	5.063e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.536	4.2432
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0014	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0012	0.0012	0.0012

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0772	0.0667	3.3764	1.7576
CP to QN ↑	0.0799	0.0513	5.6724	2.8571
CP to TQ ↓	0.0546	0.0338	4.6347	3.2625
CP to TQ ↑	0.0557	0.0467	10.4564	7.5940
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0637	0.0694	0.8814	0.4627
CP to QN ↑	0.0532	0.0573	1.4457	0.7414
CP to TQ ↓	0.0352	0.0366	4.2540	4.2724
CP to TQ ↑	0.0475	0.0488	9.6976	10.2256

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0895	0.0963	0.0963	0.0963
CP ↑	min_pulse_width to CP	0.0483	0.0253	0.0290	0.0301
D ↓	hold_rising to CP	-0.0673	-0.0264	-0.0264	-0.0264
D ↑	hold_rising to CP	-0.0212	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0994	0.0658	0.0658	0.0658
D ↑	setup_rising to CP	0.0481	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0405	-0.0240	-0.0240	-0.0215
TE ↑	hold_rising to CP	-0.0279	-0.0137	-0.0137	-0.0137
TE ↓	setup_rising to CP	0.0796	0.0635	0.0635	0.0660
TE ↑	setup_rising to CP	0.1539	0.1272	0.1272	0.1272
TI ↓	hold_rising to CP	-0.1286	-0.0825	-0.0825	-0.0825
TI ↑	hold_rising to CP	-0.0374	-0.0159	-0.0159	-0.0159
TI ↓	setup_rising to CP	0.1625	0.1234	0.1234	0.1275
TI ↑	setup_rising to CP	0.0617	0.0448	0.0448	0.0448

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	2.801e-05	5.131e-09
X8_P10	3.110e-05	4.789e-09
X17_P10	3.559e-05	4.954e-09
X33_P10	4.427e-05	5.286e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10

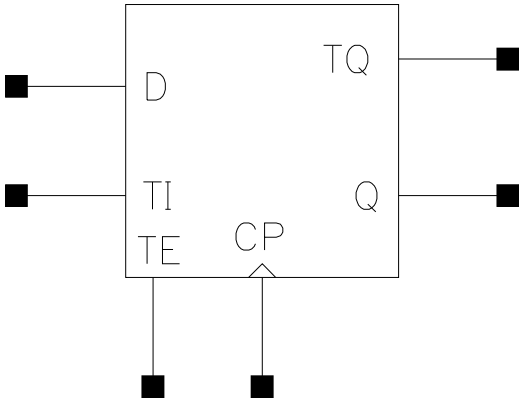
Clock 100Mhz Data 0Mhz	5.416e-03	5.444e-03	5.454e-03	5.459e-03
Clock 100Mhz Data 25Mhz	8.494e-03	8.741e-03	9.210e-03	1.046e-02
Clock 100Mhz Data 50Mhz	1.157e-02	1.204e-02	1.297e-02	1.546e-02
Clock = 0 Data 100Mhz	7.184e-03	6.709e-03	6.551e-03	6.473e-03
Clock = 1 Data 100Mhz	1.818e-03	9.397e-04	6.468e-04	5.004e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.400	4.0800
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008

TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0797	0.0414	3.9068	1.8058
CP to Q ↑	0.0625	0.0500	5.8669	2.8946
CP to TQ ↓	0.0757	0.0427	3.9154	4.3752
CP to TQ ↑	0.0640	0.0546	7.6462	10.3746
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0586	0.0647	0.8852	0.4606
CP to Q ↑	0.0832	0.0884	1.4561	0.7315
CP to TQ ↓	0.0609	0.0677	4.1616	4.2459
CP to TQ ↑	0.0880	0.0949	10.0279	10.1306

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0901	0.0963	0.0963	0.0963
CP ↑	min_pulse_width to CP	0.0675	0.0301	0.0253	0.0253
D ↓	hold_rising to CP	-0.0698	-0.0264	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0212	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0991	0.0658	0.0658	0.0658
D ↑	setup_rising to CP	0.0481	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0405	-0.0215	-0.0237	-0.0237
TE ↑	hold_rising to CP	-0.0279	-0.0137	-0.0137	-0.0137
TE ↓	setup_rising to CP	0.0827	0.0660	0.0660	0.0660
TE ↑	setup_rising to CP	0.1539	0.1272	0.1272	0.1272
TI ↓	hold_rising to CP	-0.1326	-0.0825	-0.0840	-0.0840
TI ↑	hold_rising to CP	-0.0374	-0.0159	-0.0159	-0.0159
TI ↓	setup_rising to CP	0.1640	0.1270	0.1270	0.1270
TI ↑	setup_rising to CP	0.0617	0.0448	0.0448	0.0448

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	2.798e-05	4.954e-09
X8_P10	2.962e-05	4.623e-09
X17_P10	3.854e-05	4.954e-09
X33_P10	4.569e-05	5.286e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

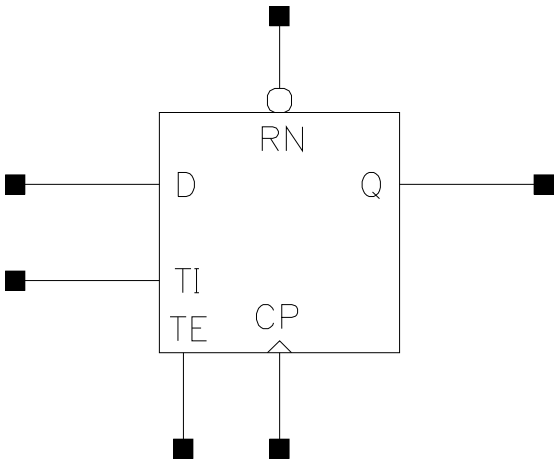
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.318e-03	5.393e-03	5.415e-03	5.427e-03
Clock 100Mhz Data 25Mhz	8.713e-03	8.559e-03	9.486e-03	1.062e-02
Clock 100Mhz Data 50Mhz	1.211e-02	1.173e-02	1.356e-02	1.582e-02
Clock = 0 Data 100Mhz	7.142e-03	6.677e-03	6.524e-03	6.449e-03
Clock = 1 Data 100Mhz	1.806e-03	9.333e-04	6.426e-04	4.973e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.672	4.4064
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
RN	0.0010	0.0008	0.0009	0.0009
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0724	0.0397	3.9709	1.8122
CP to Q ↑	0.0598	0.0506	5.7970	2.9127
RN to Q ↓	0.0515	0.0613	3.4786	1.7609
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0595	0.0659	0.8684	0.4580
CP to Q ↑	0.0746	0.0795	1.4262	0.7269
RN to Q ↓	0.0742	0.0806	0.8694	0.4582

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1010	0.0982	0.0992	0.0992
CP ↑	min_pulse_width to CP	0.0627	0.0301	0.0253	0.0253
D ↓	hold_rising to CP	-0.0594	-0.0188	-0.0188	-0.0188
D ↑	hold_rising to CP	-0.0286	-0.0047	-0.0044	-0.0044
D ↓	setup_rising to CP	0.0995	0.0635	0.0635	0.0635
D ↑	setup_rising to CP	0.0560	0.0344	0.0344	0.0344
RN ↓	min_pulse_width to RN	0.0659	0.0708	0.0637	0.0637
RN ↑	recovery_rising to CP	0.0197	0.0149	0.0149	0.0149
RN ↑	removal_rising to CP	-0.0123	-0.0080	-0.0080	-0.0080
TE ↓	hold_rising to CP	-0.0429	-0.0166	-0.0166	-0.0166
TE ↑	hold_rising to CP	-0.0383	-0.0242	-0.0242	-0.0242
TE ↓	setup_rising to CP	0.0796	0.0609	0.0609	0.0609
TE ↑	setup_rising to CP	0.1512	0.1223	0.1223	0.1223
TI ↓	hold_rising to CP	-0.1229	-0.0678	-0.0678	-0.0678
TI ↑	hold_rising to CP	-0.0421	-0.0249	-0.0264	-0.0264
TI ↓	setup_rising to CP	0.1625	0.1186	0.1186	0.1186
TI ↑	setup_rising to CP	0.0720	0.0561	0.0561	0.0561

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	2.803e-05	5.286e-09
X8_P10	2.995e-05	4.954e-09
X17_P10	3.845e-05	5.451e-09
X33_P10	4.439e-05	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.869e-03	5.924e-03	5.967e-03	5.989e-03

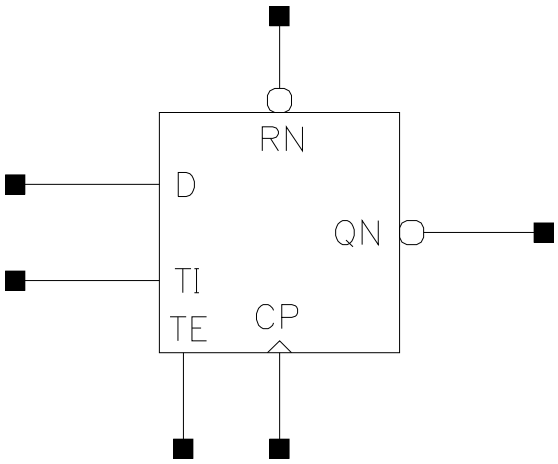
Clock 100Mhz Data 25Mhz	9.072e-03	8.972e-03	1.005e-02	1.117e-02
Clock 100Mhz Data 50Mhz	1.227e-02	1.202e-02	1.413e-02	1.636e-02
Clock = 0 Data 100Mhz	7.228e-03	6.656e-03	6.467e-03	6.372e-03
Clock = 1 Data 100Mhz	1.849e-03	9.659e-04	6.717e-04	5.247e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	3.944	4.7328
X33_P10	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
RN	0.0010	0.0009	0.0010	0.0010
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0671	0.0623	3.1937	1.7040
CP to QN ↑	0.0745	0.0479	5.6505	2.8247
RN to QN ↑	0.0587	0.0631	5.6389	2.8285
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0624	0.0690	0.8688	0.4573
CP to QN ↑	0.0535	0.0595	1.4375	0.7355
RN to QN ↑	0.0741	0.0793	1.4352	0.7340

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1010	0.0981	0.0993	0.0993
CP ↑	min_pulse_width to CP	0.0434	0.0253	0.0301	0.0338
D ↓	hold_rising to CP	-0.0624	-0.0188	-0.0188	-0.0188
D ↑	hold_rising to CP	-0.0286	-0.0047	-0.0047	-0.0047
D ↓	setup_rising to CP	0.0995	0.0635	0.0635	0.0635
D ↑	setup_rising to CP	0.0560	0.0344	0.0344	0.0344
RN ↓	min_pulse_width to RN	0.0632	0.0615	0.0779	0.0779
RN ↑	recovery_rising to CP	0.0197	0.0197	0.0149	0.0149
RN ↑	removal_rising to CP	-0.0098	-0.0101	-0.0076	-0.0076
TE ↓	hold_rising to CP	-0.0429	-0.0166	-0.0166	-0.0166
TE ↑	hold_rising to CP	-0.0383	-0.0242	-0.0242	-0.0242
TE ↓	setup_rising to CP	0.0796	0.0609	0.0609	0.0609
TE ↑	setup_rising to CP	0.1512	0.1223	0.1223	0.1223
TI ↓	hold_rising to CP	-0.1229	-0.0678	-0.0680	-0.0680
TI ↑	hold_rising to CP	-0.0421	-0.0264	-0.0249	-0.0249
TI ↓	setup_rising to CP	0.1625	0.1188	0.1186	0.1186
TI ↑	setup_rising to CP	0.0720	0.0546	0.0561	0.0561

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	2.946e-05	5.347e-09
X8_P10	3.180e-05	5.120e-09
X17_P10	3.954e-05	5.286e-09
X33_P10	4.775e-05	5.617e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.827e-03	5.894e-03	5.916e-03	5.927e-03

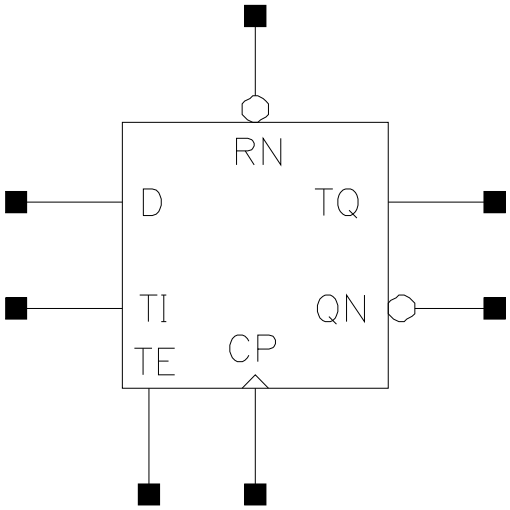
Clock 100Mhz Data 25Mhz	8.844e-03	8.950e-03	9.899e-03	1.100e-02
Clock 100Mhz Data 50Mhz	1.186e-02	1.201e-02	1.388e-02	1.608e-02
Clock = 0 Data 100Mhz	7.222e-03	6.651e-03	6.467e-03	6.376e-03
Clock = 1 Data 100Mhz	1.847e-03	9.563e-04	6.594e-04	5.110e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008

RN	0.0011	0.0008	0.0010	0.0010
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0750	0.0650	3.2014	1.7905
CP to QN ↑	0.0977	0.0540	5.0736	2.9297
CP to TQ ↓	0.0678	0.0360	4.1893	3.3808
CP to TQ ↑	0.0617	0.0508	8.5437	7.9416
RN to QN ↑	0.0685	0.0751	5.1479	2.9327
RN to TQ ↓	0.0508	0.0595	3.6239	3.2911
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0677	0.0736	0.8888	0.4689
CP to QN ↑	0.0551	0.0583	1.4641	0.7375
CP to TQ ↓	0.0376	0.0390	4.1688	4.0834
CP to TQ ↑	0.0507	0.0521	7.4833	7.5911
RN to QN ↑	0.0757	0.0780	1.4655	0.7378
RN to TQ ↓	0.0606	0.0613	4.0702	3.9791

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0992	0.0981	0.0992	0.0992
CP ↑	min_pulse_width to CP	0.0657	0.0301	0.0301	0.0301
D ↓	hold_rising to CP	-0.0594	-0.0166	-0.0188	-0.0188
D ↑	hold_rising to CP	-0.0286	-0.0047	-0.0047	-0.0047
D ↓	setup_rising to CP	0.0995	0.0635	0.0635	0.0635
D ↑	setup_rising to CP	0.0560	0.0344	0.0344	0.0344
RN ↓	min_pulse_width to RN	0.0681	0.0708	0.0708	0.0757
RN ↑	recovery_rising to CP	0.0197	0.0149	0.0172	0.0172
RN ↑	removal_rising to CP	-0.0149	-0.0076	-0.0080	-0.0080
TE ↓	hold_rising to CP	-0.0429	-0.0166	-0.0166	-0.0166
TE ↑	hold_rising to CP	-0.0383	-0.0242	-0.0242	-0.0242
TE ↓	setup_rising to CP	0.0796	0.0609	0.0609	0.0609
TE ↑	setup_rising to CP	0.1512	0.1223	0.1223	0.1223
TI ↓	hold_rising to CP	-0.1229	-0.0678	-0.0678	-0.0680
TI ↑	hold_rising to CP	-0.0421	-0.0249	-0.0264	-0.0264
TI ↓	setup_rising to CP	0.1584	0.1188	0.1186	0.1186
TI ↑	setup_rising to CP	0.0720	0.0561	0.0561	0.0561

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	3.090e-05	5.451e-09
X8_P10	3.338e-05	5.120e-09
X17_P10	3.914e-05	5.451e-09
X33_P10	4.859e-05	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

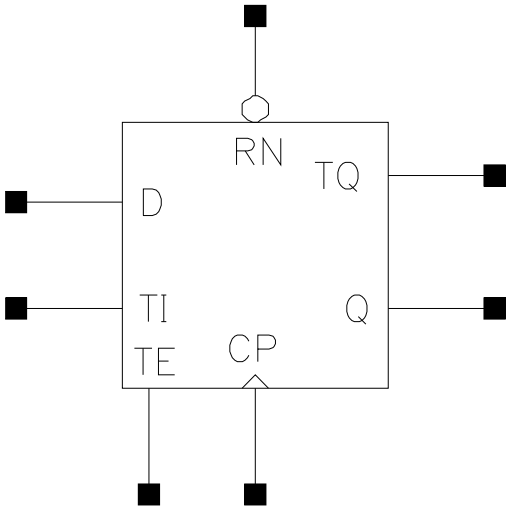
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.825e-03	5.897e-03	5.948e-03	5.975e-03
Clock 100Mhz Data 25Mhz	9.236e-03	9.204e-03	9.790e-03	1.108e-02
Clock 100Mhz Data 50Mhz	1.265e-02	1.251e-02	1.363e-02	1.618e-02
Clock = 0 Data 100Mhz	7.213e-03	6.648e-03	6.456e-03	6.360e-03
Clock = 1 Data 100Mhz	1.847e-03	9.651e-04	6.710e-04	5.241e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008

RN	0.0010	0.0010	0.0009	0.0009
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0825	0.0433	4.2075	1.8655
CP to Q ↑	0.0641	0.0529	6.0069	3.0107
CP to TQ ↓	0.0778	0.0432	5.2090	4.4212
CP to TQ ↑	0.0665	0.0556	11.3076	10.3318
RN to Q ↓	0.0560	0.0641	3.6499	1.8027
RN to TQ ↓	0.0536	0.0642	4.5836	4.2998
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0620	0.0681	0.8813	0.4642
CP to Q ↑	0.0758	0.0803	1.4324	0.7302
CP to TQ ↓	0.0643	0.0719	4.1859	4.2677
CP to TQ ↑	0.0804	0.0876	10.1386	10.1856
RN to Q ↓	0.0763	0.0825	0.8818	0.4637
RN to TQ ↓	0.0786	0.0864	4.1852	4.2683

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1010	0.0982	0.0993	0.0981
CP ↑	min_pulse_width to CP	0.0724	0.0338	0.0253	0.0253
D ↓	hold_rising to CP	-0.0597	-0.0166	-0.0188	-0.0188
D ↑	hold_rising to CP	-0.0286	-0.0047	-0.0047	-0.0047
D ↓	setup_rising to CP	0.0995	0.0635	0.0635	0.0635
D ↑	setup_rising to CP	0.0560	0.0344	0.0344	0.0344
RN ↓	min_pulse_width to RN	0.0708	0.0806	0.0637	0.0637
RN ↑	recovery_rising to CP	0.0174	0.0197	0.0149	0.0149
RN ↑	removal_rising to CP	-0.0098	-0.0101	-0.0076	-0.0076
TE ↓	hold_rising to CP	-0.0429	-0.0169	-0.0166	-0.0166
TE ↑	hold_rising to CP	-0.0383	-0.0242	-0.0242	-0.0242
TE ↓	setup_rising to CP	0.0796	0.0609	0.0609	0.0609
TE ↑	setup_rising to CP	0.1512	0.1223	0.1223	0.1223
TI ↓	hold_rising to CP	-0.1229	-0.0680	-0.0678	-0.0678
TI ↑	hold_rising to CP	-0.0421	-0.0249	-0.0264	-0.0264
TI ↓	setup_rising to CP	0.1584	0.1186	0.1186	0.1186
TI ↑	setup_rising to CP	0.0720	0.0561	0.0546	0.0546

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	2.928e-05	5.451e-09
X8_P10	3.117e-05	5.120e-09
X17_P10	3.924e-05	5.451e-09
X33_P10	4.520e-05	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

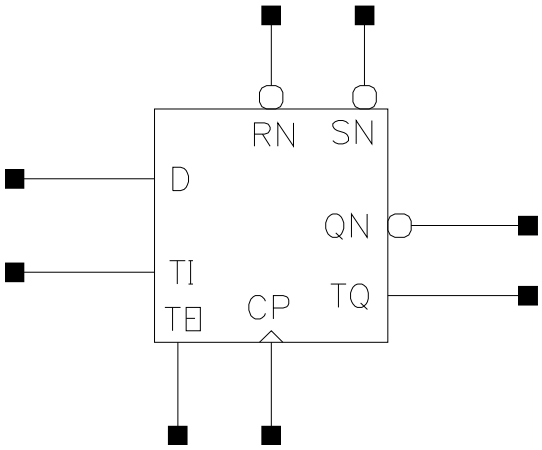
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.863e-03	5.918e-03	5.935e-03	5.943e-03
Clock 100Mhz Data 25Mhz	9.377e-03	9.216e-03	1.030e-02	1.142e-02
Clock 100Mhz Data 50Mhz	1.289e-02	1.251e-02	1.466e-02	1.689e-02
Clock = 0 Data 100Mhz	7.222e-03	6.653e-03	6.464e-03	6.369e-03
Clock = 1 Data 100Mhz	1.849e-03	9.572e-04	6.600e-04	5.115e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.352	5.2224
X17_P10	1.200	4.488	5.3856
X33_P10	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007
RN	0.0010	0.0010	0.0010

SN	0.0014	0.0014	0.0014
TE	0.0012	0.0012	0.0012
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0718	0.0770	1.7375	0.8955
CP to QN ↑	0.0555	0.0586	2.8393	1.4357
CP to TQ ↓	0.0415	0.0415	5.1872	5.1886
CP to TQ ↑	0.0590	0.0590	13.0615	13.0736
RN to QN ↓	0.0656	0.0717	1.7448	0.8976
RN to QN ↑	0.0650	0.0677	2.8344	1.4352
RN to TQ ↓	0.0525	0.0525	5.0946	5.0899
RN to TQ ↑	0.0515	0.0514	13.2008	13.2093
SN to QN ↓	0.0729	0.0780	1.7399	0.8964
SN to TQ ↑	0.0605	0.0605	13.0533	13.0633
	X33_P10		**X33_P10**	
CP to QN ↓	0.0897		0.4777	
CP to QN ↑	0.0662		0.7347	
CP to TQ ↓	0.0416		5.2041	
CP to TQ ↑	0.0592		13.1066	
RN to QN ↓	0.0859		0.4776	
RN to QN ↑	0.0745		0.7348	
RN to TQ ↓	0.0526		5.1083	
RN to TQ ↑	0.0516		13.2776	
SN to QN ↓	0.0905		0.4779	
SN to TQ ↑	0.0607		13.0995	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1041	0.1041	0.1041
CP ↑	min_pulse_width to CP	0.0301	0.0301	0.0349
D ↓	hold_rising to CP	-0.0188	-0.0188	-0.0188
D ↑	hold_rising to CP	-0.0047	-0.0047	-0.0047
D ↓	setup_rising to CP	0.0683	0.0683	0.0683
D ↑	setup_rising to CP	0.0344	0.0344	0.0344
RN ↓	min_pulse_width to RN	0.0730	0.0779	0.0828
RN ↑	non_seq_hold_rising to SN	-0.0286	-0.0286	-0.0286
RN ↑	non_seq_setup_rising to SN	0.0669	0.0669	0.0669
RN ↑	recovery_rising to CP	0.0268	0.0268	0.0268
RN ↑	removal_rising to CP	-0.0171	-0.0171	-0.0171
SN ↓	min_pulse_width to SN	0.0642	0.0669	0.0696
SN ↑	recovery_rising to CP	0.0085	0.0085	0.0085
SN ↑	removal_rising to CP	0.0311	0.0311	0.0311

TE ↓	hold_rising to CP	-0.0166	-0.0166	-0.0166
TE ↑	hold_rising to CP	-0.0242	-0.0242	-0.0242
TE ↓	setup_rising to CP	0.0660	0.0660	0.0660
TE ↑	setup_rising to CP	0.1272	0.1272	0.1272
TI ↓	hold_rising to CP	-0.0693	-0.0693	-0.0693
TI ↑	hold_rising to CP	-0.0249	-0.0249	-0.0249
TI ↓	setup_rising to CP	0.1235	0.1235	0.1235
TI ↑	setup_rising to CP	0.0561	0.0561	0.0561

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	3.684e-05	5.800e-09
X17_P10	4.144e-05	5.966e-09
X33_P10	4.934e-05	6.297e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

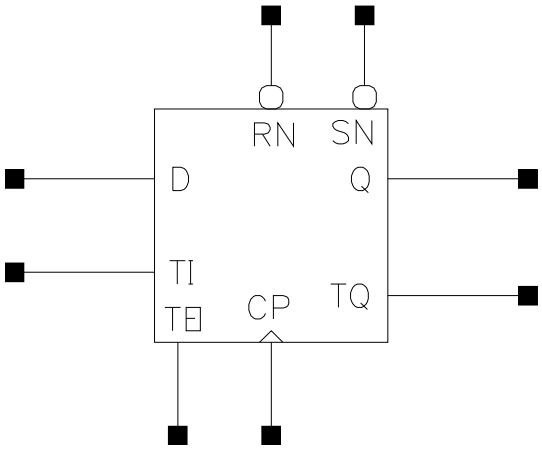
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	6.261e-03	6.261e-03	6.263e-03
Clock 100Mhz Data 25Mhz	9.590e-03	1.013e-02	1.163e-02
Clock 100Mhz Data 50Mhz	1.292e-02	1.401e-02	1.699e-02
Clock = 0 Data 100Mhz	6.292e-03	6.290e-03	6.291e-03
Clock = 1 Data 100Mhz	8.494e-05	8.501e-05	8.506e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.216	5.0592
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007
RN	0.0010	0.0010	0.0010

SN	0.0014	0.0014	0.0014
TE	0.0012	0.0012	0.0012
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0467	0.0530	1.8174	0.9434
CP to Q ↑	0.0580	0.0618	2.9078	1.4789
CP to TQ ↓	0.0476	0.0543	5.2870	5.3800
CP to TQ ↑	0.0636	0.0705	12.8165	12.9063
RN to Q ↓	0.0552	0.0589	1.7507	0.9049
RN to Q ↑	0.0615	0.0643	2.8920	1.4673
RN to TQ ↓	0.0561	0.0602	5.1619	5.2202
RN to TQ ↑	0.0667	0.0720	12.7579	12.8371
SN to Q ↑	0.0591	0.0621	2.8951	1.4693
SN to TQ ↑	0.0641	0.0697	12.7825	12.8632
	X33_P10		**X33_P10**	
CP to Q ↓	0.0685		0.5095	
CP to Q ↑	0.0716		0.7659	
CP to TQ ↓	0.0663		5.6250	
CP to TQ ↑	0.0831		13.0720	
RN to Q ↓	0.0686		0.4827	
RN to Q ↑	0.0718		0.7569	
RN to TQ ↓	0.0676		5.3836	
RN to TQ ↑	0.0815		12.9752	
SN to Q ↑	0.0699		0.7564	
SN to TQ ↑	0.0796		12.9946	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1041	0.1041	0.1041
CP ↑	min_pulse_width to CP	0.0349	0.0434	0.0579
D ↓	hold_rising to CP	-0.0188	-0.0191	-0.0166
D ↑	hold_rising to CP	-0.0047	-0.0047	-0.0047
D ↓	setup_rising to CP	0.0683	0.0683	0.0683
D ↑	setup_rising to CP	0.0344	0.0344	0.0344
RN ↓	min_pulse_width to RN	0.0876	0.1023	0.1316
RN ↑	non_seq_hold_rising to SN	-0.0336	-0.0383	-0.0531
RN ↑	non_seq_setup_rising to SN	0.0620	0.0620	0.0825
RN ↑	recovery_rising to CP	0.0246	0.0246	0.0246
RN ↑	removal_rising to CP	-0.0149	-0.0149	-0.0149
SN ↓	min_pulse_width to SN	0.0696	0.0793	0.0989
SN ↑	recovery_rising to CP	0.0082	0.0082	0.0082
SN ↑	removal_rising to CP	0.0311	0.0311	0.0311

TE ↓	hold_rising to CP	-0.0166	-0.0166	-0.0166
TE ↑	hold_rising to CP	-0.0242	-0.0242	-0.0242
TE ↓	setup_rising to CP	0.0660	0.0658	0.0658
TE ↑	setup_rising to CP	0.1272	0.1272	0.1272
TI ↓	hold_rising to CP	-0.0678	-0.0678	-0.0680
TI ↑	hold_rising to CP	-0.0249	-0.0249	-0.0249
TI ↓	setup_rising to CP	0.1235	0.1235	0.1235
TI ↑	setup_rising to CP	0.0561	0.0561	0.0561

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P10	3.538e-05	5.628e-09
X17_P10	3.911e-05	5.794e-09
X33_P10	4.567e-05	6.125e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

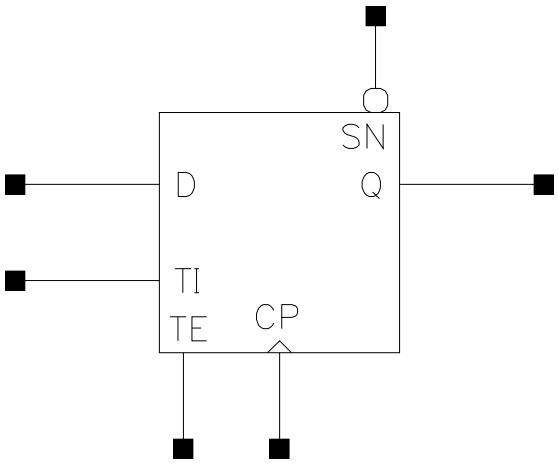
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	6.238e-03	6.238e-03	6.240e-03
Clock 100Mhz Data 25Mhz	9.513e-03	1.025e-02	1.227e-02
Clock 100Mhz Data 50Mhz	1.279e-02	1.426e-02	1.829e-02
Clock = 0 Data 100Mhz	6.289e-03	6.288e-03	6.288e-03
Clock = 1 Data 100Mhz	8.470e-05	8.475e-05	8.485e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0005	0.0005	0.0005
SN	0.0016	0.0016	0.0016	0.0016
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005
	X33_P10			

CP	0.0011			
D	0.0005			
SN	0.0016			
TE	0.0012			
TI	0.0005			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to Q ↓	0.0725	0.0409	3.9843	1.8028
CP to Q ↑	0.0624	0.0530	5.8395	2.8934
SN to Q ↑	0.0430	0.0451	5.6863	2.8701
	X17_P10	X25_P10	X17_P10	X25_P10
CP to Q ↓	0.0588	0.0621	0.8694	0.6028
CP to Q ↑	0.0752	0.0779	1.4251	0.9662
SN to Q ↑	0.0680	0.0707	1.4256	0.9660
	X33_P10		X33_P10	
CP to Q ↓	0.0648		0.4584	
CP to Q ↑	0.0798		0.7274	
SN to Q ↑	0.0726		0.7273	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.1021	0.1040	0.1040	0.1040
CP ↑	min_pulse_width to CP	0.0627	0.0301	0.0253	0.0253
D ↓	hold_rising to CP	-0.0650	-0.0215	-0.0215	-0.0215
D ↑	hold_rising to CP	-0.0264	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.1021	0.0711	0.0711	0.0711
D ↑	setup_rising to CP	0.0530	0.0295	0.0295	0.0295
SN ↓	min_pulse_width to SN	0.0474	0.0522	0.0496	0.0496
SN ↑	recovery_rising to CP	0.0081	0.0085	0.0085	0.0085
SN ↑	removal_rising to CP	0.0239	0.0312	0.0312	0.0312
TE ↓	hold_rising to CP	-0.0429	-0.0193	-0.0215	-0.0215
TE ↑	hold_rising to CP	-0.0331	-0.0193	-0.0193	-0.0193
TE ↓	setup_rising to CP	0.0849	0.0660	0.0660	0.0660
TE ↑	setup_rising to CP	0.1565	0.1299	0.1299	0.1299
TI ↓	hold_rising to CP	-0.1244	-0.0742	-0.0742	-0.0742
TI ↑	hold_rising to CP	-0.0382	-0.0200	-0.0215	-0.0215
TI ↓	setup_rising to CP	0.1640	0.1270	0.1270	0.1270
TI ↑	setup_rising to CP	0.0679	0.0497	0.0497	0.0497
		X33_P10			

CP ↓	min_pulse_width to CP	0.1040			
CP ↑	min_pulse_width to CP	0.0253			
D ↓	hold_rising to CP	-0.0215			
D ↑	hold_rising to CP	0.0009			
D ↓	setup_rising to CP	0.0711			
D ↑	setup_rising to CP	0.0295			
SN ↓	min_pulse_width to SN	0.0496			
SN ↑	recovery_rising to CP	0.0085			
SN ↑	removal_rising to CP	0.0312			
TE ↓	hold_rising to CP	-0.0215			
TE ↑	hold_rising to CP	-0.0193			
TE ↓	setup_rising to CP	0.0660			
TE ↑	setup_rising to CP	0.1299			
TI ↓	hold_rising to CP	-0.0742			
TI ↑	hold_rising to CP	-0.0215			
TI ↓	setup_rising to CP	0.1270			
TI ↑	setup_rising to CP	0.0497			

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	2.971e-05	5.286e-09
X8_P10	3.216e-05	5.120e-09
X17_P10	4.000e-05	5.451e-09
X25_P10	4.413e-05	5.617e-09
X33_P10	4.821e-05	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	5.716e-03	5.869e-03	5.918e-03	5.943e-03
Clock 100Mhz Data 25Mhz	8.893e-03	9.005e-03	1.001e-02	1.058e-02
Clock 100Mhz Data 50Mhz	1.207e-02	1.214e-02	1.410e-02	1.522e-02
Clock = 0 Data 100Mhz	6.944e-03	6.536e-03	6.401e-03	6.333e-03
Clock = 1 Data 100Mhz	1.849e-03	9.571e-04	6.599e-04	5.114e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	5.958e-03			

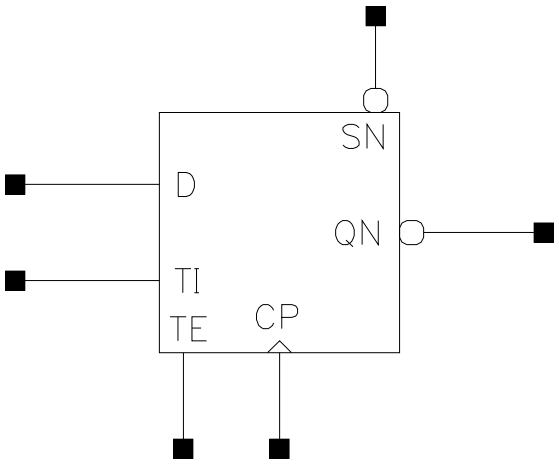
Clock 100Mhz Data 25Mhz	1.109e-02			
Clock 100Mhz Data 50Mhz	1.623e-02			
Clock = 0 Data 100Mhz	6.292e-03			
Clock = 1 Data 100Mhz	4.223e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0005	0.0005	0.0005
SN	0.0016	0.0016	0.0016	0.0016
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005
	X33_P10			

CP	0.0011			
D	0.0005			
SN	0.0016			
TE	0.0012			
TI	0.0005			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0700	0.0630	3.1960	1.7064
CP to QN ↑	0.0745	0.0474	5.6414	2.8355
SN to QN ↓	0.0523	0.0558	3.1850	1.7047
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
CP to QN ↓	0.0663	0.0704	0.8730	0.6043
CP to QN ↑	0.0562	0.0598	1.4262	0.9681
SN to QN ↓	0.0574	0.0611	0.8710	0.6028
	X33_P10		**X33_P10**	
CP to QN ↓	0.0736		0.4599	
CP to QN ↑	0.0624		0.7280	
SN to QN ↓	0.0641		0.4593	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.1021	0.1040	0.1040	0.1040
CP ↑	min_pulse_width to CP	0.0434	0.0253	0.0301	0.0338
D ↓	hold_rising to CP	-0.0650	-0.0215	-0.0215	-0.0215
D ↑	hold_rising to CP	-0.0261	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.1021	0.0711	0.0711	0.0711
D ↑	setup_rising to CP	0.0530	0.0295	0.0295	0.0295
SN ↓	min_pulse_width to SN	0.0425	0.0496	0.0544	0.0544
SN ↑	recovery_rising to CP	0.0056	0.0085	0.0082	0.0082
SN ↑	removal_rising to CP	0.0239	0.0312	0.0312	0.0312
TE ↓	hold_rising to CP	-0.0429	-0.0215	-0.0193	-0.0193
TE ↑	hold_rising to CP	-0.0331	-0.0193	-0.0193	-0.0193
TE ↓	setup_rising to CP	0.0849	0.0660	0.0660	0.0660
TE ↑	setup_rising to CP	0.1565	0.1299	0.1299	0.1299
TI ↓	hold_rising to CP	-0.1239	-0.0742	-0.0742	-0.0742
TI ↑	hold_rising to CP	-0.0382	-0.0215	-0.0200	-0.0200
TI ↓	setup_rising to CP	0.1640	0.1285	0.1285	0.1285
TI ↑	setup_rising to CP	0.0679	0.0497	0.0497	0.0497
		X33_P10			

CP ↓	min_pulse_width to CP	0.1040			
CP ↑	min_pulse_width to CP	0.0338			
D ↓	hold_rising to CP	-0.0215			
D ↑	hold_rising to CP	0.0009			
D ↓	setup_rising to CP	0.0711			
D ↑	setup_rising to CP	0.0295			
SN ↓	min_pulse_width to SN	0.0544			
SN ↑	recovery_rising to CP	0.0082			
SN ↑	removal_rising to CP	0.0312			
TE ↓	hold_rising to CP	-0.0193			
TE ↑	hold_rising to CP	-0.0193			
TE ↓	setup_rising to CP	0.0660			
TE ↑	setup_rising to CP	0.1299			
TI ↓	hold_rising to CP	-0.0742			
TI ↑	hold_rising to CP	-0.0200			
TI ↓	setup_rising to CP	0.1285			
TI ↑	setup_rising to CP	0.0497			

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	2.862e-05	5.286e-09
X8_P10	3.029e-05	5.120e-09
X17_P10	3.849e-05	5.451e-09
X25_P10	4.144e-05	5.617e-09
X33_P10	4.442e-05	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	5.716e-03	5.870e-03	5.916e-03	5.940e-03
Clock 100Mhz Data 25Mhz	8.666e-03	8.910e-03	1.006e-02	1.065e-02
Clock 100Mhz Data 50Mhz	1.162e-02	1.195e-02	1.419e-02	1.536e-02
Clock = 0 Data 100Mhz	6.945e-03	6.541e-03	6.402e-03	6.334e-03
Clock = 1 Data 100Mhz	1.849e-03	9.575e-04	6.604e-04	5.119e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	5.954e-03			

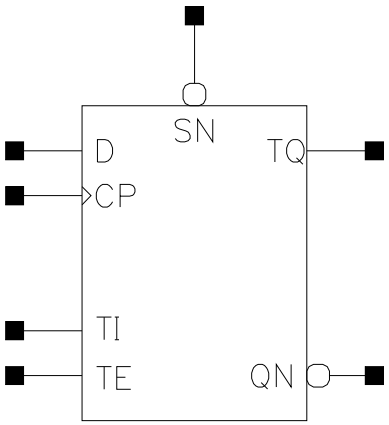
Clock 100Mhz Data 25Mhz	1.120e-02			
Clock 100Mhz Data 50Mhz	1.644e-02			
Clock = 0 Data 100Mhz	6.293e-03			
Clock = 1 Data 100Mhz	4.228e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.216	5.0592
X8_P10	1.200	4.080	4.8960
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0005	0.0005	0.0005

SN	0.0017	0.0018	0.0017	0.0017
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0802	0.0661	3.1933	1.7136
CP to QN ↑	0.0971	0.0539	5.5621	2.8846
CP to TQ ↓	0.0696	0.0363	4.6979	3.8894
CP to TQ ↑	0.0620	0.0497	7.6255	7.4438
SN to QN ↓	0.0514	0.0574	3.1954	1.7119
SN to TQ ↑	0.0365	0.0405	7.4813	7.4615
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0666	0.0739	0.8927	0.4550
CP to QN ↑	0.0607	0.0674	1.4370	0.7317
CP to TQ ↓	0.0452	0.0451	4.0687	4.0699
CP to TQ ↑	0.0560	0.0560	7.5029	7.5204
SN to QN ↓	0.0516	0.0581	0.8924	0.4551
SN to TQ ↑	0.0419	0.0420	7.4314	7.4505

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1021	0.1040	0.1040	0.1040
CP ↑	min_pulse_width to CP	0.0638	0.0290	0.0349	0.0386
D ↓	hold_rising to CP	-0.0650	-0.0215	-0.0215	-0.0215
D ↑	hold_rising to CP	-0.0261	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.1021	0.0711	0.0711	0.0711
D ↑	setup_rising to CP	0.0530	0.0295	0.0295	0.0295
SN ↓	min_pulse_width to SN	0.0398	0.0425	0.0425	0.0452
SN ↑	recovery_rising to CP	0.0056	0.0029	0.0029	0.0054
SN ↑	removal_rising to CP	0.0239	0.0312	0.0312	0.0312
TE ↓	hold_rising to CP	-0.0429	-0.0218	-0.0193	-0.0193
TE ↑	hold_rising to CP	-0.0331	-0.0193	-0.0193	-0.0193
TE ↓	setup_rising to CP	0.0849	0.0660	0.0660	0.0660
TE ↑	setup_rising to CP	0.1565	0.1299	0.1324	0.1324
TI ↓	hold_rising to CP	-0.1244	-0.0742	-0.0742	-0.0742
TI ↑	hold_rising to CP	-0.0423	-0.0200	-0.0200	-0.0200
TI ↓	setup_rising to CP	0.1640	0.1285	0.1285	0.1285
TI ↑	setup_rising to CP	0.0679	0.0497	0.0497	0.0497

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	3.167e-05	5.617e-09
X8_P10	3.332e-05	5.451e-09
X17_P10	4.152e-05	5.782e-09
X33_P10	4.745e-05	6.114e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

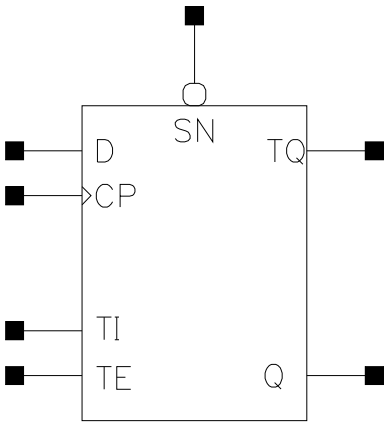
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.723e-03	5.876e-03	5.929e-03	5.955e-03
Clock 100Mhz Data 25Mhz	9.188e-03	9.256e-03	1.034e-02	1.147e-02
Clock 100Mhz Data 50Mhz	1.265e-02	1.264e-02	1.474e-02	1.699e-02
Clock = 0 Data 100Mhz	6.958e-03	6.549e-03	6.413e-03	6.345e-03
Clock = 1 Data 100Mhz	1.849e-03	9.572e-04	6.599e-04	5.113e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.944	4.7328
X17_P10	1.200	4.216	5.0592
X33_P10	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0005	0.0005	0.0005

SN	0.0017	0.0016	0.0016	0.0016
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0838	0.0442	4.1046	1.8418
CP to Q ↑	0.0667	0.0553	5.8664	2.9293
CP to TQ ↓	0.0843	0.0454	5.7974	4.4430
CP to TQ ↑	0.0657	0.0605	7.6847	10.4277
SN to Q ↑	0.0385	0.0467	5.7003	2.8991
SN to TQ ↑	0.0377	0.0508	7.5039	10.3764
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0604	0.0664	0.8927	0.4663
CP to Q ↑	0.0766	0.0810	1.4327	0.7301
CP to TQ ↓	0.0628	0.0703	4.1846	4.2585
CP to TQ ↑	0.0814	0.0882	10.1445	10.1940
SN to Q ↑	0.0694	0.0738	1.4337	0.7303
SN to TQ ↑	0.0742	0.0810	10.1410	10.1926

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1021	0.1040	0.1040	0.1040
CP ↑	min_pulse_width to CP	0.0734	0.0338	0.0253	0.0253
D ↓	hold_rising to CP	-0.0650	-0.0215	-0.0215	-0.0215
D ↑	hold_rising to CP	-0.0264	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.1021	0.0711	0.0711	0.0711
D ↑	setup_rising to CP	0.0530	0.0295	0.0295	0.0295
SN ↓	min_pulse_width to SN	0.0398	0.0571	0.0496	0.0496
SN ↑	recovery_rising to CP	0.0081	0.0082	0.0085	0.0085
SN ↑	removal_rising to CP	0.0239	0.0312	0.0312	0.0312
TE ↓	hold_rising to CP	-0.0429	-0.0197	-0.0215	-0.0215
TE ↑	hold_rising to CP	-0.0331	-0.0193	-0.0193	-0.0193
TE ↓	setup_rising to CP	0.0849	0.0660	0.0660	0.0660
TE ↑	setup_rising to CP	0.1565	0.1299	0.1299	0.1299
TI ↓	hold_rising to CP	-0.1244	-0.0742	-0.0742	-0.0742
TI ↑	hold_rising to CP	-0.0382	-0.0200	-0.0215	-0.0215
TI ↓	setup_rising to CP	0.1638	0.1270	0.1270	0.1270
TI ↑	setup_rising to CP	0.0679	0.0497	0.0497	0.0497

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	3.166e-05	5.451e-09
X8_P10	3.406e-05	5.286e-09
X17_P10	4.182e-05	5.617e-09
X33_P10	5.000e-05	5.948e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

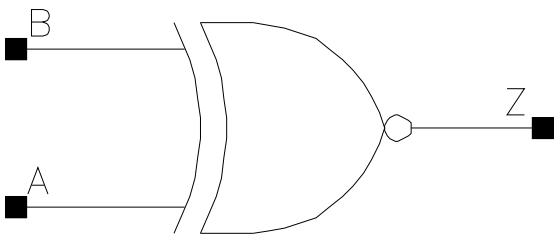
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	5.718e-03	5.870e-03	5.919e-03	5.944e-03
Clock 100Mhz Data 25Mhz	9.288e-03	9.297e-03	1.030e-02	1.144e-02
Clock 100Mhz Data 50Mhz	1.286e-02	1.272e-02	1.468e-02	1.694e-02
Clock = 0 Data 100Mhz	6.958e-03	6.543e-03	6.405e-03	6.335e-03
Clock = 1 Data 100Mhz	1.849e-03	9.575e-04	6.602e-04	5.116e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P10	X8_P10	X17_P10	X25_P10
A	0.0019	0.0008	0.0011	0.0017
B	0.0016	0.0016	0.0020	0.0028
	X33_P10			
A	0.0019			
B	0.0033			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X8_P10**	**X6_P10**	**X8_P10**
A to Z ↓	0.0193	0.0426	3.0116	1.8593
A to Z ↑	0.0204	0.0396	4.3851	2.9843
B to Z ↓	0.0179	0.0298	3.0097	1.8397
B to Z ↑	0.0210	0.0287	4.3950	2.9761
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
A to Z ↓	0.0411	0.0417	0.9141	0.6279
A to Z ↑	0.0368	0.0373	1.4642	0.9754

B to Z ↓	0.0308	0.0300	0.9097	0.6253
B to Z ↑	0.0291	0.0283	1.4615	0.9726
	X33_P10		**X33_P10**	
A to Z ↓	0.0398		0.4708	
A to Z ↑	0.0363		0.7325	
B to Z ↓	0.0290		0.4693	
B to Z ↑	0.0281		0.7316	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P10	1.216e-05	1.642e-09
X8_P10	1.726e-05	2.139e-09
X17_P10	2.557e-05	2.304e-09
X25_P10	4.103e-05	3.298e-09
X33_P10	5.168e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	3.644e-03	6.831e-03	1.009e-02	1.617e-02
B to Z	3.485e-03	4.843e-03	7.811e-03	1.226e-02
	X33_P10			
A to Z	1.986e-02			
B to Z	1.553e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

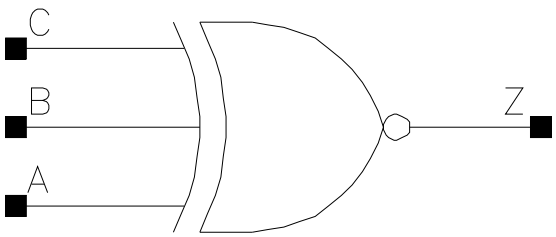
Pin Cycle (vdds)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	7.953e-07	1.331e-07	3.902e-07	-1.245e-07
B to Z	9.267e-06	4.351e-07	4.212e-07	1.069e-06
	X33_P10			
A to Z	3.264e-07			
B to Z	9.186e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	2.176	2.6112
X16_P10	1.200	2.720	3.2640
X25_P10	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X16_P10	X25_P10
A	0.0032	0.0027	0.0034	0.0049
B	0.0035	0.0025	0.0033	0.0045
C	0.0022	0.0008	0.0008	0.0009

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0305	0.0514	3.5570	1.9580
A to Z ↑	0.0299	0.0470	6.2080	2.9569
B to Z ↓	0.0313	0.0517	3.5615	1.9576
B to Z ↑	0.0302	0.0474	6.2047	2.9590
C to Z ↓	0.0309	0.0686	3.5678	1.9570
C to Z ↑	0.0292	0.0638	6.2088	2.9572
	X16_P10	**X25_P10**	**X16_P10**	**X25_P10**
A to Z ↓	0.0520	0.0522	1.0044	0.6421
A to Z ↑	0.0509	0.0511	1.5476	0.9775
B to Z ↓	0.0526	0.0534	1.0043	0.6421

B to Z ↑	0.0514	0.0523	1.5484	0.9776
C to Z ↓	0.0732	0.0782	1.0038	0.6416
C to Z ↑	0.0712	0.0767	1.5478	0.9780

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	1.510e-05	2.967e-09
X8_P10	1.661e-05	3.132e-09
X16_P10	2.572e-05	3.795e-09
X25_P10	3.654e-05	5.286e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	3.948e-03	5.480e-03	9.096e-03	1.382e-02
B to Z	3.794e-03	5.360e-03	8.975e-03	1.372e-02
C to Z	3.672e-03	8.136e-03	1.233e-02	1.865e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

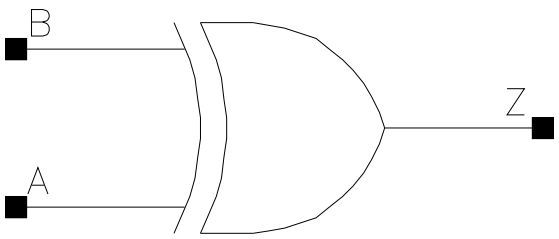
Pin Cycle (vdds)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	-3.488e-06	-1.761e-06	-2.178e-06	-3.523e-06
B to Z	3.014e-05	1.209e-05	1.936e-05	2.955e-05
C to Z	4.717e-05	2.252e-05	3.249e-05	4.717e-05

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.224	1.4688
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.224	1.4688
X16_P10	1.200	1.360	1.6320
X25_P10	1.200	2.176	2.6112
X31_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X16_P10
A	0.0008	0.0018	0.0011	0.0013
B	0.0014	0.0016	0.0016	0.0018
	X25_P10	X31_P10		
A	0.0017	0.0022		
B	0.0029	0.0037		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0386	0.0193	3.2699	2.3684
A to Z ↑	0.0371	0.0217	5.5156	5.5219
B to Z ↓	0.0280	0.0199	3.2426	2.3878
B to Z ↑	0.0281	0.0201	5.5105	5.5201
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0349	0.0369	1.8132	0.9372

A to Z ↑	0.0325	0.0345	2.9122	1.4679
B to Z ↓	0.0271	0.0284	1.8040	0.9333
B to Z ↑	0.0260	0.0278	2.9113	1.4671
	X25_P10	**X31_P10**	**X25_P10**	**X31_P10**
A to Z ↓	0.0391	0.0370	0.6225	0.4980
A to Z ↑	0.0364	0.0348	0.9724	0.7822
B to Z ↓	0.0292	0.0275	0.6222	0.4974
B to Z ↑	0.0277	0.0265	0.9722	0.7825

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	1.451e-05	1.973e-09
X6_P10	1.292e-05	1.642e-09
X8_P10	2.067e-05	1.973e-09
X16_P10	2.773e-05	2.139e-09
X25_P10	4.010e-05	3.132e-09
X31_P10	5.022e-05	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	5.142e-03	3.639e-03	6.369e-03	9.447e-03
B to Z	3.984e-03	3.416e-03	5.251e-03	7.884e-03
	X25_P10	X31_P10		
A to Z	1.489e-02	1.825e-02		
B to Z	1.104e-02	1.353e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

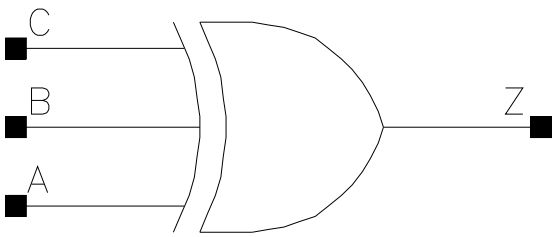
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	1.210e-08	1.244e-06	5.561e-07	7.300e-09
B to Z	2.527e-07	1.282e-05	7.149e-07	6.079e-07
	X25_P10	X31_P10		
A to Z	2.702e-07	7.160e-07		
B to Z	4.003e-07	6.107e-07		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X24_P10	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X24_P10
A	0.0028	0.0027	0.0034	0.0059
B	0.0028	0.0025	0.0031	0.0049
C	0.0009	0.0018	0.0025	0.0037

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0308	0.0514	3.7496	1.9571
A to Z ↑	0.0300	0.0470	6.7764	2.9549
B to Z ↓	0.0312	0.0518	3.7537	1.9561
B to Z ↑	0.0304	0.0474	6.7721	2.9561
C to Z ↓	0.0537	0.0507	3.7364	1.9573
C to Z ↑	0.0529	0.0461	6.7517	2.9558
	X17_P10	**X24_P10**	**X17_P10**	**X24_P10**
A to Z ↓	0.0479	0.0555	0.9347	0.6750
A to Z ↑	0.0470	0.0423	1.4435	0.9800
B to Z ↓	0.0482	0.0559	0.9342	0.6745

B to Z ↑	0.0473	0.0424	1.4435	0.9800
C to Z ↓	0.0477	0.0544	0.9343	0.6742
C to Z ↑	0.0468	0.0421	1.4430	0.9805

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P10	1.714e-05	2.967e-09
X8_P10	1.395e-05	2.801e-09
X17_P10	2.269e-05	2.967e-09
X24_P10	3.995e-05	5.120e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	3.704e-03	5.484e-03	8.780e-03	1.481e-02
B to Z	3.631e-03	5.356e-03	8.621e-03	1.449e-02
C to Z	7.323e-03	5.215e-03	8.534e-03	1.422e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	-2.123e-06	-1.975e-06	-2.230e-06	-8.517e-06
B to Z	1.973e-05	1.213e-05	2.056e-05	3.089e-05
C to Z	3.684e-05	2.585e-05	3.720e-05	7.551e-05

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