

## 1. Release Notes

### 1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library Name	C28SOI_IO_EXT_ALLF_CORESUPPLY_EG_6U1X2T8XLB
Library Version	7.1
Library Type	IO Cells
Technology	CMOS028_FDSOI
DK Version	

### 1.2 Impact of Product Release

For latest information, please refer to LYS (<http://col2.cro.st.com/libyield>).

### 1.3 Related Documentation

- C28SOI\_IO\_EXT\_ALLF\_CORESUPPLY\_EG Release Notes and Known Problems and Solutions
- C28SOI\_IO\_EXT\_ALLF\_CORESUPPLY\_EG\_ff28\_0.90V\_125C\_2ey\_ss28\_0.90V\_m40C\_2ey\_7.0 DataBook
- C28SOI\_IO\_EXT\_ALLF\_CORESUPPLY\_EG\_ff28\_1.10V\_m40C\_tt28\_1.00V\_25C\_ss28\_0.90V\_125C\_7.0 DataBook
- C28SOI\_IO\_EXT\_ALLF\_CORESUPPLY\_EG\_ff28\_0.90V\_m40C\_2ey\_ss28\_0.90V\_125C\_2ey\_7.0 DataBook
- C28SOI\_IO\_EXT\_ALLF\_CORESUPPLY\_EG\_ff28\_1.10V\_125C\_ss28\_0.90V\_m40C\_7.0 DataBook
- C28SOI\_IO\_EXT\_ALLF\_CORESUPPLY\_EG User Manual
- C28SOI\_IO\_EXT\_ALLF\_CORESUPPLY\_EG HDL MODELS model usage guidelines

## 2. Changes with respect to all Previous Versions

### 2.1 Changes in Version 7.1 w.r.t Version 7.0

Final MAT10 Package aligned with latest BE

### 2.2 Changes in Version 7.0 w.r.t Version 6.0

7 new corners added

ff28\_1.30V\_125C

ff28\_1.30V\_m40C

ss28\_1.10V\_125C

ss28\_1.10V\_m40C

ss28\_1.15V\_125C

ss28\_1.15V\_m40C

tt28\_1.20V\_25C

A. 1 new cell ESDCLAMP\_1V0\_45U\_130U\_EXT added

B. This package contains Verilog, libs, Cadence LEF, SIP, SIGNOFF GDS, CDL and SYN-OPSYS LAYOUT, IODA, VOLTUS & FRAM.

(1) Verilog Models:

I. Verilog (.v) model : Compliance with power aware flow.

II. In VERILOG Pin name, Pin direction and functionality is aligned with Usermanual .

(2) Liberty NLDM (STF) :

I. STF view is compliance with UPF flow .

ESDCLAMP\_1V0\_45U\_130U\_EXT Cell addition

### 2.3 Version 6.0

A. This is the Final release.

B. This package contains Verilog, libs, Cadence LEF, SIP, SIGNOFF GDS, CDL and SYN-

**OPSYS LAYOUT & FRAM.****(1) Verilog Models:**

**I. Verilog (.v) model : Compliance with power aware flow.**

**II. In VERILOG Pin name, Pin direction and functionality is aligned with Usermanual .**

**(2) Liberty NLDM (STF) :**

**I. STF view is compliance with UPF flow .**

**BE First Release**

### 3. Known Problems and Solutions of this release



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**DRC errors**

- cell Level



**EMET ERRORS, Ignorable, can be corrected on chip level during EMET structure development**

EMET.DEN.1  
EMET.DEN.10  
EMET.DEN.11  
EMET.DEN.12  
EMET.DEN.2  
EMET.DEN.3  
EMET.DEN.4  
EMET.DEN.5  
EMET.DEN.6  
EMET.DEN.7  
EMET.DEN.8  
EMET.DEN.9



**Minimum Density Errors, Ignorable, can be corrected on chip level**

M6.DEN.1  
IA.DEN.1

**IB.DEN.1**  
**M6.DEN.8**  
**IA.DEN.8**  
**IB.DEN.8**

**For CORECELL\_B2B\_EXT M5.DEN.8.1**  
**- Internal IP DRC, cell smaller than DRC window**



**LVS errors**

**-cell level**  
**No error**



**ERC errors**

**ERC1a: Ignorable, can be corrected by defining the correct ground in lvs customization file**

## 4. Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (<http://col2.cro.st.com/helpdesk>).

Non-ST users, please contact the respective Customer Support.



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