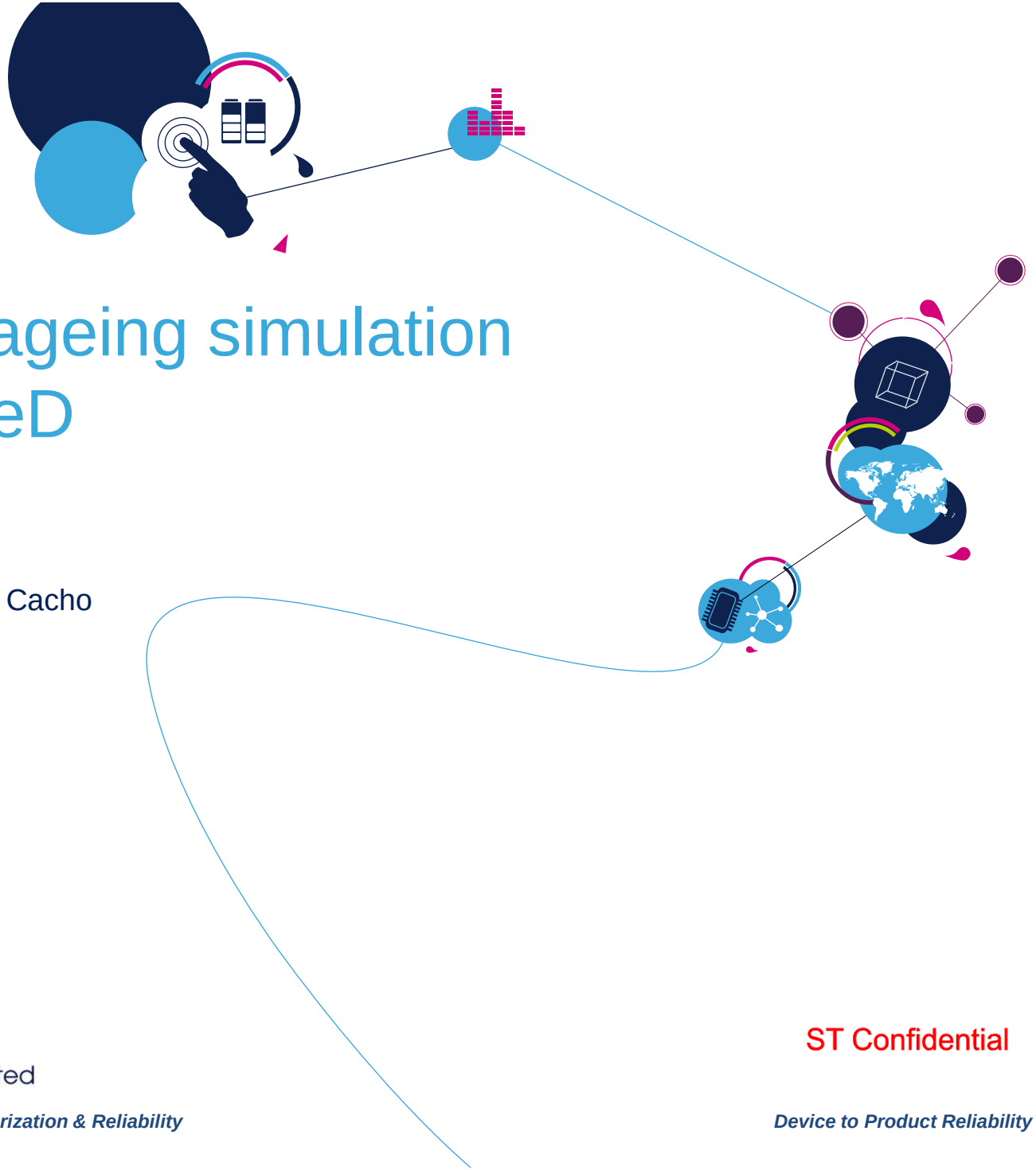

Tutorial for ageing simulation using WiCkeD

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life.augmented

TRD / STD / TPS / **Electrical Characterization & Reliability**

ST Confidential

Device to Product Reliability

Introduction

- MunEDA WiCkeD offers both, interactive design analysis and diagnosis tools and fully-automatic sizing and optimization tools. Both complement the designer in its familiar manual or tool-supported design flow.

- Configuration
  - WiCkeD release 6.6 and latest
  - UDRM code release 2.1 and latest
  - Package models DK2.3 and latest

- Reference documentation
  - /sw/muneda/wicked/6.7-p6.7-2/lnx86/wicked6.7/doc/

- Support
  - Helpdesk request

Introduction

- For the first time, sizing and optimization can be performed with reliability models only with eldo simulator

- Ceconfiguration.xml file provided in the Design Kit contains a section:
  - For reliability constraints:
    - script to extract eldo age measurements (agereport_measurements.tcl & readagereport.sh) are provided in the Design Kit ($DKITROOT/DATA/ELDO/CORNERS)

```
<ENTITYEXTRACTOR NAMECONVENTION="NETLIST" SIMULATOR="ELDO" IDENTIFIER="READAGEREPORT">
    <RUNSCRIPT FILE="readagereport.sh"/>
    <EXTRACTIONTEMPLATE FILE="agereport_measurements.tcl" NETLIST="NO"/>
  </ENTITYEXTRACTOR>
 </SIMULATIONENVIRONMENT>
```

  - For reliability rules:

```
 <ENTITYRULE SIMULATOR="ELDO" IDENTIFIER="Vth_deg" EXTRACTOR="READAGEREPORT" ANALYSIS="TRAN"
TYPE="INEQUALITY" DESCRIPTION="upper bound on Vth shift"> Vth_safetymargin %eachinstance%
    </ENTITYRULE>
      <ENTITYRULE SIMULATOR="ELDO" IDENTIFIER="mu0_deg" EXTRACTOR="READAGEREPORT" ANALYSIS="TRAN"
TYPE="INEQUALITY" DESCRIPTION="upper bound on mobility degradation"> mu0_safetymargin %eachinstance%
    </ENTITYRULE>
      <ENTITYRULE SIMULATOR="ELDO" IDENTIFIER="FIT" EXTRACTOR="READAGEREPORT" ANALYSIS="TRAN"
TYPE="INEQUALITY" DESCRIPTION="upper bound on FIT"> FIT_safetymargin %eachinstance%
    </ENTITYRULE>
```

Flow description

- Before launching wicked, define a reliability analysis in your netlist (.age command)
  - In Standalone:
    - For the detailed syntax, please refer to eldo documentation:
      - Eldo Reference Manual: Simulator Commands Chapter 3 => .AGE
    - First use the **mode=save** to perform a normal aged simulation and save the stress values at the end of the process in a file
    - Add a **.ALTER** command in your netlist and use the **mode=load** of age command to load the stress values previously saved in a file in order to perform a single simulation
  - In Cadence environment, you can define your reliability analysis in ADE L through the “Setup Corners” window, by clicking on “Reliability” tab. The ageing analysis will be saved in a *age_commands* file

Flow description

eldo template netlist for ageing analysis with Wicked

- Example of eldo netlist
  - In this example, stress is performed in .tran and characterization in .dc
  - A performance must be extracted in .aex

```
**** Template of netlist

.option aex
.include models
.include Mynetlist

*** temperature of stress
.temp 125
*** temperature of characterization
.param Tcharac=25

.age
+ tage=2 tunit=y hci=1 bti=1 tddb=1
+ tstart=0n
+ tstop=10n
+ nbrun=1
+ log
+ mode=save AGELIB = stress.lib  ASCII
+ ageall
+ agedsim=NO
+ compute_last=NO
+ plot=ALL
+ circuit_report=1
+ area_scaling=1

XCKT 1 2 3 4 5 6 Mysubckt

*** source
Vb 1 0 PWL( 0 1.155 1e-08 1.155 )
…

.TRAN 1p 10n
.DC

.alter
```

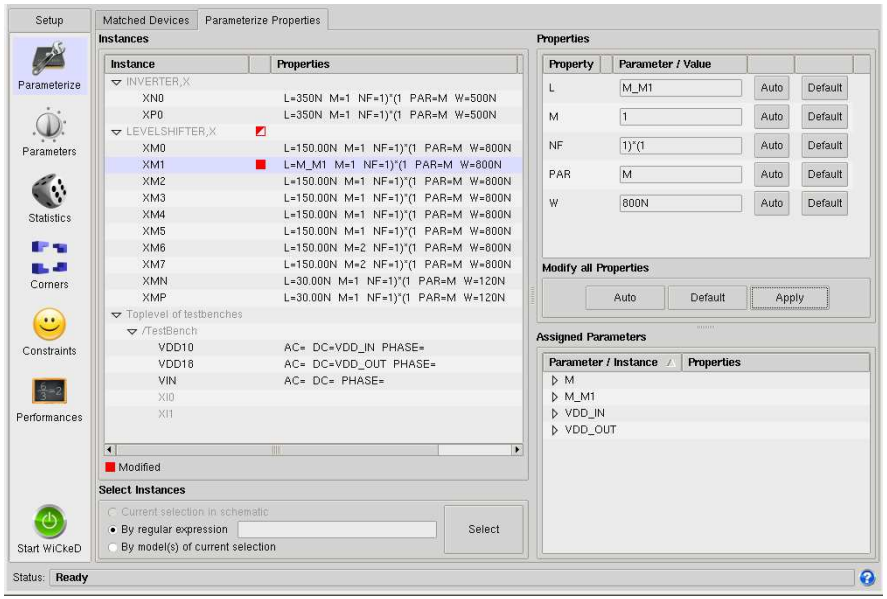
Cont’

```
.age
+ tage=2
+ tunit=y
+ hci=1
+ bti=1
+ tddb=1
+ nbrun=1
+ log
+ mode=load AGELIB = stress.lib  ASCII
+ ageall
+ agedsim=NO
+ compute_last=NO
+ plot=ALL
+ area_scaling=1

* START SOURCES
Va 3 0 DC 0
Vb 1 0 DC 0.05
…

.DC Va 0 1 0.01
.PRINT DC I(VDGROUND)
.PLOT DC I(VDGROUND)

.temp Tchar

.DEFWAVE dc perf=abs(I(Vd))
.extract dc label=Myperfo yval(w(perf),1)

.END
```

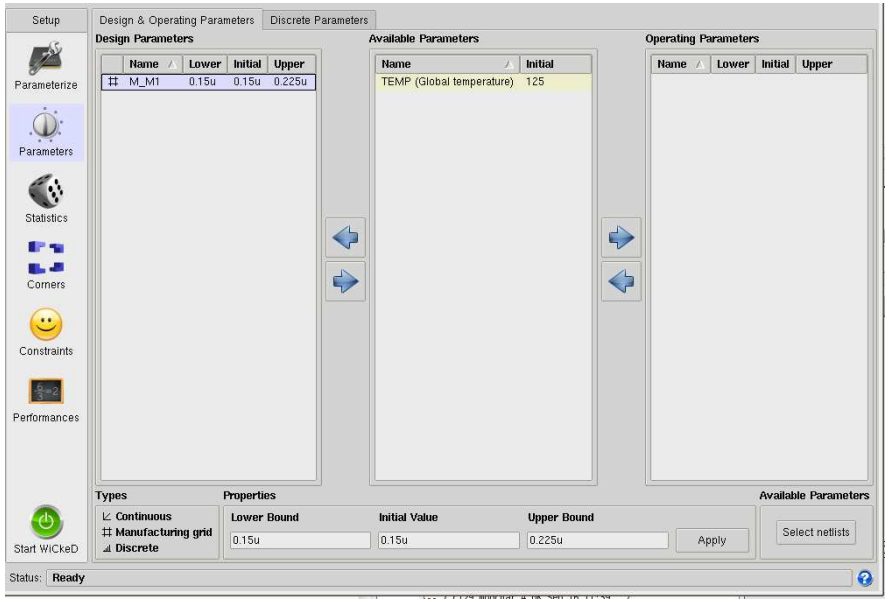
Flow description

- Flow constraint editor flow
  - Import your netlist
  - Parameterize (A)
  - Parameters (B)

(A)



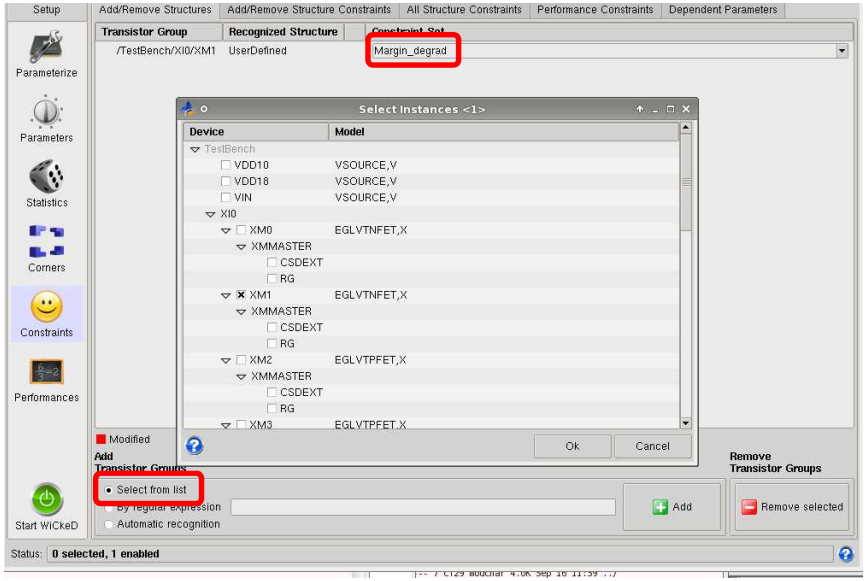
(B)



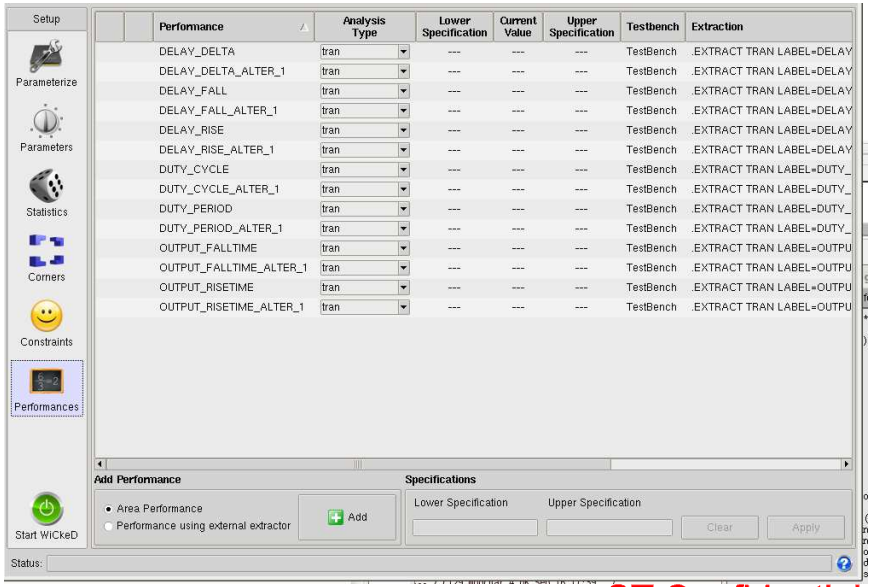
Flow description

- Flow constraint editor flow
  - Statistics: **disable mismatch & global variations**
  - Corners: **‘no corners’ methods**
  - Constraints (C): **click on Select from list (choice your devices) then select Margin_degrad constraints in Constraint Set tab**
  - Performances (D)

(C)



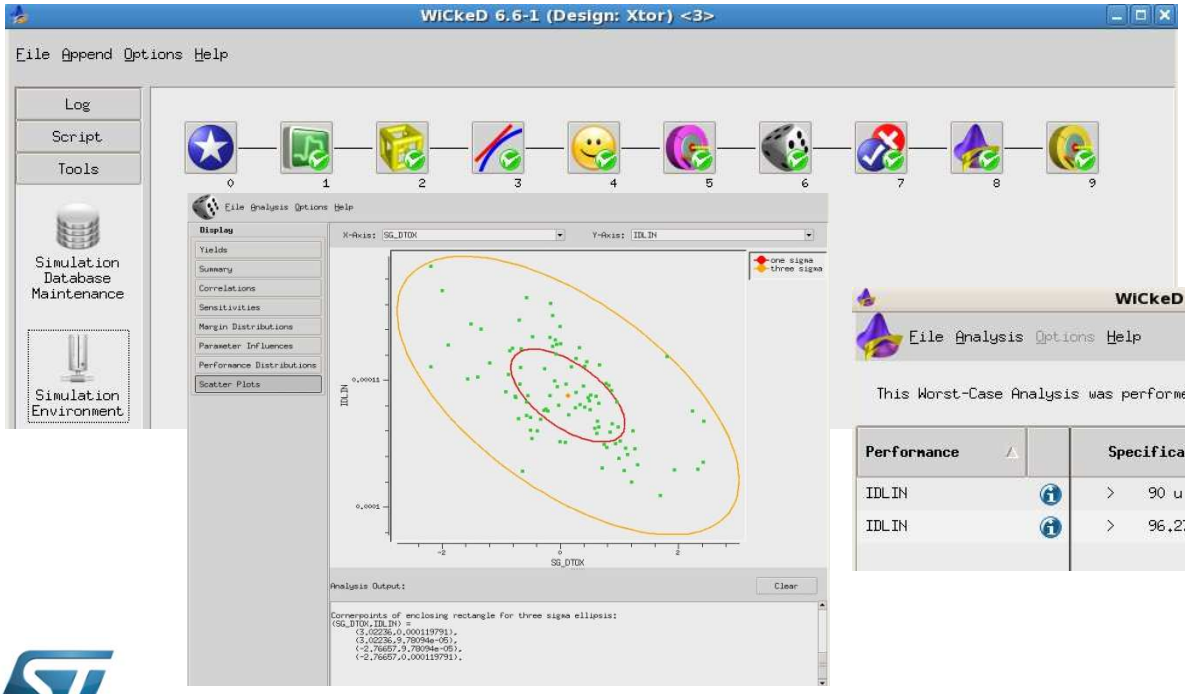
(D)

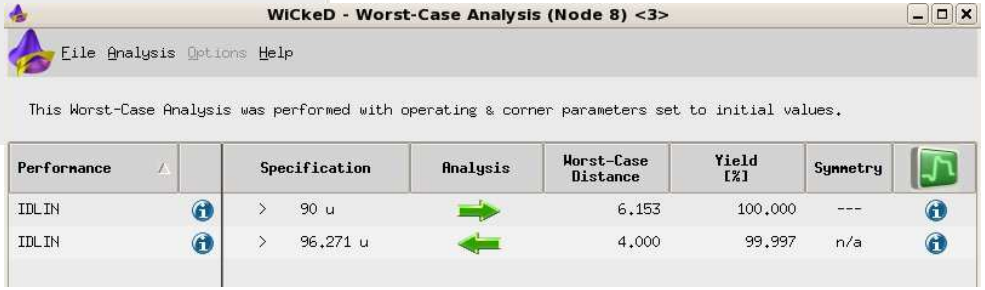


Flow description

- Flow
  - Parameterize (A)
  - Parameters (B)
  - Statistics: disable mismatch & global variations
  - Corners: ‘no corners’ methods
  - Constraints (C)
  - Performances (D)
  - Analyses and sizing/optimization (D)

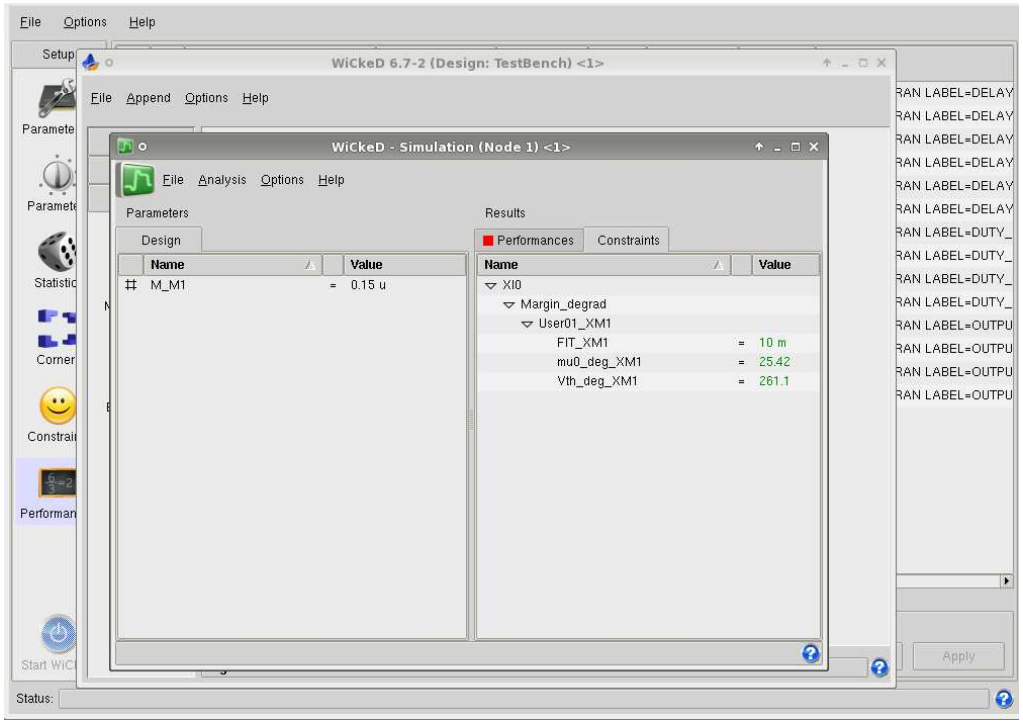
- Results
  - Sensitivity analysis
  - Feasibility optimization
  - Deterministic Optimization
  - Monte Carlo Analysis
  - Worst Case Analysis
  - Yield Optimization
  - ……





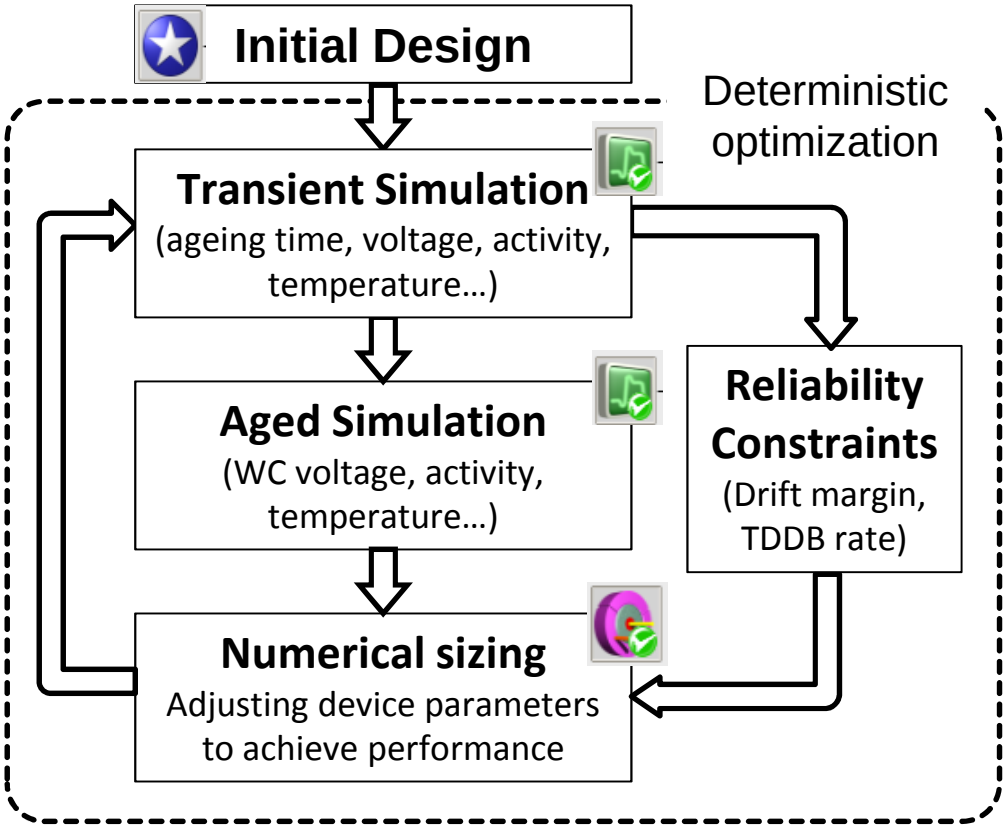
Results

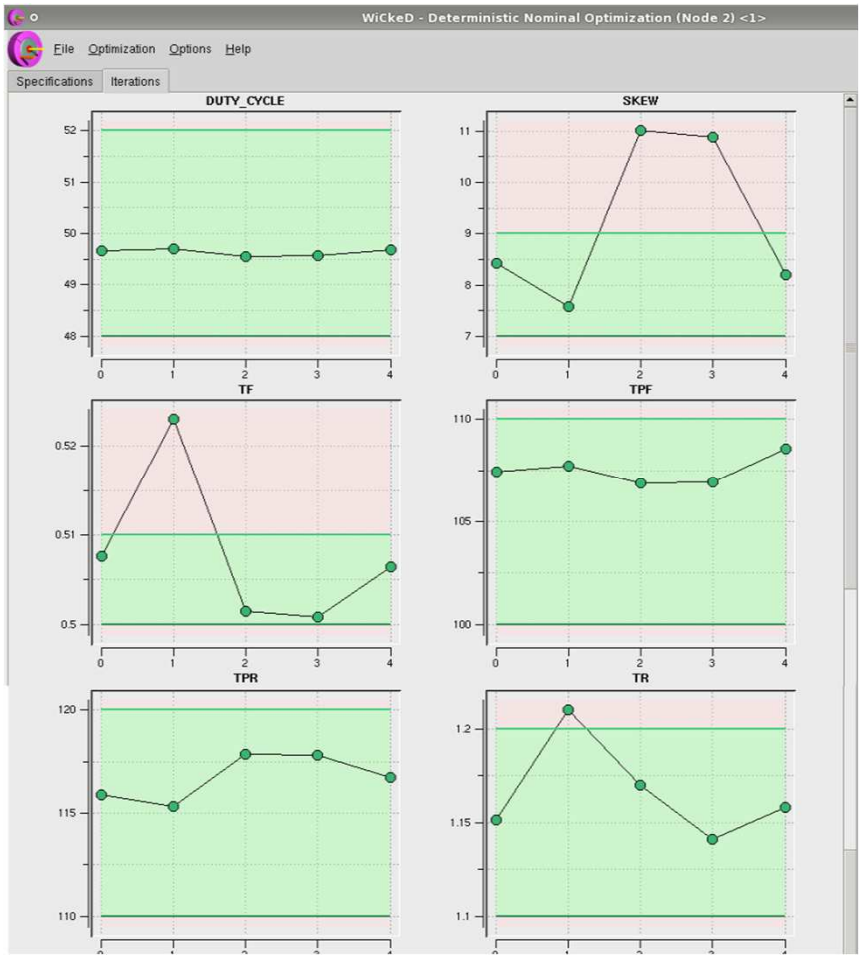
- Simulation
  - Visualization of reliability constraints



Results

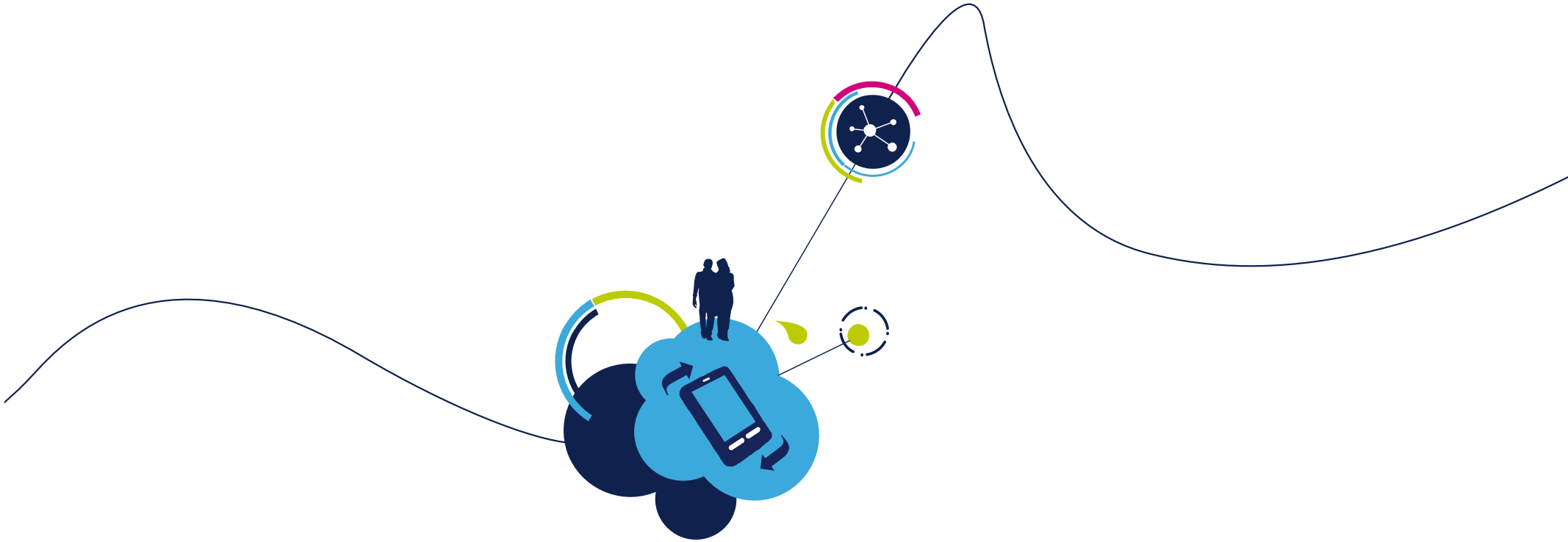
- Sizing under reliability constraints
  - Adjusting device parameters to achieve IP performances and Reliability
  - Automated sizing loop with optimal performance/reliability trade-off





JEDEC references

- JEDEC JEP122F: Failure Mechanisms and Models for Semiconductor Devices.
- JEDEC JEP143B.01: Solid State Reliability Assessment and Qualification Methodologies.
- JEDEC JEP148A: Reliability Qualification of Semiconductor Devices based on Physics of Failure Risk and Opportunity Assessment.
- JEDEC/FSA Joint Publication JP001-01: Foundry Process Qualification Guidelines.



End of report