C28SOI_IO_ALLF_FRAMEKIT_EG User's Manual

Includes leafcells needed for all frames designed in 28 nm FDSOI technology

Overview

The C28SOI_IO_ALLF_FRAMEKIT_EG library contains leafcells in all frames and is mandatory for any 28nm FDSOI IO library.

Features

- Supports compatible standard digital frame (CSF), 3V3 standard digital frame (3V3SF) and analog frame (ANAF).
- FC (Flip-chip), CL (Cluster) and 2ROWS frames provided.

Applications

- Serves as a reference library for all other 28 nm FDSOI IO libraries.

Information Snapshot

Process Options

- GO1: SVT
- GO2: 28 Å

Packaging

- Flip-chip

Table 1 : Operating Values

Symbol	Parameter	Frame	Min	Typ	Max	Unit
vdd	Core supply voltage	-	*	1.0	1.1	V
vdde	Pad supply voltage	ANA	*	1.0	1.1	V
		CSF ANA	*	1.8	1.95	
		ANA 3V3SF	*	3.3	3.6	
$T_{junction}$	Operating junction temperature	-	- 40	25	125	°C

* As per Design Platform specification

For more details about electrical specifications, please refer *Section 3: Electrical Specifications*.

1. Quick References

The document uses the following convention to indicate logic levels:

L indicates logic low.
H indicates logic high.
X indicates don't care state.
Z indicates high impedance state.
'-' (Hyphen) indicates 'No activity'.

** suffixed in library name indicates multiple metallization options.*
*** suffixed in cell name indicates multiple packages / configurations.*

1.1 Metal Stacking Convention

The metallization option supported by this library can be referred from its product package. The following is the convention that can be used to decode the segment in the library name:

- 7 metal option (5U1X2T8XLB) known as 5002 refers as follows:
  - 5U1X refers to the first 5 levels with 1X pitch (thin) metal.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 8 metal option (6U1X2T8XLB) known as 6002 refers as follows:
  - 6U1X refers to the first 6 levels with 1X pitch (thin) metal in ultra-low K.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 10 metal option (6U1X2U2X2T8XLB) known as 6202 refers as follows:
  - 6U1X refers to the first 6 levels with 1x pitch (thin) metal in ultra-low K.
  - 2U2X refers to the next 2 levels with 2x pitch (thin) metal in ultra-low K.
  - 2T8X refers to 2 levels with 8x (thick) metal in oxide.
  - LB is the Alucap.

1.2 Reference Documentation

The following documents can be used for further study:

- CMOS028 FDSOI DRM.

1.3 Reference library

The C28SOI_IO_ALLF_FRAMEKIT_EG library doesn't refer to any cell from other 28nm FDSOI libraries in the offer, it is the reference library.

1.4 Acronyms and Abbreviations Used

Table 2 : Acronyms and Abbreviations

Acronym/Abbreviation	Description
B2B	Back-to-Back
CDM	Charge Device Model
DRM	Design Rule Manual
ESD	Electrostatic Discharge
HBM	Human Body Model
FC	Flip-chip
CL	Cluster
MM	Machine Model
SVT	Standard V_T
2ROWS	Two rows

2. Functional Specifications

2.1 IO Frames

The C28SOI_IO_ALLF_FRAMEKIT_EG library contains the development kit for IO frames. It allows the generation of following:

- Compatible standard frame (CSF): It is the layout framework of 1.8 V families of digital IOs.
- 3V3 standard frame (3V3SF): It is the layout framework of 3.3 V families of digital standard IOs.
- ANA frame (ANAF): It is the layout framework of all 1.0V, 1.8 V and 3.3 V families of analog IOs.

The assumptions for the metal configurations are:

- All the metal layers are used in the IO frame:
  - Metal1 to metal4 are used for internal IO routing.
  - Metal5 and upper metals are used for bus/power rails.
- The top metal is allocated for vertical and flip-chip connections.

2.2 IO Pads

Flip-chip and cluster views are provided by the C28SOI_IO_ALLF_FRAMEKIT_EG library. The routing grid measures 0.1 µm in ‘X’ and ‘Y’ direction.

2.3 Floor plan

The different available areas for different frames provided by the library are given in the table below

Table 3 : Available area for different supported frames

Frame	Parameter	Width (µm)	Height (µm)	Area (µm)^2
CSF frame (40um width)	ESD area	38.5	18.668	718.71
	Active free area	38.79	69.604	2699.93
3V3SF (40um width)	ESD area	37.5	17.224	645.90
	Active free area	37.5	71.354	2675.77
ANAF (40um width)	ESD area	NA	NA	NA
	Active free area	37.5	79.257	2972.13

3. Electrical Specifications

3.1 ESD and Latch-up Characteristics

The ESD network is designed and simulated to withstand the following levels under worst-case process conditions.

Table 4 : ESD and Latch-up Characteristics

Symbol	Parameter	Conditions	Target	Unit
V_{ESD}	Electrostatic discharge voltage	Human Body Model (HBM) [1]	2000	V
		Machine Model (MM) [1]	100	V
		Charge Device Model (CDM) [1]	500V JEDEC	V
$I_{latch-up}$	Injection current	Maximum operating junction temperature 125 °C [2]	100	mA
	Over-voltage stress		1.5 * vdde	V

[1] ESD qualification: according to Electrostatic Discharge Sensitivity Measurement

[2] Latch-up qualification: according to Latch-up Sensitivity Measurement

The level of CDM current seen at a given pre-charge voltage varies significantly with the chip size and package type. For instance, larger dies/packages generates higher CDM current.

However, this package size dependence has been considered during IO qualification, so that the above CDM commitment remains valid for any die/package size (even for large die/package sizes of hundreds of mm^2).

4. Contact Information

ST users, login to **HELPDESK**. (http://col2.cro.st.com/helpdesk) for submitting queries or support requests.

Non-ST users, contact Customer Support personnel.

Appendix A: Document Revision History

Table 5 : Document Revision History

Date	Document Version	Comments
08-February-2016	1.6	• Improved header • Table1: max voltage added • Table 2 “acronyms and abbreviations” completed • **T**able 4 “ESD and Latch-up Characteristics” improved
18-September-2014	1.5	• Alignment with new template
18-July-2014	1.4	• CSF frame addition • Electrical specifications updated (table 1 and 4)
07-March-2014	1.3	• Electrical specification section updated • Confidentiality note added
02-May-2013	1.2	• 3V3SF Frame addition
12-Dec-2012	1.1	• Ported to the new template
16-May-2012	1.0	• First release

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