

Analog Flow PDK 28FDSOI

M1. Schematic and Simulation

FD-SOI



life.augmented

Company Confidential

CMOS & Derivative PDK



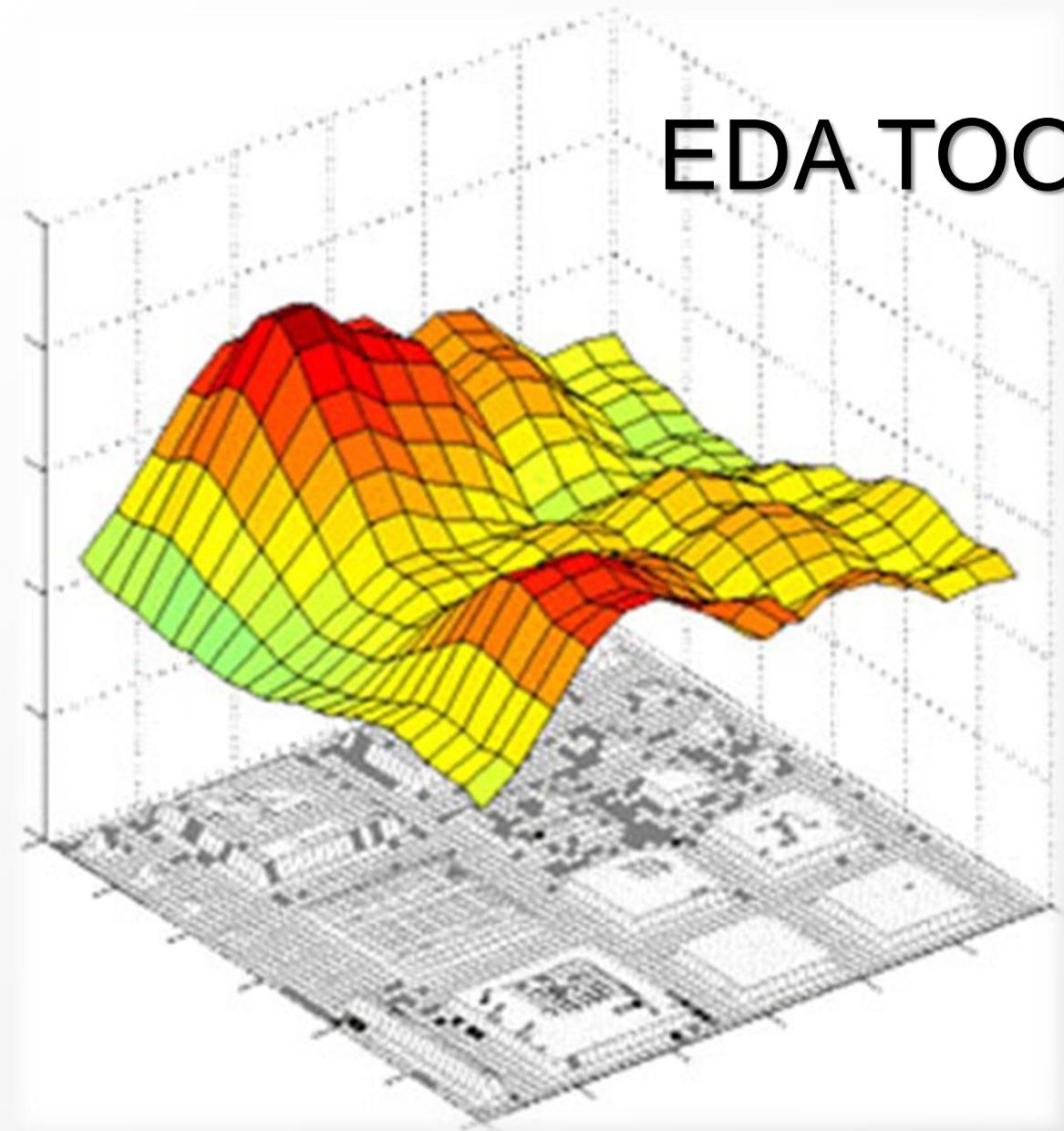
- Identify the key concept of simulation
- Identify the simulation flow
- Configure the CAD tools



AGENDA



EDA TOOLS & MODELS



PART I

CMOS & Derivative PDK

Model Information

EDA Tools &
Models



Technology
Variation
Modeling

Simulation
Flow

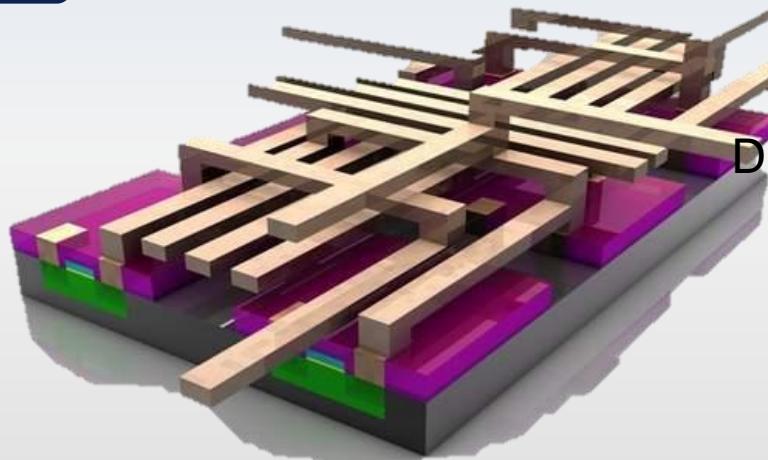
Extra-Tools

Devices
Documentation

UTSOI2

Ultra Thin Fully Depleted SOI MOSFET Model

fully integrated in Eldo (LEVEL 80), XA(-eldo & -hspice),
Hspice (LEVEL 76), Spectre (model name is utsoi)



2.1 (VerilogA code version 2.1)

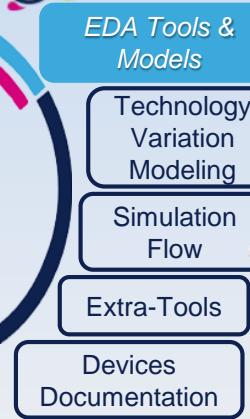
utsoimod

4 (external) + 1 facultative thermal node

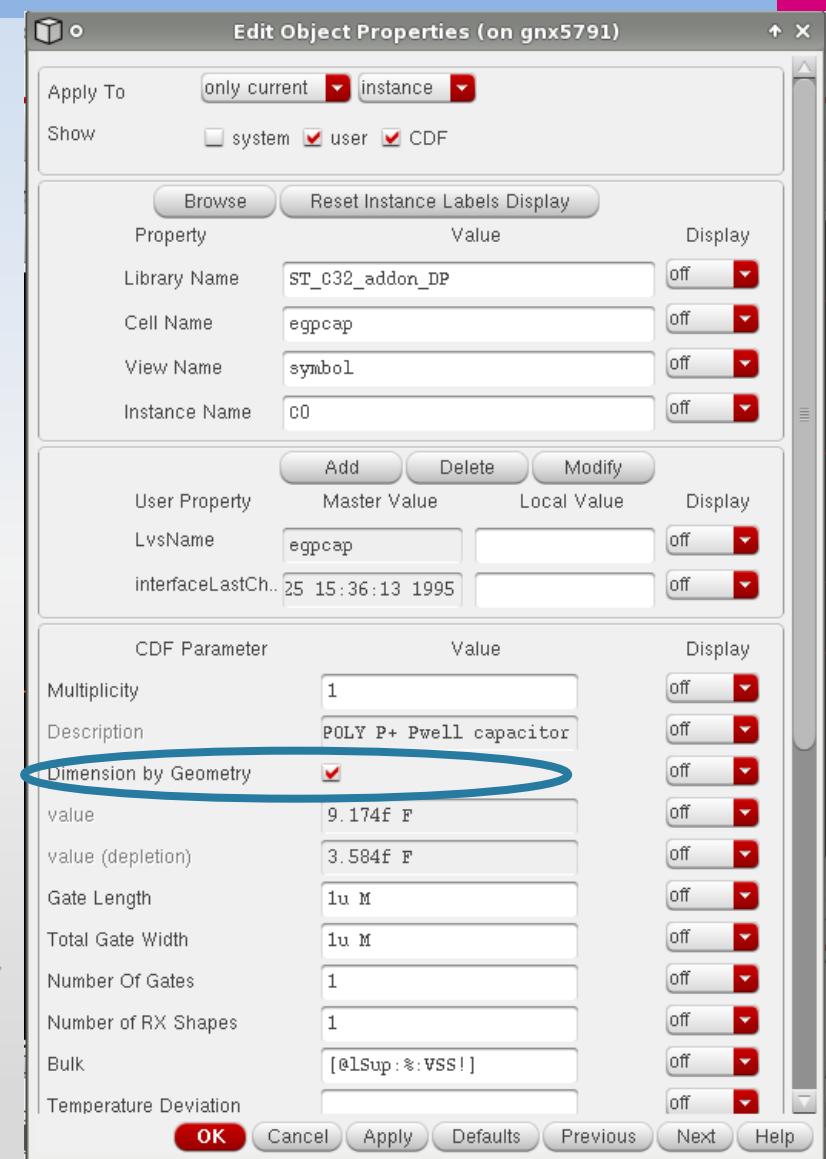


- The Length Unit in CMOS28FDSOI is the **meter**
- Model / Device in cmos32lp cadence library :
 - The name of the model is the name of the device
- No user Model in the CDF of the components :
 - Create your own symbol or create a new library with a model with the same name as one existing in the DK and select the new library in the Setup Corners form

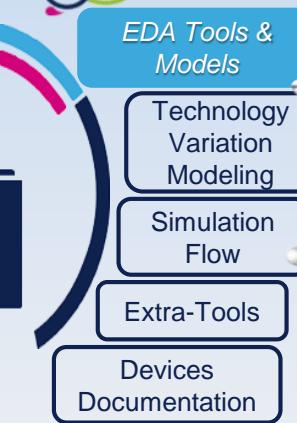
Geom vs Elec : resistors & capacitors



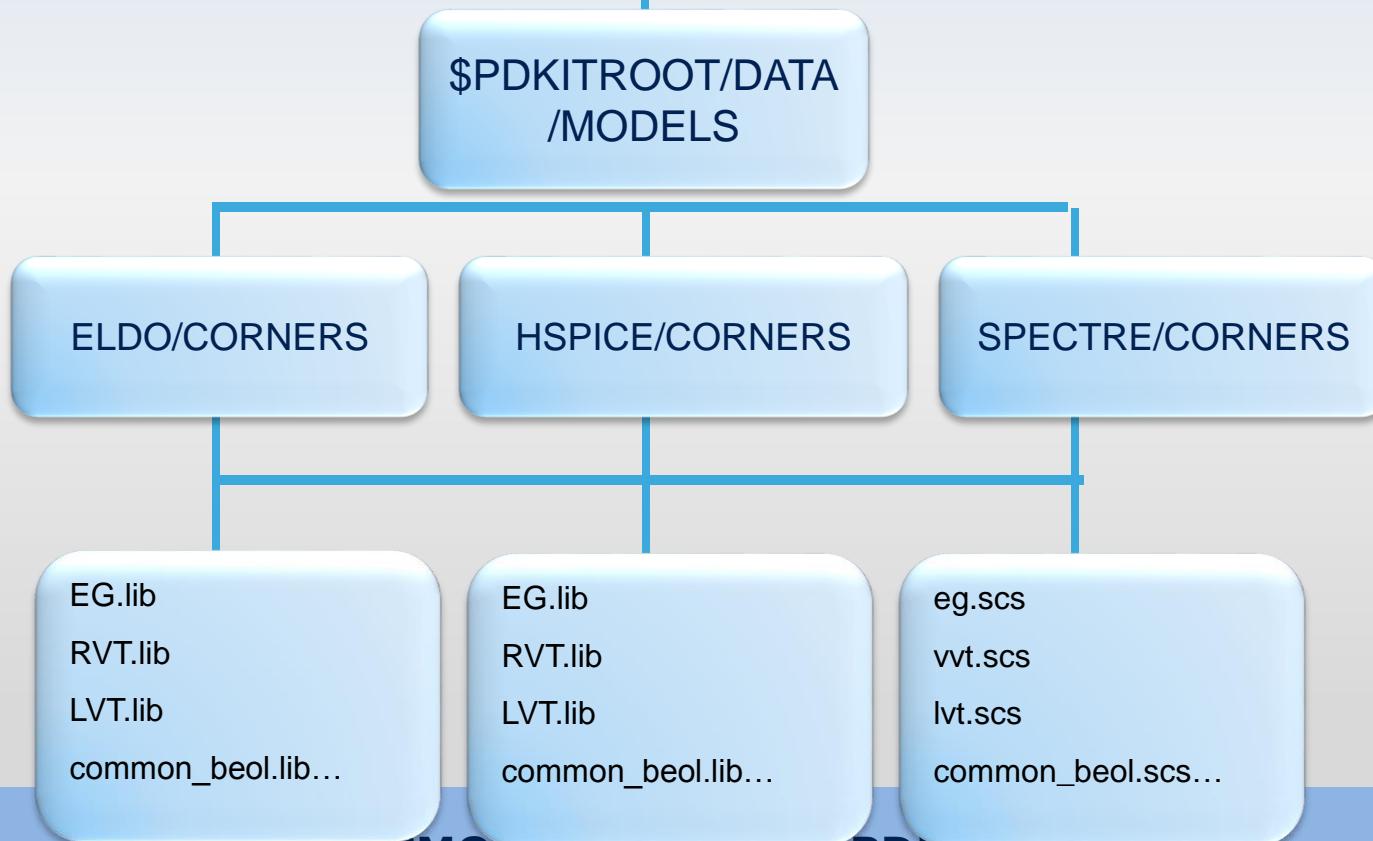
- Geometrical parameters (W , L) are used for netlisting (instead of Electrical R , C)
- This description is closer to the technology, more realistic
- You can:
 - Recalculate the Resistor Geometry
 - the aim is to change the value of the body resistance. W and L will be recalculated.
 - Recalculate the Resistor Value
 - the aim is to change the geometry (w and/or l). R_{body} will be recalculated.



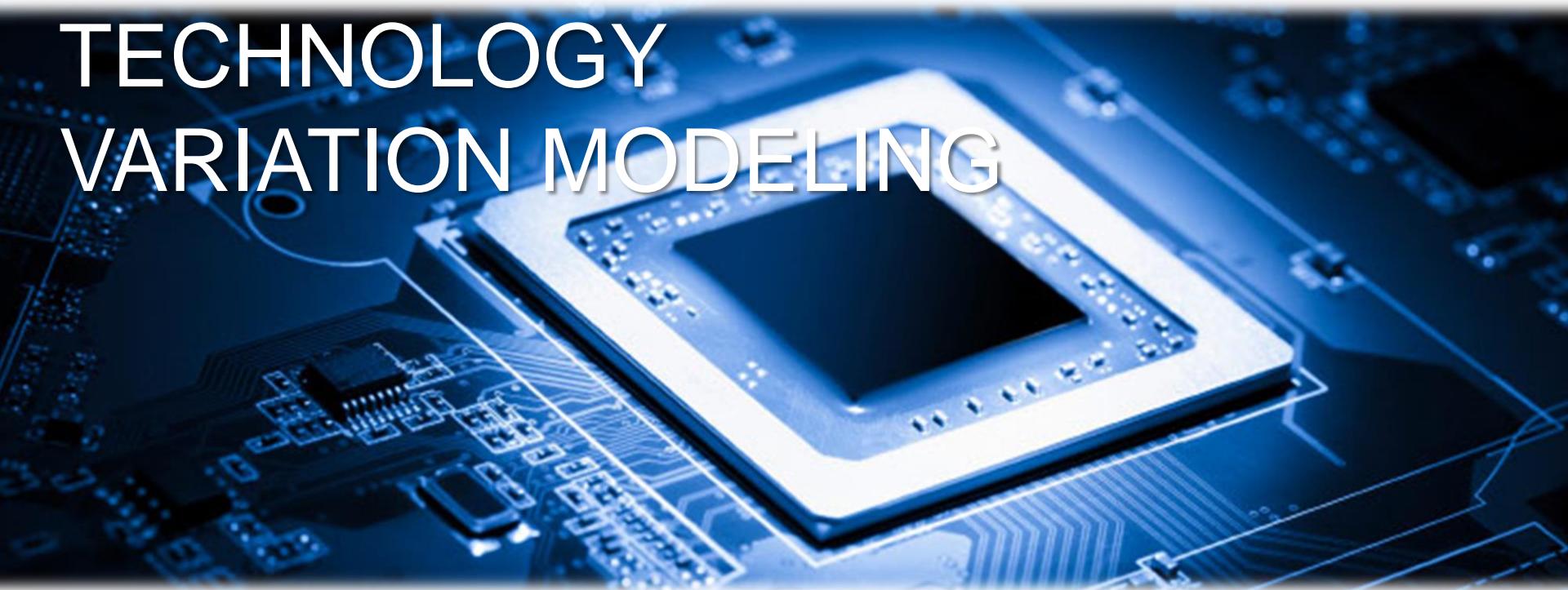
Library Files in the Design Kit



- one sub-product per simulator
- one Library File per component type or family
- some Skill files to drive *Analog Artist* interface



TECHNOLOGY VARIATION MODELING

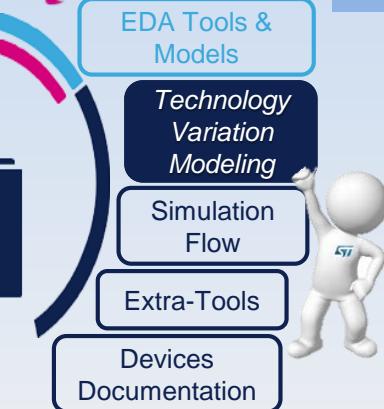


Technology variations description

PART II

CMOS & Derivative PDK

Technology Variations description

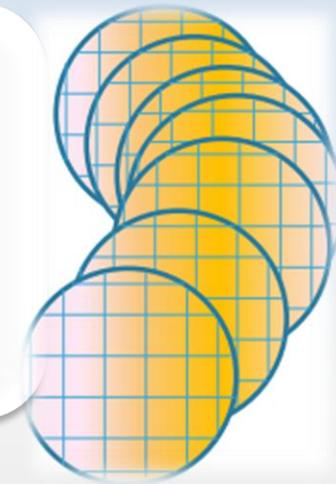


Two ways to modelize variations

Global

affect all the devices of the chip in the same way due to process variability

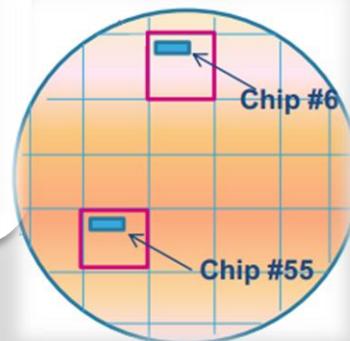
Ex: poly and active CD dimension due to etching



Local

which vary from one device to another and cause mismatch between identical devices.

Ex: sheet resistances for resistors



Technology Variations description: Global variation

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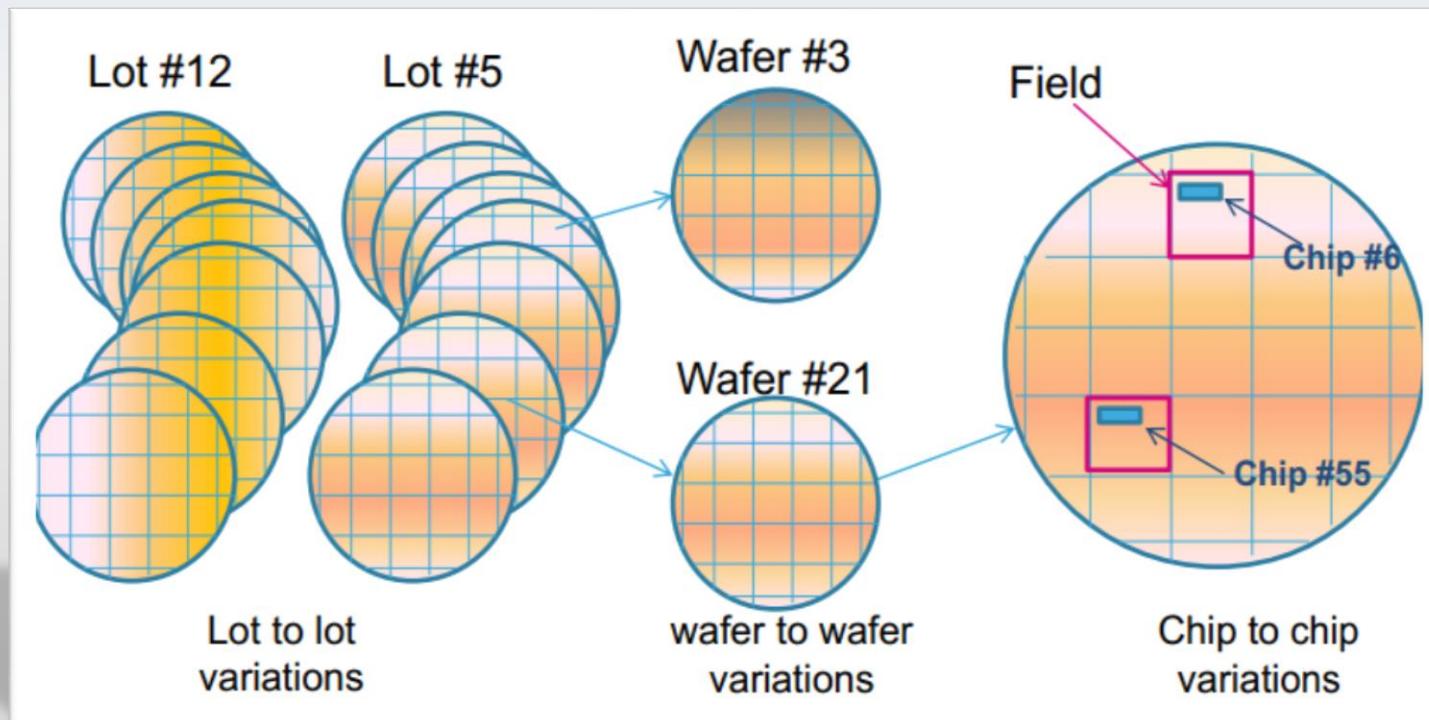
Model accounts for these variations:

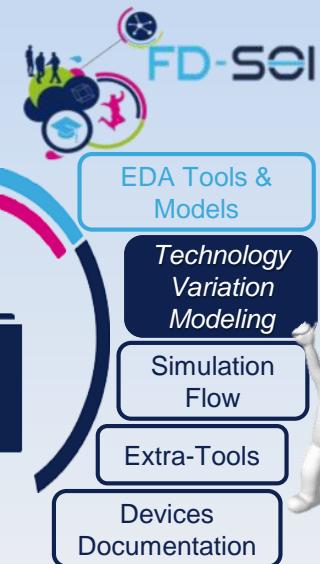
Pre-Defined Corners (SS, FF, SSF, FFF...)

Monte-Carlo simulations (Statmotherfab)

User Defined Corners (USER)

Correlations between devices parameters





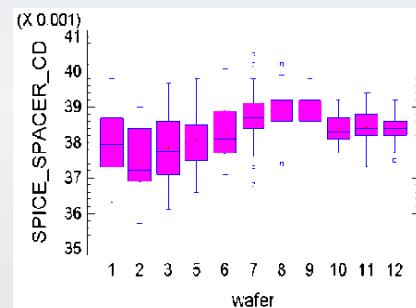
Technology Variations description: Global variation

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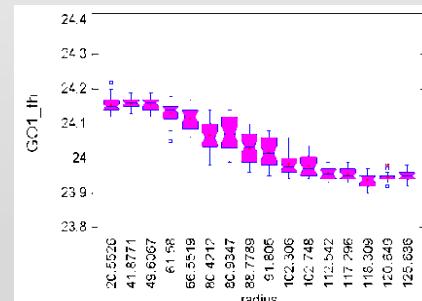
• Origins

- Different equipment between fabs
- Temperature control in 25 wafers foops
- Center-edge effect of the CMP

Wafer to wafer



Die to die (intrawafer)



- All devices on a die are supposed to be exposed to the same process variation

- Controlled by process in a given range

- Model accounts for these variations:

- Pre-Defined Corners (SSF, FFF...)
- Monte-Carlo simulations (stat)

Technology Variations description: Global variation

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The variations of each Global Parameter may impact several devices
Ex: nmos transistor and P+/Pwell capacitor

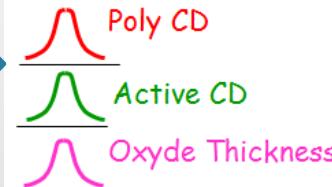
$$I_{on} \propto \frac{U_0 \cdot \epsilon}{T_{ox} + \Delta T_{ox}} \frac{W + \Delta W}{L + \Delta L} f(V_{th})$$

$$Cap \propto \frac{\epsilon}{T_{ox} + \Delta T_{ox}} (W + \Delta W) (L + \Delta L) g(V_{fb})$$

Global variations can be split in 2 categories

Common

Common Variations



Specific

Specific Variations



Not for 28FDSOI MOSFETs

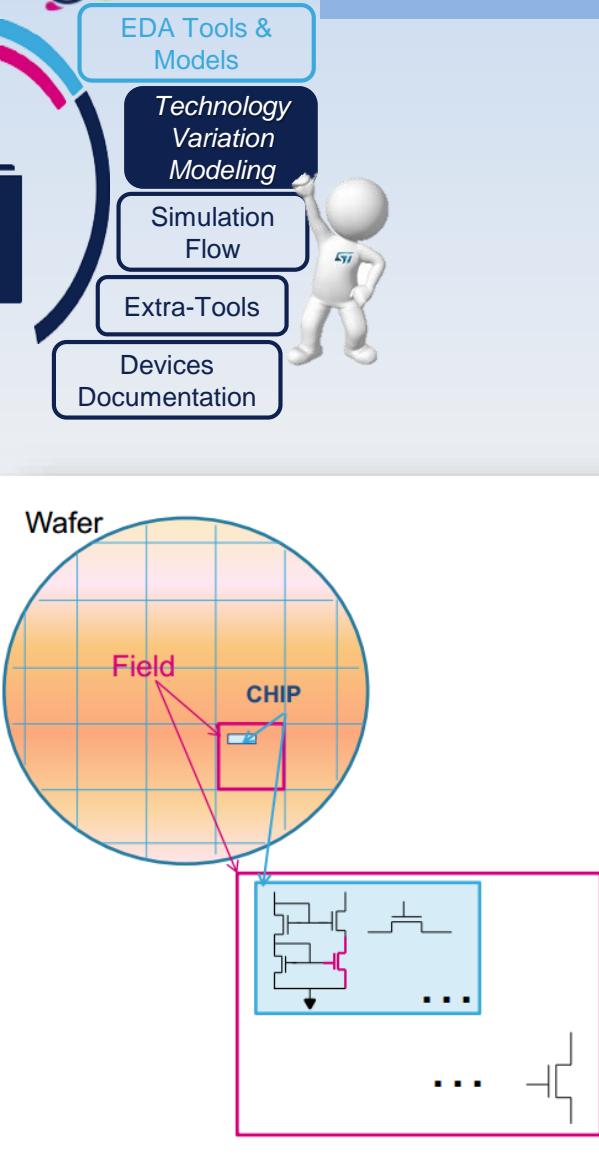
correlated with other devices

- Definition of a set of parameters which impact several different devices like poly CD variation (both impacted nmos and pmos)
- Prevent unphysical simulation such as max CD for nmos and min for pmos

Not correlated to other devices

- Defined in the model of the device

Technology Variations description: Local variation

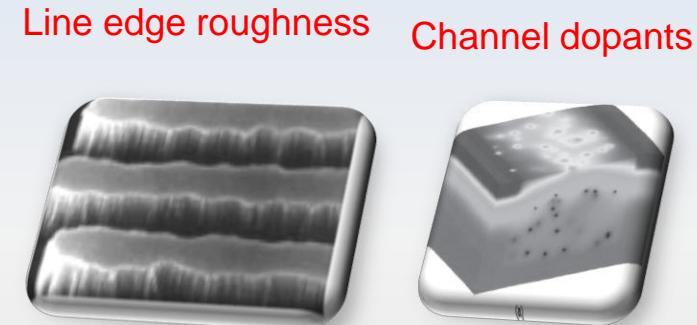


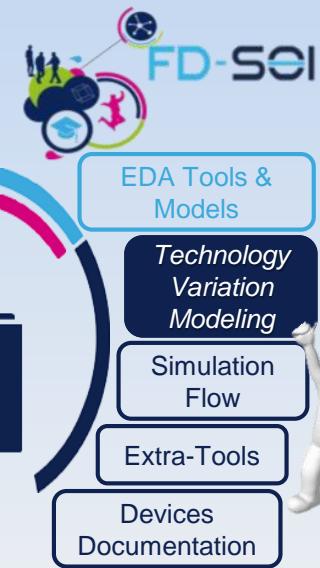
- Also called stochastic, random, mismatch

- Origins
 - Channel dopants
 - Line edge roughness

- Can not be controlled

- Affect adjacent devices
 - No correlations between device parameters
 - Mismatch estimation through Monte Carlo simulation





Mismatch control flags features

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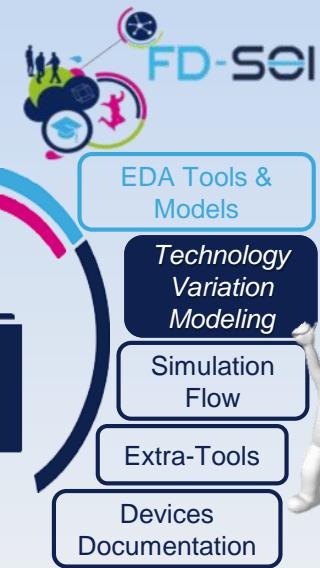
- Flags have been introduced to describe the mismatch at the device level. One flag is defined for each family of devices (lvt / rvt / cmom / rpolyp ...).
- Technically, once activated (flag = 1) , internal parameters of the model card will be randomly selected on a gaussian curve centered on the predefined corner for each device → local mismatch will be observed.

TECHNOLOGY VARIATION MODELING

Technology variations modeling

PART II

CMOS & Derivative PDK



Technology Variation Modelling

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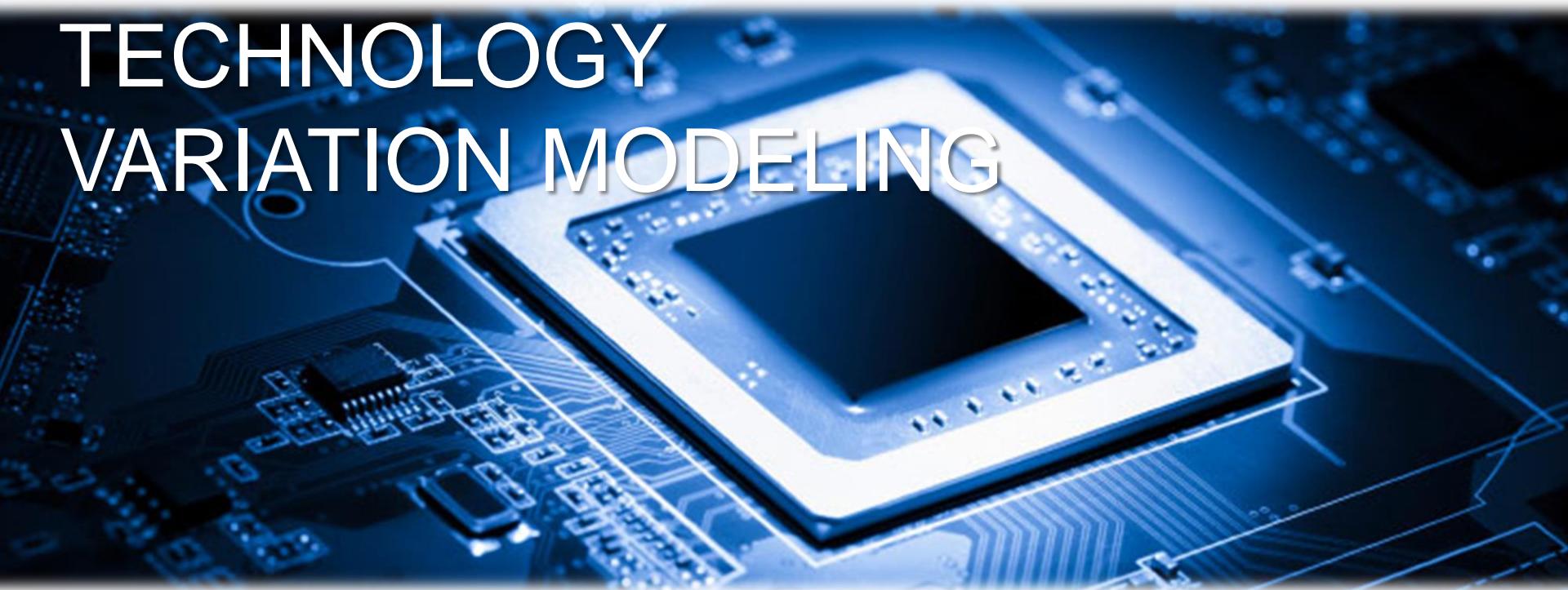
We have 2 methodologies to model the global technology variations:

Pre-Defined Corners (PDC)
Statistical variations
User Corners

Mismatch effects modelling

**defined in the model card & can be added to global variations
whatever the methodology used (statistical, user defined, PDC)**

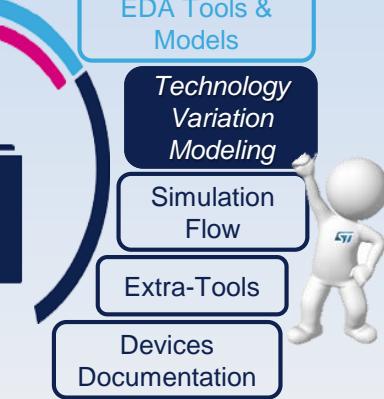
TECHNOLOGY VARIATION MODELING



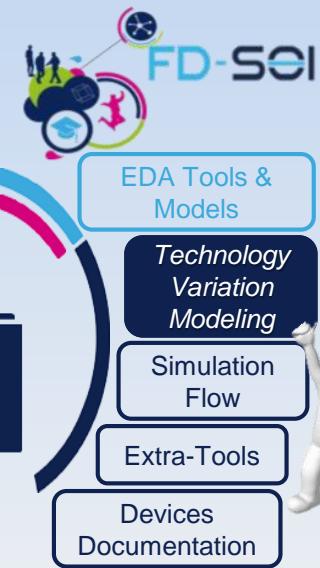
- *Technology Variation Modeling*
 - *Predefined Corners*

PART II

CMOS & Derivative PDK



- Passive devices: "worst" and "best" case definition is easy
 - For the capacitors, extreme values are the maximum of Capacitance (CMAX) and the minimum of capacitance (CMIN),
 - For the resistors, RMAX and RMIN are the extreme cases
- MOS transistors: "worst" and "best" case definition is more tricky
 - Several characteristics could have been selected: Speed, GM, Rds, Noise, ...
- The circuit performances covered by the PDC are mainly digital oriented
 - Pre-defined corners (PDC) are created to reach worst and best cases for:
 - The circuit speed performances (FF, SS corners)
 - The ION(NMOS)/ION(PMOS) ratio (SF, FS corners)
 - Corners are SLOW or FAST, including NMOS then PMOS
 - Ex: FF: NMOS fast, PMOS fast
 - Ex: SF: NMOS slow, PMOS fast
 - Pre-defined corners are not adapted to any circuit
- Depending on the considered performance, the number of sigma of the model parameter is defined and fixed



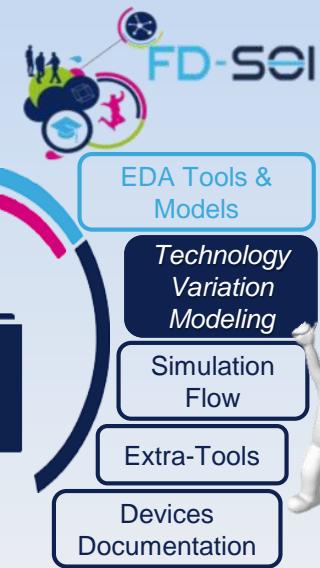
Technology Variations Modelling: MOS fast and slow corners

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- The identified device characteristic for the MOS is the drain current

$$I_{ds} = \mu \frac{\epsilon_{ox}}{T_{ox}} \frac{W - \Delta W}{L - \Delta L} (V_{GS} - V_{th} - \dots) V_{DS}$$

- To maximize drain current (FAST corner), one has to
 - Increase μ , ΔW
 - Reduce V_{th} , ΔL and T_{ox}
- To minimize drain current (SLOW corner), one has to
 - Reduce μ , ΔW
 - Increase V_{th} , ΔL and T_{ox}



Technology Variations Modelling: MOS pre-defined corners construction

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- Process Parameters (P) Variations are expressed as a Deviation (D) reflecting a shift versus the typical (T) value

$$P = T + D$$

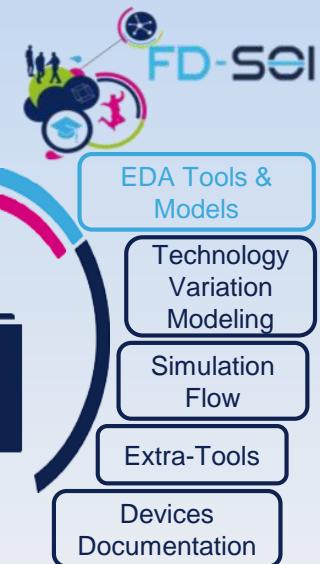
- Typical (or Nominal) Corners: TT, typ no deviation
- Pre-Defined Corners (PDC): FF, FS,...,rmax, cmin,...

Deviation is set by the modelling engineer to optimize device performances (speed for fet, resistance or capacitance value, Veb/Beta for bipolar,...)

$$P = T + (N\sigma)$$

- Statistical Corners: The deviation is defined by a statistical distribution

$$P = T + \text{gauss}(0, \sigma)$$



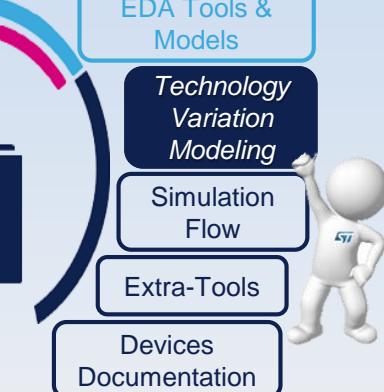
MOSFETs variation modeling

- Global variations are set with `common_fet` and `common_feol` section
- Local variations are set thanks to `<family>_dev` flag
 - `<family>_dev=0`: no local variations
 - `<family>_dev=1`: local variations in MC simulations
 - `<family>_dev=2*`: local variations in corners (*for Wafer Acceptance Criteria only*)
 - `<family>_dev=3*`: user-defined local variations
- See next slides for netlist examples
 - Note: usage of **USER defined variations** is not described here.
 - The attendance to a dedicated training on this purpose is recommended.

	Definition	Corner/ <code><family>_dev</code>	
MonteCarlo (MC)	MC, global + local	statmotherfab	1
	MC, global only	statmotherfab	0
Performance corners	timing, global + local (<i>on given R. O.</i>)	SS/FF	2
	timing, global only	SS/FF	0
Functional corners	device, global + local	SSF/FFF/SF/FS	2
	device, global only	SSF/FFF/SF/FS	0

Note: Functional corners (F) are copied into historical (A) corners: FSA=FS, SFA=SF, FFA=FFF, SSA=SSF

*`family_dev=2` and `3` are not supported for `_acc`, `_rf` and `_rfseg` models



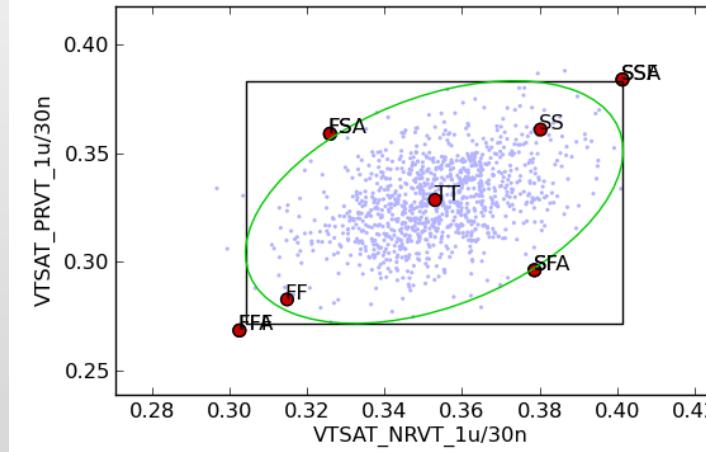
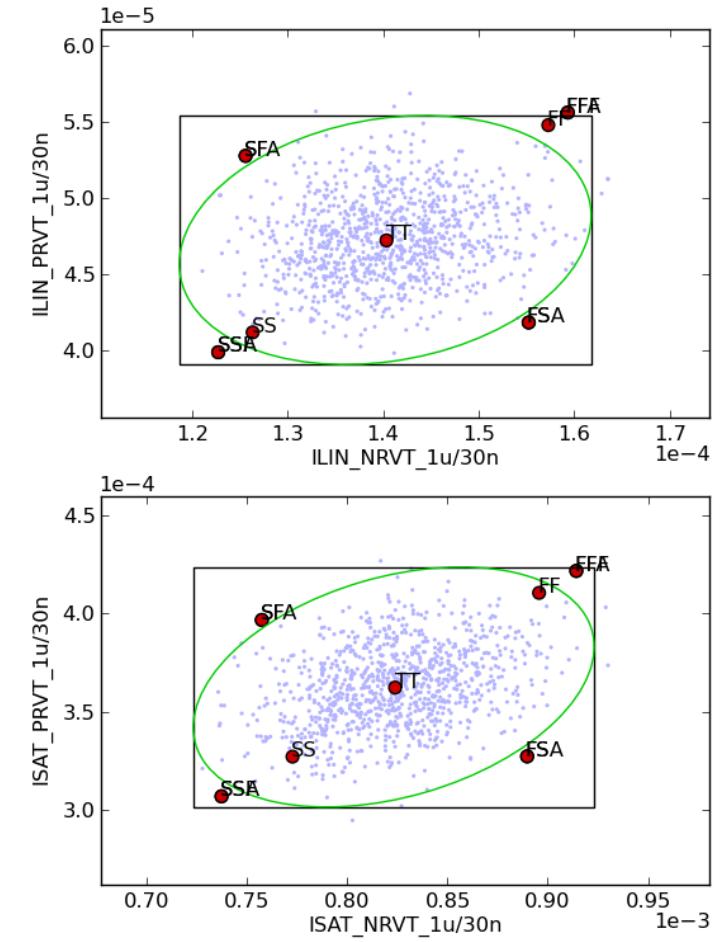
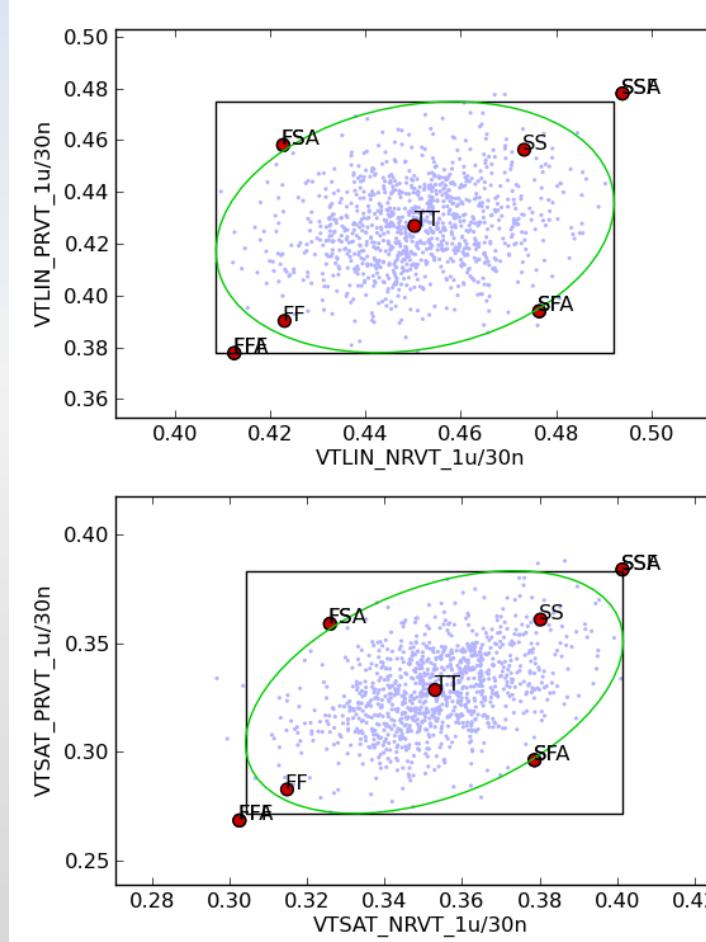
Corners	Active DW	Poly DL	Gate oxide Tox	NMOS			PMOS		
				μ	Vth	Rs	μ	Vth	Rs
pro_SS(F)			↗	↘	↗	↗	↘	↗	↗
pro_SF(F)			=	↘	↗	↗	↗	↘	↘
pro_TT			=	=	=	=	=	=	=
pro_FS			=	↗	↘	↘	↘	↗	↗
pro_FF(F)			↘	↗	↘	↘	↗	↘	↘
pro_SS(F)	↘	↗							
pro_SF, TT, FF(F)	=	=							
pro_FF(F)	↗	↘							

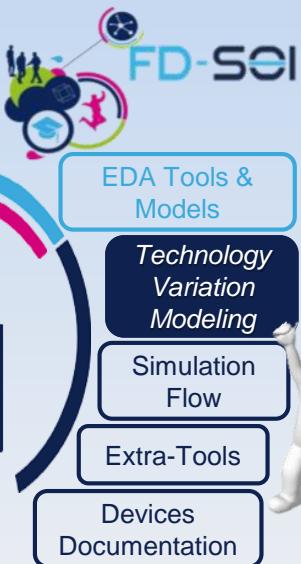
Pre-defined corners affect all MOS at once

Unrealistic corner combinations between NMOS and PMOS are impossible.

Monte-Carlo vs PDC illustration

Illustration: RVT W/L = 210nm/30nm (NMOS) 300nm/30nm (PMOS)





Bipolar and passives pre-defined corners

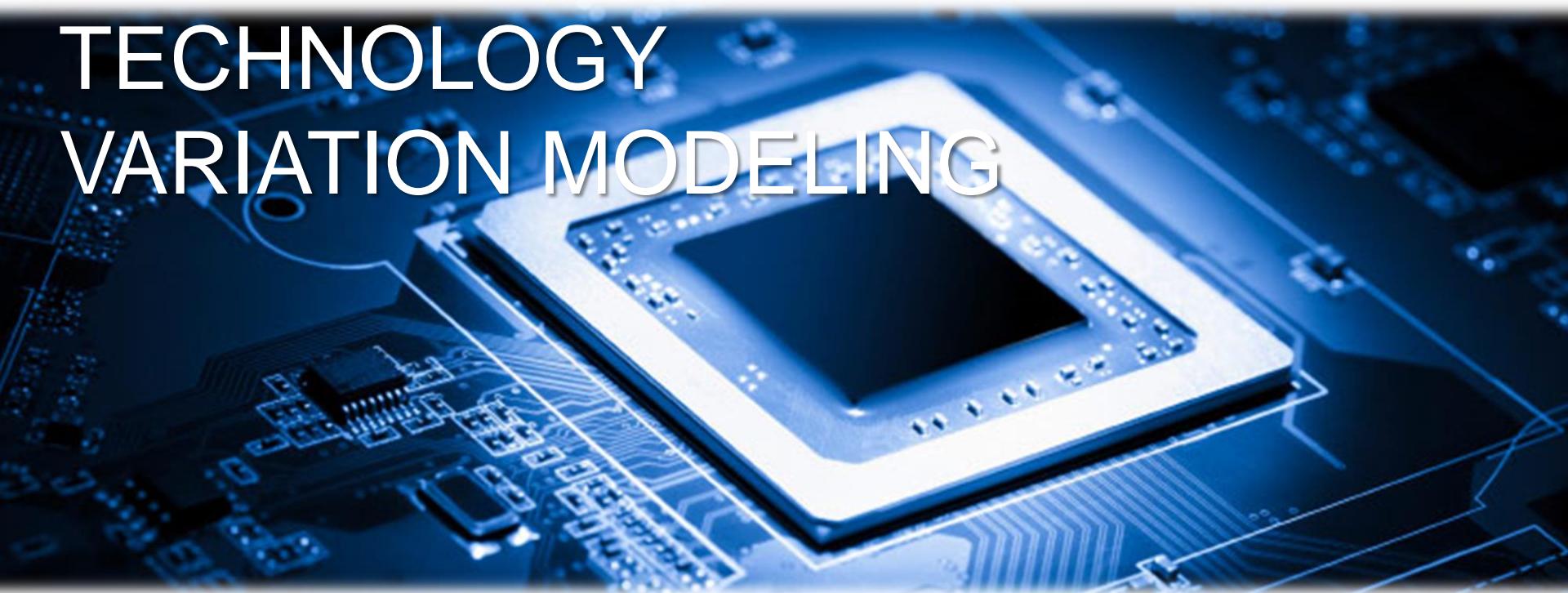
- Bipolar model
- 2 types of PDC corners:
 - GAIN corners minimize/maximize the gain of the device
 - BMIN [BMAX] corners decreases [increases] IC and increases [decreases] IB
 - Collector and Base current corners
 - IMIN [IMAX] corners minimize [maximize] IC and IB.

- Passive models
 - For the capacitors, corners minimize/maximize the capacitance: CMIN, CMAX
 - BE capacitors worst cases based on BE spacing, thickness, permittivity, ...
 - Polywell capacitor worst cases correlated to TOX variations
 - **Unrealistic combination between active and passive is possible**
 - Ex: you may choose MOS fast (thin tox) and capa slow (thick tox)
 - For the resistors, corners minimize/maximize the resistance: RMIN/RMAX
 - Mainly based on sheet resistance variations provided in DRM.

These pre-defined corners are independent from MOS ones

There is no correlation between actives and passives

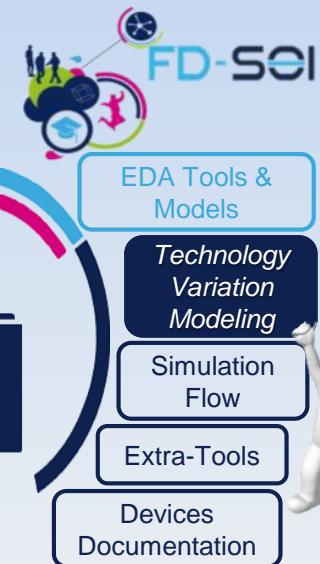
TECHNOLOGY VARIATION MODELING



- *Technology Variation Modeling*
 - *Statistical Corners*

PART II

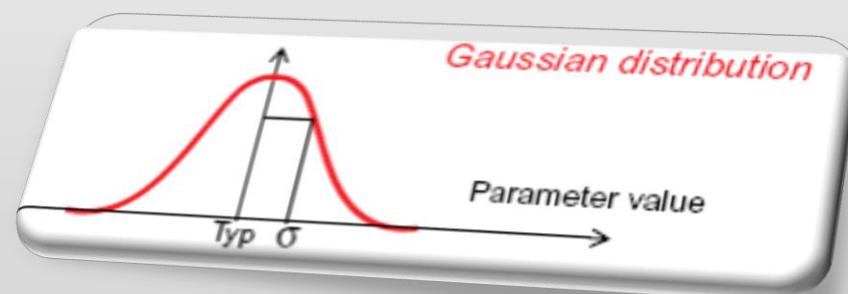
CMOS & Derivative PDK

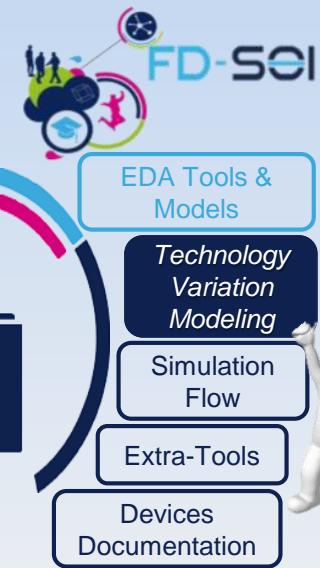


Technology Variations Modelling: Statistical modeling of global variations

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- Each process variation is defined following a statistical distribution law
 - **NORMAL** distribution is defined by
 - The mean value
 - The standard deviation value (σ)
 - Monte-Carlo used to randomly select, for each run, a value for each technology variation with the probability defined by the related distribution law
 - Stat option available: **Motherfab**
 - Defined to evaluate the design sensitivity to process shift

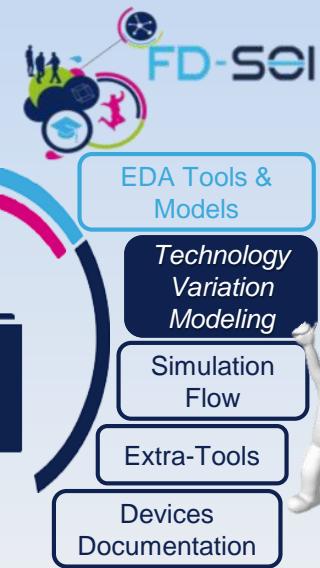




Technology Variations Modelling: Statistical modeling of global variations

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- All correlations are supported in global variations
 - Intrinsic correlations
 - Correlations between some device parameters of a given device
 - Intra-family correlations
 - Correlations between some devices of a given family
 - Ex: poly CD between NMOS and PMOS
 - Inter-family correlations
 - Correlations between different families of devices like active and passives
 - EX: poly sheet resistance and poly CD between MOS transistors and resistors
 - No unrealistic combination is possible.



Technology Variations modelling summary

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• Variations

- Global variations reflect process variations
 - All devices on a die are exposed to the same global variations
- Local variations reflect random fluctuations
 - Identically designed neighbors are slightly different

• Variations modeling

- Statistical modeling is the reference
 - Adapted to all devices / figure of merit
 - Correlation taken into account
- Pre-defined corners are defined for digital figure of merit
 - Not always relevant for analog design
 - Reflect global variations. Local variations can be modeled on top of them

SIMULATION FLOW

PART III

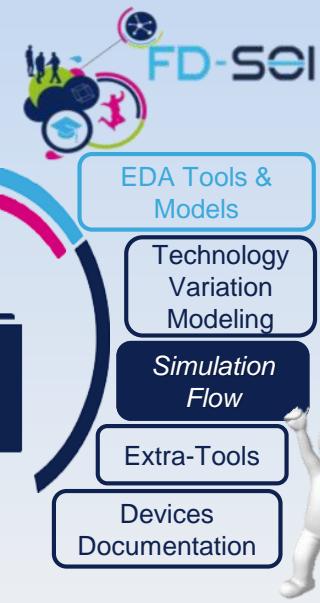
CMOS & Derivative PDK

SIMULATION FLOW

PART III

- *How to set corners*

CMOS & Derivative PDK



How to set corners

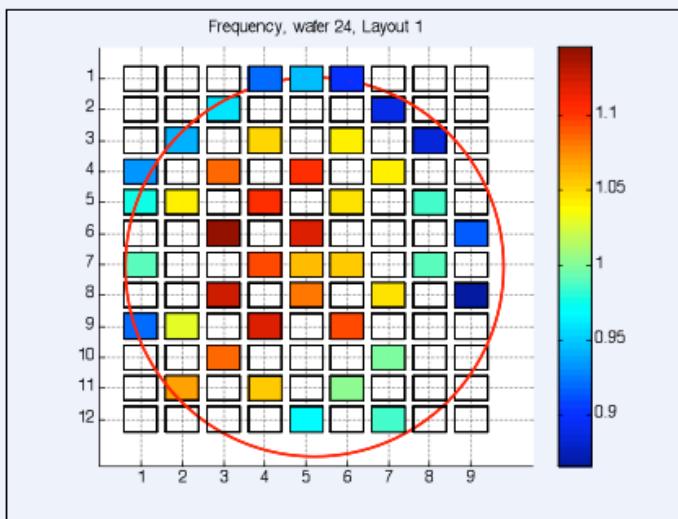
33

- Devices may be correlated through Common Variations
 - Mosfets corners are specified by setting corners in correlation common files
 - common_fet.lib
 - common_feol.lib

Common FET Variations	Device Specific Variations
Poly CD (PC)	Threshold Voltage (Vth) - FET
Active CD (RX)	Flat Band Voltage (Vfb) - Capacitor
Oxyde Thickness (Tox)	Sheet Resistance - Resistor

- Examples of Mosfet corners setting:
 - Simulating a nfet in **SSF** corner
 - .lib <eldolibpath>/common_feol.lib **PRO_SSA**
 - .lib <eldolibpath>/common_fet.lib **PRO_SSA**
 - .lib <eldolibpath>/RVT.lib **rvt_TT**
 - Simulating a nfet in **stat** corner
 - .lib <eldolibpath>/common_feol.lib **PRO_statmotherfab**
 - .lib <eldolibpath>/common_fet.lib **PRO_statmotherfab**
 - .lib <eldolibpath>/RVT.lib **rvt_TT**

How to set corners: Monte Carlo Simulation



Each die (due to its position) is affected in a different way.
All the devices inside it follow a unique trend : For each STAT run, global random parameters (gaussian distribution) are computed and affect each device in the same way : to cover more die : need significant # of runs.

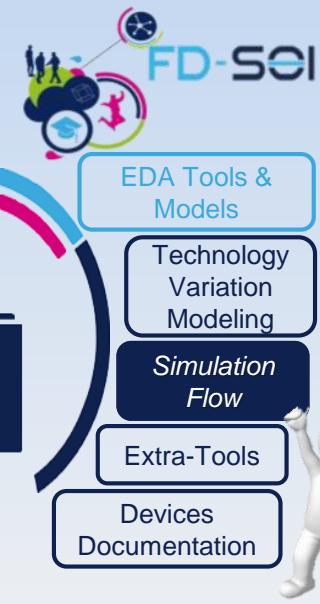


Montecarlo Simulation :

All flags set → *_dev = 1
 Passive devices → corner stat
 Common libraries → corner stat
 For a full coverage of the scenarios
 Lot of runs ...

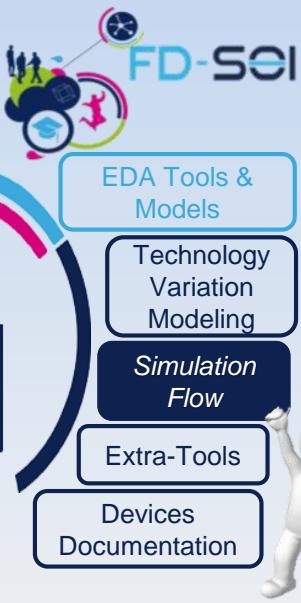
- Examples of rvt corner setting:

- .param rvt_dev =1
- .param lvt_dev =1
-
- .lib < eldolibpath >/common_feoL.lib **PRO_statmotherfab**
- .lib < eldolibpath >/common_fet.lib **PRO_statmotherfab**
- .lib < eldolibpath >/RVT.lib **rvt_TT**
- lib < eldolibpath >/LVT.lib **lvt_TT**



How to set corners: example of netlist

- Examples of rvt corner setting:
 - Simulating a netlist with local mismatch :
 - .param rvt_dev =1
 - .param lvt_dev =1
 -
 - .lib < eldolibpath >/common_feol.lib **PRO_statmotherfab**
 - .lib < eldolibpath >/common_fet.lib **PRO_statmotherfab**
 - .lib < eldolibpath >/RVT.lib **rvt_TT**
 - lib < eldolibpath >/LVT.lib **lvt_TT**
 - Examples of capa/res corner setting:
 - Simulating a netlist with local mismatch :
 - .param rpolyp_dev =1
 - .param egncap_dev =0
 - .lib < eldolibpath >/EG_cpoly.lib' **engcap_cmax**
 - .lib < eldolibpath >/resistor.lib' **rpolyp_rmin**
 - .lib < eldolibpath >/RVT.lib **rvt_TT**
 -



How to set corners

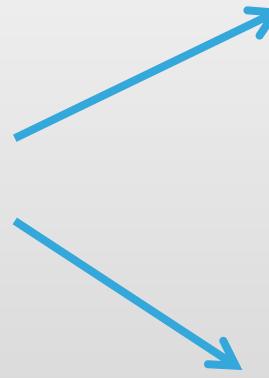
36

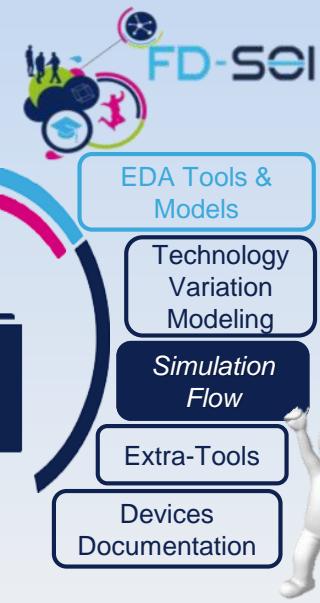
By default local mismatch turned off



```
* -----  
* Mismatch Variations Selection  
* -----  
.param cmom_6u1x_2u2x_2t8x_lb_dev=0  
.param pnpv_dev=0  
.param lvt_dev=0  
.param eglvt_dev=0  
    . . .  
    . . .  
.param veriloga_dev=0  
  
* -----  
* Models Library Files References  
* -----  
.lib '$PDKITROOT/DATA/MODELS/ELDO/CORNERS/common_beol.lib'  
PRO_TT  
.lib '$PDKITROOT/DATA/MODELS/ELDO/CORNERS/common_feol.lib'  
PRO_TT  
.lib '$PDKITROOT/DATA/MODELS/ELDO/CORNERS/common_fet.lib'  
PRO_TT  
    . . .  
    . . .  
    . . .  
  
.lib '$PDKITROOT/DATA/MODELS/ELDO/CORNERS/bipolar.lib' pnpv_typ  
.lib '$PDKITROOT/DATA/MODELS/ELDO/CORNERS/LVT.lib' lvt_TYP  
.lib '$PDKITROOT/DATA/MODELS/ELDO/CORNERS/EGLVT.lib' eglvt_TYP  
.lib '$PDKITROOT/DATA/MODELS/ELDO/CORNERS/veriloga.lib'  
veriloga_TYP
```

By default, typical corners selected.





Corner setup : summary

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Family name	devices	corners	dependency
RVT	nfet , pfet	TT	common_fet & feol
LVT	lvtnfet, lvtpfet	TT	common_fet & feol
resistor	rpolyp	TT , rmax, rmin, stat	common_feol
diode	diodetwx , diodenx ...	typ , fast , slow	--



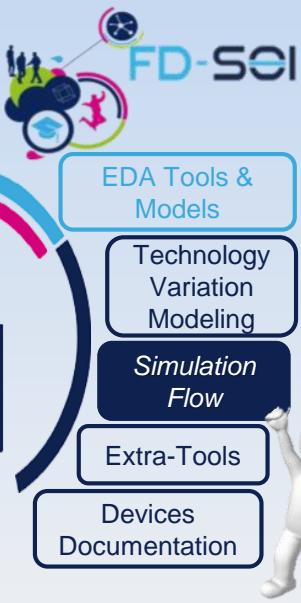
Library names (correlation)	Corners available
common_beol	TT cmax cmin stat
common_feol	TT FF FFF FS SF SFF SS SSF stat
common_fet	TT FF FFF FS SF SFF SS SSF stat
common_esd	TT ESDBC ESDWC stat

SIMULATION FLOW

PART III

- *How to simulate*

CMOS & Derivative PDK



Corners file

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- A “corners” file is provided within the PDK at the path:
 - contains the link to the models with the setting of the corners
 - contains the setting of mdev flags for each device family
 - When set to 1 the mismatch is taken into account during simulation for the corresponding family
 - copy it " from \$PDKITROOT/DATA/MODELS/<simulator>/CORNERS/ directory in the working directory
 - By default, all corners are set to the typical corner TT
 - No mismatch: all the flag : <family_dev>=0
 - Could be used as it is
 - Up to you to update this file according to the type of simulations/corners wanted (SF, stat, Monte carlo...)

- The corners file need be loaded in ADE
 - Setup → Model Libraries
 - Switch View List/Stop View List to specify for the simulation
 - Setup → Environment

Recommended to use the .simrc , .cdsinit and cds.lib available in the PDK which set the environment

EDA Tools &
Models

Technology
Variation
Modeling

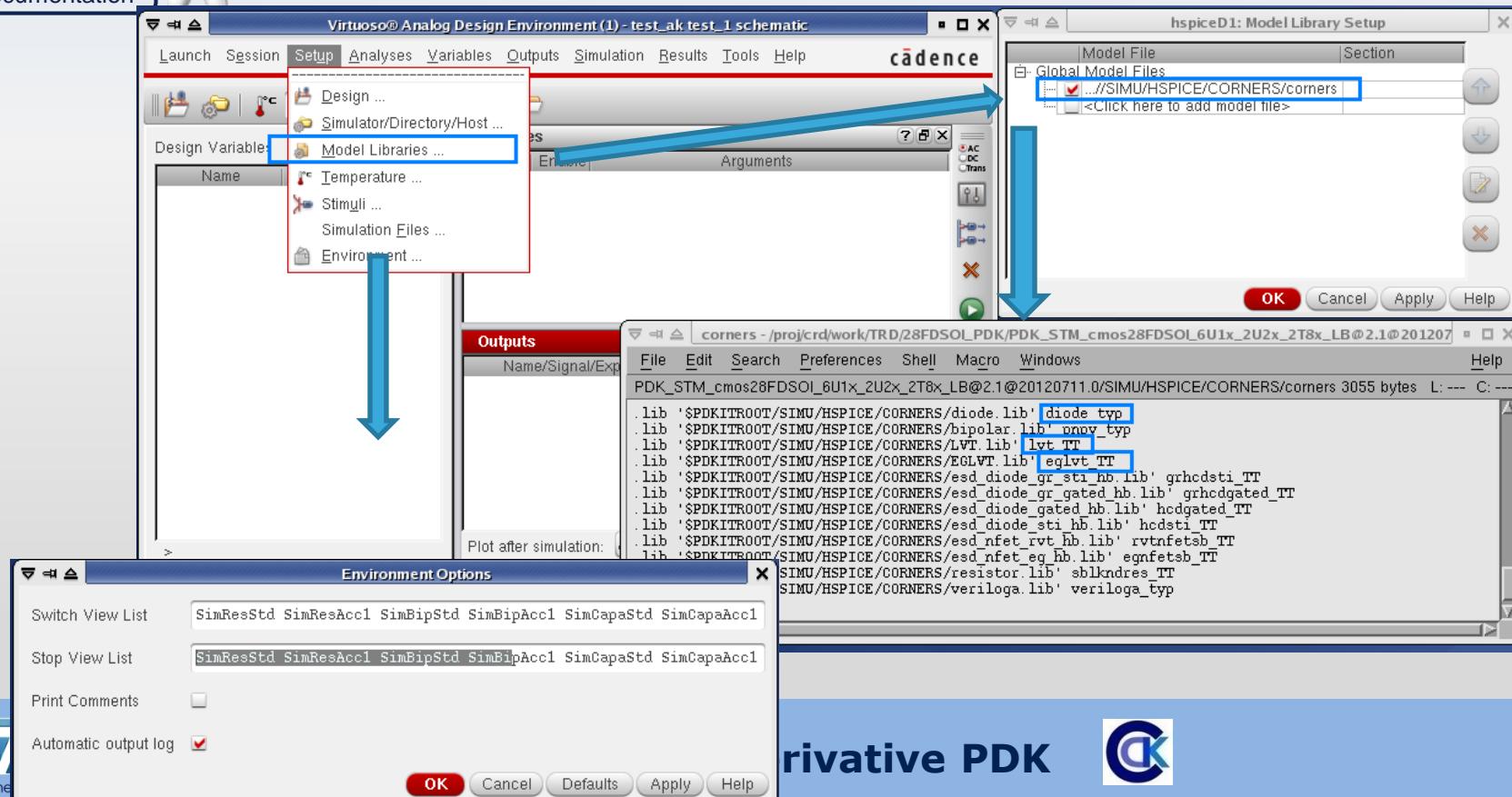
Simulation
Flow

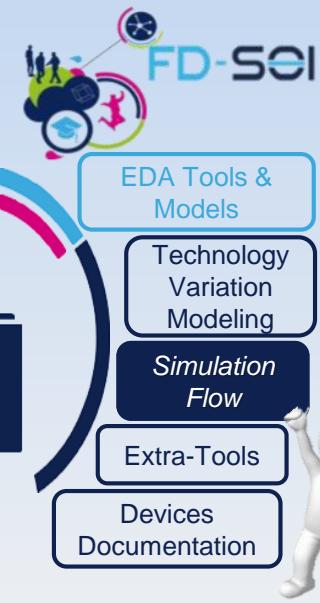
Extra-Tools

Devices
Documentation



- The corners file needs to be loaded in ADE
 - Setup → Model Libraries
- Switch View List/Stop View List to specify for the simulation
 - Setup → Environment



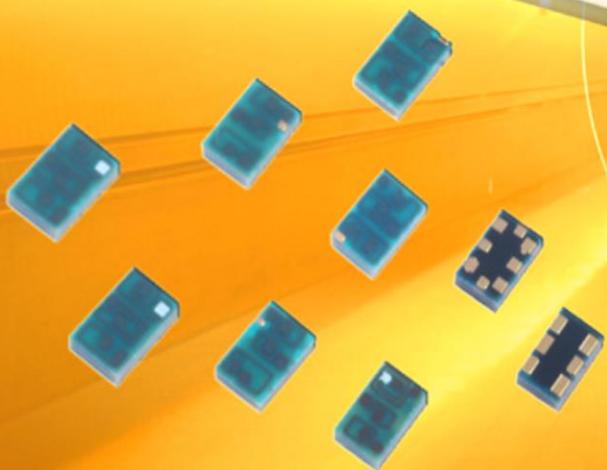


Simulate in batch

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- Include corners file in the netlist. Following line to add:
 - For Eldo: ".include 'corners.lib'"
 - For Hspice: ".include "corners.lib""
 - For Spectre: "include "corners.scs""
- Launch simulation by running:
 - eldo <netlist>
 - hspice <netlist>
 - spectre <netlist>

DOCUMENTATION DEVICES



PART IV

CMOS & Derivative PDK

EDA Tools & Models

Technology Variation Modeling

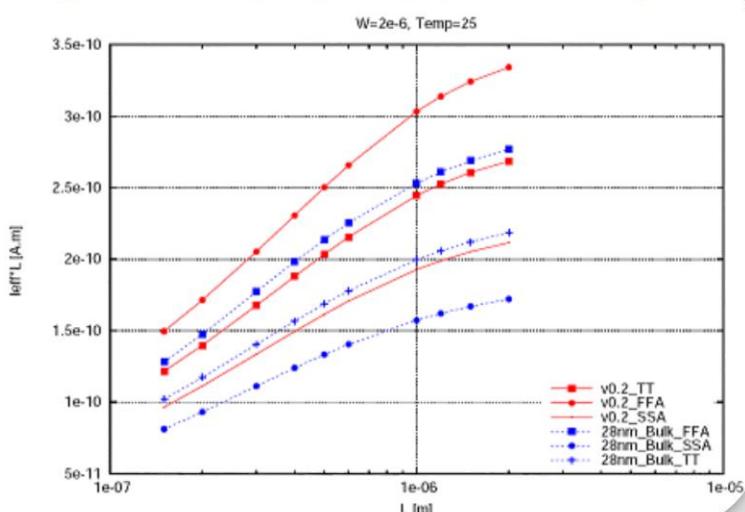
Simulation Flow

Extra-Tools

Devices Documentation



eglvtnfet leff*L [A.m] vs. L [m], W=2e-6, Temp=25



- Models documentation available at:
 - **\$PDKROOT/doc/TECHNOLOGY/MODELS/**
 - A standard report for each device
 - General information
 - Simulation Data
 - Electrical Characteristics
 - Output parameters...

- The model reference Guide
 - **Mosfet corners ,global flags / switches**
 - **Non-fet devices : list and corners...**
 - **Compact model information, models feature**

- Identify the key concept of simulation
- Identify the simulation flow
- Configure the CAD tools





Thanks for your attention