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C28SOI_SC_12_CLK_LL Databook

12 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

Overview

- C28SOI_SC_12_CLK_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 328 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

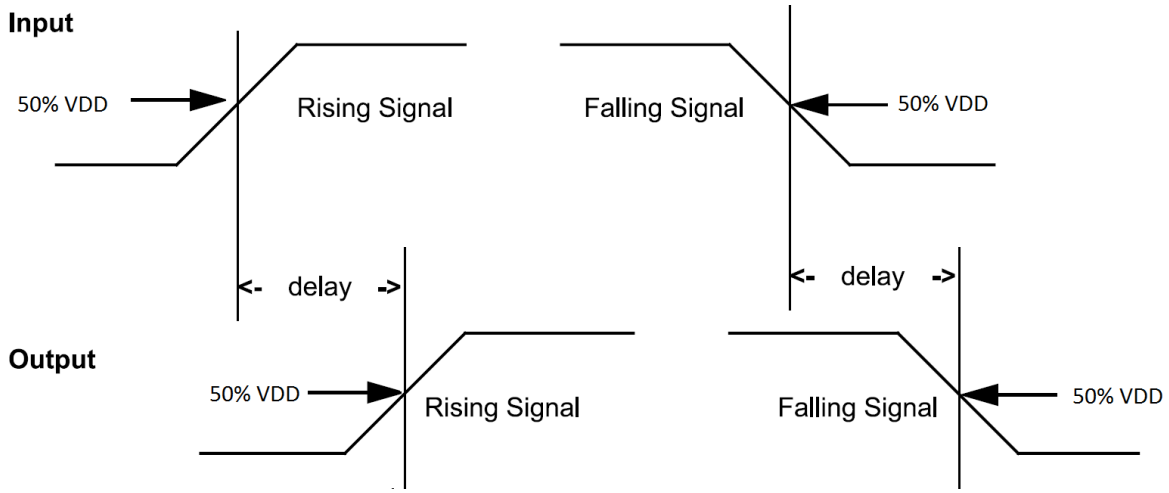


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

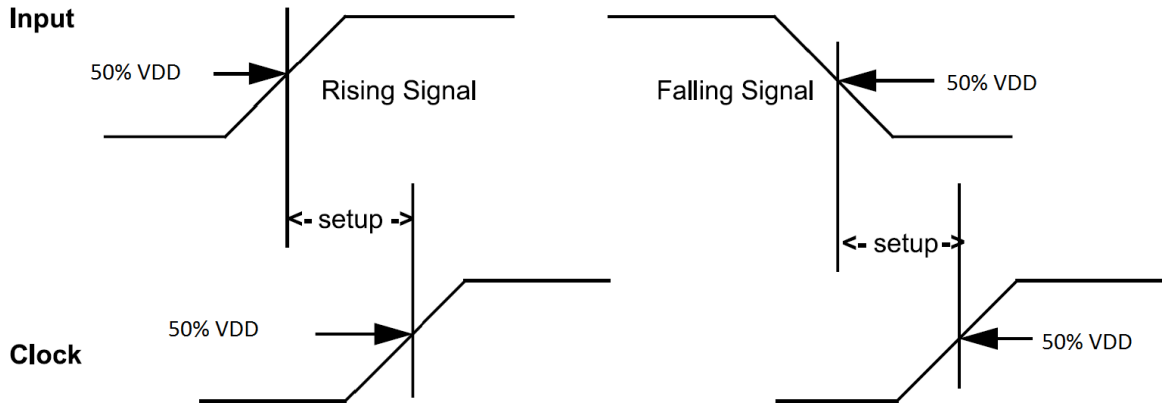


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

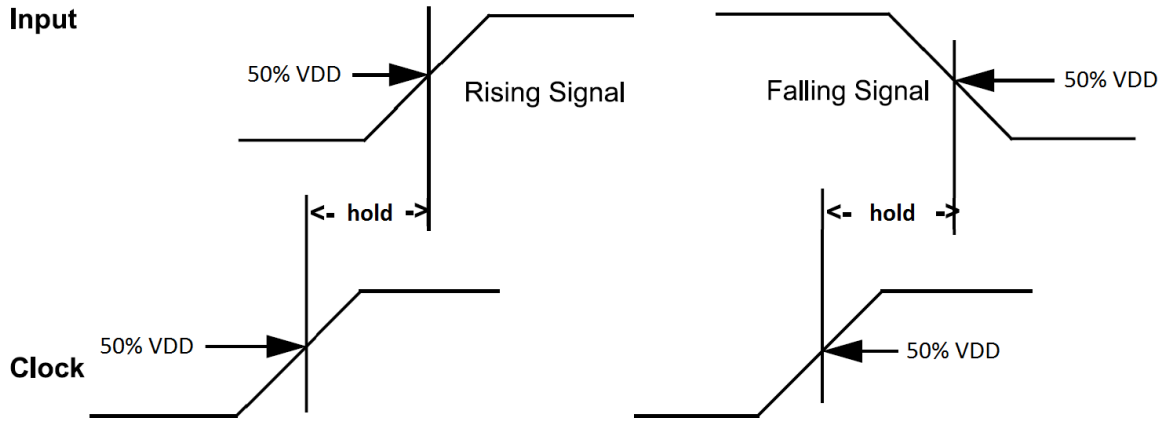


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

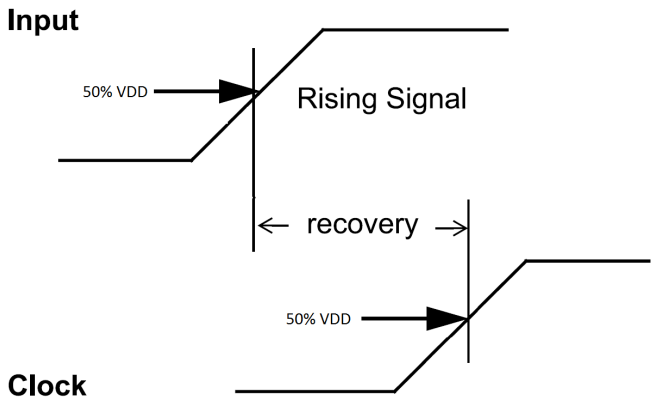


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

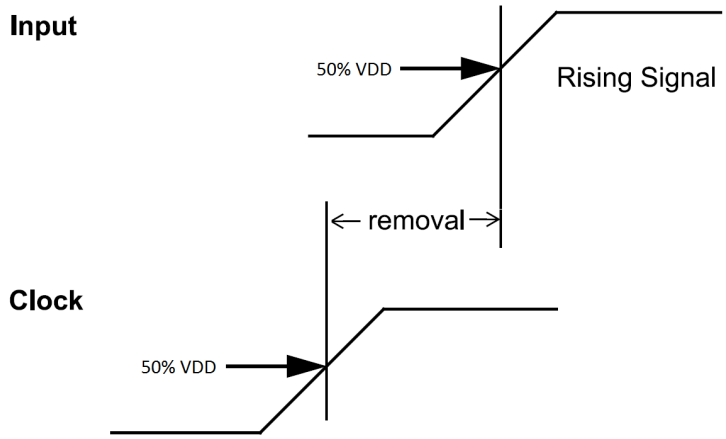


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

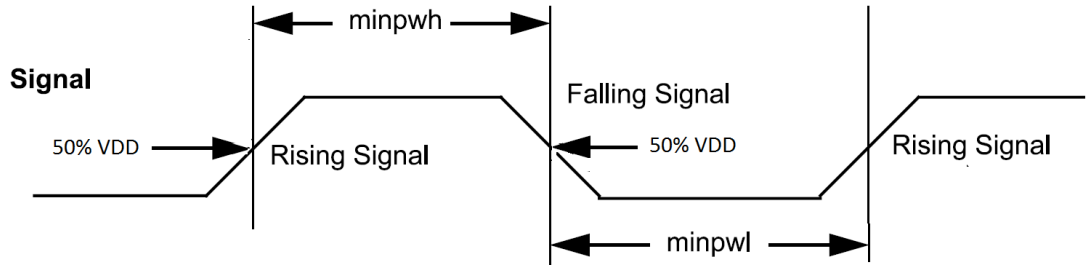


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

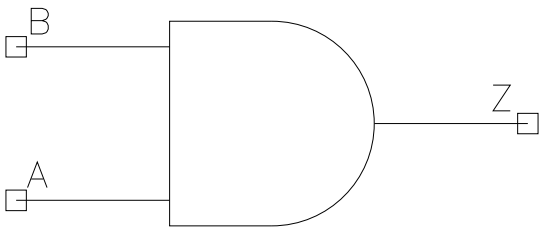
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

CNAND2

Cell Description

2 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.680	0.8160
X15_P4	1.200	0.680	0.8160
X15_P10	1.200	0.680	0.8160
X15_P16	1.200	0.680	0.8160
X20_P0	1.200	0.816	0.9792
X20_P4	1.200	0.816	0.9792
X20_P10	1.200	0.816	0.9792
X20_P16	1.200	0.816	0.9792
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0008	0.0009	0.0009	0.0010
B	0.0008	0.0008	0.0009	0.0009
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0008	0.0009	0.0009	0.0010
B	0.0008	0.0008	0.0009	0.0009
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0014	0.0014	0.0015	0.0016
B	0.0014	0.0014	0.0015	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0258	0.0289	1.2351	1.3395
A to Z ↑	0.0218	0.0241	1.4701	1.6561
B to Z ↓	0.0247	0.0276	1.2358	1.3380
B to Z ↑	0.0230	0.0255	1.4699	1.6558
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0347	0.0398	1.4881	1.6201
A to Z ↑	0.0287	0.0327	1.9387	2.2027
B to Z ↓	0.0330	0.0379	1.4864	1.6178
B to Z ↑	0.0301	0.0342	1.9376	2.2009
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0285	0.0330	0.9099	0.9887
A to Z ↑	0.0245	0.0281	1.0875	1.2246
B to Z ↓	0.0275	0.0317	0.9102	0.9871
B to Z ↑	0.0258	0.0296	1.0869	1.2257
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0395	0.0453	1.0984	1.1961
A to Z ↑	0.0334	0.0380	1.4351	1.6311
B to Z ↓	0.0379	0.0436	1.0966	1.1958
B to Z ↑	0.0349	0.0396	1.4357	1.6312
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0283	0.0322	0.5151	0.5586
A to Z ↑	0.0212	0.0242	0.7411	0.8328
B to Z ↓	0.0259	0.0295	0.5140	0.5567
B to Z ↑	0.0217	0.0247	0.7410	0.8338
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0383	0.0445	0.6200	0.6755
A to Z ↑	0.0287	0.0332	0.9737	1.1041
B to Z ↓	0.0349	0.0404	0.6180	0.6735
B to Z ↑	0.0290	0.0333	0.9739	1.1044

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X15_P0	1.867e-04	1.000e-20
X15_P4	6.346e-05	1.000e-20
X15_P10	1.897e-05	1.000e-20
X15_P16	8.316e-06	1.000e-20
X20_P0	2.323e-04	1.000e-20
X20_P4	7.851e-05	1.000e-20
X20_P10	2.335e-05	1.000e-20
X20_P16	1.020e-05	1.000e-20
X33_P0	3.615e-04	1.000e-20
X33_P4	1.243e-04	1.000e-20
X33_P10	3.765e-05	1.000e-20
X33_P16	1.666e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.682e-05	1.513e-05	1.457e-05	1.350e-05
B (output stable)	2.812e-05	2.866e-05	2.861e-05	2.796e-05
A to Z	3.379e-03	3.144e-03	3.151e-03	3.182e-03

B to Z	3.288e-03	3.032e-03	3.003e-03	3.020e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	1.718e-05	1.544e-05	1.469e-05	1.368e-05
B (output stable)	2.818e-05	2.865e-05	2.850e-05	2.794e-05
A to Z	4.470e-03	4.321e-03	4.299e-03	4.312e-03
B to Z	4.387e-03	4.209e-03	4.152e-03	4.151e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	6.914e-05	6.363e-05	5.952e-05	5.769e-05
B (output stable)	1.810e-04	1.831e-04	1.972e-04	2.513e-04
A to Z	6.915e-03	6.580e-03	6.506e-03	6.695e-03
B to Z	6.491e-03	6.094e-03	5.945e-03	6.063e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

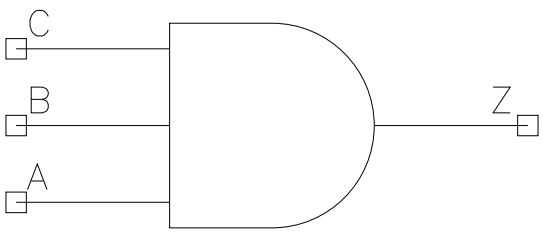
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAND3

Cell Description

3 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X25_P0	1.200	1.360	1.6320
X25_P4	1.200	1.360	1.6320
X25_P10	1.200	1.360	1.6320
X25_P16	1.200	1.360	1.6320
X33_P0	1.200	1.768	2.1216
X33_P4	1.200	1.768	2.1216
X33_P10	1.200	1.768	2.1216
X33_P16	1.200	1.768	2.1216

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0008	0.0008	0.0009	0.0009
B	0.0008	0.0008	0.0008	0.0008
C	0.0008	0.0008	0.0008	0.0008
	X25_P0	X25_P4	X25_P10	X25_P16
A	0.0016	0.0017	0.0018	0.0019
B	0.0014	0.0015	0.0016	0.0017
C	0.0014	0.0015	0.0016	0.0016
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0019	0.0020	0.0021	0.0022
B	0.0017	0.0018	0.0019	0.0020

C	0.0017	0.0018	0.0019	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0334	0.0380	1.0255	1.1119
A to Z ↑	0.0312	0.0355	1.0589	1.1928
B to Z ↓	0.0325	0.0369	1.0253	1.1110
B to Z ↑	0.0324	0.0364	1.0583	1.1912
C to Z ↓	0.0314	0.0356	1.0243	1.1094
C to Z ↑	0.0330	0.0370	1.0586	1.1925
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
A to Z ↓	0.0453	0.0526	1.2339	1.3451
A to Z ↑	0.0422	0.0491	1.3958	1.5870
B to Z ↓	0.0440	0.0509	1.2338	1.3442
B to Z ↑	0.0428	0.0492	1.3964	1.5878
C to Z ↓	0.0422	0.0489	1.2317	1.3422
C to Z ↑	0.0433	0.0497	1.3959	1.5875
	X25_P0	**X25_P4**	**X25_P0**	**X25_P4**
A to Z ↓	0.0248	0.0283	0.6920	0.7497
A to Z ↑	0.0242	0.0276	1.0019	1.1247
B to Z ↓	0.0237	0.0271	0.6922	0.7488
B to Z ↑	0.0253	0.0285	1.0011	1.1248
C to Z ↓	0.0224	0.0256	0.6917	0.7486
C to Z ↑	0.0260	0.0291	1.0000	1.1235
	X25_P10	**X25_P16**	**X25_P10**	**X25_P16**
A to Z ↓	0.0337	0.0387	0.8315	0.9042
A to Z ↑	0.0330	0.0380	1.3116	1.4887
B to Z ↓	0.0322	0.0369	0.8297	0.9040
B to Z ↑	0.0336	0.0384	1.3119	1.4871
C to Z ↓	0.0302	0.0345	0.8300	0.9021
C to Z ↑	0.0341	0.0387	1.3127	1.4887
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0259	0.0299	0.5086	0.5517
A to Z ↑	0.0267	0.0306	0.5161	0.5799
B to Z ↓	0.0250	0.0287	0.5077	0.5502
B to Z ↑	0.0280	0.0316	0.5155	0.5792
C to Z ↓	0.0240	0.0275	0.5080	0.5504
C to Z ↑	0.0288	0.0324	0.5151	0.5793
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0356	0.0410	0.6122	0.6670
A to Z ↑	0.0364	0.0420	0.6770	0.7682
B to Z ↓	0.0341	0.0393	0.6121	0.6667
B to Z ↑	0.0370	0.0423	0.6767	0.7676
C to Z ↓	0.0327	0.0375	0.6114	0.6656
C to Z ↑	0.0377	0.0428	0.6770	0.7677

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P0	2.519e-04	1.000e-20
X17_P4	8.403e-05	1.000e-20

X17_P10	2.456e-05	1.000e-20
X17_P16	1.058e-05	1.000e-20
X25_P0	2.966e-04	1.000e-20
X25_P4	1.008e-04	1.000e-20
X25_P10	3.008e-05	1.000e-20
X25_P16	1.316e-05	1.000e-20
X33_P0	5.440e-04	1.000e-20
X33_P4	1.833e-04	1.000e-20
X33_P10	5.394e-05	1.000e-20
X33_P16	2.328e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	1.986e-05	1.872e-05	1.818e-05	1.724e-05
B (output stable)	2.262e-05	2.119e-05	2.399e-05	3.493e-05
C (output stable)	4.935e-05	5.054e-05	6.476e-05	8.315e-05
A to Z	5.105e-03	4.797e-03	4.719e-03	4.778e-03
B to Z	4.996e-03	4.666e-03	4.563e-03	4.601e-03
C to Z	4.896e-03	4.544e-03	4.411e-03	4.431e-03
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	3.711e-05	3.416e-05	3.226e-05	3.099e-05
B (output stable)	4.462e-05	4.099e-05	4.539e-05	6.667e-05
C (output stable)	1.023e-04	1.046e-04	1.322e-04	1.687e-04
A to Z	5.965e-03	5.718e-03	5.701e-03	5.817e-03
B to Z	5.721e-03	5.435e-03	5.382e-03	5.465e-03
C to Z	5.506e-03	5.183e-03	5.071e-03	5.114e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	4.485e-05	4.190e-05	4.080e-05	3.887e-05
B (output stable)	5.464e-05	5.130e-05	5.739e-05	8.376e-05
C (output stable)	1.290e-04	1.319e-04	1.666e-04	2.115e-04
A to Z	9.589e-03	9.189e-03	9.038e-03	9.175e-03
B to Z	9.312e-03	8.859e-03	8.650e-03	8.748e-03
C to Z	9.072e-03	8.559e-03	8.286e-03	8.326e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

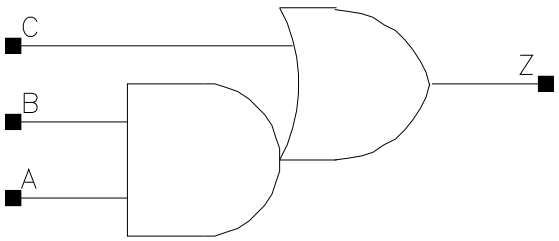
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	1.632	1.9584
X33_P4	1.200	1.632	1.9584
X33_P10	1.200	1.632	1.9584
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0017	0.0018	0.0018	0.0019
B	0.0015	0.0015	0.0016	0.0017
C	0.0014	0.0015	0.0016	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0280	0.0321	0.5183	0.5620
A to Z ↑	0.0263	0.0297	0.7417	0.8347
B to Z ↓	0.0267	0.0305	0.5175	0.5613
B to Z ↑	0.0277	0.0311	0.7407	0.8346
C to Z ↓	0.0279	0.0323	0.5168	0.5603
C to Z ↑	0.0283	0.0318	0.7388	0.8315
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0383	0.0442	0.6244	0.6800

A to Z ↑	0.0349	0.0399	0.9752	1.1064
B to Z ↓	0.0361	0.0416	0.6236	0.6800
B to Z ↑	0.0362	0.0411	0.9742	1.1059
C to Z ↓	0.0389	0.0450	0.6224	0.6786
C to Z ↑	0.0370	0.0417	0.9715	1.1021

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X33_P0	3.623e-04	1.000e-20
X33_P4	1.280e-04	1.000e-20
X33_P10	3.994e-05	1.000e-20
X33_P16	1.807e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.253e-04	1.222e-04	1.097e-04	7.685e-05
B (output stable)	1.505e-04	1.493e-04	1.379e-04	1.148e-04
C (output stable)	1.792e-04	1.689e-04	1.672e-04	1.692e-04
A to Z	7.477e-03	7.038e-03	6.886e-03	6.946e-03
B to Z	7.259e-03	6.771e-03	6.557e-03	6.569e-03
C to Z	8.061e-03	7.725e-03	7.691e-03	7.815e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

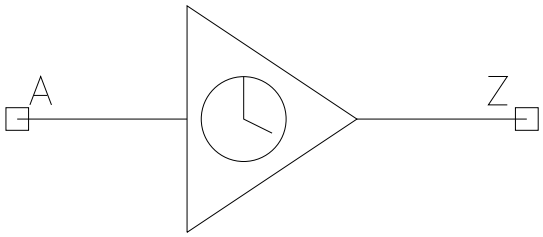
Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNBF

Cell Description

Buffer with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X4_P4	1.200	0.408	0.4896
X4_P10	1.200	0.408	0.4896
X4_P16	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X15_P0	1.200	0.544	0.6528
X15_P4	1.200	0.544	0.6528
X15_P10	1.200	0.544	0.6528
X15_P16	1.200	0.544	0.6528
X22_P0	1.200	0.680	0.8160
X22_P4	1.200	0.680	0.8160
X22_P10	1.200	0.680	0.8160
X22_P16	1.200	0.680	0.8160
X30_P0	1.200	0.952	1.1424
X30_P4	1.200	0.952	1.1424
X30_P10	1.200	0.952	1.1424
X30_P16	1.200	0.952	1.1424
X38_P0	1.200	1.088	1.3056
X38_P4	1.200	1.088	1.3056
X38_P10	1.200	1.088	1.3056
X38_P16	1.200	1.088	1.3056
X44_P0	1.200	1.224	1.4688
X44_P4	1.200	1.224	1.4688
X44_P10	1.200	1.224	1.4688
X44_P16	1.200	1.224	1.4688
X52_P0	1.200	1.496	1.7952
X52_P4	1.200	1.496	1.7952
X52_P10	1.200	1.496	1.7952
X52_P16	1.200	1.496	1.7952
X59_P0	1.200	1.632	1.9584

X59_P4	1.200	1.632	1.9584
X59_P10	1.200	1.632	1.9584
X59_P16	1.200	1.632	1.9584
X70_P0	1.200	1.768	2.1216
X70_P4	1.200	1.768	2.1216
X70_P10	1.200	1.768	2.1216
X70_P16	1.200	1.768	2.1216
X94_P0	1.200	2.312	2.7744
X94_P4	1.200	2.312	2.7744
X94_P10	1.200	2.312	2.7744
X94_P16	1.200	2.312	2.7744
X133_P0	1.200	3.264	3.9168
X133_P4	1.200	3.264	3.9168
X133_P10	1.200	3.264	3.9168
X133_P16	1.200	3.264	3.9168

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X4_P4	X4_P10	X4_P16
A	0.0006	0.0006	0.0007	0.0007
	X7_P0	X7_P4	X7_P10	X7_P16
A	0.0006	0.0007	0.0007	0.0007
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0008	0.0009	0.0009	0.0010
	X22_P0	X22_P4	X22_P10	X22_P16
A	0.0010	0.0010	0.0011	0.0011
	X30_P0	X30_P4	X30_P10	X30_P16
A	0.0014	0.0014	0.0015	0.0016
	X38_P0	X38_P4	X38_P10	X38_P16
A	0.0016	0.0017	0.0018	0.0019
	X44_P0	X44_P4	X44_P10	X44_P16
A	0.0017	0.0017	0.0019	0.0020
	X52_P0	X52_P4	X52_P10	X52_P16
A	0.0022	0.0023	0.0025	0.0026
	X59_P0	X59_P4	X59_P10	X59_P16
A	0.0025	0.0026	0.0028	0.0030
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0026	0.0027	0.0029	0.0031
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0034	0.0035	0.0038	0.0041
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0050	0.0052	0.0057	0.0061

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X4_P4	X4_P0	X4_P4
A to Z ↓	0.0255	0.0289	4.5398	4.9065

A to Z ↑	0.0195	0.0222	5.4617	6.1571
	X4_P10	**X4_P16**	**X4_P10**	**X4_P16**
A to Z ↓	0.0340	0.0386	5.4284	5.8946
A to Z ↑	0.0261	0.0295	7.2123	8.2059
	X7_P0	**X7_P4**	**X7_P0**	**X7_P4**
A to Z ↓	0.0251	0.0286	2.3907	2.5867
A to Z ↑	0.0188	0.0215	3.1241	3.5211
	X7_P10	**X7_P16**	**X7_P10**	**X7_P16**
A to Z ↓	0.0338	0.0387	2.8696	3.1222
A to Z ↑	0.0253	0.0287	4.1199	4.6818
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0235	0.0268	1.2534	1.3599
A to Z ↑	0.0197	0.0223	1.4592	1.6440
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0317	0.0367	1.5077	1.6419
A to Z ↑	0.0260	0.0297	1.9256	2.1854
	X22_P0	**X22_P4**	**X22_P0**	**X22_P4**
A to Z ↓	0.0235	0.0271	0.8551	0.9271
A to Z ↑	0.0207	0.0235	0.9807	1.1056
	X22_P10	**X22_P16**	**X22_P10**	**X22_P16**
A to Z ↓	0.0323	0.0372	1.0298	1.1215
A to Z ↑	0.0276	0.0312	1.2928	1.4690
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**
A to Z ↓	0.0224	0.0257	0.5986	0.6491
A to Z ↑	0.0183	0.0210	0.7338	0.8258
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
A to Z ↓	0.0302	0.0350	0.7204	0.7855
A to Z ↑	0.0243	0.0278	0.9655	1.0969
	X38_P0	**X38_P4**	**X38_P0**	**X38_P4**
A to Z ↓	0.0222	0.0255	0.4819	0.5221
A to Z ↑	0.0188	0.0214	0.5891	0.6633
	X38_P10	**X38_P16**	**X38_P10**	**X38_P16**
A to Z ↓	0.0303	0.0348	0.5807	0.6323
A to Z ↑	0.0250	0.0284	0.7750	0.8787
	X44_P0	**X44_P4**	**X44_P0**	**X44_P4**
A to Z ↓	0.0226	0.0259	0.4162	0.4512
A to Z ↑	0.0192	0.0219	0.5174	0.5835
	X44_P10	**X44_P16**	**X44_P10**	**X44_P16**
A to Z ↓	0.0309	0.0356	0.5012	0.5464
A to Z ↑	0.0256	0.0290	0.6827	0.7753
	X52_P0	**X52_P4**	**X52_P0**	**X52_P4**
A to Z ↓	0.0222	0.0254	0.3584	0.3885
A to Z ↑	0.0202	0.0229	0.4319	0.4863
	X52_P10	**X52_P16**	**X52_P10**	**X52_P16**
A to Z ↓	0.0303	0.0349	0.4315	0.4709
A to Z ↑	0.0268	0.0303	0.5681	0.6446
	X59_P0	**X59_P4**	**X59_P0**	**X59_P4**
A to Z ↓	0.0221	0.0253	0.3138	0.3407
A to Z ↑	0.0190	0.0216	0.3830	0.4309
	X59_P10	**X59_P16**	**X59_P10**	**X59_P16**
A to Z ↓	0.0299	0.0347	0.3779	0.4124
A to Z ↑	0.0252	0.0287	0.5039	0.5718

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0235	0.0266	0.2603	0.2820
A to Z ↑	0.0199	0.0224	0.3313	0.3722
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0317	0.0364	0.3135	0.3420
A to Z ↑	0.0262	0.0296	0.4347	0.4926
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0231	0.0262	0.1978	0.2149
A to Z ↑	0.0196	0.0221	0.2509	0.2824
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0311	0.0357	0.2387	0.2603
A to Z ↑	0.0258	0.0292	0.3297	0.3740
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0233	0.0264	0.1450	0.1579
A to Z ↑	0.0200	0.0226	0.1815	0.2044
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0312	0.0358	0.1757	0.1915
A to Z ↑	0.0263	0.0298	0.2383	0.2700

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P0	4.286e-05	1.000e-20
X4_P4	1.534e-05	1.000e-20
X4_P10	4.952e-06	1.000e-20
X4_P16	2.312e-06	1.000e-20
X7_P0	8.026e-05	1.000e-20
X7_P4	2.821e-05	1.000e-20
X7_P10	8.826e-06	1.000e-20
X7_P16	4.015e-06	1.000e-20
X15_P0	1.610e-04	1.000e-20
X15_P4	5.563e-05	1.000e-20
X15_P10	1.699e-05	1.000e-20
X15_P16	7.579e-06	1.000e-20
X22_P0	2.385e-04	1.000e-20
X22_P4	8.181e-05	1.000e-20
X22_P10	2.471e-05	1.000e-20
X22_P16	1.093e-05	1.000e-20
X30_P0	3.100e-04	1.000e-20
X30_P4	1.072e-04	1.000e-20
X30_P10	3.273e-05	1.000e-20
X30_P16	1.457e-05	1.000e-20
X38_P0	3.945e-04	1.000e-20
X38_P4	1.361e-04	1.000e-20
X38_P10	4.134e-05	1.000e-20
X38_P16	1.833e-05	1.000e-20
X44_P0	4.457e-04	1.000e-20
X44_P4	1.529e-04	1.000e-20
X44_P10	4.623e-05	1.000e-20
X44_P16	2.045e-05	1.000e-20
X52_P0	5.274e-04	1.000e-20
X52_P4	1.820e-04	1.000e-20
X52_P10	5.528e-05	1.000e-20

X52_P16	2.450e-05	1.000e-20
X59_P0	6.170e-04	1.000e-20
X59_P4	2.117e-04	1.000e-20
X59_P10	6.394e-05	1.000e-20
X59_P16	2.824e-05	1.000e-20
X70_P0	7.026e-04	1.000e-20
X70_P4	2.426e-04	1.000e-20
X70_P10	7.365e-05	1.000e-20
X70_P16	3.262e-05	1.000e-20
X94_P0	9.315e-04	1.000e-20
X94_P4	3.215e-04	1.000e-20
X94_P10	9.756e-05	1.000e-20
X94_P16	4.318e-05	1.000e-20
X133_P0	1.325e-03	1.000e-20
X133_P4	4.583e-04	1.000e-20
X133_P10	1.393e-04	1.000e-20
X133_P16	6.169e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	1.292e-03	1.253e-03	1.253e-03	1.275e-03
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	1.747e-03	1.679e-03	1.669e-03	1.704e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	3.033e-03	2.876e-03	2.838e-03	2.898e-03
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	4.496e-03	4.277e-03	4.220e-03	4.304e-03
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	5.785e-03	5.506e-03	5.306e-03	5.454e-03
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	7.321e-03	6.956e-03	6.822e-03	6.917e-03
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	8.242e-03	7.807e-03	7.591e-03	7.734e-03
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	1.012e-02	9.545e-03	9.441e-03	9.562e-03
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	1.130e-02	1.075e-02	1.045e-02	1.074e-02
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	1.349e-02	1.267e-02	1.244e-02	1.260e-02
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	1.762e-02	1.650e-02	1.616e-02	1.637e-02
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	2.634e-02	2.496e-02	2.430e-02	2.441e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

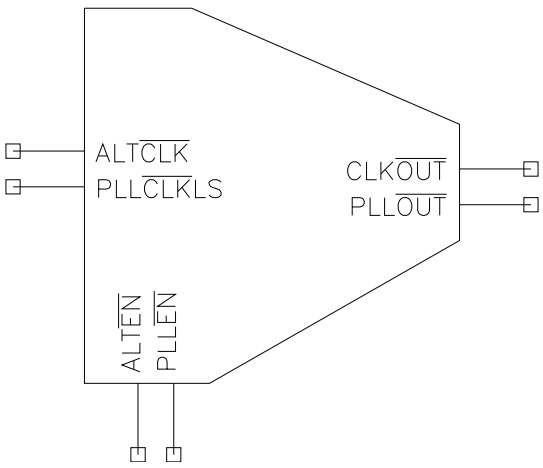
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNGFMUX21

Cell Description

2:1 Glitch-free MUX for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	2.400	2.856	6.8544
X15_P4	2.400	2.856	6.8544
X15_P10	2.400	2.856	6.8544
X15_P16	2.400	2.856	6.8544
X30_P0	2.400	3.944	9.4656
X30_P4	2.400	3.944	9.4656
X30_P10	2.400	3.944	9.4656
X30_P16	2.400	3.944	9.4656

Truth Table

PLL_CLK_LS	ALT_CLK	IPLL_EN_LD	IALT_EN_LD	CLK_OUT
0	-	-	0	0
0	0	-	-	0
-	0	0	-	0
PLL_CLK_LS	1	-	1	1
1	ALT_CLK	1	-	1
1	1	0	0	0

PLL_CLK_LS	PLL_OUT
PLL_CLK_LS	PLL_CLK_LS
1	1

PLL_EN	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

PLL_EN	0	-	PLL_EN
-	-	IPLL_EN_LD	IPLL_EN_LD
-	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

ALT_EN	ALT_CLK	IALT_EN_LD	IALT_EN_LD
ALT_EN	0	-	ALT_EN
-	-	IALT_EN_LD	IALT_EN_LD
-	ALT_CLK	IALT_EN_LD	IALT_EN_LD

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK	0.0023	0.0024	0.0025	0.0027
ALT_EN	0.0005	0.0005	0.0006	0.0006
PLL_CLK_LS	0.0029	0.0031	0.0032	0.0034
PLL_EN	0.0005	0.0005	0.0005	0.0006
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK	0.0035	0.0037	0.0039	0.0041
ALT_EN	0.0005	0.0005	0.0006	0.0006
PLL_CLK_LS	0.0048	0.0051	0.0054	0.0057
PLL_EN	0.0005	0.0005	0.0005	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
ALT_CLK to CLK_OUT ↓	0.0316	0.0358	1.2705	1.3843
ALT_CLK to CLK_OUT ↑	0.0236	0.0271	1.7193	1.9390
PLL_CLK_LS to CLK_OUT ↓	0.0286	0.0323	1.2737	1.3884
PLL_CLK_LS to CLK_OUT ↑	0.0228	0.0260	1.7218	1.9405
PLL_CLK_LS to PLL_OUT ↓	0.0239	0.0274	1.1903	1.2878
PLL_CLK_LS to PLL_OUT ↑	0.0201	0.0228	1.4638	1.6497
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
ALT_CLK to CLK_OUT ↓	0.0425	0.0489	1.5496	1.7004
ALT_CLK to CLK_OUT ↑	0.0327	0.0379	2.2709	2.5785
PLL_CLK_LS to CLK_OUT ↓	0.0380	0.0434	1.5545	1.7042
PLL_CLK_LS to CLK_OUT ↑	0.0307	0.0350	2.2730	2.5847
PLL_CLK_LS to PLL_OUT ↓	0.0325	0.0374	1.4292	1.5563
PLL_CLK_LS to PLL_OUT ↑	0.0267	0.0302	1.9305	2.1925
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**

ALT_CLK to CLK_OUT ↓	0.0303	0.0346	0.6553	0.7135
ALT_CLK to CLK_OUT ↑	0.0235	0.0272	0.7660	0.8623
PLL_CLK_LS to CLK_OUT ↓	0.0280	0.0315	0.6598	0.7184
PLL_CLK_LS to CLK_OUT ↑	0.0233	0.0264	0.7693	0.8656
PLL_CLK_LS to PLL_OUT ↓	0.0202	0.0232	0.6058	0.6566
PLL_CLK_LS to PLL_OUT ↑	0.0173	0.0197	0.7337	0.8267
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
ALT_CLK to CLK_OUT ↓	0.0412	0.0469	0.7978	0.8743
ALT_CLK to CLK_OUT ↑	0.0329	0.0378	1.0083	1.1446
PLL_CLK_LS to CLK_OUT ↓	0.0369	0.0420	0.8028	0.8792
PLL_CLK_LS to CLK_OUT ↑	0.0311	0.0353	1.0124	1.1492
PLL_CLK_LS to PLL_OUT ↓	0.0277	0.0318	0.7291	0.7930
PLL_CLK_LS to PLL_OUT ↑	0.0232	0.0262	0.9668	1.0973

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0508	0.0588	0.0680	0.0771
ALT_EN ↓	hold_rising to ALT_CLK	-0.0198	-0.0247	-0.0318	-0.0416
ALT_EN ↑	hold_rising to ALT_CLK	-0.0017	-0.0071	-0.0120	-0.0169
ALT_EN ↓	setup_rising to ALT_CLK	0.0504	0.0543	0.0667	0.0764
ALT_EN ↑	setup_rising to ALT_CLK	0.0293	0.0342	0.0417	0.0514
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0508	0.0588	0.0680	0.0771
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0198	-0.0269	-0.0367	-0.0464
PLL_EN ↑	hold_rising to PLL_CLK_LS	-0.0017	-0.0071	-0.0120	-0.0169
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0472	0.0543	0.0672	0.0764
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0293	0.0342	0.0417	0.0514
		X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0508	0.0588	0.0680	0.0771
ALT_EN ↓	hold_rising to ALT_CLK	-0.0198	-0.0247	-0.0318	-0.0421

ALT_EN ↑	hold_rising to ALT_CLK	-0.0017	-0.0071	-0.0120	-0.0169
ALT_EN ↓	setup_rising to ALT_CLK	0.0472	0.0543	0.0672	0.0770
ALT_EN ↑	setup_rising to ALT_CLK	0.0346	0.0391	0.0460	0.0563
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0508	0.0588	0.0680	0.0771
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0225	-0.0269	-0.0367	-0.0491
PLL_EN ↑	hold_rising to PLL_CLK_LS	-0.0017	-0.0071	-0.0120	-0.0169
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0504	0.0543	0.0672	0.0764
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0346	0.0395	0.0519	0.0589

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X15_P0	7.581e-04	1.000e-20
X15_P4	2.671e-04	1.000e-20
X15_P10	8.375e-05	1.000e-20
X15_P16	3.814e-05	1.000e-20
X30_P0	1.323e-03	1.000e-20
X30_P4	4.615e-04	1.000e-20
X30_P10	1.427e-04	1.000e-20
X30_P16	6.426e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	2.936e-03	2.891e-03	2.928e-03	3.020e-03
ALT_EN (output stable)	2.008e-03	1.956e-03	1.972e-03	2.037e-03
PLL_CLK_LS (output stable)	1.233e-02	7.874e-03	7.068e-03	6.423e-03
PLL_EN (output stable)	2.037e-03	1.987e-03	2.003e-03	2.058e-03
ALT_CLK to CLK_OUT	6.186e-03	6.070e-03	6.173e-03	6.403e-03
PLL_CLK_LS to CLK_OUT	4.027e-03	3.873e-03	5.179e-03	5.288e-03
PLL_CLK_LS to PLL_OUT	1.451e-02	7.856e-03	7.980e-03	6.892e-03
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	3.651e-03	3.619e-03	3.712e-03	3.842e-03
ALT_EN (output stable)	2.197e-03	2.160e-03	2.193e-03	2.275e-03
PLL_CLK_LS (output stable)	2.051e-02	1.260e-02	9.807e-03	9.367e-03

PLL_EN (output stable)	2.297e-03	2.276e-03	2.336e-03	2.418e-03
ALT_CLK to CLK_OUT	1.095e-02	1.085e-02	1.115e-02	1.143e-02
PLL_CLK_LS to CLK_OUT	7.161e-03	6.883e-03	6.864e-03	6.969e-03
PLL_CLK_LS to PLL_OUT	2.578e-02	1.384e-02	9.498e-03	8.536e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

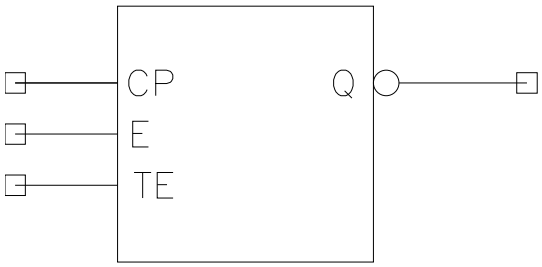
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_CLK to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to PLL_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_CLK to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to PLL_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNHLS

Cell Description

Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LLP_-CNHLSX7_P0	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX7_P4	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX7_P10	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX7_P16	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX15_P0	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX15_P4	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX15_P10	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX15_P16	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX22_P0	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX22_P4	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX22_P10	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX22_P16	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX29_P0	1.200	2.448	2.9376
C12T28SOI_LLP_-CNHLSX29_P4	1.200	2.448	2.9376
C12T28SOI_LLP_-CNHLSX29_P10	1.200	2.448	2.9376
C12T28SOI_LLP_-CNHLSX29_P16	1.200	2.448	2.9376

C12T28SOI_LLP_-CNHLSX36_P0	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX36_P4	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX36_P10	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX36_P16	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX51_P0	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX51_P4	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX51_P10	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX51_P16	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX58_P0	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX58_P4	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX58_P10	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX58_P16	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX71_P0	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX71_P4	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX71_P10	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX71_P16	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX93_P0	1.200	4.896	5.8752
C12T28SOI_LLP_-CNHLSX93_P4	1.200	4.896	5.8752
C12T28SOI_LLP_-CNHLSX93_P10	1.200	4.896	5.8752
C12T28SOI_LLP_-CNHLSX93_P16	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX29_P0	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX29_P4	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX29_P10	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX29_P16	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX36_P0	1.200	3.128	3.7536
C12T28SOI_LLPHP_-CNHLSX36_P4	1.200	3.128	3.7536

C12T28SOI_LLPHP_-CNHLSX36_P10	1.200	3.128	3.7536
C12T28SOI_LLPHP_-CNHLSX36_P16	1.200	3.128	3.7536
C12T28SOI_LLPHP_-CNHLSX44_P0	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX44_P4	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX44_P10	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX44_P16	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX51_P0	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX51_P4	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX51_P10	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX51_P16	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX58_P0	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX58_P4	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX58_P10	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX58_P16	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX71_P0	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX71_P4	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX71_P10	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX71_P16	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX86_P0	1.200	5.304	6.3648
C12T28SOI_LLPHP_-CNHLSX86_P4	1.200	5.304	6.3648
C12T28SOI_LLPHP_-CNHLSX86_P10	1.200	5.304	6.3648
C12T28SOI_LLPHP_-CNHLSX86_P16	1.200	5.304	6.3648

Truth Table

CP	E	TE	OLDIE	Q
0	-	-	-	0
1	-	-	OLDIE	OLDIE

OLDIE	OLDIE
OLDIE	OLDIE

Pin Capacitance

Pin	C12T28SOI_LLP_-CNHLSX7_P0	C12T28SOI_LLP_-CNHLSX7_P4	C12T28SOI_LLP_-CNHLSX7_P10	C12T28SOI_LLP_-CNHLSX7_P16
CP	0.0019	0.0019	0.0020	0.0021
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LLP_-CNHLSX15_P0	C12T28SOI_LLP_-CNHLSX15_P4	C12T28SOI_LLP_-CNHLSX15_P10	C12T28SOI_LLP_-CNHLSX15_P16
CP	0.0025	0.0026	0.0027	0.0029
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LLP_-CNHLSX22_P0	C12T28SOI_LLP_-CNHLSX22_P4	C12T28SOI_LLP_-CNHLSX22_P10	C12T28SOI_LLP_-CNHLSX22_P16
CP	0.0026	0.0027	0.0029	0.0031
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LLP_-CNHLSX29_P0	C12T28SOI_LLP_-CNHLSX29_P4	C12T28SOI_LLP_-CNHLSX29_P10	C12T28SOI_LLP_-CNHLSX29_P16
CP	0.0028	0.0029	0.0031	0.0033
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LLP_-CNHLSX36_P0	C12T28SOI_LLP_-CNHLSX36_P4	C12T28SOI_LLP_-CNHLSX36_P10	C12T28SOI_LLP_-CNHLSX36_P16
CP	0.0031	0.0032	0.0034	0.0037
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LLP_-CNHLSX51_P0	C12T28SOI_LLP_-CNHLSX51_P4	C12T28SOI_LLP_-CNHLSX51_P10	C12T28SOI_LLP_-CNHLSX51_P16
CP	0.0037	0.0038	0.0041	0.0043
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LLP_-CNHLSX58_P0	C12T28SOI_LLP_-CNHLSX58_P4	C12T28SOI_LLP_-CNHLSX58_P10	C12T28SOI_LLP_-CNHLSX58_P16
CP	0.0050	0.0052	0.0056	0.0060
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LLP_-CNHLSX71_P0	C12T28SOI_LLP_-CNHLSX71_P4	C12T28SOI_LLP_-CNHLSX71_P10	C12T28SOI_LLP_-CNHLSX71_P16
CP	0.0058	0.0060	0.0065	0.0069
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LLP_-CNHLSX93_P0	C12T28SOI_LLP_-CNHLSX93_P4	C12T28SOI_LLP_-CNHLSX93_P10	C12T28SOI_LLP_-CNHLSX93_P16
CP	0.0068	0.0071	0.0077	0.0081
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LLPHP_-CNHLSX29_P0	C12T28SOI_LLPHP_-CNHLSX29_P4	C12T28SOI_LLPHP_-CNHLSX29_P10	C12T28SOI_LLPHP_-CNHLSX29_P16
CP	0.0022	0.0023	0.0025	0.0026
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0010
	C12T28SOI_LLPHP_-CNHLSX36_P0	C12T28SOI_LLPHP_-CNHLSX36_P4	C12T28SOI_LLPHP_-CNHLSX36_P10	C12T28SOI_LLPHP_-CNHLSX36_P16

CP	0.0025	0.0026	0.0028	0.0030
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0010
	C12T28SOI_LLPHP_-CNHLSX44_P0	C12T28SOI_LLPHP_-CNHLSX44_P4	C12T28SOI_LLPHP_-CNHLSX44_P10	C12T28SOI_LLPHP_-CNHLSX44_P16
CP	0.0030	0.0031	0.0033	0.0035
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0010
	C12T28SOI_LLPHP_-CNHLSX51_P0	C12T28SOI_LLPHP_-CNHLSX51_P4	C12T28SOI_LLPHP_-CNHLSX51_P10	C12T28SOI_LLPHP_-CNHLSX51_P16
CP	0.0030	0.0031	0.0033	0.0034
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0010
	C12T28SOI_LLPHP_-CNHLSX58_P0	C12T28SOI_LLPHP_-CNHLSX58_P4	C12T28SOI_LLPHP_-CNHLSX58_P10	C12T28SOI_LLPHP_-CNHLSX58_P16
CP	0.0040	0.0042	0.0045	0.0048
E	0.0005	0.0006	0.0006	0.0007
TE	0.0008	0.0009	0.0009	0.0010
	C12T28SOI_LLPHP_-CNHLSX71_P0	C12T28SOI_LLPHP_-CNHLSX71_P4	C12T28SOI_LLPHP_-CNHLSX71_P10	C12T28SOI_LLPHP_-CNHLSX71_P16
CP	0.0050	0.0052	0.0055	0.0059
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0010
	C12T28SOI_LLPHP_-CNHLSX86_P0	C12T28SOI_LLPHP_-CNHLSX86_P4	C12T28SOI_LLPHP_-CNHLSX86_P10	C12T28SOI_LLPHP_-CNHLSX86_P16
CP	0.0060	0.0063	0.0067	0.0071
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LLP_-CNHLSX7_P0	**C12T28SOI_LLP_-CNHLSX7_P4**	**C12T28SOI_LLP_-CNHLSX7_P0**	**C12T28SOI_LLP_-CNHLSX7_P4**
CP to Q ↓	0.0295	0.0336	2.5011	2.7102
CP to Q ↑	0.0221	0.0252	2.9328	3.3094
	C12T28SOI_LLP_-CNHLSX7_P10	**C12T28SOI_LLP_-CNHLSX7_P16**	**C12T28SOI_LLP_-CNHLSX7_P10**	**C12T28SOI_LLP_-CNHLSX7_P16**
CP to Q ↓	0.0398	0.0458	3.0102	3.2822
CP to Q ↑	0.0298	0.0340	3.8735	4.3993
	C12T28SOI_LLP_-CNHLSX15_P0	**C12T28SOI_LLP_-CNHLSX15_P4**	**C12T28SOI_LLP_-CNHLSX15_P0**	**C12T28SOI_LLP_-CNHLSX15_P4**
CP to Q ↓	0.0246	0.0278	1.2541	1.3588
CP to Q ↑	0.0206	0.0233	1.4747	1.6599
	C12T28SOI_LLP_-CNHLSX15_P10	**C12T28SOI_LLP_-CNHLSX15_P16**	**C12T28SOI_LLP_-CNHLSX15_P10**	**C12T28SOI_LLP_-CNHLSX15_P16**
CP to Q ↓	0.0332	0.0378	1.5100	1.6440
CP to Q ↑	0.0276	0.0312	1.9433	2.2043
	C12T28SOI_LLP_-CNHLSX22_P0	**C12T28SOI_LLP_-CNHLSX22_P4**	**C12T28SOI_LLP_-CNHLSX22_P0**	**C12T28SOI_LLP_-CNHLSX22_P4**
CP to Q ↓	0.0245	0.0279	0.8651	0.9378
CP to Q ↑	0.0222	0.0251	0.9912	1.1175
	C12T28SOI_LLP_-CNHLSX22_P10	**C12T28SOI_LLP_-CNHLSX22_P16**	**C12T28SOI_LLP_-CNHLSX22_P10**	**C12T28SOI_LLP_-CNHLSX22_P16**

CP to Q ↓	0.0331	0.0383	1.0415	1.1346
CP to Q ↑	0.0294	0.0337	1.3059	1.4841
	C12T28SOI_LLP_-CNHLSX29_P0	**C12T28SOI_LLP_-CNHLSX29_P4**	**C12T28SOI_LLP_-CNHLSX29_P0**	**C12T28SOI_LLP_-CNHLSX29_P4**
CP to Q ↓	0.0246	0.0281	0.6486	0.7038
CP to Q ↑	0.0218	0.0248	0.7426	0.8379
	C12T28SOI_LLP_-CNHLSX29_P10	**C12T28SOI_LLP_-CNHLSX29_P16**	**C12T28SOI_LLP_-CNHLSX29_P10**	**C12T28SOI_LLP_-CNHLSX29_P16**
CP to Q ↓	0.0329	0.0381	0.7817	0.8520
CP to Q ↑	0.0289	0.0332	0.9801	1.1124
	C12T28SOI_LLP_-CNHLSX36_P0	**C12T28SOI_LLP_-CNHLSX36_P4**	**C12T28SOI_LLP_-CNHLSX36_P0**	**C12T28SOI_LLP_-CNHLSX36_P4**
CP to Q ↓	0.0243	0.0276	0.5185	0.5619
CP to Q ↑	0.0214	0.0243	0.5952	0.6706
	C12T28SOI_LLP_-CNHLSX36_P10	**C12T28SOI_LLP_-CNHLSX36_P16**	**C12T28SOI_LLP_-CNHLSX36_P10**	**C12T28SOI_LLP_-CNHLSX36_P16**
CP to Q ↓	0.0328	0.0379	0.6249	0.6809
CP to Q ↑	0.0286	0.0328	0.7838	0.8907
	C12T28SOI_LLP_-CNHLSX51_P0	**C12T28SOI_LLP_-CNHLSX51_P4**	**C12T28SOI_LLP_-CNHLSX51_P0**	**C12T28SOI_LLP_-CNHLSX51_P4**
CP to Q ↓	0.0263	0.0301	0.3764	0.4086
CP to Q ↑	0.0220	0.0251	0.4280	0.4820
	C12T28SOI_LLP_-CNHLSX51_P10	**C12T28SOI_LLP_-CNHLSX51_P16**	**C12T28SOI_LLP_-CNHLSX51_P10**	**C12T28SOI_LLP_-CNHLSX51_P16**
CP to Q ↓	0.0357	0.0412	0.4540	0.4948
CP to Q ↑	0.0296	0.0337	0.5636	0.6389
	C12T28SOI_LLP_-CNHLSX58_P0	**C12T28SOI_LLP_-CNHLSX58_P4**	**C12T28SOI_LLP_-CNHLSX58_P0**	**C12T28SOI_LLP_-CNHLSX58_P4**
CP to Q ↓	0.0231	0.0263	0.3305	0.3585
CP to Q ↑	0.0191	0.0218	0.3754	0.4228
	C12T28SOI_LLP_-CNHLSX58_P10	**C12T28SOI_LLP_-CNHLSX58_P16**	**C12T28SOI_LLP_-CNHLSX58_P10**	**C12T28SOI_LLP_-CNHLSX58_P16**
CP to Q ↓	0.0310	0.0356	0.3977	0.4327
CP to Q ↑	0.0255	0.0290	0.4943	0.5611
	C12T28SOI_LLP_-CNHLSX71_P0	**C12T28SOI_LLP_-CNHLSX71_P4**	**C12T28SOI_LLP_-CNHLSX71_P0**	**C12T28SOI_LLP_-CNHLSX71_P4**
CP to Q ↓	0.0224	0.0256	0.2737	0.2967
CP to Q ↑	0.0195	0.0222	0.3051	0.3437
	C12T28SOI_LLP_-CNHLSX71_P10	**C12T28SOI_LLP_-CNHLSX71_P16**	**C12T28SOI_LLP_-CNHLSX71_P10**	**C12T28SOI_LLP_-CNHLSX71_P16**
CP to Q ↓	0.0305	0.0348	0.3293	0.3587
CP to Q ↑	0.0261	0.0295	0.4020	0.4559
	C12T28SOI_LLP_-CNHLSX93_P0	**C12T28SOI_LLP_-CNHLSX93_P4**	**C12T28SOI_LLP_-CNHLSX93_P0**	**C12T28SOI_LLP_-CNHLSX93_P4**
CP to Q ↓	0.0237	0.0267	0.2154	0.2333
CP to Q ↑	0.0209	0.0234	0.2406	0.2703
	C12T28SOI_LLP_-CNHLSX93_P10	**C12T28SOI_LLP_-CNHLSX93_P16**	**C12T28SOI_LLP_-CNHLSX93_P10**	**C12T28SOI_LLP_-CNHLSX93_P16**
CP to Q ↓	0.0318	0.0364	0.2592	0.2827
CP to Q ↑	0.0276	0.0314	0.3159	0.3577
	C12T28SOI_-LLPHP_-CNHLSX29_P0	**C12T28SOI_-LLPHP_-CNHLSX29_P4**	**C12T28SOI_-LLPHP_-CNHLSX29_P0**	**C12T28SOI_-LLPHP_-CNHLSX29_P4**

CP to Q ↓	0.0234	0.0266	0.6580	0.7127
CP to Q ↑	0.0207	0.0234	0.7528	0.8440
	C12T28SOI_-LLPHP_-CNHLSX29_P10	**C12T28SOI_-LLPHP_-CNHLSX29_P16**	**C12T28SOI_-LLPHP_-CNHLSX29_P10**	**C12T28SOI_-LLPHP_-CNHLSX29_P16**
CP to Q ↓	0.0313	0.0360	0.7902	0.8610
CP to Q ↑	0.0274	0.0312	0.9850	1.1164
	C12T28SOI_-LLPHP_-CNHLSX36_P0	**C12T28SOI_-LLPHP_-CNHLSX36_P4**	**C12T28SOI_-LLPHP_-CNHLSX36_P0**	**C12T28SOI_-LLPHP_-CNHLSX36_P4**
CP to Q ↓	0.0231	0.0263	0.5254	0.5687
CP to Q ↑	0.0203	0.0231	0.6044	0.6783
	C12T28SOI_-LLPHP_-CNHLSX36_P10	**C12T28SOI_-LLPHP_-CNHLSX36_P16**	**C12T28SOI_-LLPHP_-CNHLSX36_P10**	**C12T28SOI_-LLPHP_-CNHLSX36_P16**
CP to Q ↓	0.0312	0.0359	0.6317	0.6865
CP to Q ↑	0.0272	0.0310	0.7916	0.8972
	C12T28SOI_-LLPHP_-CNHLSX44_P0	**C12T28SOI_-LLPHP_-CNHLSX44_P4**	**C12T28SOI_-LLPHP_-CNHLSX44_P0**	**C12T28SOI_-LLPHP_-CNHLSX44_P4**
CP to Q ↓	0.0233	0.0263	0.4391	0.4750
CP to Q ↑	0.0197	0.0222	0.5054	0.5666
	C12T28SOI_-LLPHP_-CNHLSX44_P10	**C12T28SOI_-LLPHP_-CNHLSX44_P16**	**C12T28SOI_-LLPHP_-CNHLSX44_P10**	**C12T28SOI_-LLPHP_-CNHLSX44_P16**
CP to Q ↓	0.0311	0.0355	0.5276	0.5736
CP to Q ↑	0.0260	0.0293	0.6606	0.7479
	C12T28SOI_-LLPHP_-CNHLSX51_P0	**C12T28SOI_-LLPHP_-CNHLSX51_P4**	**C12T28SOI_-LLPHP_-CNHLSX51_P0**	**C12T28SOI_-LLPHP_-CNHLSX51_P4**
CP to Q ↓	0.0249	0.0283	0.3795	0.4111
CP to Q ↑	0.0212	0.0239	0.4352	0.4882
	C12T28SOI_-LLPHP_-CNHLSX51_P10	**C12T28SOI_-LLPHP_-CNHLSX51_P16**	**C12T28SOI_-LLPHP_-CNHLSX51_P10**	**C12T28SOI_-LLPHP_-CNHLSX51_P16**
CP to Q ↓	0.0331	0.0383	0.4564	0.4961
CP to Q ↑	0.0277	0.0316	0.5690	0.6446
	C12T28SOI_-LLPHP_-CNHLSX58_P0	**C12T28SOI_-LLPHP_-CNHLSX58_P4**	**C12T28SOI_-LLPHP_-CNHLSX58_P0**	**C12T28SOI_-LLPHP_-CNHLSX58_P4**
CP to Q ↓	0.0215	0.0244	0.3309	0.3584
CP to Q ↑	0.0180	0.0203	0.3829	0.4295
	C12T28SOI_-LLPHP_-CNHLSX58_P10	**C12T28SOI_-LLPHP_-CNHLSX58_P16**	**C12T28SOI_-LLPHP_-CNHLSX58_P10**	**C12T28SOI_-LLPHP_-CNHLSX58_P16**
CP to Q ↓	0.0287	0.0334	0.3969	0.4320
CP to Q ↑	0.0237	0.0273	0.5002	0.5666
	C12T28SOI_-LLPHP_-CNHLSX71_P0	**C12T28SOI_-LLPHP_-CNHLSX71_P4**	**C12T28SOI_-LLPHP_-CNHLSX71_P0**	**C12T28SOI_-LLPHP_-CNHLSX71_P4**
CP to Q ↓	0.0212	0.0244	0.2748	0.2976
CP to Q ↑	0.0185	0.0212	0.3111	0.3491

	C12T28SOI_-LLPHP_-CNHLSX71_P10	C12T28SOI_-LLPHP_-CNHLSX71_P16	C12T28SOI_-LLPHP_-CNHLSX71_P10	C12T28SOI_-LLPHP_-CNHLSX71_P16
CP to Q ↓	0.0286	0.0330	0.3300	0.3589
CP to Q ↑	0.0245	0.0281	0.4058	0.4602
	C12T28SOI_-LLPHP_-CNHLSX86_P0	**C12T28SOI_-LLPHP_-CNHLSX86_P4**	**C12T28SOI_-LLPHP_-CNHLSX86_P0**	**C12T28SOI_-LLPHP_-CNHLSX86_P4**
CP to Q ↓	0.0208	0.0238	0.2320	0.2509
CP to Q ↑	0.0186	0.0211	0.2624	0.2938
	C12T28SOI_-LLPHP_-CNHLSX86_P10	**C12T28SOI_-LLPHP_-CNHLSX86_P16**	**C12T28SOI_-LLPHP_-CNHLSX86_P10**	**C12T28SOI_-LLPHP_-CNHLSX86_P16**
CP to Q ↓	0.0281	0.0324	0.2780	0.3026
CP to Q ↑	0.0246	0.0280	0.3422	0.3870

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C12T28SOI_-LLP_CNHLSX7_-P0	C12T28SOI_-LLP_CNHLSX7_-P4	C12T28SOI_-LLP_CNHLSX7_-P10	C12T28SOI_-LLP_CNHLSX7_-P16
CP ↓	min_pulse_width to CP	0.0300	0.0357	0.0401	0.0463
E ↓	hold_rising to CP	-0.0078	-0.0127	-0.0171	-0.0220
E ↑	hold_rising to CP	0.0058	0.0032	0.0036	-0.0013
E ↓	setup_rising to CP	0.0355	0.0372	0.0479	0.0523
E ↑	setup_rising to CP	0.0216	0.0265	0.0313	0.0384
TE ↓	hold_rising to CP	-0.0084	-0.0101	-0.0208	-0.0252
TE ↑	hold_rising to CP	0.0058	0.0036	0.0014	-0.0035
TE ↓	setup_rising to CP	0.0354	0.0409	0.0448	0.0518
TE ↑	setup_rising to CP	0.0244	0.0260	0.0367	0.0416
		C12T28SOI_-LLP_-CNHLSX15_P0	C12T28SOI_-LLP_-CNHLSX15_P4	C12T28SOI_-LLP_-CNHLSX15_P10	C12T28SOI_-LLP_-CNHLSX15_P16
CP ↓	min_pulse_width to CP	0.0302	0.0334	0.0378	0.0446
E ↓	hold_rising to CP	-0.0078	-0.0127	-0.0171	-0.0220
E ↑	hold_rising to CP	0.0058	0.0032	0.0036	-0.0013
E ↓	setup_rising to CP	0.0355	0.0404	0.0479	0.0518
E ↑	setup_rising to CP	0.0245	0.0265	0.0336	0.0416
TE ↓	hold_rising to CP	-0.0084	-0.0101	-0.0208	-0.0252
TE ↑	hold_rising to CP	0.0058	0.0036	-0.0013	-0.0035
TE ↓	setup_rising to CP	0.0354	0.0409	0.0448	0.0550
TE ↑	setup_rising to CP	0.0244	0.0260	0.0367	0.0442

		C12T28SOI_-LLP_-CNHLSX22_P0	C12T28SOI_-LLP_-CNHLSX22_P4	C12T28SOI_-LLP_-CNHLSX22_P10	C12T28SOI_-LLP_-CNHLSX22_P16
CP ↓	min_pulse_width to CP	0.0335	0.0364	0.0426	0.0494
E ↓	hold_rising to CP	-0.0101	-0.0155	-0.0220	-0.0295
E ↑	hold_rising to CP	0.0058	0.0036	-0.0013	-0.0035
E ↓	setup_rising to CP	0.0376	0.0420	0.0527	0.0593
E ↑	setup_rising to CP	0.0266	0.0319	0.0368	0.0465
TE ↓	hold_rising to CP	-0.0105	-0.0149	-0.0225	-0.0301
TE ↑	hold_rising to CP	0.0036	0.0036	-0.0013	-0.0035
TE ↓	setup_rising to CP	0.0382	0.0457	0.0496	0.0599
TE ↑	setup_rising to CP	0.0265	0.0313	0.0384	0.0491
		C12T28SOI_-LLP_-CNHLSX29_P0	C12T28SOI_-LLP_-CNHLSX29_P4	C12T28SOI_-LLP_-CNHLSX29_P10	C12T28SOI_-LLP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0342	0.0380	0.0432	0.0518
E ↓	hold_rising to CP	-0.0127	-0.0176	-0.0220	-0.0295
E ↑	hold_rising to CP	0.0058	0.0036	-0.0013	-0.0039
E ↓	setup_rising to CP	0.0403	0.0452	0.0518	0.0593
E ↑	setup_rising to CP	0.0266	0.0319	0.0384	0.0465
TE ↓	hold_rising to CP	-0.0133	-0.0149	-0.0252	-0.0296
TE ↑	hold_rising to CP	0.0036	0.0036	-0.0013	-0.0035
TE ↓	setup_rising to CP	0.0403	0.0448	0.0555	0.0620
TE ↑	setup_rising to CP	0.0261	0.0309	0.0416	0.0491
		C12T28SOI_-LLP_-CNHLSX36_P0	C12T28SOI_-LLP_-CNHLSX36_P4	C12T28SOI_-LLP_-CNHLSX36_P10	C12T28SOI_-LLP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0342	0.0387	0.0432	0.0518
E ↓	hold_rising to CP	-0.0127	-0.0176	-0.0220	-0.0323
E ↑	hold_rising to CP	0.0058	0.0036	-0.0013	-0.0035
E ↓	setup_rising to CP	0.0403	0.0452	0.0518	0.0625
E ↑	setup_rising to CP	0.0266	0.0319	0.0394	0.0465
TE ↓	hold_rising to CP	-0.0133	-0.0149	-0.0252	-0.0322
TE ↑	hold_rising to CP	0.0036	0.0036	-0.0013	-0.0035
TE ↓	setup_rising to CP	0.0403	0.0448	0.0550	0.0620
TE ↑	setup_rising to CP	0.0265	0.0313	0.0416	0.0491

		C12T28SOI_-LLP_-CNHLSX51_P0	C12T28SOI_-LLP_-CNHLSX51_P4	C12T28SOI_-LLP_-CNHLSX51_P10	C12T28SOI_-LLP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0318	0.0380	0.0424	0.0510
E ↓	hold_rising to CP	-0.0106	-0.0155	-0.0230	-0.0274
E ↑	hold_rising to CP	0.0058	0.0036	-0.0013	-0.0039
E ↓	setup_rising to CP	0.0349	0.0430	0.0469	0.0572
E ↑	setup_rising to CP	0.0266	0.0319	0.0384	0.0465
TE ↓	hold_rising to CP	-0.0105	-0.0159	-0.0198	-0.0306
TE ↑	hold_rising to CP	0.0036	0.0036	-0.0013	-0.0035
TE ↓	setup_rising to CP	0.0350	0.0399	0.0502	0.0571
TE ↑	setup_rising to CP	0.0265	0.0313	0.0416	0.0487
		C12T28SOI_-LLP_-CNHLSX58_P0	C12T28SOI_-LLP_-CNHLSX58_P4	C12T28SOI_-LLP_-CNHLSX58_P10	C12T28SOI_-LLP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0342	0.0387	0.0474	0.0543
E ↓	hold_rising to CP	-0.0155	-0.0204	-0.0269	-0.0376
E ↑	hold_rising to CP	0.0058	0.0036	-0.0013	-0.0035
E ↓	setup_rising to CP	0.0424	0.0473	0.0576	0.0641
E ↑	setup_rising to CP	0.0293	0.0310	0.0417	0.0482
TE ↓	hold_rising to CP	-0.0154	-0.0202	-0.0306	-0.0376
TE ↑	hold_rising to CP	0.0036	0.0010	-0.0039	-0.0067
TE ↓	setup_rising to CP	0.0431	0.0448	0.0550	0.0648
TE ↑	setup_rising to CP	0.0293	0.0368	0.0438	0.0540
		C12T28SOI_-LLP_-CNHLSX71_P0	C12T28SOI_-LLP_-CNHLSX71_P4	C12T28SOI_-LLP_-CNHLSX71_P10	C12T28SOI_-LLP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0349	0.0394	0.0474	0.0549
E ↓	hold_rising to CP	-0.0155	-0.0230	-0.0269	-0.0376
E ↑	hold_rising to CP	0.0058	0.0036	-0.0013	-0.0035
E ↓	setup_rising to CP	0.0425	0.0473	0.0576	0.0641
E ↑	setup_rising to CP	0.0293	0.0342	0.0417	0.0514
TE ↓	hold_rising to CP	-0.0154	-0.0202	-0.0306	-0.0376
TE ↑	hold_rising to CP	0.0036	-0.0017	-0.0039	-0.0067
TE ↓	setup_rising to CP	0.0431	0.0506	0.0545	0.0648
TE ↑	setup_rising to CP	0.0319	0.0368	0.0433	0.0535

		C12T28SOI_-LLP_-CNHLSX93_P0	C12T28SOI_-LLP_-CNHLSX93_P4	C12T28SOI_-LLP_-CNHLSX93_P10	C12T28SOI_-LLP_-CNHLSX93_P16
CP ↓	min_pulse_width to CP	0.0348	0.0412	0.0504	0.0597
E ↓	hold_rising to CP	-0.0176	-0.0230	-0.0328	-0.0372
E ↑	hold_rising to CP	0.0058	0.0036	-0.0013	-0.0035
E ↓	setup_rising to CP	0.0457	0.0501	0.0572	0.0674
E ↑	setup_rising to CP	0.0288	0.0368	0.0465	0.0563
TE ↓	hold_rising to CP	-0.0181	-0.0198	-0.0301	-0.0403
TE ↑	hold_rising to CP	0.0036	0.0010	-0.0039	-0.0067
TE ↓	setup_rising to CP	0.0457	0.0506	0.0604	0.0669
TE ↑	setup_rising to CP	0.0314	0.0362	0.0465	0.0589
		C12T28SOI_-LLPHP_-CNHLSX29_P0	C12T28SOI_-LLPHP_-CNHLSX29_P4	C12T28SOI_-LLPHP_-CNHLSX29_P10	C12T28SOI_-LLPHP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0400	0.0481	0.0580	0.0714
E ↓	hold_rising to CP	0.0026	0.0004	-0.0045	-0.0041
E ↑	hold_rising to CP	0.0269	0.0296	0.0292	0.0319
E ↓	setup_rising to CP	0.0317	0.0338	0.0440	0.0489
E ↑	setup_rising to CP	0.0200	0.0249	0.0320	0.0368
TE ↓	hold_rising to CP	0.0026	0.0032	-0.0023	-0.0072
TE ↑	hold_rising to CP	0.0243	0.0270	0.0270	0.0323
TE ↓	setup_rising to CP	0.0322	0.0370	0.0419	0.0490
TE ↑	setup_rising to CP	0.0191	0.0244	0.0319	0.0394
		C12T28SOI_-LLPHP_-CNHLSX36_P0	C12T28SOI_-LLPHP_-CNHLSX36_P4	C12T28SOI_-LLPHP_-CNHLSX36_P10	C12T28SOI_-LLPHP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0400	0.0481	0.0580	0.0714
E ↓	hold_rising to CP	0.0026	0.0004	-0.0045	-0.0067
E ↑	hold_rising to CP	0.0269	0.0296	0.0292	0.0319
E ↓	setup_rising to CP	0.0317	0.0366	0.0440	0.0489
E ↑	setup_rising to CP	0.0200	0.0249	0.0320	0.0368
TE ↓	hold_rising to CP	0.0026	0.0036	-0.0023	-0.0072
TE ↑	hold_rising to CP	0.0243	0.0270	0.0270	0.0323
TE ↓	setup_rising to CP	0.0322	0.0370	0.0415	0.0490
TE ↑	setup_rising to CP	0.0196	0.0245	0.0319	0.0394

		C12T28SOI_-LLPHP_-CNHLSX44_P0	C12T28SOI_-LLPHP_-CNHLSX44_P4	C12T28SOI_-LLPHP_-CNHLSX44_P10	C12T28SOI_-LLPHP_-CNHLSX44_P16
CP ↓	min_pulse_width to CP	0.0417	0.0487	0.0621	0.0721
E ↓	hold_rising to CP	0.0031	0.0004	-0.0045	-0.0067
E ↑	hold_rising to CP	0.0269	0.0297	0.0292	0.0319
E ↓	setup_rising to CP	0.0317	0.0365	0.0440	0.0485
E ↑	setup_rising to CP	0.0195	0.0245	0.0320	0.0394
TE ↓	hold_rising to CP	0.0026	0.0036	-0.0018	-0.0072
TE ↑	hold_rising to CP	0.0243	0.0270	0.0270	0.0297
TE ↓	setup_rising to CP	0.0312	0.0366	0.0415	0.0516
TE ↑	setup_rising to CP	0.0191	0.0271	0.0319	0.0417
		C12T28SOI_-LLPHP_-CNHLSX51_P0	C12T28SOI_-LLPHP_-CNHLSX51_P4	C12T28SOI_-LLPHP_-CNHLSX51_P10	C12T28SOI_-LLPHP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0417	0.0494	0.0604	0.0721
E ↓	hold_rising to CP	0.0031	0.0004	-0.0045	-0.0067
E ↑	hold_rising to CP	0.0269	0.0296	0.0292	0.0319
E ↓	setup_rising to CP	0.0317	0.0366	0.0440	0.0489
E ↑	setup_rising to CP	0.0195	0.0245	0.0320	0.0394
TE ↓	hold_rising to CP	0.0026	0.0036	-0.0018	-0.0072
TE ↑	hold_rising to CP	0.0243	0.0270	0.0270	0.0297
TE ↓	setup_rising to CP	0.0322	0.0370	0.0415	0.0490
TE ↑	setup_rising to CP	0.0191	0.0271	0.0319	0.0417
		C12T28SOI_-LLPHP_-CNHLSX58_P0	C12T28SOI_-LLPHP_-CNHLSX58_P4	C12T28SOI_-LLPHP_-CNHLSX58_P10	C12T28SOI_-LLPHP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0434	0.0494	0.0628	0.0761
E ↓	hold_rising to CP	0.0031	0.0010	-0.0045	-0.0094
E ↑	hold_rising to CP	0.0269	0.0297	0.0292	0.0319
E ↓	setup_rising to CP	0.0365	0.0414	0.0489	0.0533
E ↑	setup_rising to CP	0.0191	0.0245	0.0320	0.0417
TE ↓	hold_rising to CP	0.0032	-0.0023	-0.0039	-0.0094
TE ↑	hold_rising to CP	0.0243	0.0270	0.0270	0.0297
TE ↓	setup_rising to CP	0.0370	0.0419	0.0463	0.0565
TE ↑	setup_rising to CP	0.0217	0.0271	0.0336	0.0417

		C12T28SOI_-LLPHP_-CNHLSX71_P0	C12T28SOI_-LLPHP_-CNHLSX71_P4	C12T28SOI_-LLPHP_-CNHLSX71_P10	C12T28SOI_-LLPHP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0448	0.0535	0.0669	0.0809
E ↓	hold_rising to CP	-0.0018	-0.0045	-0.0094	-0.0143
E ↑	hold_rising to CP	0.0243	0.0276	0.0270	0.0319
E ↓	setup_rising to CP	0.0386	0.0435	0.0538	0.0582
E ↑	setup_rising to CP	0.0249	0.0298	0.0368	0.0438
TE ↓	hold_rising to CP	-0.0022	-0.0013	-0.0094	-0.0143
TE ↑	hold_rising to CP	0.0244	0.0244	0.0270	0.0297
TE ↓	setup_rising to CP	0.0393	0.0442	0.0512	0.0614
TE ↑	setup_rising to CP	0.0245	0.0293	0.0368	0.0465
		C12T28SOI_-LLPHP_-CNHLSX86_P0	C12T28SOI_-LLPHP_-CNHLSX86_P4	C12T28SOI_-LLPHP_-CNHLSX86_P10	C12T28SOI_-LLPHP_-CNHLSX86_P16
CP ↓	min_pulse_width to CP	0.0449	0.0542	0.0668	0.0809
E ↓	hold_rising to CP	0.0010	-0.0018	-0.0035	-0.0089
E ↑	hold_rising to CP	0.0243	0.0270	0.0297	0.0319
E ↓	setup_rising to CP	0.0386	0.0440	0.0479	0.0586
E ↑	setup_rising to CP	0.0249	0.0298	0.0369	0.0466
TE ↓	hold_rising to CP	0.0004	-0.0023	-0.0072	-0.0121
TE ↑	hold_rising to CP	0.0244	0.0276	0.0270	0.0297
TE ↓	setup_rising to CP	0.0361	0.0409	0.0517	0.0587
TE ↑	setup_rising to CP	0.0249	0.0293	0.0368	0.0465

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LLP_CNHLSX7_P0	2.719e-04	1.000e-20
C12T28SOI_LLP_CNHLSX7_P4	9.512e-05	1.000e-20
C12T28SOI_LLP_CNHLSX7_P10	2.954e-05	1.000e-20
C12T28SOI_LLP_CNHLSX7_P16	1.335e-05	1.000e-20
C12T28SOI_LLP_CNHLSX15_P0	3.780e-04	1.000e-20
C12T28SOI_LLP_CNHLSX15_P4	1.312e-04	1.000e-20
C12T28SOI_LLP_CNHLSX15_P10	4.029e-05	1.000e-20
C12T28SOI_LLP_CNHLSX15_P16	1.805e-05	1.000e-20
C12T28SOI_LLP_CNHLSX22_P0	4.655e-04	1.000e-20
C12T28SOI_LLP_CNHLSX22_P4	1.599e-04	1.000e-20
C12T28SOI_LLP_CNHLSX22_P10	4.847e-05	1.000e-20
C12T28SOI_LLP_CNHLSX22_P16	2.150e-05	1.000e-20
C12T28SOI_LLP_CNHLSX29_P0	5.247e-04	1.000e-20
C12T28SOI_LLP_CNHLSX29_P4	1.803e-04	1.000e-20
C12T28SOI_LLP_CNHLSX29_P10	5.473e-05	1.000e-20
C12T28SOI_LLP_CNHLSX29_P16	2.429e-05	1.000e-20

C12T28SOI_LLP_CNHLSX36_P0	6.007e-04	1.000e-20
C12T28SOI_LLP_CNHLSX36_P4	2.061e-04	1.000e-20
C12T28SOI_LLP_CNHLSX36_P10	6.246e-05	1.000e-20
C12T28SOI_LLP_CNHLSX36_P16	2.769e-05	1.000e-20
C12T28SOI_LLP_CNHLSX51_P0	7.540e-04	1.000e-20
C12T28SOI_LLP_CNHLSX51_P4	2.594e-04	1.000e-20
C12T28SOI_LLP_CNHLSX51_P10	7.869e-05	1.000e-20
C12T28SOI_LLP_CNHLSX51_P16	3.489e-05	1.000e-20
C12T28SOI_LLP_CNHLSX58_P0	9.203e-04	1.000e-20
C12T28SOI_LLP_CNHLSX58_P4	3.166e-04	1.000e-20
C12T28SOI_LLP_CNHLSX58_P10	9.617e-05	1.000e-20
C12T28SOI_LLP_CNHLSX58_P16	4.272e-05	1.000e-20
C12T28SOI_LLP_CNHLSX71_P0	1.087e-03	1.000e-20
C12T28SOI_LLP_CNHLSX71_P4	3.738e-04	1.000e-20
C12T28SOI_LLP_CNHLSX71_P10	1.134e-04	1.000e-20
C12T28SOI_LLP_CNHLSX71_P16	5.028e-05	1.000e-20
C12T28SOI_LLP_CNHLSX93_P0	1.332e-03	1.000e-20
C12T28SOI_LLP_CNHLSX93_P4	4.579e-04	1.000e-20
C12T28SOI_LLP_CNHLSX93_P10	1.387e-04	1.000e-20
C12T28SOI_LLP_CNHLSX93_P16	6.143e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P0	5.953e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P4	2.056e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P10	6.282e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P16	2.805e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P0	6.706e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P4	2.312e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P10	7.052e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P16	3.144e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P0	7.688e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P4	2.655e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P10	8.097e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P16	3.605e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P0	8.331e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P4	2.871e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P10	8.733e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P16	3.880e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P0	9.893e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P4	3.411e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P10	1.040e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P16	4.630e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P0	1.164e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P4	4.001e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P10	1.215e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P16	5.399e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P0	1.338e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P4	4.609e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P10	1.401e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P16	6.222e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LLP_-CNHLSX7_P0	C12T28SOI_LLP_-CNHLSX7_P4	C12T28SOI_LLP_-CNHLSX7_P10	C12T28SOI_LLP_-CNHLSX7_P16

CP (output stable)	1.913e-03	1.893e-03	1.931e-03	1.993e-03
E (output stable)	1.045e-03	9.969e-04	9.772e-04	9.812e-04
TE (output stable)	1.114e-03	1.081e-03	1.084e-03	1.106e-03
CP to Q	2.842e-03	2.713e-03	2.680e-03	2.720e-03
	C12T28SOI_LLP_-CNHLSX15_P0	C12T28SOI_LLP_-CNHLSX15_P4	C12T28SOI_LLP_-CNHLSX15_P10	C12T28SOI_LLP_-CNHLSX15_P16
CP (output stable)	2.211e-03	2.199e-03	2.259e-03	2.337e-03
E (output stable)	1.068e-03	1.024e-03	1.008e-03	1.017e-03
TE (output stable)	1.137e-03	1.107e-03	1.114e-03	1.142e-03
CP to Q	4.227e-03	3.989e-03	3.963e-03	3.993e-03
	C12T28SOI_LLP_-CNHLSX22_P0	C12T28SOI_LLP_-CNHLSX22_P4	C12T28SOI_LLP_-CNHLSX22_P10	C12T28SOI_LLP_-CNHLSX22_P16
CP (output stable)	2.466e-03	2.462e-03	2.531e-03	2.623e-03
E (output stable)	1.143e-03	1.099e-03	1.085e-03	1.095e-03
TE (output stable)	1.212e-03	1.182e-03	1.191e-03	1.220e-03
CP to Q	5.499e-03	5.199e-03	5.103e-03	5.201e-03
	C12T28SOI_LLP_-CNHLSX29_P0	C12T28SOI_LLP_-CNHLSX29_P4	C12T28SOI_LLP_-CNHLSX29_P10	C12T28SOI_LLP_-CNHLSX29_P16
CP (output stable)	2.561e-03	2.568e-03	2.649e-03	2.766e-03
E (output stable)	1.165e-03	1.119e-03	1.104e-03	1.114e-03
TE (output stable)	1.234e-03	1.203e-03	1.211e-03	1.239e-03
CP to Q	6.746e-03	6.385e-03	6.189e-03	6.331e-03
	C12T28SOI_LLP_-CNHLSX36_P0	C12T28SOI_LLP_-CNHLSX36_P4	C12T28SOI_LLP_-CNHLSX36_P10	C12T28SOI_LLP_-CNHLSX36_P16
CP (output stable)	2.735e-03	2.736e-03	2.840e-03	2.957e-03
E (output stable)	1.168e-03	1.122e-03	1.108e-03	1.119e-03
TE (output stable)	1.236e-03	1.206e-03	1.214e-03	1.244e-03
CP to Q	7.848e-03	7.387e-03	7.285e-03	7.433e-03
	C12T28SOI_LLP_-CNHLSX51_P0	C12T28SOI_LLP_-CNHLSX51_P4	C12T28SOI_LLP_-CNHLSX51_P10	C12T28SOI_LLP_-CNHLSX51_P16
CP (output stable)	2.978e-03	3.007e-03	3.136e-03	3.308e-03
E (output stable)	1.164e-03	1.125e-03	1.117e-03	1.133e-03
TE (output stable)	1.233e-03	1.208e-03	1.223e-03	1.258e-03
CP to Q	1.068e-02	1.012e-02	9.943e-03	1.007e-02
	C12T28SOI_LLP_-CNHLSX58_P0	C12T28SOI_LLP_-CNHLSX58_P4	C12T28SOI_LLP_-CNHLSX58_P10	C12T28SOI_LLP_-CNHLSX58_P16
CP (output stable)	3.870e-03	3.933e-03	4.086e-03	4.308e-03
E (output stable)	1.279e-03	1.243e-03	1.239e-03	1.260e-03
TE (output stable)	1.347e-03	1.325e-03	1.344e-03	1.383e-03
CP to Q	1.215e-02	1.146e-02	1.117e-02	1.130e-02
	C12T28SOI_LLP_-CNHLSX71_P0	C12T28SOI_LLP_-CNHLSX71_P4	C12T28SOI_LLP_-CNHLSX71_P10	C12T28SOI_LLP_-CNHLSX71_P16
CP (output stable)	4.327e-03	4.421e-03	4.634e-03	4.887e-03
E (output stable)	1.318e-03	1.284e-03	1.285e-03	1.310e-03
TE (output stable)	1.386e-03	1.366e-03	1.389e-03	1.433e-03
CP to Q	1.482e-02	1.406e-02	1.387e-02	1.392e-02
	C12T28SOI_LLP_-CNHLSX93_P0	C12T28SOI_LLP_-CNHLSX93_P4	C12T28SOI_LLP_-CNHLSX93_P10	C12T28SOI_LLP_-CNHLSX93_P16
CP (output stable)	4.917e-03	5.013e-03	5.312e-03	5.623e-03
E (output stable)	1.409e-03	1.377e-03	1.385e-03	1.417e-03
TE (output stable)	1.478e-03	1.460e-03	1.490e-03	1.541e-03
CP to Q	1.946e-02	1.810e-02	1.782e-02	1.804e-02

	C12T28SOI_LLPHP_-CNHLSX29_P0	C12T28SOI_LLPHP_-CNHLSX29_P4	C12T28SOI_LLPHP_-CNHLSX29_P10	C12T28SOI_LLPHP_-CNHLSX29_P16
CP (output stable)	3.576e-03	3.630e-03	3.756e-03	3.918e-03
E (output stable)	1.102e-03	1.050e-03	1.028e-03	1.033e-03
TE (output stable)	1.170e-03	1.133e-03	1.134e-03	1.159e-03
CP to Q	8.127e-03	7.770e-03	7.680e-03	7.835e-03
	C12T28SOI_LLPHP_-CNHLSX36_P0	C12T28SOI_LLPHP_-CNHLSX36_P4	C12T28SOI_LLPHP_-CNHLSX36_P10	C12T28SOI_LLPHP_-CNHLSX36_P16
CP (output stable)	3.726e-03	3.785e-03	3.925e-03	4.103e-03
E (output stable)	1.108e-03	1.055e-03	1.035e-03	1.042e-03
TE (output stable)	1.175e-03	1.138e-03	1.141e-03	1.168e-03
CP to Q	9.205e-03	8.810e-03	8.726e-03	8.900e-03
	C12T28SOI_LLPHP_-CNHLSX44_P0	C12T28SOI_LLPHP_-CNHLSX44_P4	C12T28SOI_LLPHP_-CNHLSX44_P10	C12T28SOI_LLPHP_-CNHLSX44_P16
CP (output stable)	3.998e-03	4.073e-03	4.239e-03	4.419e-03
E (output stable)	1.141e-03	1.091e-03	1.075e-03	1.084e-03
TE (output stable)	1.208e-03	1.174e-03	1.181e-03	1.210e-03
CP to Q	1.067e-02	1.009e-02	9.997e-03	1.007e-02
	C12T28SOI_LLPHP_-CNHLSX51_P0	C12T28SOI_LLPHP_-CNHLSX51_P4	C12T28SOI_LLPHP_-CNHLSX51_P10	C12T28SOI_LLPHP_-CNHLSX51_P16
CP (output stable)	4.022e-03	4.064e-03	4.234e-03	4.439e-03
E (output stable)	1.141e-03	1.091e-03	1.075e-03	1.084e-03
TE (output stable)	1.208e-03	1.174e-03	1.181e-03	1.210e-03
CP to Q	1.192e-02	1.130e-02	1.099e-02	1.122e-02
	C12T28SOI_LLPHP_-CNHLSX58_P0	C12T28SOI_LLPHP_-CNHLSX58_P4	C12T28SOI_LLPHP_-CNHLSX58_P10	C12T28SOI_LLPHP_-CNHLSX58_P16
CP (output stable)	4.657e-03	4.752e-03	4.984e-03	5.232e-03
E (output stable)	1.194e-03	1.146e-03	1.135e-03	1.150e-03
TE (output stable)	1.261e-03	1.229e-03	1.241e-03	1.276e-03
CP to Q	1.296e-02	1.223e-02	1.194e-02	1.227e-02
	C12T28SOI_LLPHP_-CNHLSX71_P0	C12T28SOI_LLPHP_-CNHLSX71_P4	C12T28SOI_LLPHP_-CNHLSX71_P10	C12T28SOI_LLPHP_-CNHLSX71_P16
CP (output stable)	5.190e-03	5.313e-03	5.566e-03	5.874e-03
E (output stable)	1.282e-03	1.236e-03	1.227e-03	1.244e-03
TE (output stable)	1.349e-03	1.319e-03	1.333e-03	1.370e-03
CP to Q	1.549e-02	1.487e-02	1.442e-02	1.474e-02
	C12T28SOI_LLPHP_-CNHLSX86_P0	C12T28SOI_LLPHP_-CNHLSX86_P4	C12T28SOI_LLPHP_-CNHLSX86_P10	C12T28SOI_LLPHP_-CNHLSX86_P16
CP (output stable)	5.626e-03	5.758e-03	6.053e-03	6.411e-03
E (output stable)	1.300e-03	1.259e-03	1.261e-03	1.286e-03
TE (output stable)	1.367e-03	1.343e-03	1.367e-03	1.412e-03
CP to Q	1.797e-02	1.710e-02	1.673e-02	1.702e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LLP_-CNHLSX7_P0	C12T28SOI_LLP_-CNHLSX7_P4	C12T28SOI_LLP_-CNHLSX7_P10	C12T28SOI_LLP_-CNHLSX7_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX15_P0	C12T28SOI_LLP_-CNHLSX15_P4	C12T28SOI_LLP_-CNHLSX15_P10	C12T28SOI_LLP_-CNHLSX15_P16

CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX22_P0	C12T28SOI_LLP_-CNHLSX22_P4	C12T28SOI_LLP_-CNHLSX22_P10	C12T28SOI_LLP_-CNHLSX22_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX29_P0	C12T28SOI_LLP_-CNHLSX29_P4	C12T28SOI_LLP_-CNHLSX29_P10	C12T28SOI_LLP_-CNHLSX29_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX36_P0	C12T28SOI_LLP_-CNHLSX36_P4	C12T28SOI_LLP_-CNHLSX36_P10	C12T28SOI_LLP_-CNHLSX36_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX51_P0	C12T28SOI_LLP_-CNHLSX51_P4	C12T28SOI_LLP_-CNHLSX51_P10	C12T28SOI_LLP_-CNHLSX51_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX58_P0	C12T28SOI_LLP_-CNHLSX58_P4	C12T28SOI_LLP_-CNHLSX58_P10	C12T28SOI_LLP_-CNHLSX58_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX71_P0	C12T28SOI_LLP_-CNHLSX71_P4	C12T28SOI_LLP_-CNHLSX71_P10	C12T28SOI_LLP_-CNHLSX71_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX93_P0	C12T28SOI_LLP_-CNHLSX93_P4	C12T28SOI_LLP_-CNHLSX93_P10	C12T28SOI_LLP_-CNHLSX93_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX29_P0	C12T28SOI_LLPHP_-CNHLSX29_P4	C12T28SOI_LLPHP_-CNHLSX29_P10	C12T28SOI_LLPHP_-CNHLSX29_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

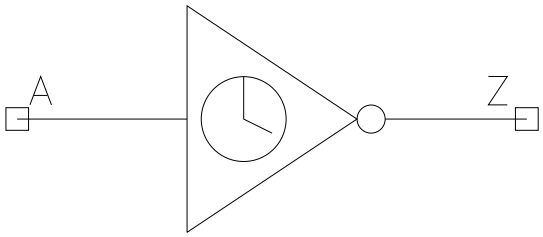
	C12T28SOI_LLPHP_-CNHLSX36_P0	C12T28SOI_LLPHP_-CNHLSX36_P4	C12T28SOI_LLPHP_-CNHLSX36_P10	C12T28SOI_LLPHP_-CNHLSX36_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX44_P0	C12T28SOI_LLPHP_-CNHLSX44_P4	C12T28SOI_LLPHP_-CNHLSX44_P10	C12T28SOI_LLPHP_-CNHLSX44_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX51_P0	C12T28SOI_LLPHP_-CNHLSX51_P4	C12T28SOI_LLPHP_-CNHLSX51_P10	C12T28SOI_LLPHP_-CNHLSX51_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX58_P0	C12T28SOI_LLPHP_-CNHLSX58_P4	C12T28SOI_LLPHP_-CNHLSX58_P10	C12T28SOI_LLPHP_-CNHLSX58_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX71_P0	C12T28SOI_LLPHP_-CNHLSX71_P4	C12T28SOI_LLPHP_-CNHLSX71_P10	C12T28SOI_LLPHP_-CNHLSX71_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX86_P0	C12T28SOI_LLPHP_-CNHLSX86_P4	C12T28SOI_LLPHP_-CNHLSX86_P10	C12T28SOI_LLPHP_-CNHLSX86_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNIV

Cell Description

Inverter with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.272	0.3264
X5_P4	1.200	0.272	0.3264
X5_P10	1.200	0.272	0.3264
X5_P16	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X16_P0	1.200	0.408	0.4896
X16_P4	1.200	0.408	0.4896
X16_P10	1.200	0.408	0.4896
X16_P16	1.200	0.408	0.4896
X23_P0	1.200	0.544	0.6528
X23_P4	1.200	0.544	0.6528
X23_P10	1.200	0.544	0.6528
X23_P16	1.200	0.544	0.6528
X31_P0	1.200	0.680	0.8160
X31_P4	1.200	0.680	0.8160
X31_P10	1.200	0.680	0.8160
X31_P16	1.200	0.680	0.8160
X39_P0	1.200	0.816	0.9792
X39_P4	1.200	0.816	0.9792
X39_P10	1.200	0.816	0.9792
X39_P16	1.200	0.816	0.9792
X47_P0	1.200	0.952	1.1424
X47_P4	1.200	0.952	1.1424
X47_P10	1.200	0.952	1.1424
X47_P16	1.200	0.952	1.1424
X55_P0	1.200	1.088	1.3056
X55_P4	1.200	1.088	1.3056
X55_P10	1.200	1.088	1.3056
X55_P16	1.200	1.088	1.3056
X61_P0	1.200	1.224	1.4688

X61_P4	1.200	1.224	1.4688
X61_P10	1.200	1.224	1.4688
X61_P16	1.200	1.224	1.4688
X70_P0	1.200	1.360	1.6320
X70_P4	1.200	1.360	1.6320
X70_P10	1.200	1.360	1.6320
X70_P16	1.200	1.360	1.6320
X94_P0	1.200	1.768	2.1216
X94_P4	1.200	1.768	2.1216
X94_P10	1.200	1.768	2.1216
X94_P16	1.200	1.768	2.1216
X133_P0	1.200	2.448	2.9376
X133_P4	1.200	2.448	2.9376
X133_P10	1.200	2.448	2.9376
X133_P16	1.200	2.448	2.9376

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X5_P0	X5_P4	X5_P10	X5_P16
A	0.0005	0.0005	0.0006	0.0006
	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0007	0.0008	0.0008	0.0009
	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0014	0.0014	0.0015	0.0016
	X23_P0	X23_P4	X23_P10	X23_P16
A	0.0021	0.0021	0.0023	0.0024
	X31_P0	X31_P4	X31_P10	X31_P16
A	0.0027	0.0028	0.0030	0.0032
	X39_P0	X39_P4	X39_P10	X39_P16
A	0.0034	0.0035	0.0038	0.0040
	X47_P0	X47_P4	X47_P10	X47_P16
A	0.0042	0.0043	0.0046	0.0048
	X55_P0	X55_P4	X55_P10	X55_P16
A	0.0048	0.0050	0.0053	0.0055
	X61_P0	X61_P4	X61_P10	X61_P16
A	0.0053	0.0055	0.0059	0.0063
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0063	0.0065	0.0069	0.0073
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0087	0.0090	0.0095	0.0100
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0128	0.0132	0.0140	0.0145

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X5_P4	X5_P0	X5_P4
A to Z ↓	0.0061	0.0073	3.6962	3.9842

A to Z ↑	0.0113	0.0125	5.5465	6.2437
	X5_P10	**X5_P16**	**X5_P10**	**X5_P16**
A to Z ↓	0.0088	0.0100	4.3845	4.7495
A to Z ↑	0.0143	0.0159	7.2848	8.2680
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0059	0.0069	2.3212	2.5037
A to Z ↑	0.0086	0.0098	2.9643	3.3307
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0082	0.0093	2.7591	2.9891
A to Z ↑	0.0113	0.0127	3.8890	4.4026
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0047	0.0056	1.1396	1.2295
A to Z ↑	0.0075	0.0084	1.4800	1.6618
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0068	0.0078	1.3553	1.4676
A to Z ↑	0.0098	0.0109	1.9385	2.1930
	X23_P0	**X23_P4**	**X23_P0**	**X23_P4**
A to Z ↓	0.0052	0.0062	0.8110	0.8750
A to Z ↑	0.0075	0.0085	1.0048	1.1277
	X23_P10	**X23_P16**	**X23_P10**	**X23_P16**
A to Z ↓	0.0074	0.0084	0.9651	1.0452
A to Z ↑	0.0100	0.0112	1.3136	1.4848
	X31_P0	**X31_P4**	**X31_P0**	**X31_P4**
A to Z ↓	0.0049	0.0057	0.5870	0.6334
A to Z ↑	0.0072	0.0081	0.7508	0.8432
	X31_P10	**X31_P16**	**X31_P10**	**X31_P16**
A to Z ↓	0.0068	0.0079	0.6992	0.7569
A to Z ↑	0.0094	0.0107	0.9808	1.1103
	X39_P0	**X39_P4**	**X39_P0**	**X39_P4**
A to Z ↓	0.0052	0.0061	0.4742	0.5116
A to Z ↑	0.0075	0.0084	0.6045	0.6782
	X39_P10	**X39_P16**	**X39_P10**	**X39_P16**
A to Z ↓	0.0074	0.0084	0.5649	0.6120
A to Z ↑	0.0099	0.0111	0.7894	0.8922
	X47_P0	**X47_P4**	**X47_P0**	**X47_P4**
A to Z ↓	0.0052	0.0061	0.3946	0.4260
A to Z ↑	0.0074	0.0084	0.5039	0.5645
	X47_P10	**X47_P16**	**X47_P10**	**X47_P16**
A to Z ↓	0.0072	0.0083	0.4704	0.5098
A to Z ↑	0.0097	0.0110	0.6576	0.7431
	X55_P0	**X55_P4**	**X55_P0**	**X55_P4**
A to Z ↓	0.0055	0.0065	0.3399	0.3671
A to Z ↑	0.0077	0.0086	0.4324	0.4851
	X55_P10	**X55_P16**	**X55_P10**	**X55_P16**
A to Z ↓	0.0077	0.0087	0.4058	0.4398
A to Z ↑	0.0101	0.0112	0.5644	0.6375
	X61_P0	**X61_P4**	**X61_P0**	**X61_P4**
A to Z ↓	0.0056	0.0065	0.3061	0.3303
A to Z ↑	0.0078	0.0087	0.3916	0.4396
	X61_P10	**X61_P16**	**X61_P10**	**X61_P16**
A to Z ↓	0.0077	0.0088	0.3651	0.3955
A to Z ↑	0.0101	0.0114	0.5115	0.5787

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0060	0.0069	0.2681	0.2895
A to Z ↑	0.0081	0.0090	0.3398	0.3810
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0081	0.0092	0.3194	0.3461
A to Z ↑	0.0104	0.0117	0.4426	0.4994
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0071	0.0080	0.2054	0.2217
A to Z ↑	0.0091	0.0099	0.2583	0.2893
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0093	0.0104	0.2444	0.2646
A to Z ↑	0.0114	0.0126	0.3359	0.3792
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0087	0.0095	0.1510	0.1627
A to Z ↑	0.0105	0.0113	0.1863	0.2085
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0109	0.0121	0.1794	0.1938
A to Z ↑	0.0130	0.0144	0.2416	0.2719

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P0	2.960e-05	1.000e-20
X5_P4	1.063e-05	1.000e-20
X5_P10	3.423e-06	1.000e-20
X5_P16	1.591e-06	1.000e-20
X8_P0	6.374e-05	1.000e-20
X8_P4	2.225e-05	1.000e-20
X8_P10	6.868e-06	1.000e-20
X8_P16	3.086e-06	1.000e-20
X16_P0	1.290e-04	1.000e-20
X16_P4	4.483e-05	1.000e-20
X16_P10	1.375e-05	1.000e-20
X16_P16	6.151e-06	1.000e-20
X23_P0	1.828e-04	1.000e-20
X23_P4	6.339e-05	1.000e-20
X23_P10	1.937e-05	1.000e-20
X23_P16	8.636e-06	1.000e-20
X31_P0	2.472e-04	1.000e-20
X31_P4	8.536e-05	1.000e-20
X31_P10	2.596e-05	1.000e-20
X31_P16	1.153e-05	1.000e-20
X39_P0	3.039e-04	1.000e-20
X39_P4	1.050e-04	1.000e-20
X39_P10	3.191e-05	1.000e-20
X39_P16	1.416e-05	1.000e-20
X47_P0	3.565e-04	1.000e-20
X47_P4	1.235e-04	1.000e-20
X47_P10	3.766e-05	1.000e-20
X47_P16	1.673e-05	1.000e-20
X55_P0	4.205e-04	1.000e-20
X55_P4	1.450e-04	1.000e-20
X55_P10	4.397e-05	1.000e-20

X55_P16	1.948e-05	1.000e-20
X61_P0	4.632e-04	1.000e-20
X61_P4	1.591e-04	1.000e-20
X61_P10	4.814e-05	1.000e-20
X61_P16	2.130e-05	1.000e-20
X70_P0	5.279e-04	1.000e-20
X70_P4	1.827e-04	1.000e-20
X70_P10	5.559e-05	1.000e-20
X70_P16	2.466e-05	1.000e-20
X94_P0	6.994e-04	1.000e-20
X94_P4	2.419e-04	1.000e-20
X94_P10	7.352e-05	1.000e-20
X94_P16	3.258e-05	1.000e-20
X133_P0	1.018e-03	1.000e-20
X133_P4	3.491e-04	1.000e-20
X133_P10	1.052e-04	1.000e-20
X133_P16	4.638e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	5.643e-04	4.802e-04	4.236e-04	3.993e-04
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	9.080e-04	7.443e-04	6.232e-04	5.721e-04
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	1.695e-03	1.344e-03	1.078e-03	9.507e-04
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	2.524e-03	2.031e-03	1.657e-03	1.479e-03
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	3.311e-03	2.603e-03	2.051e-03	1.835e-03
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	4.180e-03	3.323e-03	2.685e-03	2.391e-03
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	4.954e-03	3.943e-03	3.152e-03	2.809e-03
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	5.875e-03	4.672e-03	3.786e-03	3.353e-03
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	6.453e-03	5.091e-03	4.090e-03	3.614e-03
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	7.559e-03	5.998e-03	4.835e-03	4.298e-03
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	1.035e-02	8.140e-03	6.509e-03	5.739e-03
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	1.590e-02	1.246e-02	1.002e-02	8.822e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

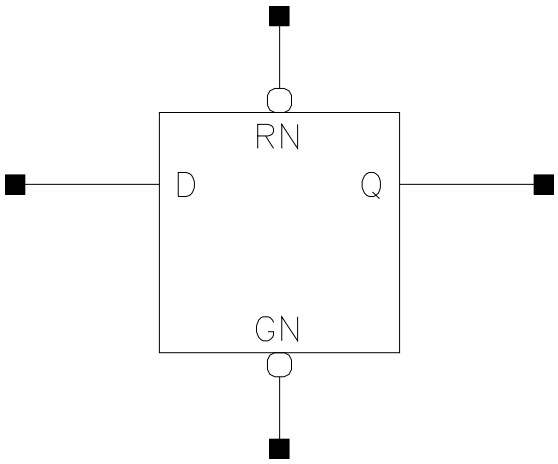
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNLDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
D	0.0011	0.0011	0.0012	0.0012
GN	0.0021	0.0022	0.0023	0.0024
RN	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	X33_P4	X33_P0	X33_P4

D to Q ↓	0.0453	0.0519	0.5471	0.5959
D to Q ↑	0.0480	0.0542	0.7753	0.8756
GN to Q ↓	0.0418	0.0477	0.5476	0.5957
GN to Q ↑	0.0523	0.0592	0.7758	0.8759
RN to Q ↓	0.0617	0.0710	0.5665	0.6192
RN to Q ↑	0.0536	0.0603	0.7759	0.8748
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D to Q ↓	0.0625	0.0733	0.6662	0.7300
D to Q ↑	0.0641	0.0740	1.0260	1.1668
GN to Q ↓	0.0568	0.0658	0.6660	0.7301
GN to Q ↑	0.0699	0.0805	1.0266	1.1673
RN to Q ↓	0.0860	0.1011	0.6959	0.7669
RN to Q ↑	0.0708	0.0811	1.0260	1.1672

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X33_P0	X33_P4	X33_P10	X33_P16
D ↓	hold_rising to GN	-0.0046	-0.0091	-0.0194	-0.0259
D ↑	hold_rising to GN	-0.0114	-0.0163	-0.0266	-0.0305
D ↓	setup_rising to GN	0.0499	0.0569	0.0663	0.0786
D ↑	setup_rising to GN	0.0540	0.0611	0.0708	0.0806
GN ↓	min_pulse_width to GN	0.0543	0.0623	0.0745	0.0835
RN ↓	min_pulse_width to RN	0.0735	0.0806	0.0974	0.1121
RN ↑	recovery_rising to GN	0.0579	0.0682	0.0778	0.0902
RN ↑	removal_rising to GN	-0.0359	-0.0440	-0.0537	-0.0608

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X33_P0	4.166e-04	1.000e-20
X33_P4	1.439e-04	1.000e-20
X33_P10	4.391e-05	1.000e-20
X33_P16	1.955e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	5.433e-05	6.334e-05	1.006e-04	1.176e-04
GN (output stable)	1.534e-03	1.445e-03	1.425e-03	1.434e-03
RN (output stable)	7.827e-05	7.283e-05	6.743e-05	6.136e-05
D to Q	1.205e-02	1.117e-02	1.066e-02	1.061e-02
GN to Q	1.471e-02	1.378e-02	1.327e-02	1.326e-02
RN to Q	9.315e-03	8.693e-03	8.353e-03	8.298e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

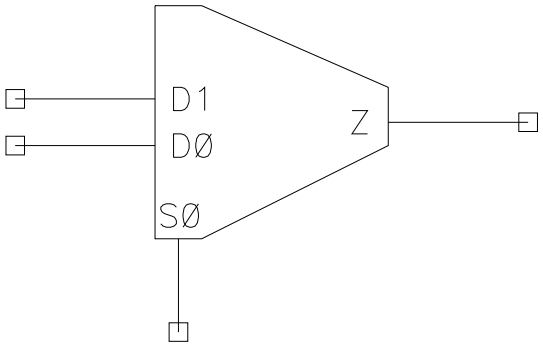
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX21

Cell Description

2:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320
X17_P4	1.200	1.360	1.6320
X17_P10	1.200	1.360	1.6320
X17_P16	1.200	1.360	1.6320
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0010	0.0010	0.0011	0.0011
D1	0.0010	0.0010	0.0011	0.0011
S0	0.0013	0.0014	0.0015	0.0016
	X33_P0	X33_P4	X33_P10	X33_P16
D0	0.0018	0.0018	0.0020	0.0021
D1	0.0017	0.0018	0.0019	0.0021
S0	0.0023	0.0024	0.0025	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X17_P4	X17_P0	X17_P4

D0 to Z ↓	0.0299	0.0339	1.0245	1.1101
D0 to Z ↑	0.0251	0.0283	1.4751	1.6604
D1 to Z ↓	0.0294	0.0334	1.0226	1.1081
D1 to Z ↑	0.0238	0.0267	1.4737	1.6568
S0 to Z ↓	0.0282	0.0319	1.0207	1.1057
S0 to Z ↑	0.0280	0.0316	1.4732	1.6573
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0402	0.0463	1.2326	1.3452
D0 to Z ↑	0.0333	0.0380	1.9395	2.1997
D1 to Z ↓	0.0398	0.0459	1.2306	1.3432
D1 to Z ↑	0.0313	0.0357	1.9351	2.1982
S0 to Z ↓	0.0377	0.0432	1.2294	1.3410
S0 to Z ↑	0.0372	0.0426	1.9372	2.1959
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
D0 to Z ↓	0.0287	0.0328	0.5266	0.5712
D0 to Z ↑	0.0247	0.0280	0.7426	0.8343
D1 to Z ↓	0.0296	0.0338	0.5269	0.5718
D1 to Z ↑	0.0240	0.0271	0.7416	0.8353
S0 to Z ↓	0.0294	0.0334	0.5261	0.5705
S0 to Z ↑	0.0281	0.0319	0.7425	0.8348
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D0 to Z ↓	0.0391	0.0448	0.6354	0.6928
D0 to Z ↑	0.0332	0.0376	0.9749	1.1067
D1 to Z ↓	0.0403	0.0465	0.6360	0.6936
D1 to Z ↑	0.0317	0.0360	0.9761	1.1065
S0 to Z ↓	0.0395	0.0451	0.6348	0.6918
S0 to Z ↑	0.0377	0.0431	0.9757	1.1063

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P0	3.359e-04	1.000e-20
X17_P4	1.176e-04	1.000e-20
X17_P10	3.645e-05	1.000e-20
X17_P16	1.643e-05	1.000e-20
X33_P0	6.591e-04	1.000e-20
X33_P4	2.307e-04	1.000e-20
X33_P10	7.135e-05	1.000e-20
X33_P16	3.209e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	1.328e-03	1.182e-03	1.079e-03	1.035e-03
D1 (output stable)	1.288e-03	1.131e-03	1.020e-03	9.723e-04
S0 (output stable)	1.132e-03	1.094e-03	1.089e-03	1.108e-03
D0 to Z	4.717e-03	4.446e-03	4.363e-03	4.418e-03
D1 to Z	4.612e-03	4.327e-03	4.247e-03	4.297e-03
S0 to Z	5.001e-03	4.735e-03	4.663e-03	4.724e-03
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	2.191e-03	1.876e-03	1.643e-03	1.536e-03
D1 (output stable)	2.255e-03	1.945e-03	1.715e-03	1.613e-03
S0 (output stable)	1.844e-03	1.765e-03	1.743e-03	1.777e-03

D0 to Z	9.193e-03	8.725e-03	8.647e-03	8.658e-03
D1 to Z	9.124e-03	8.650e-03	8.508e-03	8.578e-03
S0 to Z	9.919e-03	9.464e-03	9.385e-03	9.442e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

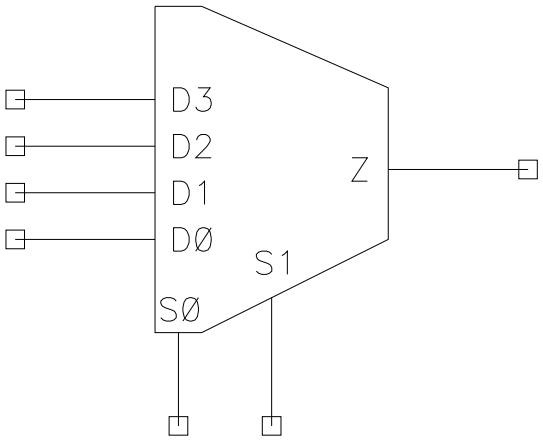
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX41

Cell Description

4:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	2.400	2.176	5.2224
X17_P4	2.400	2.176	5.2224
X17_P10	2.400	2.176	5.2224
X17_P16	2.400	2.176	5.2224
X27_P0	2.400	2.312	5.5488
X27_P4	2.400	2.312	5.5488
X27_P10	2.400	2.312	5.5488
X27_P16	2.400	2.312	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0014	0.0015	0.0016	0.0016
D1	0.0013	0.0014	0.0015	0.0016
D2	0.0014	0.0015	0.0016	0.0016
D3	0.0014	0.0015	0.0015	0.0016
S0	0.0036	0.0038	0.0041	0.0043
S1	0.0021	0.0022	0.0024	0.0025

	X27_P0	X27_P4	X27_P10	X27_P16
D0	0.0013	0.0013	0.0014	0.0015
D1	0.0012	0.0013	0.0014	0.0014
D2	0.0012	0.0013	0.0013	0.0014
D3	0.0012	0.0013	0.0013	0.0014
S0	0.0032	0.0033	0.0036	0.0038
S1	0.0019	0.0020	0.0022	0.0023

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
D0 to Z ↓	0.0453	0.0524	1.0624	1.1515
D0 to Z ↑	0.0363	0.0414	1.5006	1.6866
D1 to Z ↓	0.0448	0.0518	1.0619	1.1515
D1 to Z ↑	0.0360	0.0410	1.4998	1.6883
D2 to Z ↓	0.0463	0.0536	1.0631	1.1520
D2 to Z ↑	0.0360	0.0410	1.4988	1.6876
D3 to Z ↓	0.0458	0.0530	1.0624	1.1522
D3 to Z ↑	0.0357	0.0406	1.4985	1.6848
S0 to Z ↓	0.0545	0.0630	1.0605	1.1493
S0 to Z ↑	0.0476	0.0546	1.5018	1.6893
S1 to Z ↓	0.0371	0.0424	1.0628	1.1519
S1 to Z ↑	0.0362	0.0410	1.5008	1.6881
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0625	0.0731	1.2787	1.3961
D0 to Z ↑	0.0486	0.0559	1.9702	2.2371
D1 to Z ↓	0.0619	0.0723	1.2784	1.3954
D1 to Z ↑	0.0482	0.0555	1.9717	2.2378
D2 to Z ↓	0.0643	0.0750	1.2801	1.3971
D2 to Z ↑	0.0483	0.0554	1.9698	2.2359
D3 to Z ↓	0.0636	0.0742	1.2788	1.3954
D3 to Z ↑	0.0478	0.0549	1.9679	2.2337
S0 to Z ↓	0.0757	0.0884	1.2768	1.3935
S0 to Z ↑	0.0651	0.0756	1.9729	2.2394
S1 to Z ↓	0.0500	0.0579	1.2792	1.3962
S1 to Z ↑	0.0481	0.0551	1.9720	2.2380
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0510	0.0588	0.6729	0.7320
D0 to Z ↑	0.0461	0.0523	1.0125	1.1393
D1 to Z ↓	0.0460	0.0529	0.6639	0.7215
D1 to Z ↑	0.0450	0.0510	1.0128	1.1394
D2 to Z ↓	0.0536	0.0621	0.6759	0.7348
D2 to Z ↑	0.0456	0.0517	1.0126	1.1391
D3 to Z ↓	0.0530	0.0613	0.6752	0.7345
D3 to Z ↑	0.0450	0.0510	1.0122	1.1389
S0 to Z ↓	0.0605	0.0698	0.6704	0.7287
S0 to Z ↑	0.0556	0.0637	1.0142	1.1405
S1 to Z ↓	0.0398	0.0458	0.6730	0.7314
S1 to Z ↑	0.0504	0.0567	1.0122	1.1386
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.0711	0.0826	0.8168	0.8943
D0 to Z ↑	0.0621	0.0711	1.3306	1.5104

D1 to Z ↓	0.0638	0.0740	0.8041	0.8786
D1 to Z ↑	0.0607	0.0696	1.3310	1.5108
D2 to Z ↓	0.0752	0.0872	0.8209	0.8989
D2 to Z ↑	0.0614	0.0701	1.3310	1.5090
D3 to Z ↓	0.0744	0.0863	0.8209	0.8986
D3 to Z ↑	0.0606	0.0692	1.3309	1.5086
S0 to Z ↓	0.0842	0.0977	0.8130	0.8894
S0 to Z ↑	0.0764	0.0881	1.3332	1.5119
S1 to Z ↓	0.0551	0.0634	0.8162	0.8935
S1 to Z ↑	0.0671	0.0767	1.3312	1.5101

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P0	4.499e-04	1.000e-20
X17_P4	1.601e-04	1.000e-20
X17_P10	5.056e-05	1.000e-20
X17_P16	2.310e-05	1.000e-20
X27_P0	4.677e-04	1.000e-20
X27_P4	1.659e-04	1.000e-20
X27_P10	5.226e-05	1.000e-20
X27_P16	2.384e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	1.049e-04	1.015e-04	9.950e-05	7.412e-05
D1 (output stable)	7.844e-05	7.511e-05	7.206e-05	6.155e-05
D2 (output stable)	1.074e-04	1.035e-04	1.005e-04	7.942e-05
D3 (output stable)	1.059e-04	1.023e-04	1.023e-04	9.347e-05
S0 (output stable)	3.025e-03	3.066e-03	3.217e-03	3.403e-03
S1 (output stable)	2.802e-03	2.769e-03	2.818e-03	2.786e-03
D0 to Z	7.086e-03	6.981e-03	7.018e-03	7.234e-03
D1 to Z	7.071e-03	6.965e-03	7.004e-03	7.223e-03
D2 to Z	7.316e-03	7.209e-03	7.284e-03	7.496e-03
D3 to Z	7.214e-03	7.104e-03	7.178e-03	7.390e-03
S0 to Z	1.049e-02	1.051e-02	1.080e-02	1.124e-02
S1 to Z	8.379e-03	8.152e-03	8.035e-03	7.840e-03
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	1.006e-04	9.623e-05	8.897e-05	6.268e-05
D1 (output stable)	7.904e-05	7.557e-05	7.276e-05	6.444e-05
D2 (output stable)	1.001e-04	9.540e-05	8.670e-05	6.704e-05
D3 (output stable)	9.820e-05	9.420e-05	9.304e-05	8.193e-05
S0 (output stable)	2.838e-03	2.858e-03	2.979e-03	3.136e-03
S1 (output stable)	2.494e-03	2.481e-03	2.523e-03	2.502e-03
D0 to Z	9.363e-03	8.914e-03	8.809e-03	8.855e-03
D1 to Z	9.094e-03	8.688e-03	8.615e-03	8.680e-03
D2 to Z	9.551e-03	9.101e-03	9.000e-03	9.011e-03
D3 to Z	9.438e-03	8.989e-03	8.891e-03	8.899e-03
S0 to Z	1.243e-02	1.210e-02	1.219e-02	1.242e-02
S1 to Z	1.037e-02	9.855e-03	9.598e-03	9.267e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

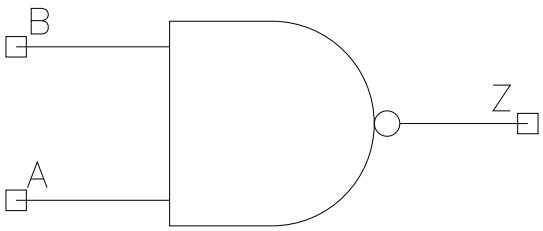
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2

Cell Description

2 input NAND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X33_P0	1.200	1.224	1.4688
X33_P4	1.200	1.224	1.4688
X33_P10	1.200	1.224	1.4688
X33_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0018	0.0019	0.0020	0.0022
B	0.0017	0.0017	0.0018	0.0019
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0007	0.0008	0.0008	0.0008
B	0.0007	0.0007	0.0008	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0070	0.0084	1.4044	1.5255
A to Z ↑	0.0126	0.0142	1.5275	1.7166
B to Z ↓	0.0071	0.0081	1.4178	1.5418
B to Z ↑	0.0100	0.0112	1.5364	1.7272
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0103	0.0118	1.6994	1.8591
A to Z ↑	0.0166	0.0188	2.0027	2.2659
B to Z ↓	0.0096	0.0108	1.7194	1.8786
B to Z ↑	0.0129	0.0144	2.0133	2.2802
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0327	0.0373	0.5182	0.5614
A to Z ↑	0.0372	0.0422	0.7383	0.8303
B to Z ↓	0.0340	0.0388	0.5182	0.5617
B to Z ↑	0.0361	0.0411	0.7380	0.8310
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0456	0.0530	0.6232	0.6786
A to Z ↑	0.0513	0.0593	0.9705	1.1004
B to Z ↓	0.0471	0.0544	0.6231	0.6788
B to Z ↑	0.0497	0.0574	0.9704	1.1005

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X15_P0	1.387e-04	1.000e-20
X15_P4	4.939e-05	1.000e-20
X15_P10	1.562e-05	1.000e-20
X15_P16	7.153e-06	1.000e-20
X33_P0	3.723e-04	1.000e-20
X33_P4	1.309e-04	1.000e-20
X33_P10	4.073e-05	1.000e-20
X33_P16	1.839e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	8.841e-05	8.303e-05	7.714e-05	7.557e-05
B (output stable)	1.850e-04	1.922e-04	1.987e-04	2.416e-04
A to Z	2.536e-03	2.290e-03	2.170e-03	2.157e-03
B to Z	2.074e-03	1.752e-03	1.517e-03	1.412e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.518e-05	1.301e-05	1.255e-05	1.180e-05
B (output stable)	2.368e-05	2.358e-05	2.360e-05	2.309e-05
A to Z	7.507e-03	7.332e-03	7.595e-03	7.853e-03
B to Z	7.431e-03	7.238e-03	7.475e-03	7.714e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

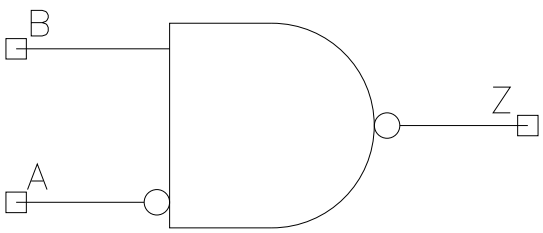
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2A

Cell Description

2 input NAND with A input inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0008	0.0008	0.0009	0.0009
B	0.0009	0.0009	0.0010	0.0011
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0011	0.0012	0.0012	0.0013
B	0.0008	0.0009	0.0009	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0267	0.0306	1.0105	1.0961
A to Z ↑	0.0233	0.0262	1.4713	1.6589
B to Z ↓	0.0307	0.0350	1.0092	1.0945
B to Z ↑	0.0297	0.0336	1.4699	1.6563
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**

A to Z ↓	0.0374	0.0431	1.2192	1.3289
A to Z ↑	0.0310	0.0348	1.9377	2.1985
B to Z ↓	0.0428	0.0491	1.2174	1.3280
B to Z ↑	0.0401	0.0457	1.9378	2.1986
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0298	0.0343	0.6075	0.6593
A to Z ↑	0.0268	0.0302	0.9659	1.0865
B to Z ↓	0.0322	0.0369	0.6064	0.6583
B to Z ↑	0.0329	0.0374	0.9621	1.0831
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0412	0.0480	0.7338	0.8014
A to Z ↑	0.0352	0.0400	1.2682	1.4404
B to Z ↓	0.0443	0.0516	0.7327	0.8012
B to Z ↑	0.0445	0.0515	1.2643	1.4362

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P0	2.314e-04	1.000e-20
X17_P4	8.216e-05	1.000e-20
X17_P10	2.584e-05	1.000e-20
X17_P16	1.177e-05	1.000e-20
X27_P0	3.009e-04	1.000e-20
X27_P4	1.070e-04	1.000e-20
X27_P10	3.382e-05	1.000e-20
X27_P16	1.548e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	3.033e-05	2.904e-05	2.816e-05	2.859e-05
B (output stable)	1.246e-03	1.115e-03	1.037e-03	1.015e-03
A to Z	3.773e-03	3.565e-03	3.590e-03	3.605e-03
B to Z	4.886e-03	4.671e-03	4.735e-03	4.771e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.027e-04	9.791e-05	9.790e-05	9.831e-05
B (output stable)	1.349e-03	1.245e-03	1.162e-03	1.182e-03
A to Z	6.212e-03	5.921e-03	5.866e-03	5.997e-03
B to Z	6.980e-03	6.745e-03	6.779e-03	6.971e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

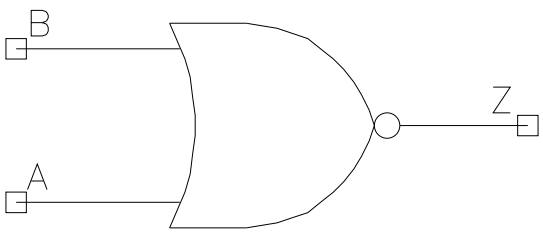
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2

Cell Description

2 input NOR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	0.952	1.1424
X14_P4	1.200	0.952	1.1424
X14_P10	1.200	0.952	1.1424
X14_P16	1.200	0.952	1.1424
X33_P0	1.200	1.496	1.7952
X33_P4	1.200	1.496	1.7952
X33_P10	1.200	1.496	1.7952
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0020	0.0021	0.0022	0.0024
B	0.0018	0.0019	0.0020	0.0021
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0008	0.0009	0.0009	0.0010
B	0.0008	0.0009	0.0009	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0097	0.0110	1.1551	1.2472
A to Z ↑	0.0107	0.0128	1.9688	2.1746
B to Z ↓	0.0071	0.0082	1.1661	1.2581
B to Z ↑	0.0100	0.0111	1.9806	2.1915
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**

A to Z ↓	0.0129	0.0145	1.3747	1.4872
A to Z ↑	0.0155	0.0180	2.4887	2.7901
B to Z ↓	0.0097	0.0109	1.3878	1.5014
B to Z ↑	0.0128	0.0145	2.5100	2.8127
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0370	0.0424	0.5124	0.5549
A to Z ↑	0.0337	0.0391	0.7353	0.8279
B to Z ↓	0.0352	0.0403	0.5124	0.5544
B to Z ↑	0.0344	0.0395	0.7367	0.8277
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0500	0.0586	0.6163	0.6717
A to Z ↑	0.0467	0.0553	0.9663	1.0952
B to Z ↓	0.0476	0.0561	0.6160	0.6704
B to Z ↑	0.0465	0.0548	0.9664	1.0949

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X14_P0	1.752e-04	1.000e-20
X14_P4	6.087e-05	1.000e-20
X14_P10	1.860e-05	1.000e-20
X14_P16	8.270e-06	1.000e-20
X33_P0	4.607e-04	1.000e-20
X33_P4	1.605e-04	1.000e-20
X33_P10	4.932e-05	1.000e-20
X33_P16	2.206e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	1.275e-04	1.246e-04	1.222e-04	1.241e-04
B (output stable)	2.724e-04	2.740e-04	2.562e-04	2.166e-04
A to Z	2.789e-03	2.588e-03	2.502e-03	2.517e-03
B to Z	2.131e-03	1.797e-03	1.552e-03	1.446e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	3.041e-05	2.977e-05	2.932e-05	2.920e-05
B (output stable)	5.368e-05	5.347e-05	5.124e-05	4.860e-05
A to Z	8.395e-03	8.274e-03	8.281e-03	8.685e-03
B to Z	8.244e-03	8.080e-03	8.029e-03	8.417e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

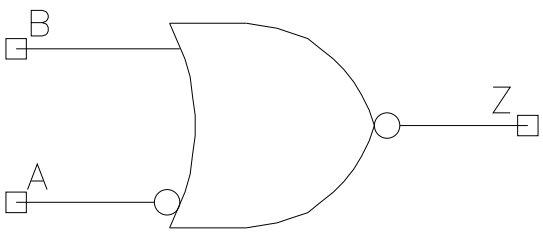
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2A

Cell Description

2 input NOR with A input Inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	1.224	1.4688
X15_P4	1.200	1.224	1.4688
X15_P10	1.200	1.224	1.4688
X15_P16	1.200	1.224	1.4688
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0012	0.0013	0.0013	0.0014
B	0.0008	0.0009	0.0009	0.0010
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0014	0.0015	0.0016	0.0017
B	0.0009	0.0009	0.0010	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0289	0.0329	1.2669	1.3720
A to Z ↑	0.0201	0.0231	1.4771	1.6628
B to Z ↓	0.0289	0.0333	1.2609	1.3651
B to Z ↑	0.0282	0.0322	1.4740	1.6578
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0390	0.0448	1.5226	1.6598
A to Z ↑	0.0276	0.0316	1.9422	2.2076
B to Z ↓	0.0400	0.0464	1.5173	1.6525
B to Z ↑	0.0383	0.0440	1.9410	2.2049
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0245	0.0279	0.7152	0.7745
A to Z ↑	0.0218	0.0247	0.7856	0.8831
B to Z ↓	0.0291	0.0334	0.7143	0.7731
B to Z ↑	0.0307	0.0350	0.7832	0.8822
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0335	0.0383	0.8587	0.9354
A to Z ↑	0.0295	0.0333	1.0324	1.1700
B to Z ↓	0.0407	0.0468	0.8584	0.9344
B to Z ↑	0.0420	0.0479	1.0303	1.1693

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X15_P0	2.604e-04	1.000e-20
X15_P4	8.910e-05	1.000e-20
X15_P10	2.688e-05	1.000e-20
X15_P16	1.188e-05	1.000e-20
X27_P0	4.192e-04	1.000e-20
X27_P4	1.425e-04	1.000e-20
X27_P10	4.269e-05	1.000e-20
X27_P16	1.876e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	5.759e-05	5.335e-05	4.865e-05	4.662e-05
B (output stable)	1.358e-03	1.242e-03	1.203e-03	1.233e-03
A to Z	3.827e-03	3.690e-03	3.691e-03	3.773e-03
B to Z	4.750e-03	4.623e-03	4.657e-03	4.781e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	8.527e-05	7.799e-05	7.285e-05	7.083e-05
B (output stable)	1.519e-03	1.405e-03	1.415e-03	1.479e-03
A to Z	6.242e-03	5.954e-03	5.997e-03	6.068e-03
B to Z	7.265e-03	7.066e-03	7.246e-03	7.366e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

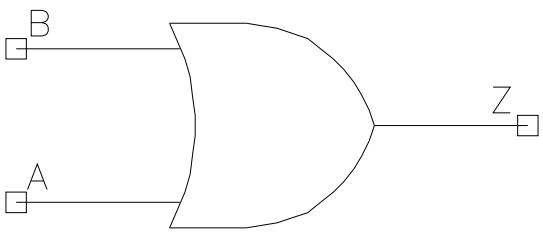
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR2

Cell Description

2 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X20_P0	1.200	1.360	1.6320
X20_P4	1.200	1.360	1.6320
X20_P10	1.200	1.360	1.6320
X20_P16	1.200	1.360	1.6320
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320
X37_P0	1.200	1.632	1.9584
X37_P4	1.200	1.632	1.9584
X37_P10	1.200	1.632	1.9584
X37_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0015	0.0016	0.0017	0.0018
B	0.0013	0.0014	0.0015	0.0016
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0022	0.0024	0.0026	0.0027
B	0.0023	0.0024	0.0026	0.0028
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0016	0.0016	0.0017	0.0018

B	0.0016	0.0016	0.0017	0.0018
	X37_P0	X37_P4	X37_P10	X37_P16
A	0.0022	0.0024	0.0025	0.0027
B	0.0023	0.0024	0.0026	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0219	0.0254	1.1465	1.2409
A to Z ↑	0.0179	0.0204	1.5465	1.7441
B to Z ↓	0.0213	0.0243	1.1456	1.2425
B to Z ↑	0.0161	0.0185	1.5456	1.7395
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0305	0.0355	1.3776	1.5014
A to Z ↑	0.0240	0.0271	2.0393	2.3190
B to Z ↓	0.0286	0.0328	1.3778	1.5026
B to Z ↑	0.0215	0.0244	2.0389	2.3147
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0201	0.0235	0.8994	0.9741
A to Z ↑	0.0186	0.0211	1.0731	1.2070
B to Z ↓	0.0197	0.0225	0.8998	0.9737
B to Z ↑	0.0164	0.0186	1.0717	1.2051
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0284	0.0331	1.0796	1.1759
A to Z ↑	0.0246	0.0279	1.4120	1.6023
B to Z ↓	0.0266	0.0307	1.0810	1.1767
B to Z ↑	0.0217	0.0246	1.4102	1.5996
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0267	0.0308	0.5163	0.5593
A to Z ↑	0.0221	0.0250	0.7278	0.8195
B to Z ↓	0.0260	0.0296	0.5162	0.5596
B to Z ↑	0.0200	0.0227	0.7264	0.8184
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0374	0.0434	0.6222	0.6779
A to Z ↑	0.0294	0.0332	0.9587	1.0878
B to Z ↓	0.0353	0.0405	0.6222	0.6784
B to Z ↑	0.0266	0.0300	0.9571	1.0861
	X37_P0	**X37_P4**	**X37_P0**	**X37_P4**
A to Z ↓	0.0240	0.0279	0.5018	0.5434
A to Z ↑	0.0211	0.0239	0.5924	0.6665
B to Z ↓	0.0239	0.0274	0.5014	0.5441
B to Z ↑	0.0191	0.0218	0.5904	0.6653
	X37_P10	**X37_P16**	**X37_P10**	**X37_P16**
A to Z ↓	0.0338	0.0390	0.6040	0.6583
A to Z ↑	0.0280	0.0314	0.7784	0.8827
B to Z ↓	0.0326	0.0372	0.6045	0.6577
B to Z ↑	0.0254	0.0284	0.7769	0.8812

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X15_P0	1.870e-04	1.000e-20

X15_P4	6.629e-05	1.000e-20
X15_P10	2.084e-05	1.000e-20
X15_P16	9.487e-06	1.000e-20
X20_P0	3.111e-04	1.000e-20
X20_P4	1.095e-04	1.000e-20
X20_P10	3.404e-05	1.000e-20
X20_P16	1.537e-05	1.000e-20
X33_P0	3.253e-04	1.000e-20
X33_P4	1.169e-04	1.000e-20
X33_P10	3.718e-05	1.000e-20
X33_P16	1.706e-05	1.000e-20
X37_P0	4.125e-04	1.000e-20
X37_P4	1.458e-04	1.000e-20
X37_P10	4.550e-05	1.000e-20
X37_P16	2.059e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	7.491e-05	7.266e-05	7.170e-05	7.312e-05
B (output stable)	1.612e-04	1.616e-04	1.593e-04	1.234e-04
A to Z	3.850e-03	3.704e-03	3.716e-03	3.814e-03
B to Z	3.445e-03	3.229e-03	3.143e-03	3.162e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	1.328e-04	1.282e-04	1.266e-04	1.263e-04
B (output stable)	2.729e-04	2.737e-04	2.560e-04	2.115e-04
A to Z	5.886e-03	5.704e-03	5.719e-03	5.921e-03
B to Z	5.202e-03	4.893e-03	4.763e-03	4.832e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.014e-04	9.809e-05	9.611e-05	9.840e-05
B (output stable)	2.579e-04	2.600e-04	2.547e-04	1.849e-04
A to Z	7.382e-03	7.055e-03	7.043e-03	7.180e-03
B to Z	6.812e-03	6.387e-03	6.266e-03	6.304e-03
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	1.325e-04	1.283e-04	1.279e-04	1.293e-04
B (output stable)	2.750e-04	2.772e-04	2.599e-04	2.113e-04
A to Z	8.661e-03	8.376e-03	8.397e-03	8.508e-03
B to Z	7.975e-03	7.570e-03	7.433e-03	7.436e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

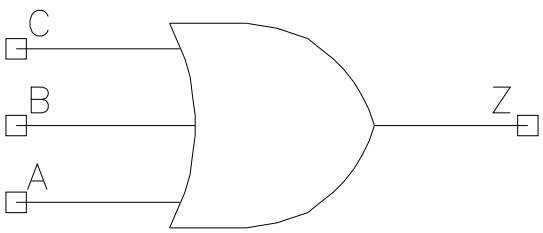
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR3

Cell Description

3 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	1.360	1.6320
X14_P4	1.200	1.360	1.6320
X14_P10	1.200	1.360	1.6320
X14_P16	1.200	1.360	1.6320
X20_P0	1.200	1.632	1.9584
X20_P4	1.200	1.632	1.9584
X20_P10	1.200	1.632	1.9584
X20_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0008	0.0009	0.0010	0.0010
B	0.0008	0.0009	0.0009	0.0010
C	0.0008	0.0009	0.0009	0.0010
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0008	0.0009	0.0009	0.0010
B	0.0008	0.0009	0.0009	0.0010
C	0.0008	0.0009	0.0009	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	X14_P4	X14_P0	X14_P4
A to Z ↓	0.0436	0.0499	1.2658	1.3712
A to Z ↑	0.0368	0.0421	1.5518	1.7479

B to Z ↓	0.0433	0.0500	1.2641	1.3710
B to Z ↑	0.0387	0.0441	1.5525	1.7459
C to Z ↓	0.0406	0.0463	1.2646	1.3718
C to Z ↑	0.0341	0.0389	1.5527	1.7478
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0599	0.0700	1.5219	1.6611
A to Z ↑	0.0500	0.0579	2.0411	2.3194
B to Z ↓	0.0605	0.0711	1.5240	1.6609
B to Z ↑	0.0524	0.0606	2.0414	2.3167
C to Z ↓	0.0552	0.0643	1.5238	1.6608
C to Z ↑	0.0464	0.0536	2.0418	2.3181
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0433	0.0497	0.9269	1.0043
A to Z ↑	0.0398	0.0459	1.0931	1.2299
B to Z ↓	0.0429	0.0497	0.9258	1.0043
B to Z ↑	0.0414	0.0476	1.0924	1.2300
C to Z ↓	0.0391	0.0449	0.9266	1.0039
C to Z ↑	0.0379	0.0436	1.0935	1.2293
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0598	0.0697	1.1145	1.2127
A to Z ↑	0.0551	0.0641	1.4330	1.6273
B to Z ↓	0.0604	0.0708	1.1130	1.2135
B to Z ↑	0.0572	0.0664	1.4345	1.6272
C to Z ↓	0.0540	0.0627	1.1124	1.2125
C to Z ↑	0.0525	0.0609	1.4358	1.6267

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X14_P0	2.745e-04	1.000e-20
X14_P4	9.755e-05	1.000e-20
X14_P10	3.081e-05	1.000e-20
X14_P16	1.410e-05	1.000e-20
X20_P0	3.263e-04	1.000e-20
X20_P4	1.164e-04	1.000e-20
X20_P10	3.683e-05	1.000e-20
X20_P16	1.687e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	4.682e-04	4.475e-04	4.431e-04	4.514e-04
B (output stable)	5.095e-04	4.994e-04	5.118e-04	5.338e-04
C (output stable)	1.178e-03	1.081e-03	1.032e-03	1.028e-03
A to Z	5.431e-03	5.360e-03	5.445e-03	5.649e-03
B to Z	5.594e-03	5.556e-03	5.687e-03	5.927e-03
C to Z	5.374e-03	5.271e-03	5.332e-03	5.511e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	4.565e-04	4.348e-04	4.282e-04	4.346e-04
B (output stable)	4.952e-04	4.833e-04	4.935e-04	5.130e-04
C (output stable)	1.115e-03	1.014e-03	9.595e-04	9.503e-04
A to Z	6.526e-03	6.474e-03	6.605e-03	6.826e-03
B to Z	6.682e-03	6.662e-03	6.837e-03	7.095e-03

C to Z	6.432e-03	6.355e-03	6.463e-03	6.665e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

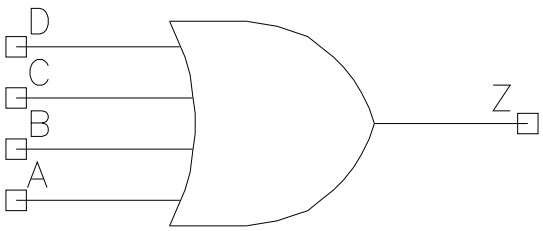
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR4

Cell Description

4 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X20_P4	1.200	2.176	2.6112
X20_P10	1.200	2.176	2.6112
X20_P16	1.200	2.176	2.6112
X27_P0	1.200	2.312	2.7744
X27_P4	1.200	2.312	2.7744
X27_P10	1.200	2.312	2.7744
X27_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0012	0.0013	0.0013	0.0014
B	0.0013	0.0014	0.0015	0.0015
C	0.0012	0.0013	0.0014	0.0014
D	0.0013	0.0014	0.0015	0.0015
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0012	0.0013	0.0013	0.0013
B	0.0013	0.0014	0.0014	0.0015
C	0.0012	0.0013	0.0014	0.0014
D	0.0014	0.0015	0.0016	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0298	0.0345	0.9218	1.0038
A to Z ↑	0.0292	0.0333	1.2803	1.4406
B to Z ↓	0.0280	0.0323	0.9220	1.0051
B to Z ↑	0.0274	0.0311	1.2807	1.4418
C to Z ↓	0.0284	0.0327	0.9181	1.0009
C to Z ↑	0.0278	0.0314	1.2726	1.4344
D to Z ↓	0.0272	0.0311	0.9173	1.0007
D to Z ↑	0.0261	0.0293	1.2720	1.4311
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0410	0.0479	1.1238	1.2331
A to Z ↑	0.0389	0.0450	1.6877	1.9173
B to Z ↓	0.0381	0.0445	1.1244	1.2342
B to Z ↑	0.0362	0.0418	1.6866	1.9146
C to Z ↓	0.0392	0.0445	1.1205	1.2287
C to Z ↑	0.0368	0.0411	1.6789	1.9117
D to Z ↓	0.0370	0.0419	1.1203	1.2288
D to Z ↑	0.0342	0.0382	1.6782	1.9074
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0325	0.0376	0.7576	0.8260
A to Z ↑	0.0310	0.0354	0.9592	1.0797
B to Z ↓	0.0308	0.0355	0.7584	0.8267
B to Z ↑	0.0293	0.0333	0.9574	1.0806
C to Z ↓	0.0296	0.0340	0.7532	0.8213
C to Z ↑	0.0281	0.0317	0.9519	1.0739
D to Z ↓	0.0284	0.0324	0.7532	0.8214
D to Z ↑	0.0260	0.0293	0.9511	1.0736
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0450	0.0521	0.9250	1.0167
A to Z ↑	0.0416	0.0474	1.2648	1.4369
B to Z ↓	0.0424	0.0490	0.9255	1.0174
B to Z ↑	0.0391	0.0445	1.2630	1.4364
C to Z ↓	0.0407	0.0471	0.9201	1.0097
C to Z ↑	0.0372	0.0422	1.2588	1.4330
D to Z ↓	0.0386	0.0445	0.9200	1.0100
D to Z ↑	0.0343	0.0388	1.2574	1.4295

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X20_P0	2.734e-04	1.000e-20
X20_P4	9.944e-05	1.000e-20
X20_P10	3.228e-05	1.000e-20
X20_P16	1.505e-05	1.000e-20
X27_P0	2.977e-04	1.000e-20
X27_P4	1.086e-04	1.000e-20
X27_P10	3.539e-05	1.000e-20
X27_P16	1.655e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	1.344e-03	1.373e-03	1.428e-03	1.531e-03

B (output stable)	1.233e-03	1.230e-03	1.246e-03	1.319e-03
C (output stable)	1.307e-03	1.310e-03	1.364e-03	1.453e-03
D (output stable)	1.192e-03	1.163e-03	1.174e-03	1.233e-03
A to Z	6.680e-03	6.678e-03	6.819e-03	7.164e-03
B to Z	6.385e-03	6.313e-03	6.370e-03	6.663e-03
C to Z	6.302e-03	6.130e-03	6.200e-03	6.236e-03
D to Z	6.004e-03	5.761e-03	5.738e-03	5.724e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.539e-03	1.587e-03	1.683e-03	1.784e-03
B (output stable)	1.426e-03	1.441e-03	1.502e-03	1.576e-03
C (output stable)	1.372e-03	1.376e-03	1.438e-03	1.539e-03
D (output stable)	1.258e-03	1.230e-03	1.249e-03	1.318e-03
A to Z	8.056e-03	7.995e-03	8.142e-03	8.448e-03
B to Z	7.749e-03	7.616e-03	7.693e-03	7.950e-03
C to Z	7.140e-03	6.902e-03	6.921e-03	7.103e-03
D to Z	6.854e-03	6.545e-03	6.482e-03	6.609e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

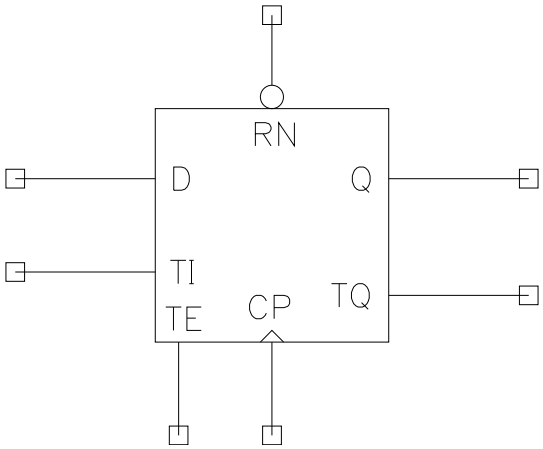
Pin Cycle (vdds)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNSDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.080	4.8960
X15_P4	1.200	4.080	4.8960
X15_P10	1.200	4.080	4.8960
X15_P16	1.200	4.080	4.8960

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0007	0.0008	0.0008	0.0009
D	0.0006	0.0006	0.0006	0.0006
RN	0.0008	0.0008	0.0008	0.0008

TE	0.0009	0.0010	0.0010	0.0011
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	X15_P4	X15_P0	X15_P4
CP to Q ↓	0.0679	0.0776	1.2751	1.3817
CP to Q ↑	0.0709	0.0809	1.4496	1.6329
CP to TQ ↓	0.0696	0.0797	6.3132	6.7929
CP to TQ ↑	0.0769	0.0878	14.2069	16.0733
RN to Q ↓	0.0818	0.0942	1.2741	1.3776
RN to TQ ↓	0.0835	0.0963	6.3101	6.7890
	X15_P10	X15_P16	X15_P10	X15_P16
CP to Q ↓	0.0927	0.1073	1.5320	1.6665
CP to Q ↑	0.0965	0.1114	1.9107	2.1694
CP to TQ ↓	0.0953	0.1105	7.4599	8.0471
CP to TQ ↑	0.1046	0.1209	18.8815	21.5296
RN to Q ↓	0.1138	0.1332	1.5290	1.6634
RN to TQ ↓	0.1165	0.1363	7.4570	8.0434

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.0760	0.0894	0.1129	0.1340
CP ↑	min_pulse_width to CP	0.0390	0.0435	0.0480	0.0526
D ↓	hold_rising to CP	-0.0072	-0.0126	-0.0170	-0.0241
D ↑	hold_rising to CP	-0.0115	-0.0169	-0.0218	-0.0267
D ↓	setup_rising to CP	0.0468	0.0570	0.0684	0.0840
D ↑	setup_rising to CP	0.0417	0.0465	0.0563	0.0637
RN ↓	min_pulse_width to RN	0.0615	0.0686	0.0833	0.0952
RN ↑	recovery_rising to CP	0.0151	0.0173	0.0222	0.0271
RN ↑	removal_rising to CP	-0.0035	-0.0061	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0055	-0.0072	-0.0143	-0.0224
TE ↑	hold_rising to CP	-0.0244	-0.0293	-0.0391	-0.0462
TE ↓	setup_rising to CP	0.0635	0.0705	0.0852	0.1003
TE ↑	setup_rising to CP	0.0960	0.1182	0.1443	0.1736
TI ↓	hold_rising to CP	-0.0488	-0.0642	-0.0795	-0.0988
TI ↑	hold_rising to CP	-0.0251	-0.0315	-0.0377	-0.0439
TI ↓	setup_rising to CP	0.0932	0.1127	0.1400	0.1684
TI ↑	setup_rising to CP	0.0557	0.0613	0.0723	0.0836

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X15_P0	4.499e-04	1.000e-20
X15_P4	1.585e-04	1.000e-20
X15_P10	4.980e-05	1.000e-20
X15_P16	2.274e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

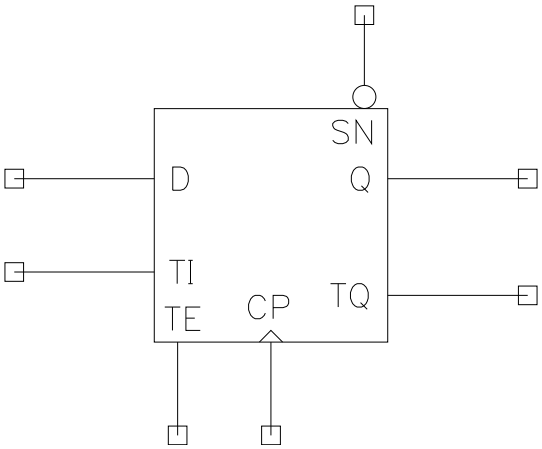
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	7.552e-03	7.511e-03	7.541e-03	7.611e-03
Clock 100Mhz Data 25Mhz	8.022e-03	7.986e-03	8.068e-03	8.200e-03
Clock 100Mhz Data 50Mhz	8.492e-03	8.462e-03	8.595e-03	8.789e-03
Clock = 0 Data 100Mhz	3.429e-03	3.445e-03	3.488e-03	3.543e-03
Clock = 1 Data 100Mhz	3.641e-05	3.526e-05	3.431e-05	3.377e-05

CNSDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.216	5.0592
X15_P4	1.200	4.216	5.0592
X15_P10	1.200	4.216	5.0592
X15_P16	1.200	4.216	5.0592

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0007	0.0008	0.0008	0.0009
D	0.0004	0.0004	0.0004	0.0005
SN	0.0014	0.0014	0.0016	0.0016

TE	0.0009	0.0010	0.0010	0.0011
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	X15_P4	X15_P0	X15_P4
CP to Q ↓	0.0681	0.0778	1.2762	1.3818
CP to Q ↑	0.0714	0.0815	1.4508	1.6340
CP to TQ ↓	0.0698	0.0800	6.3223	6.8041
CP to TQ ↑	0.0774	0.0884	14.2051	16.0674
SN to Q ↑	0.0688	0.0785	1.4501	1.6325
SN to TQ ↑	0.0748	0.0855	14.2078	16.0772
	X15_P10	X15_P16	X15_P10	X15_P16
CP to Q ↓	0.0929	0.1074	1.5326	1.6666
CP to Q ↑	0.0970	0.1121	1.9099	2.1692
CP to TQ ↓	0.0956	0.1108	7.4709	8.0614
CP to TQ ↑	0.1055	0.1219	18.8830	21.5375
SN to Q ↑	0.0935	0.1080	1.9106	2.1688
SN to TQ ↑	0.1019	0.1178	18.8870	21.5408

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.0837	0.0995	0.1206	0.1434
CP ↑	min_pulse_width to CP	0.0390	0.0435	0.0480	0.0560
D ↓	hold_rising to CP	-0.0094	-0.0143	-0.0224	-0.0290
D ↑	hold_rising to CP	-0.0098	-0.0115	-0.0165	-0.0240
D ↓	setup_rising to CP	0.0516	0.0614	0.0786	0.0938
D ↑	setup_rising to CP	0.0363	0.0417	0.0524	0.0562
SN ↓	min_pulse_width to SN	0.0447	0.0496	0.0593	0.0642
SN ↑	recovery_rising to CP	-0.0017	0.0005	0.0031	0.0063
SN ↑	removal_rising to CP	0.0308	0.0357	0.0406	0.0423
TE ↓	hold_rising to CP	-0.0072	-0.0121	-0.0192	-0.0273
TE ↑	hold_rising to CP	-0.0196	-0.0240	-0.0342	-0.0413
TE ↓	setup_rising to CP	0.0586	0.0657	0.0803	0.0900
TE ↑	setup_rising to CP	0.1057	0.1284	0.1573	0.1860
TI ↓	hold_rising to CP	-0.0586	-0.0697	-0.0892	-0.1101
TI ↑	hold_rising to CP	-0.0203	-0.0267	-0.0328	-0.0426
TI ↓	setup_rising to CP	0.1029	0.1224	0.1540	0.1790
TI ↑	setup_rising to CP	0.0502	0.0564	0.0674	0.0771

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X15_P0	4.352e-04	1.000e-20
X15_P4	1.545e-04	1.000e-20
X15_P10	4.897e-05	1.000e-20
X15_P16	2.250e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

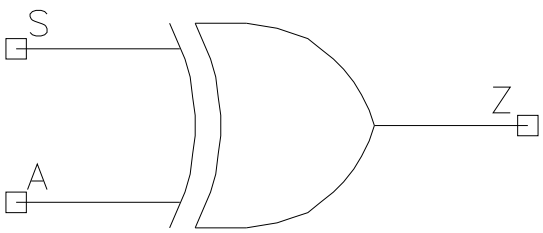
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	7.622e-03	7.582e-03	7.614e-03	7.686e-03
Clock 100Mhz Data 25Mhz	8.117e-03	8.083e-03	8.167e-03	8.300e-03
Clock 100Mhz Data 50Mhz	8.613e-03	8.585e-03	8.721e-03	8.914e-03
Clock = 0 Data 100Mhz	3.470e-03	3.481e-03	3.522e-03	3.574e-03
Clock = 1 Data 100Mhz	3.625e-05	3.512e-05	3.424e-05	3.369e-05

CNXOR2

Cell Description

2 input Exclusive OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X16_P0	1.200	1.360	1.6320
X16_P4	1.200	1.360	1.6320
X16_P10	1.200	1.360	1.6320
X16_P16	1.200	1.360	1.6320
X27_P0	1.200	2.040	2.4480
X27_P4	1.200	2.040	2.4480
X27_P10	1.200	2.040	2.4480
X27_P16	1.200	2.040	2.4480

Truth Table

A	S	Z
1	S	!S
0	S	S

Pin Capacitance

Pin	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0010	0.0011	0.0011	0.0012
S	0.0015	0.0015	0.0016	0.0018
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0014	0.0015	0.0016	0.0017
S	0.0021	0.0021	0.0023	0.0024

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0342	0.0392	1.0653	1.1544
A to Z ↑	0.0321	0.0364	1.4937	1.6836
S to Z ↓	0.0261	0.0298	1.0614	1.1512
S to Z ↑	0.0256	0.0291	1.4927	1.6823
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0466	0.0542	1.2812	1.3982

A to Z ↑	0.0425	0.0488	1.9710	2.2391
S to Z ↓	0.0350	0.0405	1.2787	1.3946
S to Z ↑	0.0340	0.0391	1.9685	2.2374
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0353	0.0404	0.7139	0.7750
A to Z ↑	0.0348	0.0394	0.7942	0.8935
S to Z ↓	0.0287	0.0327	0.7133	0.7745
S to Z ↑	0.0285	0.0323	0.7945	0.8929
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0484	0.0557	0.8619	0.9407
A to Z ↑	0.0467	0.0532	1.0448	1.1855
S to Z ↓	0.0388	0.0446	0.8614	0.9397
S to Z ↑	0.0381	0.0435	1.0445	1.1860

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X16_P0	4.072e-04	1.000e-20
X16_P4	1.418e-04	1.000e-20
X16_P10	4.366e-05	1.000e-20
X16_P16	1.960e-05	1.000e-20
X27_P0	6.373e-04	1.000e-20
X27_P4	2.192e-04	1.000e-20
X27_P10	6.651e-05	1.000e-20
X27_P16	2.952e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	5.916e-03	5.675e-03	5.549e-03	5.676e-03
S to Z	5.090e-03	4.803e-03	4.627e-03	4.709e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	1.059e-02	1.010e-02	9.979e-03	1.003e-02
S to Z	8.172e-03	7.665e-03	7.441e-03	7.470e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

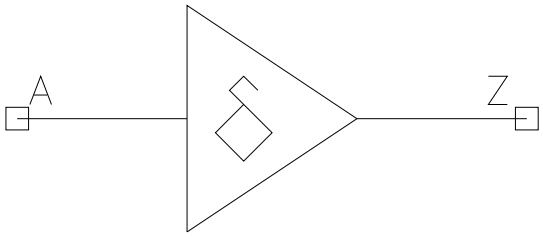
Pin Cycle (vdds)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DLYHF

Cell Description

Delay cell for Hold Time Fixing

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-DLYHFM4X7_P0	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X7_P4	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X7_P10	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X7_P16	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X15_P0	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM4X15_P4	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM4X15_P10	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM4X15_P16	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM8X7_P0	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X7_P4	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X7_P10	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X7_P16	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X15_P0	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X15_P4	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X15_P10	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X15_P16	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X54_P0	1.200	4.216	5.0592

C12T28SOI_LL_-DLYHFM8X54_P4	1.200	4.216	5.0592
C12T28SOI_LL_-DLYHFM8X54_P10	1.200	4.216	5.0592
C12T28SOI_LL_-DLYHFM8X54_P16	1.200	4.216	5.0592

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C12T28SOI_LL_-DLYHFM4X7_P0	C12T28SOI_LL_-DLYHFM4X7_P4	C12T28SOI_LL_-DLYHFM4X7_P10	C12T28SOI_LL_-DLYHFM4X7_P16
A	0.0007	0.0007	0.0007	0.0008
	C12T28SOI_LL_-DLYHFM4X15_P0	C12T28SOI_LL_-DLYHFM4X15_P4	C12T28SOI_LL_-DLYHFM4X15_P10	C12T28SOI_LL_-DLYHFM4X15_P16
A	0.0007	0.0007	0.0007	0.0008
	C12T28SOI_LL_-DLYHFM8X7_P0	C12T28SOI_LL_-DLYHFM8X7_P4	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A	0.0007	0.0007	0.0007	0.0007
	C12T28SOI_LL_-DLYHFM8X15_P0	C12T28SOI_LL_-DLYHFM8X15_P4	C12T28SOI_LL_-DLYHFM8X15_P10	C12T28SOI_LL_-DLYHFM8X15_P16
A	0.0007	0.0007	0.0007	0.0007
	C12T28SOI_LL_-DLYHFM8X54_P0	C12T28SOI_LL_-DLYHFM8X54_P4	C12T28SOI_LL_-DLYHFM8X54_P10	C12T28SOI_LL_-DLYHFM8X54_P16
A	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-DLYHFM4X7_P0	**C12T28SOI_LL_-DLYHFM4X7_P4**	**C12T28SOI_LL_-DLYHFM4X7_P0**	**C12T28SOI_LL_-DLYHFM4X7_P4**
A to Z ↓	0.0961	0.1102	2.4511	2.6667
A to Z ↑	0.0945	0.1086	3.4208	3.8608
	C12T28SOI_LL_-DLYHFM4X7_P10	**C12T28SOI_LL_-DLYHFM4X7_P16**	**C12T28SOI_LL_-DLYHFM4X7_P10**	**C12T28SOI_LL_-DLYHFM4X7_P16**
A to Z ↓	0.1326	0.1549	2.9791	3.2612
A to Z ↑	0.1308	0.1529	4.5190	5.1367
	C12T28SOI_LL_-DLYHFM4X15_P0	**C12T28SOI_LL_-DLYHFM4X15_P4**	**C12T28SOI_LL_-DLYHFM4X15_P0**	**C12T28SOI_LL_-DLYHFM4X15_P4**
A to Z ↓	0.1037	0.1191	1.1852	1.2916
A to Z ↑	0.1046	0.1201	1.5824	1.7857
	C12T28SOI_LL_-DLYHFM4X15_P10	**C12T28SOI_LL_-DLYHFM4X15_P16**	**C12T28SOI_LL_-DLYHFM4X15_P10**	**C12T28SOI_LL_-DLYHFM4X15_P16**
A to Z ↓	0.1440	0.1691	1.4497	1.5919
A to Z ↑	0.1451	0.1700	2.0917	2.3814
	C12T28SOI_LL_-DLYHFM8X7_P0	**C12T28SOI_LL_-DLYHFM8X7_P4**	**C12T28SOI_LL_-DLYHFM8X7_P0**	**C12T28SOI_LL_-DLYHFM8X7_P4**
A to Z ↓	0.1734	0.1997	2.4656	2.6807
A to Z ↑	0.1635	0.1881	3.1568	3.5558

	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A to Z ↓	0.2417	0.2837	2.9981	3.2869
A to Z ↑	0.2273	0.2662	4.1585	4.7264
	C12T28SOI_LL_-DLYHFM8X15_P0	**C12T28SOI_LL_-DLYHFM8X15_P4**	**C12T28SOI_LL_-DLYHFM8X15_P0**	**C12T28SOI_LL_-DLYHFM8X15_P4**
A to Z ↓	0.1795	0.2071	1.1849	1.2950
A to Z ↑	0.1737	0.2001	1.5833	1.7869
	C12T28SOI_LL_-DLYHFM8X15_P10	**C12T28SOI_LL_-DLYHFM8X15_P16**	**C12T28SOI_LL_-DLYHFM8X15_P10**	**C12T28SOI_LL_-DLYHFM8X15_P16**
A to Z ↓	0.2512	0.2955	1.4532	1.6008
A to Z ↑	0.2420	0.2837	2.0948	2.3819
	C12T28SOI_LL_-DLYHFM8X54_P0	**C12T28SOI_LL_-DLYHFM8X54_P4**	**C12T28SOI_LL_-DLYHFM8X54_P0**	**C12T28SOI_LL_-DLYHFM8X54_P4**
A to Z ↓	0.2338	0.2709	0.3141	0.3410
A to Z ↑	0.2117	0.2456	0.4527	0.5088
	C12T28SOI_LL_-DLYHFM8X54_P10	**C12T28SOI_LL_-DLYHFM8X54_P16**	**C12T28SOI_LL_-DLYHFM8X54_P10**	**C12T28SOI_LL_-DLYHFM8X54_P16**
A to Z ↓	0.3289	0.3891	0.3793	0.4143
A to Z ↑	0.2988	0.3541	0.5928	0.6725

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_DLYHFM4X7_P0	6.373e-05	1.000e-20
C12T28SOI_LL_DLYHFM4X7_P4	2.303e-05	1.000e-20
C12T28SOI_LL_DLYHFM4X7_P10	7.478e-06	1.000e-20
C12T28SOI_LL_DLYHFM4X7_P16	3.508e-06	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P0	1.297e-04	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P4	4.579e-05	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P10	1.439e-05	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P16	6.579e-06	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P0	7.171e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P4	2.628e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P10	8.689e-06	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P16	4.130e-06	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P0	1.348e-04	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P4	4.800e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P10	1.528e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P16	7.061e-06	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P0	4.975e-04	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P4	1.782e-04	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P10	5.670e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P16	2.603e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-DLYHFM4X7_P0	C12T28SOI_LL_-DLYHFM4X7_P4	C12T28SOI_LL_-DLYHFM4X7_P10	C12T28SOI_LL_-DLYHFM4X7_P16
A to Z	3.663e-03	3.638e-03	3.712e-03	3.833e-03
	C12T28SOI_LL_-DLYHFM4X15_P0	C12T28SOI_LL_-DLYHFM4X15_P4	C12T28SOI_LL_-DLYHFM4X15_P10	C12T28SOI_LL_-DLYHFM4X15_P16
A to Z	5.930e-03	5.663e-03	5.572e-03	5.638e-03

	C12T28SOI_LL_-DLYHFM8X7_P0	C12T28SOI_LL_-DLYHFM8X7_P4	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A to Z	5.680e-03	5.681e-03	5.822e-03	6.015e-03
	C12T28SOI_LL_-DLYHFM8X15_P0	C12T28SOI_LL_-DLYHFM8X15_P4	C12T28SOI_LL_-DLYHFM8X15_P10	C12T28SOI_LL_-DLYHFM8X15_P16
A to Z	7.926e-03	7.694e-03	7.669e-03	7.807e-03
	C12T28SOI_LL_-DLYHFM8X54_P0	C12T28SOI_LL_-DLYHFM8X54_P4	C12T28SOI_LL_-DLYHFM8X54_P10	C12T28SOI_LL_-DLYHFM8X54_P16
A to Z	2.355e-02	2.350e-02	2.400e-02	2.508e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

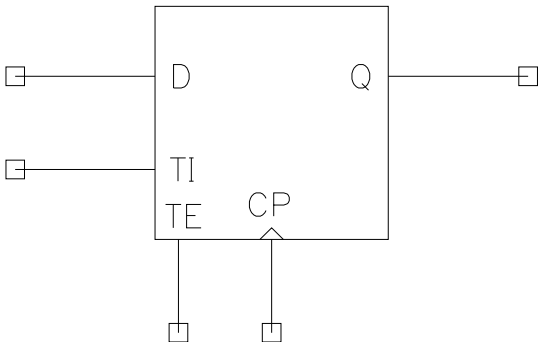
Pin Cycle (vdds)	C12T28SOI_LL_-DLYHFM4X7_P0	C12T28SOI_LL_-DLYHFM4X7_P4	C12T28SOI_LL_-DLYHFM4X7_P10	C12T28SOI_LL_-DLYHFM4X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM4X15_P0	C12T28SOI_LL_-DLYHFM4X15_P4	C12T28SOI_LL_-DLYHFM4X15_P10	C12T28SOI_LL_-DLYHFM4X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM8X7_P0	C12T28SOI_LL_-DLYHFM8X7_P4	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM8X15_P0	C12T28SOI_LL_-DLYHFM8X15_P4	C12T28SOI_LL_-DLYHFM8X15_P10	C12T28SOI_LL_-DLYHFM8X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM8X54_P0	C12T28SOI_LL_-DLYHFM8X54_P4	C12T28SOI_LL_-DLYHFM8X54_P10	C12T28SOI_LL_-DLYHFM8X54_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFSYNCPQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.400	8.1600
X8_P4	2.400	3.400	8.1600
X8_P10	2.400	3.400	8.1600
X8_P16	2.400	3.400	8.1600

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0008	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0007	0.0007
TE	0.0009	0.0009	0.0010	0.0010
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X8_P4	X8_P0	X8_P4
CP to Q ↓	0.1132	0.1309	1.9791	2.1464
CP to Q ↑	0.1343	0.1541	2.9114	3.2879

	X8_P10	X8_P16	X8_P10	X8_P16
CP to Q ↓	0.1593	0.1871	2.3860	2.6013
CP to Q ↑	0.1859	0.2177	3.8503	4.3760

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1682	0.1998	0.2484	0.2947
CP ↑	min_pulse_width to CP	0.0691	0.0783	0.0923	0.1110
D ↓	hold_rising to CP	-0.0462	-0.0560	-0.0729	-0.0908
D ↑	hold_rising to CP	-0.0212	-0.0261	-0.0364	-0.0462
D ↓	setup_rising to CP	0.0954	0.1100	0.1344	0.1620
D ↑	setup_rising to CP	0.0489	0.0563	0.0661	0.0762
TE ↓	hold_rising to CP	-0.0414	-0.0511	-0.0712	-0.0827
TE ↑	hold_rising to CP	-0.0586	-0.0684	-0.0830	-0.0999
TE ↓	setup_rising to CP	0.0940	0.1086	0.1297	0.1547
TE ↑	setup_rising to CP	0.1942	0.2273	0.2810	0.3353
TI ↓	hold_rising to CP	-0.1303	-0.1576	-0.1980	-0.2413
TI ↑	hold_rising to CP	-0.0608	-0.0719	-0.0865	-0.1025
TI ↓	setup_rising to CP	0.1902	0.2216	0.2704	0.3248
TI ↑	setup_rising to CP	0.0903	0.1015	0.1177	0.1323

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	5.595e-04	1.000e-20
X8_P4	1.993e-04	1.000e-20
X8_P10	6.340e-05	1.000e-20
X8_P16	2.919e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

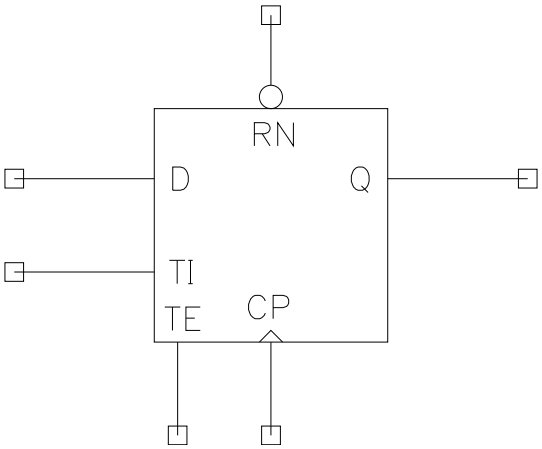
Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	1.430e-02	1.451e-02	1.487e-02	1.529e-02
Clock 100Mhz Data 25Mhz	1.510e-02	1.516e-02	1.548e-02	1.589e-02
Clock 100Mhz Data 50Mhz	1.590e-02	1.582e-02	1.610e-02	1.649e-02
Clock = 0 Data 100Mhz	8.324e-03	8.147e-03	8.035e-03	8.002e-03
Clock = 1 Data 100Mhz	2.825e-05	2.703e-05	2.614e-05	2.565e-05

SDFSYNCPRQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0008	0.0008	0.0009	0.0009
D	0.0006	0.0006	0.0007	0.0007
RN	0.0017	0.0018	0.0019	0.0021
TE	0.0009	0.0009	0.0010	0.0010
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
CP to Q ↓	0.1249	0.1444	1.9870	2.1569
CP to Q ↑	0.1350	0.1551	2.9015	3.2747
RN to Q ↓	0.1298	0.1521	1.9850	2.1545
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
CP to Q ↓	0.1751	0.2057	2.3958	2.6174
CP to Q ↑	0.1872	0.2192	3.8404	4.3636
RN to Q ↓	0.1879	0.2240	2.3988	2.6161

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1658	0.1974	0.2444	0.2924
CP ↑	min_pulse_width to CP	0.0690	0.0782	0.0921	0.1095
D ↓	hold_rising to CP	-0.0446	-0.0566	-0.0712	-0.0876
D ↑	hold_rising to CP	-0.0244	-0.0289	-0.0364	-0.0462
D ↓	setup_rising to CP	0.0905	0.1052	0.1322	0.1545
D ↑	setup_rising to CP	0.0510	0.0558	0.0660	0.0758
RN ↓	min_pulse_width to RN	0.1099	0.1267	0.1538	0.1804
RN ↑	recovery_rising to CP	0.0103	0.0125	0.0151	0.0146
RN ↑	removal_rising to CP	-0.0051	-0.0077	-0.0099	-0.0099
TE ↓	hold_rising to CP	-0.0392	-0.0512	-0.0658	-0.0831
TE ↑	hold_rising to CP	-0.0576	-0.0706	-0.0852	-0.0999
TE ↓	setup_rising to CP	0.0886	0.1037	0.1275	0.1498
TE ↑	setup_rising to CP	0.1860	0.2228	0.2771	0.3276
TI ↓	hold_rising to CP	-0.1270	-0.1527	-0.1974	-0.2371
TI ↑	hold_rising to CP	-0.0614	-0.0719	-0.0879	-0.1025
TI ↓	setup_rising to CP	0.1810	0.2152	0.2655	0.3159
TI ↑	setup_rising to CP	0.0954	0.1051	0.1220	0.1371

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	5.692e-04	1.000e-20
X8_P4	2.030e-04	1.000e-20
X8_P10	6.472e-05	1.000e-20
X8_P16	2.987e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	1.486e-02	1.508e-02	1.546e-02	1.590e-02

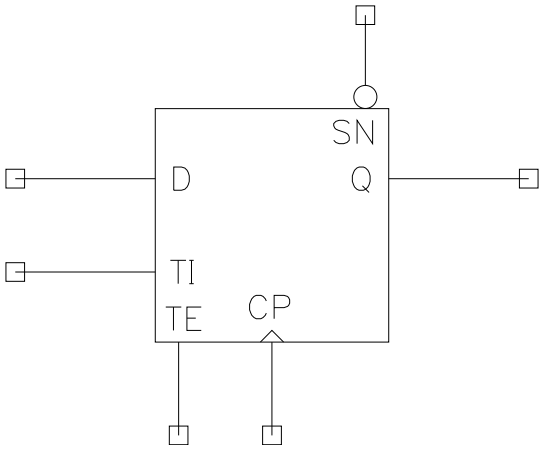
Clock 100Mhz Data 25Mhz	1.559e-02	1.567e-02	1.601e-02	1.644e-02
Clock 100Mhz Data 50Mhz	1.632e-02	1.626e-02	1.656e-02	1.699e-02
Clock = 0 Data 100Mhz	8.167e-03	8.014e-03	7.933e-03	7.922e-03
Clock = 1 Data 100Mhz	2.832e-05	2.712e-05	2.630e-05	2.584e-05

SDFSYNCPSQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0008	0.0008	0.0009	0.0009
D	0.0004	0.0004	0.0005	0.0005
SN	0.0015	0.0016	0.0017	0.0018
TE	0.0009	0.0009	0.0010	0.0010
TI	0.0003	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X8_P4	X8_P0	X8_P4
CP to Q ↓	0.0949	0.1089	2.3400	2.5780
CP to Q ↑	0.1150	0.1318	3.1048	3.5078
SN to Q ↑	0.1430	0.1638	2.9607	3.3551
	X8_P10	X8_P16	X8_P10	X8_P16
CP to Q ↓	0.1307	0.1520	2.9309	3.2629
CP to Q ↑	0.1588	0.1858	4.1130	4.6879
SN to Q ↑	0.1977	0.2320	3.9431	4.4911

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1581	0.1886	0.2343	0.2789
CP ↑	min_pulse_width to CP	0.0738	0.0831	0.1017	0.1156
D ↓	hold_rising to CP	-0.0370	-0.0436	-0.0566	-0.0680
D ↑	hold_rising to CP	-0.0212	-0.0266	-0.0364	-0.0435
D ↓	setup_rising to CP	0.0856	0.1029	0.1224	0.1473
D ↑	setup_rising to CP	0.0515	0.0563	0.0660	0.0763
SN ↓	min_pulse_width to SN	0.1353	0.1548	0.1868	0.2161
SN ↑	recovery_rising to CP	-0.0039	-0.0017	-0.0007	-0.0040
SN ↑	removal_rising to CP	0.0452	0.0502	0.0574	0.0667
TE ↓	hold_rising to CP	-0.0289	-0.0397	-0.0512	-0.0632
TE ↑	hold_rising to CP	-0.0635	-0.0706	-0.0852	-0.1053
TE ↓	setup_rising to CP	0.0808	0.0956	0.1205	0.1400
TE ↑	setup_rising to CP	0.1812	0.2180	0.2722	0.3206
TI ↓	hold_rising to CP	-0.1172	-0.1429	-0.1818	-0.2175
TI ↑	hold_rising to CP	-0.0654	-0.0725	-0.0876	-0.1081
TI ↓	setup_rising to CP	0.1761	0.2118	0.2613	0.3058
TI ↑	setup_rising to CP	0.0967	0.1080	0.1266	0.1420

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	5.327e-04	1.000e-20
X8_P4	1.931e-04	1.000e-20
X8_P10	6.256e-05	1.000e-20
X8_P16	2.918e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	1.459e-02	1.481e-02	1.519e-02	1.563e-02

Clock 100Mhz Data 25Mhz	1.528e-02	1.530e-02	1.559e-02	1.599e-02
Clock 100Mhz Data 50Mhz	1.597e-02	1.579e-02	1.599e-02	1.634e-02
Clock = 0 Data 100Mhz	8.002e-03	7.895e-03	7.853e-03	7.875e-03
Clock = 1 Data 100Mhz	3.709e-05	3.582e-05	3.492e-05	3.436e-05

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