

RISC-V: high performance embedded SweRV™ core microarchitecture, performance and CHIPS Alliance

Ted Marena

Western Digital Corporation

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Forward-Looking Statements

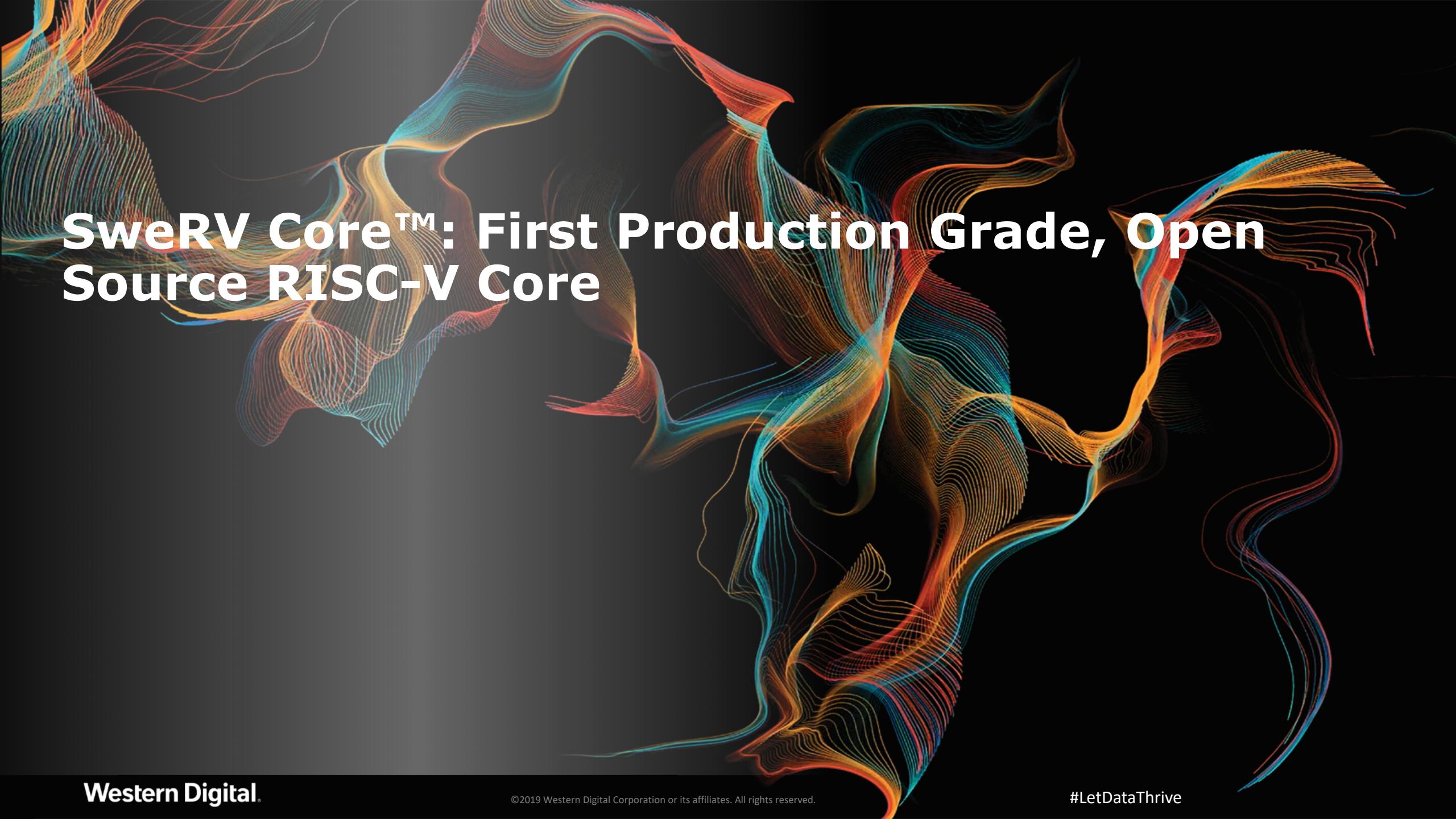
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This presentation contains certain forward-looking statements that involve risks and uncertainties, including, but not limited to, statements regarding: the RISC-V Foundation and its initiatives; our contributions to and investments in the RISC-V ecosystem; the transition of our devices, platforms and systems to RISC-V architectures; shipments of RISC-V processor cores; our business strategy, growth opportunities and technology development efforts; market trends and data growth and its drivers. Forward-looking statements should not be read as a guarantee of future performance or results, and will not necessarily be accurate indications of the times at, or by, which such performance or results will be achieved, if at all. Forward-looking statements are subject to risks and uncertainties that could cause actual performance or results to differ materially from those expressed in or suggested by the forward-looking statements.

Additional key risks and uncertainties include the impact of continued uncertainty and volatility in global economic conditions; actions by competitors; business conditions; growth in our markets; and pricing trends and fluctuations in average selling prices. More information about the other risks and uncertainties that could affect our business are listed in our filings with the Securities and Exchange Commission (the “SEC”) and available on the SEC’s website at www.sec.gov, including our most recently filed periodic report, to which your attention is directed. We do not undertake any obligation to publicly update or revise any forward-looking statement, whether as a result of new information, future developments or otherwise, except as otherwise required by law.

Agenda

- SweRV core
 - Microarchitecture
 - Performance benchmarks
- SweRV core ISS
- SweRV FPGA Design
- CHIPS Alliance
- Conclusion



SweRV Core™: First Production Grade, Open Source RISC-V Core

SweRV – Now Developed in CHIPS Alliance

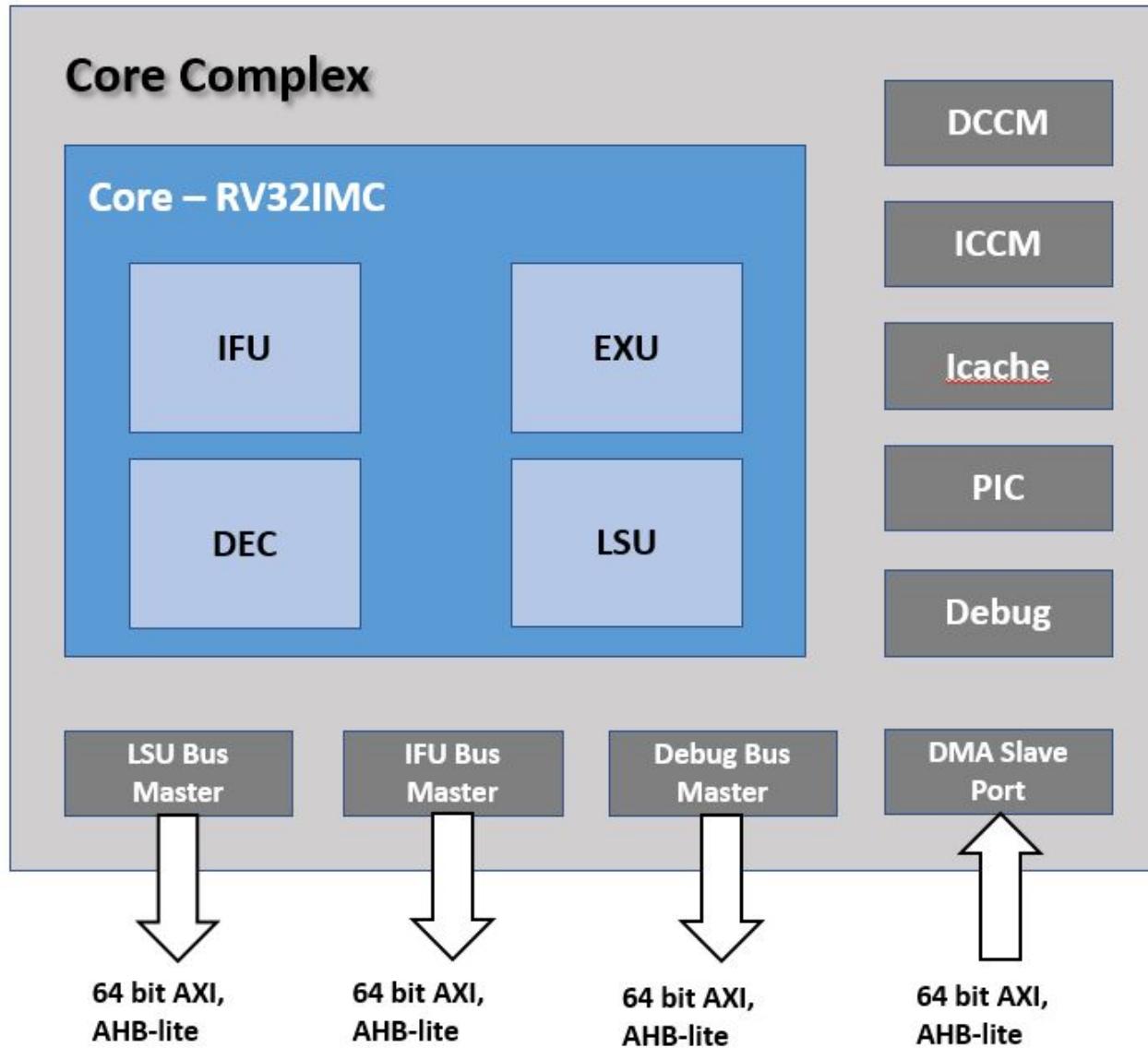
<https://github.com/chipsalliance/Cores-SweRV>

- SweRV has generated 100s of clones & tens of 1000s of views



- Future development will be in this open source hardware group

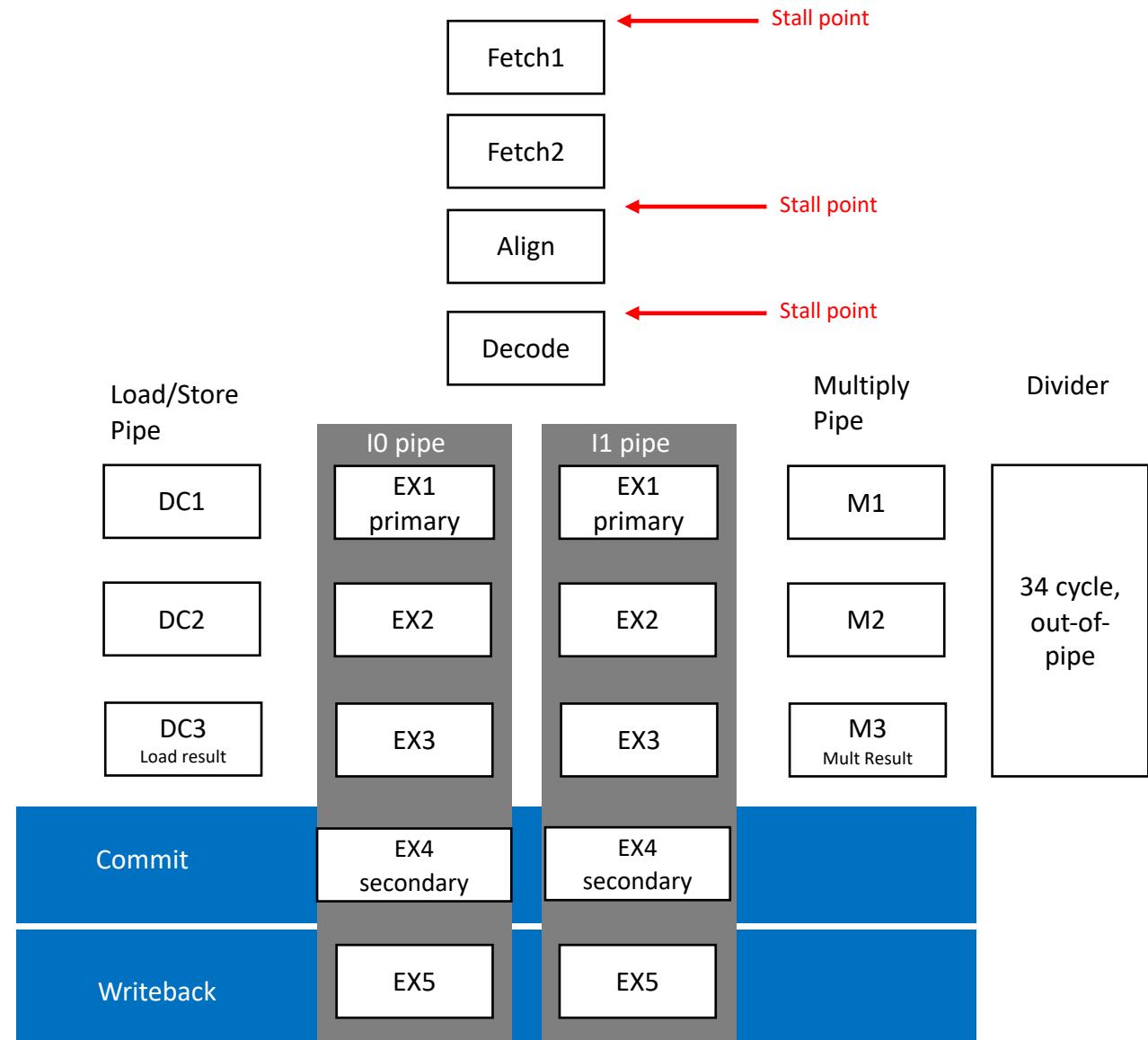
SweRV Core™ Complex



- RISCV 32IMC Core
 - First internally developed RISCV core
- RISCV debug support
- Programmable Interrupt Controller
 - Support for up to 255 external interrupts
- AHB-lite, AXI bus support
- Frequency target
 - 1 GHz at SSG process corner
- Technology
 - TSMC 28 nm

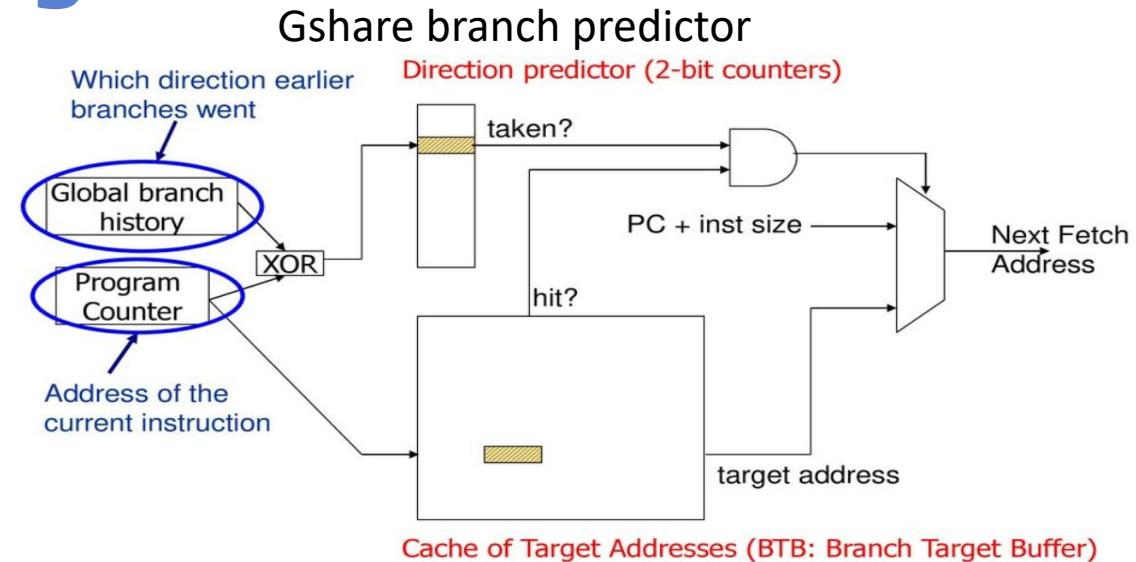
SweRV Microarchitecture

- 9 stage pipeline
- 3 stall points
 - Before Fetch
 - Align
 - Decode
- EX pipes
 - ALU ops statically assigned to I0, I1 pipes
- Load/store pipe
 - Load-to-use of 2
- Multiply pipe
 - 3 cycle pipelined multiplier
- Divide pipe
 - 34 cycles, out-of-pipe



SweRV - Branch Handling

- Branch direction is predicted using GSHARE algorithm
 - XOR of global branch history and PC
 - Used to lookup branch direction in branch history table (BHT)
 - PC hash
 - Used to lookup the branch target in branch target buffer (BTB)
- Predicted taken branches that hit in the BTB result in 1 cycle branch penalty
- Branches that mispredict in primary alus result in 4 cycle branch penalty
- Branches that mispredict in secondary alus result in 7 cycle branch penalty

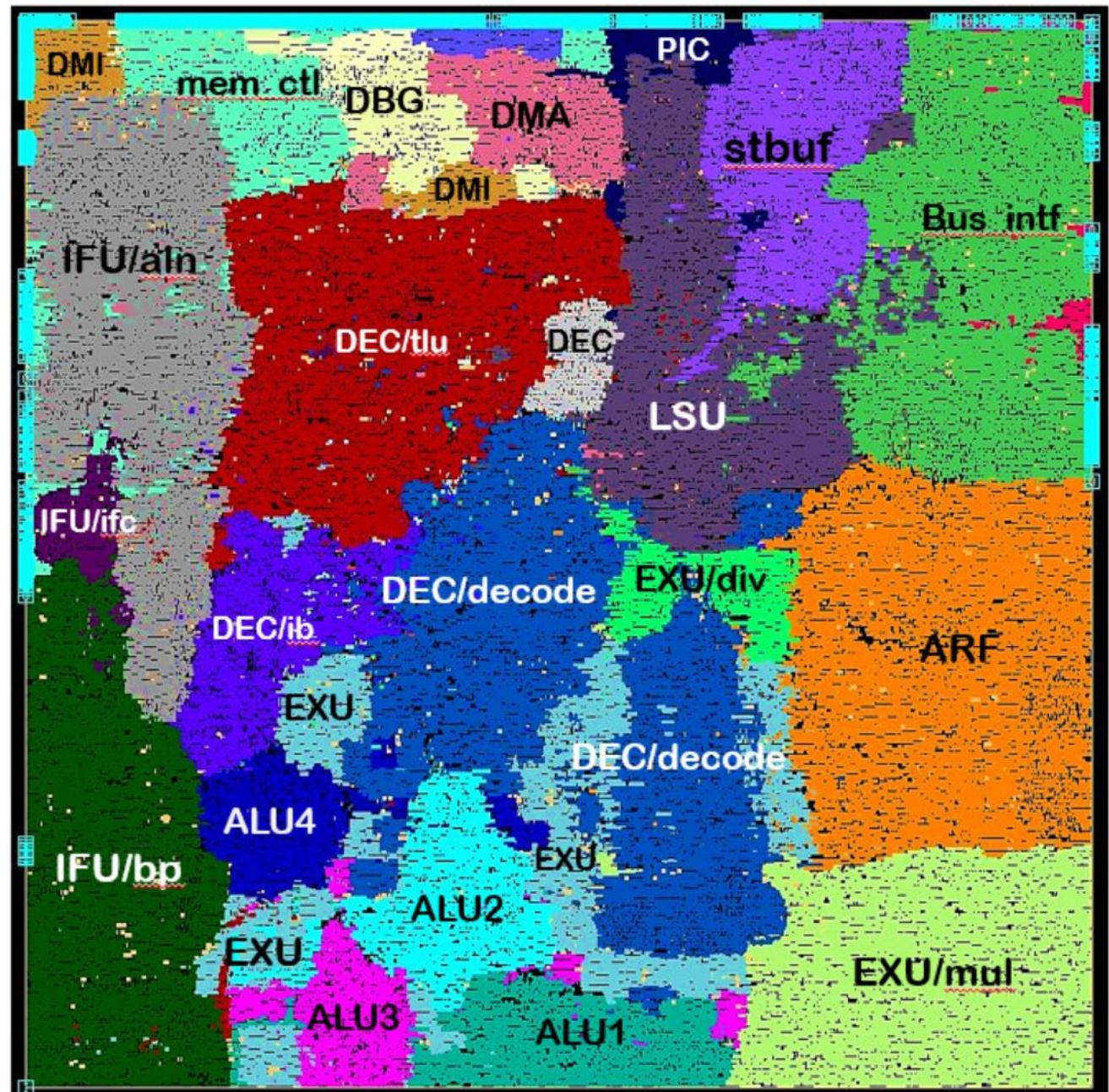


SweRV branch redirect cases:

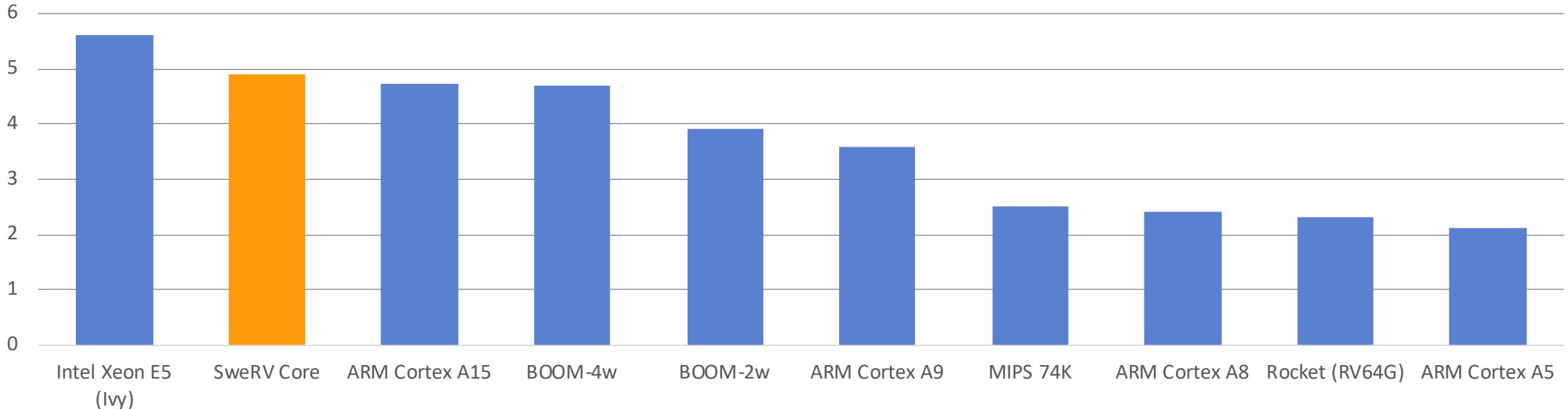
FETCH1		B		T1			T2		T3
FETCH2			B						
ALIGN				B					
DECODE					B				
E1/DC1						B			
E2/DC2							B		
E3/DC3								B	
E4/COMMIT									B
E5/WRITEB									B

SweRV Core Physical Design

- TSMC 28 nm
 - 125 C, SVT, 150 ps clock skew
- SSG corner w/out memories
 - 1 GHZ
 - .132 mm²
 - 800 MHZ
 - .100 mm²
 - 500 MHZ
 - .093 mm²
- TT corner w/out memories
 - 1 GHZ
 - .092 mm²
 - 800 MHZ
 - .091 mm²
 - 500 MHZ
 - .088 mm²



SweRV Core Performance



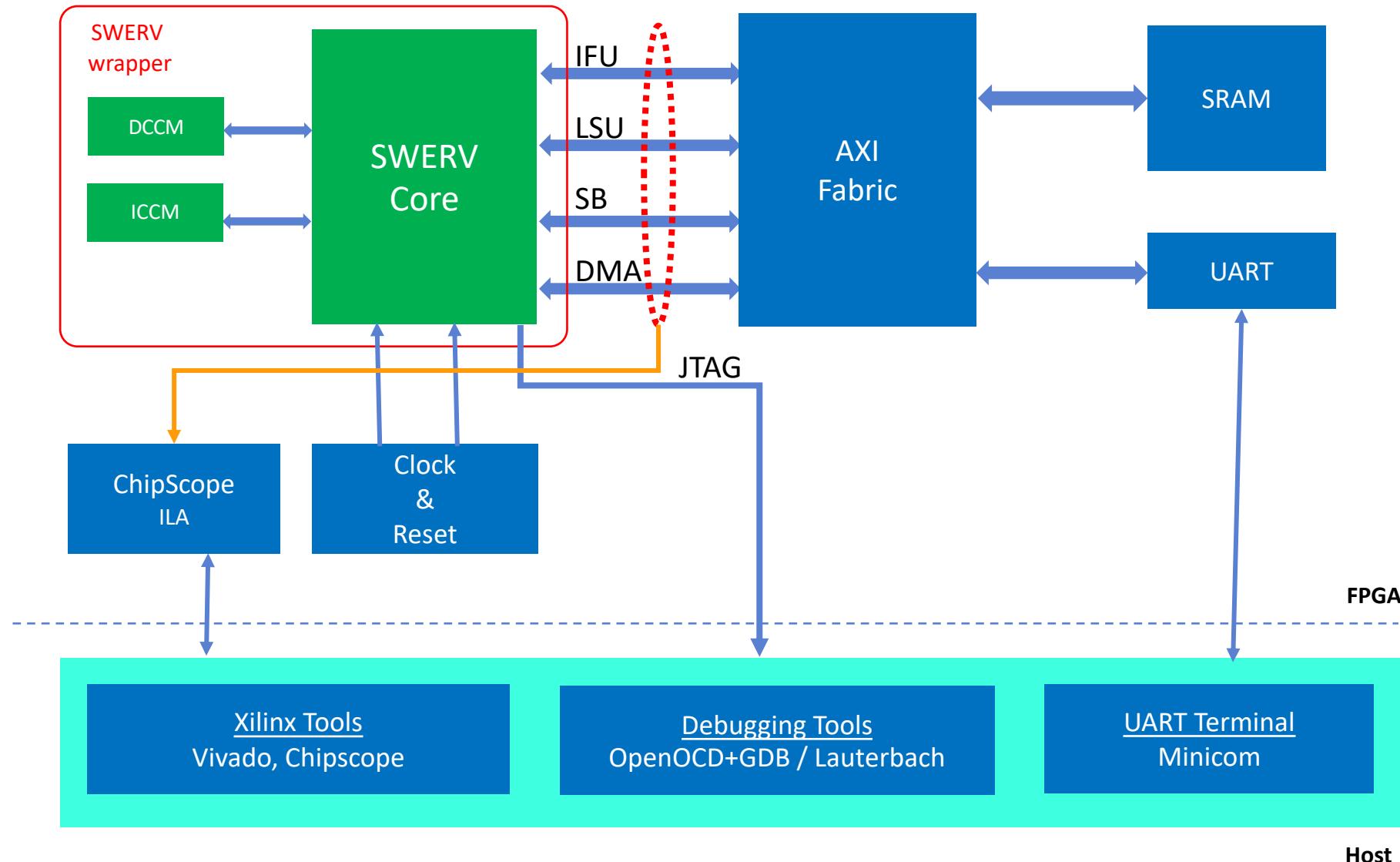
- 4.9 CoreMark/MHz
 - Additional performance gains are possible with compiler optimizations
 - Validated on FPGA model
- 2.3 DMIPs/MHz
 - <https://github.com/chipsalliance/Cores-SweRV>

CoreMark data from C.Celio, D.Patterson, K.Asanovic,<https://www2.eecs.berkeley.edu/Pubs/TechRpts/2015/EECS-2015-167.pdf>

SweRV Instruction Set Simulator

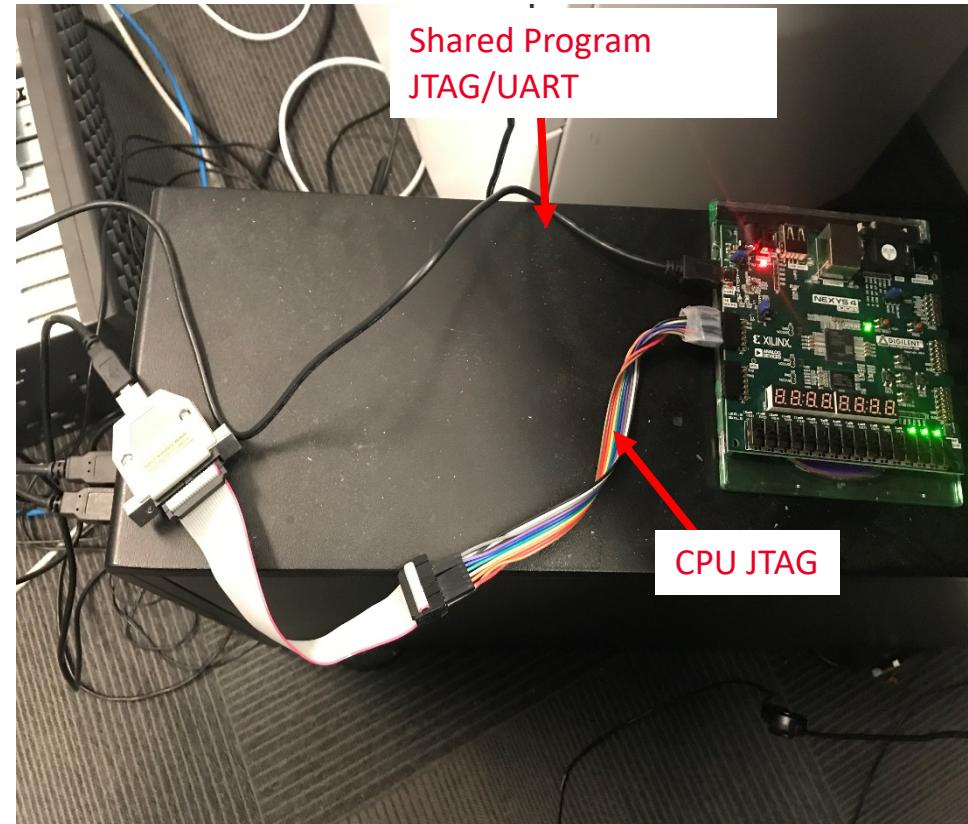
- Open sourced: <https://github.com/westerndigitalcorporation/swerv-ISS>
- SweRV core ISS is a set of tools for RISC-V functional and performance testing:
 - includes load and run RISC-V executable and linkable (ELF) binaries
 - Verilog format hexadecimal memory image files
- It currently implements the RV32I instruction set with M, F and C extensions, and RV64I:
 - All control and status registers are implemented and it is architected with multi-hart support
- In the interactive mode, the SweRV ISS can:
 - run and debug RISC-V software
 - examine RISC-V state and memory contents
 - run in single and multiple steps

SweRV Core Nexys4 Reference Design Overview



SweRV FPGA Prototype

- Prototype on Nexys-4 DDR board
 - Artix 7 FPGA (Xilinx part number XC7A100T-1CSG324C)
 - 128MiB DDR2
 - Quad-SPI flash
- System clock runs at 40 MHz
- Shared JTAG/UART port is primarily used to download the bit file on FPGA and UART printf.
- Olimex CPU JTAG probe is used to download and debug application software
- We used Xilinx Vivado 2018.2 toolchain for our reference design



https://github.com/westerndigitalcorporation/swerv_eh1_fpga

SweRV processor performance in Achronix

- **Performance**

- Fmax = 195MHz

- **Utilization**

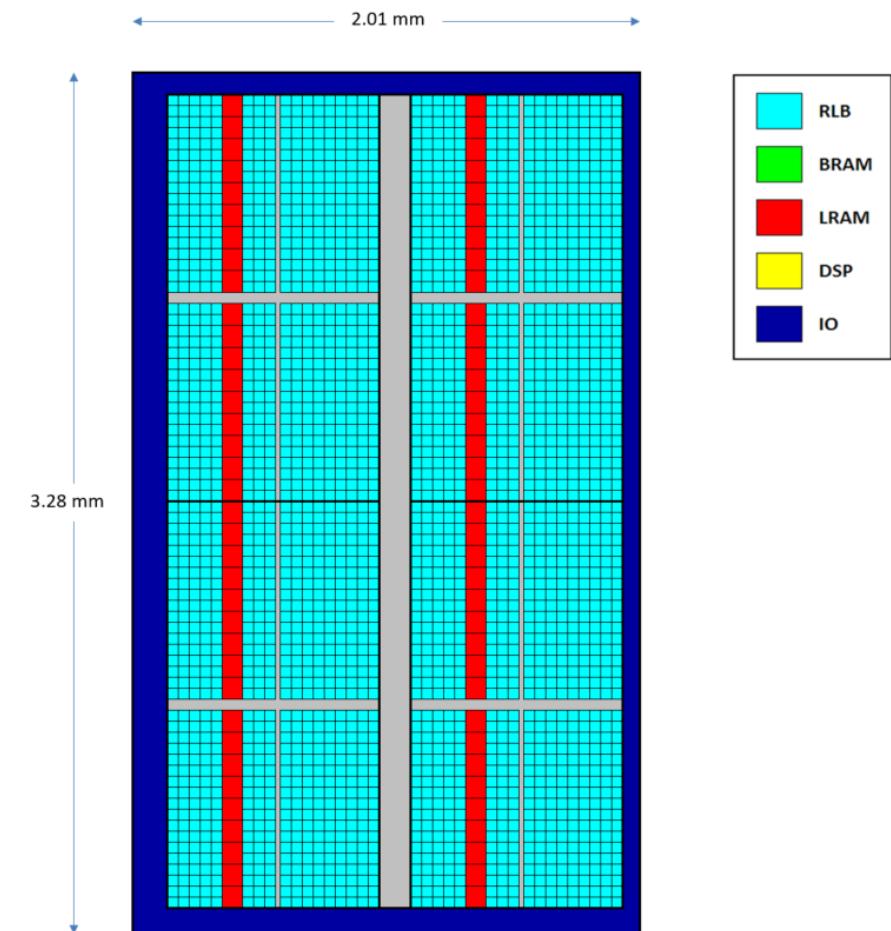
- 14K DFF
 - 29K LUT
 - 8x BRAM
 - 136x LRAM
 - 8x MLP72_INT16_MULT_2X

- **Die Size**

- 6.6mm² in TSMCN7



Collective Summary of All Corners					
Clock / Group	Slack (ns)		Frequency (MHz)		Comment
	setup	hold	Target	Upper Limit	
async_default	1.635	0.328	200.0	297.1	---
jtag_clk	48.307	0.119	10.0	295.3	---
sys_clk	-0.123	0.011	200.0	195.2	---



Configuration file and presentation at: <https://wdc.box.com/s/m3ys0pp9trtulnf3rng2kuzi7cytz6k6>

CHIPS Alliance – Open Source Collaboration for Hardware



What is CHIPS Alliance?

- Organization which develops and hosts:
 - High quality, open source hardware code (IP cores, interconnect IP, PHYs, etc)
 - Open source software development tools – design, verification,...
- A barrier free environment for collaboration:
 - Standards organization framework for collaboration and development
 - Roadmap definition for IP and tools
 - Legal framework – Apache v2 license
- Shared resources (\$ and time) which lower the cost of hardware development:
 - For RTL IP and tools

CHIPS Alliance – who are we?

- Open source hardware and open source design and verification tools
 - Fully open design methodology: from high level synthesis, to P&R, synthesis, physical design, PDks



Google

Esperanto
TECHNOLOGIES

imperas

Alibaba

codasip

antmicro

Western Digital.

SiFive

metrics

- Extraordinary individuals: Wilson Snyder, Olof Kindgren

CHIPS Alliance – organizational structure



Zvonimir Bandic
(Chairman)
Richard Ho (Vice-chairman)
Xiaoning Qi
Dave Ditzel
Yunsup Lee

CHIPS Alliance Board
of Directors

Ted Marena
Interim Director

Henry Cook
Technical Committee

Workgroup Chairs

Project maintainer 1

Project maintainer 2

Project maintainer 3

Verif. Engineer 1

SW Engineer 2

Brian Warner
Operations
Community Manager

Linux Foundation
Legal

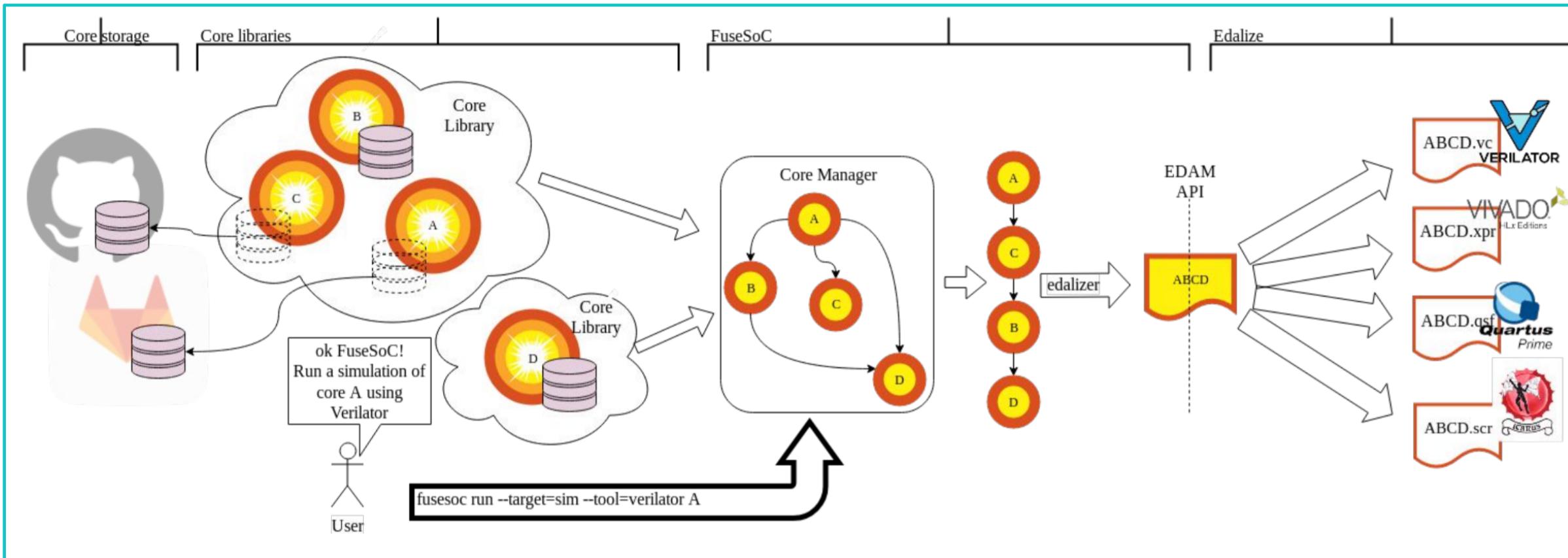
Linux Foundation
Finance / Operations

Michael Gieda
Outreach
Committee

Linux Foundation
Events

Advocacy + Outreach

Example Project Progress



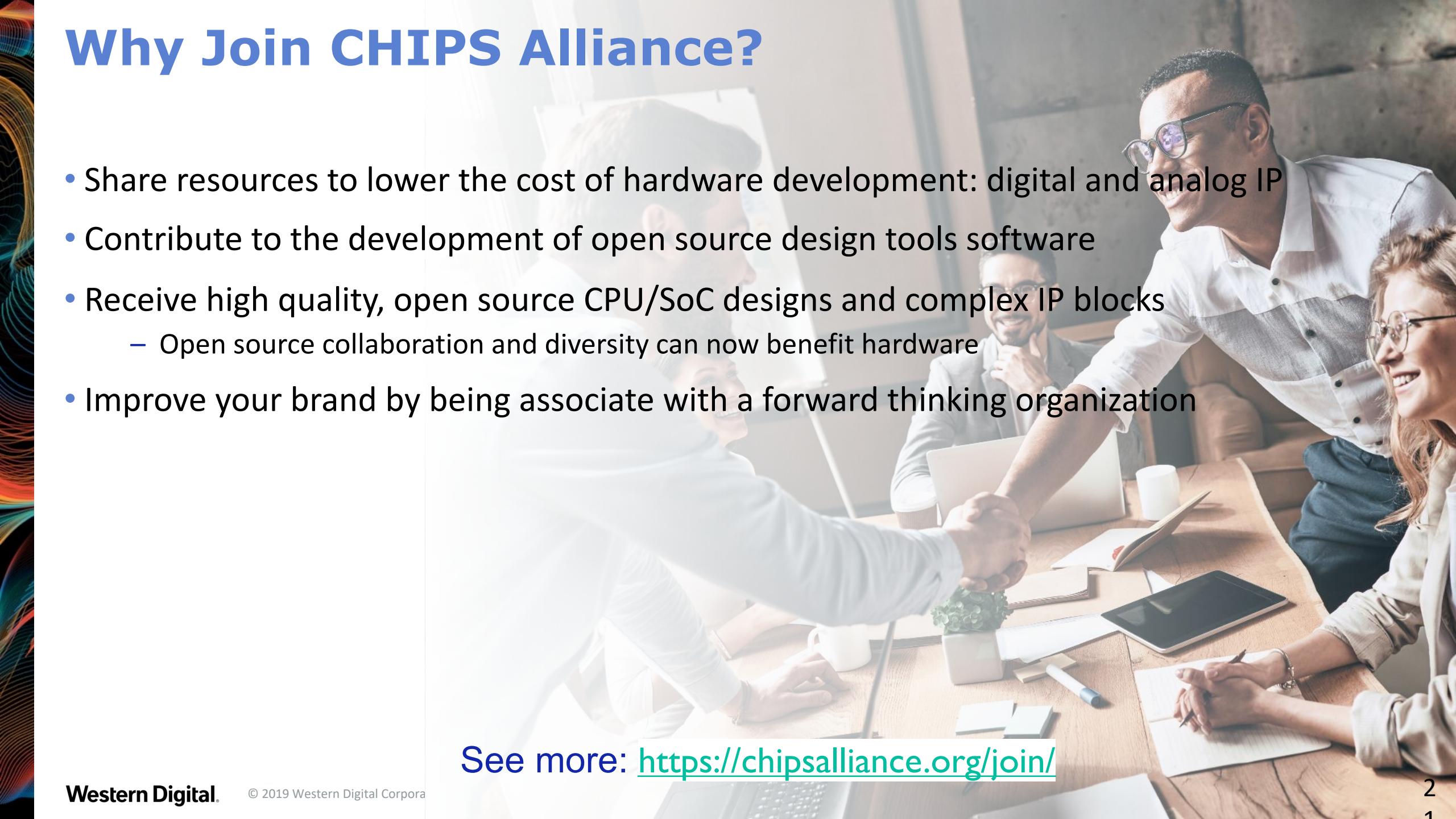
- FuseSoC is a package manager... ...and a build tool for HDL
 - Now supports SweRV Core

Events

- › First CHIPS Alliance workshop:
 - › Held in Mountain View, June 19 2019
- › Upcoming Workshops:
 - › Munich event in November
 - › Shanghai, China, During the week of March 9th
 - › Bay Area Workshop
- › For the latest: www.chipsalliance.org

Why Join CHIPS Alliance?

- Share resources to lower the cost of hardware development: digital and analog IP
- Contribute to the development of open source design tools software
- Receive high quality, open source CPU/SoC designs and complex IP blocks
 - Open source collaboration and diversity can now benefit hardware
- Improve your brand by being associate with a forward thinking organization



See more: <https://chipsalliance.org/join/>

Summary

- SweRV Core EH1 and SweRV ISS now available on Github
- SweRV Core FPGA design on Github
- Open sourced these to help accelerate the RISC-V Ecosystem
- Join CHIPS Alliance to accelerate RISC-V hardware and open source software development tools



BACKUP