C28SOI_SC_8_CLK_LL

Release Notes and Known Problems and Solutions

8 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

1 Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library name	C28SOI_SC_8_CLK_LL
Library version	5.3
Library type	Standard Cells
Technology	CMOS028_FDSOI

1.2 Related Documentation

- StandardCell_Notes.pdf Present in Design Package
- User Manual C28SOI_SC_8_CLK_LL_um.pdf present in doc directory of Product itself.
- Datasheets C28SOI_SC_8_CLK_LL_*_ds.pdf present in doc directory of Product itself.

2 Release Details

2.1 Current Release Details, Version 5.3

- LVF support has been added.
- The product remains aligned to DP28FDSOI 2.5 specifications.

2.2 Version 5.2

- Updated for Missing V1bar inside Abstract Views : In last release, there was an issue related to V1bar not visible inside Abstract Views (LEF & FRAM). It was present in layout but got missed in abstract views. Due to which DRC issue can happen as during P&R, tools work with abstract view and because of missing V1bar there, it can do some routing violating rules with V1bar, which can raise DRC issues during Signoff working with GDS. So Now Abstract views (LEF & FRAM) have been updated to have proper V1bar information. Also as abstract has changed, therefore corresponding footprint information modelled in libs has also got updated.
  - Issue was there only for few cells, so only below mentioned cells (All PolyBias : P0, P4,P10,P16) have been updated for V1bar -
    - C8T28SOIDV_LL_CNGFMUX21X30_P*

2.3 Version 5.1

- Cells have been re-characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.
- To enable support for Cadence Voltus Flow, CCS-Power has been added.
- Characterization corners have been re-defined in-line with DP Specifications.
- The product is aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.

2.4 Version 5.0

- Dummy Poly in layout across various cells has been cut for DFM robustness.
- Total 48 cells including All PolyBias (P0,P4,P10,P16) have been added to further enrich the offer.
  - Metastable Flops (SDFSYNCP*) optimized for Pulse width improvement
    - C8T28SOIDV_LL1_SDFSYNCPQX5_P*
    - C8T28SOIDV_LL1_SDFSYNCPRQX5_P*
    - C8T28SOIDV_LL1_SDFSYNCPSQX5_P*
  - Low Power and Area Clock Gating Cells
    - C8T28SOI_LLP1_CNHLSX10_P*
    - C8T28SOI_LLP1_CNHLSX14_P*
    - C8T28SOI_LLP1_CNHLSX19_P*
    - C8T28SOI_LLP1_CNHLSX24_P*
    - C8T28SOI_LLP1_CNHLSX29_P*

- C8T28SOI_LLP1_CNHLSX34_P*
- C8T28SOI_LLP1_CNHLSX38_P*
- C8T28SOI_LLP1_CNHLSX57_P*

– Glitch Free Mux for Clock Switching
- C8T28SOIDV_LL_CNGFMUX21X30_P*

■ Total 108 cells have been updated for Robustness relative to contact punch through effect. Minimum Enclosure of 20nm for RX/CA has been ensured. There is no change in Cell Area and Abstract because of contact robustness update.

– Updated cells (All PolyBias : P0, P4,P10,P16) are -

C8T28SOIDV_LL_CNIVX18_P*	C8T28SOIDV_LL_CNIVX74_P*
C8T28SOIDV_LL_CNLDLRQX19_P*	C8T28SOIDV_LL_CNMUX41X27_P*
C8T28SOIDV_LL_SDFSYNCPRQX5_P*	C8T28SOIDV_LL_SDFSYNCPSQX5_P*
C8T28SOI_LL_CNAND2X19_P*	C8T28SOI_LL_CNBFX12_P*
C8T28SOI_LL_CNBFX23_P*	C8T28SOI_LL_CNBFX37_P*
C8T28SOI_LL_CNBFX54_P*	C8T28SOI_LL_CNBFX8_P*
C8T28SOI_LL_CNIVX74_P*	C8T28SOI_LL_CNMUX21X27_P*
C8T28SOI_LL_CNNOR2AX27_P*	C8T28SOI_LL_CNNOR2X27_P*
C8T28SOI_LL_CNOR2X19_P*	C8T28SOI_LL_CNOR3X14_P*
C8T28SOI_LL_DLYHFM4X4_P*	C8T28SOI_LL_DLYHFM8X12_P*
C8T28SOI_LL_DLYHFM8X30_P*	C8T28SOI_LL_DLYHFM8X4_P*
C8T28SOI_LLP_CNHLSX27_P*	C8T28SOI_LLP_CNHLSX30_P*
C8T28SOI_LLP_CNHLSX38_P*	C8T28SOI_LLP_CNHLSX54_P*
C8T28SOI_LLP_CNHLSX9_P*	

■ Cells has been characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.

■ The product has been aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.

■ For Global Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.5 Version 4.0

■ Total 12 cells have been added to further enrich the offer.

– Balanced AND-OR Boolean Function
- C8T28SOI_LL_CNAO12X19_P*

– Balanced LATCH cells
- C8T28SOIDV_LL_CNLDLRQX19_P*

– High Drive DLY cells
- C8T28SOI_LL_DLYHFM8X30_P*

■ For EMG protection, In High Drive cells, routing on thin (comb) part of fatpin was blocked through Route Guide in Milkyway and obstruction in cadence LEF. In previous Library version, the pin shape was removed under obstruction from CADENCE LEF when there was an obstruction overlapping a pin. But with this method, PnR tool was not able to correctly understand the shape of pin. Therefore LEF generation algorithm has been updated not to delete obstruction under pin shape but rather to have the obstruction with

"SPACING 0.0" (equivalent to zero-min-spacing route guide for FRAM). Due to this Algorithm Update, CADENCE LEF is changed).

- The product has been aligned to DP28FDSOI 2.4 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.6 Version 3.0

- For EMG protection, In High Drive cells of CLK library, routing on thin (comb) part of fatpin has been blocked through Route Guide in Milkyway and obstruction in cadence LEF. Therfore, there is change in Abstract for few cells mentioned below.

  – Cells with Change in Abstract (152 cells including All PolyBias: P0,P4,P10,P16)

C8T28SOIDV_LL_CNBFX28_P*	C8T28SOIDV_LL_CNBFX37_P*
C8T28SOIDV_LL_CNBFX55_P*	C8T28SOIDV_LL_CNBFX74_P*
C8T28SOIDV_LL_CNIVX28_P*	C8T28SOIDV_LL_CNIVX37_P*
C8T28SOIDV_LL_CNIVX55_P*	C8T28SOIDV_LL_CNIVX74_P*
C8T28SOIDV_LL_CNMUX41X27_P*	C8T28SOIDV_LL_CNOR3X27_P*
C8T28SOIDV_LL_CNOR4X27_P*	C8T28SOI_LL_CNAND2X19_P*
C8T28SOI_LL_CNAND2X27_P*	C8T28SOI_LL_CNAND3X27_P*
C8T28SOI_LL_CNBFX23_P*	C8T28SOI_LL_CNBFX28_P*
C8T28SOI_LL_CNBFX32_P*	C8T28SOI_LL_CNBFX37_P*
C8T28SOI_LL_CNBFX54_P*	C8T28SOI_LL_CNIVX18_P*
C8T28SOI_LL_CNIVX22_P*	C8T28SOI_LL_CNIVX27_P*
C8T28SOI_LL_CNIVX32_P*	C8T28SOI_LL_CNIVX37_P*
C8T28SOI_LL_CNIVX74_P*	C8T28SOI_LL_CNMUX21X27_P*
C8T28SOI_LL_CNNAND2AX27_P*	C8T28SOI_LL_CNNAND2X27_P*
C8T28SOI_LL_CNNOR2AX27_P*	C8T28SOI_LL_CNNOR2X27_P*
C8T28SOI_LL_CNOR2X19_P*	C8T28SOI_LL_CNOR2X37_P*
C8T28SOI_LL_CNXOR2X27_P*	C8T28SOI_LLP_CNHLSX21_P*
C8T28SOI_LLP_CNHLSX27_P*	C8T28SOI_LLP_CNHLSX30_P*
C8T28SOI_LLP_CNHLSX38_P*	C8T28SOI_LLP_CNHLSX54_P*

- Tau Infomation "doc/Tau_Info.csv" has been added in this release.
- The product has been aligned to DP28FDSOI 2.3 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.7 Version 2.2

- Total 180 cells including All PolyBias varients : P0, P4,P10,P16 have been updated to have better manufacturability. Cell Area is not changed for these cells but there are few cells for which abstract is changed. Updated Cells are -

  – Cells with Change in Abstract (96 cells including All PolyBias varients)

C8T28SOIDV_LL_CNBFX28_P*	C8T28SOIDV_LL_CNBFX37_P*
C8T28SOIDV_LL_CNBFX74_P*	C8T28SOIDV_LL_CNIVX74_P*
C8T28SOIDV_LL_CNMUX41X27_P*	C8T28SOIDV_LL_CNOR3X27_P*
C8T28SOIDV_LL_CNOR4X27_P*	C8T28SOIDV_LL_CNSDFPSQTX9_P*
C8T28SOI_LL_CNAND2X19_P*	C8T28SOI_LL_CNAND2X27_P*
C8T28SOI_LL_CNBFX37_P*	C8T28SOI_LL_CNBFX54_P*
C8T28SOI_LL_CNIVX27_P*	C8T28SOI_LL_CNIVX74_P*
C8T28SOI_LL_CNNAND2X15_P*	C8T28SOI_LL_CNNOR2X15_P*
C8T28SOI_LL_CNOR2X19_P*	C8T28SOI_LL_CNXOR2X27_P*
C8T28SOI_LLP_CNHLSX13_P*	C8T28SOI_LLP_CNHLSX17_P*
C8T28SOI_LLP_CNHLSX21_P*	C8T28SOI_LLP_CNHLSX4_P*
C8T28SOI_LLP_CNHLSX54_P*	C8T28SOI_LLP_CNHLSX9_P*

  – Cells without any change in Abstract (84 cells including All PolyBias varients)

C8T28SOIDV_LL_CNBFX55_P*	C8T28SOIDV_LL_CNIVX28_P*
C8T28SOIDV_LL_CNIVX37_P*	C8T28SOIDV_LL_CNIVX55_P*
C8T28SOI_LL_CNAND3X27_P*	C8T28SOI_LL_CNBFX23_P*
C8T28SOI_LL_CNBFX28_P*	C8T28SOI_LL_CNBFX32_P*
C8T28SOI_LL_CNIVX18_P*	C8T28SOI_LL_CNIVX22_P*
C8T28SOI_LL_CNIVX32_P*	C8T28SOI_LL_CNIVX37_P*
C8T28SOI_LL_CNMUX21X27_P*	C8T28SOI_LL_CNNAND2AX27_P*
C8T28SOI_LL_CNNAND2X27_P*	C8T28SOI_LL_CNNOR2AX27_P*
C8T28SOI_LL_CNNOR2X27_P*	C8T28SOI_LL_CNOR2X37_P*
C8T28SOI_LLP_CNHLSX27_P*	C8T28SOI_LLP_CNHLSX30_P*
C8T28SOI_LLP_CNHLSX38_P*	

- Library has been re-characterized only for these updated 180 cells and all views has been updated accordingly.
- Tau Infomation "doc/Tau_Info.csv" has been removed in this version of Product.
- The Product remains aligned to DP28FDSOI_7ML 1.0.

2.8 Version 2.1

- 56 new Cells have been added (All PolyBias : P0, P4,P10,P16)

– Higher Drive combinational cells (X27 Drive)
  - C8T28SOI_LL_CNAND2X27_P*
  - C8T28SOI_LL_CNAND3X27_P*
  - C8T28SOI_LL_CNNOR2AX27_P*
  - C8T28SOI_LL_CNNOR2X27_P*
  - C8T28SOIDV_LL_CNOR3X27_P*
  - C8T28SOIDV_LL_CNOR4X27_P*
  - C8T28SOI_LL_CNNAND2AX27_P*
  - C8T28SOI_LL_CNNAND2X27_P*
  - C8T28SOI_LL_CNMUX21X27_P*
  - C8T28SOI_LL_CNXOR2X27_P*

– Higher Drive Delay cells (X12 Drive)
  - C8T28SOI_LL_DLYHFM4X12_P*
  - C8T28SOI_LL_DLYHFM8X12_P*

– New Functionality - CNMUX41
  - C8T28SOIDV_LL_CNMUX41X9_P*
  - C8T28SOIDV_LL_CNMUX41X27_P*

■ 12 Cells (SYNCLVHP Flops) have been removed as these flops were not having significant gain in TAU value at low voltage with respect to normal SYNCP Flops offered in this library itself -
  – C8T28SOITV_LL_SDFSYNCLVHPPQX5_P* (P0/P4/P10/P16)
  – C8T28SOITV_LL_SDFSYNCLVHPPRQX5_P* (P0/P4/P10/P16)
  – C8T28SOITV_LL_SDFSYNCLVHPPSQX5_P* (P0/P4/P10/P16)

■ Tau_Info.csv has been updated to have more accurate and correct Tau Information for Balanced Flops (CNSDFP*) and Metastable Flops (SDFSYNCP*)

■ The Product remains aligned to DP28FDSOI_7ML 1.0.

2.9 Version 2.0

■ The Product is aligned to DP28FDSOI_7ML 1.0. Refer to Design Package Documents for more details.

■ For Standard Cell Library Specific Features, Refer to StandardCell_Notes.pdf Present in Design Package.

3 Known Problems and Solutions

3.1 DP related Generic Problems

- For Generic Standard cell Library related problem for this DP, please refer to KPS section inside StandardCell_Notes.pdf Present in Design Package.

3.2 Placement Restriction

➥ Specific Placement restriction due to Poly Landing pad

☞ Placement restriction has been modelled in CADENCE LEF - through “Symmetry property” and in SYNOPSYS FRAM - through “spacing_label property” for the following cells:

- C8T28SOI_LL_CNIVX2_P0
- C8T28SOI_LL_CNIVX2_P10
- C8T28SOI_LL_CNIVX2_P16
- C8T28SOI_LL_CNIVX2_P4
- C8T28SOI_LL_CNIVX4_P0
- C8T28SOI_LL_CNIVX4_P10
- C8T28SOI_LL_CNIVX4_P16
- C8T28SOI_LL_CNIVX4_P4

	*As mentioned above, modelling the placement constraint is different between Synopsys and Cadence. Therefore Need to be careful, if You do P&R with Synopsys and then go inside Cadence, the placement created by ICC could be declared as invalid by Encounter tool.*

3.3 Dont_use and dont_touch cells

➥ Specific attributes dont_use and dont_touch in Synopsys Technology File

☞ The “dont_touch” and “dont_use” attributes are defined in the Synopsys Technology Files for few cells. Reason can be -

a) Cell has some specific custom feature. Therefore We want to ensure that Either these cells are not automatically picked during Synthesis unless the designer

wishes to specically use them in the design or those are not replaced during Design Optimization.

b) Cell's functionality is not properly understood by tools.

Cells with such attributes are as following:

- C8T28SOIDV_LL_SDFSYNCPQX5_P*
- C8T28SOIDV_LL_SDFSYNCPRQX5_P*
- C8T28SOIDV_LL_SDFSYNCPSQX5_P*
- C8T28SOIDV_LL1_SDFSYNCPQX5_P*
- C8T28SOIDV_LL1_SDFSYNCPRQX5_P*
- C8T28SOIDV_LL1_SDFSYNCPSQX5_P*
- C8T28SOI_LLP_CNHLSX13_P*
- C8T28SOI_LLP_CNHLSX17_P*
- C8T28SOI_LLP_CNHLSX21_P*
- C8T28SOI_LLP_CNHLSX27_P*
- C8T28SOI_LLP_CNHLSX30_P*
- C8T28SOI_LLP_CNHLSX38_P*
- C8T28SOI_LLP_CNHLSX4_P*
- C8T28SOI_LLP_CNHLSX54_P*
- C8T28SOI_LLP_CNHLSX9_P*
- C8T28SOI_LLP1_CNHLSX10_P*
- C8T28SOI_LLP1_CNHLSX14_P*
- C8T28SOI_LLP1_CNHLSX19_P*
- C8T28SOI_LLP1_CNHLSX24_P*
- C8T28SOI_LLP1_CNHLSX29_P*
- C8T28SOI_LLP1_CNHLSX34_P*
- C8T28SOI_LLP1_CNHLSX38_P*
- C8T28SOI_LLP1_CNHLSX57_P*

4 Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.

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