C28SOI_SC_12_CORE_LR
Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells

Overview

- C28SOI_SC_12_CORE_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

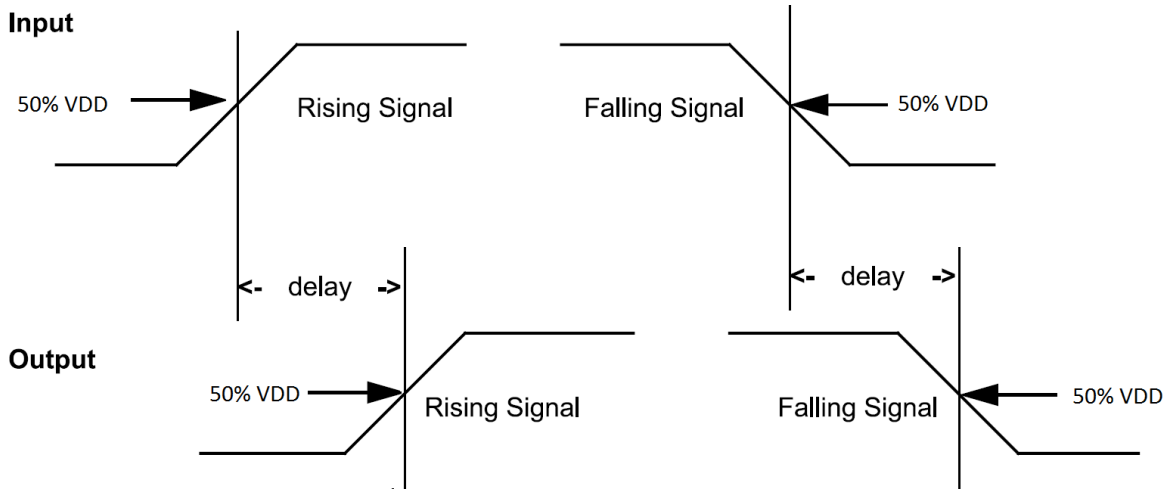


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

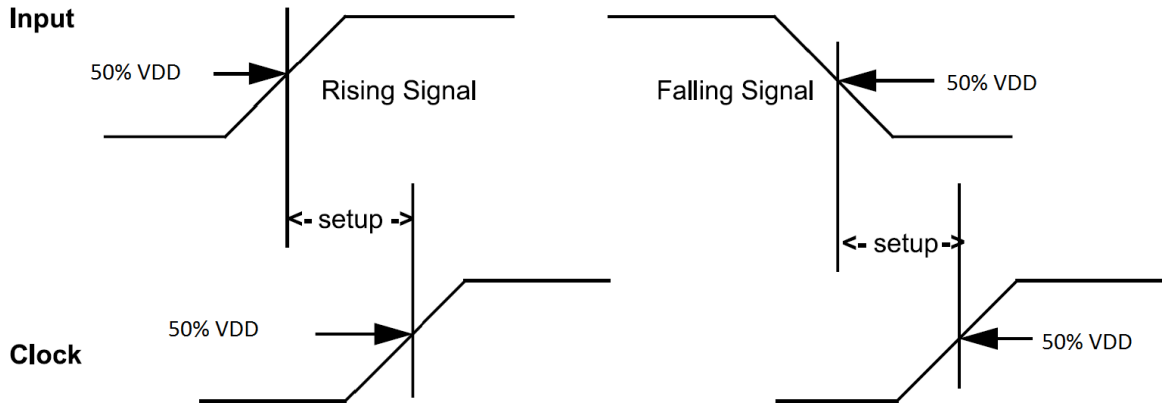


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

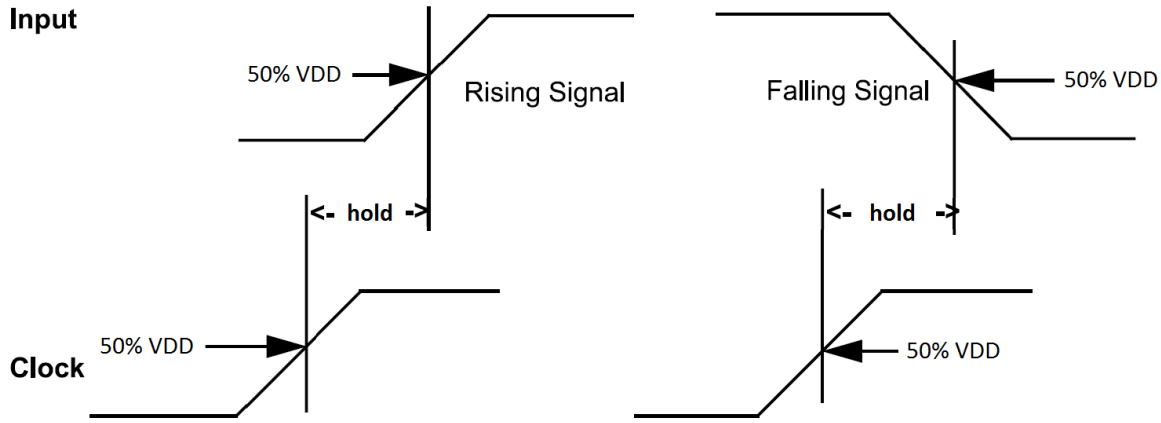


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

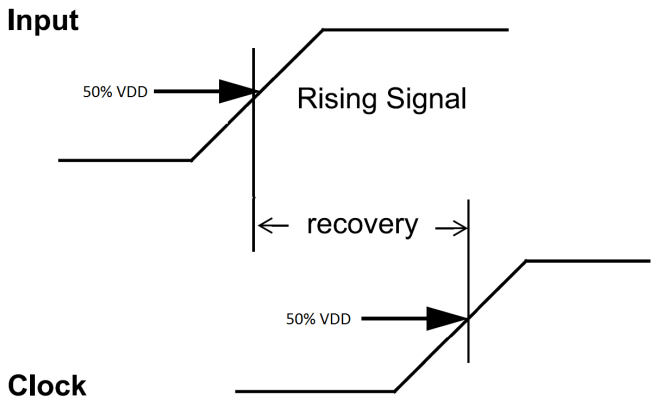


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

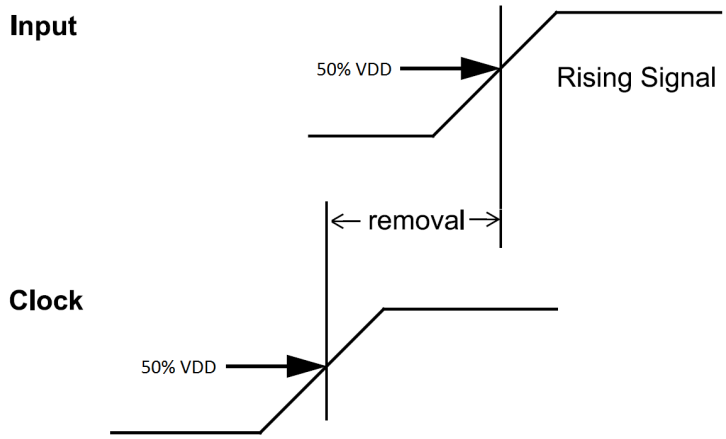


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

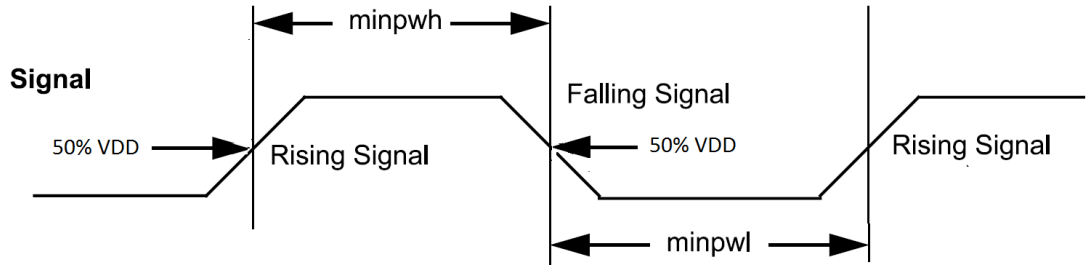


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

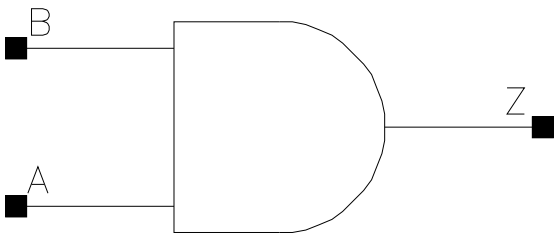
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X25_P0	1.200	1.088	1.3056
X33_P0	1.200	1.360	1.6320
X42_P0	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0008	0.0011	0.0017	0.0020
B	0.0007	0.0010	0.0016	0.0020
	X42_P0			
A	0.0020			
B	0.0020			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0225	0.0189	1.5250	0.7716
A to Z ↑	0.0166	0.0160	2.3330	1.1278
B to Z ↓	0.0213	0.0179	1.5254	0.7710
B to Z ↑	0.0178	0.0172	2.3309	1.1271
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0196	0.0190	0.5107	0.3809

A to Z ↑	0.0156	0.0162	0.7457	0.5641
B to Z ↓	0.0186	0.0175	0.5100	0.3801
B to Z ↑	0.0167	0.0171	0.7459	0.5637
	X42_P0		**X42_P0**	
A to Z ↓	0.0206		0.3094	
A to Z ↑	0.0178		0.4520	
B to Z ↓	0.0190		0.3088	
B to Z ↑	0.0188		0.4513	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	6.243e-05	1.145e-09
X16_P0	1.252e-04	1.310e-09
X25_P0	1.799e-04	1.807e-09
X33_P0	2.413e-04	2.139e-09
X42_P0	2.772e-04	2.304e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	2.077e-05	3.887e-05	5.967e-05	1.414e-04
B (output stable)	2.738e-05	4.892e-05	7.655e-05	2.860e-04
A to Z	3.500e-03	6.080e-03	9.340e-03	1.234e-02
B to Z	3.390e-03	5.907e-03	9.058e-03	1.168e-02
	X42_P0			
A (output stable)	1.412e-04			
B (output stable)	2.832e-04			
A to Z	1.496e-02			
B to Z	1.428e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

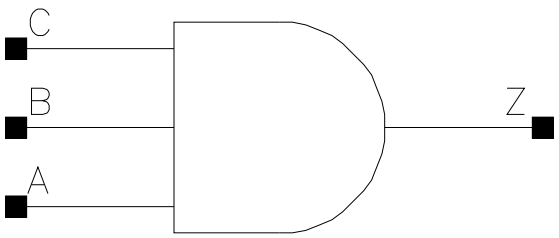
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	9.741e-08	8.497e-08	2.400e-08	7.679e-08
B (output stable)	9.930e-08	8.735e-08	7.220e-08	5.190e-08
A to Z	1.091e-06	1.018e-06	3.185e-06	1.990e-06
B to Z	4.071e-07	8.212e-08	7.750e-07	-1.148e-07
	X42_P0			
A (output stable)	7.753e-08			
B (output stable)	5.370e-08			
A to Z	1.256e-06			
B to Z	-4.750e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X25_P0	1.200	1.360	1.6320
X33_P0	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0007	0.0011	0.0018	0.0021
B	0.0006	0.0011	0.0016	0.0020
C	0.0007	0.0011	0.0015	0.0019

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0242	0.0208	1.5414	0.7533
A to Z ↑	0.0209	0.0201	2.3490	1.1179
B to Z ↓	0.0234	0.0199	1.5412	0.7527
B to Z ↑	0.0222	0.0215	2.3495	1.1177
C to Z ↓	0.0223	0.0188	1.5385	0.7514
C to Z ↑	0.0232	0.0221	2.3475	1.1178
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0208	0.0199	0.5170	0.3867

A to Z ↑	0.0197	0.0190	0.7664	0.5738
B to Z ↓	0.0199	0.0189	0.5168	0.3856
B to Z ↑	0.0210	0.0203	0.7658	0.5737
C to Z ↓	0.0188	0.0180	0.5163	0.3857
C to Z ↑	0.0218	0.0212	0.7659	0.5735

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	5.402e-05	1.310e-09
X17_P0	1.103e-04	1.476e-09
X25_P0	1.594e-04	2.139e-09
X33_P0	2.116e-04	2.304e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	2.387e-05	4.667e-05	6.434e-05	8.638e-05
B (output stable)	2.907e-05	5.550e-05	8.123e-05	1.087e-04
C (output stable)	5.276e-05	9.917e-05	1.480e-04	2.050e-04
A to Z	3.862e-03	6.997e-03	1.024e-02	1.319e-02
B to Z	3.723e-03	6.760e-03	9.851e-03	1.267e-02
C to Z	3.618e-03	6.561e-03	9.526e-03	1.224e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

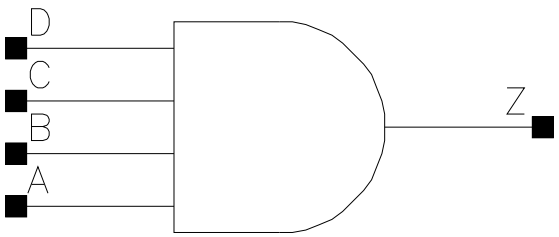
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	1.105e-07	9.504e-08	7.343e-08	6.147e-08
B (output stable)	1.119e-07	8.985e-08	7.883e-08	6.772e-08
C (output stable)	1.030e-07	9.544e-08	7.997e-08	6.639e-08
A to Z	2.412e-07	1.041e-07	3.179e-07	1.582e-07
B to Z	1.386e-08	-3.016e-07	-5.686e-07	-3.131e-07
C to Z	-3.120e-08	-9.300e-08	-1.958e-08	-1.140e-06

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X6_P0	1.200	1.088	1.3056
X20_P0	1.200	2.312	2.7744
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P0	X6_P0	X20_P0	X27_P0
A	0.0006	0.0008	0.0018	0.0020
B	0.0005	0.0008	0.0018	0.0020
C	0.0005	0.0008	0.0017	0.0020
D	0.0005	0.0008	0.0018	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X6_P0	X4_P0	X6_P0
A to Z ↓	0.0250	0.0221	2.7748	1.8444
A to Z ↑	0.0225	0.0174	7.8271	4.3110
B to Z ↓	0.0241	0.0207	2.7745	1.8432
B to Z ↑	0.0239	0.0183	7.8305	4.3115
C to Z ↓	0.0258	0.0236	2.7457	1.8521
C to Z ↑	0.0227	0.0175	7.8338	4.3177

D to Z ↓	0.0249	0.0220	2.7434	1.8523
D to Z ↑	0.0246	0.0184	7.8373	4.3168
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0215	0.0202	0.5445	0.3861
A to Z ↑	0.0180	0.0207	1.4470	1.1028
B to Z ↓	0.0197	0.0186	0.5431	0.3851
B to Z ↑	0.0187	0.0217	1.4471	1.1029
C to Z ↓	0.0211	0.0195	0.5468	0.3870
C to Z ↑	0.0162	0.0182	1.4463	1.1017
D to Z ↓	0.0192	0.0180	0.5457	0.3855
D to Z ↑	0.0167	0.0191	1.4460	1.1010

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	3.906e-05	1.807e-09
X6_P0	8.070e-05	1.807e-09
X20_P0	2.241e-04	3.298e-09
X27_P0	2.630e-04	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	5.832e-04	9.447e-04	2.748e-03	3.363e-03
B (output stable)	5.499e-04	8.796e-04	2.556e-03	3.161e-03
C (output stable)	5.602e-04	9.528e-04	2.414e-03	2.962e-03
D (output stable)	5.315e-04	8.841e-04	2.206e-03	2.749e-03
A to Z	2.391e-03	3.757e-03	1.124e-02	1.458e-02
B to Z	2.312e-03	3.599e-03	1.055e-02	1.389e-02
C to Z	2.394e-03	3.863e-03	9.922e-03	1.257e-02
D to Z	2.312e-03	3.698e-03	9.243e-03	1.191e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

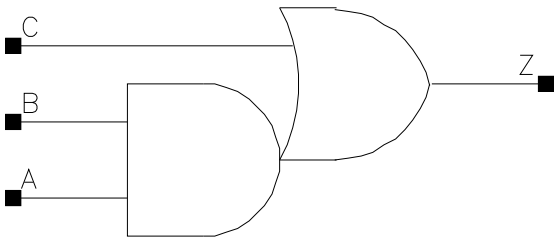
Pin Cycle (vdds)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	3.561e-07	1.635e-07	4.885e-07	1.966e-06
B (output stable)	3.369e-07	2.371e-07	6.882e-07	1.875e-06
C (output stable)	1.967e-07	2.936e-07	9.450e-07	8.856e-07
D (output stable)	1.325e-07	2.360e-07	4.627e-07	5.233e-07
A to Z	8.869e-07	1.788e-07	4.080e-06	5.940e-06
B to Z	8.490e-08	4.982e-07	4.762e-06	3.624e-06
C to Z	-1.406e-07	6.762e-07	2.463e-06	-1.296e-06
D to Z	-1.957e-07	-3.998e-07	1.323e-06	-2.715e-06

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0007	0.0010	0.0021
B	0.0007	0.0010	0.0019
C	0.0008	0.0011	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0285	0.0262	1.5622	0.7642
A to Z ↑	0.0172	0.0157	2.2595	1.1121
B to Z ↓	0.0265	0.0243	1.5550	0.7616
B to Z ↑	0.0186	0.0172	2.2592	1.1108
C to Z ↓	0.0266	0.0245	1.5550	0.7616
C to Z ↑	0.0164	0.0156	2.2464	1.1061
	X33_P0		**X33_P0**	
A to Z ↓	0.0262		0.3886	
A to Z ↑	0.0161		0.5605	

B to Z ↓	0.0245		0.3878	
B to Z ↑	0.0173		0.5602	
C to Z ↓	0.0247		0.3873	
C to Z ↑	0.0155		0.5579	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	7.535e-05	1.310e-09
X17_P0	1.441e-04	1.476e-09
X33_P0	2.834e-04	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	6.319e-05	9.895e-05	2.331e-04
B (output stable)	6.661e-05	1.074e-04	2.678e-04
C (output stable)	7.887e-05	1.326e-04	3.019e-04
A to Z	3.696e-03	6.655e-03	1.319e-02
B to Z	3.551e-03	6.394e-03	1.261e-02
C to Z	3.905e-03	6.976e-03	1.392e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

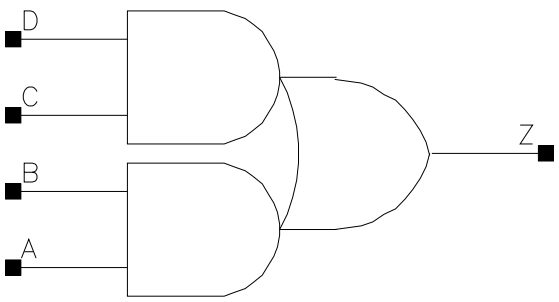
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	8.620e-07	7.133e-07	1.331e-06
B (output stable)	9.020e-07	6.692e-07	1.259e-06
C (output stable)	4.869e-07	6.976e-07	1.406e-06
A to Z	5.226e-07	1.384e-06	2.134e-06
B to Z	1.345e-07	4.983e-07	6.805e-07
C to Z	8.747e-07	1.300e-06	3.436e-06

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0010	0.0020
B	0.0007	0.0011	0.0019
C	0.0006	0.0010	0.0020
D	0.0007	0.0011	0.0019

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0311	0.0281	1.5139	0.7631
A to Z ↑	0.0223	0.0210	2.2310	1.1114
B to Z ↓	0.0289	0.0262	1.5069	0.7608
B to Z ↑	0.0238	0.0228	2.2305	1.1108

C to Z ↓	0.0293	0.0270	1.5078	0.7609
C to Z ↑	0.0191	0.0180	2.2233	1.1075
D to Z ↓	0.0280	0.0256	1.5045	0.7592
D to Z ↑	0.0207	0.0195	2.2219	1.1063
	X33_P0		**X33_P0**	
A to Z ↓	0.0264		0.3886	
A to Z ↑	0.0190		0.5625	
B to Z ↓	0.0250		0.3884	
B to Z ↑	0.0206		0.5621	
C to Z ↓	0.0253		0.3880	
C to Z ↑	0.0162		0.5605	
D to Z ↓	0.0240		0.3872	
D to Z ↑	0.0175		0.5601	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	8.209e-05	1.642e-09
X17_P0	1.558e-04	1.807e-09
X33_P0	2.948e-04	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	5.187e-05	7.390e-05	1.044e-04
B (output stable)	1.254e-04	1.614e-04	1.147e-04
C (output stable)	5.900e-05	9.710e-05	2.126e-04
D (output stable)	6.045e-05	1.025e-04	2.310e-04
A to Z	4.694e-03	8.220e-03	1.498e-02
B to Z	4.411e-03	7.857e-03	1.449e-02
C to Z	4.136e-03	7.336e-03	1.325e-02
D to Z	4.017e-03	7.110e-03	1.281e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

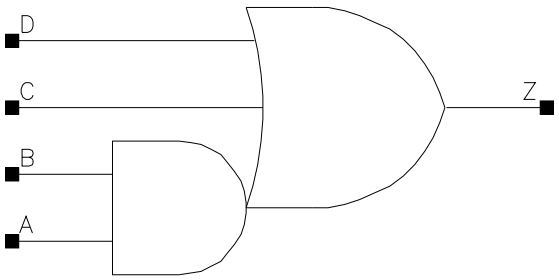
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	1.660e-07	2.138e-07	3.017e-07
B (output stable)	1.232e-07	1.741e-07	2.530e-07
C (output stable)	2.836e-07	4.005e-07	7.440e-07
D (output stable)	2.714e-07	3.799e-07	7.128e-07
A to Z	2.167e-07	2.683e-07	9.957e-07
B to Z	3.034e-07	2.123e-07	6.503e-07
C to Z	3.931e-07	4.348e-07	1.770e-06
D to Z	1.126e-07	1.710e-09	3.581e-07

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	0.952	1.1424
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0007	0.0010	0.0019
B	0.0007	0.0010	0.0020
C	0.0007	0.0010	0.0019
D	0.0007	0.0011	0.0019

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0367	0.0330	1.6249	0.8032
A to Z ↑	0.0186	0.0173	2.2481	1.1568
B to Z ↓	0.0353	0.0311	1.6201	0.7998
B to Z ↑	0.0200	0.0183	2.2484	1.1558
C to Z ↓	0.0364	0.0327	1.6187	0.8000
C to Z ↑	0.0178	0.0168	2.2355	1.1504

D to Z ↓	0.0370	0.0334	1.6193	0.8007
D to Z ↑	0.0174	0.0166	2.2349	1.1501
	X33_P0		**X33_P0**	
A to Z ↓	0.0338		0.4025	
A to Z ↑	0.0173		0.5613	
B to Z ↓	0.0307		0.3996	
B to Z ↑	0.0181		0.5610	
C to Z ↓	0.0339		0.4006	
C to Z ↑	0.0166		0.5585	
D to Z ↓	0.0338		0.4007	
D to Z ↑	0.0159		0.5579	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	7.192e-05	1.476e-09
X17_P0	1.392e-04	1.642e-09
X33_P0	2.776e-04	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	7.106e-05	1.323e-04	3.044e-04
B (output stable)	7.070e-05	1.275e-04	3.275e-04
C (output stable)	4.301e-05	7.965e-05	2.169e-04
D (output stable)	5.375e-05	1.001e-04	3.271e-04
A to Z	4.182e-03	7.294e-03	1.483e-02
B to Z	4.059e-03	7.029e-03	1.392e-02
C to Z	4.583e-03	7.974e-03	1.634e-02
D to Z	4.382e-03	7.649e-03	1.539e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

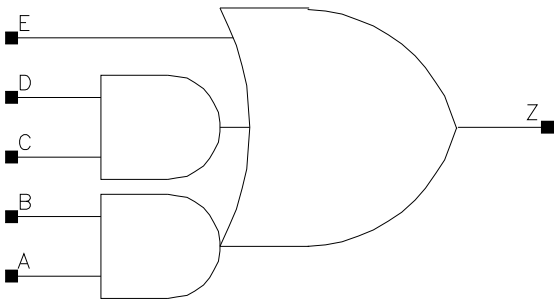
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	8.423e-06	9.341e-06	2.344e-05
B (output stable)	8.154e-06	8.462e-06	2.335e-05
C (output stable)	2.781e-07	4.219e-07	8.761e-07
D (output stable)	9.598e-07	1.161e-06	3.564e-06
A to Z	4.460e-07	5.484e-07	6.106e-07
B to Z	2.810e-08	1.297e-08	-3.226e-07
C to Z	1.066e-06	1.686e-06	2.804e-06
D to Z	9.967e-07	1.196e-06	2.574e-06

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.088	1.3056
X17_P0	1.200	1.224	1.4688
X33_P0	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0010	0.0020
B	0.0007	0.0010	0.0019
C	0.0008	0.0012	0.0020
D	0.0007	0.0010	0.0020
E	0.0007	0.0010	0.0019

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0427	0.0376	1.5533	0.7821
A to Z ↑	0.0237	0.0209	2.2076	1.1159

B to Z ↓	0.0412	0.0359	1.5473	0.7803
B to Z ↑	0.0257	0.0226	2.2064	1.1150
C to Z ↓	0.0379	0.0346	1.5479	0.7802
C to Z ↑	0.0198	0.0174	2.1913	1.1089
D to Z ↓	0.0354	0.0317	1.5401	0.7758
D to Z ↑	0.0213	0.0187	2.1902	1.1088
E to Z ↓	0.0382	0.0338	1.5398	0.7767
E to Z ↑	0.0187	0.0166	2.1754	1.1033
	X33_P0		**X33_P0**	
A to Z ↓	0.0369		0.4021	
A to Z ↑	0.0214		0.5642	
B to Z ↓	0.0348		0.4012	
B to Z ↑	0.0232		0.5637	
C to Z ↓	0.0334		0.4009	
C to Z ↑	0.0174		0.5600	
D to Z ↓	0.0310		0.3990	
D to Z ↑	0.0188		0.5596	
E to Z ↓	0.0332		0.3996	
E to Z ↑	0.0166		0.5571	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	8.509e-05	1.807e-09
X17_P0	1.609e-04	1.973e-09
X33_P0	2.976e-04	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	2.773e-05	4.553e-05	1.025e-04
B (output stable)	3.308e-05	4.687e-05	1.141e-04
C (output stable)	8.915e-05	1.267e-04	3.091e-04
D (output stable)	1.016e-04	1.479e-04	3.301e-04
E (output stable)	1.420e-04	1.899e-04	4.394e-04
A to Z	5.479e-03	9.161e-03	1.793e-02
B to Z	5.346e-03	8.878e-03	1.720e-02
C to Z	4.525e-03	7.743e-03	1.499e-02
D to Z	4.359e-03	7.415e-03	1.429e-02
E to Z	4.779e-03	8.052e-03	1.563e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	2.015e-07	2.612e-07	3.994e-07
B (output stable)	1.860e-07	2.534e-07	3.418e-07
C (output stable)	3.627e-06	1.521e-06	4.810e-06
D (output stable)	4.555e-06	2.018e-06	4.754e-06
E (output stable)	1.067e-06	1.466e-06	2.985e-06
A to Z	8.053e-07	8.540e-07	9.337e-07
B to Z	1.042e-06	8.113e-07	1.153e-06
C to Z	1.923e-07	4.243e-07	-7.345e-07
D to Z	8.367e-09	-1.913e-08	-3.534e-07

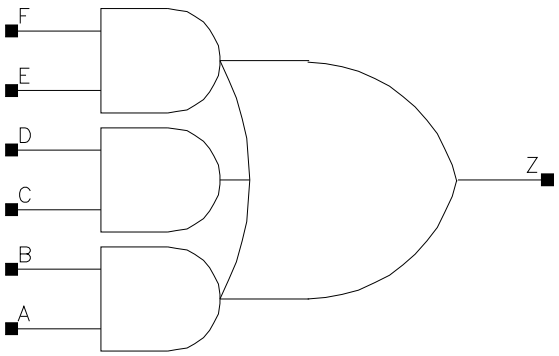
E to Z	5.272e-07	7.467e-07	1.871e-06

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.360	1.6320
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
A	0.0006	0.0007	0.0010	0.0020

B	0.0007	0.0008	0.0013	0.0019
C	0.0006	0.0007	0.0010	0.0020
D	0.0007	0.0008	0.0010	0.0019
E	0.0007	0.0008	0.0010	0.0021
F	0.0007	0.0008	0.0010	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0429	0.0411	2.8814	1.5620
A to Z ↑	0.0248	0.0244	4.2760	2.2610
B to Z ↓	0.0397	0.0382	2.8594	1.5519
B to Z ↑	0.0261	0.0260	4.2726	2.2592
C to Z ↓	0.0396	0.0383	2.8719	1.5578
C to Z ↑	0.0226	0.0222	4.2499	2.2475
D to Z ↓	0.0378	0.0366	2.8600	1.5519
D to Z ↑	0.0244	0.0241	4.2479	2.2463
E to Z ↓	0.0340	0.0337	2.8574	1.5511
E to Z ↑	0.0187	0.0185	4.2282	2.2376
F to Z ↓	0.0319	0.0317	2.8443	1.5451
F to Z ↑	0.0200	0.0200	4.2287	2.2358
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
A to Z ↓	0.0400	0.0384	0.7863	0.4010
A to Z ↑	0.0230	0.0230	1.1197	0.5661
B to Z ↓	0.0378	0.0365	0.7809	0.3999
B to Z ↑	0.0250	0.0248	1.1192	0.5657
C to Z ↓	0.0378	0.0363	0.7841	0.4007
C to Z ↑	0.0209	0.0213	1.1134	0.5631
D to Z ↓	0.0358	0.0346	0.7808	0.3996
D to Z ↑	0.0228	0.0230	1.1135	0.5628
E to Z ↓	0.0333	0.0335	0.7805	0.3994
E to Z ↑	0.0175	0.0182	1.1087	0.5613
F to Z ↓	0.0313	0.0313	0.7775	0.3978
F to Z ↑	0.0189	0.0199	1.1085	0.5609

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	6.933e-05	2.139e-09
X8_P0	1.035e-04	2.139e-09
X17_P0	1.741e-04	2.304e-09
X33_P0	3.183e-04	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	5.372e-05	6.266e-05	7.950e-05	1.440e-04
B (output stable)	1.037e-04	1.164e-04	1.224e-04	1.679e-04
C (output stable)	5.708e-05	6.845e-05	8.754e-05	1.943e-04
D (output stable)	6.082e-05	7.344e-05	9.208e-05	2.314e-04
E (output stable)	1.423e-04	1.770e-04	2.274e-04	3.904e-04
F (output stable)	1.424e-04	1.742e-04	2.326e-04	4.180e-04

A to Z	4.606e-03	6.340e-03	1.008e-02	1.911e-02
B to Z	4.293e-03	5.967e-03	9.555e-03	1.837e-02
C to Z	3.981e-03	5.583e-03	9.041e-03	1.720e-02
D to Z	3.836e-03	5.399e-03	8.752e-03	1.658e-02
E to Z	3.322e-03	4.828e-03	7.933e-03	1.552e-02
F to Z	3.183e-03	4.648e-03	7.661e-03	1.488e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

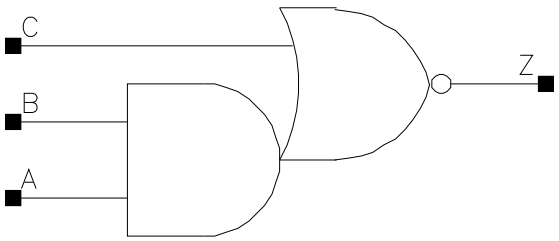
Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	2.477e-07	2.887e-07	3.316e-07	6.002e-07
B (output stable)	2.096e-07	2.597e-07	4.645e-07	5.017e-07
C (output stable)	6.281e-07	6.530e-07	8.677e-07	1.680e-06
D (output stable)	6.712e-07	6.742e-07	8.226e-07	1.609e-06
E (output stable)	7.627e-06	6.542e-06	4.981e-06	4.386e-06
F (output stable)	7.439e-06	6.187e-06	4.924e-06	4.270e-06
A to Z	1.078e-06	1.266e-06	1.628e-06	1.679e-06
B to Z	1.223e-06	1.519e-06	1.572e-06	2.193e-06
C to Z	3.426e-07	4.496e-07	5.890e-07	2.488e-07
D to Z	3.230e-07	3.573e-07	6.317e-07	3.036e-07
E to Z	1.845e-08	1.882e-07	3.907e-07	-7.612e-07
F to Z	-1.605e-07	-5.674e-08	-8.770e-08	-5.368e-07

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008
X44_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X33_P0	X44_P0
A	0.0008	0.0025	0.0051	0.0069
B	0.0008	0.0024	0.0049	0.0067
C	0.0009	0.0027	0.0054	0.0070

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0057	0.0058	2.5863	0.8789
A to Z ↑	0.0143	0.0146	4.4302	1.4898
B to Z ↓	0.0061	0.0062	2.6166	0.8925
B to Z ↑	0.0120	0.0117	4.3530	1.4891
C to Z ↓	0.0060	0.0062	1.5950	0.5478
C to Z ↑	0.0134	0.0133	4.0385	1.3719
	X33_P0	**X44_P0**	**X33_P0**	**X44_P0**
A to Z ↓	0.0061	0.0060	0.4487	0.3404

A to Z ↑	0.0146	0.0147	0.7472	0.5683
B to Z ↓	0.0063	0.0064	0.4556	0.3458
B to Z ↑	0.0118	0.0118	0.7448	0.5645
C to Z ↓	0.0077	0.0078	0.3247	0.2517
C to Z ↑	0.0136	0.0134	0.6869	0.5215

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P0	5.622e-05	1.145e-09
X17_P0	1.531e-04	2.139e-09
X33_P0	2.856e-04	3.629e-09
X44_P0	3.829e-04	4.623e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	1.024e-04	3.050e-04	6.894e-04	8.629e-04
B (output stable)	1.066e-04	3.501e-04	7.756e-04	9.712e-04
C (output stable)	1.301e-04	3.953e-04	8.722e-04	1.117e-03
A to Z	1.914e-03	5.867e-03	1.180e-02	1.560e-02
B to Z	1.726e-03	4.977e-03	1.008e-02	1.332e-02
C to Z	2.465e-03	7.272e-03	1.461e-02	1.914e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

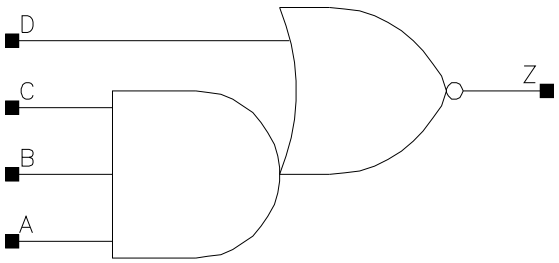
Pin Cycle (vdds)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	6.551e-07	1.528e-06	3.258e-06	3.736e-06
B (output stable)	6.366e-07	1.456e-06	3.250e-06	3.641e-06
C (output stable)	6.680e-07	1.521e-06	3.410e-06	3.933e-06
A to Z	7.532e-07	5.850e-07	2.971e-06	4.062e-06
B to Z	1.093e-06	1.940e-06	5.459e-06	3.810e-06
C to Z	2.396e-06	5.251e-06	7.737e-06	9.990e-06

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X29_P0	1.200	3.536	4.2432
X38_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X29_P0	X38_P0
A	0.0009	0.0052	0.0068
B	0.0008	0.0051	0.0066
C	0.0008	0.0049	0.0065
D	0.0009	0.0053	0.0067

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X29_P0	X5_P0	X29_P0
A to Z ↓	0.0091	0.0097	3.5871	0.6268
A to Z ↑	0.0178	0.0179	4.4328	0.7389
B to Z ↓	0.0100	0.0101	3.6055	0.6310
B to Z ↑	0.0160	0.0159	4.4350	0.7452
C to Z ↓	0.0100	0.0100	3.6234	0.6348
C to Z ↑	0.0138	0.0134	4.3660	0.7509
D to Z ↓	0.0079	0.0097	1.6295	0.3266

D to Z ↑	0.0157	0.0158	3.7754	0.6380
	X38_P0		**X38_P0**	
A to Z ↓	0.0094		0.4876	
A to Z ↑	0.0174		0.5579	
B to Z ↓	0.0099		0.4910	
B to Z ↑	0.0153		0.5642	
C to Z ↓	0.0097		0.4941	
C to Z ↑	0.0129		0.5709	
D to Z ↓	0.0104		0.2721	
D to Z ↑	0.0154		0.4828	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P0	5.570e-05	1.310e-09
X29_P0	2.790e-04	4.789e-09
X38_P0	3.556e-04	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P0	X29_P0	X38_P0
A (output stable)	6.311e-05	5.071e-04	6.554e-04
B (output stable)	6.927e-05	5.388e-04	7.001e-04
C (output stable)	8.746e-05	7.626e-04	9.793e-04
D (output stable)	1.647e-04	1.191e-03	1.582e-03
A to Z	2.460e-03	1.518e-02	1.924e-02
B to Z	2.212e-03	1.310e-02	1.662e-02
C to Z	2.003e-03	1.134e-02	1.428e-02
D to Z	3.030e-03	1.806e-02	2.309e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

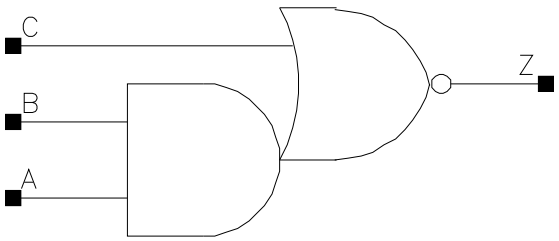
Pin Cycle (vdds)	X5_P0	X29_P0	X38_P0
A (output stable)	5.433e-07	5.173e-06	6.494e-06
B (output stable)	4.715e-07	4.982e-06	6.285e-06
C (output stable)	5.065e-07	4.922e-06	6.256e-06
D (output stable)	6.856e-07	4.689e-06	6.144e-06
A to Z	1.013e-06	3.805e-06	3.941e-06
B to Z	-1.600e-08	1.025e-06	2.770e-06
C to Z	-9.900e-08	-3.820e-07	-3.826e-06
D to Z	1.310e-06	7.889e-06	7.700e-06

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X11_P0	1.200	1.088	1.3056
X16_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X11_P0	X16_P0	X23_P0
A	0.0009	0.0018	0.0027	0.0036
B	0.0009	0.0018	0.0026	0.0035
C	0.0009	0.0017	0.0025	0.0035
	X46_P0			
A	0.0070			
B	0.0068			
C	0.0069			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X11_P0	X6_P0	X11_P0
A to Z ↓	0.0072	0.0079	2.4926	1.2741
A to Z ↑	0.0143	0.0151	4.4218	2.1674
B to Z ↓	0.0081	0.0084	2.5204	1.2894

B to Z ↑	0.0124	0.0126	4.3596	2.1744
C to Z ↓	0.0033	0.0040	1.6459	0.9599
C to Z ↑	0.0119	0.0116	4.0582	2.0061
	X16_P0	**X23_P0**	**X16_P0**	**X23_P0**
A to Z ↓	0.0074	0.0077	0.8783	0.6623
A to Z ↑	0.0141	0.0145	1.4594	1.1071
B to Z ↓	0.0083	0.0083	0.8903	0.6705
B to Z ↑	0.0117	0.0120	1.4578	1.1108
C to Z ↓	0.0041	0.0032	0.6652	0.4237
C to Z ↑	0.0110	0.0117	1.3507	1.0242
	X46_P0		**X46_P0**	
A to Z ↓	0.0074		0.3404	
A to Z ↑	0.0140		0.5773	
B to Z ↓	0.0081		0.3451	
B to Z ↑	0.0114		0.5753	
C to Z ↓	0.0035		0.2166	
C to Z ↑	0.0118		0.5325	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P0	5.553e-05	1.145e-09
X11_P0	1.098e-04	1.807e-09
X16_P0	1.495e-04	2.139e-09
X23_P0	2.105e-04	2.801e-09
X46_P0	4.019e-04	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	3.941e-05	1.097e-04	1.432e-04	2.056e-04
B (output stable)	4.462e-05	1.556e-04	1.752e-04	2.637e-04
C (output stable)	3.270e-04	7.934e-04	9.318e-04	1.339e-03
A to Z	2.368e-03	5.066e-03	7.038e-03	9.589e-03
B to Z	2.150e-03	4.436e-03	6.117e-03	8.334e-03
C to Z	1.780e-03	3.562e-03	5.022e-03	7.070e-03
	X46_P0			
A (output stable)	3.736e-04			
B (output stable)	4.593e-04			
C (output stable)	2.236e-03			
A to Z	1.803e-02			
B to Z	1.567e-02			
C to Z	1.357e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	2.422e-07	4.410e-07	3.617e-07	5.076e-07
B (output stable)	2.207e-07	4.321e-07	3.226e-07	4.458e-07
C (output stable)	1.022e-06	2.443e-06	2.295e-06	3.429e-06
A to Z	2.053e-06	4.207e-06	4.617e-06	5.524e-06
B to Z	6.660e-07	1.883e-06	1.348e-06	5.993e-06
C to Z	7.217e-07	1.866e-07	-7.867e-08	-1.427e-07

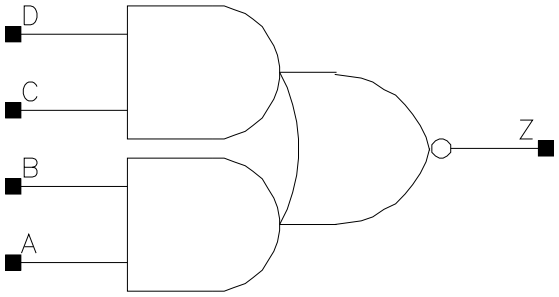
	X46_P0			
A (output stable)	8.242e-07			
B (output stable)	7.761e-07			
C (output stable)	5.600e-06			
A to Z	1.150e-05			
B to Z	1.234e-05			
C to Z	-9.700e-07			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P0	X10_P0	X16_P0	X21_P0
A	0.0007	0.0019	0.0027	0.0035
B	0.0007	0.0017	0.0026	0.0035
C	0.0007	0.0018	0.0026	0.0035
D	0.0007	0.0016	0.0025	0.0034
	X42_P0			
A	0.0071			
B	0.0069			
C	0.0069			
D	0.0068			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X10_P0**	**X4_P0**	**X10_P0**
A to Z ↓	0.0085	0.0086	3.0658	1.2202
A to Z ↑	0.0186	0.0159	5.9578	1.9993
B to Z ↓	0.0095	0.0097	3.1040	1.2366
B to Z ↑	0.0166	0.0144	5.9348	2.0516
C to Z ↓	0.0058	0.0056	3.1474	1.2294
C to Z ↑	0.0162	0.0142	5.9481	2.0087
D to Z ↓	0.0063	0.0062	3.1951	1.2497
D to Z ↑	0.0140	0.0124	5.9242	2.0397
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0094	0.0093	0.8810	0.6644
A to Z ↑	0.0166	0.0165	1.3504	1.0467
B to Z ↓	0.0105	0.0101	0.8915	0.6722
B to Z ↑	0.0143	0.0142	1.3499	1.0482
C to Z ↓	0.0060	0.0062	0.8817	0.6659
C to Z ↑	0.0146	0.0150	1.3493	1.0444
D to Z ↓	0.0068	0.0065	0.8952	0.6757
D to Z ↑	0.0121	0.0124	1.3504	1.0454
	X42_P0		**X42_P0**	
A to Z ↓	0.0100		0.3460	
A to Z ↑	0.0169		0.5267	
B to Z ↓	0.0107		0.3502	
B to Z ↑	0.0143		0.5241	
C to Z ↓	0.0067		0.3419	
C to Z ↑	0.0152		0.5266	
D to Z ↓	0.0071		0.3472	
D to Z ↑	0.0126		0.5243	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	4.915e-05	1.310e-09
X10_P0	1.318e-04	2.139e-09
X16_P0	1.794e-04	2.635e-09
X21_P0	2.415e-04	3.464e-09
X42_P0	4.670e-04	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	4.244e-05	1.008e-04	1.955e-04	2.639e-04
B (output stable)	4.598e-05	1.149e-04	2.747e-04	3.878e-04
C (output stable)	9.395e-05	2.157e-04	3.755e-04	4.722e-04
D (output stable)	1.013e-04	2.363e-04	4.559e-04	5.908e-04
A to Z	2.287e-03	5.747e-03	8.839e-03	1.144e-02
B to Z	2.076e-03	5.235e-03	7.836e-03	1.015e-02
C to Z	1.610e-03	4.198e-03	6.315e-03	8.442e-03
D to Z	1.436e-03	3.745e-03	5.428e-03	7.256e-03
	X42_P0			
A (output stable)	5.077e-04			
B (output stable)	6.975e-04			
C (output stable)	9.202e-04			
D (output stable)	1.122e-03			

A to Z	2.270e-02			
B to Z	2.014e-02			
C to Z	1.663e-02			
D to Z	1.439e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

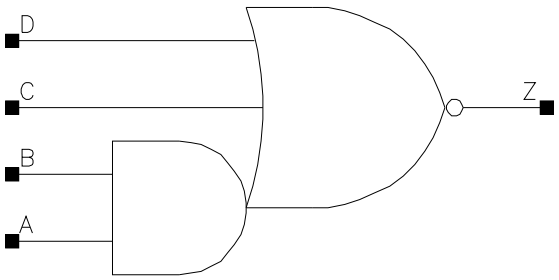
Pin Cycle (vdds)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	2.292e-07	2.958e-07	4.165e-07	4.436e-07
B (output stable)	2.244e-07	3.277e-07	3.529e-07	4.507e-07
C (output stable)	4.947e-07	9.020e-07	1.170e-06	1.372e-06
D (output stable)	4.914e-07	7.666e-07	1.130e-06	1.443e-06
A to Z	1.520e-06	3.807e-06	4.771e-06	6.570e-06
B to Z	9.620e-07	2.258e-06	3.106e-06	3.888e-06
C to Z	4.447e-07	7.933e-07	1.200e-06	1.706e-06
D to Z	5.662e-07	1.650e-06	2.383e-06	1.957e-06
	X42_P0			
A (output stable)	8.911e-07			
B (output stable)	7.554e-07			
C (output stable)	2.456e-06			
D (output stable)	2.553e-06			
A to Z	8.887e-06			
B to Z	6.577e-06			
C to Z	2.508e-06			
D to Z	1.881e-06			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X35_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P0	X35_P0
A	0.0008	0.0066
B	0.0009	0.0063
C	0.0009	0.0063
D	0.0009	0.0060

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X35_P0	X5_P0	X35_P0
A to Z ↓	0.0069	0.0073	2.6121	0.3875
A to Z ↑	0.0189	0.0178	6.5267	0.8428
B to Z ↓	0.0074	0.0078	2.6511	0.3943
B to Z ↑	0.0161	0.0147	6.4718	0.8414
C to Z ↓	0.0078	0.0114	1.6973	0.3239
C to Z ↑	0.0191	0.0187	6.1576	0.7971
D to Z ↓	0.0073	0.0103	1.7124	0.3237

D to Z ↑	0.0193	0.0181	6.1696	0.8002

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P0	4.431e-05	1.310e-09
X35_P0	2.787e-04	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P0	X35_P0
A (output stable)	1.270e-04	1.034e-03
B (output stable)	1.259e-04	1.078e-03
C (output stable)	7.553e-05	8.164e-04
D (output stable)	9.677e-05	1.044e-03
A to Z	2.099e-03	1.537e-02
B to Z	1.871e-03	1.320e-02
C to Z	2.981e-03	2.254e-02
D to Z	2.600e-03	1.873e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

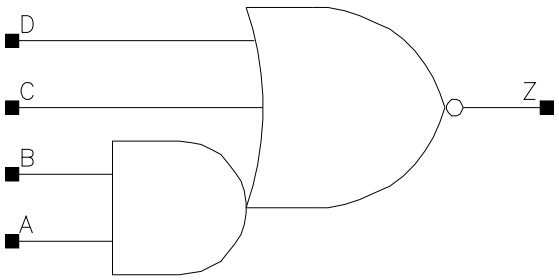
Pin Cycle (vdds)	X5_P0	X35_P0
A (output stable)	8.950e-06	6.022e-05
B (output stable)	8.420e-06	6.056e-05
C (output stable)	3.836e-07	2.278e-06
D (output stable)	1.117e-06	1.035e-05
A to Z	4.376e-07	3.768e-06
B to Z	-1.436e-07	-2.537e-06
C to Z	1.411e-06	6.210e-06
D to Z	1.693e-06	2.627e-06

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X17_P0	1.200	2.448	2.9376
X34_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P0	X17_P0	X34_P0
A	0.0009	0.0035	0.0071
B	0.0009	0.0034	0.0069
C	0.0008	0.0031	0.0061
D	0.0008	0.0030	0.0057

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X17_P0	X4_P0	X17_P0
A to Z ↓	0.0088	0.0096	2.8211	0.7470
A to Z ↑	0.0189	0.0199	6.5740	1.6277
B to Z ↓	0.0099	0.0104	2.8581	0.7564
B to Z ↑	0.0167	0.0169	6.4975	1.6298
C to Z ↓	0.0087	0.0085	2.6450	0.6423
C to Z ↑	0.0145	0.0150	6.1904	1.5428

D to Z ↓	0.0068	0.0059	2.6958	0.6467
D to Z ↑	0.0142	0.0133	6.2077	1.5462
	X34_P0		**X34_P0**	
A to Z ↓	0.0094		0.3839	
A to Z ↑	0.0195		0.8319	
B to Z ↓	0.0105		0.3887	
B to Z ↑	0.0166		0.8281	
C to Z ↓	0.0088		0.3428	
C to Z ↑	0.0146		0.7866	
D to Z ↓	0.0063		0.3463	
D to Z ↑	0.0130		0.7885	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	3.892e-05	1.310e-09
X17_P0	1.496e-04	3.464e-09
X34_P0	2.848e-04	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X17_P0	X34_P0
A (output stable)	3.601e-05	1.774e-04	3.521e-04
B (output stable)	3.723e-05	2.091e-04	3.930e-04
C (output stable)	9.815e-05	5.236e-04	1.006e-03
D (output stable)	1.775e-04	1.118e-03	2.121e-03
A to Z	2.720e-03	1.154e-02	2.238e-02
B to Z	2.495e-03	1.022e-02	1.989e-02
C to Z	1.892e-03	7.987e-03	1.525e-02
D to Z	1.586e-03	6.191e-03	1.182e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

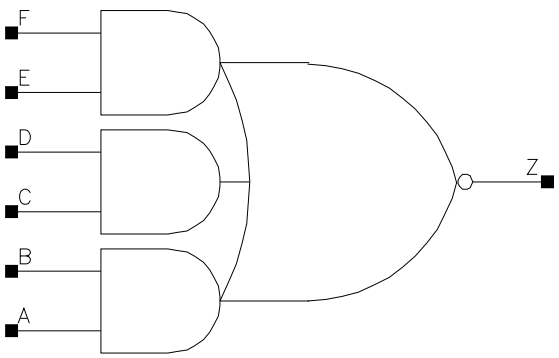
Pin Cycle (vdds)	X4_P0	X17_P0	X34_P0
A (output stable)	2.703e-07	5.649e-07	1.019e-06
B (output stable)	2.515e-07	5.306e-07	9.303e-07
C (output stable)	8.883e-07	3.581e-06	6.625e-06
D (output stable)	7.262e-07	5.455e-06	8.421e-06
A to Z	1.869e-06	5.071e-06	9.710e-06
B to Z	1.248e-06	5.148e-06	1.126e-05
C to Z	4.497e-07	2.315e-06	3.736e-06
D to Z	-5.647e-08	6.997e-07	2.614e-06

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X8_P0	1.200	2.176	2.6112
X13_P0	1.200	2.720	3.2640
X17_P0	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P0	X8_P0	X13_P0	X17_P0
A	0.0009	0.0017	0.0026	0.0035

B	0.0009	0.0017	0.0025	0.0033
C	0.0008	0.0017	0.0025	0.0033
D	0.0008	0.0016	0.0024	0.0032
E	0.0010	0.0017	0.0025	0.0032
F	0.0009	0.0016	0.0023	0.0031

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0110	0.0135	2.4988	1.4441
A to Z ↑	0.0275	0.0273	6.2897	2.9330
B to Z ↓	0.0125	0.0147	2.5304	1.4568
B to Z ↑	0.0252	0.0246	6.2798	2.9397
C to Z ↓	0.0098	0.0119	2.4822	1.4590
C to Z ↑	0.0245	0.0248	6.3227	2.9456
D to Z ↓	0.0109	0.0132	2.5200	1.4765
D to Z ↑	0.0221	0.0221	6.2848	2.9434
E to Z ↓	0.0068	0.0085	2.4609	1.4633
E to Z ↑	0.0204	0.0203	6.2431	2.9199
F to Z ↓	0.0073	0.0093	2.5096	1.4874
F to Z ↑	0.0180	0.0175	6.2872	2.9232
	X13_P0	X17_P0	X13_P0	X17_P0
A to Z ↓	0.0128	0.0130	0.9821	0.7501
A to Z ↑	0.0252	0.0255	1.9379	1.4869
B to Z ↓	0.0144	0.0143	0.9910	0.7565
B to Z ↑	0.0229	0.0228	1.9447	1.4870
C to Z ↓	0.0114	0.0114	0.9876	0.7435
C to Z ↑	0.0228	0.0232	1.9486	1.4967
D to Z ↓	0.0128	0.0124	0.9989	0.7518
D to Z ↑	0.0204	0.0205	1.9510	1.4938
E to Z ↓	0.0082	0.0081	0.9858	0.7459
E to Z ↑	0.0191	0.0192	1.9370	1.4809
F to Z ↓	0.0089	0.0085	1.0010	0.7573
F to Z ↑	0.0164	0.0164	1.9398	1.4874

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	7.443e-05	1.807e-09
X8_P0	1.450e-04	3.132e-09
X13_P0	2.006e-04	3.795e-09
X17_P0	2.681e-04	4.954e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	6.584e-05	1.557e-04	2.165e-04	2.956e-04
B (output stable)	6.790e-05	2.083e-04	2.547e-04	3.781e-04
C (output stable)	1.012e-04	2.184e-04	2.878e-04	4.001e-04
D (output stable)	1.049e-04	2.866e-04	3.358e-04	4.834e-04
E (output stable)	1.936e-04	4.608e-04	6.226e-04	8.373e-04
F (output stable)	2.155e-04	5.197e-04	6.692e-04	9.199e-04

A to Z	4.151e-03	8.671e-03	1.205e-02	1.605e-02
B to Z	3.870e-03	7.954e-03	1.114e-02	1.469e-02
C to Z	3.223e-03	6.941e-03	9.474e-03	1.259e-02
D to Z	2.979e-03	6.303e-03	8.647e-03	1.138e-02
E to Z	2.358e-03	5.108e-03	7.042e-03	9.291e-03
F to Z	2.138e-03	4.502e-03	6.224e-03	8.158e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

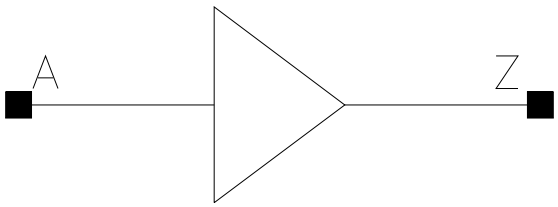
Pin Cycle (vdds)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	3.822e-07	6.832e-07	6.933e-07	8.901e-07
B (output stable)	3.793e-07	6.251e-07	6.248e-07	7.746e-07
C (output stable)	1.060e-06	2.091e-06	2.350e-06	3.267e-06
D (output stable)	1.046e-06	2.047e-06	2.360e-06	3.235e-06
E (output stable)	5.056e-06	1.273e-05	1.126e-05	1.557e-05
F (output stable)	6.322e-06	1.295e-05	1.135e-05	1.539e-05
A to Z	2.784e-06	4.469e-06	4.923e-06	6.594e-06
B to Z	2.818e-06	4.853e-06	5.112e-06	7.031e-06
C to Z	9.461e-07	1.440e-06	1.403e-06	2.377e-06
D to Z	6.563e-07	1.201e-06	1.277e-06	1.947e-06
E to Z	8.384e-08	-8.319e-07	-5.417e-07	-1.028e-06
F to Z	6.682e-08	-1.110e-06	-8.814e-07	-1.018e-06

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X6_P0	1.200	0.408	0.4896
X8_P0	1.200	0.408	0.4896
X13_P0	1.200	0.544	0.6528
X16_P0	1.200	0.544	0.6528
X21_P0	1.200	0.680	0.8160
X25_P0	1.200	0.680	0.8160
X29_P0	1.200	0.952	1.1424
X33_P0	1.200	0.952	1.1424
X42_P0	1.200	1.088	1.3056
X50_P0	1.200	1.224	1.4688
X58_P0	1.200	1.496	1.7952
X67_P0	1.200	1.632	1.9584
X75_P0	1.200	1.768	2.1216
X84_P0	1.200	1.904	2.2848
X100_P0	1.200	2.312	2.7744
X134_P0	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0008	0.0008	0.0008	0.0008
	X16_P0	X21_P0	X25_P0	X29_P0
A	0.0008	0.0011	0.0011	0.0015
	X33_P0	X42_P0	X50_P0	X58_P0
A	0.0015	0.0017	0.0020	0.0030

	X67_P0	X75_P0	X84_P0	X100_P0
A	0.0030	0.0030	0.0030	0.0040
	X134_P0			
A	0.0051			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0181	0.0182	2.6947	2.0078
A to Z ↑	0.0130	0.0129	4.1888	3.1221
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0189	0.0213	1.5099	0.9616
A to Z ↑	0.0136	0.0156	2.2570	1.4605
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0229	0.0196	0.7711	0.5926
A to Z ↑	0.0167	0.0144	1.1293	0.8818
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0206	0.0195	0.5119	0.4305
A to Z ↑	0.0152	0.0138	0.7450	0.6306
	X33_P0	**X42_P0**	**X33_P0**	**X42_P0**
A to Z ↓	0.0204	0.0200	0.3829	0.3115
A to Z ↑	0.0145	0.0148	0.5572	0.4488
	X50_P0	**X58_P0**	**X50_P0**	**X58_P0**
A to Z ↓	0.0197	0.0184	0.2585	0.2231
A to Z ↑	0.0144	0.0135	0.3724	0.3206
	X67_P0	**X75_P0**	**X67_P0**	**X75_P0**
A to Z ↓	0.0193	0.0204	0.1957	0.1763
A to Z ↑	0.0142	0.0151	0.2808	0.2512
	X84_P0	**X100_P0**	**X84_P0**	**X100_P0**
A to Z ↓	0.0211	0.0200	0.1594	0.1340
A to Z ↑	0.0158	0.0149	0.2267	0.1902
	X134_P0		**X134_P0**	
A to Z ↓	0.0211		0.1040	
A to Z ↑	0.0161		0.1452	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	5.093e-05	9.792e-10
X6_P0	6.111e-05	9.792e-10
X8_P0	7.214e-05	9.792e-10
X13_P0	9.712e-05	1.145e-09
X16_P0	1.176e-04	1.145e-09
X21_P0	1.610e-04	1.310e-09
X25_P0	1.733e-04	1.310e-09
X29_P0	2.135e-04	1.642e-09
X33_P0	2.189e-04	1.642e-09
X42_P0	2.711e-04	1.807e-09
X50_P0	3.239e-04	1.973e-09
X58_P0	3.993e-04	2.304e-09
X67_P0	4.371e-04	2.470e-09
X75_P0	4.748e-04	2.635e-09

X84_P0	5.126e-04	2.801e-09
X100_P0	6.258e-04	3.298e-09
X134_P0	8.146e-04	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	2.501e-03	2.792e-03	3.310e-03	4.524e-03
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	5.554e-03	7.334e-03	8.349e-03	9.592e-03
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	1.057e-02	1.323e-02	1.559e-02	1.890e-02
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	2.109e-02	2.372e-02	2.610e-02	3.125e-02
	X134_P0			
A to Z	4.353e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

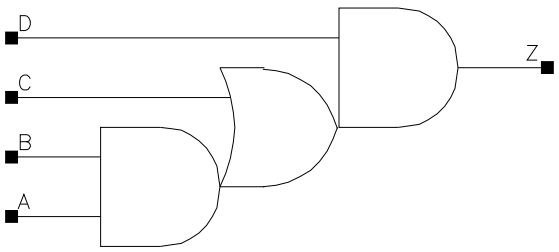
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	1.456e-08	1.574e-06	-3.942e-07	1.166e-06
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	7.887e-07	3.642e-06	-7.854e-07	-4.887e-07
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	3.736e-06	5.216e-06	5.600e-06	8.805e-06
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	-9.800e-07	7.389e-06	5.793e-06	1.058e-05
	X134_P0			
A to Z	8.246e-06			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.632	1.9584
X25_P0	1.200	1.768	2.1216
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0010	0.0021	0.0021	0.0020
B	0.0010	0.0019	0.0019	0.0019
C	0.0011	0.0023	0.0023	0.0023
D	0.0015	0.0020	0.0020	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0238	0.0226	1.5429	0.7641
A to Z ↑	0.0214	0.0203	2.2866	1.1154
B to Z ↓	0.0220	0.0207	1.5379	0.7628
B to Z ↑	0.0220	0.0206	2.2853	1.1155
C to Z ↓	0.0214	0.0201	1.5343	0.7609
C to Z ↑	0.0160	0.0147	2.2664	1.1056

D to Z ↓	0.0205	0.0184	1.5218	0.7552
D to Z ↑	0.0180	0.0158	2.2727	1.1078
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0248	0.0262	0.5185	0.3896
A to Z ↑	0.0223	0.0236	0.7555	0.5672
B to Z ↓	0.0230	0.0248	0.5176	0.3894
B to Z ↑	0.0228	0.0244	0.7552	0.5658
C to Z ↓	0.0224	0.0242	0.5158	0.3879
C to Z ↑	0.0166	0.0179	0.7480	0.5604
D to Z ↓	0.0198	0.0208	0.5109	0.3831
D to Z ↑	0.0174	0.0185	0.7496	0.5622

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	9.902e-05	1.642e-09
X17_P0	1.871e-04	2.470e-09
X25_P0	2.234e-04	2.635e-09
X33_P0	2.598e-04	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	7.626e-05	1.608e-04	1.613e-04	1.435e-04
B (output stable)	8.821e-05	1.926e-04	1.941e-04	1.648e-04
C (output stable)	2.703e-04	4.355e-04	4.378e-04	4.208e-04
D (output stable)	1.585e-04	2.439e-04	2.453e-04	2.416e-04
A to Z	5.138e-03	9.571e-03	1.228e-02	1.477e-02
B to Z	4.872e-03	8.911e-03	1.157e-02	1.420e-02
C to Z	4.352e-03	7.820e-03	1.034e-02	1.267e-02
D to Z	5.255e-03	9.449e-03	1.180e-02	1.389e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

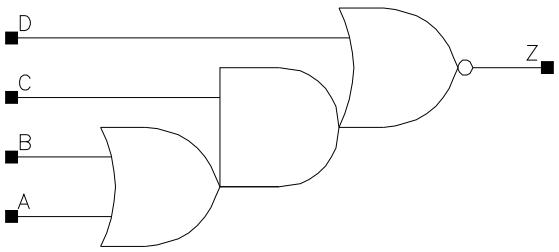
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	1.157e-07	1.217e-07	1.243e-07	1.190e-07
B (output stable)	1.418e-07	1.671e-07	1.647e-07	1.624e-07
C (output stable)	3.195e-07	5.380e-07	5.185e-07	4.992e-07
D (output stable)	9.317e-08	5.336e-08	5.754e-08	6.850e-08
A to Z	2.680e-07	3.060e-07	1.710e-07	-1.000e-07
B to Z	5.390e-07	4.660e-07	4.740e-07	4.270e-07
C to Z	4.556e-07	1.721e-06	4.220e-07	4.002e-07
D to Z	9.248e-07	-4.386e-08	-2.623e-08	2.937e-07

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.952	1.1424
X11_P0	1.200	1.496	1.7952
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X16_P0	X21_P0
A	0.0009	0.0017	0.0027	0.0036
B	0.0009	0.0017	0.0027	0.0034
C	0.0009	0.0017	0.0026	0.0036
D	0.0012	0.0018	0.0026	0.0035

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0091	0.0086	2.4709	1.3023
A to Z ↑	0.0228	0.0213	6.4582	3.3782
B to Z ↓	0.0086	0.0082	2.4057	1.2768
B to Z ↑	0.0223	0.0212	6.4689	3.3842
C to Z ↓	0.0086	0.0082	2.3047	1.2154
C to Z ↑	0.0144	0.0132	4.3491	2.2407

D to Z ↓	0.0039	0.0028	1.6039	0.8102
D to Z ↑	0.0145	0.0130	4.6546	2.4039
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0086	0.0089	0.8727	0.6756
A to Z ↑	0.0197	0.0209	2.1602	1.6761
B to Z ↓	0.0079	0.0082	0.8796	0.6778
B to Z ↑	0.0199	0.0206	2.1643	1.6793
C to Z ↓	0.0083	0.0085	0.8317	0.6396
C to Z ↑	0.0126	0.0128	1.4797	1.1122
D to Z ↓	0.0030	0.0031	0.5622	0.4285
D to Z ↑	0.0122	0.0122	1.5728	1.1933

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P0	6.226e-05	1.642e-09
X11_P0	1.155e-04	2.304e-09
X16_P0	1.573e-04	2.635e-09
X21_P0	2.079e-04	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	4.292e-05	8.043e-05	1.066e-04	1.723e-04
B (output stable)	5.172e-05	9.396e-05	1.284e-04	2.075e-04
C (output stable)	1.087e-04	2.197e-04	3.035e-04	4.241e-04
D (output stable)	4.273e-04	8.904e-04	1.272e-03	1.784e-03
A to Z	3.375e-03	6.007e-03	8.482e-03	1.180e-02
B to Z	2.834e-03	5.096e-03	7.403e-03	9.958e-03
C to Z	2.610e-03	4.624e-03	6.669e-03	9.107e-03
D to Z	2.007e-03	3.632e-03	5.130e-03	6.803e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

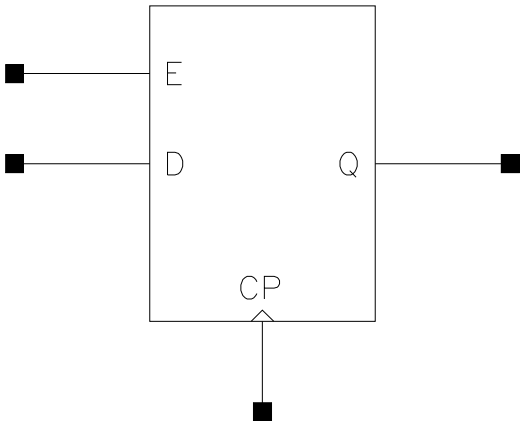
Pin Cycle (vdds)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	3.431e-07	3.455e-07	4.062e-07	8.609e-07
B (output stable)	7.521e-07	1.122e-06	1.368e-06	2.141e-06
C (output stable)	4.073e-07	6.435e-07	8.700e-07	1.179e-06
D (output stable)	1.414e-06	2.525e-06	3.316e-06	5.000e-06
A to Z	1.803e-06	4.231e-06	2.220e-06	3.113e-06
B to Z	1.528e-06	7.370e-07	4.449e-06	1.454e-06
C to Z	1.538e-06	2.573e-06	4.441e-06	3.679e-06
D to Z	5.926e-07	1.914e-07	-5.640e-08	-1.196e-06

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.128	3.7536
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0011	0.0011	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0270	0.0311	1.5225	0.7838
CP to Q ↑	0.0338	0.0364	2.2985	1.1517
	X33_P0		**X33_P0**	
CP to Q ↓	0.0474		0.3884	
CP to Q ↑	0.0578		0.5717	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0364	0.0364	0.0364
CP ↑	min_pulse_width to CP	0.0205	0.0253	0.0193
D ↓	hold_rising to CP	-0.0068	-0.0068	-0.0068
D ↑	hold_rising to CP	0.0027	0.0027	0.0027
D ↓	setup_rising to CP	0.0366	0.0366	0.0366
D ↑	setup_rising to CP	0.0217	0.0217	0.0217
E ↓	hold_rising to CP	-0.0042	-0.0042	-0.0042
E ↑	hold_rising to CP	0.0058	0.0058	0.0058
E ↓	setup_rising to CP	0.0411	0.0411	0.0411
E ↑	setup_rising to CP	0.0368	0.0368	0.0368

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	2.789e-04	4.126e-09
X17_P0	3.191e-04	4.292e-09
X33_P0	4.512e-04	4.954e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

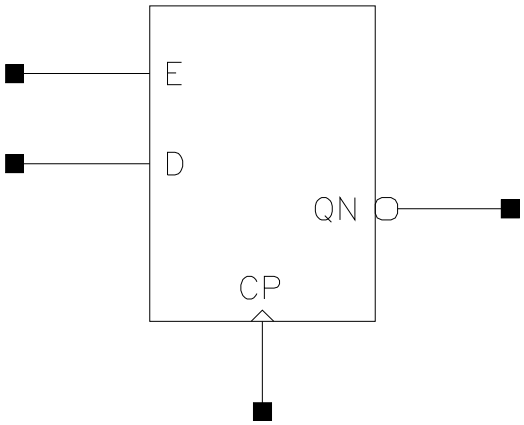
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.369e-03	5.370e-03	5.376e-03
Clock 100Mhz Data 25Mhz	1.143e-02	1.281e-02	1.623e-02
Clock 100Mhz Data 50Mhz	1.749e-02	2.026e-02	2.709e-02
Clock = 0 Data 100Mhz	6.819e-03	6.818e-03	6.818e-03
Clock = 1 Data 100Mhz	1.983e-03	1.983e-03	1.983e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.264	3.9168
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0008	0.0011	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0463	0.0441	1.5702	0.7515
CP to QN ↑	0.0369	0.0377	2.3335	1.1192
	X33_P0		**X33_P0**	
CP to QN ↓	0.0473		0.3894	
CP to QN ↑	0.0416		0.5740	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0364	0.0364	0.0364
CP ↑	min_pulse_width to CP	0.0193	0.0205	0.0242
D ↓	hold_rising to CP	-0.0068	-0.0068	-0.0068
D ↑	hold_rising to CP	0.0027	0.0027	0.0027
D ↓	setup_rising to CP	0.0366	0.0366	0.0366
D ↑	setup_rising to CP	0.0217	0.0217	0.0217
E ↓	hold_rising to CP	-0.0042	-0.0042	-0.0042
E ↑	hold_rising to CP	0.0058	0.0058	0.0058
E ↓	setup_rising to CP	0.0411	0.0411	0.0411
E ↑	setup_rising to CP	0.0368	0.0368	0.0368

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	2.782e-04	4.126e-09
X17_P0	3.437e-04	4.457e-09
X33_P0	4.410e-04	4.954e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

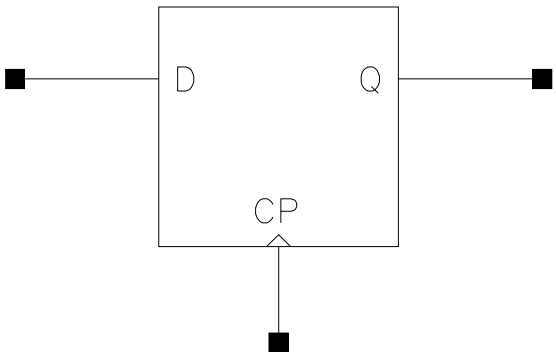
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.370e-03	5.370e-03	5.369e-03
Clock 100Mhz Data 25Mhz	1.144e-02	1.307e-02	1.619e-02
Clock 100Mhz Data 50Mhz	1.750e-02	2.077e-02	2.702e-02
Clock = 0 Data 100Mhz	6.819e-03	6.818e-03	6.816e-03
Clock = 1 Data 100Mhz	1.983e-03	1.983e-03	1.983e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.176	2.6112
X17_P0	1.200	2.448	2.9376
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0281	0.0314	1.5156	0.7774
CP to Q ↑	0.0338	0.0380	2.2226	1.1272
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to Q ↓	0.0403	0.0415	0.4572	0.4158
CP to Q ↑	0.0433	0.0444	0.6312	0.5770

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0365	0.0365	0.0365	0.0365
CP ↑	min_pulse_width to CP	0.0205	0.0242	0.0338	0.0338
D ↓	hold_rising to CP	0.0127	0.0131	0.0131	0.0131
D ↑	hold_rising to CP	0.0146	0.0150	0.0146	0.0146
D ↓	setup_rising to CP	0.0171	0.0164	0.0164	0.0164
D ↑	setup_rising to CP	0.0097	0.0122	0.0122	0.0122

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	2.231e-04	3.132e-09
X17_P0	2.672e-04	3.464e-09
X30_P0	3.420e-04	3.795e-09
X33_P0	3.440e-04	3.795e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

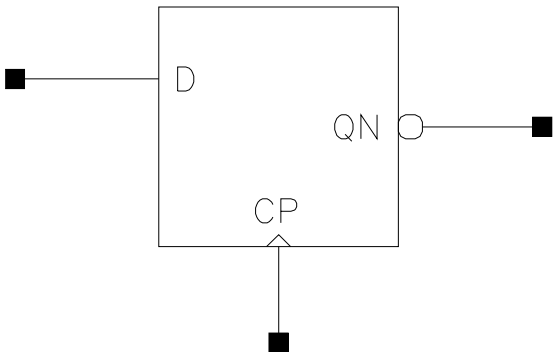
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.568e-03	5.586e-03	5.592e-03	5.595e-03
Clock 100Mhz Data 25Mhz	1.012e-02	1.189e-02	1.535e-02	1.606e-02
Clock 100Mhz Data 50Mhz	1.467e-02	1.820e-02	2.511e-02	2.652e-02
Clock = 0 Data 100Mhz	4.516e-03	4.642e-03	4.681e-03	4.701e-03
Clock = 1 Data 100Mhz	3.648e-05	3.623e-05	3.631e-05	3.635e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0272	0.0316	1.5617	0.8005
CP to QN ↑	0.0286	0.0308	2.2196	1.1296
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to QN ↓	0.0469	0.0472	0.4273	0.3884
CP to QN ↑	0.0389	0.0443	0.6130	0.5722

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0364	0.0364	0.0365	0.0365
CP ↑	min_pulse_width to CP	0.0205	0.0242	0.0205	0.0242
D ↓	hold_rising to CP	0.0152	0.0149	0.0131	0.0127
D ↑	hold_rising to CP	0.0177	0.0177	0.0150	0.0146
D ↓	setup_rising to CP	0.0146	0.0171	0.0164	0.0168
D ↑	setup_rising to CP	0.0122	0.0122	0.0122	0.0097

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	2.102e-04	2.801e-09
X17_P0	2.511e-04	2.967e-09
X30_P0	3.695e-04	3.795e-09
X33_P0	3.853e-04	3.961e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

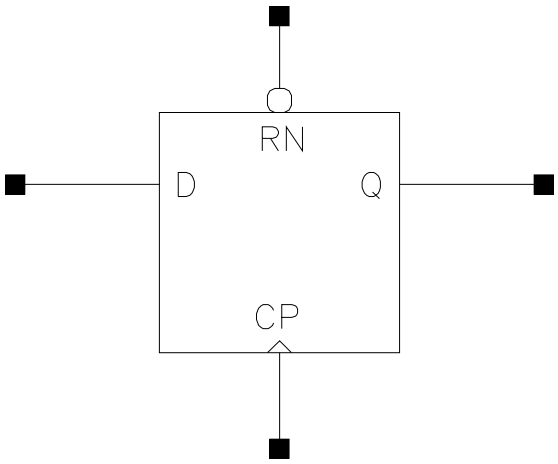
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.395e-03	5.397e-03	5.465e-03	5.495e-03
Clock 100Mhz Data 25Mhz	9.669e-03	1.113e-02	1.394e-02	1.489e-02
Clock 100Mhz Data 50Mhz	1.394e-02	1.686e-02	2.241e-02	2.430e-02
Clock = 0 Data 100Mhz	4.052e-03	4.052e-03	4.288e-03	4.346e-03
Clock = 1 Data 100Mhz	3.488e-05	3.518e-05	3.547e-05	3.577e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0010	0.0010
D	0.0007	0.0007
RN	0.0010	0.0010

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0327	0.0412	0.7845	0.4628
CP to Q ↑	0.0392	0.0443	1.1321	0.6336
RN to Q ↓	0.0448	0.0501	0.7646	0.4473

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0365	0.0365
CP ↑	min_pulse_width to CP	0.0253	0.0338
D ↓	hold_rising to CP	0.0131	0.0131
D ↑	hold_rising to CP	0.0128	0.0128
D ↓	setup_rising to CP	0.0195	0.0195
D ↑	setup_rising to CP	0.0119	0.0119
RN ↓	min_pulse_width to RN	0.0664	0.0854
RN ↑	recovery_rising to CP	0.0071	0.0071
RN ↑	removal_rising to CP	-0.0030	-0.0030

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P0	2.860e-04	4.292e-09
X30_P0	3.570e-04	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

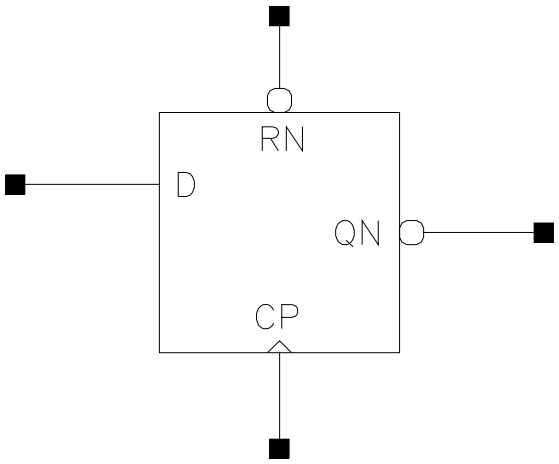
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	5.884e-03	5.886e-03
Clock 100Mhz Data 25Mhz	1.257e-02	1.596e-02
Clock 100Mhz Data 50Mhz	1.925e-02	2.603e-02
Clock = 0 Data 100Mhz	5.446e-03	5.449e-03
Clock = 1 Data 100Mhz	3.673e-05	3.668e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0010	0.0010
D	0.0007	0.0007
RN	0.0010	0.0010

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0450	0.0489	0.7465	0.4288
CP to QN ↑	0.0374	0.0408	1.1088	0.6160
RN to QN ↑	0.0511	0.0542	1.1074	0.6153

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0365	0.0365
CP ↑	min_pulse_width to CP	0.0205	0.0242
D ↓	hold_rising to CP	0.0131	0.0131
D ↑	hold_rising to CP	0.0128	0.0128
D ↓	setup_rising to CP	0.0220	0.0195
D ↑	setup_rising to CP	0.0119	0.0119
RN ↓	min_pulse_width to RN	0.0540	0.0566
RN ↑	recovery_rising to CP	0.0071	0.0071
RN ↑	removal_rising to CP	-0.0030	-0.0030

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P0	3.290e-04	4.292e-09
X30_P0	4.043e-04	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

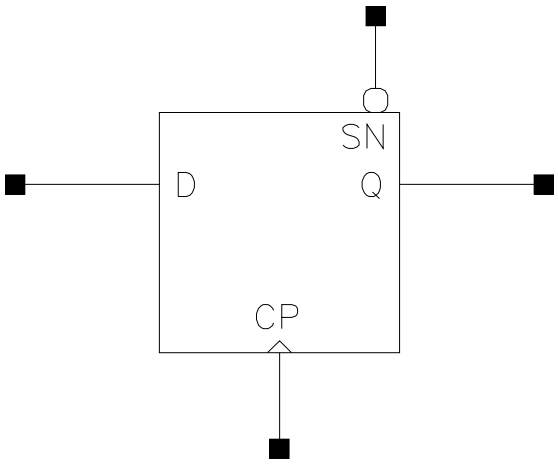
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	5.884e-03	5.884e-03
Clock 100Mhz Data 25Mhz	1.273e-02	1.487e-02
Clock 100Mhz Data 50Mhz	1.957e-02	2.387e-02
Clock = 0 Data 100Mhz	5.508e-03	5.493e-03
Clock = 1 Data 100Mhz	3.664e-05	3.668e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0013	0.0013

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0329	0.0418	0.7846	0.4606
CP to Q ↑	0.0387	0.0441	1.1327	0.6339
SN to Q ↑	0.0328	0.0361	1.1198	0.6243

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0402	0.0402
CP ↑	min_pulse_width to CP	0.0253	0.0338
D ↓	hold_rising to CP	0.0131	0.0131
D ↑	hold_rising to CP	0.0128	0.0125
D ↓	setup_rising to CP	0.0220	0.0220
D ↑	setup_rising to CP	0.0122	0.0123
SN ↓	min_pulse_width to SN	0.0430	0.0479
SN ↑	recovery_rising to CP	0.0007	0.0007
SN ↑	removal_rising to CP	0.0187	0.0187

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P0	2.979e-04	4.292e-09
X30_P0	3.749e-04	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

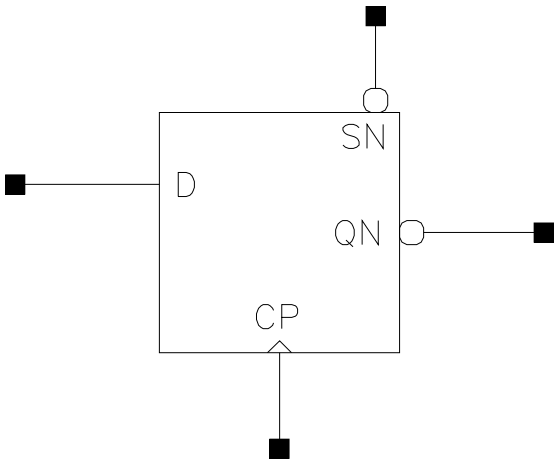
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	5.966e-03	5.951e-03
Clock 100Mhz Data 25Mhz	1.268e-02	1.602e-02
Clock 100Mhz Data 50Mhz	1.939e-02	2.609e-02
Clock = 0 Data 100Mhz	5.385e-03	5.385e-03
Clock = 1 Data 100Mhz	3.648e-05	3.673e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0013	0.0013

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0446	0.0485	0.7478	0.4295
CP to QN ↑	0.0376	0.0409	1.1051	0.6146
SN to QN ↓	0.0393	0.0429	0.7478	0.4293

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0402	0.0402
CP ↑	min_pulse_width to CP	0.0205	0.0242
D ↓	hold_rising to CP	0.0100	0.0100
D ↑	hold_rising to CP	0.0128	0.0128
D ↓	setup_rising to CP	0.0216	0.0216
D ↑	setup_rising to CP	0.0122	0.0122
SN ↓	min_pulse_width to SN	0.0354	0.0354
SN ↑	recovery_rising to CP	0.0007	0.0007
SN ↑	removal_rising to CP	0.0187	0.0187

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P0	3.150e-04	4.292e-09
X30_P0	3.834e-04	4.623e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

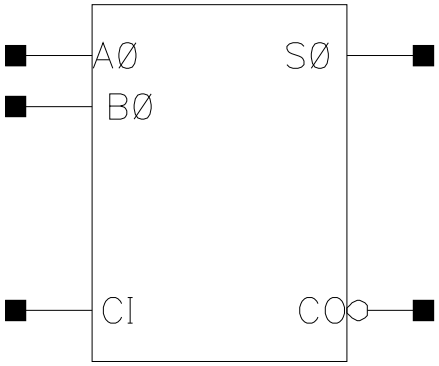
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	5.955e-03	5.951e-03
Clock 100Mhz Data 25Mhz	1.278e-02	1.491e-02
Clock 100Mhz Data 50Mhz	1.960e-02	2.386e-02
Clock = 0 Data 100Mhz	5.385e-03	5.387e-03
Clock = 1 Data 100Mhz	3.689e-05	3.689e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_P0	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_P0	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_P0	1.200	3.672	4.4064
C12T28SOI_LRS1_FA1X33_P0	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_FA1X8_P0	C12T28SOI_LR_FA1X33_P0	C12T28SOI_LRS1_FA1X8_P0	C12T28SOI_LRS1_FA1X33_P0
A0	0.0033	0.0067	0.0029	0.0057
B0	0.0030	0.0064	0.0032	0.0056
CI	0.0022	0.0047	0.0022	0.0040

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0
A0 to CO ↓	0.0312	0.0343	1.5822	0.4133
A0 to CO ↑	0.0227	0.0241	2.2880	0.5882
A0 to S0 ↓	0.0320	0.0409	1.5643	0.4043
A0 to S0 ↑	0.0331	0.0409	2.2703	0.5824
B0 to CO ↓	0.0313	0.0349	1.5866	0.4152
B0 to CO ↑	0.0235	0.0251	2.2893	0.5859
B0 to S0 ↓	0.0326	0.0418	1.5652	0.4044
B0 to S0 ↑	0.0336	0.0418	2.2710	0.5823
CI to CO ↓	0.0310	0.0352	1.5875	0.4139
CI to CO ↑	0.0235	0.0248	2.2866	0.5877
CI to S0 ↓	0.0324	0.0415	1.5651	0.4043
CI to S0 ↑	0.0339	0.0424	2.2702	0.5822
	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0
A0 to CO ↓	0.0213	0.0259	2.8531	0.4924
A0 to CO ↑	0.0175	0.0198	2.3367	0.5766
A0 to S0 ↓	0.0428	0.0527	1.6907	0.4228
A0 to S0 ↑	0.0398	0.0431	2.3571	0.5930
B0 to CO ↓	0.0224	0.0273	2.8548	0.4931
B0 to CO ↑	0.0160	0.0188	2.3347	0.5767
B0 to S0 ↓	0.0431	0.0542	1.6911	0.4228
B0 to S0 ↑	0.0401	0.0445	2.3567	0.5932
CI to CO ↓	0.0221	0.0378	2.8487	0.4993
CI to CO ↑	0.0176	0.0216	2.3977	0.5807
CI to S0 ↓	0.0251	0.0322	1.6926	0.4233
CI to S0 ↑	0.0213	0.0215	2.3560	0.5933

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_FA1X8_P0	2.309e-04	3.132e-09
C12T28SOI_LR_FA1X33_P0	6.159e-04	6.445e-09
C12T28SOI_LRS1_FA1X8_P0	5.283e-04	4.954e-09
C12T28SOI_LRS1_FA1X33_P0	1.098e-03	1.025e-08

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0
A0 to CO	5.376e-03	1.666e-02	8.132e-03	2.079e-02
A0 to S0	5.406e-03	1.726e-02	1.086e-02	2.555e-02
B0 to CO	5.449e-03	1.702e-02	8.199e-03	2.105e-02
B0 to S0	5.390e-03	1.730e-02	1.103e-02	2.603e-02
CI to CO	5.570e-03	1.735e-02	5.949e-03	1.938e-02
CI to S0	5.377e-03	1.730e-02	6.749e-03	2.069e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0
A0 to CO	-1.228e-07	-3.506e-07	2.969e-07	5.054e-07

A0 to S0	2.121e-07	1.970e-08	1.768e-07	3.917e-07
B0 to CO	-8.031e-08	-2.659e-07	2.590e-08	1.864e-06
B0 to S0	4.407e-07	1.708e-07	-1.563e-07	1.786e-06
CI to CO	-8.905e-08	-2.675e-07	8.070e-07	-4.420e-07
CI to S0	4.520e-07	6.675e-09	1.241e-06	-9.698e-08

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X33_P0	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X33_P0
A0	0.0011	0.0033
B0	0.0010	0.0028

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
A0 to CO ↓	0.0243	0.0230	1.5656	0.3888
A0 to CO ↑	0.0209	0.0194	2.2591	0.5834
A0 to S0 ↓	0.0295	0.0289	1.5367	0.3886
A0 to S0 ↑	0.0291	0.0337	2.2350	0.5755
B0 to CO ↓	0.0235	0.0211	1.5643	0.3861
B0 to CO ↑	0.0227	0.0208	2.2578	0.5831
B0 to S0 ↓	0.0312	0.0296	1.5358	0.3885
B0 to S0 ↑	0.0285	0.0323	2.2339	0.5752

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	1.458e-04	1.973e-09
X33_P0	5.543e-04	4.126e-09

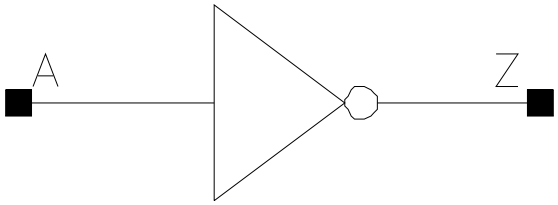
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X33_P0
A0 to CO	4.110e-03	1.420e-02
A0 to S0	3.910e-03	1.427e-02
B0 to CO	4.196e-03	1.462e-02
B0 to S0	3.881e-03	1.400e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X8_P0	X33_P0
A0 to CO	1.624e-07	6.883e-07
A0 to S0	2.586e-07	3.401e-07
B0 to CO	3.090e-08	3.650e-07
B0 to S0	1.058e-07	1.149e-08

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.272	0.3264
X6_P0	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X13_P0	1.200	0.408	0.4896
X17_P0	1.200	0.408	0.4896
X21_P0	1.200	0.544	0.6528
X25_P0	1.200	0.544	0.6528
X29_P0	1.200	0.680	0.8160
X33_P0	1.200	0.680	0.8160
X50_P0	1.200	0.952	1.1424
X58_P0	1.200	1.088	1.3056
X67_P0	1.200	1.224	1.4688
X75_P0	1.200	1.360	1.6320
X84_P0	1.200	1.496	1.7952
X100_P0	1.200	1.768	2.1216
X134_P0	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0006	0.0007	0.0009	0.0014
	X17_P0	X21_P0	X25_P0	X29_P0
A	0.0018	0.0024	0.0027	0.0033
	X33_P0	X50_P0	X58_P0	X67_P0
A	0.0036	0.0054	0.0064	0.0073
	X75_P0	X84_P0	X100_P0	X134_P0

A	0.0084	0.0094	0.0114	0.0155

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0036	0.0034	2.8907	2.2623
A to Z ↑	0.0097	0.0090	4.3281	3.2979
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0028	0.0021	1.5700	1.0052
A to Z ↑	0.0084	0.0078	2.3100	1.5112
	X17_P0	**X21_P0**	**X17_P0**	**X21_P0**
A to Z ↓	0.0021	0.0025	0.7791	0.6211
A to Z ↑	0.0075	0.0078	1.1393	0.9114
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0025	0.0022	0.5334	0.4506
A to Z ↑	0.0076	0.0073	0.7669	0.6517
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0022	0.0024	0.4007	0.2703
A to Z ↑	0.0071	0.0072	0.5746	0.3850
	X58_P0	**X67_P0**	**X58_P0**	**X67_P0**
A to Z ↓	0.0027	0.0027	0.2344	0.2060
A to Z ↑	0.0074	0.0073	0.3319	0.2912
	X75_P0	**X84_P0**	**X75_P0**	**X84_P0**
A to Z ↓	0.0031	0.0033	0.1860	0.1685
A to Z ↑	0.0077	0.0078	0.2614	0.2366
	X100_P0	**X134_P0**	**X100_P0**	**X134_P0**
A to Z ↓	0.0040	0.0048	0.1436	0.1123
A to Z ↑	0.0085	0.0092	0.1994	0.1538

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.654e-05	8.135e-10
X6_P0	3.338e-05	8.135e-10
X8_P0	4.685e-05	8.135e-10
X13_P0	7.413e-05	9.792e-10
X17_P0	9.270e-05	9.792e-10
X21_P0	1.180e-04	1.145e-09
X25_P0	1.313e-04	1.145e-09
X29_P0	1.606e-04	1.310e-09
X33_P0	1.691e-04	1.310e-09
X50_P0	2.444e-04	1.642e-09
X58_P0	2.821e-04	1.807e-09
X67_P0	3.198e-04	1.973e-09
X75_P0	3.575e-04	2.139e-09
X84_P0	3.953e-04	2.304e-09
X100_P0	4.707e-04	2.635e-09
X134_P0	6.216e-04	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0

A to Z	1.046e-03	1.316e-03	1.801e-03	2.715e-03
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	3.492e-03	4.551e-03	5.239e-03	6.092e-03
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	6.716e-03	9.959e-03	1.179e-02	1.325e-02
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	1.515e-02	1.683e-02	2.070e-02	2.861e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

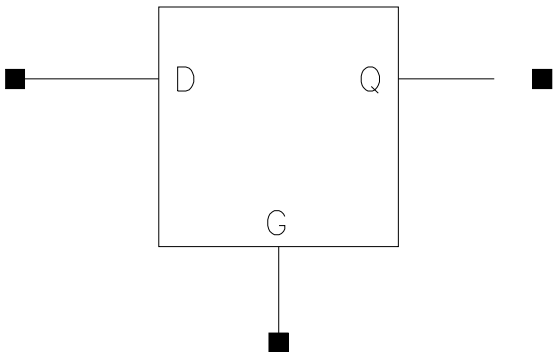
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	2.552e-07	5.610e-08	1.317e-07	-9.755e-07
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	-1.592e-06	-3.879e-06	-3.309e-06	-2.693e-06
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	-2.961e-06	-4.555e-06	-6.578e-06	1.270e-07
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	7.520e-07	1.580e-07	-2.540e-07	7.390e-07

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X23_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P0	X23_P0
D	0.0006	0.0014
G	0.0012	0.0019

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X23_P0	X8_P0	X23_P0
D to Q ↓	0.0351	0.0287	1.5772	0.7231
D to Q ↑	0.0225	0.0229	2.2259	0.5924
G to Q ↓	0.0350	0.0293	1.5707	0.7218
G to Q ↑	0.0219	0.0200	2.2272	0.5931

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X23_P0
D ↓	hold_falling to G	0.0005	0.0051
D ↑	hold_falling to G	0.0089	0.0094
D ↓	setup_falling to G	0.0366	0.0245
D ↑	setup_falling to G	0.0229	0.0280
G ↑	min_pulse_width to G	0.0301	0.0301

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	1.246e-04	1.973e-09
X23_P0	2.587e-04	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X23_P0
D (output stable)	2.521e-05	1.005e-04
G (output stable)	1.549e-03	3.054e-03
D to Q	7.016e-03	1.397e-02
G to Q	6.853e-03	1.326e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

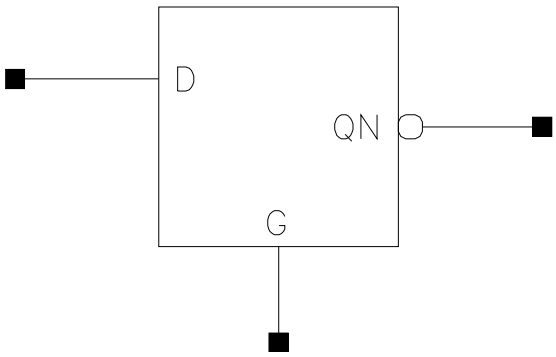
Pin Cycle (vdds)	X8_P0	X23_P0
D (output stable)	1.456e-07	3.521e-07
G (output stable)	5.400e-07	9.759e-07
D to Q	2.842e-07	2.195e-07
G to Q	5.931e-05	2.849e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P0
D	0.0006
G	0.0014

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P0	X17_P0
D to QN ↓	0.0290	0.7491
D to QN ↑	0.0394	1.0975
G to QN ↓	0.0279	0.7487
G to QN ↑	0.0381	1.0982

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X17_P0
D ↓	hold_falling to G	-0.0044
D ↑	hold_falling to G	0.0065
D ↓	setup_falling to G	0.0293
D ↑	setup_falling to G	0.0211
G ↑	min_pulse_width to G	0.0242

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P0	1.878e-04	2.139e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X17_P0
D (output stable)	2.580e-05
G (output stable)	1.932e-03
D to QN	8.287e-03
G to QN	8.254e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

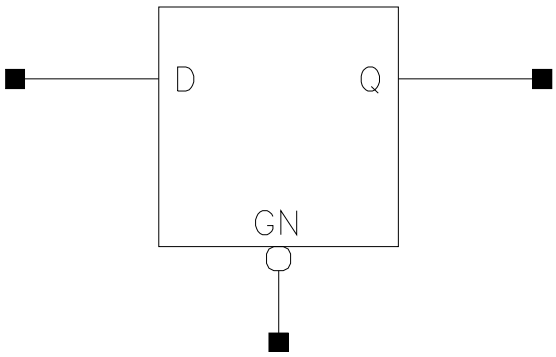
Pin Cycle (vdds)	X17_P0
D (output stable)	1.598e-07
G (output stable)	1.938e-06
D to QN	5.701e-07
G to QN	1.040e-04

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
D	0.0006	0.0008	0.0018
GN	0.0011	0.0015	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D to Q ↓	0.0355	0.0313	1.5811	0.7809
D to Q ↑	0.0228	0.0218	2.2289	1.1426
GN to Q ↓	0.0332	0.0285	1.5813	0.7819
GN to Q ↑	0.0348	0.0339	2.2236	1.1414

	X33_P0		X33_P0	
D to Q ↓	0.0302		0.3994	
D to Q ↑	0.0184		0.5746	
GN to Q ↓	0.0266		0.3996	
GN to Q ↑	0.0267		0.5737	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X17_P0	X33_P0
D ↓	hold_rising to GN	-0.0029	0.0023	0.0023
D ↑	hold_rising to GN	0.0106	0.0128	0.0128
D ↓	setup_rising to GN	0.0394	0.0345	0.0352
D ↑	setup_rising to GN	0.0221	0.0190	0.0168
GN ↓	min_pulse_width to GN	0.0470	0.0414	0.0369

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	1.181e-04	1.973e-09
X17_P0	1.830e-04	2.304e-09
X33_P0	3.015e-04	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
D (output stable)	2.484e-05	4.109e-05	1.099e-04
GN (output stable)	1.539e-03	2.070e-03	2.766e-03
D to Q	7.061e-03	1.025e-02	1.658e-02
GN to Q	9.673e-03	1.342e-02	2.007e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

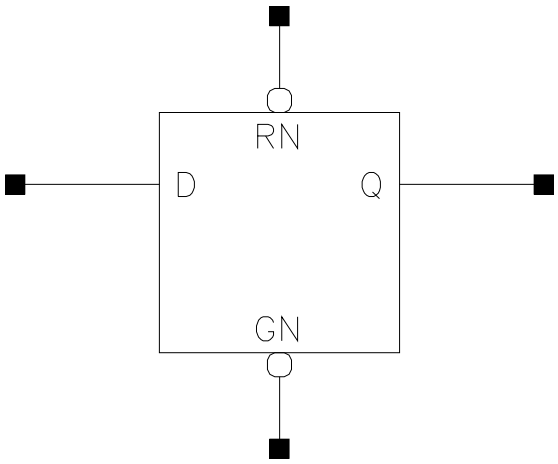
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
D (output stable)	1.563e-07	1.793e-07	3.608e-07
GN (output stable)	5.011e-07	3.011e-07	1.366e-06
D to Q	3.045e-07	2.511e-07	2.344e-07
GN to Q	-6.172e-05	-3.700e-05	-5.585e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.496	1.7952
X33_P0	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X33_P0
D	0.0006	0.0015
GN	0.0013	0.0024
RN	0.0006	0.0007

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
D to Q ↓	0.0330	0.0304	1.5466	0.4009
D to Q ↑	0.0295	0.0384	2.2615	0.5871

GN to Q ↓	0.0310	0.0285	1.5495	0.4017
GN to Q ↑	0.0394	0.0418	2.2618	0.5865
RN to Q ↓	0.0273	0.0470	1.4773	0.4057
RN to Q ↑	0.0301	0.0427	2.2646	0.5872

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X33_P0
D ↓	hold_rising to GN	-0.0002	0.0016
D ↑	hold_rising to GN	0.0058	-0.0039
D ↓	setup_rising to GN	0.0346	0.0328
D ↑	setup_rising to GN	0.0291	0.0440
GN ↓	min_pulse_width to GN	0.0424	0.0451
RN ↓	min_pulse_width to RN	0.0327	0.0615
RN ↑	recovery_rising to GN	0.0291	0.0459
RN ↑	removal_rising to GN	-0.0169	-0.0292

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	1.156e-04	2.304e-09
X33_P0	2.645e-04	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X33_P0
D (output stable)	6.607e-05	1.273e-04
GN (output stable)	1.730e-03	2.771e-03
RN (output stable)	7.047e-05	1.293e-04
D to Q	7.095e-03	1.984e-02
GN to Q	9.930e-03	2.409e-02
RN to Q	5.238e-03	1.628e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

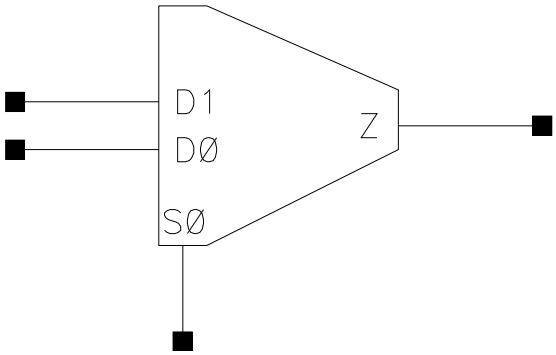
Pin Cycle (vdds)	X8_P0	X33_P0
D (output stable)	1.207e-07	1.370e-07
GN (output stable)	4.034e-07	7.771e-07
RN (output stable)	1.166e-07	1.212e-07
D to Q	1.849e-07	-1.410e-07
GN to Q	-5.800e-05	3.056e-05
RN to Q	5.664e-06	-1.895e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
D0	0.0008	0.0011	0.0015	0.0020
D1	0.0008	0.0011	0.0015	0.0020
S0	0.0013	0.0015	0.0017	0.0025

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D0 to Z ↓	0.0273	0.0250	1.5652	0.7665
D0 to Z ↑	0.0213	0.0198	2.2916	1.1225
D1 to Z ↓	0.0260	0.0245	1.5619	0.7653
D1 to Z ↑	0.0196	0.0187	2.2869	1.1215
S0 to Z ↓	0.0234	0.0231	1.5533	0.7624
S0 to Z ↑	0.0223	0.0229	2.2863	1.1214

	X25_P0	X33_P0	X25_P0	X33_P0
D0 to Z ↓	0.0264	0.0240	0.5263	0.3946
D0 to Z ↑	0.0211	0.0196	0.7547	0.5658
D1 to Z ↓	0.0280	0.0248	0.5285	0.3956
D1 to Z ↑	0.0205	0.0191	0.7541	0.5657
S0 to Z ↓	0.0262	0.0241	0.5255	0.3936
S0 to Z ↑	0.0254	0.0234	0.7540	0.5653

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	1.473e-04	1.973e-09
X17_P0	2.471e-04	2.139e-09
X25_P0	3.436e-04	3.298e-09
X33_P0	4.684e-04	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	1.491e-03	2.387e-03	2.873e-03	4.093e-03
D1 (output stable)	1.327e-03	2.318e-03	3.024e-03	4.162e-03
S0 (output stable)	1.767e-03	1.968e-03	2.492e-03	3.200e-03
D0 to Z	4.725e-03	8.125e-03	1.249e-02	1.586e-02
D1 to Z	4.400e-03	7.930e-03	1.262e-02	1.580e-02
S0 to Z	5.463e-03	8.561e-03	1.375e-02	1.699e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

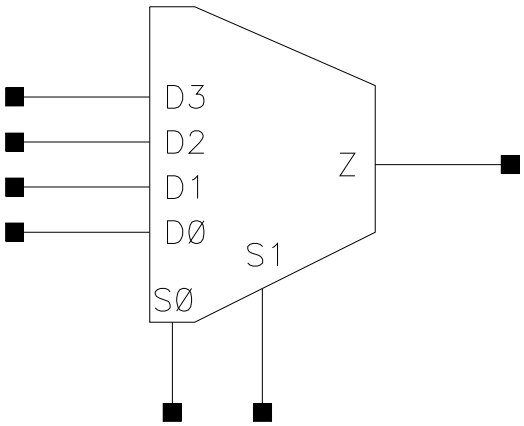
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	1.276e-06	1.260e-06	-3.295e-08	-5.070e-07
D1 (output stable)	6.269e-07	1.034e-06	0.000e+00	-5.835e-07
S0 (output stable)	3.631e-07	3.882e-07	2.392e-07	4.071e-07
D0 to Z	7.300e-09	5.395e-07	3.448e-07	6.400e-07
D1 to Z	3.870e-07	6.090e-07	3.580e-07	8.845e-07
S0 to Z	9.776e-07	7.791e-07	2.582e-07	1.097e-06

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.312	2.7744
X31_P0	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P0	X31_P0
D0	0.0006	0.0016
D1	0.0006	0.0016
D2	0.0006	0.0016
D3	0.0006	0.0016
S0	0.0020	0.0039
S1	0.0012	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X31_P0	X8_P0	X31_P0

D0 to Z ↓	0.0462	0.0484	1.6298	0.4495
D0 to Z ↑	0.0299	0.0324	2.2955	0.6195
D1 to Z ↓	0.0458	0.0484	1.6285	0.4496
D1 to Z ↑	0.0300	0.0322	2.2967	0.6194
D2 to Z ↓	0.0493	0.0453	1.6393	0.4452
D2 to Z ↑	0.0317	0.0297	2.3030	0.6153
D3 to Z ↓	0.0492	0.0450	1.6390	0.4444
D3 to Z ↑	0.0313	0.0311	2.3023	0.6173
S0 to Z ↓	0.0496	0.0517	1.6321	0.4466
S0 to Z ↑	0.0374	0.0401	2.3005	0.6181
S1 to Z ↓	0.0362	0.0365	1.6332	0.4466
S1 to Z ↑	0.0300	0.0322	2.2989	0.6174

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	1.384e-04	3.298e-09
X31_P0	3.918e-04	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X31_P0
D0 (output stable)	3.726e-05	1.820e-04
D1 (output stable)	3.670e-05	1.679e-04
D2 (output stable)	4.183e-05	1.747e-04
D3 (output stable)	4.180e-05	1.723e-04
S0 (output stable)	2.396e-03	5.237e-03
S1 (output stable)	2.089e-03	4.345e-03
D0 to Z	5.284e-03	1.899e-02
D1 to Z	5.264e-03	1.907e-02
D2 to Z	5.616e-03	1.774e-02
D3 to Z	5.597e-03	1.785e-02
S0 to Z	7.880e-03	2.406e-02
S1 to Z	6.603e-03	1.994e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

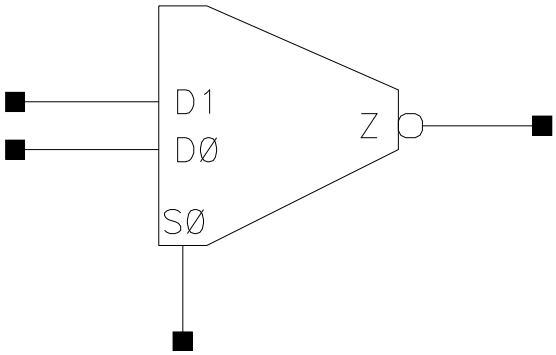
Pin Cycle (vdds)	X8_P0	X31_P0
D0 (output stable)	4.392e-07	1.516e-06
D1 (output stable)	4.487e-07	1.324e-06
D2 (output stable)	4.666e-07	1.417e-06
D3 (output stable)	4.716e-07	1.311e-06
S0 (output stable)	5.653e-07	1.605e-06
S1 (output stable)	7.562e-06	6.690e-06
D0 to Z	3.910e-07	4.874e-07
D1 to Z	3.128e-07	1.034e-06
D2 to Z	3.885e-07	8.310e-07
D3 to Z	3.758e-07	8.135e-07
S0 to Z	1.416e-06	4.032e-06
S1 to Z	1.620e-06	5.607e-07

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.816	0.9792
X5_P0	1.200	0.952	1.1424
X10_P0	1.200	1.768	2.1216
X16_P0	1.200	2.448	2.9376
X21_P0	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P0	X5_P0	X10_P0	X16_P0
D0	0.0006	0.0009	0.0018	0.0027
D1	0.0006	0.0009	0.0017	0.0027
S0	0.0011	0.0020	0.0025	0.0038
	X21_P0			
D0	0.0036			
D1	0.0035			
S0	0.0044			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X5_P0	X3_P0	X5_P0
D0 to Z ↓	0.0082	0.0082	4.5265	2.9167

D0 to Z ↑	0.0165	0.0150	9.0356	4.7534
D1 to Z ↓	0.0081	0.0080	4.4937	2.7552
D1 to Z ↑	0.0170	0.0154	9.0446	4.9695
S0 to Z ↓	0.0139	0.0120	4.4934	2.8304
S0 to Z ↑	0.0158	0.0136	9.0214	4.8482
	X10_P0	**X16_P0**	**X10_P0**	**X16_P0**
D0 to Z ↓	0.0093	0.0085	1.3808	0.9033
D0 to Z ↑	0.0162	0.0153	2.2340	1.4792
D1 to Z ↓	0.0085	0.0083	1.3289	0.8764
D1 to Z ↑	0.0162	0.0157	2.2744	1.4964
S0 to Z ↓	0.0147	0.0126	1.3521	0.8880
S0 to Z ↑	0.0162	0.0140	2.2508	1.4858
	X21_P0		**X21_P0**	
D0 to Z ↓	0.0084		0.6916	
D0 to Z ↑	0.0150		1.1219	
D1 to Z ↓	0.0083		0.6666	
D1 to Z ↑	0.0157		1.1170	
S0 to Z ↓	0.0133		0.6779	
S0 to Z ↑	0.0144		1.1171	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P0	5.435e-05	1.476e-09
X5_P0	1.053e-04	1.642e-09
X10_P0	1.781e-04	2.635e-09
X16_P0	2.728e-04	3.464e-09
X21_P0	3.323e-04	4.292e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	2.513e-05	5.644e-05	1.612e-04	2.457e-04
D1 (output stable)	2.514e-05	5.786e-05	1.362e-04	2.384e-04
S0 (output stable)	1.556e-03	2.485e-03	3.694e-03	6.232e-03
D0 to Z	1.369e-03	2.305e-03	5.503e-03	7.811e-03
D1 to Z	1.374e-03	2.284e-03	5.314e-03	7.734e-03
S0 to Z	2.618e-03	4.145e-03	7.740e-03	1.171e-02
	X21_P0			
D0 (output stable)	3.163e-04			
D1 (output stable)	3.173e-04			
S0 (output stable)	6.762e-03			
D0 to Z	1.012e-02			
D1 to Z	1.024e-02			
S0 to Z	1.406e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	1.472e-07	1.921e-07	3.062e-07	7.579e-07
D1 (output stable)	1.464e-07	3.677e-07	3.044e-07	6.607e-07
S0 (output stable)	6.704e-07	1.545e-06	1.279e-06	2.370e-06
D0 to Z	5.729e-07	1.558e-06	2.892e-06	6.342e-06

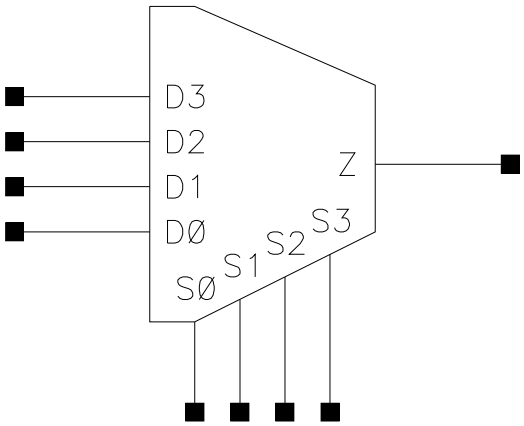
D1 to Z	6.427e-07	1.608e-06	2.801e-06	4.655e-06
S0 to Z	4.949e-07	1.228e-06	2.871e-06	-9.325e-07
	X21_P0			
D0 (output stable)	8.772e-07			
D1 (output stable)	9.850e-07			
S0 (output stable)	1.579e-06			
D0 to Z	8.353e-06			
D1 to Z	6.652e-06			
S0 to Z	-6.780e-07			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	1.768	2.1216
X27_P0	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P0	X27_P0
D0	0.0007	0.0020
D1	0.0007	0.0021
D2	0.0007	0.0020
D3	0.0007	0.0021
S0	0.0007	0.0019
S1	0.0008	0.0020
S2	0.0007	0.0019
S3	0.0007	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	X27_P0	X7_P0	X27_P0
D0 to Z ↓	0.0356	0.0300	2.3940	0.6585
D0 to Z ↑	0.0252	0.0215	2.2453	0.5630
D1 to Z ↓	0.0337	0.0288	2.3912	0.6581
D1 to Z ↑	0.0224	0.0187	2.2367	0.5610
D2 to Z ↓	0.0363	0.0295	2.4017	0.6590
D2 to Z ↑	0.0248	0.0203	2.2517	0.5646
D3 to Z ↓	0.0344	0.0281	2.3961	0.6578
D3 to Z ↑	0.0220	0.0175	2.2439	0.5623
S0 to Z ↓	0.0344	0.0284	2.3934	0.6582
S0 to Z ↑	0.0272	0.0231	2.2432	0.5625
S1 to Z ↓	0.0326	0.0271	2.3902	0.6577
S1 to Z ↑	0.0241	0.0199	2.2366	0.5606
S2 to Z ↓	0.0350	0.0277	2.4000	0.6585
S2 to Z ↑	0.0268	0.0219	2.2506	0.5641
S3 to Z ↓	0.0334	0.0264	2.3951	0.6573
S3 to Z ↑	0.0237	0.0187	2.2440	0.5621

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X7_P0	1.205e-04	2.635e-09
X27_P0	4.306e-04	4.954e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X7_P0	X27_P0
D0 (output stable)	6.700e-04	2.129e-03
D1 (output stable)	5.984e-04	1.861e-03
D2 (output stable)	6.218e-04	1.966e-03
D3 (output stable)	5.499e-04	1.690e-03
S0 (output stable)	6.507e-04	2.028e-03
S1 (output stable)	5.776e-04	1.774e-03
S2 (output stable)	6.030e-04	1.863e-03
S3 (output stable)	5.292e-04	1.605e-03
D0 to Z	5.477e-03	1.700e-02
D1 to Z	4.920e-03	1.518e-02
D2 to Z	5.393e-03	1.560e-02
D3 to Z	4.849e-03	1.377e-02
S0 to Z	5.365e-03	1.636e-02
S1 to Z	4.811e-03	1.459e-02
S2 to Z	5.279e-03	1.492e-02
S3 to Z	4.738e-03	1.317e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

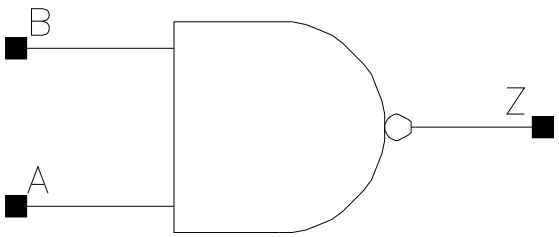
Pin Cycle (vdds)	X7_P0	X27_P0
D0 (output stable)	2.603e-07	4.669e-07
D1 (output stable)	4.440e-07	6.214e-07
D2 (output stable)	2.463e-07	5.451e-07
D3 (output stable)	4.189e-07	7.090e-07
S0 (output stable)	2.420e-07	4.473e-07
S1 (output stable)	4.302e-07	5.351e-07
S2 (output stable)	2.196e-07	5.378e-07
S3 (output stable)	3.963e-07	5.997e-07
D0 to Z	5.782e-07	1.946e-06
D1 to Z	4.618e-08	1.962e-06
D2 to Z	5.479e-07	1.797e-06
D3 to Z	4.740e-08	1.849e-06
S0 to Z	5.161e-07	1.710e-06
S1 to Z	2.360e-07	1.400e-06
S2 to Z	5.475e-07	1.644e-06
S3 to Z	2.497e-07	1.491e-06

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P0	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P0	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P0	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P0	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P0	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P0	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P0	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P0	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P0	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P0	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P0	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P0	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P0	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P0	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P0	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P0	C12T28SOI_LR_-NAND2X5_P0	C12T28SOI_LR_-NAND2X7_P0	C12T28SOI_LR_-NAND2X10_P0
A	0.0006	0.0008	0.0009	0.0015
B	0.0006	0.0008	0.0009	0.0014
	C12T28SOI_LR_-NAND2X13_P0	C12T28SOI_LR_-NAND2X17_P0	C12T28SOI_LR_-NAND2X20_P0	C12T28SOI_LR_-NAND2X24_P0
A	0.0018	0.0023	0.0027	0.0033
B	0.0018	0.0023	0.0026	0.0031
	C12T28SOI_LR_-NAND2X27_P0	C12T28SOI_LR_-NAND2X42_P0	C12T28SOI_LR_-NAND2X47_P0	C12T28SOI_LR_-NAND2X50_P0
A	0.0037	0.0010	0.0010	0.0010
B	0.0035	0.0011	0.0011	0.0011
	C12T28SOI_LR_-NAND2X58_P0	C12T28SOI_LR_-NAND2X67_P0	C12T28SOI_-LRBR0D8_-NAND2X7_P0	C12T28SOI_-LRBR0D8_-NAND2X14_P0
A	0.0010	0.0010	0.0009	0.0018
B	0.0011	0.0011	0.0009	0.0017
	C12T28SOI_LRS_-NAND2X40_P0	C12T28SOI_LRS_-NAND2X54_P0		
A	0.0055	0.0073		
B	0.0052	0.0071		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P0	**C12T28SOI_LR_-NAND2X5_P0**	**C12T28SOI_LR_-NAND2X3_P0**	**C12T28SOI_LR_-NAND2X5_P0**
A to Z ↓	0.0060	0.0052	4.4380	2.9256
A to Z ↑	0.0114	0.0105	4.3586	2.8359
B to Z ↓	0.0068	0.0059	4.5032	2.9654
B to Z ↑	0.0101	0.0091	4.3860	2.8542
	C12T28SOI_LR_-NAND2X7_P0	**C12T28SOI_LR_-NAND2X10_P0**	**C12T28SOI_LR_-NAND2X7_P0**	**C12T28SOI_LR_-NAND2X10_P0**
A to Z ↓	0.0052	0.0059	2.4728	1.6315
A to Z ↑	0.0102	0.0108	2.3022	1.5001
B to Z ↓	0.0059	0.0059	2.5043	1.6522
B to Z ↑	0.0087	0.0086	2.3275	1.5116
	C12T28SOI_LR_-NAND2X13_P0	**C12T28SOI_LR_-NAND2X17_P0**	**C12T28SOI_LR_-NAND2X13_P0**	**C12T28SOI_LR_-NAND2X17_P0**
A to Z ↓	0.0057	0.0055	1.2708	0.9994

A to Z ↑	0.0103	0.0103	1.1374	0.9102
B to Z ↓	0.0058	0.0060	1.2860	1.0114
B to Z ↑	0.0082	0.0085	1.1463	0.9177
	C12T28SOI_LR_-NAND2X20_P0	**C12T28SOI_LR_-NAND2X24_P0**	**C12T28SOI_LR_-NAND2X20_P0**	**C12T28SOI_LR_-NAND2X24_P0**
A to Z ↓	0.0055	0.0057	0.8686	0.7370
A to Z ↑	0.0101	0.0102	0.7662	0.6506
B to Z ↓	0.0062	0.0059	0.8791	0.7452
B to Z ↑	0.0083	0.0081	0.7731	0.6561
	C12T28SOI_LR_-NAND2X27_P0	**C12T28SOI_LR_-NAND2X42_P0**	**C12T28SOI_LR_-NAND2X27_P0**	**C12T28SOI_LR_-NAND2X42_P0**
A to Z ↓	0.0055	0.0246	0.6602	0.3129
A to Z ↑	0.0100	0.0273	0.5751	0.4476
B to Z ↓	0.0058	0.0258	0.6678	0.3127
B to Z ↑	0.0078	0.0262	0.5798	0.4478
	C12T28SOI_LR_-NAND2X47_P0	**C12T28SOI_LR_-NAND2X50_P0**	**C12T28SOI_LR_-NAND2X47_P0**	**C12T28SOI_LR_-NAND2X50_P0**
A to Z ↓	0.0255	0.0257	0.2772	0.2609
A to Z ↑	0.0279	0.0281	0.3889	0.3738
B to Z ↓	0.0266	0.0268	0.2773	0.2611
B to Z ↑	0.0268	0.0270	0.3888	0.3742
	C12T28SOI_LR_-NAND2X58_P0	**C12T28SOI_LR_-NAND2X67_P0**	**C12T28SOI_LR_-NAND2X58_P0**	**C12T28SOI_LR_-NAND2X67_P0**
A to Z ↓	0.0270	0.0280	0.2262	0.1988
A to Z ↑	0.0291	0.0299	0.3218	0.2825
B to Z ↓	0.0281	0.0291	0.2262	0.1988
B to Z ↑	0.0280	0.0288	0.3220	0.2825
	C12T28SOI_-LRBR0D8_-NAND2X7_P0	**C12T28SOI_-LRBR0D8_-NAND2X14_P0**	**C12T28SOI_-LRBR0D8_-NAND2X7_P0**	**C12T28SOI_-LRBR0D8_-NAND2X14_P0**
A to Z ↓	0.0030	0.0036	1.8930	1.0018
A to Z ↑	0.0128	0.0130	3.0215	1.4822
B to Z ↓	0.0031	0.0030	1.9290	1.0204
B to Z ↑	0.0109	0.0099	3.1278	1.5117
	C12T28SOI_LRS_-NAND2X40_P0	**C12T28SOI_LRS_-NAND2X54_P0**	**C12T28SOI_LRS_-NAND2X40_P0**	**C12T28SOI_LRS_-NAND2X54_P0**
A to Z ↓	0.0056	0.0056	0.4478	0.3391
A to Z ↑	0.0099	0.0099	0.3859	0.2911
B to Z ↓	0.0059	0.0062	0.4532	0.3433
B to Z ↑	0.0078	0.0079	0.3890	0.2937

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P0	2.519e-05	9.792e-10
C12T28SOI_LR_NAND2X5_P0	3.928e-05	9.792e-10
C12T28SOI_LR_NAND2X7_P0	4.602e-05	9.792e-10
C12T28SOI_LR_NAND2X10_P0	6.864e-05	1.310e-09
C12T28SOI_LR_NAND2X13_P0	8.671e-05	1.310e-09
C12T28SOI_LR_NAND2X17_P0	1.113e-04	1.642e-09
C12T28SOI_LR_NAND2X20_P0	1.245e-04	1.642e-09
C12T28SOI_LR_NAND2X24_P0	1.538e-04	1.973e-09
C12T28SOI_LR_NAND2X27_P0	1.623e-04	1.973e-09

C12T28SOI_LR_NAND2X42_P0	3.337e-04	2.139e-09
C12T28SOI_LR_NAND2X47_P0	3.796e-04	2.304e-09
C12T28SOI_LR_NAND2X50_P0	3.733e-04	2.304e-09
C12T28SOI_LR_NAND2X58_P0	4.129e-04	2.470e-09
C12T28SOI_LR_NAND2X67_P0	4.526e-04	2.635e-09
C12T28SOI_LRBR0D8_NAND2X7_P0	4.825e-05	1.804e-09
C12T28SOI_LRBR0D8_NAND2X14_-P0	8.972e-05	2.156e-09
C12T28SOI_LRS_NAND2X40_P0	2.381e-04	2.635e-09
C12T28SOI_LRS_NAND2X54_P0	3.139e-04	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P0	C12T28SOI_LR_-NAND2X5_P0	C12T28SOI_LR_-NAND2X7_P0	C12T28SOI_LR_-NAND2X10_P0
A (output stable)	2.019e-05	3.129e-05	3.697e-05	1.158e-04
B (output stable)	2.375e-05	3.639e-05	4.432e-05	2.354e-04
A to Z	1.179e-03	1.672e-03	2.003e-03	3.257e-03
B to Z	1.074e-03	1.516e-03	1.799e-03	2.777e-03
	C12T28SOI_LR_-NAND2X13_P0	C12T28SOI_LR_-NAND2X17_P0	C12T28SOI_LR_-NAND2X20_P0	C12T28SOI_LR_-NAND2X24_P0
A (output stable)	1.379e-04	1.651e-04	1.838e-04	2.499e-04
B (output stable)	2.676e-04	2.853e-04	3.099e-04	4.493e-04
A to Z	4.093e-03	5.187e-03	5.966e-03	7.167e-03
B to Z	3.530e-03	4.536e-03	5.245e-03	6.201e-03
	C12T28SOI_LR_-NAND2X27_P0	C12T28SOI_LR_-NAND2X42_P0	C12T28SOI_LR_-NAND2X47_P0	C12T28SOI_LR_-NAND2X50_P0
A (output stable)	2.705e-04	4.118e-05	4.054e-05	4.136e-05
B (output stable)	4.729e-04	4.936e-05	4.936e-05	5.036e-05
A to Z	7.860e-03	1.568e-02	1.729e-02	1.780e-02
B to Z	6.775e-03	1.550e-02	1.710e-02	1.761e-02
	C12T28SOI_LR_-NAND2X58_P0	C12T28SOI_LR_-NAND2X67_P0	C12T28SOI_-LRBR0D8_-NAND2X7_P0	C12T28SOI_-LRBR0D8_-NAND2X14_P0
A (output stable)	4.054e-05	4.104e-05	4.837e-05	1.730e-04
B (output stable)	5.036e-05	5.036e-05	5.828e-05	3.448e-04
A to Z	2.043e-02	2.283e-02	1.979e-03	4.067e-03
B to Z	2.025e-02	2.265e-02	1.700e-03	3.268e-03
	C12T28SOI_LRS_-NAND2X40_P0	C12T28SOI_LRS_-NAND2X54_P0		
A (output stable)	3.867e-04	5.047e-04		
B (output stable)	6.552e-04	8.402e-04		
A to Z	1.165e-02	1.550e-02		
B to Z	1.010e-02	1.349e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P0	C12T28SOI_LR_-NAND2X5_P0	C12T28SOI_LR_-NAND2X7_P0	C12T28SOI_LR_-NAND2X10_P0
A (output stable)	7.800e-08	8.550e-08	8.335e-08	6.840e-08
B (output stable)	9.350e-08	8.423e-08	7.944e-08	3.070e-08
A to Z	4.143e-07	7.700e-07	8.907e-07	1.452e-06
B to Z	3.844e-07	8.950e-07	1.191e-06	1.897e-06

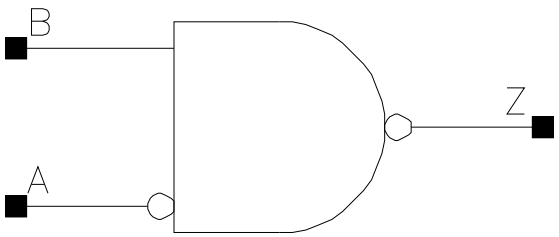
	C12T28SOI_LR_-NAND2X13_P0	C12T28SOI_LR_-NAND2X17_P0	C12T28SOI_LR_-NAND2X20_P0	C12T28SOI_LR_-NAND2X24_P0
A (output stable)	4.740e-08	2.670e-08	3.020e-08	-4.520e-08
B (output stable)	1.840e-08	4.000e-10	1.070e-08	-5.620e-08
A to Z	1.343e-06	1.285e-06	1.552e-06	2.364e-06
B to Z	4.090e-07	2.367e-06	1.140e-06	-3.000e-08
	C12T28SOI_LR_-NAND2X27_P0	C12T28SOI_LR_-NAND2X42_P0	C12T28SOI_LR_-NAND2X47_P0	C12T28SOI_LR_-NAND2X50_P0
A (output stable)	-5.680e-08	8.928e-08	8.927e-08	8.953e-08
B (output stable)	-6.480e-08	8.808e-08	8.858e-08	8.871e-08
A to Z	2.577e-06	2.720e-07	2.590e-07	2.250e-07
B to Z	-2.325e-06	-2.180e-07	-2.960e-07	-2.350e-07
	C12T28SOI_LR_-NAND2X58_P0	C12T28SOI_LR_-NAND2X67_P0	C12T28SOI_-LRBR0D8_-NAND2X7_P0	C12T28SOI_-LRBR0D8_-NAND2X14_P0
A (output stable)	8.956e-08	9.021e-08	9.350e-08	2.110e-08
B (output stable)	8.869e-08	8.890e-08	8.508e-08	-4.480e-08
A to Z	2.050e-07	2.950e-07	6.223e-07	3.970e-07
B to Z	-3.090e-07	-2.500e-07	2.745e-07	-1.940e-07
	C12T28SOI_LRS_-NAND2X40_P0	C12T28SOI_LRS_-NAND2X54_P0		
A (output stable)	-1.260e-07	-1.925e-07		
B (output stable)	-1.659e-07	-2.484e-07		
A to Z	2.790e-07	5.783e-06		
B to Z	-2.583e-06	-9.256e-06		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X7_P0	1.200	0.544	0.6528
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X40_P0	1.200	2.312	2.7744
X54_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P0	X7_P0	X13_P0	X27_P0
A	0.0008	0.0008	0.0011	0.0020
B	0.0007	0.0009	0.0017	0.0035
	X40_P0	X54_P0		
A	0.0030	0.0039		
B	0.0051	0.0070		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0195	0.0206	4.3592	2.4447
A to Z ↑	0.0140	0.0147	4.1867	2.2550
B to Z ↓	0.0070	0.0059	4.5334	2.5208
B to Z ↑	0.0102	0.0087	4.3886	2.3490
	X13_P0	**X27_P0**	**X13_P0**	**X27_P0**

A to Z ↓	0.0195	0.0190	1.3268	0.6581
A to Z ↑	0.0143	0.0140	1.1630	0.5635
B to Z ↓	0.0058	0.0057	1.3688	0.6799
B to Z ↑	0.0081	0.0077	1.1719	0.5808
	X40_P0	**X54_P0**	**X40_P0**	**X54_P0**
A to Z ↓	0.0192	0.0192	0.4386	0.3329
A to Z ↑	0.0143	0.0142	0.3749	0.2835
B to Z ↓	0.0059	0.0060	0.4531	0.3438
B to Z ↑	0.0078	0.0078	0.3905	0.2951

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P0	4.856e-05	1.145e-09
X7_P0	6.859e-05	1.145e-09
X13_P0	1.383e-04	1.642e-09
X27_P0	2.523e-04	2.470e-09
X40_P0	3.660e-04	3.298e-09
X54_P0	4.796e-04	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	1.657e-03	1.969e-03	3.351e-03	6.581e-03
B (output stable)	2.455e-05	4.463e-05	2.497e-04	4.266e-04
A to Z	2.608e-03	3.516e-03	6.453e-03	1.270e-02
B to Z	1.075e-03	1.784e-03	3.478e-03	6.793e-03
	X40_P0	X54_P0		
A (output stable)	9.919e-03	1.299e-02		
B (output stable)	6.190e-04	8.107e-04		
A to Z	1.906e-02	2.523e-02		
B to Z	1.009e-02	1.336e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

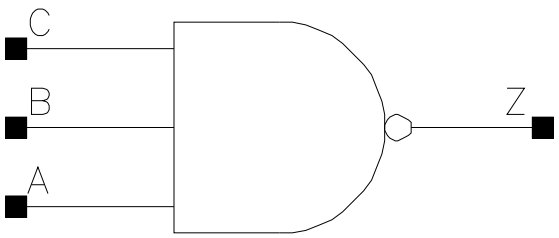
Pin Cycle (vdds)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	4.910e-08	2.573e-07	4.985e-07	5.457e-07
B (output stable)	9.230e-08	7.956e-08	4.290e-08	-6.710e-08
A to Z	1.167e-06	1.325e-07	2.895e-06	5.862e-06
B to Z	3.571e-07	1.177e-06	3.860e-07	2.050e-06
	X40_P0	X54_P0		
A (output stable)	5.100e-07	7.120e-07		
B (output stable)	-1.529e-07	-2.684e-07		
A to Z	8.180e-06	-1.712e-06		
B to Z	3.322e-06	6.111e-06		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P0	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P0	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P0	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P0	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P0	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P0	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P0	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P0	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P0	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P0	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P0	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P0	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P0	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P0	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P0	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A	0.0007	0.0009	0.0015	0.0018
B	0.0008	0.0009	0.0014	0.0017
C	0.0007	0.0009	0.0014	0.0017
	C12T28SOI_LR_-NAND3X15_P0	C12T28SOI_LR_-NAND3X18_P0	C12T28SOI_LR_-NAND3X21_P0	C12T28SOI_LR_-NAND3X24_P0
A	0.0023	0.0027	0.0033	0.0036
B	0.0023	0.0026	0.0031	0.0035
C	0.0022	0.0025	0.0031	0.0034
	C12T28SOI_LR_-NAND3X35_P0	C12T28SOI_LR_-NAND3X47_P0	C12T28SOI_-LRBR0P6_-NAND3X6_P0	C12T28SOI_-LRBR0P6_-NAND3X12_P0
A	0.0054	0.0073	0.0009	0.0018
B	0.0052	0.0070	0.0010	0.0017
C	0.0051	0.0070	0.0009	0.0017
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	C12T28SOI_-LRBR0P6_-NAND3X24_P0	C12T28SOI_-LRBR0P6_-NAND3X35_P0	C12T28SOI_-LRBR0P6_-NAND3X47_P0
A	0.0026	0.0035	0.0053	0.0071
B	0.0025	0.0034	0.0051	0.0069
C	0.0025	0.0033	0.0050	0.0067
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0			
A	0.0027			
B	0.0026			
C	0.0025			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P0	**C12T28SOI_LR_-NAND3X6_P0**	**C12T28SOI_LR_-NAND3X4_P0**	**C12T28SOI_LR_-NAND3X6_P0**
A to Z ↓	0.0099	0.0089	4.6323	3.3599
A to Z ↑	0.0142	0.0129	3.2180	2.2462
B to Z ↓	0.0111	0.0099	4.6581	3.3785
B to Z ↑	0.0135	0.0121	3.2246	2.2514
C to Z ↓	0.0106	0.0097	4.6783	3.3925
C to Z ↑	0.0115	0.0103	3.2265	2.2647

	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A to Z ↓	0.0098	0.0093	2.2656	1.7873
A to Z ↑	0.0135	0.0128	1.5123	1.1516
B to Z ↓	0.0101	0.0097	2.2767	1.7957
B to Z ↑	0.0122	0.0115	1.5158	1.1540
C to Z ↓	0.0097	0.0094	2.2860	1.8037
C to Z ↑	0.0103	0.0096	1.5099	1.1452
	C12T28SOI_LR_-NAND3X15_P0	**C12T28SOI_LR_-NAND3X18_P0**	**C12T28SOI_LR_-NAND3X15_P0**	**C12T28SOI_LR_-NAND3X18_P0**
A to Z ↓	0.0088	0.0087	1.4187	1.2312
A to Z ↑	0.0124	0.0121	0.9129	0.7661
B to Z ↓	0.0096	0.0095	1.4271	1.2377
B to Z ↑	0.0111	0.0108	0.9154	0.7680
C to Z ↓	0.0094	0.0093	1.4332	1.2429
C to Z ↑	0.0094	0.0090	0.9218	0.7733
	C12T28SOI_LR_-NAND3X21_P0	**C12T28SOI_LR_-NAND3X24_P0**	**C12T28SOI_LR_-NAND3X21_P0**	**C12T28SOI_LR_-NAND3X24_P0**
A to Z ↓	0.0091	0.0090	1.0415	0.9355
A to Z ↑	0.0125	0.0123	0.6561	0.5803
B to Z ↓	0.0097	0.0096	1.0464	0.9400
B to Z ↑	0.0112	0.0110	0.6572	0.5810
C to Z ↓	0.0095	0.0095	1.0510	0.9441
C to Z ↑	0.0094	0.0092	0.6581	0.5817
	C12T28SOI_LR_-NAND3X35_P0	**C12T28SOI_LR_-NAND3X47_P0**	**C12T28SOI_LR_-NAND3X35_P0**	**C12T28SOI_LR_-NAND3X47_P0**
A to Z ↓	0.0085	0.0088	0.6384	0.4868
A to Z ↑	0.0119	0.0121	0.3894	0.2950
B to Z ↓	0.0094	0.0096	0.6420	0.4895
B to Z ↑	0.0107	0.0107	0.3897	0.2938
C to Z ↓	0.0093	0.0094	0.6449	0.4918
C to Z ↑	0.0088	0.0087	0.3917	0.2951
	C12T28SOI_-LRBR0P6_-NAND3X6_P0	**C12T28SOI_-LRBR0P6_-NAND3X12_P0**	**C12T28SOI_-LRBR0P6_-NAND3X6_P0**	**C12T28SOI_-LRBR0P6_-NAND3X12_P0**
A to Z ↓	0.0057	0.0060	2.3177	1.2291
A to Z ↑	0.0185	0.0184	3.4561	1.7686
B to Z ↓	0.0060	0.0055	2.3450	1.2437
B to Z ↑	0.0167	0.0159	3.4674	1.7727
C to Z ↓	0.0049	0.0043	2.3728	1.2590
C to Z ↑	0.0134	0.0123	3.4848	1.7775
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	**C12T28SOI_-LRBR0P6_-NAND3X24_P0**	**C12T28SOI_-LRBR0P6_-NAND3X18_P0**	**C12T28SOI_-LRBR0P6_-NAND3X24_P0**
A to Z ↓	0.0054	0.0057	0.8473	0.6430
A to Z ↑	0.0175	0.0178	1.1772	0.8901
B to Z ↓	0.0053	0.0053	0.8577	0.6508
B to Z ↑	0.0150	0.0154	1.1811	0.8920
C to Z ↓	0.0044	0.0043	0.8669	0.6583
C to Z ↑	0.0120	0.0120	1.1889	0.8921
	C12T28SOI_-LRBR0P6_-NAND3X35_P0	**C12T28SOI_-LRBR0P6_-NAND3X47_P0**	**C12T28SOI_-LRBR0P6_-NAND3X35_P0**	**C12T28SOI_-LRBR0P6_-NAND3X47_P0**

A to Z ↓	0.0053	0.0054	0.4398	0.3365
A to Z ↑	0.0178	0.0178	0.6136	0.4643
B to Z ↓	0.0052	0.0052	0.4457	0.3409
B to Z ↑	0.0153	0.0153	0.6140	0.4642
C to Z ↓	0.0043	0.0045	0.4509	0.3445
C to Z ↑	0.0119	0.0120	0.6190	0.4652
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P0**	
A to Z ↓	0.0060		0.8327	
A to Z ↑	0.0178		1.1264	
B to Z ↓	0.0054		0.8420	
B to Z ↑	0.0154		1.1294	
C to Z ↓	0.0043		0.8519	
C to Z ↑	0.0119		1.1199	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P0	2.760e-05	1.310e-09
C12T28SOI_LR_NAND3X6_P0	3.882e-05	1.310e-09
C12T28SOI_LR_NAND3X9_P0	5.551e-05	1.807e-09
C12T28SOI_LR_NAND3X12_P0	6.988e-05	1.807e-09
C12T28SOI_LR_NAND3X15_P0	8.556e-05	2.139e-09
C12T28SOI_LR_NAND3X18_P0	9.599e-05	2.139e-09
C12T28SOI_LR_NAND3X21_P0	1.226e-04	2.801e-09
C12T28SOI_LR_NAND3X24_P0	1.296e-04	2.801e-09
C12T28SOI_LR_NAND3X35_P0	1.890e-04	3.795e-09
C12T28SOI_LR_NAND3X47_P0	2.486e-04	4.789e-09
C12T28SOI_LRBR0P6_NAND3X6_P0	4.163e-05	2.248e-09
C12T28SOI_LRBR0P6_NAND3X12_-P0	7.605e-05	2.790e-09
C12T28SOI_LRBR0P6_NAND3X18_-P0	1.034e-04	3.151e-09
C12T28SOI_LRBR0P6_NAND3X24_-P0	1.428e-04	3.874e-09
C12T28SOI_LRBR0P6_NAND3X35_-P0	2.092e-04	4.958e-09
C12T28SOI_LRBR0P6_NAND3X47_-P0	2.760e-04	6.042e-09
C12T28SOIDV_LRBR0P6_-NAND3X18_P0	1.233e-04	2.606e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A (output stable)	4.111e-05	5.445e-05	1.239e-04	1.442e-04
B (output stable)	5.801e-05	7.296e-05	1.509e-04	1.789e-04
C (output stable)	1.804e-04	2.109e-04	3.214e-04	3.738e-04
A to Z	2.142e-03	2.724e-03	4.311e-03	5.243e-03
B to Z	1.963e-03	2.474e-03	3.730e-03	4.549e-03
C to Z	1.711e-03	2.187e-03	3.253e-03	4.002e-03

	C12T28SOI_LR_-NAND3X15_P0	C12T28SOI_LR_-NAND3X18_P0	C12T28SOI_LR_-NAND3X21_P0	C12T28SOI_LR_-NAND3X24_P0
A (output stable)	1.626e-04	1.837e-04	2.523e-04	2.723e-04
B (output stable)	2.018e-04	2.317e-04	3.043e-04	3.315e-04
C (output stable)	4.149e-04	4.623e-04	6.147e-04	6.674e-04
A to Z	6.416e-03	7.320e-03	9.037e-03	9.926e-03
B to Z	5.560e-03	6.349e-03	7.849e-03	8.633e-03
C to Z	4.954e-03	5.628e-03	6.915e-03	7.585e-03
	C12T28SOI_LR_-NAND3X35_P0	C12T28SOI_LR_-NAND3X47_P0	C12T28SOI_-LRBR0P6_-NAND3X6_P0	C12T28SOI_-LRBR0P6_-NAND3X12_P0
A (output stable)	3.765e-04	5.000e-04	7.818e-05	2.068e-04
B (output stable)	4.657e-04	6.092e-04	1.042e-04	2.617e-04
C (output stable)	9.714e-04	1.249e-03	2.857e-04	5.360e-04
A to Z	1.437e-02	1.906e-02	2.807e-03	5.452e-03
B to Z	1.240e-02	1.646e-02	2.417e-03	4.415e-03
C to Z	1.078e-02	1.435e-02	1.946e-03	3.473e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	C12T28SOI_-LRBR0P6_-NAND3X24_P0	C12T28SOI_-LRBR0P6_-NAND3X35_P0	C12T28SOI_-LRBR0P6_-NAND3X47_P0
A (output stable)	2.644e-04	3.877e-04	5.365e-04	7.030e-04
B (output stable)	3.245e-04	4.806e-04	6.609e-04	8.732e-04
C (output stable)	6.134e-04	9.653e-04	1.406e-03	1.818e-03
A to Z	7.576e-03	1.032e-02	1.508e-02	1.967e-02
B to Z	6.106e-03	8.370e-03	1.217e-02	1.594e-02
C to Z	4.964e-03	6.631e-03	9.541e-03	1.256e-02
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0			
A (output stable)	3.035e-04			
B (output stable)	3.898e-04			
C (output stable)	7.535e-04			
A to Z	8.142e-03			
B to Z	6.612e-03			
C to Z	5.252e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A (output stable)	9.437e-08	7.804e-08	8.573e-08	6.613e-08
B (output stable)	9.297e-08	8.203e-08	4.957e-08	6.433e-08
C (output stable)	9.827e-08	3.230e-08	-1.017e-08	5.577e-08
A to Z	9.310e-07	1.829e-06	1.983e-06	1.796e-06
B to Z	5.420e-07	3.630e-07	3.390e-07	1.774e-06
C to Z	2.480e-07	-1.700e-08	-1.480e-07	9.800e-08
	C12T28SOI_LR_-NAND3X15_P0	C12T28SOI_LR_-NAND3X18_P0	C12T28SOI_LR_-NAND3X21_P0	C12T28SOI_LR_-NAND3X24_P0
A (output stable)	4.023e-08	3.137e-08	1.533e-09	1.450e-08
B (output stable)	4.500e-09	-9.070e-09	-5.007e-08	-6.750e-08
C (output stable)	1.470e-08	5.667e-10	-7.990e-08	-9.697e-08
A to Z	2.792e-06	3.951e-06	3.726e-06	5.621e-06
B to Z	1.492e-06	3.253e-06	3.818e-06	4.599e-06

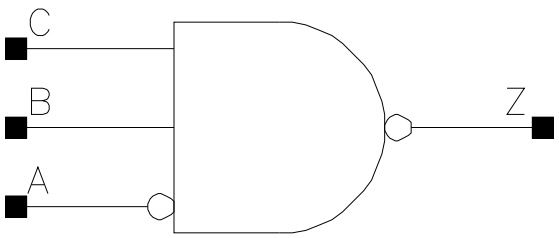
C to Z	5.980e-07	4.570e-07	1.100e-06	6.280e-07
	C12T28SOI_LR_-NAND3X35_P0	C12T28SOI_LR_-NAND3X47_P0	C12T28SOI_-LRBR0P6_-NAND3X6_P0	C12T28SOI_-LRBR0P6_-NAND3X12_P0
A (output stable)	-5.093e-08	-8.240e-08	8.344e-08	5.904e-08
B (output stable)	-1.522e-07	-2.071e-07	4.808e-08	-2.663e-08
C (output stable)	-1.622e-07	-2.445e-07	-1.161e-07	-8.990e-08
A to Z	6.667e-06	8.884e-06	8.490e-07	1.613e-06
B to Z	6.454e-06	7.812e-06	1.482e-06	1.982e-06
C to Z	1.351e-06	-2.327e-06	1.787e-06	1.638e-06
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	C12T28SOI_-LRBR0P6_-NAND3X24_P0	C12T28SOI_-LRBR0P6_-NAND3X35_P0	C12T28SOI_-LRBR0P6_-NAND3X47_P0
A (output stable)	8.027e-08	2.480e-08	2.603e-08	-4.863e-08
B (output stable)	5.590e-08	-1.050e-07	-1.047e-07	-1.708e-07
C (output stable)	5.053e-08	-1.401e-07	-1.426e-07	-2.117e-07
A to Z	1.310e-06	1.701e-06	2.010e-06	4.154e-06
B to Z	2.613e-06	3.256e-06	4.225e-06	4.265e-06
C to Z	-1.260e-07	5.010e-07	2.829e-06	1.906e-06
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0			
A (output stable)	7.350e-08			
B (output stable)	5.300e-08			
C (output stable)	7.830e-08			
A to Z	2.367e-06			
B to Z	2.752e-06			
C to Z	8.510e-07			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.816	0.9792
X12_P0	1.200	1.224	1.4688
X18_P0	1.200	1.496	1.7952
X24_P0	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0008	0.0011	0.0011	0.0020
B	0.0009	0.0017	0.0026	0.0035
C	0.0009	0.0017	0.0025	0.0034

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X12_P0**	**X6_P0**	**X12_P0**
A to Z ↓	0.0230	0.0224	3.3292	1.7940
A to Z ↑	0.0160	0.0156	2.1918	1.1021
B to Z ↓	0.0091	0.0092	3.3717	1.8178
B to Z ↑	0.0110	0.0108	2.2601	1.1409
C to Z ↓	0.0093	0.0088	3.3900	1.8254
C to Z ↑	0.0097	0.0088	2.2721	1.1501
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0256	0.0221	1.2281	0.9336

A to Z ↑	0.0185	0.0150	0.7422	0.5569
B to Z ↓	0.0095	0.0092	1.2419	0.9454
B to Z ↑	0.0108	0.0107	0.7690	0.5785
C to Z ↓	0.0095	0.0089	1.2468	0.9494
C to Z ↑	0.0092	0.0086	0.7743	0.5831

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P0	5.910e-05	1.476e-09
X12_P0	1.155e-04	1.973e-09
X18_P0	1.408e-04	2.304e-09
X24_P0	2.222e-04	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	1.913e-03	3.504e-03	4.428e-03	6.697e-03
B (output stable)	5.427e-05	1.583e-04	2.428e-04	3.473e-04
C (output stable)	9.758e-05	3.803e-04	4.668e-04	6.834e-04
A to Z	4.071e-03	7.889e-03	1.117e-02	1.530e-02
B to Z	2.223e-03	4.275e-03	6.347e-03	8.282e-03
C to Z	2.036e-03	3.696e-03	5.646e-03	7.138e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

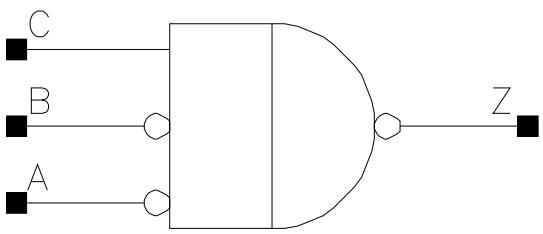
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	2.789e-07	3.642e-07	4.550e-08	-1.511e-07
B (output stable)	9.266e-08	3.681e-08	2.543e-08	-7.413e-08
C (output stable)	8.514e-08	1.533e-08	2.633e-08	-6.160e-08
A to Z	4.460e-07	3.396e-06	3.434e-06	7.160e-06
B to Z	9.350e-07	2.180e-06	3.486e-06	4.724e-06
C to Z	-1.800e-08	-6.180e-07	-3.320e-07	1.589e-06

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	0.816	0.9792
X13_P0	1.200	1.088	1.3056
X20_P0	1.200	1.632	1.9584
X27_P0	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P0	X13_P0	X20_P0	X27_P0
A	0.0010	0.0010	0.0020	0.0018
B	0.0011	0.0011	0.0020	0.0019
C	0.0009	0.0018	0.0026	0.0035

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	**X13_P0**	**X7_P0**	**X13_P0**
A to Z ↓	0.0215	0.0261	2.3519	1.2555
A to Z ↑	0.0135	0.0161	2.1719	1.0941
B to Z ↓	0.0228	0.0277	2.3522	1.2550
B to Z ↑	0.0125	0.0150	2.1702	1.0937
C to Z ↓	0.0058	0.0056	2.4221	1.2870
C to Z ↑	0.0087	0.0080	2.2605	1.1452
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0238	0.0261	0.8560	0.6538
A to Z ↑	0.0147	0.0183	0.7394	0.5554
B to Z ↓	0.0240	0.0266	0.8561	0.6530

B to Z ↑	0.0132	0.0170	0.7375	0.5549
C to Z ↓	0.0064	0.0061	0.8796	0.6702
C to Z ↑	0.0085	0.0082	0.7727	0.5806

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X7_P0	8.754e-05	1.476e-09
X13_P0	1.182e-04	1.807e-09
X20_P0	1.865e-04	2.470e-09
X27_P0	2.081e-04	2.801e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	1.076e-03	1.376e-03	2.356e-03	2.685e-03
B (output stable)	9.959e-04	1.293e-03	2.199e-03	2.544e-03
C (output stable)	4.910e-05	2.876e-04	2.955e-04	3.674e-04
A to Z	4.687e-03	7.585e-03	1.181e-02	1.478e-02
B to Z	4.403e-03	7.273e-03	1.089e-02	1.390e-02
C to Z	1.866e-03	3.503e-03	5.386e-03	7.116e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

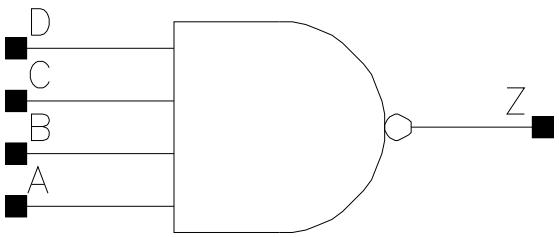
Pin Cycle (vdds)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	6.426e-07	2.648e-07	1.171e-06	5.755e-07
B (output stable)	7.066e-07	3.465e-07	1.368e-06	9.314e-07
C (output stable)	8.057e-08	4.200e-08	7.500e-09	-2.757e-08
A to Z	2.447e-06	3.967e-07	7.741e-06	2.922e-06
B to Z	1.642e-07	2.873e-06	9.760e-07	3.487e-06
C to Z	1.315e-06	6.000e-08	3.425e-06	1.012e-06

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0007	0.0006	0.0008	0.0010
B	0.0007	0.0007	0.0009	0.0011
C	0.0007	0.0007	0.0009	0.0011
D	0.0007	0.0007	0.0009	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0318	0.0321	1.5210	0.7600
A to Z ↑	0.0280	0.0305	2.2283	1.1026
B to Z ↓	0.0330	0.0338	1.5220	0.7598
B to Z ↑	0.0269	0.0299	2.2266	1.1013
C to Z ↓	0.0324	0.0319	1.5217	0.7600
C to Z ↑	0.0289	0.0315	2.2270	1.1013

D to Z ↓	0.0338	0.0332	1.5216	0.7604
D to Z ↑	0.0280	0.0303	2.2271	1.1008
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0335	0.0313	0.5239	0.3919
A to Z ↑	0.0294	0.0291	0.7439	0.5581
B to Z ↓	0.0348	0.0324	0.5238	0.3918
B to Z ↑	0.0284	0.0280	0.7438	0.5580
C to Z ↓	0.0313	0.0292	0.5239	0.3915
C to Z ↑	0.0296	0.0291	0.7430	0.5571
D to Z ↓	0.0326	0.0304	0.5235	0.3917
D to Z ↑	0.0284	0.0280	0.7434	0.5572

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	1.150e-04	1.973e-09
X17_P0	1.755e-04	2.304e-09
X25_P0	2.486e-04	2.801e-09
X33_P0	3.206e-04	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	7.721e-04	9.267e-04	1.332e-03	1.621e-03
B (output stable)	7.291e-04	8.844e-04	1.269e-03	1.540e-03
C (output stable)	7.700e-04	8.903e-04	1.319e-03	1.550e-03
D (output stable)	7.220e-04	8.412e-04	1.246e-03	1.462e-03
A to Z	5.522e-03	8.441e-03	1.280e-02	1.585e-02
B to Z	5.416e-03	8.344e-03	1.263e-02	1.564e-02
C to Z	5.645e-03	8.350e-03	1.217e-02	1.495e-02
D to Z	5.540e-03	8.228e-03	1.200e-02	1.473e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

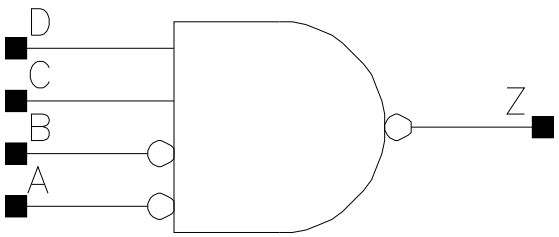
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	2.286e-07	4.162e-07	8.663e-07	9.781e-07
B (output stable)	1.844e-07	4.593e-07	5.607e-07	1.031e-06
C (output stable)	2.629e-07	2.842e-07	5.528e-07	6.241e-07
D (output stable)	1.169e-07	2.474e-07	6.909e-07	4.045e-07
A to Z	9.580e-08	1.264e-06	2.904e-06	3.783e-06
B to Z	-7.060e-08	2.115e-07	2.499e-06	3.214e-06
C to Z	1.930e-07	-2.521e-07	-8.230e-07	-6.550e-07
D to Z	-3.826e-07	-4.660e-07	-9.900e-07	-1.361e-06

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X12_P0	1.200	1.496	1.7952
X18_P0	1.200	2.040	2.4480
X24_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0010	0.0011	0.0020	0.0018
B	0.0010	0.0015	0.0021	0.0019
C	0.0009	0.0018	0.0025	0.0035
D	0.0009	0.0017	0.0025	0.0035

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X12_P0	X6_P0	X12_P0
A to Z ↓	0.0227	0.0300	3.4331	1.7981
A to Z ↑	0.0145	0.0182	2.1741	1.0966
B to Z ↓	0.0237	0.0313	3.4336	1.7986
B to Z ↑	0.0128	0.0170	2.1725	1.0962
C to Z ↓	0.0092	0.0091	3.4757	1.8170
C to Z ↑	0.0111	0.0108	2.3994	1.1404

D to Z ↓	0.0093	0.0087	3.4919	1.8245
D to Z ↑	0.0098	0.0087	2.4123	1.1493
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0261	0.0293	1.2263	0.9340
A to Z ↑	0.0158	0.0210	0.7395	0.5559
B to Z ↓	0.0264	0.0296	1.2259	0.9339
B to Z ↑	0.0142	0.0195	0.7384	0.5552
C to Z ↓	0.0092	0.0096	1.2389	0.9429
C to Z ↑	0.0106	0.0109	0.7724	0.5765
D to Z ↓	0.0091	0.0094	1.2445	0.9470
D to Z ↑	0.0089	0.0089	0.7891	0.5816

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P0	7.086e-05	1.642e-09
X12_P0	9.906e-05	2.304e-09
X18_P0	1.581e-04	2.967e-09
X24_P0	1.676e-04	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	1.245e-03	1.889e-03	2.983e-03	3.456e-03
B (output stable)	1.146e-03	1.775e-03	2.718e-03	3.201e-03
C (output stable)	5.962e-05	1.627e-04	2.357e-04	3.289e-04
D (output stable)	1.117e-04	4.016e-04	4.923e-04	7.492e-04
A to Z	4.867e-03	8.793e-03	1.308e-02	1.715e-02
B to Z	4.624e-03	8.403e-03	1.222e-02	1.622e-02
C to Z	2.155e-03	4.272e-03	6.166e-03	8.561e-03
D to Z	1.971e-03	3.683e-03	5.489e-03	7.465e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

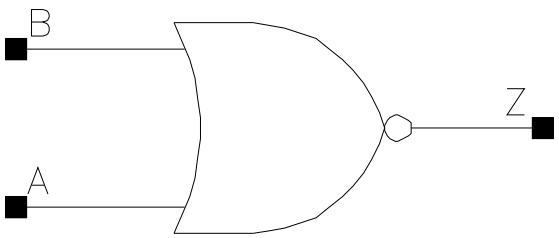
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	9.203e-07	5.326e-07	1.225e-06	5.790e-07
B (output stable)	4.125e-07	5.744e-07	1.200e-06	7.922e-07
C (output stable)	9.387e-08	3.186e-08	-3.629e-09	-7.310e-08
D (output stable)	1.032e-07	2.067e-08	1.400e-08	-1.171e-07
A to Z	3.940e-06	2.397e-06	6.874e-06	2.164e-06
B to Z	7.851e-07	1.400e-07	6.120e-07	1.720e-07
C to Z	6.020e-07	2.301e-06	3.368e-06	4.212e-06
D to Z	2.620e-07	-7.200e-07	-9.510e-07	-5.050e-07

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.408	0.4896
X5_P0	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X10_P0	1.200	0.680	0.8160
X14_P0	1.200	0.680	0.8160
X17_P0	1.200	0.952	1.1424
X21_P0	1.200	0.952	1.1424
X24_P0	1.200	1.224	1.4688
X27_P0	1.200	1.224	1.4688
X34_P0	1.200	1.496	1.7952
X40_P0	1.200	1.360	1.6320
X41_P0	1.200	1.768	2.1216
X49_P0	1.200	1.496	1.7952
X53_P0	1.200	1.904	2.2848
X55_P0	1.200	2.312	2.7744
X57_P0	1.200	1.904	2.2848
X65_P0	1.200	2.040	2.4480
X84_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P0	X5_P0	X7_P0	X10_P0
A	0.0006	0.0007	0.0009	0.0015
B	0.0006	0.0007	0.0009	0.0014
	X14_P0	X17_P0	X21_P0	X24_P0

A	0.0018	0.0024	0.0027	0.0032
B	0.0017	0.0022	0.0026	0.0031
	X27_P0	X34_P0	X40_P0	X41_P0
A	0.0036	0.0045	0.0010	0.0055
B	0.0034	0.0042	0.0011	0.0052
	X49_P0	X53_P0	X55_P0	X57_P0
A	0.0010	0.0011	0.0073	0.0011
B	0.0011	0.0010	0.0069	0.0010
	X65_P0	X84_P0		
A	0.0011	0.0011		
B	0.0010	0.0011		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X5_P0**	**X3_P0**	**X5_P0**
A to Z ↓	0.0049	0.0045	2.9147	2.1478
A to Z ↑	0.0126	0.0117	8.1800	6.0432
B to Z ↓	0.0037	0.0031	2.9892	2.1678
B to Z ↑	0.0136	0.0126	8.2328	6.0704
	X7_P0	**X10_P0**	**X7_P0**	**X10_P0**
A to Z ↓	0.0043	0.0046	1.5961	1.0252
A to Z ↑	0.0111	0.0119	4.3200	2.8736
B to Z ↓	0.0029	0.0024	1.6197	1.0375
B to Z ↑	0.0118	0.0112	4.3424	2.8858
	X14_P0	**X17_P0**	**X14_P0**	**X17_P0**
A to Z ↓	0.0045	0.0045	0.7893	0.6272
A to Z ↑	0.0112	0.0113	2.1543	1.7278
B to Z ↓	0.0024	0.0028	0.7993	0.6341
B to Z ↑	0.0108	0.0114	2.1636	1.7358
	X21_P0	**X24_P0**	**X21_P0**	**X24_P0**
A to Z ↓	0.0046	0.0045	0.5379	0.4569
A to Z ↑	0.0110	0.0111	1.4501	1.2616
B to Z ↓	0.0029	0.0025	0.5436	0.4625
B to Z ↑	0.0111	0.0110	1.4572	1.2676
	X27_P0	**X34_P0**	**X27_P0**	**X34_P0**
A to Z ↓	0.0044	0.0048	0.4077	0.3285
A to Z ↑	0.0107	0.0111	1.1183	0.8894
B to Z ↓	0.0024	0.0029	0.4128	0.3323
B to Z ↑	0.0107	0.0111	1.1239	0.8942
	X40_P0	**X41_P0**	**X40_P0**	**X41_P0**
A to Z ↓	0.0223	0.0046	0.3189	0.2738
A to Z ↑	0.0320	0.0108	0.4566	0.7366
B to Z ↓	0.0212	0.0026	0.3192	0.2772
B to Z ↑	0.0337	0.0107	0.4570	0.7403
	X49_P0	**X53_P0**	**X49_P0**	**X53_P0**
A to Z ↓	0.0232	0.0243	0.2655	0.2425
A to Z ↑	0.0329	0.0371	0.3797	0.3502
B to Z ↓	0.0221	0.0231	0.2652	0.2427
B to Z ↑	0.0346	0.0387	0.3795	0.3507
	X55_P0	**X57_P0**	**X55_P0**	**X57_P0**
A to Z ↓	0.0047	0.0247	0.2070	0.2287
A to Z ↑	0.0108	0.0375	0.5555	0.3265

B to Z ↓	0.0027	0.0235	0.2099	0.2287
B to Z ↑	0.0107	0.0390	0.5586	0.3266
	X65_P0	**X84_P0**	**X65_P0**	**X84_P0**
A to Z ↓	0.0252	0.0265	0.2003	0.1593
A to Z ↑	0.0379	0.0387	0.2859	0.2274
B to Z ↓	0.0240	0.0253	0.2002	0.1594
B to Z ↑	0.0395	0.0403	0.2858	0.2275

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P0	2.587e-05	9.792e-10
X5_P0	3.523e-05	9.792e-10
X7_P0	4.702e-05	9.792e-10
X10_P0	7.023e-05	1.310e-09
X14_P0	8.851e-05	1.310e-09
X17_P0	1.140e-04	1.642e-09
X21_P0	1.271e-04	1.642e-09
X24_P0	1.571e-04	1.973e-09
X27_P0	1.657e-04	1.973e-09
X34_P0	2.044e-04	2.304e-09
X40_P0	3.254e-04	2.139e-09
X41_P0	2.431e-04	2.635e-09
X49_P0	3.637e-04	2.304e-09
X53_P0	4.388e-04	2.801e-09
X55_P0	3.204e-04	3.298e-09
X57_P0	4.592e-04	2.801e-09
X65_P0	4.977e-04	2.967e-09
X84_P0	5.480e-04	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	3.149e-05	4.193e-05	5.702e-05	1.622e-04
B (output stable)	4.809e-05	6.306e-05	8.710e-05	3.527e-04
A to Z	1.158e-03	1.469e-03	1.977e-03	3.190e-03
B to Z	9.997e-04	1.264e-03	1.675e-03	2.487e-03
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	1.915e-04	2.327e-04	2.603e-04	3.167e-04
B (output stable)	4.076e-04	4.438e-04	4.622e-04	6.105e-04
A to Z	4.044e-03	5.133e-03	5.934e-03	7.001e-03
B to Z	3.202e-03	4.187e-03	4.853e-03	5.643e-03
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	3.440e-04	4.201e-04	5.727e-05	5.441e-04
B (output stable)	6.234e-04	7.090e-04	8.718e-05	1.011e-03
A to Z	7.651e-03	9.759e-03	1.555e-02	1.161e-02
B to Z	6.160e-03	7.967e-03	1.531e-02	9.284e-03
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	5.777e-05	5.945e-05	6.914e-04	5.959e-05
B (output stable)	8.700e-05	9.318e-05	1.210e-03	9.400e-05
A to Z	1.766e-02	2.162e-02	1.528e-02	2.265e-02
B to Z	1.742e-02	2.136e-02	1.229e-02	2.238e-02
	X65_P0	X84_P0		

A (output stable)	5.977e-05	6.309e-05		
B (output stable)	9.218e-05	9.436e-05		
A to Z	2.451e-02	2.964e-02		
B to Z	2.425e-02	2.933e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

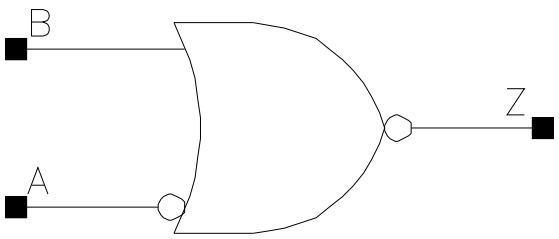
Pin Cycle (vdds)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	1.825e-07	2.271e-07	2.910e-07	7.260e-07
B (output stable)	3.407e-07	3.969e-07	4.778e-07	1.412e-06
A to Z	3.002e-07	1.068e-06	1.179e-06	1.777e-06
B to Z	3.452e-07	5.513e-07	8.173e-07	2.448e-07
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	8.058e-07	5.957e-07	5.403e-07	9.683e-07
B (output stable)	1.666e-06	1.478e-06	1.603e-06	2.528e-06
A to Z	2.095e-06	2.095e-06	2.388e-06	3.383e-06
B to Z	-5.120e-07	-6.080e-07	-5.310e-07	-8.840e-07
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	9.218e-07	8.266e-07	2.975e-07	1.421e-06
B (output stable)	2.321e-06	2.403e-06	4.935e-07	3.686e-06
A to Z	2.525e-06	3.610e-06	1.275e-06	4.883e-06
B to Z	-1.039e-06	-9.320e-07	-1.310e-07	-1.752e-06
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	2.990e-07	2.992e-07	1.937e-06	2.993e-07
B (output stable)	4.861e-07	4.979e-07	4.117e-06	4.986e-07
A to Z	1.136e-06	8.090e-07	5.200e-06	6.680e-07
B to Z	-1.760e-07	1.006e-06	-2.064e-06	8.200e-07
	X65_P0	X84_P0		
A (output stable)	3.003e-07	2.950e-07		
B (output stable)	4.993e-07	5.214e-07		
A to Z	5.760e-07	5.680e-07		
B to Z	7.890e-07	6.400e-07		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X7_P0	1.200	0.680	0.8160
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X41_P0	1.200	2.312	2.7744
X55_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X7_P0	X13_P0
A	0.0008	0.0008	0.0008	0.0011
B	0.0006	0.0009	0.0009	0.0017
	X27_P0	X41_P0	X55_P0	
A	0.0021	0.0030	0.0040	
B	0.0034	0.0051	0.0068	

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0183	0.0202	2.7179	1.8283
A to Z ↑	0.0159	0.0162	8.0878	4.2847
B to Z ↓	0.0039	0.0042	2.9612	1.9797
B to Z ↑	0.0137	0.0114	8.2142	4.3590

	X7_P0	X13_P0	X7_P0	X13_P0
A to Z ↓	0.0203	0.0187	1.4736	0.7974
A to Z ↑	0.0178	0.0171	4.2636	2.2719
B to Z ↓	0.0031	0.0026	1.5550	0.8402
B to Z ↑	0.0125	0.0116	4.3161	2.3033
	X27_P0	**X41_P0**	**X27_P0**	**X41_P0**
A to Z ↓	0.0182	0.0184	0.3821	0.2586
A to Z ↑	0.0164	0.0166	1.0878	0.7312
B to Z ↓	0.0026	0.0027	0.4154	0.2794
B to Z ↑	0.0111	0.0109	1.1037	0.7415
	X55_P0		**X55_P0**	
A to Z ↓	0.0183		0.1958	
A to Z ↑	0.0164		0.5524	
B to Z ↓	0.0027		0.2117	
B to Z ↑	0.0109		0.5602	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P0	4.906e-05	1.145e-09
X6_P0	6.715e-05	1.145e-09
X7_P0	7.736e-05	1.310e-09
X13_P0	1.375e-04	1.642e-09
X27_P0	2.554e-04	2.470e-09
X41_P0	3.707e-04	3.298e-09
X55_P0	4.859e-04	4.126e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	1.648e-03	1.941e-03	2.049e-03	3.392e-03
B (output stable)	4.782e-05	8.641e-05	1.909e-04	3.631e-04
A to Z	2.615e-03	3.478e-03	3.957e-03	6.757e-03
B to Z	1.007e-03	1.598e-03	1.840e-03	3.276e-03
	X27_P0	X41_P0	X55_P0	
A (output stable)	6.738e-03	1.007e-02	1.330e-02	
B (output stable)	7.147e-04	1.013e-03	1.257e-03	
A to Z	1.346e-02	1.999e-02	2.638e-02	
B to Z	6.473e-03	9.531e-03	1.257e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

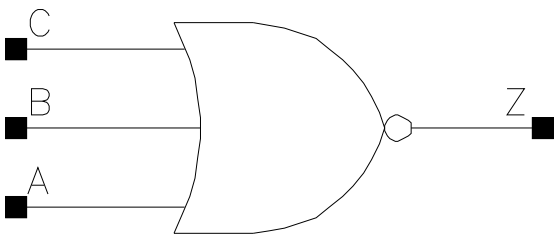
Pin Cycle (vdds)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	4.705e-07	8.468e-07	8.870e-07	2.057e-06
B (output stable)	3.495e-07	4.940e-07	9.080e-07	1.610e-06
A to Z	4.658e-07	2.400e-07	3.270e-07	6.170e-07
B to Z	3.350e-07	1.203e-07	1.067e-06	1.659e-07
	X27_P0	X41_P0	X55_P0	
A (output stable)	3.551e-06	4.496e-06	5.386e-06	
B (output stable)	2.771e-06	3.546e-06	4.177e-06	
A to Z	1.391e-06	1.652e-06	1.883e-06	
B to Z	-9.910e-07	-1.758e-06	-2.146e-06	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X9_P0	1.200	0.952	1.1424
X13_P0	1.200	0.952	1.1424
X16_P0	1.200	1.360	1.6320
X19_P0	1.200	1.496	1.7952
X22_P0	1.200	1.768	2.1216
X25_P0	1.200	1.904	2.2848
X37_P0	1.200	2.584	3.1008
X49_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P0	X6_P0	X9_P0	X13_P0
A	0.0007	0.0009	0.0014	0.0017
B	0.0007	0.0009	0.0016	0.0019
C	0.0007	0.0009	0.0013	0.0017
	X16_P0	X19_P0	X22_P0	X25_P0
A	0.0023	0.0027	0.0032	0.0036
B	0.0024	0.0031	0.0033	0.0041
C	0.0022	0.0025	0.0030	0.0033
	X37_P0	X49_P0		
A	0.0053	0.0072		
B	0.0055	0.0072		

C	0.0049	0.0067		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0060	0.0056	2.1791	1.6202
A to Z ↑	0.0167	0.0154	8.9834	6.4310
B to Z ↓	0.0053	0.0049	2.1874	1.6253
B to Z ↑	0.0168	0.0154	8.9939	6.4395
C to Z ↓	0.0041	0.0036	2.2072	1.6443
C to Z ↑	0.0170	0.0154	9.0064	6.4474
	X9_P0	**X13_P0**	**X9_P0**	**X13_P0**
A to Z ↓	0.0059	0.0057	1.0551	0.8190
A to Z ↑	0.0166	0.0155	4.2462	3.2064
B to Z ↓	0.0051	0.0047	1.0319	0.7885
B to Z ↑	0.0168	0.0154	4.2571	3.2135
C to Z ↓	0.0031	0.0028	1.0444	0.8047
C to Z ↑	0.0145	0.0136	4.2524	3.2117
	X16_P0	**X19_P0**	**X16_P0**	**X19_P0**
A to Z ↓	0.0058	0.0057	0.6313	0.5391
A to Z ↑	0.0161	0.0159	2.5752	2.1475
B to Z ↓	0.0052	0.0051	0.6341	0.5296
B to Z ↑	0.0162	0.0162	2.5799	2.1525
C to Z ↓	0.0033	0.0033	0.6392	0.5505
C to Z ↑	0.0150	0.0143	2.5799	2.1520
	X22_P0	**X25_P0**	**X22_P0**	**X25_P0**
A to Z ↓	0.0058	0.0057	0.4658	0.4104
A to Z ↑	0.0158	0.0157	1.8430	1.6161
B to Z ↓	0.0051	0.0049	0.4590	0.3969
B to Z ↑	0.0158	0.0160	1.8471	1.6199
C to Z ↓	0.0030	0.0030	0.4652	0.4123
C to Z ↑	0.0141	0.0136	1.8468	1.6191
	X37_P0	**X49_P0**	**X37_P0**	**X49_P0**
A to Z ↓	0.0058	0.0059	0.2817	0.2133
A to Z ↑	0.0153	0.0153	1.0843	0.8171
B to Z ↓	0.0051	0.0051	0.2794	0.2117
B to Z ↑	0.0152	0.0151	1.0866	0.8188
C to Z ↓	0.0034	0.0034	0.2832	0.2146
C to Z ↑	0.0138	0.0139	1.0864	0.8190

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.655e-05	1.145e-09
X6_P0	3.597e-05	1.145e-09
X9_P0	5.389e-05	1.642e-09
X13_P0	6.916e-05	1.642e-09
X16_P0	8.749e-05	2.139e-09
X19_P0	1.043e-04	2.304e-09
X22_P0	1.216e-04	2.635e-09
X25_P0	1.362e-04	2.801e-09
X37_P0	1.978e-04	3.629e-09

X49_P0	2.620e-04	4.623e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	4.561e-05	6.251e-05	1.150e-04	1.494e-04
B (output stable)	5.175e-05	7.129e-05	1.567e-04	1.892e-04
C (output stable)	1.090e-04	1.535e-04	4.124e-04	5.061e-04
A to Z	1.821e-03	2.362e-03	3.827e-03	4.753e-03
B to Z	1.570e-03	2.020e-03	3.328e-03	4.088e-03
C to Z	1.374e-03	1.735e-03	2.583e-03	3.197e-03
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	1.782e-04	2.149e-04	2.567e-04	2.976e-04
B (output stable)	2.379e-04	3.122e-04	3.484e-04	4.262e-04
C (output stable)	5.555e-04	7.237e-04	8.447e-04	1.011e-03
A to Z	6.165e-03	7.307e-03	8.460e-03	9.614e-03
B to Z	5.303e-03	6.349e-03	7.290e-03	8.351e-03
C to Z	4.368e-03	4.994e-03	5.821e-03	6.390e-03
	X37_P0	X49_P0		
A (output stable)	4.307e-04	5.721e-04		
B (output stable)	5.658e-04	7.428e-04		
C (output stable)	1.357e-03	1.792e-03		
A to Z	1.400e-02	1.862e-02		
B to Z	1.197e-02	1.589e-02		
C to Z	9.494e-03	1.261e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

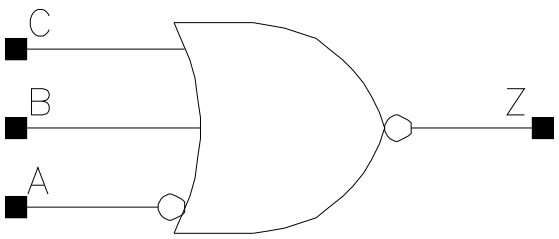
Pin Cycle (vdds)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	2.502e-07	3.078e-07	6.139e-07	7.555e-07
B (output stable)	6.399e-07	7.893e-07	2.543e-06	2.634e-06
C (output stable)	8.198e-07	8.417e-07	2.432e-05	2.175e-05
A to Z	6.660e-07	2.792e-06	3.484e-06	4.075e-06
B to Z	4.590e-07	1.781e-06	2.162e-06	1.912e-06
C to Z	6.247e-07	2.202e-07	7.930e-08	-1.517e-07
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	7.942e-07	8.898e-07	1.106e-06	1.307e-06
B (output stable)	2.151e-06	3.274e-06	3.816e-06	5.123e-06
C (output stable)	1.179e-05	1.993e-05	2.724e-05	3.930e-05
A to Z	5.387e-06	6.190e-06	7.720e-06	8.307e-06
B to Z	2.354e-06	3.053e-06	3.956e-06	4.214e-06
C to Z	1.300e-07	-2.980e-07	-3.900e-08	5.920e-07
	X37_P0	X49_P0		
A (output stable)	1.867e-06	2.391e-06		
B (output stable)	5.796e-06	7.485e-06		
C (output stable)	3.415e-05	4.189e-05		
A to Z	1.101e-05	1.529e-05		
B to Z	4.751e-06	5.636e-06		
C to Z	-1.416e-06	-1.821e-06		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.680	0.8160
X13_P0	1.200	1.224	1.4688
X19_P0	1.200	1.496	1.7952
X25_P0	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0008	0.0011	0.0011	0.0021
B	0.0009	0.0018	0.0027	0.0036
C	0.0009	0.0017	0.0025	0.0033

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X13_P0**	**X6_P0**	**X13_P0**
A to Z ↓	0.0203	0.0200	1.5278	0.8438
A to Z ↑	0.0217	0.0216	6.4902	3.1987
B to Z ↓	0.0051	0.0048	1.6306	0.7925
B to Z ↑	0.0156	0.0155	6.5211	3.2133
C to Z ↓	0.0037	0.0028	1.6440	0.8050
C to Z ↑	0.0156	0.0137	6.5283	3.2118
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0224	0.0198	0.5163	0.3921

A to Z ↑	0.0238	0.0216	2.1553	1.6174
B to Z ↓	0.0052	0.0050	0.5491	0.4102
B to Z ↑	0.0153	0.0152	2.1668	1.6261
C to Z ↓	0.0033	0.0030	0.5512	0.4146
C to Z ↑	0.0144	0.0137	2.1673	1.6260

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P0	6.002e-05	1.310e-09
X13_P0	1.201e-04	1.973e-09
X19_P0	1.457e-04	2.304e-09
X25_P0	2.253e-04	3.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	1.989e-03	3.639e-03	4.449e-03	7.063e-03
B (output stable)	7.218e-05	1.925e-04	2.739e-04	3.777e-04
C (output stable)	1.516e-04	5.278e-04	6.401e-04	9.430e-04
A to Z	4.152e-03	8.226e-03	1.111e-02	1.588e-02
B to Z	2.023e-03	4.132e-03	6.037e-03	8.035e-03
C to Z	1.748e-03	3.228e-03	4.972e-03	6.372e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

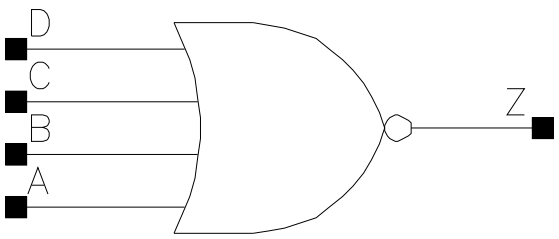
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	5.708e-07	2.178e-06	1.987e-06	3.335e-06
B (output stable)	7.921e-07	2.533e-06	2.591e-06	3.655e-06
C (output stable)	8.254e-07	2.144e-05	9.722e-06	2.592e-05
A to Z	6.070e-07	4.083e-06	2.618e-06	6.963e-06
B to Z	1.829e-06	1.888e-06	3.294e-06	3.250e-06
C to Z	2.555e-07	-1.231e-07	-3.280e-07	6.000e-07

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	1.904	2.2848
X32_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X32_P0
A	0.0007	0.0007	0.0008	0.0009
B	0.0007	0.0007	0.0009	0.0012
C	0.0006	0.0006	0.0008	0.0010
D	0.0007	0.0007	0.0009	0.0010

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0223	0.0225	1.4975	0.7368
A to Z ↑	0.0342	0.0367	2.2533	1.1164
B to Z ↓	0.0210	0.0215	1.4963	0.7366
B to Z ↑	0.0355	0.0384	2.2542	1.1171
C to Z ↓	0.0219	0.0226	1.4931	0.7352
C to Z ↑	0.0353	0.0383	2.2494	1.1170

D to Z ↓	0.0213	0.0219	1.4945	0.7354
D to Z ↑	0.0368	0.0403	2.2505	1.1172
	X25_P0	**X32_P0**	**X25_P0**	**X32_P0**
A to Z ↓	0.0233	0.0253	0.5127	0.4011
A to Z ↑	0.0366	0.0356	0.7664	0.5791
B to Z ↓	0.0223	0.0242	0.5127	0.4014
B to Z ↑	0.0383	0.0370	0.7659	0.5784
C to Z ↓	0.0225	0.0249	0.5099	0.3999
C to Z ↑	0.0366	0.0362	0.7659	0.5780
D to Z ↓	0.0214	0.0233	0.5101	0.4000
D to Z ↑	0.0382	0.0375	0.7648	0.5785

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	9.998e-05	1.973e-09
X17_P0	1.490e-04	2.139e-09
X25_P0	2.231e-04	2.801e-09
X32_P0	2.817e-04	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	7.626e-04	8.955e-04	1.261e-03	1.592e-03
B (output stable)	7.025e-04	8.332e-04	1.179e-03	1.475e-03
C (output stable)	7.272e-04	8.260e-04	1.237e-03	1.557e-03
D (output stable)	6.659e-04	7.685e-04	1.154e-03	1.444e-03
A to Z	5.105e-03	7.932e-03	1.201e-02	1.516e-02
B to Z	4.949e-03	7.782e-03	1.180e-02	1.490e-02
C to Z	5.180e-03	7.978e-03	1.147e-02	1.458e-02
D to Z	5.010e-03	7.829e-03	1.126e-02	1.429e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

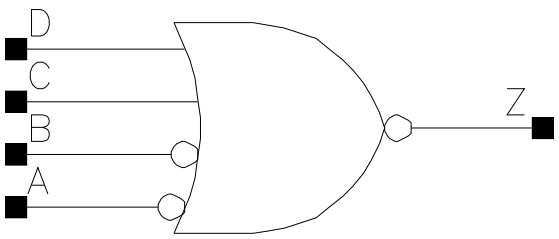
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	3.305e-07	1.842e-07	2.638e-07	2.588e-07
B (output stable)	4.719e-07	2.454e-07	2.744e-07	2.755e-07
C (output stable)	5.029e-07	3.416e-07	4.406e-07	2.972e-07
D (output stable)	5.067e-07	3.359e-07	4.703e-07	3.840e-07
A to Z	1.169e-06	2.954e-07	1.558e-06	1.037e-06
B to Z	9.767e-07	1.136e-06	1.531e-06	1.033e-06
C to Z	1.164e-06	1.295e-07	1.373e-06	9.200e-08
D to Z	8.975e-07	9.336e-07	1.781e-06	1.089e-06

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X13_P0	1.200	1.496	1.7952
X19_P0	1.200	2.040	2.4480
X25_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0010	0.0011	0.0020	0.0020
B	0.0011	0.0015	0.0020	0.0021
C	0.0009	0.0018	0.0026	0.0034
D	0.0009	0.0017	0.0025	0.0033

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X13_P0	X6_P0	X13_P0
A to Z ↓	0.0180	0.0221	1.4863	0.7482
A to Z ↑	0.0217	0.0268	6.2620	3.2568
B to Z ↓	0.0167	0.0212	1.4852	0.7478
B to Z ↑	0.0224	0.0281	6.2618	3.2569
C to Z ↓	0.0055	0.0049	1.6493	0.7942
C to Z ↑	0.0157	0.0159	6.2976	3.2739

D to Z ↓	0.0039	0.0030	1.6545	0.8030
D to Z ↑	0.0155	0.0141	6.3011	3.2718
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0196	0.0214	0.5114	0.3857
A to Z ↑	0.0241	0.0262	2.1582	1.6332
B to Z ↓	0.0179	0.0199	0.5108	0.3852
B to Z ↑	0.0248	0.0272	2.1581	1.6334
C to Z ↓	0.0053	0.0051	0.5498	0.4120
C to Z ↑	0.0153	0.0153	2.1688	1.6407
D to Z ↓	0.0033	0.0031	0.5517	0.4144
D to Z ↑	0.0144	0.0137	2.1688	1.6405

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P0	6.982e-05	1.642e-09
X13_P0	9.593e-05	2.304e-09
X19_P0	1.551e-04	2.967e-09
X25_P0	1.760e-04	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	1.253e-03	1.878e-03	2.983e-03	3.483e-03
B (output stable)	1.175e-03	1.785e-03	2.773e-03	3.319e-03
C (output stable)	8.008e-05	2.190e-04	3.145e-04	4.250e-04
D (output stable)	1.806e-04	5.581e-04	7.266e-04	1.051e-03
A to Z	5.076e-03	9.002e-03	1.364e-02	1.726e-02
B to Z	4.899e-03	8.676e-03	1.297e-02	1.665e-02
C to Z	2.089e-03	4.148e-03	5.997e-03	7.913e-03
D to Z	1.812e-03	3.298e-03	4.965e-03	6.323e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

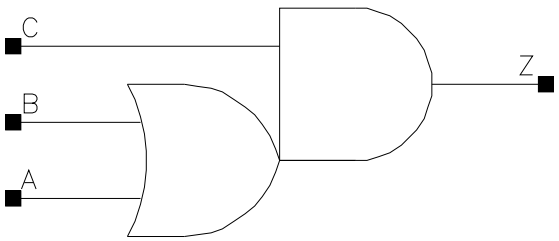
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	3.422e-07	1.111e-06	1.159e-06	2.242e-06
B (output stable)	4.372e-07	9.387e-07	1.273e-06	1.219e-06
C (output stable)	9.494e-07	3.480e-06	3.882e-06	6.533e-06
D (output stable)	9.882e-07	2.451e-05	1.501e-05	3.864e-05
A to Z	7.990e-07	5.051e-06	8.360e-06	8.732e-06
B to Z	-7.250e-07	4.418e-06	-3.200e-08	1.810e-06
C to Z	6.790e-07	1.832e-06	2.831e-06	3.150e-06
D to Z	1.785e-07	-3.097e-07	3.310e-07	-1.063e-06

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0010	0.0010	0.0019
B	0.0011	0.0011	0.0021
C	0.0011	0.0011	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0193	0.0226	1.5408	0.7695
A to Z ↑	0.0163	0.0185	2.2722	1.1207
B to Z ↓	0.0203	0.0240	1.5435	0.7683
B to Z ↑	0.0143	0.0169	2.2685	1.1196
C to Z ↓	0.0179	0.0199	1.5268	0.7582
C to Z ↑	0.0148	0.0168	2.2706	1.1200
	X33_P0		**X33_P0**	
A to Z ↓	0.0235		0.3897	
A to Z ↑	0.0201		0.5620	

B to Z ↓	0.0248		0.3898	
B to Z ↑	0.0180		0.5608	
C to Z ↓	0.0205		0.3840	
C to Z ↑	0.0177		0.5610	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	9.417e-05	1.310e-09
X17_P0	1.363e-04	1.476e-09
X33_P0	2.668e-04	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	8.680e-05	8.709e-05	1.830e-04
B (output stable)	9.964e-05	1.005e-04	2.027e-04
C (output stable)	1.001e-04	1.033e-04	2.006e-04
A to Z	4.157e-03	6.491e-03	1.351e-02
B to Z	3.838e-03	6.183e-03	1.291e-02
C to Z	4.437e-03	6.529e-03	1.356e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

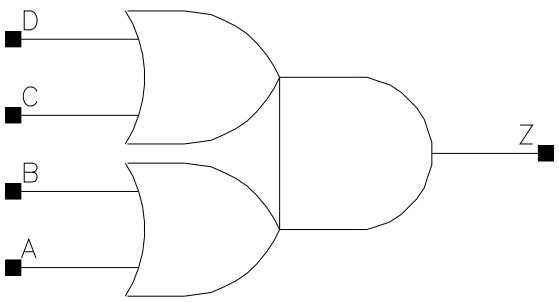
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	1.255e-07	1.295e-07	1.273e-07
B (output stable)	2.471e-07	2.427e-07	3.709e-07
C (output stable)	8.684e-08	8.703e-08	8.871e-08
A to Z	-1.105e-07	3.179e-07	2.900e-07
B to Z	2.110e-06	7.053e-07	1.348e-07
C to Z	1.882e-06	8.934e-07	1.061e-06

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0010	0.0020
B	0.0007	0.0011	0.0020
C	0.0007	0.0010	0.0020
D	0.0007	0.0010	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0317	0.0279	1.5055	0.7650
A to Z ↑	0.0217	0.0196	2.2266	1.1159
B to Z ↓	0.0337	0.0296	1.5052	0.7650
B to Z ↑	0.0207	0.0185	2.2245	1.1135

C to Z ↓	0.0277	0.0248	1.4924	0.7607
C to Z ↑	0.0215	0.0202	2.2250	1.1149
D to Z ↓	0.0290	0.0260	1.4921	0.7608
D to Z ↑	0.0200	0.0183	2.2207	1.1123
	X33_P0		**X33_P0**	
A to Z ↓	0.0283		0.3930	
A to Z ↑	0.0198		0.5608	
B to Z ↓	0.0289		0.3930	
B to Z ↑	0.0181		0.5596	
C to Z ↓	0.0246		0.3901	
C to Z ↑	0.0198		0.5598	
D to Z ↓	0.0250		0.3901	
D to Z ↑	0.0179		0.5590	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	8.441e-05	1.642e-09
X17_P0	1.605e-04	1.807e-09
X33_P0	3.014e-04	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	3.672e-05	5.928e-05	1.657e-04
B (output stable)	4.522e-05	7.571e-05	3.169e-04
C (output stable)	7.699e-05	1.076e-04	2.555e-04
D (output stable)	8.689e-05	1.255e-04	4.086e-04
A to Z	4.761e-03	8.067e-03	1.578e-02
B to Z	4.593e-03	7.745e-03	1.485e-02
C to Z	4.238e-03	7.365e-03	1.423e-02
D to Z	4.070e-03	7.039e-03	1.334e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

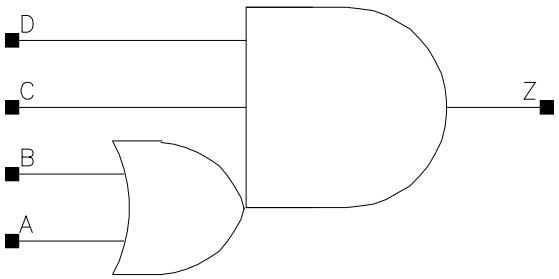
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	1.557e-07	2.354e-07	6.587e-07
B (output stable)	2.638e-07	3.979e-07	1.095e-06
C (output stable)	1.293e-07	2.008e-07	5.014e-07
D (output stable)	2.318e-07	3.469e-07	9.456e-07
A to Z	2.737e-09	1.771e-07	6.427e-07
B to Z	5.805e-08	3.156e-07	9.466e-07
C to Z	2.437e-07	1.287e-07	6.997e-07
D to Z	6.979e-08	-2.920e-09	1.046e-06

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	1.088	1.3056
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0007	0.0010	0.0017	0.0020
B	0.0007	0.0011	0.0017	0.0021
C	0.0007	0.0010	0.0017	0.0020
D	0.0007	0.0011	0.0017	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0269	0.0257	1.5753	0.7685
A to Z ↑	0.0258	0.0247	2.2968	1.1152
B to Z ↓	0.0285	0.0265	1.5749	0.7685
B to Z ↑	0.0244	0.0224	2.2955	1.1135
C to Z ↓	0.0234	0.0220	1.5423	0.7553

C to Z ↑	0.0231	0.0219	2.2948	1.1131
D to Z ↓	0.0226	0.0212	1.5422	0.7548
D to Z ↑	0.0248	0.0233	2.2955	1.1131
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0267	0.0260	0.5239	0.3920
A to Z ↑	0.0253	0.0262	0.7573	0.5679
B to Z ↓	0.0274	0.0266	0.5239	0.3921
B to Z ↑	0.0231	0.0237	0.7562	0.5668
C to Z ↓	0.0230	0.0223	0.5152	0.3854
C to Z ↑	0.0224	0.0227	0.7563	0.5666
D to Z ↓	0.0218	0.0213	0.5142	0.3849
D to Z ↑	0.0233	0.0238	0.7570	0.5667

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	6.087e-05	1.476e-09
X17_P0	1.224e-04	1.807e-09
X25_P0	1.890e-04	2.801e-09
X33_P0	2.382e-04	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	6.513e-05	1.238e-04	2.083e-04	2.327e-04
B (output stable)	6.936e-05	1.396e-04	2.431e-04	2.682e-04
C (output stable)	3.034e-05	5.959e-05	1.412e-04	1.552e-04
D (output stable)	3.607e-05	6.905e-05	1.989e-04	2.186e-04
A to Z	4.117e-03	7.546e-03	1.203e-02	1.525e-02
B to Z	3.960e-03	7.108e-03	1.130e-02	1.430e-02
C to Z	4.252e-03	7.684e-03	1.249e-02	1.554e-02
D to Z	4.115e-03	7.427e-03	1.183e-02	1.484e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

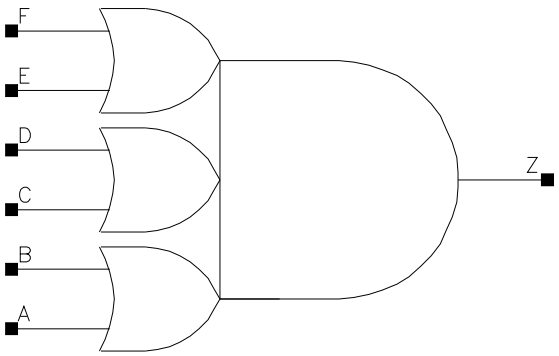
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	-1.864e-09	6.360e-08	1.117e-07	2.002e-07
B (output stable)	5.747e-08	1.885e-07	3.031e-07	4.211e-07
C (output stable)	9.927e-08	8.687e-08	9.086e-08	6.842e-08
D (output stable)	9.582e-08	8.061e-08	5.320e-08	7.018e-08
A to Z	-1.166e-07	2.080e-07	2.600e-07	2.030e-07
B to Z	-4.430e-09	-3.560e-08	-1.487e-07	-2.330e-07
C to Z	1.913e-07	2.972e-07	6.860e-07	4.857e-07
D to Z	-1.237e-07	1.067e-09	-5.467e-09	-1.217e-07

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0007	0.0010	0.0017
B	0.0007	0.0010	0.0020
C	0.0007	0.0010	0.0018
D	0.0007	0.0010	0.0020
E	0.0007	0.0010	0.0018
F	0.0007	0.0010	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0363	0.0315	1.6095	0.7811
A to Z ↑	0.0271	0.0252	2.2809	1.1277
B to Z ↓	0.0382	0.0334	1.6098	0.7813
B to Z ↑	0.0261	0.0243	2.2805	1.1277
C to Z ↓	0.0332	0.0300	1.5985	0.7795
C to Z ↑	0.0282	0.0259	2.2808	1.1277
D to Z ↓	0.0352	0.0316	1.5991	0.7794
D to Z ↑	0.0268	0.0245	2.2791	1.1270
E to Z ↓	0.0288	0.0263	1.5846	0.7740
E to Z ↑	0.0267	0.0251	2.2780	1.1266
F to Z ↓	0.0307	0.0277	1.5842	0.7742
F to Z ↑	0.0253	0.0235	2.2749	1.1248
	X33_P0		X33_P0	
A to Z ↓	0.0322		0.3996	
A to Z ↑	0.0264		0.5682	
B to Z ↓	0.0342		0.3995	
B to Z ↑	0.0244		0.5671	
C to Z ↓	0.0298		0.3972	
C to Z ↑	0.0269		0.5682	
D to Z ↓	0.0315		0.3972	
D to Z ↑	0.0251		0.5667	
E to Z ↓	0.0262		0.3945	
E to Z ↑	0.0262		0.5673	
F to Z ↓	0.0278		0.3946	
F to Z ↑	0.0241		0.5661	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	8.244e-05	1.973e-09
X17_P0	1.597e-04	2.139e-09
X33_P0	3.034e-04	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	3.486e-05	5.902e-05	1.110e-04
B (output stable)	4.099e-05	7.521e-05	1.359e-04
C (output stable)	4.810e-05	7.875e-05	1.567e-04
D (output stable)	5.554e-05	9.203e-05	1.817e-04
E (output stable)	1.137e-04	1.669e-04	3.163e-04
F (output stable)	1.169e-04	1.764e-04	3.398e-04
A to Z	5.459e-03	9.310e-03	1.870e-02
B to Z	5.276e-03	9.004e-03	1.801e-02
C to Z	5.025e-03	8.740e-03	1.736e-02
D to Z	4.851e-03	8.421e-03	1.668e-02
E to Z	4.481e-03	7.937e-03	1.582e-02
F to Z	4.327e-03	7.621e-03	1.520e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

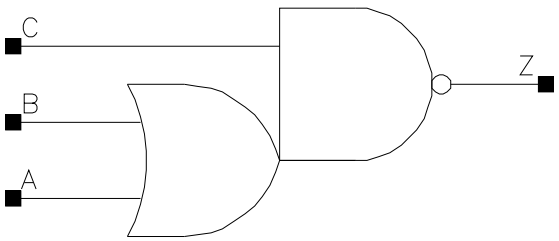
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	1.436e-07	1.970e-07	2.545e-07
B (output stable)	2.367e-07	3.203e-07	4.926e-07
C (output stable)	1.084e-07	1.533e-07	1.530e-07
D (output stable)	1.986e-07	2.766e-07	3.934e-07
E (output stable)	6.497e-08	1.147e-07	9.759e-08
F (output stable)	1.630e-07	2.600e-07	3.548e-07
A to Z	2.055e-07	1.610e-07	-1.863e-07
B to Z	6.703e-08	-2.392e-07	-1.803e-07
C to Z	1.234e-08	-1.203e-07	-2.203e-07
D to Z	-1.402e-07	-2.313e-07	-4.384e-07
E to Z	2.410e-07	2.391e-07	2.624e-07
F to Z	-2.380e-08	3.667e-08	-1.694e-07

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X34_P0	1.200	2.720	3.2640
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X34_P0	X46_P0
A	0.0008	0.0026	0.0053	0.0069
B	0.0009	0.0025	0.0050	0.0066
C	0.0009	0.0028	0.0057	0.0074

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0082	0.0085	2.7304	0.8937
A to Z ↑	0.0116	0.0122	4.3167	1.4774
B to Z ↓	0.0062	0.0065	2.6681	0.8974
B to Z ↑	0.0122	0.0122	4.3430	1.4863
C to Z ↓	0.0072	0.0072	2.4705	0.8166
C to Z ↑	0.0117	0.0116	2.3166	0.7723
	X34_P0	**X46_P0**	**X34_P0**	**X46_P0**
A to Z ↓	0.0090	0.0090	0.4558	0.3486

A to Z ↑	0.0125	0.0124	0.7381	0.5685
B to Z ↓	0.0069	0.0069	0.4630	0.3555
B to Z ↑	0.0124	0.0125	0.7424	0.5720
C to Z ↓	0.0076	0.0075	0.4191	0.3210
C to Z ↑	0.0118	0.0118	0.3866	0.2962

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P0	5.387e-05	1.145e-09
X17_P0	1.503e-04	2.139e-09
X34_P0	2.962e-04	3.795e-09
X46_P0	3.890e-04	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	7.812e-05	2.746e-04	5.712e-04	7.107e-04
B (output stable)	9.154e-05	3.423e-04	7.426e-04	8.705e-04
C (output stable)	9.112e-05	2.955e-04	6.244e-04	7.864e-04
A to Z	2.015e-03	6.275e-03	1.284e-02	1.668e-02
B to Z	1.724e-03	5.127e-03	1.046e-02	1.367e-02
C to Z	2.380e-03	7.270e-03	1.487e-02	1.934e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

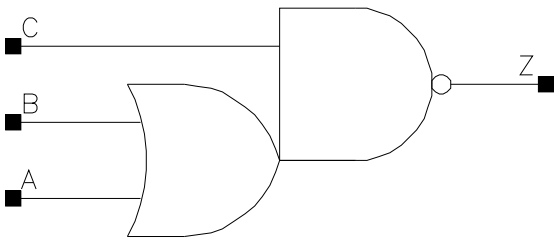
Pin Cycle (vdds)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	1.346e-07	1.699e-07	3.944e-07	2.587e-07
B (output stable)	2.548e-07	6.488e-07	1.446e-06	1.621e-06
C (output stable)	7.879e-08	2.580e-08	-1.015e-07	-9.500e-08
A to Z	8.780e-07	7.150e-07	2.671e-06	1.400e-06
B to Z	1.149e-06	3.431e-06	6.273e-06	8.688e-06
C to Z	1.384e-06	2.221e-06	2.830e-06	5.791e-06

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.544	0.6528
X11_P0	1.200	0.952	1.1424
X17_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X17_P0	X23_P0
A	0.0009	0.0017	0.0026	0.0037
B	0.0008	0.0018	0.0026	0.0034
C	0.0009	0.0018	0.0026	0.0037
	X46_P0			
A	0.0074			
B	0.0068			
C	0.0074			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0078	0.0080	2.7538	1.2857
A to Z ↑	0.0144	0.0146	4.5424	2.1566
B to Z ↓	0.0062	0.0061	2.7040	1.2500

B to Z ↑	0.0153	0.0154	4.5653	2.1677
C to Z ↓	0.0065	0.0066	2.5861	1.2024
C to Z ↑	0.0090	0.0089	2.4829	1.1705
	X17_P0	**X23_P0**	**X17_P0**	**X23_P0**
A to Z ↓	0.0076	0.0082	0.8920	0.6619
A to Z ↑	0.0137	0.0150	1.4293	1.0947
B to Z ↓	0.0059	0.0061	0.8891	0.6628
B to Z ↑	0.0145	0.0151	1.4363	1.0994
C to Z ↓	0.0064	0.0066	0.8443	0.6260
C to Z ↑	0.0083	0.0086	0.7784	0.5931
	X46_P0		**X46_P0**	
A to Z ↓	0.0081		0.3459	
A to Z ↑	0.0147		0.5547	
B to Z ↓	0.0060		0.3426	
B to Z ↑	0.0149		0.5572	
C to Z ↓	0.0067		0.3256	
C to Z ↑	0.0084		0.3004	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P0	5.422e-05	1.145e-09
X11_P0	1.071e-04	1.642e-09
X17_P0	1.556e-04	2.139e-09
X23_P0	2.086e-04	2.801e-09
X46_P0	3.980e-04	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	3.950e-05	8.712e-05	1.245e-04	2.209e-04
B (output stable)	4.655e-05	1.068e-04	1.517e-04	3.408e-04
C (output stable)	2.030e-04	4.881e-04	6.056e-04	9.067e-04
A to Z	2.263e-03	4.843e-03	6.848e-03	9.879e-03
B to Z	1.957e-03	4.236e-03	5.877e-03	8.146e-03
C to Z	1.846e-03	3.972e-03	5.645e-03	7.854e-03
	X46_P0			
A (output stable)	4.227e-04			
B (output stable)	6.264e-04			
C (output stable)	1.682e-03			
A to Z	1.916e-02			
B to Z	1.577e-02			
C to Z	1.519e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	1.619e-07	2.321e-07	3.044e-07	5.900e-07
B (output stable)	2.797e-07	5.024e-07	6.616e-07	1.265e-06
C (output stable)	6.669e-08	-4.880e-08	-6.240e-08	-1.996e-07
A to Z	1.411e-06	1.314e-06	1.618e-06	2.547e-06
B to Z	8.043e-07	4.410e-07	-6.370e-07	2.000e-08
C to Z	4.899e-07	1.477e-07	1.547e-06	1.478e-06

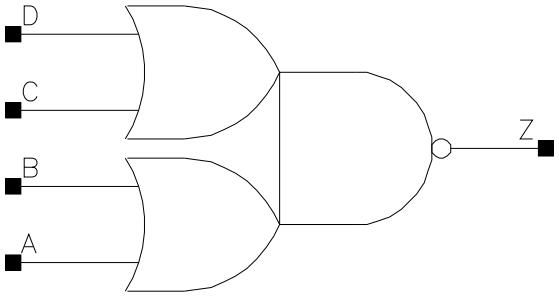
	X46_P0			
A (output stable)	9.532e-07			
B (output stable)	2.135e-06			
C (output stable)	-4.741e-07			
A to Z	5.030e-06			
B to Z	3.094e-06			
C to Z	1.737e-06			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0009	0.0018	0.0026	0.0036
B	0.0009	0.0016	0.0024	0.0034
C	0.0008	0.0017	0.0026	0.0036
D	0.0008	0.0016	0.0024	0.0034
	X42_P0			
A	0.0073			
B	0.0068			
C	0.0071			
D	0.0068			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0088	0.0097	2.5326	1.2594
A to Z ↑	0.0170	0.0169	4.7886	2.2062
B to Z ↓	0.0074	0.0078	2.4770	1.2646
B to Z ↑	0.0178	0.0169	4.8027	2.2154
C to Z ↓	0.0083	0.0092	2.6004	1.2824
C to Z ↑	0.0125	0.0129	4.6739	2.2134
D to Z ↓	0.0064	0.0069	2.5288	1.2913
D to Z ↑	0.0131	0.0124	4.6981	2.2275
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0091	0.0094	0.8616	0.6223
A to Z ↑	0.0159	0.0165	1.4860	1.0993
B to Z ↓	0.0075	0.0075	0.8651	0.6224
B to Z ↑	0.0163	0.0167	1.4939	1.1044
C to Z ↓	0.0088	0.0089	0.8796	0.6343
C to Z ↑	0.0120	0.0123	1.4921	1.1010
D to Z ↓	0.0068	0.0067	0.8874	0.6371
D to Z ↑	0.0119	0.0121	1.5029	1.1080
	X42_P0		**X42_P0**	
A to Z ↓	0.0096		0.3273	
A to Z ↑	0.0165		0.5614	
B to Z ↓	0.0077		0.3237	
B to Z ↑	0.0168		0.5639	
C to Z ↓	0.0095		0.3349	
C to Z ↑	0.0125		0.5580	
D to Z ↓	0.0071		0.3316	
D to Z ↑	0.0123		0.5617	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P0	6.267e-05	1.310e-09
X10_P0	1.296e-04	2.139e-09
X15_P0	1.839e-04	2.635e-09
X21_P0	2.405e-04	3.464e-09
X42_P0	4.655e-04	6.114e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	5.304e-05	1.600e-04	2.107e-04	3.034e-04
B (output stable)	7.014e-05	3.066e-04	3.259e-04	5.119e-04
C (output stable)	8.844e-05	2.412e-04	3.123e-04	4.489e-04
D (output stable)	1.090e-04	3.873e-04	4.234e-04	6.531e-04
A to Z	2.643e-03	5.848e-03	8.152e-03	1.143e-02
B to Z	2.338e-03	4.922e-03	6.897e-03	9.667e-03
C to Z	2.100e-03	4.707e-03	6.533e-03	9.073e-03
D to Z	1.821e-03	3.839e-03	5.375e-03	7.449e-03
	X42_P0			
A (output stable)	5.987e-04			
B (output stable)	9.946e-04			
C (output stable)	8.841e-04			
D (output stable)	1.282e-03			

A to Z	2.259e-02			
B to Z	1.910e-02			
C to Z	1.807e-02			
D to Z	1.481e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

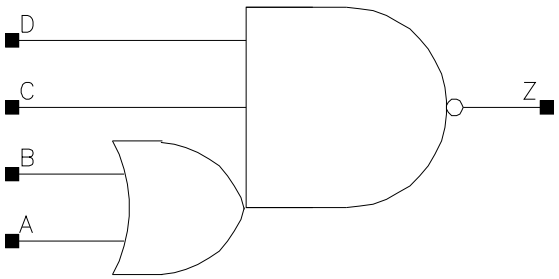
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	2.124e-07	6.170e-07	3.801e-07	7.558e-07
B (output stable)	3.778e-07	1.128e-06	1.051e-06	1.832e-06
C (output stable)	1.760e-07	4.987e-07	2.682e-07	6.161e-07
D (output stable)	3.333e-07	1.028e-06	9.331e-07	1.730e-06
A to Z	4.353e-07	2.472e-06	2.424e-06	5.393e-06
B to Z	5.126e-07	1.082e-06	2.523e-06	3.976e-06
C to Z	1.050e-06	2.912e-06	2.859e-06	6.098e-06
D to Z	7.459e-07	1.867e-06	1.814e-06	2.599e-06
	X42_P0			
A (output stable)	1.426e-06			
B (output stable)	3.252e-06			
C (output stable)	1.198e-06			
D (output stable)	2.866e-06			
A to Z	1.020e-05			
B to Z	6.445e-06			
C to Z	7.977e-06			
D to Z	4.243e-06			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X21_P0	1.200	2.448	2.9376
X31_P0	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X21_P0	X31_P0
A	0.0009	0.0017	0.0034	0.0051
B	0.0011	0.0016	0.0031	0.0048
C	0.0009	0.0018	0.0037	0.0055
D	0.0009	0.0018	0.0035	0.0053

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0126	0.0123	3.3796	1.8202
A to Z ↑	0.0153	0.0141	4.3545	2.1930
B to Z ↓	0.0109	0.0097	3.4392	1.8307
B to Z ↑	0.0161	0.0138	4.3889	2.2071
C to Z ↓	0.0105	0.0107	3.1892	1.7114

C to Z ↑	0.0141	0.0137	2.2652	1.1430
D to Z ↓	0.0117	0.0111	3.2142	1.7233
D to Z ↑	0.0134	0.0124	2.2986	1.1462
	X21_P0	**X31_P0**	**X21_P0**	**X31_P0**
A to Z ↓	0.0125	0.0128	0.9508	0.6463
A to Z ↑	0.0137	0.0137	1.0965	0.7371
B to Z ↓	0.0100	0.0101	0.9572	0.6531
B to Z ↑	0.0135	0.0135	1.1030	0.7420
C to Z ↓	0.0106	0.0108	0.8953	0.6096
C to Z ↑	0.0134	0.0135	0.5800	0.3923
D to Z ↓	0.0113	0.0115	0.9011	0.6136
D to Z ↑	0.0122	0.0123	0.5811	0.3919

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P0	4.711e-05	1.476e-09
X10_P0	8.718e-05	2.139e-09
X21_P0	1.635e-04	3.464e-09
X31_P0	2.399e-04	4.789e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	1.231e-04	2.571e-04	4.688e-04	6.968e-04
B (output stable)	1.347e-04	2.856e-04	5.182e-04	7.690e-04
C (output stable)	5.648e-05	1.579e-04	3.049e-04	4.494e-04
D (output stable)	6.703e-05	2.238e-04	3.958e-04	5.827e-04
A to Z	2.694e-03	4.817e-03	9.376e-03	1.395e-02
B to Z	2.257e-03	3.916e-03	7.588e-03	1.131e-02
C to Z	3.195e-03	6.075e-03	1.173e-02	1.743e-02
D to Z	2.938e-03	5.354e-03	1.035e-02	1.540e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

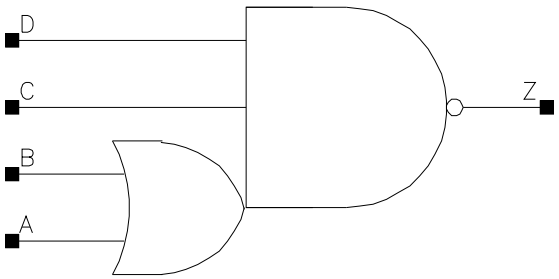
Pin Cycle (vdds)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	9.736e-08	7.203e-08	-1.110e-07	-1.815e-07
B (output stable)	2.343e-07	3.456e-07	4.147e-07	5.700e-07
C (output stable)	8.440e-08	5.252e-08	2.880e-08	-3.458e-08
D (output stable)	7.194e-08	1.600e-08	-9.980e-08	-1.330e-07
A to Z	6.650e-07	1.336e-06	3.232e-06	2.290e-06
B to Z	-3.000e-09	9.000e-08	3.480e-07	4.680e-07
C to Z	9.757e-07	1.864e-06	3.283e-06	6.067e-06
D to Z	7.123e-07	1.799e-06	2.007e-06	2.293e-06

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0009	0.0018	0.0028	0.0037
B	0.0009	0.0017	0.0025	0.0034
C	0.0009	0.0018	0.0027	0.0036
D	0.0009	0.0017	0.0026	0.0035

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0106	0.0115	3.4471	1.8086
A to Z ↑	0.0168	0.0181	4.2104	2.1535
B to Z ↓	0.0090	0.0095	3.3786	1.8114
B to Z ↑	0.0178	0.0184	4.2291	2.1625
C to Z ↓	0.0093	0.0103	3.2615	1.7288

C to Z ↑	0.0111	0.0117	2.3104	1.1687
D to Z ↓	0.0095	0.0102	3.2833	1.7384
D to Z ↑	0.0097	0.0098	2.3264	1.1780
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0113	0.0114	1.2448	0.9408
A to Z ↑	0.0173	0.0178	1.4534	1.1039
B to Z ↓	0.0095	0.0094	1.2391	0.9393
B to Z ↑	0.0178	0.0183	1.4606	1.1084
C to Z ↓	0.0100	0.0102	1.1849	0.8966
C to Z ↑	0.0111	0.0114	0.7807	0.5871
D to Z ↓	0.0100	0.0104	1.1921	0.9015
D to Z ↑	0.0094	0.0096	0.7862	0.5915

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P0	4.679e-05	1.476e-09
X10_P0	8.937e-05	2.139e-09
X15_P0	1.249e-04	2.635e-09
X21_P0	1.692e-04	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	3.455e-05	7.703e-05	1.126e-04	1.489e-04
B (output stable)	3.662e-05	1.104e-04	1.372e-04	1.982e-04
C (output stable)	7.283e-05	1.736e-04	2.513e-04	3.451e-04
D (output stable)	1.161e-04	3.841e-04	4.660e-04	6.888e-04
A to Z	2.918e-03	6.220e-03	8.849e-03	1.208e-02
B to Z	2.558e-03	5.261e-03	7.475e-03	1.022e-02
C to Z	2.309e-03	4.910e-03	6.928e-03	9.478e-03
D to Z	2.118e-03	4.320e-03	6.212e-03	8.368e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

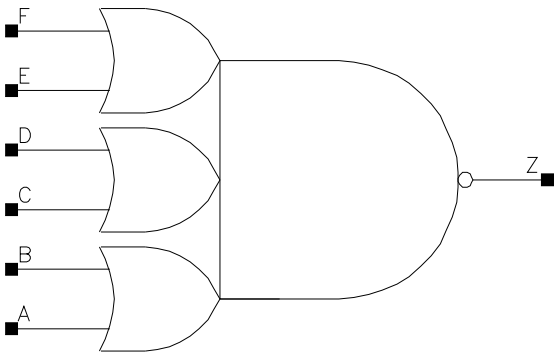
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	1.486e-07	3.308e-07	2.052e-07	4.515e-07
B (output stable)	2.384e-07	6.367e-07	5.503e-07	9.798e-07
C (output stable)	8.165e-08	4.374e-08	-2.920e-08	-5.836e-08
D (output stable)	7.844e-08	7.980e-09	-2.980e-08	-8.892e-08
A to Z	7.810e-07	2.557e-06	1.692e-06	2.897e-06
B to Z	2.890e-07	-4.870e-07	3.505e-06	5.520e-07
C to Z	1.399e-06	2.278e-06	3.066e-06	4.706e-06
D to Z	6.123e-07	1.014e-06	8.763e-07	9.157e-07

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	1.088	1.3056
X9_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X9_P0
A	0.0007	0.0018
B	0.0007	0.0017
C	0.0007	0.0018
D	0.0007	0.0016
E	0.0007	0.0017
F	0.0007	0.0016

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X9_P0	X3_P0	X9_P0
A to Z ↓	0.0138	0.0150	3.9352	1.6484
A to Z ↑	0.0229	0.0219	5.8369	2.1677
B to Z ↓	0.0127	0.0130	3.9701	1.6514
B to Z ↑	0.0247	0.0223	5.8565	2.1753
C to Z ↓	0.0138	0.0147	3.9825	1.6612
C to Z ↑	0.0198	0.0188	5.8616	2.1649
D to Z ↓	0.0124	0.0126	4.0208	1.6670
D to Z ↑	0.0214	0.0190	5.8876	2.1746
E to Z ↓	0.0122	0.0134	4.0241	1.6698
E to Z ↑	0.0153	0.0148	5.8867	2.1697
F to Z ↓	0.0109	0.0111	4.0684	1.6754
F to Z ↑	0.0166	0.0145	5.9255	2.1832

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X3_P0	5.740e-05	1.807e-09
X9_P0	1.436e-04	2.967e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X3_P0	X9_P0
A (output stable)	4.683e-05	1.554e-04
B (output stable)	5.516e-05	2.493e-04
C (output stable)	6.695e-05	1.949e-04
D (output stable)	7.526e-05	2.950e-04
E (output stable)	1.438e-04	3.658e-04
F (output stable)	1.546e-04	4.542e-04
A to Z	3.240e-03	8.341e-03
B to Z	2.984e-03	7.312e-03
C to Z	2.709e-03	6.971e-03
D to Z	2.470e-03	6.073e-03
E to Z	2.140e-03	5.717e-03
F to Z	1.927e-03	4.831e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

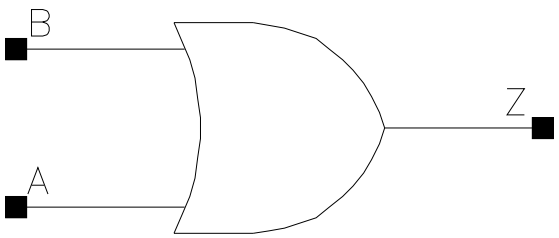
Pin Cycle (vdds)	X3_P0	X9_P0
A (output stable)	1.474e-07	5.254e-07
B (output stable)	2.746e-07	9.041e-07
C (output stable)	1.025e-07	3.532e-07
D (output stable)	2.300e-07	6.948e-07
E (output stable)	6.958e-08	2.924e-07
F (output stable)	2.057e-07	7.668e-07
A to Z	4.999e-07	7.792e-07
B to Z	2.316e-07	6.910e-07
C to Z	6.811e-08	1.167e-06
D to Z	1.113e-07	3.478e-07
E to Z	5.748e-07	1.908e-06
F to Z	6.522e-08	5.984e-07

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X33_P0	1.200	1.360	1.6320
X50_P0	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P0	X16_P0	X33_P0	X50_P0
A	0.0008	0.0010	0.0019	0.0020
B	0.0007	0.0010	0.0019	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0246	0.0223	1.5479	0.7786
A to Z ↑	0.0150	0.0163	2.2402	1.1303
B to Z ↓	0.0260	0.0235	1.5480	0.7787
B to Z ↑	0.0138	0.0149	2.2399	1.1294
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0231	0.0275	0.3855	0.2646
A to Z ↑	0.0163	0.0162	0.5514	0.3734
B to Z ↓	0.0235	0.0284	0.3858	0.2645
B to Z ↑	0.0145	0.0149	0.5509	0.3731

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	7.507e-05	1.145e-09
X16_P0	1.368e-04	1.310e-09
X33_P0	2.655e-04	2.139e-09
X50_P0	3.516e-04	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	3.281e-05	6.144e-05	1.927e-04	1.832e-04
B (output stable)	5.259e-05	9.119e-05	4.302e-04	3.997e-04
A to Z	3.654e-03	6.181e-03	1.292e-02	1.838e-02
B to Z	3.491e-03	5.922e-03	1.206e-02	1.763e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

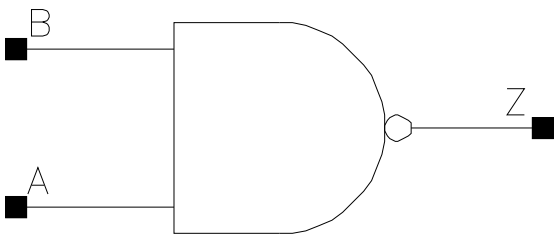
Pin Cycle (vdds)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	1.906e-07	2.894e-07	8.065e-07	7.936e-07
B (output stable)	3.376e-07	5.085e-07	1.649e-06	1.655e-06
A to Z	1.208e-07	2.001e-07	2.461e-06	2.996e-06
B to Z	2.215e-06	1.774e-06	4.085e-06	4.752e-06

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X16_P0	1.200	0.952	1.1424
X24_P0	1.200	1.088	1.3056
X32_P0	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P0	X16_P0	X24_P0	X32_P0
A	0.0010	0.0010	0.0010	0.0010
B	0.0011	0.0011	0.0011	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0201	0.0211	1.5066	0.7834
A to Z ↑	0.0238	0.0246	2.2748	1.1619
B to Z ↓	0.0213	0.0222	1.5082	0.7827
B to Z ↑	0.0226	0.0230	2.2770	1.1619
	X24_P0	**X32_P0**	**X24_P0**	**X32_P0**
A to Z ↓	0.0233	0.0241	0.5287	0.3951
A to Z ↑	0.0263	0.0268	0.7766	0.5795
B to Z ↓	0.0245	0.0254	0.5280	0.3947
B to Z ↑	0.0247	0.0256	0.7768	0.5801

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	1.370e-04	1.476e-09
X16_P0	1.828e-04	1.642e-09
X24_P0	2.256e-04	1.807e-09
X32_P0	2.934e-04	1.973e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	3.755e-05	3.752e-05	3.768e-05	3.905e-05
B (output stable)	4.316e-05	4.345e-05	4.286e-05	4.418e-05
A to Z	6.597e-03	7.854e-03	1.001e-02	1.311e-02
B to Z	6.407e-03	7.672e-03	9.834e-03	1.293e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

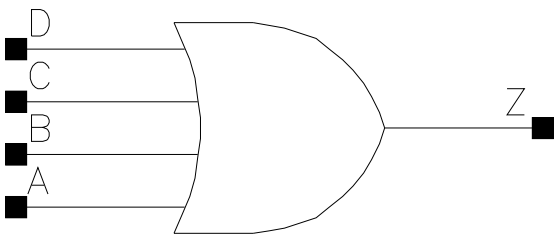
Pin Cycle (vdds)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	9.021e-08	9.186e-08	9.206e-08	9.450e-08
B (output stable)	8.307e-08	8.198e-08	8.240e-08	8.638e-08
A to Z	9.985e-07	8.056e-07	6.670e-07	4.440e-07
B to Z	-9.470e-07	6.824e-07	4.740e-07	-4.900e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X27_P0
A	0.0017	0.0020
B	0.0016	0.0020
C	0.0017	0.0020
D	0.0016	0.0021

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0252	0.0265	0.8660	0.6474
A to Z ↑	0.0166	0.0160	0.7406	0.5518
B to Z ↓	0.0259	0.0270	0.8659	0.6474
B to Z ↑	0.0153	0.0144	0.7399	0.5508
C to Z ↓	0.0248	0.0263	0.8652	0.6467
C to Z ↑	0.0158	0.0157	0.7412	0.5527
D to Z ↓	0.0256	0.0269	0.8643	0.6461
D to Z ↑	0.0147	0.0142	0.7400	0.5522

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X20_P0	2.027e-04	3.132e-09
X27_P0	2.748e-04	3.629e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X20_P0	X27_P0
A (output stable)	2.526e-03	3.461e-03
B (output stable)	2.313e-03	3.190e-03
C (output stable)	2.271e-03	3.184e-03
D (output stable)	2.063e-03	2.968e-03
A to Z	1.082e-02	1.502e-02
B to Z	1.018e-02	1.407e-02
C to Z	9.984e-03	1.376e-02
D to Z	9.402e-03	1.293e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

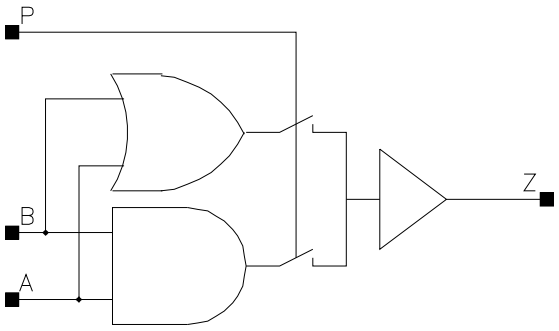
Pin Cycle (vdds)	X20_P0	X27_P0
A (output stable)	3.848e-07	6.041e-07
B (output stable)	5.422e-07	9.836e-07
C (output stable)	4.336e-07	1.231e-06
D (output stable)	6.877e-07	1.328e-06
A to Z	3.814e-06	8.624e-07
B to Z	4.862e-06	7.374e-06
C to Z	4.475e-06	7.827e-07
D to Z	1.310e-07	8.648e-06

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X16_P0	1.200	1.224	1.4688
X25_P0	1.200	2.040	2.4480
X33_P0	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0013	0.0018	0.0032	0.0033
B	0.0012	0.0018	0.0037	0.0037
P	0.0007	0.0010	0.0019	0.0019

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0297	0.0275	1.5751	0.7701
A to Z ↑	0.0199	0.0191	2.2769	1.1373
B to Z ↓	0.0302	0.0281	1.5811	0.7745
B to Z ↑	0.0208	0.0199	2.2773	1.1397
P to Z ↓	0.0285	0.0269	1.5796	0.7731
P to Z ↑	0.0204	0.0197	2.2741	1.1371
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**

A to Z ↓	0.0264	0.0284	0.5235	0.3958
A to Z ↑	0.0189	0.0202	0.7665	0.5733
B to Z ↓	0.0269	0.0286	0.5260	0.3972
B to Z ↑	0.0201	0.0212	0.7673	0.5739
P to Z ↓	0.0262	0.0281	0.5257	0.3965
P to Z ↑	0.0194	0.0207	0.7651	0.5722

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	7.693e-05	1.642e-09
X16_P0	1.552e-04	1.973e-09
X25_P0	2.560e-04	2.967e-09
X33_P0	2.955e-04	3.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	7.482e-05	1.216e-04	2.598e-04	2.638e-04
B (output stable)	8.599e-05	1.516e-04	3.898e-04	3.936e-04
P (output stable)	1.946e-04	3.398e-04	5.241e-04	5.399e-04
A to Z	4.154e-03	7.405e-03	1.233e-02	1.500e-02
B to Z	4.082e-03	7.340e-03	1.200e-02	1.469e-02
P to Z	3.876e-03	7.061e-03	1.170e-02	1.439e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

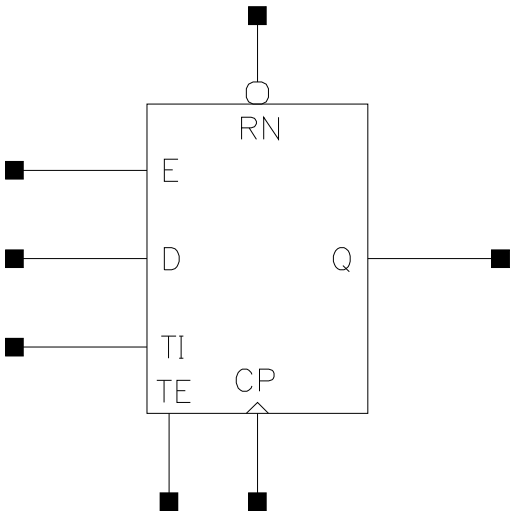
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	2.758e-07	3.667e-07	3.936e-07	4.461e-07
B (output stable)	2.842e-07	4.235e-07	7.565e-07	7.335e-07
P (output stable)	4.139e-07	6.778e-07	7.381e-07	7.474e-07
A to Z	2.956e-07	1.309e-07	4.330e-07	-2.900e-08
B to Z	2.524e-07	1.171e-07	3.258e-07	1.627e-07
P to Z	1.547e-08	-4.010e-08	2.120e-07	-2.110e-08

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.488	5.3856
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0011	0.0011
RN	0.0009	0.0007	0.0008	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
CP to Q ↓	0.0518	0.0290	3.1878	1.5316
CP to Q ↑	0.0446	0.0383	4.4629	2.2525
RN to Q ↓	0.0384	0.0451	2.8743	1.4931
	X17_P0	X33_P0	X17_P0	X33_P0
CP to Q ↓	0.0504	0.0534	0.7489	0.3915
CP to Q ↑	0.0618	0.0649	1.1059	0.5639
RN to Q ↓	0.0614	0.0650	0.7484	0.3919

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0678	0.0480	0.0480	0.0480
CP ↑	min_pulse_width to CP	0.0483	0.0242	0.0205	0.0205
D ↓	hold_rising to CP	-0.0669	-0.0283	-0.0283	-0.0283
D ↑	hold_rising to CP	-0.0428	-0.0067	-0.0123	-0.0123
D ↓	setup_rising to CP	0.1022	0.0630	0.0630	0.0630
D ↑	setup_rising to CP	0.0702	0.0367	0.0367	0.0367
E ↓	hold_rising to CP	-0.0474	-0.0474	-0.0474	-0.0474
E ↑	hold_rising to CP	-0.0354	-0.0065	-0.0065	-0.0065
E ↓	setup_rising to CP	0.0872	0.0876	0.0879	0.0879
E ↑	setup_rising to CP	0.0901	0.0663	0.0663	0.0663
RN ↓	min_pulse_width to RN	0.0518	0.0566	0.0496	0.0496
RN ↑	recovery_rising to CP	0.0126	0.0071	0.0102	0.0101
RN ↑	removal_rising to CP	-0.0076	-0.0031	-0.0027	-0.0027
TE ↓	hold_rising to CP	-0.0282	-0.0184	-0.0184	-0.0184
TE ↑	hold_rising to CP	-0.0260	-0.0166	-0.0166	-0.0166
TE ↓	setup_rising to CP	0.0680	0.0583	0.0583	0.0583
TE ↑	setup_rising to CP	0.1201	0.0806	0.0803	0.0803
TI ↓	hold_rising to CP	-0.0869	-0.0418	-0.0418	-0.0418
TI ↑	hold_rising to CP	-0.0305	-0.0133	-0.0133	-0.0133
TI ↓	setup_rising to CP	0.1222	0.0764	0.0764	0.0764
TI ↑	setup_rising to CP	0.0609	0.0422	0.0422	0.0422

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.742e-04	6.340e-09
X8_P0	2.969e-04	5.948e-09
X17_P0	3.692e-04	6.279e-09
X33_P0	4.568e-04	6.611e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

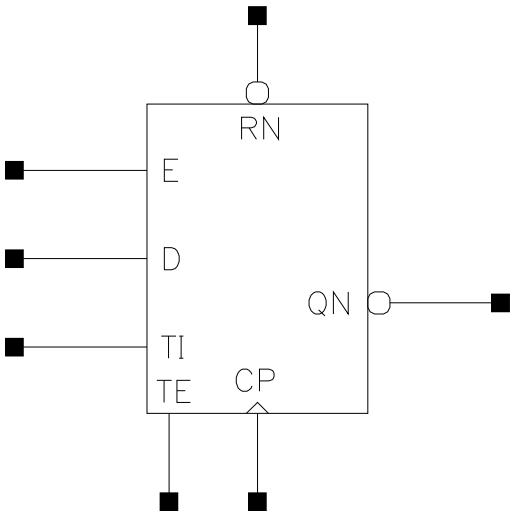
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.968e-03	5.996e-03	6.004e-03	6.008e-03
Clock 100Mhz Data 25Mhz	1.001e-02	9.982e-03	1.089e-02	1.221e-02
Clock 100Mhz Data 50Mhz	1.406e-02	1.397e-02	1.577e-02	1.840e-02
Clock = 0 Data 100Mhz	9.273e-03	8.647e-03	8.439e-03	8.338e-03
Clock = 1 Data 100Mhz	3.039e-03	3.107e-03	3.132e-03	3.144e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.624	5.5488
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0011	0.0011
RN	0.0009	0.0009	0.0009	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
CP to QN ↓	0.0542	0.0511	2.7456	1.4826
CP to QN ↑	0.0589	0.0394	4.3745	2.1869
RN to QN ↑	0.0482	0.0512	4.3730	2.1904
	X17_P0	X33_P0	X17_P0	X33_P0
CP to QN ↓	0.0493	0.0525	0.7493	0.3912
CP to QN ↑	0.0408	0.0447	1.1067	0.5653
RN to QN ↑	0.0557	0.0586	1.1031	0.5637

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0678	0.0480	0.0480	0.0480
CP ↑	min_pulse_width to CP	0.0338	0.0205	0.0242	0.0253
D ↓	hold_rising to CP	-0.0694	-0.0283	-0.0283	-0.0283
D ↑	hold_rising to CP	-0.0428	-0.0123	-0.0067	-0.0067
D ↓	setup_rising to CP	0.1015	0.0630	0.0630	0.0630
D ↑	setup_rising to CP	0.0702	0.0367	0.0367	0.0367
E ↓	hold_rising to CP	-0.0474	-0.0474	-0.0474	-0.0474
E ↑	hold_rising to CP	-0.0354	-0.0065	-0.0065	-0.0065
E ↓	setup_rising to CP	0.0902	0.0879	0.0876	0.0879
E ↑	setup_rising to CP	0.0901	0.0663	0.0663	0.0664
RN ↓	min_pulse_width to RN	0.0469	0.0496	0.0566	0.0615
RN ↑	recovery_rising to CP	0.0126	0.0127	0.0101	0.0101
RN ↑	removal_rising to CP	-0.0076	-0.0027	-0.0030	-0.0030
TE ↓	hold_rising to CP	-0.0282	-0.0184	-0.0188	-0.0188
TE ↑	hold_rising to CP	-0.0264	-0.0166	-0.0166	-0.0166
TE ↓	setup_rising to CP	0.0680	0.0583	0.0583	0.0583
TE ↑	setup_rising to CP	0.1201	0.0803	0.0803	0.0803
TI ↓	hold_rising to CP	-0.0869	-0.0418	-0.0418	-0.0418
TI ↑	hold_rising to CP	-0.0305	-0.0133	-0.0133	-0.0133
TI ↓	setup_rising to CP	0.1222	0.0764	0.0764	0.0764
TI ↑	setup_rising to CP	0.0609	0.0422	0.0422	0.0422

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.823e-04	6.340e-09
X8_P0	3.067e-04	6.114e-09
X17_P0	3.772e-04	6.279e-09
X33_P0	4.693e-04	6.611e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

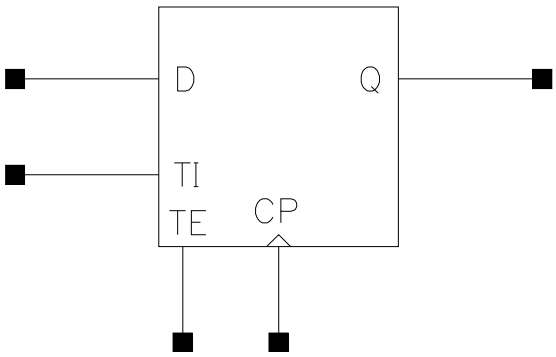
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.964e-03	5.996e-03	6.000e-03	6.002e-03
Clock 100Mhz Data 25Mhz	9.796e-03	9.998e-03	1.088e-02	1.224e-02
Clock 100Mhz Data 50Mhz	1.363e-02	1.400e-02	1.575e-02	1.848e-02
Clock = 0 Data 100Mhz	9.279e-03	8.652e-03	8.444e-03	8.341e-03
Clock = 1 Data 100Mhz	3.036e-03	3.109e-03	3.134e-03	3.147e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.400	4.0800
X8_P0	1.200	3.128	3.7536
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0429	0.0270	3.0332	1.5347
CP to Q ↑	0.0399	0.0348	4.4919	2.2224
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0415	0.0456	0.7370	0.3856
CP to Q ↑	0.0588	0.0625	1.1063	0.5639

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0630	0.0668	0.0668	0.0668
CP ↑	min_pulse_width to CP	0.0338	0.0205	0.0193	0.0193
D ↓	hold_rising to CP	-0.0425	-0.0113	-0.0144	-0.0144
D ↑	hold_rising to CP	-0.0110	0.0082	0.0082	0.0082
D ↓	setup_rising to CP	0.0729	0.0463	0.0463	0.0463
D ↑	setup_rising to CP	0.0358	0.0193	0.0193	0.0193
TE ↓	hold_rising to CP	-0.0230	-0.0095	-0.0095	-0.0095
TE ↑	hold_rising to CP	-0.0159	-0.0070	-0.0070	-0.0070
TE ↓	setup_rising to CP	0.0576	0.0441	0.0438	0.0438
TE ↑	setup_rising to CP	0.1047	0.0859	0.0859	0.0859
TI ↓	hold_rising to CP	-0.0874	-0.0519	-0.0519	-0.0519
TI ↑	hold_rising to CP	-0.0208	-0.0090	-0.0090	-0.0090
TI ↓	setup_rising to CP	0.1132	0.0867	0.0867	0.0867
TI ↑	setup_rising to CP	0.0456	0.0332	0.0332	0.0332

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.171e-04	4.623e-09
X8_P0	2.447e-04	4.292e-09
X17_P0	3.417e-04	4.789e-09
X33_P0	4.181e-04	5.120e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

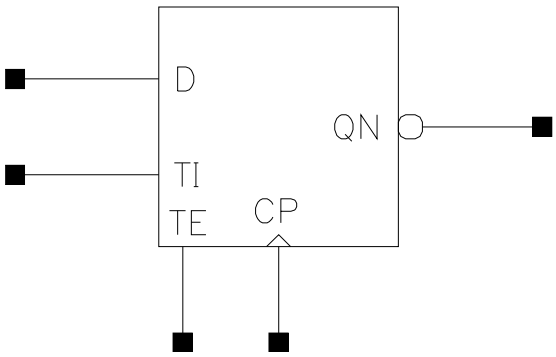
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.440e-03	5.475e-03	5.483e-03	5.488e-03
Clock 100Mhz Data 25Mhz	8.298e-03	8.285e-03	9.223e-03	1.037e-02
Clock 100Mhz Data 50Mhz	1.116e-02	1.110e-02	1.296e-02	1.525e-02
Clock = 0 Data 100Mhz	7.247e-03	6.679e-03	6.492e-03	6.400e-03
Clock = 1 Data 100Mhz	1.739e-03	9.044e-04	6.262e-04	4.872e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.536	4.2432
X8_P0	1.200	3.264	3.9168
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0505	0.0531	3.1442	1.5203
CP to QN ↑	0.0470	0.0361	4.4627	2.1939
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0422	0.0465	0.7379	0.3855
CP to QN ↑	0.0355	0.0394	1.1073	0.5643

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0630	0.0668	0.0668	0.0668
CP ↑	min_pulse_width to CP	0.0290	0.0193	0.0205	0.0205
D ↓	hold_rising to CP	-0.0425	-0.0113	-0.0113	-0.0113
D ↑	hold_rising to CP	-0.0110	0.0082	0.0082	0.0082
D ↓	setup_rising to CP	0.0729	0.0463	0.0463	0.0463
D ↑	setup_rising to CP	0.0358	0.0193	0.0193	0.0193
TE ↓	hold_rising to CP	-0.0230	-0.0095	-0.0095	-0.0095
TE ↑	hold_rising to CP	-0.0159	-0.0070	-0.0070	-0.0070
TE ↓	setup_rising to CP	0.0576	0.0441	0.0438	0.0438
TE ↑	setup_rising to CP	0.1047	0.0859	0.0855	0.0859
TI ↓	hold_rising to CP	-0.0874	-0.0519	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0208	-0.0090	-0.0090	-0.0090
TI ↓	setup_rising to CP	0.1132	0.0867	0.0867	0.0867
TI ↑	setup_rising to CP	0.0471	0.0332	0.0332	0.0332

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.210e-04	4.789e-09
X8_P0	2.476e-04	4.457e-09
X17_P0	3.375e-04	4.789e-09
X33_P0	4.140e-04	5.120e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

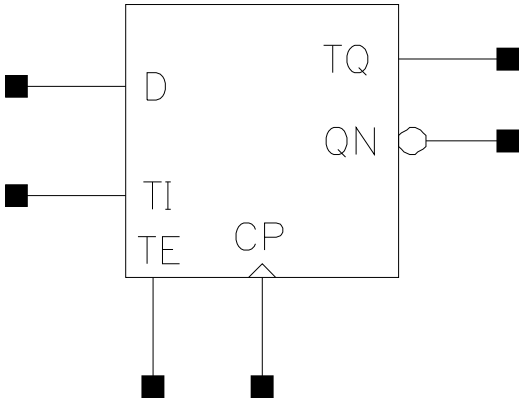
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.387e-03	5.448e-03	5.466e-03	5.475e-03
Clock 100Mhz Data 25Mhz	8.179e-03	8.416e-03	9.171e-03	1.032e-02
Clock 100Mhz Data 50Mhz	1.097e-02	1.138e-02	1.288e-02	1.517e-02
Clock = 0 Data 100Mhz	7.286e-03	6.696e-03	6.501e-03	6.404e-03
Clock = 1 Data 100Mhz	1.729e-03	8.991e-04	6.228e-04	4.846e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.536	4.2432
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0012	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0559	0.0485	2.8555	1.4985
CP to QN ↑	0.0566	0.0374	4.4155	2.2080
CP to TQ ↓	0.0389	0.0246	3.8371	2.7602
CP to TQ ↑	0.0409	0.0345	8.1538	5.9035
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0464	0.0505	0.7542	0.3941
CP to QN ↑	0.0388	0.0418	1.1203	0.5762
CP to TQ ↓	0.0255	0.0265	3.6073	3.6141
CP to TQ ↑	0.0351	0.0360	7.6066	8.0227

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0630	0.0668	0.0668	0.0668
CP ↑	min_pulse_width to CP	0.0338	0.0205	0.0205	0.0242
D ↓	hold_rising to CP	-0.0429	-0.0113	-0.0113	-0.0113
D ↑	hold_rising to CP	-0.0110	0.0082	0.0082	0.0082
D ↓	setup_rising to CP	0.0673	0.0463	0.0463	0.0463
D ↑	setup_rising to CP	0.0358	0.0193	0.0193	0.0193
TE ↓	hold_rising to CP	-0.0230	-0.0095	-0.0095	-0.0095
TE ↑	hold_rising to CP	-0.0159	-0.0070	-0.0070	-0.0070
TE ↓	setup_rising to CP	0.0579	0.0438	0.0438	0.0438
TE ↑	setup_rising to CP	0.1050	0.0859	0.0859	0.0859
TI ↓	hold_rising to CP	-0.0833	-0.0521	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0208	-0.0090	-0.0090	-0.0090
TI ↓	setup_rising to CP	0.1117	0.0867	0.0867	0.0867
TI ↑	setup_rising to CP	0.0471	0.0332	0.0332	0.0332

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.436e-04	5.131e-09
X8_P0	2.762e-04	4.789e-09
X17_P0	3.241e-04	4.954e-09
X33_P0	4.135e-04	5.286e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0

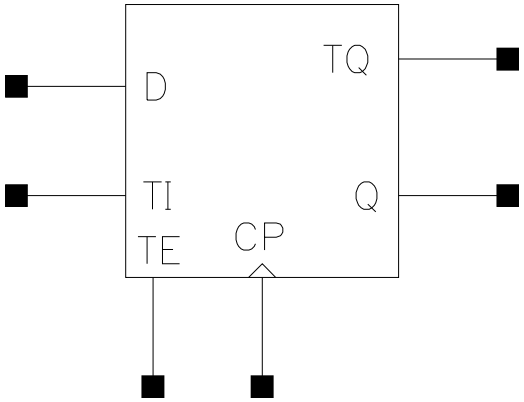
Clock 100Mhz Data 0Mhz	5.521e-03	5.516e-03	5.514e-03	5.514e-03
Clock 100Mhz Data 25Mhz	8.644e-03	8.777e-03	9.252e-03	1.061e-02
Clock 100Mhz Data 50Mhz	1.177e-02	1.204e-02	1.299e-02	1.571e-02
Clock = 0 Data 100Mhz	7.281e-03	6.710e-03	6.519e-03	6.423e-03
Clock = 1 Data 100Mhz	1.738e-03	9.041e-04	6.260e-04	4.871e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.400	4.0800
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0570	0.0304	3.1650	1.5257
CP to Q ↑	0.0461	0.0371	4.5443	2.2365
CP to TQ ↓	0.0536	0.0309	3.1703	3.7115
CP to TQ ↑	0.0472	0.0404	5.9598	8.1553
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0426	0.0468	0.7575	0.3933
CP to Q ↑	0.0599	0.0637	1.1308	0.5678
CP to TQ ↓	0.0440	0.0485	3.5484	3.6136
CP to TQ ↑	0.0633	0.0683	7.8689	7.9580

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0630	0.0668	0.0668	0.0668
CP ↑	min_pulse_width to CP	0.0482	0.0242	0.0193	0.0193
D ↓	hold_rising to CP	-0.0425	-0.0113	-0.0144	-0.0144
D ↑	hold_rising to CP	-0.0110	0.0082	0.0057	0.0082
D ↓	setup_rising to CP	0.0729	0.0463	0.0463	0.0463
D ↑	setup_rising to CP	0.0358	0.0193	0.0193	0.0193
TE ↓	hold_rising to CP	-0.0230	-0.0095	-0.0095	-0.0095
TE ↑	hold_rising to CP	-0.0159	-0.0070	-0.0070	-0.0070
TE ↓	setup_rising to CP	0.0576	0.0438	0.0438	0.0438
TE ↑	setup_rising to CP	0.1047	0.0859	0.0859	0.0859
TI ↓	hold_rising to CP	-0.0874	-0.0521	-0.0519	-0.0519
TI ↑	hold_rising to CP	-0.0208	-0.0090	-0.0090	-0.0090
TI ↓	setup_rising to CP	0.1132	0.0867	0.0867	0.0867
TI ↑	setup_rising to CP	0.0471	0.0332	0.0332	0.0332

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.425e-04	4.954e-09
X8_P0	2.610e-04	4.623e-09
X17_P0	3.548e-04	4.954e-09
X33_P0	4.307e-04	5.286e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

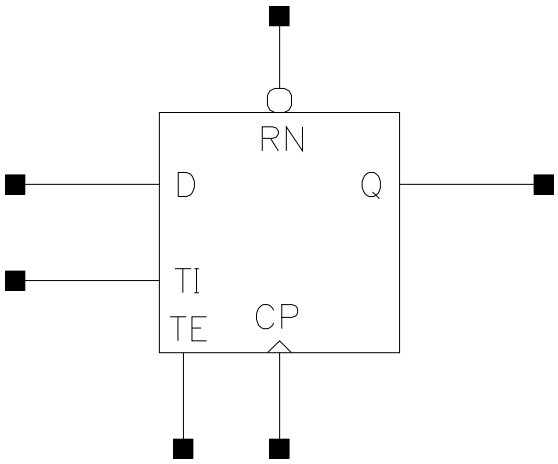
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.418e-03	5.461e-03	5.475e-03	5.481e-03
Clock 100Mhz Data 25Mhz	9.019e-03	8.646e-03	9.493e-03	1.073e-02
Clock 100Mhz Data 50Mhz	1.262e-02	1.183e-02	1.351e-02	1.599e-02
Clock = 0 Data 100Mhz	7.240e-03	6.674e-03	6.491e-03	6.399e-03
Clock = 1 Data 100Mhz	1.726e-03	8.977e-04	6.220e-04	4.840e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.672	4.4064
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
RN	0.0009	0.0007	0.0008	0.0008
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0516	0.0290	3.2229	1.5339
CP to Q ↑	0.0443	0.0375	4.4888	2.2512
RN to Q ↓	0.0384	0.0452	2.8852	1.4977
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0433	0.0477	0.7444	0.3908
CP to Q ↑	0.0546	0.0583	1.1030	0.5627
RN to Q ↓	0.0545	0.0590	0.7443	0.3906

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0697	0.0668	0.0697	0.0697
CP ↑	min_pulse_width to CP	0.0434	0.0242	0.0193	0.0193
D ↓	hold_rising to CP	-0.0383	-0.0068	-0.0068	-0.0068
D ↑	hold_rising to CP	-0.0159	0.0031	0.0005	0.0005
D ↓	setup_rising to CP	0.0673	0.0415	0.0411	0.0411
D ↑	setup_rising to CP	0.0463	0.0242	0.0242	0.0242
RN ↓	min_pulse_width to RN	0.0469	0.0518	0.0496	0.0496
RN ↑	recovery_rising to CP	0.0126	0.0127	0.0127	0.0127
RN ↑	removal_rising to CP	-0.0076	-0.0027	-0.0027	-0.0027
TE ↓	hold_rising to CP	-0.0230	-0.0021	-0.0046	-0.0046
TE ↑	hold_rising to CP	-0.0264	-0.0144	-0.0140	-0.0140
TE ↓	setup_rising to CP	0.0583	0.0432	0.0432	0.0432
TE ↑	setup_rising to CP	0.0998	0.0810	0.0810	0.0810
TI ↓	hold_rising to CP	-0.0776	-0.0367	-0.0408	-0.0367
TI ↑	hold_rising to CP	-0.0271	-0.0139	-0.0147	-0.0147
TI ↓	setup_rising to CP	0.1124	0.0818	0.0818	0.0818
TI ↑	setup_rising to CP	0.0554	0.0396	0.0435	0.0435

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.438e-04	5.286e-09
X8_P0	2.628e-04	4.954e-09
X17_P0	3.529e-04	5.451e-09
X33_P0	4.253e-04	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.963e-03	5.984e-03	6.015e-03	6.031e-03

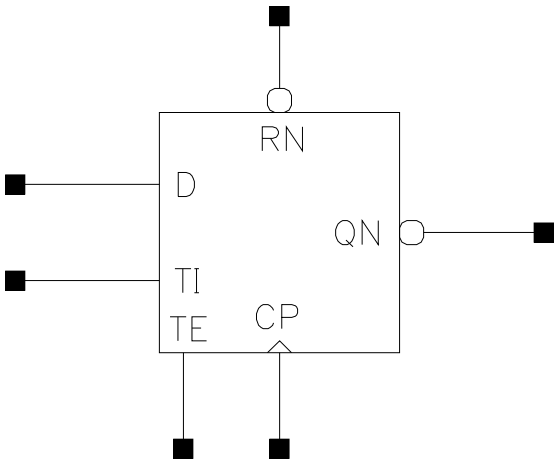
Clock 100Mhz Data 25Mhz	9.259e-03	9.009e-03	9.980e-03	1.117e-02
Clock 100Mhz Data 50Mhz	1.255e-02	1.203e-02	1.394e-02	1.631e-02
Clock = 0 Data 100Mhz	7.157e-03	6.498e-03	6.284e-03	6.178e-03
Clock = 1 Data 100Mhz	1.769e-03	9.214e-04	6.389e-04	4.977e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	3.944	4.7328
X33_P0	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
RN	0.0009	0.0009	0.0009	0.0009
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0492	0.0457	2.7047	1.4516
CP to QN ↑	0.0535	0.0353	4.3916	2.1768
RN to QN ↑	0.0435	0.0468	4.3811	2.1790
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0457	0.0502	0.7442	0.3903
CP to QN ↑	0.0387	0.0429	1.1138	0.5708
RN to QN ↑	0.0543	0.0580	1.1127	0.5705

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0697	0.0668	0.0668	0.0687
CP ↑	min_pulse_width to CP	0.0338	0.0205	0.0242	0.0242
D ↓	hold_rising to CP	-0.0383	-0.0068	-0.0068	-0.0068
D ↑	hold_rising to CP	-0.0159	0.0031	0.0031	0.0031
D ↓	setup_rising to CP	0.0673	0.0415	0.0411	0.0411
D ↑	setup_rising to CP	0.0463	0.0242	0.0242	0.0242
RN ↓	min_pulse_width to RN	0.0469	0.0474	0.0566	0.0588
RN ↑	recovery_rising to CP	0.0126	0.0127	0.0127	0.0127
RN ↑	removal_rising to CP	-0.0076	-0.0023	-0.0027	-0.0027
TE ↓	hold_rising to CP	-0.0230	-0.0046	-0.0021	-0.0021
TE ↑	hold_rising to CP	-0.0260	-0.0144	-0.0144	-0.0144
TE ↓	setup_rising to CP	0.0583	0.0432	0.0432	0.0432
TE ↑	setup_rising to CP	0.0998	0.0810	0.0810	0.0810
TI ↓	hold_rising to CP	-0.0771	-0.0367	-0.0367	-0.0367
TI ↑	hold_rising to CP	-0.0312	-0.0137	-0.0139	-0.0139
TI ↓	setup_rising to CP	0.1083	0.0762	0.0818	0.0818
TI ↑	setup_rising to CP	0.0554	0.0396	0.0396	0.0396

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.536e-04	5.347e-09
X8_P0	2.727e-04	5.120e-09
X17_P0	3.562e-04	5.286e-09
X33_P0	4.345e-04	5.617e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.917e-03	5.959e-03	5.971e-03	5.977e-03

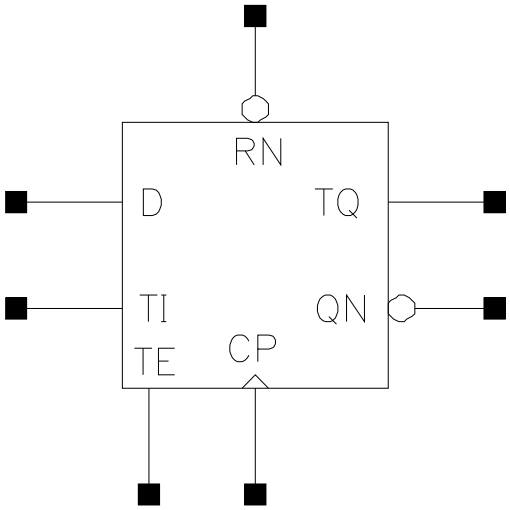
Clock 100Mhz Data 25Mhz	8.922e-03	8.937e-03	9.903e-03	1.107e-02
Clock 100Mhz Data 50Mhz	1.193e-02	1.191e-02	1.384e-02	1.616e-02
Clock = 0 Data 100Mhz	7.158e-03	6.497e-03	6.284e-03	6.178e-03
Clock = 1 Data 100Mhz	1.767e-03	9.203e-04	6.383e-04	4.973e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

RN	0.0010	0.0007	0.0008	0.0008
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0548	0.0477	2.7134	1.5324
CP to QN ↑	0.0694	0.0394	3.9450	2.2653
CP to TQ ↓	0.0481	0.0262	3.4308	2.8470
CP to TQ ↑	0.0458	0.0377	6.6795	6.2038
RN to QN ↑	0.0507	0.0526	3.9970	2.2588
RN to TQ ↓	0.0376	0.0437	3.0512	2.7827
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0494	0.0537	0.7604	0.3994
CP to QN ↑	0.0399	0.0422	1.1357	0.5732
CP to TQ ↓	0.0273	0.0281	3.5293	3.4589
CP to TQ ↑	0.0375	0.0384	5.8424	5.9312
RN to QN ↑	0.0556	0.0573	1.1364	0.5737
RN to TQ ↓	0.0446	0.0450	3.4599	3.3840

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0697	0.0668	0.0692	0.0692
CP ↑	min_pulse_width to CP	0.0483	0.0205	0.0205	0.0242
D ↓	hold_rising to CP	-0.0383	-0.0068	-0.0068	-0.0068
D ↑	hold_rising to CP	-0.0159	0.0031	0.0031	0.0031
D ↓	setup_rising to CP	0.0673	0.0415	0.0411	0.0411
D ↑	setup_rising to CP	0.0463	0.0242	0.0242	0.0242
RN ↓	min_pulse_width to RN	0.0518	0.0518	0.0518	0.0566
RN ↑	recovery_rising to CP	0.0148	0.0127	0.0127	0.0127
RN ↑	removal_rising to CP	-0.0100	-0.0027	-0.0027	-0.0027
TE ↓	hold_rising to CP	-0.0230	-0.0046	-0.0046	-0.0021
TE ↑	hold_rising to CP	-0.0260	-0.0144	-0.0144	-0.0144
TE ↓	setup_rising to CP	0.0583	0.0432	0.0432	0.0432
TE ↑	setup_rising to CP	0.0998	0.0810	0.0810	0.0810
TI ↓	hold_rising to CP	-0.0776	-0.0367	-0.0367	-0.0367
TI ↑	hold_rising to CP	-0.0312	-0.0139	-0.0137	-0.0137
TI ↓	setup_rising to CP	0.1083	0.0818	0.0818	0.0818
TI ↑	setup_rising to CP	0.0554	0.0396	0.0435	0.0435

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.732e-04	5.451e-09
X8_P0	2.888e-04	5.120e-09
X17_P0	3.426e-04	5.451e-09
X33_P0	4.320e-04	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

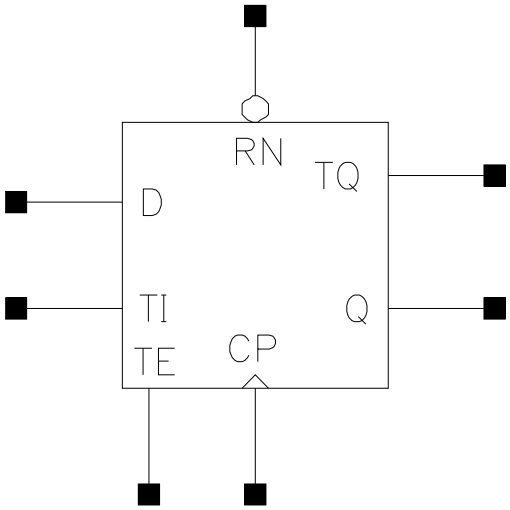
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.920e-03	5.959e-03	5.998e-03	6.019e-03
Clock 100Mhz Data 25Mhz	9.402e-03	9.197e-03	9.804e-03	1.120e-02
Clock 100Mhz Data 50Mhz	1.288e-02	1.244e-02	1.361e-02	1.638e-02
Clock = 0 Data 100Mhz	7.148e-03	6.494e-03	6.276e-03	6.167e-03
Clock = 1 Data 100Mhz	1.767e-03	9.205e-04	6.383e-04	4.972e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

RN	0.0009	0.0009	0.0008	0.0008
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0585	0.0316	3.4168	1.5755
CP to Q ↑	0.0474	0.0394	4.6750	2.3361
CP to TQ ↓	0.0544	0.0311	4.2828	3.7394
CP to TQ ↑	0.0490	0.0411	8.8941	8.1249
RN to Q ↓	0.0417	0.0475	3.0350	1.5336
RN to TQ ↓	0.0393	0.0472	3.8559	3.6550
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0453	0.0495	0.7546	0.3957
CP to Q ↑	0.0557	0.0592	1.1081	0.5660
CP to TQ ↓	0.0468	0.0519	3.5709	3.6378
CP to TQ ↑	0.0590	0.0644	7.9724	8.0151
RN to Q ↓	0.0561	0.0605	0.7547	0.3961
RN to TQ ↓	0.0576	0.0628	3.5703	3.6360

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0697	0.0668	0.0668	0.0668
CP ↑	min_pulse_width to CP	0.0531	0.0242	0.0205	0.0205
D ↓	hold_rising to CP	-0.0383	-0.0068	-0.0068	-0.0068
D ↑	hold_rising to CP	-0.0159	0.0031	0.0031	0.0031
D ↓	setup_rising to CP	0.0673	0.0415	0.0415	0.0415
D ↑	setup_rising to CP	0.0463	0.0242	0.0242	0.0242
RN ↓	min_pulse_width to RN	0.0518	0.0588	0.0496	0.0496
RN ↑	recovery_rising to CP	0.0126	0.0127	0.0127	0.0127
RN ↑	removal_rising to CP	-0.0076	-0.0024	-0.0027	-0.0027
TE ↓	hold_rising to CP	-0.0230	-0.0021	-0.0046	-0.0046
TE ↑	hold_rising to CP	-0.0264	-0.0144	-0.0144	-0.0144
TE ↓	setup_rising to CP	0.0583	0.0432	0.0432	0.0432
TE ↑	setup_rising to CP	0.0998	0.0810	0.0810	0.0810
TI ↓	hold_rising to CP	-0.0776	-0.0367	-0.0367	-0.0367
TI ↑	hold_rising to CP	-0.0271	-0.0139	-0.0137	-0.0137
TI ↓	setup_rising to CP	0.1124	0.0818	0.0818	0.0818
TI ↑	setup_rising to CP	0.0554	0.0396	0.0396	0.0396

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.523e-04	5.451e-09
X8_P0	2.748e-04	5.120e-09
X17_P0	3.600e-04	5.451e-09
X33_P0	4.326e-04	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

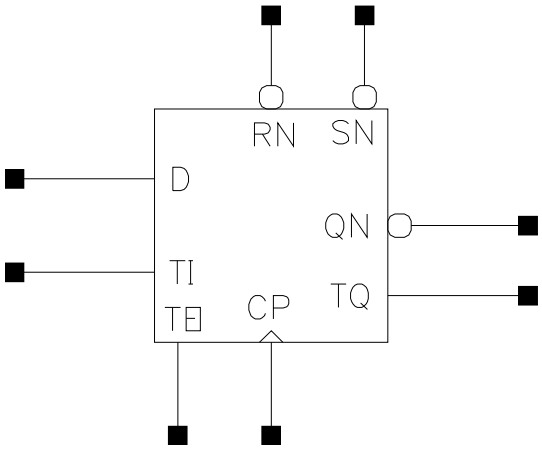
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.954e-03	5.977e-03	5.984e-03	5.987e-03
Clock 100Mhz Data 25Mhz	9.629e-03	9.286e-03	1.023e-02	1.146e-02
Clock 100Mhz Data 50Mhz	1.330e-02	1.260e-02	1.447e-02	1.693e-02
Clock = 0 Data 100Mhz	7.154e-03	6.498e-03	6.279e-03	6.169e-03
Clock = 1 Data 100Mhz	1.768e-03	9.211e-04	6.388e-04	4.978e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.352	5.2224
X17_P0	1.200	4.488	5.3856
X33_P0	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0009

SN	0.0013	0.0013	0.0013
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0531	0.0566	1.4824	0.7619
CP to QN ↑	0.0405	0.0428	2.1932	1.1123
CP to TQ ↓	0.0305	0.0304	4.3546	4.3598
CP to TQ ↑	0.0440	0.0441	10.1855	10.2012
RN to QN ↓	0.0486	0.0527	1.4867	0.7628
RN to QN ↑	0.0480	0.0499	2.1911	1.1110
RN to TQ ↓	0.0389	0.0389	4.2952	4.2988
RN to TQ ↑	0.0386	0.0385	10.2862	10.2894
SN to QN ↓	0.0544	0.0579	1.4809	0.7623
SN to TQ ↑	0.0456	0.0456	10.1766	10.1881
	X33_P0		**X33_P0**	
CP to QN ↓	0.0651		0.4020	
CP to QN ↑	0.0481		0.5696	
CP to TQ ↓	0.0305		4.3707	
CP to TQ ↑	0.0441		10.2236	
RN to QN ↓	0.0621		0.4022	
RN to QN ↑	0.0548		0.5693	
RN to TQ ↓	0.0389		4.3111	
RN to TQ ↑	0.0385		10.3268	
SN to QN ↓	0.0663		0.4027	
SN to TQ ↑	0.0457		10.2116	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0716	0.0716	0.0716
CP ↑	min_pulse_width to CP	0.0242	0.0242	0.0253
D ↓	hold_rising to CP	-0.0068	-0.0068	-0.0068
D ↑	hold_rising to CP	0.0031	0.0031	0.0031
D ↓	setup_rising to CP	0.0463	0.0463	0.0463
D ↑	setup_rising to CP	0.0242	0.0242	0.0242
RN ↓	min_pulse_width to RN	0.0566	0.0566	0.0615
RN ↑	non_seq_hold_rising to SN	-0.0187	-0.0187	-0.0187
RN ↑	non_seq_setup_rising to SN	0.0473	0.0473	0.0473
RN ↑	recovery_rising to CP	0.0197	0.0197	0.0197
RN ↑	removal_rising to CP	-0.0096	-0.0096	-0.0096
SN ↓	min_pulse_width to SN	0.0522	0.0522	0.0549
SN ↑	recovery_rising to CP	0.0004	0.0004	0.0004
SN ↑	removal_rising to CP	0.0238	0.0238	0.0238

TE ↓	hold_rising to CP	-0.0046	-0.0046	-0.0046
TE ↑	hold_rising to CP	-0.0144	-0.0144	-0.0144
TE ↓	setup_rising to CP	0.0463	0.0463	0.0463
TE ↑	setup_rising to CP	0.0859	0.0859	0.0859
TI ↓	hold_rising to CP	-0.0423	-0.0423	-0.0423
TI ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
TI ↓	setup_rising to CP	0.0826	0.0826	0.0826
TI ↑	setup_rising to CP	0.0437	0.0437	0.0437

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	3.192e-04	5.800e-09
X17_P0	3.629e-04	5.966e-09
X33_P0	4.411e-04	6.297e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

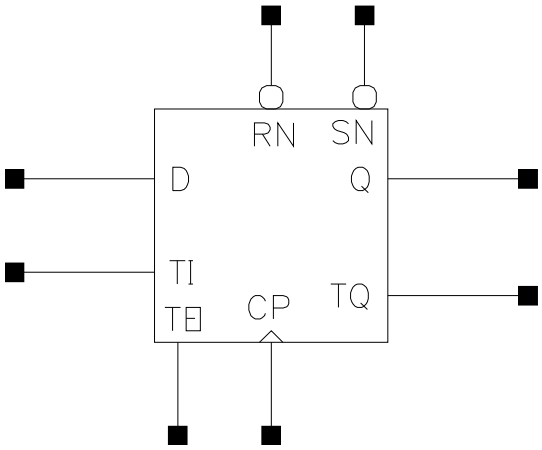
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	6.301e-03	6.301e-03	6.301e-03
Clock 100Mhz Data 25Mhz	9.543e-03	1.014e-02	1.182e-02
Clock 100Mhz Data 50Mhz	1.278e-02	1.397e-02	1.734e-02
Clock = 0 Data 100Mhz	6.010e-03	6.009e-03	6.010e-03
Clock = 1 Data 100Mhz	7.432e-05	7.462e-05	7.467e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.216	5.0592
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0009

SN	0.0013	0.0013	0.0013
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0343	0.0386	1.5302	0.7922
CP to Q ↑	0.0435	0.0464	2.2438	1.1431
CP to TQ ↓	0.0342	0.0384	4.4329	4.4956
CP to TQ ↑	0.0473	0.0522	10.0961	10.1626
RN to Q ↓	0.0412	0.0437	1.4880	0.7662
RN to Q ↑	0.0457	0.0478	2.2323	1.1345
RN to TQ ↓	0.0413	0.0439	4.3476	4.3848
RN to TQ ↑	0.0492	0.0529	10.0429	10.1103
SN to Q ↑	0.0448	0.0471	2.2344	1.1346
SN to TQ ↑	0.0482	0.0520	10.0604	10.1317
	X33_P0		**X33_P0**	
CP to Q ↓	0.0495		0.4226	
CP to Q ↑	0.0538		0.5919	
CP to TQ ↓	0.0461		4.6660	
CP to TQ ↑	0.0612		10.2863	
RN to Q ↓	0.0507		0.4053	
RN to Q ↑	0.0535		0.5857	
RN to TQ ↓	0.0485		4.4998	
RN to TQ ↑	0.0596		10.2189	
SN to Q ↑	0.0530		0.5859	
SN to TQ ↑	0.0590		10.2375	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0716	0.0716	0.0716
CP ↑	min_pulse_width to CP	0.0253	0.0301	0.0434
D ↓	hold_rising to CP	-0.0068	-0.0068	-0.0068
D ↑	hold_rising to CP	0.0031	0.0031	0.0031
D ↓	setup_rising to CP	0.0463	0.0463	0.0463
D ↑	setup_rising to CP	0.0273	0.0273	0.0273
RN ↓	min_pulse_width to RN	0.0637	0.0735	0.0979
RN ↑	non_seq_hold_rising to SN	-0.0237	-0.0286	-0.0360
RN ↑	non_seq_setup_rising to SN	0.0451	0.0451	0.0600
RN ↑	recovery_rising to CP	0.0175	0.0175	0.0175
RN ↑	removal_rising to CP	-0.0075	-0.0075	-0.0075
SN ↓	min_pulse_width to SN	0.0549	0.0598	0.0745
SN ↑	recovery_rising to CP	0.0004	0.0004	0.0029
SN ↑	removal_rising to CP	0.0238	0.0235	0.0235

TE ↓	hold_rising to CP	-0.0046	-0.0046	-0.0046
TE ↑	hold_rising to CP	-0.0144	-0.0144	-0.0144
TE ↓	setup_rising to CP	0.0463	0.0463	0.0463
TE ↑	setup_rising to CP	0.0859	0.0859	0.0859
TI ↓	hold_rising to CP	-0.0423	-0.0423	-0.0423
TI ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
TI ↓	setup_rising to CP	0.0826	0.0867	0.0867
TI ↑	setup_rising to CP	0.0437	0.0437	0.0437

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	3.107e-04	5.628e-09
X17_P0	3.513e-04	5.794e-09
X33_P0	4.263e-04	6.125e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

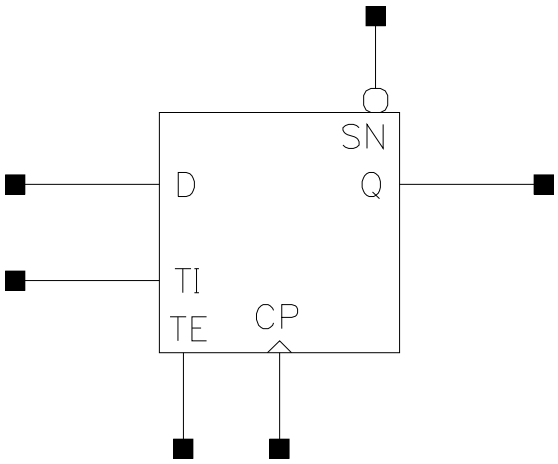
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	6.292e-03	6.293e-03	6.294e-03
Clock 100Mhz Data 25Mhz	9.568e-03	1.046e-02	1.300e-02
Clock 100Mhz Data 50Mhz	1.284e-02	1.463e-02	1.970e-02
Clock = 0 Data 100Mhz	6.008e-03	6.009e-03	6.009e-03
Clock = 1 Data 100Mhz	7.433e-05	7.409e-05	7.437e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0014	0.0014	0.0014	0.0014
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0009			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0516	0.0298	3.2308	1.5223
CP to Q ↑	0.0461	0.0395	4.5217	2.2341
SN to Q ↑	0.0324	0.0343	4.4147	2.2146
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
CP to Q ↓	0.0428	0.0450	0.7447	0.5156
CP to Q ↑	0.0553	0.0571	1.1032	0.7497
SN to Q ↑	0.0505	0.0524	1.1030	0.7495
	X33_P0		**X33_P0**	
CP to Q ↓	0.0468		0.3913	
CP to Q ↑	0.0585		0.5636	
SN to Q ↑	0.0537		0.5636	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.0745	0.0746	0.0746	0.0746
CP ↑	min_pulse_width to CP	0.0434	0.0242	0.0193	0.0193
D ↓	hold_rising to CP	-0.0376	-0.0092	-0.0092	-0.0092
D ↑	hold_rising to CP	-0.0166	0.0057	0.0057	0.0057
D ↓	setup_rising to CP	0.0729	0.0459	0.0463	0.0463
D ↑	setup_rising to CP	0.0410	0.0221	0.0221	0.0221
SN ↓	min_pulse_width to SN	0.0376	0.0425	0.0376	0.0376
SN ↑	recovery_rising to CP	0.0004	0.0029	0.0029	0.0029
SN ↑	removal_rising to CP	0.0190	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0286	-0.0039	-0.0039	-0.0039
TE ↑	hold_rising to CP	-0.0208	-0.0091	-0.0091	-0.0088
TE ↓	setup_rising to CP	0.0576	0.0438	0.0438	0.0438
TE ↑	setup_rising to CP	0.1047	0.0855	0.0855	0.0855
TI ↓	hold_rising to CP	-0.0825	-0.0472	-0.0472	-0.0472
TI ↑	hold_rising to CP	-0.0256	-0.0083	-0.0083	-0.0083
TI ↓	setup_rising to CP	0.1132	0.0867	0.0867	0.0867
TI ↑	setup_rising to CP	0.0520	0.0347	0.0347	0.0347
		X33_P0			

CP ↓	min_pulse_width to CP	0.0746			
CP ↑	min_pulse_width to CP	0.0193			
D ↓	hold_rising to CP	-0.0092			
D ↑	hold_rising to CP	0.0057			
D ↓	setup_rising to CP	0.0463			
D ↑	setup_rising to CP	0.0221			
SN ↓	min_pulse_width to SN	0.0376			
SN ↑	recovery_rising to CP	0.0029			
SN ↑	removal_rising to CP	0.0239			
TE ↓	hold_rising to CP	-0.0039			
TE ↑	hold_rising to CP	-0.0091			
TE ↓	setup_rising to CP	0.0438			
TE ↑	setup_rising to CP	0.0855			
TI ↓	hold_rising to CP	-0.0472			
TI ↑	hold_rising to CP	-0.0083			
TI ↓	setup_rising to CP	0.0867			
TI ↑	setup_rising to CP	0.0347			

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.516e-04	5.286e-09
X8_P0	2.776e-04	5.120e-09
X17_P0	3.610e-04	5.451e-09
X25_P0	4.003e-04	5.617e-09
X33_P0	4.393e-04	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	5.818e-03	5.936e-03	5.976e-03	5.995e-03
Clock 100Mhz Data 25Mhz	9.105e-03	9.077e-03	9.960e-03	1.054e-02
Clock 100Mhz Data 50Mhz	1.239e-02	1.222e-02	1.394e-02	1.508e-02
Clock = 0 Data 100Mhz	6.864e-03	6.385e-03	6.226e-03	6.147e-03
Clock = 1 Data 100Mhz	1.768e-03	9.210e-04	6.387e-04	4.977e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	6.007e-03			

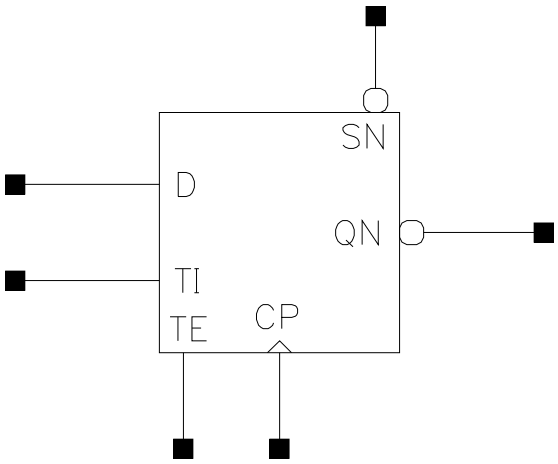
Clock 100Mhz Data 25Mhz	1.109e-02			
Clock 100Mhz Data 50Mhz	1.618e-02			
Clock = 0 Data 100Mhz	6.099e-03			
Clock = 1 Data 100Mhz	4.130e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0014	0.0014	0.0014	0.0014
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0009			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0511	0.0463	2.7051	1.4553
CP to QN ↑	0.0534	0.0347	4.3757	2.1852
SN to QN ↓	0.0389	0.0416	2.6992	1.4536
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
CP to QN ↓	0.0489	0.0516	0.7467	0.5169
CP to QN ↑	0.0408	0.0433	1.1031	0.7502
SN to QN ↓	0.0429	0.0454	0.7458	0.5160
	X33_P0		**X33_P0**	
CP to QN ↓	0.0539		0.3922	
CP to QN ↑	0.0453		0.5636	
SN to QN ↓	0.0475		0.3918	

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.0727	0.0746	0.0746	0.0746
CP ↑	min_pulse_width to CP	0.0338	0.0193	0.0242	0.0242
D ↓	hold_rising to CP	-0.0376	-0.0092	-0.0092	-0.0092
D ↑	hold_rising to CP	-0.0166	0.0057	0.0057	0.0057
D ↓	setup_rising to CP	0.0729	0.0459	0.0459	0.0460
D ↑	setup_rising to CP	0.0410	0.0221	0.0221	0.0221
SN ↓	min_pulse_width to SN	0.0327	0.0376	0.0425	0.0425
SN ↑	recovery_rising to CP	0.0004	0.0029	0.0029	0.0029
SN ↑	removal_rising to CP	0.0190	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0286	-0.0039	-0.0042	-0.0039
TE ↑	hold_rising to CP	-0.0208	-0.0091	-0.0091	-0.0091
TE ↓	setup_rising to CP	0.0576	0.0438	0.0438	0.0438
TE ↑	setup_rising to CP	0.1047	0.0855	0.0855	0.0855
TI ↓	hold_rising to CP	-0.0825	-0.0472	-0.0472	-0.0472
TI ↑	hold_rising to CP	-0.0256	-0.0083	-0.0083	-0.0083
TI ↓	setup_rising to CP	0.1132	0.0867	0.0867	0.0867
TI ↑	setup_rising to CP	0.0520	0.0347	0.0347	0.0347
		X33_P0			

CP ↓	min_pulse_width to CP	0.0746			
CP ↑	min_pulse_width to CP	0.0242			
D ↓	hold_rising to CP	-0.0092			
D ↑	hold_rising to CP	0.0057			
D ↓	setup_rising to CP	0.0460			
D ↑	setup_rising to CP	0.0221			
SN ↓	min_pulse_width to SN	0.0425			
SN ↑	recovery_rising to CP	0.0029			
SN ↑	removal_rising to CP	0.0239			
TE ↓	hold_rising to CP	-0.0039			
TE ↑	hold_rising to CP	-0.0091			
TE ↓	setup_rising to CP	0.0438			
TE ↑	setup_rising to CP	0.0855			
TI ↓	hold_rising to CP	-0.0472			
TI ↑	hold_rising to CP	-0.0083			
TI ↓	setup_rising to CP	0.0867			
TI ↑	setup_rising to CP	0.0347			

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.450e-04	5.286e-09
X8_P0	2.691e-04	5.120e-09
X17_P0	3.555e-04	5.451e-09
X25_P0	3.916e-04	5.617e-09
X33_P0	4.279e-04	5.782e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	5.820e-03	5.945e-03	5.982e-03	6.001e-03
Clock 100Mhz Data 25Mhz	8.757e-03	8.909e-03	1.012e-02	1.073e-02
Clock 100Mhz Data 50Mhz	1.170e-02	1.187e-02	1.426e-02	1.546e-02
Clock = 0 Data 100Mhz	6.864e-03	6.389e-03	6.228e-03	6.149e-03
Clock = 1 Data 100Mhz	1.768e-03	9.211e-04	6.388e-04	4.977e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	6.012e-03			

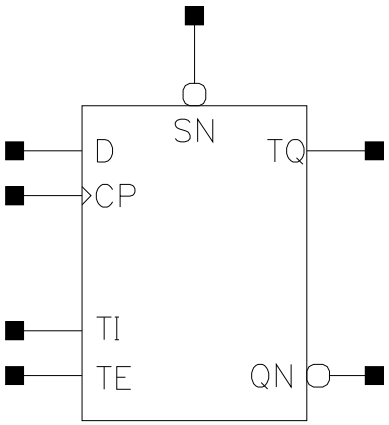
Clock 100Mhz Data 25Mhz	1.136e-02			
Clock 100Mhz Data 50Mhz	1.670e-02			
Clock = 0 Data 100Mhz	6.101e-03			
Clock = 1 Data 100Mhz	4.131e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.216	5.0592
X8_P0	1.200	4.080	4.8960
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0016	0.0015	0.0015
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0585	0.0483	2.7053	1.4639
CP to QN ↑	0.0687	0.0392	4.3317	2.2344
CP to TQ ↓	0.0495	0.0264	3.8367	3.2831
CP to TQ ↑	0.0457	0.0367	5.9490	5.8159
SN to QN ↓	0.0410	0.0424	2.7009	1.4621
SN to TQ ↑	0.0294	0.0306	5.8628	5.8249
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0487	0.0537	0.7681	0.3879
CP to QN ↑	0.0438	0.0485	1.1167	0.5693
CP to TQ ↓	0.0326	0.0325	3.4072	3.4100
CP to TQ ↑	0.0413	0.0412	5.8492	5.8626
SN to QN ↓	0.0438	0.0486	0.7674	0.3875
SN to TQ ↑	0.0363	0.0362	5.8337	5.8501

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0745	0.0746	0.0746	0.0746
CP ↑	min_pulse_width to CP	0.0483	0.0205	0.0242	0.0253
D ↓	hold_rising to CP	-0.0376	-0.0092	-0.0092	-0.0092
D ↑	hold_rising to CP	-0.0166	0.0057	0.0057	0.0057
D ↓	setup_rising to CP	0.0729	0.0459	0.0459	0.0459
D ↑	setup_rising to CP	0.0410	0.0221	0.0221	0.0221
SN ↓	min_pulse_width to SN	0.0305	0.0327	0.0354	0.0354
SN ↑	recovery_rising to CP	0.0004	0.0004	0.0029	0.0029
SN ↑	removal_rising to CP	0.0190	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0286	-0.0039	-0.0039	-0.0039
TE ↑	hold_rising to CP	-0.0208	-0.0091	-0.0091	-0.0091
TE ↓	setup_rising to CP	0.0576	0.0438	0.0438	0.0438
TE ↑	setup_rising to CP	0.1047	0.0855	0.0855	0.0855
TI ↓	hold_rising to CP	-0.0825	-0.0472	-0.0472	-0.0472
TI ↑	hold_rising to CP	-0.0256	-0.0083	-0.0083	-0.0083
TI ↓	setup_rising to CP	0.1132	0.0867	0.0867	0.0867
TI ↑	setup_rising to CP	0.0520	0.0347	0.0347	0.0347

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.776e-04	5.617e-09
X8_P0	3.014e-04	5.451e-09
X17_P0	3.880e-04	5.782e-09
X33_P0	4.604e-04	6.114e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

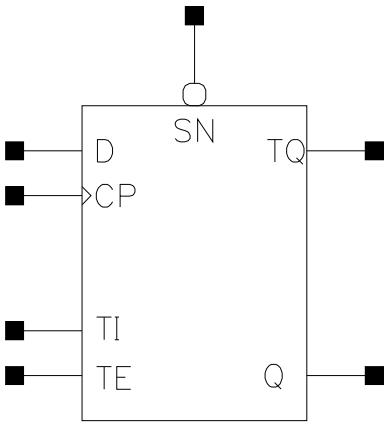
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.824e-03	5.944e-03	5.984e-03	6.004e-03
Clock 100Mhz Data 25Mhz	9.375e-03	9.258e-03	1.042e-02	1.166e-02
Clock 100Mhz Data 50Mhz	1.293e-02	1.257e-02	1.486e-02	1.732e-02
Clock = 0 Data 100Mhz	6.876e-03	6.397e-03	6.238e-03	6.158e-03
Clock = 1 Data 100Mhz	1.769e-03	9.210e-04	6.386e-04	4.974e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.944	4.7328
X17_P0	1.200	4.216	5.0592
X33_P0	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0014	0.0014	0.0014
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0592	0.0323	3.3094	1.5525
CP to Q ↑	0.0492	0.0413	4.5406	2.2636
CP to TQ ↓	0.0595	0.0327	4.7224	3.7621
CP to TQ ↑	0.0482	0.0450	5.9924	8.2026
SN to Q ↑	0.0314	0.0355	4.4344	2.2413
SN to TQ ↑	0.0306	0.0385	5.8826	8.1683
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0436	0.0479	0.7648	0.3977
CP to Q ↑	0.0560	0.0594	1.1088	0.5656
CP to TQ ↓	0.0450	0.0501	3.5673	3.6317
CP to TQ ↑	0.0593	0.0645	7.9782	8.0220
SN to Q ↑	0.0512	0.0546	1.1092	0.5655
SN to TQ ↑	0.0545	0.0597	7.9773	8.0183

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0745	0.0746	0.0746	0.0727
CP ↑	min_pulse_width to CP	0.0531	0.0242	0.0193	0.0193
D ↓	hold_rising to CP	-0.0376	-0.0092	-0.0092	-0.0092
D ↑	hold_rising to CP	-0.0166	0.0057	0.0057	0.0057
D ↓	setup_rising to CP	0.0729	0.0459	0.0463	0.0463
D ↑	setup_rising to CP	0.0407	0.0221	0.0221	0.0221
SN ↓	min_pulse_width to SN	0.0305	0.0452	0.0376	0.0376
SN ↑	recovery_rising to CP	0.0004	0.0029	0.0029	0.0029
SN ↑	removal_rising to CP	0.0190	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0286	-0.0042	-0.0039	-0.0039
TE ↑	hold_rising to CP	-0.0208	-0.0091	-0.0088	-0.0091
TE ↓	setup_rising to CP	0.0576	0.0438	0.0438	0.0438
TE ↑	setup_rising to CP	0.1047	0.0855	0.0855	0.0855
TI ↓	hold_rising to CP	-0.0825	-0.0472	-0.0472	-0.0472
TI ↑	hold_rising to CP	-0.0256	-0.0083	-0.0083	-0.0083
TI ↓	setup_rising to CP	0.1132	0.0867	0.0867	0.0867
TI ↑	setup_rising to CP	0.0520	0.0347	0.0347	0.0347

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	2.761e-04	5.451e-09
X8_P0	2.924e-04	5.286e-09
X17_P0	3.766e-04	5.617e-09
X33_P0	4.547e-04	5.948e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

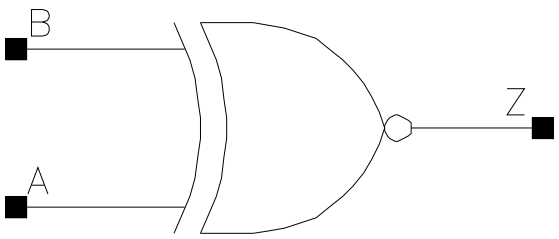
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	5.821e-03	5.937e-03	5.976e-03	5.995e-03
Clock 100Mhz Data 25Mhz	9.601e-03	9.407e-03	1.020e-02	1.145e-02
Clock 100Mhz Data 50Mhz	1.338e-02	1.288e-02	1.443e-02	1.691e-02
Clock = 0 Data 100Mhz	6.877e-03	6.392e-03	6.232e-03	6.151e-03
Clock = 1 Data 100Mhz	1.769e-03	9.213e-04	6.389e-04	4.977e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P0	X8_P0	X17_P0	X25_P0
A	0.0016	0.0007	0.0010	0.0015
B	0.0015	0.0015	0.0018	0.0025
	X33_P0			
A	0.0017			
B	0.0029			

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X8_P0**	**X6_P0**	**X8_P0**
A to Z ↓	0.0147	0.0318	2.5527	1.5779
A to Z ↑	0.0155	0.0302	3.4356	2.3089
B to Z ↓	0.0137	0.0224	2.5537	1.5622
B to Z ↑	0.0163	0.0216	3.4447	2.2989
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
A to Z ↓	0.0306	0.0310	0.7743	0.5320
A to Z ↑	0.0282	0.0283	1.1327	0.7551

B to Z ↓	0.0231	0.0224	0.7708	0.5304
B to Z ↑	0.0220	0.0213	1.1294	0.7526
	X33_P0		**X33_P0**	
A to Z ↓	0.0298		0.3989	
A to Z ↑	0.0277		0.5679	
B to Z ↓	0.0218		0.3978	
B to Z ↑	0.0213		0.5665	

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X6_P0	1.193e-04	1.642e-09
X8_P0	1.755e-04	2.139e-09
X17_P0	2.675e-04	2.304e-09
X25_P0	4.292e-04	3.298e-09
X33_P0	5.532e-04	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	3.831e-03	7.164e-03	1.084e-02	1.703e-02
B to Z	3.764e-03	5.316e-03	8.783e-03	1.349e-02
	X33_P0			
A to Z	2.114e-02			
B to Z	1.727e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

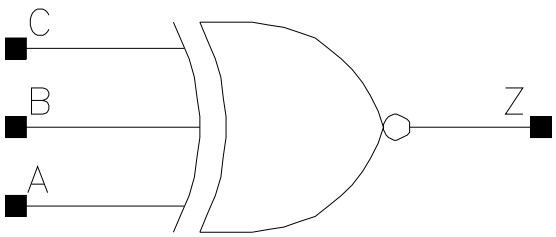
Pin Cycle (vdds)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	1.585e-06	2.970e-08	7.313e-07	6.465e-07
B to Z	5.759e-07	1.001e-06	5.601e-07	1.726e-07
	X33_P0			
A to Z	-7.457e-07			
B to Z	-2.254e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	2.176	2.6112
X16_P0	1.200	2.720	3.2640
X25_P0	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X16_P0	X25_P0
A	0.0028	0.0024	0.0029	0.0043
B	0.0031	0.0022	0.0029	0.0040
C	0.0019	0.0007	0.0007	0.0008

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0223	0.0371	2.9877	1.6555
A to Z ↑	0.0221	0.0344	4.9042	2.2837
B to Z ↓	0.0232	0.0375	2.9936	1.6554
B to Z ↑	0.0224	0.0350	4.9047	2.2849
C to Z ↓	0.0232	0.0498	2.9994	1.6539
C to Z ↑	0.0218	0.0469	4.9073	2.2836
	X16_P0	**X25_P0**	**X16_P0**	**X25_P0**
A to Z ↓	0.0379	0.0381	0.8484	0.5432
A to Z ↑	0.0376	0.0377	1.1957	0.7561
B to Z ↓	0.0385	0.0391	0.8483	0.5436

B to Z ↑	0.0383	0.0390	1.1961	0.7565
C to Z ↓	0.0532	0.0571	0.8478	0.5429
C to Z ↑	0.0524	0.0566	1.1961	0.7563

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	1.231e-04	2.967e-09
X8_P0	1.462e-04	3.132e-09
X16_P0	2.348e-04	3.795e-09
X25_P0	3.316e-04	5.286e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	3.855e-03	5.540e-03	9.431e-03	1.441e-02
B to Z	3.935e-03	5.529e-03	9.473e-03	1.455e-02
C to Z	3.909e-03	8.189e-03	1.256e-02	1.905e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

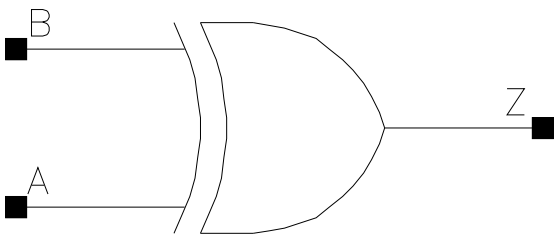
Pin Cycle (vdds)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	7.030e-07	1.933e-07	1.014e-07	2.472e-07
B to Z	8.376e-07	1.891e-07	2.147e-07	2.630e-07
C to Z	4.075e-07	3.053e-07	1.318e-07	3.615e-07

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.224	1.4688
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.224	1.4688
X16_P0	1.200	1.360	1.6320
X25_P0	1.200	2.176	2.6112
X31_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X16_P0
A	0.0008	0.0015	0.0010	0.0011
B	0.0012	0.0014	0.0015	0.0016
	X25_P0	X31_P0		
A	0.0015	0.0019		
B	0.0026	0.0033		

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0288	0.0141	2.7586	2.0162
A to Z ↑	0.0283	0.0165	4.2841	4.3439
B to Z ↓	0.0212	0.0150	2.7390	2.0316
B to Z ↑	0.0212	0.0153	4.2787	4.3430
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0259	0.0276	1.5449	0.7969

A to Z ↑	0.0247	0.0264	2.2441	1.1338
B to Z ↓	0.0205	0.0216	1.5353	0.7935
B to Z ↑	0.0197	0.0212	2.2449	1.1321
	X25_P0	**X31_P0**	**X25_P0**	**X31_P0**
A to Z ↓	0.0292	0.0278	0.5282	0.4220
A to Z ↑	0.0277	0.0266	0.7524	0.6061
B to Z ↓	0.0220	0.0207	0.5277	0.4214
B to Z ↑	0.0211	0.0204	0.7522	0.6059

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	1.491e-04	1.973e-09
X6_P0	1.237e-04	1.642e-09
X8_P0	2.123e-04	1.973e-09
X16_P0	2.972e-04	2.139e-09
X25_P0	4.197e-04	3.132e-09
X31_P0	5.485e-04	3.298e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	5.340e-03	3.775e-03	6.684e-03	1.016e-02
B to Z	4.334e-03	3.664e-03	5.773e-03	8.831e-03
	X25_P0	X31_P0		
A to Z	1.607e-02	1.990e-02		
B to Z	1.279e-02	1.596e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

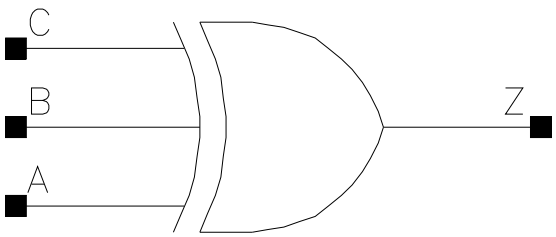
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	-4.195e-08	2.148e-06	7.791e-07	6.050e-07
B to Z	3.469e-08	1.287e-06	1.526e-06	1.004e-06
	X25_P0	X31_P0		
A to Z	-2.126e-07	1.552e-06		
B to Z	-7.512e-07	-9.191e-07		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X24_P0	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X24_P0
A	0.0024	0.0024	0.0029	0.0052
B	0.0025	0.0022	0.0027	0.0043
C	0.0008	0.0016	0.0022	0.0034

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0227	0.0371	3.1537	1.6550
A to Z ↑	0.0222	0.0344	5.3499	2.2811
B to Z ↓	0.0234	0.0375	3.1601	1.6552
B to Z ↑	0.0227	0.0350	5.3482	2.2826
C to Z ↓	0.0400	0.0369	3.1323	1.6557
C to Z ↑	0.0394	0.0343	5.3256	2.2817
	X17_P0	**X24_P0**	**X17_P0**	**X24_P0**
A to Z ↓	0.0346	0.0403	0.7915	0.5695
A to Z ↑	0.0344	0.0313	1.1156	0.7599
B to Z ↓	0.0350	0.0408	0.7917	0.5697

B to Z ↑	0.0350	0.0317	1.1163	0.7602
C to Z ↓	0.0348	0.0399	0.7915	0.5695
C to Z ↑	0.0348	0.0317	1.1155	0.7603

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	1.452e-04	2.967e-09
X8_P0	1.200e-04	2.801e-09
X17_P0	2.069e-04	2.967e-09
X24_P0	3.466e-04	5.120e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	3.674e-03	5.536e-03	9.026e-03	1.518e-02
B to Z	3.747e-03	5.526e-03	9.060e-03	1.521e-02
C to Z	7.225e-03	5.464e-03	9.068e-03	1.520e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	5.096e-07	1.960e-07	2.232e-07	5.161e-07
B to Z	6.589e-07	1.866e-07	3.360e-07	8.005e-07
C to Z	4.387e-07	1.816e-07	1.020e-07	7.052e-07

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