life.augmented

TECHNOLOGY 28FDSOI
- PEX MODELS -
Release Note for StarRC

Version 2.4
03 July 2018

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ABSTRACT

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The intent of this document is to provide information about the starRC module PEX_models_28fd@2.4.

StarRC PEX release are aligned with DRM CMOS028FDSOI rev0.4.7.

1.1 Purpose of the release.

This release is aimed at updating the LB and the StarRC version.
PEX models are aligned on DRM CMOS028FDSOI rev0.4.7.

1.2 Tool version

Synopsys StarRC: n-2017.12-sp3-1

1.3 Qualification plan

This section describes the test-cases used for RCmodels qualification and summarizes the test plan.

1.3.1 Test plan

The models have been qualified:

- by regression vs. the 28FDSOI rev2.3 PEX models
- by comparison vs Raphael simulation for the gate to contact capacitance
- by comparison vs DRM for the LB resistance

1.3.2 Test-cases description

cell	Description	Goal
C_*	5 coupled lines (layer n) between ground planes (layers n-1 & n+1), for different width & space. Dedicated to Capa	Models regression
28LP_*_	5 parallel lines, for different width & space. Dedicated to resistance	Models regression
Via_28LP	Single & double via instantiation between layers n1 & n2=n1+1 Dedicated to via resistance	Models regression
FE_testcase*	Nfet pcell for different transistor width , L and CPP. Dedicated to gate to source capacitance.	Models regression Models accuracy

1.4 Accuracy results

1.4.1 FEOL Capacitance

Rapid3D and StarRC results have been compared to Raphael 3D simulation results. The used testcase is a DOE of NFET with different gate width, length, CPP and neighbouring poly connection. We compared gate to source/drain capacitance, looking at the PEX components only (poly to TS+CA+R0+M1).

The table below shows the correlation results.

#REF!	source	family	device	purpose	GateA UXfloating	width	dw	length	cpp	sa	numco	Raphael	Rapid3D	Rapid3D vs Raphael	Star	StarRCXT vs Raphael	Star vs Rapid3D
test1	Pcell	SG	nfet	Reference	1	0,072	0	0,028	0,1134	0,0679	1	2,07819E-17	1,95E-17	-6%	2,01E-17	-3%	3%
test2	Pcell	SG	nfet	RefWretarg	1	0,072	0,006	0,028	0,1134	0,0679	1	2,16437E-17	1,88E-17	-13%	1,97E-17	-9%	5%
test3	Pcell	SG	nfet	prelayout	1	0,252	0	0,028	0,1134	0,0679	3	3,56465E-17	3,51E-17	-2%	3,18E-17	-11%	-10%
test4	Pcell	SG	nfet	prelayout	1	0,342	0	0,028	0,1134	0,0679	4	4,21772E-17	4,20E-17	0%	3,95E-17	-6%	-6%
test5	Pcell	SG	nfet	prelayout	1	0,432	0	0,028	0,1134	0,0679	5	4,87634E-17	4,95E-17	1%	4,61E-17	-6%	-7%
test6	Pcell	SG	nfet	prelayout	1	0,522	0	0,028	0,1134	0,0679	6	5,53532E-17	5,76E-17	4%	5,27E-17	-5%	-9%
test7	Pcell	SG	nfet	prelayout	1	0,612	0	0,028	0,1134	0,0679	7	6,21427E-17	6,35E-17	2%	5,92E-17	-5%	-7%
test8	Pcell	SG	nfet	prelayout	1	0,702	0	0,028	0,1134	0,0679	8	6,88361E-17	7,12E-17	3%	6,58E-17	-4%	-8%
test9	Pcell	SG	nfet	prelayout	1	0,792	0	0,028	0,1134	0,0679	9	7,54953E-17	7,87E-17	4%	7,23E-17	-4%	-8%
test10	Pcell	SG	nfet	prelayout	1	0,882	0	0,028	0,1134	0,0679	10	8,20019E-17	8,56E-17	4%	7,90E-17	-4%	-8%
test11	Pcell	SG	nfet	prelayout	1	0,972	0	0,028	0,1134	0,0679	11	8,86915E-17	9,30E-17	5%	8,56E-17	-4%	-8%
test12	Pcell	SG	nfet	prelayout	1	1,062	0	0,028	0,1134	0,0679	12	9,53788E-17	9,85E-17	3%	9,20E-17	-4%	-7%
test13	Lidwine - PEX	SG	nfet	minDRM	0	0,4356	0	0,028	0,1134	0,1813	5	4,88296E-17	4,53E-17	-7%	4,19E-17	-14%	-7%
test14	Lidwine - PEX	SG	nfet	CPPstdcell	0	0,4356	0	0,028	0,1224	0,1903	5	4,43519E-17	4,14E-17	-7%	3,87E-17	-13%	-6%
test15	Lidwine - PEX	SG	nfet	PObias10	0	0,1683	0	0,038	0,1224	0,1853	2	3,0087E-17	2,56E-17	-15%	2,44E-17	-19%	-5%
test16	Lidwine - PEX	SG	nfet	POBias10	0	0,4356	0	0,038	0,1224	0,1853	5	5,14899E-17	4,84E-17	-6%	4,32E-17	-16%	-11%
test17	Lidwine - PEX	SG	nfet	OneContact	0	0,4356	0	0,028	0,1224	0,1903	1	2,7206E-17	2,09E-17	-23%	2,16E-17	-21%	3%
test18	Lidwine - PEX	SG	nfet	FatherstContact	0	0,4356	0	0,028	0,2268	0,2938	5	2,12829E-17	1,84E-17	-13%	1,83E-17	-14%	-1%
test19	Lidwine - PEX	SG	nfet	ClosestContact	0	0,4356	0	0,028	0,2268	0,2938	5	4,87497E-17	4,84E-17	-1%	4,23E-17	-13%	-13%
test20	PEX	SG	nfet	postlayout	1	0,702	0	0,028	0,1134	0,0679	8	6,93293E-17	7,27E-17	5%	6,68E-17	-4%	-8%
test21	PEX	SG	nfet	postlayout	1	0,792	0	0,028	0,1134	0,0679	9	7,59926E-17	7,90E-17	4%	7,35E-17	-3%	-7%
test22	PEX	SG	nfet	postlayout	1	0,882	0	0,028	0,1134	0,0679	10	8,25062E-17	8,67E-17	5%	7,96E-17	-4%	-8%
test23	PEX	SG	nfet	postlayout	1	0,972	0	0,028	0,1134	0,0679	11	8,92033E-17	9,46E-17	6%	8,67E-17	-3%	-8%
test24	PEX	SG	nfet	postlayout	1	1,062	0	0,028	0,1134	0,0679	12	9,58406E-17	1,02E-16	6%	9,30E-17	-3%	-8%

Figure 1: NGate to drain accuracy results

Rapid3D and StarRC are showing acceptable correlation results vs Raphael and allow us to validate our FE description in itf.

1.4.2 BEOL

M1 to IB assumptions are fully aligned on 20lpm Beta1000 PDK. This has been validated by regression test. Considering the 20lpm Beta100 as fully qualified, no additional accuracy results on BEOL have been done. Please refer to 20lpm Beta1000 qualification results for details.

For the LB, resistance results have been compared to DRM values:

				R - ST cmos028 PDK_2EFDSOI_RF_rev1.0_star2017_12_beta_NewNxtgrd - 6U1x_2T8x_LB - Star-RCXT (N-2017.12-SP3-VAL-20180521)								
				FuncCmin25	FuncRCmin25	SigCmin25	SigRCmin25	nominal25	FuncCmax25	FuncRCmax25	SigCmax25	SigRCmax25
Layer	length1	width1	space1	total1	total1	total1	total1	total1	total1	total1	total1	total1
LB/-/-	100	12	10	0,131645	0,1024056	0,1303946	0,1068172	0,1154877	0,1024056	0,131645	0,1068172	0,1303946
LB/-/-	100	20	10	0,07818505	0,06204875	0,07749869	0,06449663	0,06929259	0,06204875	0,07818505	0,06449663	0,07749869
LB/-/-	100	4	2	0,4162857	0,2929259	0,4107401	0,3106658	0,3464626	0,2929259	0,4162857	0,3106658	0,4107401
LB/-/-	100	4	4	0,4162857	0,2929259	0,4107401	0,3106658	0,3464626	0,2929259	0,4162857	0,3106658	0,4107401
				DRM								
				FuncCmin25	FuncRCmin25	SigCmin25	SigRCmin25	nominal25	FuncCmax25	FuncRCmax25	SigCmax25	SigRCmax25
Layer	length1	width1	space1	total1	total1	total1	total1	total1	total1	total1	total1	total1
LB/-/-	100	12	10	0,13163162	0,10239574	0,13037904	0,10680582	0,11547619	0,10239574	0,13163162	0,10680582	0,13037904
LB/-/-	100	20	10	0,07817716	0,06204274	0,07748962	0,06448973	0,06928571	0,06204274	0,07817716	0,06448973	0,07748962
LB/-/-	100	4	2	0,41624053	0,29289345	0,41068872	0,31063372	0,34642857	0,29289345	0,41624053	0,31063372	0,41068872
LB/-/-	100	4	4	0,41624053	0,29289345	0,41068872	0,31063372	0,34642857	0,29289345	0,41624053	0,31063372	0,41068872
				vs DRM								
				FuncCmin25	FuncRCmin25	SigCmin25	SigRCmin25	nominal25	FuncCmax25	FuncRCmax25	SigCmax25	SigRCmax25
Layer	length1	width1	space1	total1	total1	total1	total1	total1	total1	total1	total1	total1
LB/-/-	100	12	10	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%
LB/-/-	100	20	10	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%
LB/-/-	100	4	2	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%
LB/-/-	100	4	4	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%	0,0%

Figure 2: LB resistance accuracy results

1.5 Regression tests

1.5.1 FEOL capacitance regression test.

Compare to previous release, StarRCXT release update is impacting gate to poly capacitance. Impact depends on the tescase.

Test_ID	source	family	device	purpose	GateAUXfloati	width	dw	length	cpp	sa	dxyEPI	numco	Rapid3D	Star	Rapid3D vs Prev	StarRCXT vs prev
test1	Pcell	SG	nfet	Reference	1	0,072	0	0,028	0,1134	0,0679	dxyEPI	1	1,95E-17	2,01E-17	0%	2%
test2	Pcell	SG	nfet	RefWretarg	1	0,072	0,006	0,028	0,1134	0,0679	dxyEPI	1	1,88E-17	1,97E-17	-1%	2%
test3	Pcell	SG	nfet	prelayout	1	0,252	0	0,028	0,1134	0,0679	dxyEPI	3	3,51E-17	3,18E-17	-1%	-1%
test4	Pcell	SG	nfet	prelayout	1	0,342	0	0,028	0,1134	0,0679	dxyEPI	4	4,20E-17	3,95E-17	-2%	-2%
test5	Pcell	SG	nfet	prelayout	1	0,432	0	0,028	0,1134	0,0679	dxyEPI	5	4,95E-17	4,61E-17	-1%	-2%
test6	Pcell	SG	nfet	prelayout	1	0,522	0	0,028	0,1134	0,0679	dxyEPI	6	5,76E-17	5,27E-17	0%	-2%
test7	Pcell	SG	nfet	prelayout	1	0,612	0	0,028	0,1134	0,0679	dxyEPI	7	6,35E-17	5,92E-17	-1%	-3%
test8	Pcell	SG	nfet	prelayout	1	0,702	0	0,028	0,1134	0,0679	dxyEPI	8	7,12E-17	6,58E-17	-1%	-2%
test9	Pcell	SG	nfet	prelayout	1	0,792	0	0,028	0,1134	0,0679	dxyEPI	9	7,87E-17	7,23E-17	1%	-3%
test10	Pcell	SG	nfet	prelayout	1	0,882	0	0,028	0,1134	0,0679	dxyEPI	10	8,56E-17	7,90E-17	-1%	-3%
test11	Pcell	SG	nfet	prelayout	1	0,972	0	0,028	0,1134	0,0679	dxyEPI	11	9,30E-17	8,56E-17	0%	-3%
test12	Pcell	SG	nfet	prelayout	1	1,062	0	0,028	0,1134	0,0679	dxyEPI	12	9,85E-17	9,20E-17	0%	-3%
test13	Lidwine - PEX	SG	nfet	minDRM	0	0,4356	0	0,028	0,1134	0,1813	dxyEPI	5	4,53E-17	4,19E-17	0%	2%
test14	Lidwine - PEX	SG	nfet	CPPstdcell	0	0,4356	0	0,028	0,1224	0,1903	dxyEPI	5	4,14E-17	3,87E-17	0%	2%
test15	Lidwine - PEX	SG	nfet	POBias10	0	0,1683	0	0,038	0,1224	0,1853	dxyEPI	2	2,56E-17	2,44E-17	0%	2%
test16	Lidwine - PEX	SG	nfet	POBias10	0	0,4356	0	0,038	0,1224	0,1853	dxyEPI	5	4,84E-17	4,32E-17	0%	2%
test17	Lidwine - PEX	SG	nfet	OneContact	0	0,4356	0	0,028	0,1224	0,1903	dxyEPI	1	2,09E-17	2,16E-17	1%	1%
test19	Lidwine - PEX	SG	nfet	ClosestContact	0	0,4356	0	0,028	0,2268	0,2938	dxyEPI	5	4,84E-17	4,23E-17	1%	2%
test20	PEX	SG	nfet	postlayout	1	0,702	0	0,028	0,1134	0,0679	dxyEPI	8	7,27E-17	6,68E-17	-2%	-2%
test21	PEX	SG	nfet	postlayout	1	0,792	0	0,028	0,1134	0,0679	dxyEPI	9	7,90E-17	7,35E-17	2%	-2%
test22	PEX	SG	nfet	postlayout	1	0,882	0	0,028	0,1134	0,0679	dxyEPI	10	8,67E-17	7,96E-17	-1%	-5%
test23	PEX	SG	nfet	postlayout	1	0,972	0	0,028	0,1134	0,0679	dxyEPI	11	9,46E-17	8,67E-17	1%	-3%
test24	PEX	SG	nfet	postlayout	1	1,062	0	0,028	0,1134	0,0679	dxyEPI	12	1,02E-16	9,30E-17	0%	-2%

Figure 3: gate to source/drain capacitance regression results

1.5.2 BEOL resistance/capacitance regression test.

BEOL capacitance have been checked by regression test vs. previous release.

The full QA report is available on the UPT delivery.