cmos028fdsoi Technology

LVT models

DK1.2_RF_mmW

Comparison with DK1.1_RF_mmW model(s)

Ideal ring oscillators

Please use the bookmark to navigate

General information on LVT models

- Maximum supply voltage is - V.
- Validity domain is defined as follows:
  - ✔ Drawn gate length varies from 30nm to 10um.
  - ✔ Drawn transistor width varies from 0.08um to 10um.
  - ✔ Device temperature varies from -40 °C to 125 °C.

Output parameters definitions

- Model(s): lvtnfet_acc_lvtpfet_acc

lvtnfet_acc_lvtpfet_acc
Electrical characteristics per geometry

lvtnfet_acc_lvtpfet_acc @ w_n=0.42e-6, l_n=30e-9, p_la_n=0, nf_n=2, sa_n=85e9, sb_n=85e-9, sd_n=106e-9, sc_n=56e-9, pcpastrx_top_n=169e-9, pcpastrx_bot_n=57e-9, w_p=0.6e-6, l_p=30e-9, p_la_p=0, nf_p=2, sa_p=85e9, sb_p=85e-9, sd_p=106e-9, sc_p=113e-9, pcpastrx_top_p=169e-9, pcpastrx_bot_p=57e-9, vdd=0.9, temp=25.0

DK1.2_RF_mmW wrt DK1.1_RF_mmW

	SS	TT	FF
Fosc_gate [GHz]	36.39 0.0%	40.75 0.0%	44.97 0.0%
Idyn [µA]	163.2 0.0%	187.8 0.0%	217.4 0.0%
Pdyn [µW]	146.9 0.0%	169 0.0%	195.7 0.0%
Ceff [fF]	4.98 0.0%	5.12 0.0%	5.37 0.0%
Taup [ps]	13.74 0.0%	12.27 0.0%	11.12 0.0%
Istat_gate [nA]	3.55 0.0%	11.97 0.0%	48.15 0.0%
LogIstat_gate []	-8.45 -0.0%	-7.92 -0.0%	-7.32 -0.0%

lvtnfet_acc_lvtpfet_acc @ w_n=0.42e-6, l_n=30e-9, p_la_n=4e-9, nf_n=2, sa_n=85e9, sb_n=85e-9, sd_n=106e-9, sc_n=56e-9, pcpastrx_top_n=169e-9, pcpastrx_bot_n=57e-9, w_p=0.6e-6, l_p=30e-9, p_la_p=4e-9, nf_p=2, sa_p=85e9, sb_p=85e-9, sd_p=106e-9, sc_p=113e-9, pcpastrx_top_p=169e-9, pcpastrx_bot_p=57e-9, vdd=0.9, temp=25.0

DK1.2_RF_mmW wrt DK1.1_RF_mmW

	SS	TT	FF
Fosc_gate [GHz]	33.22 0.0%	36.91 0.0%	40.51 0.0%
Idyn [µA]	150.4 0.0%	171 0.0%	194.2 0.0%
Pdyn [µW]	135.3 0.0%	153.9 0.0%	174.8 0.0%
Ceff [fF]	5.03 0.0%	5.15 0.0%	5.33 0.0%
Taup [ps]	15.05 0.0%	13.55 0.0%	12.34 0.0%
Istat_gate [nA]	1.3 0.0%	3.53 0.0%	11.88 0.0%
LogIstat_gate []	-8.89 -0.0%	-8.45 -0.0%	-7.93 -0.0%

lvtnfet_acc_lvtpfet_acc @ w_n=0.42e-6, l_n=30e-9, p_la_n=10e-9, nf_n=2, sa_n=85e9, sb_n=85e-9, sd_n=106e-9, sc_n=56e-9, pcpastrx_top_n=169e-9, pcpastrx_bot_n=57e-9, w_p=0.6e-6, l_p=30e-9, p_la_p=10e-9, nf_p=2, sa_p=85e9, sb_p=85e-9, sd_p=106e-9, sc_p=113e-9, pcpastrx_top_p=169e-9, pcpastrx_bot_p=57e-9, vdd=0.9, temp=25.0

DK1.2_RF_mmW wrt DK1.1_RF_mmW

	SS	TT	FF
Fosc_gate [GHz]	28.88 0.0%	31.74 0.0%	34.5 0.0%
Idyn [µA]	134 0.0%	150.1 0.0%	167.6 0.0%
Pdyn [µW]	120.6 0.0%	135.1 0.0%	150.8 0.0%
Ceff [fF]	5.16 0.0%	5.25 0.0%	5.4 0.0%
Taup [ps]	17.32 0.0%	15.75 0.0%	14.49 0.0%
Istat_gate [nA]	0.37 0.0%	0.77 0.0%	1.98 0.0%
LogIstat_gate []	-9.43 -0.0%	-9.11 -0.0%	-8.7 -0.0%

lvtnfet_acc_lvtpfet_acc @ w_n=0.42e-6, l_n=30e-9, p_la_n=16e-9, nf_n=2, sa_n=85e9, sb_n=85e-9, sd_n=106e-9, sc_n=56e-9, pcpastrx_top_n=169e-9, pcpastrx_bot_n=57e-9, w_p=0.6e-6, l_p=30e-9, p_la_p=16e-9, nf_p=2, sa_p=85e9, sb_p=85e-9, sd_p=106e-9, sc_p=113e-9, pcpastrx_top_p=169e-9, pcpastrx_bot_p=57e-9, vdd=0.9, temp=25.0

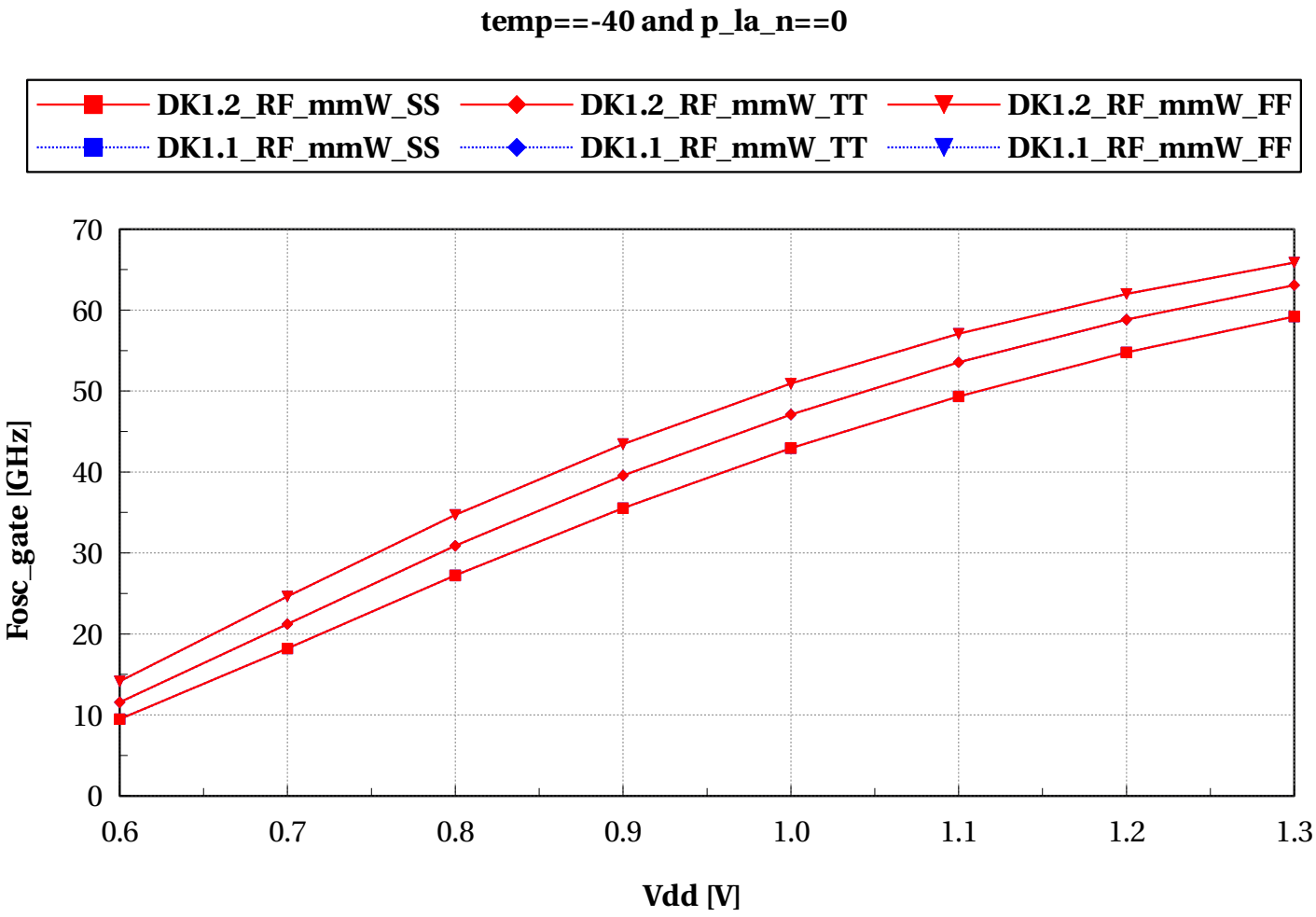
DK1.2_RF_mmW wrt DK1.1_RF_mmW

	SS	TT	FF
Fosc_gate [GHz]	25 0.0%	27.21 0.0%	29.32 0.0%
Idyn [µA]	119.8 0.0%	132.3 0.0%	146.2 0.0%
Pdyn [µW]	107.8 0.0%	119.1 0.0%	131.6 0.0%
Ceff [fF]	5.32 0.0%	5.4 0.0%	5.54 0.0%
Taup [ps]	20 0.0%	18.38 0.0%	17.05 0.0%
Istat_gate [nA]	0.14 0.0%	0.25 0.0%	0.59 0.0%
LogIstat_gate []	-9.85 -0.0%	-9.6 -0.0%	-9.23 -0.0%

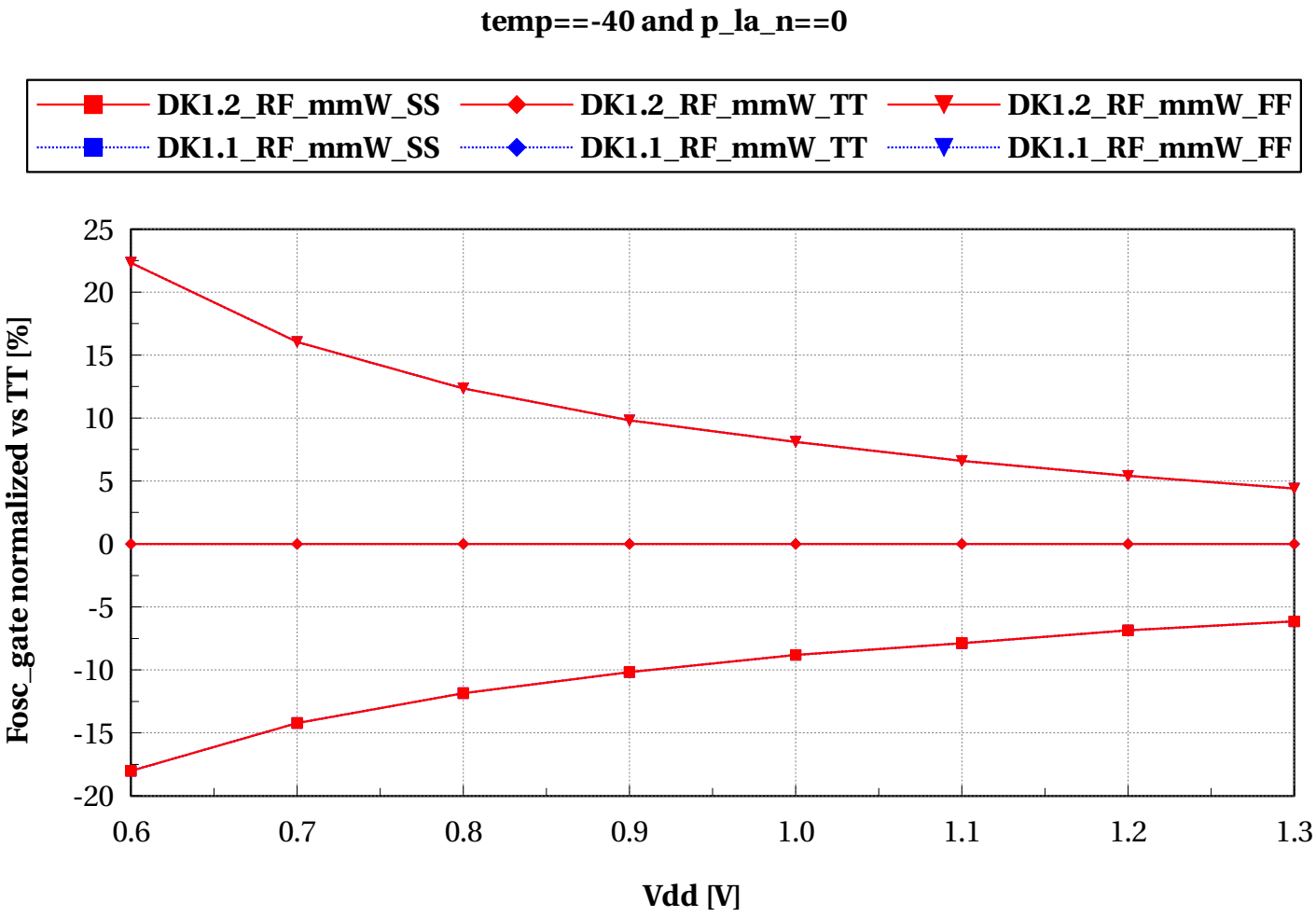
lvtnfet_acc_lvtpfet_acc
Electrical characteristics scaling

"RO FOM's vs Vdd @ T==-40C, PB=0"

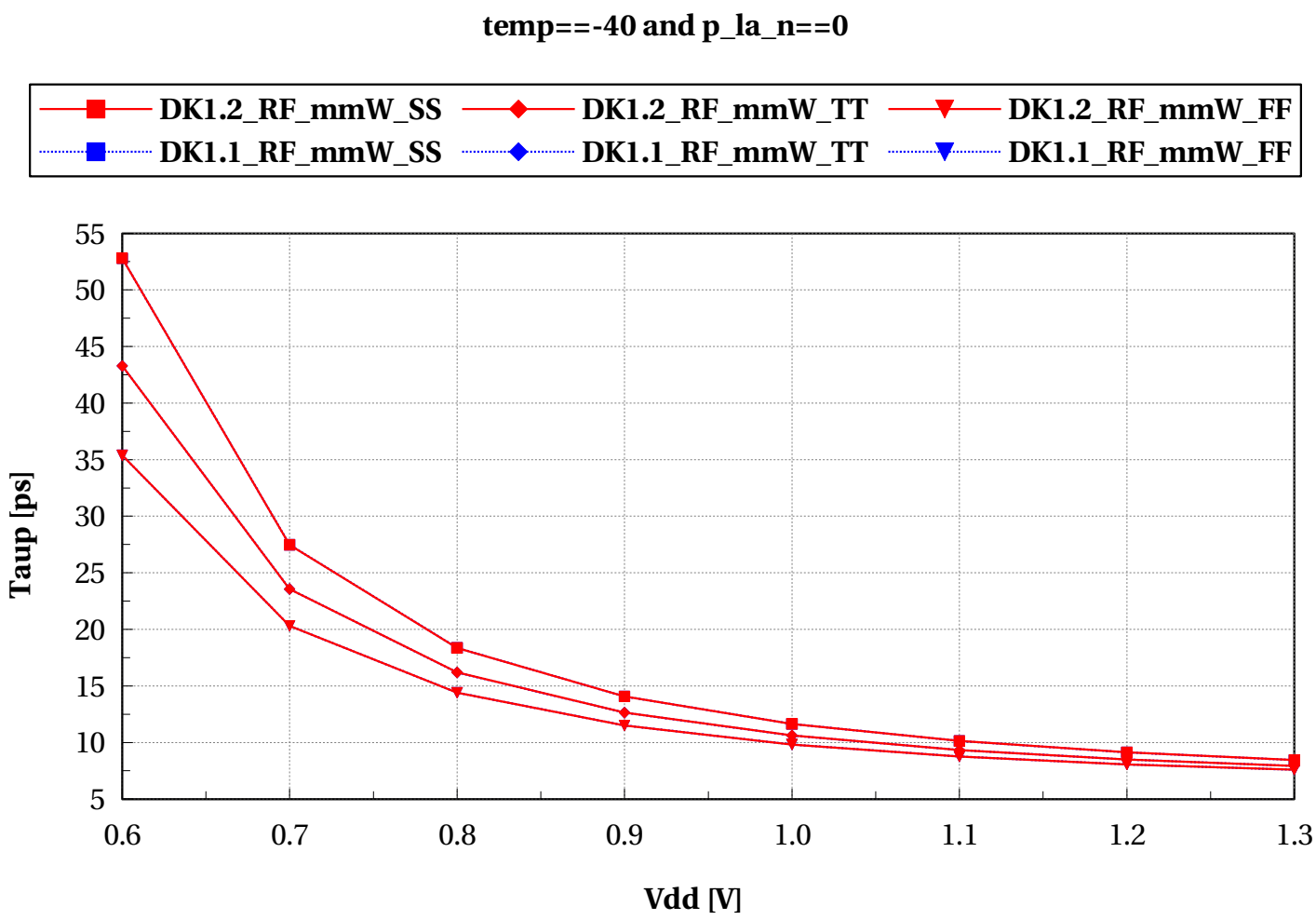
lvtnfet_acc_lvtpfet_acc, Fosc_gate [GHz] vs Vdd [V]



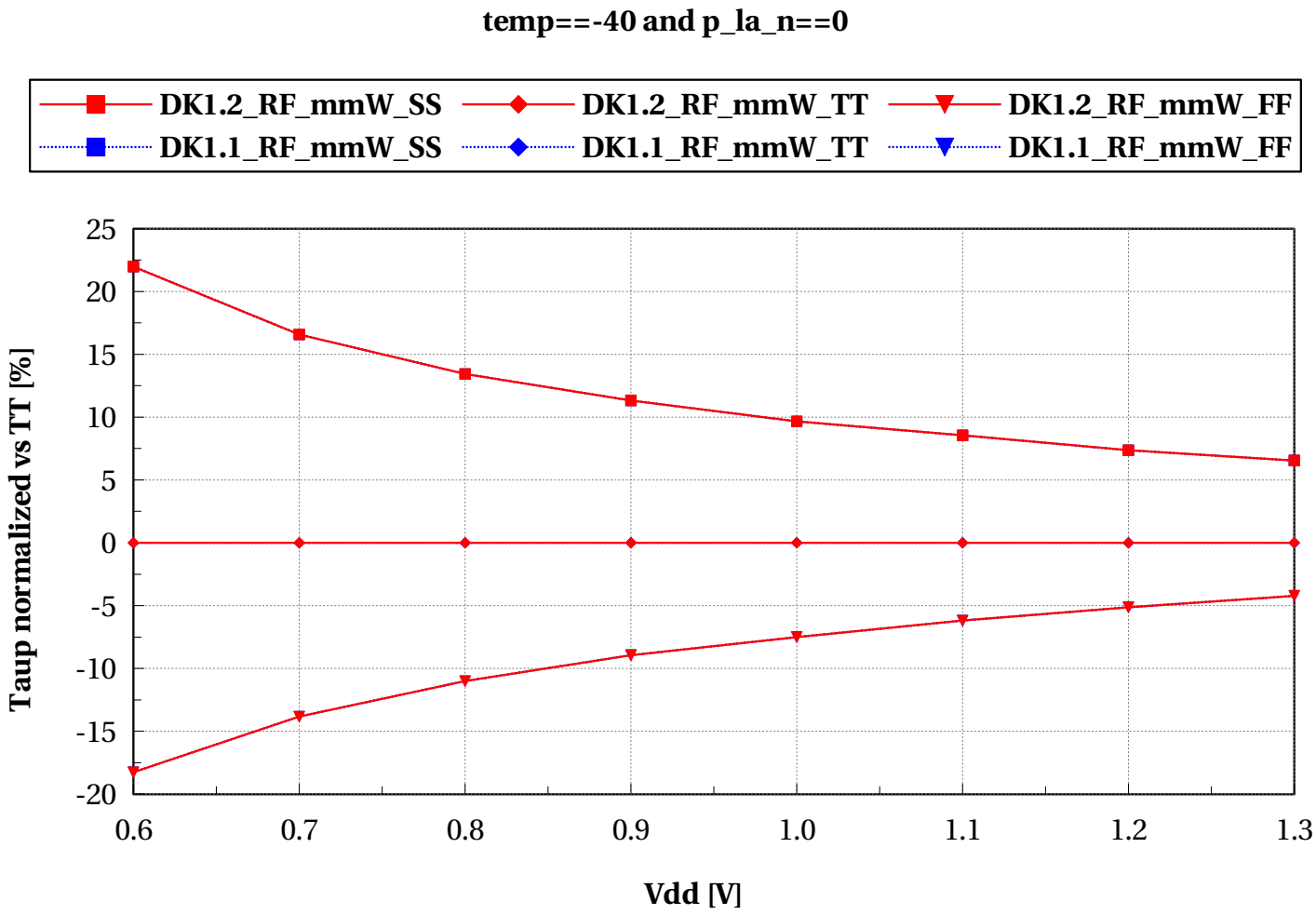
lvtnfet_acc_lvtpfet_acc, Fosc_gate normalized vs TT [%] vs Vdd [V]



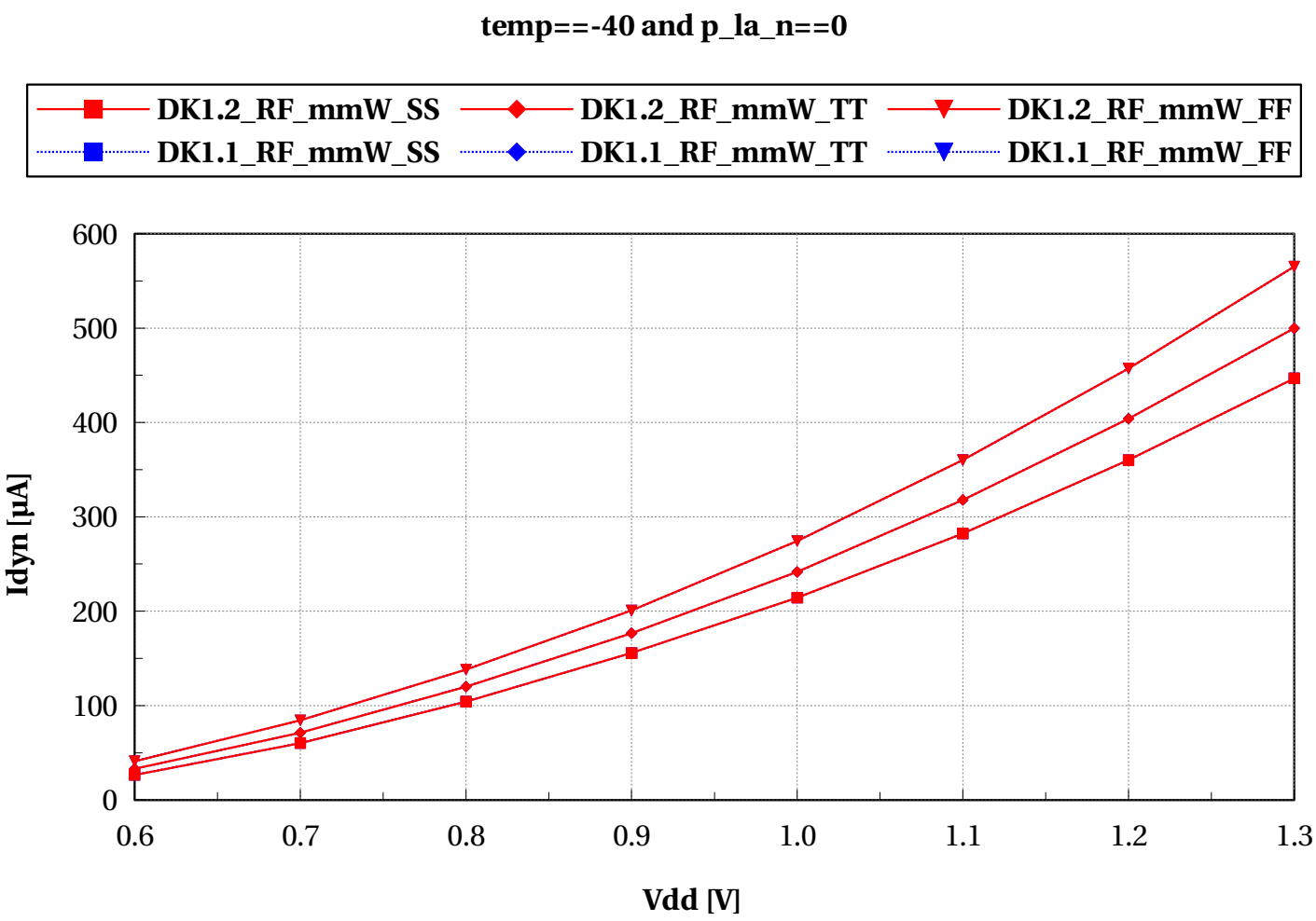
lvtnfet_acc_lvtpfet_acc, Taup [ps] vs Vdd [V]



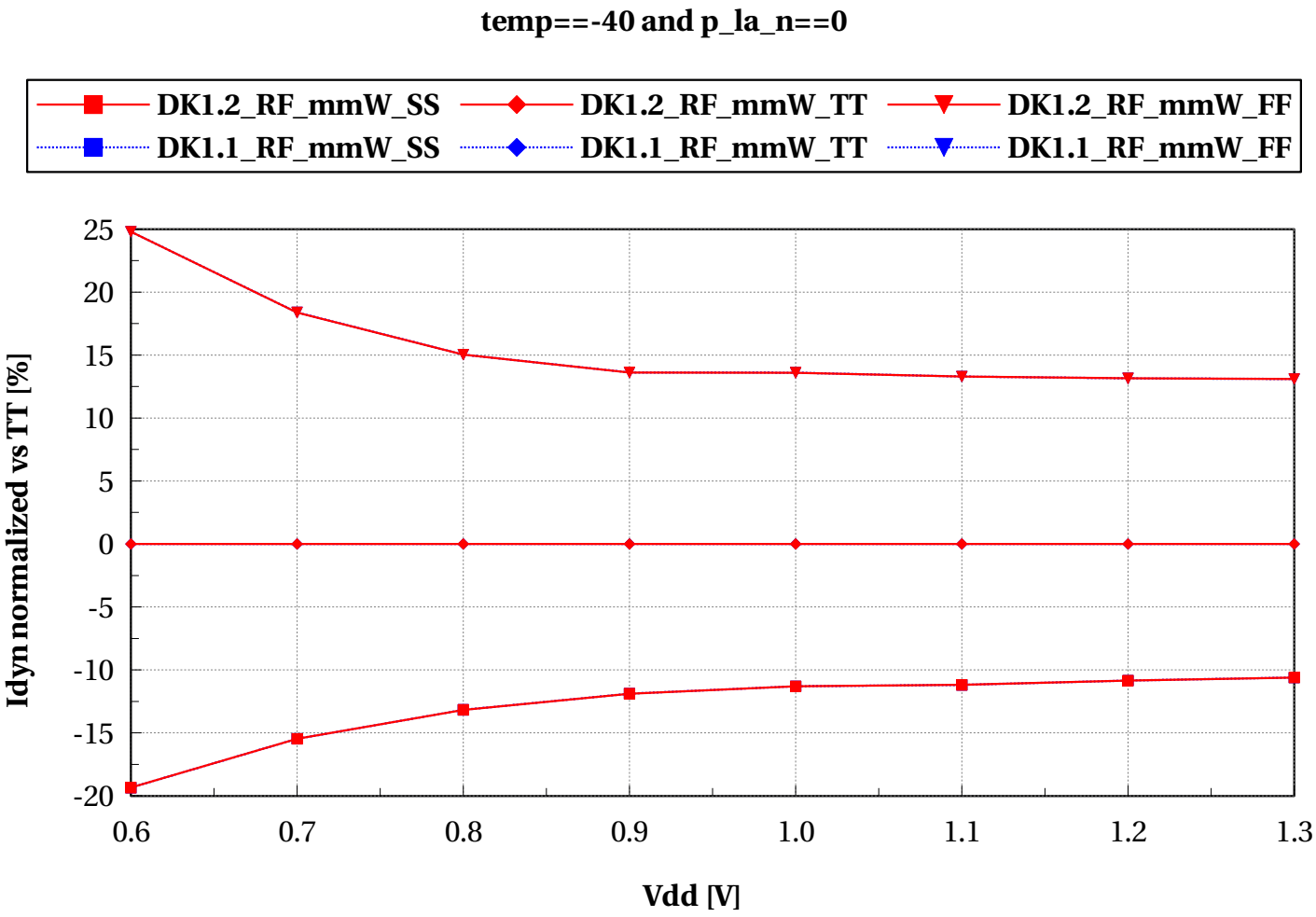
lvtnfet_acc_lvtpfet_acc, Taup normalized vs TT [%] vs Vdd [V]



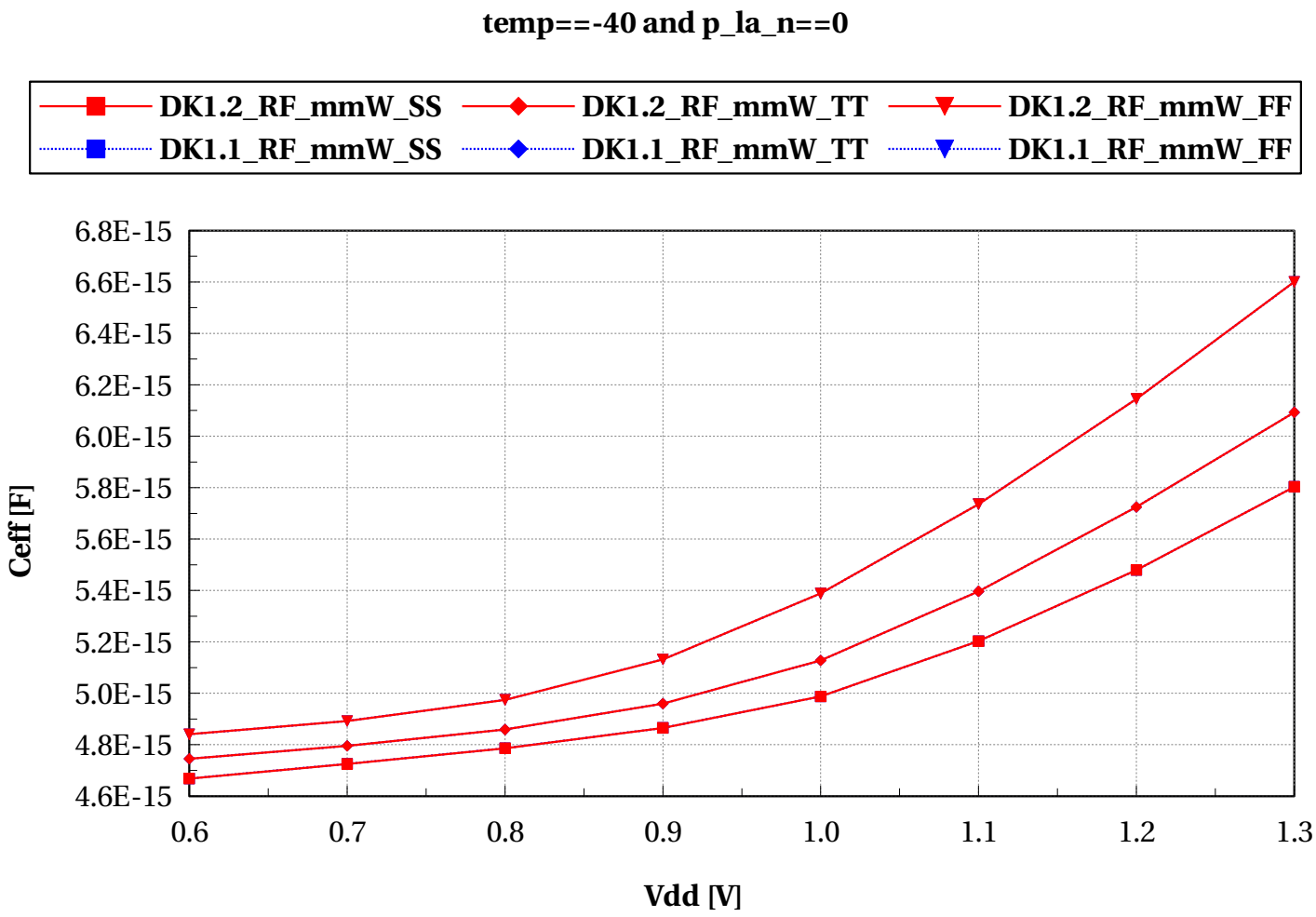
lvtnfet_acc_lvtpfet_acc, Idyn [µA] vs Vdd [V]



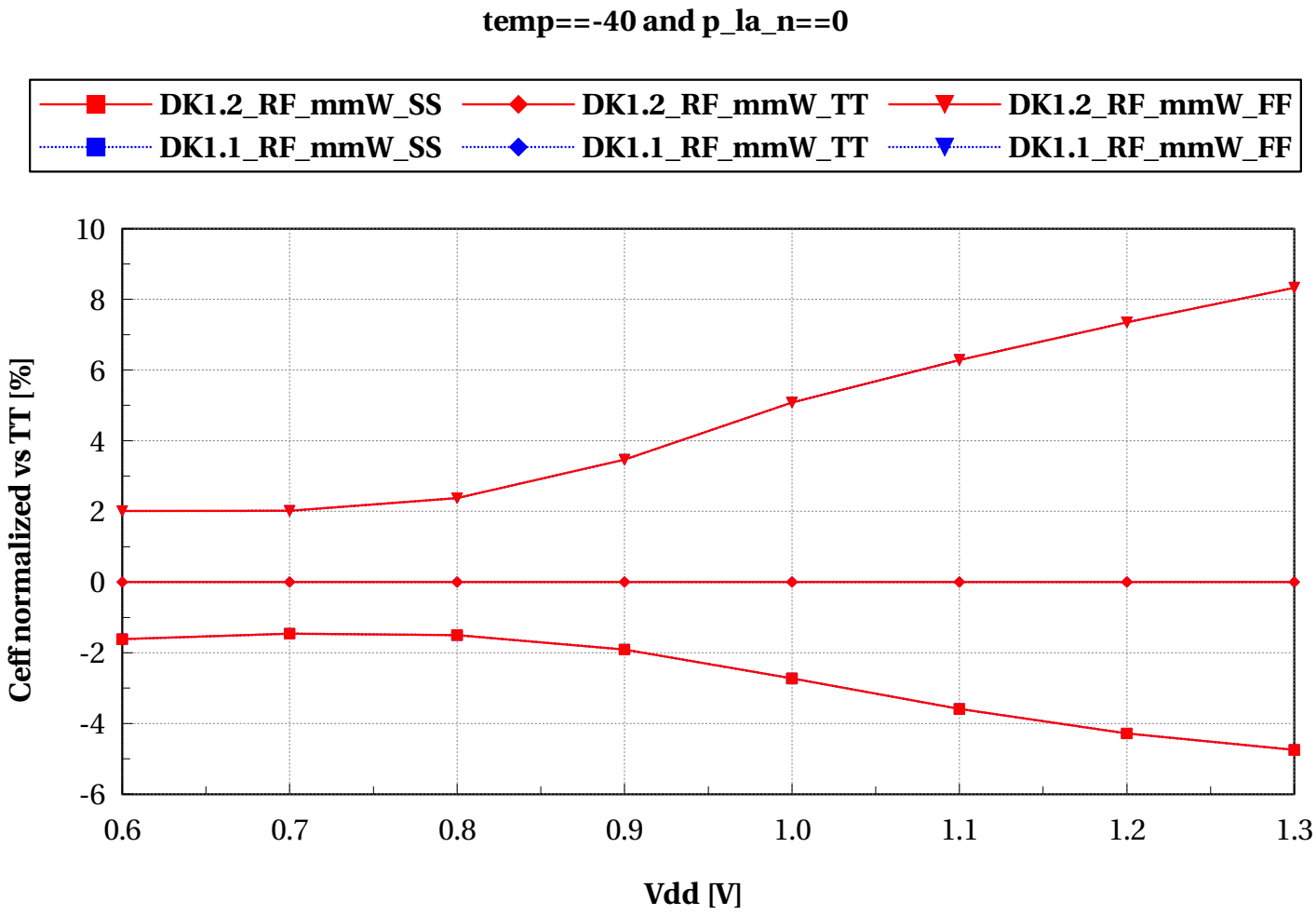
lvtnfet_acc_lvtpfet_acc, Idyn normalized vs TT [%] vs Vdd [V]



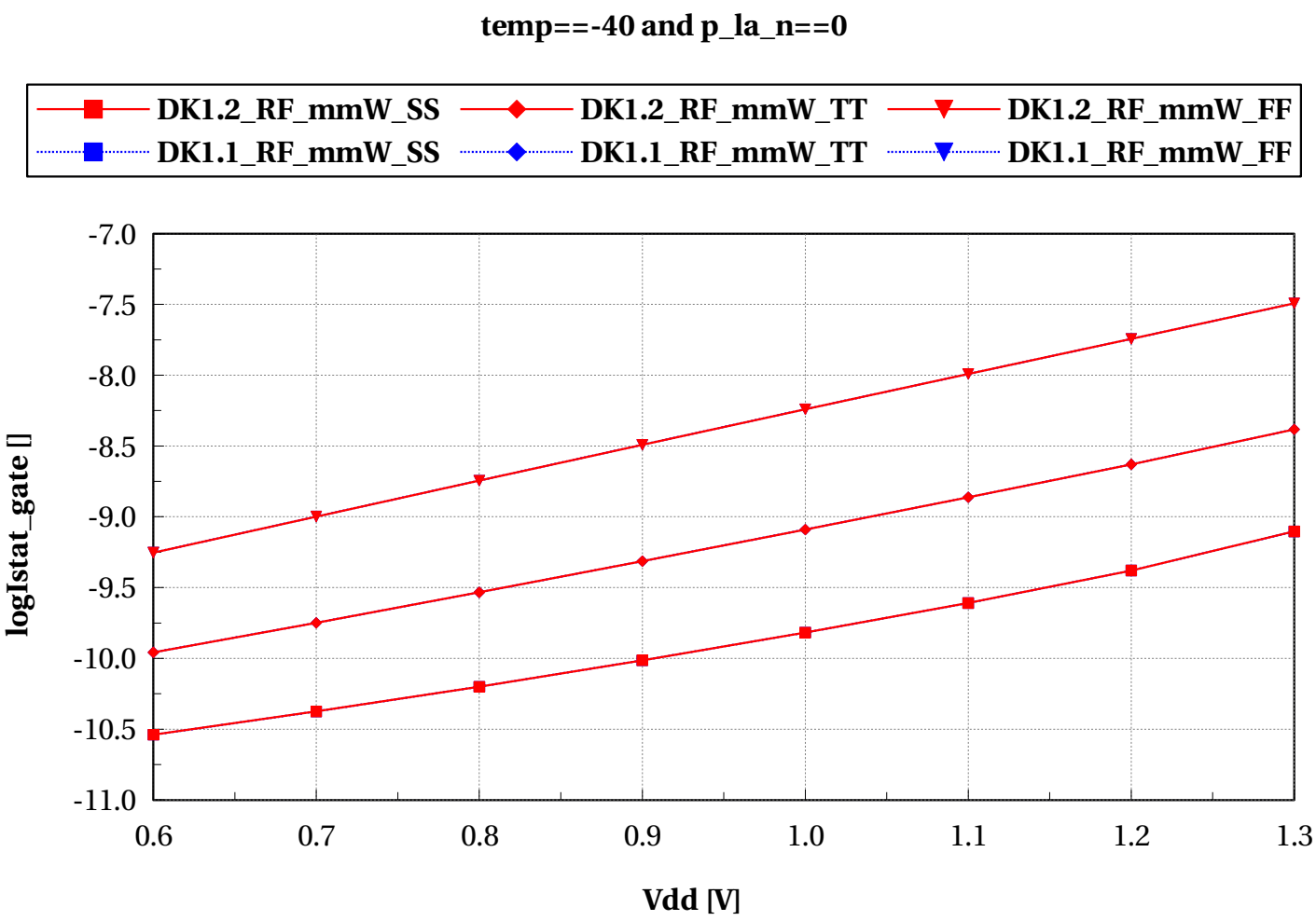
lvtnfet_acc_lvtpfet_acc, Ceff [F] vs Vdd [V]



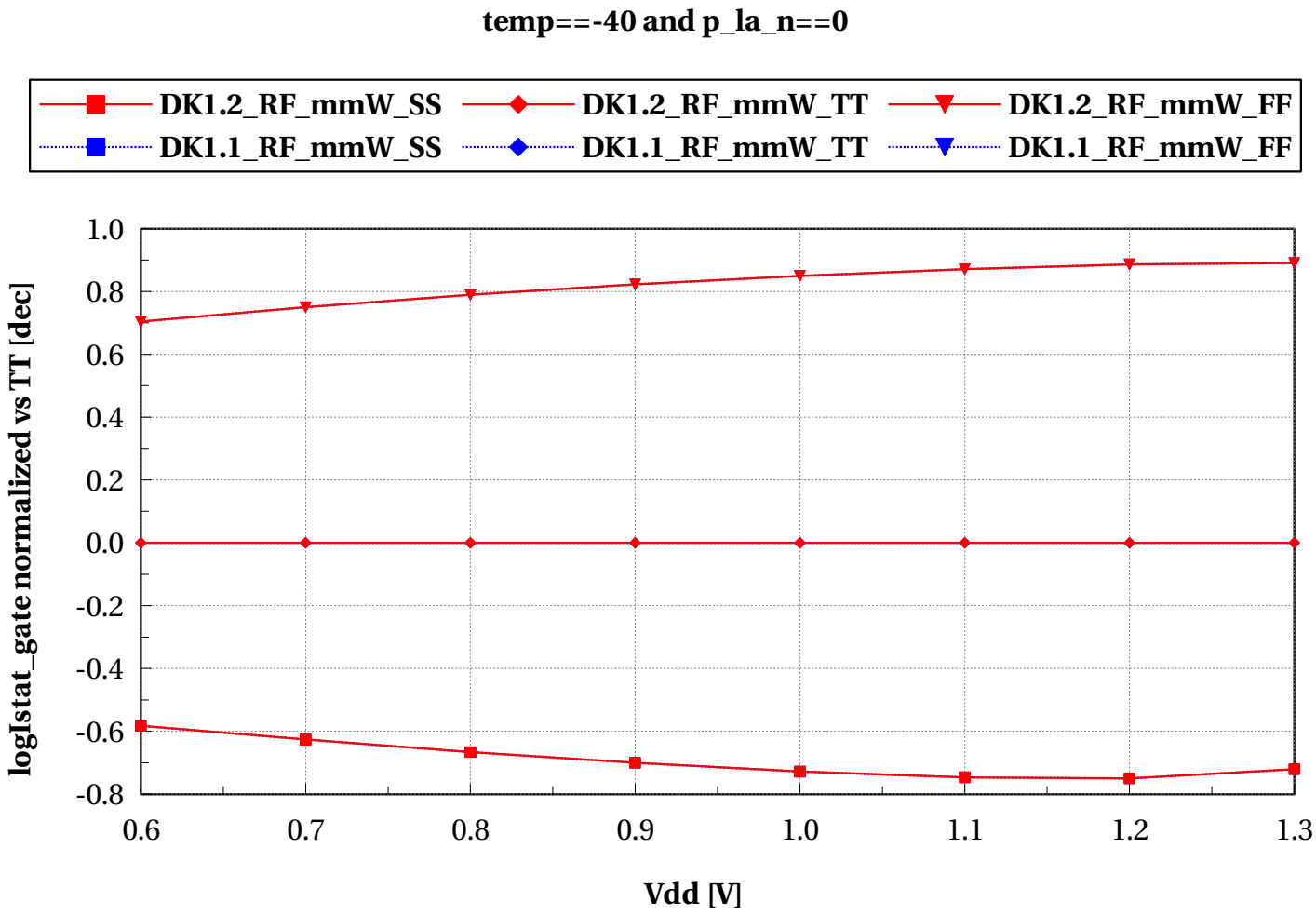
lvtnfet_acc_lvtpfet_acc, Ceff normalized vs TT [%] vs Vdd [V]



lvtnfet_acc_lvtpfet_acc, logIstat_gate [] vs Vdd [V]

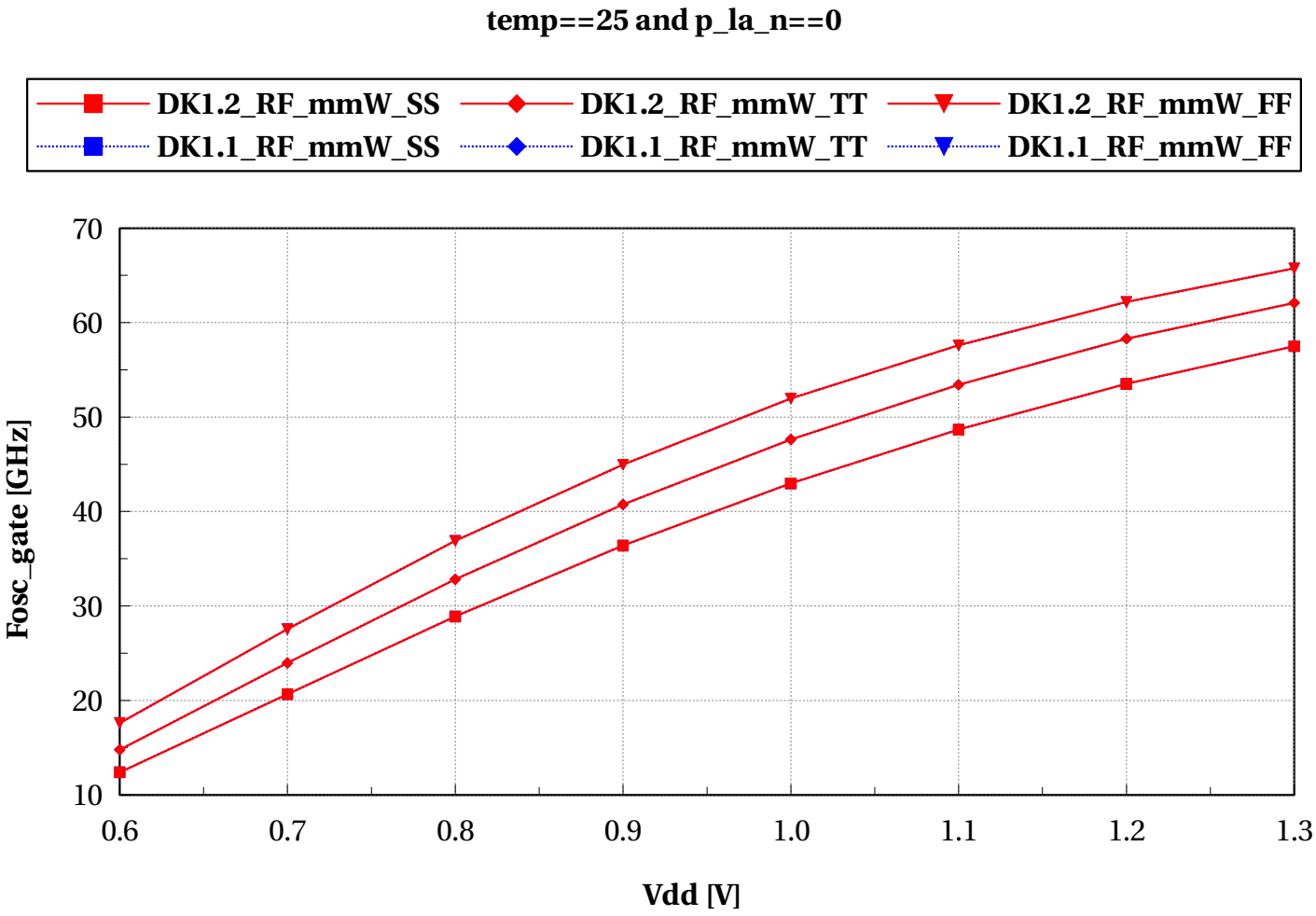


lvtnfet_acc_lvtpfet_acc, logIstat_gate normalized vs TT [dec] vs Vdd [V]

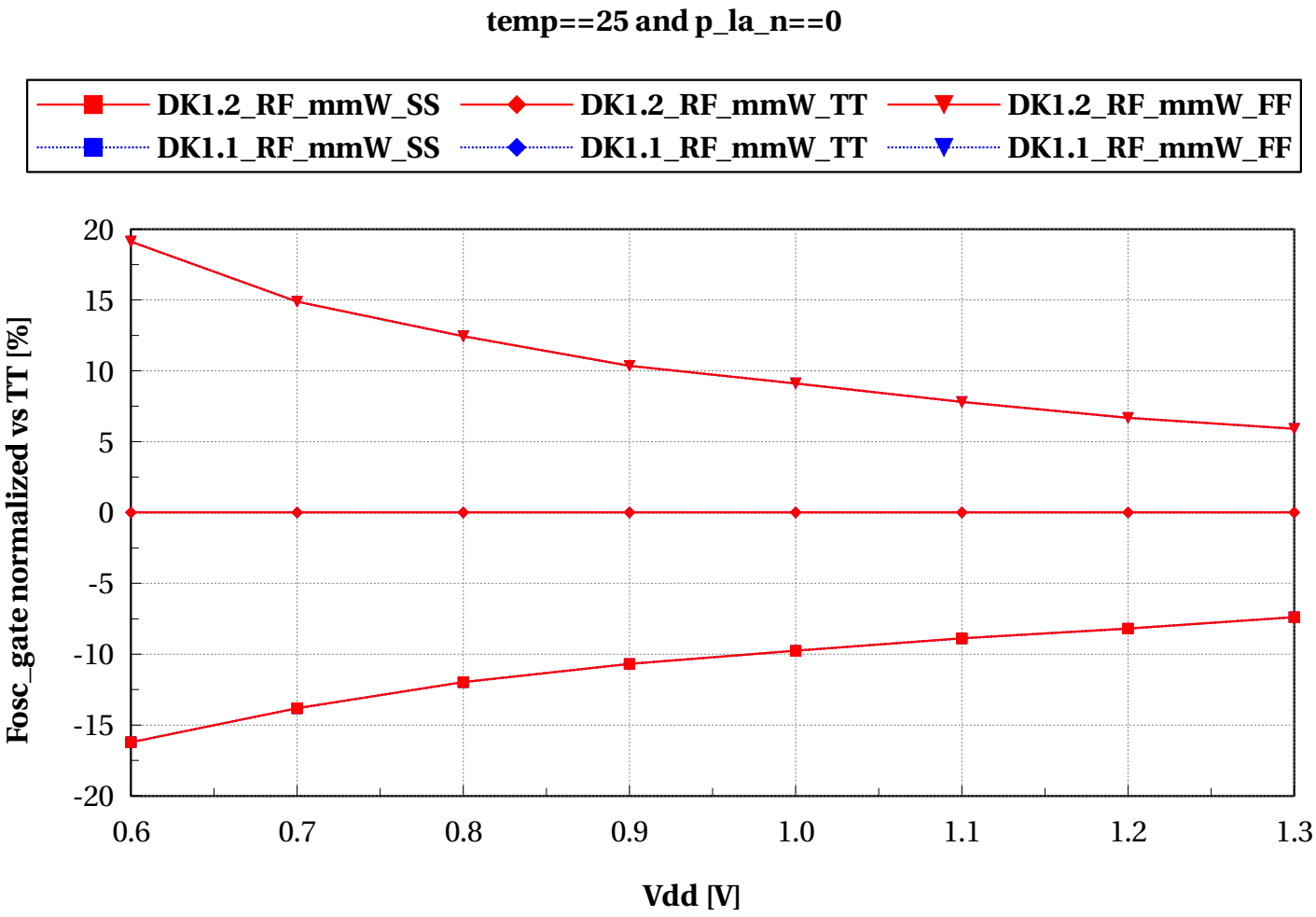


"RO FOM's vs Vdd @ T==25C, PB=0"

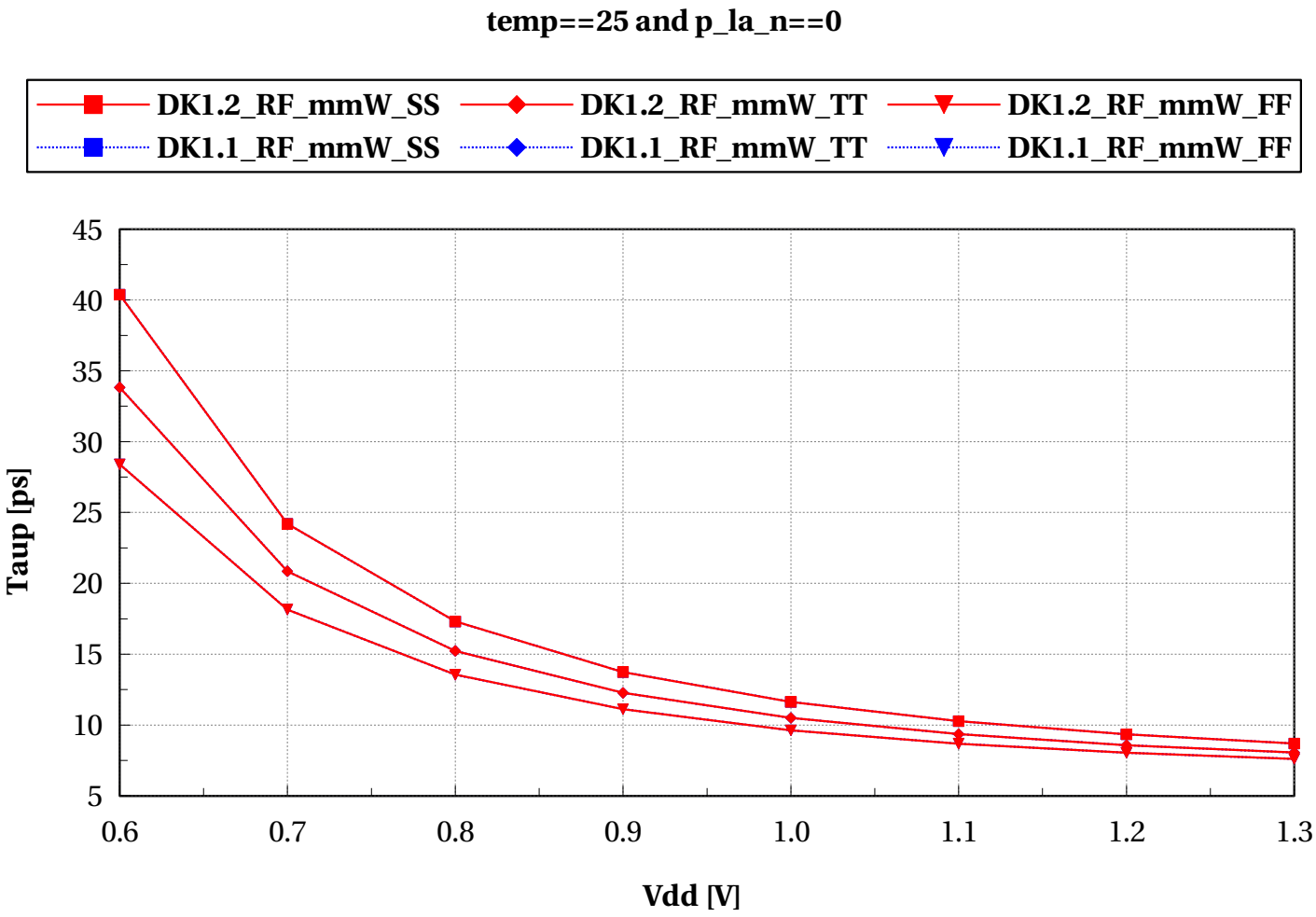
lvtnfet_acc_lvtpfet_acc, Fosc_gate [GHz] vs Vdd [V]



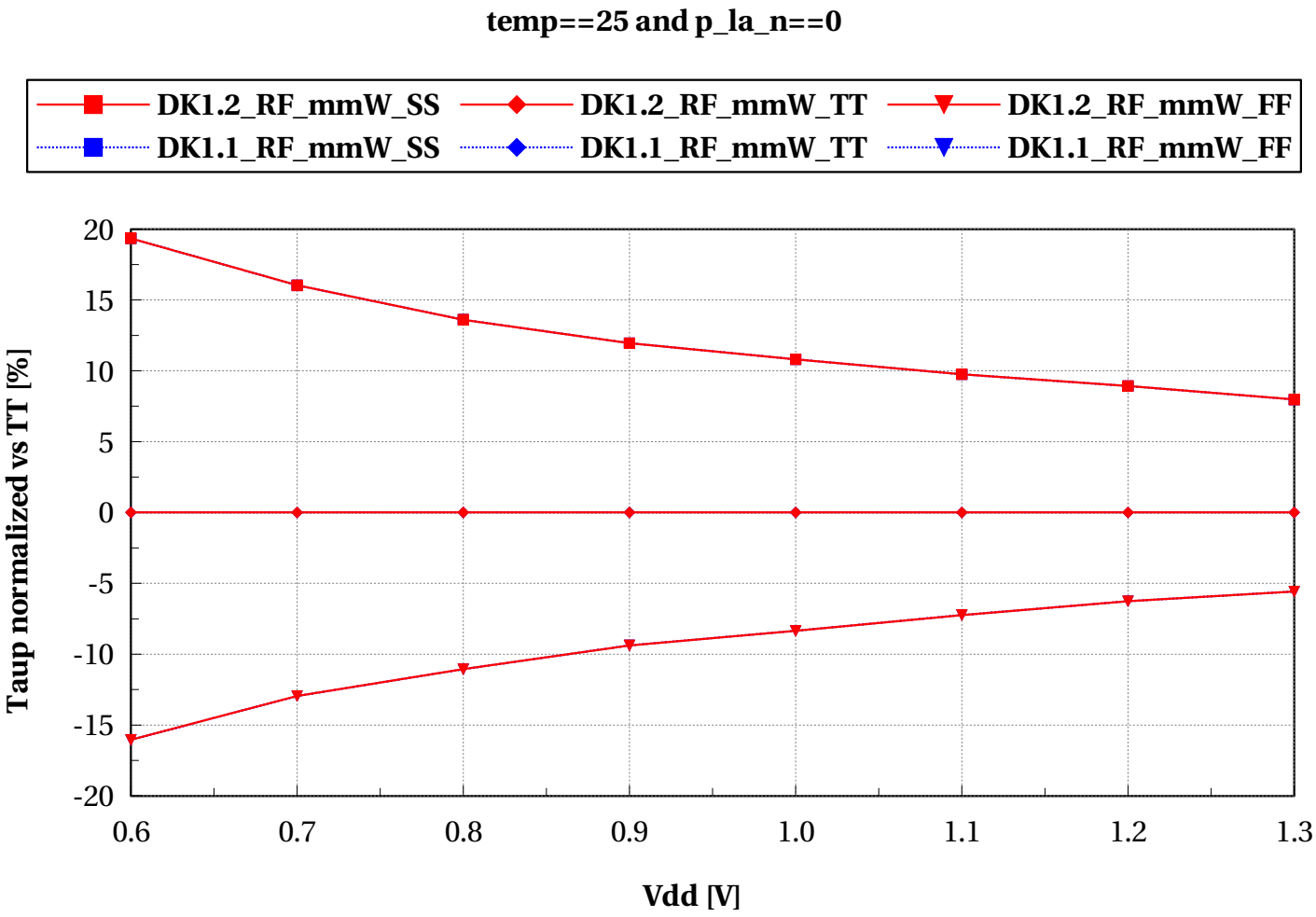
lvtnfet_acc_lvtpfet_acc, Fosc_gate normalized vs TT [%] vs Vdd [V]



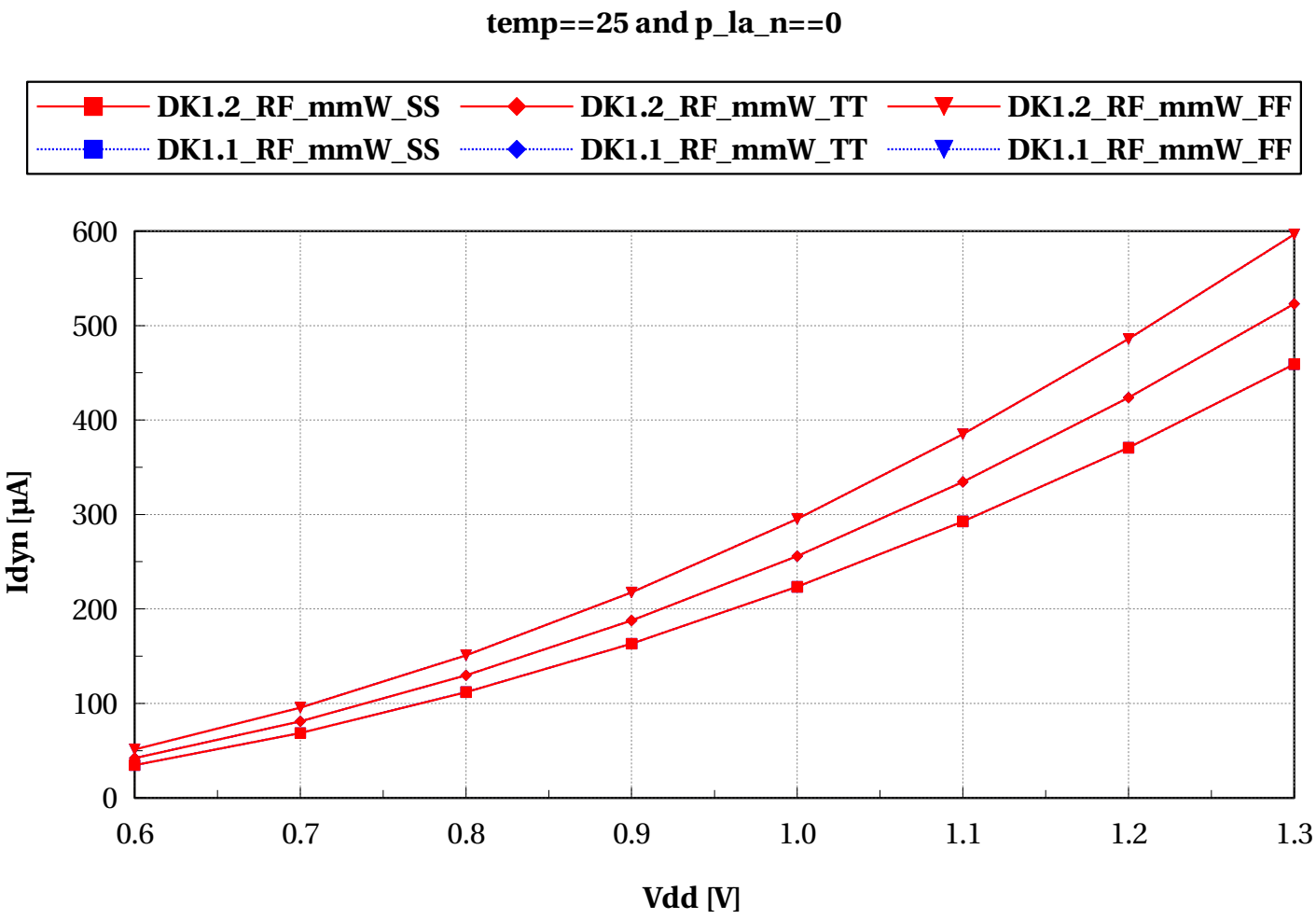
lvtnfet_acc_lvtpfet_acc, Taup [ps] vs Vdd [V]



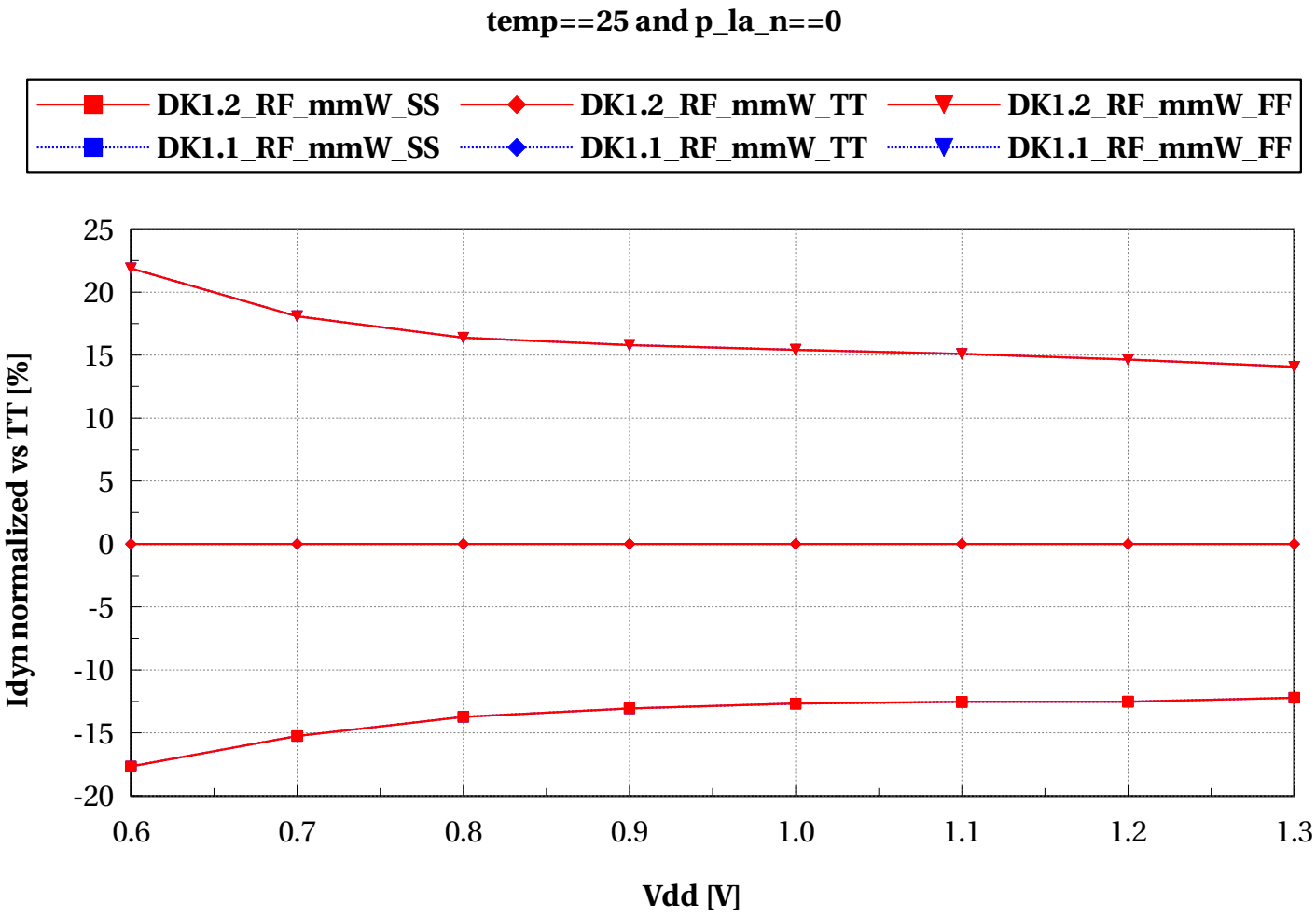
lvtnfet_acc_lvtpfet_acc, Taup normalized vs TT [%] vs Vdd [V]



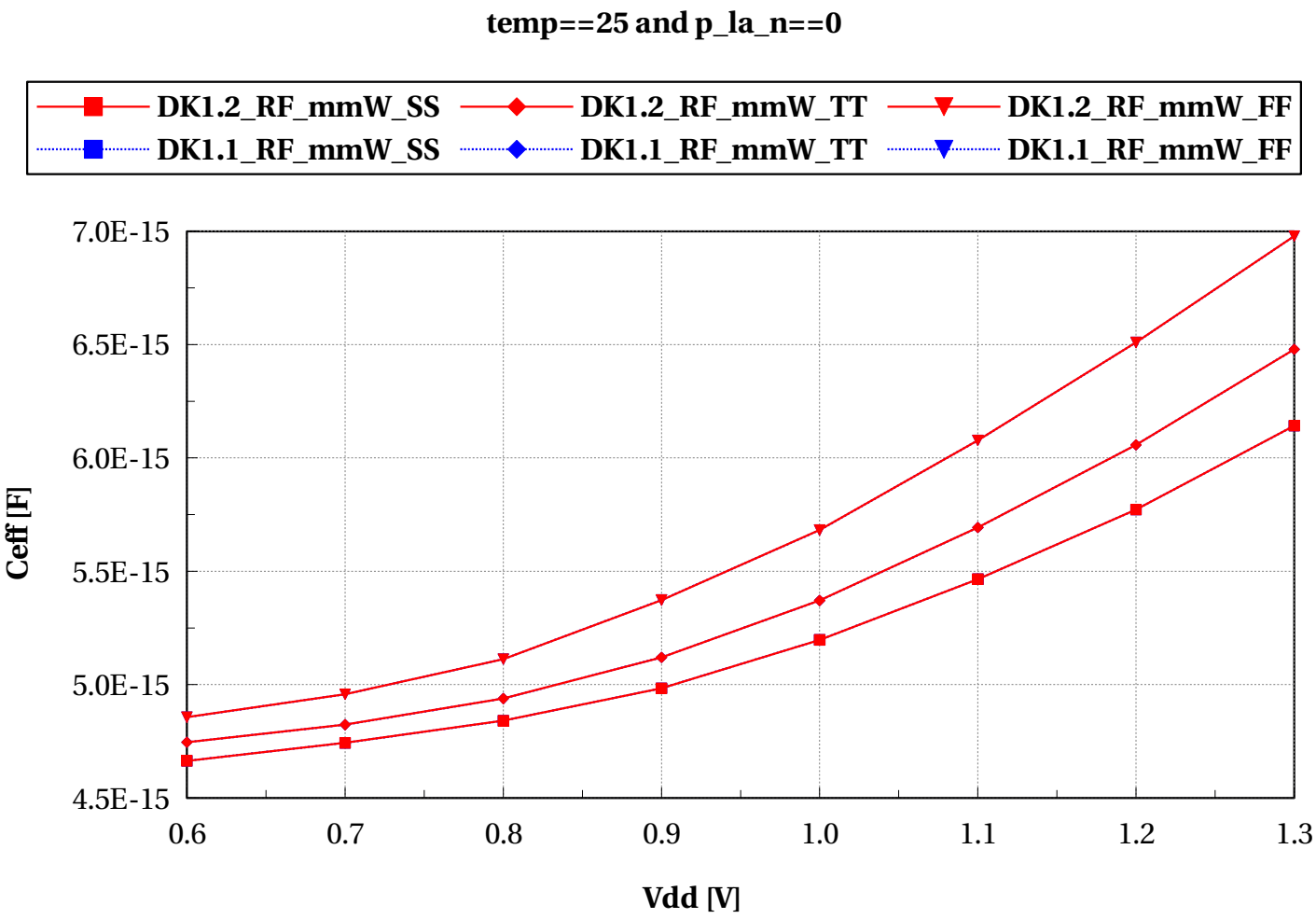
lvtnfet_acc_lvtpfet_acc, Idyn [µA] vs Vdd [V]



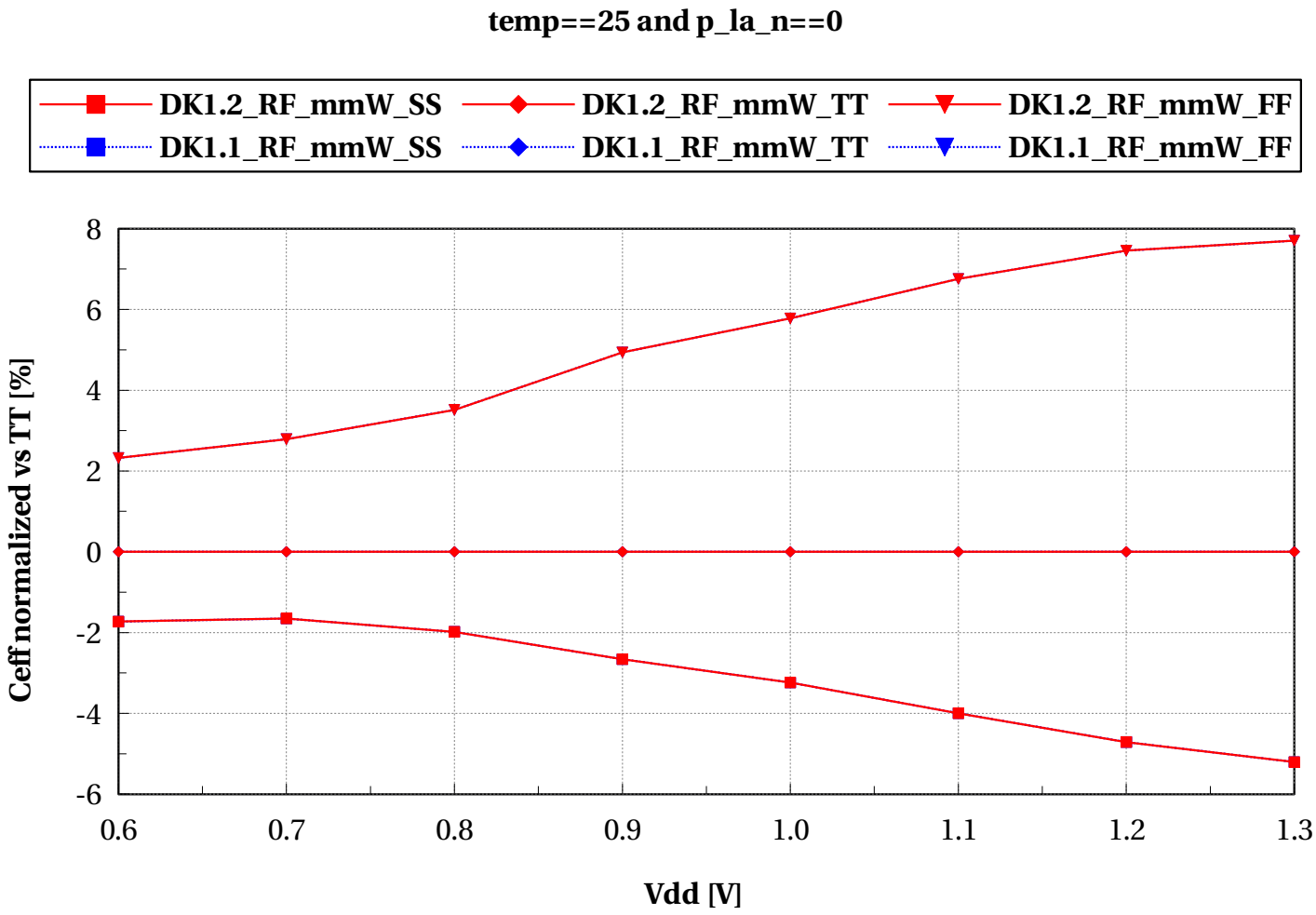
lvtnfet_acc_lvtpfet_acc, Idyn normalized vs TT [%] vs Vdd [V]



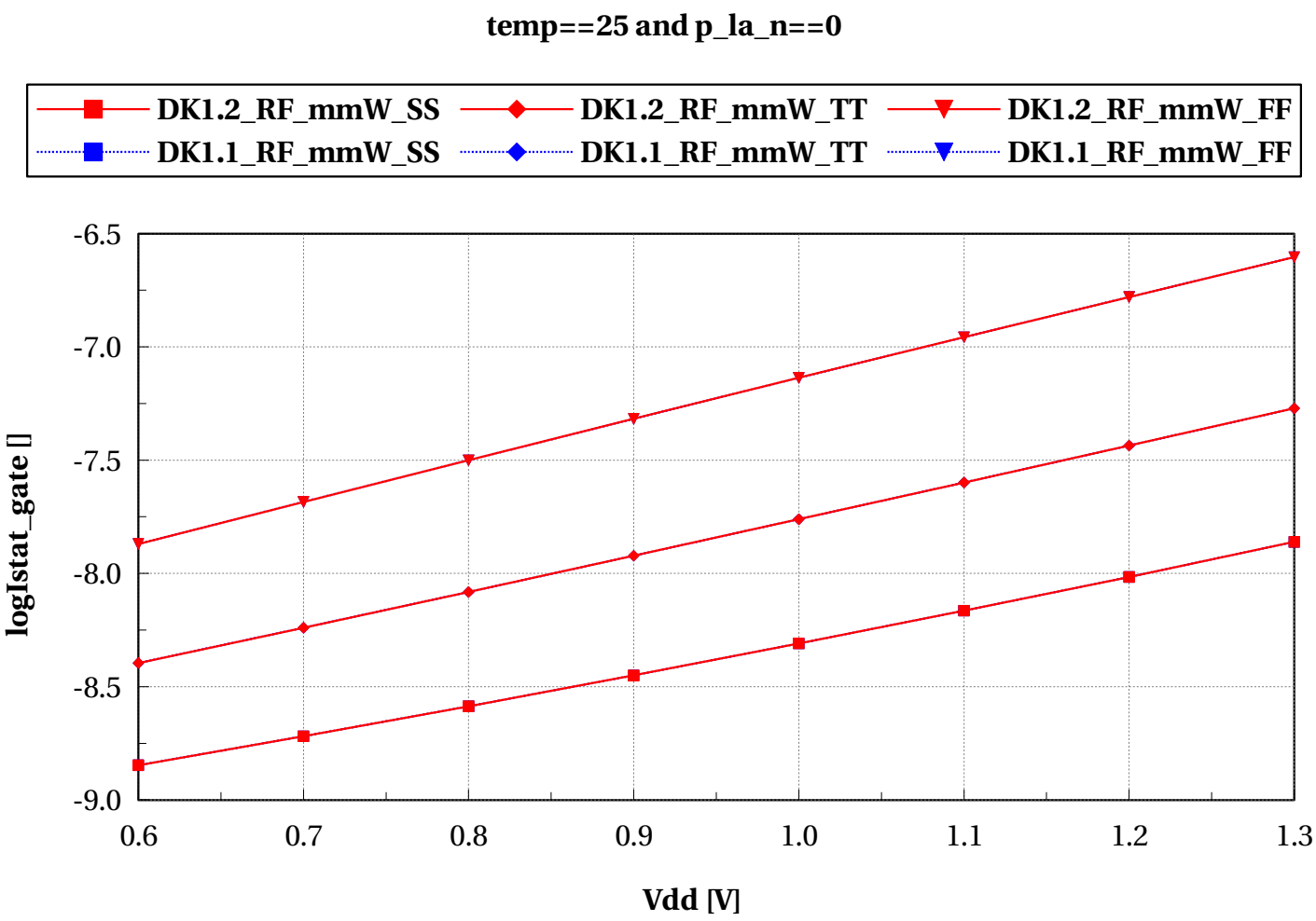
lvtnfet_acc_lvtpfet_acc, Ceff [F] vs Vdd [V]



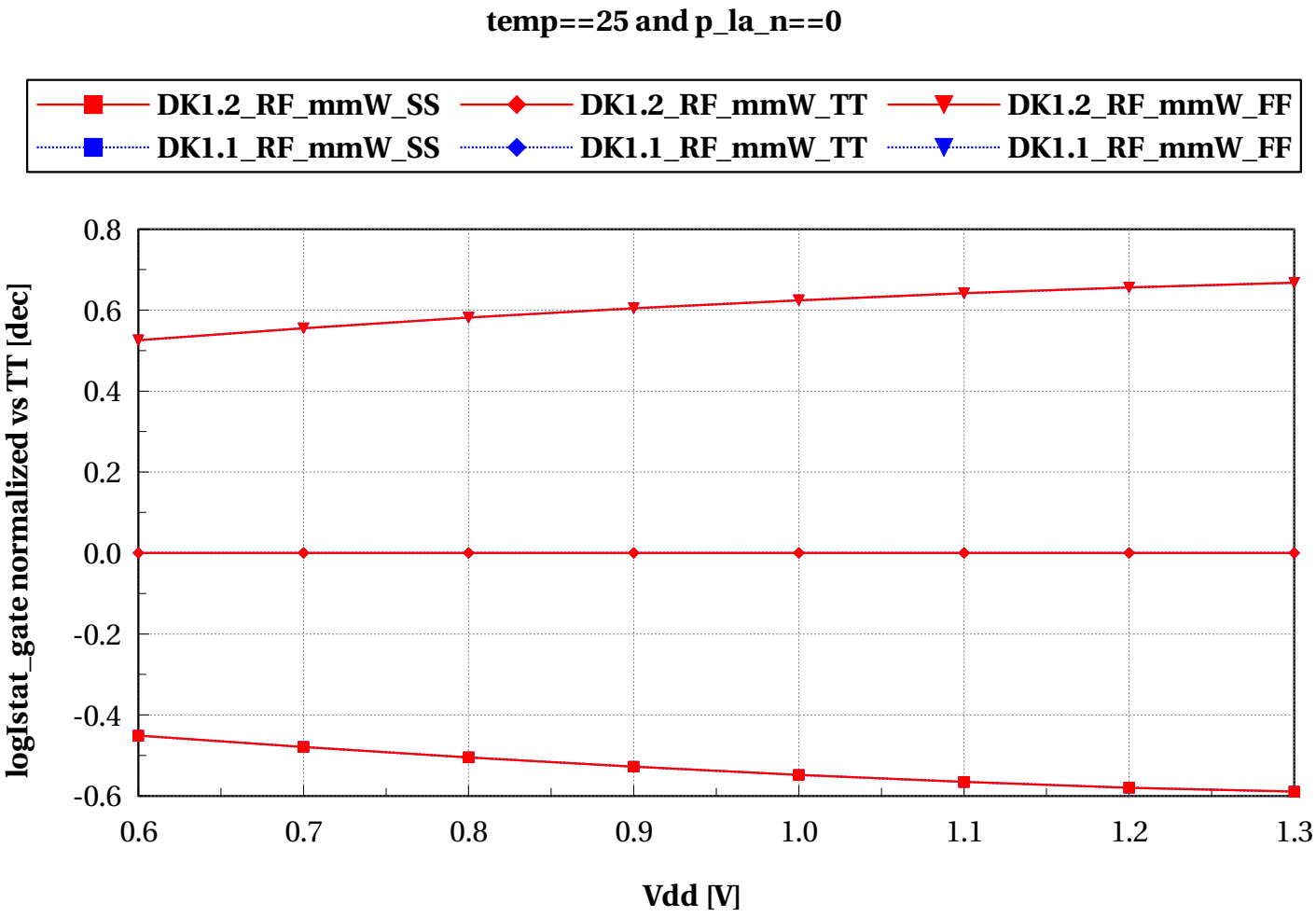
lvtnfet_acc_lvtpfet_acc, Ceff normalized vs TT [%] vs Vdd [V]



lvtnfet_acc_lvtpfet_acc, logIstat_gate [] vs Vdd [V]

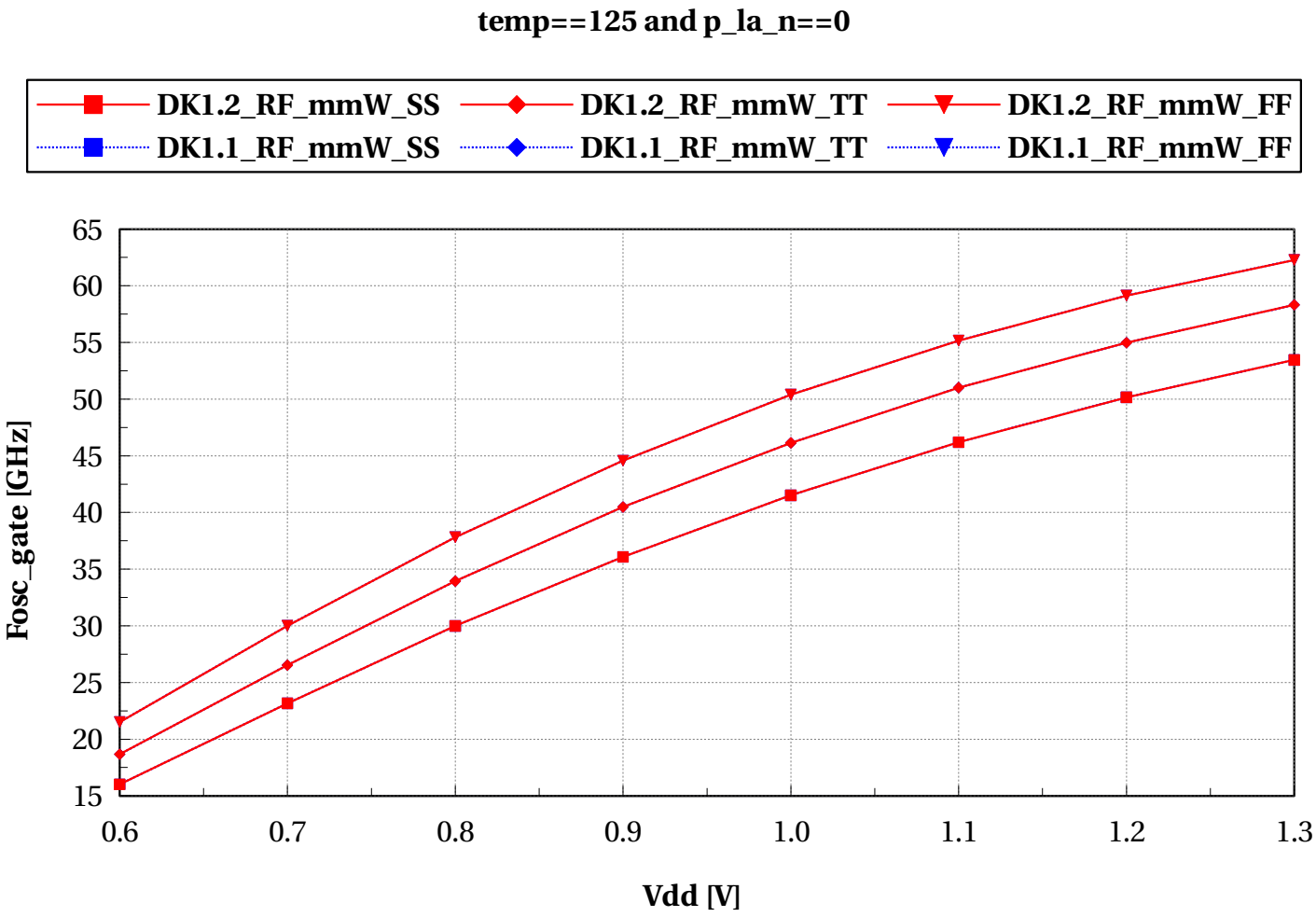


lvtnfet_acc_lvtpfet_acc, logIstat_gate normalized vs TT [dec] vs Vdd [V]

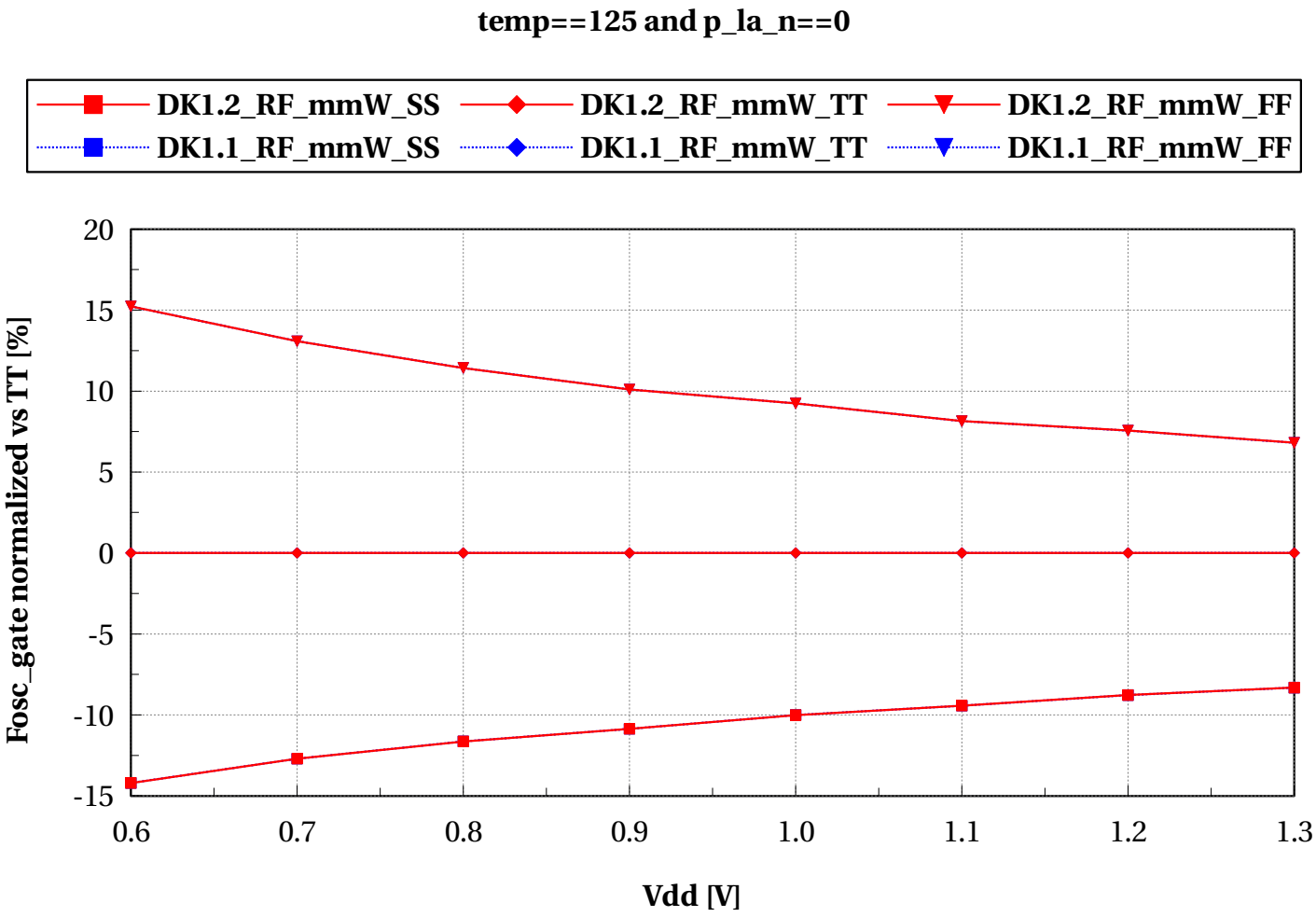


"RO FOM's vs Vdd @ T==125C, PB=0"

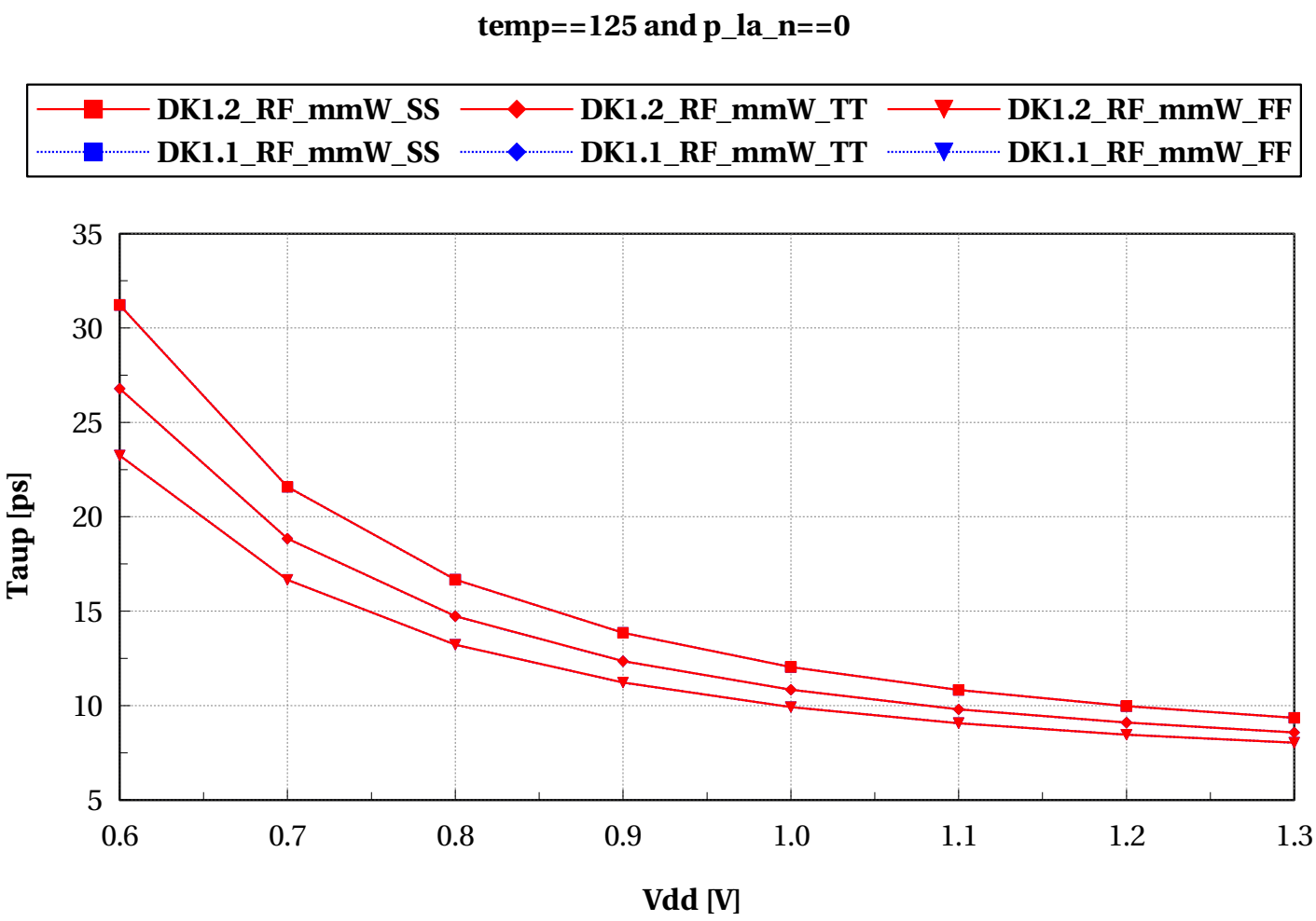
lvtnfet_acc_lvtpfet_acc, Fosc_gate [GHz] vs Vdd [V]



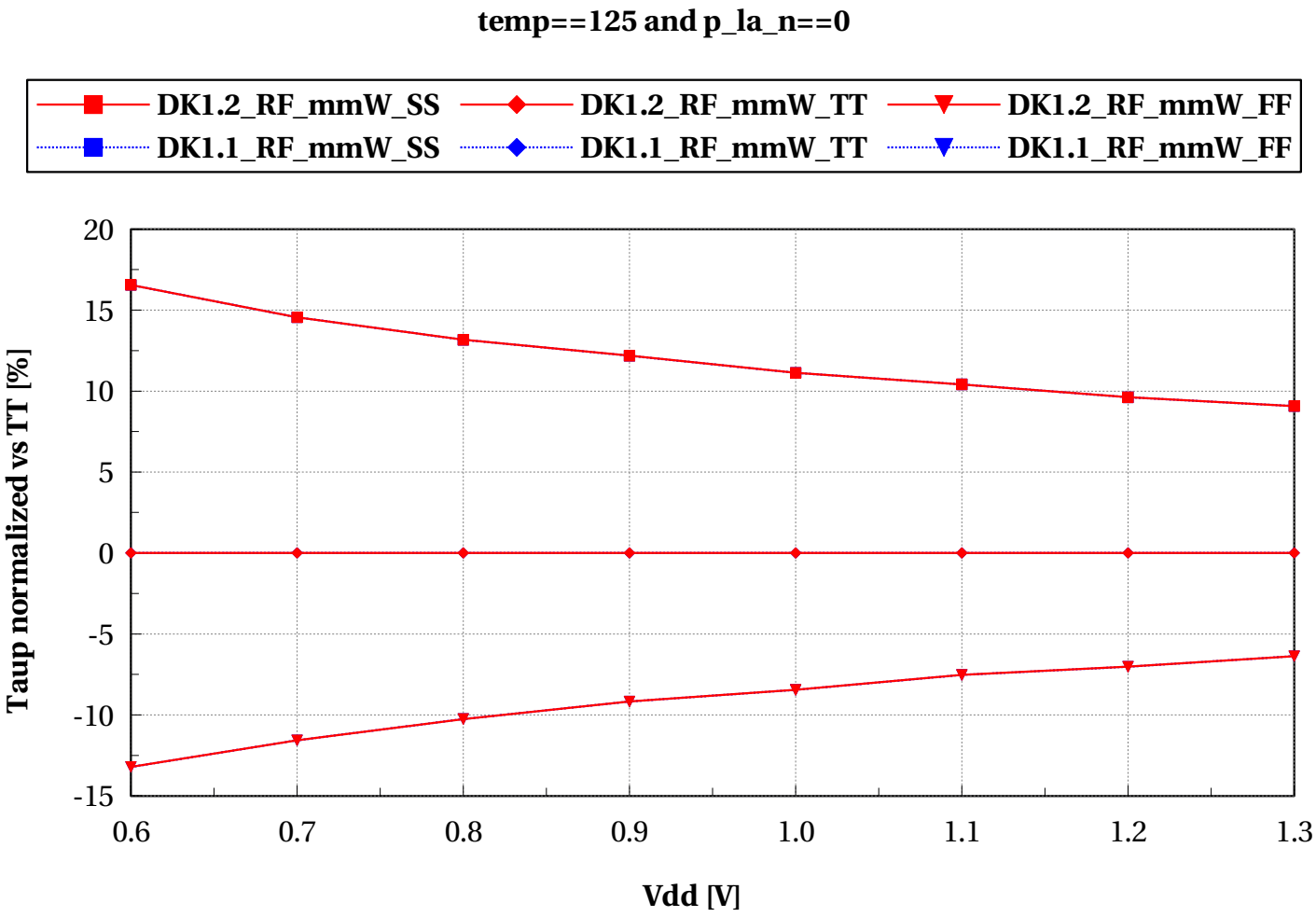
lvtnfet_acc_lvtpfet_acc, Fosc_gate normalized vs TT [%] vs Vdd [V]



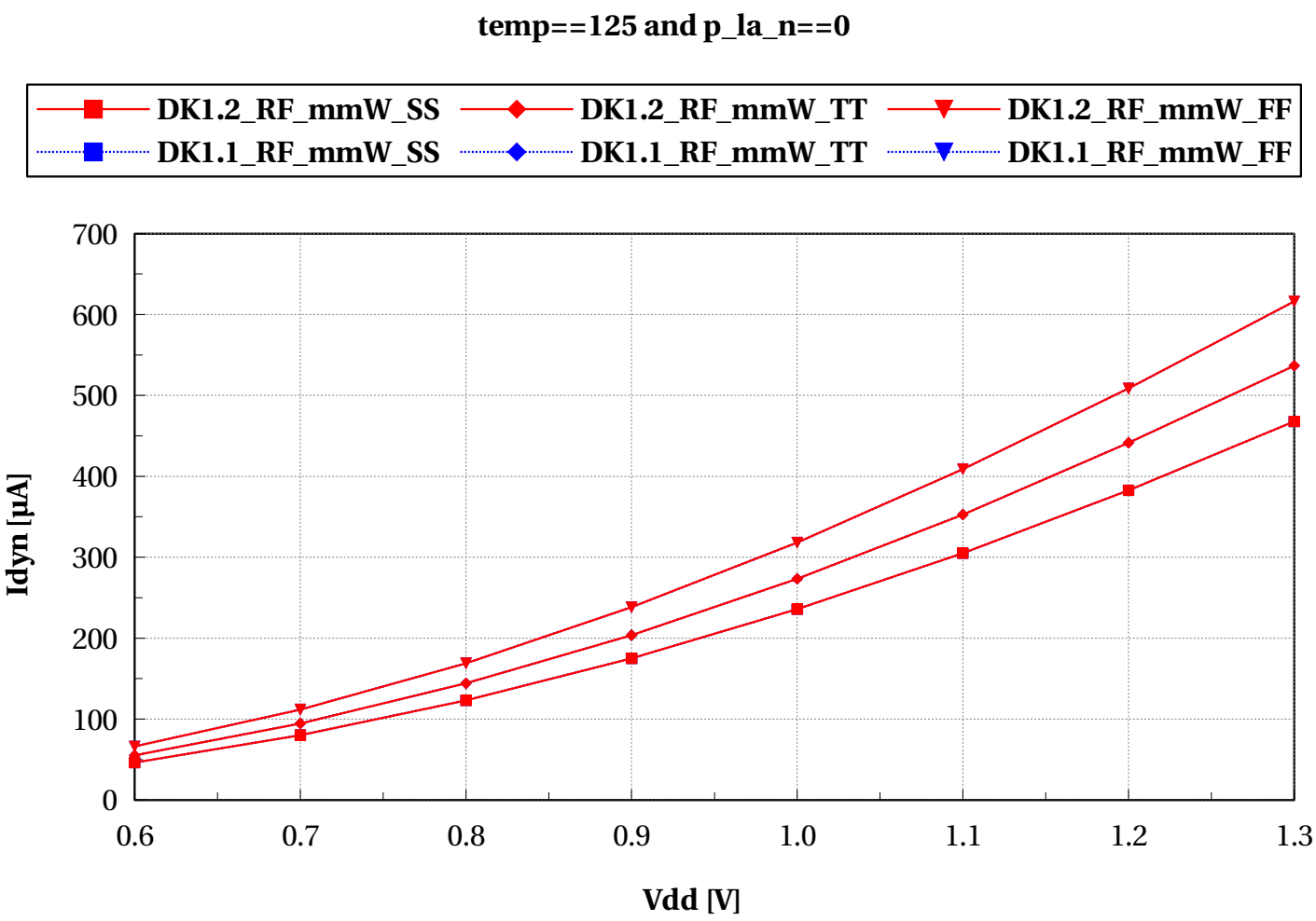
lvtnfet_acc_lvtpfet_acc, Taup [ps] vs Vdd [V]



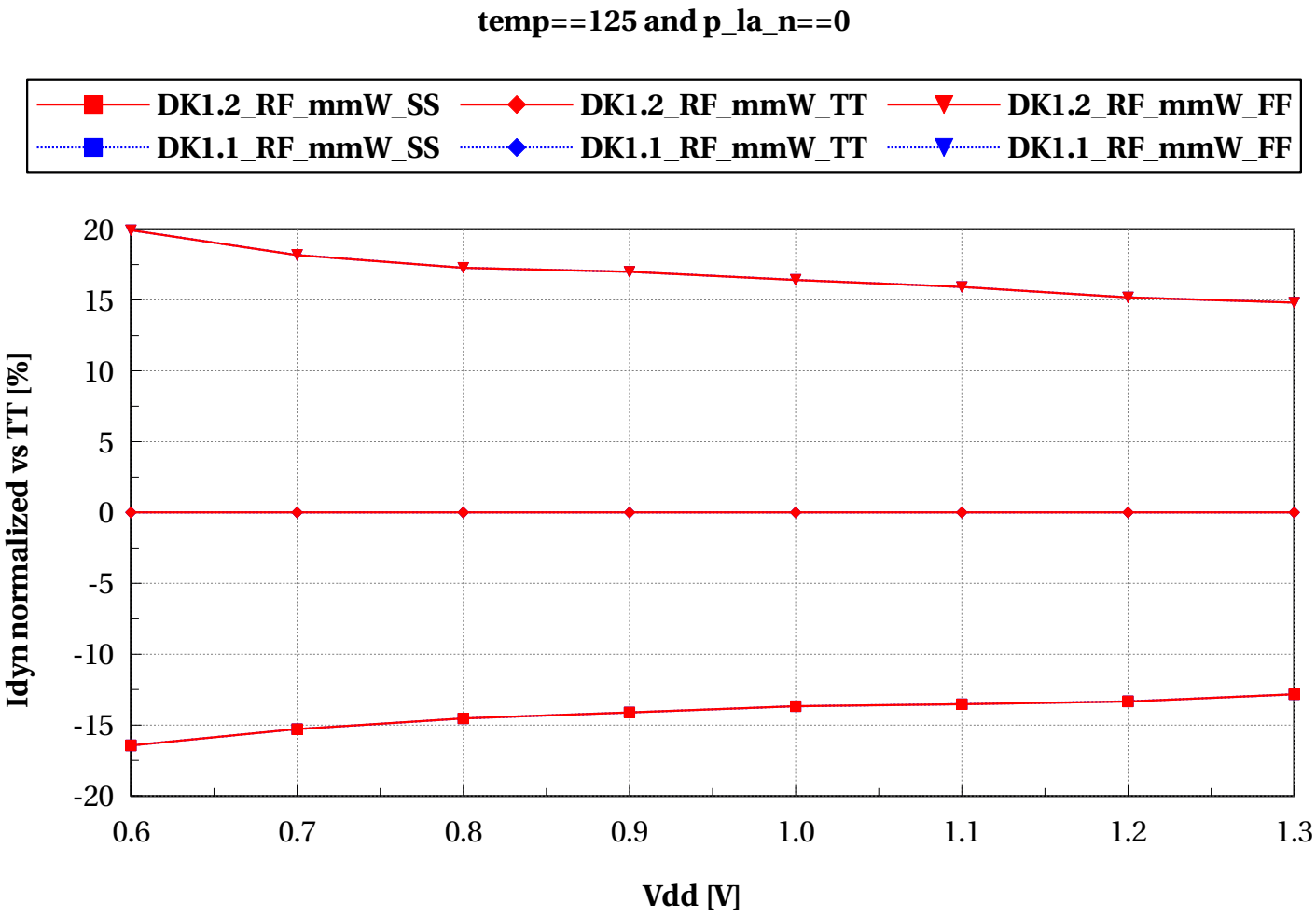
lvtnfet_acc_lvtpfet_acc, Taup normalized vs TT [%] vs Vdd [V]



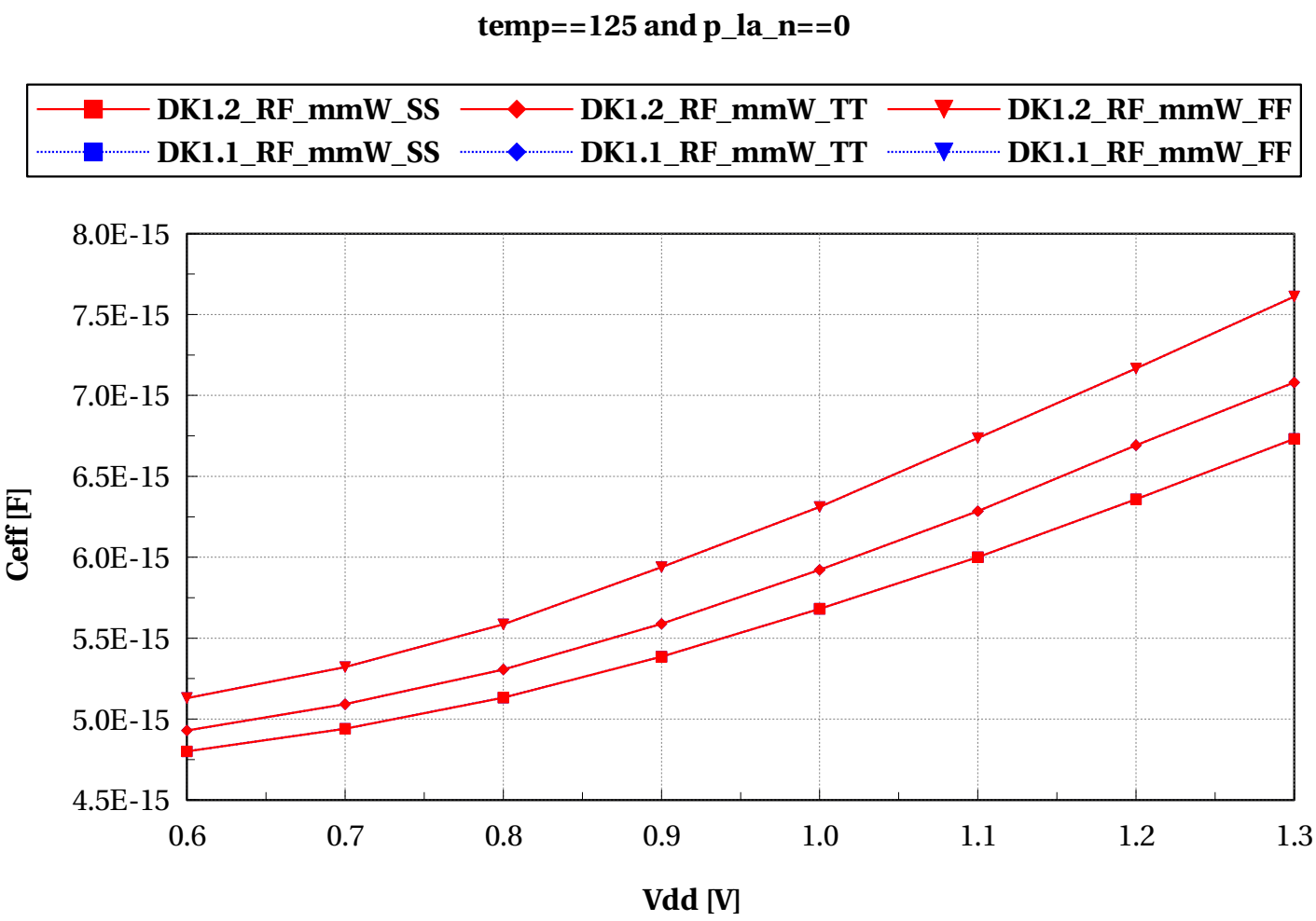
lvtnfet_acc_lvtpfet_acc, Idyn [µA] vs Vdd [V]



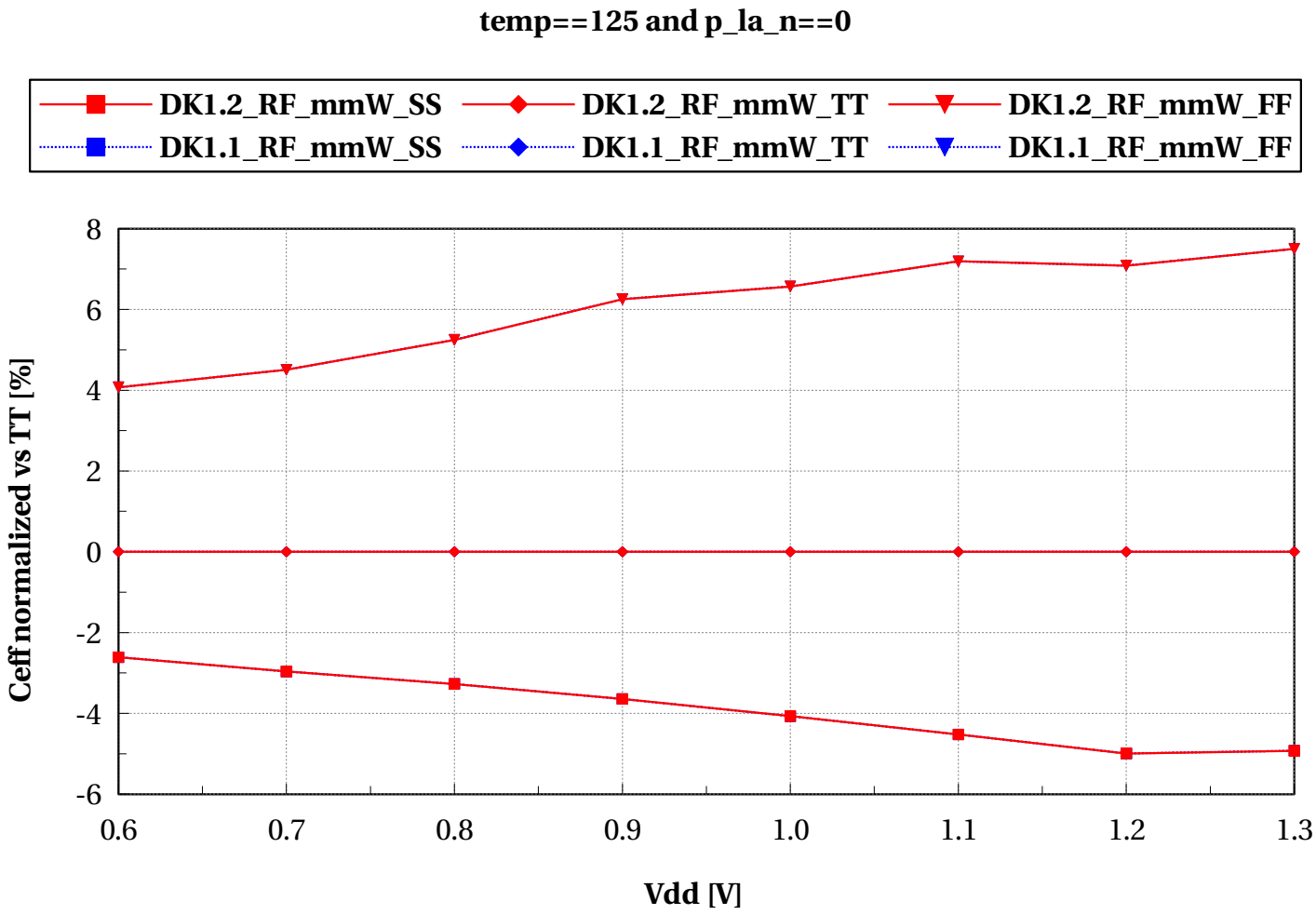
lvtnfet_acc_lvtpfet_acc, Idyn normalized vs TT [%] vs Vdd [V]



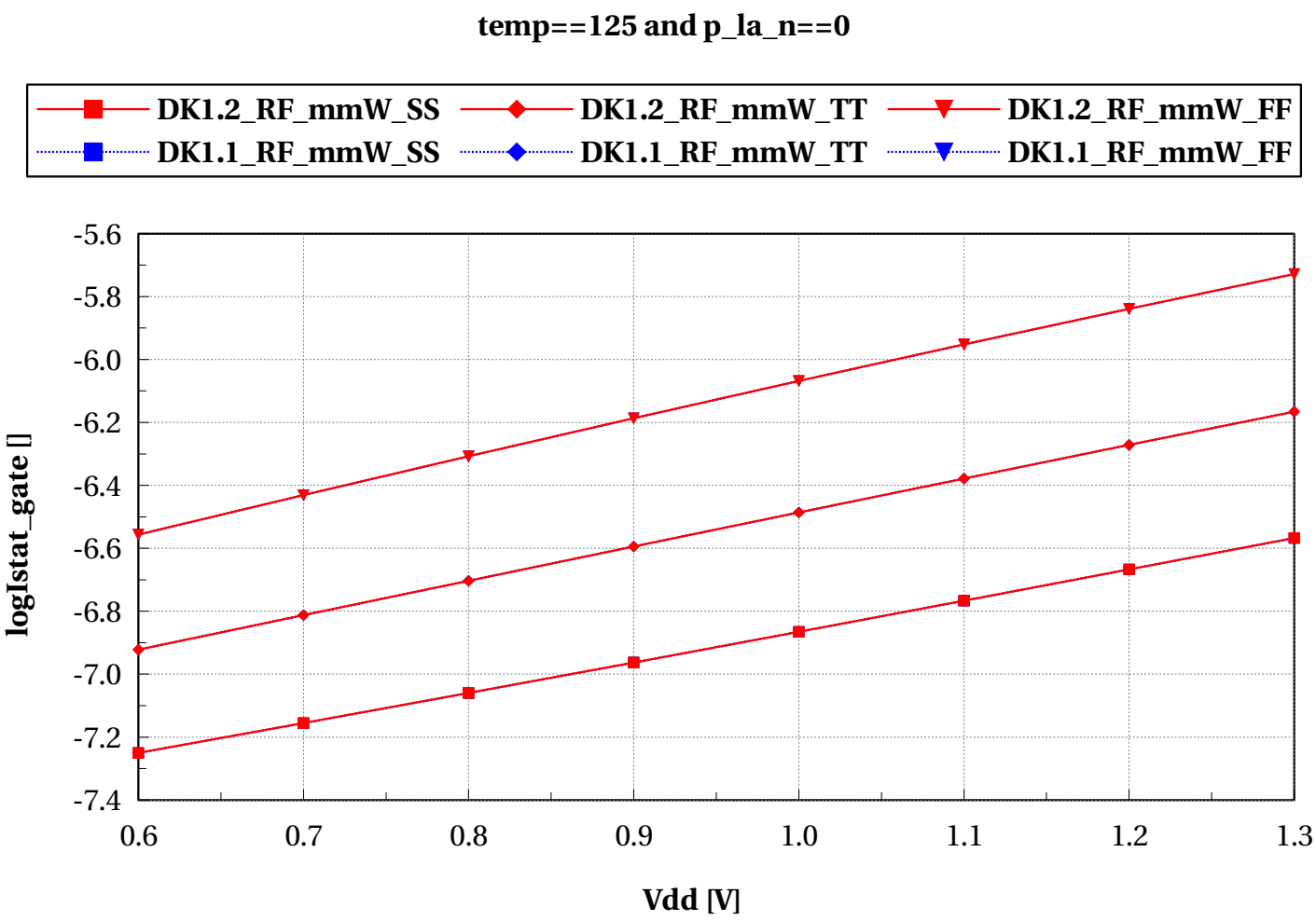
lvtnfet_acc_lvtpfet_acc, Ceff [F] vs Vdd [V]



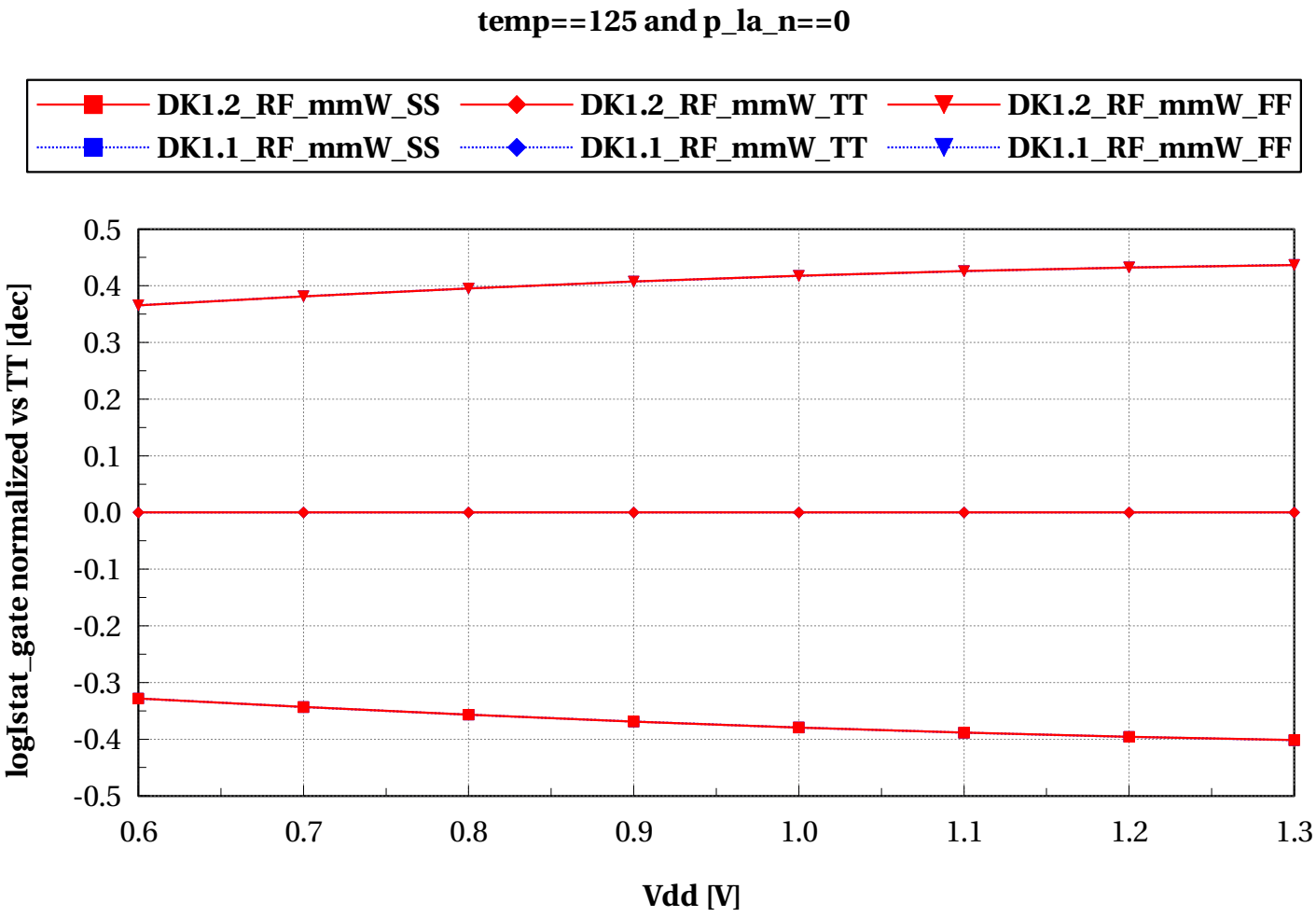
lvtnfet_acc_lvtpfet_acc, Ceff normalized vs TT [%] vs Vdd [V]



lvtnfet_acc_lvtpfet_acc, logIstat_gate [] vs Vdd [V]

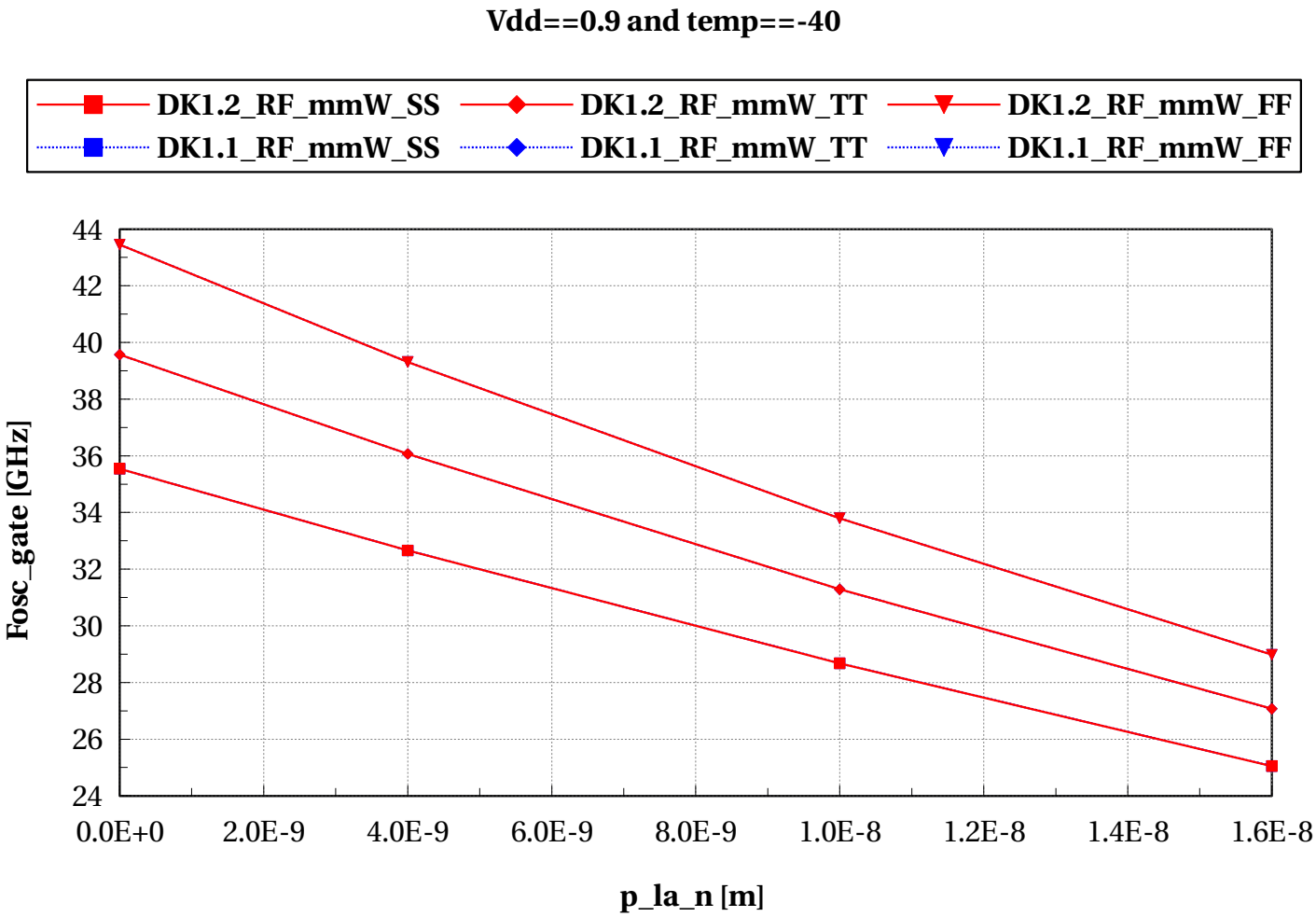


lvtnfet_acc_lvtpfet_acc, logIstat_gate normalized vs TT [dec] vs Vdd [V]

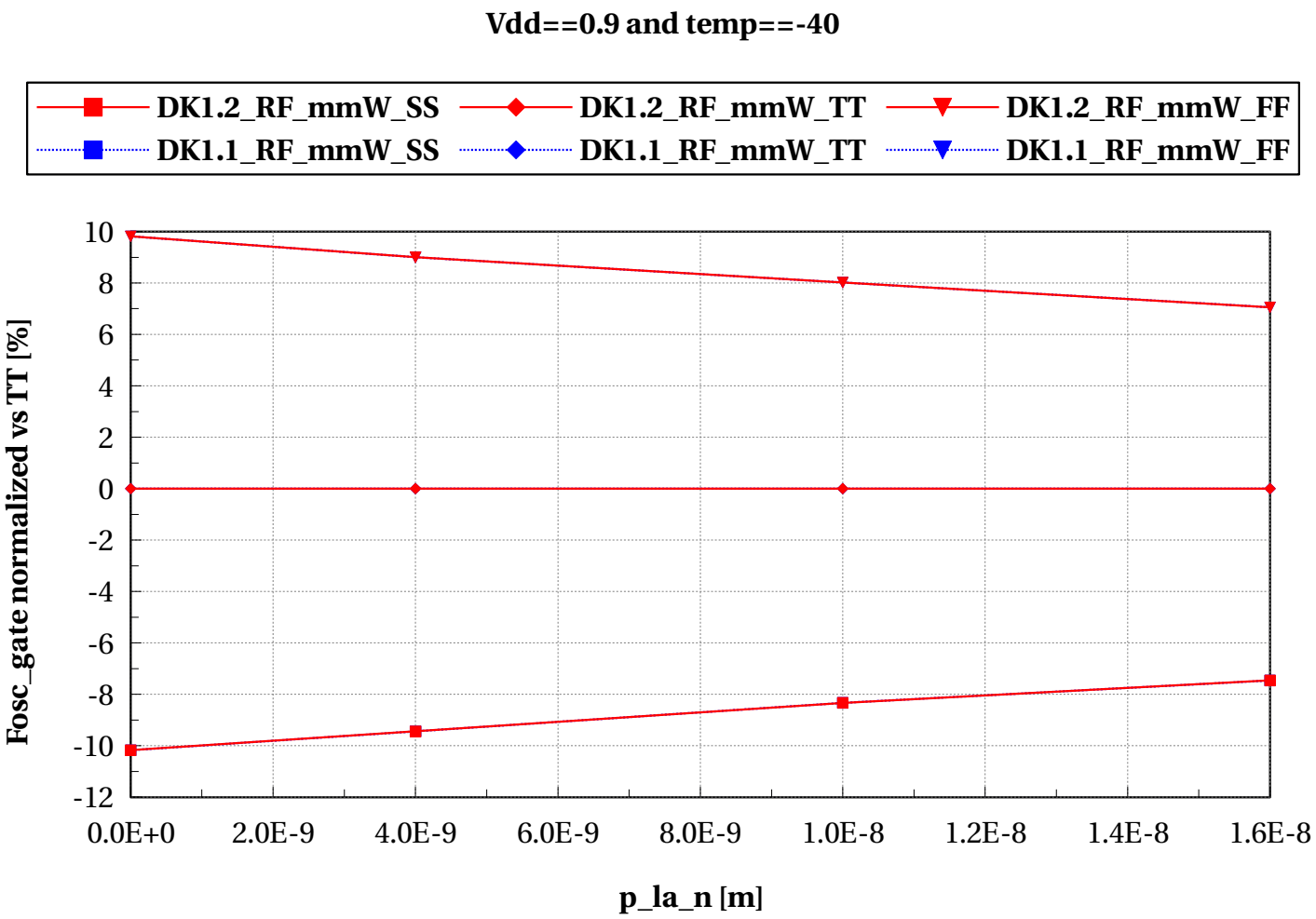


"RO FOM's vs PB @ Vdd=0.9V, T=-40C"

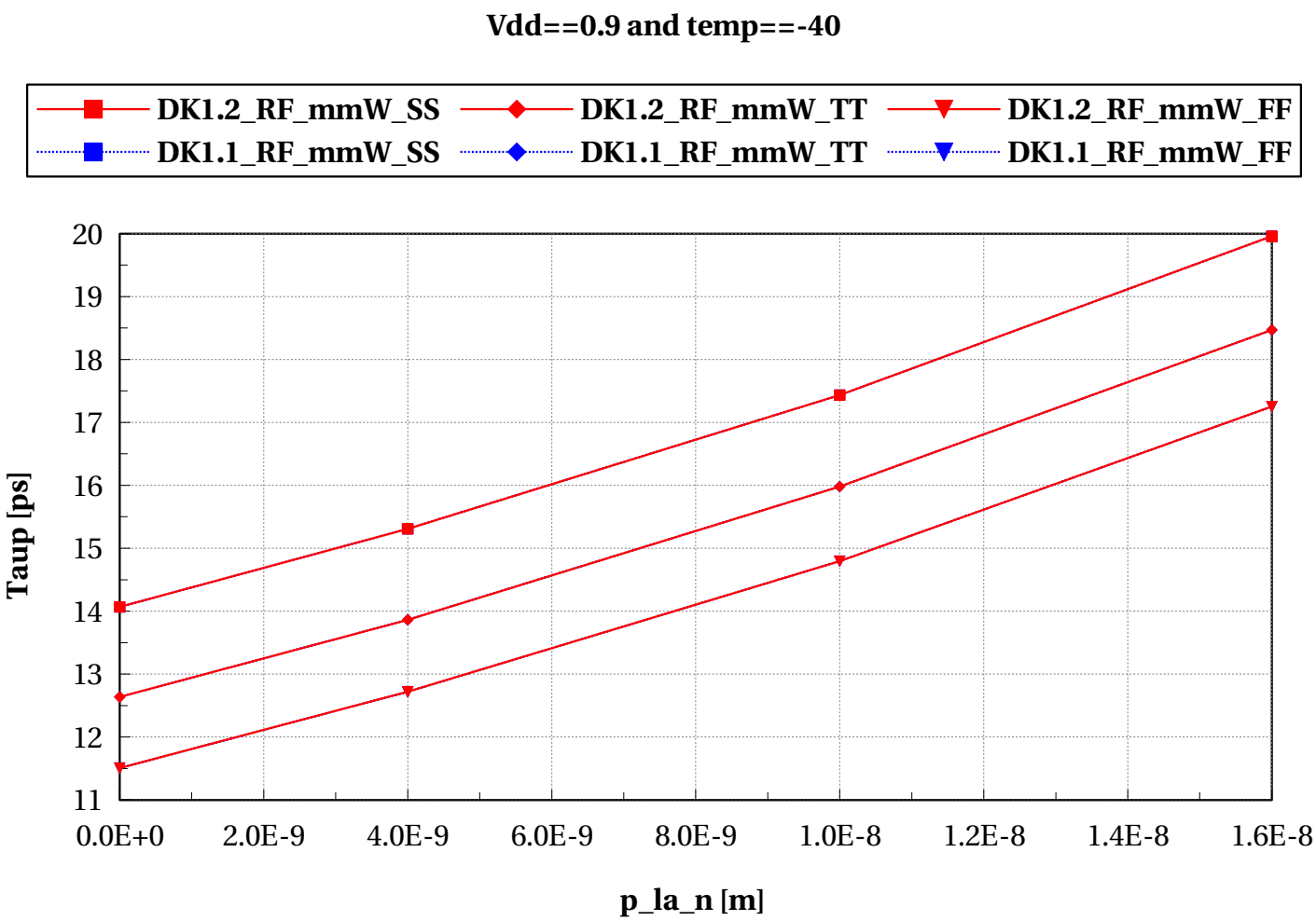
lvtnfet_acc_lvtpfet_acc, Fosc_gate [GHz] vs p_la_n [m]



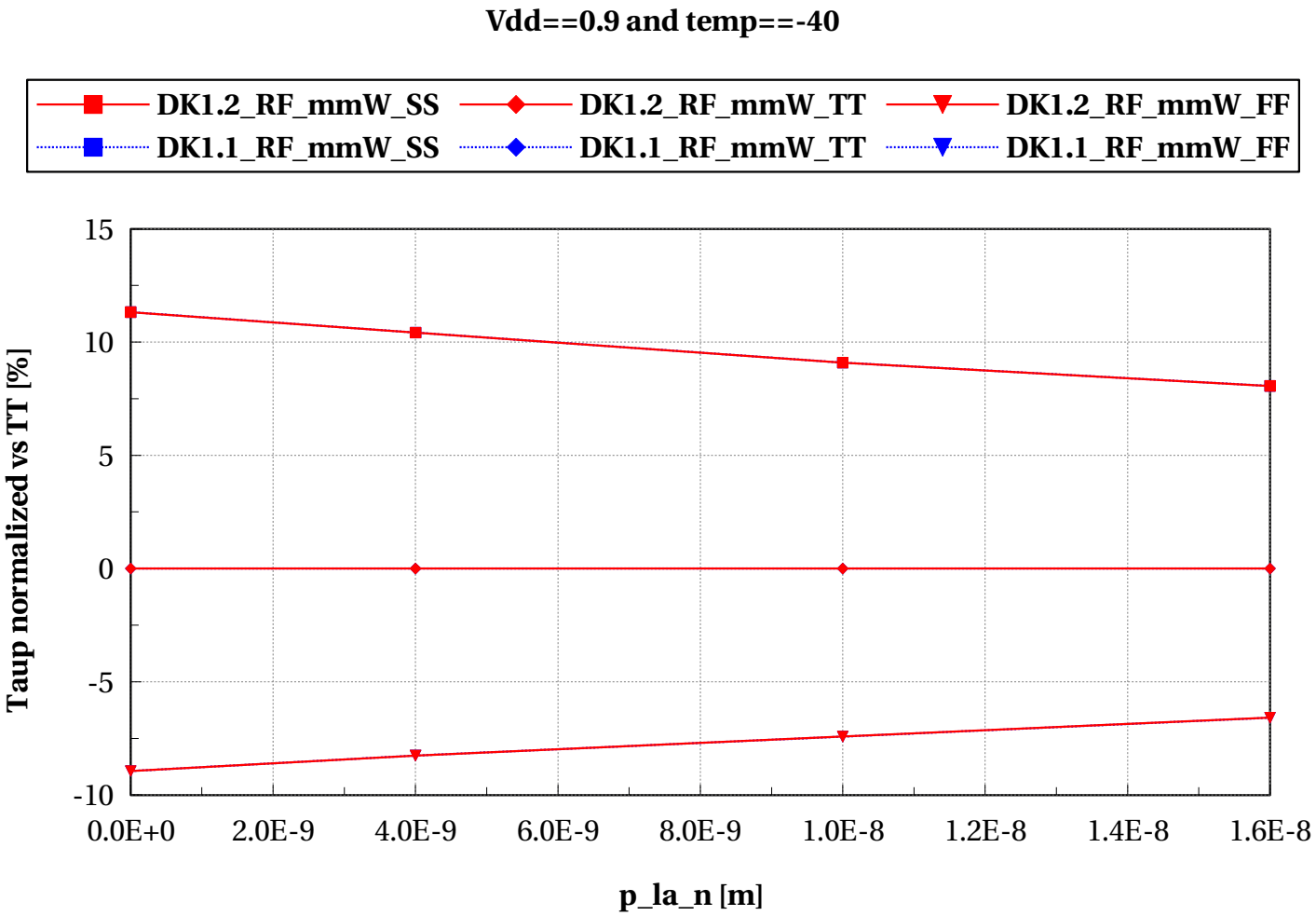
lvtnfet_acc_lvtpfet_acc, Fosc_gate normalized vs TT [%] vs p_la_n [m]



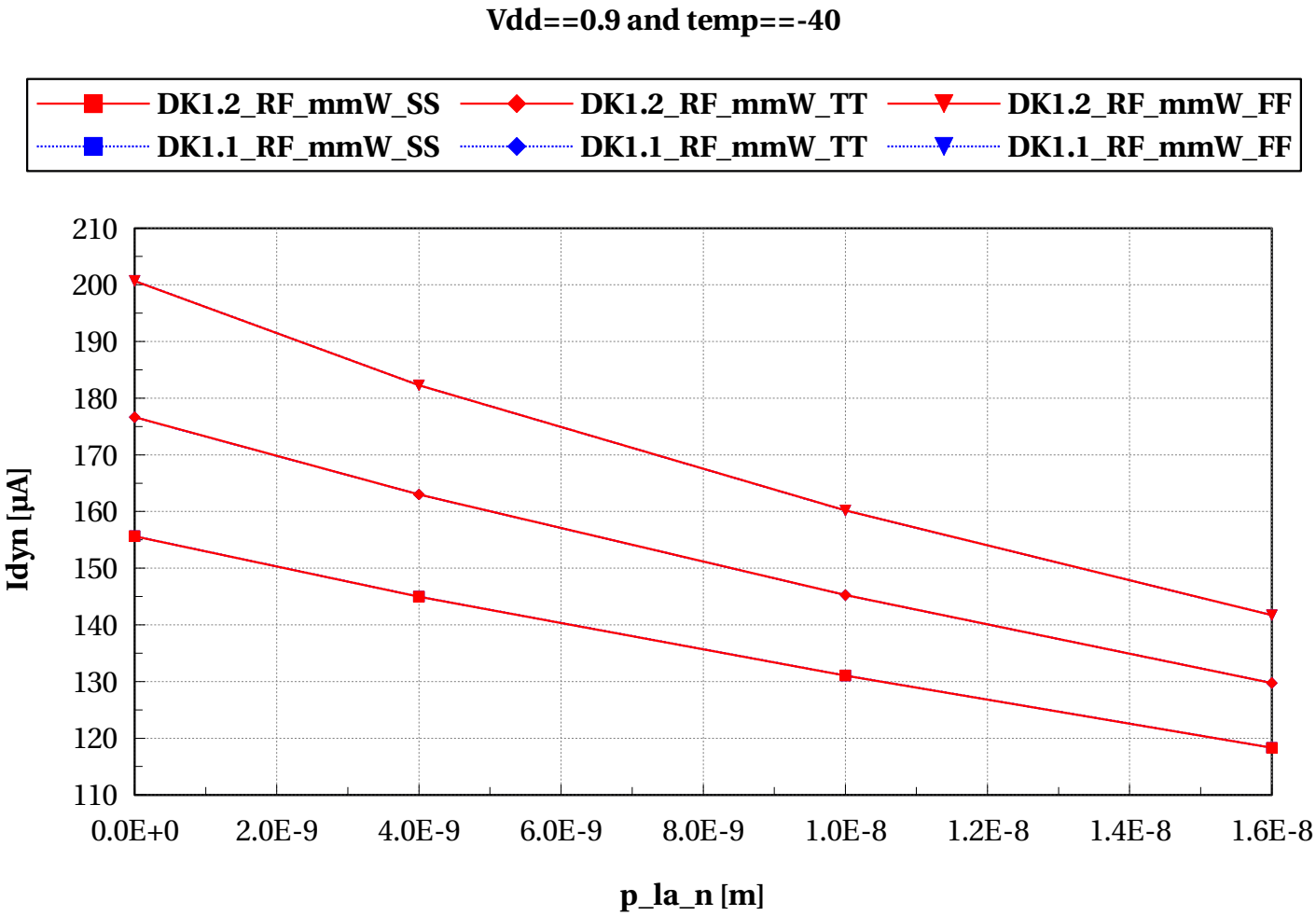
lvtnfet_acc_lvtpfet_acc, Taup [ps] vs p_la_n [m]



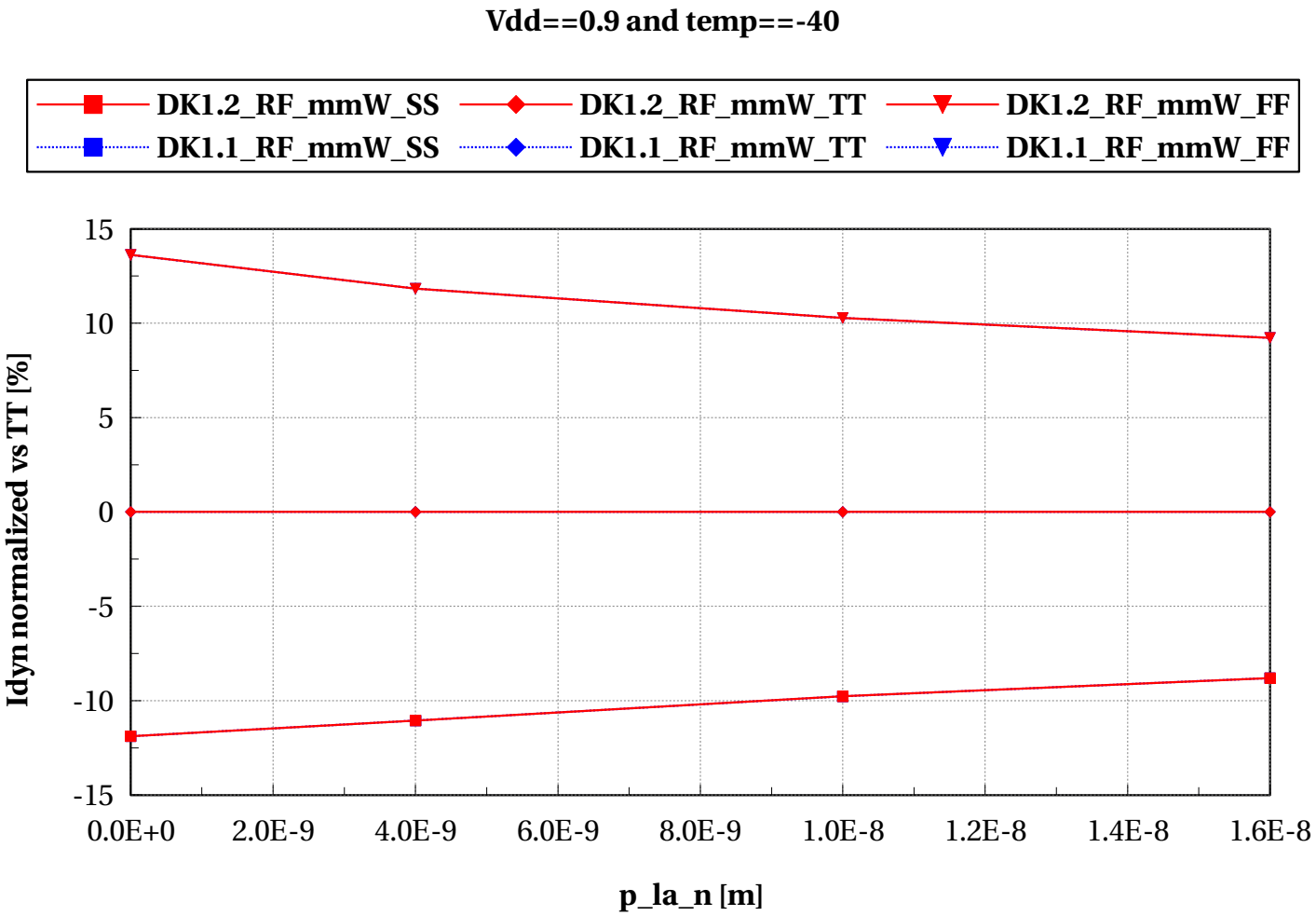
lvtnfet_acc_lvtpfet_acc, Taup normalized vs TT [%] vs p_la_n [m]



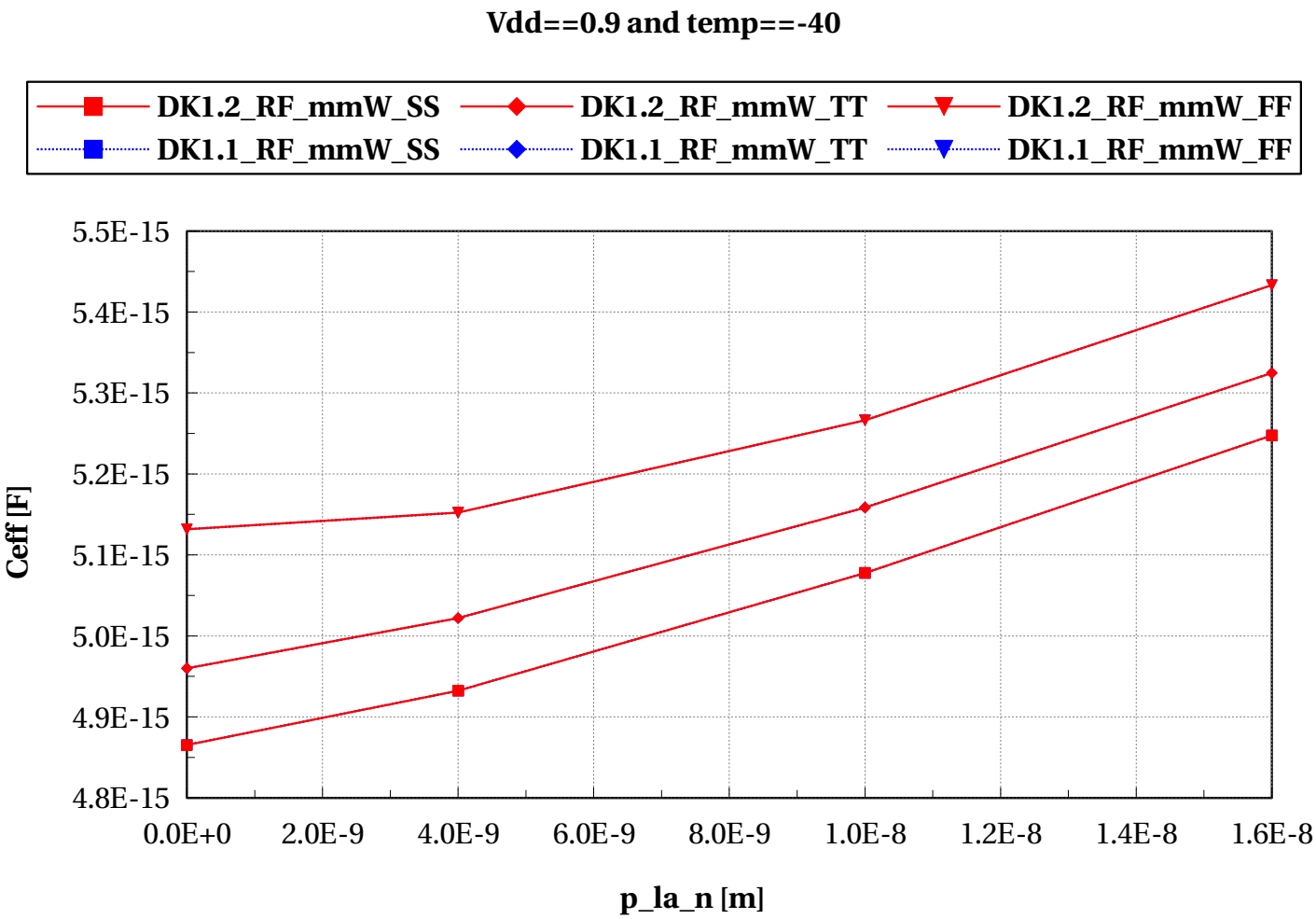
lvtnfet_acc_lvtpfet_acc, Idyn [µA] vs p_la_n [m]



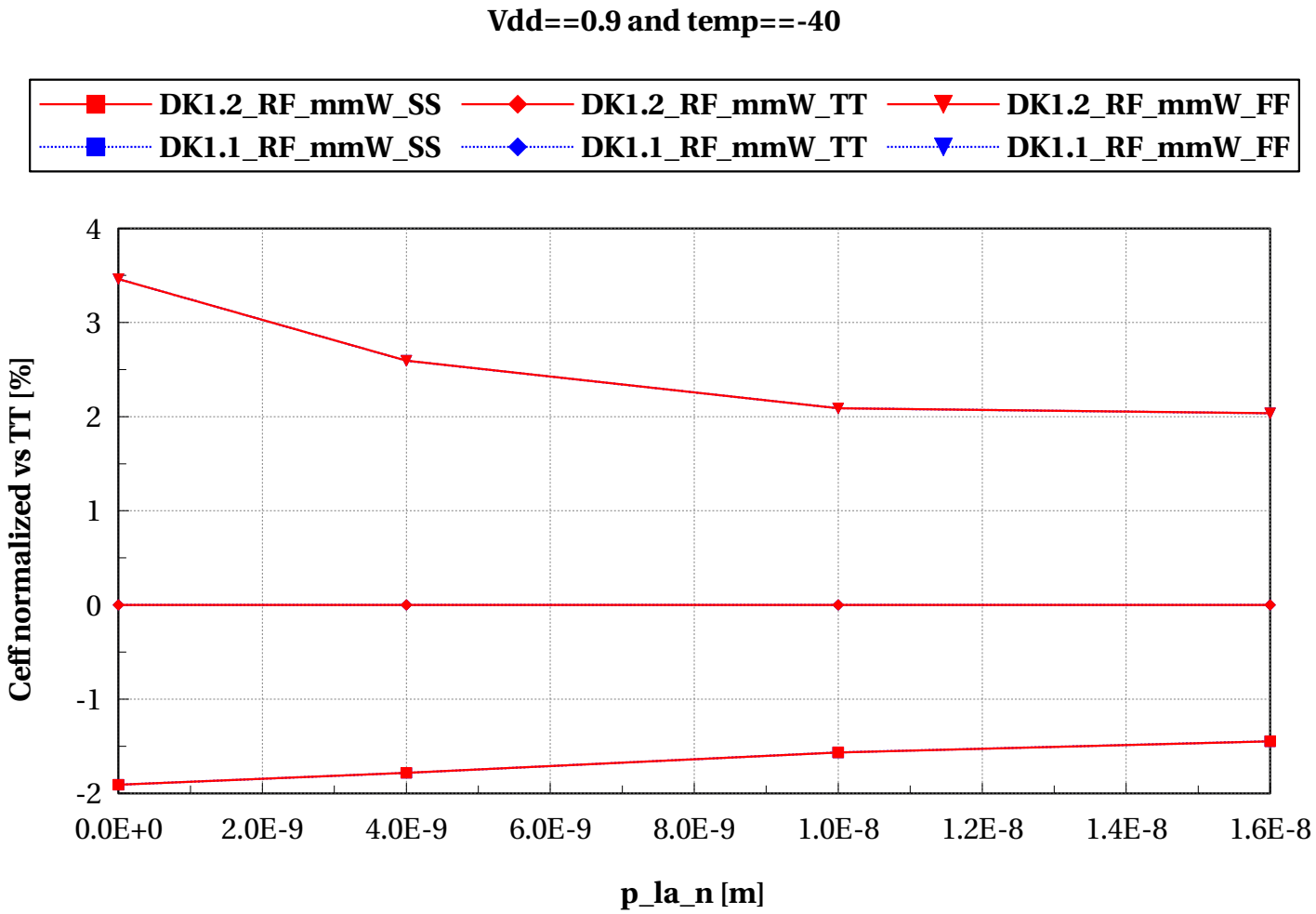
lvtnfet_acc_lvtpfet_acc, Idyn normalized vs TT [%] vs p_la_n [m]



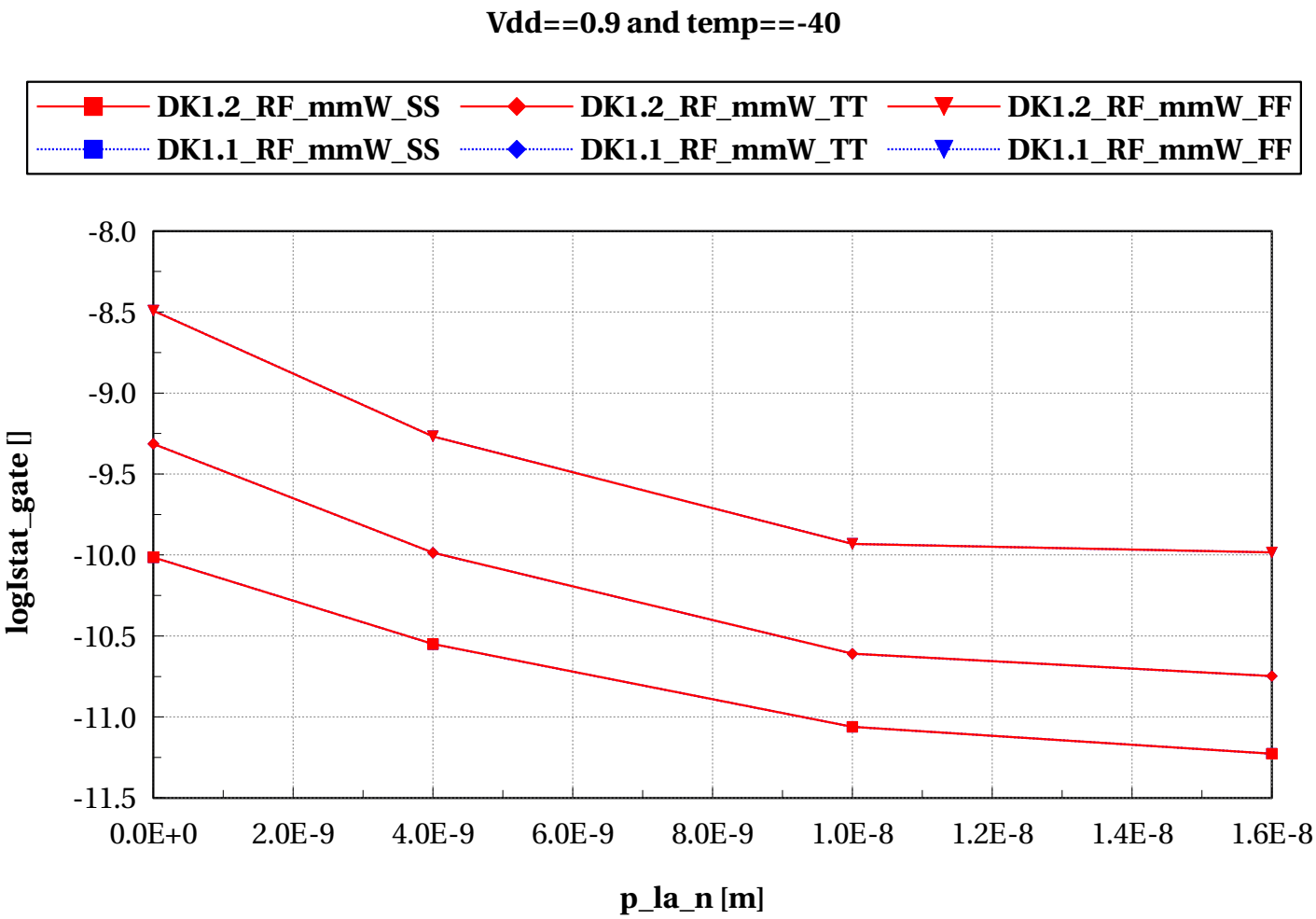
lvtnfet_acc_lvtpfet_acc, Ceff [F] vs p_la_n [m]



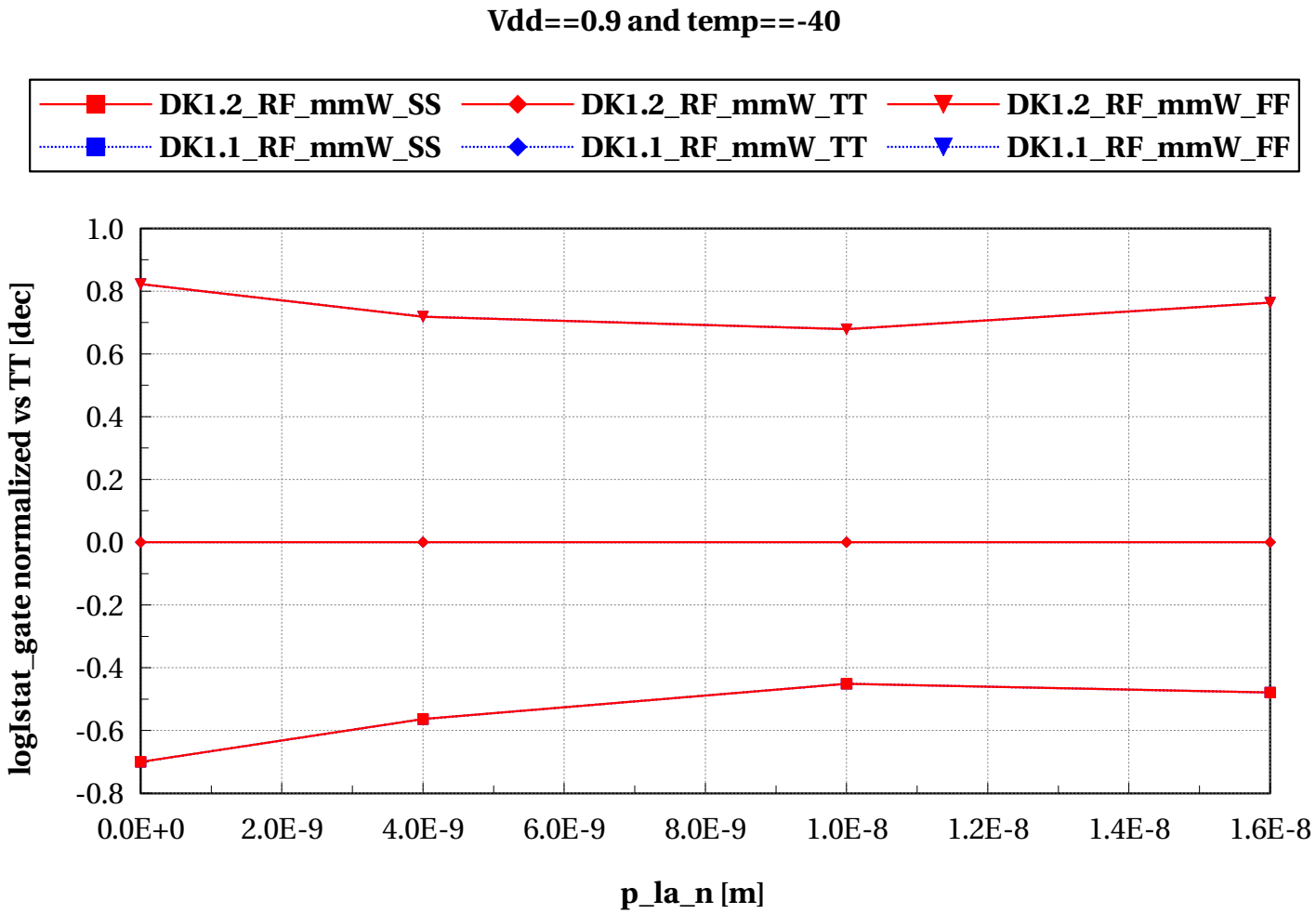
lvtnfet_acc_lvtpfet_acc, Ceff normalized vs TT [%] vs p_la_n [m]



lvtnfet_acc_lvtpfet_acc, logIstat_gate [] vs p_la_n [m]

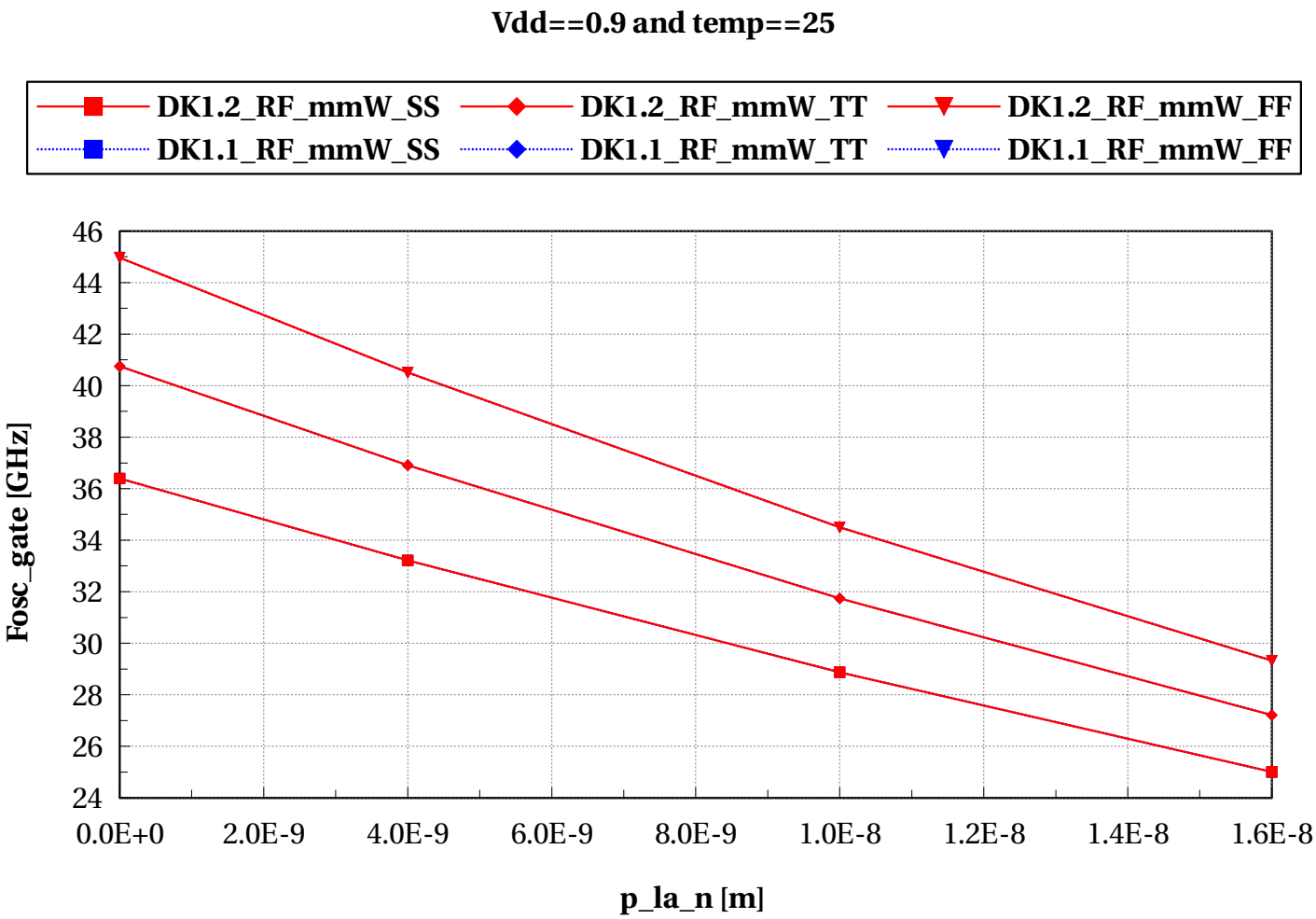


lvtnfet_acc_lvtpfet_acc, logIstat_gate normalized vs TT [dec] vs p_la_n [m]

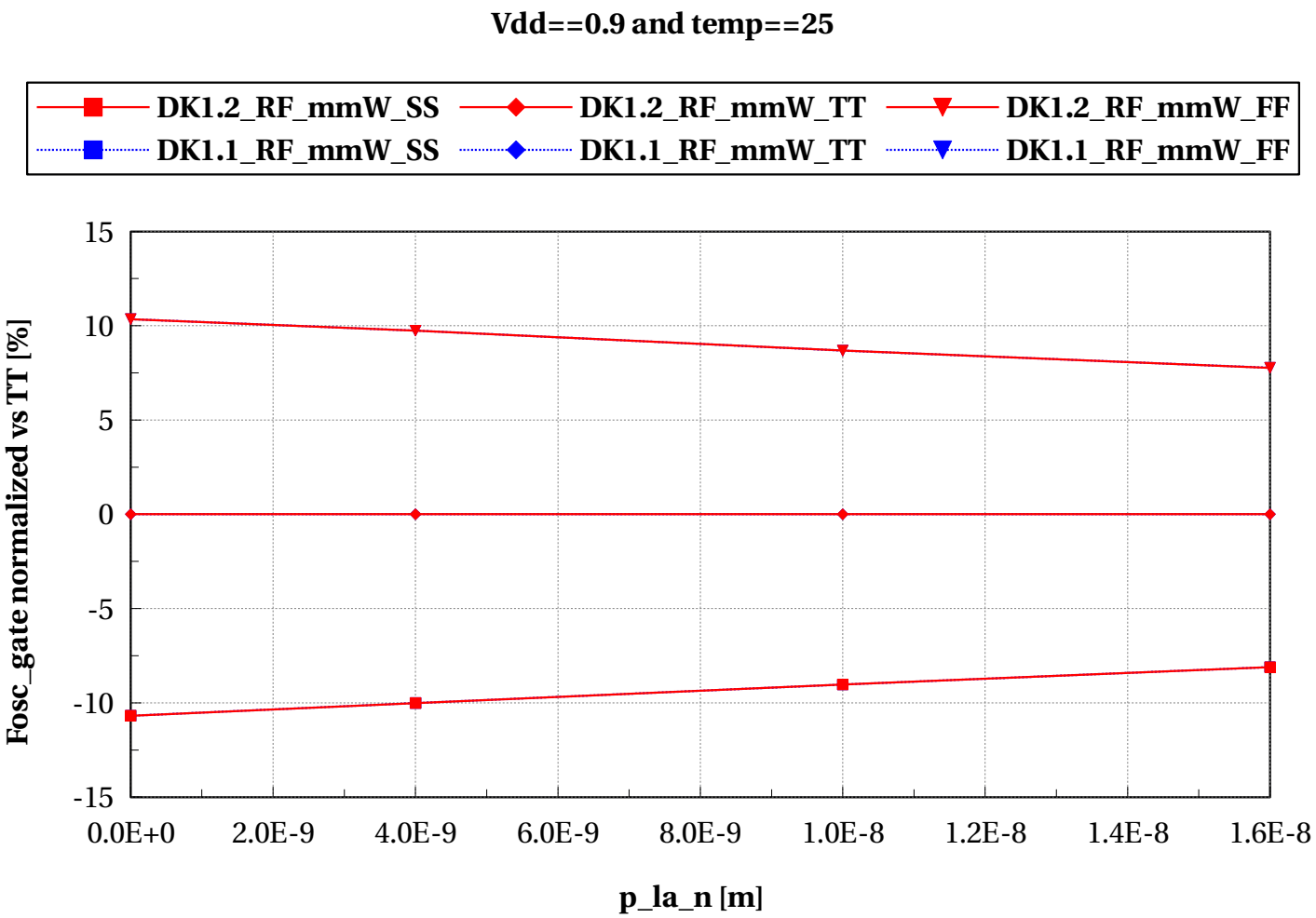


"RO FOM's vs PB @ Vdd=0.9V, T=25C"

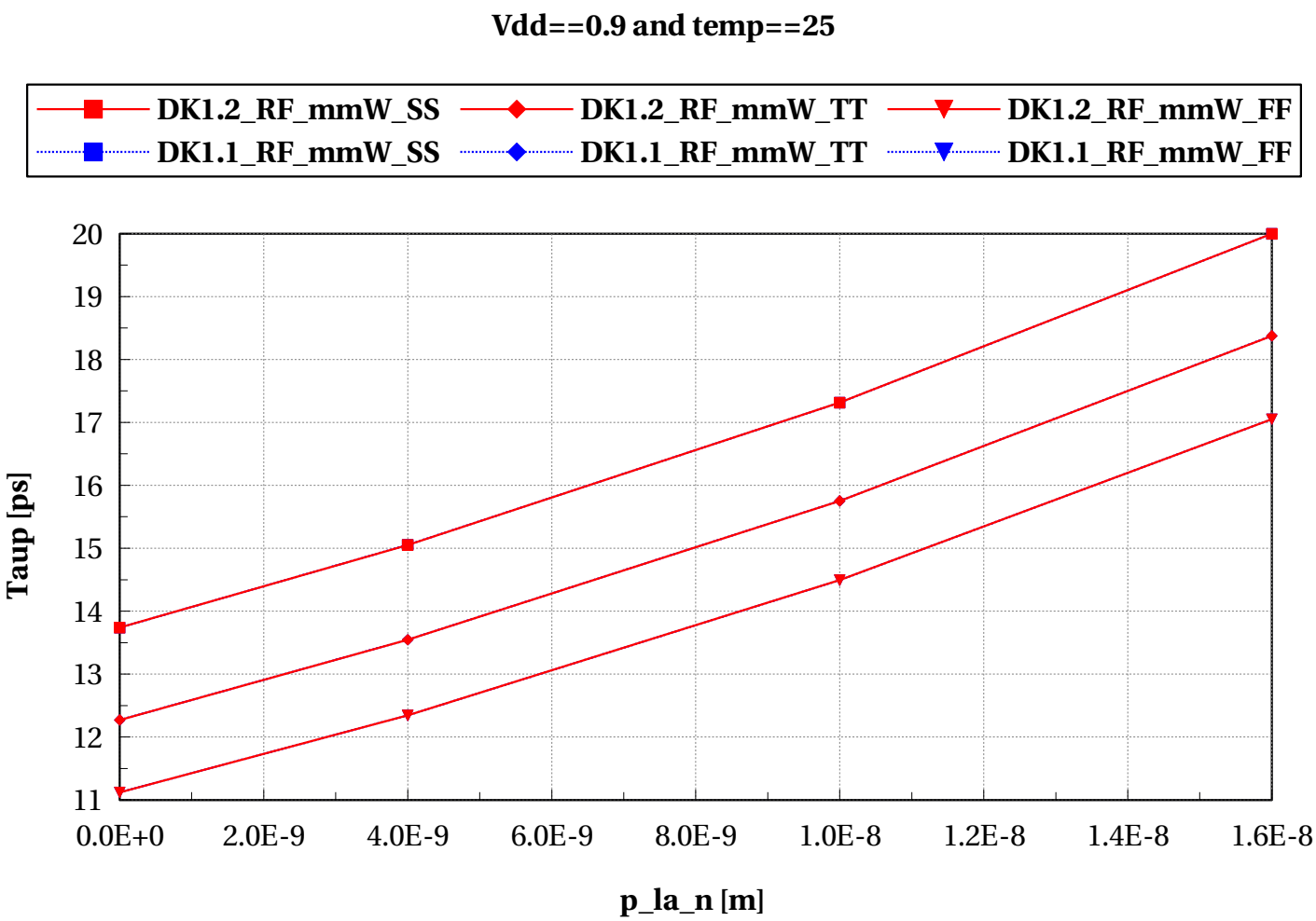
lvtnfet_acc_lvtpfet_acc, Fosc_gate [GHz] vs p_la_n [m]



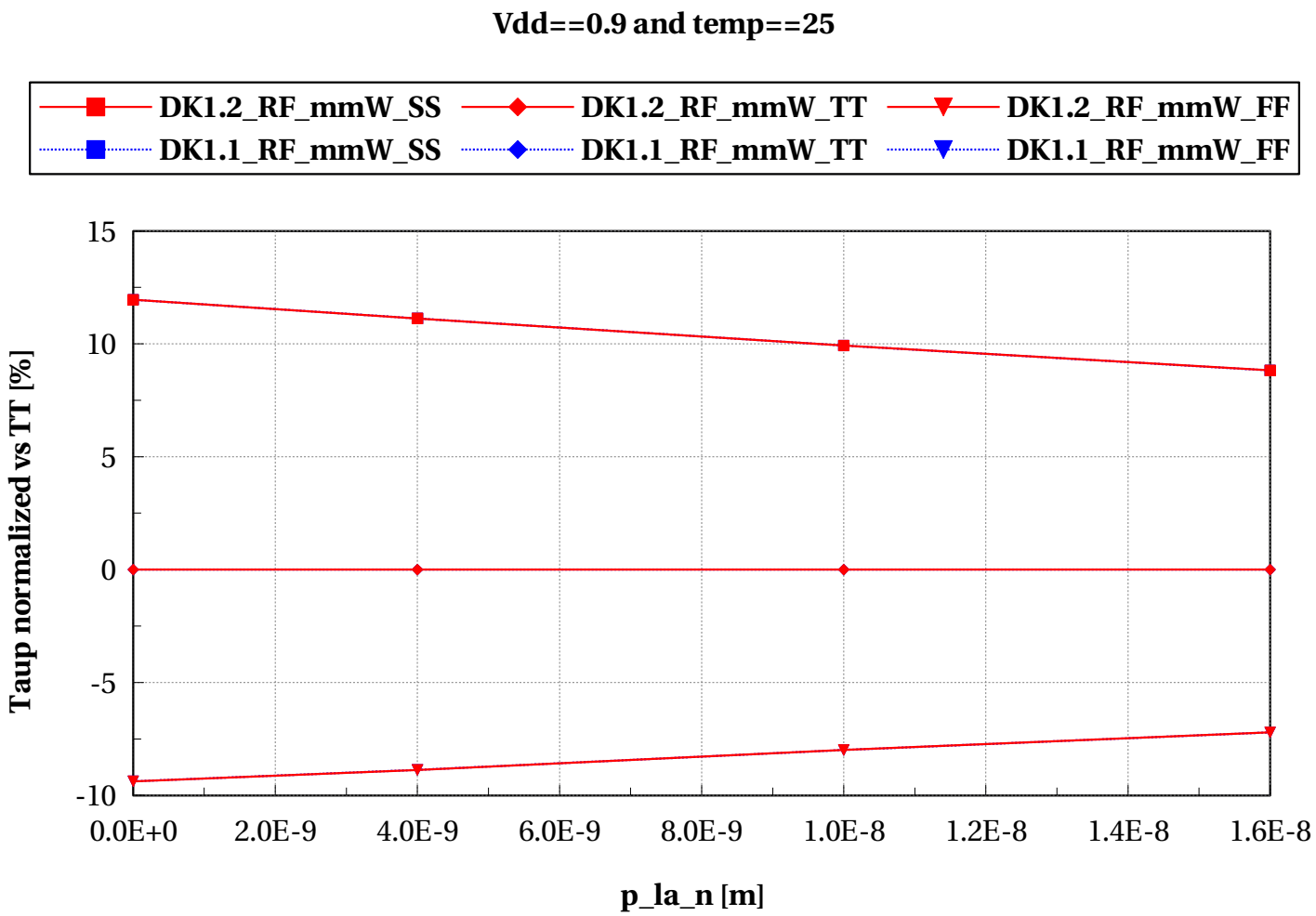
lvtnfet_acc_lvtpfet_acc, Fosc_gate normalized vs TT [%] vs p_la_n [m]



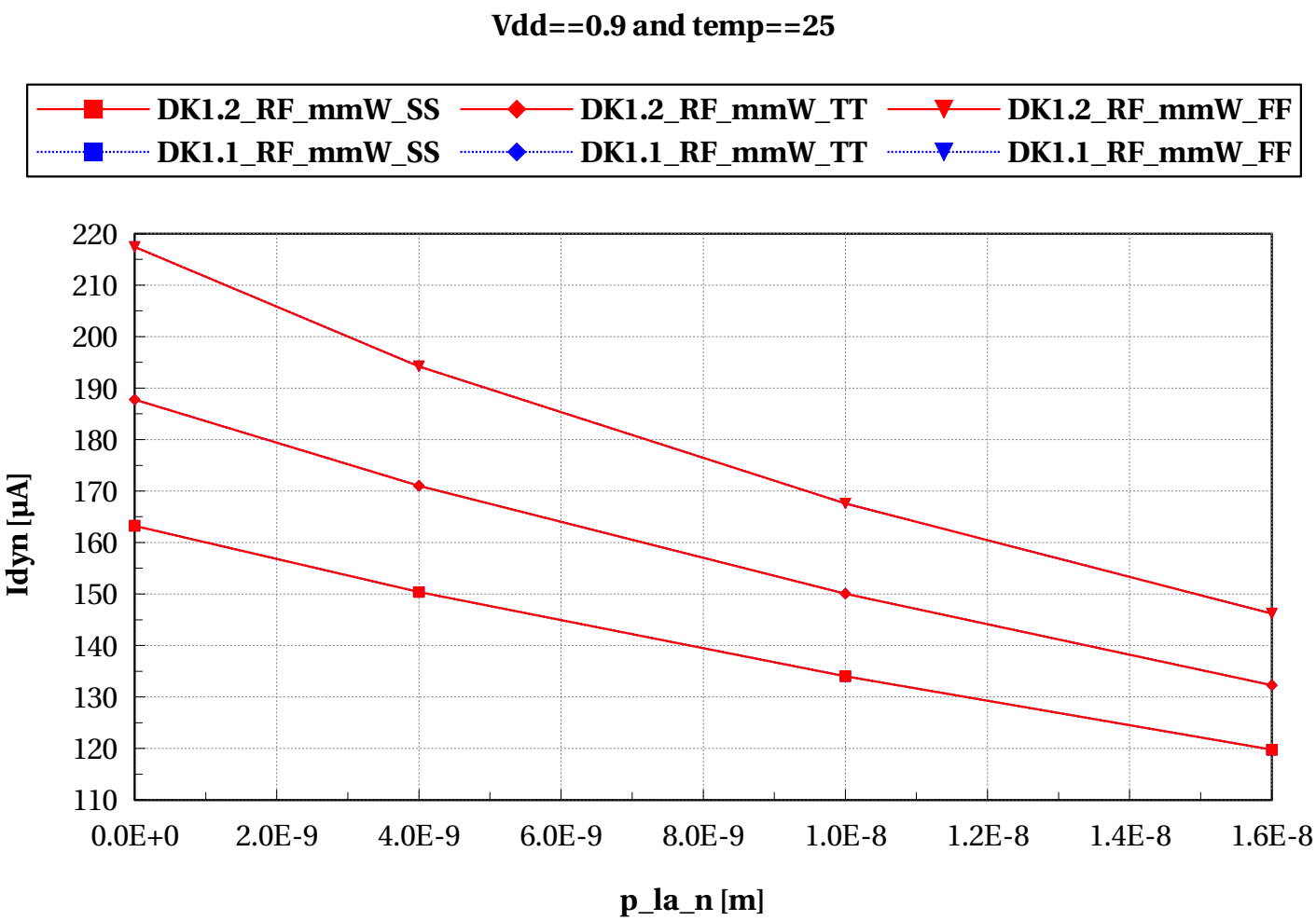
lvtnfet_acc_lvtpfet_acc, Taup [ps] vs p_la_n [m]



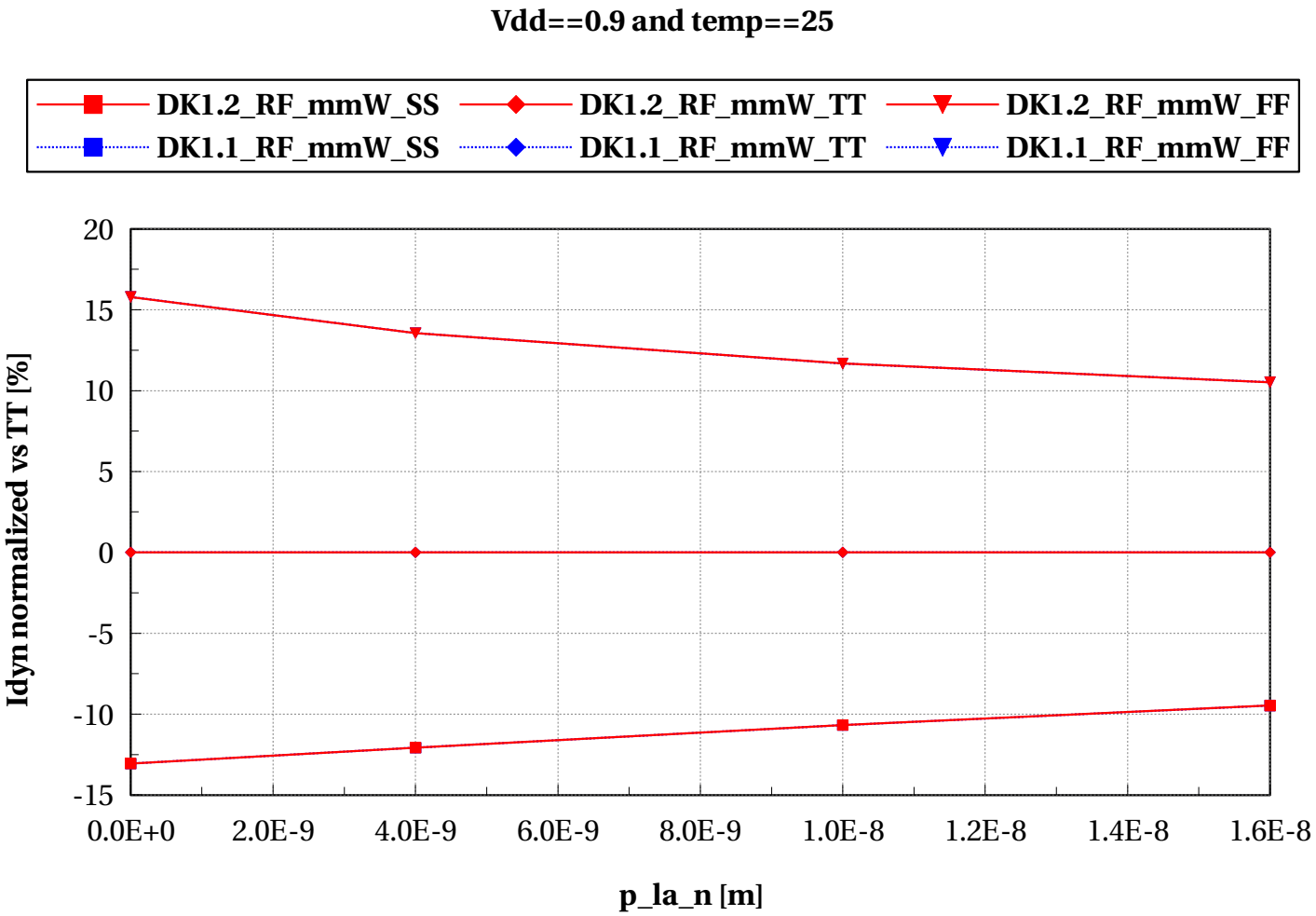
lvtnfet_acc_lvtpfet_acc, Taup normalized vs TT [%] vs p_la_n [m]



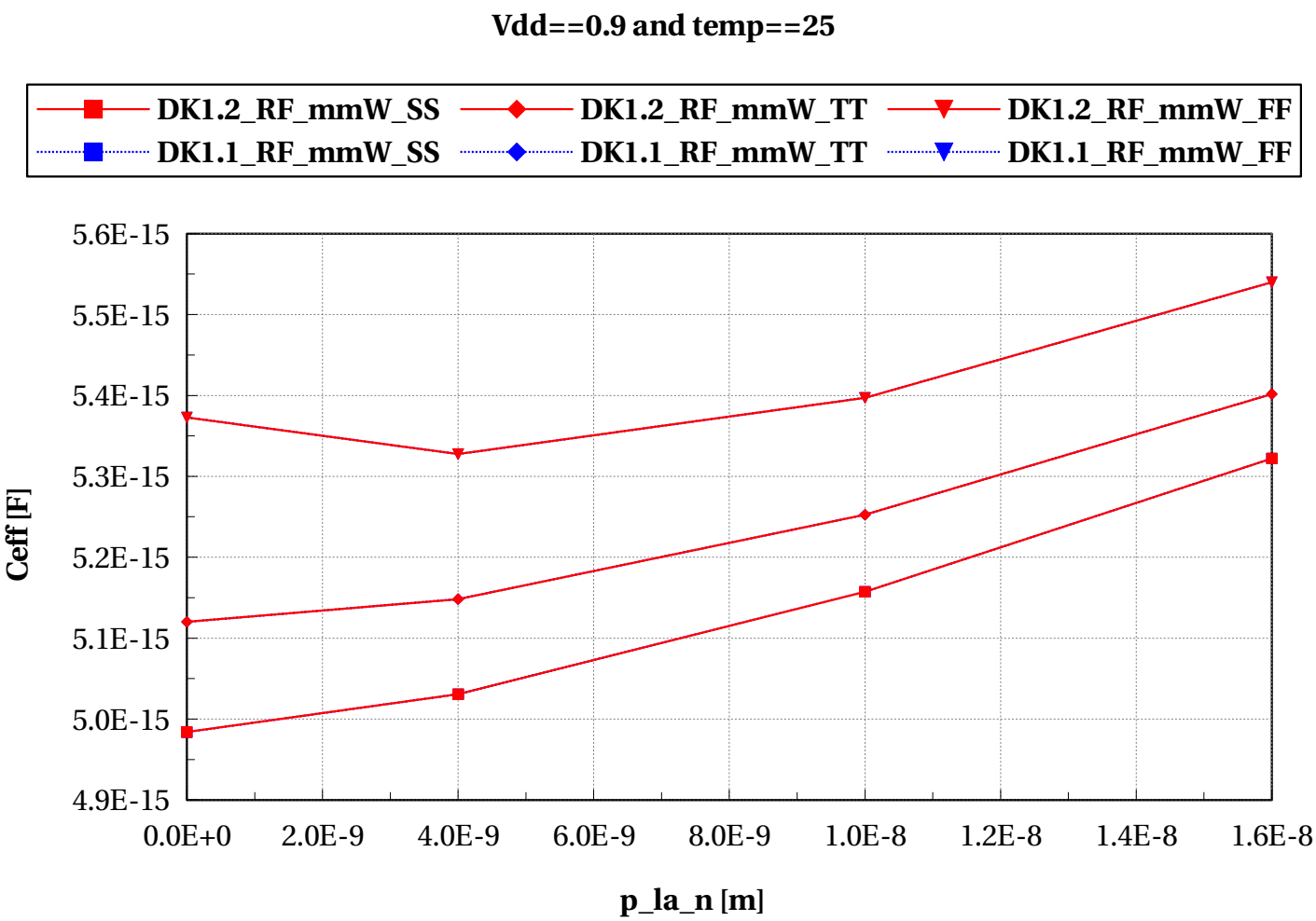
lvtnfet_acc_lvtpfet_acc, Idyn [µA] vs p_la_n [m]



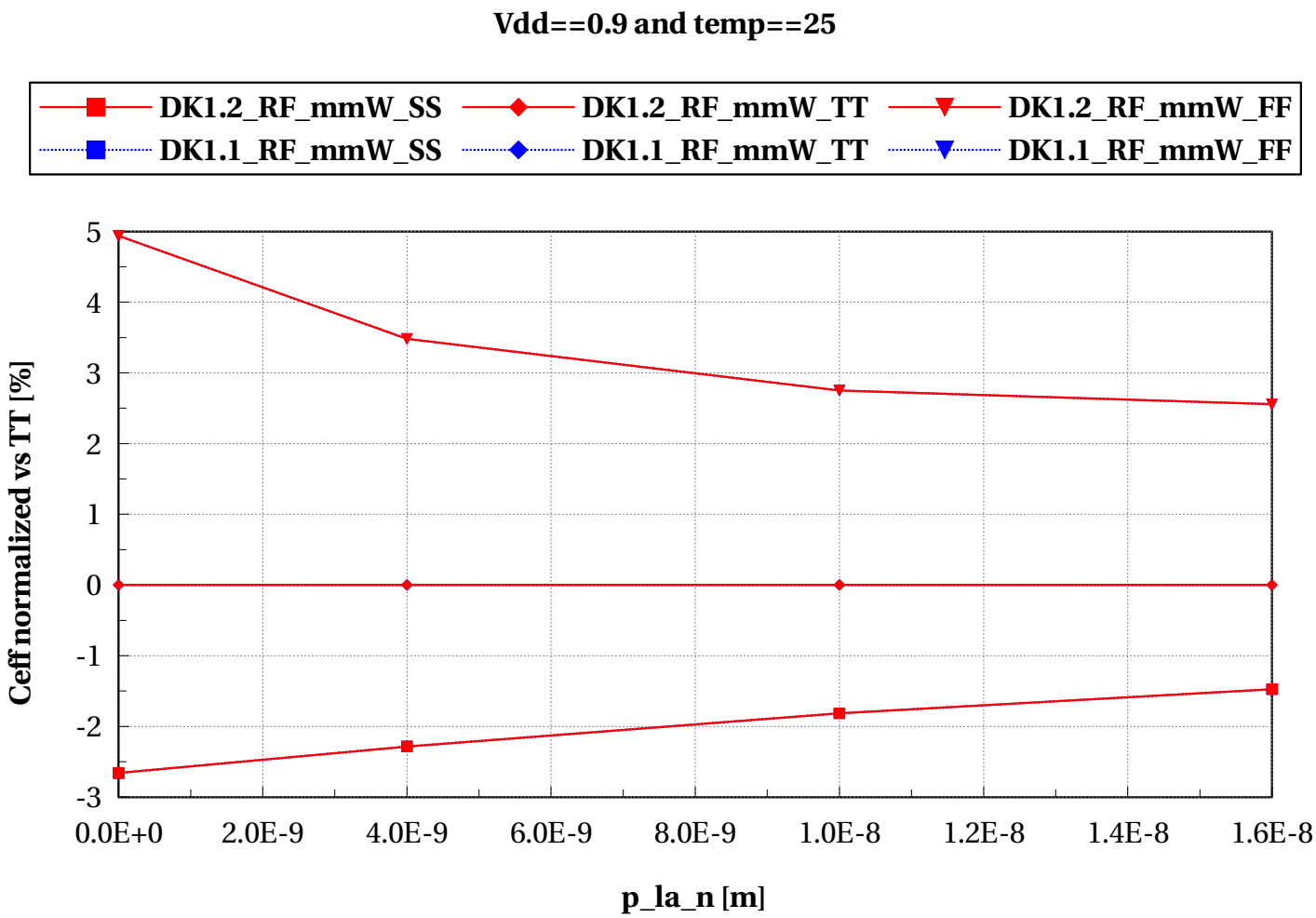
lvtnfet_acc_lvtpfet_acc, Idyn normalized vs TT [%] vs p_la_n [m]



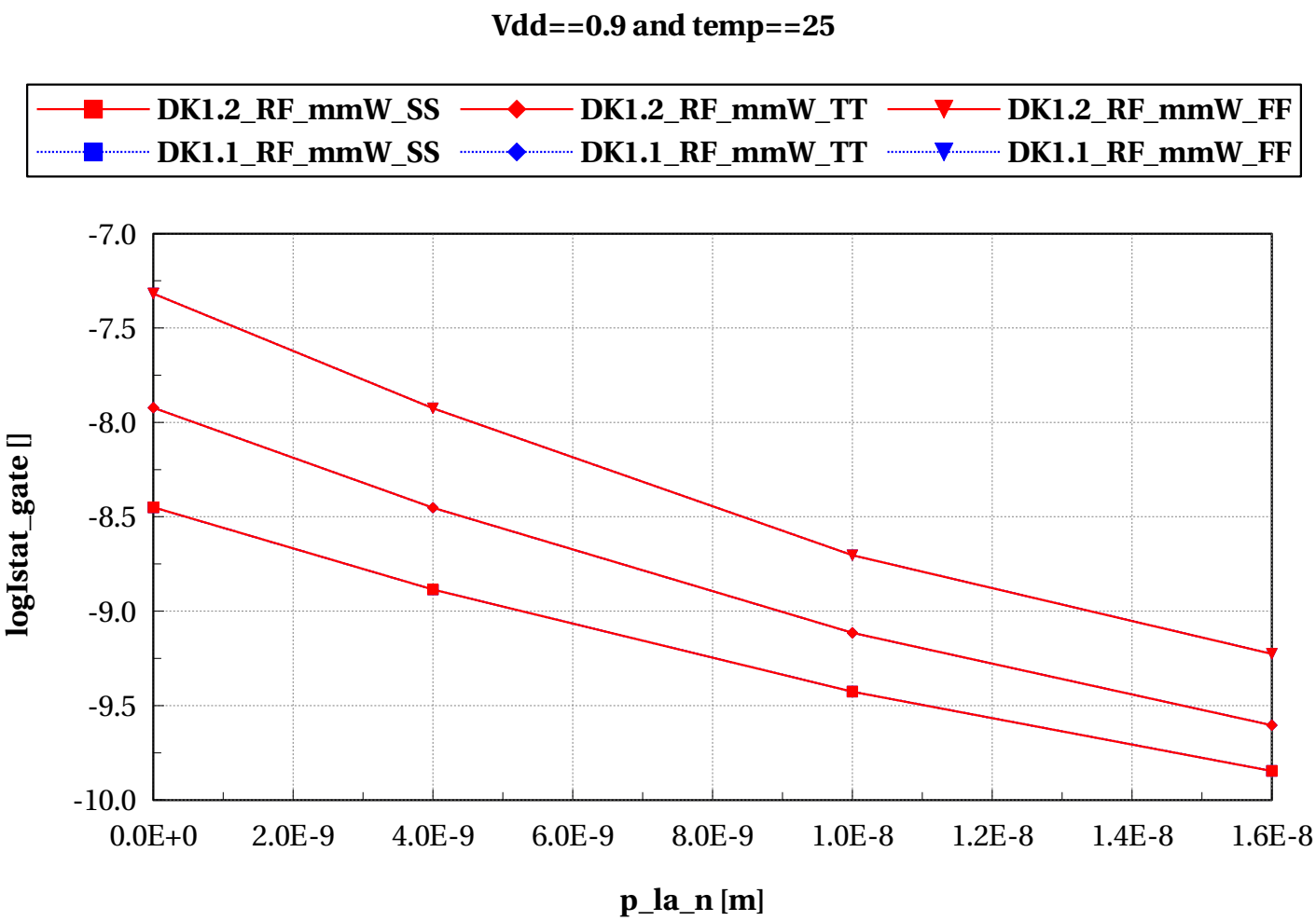
lvtnfet_acc_lvtpfet_acc, Ceff [F] vs p_la_n [m]



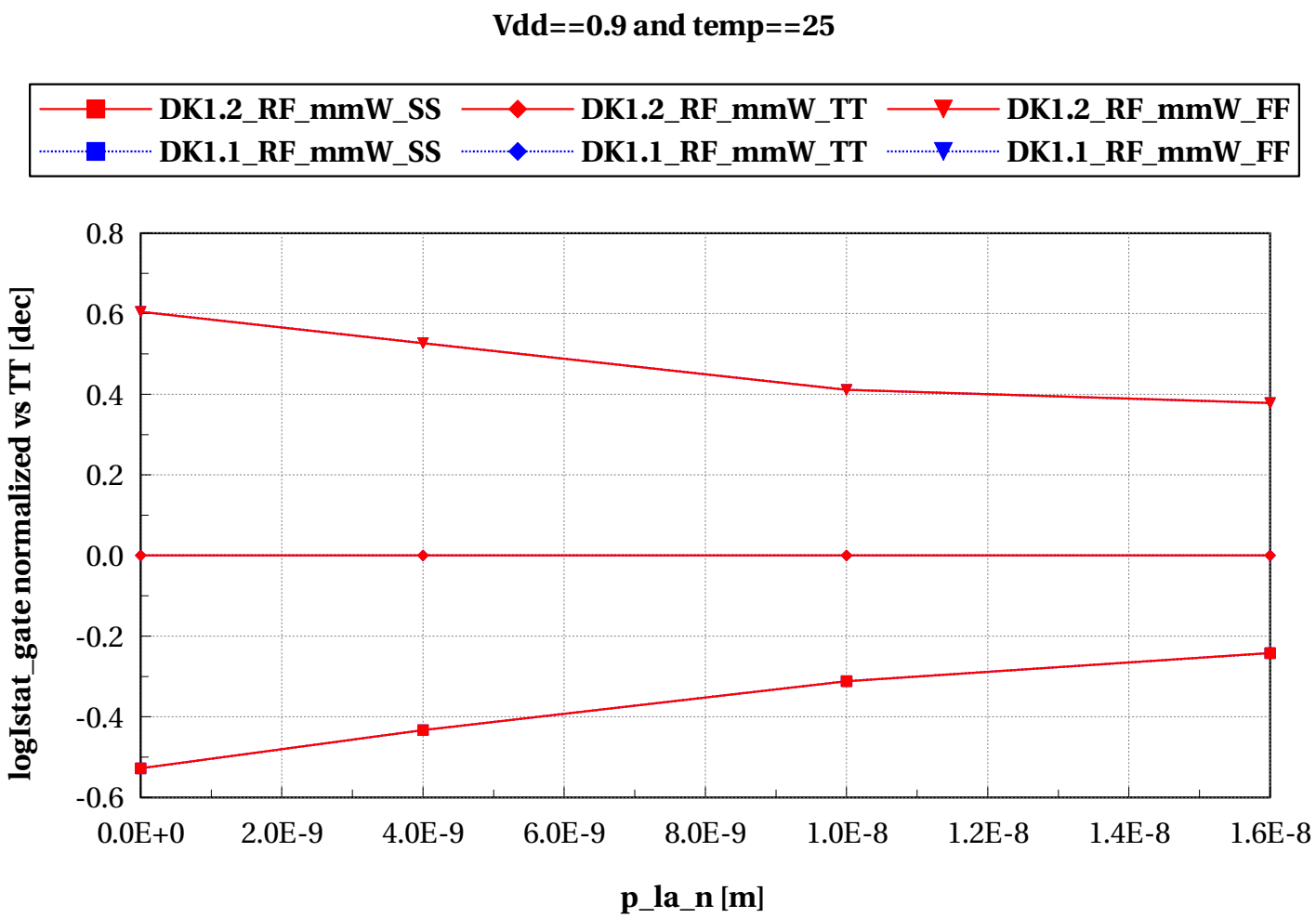
lvtnfet_acc_lvtpfet_acc, Ceff normalized vs TT [%] vs p_la_n [m]



lvtnfet_acc_lvtpfet_acc, logIstat_gate [] vs p_la_n [m]

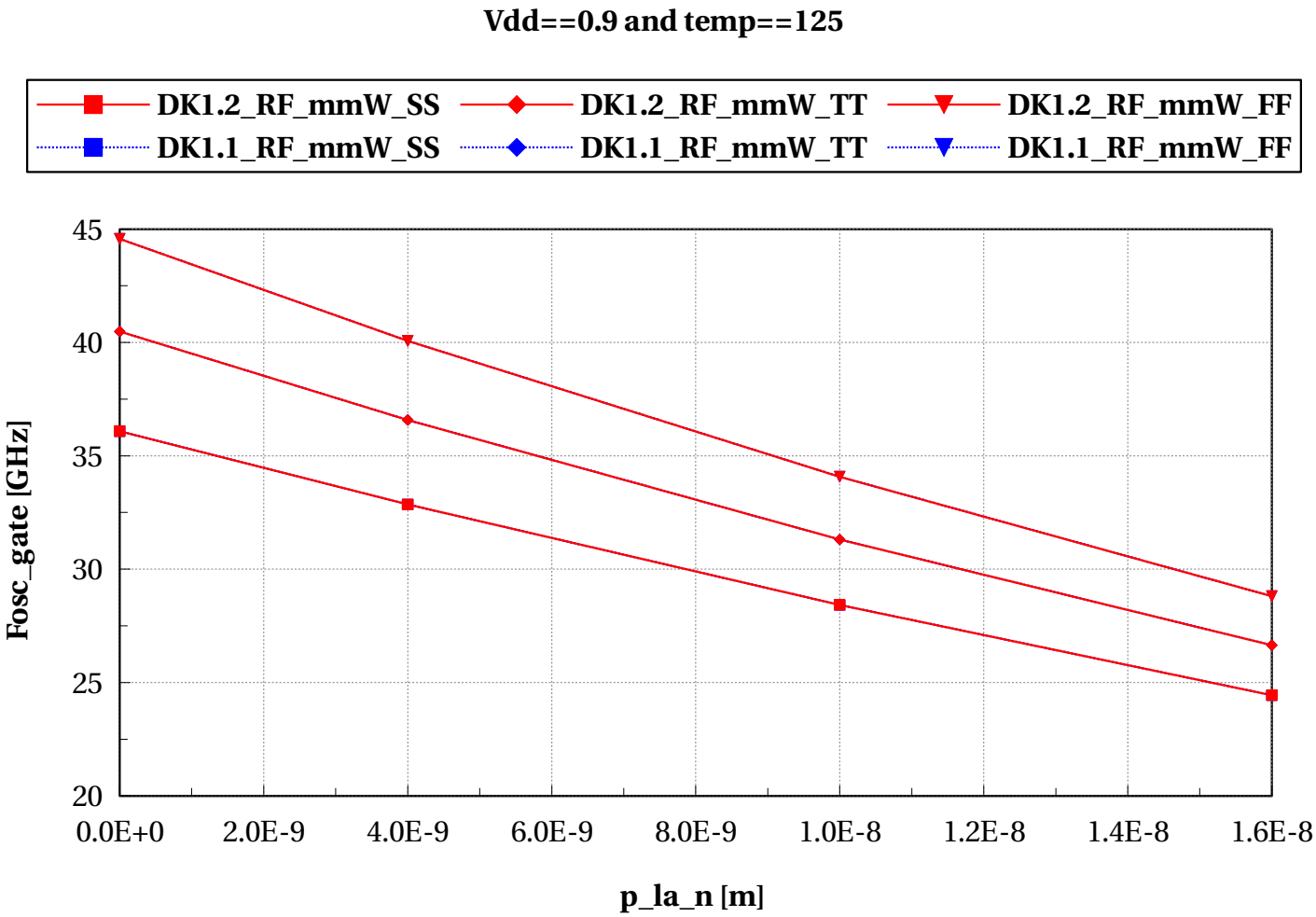


lvtnfet_acc_lvtpfet_acc, logIstat_gate normalized vs TT [dec] vs p_la_n [m]

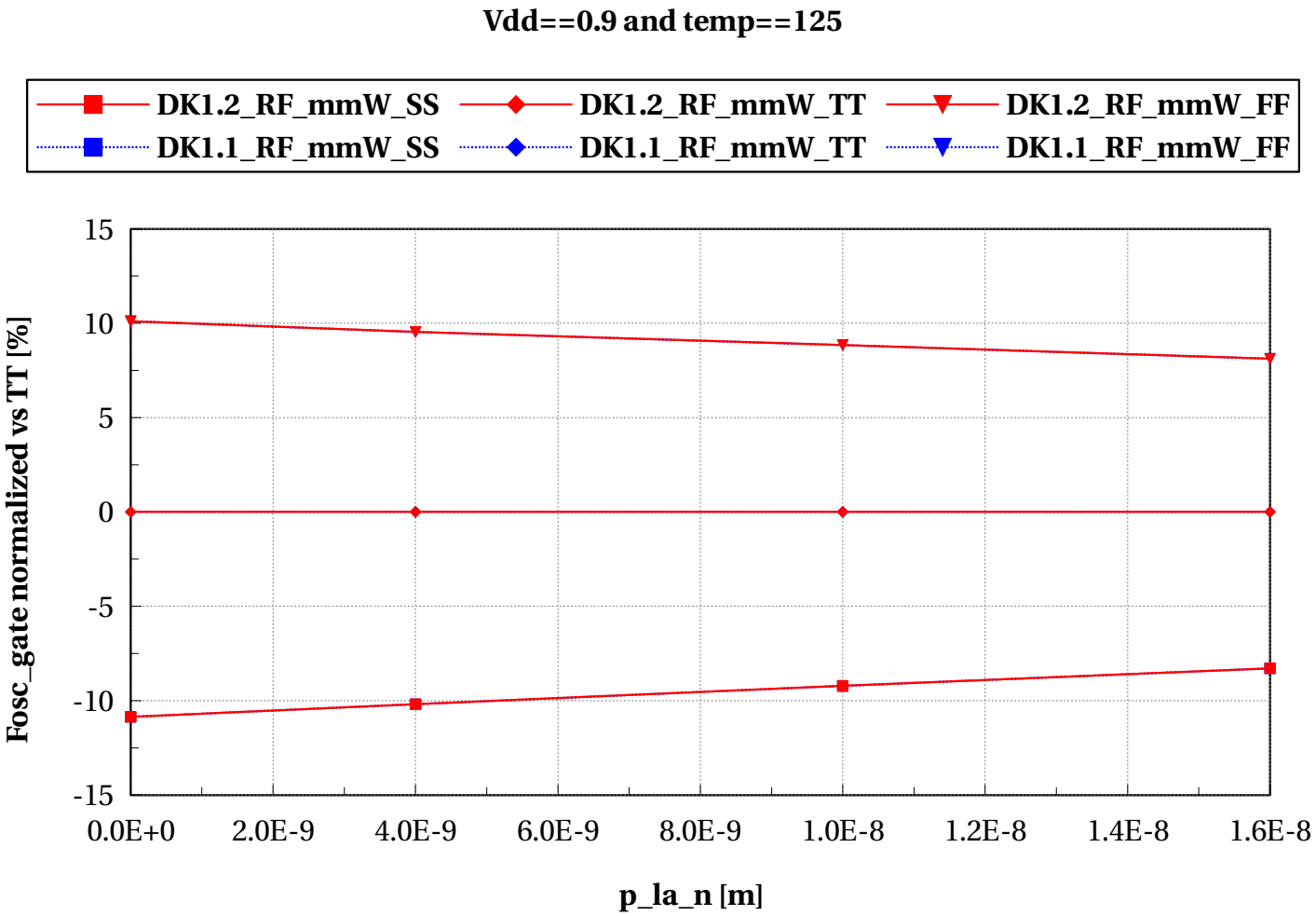


"RO FOM's vs PB @ Vdd=0.9V, T=125C"

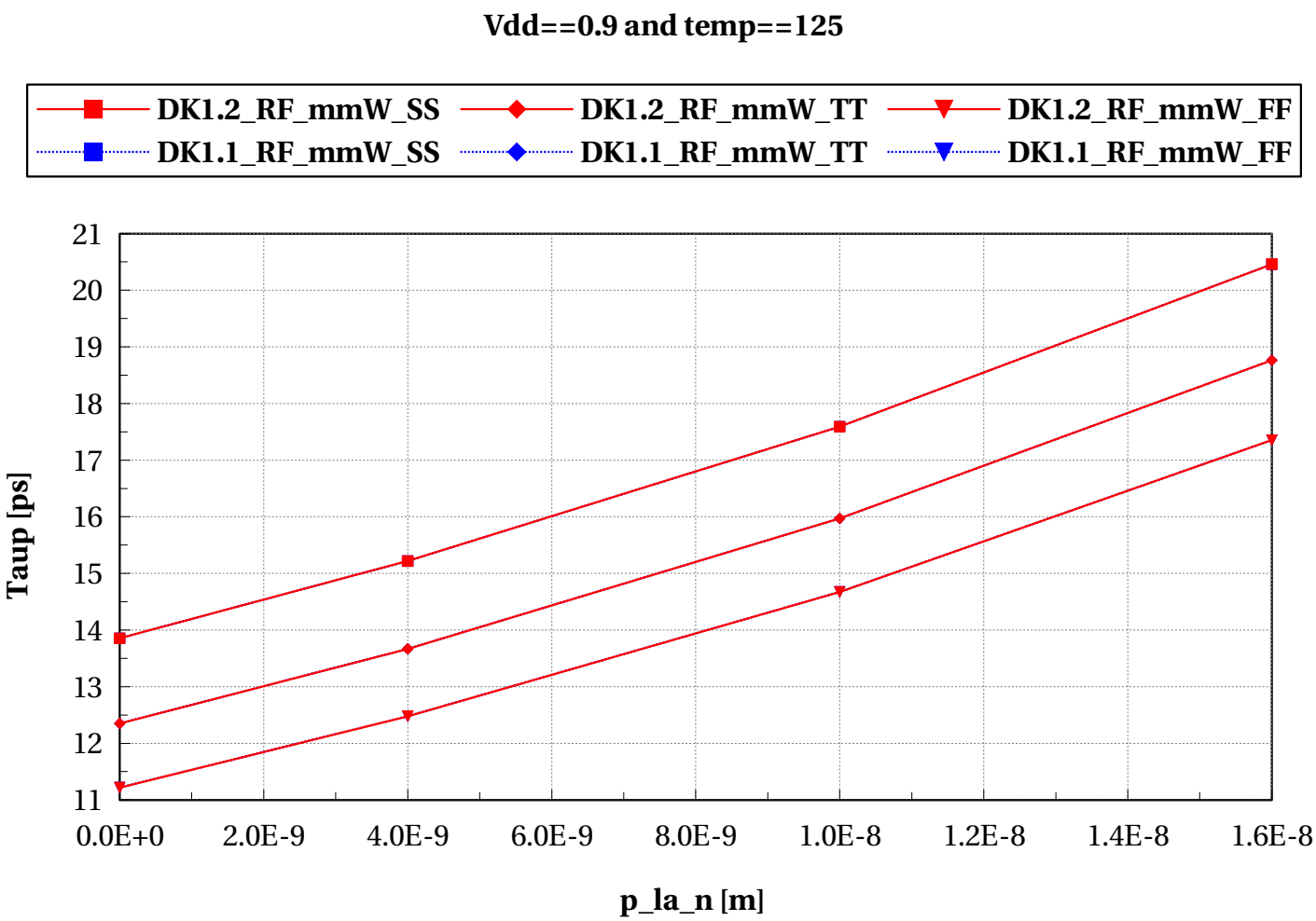
lvtnfet_acc_lvtpfet_acc, Fosc_gate [GHz] vs p_la_n [m]



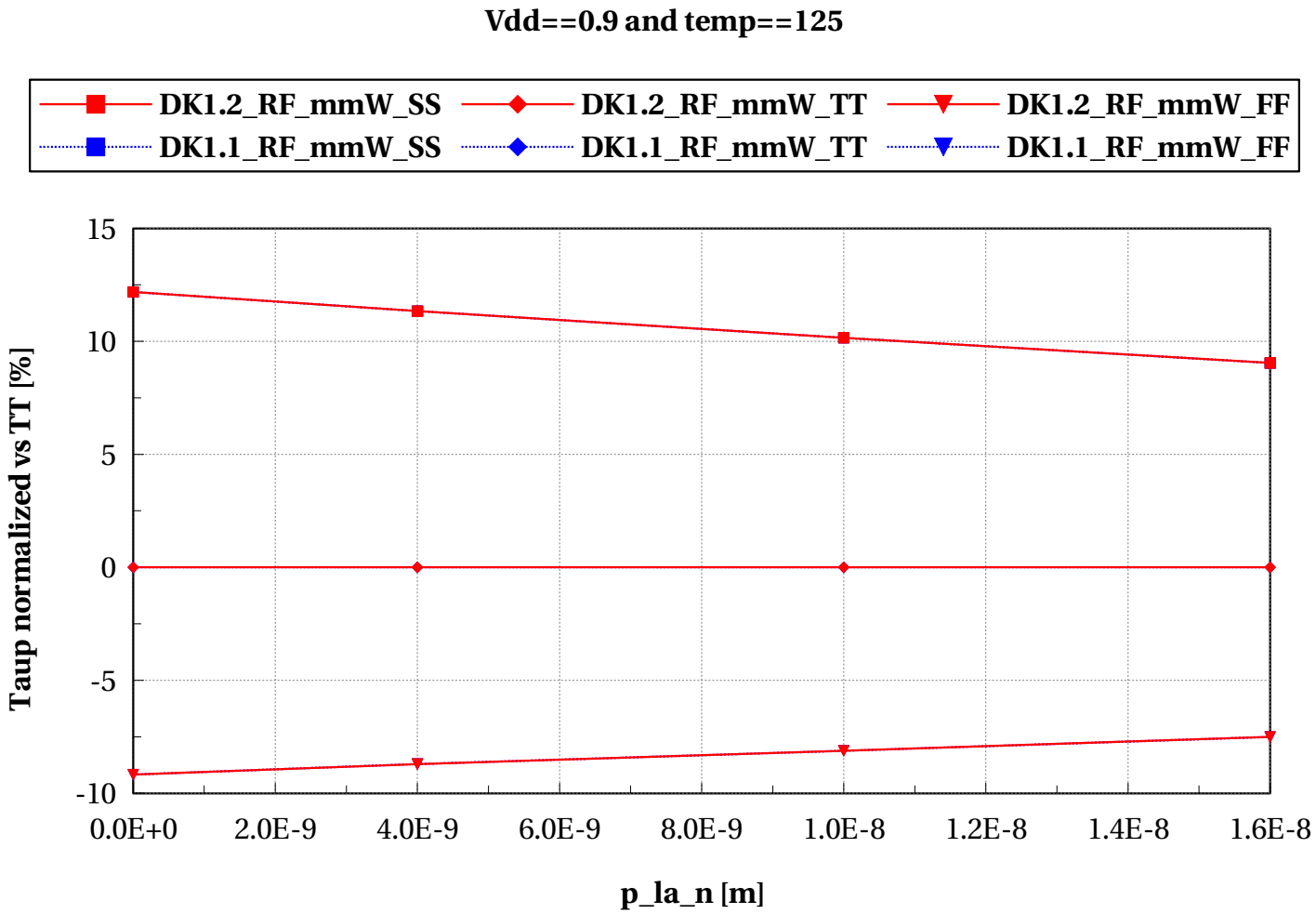
lvtnfet_acc_lvtpfet_acc, Fosc_gate normalized vs TT [%] vs p_la_n [m]



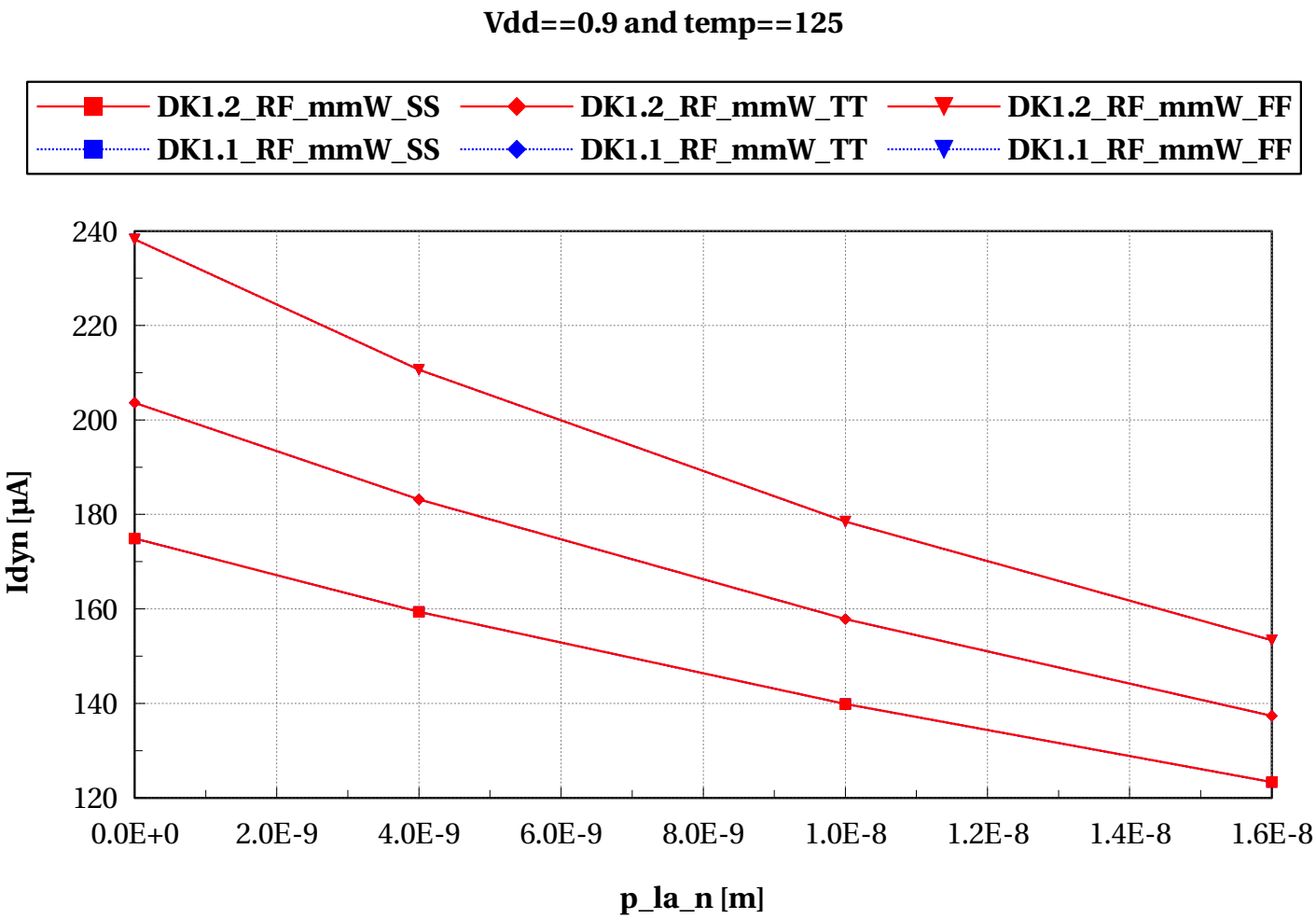
lvtnfet_acc_lvtpfet_acc, Taup [ps] vs p_la_n [m]



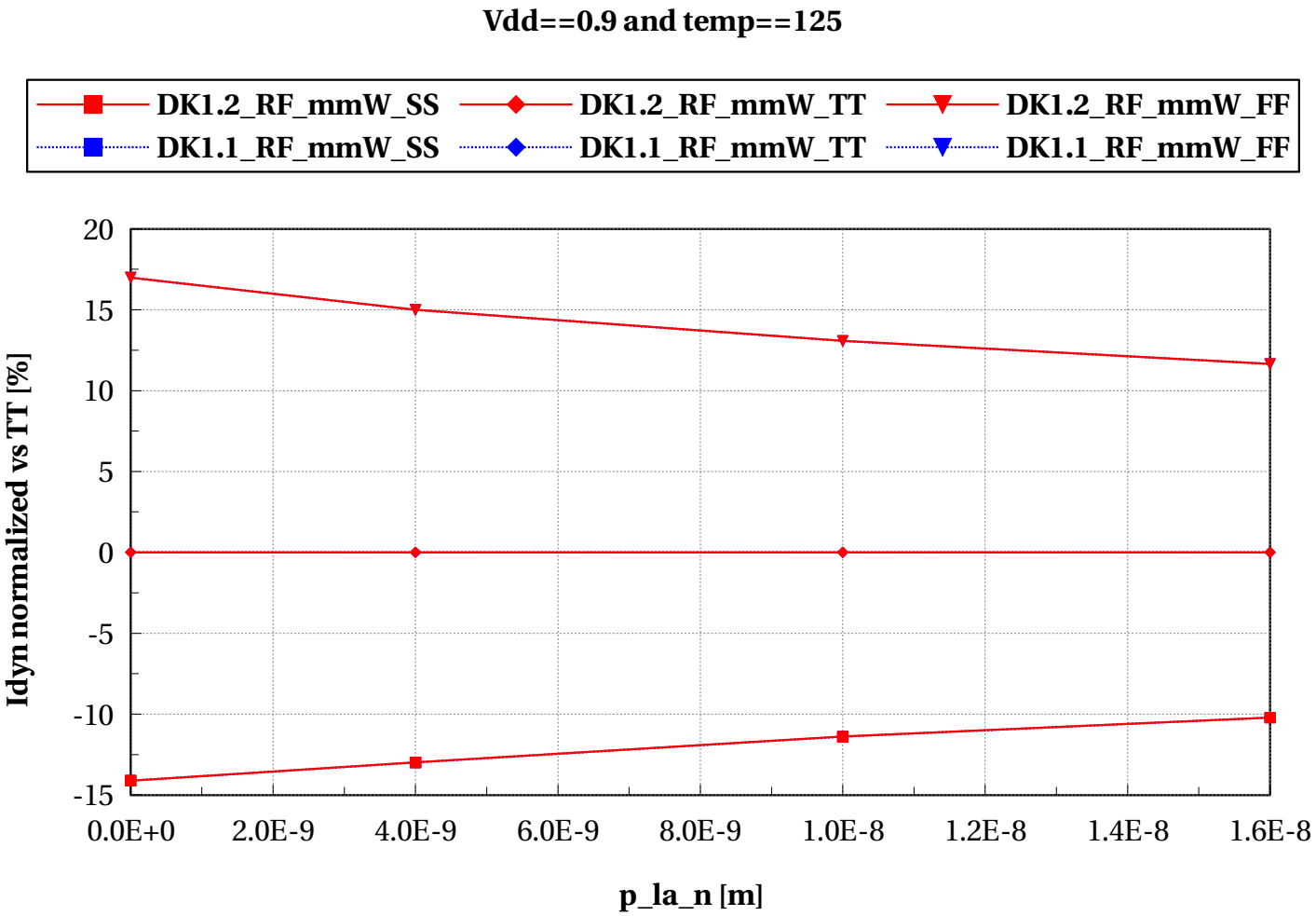
lvtnfet_acc_lvtpfet_acc, Taup normalized vs TT [%] vs p_la_n [m]



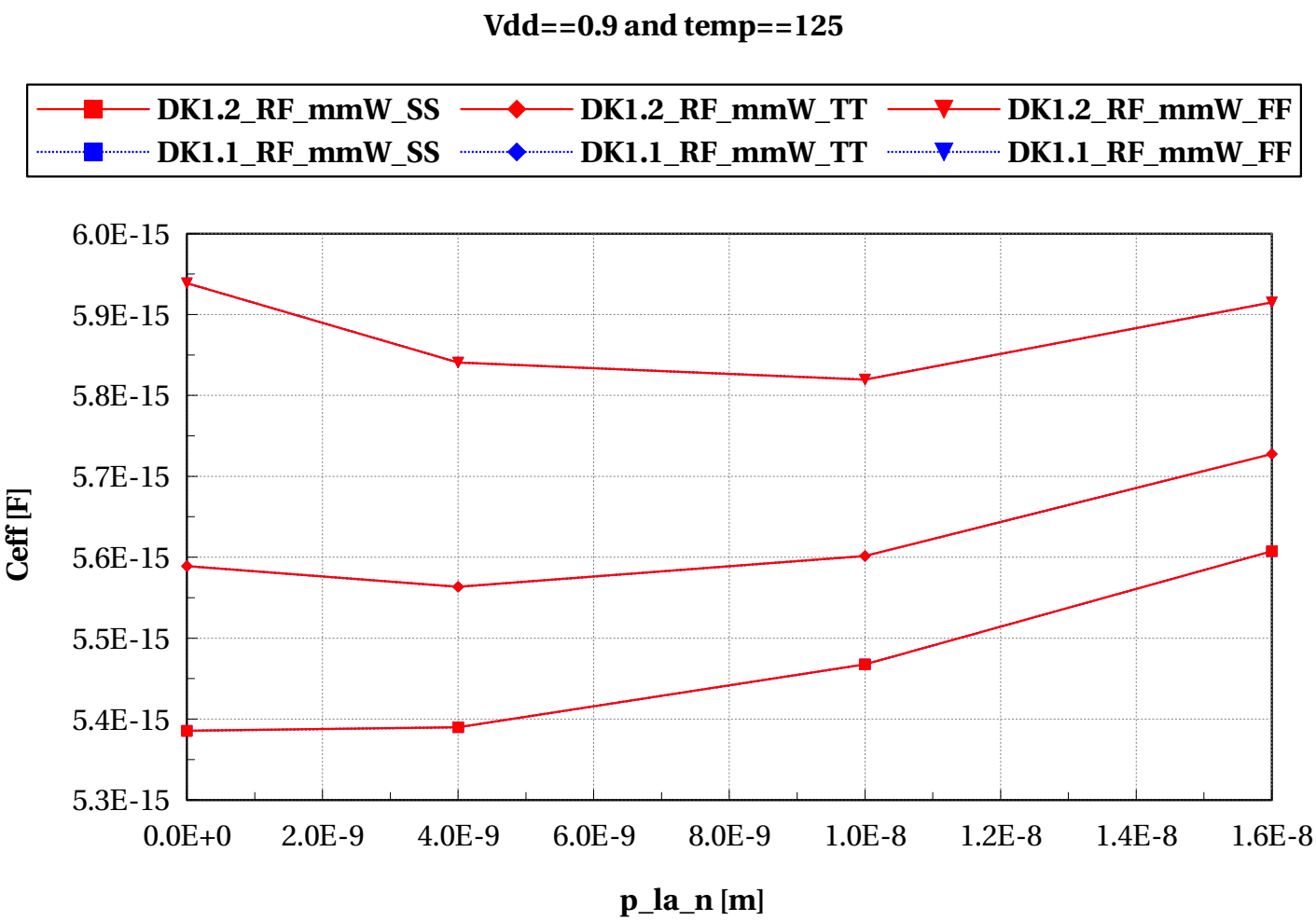
lvtnfet_acc_lvtpfet_acc, Idyn [µA] vs p_la_n [m]



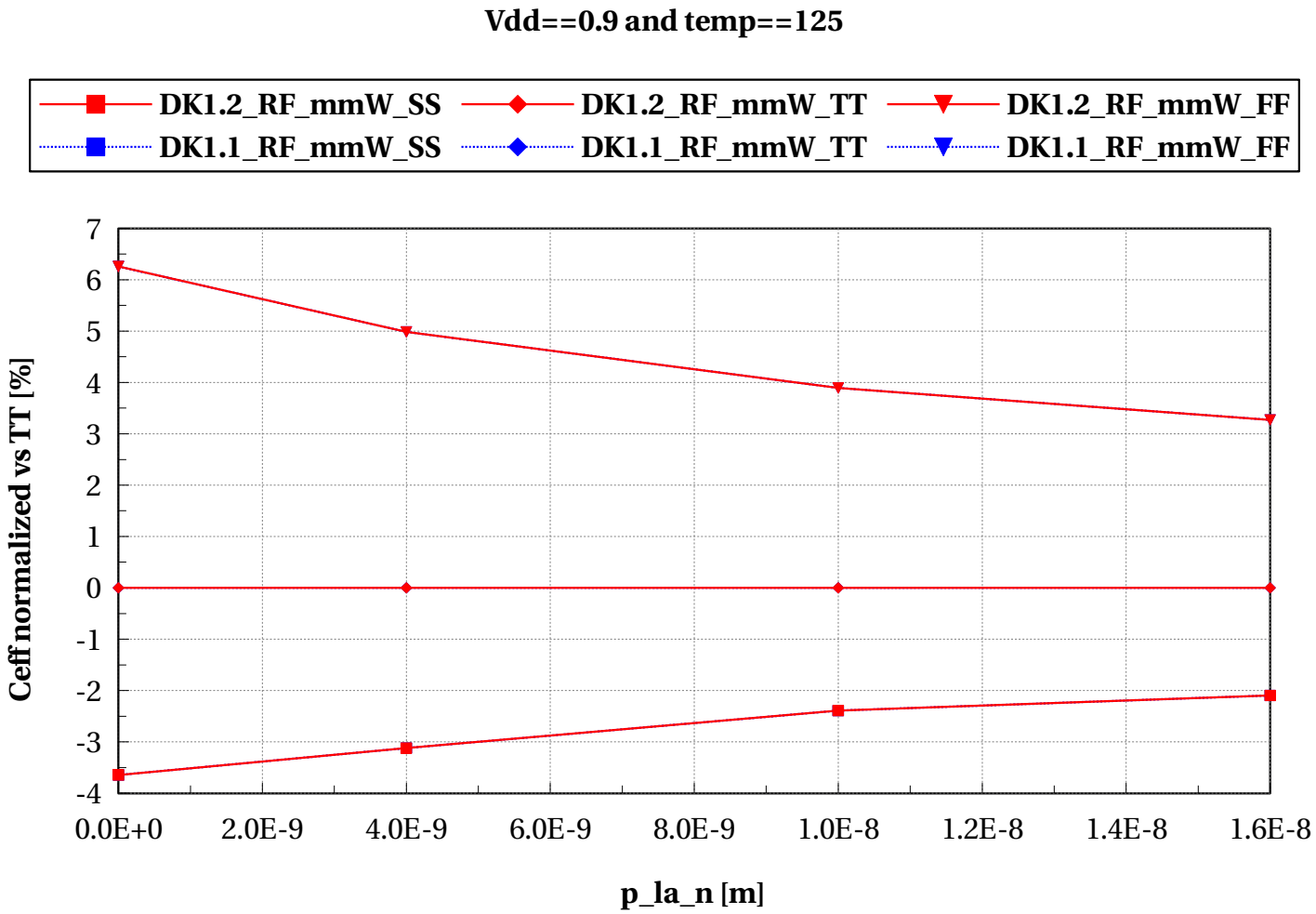
lvtnfet_acc_lvtpfet_acc, Idyn normalized vs TT [%] vs p_la_n [m]



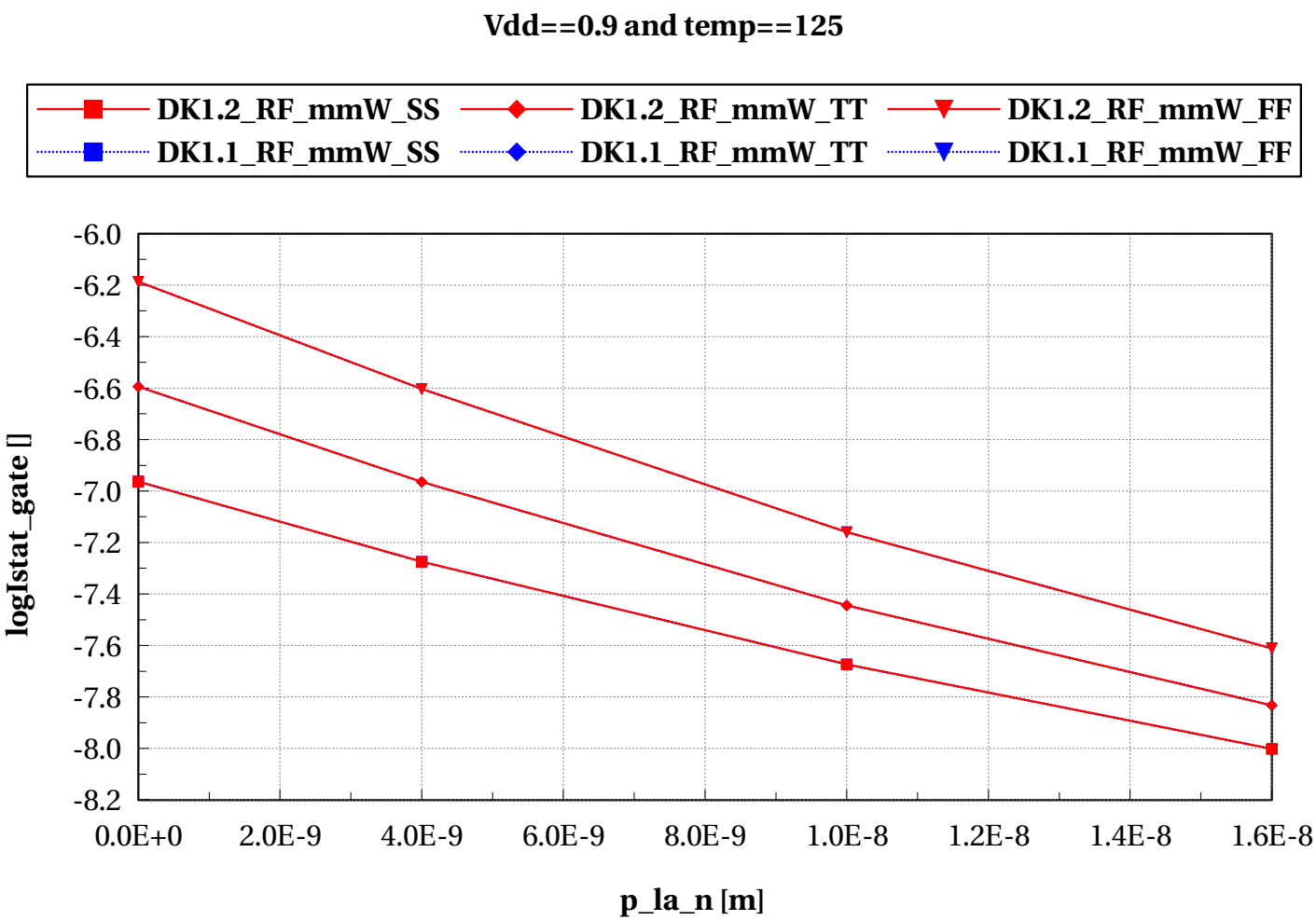
lvtnfet_acc_lvtpfet_acc, Ceff [F] vs p_la_n [m]



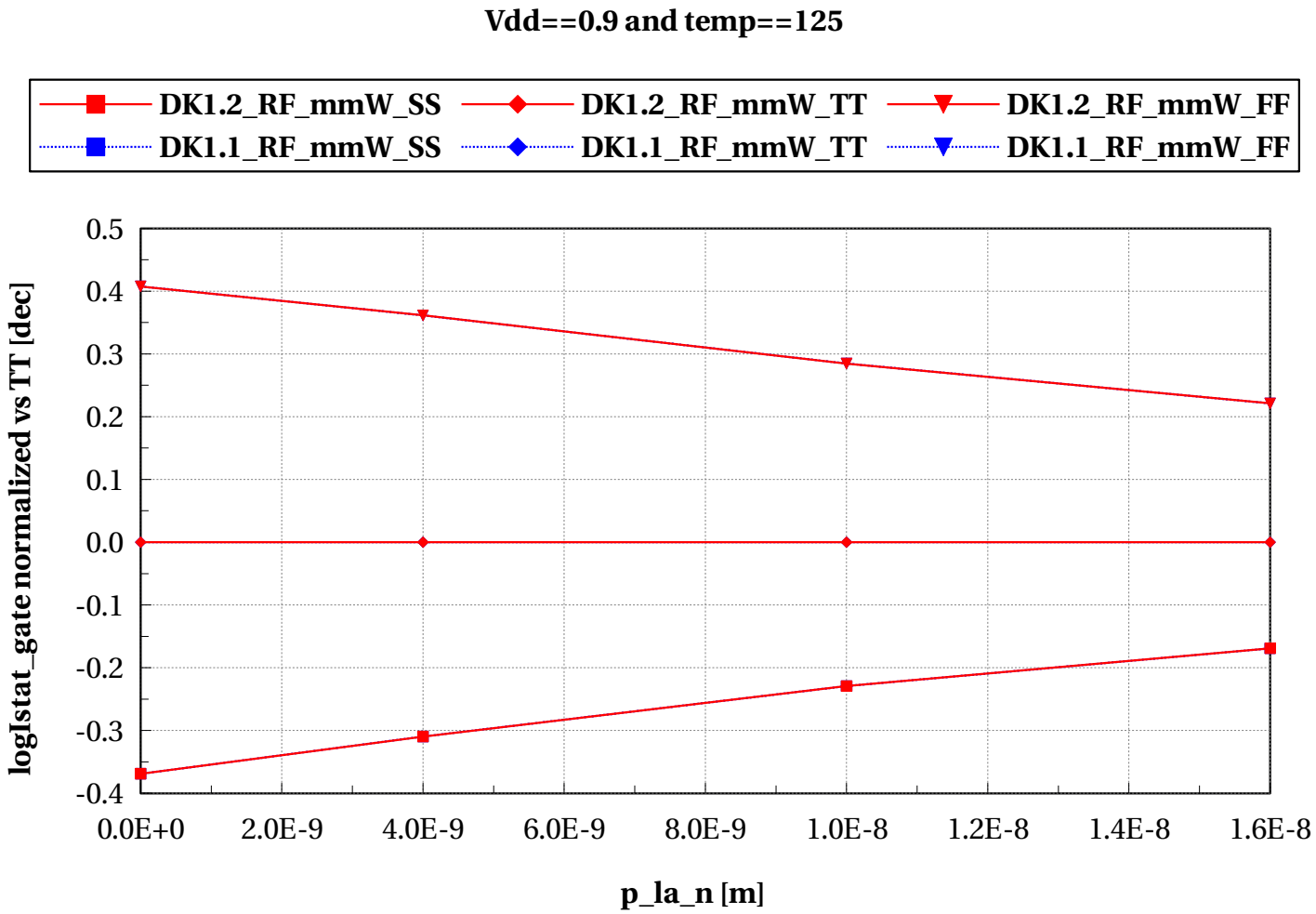
lvtnfet_acc_lvtpfet_acc, Ceff normalized vs TT [%] vs p_la_n [m]



lvtnfet_acc_lvtpfet_acc, logIstat_gate [] vs p_la_n [m]



lvtnfet_acc_lvtpfet_acc, logIstat_gate normalized vs TT [dec] vs p_la_n [m]



Annex

Conditions of simulations

The simulations were done with SBenchLSF Alpha using Eldo simulator 2018.3.

- Model lvtnfet_acc_lvtpfet_acc (DK1.2_RF_mmW)
  - ✔ Input Parameters
    - ✘ mc_runs = 1000
    - ✘ temp = 25 °C
    - ✘ rload = 0
    - ✘ vwellnfet = 0 V
    - ✘ mc_sens = 2
    - ✘ cmiller = 0 F
    - ✘ cload = 0 F
    - ✘ sbenchlsf_release = Alpha
    - ✘ ams_release = 2018.3
    - ✘ fanout = 3
    - ✘ vdd = 1 V
    - ✘ nstage = 5
    - ✘ vwellpfet = 0 V
    - ✘ mc_nsigma = 3

- ✔ Sweep Parameters
  - ✘ vdd = 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3
  - ✘ temp = -40.0, 25.0, 125.0
- ✔ Extra parameters
  - ✘ lvt_dev = 0
  - ✘ GFLAG__NOISEDEV__RVT__CMOS028FDSOI = 0
  - ✘ GFLAG__NOISEDEV__LVT__CMOS028FDSOI = 0
  - ✘ rvt_dev = 0

● Model lvtnfet_acc_lvtpfet_acc (DK1.1_RF_mmW)

- ✔ Input Parameters
  - ✘ mc_runs = 1000
  - ✘ temp = 25 °C
  - ✘ rload = 0
  - ✘ vwellnfet = 0 V
  - ✘ mc_sens = 2
  - ✘ cmiller = 0 F
  - ✘ cload = 0 F
  - ✘ sbenchlsf_release = Alpha
  - ✘ ams_release = 2018.3
  - ✘ fanout = 3
  - ✘ vdd = 1 V
  - ✘ nstage = 5
  - ✘ vwellpfet = 0 V
  - ✘ mc_nsigma = 3
- ✔ Sweep Parameters

- ✘ vdd = 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3
- ✘ temp = -40.0, 25.0, 125.0

✔ Extra parameters

- ✘ lvt_dev = 0
- ✘ GFLAG__NOISEDEV__RVT__CMOS028FDSOI = 0
- ✘ GFLAG__NOISEDEV__LVT__CMOS028FDSOI = 0
- ✘ rvt_dev = 0