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C28SOI_SC_8_COREPBP10_LL
Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 10 nm

Overview

- C28SOI_SC_8_COREPBP10_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

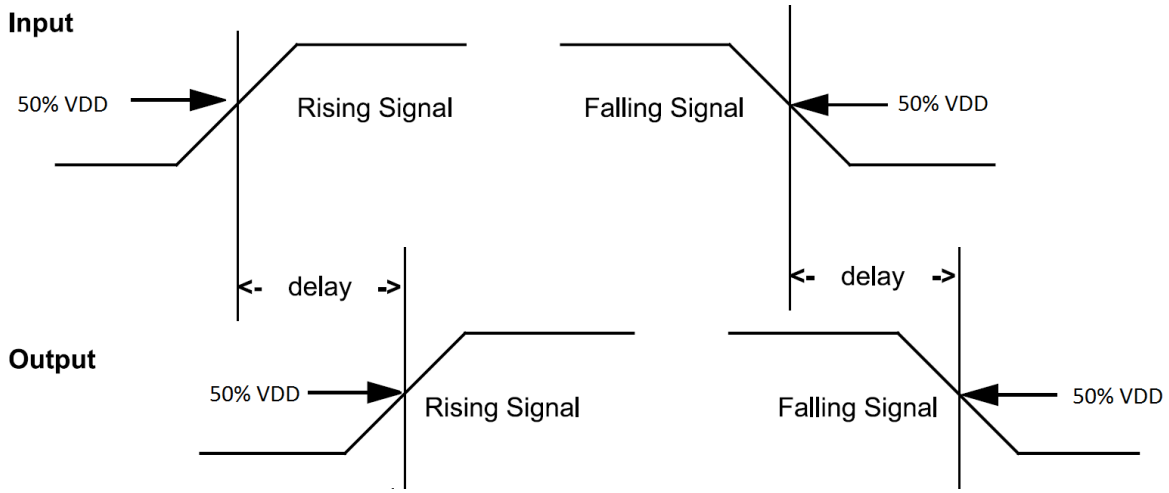


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

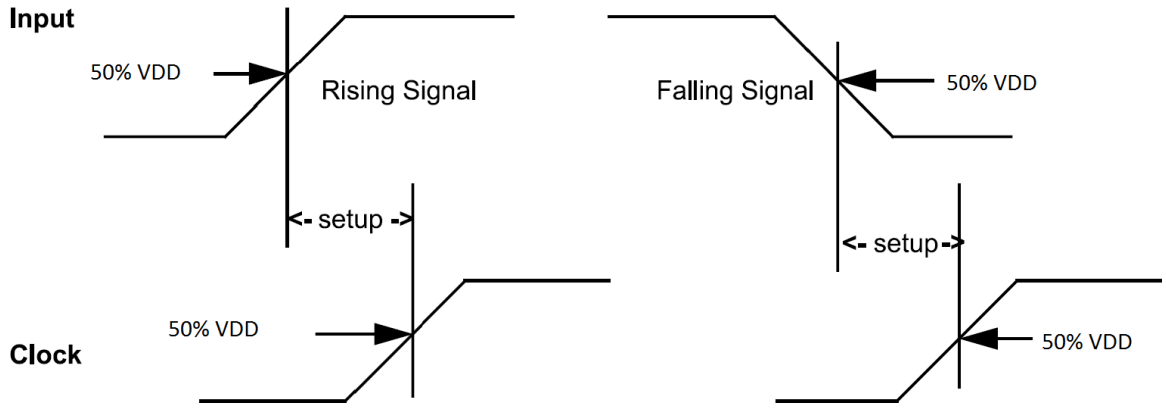


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

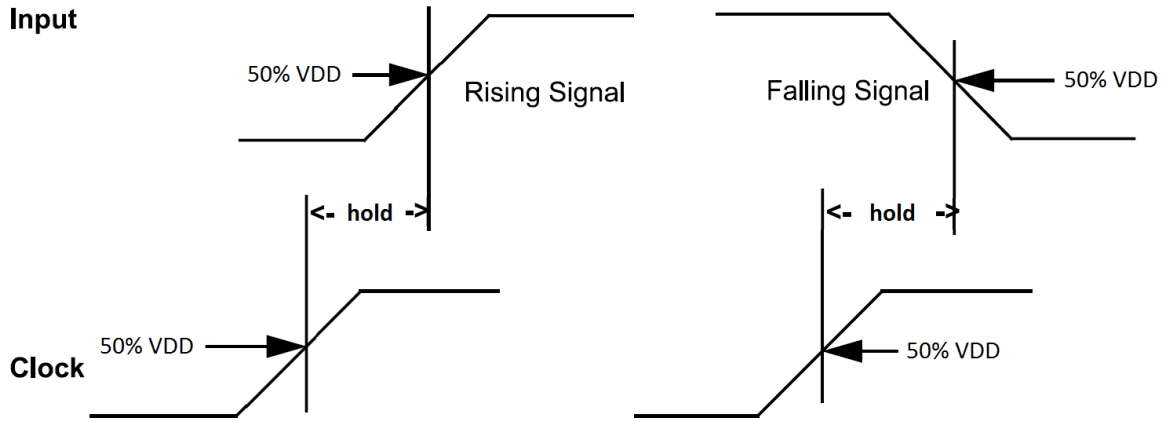


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

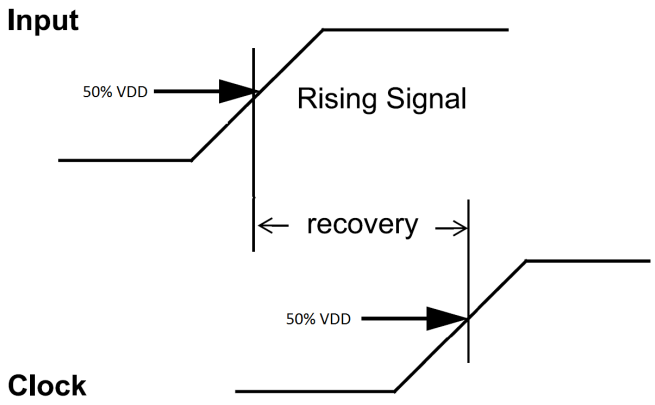


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

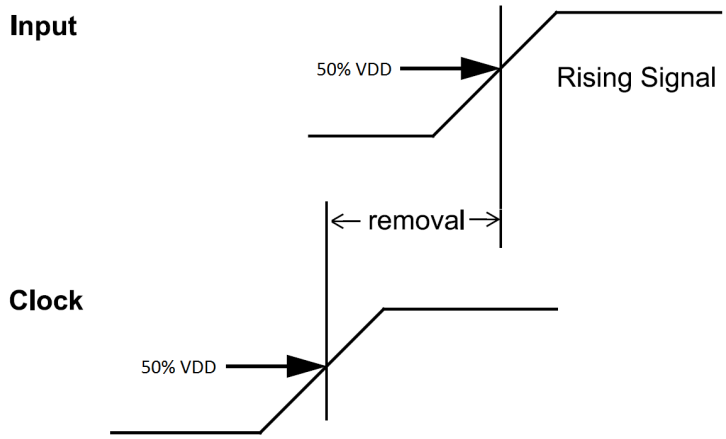


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

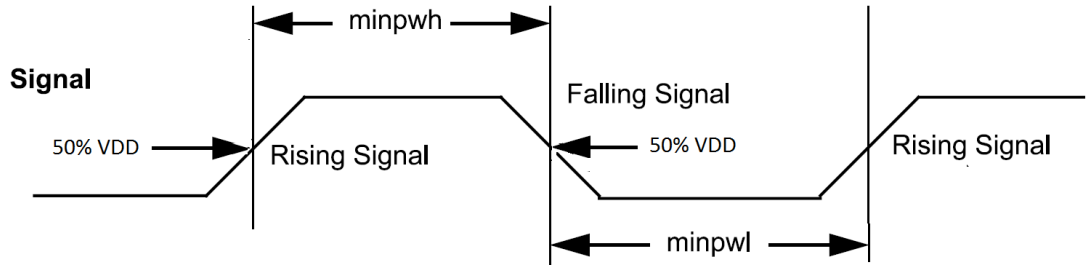


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

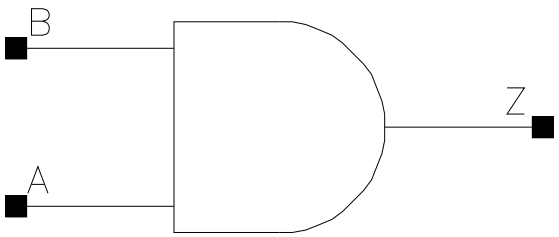
The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description	Logical Symbol
2 input AND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.544	0.4352
X10_P10	0.800	0.680	0.5440
X11_P10	1.600	0.544	0.8704
X19_P10	0.800	1.224	0.9792
X24_P10	0.800	1.360	1.0880
X29_P10	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X11_P10	X19_P10
A	0.0005	0.0007	0.0009	0.0014
B	0.0005	0.0007	0.0009	0.0013
	X24_P10	X29_P10		
A	0.0014	0.0014		
B	0.0013	0.0013		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0319	0.0261	3.2510	1.5550
A to Z ↑	0.0250	0.0233	4.9136	2.3532
B to Z ↓	0.0305	0.0245	3.2517	1.5551
B to Z ↑	0.0267	0.0247	4.9090	2.3502
	X11_P10	**X19_P10**	**X11_P10**	**X19_P10**

A to Z ↓	0.0280	0.0256	1.2280	0.8024
A to Z ↑	0.0216	0.0228	2.2576	1.1848
B to Z ↓	0.0261	0.0245	1.2274	0.8020
B to Z ↑	0.0230	0.0244	2.2571	1.1842
	X24_P10	**X29_P10**	**X24_P10**	**X29_P10**
A to Z ↓	0.0276	0.0292	0.6530	0.5439
A to Z ↑	0.0249	0.0265	0.9509	0.7900
B to Z ↓	0.0266	0.0284	0.6532	0.5448
B to Z ↑	0.0266	0.0284	0.9510	0.7904

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	2.327e-07	1.000e-20
X10_P10	5.242e-07	1.000e-20
X11_P10	6.087e-07	1.000e-20
X19_P10	1.001e-06	1.000e-20
X24_P10	1.159e-06	1.000e-20
X29_P10	1.318e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X11_P10	X19_P10
A (output stable)	7.586e-06	1.472e-05	1.969e-05	2.765e-05
B (output stable)	2.653e-05	4.916e-05	7.180e-05	1.036e-04
A to Z	1.545e-03	2.555e-03	3.076e-03	5.011e-03
B to Z	1.460e-03	2.413e-03	2.854e-03	4.706e-03
	X24_P10	X29_P10		
A (output stable)	2.777e-05	2.786e-05		
B (output stable)	1.040e-04	1.036e-04		
A to Z	6.068e-03	6.932e-03		
B to Z	5.767e-03	6.647e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

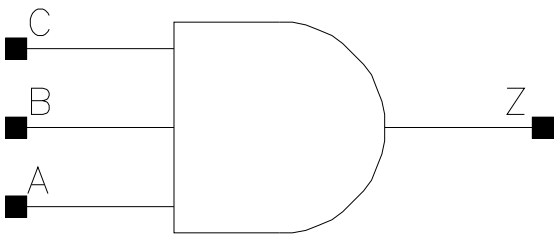
Pin Cycle (vdds)	X5_P10	X10_P10	X11_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P10	X29_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.680	0.5440
X10_P10	0.800	0.816	0.6528
X14_P10	0.800	1.360	1.0880
X19_P10	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0005	0.0008	0.0012	0.0015
B	0.0005	0.0007	0.0010	0.0014
C	0.0005	0.0007	0.0010	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0359	0.0291	3.2894	1.5654
A to Z ↑	0.0334	0.0305	4.9727	2.3815
B to Z ↓	0.0349	0.0278	3.2937	1.5639
B to Z ↑	0.0346	0.0313	4.9763	2.3828
C to Z ↓	0.0335	0.0264	3.2893	1.5638
C to Z ↑	0.0358	0.0320	4.9765	2.3817
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0293	0.0278	1.0844	0.8041

A to Z ↑	0.0292	0.0286	1.6192	1.1953
B to Z ↓	0.0279	0.0265	1.0830	0.8029
B to Z ↑	0.0301	0.0295	1.6211	1.1977
C to Z ↓	0.0266	0.0250	1.0834	0.8036
C to Z ↑	0.0311	0.0302	1.6212	1.1963

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	2.288e-07	1.000e-20
X10_P10	5.156e-07	1.000e-20
X14_P10	7.234e-07	1.000e-20
X19_P10	9.991e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	6.120e-06	1.187e-05	1.419e-05	1.972e-05
B (output stable)	2.487e-05	4.757e-05	6.733e-05	9.417e-05
C (output stable)	3.032e-05	5.620e-05	8.073e-05	1.148e-04
A to Z	1.801e-03	2.979e-03	4.320e-03	5.632e-03
B to Z	1.716e-03	2.826e-03	4.081e-03	5.311e-03
C to Z	1.642e-03	2.678e-03	3.864e-03	4.997e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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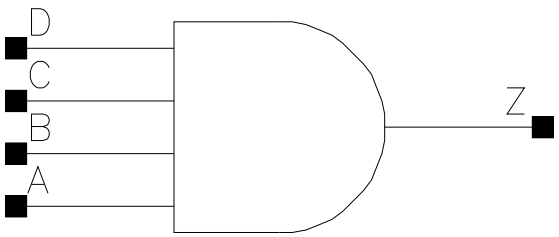
AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.088	0.8704
X3_P10	0.800	1.088	0.8704
X10_P10	0.800	2.176	1.7408
X13_P10	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P10	X3_P10	X10_P10	X13_P10
A	0.0005	0.0005	0.0011	0.0013
B	0.0005	0.0005	0.0011	0.0013
C	0.0005	0.0004	0.0011	0.0013
D	0.0005	0.0005	0.0011	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	X3_P10	X2_P10	X3_P10
A to Z ↓	0.0284	0.0303	5.9304	3.9476
A to Z ↑	0.0289	0.0289	17.9058	9.4402
B to Z ↓	0.0266	0.0292	5.9304	3.9484
B to Z ↑	0.0303	0.0305	17.9168	9.4460
C to Z ↓	0.0289	0.0310	5.9351	3.9570
C to Z ↑	0.0283	0.0281	17.9532	9.4596

D to Z ↓	0.0275	0.0303	5.9329	3.9564
D to Z ↑	0.0301	0.0308	17.9515	9.4641
	X10_P10	**X13_P10**	**X10_P10**	**X13_P10**
A to Z ↓	0.0289	0.0285	1.3635	1.0135
A to Z ↑	0.0282	0.0301	3.1382	2.4082
B to Z ↓	0.0277	0.0262	1.3635	1.0125
B to Z ↑	0.0297	0.0305	3.1387	2.4086
C to Z ↓	0.0287	0.0273	1.3548	1.0179
C to Z ↑	0.0265	0.0259	3.1389	2.4078
D to Z ↓	0.0261	0.0250	1.3529	1.0167
D to Z ↑	0.0267	0.0263	3.1400	2.4075

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P10	2.065e-07	1.000e-20
X3_P10	2.727e-07	1.000e-20
X10_P10	8.282e-07	1.000e-20
X13_P10	1.146e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P10	X3_P10	X10_P10	X13_P10
A (output stable)	3.402e-04	4.102e-04	1.087e-03	1.452e-03
B (output stable)	3.153e-04	3.838e-04	1.016e-03	1.326e-03
C (output stable)	3.426e-04	3.833e-04	1.026e-03	1.293e-03
D (output stable)	3.161e-04	3.662e-04	9.301e-04	1.159e-03
A to Z	1.269e-03	1.684e-03	4.829e-03	6.409e-03
B to Z	1.188e-03	1.597e-03	4.592e-03	5.927e-03
C to Z	1.272e-03	1.616e-03	4.126e-03	5.128e-03
D to Z	1.193e-03	1.559e-03	3.708e-03	4.654e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

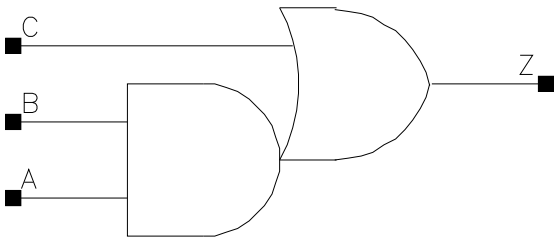
Pin Cycle (vdds)	X2_P10	X3_P10	X10_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	0.952	0.7616
X19_P10	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0004	0.0006	0.0013
B	0.0004	0.0007	0.0011
C	0.0005	0.0007	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0431	0.0379	3.1350	1.5688
A to Z ↑	0.0278	0.0253	4.5633	2.3217
B to Z ↓	0.0405	0.0355	3.1272	1.5643
B to Z ↑	0.0300	0.0274	4.5629	2.3215
C to Z ↓	0.0438	0.0370	3.1186	1.5598
C to Z ↑	0.0262	0.0239	4.5260	2.3049
	X19_P10		**X19_P10**	
A to Z ↓	0.0366		0.8200	
A to Z ↑	0.0276		1.1724	

B to Z ↓	0.0352		0.8204	
B to Z ↑	0.0297		1.1730	
C to Z ↓	0.0363		0.8173	
C to Z ↑	0.0255		1.1609	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	2.677e-07	1.000e-20
X10_P10	5.367e-07	1.000e-20
X19_P10	9.551e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	3.995e-06	1.038e-05	1.962e-05
B (output stable)	1.279e-05	2.481e-05	4.777e-05
C (output stable)	4.464e-05	5.838e-05	1.372e-04
A to Z	1.746e-03	2.849e-03	5.461e-03
B to Z	1.666e-03	2.707e-03	5.245e-03
C to Z	1.961e-03	3.113e-03	6.012e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

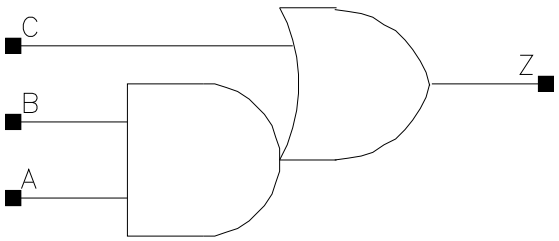
Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	0.952	0.7616
X14_P10	0.800	1.632	1.3056
X19_P10	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0004	0.0006	0.0013	0.0013
B	0.0005	0.0006	0.0013	0.0013
C	0.0005	0.0007	0.0014	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0452	0.0395	3.1206	1.5810
A to Z ↑	0.0301	0.0280	4.6570	2.3415
B to Z ↓	0.0433	0.0376	3.1150	1.5797
B to Z ↑	0.0329	0.0300	4.6545	2.3439
C to Z ↓	0.0391	0.0351	3.1017	1.5737
C to Z ↑	0.0231	0.0210	4.5986	2.3191
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0359	0.0385	1.0812	0.8120

A to Z ↑	0.0260	0.0275	1.5941	1.1889
B to Z ↓	0.0328	0.0355	1.0787	0.8102
B to Z ↑	0.0270	0.0287	1.5959	1.1883
C to Z ↓	0.0297	0.0324	1.0756	0.8077
C to Z ↑	0.0186	0.0199	1.5777	1.1739

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	2.699e-07	1.000e-20
X10_P10	5.091e-07	1.000e-20
X14_P10	9.288e-07	1.000e-20
X19_P10	1.055e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.324e-05	1.671e-05	5.254e-05	5.272e-05
B (output stable)	5.840e-05	4.750e-05	1.946e-04	1.934e-04
C (output stable)	3.886e-05	5.397e-05	1.175e-04	1.177e-04
A to Z	1.967e-03	3.023e-03	5.433e-03	6.328e-03
B to Z	1.895e-03	2.882e-03	4.961e-03	5.866e-03
C to Z	1.627e-03	2.545e-03	4.183e-03	5.053e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

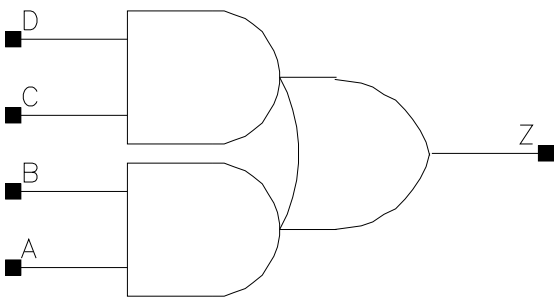
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.088	0.8704
X10_P10	0.800	1.088	0.8704
X14_P10	0.800	1.768	1.4144
X19_P10	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0005	0.0007	0.0013	0.0013
B	0.0005	0.0009	0.0012	0.0012
C	0.0005	0.0007	0.0014	0.0014
D	0.0005	0.0007	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0460	0.0393	3.1322	1.5785
A to Z ↑	0.0319	0.0297	4.6929	2.3265
B to Z ↓	0.0424	0.0362	3.1214	1.5735

B to Z ↑	0.0328	0.0309	4.6934	2.3261
C to Z ↓	0.0413	0.0359	3.1216	1.5733
C to Z ↑	0.0270	0.0248	4.6843	2.3197
D to Z ↓	0.0394	0.0340	3.1175	1.5701
D to Z ↑	0.0293	0.0268	4.6834	2.3215
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0355	0.0382	1.0812	0.8162
A to Z ↑	0.0262	0.0280	1.6002	1.1969
B to Z ↓	0.0333	0.0361	1.0801	0.8159
B to Z ↑	0.0280	0.0300	1.5994	1.1964
C to Z ↓	0.0324	0.0353	1.0784	0.8145
C to Z ↑	0.0226	0.0245	1.5939	1.1931
D to Z ↓	0.0304	0.0334	1.0782	0.8140
D to Z ↑	0.0240	0.0261	1.5946	1.1936

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	3.160e-07	1.000e-20
X10_P10	6.235e-07	1.000e-20
X14_P10	1.037e-06	1.000e-20
X19_P10	1.180e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	2.424e-05	3.116e-05	4.494e-05	4.504e-05
B (output stable)	6.219e-05	8.027e-05	8.233e-05	8.257e-05
C (output stable)	1.381e-05	1.692e-05	3.221e-05	3.228e-05
D (output stable)	2.315e-05	3.956e-05	7.678e-05	7.731e-05
A to Z	2.269e-03	3.480e-03	5.632e-03	6.667e-03
B to Z	2.052e-03	3.154e-03	5.280e-03	6.317e-03
C to Z	1.882e-03	2.906e-03	4.607e-03	5.630e-03
D to Z	1.793e-03	2.760e-03	4.294e-03	5.320e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

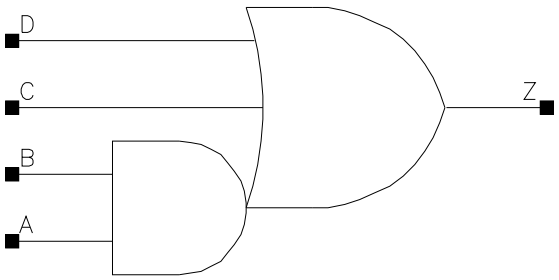
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	1.088	0.8704
X19_P10	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0004	0.0006	0.0012
B	0.0004	0.0007	0.0012
C	0.0005	0.0006	0.0013
D	0.0004	0.0006	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0533	0.0454	3.4906	1.6431
A to Z ↑	0.0289	0.0249	4.8709	2.3375
B to Z ↓	0.0511	0.0423	3.4850	1.6381
B to Z ↑	0.0312	0.0268	4.8725	2.3383
C to Z ↓	0.0562	0.0479	3.4771	1.6378
C to Z ↑	0.0268	0.0326	4.8320	2.3387

D to Z ↓	0.0560	0.0484	3.4774	1.6386
D to Z ↑	0.0266	0.0321	4.8320	2.3380
	X19_P10		**X19_P10**	
A to Z ↓	0.0450		0.8531	
A to Z ↑	0.0273		1.1625	
B to Z ↓	0.0410		0.8498	
B to Z ↑	0.0283		1.1615	
C to Z ↓	0.0463		0.8492	
C to Z ↑	0.0272		1.1539	
D to Z ↓	0.0459		0.8499	
D to Z ↑	0.0269		1.1534	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	2.258e-07	1.000e-20
X10_P10	4.768e-07	1.000e-20
X19_P10	8.782e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	3.172e-06	6.023e-06	2.172e-05
B (output stable)	7.827e-06	1.284e-05	5.117e-05
C (output stable)	6.944e-05	1.199e-04	2.089e-04
D (output stable)	7.488e-06	1.519e-05	2.334e-05
A to Z	1.833e-03	2.983e-03	5.830e-03
B to Z	1.759e-03	2.829e-03	5.368e-03
C to Z	2.111e-03	3.539e-03	6.728e-03
D to Z	1.998e-03	3.346e-03	6.292e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

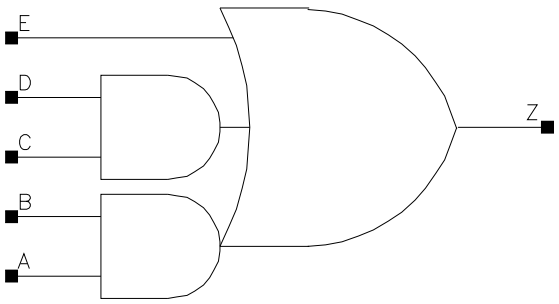
Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.088	0.8704
X10_P10	0.800	1.224	0.9792
X19_P10	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0004	0.0007	0.0013
B	0.0005	0.0007	0.0011
C	0.0004	0.0008	0.0013
D	0.0005	0.0006	0.0011
E	0.0004	0.0006	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0670	0.0533	3.3006	1.6332
A to Z ↑	0.0363	0.0309	4.7421	2.3504

B to Z ↓	0.0659	0.0510	3.2951	1.6321
B to Z ↑	0.0396	0.0331	4.7390	2.3478
C to Z ↓	0.0590	0.0472	3.2901	1.6296
C to Z ↑	0.0319	0.0264	4.7070	2.3361
D to Z ↓	0.0555	0.0430	3.2781	1.6233
D to Z ↑	0.0344	0.0280	4.7121	2.3352
E to Z ↓	0.0596	0.0472	3.2721	1.6231
E to Z ↑	0.0285	0.0244	4.6592	2.3171
	X19_P10		**X19_P10**	
A to Z ↓	0.0514		0.8438	
A to Z ↑	0.0318		1.1787	
B to Z ↓	0.0491		0.8431	
B to Z ↑	0.0343		1.1787	
C to Z ↓	0.0444		0.8408	
C to Z ↑	0.0266		1.1706	
D to Z ↓	0.0418		0.8394	
D to Z ↑	0.0286		1.1702	
E to Z ↓	0.0455		0.8387	
E to Z ↑	0.0298		1.1659	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	2.837e-07	1.000e-20
X10_P10	5.907e-07	1.000e-20
X19_P10	1.048e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	1.375e-05	2.449e-05	5.044e-05
B (output stable)	3.070e-05	3.514e-05	6.826e-05
C (output stable)	1.002e-05	1.393e-05	2.755e-05
D (output stable)	1.220e-05	2.410e-05	4.324e-05
E (output stable)	5.774e-05	5.648e-05	1.197e-04
A to Z	2.543e-03	3.921e-03	7.458e-03
B to Z	2.489e-03	3.758e-03	7.143e-03
C to Z	2.081e-03	3.128e-03	5.841e-03
D to Z	1.993e-03	2.947e-03	5.561e-03
E to Z	2.210e-03	3.381e-03	6.401e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

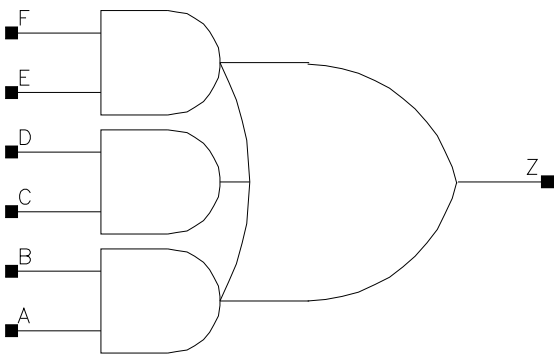
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.360	1.0880
X5_P10	0.800	1.360	1.0880
X10_P10	0.800	1.632	1.3056
X19_P10	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P10	X5_P10	X10_P10	X19_P10
A	0.0005	0.0005	0.0007	0.0012

B	0.0005	0.0005	0.0008	0.0011
C	0.0007	0.0007	0.0006	0.0012
D	0.0005	0.0005	0.0006	0.0011
E	0.0007	0.0007	0.0006	0.0013
F	0.0006	0.0006	0.0006	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X5_P10**	**X2_P10**	**X5_P10**
A to Z ↓	0.0521	0.0537	6.1438	3.3631
A to Z ↑	0.0355	0.0350	9.5586	4.9623
B to Z ↓	0.0498	0.0514	6.1262	3.3556
B to Z ↑	0.0384	0.0380	9.5518	4.9609
C to Z ↓	0.0487	0.0504	6.1395	3.3612
C to Z ↑	0.0330	0.0326	9.4744	4.9282
D to Z ↓	0.0448	0.0465	6.1209	3.3524
D to Z ↑	0.0349	0.0346	9.4742	4.9240
E to Z ↓	0.0404	0.0421	6.1121	3.3477
E to Z ↑	0.0275	0.0272	9.4251	4.9049
F to Z ↓	0.0371	0.0390	6.0976	3.3408
F to Z ↑	0.0291	0.0290	9.4269	4.9042
	X10_P10	**X19_P10**	**X10_P10**	**X19_P10**
A to Z ↓	0.0572	0.0535	1.6293	0.8415
A to Z ↑	0.0376	0.0343	2.3642	1.1846
B to Z ↓	0.0541	0.0515	1.6230	0.8409
B to Z ↑	0.0393	0.0368	2.3636	1.1846
C to Z ↓	0.0527	0.0498	1.6258	0.8407
C to Z ↑	0.0334	0.0316	2.3499	1.1770
D to Z ↓	0.0508	0.0480	1.6223	0.8401
D to Z ↑	0.0360	0.0341	2.3495	1.1776
E to Z ↓	0.0463	0.0449	1.6205	0.8379
E to Z ↑	0.0288	0.0277	2.3404	1.1736
F to Z ↓	0.0435	0.0422	1.6154	0.8367
F to Z ↑	0.0308	0.0298	2.3410	1.1736

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P10	3.113e-07	1.000e-20
X5_P10	3.948e-07	1.000e-20
X10_P10	6.488e-07	1.000e-20
X19_P10	1.224e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P10	X5_P10	X10_P10	X19_P10
A (output stable)	4.991e-05	4.988e-05	5.893e-05	1.034e-04
B (output stable)	1.050e-04	1.048e-04	1.360e-04	1.870e-04
C (output stable)	2.409e-05	2.409e-05	2.926e-05	3.876e-05
D (output stable)	3.217e-05	3.218e-05	4.490e-05	6.758e-05
E (output stable)	2.074e-05	2.065e-05	2.653e-05	3.856e-05
F (output stable)	2.811e-05	2.803e-05	3.632e-05	6.039e-05

A to Z	2.577e-03	2.902e-03	4.400e-03	8.087e-03
B to Z	2.468e-03	2.791e-03	4.122e-03	7.784e-03
C to Z	2.130e-03	2.453e-03	3.822e-03	7.063e-03
D to Z	1.999e-03	2.320e-03	3.695e-03	6.809e-03
E to Z	1.629e-03	1.945e-03	3.260e-03	6.139e-03
F to Z	1.523e-03	1.840e-03	3.121e-03	5.855e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

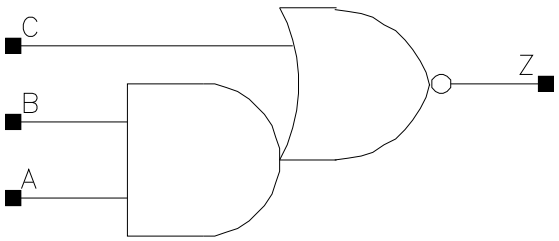
Pin Cycle (vdds)	X2_P10	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X10_P10	0.800	1.360	1.0880
X19_P10	0.800	2.584	2.0672
X25_P10	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P10	X10_P10	X19_P10	X25_P10
A	0.0006	0.0016	0.0031	0.0041
B	0.0005	0.0014	0.0028	0.0038
C	0.0006	0.0017	0.0031	0.0042

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X10_P10**	**X3_P10**	**X10_P10**
A to Z ↓	0.0099	0.0107	5.3017	1.9243
A to Z ↑	0.0181	0.0185	9.0708	3.1013
B to Z ↓	0.0103	0.0107	5.3822	1.9533
B to Z ↑	0.0150	0.0147	8.9249	3.0940
C to Z ↓	0.0107	0.0109	3.2303	1.1268
C to Z ↑	0.0186	0.0189	8.2537	2.8482
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0113	0.0112	0.9816	0.7495

A to Z ↑	0.0190	0.0187	1.5875	1.1817
B to Z ↓	0.0107	0.0107	0.9973	0.7615
B to Z ↑	0.0149	0.0149	1.5871	1.1960
C to Z ↓	0.0124	0.0125	0.6866	0.5262
C to Z ↑	0.0191	0.0190	1.4601	1.0927

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.377e-07	1.000e-20
X10_P10	6.433e-07	1.000e-20
X19_P10	1.227e-06	1.000e-20
X25_P10	1.614e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X10_P10	X19_P10	X25_P10
A (output stable)	1.195e-05	4.004e-05	8.414e-05	1.047e-04
B (output stable)	2.733e-05	1.319e-04	2.761e-04	3.511e-04
C (output stable)	6.106e-05	1.997e-04	3.845e-04	5.287e-04
A to Z	7.249e-04	2.282e-03	4.750e-03	6.171e-03
B to Z	5.811e-04	1.664e-03	3.399e-03	4.484e-03
C to Z	1.042e-03	3.115e-03	6.148e-03	8.208e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P10	X10_P10	X19_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

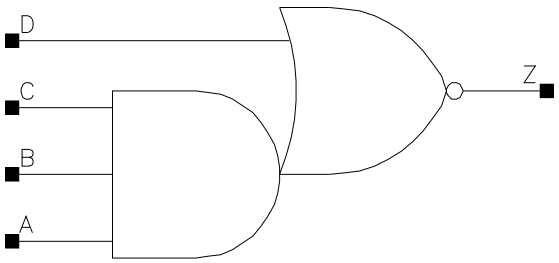
life.augmented

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X17_P10	0.800	3.536	2.8288
X22_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X17_P10	X22_P10
A	0.0005	0.0031	0.0042
B	0.0005	0.0029	0.0039
C	0.0006	0.0028	0.0037
D	0.0006	0.0032	0.0042

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X17_P10	X3_P10	X17_P10
A to Z ↓	0.0147	0.0159	7.4561	1.4286
A to Z ↑	0.0235	0.0228	9.0809	1.5278
B to Z ↓	0.0152	0.0158	7.4865	1.4349
B to Z ↑	0.0212	0.0204	9.0954	1.5526
C to Z ↓	0.0161	0.0147	7.5404	1.4452
C to Z ↑	0.0197	0.0167	9.1173	1.5633
D to Z ↓	0.0129	0.0145	3.1531	0.6760

D to Z ↑	0.0232	0.0218	7.7981	1.3243
	X22_P10		**X22_P10**	
A to Z ↓	0.0158		1.0858	
A to Z ↑	0.0225		1.1425	
B to Z ↓	0.0156		1.0910	
B to Z ↑	0.0200		1.1653	
C to Z ↓	0.0145		1.0995	
C to Z ↑	0.0165		1.1763	
D to Z ↓	0.0151		0.5600	
D to Z ↑	0.0212		0.9906	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.646e-07	1.000e-20
X17_P10	1.275e-06	1.000e-20
X22_P10	1.651e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X17_P10	X22_P10
A (output stable)	1.113e-05	7.824e-05	1.039e-04
B (output stable)	2.349e-05	1.730e-04	2.249e-04
C (output stable)	4.857e-05	3.956e-04	5.203e-04
D (output stable)	3.366e-04	1.852e-03	2.409e-03
A to Z	1.168e-03	6.749e-03	8.773e-03
B to Z	1.007e-03	5.513e-03	7.130e-03
C to Z	8.690e-04	4.198e-03	5.440e-03
D to Z	1.511e-03	8.153e-03	1.060e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

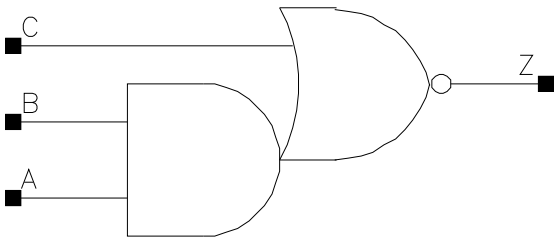
Pin Cycle (vdds)	X3_P10	X17_P10	X22_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X6_P10	0.800	1.088	0.8704
X9_P10	0.800	1.360	1.0880
X12_P10	0.800	1.904	1.5232
X25_P10	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X9_P10	X12_P10
A	0.0005	0.0012	0.0017	0.0023
B	0.0005	0.0011	0.0016	0.0022
C	0.0006	0.0010	0.0014	0.0019
	X25_P10			
A	0.0046			
B	0.0042			
C	0.0038			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0135	0.0135	6.9457	2.7992
A to Z ↑	0.0206	0.0218	10.3440	4.6002
B to Z ↓	0.0150	0.0134	7.0029	2.8337

B to Z ↑	0.0187	0.0185	10.2092	4.6147
C to Z ↓	0.0090	0.0078	4.2704	2.0367
C to Z ↑	0.0158	0.0144	9.5159	4.2673
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0129	0.0134	1.9271	1.4450
A to Z ↑	0.0205	0.0207	3.0813	2.2765
B to Z ↓	0.0133	0.0132	1.9515	1.4640
B to Z ↑	0.0172	0.0174	3.0824	2.3069
C to Z ↓	0.0078	0.0077	1.3913	1.0407
C to Z ↑	0.0137	0.0139	2.8592	2.1285
	X25_P10		**X25_P10**	
A to Z ↓	0.0132		0.7537	
A to Z ↑	0.0202		1.1559	
B to Z ↓	0.0133		0.7635	
B to Z ↑	0.0169		1.1611	
C to Z ↓	0.0076		0.5294	
C to Z ↑	0.0134		1.0769	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	1.867e-07	1.000e-20
X6_P10	4.555e-07	1.000e-20
X9_P10	6.333e-07	1.000e-20
X12_P10	8.575e-07	1.000e-20
X25_P10	1.655e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	1.725e-05	5.251e-05	6.919e-05	9.774e-05
B (output stable)	5.199e-05	1.924e-04	2.094e-04	3.239e-04
C (output stable)	4.001e-05	1.002e-04	1.362e-04	1.998e-04
A to Z	9.604e-04	2.370e-03	3.243e-03	4.488e-03
B to Z	8.440e-04	1.897e-03	2.556e-03	3.480e-03
C to Z	5.304e-04	1.149e-03	1.563e-03	2.172e-03
	X25_P10			
A (output stable)	1.892e-04			
B (output stable)	5.798e-04			
C (output stable)	3.743e-04			
A to Z	8.533e-03			
B to Z	6.674e-03			
C to Z	4.065e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

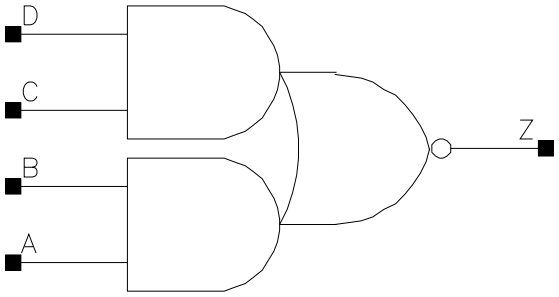
	X25_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.680	0.5440
X6_P10	0.800	1.224	0.9792
X9_P10	0.800	1.768	1.4144
X12_P10	0.800	2.448	1.9584
X24_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P10	X6_P10	X9_P10	X12_P10
A	0.0005	0.0012	0.0017	0.0023
B	0.0004	0.0010	0.0016	0.0022
C	0.0004	0.0012	0.0016	0.0021
D	0.0004	0.0010	0.0015	0.0020
	X24_P10			
A	0.0045			
B	0.0044			
C	0.0042			
D	0.0039			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X6_P10**	**X2_P10**	**X6_P10**
A to Z ↓	0.0136	0.0139	7.0682	2.6912
A to Z ↑	0.0260	0.0226	13.0117	4.2051
B to Z ↓	0.0150	0.0151	7.1503	2.7194
B to Z ↑	0.0233	0.0202	12.9834	4.2928
C to Z ↓	0.0101	0.0099	7.0908	2.7033
C to Z ↑	0.0203	0.0179	12.9990	4.1973
D to Z ↓	0.0107	0.0104	7.1997	2.7428
D to Z ↑	0.0175	0.0155	12.9630	4.3230
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0150	0.0155	1.9305	1.4525
A to Z ↑	0.0236	0.0241	2.8197	2.1194
B to Z ↓	0.0161	0.0161	1.9518	1.4687
B to Z ↑	0.0208	0.0210	2.8233	2.0933
C to Z ↓	0.0108	0.0115	1.9267	1.4550
C to Z ↑	0.0188	0.0193	2.8163	2.1001
D to Z ↓	0.0110	0.0109	1.9570	1.4784
D to Z ↑	0.0156	0.0157	2.8159	2.1093
	X24_P10		**X24_P10**	
A to Z ↓	0.0155		0.7498	
A to Z ↑	0.0237		1.0693	
B to Z ↓	0.0162		0.7583	
B to Z ↑	0.0207		1.0611	
C to Z ↓	0.0115		0.7334	
C to Z ↑	0.0193		1.0644	
D to Z ↓	0.0110		0.7458	
D to Z ↑	0.0157		1.0690	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P10	1.750e-07	1.000e-20
X6_P10	5.443e-07	1.000e-20
X9_P10	7.827e-07	1.000e-20
X12_P10	1.050e-06	1.000e-20
X24_P10	2.043e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P10	X6_P10	X9_P10	X12_P10
A (output stable)	1.742e-05	4.510e-05	8.386e-05	1.231e-04
B (output stable)	3.012e-05	8.212e-05	1.695e-04	2.456e-04
C (output stable)	1.068e-05	3.032e-05	6.202e-05	9.750e-05
D (output stable)	2.471e-05	7.273e-05	1.785e-04	2.867e-04
A to Z	1.023e-03	2.673e-03	4.244e-03	5.837e-03
B to Z	8.892e-04	2.310e-03	3.580e-03	4.909e-03
C to Z	5.874e-04	1.551e-03	2.539e-03	3.570e-03
D to Z	4.750e-04	1.262e-03	1.950e-03	2.665e-03
	X24_P10			
A (output stable)	2.208e-04			
B (output stable)	4.387e-04			
C (output stable)	1.982e-04			
D (output stable)	5.636e-04			

A to Z	1.128e-02			
B to Z	9.533e-03			
C to Z	6.944e-03			
D to Z	5.253e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

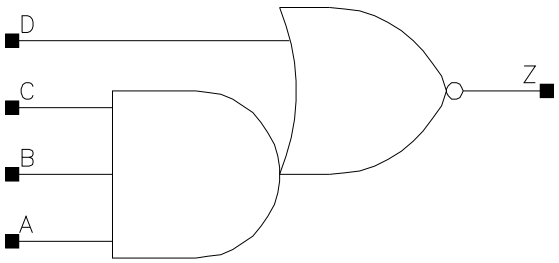
Pin Cycle (vdds)	X2_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X12_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X12_P10
A	0.0006	0.0022
B	0.0006	0.0022
C	0.0008	0.0020
D	0.0006	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X12_P10	X3_P10	X12_P10
A to Z ↓	0.0171	0.0180	7.4675	2.1194
A to Z ↑	0.0254	0.0244	8.8644	2.3103
B to Z ↓	0.0181	0.0179	7.4932	2.1265
B to Z ↑	0.0239	0.0221	8.9902	2.3109
C to Z ↓	0.0200	0.0173	7.5401	2.1383
C to Z ↑	0.0232	0.0189	9.0491	2.3273
D to Z ↓	0.0084	0.0072	3.2267	0.8807
D to Z ↑	0.0168	0.0145	7.7041	1.9859

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.735e-07	1.000e-20
X12_P10	9.358e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X12_P10
A (output stable)	2.974e-05	1.037e-04
B (output stable)	2.721e-05	1.217e-04
C (output stable)	5.326e-05	2.737e-04
D (output stable)	7.256e-05	2.819e-04
A to Z	1.548e-03	5.741e-03
B to Z	1.392e-03	4.831e-03
C to Z	1.275e-03	3.920e-03
D to Z	7.689e-04	2.440e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

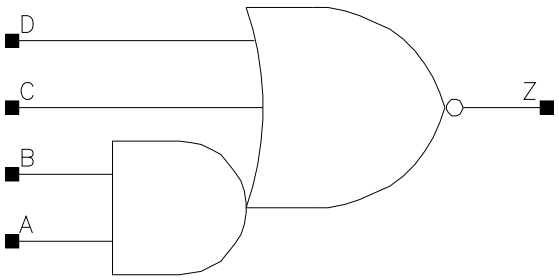
Pin Cycle (vdds)	X3_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X20_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P10	X20_P10
A	0.0005	0.0041
B	0.0005	0.0037
C	0.0006	0.0039
D	0.0006	0.0037

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X20_P10	X3_P10	X20_P10
A to Z ↓	0.0115	0.0126	5.2008	0.8489
A to Z ↑	0.0238	0.0225	13.1644	1.7072
B to Z ↓	0.0125	0.0128	5.2733	0.8613
B to Z ↑	0.0210	0.0181	13.2898	1.7091
C to Z ↓	0.0128	0.0171	3.2014	0.6692
C to Z ↑	0.0283	0.0269	12.5260	1.6113
D to Z ↓	0.0124	0.0156	3.2020	0.6686

D to Z ↑	0.0286	0.0252	12.5477	1.6165

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.336e-07	1.000e-20
X20_P10	1.404e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X20_P10
A (output stable)	7.272e-06	7.609e-05
B (output stable)	1.507e-05	1.699e-04
C (output stable)	1.225e-04	1.060e-03
D (output stable)	1.559e-05	1.069e-04
A to Z	9.592e-04	6.567e-03
B to Z	8.155e-04	5.030e-03
C to Z	1.528e-03	1.123e-02
D to Z	1.334e-03	8.891e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

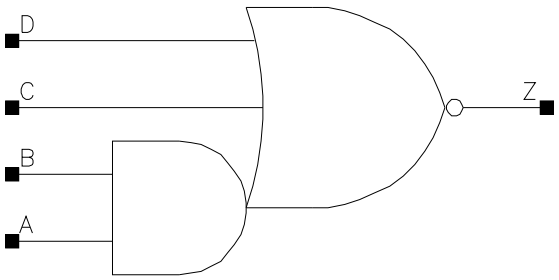
Pin Cycle (vdds)	X3_P10	X20_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.816	0.6528
X10_P10	0.800	2.448	1.9584
X19_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P10	X10_P10	X19_P10
A	0.0006	0.0022	0.0043
B	0.0005	0.0020	0.0041
C	0.0006	0.0018	0.0036
D	0.0005	0.0017	0.0032

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	X10_P10	X2_P10	X10_P10
A to Z ↓	0.0151	0.0157	6.1576	1.6495
A to Z ↑	0.0297	0.0280	13.9298	3.4036
B to Z ↓	0.0168	0.0163	6.2257	1.6668
B to Z ↑	0.0269	0.0241	13.9797	3.4127
C to Z ↓	0.0138	0.0129	5.3575	1.3512
C to Z ↑	0.0224	0.0208	13.2445	3.2290

D to Z ↓	0.0117	0.0098	5.4039	1.3667
D to Z ↑	0.0201	0.0167	13.2847	3.2466
	X19_P10		**X19_P10**	
A to Z ↓	0.0153		0.8468	
A to Z ↑	0.0272		1.7276	
B to Z ↓	0.0162		0.8564	
B to Z ↑	0.0234		1.7279	
C to Z ↓	0.0133		0.7281	
C to Z ↑	0.0200		1.6372	
D to Z ↓	0.0101		0.7371	
D to Z ↑	0.0160		1.6471	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P10	1.888e-07	1.000e-20
X10_P10	7.466e-07	1.000e-20
X19_P10	1.459e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P10	X10_P10	X19_P10
A (output stable)	2.429e-05	9.858e-05	1.928e-04
B (output stable)	2.871e-05	1.512e-04	2.860e-04
C (output stable)	2.684e-05	1.758e-04	3.313e-04
D (output stable)	1.296e-05	1.135e-04	2.059e-04
A to Z	1.476e-03	5.601e-03	1.067e-02
B to Z	1.325e-03	4.710e-03	9.003e-03
C to Z	8.860e-04	3.410e-03	6.408e-03
D to Z	6.838e-04	2.216e-03	4.114e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

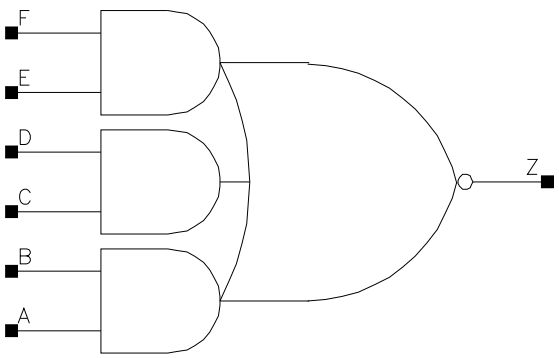
Pin Cycle (vdds)	X2_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.088	0.8704
X5_P10	0.800	2.040	1.6320
X7_P10	0.800	2.720	2.1760
X9_P10	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P10	X5_P10	X7_P10	X9_P10
A	0.0006	0.0010	0.0017	0.0022

B	0.0005	0.0011	0.0015	0.0020
C	0.0005	0.0010	0.0015	0.0023
D	0.0005	0.0011	0.0014	0.0020
E	0.0007	0.0011	0.0015	0.0019
F	0.0005	0.0009	0.0014	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X5_P10**	**X2_P10**	**X5_P10**
A to Z ↓	0.0162	0.0194	5.5021	3.1375
A to Z ↑	0.0379	0.0355	13.5074	6.1470
B to Z ↓	0.0180	0.0216	5.5636	3.1590
B to Z ↑	0.0349	0.0334	13.5642	6.1010
C to Z ↓	0.0151	0.0176	5.5466	3.1225
C to Z ↑	0.0335	0.0318	13.5886	6.1607
D to Z ↓	0.0166	0.0193	5.6263	3.1502
D to Z ↑	0.0304	0.0299	13.5716	6.1334
E to Z ↓	0.0116	0.0135	5.5863	3.0659
E to Z ↑	0.0260	0.0255	13.5616	6.1104
F to Z ↓	0.0123	0.0145	5.6836	3.1013
F to Z ↑	0.0221	0.0225	13.5268	6.1310
	X7_P10	**X9_P10**	**X7_P10**	**X9_P10**
A to Z ↓	0.0193	0.0197	2.1830	1.6630
A to Z ↑	0.0347	0.0355	4.0290	3.0330
B to Z ↓	0.0208	0.0209	2.2001	1.6757
B to Z ↑	0.0319	0.0323	4.1169	3.0797
C to Z ↓	0.0175	0.0182	2.1911	1.6519
C to Z ↑	0.0315	0.0328	4.1080	3.0812
D to Z ↓	0.0188	0.0185	2.2139	1.6688
D to Z ↑	0.0281	0.0285	4.0723	3.0567
E to Z ↓	0.0130	0.0132	2.1887	1.6538
E to Z ↑	0.0242	0.0242	4.0587	3.0605
F to Z ↓	0.0137	0.0131	2.2217	1.6810
F to Z ↑	0.0210	0.0204	4.0956	3.0583

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P10	3.212e-07	1.000e-20
X5_P10	6.476e-07	1.000e-20
X7_P10	9.367e-07	1.000e-20
X9_P10	1.221e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P10	X5_P10	X7_P10	X9_P10
A (output stable)	5.417e-05	1.052e-04	1.653e-04	2.340e-04
B (output stable)	1.232e-04	2.208e-04	3.319e-04	4.942e-04
C (output stable)	2.669e-05	4.871e-05	7.660e-05	1.242e-04
D (output stable)	4.481e-05	8.389e-05	1.463e-04	2.096e-04
E (output stable)	2.022e-05	3.888e-05	7.414e-05	1.073e-04
F (output stable)	3.328e-05	6.194e-05	1.274e-04	2.008e-04

A to Z	2.014e-03	4.113e-03	6.052e-03	8.252e-03
B to Z	1.843e-03	3.881e-03	5.444e-03	7.376e-03
C to Z	1.511e-03	3.170e-03	4.626e-03	6.290e-03
D to Z	1.353e-03	2.940e-03	4.078e-03	5.511e-03
E to Z	9.482e-04	2.185e-03	3.028e-03	4.024e-03
F to Z	8.055e-04	1.916e-03	2.526e-03	3.242e-03

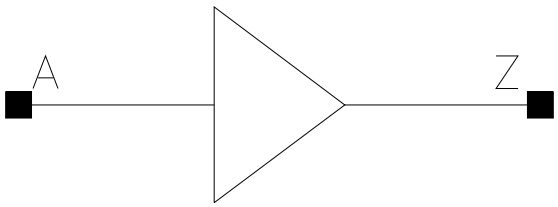
Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P10	X5_P10	X7_P10	X9_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description
Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.544	0.4352
X5_P10	0.800	0.544	0.4352
X9_P10	0.800	0.680	0.5440
X11_P10	1.600	0.408	0.6528
X13_P10	0.800	0.680	0.5440
X19_P10	0.800	0.952	0.7616
X23_P10	1.600	0.544	0.8704
X24_P10	0.800	1.088	0.8704
X29_P10	0.800	1.224	0.9792
X34_P10	1.600	0.680	1.0880
X38_P10	0.800	1.632	1.3056
X46_P10	1.600	0.952	1.5232
X57_P10	0.800	2.312	1.8496
X68_P10	1.600	1.224	1.9584
X91_P10	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P10	X5_P10	X9_P10	X11_P10
A	0.0006	0.0006	0.0006	0.0008
	X13_P10	X19_P10	X23_P10	X24_P10
A	0.0008	0.0010	0.0012	0.0012
	X29_P10	X34_P10	X38_P10	X46_P10
A	0.0014	0.0015	0.0020	0.0021
	X57_P10	X68_P10	X91_P10	
A	0.0027	0.0028	0.0038	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X5_P10**	**X2_P10**	**X5_P10**
A to Z ↓	0.0260	0.0268	5.8831	3.2057
A to Z ↑	0.0203	0.0203	9.3474	4.8144
	X9_P10	**X11_P10**	**X9_P10**	**X11_P10**
A to Z ↓	0.0321	0.0297	1.6491	1.2357
A to Z ↑	0.0241	0.0217	2.4026	2.2517
	X13_P10	**X19_P10**	**X13_P10**	**X19_P10**
A to Z ↓	0.0280	0.0283	1.1335	0.8000
A to Z ↑	0.0224	0.0212	1.6710	1.1657
	X23_P10	**X24_P10**	**X23_P10**	**X24_P10**
A to Z ↓	0.0284	0.0278	0.5987	0.6530
A to Z ↑	0.0208	0.0217	1.1346	0.9345
	X29_P10	**X34_P10**	**X29_P10**	**X34_P10**
A to Z ↓	0.0266	0.0279	0.5407	0.4131
A to Z ↑	0.0212	0.0210	0.7849	0.7756
	X38_P10	**X46_P10**	**X38_P10**	**X46_P10**
A to Z ↓	0.0262	0.0275	0.4095	0.3099
A to Z ↑	0.0210	0.0204	0.5778	0.5835
	X57_P10	**X68_P10**	**X57_P10**	**X68_P10**
A to Z ↓	0.0273	0.0270	0.2758	0.2106
A to Z ↑	0.0219	0.0204	0.3879	0.3899
	X91_P10		**X91_P10**	
A to Z ↓	0.0285		0.1630	
A to Z ↑	0.0214		0.2938	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P10	1.368e-07	1.000e-20
X5_P10	2.317e-07	1.000e-20
X9_P10	3.856e-07	1.000e-20
X11_P10	5.171e-07	1.000e-20
X13_P10	5.912e-07	1.000e-20
X19_P10	7.676e-07	1.000e-20
X23_P10	1.002e-06	1.000e-20
X24_P10	9.629e-07	1.000e-20
X29_P10	1.172e-06	1.000e-20
X34_P10	1.427e-06	1.000e-20
X38_P10	1.585e-06	1.000e-20
X46_P10	1.827e-06	1.000e-20
X57_P10	2.273e-06	1.000e-20
X68_P10	2.700e-06	1.000e-20
X91_P10	3.460e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P10	X5_P10	X9_P10	X11_P10
A to Z	1.090e-03	1.402e-03	2.223e-03	2.683e-03
	X13_P10	X19_P10	X23_P10	X24_P10
A to Z	3.209e-03	4.331e-03	4.839e-03	5.405e-03
	X29_P10	X34_P10	X38_P10	X46_P10

A to Z	6.265e-03	7.298e-03	8.641e-03	9.375e-03
	X57_P10	X68_P10	X91_P10	
A to Z	1.273e-02	1.367e-02	1.854e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

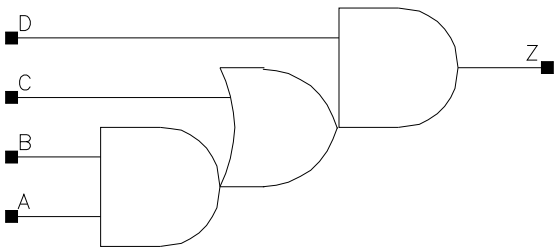
Pin Cycle (vdds)	X2_P10	X5_P10	X9_P10	X11_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P10	X19_P10	X23_P10	X24_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P10	X34_P10	X38_P10	X46_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P10	X68_P10	X91_P10	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.952	0.7616
X10_P10	0.800	1.632	1.3056
X14_P10	0.800	1.768	1.4144
X19_P10	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0006	0.0014	0.0014	0.0014
B	0.0007	0.0012	0.0012	0.0012
C	0.0007	0.0015	0.0015	0.0015
D	0.0010	0.0013	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0350	0.0323	3.2756	1.5495
A to Z ↑	0.0321	0.0294	4.9383	2.3452
B to Z ↓	0.0327	0.0298	3.2714	1.5487
B to Z ↑	0.0329	0.0298	4.9342	2.3443
C to Z ↓	0.0300	0.0272	3.2653	1.5456
C to Z ↑	0.0244	0.0219	4.8936	2.3220

D to Z ↓	0.0291	0.0252	3.2355	1.5312
D to Z ↑	0.0280	0.0239	4.8989	2.3255
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0355	0.0383	1.0848	0.8138
A to Z ↑	0.0324	0.0349	1.5749	1.1822
B to Z ↓	0.0332	0.0361	1.0833	0.8145
B to Z ↑	0.0329	0.0356	1.5740	1.1804
C to Z ↓	0.0304	0.0333	1.0805	0.8110
C to Z ↑	0.0243	0.0265	1.5545	1.1653
D to Z ↓	0.0273	0.0290	1.0659	0.7975
D to Z ↑	0.0261	0.0280	1.5579	1.1674

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	3.994e-07	1.000e-20
X10_P10	7.977e-07	1.000e-20
X14_P10	9.504e-07	1.000e-20
X19_P10	1.103e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	4.243e-05	8.524e-05	8.590e-05	8.532e-05
B (output stable)	6.240e-05	1.150e-04	1.156e-04	1.154e-04
C (output stable)	1.979e-04	3.377e-04	3.370e-04	3.350e-04
D (output stable)	6.301e-05	8.477e-05	8.555e-05	8.794e-05
A to Z	2.373e-03	4.314e-03	5.411e-03	6.432e-03
B to Z	2.219e-03	3.947e-03	5.041e-03	6.059e-03
C to Z	1.858e-03	3.216e-03	4.256e-03	5.239e-03
D to Z	2.412e-03	4.200e-03	5.220e-03	6.142e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

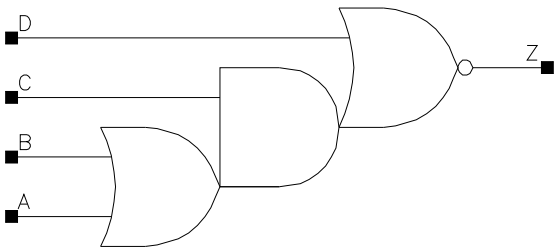
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X6_P10	0.800	1.496	1.1968
X9_P10	0.800	1.768	1.4144
X12_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X9_P10	X12_P10
A	0.0006	0.0012	0.0018	0.0022
B	0.0006	0.0011	0.0017	0.0022
C	0.0006	0.0011	0.0016	0.0021
D	0.0007	0.0011	0.0015	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0157	0.0145	5.4174	2.7689
A to Z ↑	0.0307	0.0304	13.1716	6.9417
B to Z ↓	0.0149	0.0143	5.2589	2.7880
B to Z ↑	0.0305	0.0294	13.1876	6.9539
C to Z ↓	0.0141	0.0133	5.0182	2.6053
C to Z ↑	0.0201	0.0190	9.0693	4.6942

D to Z ↓	0.0085	0.0070	3.2426	1.6518
D to Z ↑	0.0184	0.0157	9.6611	5.0260
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0146	0.0151	1.9069	1.4855
A to Z ↑	0.0284	0.0300	4.4748	3.4474
B to Z ↓	0.0140	0.0143	1.9248	1.4855
B to Z ↑	0.0282	0.0288	4.4809	3.4521
C to Z ↓	0.0136	0.0137	1.8061	1.3942
C to Z ↑	0.0184	0.0186	3.0482	2.3192
D to Z ↓	0.0072	0.0071	1.1537	0.8850
D to Z ↑	0.0148	0.0146	3.2551	2.4869

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.723e-07	1.000e-20
X6_P10	5.235e-07	1.000e-20
X9_P10	7.258e-07	1.000e-20
X12_P10	9.642e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	1.818e-05	4.651e-05	5.463e-05	9.751e-05
B (output stable)	5.505e-06	2.462e-05	3.281e-05	6.112e-05
C (output stable)	1.148e-04	2.746e-04	3.637e-04	5.522e-04
D (output stable)	2.648e-05	9.105e-05	1.045e-04	1.677e-04
A to Z	1.603e-03	3.049e-03	4.250e-03	5.919e-03
B to Z	1.390e-03	2.510e-03	3.633e-03	4.883e-03
C to Z	1.113e-03	2.026e-03	2.912e-03	3.958e-03
D to Z	7.190e-04	1.179e-03	1.636e-03	2.144e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

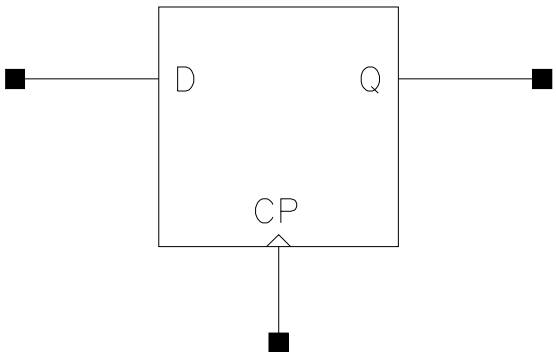
Pin Cycle (vdds)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	1.600	1.496	2.3936
X19_P10	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P10	X19_P10
CP	0.0009	0.0009
D	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P10	X19_P10	X10_P10	X19_P10
CP to Q ↓	0.0515	0.0691	1.6223	0.8847
CP to Q ↑	0.0588	0.0672	2.3151	1.1920

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P10	X19_P10
CP ↓	min_pulse_width to CP	0.0491	0.0491
CP ↑	min_pulse_width to CP	0.0406	0.0595
D ↓	hold_rising to CP	0.0124	0.0124
D ↑	hold_rising to CP	0.0081	0.0081
D ↓	setup_rising to CP	0.0273	0.0273
D ↑	setup_rising to CP	0.0200	0.0200

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P10	1.136e-06	1.000e-20
X19_P10	1.413e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

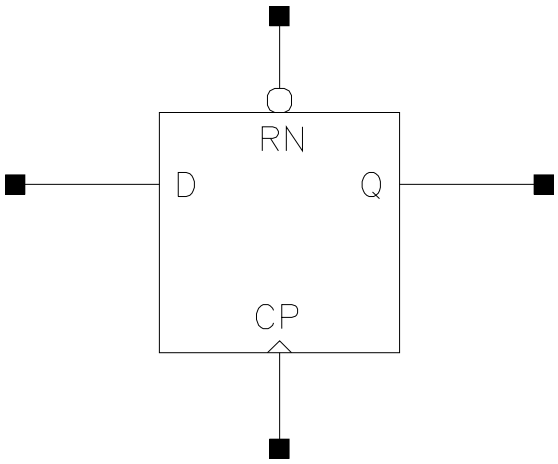
Pin Cycle	X10_P10	X19_P10
Clock 100Mhz Data 0Mhz	7.634e-03	7.640e-03
Clock 100Mhz Data 25Mhz	9.158e-03	1.064e-02
Clock 100Mhz Data 50Mhz	1.068e-02	1.363e-02
Clock = 0 Data 100Mhz	3.139e-03	3.139e-03
Clock = 1 Data 100Mhz	2.305e-05	2.313e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	1.600	1.768	2.8288
X19_P10	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P10	X19_P10
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0009	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P10	X19_P10	X10_P10	X19_P10
CP to Q ↓	0.0559	0.0719	1.6474	0.8768
CP to Q ↑	0.0612	0.0694	2.3136	1.1857
RN to Q ↓	0.0579	0.0743	1.6188	0.8438

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P10	X19_P10
CP ↓	min_pulse_width to CP	0.0490	0.0490
CP ↑	min_pulse_width to CP	0.0453	0.0595
D ↓	hold_rising to CP	0.0124	0.0124
D ↑	hold_rising to CP	0.0081	0.0081
D ↓	setup_rising to CP	0.0273	0.0273
D ↑	setup_rising to CP	0.0200	0.0200
RN ↓	min_pulse_width to RN	0.0708	0.0903
RN ↑	recovery_rising to CP	0.0103	0.0103
RN ↑	removal_rising to CP	-0.0055	-0.0055

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P10	1.312e-06	1.000e-20
X19_P10	1.657e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

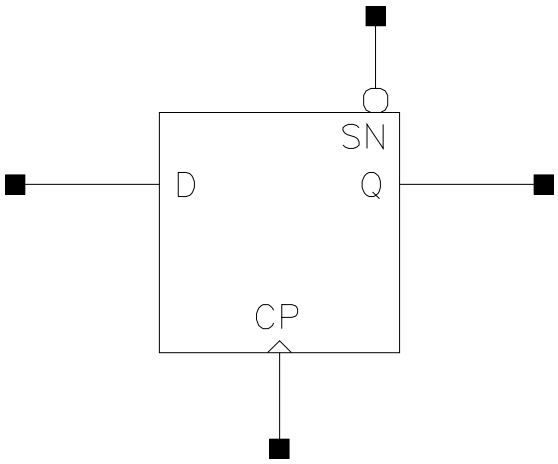
Pin Cycle	X10_P10	X19_P10
Clock 100Mhz Data 0Mhz	7.755e-03	7.756e-03
Clock 100Mhz Data 25Mhz	9.409e-03	1.089e-02
Clock 100Mhz Data 50Mhz	1.106e-02	1.402e-02
Clock = 0 Data 100Mhz	3.192e-03	3.192e-03
Clock = 1 Data 100Mhz	2.309e-05	2.318e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	1.600	1.768	2.8288
X19_P10	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P10	X19_P10
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0011	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P10	X19_P10	X10_P10	X19_P10
CP to Q ↓	0.0529	0.0702	1.6339	0.8698
CP to Q ↑	0.0606	0.0695	2.3097	1.1855
SN to Q ↑	0.0381	0.0431	2.2653	1.1510

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P10	X19_P10
CP ↓	min_pulse_width to CP	0.0525	0.0525
CP ↑	min_pulse_width to CP	0.0454	0.0595
D ↓	hold_rising to CP	0.0124	0.0124
D ↑	hold_rising to CP	0.0102	0.0102
D ↓	setup_rising to CP	0.0268	0.0268
D ↑	setup_rising to CP	0.0168	0.0168
SN ↓	min_pulse_width to SN	0.0420	0.0447
SN ↑	recovery_rising to CP	0.0037	0.0032
SN ↑	removal_rising to CP	0.0280	0.0280

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P10	1.333e-06	1.000e-20
X19_P10	1.633e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

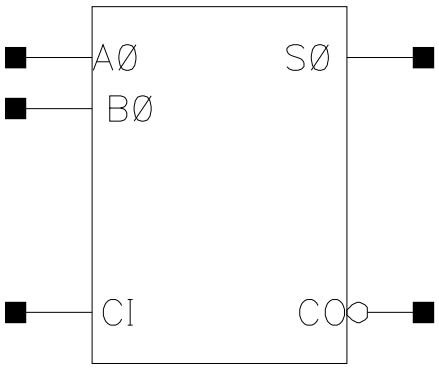
Pin Cycle	X10_P10	X19_P10
Clock 100Mhz Data 0Mhz	7.541e-03	7.543e-03
Clock 100Mhz Data 25Mhz	9.153e-03	1.069e-02
Clock 100Mhz Data 50Mhz	1.076e-02	1.384e-02
Clock = 0 Data 100Mhz	3.050e-03	3.050e-03
Clock = 1 Data 100Mhz	2.162e-05	2.172e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_-P10	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_-P10	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_-P10	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_-P10	1.600	2.720	4.3520
C8T28SOIDV_LLS1_-FA1X4_P10	1.600	2.040	3.2640
C8T28SOIDV_LLS1_-FA1X9_P10	1.600	3.128	5.0048
C8T28SOIDV_LLS1_-FA1X18_P10	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P10	C8T28SOIDV_LL_-FA1X9_P10	C8T28SOIDV_LL_-FA1X14_P10	C8T28SOIDV_LL_-FA1X19_P10
A0	0.0024	0.0025	0.0039	0.0042
B0	0.0020	0.0020	0.0036	0.0039
CI	0.0015	0.0015	0.0027	0.0029
	C8T28SOIDV_LLS1_-FA1X4_P10	C8T28SOIDV_LLS1_-FA1X9_P10	C8T28SOIDV_LLS1_-FA1X18_P10	
A0	0.0022	0.0031	0.0032	
B0	0.0021	0.0034	0.0038	
CI	0.0016	0.0024	0.0028	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P10	**C8T28SOIDV_LL_-FA1X9_P10**	**C8T28SOIDV_LL_-FA1X5_P10**	**C8T28SOIDV_LL_-FA1X9_P10**
A0 to CO ↓	0.0454	0.0484	3.3544	1.7225
A0 to CO ↑	0.0335	0.0358	4.5889	2.3440
A0 to S0 ↓	0.0490	0.0534	3.2937	1.6996
A0 to S0 ↑	0.0503	0.0543	4.5988	2.3039
B0 to CO ↓	0.0454	0.0487	3.3693	1.7311
B0 to CO ↑	0.0348	0.0370	4.5911	2.3463
B0 to S0 ↓	0.0494	0.0541	3.2929	1.6986
B0 to S0 ↑	0.0509	0.0552	4.5977	2.3035
CI to CO ↓	0.0432	0.0462	3.3712	1.7325
CI to CO ↑	0.0343	0.0365	4.5889	2.3440
CI to S0 ↓	0.0490	0.0537	3.2932	1.6987
CI to S0 ↑	0.0507	0.0548	4.5988	2.3040
	C8T28SOIDV_LL_-FA1X14_P10	**C8T28SOIDV_LL_-FA1X19_P10**	**C8T28SOIDV_LL_-FA1X14_P10**	**C8T28SOIDV_LL_-FA1X19_P10**
A0 to CO ↓	0.0464	0.0507	1.1264	0.8585
A0 to CO ↑	0.0343	0.0355	1.6134	1.2044
A0 to S0 ↓	0.0562	0.0569	1.1191	0.8312
A0 to S0 ↑	0.0573	0.0592	1.5557	1.1615
B0 to CO ↓	0.0457	0.0499	1.1298	0.8613
B0 to CO ↑	0.0348	0.0360	1.6127	1.2040
B0 to S0 ↓	0.0566	0.0572	1.1192	0.8307
B0 to S0 ↑	0.0575	0.0594	1.5566	1.1614
CI to CO ↓	0.0434	0.0476	1.1296	0.8611
CI to CO ↑	0.0341	0.0354	1.6130	1.2046
CI to S0 ↓	0.0556	0.0564	1.1189	0.8306
CI to S0 ↑	0.0567	0.0588	1.5552	1.1610
	C8T28SOIDV_-LLS1_FA1X4_P10	**C8T28SOIDV_-LLS1_FA1X9_P10**	**C8T28SOIDV_-LLS1_FA1X4_P10**	**C8T28SOIDV_-LLS1_FA1X9_P10**
A0 to CO ↓	0.0311	0.0284	6.2649	2.0930
A0 to CO ↑	0.0278	0.0259	4.6481	2.3448
A0 to S0 ↓	0.0646	0.0699	3.5185	1.2887
A0 to S0 ↑	0.0605	0.0594	4.8585	2.2920
B0 to CO ↓	0.0291	0.0292	6.2575	2.0951
B0 to CO ↑	0.0234	0.0244	4.6354	2.3429
B0 to S0 ↓	0.0651	0.0728	3.5180	1.2887
B0 to S0 ↑	0.0611	0.0624	4.8590	2.2926
CI to CO ↓	0.0295	0.0399	6.2584	2.1115
CI to CO ↑	0.0255	0.0239	4.6479	2.3606

CI to S0 ↓	0.0371	0.0441	3.5215	1.2902
CI to S0 ↑	0.0324	0.0330	4.8603	2.2929
	C8T28SOIDV_-LLS1_FA1X18_P10		**C8T28SOIDV_-LLS1_FA1X18_P10**	
A0 to CO ↓	0.0358		1.1062	
A0 to CO ↑	0.0271		1.1529	
A0 to S0 ↓	0.0743		0.6688	
A0 to S0 ↑	0.0604		1.1517	
B0 to CO ↓	0.0373		1.1075	
B0 to CO ↑	0.0258		1.1516	
B0 to S0 ↓	0.0757		0.6689	
B0 to S0 ↑	0.0622		1.1523	
CI to CO ↓	0.0496		1.1177	
CI to CO ↑	0.0282		1.1548	
CI to S0 ↓	0.0458		0.6691	
CI to S0 ↑	0.0307		1.1523	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P10	9.654e-07	1.000e-20
C8T28SOIDV_LL_FA1X9_P10	1.316e-06	1.000e-20
C8T28SOIDV_LL_FA1X14_P10	1.967e-06	1.000e-20
C8T28SOIDV_LL_FA1X19_P10	2.445e-06	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P10	1.891e-06	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P10	2.909e-06	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P10	4.426e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P10	C8T28SOIDV_LL_-FA1X9_P10	C8T28SOIDV_LL_-FA1X14_P10	C8T28SOIDV_LL_-FA1X19_P10
A0 to CO	2.626e-03	3.576e-03	5.981e-03	7.157e-03
A0 to S0	2.694e-03	3.518e-03	6.086e-03	7.313e-03
B0 to CO	2.597e-03	3.566e-03	5.897e-03	7.097e-03
B0 to S0	2.579e-03	3.423e-03	5.891e-03	7.094e-03
CI to CO	2.547e-03	3.491e-03	5.813e-03	7.055e-03
CI to S0	2.550e-03	3.381e-03	5.802e-03	7.011e-03
	C8T28SOIDV_LLS1_-FA1X4_P10	C8T28SOIDV_LLS1_-FA1X9_P10	C8T28SOIDV_LLS1_-FA1X18_P10	
A0 to CO	4.070e-03	6.177e-03	9.739e-03	
A0 to S0	5.520e-03	8.001e-03	1.216e-02	
B0 to CO	4.314e-03	6.286e-03	9.809e-03	
B0 to S0	5.900e-03	8.174e-03	1.231e-02	
CI to CO	2.897e-03	5.077e-03	8.422e-03	
CI to S0	3.277e-03	5.653e-03	9.169e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P10	C8T28SOIDV_LL_-FA1X9_P10	C8T28SOIDV_LL_-FA1X14_P10	C8T28SOIDV_LL_-FA1X19_P10
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P10	C8T28SOIDV_LLS1_-FA1X9_P10	C8T28SOIDV_LLS1_-FA1X18_P10	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P10	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P10	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P10	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P10	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P10	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P10	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P10	C8T28SOI_LL_-HA1X9_P10	C8T28SOI_LLS1_-HA1X5_P10	C8T28SOIDV_LL_-HA1X14_P10
A0	0.0008	0.0011	0.0013	0.0016
B0	0.0007	0.0011	0.0012	0.0014
	C8T28SOIDV_LL_-HA1X19_P10	C8T28SOIDV_LLS1_-HA1X11_P10		
A0	0.0020	0.0020		
B0	0.0017	0.0019		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P10	**C8T28SOI_LL_-HA1X9_P10**	**C8T28SOI_LL_-HA1X5_P10**	**C8T28SOI_LL_-HA1X9_P10**
A0 to CO ↓	0.0359	0.0308	3.3106	1.6283
A0 to CO ↑	0.0324	0.0286	4.9002	2.3660
A0 to S0 ↓	0.0455	0.0415	3.1609	1.6110
A0 to S0 ↑	0.0429	0.0394	4.7586	2.3554
B0 to CO ↓	0.0350	0.0300	3.3144	1.6295
B0 to CO ↑	0.0348	0.0310	4.9006	2.3665
B0 to S0 ↓	0.0471	0.0424	3.1597	1.6115
B0 to S0 ↑	0.0423	0.0387	4.7562	2.3558
	C8T28SOI_LLS1_-HA1X5_P10	**C8T28SOIDV_LL_-HA1X14_P10**	**C8T28SOI_LLS1_-HA1X5_P10**	**C8T28SOIDV_LL_-HA1X14_P10**
A0 to CO ↓	0.0291	0.0319	3.2362	1.1135
A0 to CO ↑	0.0260	0.0286	4.8407	1.5896
A0 to S0 ↓	0.0393	0.0459	3.2270	1.1237
A0 to S0 ↑	0.0436	0.0432	4.8661	1.5663
B0 to CO ↓	0.0276	0.0297	3.2389	1.1102
B0 to CO ↑	0.0277	0.0293	4.8405	1.5903
B0 to S0 ↓	0.0411	0.0453	3.2279	1.1230
B0 to S0 ↑	0.0428	0.0414	4.8672	1.5665
	C8T28SOIDV_LL_-HA1X19_P10	**C8T28SOIDV_-LLS1_HA1X11_P10**	**C8T28SOIDV_LL_-HA1X19_P10**	**C8T28SOIDV_-LLS1_HA1X11_P10**
A0 to CO ↓	0.0295	0.0280	0.8189	1.1680
A0 to CO ↑	0.0274	0.0278	1.2033	2.3206
A0 to S0 ↓	0.0422	0.0352	0.8139	1.1864
A0 to S0 ↑	0.0400	0.0368	1.1757	2.3381
B0 to CO ↓	0.0276	0.0265	0.8167	1.1669
B0 to CO ↑	0.0283	0.0299	1.2031	2.3203
B0 to S0 ↓	0.0423	0.0365	0.8137	1.1841
B0 to S0 ↑	0.0383	0.0368	1.1754	2.3380

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_HA1X5_P10	5.159e-07	1.000e-20
C8T28SOI_LL_HA1X9_P10	1.131e-06	1.000e-20
C8T28SOI_LLS1_HA1X5_P10	6.325e-07	1.000e-20
C8T28SOIDV_LL_HA1X14_P10	1.609e-06	1.000e-20
C8T28SOIDV_LL_HA1X19_P10	2.243e-06	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P10	1.571e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

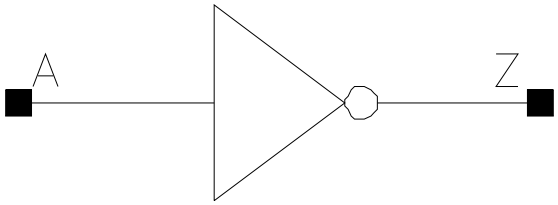
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P10	C8T28SOI_LL_-HA1X9_P10	C8T28SOI_LLS1_-HA1X5_P10	C8T28SOIDV_LL_-HA1X14_P10
A0 to CO	1.972e-03	3.177e-03	2.379e-03	5.155e-03
A0 to S0	1.773e-03	3.031e-03	2.097e-03	5.114e-03
B0 to CO	1.977e-03	3.215e-03	2.380e-03	4.996e-03
B0 to S0	1.736e-03	2.923e-03	2.029e-03	4.898e-03
	C8T28SOIDV_LL_-HA1X19_P10	C8T28SOIDV_LLS1_-HA1X11_P10		
A0 to CO	6.129e-03	4.358e-03		
A0 to S0	6.110e-03	3.956e-03		

B0 to CO	6.003e-03	4.153e-03		
B0 to S0	5.904e-03	4.174e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P10	C8T28SOI_LL_-HA1X9_P10	C8T28SOI_LLS1_-HA1X5_P10	C8T28SOIDV_LL_-HA1X14_P10
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P10	C8T28SOIDV_LLS1_-HA1X11_P10		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P10	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P10	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P10	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P10	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P10	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P10	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P10	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P10	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P10	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P10	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P10	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P10	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P10	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P10	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P10	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P10	C8T28SOI_LL_IVX3_-P10	C8T28SOI_LL_IVX5_-P10	C8T28SOI_LL_-IVX10_P10

A	0.0004	0.0005	0.0006	0.0011
	C8T28SOI_LL_-IVX14_P10	C8T28SOI_LL_-IVX19_P10	C8T28SOI_LL_-IVX29_P10	C8T28SOI_LL_-IVX34_P10
A	0.0016	0.0021	0.0031	0.0036
	C8T28SOI_LL_-IVX38_P10	C8T28SOIDV_LL_-IVX11_P10	C8T28SOIDV_LL_-IVX23_P10	C8T28SOIDV_LL_-IVX34_P10
A	0.0042	0.0012	0.0023	0.0034
	C8T28SOIDV_LL_-IVX46_P10	C8T28SOIDV_LL_-IVX68_P10	C8T28SOIDV_LL_-IVX91_P10	
A	0.0045	0.0069	0.0096	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P10	**C8T28SOI_LL_-IVX3_P10**	**C8T28SOI_LL_-IVX2_P10**	**C8T28SOI_LL_-IVX3_P10**
A to Z ↓	0.0081	0.0076	6.1170	4.7753
A to Z ↑	0.0139	0.0126	9.6092	7.2188
	C8T28SOI_LL_-IVX5_P10	**C8T28SOI_LL_-IVX10_P10**	**C8T28SOI_LL_-IVX5_P10**	**C8T28SOI_LL_-IVX10_P10**
A to Z ↓	0.0069	0.0055	3.3183	1.5981
A to Z ↑	0.0112	0.0094	4.9589	2.3569
	C8T28SOI_LL_-IVX14_P10	**C8T28SOI_LL_-IVX19_P10**	**C8T28SOI_LL_-IVX14_P10**	**C8T28SOI_LL_-IVX19_P10**
A to Z ↓	0.0058	0.0062	1.1127	0.8500
A to Z ↑	0.0094	0.0097	1.5855	1.2168
	C8T28SOI_LL_-IVX29_P10	**C8T28SOI_LL_-IVX34_P10**	**C8T28SOI_LL_-IVX29_P10**	**C8T28SOI_LL_-IVX34_P10**
A to Z ↓	0.0061	0.0057	0.5683	0.4841
A to Z ↑	0.0093	0.0089	0.8050	0.6872
	C8T28SOI_LL_-IVX38_P10	**C8T28SOIDV_LL_-IVX11_P10**	**C8T28SOI_LL_-IVX38_P10**	**C8T28SOIDV_LL_-IVX11_P10**
A to Z ↓	0.0059	0.0056	0.4302	1.2732
A to Z ↑	0.0091	0.0107	0.6099	2.3961
	C8T28SOIDV_LL_-IVX23_P10	**C8T28SOIDV_LL_-IVX34_P10**	**C8T28SOIDV_LL_-IVX23_P10**	**C8T28SOIDV_LL_-IVX34_P10**
A to Z ↓	0.0048	0.0051	0.6210	0.4268
A to Z ↑	0.0095	0.0097	1.1676	0.7834
	C8T28SOIDV_LL_-IVX46_P10	**C8T28SOIDV_LL_-IVX68_P10**	**C8T28SOIDV_LL_-IVX46_P10**	**C8T28SOIDV_LL_-IVX68_P10**
A to Z ↓	0.0050	0.0050	0.3214	0.2190
A to Z ↑	0.0093	0.0092	0.5873	0.3948
	C8T28SOIDV_LL_-IVX91_P10		**C8T28SOIDV_LL_-IVX91_P10**	
A to Z ↓	0.0055		0.1701	
A to Z ↑	0.0095		0.3004	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_IVX2_P10	7.235e-08	1.000e-20
C8T28SOI_LL_IVX3_P10	1.026e-07	1.000e-20
C8T28SOI_LL_IVX5_P10	1.592e-07	1.000e-20
C8T28SOI_LL_IVX10_P10	3.326e-07	1.000e-20

C8T28SOI_LL_IVX14_P10	4.725e-07	1.000e-20
C8T28SOI_LL_IVX19_P10	6.097e-07	1.000e-20
C8T28SOI_LL_IVX29_P10	8.844e-07	1.000e-20
C8T28SOI_LL_IVX34_P10	1.022e-06	1.000e-20
C8T28SOI_LL_IVX38_P10	1.160e-06	1.000e-20
C8T28SOIDV_LL_IVX11_P10	3.960e-07	1.000e-20
C8T28SOIDV_LL_IVX23_P10	7.846e-07	1.000e-20
C8T28SOIDV_LL_IVX34_P10	1.117e-06	1.000e-20
C8T28SOIDV_LL_IVX46_P10	1.441e-06	1.000e-20
C8T28SOIDV_LL_IVX68_P10	2.088e-06	1.000e-20
C8T28SOIDV_LL_IVX91_P10	2.738e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P10	C8T28SOI_LL_IVX3_-P10	C8T28SOI_LL_IVX5_-P10	C8T28SOI_LL_-IVX10_P10
A to Z	3.174e-04	3.782e-04	4.625e-04	8.013e-04
	C8T28SOI_LL_-IVX14_P10	C8T28SOI_LL_-IVX19_P10	C8T28SOI_LL_-IVX29_P10	C8T28SOI_LL_-IVX34_P10
A to Z	1.244e-03	1.714e-03	2.453e-03	2.710e-03
	C8T28SOI_LL_-IVX38_P10	C8T28SOIDV_LL_-IVX11_P10	C8T28SOIDV_LL_-IVX23_P10	C8T28SOIDV_LL_-IVX34_P10
A to Z	3.173e-03	9.908e-04	1.727e-03	2.677e-03
	C8T28SOIDV_LL_-IVX46_P10	C8T28SOIDV_LL_-IVX68_P10	C8T28SOIDV_LL_-IVX91_P10	
A to Z	3.272e-03	4.878e-03	6.543e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

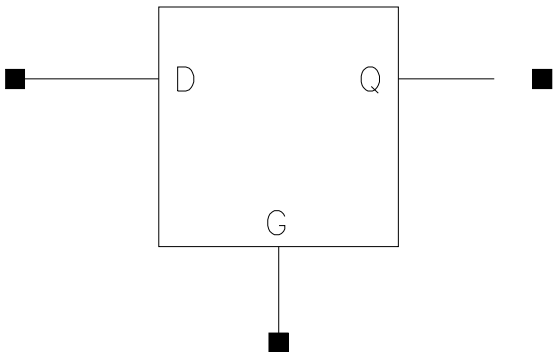
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P10	C8T28SOI_LL_IVX3_-P10	C8T28SOI_LL_IVX5_-P10	C8T28SOI_LL_-IVX10_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P10	C8T28SOI_LL_-IVX19_P10	C8T28SOI_LL_-IVX29_P10	C8T28SOI_LL_-IVX34_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P10	C8T28SOIDV_LL_-IVX11_P10	C8T28SOIDV_LL_-IVX23_P10	C8T28SOIDV_LL_-IVX34_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P10	C8T28SOIDV_LL_-IVX68_P10	C8T28SOIDV_LL_-IVX91_P10	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.360	1.0880
X9_P10	1.600	0.952	1.5232
X19_P10	1.600	1.224	1.9584
X28_P10	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10	X28_P10
D	0.0004	0.0007	0.0010	0.0016
G	0.0009	0.0009	0.0018	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D to Q ↓	0.0513	0.0487	3.3913	1.7264
D to Q ↑	0.0292	0.0342	4.7432	2.3175
G to Q ↓	0.0544	0.0507	3.3842	1.7228

G to Q ↑	0.0285	0.0321	4.7478	2.3183
	X19_P10	**X28_P10**	**X19_P10**	**X28_P10**
D to Q ↓	0.0399	0.0421	0.8248	0.5555
D to Q ↑	0.0296	0.0299	1.1663	0.7832
G to Q ↓	0.0441	0.0404	0.8233	0.5547
G to Q ↑	0.0276	0.0278	1.1672	0.7834

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P10	X9_P10	X19_P10	X28_P10
D ↓	hold_falling to G	-0.0094	-0.0094	-0.0023	-0.0039
D ↑	hold_falling to G	0.0019	0.0002	0.0019	0.0019
D ↓	setup_falling to G	0.0488	0.0440	0.0337	0.0366
D ↑	setup_falling to G	0.0302	0.0351	0.0356	0.0351
G ↑	min_pulse_width to G	0.0424	0.0410	0.0396	0.0396

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	4.196e-07	1.000e-20
X9_P10	6.779e-07	1.000e-20
X19_P10	1.149e-06	1.000e-20
X28_P10	1.558e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	1.138e-05	4.719e-05	3.512e-05	1.012e-04
G (output stable)	7.850e-04	9.289e-04	1.529e-03	1.357e-03
D to Q	2.927e-03	4.575e-03	6.825e-03	1.001e-02
G to Q	2.682e-03	4.206e-03	6.175e-03	8.527e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

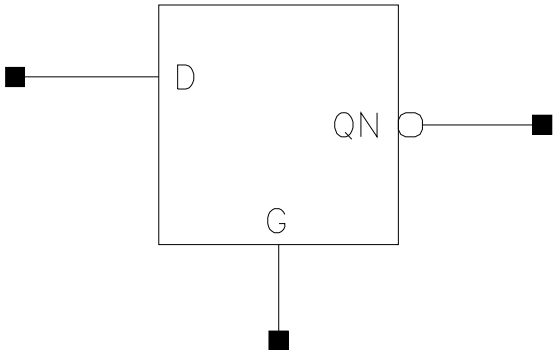
life.augmented

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P10
D	0.0004
G	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P10	X10_P10
D to QN ↓	0.0445	1.5596
D to QN ↑	0.0601	2.3057
G to QN ↓	0.0435	1.5602
G to QN ↑	0.0625	2.3030

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P10
D ↓	hold_falling to G	-0.0191
D ↑	hold_falling to G	-0.0035
D ↓	setup_falling to G	0.0440
D ↑	setup_falling to G	0.0307
G ↑	min_pulse_width to G	0.0376

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P10	6.237e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X10_P10
D (output stable)	1.552e-05
G (output stable)	8.286e-04
D to QN	3.960e-03
G to QN	3.647e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

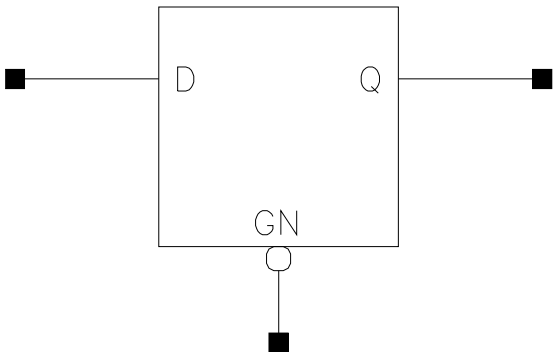
Pin Cycle (vdds)	X10_P10
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.360	1.0880
X9_P10	1.600	0.952	1.5232
X19_P10	1.600	1.224	1.9584
X28_P10	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10	X28_P10
D	0.0004	0.0007	0.0010	0.0014
GN	0.0009	0.0009	0.0013	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D to Q ↓	0.0517	0.0479	3.3991	1.7309
D to Q ↑	0.0294	0.0338	4.7387	2.3215
GN to Q ↓	0.0463	0.0455	3.3993	1.7342

GN to Q ↑	0.0500	0.0475	4.7363	2.3113
	X19_P10	**X28_P10**	**X19_P10**	**X28_P10**
D to Q ↓	0.0404	0.0406	0.8208	0.5548
D to Q ↑	0.0311	0.0307	1.1609	0.7766
GN to Q ↓	0.0362	0.0351	0.8224	0.5551
GN to Q ↑	0.0425	0.0424	1.1574	0.7760

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P10	X9_P10	X19_P10	X28_P10
D ↓	hold_rising to GN	-0.0171	-0.0123	-0.0074	-0.0047
D ↑	hold_rising to GN	0.0053	0.0032	0.0058	0.0053
D ↓	setup_rising to GN	0.0569	0.0500	0.0446	0.0419
D ↑	setup_rising to GN	0.0271	0.0319	0.0293	0.0265
GN ↓	min_pulse_width to GN	0.0599	0.0555	0.0514	0.0469

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	4.101e-07	1.000e-20
X9_P10	6.732e-07	1.000e-20
X19_P10	1.195e-06	1.000e-20
X28_P10	1.568e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	1.213e-05	2.218e-05	4.099e-05	9.535e-05
GN (output stable)	7.852e-04	9.059e-04	1.285e-03	1.352e-03
D to Q	2.921e-03	4.580e-03	7.029e-03	9.829e-03
GN to Q	4.432e-03	6.228e-03	9.099e-03	1.171e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

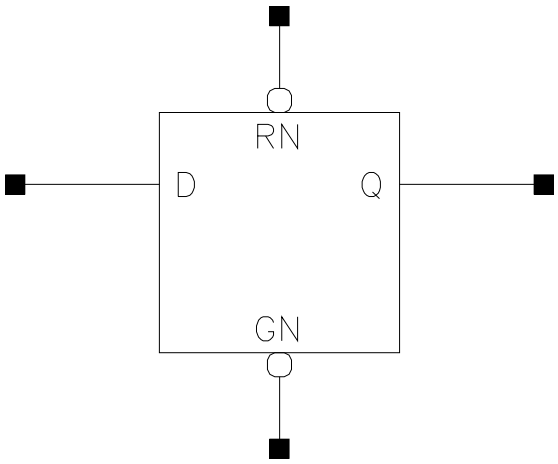
Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.632	1.3056
X9_P10	1.600	1.224	1.9584
X19_P10	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10
D	0.0004	0.0006	0.0012
GN	0.0010	0.0010	0.0015
RN	0.0004	0.0005	0.0005

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D to Q ↓	0.0527	0.0501	3.3328	1.6768

D to Q ↑	0.0467	0.0512	4.9287	2.4057
GN to Q ↓	0.0485	0.0465	3.3341	1.6792
GN to Q ↑	0.0639	0.0604	4.9241	2.4127
RN to Q ↓	0.0431	0.0537	3.2033	1.6760
RN to Q ↑	0.0506	0.0546	4.9276	2.4079
	X19_P10		**X19_P10**	
D to Q ↓	0.0420		0.8266	
D to Q ↑	0.0545		1.2168	
GN to Q ↓	0.0381		0.8268	
GN to Q ↑	0.0575		1.2213	
RN to Q ↓	0.0689		0.8914	
RN to Q ↑	0.0596		1.2191	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P10	X9_P10	X19_P10
D ↓	hold_rising to GN	-0.0171	-0.0149	-0.0068
D ↑	hold_rising to GN	-0.0061	-0.0110	-0.0159
D ↓	setup_rising to GN	0.0565	0.0549	0.0473
D ↑	setup_rising to GN	0.0465	0.0513	0.0589
GN ↓	min_pulse_width to GN	0.0647	0.0616	0.0589
RN ↓	min_pulse_width to RN	0.0540	0.0637	0.0806
RN ↑	recovery_rising to GN	0.0509	0.0562	0.0653
RN ↑	removal_rising to GN	-0.0314	-0.0359	-0.0440

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	4.245e-07	1.000e-20
X9_P10	6.654e-07	1.000e-20
X19_P10	1.139e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10
D (output stable)	6.534e-05	5.060e-05	6.300e-05
GN (output stable)	8.887e-04	8.563e-04	1.072e-03
RN (output stable)	2.333e-05	2.491e-05	2.882e-05
D to Q	3.597e-03	5.044e-03	7.648e-03
GN to Q	5.216e-03	6.618e-03	9.497e-03
RN to Q	2.834e-03	3.929e-03	6.056e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

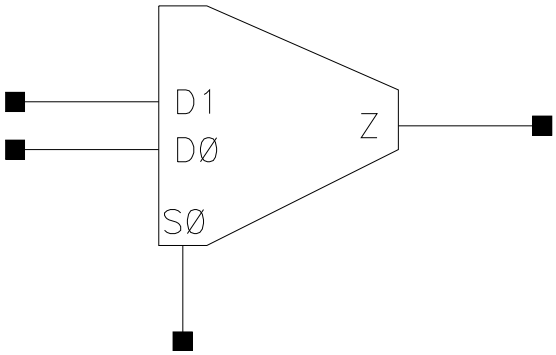
Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.360	1.0880
X9_P10	0.800	1.496	1.1968
X14_P10	0.800	2.176	1.7408
X19_P10	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P10	X9_P10	X14_P10	X19_P10
D0	0.0006	0.0007	0.0010	0.0013
D1	0.0005	0.0007	0.0010	0.0013
S0	0.0010	0.0010	0.0013	0.0016

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D0 to Z ↓	0.0386	0.0361	3.3323	1.6906
D0 to Z ↑	0.0301	0.0296	4.8537	2.4725
D1 to Z ↓	0.0391	0.0353	3.3318	1.6885
D1 to Z ↑	0.0297	0.0280	4.8622	2.4685
S0 to Z ↓	0.0366	0.0320	3.3241	1.6845
S0 to Z ↑	0.0343	0.0315	4.8603	2.4696

	X14_P10	X19_P10	X14_P10	X19_P10
D0 to Z ↓	0.0392	0.0345	1.1720	0.8437
D0 to Z ↑	0.0312	0.0288	1.6732	1.2108
D1 to Z ↓	0.0399	0.0356	1.1699	0.8453
D1 to Z ↑	0.0298	0.0279	1.6701	1.2097
S0 to Z ↓	0.0378	0.0349	1.1670	0.8430
S0 to Z ↑	0.0366	0.0333	1.6707	1.2098

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	4.794e-07	1.000e-20
X9_P10	8.164e-07	1.000e-20
X14_P10	1.082e-06	1.000e-20
X19_P10	1.605e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X9_P10	X14_P10	X19_P10
D0 (output stable)	5.166e-04	9.602e-04	1.083e-03	1.314e-03
D1 (output stable)	4.919e-04	8.007e-04	1.136e-03	1.412e-03
S0 (output stable)	8.293e-04	7.459e-04	1.218e-03	1.425e-03
D0 to Z	2.169e-03	3.359e-03	5.327e-03	6.474e-03
D1 to Z	2.111e-03	3.143e-03	5.173e-03	6.413e-03
S0 to Z	2.655e-03	3.303e-03	5.870e-03	7.049e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

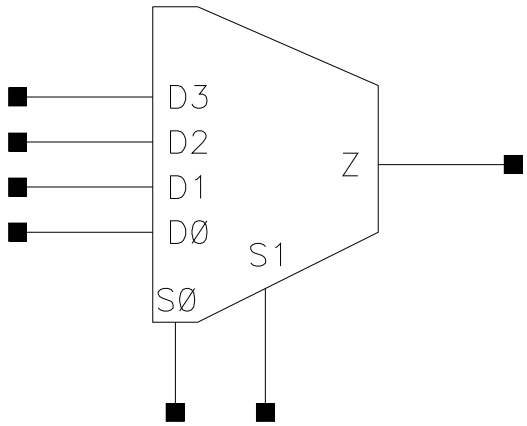
Pin Cycle (vdds)	X5_P10	X9_P10	X14_P10	X19_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.600	1.496	2.3936
X9_P10	1.600	1.768	2.8288
X13_P10	1.600	2.312	3.6992
X18_P10	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P10	X9_P10	X13_P10	X18_P10
D0	0.0004	0.0007	0.0010	0.0010
D1	0.0004	0.0005	0.0010	0.0010
D2	0.0004	0.0007	0.0010	0.0010
D3	0.0004	0.0006	0.0010	0.0010
S0	0.0013	0.0017	0.0023	0.0023
S1	0.0008	0.0009	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X9_P10	X4_P10	X9_P10
D0 to Z ↓	0.0825	0.0687	3.6370	1.7856
D0 to Z ↑	0.0501	0.0459	5.0064	2.4808
D1 to Z ↓	0.0813	0.0684	3.6320	1.7867
D1 to Z ↑	0.0501	0.0457	4.9985	2.4790
D2 to Z ↓	0.0755	0.0693	3.5822	1.7899
D2 to Z ↑	0.0485	0.0456	4.9726	2.4789
D3 to Z ↓	0.0764	0.0683	3.5873	1.7876
D3 to Z ↑	0.0493	0.0456	4.9744	2.4776
S0 to Z ↓	0.0851	0.0758	3.6091	1.7856
S0 to Z ↑	0.0597	0.0575	5.0013	2.4825
S1 to Z ↓	0.0544	0.0514	3.6059	1.7863
S1 to Z ↑	0.0427	0.0432	4.9830	2.4779
	X13_P10	X18_P10	X13_P10	X18_P10
D0 to Z ↓	0.0674	0.0732	1.2520	0.9386
D0 to Z ↑	0.0417	0.0450	1.6608	1.2569
D1 to Z ↓	0.0678	0.0736	1.2529	0.9389
D1 to Z ↑	0.0429	0.0462	1.6605	1.2575
D2 to Z ↓	0.0615	0.0667	1.2319	0.9219
D2 to Z ↑	0.0416	0.0449	1.6560	1.2550
D3 to Z ↓	0.0612	0.0663	1.2310	0.9214
D3 to Z ↑	0.0419	0.0451	1.6554	1.2544
S0 to Z ↓	0.0716	0.0771	1.2412	0.9295
S0 to Z ↑	0.0529	0.0562	1.6597	1.2572
S1 to Z ↓	0.0494	0.0549	1.2412	0.9295
S1 to Z ↑	0.0397	0.0430	1.6573	1.2555

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	5.158e-07	1.000e-20
X9_P10	8.290e-07	1.000e-20
X13_P10	1.415e-06	1.000e-20
X18_P10	1.572e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X9_P10	X13_P10	X18_P10
D0 (output stable)	9.323e-05	9.384e-05	1.712e-04	1.694e-04
D1 (output stable)	9.167e-05	1.057e-04	1.500e-04	1.484e-04
D2 (output stable)	3.344e-05	3.286e-05	4.574e-05	4.497e-05
D3 (output stable)	5.632e-05	7.689e-05	9.770e-05	9.786e-05
S0 (output stable)	1.225e-03	1.476e-03	2.381e-03	2.380e-03
S1 (output stable)	8.981e-04	1.038e-03	1.671e-03	1.670e-03
D0 to Z	2.737e-03	3.966e-03	6.515e-03	7.811e-03
D1 to Z	2.708e-03	3.959e-03	6.589e-03	7.885e-03
D2 to Z	2.570e-03	3.948e-03	6.254e-03	7.512e-03
D3 to Z	2.600e-03	3.944e-03	6.271e-03	7.522e-03
S0 to Z	4.026e-03	5.653e-03	9.125e-03	1.040e-02
S1 to Z	2.642e-03	3.866e-03	6.230e-03	7.488e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

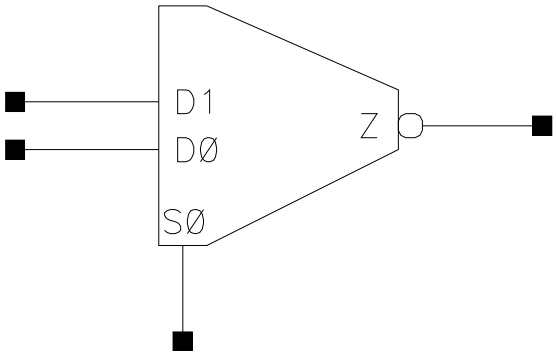
Pin Cycle (vdds)	X4_P10	X9_P10	X13_P10	X18_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P10	0.800	0.952	0.7616
X2_P10	0.800	0.952	0.7616
X6_P10	0.800	1.904	1.5232
X9_P10	0.800	2.448	1.9584
X12_P10	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P10	X2_P10	X6_P10	X9_P10
D0	0.0004	0.0005	0.0012	0.0017
D1	0.0004	0.0005	0.0011	0.0017
S0	0.0010	0.0013	0.0019	0.0027
	X12_P10			
D0	0.0023			
D1	0.0022			
S0	0.0031			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P10	X2_P10	X1_P10	X2_P10
D0 to Z ↓	0.0136	0.0131	9.2337	6.2953

D0 to Z ↑	0.0262	0.0206	20.6532	11.0534
D1 to Z ↓	0.0131	0.0123	9.1090	6.1599
D1 to Z ↑	0.0266	0.0216	20.6767	11.2288
S0 to Z ↓	0.0239	0.0168	9.1376	6.2380
S0 to Z ↑	0.0269	0.0178	20.5888	11.1424
	X6_P10	**X9_P10**	**X6_P10**	**X9_P10**
D0 to Z ↓	0.0146	0.0136	2.8413	1.9115
D0 to Z ↑	0.0217	0.0207	4.5911	3.2055
D1 to Z ↓	0.0140	0.0136	2.7800	1.9242
D1 to Z ↑	0.0230	0.0214	4.7481	3.1290
S0 to Z ↓	0.0198	0.0170	2.8105	1.9182
S0 to Z ↑	0.0205	0.0181	4.6660	3.1697
	X12_P10		**X12_P10**	
D0 to Z ↓	0.0141		1.4648	
D0 to Z ↑	0.0208		2.4186	
D1 to Z ↓	0.0135		1.4591	
D1 to Z ↑	0.0213		2.3573	
S0 to Z ↓	0.0184		1.4613	
S0 to Z ↑	0.0192		2.3884	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X1_P10	1.807e-07	1.000e-20
X2_P10	3.556e-07	1.000e-20
X6_P10	7.201e-07	1.000e-20
X9_P10	1.112e-06	1.000e-20
X12_P10	1.352e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X1_P10	X2_P10	X6_P10	X9_P10
D0 (output stable)	1.213e-05	2.437e-05	9.038e-05	1.386e-04
D1 (output stable)	1.531e-05	9.650e-05	1.112e-04	1.487e-04
S0 (output stable)	8.194e-04	8.781e-04	1.615e-03	2.400e-03
D0 to Z	7.188e-04	9.339e-04	2.484e-03	3.359e-03
D1 to Z	7.160e-04	9.272e-04	2.509e-03	3.431e-03
S0 to Z	1.396e-03	1.404e-03	3.078e-03	4.258e-03
	X12_P10			
D0 (output stable)	1.705e-04			
D1 (output stable)	1.638e-04			
S0 (output stable)	2.848e-03			
D0 to Z	4.548e-03			
D1 to Z	4.513e-03			
S0 to Z	5.415e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X1_P10	X2_P10	X6_P10	X9_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

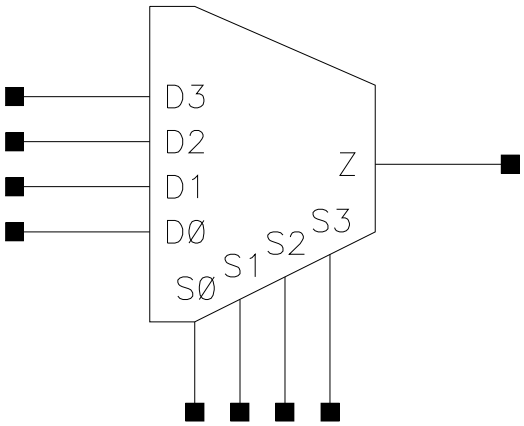
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P10			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.600	0.952	1.5232
X15_P10	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P10	X15_P10
D0	0.0006	0.0015
D1	0.0006	0.0012
D2	0.0006	0.0015
D3	0.0006	0.0012
S0	0.0006	0.0013
S1	0.0006	0.0015
S2	0.0006	0.0013
S3	0.0006	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X15_P10	X4_P10	X15_P10
D0 to Z ↓	0.0430	0.0458	5.3895	1.4256
D0 to Z ↑	0.0350	0.0341	4.5592	1.1560
D1 to Z ↓	0.0394	0.0414	5.3885	1.4249
D1 to Z ↑	0.0304	0.0299	4.5397	1.1508
D2 to Z ↓	0.0418	0.0441	5.4030	1.4288
D2 to Z ↑	0.0341	0.0323	4.5821	1.1624
D3 to Z ↓	0.0378	0.0399	5.3965	1.4268
D3 to Z ↑	0.0294	0.0285	4.5570	1.1567
S0 to Z ↓	0.0410	0.0420	5.3871	1.4245
S0 to Z ↑	0.0373	0.0346	4.5619	1.1552
S1 to Z ↓	0.0370	0.0381	5.3868	1.4239
S1 to Z ↑	0.0323	0.0305	4.5391	1.1499
S2 to Z ↓	0.0403	0.0408	5.4020	1.4272
S2 to Z ↑	0.0364	0.0332	4.5817	1.1624
S3 to Z ↓	0.0368	0.0367	5.3970	1.4250
S3 to Z ↑	0.0318	0.0290	4.5581	1.1570

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	6.199e-07	1.000e-20
X15_P10	1.830e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X15_P10
D0 (output stable)	4.100e-04	1.155e-03
D1 (output stable)	3.026e-04	8.595e-04
D2 (output stable)	4.186e-04	1.156e-03
D3 (output stable)	3.106e-04	8.541e-04
S0 (output stable)	4.074e-04	1.156e-03
S1 (output stable)	3.001e-04	8.694e-04
S2 (output stable)	3.997e-04	1.093e-03
S3 (output stable)	3.013e-04	8.328e-04
D0 to Z	3.032e-03	8.613e-03
D1 to Z	2.552e-03	7.313e-03
D2 to Z	2.755e-03	7.552e-03
D3 to Z	2.286e-03	6.296e-03
S0 to Z	2.908e-03	8.001e-03
S1 to Z	2.440e-03	6.777e-03
S2 to Z	2.655e-03	7.017e-03
S3 to Z	2.195e-03	5.749e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

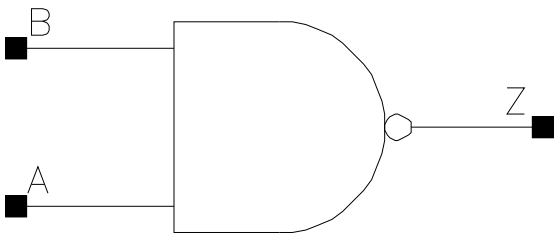
Pin Cycle (vdds)	X4_P10	X15_P10
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P10	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P10	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P10	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P10	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P10	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P10	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P10	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P10	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P10	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P10	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P10	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P10	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P10	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P10	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P10	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P10	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P10	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P10	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P10	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P10	C8T28SOI_LL_-NAND2X4_P10	C8T28SOI_LL_-NAND2X8_P10	C8T28SOI_LL_-NAND2X12_P10
A	0.0004	0.0006	0.0011	0.0016
B	0.0004	0.0005	0.0010	0.0015
	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X24_P10	C8T28SOI_-LLBR0P8_-NAND2X4_P10
A	0.0022	0.0027	0.0007	0.0007
B	0.0020	0.0025	0.0007	0.0006
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	C8T28SOI_-LLBR0P8_-NAND2X12_P10	C8T28SOI_-LLBR0P8_-NAND2X16_P10	C8T28SOI_LLS_-NAND2X8_P10
A	0.0011	0.0017	0.0022	0.0011
B	0.0010	0.0015	0.0019	0.0010
	C8T28SOI_LLS_-NAND2X15_P10	C8T28SOI_LLS_-NAND2X23_P10	C8T28SOI_LLS_-NAND2X31_P10	C8T28SOIDV_LL_-NAND2X9_P10
A	0.0022	0.0034	0.0044	0.0012
B	0.0020	0.0031	0.0041	0.0012
	C8T28SOIDV_LL_-NAND2X18_P10	C8T28SOIDV_LL_-NAND2X27_P10	C8T28SOIDV_LL_-NAND2X36_P10	
A	0.0023	0.0035	0.0047	
B	0.0022	0.0033	0.0044	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND2X2_P10	**C8T28SOI_LL_-NAND2X4_P10**	**C8T28SOI_LL_-NAND2X2_P10**	**C8T28SOI_LL_-NAND2X4_P10**
A to Z ↓	0.0105	0.0092	9.8920	5.4537
A to Z ↑	0.0161	0.0135	9.5402	4.9548
B to Z ↓	0.0119	0.0099	9.9979	5.5157
B to Z ↑	0.0149	0.0118	9.5913	5.0176
	C8T28SOI_LL_-NAND2X8_P10	**C8T28SOI_LL_-NAND2X12_P10**	**C8T28SOI_LL_-NAND2X8_P10**	**C8T28SOI_LL_-NAND2X12_P10**
A to Z ↓	0.0104	0.0100	2.7817	1.9070
A to Z ↑	0.0137	0.0133	2.3549	1.6080
B to Z ↓	0.0092	0.0096	2.8189	1.9322
B to Z ↑	0.0106	0.0109	2.3751	1.6317

	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10
A to Z ↓	0.0102	0.0100	1.4458	1.1682
A to Z ↑	0.0134	0.0133	1.2098	0.9806
B to Z ↓	0.0092	0.0097	1.4668	1.1854
B to Z ↑	0.0104	0.0107	1.2257	0.9945
	C8T28SOI_LL_-NAND2X24_P10	**C8T28SOI_-LLBR0P8_-NAND2X4_P10**	**C8T28SOI_LL_-NAND2X24_P10**	**C8T28SOI_-LLBR0P8_-NAND2X4_P10**
A to Z ↓	0.0365	0.0079	0.6540	3.8654
A to Z ↑	0.0377	0.0170	0.9569	6.3027
B to Z ↓	0.0377	0.0079	0.6542	3.9401
B to Z ↑	0.0360	0.0143	0.9554	6.3426
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	**C8T28SOI_-LLBR0P8_-NAND2X12_P10**	**C8T28SOI_-LLBR0P8_-NAND2X8_P10**	**C8T28SOI_-LLBR0P8_-NAND2X12_P10**
A to Z ↓	0.0089	0.0087	2.1346	1.4628
A to Z ↑	0.0170	0.0170	3.1723	2.1482
B to Z ↓	0.0070	0.0077	2.1791	1.4921
B to Z ↑	0.0124	0.0130	3.1999	2.1655
	C8T28SOI_-LLBR0P8_-NAND2X16_P10	**C8T28SOI_LLS_-NAND2X8_P10**	**C8T28SOI_-LLBR0P8_-NAND2X16_P10**	**C8T28SOI_LLS_-NAND2X8_P10**
A to Z ↓	0.0085	0.0105	1.1173	2.7734
A to Z ↑	0.0165	0.0137	1.6057	2.3871
B to Z ↓	0.0068	0.0092	1.1411	2.8100
B to Z ↑	0.0120	0.0107	1.6264	2.4205
	C8T28SOI_LLS_-NAND2X15_P10	**C8T28SOI_LLS_-NAND2X23_P10**	**C8T28SOI_LLS_-NAND2X15_P10**	**C8T28SOI_LLS_-NAND2X23_P10**
A to Z ↓	0.0103	0.0103	1.4417	0.9735
A to Z ↑	0.0134	0.0133	1.1890	0.7934
B to Z ↓	0.0093	0.0095	1.4631	0.9874
B to Z ↑	0.0104	0.0105	1.1989	0.8006
	C8T28SOI_LLS_-NAND2X31_P10	**C8T28SOIDV_LL_-NAND2X9_P10**	**C8T28SOI_LLS_-NAND2X31_P10**	**C8T28SOIDV_LL_-NAND2X9_P10**
A to Z ↓	0.0103	0.0087	0.7377	2.1313
A to Z ↑	0.0133	0.0140	0.5973	2.3044
B to Z ↓	0.0096	0.0089	0.7481	2.1607
B to Z ↑	0.0105	0.0119	0.6026	2.3485
	C8T28SOIDV_LL_-NAND2X18_P10	**C8T28SOIDV_LL_-NAND2X27_P10**	**C8T28SOIDV_LL_-NAND2X18_P10**	**C8T28SOIDV_LL_-NAND2X27_P10**
A to Z ↓	0.0097	0.0096	1.0883	0.7418
A to Z ↑	0.0144	0.0144	1.1577	0.7815
B to Z ↓	0.0082	0.0090	1.1050	0.7537
B to Z ↑	0.0110	0.0116	1.1677	0.7879
	C8T28SOIDV_LL_-NAND2X36_P10		**C8T28SOIDV_LL_-NAND2X36_P10**	
A to Z ↓	0.0097		0.5588	
A to Z ↑	0.0143		0.5849	
B to Z ↓	0.0084		0.5684	
B to Z ↑	0.0110		0.5906	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P10	7.841e-08	1.000e-20
C8T28SOI_LL_NAND2X4_P10	1.749e-07	1.000e-20
C8T28SOI_LL_NAND2X8_P10	3.480e-07	1.000e-20
C8T28SOI_LL_NAND2X12_P10	5.019e-07	1.000e-20
C8T28SOI_LL_NAND2X15_P10	6.563e-07	1.000e-20
C8T28SOI_LL_NAND2X19_P10	8.109e-07	1.000e-20
C8T28SOI_LL_NAND2X24_P10	1.140e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P10	1.882e-07	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P10	3.369e-07	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_-P10	4.809e-07	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_-P10	6.256e-07	1.000e-20
C8T28SOI_LLS_NAND2X8_P10	3.480e-07	1.000e-20
C8T28SOI_LLS_NAND2X15_P10	6.563e-07	1.000e-20
C8T28SOI_LLS_NAND2X23_P10	9.655e-07	1.000e-20
C8T28SOI_LLS_NAND2X31_P10	1.275e-06	1.000e-20
C8T28SOIDV_LL_NAND2X9_P10	4.310e-07	1.000e-20
C8T28SOIDV_LL_NAND2X18_P10	8.160e-07	1.000e-20
C8T28SOIDV_LL_NAND2X27_P10	1.180e-06	1.000e-20
C8T28SOIDV_LL_NAND2X36_P10	1.545e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P10	C8T28SOI_LL_-NAND2X4_P10	C8T28SOI_LL_-NAND2X8_P10	C8T28SOI_LL_-NAND2X12_P10
A (output stable)	7.167e-06	1.298e-05	4.835e-05	6.719e-05
B (output stable)	2.414e-05	4.471e-05	2.638e-04	2.897e-04
A to Z	4.424e-04	6.592e-04	1.481e-03	2.112e-03
B to Z	3.707e-04	5.206e-04	9.765e-04	1.519e-03
	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X24_P10	C8T28SOI_-LLBR0P8_-NAND2X4_P10
A (output stable)	9.527e-05	1.106e-04	1.532e-05	1.874e-05
B (output stable)	4.696e-04	4.753e-04	4.930e-05	6.356e-05
A to Z	2.846e-03	3.489e-03	7.071e-03	7.607e-04
B to Z	1.913e-03	2.494e-03	6.926e-03	5.592e-04
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	C8T28SOI_-LLBR0P8_-NAND2X12_P10	C8T28SOI_-LLBR0P8_-NAND2X16_P10	C8T28SOI_LLS_-NAND2X8_P10
A (output stable)	6.007e-05	7.764e-05	1.178e-04	4.922e-05
B (output stable)	3.237e-04	3.545e-04	5.719e-04	2.727e-04
A to Z	1.570e-03	2.323e-03	2.942e-03	1.490e-03
B to Z	9.118e-04	1.509e-03	1.727e-03	9.860e-04
	C8T28SOI_LLS_-NAND2X15_P10	C8T28SOI_LLS_-NAND2X23_P10	C8T28SOI_LLS_-NAND2X31_P10	C8T28SOIDV_LL_-NAND2X9_P10
A (output stable)	9.790e-05	1.438e-04	1.839e-04	3.373e-05
B (output stable)	4.737e-04	6.679e-04	8.421e-04	1.152e-04
A to Z	2.880e-03	4.280e-03	5.665e-03	1.557e-03
B to Z	1.941e-03	2.935e-03	3.930e-03	1.193e-03
	C8T28SOIDV_LL_-NAND2X18_P10	C8T28SOIDV_LL_-NAND2X27_P10	C8T28SOIDV_LL_-NAND2X36_P10	
A (output stable)	1.072e-04	1.478e-04	2.148e-04	

B (output stable)	6.107e-04	5.820e-04	1.186e-03	
A to Z	3.286e-03	4.864e-03	6.481e-03	
B to Z	2.139e-03	3.498e-03	4.253e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

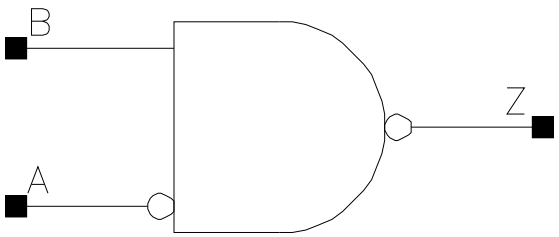
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P10	C8T28SOI_LL_-NAND2X4_P10	C8T28SOI_LL_-NAND2X8_P10	C8T28SOI_LL_-NAND2X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X24_P10	C8T28SOI_-LLBR0P8_-NAND2X4_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	C8T28SOI_-LLBR0P8_-NAND2X12_P10	C8T28SOI_-LLBR0P8_-NAND2X16_P10	C8T28SOI_LLS_-NAND2X8_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P10	C8T28SOI_LLS_-NAND2X23_P10	C8T28SOI_LLS_-NAND2X31_P10	C8T28SOIDV_LL_-NAND2X9_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P10	C8T28SOIDV_LL_-NAND2X27_P10	C8T28SOIDV_LL_-NAND2X36_P10	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.544	0.4352
X4_P10	0.800	0.680	0.5440
X9_P10	1.600	0.544	0.8704
X13_P10	1.600	0.816	1.3056
X17_P10	1.600	0.816	1.3056
X23_P10	0.800	2.312	1.8496
X27_P10	1.600	1.088	1.7408
X31_P10	0.800	2.992	2.3936
X36_P10	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P10	X4_P10	X9_P10	X13_P10
A	0.0006	0.0006	0.0010	0.0009
B	0.0004	0.0005	0.0011	0.0017
	X17_P10	X23_P10	X27_P10	X31_P10
A	0.0009	0.0020	0.0015	0.0027
B	0.0021	0.0030	0.0033	0.0039
	X36_P10			
A	0.0015			
B	0.0043			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X4_P10**	**X2_P10**	**X4_P10**
A to Z ↓	0.0273	0.0283	9.8621	5.4924
A to Z ↑	0.0213	0.0215	9.2989	4.7839
B to Z ↓	0.0122	0.0100	10.1137	5.6311
B to Z ↑	0.0150	0.0118	9.5945	5.0133
	X9_P10	**X13_P10**	**X9_P10**	**X13_P10**
A to Z ↓	0.0278	0.0336	2.1757	1.3785
A to Z ↑	0.0210	0.0253	2.2616	1.5325
B to Z ↓	0.0091	0.0090	2.2408	1.4183
B to Z ↑	0.0119	0.0123	2.3650	1.6230
	X17_P10	**X23_P10**	**X17_P10**	**X23_P10**
A to Z ↓	0.0363	0.0269	1.0896	0.9652
A to Z ↑	0.0263	0.0215	1.1595	0.7903
B to Z ↓	0.0087	0.0093	1.1178	0.9927
B to Z ↑	0.0116	0.0104	1.2338	0.8247
	X27_P10	**X31_P10**	**X27_P10**	**X31_P10**
A to Z ↓	0.0310	0.0266	0.7355	0.7296
A to Z ↑	0.0236	0.0212	0.7700	0.5761
B to Z ↓	0.0085	0.0095	0.7579	0.7503
B to Z ↑	0.0112	0.0106	0.7918	0.6205
	X36_P10		**X36_P10**	
A to Z ↓	0.0356		0.5570	
A to Z ↑	0.0268		0.5779	
B to Z ↓	0.0084		0.5714	
B to Z ↑	0.0109		0.5947	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P10	1.378e-07	1.000e-20
X4_P10	2.433e-07	1.000e-20
X9_P10	6.139e-07	1.000e-20
X13_P10	7.454e-07	1.000e-20
X17_P10	9.627e-07	1.000e-20
X23_P10	1.426e-06	1.000e-20
X27_P10	1.534e-06	1.000e-20
X31_P10	1.873e-06	1.000e-20
X36_P10	1.907e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P10	X4_P10	X9_P10	X13_P10
A (output stable)	6.696e-04	8.538e-04	1.643e-03	2.445e-03
B (output stable)	2.454e-05	4.523e-05	1.184e-04	2.984e-04
A to Z	1.145e-03	1.555e-03	3.325e-03	5.258e-03
B to Z	3.741e-04	5.167e-04	1.212e-03	1.852e-03
	X17_P10	X23_P10	X27_P10	X31_P10
A (output stable)	2.754e-03	4.340e-03	4.332e-03	5.672e-03
B (output stable)	3.572e-04	6.098e-04	5.870e-04	8.110e-04
A to Z	6.212e-03	8.878e-03	9.237e-03	1.174e-02
B to Z	2.254e-03	2.928e-03	3.278e-03	3.883e-03
	X36_P10			
A (output stable)	5.749e-03			

B (output stable)	8.972e-04			
A to Z	1.222e-02			
B to Z	4.195e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

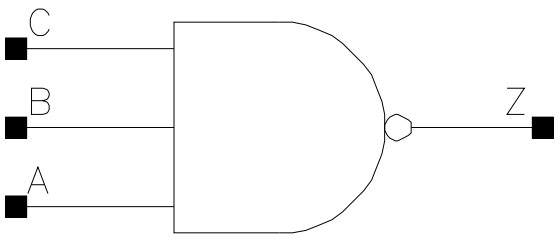
Pin Cycle (vdds)	X2_P10	X4_P10	X9_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P10	X23_P10	X27_P10	X31_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P10	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P10	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P10	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P10	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P10	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P10	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P10	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P10	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P10	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P10	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P10	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P10	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P10	C8T28SOI_LL_-NAND3X7_P10	C8T28SOI_LL_-NAND3X10_P10	C8T28SOI_LL_-NAND3X14_P10
A	0.0006	0.0011	0.0017	0.0022
B	0.0005	0.0011	0.0016	0.0021
C	0.0006	0.0010	0.0015	0.0020
	C8T28SOI_LL_-NAND3X20_P10	C8T28SOI_LL_-NAND3X27_P10	C8T28SOI_-LLBR0P6_-NAND3X3_P10	C8T28SOI_-LLBR0P6_-NAND3X7_P10
A	0.0033	0.0044	0.0007	0.0012
B	0.0031	0.0042	0.0006	0.0011
C	0.0029	0.0040	0.0006	0.0010
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	C8T28SOI_-LLBR0P6_-NAND3X14_P10	C8T28SOI_-LLBR0P6_-NAND3X20_P10	C8T28SOI_-LLBR0P6_-NAND3X27_P10
A	0.0017	0.0022	0.0033	0.0044
B	0.0015	0.0020	0.0030	0.0040
C	0.0015	0.0020	0.0029	0.0039

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND3X3_P10	**C8T28SOI_LL_-NAND3X7_P10**	**C8T28SOI_LL_-NAND3X3_P10**	**C8T28SOI_LL_-NAND3X7_P10**
A to Z ↓	0.0136	0.0156	7.9142	4.0078
A to Z ↑	0.0167	0.0172	5.0016	2.4469
B to Z ↓	0.0141	0.0151	7.9496	4.0248
B to Z ↑	0.0154	0.0157	5.0273	2.4521
C to Z ↓	0.0143	0.0135	7.9979	4.0475
C to Z ↑	0.0138	0.0128	5.0716	2.3744
	C8T28SOI_LL_-NAND3X10_P10	**C8T28SOI_LL_-NAND3X14_P10**	**C8T28SOI_LL_-NAND3X10_P10**	**C8T28SOI_LL_-NAND3X14_P10**
A to Z ↓	0.0148	0.0152	2.7668	2.0909
A to Z ↑	0.0163	0.0167	1.5739	1.2318
B to Z ↓	0.0149	0.0147	2.7790	2.1001
B to Z ↑	0.0149	0.0150	1.6270	1.2320
C to Z ↓	0.0135	0.0134	2.7969	2.1139
C to Z ↑	0.0126	0.0125	1.6396	1.2215
	C8T28SOI_LL_-NAND3X20_P10	**C8T28SOI_LL_-NAND3X27_P10**	**C8T28SOI_LL_-NAND3X20_P10**	**C8T28SOI_LL_-NAND3X27_P10**
A to Z ↓	0.0148	0.0149	1.4235	1.0832
A to Z ↑	0.0161	0.0161	0.7927	0.5983
B to Z ↓	0.0148	0.0149	1.4298	1.0879
B to Z ↑	0.0146	0.0146	0.7936	0.5974
C to Z ↓	0.0133	0.0135	1.4394	1.0953
C to Z ↑	0.0121	0.0122	0.8180	0.6163
	C8T28SOI_-LLBR0P6_-NAND3X3_P10	**C8T28SOI_-LLBR0P6_-NAND3X7_P10**	**C8T28SOI_-LLBR0P6_-NAND3X3_P10**	**C8T28SOI_-LLBR0P6_-NAND3X7_P10**
A to Z ↓	0.0105	0.0128	4.9867	2.8124
A to Z ↑	0.0230	0.0247	7.4757	3.8144
B to Z ↓	0.0102	0.0118	5.0416	2.8347
B to Z ↑	0.0202	0.0213	7.4942	3.8262

C to Z ↓	0.0096	0.0096	5.1138	2.8707
C to Z ↑	0.0167	0.0163	7.5556	3.7938
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	**C8T28SOI_-LLBR0P6_-NAND3X14_P10**	**C8T28SOI_-LLBR0P6_-NAND3X10_P10**	**C8T28SOI_-LLBR0P6_-NAND3X14_P10**
A to Z ↓	0.0118	0.0125	1.8776	1.4288
A to Z ↑	0.0233	0.0239	2.5415	1.9261
B to Z ↓	0.0110	0.0112	1.8965	1.4413
B to Z ↑	0.0199	0.0203	2.5529	1.9316
C to Z ↓	0.0091	0.0088	1.9225	1.4630
C to Z ↑	0.0154	0.0152	2.5752	1.9299
	C8T28SOI_-LLBR0P6_-NAND3X20_P10	**C8T28SOI_-LLBR0P6_-NAND3X27_P10**	**C8T28SOI_-LLBR0P6_-NAND3X20_P10**	**C8T28SOI_-LLBR0P6_-NAND3X27_P10**
A to Z ↓	0.0120	0.0120	0.9663	0.7414
A to Z ↑	0.0234	0.0233	1.2811	0.9664
B to Z ↓	0.0111	0.0111	0.9754	0.7483
B to Z ↑	0.0200	0.0198	1.2838	0.9661
C to Z ↓	0.0087	0.0089	0.9899	0.7591
C to Z ↑	0.0148	0.0148	1.2944	0.9735

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P10	1.514e-07	1.000e-20
C8T28SOI_LL_NAND3X7_P10	3.172e-07	1.000e-20
C8T28SOI_LL_NAND3X10_P10	4.421e-07	1.000e-20
C8T28SOI_LL_NAND3X14_P10	5.956e-07	1.000e-20
C8T28SOI_LL_NAND3X20_P10	8.756e-07	1.000e-20
C8T28SOI_LL_NAND3X27_P10	1.154e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P10	1.664e-07	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P10	3.236e-07	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_-P10	4.366e-07	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_-P10	5.942e-07	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_-P10	8.669e-07	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_-P10	1.137e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P10	C8T28SOI_LL_-NAND3X7_P10	C8T28SOI_LL_-NAND3X10_P10	C8T28SOI_LL_-NAND3X14_P10
A (output stable)	9.591e-06	3.743e-05	4.342e-05	6.656e-05
B (output stable)	4.457e-05	1.468e-04	2.054e-04	2.728e-04
C (output stable)	5.607e-05	1.663e-04	2.134e-04	2.996e-04
A to Z	1.003e-03	2.285e-03	3.166e-03	4.310e-03
B to Z	8.519e-04	1.850e-03	2.559e-03	3.458e-03
C to Z	7.099e-04	1.385e-03	1.935e-03	2.597e-03
	C8T28SOI_LL_-NAND3X20_P10	C8T28SOI_LL_-NAND3X27_P10	C8T28SOI_-LLBR0P6_-NAND3X3_P10	C8T28SOI_-LLBR0P6_-NAND3X7_P10

A (output stable)	8.798e-05	1.163e-04	1.508e-05	5.023e-05
B (output stable)	3.939e-04	5.282e-04	7.124e-05	1.994e-04
C (output stable)	4.537e-04	5.777e-04	9.029e-05	2.483e-04
A to Z	6.247e-03	8.297e-03	1.113e-03	2.554e-03
B to Z	5.056e-03	6.698e-03	8.753e-04	1.930e-03
C to Z	3.696e-03	4.934e-03	6.295e-04	1.247e-03
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	C8T28SOI_-LLBR0P6_-NAND3X14_P10	C8T28SOI_-LLBR0P6_-NAND3X20_P10	C8T28SOI_-LLBR0P6_-NAND3X27_P10
A (output stable)	5.844e-05	9.568e-05	1.192e-04	1.614e-04
B (output stable)	2.769e-04	3.989e-04	5.643e-04	7.494e-04
C (output stable)	3.103e-04	4.397e-04	6.537e-04	8.454e-04
A to Z	3.455e-03	4.809e-03	6.918e-03	9.142e-03
B to Z	2.530e-03	3.500e-03	5.051e-03	6.651e-03
C to Z	1.657e-03	2.175e-03	3.106e-03	4.116e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

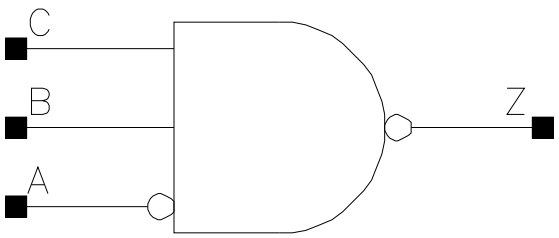
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P10	C8T28SOI_LL_-NAND3X7_P10	C8T28SOI_LL_-NAND3X10_P10	C8T28SOI_LL_-NAND3X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P10	C8T28SOI_LL_-NAND3X27_P10	C8T28SOI_-LLBR0P6_-NAND3X3_P10	C8T28SOI_-LLBR0P6_-NAND3X7_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	C8T28SOI_-LLBR0P6_-NAND3X14_P10	C8T28SOI_-LLBR0P6_-NAND3X20_P10	C8T28SOI_-LLBR0P6_-NAND3X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X7_P10	0.800	1.360	1.0880
X10_P10	0.800	1.632	1.3056
X14_P10	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X10_P10	X14_P10
A	0.0007	0.0010	0.0008	0.0008
B	0.0005	0.0011	0.0016	0.0021
C	0.0006	0.0010	0.0015	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0340	0.0331	7.9117	4.0247
A to Z ↑	0.0242	0.0246	4.7953	2.3099
B to Z ↓	0.0137	0.0148	8.0043	4.0649
B to Z ↑	0.0150	0.0151	5.0346	2.3812
C to Z ↓	0.0139	0.0130	8.0544	4.0877
C to Z ↑	0.0133	0.0123	5.0795	2.3787
	X10_P10	**X14_P10**	**X10_P10**	**X14_P10**
A to Z ↓	0.0365	0.0395	2.7545	2.0993

A to Z ↑	0.0274	0.0300	1.5833	1.1833
B to Z ↓	0.0148	0.0144	2.7778	2.1160
B to Z ↑	0.0148	0.0146	1.6290	1.2180
C to Z ↓	0.0134	0.0130	2.7954	2.1292
C to Z ↑	0.0125	0.0119	1.6440	1.2234

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.119e-07	1.000e-20
X7_P10	4.739e-07	1.000e-20
X10_P10	6.013e-07	1.000e-20
X14_P10	7.567e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	8.649e-04	1.574e-03	2.027e-03	2.496e-03
B (output stable)	2.213e-05	6.276e-05	1.055e-04	1.301e-04
C (output stable)	6.103e-05	2.159e-04	2.605e-04	3.690e-04
A to Z	1.876e-03	3.961e-03	5.546e-03	7.094e-03
B to Z	8.088e-04	1.765e-03	2.551e-03	3.319e-03
C to Z	6.625e-04	1.282e-03	1.921e-03	2.434e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

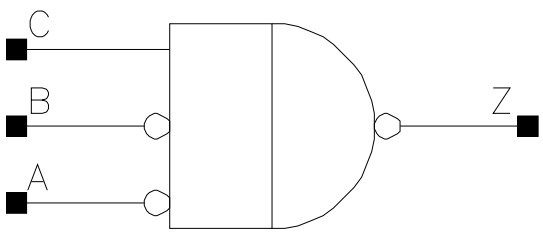
Pin Cycle (vdds)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	0.816	0.6528
X8_P10	0.800	1.088	0.8704
X12_P10	0.800	1.632	1.3056
X15_P10	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X12_P10	X15_P10
A	0.0007	0.0007	0.0013	0.0012
B	0.0008	0.0007	0.0013	0.0012
C	0.0006	0.0010	0.0015	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0303	0.0373	5.1543	2.7601
A to Z ↑	0.0208	0.0241	4.5725	2.2826
B to Z ↓	0.0308	0.0379	5.1572	2.7608
B to Z ↑	0.0195	0.0229	4.5701	2.2826
C to Z ↓	0.0101	0.0093	5.2716	2.8120
C to Z ↑	0.0119	0.0108	4.6524	2.3977
	X12_P10	**X15_P10**	**X12_P10**	**X15_P10**
A to Z ↓	0.0341	0.0375	1.8841	1.4380
A to Z ↑	0.0221	0.0260	1.5231	1.1476
B to Z ↓	0.0324	0.0361	1.8840	1.4385

B to Z ↑	0.0201	0.0239	1.5194	1.1460
C to Z ↓	0.0101	0.0093	1.9255	1.4699
C to Z ↑	0.0113	0.0103	1.6292	1.1959

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	3.410e-07	1.000e-20
X8_P10	4.561e-07	1.000e-20
X12_P10	7.271e-07	1.000e-20
X15_P10	8.051e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	4.743e-04	6.559e-04	1.100e-03	1.272e-03
B (output stable)	3.938e-04	5.671e-04	8.424e-04	1.017e-03
C (output stable)	4.846e-05	2.074e-04	2.531e-04	3.592e-04
A to Z	2.161e-03	3.570e-03	5.625e-03	6.808e-03
B to Z	1.958e-03	3.366e-03	4.937e-03	6.166e-03
C to Z	5.844e-04	1.007e-03	1.642e-03	1.950e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

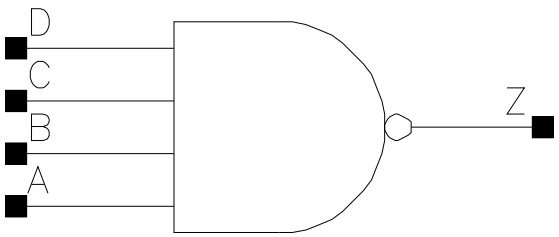
Pin Cycle (vdds)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.224	0.9792
X10_P10	0.800	1.360	1.0880
X14_P10	0.800	1.904	1.5232
X18_P10	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X18_P10
A	0.0005	0.0005	0.0005	0.0006
B	0.0005	0.0005	0.0006	0.0008
C	0.0004	0.0004	0.0005	0.0007
D	0.0005	0.0005	0.0006	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0489	0.0459	3.1332	1.5811
A to Z ↑	0.0401	0.0412	4.6074	2.3378
B to Z ↓	0.0508	0.0481	3.1329	1.5798
B to Z ↑	0.0388	0.0406	4.6125	2.3382
C to Z ↓	0.0503	0.0467	3.1314	1.5807
C to Z ↑	0.0417	0.0434	4.6102	2.3369

D to Z ↓	0.0527	0.0491	3.1308	1.5809
D to Z ↑	0.0412	0.0430	4.6019	2.3375
	X14_P10	**X18_P10**	**X14_P10**	**X18_P10**
A to Z ↓	0.0493	0.0462	1.0939	0.8809
A to Z ↑	0.0411	0.0401	1.6062	1.2702
B to Z ↓	0.0515	0.0480	1.0936	0.8808
B to Z ↑	0.0398	0.0392	1.6060	1.2704
C to Z ↓	0.0473	0.0424	1.0924	0.8806
C to Z ↑	0.0416	0.0394	1.6032	1.2686
D to Z ↓	0.0495	0.0440	1.0926	0.8803
D to Z ↑	0.0408	0.0380	1.6016	1.2689

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	3.540e-07	1.000e-20
X10_P10	5.424e-07	1.000e-20
X14_P10	7.864e-07	1.000e-20
X18_P10	1.010e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	3.476e-04	4.234e-04	6.259e-04	6.873e-04
B (output stable)	3.271e-04	4.022e-04	5.965e-04	6.549e-04
C (output stable)	3.735e-04	4.191e-04	6.433e-04	6.336e-04
D (output stable)	3.508e-04	3.973e-04	5.905e-04	5.785e-04
A to Z	2.593e-03	3.698e-03	5.749e-03	6.707e-03
B to Z	2.522e-03	3.627e-03	5.647e-03	6.594e-03
C to Z	2.729e-03	3.752e-03	5.433e-03	6.194e-03
D to Z	2.671e-03	3.684e-03	5.334e-03	6.064e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

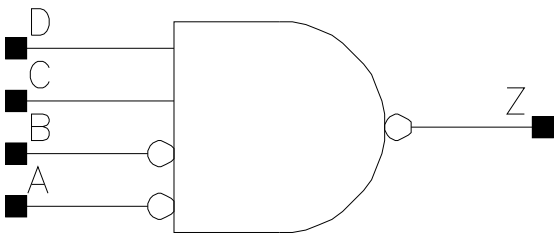
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.952	0.7616
X7_P10	0.800	1.360	1.0880
X10_P10	0.800	2.040	1.6320
X14_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P10	X7_P10	X10_P10	X14_P10
A	0.0007	0.0007	0.0013	0.0012
B	0.0007	0.0007	0.0014	0.0013
C	0.0007	0.0011	0.0016	0.0021
D	0.0005	0.0010	0.0015	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X7_P10	X3_P10	X7_P10
A to Z ↓	0.0348	0.0408	7.5933	4.0272
A to Z ↑	0.0226	0.0260	4.6319	2.3203
B to Z ↓	0.0347	0.0412	7.5972	4.0274
B to Z ↑	0.0211	0.0245	4.6334	2.3200
C to Z ↓	0.0141	0.0147	7.6903	4.0566
C to Z ↑	0.0154	0.0150	4.8067	2.3853

D to Z ↓	0.0138	0.0129	7.7240	4.0794
D to Z ↑	0.0133	0.0122	4.8075	2.3795
	X10_P10	**X14_P10**	**X10_P10**	**X14_P10**
A to Z ↓	0.0385	0.0420	2.7515	2.1053
A to Z ↑	0.0239	0.0296	1.5663	1.1569
B to Z ↓	0.0368	0.0411	2.7521	2.1050
B to Z ↑	0.0219	0.0278	1.5638	1.1547
C to Z ↓	0.0147	0.0144	2.7737	2.1193
C to Z ↑	0.0149	0.0146	1.6304	1.2197
D to Z ↓	0.0134	0.0130	2.7913	2.1326
D to Z ↑	0.0125	0.0120	1.6445	1.2254

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	3.117e-07	1.000e-20
X7_P10	4.108e-07	1.000e-20
X10_P10	6.759e-07	1.000e-20
X14_P10	7.265e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	5.767e-04	7.889e-04	1.396e-03	1.638e-03
B (output stable)	4.815e-04	6.984e-04	1.091e-03	1.367e-03
C (output stable)	7.027e-05	1.156e-04	1.769e-04	2.296e-04
D (output stable)	7.510e-05	2.045e-04	2.635e-04	3.473e-04
A to Z	2.547e-03	4.190e-03	6.591e-03	8.333e-03
B to Z	2.351e-03	3.996e-03	5.922e-03	7.732e-03
C to Z	8.698e-04	1.754e-03	2.522e-03	3.315e-03
D to Z	7.231e-04	1.270e-03	1.902e-03	2.452e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

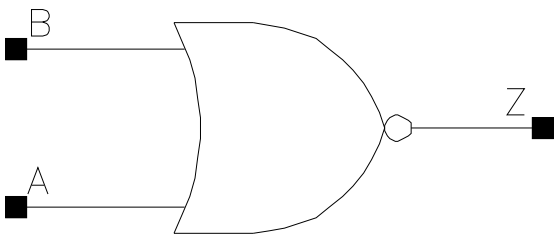
Pin Cycle (vdds)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.408	0.3264
X4_P10	0.800	0.408	0.3264
X8_P10	0.800	0.680	0.5440
X9_P10	1.600	0.408	0.6528
X12_P10	0.800	0.952	0.7616
X16_P10	0.800	1.224	0.9792
X19_P10	1.600	0.680	1.0880
X20_P10	0.800	1.496	1.1968
X23_P10	0.800	1.496	1.1968
X24_P10	0.800	1.768	1.4144
X27_P10	0.800	1.632	1.3056
X29_P10	1.600	0.952	1.5232
X31_P10	0.800	2.312	1.8496
X34_P10	0.800	2.040	1.6320
X38_P10	0.800	2.176	1.7408
X39_P10	1.600	1.224	1.9584
X46_P10	1.600	1.224	1.9584
X57_P10	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P10	X4_P10	X8_P10	X9_P10
A	0.0004	0.0006	0.0011	0.0012
B	0.0004	0.0005	0.0010	0.0011
	X12_P10	X16_P10	X19_P10	X20_P10

A	0.0017	0.0022	0.0024	0.0028
B	0.0015	0.0020	0.0022	0.0024
	X23_P10	X24_P10	X27_P10	X29_P10
A	0.0008	0.0033	0.0008	0.0036
B	0.0007	0.0030	0.0007	0.0033
	X31_P10	X34_P10	X38_P10	X39_P10
A	0.0044	0.0008	0.0008	0.0048
B	0.0041	0.0007	0.0007	0.0044
	X46_P10	X57_P10		
A	0.0007	0.0007		
B	0.0008	0.0008		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X4_P10**	**X2_P10**	**X4_P10**
A to Z ↓	0.0101	0.0096	6.0950	3.3512
A to Z ↑	0.0185	0.0165	18.0177	9.6976
B to Z ↓	0.0090	0.0081	6.1384	3.3812
B to Z ↑	0.0187	0.0162	18.1037	9.7351
	X8_P10	**X9_P10**	**X8_P10**	**X9_P10**
A to Z ↓	0.0090	0.0082	1.6178	1.2846
A to Z ↑	0.0160	0.0153	4.5898	4.3810
B to Z ↓	0.0064	0.0068	1.6206	1.3324
B to Z ↑	0.0127	0.0148	4.6190	4.4048
	X12_P10	**X16_P10**	**X12_P10**	**X16_P10**
A to Z ↓	0.0092	0.0092	1.1104	0.8255
A to Z ↑	0.0155	0.0159	3.0135	2.3028
B to Z ↓	0.0069	0.0067	1.1219	0.8349
B to Z ↑	0.0131	0.0129	3.0333	2.3185
	X19_P10	**X20_P10**	**X19_P10**	**X20_P10**
A to Z ↓	0.0089	0.0094	0.6498	0.6791
A to Z ↑	0.0173	0.0156	2.2426	1.8282
B to Z ↓	0.0069	0.0070	0.6571	0.6868
B to Z ↑	0.0148	0.0132	2.2552	1.8408
	X23_P10	**X24_P10**	**X23_P10**	**X24_P10**
A to Z ↓	0.0334	0.0092	0.6850	0.5621
A to Z ↑	0.0459	0.0157	0.9659	1.5418
B to Z ↓	0.0316	0.0067	0.6844	0.5692
B to Z ↑	0.0459	0.0128	0.9669	1.5531
	X27_P10	**X29_P10**	**X27_P10**	**X29_P10**
A to Z ↓	0.0349	0.0085	0.5714	0.4300
A to Z ↑	0.0473	0.0163	0.8073	1.5065
B to Z ↓	0.0331	0.0066	0.5707	0.4343
B to Z ↑	0.0474	0.0143	0.8072	1.5151
	X31_P10	**X34_P10**	**X31_P10**	**X34_P10**
A to Z ↓	0.0093	0.0366	0.4190	0.4686
A to Z ↑	0.0158	0.0535	1.1564	0.6597
B to Z ↓	0.0070	0.0349	0.4248	0.4687
B to Z ↑	0.0130	0.0539	1.1651	0.6602
	X38_P10	**X39_P10**	**X38_P10**	**X39_P10**
A to Z ↓	0.0372	0.0087	0.4083	0.3281
A to Z ↑	0.0539	0.0167	0.5786	1.1307

B to Z ↓	0.0355	0.0067	0.4084	0.3323
B to Z ↑	0.0542	0.0141	0.5786	1.1367
	X46_P10	**X57_P10**	**X46_P10**	**X57_P10**
A to Z ↓	0.0419	0.0453	0.3118	0.2558
A to Z ↑	0.0554	0.0579	0.5746	0.4628
B to Z ↓	0.0406	0.0439	0.3114	0.2556
B to Z ↑	0.0566	0.0591	0.5746	0.4627

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P10	7.958e-08	1.000e-20
X4_P10	1.732e-07	1.000e-20
X8_P10	3.578e-07	1.000e-20
X9_P10	4.365e-07	1.000e-20
X12_P10	5.175e-07	1.000e-20
X16_P10	6.777e-07	1.000e-20
X19_P10	8.317e-07	1.000e-20
X20_P10	8.380e-07	1.000e-20
X23_P10	1.210e-06	1.000e-20
X24_P10	9.984e-07	1.000e-20
X27_P10	1.367e-06	1.000e-20
X29_P10	1.206e-06	1.000e-20
X31_P10	1.319e-06	1.000e-20
X34_P10	1.727e-06	1.000e-20
X38_P10	1.886e-06	1.000e-20
X39_P10	1.582e-06	1.000e-20
X46_P10	2.041e-06	1.000e-20
X57_P10	2.395e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P10	X4_P10	X8_P10	X9_P10
A (output stable)	1.508e-05	2.552e-05	9.630e-05	5.564e-05
B (output stable)	3.877e-06	7.003e-06	5.327e-05	1.730e-05
A to Z	4.638e-04	7.581e-04	1.525e-03	1.535e-03
B to Z	3.621e-04	5.677e-04	8.799e-04	1.152e-03
	X12_P10	X16_P10	X19_P10	X20_P10
A (output stable)	1.368e-04	1.921e-04	2.033e-04	2.277e-04
B (output stable)	7.261e-05	9.560e-05	1.174e-04	1.114e-04
A to Z	2.245e-03	3.034e-03	3.460e-03	3.759e-03
B to Z	1.410e-03	1.818e-03	2.311e-03	2.368e-03
	X23_P10	X24_P10	X27_P10	X29_P10
A (output stable)	2.761e-05	2.826e-04	2.772e-05	2.668e-04
B (output stable)	7.670e-06	1.297e-04	7.773e-06	1.347e-04
A to Z	7.008e-03	4.484e-03	7.821e-03	4.813e-03
B to Z	6.814e-03	2.723e-03	7.630e-03	3.240e-03
	X31_P10	X34_P10	X38_P10	X39_P10
A (output stable)	3.810e-04	2.923e-05	2.931e-05	4.011e-04
B (output stable)	1.767e-04	8.505e-06	8.607e-06	1.986e-04
A to Z	5.974e-03	1.049e-02	1.125e-02	6.577e-03
B to Z	3.681e-03	1.027e-02	1.103e-02	4.300e-03
	X46_P10	X57_P10		

A (output stable)	2.985e-05	3.004e-05		
B (output stable)	1.016e-05	1.034e-05		
A to Z	1.222e-02	1.482e-02		
B to Z	1.204e-02	1.463e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

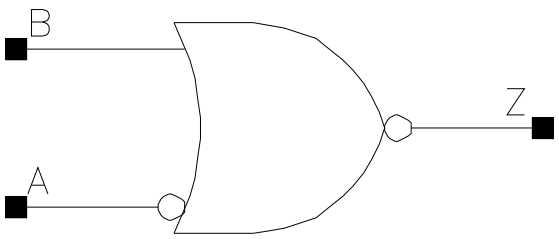
Pin Cycle (vdds)	X2_P10	X4_P10	X8_P10	X9_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P10	X16_P10	X19_P10	X20_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P10	X24_P10	X27_P10	X29_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P10	X34_P10	X38_P10	X39_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P10	X57_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.544	0.4352
X3_P10	0.800	0.544	0.4352
X4_P10	0.800	0.544	0.4352
X10_P10	1.600	0.544	0.8704
X14_P10	1.600	0.816	1.3056
X19_P10	1.600	0.816	1.3056
X29_P10	1.600	1.088	1.7408
X39_P10	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P10	X3_P10	X4_P10	X10_P10
A	0.0006	0.0006	0.0006	0.0010
B	0.0004	0.0004	0.0005	0.0011
	X14_P10	X19_P10	X29_P10	X39_P10
A	0.0010	0.0010	0.0015	0.0015
B	0.0017	0.0021	0.0033	0.0043

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X3_P10**	**X2_P10**	**X3_P10**
A to Z ↓	0.0263	0.0266	5.8786	4.4644
A to Z ↑	0.0244	0.0243	17.8962	15.1337
B to Z ↓	0.0088	0.0078	6.1839	4.6828

B to Z ↑	0.0179	0.0170	18.0965	15.2695
	X4_P10	**X10_P10**	**X4_P10**	**X10_P10**
A to Z ↓	0.0274	0.0271	3.4441	1.2523
A to Z ↑	0.0241	0.0235	10.9148	4.3183
B to Z ↓	0.0074	0.0069	3.6098	1.2716
B to Z ↑	0.0153	0.0152	11.0359	4.3659
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0326	0.0345	0.7894	0.6183
A to Z ↑	0.0271	0.0279	2.9449	2.1687
B to Z ↓	0.0065	0.0062	0.8813	0.6919
B to Z ↑	0.0143	0.0132	2.9817	2.1964
	X29_P10	**X39_P10**	**X29_P10**	**X39_P10**
A to Z ↓	0.0299	0.0345	0.4160	0.3131
A to Z ↑	0.0265	0.0286	1.5024	1.1052
B to Z ↓	0.0065	0.0061	0.4355	0.3420
B to Z ↑	0.0141	0.0129	1.5210	1.1189

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P10	1.412e-07	1.000e-20
X3_P10	1.687e-07	1.000e-20
X4_P10	2.205e-07	1.000e-20
X10_P10	6.349e-07	1.000e-20
X14_P10	7.579e-07	1.000e-20
X19_P10	1.018e-06	1.000e-20
X29_P10	1.562e-06	1.000e-20
X39_P10	1.958e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P10	X3_P10	X4_P10	X10_P10
A (output stable)	6.714e-04	7.339e-04	8.250e-04	1.687e-03
B (output stable)	9.469e-06	1.290e-05	2.179e-05	6.339e-05
A to Z	1.161e-03	1.281e-03	1.491e-03	3.395e-03
B to Z	3.387e-04	3.800e-04	4.511e-04	1.212e-03
	X14_P10	X19_P10	X29_P10	X39_P10
A (output stable)	2.540e-03	2.881e-03	4.353e-03	5.707e-03
B (output stable)	8.459e-05	1.317e-04	2.409e-04	2.593e-04
A to Z	4.979e-03	5.944e-03	9.467e-03	1.181e-02
B to Z	1.602e-03	1.934e-03	3.199e-03	3.791e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P10	X3_P10	X4_P10	X10_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P10	X19_P10	X29_P10	X39_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

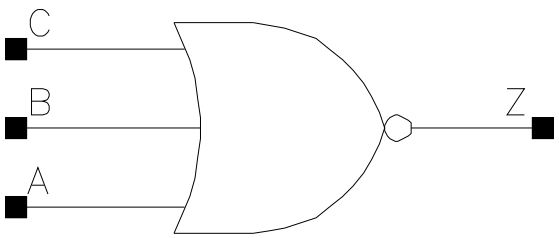
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.544	0.4352
X7_P10	0.800	0.952	0.7616
X11_P10	0.800	1.360	1.0880
X14_P10	0.800	1.768	1.4144
X21_P10	0.800	2.584	2.0672
X29_P10	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X11_P10	X14_P10
A	0.0006	0.0010	0.0017	0.0023
B	0.0006	0.0012	0.0016	0.0023
C	0.0006	0.0010	0.0015	0.0020
	X21_P10	X29_P10		
A	0.0035	0.0046		
B	0.0034	0.0046		
C	0.0030	0.0040		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0109	0.0110	3.4056	1.7877
A to Z ↑	0.0218	0.0227	13.5774	7.0011

B to Z ↓	0.0102	0.0101	3.4319	1.7175
B to Z ↑	0.0208	0.0225	13.6065	7.0167
C to Z ↓	0.0088	0.0074	3.4750	1.7395
C to Z ↑	0.0191	0.0161	13.6543	7.0358
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0110	0.0110	1.1208	0.8613
A to Z ↑	0.0230	0.0224	4.6177	3.3581
B to Z ↓	0.0103	0.0101	1.1326	0.8370
B to Z ↑	0.0211	0.0219	4.6273	3.3635
C to Z ↓	0.0080	0.0077	1.1315	0.8518
C to Z ↑	0.0176	0.0164	4.6400	3.3760
	X21_P10	**X29_P10**	**X21_P10**	**X29_P10**
A to Z ↓	0.0110	0.0111	0.5735	0.4307
A to Z ↑	0.0223	0.0224	2.2544	1.6953
B to Z ↓	0.0102	0.0103	0.5631	0.4262
B to Z ↑	0.0216	0.0217	2.2579	1.6980
C to Z ↓	0.0079	0.0079	0.5749	0.4343
C to Z ↑	0.0165	0.0166	2.2658	1.7043

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	1.620e-07	1.000e-20
X7_P10	3.136e-07	1.000e-20
X11_P10	4.815e-07	1.000e-20
X14_P10	6.477e-07	1.000e-20
X21_P10	9.567e-07	1.000e-20
X29_P10	1.269e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	8.988e-05	2.544e-04	3.949e-04	5.091e-04
B (output stable)	-9.465e-06	6.417e-05	2.289e-06	9.939e-05
C (output stable)	5.039e-06	2.987e-05	3.180e-05	5.982e-05
A to Z	1.014e-03	2.066e-03	3.258e-03	4.254e-03
B to Z	8.155e-04	1.718e-03	2.464e-03	3.515e-03
C to Z	6.135e-04	1.004e-03	1.726e-03	2.134e-03
	X21_P10	X29_P10		
A (output stable)	7.370e-04	9.776e-04		
B (output stable)	1.284e-04	1.689e-04		
C (output stable)	9.048e-05	1.246e-04		
A to Z	6.303e-03	8.400e-03		
B to Z	5.154e-03	6.878e-03		
C to Z	3.199e-03	4.284e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

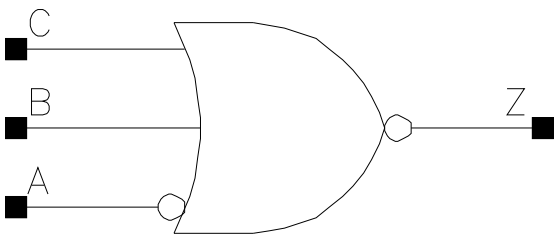
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P10	X29_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X7_P10	0.800	1.360	1.0880
X11_P10	0.800	1.632	1.3056
X14_P10	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X11_P10	X14_P10
A	0.0007	0.0007	0.0010	0.0014
B	0.0006	0.0011	0.0016	0.0021
C	0.0006	0.0010	0.0015	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0294	0.0265	3.2616	1.5352
A to Z ↑	0.0317	0.0318	13.6159	6.6584
B to Z ↓	0.0102	0.0102	3.4469	1.6310
B to Z ↑	0.0207	0.0221	13.6940	6.6891
C to Z ↓	0.0088	0.0077	3.4829	1.6459
C to Z ↑	0.0191	0.0169	13.7449	6.7083
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0322	0.0257	1.0873	0.8029

A to Z ↑	0.0356	0.0312	4.6216	3.4054
B to Z ↓	0.0102	0.0100	1.1339	0.8459
B to Z ↑	0.0209	0.0212	4.6434	3.4237
C to Z ↓	0.0079	0.0077	1.1339	0.8567
C to Z ↑	0.0173	0.0165	4.6568	3.4354

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.285e-07	1.000e-20
X7_P10	5.232e-07	1.000e-20
X11_P10	6.348e-07	1.000e-20
X14_P10	9.499e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	9.528e-04	1.807e-03	2.404e-03	3.310e-03
B (output stable)	5.753e-06	4.440e-05	5.077e-05	9.776e-05
C (output stable)	1.082e-05	5.605e-05	5.968e-05	9.721e-05
A to Z	1.954e-03	4.064e-03	5.572e-03	7.641e-03
B to Z	8.075e-04	1.785e-03	2.457e-03	3.340e-03
C to Z	6.067e-04	1.130e-03	1.679e-03	2.129e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

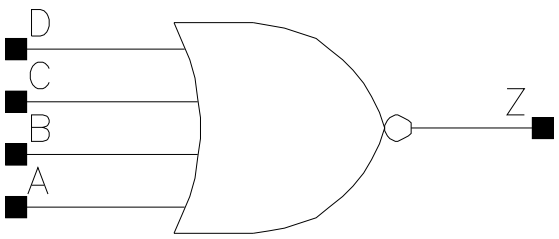
Pin Cycle (vdds)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.224	0.9792
X10_P10	0.800	1.632	1.3056
X14_P10	0.800	1.904	1.5232
X18_P10	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X18_P10
A	0.0005	0.0004	0.0005	0.0006
B	0.0005	0.0006	0.0007	0.0007
C	0.0005	0.0005	0.0005	0.0007
D	0.0006	0.0005	0.0006	0.0006

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0322	0.0365	3.2386	1.5547
A to Z ↑	0.0515	0.0578	4.8607	2.3368
B to Z ↓	0.0312	0.0366	3.2389	1.5546
B to Z ↑	0.0522	0.0605	4.8645	2.3378
C to Z ↓	0.0329	0.0371	3.2370	1.5513
C to Z ↑	0.0546	0.0623	4.8659	2.3387

D to Z ↓	0.0326	0.0358	3.2310	1.5514
D to Z ↑	0.0563	0.0628	4.8648	2.3382
	X14_P10	**X18_P10**	**X14_P10**	**X18_P10**
A to Z ↓	0.0354	0.0368	1.0739	0.8494
A to Z ↑	0.0534	0.0520	1.6120	1.2117
B to Z ↓	0.0348	0.0355	1.0742	0.8499
B to Z ↑	0.0550	0.0526	1.6127	1.2133
C to Z ↓	0.0344	0.0366	1.0702	0.8475
C to Z ↑	0.0533	0.0526	1.6108	1.2125
D to Z ↓	0.0333	0.0351	1.0700	0.8475
D to Z ↑	0.0542	0.0531	1.6098	1.2107

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	4.228e-07	1.000e-20
X10_P10	6.311e-07	1.000e-20
X14_P10	9.384e-07	1.000e-20
X18_P10	1.230e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	3.742e-04	4.901e-04	6.091e-04	7.532e-04
B (output stable)	3.235e-04	4.495e-04	5.464e-04	6.601e-04
C (output stable)	3.996e-04	4.754e-04	6.454e-04	8.182e-04
D (output stable)	3.505e-04	4.237e-04	5.748e-04	7.224e-04
A to Z	2.584e-03	4.046e-03	5.733e-03	7.279e-03
B to Z	2.477e-03	3.955e-03	5.594e-03	7.098e-03
C to Z	2.667e-03	3.950e-03	5.347e-03	6.816e-03
D to Z	2.585e-03	3.852e-03	5.214e-03	6.624e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

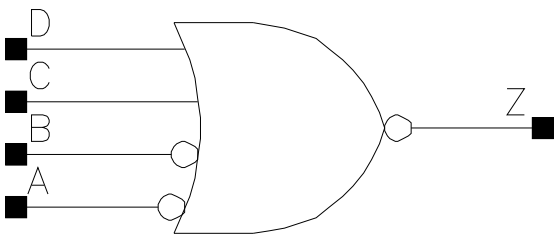
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	1.224	0.9792
X7_P10	0.800	1.496	1.1968
X11_P10	0.800	2.040	1.6320
X14_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P10	X7_P10	X11_P10	X14_P10
A	0.0007	0.0007	0.0014	0.0013
B	0.0008	0.0008	0.0014	0.0014
C	0.0005	0.0011	0.0015	0.0021
D	0.0005	0.0010	0.0015	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X7_P10	X4_P10	X7_P10
A to Z ↓	0.0290	0.0306	3.0233	1.5625
A to Z ↑	0.0389	0.0387	13.0774	6.7544
B to Z ↓	0.0269	0.0284	3.0217	1.5610
B to Z ↑	0.0391	0.0391	13.0870	6.7575
C to Z ↓	0.0104	0.0101	3.1502	1.6446
C to Z ↑	0.0217	0.0219	13.1360	6.7882

D to Z ↓	0.0090	0.0077	3.1720	1.6452
D to Z ↑	0.0201	0.0170	13.1611	6.8073
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0277	0.0305	1.0724	0.8060
A to Z ↑	0.0358	0.0390	4.5660	3.3948
B to Z ↓	0.0252	0.0284	1.0707	0.8046
B to Z ↑	0.0358	0.0398	4.5664	3.3949
C to Z ↓	0.0103	0.0103	1.1331	0.8444
C to Z ↑	0.0208	0.0214	4.5853	3.4090
D to Z ↓	0.0079	0.0078	1.1342	0.8479
D to Z ↑	0.0174	0.0167	4.5990	3.4195

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	3.476e-07	1.000e-20
X7_P10	4.788e-07	1.000e-20
X11_P10	7.623e-07	1.000e-20
X14_P10	8.936e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X7_P10	X11_P10	X14_P10
A (output stable)	7.915e-04	9.685e-04	1.522e-03	1.889e-03
B (output stable)	7.303e-04	9.030e-04	1.374e-03	1.764e-03
C (output stable)	5.358e-05	3.376e-05	6.077e-05	9.563e-05
D (output stable)	5.296e-05	7.675e-05	1.011e-04	1.690e-04
A to Z	3.191e-03	4.406e-03	6.710e-03	8.768e-03
B to Z	2.933e-03	4.153e-03	6.179e-03	8.301e-03
C to Z	9.124e-04	1.754e-03	2.467e-03	3.398e-03
D to Z	7.143e-04	1.122e-03	1.690e-03	2.191e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

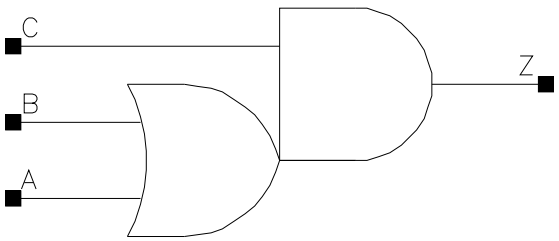
Pin Cycle (vdds)	X4_P10	X7_P10	X11_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.680	0.5440
X10_P10	0.800	0.952	0.7616
X19_P10	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0006	0.0007	0.0012
B	0.0007	0.0007	0.0014
C	0.0008	0.0009	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0287	0.0325	3.1253	1.5641
A to Z ↑	0.0237	0.0279	5.3671	2.3393
B to Z ↓	0.0292	0.0332	3.1279	1.5649
B to Z ↑	0.0218	0.0257	5.3671	2.3355
C to Z ↓	0.0264	0.0285	3.0883	1.5390
C to Z ↑	0.0226	0.0257	5.3637	2.3362
	X19_P10		**X19_P10**	
A to Z ↓	0.0337		0.8167	
A to Z ↑	0.0292		1.1960	

B to Z ↓	0.0344		0.8174	
B to Z ↑	0.0267		1.1932	
C to Z ↓	0.0286		0.8012	
C to Z ↑	0.0260		1.1929	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	3.429e-07	1.000e-20
X10_P10	5.726e-07	1.000e-20
X19_P10	1.076e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	7.741e-05	8.298e-05	1.578e-04
B (output stable)	3.718e-05	4.167e-05	6.972e-05
C (output stable)	4.660e-05	4.337e-05	9.619e-05
A to Z	1.743e-03	2.814e-03	5.687e-03
B to Z	1.573e-03	2.610e-03	5.295e-03
C to Z	1.938e-03	2.970e-03	5.870e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

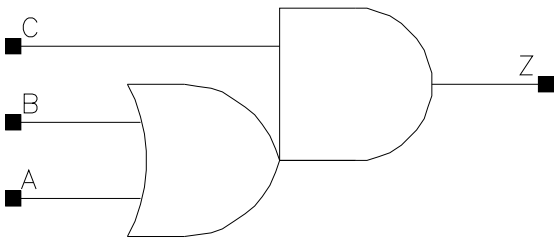
Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	1.360	1.0880
X14_P10	0.800	1.496	1.1968
X19_P10	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0006	0.0013	0.0013	0.0013
B	0.0007	0.0013	0.0012	0.0012
C	0.0007	0.0013	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0352	0.0296	3.0516	1.5473
A to Z ↑	0.0244	0.0224	4.6382	2.2694
B to Z ↓	0.0358	0.0297	3.0550	1.5460
B to Z ↑	0.0227	0.0207	4.6328	2.2708
C to Z ↓	0.0240	0.0199	2.9967	1.5257
C to Z ↑	0.0225	0.0201	4.6317	2.2682
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0329	0.0358	1.0806	0.8160

A to Z ↑	0.0247	0.0265	1.5396	1.1560
B to Z ↓	0.0332	0.0363	1.0816	0.8159
B to Z ↑	0.0231	0.0251	1.5389	1.1554
C to Z ↓	0.0224	0.0245	1.0603	0.7979
C to Z ↑	0.0227	0.0248	1.5370	1.1543

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	3.956e-07	1.000e-20
X10_P10	7.996e-07	1.000e-20
X14_P10	9.494e-07	1.000e-20
X19_P10	1.097e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.803e-05	4.036e-05	4.050e-05	3.963e-05
B (output stable)	9.515e-06	2.075e-05	2.067e-05	2.098e-05
C (output stable)	2.035e-04	3.986e-04	3.984e-04	4.047e-04
A to Z	2.242e-03	3.938e-03	5.029e-03	6.045e-03
B to Z	2.051e-03	3.485e-03	4.581e-03	5.608e-03
C to Z	1.786e-03	2.988e-03	4.039e-03	4.980e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

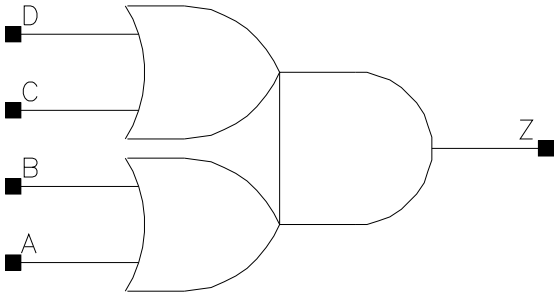
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.952	0.7616
X10_P10	0.800	1.088	0.8704
X14_P10	0.800	1.904	1.5232
X19_P10	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0004	0.0006	0.0012	0.0012
B	0.0004	0.0007	0.0013	0.0013
C	0.0005	0.0007	0.0013	0.0013
D	0.0004	0.0007	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0488	0.0395	3.1697	1.5768
A to Z ↑	0.0331	0.0289	4.6586	2.3248
B to Z ↓	0.0497	0.0402	3.1703	1.5776

B to Z ↑	0.0317	0.0273	4.6529	2.3206
C to Z ↓	0.0416	0.0349	3.1475	1.5705
C to Z ↑	0.0321	0.0290	4.6541	2.3223
D to Z ↓	0.0423	0.0353	3.1490	1.5720
D to Z ↑	0.0303	0.0269	4.6484	2.3193
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0377	0.0400	1.0976	0.8237
A to Z ↑	0.0274	0.0287	1.5441	1.1609
B to Z ↓	0.0369	0.0392	1.0982	0.8245
B to Z ↑	0.0253	0.0265	1.5408	1.1587
C to Z ↓	0.0322	0.0346	1.0927	0.8202
C to Z ↑	0.0267	0.0281	1.5417	1.1596
D to Z ↓	0.0308	0.0334	1.0941	0.8212
D to Z ↑	0.0241	0.0256	1.5390	1.1569

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	2.898e-07	1.000e-20
X10_P10	6.127e-07	1.000e-20
X14_P10	1.026e-06	1.000e-20
X19_P10	1.158e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.436e-05	2.408e-05	7.531e-05	7.527e-05
B (output stable)	1.339e-05	1.678e-05	4.882e-05	4.896e-05
C (output stable)	2.843e-05	5.124e-05	1.538e-04	1.540e-04
D (output stable)	5.418e-05	6.574e-05	1.557e-04	1.545e-04
A to Z	2.206e-03	3.443e-03	5.883e-03	6.711e-03
B to Z	2.096e-03	3.226e-03	5.276e-03	6.108e-03
C to Z	1.900e-03	3.031e-03	5.031e-03	5.858e-03
D to Z	1.794e-03	2.829e-03	4.402e-03	5.242e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

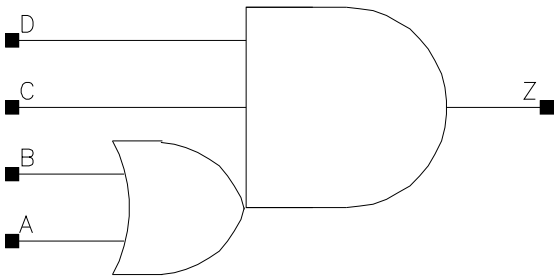
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	0.816	0.6528
X10_P10	0.800	1.088	0.8704
X14_P10	0.800	1.904	1.5232
X19_P10	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P10	X10_P10	X14_P10	X19_P10
A	0.0004	0.0009	0.0011	0.0013
B	0.0005	0.0007	0.0011	0.0013
C	0.0005	0.0007	0.0011	0.0013
D	0.0005	0.0007	0.0011	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X10_P10	X4_P10	X10_P10
A to Z ↓	0.0414	0.0399	3.4483	1.6091
A to Z ↑	0.0370	0.0384	4.9451	2.3690
B to Z ↓	0.0428	0.0378	3.4510	1.6097
B to Z ↑	0.0355	0.0337	4.9452	2.3669
C to Z ↓	0.0352	0.0313	3.3520	1.5733

C to Z ↑	0.0350	0.0339	4.9407	2.3640
D to Z ↓	0.0344	0.0302	3.3513	1.5728
D to Z ↑	0.0368	0.0352	4.9429	2.3648
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0393	0.0375	1.1001	0.8171
A to Z ↑	0.0370	0.0377	1.5767	1.1819
B to Z ↓	0.0381	0.0365	1.0997	0.8169
B to Z ↑	0.0337	0.0343	1.5734	1.1789
C to Z ↓	0.0327	0.0313	1.0752	0.8005
C to Z ↑	0.0341	0.0343	1.5733	1.1774
D to Z ↓	0.0310	0.0298	1.0731	0.7996
D to Z ↑	0.0344	0.0347	1.5728	1.1782

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	2.521e-07	1.000e-20
X10_P10	5.518e-07	1.000e-20
X14_P10	8.202e-07	1.000e-20
X19_P10	1.084e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X10_P10	X14_P10	X19_P10
A (output stable)	5.454e-05	9.431e-05	1.664e-04	1.924e-04
B (output stable)	3.955e-05	6.482e-05	1.049e-04	1.224e-04
C (output stable)	9.328e-06	2.049e-05	4.876e-05	5.477e-05
D (output stable)	2.391e-05	3.943e-05	1.309e-04	1.407e-04
A to Z	1.854e-03	3.345e-03	5.114e-03	6.349e-03
B to Z	1.763e-03	2.979e-03	4.620e-03	5.735e-03
C to Z	2.054e-03	3.458e-03	5.523e-03	6.761e-03
D to Z	1.963e-03	3.306e-03	5.133e-03	6.324e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

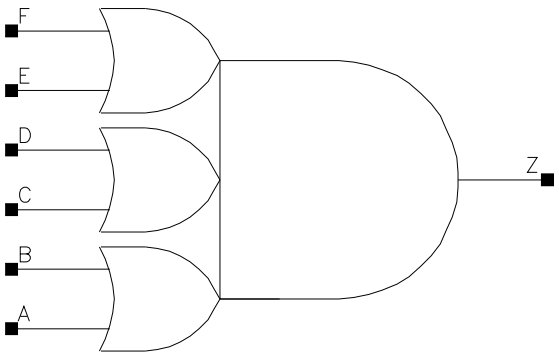
Pin Cycle (vdds)	X4_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	1.360	1.0880
X9_P10	0.800	1.496	1.1968
X19_P10	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P10	X9_P10	X19_P10
A	0.0005	0.0006	0.0011
B	0.0006	0.0008	0.0013
C	0.0005	0.0006	0.0011
D	0.0004	0.0006	0.0013
E	0.0005	0.0006	0.0011
F	0.0005	0.0007	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X9_P10	X4_P10	X9_P10
A to Z ↓	0.0575	0.0477	3.5125	1.7347
A to Z ↑	0.0429	0.0405	5.0831	2.4977
B to Z ↓	0.0599	0.0497	3.5133	1.7350
B to Z ↑	0.0426	0.0392	5.0871	2.4950
C to Z ↓	0.0528	0.0435	3.4914	1.7250
C to Z ↑	0.0432	0.0398	5.0882	2.4969
D to Z ↓	0.0535	0.0442	3.4922	1.7253
D to Z ↑	0.0411	0.0375	5.0842	2.4949
E to Z ↓	0.0452	0.0384	3.4654	1.7170
E to Z ↑	0.0398	0.0378	5.0799	2.4944
F to Z ↓	0.0465	0.0396	3.4667	1.7177
F to Z ↑	0.0384	0.0360	5.0763	2.4917
	X19_P10		X19_P10	
A to Z ↓	0.0466		0.8336	
A to Z ↑	0.0390		1.1812	
B to Z ↓	0.0479		0.8339	
B to Z ↑	0.0364		1.1779	
C to Z ↓	0.0430		0.8288	
C to Z ↑	0.0388		1.1807	
D to Z ↓	0.0440		0.8293	
D to Z ↑	0.0366		1.1774	
E to Z ↓	0.0379		0.8251	
E to Z ↑	0.0372		1.1791	
F to Z ↓	0.0389		0.8258	
F to Z ↑	0.0348		1.1763	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	3.055e-07	1.000e-20
X9_P10	6.344e-07	1.000e-20
X19_P10	1.258e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X9_P10	X19_P10
A (output stable)	1.111e-05	1.876e-05	3.498e-05
B (output stable)	1.065e-05	1.578e-05	1.833e-05
C (output stable)	2.656e-05	3.942e-05	8.143e-05
D (output stable)	3.297e-05	4.866e-05	9.722e-05
E (output stable)	3.764e-05	5.726e-05	1.137e-04
F (output stable)	9.449e-05	1.208e-04	2.290e-04
A to Z	2.633e-03	4.114e-03	7.984e-03
B to Z	2.556e-03	3.952e-03	7.606e-03
C to Z	2.375e-03	3.739e-03	7.306e-03
D to Z	2.262e-03	3.531e-03	6.918e-03
E to Z	2.039e-03	3.321e-03	6.492e-03
F to Z	1.950e-03	3.145e-03	6.140e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

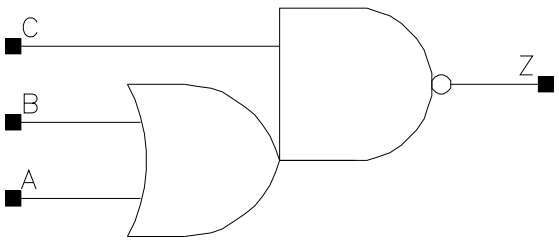
Pin Cycle (vdds)	X4_P10	X9_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.544	0.4352
X10_P10	0.800	1.360	1.0880
X20_P10	0.800	2.720	2.1760
X26_P10	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P10	X10_P10	X20_P10	X26_P10
A	0.0005	0.0016	0.0031	0.0041
B	0.0005	0.0014	0.0028	0.0039
C	0.0005	0.0016	0.0033	0.0045

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X10_P10**	**X3_P10**	**X10_P10**
A to Z ↓	0.0123	0.0135	6.1714	1.9470
A to Z ↑	0.0166	0.0170	11.0312	3.0562
B to Z ↓	0.0101	0.0107	6.0528	1.9594
B to Z ↑	0.0162	0.0149	11.0899	3.0803
C to Z ↓	0.0116	0.0121	5.5895	1.7823
C to Z ↑	0.0162	0.0152	5.8730	1.6314
	X20_P10	**X26_P10**	**X20_P10**	**X26_P10**
A to Z ↓	0.0140	0.0141	0.9960	0.7543

A to Z ↑	0.0175	0.0176	1.5660	1.1777
B to Z ↓	0.0112	0.0113	1.0065	0.7657
B to Z ↑	0.0156	0.0156	1.5775	1.1870
C to Z ↓	0.0127	0.0128	0.9143	0.6938
C to Z ↑	0.0155	0.0155	0.8011	0.6020

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	1.821e-07	1.000e-20
X10_P10	6.289e-07	1.000e-20
X20_P10	1.243e-06	1.000e-20
X26_P10	1.637e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X10_P10	X20_P10	X26_P10
A (output stable)	7.059e-05	2.518e-04	5.113e-04	6.615e-04
B (output stable)	3.602e-05	1.169e-04	2.302e-04	2.983e-04
C (output stable)	4.133e-05	1.309e-04	2.898e-04	3.763e-04
A to Z	6.615e-04	2.534e-03	5.248e-03	6.987e-03
B to Z	4.988e-04	1.688e-03	3.625e-03	4.841e-03
C to Z	8.352e-04	2.887e-03	6.056e-03	7.999e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P10	X10_P10	X20_P10	X26_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

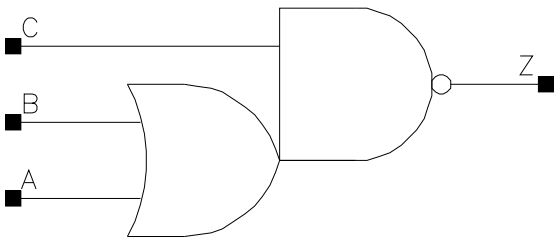
life.augmented

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X7_P10	0.800	0.952	0.7616
X10_P10	0.800	1.360	1.0880
X13_P10	0.800	1.904	1.5232
X26_P10	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X10_P10	X13_P10
A	0.0006	0.0011	0.0018	0.0022
B	0.0006	0.0011	0.0016	0.0020
C	0.0007	0.0010	0.0015	0.0021
	X26_P10			
A	0.0044			
B	0.0040			
C	0.0040			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X7_P10	X3_P10	X7_P10
A to Z ↓	0.0148	0.0134	5.3832	2.8040
A to Z ↑	0.0220	0.0197	8.8091	4.5309
B to Z ↓	0.0130	0.0113	5.4009	2.7253

B to Z ↑	0.0221	0.0194	8.8520	4.5511
C to Z ↓	0.0122	0.0105	5.1133	2.6059
C to Z ↑	0.0137	0.0117	4.8114	2.5119
	X10_P10	**X13_P10**	**X10_P10**	**X13_P10**
A to Z ↓	0.0130	0.0138	1.8957	1.4493
A to Z ↑	0.0191	0.0208	2.9890	2.2957
B to Z ↓	0.0110	0.0113	1.8866	1.4514
B to Z ↑	0.0187	0.0188	3.0039	2.3093
C to Z ↓	0.0102	0.0104	1.7896	1.3646
C to Z ↑	0.0111	0.0111	1.6532	1.2522
	X26_P10		**X26_P10**	
A to Z ↓	0.0137		0.7489	
A to Z ↑	0.0205		1.1579	
B to Z ↓	0.0111		0.7462	
B to Z ↑	0.0185		1.1651	
C to Z ↓	0.0105		0.7038	
C to Z ↑	0.0109		0.6314	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.537e-07	1.000e-20
X7_P10	4.562e-07	1.000e-20
X10_P10	6.666e-07	1.000e-20
X13_P10	8.931e-07	1.000e-20
X26_P10	1.720e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X7_P10	X10_P10	X13_P10
A (output stable)	1.982e-05	4.045e-05	5.673e-05	1.144e-04
B (output stable)	1.006e-05	1.962e-05	2.879e-05	5.050e-05
C (output stable)	2.184e-04	3.995e-04	5.483e-04	7.800e-04
A to Z	1.311e-03	2.113e-03	3.064e-03	4.482e-03
B to Z	1.078e-03	1.674e-03	2.384e-03	3.227e-03
C to Z	7.750e-04	1.264e-03	1.777e-03	2.486e-03
	X26_P10			
A (output stable)	2.148e-04			
B (output stable)	9.572e-05			
C (output stable)	1.464e-03			
A to Z	8.673e-03			
B to Z	6.164e-03			
C to Z	4.756e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P10	X7_P10	X10_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

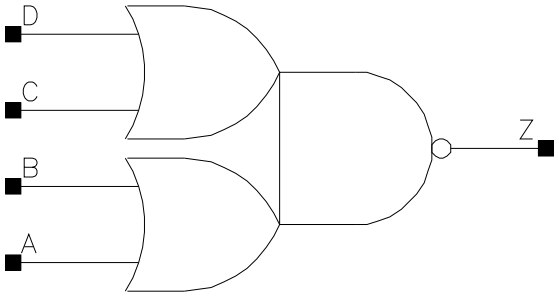
	X26_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X6_P10	0.800	1.360	1.0880
X8_P10	0.800	1.768	1.4144
X11_P10	0.800	2.448	1.9584
X24_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X8_P10	X11_P10
A	0.0006	0.0011	0.0016	0.0022
B	0.0005	0.0010	0.0015	0.0019
C	0.0005	0.0011	0.0015	0.0021
D	0.0005	0.0009	0.0014	0.0019
	X24_P10			
A	0.0046			
B	0.0041			
C	0.0043			
D	0.0039			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X6_P10**	**X3_P10**	**X6_P10**
A to Z ↓	0.0141	0.0163	5.0626	2.7567
A to Z ↑	0.0241	0.0242	10.9161	4.7834
B to Z ↓	0.0127	0.0140	5.0173	2.7651
B to Z ↑	0.0243	0.0223	10.9467	4.8071
C to Z ↓	0.0119	0.0143	5.1663	2.7789
C to Z ↑	0.0170	0.0184	10.9541	4.8080
D to Z ↓	0.0102	0.0113	5.1207	2.8109
D to Z ↑	0.0166	0.0153	11.0031	4.8443
	X8_P10	**X11_P10**	**X8_P10**	**X11_P10**
A to Z ↓	0.0156	0.0158	1.8882	1.4317
A to Z ↑	0.0227	0.0229	3.2067	2.4049
B to Z ↓	0.0136	0.0135	1.8993	1.4343
B to Z ↑	0.0215	0.0214	3.2255	2.4192
C to Z ↓	0.0139	0.0143	1.9152	1.4509
C to Z ↑	0.0171	0.0177	3.2018	2.4233
D to Z ↓	0.0115	0.0114	1.9405	1.4584
D to Z ↑	0.0151	0.0151	3.2306	2.4450
	X24_P10		**X24_P10**	
A to Z ↓	0.0159		0.7033	
A to Z ↑	0.0229		1.1603	
B to Z ↓	0.0136		0.6981	
B to Z ↑	0.0216		1.1671	
C to Z ↓	0.0147		0.7130	
C to Z ↑	0.0176		1.1620	
D to Z ↓	0.0117		0.7110	
D to Z ↑	0.0153		1.1723	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.455e-07	1.000e-20
X6_P10	5.367e-07	1.000e-20
X8_P10	7.676e-07	1.000e-20
X11_P10	1.035e-06	1.000e-20
X24_P10	2.087e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X6_P10	X8_P10	X11_P10
A (output stable)	2.081e-05	7.787e-05	9.818e-05	1.395e-04
B (output stable)	1.367e-05	4.870e-05	6.020e-05	8.621e-05
C (output stable)	4.878e-05	1.589e-04	1.932e-04	2.894e-04
D (output stable)	6.740e-05	1.595e-04	2.078e-04	2.808e-04
A to Z	1.214e-03	2.846e-03	3.937e-03	5.322e-03
B to Z	1.024e-03	2.213e-03	3.058e-03	4.118e-03
C to Z	7.503e-04	1.992e-03	2.728e-03	3.801e-03
D to Z	5.895e-04	1.354e-03	1.918e-03	2.623e-03
	X24_P10			
A (output stable)	2.853e-04			
B (output stable)	1.629e-04			
C (output stable)	5.597e-04			
D (output stable)	5.466e-04			

A to Z	1.096e-02			
B to Z	8.503e-03			
C to Z	7.818e-03			
D to Z	5.465e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

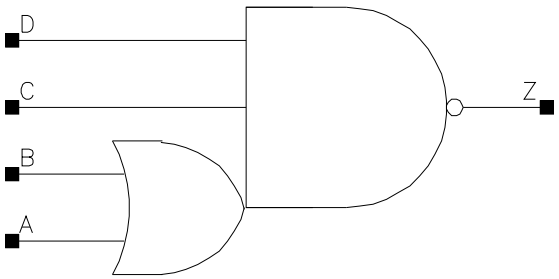
Pin Cycle (vdds)	X3_P10	X6_P10	X8_P10	X11_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X6_P10	0.800	1.360	1.0880
X12_P10	0.800	2.448	1.9584
X18_P10	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X12_P10	X18_P10
A	0.0007	0.0010	0.0020	0.0030
B	0.0005	0.0010	0.0019	0.0028
C	0.0006	0.0011	0.0022	0.0034
D	0.0006	0.0011	0.0021	0.0031

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0210	0.0180	7.5622	4.0801
A to Z ↑	0.0237	0.0197	9.1372	4.5956
B to Z ↓	0.0159	0.0143	7.5978	4.0994
B to Z ↑	0.0202	0.0174	9.1662	4.6253
C to Z ↓	0.0175	0.0177	7.1164	3.8420

C to Z ↑	0.0191	0.0184	4.6328	2.3862
D to Z ↓	0.0188	0.0174	7.1489	3.8603
D to Z ↑	0.0185	0.0168	4.7652	2.3930
	X12_P10	**X18_P10**	**X12_P10**	**X18_P10**
A to Z ↓	0.0184	0.0186	2.1256	1.4377
A to Z ↑	0.0194	0.0194	2.3034	1.5445
B to Z ↓	0.0145	0.0148	2.1381	1.4483
B to Z ↑	0.0171	0.0173	2.3202	1.5554
C to Z ↓	0.0175	0.0177	2.0023	1.3558
C to Z ↑	0.0181	0.0180	1.2167	0.8006
D to Z ↓	0.0174	0.0175	2.0125	1.3623
D to Z ↑	0.0165	0.0164	1.2133	0.8102

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.113e-07	1.000e-20
X6_P10	3.959e-07	1.000e-20
X12_P10	7.506e-07	1.000e-20
X18_P10	1.106e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X6_P10	X12_P10	X18_P10
A (output stable)	9.970e-05	1.981e-04	3.730e-04	5.459e-04
B (output stable)	7.124e-05	1.301e-04	2.407e-04	3.429e-04
C (output stable)	1.570e-05	4.803e-05	8.177e-05	1.233e-04
D (output stable)	4.052e-05	1.241e-04	2.114e-04	3.371e-04
A to Z	1.320e-03	2.086e-03	4.098e-03	6.113e-03
B to Z	9.389e-04	1.477e-03	2.857e-03	4.314e-03
C to Z	1.519e-03	2.806e-03	5.337e-03	8.006e-03
D to Z	1.381e-03	2.338e-03	4.473e-03	6.647e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

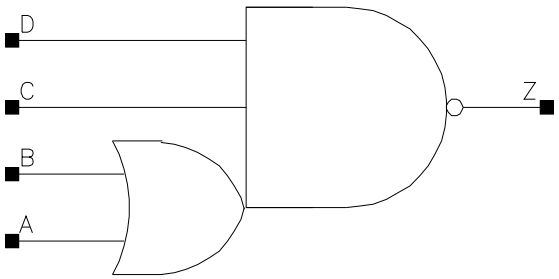
Pin Cycle (vdds)	X3_P10	X6_P10	X12_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X6_P10	0.800	1.360	1.0880
X9_P10	0.800	1.768	1.4144
X12_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X9_P10	X12_P10
A	0.0006	0.0011	0.0018	0.0023
B	0.0006	0.0010	0.0015	0.0023
C	0.0005	0.0010	0.0016	0.0021
D	0.0005	0.0010	0.0015	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0180	0.0185	8.1452	4.0253
A to Z ↑	0.0234	0.0248	9.2538	4.5876
B to Z ↓	0.0157	0.0157	7.9898	4.0438
B to Z ↑	0.0235	0.0234	9.2909	4.6071
C to Z ↓	0.0143	0.0153	7.6893	3.8432

C to Z ↑	0.0150	0.0152	5.0308	2.4819
D to Z ↓	0.0145	0.0142	7.7404	3.8711
D to Z ↑	0.0133	0.0128	5.0748	2.5017
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0188	0.0188	2.7711	2.1061
A to Z ↑	0.0241	0.0246	3.0251	2.3595
B to Z ↓	0.0161	0.0160	2.7706	2.1095
B to Z ↑	0.0230	0.0237	3.0398	2.3715
C to Z ↓	0.0152	0.0154	2.6382	2.0055
C to Z ↑	0.0148	0.0150	1.6375	1.2424
D to Z ↓	0.0145	0.0143	2.6562	2.0207
D to Z ↑	0.0126	0.0124	1.6515	1.2565

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.021e-07	1.000e-20
X6_P10	4.275e-07	1.000e-20
X9_P10	6.044e-07	1.000e-20
X12_P10	8.112e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	1.117e-05	3.054e-05	4.616e-05	5.857e-05
B (output stable)	6.935e-06	2.071e-05	2.996e-05	4.887e-05
C (output stable)	4.876e-05	1.048e-04	1.514e-04	1.908e-04
D (output stable)	1.069e-04	3.659e-04	4.342e-04	6.789e-04
A to Z	1.366e-03	2.985e-03	4.355e-03	5.832e-03
B to Z	1.141e-03	2.337e-03	3.400e-03	4.540e-03
C to Z	8.752e-04	1.961e-03	2.791e-03	3.801e-03
D to Z	7.294e-04	1.525e-03	2.212e-03	2.922e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

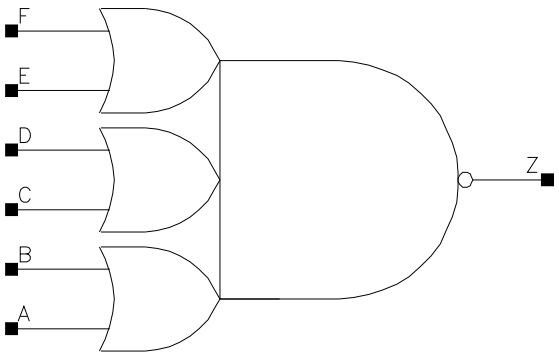
Pin Cycle (vdds)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.224	0.9792
X3_P10	0.800	1.224	0.9792
X5_P10	0.800	2.040	1.6320
X8_P10	0.800	2.720	2.1760
X10_P10	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P10	X3_P10	X5_P10	X8_P10
A	0.0005	0.0006	0.0011	0.0017
B	0.0005	0.0006	0.0010	0.0016
C	0.0005	0.0006	0.0011	0.0016
D	0.0005	0.0005	0.0010	0.0015

E	0.0004	0.0006	0.0010	0.0015
F	0.0004	0.0005	0.0010	0.0014
	X10_P10			
A	0.0023			
B	0.0021			
C	0.0021			
D	0.0020			
E	0.0020			
F	0.0019			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X3_P10**	**X2_P10**	**X3_P10**
A to Z ↓	0.0231	0.0223	8.8836	6.9273
A to Z ↑	0.0326	0.0285	12.6370	8.7185
B to Z ↓	0.0216	0.0206	8.9064	6.9672
B to Z ↑	0.0336	0.0294	12.6674	8.7470
C to Z ↓	0.0226	0.0221	8.9296	6.9494
C to Z ↑	0.0285	0.0255	12.6401	8.8647
D to Z ↓	0.0215	0.0199	9.0155	7.0378
D to Z ↑	0.0301	0.0257	12.6970	8.8900
E to Z ↓	0.0196	0.0192	8.9838	6.9840
E to Z ↑	0.0225	0.0202	12.6584	8.8850
F to Z ↓	0.0181	0.0171	9.0629	7.0816
F to Z ↑	0.0231	0.0202	12.7235	8.9287
	X5_P10	**X8_P10**	**X5_P10**	**X8_P10**
A to Z ↓	0.0237	0.0233	3.7036	2.5245
A to Z ↑	0.0297	0.0287	4.5864	3.0350
B to Z ↓	0.0210	0.0207	3.7224	2.5266
B to Z ↑	0.0285	0.0282	4.6039	3.0479
C to Z ↓	0.0217	0.0224	3.7282	2.5393
C to Z ↑	0.0252	0.0249	4.6339	3.1061
D to Z ↓	0.0190	0.0196	3.7397	2.5449
D to Z ↑	0.0241	0.0246	4.6567	3.1214
E to Z ↓	0.0202	0.0201	3.7593	2.5550
E to Z ↑	0.0205	0.0199	4.6378	3.1171
F to Z ↓	0.0170	0.0170	3.7769	2.5557
F to Z ↑	0.0186	0.0188	4.6697	3.1400
	X10_P10		**X10_P10**	
A to Z ↓	0.0238		1.9177	
A to Z ↑	0.0292		2.3073	
B to Z ↓	0.0211		1.9214	
B to Z ↑	0.0283		2.3164	
C to Z ↓	0.0221		1.9276	
C to Z ↑	0.0250		2.3527	
D to Z ↓	0.0194		1.9325	
D to Z ↑	0.0242		2.3647	
E to Z ↓	0.0203		1.9391	
E to Z ↑	0.0202		2.3467	
F to Z ↓	0.0175		1.9508	
F to Z ↑	0.0188		2.3637	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P10	2.367e-07	1.000e-20
X3_P10	3.582e-07	1.000e-20
X5_P10	6.788e-07	1.000e-20
X8_P10	9.701e-07	1.000e-20
X10_P10	1.291e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P10	X3_P10	X5_P10	X8_P10
A (output stable)	1.443e-05	1.949e-05	6.526e-05	8.178e-05
B (output stable)	8.204e-06	1.154e-05	4.042e-05	4.909e-05
C (output stable)	3.441e-05	4.638e-05	1.120e-04	1.454e-04
D (output stable)	4.273e-05	5.003e-05	1.259e-04	1.671e-04
E (output stable)	4.925e-05	6.360e-05	1.364e-04	1.814e-04
F (output stable)	1.099e-04	1.334e-04	2.446e-04	3.574e-04
A to Z	1.704e-03	2.070e-03	4.195e-03	6.041e-03
B to Z	1.550e-03	1.859e-03	3.553e-03	5.139e-03
C to Z	1.394e-03	1.715e-03	3.326e-03	4.867e-03
D to Z	1.261e-03	1.493e-03	2.753e-03	4.105e-03
E to Z	1.035e-03	1.282e-03	2.605e-03	3.692e-03
F to Z	9.026e-04	1.084e-03	2.035e-03	2.969e-03
	X10_P10			
A (output stable)	1.184e-04			
B (output stable)	7.438e-05			
C (output stable)	2.114e-04			
D (output stable)	2.404e-04			
E (output stable)	2.487e-04			
F (output stable)	4.632e-04			
A to Z	8.169e-03			
B to Z	6.908e-03			
C to Z	6.513e-03			
D to Z	5.412e-03			
E to Z	5.047e-03			
F to Z	4.011e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P10	X3_P10	X5_P10	X8_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P10			

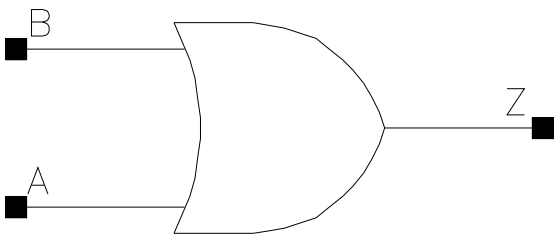
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.544	0.4352
X9_P10	0.800	0.680	0.5440
X19_P10	0.800	1.360	1.0880
X29_P10	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10	X29_P10
A	0.0005	0.0007	0.0012	0.0012
B	0.0005	0.0006	0.0013	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X9_P10**	**X5_P10**	**X9_P10**
A to Z ↓	0.0367	0.0325	3.3108	1.6714
A to Z ↑	0.0226	0.0237	4.8160	2.4321
B to Z ↓	0.0370	0.0324	3.3122	1.6716
B to Z ↑	0.0215	0.0221	4.8165	2.4330
	X19_P10	**X29_P10**	**X19_P10**	**X29_P10**
A to Z ↓	0.0329	0.0389	0.8030	0.5519
A to Z ↑	0.0234	0.0268	1.1502	0.7730
B to Z ↓	0.0314	0.0377	0.8033	0.5517
B to Z ↑	0.0213	0.0248	1.1479	0.7720

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	2.242e-07	1.000e-20
X9_P10	4.273e-07	1.000e-20
X19_P10	8.707e-07	1.000e-20
X29_P10	1.104e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10	X29_P10
A (output stable)	1.580e-05	2.820e-05	1.012e-04	1.014e-04
B (output stable)	4.486e-06	7.028e-06	6.475e-05	6.518e-05
A to Z	1.614e-03	2.568e-03	5.407e-03	7.527e-03
B to Z	1.503e-03	2.372e-03	4.755e-03	6.892e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

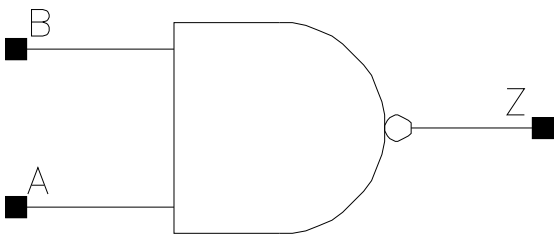
Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10	X29_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X9_P10	0.800	0.952	0.7616
X14_P10	0.800	1.088	0.8704
X18_P10	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P10	X9_P10	X14_P10	X18_P10
A	0.0007	0.0007	0.0007	0.0006
B	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X9_P10**	**X5_P10**	**X9_P10**
A to Z ↓	0.0288	0.0331	2.9834	1.6354
A to Z ↑	0.0314	0.0346	4.6177	2.4368
B to Z ↓	0.0298	0.0348	2.9840	1.6359
B to Z ↑	0.0296	0.0333	4.6188	2.4375
	X14_P10	**X18_P10**	**X14_P10**	**X18_P10**
A to Z ↓	0.0366	0.0387	1.1364	0.8591
A to Z ↑	0.0370	0.0380	1.6135	1.2499
B to Z ↓	0.0383	0.0402	1.1361	0.8596
B to Z ↑	0.0358	0.0367	1.6147	1.2505

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	5.336e-07	1.000e-20
X9_P10	6.286e-07	1.000e-20
X14_P10	7.481e-07	1.000e-20
X18_P10	8.054e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X9_P10	X14_P10	X18_P10
A (output stable)	1.435e-05	1.354e-05	1.364e-05	1.394e-05
B (output stable)	4.944e-05	4.558e-05	4.569e-05	4.438e-05
A to Z	2.961e-03	3.807e-03	4.874e-03	5.407e-03
B to Z	2.816e-03	3.675e-03	4.743e-03	5.275e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

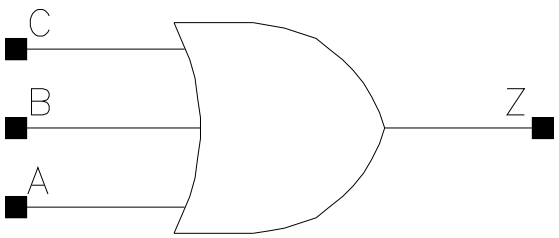
Pin Cycle (vdds)	X5_P10	X9_P10	X14_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.680	0.5440
X10_P10	0.800	0.952	0.7616
X14_P10	0.800	1.496	1.1968
X19_P10	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0005	0.0007	0.0012	0.0019
B	0.0004	0.0007	0.0014	0.0018
C	0.0005	0.0007	0.0013	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0488	0.0436	3.4387	1.6381
A to Z ↑	0.0261	0.0232	4.8381	2.2938
B to Z ↓	0.0481	0.0429	3.4406	1.6373
B to Z ↑	0.0255	0.0222	4.8379	2.2908
C to Z ↓	0.0476	0.0416	3.4389	1.6383
C to Z ↑	0.0245	0.0208	4.8304	2.2921
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0410	0.0395	1.0968	0.8396

A to Z ↑	0.0215	0.0212	1.5694	1.2039
B to Z ↓	0.0413	0.0383	1.0973	0.8405
B to Z ↑	0.0204	0.0205	1.5651	1.2008
C to Z ↓	0.0364	0.0355	1.0973	0.8404
C to Z ↑	0.0185	0.0186	1.5640	1.2002

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	2.114e-07	1.000e-20
X10_P10	4.296e-07	1.000e-20
X14_P10	7.318e-07	1.000e-20
X19_P10	9.971e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	6.164e-05	9.558e-05	2.490e-04	3.914e-04
B (output stable)	-2.150e-06	-8.780e-06	6.499e-05	7.952e-07
C (output stable)	2.696e-06	5.798e-06	4.381e-05	3.124e-05
A to Z	1.914e-03	3.121e-03	5.174e-03	7.363e-03
B to Z	1.792e-03	2.913e-03	4.832e-03	6.578e-03
C to Z	1.683e-03	2.704e-03	4.143e-03	5.815e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

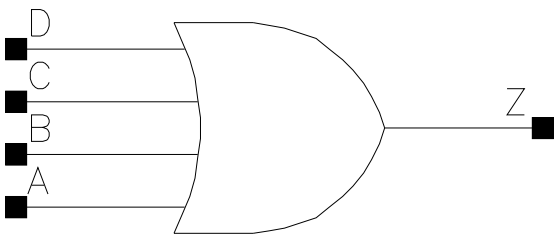
life.augmented

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	1.224	0.9792
X8_P10	0.800	1.496	1.1968
X12_P10	0.800	2.176	1.7408
X15_P10	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X12_P10	X15_P10
A	0.0004	0.0006	0.0012	0.0013
B	0.0005	0.0007	0.0011	0.0013
C	0.0004	0.0006	0.0011	0.0013
D	0.0005	0.0007	0.0011	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
A to Z ↓	0.0383	0.0364	5.2009	2.7603
A to Z ↑	0.0234	0.0238	4.4981	2.4052
B to Z ↓	0.0394	0.0372	5.2015	2.7609
B to Z ↑	0.0224	0.0227	4.4988	2.4041
C to Z ↓	0.0405	0.0354	5.2103	2.7581
C to Z ↑	0.0240	0.0232	4.6143	2.4135

D to Z ↓	0.0421	0.0364	5.2111	2.7576
D to Z ↑	0.0233	0.0221	4.6106	2.4114
	X12_P10	**X15_P10**	**X12_P10**	**X15_P10**
A to Z ↓	0.0372	0.0374	1.9114	1.4330
A to Z ↑	0.0243	0.0231	1.5367	1.1786
B to Z ↓	0.0366	0.0361	1.9130	1.4328
B to Z ↑	0.0230	0.0213	1.5356	1.1769
C to Z ↓	0.0360	0.0354	1.9109	1.4323
C to Z ↑	0.0232	0.0220	1.5314	1.1848
D to Z ↓	0.0354	0.0344	1.9106	1.4323
D to Z ↑	0.0219	0.0203	1.5282	1.1843

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	2.777e-07	1.000e-20
X8_P10	5.882e-07	1.000e-20
X12_P10	7.432e-07	1.000e-20
X15_P10	1.097e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	4.404e-04	7.695e-04	1.205e-03	1.626e-03
B (output stable)	3.927e-04	6.747e-04	1.008e-03	1.330e-03
C (output stable)	4.349e-04	7.624e-04	1.139e-03	1.554e-03
D (output stable)	3.865e-04	6.678e-04	9.322e-04	1.265e-03
A to Z	1.805e-03	3.585e-03	5.134e-03	6.775e-03
B to Z	1.711e-03	3.395e-03	4.722e-03	6.129e-03
C to Z	1.801e-03	3.119e-03	4.497e-03	5.663e-03
D to Z	1.712e-03	2.934e-03	4.087e-03	5.097e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

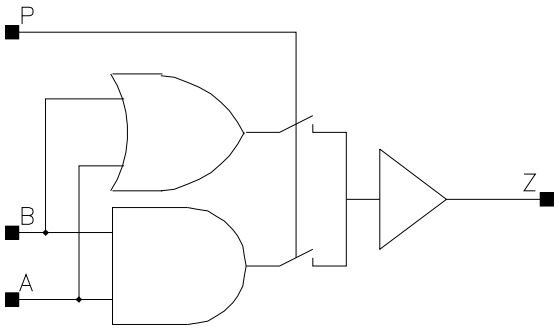
Pin Cycle (vdds)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.952	0.7616
X10_P10	1.600	0.816	1.3056
X14_P10	1.600	1.224	1.9584
X19_P10	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0010	0.0011	0.0022	0.0022
B	0.0009	0.0013	0.0023	0.0024
P	0.0005	0.0007	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0455	0.0411	3.3659	1.5673
A to Z ↑	0.0257	0.0296	4.8499	2.3144
B to Z ↓	0.0451	0.0419	3.3798	1.5759
B to Z ↑	0.0268	0.0311	4.8528	2.3179
P to Z ↓	0.0411	0.0395	3.3823	1.5792
P to Z ↑	0.0258	0.0305	4.8522	2.3164
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**

A to Z ↓	0.0381	0.0407	1.0816	0.8069
A to Z ↑	0.0286	0.0299	1.5865	1.1859
B to Z ↓	0.0363	0.0391	1.0935	0.8145
B to Z ↑	0.0283	0.0300	1.5889	1.1869
P to Z ↓	0.0348	0.0379	1.0983	0.8171
P to Z ↑	0.0284	0.0302	1.5880	1.1868

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	3.134e-07	1.000e-20
X10_P10	6.819e-07	1.000e-20
X14_P10	1.121e-06	1.000e-20
X19_P10	1.291e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	3.928e-05	6.504e-05	1.621e-04	1.519e-04
B (output stable)	9.173e-05	1.149e-04	3.923e-04	3.370e-04
P (output stable)	1.104e-04	1.521e-04	2.591e-04	2.545e-04
A to Z	1.968e-03	3.637e-03	5.943e-03	6.954e-03
B to Z	1.892e-03	3.558e-03	5.492e-03	6.537e-03
P to Z	1.685e-03	3.283e-03	5.235e-03	6.314e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

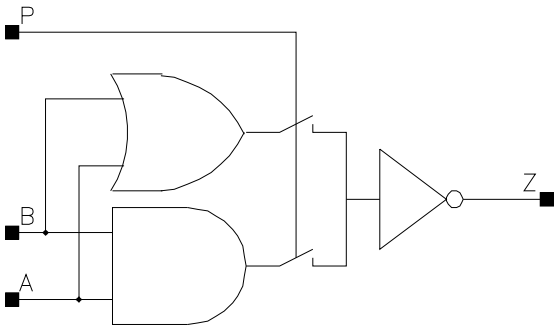
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.600	0.544	0.8704
X10_P10	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P10	X10_P10
A	0.0011	0.0021
B	0.0010	0.0019
P	0.0007	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0156	0.0149	5.2580	2.7527
A to Z ↑	0.0244	0.0230	8.8411	4.4809
B to Z ↓	0.0163	0.0143	5.2032	2.7616
B to Z ↑	0.0242	0.0206	8.8152	4.5416
P to Z ↓	0.0160	0.0133	5.3393	2.7906
P to Z ↑	0.0224	0.0182	8.9137	4.5160

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	3.373e-07	1.000e-20
X10_P10	6.286e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10
A (output stable)	5.575e-05	1.676e-04
B (output stable)	1.055e-04	3.486e-04
P (output stable)	1.265e-04	2.939e-04
A to Z	1.489e-03	2.666e-03
B to Z	1.366e-03	2.154e-03
P to Z	1.129e-03	1.829e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

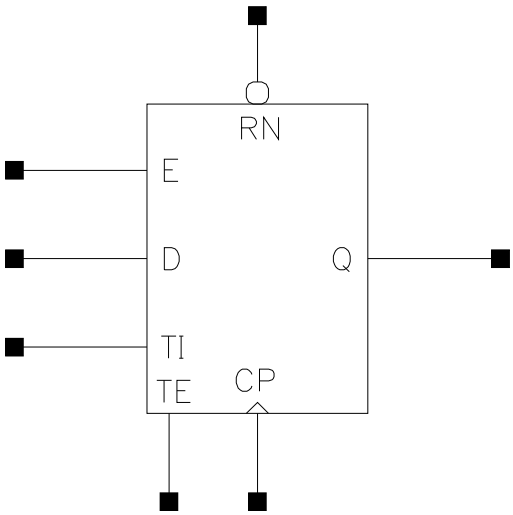
Pin Cycle (vdds)	X5_P10	X10_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.600	2.992	4.7872
X10_P10	1.600	3.128	5.0048
X19_P10	1.600	3.264	5.2224
X23_P10	1.600	3.264	5.2224
X29_P10	1.600	3.536	5.6576
X34_P10	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10	X23_P10
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0012	0.0012	0.0012	0.0012

RN	0.0009	0.0009	0.0009	0.0009
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P10	X34_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0012	0.0012		
RN	0.0009	0.0009		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
CP to Q ↓	0.0562	0.0895	3.0903	1.5412
CP to Q ↑	0.0760	0.1194	4.5656	2.3096
RN to Q ↓	0.0486	0.0878	3.1022	1.5408
	X19_P10	**X23_P10**	**X19_P10**	**X23_P10**
CP to Q ↓	0.0969	0.0974	0.8003	0.6037
CP to Q ↑	0.1240	0.1224	1.1694	1.1431
RN to Q ↓	0.0893	0.0900	0.8002	0.6042
	X29_P10	**X34_P10**	**X29_P10**	**X34_P10**
CP to Q ↓	0.0835	0.0830	0.5274	0.4166
CP to Q ↑	0.1002	0.1010	0.7736	0.7723
RN to Q ↓	0.0776	0.0770	0.5279	0.4166

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P10	X10_P10	X19_P10	X23_P10
CP ↓	min_pulse_width to CP	0.0711	0.0711	0.0711	0.0711
CP ↑	min_pulse_width to CP	0.0483	0.0484	0.0484	0.0484
D ↓	hold_rising to CP	-0.0485	-0.0485	-0.0485	-0.0485
D ↑	hold_rising to CP	-0.0169	-0.0169	-0.0169	-0.0169
D ↓	setup_rising to CP	0.0879	0.0879	0.0912	0.0912
D ↑	setup_rising to CP	0.0444	0.0444	0.0444	0.0444
E ↓	hold_rising to CP	-0.0435	-0.0435	-0.0435	-0.0435
E ↑	hold_rising to CP	-0.0169	-0.0169	-0.0169	-0.0169
E ↓	setup_rising to CP	0.1176	0.1176	0.1176	0.1176
E ↑	setup_rising to CP	0.0884	0.0884	0.0884	0.0884
RN ↓	min_pulse_width to RN	0.0637	0.0588	0.0610	0.0637
RN ↑	recovery_rising to CP	0.0005	0.0005	0.0010	0.0010
RN ↑	removal_rising to CP	0.0096	0.0096	0.0096	0.0096
TE ↓	hold_rising to CP	-0.0240	-0.0240	-0.0240	-0.0240

TE ↑	hold_rising to CP	-0.0093	-0.0093	-0.0093	-0.0093
TE ↓	setup_rising to CP	0.0706	0.0706	0.0706	0.0706
TE ↑	setup_rising to CP	0.0884	0.0884	0.0884	0.0884
TI ↓	hold_rising to CP	-0.0440	-0.0440	-0.0440	-0.0440
TI ↑	hold_rising to CP	-0.0107	-0.0107	-0.0107	-0.0107
TI ↓	setup_rising to CP	0.0875	0.0832	0.0875	0.0875
TI ↑	setup_rising to CP	0.0353	0.0353	0.0353	0.0353
		X29_P10	X34_P10		
CP ↓	min_pulse_width to CP	0.0728	0.0728		
CP ↑	min_pulse_width to CP	0.0483	0.0483		
D ↓	hold_rising to CP	-0.0485	-0.0485		
D ↑	hold_rising to CP	-0.0143	-0.0143		
D ↓	setup_rising to CP	0.0879	0.0912		
D ↑	setup_rising to CP	0.0444	0.0444		
E ↓	hold_rising to CP	-0.0435	-0.0435		
E ↑	hold_rising to CP	-0.0169	-0.0169		
E ↓	setup_rising to CP	0.1176	0.1176		
E ↑	setup_rising to CP	0.0884	0.0884		
RN ↓	min_pulse_width to RN	0.0659	0.0659		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0096	0.0096		
TE ↓	hold_rising to CP	-0.0240	-0.0240		
TE ↑	hold_rising to CP	-0.0093	-0.0093		
TE ↓	setup_rising to CP	0.0706	0.0706		
TE ↑	setup_rising to CP	0.0884	0.0884		
TI ↓	hold_rising to CP	-0.0440	-0.0440		
TI ↑	hold_rising to CP	-0.0107	-0.0107		
TI ↓	setup_rising to CP	0.0875	0.0875		
TI ↑	setup_rising to CP	0.0353	0.0353		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	1.207e-06	1.000e-20
X10_P10	1.463e-06	1.000e-20
X19_P10	1.918e-06	1.000e-20
X23_P10	2.019e-06	1.000e-20

X29_P10	2.480e-06	1.000e-20
X34_P10	2.627e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

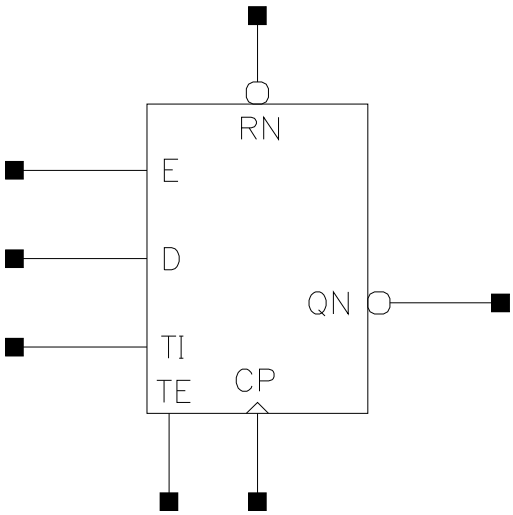
Pin Cycle	X5_P10	X10_P10	X19_P10	X23_P10
Clock 100Mhz Data 0Mhz	7.922e-03	7.914e-03	7.921e-03	7.924e-03
Clock 100Mhz Data 25Mhz	8.186e-03	8.636e-03	9.334e-03	9.384e-03
Clock 100Mhz Data 50Mhz	8.450e-03	9.359e-03	1.075e-02	1.084e-02
Clock = 0 Data 100Mhz	4.653e-03	4.652e-03	4.651e-03	4.651e-03
Clock = 1 Data 100Mhz	1.925e-03	1.926e-03	1.926e-03	1.926e-03
	X29_P10	X34_P10		
Clock 100Mhz Data 0Mhz	7.925e-03	7.926e-03		
Clock 100Mhz Data 25Mhz	1.010e-02	1.030e-02		
Clock 100Mhz Data 50Mhz	1.228e-02	1.268e-02		
Clock = 0 Data 100Mhz	4.650e-03	4.650e-03		
Clock = 1 Data 100Mhz	1.925e-03	1.925e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.600	2.992	4.7872
X10_P10	1.600	3.128	5.0048
X19_P10	1.600	3.264	5.2224
X23_P10	1.600	3.264	5.2224
X29_P10	1.600	3.536	5.6576
X34_P10	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10	X23_P10
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0012	0.0013	0.0013	0.0013

RN	0.0009	0.0009	0.0009	0.0009
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P10	X34_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0013	0.0012		
RN	0.0009	0.0009		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
CP to QN ↓	0.1050	0.0911	3.0964	1.5389
CP to QN ↑	0.0750	0.0708	4.5562	2.3084
RN to QN ↑	0.0731	0.0648	4.5581	2.3110
	X19_P10	**X23_P10**	**X19_P10**	**X23_P10**
CP to QN ↓	0.0955	0.0963	0.7936	0.6038
CP to QN ↑	0.0773	0.0751	1.1700	1.1422
RN to QN ↑	0.0716	0.0692	1.1711	1.1441
	X29_P10	**X34_P10**	**X29_P10**	**X34_P10**
CP to QN ↓	0.1307	0.1281	0.5280	0.4104
CP to QN ↑	0.1004	0.0992	0.7753	0.7724
RN to QN ↑	0.0924	0.0976	0.7748	0.7712

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P10	X10_P10	X19_P10	X23_P10
CP ↓	min_pulse_width to CP	0.0711	0.0728	0.0728	0.0728
CP ↑	min_pulse_width to CP	0.0483	0.0483	0.0483	0.0483
D ↓	hold_rising to CP	-0.0485	-0.0485	-0.0485	-0.0485
D ↑	hold_rising to CP	-0.0169	-0.0143	-0.0143	-0.0143
D ↓	setup_rising to CP	0.0912	0.0912	0.0912	0.0912
D ↑	setup_rising to CP	0.0444	0.0444	0.0444	0.0444
E ↓	hold_rising to CP	-0.0435	-0.0435	-0.0435	-0.0435
E ↑	hold_rising to CP	-0.0169	-0.0169	-0.0169	-0.0169
E ↓	setup_rising to CP	0.1176	0.1176	0.1176	0.1171
E ↑	setup_rising to CP	0.0884	0.0884	0.0884	0.0884
RN ↓	min_pulse_width to RN	0.0588	0.0610	0.0681	0.0681
RN ↑	recovery_rising to CP	0.0005	0.0005	0.0005	0.0005
RN ↑	removal_rising to CP	0.0096	0.0096	0.0096	0.0096
TE ↓	hold_rising to CP	-0.0240	-0.0240	-0.0240	-0.0240

TE ↑	hold_rising to CP	-0.0093	-0.0093	-0.0093	-0.0093
TE ↓	setup_rising to CP	0.0706	0.0706	0.0706	0.0706
TE ↑	setup_rising to CP	0.0884	0.0884	0.0884	0.0884
TI ↓	hold_rising to CP	-0.0440	-0.0440	-0.0440	-0.0440
TI ↑	hold_rising to CP	-0.0107	-0.0107	-0.0107	-0.0107
TI ↓	setup_rising to CP	0.0875	0.0875	0.0891	0.0891
TI ↑	setup_rising to CP	0.0353	0.0353	0.0353	0.0353
		X29_P10	X34_P10		
CP ↓	min_pulse_width to CP	0.0711	0.0711		
CP ↑	min_pulse_width to CP	0.0484	0.0484		
D ↓	hold_rising to CP	-0.0485	-0.0485		
D ↑	hold_rising to CP	-0.0169	-0.0169		
D ↓	setup_rising to CP	0.0879	0.0912		
D ↑	setup_rising to CP	0.0444	0.0444		
E ↓	hold_rising to CP	-0.0435	-0.0435		
E ↑	hold_rising to CP	-0.0169	-0.0169		
E ↓	setup_rising to CP	0.1176	0.1176		
E ↑	setup_rising to CP	0.0884	0.0884		
RN ↓	min_pulse_width to RN	0.0588	0.0588		
RN ↑	recovery_rising to CP	0.0010	0.0010		
RN ↑	removal_rising to CP	0.0096	0.0096		
TE ↓	hold_rising to CP	-0.0240	-0.0240		
TE ↑	hold_rising to CP	-0.0093	-0.0093		
TE ↓	setup_rising to CP	0.0706	0.0706		
TE ↑	setup_rising to CP	0.0884	0.0884		
TI ↓	hold_rising to CP	-0.0437	-0.0437		
TI ↑	hold_rising to CP	-0.0107	-0.0107		
TI ↓	setup_rising to CP	0.0875	0.0875		
TI ↑	setup_rising to CP	0.0353	0.0353		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	1.200e-06	1.000e-20
X10_P10	1.432e-06	1.000e-20
X19_P10	1.871e-06	1.000e-20
X23_P10	2.023e-06	1.000e-20

X29_P10	2.379e-06	1.000e-20
X34_P10	2.580e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

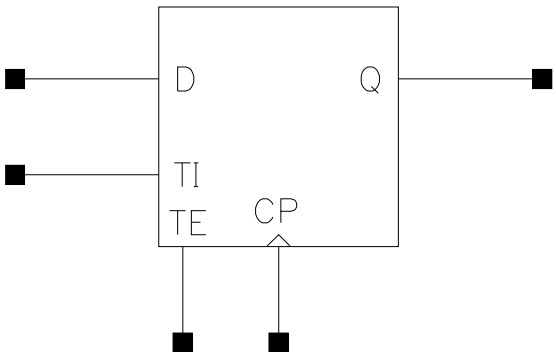
Pin Cycle	X5_P10	X10_P10	X19_P10	X23_P10
Clock 100Mhz Data 0Mhz	7.812e-03	7.820e-03	7.820e-03	7.821e-03
Clock 100Mhz Data 25Mhz	8.180e-03	8.554e-03	9.265e-03	9.299e-03
Clock 100Mhz Data 50Mhz	8.548e-03	9.289e-03	1.071e-02	1.078e-02
Clock = 0 Data 100Mhz	4.616e-03	4.615e-03	4.615e-03	4.615e-03
Clock = 1 Data 100Mhz	1.926e-03	1.926e-03	1.926e-03	1.926e-03
	X29_P10	X34_P10		
Clock 100Mhz Data 0Mhz	7.822e-03	7.821e-03		
Clock 100Mhz Data 25Mhz	1.011e-02	1.028e-02		
Clock 100Mhz Data 50Mhz	1.240e-02	1.273e-02		
Clock = 0 Data 100Mhz	4.614e-03	4.614e-03		
Clock = 1 Data 100Mhz	1.925e-03	1.925e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P10	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P10	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P10	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P10	C8T28SOI_LLHF_-SDFPQX3_P10	C8T28SOIDV_LL_-SDFPQX5_P10	C8T28SOIDV_LL_-SDFPQX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P10	C8T28SOIDV_LL_-SDFPQX23_P10	C8T28SOIDV_LL_-SDFPQX29_P10	
CP	0.0005	0.0005	0.0005	
D	0.0005	0.0005	0.0005	
TE	0.0009	0.0009	0.0009	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P10	**C8T28SOI_LLHF_-SDFPQX3_P10**	**C8T28SOI_LL_-SDFPQX5_P10**	**C8T28SOI_LLHF_-SDFPQX3_P10**
CP to Q ↓	0.0590	0.0506	3.2564	4.9807
CP to Q ↑	0.0559	0.0647	4.6042	7.1171
	C8T28SOIDV_LL_-SDFPQX5_P10	**C8T28SOIDV_LL_-SDFPQX10_P10**	**C8T28SOIDV_LL_-SDFPQX5_P10**	**C8T28SOIDV_LL_-SDFPQX10_P10**
CP to Q ↓	0.0525	0.0730	3.0867	1.4905
CP to Q ↑	0.0652	0.0942	4.5558	2.2832
	C8T28SOIDV_LL_-SDFPQX19_P10	**C8T28SOIDV_LL_-SDFPQX23_P10**	**C8T28SOIDV_LL_-SDFPQX19_P10**	**C8T28SOIDV_LL_-SDFPQX23_P10**
CP to Q ↓	0.0795	0.0816	0.7787	0.5994
CP to Q ↑	0.1000	0.1020	1.1551	1.1450
	C8T28SOIDV_LL_-SDFPQX29_P10		**C8T28SOIDV_LL_-SDFPQX29_P10**	
CP to Q ↓	0.0782		0.5222	
CP to Q ↑	0.0950		0.7657	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P10	C8T28SOI_-LLHF_-SDFPQX3_P10	C8T28SOIDV_-LL_SDFPQX5_-P10	C8T28SOIDV_-LL_SDFPQX10_-P10
CP ↓	min_pulse_width to CP	0.0943	0.0950	0.0815	0.0815
CP ↑	min_pulse_width to CP	0.0452	0.0407	0.0437	0.0404
D ↓	hold_rising to CP	-0.0436	-0.0919	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0120	-0.0094	-0.0022	-0.0022
D ↓	setup_rising to CP	0.0830	0.1364	0.0538	0.0538
D ↑	setup_rising to CP	0.0368	0.0391	0.0271	0.0271
TE ↓	hold_rising to CP	-0.0289	-0.0311	-0.0077	-0.0077
TE ↑	hold_rising to CP	-0.0098	-0.0067	-0.0098	-0.0098
TE ↓	setup_rising to CP	0.0782	0.1095	0.0517	0.0517
TE ↑	setup_rising to CP	0.0982	0.1275	0.0982	0.0982

TI ↓	hold_rising to CP	-0.0586	-0.0867	-0.0502	-0.0502
TI ↑	hold_rising to CP	-0.0104	-0.0049	-0.0120	-0.0120
TI ↓	setup_rising to CP	0.0981	0.1266	0.0945	0.0945
TI ↑	setup_rising to CP	0.0368	0.0355	0.0368	0.0368
		C8T28SOIDV_-LL_SDFPQX19_-P10	C8T28SOIDV_-LL_SDFPQX23_-P10	C8T28SOIDV_-LL_SDFPQX29_-P10	
CP ↓	min_pulse_width to CP	0.0815	0.0815	0.0822	
CP ↑	min_pulse_width to CP	0.0404	0.0437	0.0437	
D ↓	hold_rising to CP	-0.0094	-0.0094	-0.0094	
D ↑	hold_rising to CP	-0.0022	-0.0022	-0.0022	
D ↓	setup_rising to CP	0.0538	0.0538	0.0596	
D ↑	setup_rising to CP	0.0271	0.0271	0.0271	
TE ↓	hold_rising to CP	-0.0077	-0.0077	-0.0072	
TE ↑	hold_rising to CP	-0.0098	-0.0098	-0.0098	
TE ↓	setup_rising to CP	0.0517	0.0517	0.0539	
TE ↑	setup_rising to CP	0.0982	0.0982	0.1008	
TI ↓	hold_rising to CP	-0.0502	-0.0502	-0.0502	
TI ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120	
TI ↓	setup_rising to CP	0.0945	0.0945	0.0988	
TI ↑	setup_rising to CP	0.0368	0.0368	0.0368	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P10	1.000e-06	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P10	8.772e-07	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P10	9.389e-07	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P10	1.274e-06	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P10	1.563e-06	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P10	1.698e-06	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P10	2.017e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P10	C8T28SOI_LLHF_-SDFPQX3_P10	C8T28SOIDV_LL_-SDFPQX5_P10	C8T28SOIDV_LL_-SDFPQX10_P10
Clock 100Mhz Data 0Mhz	7.498e-03	7.249e-03	6.948e-03	6.793e-03
Clock 100Mhz Data 25Mhz	7.200e-03	6.959e-03	6.798e-03	7.139e-03
Clock 100Mhz Data 50Mhz	6.902e-03	6.668e-03	6.648e-03	7.486e-03

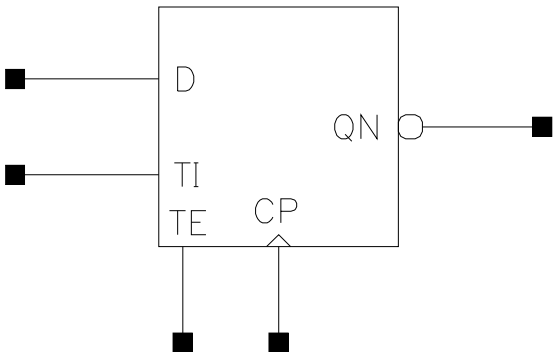
Clock = 0 Data 100Mhz	3.571e-03	3.692e-03	3.526e-03	3.441e-03
Clock = 1 Data 100Mhz	6.257e-05	5.109e-04	3.602e-04	2.848e-04
	C8T28SOIDV_LL_-SDFPQX19_P10	C8T28SOIDV_LL_-SDFPQX23_P10	C8T28SOIDV_LL_-SDFPQX29_P10	
Clock 100Mhz Data 0Mhz	6.703e-03	6.644e-03	6.602e-03	
Clock 100Mhz Data 25Mhz	7.632e-03	7.639e-03	8.182e-03	
Clock 100Mhz Data 50Mhz	8.561e-03	8.634e-03	9.763e-03	
Clock = 0 Data 100Mhz	3.388e-03	3.353e-03	3.331e-03	
Clock = 1 Data 100Mhz	2.396e-04	2.095e-04	1.879e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P10	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P10	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P10	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P10	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P10	C8T28SOI_LLHF_-SDFPQNX3_P10	C8T28SOIDV_LL_-SDFPQNX5_P10	C8T28SOIDV_LL_-SDFPQNX10_P10

CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P10	C8T28SOIDV_LL_-SDFPQNX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P10	**C8T28SOI_LLHF_-SDFPQNX3_P10**	**C8T28SOI_LL_-SDFPQNX5_P10**	**C8T28SOI_LLHF_-SDFPQNX3_P10**
CP to QN ↓	0.0733	0.0788	3.1196	4.6599
CP to QN ↑	0.0642	0.0613	4.9839	6.9266
	C8T28SOIDV_LL_-SDFPQNX5_P10	**C8T28SOIDV_LL_-SDFPQNX10_P10**	**C8T28SOIDV_LL_-SDFPQNX5_P10**	**C8T28SOIDV_LL_-SDFPQNX10_P10**
CP to QN ↓	0.0810	0.0761	3.0191	1.5042
CP to QN ↑	0.0595	0.0648	4.5101	2.2839
	C8T28SOIDV_LL_-SDFPQNX19_P10	**C8T28SOIDV_LL_-SDFPQNX29_P10**	**C8T28SOIDV_LL_-SDFPQNX19_P10**	**C8T28SOIDV_LL_-SDFPQNX29_P10**
CP to QN ↓	0.0859	0.0992	0.7867	0.5331
CP to QN ↑	0.0767	0.0853	1.1765	0.7715

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P10	C8T28SOI_-LLHF_-SDFPQNX3_P10	C8T28SOIDV_-LL_SDFPQNX5_-P10	C8T28SOIDV_-LL_-SDFPQNX10_-P10
CP ↓	min_pulse_width to CP	0.0943	0.0902	0.0815	0.0815
CP ↑	min_pulse_width to CP	0.0392	0.0360	0.0404	0.0436
D ↓	hold_rising to CP	-0.0436	-0.0893	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0120	-0.0094	-0.0022	-0.0022
D ↓	setup_rising to CP	0.0830	0.1338	0.0570	0.0570
D ↑	setup_rising to CP	0.0368	0.0391	0.0271	0.0271
TE ↓	hold_rising to CP	-0.0289	-0.0305	-0.0077	-0.0077
TE ↑	hold_rising to CP	-0.0098	-0.0067	-0.0066	-0.0098
TE ↓	setup_rising to CP	0.0782	0.1073	0.0517	0.0517
TE ↑	setup_rising to CP	0.0982	0.1275	0.0982	0.0982
TI ↓	hold_rising to CP	-0.0583	-0.0867	-0.0502	-0.0502
TI ↑	hold_rising to CP	-0.0104	-0.0049	-0.0064	-0.0120
TI ↓	setup_rising to CP	0.0981	0.1250	0.0945	0.0945

TI ↑	setup_rising to CP	0.0368	0.0355	0.0355	0.0368
		C8T28SOIDV_-LL_-SDFPQNX19_-P10	C8T28SOIDV_-LL_-SDFPQNX29_-P10		
CP ↓	min_pulse_width to CP	0.0815	0.0815		
CP ↑	min_pulse_width to CP	0.0483	0.0404		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	-0.0022	-0.0022		
D ↓	setup_rising to CP	0.0538	0.0538		
D ↑	setup_rising to CP	0.0271	0.0271		
TE ↓	hold_rising to CP	-0.0077	-0.0077		
TE ↑	hold_rising to CP	-0.0098	-0.0098		
TE ↓	setup_rising to CP	0.0517	0.0517		
TE ↑	setup_rising to CP	0.0982	0.0982		
TI ↓	hold_rising to CP	-0.0502	-0.0502		
TI ↑	hold_rising to CP	-0.0120	-0.0120		
TI ↓	setup_rising to CP	0.0945	0.0945		
TI ↑	setup_rising to CP	0.0368	0.0368		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P10	9.899e-07	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P10	8.912e-07	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P10	9.473e-07	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P10	1.246e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P10	1.566e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P10	2.343e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P10	C8T28SOI_LLHF_-SDFPQNX3_P10	C8T28SOIDV_LL_-SDFPQNX5_P10	C8T28SOIDV_LL_-SDFPQNX10_P10
Clock 100Mhz Data 0Mhz	7.552e-03	7.332e-03	7.024e-03	6.858e-03
Clock 100Mhz Data 25Mhz	7.218e-03	7.063e-03	6.804e-03	7.119e-03
Clock 100Mhz Data 50Mhz	6.883e-03	6.794e-03	6.584e-03	7.380e-03
Clock = 0 Data 100Mhz	3.603e-03	3.732e-03	3.568e-03	3.482e-03
Clock = 1 Data 100Mhz	8.949e-05	5.264e-04	3.840e-04	3.128e-04

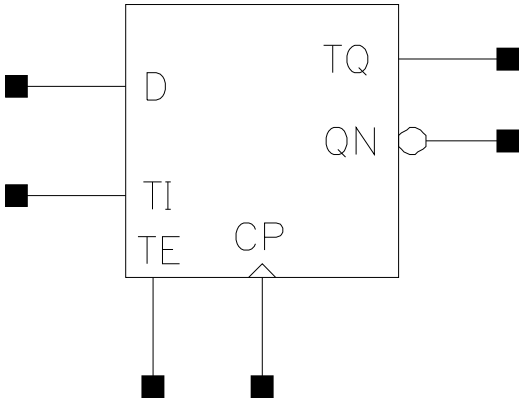
	C8T28SOIDV_LL_-SDFPQNX19_P10	C8T28SOIDV_LL_-SDFPQNX29_P10		
Clock 100Mhz Data 0Mhz	6.762e-03	6.696e-03		
Clock 100Mhz Data 25Mhz	7.760e-03	8.741e-03		
Clock 100Mhz Data 50Mhz	8.757e-03	1.079e-02		
Clock = 0 Data 100Mhz	3.426e-03	3.392e-03		
Clock = 1 Data 100Mhz	2.700e-04	2.415e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P10	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P10	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P10	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P10	C8T28SOI_LLHF_-SDFPQNTX3_P10	C8T28SOIDV_LL_-SDFPQNTX5_P10	C8T28SOIDV_LL_-SDFPQNTX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P10	C8T28SOIDV_LL_-SDFPQNTX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQNTX5_P10	**C8T28SOI_LLHF_-SDFPQNTX3_P10**	**C8T28SOI_LL_-SDFPQNTX5_P10**	**C8T28SOI_LLHF_-SDFPQNTX3_P10**
CP to QN ↓	0.0826	0.0860	3.2347	4.7432
CP to QN ↑	0.0824	0.0759	4.9880	6.9438
CP to TQ ↓	0.0682	0.0533	8.4164	5.4979
CP to TQ ↑	0.0699	0.0641	23.2937	12.5607
	C8T28SOIDV_LL_-SDFPQNTX5_P10	**C8T28SOIDV_LL_-SDFPQNTX10_P10**	**C8T28SOIDV_LL_-SDFPQNTX5_P10**	**C8T28SOIDV_LL_-SDFPQNTX10_P10**
CP to QN ↓	0.0869	0.0844	2.9701	1.5172
CP to QN ↑	0.0700	0.0706	4.5097	2.2866
CP to TQ ↓	0.0494	0.0516	5.4683	5.6931
CP to TQ ↑	0.0652	0.0667	9.9290	10.3634
	C8T28SOIDV_LL_-SDFPQNTX19_P10	**C8T28SOIDV_LL_-SDFPQNTX29_P10**	**C8T28SOIDV_LL_-SDFPQNTX19_P10**	**C8T28SOIDV_LL_-SDFPQNTX29_P10**
CP to QN ↓	0.0869	0.1017	0.7833	0.5358
CP to QN ↑	0.0767	0.0909	1.1651	0.7697
CP to TQ ↓	0.0537	0.0521	5.5949	5.7281
CP to TQ ↑	0.0687	0.0691	10.5782	13.5352

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_-P10	C8T28SOI_-LLHF_-SDFPQNTX3_-P10	C8T28SOIDV_-LL_-SDFPQNTX5_-P10	C8T28SOIDV_-LL_-SDFPQNTX10_-P10
CP ↓	min_pulse_width to CP	0.0943	0.0902	0.0822	0.0815
CP ↑	min_pulse_width to CP	0.0500	0.0454	0.0437	0.0437
D ↓	hold_rising to CP	-0.0436	-0.0893	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0120	-0.0094	-0.0022	-0.0022
D ↓	setup_rising to CP	0.0830	0.1306	0.0570	0.0538

D ↑	setup_rising to CP	0.0368	0.0417	0.0271	0.0271
TE ↓	hold_rising to CP	-0.0289	-0.0305	-0.0072	-0.0077
TE ↑	hold_rising to CP	-0.0098	-0.0093	-0.0066	-0.0098
TE ↓	setup_rising to CP	0.0782	0.1073	0.0517	0.0517
TE ↑	setup_rising to CP	0.0982	0.1275	0.1008	0.0982
TI ↓	hold_rising to CP	-0.0586	-0.0870	-0.0502	-0.0502
TI ↑	hold_rising to CP	-0.0104	-0.0049	-0.0064	-0.0120
TI ↓	setup_rising to CP	0.0981	0.1250	0.0945	0.0945
TI ↑	setup_rising to CP	0.0368	0.0355	0.0353	0.0368
		C8T28SOIDV_-LL_-SDFPQNTX19_-P10	C8T28SOIDV_-LL_-SDFPQNTX29_-P10		
CP ↓	min_pulse_width to CP	0.0815	0.0815		
CP ↑	min_pulse_width to CP	0.0483	0.0437		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	-0.0022	-0.0022		
D ↓	setup_rising to CP	0.0538	0.0538		
D ↑	setup_rising to CP	0.0271	0.0271		
TE ↓	hold_rising to CP	-0.0077	-0.0077		
TE ↑	hold_rising to CP	-0.0098	-0.0098		
TE ↓	setup_rising to CP	0.0517	0.0517		
TE ↑	setup_rising to CP	0.0982	0.0982		
TI ↓	hold_rising to CP	-0.0502	-0.0502		
TI ↑	hold_rising to CP	-0.0120	-0.0120		
TI ↓	setup_rising to CP	0.0945	0.0945		
TI ↑	setup_rising to CP	0.0368	0.0368		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P10	1.011e-06	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P10	9.488e-07	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P10	1.008e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P10	1.187e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P10	1.555e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P10	2.366e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

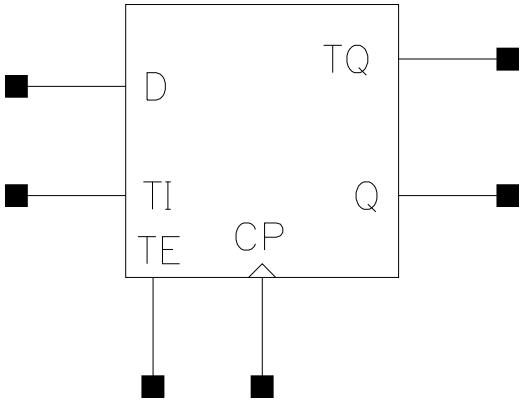
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P10	C8T28SOI_LLHF_-SDFPQNTX3_P10	C8T28SOIDV_LL_-SDFPQNTX5_P10	C8T28SOIDV_LL_-SDFPQNTX10_P10
Clock 100Mhz Data 0Mhz	7.437e-03	7.224e-03	6.937e-03	6.786e-03
Clock 100Mhz Data 25Mhz	7.441e-03	7.212e-03	6.961e-03	7.058e-03
Clock 100Mhz Data 50Mhz	7.446e-03	7.200e-03	6.986e-03	7.331e-03
Clock = 0 Data 100Mhz	3.574e-03	3.704e-03	3.541e-03	3.454e-03
Clock = 1 Data 100Mhz	3.746e-05	5.034e-04	3.493e-04	2.724e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P10	C8T28SOIDV_LL_-SDFPQNTX29_P10		
Clock 100Mhz Data 0Mhz	6.694e-03	6.630e-03		
Clock 100Mhz Data 25Mhz	7.611e-03	8.876e-03		
Clock 100Mhz Data 50Mhz	8.527e-03	1.112e-02		
Clock = 0 Data 100Mhz	3.400e-03	3.366e-03		
Clock = 1 Data 100Mhz	2.263e-04	1.956e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P10	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P10	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P10	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P10	C8T28SOI_LLHF_-SDFPQTX3_P10	C8T28SOIDV_LL_-SDFPQTX5_P10	C8T28SOIDV_LL_-SDFPQTX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P10	C8T28SOIDV_LL_-SDFPQTX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQTX5_P10	**C8T28SOI_LLHF_-SDFPQTX3_P10**	**C8T28SOI_LL_-SDFPQTX5_P10**	**C8T28SOI_LLHF_-SDFPQTX3_P10**
CP to Q ↓	0.0696	0.0641	3.4698	5.1777
CP to Q ↑	0.0607	0.0653	4.6433	7.2285
CP to TQ ↓	0.0839	0.0635	9.1874	5.6800
CP to TQ ↑	0.0772	0.0690	23.5212	12.7600
	C8T28SOIDV_LL_-SDFPQTX5_P10	**C8T28SOIDV_LL_-SDFPQTX10_P10**	**C8T28SOIDV_LL_-SDFPQTX5_P10**	**C8T28SOIDV_LL_-SDFPQTX10_P10**
CP to Q ↓	0.0572	0.0749	3.1694	1.4971
CP to Q ↑	0.0676	0.0959	4.6284	2.2850
CP to TQ ↓	0.0572	0.0773	5.6480	5.7179
CP to TQ ↑	0.0696	0.0997	10.9096	10.7780
	C8T28SOIDV_LL_-SDFPQTX19_P10	**C8T28SOIDV_LL_-SDFPQTX29_P10**	**C8T28SOIDV_LL_-SDFPQTX19_P10**	**C8T28SOIDV_LL_-SDFPQTX29_P10**
CP to Q ↓	0.0811	0.0890	0.7813	0.5085
CP to Q ↑	0.1007	0.0996	1.1570	0.7628
CP to TQ ↓	0.0849	0.0549	5.7708	5.9014
CP to TQ ↑	0.1065	0.0706	10.8157	13.5322

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P10	C8T28SOI_-LLHF_-SDFPQTX3_P10	C8T28SOIDV_-LL_SDFPQTX5_-P10	C8T28SOIDV_-LL_-SDFPQTX10_-P10
CP ↓	min_pulse_width to CP	0.0943	0.0902	0.0815	0.0815
CP ↑	min_pulse_width to CP	0.0594	0.0500	0.0484	0.0404
D ↓	hold_rising to CP	-0.0436	-0.0893	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0120	-0.0094	-0.0022	-0.0022
D ↓	setup_rising to CP	0.0830	0.1338	0.0538	0.0538

D ↑	setup_rising to CP	0.0368	0.0391	0.0271	0.0271
TE ↓	hold_rising to CP	-0.0289	-0.0305	-0.0077	-0.0077
TE ↑	hold_rising to CP	-0.0098	-0.0067	-0.0098	-0.0098
TE ↓	setup_rising to CP	0.0782	0.1073	0.0517	0.0517
TE ↑	setup_rising to CP	0.0982	0.1275	0.0982	0.0982
TI ↓	hold_rising to CP	-0.0586	-0.0867	-0.0502	-0.0502
TI ↑	hold_rising to CP	-0.0104	-0.0049	-0.0120	-0.0120
TI ↓	setup_rising to CP	0.0981	0.1250	0.0945	0.0945
TI ↑	setup_rising to CP	0.0368	0.0355	0.0368	0.0368
		C8T28SOIDV_-LL_-SDFPQTX19_-P10	C8T28SOIDV_-LL_-SDFPQTX29_-P10		
CP ↓	min_pulse_width to CP	0.0815	0.0822		
CP ↑	min_pulse_width to CP	0.0404	0.0483		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	-0.0022	-0.0022		
D ↓	setup_rising to CP	0.0538	0.0570		
D ↑	setup_rising to CP	0.0271	0.0271		
TE ↓	hold_rising to CP	-0.0077	-0.0072		
TE ↑	hold_rising to CP	-0.0098	-0.0098		
TE ↓	setup_rising to CP	0.0517	0.0517		
TE ↑	setup_rising to CP	0.0982	0.1008		
TI ↓	hold_rising to CP	-0.0502	-0.0502		
TI ↑	hold_rising to CP	-0.0120	-0.0120		
TI ↓	setup_rising to CP	0.0945	0.0988		
TI ↑	setup_rising to CP	0.0368	0.0368		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P10	1.027e-06	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P10	9.486e-07	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P10	1.002e-06	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P10	1.333e-06	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P10	1.646e-06	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P10	2.133e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

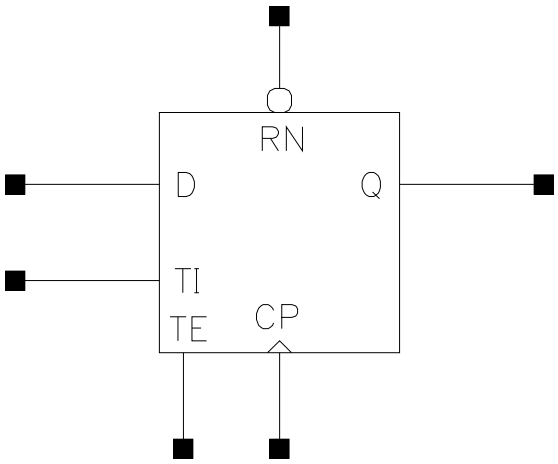
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P10	C8T28SOI_LLHF_-SDFPQTX3_P10	C8T28SOIDV_LL_-SDFPQTX5_P10	C8T28SOIDV_LL_-SDFPQTX10_P10
Clock 100Mhz Data 0Mhz	7.438e-03	7.267e-03	6.963e-03	6.804e-03
Clock 100Mhz Data 25Mhz	7.433e-03	7.212e-03	6.976e-03	7.313e-03
Clock 100Mhz Data 50Mhz	7.427e-03	7.157e-03	6.990e-03	7.823e-03
Clock = 0 Data 100Mhz	3.575e-03	3.705e-03	3.536e-03	3.448e-03
Clock = 1 Data 100Mhz	3.855e-05	5.017e-04	3.485e-04	2.719e-04
	C8T28SOIDV_LL_-SDFPQTX19_P10	C8T28SOIDV_LL_-SDFPQTX29_P10		
Clock 100Mhz Data 0Mhz	6.711e-03	6.654e-03		
Clock 100Mhz Data 25Mhz	7.821e-03	8.458e-03		
Clock 100Mhz Data 50Mhz	8.931e-03	1.026e-02		
Clock = 0 Data 100Mhz	3.394e-03	3.362e-03		
Clock = 1 Data 100Mhz	2.259e-04	1.953e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P10	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P10	C8T28SOI_LLHF_-SDFPRQX3_P10	C8T28SOIDV_LL_-SDFPRQX5_P10	C8T28SOIDV_LL_-SDFPRQX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P10	C8T28SOIDV_LL_-SDFPRQX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0009	0.0009		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P10	**C8T28SOI_LLHF_-SDFPRQX3_P10**	**C8T28SOI_LL_-SDFPRQX5_P10**	**C8T28SOI_LLHF_-SDFPRQX3_P10**
CP to Q ↓	0.0672	0.0611	3.2815	5.0099
CP to Q ↑	0.0582	0.0648	4.6078	7.0471
RN to Q ↓	0.0612	0.0600	3.0284	4.6882
	C8T28SOIDV_LL_-SDFPRQX5_P10	**C8T28SOIDV_LL_-SDFPRQX10_P10**	**C8T28SOIDV_LL_-SDFPRQX5_P10**	**C8T28SOIDV_LL_-SDFPRQX10_P10**
CP to Q ↓	0.0533	0.0749	3.0775	1.5077
CP to Q ↑	0.0680	0.0978	4.5522	2.2896
RN to Q ↓	0.0504	0.0773	3.0560	1.5070
	C8T28SOIDV_LL_-SDFPRQX19_P10	**C8T28SOIDV_LL_-SDFPRQX29_P10**	**C8T28SOIDV_LL_-SDFPRQX19_P10**	**C8T28SOIDV_LL_-SDFPRQX29_P10**
CP to Q ↓	0.0801	0.0815	0.7792	0.5329
CP to Q ↑	0.1027	0.1069	1.1740	0.7981
RN to Q ↓	0.0828	0.0842	0.7796	0.5324

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P10	C8T28SOI_-LLHF_-SDFPRQX3_P10	C8T28SOIDV_-LL_SDFPRQX5_-P10	C8T28SOIDV_-LL_-SDFPRQX10_-P10
CP ↓	min_pulse_width to CP	0.0978	0.0902	0.0857	0.0856
CP ↑	min_pulse_width to CP	0.0546	0.0454	0.0437	0.0438
D ↓	hold_rising to CP	-0.0441	-0.0897	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0120	-0.0120	-0.0022	-0.0017
D ↓	setup_rising to CP	0.0830	0.1315	0.0596	0.0596
D ↑	setup_rising to CP	0.0417	0.0417	0.0293	0.0293
RN ↓	min_pulse_width to RN	0.0664	0.0637	0.0588	0.0540
RN ↑	recovery_rising to CP	0.0076	0.0054	0.0054	0.0054

RN ↑	removal_rising to CP	0.0047	0.0047	0.0043	0.0047
TE ↓	hold_rising to CP	-0.0284	-0.0301	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0094	-0.0088	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.0814	0.1073	0.0539	0.0539
TE ↑	setup_rising to CP	0.0982	0.1275	0.0982	0.0982
TI ↓	hold_rising to CP	-0.0586	-0.0870	-0.0502	-0.0502
TI ↑	hold_rising to CP	-0.0120	-0.0107	-0.0120	-0.0117
TI ↓	setup_rising to CP	0.0981	0.1214	0.0945	0.0945
TI ↑	setup_rising to CP	0.0402	0.0353	0.0417	0.0417
		C8T28SOIDV_-LL_-SDFPRQX19_-P10	C8T28SOIDV_-LL_-SDFPRQX29_-P10		
CP ↓	min_pulse_width to CP	0.0857	0.0856		
CP ↑	min_pulse_width to CP	0.0438	0.0438		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	-0.0017	-0.0017		
D ↓	setup_rising to CP	0.0596	0.0591		
D ↑	setup_rising to CP	0.0293	0.0293		
RN ↓	min_pulse_width to RN	0.0540	0.0562		
RN ↑	recovery_rising to CP	0.0054	0.0059		
RN ↑	removal_rising to CP	0.0047	0.0043		
TE ↓	hold_rising to CP	-0.0072	-0.0072		
TE ↑	hold_rising to CP	-0.0120	-0.0120		
TE ↓	setup_rising to CP	0.0539	0.0571		
TE ↑	setup_rising to CP	0.0982	0.0982		
TI ↓	hold_rising to CP	-0.0502	-0.0502		
TI ↑	hold_rising to CP	-0.0117	-0.0110		
TI ↓	setup_rising to CP	0.0945	0.0988		
TI ↑	setup_rising to CP	0.0417	0.0417		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P10	1.073e-06	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P10	9.735e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P10	1.018e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P10	1.326e-06	1.000e-20

C8T28SOIDV_LL_SDFPRQX19_P10	1.661e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P10	2.086e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

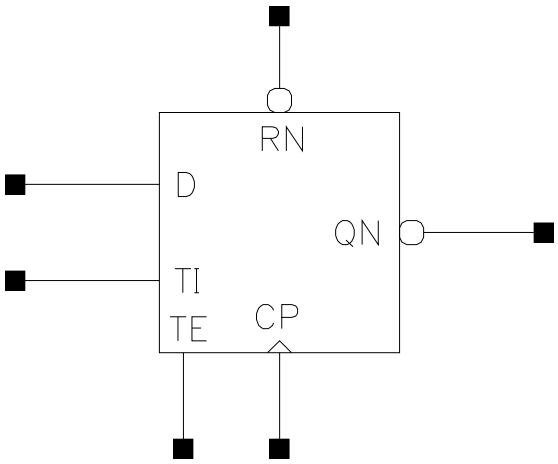
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P10	C8T28SOI_LLHF_-SDFPRQX3_P10	C8T28SOIDV_LL_-SDFPRQX5_P10	C8T28SOIDV_LL_-SDFPRQX10_P10
Clock 100Mhz Data 0Mhz	7.834e-03	7.543e-03	7.233e-03	7.079e-03
Clock 100Mhz Data 25Mhz	7.511e-03	7.277e-03	7.005e-03	7.390e-03
Clock 100Mhz Data 50Mhz	7.188e-03	7.012e-03	6.777e-03	7.701e-03
Clock = 0 Data 100Mhz	3.475e-03	3.636e-03	3.529e-03	3.476e-03
Clock = 1 Data 100Mhz	9.176e-05	5.307e-04	3.872e-04	3.155e-04
	C8T28SOIDV_LL_-SDFPRQX19_P10	C8T28SOIDV_LL_-SDFPRQX29_P10		
Clock 100Mhz Data 0Mhz	6.985e-03	6.925e-03		
Clock 100Mhz Data 25Mhz	7.864e-03	8.568e-03		
Clock 100Mhz Data 50Mhz	8.743e-03	1.021e-02		
Clock = 0 Data 100Mhz	3.443e-03	3.424e-03		
Clock = 1 Data 100Mhz	2.725e-04	2.439e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P10	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P10	C8T28SOI_LLHF_-SDFPRQNX3_P10	C8T28SOIDV_LL_-SDFPRQNX5_P10	C8T28SOIDV_LL_-SDFPRQNX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P10	C8T28SOIDV_LL_-SDFPRQNX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNX5_P10	**C8T28SOI_LLHF_-SDFPRQNX3_P10**	**C8T28SOI_LL_-SDFPRQNX5_P10**	**C8T28SOI_LLHF_-SDFPRQNX3_P10**
CP to QN ↓	0.0771	0.0820	3.2021	4.6721
CP to QN ↑	0.0712	0.0669	4.7553	6.9242
RN to QN ↑	0.0711	0.0698	4.7506	6.9088
	C8T28SOIDV_LL_-SDFPRQNX5_P10	**C8T28SOIDV_LL_-SDFPRQNX10_P10**	**C8T28SOIDV_LL_-SDFPRQNX5_P10**	**C8T28SOIDV_LL_-SDFPRQNX10_P10**
CP to QN ↓	0.0872	0.0791	2.9574	1.5084
CP to QN ↑	0.0659	0.0655	4.5044	2.2888
RN to QN ↑	0.0627	0.0632	4.5044	2.2894
	C8T28SOIDV_LL_-SDFPRQNX19_P10	**C8T28SOIDV_LL_-SDFPRQNX29_P10**	**C8T28SOIDV_LL_-SDFPRQNX19_P10**	**C8T28SOIDV_LL_-SDFPRQNX29_P10**
CP to QN ↓	0.0880	0.0936	0.7989	0.5361
CP to QN ↑	0.0726	0.0815	1.1777	0.7936
RN to QN ↑	0.0681	0.0786	1.1785	0.7929

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P10	C8T28SOI_-LLHF_-SDFPRQNX3_-P10	C8T28SOIDV_-LL_-SDFPRQNX5_-P10	C8T28SOIDV_-LL_-SDFPRQNX10_-P10
CP ↓	min_pulse_width to CP	0.0960	0.0902	0.0856	0.0856
CP ↑	min_pulse_width to CP	0.0438	0.0407	0.0438	0.0437
D ↓	hold_rising to CP	-0.0436	-0.0870	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0120	-0.0120	-0.0022	-0.0022
D ↓	setup_rising to CP	0.0830	0.1315	0.0596	0.0596
D ↑	setup_rising to CP	0.0385	0.0417	0.0265	0.0293
RN ↓	min_pulse_width to RN	0.0664	0.0637	0.0562	0.0610
RN ↑	recovery_rising to CP	0.0076	0.0054	0.0054	0.0054

RN ↑	removal_rising to CP	0.0047	0.0047	0.0043	0.0047
TE ↓	hold_rising to CP	-0.0284	-0.0301	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0094	-0.0088	-0.0093	-0.0120
TE ↓	setup_rising to CP	0.0782	0.1073	0.0539	0.0539
TE ↑	setup_rising to CP	0.0982	0.1275	0.0982	0.0982
TI ↓	hold_rising to CP	-0.0586	-0.0870	-0.0502	-0.0502
TI ↑	hold_rising to CP	-0.0120	-0.0107	-0.0120	-0.0120
TI ↓	setup_rising to CP	0.0981	0.1214	0.0945	0.0945
TI ↑	setup_rising to CP	0.0404	0.0353	0.0417	0.0417
		C8T28SOIDV_-LL_-SDFPRQNX19_-P10	C8T28SOIDV_-LL_-SDFPRQNX29_-P10		
CP ↓	min_pulse_width to CP	0.0863	0.0863		
CP ↑	min_pulse_width to CP	0.0483	0.0530		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	-0.0022	-0.0022		
D ↓	setup_rising to CP	0.0596	0.0596		
D ↑	setup_rising to CP	0.0265	0.0265		
RN ↓	min_pulse_width to RN	0.0632	0.0752		
RN ↑	recovery_rising to CP	0.0027	0.0027		
RN ↑	removal_rising to CP	0.0038	0.0038		
TE ↓	hold_rising to CP	-0.0077	-0.0045		
TE ↑	hold_rising to CP	-0.0093	-0.0093		
TE ↓	setup_rising to CP	0.0539	0.0539		
TE ↑	setup_rising to CP	0.0982	0.0982		
TI ↓	hold_rising to CP	-0.0509	-0.0496		
TI ↑	hold_rising to CP	-0.0120	-0.0120		
TI ↓	setup_rising to CP	0.0945	0.0945		
TI ↑	setup_rising to CP	0.0417	0.0417		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P10	1.057e-06	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P10	9.824e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P10	1.012e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P10	1.309e-06	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P10	1.550e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P10	1.979e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

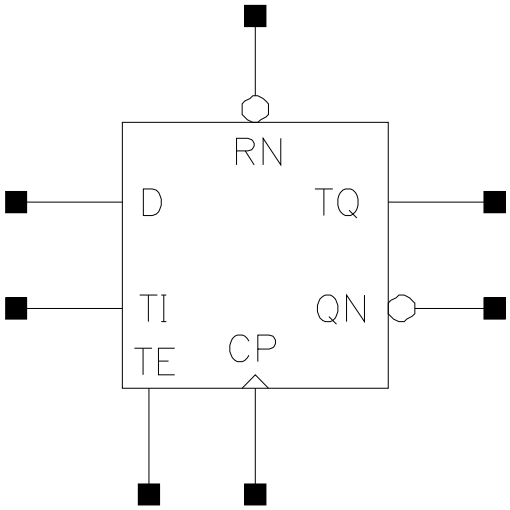
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P10	C8T28SOI_LLHF_-SDFPRQNX3_P10	C8T28SOIDV_LL_-SDFPRQNX5_P10	C8T28SOIDV_LL_-SDFPRQNX10_P10
Clock 100Mhz Data 0Mhz	7.539e-03	7.346e-03	7.007e-03	6.836e-03
Clock 100Mhz Data 25Mhz	7.289e-03	7.140e-03	6.912e-03	7.207e-03
Clock 100Mhz Data 50Mhz	7.038e-03	6.935e-03	6.816e-03	7.577e-03
Clock = 0 Data 100Mhz	3.479e-03	3.640e-03	3.552e-03	3.505e-03
Clock = 1 Data 100Mhz	4.844e-05	5.082e-04	3.552e-04	2.788e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P10	C8T28SOIDV_LL_-SDFPRQNX29_P10		
Clock 100Mhz Data 0Mhz	6.791e-03	6.788e-03		
Clock 100Mhz Data 25Mhz	7.741e-03	8.577e-03		
Clock 100Mhz Data 50Mhz	8.690e-03	1.037e-02		
Clock = 0 Data 100Mhz	3.473e-03	3.451e-03		
Clock = 1 Data 100Mhz	2.330e-04	2.024e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P10	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P10	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P10	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P10	C8T28SOI_LLHF_-SDFPRQNTX3_P10	C8T28SOIDV_LL_-SDFPRQNTX5_P10	C8T28SOIDV_LL_-SDFPRQNTX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P10	C8T28SOIDV_LL_-SDFPRQNTX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNTX5_P10	**C8T28SOI_LLHF_-SDFPRQNTX3_P10**	**C8T28SOI_LL_-SDFPRQNTX5_P10**	**C8T28SOI_LLHF_-SDFPRQNTX3_P10**
CP to QN ↓	0.0853	0.0892	3.1507	4.7328
CP to QN ↑	0.0895	0.0820	4.9949	6.9497
CP to TQ ↓	0.0760	0.0592	8.8050	5.5425
CP to TQ ↑	0.0713	0.0670	23.2980	12.5866
RN to QN ↑	0.0782	0.0755	4.9966	6.9834
RN to TQ ↓	0.0674	0.0594	8.5313	5.2968
	C8T28SOIDV_LL_-SDFPRQNTX5_P10	**C8T28SOIDV_LL_-SDFPRQNTX10_P10**	**C8T28SOIDV_LL_-SDFPRQNTX5_P10**	**C8T28SOIDV_LL_-SDFPRQNTX10_P10**
CP to QN ↓	0.0919	0.0974	2.9992	1.5615
CP to QN ↑	0.0724	0.0764	4.4894	2.2797
CP to TQ ↓	0.0506	0.0513	5.4849	5.5255
CP to TQ ↑	0.0687	0.0687	9.9358	9.9467
RN to QN ↑	0.0698	0.0743	4.4944	2.2781
RN to TQ ↓	0.0465	0.0476	5.4916	5.5353
	C8T28SOIDV_LL_-SDFPRQNTX19_P10	**C8T28SOIDV_LL_-SDFPRQNTX29_P10**	**C8T28SOIDV_LL_-SDFPRQNTX19_P10**	**C8T28SOIDV_LL_-SDFPRQNTX29_P10**
CP to QN ↓	0.0920	0.0938	0.7853	0.5361
CP to QN ↑	0.0786	0.0881	1.1537	0.7874
CP to TQ ↓	0.0554	0.0674	5.5798	6.3397
CP to TQ ↑	0.0730	0.0810	9.9664	11.4301
RN to QN ↑	0.0741	0.0842	1.1536	0.7861
RN to TQ ↓	0.0496	0.0624	5.5663	6.2305

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P10	C8T28SOI_-LLHF_-SDFPRQNTX3_-P10	C8T28SOIDV_-LL_-SDFPRQNTX5_-P10	C8T28SOIDV_-LL_SDF-PRQNTX10_P10
CP ↓	min_pulse_width to CP	0.0978	0.0902	0.0856	0.0856
CP ↑	min_pulse_width to CP	0.0546	0.0500	0.0437	0.0451
D ↓	hold_rising to CP	-0.0441	-0.0870	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0120	-0.0120	-0.0022	-0.0022
D ↓	setup_rising to CP	0.0830	0.1315	0.0596	0.0596
D ↑	setup_rising to CP	0.0385	0.0412	0.0265	0.0293
RN ↓	min_pulse_width to RN	0.0686	0.0659	0.0659	0.0659
RN ↑	recovery_rising to CP	0.0076	0.0054	0.0054	0.0054
RN ↑	removal_rising to CP	0.0047	0.0047	0.0043	0.0047
TE ↓	hold_rising to CP	-0.0284	-0.0301	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0094	-0.0088	-0.0093	-0.0120
TE ↓	setup_rising to CP	0.0782	0.1073	0.0539	0.0539
TE ↑	setup_rising to CP	0.0982	0.1275	0.0982	0.0982
TI ↓	hold_rising to CP	-0.0586	-0.0870	-0.0502	-0.0502
TI ↑	hold_rising to CP	-0.0104	-0.0107	-0.0120	-0.0120
TI ↓	setup_rising to CP	0.0981	0.1207	0.0988	0.0988
TI ↑	setup_rising to CP	0.0404	0.0353	0.0417	0.0417
		C8T28SOIDV_-LL_SDF-PRQNTX19_P10	C8T28SOIDV_-LL_SDF-PRQNTX29_P10		
CP ↓	min_pulse_width to CP	0.0863	0.0863		
CP ↑	min_pulse_width to CP	0.0483	0.0578		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	-0.0022	-0.0022		
D ↓	setup_rising to CP	0.0596	0.0596		
D ↑	setup_rising to CP	0.0265	0.0265		
RN ↓	min_pulse_width to RN	0.0681	0.0850		
RN ↑	recovery_rising to CP	0.0027	0.0059		
RN ↑	removal_rising to CP	0.0038	0.0038		
TE ↓	hold_rising to CP	-0.0077	-0.0077		
TE ↑	hold_rising to CP	-0.0120	-0.0093		

TE ↓	setup_rising to CP	0.0539	0.0539		
TE ↑	setup_rising to CP	0.0982	0.0982		
TI ↓	hold_rising to CP	-0.0509	-0.0509		
TI ↑	hold_rising to CP	-0.0120	-0.0120		
TI ↓	setup_rising to CP	0.0945	0.0945		
TI ↑	setup_rising to CP	0.0417	0.0417		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P10	1.080e-06	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P10	1.032e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P10	1.075e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_P10	1.203e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_P10	1.556e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_P10	2.031e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

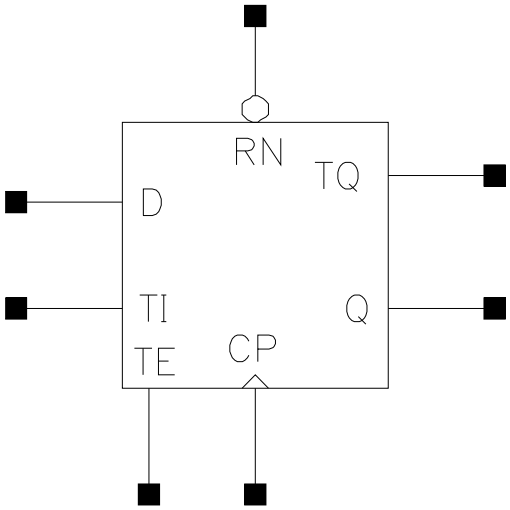
Pin Cycle	C8T28SOI_LL_SDFPRQNTX5_P10	C8T28SOI_LLHF_SDFPRQNTX3_P10	C8T28SOIDV_LL_SDFPRQNTX5_P10	C8T28SOIDV_LL_SDFPRQNTX10_P10
Clock 100Mhz Data 0Mhz	7.726e-03	7.497e-03	7.151e-03	6.967e-03
Clock 100Mhz Data 25Mhz	7.674e-03	7.441e-03	7.176e-03	7.283e-03
Clock 100Mhz Data 50Mhz	7.622e-03	7.385e-03	7.200e-03	7.599e-03
Clock = 0 Data 100Mhz	3.455e-03	3.629e-03	3.530e-03	3.476e-03
Clock = 1 Data 100Mhz	8.387e-05	5.294e-04	3.848e-04	3.123e-04
	C8T28SOIDV_LL_SDFPRQNTX19_P10	C8T28SOIDV_LL_SDFPRQNTX29_P10		
Clock 100Mhz Data 0Mhz	6.917e-03	6.875e-03		
Clock 100Mhz Data 25Mhz	7.808e-03	8.758e-03		
Clock 100Mhz Data 50Mhz	8.699e-03	1.064e-02		
Clock = 0 Data 100Mhz	3.443e-03	3.422e-03		
Clock = 1 Data 100Mhz	2.688e-04	2.398e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P10	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P10	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P10	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P10	C8T28SOI_LLHF_-SDFPRQTX3_P10	C8T28SOIDV_LL_-SDFPRQTX5_P10	C8T28SOIDV_LL_-SDFPRQTX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P10	C8T28SOIDV_LL_-SDFPRQTX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0009	0.0009		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQTX5_P10	**C8T28SOI_LLHF_-SDFPRQTX3_P10**	**C8T28SOI_LL_-SDFPRQTX5_P10**	**C8T28SOI_LLHF_-SDFPRQTX3_P10**
CP to Q ↓	0.0786	0.0681	3.5256	5.2060
CP to Q ↑	0.0627	0.0676	4.6489	7.2309
CP to TQ ↓	0.0935	0.0672	9.2588	5.7096
CP to TQ ↑	0.0791	0.0711	23.3461	12.7733
RN to Q ↓	0.0564	0.0630	3.3028	4.8249
RN to TQ ↓	0.0700	0.0628	8.9424	5.4081
	C8T28SOIDV_LL_-SDFPRQTX5_P10	**C8T28SOIDV_LL_-SDFPRQTX10_P10**	**C8T28SOIDV_LL_-SDFPRQTX5_P10**	**C8T28SOIDV_LL_-SDFPRQTX10_P10**
CP to Q ↓	0.0578	0.0762	3.1852	1.5337
CP to Q ↑	0.0703	0.0988	4.5980	2.2799
CP to TQ ↓	0.0586	0.0791	5.6428	5.4861
CP to TQ ↑	0.0729	0.1028	10.0900	10.0174
RN to Q ↓	0.0555	0.0793	3.1495	1.5327
RN to TQ ↓	0.0564	0.0822	5.6006	5.4867
	C8T28SOIDV_LL_-SDFPRQTX19_P10	**C8T28SOIDV_LL_-SDFPRQTX29_P10**	**C8T28SOIDV_LL_-SDFPRQTX19_P10**	**C8T28SOIDV_LL_-SDFPRQTX29_P10**
CP to Q ↓	0.0850	0.0822	0.8104	0.5425
CP to Q ↑	0.1054	0.1071	1.1600	0.7918
CP to TQ ↓	0.0893	0.0848	5.5488	5.4315
CP to TQ ↑	0.1111	0.1122	10.0174	10.3017
RN to Q ↓	0.0826	0.0849	0.8106	0.5430
RN to TQ ↓	0.0869	0.0875	5.5483	5.4329

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_-P10	C8T28SOI_-LLHF_-SDFPRQTX3_-P10	C8T28SOIDV_-LL_-SDFPRQTX5_-P10	C8T28SOIDV_-LL_-SDFPRQTX10_-P10
CP ↓	min_pulse_width to CP	0.0978	0.0902	0.0856	0.0856
CP ↑	min_pulse_width to CP	0.0641	0.0548	0.0484	0.0438
D ↓	hold_rising to CP	-0.0441	-0.0870	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0120	-0.0120	-0.0022	-0.0017
D ↓	setup_rising to CP	0.0830	0.1315	0.0596	0.0596
D ↑	setup_rising to CP	0.0385	0.0412	0.0293	0.0293
RN ↓	min_pulse_width to RN	0.0730	0.0637	0.0659	0.0540
RN ↑	recovery_rising to CP	0.0076	0.0054	0.0054	0.0059
RN ↑	removal_rising to CP	0.0047	0.0021	0.0043	0.0043
TE ↓	hold_rising to CP	-0.0284	-0.0301	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0094	-0.0088	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.0782	0.1073	0.0539	0.0539
TE ↑	setup_rising to CP	0.0982	0.1275	0.0982	0.0982
TI ↓	hold_rising to CP	-0.0586	-0.0870	-0.0502	-0.0502
TI ↑	hold_rising to CP	-0.0104	-0.0107	-0.0120	-0.0110
TI ↓	setup_rising to CP	0.0981	0.1207	0.0945	0.0945
TI ↑	setup_rising to CP	0.0402	0.0346	0.0417	0.0417
		C8T28SOIDV_-LL_-SDFPRQTX19_-P10	C8T28SOIDV_-LL_-SDFPRQTX29_-P10		
CP ↓	min_pulse_width to CP	0.0857	0.0856		
CP ↑	min_pulse_width to CP	0.0438	0.0438		
D ↓	hold_rising to CP	-0.0094	-0.0094		
D ↑	hold_rising to CP	-0.0017	-0.0017		
D ↓	setup_rising to CP	0.0596	0.0591		
D ↑	setup_rising to CP	0.0293	0.0293		
RN ↓	min_pulse_width to RN	0.0562	0.0562		
RN ↑	recovery_rising to CP	0.0059	0.0059		
RN ↑	removal_rising to CP	0.0043	0.0043		
TE ↓	hold_rising to CP	-0.0072	-0.0072		
TE ↑	hold_rising to CP	-0.0120	-0.0120		

TE ↓	setup_rising to CP	0.0539	0.0571		
TE ↑	setup_rising to CP	0.0982	0.0982		
TI ↓	hold_rising to CP	-0.0502	-0.0502		
TI ↑	hold_rising to CP	-0.0117	-0.0110		
TI ↓	setup_rising to CP	0.0945	0.0988		
TI ↑	setup_rising to CP	0.0417	0.0417		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P10	1.106e-06	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P10	1.027e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P10	1.081e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P10	1.392e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P10	1.696e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P10	2.149e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

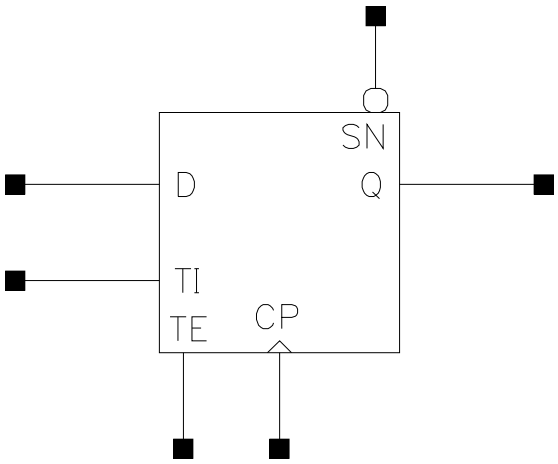
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P10	C8T28SOI_LLHF_-SDFPRQTX3_P10	C8T28SOIDV_LL_-SDFPRQTX5_P10	C8T28SOIDV_LL_-SDFPRQTX10_P10
Clock 100Mhz Data 0Mhz	7.817e-03	7.509e-03	7.212e-03	7.064e-03
Clock 100Mhz Data 25Mhz	7.754e-03	7.426e-03	7.155e-03	7.578e-03
Clock 100Mhz Data 50Mhz	7.691e-03	7.344e-03	7.097e-03	8.091e-03
Clock = 0 Data 100Mhz	3.462e-03	3.634e-03	3.528e-03	3.475e-03
Clock = 1 Data 100Mhz	3.010e-05	5.026e-04	3.461e-04	2.679e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P10	C8T28SOIDV_LL_-SDFPRQTX29_P10		
Clock 100Mhz Data 0Mhz	6.974e-03	6.916e-03		
Clock 100Mhz Data 25Mhz	8.051e-03	8.667e-03		
Clock 100Mhz Data 50Mhz	9.127e-03	1.042e-02		
Clock = 0 Data 100Mhz	3.444e-03	3.424e-03		
Clock = 1 Data 100Mhz	2.210e-04	1.898e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P10	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P10	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P10	C8T28SOI_LLHF_-SDFPSQX3_P10	C8T28SOIDV_LL_-SDFPSQX5_P10	C8T28SOIDV_LL_-SDFPSQX10_P10
CP	0.0007	0.0007	0.0005	0.0006
D	0.0003	0.0005	0.0004	0.0004
SN	0.0013	0.0014	0.0010	0.0011
TE	0.0010	0.0010	0.0010	0.0010
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQX14_P10	C8T28SOIDV_LL_-SDFPSQX19_P10	C8T28SOIDV_LL_-SDFPSQX29_P10	
CP	0.0006	0.0006	0.0006	
D	0.0004	0.0004	0.0004	
SN	0.0011	0.0011	0.0011	
TE	0.0010	0.0010	0.0010	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P10	**C8T28SOI_LLHF_-SDFPSQX3_P10**	**C8T28SOI_LL_-SDFPSQX5_P10**	**C8T28SOI_LLHF_-SDFPSQX3_P10**
CP to Q ↓	0.0695	0.0620	3.3682	5.1026
CP to Q ↑	0.0597	0.0661	4.6365	7.0692
SN to Q ↑	0.0497	0.0453	4.5825	6.9915
	C8T28SOIDV_LL_-SDFPSQX5_P10	**C8T28SOIDV_LL_-SDFPSQX10_P10**	**C8T28SOIDV_LL_-SDFPSQX5_P10**	**C8T28SOIDV_LL_-SDFPSQX10_P10**
CP to Q ↓	0.0524	0.0755	3.0761	1.4753
CP to Q ↑	0.0649	0.1045	4.5534	2.2719
SN to Q ↑	0.0453	0.0826	4.5404	2.2721
	C8T28SOIDV_LL_-SDFPSQX14_P10	**C8T28SOIDV_LL_-SDFPSQX19_P10**	**C8T28SOIDV_LL_-SDFPSQX14_P10**	**C8T28SOIDV_LL_-SDFPSQX19_P10**
CP to Q ↓	0.0761	0.0808	1.0153	0.7855
CP to Q ↑	0.1045	0.1082	1.5287	1.1535
SN to Q ↑	0.0823	0.0860	1.5288	1.1541
	C8T28SOIDV_LL_-SDFPSQX29_P10		**C8T28SOIDV_LL_-SDFPSQX29_P10**	
CP to Q ↓	0.0804		0.5325	
CP to Q ↑	0.1135		0.7659	
SN to Q ↑	0.0913		0.7662	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P10	C8T28SOI_-LLHF_-SDFPSQX3_P10	C8T28SOIDV_-LL_SDFPSQX5_-P10	C8T28SOIDV_-LL_-SDFPSQX10_-P10
CP ↓	min_pulse_width to CP	0.1025	0.1045	0.0887	0.0904
CP ↑	min_pulse_width to CP	0.0594	0.0454	0.0437	0.0438
D ↓	hold_rising to CP	-0.0458	-0.0942	-0.0197	-0.0246
D ↑	hold_rising to CP	-0.0088	-0.0094	-0.0013	-0.0013
D ↓	setup_rising to CP	0.0879	0.1435	0.0635	0.0684
D ↑	setup_rising to CP	0.0368	0.0417	0.0320	0.0320

SN ↓	min_pulse_width to SN	0.0474	0.0425	0.0403	0.0425
SN ↑	recovery_rising to CP	0.0085	0.0106	0.0009	-0.0017
SN ↑	removal_rising to CP	0.0206	0.0287	0.0303	0.0362
TE ↓	hold_rising to CP	-0.0289	-0.0311	-0.0143	-0.0192
TE ↑	hold_rising to CP	-0.0098	-0.0067	0.0010	-0.0066
TE ↓	setup_rising to CP	0.0857	0.1170	0.0640	0.0668
TE ↑	setup_rising to CP	0.1052	0.1372	0.1008	0.0955
TI ↓	hold_rising to CP	-0.0635	-0.0918	-0.0488	-0.0453
TI ↑	hold_rising to CP	-0.0064	-0.0049	-0.0000	-0.0064
TI ↓	setup_rising to CP	0.1027	0.1348	0.0945	0.0940
TI ↑	setup_rising to CP	0.0368	0.0355	0.0306	0.0368
		C8T28SOIDV_-LL_-SDFPSQX14_-P10	C8T28SOIDV_-LL_-SDFPSQX19_-P10	C8T28SOIDV_-LL_-SDFPSQX29_-P10	
CP ↓	min_pulse_width to CP	0.0904	0.0904	0.0904	
CP ↑	min_pulse_width to CP	0.0404	0.0404	0.0438	
D ↓	hold_rising to CP	-0.0246	-0.0246	-0.0246	
D ↑	hold_rising to CP	-0.0013	-0.0013	-0.0013	
D ↓	setup_rising to CP	0.0684	0.0684	0.0684	
D ↑	setup_rising to CP	0.0320	0.0320	0.0320	
SN ↓	min_pulse_width to SN	0.0425	0.0425	0.0452	
SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	
SN ↑	removal_rising to CP	0.0362	0.0362	0.0362	
TE ↓	hold_rising to CP	-0.0192	-0.0192	-0.0192	
TE ↑	hold_rising to CP	-0.0066	-0.0066	-0.0066	
TE ↓	setup_rising to CP	0.0668	0.0668	0.0668	
TE ↑	setup_rising to CP	0.0955	0.0955	0.0955	
TI ↓	hold_rising to CP	-0.0453	-0.0453	-0.0453	
TI ↑	hold_rising to CP	-0.0064	-0.0064	-0.0064	
TI ↓	setup_rising to CP	0.0940	0.0940	0.0940	
TI ↑	setup_rising to CP	0.0368	0.0368	0.0368	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds

C8T28SOI_LL_SDFPSQX5_P10	1.093e-06	1.000e-20
C8T28SOI_LLHF_SDFPSQX3_P10	1.006e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P10	1.051e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P10	1.385e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P10	1.551e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P10	1.749e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P10	2.127e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

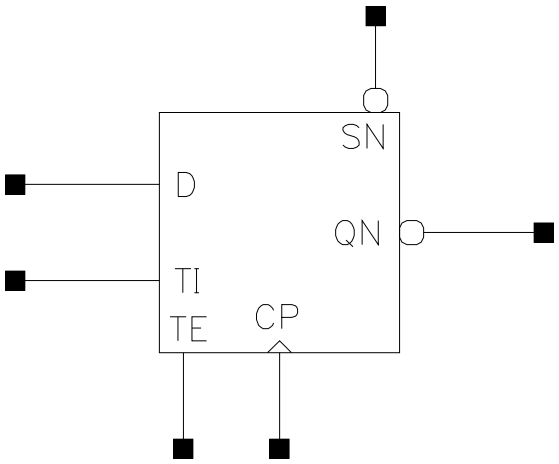
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P10	C8T28SOI_LLHF_-SDFPSQX3_P10	C8T28SOIDV_LL_-SDFPSQX5_P10	C8T28SOIDV_LL_-SDFPSQX10_P10
Clock 100Mhz Data 0Mhz	7.496e-03	7.260e-03	6.955e-03	6.810e-03
Clock 100Mhz Data 25Mhz	7.409e-03	7.117e-03	6.782e-03	7.270e-03
Clock 100Mhz Data 50Mhz	7.322e-03	6.974e-03	6.608e-03	7.731e-03
Clock = 0 Data 100Mhz	3.577e-03	3.734e-03	3.657e-03	3.639e-03
Clock = 1 Data 100Mhz	5.041e-05	5.069e-04	3.537e-04	2.774e-04
	C8T28SOIDV_LL_-SDFPSQX14_P10	C8T28SOIDV_LL_-SDFPSQX19_P10	C8T28SOIDV_LL_-SDFPSQX29_P10	
Clock 100Mhz Data 0Mhz	6.723e-03	6.664e-03	6.623e-03	
Clock 100Mhz Data 25Mhz	7.421e-03	7.770e-03	8.249e-03	
Clock 100Mhz Data 50Mhz	8.119e-03	8.876e-03	9.876e-03	
Clock = 0 Data 100Mhz	3.628e-03	3.621e-03	3.616e-03	
Clock = 1 Data 100Mhz	2.315e-04	2.010e-04	1.792e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P10	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P10	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P10	C8T28SOI_LLHF_-SDFPSQNX3_P10	C8T28SOIDV_LL_-SDFPSQNX5_P10	C8T28SOIDV_LL_-SDFPSQNX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0005	0.0004	0.0004
SN	0.0013	0.0013	0.0011	0.0011
TE	0.0010	0.0010	0.0010	0.0010
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNX14_P10	C8T28SOIDV_LL_-SDFPSQNX19_P10	C8T28SOIDV_LL_-SDFPSQNX23_P10	C8T28SOIDV_LL_-SDFPSQNX29_P10
CP	0.0005	0.0005	0.0005	0.0005
D	0.0004	0.0004	0.0004	0.0004
SN	0.0011	0.0011	0.0011	0.0010
TE	0.0010	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNX5_P10	**C8T28SOI_LLHF_-SDFPSQNX3_P10**	**C8T28SOI_LL_-SDFPSQNX5_P10**	**C8T28SOI_LLHF_-SDFPSQNX3_P10**
CP to QN ↓	0.0810	0.0820	3.2858	4.6534
CP to QN ↑	0.0756	0.0700	4.8331	6.9340
SN to QN ↓	0.0721	0.0620	3.2886	4.6519
	C8T28SOIDV_LL_-SDFPSQNX5_P10	**C8T28SOIDV_LL_-SDFPSQNX10_P10**	**C8T28SOIDV_LL_-SDFPSQNX5_P10**	**C8T28SOIDV_LL_-SDFPSQNX10_P10**
CP to QN ↓	0.0869	0.0813	2.9455	1.4939
CP to QN ↑	0.0689	0.0709	4.5075	2.2551
SN to QN ↓	0.0665	0.0593	2.9415	1.4934
	C8T28SOIDV_LL_-SDFPSQNX14_P10	**C8T28SOIDV_LL_-SDFPSQNX19_P10**	**C8T28SOIDV_LL_-SDFPSQNX14_P10**	**C8T28SOIDV_LL_-SDFPSQNX19_P10**
CP to QN ↓	0.0845	0.0867	1.0023	0.7663
CP to QN ↑	0.0731	0.0755	1.5152	1.1411
SN to QN ↓	0.0610	0.0640	1.0013	0.7660
	C8T28SOIDV_LL_-SDFPSQNX23_P10	**C8T28SOIDV_LL_-SDFPSQNX29_P10**	**C8T28SOIDV_LL_-SDFPSQNX23_P10**	**C8T28SOIDV_LL_-SDFPSQNX29_P10**
CP to QN ↓	0.0878	0.0848	0.6084	0.5263
CP to QN ↑	0.0752	0.0769	1.1365	0.7655
SN to QN ↓	0.0657	0.0655	0.6079	0.5261

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P10	C8T28SOI_-LLHF_-SDFPSQNX3_-P10	C8T28SOIDV_-LL_-SDFPSQNX5_-P10	C8T28SOIDV_-LL_-SDFPSQNX10_-P10
CP ↓	min_pulse_width to CP	0.1025	0.1045	0.0887	0.0928
CP ↑	min_pulse_width to CP	0.0452	0.0407	0.0437	0.0451
D ↓	hold_rising to CP	-0.0490	-0.0942	-0.0197	-0.0143
D ↑	hold_rising to CP	-0.0120	-0.0094	-0.0013	-0.0017
D ↓	setup_rising to CP	0.0879	0.1435	0.0635	0.0635

D ↑	setup_rising to CP	0.0368	0.0417	0.0320	0.0320
SN ↓	min_pulse_width to SN	0.0474	0.0398	0.0403	0.0425
SN ↑	recovery_rising to CP	0.0053	0.0106	-0.0017	0.0009
SN ↑	removal_rising to CP	0.0206	0.0287	0.0303	0.0358
TE ↓	hold_rising to CP	-0.0289	-0.0311	-0.0143	-0.0147
TE ↑	hold_rising to CP	-0.0098	-0.0067	0.0010	0.0010
TE ↓	setup_rising to CP	0.0857	0.1170	0.0640	0.0668
TE ↑	setup_rising to CP	0.1057	0.1372	0.1008	0.1008
TI ↓	hold_rising to CP	-0.0635	-0.0916	-0.0486	-0.0496
TI ↑	hold_rising to CP	-0.0064	-0.0049	-0.0000	-0.0000
TI ↓	setup_rising to CP	0.1027	0.1348	0.0945	0.0945
TI ↑	setup_rising to CP	0.0368	0.0355	0.0306	0.0306
		C8T28SOIDV_-LL_-SDFPSQNX14_-P10	C8T28SOIDV_-LL_-SDFPSQNX19_-P10	C8T28SOIDV_-LL_-SDFPSQNX23_-P10	C8T28SOIDV_-LL_-SDFPSQNX29_-P10
CP ↓	min_pulse_width to CP	0.0928	0.0928	0.0928	0.0887
CP ↑	min_pulse_width to CP	0.0483	0.0483	0.0483	0.0497
D ↓	hold_rising to CP	-0.0143	-0.0143	-0.0143	-0.0197
D ↑	hold_rising to CP	-0.0017	-0.0013	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0635	0.0635	0.0635	0.0635
D ↑	setup_rising to CP	0.0320	0.0320	0.0320	0.0320
SN ↓	min_pulse_width to SN	0.0425	0.0425	0.0452	0.0452
SN ↑	recovery_rising to CP	0.0009	0.0009	0.0009	0.0009
SN ↑	removal_rising to CP	0.0358	0.0358	0.0358	0.0303
TE ↓	hold_rising to CP	-0.0147	-0.0147	-0.0147	-0.0143
TE ↑	hold_rising to CP	0.0010	0.0010	0.0010	0.0010
TE ↓	setup_rising to CP	0.0668	0.0668	0.0668	0.0640
TE ↑	setup_rising to CP	0.1008	0.1008	0.1008	0.1008
TI ↓	hold_rising to CP	-0.0496	-0.0496	-0.0496	-0.0488
TI ↑	hold_rising to CP	-0.0000	-0.0000	-0.0000	-0.0000
TI ↓	setup_rising to CP	0.0945	0.0945	0.0945	0.0988
TI ↑	setup_rising to CP	0.0306	0.0306	0.0306	0.0306

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P10	1.093e-06	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P10	1.004e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P10	1.071e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P10	1.433e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P10	1.564e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P10	1.762e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P10	1.872e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P10	2.221e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

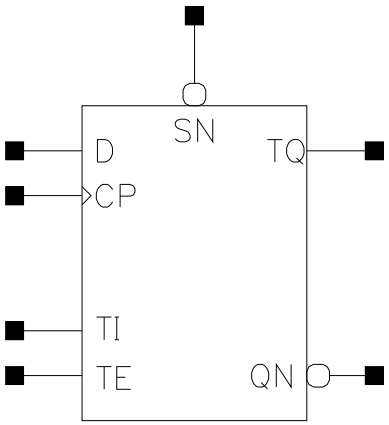
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P10	C8T28SOI_LLHF_-SDFPSQNX3_P10	C8T28SOIDV_LL_-SDFPSQNX5_P10	C8T28SOIDV_LL_-SDFPSQNX10_P10
Clock 100Mhz Data 0Mhz	7.483e-03	7.246e-03	6.909e-03	6.801e-03
Clock 100Mhz Data 25Mhz	7.338e-03	7.085e-03	6.876e-03	7.308e-03
Clock 100Mhz Data 50Mhz	7.193e-03	6.923e-03	6.842e-03	7.814e-03
Clock = 0 Data 100Mhz	3.575e-03	3.734e-03	3.657e-03	3.622e-03
Clock = 1 Data 100Mhz	7.454e-05	5.190e-04	3.716e-04	2.980e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P10	C8T28SOIDV_LL_-SDFPSQNX19_P10	C8T28SOIDV_LL_-SDFPSQNX23_P10	C8T28SOIDV_LL_-SDFPSQNX29_P10
Clock 100Mhz Data 0Mhz	6.734e-03	6.691e-03	6.660e-03	6.613e-03
Clock 100Mhz Data 25Mhz	7.491e-03	7.689e-03	7.767e-03	8.272e-03
Clock 100Mhz Data 50Mhz	8.248e-03	8.687e-03	8.873e-03	9.932e-03
Clock = 0 Data 100Mhz	3.601e-03	3.587e-03	3.577e-03	3.569e-03
Clock = 1 Data 100Mhz	2.538e-04	2.244e-04	2.034e-04	1.876e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P10	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P10	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P10	C8T28SOI_LLHF_-SDFPSQNTX3_P10	C8T28SOIDV_LL_-SDFPSQNTX5_P10	C8T28SOIDV_LL_-SDFPSQNTX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0005	0.0004	0.0004
SN	0.0013	0.0014	0.0010	0.0010
TE	0.0010	0.0010	0.0010	0.0010
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNTX19_P10	C8T28SOIDV_LL_-SDFPSQNTX23_P10	C8T28SOIDV_LL_-SDFPSQNTX29_P10	
CP	0.0005	0.0005	0.0005	
D	0.0004	0.0004	0.0004	
SN	0.0010	0.0010	0.0010	
TE	0.0010	0.0010	0.0010	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P10	**C8T28SOI_LLHF_-SDFPSQNTX3_P10**	**C8T28SOI_LL_-SDFPSQNTX5_P10**	**C8T28SOI_LLHF_-SDFPSQNTX3_P10**
CP to QN ↓	0.0884	0.0882	3.3395	4.7036
CP to QN ↑	0.0891	0.0832	4.7585	6.9616
CP to TQ ↓	0.0742	0.0600	8.7059	5.5862
CP to TQ ↑	0.0730	0.0684	23.2976	12.5961
SN to QN ↓	0.0768	0.0662	3.3406	4.7116
SN to TQ ↑	0.0620	0.0474	23.2530	12.5465
	C8T28SOIDV_LL_-SDFPSQNTX5_P10	**C8T28SOIDV_LL_-SDFPSQNTX10_P10**	**C8T28SOIDV_LL_-SDFPSQNTX5_P10**	**C8T28SOIDV_LL_-SDFPSQNTX10_P10**
CP to QN ↓	0.0873	0.0820	3.0054	1.4840
CP to QN ↑	0.0717	0.0761	4.5100	2.2691
CP to TQ ↓	0.0510	0.0592	5.5415	5.6235
CP to TQ ↑	0.0661	0.0694	10.7773	10.8554
SN to QN ↓	0.0660	0.0620	3.0097	1.4857
SN to TQ ↑	0.0448	0.0495	10.7651	10.8019
	C8T28SOIDV_LL_-SDFPSQNTX19_P10	**C8T28SOIDV_LL_-SDFPSQNTX23_P10**	**C8T28SOIDV_LL_-SDFPSQNTX19_P10**	**C8T28SOIDV_LL_-SDFPSQNTX23_P10**
CP to QN ↓	0.0871	0.0892	0.7604	0.6067
CP to QN ↑	0.0812	0.0804	1.1466	1.1380
CP to TQ ↓	0.0591	0.0600	5.6179	5.6677
CP to TQ ↑	0.0694	0.0702	10.8574	10.8733
SN to QN ↓	0.0670	0.0690	0.7600	0.6061
SN to TQ ↑	0.0494	0.0502	10.8036	10.8134
	C8T28SOIDV_LL_-SDFPSQNTX29_P10		**C8T28SOIDV_LL_-SDFPSQNTX29_P10**	
CP to QN ↓	0.0887		0.5275	
CP to QN ↑	0.0827		0.7664	

CP to TQ ↓	0.0629		5.7802	
CP to TQ ↑	0.0745		12.5339	
SN to QN ↓	0.0685		0.5269	
SN to TQ ↑	0.0544		12.4699	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P10	C8T28SOI_-LLHF_-SDFPSQNTX3_-P10	C8T28SOIDV_-LL_-SDFPSQNTX5_-P10	C8T28SOIDV_-LL_SDFP-SQNTX10_P10
CP ↓	min_pulse_width to CP	0.1038	0.1045	0.0887	0.0904
CP ↑	min_pulse_width to CP	0.0546	0.0500	0.0437	0.0497
D ↓	hold_rising to CP	-0.0485	-0.0942	-0.0197	-0.0197
D ↑	hold_rising to CP	-0.0088	-0.0094	-0.0013	-0.0017
D ↓	setup_rising to CP	0.0905	0.1435	0.0635	0.0635
D ↑	setup_rising to CP	0.0368	0.0417	0.0320	0.0320
SN ↓	min_pulse_width to SN	0.0522	0.0425	0.0425	0.0452
SN ↑	recovery_rising to CP	0.0106	0.0106	-0.0017	0.0005
SN ↑	removal_rising to CP	0.0212	0.0287	0.0303	0.0303
TE ↓	hold_rising to CP	-0.0289	-0.0305	-0.0143	-0.0143
TE ↑	hold_rising to CP	-0.0098	-0.0067	0.0010	0.0010
TE ↓	setup_rising to CP	0.0880	0.1170	0.0640	0.0636
TE ↑	setup_rising to CP	0.1079	0.1372	0.1008	0.1008
TI ↓	hold_rising to CP	-0.0632	-0.0918	-0.0488	-0.0488
TI ↑	hold_rising to CP	-0.0064	-0.0049	-0.0000	-0.0000
TI ↓	setup_rising to CP	0.1079	0.1348	0.0945	0.0988
TI ↑	setup_rising to CP	0.0368	0.0355	0.0306	0.0306
		C8T28SOIDV_-LL_SDFP-SQNTX19_P10	C8T28SOIDV_-LL_SDFP-SQNTX23_P10	C8T28SOIDV_-LL_SDFP-SQNTX29_P10	
CP ↓	min_pulse_width to CP	0.0904	0.0887	0.0887	
CP ↑	min_pulse_width to CP	0.0531	0.0531	0.0530	
D ↓	hold_rising to CP	-0.0197	-0.0197	-0.0197	
D ↑	hold_rising to CP	-0.0013	-0.0017	-0.0017	
D ↓	setup_rising to CP	0.0635	0.0635	0.0635	
D ↑	setup_rising to CP	0.0320	0.0320	0.0320	
SN ↓	min_pulse_width to SN	0.0452	0.0452	0.0479	

SN ↑	recovery_rising to CP	0.0005	0.0005	0.0005	
SN ↑	removal_rising to CP	0.0303	0.0303	0.0303	
TE ↓	hold_rising to CP	-0.0143	-0.0143	-0.0143	
TE ↑	hold_rising to CP	0.0010	0.0010	0.0010	
TE ↓	setup_rising to CP	0.0636	0.0640	0.0640	
TE ↑	setup_rising to CP	0.1008	0.1008	0.1008	
TI ↓	hold_rising to CP	-0.0488	-0.0488	-0.0488	
TI ↑	hold_rising to CP	-0.0000	-0.0000	-0.0000	
TI ↓	setup_rising to CP	0.0988	0.0988	0.0988	
TI ↑	setup_rising to CP	0.0306	0.0306	0.0306	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P10	1.104e-06	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P10	1.070e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P10	1.147e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_-P10	1.501e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_-P10	1.840e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_-P10	1.960e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_-P10	2.281e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P10	C8T28SOI_LLHF_-SDFPSQNTX3_P10	C8T28SOIDV_LL_-SDFPSQNTX5_P10	C8T28SOIDV_LL_-SDFPSQNTX10_P10
Clock 100Mhz Data 0Mhz	7.493e-03	7.252e-03	6.996e-03	6.869e-03
Clock 100Mhz Data 25Mhz	7.557e-03	7.291e-03	7.022e-03	7.469e-03
Clock 100Mhz Data 50Mhz	7.621e-03	7.330e-03	7.048e-03	8.070e-03
Clock = 0 Data 100Mhz	3.569e-03	3.730e-03	3.650e-03	3.610e-03
Clock = 1 Data 100Mhz	3.937e-05	5.023e-04	3.486e-04	2.717e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P10	C8T28SOIDV_LL_-SDFPSQNTX23_P10	C8T28SOIDV_LL_-SDFPSQNTX29_P10	
Clock 100Mhz Data 0Mhz	6.793e-03	6.742e-03	6.707e-03	
Clock 100Mhz Data 25Mhz	7.870e-03	7.965e-03	8.478e-03	
Clock 100Mhz Data 50Mhz	8.948e-03	9.187e-03	1.025e-02	

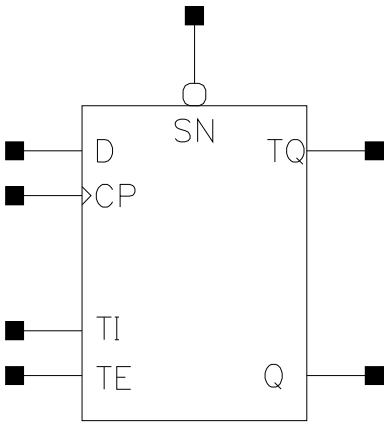
Clock = 0 Data 100Mhz	3.587e-03	3.571e-03	3.561e-03	
Clock = 1 Data 100Mhz	2.257e-04	1.949e-04	1.731e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P10	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P10	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P10	C8T28SOI_LLHF_-SDFPSQTX3_P10	C8T28SOIDV_LL_-SDFPSQTX5_P10	C8T28SOIDV_LL_-SDFPSQTX10_P10
CP	0.0007	0.0007	0.0005	0.0006
D	0.0003	0.0005	0.0003	0.0004
SN	0.0013	0.0014	0.0010	0.0011
TE	0.0010	0.0010	0.0010	0.0010
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQTX19_P10	C8T28SOIDV_LL_-SDFPSQTX29_P10		
CP	0.0006	0.0006		
D	0.0004	0.0004		
SN	0.0011	0.0011		
TE	0.0010	0.0010		
TI	0.0004	0.0004		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPSQTX5_P10	**C8T28SOI_LLHF_-SDFPSQTX3_P10**	**C8T28SOI_LL_-SDFPSQTX5_P10**	**C8T28SOI_LLHF_-SDFPSQTX3_P10**
CP to Q ↓	0.0756	0.0689	3.5603	5.2793
CP to Q ↑	0.0631	0.0689	4.6521	7.2373
CP to TQ ↓	0.0907	0.0678	9.2062	5.7647
CP to TQ ↑	0.0800	0.0723	23.3201	12.7819
SN to Q ↑	0.0521	0.0474	4.5859	7.1496
SN to TQ ↑	0.0669	0.0504	23.2590	12.7162
	C8T28SOIDV_LL_-SDFPSQTX5_P10	**C8T28SOIDV_LL_-SDFPSQTX10_P10**	**C8T28SOIDV_LL_-SDFPSQTX5_P10**	**C8T28SOIDV_LL_-SDFPSQTX10_P10**
CP to Q ↓	0.0586	0.0747	3.1708	1.5207
CP to Q ↑	0.0677	0.1035	4.6161	2.2965
CP to TQ ↓	0.0598	0.0770	5.6394	5.6853
CP to TQ ↑	0.0697	0.1076	10.9099	10.7580
SN to Q ↑	0.0477	0.0813	4.6056	2.2953
SN to TQ ↑	0.0497	0.0854	10.8633	10.7602
	C8T28SOIDV_LL_-SDFPSQTX19_P10	**C8T28SOIDV_LL_-SDFPSQTX29_P10**	**C8T28SOIDV_LL_-SDFPSQTX19_P10**	**C8T28SOIDV_LL_-SDFPSQTX29_P10**
CP to Q ↓	0.0812	0.0913	0.7921	0.5187
CP to Q ↑	0.1092	0.1186	1.1797	0.7811
CP to TQ ↓	0.0822	0.0518	4.9004	5.0814
CP to TQ ↑	0.1142	0.0725	12.4641	12.5465
SN to Q ↑	0.0869	0.0961	1.1797	0.7816
SN to TQ ↑	0.0918	0.0505	12.4656	12.5350

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_-P10	C8T28SOI_-LLHF_-SDFPSQTX3_-P10	C8T28SOIDV_-LL_-SDFPSQTX5_-P10	C8T28SOIDV_-LL_-SDFPSQTX10_-P10
CP ↓	min_pulse_width to CP	0.1038	0.1045	0.0904	0.0911
CP ↑	min_pulse_width to CP	0.0642	0.0548	0.0484	0.0404
D ↓	hold_rising to CP	-0.0490	-0.0942	-0.0197	-0.0246
D ↑	hold_rising to CP	-0.0088	-0.0094	-0.0017	-0.0013
D ↓	setup_rising to CP	0.0937	0.1435	0.0635	0.0684
D ↑	setup_rising to CP	0.0368	0.0417	0.0320	0.0320
SN ↓	min_pulse_width to SN	0.0522	0.0425	0.0425	0.0425
SN ↑	recovery_rising to CP	0.0106	0.0106	0.0005	-0.0017
SN ↑	removal_rising to CP	0.0212	0.0287	0.0303	0.0362
TE ↓	hold_rising to CP	-0.0256	-0.0311	-0.0143	-0.0192
TE ↑	hold_rising to CP	-0.0098	-0.0067	0.0010	-0.0066
TE ↓	setup_rising to CP	0.0880	0.1170	0.0636	0.0668
TE ↑	setup_rising to CP	0.1079	0.1372	0.1008	0.0955
TI ↓	hold_rising to CP	-0.0632	-0.0918	-0.0488	-0.0496
TI ↑	hold_rising to CP	-0.0064	-0.0049	-0.0000	-0.0064
TI ↓	setup_rising to CP	0.1079	0.1348	0.0988	0.0932
TI ↑	setup_rising to CP	0.0368	0.0355	0.0306	0.0368

		C8T28SOIDV_-LL_-SDFPSQTX19_-P10	C8T28SOIDV_-LL_-SDFPSQTX29_-P10		
CP ↓	min_pulse_width to CP	0.0904	0.0911		
CP ↑	min_pulse_width to CP	0.0404	0.0485		
D ↓	hold_rising to CP	-0.0246	-0.0246		
D ↑	hold_rising to CP	-0.0013	-0.0013		
D ↓	setup_rising to CP	0.0684	0.0684		
D ↑	setup_rising to CP	0.0320	0.0320		
SN ↓	min_pulse_width to SN	0.0425	0.0500		
SN ↑	recovery_rising to CP	-0.0017	-0.0017		
SN ↑	removal_rising to CP	0.0362	0.0362		
TE ↓	hold_rising to CP	-0.0192	-0.0192		
TE ↑	hold_rising to CP	-0.0066	-0.0066		

TE ↓	setup_rising to CP	0.0668	0.0668		
TE ↑	setup_rising to CP	0.0955	0.0955		
TI ↓	hold_rising to CP	-0.0453	-0.0453		
TI ↑	hold_rising to CP	-0.0064	-0.0064		
TI ↓	setup_rising to CP	0.0940	0.0940		
TI ↑	setup_rising to CP	0.0368	0.0368		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P10	1.103e-06	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P10	1.070e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P10	1.134e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P10	1.446e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P10	1.747e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P10	2.250e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

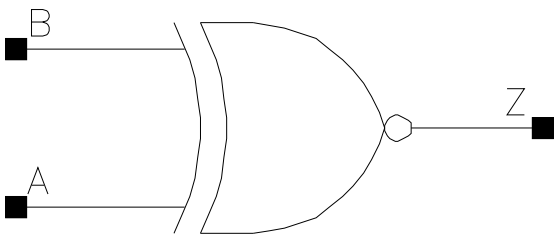
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P10	C8T28SOI_LLHF_-SDFPSQTX3_P10	C8T28SOIDV_LL_-SDFPSQTX5_P10	C8T28SOIDV_LL_-SDFPSQTX10_P10
Clock 100Mhz Data 0Mhz	7.499e-03	7.265e-03	7.009e-03	6.883e-03
Clock 100Mhz Data 25Mhz	7.548e-03	7.280e-03	7.009e-03	7.431e-03
Clock 100Mhz Data 50Mhz	7.597e-03	7.296e-03	7.009e-03	7.979e-03
Clock = 0 Data 100Mhz	3.569e-03	3.731e-03	3.650e-03	3.643e-03
Clock = 1 Data 100Mhz	3.940e-05	5.023e-04	3.486e-04	2.725e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P10	C8T28SOIDV_LL_-SDFPSQTX29_P10		
Clock 100Mhz Data 0Mhz	6.807e-03	6.758e-03		
Clock 100Mhz Data 25Mhz	7.951e-03	8.555e-03		
Clock 100Mhz Data 50Mhz	9.094e-03	1.035e-02		
Clock = 0 Data 100Mhz	3.631e-03	3.623e-03		
Clock = 1 Data 100Mhz	2.268e-04	1.964e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.600	0.544	0.8704
X5_P10	0.800	1.496	1.1968
X8_P10	1.600	1.088	1.7408
X9_P10	0.800	1.632	1.3056
X11_P10	1.600	1.360	2.1760
X14_P10	0.800	2.312	1.8496
X15_P10	1.600	1.904	3.0464
X19_P10	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P10	X5_P10	X8_P10	X9_P10
A	0.0010	0.0005	0.0017	0.0007
B	0.0010	0.0010	0.0014	0.0012
	X11_P10	X14_P10	X15_P10	X19_P10
A	0.0026	0.0010	0.0030	0.0012
B	0.0023	0.0016	0.0027	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X5_P10	X4_P10	X5_P10
A to Z ↓	0.0185	0.0517	4.2215	3.1844
A to Z ↑	0.0207	0.0459	6.5872	4.8938
B to Z ↓	0.0174	0.0390	4.2222	3.1704
B to Z ↑	0.0214	0.0352	6.6064	4.8904

	X8_P10	X9_P10	X8_P10	X9_P10
A to Z ↓	0.0220	0.0481	2.2344	1.6425
A to Z ↑	0.0252	0.0435	3.5178	2.4993
B to Z ↓	0.0209	0.0373	2.2345	1.6388
B to Z ↑	0.0249	0.0343	3.5267	2.4982
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0205	0.0457	1.5691	1.1197
A to Z ↑	0.0230	0.0407	2.2886	1.6105
B to Z ↓	0.0187	0.0348	1.5695	1.1159
B to Z ↑	0.0223	0.0322	2.2976	1.6070
	X15_P10	**X19_P10**	**X15_P10**	**X19_P10**
A to Z ↓	0.0225	0.0423	1.1905	0.8329
A to Z ↑	0.0255	0.0389	1.7451	1.1978
B to Z ↓	0.0207	0.0332	1.1901	0.8306
B to Z ↑	0.0248	0.0314	1.7511	1.1959

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	5.250e-07	1.000e-20
X5_P10	5.300e-07	1.000e-20
X8_P10	8.381e-07	1.000e-20
X9_P10	8.763e-07	1.000e-20
X11_P10	1.264e-06	1.000e-20
X14_P10	1.307e-06	1.000e-20
X15_P10	1.602e-06	1.000e-20
X19_P10	1.833e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X5_P10	X8_P10	X9_P10
A to Z	1.656e-03	3.465e-03	3.296e-03	4.774e-03
B to Z	1.593e-03	2.747e-03	3.071e-03	3.789e-03
	X11_P10	X14_P10	X15_P10	X19_P10
A to Z	4.627e-03	7.563e-03	6.309e-03	9.141e-03
B to Z	4.300e-03	5.881e-03	5.861e-03	7.261e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

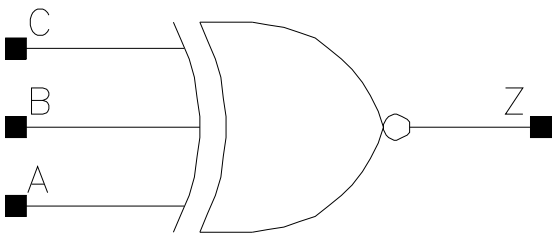
Pin Cycle (vdds)	X4_P10	X5_P10	X8_P10	X9_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P10	X14_P10	X15_P10	X19_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P10	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P10	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P10	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P10	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P10	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P10	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P10	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P10	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P10	C8T28SOIDV_LL_-XNOR3X4_P10	C8T28SOIDV_LL_-XNOR3X9_P10	C8T28SOIDV_LL_-XNOR3X13_P10
A	0.0016	0.0016	0.0020	0.0027
B	0.0016	0.0015	0.0019	0.0026
C	0.0007	0.0007	0.0006	0.0006
	C8T28SOIDV_LLS_-XNOR3X1_P10	C8T28SOIDV_LLS_-XNOR3X2_P10	C8T28SOIDV_LLS_-XNOR3X5_P10	C8T28SOIDV_LLS_-XNOR3X7_P10

A	0.0015	0.0018	0.0038	0.0059
B	0.0016	0.0018	0.0035	0.0055
C	0.0011	0.0013	0.0026	0.0037

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XNOR3X2_P10	C8T28SOIDV_LL_-XNOR3X4_P10	C8T28SOIDV_LL_-XNOR3X2_P10	C8T28SOIDV_LL_-XNOR3X4_P10
A to Z ↓	0.0528	0.0560	6.3568	3.4517
A to Z ↑	0.0498	0.0507	9.1722	4.9571
B to Z ↓	0.0531	0.0564	6.3577	3.4502
B to Z ↑	0.0505	0.0515	9.1795	4.9592
C to Z ↓	0.0708	0.0752	6.3523	3.4499
C to Z ↑	0.0678	0.0696	9.1758	4.9569
	C8T28SOIDV_LL_-XNOR3X9_P10	C8T28SOIDV_LL_-XNOR3X13_P10	C8T28SOIDV_LL_-XNOR3X9_P10	C8T28SOIDV_LL_-XNOR3X13_P10
A to Z ↓	0.0483	0.0549	1.7413	1.1965
A to Z ↑	0.0500	0.0566	2.4242	1.6902
B to Z ↓	0.0489	0.0555	1.7408	1.1962
B to Z ↑	0.0509	0.0577	2.4236	1.6905
C to Z ↓	0.0695	0.0827	1.7394	1.1957
C to Z ↑	0.0709	0.0848	2.4249	1.6910
	C8T28SOIDV_LLS_-XNOR3X1_P10	C8T28SOIDV_LLS_-XNOR3X2_P10	C8T28SOIDV_LLS_-XNOR3X1_P10	C8T28SOIDV_LLS_-XNOR3X2_P10
A to Z ↓	0.0321	0.0358	11.6640	6.4959
A to Z ↑	0.0336	0.0330	19.7446	10.3678
B to Z ↓	0.0329	0.0368	11.6738	6.4997
B to Z ↑	0.0343	0.0339	19.7249	10.3595
C to Z ↓	0.0318	0.0349	11.6737	6.5123
C to Z ↑	0.0335	0.0325	19.6845	10.3438
	C8T28SOIDV_LLS_-XNOR3X5_P10	C8T28SOIDV_LLS_-XNOR3X7_P10	C8T28SOIDV_LLS_-XNOR3X5_P10	C8T28SOIDV_LLS_-XNOR3X7_P10
A to Z ↓	0.0364	0.0315	3.1263	2.1709
A to Z ↑	0.0351	0.0308	5.1082	3.4205
B to Z ↓	0.0359	0.0306	3.1321	2.1758
B to Z ↑	0.0347	0.0302	5.1040	3.4180
C to Z ↓	0.0343	0.0293	3.1287	2.1776
C to Z ↑	0.0330	0.0286	5.0856	3.4114

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P10	4.229e-07	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P10	4.979e-07	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P10	8.697e-07	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P10	1.230e-06	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P10	3.012e-07	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P10	5.103e-07	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P10	1.211e-06	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P10	1.837e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P10	C8T28SOIDV_LL_-XNOR3X4_P10	C8T28SOIDV_LL_-XNOR3X9_P10	C8T28SOIDV_LL_-XNOR3X13_P10
A to Z	2.243e-03	2.607e-03	3.851e-03	6.328e-03
B to Z	2.190e-03	2.557e-03	3.805e-03	6.247e-03
C to Z	3.502e-03	3.921e-03	5.509e-03	8.875e-03
	C8T28SOIDV_LLS_-XNOR3X1_P10	C8T28SOIDV_LLS_-XNOR3X2_P10	C8T28SOIDV_LLS_-XNOR3X5_P10	C8T28SOIDV_LLS_-XNOR3X7_P10
A to Z	1.369e-03	1.966e-03	4.387e-03	6.034e-03
B to Z	1.296e-03	1.893e-03	4.076e-03	5.502e-03
C to Z	1.252e-03	1.842e-03	3.931e-03	5.281e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

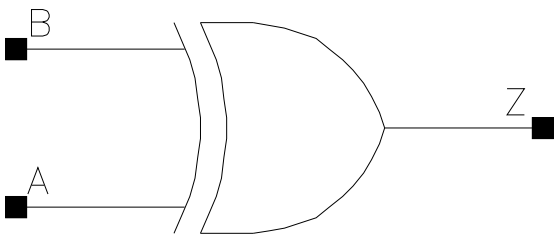
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P10	C8T28SOIDV_LL_-XNOR3X4_P10	C8T28SOIDV_LL_-XNOR3X9_P10	C8T28SOIDV_LL_-XNOR3X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P10	C8T28SOIDV_LLS_-XNOR3X2_P10	C8T28SOIDV_LLS_-XNOR3X5_P10	C8T28SOIDV_LLS_-XNOR3X7_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.360	1.0880
X4_P10	1.600	0.544	0.8704
X5_P10	0.800	1.360	1.0880
X8_P10	1.600	1.088	1.7408
X9_P10	0.800	1.496	1.1968
X12_P10	1.600	1.360	2.1760
X13_P10	0.800	2.176	1.7408
X15_P10	1.600	1.904	3.0464
X17_P10	0.800	2.312	1.8496
X18_P10	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P10	X4_P10	X5_P10	X8_P10
A	0.0005	0.0010	0.0007	0.0017
B	0.0010	0.0010	0.0011	0.0016
	X9_P10	X12_P10	X13_P10	X15_P10
A	0.0007	0.0027	0.0013	0.0031
B	0.0014	0.0020	0.0023	0.0026
	X17_P10	X18_P10		
A	0.0013	0.0017		
B	0.0023	0.0020		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X4_P10**	**X2_P10**	**X4_P10**
A to Z ↓	0.0445	0.0191	6.0633	3.2183
A to Z ↑	0.0417	0.0226	9.4369	8.7606
B to Z ↓	0.0341	0.0194	6.0253	3.2498
B to Z ↑	0.0345	0.0210	9.4376	8.7587
	X5_P10	**X8_P10**	**X5_P10**	**X8_P10**
A to Z ↓	0.0416	0.0246	3.2783	1.7564
A to Z ↑	0.0374	0.0269	4.7776	4.5987
B to Z ↓	0.0318	0.0255	3.2670	1.7757
B to Z ↑	0.0306	0.0254	4.7718	4.5939
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0406	0.0224	1.7256	1.1819
A to Z ↑	0.0377	0.0243	2.4897	3.0812
B to Z ↓	0.0314	0.0215	1.7205	1.1948
B to Z ↑	0.0304	0.0221	2.4899	3.0800
	X13_P10	**X15_P10**	**X13_P10**	**X15_P10**
A to Z ↓	0.0375	0.0242	1.1816	0.9214
A to Z ↑	0.0349	0.0278	1.7282	2.7443
B to Z ↓	0.0269	0.0232	1.1778	0.9318
B to Z ↑	0.0253	0.0253	1.7256	2.7423
	X17_P10	**X18_P10**	**X17_P10**	**X18_P10**
A to Z ↓	0.0396	0.0441	0.8956	0.8938
A to Z ↑	0.0364	0.0392	1.2941	1.2628
B to Z ↓	0.0293	0.0352	0.8937	0.8929
B to Z ↑	0.0270	0.0311	1.2928	1.2617

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P10	4.005e-07	1.000e-20
X4_P10	5.195e-07	1.000e-20
X5_P10	6.463e-07	1.000e-20
X8_P10	8.305e-07	1.000e-20
X9_P10	1.055e-06	1.000e-20
X12_P10	1.259e-06	1.000e-20
X13_P10	1.692e-06	1.000e-20
X15_P10	1.516e-06	1.000e-20
X17_P10	1.822e-06	1.000e-20
X18_P10	1.805e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P10	X4_P10	X5_P10	X8_P10
A to Z	2.591e-03	1.695e-03	3.249e-03	3.353e-03
B to Z	2.245e-03	1.591e-03	2.758e-03	3.280e-03
	X9_P10	X12_P10	X13_P10	X15_P10
A to Z	4.610e-03	4.812e-03	7.535e-03	6.241e-03
B to Z	3.993e-03	4.384e-03	4.873e-03	5.799e-03
	X17_P10	X18_P10		
A to Z	8.426e-03	9.333e-03		
B to Z	5.745e-03	7.054e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

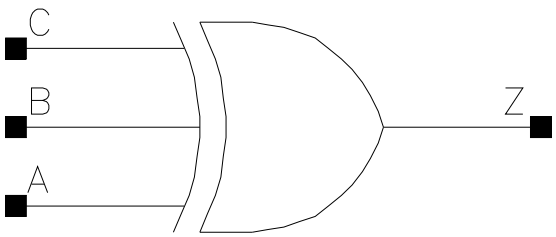
Pin Cycle (vdds)	X2_P10	X4_P10	X5_P10	X8_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P10	X12_P10	X13_P10	X15_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P10	X18_P10		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P10	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P10	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P10	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P10	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P10	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P10	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P10	C8T28SOIDV_LL_-XOR3X4_P10	C8T28SOIDV_LL_-XOR3X9_P10	C8T28SOIDV_LL_-XOR3X13_P10
A	0.0017	0.0015	0.0019	0.0027
B	0.0016	0.0016	0.0019	0.0026
C	0.0010	0.0010	0.0014	0.0021
	C8T28SOIDV_LLS_-XOR3X1_P10	C8T28SOIDV_LLS_-XOR3X2_P10	C8T28SOIDV_LLS_-XOR3X5_P10	C8T28SOIDV_LLS_-XOR3X7_P10

A	0.0017	0.0018	0.0031	0.0047
B	0.0018	0.0018	0.0030	0.0048
C	0.0006	0.0006	0.0006	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P10	**C8T28SOIDV_LL_-XOR3X4_P10**	**C8T28SOIDV_LL_-XOR3X2_P10**	**C8T28SOIDV_LL_-XOR3X4_P10**
A to Z ↓	0.0514	0.0561	6.3833	3.4636
A to Z ↑	0.0488	0.0522	9.4503	4.9651
B to Z ↓	0.0517	0.0571	6.3860	3.4630
B to Z ↑	0.0493	0.0534	9.4551	4.9694
C to Z ↓	0.0509	0.0561	6.3831	3.4635
C to Z ↑	0.0483	0.0520	9.4552	4.9694
	C8T28SOIDV_LL_-XOR3X9_P10	**C8T28SOIDV_LL_-XOR3X13_P10**	**C8T28SOIDV_LL_-XOR3X9_P10**	**C8T28SOIDV_LL_-XOR3X13_P10**
A to Z ↓	0.0510	0.0563	1.7283	1.1720
A to Z ↑	0.0513	0.0575	2.4399	1.6436
B to Z ↓	0.0520	0.0571	1.7277	1.1720
B to Z ↑	0.0524	0.0587	2.4426	1.6452
C to Z ↓	0.0507	0.0564	1.7276	1.1723
C to Z ↑	0.0508	0.0583	2.4416	1.6445
	C8T28SOIDV_LLS_-XOR3X1_P10	**C8T28SOIDV_LLS_-XOR3X2_P10**	**C8T28SOIDV_LLS_-XOR3X1_P10**	**C8T28SOIDV_LLS_-XOR3X2_P10**
A to Z ↓	0.0337	0.0371	8.3380	6.6336
A to Z ↑	0.0338	0.0330	14.1891	9.9008
B to Z ↓	0.0346	0.0377	8.3623	6.6392
B to Z ↑	0.0345	0.0334	14.1937	9.8946
C to Z ↓	0.0528	0.0570	8.3076	6.5957
C to Z ↑	0.0539	0.0537	14.1649	9.8509
	C8T28SOIDV_LLS_-XOR3X5_P10	**C8T28SOIDV_LLS_-XOR3X7_P10**	**C8T28SOIDV_LLS_-XOR3X5_P10**	**C8T28SOIDV_LLS_-XOR3X7_P10**
A to Z ↓	0.0490	0.0421	3.4401	2.3873
A to Z ↑	0.0409	0.0356	5.1513	3.4830
B to Z ↓	0.0468	0.0417	3.4497	2.3921
B to Z ↑	0.0400	0.0355	5.1466	3.4806
C to Z ↓	0.0787	0.0658	3.4454	2.3801
C to Z ↑	0.0724	0.0599	5.1398	3.4700

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P10	3.548e-07	1.000e-20
C8T28SOIDV_LL_XOR3X4_P10	4.382e-07	1.000e-20
C8T28SOIDV_LL_XOR3X9_P10	7.843e-07	1.000e-20
C8T28SOIDV_LL_XOR3X13_P10	1.170e-06	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P10	4.984e-07	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P10	5.898e-07	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P10	1.023e-06	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P10	1.535e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P10	C8T28SOIDV_LL_-XOR3X4_P10	C8T28SOIDV_LL_-XOR3X9_P10	C8T28SOIDV_LL_-XOR3X13_P10
A to Z	2.149e-03	2.614e-03	3.900e-03	6.727e-03
B to Z	2.059e-03	2.544e-03	3.821e-03	6.586e-03
C to Z	2.011e-03	2.489e-03	3.766e-03	6.552e-03
	C8T28SOIDV_LLS_-XOR3X1_P10	C8T28SOIDV_LLS_-XOR3X2_P10	C8T28SOIDV_LLS_-XOR3X5_P10	C8T28SOIDV_LLS_-XOR3X7_P10
A to Z	1.643e-03	1.995e-03	3.952e-03	5.540e-03
B to Z	1.616e-03	1.954e-03	3.788e-03	5.298e-03
C to Z	3.119e-03	3.551e-03	6.530e-03	9.161e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P10	C8T28SOIDV_LL_-XOR3X4_P10	C8T28SOIDV_LL_-XOR3X9_P10	C8T28SOIDV_LL_-XOR3X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P10	C8T28SOIDV_LLS_-XOR3X2_P10	C8T28SOIDV_LLS_-XOR3X5_P10	C8T28SOIDV_LLS_-XOR3X7_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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