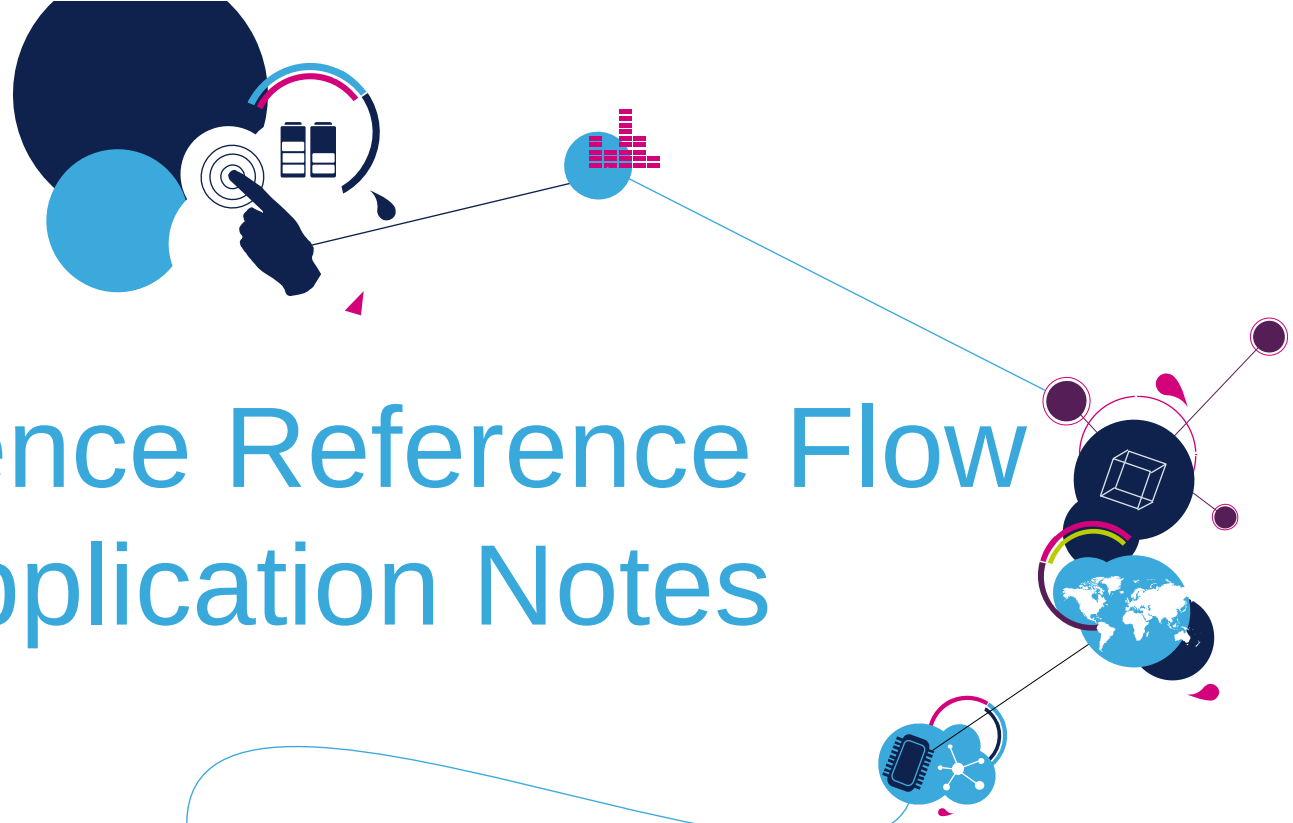

28nm FD-SOI Cadence Reference Flow Place-and-Route Application Notes

Version 3.0

Digital Design Flows & Methodologies

October 2018

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Revisions

Version	Date	Comment
3.0	October 2018	• Voltage Spacing Management
2.0	March 2018	• Updated EDA tools versions • Add IP/memory implementation guidelines
1.0	June 2017	Initial Version

Prerequisites : Documentation

- Please refer to the **Foundation_Cadence_TechnoKit_cmos028FDSOI** User Manual for the description of the technology files

- Please refer to the **28nm FD-SOI Cadence Reference Flow Sign-Off Application Notes** for
  - Description of 28nm-FDSOI Sign-Off RC extraction scenarios
  - Description of 28nm-FDSOI Sign-Off STA scenarios
  - Description of clock tree implementation rules
  - On-Chip-Variation derating factors

Prerequisites : Technology

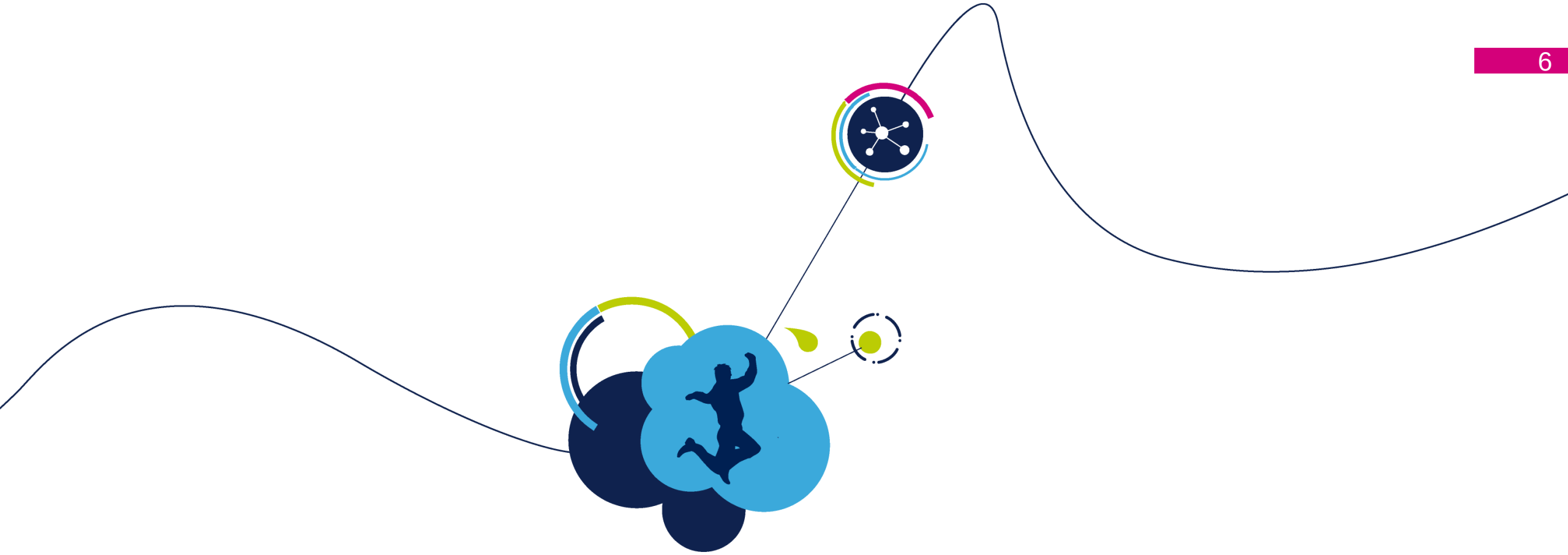
- In P&R, **only dominant STA scenarios** for setup, hold and worst leakage corner are sufficient (identified from a first Signoff loop)
- Clock tree must follow “**Clock Tree Implementation Rules**”
- Place-and-Route **OCV** values must be taken from Signoff Application Notes
- **RVT and LVT standard-cells cannot be mixed** in the same standard-cell placement area, due to LVT being flip-well architecture

EDA Tools Versions

- The 28nm FD-SOI Cadence Reference Flow has been qualified with the following EDA tools

Place-and-Route Step	EDA Tool & Version
Place-and-Route	Cadence Innovus 17.15
LPA	MVS 17.12

- EDA tools versions used for flow execution are left up to user discretion



Innovus : Static Timing Analysis Settings

Required Settings for Innovus

- The following variables have to be set in Innovus for static timing analysis in 28nm FD-SOI:
  - setDesignMode -process 28
  - setAnalysisMode -analysisType onChipVariation
  - set_global timing_cppr_transition_sense same_transition_expanded
  - set_global timing_use_latch_early_launch_edge false
  - set_global timing_enable_early_late_data_slews_for_setuphold_mode_checks false
  - set_global timing_allow_input_delay_on_clock_source true
  - set_global timing_enable_pessimistic_cppr_for_reconvergent_clock_paths true
  - set_global timing_enable_power_ground_constants true
  - setDelayCalMode -SIAware
- CCS libraries mandatory true

Setting STA 0y/2ey in Innovus

- The following lines describe how to mix fresh (0y) and aged (2ey) libraries during Static Timing Analysis in Cadence Innovus

  → In file: mmmc view_definitions.tcl :

```
create_rc_corner -name RC1 ... -T -40 -qx_tech_file <path>
…
create_library_set -name LS1_fresh -timing [list <FRESH ccs lib path>]
create_library_set -name LS1_aging -timing [list <AGING ccs lib path>]
...
create_delay_corner -name DC1 -rc_corner RC1 -early_library_set LS1_fresh -late_library_set LS1_aging ...
...
create_constraint_mode -name CM1 -sdc_files [list <sdc file path>]
...
create_analysis_view -name AV1 -constraint_mode CM1 -delay_corner DC1 ; # All views can be created here
...
set_analysis_view -setup AV1 -hold AV2 ; # Only activate required set of views for each step.
```

Example of set_timing_derate Commands in Innovus -1-

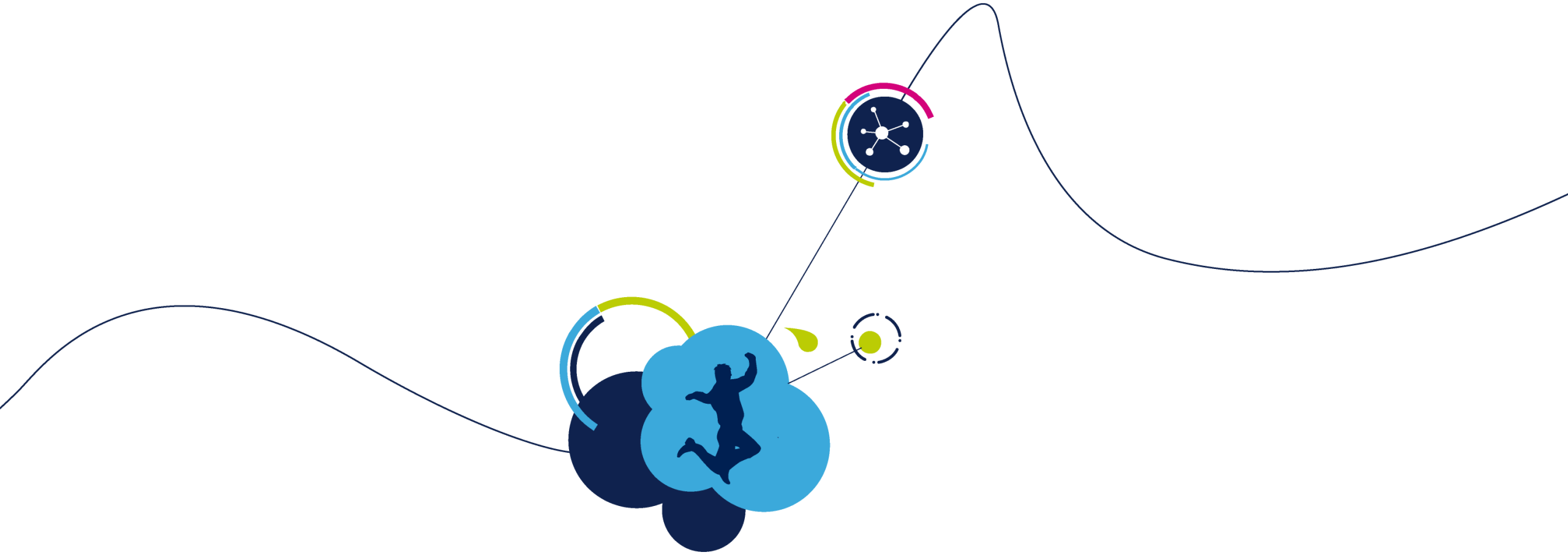
- The following lines describe an example of how to specify for a delay corner a derating factor of +/-5% on the clock paths and -23% on the data paths for hold checks in Innovus:

```
set_timing_derate -delay_corner DC1 -clock –early 0.95     ; # for a value of +-5%
set_timing_derate -delay_corner DC1 -clock –late 1.05      ; # for a value of +-5%
set_timing_derate -delay_corner DC1 -data –early 0.77      ; # -23% on hold data paths
set_timing_derate -delay_corner DC1 -data –late 1.00       ; # +0% on setup data paths
```

Example of set_timing_derate Commands in Innovus -2-

- No derate is applied on the dynamic portion of net delays

```
foreach delayCornerName  [all_delay_corners ] {
    set_timing_derate        -delay_corner ${delayCornerName} -clock -early -net_delay -dynamic    1.00
    set_timing_derate        -delay_corner ${delayCornerName} -clock -late -net_delay -dynamic     1.00
    set_timing_derate        -delay_corner ${delayCornerName} -data -early -net_delay -dynamic     1.00
    set_timing_derate        -delay_corner ${delayCornerName} -data -late -net_delay -dynamic      1.00
```



Innovus Place-and-Route Flow

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LVT vdds logic connection

- Use this variable to avoid the following error in Innovus for LVT designs with no external biasing:

```
"**ERROR: (IMPDB-1220):   A global net connection(GNC) rule for connecting
pin 'vdds' of cell 'C8T28SOI_LL_FILLERCELL4' to global net 'VSS' was
specified.  The connection cannot be made because the power pin and the
ground net are not of the same polarity.  Check the imported design and
make sure the GNC rule is correctly specified or generated."
```

```
set init_ignore_pgpin_polarity_check {vdds gnds vddsma}
```

- Add the following statements in the UPF file:

```
set_design_attributes -elements {.} -attribute enable_bias true
create_supply_set .... -function {pwell gnd} -function {nwell gnd}
```

Nanoroute Settings -1-

- The following lines force **Innovus** in *autoViaGen* mode, ensure multi-cut vias usage, and allows diodes antenna fixing:
  - setNanoRouteMode -routeExpUseAutoVia true
  - setNanoRouteMode -drouteUseMultiCutViaEffort high
  - setNanoRouteMode -droutePostRouteSwapVia multicut
  - setNanoRouteMode -routeInsertAntennaDiode true
  - setNanoRouteMode -routeAntennaCellName *<List of cells to be used (all power domain)>*

Nanoroute Settings -2-

- The following lines enable lithography driven routing, and define top routing layer:
  - setNanoRouteMode –routeWithLithoDriven true
  - setNanoRouteMode -routeTopRoutingLayer <layer number>

Nanoroute Settings -3-

- When FBB voltage is below -0,6V, negative voltages are not well supported in Innovus tech file (Innovus version 17.1 onwards) (CCR #2003674), so voltage spacing rules won't be properly applied.
- The workaround is to load a Non Default Rule, provided in the FoundationTechnoKit :

```
${Foundation_Cadence_TechnoKitTRoot}/LEF/high_voltage.lef
```

- The rule has to be applied to the bias net with negative voltage :

```
setAttribute -net vdds -non_default_rule HighVoltageFBBLowerThan600mVvsGO1
-non_default_rule_effort hard
setNanoRouteMode -routeEnforceNdrOnSpecialNetWire true
```

Timing Convergence -1-

- The following lines improve convergence by limiting the length of the wires, and manage delay-cells:
  - setOptMode –maxLength 900
  - set_ccopt_property max_source_to_sink_net_length 300
  - setDontUse <delay cells> true ; setOptMode –holdFixingCells <delay cells, buffers cells, inverter cells>

Timing Convergence -2-

- It is recommended to create a LEF defining a double space rule and apply it to clock tree nets using *create_route_type* + *set_ccopt_property*… Example (10ML):

```
############################## 2x spacing starting for B1 B2 ############################
NONDEFAULTRULE ctsDoubleCutDoubleSpacingShield
#########################################################################################
LAYER M1
  WIDTH  0.050 ;
  SPACING  0.050 ;
END   M1….
LAYER B1
  WIDTH  0.100 ;
  SPACING  0.300 ;
END   B1
LAYER B2
  WIDTH  0.100 ;
  SPACING  0.300 ;
END   B2
....LAYER LB
  WIDTH   4.00 ;
  SPACING 2.00 ;
END LB
END ctsDoubleCutDoubleSpacingShield
```

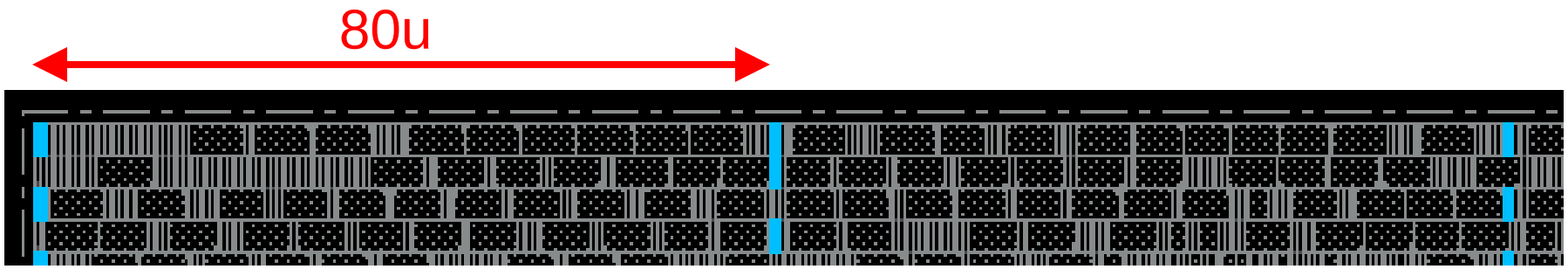
```
create_route_type -name route_type_nonleaf_from_edi_cts -top_preferred_layer 8 \
   -bottom_preferred_layer 7 -non_default_rule ctsDoubleCutDoubleSpacingShield
create_route_type -name route_type_leaf_from_edi_cts -top_preferred_layer 4 \
   -bottom_preferred_layer 3 -non_default_rule ctsDoubleCutDoubleSpacing
set_ccopt_property route_type -net_type leaf route_type_leaf_from_edi_cts
set_ccopt_property route_type -net_type top route_type_nonleaf_from_edi_cts
set_ccopt_property route_type -net_type trunk route_type_nonleaf_from_edi_cts
```

Tie Cells Insertion Flow

- The following lines can be used to manage tie-up tie-low connections with tie-cells:
  - setTieHiLoMode -maxFanout 20 -maxDistance 50
  - setTieHiLoMode -honorDontUse true
  - setTieHiLoMode -cell <list of tie-high and tie-low cells>
  - addTieHiLo -powerDomain … -prefix ...

Welltaps Insertion Flow

- The following lines ensure DRC-clean welltaps insertion: every standard-cell is at maximum 40u from a welltap:
  - addWellTap -cell <welltap cell> -checkerboard -cellInterval 160 -prefix WT



Top/Bottom/Left/Right Endcaps Insertion Flow

- The following lines insert :
  - Left and right endcap standard-cells, to ensure P&R context is the same as the one used during library timing characterization. Minimum size must be FILLERPFOP2:

```
setEndCapMode -prefix ENDCAP_LEFT_RIGHT –leftEdge <fillerfop2 cell> -rightEdge <fillerfop2 cell>
addEndCap
```

  - Top and bottom endcap standard-cells on the first bottom and the last top standard-cell row, to be DRC clean:

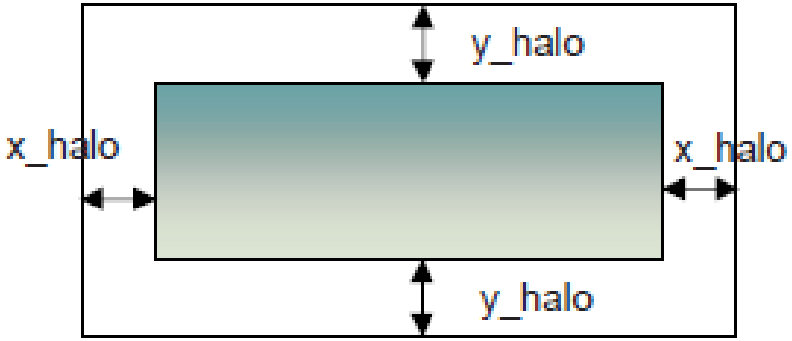
```
setEndCapMode -prefix ENDCAP_TOP_BOTTOM -bottomEdge <list of fillercells> -topEdge <list of fillercells>
addEndCap
```

CTS Halos

- The following lines in CTS spec file define CTS halos, to avoid electromigration/IR-Drop issues, by keeping a certain minimum distance between clock inverters and/or gating cells…
- Recommended values are y_halo=0.1u and

  x_halo=4u for small drives or 8u for higher drives.
- Example:

```
AutoCTSRootPin clk1
MaxSkew <max_tran>ps
CellHalo
+ <clock cell with drive<X56 >   4   0.1
+ <clock cell with drive>X55 >   8   0.1
End
```



Memories, IPs -1-

- Memory pins are drawn with vertical M4 shapes (non-preferential direction)
- To connect memory cuts to the PG grid, vias are stacked at each intersection between memory M4 pins and PG grid stripes.
- At floorplan-level, a 1 um hard halo is generally defined around the IPs
- Around memories/IPs, soft placement blockages may be defined to get easier pin access

Memories, IPs -2-

- Full metal obstructions are generally defined in the LEF file of the digital IPs
  - This avoids top-level routing over the IP
  - During top-level routing, the IP is seen as large metal shape, which forces the router to respect fat layer spacing rules (typically around 0.5um, which corresponds to 5 tracks)
- Routing blockages may be defined inside the digital IP at the boundary in order to avoid long nets in the preferentials directions. This will limit coupling effects between top-level routing and block-level routing.

Keep out distance between RVT and LVT

- LVT being a flip-well architecture, it cannot be mixed with RVT cells on a same standard cells area

- Some dedicated islands have to be created in case RVT and LVT are used for digital sections on the same chip, since both cannot be merged inside a standard cells row

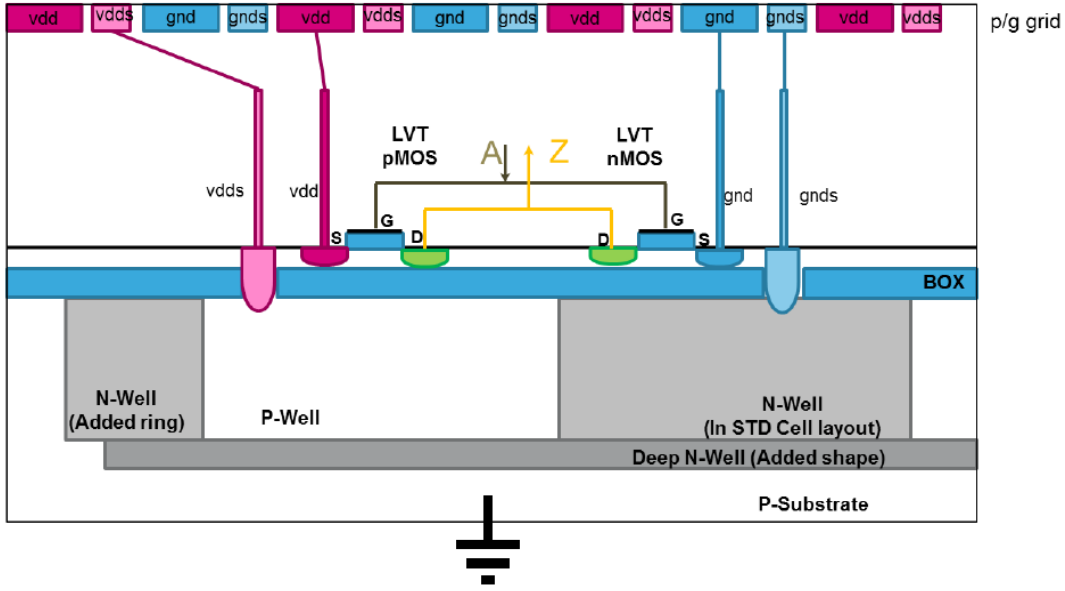
- **DRM** rules have to be honored for such configurations

Top level placement of Deep NWell/ Block Construction level guidelines -1-

- To apply a body bias voltage to the P-Well, it is required to isolate the P-Well areas from the P-Substrate.
- This typically occurs in case of a single VT (LVT or RVT) design where we want to apply Back Bias (BB) voltages to some design portions
- The isolation is implemented using a

deep n-type implant (Deep N-Well) and

an N-Well ring.



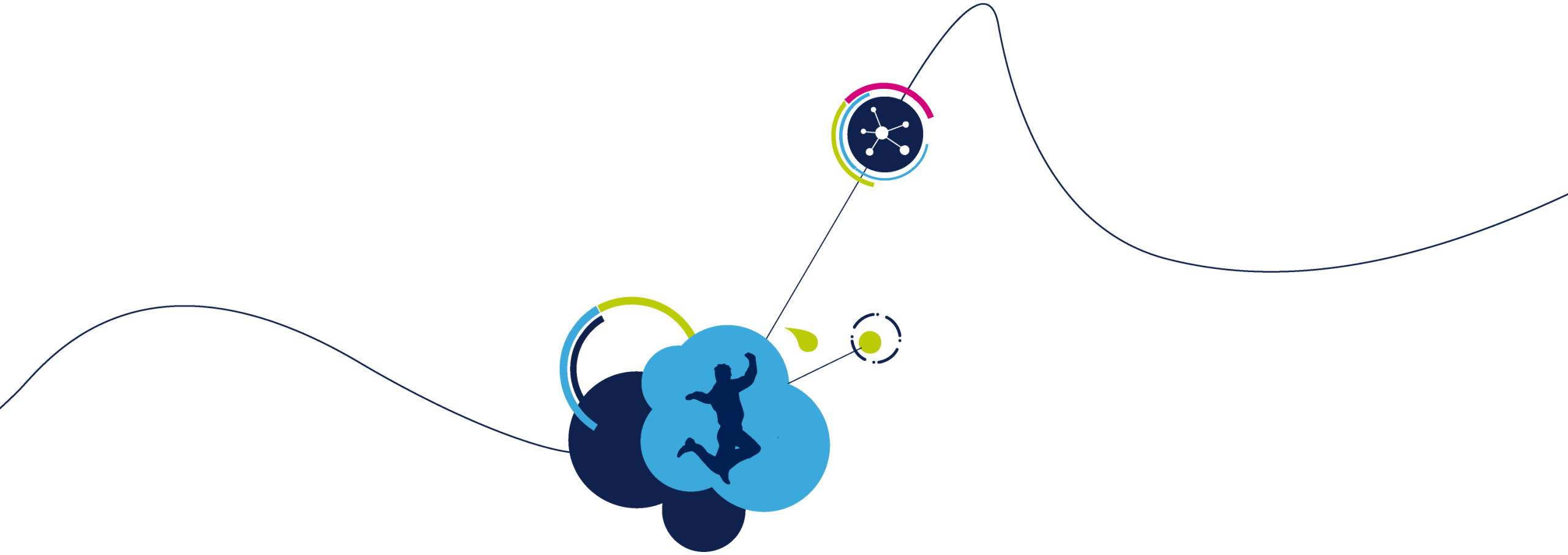
LVT Body biased configuration with deep N-Well

Top level placement of Deep NWell/ Block Construction level guidelines -2-

- It is required to implement a power grid that distributes supply (vdd), ground (gnd) and substrates polarization (gnds, vdds)

- **To isolate the P-Well from P-Substrate it is required to:**
  - Add an N-Well ring around the biased region to side-isolate P-Well
  - Add under the biased region a deep N-Well layer (T3) with boundary over N-Well ring

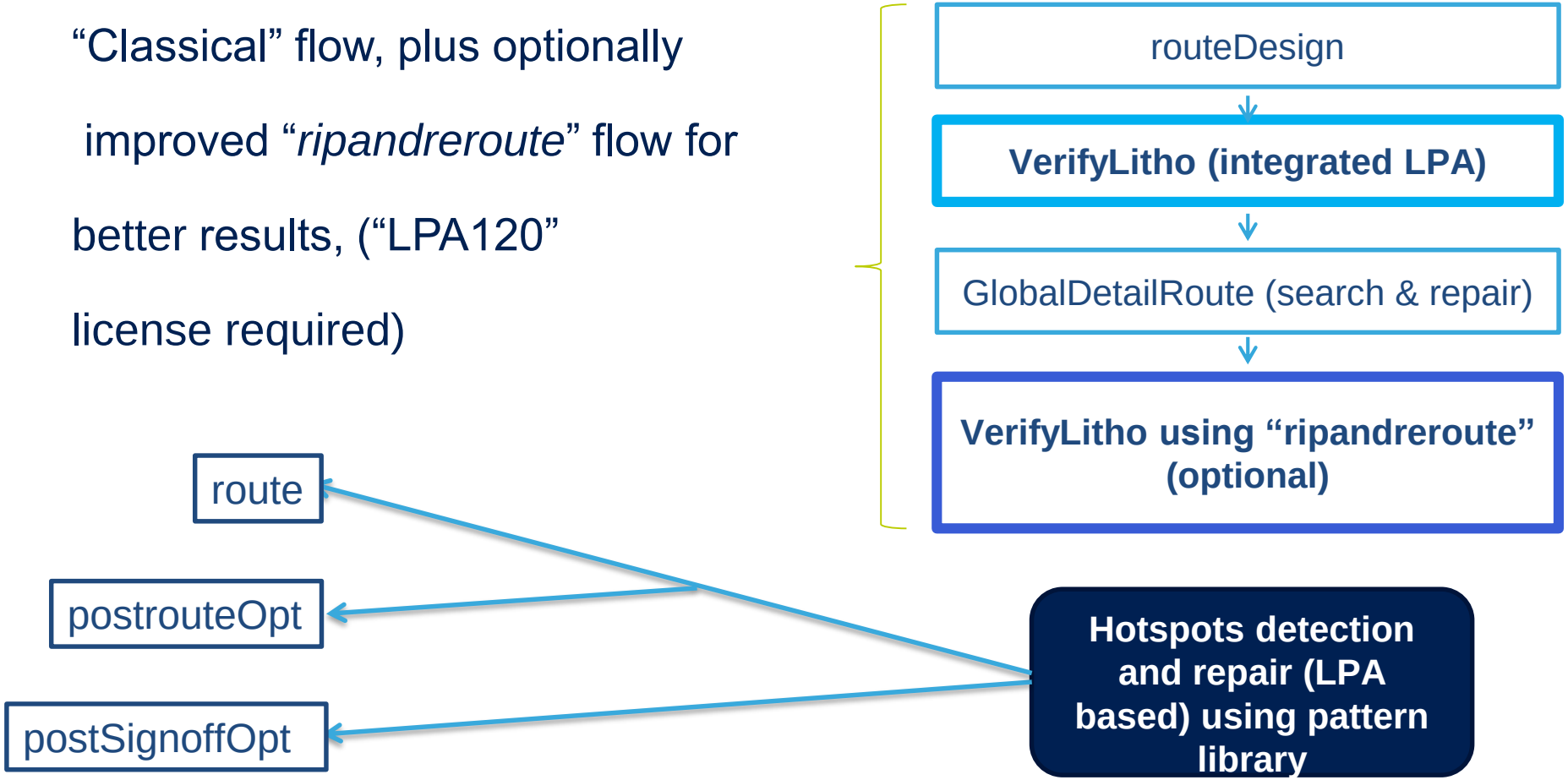
- **Please refer to DRM for**
  - Deep-NWell/T3 – Deep-NWell/T3 spacing rules
  - Deep-NWell/T3 – NW spacing rules
  - T3 – NW overlap rule



LPA Litho Fixing Flow

LPA Lithography Hotspots Fixing

"Classical" flow, plus optionally improved "*ripandreroute*" flow for better results, ("LPA120" license required)



LPA Lithography Hotspots Fixing Script -1-

- The following line is set before routing:

```
setNanoRouteMode –routeWithLithoDriven true
```

- The following lines call “lpa” after routing:

```
suppressMessage ENCOGDS-392
set lpa::ignoreCdnInitWarning 1
clearDrc
set outDir "./LPA/LPA.route__${route_pass_number}.ref_classical“
set techfile <Foundation_Cadence_TechnoKit_cmos028FDSOI unix path>/LPA
verifyLitho -streamOutOptions { -outputMacros } -routingLayersOnly -techFile $techfile -dir $outDir
file delete -force ${outDir}/INPUT/input.gds
foreach file [glob ${outDir}/M*] { file delete -force ${file} }
loadViolationReport -type CDNLitho -filename $outDir/DMC/merged.hif
```

LPA Lithography Hotspots Fixing Script -2-


```
# litho repair
  setNanoRouteMode   –droutePostRouteLithoRepair true –routeInsertAntennaDiode false \
                              -drouteExpAdvancedSearchRepairEffort max -drouteFixAntenna false
  globalDetailRoute
(restore Nanoroute settings)
# hotspots check
set outDir "./LPA/LPA.route__${route_pass_number}.fix_classical“
 verifyLitho  -streamOutOptions { -outputMacros } -routingLayersOnly -techFile $techfile -dir $outDir
  file delete -force ${outDir}/INPUT/input.gds
  foreach file [glob ${outDir}/M*] { file delete -force ${file} }
```

LPA Lithography Hotspots Fixing Script -3-


```
# hotspot fixing – ripandreroute - optionnal
  set backup(setVerifyGeometryMode_report) [getVerifyGeometryMode -report]
set_verify_drc_mode -report ./LPA/verifyLitho_ripandreroute.[pid].geom.rpt
set outDir "./LPA/LPA.route__$route_pass_number.ripandreroute“
set status [ catch { verifyLitho  -streamOutOptions { -outputMacros } -routingLayersOnly \
                -techFile $techfile -dir $outDir -apply ripandreroute } ]
  if { $status == 1 } {
       puts"Advanced litho fixing finished with an 'error' . Please check if LPA120 licence is available."
  } else {
       file delete -force ${outDir}/INPUT/input.gds
       foreach file [glob ${outDir}/M*] { file delete -force ${file} }
       set_verify_drc_mode -report $backup(setVerifyGeometryMode_report)
```

LPA Lithography Hotspots Fixing Script -4-


```
setNanoRouteMode    -drouteFixAntenna false -routeInsertAntennaDiode false \
                                    -routeWithLithoDriven false -droutePostRouteLithoRepair false
    globalDetailRoute
    (reset nanoroute settings)
  # Remove route blockages added by 'ripandreroute
    deleteRouteBlk -name *_litho_repair
  # Hotspot check
set outDir "./LPA/LPA.route__${route_pass_number}.fix_ripandreroute“
    verifyLitho  -streamOutOptions { -outputMacros } -routingLayersOnly -techFile $techfile \
                          -dir $outDir
    file delete -force ${outDir}/INPUT/input.gds
    foreach file [glob ${outDir}/M*] { file delete -force ${file} }
```