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C28SOI_SC_8_CLK_LL Databook

8 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

Overview

- C28SOI_SC_8_CLK_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 388 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

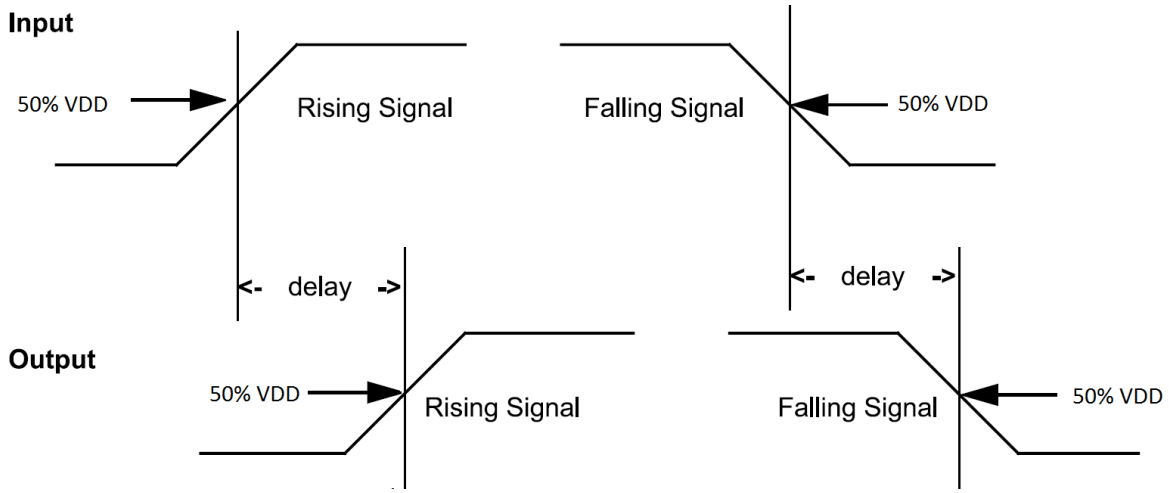


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

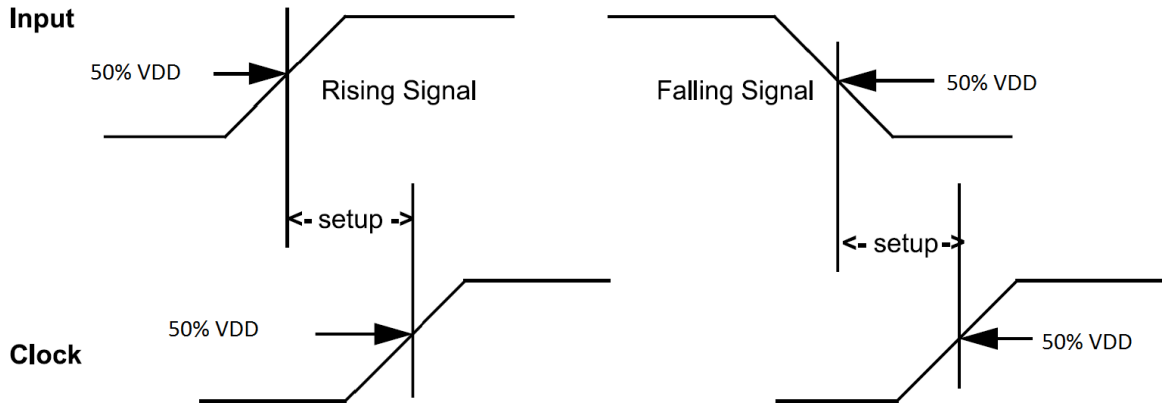


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

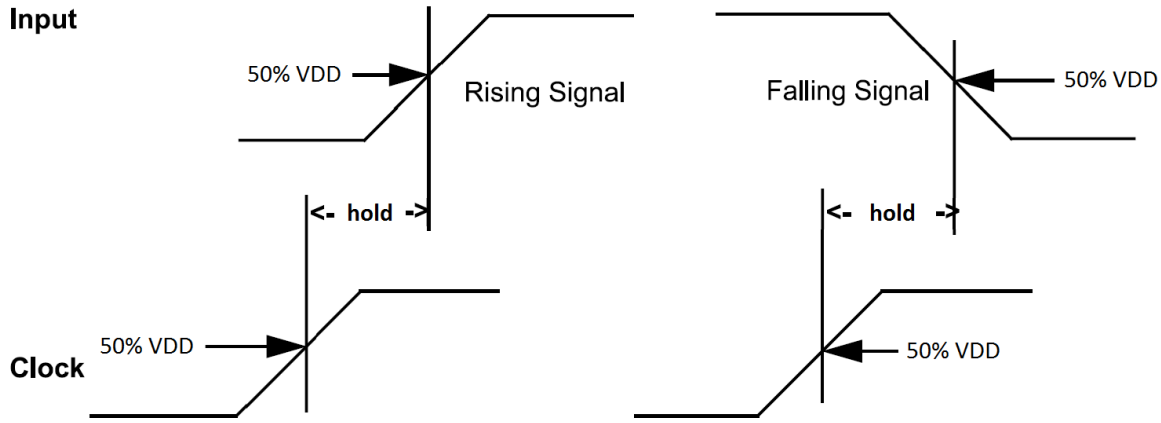


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

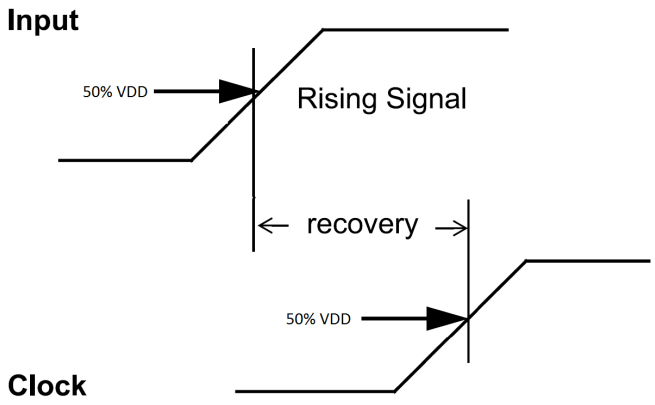


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

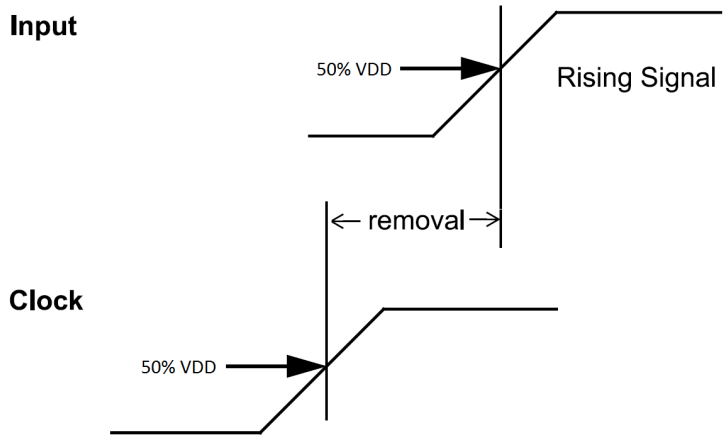


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

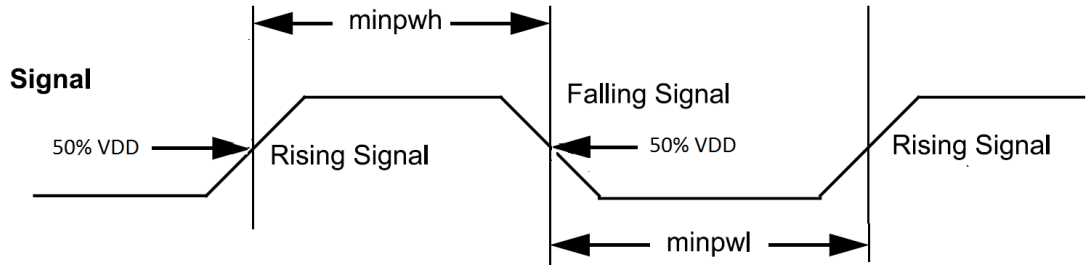


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

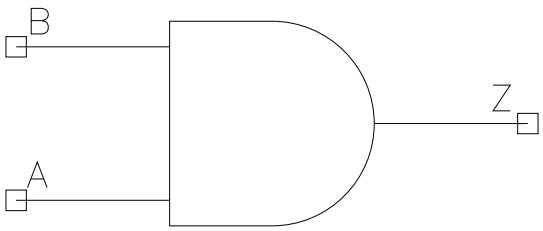
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

CNAND2

Cell Description

2 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	0.800	1.496	1.1968
X14_P4	0.800	1.496	1.1968
X14_P10	0.800	1.496	1.1968
X14_P16	0.800	1.496	1.1968
X19_P0	0.800	1.632	1.3056
X19_P4	0.800	1.632	1.3056
X19_P10	0.800	1.632	1.3056
X19_P16	0.800	1.632	1.3056
X27_P0	0.800	1.632	1.3056
X27_P4	0.800	1.632	1.3056
X27_P10	0.800	1.632	1.3056
X27_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0013	0.0014	0.0015	0.0016
B	0.0013	0.0014	0.0015	0.0016
	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0013	0.0014	0.0015	0.0015
B	0.0013	0.0014	0.0015	0.0016
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0011	0.0012	0.0012	0.0013
B	0.0010	0.0010	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0233	0.0265	1.2218	1.3188
A to Z ↑	0.0182	0.0209	1.7269	1.9432
B to Z ↓	0.0219	0.0248	1.2205	1.3159
B to Z ↑	0.0195	0.0221	1.7276	1.9432
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0313	0.0357	1.4581	1.5825
A to Z ↑	0.0249	0.0285	2.2691	2.5783
B to Z ↓	0.0291	0.0332	1.4555	1.5816
B to Z ↑	0.0260	0.0295	2.2714	2.5814
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0253	0.0287	0.9345	1.0107
A to Z ↑	0.0200	0.0229	1.3265	1.4885
B to Z ↓	0.0240	0.0272	0.9340	1.0095
B to Z ↑	0.0215	0.0244	1.3268	1.4887
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0340	0.0389	1.1176	1.2141
A to Z ↑	0.0273	0.0312	1.7382	1.9727
B to Z ↓	0.0320	0.0365	1.1156	1.2138
B to Z ↑	0.0286	0.0325	1.7375	1.9738
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0276	0.0318	0.7899	0.8549
A to Z ↑	0.0247	0.0282	0.7641	0.8588
B to Z ↓	0.0272	0.0313	0.7899	0.8556
B to Z ↑	0.0262	0.0298	0.7639	0.8577
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0374	0.0431	0.9475	1.0310
A to Z ↑	0.0326	0.0372	1.0030	1.1397
B to Z ↓	0.0367	0.0422	0.9484	1.0322
B to Z ↑	0.0343	0.0389	1.0016	1.1390

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X14_P0	1.549e-04	1.000e-20
X14_P4	5.500e-05	1.000e-20
X14_P10	1.746e-05	1.000e-20
X14_P16	8.019e-06	1.000e-20
X19_P0	1.828e-04	1.000e-20
X19_P4	6.467e-05	1.000e-20
X19_P10	2.044e-05	1.000e-20
X19_P16	9.352e-06	1.000e-20
X27_P0	2.483e-04	1.000e-20
X27_P4	8.591e-05	1.000e-20
X27_P10	2.644e-05	1.000e-20
X27_P16	1.185e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	5.486e-05	5.099e-05	4.812e-05	4.666e-05
B (output stable)	1.284e-04	1.303e-04	1.343e-04	1.699e-04
A to Z	3.801e-03	3.677e-03	3.688e-03	3.775e-03

B to Z	3.524e-03	3.357e-03	3.312e-03	3.357e-03
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	5.523e-05	5.129e-05	4.821e-05	4.674e-05
B (output stable)	1.289e-04	1.310e-04	1.343e-04	1.702e-04
A to Z	4.719e-03	4.563e-03	4.577e-03	4.678e-03
B to Z	4.455e-03	4.252e-03	4.206e-03	4.266e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	2.205e-05	2.052e-05	1.977e-05	1.838e-05
B (output stable)	4.036e-05	4.177e-05	4.138e-05	4.044e-05
A to Z	6.075e-03	5.835e-03	5.640e-03	5.739e-03
B to Z	5.981e-03	5.698e-03	5.455e-03	5.525e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

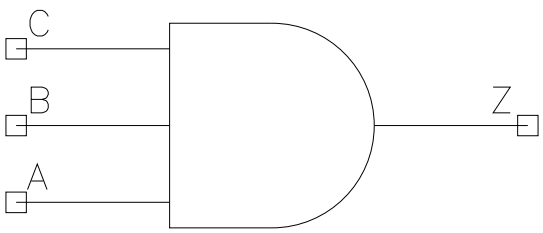
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAND3

Cell Description

3 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	0.800	0.816	0.6528
X10_P4	0.800	0.816	0.6528
X10_P10	0.800	0.816	0.6528
X10_P16	0.800	0.816	0.6528
X14_P0	0.800	1.360	1.0880
X14_P4	0.800	1.360	1.0880
X14_P10	0.800	1.360	1.0880
X14_P16	0.800	1.360	1.0880
X19_P0	0.800	1.496	1.1968
X19_P4	0.800	1.496	1.1968
X19_P10	0.800	1.496	1.1968
X19_P16	0.800	1.496	1.1968
X27_P0	0.800	2.312	1.8496
X27_P4	0.800	2.312	1.8496
X27_P10	0.800	2.312	1.8496
X27_P16	0.800	2.312	1.8496

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X10_P0	X10_P4	X10_P10	X10_P16
A	0.0006	0.0007	0.0007	0.0007
B	0.0006	0.0006	0.0006	0.0006
C	0.0006	0.0006	0.0006	0.0007
	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0011	0.0011	0.0011	0.0012
B	0.0009	0.0009	0.0009	0.0010

C	0.0008	0.0008	0.0009	0.0009
	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0013	0.0013	0.0014	0.0014
B	0.0011	0.0012	0.0012	0.0013
C	0.0010	0.0011	0.0011	0.0012
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0015	0.0015	0.0016	0.0017
B	0.0015	0.0015	0.0016	0.0017
C	0.0015	0.0015	0.0016	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	**X10_P4**	**X10_P0**	**X10_P4**
A to Z ↓	0.0256	0.0294	1.8071	1.9546
A to Z ↑	0.0283	0.0322	2.6563	2.9820
B to Z ↓	0.0245	0.0280	1.8064	1.9508
B to Z ↑	0.0293	0.0330	2.6553	2.9827
C to Z ↓	0.0235	0.0269	1.8043	1.9504
C to Z ↑	0.0300	0.0337	2.6551	2.9834
	X10_P10	**X10_P16**	**X10_P10**	**X10_P16**
A to Z ↓	0.0350	0.0402	2.1648	2.3532
A to Z ↑	0.0383	0.0441	3.4865	3.9610
B to Z ↓	0.0333	0.0381	2.1620	2.3501
B to Z ↑	0.0387	0.0441	3.4860	3.9611
C to Z ↓	0.0318	0.0364	2.1607	2.3468
C to Z ↑	0.0393	0.0446	3.4867	3.9603
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0261	0.0296	1.2440	1.3449
A to Z ↑	0.0275	0.0311	1.8016	2.0246
B to Z ↓	0.0249	0.0283	1.2432	1.3422
B to Z ↑	0.0286	0.0319	1.8001	2.0220
C to Z ↓	0.0239	0.0271	1.2421	1.3425
C to Z ↑	0.0295	0.0330	1.8036	2.0240
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0351	0.0405	1.4897	1.6209
A to Z ↑	0.0369	0.0430	2.3604	2.6819
B to Z ↓	0.0335	0.0386	1.4881	1.6198
B to Z ↑	0.0374	0.0430	2.3607	2.6821
C to Z ↓	0.0320	0.0369	1.4875	1.6184
C to Z ↑	0.0384	0.0439	2.3603	2.6824
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0245	0.0280	0.9260	1.0015
A to Z ↑	0.0266	0.0301	1.3359	1.4989
B to Z ↓	0.0234	0.0266	0.9246	0.9994
B to Z ↑	0.0278	0.0310	1.3366	1.5003
C to Z ↓	0.0224	0.0254	0.9243	0.9988
C to Z ↑	0.0286	0.0317	1.3356	1.5005
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0332	0.0382	1.1088	1.2060
A to Z ↑	0.0357	0.0413	1.7518	1.9908
B to Z ↓	0.0315	0.0363	1.1070	1.2040
B to Z ↑	0.0363	0.0416	1.7504	1.9905

C to Z ↓	0.0299	0.0343	1.1070	1.2035
C to Z ↑	0.0368	0.0419	1.7512	1.9905
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0293	0.0334	0.7898	0.8563
A to Z ↑	0.0274	0.0314	0.7683	0.8629
B to Z ↓	0.0282	0.0322	0.7898	0.8553
B to Z ↑	0.0285	0.0323	0.7679	0.8632
C to Z ↓	0.0278	0.0316	0.7898	0.8552
C to Z ↑	0.0286	0.0321	0.7665	0.8619
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0398	0.0457	0.9479	1.0316
A to Z ↑	0.0375	0.0432	1.0068	1.1459
B to Z ↓	0.0382	0.0438	0.9476	1.0311
B to Z ↑	0.0381	0.0434	1.0079	1.1464
C to Z ↓	0.0375	0.0429	0.9474	1.0314
C to Z ↑	0.0376	0.0426	1.0083	1.1464

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P0	8.732e-05	1.000e-20
X10_P4	3.014e-05	1.000e-20
X10_P10	9.281e-06	1.000e-20
X10_P16	4.174e-06	1.000e-20
X14_P0	1.215e-04	1.000e-20
X14_P4	4.209e-05	1.000e-20
X14_P10	1.303e-05	1.000e-20
X14_P16	5.885e-06	1.000e-20
X19_P0	1.679e-04	1.000e-20
X19_P4	5.819e-05	1.000e-20
X19_P10	1.798e-05	1.000e-20
X19_P16	8.092e-06	1.000e-20
X27_P0	2.747e-04	1.000e-20
X27_P4	9.388e-05	1.000e-20
X27_P10	2.858e-05	1.000e-20
X27_P16	1.274e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X10_P0	X10_P4	X10_P10	X10_P16
A (output stable)	1.403e-05	1.317e-05	1.257e-05	1.217e-05
B (output stable)	1.652e-05	1.527e-05	1.679e-05	2.378e-05
C (output stable)	3.545e-05	3.649e-05	4.600e-05	5.854e-05
A to Z	2.417e-03	2.333e-03	2.331e-03	2.373e-03
B to Z	2.337e-03	2.240e-03	2.221e-03	2.250e-03
C to Z	2.269e-03	2.157e-03	2.119e-03	2.136e-03
	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	1.873e-05	1.720e-05	1.633e-05	1.582e-05
B (output stable)	2.316e-05	2.150e-05	2.279e-05	3.171e-05
C (output stable)	5.096e-05	5.277e-05	6.503e-05	8.153e-05
A to Z	3.562e-03	3.393e-03	3.369e-03	3.460e-03
B to Z	3.429e-03	3.250e-03	3.199e-03	3.274e-03
C to Z	3.329e-03	3.132e-03	3.055e-03	3.114e-03

	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	2.550e-05	2.375e-05	2.269e-05	2.174e-05
B (output stable)	3.229e-05	3.015e-05	3.320e-05	4.670e-05
C (output stable)	7.535e-05	7.751e-05	9.667e-05	1.210e-04
A to Z	4.650e-03	4.428e-03	4.390e-03	4.502e-03
B to Z	4.474e-03	4.228e-03	4.162e-03	4.250e-03
C to Z	4.318e-03	4.045e-03	3.942e-03	4.007e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	5.999e-05	5.643e-05	5.315e-05	5.157e-05
B (output stable)	7.642e-05	7.321e-05	9.130e-05	1.226e-04
C (output stable)	1.771e-04	1.837e-04	2.613e-04	3.098e-04
A to Z	7.249e-03	6.993e-03	7.004e-03	7.134e-03
B to Z	6.969e-03	6.672e-03	6.631e-03	6.729e-03
C to Z	6.734e-03	6.378e-03	6.264e-03	6.316e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

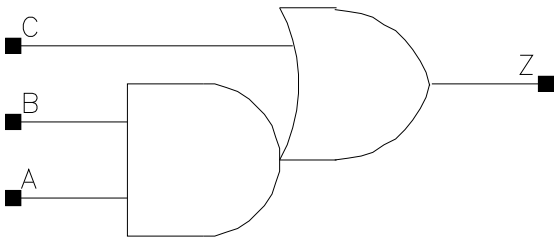
Pin Cycle (vdds)	X10_P0	X10_P4	X10_P10	X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	0.800	1.632	1.3056
X19_P4	0.800	1.632	1.3056
X19_P10	0.800	1.632	1.3056
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0011	0.0011	0.0012	0.0012
B	0.0010	0.0010	0.0010	0.0011
C	0.0010	0.0010	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0322	0.0367	0.9370	1.0150
A to Z ↑	0.0240	0.0272	1.3115	1.4736
B to Z ↓	0.0310	0.0351	0.9364	1.0141
B to Z ↑	0.0258	0.0291	1.3097	1.4736
C to Z ↓	0.0315	0.0362	0.9349	1.0115
C to Z ↑	0.0237	0.0268	1.3039	1.4648
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0436	0.0502	1.1252	1.2257

A to Z ↑	0.0320	0.0365	1.7219	1.9551
B to Z ↓	0.0416	0.0478	1.1244	1.2251
B to Z ↑	0.0340	0.0385	1.7216	1.9558
C to Z ↓	0.0434	0.0503	1.1215	1.2225
C to Z ↑	0.0313	0.0353	1.7124	1.9456

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X19_P0	1.696e-04	1.000e-20
X19_P4	6.187e-05	1.000e-20
X19_P10	2.022e-05	1.000e-20
X19_P16	9.474e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	7.061e-05	6.886e-05	5.362e-05	3.598e-05
B (output stable)	7.888e-05	7.780e-05	6.180e-05	4.376e-05
C (output stable)	1.053e-04	1.009e-04	9.962e-05	1.004e-04
A to Z	4.632e-03	4.410e-03	4.348e-03	4.395e-03
B to Z	4.516e-03	4.266e-03	4.173e-03	4.197e-03
C to Z	4.894e-03	4.736e-03	4.746e-03	4.840e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

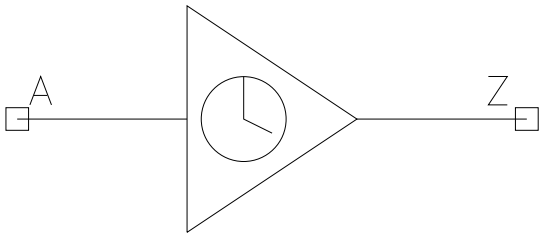
Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNBF

Cell Description

Buffer with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_CNBFX2_P0	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX2_P4	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX2_-P10	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX2_-P16	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_P0	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_P4	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_-P10	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_-P16	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX8_P0	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX8_P4	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX8_-P10	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX8_-P16	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX12_-P0	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX12_-P4	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX12_-P10	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX12_-P16	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX18_-P0	0.800	0.952	0.7616
C8T28SOI_LL_CNBFX18_-P4	0.800	0.952	0.7616
C8T28SOI_LL_CNBFX18_-P10	0.800	0.952	0.7616
C8T28SOI_LL_CNBFX18_-P16	0.800	0.952	0.7616

C8T28SOI_LL_CNBFX23_-P0	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX23_-P4	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX23_-P10	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX23_-P16	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX28_-P0	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX28_-P4	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX28_-P10	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX28_-P16	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX32_-P0	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX32_-P4	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX32_-P10	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX32_-P16	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX37_-P0	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX37_-P4	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX37_-P10	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX37_-P16	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX54_-P0	0.800	2.312	1.8496
C8T28SOI_LL_CNBFX54_-P4	0.800	2.312	1.8496
C8T28SOI_LL_CNBFX54_-P10	0.800	2.312	1.8496
C8T28SOI_LL_CNBFX54_-P16	0.800	2.312	1.8496
C8T28SOIDV_LL_-CNBFX18_P0	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX18_P4	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX18_P10	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX18_P16	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX28_P0	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNBFX28_P4	1.600	0.680	1.0880

C8T28SOIDV_LL_-CNBFX28_P10	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNBFX28_P16	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNBFX37_P0	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX37_P4	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX37_P10	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX37_P16	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX55_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX55_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX55_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX55_P16	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX74_P0	1.600	1.632	2.6112
C8T28SOIDV_LL_-CNBFX74_P4	1.600	1.632	2.6112
C8T28SOIDV_LL_-CNBFX74_P10	1.600	1.632	2.6112
C8T28SOIDV_LL_-CNBFX74_P16	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C8T28SOI_LL_-CNBFX2_P0	C8T28SOI_LL_-CNBFX2_P4	C8T28SOI_LL_-CNBFX2_P10	C8T28SOI_LL_-CNBFX2_P16
A	0.0005	0.0005	0.0005	0.0005
	C8T28SOI_LL_-CNBFX4_P0	C8T28SOI_LL_-CNBFX4_P4	C8T28SOI_LL_-CNBFX4_P10	C8T28SOI_LL_-CNBFX4_P16
A	0.0005	0.0005	0.0005	0.0005
	C8T28SOI_LL_-CNBFX8_P0	C8T28SOI_LL_-CNBFX8_P4	C8T28SOI_LL_-CNBFX8_P10	C8T28SOI_LL_-CNBFX8_P16
A	0.0006	0.0006	0.0006	0.0007
	C8T28SOI_LL_-CNBFX12_P0	C8T28SOI_LL_-CNBFX12_P4	C8T28SOI_LL_-CNBFX12_P10	C8T28SOI_LL_-CNBFX12_P16
A	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LL_-CNBFX18_P0	C8T28SOI_LL_-CNBFX18_P4	C8T28SOI_LL_-CNBFX18_P10	C8T28SOI_LL_-CNBFX18_P16
A	0.0008	0.0009	0.0009	0.0010
	C8T28SOI_LL_-CNBFX23_P0	C8T28SOI_LL_-CNBFX23_P4	C8T28SOI_LL_-CNBFX23_P10	C8T28SOI_LL_-CNBFX23_P16
A	0.0010	0.0010	0.0011	0.0011

	C8T28SOI_LL_-CNBFX28_P0	C8T28SOI_LL_-CNBFX28_P4	C8T28SOI_LL_-CNBFX28_P10	C8T28SOI_LL_-CNBFX28_P16
A	0.0011	0.0012	0.0012	0.0013
	C8T28SOI_LL_-CNBFX32_P0	C8T28SOI_LL_-CNBFX32_P4	C8T28SOI_LL_-CNBFX32_P10	C8T28SOI_LL_-CNBFX32_P16
A	0.0014	0.0015	0.0016	0.0017
	C8T28SOI_LL_-CNBFX37_P0	C8T28SOI_LL_-CNBFX37_P4	C8T28SOI_LL_-CNBFX37_P10	C8T28SOI_LL_-CNBFX37_P16
A	0.0015	0.0016	0.0017	0.0018
	C8T28SOI_LL_-CNBFX54_P0	C8T28SOI_LL_-CNBFX54_P4	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A	0.0021	0.0022	0.0023	0.0025
	C8T28SOIDV_LL_-CNBFX18_P0	C8T28SOIDV_LL_-CNBFX18_P4	C8T28SOIDV_LL_-CNBFX18_P10	C8T28SOIDV_LL_-CNBFX18_P16
A	0.0011	0.0011	0.0012	0.0013
	C8T28SOIDV_LL_-CNBFX28_P0	C8T28SOIDV_LL_-CNBFX28_P4	C8T28SOIDV_LL_-CNBFX28_P10	C8T28SOIDV_LL_-CNBFX28_P16
A	0.0012	0.0012	0.0013	0.0014
	C8T28SOIDV_LL_-CNBFX37_P0	C8T28SOIDV_LL_-CNBFX37_P4	C8T28SOIDV_LL_-CNBFX37_P10	C8T28SOIDV_LL_-CNBFX37_P16
A	0.0015	0.0016	0.0018	0.0018
	C8T28SOIDV_LL_-CNBFX55_P0	C8T28SOIDV_LL_-CNBFX55_P4	C8T28SOIDV_LL_-CNBFX55_P10	C8T28SOIDV_LL_-CNBFX55_P16
A	0.0021	0.0022	0.0024	0.0025
	C8T28SOIDV_LL_-CNBFX74_P0	C8T28SOIDV_LL_-CNBFX74_P4	C8T28SOIDV_LL_-CNBFX74_P10	C8T28SOIDV_LL_-CNBFX74_P16
A	0.0027	0.0029	0.0030	0.0032

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-CNBFX2_P0	**C8T28SOI_LL_-CNBFX2_P4**	**C8T28SOI_LL_-CNBFX2_P0**	**C8T28SOI_LL_-CNBFX2_P4**
A to Z ↓	0.0244	0.0277	7.8340	8.4417
A to Z ↑	0.0194	0.0221	10.6594	12.0658
	C8T28SOI_LL_-CNBFX2_P10	**C8T28SOI_LL_-CNBFX2_P16**	**C8T28SOI_LL_-CNBFX2_P10**	**C8T28SOI_LL_-CNBFX2_P16**
A to Z ↓	0.0326	0.0371	9.3075	10.0838
A to Z ↑	0.0261	0.0297	14.2177	16.2937
	C8T28SOI_LL_-CNBFX4_P0	**C8T28SOI_LL_-CNBFX4_P4**	**C8T28SOI_LL_-CNBFX4_P0**	**C8T28SOI_LL_-CNBFX4_P4**
A to Z ↓	0.0250	0.0285	4.5072	4.8692
A to Z ↑	0.0185	0.0212	5.5529	6.2325
	C8T28SOI_LL_-CNBFX4_P10	**C8T28SOI_LL_-CNBFX4_P16**	**C8T28SOI_LL_-CNBFX4_P10**	**C8T28SOI_LL_-CNBFX4_P16**
A to Z ↓	0.0336	0.0384	5.3877	5.8566
A to Z ↑	0.0250	0.0283	7.2930	8.2809
	C8T28SOI_LL_-CNBFX8_P0	**C8T28SOI_LL_-CNBFX8_P4**	**C8T28SOI_LL_-CNBFX8_P0**	**C8T28SOI_LL_-CNBFX8_P4**
A to Z ↓	0.0234	0.0266	2.2502	2.4368
A to Z ↑	0.0179	0.0205	2.6938	3.0322
	C8T28SOI_LL_-CNBFX8_P10	**C8T28SOI_LL_-CNBFX8_P16**	**C8T28SOI_LL_-CNBFX8_P10**	**C8T28SOI_LL_-CNBFX8_P16**
A to Z ↓	0.0316	0.0362	2.6989	2.9329

A to Z ↑	0.0241	0.0274	3.5394	4.0287
	C8T28SOI_LL_-CNBFX12_P0	**C8T28SOI_LL_-CNBFX12_P4**	**C8T28SOI_LL_-CNBFX12_P0**	**C8T28SOI_LL_-CNBFX12_P4**
A to Z ↓	0.0250	0.0286	1.5354	1.6615
A to Z ↑	0.0215	0.0244	1.7709	1.9912
	C8T28SOI_LL_-CNBFX12_P10	**C8T28SOI_LL_-CNBFX12_P16**	**C8T28SOI_LL_-CNBFX12_P10**	**C8T28SOI_LL_-CNBFX12_P16**
A to Z ↓	0.0341	0.0394	1.8396	2.0011
A to Z ↑	0.0286	0.0324	2.3299	2.6489
	C8T28SOI_LL_-CNBFX18_P0	**C8T28SOI_LL_-CNBFX18_P4**	**C8T28SOI_LL_-CNBFX18_P0**	**C8T28SOI_LL_-CNBFX18_P4**
A to Z ↓	0.0240	0.0275	0.9953	1.0799
A to Z ↑	0.0191	0.0219	1.3210	1.4854
	C8T28SOI_LL_-CNBFX18_P10	**C8T28SOI_LL_-CNBFX18_P16**	**C8T28SOI_LL_-CNBFX18_P10**	**C8T28SOI_LL_-CNBFX18_P16**
A to Z ↓	0.0327	0.0374	1.1972	1.3039
A to Z ↑	0.0257	0.0291	1.7372	1.9737
	C8T28SOI_LL_-CNBFX23_P0	**C8T28SOI_LL_-CNBFX23_P4**	**C8T28SOI_LL_-CNBFX23_P0**	**C8T28SOI_LL_-CNBFX23_P4**
A to Z ↓	0.0243	0.0276	0.7758	0.8399
A to Z ↑	0.0192	0.0218	1.0539	1.1844
	C8T28SOI_LL_-CNBFX23_P10	**C8T28SOI_LL_-CNBFX23_P16**	**C8T28SOI_LL_-CNBFX23_P10**	**C8T28SOI_LL_-CNBFX23_P16**
A to Z ↓	0.0330	0.0377	0.9315	1.0138
A to Z ↑	0.0259	0.0292	1.3881	1.5786
	C8T28SOI_LL_-CNBFX28_P0	**C8T28SOI_LL_-CNBFX28_P4**	**C8T28SOI_LL_-CNBFX28_P0**	**C8T28SOI_LL_-CNBFX28_P4**
A to Z ↓	0.0240	0.0275	0.6403	0.6944
A to Z ↑	0.0191	0.0219	0.8829	0.9934
	C8T28SOI_LL_-CNBFX28_P10	**C8T28SOI_LL_-CNBFX28_P16**	**C8T28SOI_LL_-CNBFX28_P10**	**C8T28SOI_LL_-CNBFX28_P16**
A to Z ↓	0.0324	0.0372	0.7701	0.8379
A to Z ↑	0.0255	0.0289	1.1616	1.3204
	C8T28SOI_LL_-CNBFX32_P0	**C8T28SOI_LL_-CNBFX32_P4**	**C8T28SOI_LL_-CNBFX32_P0**	**C8T28SOI_LL_-CNBFX32_P4**
A to Z ↓	0.0250	0.0286	0.5554	0.6018
A to Z ↑	0.0194	0.0222	0.7582	0.8543
	C8T28SOI_LL_-CNBFX32_P10	**C8T28SOI_LL_-CNBFX32_P16**	**C8T28SOI_LL_-CNBFX32_P10**	**C8T28SOI_LL_-CNBFX32_P16**
A to Z ↓	0.0337	0.0387	0.6663	0.7258
A to Z ↑	0.0260	0.0294	0.9980	1.1342
	C8T28SOI_LL_-CNBFX37_P0	**C8T28SOI_LL_-CNBFX37_P4**	**C8T28SOI_LL_-CNBFX37_P0**	**C8T28SOI_LL_-CNBFX37_P4**
A to Z ↓	0.0245	0.0278	0.4812	0.5217
A to Z ↑	0.0195	0.0222	0.6629	0.7451
	C8T28SOI_LL_-CNBFX37_P10	**C8T28SOI_LL_-CNBFX37_P16**	**C8T28SOI_LL_-CNBFX37_P10**	**C8T28SOI_LL_-CNBFX37_P16**
A to Z ↓	0.0331	0.0379	0.5790	0.6307
A to Z ↑	0.0261	0.0295	0.8724	0.9917
	C8T28SOI_LL_-CNBFX54_P0	**C8T28SOI_LL_-CNBFX54_P4**	**C8T28SOI_LL_-CNBFX54_P0**	**C8T28SOI_LL_-CNBFX54_P4**
A to Z ↓	0.0240	0.0275	0.3370	0.3653
A to Z ↑	0.0198	0.0225	0.4432	0.4978

	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A to Z ↓	0.0325	0.0374	0.4058	0.4422
A to Z ↑	0.0263	0.0299	0.5824	0.6626
	C8T28SOIDV_LL_-CNBFX18_P0	**C8T28SOIDV_LL_-CNBFX18_P4**	**C8T28SOIDV_LL_-CNBFX18_P0**	**C8T28SOIDV_LL_-CNBFX18_P4**
A to Z ↓	0.0220	0.0251	0.9194	0.9954
A to Z ↑	0.0194	0.0220	1.3041	1.4697
	C8T28SOIDV_LL_-CNBFX18_P10	**C8T28SOIDV_LL_-CNBFX18_P16**	**C8T28SOIDV_LL_-CNBFX18_P10**	**C8T28SOIDV_LL_-CNBFX18_P16**
A to Z ↓	0.0299	0.0344	1.1047	1.2030
A to Z ↑	0.0258	0.0293	1.7180	1.9553
	C8T28SOIDV_LL_-CNBFX28_P0	**C8T28SOIDV_LL_-CNBFX28_P4**	**C8T28SOIDV_LL_-CNBFX28_P0**	**C8T28SOIDV_LL_-CNBFX28_P4**
A to Z ↓	0.0246	0.0284	0.6220	0.6747
A to Z ↑	0.0202	0.0232	0.8872	0.9963
	C8T28SOIDV_LL_-CNBFX28_P10	**C8T28SOIDV_LL_-CNBFX28_P16**	**C8T28SOIDV_LL_-CNBFX28_P10**	**C8T28SOIDV_LL_-CNBFX28_P16**
A to Z ↓	0.0333	0.0389	0.7501	0.8181
A to Z ↑	0.0268	0.0308	1.1662	1.3259
	C8T28SOIDV_LL_-CNBFX37_P0	**C8T28SOIDV_LL_-CNBFX37_P4**	**C8T28SOIDV_LL_-CNBFX37_P0**	**C8T28SOIDV_LL_-CNBFX37_P4**
A to Z ↓	0.0238	0.0274	0.4685	0.5090
A to Z ↑	0.0191	0.0219	0.6655	0.7489
	C8T28SOIDV_LL_-CNBFX37_P10	**C8T28SOIDV_LL_-CNBFX37_P16**	**C8T28SOIDV_LL_-CNBFX37_P10**	**C8T28SOIDV_LL_-CNBFX37_P16**
A to Z ↓	0.0329	0.0377	0.5663	0.6176
A to Z ↑	0.0261	0.0294	0.8758	0.9943
	C8T28SOIDV_LL_-CNBFX55_P0	**C8T28SOIDV_LL_-CNBFX55_P4**	**C8T28SOIDV_LL_-CNBFX55_P0**	**C8T28SOIDV_LL_-CNBFX55_P4**
A to Z ↓	0.0236	0.0269	0.3170	0.3441
A to Z ↑	0.0194	0.0220	0.4433	0.4990
	C8T28SOIDV_LL_-CNBFX55_P10	**C8T28SOIDV_LL_-CNBFX55_P16**	**C8T28SOIDV_LL_-CNBFX55_P10**	**C8T28SOIDV_LL_-CNBFX55_P16**
A to Z ↓	0.0322	0.0373	0.3828	0.4177
A to Z ↑	0.0259	0.0295	0.5824	0.6622
	C8T28SOIDV_LL_-CNBFX74_P0	**C8T28SOIDV_LL_-CNBFX74_P4**	**C8T28SOIDV_LL_-CNBFX74_P0**	**C8T28SOIDV_LL_-CNBFX74_P4**
A to Z ↓	0.0247	0.0283	0.2407	0.2613
A to Z ↑	0.0212	0.0241	0.3351	0.3766
	C8T28SOIDV_LL_-CNBFX74_P10	**C8T28SOIDV_LL_-CNBFX74_P16**	**C8T28SOIDV_LL_-CNBFX74_P10**	**C8T28SOIDV_LL_-CNBFX74_P16**
A to Z ↓	0.0337	0.0389	0.2910	0.3177
A to Z ↑	0.0282	0.0320	0.4404	0.5001

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_CNBFX2_P0	2.336e-05	1.000e-20
C8T28SOI_LL_CNBFX2_P4	8.554e-06	1.000e-20
C8T28SOI_LL_CNBFX2_P10	2.858e-06	1.000e-20
C8T28SOI_LL_CNBFX2_P16	1.371e-06	1.000e-20
C8T28SOI_LL_CNBFX4_P0	3.829e-05	1.000e-20

C8T28SOI_LL_CNBFX4_P4	1.386e-05	1.000e-20
C8T28SOI_LL_CNBFX4_P10	4.527e-06	1.000e-20
C8T28SOI_LL_CNBFX4_P16	2.129e-06	1.000e-20
C8T28SOI_LL_CNBFX8_P0	7.505e-05	1.000e-20
C8T28SOI_LL_CNBFX8_P4	2.661e-05	1.000e-20
C8T28SOI_LL_CNBFX8_P10	8.461e-06	1.000e-20
C8T28SOI_LL_CNBFX8_P16	3.899e-06	1.000e-20
C8T28SOI_LL_CNBFX12_P0	1.055e-04	1.000e-20
C8T28SOI_LL_CNBFX12_P4	3.707e-05	1.000e-20
C8T28SOI_LL_CNBFX12_P10	1.165e-05	1.000e-20
C8T28SOI_LL_CNBFX12_P16	5.322e-06	1.000e-20
C8T28SOI_LL_CNBFX18_P0	1.381e-04	1.000e-20
C8T28SOI_LL_CNBFX18_P4	4.919e-05	1.000e-20
C8T28SOI_LL_CNBFX18_P10	1.569e-05	1.000e-20
C8T28SOI_LL_CNBFX18_P16	7.235e-06	1.000e-20
C8T28SOI_LL_CNBFX23_P0	1.767e-04	1.000e-20
C8T28SOI_LL_CNBFX23_P4	6.255e-05	1.000e-20
C8T28SOI_LL_CNBFX23_P10	1.984e-05	1.000e-20
C8T28SOI_LL_CNBFX23_P16	9.121e-06	1.000e-20
C8T28SOI_LL_CNBFX28_P0	2.112e-04	1.000e-20
C8T28SOI_LL_CNBFX28_P4	7.507e-05	1.000e-20
C8T28SOI_LL_CNBFX28_P10	2.382e-05	1.000e-20
C8T28SOI_LL_CNBFX28_P16	1.093e-05	1.000e-20
C8T28SOI_LL_CNBFX32_P0	2.387e-04	1.000e-20
C8T28SOI_LL_CNBFX32_P4	8.494e-05	1.000e-20
C8T28SOI_LL_CNBFX32_P10	2.706e-05	1.000e-20
C8T28SOI_LL_CNBFX32_P16	1.247e-05	1.000e-20
C8T28SOI_LL_CNBFX37_P0	2.817e-04	1.000e-20
C8T28SOI_LL_CNBFX37_P4	9.976e-05	1.000e-20
C8T28SOI_LL_CNBFX37_P10	3.156e-05	1.000e-20
C8T28SOI_LL_CNBFX37_P16	1.446e-05	1.000e-20
C8T28SOI_LL_CNBFX54_P0	4.205e-04	1.000e-20
C8T28SOI_LL_CNBFX54_P4	1.476e-04	1.000e-20
C8T28SOI_LL_CNBFX54_P10	4.626e-05	1.000e-20
C8T28SOI_LL_CNBFX54_P16	2.107e-05	1.000e-20
C8T28SOIDV_LL_CNBFX18_P0	1.619e-04	1.000e-20
C8T28SOIDV_LL_CNBFX18_P4	5.720e-05	1.000e-20
C8T28SOIDV_LL_CNBFX18_P10	1.805e-05	1.000e-20
C8T28SOIDV_LL_CNBFX18_P16	8.264e-06	1.000e-20
C8T28SOIDV_LL_CNBFX28_P0	2.246e-04	1.000e-20
C8T28SOIDV_LL_CNBFX28_P4	7.912e-05	1.000e-20
C8T28SOIDV_LL_CNBFX28_P10	2.485e-05	1.000e-20
C8T28SOIDV_LL_CNBFX28_P16	1.133e-05	1.000e-20
C8T28SOIDV_LL_CNBFX37_P0	2.923e-04	1.000e-20
C8T28SOIDV_LL_CNBFX37_P4	1.027e-04	1.000e-20
C8T28SOIDV_LL_CNBFX37_P10	3.219e-05	1.000e-20
C8T28SOIDV_LL_CNBFX37_P16	1.466e-05	1.000e-20
C8T28SOIDV_LL_CNBFX55_P0	4.331e-04	1.000e-20
C8T28SOIDV_LL_CNBFX55_P4	1.520e-04	1.000e-20
C8T28SOIDV_LL_CNBFX55_P10	4.751e-05	1.000e-20
C8T28SOIDV_LL_CNBFX55_P16	2.158e-05	1.000e-20
C8T28SOIDV_LL_CNBFX74_P0	5.543e-04	1.000e-20

C8T28SOIDV_LL_CNBFX74_P4	1.947e-04	1.000e-20
C8T28SOIDV_LL_CNBFX74_P10	6.088e-05	1.000e-20
C8T28SOIDV_LL_CNBFX74_P16	2.764e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_-CNBFX2_P0	C8T28SOI_LL_-CNBFX2_P4	C8T28SOI_LL_-CNBFX2_P10	C8T28SOI_LL_-CNBFX2_P16
A to Z	8.640e-04	8.365e-04	8.345e-04	8.495e-04
	C8T28SOI_LL_-CNBFX4_P0	C8T28SOI_LL_-CNBFX4_P4	C8T28SOI_LL_-CNBFX4_P10	C8T28SOI_LL_-CNBFX4_P16
A to Z	1.088e-03	1.053e-03	1.054e-03	1.077e-03
	C8T28SOI_LL_-CNBFX8_P0	C8T28SOI_LL_-CNBFX8_P4	C8T28SOI_LL_-CNBFX8_P10	C8T28SOI_LL_-CNBFX8_P16
A to Z	1.783e-03	1.703e-03	1.689e-03	1.723e-03
	C8T28SOI_LL_-CNBFX12_P0	C8T28SOI_LL_-CNBFX12_P4	C8T28SOI_LL_-CNBFX12_P10	C8T28SOI_LL_-CNBFX12_P16
A to Z	2.643e-03	2.525e-03	2.502e-03	2.551e-03
	C8T28SOI_LL_-CNBFX18_P0	C8T28SOI_LL_-CNBFX18_P4	C8T28SOI_LL_-CNBFX18_P10	C8T28SOI_LL_-CNBFX18_P16
A to Z	3.533e-03	3.381e-03	3.339e-03	3.375e-03
	C8T28SOI_LL_-CNBFX23_P0	C8T28SOI_LL_-CNBFX23_P4	C8T28SOI_LL_-CNBFX23_P10	C8T28SOI_LL_-CNBFX23_P16
A to Z	4.518e-03	4.272e-03	4.283e-03	4.330e-03
	C8T28SOI_LL_-CNBFX28_P0	C8T28SOI_LL_-CNBFX28_P4	C8T28SOI_LL_-CNBFX28_P10	C8T28SOI_LL_-CNBFX28_P16
A to Z	5.237e-03	5.003e-03	4.887e-03	4.947e-03
	C8T28SOI_LL_-CNBFX32_P0	C8T28SOI_LL_-CNBFX32_P4	C8T28SOI_LL_-CNBFX32_P10	C8T28SOI_LL_-CNBFX32_P16
A to Z	6.327e-03	6.051e-03	5.945e-03	6.032e-03
	C8T28SOI_LL_-CNBFX37_P0	C8T28SOI_LL_-CNBFX37_P4	C8T28SOI_LL_-CNBFX37_P10	C8T28SOI_LL_-CNBFX37_P16
A to Z	7.200e-03	6.822e-03	6.746e-03	6.834e-03
	C8T28SOI_LL_-CNBFX54_P0	C8T28SOI_LL_-CNBFX54_P4	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A to Z	1.042e-02	9.879e-03	9.687e-03	9.888e-03
	C8T28SOIDV_LL_-CNBFX18_P0	C8T28SOIDV_LL_-CNBFX18_P4	C8T28SOIDV_LL_-CNBFX18_P10	C8T28SOIDV_LL_-CNBFX18_P16
A to Z	3.658e-03	3.491e-03	3.469e-03	3.548e-03
	C8T28SOIDV_LL_-CNBFX28_P0	C8T28SOIDV_LL_-CNBFX28_P4	C8T28SOIDV_LL_-CNBFX28_P10	C8T28SOIDV_LL_-CNBFX28_P16
A to Z	5.439e-03	5.249e-03	5.118e-03	5.298e-03
	C8T28SOIDV_LL_-CNBFX37_P0	C8T28SOIDV_LL_-CNBFX37_P4	C8T28SOIDV_LL_-CNBFX37_P10	C8T28SOIDV_LL_-CNBFX37_P16
A to Z	6.919e-03	6.590e-03	6.611e-03	6.686e-03
	C8T28SOIDV_LL_-CNBFX55_P0	C8T28SOIDV_LL_-CNBFX55_P4	C8T28SOIDV_LL_-CNBFX55_P10	C8T28SOIDV_LL_-CNBFX55_P16
A to Z	1.021e-02	9.715e-03	9.663e-03	9.911e-03
	C8T28SOIDV_LL_-CNBFX74_P0	C8T28SOIDV_LL_-CNBFX74_P4	C8T28SOIDV_LL_-CNBFX74_P10	C8T28SOIDV_LL_-CNBFX74_P16
A to Z	1.378e-02	1.319e-02	1.296e-02	1.330e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

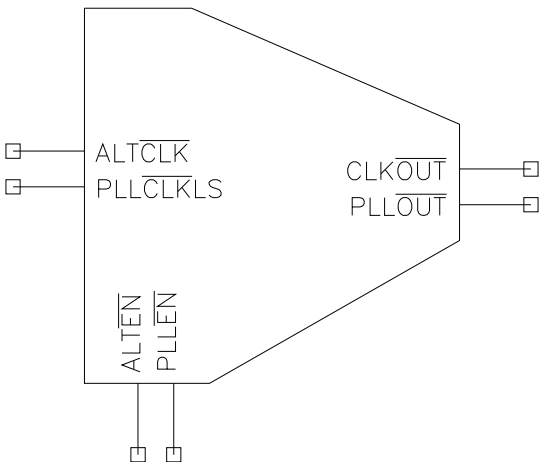
Pin Cycle (vdds)	C8T28SOI_LL_-CNBFX2_P0	C8T28SOI_LL_-CNBFX2_P4	C8T28SOI_LL_-CNBFX2_P10	C8T28SOI_LL_-CNBFX2_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX4_P0	C8T28SOI_LL_-CNBFX4_P4	C8T28SOI_LL_-CNBFX4_P10	C8T28SOI_LL_-CNBFX4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX8_P0	C8T28SOI_LL_-CNBFX8_P4	C8T28SOI_LL_-CNBFX8_P10	C8T28SOI_LL_-CNBFX8_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX12_P0	C8T28SOI_LL_-CNBFX12_P4	C8T28SOI_LL_-CNBFX12_P10	C8T28SOI_LL_-CNBFX12_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX18_P0	C8T28SOI_LL_-CNBFX18_P4	C8T28SOI_LL_-CNBFX18_P10	C8T28SOI_LL_-CNBFX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX23_P0	C8T28SOI_LL_-CNBFX23_P4	C8T28SOI_LL_-CNBFX23_P10	C8T28SOI_LL_-CNBFX23_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX28_P0	C8T28SOI_LL_-CNBFX28_P4	C8T28SOI_LL_-CNBFX28_P10	C8T28SOI_LL_-CNBFX28_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX32_P0	C8T28SOI_LL_-CNBFX32_P4	C8T28SOI_LL_-CNBFX32_P10	C8T28SOI_LL_-CNBFX32_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX37_P0	C8T28SOI_LL_-CNBFX37_P4	C8T28SOI_LL_-CNBFX37_P10	C8T28SOI_LL_-CNBFX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX54_P0	C8T28SOI_LL_-CNBFX54_P4	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX18_P0	C8T28SOIDV_LL_-CNBFX18_P4	C8T28SOIDV_LL_-CNBFX18_P10	C8T28SOIDV_LL_-CNBFX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX28_P0	C8T28SOIDV_LL_-CNBFX28_P4	C8T28SOIDV_LL_-CNBFX28_P10	C8T28SOIDV_LL_-CNBFX28_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX37_P0	C8T28SOIDV_LL_-CNBFX37_P4	C8T28SOIDV_LL_-CNBFX37_P10	C8T28SOIDV_LL_-CNBFX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX55_P0	C8T28SOIDV_LL_-CNBFX55_P4	C8T28SOIDV_LL_-CNBFX55_P10	C8T28SOIDV_LL_-CNBFX55_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX74_P0	C8T28SOIDV_LL_-CNBFX74_P4	C8T28SOIDV_LL_-CNBFX74_P10	C8T28SOIDV_LL_-CNBFX74_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNGFMUX21

Cell Description

2:1 Glitch-free MUX for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X30_P0	1.600	4.488	7.1808
X30_P4	1.600	4.488	7.1808
X30_P10	1.600	4.488	7.1808
X30_P16	1.600	4.488	7.1808

Truth Table

PLL_CLK_LS	ALT_CLK	IPLL_EN_LD	IALT_EN_LD	CLK_OUT
0	-	-	0	0
0	0	-	-	0
-	0	0	-	0
PLL_CLK_LS	1	-	1	1
1	ALT_CLK	1	-	1
1	1	0	0	0

PLL_CLK_LS	PLL_OUT
PLL_CLK_LS	PLL_CLK_LS
1	1

PLL_EN	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD
PLL_EN	0	-	PLL_EN
-	-	IPLL_EN_LD	IPLL_EN_LD
-	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

ALT_EN	ALT_CLK	IALT_EN_LD	IALT_EN_LD
ALT_EN	0	-	ALT_EN
-	-	IALT_EN_LD	IALT_EN_LD
-	ALT_CLK	IALT_EN_LD	IALT_EN_LD

Pin Capacitance

Pin	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK	0.0024	0.0025	0.0026	0.0027
ALT_EN	0.0004	0.0004	0.0005	0.0005
PLL_CLK_LS	0.0041	0.0042	0.0044	0.0046
PLL_EN	0.0004	0.0004	0.0004	0.0005

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**
ALT_CLK to CLK_OUT ↓	0.0330	0.0376	0.6807	0.7402
ALT_CLK to CLK_OUT ↑	0.0305	0.0349	0.9658	1.0853
PLL_CLK_LS to CLK_OUT ↓	0.0317	0.0358	0.6845	0.7443
PLL_CLK_LS to CLK_OUT ↑	0.0315	0.0355	0.9708	1.0910
PLL_CLK_LS to PLL_OUT ↓	0.0209	0.0236	0.5451	0.5887
PLL_CLK_LS to PLL_OUT ↑	0.0206	0.0231	0.8872	0.9981
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
ALT_CLK to CLK_OUT ↓	0.0446	0.0514	0.8265	0.9057
ALT_CLK to CLK_OUT ↑	0.0418	0.0487	1.2696	1.4441
PLL_CLK_LS to CLK_OUT ↓	0.0423	0.0483	0.8307	0.9094
PLL_CLK_LS to CLK_OUT ↑	0.0417	0.0474	1.2753	1.4510
PLL_CLK_LS to PLL_OUT ↓	0.0281	0.0322	0.6517	0.7081
PLL_CLK_LS to PLL_OUT ↑	0.0271	0.0306	1.1673	1.3276

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0633	0.0678	0.0816	0.0908
ALT_EN ↓	hold_rising to ALT_CLK	-0.0292	-0.0367	-0.0464	-0.0562
ALT_EN ↑	hold_rising to ALT_CLK	-0.0045	-0.0066	-0.0110	-0.0165
ALT_EN ↓	setup_rising to ALT_CLK	0.0591	0.0666	0.0812	0.0964

ALT_EN ↑	setup_rising to ALT_CLK	0.0337	0.0412	0.0509	0.0612
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0553	0.0633	0.0725	0.0816
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0247	-0.0318	-0.0442	-0.0567
PLL_EN ↑	hold_rising to PLL_CLK_LS	0.0003	-0.0017	-0.0071	-0.0120
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0520	0.0564	0.0720	0.0812
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0347	0.0395	0.0519	0.0622

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X30_P0	7.709e-04	1.000e-20
X30_P4	2.762e-04	1.000e-20
X30_P10	8.897e-05	1.000e-20
X30_P16	4.141e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	2.728e-03	2.721e-03	2.788e-03	2.897e-03
ALT_EN (output stable)	1.632e-03	1.598e-03	1.608e-03	1.653e-03
PLL_CLK_LS (output stable)	1.478e-02	1.015e-02	8.598e-03	8.423e-03
PLL_EN (output stable)	1.436e-03	1.427e-03	1.464e-03	1.514e-03
ALT_CLK to CLK_OUT	9.203e-03	9.106e-03	9.309e-03	9.665e-03
PLL_CLK_LS to CLK_OUT	6.546e-03	6.271e-03	6.281e-03	6.406e-03
PLL_CLK_LS to PLL_OUT	1.756e-02	1.072e-02	8.243e-03	7.728e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_CLK to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00

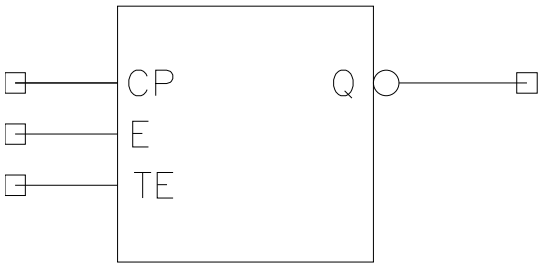
PLL_CLK_LS to PLL_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNHLS

Cell Description

Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LLP1_-CNHLSX10_P0	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX10_P4	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX10_P10	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX10_P16	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX14_P0	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX14_P4	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX14_P10	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX14_P16	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX19_P0	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX19_P4	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX19_P10	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX19_P16	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX24_P0	0.800	2.584	2.0672
C8T28SOI_LLP1_-CNHLSX24_P4	0.800	2.584	2.0672
C8T28SOI_LLP1_-CNHLSX24_P10	0.800	2.584	2.0672
C8T28SOI_LLP1_-CNHLSX24_P16	0.800	2.584	2.0672

C8T28SOI_LLP1_-CNHLSX29_P0	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX29_P4	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX29_P10	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX29_P16	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX34_P0	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX34_P4	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX34_P10	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX34_P16	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX38_P0	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX38_P4	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX38_P10	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX38_P16	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX57_P0	0.800	4.080	3.2640
C8T28SOI_LLP1_-CNHLSX57_P4	0.800	4.080	3.2640
C8T28SOI_LLP1_-CNHLSX57_P10	0.800	4.080	3.2640
C8T28SOI_LLP1_-CNHLSX57_P16	0.800	4.080	3.2640
C8T28SOI_LLP_-CNHLSX4_P0	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX4_P4	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX4_P10	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX4_P16	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX9_P0	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX9_P4	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX9_P10	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX9_P16	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX13_P0	0.800	2.312	1.8496
C8T28SOI_LLP_-CNHLSX13_P4	0.800	2.312	1.8496

C8T28SOI_LLP_-CNHLSX13_P10	0.800	2.312	1.8496
C8T28SOI_LLP_-CNHLSX13_P16	0.800	2.312	1.8496
C8T28SOI_LLP_-CNHLSX17_P0	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX17_P4	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX17_P10	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX17_P16	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX21_P0	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX21_P4	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX21_P10	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX21_P16	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX27_P0	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX27_P4	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX27_P10	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX27_P16	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX30_P0	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX30_P4	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX30_P10	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX30_P16	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX38_P0	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX38_P4	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX38_P10	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX38_P16	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX54_P0	0.800	5.304	4.2432
C8T28SOI_LLP_-CNHLSX54_P4	0.800	5.304	4.2432
C8T28SOI_LLP_-CNHLSX54_P10	0.800	5.304	4.2432
C8T28SOI_LLP_-CNHLSX54_P16	0.800	5.304	4.2432

Truth Table

CP	E	TE	OLDIE	Q
0	-	-	-	0
1	-	-	OLDIE	OLDIE

OLDIE	OLDIE
OLDIE	OLDIE

Pin Capacitance

Pin	C8T28SOI_LLP1_-CNHLSX10_P0	C8T28SOI_LLP1_-CNHLSX10_P4	C8T28SOI_LLP1_-CNHLSX10_P10	C8T28SOI_LLP1_-CNHLSX10_P16
CP	0.0010	0.0010	0.0011	0.0012
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0006	0.0007
	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P10	C8T28SOI_LLP1_-CNHLSX14_P16
CP	0.0010	0.0010	0.0011	0.0012
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0006	0.0007
	C8T28SOI_LLP1_-CNHLSX19_P0	C8T28SOI_LLP1_-CNHLSX19_P4	C8T28SOI_LLP1_-CNHLSX19_P10	C8T28SOI_LLP1_-CNHLSX19_P16
CP	0.0015	0.0016	0.0017	0.0018
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP1_-CNHLSX24_P0	C8T28SOI_LLP1_-CNHLSX24_P4	C8T28SOI_LLP1_-CNHLSX24_P10	C8T28SOI_LLP1_-CNHLSX24_P16
CP	0.0015	0.0016	0.0017	0.0018
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0006	0.0007
	C8T28SOI_LLP1_-CNHLSX29_P0	C8T28SOI_LLP1_-CNHLSX29_P4	C8T28SOI_LLP1_-CNHLSX29_P10	C8T28SOI_LLP1_-CNHLSX29_P16
CP	0.0016	0.0017	0.0018	0.0018
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0006	0.0007
	C8T28SOI_LLP1_-CNHLSX34_P0	C8T28SOI_LLP1_-CNHLSX34_P4	C8T28SOI_LLP1_-CNHLSX34_P10	C8T28SOI_LLP1_-CNHLSX34_P16
CP	0.0016	0.0017	0.0018	0.0018
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0006	0.0007
	C8T28SOI_LLP1_-CNHLSX38_P0	C8T28SOI_LLP1_-CNHLSX38_P4	C8T28SOI_LLP1_-CNHLSX38_P10	C8T28SOI_LLP1_-CNHLSX38_P16
CP	0.0016	0.0016	0.0018	0.0018
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0006	0.0007
	C8T28SOI_LLP1_-CNHLSX57_P0	C8T28SOI_LLP1_-CNHLSX57_P4	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP	0.0025	0.0027	0.0028	0.0029
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP	0.0014	0.0014	0.0015	0.0016
E	0.0003	0.0003	0.0003	0.0004

TE	0.0005	0.0006	0.0006	0.0006
	C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP	0.0018	0.0019	0.0019	0.0020
E	0.0003	0.0003	0.0003	0.0004
TE	0.0006	0.0006	0.0006	0.0006
	C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP	0.0019	0.0019	0.0020	0.0021
E	0.0003	0.0003	0.0003	0.0004
TE	0.0006	0.0006	0.0006	0.0006
	C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP	0.0019	0.0019	0.0020	0.0020
E	0.0003	0.0003	0.0003	0.0004
TE	0.0006	0.0006	0.0006	0.0006
	C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP	0.0019	0.0019	0.0020	0.0020
E	0.0003	0.0003	0.0003	0.0004
TE	0.0006	0.0006	0.0006	0.0006
	C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP	0.0025	0.0026	0.0028	0.0029
E	0.0003	0.0003	0.0003	0.0004
TE	0.0006	0.0006	0.0006	0.0006
	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP	0.0026	0.0026	0.0028	0.0029
E	0.0003	0.0003	0.0003	0.0004
TE	0.0006	0.0006	0.0006	0.0006
	C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP	0.0025	0.0026	0.0027	0.0028
E	0.0003	0.0003	0.0003	0.0004
TE	0.0006	0.0006	0.0006	0.0006
	C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP	0.0047	0.0049	0.0051	0.0053
E	0.0003	0.0003	0.0003	0.0004
TE	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LLP1_-CNHLSX10_P0	**C8T28SOI_LLP1_-CNHLSX10_P4**	**C8T28SOI_LLP1_-CNHLSX10_P0**	**C8T28SOI_LLP1_-CNHLSX10_P4**
CP to Q ↓	0.0316	0.0358	1.8602	2.0131
CP to Q ↑	0.0292	0.0329	2.6100	2.9344
	C8T28SOI_LLP1_-CNHLSX10_P10	**C8T28SOI_LLP1_-CNHLSX10_P16**	**C8T28SOI_LLP1_-CNHLSX10_P10**	**C8T28SOI_LLP1_-CNHLSX10_P16**
CP to Q ↓	0.0423	0.0484	2.2348	2.4341
CP to Q ↑	0.0384	0.0433	3.4332	3.9001

	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4
CP to Q ↓	0.0339	0.0386	1.2603	1.3661
CP to Q ↑	0.0315	0.0355	1.7556	1.9728
	C8T28SOI_LLP1_-CNHLSX14_P10	**C8T28SOI_LLP1_-CNHLSX14_P16**	**C8T28SOI_LLP1_-CNHLSX14_P10**	**C8T28SOI_LLP1_-CNHLSX14_P16**
CP to Q ↓	0.0458	0.0527	1.5191	1.6580
CP to Q ↑	0.0414	0.0467	2.3111	2.6271
	C8T28SOI_LLP1_-CNHLSX19_P0	**C8T28SOI_LLP1_-CNHLSX19_P4**	**C8T28SOI_LLP1_-CNHLSX19_P0**	**C8T28SOI_LLP1_-CNHLSX19_P4**
CP to Q ↓	0.0270	0.0307	0.9271	1.0033
CP to Q ↑	0.0250	0.0282	1.3064	1.4681
	C8T28SOI_LLP1_-CNHLSX19_P10	**C8T28SOI_LLP1_-CNHLSX19_P16**	**C8T28SOI_LLP1_-CNHLSX19_P10**	**C8T28SOI_LLP1_-CNHLSX19_P16**
CP to Q ↓	0.0362	0.0415	1.1107	1.2094
CP to Q ↑	0.0329	0.0372	1.7162	1.9517
	C8T28SOI_LLP1_-CNHLSX24_P0	**C8T28SOI_LLP1_-CNHLSX24_P4**	**C8T28SOI_LLP1_-CNHLSX24_P0**	**C8T28SOI_LLP1_-CNHLSX24_P4**
CP to Q ↓	0.0293	0.0333	0.7559	0.8176
CP to Q ↑	0.0272	0.0306	1.0528	1.1838
	C8T28SOI_LLP1_-CNHLSX24_P10	**C8T28SOI_LLP1_-CNHLSX24_P16**	**C8T28SOI_LLP1_-CNHLSX24_P10**	**C8T28SOI_LLP1_-CNHLSX24_P16**
CP to Q ↓	0.0395	0.0452	0.9071	0.9872
CP to Q ↑	0.0358	0.0404	1.3820	1.5703
	C8T28SOI_LLP1_-CNHLSX29_P0	**C8T28SOI_LLP1_-CNHLSX29_P4**	**C8T28SOI_LLP1_-CNHLSX29_P0**	**C8T28SOI_LLP1_-CNHLSX29_P4**
CP to Q ↓	0.0284	0.0323	0.6318	0.6847
CP to Q ↑	0.0273	0.0306	0.8802	0.9886
	C8T28SOI_LLP1_-CNHLSX29_P10	**C8T28SOI_LLP1_-CNHLSX29_P16**	**C8T28SOI_LLP1_-CNHLSX29_P10**	**C8T28SOI_LLP1_-CNHLSX29_P16**
CP to Q ↓	0.0383	0.0439	0.7605	0.8284
CP to Q ↑	0.0356	0.0403	1.1555	1.3123
	C8T28SOI_LLP1_-CNHLSX34_P0	**C8T28SOI_LLP1_-CNHLSX34_P4**	**C8T28SOI_LLP1_-CNHLSX34_P0**	**C8T28SOI_LLP1_-CNHLSX34_P4**
CP to Q ↓	0.0301	0.0343	0.5482	0.5935
CP to Q ↑	0.0290	0.0326	0.7585	0.8512
	C8T28SOI_LLP1_-CNHLSX34_P10	**C8T28SOI_LLP1_-CNHLSX34_P16**	**C8T28SOI_LLP1_-CNHLSX34_P10**	**C8T28SOI_LLP1_-CNHLSX34_P16**
CP to Q ↓	0.0409	0.0468	0.6595	0.7185
CP to Q ↑	0.0382	0.0429	0.9945	1.1295
	C8T28SOI_LLP1_-CNHLSX38_P0	**C8T28SOI_LLP1_-CNHLSX38_P4**	**C8T28SOI_LLP1_-CNHLSX38_P0**	**C8T28SOI_LLP1_-CNHLSX38_P4**
CP to Q ↓	0.0314	0.0359	0.4799	0.5199
CP to Q ↑	0.0304	0.0341	0.6645	0.7462
	C8T28SOI_LLP1_-CNHLSX38_P10	**C8T28SOI_LLP1_-CNHLSX38_P16**	**C8T28SOI_LLP1_-CNHLSX38_P10**	**C8T28SOI_LLP1_-CNHLSX38_P16**
CP to Q ↓	0.0429	0.0491	0.5787	0.6311
CP to Q ↑	0.0400	0.0449	0.8724	0.9915
	C8T28SOI_LLP1_-CNHLSX57_P0	**C8T28SOI_LLP1_-CNHLSX57_P4**	**C8T28SOI_LLP1_-CNHLSX57_P0**	**C8T28SOI_LLP1_-CNHLSX57_P4**
CP to Q ↓	0.0296	0.0337	0.3215	0.3480
CP to Q ↑	0.0281	0.0316	0.4564	0.5110

	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP to Q ↓	0.0401	0.0458	0.3861	0.4206
CP to Q ↑	0.0371	0.0418	0.5961	0.6759
	C8T28SOI_LLP_-CNHLSX4_P0	**C8T28SOI_LLP_-CNHLSX4_P4**	**C8T28SOI_LLP_-CNHLSX4_P0**	**C8T28SOI_LLP_-CNHLSX4_P4**
CP to Q ↓	0.0335	0.0385	4.6314	5.0153
CP to Q ↑	0.0242	0.0276	5.4675	6.1422
	C8T28SOI_LLP_-CNHLSX4_P10	**C8T28SOI_LLP_-CNHLSX4_P16**	**C8T28SOI_LLP_-CNHLSX4_P10**	**C8T28SOI_LLP_-CNHLSX4_P16**
CP to Q ↓	0.0460	0.0531	5.5532	6.0485
CP to Q ↑	0.0326	0.0371	7.1660	8.1373
	C8T28SOI_LLP_-CNHLSX9_P0	**C8T28SOI_LLP_-CNHLSX9_P4**	**C8T28SOI_LLP_-CNHLSX9_P0**	**C8T28SOI_LLP_-CNHLSX9_P4**
CP to Q ↓	0.0287	0.0327	2.1167	2.2901
CP to Q ↑	0.0210	0.0240	2.6977	3.0345
	C8T28SOI_LLP_-CNHLSX9_P10	**C8T28SOI_LLP_-CNHLSX9_P16**	**C8T28SOI_LLP_-CNHLSX9_P10**	**C8T28SOI_LLP_-CNHLSX9_P16**
CP to Q ↓	0.0389	0.0449	2.5384	2.7629
CP to Q ↑	0.0284	0.0323	3.5487	4.0352
	C8T28SOI_LLP_-CNHLSX13_P0	**C8T28SOI_LLP_-CNHLSX13_P4**	**C8T28SOI_LLP_-CNHLSX13_P0**	**C8T28SOI_LLP_-CNHLSX13_P4**
CP to Q ↓	0.0338	0.0388	1.4309	1.5516
CP to Q ↑	0.0250	0.0286	1.8122	2.0404
	C8T28SOI_LLP_-CNHLSX13_P10	**C8T28SOI_LLP_-CNHLSX13_P16**	**C8T28SOI_LLP_-CNHLSX13_P10**	**C8T28SOI_LLP_-CNHLSX13_P16**
CP to Q ↓	0.0464	0.0539	1.7236	1.8781
CP to Q ↑	0.0338	0.0386	2.3843	2.7116
	C8T28SOI_LLP_-CNHLSX17_P0	**C8T28SOI_LLP_-CNHLSX17_P4**	**C8T28SOI_LLP_-CNHLSX17_P0**	**C8T28SOI_LLP_-CNHLSX17_P4**
CP to Q ↓	0.0384	0.0439	1.1055	1.1996
CP to Q ↑	0.0282	0.0321	1.3608	1.5319
	C8T28SOI_LLP_-CNHLSX17_P10	**C8T28SOI_LLP_-CNHLSX17_P16**	**C8T28SOI_LLP_-CNHLSX17_P10**	**C8T28SOI_LLP_-CNHLSX17_P16**
CP to Q ↓	0.0534	0.0614	1.3340	1.4548
CP to Q ↑	0.0383	0.0431	1.7960	2.0419
	C8T28SOI_LLP_-CNHLSX21_P0	**C8T28SOI_LLP_-CNHLSX21_P4**	**C8T28SOI_LLP_-CNHLSX21_P0**	**C8T28SOI_LLP_-CNHLSX21_P4**
CP to Q ↓	0.0434	0.0497	0.8977	0.9757
CP to Q ↑	0.0322	0.0363	1.1064	1.2442
	C8T28SOI_LLP_-CNHLSX21_P10	**C8T28SOI_LLP_-CNHLSX21_P16**	**C8T28SOI_LLP_-CNHLSX21_P10**	**C8T28SOI_LLP_-CNHLSX21_P16**
CP to Q ↓	0.0598	0.0697	1.0879	1.1888
CP to Q ↑	0.0426	0.0485	1.4563	1.6559
	C8T28SOI_LLP_-CNHLSX27_P0	**C8T28SOI_LLP_-CNHLSX27_P4**	**C8T28SOI_LLP_-CNHLSX27_P0**	**C8T28SOI_LLP_-CNHLSX27_P4**
CP to Q ↓	0.0267	0.0304	0.7333	0.7939
CP to Q ↑	0.0217	0.0247	0.8256	0.9290
	C8T28SOI_LLP_-CNHLSX27_P10	**C8T28SOI_LLP_-CNHLSX27_P16**	**C8T28SOI_LLP_-CNHLSX27_P10**	**C8T28SOI_LLP_-CNHLSX27_P16**
CP to Q ↓	0.0361	0.0415	0.8785	0.9569
CP to Q ↑	0.0292	0.0332	1.0876	1.2351

	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4
CP to Q ↓	0.0284	0.0323	0.6461	0.7004
CP to Q ↑	0.0233	0.0264	0.7300	0.8210
	C8T28SOI_LLP_-CNHLSX30_P10	**C8T28SOI_LLP_-CNHLSX30_P16**	**C8T28SOI_LLP_-CNHLSX30_P10**	**C8T28SOI_LLP_-CNHLSX30_P16**
CP to Q ↓	0.0385	0.0442	0.7767	0.8454
CP to Q ↑	0.0313	0.0354	0.9604	1.0920
	C8T28SOI_LLP_-CNHLSX38_P0	**C8T28SOI_LLP_-CNHLSX38_P4**	**C8T28SOI_LLP_-CNHLSX38_P0**	**C8T28SOI_LLP_-CNHLSX38_P4**
CP to Q ↓	0.0316	0.0357	0.5190	0.5625
CP to Q ↑	0.0260	0.0291	0.5887	0.6621
	C8T28SOI_LLP_-CNHLSX38_P10	**C8T28SOI_LLP_-CNHLSX38_P16**	**C8T28SOI_LLP_-CNHLSX38_P10**	**C8T28SOI_LLP_-CNHLSX38_P16**
CP to Q ↓	0.0427	0.0490	0.6244	0.6801
CP to Q ↑	0.0343	0.0389	0.7739	0.8795
	C8T28SOI_LLP_-CNHLSX54_P0	**C8T28SOI_LLP_-CNHLSX54_P4**	**C8T28SOI_LLP_-CNHLSX54_P0**	**C8T28SOI_LLP_-CNHLSX54_P4**
CP to Q ↓	0.0240	0.0271	0.3624	0.3923
CP to Q ↑	0.0211	0.0237	0.4232	0.4751
	C8T28SOI_LLP_-CNHLSX54_P10	**C8T28SOI_LLP_-CNHLSX54_P16**	**C8T28SOI_LLP_-CNHLSX54_P10**	**C8T28SOI_LLP_-CNHLSX54_P16**
CP to Q ↓	0.0323	0.0369	0.4352	0.4729
CP to Q ↑	0.0281	0.0318	0.5536	0.6292

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_-LLP1_-CNHLSX10_P0	C8T28SOI_-LLP1_-CNHLSX10_P4	C8T28SOI_-LLP1_-CNHLSX10_P10	C8T28SOI_-LLP1_-CNHLSX10_P16
CP ↓	min_pulse_width to CP	0.0589	0.0646	0.0771	0.0897
E ↓	hold_rising to CP	-0.0023	-0.0018	-0.0067	-0.0143
E ↑	hold_rising to CP	-0.0102	-0.0177	-0.0274	-0.0345
E ↓	setup_rising to CP	0.0268	0.0289	0.0343	0.0392
E ↑	setup_rising to CP	0.0450	0.0521	0.0667	0.0791
TE ↓	hold_rising to CP	0.0004	-0.0017	-0.0071	-0.0116
TE ↑	hold_rising to CP	-0.0128	-0.0203	-0.0296	-0.0394
TE ↓	setup_rising to CP	0.0273	0.0295	0.0370	0.0419
TE ↑	setup_rising to CP	0.0476	0.0574	0.0693	0.0786
		C8T28SOI_-LLP1_-CNHLSX14_P0	C8T28SOI_-LLP1_-CNHLSX14_P4	C8T28SOI_-LLP1_-CNHLSX14_P10	C8T28SOI_-LLP1_-CNHLSX14_P16
CP ↓	min_pulse_width to CP	0.0602	0.0681	0.0771	0.0897
E ↓	hold_rising to CP	0.0026	-0.0023	-0.0045	-0.0094
E ↑	hold_rising to CP	-0.0102	-0.0177	-0.0274	-0.0345
E ↓	setup_rising to CP	0.0240	0.0268	0.0317	0.0397

E ↑	setup_rising to CP	0.0477	0.0548	0.0667	0.0787
TE ↓	hold_rising to CP	0.0032	-0.0023	-0.0072	-0.0126
TE ↑	hold_rising to CP	-0.0128	-0.0203	-0.0296	-0.0394
TE ↓	setup_rising to CP	0.0247	0.0273	0.0317	0.0366
TE ↑	setup_rising to CP	0.0472	0.0570	0.0693	0.0807
		C8T28SOI_-LLP1_-CNHLSX19_P0	C8T28SOI_-LLP1_-CNHLSX19_P4	C8T28SOI_-LLP1_-CNHLSX19_P10	C8T28SOI_-LLP1_-CNHLSX19_P16
CP ↓	min_pulse_width to CP	0.0680	0.0771	0.0896	0.1034
E ↓	hold_rising to CP	-0.0071	-0.0088	-0.0142	-0.0191
E ↑	hold_rising to CP	-0.0155	-0.0226	-0.0323	-0.0442
E ↓	setup_rising to CP	0.0317	0.0366	0.0414	0.0489
E ↑	setup_rising to CP	0.0499	0.0569	0.0716	0.0888
TE ↓	hold_rising to CP	-0.0045	-0.0094	-0.0169	-0.0218
TE ↑	hold_rising to CP	-0.0177	-0.0225	-0.0345	-0.0442
TE ↓	setup_rising to CP	0.0312	0.0371	0.0415	0.0484
TE ↑	setup_rising to CP	0.0525	0.0623	0.0737	0.0883
		C8T28SOI_-LLP1_-CNHLSX24_P0	C8T28SOI_-LLP1_-CNHLSX24_P4	C8T28SOI_-LLP1_-CNHLSX24_P10	C8T28SOI_-LLP1_-CNHLSX24_P16
CP ↓	min_pulse_width to CP	0.0680	0.0771	0.0909	0.1064
E ↓	hold_rising to CP	-0.0039	-0.0067	-0.0143	-0.0191
E ↑	hold_rising to CP	-0.0155	-0.0226	-0.0323	-0.0442
E ↓	setup_rising to CP	0.0317	0.0338	0.0382	0.0489
E ↑	setup_rising to CP	0.0499	0.0596	0.0742	0.0888
TE ↓	hold_rising to CP	-0.0045	-0.0066	-0.0111	-0.0191
TE ↑	hold_rising to CP	-0.0177	-0.0225	-0.0345	-0.0442
TE ↓	setup_rising to CP	0.0322	0.0371	0.0415	0.0463
TE ↑	setup_rising to CP	0.0525	0.0618	0.0764	0.0910
		C8T28SOI_-LLP1_-CNHLSX29_P0	C8T28SOI_-LLP1_-CNHLSX29_P4	C8T28SOI_-LLP1_-CNHLSX29_P10	C8T28SOI_-LLP1_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0771	0.0862	0.1034	0.1219
E ↓	hold_rising to CP	-0.0071	-0.0088	-0.0137	-0.0182
E ↑	hold_rising to CP	-0.0200	-0.0307	-0.0420	-0.0540
E ↓	setup_rising to CP	0.0317	0.0366	0.0440	0.0489
E ↑	setup_rising to CP	0.0564	0.0667	0.0862	0.1035

TE ↓	hold_rising to CP	-0.0071	-0.0094	-0.0169	-0.0214
TE ↑	hold_rising to CP	-0.0225	-0.0323	-0.0442	-0.0594
TE ↓	setup_rising to CP	0.0312	0.0366	0.0409	0.0517
TE ↑	setup_rising to CP	0.0596	0.0720	0.0888	0.1030
		C8T28SOI_-LLP1_-CNHLSX34_P0	C8T28SOI_-LLP1_-CNHLSX34_P4	C8T28SOI_-LLP1_-CNHLSX34_P10	C8T28SOI_-LLP1_-CNHLSX34_P16
CP ↓	min_pulse_width to CP	0.0771	0.0897	0.1047	0.1219
E ↓	hold_rising to CP	-0.0072	-0.0094	-0.0143	-0.0191
E ↑	hold_rising to CP	-0.0200	-0.0307	-0.0420	-0.0540
E ↓	setup_rising to CP	0.0317	0.0366	0.0441	0.0489
E ↑	setup_rising to CP	0.0596	0.0694	0.0862	0.1035
TE ↓	hold_rising to CP	-0.0045	-0.0094	-0.0169	-0.0218
TE ↑	hold_rising to CP	-0.0225	-0.0323	-0.0442	-0.0594
TE ↓	setup_rising to CP	0.0316	0.0371	0.0415	0.0517
TE ↑	setup_rising to CP	0.0623	0.0716	0.0888	0.1051
		C8T28SOI_-LLP1_-CNHLSX38_P0	C8T28SOI_-LLP1_-CNHLSX38_P4	C8T28SOI_-LLP1_-CNHLSX38_P10	C8T28SOI_-LLP1_-CNHLSX38_P16
CP ↓	min_pulse_width to CP	0.0771	0.0897	0.1082	0.1219
E ↓	hold_rising to CP	-0.0039	-0.0067	-0.0143	-0.0192
E ↑	hold_rising to CP	-0.0200	-0.0307	-0.0420	-0.0540
E ↓	setup_rising to CP	0.0321	0.0370	0.0414	0.0489
E ↑	setup_rising to CP	0.0596	0.0720	0.0862	0.1030
TE ↓	hold_rising to CP	-0.0050	-0.0066	-0.0116	-0.0224
TE ↑	hold_rising to CP	-0.0225	-0.0323	-0.0442	-0.0594
TE ↓	setup_rising to CP	0.0322	0.0371	0.0419	0.0490
TE ↑	setup_rising to CP	0.0623	0.0716	0.0884	0.1083
		C8T28SOI_-LLP1_-CNHLSX57_P0	C8T28SOI_-LLP1_-CNHLSX57_P4	C8T28SOI_-LLP1_-CNHLSX57_P10	C8T28SOI_-LLP1_-CNHLSX57_P16
CP ↓	min_pulse_width to CP	0.0864	0.0990	0.1173	0.1358
E ↓	hold_rising to CP	-0.0067	-0.0120	-0.0165	-0.0240
E ↑	hold_rising to CP	-0.0226	-0.0323	-0.0469	-0.0589
E ↓	setup_rising to CP	0.0370	0.0387	0.0431	0.0538
E ↑	setup_rising to CP	0.0645	0.0765	0.0960	0.1181
TE ↓	hold_rising to CP	-0.0066	-0.0120	-0.0169	-0.0214
TE ↑	hold_rising to CP	-0.0252	-0.0323	-0.0491	-0.0643

TE ↓	setup_rising to CP	0.0344	0.0393	0.0468	0.0539
TE ↑	setup_rising to CP	0.0671	0.0791	0.0986	0.1176
		C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP ↓	min_pulse_width to CP	0.0376	0.0438	0.0531	0.0576
E ↓	hold_rising to CP	-0.0176	-0.0230	-0.0295	-0.0372
E ↑	hold_rising to CP	-0.0013	-0.0039	-0.0088	-0.0142
E ↓	setup_rising to CP	0.0419	0.0468	0.0571	0.0669
E ↑	setup_rising to CP	0.0310	0.0358	0.0465	0.0535
TE ↓	hold_rising to CP	-0.0149	-0.0198	-0.0301	-0.0371
TE ↑	hold_rising to CP	-0.0013	-0.0061	-0.0083	-0.0132
TE ↓	setup_rising to CP	0.0457	0.0505	0.0571	0.0668
TE ↑	setup_rising to CP	0.0341	0.0416	0.0491	0.0562
		C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP ↓	min_pulse_width to CP	0.0337	0.0406	0.0468	0.0554
E ↓	hold_rising to CP	-0.0123	-0.0171	-0.0279	-0.0350
E ↑	hold_rising to CP	0.0009	-0.0013	-0.0067	-0.0083
E ↓	setup_rising to CP	0.0429	0.0478	0.0544	0.0646
E ↑	setup_rising to CP	0.0293	0.0342	0.0416	0.0487
TE ↓	hold_rising to CP	-0.0159	-0.0208	-0.0273	-0.0350
TE ↑	hold_rising to CP	-0.0017	-0.0013	-0.0061	-0.0083
TE ↓	setup_rising to CP	0.0398	0.0447	0.0550	0.0615
TE ↑	setup_rising to CP	0.0314	0.0368	0.0438	0.0481
		C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP ↓	min_pulse_width to CP	0.0360	0.0399	0.0491	0.0578
E ↓	hold_rising to CP	-0.0123	-0.0171	-0.0279	-0.0350
E ↑	hold_rising to CP	0.0009	-0.0013	-0.0067	-0.0083
E ↓	setup_rising to CP	0.0429	0.0478	0.0544	0.0646
E ↑	setup_rising to CP	0.0293	0.0368	0.0416	0.0481
TE ↓	hold_rising to CP	-0.0159	-0.0208	-0.0273	-0.0350
TE ↑	hold_rising to CP	-0.0017	-0.0013	-0.0061	-0.0083
TE ↓	setup_rising to CP	0.0398	0.0447	0.0550	0.0648
TE ↑	setup_rising to CP	0.0314	0.0368	0.0433	0.0539

		C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP ↓	min_pulse_width to CP	0.0367	0.0423	0.0509	0.0602
E ↓	hold_rising to CP	-0.0123	-0.0171	-0.0279	-0.0350
E ↑	hold_rising to CP	0.0009	-0.0013	-0.0035	-0.0083
E ↓	setup_rising to CP	0.0429	0.0478	0.0544	0.0646
E ↑	setup_rising to CP	0.0293	0.0368	0.0416	0.0481
TE ↓	hold_rising to CP	-0.0159	-0.0208	-0.0273	-0.0350
TE ↑	hold_rising to CP	-0.0017	-0.0013	-0.0061	-0.0083
TE ↓	setup_rising to CP	0.0398	0.0447	0.0550	0.0648
TE ↑	setup_rising to CP	0.0314	0.0368	0.0433	0.0540
		C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP ↓	min_pulse_width to CP	0.0384	0.0423	0.0533	0.0619
E ↓	hold_rising to CP	-0.0123	-0.0171	-0.0279	-0.0350
E ↑	hold_rising to CP	0.0009	-0.0013	-0.0035	-0.0083
E ↓	setup_rising to CP	0.0429	0.0478	0.0544	0.0646
E ↑	setup_rising to CP	0.0293	0.0368	0.0416	0.0481
TE ↓	hold_rising to CP	-0.0159	-0.0208	-0.0273	-0.0350
TE ↑	hold_rising to CP	-0.0017	-0.0013	-0.0061	-0.0083
TE ↓	setup_rising to CP	0.0398	0.0447	0.0550	0.0648
TE ↑	setup_rising to CP	0.0314	0.0368	0.0433	0.0540
		C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP ↓	min_pulse_width to CP	0.0392	0.0455	0.0540	0.0610
E ↓	hold_rising to CP	-0.0171	-0.0220	-0.0323	-0.0421
E ↑	hold_rising to CP	-0.0013	-0.0039	-0.0088	-0.0142
E ↓	setup_rising to CP	0.0473	0.0517	0.0620	0.0718
E ↑	setup_rising to CP	0.0368	0.0417	0.0514	0.0579
TE ↓	hold_rising to CP	-0.0208	-0.0252	-0.0318	-0.0420
TE ↑	hold_rising to CP	-0.0013	-0.0061	-0.0083	-0.0132
TE ↓	setup_rising to CP	0.0447	0.0522	0.0620	0.0717
TE ↑	setup_rising to CP	0.0363	0.0407	0.0540	0.0637
		C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP ↓	min_pulse_width to CP	0.0385	0.0437	0.0516	0.0609
E ↓	hold_rising to CP	-0.0171	-0.0220	-0.0323	-0.0421

E ↑	hold_rising to CP	-0.0013	-0.0071	-0.0088	-0.0137
E ↓	setup_rising to CP	0.0478	0.0517	0.0620	0.0718
E ↑	setup_rising to CP	0.0368	0.0417	0.0514	0.0584
TE ↓	hold_rising to CP	-0.0208	-0.0252	-0.0322	-0.0420
TE ↑	hold_rising to CP	-0.0013	-0.0061	-0.0083	-0.0132
TE ↓	setup_rising to CP	0.0447	0.0522	0.0620	0.0717
TE ↑	setup_rising to CP	0.0363	0.0411	0.0540	0.0637
		C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP ↓	min_pulse_width to CP	0.0384	0.0454	0.0515	0.0607
E ↓	hold_rising to CP	-0.0171	-0.0220	-0.0323	-0.0389
E ↑	hold_rising to CP	-0.0013	-0.0071	-0.0088	-0.0137
E ↓	setup_rising to CP	0.0473	0.0517	0.0620	0.0718
E ↑	setup_rising to CP	0.0368	0.0417	0.0514	0.0579
TE ↓	hold_rising to CP	-0.0208	-0.0257	-0.0322	-0.0425
TE ↑	hold_rising to CP	-0.0013	-0.0061	-0.0083	-0.0132
TE ↓	setup_rising to CP	0.0447	0.0554	0.0620	0.0717
TE ↑	setup_rising to CP	0.0363	0.0407	0.0540	0.0637
		C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP ↓	min_pulse_width to CP	0.0410	0.0456	0.0550	0.0643
E ↓	hold_rising to CP	-0.0204	-0.0279	-0.0376	-0.0447
E ↑	hold_rising to CP	0.0009	-0.0013	-0.0061	-0.0083
E ↓	setup_rising to CP	0.0473	0.0517	0.0641	0.0744
E ↑	setup_rising to CP	0.0369	0.0417	0.0514	0.0638
TE ↓	hold_rising to CP	-0.0202	-0.0247	-0.0376	-0.0474
TE ↑	hold_rising to CP	-0.0013	-0.0039	-0.0083	-0.0137
TE ↓	setup_rising to CP	0.0479	0.0554	0.0647	0.0771
TE ↑	setup_rising to CP	0.0363	0.0407	0.0536	0.0633

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LLP1_CNHLSX10_P0	1.518e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX10_P4	5.462e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX10_P10	1.765e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX10_P16	8.228e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX14_P0	1.797e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX14_P4	6.435e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX14_P10	2.068e-05	1.000e-20

C8T28SOI_LLP1_CNHLSX14_P16	9.593e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P0	2.340e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P4	8.375e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P10	2.686e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P16	1.244e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P0	2.609e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P4	9.316e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P10	2.980e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P16	1.376e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P0	3.097e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P4	1.100e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P10	3.492e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P16	1.603e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P0	3.366e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P4	1.194e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P10	3.786e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P16	1.736e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P0	3.635e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P4	1.288e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P10	4.080e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P16	1.869e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P0	5.034e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P4	1.788e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P10	5.676e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P16	2.604e-05	1.000e-20
C8T28SOI_LLP_CNHLSX4_P0	1.222e-04	1.000e-20
C8T28SOI_LLP_CNHLSX4_P4	4.402e-05	1.000e-20
C8T28SOI_LLP_CNHLSX4_P10	1.431e-05	1.000e-20
C8T28SOI_LLP_CNHLSX4_P16	6.708e-06	1.000e-20
C8T28SOI_LLP_CNHLSX9_P0	1.661e-04	1.000e-20
C8T28SOI_LLP_CNHLSX9_P4	5.914e-05	1.000e-20
C8T28SOI_LLP_CNHLSX9_P10	1.895e-05	1.000e-20
C8T28SOI_LLP_CNHLSX9_P16	8.791e-06	1.000e-20
C8T28SOI_LLP_CNHLSX13_P0	1.908e-04	1.000e-20
C8T28SOI_LLP_CNHLSX13_P4	6.777e-05	1.000e-20
C8T28SOI_LLP_CNHLSX13_P10	2.163e-05	1.000e-20
C8T28SOI_LLP_CNHLSX13_P16	9.998e-06	1.000e-20
C8T28SOI_LLP_CNHLSX17_P0	2.174e-04	1.000e-20
C8T28SOI_LLP_CNHLSX17_P4	7.677e-05	1.000e-20
C8T28SOI_LLP_CNHLSX17_P10	2.436e-05	1.000e-20
C8T28SOI_LLP_CNHLSX17_P16	1.122e-05	1.000e-20
C8T28SOI_LLP_CNHLSX21_P0	2.382e-04	1.000e-20
C8T28SOI_LLP_CNHLSX21_P4	8.453e-05	1.000e-20
C8T28SOI_LLP_CNHLSX21_P10	2.689e-05	1.000e-20
C8T28SOI_LLP_CNHLSX21_P16	1.239e-05	1.000e-20
C8T28SOI_LLP_CNHLSX27_P0	3.279e-04	1.000e-20
C8T28SOI_LLP_CNHLSX27_P4	1.149e-04	1.000e-20
C8T28SOI_LLP_CNHLSX27_P10	3.615e-05	1.000e-20
C8T28SOI_LLP_CNHLSX27_P16	1.655e-05	1.000e-20
C8T28SOI_LLP_CNHLSX30_P0	3.571e-04	1.000e-20
C8T28SOI_LLP_CNHLSX30_P4	1.251e-04	1.000e-20
C8T28SOI_LLP_CNHLSX30_P10	3.934e-05	1.000e-20

C8T28SOI_LLP_CNHLSX30_P16	1.800e-05	1.000e-20
C8T28SOI_LLP_CNHLSX38_P0	4.066e-04	1.000e-20
C8T28SOI_LLP_CNHLSX38_P4	1.419e-04	1.000e-20
C8T28SOI_LLP_CNHLSX38_P10	4.443e-05	1.000e-20
C8T28SOI_LLP_CNHLSX38_P16	2.027e-05	1.000e-20
C8T28SOI_LLP_CNHLSX54_P0	6.029e-04	1.000e-20
C8T28SOI_LLP_CNHLSX54_P4	2.103e-04	1.000e-20
C8T28SOI_LLP_CNHLSX54_P10	6.569e-05	1.000e-20
C8T28SOI_LLP_CNHLSX54_P16	2.990e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LLP1_-CNHLSX10_P0	C8T28SOI_LLP1_-CNHLSX10_P4	C8T28SOI_LLP1_-CNHLSX10_P10	C8T28SOI_LLP1_-CNHLSX10_P16
CP (output stable)	1.043e-03	1.050e-03	1.082e-03	1.119e-03
E (output stable)	7.535e-04	7.395e-04	7.483e-04	7.654e-04
TE (output stable)	7.904e-04	7.870e-04	8.105e-04	8.401e-04
CP to Q	2.855e-03	2.774e-03	2.775e-03	2.832e-03
	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P10	C8T28SOI_LLP1_-CNHLSX14_P16
CP (output stable)	1.044e-03	1.051e-03	1.086e-03	1.122e-03
E (output stable)	7.537e-04	7.393e-04	7.481e-04	7.652e-04
TE (output stable)	7.905e-04	7.867e-04	8.102e-04	8.398e-04
CP to Q	3.607e-03	3.458e-03	3.419e-03	3.466e-03
	C8T28SOI_LLP1_-CNHLSX19_P0	C8T28SOI_LLP1_-CNHLSX19_P4	C8T28SOI_LLP1_-CNHLSX19_P10	C8T28SOI_LLP1_-CNHLSX19_P16
CP (output stable)	1.470e-03	1.495e-03	1.556e-03	1.622e-03
E (output stable)	8.195e-04	8.075e-04	8.203e-04	8.417e-04
TE (output stable)	8.564e-04	8.550e-04	8.826e-04	9.165e-04
CP to Q	4.479e-03	4.309e-03	4.286e-03	4.353e-03
	C8T28SOI_LLP1_-CNHLSX24_P0	C8T28SOI_LLP1_-CNHLSX24_P4	C8T28SOI_LLP1_-CNHLSX24_P10	C8T28SOI_LLP1_-CNHLSX24_P16
CP (output stable)	1.482e-03	1.508e-03	1.569e-03	1.636e-03
E (output stable)	8.204e-04	8.084e-04	8.213e-04	8.426e-04
TE (output stable)	8.574e-04	8.558e-04	8.835e-04	9.173e-04
CP to Q	5.391e-03	5.170e-03	5.127e-03	5.201e-03
	C8T28SOI_LLP1_-CNHLSX29_P0	C8T28SOI_LLP1_-CNHLSX29_P4	C8T28SOI_LLP1_-CNHLSX29_P10	C8T28SOI_LLP1_-CNHLSX29_P16
CP (output stable)	1.616e-03	1.644e-03	1.718e-03	1.797e-03
E (output stable)	8.727e-04	8.626e-04	8.808e-04	9.071e-04
TE (output stable)	9.091e-04	9.095e-04	9.423e-04	9.809e-04
CP to Q	6.160e-03	5.893e-03	5.837e-03	5.921e-03
	C8T28SOI_LLP1_-CNHLSX34_P0	C8T28SOI_LLP1_-CNHLSX34_P4	C8T28SOI_LLP1_-CNHLSX34_P10	C8T28SOI_LLP1_-CNHLSX34_P16
CP (output stable)	1.618e-03	1.647e-03	1.700e-03	1.797e-03
E (output stable)	8.729e-04	8.632e-04	8.810e-04	9.074e-04
TE (output stable)	9.089e-04	9.102e-04	9.425e-04	9.813e-04
CP to Q	7.042e-03	6.723e-03	6.706e-03	6.727e-03
	C8T28SOI_LLP1_-CNHLSX38_P0	C8T28SOI_LLP1_-CNHLSX38_P4	C8T28SOI_LLP1_-CNHLSX38_P10	C8T28SOI_LLP1_-CNHLSX38_P16
CP (output stable)	1.617e-03	1.647e-03	1.708e-03	1.799e-03
E (output stable)	8.730e-04	8.630e-04	8.811e-04	9.075e-04
TE (output stable)	9.095e-04	9.100e-04	9.428e-04	9.815e-04

CP to Q	7.887e-03	7.493e-03	7.434e-03	7.426e-03
	C8T28SOI_LLP1_-CNHLSX57_P0	C8T28SOI_LLP1_-CNHLSX57_P4	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP (output stable)	2.084e-03	2.135e-03	2.223e-03	2.357e-03
E (output stable)	9.297e-04	9.217e-04	9.427e-04	9.713e-04
TE (output stable)	9.667e-04	9.691e-04	1.005e-03	1.046e-03
CP to Q	1.147e-02	1.091e-02	1.079e-02	1.084e-02
	C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP (output stable)	1.391e-03	1.385e-03	1.412e-03	1.456e-03
E (output stable)	7.840e-04	7.606e-04	7.535e-04	7.583e-04
TE (output stable)	8.245e-04	8.095e-04	8.143e-04	8.299e-04
CP to Q	1.948e-03	1.881e-03	1.870e-03	1.897e-03
	C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP (output stable)	1.449e-03	1.446e-03	1.484e-03	1.532e-03
E (output stable)	7.522e-04	7.321e-04	7.272e-04	7.337e-04
TE (output stable)	7.937e-04	7.823e-04	7.896e-04	8.072e-04
CP to Q	2.618e-03	2.511e-03	2.486e-03	2.522e-03
	C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP (output stable)	1.484e-03	1.482e-03	1.518e-03	1.569e-03
E (output stable)	7.572e-04	7.372e-04	7.335e-04	7.406e-04
TE (output stable)	7.989e-04	7.875e-04	7.958e-04	8.140e-04
CP to Q	3.501e-03	3.344e-03	3.299e-03	3.345e-03
	C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP (output stable)	1.486e-03	1.483e-03	1.517e-03	1.571e-03
E (output stable)	7.579e-04	7.374e-04	7.336e-04	7.408e-04
TE (output stable)	7.994e-04	7.877e-04	7.961e-04	8.142e-04
CP to Q	4.386e-03	4.143e-03	4.088e-03	4.061e-03
	C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP (output stable)	1.483e-03	1.479e-03	1.518e-03	1.569e-03
E (output stable)	7.573e-04	7.378e-04	7.338e-04	7.409e-04
TE (output stable)	7.990e-04	7.881e-04	7.963e-04	8.142e-04
CP to Q	5.490e-03	5.132e-03	4.966e-03	4.956e-03
	C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP (output stable)	2.012e-03	2.034e-03	2.103e-03	2.209e-03
E (output stable)	8.474e-04	8.293e-04	8.298e-04	8.407e-04
TE (output stable)	8.891e-04	8.797e-04	8.923e-04	9.143e-04
CP to Q	6.143e-03	5.851e-03	5.809e-03	5.869e-03
	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP (output stable)	2.007e-03	2.029e-03	2.105e-03	2.204e-03
E (output stable)	8.467e-04	8.283e-04	8.293e-04	8.402e-04
TE (output stable)	8.886e-04	8.787e-04	8.918e-04	9.139e-04
CP to Q	6.961e-03	6.615e-03	6.575e-03	6.610e-03
	C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP (output stable)	2.011e-03	2.032e-03	2.114e-03	2.206e-03
E (output stable)	8.458e-04	8.274e-04	8.284e-04	8.394e-04

TE (output stable)	8.878e-04	8.778e-04	8.909e-04	9.128e-04
CP to Q	8.618e-03	8.004e-03	7.911e-03	7.927e-03
	C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP (output stable)	3.003e-03	3.084e-03	3.219e-03	3.411e-03
E (output stable)	9.137e-04	9.019e-04	9.134e-04	9.337e-04
TE (output stable)	9.559e-04	9.525e-04	9.761e-04	1.007e-03
CP to Q	1.123e-02	1.058e-02	1.057e-02	1.061e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOI_LLP1_-CNHLSX10_P0	C8T28SOI_LLP1_-CNHLSX10_P4	C8T28SOI_LLP1_-CNHLSX10_P10	C8T28SOI_LLP1_-CNHLSX10_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P10	C8T28SOI_LLP1_-CNHLSX14_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX19_P0	C8T28SOI_LLP1_-CNHLSX19_P4	C8T28SOI_LLP1_-CNHLSX19_P10	C8T28SOI_LLP1_-CNHLSX19_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX24_P0	C8T28SOI_LLP1_-CNHLSX24_P4	C8T28SOI_LLP1_-CNHLSX24_P10	C8T28SOI_LLP1_-CNHLSX24_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX29_P0	C8T28SOI_LLP1_-CNHLSX29_P4	C8T28SOI_LLP1_-CNHLSX29_P10	C8T28SOI_LLP1_-CNHLSX29_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX34_P0	C8T28SOI_LLP1_-CNHLSX34_P4	C8T28SOI_LLP1_-CNHLSX34_P10	C8T28SOI_LLP1_-CNHLSX34_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX38_P0	C8T28SOI_LLP1_-CNHLSX38_P4	C8T28SOI_LLP1_-CNHLSX38_P10	C8T28SOI_LLP1_-CNHLSX38_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

	C8T28SOI_LLP1_-CNHLSX57_P0	C8T28SOI_LLP1_-CNHLSX57_P4	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

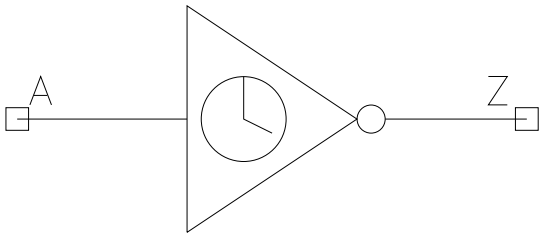
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNIV

Cell Description

Inverter with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_CNIVX2_P0	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX2_P4	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX2_-P10	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX2_-P16	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_P0	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_P4	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_-P10	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_-P16	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX9_P0	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX9_P4	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX9_-P10	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX9_-P16	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX14_-P0	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX14_-P4	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX14_-P10	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX14_-P16	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX18_-P0	0.800	0.680	0.5440
C8T28SOI_LL_CNIVX18_-P4	0.800	0.680	0.5440
C8T28SOI_LL_CNIVX18_-P10	0.800	0.680	0.5440
C8T28SOI_LL_CNIVX18_-P16	0.800	0.680	0.5440

C8T28SOI_LL_CNIVX22_P0	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX22_P4	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX22_P10	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX22_P16	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX27_P0	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX27_P4	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX27_P10	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX27_P16	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX32_P0	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX32_P4	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX32_P10	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX32_P16	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX37_P0	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX37_P4	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX37_P10	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX37_P16	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX74_P0	0.800	2.312	1.8496
C8T28SOI_LL_CNIVX74_P4	0.800	2.312	1.8496
C8T28SOI_LL_CNIVX74_P10	0.800	2.312	1.8496
C8T28SOI_LL_CNIVX74_P16	0.800	2.312	1.8496
C8T28SOIDV_LL_CNIVX18_P0	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX18_P4	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX18_P10	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX18_P16	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX28_P0	1.600	0.544	0.8704
C8T28SOIDV_LL_CNIVX28_P4	1.600	0.544	0.8704

C8T28SOIDV_LL_-CNIVX28_P10	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNIVX28_P16	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNIVX37_P0	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX37_P4	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX37_P10	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX37_P16	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX55_P0	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX55_P4	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX55_P10	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX55_P16	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX74_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNIVX74_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNIVX74_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNIVX74_P16	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_-CNIVX2_P0	C8T28SOI_LL_-CNIVX2_P4	C8T28SOI_LL_-CNIVX2_P10	C8T28SOI_LL_-CNIVX2_P16
A	0.0003	0.0003	0.0004	0.0004
	C8T28SOI_LL_-CNIVX4_P0	C8T28SOI_LL_-CNIVX4_P4	C8T28SOI_LL_-CNIVX4_P10	C8T28SOI_LL_-CNIVX4_P16
A	0.0005	0.0005	0.0005	0.0005
	C8T28SOI_LL_-CNIVX9_P0	C8T28SOI_LL_-CNIVX9_P4	C8T28SOI_LL_-CNIVX9_P10	C8T28SOI_LL_-CNIVX9_P16
A	0.0008	0.0009	0.0009	0.0010
	C8T28SOI_LL_-CNIVX14_P0	C8T28SOI_LL_-CNIVX14_P4	C8T28SOI_LL_-CNIVX14_P10	C8T28SOI_LL_-CNIVX14_P16
A	0.0013	0.0013	0.0014	0.0015
	C8T28SOI_LL_-CNIVX18_P0	C8T28SOI_LL_-CNIVX18_P4	C8T28SOI_LL_-CNIVX18_P10	C8T28SOI_LL_-CNIVX18_P16
A	0.0016	0.0017	0.0018	0.0019
	C8T28SOI_LL_-CNIVX22_P0	C8T28SOI_LL_-CNIVX22_P4	C8T28SOI_LL_-CNIVX22_P10	C8T28SOI_LL_-CNIVX22_P16
A	0.0021	0.0021	0.0023	0.0024

	C8T28SOI_LL_-CNIVX27_P0	C8T28SOI_LL_-CNIVX27_P4	C8T28SOI_LL_-CNIVX27_P10	C8T28SOI_LL_-CNIVX27_P16
A	0.0024	0.0025	0.0027	0.0029
	C8T28SOI_LL_-CNIVX32_P0	C8T28SOI_LL_-CNIVX32_P4	C8T28SOI_LL_-CNIVX32_P10	C8T28SOI_LL_-CNIVX32_P16
A	0.0029	0.0030	0.0032	0.0034
	C8T28SOI_LL_-CNIVX37_P0	C8T28SOI_LL_-CNIVX37_P4	C8T28SOI_LL_-CNIVX37_P10	C8T28SOI_LL_-CNIVX37_P16
A	0.0033	0.0034	0.0036	0.0038
	C8T28SOI_LL_-CNIVX74_P0	C8T28SOI_LL_-CNIVX74_P4	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A	0.0068	0.0070	0.0073	0.0079
	C8T28SOIDV_LL_-CNIVX18_P0	C8T28SOIDV_LL_-CNIVX18_P4	C8T28SOIDV_LL_-CNIVX18_P10	C8T28SOIDV_LL_-CNIVX18_P16
A	0.0016	0.0017	0.0018	0.0019
	C8T28SOIDV_LL_-CNIVX28_P0	C8T28SOIDV_LL_-CNIVX28_P4	C8T28SOIDV_LL_-CNIVX28_P10	C8T28SOIDV_LL_-CNIVX28_P16
A	0.0025	0.0025	0.0027	0.0029
	C8T28SOIDV_LL_-CNIVX37_P0	C8T28SOIDV_LL_-CNIVX37_P4	C8T28SOIDV_LL_-CNIVX37_P10	C8T28SOIDV_LL_-CNIVX37_P16
A	0.0032	0.0033	0.0035	0.0038
	C8T28SOIDV_LL_-CNIVX55_P0	C8T28SOIDV_LL_-CNIVX55_P4	C8T28SOIDV_LL_-CNIVX55_P10	C8T28SOIDV_LL_-CNIVX55_P16
A	0.0049	0.0050	0.0053	0.0058
	C8T28SOIDV_LL_-CNIVX74_P0	C8T28SOIDV_LL_-CNIVX74_P4	C8T28SOIDV_LL_-CNIVX74_P10	C8T28SOIDV_LL_-CNIVX74_P16
A	0.0067	0.0069	0.0073	0.0078

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-CNIVX2_P0	**C8T28SOI_LL_-CNIVX2_P4**	**C8T28SOI_LL_-CNIVX2_P0**	**C8T28SOI_LL_-CNIVX2_P4**
A to Z ↓	0.0073	0.0086	7.9972	8.5924
A to Z ↑	0.0122	0.0137	9.6278	10.8313
	C8T28SOI_LL_-CNIVX2_P10	**C8T28SOI_LL_-CNIVX2_P16**	**C8T28SOI_LL_-CNIVX2_P10**	**C8T28SOI_LL_-CNIVX2_P16**
A to Z ↓	0.0103	0.0117	9.4370	10.1751
A to Z ↑	0.0157	0.0175	12.7020	14.4655
	C8T28SOI_LL_-CNIVX4_P0	**C8T28SOI_LL_-CNIVX4_P4**	**C8T28SOI_LL_-CNIVX4_P0**	**C8T28SOI_LL_-CNIVX4_P4**
A to Z ↓	0.0055	0.0066	3.9787	4.2801
A to Z ↑	0.0104	0.0116	5.8874	6.6032
	C8T28SOI_LL_-CNIVX4_P10	**C8T28SOI_LL_-CNIVX4_P16**	**C8T28SOI_LL_-CNIVX4_P10**	**C8T28SOI_LL_-CNIVX4_P16**
A to Z ↓	0.0081	0.0093	4.7092	5.0833
A to Z ↑	0.0133	0.0148	7.7003	8.7313
	C8T28SOI_LL_-CNIVX9_P0	**C8T28SOI_LL_-CNIVX9_P4**	**C8T28SOI_LL_-CNIVX9_P0**	**C8T28SOI_LL_-CNIVX9_P4**
A to Z ↓	0.0043	0.0053	1.9169	2.0643
A to Z ↑	0.0086	0.0096	2.7012	3.0262
	C8T28SOI_LL_-CNIVX9_P10	**C8T28SOI_LL_-CNIVX9_P16**	**C8T28SOI_LL_-CNIVX9_P10**	**C8T28SOI_LL_-CNIVX9_P16**
A to Z ↓	0.0066	0.0076	2.2696	2.4536

A to Z ↑	0.0109	0.0122	3.5274	3.9952
	C8T28SOI_LL_-CNIVX14_P0	**C8T28SOI_LL_-CNIVX14_P4**	**C8T28SOI_LL_-CNIVX14_P0**	**C8T28SOI_LL_-CNIVX14_P4**
A to Z ↓	0.0046	0.0056	1.2905	1.3897
A to Z ↑	0.0087	0.0097	1.8302	2.0486
	C8T28SOI_LL_-CNIVX14_P10	**C8T28SOI_LL_-CNIVX14_P16**	**C8T28SOI_LL_-CNIVX14_P10**	**C8T28SOI_LL_-CNIVX14_P16**
A to Z ↓	0.0069	0.0080	1.5280	1.6511
A to Z ↑	0.0111	0.0124	2.3853	2.7010
	C8T28SOI_LL_-CNIVX18_P0	**C8T28SOI_LL_-CNIVX18_P4**	**C8T28SOI_LL_-CNIVX18_P0**	**C8T28SOI_LL_-CNIVX18_P4**
A to Z ↓	0.0051	0.0061	1.0244	1.1047
A to Z ↑	0.0089	0.0099	1.3848	1.5515
	C8T28SOI_LL_-CNIVX18_P10	**C8T28SOI_LL_-CNIVX18_P16**	**C8T28SOI_LL_-CNIVX18_P10**	**C8T28SOI_LL_-CNIVX18_P16**
A to Z ↓	0.0075	0.0087	1.2170	1.3194
A to Z ↑	0.0114	0.0128	1.8025	2.0398
	C8T28SOI_LL_-CNIVX22_P0	**C8T28SOI_LL_-CNIVX22_P4**	**C8T28SOI_LL_-CNIVX22_P0**	**C8T28SOI_LL_-CNIVX22_P4**
A to Z ↓	0.0046	0.0056	0.8232	0.8882
A to Z ↑	0.0083	0.0092	1.1062	1.2374
	C8T28SOI_LL_-CNIVX22_P10	**C8T28SOI_LL_-CNIVX22_P16**	**C8T28SOI_LL_-CNIVX22_P10**	**C8T28SOI_LL_-CNIVX22_P16**
A to Z ↓	0.0069	0.0080	0.9777	1.0599
A to Z ↑	0.0106	0.0120	1.4391	1.6277
	C8T28SOI_LL_-CNIVX27_P0	**C8T28SOI_LL_-CNIVX27_P4**	**C8T28SOI_LL_-CNIVX27_P0**	**C8T28SOI_LL_-CNIVX27_P4**
A to Z ↓	0.0051	0.0061	0.6862	0.7392
A to Z ↑	0.0087	0.0097	0.9203	1.0282
	C8T28SOI_LL_-CNIVX27_P10	**C8T28SOI_LL_-CNIVX27_P16**	**C8T28SOI_LL_-CNIVX27_P10**	**C8T28SOI_LL_-CNIVX27_P16**
A to Z ↓	0.0075	0.0086	0.8162	0.8835
A to Z ↑	0.0112	0.0125	1.1969	1.3535
	C8T28SOI_LL_-CNIVX32_P0	**C8T28SOI_LL_-CNIVX32_P4**	**C8T28SOI_LL_-CNIVX32_P0**	**C8T28SOI_LL_-CNIVX32_P4**
A to Z ↓	0.0049	0.0060	0.5647	0.6085
A to Z ↑	0.0087	0.0098	0.7856	0.8808
	C8T28SOI_LL_-CNIVX32_P10	**C8T28SOI_LL_-CNIVX32_P16**	**C8T28SOI_LL_-CNIVX32_P10**	**C8T28SOI_LL_-CNIVX32_P16**
A to Z ↓	0.0073	0.0084	0.6713	0.7268
A to Z ↑	0.0111	0.0125	1.0230	1.1575
	C8T28SOI_LL_-CNIVX37_P0	**C8T28SOI_LL_-CNIVX37_P4**	**C8T28SOI_LL_-CNIVX37_P0**	**C8T28SOI_LL_-CNIVX37_P4**
A to Z ↓	0.0050	0.0061	0.4988	0.5376
A to Z ↑	0.0088	0.0099	0.6914	0.7750
	C8T28SOI_LL_-CNIVX37_P10	**C8T28SOI_LL_-CNIVX37_P16**	**C8T28SOI_LL_-CNIVX37_P10**	**C8T28SOI_LL_-CNIVX37_P16**
A to Z ↓	0.0075	0.0086	0.5931	0.6417
A to Z ↑	0.0113	0.0126	0.8997	1.0178
	C8T28SOI_LL_-CNIVX74_P0	**C8T28SOI_LL_-CNIVX74_P4**	**C8T28SOI_LL_-CNIVX74_P0**	**C8T28SOI_LL_-CNIVX74_P4**
A to Z ↓	0.0070	0.0083	0.2527	0.2724
A to Z ↑	0.0105	0.0117	0.3488	0.3906

	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A to Z ↓	0.0097	0.0110	0.3005	0.3250
A to Z ↑	0.0132	0.0146	0.4535	0.5123
	C8T28SOIDV_LL_-CNIVX18_P0	**C8T28SOIDV_LL_-CNIVX18_P4**	**C8T28SOIDV_LL_-CNIVX18_P0**	**C8T28SOIDV_LL_-CNIVX18_P4**
A to Z ↓	0.0045	0.0055	0.9411	1.0162
A to Z ↑	0.0083	0.0093	1.3429	1.5055
	C8T28SOIDV_LL_-CNIVX18_P10	**C8T28SOIDV_LL_-CNIVX18_P16**	**C8T28SOIDV_LL_-CNIVX18_P10**	**C8T28SOIDV_LL_-CNIVX18_P16**
A to Z ↓	0.0069	0.0080	1.1192	1.2136
A to Z ↑	0.0107	0.0120	1.7562	1.9898
	C8T28SOIDV_LL_-CNIVX28_P0	**C8T28SOIDV_LL_-CNIVX28_P4**	**C8T28SOIDV_LL_-CNIVX28_P0**	**C8T28SOIDV_LL_-CNIVX28_P4**
A to Z ↓	0.0049	0.0059	0.6405	0.6916
A to Z ↑	0.0084	0.0094	0.8955	1.0041
	C8T28SOIDV_LL_-CNIVX28_P10	**C8T28SOIDV_LL_-CNIVX28_P16**	**C8T28SOIDV_LL_-CNIVX28_P10**	**C8T28SOIDV_LL_-CNIVX28_P16**
A to Z ↓	0.0072	0.0083	0.7623	0.8266
A to Z ↑	0.0109	0.0122	1.1710	1.3277
	C8T28SOIDV_LL_-CNIVX37_P0	**C8T28SOIDV_LL_-CNIVX37_P4**	**C8T28SOIDV_LL_-CNIVX37_P0**	**C8T28SOIDV_LL_-CNIVX37_P4**
A to Z ↓	0.0047	0.0056	0.4827	0.5211
A to Z ↑	0.0080	0.0089	0.6714	0.7528
	C8T28SOIDV_LL_-CNIVX37_P10	**C8T28SOIDV_LL_-CNIVX37_P16**	**C8T28SOIDV_LL_-CNIVX37_P10**	**C8T28SOIDV_LL_-CNIVX37_P16**
A to Z ↓	0.0070	0.0079	0.5754	0.6235
A to Z ↑	0.0104	0.0115	0.8777	0.9946
	C8T28SOIDV_LL_-CNIVX55_P0	**C8T28SOIDV_LL_-CNIVX55_P4**	**C8T28SOIDV_LL_-CNIVX55_P0**	**C8T28SOIDV_LL_-CNIVX55_P4**
A to Z ↓	0.0047	0.0057	0.3252	0.3511
A to Z ↑	0.0079	0.0088	0.4492	0.5033
	C8T28SOIDV_LL_-CNIVX55_P10	**C8T28SOIDV_LL_-CNIVX55_P16**	**C8T28SOIDV_LL_-CNIVX55_P10**	**C8T28SOIDV_LL_-CNIVX55_P16**
A to Z ↓	0.0070	0.0080	0.3879	0.4204
A to Z ↑	0.0102	0.0115	0.5869	0.6647
	C8T28SOIDV_LL_-CNIVX74_P0	**C8T28SOIDV_LL_-CNIVX74_P4**	**C8T28SOIDV_LL_-CNIVX74_P0**	**C8T28SOIDV_LL_-CNIVX74_P4**
A to Z ↓	0.0052	0.0062	0.2475	0.2676
A to Z ↑	0.0082	0.0091	0.3383	0.3794
	C8T28SOIDV_LL_-CNIVX74_P10	**C8T28SOIDV_LL_-CNIVX74_P16**	**C8T28SOIDV_LL_-CNIVX74_P10**	**C8T28SOIDV_LL_-CNIVX74_P16**
A to Z ↓	0.0074	0.0085	0.2951	0.3198
A to Z ↑	0.0105	0.0118	0.4415	0.5000

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_CNIVX2_P0	1.351e-05	1.000e-20
C8T28SOI_LL_CNIVX2_P4	4.925e-06	1.000e-20
C8T28SOI_LL_CNIVX2_P10	1.635e-06	1.000e-20
C8T28SOI_LL_CNIVX2_P16	7.797e-07	1.000e-20
C8T28SOI_LL_CNIVX4_P0	2.683e-05	1.000e-20

C8T28SOI_LL_CNIVX4_P4	9.724e-06	1.000e-20
C8T28SOI_LL_CNIVX4_P10	3.169e-06	1.000e-20
C8T28SOI_LL_CNIVX4_P16	1.485e-06	1.000e-20
C8T28SOI_LL_CNIVX9_P0	5.725e-05	1.000e-20
C8T28SOI_LL_CNIVX9_P4	2.062e-05	1.000e-20
C8T28SOI_LL_CNIVX9_P10	6.649e-06	1.000e-20
C8T28SOI_LL_CNIVX9_P16	3.089e-06	1.000e-20
C8T28SOI_LL_CNIVX14_P0	8.348e-05	1.000e-20
C8T28SOI_LL_CNIVX14_P4	2.993e-05	1.000e-20
C8T28SOI_LL_CNIVX14_P10	9.608e-06	1.000e-20
C8T28SOI_LL_CNIVX14_P16	4.452e-06	1.000e-20
C8T28SOI_LL_CNIVX18_P0	1.064e-04	1.000e-20
C8T28SOI_LL_CNIVX18_P4	3.807e-05	1.000e-20
C8T28SOI_LL_CNIVX18_P10	1.216e-05	1.000e-20
C8T28SOI_LL_CNIVX18_P16	5.603e-06	1.000e-20
C8T28SOI_LL_CNIVX22_P0	1.308e-04	1.000e-20
C8T28SOI_LL_CNIVX22_P4	4.676e-05	1.000e-20
C8T28SOI_LL_CNIVX22_P10	1.491e-05	1.000e-20
C8T28SOI_LL_CNIVX22_P16	6.863e-06	1.000e-20
C8T28SOI_LL_CNIVX27_P0	1.553e-04	1.000e-20
C8T28SOI_LL_CNIVX27_P4	5.546e-05	1.000e-20
C8T28SOI_LL_CNIVX27_P10	1.767e-05	1.000e-20
C8T28SOI_LL_CNIVX27_P16	8.126e-06	1.000e-20
C8T28SOI_LL_CNIVX32_P0	1.823e-04	1.000e-20
C8T28SOI_LL_CNIVX32_P4	6.525e-05	1.000e-20
C8T28SOI_LL_CNIVX32_P10	2.082e-05	1.000e-20
C8T28SOI_LL_CNIVX32_P16	9.583e-06	1.000e-20
C8T28SOI_LL_CNIVX37_P0	2.071e-04	1.000e-20
C8T28SOI_LL_CNIVX37_P4	7.409e-05	1.000e-20
C8T28SOI_LL_CNIVX37_P10	2.363e-05	1.000e-20
C8T28SOI_LL_CNIVX37_P16	1.087e-05	1.000e-20
C8T28SOI_LL_CNIVX74_P0	4.052e-04	1.000e-20
C8T28SOI_LL_CNIVX74_P4	1.448e-04	1.000e-20
C8T28SOI_LL_CNIVX74_P10	4.610e-05	1.000e-20
C8T28SOI_LL_CNIVX74_P16	2.118e-05	1.000e-20
C8T28SOIDV_LL_CNIVX18_P0	1.175e-04	1.000e-20
C8T28SOIDV_LL_CNIVX18_P4	4.177e-05	1.000e-20
C8T28SOIDV_LL_CNIVX18_P10	1.325e-05	1.000e-20
C8T28SOIDV_LL_CNIVX18_P16	6.083e-06	1.000e-20
C8T28SOIDV_LL_CNIVX28_P0	1.743e-04	1.000e-20
C8T28SOIDV_LL_CNIVX28_P4	6.136e-05	1.000e-20
C8T28SOIDV_LL_CNIVX28_P10	1.926e-05	1.000e-20
C8T28SOIDV_LL_CNIVX28_P16	8.788e-06	1.000e-20
C8T28SOIDV_LL_CNIVX37_P0	2.280e-04	1.000e-20
C8T28SOIDV_LL_CNIVX37_P4	7.999e-05	1.000e-20
C8T28SOIDV_LL_CNIVX37_P10	2.502e-05	1.000e-20
C8T28SOIDV_LL_CNIVX37_P16	1.138e-05	1.000e-20
C8T28SOIDV_LL_CNIVX55_P0	3.351e-04	1.000e-20
C8T28SOIDV_LL_CNIVX55_P4	1.172e-04	1.000e-20
C8T28SOIDV_LL_CNIVX55_P10	3.650e-05	1.000e-20
C8T28SOIDV_LL_CNIVX55_P16	1.655e-05	1.000e-20
C8T28SOIDV_LL_CNIVX74_P0	4.440e-04	1.000e-20

C8T28SOIDV_LL_CNIVX74_P4	1.549e-04	1.000e-20
C8T28SOIDV_LL_CNIVX74_P10	4.815e-05	1.000e-20
C8T28SOIDV_LL_CNIVX74_P16	2.179e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_-CNIVX2_P0	C8T28SOI_LL_-CNIVX2_P4	C8T28SOI_LL_-CNIVX2_P10	C8T28SOI_LL_-CNIVX2_P16
A to Z	3.263e-04	2.851e-04	2.578e-04	2.478e-04
	C8T28SOI_LL_-CNIVX4_P0	C8T28SOI_LL_-CNIVX4_P4	C8T28SOI_LL_-CNIVX4_P10	C8T28SOI_LL_-CNIVX4_P16
A to Z	4.891e-04	4.100e-04	3.548e-04	3.299e-04
	C8T28SOI_LL_-CNIVX9_P0	C8T28SOI_LL_-CNIVX9_P4	C8T28SOI_LL_-CNIVX9_P10	C8T28SOI_LL_-CNIVX9_P16
A to Z	9.521e-04	7.661e-04	6.277e-04	5.652e-04
	C8T28SOI_LL_-CNIVX14_P0	C8T28SOI_LL_-CNIVX14_P4	C8T28SOI_LL_-CNIVX14_P10	C8T28SOI_LL_-CNIVX14_P16
A to Z	1.463e-03	1.190e-03	9.870e-04	8.982e-04
	C8T28SOI_LL_-CNIVX18_P0	C8T28SOI_LL_-CNIVX18_P4	C8T28SOI_LL_-CNIVX18_P10	C8T28SOI_LL_-CNIVX18_P16
A to Z	1.954e-03	1.605e-03	1.350e-03	1.241e-03
	C8T28SOI_LL_-CNIVX22_P0	C8T28SOI_LL_-CNIVX22_P4	C8T28SOI_LL_-CNIVX22_P10	C8T28SOI_LL_-CNIVX22_P16
A to Z	2.330e-03	1.878e-03	1.549e-03	1.402e-03
	C8T28SOI_LL_-CNIVX27_P0	C8T28SOI_LL_-CNIVX27_P4	C8T28SOI_LL_-CNIVX27_P10	C8T28SOI_LL_-CNIVX27_P16
A to Z	2.864e-03	2.336e-03	1.947e-03	1.774e-03
	C8T28SOI_LL_-CNIVX32_P0	C8T28SOI_LL_-CNIVX32_P4	C8T28SOI_LL_-CNIVX32_P10	C8T28SOI_LL_-CNIVX32_P16
A to Z	3.330e-03	2.698e-03	2.229e-03	2.018e-03
	C8T28SOI_LL_-CNIVX37_P0	C8T28SOI_LL_-CNIVX37_P4	C8T28SOI_LL_-CNIVX37_P10	C8T28SOI_LL_-CNIVX37_P16
A to Z	3.828e-03	3.122e-03	2.598e-03	2.360e-03
	C8T28SOI_LL_-CNIVX74_P0	C8T28SOI_LL_-CNIVX74_P4	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A to Z	7.962e-03	6.476e-03	5.302e-03	4.748e-03
	C8T28SOIDV_LL_-CNIVX18_P0	C8T28SOIDV_LL_-CNIVX18_P4	C8T28SOIDV_LL_-CNIVX18_P10	C8T28SOIDV_LL_-CNIVX18_P16
A to Z	1.892e-03	1.514e-03	1.244e-03	1.120e-03
	C8T28SOIDV_LL_-CNIVX28_P0	C8T28SOIDV_LL_-CNIVX28_P4	C8T28SOIDV_LL_-CNIVX28_P10	C8T28SOIDV_LL_-CNIVX28_P16
A to Z	2.912e-03	2.355e-03	1.956e-03	1.781e-03
	C8T28SOIDV_LL_-CNIVX37_P0	C8T28SOIDV_LL_-CNIVX37_P4	C8T28SOIDV_LL_-CNIVX37_P10	C8T28SOIDV_LL_-CNIVX37_P16
A to Z	3.711e-03	2.950e-03	2.419e-03	2.152e-03
	C8T28SOIDV_LL_-CNIVX55_P0	C8T28SOIDV_LL_-CNIVX55_P4	C8T28SOIDV_LL_-CNIVX55_P10	C8T28SOIDV_LL_-CNIVX55_P16
A to Z	5.500e-03	4.397e-03	3.601e-03	3.224e-03
	C8T28SOIDV_LL_-CNIVX74_P0	C8T28SOIDV_LL_-CNIVX74_P4	C8T28SOIDV_LL_-CNIVX74_P10	C8T28SOIDV_LL_-CNIVX74_P16
A to Z	7.407e-03	5.930e-03	4.850e-03	4.344e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

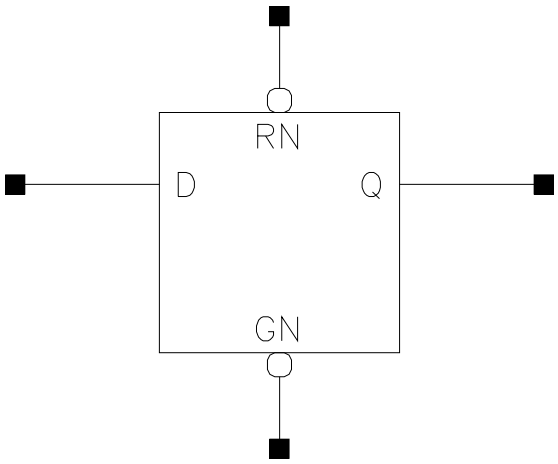
Pin Cycle (vdds)	C8T28SOI_LL_-CNIVX2_P0	C8T28SOI_LL_-CNIVX2_P4	C8T28SOI_LL_-CNIVX2_P10	C8T28SOI_LL_-CNIVX2_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX4_P0	C8T28SOI_LL_-CNIVX4_P4	C8T28SOI_LL_-CNIVX4_P10	C8T28SOI_LL_-CNIVX4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX9_P0	C8T28SOI_LL_-CNIVX9_P4	C8T28SOI_LL_-CNIVX9_P10	C8T28SOI_LL_-CNIVX9_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX14_P0	C8T28SOI_LL_-CNIVX14_P4	C8T28SOI_LL_-CNIVX14_P10	C8T28SOI_LL_-CNIVX14_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX18_P0	C8T28SOI_LL_-CNIVX18_P4	C8T28SOI_LL_-CNIVX18_P10	C8T28SOI_LL_-CNIVX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX22_P0	C8T28SOI_LL_-CNIVX22_P4	C8T28SOI_LL_-CNIVX22_P10	C8T28SOI_LL_-CNIVX22_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX27_P0	C8T28SOI_LL_-CNIVX27_P4	C8T28SOI_LL_-CNIVX27_P10	C8T28SOI_LL_-CNIVX27_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX32_P0	C8T28SOI_LL_-CNIVX32_P4	C8T28SOI_LL_-CNIVX32_P10	C8T28SOI_LL_-CNIVX32_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX37_P0	C8T28SOI_LL_-CNIVX37_P4	C8T28SOI_LL_-CNIVX37_P10	C8T28SOI_LL_-CNIVX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX74_P0	C8T28SOI_LL_-CNIVX74_P4	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX18_P0	C8T28SOIDV_LL_-CNIVX18_P4	C8T28SOIDV_LL_-CNIVX18_P10	C8T28SOIDV_LL_-CNIVX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX28_P0	C8T28SOIDV_LL_-CNIVX28_P4	C8T28SOIDV_LL_-CNIVX28_P10	C8T28SOIDV_LL_-CNIVX28_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX37_P0	C8T28SOIDV_LL_-CNIVX37_P4	C8T28SOIDV_LL_-CNIVX37_P10	C8T28SOIDV_LL_-CNIVX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX55_P0	C8T28SOIDV_LL_-CNIVX55_P4	C8T28SOIDV_LL_-CNIVX55_P10	C8T28SOIDV_LL_-CNIVX55_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX74_P0	C8T28SOIDV_LL_-CNIVX74_P4	C8T28SOIDV_LL_-CNIVX74_P10	C8T28SOIDV_LL_-CNIVX74_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNLDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	1.600	1.360	2.1760
X19_P4	1.600	1.360	2.1760
X19_P10	1.600	1.360	2.1760
X19_P16	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
D	0.0009	0.0010	0.0010	0.0010
GN	0.0012	0.0013	0.0013	0.0014
RN	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	X19_P4	X19_P0	X19_P4

D to Q ↓	0.0466	0.0538	0.9468	1.0319
D to Q ↑	0.0479	0.0542	1.3412	1.5139
GN to Q ↓	0.0415	0.0478	0.9470	1.0323
GN to Q ↑	0.0532	0.0602	1.3451	1.5180
RN to Q ↓	0.0632	0.0731	0.9838	1.0777
RN to Q ↑	0.0536	0.0604	1.3429	1.5138
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
D to Q ↓	0.0653	0.0768	1.1547	1.2673
D to Q ↑	0.0643	0.0740	1.7783	2.0258
GN to Q ↓	0.0573	0.0666	1.1555	1.2666
GN to Q ↑	0.0712	0.0818	1.7834	2.0332
RN to Q ↓	0.0890	0.1048	1.2130	1.3387
RN to Q ↑	0.0709	0.0811	1.7779	2.0285

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X19_P0	X19_P4	X19_P10	X19_P16
D ↓	hold_rising to GN	-0.0101	-0.0149	-0.0243	-0.0308
D ↑	hold_rising to GN	-0.0088	-0.0137	-0.0212	-0.0289
D ↓	setup_rising to GN	0.0494	0.0597	0.0715	0.0835
D ↑	setup_rising to GN	0.0482	0.0590	0.0687	0.0811
GN ↓	min_pulse_width to GN	0.0576	0.0621	0.0756	0.0856
RN ↓	min_pulse_width to RN	0.0735	0.0854	0.1023	0.1169
RN ↑	recovery_rising to GN	0.0579	0.0682	0.0779	0.0902
RN ↑	removal_rising to GN	-0.0365	-0.0413	-0.0479	-0.0586

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X19_P0	1.966e-04	1.000e-20
X19_P4	6.860e-05	1.000e-20
X19_P10	2.148e-05	1.000e-20
X19_P16	9.807e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
D (output stable)	3.552e-05	4.286e-05	6.643e-05	7.720e-05
GN (output stable)	9.241e-04	8.940e-04	8.990e-04	9.110e-04
RN (output stable)	5.693e-05	5.271e-05	4.614e-05	4.196e-05
D to Q	7.016e-03	6.570e-03	6.368e-03	6.383e-03
GN to Q	8.467e-03	8.003e-03	7.808e-03	7.846e-03
RN to Q	5.520e-03	5.191e-03	5.043e-03	5.045e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

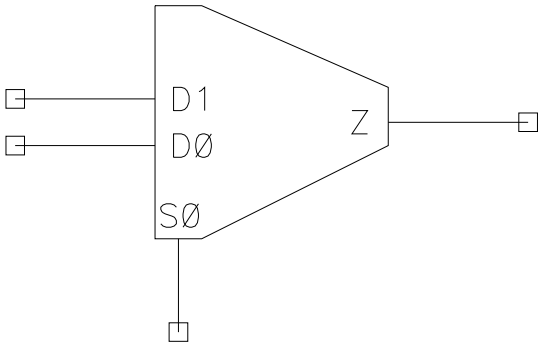
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX21

Cell Description

2:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	1.632	1.3056
X9_P4	0.800	1.632	1.3056
X9_P10	0.800	1.632	1.3056
X9_P16	0.800	1.632	1.3056
X15_P0	0.800	2.312	1.8496
X15_P4	0.800	2.312	1.8496
X15_P10	0.800	2.312	1.8496
X15_P16	0.800	2.312	1.8496
X27_P0	0.800	2.584	2.0672
X27_P4	0.800	2.584	2.0672
X27_P10	0.800	2.584	2.0672
X27_P16	0.800	2.584	2.0672

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
D0	0.0006	0.0006	0.0006	0.0007
D1	0.0006	0.0006	0.0007	0.0007
S0	0.0011	0.0011	0.0012	0.0013
	X15_P0	X15_P4	X15_P10	X15_P16
D0	0.0009	0.0010	0.0010	0.0011
D1	0.0009	0.0010	0.0010	0.0011
S0	0.0011	0.0011	0.0012	0.0012
	X27_P0	X27_P4	X27_P10	X27_P16

D0	0.0010	0.0010	0.0011	0.0011
D1	0.0010	0.0010	0.0011	0.0011
S0	0.0013	0.0013	0.0014	0.0015

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
D0 to Z ↓	0.0329	0.0375	1.8930	2.0519
D0 to Z ↑	0.0268	0.0304	2.8194	3.1653
D1 to Z ↓	0.0327	0.0373	1.8910	2.0494
D1 to Z ↑	0.0260	0.0294	2.8151	3.1631
S0 to Z ↓	0.0275	0.0314	1.8854	2.0422
S0 to Z ↑	0.0266	0.0302	2.8149	3.1607
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
D0 to Z ↓	0.0445	0.0511	2.2750	2.4808
D0 to Z ↑	0.0355	0.0403	3.7007	4.2064
D1 to Z ↓	0.0444	0.0511	2.2748	2.4766
D1 to Z ↑	0.0344	0.0390	3.6972	4.2020
S0 to Z ↓	0.0371	0.0426	2.2676	2.4728
S0 to Z ↑	0.0355	0.0405	3.6969	4.2047
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
D0 to Z ↓	0.0307	0.0351	1.2914	1.4008
D0 to Z ↑	0.0305	0.0344	1.5168	1.7057
D1 to Z ↓	0.0326	0.0373	1.2943	1.4021
D1 to Z ↑	0.0289	0.0325	1.5142	1.7017
S0 to Z ↓	0.0338	0.0385	1.2904	1.3986
S0 to Z ↑	0.0340	0.0386	1.5160	1.7026
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
D0 to Z ↓	0.0418	0.0481	1.5548	1.6957
D0 to Z ↑	0.0404	0.0459	1.9953	2.2694
D1 to Z ↓	0.0445	0.0515	1.5574	1.6993
D1 to Z ↑	0.0380	0.0431	1.9909	2.2652
S0 to Z ↓	0.0456	0.0522	1.5535	1.6944
S0 to Z ↑	0.0455	0.0519	1.9909	2.2667
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0342	0.0391	0.7092	0.7699
D0 to Z ↑	0.0321	0.0362	0.8939	1.0044
D1 to Z ↓	0.0358	0.0411	0.7110	0.7722
D1 to Z ↑	0.0323	0.0363	0.8950	1.0048
S0 to Z ↓	0.0362	0.0412	0.7098	0.7702
S0 to Z ↑	0.0342	0.0387	0.8927	1.0046
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.0467	0.0540	0.8581	0.9371
D0 to Z ↑	0.0425	0.0484	1.1726	1.3335
D1 to Z ↓	0.0492	0.0569	0.8601	0.9401
D1 to Z ↑	0.0424	0.0481	1.1735	1.3329
S0 to Z ↓	0.0489	0.0562	0.8581	0.9378
S0 to Z ↑	0.0456	0.0521	1.1723	1.3326

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds

X9_P0	1.676e-04	1.000e-20
X9_P4	6.000e-05	1.000e-20
X9_P10	1.926e-05	1.000e-20
X9_P16	8.935e-06	1.000e-20
X15_P0	2.294e-04	1.000e-20
X15_P4	8.138e-05	1.000e-20
X15_P10	2.597e-05	1.000e-20
X15_P16	1.201e-05	1.000e-20
X27_P0	3.275e-04	1.000e-20
X27_P4	1.167e-04	1.000e-20
X27_P10	3.719e-05	1.000e-20
X27_P16	1.712e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	8.825e-04	8.128e-04	7.650e-04	7.458e-04
D1 (output stable)	8.607e-04	7.903e-04	7.418e-04	7.217e-04
S0 (output stable)	9.866e-04	9.351e-04	9.151e-04	9.212e-04
D0 to Z	2.867e-03	2.751e-03	2.723e-03	2.759e-03
D1 to Z	2.784e-03	2.672e-03	2.649e-03	2.687e-03
S0 to Z	3.190e-03	3.049e-03	3.007e-03	3.042e-03
	X15_P0	X15_P4	X15_P10	X15_P16
D0 (output stable)	1.158e-03	1.026e-03	9.364e-04	8.969e-04
D1 (output stable)	1.229e-03	1.108e-03	1.026e-03	9.899e-04
S0 (output stable)	9.606e-04	9.432e-04	9.508e-04	9.730e-04
D0 to Z	4.886e-03	4.647e-03	4.572e-03	4.610e-03
D1 to Z	4.808e-03	4.572e-03	4.498e-03	4.536e-03
S0 to Z	5.236e-03	5.014e-03	4.957e-03	5.010e-03
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	1.286e-03	1.135e-03	1.031e-03	9.831e-04
D1 (output stable)	1.312e-03	1.176e-03	1.081e-03	1.040e-03
S0 (output stable)	1.119e-03	1.089e-03	1.090e-03	1.113e-03
D0 to Z	7.462e-03	7.035e-03	6.852e-03	6.871e-03
D1 to Z	7.469e-03	7.032e-03	6.833e-03	6.844e-03
S0 to Z	7.914e-03	7.494e-03	7.320e-03	7.352e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

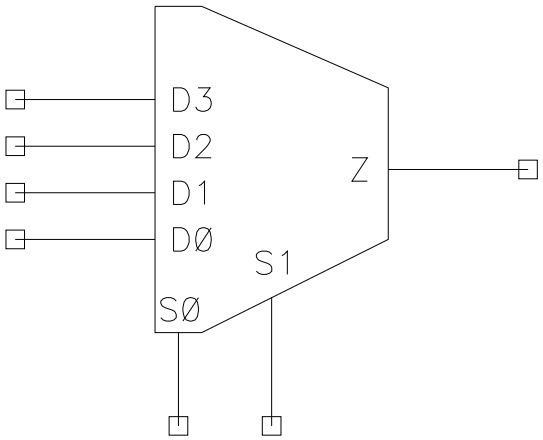
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX41

Cell Description

4:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	1.600	1.768	2.8288
X9_P4	1.600	1.768	2.8288
X9_P10	1.600	1.768	2.8288
X9_P16	1.600	1.768	2.8288
X27_P0	1.600	2.584	4.1344
X27_P4	1.600	2.584	4.1344
X27_P10	1.600	2.584	4.1344
X27_P16	1.600	2.584	4.1344

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
D0	0.0006	0.0006	0.0006	0.0006
D1	0.0004	0.0004	0.0005	0.0005
D2	0.0006	0.0006	0.0006	0.0006
D3	0.0004	0.0005	0.0005	0.0005
S0	0.0015	0.0015	0.0016	0.0017
S1	0.0008	0.0008	0.0009	0.0009

	X27_P0	X27_P4	X27_P10	X27_P16
D0	0.0008	0.0008	0.0009	0.0009
D1	0.0007	0.0007	0.0008	0.0008
D2	0.0008	0.0009	0.0009	0.0009
D3	0.0008	0.0008	0.0009	0.0009
S0	0.0021	0.0022	0.0023	0.0025
S1	0.0016	0.0017	0.0018	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
D0 to Z ↓	0.0598	0.0690	1.9939	2.1679
D0 to Z ↑	0.0508	0.0574	2.8726	3.2329
D1 to Z ↓	0.0595	0.0686	1.9937	2.1688
D1 to Z ↑	0.0504	0.0570	2.8720	3.2312
D2 to Z ↓	0.0602	0.0694	1.9997	2.1750
D2 to Z ↑	0.0485	0.0549	2.8616	3.2222
D3 to Z ↓	0.0588	0.0678	1.9993	2.1744
D3 to Z ↑	0.0480	0.0544	2.8586	3.2194
S0 to Z ↓	0.0653	0.0758	1.9954	2.1699
S0 to Z ↑	0.0605	0.0691	2.8718	3.2325
S1 to Z ↓	0.0451	0.0520	1.9955	2.1692
S1 to Z ↑	0.0475	0.0535	2.8664	3.2272
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
D0 to Z ↓	0.0829	0.0966	2.4187	2.6516
D0 to Z ↑	0.0675	0.0773	3.7863	4.3134
D1 to Z ↓	0.0826	0.0962	2.4216	2.6537
D1 to Z ↑	0.0673	0.0771	3.7863	4.3107
D2 to Z ↓	0.0836	0.0975	2.4280	2.6612
D2 to Z ↑	0.0648	0.0743	3.7713	4.2941
D3 to Z ↓	0.0818	0.0955	2.4260	2.6600
D3 to Z ↑	0.0642	0.0736	3.7690	4.2935
S0 to Z ↓	0.0919	0.1077	2.4220	2.6541
S0 to Z ↑	0.0823	0.0952	3.7851	4.3100
S1 to Z ↓	0.0626	0.0729	2.4232	2.6556
S1 to Z ↑	0.0629	0.0720	3.7783	4.3031
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0631	0.0727	0.6657	0.7258
D0 to Z ↑	0.0588	0.0666	1.0411	1.1715
D1 to Z ↓	0.0684	0.0789	0.6735	0.7348
D1 to Z ↑	0.0588	0.0666	1.0420	1.1719
D2 to Z ↓	0.0676	0.0778	0.6713	0.7320
D2 to Z ↑	0.0593	0.0670	1.0419	1.1722
D3 to Z ↓	0.0646	0.0744	0.6676	0.7275
D3 to Z ↑	0.0585	0.0661	1.0416	1.1716
S0 to Z ↓	0.0757	0.0874	0.6683	0.7284
S0 to Z ↑	0.0715	0.0814	1.0425	1.1722
S1 to Z ↓	0.0523	0.0602	0.6696	0.7302
S1 to Z ↑	0.0577	0.0649	1.0426	1.1714
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.0877	0.1023	0.8136	0.8939
D0 to Z ↑	0.0788	0.0907	1.3696	1.5597

D1 to Z ↓	0.0952	0.1111	0.8247	0.9076
D1 to Z ↑	0.0788	0.0906	1.3700	1.5595
D2 to Z ↓	0.0940	0.1097	0.8213	0.9034
D2 to Z ↑	0.0792	0.0910	1.3708	1.5590
D3 to Z ↓	0.0899	0.1049	0.8158	0.8972
D3 to Z ↑	0.0783	0.0899	1.3709	1.5597
S0 to Z ↓	0.1055	0.1232	0.8168	0.8983
S0 to Z ↑	0.0972	0.1126	1.3716	1.5611
S1 to Z ↓	0.0726	0.0849	0.8189	0.9008
S1 to Z ↑	0.0766	0.0880	1.3706	1.5593

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X9_P0	1.283e-04	1.000e-20
X9_P4	4.670e-05	1.000e-20
X9_P10	1.536e-05	1.000e-20
X9_P16	7.261e-06	1.000e-20
X27_P0	2.997e-04	1.000e-20
X27_P4	1.079e-04	1.000e-20
X27_P10	3.500e-05	1.000e-20
X27_P16	1.637e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	3.499e-05	3.369e-05	2.917e-05	2.114e-05
D1 (output stable)	4.657e-05	4.547e-05	4.351e-05	3.872e-05
D2 (output stable)	4.591e-05	4.467e-05	4.323e-05	3.620e-05
D3 (output stable)	4.731e-05	4.563e-05	4.282e-05	3.761e-05
S0 (output stable)	9.621e-04	9.697e-04	1.013e-03	1.069e-03
S1 (output stable)	1.133e-03	1.096e-03	1.011e-03	9.896e-04
D0 to Z	3.532e-03	3.357e-03	3.288e-03	3.317e-03
D1 to Z	3.516e-03	3.342e-03	3.280e-03	3.309e-03
D2 to Z	3.460e-03	3.286e-03	3.221e-03	3.243e-03
D3 to Z	3.442e-03	3.267e-03	3.201e-03	3.222e-03
S0 to Z	4.600e-03	4.458e-03	4.455e-03	4.550e-03
S1 to Z	3.943e-03	3.727e-03	3.477e-03	3.397e-03
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	7.016e-05	6.719e-05	6.002e-05	4.401e-05
D1 (output stable)	4.935e-05	4.651e-05	4.491e-05	4.217e-05
D2 (output stable)	7.218e-05	6.846e-05	6.164e-05	4.704e-05
D3 (output stable)	6.939e-05	6.661e-05	6.737e-05	5.873e-05
S0 (output stable)	1.805e-03	1.832e-03	1.919e-03	2.013e-03
S1 (output stable)	1.732e-03	1.694e-03	1.673e-03	1.672e-03
D0 to Z	1.002e-02	9.307e-03	8.931e-03	8.887e-03
D1 to Z	1.029e-02	9.546e-03	9.140e-03	9.088e-03
D2 to Z	1.030e-02	9.562e-03	9.172e-03	9.122e-03
D3 to Z	1.010e-02	9.388e-03	9.013e-03	8.973e-03
S0 to Z	1.215e-02	1.149e-02	1.122e-02	1.128e-02
S1 to Z	1.082e-02	1.003e-02	9.443e-03	9.177e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

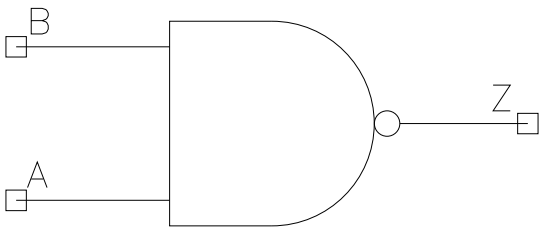
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2

Cell Description

2 input NAND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	0.800	0.952	0.7616
X8_P4	0.800	0.952	0.7616
X8_P10	0.800	0.952	0.7616
X8_P16	0.800	0.952	0.7616
X15_P0	0.800	1.224	0.9792
X15_P4	0.800	1.224	0.9792
X15_P10	0.800	1.224	0.9792
X15_P16	0.800	1.224	0.9792
X27_P0	0.800	1.632	1.3056
X27_P4	0.800	1.632	1.3056
X27_P10	0.800	1.632	1.3056
X27_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0010	0.0011	0.0011	0.0012
B	0.0009	0.0010	0.0010	0.0011
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0005	0.0005	0.0005	0.0005
B	0.0004	0.0004	0.0005	0.0005
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0005	0.0005	0.0006	0.0006
B	0.0006	0.0006	0.0007	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0069	0.0085	2.5238	2.7401
A to Z ↑	0.0145	0.0163	3.0907	3.4686
B to Z ↓	0.0070	0.0082	2.5513	2.7713
B to Z ↑	0.0120	0.0132	3.1073	3.4872
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0105	0.0121	3.0495	3.3351
A to Z ↑	0.0189	0.0212	4.0536	4.6013
B to Z ↓	0.0099	0.0112	3.0861	3.3713
B to Z ↑	0.0151	0.0168	4.0759	4.6289
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0354	0.0409	1.2641	1.3684
A to Z ↑	0.0373	0.0427	1.4659	1.6510
B to Z ↓	0.0372	0.0428	1.2630	1.3667
B to Z ↑	0.0380	0.0435	1.4686	1.6495
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0491	0.0573	1.5169	1.6501
A to Z ↑	0.0507	0.0585	1.9302	2.1944
B to Z ↓	0.0511	0.0593	1.5159	1.6502
B to Z ↑	0.0516	0.0596	1.9316	2.1952
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0354	0.0406	0.6517	0.7059
A to Z ↑	0.0365	0.0417	0.8729	0.9812
B to Z ↓	0.0362	0.0416	0.6510	0.7057
B to Z ↑	0.0357	0.0407	0.8740	0.9825
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0487	0.0566	0.7834	0.8537
A to Z ↑	0.0495	0.0570	1.1474	1.3015
B to Z ↓	0.0497	0.0576	0.7835	0.8548
B to Z ↑	0.0482	0.0555	1.1467	1.3034

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	5.814e-05	1.000e-20
X8_P4	2.142e-05	1.000e-20
X8_P10	7.116e-06	1.000e-20
X8_P16	3.383e-06	1.000e-20
X15_P0	1.316e-04	1.000e-20
X15_P4	4.725e-05	1.000e-20
X15_P10	1.529e-05	1.000e-20
X15_P16	7.142e-06	1.000e-20
X27_P0	2.333e-04	1.000e-20
X27_P4	8.411e-05	1.000e-20
X27_P10	2.711e-05	1.000e-20
X27_P16	1.259e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	5.435e-05	5.059e-05	4.752e-05	4.595e-05
B (output stable)	1.277e-04	1.297e-04	1.338e-04	1.673e-04
A to Z	1.416e-03	1.312e-03	1.271e-03	1.271e-03

B to Z	1.139e-03	9.867e-04	8.844e-04	8.374e-04
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	8.245e-06	7.664e-06	7.400e-06	7.077e-06
B (output stable)	1.567e-05	1.612e-05	1.599e-05	1.563e-05
A to Z	4.061e-03	4.019e-03	4.044e-03	4.168e-03
B to Z	4.017e-03	3.962e-03	3.974e-03	4.088e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.268e-05	1.144e-05	1.085e-05	1.063e-05
B (output stable)	1.868e-05	1.920e-05	1.880e-05	1.864e-05
A to Z	6.275e-03	6.143e-03	6.174e-03	6.320e-03
B to Z	6.225e-03	6.081e-03	6.090e-03	6.228e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

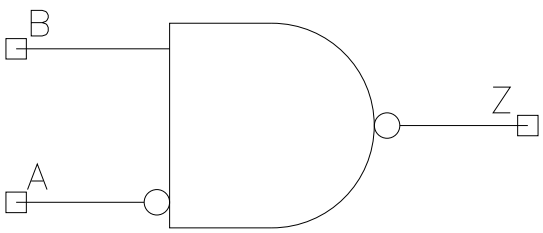
Pin Cycle (vdds)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2A

Cell Description

2 input NAND with A input inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	0.952	0.7616
X9_P4	0.800	0.952	0.7616
X9_P10	0.800	0.952	0.7616
X9_P16	0.800	0.952	0.7616
X15_P0	0.800	1.360	1.0880
X15_P4	0.800	1.360	1.0880
X15_P10	0.800	1.360	1.0880
X15_P16	0.800	1.360	1.0880
X27_P0	0.800	2.856	2.2848
X27_P4	0.800	2.856	2.2848
X27_P10	0.800	2.856	2.2848
X27_P16	0.800	2.856	2.2848

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
A	0.0005	0.0005	0.0005	0.0006
B	0.0005	0.0005	0.0006	0.0006
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0005	0.0005	0.0005	0.0006
B	0.0005	0.0005	0.0005	0.0006
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0015	0.0016	0.0017	0.0018
B	0.0031	0.0032	0.0033	0.0035

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
A to Z ↓	0.0278	0.0321	1.8687	2.0215
A to Z ↑	0.0219	0.0249	2.6718	2.9975
B to Z ↓	0.0303	0.0351	1.8668	2.0195
B to Z ↑	0.0310	0.0350	2.6660	2.9914
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
A to Z ↓	0.0386	0.0449	2.2436	2.4481
A to Z ↑	0.0291	0.0330	3.4950	3.9744
B to Z ↓	0.0425	0.0497	2.2438	2.4455
B to Z ↑	0.0412	0.0471	3.4984	3.9692
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0477	0.0550	1.3022	1.4080
A to Z ↑	0.0420	0.0484	1.4574	1.6339
B to Z ↓	0.0359	0.0414	1.3015	1.4078
B to Z ↑	0.0368	0.0420	1.4561	1.6349
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0662	0.0775	1.5585	1.6977
A to Z ↑	0.0584	0.0682	1.9050	2.1653
B to Z ↓	0.0498	0.0582	1.5585	1.6965
B to Z ↑	0.0498	0.0575	1.9087	2.1647
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0241	0.0275	0.8572	0.9322
A to Z ↑	0.0234	0.0268	0.8716	0.9813
B to Z ↓	0.0082	0.0092	0.8769	0.9520
B to Z ↑	0.0092	0.0104	0.7214	0.8080
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0326	0.0372	1.0408	1.1381
A to Z ↑	0.0316	0.0360	1.1498	1.3080
B to Z ↓	0.0106	0.0118	1.0596	1.1577
B to Z ↑	0.0121	0.0135	0.9377	1.0609

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X9_P0	1.099e-04	1.000e-20
X9_P4	4.002e-05	1.000e-20
X9_P10	1.305e-05	1.000e-20
X9_P16	6.117e-06	1.000e-20
X15_P0	1.359e-04	1.000e-20
X15_P4	4.963e-05	1.000e-20
X15_P10	1.635e-05	1.000e-20
X15_P16	7.735e-06	1.000e-20
X27_P0	2.686e-04	1.000e-20
X27_P4	9.669e-05	1.000e-20
X27_P10	3.130e-05	1.000e-20
X27_P16	1.461e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	1.797e-05	1.728e-05	1.697e-05	1.665e-05
B (output stable)	7.437e-04	6.753e-04	6.368e-04	6.256e-04
A to Z	2.150e-03	2.065e-03	2.050e-03	2.089e-03

B to Z	2.846e-03	2.763e-03	2.765e-03	2.824e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	6.072e-04	5.847e-04	5.857e-04	6.016e-04
B (output stable)	1.471e-05	1.467e-05	1.468e-05	1.469e-05
A to Z	4.495e-03	4.461e-03	4.550e-03	4.724e-03
B to Z	3.874e-03	3.807e-03	3.853e-03	3.993e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	3.437e-03	3.395e-03	3.498e-03	3.645e-03
B (output stable)	3.481e-04	3.552e-04	3.829e-04	4.797e-04
A to Z	7.610e-03	7.538e-03	7.719e-03	7.923e-03
B to Z	3.856e-03	3.257e-03	2.823e-03	2.620e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

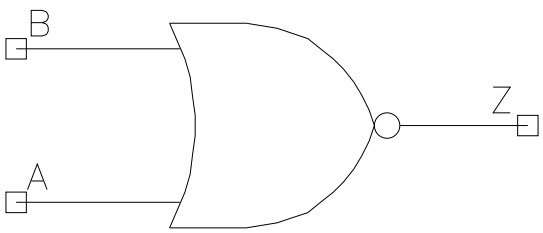
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2

Cell Description

2 input NOR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	0.800	0.952	0.7616
X8_P4	0.800	0.952	0.7616
X8_P10	0.800	0.952	0.7616
X8_P16	0.800	0.952	0.7616
X15_P0	0.800	1.360	1.0880
X15_P4	0.800	1.360	1.0880
X15_P10	0.800	1.360	1.0880
X15_P16	0.800	1.360	1.0880
X27_P0	0.800	1.632	1.3056
X27_P4	0.800	1.632	1.3056
X27_P10	0.800	1.632	1.3056
X27_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0012	0.0012	0.0013	0.0014
B	0.0010	0.0011	0.0011	0.0012
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0004	0.0005	0.0005	0.0005
B	0.0005	0.0005	0.0005	0.0006
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0005	0.0005	0.0006	0.0006
B	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0096	0.0111	2.1215	2.2866
A to Z ↑	0.0126	0.0148	3.7735	4.1724
B to Z ↓	0.0071	0.0083	2.1245	2.2908
B to Z ↑	0.0114	0.0127	3.7911	4.1983
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0132	0.0148	2.5153	2.7232
A to Z ↑	0.0178	0.0204	4.7806	5.3681
B to Z ↓	0.0099	0.0112	2.5222	2.7286
B to Z ↑	0.0145	0.0162	4.8157	5.4052
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0343	0.0396	1.2570	1.3604
A to Z ↑	0.0371	0.0427	1.4603	1.6438
B to Z ↓	0.0332	0.0384	1.2552	1.3607
B to Z ↑	0.0382	0.0437	1.4603	1.6431
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0478	0.0555	1.5072	1.6401
A to Z ↑	0.0515	0.0599	1.9256	2.1911
B to Z ↓	0.0463	0.0539	1.5072	1.6386
B to Z ↑	0.0521	0.0601	1.9255	2.1910
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0362	0.0423	0.6951	0.7542
A to Z ↑	0.0374	0.0433	0.8597	0.9659
B to Z ↓	0.0366	0.0426	0.6949	0.7536
B to Z ↑	0.0383	0.0440	0.8592	0.9670
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0509	0.0598	0.8377	0.9142
A to Z ↑	0.0520	0.0606	1.1301	1.2857
B to Z ↓	0.0513	0.0600	0.8372	0.9138
B to Z ↑	0.0524	0.0606	1.1316	1.2852

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P0	7.116e-05	1.000e-20
X8_P4	2.526e-05	1.000e-20
X8_P10	8.029e-06	1.000e-20
X8_P16	3.693e-06	1.000e-20
X15_P0	1.638e-04	1.000e-20
X15_P4	5.756e-05	1.000e-20
X15_P10	1.817e-05	1.000e-20
X15_P16	8.336e-06	1.000e-20
X27_P0	2.611e-04	1.000e-20
X27_P4	9.031e-05	1.000e-20
X27_P10	2.788e-05	1.000e-20
X27_P16	1.257e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	8.107e-05	7.907e-05	7.829e-05	8.059e-05
B (output stable)	1.828e-04	1.829e-04	1.684e-04	1.113e-04
A to Z	1.598e-03	1.513e-03	1.494e-03	1.520e-03

B to Z	1.193e-03	1.028e-03	9.132e-04	8.620e-04
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.510e-05	1.460e-05	1.437e-05	1.408e-05
B (output stable)	2.497e-05	2.444e-05	2.356e-05	1.962e-05
A to Z	4.097e-03	4.041e-03	4.120e-03	4.236e-03
B to Z	4.025e-03	3.952e-03	4.008e-03	4.114e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.905e-05	1.773e-05	1.769e-05	1.726e-05
B (output stable)	3.100e-05	3.084e-05	2.967e-05	2.600e-05
A to Z	6.149e-03	6.078e-03	6.062e-03	6.253e-03
B to Z	6.060e-03	5.968e-03	5.926e-03	6.100e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

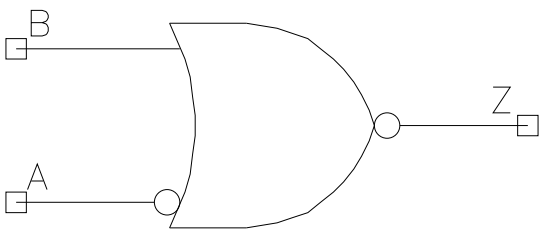
Pin Cycle (vdds)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2A

Cell Description

2 input NOR with A input Inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	1.360	1.0880
X9_P4	0.800	1.360	1.0880
X9_P10	0.800	1.360	1.0880
X9_P16	0.800	1.360	1.0880
X15_P0	0.800	1.496	1.1968
X15_P4	0.800	1.496	1.1968
X15_P10	0.800	1.496	1.1968
X15_P16	0.800	1.496	1.1968
X27_P0	0.800	1.768	1.4144
X27_P4	0.800	1.768	1.4144
X27_P10	0.800	1.768	1.4144
X27_P16	0.800	1.768	1.4144

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
A	0.0009	0.0009	0.0010	0.0010
B	0.0007	0.0007	0.0008	0.0008
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0006	0.0006	0.0006	0.0007
B	0.0006	0.0006	0.0006	0.0007
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0006	0.0006	0.0007	0.0007
B	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
A to Z ↓	0.0284	0.0322	1.8423	1.9899
A to Z ↑	0.0181	0.0210	2.8057	3.1500
B to Z ↓	0.0273	0.0318	1.8332	1.9846
B to Z ↑	0.0305	0.0346	2.8042	3.1494
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
A to Z ↓	0.0381	0.0436	2.2061	2.3971
A to Z ↑	0.0252	0.0289	3.6814	4.1812
B to Z ↓	0.0386	0.0450	2.1977	2.3907
B to Z ↑	0.0407	0.0465	3.6779	4.1804
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0457	0.0527	1.2586	1.3613
A to Z ↑	0.0431	0.0502	1.4622	1.6458
B to Z ↓	0.0334	0.0388	1.2566	1.3618
B to Z ↑	0.0396	0.0453	1.4623	1.6436
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0633	0.0738	1.5081	1.6397
A to Z ↑	0.0608	0.0710	1.9271	2.1935
B to Z ↓	0.0465	0.0541	1.5089	1.6413
B to Z ↑	0.0540	0.0624	1.9266	2.1913
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0460	0.0532	0.6647	0.7218
A to Z ↑	0.0445	0.0512	0.8659	0.9736
B to Z ↓	0.0376	0.0434	0.6651	0.7208
B to Z ↑	0.0391	0.0446	0.8660	0.9737
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0647	0.0764	0.8017	0.8768
A to Z ↑	0.0618	0.0723	1.1380	1.2944
B to Z ↓	0.0524	0.0617	0.8023	0.8758
B to Z ↑	0.0530	0.0616	1.1384	1.2935

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X9_P0	1.247e-04	1.000e-20
X9_P4	4.449e-05	1.000e-20
X9_P10	1.425e-05	1.000e-20
X9_P16	6.607e-06	1.000e-20
X15_P0	1.889e-04	1.000e-20
X15_P4	6.646e-05	1.000e-20
X15_P10	2.098e-05	1.000e-20
X15_P16	9.624e-06	1.000e-20
X27_P0	2.750e-04	1.000e-20
X27_P4	9.648e-05	1.000e-20
X27_P10	3.018e-05	1.000e-20
X27_P16	1.371e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	4.816e-05	4.385e-05	4.021e-05	3.870e-05
B (output stable)	9.804e-04	9.083e-04	8.917e-04	9.221e-04
A to Z	2.490e-03	2.419e-03	2.434e-03	2.486e-03

B to Z	3.131e-03	3.067e-03	3.102e-03	3.174e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	7.807e-04	7.422e-04	7.345e-04	7.469e-04
B (output stable)	2.670e-05	2.629e-05	2.530e-05	2.418e-05
A to Z	4.918e-03	4.891e-03	4.958e-03	5.115e-03
B to Z	4.109e-03	4.054e-03	4.077e-03	4.200e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	8.028e-04	7.560e-04	7.458e-04	7.598e-04
B (output stable)	3.250e-05	3.159e-05	3.027e-05	2.869e-05
A to Z	7.155e-03	6.988e-03	7.060e-03	7.307e-03
B to Z	6.321e-03	6.115e-03	6.123e-03	6.326e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

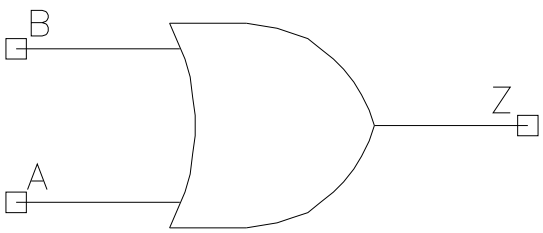
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR2

Cell Description

2 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	0.800	1.632	1.3056
X19_P4	0.800	1.632	1.3056
X19_P10	0.800	1.632	1.3056
X19_P16	0.800	1.632	1.3056
X37_P0	0.800	2.176	1.7408
X37_P4	0.800	2.176	1.7408
X37_P10	0.800	2.176	1.7408
X37_P16	0.800	2.176	1.7408

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0014	0.0014	0.0015	0.0016
B	0.0013	0.0014	0.0015	0.0015
	X37_P0	X37_P4	X37_P10	X37_P16
A	0.0014	0.0014	0.0015	0.0016
B	0.0013	0.0014	0.0014	0.0015

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0256	0.0294	0.9403	1.0176
A to Z ↑	0.0216	0.0244	1.3505	1.5129
B to Z ↓	0.0255	0.0287	0.9405	1.0173
B to Z ↑	0.0194	0.0219	1.3492	1.5101
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**

A to Z ↓	0.0352	0.0411	1.1263	1.2270
A to Z ↑	0.0284	0.0323	1.7621	1.9989
B to Z ↓	0.0338	0.0389	1.1271	1.2264
B to Z ↑	0.0256	0.0290	1.7595	1.9966
	X37_P0	**X37_P4**	**X37_P0**	**X37_P4**
A to Z ↓	0.0320	0.0367	0.4831	0.5229
A to Z ↑	0.0269	0.0302	0.7094	0.7983
B to Z ↓	0.0326	0.0371	0.4828	0.5231
B to Z ↑	0.0248	0.0280	0.7096	0.7966
	X37_P10	**X37_P16**	**X37_P10**	**X37_P16**
A to Z ↓	0.0441	0.0519	0.5810	0.6347
A to Z ↑	0.0352	0.0401	0.9320	1.0597
B to Z ↓	0.0438	0.0510	0.5808	0.6342
B to Z ↑	0.0326	0.0372	0.9298	1.0573

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X19_P0	1.714e-04	1.000e-20
X19_P4	6.299e-05	1.000e-20
X19_P10	2.075e-05	1.000e-20
X19_P16	9.784e-06	1.000e-20
X37_P0	2.578e-04	1.000e-20
X37_P4	9.507e-05	1.000e-20
X37_P10	3.145e-05	1.000e-20
X37_P16	1.487e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	8.028e-05	7.751e-05	7.672e-05	7.835e-05
B (output stable)	1.780e-04	1.778e-04	1.661e-04	1.125e-04
A to Z	4.741e-03	4.565e-03	4.579e-03	4.710e-03
B to Z	4.335e-03	4.085e-03	4.022e-03	4.083e-03
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	7.881e-05	7.618e-05	7.568e-05	7.664e-05
B (output stable)	1.828e-04	1.841e-04	1.768e-04	1.217e-04
A to Z	8.430e-03	7.993e-03	7.826e-03	8.033e-03
B to Z	8.005e-03	7.513e-03	7.260e-03	7.410e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

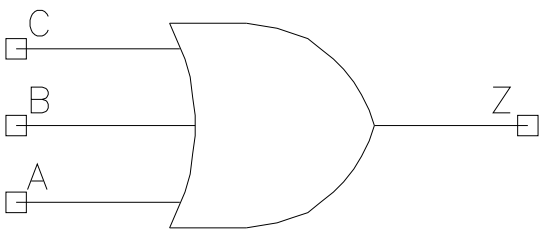
Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR3

Cell Description

3 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	0.800	2.312	1.8496
X14_P4	0.800	2.312	1.8496
X14_P10	0.800	2.312	1.8496
X14_P16	0.800	2.312	1.8496
X19_P0	0.800	2.448	1.9584
X19_P4	0.800	2.448	1.9584
X19_P10	0.800	2.448	1.9584
X19_P16	0.800	2.448	1.9584
X27_P0	1.600	2.312	3.6992
X27_P4	1.600	2.312	3.6992
X27_P10	1.600	2.312	3.6992
X27_P16	1.600	2.312	3.6992

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0004	0.0004	0.0004	0.0005
B	0.0004	0.0004	0.0005	0.0005
C	0.0004	0.0004	0.0005	0.0005
	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0004	0.0004	0.0004	0.0005
B	0.0004	0.0004	0.0005	0.0005
C	0.0004	0.0004	0.0005	0.0005
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0018	0.0019	0.0020	0.0021
B	0.0019	0.0020	0.0021	0.0022

C	0.0017	0.0017	0.0018	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0564	0.0648	1.2296	1.3290
A to Z ↑	0.0514	0.0585	1.7673	1.9849
B to Z ↓	0.0577	0.0659	1.2281	1.3296
B to Z ↑	0.0504	0.0574	1.7694	1.9828
C to Z ↓	0.0484	0.0550	1.2296	1.3278
C to Z ↑	0.0451	0.0512	1.7697	1.9855
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0787	0.0918	1.4734	1.6043
A to Z ↑	0.0701	0.0808	2.3151	2.6317
B to Z ↓	0.0794	0.0922	1.4734	1.6035
B to Z ↑	0.0688	0.0793	2.3157	2.6303
C to Z ↓	0.0662	0.0765	1.4730	1.6043
C to Z ↑	0.0613	0.0705	2.3155	2.6318
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0590	0.0681	0.9291	1.0057
A to Z ↑	0.0533	0.0609	1.3261	1.4900
B to Z ↓	0.0603	0.0692	0.9288	1.0055
B to Z ↑	0.0523	0.0598	1.3259	1.4889
C to Z ↓	0.0509	0.0584	0.9294	1.0051
C to Z ↑	0.0470	0.0536	1.3251	1.4878
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0828	0.0965	1.1150	1.2141
A to Z ↑	0.0729	0.0837	1.7390	1.9742
B to Z ↓	0.0835	0.0968	1.1148	1.2145
B to Z ↑	0.0716	0.0823	1.7385	1.9726
C to Z ↓	0.0703	0.0811	1.1160	1.2133
C to Z ↑	0.0640	0.0733	1.7384	1.9733
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0312	0.0360	0.8135	0.8857
A to Z ↑	0.0289	0.0327	0.8566	0.9634
B to Z ↓	0.0304	0.0347	0.8130	0.8859
B to Z ↑	0.0273	0.0309	0.8555	0.9616
C to Z ↓	0.0236	0.0268	0.8069	0.8784
C to Z ↑	0.0219	0.0247	0.8592	0.9655
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0433	0.0502	0.9901	1.0864
A to Z ↑	0.0385	0.0439	1.1268	1.2815
B to Z ↓	0.0412	0.0473	0.9904	1.0859
B to Z ↑	0.0364	0.0414	1.1254	1.2793
C to Z ↓	0.0315	0.0358	0.9816	1.0761
C to Z ↑	0.0289	0.0325	1.1284	1.2847

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X14_P0	1.772e-04	1.000e-20
X14_P4	6.615e-05	1.000e-20

X14_P10	2.220e-05	1.000e-20
X14_P16	1.061e-05	1.000e-20
X19_P0	1.975e-04	1.000e-20
X19_P4	7.393e-05	1.000e-20
X19_P10	2.488e-05	1.000e-20
X19_P16	1.191e-05	1.000e-20
X27_P0	3.199e-04	1.000e-20
X27_P4	1.180e-04	1.000e-20
X27_P10	3.908e-05	1.000e-20
X27_P16	1.849e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	3.655e-04	3.697e-04	3.857e-04	4.025e-04
B (output stable)	3.502e-04	3.506e-04	3.612e-04	3.720e-04
C (output stable)	9.370e-04	9.068e-04	9.048e-04	9.164e-04
A to Z	5.418e-03	5.339e-03	5.504e-03	5.652e-03
B to Z	5.356e-03	5.265e-03	5.415e-03	5.552e-03
C to Z	5.265e-03	5.163e-03	5.296e-03	5.426e-03
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	3.659e-04	3.699e-04	3.858e-04	4.031e-04
B (output stable)	3.503e-04	3.508e-04	3.613e-04	3.722e-04
C (output stable)	9.362e-04	9.068e-04	9.059e-04	9.151e-04
A to Z	6.271e-03	6.201e-03	6.318e-03	6.442e-03
B to Z	6.210e-03	6.126e-03	6.228e-03	6.342e-03
C to Z	6.116e-03	6.022e-03	6.113e-03	6.210e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.677e-03	1.698e-03	1.784e-03	1.883e-03
B (output stable)	1.547e-03	1.543e-03	1.575e-03	1.584e-03
C (output stable)	3.199e-03	3.101e-03	3.152e-03	3.353e-03
A to Z	9.585e-03	9.542e-03	9.831e-03	1.019e-02
B to Z	8.907e-03	8.768e-03	8.944e-03	9.221e-03
C to Z	6.901e-03	6.660e-03	6.656e-03	6.734e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

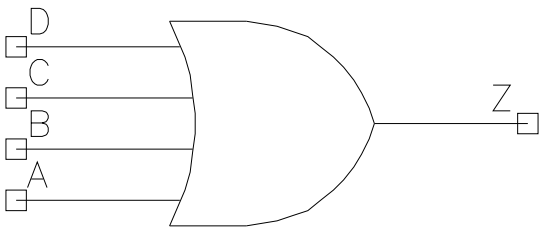
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR4

Cell Description

4 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	0.800	2.448	1.9584
X19_P4	0.800	2.448	1.9584
X19_P10	0.800	2.448	1.9584
X19_P16	0.800	2.448	1.9584
X27_P0	1.600	2.584	4.1344
X27_P4	1.600	2.584	4.1344
X27_P10	1.600	2.584	4.1344
X27_P16	1.600	2.584	4.1344

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0004	0.0004	0.0004	0.0005
B	0.0004	0.0004	0.0005	0.0005
C	0.0005	0.0005	0.0005	0.0005
D	0.0004	0.0004	0.0004	0.0005
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0019	0.0020	0.0021	0.0022
B	0.0017	0.0018	0.0019	0.0020
C	0.0019	0.0020	0.0021	0.0022
D	0.0018	0.0019	0.0020	0.0021

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0598	0.0689	0.9293	1.0061
A to Z ↑	0.0485	0.0556	1.3256	1.4884
B to Z ↓	0.0610	0.0700	0.9298	1.0057
B to Z ↑	0.0476	0.0545	1.3254	1.4863
C to Z ↓	0.0576	0.0664	0.9298	1.0060
C to Z ↑	0.0445	0.0510	1.3254	1.4901
D to Z ↓	0.0586	0.0672	0.9292	1.0061
D to Z ↑	0.0434	0.0498	1.3248	1.4870
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0834	0.0975	1.1159	1.2157
A to Z ↑	0.0662	0.0763	1.7375	1.9717
B to Z ↓	0.0841	0.0979	1.1161	1.2150
B to Z ↑	0.0649	0.0749	1.7369	1.9724
C to Z ↓	0.0802	0.0938	1.1156	1.2143
C to Z ↑	0.0608	0.0701	1.7381	1.9729
D to Z ↓	0.0806	0.0938	1.1149	1.2138
D to Z ↑	0.0594	0.0685	1.7367	1.9725
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0292	0.0339	0.8182	0.8909
A to Z ↑	0.0289	0.0328	0.8621	0.9698
B to Z ↓	0.0300	0.0342	0.8182	0.8909
B to Z ↑	0.0265	0.0300	0.8606	0.9684
C to Z ↓	0.0284	0.0324	0.8158	0.8892
C to Z ↑	0.0266	0.0299	0.8655	0.9723
D to Z ↓	0.0275	0.0311	0.8161	0.8887
D to Z ↑	0.0244	0.0273	0.8639	0.9711
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0409	0.0475	0.9958	1.0927
A to Z ↑	0.0385	0.0438	1.1334	1.2886
B to Z ↓	0.0406	0.0466	0.9967	1.0929
B to Z ↑	0.0353	0.0401	1.1310	1.2856
C to Z ↓	0.0389	0.0449	0.9946	1.0900
C to Z ↑	0.0350	0.0396	1.1371	1.2925
D to Z ↓	0.0366	0.0420	0.9945	1.0911
D to Z ↑	0.0317	0.0358	1.1348	1.2901

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X19_P0	1.808e-04	1.000e-20
X19_P4	6.775e-05	1.000e-20
X19_P10	2.284e-05	1.000e-20
X19_P16	1.095e-05	1.000e-20
X27_P0	3.005e-04	1.000e-20
X27_P4	1.116e-04	1.000e-20
X27_P10	3.724e-05	1.000e-20
X27_P16	1.771e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	4.508e-04	4.540e-04	4.703e-04	4.884e-04

B (output stable)	4.285e-04	4.265e-04	4.364e-04	4.479e-04
C (output stable)	3.675e-04	3.643e-04	3.726e-04	3.830e-04
D (output stable)	3.441e-04	3.354e-04	3.362e-04	3.394e-04
A to Z	5.839e-03	5.795e-03	5.879e-03	6.031e-03
B to Z	5.776e-03	5.720e-03	5.789e-03	5.933e-03
C to Z	5.605e-03	5.556e-03	5.627e-03	5.772e-03
D to Z	5.572e-03	5.507e-03	5.563e-03	5.697e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	2.048e-03	2.076e-03	2.178e-03	2.288e-03
B (output stable)	1.843e-03	1.839e-03	1.895e-03	1.929e-03
C (output stable)	1.850e-03	1.844e-03	1.912e-03	2.047e-03
D (output stable)	1.649e-03	1.604e-03	1.607e-03	1.660e-03
A to Z	9.250e-03	9.205e-03	9.466e-03	9.789e-03
B to Z	8.564e-03	8.443e-03	8.609e-03	8.864e-03
C to Z	7.951e-03	7.716e-03	7.775e-03	7.955e-03
D to Z	7.286e-03	6.955e-03	6.889e-03	6.989e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

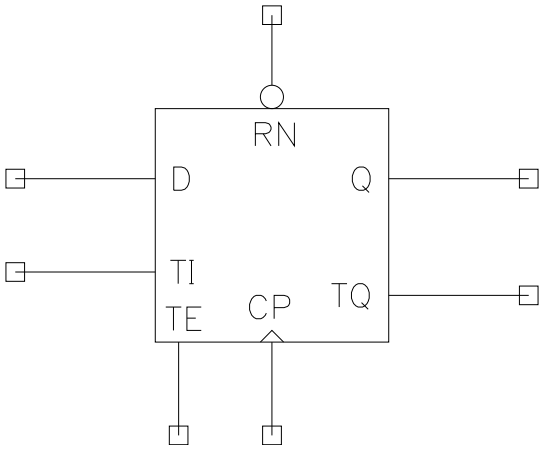
Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNSDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	1.600	2.176	3.4816
X9_P4	1.600	2.176	3.4816
X9_P10	1.600	2.176	3.4816
X9_P16	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
CP	0.0005	0.0005	0.0005	0.0005
D	0.0004	0.0004	0.0004	0.0005
RN	0.0007	0.0007	0.0007	0.0008

TE	0.0007	0.0008	0.0008	0.0009
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	X9_P4	X9_P0	X9_P4
CP to Q ↓	0.0804	0.0919	1.9310	2.0908
CP to Q ↑	0.0843	0.0966	2.5451	2.8607
CP to TQ ↓	0.0824	0.0944	6.9824	7.5247
CP to TQ ↑	0.0886	0.1016	14.0398	15.9058
RN to Q ↓	0.0733	0.0840	1.9297	2.0886
RN to TQ ↓	0.0754	0.0865	6.9814	7.5228
	X9_P10	X9_P16	X9_P10	X9_P16
CP to Q ↓	0.1100	0.1275	2.3196	2.5239
CP to Q ↑	0.1157	0.1340	3.3534	3.8145
CP to TQ ↓	0.1131	0.1312	8.2929	8.9780
CP to TQ ↑	0.1216	0.1409	18.7125	21.3604
RN to Q ↓	0.1010	0.1174	2.3194	2.5247
RN to TQ ↓	0.1041	0.1211	8.2927	8.9786

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X9_P0	X9_P4	X9_P10	X9_P16
CP ↓	min_pulse_width to CP	0.0706	0.0858	0.1058	0.1281
CP ↑	min_pulse_width to CP	0.0439	0.0484	0.0576	0.0621
D ↓	hold_rising to CP	-0.0019	-0.0068	-0.0143	-0.0214
D ↑	hold_rising to CP	-0.0017	-0.0045	-0.0120	-0.0169
D ↓	setup_rising to CP	0.0467	0.0537	0.0688	0.0840
D ↑	setup_rising to CP	0.0298	0.0347	0.0417	0.0466
RN ↓	min_pulse_width to RN	0.0540	0.0610	0.0708	0.0828
RN ↑	recovery_rising to CP	0.0103	0.0103	0.0151	0.0206
RN ↑	removal_rising to CP	-0.0007	-0.0006	-0.0028	-0.0060
TE ↓	hold_rising to CP	0.0003	-0.0045	-0.0126	-0.0198
TE ↑	hold_rising to CP	-0.0147	-0.0196	-0.0244	-0.0316
TE ↓	setup_rising to CP	0.0415	0.0517	0.0668	0.0792
TE ↑	setup_rising to CP	0.0835	0.1030	0.1301	0.1545
TI ↓	hold_rising to CP	-0.0426	-0.0537	-0.0753	-0.0890
TI ↑	hold_rising to CP	-0.0157	-0.0203	-0.0267	-0.0328
TI ↓	setup_rising to CP	0.0819	0.0981	0.1280	0.1497
TI ↑	setup_rising to CP	0.0437	0.0502	0.0579	0.0677

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X9_P0	2.469e-04	1.000e-20
X9_P4	8.985e-05	1.000e-20
X9_P10	2.955e-05	1.000e-20
X9_P16	1.398e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

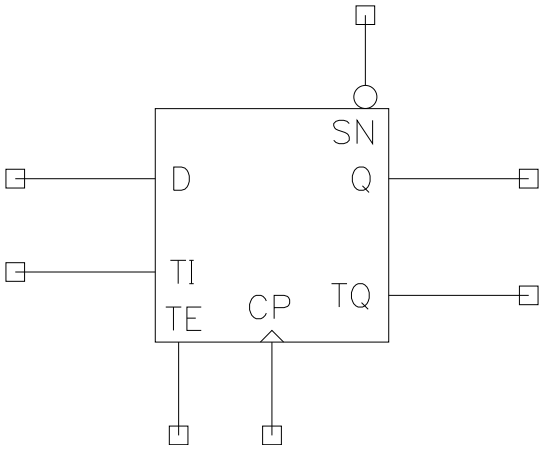
Pin Cycle	X9_P0	X9_P4	X9_P10	X9_P16
Clock 100Mhz Data 0Mhz	5.148e-03	5.154e-03	5.206e-03	5.276e-03
Clock 100Mhz Data 25Mhz	5.522e-03	5.530e-03	5.615e-03	5.725e-03
Clock 100Mhz Data 50Mhz	5.897e-03	5.906e-03	6.024e-03	6.173e-03
Clock = 0 Data 100Mhz	2.215e-03	2.233e-03	2.272e-03	2.317e-03
Clock = 1 Data 100Mhz	2.889e-05	2.753e-05	2.652e-05	2.594e-05

CNSDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	1.600	2.176	3.4816
X9_P4	1.600	2.176	3.4816
X9_P10	1.600	2.176	3.4816
X9_P16	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
CP	0.0005	0.0005	0.0005	0.0005
D	0.0003	0.0003	0.0003	0.0003
SN	0.0007	0.0008	0.0008	0.0009

TE	0.0008	0.0008	0.0008	0.0009
TI	0.0003	0.0003	0.0003	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	X9_P4	X9_P0	X9_P4
CP to Q ↓	0.0800	0.0916	1.9392	2.0956
CP to Q ↑	0.0819	0.0940	2.5503	2.8684
CP to TQ ↓	0.0816	0.0937	6.9935	7.5350
CP to TQ ↑	0.0859	0.0987	14.0242	15.8812
SN to Q ↑	0.0601	0.0691	2.5504	2.8660
SN to TQ ↑	0.0641	0.0738	14.0236	15.8839
	X9_P10	X9_P16	X9_P10	X9_P16
CP to Q ↓	0.1097	0.1273	2.3201	2.5221
CP to Q ↑	0.1129	0.1312	3.3541	3.8196
CP to TQ ↓	0.1124	0.1306	8.3039	8.9886
CP to TQ ↑	0.1186	0.1379	18.6912	21.3375
SN to Q ↑	0.0830	0.1015	3.3567	3.8200
SN to TQ ↑	0.0887	0.1081	18.6929	21.3379

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X9_P0	X9_P4	X9_P10	X9_P16
CP ↓	min_pulse_width to CP	0.0795	0.0936	0.1171	0.1376
CP ↑	min_pulse_width to CP	0.0439	0.0484	0.0576	0.0621
D ↓	hold_rising to CP	-0.0094	-0.0143	-0.0192	-0.0295
D ↑	hold_rising to CP	-0.0045	-0.0093	-0.0169	-0.0218
D ↓	setup_rising to CP	0.0516	0.0613	0.0791	0.0905
D ↑	setup_rising to CP	0.0347	0.0363	0.0466	0.0514
SN ↓	min_pulse_width to SN	0.0469	0.0518	0.0615	0.0686
SN ↑	recovery_rising to CP	-0.0066	-0.0007	-0.0012	-0.0012
SN ↑	removal_rising to CP	0.0333	0.0356	0.0405	0.0481
TE ↓	hold_rising to CP	-0.0072	-0.0126	-0.0175	-0.0241
TE ↑	hold_rising to CP	-0.0071	-0.0120	-0.0195	-0.0244
TE ↓	setup_rising to CP	0.0495	0.0565	0.0738	0.0889
TE ↑	setup_rising to CP	0.0933	0.1133	0.1398	0.1648
TI ↓	hold_rising to CP	-0.0524	-0.0635	-0.0835	-0.0990
TI ↑	hold_rising to CP	-0.0093	-0.0141	-0.0202	-0.0267
TI ↓	setup_rising to CP	0.0918	0.1078	0.1378	0.1595
TI ↑	setup_rising to CP	0.0391	0.0453	0.0517	0.0564

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X9_P0	2.345e-04	1.000e-20
X9_P4	8.631e-05	1.000e-20
X9_P10	2.875e-05	1.000e-20
X9_P16	1.372e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

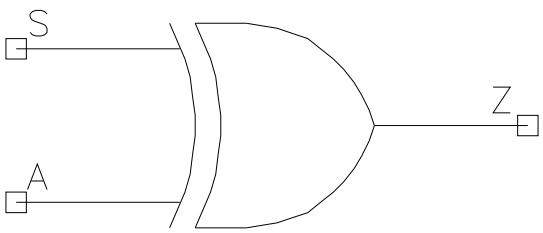
Pin Cycle	X9_P0	X9_P4	X9_P10	X9_P16
Clock 100Mhz Data 0Mhz	5.035e-03	5.043e-03	5.096e-03	5.167e-03
Clock 100Mhz Data 25Mhz	5.455e-03	5.467e-03	5.556e-03	5.671e-03
Clock 100Mhz Data 50Mhz	5.875e-03	5.890e-03	6.017e-03	6.175e-03
Clock = 0 Data 100Mhz	2.344e-03	2.359e-03	2.393e-03	2.433e-03
Clock = 1 Data 100Mhz	2.682e-05	2.587e-05	2.505e-05	2.455e-05

CNXOR2

Cell Description

2 input Exclusive OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	1.496	1.1968
X9_P4	0.800	1.496	1.1968
X9_P10	0.800	1.496	1.1968
X9_P16	0.800	1.496	1.1968
X15_P0	0.800	2.312	1.8496
X15_P4	0.800	2.312	1.8496
X15_P10	0.800	2.312	1.8496
X15_P16	0.800	2.312	1.8496
X27_P0	0.800	2.584	2.0672
X27_P4	0.800	2.584	2.0672
X27_P10	0.800	2.584	2.0672
X27_P16	0.800	2.584	2.0672

Truth Table

A	S	Z
1	S	!S
0	S	S

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
A	0.0006	0.0006	0.0006	0.0007
S	0.0012	0.0013	0.0013	0.0014
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0011	0.0011	0.0012	0.0013
S	0.0019	0.0019	0.0021	0.0022
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0009	0.0010	0.0011	0.0011
S	0.0019	0.0019	0.0020	0.0021

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
A to Z ↓	0.0371	0.0426	2.0142	2.1829
A to Z ↑	0.0359	0.0405	2.8329	3.1811
S to Z ↓	0.0284	0.0324	2.0063	2.1759
S to Z ↑	0.0283	0.0321	2.8334	3.1801
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
A to Z ↓	0.0510	0.0590	2.4250	2.6467
A to Z ↑	0.0475	0.0541	3.7110	4.2185
S to Z ↓	0.0383	0.0439	2.4186	2.6374
S to Z ↑	0.0377	0.0431	3.7111	4.2158
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0343	0.0395	1.2851	1.3906
A to Z ↑	0.0331	0.0376	1.5016	1.6898
S to Z ↓	0.0249	0.0286	1.2826	1.3894
S to Z ↑	0.0238	0.0272	1.4999	1.6870
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0474	0.0549	1.5438	1.6827
A to Z ↑	0.0444	0.0507	1.9761	2.2472
S to Z ↓	0.0342	0.0394	1.5415	1.6802
S to Z ↑	0.0322	0.0367	1.9737	2.2457
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0412	0.0472	0.7267	0.7874
A to Z ↑	0.0409	0.0461	0.8974	1.0094
S to Z ↓	0.0312	0.0357	0.7264	0.7875
S to Z ↑	0.0305	0.0345	0.8973	1.0085
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0567	0.0658	0.8769	0.9577
A to Z ↑	0.0545	0.0624	1.1791	1.3406
S to Z ↓	0.0429	0.0497	0.8759	0.9576
S to Z ↑	0.0409	0.0468	1.1798	1.3415

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X9_P0	1.897e-04	1.000e-20
X9_P4	6.770e-05	1.000e-20
X9_P10	2.164e-05	1.000e-20
X9_P16	1.000e-05	1.000e-20
X15_P0	3.283e-04	1.000e-20
X15_P4	1.160e-04	1.000e-20
X15_P10	3.672e-05	1.000e-20
X15_P16	1.686e-05	1.000e-20
X27_P0	3.868e-04	1.000e-20
X27_P4	1.360e-04	1.000e-20
X27_P10	4.283e-05	1.000e-20
X27_P16	1.960e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
A to Z	3.771e-03	3.650e-03	3.631e-03	3.689e-03
S to Z	3.318e-03	3.172e-03	3.124e-03	3.160e-03
	X15_P0	X15_P4	X15_P10	X15_P16

A to Z	6.633e-03	6.418e-03	6.391e-03	6.476e-03
S to Z	4.675e-03	4.365e-03	4.216e-03	4.208e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	9.253e-03	8.733e-03	8.537e-03	8.569e-03
S to Z	7.547e-03	6.936e-03	6.623e-03	6.574e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

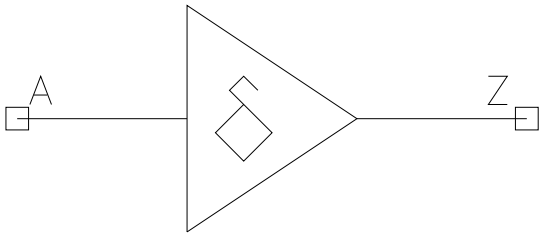
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DLYHF

Cell Description

Delay cell for Hold Time Fixing

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-DLYHFM4X4_P0	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X4_P4	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X4_P10	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X4_P16	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X12_P0	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM4X12_P4	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM4X12_P10	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM4X12_P16	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM8X4_P0	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X4_P4	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X4_P10	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X4_P16	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X12_P0	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X12_P4	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X12_P10	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X12_P16	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X30_P0	0.800	5.848	4.6784

C8T28SOI_LL_-DLYHFM8X30_P4	0.800	5.848	4.6784
C8T28SOI_LL_-DLYHFM8X30_P10	0.800	5.848	4.6784
C8T28SOI_LL_-DLYHFM8X30_P16	0.800	5.848	4.6784

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C8T28SOI_LL_-DLYHFM4X4_P0	C8T28SOI_LL_-DLYHFM4X4_P4	C8T28SOI_LL_-DLYHFM4X4_P10	C8T28SOI_LL_-DLYHFM4X4_P16
A	0.0007	0.0007	0.0007	0.0008
	C8T28SOI_LL_-DLYHFM4X12_P0	C8T28SOI_LL_-DLYHFM4X12_P4	C8T28SOI_LL_-DLYHFM4X12_P10	C8T28SOI_LL_-DLYHFM4X12_P16
A	0.0007	0.0007	0.0007	0.0007
	C8T28SOI_LL_-DLYHFM8X4_P0	C8T28SOI_LL_-DLYHFM8X4_P4	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LL_-DLYHFM8X12_P0	C8T28SOI_LL_-DLYHFM8X12_P4	C8T28SOI_LL_-DLYHFM8X12_P10	C8T28SOI_LL_-DLYHFM8X12_P16
A	0.0006	0.0006	0.0006	0.0006
	C8T28SOI_LL_-DLYHFM8X30_P0	C8T28SOI_LL_-DLYHFM8X30_P4	C8T28SOI_LL_-DLYHFM8X30_P10	C8T28SOI_LL_-DLYHFM8X30_P16
A	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-DLYHFM4X4_P0	**C8T28SOI_LL_-DLYHFM4X4_P4**	**C8T28SOI_LL_-DLYHFM4X4_P0**	**C8T28SOI_LL_-DLYHFM4X4_P4**
A to Z ↓	0.0868	0.0993	4.5421	4.9178
A to Z ↑	0.0834	0.0955	5.3546	6.0295
	C8T28SOI_LL_-DLYHFM4X4_P10	**C8T28SOI_LL_-DLYHFM4X4_P16**	**C8T28SOI_LL_-DLYHFM4X4_P10**	**C8T28SOI_LL_-DLYHFM4X4_P16**
A to Z ↓	0.1190	0.1386	5.4572	5.9485
A to Z ↑	0.1146	0.1335	7.0604	8.0287
	C8T28SOI_LL_-DLYHFM4X12_P0	**C8T28SOI_LL_-DLYHFM4X12_P4**	**C8T28SOI_LL_-DLYHFM4X12_P0**	**C8T28SOI_LL_-DLYHFM4X12_P4**
A to Z ↓	0.0977	0.1122	1.5972	1.7380
A to Z ↑	0.0926	0.1062	2.0313	2.2874
	C8T28SOI_LL_-DLYHFM4X12_P10	**C8T28SOI_LL_-DLYHFM4X12_P16**	**C8T28SOI_LL_-DLYHFM4X12_P10**	**C8T28SOI_LL_-DLYHFM4X12_P16**
A to Z ↓	0.1355	0.1590	1.9378	2.1230
A to Z ↑	0.1277	0.1492	2.6803	3.0557
	C8T28SOI_LL_-DLYHFM8X4_P0	**C8T28SOI_LL_-DLYHFM8X4_P4**	**C8T28SOI_LL_-DLYHFM8X4_P0**	**C8T28SOI_LL_-DLYHFM8X4_P4**
A to Z ↓	0.1646	0.1900	4.5274	4.9062
A to Z ↑	0.1498	0.1710	5.2522	5.9065

	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A to Z ↓	0.2319	0.2743	5.4363	5.9212
A to Z ↑	0.2051	0.2388	6.9264	7.8809
	C8T28SOI_LL_-DLYHFM8X12_P0	**C8T28SOI_LL_-DLYHFM8X12_P4**	**C8T28SOI_LL_-DLYHFM8X12_P0**	**C8T28SOI_LL_-DLYHFM8X12_P4**
A to Z ↓	0.1770	0.2046	1.5828	1.7202
A to Z ↑	0.1611	0.1840	2.0237	2.2795
	C8T28SOI_LL_-DLYHFM8X12_P10	**C8T28SOI_LL_-DLYHFM8X12_P16**	**C8T28SOI_LL_-DLYHFM8X12_P10**	**C8T28SOI_LL_-DLYHFM8X12_P16**
A to Z ↓	0.2504	0.2969	1.9207	2.1034
A to Z ↑	0.2211	0.2577	2.6724	3.0452
	C8T28SOI_LL_-DLYHFM8X30_P0	**C8T28SOI_LL_-DLYHFM8X30_P4**	**C8T28SOI_LL_-DLYHFM8X30_P0**	**C8T28SOI_LL_-DLYHFM8X30_P4**
A to Z ↓	0.2235	0.2582	0.6058	0.6558
A to Z ↑	0.2236	0.2576	0.8079	0.9087
	C8T28SOI_LL_-DLYHFM8X30_P10	**C8T28SOI_LL_-DLYHFM8X30_P16**	**C8T28SOI_LL_-DLYHFM8X30_P10**	**C8T28SOI_LL_-DLYHFM8X30_P16**
A to Z ↓	0.3151	0.3730	0.7289	0.7940
A to Z ↑	0.3125	0.3677	1.0627	1.2081

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_DLYHFM4X4_P0	3.528e-05	1.000e-20
C8T28SOI_LL_DLYHFM4X4_P4	1.321e-05	1.000e-20
C8T28SOI_LL_DLYHFM4X4_P10	4.505e-06	1.000e-20
C8T28SOI_LL_DLYHFM4X4_P16	2.190e-06	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P0	7.903e-05	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P4	2.855e-05	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P10	9.329e-06	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P16	4.400e-06	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P0	5.862e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P4	2.323e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P10	8.443e-06	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P16	4.287e-06	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P0	9.972e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P4	3.756e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P10	1.293e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P16	6.338e-06	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P0	2.315e-04	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P4	8.598e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P10	2.901e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P16	1.398e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_-DLYHFM4X4_P0	C8T28SOI_LL_-DLYHFM4X4_P4	C8T28SOI_LL_-DLYHFM4X4_P10	C8T28SOI_LL_-DLYHFM4X4_P16
A to Z	2.911e-03	2.951e-03	3.065e-03	3.194e-03
	C8T28SOI_LL_-DLYHFM4X12_P0	C8T28SOI_LL_-DLYHFM4X12_P4	C8T28SOI_LL_-DLYHFM4X12_P10	C8T28SOI_LL_-DLYHFM4X12_P16
A to Z	4.836e-03	4.711e-03	4.722e-03	4.831e-03

	C8T28SOI_LL_-DLYHFM8X4_P0	C8T28SOI_LL_-DLYHFM8X4_P4	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A to Z	8.463e-03	8.578e-03	8.942e-03	9.338e-03
	C8T28SOI_LL_-DLYHFM8X12_P0	C8T28SOI_LL_-DLYHFM8X12_P4	C8T28SOI_LL_-DLYHFM8X12_P10	C8T28SOI_LL_-DLYHFM8X12_P16
A to Z	1.002e-02	9.982e-03	1.025e-02	1.061e-02
	C8T28SOI_LL_-DLYHFM8X30_P0	C8T28SOI_LL_-DLYHFM8X30_P4	C8T28SOI_LL_-DLYHFM8X30_P10	C8T28SOI_LL_-DLYHFM8X30_P16
A to Z	1.849e-02	1.849e-02	1.901e-02	1.975e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

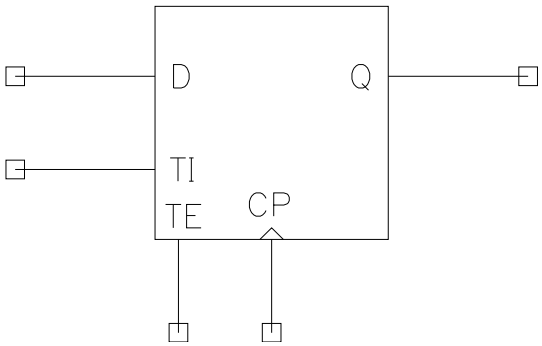
Pin Cycle (vdds)	C8T28SOI_LL_-DLYHFM4X4_P0	C8T28SOI_LL_-DLYHFM4X4_P4	C8T28SOI_LL_-DLYHFM4X4_P10	C8T28SOI_LL_-DLYHFM4X4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM4X12_P0	C8T28SOI_LL_-DLYHFM4X12_P4	C8T28SOI_LL_-DLYHFM4X12_P10	C8T28SOI_LL_-DLYHFM4X12_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM8X4_P0	C8T28SOI_LL_-DLYHFM8X4_P4	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM8X12_P0	C8T28SOI_LL_-DLYHFM8X12_P4	C8T28SOI_LL_-DLYHFM8X12_P10	C8T28SOI_LL_-DLYHFM8X12_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM8X30_P0	C8T28SOI_LL_-DLYHFM8X30_P4	C8T28SOI_LL_-DLYHFM8X30_P10	C8T28SOI_LL_-DLYHFM8X30_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFSYNCPQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	1.600	3.264	5.2224
C8T28SOIDV_LL1_-SDFSYNCPQX5_P4	1.600	3.264	5.2224
C8T28SOIDV_LL1_-SDFSYNCPQX5_P10	1.600	3.264	5.2224
C8T28SOIDV_LL1_-SDFSYNCPQX5_P16	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P0	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P4	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P10	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P16	1.600	3.264	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	C8T28SOIDV_LL1_-SDFSYNCPQX5_P4	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16
CP	0.0006	0.0006	0.0006	0.0007
D	0.0008	0.0008	0.0009	0.0009
TE	0.0008	0.0008	0.0009	0.0009
TI	0.0004	0.0004	0.0004	0.0004
	C8T28SOIDV_LL_-SDFSYNCPQX5_P0	C8T28SOIDV_LL_-SDFSYNCPQX5_P4	C8T28SOIDV_LL_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPQX5_-P16
CP	0.0004	0.0004	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0005
TE	0.0007	0.0008	0.0008	0.0009
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	**C8T28SOIDV_LL1_-SDFSYNCPQX5_P4**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_P0**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_P4**
CP to Q ↓	0.0828	0.0950	4.0340	4.4407
CP to Q ↑	0.0980	0.1122	5.3192	6.0063
	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10	**C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16**
CP to Q ↓	0.1145	0.1331	5.0424	5.6146
CP to Q ↑	0.1351	0.1577	7.0510	8.0386
	C8T28SOIDV_LL_-SDFSYNCPQX5_P0	**C8T28SOIDV_LL_-SDFSYNCPQX5_P4**	**C8T28SOIDV_LL_-SDFSYNCPQX5_P0**	**C8T28SOIDV_LL_-SDFSYNCPQX5_P4**
CP to Q ↓	0.1257	0.1452	4.3693	4.8591
CP to Q ↑	0.1554	0.1789	5.3944	6.0937
	C8T28SOIDV_LL_-SDFSYNCPQX5_-P10	**C8T28SOIDV_LL_-SDFSYNCPQX5_-P16**	**C8T28SOIDV_LL_-SDFSYNCPQX5_-P10**	**C8T28SOIDV_LL_-SDFSYNCPQX5_-P16**
CP to Q ↓	0.1756	0.2052	5.5815	6.2856
CP to Q ↑	0.2173	0.2557	7.1613	8.1726

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P0	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P4	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P10	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P16
CP ↓	min_pulse_width to CP	0.1274	0.1484	0.1871	0.2206
CP ↑	min_pulse_width to CP	0.0673	0.0766	0.0904	0.1044
D ↓	hold_rising to CP	-0.0294	-0.0365	-0.0522	-0.0610
D ↑	hold_rising to CP	-0.0098	-0.0147	-0.0191	-0.0267
D ↓	setup_rising to CP	0.0689	0.0808	0.1004	0.1208
D ↑	setup_rising to CP	0.0337	0.0395	0.0465	0.0514
TE ↓	hold_rising to CP	-0.0322	-0.0387	-0.0507	-0.0605
TE ↑	hold_rising to CP	-0.0342	-0.0387	-0.0511	-0.0608

TE ↓	setup_rising to CP	0.0712	0.0831	0.1031	0.1203
TE ↑	setup_rising to CP	0.1714	0.2007	0.2521	0.2957
TI ↓	hold_rising to CP	-0.1332	-0.1573	-0.2020	-0.2419
TI ↑	hold_rising to CP	-0.0361	-0.0426	-0.0537	-0.0635
TI ↓	setup_rising to CP	0.1712	0.2018	0.2516	0.2970
TI ↑	setup_rising to CP	0.0619	0.0723	0.0833	0.0946
		C8T28SOIDV_-LL_SDF-SYNCPQX5_P0	C8T28SOIDV_-LL_SDF-SYNCPQX5_P4	C8T28SOIDV_-LL_SDF-SYNCPQX5_P10	C8T28SOIDV_-LL_SDF-SYNCPQX5_P16
CP ↓	min_pulse_width to CP	0.2202	0.2625	0.3268	0.3919
CP ↑	min_pulse_width to CP	0.1014	0.1154	0.1374	0.1608
D ↓	hold_rising to CP	-0.0609	-0.0761	-0.0974	-0.1169
D ↑	hold_rising to CP	-0.0511	-0.0608	-0.0728	-0.0853
D ↓	setup_rising to CP	0.1257	0.1447	0.1789	0.2103
D ↑	setup_rising to CP	0.0834	0.0909	0.1054	0.1206
TE ↓	hold_rising to CP	-0.0560	-0.0707	-0.0903	-0.1094
TE ↑	hold_rising to CP	-0.0830	-0.0928	-0.1145	-0.1341
TE ↓	setup_rising to CP	0.1178	0.1395	0.1742	0.2055
TE ↑	setup_rising to CP	0.2137	0.2544	0.3184	0.3796
TI ↓	hold_rising to CP	-0.1416	-0.1758	-0.2267	-0.2704
TI ↑	hold_rising to CP	-0.0852	-0.0963	-0.1158	-0.1354
TI ↓	setup_rising to CP	0.2105	0.2493	0.3094	0.3696
TI ↑	setup_rising to CP	0.1198	0.1311	0.1505	0.1716

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL1_SDFSYNCPQX5_-P0	3.560e-04	1.000e-20
C8T28SOIDV_LL1_SDFSYNCPQX5_-P4	1.293e-04	1.000e-20
C8T28SOIDV_LL1_SDFSYNCPQX5_-P10	4.231e-05	1.000e-20
C8T28SOIDV_LL1_SDFSYNCPQX5_-P16	1.992e-05	1.000e-20
C8T28SOIDV_LL_SDFSYNCPQX5_-P0	3.554e-04	1.000e-20
C8T28SOIDV_LL_SDFSYNCPQX5_-P4	1.282e-04	1.000e-20
C8T28SOIDV_LL_SDFSYNCPQX5_-P10	4.165e-05	1.000e-20

C8T28SOIDV_LL_SDFSYNCPQX5_-P16	1.951e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

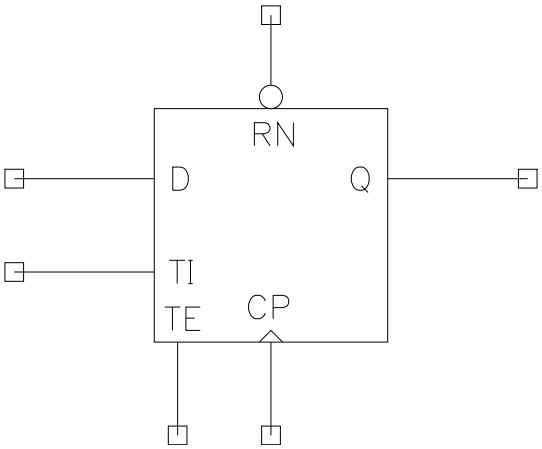
Pin Cycle	C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	C8T28SOIDV_LL1_-SDFSYNCPQX5_P4	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16
Clock 100Mhz Data 0Mhz	1.062e-02	1.074e-02	1.098e-02	1.126e-02
Clock 100Mhz Data 25Mhz	1.117e-02	1.121e-02	1.139e-02	1.169e-02
Clock 100Mhz Data 50Mhz	1.172e-02	1.167e-02	1.180e-02	1.213e-02
Clock = 0 Data 100Mhz	6.369e-03	6.324e-03	6.346e-03	6.403e-03
Clock = 1 Data 100Mhz	5.775e-05	5.549e-05	5.389e-05	5.296e-05
	C8T28SOIDV_LL_-SDFSYNCPQX5_P0	C8T28SOIDV_LL_-SDFSYNCPQX5_P4	C8T28SOIDV_LL_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPQX5_-P16
Clock 100Mhz Data 0Mhz	1.119e-02	1.121e-02	1.133e-02	1.151e-02
Clock 100Mhz Data 25Mhz	1.231e-02	1.231e-02	1.245e-02	1.268e-02
Clock 100Mhz Data 50Mhz	1.343e-02	1.341e-02	1.356e-02	1.385e-02
Clock = 0 Data 100Mhz	7.146e-03	7.520e-03	7.728e-03	7.875e-03
Clock = 1 Data 100Mhz	4.697e-05	4.263e-05	3.937e-05	3.693e-05

SDFSYNCPRQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P0	1.600	3.944	6.3104
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P4	1.600	3.944	6.3104
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P10	1.600	3.944	6.3104
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P16	1.600	3.944	6.3104
C8T28SOIDV_LL_-SDFSYNCPRQX5_P0	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPRQX5_P4	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPRQX5_P10	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPRQX5_P16	1.600	4.080	6.5280

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI

-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16
CP	0.0006	0.0006	0.0007	0.0007
D	0.0008	0.0008	0.0009	0.0009
RN	0.0011	0.0012	0.0013	0.0013
TE	0.0007	0.0008	0.0008	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16
CP	0.0004	0.0004	0.0004	0.0004
D	0.0004	0.0004	0.0004	0.0005
RN	0.0018	0.0018	0.0019	0.0020
TE	0.0007	0.0008	0.0008	0.0009
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4**
CP to Q ↓	0.0923	0.1062	4.0220	4.4202
CP to Q ↑	0.1009	0.1157	5.3123	5.9933
RN to Q ↓	0.0922	0.1070	3.4454	3.7683
	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16**
CP to Q ↓	0.1278	0.1489	5.0172	5.5810
CP to Q ↑	0.1391	0.1621	7.0401	8.0238
RN to Q ↓	0.1305	0.1538	4.2283	4.6488
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4**
CP to Q ↓	0.1380	0.1583	4.3606	4.8384
CP to Q ↑	0.1635	0.1881	5.4128	6.1140
RN to Q ↓	0.0961	0.1114	3.4677	3.7963
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16**
CP to Q ↓	0.1905	0.2216	5.5641	6.2438
CP to Q ↑	0.2280	0.2680	7.1841	8.1894
RN to Q ↓	0.1358	0.1597	4.2600	4.6826

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P0	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P4	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P10	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P16
CP ↓	min_pulse_width to CP	0.1329	0.1571	0.1956	0.2325
CP ↑	min_pulse_width to CP	0.0767	0.0873	0.1046	0.1234
D ↓	hold_rising to CP	-0.0316	-0.0414	-0.0512	-0.0664
D ↑	hold_rising to CP	-0.0137	-0.0191	-0.0267	-0.0364
D ↓	setup_rising to CP	0.0738	0.0857	0.1056	0.1257
D ↑	setup_rising to CP	0.0444	0.0492	0.0567	0.0611
RN ↓	min_pulse_width to RN	0.1072	0.1218	0.1462	0.1707
RN ↑	recovery_rising to CP	0.0005	0.0031	0.0037	0.0004
RN ↑	removal_rising to CP	0.0043	0.0043	0.0048	0.0042
TE ↓	hold_rising to CP	-0.0338	-0.0409	-0.0507	-0.0627
TE ↑	hold_rising to CP	-0.0407	-0.0488	-0.0608	-0.0706
TE ↓	setup_rising to CP	0.0734	0.0885	0.1052	0.1252
TE ↑	setup_rising to CP	0.1763	0.2110	0.2598	0.3113
TI ↓	hold_rising to CP	-0.1332	-0.1625	-0.2029	-0.2417
TI ↑	hold_rising to CP	-0.0419	-0.0524	-0.0634	-0.0730
TI ↓	setup_rising to CP	0.1761	0.2067	0.2564	0.3010
TI ↑	setup_rising to CP	0.0759	0.0820	0.0973	0.1079
		C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P0	C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P4	C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P10	C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P16
CP ↓	min_pulse_width to CP	0.2003	0.2412	0.3016	0.3620
CP ↑	min_pulse_width to CP	0.1106	0.1280	0.1513	0.1782
D ↓	hold_rising to CP	-0.0419	-0.0517	-0.0686	-0.0833
D ↑	hold_rising to CP	-0.0413	-0.0511	-0.0608	-0.0729
D ↓	setup_rising to CP	0.1008	0.1175	0.1473	0.1734
D ↑	setup_rising to CP	0.0709	0.0784	0.0903	0.1027
RN ↓	min_pulse_width to RN	0.1099	0.1267	0.1538	0.1782
RN ↑	recovery_rising to CP	0.0027	0.0037	0.0004	-0.0049
RN ↑	removal_rising to CP	0.0020	0.0015	0.0047	0.0096
TE ↓	hold_rising to CP	-0.0365	-0.0463	-0.0615	-0.0784
TE ↑	hold_rising to CP	-0.0733	-0.0830	-0.1031	-0.1195

TE ↓	setup_rising to CP	0.0956	0.1160	0.1426	0.1664
TE ↑	setup_rising to CP	0.1860	0.2261	0.2820	0.3357
TI ↓	hold_rising to CP	-0.1228	-0.1478	-0.1882	-0.2273
TI ↑	hold_rising to CP	-0.0768	-0.0865	-0.1061	-0.1221
TI ↓	setup_rising to CP	0.1868	0.2207	0.2760	0.3253
TI ↑	setup_rising to CP	0.1100	0.1213	0.1372	0.1576

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P0	3.891e-04	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P4	1.412e-04	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P10	4.619e-05	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P16	2.175e-05	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P0	3.761e-04	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P4	1.362e-04	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P10	4.442e-05	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P16	2.086e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16
Clock 100Mhz Data 0Mhz	1.147e-02	1.163e-02	1.190e-02	1.221e-02
Clock 100Mhz Data 25Mhz	1.221e-02	1.224e-02	1.245e-02	1.275e-02
Clock 100Mhz Data 50Mhz	1.294e-02	1.285e-02	1.300e-02	1.330e-02
Clock = 0 Data 100Mhz	7.592e-03	7.506e-03	7.491e-03	7.528e-03
Clock = 1 Data 100Mhz	5.491e-05	5.307e-05	5.177e-05	5.110e-05
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16
Clock 100Mhz Data 0Mhz	1.211e-02	1.212e-02	1.225e-02	1.244e-02
Clock 100Mhz Data 25Mhz	1.327e-02	1.320e-02	1.331e-02	1.352e-02

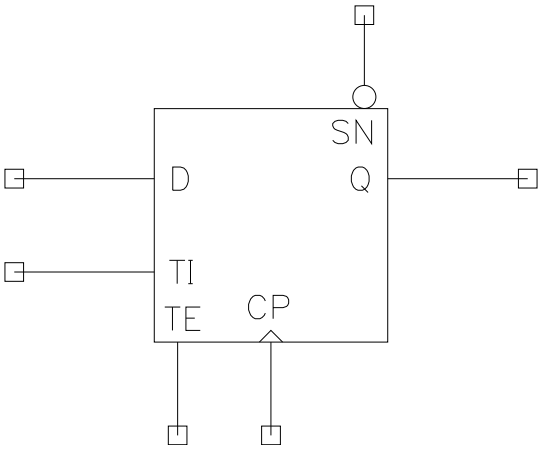
Clock 100Mhz Data 50Mhz	1.442e-02	1.428e-02	1.438e-02	1.461e-02
Clock = 0 Data 100Mhz	7.895e-03	8.050e-03	8.127e-03	8.187e-03
Clock = 1 Data 100Mhz	4.689e-05	4.378e-05	4.134e-05	3.944e-05

SDFSYNCPSQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P0	1.600	4.080	6.5280
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P4	1.600	4.080	6.5280
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P10	1.600	4.080	6.5280
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P16	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P0	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P4	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P10	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P16	1.600	4.080	6.5280

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI

-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16
CP	0.0005	0.0005	0.0006	0.0006
D	0.0006	0.0006	0.0006	0.0007
SN	0.0014	0.0014	0.0015	0.0015
TE	0.0008	0.0009	0.0009	0.0010
TI	0.0003	0.0003	0.0004	0.0004
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16
CP	0.0004	0.0004	0.0004	0.0004
D	0.0003	0.0003	0.0003	0.0003
SN	0.0013	0.0014	0.0014	0.0015
TE	0.0007	0.0008	0.0008	0.0009
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4**
CP to Q ↓	0.1020	0.1168	4.2491	4.6728
CP to Q ↑	0.1042	0.1193	5.3532	6.0399
SN to Q ↑	0.1139	0.1300	5.1235	5.7948
	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16**
CP to Q ↓	0.1395	0.1621	5.3012	5.8944
CP to Q ↑	0.1433	0.1661	7.0913	8.0851
SN to Q ↑	0.1558	0.1816	6.7995	7.7554
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4**
CP to Q ↓	0.1457	0.1672	4.5239	5.0313
CP to Q ↑	0.1684	0.1937	5.4517	6.1574
SN to Q ↑	0.0864	0.0990	5.2413	5.9186
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16**
CP to Q ↓	0.2005	0.2328	5.7700	6.4719
CP to Q ↑	0.2340	0.2741	7.2313	8.2421
SN to Q ↑	0.1343	0.1560	6.8164	7.7634

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P0	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P4	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P10	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P16
CP ↓	min_pulse_width to CP	0.1250	0.1461	0.1813	0.2159
CP ↑	min_pulse_width to CP	0.0828	0.0969	0.1142	0.1329
D ↓	hold_rising to CP	-0.0299	-0.0365	-0.0463	-0.0583
D ↑	hold_rising to CP	-0.0137	-0.0212	-0.0289	-0.0364
D ↓	setup_rising to CP	0.0689	0.0818	0.0955	0.1127
D ↑	setup_rising to CP	0.0444	0.0492	0.0563	0.0664
SN ↓	min_pulse_width to SN	0.1060	0.1206	0.1450	0.1694
SN ↑	recovery_rising to CP	-0.0088	-0.0062	-0.0115	-0.0105
SN ↑	removal_rising to CP	0.0346	0.0428	0.0472	0.0548
TE ↓	hold_rising to CP	-0.0289	-0.0360	-0.0491	-0.0615
TE ↑	hold_rising to CP	-0.0440	-0.0511	-0.0657	-0.0755
TE ↓	setup_rising to CP	0.0685	0.0782	0.0982	0.1155
TE ↑	setup_rising to CP	0.1714	0.2012	0.2478	0.2913
TI ↓	hold_rising to CP	-0.1270	-0.1527	-0.1931	-0.2329
TI ↑	hold_rising to CP	-0.0462	-0.0521	-0.0668	-0.0781
TI ↓	setup_rising to CP	0.1679	0.1972	0.2418	0.2830
TI ↑	setup_rising to CP	0.0759	0.0820	0.0973	0.1079
		C8T28SOIDV_-LL_SDFSYNCP-SQX5_P0	C8T28SOIDV_-LL_SDFSYNCP-SQX5_P4	C8T28SOIDV_-LL_SDFSYNCP-SQX5_P10	C8T28SOIDV_-LL_SDFSYNCP-SQX5_P16
CP ↓	min_pulse_width to CP	0.2074	0.2483	0.3111	0.3732
CP ↑	min_pulse_width to CP	0.1201	0.1375	0.1657	0.1890
D ↓	hold_rising to CP	-0.0468	-0.0566	-0.0735	-0.0882
D ↑	hold_rising to CP	-0.0407	-0.0510	-0.0631	-0.0761
D ↓	setup_rising to CP	0.1078	0.1278	0.1539	0.1815
D ↑	setup_rising to CP	0.0709	0.0806	0.0930	0.1076
SN ↓	min_pulse_width to SN	0.1147	0.1316	0.1587	0.1853
SN ↑	recovery_rising to CP	-0.0283	-0.0306	-0.0355	-0.0398
SN ↑	removal_rising to CP	0.0768	0.0866	0.1057	0.1231
TE ↓	hold_rising to CP	-0.0414	-0.0512	-0.0664	-0.0833
TE ↑	hold_rising to CP	-0.0723	-0.0879	-0.1048	-0.1244

TE ↓	setup_rising to CP	0.1036	0.1199	0.1497	0.1767
TE ↑	setup_rising to CP	0.1958	0.2354	0.2908	0.3503
TI ↓	hold_rising to CP	-0.1270	-0.1576	-0.1980	-0.2371
TI ↑	hold_rising to CP	-0.0803	-0.0914	-0.1074	-0.1270
TI ↓	setup_rising to CP	0.1966	0.2313	0.2866	0.3410
TI ↑	setup_rising to CP	0.1116	0.1210	0.1420	0.1618

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P0	3.832e-04	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P4	1.412e-04	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P10	4.689e-05	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P16	2.229e-05	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P0	3.732e-04	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P4	1.367e-04	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P10	4.506e-05	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P16	2.131e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16
Clock 100Mhz Data 0Mhz	1.066e-02	1.081e-02	1.106e-02	1.133e-02
Clock 100Mhz Data 25Mhz	1.177e-02	1.178e-02	1.194e-02	1.219e-02
Clock 100Mhz Data 50Mhz	1.288e-02	1.275e-02	1.283e-02	1.306e-02
Clock = 0 Data 100Mhz	7.179e-03	7.102e-03	7.097e-03	7.137e-03
Clock = 1 Data 100Mhz	5.832e-05	5.602e-05	5.431e-05	5.342e-05
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16
Clock 100Mhz Data 0Mhz	1.141e-02	1.154e-02	1.175e-02	1.200e-02
Clock 100Mhz Data 25Mhz	1.298e-02	1.300e-02	1.317e-02	1.342e-02

Clock 100Mhz Data 50Mhz	1.454e-02	1.446e-02	1.459e-02	1.485e-02
Clock = 0 Data 100Mhz	7.775e-03	8.085e-03	8.254e-03	8.377e-03
Clock = 1 Data 100Mhz	4.891e-05	4.546e-05	4.278e-05	4.070e-05

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