Central CAD
& Design Solutions

Electrical Rule Check (ERC) Description

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1. Introduction:

Calibre LVS techfile contains a set of ERC checks and connectivity softcheck rules managed by switches available in the customization file.

The following documentation describes each ERC and softchecks switches:

- ERC1_ST, ERC2_ST,ERC3_ST and ERC_SR_CONNECTION ERC rules ;
- psub, NWT3, TW and nbanb softcheck rules ;
- ERC1a, ERC3a, ERC3b, ERC10, ERC11, ERC12, ERC13, ERC_OPT1 optional ERC rules

2. Sign-off ERC rules:

ERC1_ST, ERC2_ST and ERC3_ST rules check Wells biasing + NWell / Deep NWell / PWell / P Substrate not connected to a node.

These rules can be turned OFF or ON thanks to the calibre variable RUN_ERC:
- If RUN_ERC is defined, these checks are performed (this is the default behaviour)
- If RUN_ERC is not defined, these checks are not performed.

ERC1_ST :
Checks floating Pwells. PWELL or substrate that contains MOS and/or CAP devices not physically connected with(RX and BP) junction (=ptap).
Example:

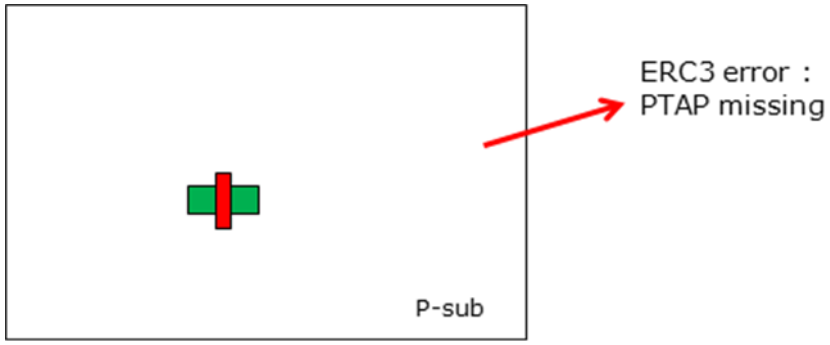

Fig1: ERC1_ST example

ERC2_ST :
Checks floating nwells. floating NWELL: NWELL not physically connected with (RX not BP) junction (=ntap)

Example:

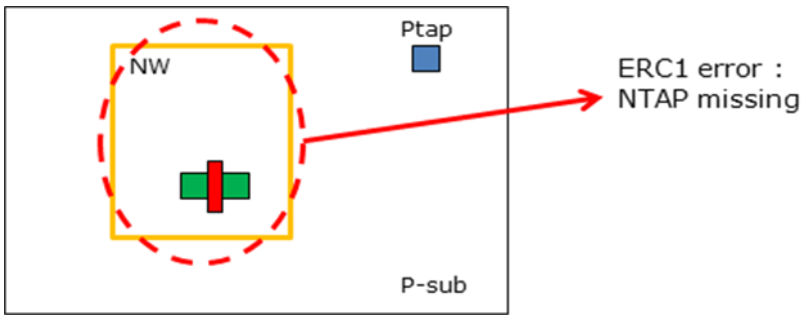

Fig2: ERC2_ST example

ERC3_ST:
Checks floating Deep NWELL (T3) : Deep NWELL(= T3) not connected to any (NWELL connected with RX not BP junction (=ntap))

ERC_SR_CONNECTION:
Highlights sealring connected by metal to internal chip and that is not connected to a ground net. Sealring is globally connected to substrate, so must either be floating, or connected to same voltage as substrate, so to a 'ground' label. This is similar to the rule ERC6, except that the sealring can be left floating (no connection by metal to internal chip).

3. sign-off softcheck rules:

psub_contact rule:
checks substrate connected to several (RX and BP) junctions (= ptap)

Example:

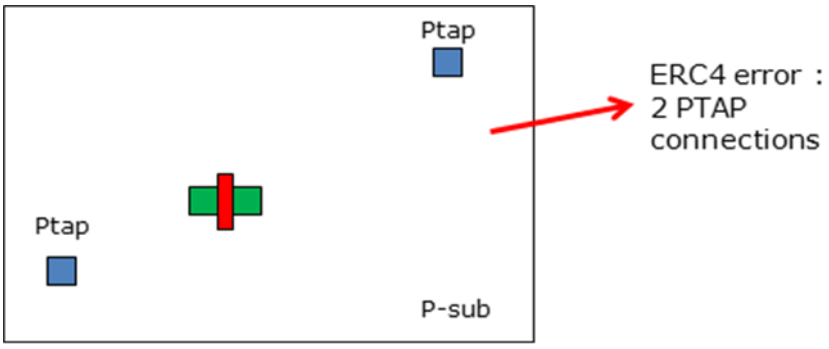

Fig3: psub_contact example

To avoid this error, two solutions:

- The first one is to have only one ptap to connect the substrate (=> delete one unconnected ptap).
- The second one is to connect all the ptap together:

Example:

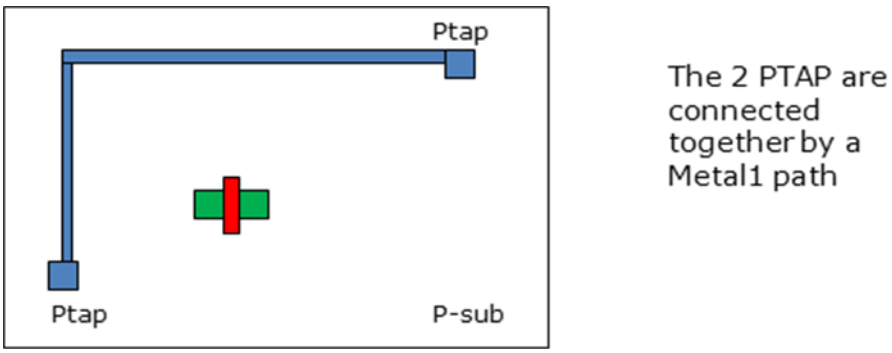

Fig4: psub_contact - Good case configiration example

TW_contact rule :
checks TW regions (PWELL isolated by NWELL ring and covered by T3) connected to several (RX and BP) junctions (= ptap)

same as psub_contact rule, but applicated to TW regions (=isolated Pwell)

NWT3_contact rule :
checks NWELL regions connected to several (RX not BP) junctions (= ntap)

same as psub_contact rule, but applicated to NW regions (=Nwell)

nband_contact rule :
checks T3 regions (=Deep-Nwell) connected to several (RX not BP) junctions (= ntap)through Nwells.

same as psub_contact rule, but applicated to TW regions (=isolated Pwell)

4. Optional ERC rules:

ERC1a, ERC3a, ERC3b, ERC10, ERC11, ERC12, ERC13, ERC_OPT1 are optional ERC rules, recommended for best design practice.

These rules can be turned OFF or ON thanks to the calibre variable OPTIONAL_ERC:

- If OPTIONAL_ERC is defined, these checks are performed (this is the default behaviour under cadence)
- If OPTIONAL_ERC is not defined, these checks are not performed. (this is the default behaviour for sign-off checks)

ERC_OPT1 :
Checks soft connections through RX. So it highlights when RX is used as a connection path
Checks soft connections through PO. So it highlights when poly is used as a connection path.
For best design performances, you should only use metal to correctly propagate signals.

ERC1a, ERC3a and ERC3b :
All Substrate Regions not identified as controlled, should be tied to GND or most negative chip supply (GND).
No PSUB region should be tied to a define PWR or NPWR.

Substrate region covers the whole chip. You should not apply forward or back body biasing at this level.
Note you have to enter top level power names in customization interface :

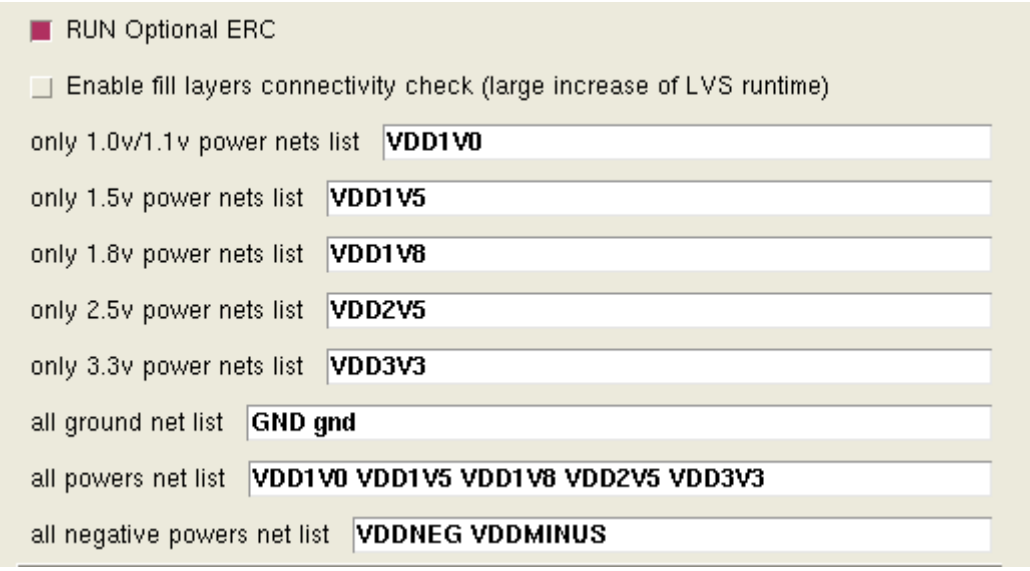

Fig5: power names for ERC optional checks

ERC10, ERC11, ERC12 and ERC13 :

Anode of pdiode in a nwell connected to VDD cannot have a path to a higher VDD
that would mean the diode is not connected in reverse mode but in direct mode ; which is not an usual configuration.

ERC_PWTW_DIODE

All T3 layer should be covered by LVS1;drawing8 marker for checking the diodepwtw/diodenwx/diodetwx connection. The layer LVS1;drawing8 purpose is to allow identification of the well to substrates diodes at LVS stage, and to compare them with respect to schematic. If no LVS1;drawing8 is used, these well to substrates diodes are extracted in PLS level ; so a post-layout simulation must be performed to validate your circuit behaviour.

5. Configuration example:

Next figures illustrate an example of a standard configuration correctly connected to substrate.

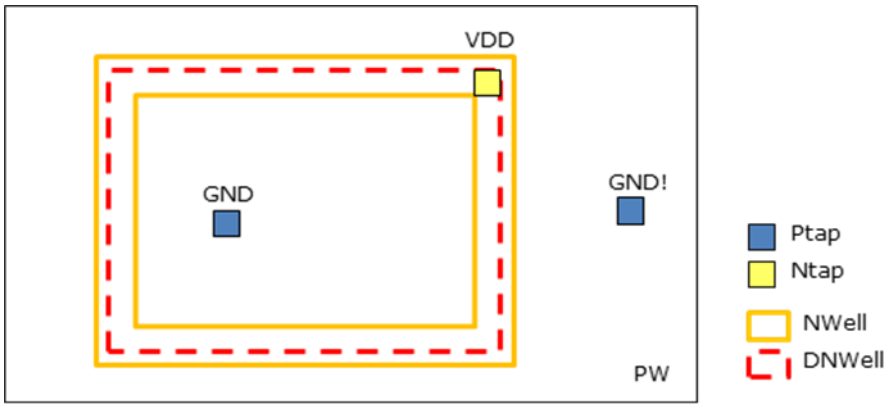

Fig9: Configuration top view

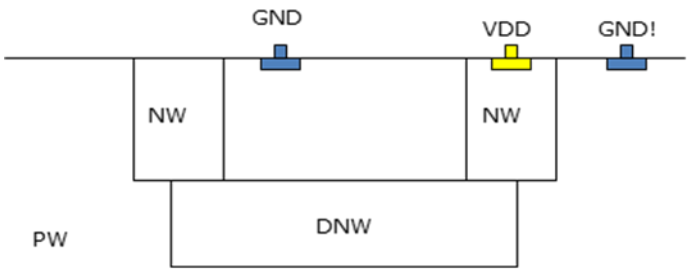

Fig10: Configuration Cross-section

6. ERC rules specific to devices:

Some devices have been developed with specific ERC rules to check their correct construct. This is the case of the **tline_flex** device.

For each metal level (M1, M2, M3, M4, M5, M6, {B1, B2}, IA, IB, LB), the rule 'ERC_TLINE_FLEX_{metal level}' forbids the presence of the corresponding metal over the transmission line.