

12 track Standard Cell Library comprising commonly used booleans and sequential cells

## 1 Release Notes

### 1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library name	C28SOI_SC_12_CORE_LR
Library version	5.1
Library type	Standard Cells
Technology	CMOS028_FDSOI

### 1.2 Related Documentation

- [StandardCell\\_Notes.pdf](#) Present in Design Package
- [User Manual](#) C28SOI\_SC\_12\_CORE\_LR\_um.pdf present in doc directory of Product itself.
- [Datasheets](#) C28SOI\_SC\_12\_CORE\_LR\_\*\_ds.pdf present in doc directory of Product itself.

## 2 Release Details

### 2.1 Current Release Details, Version 5.1

- Dummy Poly in layout across various cells has been cut for DFM robustness.
- Verilog Model for below cells have been updated to enable proper checking of E-CP timing checks

C12T28SOI_LR_DFPHQNX17_P0	C12T28SOI_LR_DFPHQNX33_P0
C12T28SOI_LR_DFPHQNX8_P0	C12T28SOI_LR_DFPHQX17_P0
C12T28SOI_LR_DFPHQX33_P0	C12T28SOI_LR_DFPHQX8_P0
C12T28SOI_LR_SDFPHRQNX17_P0	C12T28SOI_LR_SDFPHRQNX33_P0
C12T28SOI_LRHF_SDFPHRQNX4_P0	C12T28SOI_LR_SDFPHRQNX8_P0
C12T28SOI_LR_SDFPHRQX17_P0	C12T28SOI_LR_SDFPHRQX33_P0
C12T28SOI_LRHF_SDFPHRQX4_P0	C12T28SOI_LR_SDFPHRQX8_P0

- Verilog Model for Combinational cells has been updated to enable simulation of ring oscillators and other combinatorial loop in non-timing mode i.e. without sdf timing.
- Total 48 cells have been updated for Robustness relative to contact punch through effect. Minimum Enclosure of 20nm for RX/CA has been ensured. There is no change in Cell Area and Abstract because of contact robustness update.
  - Updated cells are-

C12T28SOI_LR_AND2X25_P0	C12T28SOI_LR_AND3X25_P0
C12T28SOI_LR_AND4X27_P0	C12T28SOI_LR_AND4X4_P0
C12T28SOI_LR_AOI11X8_P0	C12T28SOI_LR_AOI13X38_P0
C12T28SOI_LR_AOI211X17_P0	C12T28SOI_LR_BFX29_P0
C12T28SOI_LR_BFX33_P0	C12T28SOI_LRBR0P6_NAND3X12_P0
C12T28SOI_LR_CB4I1X17_P0	C12T28SOI_LR_DFPQNX30_P0
C12T28SOI_LR_DFPQX17_P0	C12T28SOI_LR_DFPQX30_P0
C12T28SOI_LR_DFPQX33_P0	C12T28SOI_LR_DFPRQNX17_P0
C12T28SOI_LR_DFPRQNX30_P0	C12T28SOI_LR_DFPRQX17_P0
C12T28SOI_LR_DFPRQX30_P0	C12T28SOI_LR_DFPSQX30_P0
C12T28SOI_LRHF_SDFPRQX4_P0	C12T28SOI_LR_IVX4_P0
C12T28SOI_LR_MUX21X8_P0	C12T28SOI_LR_MUX41X8_P0
C12T28SOI_LR_MUXI21X5_P0	C12T28SOI_LR_MX41X27_P0
C12T28SOI_LR_MX41X7_P0	C12T28SOI_LR_NAND2X50_P0
C12T28SOI_LR_NAND3AX24_P0	C12T28SOI_LR_NOR2X3_P0
C12T28SOI_LR_NOR4ABX13_P0	C12T28SOI_LR_NOR4X32_P0
C12T28SOI_LR_OAI112X10_P0	C12T28SOI_LR_OAI112X21_P0
C12T28SOI_LR_OAI211X10_P0	C12T28SOI_LR_OAI211X21_P0
C12T28SOI_LR_OAI222X9_P0	C12T28SOI_LR_OAI22X10_P0
C12T28SOI_LR_OAI22X15_P0	C12T28SOI_LR_OR2ABX16_P0
C12T28SOI_LR_OR2ABX24_P0	C12T28SOI_LR_OR2X8_P0
C12T28SOI_LRS1_FA1X8_P0	C12T28SOI_LR_SDFPRQNTX17_P0
C12T28SOI_LR_SDFPRQNTX33_P0	C12T28SOI_LR_SDFPRQNTX8_P0
C12T28SOI_LR_SDFPRQTX17_P0	C12T28SOI_LRS_NOR2X34_P0

- To enable support for Cadence Voltus Flow, CCS-Power has been added.

- Cells has been characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.
- The product has been aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Global Updates and Features related to Standard Cell Library, Refer to StandardCell\_Notes.pdf Present in Design Package.

## 2.2 Version 4.0

- Total 37 cells have been added to further enrich the offer.
  - Cells addition for better drive granularity.

C12T28SOI_LR_BFX13_P0	C12T28SOI_LR_BFX21_P0
C12T28SOI_LR_BFX29_P0	C12T28SOI_LR_BFX58_P0
C12T28SOI_LR_BFX6_P0	C12T28SOI_LR_BFX75_P0
C12T28SOI_LR_BFX84_P0	C12T28SOI_LR_IVX13_P0
C12T28SOI_LR_IVX21_P0	C12T28SOI_LR_IVX29_P0
C12T28SOI_LR_IVX75_P0	C12T28SOI_LR_IVX84_P0
C12T28SOI_LR_NAND2X10_P0	C12T28SOI_LR_NAND2X17_P0
C12T28SOI_LR_NAND2X24_P0	C12T28SOI_LR_NAND2X47_P0
C12T28SOI_LR_NAND2X58_P0	C12T28SOI_LR_NAND2X5_P0
C12T28SOI_LR_NAND2X67_P0	C12T28SOI_LR_NAND3X15_P0
C12T28SOI_LR_NAND3X21_P0	C12T28SOI_LR_NAND3X4_P0
C12T28SOI_LR_NAND3X9_P0	C12T28SOI_LR_NOR2X10_P0
C12T28SOI_LR_NOR2X17_P0	C12T28SOI_LR_NOR2X24_P0
C12T28SOI_LR_NOR2X5_P0	C12T28SOI_LR_NOR3X16_P0
C12T28SOI_LR_NOR3X22_P0	C12T28SOI_LR_NOR3X4_P0
C12T28SOI_LR_NOR3X9_P0	

- Addition of new functionality: Set-Reset Flip Flops

C12T28SOI_LR_SDFPRSQNTX17_P0	C12T28SOI_LR_SDFPRSQNTX33_P0
C12T28SOI_LR_SDFPRSQNTX8_P0	C12T28SOI_LR_SDFPRSQTX17_P0
C12T28SOI_LR_SDFPRSQTX33_P0	C12T28SOI_LR_SDFPRSQTX8_P0

- The product is aligned to DP28FDSOI 2.4 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell\_Notes.pdf Present in Design Package

## 2.3 Version 3.0

- Cells have been updated to have better design manufacturability, but for few cells, there is change in Abstract and Cell Area. Details are as below -
  - Cells with Change in Abstract ( 66 cells )

C12T28SOI_LRBR0P6_NAND3X35_P0	C12T28SOI_LR_DFPQNX17_P0
C12T28SOI_LR_DFPQX33_P0	C12T28SOI_LRHF_SDFPHRQNX4_P0
C12T28SOI_LRHF_SDFPHRQX4_P0	C12T28SOI_LRHF_SDFPQNTX4_P0
C12T28SOI_LRHF_SDFPQNX4_P0	C12T28SOI_LRHF_SDFPQTX4_P0
C12T28SOI_LRHF_SDFPQX4_P0	C12T28SOI_LRHF_SDFPRQNTX4_P0
C12T28SOI_LRHF_SDFPRQNX4_P0	C12T28SOI_LRHF_SDFPRQTX4_P0
C12T28SOI_LRHF_SDFPRQX4_P0	C12T28SOI_LRHF_SDFPSQNTX4_P0
C12T28SOI_LRHF_SDFPSQNX4_P0	C12T28SOI_LRHF_SDFPSQTX4_P0
C12T28SOI_LRHF_SDFPSQX4_P0	C12T28SOI_LR_MUX21X8_P0
C12T28SOI_LR_MUXI21X21_P0	C12T28SOI_LR_NOR2X40_P0
C12T28SOI_LR_NOR3AX13_P0	C12T28SOI_LR_NOR3AX25_P0
C12T28SOI_LRS1_FA1X33_P0	C12T28SOI_LR_SDFPHRQNX17_P0
C12T28SOI_LR_SDFPHRQNX33_P0	C12T28SOI_LR_SDFPHRQNX8_P0
C12T28SOI_LR_SDFPHRQX17_P0	C12T28SOI_LR_SDFPHRQX33_P0
C12T28SOI_LR_SDFPHRQX8_P0	C12T28SOI_LR_SDFPQNTX17_P0
C12T28SOI_LR_SDFPQNTX33_P0	C12T28SOI_LR_SDFPQNTX8_P0
C12T28SOI_LR_SDFPQNX17_P0	C12T28SOI_LR_SDFPQNX33_P0
C12T28SOI_LR_SDFPQTX17_P0	C12T28SOI_LR_SDFPQTX33_P0
C12T28SOI_LR_SDFPQX17_P0	C12T28SOI_LR_SDFPQX33_P0
C12T28SOI_LR_SDFPQX8_P0	C12T28SOI_LR_SDFPRQNTX17_P0
C12T28SOI_LR_SDFPRQNTX33_P0	C12T28SOI_LR_SDFPRQNTX8_P0
C12T28SOI_LR_SDFPRQNX17_P0	C12T28SOI_LR_SDFPRQNX33_P0
C12T28SOI_LR_SDFPRQTX17_P0	C12T28SOI_LR_SDFPRQTX33_P0
C12T28SOI_LR_SDFPRQTX8_P0	C12T28SOI_LR_SDFPRQX17_P0
C12T28SOI_LR_SDFPRQX33_P0	C12T28SOI_LR_SDFPRQX8_P0
C12T28SOI_LR_SDFPSQNTX17_P0	C12T28SOI_LR_SDFPSQNTX33_P0
C12T28SOI_LR_SDFPSQNTX8_P0	C12T28SOI_LR_SDFPSQNX17_P0
C12T28SOI_LR_SDFPSQNX25_P0	C12T28SOI_LR_SDFPSQNX33_P0
C12T28SOI_LR_SDFPSQNX8_P0	C12T28SOI_LR_SDFPSQTX17_P0
C12T28SOI_LR_SDFPSQTX33_P0	C12T28SOI_LR_SDFPSQTX8_P0
C12T28SOI_LR_SDFPSQX17_P0	C12T28SOI_LR_SDFPSQX25_P0
C12T28SOI_LR_SDFPSQX33_P0	C12T28SOI_LR_SDFPSQX8_P0
C12T28SOI_LRS_XNOR3X4_P0	C12T28SOI_LRS_XOR3X4_P0

- Cells with Change in Area ( 1 cell )
  - C12T28SOI\_LR\_DFPQX33\_P0

- The product is aligned to DP28FDSOI 2.3 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell\_Notes.pdf Present in Design Package

## **2.4      Version 2.0**

- The Product is aligned to DP28FDSOI\_7ML 1.0. Refer to Design Package Documents for more details.
- For Standard Cell Library Specific Features, Refer to StandardCell\_Notes.pdf Present in Design Package.

## 3 Known Problems and Solutions

### 3.1 DP related Generic Problems

- For Generic Standard cell Library related problem for this DP, please refer to KPS section inside StandardCell\_Notes.pdf Present in Design Package.

### 3.2 Placement Restriction

➡ Specific Placement restriction due to Poly Landing pad

☞ Placement restriction has been modelled in CADENCE LEF - through “Symmetry property” and in SYNOPSYS FRAM - through “spacing\_label property” for the following cells:

- C12T28SOI\_LR\_IVX4\_P0
- C12T28SOI\_LR\_IVX6\_P0
- C12T28SOI\_LR\_IVX8\_P0



*As mentioned above, modelling the placement constraint is different between Synopsys and Cadence. Therefore Need to be careful, if You do P&R with Synopsys and then go inside Cadence, the placement created by ICC could be declared as invalid by Encounter tool.*

## 4 Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (<http://col2.cro.st.com/helpdesk>).

Non-ST users, please contact the respective Customer Support.



**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2016 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)