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C28SOI_SC_8_COREPBP16_LL Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 16 nm

Overview

- C28SOI_SC_8_COREPBP16_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

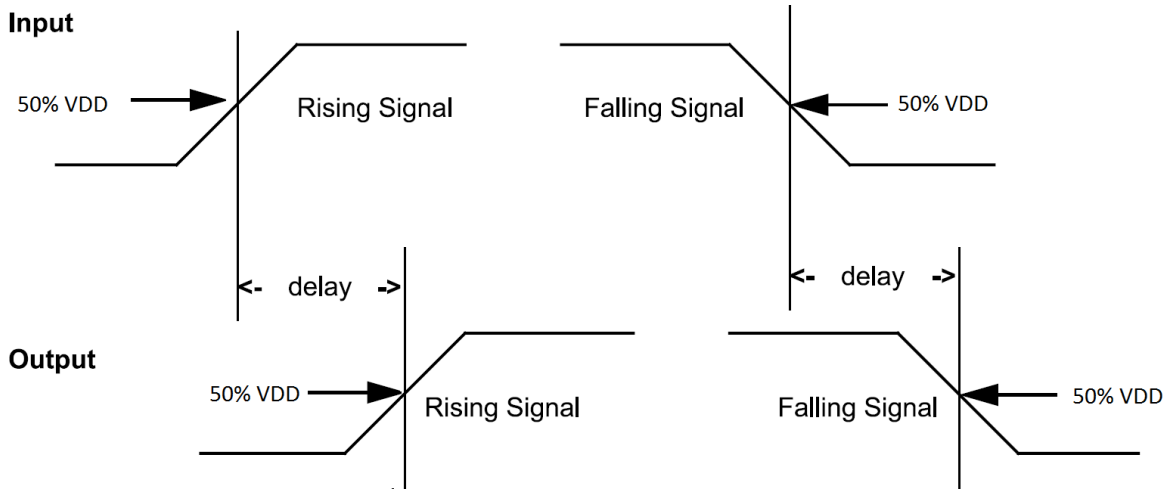


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

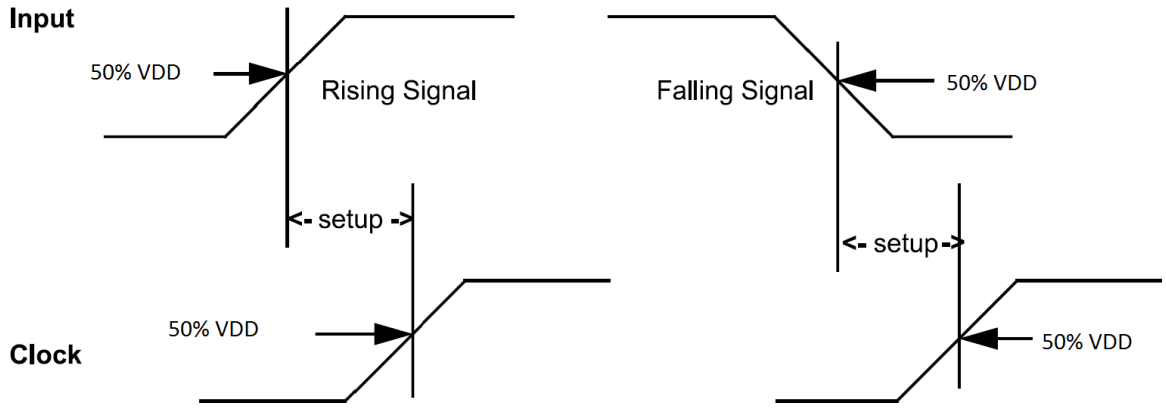


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

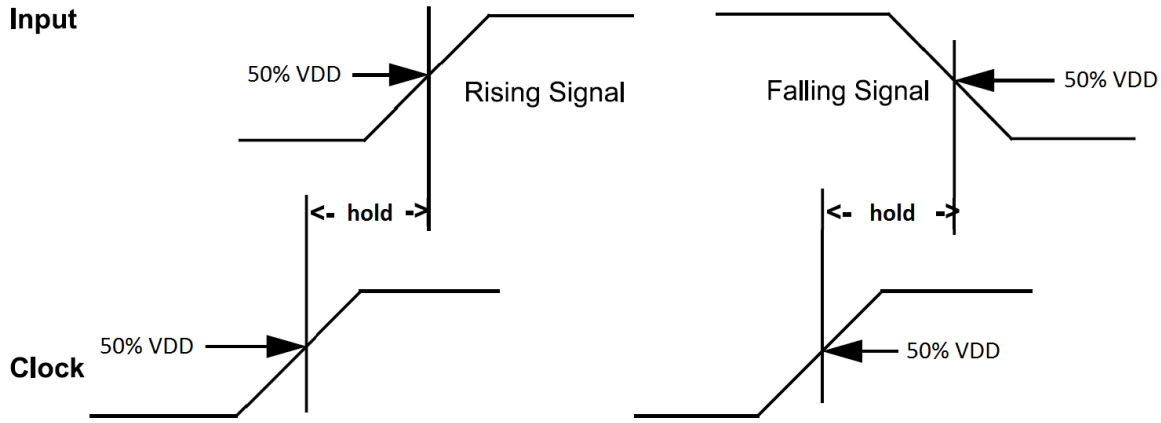


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

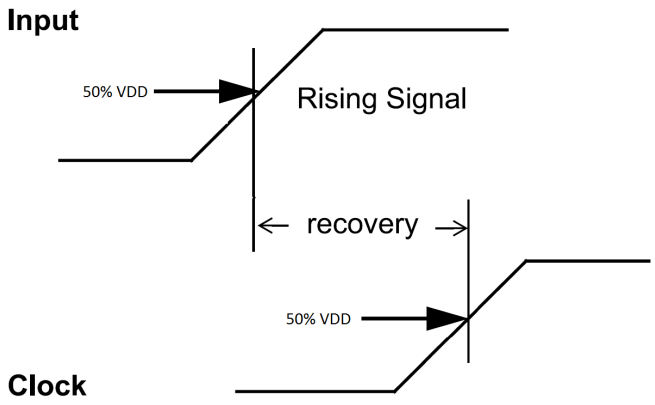


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

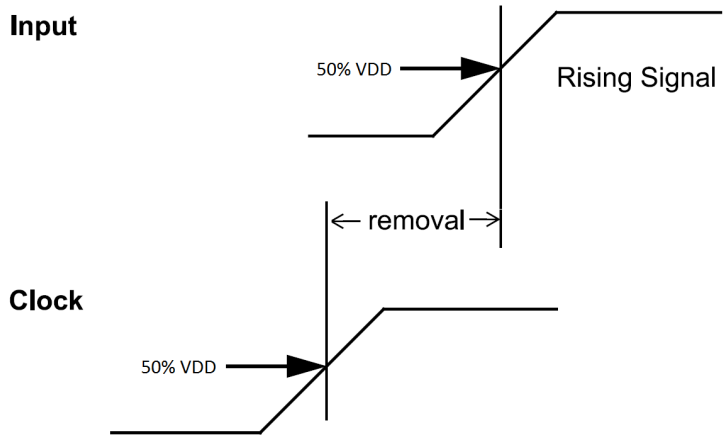


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

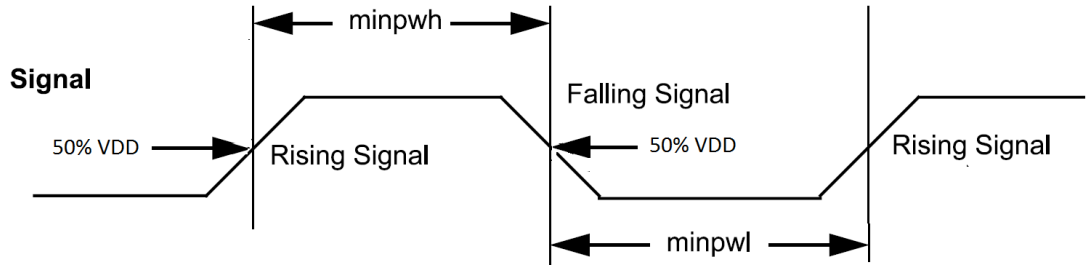


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

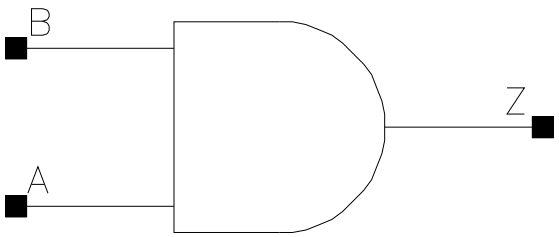
The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description	Logical Symbol
2 input AND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.544	0.4352
X10_P16	0.800	0.680	0.5440
X11_P16	1.600	0.544	0.8704
X19_P16	0.800	1.224	0.9792
X24_P16	0.800	1.360	1.0880
X29_P16	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X11_P16	X19_P16
A	0.0005	0.0007	0.0009	0.0014
B	0.0004	0.0007	0.0009	0.0013
	X24_P16	X29_P16		
A	0.0014	0.0014		
B	0.0012	0.0012		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0450	0.0358	4.9099	2.3337
A to Z ↑	0.0361	0.0324	8.1781	3.9147
B to Z ↓	0.0433	0.0335	4.9110	2.3340
B to Z ↑	0.0379	0.0337	8.1891	3.9151
	X11_P16	**X19_P16**	**X11_P16**	**X19_P16**

A to Z ↓	0.0392	0.0349	1.8118	1.2023
A to Z ↑	0.0306	0.0316	3.8111	1.9705
B to Z ↓	0.0364	0.0332	1.8085	1.2013
B to Z ↑	0.0320	0.0331	3.8101	1.9710
	X24_P16	**X29_P16**	**X24_P16**	**X29_P16**
A to Z ↓	0.0379	0.0400	0.9758	0.8150
A to Z ↑	0.0347	0.0367	1.5815	1.3150
B to Z ↓	0.0364	0.0387	0.9755	0.8151
B to Z ↑	0.0364	0.0386	1.5821	1.3148

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	2.117e-06	1.000e-20
X10_P16	4.538e-06	1.000e-20
X11_P16	5.314e-06	1.000e-20
X19_P16	8.663e-06	1.000e-20
X24_P16	9.996e-06	1.000e-20
X29_P16	1.133e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X11_P16	X19_P16
A (output stable)	4.741e-06	9.861e-06	1.307e-05	1.859e-05
B (output stable)	1.112e-05	2.076e-05	2.882e-05	4.246e-05
A to Z	1.232e-03	2.026e-03	2.505e-03	3.953e-03
B to Z	1.170e-03	1.912e-03	2.329e-03	3.715e-03
	X24_P16	X29_P16		
A (output stable)	1.866e-05	1.870e-05		
B (output stable)	4.234e-05	4.244e-05		
A to Z	4.832e-03	5.505e-03		
B to Z	4.595e-03	5.274e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

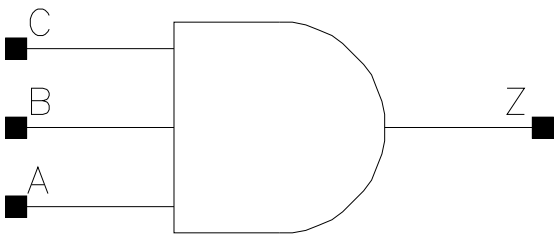
Pin Cycle (vdds)	X5_P16	X10_P16	X11_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P16	X29_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.680	0.5440
X10_P16	0.800	0.816	0.6528
X14_P16	0.800	1.360	1.0880
X19_P16	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0005	0.0007	0.0012	0.0014
B	0.0004	0.0006	0.0010	0.0013
C	0.0004	0.0007	0.0009	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0508	0.0402	4.9709	2.3532
A to Z ↑	0.0503	0.0441	8.2825	3.9610
B to Z ↓	0.0496	0.0381	4.9771	2.3501
B to Z ↑	0.0506	0.0441	8.2919	3.9611
C to Z ↓	0.0478	0.0364	4.9679	2.3468
C to Z ↑	0.0519	0.0446	8.2863	3.9603
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0405	0.0382	1.6209	1.2060

A to Z ↑	0.0430	0.0413	2.6819	1.9908
B to Z ↓	0.0386	0.0363	1.6198	1.2040
B to Z ↑	0.0430	0.0416	2.6821	1.9905
C to Z ↓	0.0369	0.0343	1.6184	1.2035
C to Z ↑	0.0439	0.0419	2.6824	1.9905

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	1.918e-06	1.000e-20
X10_P16	4.174e-06	1.000e-20
X14_P16	5.885e-06	1.000e-20
X19_P16	8.092e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	5.748e-06	1.217e-05	1.582e-05	2.174e-05
B (output stable)	1.092e-05	2.378e-05	3.171e-05	4.670e-05
C (output stable)	2.823e-05	5.854e-05	8.153e-05	1.210e-04
A to Z	1.441e-03	2.373e-03	3.460e-03	4.502e-03
B to Z	1.377e-03	2.250e-03	3.274e-03	4.250e-03
C to Z	1.325e-03	2.136e-03	3.114e-03	4.007e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

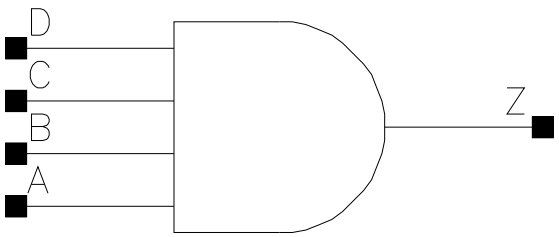
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.088	0.8704
X3_P16	0.800	1.088	0.8704
X10_P16	0.800	2.176	1.7408
X13_P16	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P16	X3_P16	X10_P16	X13_P16
A	0.0005	0.0005	0.0011	0.0012
B	0.0005	0.0004	0.0011	0.0012
C	0.0004	0.0004	0.0010	0.0012
D	0.0005	0.0005	0.0010	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	X3_P16	X2_P16	X3_P16
A to Z ↓	0.0395	0.0424	9.4175	6.0524
A to Z ↑	0.0424	0.0419	30.0825	15.3580
B to Z ↓	0.0372	0.0410	9.4158	6.0492
B to Z ↑	0.0439	0.0436	30.0874	15.3650
C to Z ↓	0.0403	0.0434	9.4256	6.0611
C to Z ↑	0.0415	0.0406	30.1140	15.3908

D to Z ↓	0.0385	0.0428	9.4151	6.0583
D to Z ↑	0.0436	0.0442	30.1303	15.3908
	X10_P16	**X13_P16**	**X10_P16**	**X13_P16**
A to Z ↓	0.0396	0.0394	2.0848	1.5473
A to Z ↑	0.0397	0.0426	5.0279	3.8523
B to Z ↓	0.0379	0.0361	2.0848	1.5461
B to Z ↑	0.0413	0.0425	5.0268	3.8565
C to Z ↓	0.0395	0.0372	2.0678	1.5539
C to Z ↑	0.0370	0.0357	5.0268	3.8529
D to Z ↓	0.0359	0.0340	2.0618	1.5510
D to Z ↑	0.0368	0.0356	5.0235	3.8527

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P16	1.895e-06	1.000e-20
X3_P16	2.437e-06	1.000e-20
X10_P16	7.135e-06	1.000e-20
X13_P16	9.750e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P16	X3_P16	X10_P16	X13_P16
A (output stable)	2.637e-04	3.212e-04	8.359e-04	1.147e-03
B (output stable)	2.419e-04	2.977e-04	7.726e-04	1.058e-03
C (output stable)	2.648e-04	2.946e-04	7.900e-04	9.970e-04
D (output stable)	2.437e-04	2.814e-04	7.206e-04	9.027e-04
A to Z	9.906e-04	1.331e-03	3.758e-03	5.108e-03
B to Z	9.299e-04	1.265e-03	3.589e-03	4.717e-03
C to Z	9.990e-04	1.279e-03	3.254e-03	4.030e-03
D to Z	9.428e-04	1.244e-03	2.926e-03	3.639e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

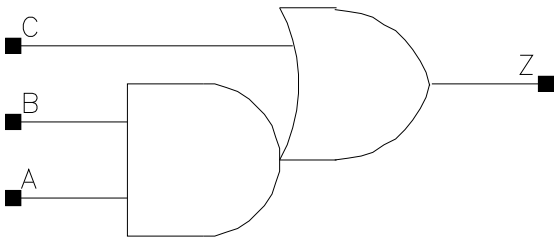
Pin Cycle (vdds)	X2_P16	X3_P16	X10_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	0.952	0.7616
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0004	0.0006	0.0012
B	0.0004	0.0006	0.0010
C	0.0005	0.0006	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0621	0.0526	4.7298	2.3638
A to Z ↑	0.0404	0.0354	7.6942	3.8882
B to Z ↓	0.0587	0.0496	4.7157	2.3554
B to Z ↑	0.0427	0.0376	7.6893	3.8903
C to Z ↓	0.0649	0.0528	4.6991	2.3522
C to Z ↑	0.0366	0.0321	7.6442	3.8611
	X19_P16		**X19_P16**	
A to Z ↓	0.0508		1.2278	
A to Z ↑	0.0390		1.9624	

B to Z ↓	0.0485		1.2275	
B to Z ↑	0.0412		1.9605	
C to Z ↓	0.0512		1.2239	
C to Z ↑	0.0345		1.9437	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	2.676e-06	1.000e-20
X10_P16	5.252e-06	1.000e-20
X19_P16	9.310e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	7.446e-06	1.623e-05	3.415e-05
B (output stable)	9.464e-06	2.011e-05	4.094e-05
C (output stable)	3.119e-05	4.121e-05	9.933e-05
A to Z	1.406e-03	2.280e-03	4.374e-03
B to Z	1.348e-03	2.171e-03	4.206e-03
C to Z	1.580e-03	2.494e-03	4.804e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

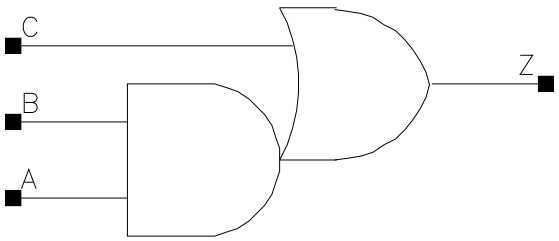
Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	0.952	0.7616
X14_P16	0.800	1.632	1.3056
X19_P16	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0004	0.0006	0.0012	0.0012
B	0.0004	0.0006	0.0012	0.0012
C	0.0005	0.0006	0.0013	0.0013

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0666	0.0567	4.7088	2.3884
A to Z ↑	0.0438	0.0394	7.8077	3.9127
B to Z ↓	0.0643	0.0541	4.6971	2.3839
B to Z ↑	0.0470	0.0415	7.7935	3.9103
C to Z ↓	0.0563	0.0489	4.6731	2.3739
C to Z ↑	0.0322	0.0284	7.7110	3.8701
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0509	0.0546	1.6149	1.2189

A to Z ↑	0.0360	0.0380	2.6474	1.9785
B to Z ↓	0.0462	0.0500	1.6089	1.2142
B to Z ↑	0.0366	0.0388	2.6431	1.9750
C to Z ↓	0.0404	0.0443	1.6046	1.2099
C to Z ↑	0.0249	0.0264	2.6175	1.9554

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	2.682e-06	1.000e-20
X10_P16	4.931e-06	1.000e-20
X14_P16	8.882e-06	1.000e-20
X19_P16	1.019e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	7.592e-06	9.958e-06	3.347e-05	3.352e-05
B (output stable)	1.019e-05	1.301e-05	7.179e-05	7.169e-05
C (output stable)	4.881e-05	8.349e-05	2.067e-04	2.070e-04
A to Z	1.583e-03	2.428e-03	4.332e-03	5.049e-03
B to Z	1.532e-03	2.318e-03	3.940e-03	4.655e-03
C to Z	1.310e-03	2.028e-03	3.283e-03	3.977e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

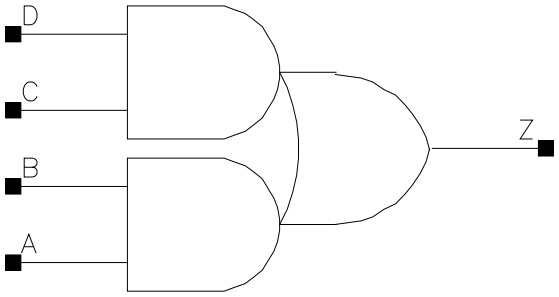
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.088	0.8704
X10_P16	0.800	1.088	0.8704
X14_P16	0.800	1.768	1.4144
X19_P16	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0005	0.0006	0.0013	0.0013
B	0.0005	0.0008	0.0011	0.0011
C	0.0004	0.0006	0.0013	0.0013
D	0.0005	0.0006	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0674	0.0557	4.7245	2.3682
A to Z ↑	0.0460	0.0414	7.8355	3.8921
B to Z ↓	0.0622	0.0511	4.6938	2.3571

B to Z ↑	0.0463	0.0420	7.8380	3.8889
C to Z ↓	0.0590	0.0494	4.7012	2.3600
C to Z ↑	0.0387	0.0344	7.8179	3.8795
D to Z ↓	0.0566	0.0470	4.6900	2.3539
D to Z ↑	0.0414	0.0365	7.8184	3.8850
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0501	0.0538	1.6149	1.2222
A to Z ↑	0.0366	0.0389	2.6534	1.9869
B to Z ↓	0.0469	0.0508	1.6127	1.2203
B to Z ↑	0.0385	0.0409	2.6507	1.9857
C to Z ↓	0.0445	0.0485	1.6106	1.2190
C to Z ↑	0.0314	0.0339	2.6415	1.9790
D to Z ↓	0.0416	0.0456	1.6089	1.2168
D to Z ↑	0.0329	0.0355	2.6422	1.9798

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	2.959e-06	1.000e-20
X10_P16	5.691e-06	1.000e-20
X14_P16	9.361e-06	1.000e-20
X19_P16	1.068e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	1.740e-05	2.351e-05	2.912e-05	2.922e-05
B (output stable)	9.291e-05	9.580e-05	4.058e-05	4.079e-05
C (output stable)	1.509e-05	2.168e-05	4.657e-05	4.681e-05
D (output stable)	1.806e-05	2.906e-05	6.121e-05	6.145e-05
A to Z	1.827e-03	2.769e-03	4.489e-03	5.279e-03
B to Z	1.652e-03	2.500e-03	4.217e-03	5.006e-03
C to Z	1.511e-03	2.293e-03	3.649e-03	4.444e-03
D to Z	1.444e-03	2.184e-03	3.415e-03	4.194e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

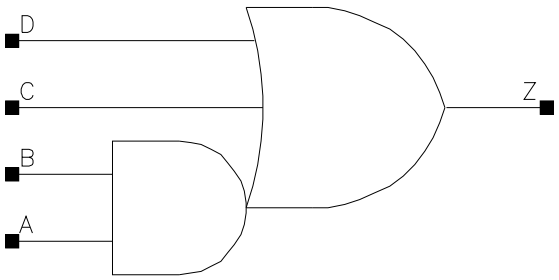
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	1.088	0.8704
X19_P16	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0004	0.0006	0.0011
B	0.0004	0.0006	0.0011
C	0.0005	0.0006	0.0012
D	0.0004	0.0006	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0782	0.0640	5.3099	2.4765
A to Z ↑	0.0418	0.0347	8.1623	3.8979
B to Z ↓	0.0753	0.0598	5.2961	2.4669
B to Z ↑	0.0444	0.0368	8.1648	3.9027
C to Z ↓	0.0852	0.0702	5.2853	2.4661
C to Z ↑	0.0369	0.0449	8.1068	3.9114

D to Z ↓	0.0834	0.0698	5.2864	2.4673
D to Z ↑	0.0368	0.0446	8.1010	3.9071
	X19_P16		**X19_P16**	
A to Z ↓	0.0623		1.2807	
A to Z ↑	0.0376		1.9469	
B to Z ↓	0.0563		1.2734	
B to Z ↑	0.0381		1.9442	
C to Z ↓	0.0667		1.2752	
C to Z ↑	0.0364		1.9368	
D to Z ↓	0.0649		1.2750	
D to Z ↑	0.0358		1.9344	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	2.267e-06	1.000e-20
X10_P16	4.781e-06	1.000e-20
X19_P16	8.747e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	1.042e-05	1.750e-05	4.106e-05
B (output stable)	1.114e-05	1.888e-05	5.871e-05
C (output stable)	1.356e-05	2.586e-05	5.441e-05
D (output stable)	1.107e-05	2.354e-05	4.446e-05
A to Z	1.481e-03	2.401e-03	4.607e-03
B to Z	1.428e-03	2.280e-03	4.221e-03
C to Z	1.700e-03	2.860e-03	5.334e-03
D to Z	1.612e-03	2.707e-03	4.982e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

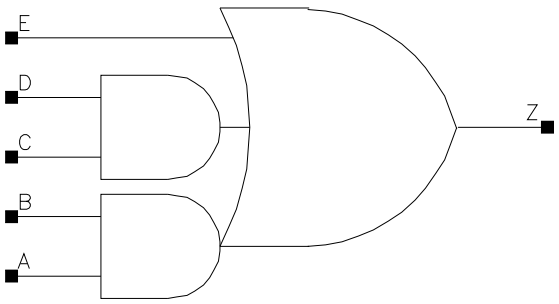
Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.088	0.8704
X10_P16	0.800	1.224	0.9792
X19_P16	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0004	0.0006	0.0012
B	0.0004	0.0006	0.0010
C	0.0004	0.0008	0.0012
D	0.0004	0.0006	0.0010
E	0.0004	0.0006	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.1015	0.0776	5.0124	2.4591
A to Z ↑	0.0531	0.0434	7.9241	3.9254

B to Z ↓	0.1004	0.0743	4.9991	2.4538
B to Z ↑	0.0571	0.0457	7.9234	3.9257
C to Z ↓	0.0873	0.0665	4.9931	2.4498
C to Z ↑	0.0468	0.0369	7.8588	3.9001
D to Z ↓	0.0825	0.0607	4.9689	2.4399
D to Z ↑	0.0493	0.0385	7.8600	3.8978
E to Z ↓	0.0894	0.0678	4.9609	2.4402
E to Z ↑	0.0396	0.0328	7.7820	3.8733
	X19_P16		**X19_P16**	
A to Z ↓	0.0745		1.2680	
A to Z ↑	0.0452		1.9750	
B to Z ↓	0.0712		1.2664	
B to Z ↑	0.0477		1.9731	
C to Z ↓	0.0619		1.2628	
C to Z ↑	0.0373		1.9571	
D to Z ↓	0.0584		1.2600	
D to Z ↑	0.0395		1.9575	
E to Z ↓	0.0648		1.2590	
E to Z ↑	0.0409		1.9511	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	2.755e-06	1.000e-20
X10_P16	5.615e-06	1.000e-20
X19_P16	9.993e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	7.940e-06	1.411e-05	2.906e-05
B (output stable)	1.160e-05	1.618e-05	2.993e-05
C (output stable)	1.777e-05	2.265e-05	4.652e-05
D (output stable)	1.919e-05	2.688e-05	5.178e-05
E (output stable)	2.911e-05	5.485e-05	1.080e-04
A to Z	2.059e-03	3.157e-03	6.031e-03
B to Z	2.028e-03	3.031e-03	5.787e-03
C to Z	1.694e-03	2.517e-03	4.694e-03
D to Z	1.629e-03	2.371e-03	4.488e-03
E to Z	1.792e-03	2.715e-03	5.162e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

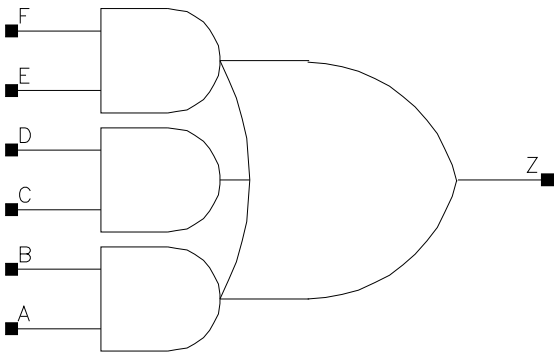
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.360	1.0880
X5_P16	0.800	1.360	1.0880
X10_P16	0.800	1.632	1.3056
X19_P16	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P16	X5_P16	X10_P16	X19_P16
A	0.0005	0.0005	0.0007	0.0012

B	0.0005	0.0005	0.0007	0.0010
C	0.0007	0.0007	0.0006	0.0011
D	0.0005	0.0005	0.0005	0.0010
E	0.0006	0.0006	0.0006	0.0012
F	0.0005	0.0005	0.0006	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X5_P16**	**X2_P16**	**X5_P16**
A to Z ↓	0.0753	0.0779	9.7174	5.0764
A to Z ↑	0.0518	0.0506	16.2014	8.2952
B to Z ↓	0.0723	0.0749	9.6848	5.0622
B to Z ↑	0.0548	0.0537	16.1981	8.2939
C to Z ↓	0.0697	0.0724	9.6991	5.0698
C to Z ↑	0.0482	0.0472	16.0496	8.2289
D to Z ↓	0.0642	0.0669	9.6739	5.0560
D to Z ↑	0.0497	0.0488	16.0422	8.2274
E to Z ↓	0.0566	0.0591	9.6559	5.0499
E to Z ↑	0.0399	0.0389	15.9510	8.1864
F to Z ↓	0.0520	0.0548	9.6338	5.0382
F to Z ↑	0.0413	0.0407	15.9570	8.1857
	X10_P16	**X19_P16**	**X10_P16**	**X19_P16**
A to Z ↓	0.0836	0.0770	2.4637	1.2668
A to Z ↑	0.0536	0.0487	3.9577	1.9827
B to Z ↓	0.0789	0.0741	2.4488	1.2645
B to Z ↑	0.0547	0.0512	3.9564	1.9817
C to Z ↓	0.0757	0.0708	2.4548	1.2645
C to Z ↑	0.0475	0.0448	3.9349	1.9694
D to Z ↓	0.0731	0.0682	2.4476	1.2625
D to Z ↑	0.0503	0.0474	3.9345	1.9682
E to Z ↓	0.0652	0.0626	2.4455	1.2607
E to Z ↑	0.0407	0.0389	3.9164	1.9616
F to Z ↓	0.0614	0.0588	2.4376	1.2575
F to Z ↑	0.0428	0.0410	3.9146	1.9616

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P16	2.849e-06	1.000e-20
X5_P16	3.636e-06	1.000e-20
X10_P16	6.017e-06	1.000e-20
X19_P16	1.120e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P16	X5_P16	X10_P16	X19_P16
A (output stable)	1.709e-05	1.707e-05	2.575e-05	3.881e-05
B (output stable)	1.839e-05	1.839e-05	6.650e-05	4.267e-05
C (output stable)	1.360e-05	1.361e-05	1.883e-05	3.204e-05
D (output stable)	1.730e-05	1.731e-05	2.318e-05	4.172e-05
E (output stable)	2.647e-05	2.658e-05	3.684e-05	5.860e-05
F (output stable)	3.023e-05	3.031e-05	3.996e-05	6.685e-05

A to Z	2.038e-03	2.316e-03	3.562e-03	6.501e-03
B to Z	1.960e-03	2.236e-03	3.334e-03	6.266e-03
C to Z	1.687e-03	1.962e-03	3.087e-03	5.676e-03
D to Z	1.586e-03	1.858e-03	2.990e-03	5.479e-03
E to Z	1.283e-03	1.550e-03	2.627e-03	4.923e-03
F to Z	1.202e-03	1.469e-03	2.519e-03	4.699e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

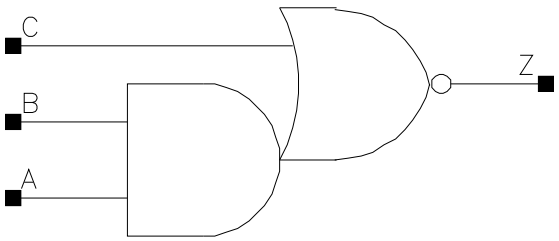
Pin Cycle (vdds)	X2_P16	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X10_P16	0.800	1.360	1.0880
X19_P16	0.800	2.584	2.0672
X25_P16	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P16	X10_P16	X19_P16	X25_P16
A	0.0006	0.0015	0.0030	0.0038
B	0.0005	0.0013	0.0027	0.0036
C	0.0006	0.0016	0.0029	0.0039

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X10_P16**	**X3_P16**	**X10_P16**
A to Z ↓	0.0131	0.0142	8.1434	2.9203
A to Z ↑	0.0236	0.0242	14.4919	4.9237
B to Z ↓	0.0137	0.0139	8.2003	2.9447
B to Z ↑	0.0197	0.0192	14.3454	4.9183
C to Z ↓	0.0138	0.0141	4.7106	1.6402
C to Z ↑	0.0253	0.0257	13.2276	4.5175
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0150	0.0147	1.4795	1.1260

A to Z ↑	0.0250	0.0245	2.5011	1.8666
B to Z ↓	0.0139	0.0140	1.4930	1.1354
B to Z ↑	0.0194	0.0194	2.5019	1.8815
C to Z ↓	0.0160	0.0162	1.0014	0.7735
C to Z ↑	0.0260	0.0259	2.2974	1.7202

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	2.101e-06	1.000e-20
X10_P16	5.673e-06	1.000e-20
X19_P16	1.077e-05	1.000e-20
X25_P16	1.412e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X10_P16	X19_P16	X25_P16
A (output stable)	1.695e-05	6.087e-05	1.250e-04	1.600e-04
B (output stable)	2.175e-05	1.026e-04	2.241e-04	2.828e-04
C (output stable)	4.369e-05	1.445e-04	2.822e-04	3.897e-04
A to Z	5.571e-04	1.770e-03	3.709e-03	4.794e-03
B to Z	4.454e-04	1.278e-03	2.606e-03	3.444e-03
C to Z	8.208e-04	2.469e-03	4.918e-03	6.564e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

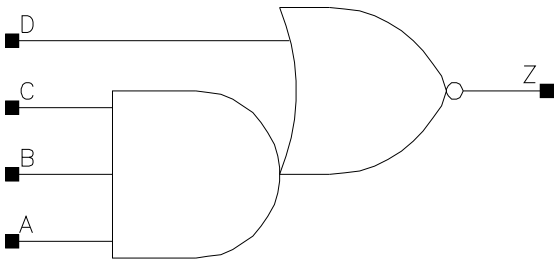
Pin Cycle (vdds)	X3_P16	X10_P16	X19_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X17_P16	0.800	3.536	2.8288
X22_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X17_P16	X22_P16
A	0.0005	0.0029	0.0039
B	0.0005	0.0028	0.0037
C	0.0006	0.0026	0.0035
D	0.0006	0.0031	0.0039

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X17_P16	X3_P16	X17_P16
A to Z ↓	0.0202	0.0216	11.6924	2.1729
A to Z ↑	0.0312	0.0303	14.4964	2.4382
B to Z ↓	0.0203	0.0209	11.7050	2.1769
B to Z ↑	0.0280	0.0269	14.5070	2.4626
C to Z ↓	0.0217	0.0190	11.7569	2.1839
C to Z ↑	0.0264	0.0220	14.5504	2.4734
D to Z ↓	0.0168	0.0186	4.5963	0.9882

D to Z ↑	0.0318	0.0298	12.3970	2.0961
	X22_P16		**X22_P16**	
A to Z ↓	0.0214		1.6463	
A to Z ↑	0.0299		1.8239	
B to Z ↓	0.0205		1.6504	
B to Z ↑	0.0264		1.8464	
C to Z ↓	0.0188		1.6560	
C to Z ↑	0.0217		1.8582	
D to Z ↓	0.0194		0.8203	
D to Z ↑	0.0290		1.5681	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	2.270e-06	1.000e-20
X17_P16	1.059e-05	1.000e-20
X22_P16	1.359e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X17_P16	X22_P16
A (output stable)	1.230e-05	8.990e-05	1.208e-04
B (output stable)	1.692e-05	1.578e-04	2.088e-04
C (output stable)	3.274e-05	3.458e-04	4.504e-04
D (output stable)	6.692e-05	4.109e-04	5.405e-04
A to Z	9.112e-04	5.298e-03	6.889e-03
B to Z	7.874e-04	4.311e-03	5.571e-03
C to Z	6.860e-04	3.255e-03	4.213e-03
D to Z	1.204e-03	6.497e-03	8.438e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

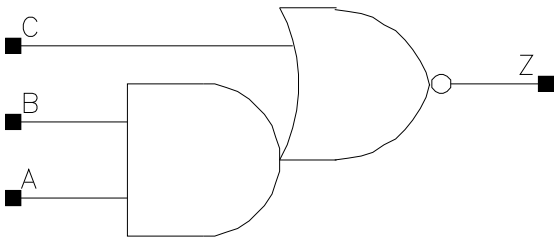
Pin Cycle (vdds)	X3_P16	X17_P16	X22_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X6_P16	0.800	1.088	0.8704
X9_P16	0.800	1.360	1.0880
X12_P16	0.800	1.904	1.5232
X25_P16	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X9_P16	X12_P16
A	0.0005	0.0011	0.0017	0.0022
B	0.0005	0.0011	0.0015	0.0020
C	0.0006	0.0009	0.0013	0.0018
	X25_P16			
A	0.0044			
B	0.0040			
C	0.0035			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0181	0.0178	10.9286	4.2550
A to Z ↑	0.0282	0.0299	16.6535	7.3325
B to Z ↓	0.0199	0.0174	10.9730	4.2819

B to Z ↑	0.0257	0.0252	16.5231	7.3501
C to Z ↓	0.0121	0.0105	6.3917	2.9922
C to Z ↑	0.0209	0.0189	15.3529	6.7820
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0170	0.0177	2.9244	2.1869
A to Z ↑	0.0281	0.0285	4.9040	3.6396
B to Z ↓	0.0172	0.0171	2.9430	2.2022
B to Z ↑	0.0234	0.0237	4.9061	3.6741
C to Z ↓	0.0105	0.0103	2.0545	1.5291
C to Z ↑	0.0180	0.0182	4.5408	3.3873
	X25_P16		**X25_P16**	
A to Z ↓	0.0174		1.1376	
A to Z ↑	0.0276		1.8387	
B to Z ↓	0.0171		1.1453	
B to Z ↑	0.0229		1.8455	
C to Z ↓	0.0101		0.7788	
C to Z ↑	0.0175		1.7082	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	1.640e-06	1.000e-20
X6_P16	3.977e-06	1.000e-20
X9_P16	5.448e-06	1.000e-20
X12_P16	7.432e-06	1.000e-20
X25_P16	1.428e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	1.003e-05	3.301e-05	4.368e-05	6.424e-05
B (output stable)	1.280e-05	7.117e-05	8.062e-05	1.375e-04
C (output stable)	7.787e-05	1.966e-04	2.723e-04	3.736e-04
A to Z	7.567e-04	1.894e-03	2.575e-03	3.572e-03
B to Z	6.696e-04	1.508e-03	2.024e-03	2.757e-03
C to Z	4.100e-04	8.798e-04	1.190e-03	1.656e-03
	X25_P16			
A (output stable)	1.205e-04			
B (output stable)	2.393e-04			
C (output stable)	7.199e-04			
A to Z	6.769e-03			
B to Z	5.277e-03			
C to Z	3.083e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

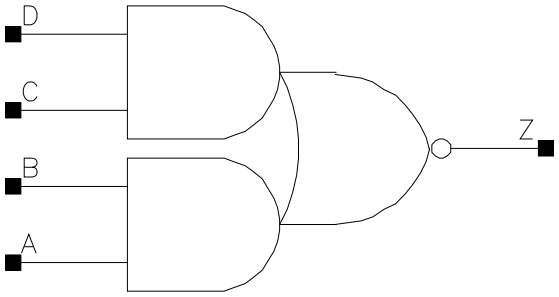
	X25_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.680	0.5440
X6_P16	0.800	1.224	0.9792
X9_P16	0.800	1.768	1.4144
X12_P16	0.800	2.448	1.9584
X24_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P16	X6_P16	X9_P16	X12_P16
A	0.0004	0.0012	0.0017	0.0022
B	0.0004	0.0010	0.0015	0.0021
C	0.0004	0.0012	0.0015	0.0020
D	0.0004	0.0009	0.0014	0.0018
	X24_P16			
A	0.0043			
B	0.0041			
C	0.0040			
D	0.0037			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X6_P16**	**X2_P16**	**X6_P16**
A to Z ↓	0.0181	0.0185	11.0962	4.1562
A to Z ↑	0.0357	0.0308	21.1934	6.6951
B to Z ↓	0.0197	0.0197	11.1463	4.1767
B to Z ↑	0.0320	0.0275	21.1715	6.7958
C to Z ↓	0.0133	0.0131	11.0907	4.1630
C to Z ↑	0.0268	0.0235	21.2005	6.6999
D to Z ↓	0.0142	0.0137	11.1722	4.1960
D to Z ↑	0.0230	0.0202	21.1737	6.8413
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0200	0.0206	2.9307	2.1973
A to Z ↑	0.0323	0.0330	4.4879	3.3710
B to Z ↓	0.0209	0.0208	2.9457	2.2095
B to Z ↑	0.0284	0.0288	4.4953	3.3439
C to Z ↓	0.0143	0.0151	2.9219	2.1970
C to Z ↑	0.0248	0.0255	4.4938	3.3581
D to Z ↓	0.0144	0.0141	2.9474	2.2174
D to Z ↑	0.0205	0.0207	4.4970	3.3685
	X24_P16		**X24_P16**	
A to Z ↓	0.0204		1.1272	
A to Z ↑	0.0323		1.6951	
B to Z ↓	0.0209		1.1331	
B to Z ↑	0.0282		1.6871	
C to Z ↓	0.0151		1.1077	
C to Z ↑	0.0254		1.6936	
D to Z ↓	0.0143		1.1182	
D to Z ↑	0.0206		1.6996	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P16	1.616e-06	1.000e-20
X6_P16	4.790e-06	1.000e-20
X9_P16	6.919e-06	1.000e-20
X12_P16	9.342e-06	1.000e-20
X24_P16	1.810e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P16	X6_P16	X9_P16	X12_P16
A (output stable)	1.149e-05	2.924e-05	5.780e-05	8.683e-05
B (output stable)	1.479e-05	4.090e-05	1.319e-04	2.233e-04
C (output stable)	1.694e-05	4.443e-05	8.174e-05	1.180e-04
D (output stable)	2.201e-05	6.001e-05	1.433e-04	2.417e-04
A to Z	8.016e-04	2.105e-03	3.367e-03	4.634e-03
B to Z	7.026e-04	1.826e-03	2.842e-03	3.893e-03
C to Z	4.491e-04	1.189e-03	1.972e-03	2.781e-03
D to Z	3.650e-04	9.648e-04	1.502e-03	2.052e-03
	X24_P16			
A (output stable)	1.584e-04			
B (output stable)	3.635e-04			
C (output stable)	2.297e-04			
D (output stable)	4.735e-04			

A to Z	8.932e-03			
B to Z	7.550e-03			
C to Z	5.403e-03			
D to Z	4.037e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

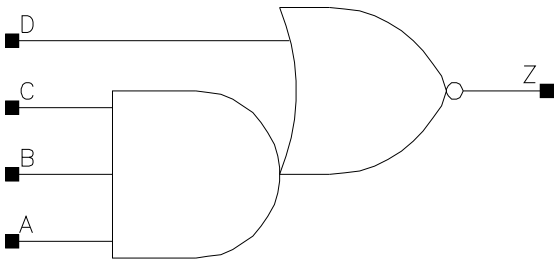
Pin Cycle (vdds)	X2_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X12_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X12_P16
A	0.0006	0.0022
B	0.0006	0.0021
C	0.0007	0.0020
D	0.0005	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X12_P16	X3_P16	X12_P16
A to Z ↓	0.0237	0.0246	11.7217	3.2325
A to Z ↑	0.0351	0.0335	14.2846	3.6798
B to Z ↓	0.0243	0.0238	11.7354	3.2368
B to Z ↑	0.0328	0.0301	14.4188	3.6782
C to Z ↓	0.0271	0.0225	11.7770	3.2434
C to Z ↑	0.0322	0.0257	14.5008	3.6967
D to Z ↓	0.0113	0.0096	4.6683	1.2678
D to Z ↑	0.0222	0.0190	12.3529	3.1586

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	2.289e-06	1.000e-20
X12_P16	7.677e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X12_P16
A (output stable)	8.505e-06	4.784e-05
B (output stable)	1.299e-05	9.910e-05
C (output stable)	3.006e-05	2.041e-04
D (output stable)	1.555e-04	5.770e-04
A to Z	1.221e-03	4.556e-03
B to Z	1.102e-03	3.822e-03
C to Z	1.022e-03	3.102e-03
D to Z	5.981e-04	1.870e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

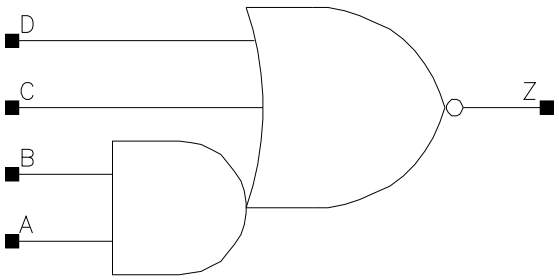
Pin Cycle (vdds)	X3_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X20_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P16	X20_P16
A	0.0005	0.0039
B	0.0005	0.0035
C	0.0006	0.0038
D	0.0006	0.0036

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X20_P16	X3_P16	X20_P16
A to Z ↓	0.0153	0.0168	7.9804	1.2728
A to Z ↑	0.0316	0.0300	20.9463	2.6869
B to Z ↓	0.0167	0.0166	8.0385	1.2832
B to Z ↑	0.0279	0.0240	21.0905	2.6900
C to Z ↓	0.0164	0.0217	4.6758	0.9804
C to Z ↑	0.0400	0.0379	19.8967	2.5375
D to Z ↓	0.0161	0.0202	4.6671	0.9770

D to Z ↑	0.0398	0.0347	19.9125	2.5412

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	1.878e-06	1.000e-20
X20_P16	1.117e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X20_P16
A (output stable)	1.992e-05	1.629e-04
B (output stable)	2.204e-05	2.067e-04
C (output stable)	2.597e-05	3.024e-04
D (output stable)	2.439e-05	2.016e-04
A to Z	7.488e-04	5.151e-03
B to Z	6.408e-04	3.920e-03
C to Z	1.216e-03	8.997e-03
D to Z	1.064e-03	7.103e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

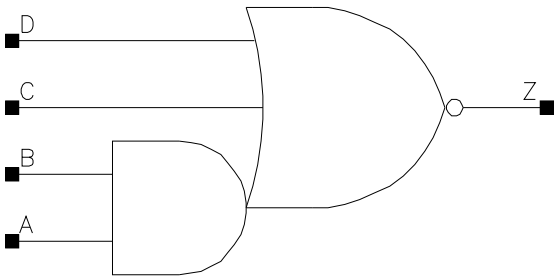
Pin Cycle (vdds)	X3_P16	X20_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.816	0.6528
X10_P16	0.800	2.448	1.9584
X19_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P16	X10_P16	X19_P16
A	0.0005	0.0021	0.0041
B	0.0005	0.0019	0.0038
C	0.0006	0.0017	0.0034
D	0.0005	0.0016	0.0030

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	X10_P16	X2_P16	X10_P16
A to Z ↓	0.0201	0.0208	9.5748	2.5311
A to Z ↑	0.0416	0.0391	22.1637	5.3595
B to Z ↓	0.0221	0.0211	9.6187	2.5449
B to Z ↑	0.0378	0.0335	22.2331	5.3757
C to Z ↓	0.0185	0.0170	8.1762	2.0652
C to Z ↑	0.0308	0.0284	21.0434	5.0795

D to Z ↓	0.0157	0.0131	8.2275	2.0804
D to Z ↑	0.0269	0.0220	21.0753	5.0971
	X19_P16		**X19_P16**	
A to Z ↓	0.0203		1.2936	
A to Z ↑	0.0381		2.7067	
B to Z ↓	0.0209		1.3004	
B to Z ↑	0.0325		2.7092	
C to Z ↓	0.0173		1.0890	
C to Z ↑	0.0275		2.5630	
D to Z ↓	0.0133		1.0980	
D to Z ↑	0.0209		2.5725	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P16	1.494e-06	1.000e-20
X10_P16	5.753e-06	1.000e-20
X19_P16	1.114e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P16	X10_P16	X19_P16
A (output stable)	1.246e-05	5.241e-05	1.020e-04
B (output stable)	1.239e-05	8.350e-05	1.552e-04
C (output stable)	8.148e-06	9.371e-05	1.840e-04
D (output stable)	3.730e-05	2.092e-04	4.018e-04
A to Z	1.168e-03	4.445e-03	8.529e-03
B to Z	1.056e-03	3.740e-03	7.186e-03
C to Z	7.040e-04	2.703e-03	5.102e-03
D to Z	5.382e-04	1.709e-03	3.162e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

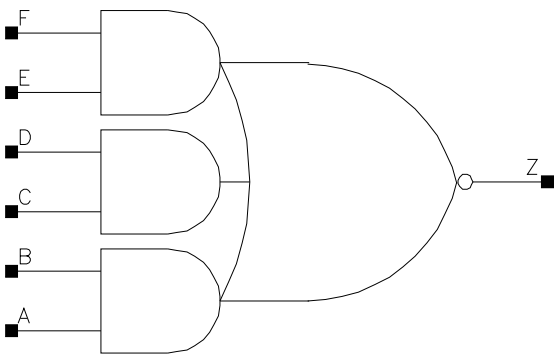
Pin Cycle (vdds)	X2_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.088	0.8704
X5_P16	0.800	2.040	1.6320
X7_P16	0.800	2.720	2.1760
X9_P16	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P16	X5_P16	X7_P16	X9_P16
A	0.0005	0.0010	0.0016	0.0021

B	0.0005	0.0011	0.0014	0.0019
C	0.0005	0.0009	0.0015	0.0022
D	0.0005	0.0010	0.0014	0.0019
E	0.0006	0.0010	0.0014	0.0018
F	0.0005	0.0008	0.0013	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X5_P16**	**X2_P16**	**X5_P16**
A to Z ↓	0.0213	0.0261	8.4727	4.8646
A to Z ↑	0.0536	0.0497	21.4435	9.6371
B to Z ↓	0.0234	0.0287	8.5086	4.8776
B to Z ↑	0.0492	0.0471	21.5226	9.5906
C to Z ↓	0.0200	0.0236	8.5418	4.8300
C to Z ↑	0.0463	0.0437	21.5209	9.6489
D to Z ↓	0.0218	0.0259	8.5967	4.8496
D to Z ↑	0.0421	0.0414	21.5253	9.6226
E to Z ↓	0.0155	0.0182	8.5649	4.7662
E to Z ↑	0.0347	0.0340	21.5229	9.6081
F to Z ↓	0.0162	0.0193	8.6368	4.7887
F to Z ↑	0.0292	0.0299	21.4978	9.6284
	X7_P16	**X9_P16**	**X7_P16**	**X9_P16**
A to Z ↓	0.0259	0.0264	3.3566	2.5501
A to Z ↑	0.0488	0.0499	6.3483	4.7809
B to Z ↓	0.0272	0.0273	3.3661	2.5577
B to Z ↑	0.0446	0.0451	6.4452	4.8338
C to Z ↓	0.0236	0.0243	3.3677	2.5296
C to Z ↑	0.0433	0.0450	6.4314	4.8321
D to Z ↓	0.0248	0.0243	3.3828	2.5401
D to Z ↑	0.0387	0.0391	6.3967	4.8073
E to Z ↓	0.0174	0.0176	3.3612	2.5272
E to Z ↑	0.0322	0.0322	6.3862	4.8148
F to Z ↓	0.0180	0.0171	3.3854	2.5481
F to Z ↑	0.0278	0.0269	6.4279	4.8136

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P16	2.728e-06	1.000e-20
X5_P16	5.413e-06	1.000e-20
X7_P16	7.721e-06	1.000e-20
X9_P16	1.020e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

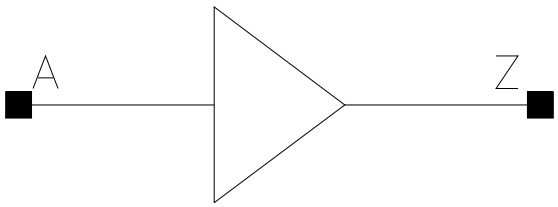
Pin Cycle (vdd)	X2_P16	X5_P16	X7_P16	X9_P16
A (output stable)	1.963e-05	3.616e-05	6.612e-05	9.286e-05
B (output stable)	2.207e-05	4.784e-05	1.046e-04	1.756e-04
C (output stable)	1.878e-05	3.805e-05	6.001e-05	8.498e-05
D (output stable)	2.332e-05	4.640e-05	1.070e-04	1.555e-04
E (output stable)	2.762e-05	6.090e-05	1.010e-04	1.433e-04
F (output stable)	3.436e-05	6.935e-05	1.373e-04	2.236e-04

A to Z	1.590e-03	3.252e-03	4.785e-03	6.543e-03
B to Z	1.462e-03	3.087e-03	4.317e-03	5.852e-03
C to Z	1.191e-03	2.504e-03	3.661e-03	4.990e-03
D to Z	1.074e-03	2.340e-03	3.235e-03	4.368e-03
E to Z	7.375e-04	1.709e-03	2.362e-03	3.140e-03
F to Z	6.273e-04	1.505e-03	1.969e-03	2.513e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X2_P16	X5_P16	X7_P16	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.544	0.4352
X5_P16	0.800	0.544	0.4352
X9_P16	0.800	0.680	0.5440
X11_P16	1.600	0.408	0.6528
X13_P16	0.800	0.680	0.5440
X19_P16	0.800	0.952	0.7616
X23_P16	1.600	0.544	0.8704
X24_P16	0.800	1.088	0.8704
X29_P16	0.800	1.224	0.9792
X34_P16	1.600	0.680	1.0880
X38_P16	0.800	1.632	1.3056
X46_P16	1.600	0.952	1.5232
X57_P16	0.800	2.312	1.8496
X68_P16	1.600	1.224	1.9584
X91_P16	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P16	X5_P16	X9_P16	X11_P16
A	0.0006	0.0006	0.0005	0.0008
	X13_P16	X19_P16	X23_P16	X24_P16
A	0.0007	0.0010	0.0012	0.0011
	X29_P16	X34_P16	X38_P16	X46_P16
A	0.0013	0.0015	0.0020	0.0020
	X57_P16	X68_P16	X91_P16	
A	0.0026	0.0028	0.0036	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X5_P16**	**X2_P16**	**X5_P16**
A to Z ↓	0.0365	0.0375	9.3045	4.8303
A to Z ↑	0.0288	0.0282	15.8254	8.0742
	X9_P16	**X11_P16**	**X9_P16**	**X11_P16**
A to Z ↓	0.0452	0.0416	2.4848	1.8161
A to Z ↑	0.0332	0.0298	4.0301	3.7986
	X13_P16	**X19_P16**	**X13_P16**	**X19_P16**
A to Z ↓	0.0390	0.0394	1.6987	1.2018
A to Z ↑	0.0303	0.0287	2.7604	1.9482
	X23_P16	**X24_P16**	**X23_P16**	**X24_P16**
A to Z ↓	0.0401	0.0383	0.8820	0.9753
A to Z ↑	0.0283	0.0292	1.9083	1.5590
	X29_P16	**X34_P16**	**X29_P16**	**X34_P16**
A to Z ↓	0.0366	0.0387	0.8101	0.6046
A to Z ↑	0.0283	0.0281	1.3071	1.2933
	X38_P16	**X46_P16**	**X38_P16**	**X46_P16**
A to Z ↓	0.0359	0.0382	0.6125	0.4554
A to Z ↑	0.0280	0.0275	0.9677	0.9721
	X57_P16	**X68_P16**	**X57_P16**	**X68_P16**
A to Z ↓	0.0372	0.0373	0.4117	0.3089
A to Z ↑	0.0289	0.0271	0.6480	0.6506
	X91_P16		**X91_P16**	
A to Z ↓	0.0393		0.2384	
A to Z ↑	0.0284		0.4893	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P16	1.449e-06	1.000e-20
X5_P16	2.325e-06	1.000e-20
X9_P16	3.749e-06	1.000e-20
X11_P16	4.983e-06	1.000e-20
X13_P16	5.642e-06	1.000e-20
X19_P16	7.450e-06	1.000e-20
X23_P16	9.527e-06	1.000e-20
X24_P16	9.261e-06	1.000e-20
X29_P16	1.122e-05	1.000e-20
X34_P16	1.358e-05	1.000e-20
X38_P16	1.516e-05	1.000e-20
X46_P16	1.745e-05	1.000e-20
X57_P16	2.175e-05	1.000e-20
X68_P16	2.564e-05	1.000e-20
X91_P16	3.298e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P16	X5_P16	X9_P16	X11_P16
A to Z	8.631e-04	1.120e-03	1.783e-03	2.176e-03
	X13_P16	X19_P16	X23_P16	X24_P16
A to Z	2.567e-03	3.457e-03	3.955e-03	4.274e-03
	X29_P16	X34_P16	X38_P16	X46_P16

A to Z	4.955e-03	5.862e-03	6.852e-03	7.569e-03
	X57_P16	X68_P16	X91_P16	
A to Z	9.976e-03	1.097e-02	1.480e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

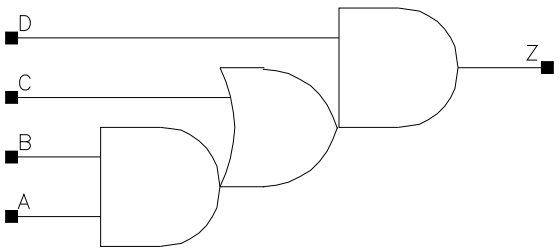
Pin Cycle (vdds)	X2_P16	X5_P16	X9_P16	X11_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P16	X19_P16	X23_P16	X24_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P16	X34_P16	X38_P16	X46_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P16	X68_P16	X91_P16	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.952	0.7616
X10_P16	0.800	1.632	1.3056
X14_P16	0.800	1.768	1.4144
X19_P16	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0006	0.0013	0.0013	0.0013
B	0.0006	0.0012	0.0011	0.0011
C	0.0006	0.0014	0.0014	0.0014
D	0.0010	0.0013	0.0013	0.0013

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0499	0.0454	4.9477	2.3409
A to Z ↑	0.0456	0.0410	8.2349	3.9172
B to Z ↓	0.0466	0.0419	4.9274	2.3335
B to Z ↑	0.0462	0.0411	8.2387	3.9142
C to Z ↓	0.0415	0.0371	4.9233	2.3301
C to Z ↑	0.0337	0.0296	8.1709	3.8798

D to Z ↓	0.0405	0.0344	4.8798	2.3109
D to Z ↑	0.0398	0.0333	8.1837	3.8837
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0508	0.0545	1.6276	1.2256
A to Z ↑	0.0459	0.0490	2.6289	1.9744
B to Z ↓	0.0474	0.0512	1.6258	1.2237
B to Z ↑	0.0460	0.0491	2.6305	1.9765
C to Z ↓	0.0422	0.0460	1.6189	1.2189
C to Z ↑	0.0333	0.0357	2.5984	1.9503
D to Z ↓	0.0377	0.0399	1.5980	1.1996
D to Z ↑	0.0368	0.0391	2.6018	1.9542

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	3.527e-06	1.000e-20
X10_P16	6.953e-06	1.000e-20
X14_P16	8.276e-06	1.000e-20
X19_P16	9.604e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	4.082e-05	7.789e-05	7.872e-05	7.876e-05
B (output stable)	5.254e-05	9.850e-05	9.929e-05	9.940e-05
C (output stable)	1.560e-04	2.545e-04	2.530e-04	2.530e-04
D (output stable)	4.892e-05	7.283e-05	7.374e-05	7.363e-05
A to Z	1.895e-03	3.417e-03	4.372e-03	5.138e-03
B to Z	1.777e-03	3.138e-03	4.087e-03	4.845e-03
C to Z	1.479e-03	2.534e-03	3.427e-03	4.148e-03
D to Z	1.938e-03	3.328e-03	4.199e-03	4.878e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

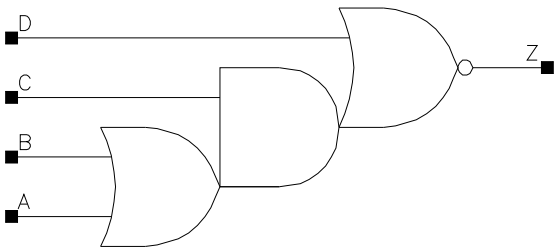
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X6_P16	0.800	1.496	1.1968
X9_P16	0.800	1.768	1.4144
X12_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X9_P16	X12_P16
A	0.0006	0.0011	0.0017	0.0021
B	0.0006	0.0010	0.0016	0.0021
C	0.0006	0.0010	0.0015	0.0020
D	0.0007	0.0010	0.0014	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0209	0.0191	8.2775	4.2147
A to Z ↑	0.0438	0.0427	20.9894	10.8722
B to Z ↓	0.0200	0.0189	8.1015	4.2423
B to Z ↑	0.0428	0.0404	20.9993	10.8782
C to Z ↓	0.0185	0.0172	7.6207	3.9267
C to Z ↑	0.0275	0.0259	14.5069	7.4324

D to Z ↓	0.0116	0.0095	4.6924	2.3877
D to Z ↑	0.0245	0.0205	15.4108	7.9121
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0193	0.0197	2.9101	2.2381
A to Z ↑	0.0399	0.0420	7.0894	5.4170
B to Z ↓	0.0186	0.0188	2.9233	2.2326
B to Z ↑	0.0391	0.0397	7.0898	5.4189
C to Z ↓	0.0175	0.0175	2.7205	2.0778
C to Z ↑	0.0251	0.0253	4.8690	3.6897
D to Z ↓	0.0097	0.0095	1.6646	1.2724
D to Z ↑	0.0193	0.0190	5.1753	3.9312

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	2.246e-06	1.000e-20
X6_P16	4.308e-06	1.000e-20
X9_P16	5.841e-06	1.000e-20
X12_P16	7.798e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	9.890e-06	2.494e-05	3.014e-05	5.167e-05
B (output stable)	3.421e-06	6.957e-06	1.045e-05	1.331e-05
C (output stable)	4.212e-05	9.370e-05	1.258e-04	1.714e-04
D (output stable)	7.641e-05	1.902e-04	2.576e-04	3.708e-04
A to Z	1.274e-03	2.416e-03	3.363e-03	4.706e-03
B to Z	1.110e-03	1.991e-03	2.879e-03	3.874e-03
C to Z	8.857e-04	1.608e-03	2.309e-03	3.146e-03
D to Z	5.626e-04	9.027e-04	1.246e-03	1.631e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

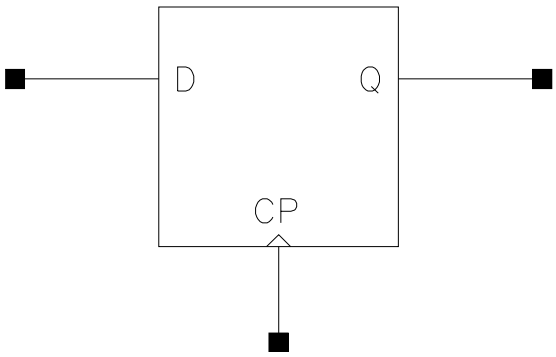
Pin Cycle (vdds)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	1.600	1.496	2.3936
X19_P16	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P16	X19_P16
CP	0.0009	0.0009
D	0.0007	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P16	X19_P16	X10_P16	X19_P16
CP to Q ↓	0.0763	0.1043	2.4642	1.3494
CP to Q ↑	0.0878	0.1007	3.8977	1.9978

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P16	X19_P16
CP ↓	min_pulse_width to CP	0.0805	0.0805
CP ↑	min_pulse_width to CP	0.0639	0.0925
D ↓	hold_rising to CP	0.0123	0.0123
D ↑	hold_rising to CP	0.0026	0.0026
D ↓	setup_rising to CP	0.0424	0.0424
D ↑	setup_rising to CP	0.0248	0.0248

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P16	1.107e-05	1.000e-20
X19_P16	1.374e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

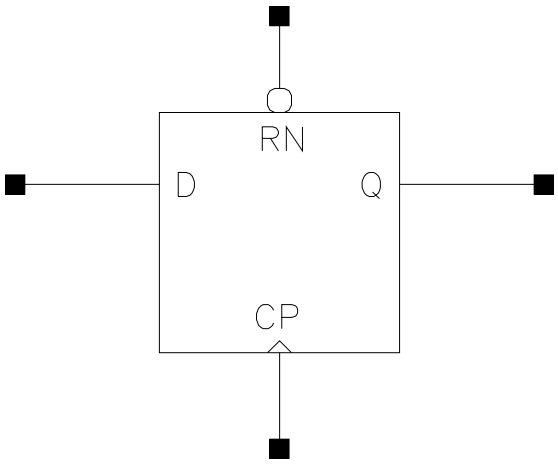
Pin Cycle	X10_P16	X19_P16
Clock 100Mhz Data 0Mhz	6.136e-03	6.139e-03
Clock 100Mhz Data 25Mhz	7.364e-03	8.638e-03
Clock 100Mhz Data 50Mhz	8.592e-03	1.114e-02
Clock = 0 Data 100Mhz	2.463e-03	2.463e-03
Clock = 1 Data 100Mhz	1.356e-05	1.364e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	1.600	1.768	2.8288
X19_P16	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P16	X19_P16
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0008	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P16	X19_P16	X10_P16	X19_P16
CP to Q ↓	0.0834	0.1090	2.5050	1.3343
CP to Q ↑	0.0915	0.1044	3.8913	1.9867
RN to Q ↓	0.0867	0.1142	2.4664	1.2872

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P16	X19_P16
CP ↓	min_pulse_width to CP	0.0805	0.0805
CP ↑	min_pulse_width to CP	0.0674	0.0925
D ↓	hold_rising to CP	0.0123	0.0123
D ↑	hold_rising to CP	0.0026	0.0026
D ↓	setup_rising to CP	0.0392	0.0392
D ↑	setup_rising to CP	0.0270	0.0270
RN ↓	min_pulse_width to RN	0.1023	0.1338
RN ↑	recovery_rising to CP	0.0178	0.0173
RN ↑	removal_rising to CP	-0.0077	-0.0077

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P16	1.228e-05	1.000e-20
X19_P16	1.523e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

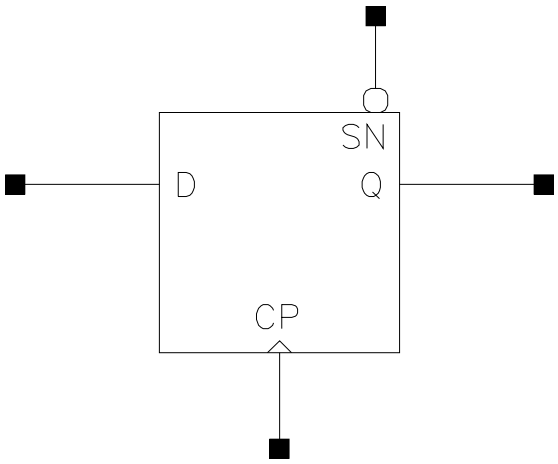
Pin Cycle	X10_P16	X19_P16
Clock 100Mhz Data 0Mhz	6.197e-03	6.198e-03
Clock 100Mhz Data 25Mhz	7.542e-03	8.824e-03
Clock 100Mhz Data 50Mhz	8.888e-03	1.145e-02
Clock = 0 Data 100Mhz	2.481e-03	2.481e-03
Clock = 1 Data 100Mhz	1.382e-05	1.389e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	1.600	1.768	2.8288
X19_P16	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P16	X19_P16
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0010	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P16	X19_P16	X10_P16	X19_P16
CP to Q ↓	0.0786	0.1065	2.4834	1.3255
CP to Q ↑	0.0909	0.1049	3.8900	1.9885
SN to Q ↑	0.0540	0.0616	3.8172	1.9318

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P16	X19_P16
CP ↓	min_pulse_width to CP	0.0805	0.0805
CP ↑	min_pulse_width to CP	0.0639	0.0925
D ↓	hold_rising to CP	0.0123	0.0123
D ↑	hold_rising to CP	0.0053	0.0053
D ↓	setup_rising to CP	0.0419	0.0424
D ↑	setup_rising to CP	0.0216	0.0216
SN ↓	min_pulse_width to SN	0.0566	0.0593
SN ↑	recovery_rising to CP	0.0086	0.0107
SN ↑	removal_rising to CP	0.0454	0.0454

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P16	1.290e-05	1.000e-20
X19_P16	1.603e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

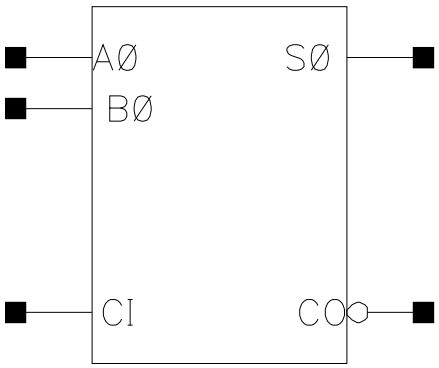
Pin Cycle	X10_P16	X19_P16
Clock 100Mhz Data 0Mhz	6.082e-03	6.085e-03
Clock 100Mhz Data 25Mhz	7.364e-03	8.704e-03
Clock 100Mhz Data 50Mhz	8.646e-03	1.132e-02
Clock = 0 Data 100Mhz	2.386e-03	2.386e-03
Clock = 1 Data 100Mhz	1.381e-05	1.389e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_-P16	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_-P16	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_-P16	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_-P16	1.600	2.720	4.3520
C8T28SOIDV_LLS1_-FA1X4_P16	1.600	2.040	3.2640
C8T28SOIDV_LLS1_-FA1X9_P16	1.600	3.128	5.0048
C8T28SOIDV_LLS1_-FA1X18_P16	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P16	C8T28SOIDV_LL_-FA1X9_P16	C8T28SOIDV_LL_-FA1X14_P16	C8T28SOIDV_LL_-FA1X19_P16
A0	0.0023	0.0024	0.0038	0.0041
B0	0.0019	0.0020	0.0035	0.0038
CI	0.0015	0.0015	0.0026	0.0029
	C8T28SOIDV_LLS1_-FA1X4_P16	C8T28SOIDV_LLS1_-FA1X9_P16	C8T28SOIDV_LLS1_-FA1X18_P16	
A0	0.0022	0.0030	0.0031	
B0	0.0021	0.0033	0.0037	
CI	0.0016	0.0023	0.0027	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P16	**C8T28SOIDV_LL_-FA1X9_P16**	**C8T28SOIDV_LL_-FA1X5_P16**	**C8T28SOIDV_LL_-FA1X9_P16**
A0 to CO ↓	0.0665	0.0707	5.0700	2.6082
A0 to CO ↑	0.0483	0.0510	7.7162	3.9297
A0 to S0 ↓	0.0722	0.0788	4.9906	2.5732
A0 to S0 ↑	0.0745	0.0802	7.6877	3.8659
B0 to CO ↓	0.0663	0.0704	5.0924	2.6221
B0 to CO ↑	0.0498	0.0523	7.7195	3.9332
B0 to S0 ↓	0.0724	0.0793	4.9912	2.5737
B0 to S0 ↑	0.0750	0.0810	7.6900	3.8653
CI to CO ↓	0.0619	0.0655	5.0888	2.6206
CI to CO ↑	0.0483	0.0505	7.7155	3.9268
CI to S0 ↓	0.0717	0.0786	4.9929	2.5731
CI to S0 ↑	0.0742	0.0799	7.6889	3.8664
	C8T28SOIDV_LL_-FA1X14_P16	**C8T28SOIDV_LL_-FA1X19_P16**	**C8T28SOIDV_LL_-FA1X14_P16**	**C8T28SOIDV_LL_-FA1X19_P16**
A0 to CO ↓	0.0675	0.0742	1.6892	1.2920
A0 to CO ↑	0.0489	0.0505	2.6737	2.0019
A0 to S0 ↓	0.0830	0.0835	1.6822	1.2519
A0 to S0 ↑	0.0849	0.0875	2.6048	1.9450
B0 to CO ↓	0.0660	0.0727	1.6966	1.2968
B0 to CO ↑	0.0493	0.0509	2.6737	2.0013
B0 to S0 ↓	0.0831	0.0837	1.6818	1.2517
B0 to S0 ↑	0.0850	0.0875	2.6060	1.9459
CI to CO ↓	0.0617	0.0681	1.6942	1.2947
CI to CO ↑	0.0476	0.0493	2.6731	2.0012
CI to S0 ↓	0.0818	0.0823	1.6818	1.2511
CI to S0 ↑	0.0832	0.0858	2.6052	1.9453
	C8T28SOIDV_-LLS1_FA1X4_P16	**C8T28SOIDV_-LLS1_FA1X9_P16**	**C8T28SOIDV_-LLS1_FA1X4_P16**	**C8T28SOIDV_-LLS1_FA1X9_P16**
A0 to CO ↓	0.0426	0.0396	9.8618	3.1901
A0 to CO ↑	0.0372	0.0361	7.7347	3.9251
A0 to S0 ↓	0.0947	0.1043	5.3508	1.9145
A0 to S0 ↑	0.0885	0.0883	8.1802	3.8514
B0 to CO ↓	0.0405	0.0404	9.8464	3.1919
B0 to CO ↑	0.0328	0.0343	7.7132	3.9224
B0 to S0 ↓	0.0966	0.1086	5.3500	1.9150
B0 to S0 ↑	0.0906	0.0926	8.1725	3.8499
CI to CO ↓	0.0409	0.0563	9.8503	3.2191
CI to CO ↑	0.0359	0.0339	7.7343	3.9460

CI to S0 ↓	0.0522	0.0628	5.3502	1.9162
CI to S0 ↑	0.0462	0.0468	8.1758	3.8501
	C8T28SOIDV_-LLS1_FA1X18_P16		**C8T28SOIDV_-LLS1_FA1X18_P16**	
A0 to CO ↓	0.0504		1.6557	
A0 to CO ↑	0.0378		1.9282	
A0 to S0 ↓	0.1104		0.9920	
A0 to S0 ↑	0.0888		1.9295	
B0 to CO ↓	0.0519		1.6565	
B0 to CO ↑	0.0362		1.9268	
B0 to S0 ↓	0.1129		0.9920	
B0 to S0 ↑	0.0914		1.9290	
CI to CO ↓	0.0710		1.6748	
CI to CO ↑	0.0393		1.9322	
CI to S0 ↓	0.0652		0.9920	
CI to S0 ↑	0.0430		1.9283	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P16	8.307e-06	1.000e-20
C8T28SOIDV_LL_FA1X9_P16	1.168e-05	1.000e-20
C8T28SOIDV_LL_FA1X14_P16	1.748e-05	1.000e-20
C8T28SOIDV_LL_FA1X19_P16	2.170e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P16	1.789e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P16	2.730e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P16	4.103e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P16	C8T28SOIDV_LL_-FA1X9_P16	C8T28SOIDV_LL_-FA1X14_P16	C8T28SOIDV_LL_-FA1X19_P16
A0 to CO	2.093e-03	2.879e-03	4.782e-03	5.757e-03
A0 to S0	2.144e-03	2.831e-03	4.878e-03	5.884e-03
B0 to CO	2.115e-03	2.914e-03	4.812e-03	5.821e-03
B0 to S0	2.098e-03	2.800e-03	4.812e-03	5.812e-03
CI to CO	2.090e-03	2.864e-03	4.784e-03	5.823e-03
CI to S0	2.081e-03	2.781e-03	4.773e-03	5.765e-03
	C8T28SOIDV_LLS1_-FA1X4_P16	C8T28SOIDV_LLS1_-FA1X9_P16	C8T28SOIDV_LLS1_-FA1X18_P16	
A0 to CO	3.232e-03	4.947e-03	7.844e-03	
A0 to S0	4.385e-03	6.410e-03	9.829e-03	
B0 to CO	3.439e-03	5.040e-03	7.916e-03	
B0 to S0	4.742e-03	6.610e-03	1.001e-02	
CI to CO	2.294e-03	4.073e-03	6.797e-03	
CI to S0	2.596e-03	4.537e-03	7.408e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P16	C8T28SOIDV_LL_-FA1X9_P16	C8T28SOIDV_LL_-FA1X14_P16	C8T28SOIDV_LL_-FA1X19_P16
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P16	C8T28SOIDV_LLS1_-FA1X9_P16	C8T28SOIDV_LLS1_-FA1X18_P16	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P16	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P16	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P16	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P16	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P16	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P16	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P16	C8T28SOI_LL_-HA1X9_P16	C8T28SOI_LLS1_-HA1X5_P16	C8T28SOIDV_LL_-HA1X14_P16
A0	0.0008	0.0011	0.0013	0.0016
B0	0.0007	0.0012	0.0012	0.0014
	C8T28SOIDV_LL_-HA1X19_P16	C8T28SOIDV_LLS1_-HA1X11_P16		
A0	0.0019	0.0020		
B0	0.0017	0.0019		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P16	**C8T28SOI_LL_-HA1X9_P16**	**C8T28SOI_LL_-HA1X5_P16**	**C8T28SOI_LL_-HA1X9_P16**
A0 to CO ↓	0.0509	0.0428	4.9995	2.4527
A0 to CO ↑	0.0474	0.0403	8.2110	3.9408
A0 to S0 ↓	0.0686	0.0605	4.7966	2.4271
A0 to S0 ↑	0.0624	0.0556	8.0228	3.9166
B0 to CO ↓	0.0499	0.0418	5.0050	2.4496
B0 to CO ↑	0.0496	0.0430	8.2128	3.9420
B0 to S0 ↓	0.0698	0.0606	4.7982	2.4267
B0 to S0 ↑	0.0620	0.0549	8.0228	3.9157
	C8T28SOI_LLS1_-HA1X5_P16	**C8T28SOIDV_LL_-HA1X14_P16**	**C8T28SOI_LLS1_-HA1X5_P16**	**C8T28SOIDV_LL_-HA1X14_P16**
A0 to CO ↓	0.0406	0.0441	4.8831	1.6591
A0 to CO ↑	0.0377	0.0401	8.1110	2.6360
A0 to S0 ↓	0.0585	0.0674	4.8704	1.6644
A0 to S0 ↑	0.0637	0.0613	8.1541	2.6105
B0 to CO ↓	0.0387	0.0410	4.8836	1.6519
B0 to CO ↑	0.0392	0.0402	8.1088	2.6362
B0 to S0 ↓	0.0604	0.0654	4.8708	1.6654
B0 to S0 ↑	0.0632	0.0588	8.1574	2.6109
	C8T28SOIDV_LL_-HA1X19_P16	**C8T28SOIDV_-LLS1_HA1X11_P16**	**C8T28SOIDV_LL_-HA1X19_P16**	**C8T28SOIDV_-LLS1_HA1X11_P16**
A0 to CO ↓	0.0404	0.0387	1.2116	1.7152
A0 to CO ↑	0.0378	0.0397	1.9887	3.8786
A0 to S0 ↓	0.0612	0.0509	1.2016	1.7447
A0 to S0 ↑	0.0562	0.0522	1.9579	3.9042
B0 to CO ↓	0.0378	0.0368	1.2071	1.7121
B0 to CO ↑	0.0384	0.0419	1.9890	3.8781
B0 to S0 ↓	0.0602	0.0531	1.2031	1.7435
B0 to S0 ↑	0.0541	0.0520	1.9579	3.9024

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_HA1X5_P16	4.864e-06	1.000e-20
C8T28SOI_LL_HA1X9_P16	1.014e-05	1.000e-20
C8T28SOI_LLS1_HA1X5_P16	5.971e-06	1.000e-20
C8T28SOIDV_LL_HA1X14_P16	1.438e-05	1.000e-20
C8T28SOIDV_LL_HA1X19_P16	1.984e-05	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P16	1.420e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

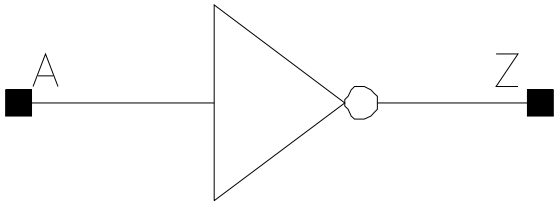
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P16	C8T28SOI_LL_-HA1X9_P16	C8T28SOI_LLS1_-HA1X5_P16	C8T28SOIDV_LL_-HA1X14_P16
A0 to CO	1.586e-03	2.539e-03	1.903e-03	4.108e-03
A0 to S0	1.424e-03	2.427e-03	1.677e-03	4.113e-03
B0 to CO	1.605e-03	2.626e-03	1.936e-03	4.070e-03
B0 to S0	1.399e-03	2.355e-03	1.629e-03	3.963e-03
	C8T28SOIDV_LL_-HA1X19_P16	C8T28SOIDV_LLS1_-HA1X11_P16		
A0 to CO	4.932e-03	3.582e-03		
A0 to S0	4.931e-03	3.227e-03		

B0 to CO	4.919e-03	3.315e-03		
B0 to S0	4.782e-03	3.340e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P16	C8T28SOI_LL_-HA1X9_P16	C8T28SOI_LLS1_-HA1X5_P16	C8T28SOIDV_LL_-HA1X14_P16
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P16	C8T28SOIDV_LLS1_-HA1X11_P16		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P16	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P16	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P16	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P16	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P16	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P16	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P16	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P16	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P16	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P16	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P16	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P16	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P16	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P16	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P16	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P16	C8T28SOI_LL_IVX3_-P16	C8T28SOI_LL_IVX5_-P16	C8T28SOI_LL_-IVX10_P16

A	0.0004	0.0004	0.0005	0.0010
	C8T28SOI_LL_-IVX14_P16	C8T28SOI_LL_-IVX19_P16	C8T28SOI_LL_-IVX29_P16	C8T28SOI_LL_-IVX34_P16
A	0.0015	0.0020	0.0029	0.0034
	C8T28SOI_LL_-IVX38_P16	C8T28SOIDV_LL_-IVX11_P16	C8T28SOIDV_LL_-IVX23_P16	C8T28SOIDV_LL_-IVX34_P16
A	0.0039	0.0011	0.0022	0.0032
	C8T28SOIDV_LL_-IVX46_P16	C8T28SOIDV_LL_-IVX68_P16	C8T28SOIDV_LL_-IVX91_P16	
A	0.0043	0.0065	0.0089	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P16	**C8T28SOI_LL_-IVX3_P16**	**C8T28SOI_LL_-IVX2_P16**	**C8T28SOI_LL_-IVX3_P16**
A to Z ↓	0.0111	0.0104	9.4289	7.2042
A to Z ↑	0.0185	0.0167	16.0094	11.9377
	C8T28SOI_LL_-IVX5_P16	**C8T28SOI_LL_-IVX10_P16**	**C8T28SOI_LL_-IVX5_P16**	**C8T28SOI_LL_-IVX10_P16**
A to Z ↓	0.0095	0.0076	4.8943	2.3417
A to Z ↑	0.0147	0.0122	8.1847	3.8912
	C8T28SOI_LL_-IVX14_P16	**C8T28SOI_LL_-IVX19_P16**	**C8T28SOI_LL_-IVX14_P16**	**C8T28SOI_LL_-IVX19_P16**
A to Z ↓	0.0079	0.0083	1.6171	1.2349
A to Z ↑	0.0123	0.0127	2.6096	1.9885
	C8T28SOI_LL_-IVX29_P16	**C8T28SOI_LL_-IVX34_P16**	**C8T28SOI_LL_-IVX29_P16**	**C8T28SOI_LL_-IVX34_P16**
A to Z ↓	0.0082	0.0077	0.8286	0.7076
A to Z ↑	0.0123	0.0117	1.3187	1.1289
	C8T28SOI_LL_-IVX38_P16	**C8T28SOIDV_LL_-IVX11_P16**	**C8T28SOI_LL_-IVX38_P16**	**C8T28SOIDV_LL_-IVX11_P16**
A to Z ↓	0.0080	0.0077	0.6263	1.8213
A to Z ↑	0.0120	0.0141	0.9962	3.9658
	C8T28SOIDV_LL_-IVX23_P16	**C8T28SOIDV_LL_-IVX34_P16**	**C8T28SOIDV_LL_-IVX23_P16**	**C8T28SOIDV_LL_-IVX34_P16**
A to Z ↓	0.0065	0.0070	0.8865	0.6072
A to Z ↑	0.0124	0.0127	1.9327	1.2941
	C8T28SOIDV_LL_-IVX46_P16	**C8T28SOIDV_LL_-IVX68_P16**	**C8T28SOIDV_LL_-IVX46_P16**	**C8T28SOIDV_LL_-IVX68_P16**
A to Z ↓	0.0068	0.0068	0.4583	0.3113
A to Z ↑	0.0121	0.0121	0.9710	0.6498
	C8T28SOIDV_LL_-IVX91_P16		**C8T28SOIDV_LL_-IVX91_P16**	
A to Z ↓	0.0073		0.2395	
A to Z ↑	0.0124		0.4917	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_IVX2_P16	7.695e-07	1.000e-20
C8T28SOI_LL_IVX3_P16	1.039e-06	1.000e-20
C8T28SOI_LL_IVX5_P16	1.563e-06	1.000e-20
C8T28SOI_LL_IVX10_P16	3.212e-06	1.000e-20

C8T28SOI_LL_IVX14_P16	4.565e-06	1.000e-20
C8T28SOI_LL_IVX19_P16	5.881e-06	1.000e-20
C8T28SOI_LL_IVX29_P16	8.509e-06	1.000e-20
C8T28SOI_LL_IVX34_P16	9.826e-06	1.000e-20
C8T28SOI_LL_IVX38_P16	1.114e-05	1.000e-20
C8T28SOIDV_LL_IVX11_P16	3.769e-06	1.000e-20
C8T28SOIDV_LL_IVX23_P16	7.454e-06	1.000e-20
C8T28SOIDV_LL_IVX34_P16	1.060e-05	1.000e-20
C8T28SOIDV_LL_IVX46_P16	1.365e-05	1.000e-20
C8T28SOIDV_LL_IVX68_P16	1.974e-05	1.000e-20
C8T28SOIDV_LL_IVX91_P16	2.584e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P16	C8T28SOI_LL_IVX3_-P16	C8T28SOI_LL_IVX5_-P16	C8T28SOI_LL_-IVX10_P16
A to Z	2.438e-04	2.892e-04	3.486e-04	5.809e-04
	C8T28SOI_LL_-IVX14_P16	C8T28SOI_LL_-IVX19_P16	C8T28SOI_LL_-IVX29_P16	C8T28SOI_LL_-IVX34_P16
A to Z	9.114e-04	1.267e-03	1.812e-03	1.978e-03
	C8T28SOI_LL_-IVX38_P16	C8T28SOIDV_LL_-IVX11_P16	C8T28SOIDV_LL_-IVX23_P16	C8T28SOIDV_LL_-IVX34_P16
A to Z	2.330e-03	7.401e-04	1.248e-03	1.959e-03
	C8T28SOIDV_LL_-IVX46_P16	C8T28SOIDV_LL_-IVX68_P16	C8T28SOIDV_LL_-IVX91_P16	
A to Z	2.404e-03	3.592e-03	4.795e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

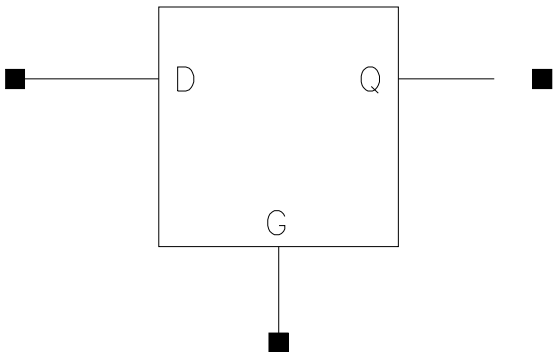
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P16	C8T28SOI_LL_IVX3_-P16	C8T28SOI_LL_IVX5_-P16	C8T28SOI_LL_-IVX10_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P16	C8T28SOI_LL_-IVX19_P16	C8T28SOI_LL_-IVX29_P16	C8T28SOI_LL_-IVX34_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P16	C8T28SOIDV_LL_-IVX11_P16	C8T28SOIDV_LL_-IVX23_P16	C8T28SOIDV_LL_-IVX34_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P16	C8T28SOIDV_LL_-IVX68_P16	C8T28SOIDV_LL_-IVX91_P16	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.360	1.0880
X9_P16	1.600	0.952	1.5232
X19_P16	1.600	1.224	1.9584
X28_P16	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16	X28_P16
D	0.0004	0.0006	0.0009	0.0016
G	0.0009	0.0009	0.0018	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D to Q ↓	0.0767	0.0714	5.1440	2.5471
D to Q ↑	0.0415	0.0492	7.9076	3.8943
G to Q ↓	0.0840	0.0757	5.1383	2.5476

G to Q ↑	0.0400	0.0449	7.9099	3.8981
	X19_P16	**X28_P16**	**X19_P16**	**X28_P16**
D to Q ↓	0.0579	0.0613	1.2228	0.8233
D to Q ↑	0.0411	0.0417	1.9543	1.3080
G to Q ↓	0.0654	0.0594	1.2226	0.8224
G to Q ↑	0.0379	0.0381	1.9560	1.3091

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P16	X9_P16	X19_P16	X28_P16
D ↓	hold_falling to G	-0.0237	-0.0241	-0.0094	-0.0133
D ↑	hold_falling to G	-0.0052	-0.0100	-0.0052	-0.0052
D ↓	setup_falling to G	0.0682	0.0635	0.0489	0.0538
D ↑	setup_falling to G	0.0458	0.0497	0.0448	0.0448
G ↑	min_pulse_width to G	0.0693	0.0610	0.0500	0.0487

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	4.259e-06	1.000e-20
X9_P16	6.609e-06	1.000e-20
X19_P16	1.114e-05	1.000e-20
X28_P16	1.495e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	6.773e-06	1.891e-05	2.150e-05	6.252e-05
G (output stable)	6.176e-04	7.352e-04	1.207e-03	1.108e-03
D to Q	2.353e-03	3.723e-03	5.530e-03	8.148e-03
G to Q	2.181e-03	3.425e-03	5.006e-03	6.912e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

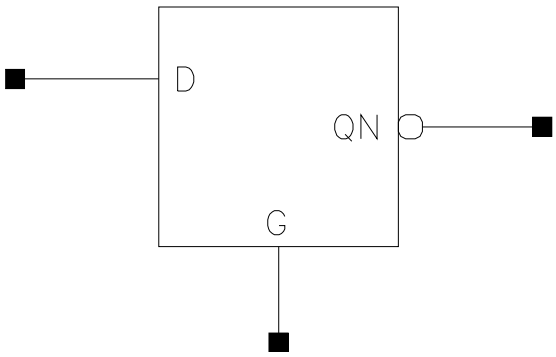
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P16
D	0.0004
G	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P16	X10_P16
D to QN ↓	0.0670	2.3495
D to QN ↑	0.0900	3.8635
G to QN ↓	0.0654	2.3478
G to QN ↑	0.0962	3.8660

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P16
D ↓	hold_falling to G	-0.0360
D ↑	hold_falling to G	-0.0159
D ↓	setup_falling to G	0.0635
D ↑	setup_falling to G	0.0432
G ↑	min_pulse_width to G	0.0645

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P16	6.175e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X10_P16
D (output stable)	6.665e-06
G (output stable)	6.439e-04
D to QN	3.166e-03
G to QN	2.931e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

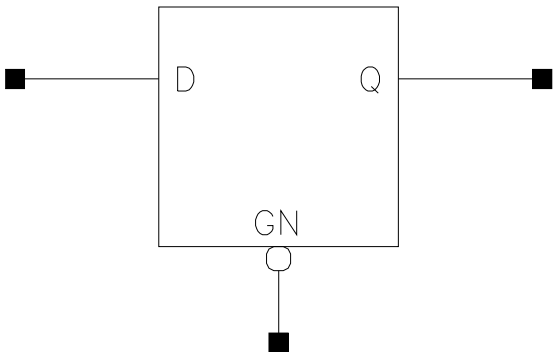
Pin Cycle (vdds)	X10_P16
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.360	1.0880
X9_P16	1.600	0.952	1.5232
X19_P16	1.600	1.224	1.9584
X28_P16	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16	X28_P16
D	0.0004	0.0007	0.0009	0.0014
GN	0.0008	0.0009	0.0013	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D to Q ↓	0.0775	0.0699	5.1569	2.5571
D to Q ↑	0.0419	0.0487	7.8982	3.9046
GN to Q ↓	0.0682	0.0647	5.1541	2.5594

GN to Q ↑	0.0737	0.0692	7.8964	3.8914
	X19_P16	**X28_P16**	**X19_P16**	**X28_P16**
D to Q ↓	0.0584	0.0580	1.2222	0.8190
D to Q ↑	0.0435	0.0424	1.9480	1.2991
GN to Q ↓	0.0510	0.0483	1.2227	0.8197
GN to Q ↑	0.0609	0.0602	1.9445	1.2976

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P16	X9_P16	X19_P16	X28_P16
D ↓	hold_rising to GN	-0.0314	-0.0269	-0.0162	-0.0162
D ↑	hold_rising to GN	0.0004	-0.0071	-0.0017	-0.0022
D ↓	setup_rising to GN	0.0834	0.0711	0.0672	0.0614
D ↑	setup_rising to GN	0.0368	0.0465	0.0416	0.0367
GN ↓	min_pulse_width to GN	0.0849	0.0772	0.0684	0.0606

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	4.003e-06	1.000e-20
X9_P16	6.371e-06	1.000e-20
X19_P16	1.109e-05	1.000e-20
X28_P16	1.448e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	6.640e-06	1.084e-05	2.144e-05	5.310e-05
GN (output stable)	6.190e-04	7.201e-04	1.027e-03	1.103e-03
D to Q	2.351e-03	3.724e-03	5.717e-03	7.856e-03
GN to Q	3.550e-03	5.032e-03	7.359e-03	9.335e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

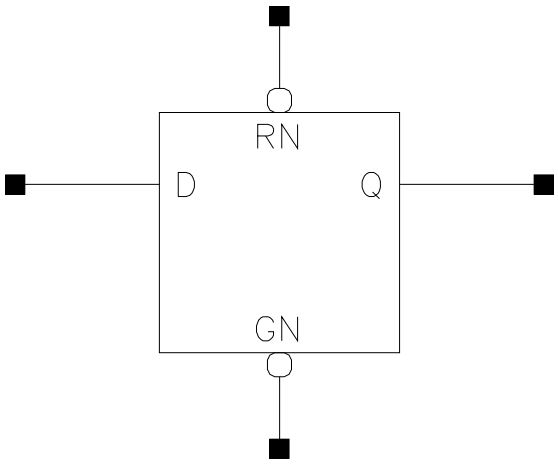
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.632	1.3056
X9_P16	1.600	1.224	1.9584
X19_P16	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16
D	0.0004	0.0006	0.0011
GN	0.0010	0.0010	0.0015
RN	0.0004	0.0005	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D to Q ↓	0.0786	0.0740	5.0576	2.5003

D to Q ↑	0.0692	0.0766	8.2167	4.0420
GN to Q ↓	0.0711	0.0672	5.0545	2.5018
GN to Q ↑	0.0968	0.0914	8.2158	4.0544
RN to Q ↓	0.0616	0.0791	4.8293	2.5089
RN to Q ↑	0.0770	0.0826	8.2134	4.0472
	X19_P16		**X19_P16**	
D to Q ↓	0.0613		1.2290	
D to Q ↑	0.0818		2.0410	
GN to Q ↓	0.0542		1.2306	
GN to Q ↑	0.0866		2.0485	
RN to Q ↓	0.1034		1.3424	
RN to Q ↑	0.0883		2.0460	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P16	X9_P16	X19_P16
D ↓	hold_rising to GN	-0.0314	-0.0318	-0.0194
D ↑	hold_rising to GN	-0.0218	-0.0257	-0.0359
D ↓	setup_rising to GN	0.0884	0.0819	0.0668
D ↑	setup_rising to GN	0.0709	0.0757	0.0907
GN ↓	min_pulse_width to GN	0.0932	0.0901	0.0902
RN ↓	min_pulse_width to RN	0.0757	0.0903	0.1169
RN ↑	recovery_rising to GN	0.0785	0.0881	0.1000
RN ↑	removal_rising to GN	-0.0493	-0.0560	-0.0657

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	3.830e-06	1.000e-20
X9_P16	5.832e-06	1.000e-20
X19_P16	9.860e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16
D (output stable)	5.302e-05	5.040e-05	7.312e-05
GN (output stable)	7.025e-04	7.177e-04	8.918e-04
RN (output stable)	2.156e-05	2.758e-05	3.900e-05
D to Q	2.919e-03	4.151e-03	6.326e-03
GN to Q	4.217e-03	5.398e-03	7.785e-03
RN to Q	2.268e-03	3.219e-03	5.060e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

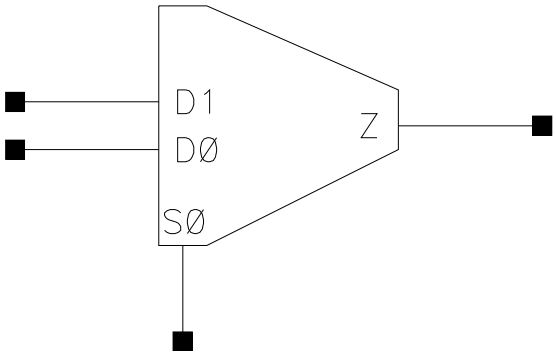
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.360	1.0880
X9_P16	0.800	1.496	1.1968
X14_P16	0.800	2.176	1.7408
X19_P16	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P16	X9_P16	X14_P16	X19_P16
D0	0.0006	0.0007	0.0009	0.0012
D1	0.0005	0.0007	0.0009	0.0012
S0	0.0010	0.0010	0.0012	0.0015

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D0 to Z ↓	0.0550	0.0507	5.0368	2.5486
D0 to Z ↑	0.0431	0.0413	8.1348	4.1097
D1 to Z ↓	0.0557	0.0495	5.0322	2.5458
D1 to Z ↑	0.0423	0.0388	8.1484	4.1043
S0 to Z ↓	0.0522	0.0443	5.0235	2.5403
S0 to Z ↑	0.0492	0.0440	8.1395	4.1058

	X14_P16	X19_P16	X14_P16	X19_P16
D0 to Z ↓	0.0555	0.0480	1.7619	1.2681
D0 to Z ↑	0.0443	0.0401	2.7718	2.0134
D1 to Z ↓	0.0564	0.0496	1.7601	1.2679
D1 to Z ↑	0.0417	0.0384	2.7682	2.0126
S0 to Z ↓	0.0529	0.0478	1.7560	1.2656
S0 to Z ↑	0.0518	0.0461	2.7702	2.0124

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	4.904e-06	1.000e-20
X9_P16	7.915e-06	1.000e-20
X14_P16	1.068e-05	1.000e-20
X19_P16	1.546e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X9_P16	X14_P16	X19_P16
D0 (output stable)	3.987e-04	7.525e-04	8.347e-04	1.000e-03
D1 (output stable)	3.775e-04	6.204e-04	8.789e-04	1.085e-03
S0 (output stable)	6.594e-04	5.922e-04	9.699e-04	1.130e-03
D0 to Z	1.739e-03	2.682e-03	4.276e-03	5.168e-03
D1 to Z	1.687e-03	2.510e-03	4.149e-03	5.119e-03
S0 to Z	2.125e-03	2.633e-03	4.712e-03	5.631e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

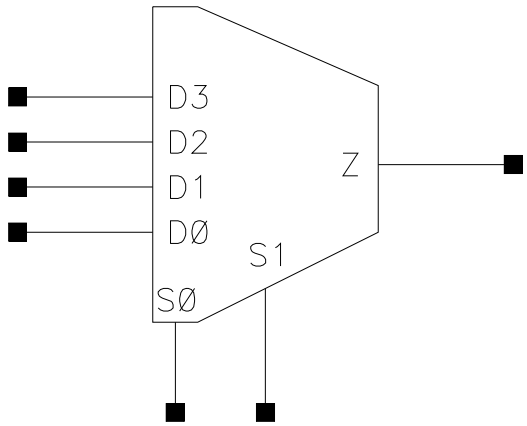
Pin Cycle (vdds)	X5_P16	X9_P16	X14_P16	X19_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.600	1.496	2.3936
X9_P16	1.600	1.768	2.8288
X13_P16	1.600	2.312	3.6992
X18_P16	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P16	X9_P16	X13_P16	X18_P16
D0	0.0004	0.0007	0.0009	0.0009
D1	0.0004	0.0005	0.0009	0.0009
D2	0.0004	0.0006	0.0009	0.0009
D3	0.0004	0.0005	0.0009	0.0009
S0	0.0013	0.0017	0.0022	0.0022
S1	0.0008	0.0009	0.0014	0.0013

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X9_P16	X4_P16	X9_P16
D0 to Z ↓	0.1244	0.1015	5.5977	2.7373
D0 to Z ↑	0.0751	0.0667	8.4194	4.1618
D1 to Z ↓	0.1226	0.1009	5.5874	2.7391
D1 to Z ↑	0.0752	0.0663	8.3965	4.1573
D2 to Z ↓	0.1147	0.1023	5.5276	2.7454
D2 to Z ↑	0.0724	0.0660	8.3535	4.1540
D3 to Z ↓	0.1164	0.1011	5.5439	2.7438
D3 to Z ↑	0.0735	0.0659	8.3549	4.1509
S0 to Z ↓	0.1310	0.1140	5.5639	2.7395
S0 to Z ↑	0.0905	0.0852	8.4075	4.1665
S1 to Z ↓	0.0825	0.0760	5.5584	2.7400
S1 to Z ↑	0.0682	0.0643	8.3850	4.1573
	X13_P16	X18_P16	X13_P16	X18_P16
D0 to Z ↓	0.0955	0.1041	1.8906	1.4158
D0 to Z ↑	0.0599	0.0648	2.7758	2.1000
D1 to Z ↓	0.0962	0.1048	1.8927	1.4173
D1 to Z ↑	0.0615	0.0664	2.7760	2.0995
D2 to Z ↓	0.0895	0.0975	1.8698	1.3998
D2 to Z ↑	0.0593	0.0642	2.7689	2.0964
D3 to Z ↓	0.0893	0.0973	1.8701	1.3998
D3 to Z ↑	0.0597	0.0646	2.7673	2.0942
S0 to Z ↓	0.1044	0.1127	1.8800	1.4082
S0 to Z ↑	0.0774	0.0823	2.7755	2.1009
S1 to Z ↓	0.0703	0.0785	1.8796	1.4078
S1 to Z ↑	0.0578	0.0627	2.7716	2.0981

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	4.764e-06	1.000e-20
X9_P16	7.450e-06	1.000e-20
X13_P16	1.228e-05	1.000e-20
X18_P16	1.380e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X9_P16	X13_P16	X18_P16
D0 (output stable)	2.806e-05	2.226e-05	6.046e-05	5.960e-05
D1 (output stable)	3.852e-05	3.918e-05	4.764e-05	4.726e-05
D2 (output stable)	3.650e-05	3.713e-05	5.247e-05	5.188e-05
D3 (output stable)	2.678e-05	3.768e-05	4.569e-05	4.557e-05
S0 (output stable)	8.674e-04	1.081e-03	1.770e-03	1.770e-03
S1 (output stable)	8.420e-04	9.578e-04	1.517e-03	1.517e-03
D0 to Z	2.239e-03	3.252e-03	5.248e-03	6.330e-03
D1 to Z	2.214e-03	3.239e-03	5.312e-03	6.397e-03
D2 to Z	2.103e-03	3.233e-03	5.057e-03	6.118e-03
D3 to Z	2.129e-03	3.232e-03	5.076e-03	6.136e-03
S0 to Z	3.199e-03	4.532e-03	7.252e-03	8.332e-03
S1 to Z	2.310e-03	3.315e-03	5.272e-03	6.332e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

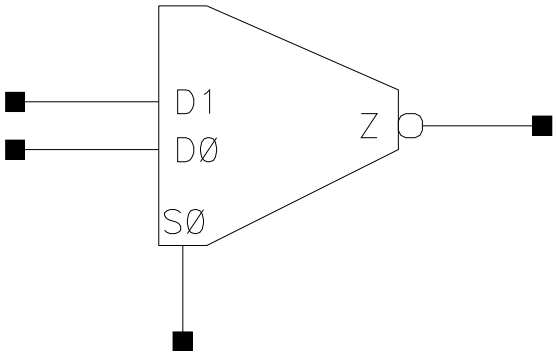
Pin Cycle (vdds)	X4_P16	X9_P16	X13_P16	X18_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P16	0.800	0.952	0.7616
X2_P16	0.800	0.952	0.7616
X6_P16	0.800	1.904	1.5232
X9_P16	0.800	2.448	1.9584
X12_P16	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P16	X2_P16	X6_P16	X9_P16
D0	0.0004	0.0005	0.0011	0.0016
D1	0.0004	0.0005	0.0011	0.0016
S0	0.0010	0.0013	0.0019	0.0027
	X12_P16			
D0	0.0021			
D1	0.0021			
S0	0.0031			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P16	X2_P16	X1_P16	X2_P16
D0 to Z ↓	0.0183	0.0176	14.6664	9.6880

D0 to Z ↑	0.0371	0.0282	34.8584	17.9587
D1 to Z ↓	0.0174	0.0163	14.4551	9.5616
D1 to Z ↑	0.0376	0.0296	34.9061	18.1047
S0 to Z ↓	0.0340	0.0230	14.4812	9.6300
S0 to Z ↑	0.0392	0.0246	34.7237	18.0193
	X6_P16	**X9_P16**	**X6_P16**	**X9_P16**
D0 to Z ↓	0.0197	0.0182	4.2658	2.8733
D0 to Z ↑	0.0298	0.0283	7.3209	5.0846
D1 to Z ↓	0.0186	0.0179	4.2055	2.8908
D1 to Z ↑	0.0318	0.0294	7.5377	4.9523
S0 to Z ↓	0.0271	0.0231	4.2272	2.8777
S0 to Z ↑	0.0282	0.0248	7.4182	5.0189
	X12_P16		**X12_P16**	
D0 to Z ↓	0.0189		2.1957	
D0 to Z ↑	0.0285		3.8311	
D1 to Z ↓	0.0178		2.1895	
D1 to Z ↑	0.0291		3.7239	
S0 to Z ↓	0.0253		2.1880	
S0 to Z ↑	0.0263		3.7749	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X1_P16	1.833e-06	1.000e-20
X2_P16	3.377e-06	1.000e-20
X6_P16	6.705e-06	1.000e-20
X9_P16	1.035e-05	1.000e-20
X12_P16	1.252e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X1_P16	X2_P16	X6_P16	X9_P16
D0 (output stable)	6.529e-06	1.506e-05	4.943e-05	6.974e-05
D1 (output stable)	6.302e-06	1.651e-05	5.218e-05	7.532e-05
S0 (output stable)	6.427e-04	6.865e-04	1.277e-03	1.891e-03
D0 to Z	5.572e-04	7.326e-04	1.956e-03	2.633e-03
D1 to Z	5.535e-04	7.291e-04	1.987e-03	2.705e-03
S0 to Z	1.129e-03	1.154e-03	2.570e-03	3.538e-03
	X12_P16			
D0 (output stable)	9.234e-05			
D1 (output stable)	9.318e-05			
S0 (output stable)	2.271e-03			
D0 to Z	3.569e-03			
D1 to Z	3.548e-03			
S0 to Z	4.529e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X1_P16	X2_P16	X6_P16	X9_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

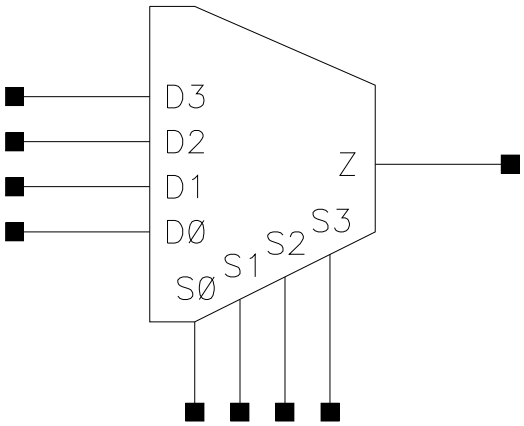
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P16			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.600	0.952	1.5232
X15_P16	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
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0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P16	X15_P16
D0	0.0005	0.0014
D1	0.0006	0.0011
D2	0.0006	0.0014
D3	0.0005	0.0011
S0	0.0005	0.0012
S1	0.0005	0.0014
S2	0.0006	0.0012
S3	0.0006	0.0013

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X15_P16	X4_P16	X15_P16
D0 to Z ↓	0.0614	0.0657	8.3396	2.1931
D0 to Z ↑	0.0512	0.0483	7.6934	1.9417
D1 to Z ↓	0.0553	0.0580	8.3342	2.1920
D1 to Z ↑	0.0442	0.0424	7.6578	1.9322
D2 to Z ↓	0.0598	0.0631	8.3567	2.1967
D2 to Z ↑	0.0496	0.0453	7.7242	1.9517
D3 to Z ↓	0.0530	0.0556	8.3435	2.1937
D3 to Z ↑	0.0425	0.0397	7.6901	1.9424
S0 to Z ↓	0.0587	0.0600	8.3382	2.1917
S0 to Z ↑	0.0536	0.0481	7.6969	1.9418
S1 to Z ↓	0.0521	0.0530	8.3355	2.1904
S1 to Z ↑	0.0461	0.0424	7.6591	1.9309
S2 to Z ↓	0.0578	0.0580	8.3524	2.1940
S2 to Z ↑	0.0520	0.0455	7.7241	1.9522
S3 to Z ↓	0.0518	0.0507	8.3446	2.1907
S3 to Z ↑	0.0453	0.0395	7.6853	1.9415

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	5.569e-06	1.000e-20
X15_P16	1.644e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X15_P16
D0 (output stable)	3.194e-04	9.080e-04
D1 (output stable)	2.484e-04	7.053e-04
D2 (output stable)	3.199e-04	8.998e-04
D3 (output stable)	2.501e-04	6.991e-04
S0 (output stable)	3.035e-04	8.835e-04
S1 (output stable)	2.356e-04	7.030e-04
S2 (output stable)	3.105e-04	8.852e-04
S3 (output stable)	2.416e-04	7.033e-04
D0 to Z	2.412e-03	6.870e-03
D1 to Z	2.032e-03	5.829e-03
D2 to Z	2.198e-03	6.029e-03
D3 to Z	1.821e-03	5.002e-03
S0 to Z	2.322e-03	6.375e-03
S1 to Z	1.948e-03	5.388e-03
S2 to Z	2.127e-03	5.584e-03
S3 to Z	1.760e-03	4.550e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

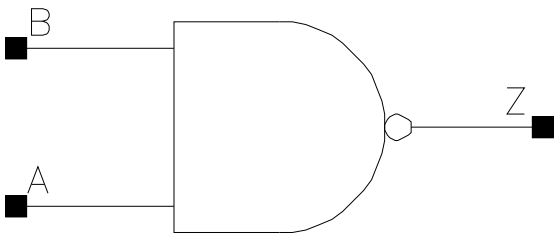
Pin Cycle (vdds)	X4_P16	X15_P16
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P16	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P16	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P16	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P16	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P16	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P16	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P16	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P16	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P16	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P16	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P16	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P16	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P16	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P16	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P16	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P16	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P16	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P16	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P16	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P16	C8T28SOI_LL_-NAND2X4_P16	C8T28SOI_LL_-NAND2X8_P16	C8T28SOI_LL_-NAND2X12_P16
A	0.0004	0.0005	0.0011	0.0016
B	0.0004	0.0005	0.0010	0.0014
	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X24_P16	C8T28SOI_-LLBR0P8_-NAND2X4_P16
A	0.0020	0.0025	0.0007	0.0007
B	0.0019	0.0024	0.0007	0.0005
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	C8T28SOI_-LLBR0P8_-NAND2X12_P16	C8T28SOI_-LLBR0P8_-NAND2X16_P16	C8T28SOI_LLS_-NAND2X8_P16
A	0.0011	0.0016	0.0021	0.0011
B	0.0009	0.0014	0.0018	0.0009
	C8T28SOI_LLS_-NAND2X15_P16	C8T28SOI_LLS_-NAND2X23_P16	C8T28SOI_LLS_-NAND2X31_P16	C8T28SOIDV_LL_-NAND2X9_P16
A	0.0021	0.0032	0.0042	0.0011
B	0.0019	0.0028	0.0038	0.0012
	C8T28SOIDV_LL_-NAND2X18_P16	C8T28SOIDV_LL_-NAND2X27_P16	C8T28SOIDV_LL_-NAND2X36_P16	
A	0.0023	0.0034	0.0045	
B	0.0021	0.0031	0.0041	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-NAND2X2_P16	**C8T28SOI_LL_-NAND2X4_P16**	**C8T28SOI_LL_-NAND2X2_P16**	**C8T28SOI_LL_-NAND2X4_P16**
A to Z ↓	0.0140	0.0121	15.9319	8.4488
A to Z ↑	0.0213	0.0176	15.9425	8.1487
B to Z ↓	0.0161	0.0131	16.0206	8.4981
B to Z ↑	0.0199	0.0155	15.9880	8.2378
	C8T28SOI_LL_-NAND2X8_P16	**C8T28SOI_LL_-NAND2X12_P16**	**C8T28SOI_LL_-NAND2X8_P16**	**C8T28SOI_LL_-NAND2X12_P16**
A to Z ↓	0.0138	0.0132	4.2360	2.8893
A to Z ↑	0.0180	0.0175	3.8838	2.6315
B to Z ↓	0.0120	0.0126	4.2690	2.9126
B to Z ↑	0.0139	0.0143	3.9079	2.6590

	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16
A to Z ↓	0.0136	0.0133	2.1875	1.7650
A to Z ↑	0.0175	0.0175	1.9757	1.5937
B to Z ↓	0.0121	0.0126	2.2074	1.7807
B to Z ↑	0.0137	0.0142	1.9951	1.6107
	C8T28SOI_LL_-NAND2X24_P16	**C8T28SOI_-LLBR0P8_-NAND2X4_P16**	**C8T28SOI_LL_-NAND2X24_P16**	**C8T28SOI_-LLBR0P8_-NAND2X4_P16**
A to Z ↓	0.0529	0.0106	0.9775	5.8860
A to Z ↑	0.0529	0.0224	1.5821	10.4681
B to Z ↓	0.0541	0.0108	0.9776	5.9449
B to Z ↑	0.0506	0.0188	1.5822	10.4964
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	**C8T28SOI_-LLBR0P8_-NAND2X12_P16**	**C8T28SOI_-LLBR0P8_-NAND2X8_P16**	**C8T28SOI_-LLBR0P8_-NAND2X12_P16**
A to Z ↓	0.0118	0.0116	3.1846	2.1752
A to Z ↑	0.0226	0.0226	5.2560	3.5429
B to Z ↓	0.0093	0.0102	3.2259	2.2008
B to Z ↑	0.0163	0.0172	5.2892	3.5632
	C8T28SOI_-LLBR0P8_-NAND2X16_P16	**C8T28SOI_LLS_-NAND2X8_P16**	**C8T28SOI_-LLBR0P8_-NAND2X16_P16**	**C8T28SOI_LLS_-NAND2X8_P16**
A to Z ↓	0.0114	0.0139	1.6557	4.2244
A to Z ↑	0.0218	0.0181	2.6520	3.9194
B to Z ↓	0.0090	0.0120	1.6775	4.2556
B to Z ↑	0.0156	0.0140	2.6779	3.9543
	C8T28SOI_LLS_-NAND2X15_P16	**C8T28SOI_LLS_-NAND2X23_P16**	**C8T28SOI_LLS_-NAND2X15_P16**	**C8T28SOI_LLS_-NAND2X23_P16**
A to Z ↓	0.0137	0.0137	2.1840	1.4718
A to Z ↑	0.0176	0.0175	1.9533	1.3029
B to Z ↓	0.0122	0.0124	2.2031	1.4847
B to Z ↑	0.0137	0.0138	1.9665	1.3119
	C8T28SOI_LLS_-NAND2X31_P16	**C8T28SOIDV_LL_-NAND2X9_P16**	**C8T28SOI_LLS_-NAND2X31_P16**	**C8T28SOIDV_LL_-NAND2X9_P16**
A to Z ↓	0.0136	0.0115	1.1124	3.2059
A to Z ↑	0.0174	0.0185	0.9797	3.8265
B to Z ↓	0.0125	0.0117	1.1223	3.2328
B to Z ↑	0.0138	0.0157	0.9873	3.8767
	C8T28SOIDV_LL_-NAND2X18_P16	**C8T28SOIDV_LL_-NAND2X27_P16**	**C8T28SOIDV_LL_-NAND2X18_P16**	**C8T28SOIDV_LL_-NAND2X27_P16**
A to Z ↓	0.0128	0.0125	1.6162	1.1001
A to Z ↑	0.0192	0.0191	1.9197	1.2903
B to Z ↓	0.0108	0.0117	1.6339	1.1110
B to Z ↑	0.0145	0.0153	1.9319	1.2983
	C8T28SOIDV_LL_-NAND2X36_P16		**C8T28SOIDV_LL_-NAND2X36_P16**	
A to Z ↓	0.0129		0.8288	
A to Z ↑	0.0190		0.9668	
B to Z ↓	0.0109		0.8380	
B to Z ↑	0.0144		0.9736	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P16	8.060e-07	1.000e-20
C8T28SOI_LL_NAND2X4_P16	1.662e-06	1.000e-20
C8T28SOI_LL_NAND2X8_P16	3.251e-06	1.000e-20
C8T28SOI_LL_NAND2X12_P16	4.674e-06	1.000e-20
C8T28SOI_LL_NAND2X15_P16	6.102e-06	1.000e-20
C8T28SOI_LL_NAND2X19_P16	7.530e-06	1.000e-20
C8T28SOI_LL_NAND2X24_P16	1.137e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P16	1.881e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P16	3.354e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_-P16	4.776e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_-P16	6.204e-06	1.000e-20
C8T28SOI_LLS_NAND2X8_P16	3.251e-06	1.000e-20
C8T28SOI_LLS_NAND2X15_P16	6.102e-06	1.000e-20
C8T28SOI_LLS_NAND2X23_P16	8.959e-06	1.000e-20
C8T28SOI_LLS_NAND2X31_P16	1.182e-05	1.000e-20
C8T28SOIDV_LL_NAND2X9_P16	4.028e-06	1.000e-20
C8T28SOIDV_LL_NAND2X18_P16	7.584e-06	1.000e-20
C8T28SOIDV_LL_NAND2X27_P16	1.092e-05	1.000e-20
C8T28SOIDV_LL_NAND2X36_P16	1.427e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P16	C8T28SOI_LL_-NAND2X4_P16	C8T28SOI_LL_-NAND2X8_P16	C8T28SOI_LL_-NAND2X12_P16
A (output stable)	4.510e-06	8.845e-06	4.250e-05	5.363e-05
B (output stable)	9.768e-06	1.873e-05	1.738e-04	1.699e-04
A to Z	3.395e-04	5.012e-04	1.148e-03	1.624e-03
B to Z	2.880e-04	3.952e-04	7.294e-04	1.143e-03
	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X24_P16	C8T28SOI_-LLBR0P8_-NAND2X4_P16
A (output stable)	7.966e-05	8.772e-05	1.033e-05	1.232e-05
B (output stable)	3.020e-04	2.756e-04	2.077e-05	2.617e-05
A to Z	2.198e-03	2.689e-03	5.610e-03	5.871e-04
B to Z	1.432e-03	1.883e-03	5.497e-03	4.271e-04
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	C8T28SOI_-LLBR0P8_-NAND2X12_P16	C8T28SOI_-LLBR0P8_-NAND2X16_P16	C8T28SOI_LLS_-NAND2X8_P16
A (output stable)	5.151e-05	6.187e-05	9.770e-05	4.328e-05
B (output stable)	2.072e-04	1.973e-04	3.554e-04	1.846e-04
A to Z	1.225e-03	1.811e-03	2.281e-03	1.157e-03
B to Z	6.838e-04	1.150e-03	1.280e-03	7.366e-04
	C8T28SOI_LLS_-NAND2X15_P16	C8T28SOI_LLS_-NAND2X23_P16	C8T28SOI_LLS_-NAND2X31_P16	C8T28SOIDV_LL_-NAND2X9_P16
A (output stable)	8.317e-05	1.206e-04	1.536e-04	2.309e-05
B (output stable)	3.136e-04	4.407e-04	5.414e-04	4.831e-05
A to Z	2.227e-03	3.318e-03	4.377e-03	1.200e-03
B to Z	1.455e-03	2.205e-03	2.956e-03	9.074e-04
	C8T28SOIDV_LL_-NAND2X18_P16	C8T28SOIDV_LL_-NAND2X27_P16	C8T28SOIDV_LL_-NAND2X36_P16	
A (output stable)	9.517e-05	1.118e-04	1.900e-04	

B (output stable)	4.063e-04	3.182e-04	7.992e-04	
A to Z	2.582e-03	3.787e-03	5.092e-03	
B to Z	1.603e-03	2.662e-03	3.192e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

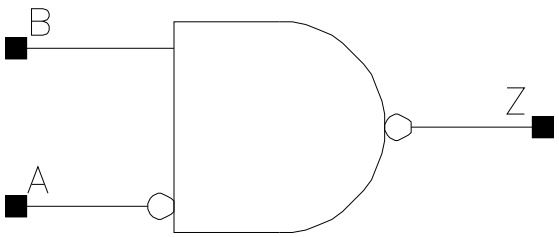
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P16	C8T28SOI_LL_-NAND2X4_P16	C8T28SOI_LL_-NAND2X8_P16	C8T28SOI_LL_-NAND2X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X24_P16	C8T28SOI_-LLBR0P8_-NAND2X4_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	C8T28SOI_-LLBR0P8_-NAND2X12_P16	C8T28SOI_-LLBR0P8_-NAND2X16_P16	C8T28SOI_LLS_-NAND2X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P16	C8T28SOI_LLS_-NAND2X23_P16	C8T28SOI_LLS_-NAND2X31_P16	C8T28SOIDV_LL_-NAND2X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P16	C8T28SOIDV_LL_-NAND2X27_P16	C8T28SOIDV_LL_-NAND2X36_P16	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.544	0.4352
X4_P16	0.800	0.680	0.5440
X9_P16	1.600	0.544	0.8704
X13_P16	1.600	0.816	1.3056
X17_P16	1.600	0.816	1.3056
X23_P16	0.800	2.312	1.8496
X27_P16	1.600	1.088	1.7408
X31_P16	0.800	2.992	2.3936
X36_P16	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P16	X4_P16	X9_P16	X13_P16
A	0.0005	0.0006	0.0010	0.0009
B	0.0004	0.0005	0.0011	0.0017
	X17_P16	X23_P16	X27_P16	X31_P16
A	0.0009	0.0019	0.0015	0.0026
B	0.0020	0.0028	0.0031	0.0037
	X36_P16			
A	0.0015			
B	0.0041			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X4_P16**	**X2_P16**	**X4_P16**
A to Z ↓	0.0382	0.0395	16.0608	8.5482
A to Z ↑	0.0301	0.0302	15.7790	8.0193
B to Z ↓	0.0164	0.0132	16.2470	8.6466
B to Z ↑	0.0201	0.0154	15.9911	8.2331
	X9_P16	**X13_P16**	**X9_P16**	**X13_P16**
A to Z ↓	0.0384	0.0471	3.2800	2.1029
A to Z ↑	0.0291	0.0350	3.8033	2.5766
B to Z ↓	0.0120	0.0119	3.3305	2.1275
B to Z ↑	0.0157	0.0162	3.8891	2.6664
	X17_P16	**X23_P16**	**X17_P16**	**X23_P16**
A to Z ↓	0.0515	0.0365	1.6490	1.4639
A to Z ↑	0.0365	0.0291	1.9524	1.3088
B to Z ↓	0.0114	0.0120	1.6631	1.4863
B to Z ↑	0.0153	0.0136	2.0190	1.3379
	X27_P16	**X31_P16**	**X27_P16**	**X31_P16**
A to Z ↓	0.0434	0.0364	1.1023	1.1058
A to Z ↑	0.0324	0.0289	1.2857	0.9638
B to Z ↓	0.0112	0.0122	1.1173	1.1226
B to Z ↑	0.0146	0.0137	1.3026	1.0066
	X36_P16		**X36_P16**	
A to Z ↓	0.0500		0.8353	
A to Z ↑	0.0366		0.9664	
B to Z ↓	0.0110		0.8435	
B to Z ↑	0.0142		0.9779	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P16	1.426e-06	1.000e-20
X4_P16	2.372e-06	1.000e-20
X9_P16	5.747e-06	1.000e-20
X13_P16	7.065e-06	1.000e-20
X17_P16	9.005e-06	1.000e-20
X23_P16	1.340e-05	1.000e-20
X27_P16	1.420e-05	1.000e-20
X31_P16	1.757e-05	1.000e-20
X36_P16	1.759e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P16	X4_P16	X9_P16	X13_P16
A (output stable)	5.231e-04	6.798e-04	1.318e-03	1.950e-03
B (output stable)	9.867e-06	1.875e-05	5.071e-05	1.540e-04
A to Z	8.915e-04	1.226e-03	2.660e-03	4.222e-03
B to Z	2.910e-04	3.922e-04	9.227e-04	1.410e-03
	X17_P16	X23_P16	X27_P16	X31_P16
A (output stable)	2.229e-03	3.295e-03	3.451e-03	4.363e-03
B (output stable)	1.819e-04	3.766e-04	3.379e-04	5.003e-04
A to Z	5.040e-03	6.955e-03	7.454e-03	9.243e-03
B to Z	1.713e-03	2.189e-03	2.472e-03	2.907e-03
	X36_P16			
A (output stable)	4.528e-03			

B (output stable)	5.526e-04			
A to Z	9.872e-03			
B to Z	3.147e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

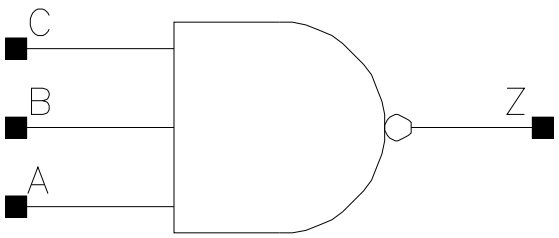
Pin Cycle (vdds)	X2_P16	X4_P16	X9_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P16	X23_P16	X27_P16	X31_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P16	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P16	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P16	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P16	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P16	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P16	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P16	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P16	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P16	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P16	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P16	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P16	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P16	C8T28SOI_LL_-NAND3X7_P16	C8T28SOI_LL_-NAND3X10_P16	C8T28SOI_LL_-NAND3X14_P16
A	0.0005	0.0010	0.0016	0.0021
B	0.0005	0.0010	0.0015	0.0019
C	0.0005	0.0010	0.0014	0.0018
	C8T28SOI_LL_-NAND3X20_P16	C8T28SOI_LL_-NAND3X27_P16	C8T28SOI_-LLBR0P6_-NAND3X3_P16	C8T28SOI_-LLBR0P6_-NAND3X7_P16
A	0.0031	0.0041	0.0007	0.0011
B	0.0029	0.0039	0.0005	0.0010
C	0.0027	0.0037	0.0005	0.0009
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	C8T28SOI_-LLBR0P6_-NAND3X14_P16	C8T28SOI_-LLBR0P6_-NAND3X20_P16	C8T28SOI_-LLBR0P6_-NAND3X27_P16
A	0.0016	0.0021	0.0031	0.0042
B	0.0015	0.0019	0.0029	0.0038
C	0.0014	0.0018	0.0027	0.0036

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND3X3_P16	**C8T28SOI_LL_-NAND3X7_P16**	**C8T28SOI_LL_-NAND3X3_P16**	**C8T28SOI_LL_-NAND3X7_P16**
A to Z ↓	0.0186	0.0212	12.4519	6.1472
A to Z ↑	0.0220	0.0227	8.1933	3.9789
B to Z ↓	0.0187	0.0200	12.4744	6.1596
B to Z ↑	0.0203	0.0207	8.2184	3.9847
C to Z ↓	0.0190	0.0176	12.5066	6.1766
C to Z ↑	0.0182	0.0171	8.2780	3.9018
	C8T28SOI_LL_-NAND3X10_P16	**C8T28SOI_LL_-NAND3X14_P16**	**C8T28SOI_LL_-NAND3X10_P16**	**C8T28SOI_LL_-NAND3X14_P16**
A to Z ↓	0.0201	0.0206	4.2433	3.1897
A to Z ↑	0.0215	0.0219	2.5917	2.0006
B to Z ↓	0.0196	0.0195	4.2515	3.1958
B to Z ↑	0.0197	0.0198	2.6502	2.0005
C to Z ↓	0.0176	0.0173	4.2649	3.2063
C to Z ↑	0.0165	0.0164	2.6650	1.9895
	C8T28SOI_LL_-NAND3X20_P16	**C8T28SOI_LL_-NAND3X27_P16**	**C8T28SOI_LL_-NAND3X20_P16**	**C8T28SOI_LL_-NAND3X27_P16**
A to Z ↓	0.0200	0.0201	2.1658	1.6428
A to Z ↑	0.0212	0.0212	1.3025	0.9806
B to Z ↓	0.0194	0.0195	2.1704	1.6460
B to Z ↑	0.0193	0.0192	1.3036	0.9801
C to Z ↓	0.0171	0.0173	2.1776	1.6518
C to Z ↑	0.0160	0.0160	1.3306	1.0010
	C8T28SOI_-LLBR0P6_-NAND3X3_P16	**C8T28SOI_-LLBR0P6_-NAND3X7_P16**	**C8T28SOI_-LLBR0P6_-NAND3X3_P16**	**C8T28SOI_-LLBR0P6_-NAND3X7_P16**
A to Z ↓	0.0141	0.0171	7.6958	4.1890
A to Z ↑	0.0311	0.0336	12.5211	6.3464
B to Z ↓	0.0135	0.0156	7.7394	4.2063
B to Z ↑	0.0270	0.0288	12.5085	6.3524

C to Z ↓	0.0128	0.0124	7.8012	4.2358
C to Z ↑	0.0224	0.0217	12.5872	6.3151
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	**C8T28SOI_-LLBR0P6_-NAND3X14_P16**	**C8T28SOI_-LLBR0P6_-NAND3X10_P16**	**C8T28SOI_-LLBR0P6_-NAND3X14_P16**
A to Z ↓	0.0158	0.0167	2.8250	2.1333
A to Z ↑	0.0316	0.0324	4.2342	3.1966
B to Z ↓	0.0144	0.0147	2.8393	2.1431
B to Z ↑	0.0268	0.0273	4.2423	3.2031
C to Z ↓	0.0120	0.0115	2.8622	2.1616
C to Z ↑	0.0206	0.0201	4.2690	3.2014
	C8T28SOI_-LLBR0P6_-NAND3X20_P16	**C8T28SOI_-LLBR0P6_-NAND3X27_P16**	**C8T28SOI_-LLBR0P6_-NAND3X20_P16**	**C8T28SOI_-LLBR0P6_-NAND3X27_P16**
A to Z ↓	0.0159	0.0160	1.4421	1.1002
A to Z ↑	0.0316	0.0315	2.1285	1.6018
B to Z ↓	0.0146	0.0145	1.4492	1.1059
B to Z ↑	0.0268	0.0266	2.1307	1.6025
C to Z ↓	0.0114	0.0115	1.4619	1.1152
C to Z ↑	0.0196	0.0196	2.1448	1.6113

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P16	1.347e-06	1.000e-20
C8T28SOI_LL_NAND3X7_P16	2.822e-06	1.000e-20
C8T28SOI_LL_NAND3X10_P16	3.838e-06	1.000e-20
C8T28SOI_LL_NAND3X14_P16	5.222e-06	1.000e-20
C8T28SOI_LL_NAND3X20_P16	7.623e-06	1.000e-20
C8T28SOI_LL_NAND3X27_P16	1.002e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P16	1.614e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P16	3.154e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_-P16	4.160e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_-P16	5.716e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_-P16	8.278e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_-P16	1.083e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P16	C8T28SOI_LL_-NAND3X7_P16	C8T28SOI_LL_-NAND3X10_P16	C8T28SOI_LL_-NAND3X14_P16
A (output stable)	1.057e-05	4.326e-05	5.562e-05	8.159e-05
B (output stable)	2.036e-05	1.026e-04	1.384e-04	1.928e-04
C (output stable)	5.116e-05	2.658e-04	3.298e-04	4.847e-04
A to Z	7.749e-04	1.804e-03	2.481e-03	3.388e-03
B to Z	6.615e-04	1.450e-03	1.995e-03	2.701e-03
C to Z	5.533e-04	1.070e-03	1.492e-03	1.991e-03
	C8T28SOI_LL_-NAND3X20_P16	C8T28SOI_LL_-NAND3X27_P16	C8T28SOI_-LLBR0P6_-NAND3X3_P16	C8T28SOI_-LLBR0P6_-NAND3X7_P16

A (output stable)	1.083e-04	1.441e-04	1.665e-05	5.807e-05
B (output stable)	2.696e-04	3.602e-04	3.324e-05	1.324e-04
C (output stable)	7.285e-04	9.503e-04	8.522e-05	3.575e-04
A to Z	4.882e-03	6.486e-03	8.689e-04	2.032e-03
B to Z	3.927e-03	5.202e-03	6.819e-04	1.523e-03
C to Z	2.833e-03	3.784e-03	4.888e-04	9.640e-04
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	C8T28SOI_-LLBR0P6_-NAND3X14_P16	C8T28SOI_-LLBR0P6_-NAND3X20_P16	C8T28SOI_-LLBR0P6_-NAND3X27_P16
A (output stable)	7.427e-05	1.187e-04	1.524e-04	2.079e-04
B (output stable)	1.763e-04	2.761e-04	3.717e-04	4.963e-04
C (output stable)	4.428e-04	6.891e-04	9.816e-04	1.266e-03
A to Z	2.732e-03	3.822e-03	5.468e-03	7.248e-03
B to Z	1.982e-03	2.753e-03	3.960e-03	5.202e-03
C to Z	1.273e-03	1.658e-03	2.362e-03	3.135e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

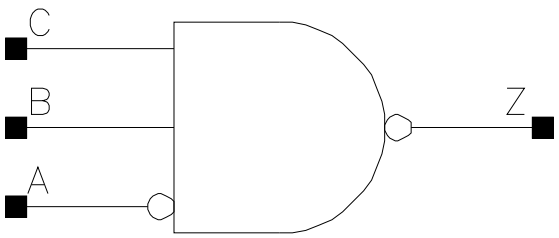
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P16	C8T28SOI_LL_-NAND3X7_P16	C8T28SOI_LL_-NAND3X10_P16	C8T28SOI_LL_-NAND3X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P16	C8T28SOI_LL_-NAND3X27_P16	C8T28SOI_-LLBR0P6_-NAND3X3_P16	C8T28SOI_-LLBR0P6_-NAND3X7_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	C8T28SOI_-LLBR0P6_-NAND3X14_P16	C8T28SOI_-LLBR0P6_-NAND3X20_P16	C8T28SOI_-LLBR0P6_-NAND3X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X7_P16	0.800	1.360	1.0880
X10_P16	0.800	1.632	1.3056
X14_P16	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X10_P16	X14_P16
A	0.0006	0.0010	0.0008	0.0008
B	0.0005	0.0010	0.0015	0.0020
C	0.0005	0.0010	0.0014	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0482	0.0462	12.4930	6.1939
A to Z ↑	0.0344	0.0343	8.0253	3.8645
B to Z ↓	0.0182	0.0196	12.5581	6.2215
B to Z ↑	0.0197	0.0199	8.2270	3.9085
C to Z ↓	0.0184	0.0169	12.5939	6.2384
C to Z ↑	0.0177	0.0162	8.2955	3.9083
	X10_P16	**X14_P16**	**X10_P16**	**X14_P16**
A to Z ↓	0.0510	0.0553	4.2397	3.2120

A to Z ↑	0.0378	0.0413	2.6236	1.9644
B to Z ↓	0.0196	0.0189	4.2538	3.2196
B to Z ↑	0.0196	0.0192	2.6530	1.9854
C to Z ↓	0.0174	0.0166	4.2677	3.2302
C to Z ↑	0.0164	0.0157	2.6698	1.9918

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	1.986e-06	1.000e-20
X7_P16	4.314e-06	1.000e-20
X10_P16	5.324e-06	1.000e-20
X14_P16	6.719e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	6.969e-04	1.277e-03	1.648e-03	2.012e-03
B (output stable)	2.119e-05	8.473e-05	1.443e-04	1.754e-04
C (output stable)	5.191e-05	2.734e-04	3.465e-04	4.796e-04
A to Z	1.475e-03	3.141e-03	4.361e-03	5.589e-03
B to Z	6.236e-04	1.378e-03	1.992e-03	2.575e-03
C to Z	5.136e-04	9.812e-04	1.475e-03	1.858e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

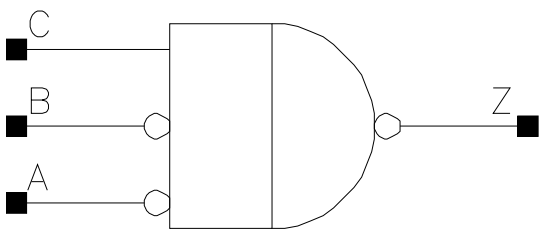
Pin Cycle (vdds)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	0.816	0.6528
X8_P16	0.800	1.088	0.8704
X12_P16	0.800	1.632	1.3056
X15_P16	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X12_P16	X15_P16
A	0.0007	0.0007	0.0012	0.0011
B	0.0007	0.0007	0.0012	0.0011
C	0.0005	0.0010	0.0014	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0428	0.0534	7.9909	4.2364
A to Z ↑	0.0286	0.0331	7.6647	3.8324
B to Z ↓	0.0426	0.0532	7.9908	4.2347
B to Z ↑	0.0270	0.0315	7.6619	3.8329
C to Z ↓	0.0135	0.0122	8.0616	4.2582
C to Z ↑	0.0158	0.0141	7.6891	3.9326
	X12_P16	**X15_P16**	**X12_P16**	**X15_P16**
A to Z ↓	0.0486	0.0534	2.8791	2.1949
A to Z ↑	0.0305	0.0358	2.5593	1.9270
B to Z ↓	0.0451	0.0501	2.8794	2.1951

B to Z ↑	0.0280	0.0330	2.5541	1.9244
C to Z ↓	0.0131	0.0121	2.9054	2.2105
C to Z ↑	0.0148	0.0136	2.6574	1.9631

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	3.275e-06	1.000e-20
X8_P16	4.462e-06	1.000e-20
X12_P16	7.045e-06	1.000e-20
X15_P16	7.860e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	3.721e-04	5.155e-04	8.751e-04	1.003e-03
B (output stable)	3.241e-04	4.666e-04	7.155e-04	8.476e-04
C (output stable)	2.048e-05	1.773e-04	1.742e-04	2.881e-04
A to Z	1.709e-03	2.842e-03	4.501e-03	5.430e-03
B to Z	1.548e-03	2.681e-03	3.954e-03	4.898e-03
C to Z	4.473e-04	7.545e-04	1.245e-03	1.461e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

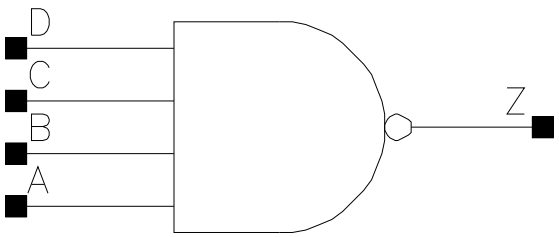
Pin Cycle (vdds)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.224	0.9792
X10_P16	0.800	1.360	1.0880
X14_P16	0.800	1.904	1.5232
X18_P16	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X18_P16
A	0.0004	0.0005	0.0005	0.0006
B	0.0005	0.0005	0.0006	0.0008
C	0.0004	0.0004	0.0005	0.0006
D	0.0005	0.0005	0.0005	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0746	0.0686	4.7295	2.3815
A to Z ↑	0.0578	0.0588	7.7242	3.8912
B to Z ↓	0.0770	0.0713	4.7307	2.3814
B to Z ↑	0.0562	0.0583	7.7181	3.8903
C to Z ↓	0.0768	0.0696	4.7302	2.3835
C to Z ↑	0.0600	0.0621	7.7115	3.8933

D to Z ↓	0.0800	0.0727	4.7266	2.3826
D to Z ↑	0.0598	0.0621	7.7110	3.8946
	X14_P16	**X18_P16**	**X14_P16**	**X18_P16**
A to Z ↓	0.0736	0.0676	1.6417	1.3327
A to Z ↑	0.0582	0.0566	2.6539	2.1070
B to Z ↓	0.0762	0.0699	1.6411	1.3328
B to Z ↑	0.0566	0.0556	2.6559	2.1061
C to Z ↓	0.0699	0.0616	1.6398	1.3324
C to Z ↑	0.0589	0.0556	2.6500	2.1055
D to Z ↓	0.0725	0.0635	1.6393	1.3326
D to Z ↑	0.0582	0.0537	2.6483	2.1060

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	3.691e-06	1.000e-20
X10_P16	5.754e-06	1.000e-20
X14_P16	8.141e-06	1.000e-20
X18_P16	1.034e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	2.692e-04	3.323e-04	4.890e-04	5.369e-04
B (output stable)	2.516e-04	3.131e-04	4.630e-04	5.072e-04
C (output stable)	2.883e-04	3.231e-04	5.027e-04	4.942e-04
D (output stable)	2.709e-04	3.053e-04	4.735e-04	4.564e-04
A to Z	2.064e-03	2.955e-03	4.604e-03	5.351e-03
B to Z	2.014e-03	2.903e-03	4.529e-03	5.270e-03
C to Z	2.180e-03	3.006e-03	4.358e-03	4.921e-03
D to Z	2.144e-03	2.961e-03	4.287e-03	4.826e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

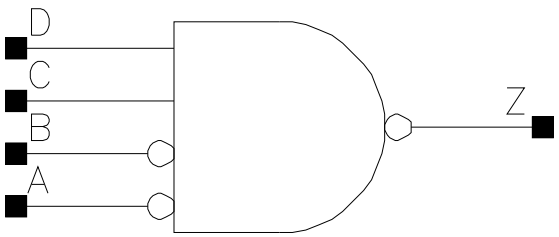
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.952	0.7616
X7_P16	0.800	1.360	1.0880
X10_P16	0.800	2.040	1.6320
X14_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P16	X7_P16	X10_P16	X14_P16
A	0.0007	0.0007	0.0013	0.0011
B	0.0007	0.0007	0.0013	0.0012
C	0.0007	0.0010	0.0015	0.0019
D	0.0005	0.0010	0.0014	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X7_P16	X3_P16	X7_P16
A to Z ↓	0.0496	0.0587	11.8188	6.2052
A to Z ↑	0.0316	0.0360	7.7304	3.8740
B to Z ↓	0.0486	0.0580	11.8223	6.2064
B to Z ↑	0.0296	0.0341	7.7232	3.8744
C to Z ↓	0.0187	0.0194	11.8841	6.2162
C to Z ↑	0.0203	0.0198	7.8557	3.9128

D to Z ↓	0.0181	0.0167	11.9019	6.2338
D to Z ↑	0.0177	0.0161	7.8379	3.9095
	X10_P16	**X14_P16**	**X10_P16**	**X14_P16**
A to Z ↓	0.0545	0.0599	4.2349	3.2220
A to Z ↑	0.0330	0.0412	2.6057	1.9385
B to Z ↓	0.0508	0.0574	4.2358	3.2218
B to Z ↑	0.0304	0.0387	2.5997	1.9347
C to Z ↓	0.0194	0.0189	4.2459	3.2248
C to Z ↑	0.0195	0.0192	2.6539	1.9876
D to Z ↓	0.0173	0.0168	4.2596	3.2356
D to Z ↑	0.0164	0.0158	2.6709	1.9937

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	2.864e-06	1.000e-20
X7_P16	3.787e-06	1.000e-20
X10_P16	6.187e-06	1.000e-20
X14_P16	6.665e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	4.601e-04	6.345e-04	1.111e-03	1.311e-03
B (output stable)	3.955e-04	5.699e-04	8.957e-04	1.120e-03
C (output stable)	5.219e-05	1.008e-04	1.578e-04	2.096e-04
D (output stable)	1.140e-04	3.095e-04	3.874e-04	5.443e-04
A to Z	2.017e-03	3.326e-03	5.197e-03	6.595e-03
B to Z	1.858e-03	3.168e-03	4.658e-03	6.112e-03
C to Z	6.754e-04	1.369e-03	1.964e-03	2.572e-03
D to Z	5.604e-04	9.707e-04	1.458e-03	1.870e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

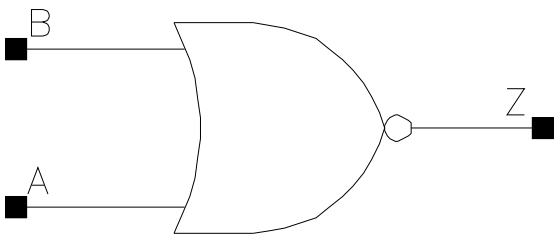
Pin Cycle (vdds)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.408	0.3264
X4_P16	0.800	0.408	0.3264
X8_P16	0.800	0.680	0.5440
X9_P16	1.600	0.408	0.6528
X12_P16	0.800	0.952	0.7616
X16_P16	0.800	1.224	0.9792
X19_P16	1.600	0.680	1.0880
X20_P16	0.800	1.496	1.1968
X23_P16	0.800	1.496	1.1968
X24_P16	0.800	1.768	1.4144
X27_P16	0.800	1.632	1.3056
X29_P16	1.600	0.952	1.5232
X31_P16	0.800	2.312	1.8496
X34_P16	0.800	2.040	1.6320
X38_P16	0.800	2.176	1.7408
X39_P16	1.600	1.224	1.9584
X46_P16	1.600	1.224	1.9584
X57_P16	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P16	X4_P16	X8_P16	X9_P16
A	0.0004	0.0005	0.0011	0.0011
B	0.0004	0.0005	0.0010	0.0011
	X12_P16	X16_P16	X19_P16	X20_P16

A	0.0016	0.0021	0.0023	0.0027
B	0.0014	0.0019	0.0021	0.0023
	X23_P16	X24_P16	X27_P16	X29_P16
A	0.0007	0.0031	0.0007	0.0035
B	0.0006	0.0028	0.0006	0.0031
	X31_P16	X34_P16	X38_P16	X39_P16
A	0.0041	0.0007	0.0007	0.0046
B	0.0038	0.0007	0.0007	0.0042
	X46_P16	X57_P16		
A	0.0007	0.0007		
B	0.0008	0.0008		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X4_P16**	**X2_P16**	**X4_P16**
A to Z ↓	0.0135	0.0126	9.4244	4.9292
A to Z ↑	0.0254	0.0224	30.1266	15.7081
B to Z ↓	0.0122	0.0110	9.4804	4.9643
B to Z ↑	0.0252	0.0214	30.2210	15.7554
	X8_P16	**X9_P16**	**X8_P16**	**X9_P16**
A to Z ↓	0.0118	0.0107	2.3731	1.8369
A to Z ↑	0.0218	0.0207	7.3215	7.0974
B to Z ↓	0.0087	0.0093	2.3778	1.8894
B to Z ↑	0.0165	0.0196	7.3537	7.1175
	X12_P16	**X16_P16**	**X12_P16**	**X16_P16**
A to Z ↓	0.0120	0.0120	1.6217	1.2111
A to Z ↑	0.0211	0.0216	4.8284	3.6716
B to Z ↓	0.0093	0.0090	1.6351	1.2217
B to Z ↑	0.0172	0.0168	4.8542	3.6876
	X19_P16	**X20_P16**	**X19_P16**	**X20_P16**
A to Z ↓	0.0114	0.0123	0.9230	0.9901
A to Z ↑	0.0237	0.0213	3.6054	2.9220
B to Z ↓	0.0094	0.0094	0.9303	0.9986
B to Z ↑	0.0195	0.0172	3.6146	2.9351
	X23_P16	**X24_P16**	**X23_P16**	**X24_P16**
A to Z ↓	0.0476	0.0120	1.0287	0.8219
A to Z ↑	0.0669	0.0213	1.6172	2.4553
B to Z ↓	0.0452	0.0091	1.0282	0.8293
B to Z ↑	0.0656	0.0167	1.6174	2.4663
	X27_P16	**X29_P16**	**X27_P16**	**X29_P16**
A to Z ↓	0.0503	0.0111	0.8592	0.6136
A to Z ↑	0.0693	0.0223	1.3500	2.4165
B to Z ↓	0.0478	0.0089	0.8586	0.6184
B to Z ↑	0.0681	0.0188	1.3499	2.4219
	X31_P16	**X34_P16**	**X31_P16**	**X34_P16**
A to Z ↓	0.0121	0.0514	0.6150	0.7003
A to Z ↑	0.0214	0.0778	1.8396	1.1060
B to Z ↓	0.0093	0.0493	0.6205	0.6998
B to Z ↑	0.0169	0.0770	1.8487	1.1062
	X38_P16	**X39_P16**	**X38_P16**	**X39_P16**
A to Z ↓	0.0530	0.0113	0.6113	0.4671
A to Z ↑	0.0791	0.0228	0.9698	1.8109

B to Z ↓	0.0509	0.0090	0.6115	0.4718
B to Z ↑	0.0783	0.0186	0.9700	1.8168
	X46_P16	**X57_P16**	**X46_P16**	**X57_P16**
A to Z ↓	0.0617	0.0674	0.4590	0.3764
A to Z ↑	0.0823	0.0863	0.9635	0.7747
B to Z ↓	0.0600	0.0656	0.4593	0.3763
B to Z ↑	0.0825	0.0866	0.9637	0.7746

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P16	7.617e-07	1.000e-20
X4_P16	1.580e-06	1.000e-20
X8_P16	3.213e-06	1.000e-20
X9_P16	3.876e-06	1.000e-20
X12_P16	4.640e-06	1.000e-20
X16_P16	6.072e-06	1.000e-20
X19_P16	7.344e-06	1.000e-20
X20_P16	7.504e-06	1.000e-20
X23_P16	1.072e-05	1.000e-20
X24_P16	8.936e-06	1.000e-20
X27_P16	1.201e-05	1.000e-20
X29_P16	1.062e-05	1.000e-20
X31_P16	1.180e-05	1.000e-20
X34_P16	1.567e-05	1.000e-20
X38_P16	1.701e-05	1.000e-20
X39_P16	1.391e-05	1.000e-20
X46_P16	1.785e-05	1.000e-20
X57_P16	2.076e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P16	X4_P16	X8_P16	X9_P16
A (output stable)	8.455e-06	1.504e-05	6.316e-05	3.344e-05
B (output stable)	9.539e-06	2.218e-05	8.763e-05	5.171e-05
A to Z	3.609e-04	5.947e-04	1.204e-03	1.201e-03
B to Z	2.828e-04	4.414e-04	6.562e-04	8.845e-04
	X12_P16	X16_P16	X19_P16	X20_P16
A (output stable)	8.842e-05	1.248e-04	1.308e-04	1.474e-04
B (output stable)	1.215e-04	1.662e-04	1.871e-04	1.938e-04
A to Z	1.768e-03	2.398e-03	2.755e-03	2.980e-03
B to Z	1.065e-03	1.365e-03	1.776e-03	1.788e-03
	X23_P16	X24_P16	X27_P16	X29_P16
A (output stable)	1.640e-05	1.839e-04	1.647e-05	1.711e-04
B (output stable)	2.475e-05	2.349e-04	2.482e-05	2.351e-04
A to Z	5.606e-03	3.527e-03	6.313e-03	3.817e-03
B to Z	5.445e-03	2.044e-03	6.150e-03	2.482e-03
	X31_P16	X34_P16	X38_P16	X39_P16
A (output stable)	2.470e-04	1.739e-05	1.748e-05	2.576e-04
B (output stable)	3.152e-04	2.678e-05	2.688e-05	3.454e-04
A to Z	4.710e-03	8.318e-03	9.057e-03	5.224e-03
B to Z	2.763e-03	8.148e-03	8.885e-03	3.297e-03
	X46_P16	X57_P16		

A (output stable)	1.766e-05	1.789e-05		
B (output stable)	2.730e-05	2.746e-05		
A to Z	1.004e-02	1.227e-02		
B to Z	9.900e-03	1.213e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

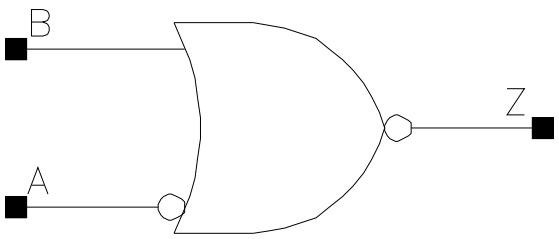
Pin Cycle (vdds)	X2_P16	X4_P16	X8_P16	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P16	X16_P16	X19_P16	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P16	X24_P16	X27_P16	X29_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P16	X34_P16	X38_P16	X39_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P16	X57_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.544	0.4352
X3_P16	0.800	0.544	0.4352
X4_P16	0.800	0.544	0.4352
X10_P16	1.600	0.544	0.8704
X14_P16	1.600	0.816	1.3056
X19_P16	1.600	0.816	1.3056
X29_P16	1.600	1.088	1.7408
X39_P16	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P16	X3_P16	X4_P16	X10_P16
A	0.0006	0.0005	0.0006	0.0010
B	0.0003	0.0004	0.0005	0.0011
	X14_P16	X19_P16	X29_P16	X39_P16
A	0.0009	0.0009	0.0015	0.0015
B	0.0017	0.0020	0.0031	0.0041

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	X3_P16	X2_P16	X3_P16
A to Z ↓	0.0370	0.0372	9.3281	6.9035
A to Z ↑	0.0352	0.0348	30.0236	25.1528
B to Z ↓	0.0119	0.0106	9.5622	7.0609

B to Z ↑	0.0241	0.0227	30.2059	25.2502
	X4_P16	**X10_P16**	**X4_P16**	**X10_P16**
A to Z ↓	0.0384	0.0374	5.2243	1.8148
A to Z ↑	0.0342	0.0329	17.8436	7.0379
B to Z ↓	0.0100	0.0094	5.3420	1.8073
B to Z ↑	0.0201	0.0202	17.9162	7.0710
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0459	0.0494	1.1742	0.9098
A to Z ↑	0.0377	0.0388	4.8356	3.5303
B to Z ↓	0.0088	0.0084	1.2517	0.9726
B to Z ↑	0.0190	0.0174	4.8600	3.5495
	X29_P16	**X39_P16**	**X29_P16**	**X39_P16**
A to Z ↓	0.0421	0.0482	0.6105	0.4602
A to Z ↑	0.0368	0.0387	2.4152	1.7890
B to Z ↓	0.0088	0.0084	0.6198	0.4838
B to Z ↑	0.0186	0.0172	2.4284	1.7974

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P16	1.406e-06	1.000e-20
X3_P16	1.655e-06	1.000e-20
X4_P16	2.106e-06	1.000e-20
X10_P16	5.747e-06	1.000e-20
X14_P16	6.868e-06	1.000e-20
X19_P16	9.085e-06	1.000e-20
X29_P16	1.394e-05	1.000e-20
X39_P16	1.734e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P16	X3_P16	X4_P16	X10_P16
A (output stable)	5.274e-04	5.769e-04	6.529e-04	1.346e-03
B (output stable)	1.304e-05	1.566e-05	2.228e-05	5.965e-05
A to Z	9.128e-04	1.010e-03	1.184e-03	2.721e-03
B to Z	2.637e-04	2.926e-04	3.461e-04	9.325e-04
	X14_P16	X19_P16	X29_P16	X39_P16
A (output stable)	2.039e-03	2.365e-03	3.502e-03	4.508e-03
B (output stable)	8.867e-05	1.197e-04	3.335e-04	2.360e-04
A to Z	3.996e-03	4.821e-03	7.661e-03	9.419e-03
B to Z	1.217e-03	1.487e-03	2.444e-03	2.927e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X2_P16	X3_P16	X4_P16	X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P16	X19_P16	X29_P16	X39_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

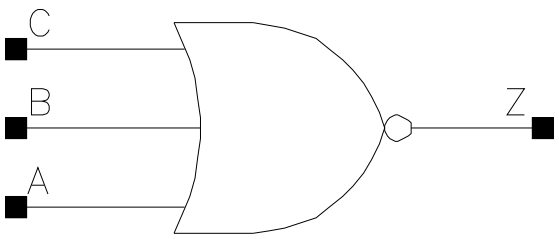
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.544	0.4352
X7_P16	0.800	0.952	0.7616
X11_P16	0.800	1.360	1.0880
X14_P16	0.800	1.768	1.4144
X21_P16	0.800	2.584	2.0672
X29_P16	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X11_P16	X14_P16
A	0.0005	0.0010	0.0016	0.0021
B	0.0005	0.0011	0.0015	0.0022
C	0.0005	0.0009	0.0014	0.0019
	X21_P16	X29_P16		
A	0.0033	0.0043		
B	0.0033	0.0043		
C	0.0028	0.0037		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0141	0.0139	4.9980	2.6192
A to Z ↑	0.0305	0.0316	21.8092	11.1263

B to Z ↓	0.0134	0.0133	5.0209	2.5320
B to Z ↑	0.0284	0.0312	21.8322	11.1403
C to Z ↓	0.0118	0.0101	5.0733	2.5508
C to Z ↑	0.0255	0.0210	21.8856	11.1535
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0140	0.0140	1.6375	1.2536
A to Z ↑	0.0320	0.0312	7.2446	5.3204
B to Z ↓	0.0134	0.0132	1.6556	1.2228
B to Z ↑	0.0287	0.0303	7.2515	5.3259
C to Z ↓	0.0108	0.0103	1.6451	1.2374
C to Z ↑	0.0230	0.0213	7.2613	5.3359
	X21_P16	**X29_P16**	**X21_P16**	**X29_P16**
A to Z ↓	0.0139	0.0140	0.8360	0.6281
A to Z ↑	0.0309	0.0310	3.5640	2.6788
B to Z ↓	0.0133	0.0134	0.8227	0.6214
B to Z ↑	0.0298	0.0299	3.5665	2.6800
C to Z ↓	0.0105	0.0106	0.8349	0.6304
C to Z ↑	0.0215	0.0216	3.5737	2.6855

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	1.297e-06	1.000e-20
X7_P16	2.475e-06	1.000e-20
X11_P16	3.809e-06	1.000e-20
X14_P16	5.096e-06	1.000e-20
X21_P16	7.525e-06	1.000e-20
X29_P16	9.974e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	1.889e-05	4.400e-05	8.407e-05	9.138e-05
B (output stable)	-1.655e-07	1.501e-05	3.009e-06	2.583e-05
C (output stable)	2.203e-05	7.407e-05	8.985e-05	1.509e-04
A to Z	7.989e-04	1.638e-03	2.588e-03	3.373e-03
B to Z	6.415e-04	1.370e-03	1.950e-03	2.798e-03
C to Z	4.786e-04	7.670e-04	1.330e-03	1.635e-03
	X21_P16	X29_P16		
A (output stable)	1.357e-04	1.800e-04		
B (output stable)	3.896e-05	5.161e-05		
C (output stable)	2.238e-04	3.060e-04		
A to Z	4.991e-03	6.656e-03		
B to Z	4.097e-03	5.475e-03		
C to Z	2.453e-03	3.288e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

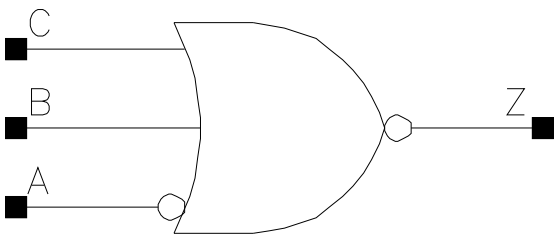
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P16	X29_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X7_P16	0.800	1.360	1.0880
X11_P16	0.800	1.632	1.3056
X14_P16	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X11_P16	X14_P16
A	0.0007	0.0007	0.0009	0.0013
B	0.0006	0.0011	0.0015	0.0020
C	0.0005	0.0010	0.0014	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0414	0.0365	4.9223	2.3021
A to Z ↑	0.0457	0.0453	21.8594	10.5850
B to Z ↓	0.0134	0.0132	5.0483	2.3860
B to Z ↑	0.0282	0.0304	21.9191	10.6057
C to Z ↓	0.0118	0.0104	5.0861	2.3990
C to Z ↑	0.0254	0.0221	21.9755	10.6236
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0449	0.0353	1.6263	1.2023

A to Z ↑	0.0499	0.0442	7.2542	5.3756
B to Z ↓	0.0133	0.0131	1.6572	1.2316
B to Z ↑	0.0285	0.0288	7.2714	5.3875
C to Z ↓	0.0106	0.0102	1.6481	1.2425
C to Z ↑	0.0226	0.0214	7.2816	5.3975

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	1.991e-06	1.000e-20
X7_P16	4.465e-06	1.000e-20
X11_P16	5.273e-06	1.000e-20
X14_P16	8.030e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	7.113e-04	1.215e-03	1.681e-03	2.244e-03
B (output stable)	5.242e-06	3.393e-05	3.782e-05	7.099e-05
C (output stable)	2.817e-05	1.154e-04	1.273e-04	2.039e-04
A to Z	1.553e-03	3.235e-03	4.437e-03	6.096e-03
B to Z	6.353e-04	1.418e-03	1.944e-03	2.645e-03
C to Z	4.730e-04	8.669e-04	1.291e-03	1.626e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

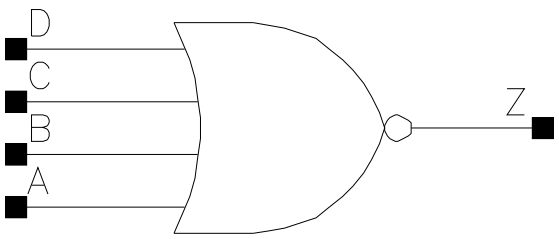
Pin Cycle (vdds)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.224	0.9792
X10_P16	0.800	1.632	1.3056
X14_P16	0.800	1.904	1.5232
X18_P16	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X18_P16
A	0.0005	0.0004	0.0005	0.0006
B	0.0005	0.0006	0.0007	0.0007
C	0.0005	0.0004	0.0005	0.0006
D	0.0005	0.0004	0.0005	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0475	0.0530	4.8993	2.3352
A to Z ↑	0.0769	0.0865	8.1329	3.9032
B to Z ↓	0.0465	0.0536	4.8997	2.3354
B to Z ↑	0.0768	0.0895	8.1334	3.9057
C to Z ↓	0.0486	0.0542	4.8945	2.3322
C to Z ↑	0.0818	0.0944	8.1305	3.9026

D to Z ↓	0.0486	0.0525	4.8875	2.3293
D to Z ↑	0.0833	0.0936	8.1230	3.9002
	X14_P16	**X18_P16**	**X14_P16**	**X18_P16**
A to Z ↓	0.0509	0.0532	1.6088	1.2796
A to Z ↑	0.0784	0.0761	2.6622	2.0294
B to Z ↓	0.0505	0.0515	1.6066	1.2791
B to Z ↑	0.0797	0.0758	2.6657	2.0309
C to Z ↓	0.0495	0.0525	1.6021	1.2745
C to Z ↑	0.0786	0.0770	2.6625	2.0304
D to Z ↓	0.0481	0.0504	1.6007	1.2744
D to Z ↑	0.0787	0.0764	2.6627	2.0307

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	3.737e-06	1.000e-20
X10_P16	5.431e-06	1.000e-20
X14_P16	8.052e-06	1.000e-20
X18_P16	1.039e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	2.913e-04	3.867e-04	4.814e-04	6.021e-04
B (output stable)	2.580e-04	3.645e-04	4.439e-04	5.429e-04
C (output stable)	3.083e-04	3.716e-04	4.997e-04	6.360e-04
D (output stable)	2.794e-04	3.381e-04	4.539e-04	5.717e-04
A to Z	2.049e-03	3.238e-03	4.574e-03	5.838e-03
B to Z	1.965e-03	3.174e-03	4.464e-03	5.700e-03
C to Z	2.125e-03	3.177e-03	4.274e-03	5.469e-03
D to Z	2.065e-03	3.100e-03	4.169e-03	5.315e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

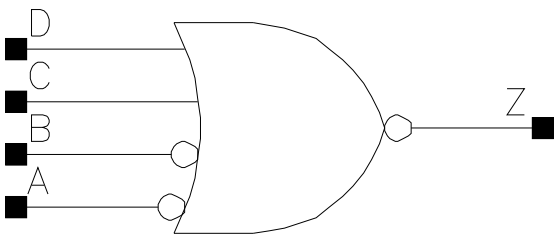
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	1.224	0.9792
X7_P16	0.800	1.496	1.1968
X11_P16	0.800	2.040	1.6320
X14_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P16	X7_P16	X11_P16	X14_P16
A	0.0007	0.0007	0.0014	0.0013
B	0.0007	0.0007	0.0013	0.0013
C	0.0005	0.0010	0.0015	0.0020
D	0.0005	0.0010	0.0014	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X7_P16	X4_P16	X7_P16
A to Z ↓	0.0404	0.0426	4.5491	2.3467
A to Z ↑	0.0571	0.0559	20.8997	10.6842
B to Z ↓	0.0372	0.0393	4.5439	2.3440
B to Z ↑	0.0568	0.0555	20.9096	10.6910
C to Z ↓	0.0136	0.0132	4.6170	2.4063
C to Z ↑	0.0297	0.0300	20.9376	10.7106

D to Z ↓	0.0120	0.0104	4.6443	2.4043
D to Z ↑	0.0267	0.0222	20.9592	10.7264
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0380	0.0419	1.6033	1.2085
A to Z ↑	0.0511	0.0557	7.1935	5.3649
B to Z ↓	0.0344	0.0390	1.6003	1.2053
B to Z ↑	0.0506	0.0561	7.1949	5.3649
C to Z ↓	0.0133	0.0133	1.6561	1.2352
C to Z ↑	0.0284	0.0292	7.2083	5.3723
D to Z ↓	0.0107	0.0104	1.6487	1.2322
D to Z ↑	0.0227	0.0219	7.2198	5.3829

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	2.916e-06	1.000e-20
X7_P16	3.818e-06	1.000e-20
X11_P16	6.152e-06	1.000e-20
X14_P16	7.070e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X7_P16	X11_P16	X14_P16
A (output stable)	5.805e-04	6.849e-04	1.086e-03	1.316e-03
B (output stable)	5.389e-04	6.434e-04	9.832e-04	1.236e-03
C (output stable)	3.710e-05	2.321e-05	3.994e-05	6.260e-05
D (output stable)	6.270e-05	1.124e-04	1.452e-04	2.302e-04
A to Z	2.558e-03	3.511e-03	5.326e-03	6.950e-03
B to Z	2.347e-03	3.302e-03	4.903e-03	6.568e-03
C to Z	7.215e-04	1.392e-03	1.954e-03	2.696e-03
D to Z	5.589e-04	8.612e-04	1.303e-03	1.683e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

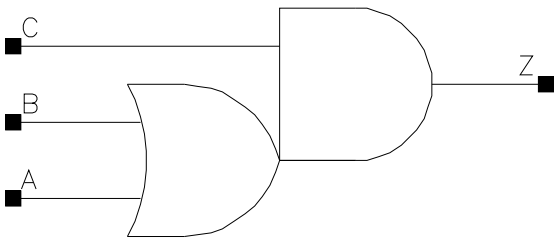
Pin Cycle (vdds)	X4_P16	X7_P16	X11_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.680	0.5440
X10_P16	0.800	0.952	0.7616
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0006	0.0006	0.0011
B	0.0006	0.0007	0.0013
C	0.0007	0.0009	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0406	0.0466	4.7030	2.3507
A to Z ↑	0.0325	0.0382	8.9676	3.9058
B to Z ↓	0.0405	0.0466	4.6984	2.3524
B to Z ↑	0.0301	0.0354	8.9612	3.8961
C to Z ↓	0.0363	0.0394	4.6409	2.3085
C to Z ↑	0.0315	0.0359	8.9675	3.8987
	X19_P16		**X19_P16**	
A to Z ↓	0.0481		1.2231	
A to Z ↑	0.0396		1.9837	

B to Z ↓	0.0482		1.2238	
B to Z ↑	0.0366		1.9800	
C to Z ↓	0.0393		1.1982	
C to Z ↑	0.0360		1.9791	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	3.129e-06	1.000e-20
X10_P16	5.181e-06	1.000e-20
X19_P16	9.696e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	4.278e-05	4.416e-05	9.246e-05
B (output stable)	4.692e-05	5.003e-05	9.775e-05
C (output stable)	2.811e-05	2.912e-05	5.716e-05
A to Z	1.380e-03	2.267e-03	4.584e-03
B to Z	1.245e-03	2.107e-03	4.280e-03
C to Z	1.538e-03	2.374e-03	4.704e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

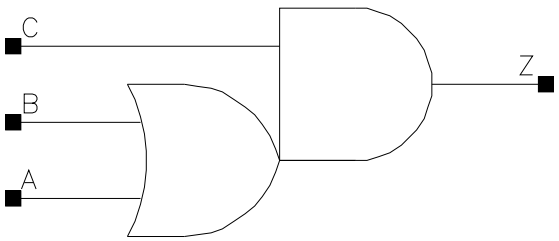
Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	1.360	1.0880
X14_P16	0.800	1.496	1.1968
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0006	0.0013	0.0013	0.0013
B	0.0006	0.0012	0.0012	0.0011
C	0.0007	0.0013	0.0013	0.0013

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0505	0.0419	4.5976	2.3241
A to Z ↑	0.0342	0.0312	7.7543	3.8271
B to Z ↓	0.0502	0.0410	4.5967	2.3243
B to Z ↑	0.0318	0.0288	7.7399	3.8236
C to Z ↓	0.0331	0.0272	4.5000	2.2837
C to Z ↑	0.0311	0.0275	7.7427	3.8195
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0465	0.0508	1.6135	1.2218

A to Z ↑	0.0342	0.0367	2.5809	1.9410
B to Z ↓	0.0458	0.0502	1.6162	1.2232
B to Z ↑	0.0318	0.0345	2.5807	1.9392
C to Z ↓	0.0304	0.0333	1.5801	1.1919
C to Z ↑	0.0307	0.0334	2.5768	1.9360

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	3.542e-06	1.000e-20
X10_P16	7.059e-06	1.000e-20
X14_P16	8.411e-06	1.000e-20
X19_P16	9.736e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	1.075e-05	2.252e-05	2.265e-05	2.288e-05
B (output stable)	1.215e-05	2.903e-05	2.908e-05	2.937e-05
C (output stable)	1.283e-04	2.656e-04	2.660e-04	2.671e-04
A to Z	1.790e-03	3.153e-03	3.997e-03	4.808e-03
B to Z	1.639e-03	2.789e-03	3.636e-03	4.451e-03
C to Z	1.421e-03	2.374e-03	3.176e-03	3.923e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

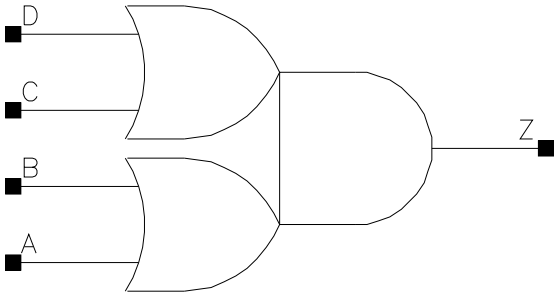
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.952	0.7616
X10_P16	0.800	1.088	0.8704
X14_P16	0.800	1.904	1.5232
X19_P16	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0004	0.0006	0.0012	0.0012
B	0.0004	0.0006	0.0012	0.0012
C	0.0004	0.0007	0.0012	0.0012
D	0.0004	0.0006	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0728	0.0568	4.7893	2.3796
A to Z ↑	0.0477	0.0401	7.7939	3.8924
B to Z ↓	0.0727	0.0566	4.7926	2.3793

B to Z ↑	0.0458	0.0379	7.7882	3.8857
C to Z ↓	0.0619	0.0502	4.7410	2.3652
C to Z ↑	0.0456	0.0395	7.7890	3.8907
D to Z ↓	0.0614	0.0494	4.7426	2.3665
D to Z ↑	0.0431	0.0368	7.7853	3.8865
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0540	0.0568	1.6411	1.2367
A to Z ↑	0.0380	0.0393	2.5893	1.9462
B to Z ↓	0.0513	0.0543	1.6421	1.2371
B to Z ↑	0.0350	0.0363	2.5820	1.9422
C to Z ↓	0.0459	0.0490	1.6303	1.2283
C to Z ↑	0.0364	0.0379	2.5884	1.9445
D to Z ↓	0.0426	0.0458	1.6307	1.2291
D to Z ↑	0.0329	0.0344	2.5816	1.9403

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	2.793e-06	1.000e-20
X10_P16	5.756e-06	1.000e-20
X14_P16	9.554e-06	1.000e-20
X19_P16	1.087e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	1.057e-05	1.646e-05	5.150e-05	5.161e-05
B (output stable)	1.033e-05	2.095e-05	6.588e-05	6.592e-05
C (output stable)	4.209e-05	4.902e-05	1.154e-04	1.151e-04
D (output stable)	4.310e-05	5.385e-05	1.322e-04	1.317e-04
A to Z	1.780e-03	2.767e-03	4.743e-03	5.362e-03
B to Z	1.697e-03	2.593e-03	4.247e-03	4.861e-03
C to Z	1.534e-03	2.436e-03	4.053e-03	4.670e-03
D to Z	1.449e-03	2.269e-03	3.536e-03	4.147e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

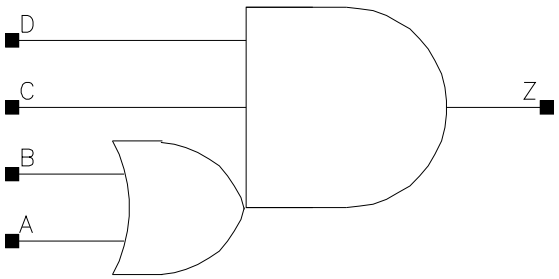
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	0.816	0.6528
X10_P16	0.800	1.088	0.8704
X14_P16	0.800	1.904	1.5232
X19_P16	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P16	X10_P16	X14_P16	X19_P16
A	0.0004	0.0009	0.0010	0.0011
B	0.0004	0.0006	0.0010	0.0012
C	0.0005	0.0007	0.0010	0.0012
D	0.0004	0.0006	0.0010	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X10_P16	X4_P16	X10_P16
A to Z ↓	0.0613	0.0578	5.2494	2.4214
A to Z ↑	0.0532	0.0544	8.2946	3.9576
B to Z ↓	0.0623	0.0530	5.2528	2.4208
B to Z ↑	0.0512	0.0471	8.2761	3.9486
C to Z ↓	0.0494	0.0434	5.0854	2.3688

C to Z ↑	0.0521	0.0490	8.2769	3.9445
D to Z ↓	0.0486	0.0419	5.0862	2.3670
D to Z ↑	0.0535	0.0498	8.2771	3.9460
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0568	0.0535	1.6445	1.2257
A to Z ↑	0.0518	0.0520	2.6390	1.9770
B to Z ↓	0.0537	0.0509	1.6455	1.2258
B to Z ↑	0.0471	0.0472	2.6290	1.9710
C to Z ↓	0.0453	0.0430	1.6072	1.2004
C to Z ↑	0.0493	0.0489	2.6290	1.9699
D to Z ↓	0.0429	0.0409	1.6028	1.1984
D to Z ↑	0.0488	0.0485	2.6304	1.9708

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	2.150e-06	1.000e-20
X10_P16	4.568e-06	1.000e-20
X14_P16	6.912e-06	1.000e-20
X19_P16	9.080e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X10_P16	X14_P16	X19_P16
A (output stable)	5.462e-05	8.353e-05	1.330e-04	1.465e-04
B (output stable)	5.183e-05	8.118e-05	1.374e-04	1.521e-04
C (output stable)	8.165e-06	1.694e-05	4.449e-05	5.027e-05
D (output stable)	1.899e-05	3.359e-05	1.321e-04	1.433e-04
A to Z	1.498e-03	2.712e-03	4.141e-03	5.124e-03
B to Z	1.428e-03	2.400e-03	3.729e-03	4.612e-03
C to Z	1.641e-03	2.773e-03	4.435e-03	5.421e-03
D to Z	1.574e-03	2.653e-03	4.118e-03	5.061e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

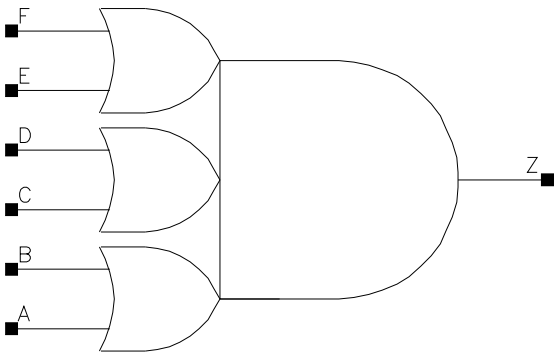
Pin Cycle (vdds)	X4_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	1.360	1.0880
X9_P16	0.800	1.496	1.1968
X19_P16	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P16	X9_P16	X19_P16
A	0.0005	0.0006	0.0010
B	0.0006	0.0008	0.0012
C	0.0004	0.0006	0.0010
D	0.0004	0.0005	0.0012
E	0.0004	0.0006	0.0010
F	0.0004	0.0006	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X9_P16	X4_P16	X9_P16
A to Z ↓	0.0865	0.0696	5.3571	2.6305
A to Z ↑	0.0640	0.0585	8.5018	4.1586
B to Z ↓	0.0888	0.0712	5.3572	2.6308
B to Z ↑	0.0636	0.0567	8.5048	4.1529
C to Z ↓	0.0794	0.0631	5.3199	2.6130
C to Z ↑	0.0634	0.0565	8.5095	4.1592
D to Z ↓	0.0788	0.0627	5.3175	2.6126
D to Z ↑	0.0602	0.0531	8.4985	4.1526
E to Z ↓	0.0675	0.0556	5.2573	2.5949
E to Z ↑	0.0573	0.0527	8.4991	4.1540
F to Z ↓	0.0683	0.0560	5.2596	2.5956
F to Z ↑	0.0553	0.0502	8.4902	4.1485
	X19_P16		X19_P16	
A to Z ↓	0.0672		1.2566	
A to Z ↑	0.0556		1.9773	
B to Z ↓	0.0678		1.2572	
B to Z ↑	0.0523		1.9720	
C to Z ↓	0.0618		1.2482	
C to Z ↑	0.0545		1.9767	
D to Z ↓	0.0621		1.2486	
D to Z ↑	0.0515		1.9709	
E to Z ↓	0.0542		1.2402	
E to Z ↑	0.0512		1.9741	
F to Z ↓	0.0547		1.2398	
F to Z ↑	0.0482		1.9693	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	2.748e-06	1.000e-20
X9_P16	5.539e-06	1.000e-20
X19_P16	1.106e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X9_P16	X19_P16
A (output stable)	9.333e-06	1.589e-05	2.862e-05
B (output stable)	1.221e-05	2.044e-05	3.419e-05
C (output stable)	2.448e-05	3.318e-05	6.373e-05
D (output stable)	2.544e-05	3.575e-05	7.023e-05
E (output stable)	7.927e-05	9.815e-05	1.843e-04
F (output stable)	7.566e-05	1.006e-04	1.866e-04
A to Z	2.129e-03	3.329e-03	6.436e-03
B to Z	2.073e-03	3.202e-03	6.140e-03
C to Z	1.923e-03	3.020e-03	5.891e-03
D to Z	1.835e-03	2.851e-03	5.584e-03
E to Z	1.649e-03	2.681e-03	5.232e-03
F to Z	1.582e-03	2.539e-03	4.947e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

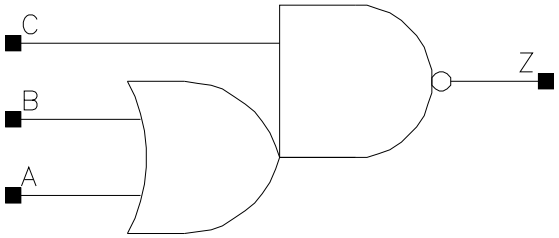
Pin Cycle (vdds)	X4_P16	X9_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.544	0.4352
X10_P16	0.800	1.360	1.0880
X20_P16	0.800	2.720	2.1760
X26_P16	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P16	X10_P16	X20_P16	X26_P16
A	0.0005	0.0015	0.0029	0.0039
B	0.0005	0.0014	0.0027	0.0036
C	0.0005	0.0016	0.0031	0.0042

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X10_P16**	**X3_P16**	**X10_P16**
A to Z ↓	0.0160	0.0174	9.4590	2.9247
A to Z ↑	0.0224	0.0232	17.9252	4.8761
B to Z ↓	0.0135	0.0140	9.3351	2.9505
B to Z ↑	0.0214	0.0196	17.9944	4.9026
C to Z ↓	0.0155	0.0160	8.6089	2.6898
C to Z ↑	0.0214	0.0199	9.6780	2.6558
	X20_P16	**X26_P16**	**X20_P16**	**X26_P16**
A to Z ↓	0.0182	0.0182	1.4906	1.1268

A to Z ↑	0.0239	0.0238	2.4805	1.8645
B to Z ↓	0.0145	0.0146	1.5016	1.1387
B to Z ↑	0.0205	0.0205	2.4918	1.8729
C to Z ↓	0.0168	0.0168	1.3704	1.0374
C to Z ↑	0.0204	0.0204	1.3113	0.9845

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	1.686e-06	1.000e-20
X10_P16	5.676e-06	1.000e-20
X20_P16	1.127e-05	1.000e-20
X26_P16	1.480e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X10_P16	X20_P16	X26_P16
A (output stable)	3.754e-05	1.417e-04	2.897e-04	3.739e-04
B (output stable)	4.253e-05	1.495e-04	3.158e-04	4.028e-04
C (output stable)	2.557e-05	9.123e-05	1.949e-04	2.535e-04
A to Z	5.141e-04	2.000e-03	4.151e-03	5.510e-03
B to Z	3.838e-04	1.293e-03	2.799e-03	3.740e-03
C to Z	6.525e-04	2.260e-03	4.762e-03	6.283e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

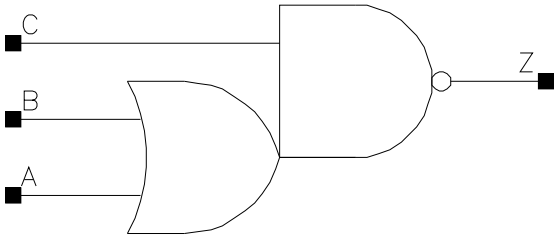
Pin Cycle (vdds)	X3_P16	X10_P16	X20_P16	X26_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X7_P16	0.800	0.952	0.7616
X10_P16	0.800	1.360	1.0880
X13_P16	0.800	1.904	1.5232
X26_P16	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X10_P16	X13_P16
A	0.0006	0.0010	0.0017	0.0021
B	0.0005	0.0011	0.0015	0.0019
C	0.0007	0.0010	0.0014	0.0019
	X26_P16			
A	0.0043			
B	0.0038			
C	0.0037			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X7_P16	X3_P16	X7_P16
A to Z ↓	0.0198	0.0177	8.1939	4.2640
A to Z ↑	0.0304	0.0267	14.2349	7.2492
B to Z ↓	0.0174	0.0151	8.2122	4.1755

B to Z ↑	0.0296	0.0257	14.2645	7.2781
C to Z ↓	0.0163	0.0138	7.6812	3.9383
C to Z ↑	0.0182	0.0153	7.8681	4.0524
	X10_P16	**X13_P16**	**X10_P16**	**X13_P16**
A to Z ↓	0.0173	0.0182	2.8769	2.1846
A to Z ↑	0.0259	0.0285	4.8026	3.6642
B to Z ↓	0.0146	0.0149	2.8704	2.1860
B to Z ↑	0.0247	0.0248	4.8190	3.6753
C to Z ↓	0.0134	0.0135	2.6898	2.0371
C to Z ↑	0.0145	0.0145	2.6787	2.0223
	X26_P16		**X26_P16**	
A to Z ↓	0.0180		1.1233	
A to Z ↑	0.0279		1.8415	
B to Z ↓	0.0145		1.1204	
B to Z ↑	0.0242		1.8489	
C to Z ↓	0.0136		1.0462	
C to Z ↑	0.0142		1.0167	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	2.254e-06	1.000e-20
X7_P16	3.958e-06	1.000e-20
X10_P16	5.773e-06	1.000e-20
X13_P16	7.822e-06	1.000e-20
X26_P16	1.495e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X7_P16	X10_P16	X13_P16
A (output stable)	1.262e-05	2.293e-05	3.393e-05	6.461e-05
B (output stable)	1.442e-05	2.786e-05	4.086e-05	7.127e-05
C (output stable)	1.364e-04	2.639e-04	3.459e-04	5.133e-04
A to Z	1.041e-03	1.665e-03	2.406e-03	3.554e-03
B to Z	8.556e-04	1.307e-03	1.849e-03	2.510e-03
C to Z	6.055e-04	9.683e-04	1.351e-03	1.900e-03
	X26_P16			
A (output stable)	1.260e-04			
B (output stable)	1.357e-04			
C (output stable)	9.356e-04			
A to Z	6.872e-03			
B to Z	4.770e-03			
C to Z	3.637e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P16	X7_P16	X10_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

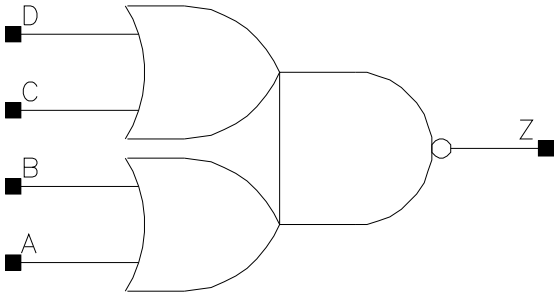
	X26_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X6_P16	0.800	1.360	1.0880
X8_P16	0.800	1.768	1.4144
X11_P16	0.800	2.448	1.9584
X24_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X8_P16	X11_P16
A	0.0005	0.0011	0.0016	0.0021
B	0.0005	0.0010	0.0014	0.0018
C	0.0005	0.0010	0.0015	0.0019
D	0.0005	0.0009	0.0013	0.0017
	X24_P16			
A	0.0044			
B	0.0039			
C	0.0041			
D	0.0036			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X6_P16**	**X3_P16**	**X6_P16**
A to Z ↓	0.0186	0.0216	7.6880	4.2031
A to Z ↑	0.0336	0.0334	17.8093	7.6503
B to Z ↓	0.0168	0.0186	7.6495	4.2093
B to Z ↑	0.0328	0.0297	17.8451	7.6736
C to Z ↓	0.0155	0.0187	7.7804	4.2176
C to Z ↑	0.0231	0.0251	17.8475	7.6703
D to Z ↓	0.0134	0.0148	7.7475	4.2494
D to Z ↑	0.0220	0.0200	17.8976	7.7054
	X8_P16	**X11_P16**	**X8_P16**	**X11_P16**
A to Z ↓	0.0208	0.0210	2.8698	2.1689
A to Z ↑	0.0313	0.0317	5.1173	3.8377
B to Z ↓	0.0180	0.0179	2.8882	2.1705
B to Z ↑	0.0285	0.0284	5.1336	3.8494
C to Z ↓	0.0182	0.0187	2.8890	2.1848
C to Z ↑	0.0234	0.0242	5.1083	3.8561
D to Z ↓	0.0151	0.0150	2.9291	2.1913
D to Z ↑	0.0199	0.0199	5.1353	3.8764
	X24_P16		**X24_P16**	
A to Z ↓	0.0209		1.0488	
A to Z ↑	0.0314		1.8443	
B to Z ↓	0.0178		1.0431	
B to Z ↑	0.0285		1.8506	
C to Z ↓	0.0189		1.0567	
C to Z ↑	0.0239		1.8460	
D to Z ↓	0.0151		1.0544	
D to Z ↑	0.0200		1.8561	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	2.159e-06	1.000e-20
X6_P16	4.665e-06	1.000e-20
X8_P16	6.583e-06	1.000e-20
X11_P16	8.911e-06	1.000e-20
X24_P16	1.809e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X6_P16	X8_P16	X11_P16
A (output stable)	1.446e-05	5.304e-05	6.714e-05	9.732e-05
B (output stable)	1.697e-05	6.742e-05	8.344e-05	1.218e-04
C (output stable)	4.681e-05	1.186e-04	1.535e-04	2.094e-04
D (output stable)	5.226e-05	1.349e-04	1.706e-04	2.335e-04
A to Z	9.588e-04	2.273e-03	3.128e-03	4.244e-03
B to Z	8.066e-04	1.748e-03	2.408e-03	3.242e-03
C to Z	5.849e-04	1.584e-03	2.160e-03	3.015e-03
D to Z	4.562e-04	1.050e-03	1.488e-03	2.033e-03
	X24_P16			
A (output stable)	1.925e-04			
B (output stable)	2.381e-04			
C (output stable)	4.027e-04			
D (output stable)	4.469e-04			

A to Z	8.706e-03			
B to Z	6.687e-03			
C to Z	6.197e-03			
D to Z	4.241e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

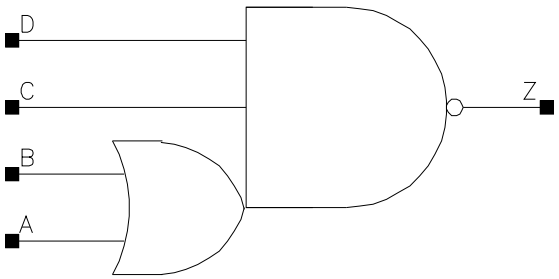
Pin Cycle (vdds)	X3_P16	X6_P16	X8_P16	X11_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X6_P16	0.800	1.360	1.0880
X12_P16	0.800	2.448	1.9584
X18_P16	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X12_P16	X18_P16
A	0.0007	0.0010	0.0020	0.0029
B	0.0005	0.0009	0.0018	0.0027
C	0.0006	0.0011	0.0020	0.0032
D	0.0005	0.0010	0.0020	0.0029

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0286	0.0236	11.7969	6.2346
A to Z ↑	0.0333	0.0269	14.6047	7.3283
B to Z ↓	0.0211	0.0187	11.7400	6.2521
B to Z ↑	0.0270	0.0230	14.6025	7.3564
C to Z ↓	0.0241	0.0241	11.0944	5.8911

C to Z ↑	0.0255	0.0244	7.6646	3.9145
D to Z ↓	0.0255	0.0232	11.1182	5.9049
D to Z ↑	0.0247	0.0223	7.8098	3.9196
	X12_P16	**X18_P16**	**X12_P16**	**X18_P16**
A to Z ↓	0.0240	0.0242	3.2277	2.1780
A to Z ↑	0.0266	0.0265	3.6697	2.4539
B to Z ↓	0.0189	0.0193	3.2397	2.1882
B to Z ↑	0.0227	0.0229	3.6866	2.4672
C to Z ↓	0.0237	0.0239	3.0501	2.0590
C to Z ↑	0.0238	0.0237	1.9836	1.3106
D to Z ↓	0.0231	0.0232	3.0564	2.0638
D to Z ↑	0.0218	0.0217	1.9788	1.3207

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	1.849e-06	1.000e-20
X6_P16	3.459e-06	1.000e-20
X12_P16	6.489e-06	1.000e-20
X18_P16	9.527e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X6_P16	X12_P16	X18_P16
A (output stable)	8.205e-05	1.671e-04	3.119e-04	4.402e-04
B (output stable)	8.062e-05	1.720e-04	3.143e-04	4.467e-04
C (output stable)	1.492e-05	4.745e-05	8.824e-05	1.409e-04
D (output stable)	3.204e-05	1.352e-04	2.379e-04	3.746e-04
A to Z	1.064e-03	1.653e-03	3.247e-03	4.839e-03
B to Z	7.425e-04	1.149e-03	2.220e-03	3.357e-03
C to Z	1.201e-03	2.225e-03	4.218e-03	6.321e-03
D to Z	1.098e-03	1.844e-03	3.522e-03	5.230e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

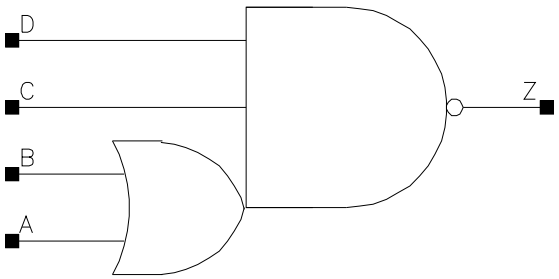
Pin Cycle (vdds)	X3_P16	X6_P16	X12_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X6_P16	0.800	1.360	1.0880
X9_P16	0.800	1.768	1.4144
X12_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X9_P16	X12_P16
A	0.0006	0.0011	0.0017	0.0021
B	0.0005	0.0010	0.0015	0.0022
C	0.0005	0.0010	0.0015	0.0020
D	0.0005	0.0010	0.0014	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0247	0.0255	12.7271	6.1875
A to Z ↑	0.0321	0.0341	14.9684	7.3183
B to Z ↓	0.0214	0.0213	12.5823	6.2089
B to Z ↑	0.0313	0.0311	14.9982	7.3397
C to Z ↓	0.0189	0.0203	12.0116	5.8814

C to Z ↑	0.0197	0.0200	8.2203	4.0147
D to Z ↓	0.0192	0.0185	12.0513	5.9024
D to Z ↑	0.0177	0.0168	8.2889	4.0361
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0258	0.0257	4.2465	3.2129
A to Z ↑	0.0333	0.0337	4.8438	3.7337
B to Z ↓	0.0217	0.0217	4.2551	3.2193
B to Z ↑	0.0306	0.0314	4.8589	3.7443
C to Z ↓	0.0201	0.0204	4.0308	3.0495
C to Z ↑	0.0195	0.0196	2.6585	2.0092
D to Z ↓	0.0189	0.0186	4.0458	3.0616
D to Z ↑	0.0166	0.0163	2.6746	2.0255

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	1.659e-06	1.000e-20
X6_P16	3.509e-06	1.000e-20
X9_P16	4.865e-06	1.000e-20
X12_P16	6.575e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	9.353e-06	2.134e-05	3.365e-05	4.183e-05
B (output stable)	9.462e-06	2.343e-05	3.541e-05	4.867e-05
C (output stable)	3.484e-05	7.656e-05	1.219e-04	1.529e-04
D (output stable)	6.366e-05	2.524e-04	2.843e-04	4.629e-04
A to Z	1.071e-03	2.360e-03	3.452e-03	4.603e-03
B to Z	8.918e-04	1.831e-03	2.666e-03	3.561e-03
C to Z	6.784e-04	1.537e-03	2.178e-03	2.971e-03
D to Z	5.678e-04	1.181e-03	1.711e-03	2.256e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

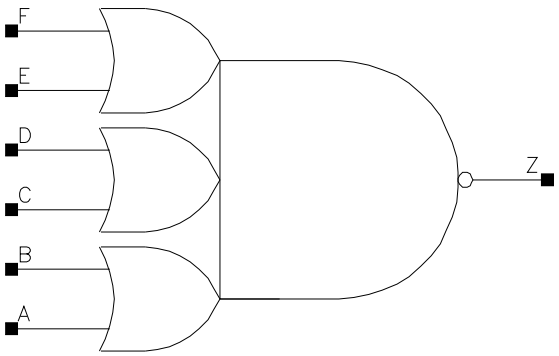
Pin Cycle (vdds)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.224	0.9792
X3_P16	0.800	1.224	0.9792
X5_P16	0.800	2.040	1.6320
X8_P16	0.800	2.720	2.1760
X10_P16	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P16	X3_P16	X5_P16	X8_P16
A	0.0005	0.0006	0.0011	0.0017
B	0.0005	0.0006	0.0010	0.0015
C	0.0004	0.0006	0.0010	0.0016
D	0.0005	0.0005	0.0010	0.0014

E	0.0004	0.0005	0.0010	0.0015
F	0.0004	0.0005	0.0009	0.0014
	X10_P16			
A	0.0022			
B	0.0020			
C	0.0020			
D	0.0019			
E	0.0019			
F	0.0018			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X3_P16**	**X2_P16**	**X3_P16**
A to Z ↓	0.0322	0.0307	13.9989	10.7122
A to Z ↑	0.0463	0.0400	20.6528	14.1459
B to Z ↓	0.0302	0.0285	14.0255	10.7575
B to Z ↑	0.0465	0.0402	20.6764	14.1650
C to Z ↓	0.0308	0.0299	14.0449	10.7330
C to Z ↑	0.0403	0.0356	20.6504	14.2926
D to Z ↓	0.0296	0.0268	14.1246	10.8188
D to Z ↑	0.0418	0.0348	20.7033	14.3085
E to Z ↓	0.0261	0.0253	14.0870	10.7615
E to Z ↑	0.0314	0.0277	20.6516	14.3116
F to Z ↓	0.0242	0.0226	14.1424	10.8440
F to Z ↑	0.0316	0.0271	20.7060	14.3439
	X5_P16	**X8_P16**	**X5_P16**	**X8_P16**
A to Z ↓	0.0323	0.0319	5.6386	3.8426
A to Z ↑	0.0414	0.0401	7.3279	4.8608
B to Z ↓	0.0284	0.0282	5.6576	3.8456
B to Z ↑	0.0383	0.0380	7.3424	4.8697
C to Z ↓	0.0291	0.0300	5.6574	3.8592
C to Z ↑	0.0348	0.0344	7.3738	4.9342
D to Z ↓	0.0253	0.0261	5.6686	3.8560
D to Z ↑	0.0321	0.0329	7.3917	4.9443
E to Z ↓	0.0265	0.0263	5.6807	3.8730
E to Z ↑	0.0282	0.0272	7.3755	4.9442
F to Z ↓	0.0222	0.0223	5.6961	3.8570
F to Z ↑	0.0246	0.0250	7.4004	4.9634
	X10_P16		**X10_P16**	
A to Z ↓	0.0324		2.9057	
A to Z ↑	0.0407		3.6791	
B to Z ↓	0.0286		2.9100	
B to Z ↑	0.0381		3.6871	
C to Z ↓	0.0296		2.9130	
C to Z ↑	0.0346		3.7255	
D to Z ↓	0.0258		2.9179	
D to Z ↑	0.0323		3.7351	
E to Z ↓	0.0266		2.9199	
E to Z ↑	0.0276		3.7183	
F to Z ↓	0.0228		2.9313	
F to Z ↑	0.0249		3.7327	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P16	2.029e-06	1.000e-20
X3_P16	3.006e-06	1.000e-20
X5_P16	5.718e-06	1.000e-20
X8_P16	8.080e-06	1.000e-20
X10_P16	1.079e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P16	X3_P16	X5_P16	X8_P16
A (output stable)	1.224e-05	1.566e-05	4.666e-05	6.259e-05
B (output stable)	1.372e-05	1.906e-05	5.605e-05	7.350e-05
C (output stable)	2.855e-05	3.450e-05	8.617e-05	1.166e-04
D (output stable)	3.019e-05	3.661e-05	9.730e-05	1.272e-04
E (output stable)	8.746e-05	1.069e-04	1.881e-04	2.859e-04
F (output stable)	9.011e-05	1.123e-04	2.001e-04	2.968e-04
A to Z	1.348e-03	1.642e-03	3.340e-03	4.805e-03
B to Z	1.232e-03	1.477e-03	2.810e-03	4.070e-03
C to Z	1.106e-03	1.365e-03	2.628e-03	3.861e-03
D to Z	1.008e-03	1.187e-03	2.169e-03	3.249e-03
E to Z	8.185e-04	1.014e-03	2.072e-03	2.928e-03
F to Z	7.162e-04	8.572e-04	1.597e-03	2.336e-03
	X10_P16			
A (output stable)	8.921e-05			
B (output stable)	1.068e-04			
C (output stable)	1.630e-04			
D (output stable)	1.830e-04			
E (output stable)	3.617e-04			
F (output stable)	3.822e-04			
A to Z	6.500e-03			
B to Z	5.476e-03			
C to Z	5.161e-03			
D to Z	4.273e-03			
E to Z	4.009e-03			
F to Z	3.156e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X2_P16	X3_P16	X5_P16	X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P16			

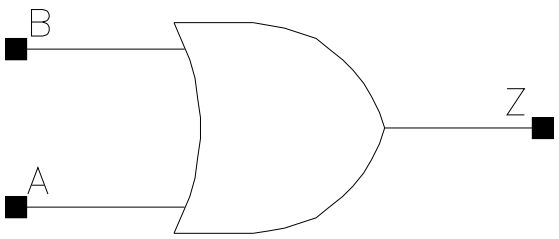
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.544	0.4352
X9_P16	0.800	0.680	0.5440
X19_P16	0.800	1.360	1.0880
X29_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16	X29_P16
A	0.0005	0.0006	0.0011	0.0011
B	0.0004	0.0006	0.0012	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X9_P16**	**X5_P16**	**X9_P16**
A to Z ↓	0.0541	0.0464	5.0025	2.5226
A to Z ↑	0.0312	0.0322	8.0742	4.0565
B to Z ↓	0.0531	0.0452	5.0046	2.5214
B to Z ↑	0.0300	0.0301	8.0801	4.0584
	X19_P16	**X29_P16**	**X19_P16**	**X29_P16**
A to Z ↓	0.0469	0.0556	1.2065	0.8278
A to Z ↑	0.0318	0.0361	1.9309	1.2943
B to Z ↓	0.0434	0.0525	1.2054	0.8274
B to Z ↑	0.0289	0.0335	1.9272	1.2934

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	2.368e-06	1.000e-20
X9_P16	4.383e-06	1.000e-20
X19_P16	8.993e-06	1.000e-20
X29_P16	1.159e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16	X29_P16
A (output stable)	8.762e-06	1.640e-05	6.632e-05	6.640e-05
B (output stable)	1.149e-05	2.417e-05	9.761e-05	9.758e-05
A to Z	1.297e-03	2.056e-03	4.345e-03	6.030e-03
B to Z	1.207e-03	1.893e-03	3.800e-03	5.498e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

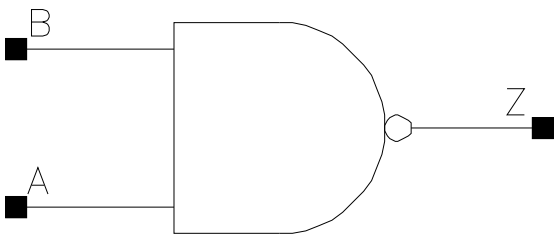
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16	X29_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X9_P16	0.800	0.952	0.7616
X14_P16	0.800	1.088	0.8704
X18_P16	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P16	X9_P16	X14_P16	X18_P16
A	0.0007	0.0006	0.0006	0.0006
B	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X9_P16**	**X5_P16**	**X9_P16**
A to Z ↓	0.0417	0.0485	4.4814	2.4640
A to Z ↑	0.0442	0.0486	7.7270	4.0585
B to Z ↓	0.0426	0.0505	4.4852	2.4650
B to Z ↑	0.0416	0.0469	7.7191	4.0641
	X14_P16	**X18_P16**	**X14_P16**	**X18_P16**
A to Z ↓	0.0542	0.0576	1.7043	1.2946
A to Z ↑	0.0523	0.0537	2.6999	2.0690
B to Z ↓	0.0562	0.0594	1.7031	1.2948
B to Z ↑	0.0507	0.0520	2.6978	2.0687

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	5.054e-06	1.000e-20
X9_P16	6.172e-06	1.000e-20
X14_P16	7.478e-06	1.000e-20
X18_P16	8.153e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X9_P16	X14_P16	X18_P16
A (output stable)	9.778e-06	9.164e-06	9.254e-06	9.546e-06
B (output stable)	2.091e-05	1.897e-05	1.907e-05	1.839e-05
A to Z	2.353e-03	3.025e-03	3.898e-03	4.336e-03
B to Z	2.240e-03	2.929e-03	3.803e-03	4.241e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

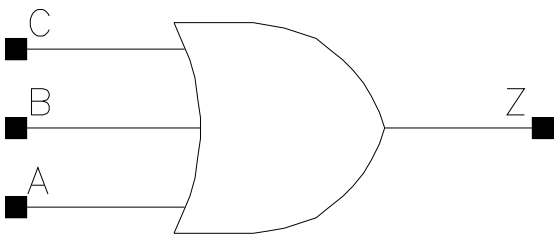
Pin Cycle (vdds)	X5_P16	X9_P16	X14_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.680	0.5440
X10_P16	0.800	0.952	0.7616
X14_P16	0.800	1.496	1.1968
X19_P16	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0005	0.0007	0.0011	0.0018
B	0.0004	0.0006	0.0013	0.0017
C	0.0005	0.0006	0.0011	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0737	0.0642	5.2090	2.4712
A to Z ↑	0.0361	0.0311	8.1046	3.8480
B to Z ↓	0.0712	0.0619	5.2127	2.4713
B to Z ↑	0.0355	0.0298	8.0943	3.8439
C to Z ↓	0.0697	0.0589	5.2128	2.4713
C to Z ↑	0.0342	0.0280	8.1009	3.8442
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0591	0.0573	1.6444	1.2518

A to Z ↑	0.0285	0.0284	2.6104	1.9886
B to Z ↓	0.0589	0.0544	1.6447	1.2518
B to Z ↑	0.0273	0.0275	2.6036	1.9842
C to Z ↓	0.0502	0.0493	1.6437	1.2535
C to Z ↑	0.0248	0.0251	2.6026	1.9796

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	2.221e-06	1.000e-20
X10_P16	4.430e-06	1.000e-20
X14_P16	7.435e-06	1.000e-20
X19_P16	1.001e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	1.156e-05	2.099e-05	4.379e-05	8.440e-05
B (output stable)	-1.391e-06	1.200e-06	1.817e-05	3.157e-06
C (output stable)	1.058e-05	2.417e-05	9.132e-05	8.854e-05
A to Z	1.542e-03	2.512e-03	4.117e-03	5.925e-03
B to Z	1.445e-03	2.341e-03	3.848e-03	5.292e-03
C to Z	1.362e-03	2.173e-03	3.278e-03	4.670e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

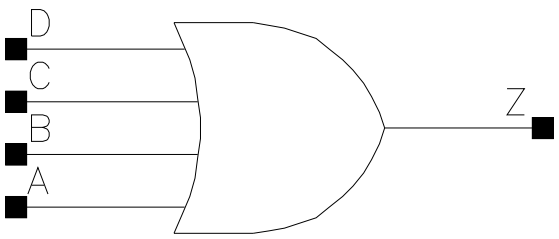
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	1.224	0.9792
X8_P16	0.800	1.496	1.1968
X12_P16	0.800	2.176	1.7408
X15_P16	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X12_P16	X15_P16
A	0.0004	0.0006	0.0011	0.0012
B	0.0004	0.0007	0.0010	0.0012
C	0.0004	0.0006	0.0011	0.0013
D	0.0005	0.0007	0.0010	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
A to Z ↓	0.0558	0.0520	8.0779	4.2483
A to Z ↑	0.0326	0.0326	7.5904	3.9693
B to Z ↓	0.0565	0.0522	8.0807	4.2456
B to Z ↑	0.0315	0.0312	7.5771	3.9668
C to Z ↓	0.0597	0.0506	8.0942	4.2416
C to Z ↑	0.0335	0.0314	7.7215	3.9824

D to Z ↓	0.0611	0.0511	8.0923	4.2411
D to Z ↑	0.0327	0.0301	7.7281	3.9803
	X12_P16	**X15_P16**	**X12_P16**	**X15_P16**
A to Z ↓	0.0534	0.0530	2.9250	2.1919
A to Z ↑	0.0335	0.0314	2.5735	1.9582
B to Z ↓	0.0511	0.0497	2.9261	2.1933
B to Z ↑	0.0316	0.0290	2.5711	1.9540
C to Z ↓	0.0514	0.0505	2.9209	2.1894
C to Z ↑	0.0316	0.0296	2.5692	1.9660
D to Z ↓	0.0493	0.0476	2.9210	2.1894
D to Z ↑	0.0297	0.0274	2.5669	1.9649

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	2.786e-06	1.000e-20
X8_P16	5.602e-06	1.000e-20
X12_P16	7.115e-06	1.000e-20
X15_P16	1.042e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	3.468e-04	6.110e-04	9.551e-04	1.290e-03
B (output stable)	3.166e-04	5.501e-04	8.206e-04	1.082e-03
C (output stable)	3.350e-04	5.870e-04	8.732e-04	1.195e-03
D (output stable)	3.063e-04	5.268e-04	7.395e-04	1.005e-03
A to Z	1.430e-03	2.848e-03	4.057e-03	5.379e-03
B to Z	1.358e-03	2.699e-03	3.723e-03	4.838e-03
C to Z	1.440e-03	2.482e-03	3.558e-03	4.547e-03
D to Z	1.376e-03	2.337e-03	3.232e-03	4.066e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

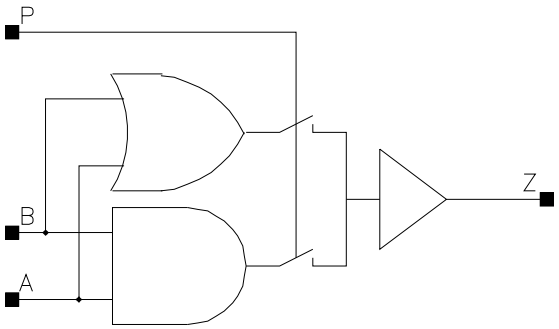
Pin Cycle (vdds)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.952	0.7616
X10_P16	1.600	0.816	1.3056
X14_P16	1.600	1.224	1.9584
X19_P16	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0009	0.0011	0.0022	0.0022
B	0.0009	0.0012	0.0022	0.0022
P	0.0005	0.0007	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0673	0.0594	5.1061	2.3676
A to Z ↑	0.0364	0.0418	8.1306	3.8814
B to Z ↓	0.0663	0.0603	5.1298	2.3790
B to Z ↑	0.0378	0.0438	8.1295	3.8866
P to Z ↓	0.0591	0.0557	5.1225	2.3791
P to Z ↑	0.0357	0.0420	8.1230	3.8829
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**

A to Z ↓	0.0543	0.0584	1.6200	1.1982
A to Z ↑	0.0396	0.0418	2.6357	1.9713
B to Z ↓	0.0514	0.0553	1.6361	1.2086
B to Z ↑	0.0392	0.0417	2.6351	1.9723
P to Z ↓	0.0482	0.0530	1.6410	1.2118
P to Z ↑	0.0385	0.0414	2.6372	1.9719

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	2.850e-06	1.000e-20
X10_P16	6.220e-06	1.000e-20
X14_P16	1.011e-05	1.000e-20
X19_P16	1.160e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	2.245e-05	3.333e-05	1.014e-04	9.696e-05
B (output stable)	2.798e-05	4.993e-05	2.058e-04	1.994e-04
P (output stable)	8.627e-05	1.394e-04	2.397e-04	2.384e-04
A to Z	1.574e-03	2.927e-03	4.760e-03	5.616e-03
B to Z	1.523e-03	2.885e-03	4.434e-03	5.300e-03
P to Z	1.346e-03	2.644e-03	4.196e-03	5.108e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

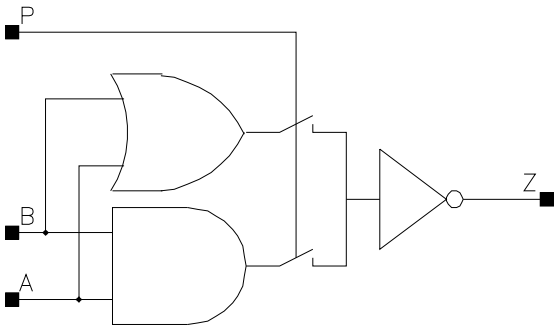
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.600	0.544	0.8704
X10_P16	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P16	X10_P16
A	0.0011	0.0020
B	0.0010	0.0018
P	0.0007	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0208	0.0197	8.0844	4.2048
A to Z ↑	0.0338	0.0316	14.2647	7.2026
B to Z ↓	0.0219	0.0189	8.0218	4.2179
B to Z ↑	0.0334	0.0279	14.2382	7.2690
P to Z ↓	0.0215	0.0171	8.1800	4.2483
P to Z ↑	0.0306	0.0237	14.3430	7.2372

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	2.878e-06	1.000e-20
X10_P16	5.317e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16
A (output stable)	3.237e-05	1.017e-04
B (output stable)	4.493e-05	1.970e-04
P (output stable)	1.141e-04	2.702e-04
A to Z	1.180e-03	2.108e-03
B to Z	1.099e-03	1.718e-03
P to Z	9.022e-04	1.439e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

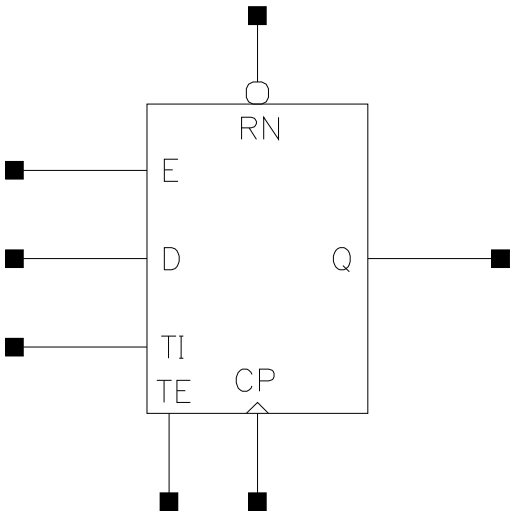
Pin Cycle (vdds)	X5_P16	X10_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.600	2.992	4.7872
X10_P16	1.600	3.128	5.0048
X19_P16	1.600	3.264	5.2224
X23_P16	1.600	3.264	5.2224
X29_P16	1.600	3.536	5.6576
X34_P16	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16	X23_P16
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0011	0.0011	0.0011	0.0011

RN	0.0009	0.0008	0.0009	0.0008
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P16	X34_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0011	0.0011		
RN	0.0009	0.0009		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
CP to Q ↓	0.0826	0.1355	4.6740	2.3137
CP to Q ↑	0.1155	0.1865	7.6913	3.8663
RN to Q ↓	0.0713	0.1336	4.7087	2.3108
	X19_P16	**X23_P16**	**X19_P16**	**X23_P16**
CP to Q ↓	0.1469	0.1482	1.1884	0.8903
CP to Q ↑	0.1927	0.1906	1.9493	1.9187
RN to Q ↓	0.1357	0.1372	1.1834	0.8868
	X29_P16	**X34_P16**	**X29_P16**	**X34_P16**
CP to Q ↓	0.1262	0.1250	0.7787	0.6093
CP to Q ↑	0.1538	0.1549	1.2922	1.2890
RN to Q ↓	0.1178	0.1165	0.7789	0.6100

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P16	X10_P16	X19_P16	X23_P16
CP ↓	min_pulse_width to CP	0.1166	0.1132	0.1132	0.1125
CP ↑	min_pulse_width to CP	0.0715	0.0669	0.0682	0.0717
D ↓	hold_rising to CP	-0.0827	-0.0827	-0.0827	-0.0827
D ↑	hold_rising to CP	-0.0316	-0.0342	-0.0342	-0.0342
D ↓	setup_rising to CP	0.1367	0.1377	0.1351	0.1351
D ↑	setup_rising to CP	0.0639	0.0644	0.0644	0.0612
E ↓	hold_rising to CP	-0.0751	-0.0746	-0.0751	-0.0751
E ↑	hold_rising to CP	-0.0338	-0.0338	-0.0338	-0.0338
E ↓	setup_rising to CP	0.1881	0.1881	0.1885	0.1891
E ↑	setup_rising to CP	0.1403	0.1345	0.1345	0.1345
RN ↓	min_pulse_width to RN	0.0952	0.0859	0.0903	0.0903
RN ↑	recovery_rising to CP	-0.0022	-0.0071	-0.0071	-0.0071
RN ↑	removal_rising to CP	0.0167	0.0167	0.0167	0.0167
TE ↓	hold_rising to CP	-0.0458	-0.0458	-0.0458	-0.0458

TE ↑	hold_rising to CP	-0.0240	-0.0240	-0.0240	-0.0240
TE ↓	setup_rising to CP	0.1099	0.1078	0.1051	0.1051
TE ↑	setup_rising to CP	0.1447	0.1426	0.1394	0.1394
TI ↓	hold_rising to CP	-0.0844	-0.0844	-0.0844	-0.0844
TI ↑	hold_rising to CP	-0.0218	-0.0253	-0.0253	-0.0253
TI ↓	setup_rising to CP	0.1371	0.1378	0.1338	0.1338
TI ↑	setup_rising to CP	0.0558	0.0515	0.0515	0.0515
		X29_P16	X34_P16		
CP ↓	min_pulse_width to CP	0.1132	0.1132		
CP ↑	min_pulse_width to CP	0.0681	0.0716		
D ↓	hold_rising to CP	-0.0827	-0.0827		
D ↑	hold_rising to CP	-0.0316	-0.0316		
D ↓	setup_rising to CP	0.1371	0.1371		
D ↑	setup_rising to CP	0.0644	0.0644		
E ↓	hold_rising to CP	-0.0751	-0.0751		
E ↑	hold_rising to CP	-0.0338	-0.0338		
E ↓	setup_rising to CP	0.1885	0.1891		
E ↑	setup_rising to CP	0.1371	0.1371		
RN ↓	min_pulse_width to RN	0.0947	0.0974		
RN ↑	recovery_rising to CP	-0.0012	-0.0012		
RN ↑	removal_rising to CP	0.0167	0.0167		
TE ↓	hold_rising to CP	-0.0458	-0.0458		
TE ↑	hold_rising to CP	-0.0240	-0.0240		
TE ↓	setup_rising to CP	0.1078	0.1078		
TE ↑	setup_rising to CP	0.1452	0.1452		
TI ↓	hold_rising to CP	-0.0844	-0.0844		
TI ↑	hold_rising to CP	-0.0218	-0.0218		
TI ↓	setup_rising to CP	0.1378	0.1378		
TI ↑	setup_rising to CP	0.0558	0.0515		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	1.159e-05	1.000e-20
X10_P16	1.408e-05	1.000e-20
X19_P16	1.811e-05	1.000e-20
X23_P16	1.902e-05	1.000e-20

X29_P16	2.302e-05	1.000e-20
X34_P16	2.444e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

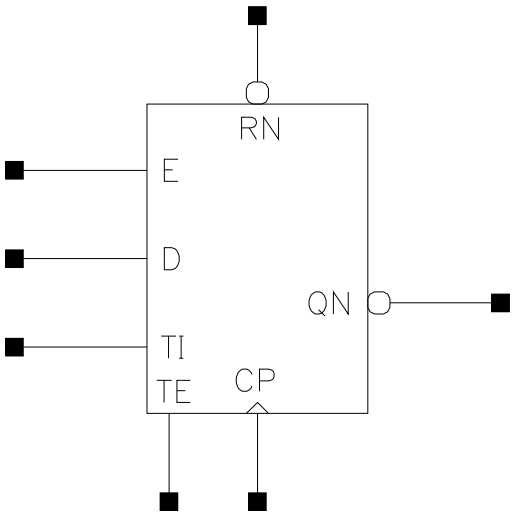
Pin Cycle	X5_P16	X10_P16	X19_P16	X23_P16
Clock 100Mhz Data 0Mhz	6.342e-03	6.331e-03	6.337e-03	6.339e-03
Clock 100Mhz Data 25Mhz	6.550e-03	6.910e-03	7.472e-03	7.531e-03
Clock 100Mhz Data 50Mhz	6.758e-03	7.489e-03	8.607e-03	8.722e-03
Clock = 0 Data 100Mhz	3.681e-03	3.681e-03	3.681e-03	3.681e-03
Clock = 1 Data 100Mhz	1.519e-03	1.519e-03	1.519e-03	1.519e-03
	X29_P16	X34_P16		
Clock 100Mhz Data 0Mhz	6.339e-03	6.340e-03		
Clock 100Mhz Data 25Mhz	8.104e-03	8.256e-03		
Clock 100Mhz Data 50Mhz	9.869e-03	1.017e-02		
Clock = 0 Data 100Mhz	3.681e-03	3.681e-03		
Clock = 1 Data 100Mhz	1.519e-03	1.519e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.600	2.992	4.7872
X10_P16	1.600	3.128	5.0048
X19_P16	1.600	3.264	5.2224
X23_P16	1.600	3.264	5.2224
X29_P16	1.600	3.536	5.6576
X34_P16	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16	X23_P16
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0011	0.0012	0.0012	0.0012

RN	0.0008	0.0008	0.0009	0.0009
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P16	X34_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0012	0.0011		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
CP to QN ↓	0.1641	0.1398	4.7096	2.3082
CP to QN ↑	0.1121	0.1050	7.6849	3.8652
RN to QN ↑	0.1097	0.0965	7.6797	3.8683
	X19_P16	**X23_P16**	**X19_P16**	**X23_P16**
CP to QN ↓	0.1469	0.1485	1.1801	0.8904
CP to QN ↑	0.1151	0.1123	1.9480	1.9171
RN to QN ↑	0.1071	0.1041	1.9487	1.9182
	X29_P16	**X34_P16**	**X29_P16**	**X34_P16**
CP to QN ↓	0.2044	0.2005	0.7785	0.6028
CP to QN ↑	0.1519	0.1503	1.2927	1.2900
RN to QN ↑	0.1491	0.1485	1.2936	1.2890

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P16	X10_P16	X19_P16	X23_P16
CP ↓	min_pulse_width to CP	0.1132	0.1166	0.1149	0.1166
CP ↑	min_pulse_width to CP	0.0668	0.0668	0.0716	0.0716
D ↓	hold_rising to CP	-0.0827	-0.0827	-0.0827	-0.0827
D ↑	hold_rising to CP	-0.0342	-0.0316	-0.0316	-0.0316
D ↓	setup_rising to CP	0.1367	0.1367	0.1367	0.1367
D ↑	setup_rising to CP	0.0644	0.0639	0.0644	0.0644
E ↓	hold_rising to CP	-0.0751	-0.0751	-0.0751	-0.0751
E ↑	hold_rising to CP	-0.0338	-0.0338	-0.0338	-0.0338
E ↓	setup_rising to CP	0.1885	0.1881	0.1881	0.1881
E ↑	setup_rising to CP	0.1403	0.1399	0.1403	0.1403
RN ↓	min_pulse_width to RN	0.0881	0.0925	0.0996	0.0996
RN ↑	recovery_rising to CP	-0.0012	-0.0012	-0.0012	-0.0012
RN ↑	removal_rising to CP	0.0167	0.0167	0.0167	0.0167
TE ↓	hold_rising to CP	-0.0458	-0.0458	-0.0458	-0.0458

TE ↑	hold_rising to CP	-0.0240	-0.0240	-0.0240	-0.0240
TE ↓	setup_rising to CP	0.1099	0.1099	0.1099	0.1099
TE ↑	setup_rising to CP	0.1447	0.1447	0.1447	0.1447
TI ↓	hold_rising to CP	-0.0844	-0.0844	-0.0844	-0.0844
TI ↑	hold_rising to CP	-0.0253	-0.0218	-0.0218	-0.0218
TI ↓	setup_rising to CP	0.1371	0.1387	0.1387	0.1387
TI ↑	setup_rising to CP	0.0515	0.0558	0.0558	0.0558
		X29_P16	X34_P16		
CP ↓	min_pulse_width to CP	0.1118	0.1118		
CP ↑	min_pulse_width to CP	0.0669	0.0669		
D ↓	hold_rising to CP	-0.0827	-0.0827		
D ↑	hold_rising to CP	-0.0342	-0.0342		
D ↓	setup_rising to CP	0.1318	0.1318		
D ↑	setup_rising to CP	0.0612	0.0612		
E ↓	hold_rising to CP	-0.0773	-0.0779		
E ↑	hold_rising to CP	-0.0338	-0.0338		
E ↓	setup_rising to CP	0.1881	0.1891		
E ↑	setup_rising to CP	0.1345	0.1345		
RN ↓	min_pulse_width to RN	0.0881	0.0859		
RN ↑	recovery_rising to CP	-0.0071	-0.0071		
RN ↑	removal_rising to CP	0.0167	0.0167		
TE ↓	hold_rising to CP	-0.0458	-0.0458		
TE ↑	hold_rising to CP	-0.0240	-0.0240		
TE ↓	setup_rising to CP	0.1051	0.1051		
TE ↑	setup_rising to CP	0.1394	0.1394		
TI ↓	hold_rising to CP	-0.0886	-0.0844		
TI ↑	hold_rising to CP	-0.0253	-0.0251		
TI ↓	setup_rising to CP	0.1338	0.1338		
TI ↑	setup_rising to CP	0.0515	0.0515		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	1.183e-05	1.000e-20
X10_P16	1.416e-05	1.000e-20
X19_P16	1.854e-05	1.000e-20
X23_P16	1.997e-05	1.000e-20

X29_P16	2.329e-05	1.000e-20
X34_P16	2.553e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

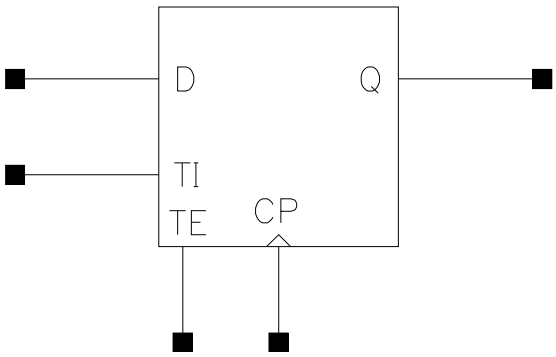
Pin Cycle	X5_P16	X10_P16	X19_P16	X23_P16
Clock 100Mhz Data 0Mhz	6.335e-03	6.341e-03	6.343e-03	6.342e-03
Clock 100Mhz Data 25Mhz	6.592e-03	6.889e-03	7.472e-03	7.518e-03
Clock 100Mhz Data 50Mhz	6.850e-03	7.436e-03	8.601e-03	8.694e-03
Clock = 0 Data 100Mhz	3.681e-03	3.682e-03	3.681e-03	3.681e-03
Clock = 1 Data 100Mhz	1.519e-03	1.519e-03	1.519e-03	1.519e-03
	X29_P16	X34_P16		
Clock 100Mhz Data 0Mhz	6.343e-03	6.343e-03		
Clock 100Mhz Data 25Mhz	8.135e-03	8.283e-03		
Clock 100Mhz Data 50Mhz	9.928e-03	1.022e-02		
Clock = 0 Data 100Mhz	3.681e-03	3.681e-03		
Clock = 1 Data 100Mhz	1.519e-03	1.519e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P16	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P16	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P16	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P16	C8T28SOI_LLHF_-SDFPQX3_P16	C8T28SOIDV_LL_-SDFPQX5_P16	C8T28SOIDV_LL_-SDFPQX10_P16
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P16	C8T28SOIDV_LL_-SDFPQX23_P16	C8T28SOIDV_LL_-SDFPQX29_P16	
CP	0.0005	0.0005	0.0005	
D	0.0005	0.0005	0.0005	
TE	0.0009	0.0009	0.0009	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P16	**C8T28SOI_LLHF_-SDFPQX3_P16**	**C8T28SOI_LL_-SDFPQX5_P16**	**C8T28SOI_LLHF_-SDFPQX3_P16**
CP to Q ↓	0.0898	0.0763	4.9660	7.7514
CP to Q ↑	0.0828	0.0984	7.7569	11.9472
	C8T28SOIDV_LL_-SDFPQX5_P16	**C8T28SOIDV_LL_-SDFPQX10_P16**	**C8T28SOIDV_LL_-SDFPQX5_P16**	**C8T28SOIDV_LL_-SDFPQX10_P16**
CP to Q ↓	0.0776	0.1097	4.6764	2.2411
CP to Q ↑	0.0987	0.1460	7.6852	3.8326
	C8T28SOIDV_LL_-SDFPQX19_P16	**C8T28SOIDV_LL_-SDFPQX23_P16**	**C8T28SOIDV_LL_-SDFPQX19_P16**	**C8T28SOIDV_LL_-SDFPQX23_P16**
CP to Q ↓	0.1201	0.1242	1.1695	0.8846
CP to Q ↑	0.1546	0.1584	1.9384	1.9207
	C8T28SOIDV_LL_-SDFPQX29_P16		**C8T28SOIDV_LL_-SDFPQX29_P16**	
CP to Q ↓	0.1181		0.7864	
CP to Q ↑	0.1463		1.2846	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P16	C8T28SOI_-LLHF_-SDFPQX3_P16	C8T28SOIDV_-LL_SDFPQX5_-P16	C8T28SOIDV_-LL_SDFPQX10_-P16
CP ↓	min_pulse_width to CP	0.1541	0.1499	0.1367	0.1332
CP ↑	min_pulse_width to CP	0.0720	0.0580	0.0622	0.0576
D ↓	hold_rising to CP	-0.0783	-0.1528	-0.0246	-0.0241
D ↑	hold_rising to CP	-0.0234	-0.0218	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1269	0.2176	0.0888	0.0888
D ↑	setup_rising to CP	0.0563	0.0563	0.0368	0.0368
TE ↓	hold_rising to CP	-0.0502	-0.0550	-0.0202	-0.0192
TE ↑	hold_rising to CP	-0.0244	-0.0191	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.1279	0.1760	0.0835	0.0814
TE ↑	setup_rising to CP	0.1590	0.2105	0.1648	0.1648

TI ↓	hold_rising to CP	-0.1039	-0.1504	-0.0906	-0.0948
TI ↑	hold_rising to CP	-0.0215	-0.0202	-0.0266	-0.0266
TI ↓	setup_rising to CP	0.1573	0.1997	0.1546	0.1546
TI ↑	setup_rising to CP	0.0528	0.0502	0.0528	0.0528
		C8T28SOIDV_-LL_SDFPQX19_-P16	C8T28SOIDV_-LL_SDFPQX23_-P16	C8T28SOIDV_-LL_SDFPQX29_-P16	
CP ↓	min_pulse_width to CP	0.1326	0.1326	0.1373	
CP ↑	min_pulse_width to CP	0.0576	0.0576	0.0576	
D ↓	hold_rising to CP	-0.0241	-0.0241	-0.0241	
D ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120	
D ↓	setup_rising to CP	0.0830	0.0830	0.0888	
D ↑	setup_rising to CP	0.0368	0.0368	0.0368	
TE ↓	hold_rising to CP	-0.0192	-0.0192	-0.0192	
TE ↑	hold_rising to CP	-0.0244	-0.0244	-0.0244	
TE ↓	setup_rising to CP	0.0814	0.0814	0.0841	
TE ↑	setup_rising to CP	0.1589	0.1589	0.1638	
TI ↓	hold_rising to CP	-0.0948	-0.0948	-0.0954	
TI ↑	hold_rising to CP	-0.0266	-0.0266	-0.0266	
TI ↓	setup_rising to CP	0.1537	0.1537	0.1589	
TI ↑	setup_rising to CP	0.0528	0.0528	0.0528	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P16	9.709e-06	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P16	8.801e-06	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P16	9.088e-06	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P16	1.233e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P16	1.506e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P16	1.633e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P16	1.924e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P16	C8T28SOI_LLHF_-SDFPQX3_P16	C8T28SOIDV_LL_-SDFPQX5_P16	C8T28SOIDV_LL_-SDFPQX10_P16
Clock 100Mhz Data 0Mhz	6.054e-03	5.820e-03	5.591e-03	5.472e-03
Clock 100Mhz Data 25Mhz	5.802e-03	5.586e-03	5.462e-03	5.730e-03
Clock 100Mhz Data 50Mhz	5.550e-03	5.351e-03	5.333e-03	5.989e-03

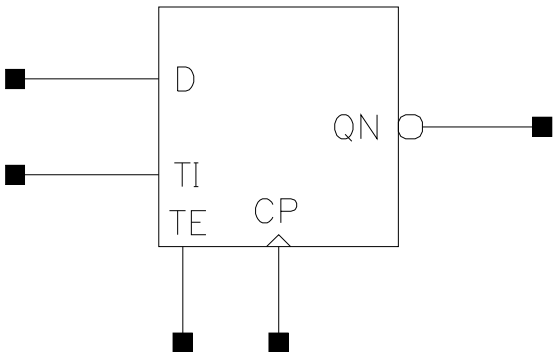
Clock = 0 Data 100Mhz	2.886e-03	2.989e-03	2.845e-03	2.770e-03
Clock = 1 Data 100Mhz	2.305e-05	3.886e-04	2.675e-04	2.071e-04
	C8T28SOIDV_LL_-SDFPQX19_P16	C8T28SOIDV_LL_-SDFPQX23_P16	C8T28SOIDV_LL_-SDFPQX29_P16	
Clock 100Mhz Data 0Mhz	5.403e-03	5.358e-03	5.326e-03	
Clock 100Mhz Data 25Mhz	6.127e-03	6.163e-03	6.590e-03	
Clock 100Mhz Data 50Mhz	6.850e-03	6.968e-03	7.855e-03	
Clock = 0 Data 100Mhz	2.724e-03	2.693e-03	2.674e-03	
Clock = 1 Data 100Mhz	1.708e-04	1.466e-04	1.294e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P16	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P16	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P16	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P16	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P16	C8T28SOI_LLHF_-SDFPQNX3_P16	C8T28SOIDV_LL_-SDFPQNX5_P16	C8T28SOIDV_LL_-SDFPQNX10_P16

CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P16	C8T28SOIDV_LL_-SDFPQNX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P16	**C8T28SOI_LLHF_-SDFPQNX3_P16**	**C8T28SOI_LL_-SDFPQNX5_P16**	**C8T28SOI_LLHF_-SDFPQNX3_P16**
CP to QN ↓	0.1122	0.1218	4.7297	7.2402
CP to QN ↑	0.0975	0.0931	8.4223	11.6847
	C8T28SOIDV_LL_-SDFPQNX5_P16	**C8T28SOIDV_LL_-SDFPQNX10_P16**	**C8T28SOIDV_LL_-SDFPQNX5_P16**	**C8T28SOIDV_LL_-SDFPQNX10_P16**
CP to QN ↓	0.1252	0.1162	4.5427	2.2677
CP to QN ↑	0.0881	0.0967	7.6059	3.8382
	C8T28SOIDV_LL_-SDFPQNX19_P16	**C8T28SOIDV_LL_-SDFPQNX29_P16**	**C8T28SOIDV_LL_-SDFPQNX19_P16**	**C8T28SOIDV_LL_-SDFPQNX29_P16**
CP to QN ↓	0.1314	0.1534	1.1799	0.7851
CP to QN ↑	0.1145	0.1293	1.9594	1.2879

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P16	C8T28SOI_-LLHF_-SDFPQNX3_P16	C8T28SOIDV_-LL_SDFPQNX5_-P16	C8T28SOIDV_-LL_-SDFPQNX10_-P16
CP ↓	min_pulse_width to CP	0.1541	0.1458	0.1367	0.1367
CP ↑	min_pulse_width to CP	0.0578	0.0532	0.0575	0.0622
D ↓	hold_rising to CP	-0.0778	-0.1528	-0.0241	-0.0246
D ↑	hold_rising to CP	-0.0234	-0.0208	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1269	0.2118	0.0888	0.0888
D ↑	setup_rising to CP	0.0536	0.0563	0.0368	0.0368
TE ↓	hold_rising to CP	-0.0502	-0.0550	-0.0192	-0.0197
TE ↑	hold_rising to CP	-0.0244	-0.0185	-0.0191	-0.0244
TE ↓	setup_rising to CP	0.1274	0.1706	0.0831	0.0835
TE ↑	setup_rising to CP	0.1590	0.2110	0.1648	0.1648
TI ↓	hold_rising to CP	-0.1039	-0.1504	-0.0948	-0.0948
TI ↑	hold_rising to CP	-0.0215	-0.0202	-0.0218	-0.0266
TI ↓	setup_rising to CP	0.1566	0.2004	0.1546	0.1546

TI ↑	setup_rising to CP	0.0528	0.0502	0.0479	0.0528
		C8T28SOIDV_-LL_-SDFPQNX19_-P16	C8T28SOIDV_-LL_-SDFPQNX29_-P16		
CP ↓	min_pulse_width to CP	0.1326	0.1326		
CP ↑	min_pulse_width to CP	0.0717	0.0576		
D ↓	hold_rising to CP	-0.0241	-0.0241		
D ↑	hold_rising to CP	-0.0120	-0.0120		
D ↓	setup_rising to CP	0.0888	0.0830		
D ↑	setup_rising to CP	0.0368	0.0368		
TE ↓	hold_rising to CP	-0.0192	-0.0192		
TE ↑	hold_rising to CP	-0.0244	-0.0244		
TE ↓	setup_rising to CP	0.0814	0.0814		
TE ↑	setup_rising to CP	0.1648	0.1616		
TI ↓	hold_rising to CP	-0.0948	-0.0948		
TI ↑	hold_rising to CP	-0.0266	-0.0266		
TI ↓	setup_rising to CP	0.1546	0.1537		
TI ↑	setup_rising to CP	0.0528	0.0528		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P16	9.612e-06	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P16	8.951e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P16	9.158e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P16	1.203e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P16	1.508e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P16	2.195e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P16	C8T28SOI_LLHF_-SDFPQNX3_P16	C8T28SOIDV_LL_-SDFPQNX5_P16	C8T28SOIDV_LL_-SDFPQNX10_P16
Clock 100Mhz Data 0Mhz	6.054e-03	5.885e-03	5.641e-03	5.509e-03
Clock 100Mhz Data 25Mhz	5.777e-03	5.665e-03	5.452e-03	5.704e-03
Clock 100Mhz Data 50Mhz	5.500e-03	5.445e-03	5.263e-03	5.900e-03
Clock = 0 Data 100Mhz	2.887e-03	3.002e-03	2.857e-03	2.781e-03
Clock = 1 Data 100Mhz	2.315e-05	3.909e-04	2.690e-04	2.082e-04

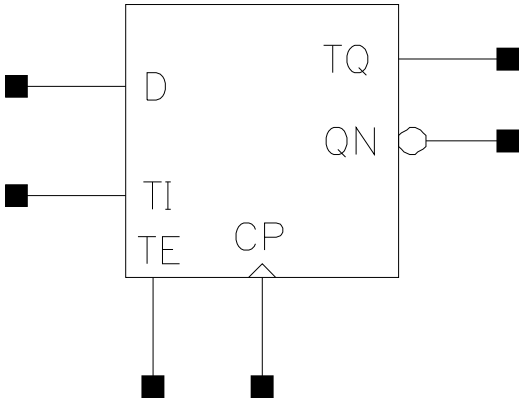
	C8T28SOIDV_LL_-SDFPQNX19_P16	C8T28SOIDV_LL_-SDFPQNX29_P16		
Clock 100Mhz Data 0Mhz	5.433e-03	5.380e-03		
Clock 100Mhz Data 25Mhz	6.205e-03	7.035e-03		
Clock 100Mhz Data 50Mhz	6.977e-03	8.691e-03		
Clock = 0 Data 100Mhz	2.731e-03	2.702e-03		
Clock = 1 Data 100Mhz	1.717e-04	1.474e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P16	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P16	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P16	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P16	C8T28SOI_LLHF_-SDFPQNTX3_P16	C8T28SOIDV_LL_-SDFPQNTX5_P16	C8T28SOIDV_LL_-SDFPQNTX10_P16
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P16	C8T28SOIDV_LL_-SDFPQNTX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQNTX5_P16	**C8T28SOI_LLHF_-SDFPQNTX3_P16**	**C8T28SOI_LL_-SDFPQNTX5_P16**	**C8T28SOI_LLHF_-SDFPQNTX3_P16**
CP to QN ↓	0.1267	0.1335	4.8862	7.3859
CP to QN ↑	0.1267	0.1172	8.4123	11.6703
CP to TQ ↓	0.1031	0.0806	13.4399	8.6525
CP to TQ ↑	0.1051	0.0974	39.8769	21.4585
	C8T28SOIDV_LL_-SDFPQNTX5_P16	**C8T28SOIDV_LL_-SDFPQNTX10_P16**	**C8T28SOIDV_LL_-SDFPQNTX5_P16**	**C8T28SOIDV_LL_-SDFPQNTX10_P16**
CP to QN ↓	0.1346	0.1298	4.4944	2.2918
CP to QN ↑	0.1050	0.1056	7.5890	3.8393
CP to TQ ↓	0.0724	0.0761	8.5718	8.9756
CP to TQ ↑	0.0988	0.1015	16.8242	17.6321
	C8T28SOIDV_LL_-SDFPQNTX19_P16	**C8T28SOIDV_LL_-SDFPQNTX29_P16**	**C8T28SOIDV_LL_-SDFPQNTX19_P16**	**C8T28SOIDV_LL_-SDFPQNTX29_P16**
CP to QN ↓	0.1341	0.1568	1.1768	0.7871
CP to QN ↑	0.1153	0.1374	1.9426	1.2840
CP to TQ ↓	0.0793	0.0767	8.7627	9.0392
CP to TQ ↑	0.1049	0.1060	17.9601	23.4212

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_-P16	C8T28SOI_-LLHF_-SDFPQNTX3_-P16	C8T28SOIDV_-LL_-SDFPQNTX5_-P16	C8T28SOIDV_-LL_-SDFPQNTX10_-P16
CP ↓	min_pulse_width to CP	0.1541	0.1458	0.1367	0.1367
CP ↑	min_pulse_width to CP	0.0781	0.0687	0.0622	0.0635
D ↓	hold_rising to CP	-0.0778	-0.1505	-0.0246	-0.0246
D ↑	hold_rising to CP	-0.0234	-0.0208	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1269	0.2122	0.0888	0.0888

D ↑	setup_rising to CP	0.0536	0.0558	0.0368	0.0368
TE ↓	hold_rising to CP	-0.0502	-0.0550	-0.0197	-0.0202
TE ↑	hold_rising to CP	-0.0244	-0.0181	-0.0196	-0.0244
TE ↓	setup_rising to CP	0.1253	0.1707	0.0831	0.0835
TE ↑	setup_rising to CP	0.1590	0.2078	0.1644	0.1648
TI ↓	hold_rising to CP	-0.1039	-0.1453	-0.0948	-0.0906
TI ↑	hold_rising to CP	-0.0215	-0.0202	-0.0218	-0.0266
TI ↓	setup_rising to CP	0.1573	0.1948	0.1546	0.1546
TI ↑	setup_rising to CP	0.0528	0.0499	0.0515	0.0528
		C8T28SOIDV_-LL_-SDFPQNTX19_-P16	C8T28SOIDV_-LL_-SDFPQNTX29_-P16		
CP ↓	min_pulse_width to CP	0.1367	0.1367		
CP ↑	min_pulse_width to CP	0.0717	0.0622		
D ↓	hold_rising to CP	-0.0246	-0.0246		
D ↑	hold_rising to CP	-0.0120	-0.0120		
D ↓	setup_rising to CP	0.0888	0.0888		
D ↑	setup_rising to CP	0.0368	0.0368		
TE ↓	hold_rising to CP	-0.0202	-0.0197		
TE ↑	hold_rising to CP	-0.0244	-0.0244		
TE ↓	setup_rising to CP	0.0835	0.0835		
TE ↑	setup_rising to CP	0.1648	0.1648		
TI ↓	hold_rising to CP	-0.0906	-0.0906		
TI ↑	hold_rising to CP	-0.0266	-0.0266		
TI ↓	setup_rising to CP	0.1546	0.1546		
TI ↑	setup_rising to CP	0.0528	0.0528		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P16	9.715e-06	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P16	9.587e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P16	9.818e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P16	1.154e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P16	1.499e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P16	2.242e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

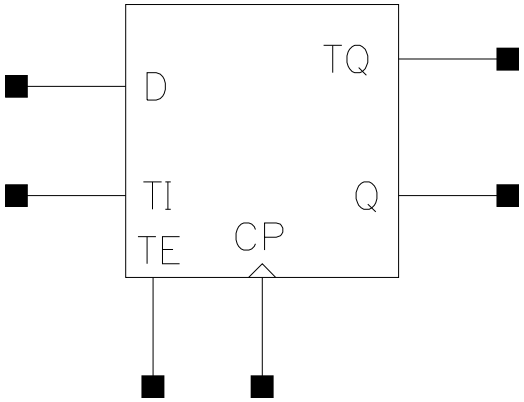
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P16	C8T28SOI_LLHF_-SDFPQNTX3_P16	C8T28SOIDV_LL_-SDFPQNTX5_P16	C8T28SOIDV_LL_-SDFPQNTX10_P16
Clock 100Mhz Data 0Mhz	6.056e-03	5.885e-03	5.637e-03	5.506e-03
Clock 100Mhz Data 25Mhz	6.011e-03	5.839e-03	5.621e-03	5.697e-03
Clock 100Mhz Data 50Mhz	5.966e-03	5.794e-03	5.606e-03	5.889e-03
Clock = 0 Data 100Mhz	2.885e-03	2.998e-03	2.856e-03	2.780e-03
Clock = 1 Data 100Mhz	2.295e-05	3.932e-04	2.706e-04	2.094e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P16	C8T28SOIDV_LL_-SDFPQNTX29_P16		
Clock 100Mhz Data 0Mhz	5.428e-03	5.373e-03		
Clock 100Mhz Data 25Mhz	6.154e-03	7.159e-03		
Clock 100Mhz Data 50Mhz	6.880e-03	8.945e-03		
Clock = 0 Data 100Mhz	2.734e-03	2.704e-03		
Clock = 1 Data 100Mhz	1.726e-04	1.482e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P16	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P16	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P16	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P16	C8T28SOI_LLHF_-SDFPQTX3_P16	C8T28SOIDV_LL_-SDFPQTX5_P16	C8T28SOIDV_LL_-SDFPQTX10_P16
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P16	C8T28SOIDV_LL_-SDFPQTX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQTX5_P16	**C8T28SOI_LLHF_-SDFPQTX3_P16**	**C8T28SOI_LL_-SDFPQTX5_P16**	**C8T28SOI_LLHF_-SDFPQTX3_P16**
CP to Q ↓	0.1067	0.0978	5.2653	8.0450
CP to Q ↑	0.0899	0.0984	7.8091	12.0657
CP to TQ ↓	0.1280	0.0963	14.6188	8.8774
CP to TQ ↑	0.1164	0.1049	40.2747	21.6947
	C8T28SOIDV_LL_-SDFPQTX5_P16	**C8T28SOIDV_LL_-SDFPQTX10_P16**	**C8T28SOIDV_LL_-SDFPQTX5_P16**	**C8T28SOIDV_LL_-SDFPQTX10_P16**
CP to Q ↓	0.0850	0.1131	4.7993	2.2560
CP to Q ↑	0.1023	0.1485	7.7609	3.8369
CP to TQ ↓	0.0846	0.1170	8.8069	9.0451
CP to TQ ↑	0.1060	0.1551	18.4508	18.3852
	C8T28SOIDV_LL_-SDFPQTX19_P16	**C8T28SOIDV_LL_-SDFPQTX29_P16**	**C8T28SOIDV_LL_-SDFPQTX19_P16**	**C8T28SOIDV_LL_-SDFPQTX29_P16**
CP to Q ↓	0.1232	0.1349	1.1722	0.7635
CP to Q ↑	0.1559	0.1530	1.9443	1.2813
CP to TQ ↓	0.1294	0.0813	9.1208	9.3273
CP to TQ ↑	0.1656	0.1083	18.4291	23.4046

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P16	C8T28SOI_-LLHF_-SDFPQTX3_P16	C8T28SOIDV_-LL_SDFPQTX5_-P16	C8T28SOIDV_-LL_-SDFPQTX10_-P16
CP ↓	min_pulse_width to CP	0.1541	0.1459	0.1367	0.1326
CP ↑	min_pulse_width to CP	0.0910	0.0734	0.0682	0.0576
D ↓	hold_rising to CP	-0.0783	-0.1532	-0.0246	-0.0241
D ↑	hold_rising to CP	-0.0234	-0.0208	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1269	0.2122	0.0888	0.0888

D ↑	setup_rising to CP	0.0531	0.0563	0.0368	0.0368
TE ↓	hold_rising to CP	-0.0502	-0.0550	-0.0202	-0.0192
TE ↑	hold_rising to CP	-0.0244	-0.0191	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.1279	0.1711	0.0835	0.0814
TE ↑	setup_rising to CP	0.1590	0.2078	0.1648	0.1648
TI ↓	hold_rising to CP	-0.1039	-0.1504	-0.0906	-0.0948
TI ↑	hold_rising to CP	-0.0215	-0.0202	-0.0266	-0.0266
TI ↓	setup_rising to CP	0.1573	0.1948	0.1546	0.1530
TI ↑	setup_rising to CP	0.0528	0.0502	0.0528	0.0528
		C8T28SOIDV_-LL_-SDFPQTX19_-P16	C8T28SOIDV_-LL_-SDFPQTX29_-P16		
CP ↓	min_pulse_width to CP	0.1326	0.1373		
CP ↑	min_pulse_width to CP	0.0576	0.0717		
D ↓	hold_rising to CP	-0.0241	-0.0241		
D ↑	hold_rising to CP	-0.0120	-0.0120		
D ↓	setup_rising to CP	0.0830	0.0888		
D ↑	setup_rising to CP	0.0368	0.0368		
TE ↓	hold_rising to CP	-0.0192	-0.0192		
TE ↑	hold_rising to CP	-0.0244	-0.0244		
TE ↓	setup_rising to CP	0.0814	0.0831		
TE ↑	setup_rising to CP	0.1589	0.1638		
TI ↓	hold_rising to CP	-0.0948	-0.0948		
TI ↑	hold_rising to CP	-0.0266	-0.0266		
TI ↓	setup_rising to CP	0.1537	0.1589		
TI ↑	setup_rising to CP	0.0528	0.0528		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P16	9.848e-06	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P16	9.585e-06	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P16	9.774e-06	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P16	1.296e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P16	1.600e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P16	2.054e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

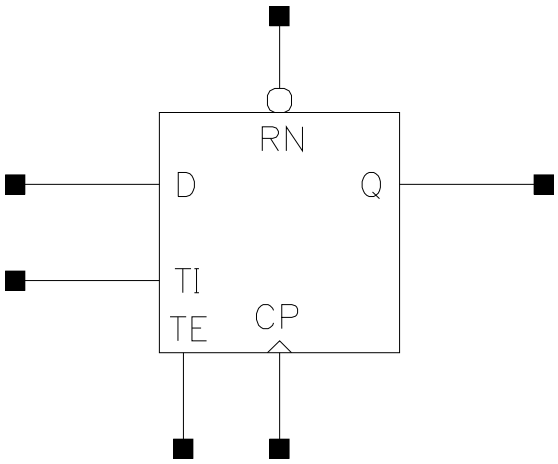
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P16	C8T28SOI_LLHF_-SDFPQTX3_P16	C8T28SOIDV_LL_-SDFPQTX5_P16	C8T28SOIDV_LL_-SDFPQTX10_P16
Clock 100Mhz Data 0Mhz	6.058e-03	5.892e-03	5.640e-03	5.509e-03
Clock 100Mhz Data 25Mhz	6.016e-03	5.828e-03	5.629e-03	5.888e-03
Clock 100Mhz Data 50Mhz	5.973e-03	5.764e-03	5.618e-03	6.268e-03
Clock = 0 Data 100Mhz	2.889e-03	3.001e-03	2.854e-03	2.777e-03
Clock = 1 Data 100Mhz	2.293e-05	3.914e-04	2.694e-04	2.085e-04
	C8T28SOIDV_LL_-SDFPQTX19_P16	C8T28SOIDV_LL_-SDFPQTX29_P16		
Clock 100Mhz Data 0Mhz	5.432e-03	5.385e-03		
Clock 100Mhz Data 25Mhz	6.305e-03	6.804e-03		
Clock 100Mhz Data 50Mhz	7.178e-03	8.223e-03		
Clock = 0 Data 100Mhz	2.730e-03	2.702e-03		
Clock = 1 Data 100Mhz	1.720e-04	1.476e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P16	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P16	C8T28SOI_LLHF_-SDFPRQX3_P16	C8T28SOIDV_LL_-SDFPRQX5_P16	C8T28SOIDV_LL_-SDFPRQX10_P16
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0007	0.0009	0.0009
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P16	C8T28SOIDV_LL_-SDFPRQX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P16	**C8T28SOI_LLHF_-SDFPRQX3_P16**	**C8T28SOI_LL_-SDFPRQX5_P16**	**C8T28SOI_LLHF_-SDFPRQX3_P16**
CP to Q ↓	0.1036	0.0934	5.0285	7.8119
CP to Q ↑	0.0863	0.0978	7.7623	11.8700
RN to Q ↓	0.0918	0.0898	4.5994	7.2788
	C8T28SOIDV_LL_-SDFPRQX5_P16	**C8T28SOIDV_LL_-SDFPRQX10_P16**	**C8T28SOIDV_LL_-SDFPRQX5_P16**	**C8T28SOIDV_LL_-SDFPRQX10_P16**
CP to Q ↓	0.0783	0.1125	4.6602	2.2721
CP to Q ↑	0.1030	0.1515	7.6776	3.8442
RN to Q ↓	0.0744	0.1163	4.6368	2.2695
	C8T28SOIDV_LL_-SDFPRQX19_P16	**C8T28SOIDV_LL_-SDFPRQX29_P16**	**C8T28SOIDV_LL_-SDFPRQX19_P16**	**C8T28SOIDV_LL_-SDFPRQX29_P16**
CP to Q ↓	0.1209	0.1227	1.1692	0.7976
CP to Q ↑	0.1587	0.1656	1.9601	1.3251
RN to Q ↓	0.1250	0.1269	1.1688	0.7960

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P16	C8T28SOI_-LLHF_-SDFPRQX3_P16	C8T28SOIDV_-LL_SDFPRQX5_-P16	C8T28SOIDV_-LL_-SDFPRQX10_-P16
CP ↓	min_pulse_width to CP	0.1575	0.1452	0.1397	0.1373
CP ↑	min_pulse_width to CP	0.0828	0.0687	0.0622	0.0576
D ↓	hold_rising to CP	-0.0783	-0.1479	-0.0246	-0.0241
D ↑	hold_rising to CP	-0.0266	-0.0266	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1327	0.2095	0.0883	0.0888
D ↑	setup_rising to CP	0.0589	0.0612	0.0417	0.0417
RN ↓	min_pulse_width to RN	0.0979	0.0952	0.0828	0.0806
RN ↑	recovery_rising to CP	0.0130	0.0085	0.0085	0.0027

RN ↑	removal_rising to CP	0.0123	0.0123	0.0118	0.0096
TE ↓	hold_rising to CP	-0.0555	-0.0571	-0.0192	-0.0192
TE ↑	hold_rising to CP	-0.0244	-0.0240	-0.0267	-0.0266
TE ↓	setup_rising to CP	0.1274	0.1711	0.0831	0.0831
TE ↑	setup_rising to CP	0.1590	0.2056	0.1589	0.1589
TI ↓	hold_rising to CP	-0.1039	-0.1456	-0.0900	-0.0906
TI ↑	hold_rising to CP	-0.0266	-0.0218	-0.0279	-0.0279
TI ↓	setup_rising to CP	0.1582	0.1948	0.1530	0.1530
TI ↑	setup_rising to CP	0.0564	0.0508	0.0612	0.0620
		C8T28SOIDV_-LL_-SDFPRQX19_-P16	C8T28SOIDV_-LL_-SDFPRQX29_-P16		
CP ↓	min_pulse_width to CP	0.1373	0.1373		
CP ↑	min_pulse_width to CP	0.0576	0.0589		
D ↓	hold_rising to CP	-0.0241	-0.0241		
D ↑	hold_rising to CP	-0.0120	-0.0120		
D ↓	setup_rising to CP	0.0888	0.0888		
D ↑	setup_rising to CP	0.0417	0.0417		
RN ↓	min_pulse_width to RN	0.0806	0.0806		
RN ↑	recovery_rising to CP	0.0027	0.0037		
RN ↑	removal_rising to CP	0.0096	0.0118		
TE ↓	hold_rising to CP	-0.0192	-0.0192		
TE ↑	hold_rising to CP	-0.0266	-0.0266		
TE ↓	setup_rising to CP	0.0841	0.0835		
TE ↑	setup_rising to CP	0.1589	0.1589		
TI ↓	hold_rising to CP	-0.0906	-0.0906		
TI ↑	hold_rising to CP	-0.0279	-0.0272		
TI ↓	setup_rising to CP	0.1537	0.1530		
TI ↑	setup_rising to CP	0.0620	0.0620		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P16	1.023e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P16	9.583e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P16	9.611e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P16	1.258e-05	1.000e-20

C8T28SOIDV_LL_SDFPRQX19_P16	1.551e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P16	1.950e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

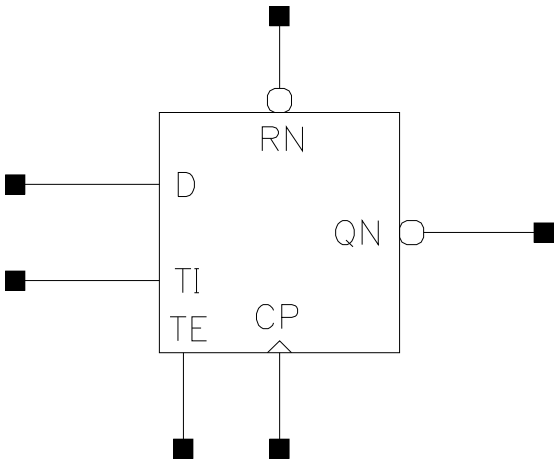
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P16	C8T28SOI_LLHF_-SDFPRQX3_P16	C8T28SOIDV_LL_-SDFPRQX5_P16	C8T28SOIDV_LL_-SDFPRQX10_P16
Clock 100Mhz Data 0Mhz	6.289e-03	6.061e-03	5.788e-03	5.652e-03
Clock 100Mhz Data 25Mhz	6.029e-03	5.843e-03	5.601e-03	5.897e-03
Clock 100Mhz Data 50Mhz	5.769e-03	5.625e-03	5.414e-03	6.142e-03
Clock = 0 Data 100Mhz	2.784e-03	2.926e-03	2.830e-03	2.784e-03
Clock = 1 Data 100Mhz	2.285e-05	3.935e-04	2.705e-04	2.090e-04
	C8T28SOIDV_LL_-SDFPRQX19_P16	C8T28SOIDV_LL_-SDFPRQX29_P16		
Clock 100Mhz Data 0Mhz	5.570e-03	5.517e-03		
Clock 100Mhz Data 25Mhz	6.271e-03	6.839e-03		
Clock 100Mhz Data 50Mhz	6.971e-03	8.161e-03		
Clock = 0 Data 100Mhz	2.755e-03	2.737e-03		
Clock = 1 Data 100Mhz	1.722e-04	1.477e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P16	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P16	C8T28SOI_LLHF_-SDFPRQNX3_P16	C8T28SOIDV_LL_-SDFPRQNX5_P16	C8T28SOIDV_LL_-SDFPRQNX10_P16
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0007	0.0009	0.0008
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P16	C8T28SOIDV_LL_-SDFPRQNX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0007	0.0007		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNX5_P16	**C8T28SOI_LLHF_-SDFPRQNX3_P16**	**C8T28SOI_LL_-SDFPRQNX5_P16**	**C8T28SOI_LLHF_-SDFPRQNX3_P16**
CP to QN ↓	0.1184	0.1268	4.8743	7.2562
CP to QN ↑	0.1091	0.1023	8.0204	11.6890
RN to QN ↑	0.1073	0.1054	8.0015	11.6594
	C8T28SOIDV_LL_-SDFPRQNX5_P16	**C8T28SOIDV_LL_-SDFPRQNX10_P16**	**C8T28SOIDV_LL_-SDFPRQNX5_P16**	**C8T28SOIDV_LL_-SDFPRQNX10_P16**
CP to QN ↓	0.1351	0.1208	4.4818	2.2739
CP to QN ↑	0.0983	0.0974	7.5935	3.8448
RN to QN ↑	0.1006	0.0941	7.5809	3.8448
	C8T28SOIDV_LL_-SDFPRQNX19_P16	**C8T28SOIDV_LL_-SDFPRQNX29_P16**	**C8T28SOIDV_LL_-SDFPRQNX19_P16**	**C8T28SOIDV_LL_-SDFPRQNX29_P16**
CP to QN ↓	0.1349	0.1441	1.1989	0.8033
CP to QN ↑	0.1081	0.1229	1.9653	1.3181
RN to QN ↑	0.1009	0.1189	1.9640	1.3178

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P16	C8T28SOI_-LLHF_-SDFPRQNX3_-P16	C8T28SOIDV_-LL_-SDFPRQNX5_-P16	C8T28SOIDV_-LL_-SDFPRQNX10_-P16
CP ↓	min_pulse_width to CP	0.1541	0.1458	0.1415	0.1397
CP ↑	min_pulse_width to CP	0.0637	0.0592	0.0589	0.0623
D ↓	hold_rising to CP	-0.0778	-0.1479	-0.0246	-0.0246
D ↑	hold_rising to CP	-0.0266	-0.0266	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1295	0.2095	0.0879	0.0879
D ↑	setup_rising to CP	0.0589	0.0612	0.0417	0.0417
RN ↓	min_pulse_width to RN	0.0979	0.0930	0.0828	0.0898
RN ↑	recovery_rising to CP	0.0134	0.0027	0.0027	0.0027

RN ↑	removal_rising to CP	0.0123	0.0064	0.0118	0.0096
TE ↓	hold_rising to CP	-0.0555	-0.0604	-0.0192	-0.0192
TE ↑	hold_rising to CP	-0.0244	-0.0240	-0.0267	-0.0267
TE ↓	setup_rising to CP	0.1274	0.1711	0.0831	0.0831
TE ↑	setup_rising to CP	0.1590	0.2056	0.1589	0.1589
TI ↓	hold_rising to CP	-0.1039	-0.1456	-0.0906	-0.0890
TI ↑	hold_rising to CP	-0.0266	-0.0218	-0.0279	-0.0279
TI ↓	setup_rising to CP	0.1566	0.1948	0.1546	0.1546
TI ↑	setup_rising to CP	0.0564	0.0508	0.0577	0.0612
		C8T28SOIDV_-LL_-SDFPRQNX19_-P16	C8T28SOIDV_-LL_-SDFPRQNX29_-P16		
CP ↓	min_pulse_width to CP	0.1414	0.1414		
CP ↑	min_pulse_width to CP	0.0669	0.0811		
D ↓	hold_rising to CP	-0.0192	-0.0192		
D ↑	hold_rising to CP	-0.0120	-0.0120		
D ↓	setup_rising to CP	0.0888	0.0888		
D ↑	setup_rising to CP	0.0417	0.0417		
RN ↓	min_pulse_width to RN	0.0898	0.1116		
RN ↑	recovery_rising to CP	0.0037	0.0004		
RN ↑	removal_rising to CP	0.0118	0.0118		
TE ↓	hold_rising to CP	-0.0175	-0.0143		
TE ↑	hold_rising to CP	-0.0267	-0.0267		
TE ↓	setup_rising to CP	0.0831	0.0835		
TE ↑	setup_rising to CP	0.1589	0.1589		
TI ↓	hold_rising to CP	-0.0900	-0.0857		
TI ↑	hold_rising to CP	-0.0279	-0.0279		
TI ↓	setup_rising to CP	0.1530	0.1537		
TI ↑	setup_rising to CP	0.0620	0.0577		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P16	1.035e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P16	9.863e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P16	9.859e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P16	1.269e-05	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P16	1.523e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P16	1.945e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

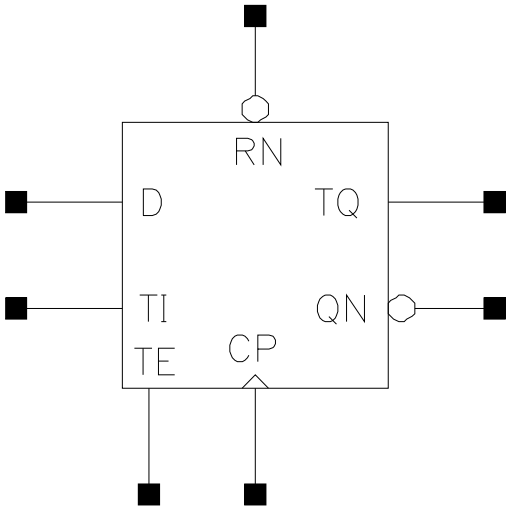
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P16	C8T28SOI_LLHF_-SDFPRQNX3_P16	C8T28SOIDV_LL_-SDFPRQNX5_P16	C8T28SOIDV_LL_-SDFPRQNX10_P16
Clock 100Mhz Data 0Mhz	6.280e-03	6.040e-03	5.776e-03	5.643e-03
Clock 100Mhz Data 25Mhz	5.987e-03	5.819e-03	5.632e-03	5.867e-03
Clock 100Mhz Data 50Mhz	5.694e-03	5.598e-03	5.488e-03	6.092e-03
Clock = 0 Data 100Mhz	2.783e-03	2.925e-03	2.833e-03	2.785e-03
Clock = 1 Data 100Mhz	2.284e-05	3.935e-04	2.705e-04	2.090e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P16	C8T28SOIDV_LL_-SDFPRQNX29_P16		
Clock 100Mhz Data 0Mhz	5.606e-03	5.601e-03		
Clock 100Mhz Data 25Mhz	6.300e-03	7.000e-03		
Clock 100Mhz Data 50Mhz	6.994e-03	8.399e-03		
Clock = 0 Data 100Mhz	2.755e-03	2.736e-03		
Clock = 1 Data 100Mhz	1.721e-04	1.476e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P16	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P16	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P16	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P16	C8T28SOI_LLHF_-SDFPRQNTX3_P16	C8T28SOIDV_LL_-SDFPRQNTX5_P16	C8T28SOIDV_LL_-SDFPRQNTX10_P16
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0007	0.0009	0.0009
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P16	C8T28SOIDV_LL_-SDFPRQNTX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0007		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNTX5_P16	**C8T28SOI_LLHF_-SDFPRQNTX3_P16**	**C8T28SOI_LL_-SDFPRQNTX5_P16**	**C8T28SOI_LLHF_-SDFPRQNTX3_P16**
CP to QN ↓	0.1310	0.1383	4.7525	7.3560
CP to QN ↑	0.1386	0.1267	8.4182	11.6766
CP to TQ ↓	0.1161	0.0900	14.1240	8.7185
CP to TQ ↑	0.1072	0.1020	39.8504	21.4985
RN to QN ↑	0.1187	0.1147	8.4254	11.7176
RN to TQ ↓	0.1012	0.0887	13.6587	8.3025
	C8T28SOIDV_LL_-SDFPRQNTX5_P16	**C8T28SOIDV_LL_-SDFPRQNTX10_P16**	**C8T28SOIDV_LL_-SDFPRQNTX5_P16**	**C8T28SOIDV_LL_-SDFPRQNTX10_P16**
CP to QN ↓	0.1427	0.1518	4.5391	2.3710
CP to QN ↑	0.1085	0.1146	7.5713	3.8372
CP to TQ ↓	0.0740	0.0753	8.5813	8.6620
CP to TQ ↑	0.1043	0.1043	16.8271	16.8370
RN to QN ↑	0.1049	0.1119	7.5669	3.8313
RN to TQ ↓	0.0678	0.0697	8.6249	8.7034
	C8T28SOIDV_LL_-SDFPRQNTX19_P16	**C8T28SOIDV_LL_-SDFPRQNTX29_P16**	**C8T28SOIDV_LL_-SDFPRQNTX19_P16**	**C8T28SOIDV_LL_-SDFPRQNTX29_P16**
CP to QN ↓	0.1418	0.1436	1.1864	0.8024
CP to QN ↑	0.1177	0.1329	1.9358	1.3085
CP to TQ ↓	0.0819	0.1007	8.7577	10.0682
CP to TQ ↑	0.1114	0.1242	16.8693	19.5025
RN to QN ↑	0.1106	0.1273	1.9344	1.3067
RN to TQ ↓	0.0726	0.0928	8.7654	9.9264

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P16	C8T28SOI_-LLHF_-SDFPRQNTX3_-P16	C8T28SOIDV_-LL_-SDFPRQNTX5_-P16	C8T28SOIDV_-LL_SDF-PRQNTX10_P16
CP ↓	min_pulse_width to CP	0.1541	0.1451	0.1414	0.1397
CP ↑	min_pulse_width to CP	0.0876	0.0769	0.0622	0.0670
D ↓	hold_rising to CP	-0.0783	-0.1483	-0.0246	-0.0246
D ↑	hold_rising to CP	-0.0266	-0.0266	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1269	0.2095	0.0888	0.0888
D ↑	setup_rising to CP	0.0589	0.0612	0.0417	0.0417
RN ↓	min_pulse_width to RN	0.1023	0.0974	0.0925	0.0974
RN ↑	recovery_rising to CP	0.0134	0.0081	0.0059	0.0059
RN ↑	removal_rising to CP	0.0064	0.0064	0.0118	0.0096
TE ↓	hold_rising to CP	-0.0555	-0.0604	-0.0192	-0.0192
TE ↑	hold_rising to CP	-0.0244	-0.0240	-0.0267	-0.0267
TE ↓	setup_rising to CP	0.1279	0.1711	0.0831	0.0831
TE ↑	setup_rising to CP	0.1590	0.2056	0.1648	0.1589
TI ↓	hold_rising to CP	-0.1039	-0.1456	-0.0890	-0.0900
TI ↑	hold_rising to CP	-0.0266	-0.0211	-0.0279	-0.0279
TI ↓	setup_rising to CP	0.1573	0.1948	0.1546	0.1530
TI ↑	setup_rising to CP	0.0564	0.0551	0.0577	0.0612
		C8T28SOIDV_-LL_SDF-PRQNTX19_P16	C8T28SOIDV_-LL_SDF-PRQNTX29_P16		
CP ↓	min_pulse_width to CP	0.1414	0.1414		
CP ↑	min_pulse_width to CP	0.0717	0.0858		
D ↓	hold_rising to CP	-0.0192	-0.0192		
D ↑	hold_rising to CP	-0.0120	-0.0120		
D ↓	setup_rising to CP	0.0888	0.0883		
D ↑	setup_rising to CP	0.0417	0.0417		
RN ↓	min_pulse_width to RN	0.0996	0.1191		
RN ↑	recovery_rising to CP	0.0027	0.0027		
RN ↑	removal_rising to CP	0.0118	0.0118		
TE ↓	hold_rising to CP	-0.0143	-0.0175		
TE ↑	hold_rising to CP	-0.0267	-0.0267		

TE ↓	setup_rising to CP	0.0831	0.0831		
TE ↑	setup_rising to CP	0.1589	0.1589		
TI ↓	hold_rising to CP	-0.0900	-0.0900		
TI ↑	hold_rising to CP	-0.0279	-0.0279		
TI ↓	setup_rising to CP	0.1530	0.1546		
TI ↑	setup_rising to CP	0.0620	0.0620		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P16	1.043e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P16	1.033e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P16	1.045e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_P16	1.185e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_P16	1.534e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_P16	1.994e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

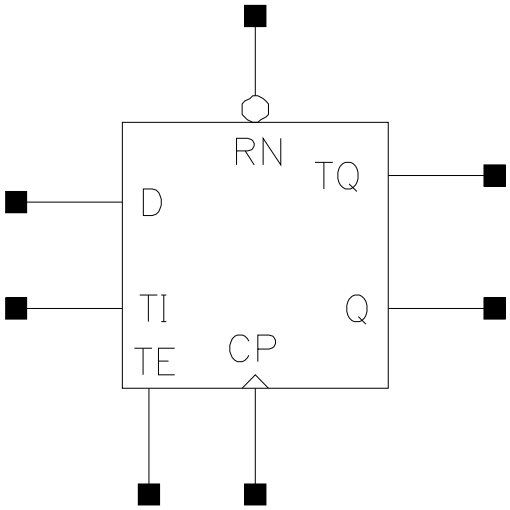
Pin Cycle	C8T28SOI_LL_SDFPRQNTX5_P16	C8T28SOI_LLHF_SDFPRQNTX3_P16	C8T28SOIDV_LL_SDFPRQNTX5_P16	C8T28SOIDV_LL_SDFPRQNTX10_P16
Clock 100Mhz Data 0Mhz	6.290e-03	6.047e-03	5.791e-03	5.654e-03
Clock 100Mhz Data 25Mhz	6.208e-03	5.994e-03	5.783e-03	5.884e-03
Clock 100Mhz Data 50Mhz	6.125e-03	5.941e-03	5.776e-03	6.113e-03
Clock = 0 Data 100Mhz	2.773e-03	2.923e-03	2.834e-03	2.786e-03
Clock = 1 Data 100Mhz	2.285e-05	3.956e-04	2.719e-04	2.101e-04
	C8T28SOIDV_LL_SDFPRQNTX19_P16	C8T28SOIDV_LL_SDFPRQNTX29_P16		
Clock 100Mhz Data 0Mhz	5.618e-03	5.586e-03		
Clock 100Mhz Data 25Mhz	6.312e-03	7.095e-03		
Clock 100Mhz Data 50Mhz	7.006e-03	8.605e-03		
Clock = 0 Data 100Mhz	2.757e-03	2.738e-03		
Clock = 1 Data 100Mhz	1.730e-04	1.484e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P16	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P16	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P16	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P16	C8T28SOI_LLHF_-SDFPRQTX3_P16	C8T28SOIDV_LL_-SDFPRQTX5_P16	C8T28SOIDV_LL_-SDFPRQTX10_P16
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0007	0.0009	0.0008
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P16	C8T28SOIDV_LL_-SDFPRQTX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQTX5_P16	**C8T28SOI_LLHF_-SDFPRQTX3_P16**	**C8T28SOI_LL_-SDFPRQTX5_P16**	**C8T28SOI_LLHF_-SDFPRQTX3_P16**
CP to Q ↓	0.1219	0.1046	5.3675	8.0853
CP to Q ↑	0.0930	0.1021	7.8199	12.0714
CP to TQ ↓	0.1440	0.1026	14.7516	8.9285
CP to TQ ↑	0.1196	0.1083	39.9203	21.7013
RN to Q ↓	0.0974	0.0945	4.8305	7.4725
RN to TQ ↓	0.1120	0.0942	14.1460	8.4335
	C8T28SOIDV_LL_-SDFPRQTX5_P16	**C8T28SOIDV_LL_-SDFPRQTX10_P16**	**C8T28SOIDV_LL_-SDFPRQTX5_P16**	**C8T28SOIDV_LL_-SDFPRQTX10_P16**
CP to Q ↓	0.0854	0.1147	4.7971	2.3022
CP to Q ↑	0.1065	0.1526	7.7311	3.8420
CP to TQ ↓	0.0867	0.1192	8.7803	8.5363
CP to TQ ↑	0.1110	0.1591	16.9970	16.8771
RN to Q ↓	0.0826	0.1197	4.7546	2.2992
RN to TQ ↓	0.0838	0.1243	8.7352	8.5358
	C8T28SOIDV_LL_-SDFPRQTX19_P16	**C8T28SOIDV_LL_-SDFPRQTX29_P16**	**C8T28SOIDV_LL_-SDFPRQTX19_P16**	**C8T28SOIDV_LL_-SDFPRQTX29_P16**
CP to Q ↓	0.1290	0.1236	1.2127	0.8093
CP to Q ↑	0.1627	0.1656	1.9472	1.3168
CP to TQ ↓	0.1357	0.1278	8.6315	8.5333
CP to TQ ↑	0.1722	0.1741	16.8750	17.5260
RN to Q ↓	0.1323	0.1278	1.2126	0.8079
RN to TQ ↓	0.1391	0.1321	8.6317	8.5328

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_-P16	C8T28SOI_-LLHF_-SDFPRQTX3_-P16	C8T28SOIDV_-LL_-SDFPRQTX5_-P16	C8T28SOIDV_-LL_-SDFPRQTX10_-P16
CP ↓	min_pulse_width to CP	0.1541	0.1452	0.1397	0.1373
CP ↑	min_pulse_width to CP	0.1017	0.0816	0.0669	0.0576
D ↓	hold_rising to CP	-0.0755	-0.1483	-0.0246	-0.0241
D ↑	hold_rising to CP	-0.0266	-0.0266	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1269	0.2095	0.0883	0.0888
D ↑	setup_rising to CP	0.0589	0.0612	0.0417	0.0417
RN ↓	min_pulse_width to RN	0.1045	0.0974	0.0925	0.0806
RN ↑	recovery_rising to CP	0.0125	0.0076	0.0085	0.0037
RN ↑	removal_rising to CP	0.0064	0.0070	0.0118	0.0118
TE ↓	hold_rising to CP	-0.0555	-0.0604	-0.0197	-0.0192
TE ↑	hold_rising to CP	-0.0244	-0.0240	-0.0267	-0.0266
TE ↓	setup_rising to CP	0.1253	0.1711	0.0831	0.0835
TE ↑	setup_rising to CP	0.1590	0.2056	0.1589	0.1589
TI ↓	hold_rising to CP	-0.1026	-0.1456	-0.0900	-0.0906
TI ↑	hold_rising to CP	-0.0266	-0.0211	-0.0279	-0.0279
TI ↓	setup_rising to CP	0.1573	0.1948	0.1546	0.1530
TI ↑	setup_rising to CP	0.0564	0.0551	0.0612	0.0620
		C8T28SOIDV_-LL_-SDFPRQTX19_-P16	C8T28SOIDV_-LL_-SDFPRQTX29_-P16		
CP ↓	min_pulse_width to CP	0.1373	0.1373		
CP ↑	min_pulse_width to CP	0.0589	0.0589		
D ↓	hold_rising to CP	-0.0241	-0.0241		
D ↑	hold_rising to CP	-0.0120	-0.0120		
D ↓	setup_rising to CP	0.0856	0.0888		
D ↑	setup_rising to CP	0.0417	0.0417		
RN ↓	min_pulse_width to RN	0.0806	0.0806		
RN ↑	recovery_rising to CP	0.0037	0.0037		
RN ↑	removal_rising to CP	0.0118	0.0118		
TE ↓	hold_rising to CP	-0.0192	-0.0192		
TE ↑	hold_rising to CP	-0.0266	-0.0266		

TE ↓	setup_rising to CP	0.0841	0.0835		
TE ↑	setup_rising to CP	0.1594	0.1589		
TI ↓	hold_rising to CP	-0.0906	-0.0906		
TI ↑	hold_rising to CP	-0.0279	-0.0315		
TI ↓	setup_rising to CP	0.1540	0.1537		
TI ↑	setup_rising to CP	0.0620	0.0620		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P16	1.036e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P16	1.010e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P16	1.021e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P16	1.329e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P16	1.596e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P16	2.018e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

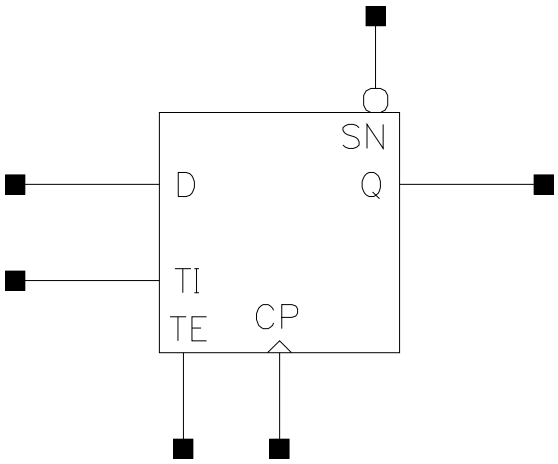
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P16	C8T28SOI_LLHF_-SDFPRQTX3_P16	C8T28SOIDV_LL_-SDFPRQTX5_P16	C8T28SOIDV_LL_-SDFPRQTX10_P16
Clock 100Mhz Data 0Mhz	6.294e-03	6.053e-03	5.784e-03	5.650e-03
Clock 100Mhz Data 25Mhz	6.239e-03	5.978e-03	5.733e-03	6.059e-03
Clock 100Mhz Data 50Mhz	6.184e-03	5.902e-03	5.682e-03	6.468e-03
Clock = 0 Data 100Mhz	2.776e-03	2.924e-03	2.830e-03	2.784e-03
Clock = 1 Data 100Mhz	2.285e-05	3.962e-04	2.723e-04	2.104e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P16	C8T28SOIDV_LL_-SDFPRQTX29_P16		
Clock 100Mhz Data 0Mhz	5.569e-03	5.516e-03		
Clock 100Mhz Data 25Mhz	6.443e-03	6.920e-03		
Clock 100Mhz Data 50Mhz	7.316e-03	8.325e-03		
Clock = 0 Data 100Mhz	2.756e-03	2.738e-03		
Clock = 1 Data 100Mhz	1.733e-04	1.486e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P16	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P16	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P16	C8T28SOI_LLHF_-SDFPSQX3_P16	C8T28SOIDV_LL_-SDFPSQX5_P16	C8T28SOIDV_LL_-SDFPSQX10_P16
CP	0.0007	0.0007	0.0005	0.0006
D	0.0003	0.0004	0.0003	0.0004
SN	0.0013	0.0012	0.0010	0.0010
TE	0.0010	0.0010	0.0009	0.0010
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQX14_P16	C8T28SOIDV_LL_-SDFPSQX19_P16	C8T28SOIDV_LL_-SDFPSQX29_P16	
CP	0.0006	0.0006	0.0006	
D	0.0004	0.0004	0.0004	
SN	0.0010	0.0010	0.0010	
TE	0.0010	0.0010	0.0010	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P16	**C8T28SOI_LLHF_-SDFPSQX3_P16**	**C8T28SOI_LL_-SDFPSQX5_P16**	**C8T28SOI_LLHF_-SDFPSQX3_P16**
CP to Q ↓	0.1076	0.0948	5.1766	7.9576
CP to Q ↑	0.0890	0.1003	7.8112	11.8990
SN to Q ↑	0.0731	0.0661	7.7309	11.7676
	C8T28SOIDV_LL_-SDFPSQX5_P16	**C8T28SOIDV_LL_-SDFPSQX10_P16**	**C8T28SOIDV_LL_-SDFPSQX5_P16**	**C8T28SOIDV_LL_-SDFPSQX10_P16**
CP to Q ↓	0.0773	0.1146	4.6598	2.2313
CP to Q ↑	0.0981	0.1629	7.6667	3.8314
SN to Q ↑	0.0659	0.1273	7.6531	3.8295
	C8T28SOIDV_LL_-SDFPSQX14_P16	**C8T28SOIDV_LL_-SDFPSQX19_P16**	**C8T28SOIDV_LL_-SDFPSQX14_P16**	**C8T28SOIDV_LL_-SDFPSQX19_P16**
CP to Q ↓	0.1156	0.1233	1.5075	1.1565
CP to Q ↑	0.1629	0.1687	2.5648	1.9314
SN to Q ↑	0.1267	0.1325	2.5644	1.9328
	C8T28SOIDV_LL_-SDFPSQX29_P16		**C8T28SOIDV_LL_-SDFPSQX29_P16**	
CP to Q ↓	0.1227		0.7841	
CP to Q ↑	0.1789		1.2849	
SN to Q ↑	0.1429		1.2841	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P16	C8T28SOI_-LLHF_-SDFPSQX3_P16	C8T28SOIDV_-LL_SDFPSQX5_-P16	C8T28SOIDV_-LL_-SDFPSQX10_-P16
CP ↓	min_pulse_width to CP	0.1669	0.1688	0.1462	0.1456
CP ↑	min_pulse_width to CP	0.0924	0.0735	0.0622	0.0589
D ↓	hold_rising to CP	-0.0832	-0.1603	-0.0344	-0.0442
D ↑	hold_rising to CP	-0.0213	-0.0218	-0.0116	-0.0116
D ↓	setup_rising to CP	0.1425	0.2317	0.1025	0.1083
D ↑	setup_rising to CP	0.0536	0.0558	0.0417	0.0417

SN ↓	min_pulse_width to SN	0.0691	0.0571	0.0571	0.0620
SN ↑	recovery_rising to CP	0.0160	0.0150	0.0037	0.0009
SN ↑	removal_rising to CP	0.0353	0.0483	0.0553	0.0553
TE ↓	hold_rising to CP	-0.0506	-0.0550	-0.0290	-0.0355
TE ↑	hold_rising to CP	-0.0218	-0.0191	-0.0120	-0.0191
TE ↓	setup_rising to CP	0.1367	0.1911	0.1009	0.1030
TE ↑	setup_rising to CP	0.1746	0.2277	0.1648	0.1546
TI ↓	hold_rising to CP	-0.1130	-0.1553	-0.0844	-0.0844
TI ↑	hold_rising to CP	-0.0218	-0.0162	-0.0105	-0.0217
TI ↓	setup_rising to CP	0.1679	0.2143	0.1573	0.1433
TI ↑	setup_rising to CP	0.0512	0.0502	0.0404	0.0515
		C8T28SOIDV_-LL_-SDFPSQX14_-P16	C8T28SOIDV_-LL_-SDFPSQX19_-P16	C8T28SOIDV_-LL_-SDFPSQX29_-P16	
CP ↓	min_pulse_width to CP	0.1439	0.1421	0.1421	
CP ↑	min_pulse_width to CP	0.0589	0.0589	0.0590	
D ↓	hold_rising to CP	-0.0442	-0.0436	-0.0436	
D ↑	hold_rising to CP	-0.0116	-0.0116	-0.0116	
D ↓	setup_rising to CP	0.1083	0.1051	0.1083	
D ↑	setup_rising to CP	0.0417	0.0417	0.0417	
SN ↓	min_pulse_width to SN	0.0620	0.0620	0.0647	
SN ↑	recovery_rising to CP	0.0009	-0.0012	-0.0012	
SN ↑	removal_rising to CP	0.0553	0.0553	0.0553	
TE ↓	hold_rising to CP	-0.0355	-0.0355	-0.0355	
TE ↑	hold_rising to CP	-0.0191	-0.0191	-0.0191	
TE ↓	setup_rising to CP	0.1030	0.1036	0.1036	
TE ↑	setup_rising to CP	0.1550	0.1550	0.1550	
TI ↓	hold_rising to CP	-0.0844	-0.0844	-0.0844	
TI ↑	hold_rising to CP	-0.0217	-0.0217	-0.0217	
TI ↓	setup_rising to CP	0.1433	0.1433	0.1433	
TI ↑	setup_rising to CP	0.0515	0.0515	0.0515	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds

C8T28SOI_LL_SDFPSQX5_P16	1.049e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQX3_P16	9.911e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P16	9.994e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P16	1.329e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P16	1.484e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P16	1.673e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P16	2.035e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

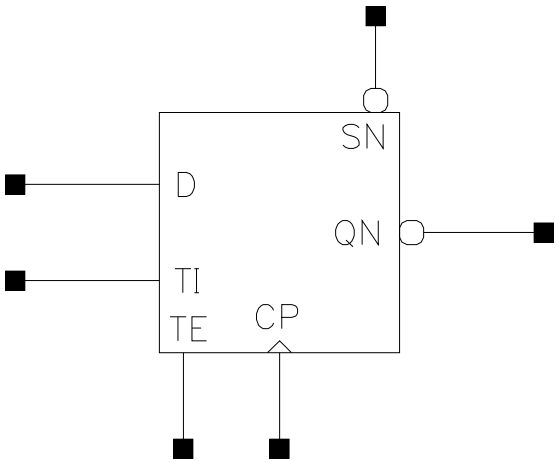
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P16	C8T28SOI_LLHF_-SDFPSQX3_P16	C8T28SOIDV_LL_-SDFPSQX5_P16	C8T28SOIDV_LL_-SDFPSQX10_P16
Clock 100Mhz Data 0Mhz	6.196e-03	5.893e-03	5.655e-03	5.534e-03
Clock 100Mhz Data 25Mhz	6.060e-03	5.751e-03	5.480e-03	5.866e-03
Clock 100Mhz Data 50Mhz	5.924e-03	5.609e-03	5.304e-03	6.198e-03
Clock = 0 Data 100Mhz	2.862e-03	3.001e-03	2.931e-03	2.915e-03
Clock = 1 Data 100Mhz	2.287e-05	3.914e-04	2.692e-04	2.083e-04
	C8T28SOIDV_LL_-SDFPSQX14_P16	C8T28SOIDV_LL_-SDFPSQX19_P16	C8T28SOIDV_LL_-SDFPSQX29_P16	
Clock 100Mhz Data 0Mhz	5.462e-03	5.413e-03	5.378e-03	
Clock 100Mhz Data 25Mhz	5.993e-03	6.285e-03	6.695e-03	
Clock 100Mhz Data 50Mhz	6.524e-03	7.156e-03	8.012e-03	
Clock = 0 Data 100Mhz	2.905e-03	2.898e-03	2.893e-03	
Clock = 1 Data 100Mhz	1.718e-04	1.475e-04	1.301e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P16	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P16	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P16	C8T28SOI_LLHF_-SDFPSQNX3_P16	C8T28SOIDV_LL_-SDFPSQNX5_P16	C8T28SOIDV_LL_-SDFPSQNX10_P16
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0013	0.0012	0.0010	0.0011
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNX14_P16	C8T28SOIDV_LL_-SDFPSQNX19_P16	C8T28SOIDV_LL_-SDFPSQNX23_P16	C8T28SOIDV_LL_-SDFPSQNX29_P16
CP	0.0005	0.0005	0.0005	0.0005
D	0.0003	0.0003	0.0003	0.0003
SN	0.0010	0.0011	0.0011	0.0010
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNX5_P16	**C8T28SOI_LLHF_-SDFPSQNX3_P16**	**C8T28SOI_LL_-SDFPSQNX5_P16**	**C8T28SOI_LLHF_-SDFPSQNX3_P16**
CP to QN ↓	0.1249	0.1268	4.9799	7.2268
CP to QN ↑	0.1164	0.1072	8.0944	11.6915
SN to QN ↓	0.1108	0.0937	4.9797	7.2187
	C8T28SOIDV_LL_-SDFPSQNX5_P16	**C8T28SOIDV_LL_-SDFPSQNX10_P16**	**C8T28SOIDV_LL_-SDFPSQNX5_P16**	**C8T28SOIDV_LL_-SDFPSQNX10_P16**
CP to QN ↓	0.1345	0.1246	4.4663	2.2081
CP to QN ↑	0.1032	0.1063	7.5934	3.8081
SN to QN ↓	0.1010	0.0885	4.4656	2.2075
	C8T28SOIDV_LL_-SDFPSQNX14_P16	**C8T28SOIDV_LL_-SDFPSQNX19_P16**	**C8T28SOIDV_LL_-SDFPSQNX14_P16**	**C8T28SOIDV_LL_-SDFPSQNX19_P16**
CP to QN ↓	0.1295	0.1335	1.5106	1.1531
CP to QN ↑	0.1094	0.1130	2.5543	1.9212
SN to QN ↓	0.0913	0.0963	1.5120	1.1529
	C8T28SOIDV_LL_-SDFPSQNX23_P16	**C8T28SOIDV_LL_-SDFPSQNX29_P16**	**C8T28SOIDV_LL_-SDFPSQNX23_P16**	**C8T28SOIDV_LL_-SDFPSQNX29_P16**
CP to QN ↓	0.1354	0.1296	0.8955	0.7747
CP to QN ↑	0.1129	0.1153	1.9109	1.2817
SN to QN ↓	0.0992	0.0981	0.8944	0.7762

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P16	C8T28SOI_-LLHF_-SDFPSQNX3_-P16	C8T28SOIDV_-LL_-SDFPSQNX5_-P16	C8T28SOIDV_-LL_-SDFPSQNX10_-P16
CP ↓	min_pulse_width to CP	0.1652	0.1647	0.1462	0.1509
CP ↑	min_pulse_width to CP	0.0685	0.0592	0.0623	0.0669
D ↓	hold_rising to CP	-0.0827	-0.1603	-0.0338	-0.0312
D ↑	hold_rising to CP	-0.0240	-0.0218	-0.0116	-0.0116
D ↓	setup_rising to CP	0.1425	0.2323	0.1025	0.1025

D ↑	setup_rising to CP	0.0536	0.0563	0.0417	0.0417
SN ↓	min_pulse_width to SN	0.0669	0.0571	0.0598	0.0620
SN ↑	recovery_rising to CP	0.0102	0.0160	0.0005	0.0037
SN ↑	removal_rising to CP	0.0353	0.0483	0.0553	0.0547
TE ↓	hold_rising to CP	-0.0506	-0.0550	-0.0290	-0.0300
TE ↑	hold_rising to CP	-0.0218	-0.0191	-0.0115	-0.0120
TE ↓	setup_rising to CP	0.1371	0.1879	0.1009	0.1009
TE ↑	setup_rising to CP	0.1719	0.2277	0.1648	0.1616
TI ↓	hold_rising to CP	-0.1136	-0.1551	-0.0900	-0.0844
TI ↑	hold_rising to CP	-0.0218	-0.0202	-0.0105	-0.0105
TI ↓	setup_rising to CP	0.1679	0.2143	0.1573	0.1575
TI ↑	setup_rising to CP	0.0515	0.0502	0.0404	0.0404
		C8T28SOIDV_-LL_-SDFPSQNX14_-P16	C8T28SOIDV_-LL_-SDFPSQNX19_-P16	C8T28SOIDV_-LL_-SDFPSQNX23_-P16	C8T28SOIDV_-LL_-SDFPSQNX29_-P16
CP ↓	min_pulse_width to CP	0.1509	0.1509	0.1492	0.1462
CP ↑	min_pulse_width to CP	0.0669	0.0717	0.0717	0.0729
D ↓	hold_rising to CP	-0.0312	-0.0312	-0.0312	-0.0344
D ↑	hold_rising to CP	-0.0116	-0.0116	-0.0116	-0.0116
D ↓	setup_rising to CP	0.1029	0.1035	0.1035	0.1029
D ↑	setup_rising to CP	0.0417	0.0417	0.0417	0.0417
SN ↓	min_pulse_width to SN	0.0620	0.0620	0.0647	0.0669
SN ↑	recovery_rising to CP	0.0037	0.0037	0.0037	0.0037
SN ↑	removal_rising to CP	0.0547	0.0547	0.0547	0.0553
TE ↓	hold_rising to CP	-0.0290	-0.0290	-0.0290	-0.0290
TE ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.1009	0.1009	0.1009	0.1009
TE ↑	setup_rising to CP	0.1616	0.1616	0.1616	0.1648
TI ↓	hold_rising to CP	-0.0886	-0.0886	-0.0886	-0.0884
TI ↑	hold_rising to CP	-0.0105	-0.0105	-0.0105	-0.0105
TI ↓	setup_rising to CP	0.1575	0.1532	0.1532	0.1575
TI ↑	setup_rising to CP	0.0404	0.0404	0.0404	0.0404

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P16	1.020e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P16	9.693e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P16	9.905e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P16	1.332e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P16	1.445e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P16	1.624e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P16	1.724e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P16	2.018e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

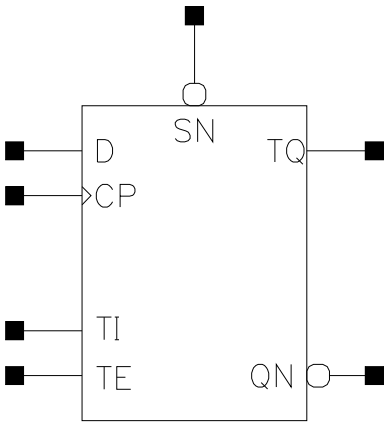
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P16	C8T28SOI_LLHF_-SDFPSQNX3_P16	C8T28SOIDV_LL_-SDFPSQNX5_P16	C8T28SOIDV_LL_-SDFPSQNX10_P16
Clock 100Mhz Data 0Mhz	6.183e-03	5.885e-03	5.648e-03	5.586e-03
Clock 100Mhz Data 25Mhz	5.995e-03	5.725e-03	5.575e-03	5.941e-03
Clock 100Mhz Data 50Mhz	5.806e-03	5.564e-03	5.501e-03	6.296e-03
Clock = 0 Data 100Mhz	2.863e-03	3.003e-03	2.933e-03	2.896e-03
Clock = 1 Data 100Mhz	2.283e-05	3.923e-04	2.698e-04	2.086e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P16	C8T28SOIDV_LL_-SDFPSQNX19_P16	C8T28SOIDV_LL_-SDFPSQNX23_P16	C8T28SOIDV_LL_-SDFPSQNX29_P16
Clock 100Mhz Data 0Mhz	5.548e-03	5.524e-03	5.507e-03	5.469e-03
Clock 100Mhz Data 25Mhz	6.090e-03	6.269e-03	6.348e-03	6.756e-03
Clock 100Mhz Data 50Mhz	6.631e-03	7.014e-03	7.189e-03	8.042e-03
Clock = 0 Data 100Mhz	2.873e-03	2.859e-03	2.848e-03	2.842e-03
Clock = 1 Data 100Mhz	1.719e-04	1.474e-04	1.299e-04	1.168e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P16	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P16	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P16	C8T28SOI_LLHF_-SDFPSQNTX3_P16	C8T28SOIDV_LL_-SDFPSQNTX5_P16	C8T28SOIDV_LL_-SDFPSQNTX10_P16
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0013	0.0012	0.0010	0.0010
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNTX19_P16	C8T28SOIDV_LL_-SDFPSQNTX23_P16	C8T28SOIDV_LL_-SDFPSQNTX29_P16	
CP	0.0005	0.0005	0.0005	
D	0.0003	0.0003	0.0003	
SN	0.0010	0.0010	0.0010	
TE	0.0009	0.0009	0.0009	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P16	**C8T28SOI_LLHF_-SDFPSQNTX3_P16**	**C8T28SOI_LL_-SDFPSQNTX5_P16**	**C8T28SOI_LLHF_-SDFPSQNTX3_P16**
CP to QN ↓	0.1367	0.1365	5.0547	7.3145
CP to QN ↑	0.1379	0.1287	8.0305	11.6997
CP to TQ ↓	0.1132	0.0911	13.9411	8.7965
CP to TQ ↑	0.1106	0.1044	39.8805	21.5114
SN to QN ↓	0.1178	0.1002	5.0475	7.3099
SN to TQ ↑	0.0930	0.0696	39.7962	21.4302
	C8T28SOIDV_LL_-SDFPSQNTX5_P16	**C8T28SOIDV_LL_-SDFPSQNTX10_P16**	**C8T28SOIDV_LL_-SDFPSQNTX5_P16**	**C8T28SOIDV_LL_-SDFPSQNTX10_P16**
CP to QN ↓	0.1349	0.1248	4.5246	2.1936
CP to QN ↑	0.1074	0.1146	7.5864	3.8108
CP to TQ ↓	0.0748	0.0877	8.6663	8.8182
CP to TQ ↑	0.1003	0.1058	18.3049	18.4089
SN to QN ↓	0.1000	0.0920	4.5323	2.1954
SN to TQ ↑	0.0654	0.0730	18.2890	18.3280
	C8T28SOIDV_LL_-SDFPSQNTX19_P16	**C8T28SOIDV_LL_-SDFPSQNTX23_P16**	**C8T28SOIDV_LL_-SDFPSQNTX19_P16**	**C8T28SOIDV_LL_-SDFPSQNTX23_P16**
CP to QN ↓	0.1327	0.1364	1.1422	0.8908
CP to QN ↑	0.1215	0.1207	1.9231	1.9087
CP to TQ ↓	0.0874	0.0888	8.7920	8.8664
CP to TQ ↑	0.1058	0.1071	18.4036	18.4257
SN to QN ↓	0.0997	0.1033	1.1438	0.8915
SN to TQ ↑	0.0729	0.0742	18.3284	18.3486
	C8T28SOIDV_LL_-SDFPSQNTX29_P16		**C8T28SOIDV_LL_-SDFPSQNTX29_P16**	
CP to QN ↓	0.1349		0.7768	
CP to QN ↑	0.1247		1.2807	

CP to TQ ↓	0.0933		9.0727	
CP to TQ ↑	0.1143		21.3957	
SN to QN ↓	0.1021		0.7773	
SN to TQ ↑	0.0815		21.3034	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P16	C8T28SOI_-LLHF_-SDFPSQNTX3_-P16	C8T28SOIDV_-LL_-SDFPSQNTX5_-P16	C8T28SOIDV_-LL_SDFP-SQNTX10_P16
CP ↓	min_pulse_width to CP	0.1682	0.1671	0.1462	0.1486
CP ↑	min_pulse_width to CP	0.0876	0.0782	0.0623	0.0716
D ↓	hold_rising to CP	-0.0849	-0.1603	-0.0344	-0.0344
D ↑	hold_rising to CP	-0.0213	-0.0218	-0.0116	-0.0116
D ↓	setup_rising to CP	0.1415	0.2317	0.1025	0.1025
D ↑	setup_rising to CP	0.0536	0.0563	0.0417	0.0417
SN ↓	min_pulse_width to SN	0.0718	0.0620	0.0620	0.0620
SN ↑	recovery_rising to CP	0.0160	0.0151	0.0005	0.0063
SN ↑	removal_rising to CP	0.0332	0.0483	0.0553	0.0553
TE ↓	hold_rising to CP	-0.0506	-0.0550	-0.0290	-0.0290
TE ↑	hold_rising to CP	-0.0218	-0.0191	-0.0115	-0.0120
TE ↓	setup_rising to CP	0.1399	0.1879	0.1009	0.1009
TE ↑	setup_rising to CP	0.1736	0.2277	0.1648	0.1648
TI ↓	hold_rising to CP	-0.1121	-0.1551	-0.0844	-0.0844
TI ↑	hold_rising to CP	-0.0218	-0.0162	-0.0105	-0.0105
TI ↓	setup_rising to CP	0.1712	0.2143	0.1573	0.1573
TI ↑	setup_rising to CP	0.0528	0.0502	0.0404	0.0404
		C8T28SOIDV_-LL_SDFP-SQNTX19_P16	C8T28SOIDV_-LL_SDFP-SQNTX23_P16	C8T28SOIDV_-LL_SDFP-SQNTX29_P16	
CP ↓	min_pulse_width to CP	0.1469	0.1486	0.1462	
CP ↑	min_pulse_width to CP	0.0764	0.0764	0.0811	
D ↓	hold_rising to CP	-0.0344	-0.0344	-0.0344	
D ↑	hold_rising to CP	-0.0116	-0.0116	-0.0116	
D ↓	setup_rising to CP	0.1025	0.1025	0.1025	
D ↑	setup_rising to CP	0.0417	0.0417	0.0417	
SN ↓	min_pulse_width to SN	0.0647	0.0647	0.0696	

SN ↑	recovery_rising to CP	0.0063	0.0063	0.0063	
SN ↑	removal_rising to CP	0.0553	0.0553	0.0553	
TE ↓	hold_rising to CP	-0.0290	-0.0290	-0.0290	
TE ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120	
TE ↓	setup_rising to CP	0.1009	0.1009	0.1009	
TE ↑	setup_rising to CP	0.1648	0.1648	0.1648	
TI ↓	hold_rising to CP	-0.0844	-0.0844	-0.0844	
TI ↑	hold_rising to CP	-0.0105	-0.0105	-0.0105	
TI ↓	setup_rising to CP	0.1573	0.1573	0.1573	
TI ↑	setup_rising to CP	0.0404	0.0404	0.0404	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P16	1.028e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P16	1.049e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P16	1.079e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_-P16	1.414e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_-P16	1.716e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_-P16	1.827e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_-P16	2.092e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P16	C8T28SOI_LLHF_-SDFPSQNTX3_P16	C8T28SOIDV_LL_-SDFPSQNTX5_P16	C8T28SOIDV_LL_-SDFPSQNTX10_P16
Clock 100Mhz Data 0Mhz	5.985e-03	5.785e-03	5.585e-03	5.485e-03
Clock 100Mhz Data 25Mhz	6.035e-03	5.826e-03	5.607e-03	5.976e-03
Clock 100Mhz Data 50Mhz	6.086e-03	5.867e-03	5.629e-03	6.468e-03
Clock = 0 Data 100Mhz	2.858e-03	2.999e-03	2.930e-03	2.896e-03
Clock = 1 Data 100Mhz	2.293e-05	3.909e-04	2.689e-04	2.079e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P16	C8T28SOIDV_LL_-SDFPSQNTX23_P16	C8T28SOIDV_LL_-SDFPSQNTX29_P16	
Clock 100Mhz Data 0Mhz	5.425e-03	5.386e-03	5.358e-03	
Clock 100Mhz Data 25Mhz	6.291e-03	6.386e-03	6.813e-03	
Clock 100Mhz Data 50Mhz	7.156e-03	7.387e-03	8.269e-03	

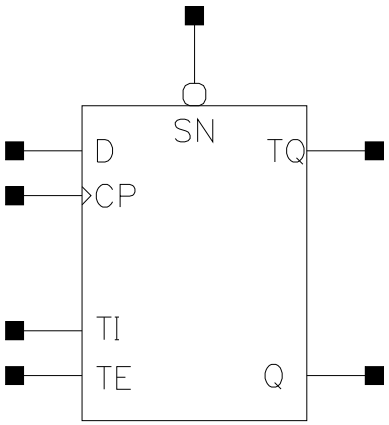
Clock = 0 Data 100Mhz	2.875e-03	2.862e-03	2.853e-03	
Clock = 1 Data 100Mhz	1.714e-04	1.470e-04	1.296e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P16	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P16	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P16	C8T28SOI_LLHF_-SDFPSQTX3_P16	C8T28SOIDV_LL_-SDFPSQTX5_P16	C8T28SOIDV_LL_-SDFPSQTX10_P16
CP	0.0007	0.0007	0.0005	0.0006
D	0.0003	0.0004	0.0003	0.0004
SN	0.0012	0.0013	0.0010	0.0010
TE	0.0010	0.0010	0.0009	0.0010
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQTX19_P16	C8T28SOIDV_LL_-SDFPSQTX29_P16		
CP	0.0006	0.0006		
D	0.0004	0.0004		
SN	0.0010	0.0010		
TE	0.0010	0.0010		
TI	0.0004	0.0004		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQTX5_P16	C8T28SOI_LLHF_-SDFPSQTX3_P16	C8T28SOI_LL_-SDFPSQTX5_P16	C8T28SOI_LLHF_-SDFPSQTX3_P16
CP to Q ↓	0.1172	0.1057	5.4201	8.1982
CP to Q ↑	0.0943	0.1044	7.8261	12.0920
CP to TQ ↓	0.1396	0.1034	14.6512	9.0133
CP to TQ ↑	0.1217	0.1105	39.8924	21.7241
SN to Q ↑	0.0766	0.0690	7.7131	11.9534
SN to TQ ↑	0.1006	0.0742	39.7858	21.6116
	C8T28SOIDV_LL_-SDFPSQTX5_P16	C8T28SOIDV_LL_-SDFPSQTX10_P16	C8T28SOIDV_LL_-SDFPSQTX5_P16	C8T28SOIDV_LL_-SDFPSQTX10_P16
CP to Q ↓	0.0871	0.1133	4.7945	2.2906
CP to Q ↑	0.1021	0.1612	7.7429	3.8502
CP to TQ ↓	0.0885	0.1170	8.7888	8.9780
CP to TQ ↑	0.1063	0.1681	18.4510	18.3542
SN to Q ↑	0.0692	0.1250	7.7176	3.8488
SN to TQ ↑	0.0735	0.1319	18.3792	18.3490
	C8T28SOIDV_LL_-SDFPSQTX19_P16	C8T28SOIDV_LL_-SDFPSQTX29_P16	C8T28SOIDV_LL_-SDFPSQTX19_P16	C8T28SOIDV_LL_-SDFPSQTX29_P16
CP to Q ↓	0.1232	0.1394	1.1847	0.7642
CP to Q ↑	0.1693	0.1858	1.9600	1.3023
CP to TQ ↓	0.1245	0.0767	7.5399	7.8603
CP to TQ ↑	0.1774	0.1105	21.2425	21.3498
SN to Q ↑	0.1330	0.1494	1.9593	1.3028
SN to TQ ↑	0.1411	0.0748	21.2412	21.3317

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_-P16	C8T28SOI_-LLHF_-SDFPSQTX3_-P16	C8T28SOIDV_-LL_-SDFPSQTX5_-P16	C8T28SOIDV_-LL_-SDFPSQTX10_-P16
CP ↓	min_pulse_width to CP	0.1682	0.1654	0.1486	0.1462
CP ↑	min_pulse_width to CP	0.1018	0.0830	0.0682	0.0589
D ↓	hold_rising to CP	-0.0827	-0.1577	-0.0344	-0.0436
D ↑	hold_rising to CP	-0.0213	-0.0218	-0.0116	-0.0137
D ↓	setup_rising to CP	0.1415	0.2323	0.1025	0.1083
D ↑	setup_rising to CP	0.0536	0.0563	0.0417	0.0417
SN ↓	min_pulse_width to SN	0.0767	0.0620	0.0620	0.0620
SN ↑	recovery_rising to CP	0.0155	0.0150	0.0063	0.0009
SN ↑	removal_rising to CP	0.0332	0.0483	0.0553	0.0553
TE ↓	hold_rising to CP	-0.0506	-0.0550	-0.0290	-0.0355
TE ↑	hold_rising to CP	-0.0218	-0.0191	-0.0120	-0.0218
TE ↓	setup_rising to CP	0.1399	0.1911	0.1009	0.1026
TE ↑	setup_rising to CP	0.1736	0.2277	0.1648	0.1540
TI ↓	hold_rising to CP	-0.1130	-0.1553	-0.0844	-0.0844
TI ↑	hold_rising to CP	-0.0218	-0.0162	-0.0105	-0.0217
TI ↓	setup_rising to CP	0.1712	0.2143	0.1573	0.1491
TI ↑	setup_rising to CP	0.0521	0.0502	0.0404	0.0515
		C8T28SOIDV_-LL_-SDFPSQTX19_-P16	C8T28SOIDV_-LL_-SDFPSQTX29_-P16		
CP ↓	min_pulse_width to CP	0.1421	0.1462		
CP ↑	min_pulse_width to CP	0.0589	0.0683		
D ↓	hold_rising to CP	-0.0436	-0.0409		
D ↑	hold_rising to CP	-0.0116	-0.0116		
D ↓	setup_rising to CP	0.1051	0.1083		
D ↑	setup_rising to CP	0.0417	0.0417		
SN ↓	min_pulse_width to SN	0.0620	0.0723		
SN ↑	recovery_rising to CP	-0.0012	0.0005		
SN ↑	removal_rising to CP	0.0553	0.0553		
TE ↓	hold_rising to CP	-0.0355	-0.0339		
TE ↑	hold_rising to CP	-0.0191	-0.0191		

TE ↓	setup_rising to CP	0.1036	0.1026		
TE ↑	setup_rising to CP	0.1550	0.1540		
TI ↓	hold_rising to CP	-0.0844	-0.0795		
TI ↑	hold_rising to CP	-0.0217	-0.0217		
TI ↓	setup_rising to CP	0.1433	0.1476		
TI ↑	setup_rising to CP	0.0515	0.0515		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P16	1.053e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P16	1.068e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P16	1.096e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P16	1.395e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P16	1.712e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P16	2.170e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

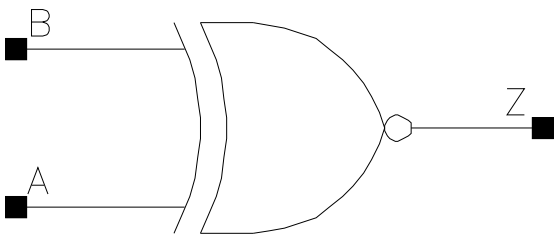
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P16	C8T28SOI_LLHF_-SDFPSQTX3_P16	C8T28SOIDV_LL_-SDFPSQTX5_P16	C8T28SOIDV_LL_-SDFPSQTX10_P16
Clock 100Mhz Data 0Mhz	5.991e-03	5.791e-03	5.591e-03	5.486e-03
Clock 100Mhz Data 25Mhz	6.043e-03	5.822e-03	5.601e-03	5.928e-03
Clock 100Mhz Data 50Mhz	6.096e-03	5.854e-03	5.610e-03	6.371e-03
Clock = 0 Data 100Mhz	2.859e-03	3.000e-03	2.930e-03	2.922e-03
Clock = 1 Data 100Mhz	2.294e-05	3.909e-04	2.689e-04	2.081e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P16	C8T28SOIDV_LL_-SDFPSQTX29_P16		
Clock 100Mhz Data 0Mhz	5.423e-03	5.382e-03		
Clock 100Mhz Data 25Mhz	6.330e-03	6.850e-03		
Clock 100Mhz Data 50Mhz	7.238e-03	8.318e-03		
Clock = 0 Data 100Mhz	2.911e-03	2.903e-03		
Clock = 1 Data 100Mhz	1.717e-04	1.474e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.600	0.544	0.8704
X5_P16	0.800	1.496	1.1968
X8_P16	1.600	1.088	1.7408
X9_P16	0.800	1.632	1.3056
X11_P16	1.600	1.360	2.1760
X14_P16	0.800	2.312	1.8496
X15_P16	1.600	1.904	3.0464
X19_P16	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P16	X5_P16	X8_P16	X9_P16
A	0.0010	0.0005	0.0017	0.0006
B	0.0010	0.0010	0.0014	0.0012
	X11_P16	X14_P16	X15_P16	X19_P16
A	0.0026	0.0009	0.0030	0.0011
B	0.0023	0.0016	0.0028	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X5_P16	X4_P16	X5_P16
A to Z ↓	0.0250	0.0764	6.4372	4.8507
A to Z ↑	0.0291	0.0667	10.8371	8.2442
B to Z ↓	0.0239	0.0556	6.4284	4.8309
B to Z ↑	0.0296	0.0505	10.8514	8.2302

	X8_P16	X9_P16	X8_P16	X9_P16
A to Z ↓	0.0298	0.0697	3.3583	2.4938
A to Z ↑	0.0355	0.0623	5.6596	4.1892
B to Z ↓	0.0287	0.0523	3.3543	2.4889
B to Z ↑	0.0345	0.0483	5.6676	4.1878
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0278	0.0666	2.3435	1.6836
A to Z ↑	0.0325	0.0581	3.7138	2.6676
B to Z ↓	0.0258	0.0487	2.3404	1.6797
B to Z ↑	0.0309	0.0451	3.7234	2.6622
	X15_P16	**X19_P16**	**X15_P16**	**X19_P16**
A to Z ↓	0.0305	0.0608	1.7692	1.2535
A to Z ↑	0.0358	0.0548	2.8187	1.9880
B to Z ↓	0.0283	0.0457	1.7650	1.2506
B to Z ↑	0.0340	0.0432	2.8221	1.9859

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	4.763e-06	1.000e-20
X5_P16	5.589e-06	1.000e-20
X8_P16	7.665e-06	1.000e-20
X9_P16	8.860e-06	1.000e-20
X11_P16	1.144e-05	1.000e-20
X14_P16	1.327e-05	1.000e-20
X15_P16	1.461e-05	1.000e-20
X19_P16	1.808e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X5_P16	X8_P16	X9_P16
A to Z	1.314e-03	2.785e-03	2.624e-03	3.840e-03
B to Z	1.284e-03	2.204e-03	2.535e-03	3.039e-03
	X11_P16	X14_P16	X15_P16	X19_P16
A to Z	3.727e-03	6.065e-03	5.039e-03	7.305e-03
B to Z	3.577e-03	4.695e-03	4.834e-03	5.783e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

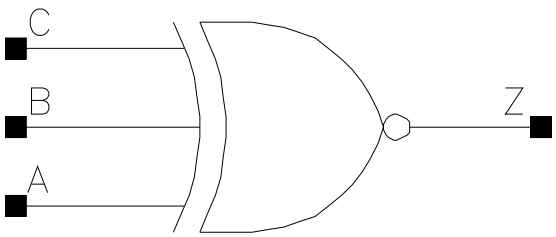
Pin Cycle (vdds)	X4_P16	X5_P16	X8_P16	X9_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P16	X14_P16	X15_P16	X19_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P16	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P16	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P16	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P16	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P16	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P16	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P16	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P16	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P16	C8T28SOIDV_LL_-XNOR3X4_P16	C8T28SOIDV_LL_-XNOR3X9_P16	C8T28SOIDV_LL_-XNOR3X13_P16
A	0.0015	0.0015	0.0020	0.0026
B	0.0015	0.0014	0.0019	0.0025
C	0.0007	0.0006	0.0006	0.0006
	C8T28SOIDV_LLS_-XNOR3X1_P16	C8T28SOIDV_LLS_-XNOR3X2_P16	C8T28SOIDV_LLS_-XNOR3X5_P16	C8T28SOIDV_LLS_-XNOR3X7_P16

A	0.0015	0.0017	0.0037	0.0057
B	0.0015	0.0018	0.0034	0.0053
C	0.0010	0.0013	0.0024	0.0036

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XNOR3X2_P16	**C8T28SOIDV_LL_-XNOR3X4_P16**	**C8T28SOIDV_LL_-XNOR3X2_P16**	**C8T28SOIDV_LL_-XNOR3X4_P16**
A to Z ↓	0.0793	0.0849	10.1442	5.3034
A to Z ↑	0.0749	0.0762	15.5869	8.3599
B to Z ↓	0.0799	0.0857	10.1502	5.3028
B to Z ↑	0.0758	0.0772	15.5907	8.3600
C to Z ↓	0.1071	0.1146	10.1476	5.3029
C to Z ↑	0.1030	0.1058	15.5797	8.3637
	C8T28SOIDV_LL_-XNOR3X9_P16	**C8T28SOIDV_LL_-XNOR3X13_P16**	**C8T28SOIDV_LL_-XNOR3X9_P16**	**C8T28SOIDV_LL_-XNOR3X13_P16**
A to Z ↓	0.0716	0.0819	2.6537	1.8097
A to Z ↑	0.0743	0.0834	4.0807	2.8049
B to Z ↓	0.0727	0.0829	2.6529	1.8099
B to Z ↑	0.0757	0.0849	4.0809	2.8045
C to Z ↓	0.1041	0.1245	2.6535	1.8092
C to Z ↑	0.1069	0.1270	4.0810	2.8061
	C8T28SOIDV_LLS_-XNOR3X1_P16	**C8T28SOIDV_LLS_-XNOR3X2_P16**	**C8T28SOIDV_LLS_-XNOR3X1_P16**	**C8T28SOIDV_LLS_-XNOR3X2_P16**
A to Z ↓	0.0465	0.0525	19.0127	10.1636
A to Z ↑	0.0487	0.0475	32.8749	16.7343
B to Z ↓	0.0476	0.0541	19.0121	10.1606
B to Z ↑	0.0496	0.0488	32.8381	16.7168
C to Z ↓	0.0457	0.0505	18.9983	10.1731
C to Z ↑	0.0485	0.0465	32.7926	16.7087
	C8T28SOIDV_LLS_-XNOR3X5_P16	**C8T28SOIDV_LLS_-XNOR3X7_P16**	**C8T28SOIDV_LLS_-XNOR3X5_P16**	**C8T28SOIDV_LLS_-XNOR3X7_P16**
A to Z ↓	0.0522	0.0439	4.7740	3.3090
A to Z ↑	0.0498	0.0428	8.1475	5.4424
B to Z ↓	0.0513	0.0424	4.7778	3.3136
B to Z ↑	0.0490	0.0420	8.1382	5.4383
C to Z ↓	0.0480	0.0405	4.7709	3.3126
C to Z ↑	0.0461	0.0396	8.1267	5.4325

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P16	3.812e-06	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P16	4.488e-06	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P16	7.713e-06	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P16	1.092e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P16	2.543e-06	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P16	4.185e-06	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P16	1.010e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P16	1.498e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P16	C8T28SOIDV_LL_-XNOR3X4_P16	C8T28SOIDV_LL_-XNOR3X9_P16	C8T28SOIDV_LL_-XNOR3X13_P16
A to Z	1.754e-03	2.073e-03	3.082e-03	5.094e-03
B to Z	1.730e-03	2.051e-03	3.088e-03	5.104e-03
C to Z	2.778e-03	3.143e-03	4.451e-03	7.198e-03
	C8T28SOIDV_LLS_-XNOR3X1_P16	C8T28SOIDV_LLS_-XNOR3X2_P16	C8T28SOIDV_LLS_-XNOR3X5_P16	C8T28SOIDV_LLS_-XNOR3X7_P16
A to Z	1.044e-03	1.530e-03	3.379e-03	4.627e-03
B to Z	1.032e-03	1.542e-03	3.362e-03	4.490e-03
C to Z	1.003e-03	1.510e-03	3.234e-03	4.336e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

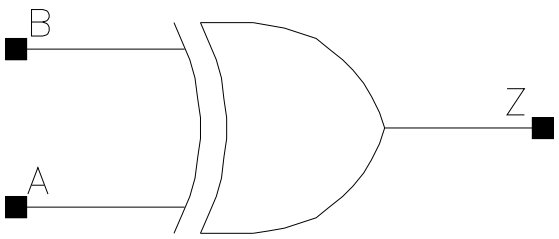
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P16	C8T28SOIDV_LL_-XNOR3X4_P16	C8T28SOIDV_LL_-XNOR3X9_P16	C8T28SOIDV_LL_-XNOR3X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P16	C8T28SOIDV_LLS_-XNOR3X2_P16	C8T28SOIDV_LLS_-XNOR3X5_P16	C8T28SOIDV_LLS_-XNOR3X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.360	1.0880
X4_P16	1.600	0.544	0.8704
X5_P16	0.800	1.360	1.0880
X8_P16	1.600	1.088	1.7408
X9_P16	0.800	1.496	1.1968
X12_P16	1.600	1.360	2.1760
X13_P16	0.800	2.176	1.7408
X15_P16	1.600	1.904	3.0464
X17_P16	0.800	2.312	1.8496
X18_P16	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P16	X4_P16	X5_P16	X8_P16
A	0.0005	0.0010	0.0007	0.0017
B	0.0010	0.0010	0.0011	0.0016
	X9_P16	X12_P16	X13_P16	X15_P16
A	0.0007	0.0026	0.0012	0.0031
B	0.0014	0.0021	0.0022	0.0026
	X17_P16	X18_P16		
A	0.0012	0.0016		
B	0.0022	0.0020		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X4_P16**	**X2_P16**	**X4_P16**
A to Z ↓	0.0651	0.0268	9.6154	4.8807
A to Z ↑	0.0610	0.0308	16.0107	14.1829
B to Z ↓	0.0485	0.0268	9.5519	4.9112
B to Z ↑	0.0502	0.0291	15.9945	14.1613
	X5_P16	**X8_P16**	**X5_P16**	**X8_P16**
A to Z ↓	0.0603	0.0351	4.9510	2.6134
A to Z ↑	0.0534	0.0368	8.0507	7.3270
B to Z ↓	0.0446	0.0357	4.9294	2.6301
B to Z ↑	0.0436	0.0353	8.0458	7.3144
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0582	0.0315	2.6146	1.7654
A to Z ↑	0.0532	0.0329	4.1455	4.9017
B to Z ↓	0.0435	0.0295	2.6078	1.7762
B to Z ↑	0.0426	0.0303	4.1451	4.8928
	X13_P16	**X15_P16**	**X13_P16**	**X15_P16**
A to Z ↓	0.0535	0.0341	1.7755	1.3609
A to Z ↑	0.0491	0.0378	2.8722	4.3334
B to Z ↓	0.0368	0.0318	1.7704	1.3698
B to Z ↑	0.0348	0.0350	2.8704	4.3248
	X17_P16	**X18_P16**	**X17_P16**	**X18_P16**
A to Z ↓	0.0566	0.0623	1.3505	1.3584
A to Z ↑	0.0513	0.0551	2.1526	2.1077
B to Z ↓	0.0399	0.0470	1.3477	1.3567
B to Z ↑	0.0371	0.0427	2.1511	2.1073

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P16	4.355e-06	1.000e-20
X4_P16	4.899e-06	1.000e-20
X5_P16	6.627e-06	1.000e-20
X8_P16	7.997e-06	1.000e-20
X9_P16	1.027e-05	1.000e-20
X12_P16	1.196e-05	1.000e-20
X13_P16	1.646e-05	1.000e-20
X15_P16	1.463e-05	1.000e-20
X17_P16	1.769e-05	1.000e-20
X18_P16	1.783e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P16	X4_P16	X5_P16	X8_P16
A to Z	2.048e-03	1.348e-03	2.591e-03	2.687e-03
B to Z	1.783e-03	1.287e-03	2.199e-03	2.663e-03
	X9_P16	X12_P16	X13_P16	X15_P16
A to Z	3.683e-03	3.783e-03	5.997e-03	4.937e-03
B to Z	3.184e-03	3.547e-03	3.821e-03	4.681e-03
	X17_P16	X18_P16		
A to Z	6.721e-03	7.439e-03		
B to Z	4.524e-03	5.570e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

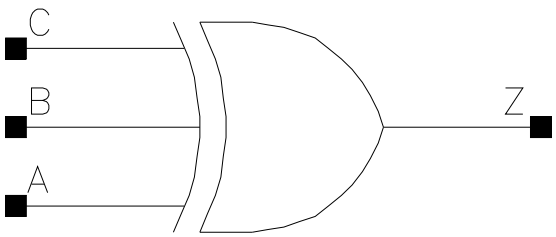
Pin Cycle (vdds)	X2_P16	X4_P16	X5_P16	X8_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P16	X12_P16	X13_P16	X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P16	X18_P16		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P16	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P16	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P16	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P16	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P16	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P16	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P16	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P16	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P16	C8T28SOIDV_LL_-XOR3X4_P16	C8T28SOIDV_LL_-XOR3X9_P16	C8T28SOIDV_LL_-XOR3X13_P16
A	0.0016	0.0015	0.0018	0.0026
B	0.0015	0.0016	0.0019	0.0025
C	0.0010	0.0010	0.0013	0.0021
	C8T28SOIDV_LLS_-XOR3X1_P16	C8T28SOIDV_LLS_-XOR3X2_P16	C8T28SOIDV_LLS_-XOR3X5_P16	C8T28SOIDV_LLS_-XOR3X7_P16

A	0.0016	0.0018	0.0030	0.0045
B	0.0017	0.0017	0.0029	0.0046
C	0.0005	0.0006	0.0005	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P16	**C8T28SOIDV_LL_-XOR3X4_P16**	**C8T28SOIDV_LL_-XOR3X2_P16**	**C8T28SOIDV_LL_-XOR3X4_P16**
A to Z ↓	0.0774	0.0854	10.2025	5.3181
A to Z ↑	0.0734	0.0789	16.0242	8.3551
B to Z ↓	0.0776	0.0865	10.2008	5.3183
B to Z ↑	0.0741	0.0806	16.0303	8.3563
C to Z ↓	0.0766	0.0852	10.2047	5.3193
C to Z ↑	0.0724	0.0780	16.0264	8.3569
	C8T28SOIDV_LL_-XOR3X9_P16	**C8T28SOIDV_LL_-XOR3X13_P16**	**C8T28SOIDV_LL_-XOR3X9_P16**	**C8T28SOIDV_LL_-XOR3X13_P16**
A to Z ↓	0.0759	0.0842	2.6352	1.7519
A to Z ↑	0.0764	0.0851	4.0927	2.7530
B to Z ↓	0.0772	0.0852	2.6361	1.7514
B to Z ↑	0.0782	0.0867	4.0952	2.7534
C to Z ↓	0.0752	0.0841	2.6352	1.7520
C to Z ↑	0.0750	0.0856	4.0957	2.7532
	C8T28SOIDV_LLS_-XOR3X1_P16	**C8T28SOIDV_LLS_-XOR3X2_P16**	**C8T28SOIDV_LLS_-XOR3X1_P16**	**C8T28SOIDV_LLS_-XOR3X2_P16**
A to Z ↓	0.0491	0.0546	13.2672	10.3970
A to Z ↑	0.0491	0.0475	23.3210	15.9607
B to Z ↓	0.0504	0.0555	13.2962	10.3942
B to Z ↑	0.0502	0.0483	23.3286	15.9451
C to Z ↓	0.0782	0.0850	13.3307	10.3972
C to Z ↑	0.0796	0.0789	23.3488	15.9197
	C8T28SOIDV_LLS_-XOR3X5_P16	**C8T28SOIDV_LLS_-XOR3X7_P16**	**C8T28SOIDV_LLS_-XOR3X5_P16**	**C8T28SOIDV_LLS_-XOR3X7_P16**
A to Z ↓	0.0736	0.0624	5.3128	3.6818
A to Z ↑	0.0597	0.0512	8.2163	5.5265
B to Z ↓	0.0698	0.0614	5.3243	3.6855
B to Z ↑	0.0582	0.0512	8.2128	5.5226
C to Z ↓	0.1184	0.0980	5.3497	3.6896
C to Z ↑	0.1070	0.0873	8.2108	5.5150

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P16	3.119e-06	1.000e-20
C8T28SOIDV_LL_XOR3X4_P16	3.858e-06	1.000e-20
C8T28SOIDV_LL_XOR3X9_P16	6.813e-06	1.000e-20
C8T28SOIDV_LL_XOR3X13_P16	1.020e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P16	4.268e-06	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P16	4.962e-06	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P16	8.647e-06	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P16	1.284e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P16	C8T28SOIDV_LL_-XOR3X4_P16	C8T28SOIDV_LL_-XOR3X9_P16	C8T28SOIDV_LL_-XOR3X13_P16
A to Z	1.672e-03	2.075e-03	3.114e-03	5.415e-03
B to Z	1.643e-03	2.064e-03	3.123e-03	5.414e-03
C to Z	1.613e-03	2.026e-03	3.091e-03	5.403e-03
	C8T28SOIDV_LLS_-XOR3X1_P16	C8T28SOIDV_LLS_-XOR3X2_P16	C8T28SOIDV_LLS_-XOR3X5_P16	C8T28SOIDV_LLS_-XOR3X7_P16
A to Z	1.280e-03	1.568e-03	3.131e-03	4.361e-03
B to Z	1.277e-03	1.577e-03	3.139e-03	4.377e-03
C to Z	2.475e-03	2.846e-03	5.229e-03	7.319e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P16	C8T28SOIDV_LL_-XOR3X4_P16	C8T28SOIDV_LL_-XOR3X9_P16	C8T28SOIDV_LL_-XOR3X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P16	C8T28SOIDV_LLS_-XOR3X2_P16	C8T28SOIDV_LLS_-XOR3X5_P16	C8T28SOIDV_LLS_-XOR3X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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