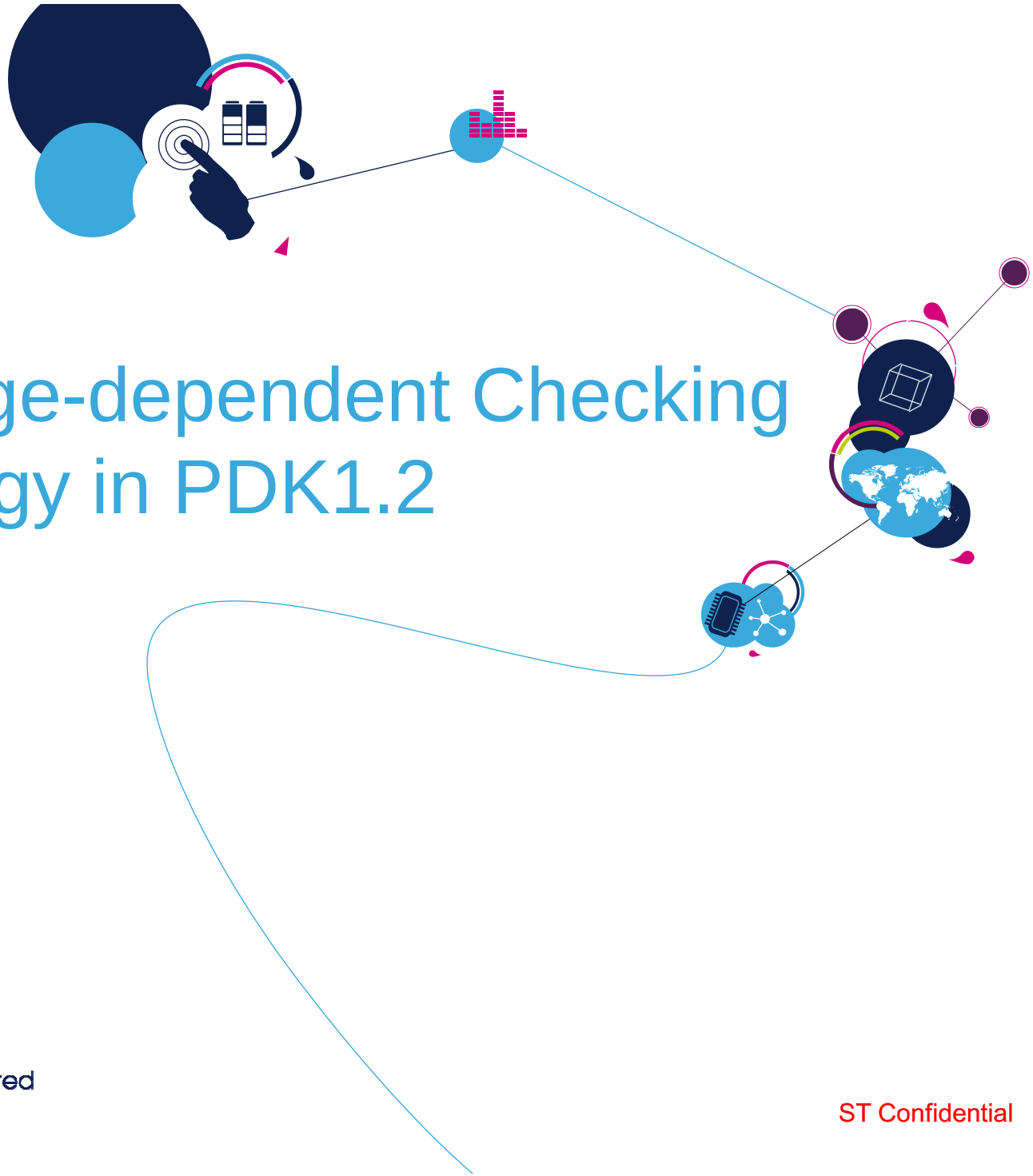
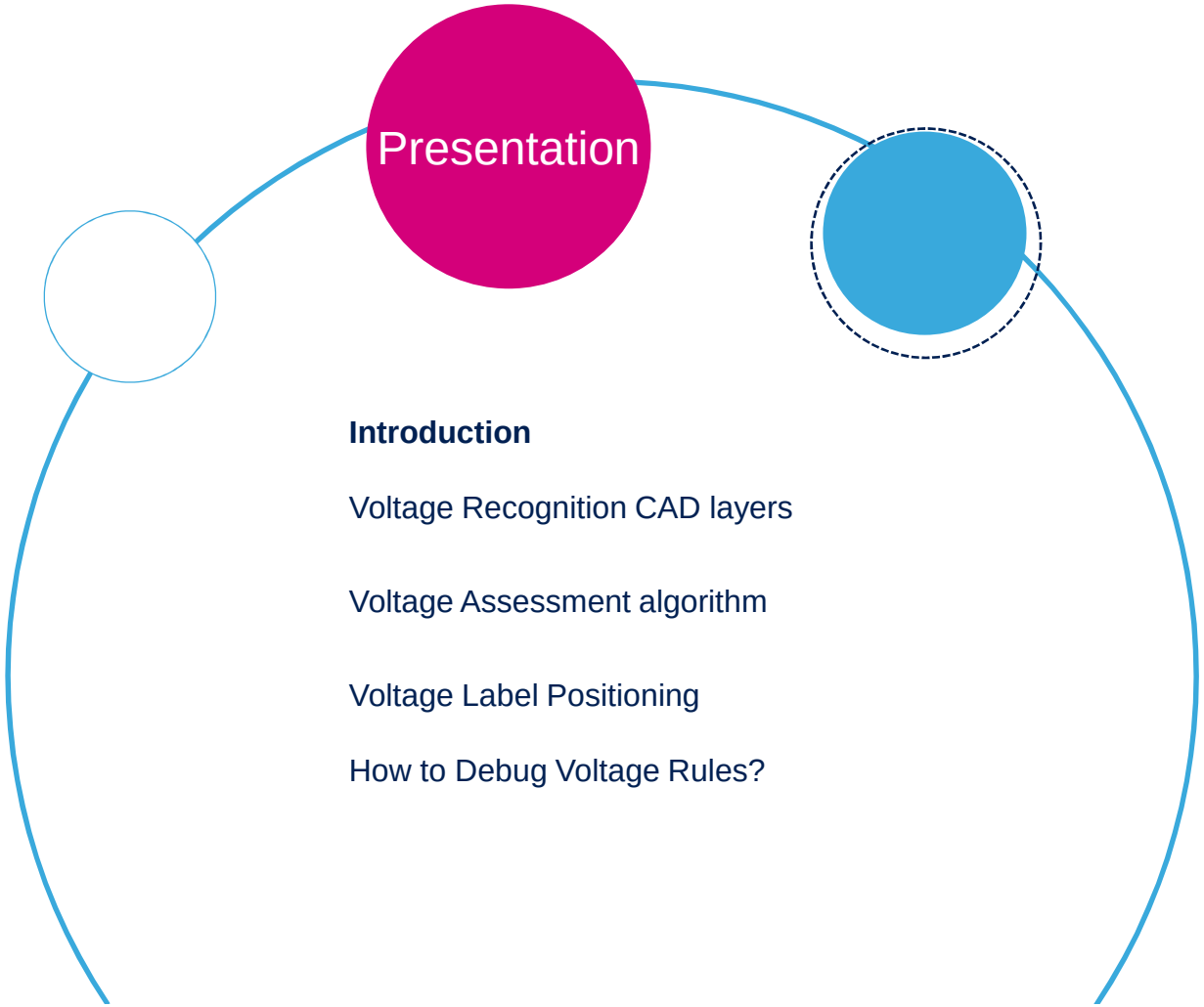


New Voltage-dependent Checking Methodology in PDK1.2

life.augmented

Agenda



Introduction

Voltage Recognition CAD layers

Voltage Assessment algorithm

Voltage Label Positioning

How to Debug Voltage Rules?

life.augmented

PDK 1.2 Updates on Voltage-dependent Checking

- Unified mechanics in between
  - Traditional voltage-related checking
  - Body Bias management
- An industry-standard approach
  - Voltage difference based
    - Deriving a min & max voltage for each net
  - Using labels to tag BB nets
    - With automatic propagation throughout connectivity & hierarchy
    - Enabling a continuous set of values
- A flexible & robust approach compatible with any mission profile
  - More appropriate for external customer usage
  - Simpler SoC integration
  - Slightly more conservative, due to coding: identical mission profile for every voltage
  - Covering voltage ranges up to 10V

Voltage determination & space requirement

- The DRC mechanism allows various voltage determination schemes
  - Information can be derived from the nature of the devices connected to the net (SG, EG, …)
  - Information can be overridden using markers (already existing in previous PDK)
  - Information can be overridden using dedicated labels
    - Note: specific layers have been introduced for that purpose: no link with LVS nets / pins / labels

➔ No need to systematically add labels
➔ This new mechanism is backward compatible with existing GDS. It complements previous mechanism & handle previous markers

- The maximum voltage difference is determined in between the 2 nets from both voltage ranges

- A unique set of rules require a given spacing for a given maximum voltage difference

Need for new Labels or not ?

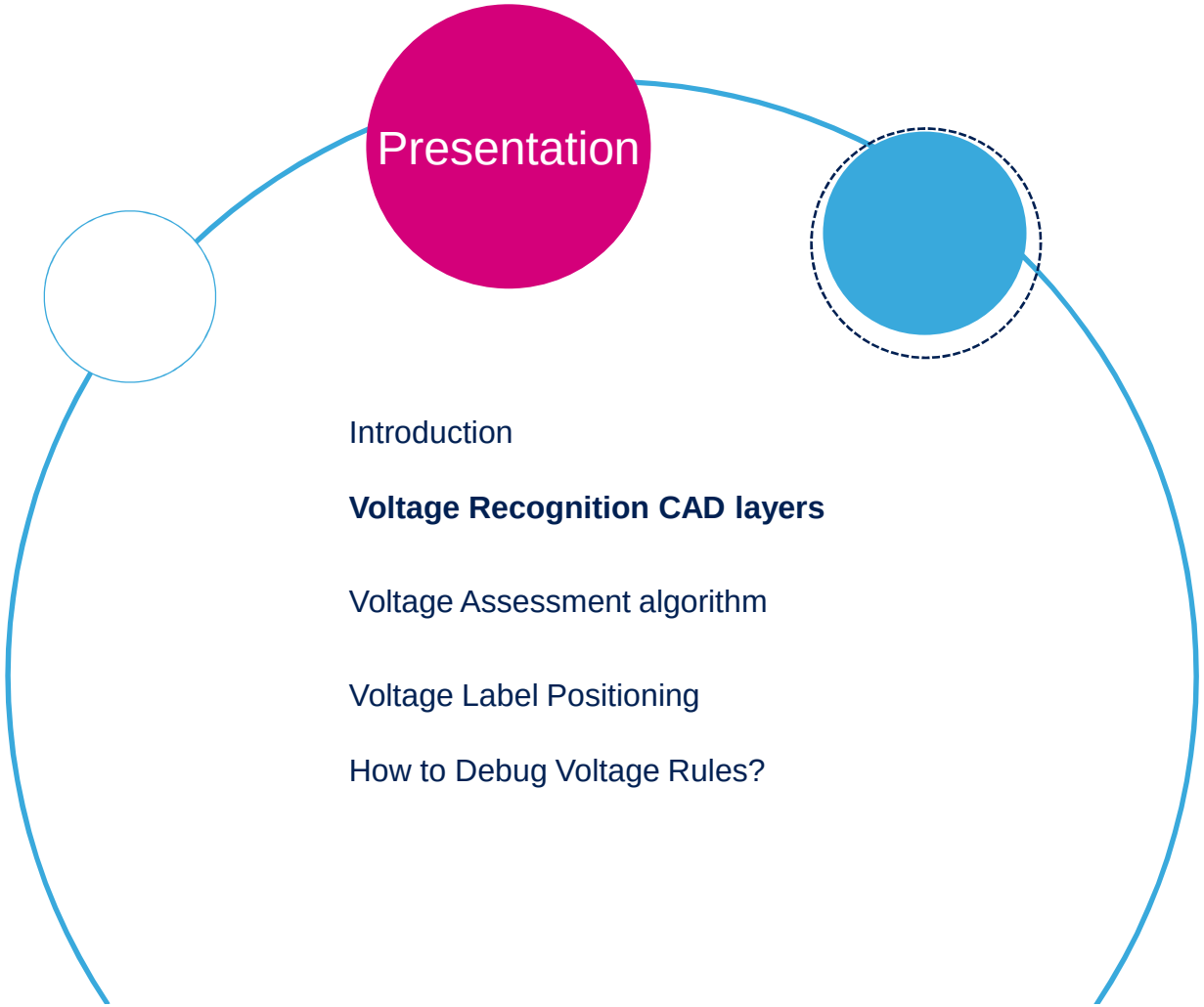
- Most of the time: no GDS modification required (no label to add)
- Labels are mandatory if
  - Negative voltage is being used
  - Voltages greater than the nominal voltage of the connected devices is being used (typical case of cascoded devices)
  - Well biasing is performed from an external bias
    Note: only 2 labels (V high & V low) for each well supply are required

Impossible to determine w/o user input

- If wells are biased with a voltage generated internally to the circuit
  - By default this voltage is assumed to be in the range [0 → nominal voltage of the connected devices]
    - E.g. [0V-1V] if connected to a SG device
    - E.g. [0V-1.8V] if connected to an EG device

    → safe: no need to add labels
  - If too conservative, can be overridden thanks to labels

Agenda



Introduction

Voltage Recognition CAD layers

Voltage Assessment algorithm

Voltage Label Positioning

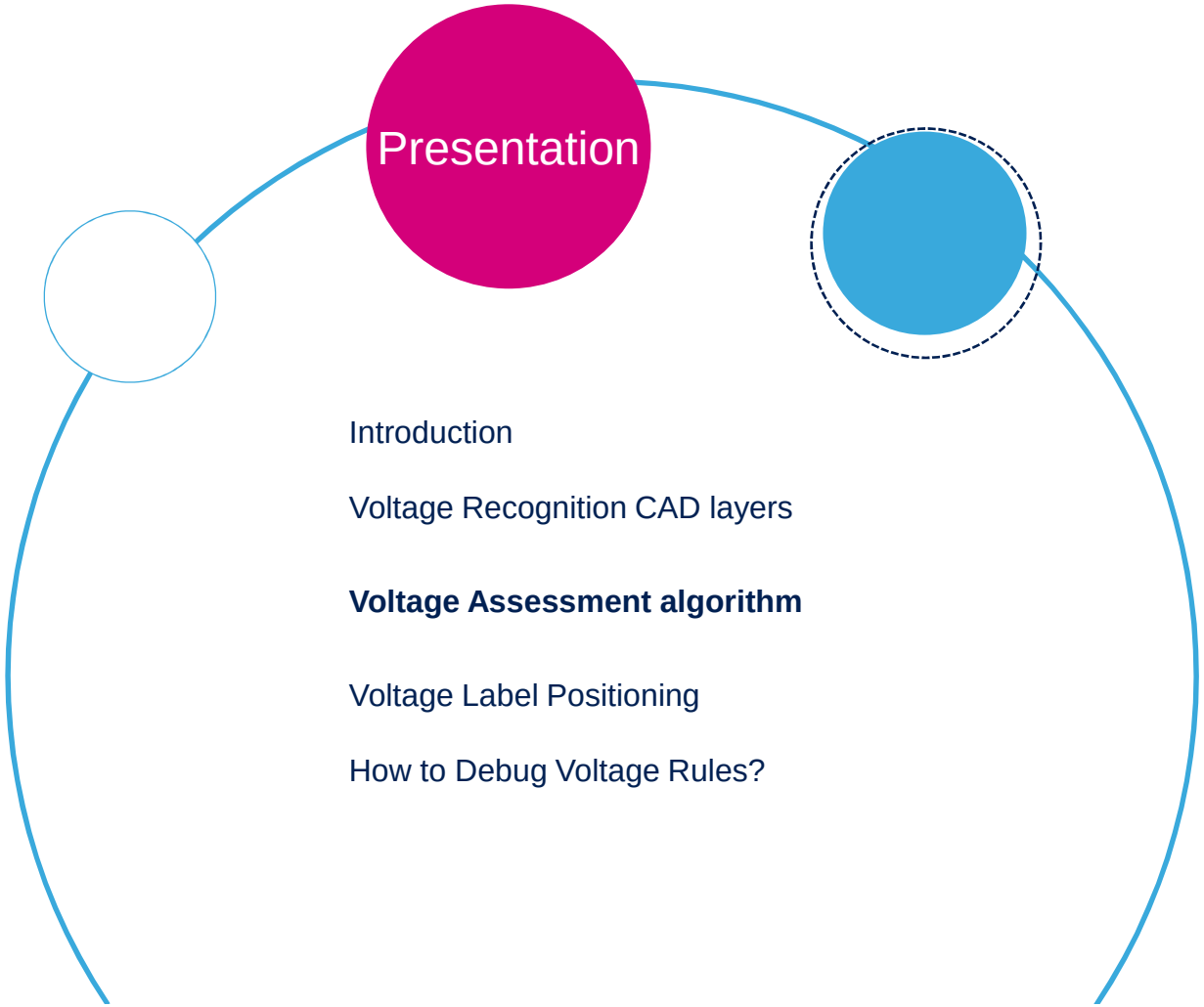
How to Debug Voltage Rules?

life.augmented

Voltage Recognition CAD layers

Name	Number	Description
RX;VH	2;155	Used to define the highest voltage of the net for RX level
RX;VL	2;156	Used to define the lowest voltage of the net for RX level
PC;VH	7;155	Used to define the highest voltage of the net for PC level
PC;VL	7;156	Used to define the lowest voltage of the net for PC level
M1;VH	15;155	Used to define the highest voltage of the net for M1 level
M1;VL	15;156	Used to define the lowest voltage of the net for M1 level
M2;VH	17;155	Used to define the highest voltage of the net for M2 level
M2;VL	17;156	Used to define the lowest voltage of the net for M2 level
M3;VH	19;155	Used to define the highest voltage of the net for M3 level
M3;VL	19;156	Used to define the lowest voltage of the net for M3 level
M4;VH	21;155	Used to define the highest voltage of the net for M4 level
M4;VL	21;156	Used to define the lowest voltage of the net for M4 level
M5;VH	31;155	Used to define the highest voltage of the net for M5 level
M5;VL	31;156	Used to define the lowest voltage of the net for M5 level
M6;VH	44;155	Used to define the highest voltage of the net for M6 level
M6;VL	44;156	Used to define the lowest voltage of the net for M6 level
B1;VH	79;155	Used to define the highest voltage of the net for B1 level
B1;VL	79;156	Used to define the lowest voltage of the net for B1 level
B2;VH	81;155	Used to define the highest voltage of the net for B2 level
B2;VL	81;156	Used to define the lowest voltage of the net for B2 level
IA;VH	136;155	Used to define the highest voltage of the net for IA level
IA;VL	136;156	Used to define the lowest voltage of the net for IA level
IB;VH	137;155	Used to define the highest voltage of the net for IB level
IB;VL	137;156	Used to define the lowest voltage of the net for IB level
LB;VH	69;155	Used to define the highest voltage of the net for LB level
LB;VL	69;156	Used to define the lowest voltage of the net for LB level

Agenda



Introduction

Voltage Recognition CAD layers

Voltage Assessment algorithm

Voltage Label Positioning

How to Debug Voltage Rules?

life.augmented

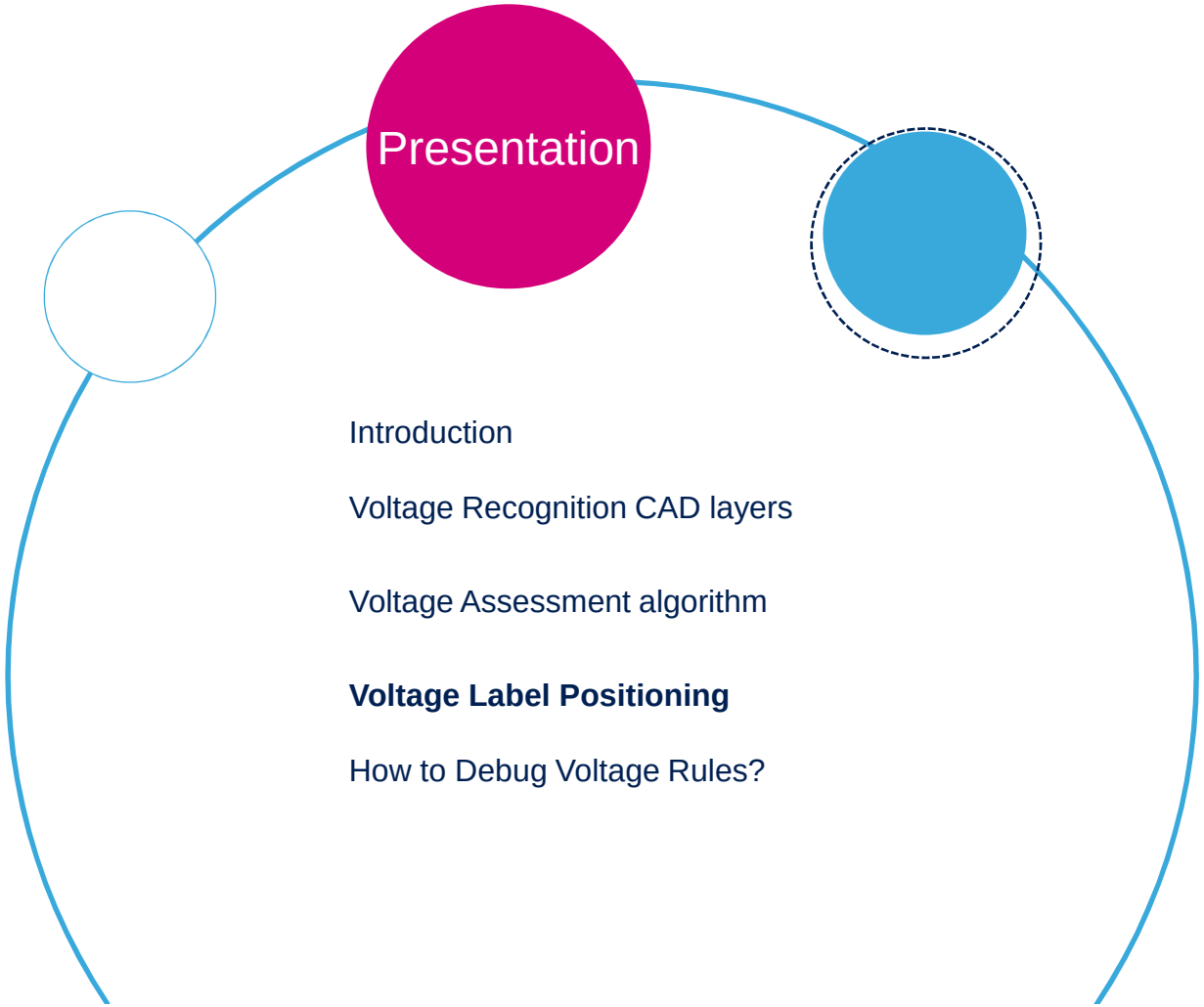
Voltage Assessment algorithm

The net voltage is determined in the following way:

- Based on **voltage information** provided by designer through xx_VL/VH labels.
  In case of net marked by different values on a same voltage label (VL/VH), it is assigned to the minimum/maximum one.

- **If not xx_VL/VH label marker** is detected ➔ **Layout** recognition (by decreasing prio order)
  1. **RX substrate contact (strap contacting the substrate (not isolated p-well))**
     VL=0.0/VH=0.0
  2. **xx_VDD maker** (eg: M1_VDD5V // M3_VDD3V3)
     VL=0.0/VH=VDD marker value (eg: 5.0 // 3.3)
     In case of net marked by different markers, it is assigned to the maximum one
  3. **SG device**
     VL=0.0 / VH=1.0
  4. **EGV MOS (EG underdriven to 1.5V)**
     VL=0.0 / VH=1.5
  5. **EG device**
     VL=0.0 / VH=1.8
  6. **Extended-drain devices (R&D device)**
     VL=0.0 / VH=5.0
  7. **Remaning floating nets**
     VL=0.0/VH=1.0

Agenda



Introduction

Voltage Recognition CAD layers

Voltage Assessment algorithm

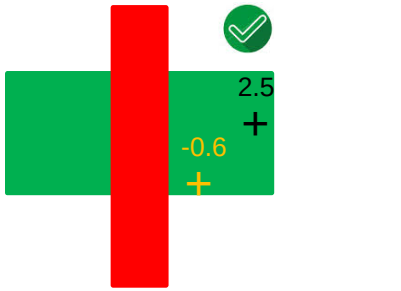
Voltage Label Positioning

How to Debug Voltage Rules?

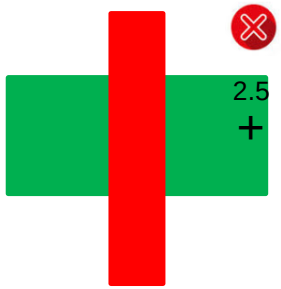
Voltage Label Positioning (1/4)

xx_VH/xx_VL labels must obey the following rules:

- Label must be covered by its corresponding “drawing” layer (example: M4_VH label must be covered by M4_drawing shape).
- Only text data is allowed.
- Only single floating point value is allowed (see following slide).
- Voltage label must be within minimum/maximum authorized Design Rule Manual values.
- If xx_VH is used, xx_VL must be used on the same shape; in the same way if xx_VL is used, xx_VH must be used on the same shape.

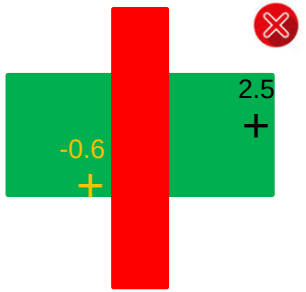


Voltage High label in CAD RX_VH
Voltage Low label in CAD RX_VL



Voltage High label in CAD RX_VH
Voltage Low Missing

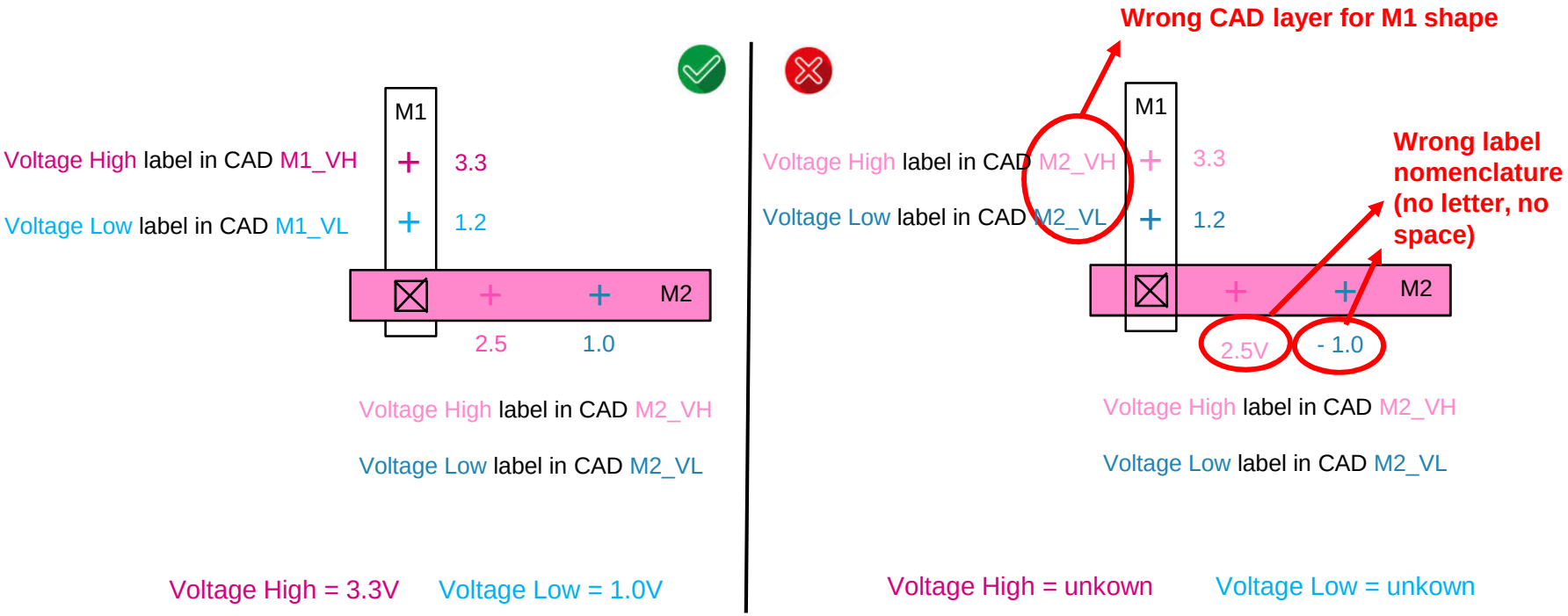
Voltage High missing
Voltage Low label in CAD RX_VL



Voltage High label in CAD RX_VH
Voltage Low label in CAD RX_VL
Voltage High missing on left diffusion
Voltage Low missing on right diffusion

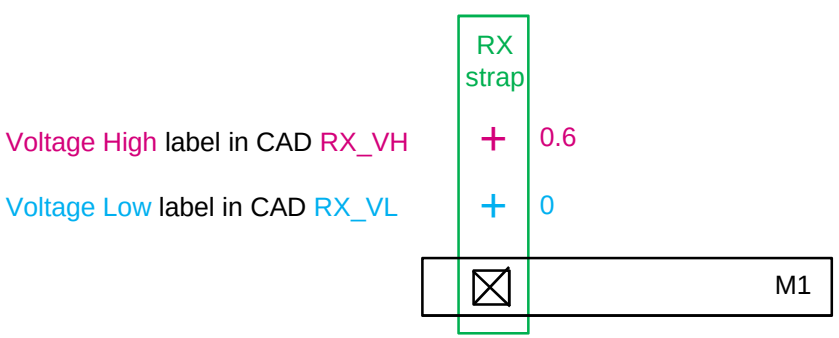
Voltage Label Positioning (2/4)

- In case of multiple Voltage labels on a same net:
  - Voltage High will be the **maximum** Voltage High value
  - Voltage Low will be the **minimum** Voltage Low value
- How to mark nets ?

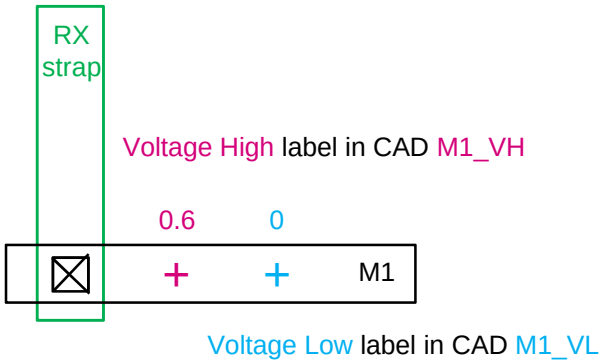


Voltage Label Positioning (3/4)

- If a body biasing of **+0.6V** is used



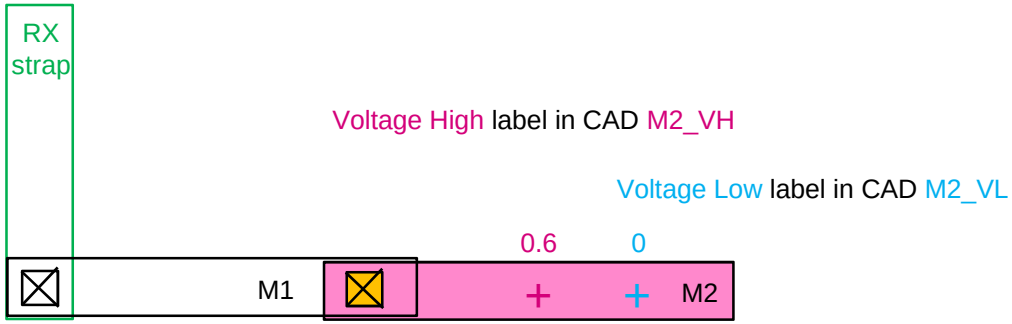
OR

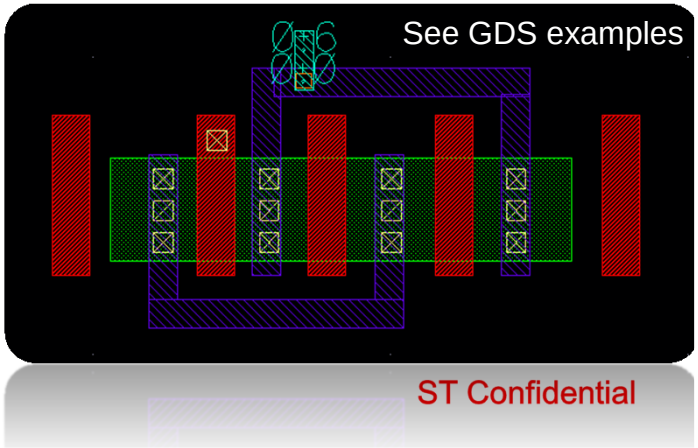


Voltage High = 0.6V Voltage Low = 0V

Voltage High = 0.6V Voltage Low = 0V

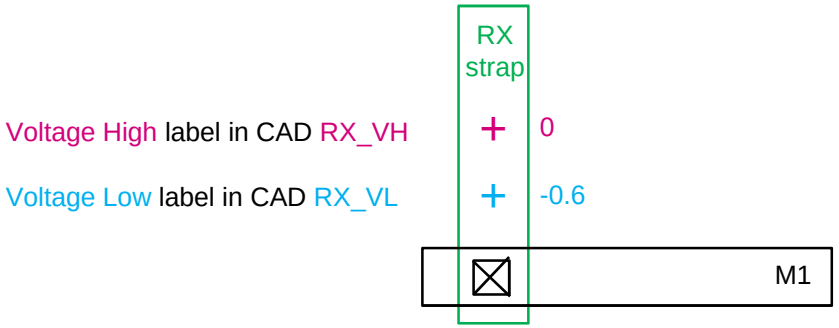
OR …. placed at other metal level **on the same net**



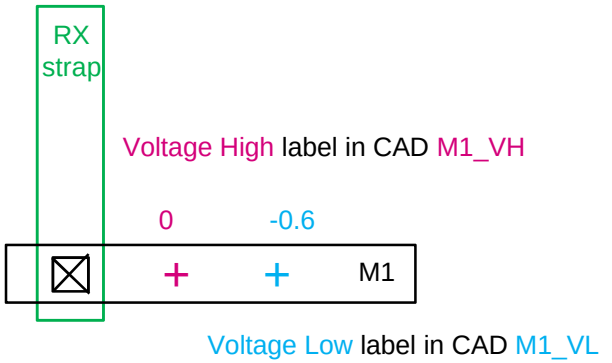


Voltage Label Positioning (4/4)

- If a body biasing of **-0.6V** is used



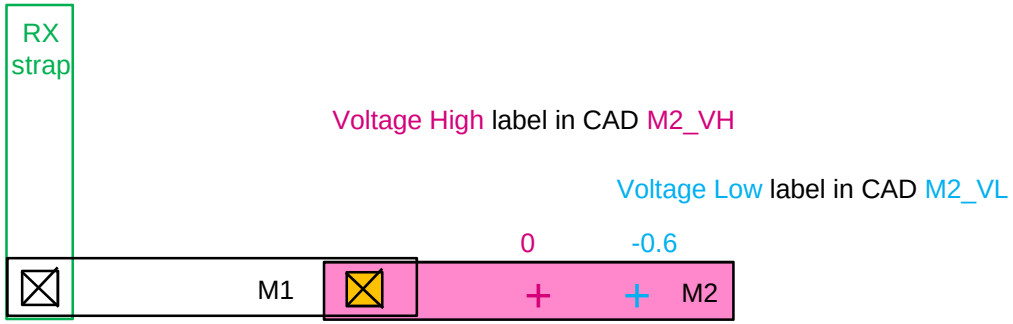
OR

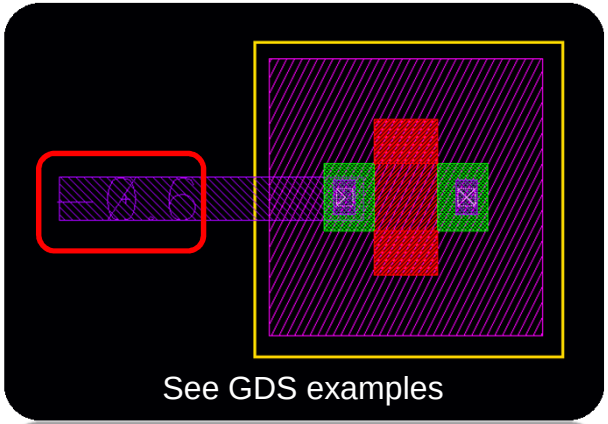


Voltage High = 0V Voltage Low = -0.6V

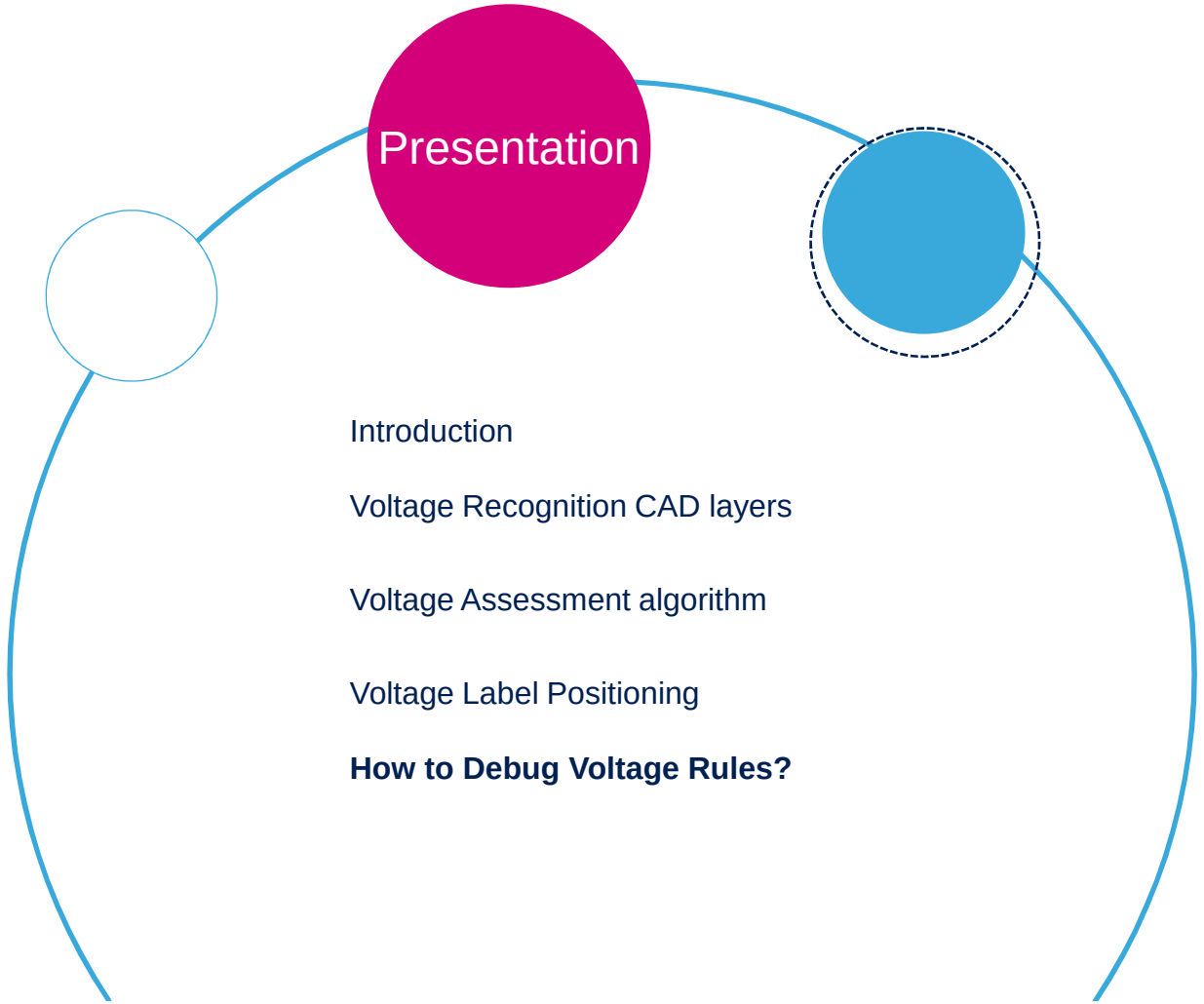
Voltage High = 0V Voltage Low = -0.6V

OR …. placed at other metal level **on the same net**





Agenda



Introduction

Voltage Recognition CAD layers

Voltage Assessment algorithm

Voltage Label Positioning

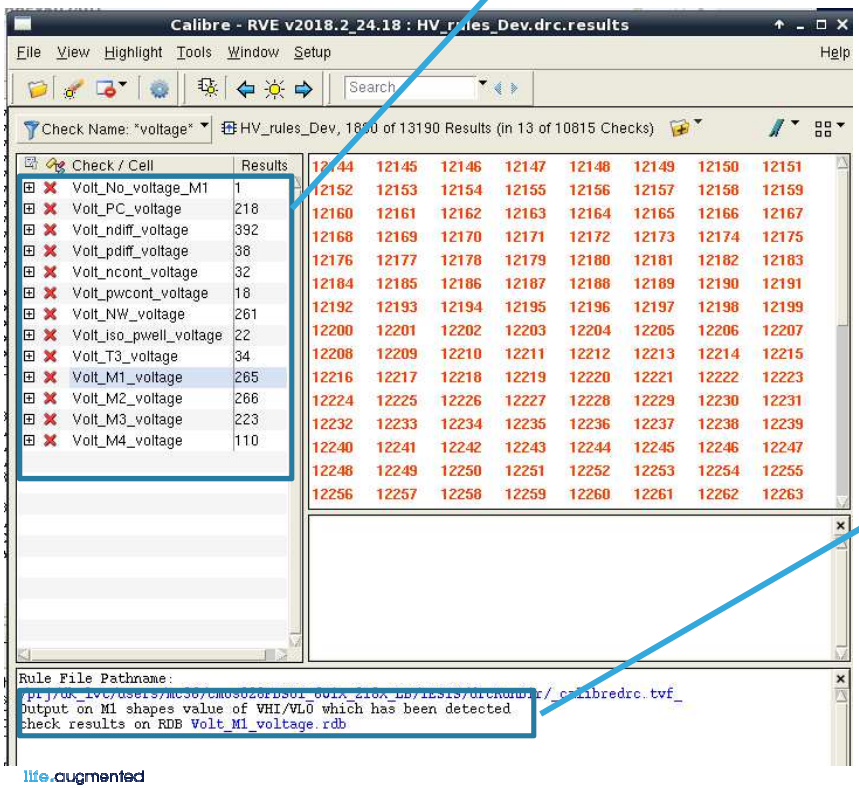
How to Debug Voltage Rules?

life.augmented

How to Debug Voltage Rules? (1/4)

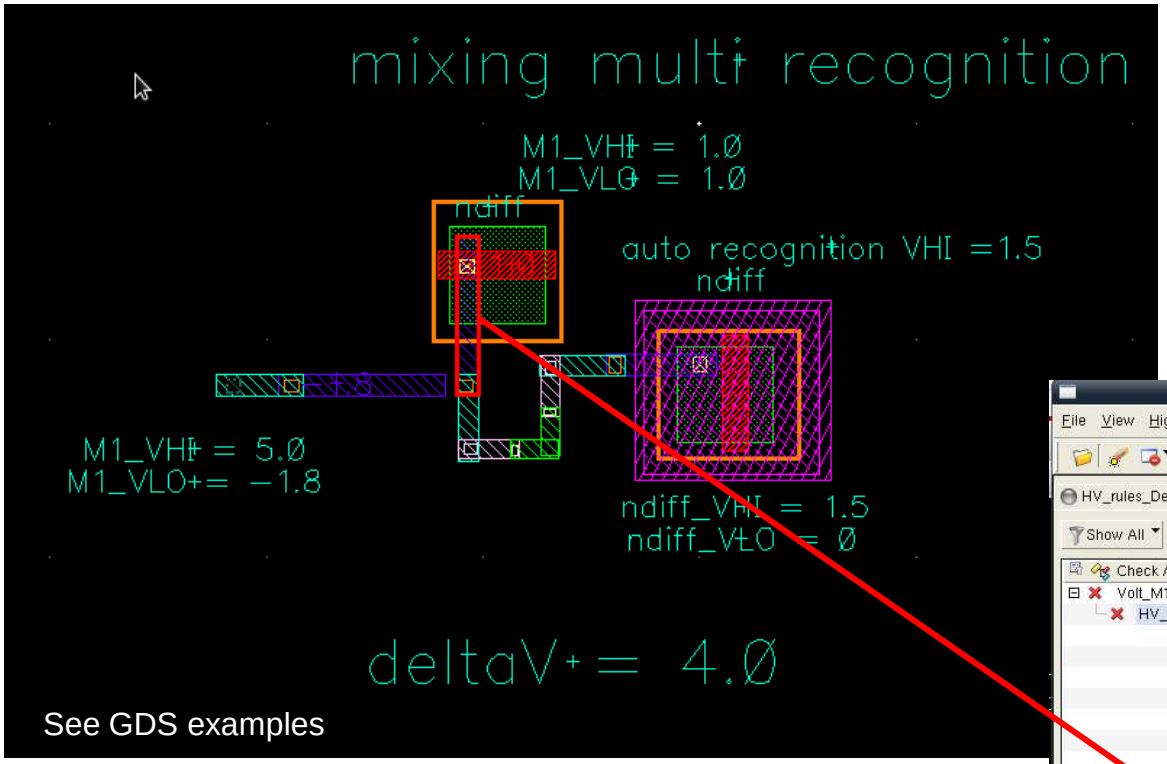
- Use VOLTAGE_DEBUG switch

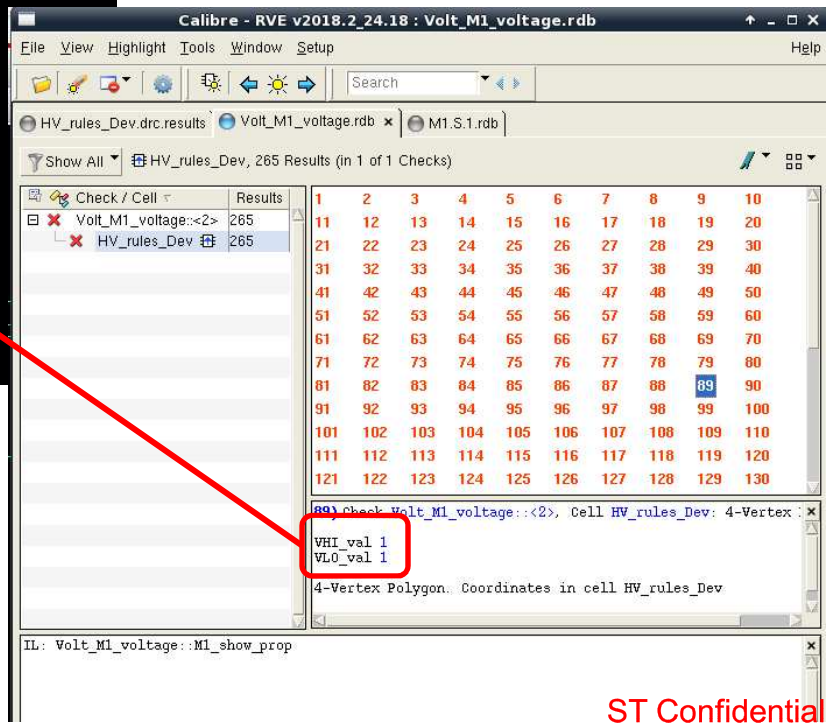
Addition debug rules **Volt_xx_voltage** will be displayed within Calibre RVE windows (not sign-off)



Voltage information is stored within RDB file

How to Debug Voltage Rules? (2/4)



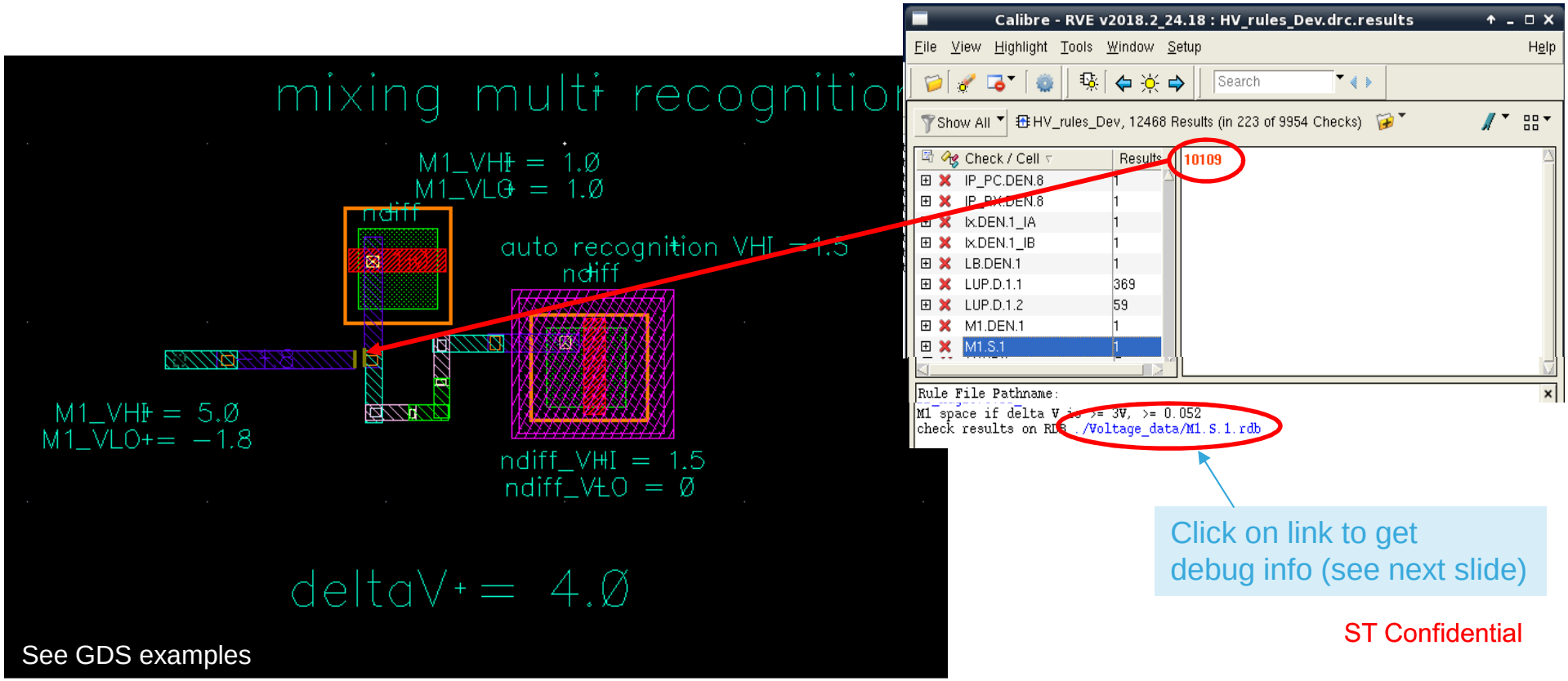


Each RX/PC/MX/LB Metal shape in the design has its VL/VH values stored within RDB file

How to Debug Voltage Rules? (3/4)

- DRM rule using “deltaV” wording as below example:
  Mx distance to (ViaBelow, ViaAbove) if delta V is >= 3V, for x=1-7.

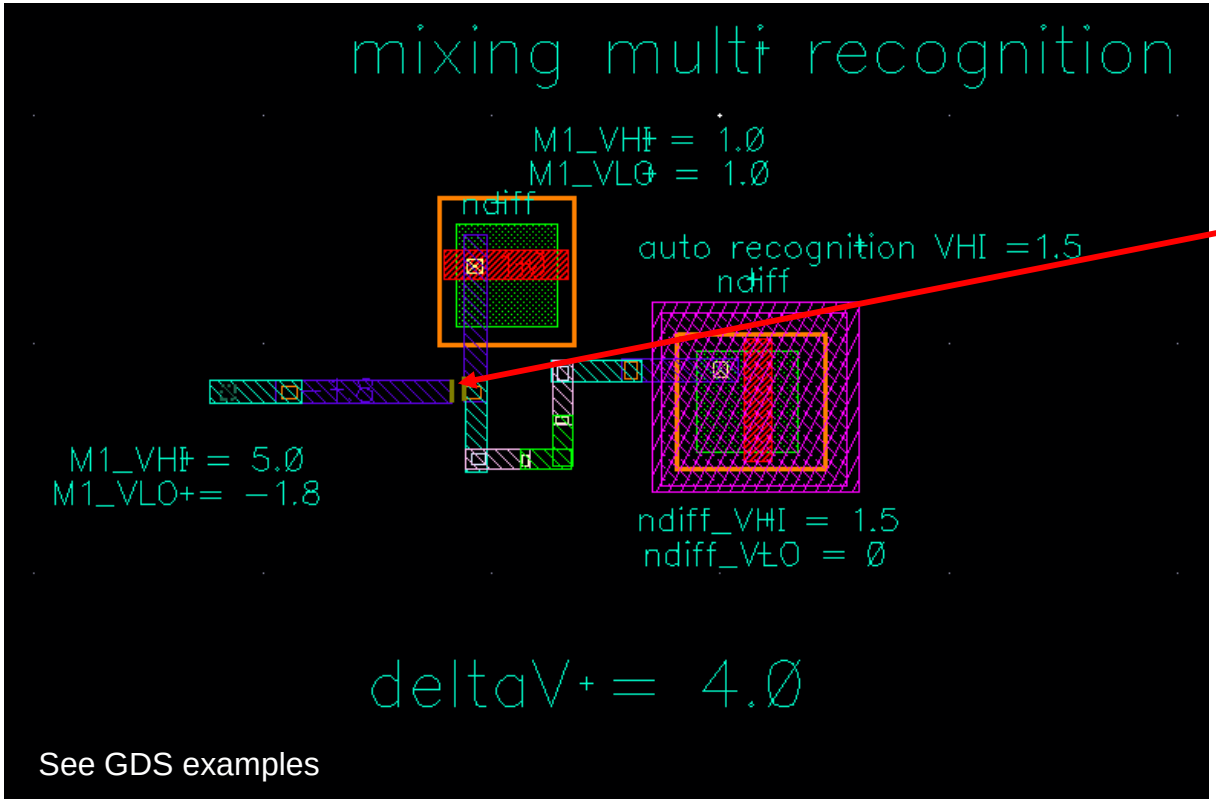
- DRC rule is including RDB file which is indicated voltage information detected, as well as corresponding deltaV which has been measured:



How to Debug Voltage Rules? (4/4)

- DRM rule using “deltaV” wording as below example:
  Mx space if delta V is >= 3V

- DRC rule is including RDB file which is indicated voltage information detected, as well as corresponding deltaV which has been measured:



See GDS examples

```
FIRST_VMIN -1.8
FIRST_VMAX 5
SECOND_VMIN 1
SECOND_VMAX 1
DELTA_V 4
SYNC 0
```

Delta V = MAX {ABS(Net 1 Voltage High – Net 2 Voltage Low); ABS(Net 2 Voltage High – Net 1 Voltage Low)}

life.augmented