Inactive Patterns Cell Application Note

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1 Introduction

The 28nm-FDSOI Process Design Kit provides following devices for mask preparation and layout finishing:

- A standard sealring pcell
- A sealring with crack detector pcell
- A pgtext pcell
- A STlogo pcell

All these devices are available in the LayoutFinishing category of ST_C32_addon_DP library.

2 Devices for Layout Finishing

2.1 Sealring

The sealring or the crack-stop is a resistant die structure blocking cracks, potentially generated in the scribe lane during the sawing, from propagating into the die.

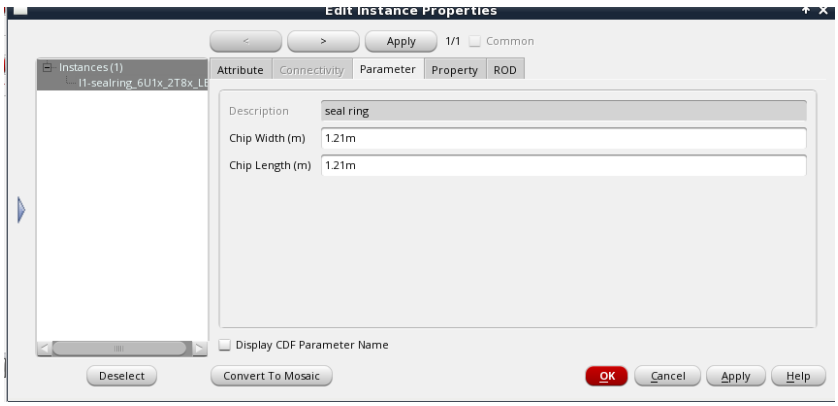
The provided sealring in the design kit is a pcell (i.e parametrized cell) that can be used by the usual "Create Instance" of Virtuoso. There are two versions of sealring: one with crack detector and one without crack detector. It is important to use one of these two pcell without modification.

Please refer to the Design Rules Manual regarding the placement of the sealring around the Chip

2.1.1 Sealring without crack detector

- Pcell name: *sealring_6U1x_2U2x_2T8x_LB, sealring_6U1x_2T8x_LB*
- Category: *LayoutFinishing*

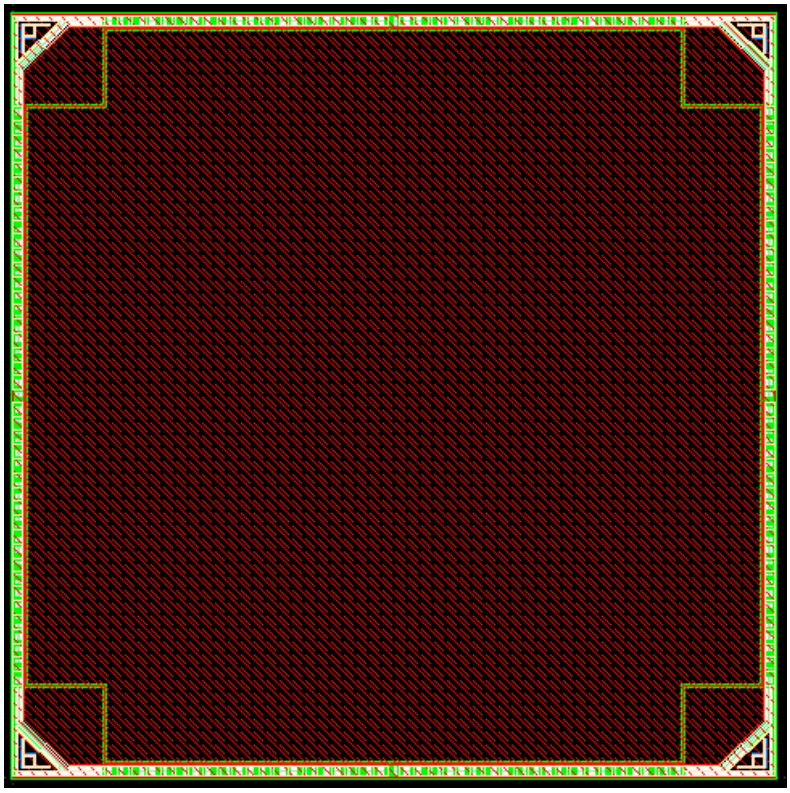
2.1.1.1 Pcell parameters:



The following parameters are available for the sealring PCell:

- **Chip Width**: internal dimensions of the ring in vertical direction, a callback round the value to be integer, in order that the external dimensions are integers too (DRC rule). that means the total sealring in X axis direction = Chip Width + 2 * 24µm.

- **Chip Length**: dimension in horizontal direction, a callback round the value to be integer, in order that the external dimensions are integers too (DRC rule). that means the total sealring in Y axis direction = Chip Length + 2 * 24µm.

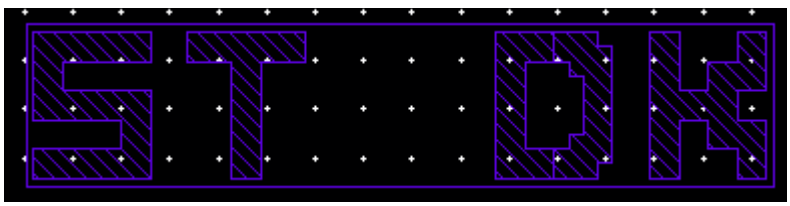


2.1.2 Sealring with crack detector

Please refer to the dedicated documentation available in
$DKITROOT/doc/MANUALS/DESIGN_FINISHING/SEALRING/SealringCS_28FD_AN.pdf

2.2 PGText

The 28nm-FDSOI Process Design-Kit provides the following Pcell for PGtext:



It allows to write letters and digits in layout view, in a single metal layer and cover it by LOGOBND layer as specified in the 28nm-FDSOI Design Rule Manual. The metal layer can be changed. The default is M1 drawing.

2.3 **Logo, copyright and year**

Logo, Copyright and Year are inactive patterns to be added inside the die.
The STLogo pcell is dedicated for the three patterns (Logo of ST, Copyright and Year) with appropriate parameters to change the year and the used Metal. Default metal is IB.
The LOGOBND layer is automatically added by the pcell around the created layout logo, copyright and year patterns.