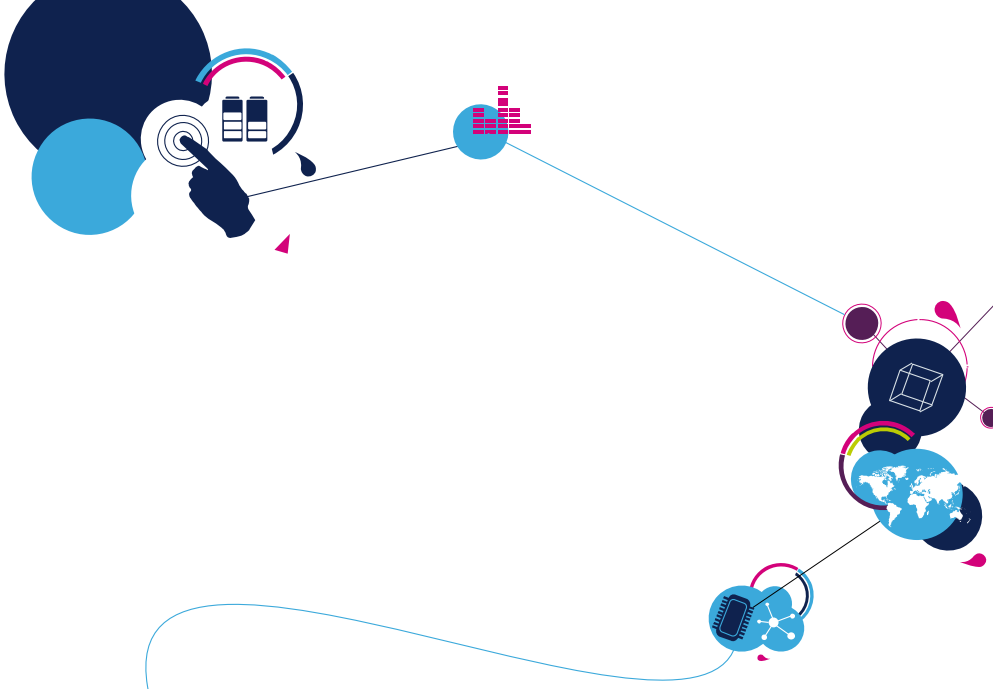

FDSOI – C028FDSOI

Spice Models

ESD UltraLowCap protections documentation

Model Maturity:	*Preliminary*
Design Kit Release:	*DK1.2_RF_mmW*
Document Revision:	*1.1*

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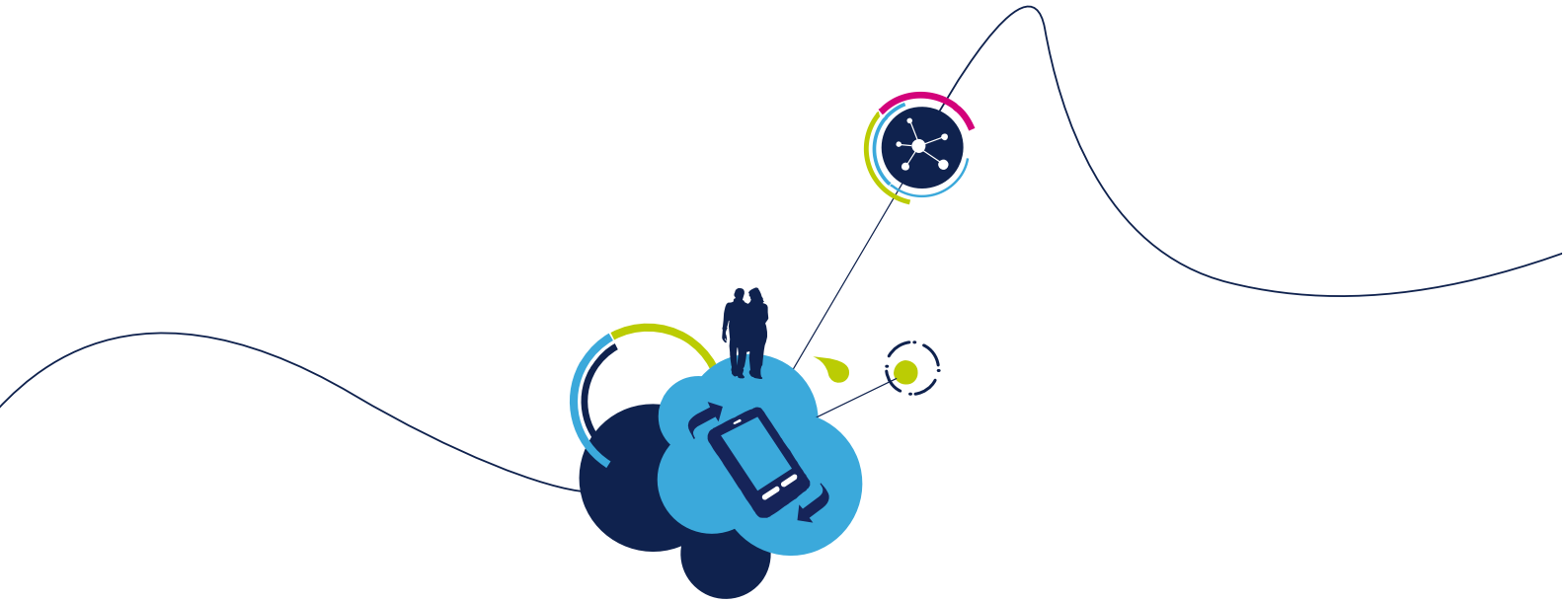

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USER'S MANUAL PURPOSE

The document provides information concerning the C028FDSOI Spice Models - ESD protection UltraLowCap from device description to physics.

DOCUMENT REVISION HISTORY

Date	Revision	Revision information
June, 2018	*1.0*	*First release*
September, 2018	*1.1*	*Update of DC and AC*

AUTHORS

Revision	***Author***
1.0	*DELMAS Antoine*
1.1	*DELMAS Antoine*

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GENERAL INFORMATION

1. SCOPE

This documentation contains the following types of information:

- Model features and limitations
- Conditions used for device characterization or model extraction
- Model-to-Hardware correlation plots

The version of the models referred in this documentation is C028FDSOI Spice Models – esd_ulc_rvt and esd_ulc_eg protection devices V 0.1 unless otherwise specified.

2. ADDITIONAL REFERENCES

Other modelling information can also be found in the following sources:

- Model syntax, input parameter options and basic topology diagrams are included
- Device performance specifications
- Circuit simulator manuals. For ELDO, HSPICE or SPECTRE users, please see the associated user manuals.

3. SIMULATION APPROACH

Ultra low cap models are built using mainly standard diodes, bipolar transistors and ESD MOSFET.

4. STATISTICS

The model has dedicated statistics (pre-defined corners) in order to take into account process variations of devices features.

Pre-defined Corners	
Name	Description
TT	Typical performances
ESDBC	Best performances
ESDWC	Worst performances

Table 1 : Pre-defined corners

5. SOA

SOA (Safe Operating Area) are included with the models. SOA libraries are used to alert the user if the device is used out of its operating area. SOAs are activated by default but be deactivated by changing the soa value to 0.

6. NOTES ON CIRCUIT SIMULATORS

The default numerical error controls may be different between simulators, which could affect accuracy of some circuit not others. User may try to tighten error controls if simulation results difference is noticeable.

MODELS OVERVIEW

1. MODEL STATUS

The UltraLowCap ESD protection device model described in this document is ***preliminary***.

This section gives a summary about the model with its instance parameters and associated features.

Cellname in DK	Model name	Maturity	Release	Model features								
				Process variations			Mismatch			Post-Layout		
										LPE		
				Pre-defined corners	User-defined corners	Statistical models	Pre-defined corners	User-defined corners	Monte carlo	Resistance	Capacitance	SOA
esd_ulc_rvt	esd_ulc_rvt	Preliminary	0.1	✓								✓
esd_ulc_eg	esd_ulc_eg	Preliminary	0.1	✓								✓

Table 2 : Model Status

2. INSTANCE PARAMETERS

Instance parameters					Unit
Name	Description	Value			
		min	default	max	

ncell	Number of cells (merged NWell/T3)	1	1	4	NA
mult	Multiplication factor	1	1	no	NA
soa	Soa flag	0	1	1	NA

Table 3 : Instance parameters

3. DEVICE DESCRIPTION

3.1. DEVICE DESCRIPTION

Ultra low cap are bidirectional ESD devices used for point to point protection (PPP). They are triacs (two interlocked SCRs), with two separated PWell, isolation NWell being used as a gate. Triggering circuit is made up of two ESD MOS, connected in BiMOS configuration, i.e. with gate connected to PWell, and drain connected to NWell gate. When an ESD applied to the device, ESD MOS trigger and inject current into the gate (NWell), thus triggering the triac.

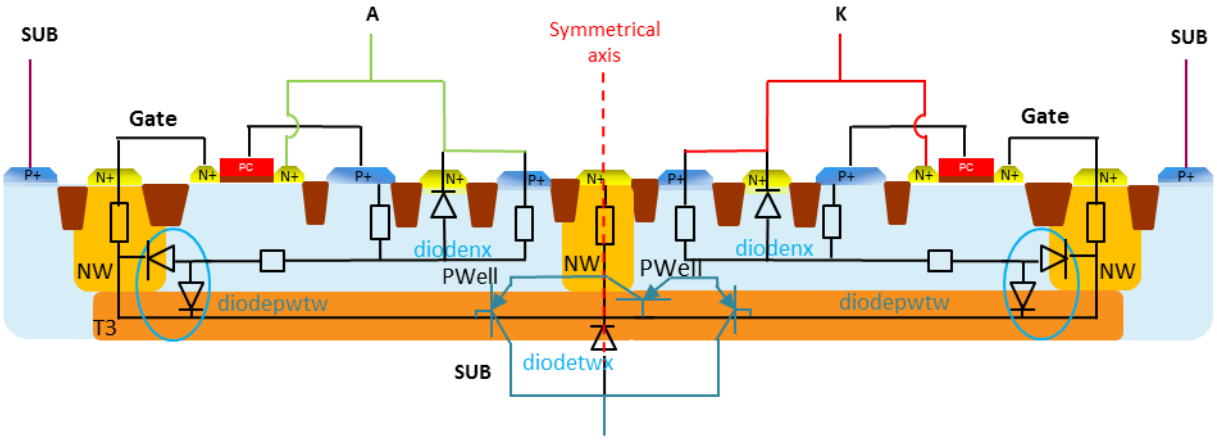

Figure 1 : Cross section of Ultra_Low cap devices

MULT: mult is a simple multiplication factor, which multiplies all dimensions equally.
NCELL: ncell allows the instantiation of up to 4 cells in parallel, with merged NWell/T3.

3.2. MODELS DESCRIPTION

Present model covers DC and AC application. A simple model featuring standard diodes, PNP bipolar transistors, ESD MOSFETs and resistors is presented on Fig. 1.
Two flavours are covered: RVT and EG, with corresponding MOS.

The Ultra low cap ESD Protection models include:

- Standard junction diodes, bipolar and MOSFET equations for IV and CV characteristics.
- Temperature influence (ambient).
- Corners
- Substrate current.

4. SIMULATIONS

In this section, some DC and AC simulations are shown. AC characteristics were obtained by S-parameter measurements on a network analyser. An artefact is observed from 65 GHz to 80 GHz, which should not be taken into account.

4.1. ESD_ULC_RVT

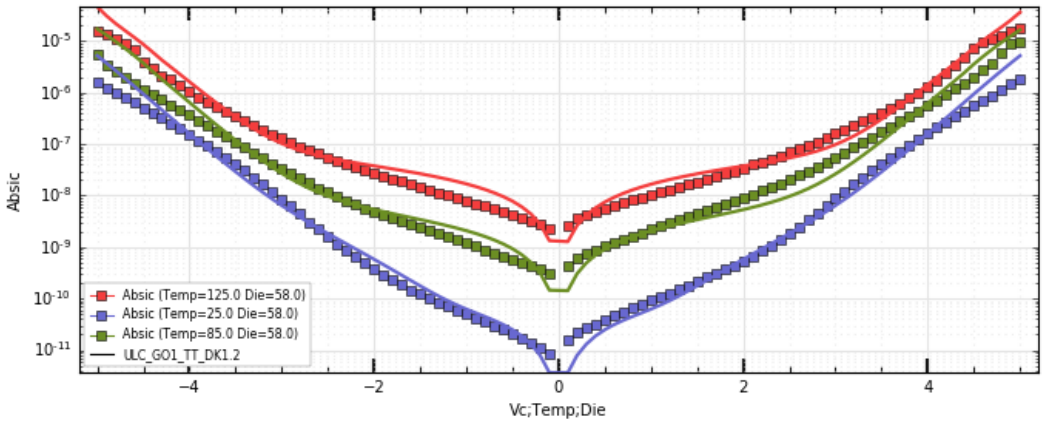

Figure 2 : DC characteristic of RVT ultra low cap devices

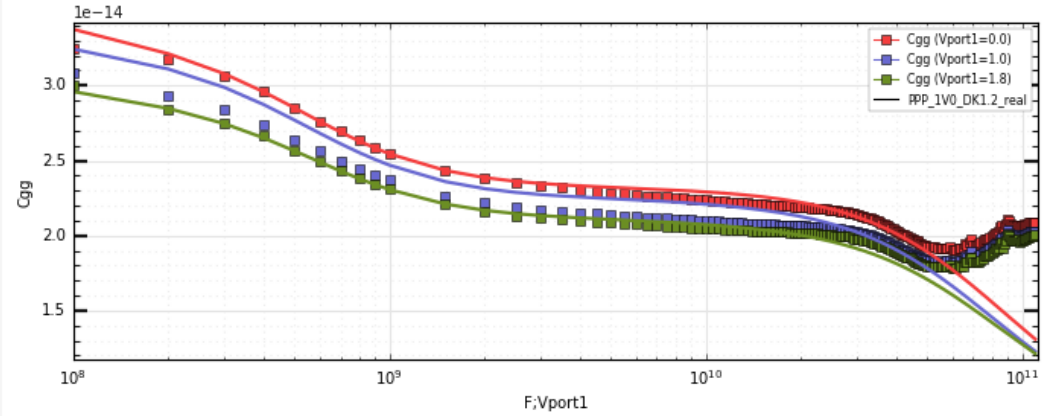

Figure 3 : AC characteristic of RVT ultra low cap devices

4.2. ESD_ULC_EG

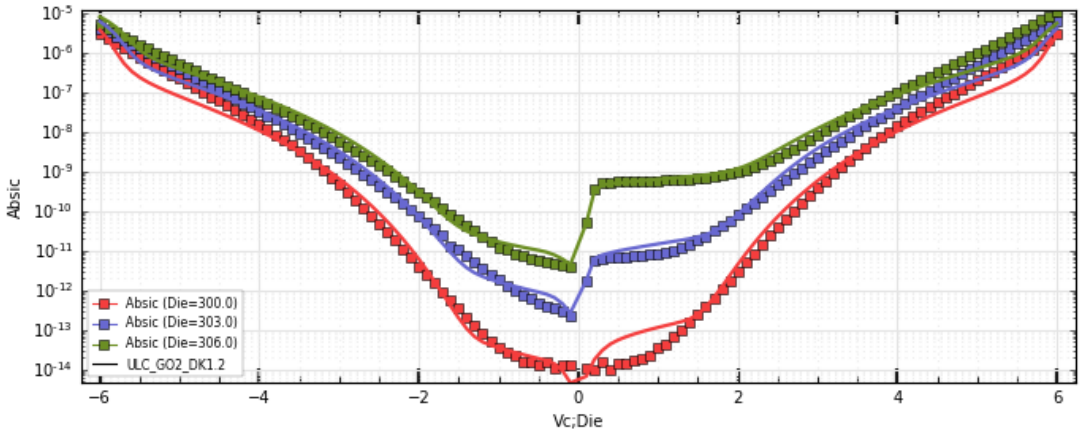

Figure 4 : DC characteristic of EG ultra low cap devices

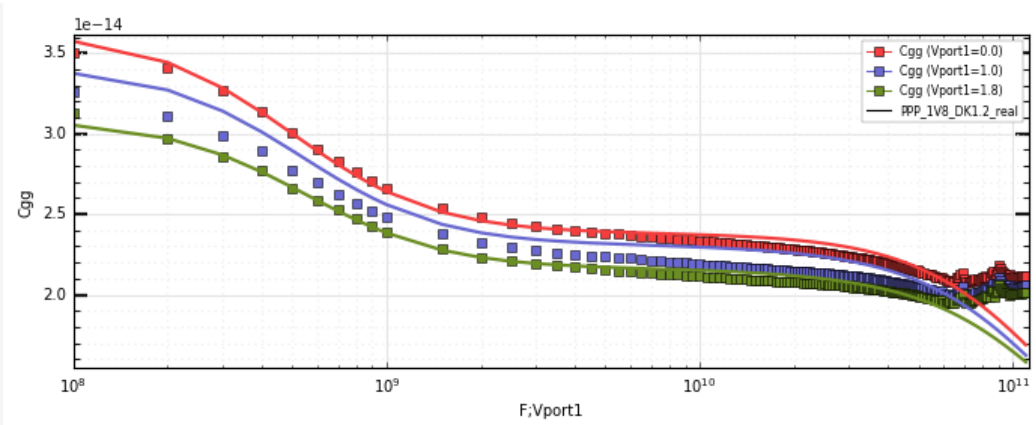

Figure 5 : AC characteristic of EG ultra low cap devices