C28SOI_SC_12_COREPBP16_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 16 nm

Overview

- C28SOI_SC_12_COREPBP16_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

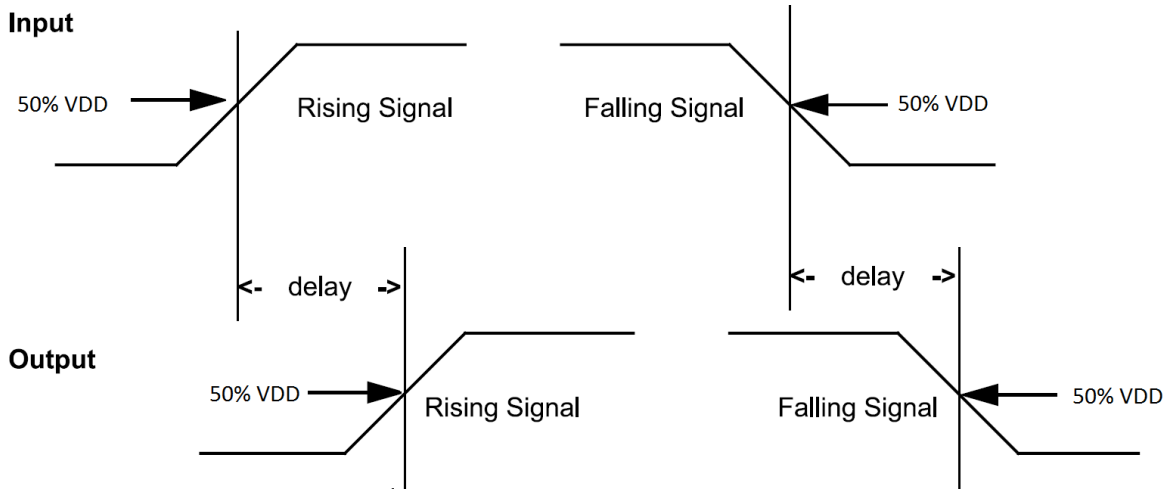


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

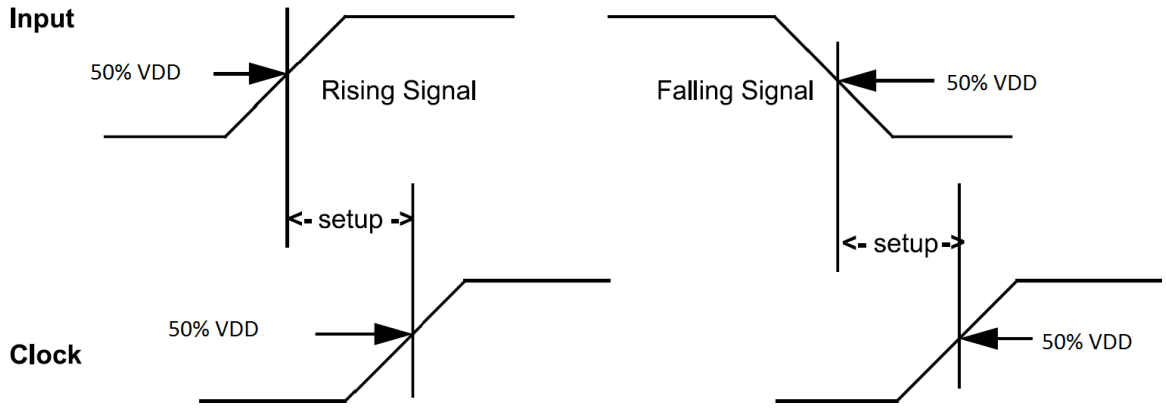


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

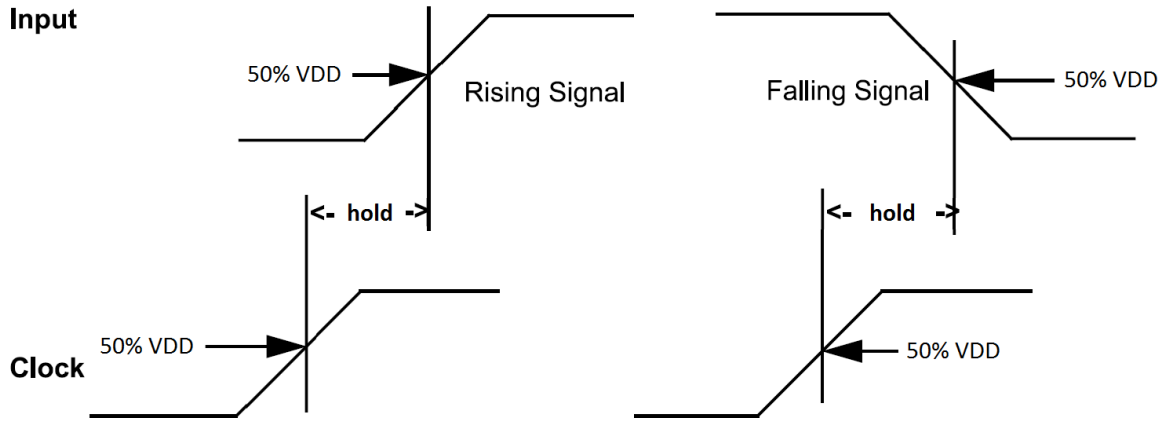


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

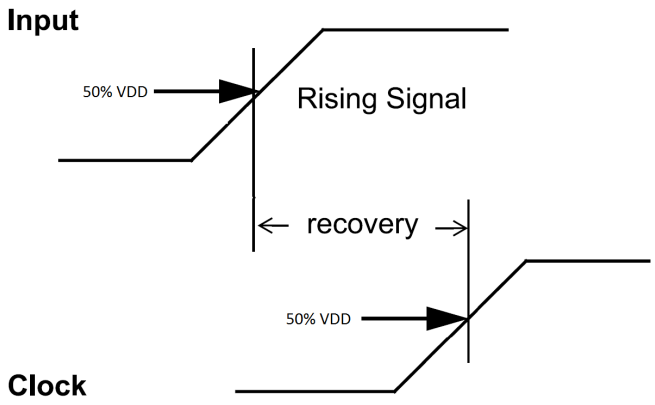


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

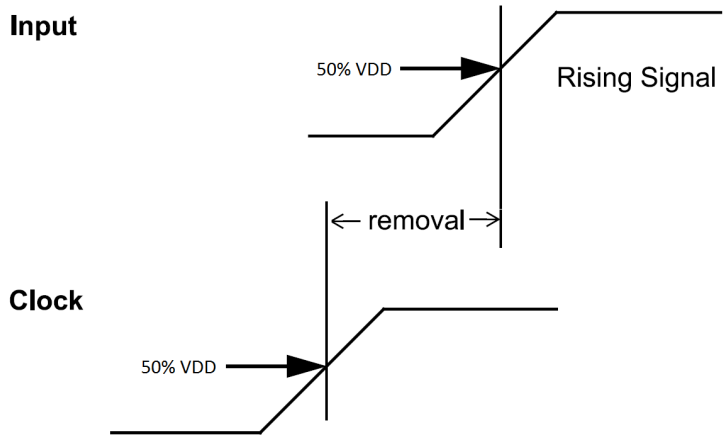


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

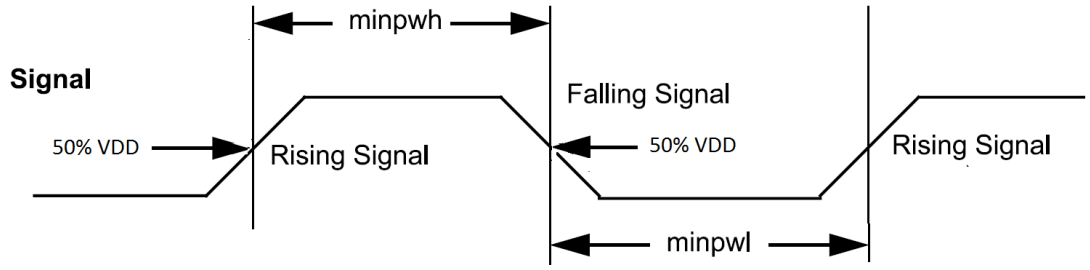


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

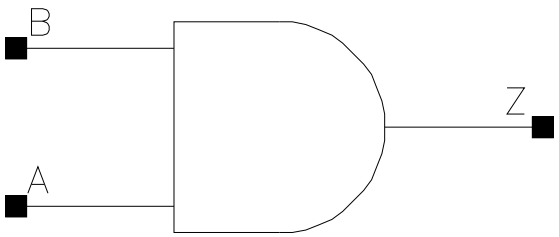
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X25_P16	1.200	1.088	1.3056
X33_P16	1.200	1.360	1.6320
X42_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0009	0.0013	0.0019	0.0024
B	0.0007	0.0012	0.0018	0.0024
	X42_P16			
A	0.0023			
B	0.0024			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0341	0.0281	1.9310	0.9803
A to Z ↑	0.0272	0.0256	2.9940	1.4515
B to Z ↓	0.0323	0.0264	1.9297	0.9804
B to Z ↑	0.0289	0.0269	2.9946	1.4517
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0290	0.0280	0.6508	0.4834

A to Z ↑	0.0252	0.0260	0.9569	0.7233
B to Z ↓	0.0275	0.0255	0.6506	0.4825
B to Z ↑	0.0266	0.0265	0.9574	0.7235
	X42_P16		**X42_P16**	
A to Z ↓	0.0302		0.3930	
A to Z ↑	0.0284		0.5795	
B to Z ↓	0.0279		0.3928	
B to Z ↑	0.0291		0.5792	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	2.174e-07	1.000e-20
X16_P16	4.449e-07	1.000e-20
X25_P16	6.605e-07	1.000e-20
X33_P16	9.097e-07	1.000e-20
X42_P16	1.050e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	1.100e-05	2.062e-05	3.152e-05	6.410e-05
B (output stable)	4.338e-05	8.167e-05	1.258e-04	4.180e-04
A to Z	2.602e-03	4.291e-03	6.657e-03	8.740e-03
B to Z	2.444e-03	4.006e-03	6.222e-03	7.842e-03
	X42_P16			
A (output stable)	6.494e-05			
B (output stable)	4.176e-04			
A to Z	1.050e-02			
B to Z	9.606e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

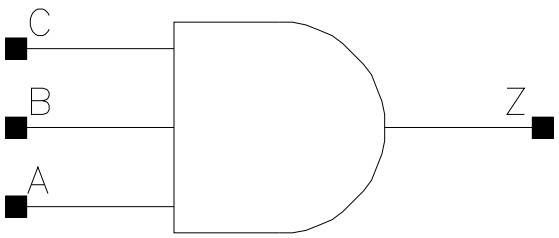
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X25_P16	1.200	1.360	1.6320
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0008	0.0012	0.0020	0.0024
B	0.0007	0.0012	0.0018	0.0023
C	0.0007	0.0012	0.0017	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0368	0.0307	1.9527	0.9554
A to Z ↑	0.0348	0.0326	3.0252	1.4376
B to Z ↓	0.0356	0.0293	1.9505	0.9540
B to Z ↑	0.0354	0.0332	3.0257	1.4375
C to Z ↓	0.0338	0.0277	1.9510	0.9538
C to Z ↑	0.0366	0.0336	3.0240	1.4378
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0311	0.0295	0.6575	0.4908

A to Z ↑	0.0321	0.0310	0.9849	0.7380
B to Z ↓	0.0298	0.0281	0.6563	0.4904
B to Z ↑	0.0328	0.0317	0.9850	0.7373
C to Z ↓	0.0280	0.0265	0.6571	0.4900
C to Z ↑	0.0334	0.0323	0.9846	0.7368

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	2.232e-07	1.000e-20
X17_P16	4.714e-07	1.000e-20
X25_P16	6.796e-07	1.000e-20
X33_P16	9.260e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	7.153e-06	1.323e-05	1.698e-05	2.435e-05
B (output stable)	3.959e-05	7.932e-05	1.106e-04	1.507e-04
C (output stable)	3.145e-05	5.795e-05	8.424e-05	1.156e-04
A to Z	2.875e-03	4.995e-03	7.299e-03	9.390e-03
B to Z	2.716e-03	4.703e-03	6.873e-03	8.811e-03
C to Z	2.576e-03	4.410e-03	6.432e-03	8.216e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

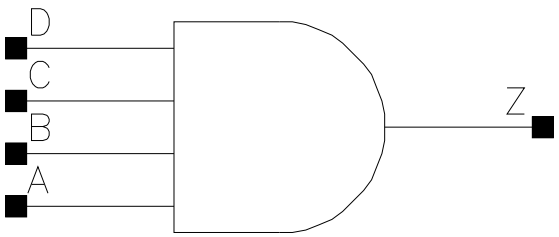
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X6_P16	1.200	1.088	1.3056
X20_P16	1.200	2.312	2.7744
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P16	X6_P16	X20_P16	X27_P16
A	0.0006	0.0009	0.0021	0.0023
B	0.0006	0.0009	0.0021	0.0023
C	0.0005	0.0009	0.0020	0.0023
D	0.0006	0.0009	0.0021	0.0024

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X6_P16	X4_P16	X6_P16
A to Z ↓	0.0387	0.0333	3.6109	2.3623
A to Z ↑	0.0359	0.0286	10.4173	5.5495
B to Z ↓	0.0374	0.0312	3.6138	2.3621
B to Z ↑	0.0378	0.0297	10.4253	5.5534
C to Z ↓	0.0397	0.0352	3.5811	2.3786
C to Z ↑	0.0352	0.0278	10.4337	5.5643

D to Z ↓	0.0384	0.0326	3.5835	2.3778
D to Z ↑	0.0378	0.0291	10.4416	5.5615
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0324	0.0301	0.6915	0.4891
A to Z ↑	0.0300	0.0333	1.8570	1.4117
B to Z ↓	0.0296	0.0277	0.6906	0.4886
B to Z ↑	0.0304	0.0339	1.8578	1.4119
C to Z ↓	0.0314	0.0289	0.6960	0.4916
C to Z ↑	0.0265	0.0289	1.8591	1.4119
D to Z ↓	0.0284	0.0267	0.6951	0.4913
D to Z ↑	0.0267	0.0295	1.8589	1.4120

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	1.518e-07	1.000e-20
X6_P16	3.207e-07	1.000e-20
X20_P16	9.835e-07	1.000e-20
X27_P16	1.256e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	4.737e-04	7.394e-04	2.204e-03	2.699e-03
B (output stable)	4.402e-04	6.681e-04	1.917e-03	2.414e-03
C (output stable)	4.477e-04	7.359e-04	1.913e-03	2.358e-03
D (output stable)	4.163e-04	6.596e-04	1.647e-03	2.050e-03
A to Z	1.917e-03	2.985e-03	9.093e-03	1.170e-02
B to Z	1.819e-03	2.783e-03	8.250e-03	1.084e-02
C to Z	1.844e-03	2.935e-03	7.565e-03	9.440e-03
D to Z	1.746e-03	2.719e-03	6.701e-03	8.586e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

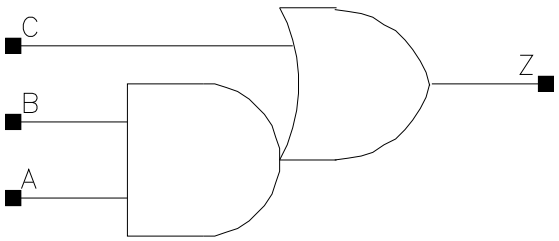
Pin Cycle (vdds)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0011	0.0023
B	0.0007	0.0012	0.0022
C	0.0008	0.0013	0.0023

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0427	0.0382	1.9862	0.9743
A to Z ↑	0.0280	0.0256	2.9067	1.4242
B to Z ↓	0.0394	0.0351	1.9830	0.9712
B to Z ↑	0.0300	0.0274	2.9071	1.4239
C to Z ↓	0.0418	0.0374	1.9782	0.9703
C to Z ↑	0.0261	0.0249	2.8859	1.4149
	X33_P16		**X33_P16**	
A to Z ↓	0.0383		0.4946	
A to Z ↑	0.0262		0.7187	

B to Z ↓	0.0354		0.4943	
B to Z ↑	0.0274		0.7179	
C to Z ↓	0.0376		0.4935	
C to Z ↑	0.0246		0.7136	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	2.264e-07	1.000e-20
X17_P16	4.605e-07	1.000e-20
X33_P16	9.209e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	6.125e-06	1.162e-05	2.995e-05
B (output stable)	2.543e-05	4.046e-05	1.389e-04
C (output stable)	5.961e-05	1.010e-04	2.311e-04
A to Z	2.652e-03	4.566e-03	9.128e-03
B to Z	2.493e-03	4.267e-03	8.395e-03
C to Z	2.957e-03	5.094e-03	1.015e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

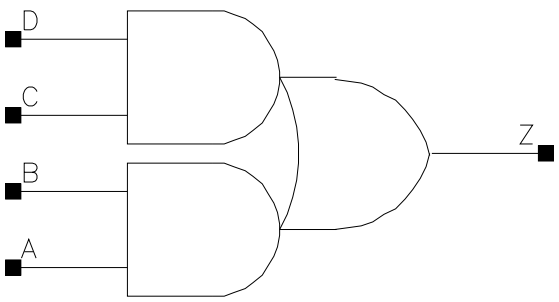
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0011	0.0023
B	0.0008	0.0012	0.0021
C	0.0007	0.0011	0.0023
D	0.0008	0.0012	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0485	0.0422	1.9168	0.9660
A to Z ↑	0.0357	0.0329	2.8698	1.4255
B to Z ↓	0.0451	0.0391	1.9115	0.9636
B to Z ↑	0.0369	0.0344	2.8703	1.4256

C to Z ↓	0.0439	0.0388	1.9101	0.9629
C to Z ↑	0.0302	0.0278	2.8644	1.4210
D to Z ↓	0.0417	0.0366	1.9066	0.9615
D to Z ↑	0.0325	0.0296	2.8629	1.4211
	X33_P16		**X33_P16**	
A to Z ↓	0.0407		0.4954	
A to Z ↑	0.0302		0.7217	
B to Z ↓	0.0384		0.4953	
B to Z ↑	0.0323		0.7216	
C to Z ↓	0.0373		0.4941	
C to Z ↑	0.0262		0.7193	
D to Z ↓	0.0350		0.4940	
D to Z ↑	0.0278		0.7191	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	2.757e-07	1.000e-20
X17_P16	5.606e-07	1.000e-20
X33_P16	1.075e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	3.419e-05	5.195e-05	6.993e-05
B (output stable)	6.139e-05	9.089e-05	1.083e-04
C (output stable)	9.958e-06	2.080e-05	3.799e-05
D (output stable)	2.951e-05	5.646e-05	1.139e-04
A to Z	3.535e-03	5.919e-03	1.112e-02
B to Z	3.250e-03	5.469e-03	1.048e-02
C to Z	2.952e-03	4.968e-03	9.205e-03
D to Z	2.808e-03	4.688e-03	8.622e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

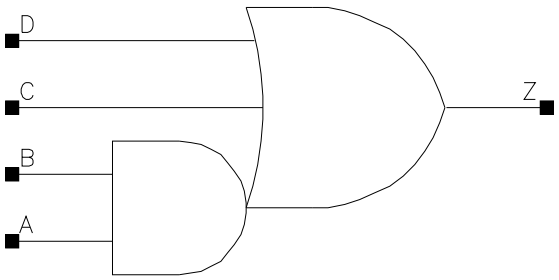
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	0.952	1.1424
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0011	0.0021
B	0.0007	0.0011	0.0021
C	0.0008	0.0011	0.0022
D	0.0007	0.0011	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0552	0.0483	2.0808	1.0301
A to Z ↑	0.0301	0.0277	2.8951	1.4832
B to Z ↓	0.0524	0.0449	2.0777	1.0291
B to Z ↑	0.0323	0.0292	2.8992	1.4827
C to Z ↓	0.0577	0.0502	2.0736	1.0278
C to Z ↑	0.0281	0.0265	2.8739	1.4725

D to Z ↓	0.0571	0.0502	2.0744	1.0280
D to Z ↑	0.0277	0.0263	2.8744	1.4711
	X33_P16		**X33_P16**	
A to Z ↓	0.0493		0.5157	
A to Z ↑	0.0279		0.7196	
B to Z ↓	0.0440		0.5140	
B to Z ↑	0.0287		0.7194	
C to Z ↓	0.0521		0.5138	
C to Z ↑	0.0262		0.7155	
D to Z ↓	0.0506		0.5141	
D to Z ↑	0.0252		0.7138	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	2.204e-07	1.000e-20
X17_P16	4.459e-07	1.000e-20
X33_P16	9.053e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	3.200e-06	6.450e-06	2.819e-05
B (output stable)	9.210e-06	1.781e-05	7.622e-05
C (output stable)	1.221e-04	2.101e-04	5.980e-04
D (output stable)	7.105e-06	1.098e-05	2.876e-05
A to Z	2.916e-03	4.908e-03	9.865e-03
B to Z	2.775e-03	4.603e-03	8.955e-03
C to Z	3.400e-03	5.750e-03	1.179e-02
D to Z	3.188e-03	5.385e-03	1.076e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

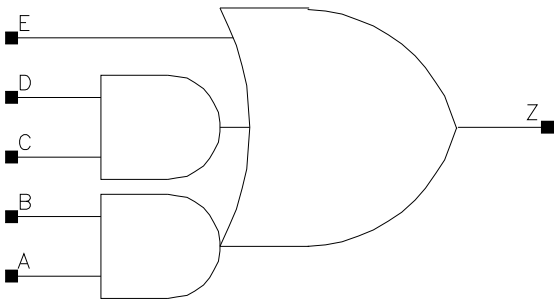
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.088	1.3056
X17_P16	1.200	1.224	1.4688
X33_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0011	0.0022
B	0.0007	0.0011	0.0021
C	0.0008	0.0013	0.0022
D	0.0007	0.0011	0.0021
E	0.0007	0.0011	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0677	0.0581	1.9869	0.9998
A to Z ↑	0.0375	0.0330	2.8449	1.4345

B to Z ↓	0.0650	0.0551	1.9829	0.9978
B to Z ↑	0.0403	0.0352	2.8446	1.4341
C to Z ↓	0.0574	0.0507	1.9777	0.9956
C to Z ↑	0.0318	0.0278	2.8204	1.4250
D to Z ↓	0.0533	0.0461	1.9701	0.9917
D to Z ↑	0.0339	0.0295	2.8223	1.4245
E to Z ↓	0.0595	0.0512	1.9679	0.9922
E to Z ↑	0.0294	0.0261	2.7941	1.4132
	X33_P16		**X33_P16**	
A to Z ↓	0.0573		0.5151	
A to Z ↑	0.0341		0.7247	
B to Z ↓	0.0537		0.5146	
B to Z ↑	0.0360		0.7252	
C to Z ↓	0.0488		0.5131	
C to Z ↑	0.0279		0.7192	
D to Z ↓	0.0449		0.5118	
D to Z ↑	0.0295		0.7190	
E to Z ↓	0.0501		0.5118	
E to Z ↑	0.0261		0.7133	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	2.765e-07	1.000e-20
X17_P16	5.504e-07	1.000e-20
X33_P16	1.041e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.267e-05	3.804e-05	8.599e-05
B (output stable)	5.854e-05	6.574e-05	1.610e-04
C (output stable)	1.344e-05	1.774e-05	4.433e-05
D (output stable)	1.428e-05	2.887e-05	7.166e-05
E (output stable)	9.329e-05	1.006e-04	2.732e-04
A to Z	4.078e-03	6.575e-03	1.302e-02
B to Z	3.943e-03	6.263e-03	1.223e-02
C to Z	3.159e-03	5.156e-03	9.990e-03
D to Z	2.994e-03	4.827e-03	9.264e-03
E to Z	3.503e-03	5.648e-03	1.097e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

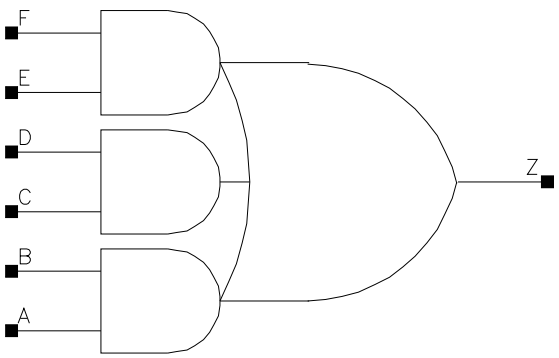
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.360	1.6320
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
A	0.0007	0.0008	0.0011	0.0022

B	0.0007	0.0009	0.0014	0.0020
C	0.0007	0.0008	0.0011	0.0021
D	0.0007	0.0008	0.0011	0.0020
E	0.0007	0.0009	0.0011	0.0022
F	0.0007	0.0008	0.0011	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0673	0.0640	3.7574	1.9820
A to Z ↑	0.0396	0.0384	5.7515	2.9026
B to Z ↓	0.0618	0.0592	3.7400	1.9730
B to Z ↑	0.0406	0.0397	5.7488	2.9027
C to Z ↓	0.0613	0.0588	3.7461	1.9775
C to Z ↑	0.0356	0.0344	5.7149	2.8840
D to Z ↓	0.0582	0.0559	3.7361	1.9715
D to Z ↑	0.0381	0.0369	5.7128	2.8823
E to Z ↓	0.0512	0.0503	3.7282	1.9681
E to Z ↑	0.0302	0.0293	5.6870	2.8707
F to Z ↓	0.0475	0.0468	3.7186	1.9626
F to Z ↑	0.0320	0.0312	5.6903	2.8716
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
A to Z ↓	0.0615	0.0595	1.0020	0.5137
A to Z ↑	0.0362	0.0365	1.4392	0.7282
B to Z ↓	0.0579	0.0562	0.9969	0.5132
B to Z ↑	0.0384	0.0384	1.4388	0.7279
C to Z ↓	0.0575	0.0555	0.9996	0.5132
C to Z ↑	0.0327	0.0337	1.4310	0.7239
D to Z ↓	0.0541	0.0525	0.9963	0.5127
D to Z ↑	0.0350	0.0356	1.4311	0.7237
E to Z ↓	0.0491	0.0498	0.9949	0.5116
E to Z ↑	0.0278	0.0293	1.4255	0.7218
F to Z ↓	0.0457	0.0461	0.9920	0.5102
F to Z ↑	0.0297	0.0312	1.4254	0.7218

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	2.397e-07	1.000e-20
X8_P16	3.744e-07	1.000e-20
X17_P16	6.394e-07	1.000e-20
X33_P16	1.196e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	7.022e-05	8.468e-05	1.021e-04	2.029e-04
B (output stable)	2.059e-04	2.370e-04	2.768e-04	5.059e-04
C (output stable)	3.255e-05	3.962e-05	5.157e-05	8.189e-05
D (output stable)	4.669e-05	5.815e-05	7.337e-05	1.425e-04
E (output stable)	2.903e-05	3.224e-05	3.906e-05	5.771e-05
F (output stable)	3.372e-05	4.050e-05	5.648e-05	1.135e-04

A to Z	3.715e-03	4.897e-03	7.376e-03	1.413e-02
B to Z	3.408e-03	4.536e-03	6.908e-03	1.334e-02
C to Z	3.121e-03	4.184e-03	6.433e-03	1.230e-02
D to Z	2.974e-03	3.997e-03	6.126e-03	1.161e-02
E to Z	2.477e-03	3.455e-03	5.350e-03	1.061e-02
F to Z	2.324e-03	3.255e-03	5.042e-03	9.917e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

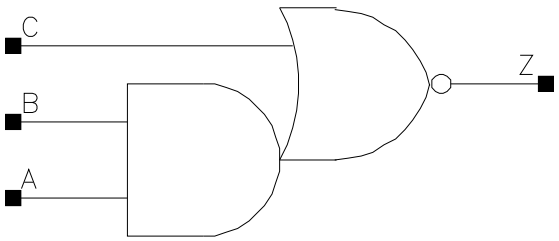
Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008
X44_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X33_P16	X44_P16
A	0.0009	0.0027	0.0054	0.0073
B	0.0009	0.0025	0.0050	0.0066
C	0.0010	0.0029	0.0056	0.0074

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0111	0.0118	3.4921	1.1859
A to Z ↑	0.0191	0.0196	5.6862	1.9051
B to Z ↓	0.0112	0.0116	3.5326	1.2026
B to Z ↑	0.0154	0.0153	5.6106	1.9068
C to Z ↓	0.0119	0.0122	1.9859	0.6826
C to Z ↑	0.0200	0.0200	5.1833	1.7517
	X33_P16	**X44_P16**	**X33_P16**	**X44_P16**
A to Z ↓	0.0121	0.0121	0.6033	0.4584

A to Z ↑	0.0196	0.0197	0.9530	0.7235
B to Z ↓	0.0115	0.0115	0.6119	0.4649
B to Z ↑	0.0152	0.0151	0.9521	0.7206
C to Z ↓	0.0136	0.0138	0.4062	0.3163
C to Z ↑	0.0203	0.0202	0.8743	0.6626

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P16	2.175e-07	1.000e-20
X17_P16	6.367e-07	1.000e-20
X33_P16	1.221e-06	1.000e-20
X44_P16	1.608e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	1.196e-05	4.272e-05	9.214e-05	1.216e-04
B (output stable)	4.256e-05	1.906e-04	4.261e-04	5.579e-04
C (output stable)	9.948e-05	3.114e-04	6.845e-04	8.927e-04
A to Z	1.192e-03	3.821e-03	7.720e-03	1.020e-02
B to Z	9.117e-04	2.690e-03	5.349e-03	7.052e-03
C to Z	1.748e-03	5.254e-03	1.069e-02	1.405e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

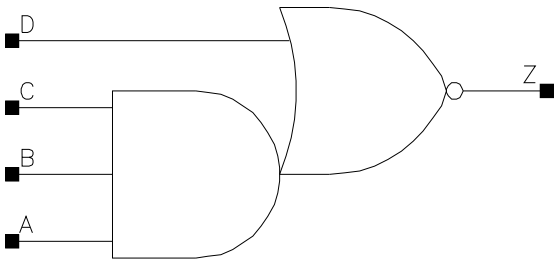
Pin Cycle (vdds)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X29_P16	1.200	3.536	4.2432
X38_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X29_P16	X38_P16
A	0.0010	0.0055	0.0072
B	0.0009	0.0053	0.0069
C	0.0009	0.0050	0.0066
D	0.0010	0.0056	0.0070

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X29_P16	X5_P16	X29_P16
A to Z ↓	0.0163	0.0176	4.9962	0.8657
A to Z ↑	0.0246	0.0246	5.6890	0.9431
B to Z ↓	0.0164	0.0169	5.0143	0.8694
B to Z ↑	0.0218	0.0216	5.6938	0.9505
C to Z ↓	0.0159	0.0156	5.0394	0.8755
C to Z ↑	0.0184	0.0176	5.6204	0.9585
D to Z ↓	0.0141	0.0159	2.0275	0.4092

D to Z ↑	0.0228	0.0233	4.8456	0.8123
	X38_P16		**X38_P16**	
A to Z ↓	0.0173		0.6687	
A to Z ↑	0.0241		0.7111	
B to Z ↓	0.0167		0.6725	
B to Z ↑	0.0212		0.7186	
C to Z ↓	0.0154		0.6768	
C to Z ↑	0.0173		0.7275	
D to Z ↓	0.0167		0.3390	
D to Z ↑	0.0229		0.6136	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.381e-07	1.000e-20
X29_P16	1.345e-06	1.000e-20
X38_P16	1.748e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X29_P16	X38_P16
A (output stable)	1.093e-05	1.042e-04	1.276e-04
B (output stable)	3.271e-05	2.466e-04	3.252e-04
C (output stable)	5.654e-05	5.246e-04	6.782e-04
D (output stable)	4.797e-04	3.813e-03	4.975e-03
A to Z	1.828e-03	1.156e-02	1.475e-02
B to Z	1.541e-03	9.230e-03	1.184e-02
C to Z	1.251e-03	6.845e-03	8.707e-03
D to Z	2.290e-03	1.406e-02	1.810e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

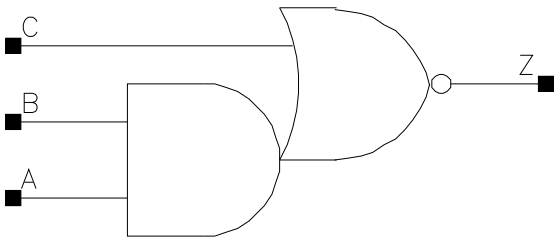
Pin Cycle (vdds)	X5_P16	X29_P16	X38_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X11_P16	1.200	1.088	1.3056
X16_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X11_P16	X16_P16	X23_P16
A	0.0010	0.0020	0.0030	0.0040
B	0.0010	0.0019	0.0028	0.0036
C	0.0010	0.0017	0.0025	0.0036
	X46_P16			
A	0.0076			
B	0.0071			
C	0.0071			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X11_P16	X6_P16	X11_P16
A to Z ↓	0.0136	0.0147	3.3717	1.7146
A to Z ↑	0.0219	0.0230	5.6630	2.7672
B to Z ↓	0.0144	0.0146	3.4063	1.7342

B to Z ↑	0.0190	0.0195	5.5868	2.7756
C to Z ↓	0.0084	0.0089	2.0450	1.2095
C to Z ↑	0.0155	0.0151	5.2144	2.5697
	X16_P16	**X23_P16**	**X16_P16**	**X23_P16**
A to Z ↓	0.0141	0.0145	1.1847	0.8909
A to Z ↑	0.0216	0.0220	1.8620	1.4119
B to Z ↓	0.0145	0.0144	1.1995	0.9009
B to Z ↑	0.0181	0.0183	1.8616	1.4174
C to Z ↓	0.0089	0.0079	0.8408	0.5273
C to Z ↑	0.0145	0.0149	1.7290	1.3116
	X46_P16		**X46_P16**	
A to Z ↓	0.0141		0.4578	
A to Z ↑	0.0213		0.7342	
B to Z ↓	0.0142		0.4630	
B to Z ↑	0.0175		0.7325	
C to Z ↓	0.0083		0.2703	
C to Z ↑	0.0150		0.6806	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P16	2.236e-07	1.000e-20
X11_P16	4.452e-07	1.000e-20
X16_P16	6.301e-07	1.000e-20
X23_P16	8.910e-07	1.000e-20
X46_P16	1.738e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	3.027e-05	8.185e-05	1.022e-04	1.456e-04
B (output stable)	1.347e-04	4.172e-04	4.537e-04	6.504e-04
C (output stable)	5.109e-05	1.381e-04	1.832e-04	2.747e-04
A to Z	1.823e-03	4.006e-03	5.487e-03	7.478e-03
B to Z	1.521e-03	3.179e-03	4.287e-03	5.767e-03
C to Z	9.158e-04	1.867e-03	2.547e-03	3.556e-03
	X46_P16			
A (output stable)	2.561e-04			
B (output stable)	1.065e-03			
C (output stable)	4.094e-04			
A to Z	1.385e-02			
B to Z	1.063e-02			
C to Z	6.721e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

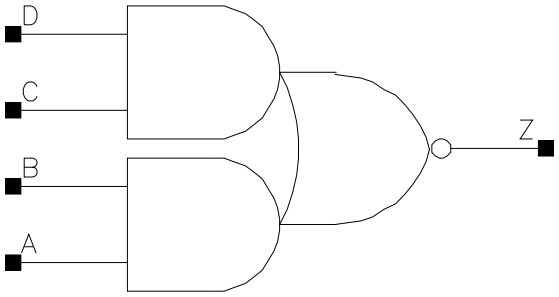
	X46_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P16	X10_P16	X16_P16	X21_P16
A	0.0008	0.0021	0.0030	0.0039
B	0.0008	0.0018	0.0028	0.0036
C	0.0007	0.0019	0.0027	0.0037
D	0.0008	0.0017	0.0025	0.0034
	X42_P16			
A	0.0077			
B	0.0072			
C	0.0072			
D	0.0068			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X10_P16**	**X4_P16**	**X10_P16**
A to Z ↓	0.0152	0.0150	4.1851	1.6496
A to Z ↑	0.0282	0.0239	7.7915	2.5556
B to Z ↓	0.0163	0.0163	4.2278	1.6674
B to Z ↑	0.0252	0.0216	7.7759	2.6198
C to Z ↓	0.0114	0.0109	4.2837	1.6593
C to Z ↑	0.0222	0.0193	7.7950	2.5739
D to Z ↓	0.0118	0.0113	4.3418	1.6836
D to Z ↑	0.0187	0.0163	7.7782	2.6137
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0163	0.0164	1.1904	0.8944
A to Z ↑	0.0249	0.0250	1.7227	1.3345
B to Z ↓	0.0172	0.0168	1.2032	0.9039
B to Z ↑	0.0218	0.0217	1.7224	1.3362
C to Z ↓	0.0119	0.0123	1.1893	0.8948
C to Z ↑	0.0200	0.0206	1.7237	1.3334
D to Z ↓	0.0118	0.0116	1.2079	0.9087
D to Z ↑	0.0163	0.0165	1.7271	1.3367
	X42_P16		**X42_P16**	
A to Z ↓	0.0171		0.4646	
A to Z ↑	0.0253		0.6686	
B to Z ↓	0.0174		0.4694	
B to Z ↑	0.0218		0.6658	
C to Z ↓	0.0128		0.4607	
C to Z ↑	0.0208		0.6697	
D to Z ↓	0.0122		0.4676	
D to Z ↑	0.0168		0.6682	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	1.893e-07	1.000e-20
X10_P16	5.532e-07	1.000e-20
X16_P16	7.905e-07	1.000e-20
X21_P16	1.062e-06	1.000e-20
X42_P16	2.087e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	2.812e-05	6.745e-05	1.250e-04	1.754e-04
B (output stable)	4.633e-05	1.139e-04	2.096e-04	2.901e-04
C (output stable)	1.266e-05	3.744e-05	8.473e-05	1.394e-04
D (output stable)	4.138e-05	1.096e-04	2.922e-04	4.506e-04
A to Z	1.875e-03	4.559e-03	7.202e-03	9.461e-03
B to Z	1.619e-03	3.930e-03	5.990e-03	7.823e-03
C to Z	1.072e-03	2.660e-03	4.240e-03	5.789e-03
D to Z	8.425e-04	2.087e-03	3.104e-03	4.151e-03
	X42_P16			
A (output stable)	3.300e-04			
B (output stable)	5.294e-04			
C (output stable)	2.483e-04			
D (output stable)	8.053e-04			

A to Z	1.863e-02			
B to Z	1.549e-02			
C to Z	1.131e-02			
D to Z	8.273e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

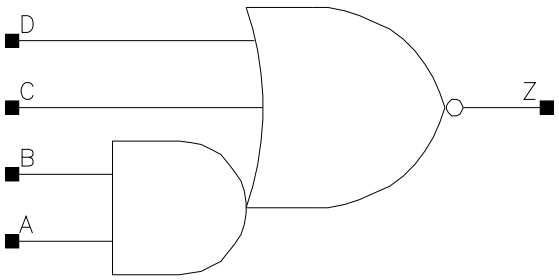
Pin Cycle (vdds)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X35_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P16	X35_P16
A	0.0009	0.0069
B	0.0009	0.0064
C	0.0010	0.0067
D	0.0010	0.0063

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X35_P16	X5_P16	X35_P16
A to Z ↓	0.0129	0.0135	3.5290	0.5202
A to Z ↑	0.0250	0.0235	8.3597	1.0727
B to Z ↓	0.0134	0.0134	3.5696	0.5280
B to Z ↑	0.0206	0.0185	8.3057	1.0727
C to Z ↓	0.0144	0.0182	2.1234	0.4063
C to Z ↑	0.0286	0.0282	7.8764	1.0114
D to Z ↓	0.0137	0.0167	2.1386	0.4056

D to Z ↑	0.0279	0.0264	7.8863	1.0142

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.255e-07	1.000e-20
X35_P16	1.528e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X35_P16
A (output stable)	6.531e-06	7.717e-05
B (output stable)	1.787e-05	2.174e-04
C (output stable)	2.050e-04	2.075e-03
D (output stable)	1.044e-05	1.163e-04
A to Z	1.458e-03	1.052e-02
B to Z	1.174e-03	7.773e-03
C to Z	2.396e-03	1.866e-02
D to Z	2.016e-03	1.464e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

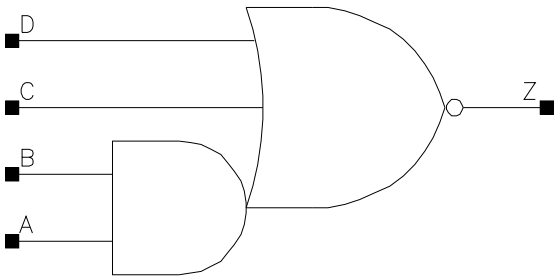
Pin Cycle (vdds)	X5_P16	X35_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X17_P16	1.200	2.448	2.9376
X34_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P16	X17_P16	X34_P16
A	0.0010	0.0039	0.0078
B	0.0009	0.0037	0.0073
C	0.0008	0.0033	0.0064
D	0.0008	0.0030	0.0059

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X17_P16	X4_P16	X17_P16
A to Z ↓	0.0158	0.0172	3.8088	1.0077
A to Z ↑	0.0290	0.0305	8.4034	2.0719
B to Z ↓	0.0172	0.0178	3.8483	1.0177
B to Z ↑	0.0255	0.0260	8.3223	2.0751
C to Z ↓	0.0145	0.0145	3.3417	0.8166
C to Z ↑	0.0212	0.0226	7.9234	1.9633

D to Z ↓	0.0120	0.0109	3.4329	0.8231
D to Z ↑	0.0187	0.0173	7.9662	1.9749
	X34_P16		**X34_P16**	
A to Z ↓	0.0171		0.5166	
A to Z ↑	0.0300		1.0564	
B to Z ↓	0.0179		0.5218	
B to Z ↑	0.0256		1.0524	
C to Z ↓	0.0149		0.4354	
C to Z ↑	0.0220		0.9989	
D to Z ↓	0.0113		0.4403	
D to Z ↑	0.0170		1.0052	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	2.001e-07	1.000e-20
X17_P16	8.012e-07	1.000e-20
X34_P16	1.565e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X17_P16	X34_P16
A (output stable)	3.681e-05	1.707e-04	3.380e-04
B (output stable)	6.036e-05	3.184e-04	6.104e-04
C (output stable)	4.955e-05	4.559e-04	8.225e-04
D (output stable)	1.108e-05	1.312e-04	2.389e-04
A to Z	2.276e-03	9.895e-03	1.914e-02
B to Z	1.996e-03	8.282e-03	1.606e-02
C to Z	1.351e-03	5.943e-03	1.130e-02
D to Z	9.383e-04	3.550e-03	6.749e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

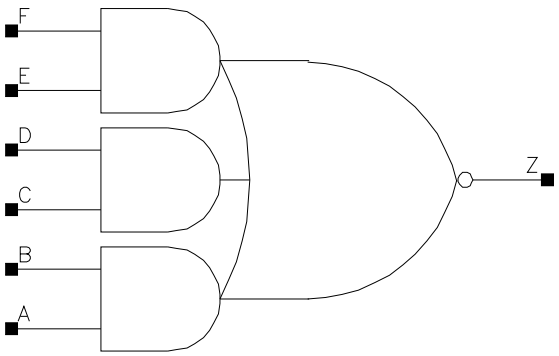
Pin Cycle (vdds)	X4_P16	X17_P16	X34_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X8_P16	1.200	2.176	2.6112
X13_P16	1.200	2.720	3.2640
X17_P16	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P16	X8_P16	X13_P16	X17_P16
A	0.0010	0.0019	0.0030	0.0039

B	0.0009	0.0018	0.0027	0.0035
C	0.0009	0.0019	0.0028	0.0035
D	0.0009	0.0017	0.0025	0.0033
E	0.0011	0.0018	0.0026	0.0034
F	0.0009	0.0016	0.0024	0.0032

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0183	0.0219	3.3851	1.9563
A to Z ↑	0.0411	0.0402	8.0651	3.7386
B to Z ↓	0.0202	0.0229	3.4156	1.9700
B to Z ↑	0.0374	0.0364	8.0577	3.7471
C to Z ↓	0.0166	0.0196	3.3566	1.9706
C to Z ↑	0.0361	0.0362	8.1065	3.7522
D to Z ↓	0.0181	0.0207	3.3962	1.9894
D to Z ↑	0.0323	0.0322	8.0664	3.7522
E to Z ↓	0.0126	0.0149	3.3096	1.9741
E to Z ↑	0.0277	0.0276	8.0409	3.7340
F to Z ↓	0.0132	0.0150	3.3653	2.0030
F to Z ↑	0.0238	0.0231	8.1028	3.7404
	X13_P16	**X17_P16**	**X13_P16**	**X17_P16**
A to Z ↓	0.0210	0.0212	1.3307	1.0145
A to Z ↑	0.0376	0.0378	2.4668	1.8909
B to Z ↓	0.0225	0.0222	1.3396	1.0218
B to Z ↑	0.0341	0.0337	2.4758	1.8915
C to Z ↓	0.0189	0.0189	1.3393	1.0048
C to Z ↑	0.0335	0.0339	2.4804	1.9038
D to Z ↓	0.0202	0.0196	1.3516	1.0145
D to Z ↑	0.0299	0.0298	2.4842	1.8997
E to Z ↓	0.0142	0.0142	1.3362	1.0073
E to Z ↑	0.0259	0.0260	2.4731	1.8896
F to Z ↓	0.0146	0.0139	1.3543	1.0219
F to Z ↑	0.0219	0.0216	2.4789	1.8989

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	3.485e-07	1.000e-20
X8_P16	6.851e-07	1.000e-20
X13_P16	9.796e-07	1.000e-20
X17_P16	1.308e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	1.015e-04	2.291e-04	3.100e-04	4.091e-04
B (output stable)	2.784e-04	6.209e-04	7.843e-04	1.035e-03
C (output stable)	4.653e-05	1.148e-04	1.420e-04	2.005e-04
D (output stable)	6.961e-05	1.953e-04	2.284e-04	3.390e-04
E (output stable)	2.744e-05	7.666e-05	1.005e-04	1.425e-04
F (output stable)	4.598e-05	1.449e-04	1.804e-04	2.701e-04

A to Z	3.621e-03	7.629e-03	1.060e-02	1.403e-02
B to Z	3.301e-03	6.845e-03	9.541e-03	1.242e-02
C to Z	2.690e-03	5.903e-03	7.974e-03	1.061e-02
D to Z	2.394e-03	5.154e-03	6.983e-03	9.128e-03
E to Z	1.706e-03	3.869e-03	5.143e-03	6.832e-03
F to Z	1.423e-03	3.102e-03	4.154e-03	5.357e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

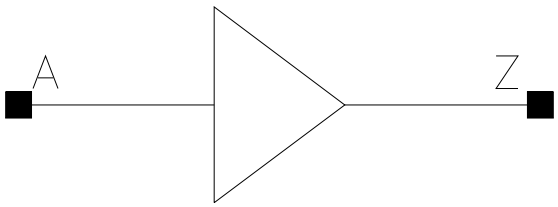
Pin Cycle (vdds)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.408	0.4896
X6_P16	1.200	0.408	0.4896
X8_P16	1.200	0.408	0.4896
X13_P16	1.200	0.544	0.6528
X16_P16	1.200	0.544	0.6528
X21_P16	1.200	0.680	0.8160
X25_P16	1.200	0.680	0.8160
X29_P16	1.200	0.952	1.1424
X33_P16	1.200	0.952	1.1424
X42_P16	1.200	1.088	1.3056
X50_P16	1.200	1.224	1.4688
X58_P16	1.200	1.496	1.7952
X67_P16	1.200	1.632	1.9584
X75_P16	1.200	1.768	2.1216
X84_P16	1.200	1.904	2.2848
X100_P16	1.200	2.312	2.7744
X134_P16	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0009	0.0009	0.0009	0.0009
	X16_P16	X21_P16	X25_P16	X29_P16
A	0.0009	0.0013	0.0013	0.0017
	X33_P16	X42_P16	X50_P16	X58_P16
A	0.0017	0.0020	0.0024	0.0035

	X67_P16	X75_P16	X84_P16	X100_P16
A	0.0035	0.0035	0.0035	0.0045
	X134_P16			
A	0.0057			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0266	0.0270	3.5215	2.5707
A to Z ↑	0.0213	0.0212	5.6209	4.0945
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0283	0.0320	1.9091	1.2347
A to Z ↑	0.0221	0.0251	2.8979	1.9088
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0346	0.0288	0.9832	0.7610
A to Z ↑	0.0267	0.0234	1.4548	1.1445
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0301	0.0290	0.6531	0.5505
A to Z ↑	0.0242	0.0225	0.9556	0.8161
	X33_P16	**X42_P16**	**X33_P16**	**X42_P16**
A to Z ↓	0.0302	0.0294	0.4886	0.3973
A to Z ↑	0.0232	0.0235	0.7131	0.5744
	X50_P16	**X58_P16**	**X50_P16**	**X58_P16**
A to Z ↓	0.0288	0.0269	0.3300	0.2845
A to Z ↑	0.0233	0.0219	0.4766	0.4096
	X67_P16	**X75_P16**	**X67_P16**	**X75_P16**
A to Z ↓	0.0282	0.0297	0.2500	0.2255
A to Z ↑	0.0229	0.0241	0.3596	0.3219
	X84_P16	**X100_P16**	**X84_P16**	**X100_P16**
A to Z ↓	0.0311	0.0289	0.2046	0.1719
A to Z ↑	0.0251	0.0236	0.2910	0.2438
	X134_P16		**X134_P16**	
A to Z ↓	0.0305		0.1340	
A to Z ↑	0.0250		0.1871	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	1.248e-07	1.000e-20
X6_P16	1.568e-07	1.000e-20
X8_P16	2.017e-07	1.000e-20
X13_P16	2.565e-07	1.000e-20
X16_P16	3.293e-07	1.000e-20
X21_P16	4.544e-07	1.000e-20
X25_P16	5.252e-07	1.000e-20
X29_P16	5.929e-07	1.000e-20
X33_P16	6.616e-07	1.000e-20
X42_P16	8.311e-07	1.000e-20
X50_P16	1.008e-06	1.000e-20
X58_P16	1.249e-06	1.000e-20
X67_P16	1.370e-06	1.000e-20
X75_P16	1.491e-06	1.000e-20

X84_P16	1.612e-06	1.000e-20
X100_P16	1.974e-06	1.000e-20
X134_P16	2.578e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	1.747e-03	1.965e-03	2.346e-03	3.140e-03
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	3.782e-03	5.134e-03	5.740e-03	6.493e-03
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	7.126e-03	8.958e-03	1.060e-02	1.294e-02
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	1.439e-02	1.611e-02	1.772e-02	2.092e-02
	X134_P16			
A to Z	2.884e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

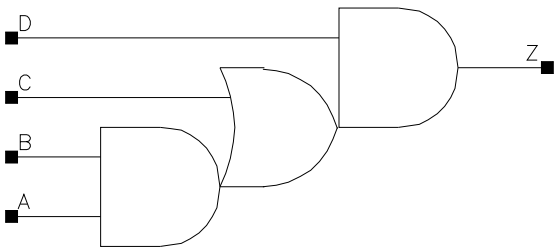
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P16			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.632	1.9584
X25_P16	1.200	1.768	2.1216
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0011	0.0024	0.0024	0.0023
B	0.0011	0.0022	0.0021	0.0021
C	0.0012	0.0026	0.0026	0.0025
D	0.0017	0.0023	0.0023	0.0023

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0367	0.0348	1.9502	0.9680
A to Z ↑	0.0337	0.0320	2.9426	1.4314
B to Z ↓	0.0336	0.0315	1.9453	0.9684
B to Z ↑	0.0340	0.0317	2.9437	1.4301
C to Z ↓	0.0309	0.0287	1.9418	0.9657
C to Z ↑	0.0253	0.0232	2.9137	1.4164

D to Z ↓	0.0303	0.0270	1.9217	0.9566
D to Z ↑	0.0293	0.0258	2.9178	1.4188
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0382	0.0407	0.6589	0.4978
A to Z ↑	0.0352	0.0373	0.9703	0.7295
B to Z ↓	0.0350	0.0381	0.6595	0.4974
B to Z ↑	0.0350	0.0378	0.9703	0.7297
C to Z ↓	0.0323	0.0353	0.6572	0.4952
C to Z ↑	0.0260	0.0282	0.9595	0.7203
D to Z ↓	0.0292	0.0310	0.6487	0.4871
D to Z ↑	0.0283	0.0301	0.9611	0.7215

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	3.826e-07	1.000e-20
X17_P16	7.494e-07	1.000e-20
X25_P16	8.848e-07	1.000e-20
X33_P16	1.020e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	4.221e-05	9.592e-05	9.608e-05	8.943e-05
B (output stable)	8.906e-05	1.502e-04	1.505e-04	1.510e-04
C (output stable)	3.227e-04	5.549e-04	5.584e-04	5.335e-04
D (output stable)	8.776e-05	1.125e-04	1.083e-04	1.073e-04
A to Z	4.014e-03	7.369e-03	9.172e-03	1.068e-02
B to Z	3.691e-03	6.571e-03	8.370e-03	9.997e-03
C to Z	3.056e-03	5.287e-03	7.047e-03	8.609e-03
D to Z	4.070e-03	7.058e-03	8.791e-03	1.025e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

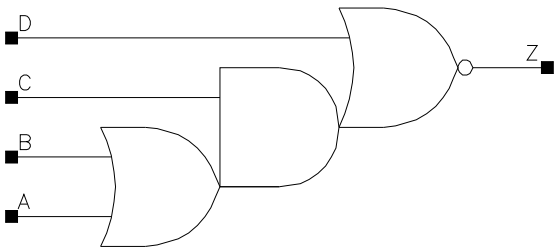
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.952	1.1424
X11_P16	1.200	1.496	1.7952
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X16_P16	X21_P16
A	0.0011	0.0020	0.0029	0.0039
B	0.0010	0.0019	0.0029	0.0038
C	0.0010	0.0019	0.0028	0.0037
D	0.0012	0.0018	0.0027	0.0036

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0167	0.0161	3.3227	1.7494
A to Z ↑	0.0344	0.0322	8.2406	4.3118
B to Z ↓	0.0159	0.0156	3.2374	1.7166
B to Z ↑	0.0326	0.0311	8.2525	4.3188
C to Z ↓	0.0152	0.0146	3.0712	1.6190
C to Z ↑	0.0214	0.0200	5.5632	2.8643

D to Z ↓	0.0093	0.0081	1.9747	0.9992
D to Z ↑	0.0187	0.0164	5.9692	3.0845
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0160	0.0164	1.1788	0.9084
A to Z ↑	0.0300	0.0317	2.7562	2.1319
B to Z ↓	0.0152	0.0156	1.1865	0.9100
B to Z ↑	0.0295	0.0303	2.7590	2.1346
C to Z ↓	0.0147	0.0148	1.1121	0.8521
C to Z ↑	0.0193	0.0194	1.8903	1.4184
D to Z ↓	0.0080	0.0080	0.6985	0.5331
D to Z ↑	0.0153	0.0153	2.0175	1.5276

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.847e-07	1.000e-20
X11_P16	5.477e-07	1.000e-20
X16_P16	7.735e-07	1.000e-20
X21_P16	1.036e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	4.441e-05	7.532e-05	9.484e-05	1.665e-04
B (output stable)	2.945e-05	6.970e-05	8.684e-05	1.324e-04
C (output stable)	2.735e-04	5.240e-04	7.126e-04	1.054e-03
D (output stable)	4.423e-05	8.392e-05	1.078e-04	1.793e-04
A to Z	2.906e-03	5.122e-03	7.176e-03	1.005e-02
B to Z	2.352e-03	4.184e-03	6.029e-03	8.142e-03
C to Z	1.945e-03	3.378e-03	4.819e-03	6.601e-03
D to Z	1.127e-03	1.909e-03	2.575e-03	3.434e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

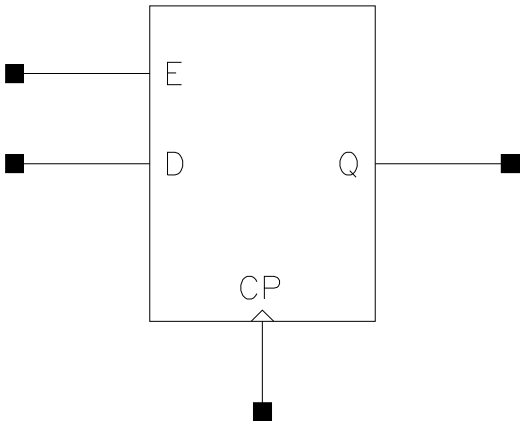
Pin Cycle (vdds)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.128	3.7536
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008
E	0.0013	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0435	0.0501	1.9444	1.0057
CP to Q ↑	0.0535	0.0573	2.9624	1.4821
	X33_P16		**X33_P16**	
CP to Q ↓	0.0744		0.4961	
CP to Q ↑	0.0911		0.7326	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0571	0.0571	0.0571
CP ↑	min_pulse_width to CP	0.0360	0.0407	0.0313
D ↓	hold_rising to CP	-0.0191	-0.0191	-0.0191
D ↑	hold_rising to CP	-0.0071	-0.0071	-0.0067
D ↓	setup_rising to CP	0.0587	0.0587	0.0587
D ↑	setup_rising to CP	0.0368	0.0368	0.0368
E ↓	hold_rising to CP	-0.0144	-0.0116	-0.0144
E ↑	hold_rising to CP	-0.0067	-0.0067	-0.0067
E ↓	setup_rising to CP	0.0604	0.0604	0.0604
E ↑	setup_rising to CP	0.0671	0.0671	0.0671

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	8.532e-07	1.000e-20
X17_P16	9.799e-07	1.000e-20
X33_P16	1.381e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

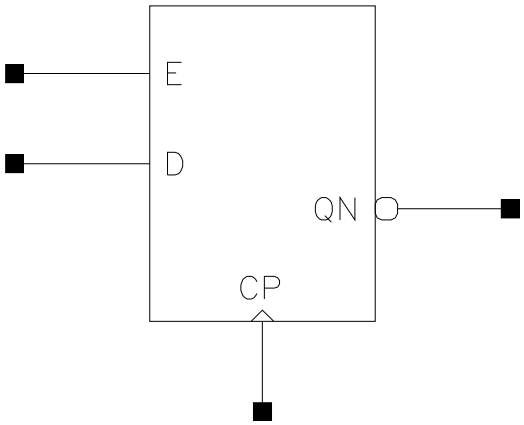
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	8.459e-03	8.462e-03	8.473e-03
Clock 100Mhz Data 25Mhz	1.116e-02	1.192e-02	1.486e-02
Clock 100Mhz Data 50Mhz	1.386e-02	1.538e-02	2.126e-02
Clock = 0 Data 100Mhz	5.467e-03	5.467e-03	5.467e-03
Clock = 1 Data 100Mhz	1.482e-03	1.482e-03	1.482e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.264	3.9168
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008
E	0.0010	0.0013	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.0746	0.0702	1.9976	0.9545
CP to QN ↑	0.0575	0.0592	2.9879	1.4315
	X33_P16		**X33_P16**	
CP to QN ↓	0.0755		0.4982	
CP to QN ↑	0.0656		0.7351	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0571	0.0571	0.0571
CP ↑	min_pulse_width to CP	0.0313	0.0346	0.0359
D ↓	hold_rising to CP	-0.0191	-0.0191	-0.0191
D ↑	hold_rising to CP	-0.0067	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0587	0.0587	0.0587
D ↑	setup_rising to CP	0.0368	0.0368	0.0368
E ↓	hold_rising to CP	-0.0144	-0.0148	-0.0116
E ↑	hold_rising to CP	-0.0067	-0.0067	-0.0067
E ↓	setup_rising to CP	0.0604	0.0604	0.0604
E ↑	setup_rising to CP	0.0671	0.0671	0.0671

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	8.451e-07	1.000e-20
X17_P16	1.056e-06	1.000e-20
X33_P16	1.350e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

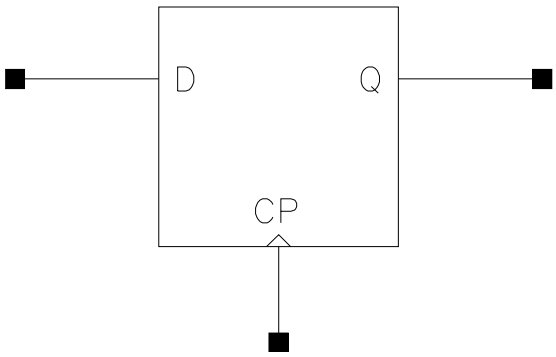
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	8.452e-03	8.455e-03	8.457e-03
Clock 100Mhz Data 25Mhz	1.122e-02	1.251e-02	1.465e-02
Clock 100Mhz Data 50Mhz	1.398e-02	1.657e-02	2.084e-02
Clock = 0 Data 100Mhz	5.484e-03	5.483e-03	5.483e-03
Clock = 1 Data 100Mhz	1.481e-03	1.481e-03	1.481e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.176	2.6112
X17_P16	1.200	2.448	2.9376
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0454	0.0502	1.9342	0.9965
CP to Q ↑	0.0539	0.0600	2.8564	1.4535
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to Q ↓	0.0633	0.0657	0.5939	0.5401
CP to Q ↑	0.0680	0.0694	0.8253	0.7493

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0523	0.0523	0.0523	0.0523
CP ↑	min_pulse_width to CP	0.0360	0.0406	0.0514	0.0548
D ↓	hold_rising to CP	0.0075	0.0075	0.0075	0.0075
D ↑	hold_rising to CP	0.0107	0.0107	0.0107	0.0107
D ↓	setup_rising to CP	0.0326	0.0321	0.0321	0.0321
D ↑	setup_rising to CP	0.0168	0.0168	0.0168	0.0168

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	6.691e-07	1.000e-20
X17_P16	8.073e-07	1.000e-20
X30_P16	9.989e-07	1.000e-20
X33_P16	1.051e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

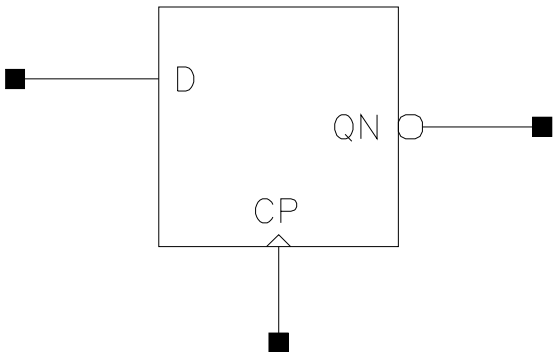
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	8.862e-03	8.919e-03	8.941e-03	8.951e-03
Clock 100Mhz Data 25Mhz	1.022e-02	1.137e-02	1.307e-02	1.345e-02
Clock 100Mhz Data 50Mhz	1.159e-02	1.382e-02	1.720e-02	1.795e-02
Clock = 0 Data 100Mhz	3.751e-03	3.866e-03	3.901e-03	3.918e-03
Clock = 1 Data 100Mhz	3.903e-05	3.915e-05	3.926e-05	3.931e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.0444	0.0527	2.0001	1.0324
CP to QN ↑	0.0467	0.0497	2.8526	1.4530
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to QN ↓	0.0750	0.0754	0.5474	0.4965
CP to QN ↑	0.0611	0.0703	0.7926	0.7340

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0462	0.0462	0.0523	0.0523
CP ↑	min_pulse_width to CP	0.0346	0.0406	0.0360	0.0406
D ↓	hold_rising to CP	0.0124	0.0124	0.0075	0.0102
D ↑	hold_rising to CP	0.0098	0.0098	0.0081	0.0107
D ↓	setup_rising to CP	0.0229	0.0223	0.0321	0.0326
D ↑	setup_rising to CP	0.0200	0.0200	0.0168	0.0168

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	6.145e-07	1.000e-20
X17_P16	7.430e-07	1.000e-20
X30_P16	1.098e-06	1.000e-20
X33_P16	1.169e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

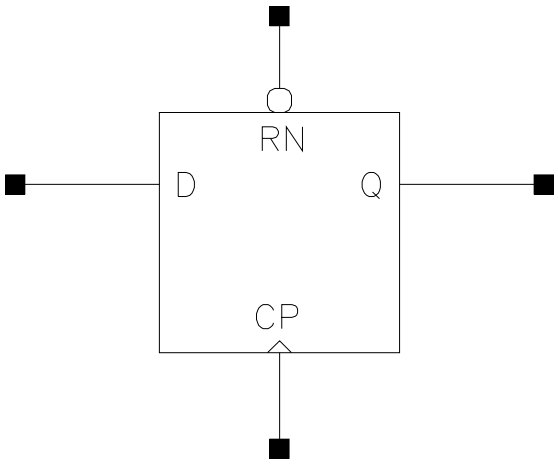
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	8.564e-03	8.568e-03	8.712e-03	8.770e-03
Clock 100Mhz Data 25Mhz	9.743e-03	1.058e-02	1.309e-02	1.366e-02
Clock 100Mhz Data 50Mhz	1.092e-02	1.259e-02	1.747e-02	1.854e-02
Clock = 0 Data 100Mhz	3.235e-03	3.235e-03	3.484e-03	3.553e-03
Clock = 1 Data 100Mhz	3.882e-05	3.887e-05	3.915e-05	3.926e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0011	0.0011
D	0.0008	0.0008
RN	0.0011	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0523	0.0653	1.0055	0.6038
CP to Q ↑	0.0616	0.0694	1.4580	0.8290
RN to Q ↓	0.0846	0.1128	1.0646	0.6403

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0570	0.0571
CP ↑	min_pulse_width to CP	0.0406	0.0547
D ↓	hold_rising to CP	0.0075	0.0075
D ↑	hold_rising to CP	0.0081	0.0081
D ↓	setup_rising to CP	0.0343	0.0343
D ↑	setup_rising to CP	0.0222	0.0222
RN ↓	min_pulse_width to RN	0.1045	0.1338
RN ↑	recovery_rising to CP	0.0173	0.0173
RN ↑	removal_rising to CP	-0.0076	-0.0076

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P16	9.203e-07	1.000e-20
X30_P16	1.130e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

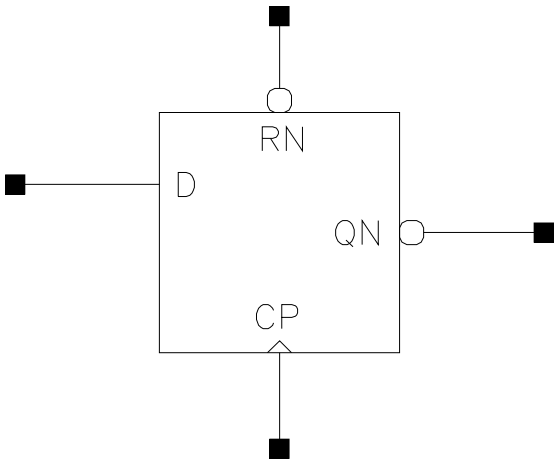
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	9.521e-03	9.519e-03
Clock 100Mhz Data 25Mhz	1.212e-02	1.378e-02
Clock 100Mhz Data 50Mhz	1.472e-02	1.804e-02
Clock = 0 Data 100Mhz	4.545e-03	4.548e-03
Clock = 1 Data 100Mhz	3.959e-05	3.976e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0011	0.0011
D	0.0008	0.0008
RN	0.0011	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.0717	0.0774	0.9477	0.5490
CP to QN ↑	0.0592	0.0637	1.4204	0.7959
RN to QN ↑	0.0868	0.0925	1.4239	0.7987

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0570	0.0570
CP ↑	min_pulse_width to CP	0.0346	0.0359
D ↓	hold_rising to CP	0.0079	0.0079
D ↑	hold_rising to CP	0.0081	0.0081
D ↓	setup_rising to CP	0.0343	0.0343
D ↑	setup_rising to CP	0.0222	0.0222
RN ↓	min_pulse_width to RN	0.0850	0.0850
RN ↑	recovery_rising to CP	0.0173	0.0173
RN ↑	removal_rising to CP	-0.0076	-0.0076

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P16	9.934e-07	1.000e-20
X30_P16	1.165e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

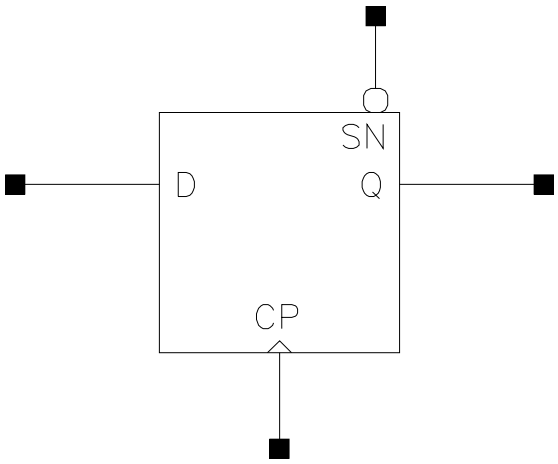
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	9.529e-03	9.524e-03
Clock 100Mhz Data 25Mhz	1.269e-02	1.408e-02
Clock 100Mhz Data 50Mhz	1.585e-02	1.864e-02
Clock = 0 Data 100Mhz	4.608e-03	4.591e-03
Clock = 1 Data 100Mhz	3.959e-05	3.967e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0011	0.0011
D	0.0008	0.0008
SN	0.0014	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0521	0.0659	1.0070	0.6009
CP to Q ↑	0.0610	0.0693	1.4597	0.8291
SN to Q ↑	0.0605	0.0708	1.4634	0.8305

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0584	0.0584
CP ↑	min_pulse_width to CP	0.0406	0.0547
D ↓	hold_rising to CP	0.0053	0.0079
D ↑	hold_rising to CP	0.0081	0.0081
D ↓	setup_rising to CP	0.0392	0.0392
D ↑	setup_rising to CP	0.0200	0.0200
SN ↓	min_pulse_width to SN	0.0576	0.0701
SN ↑	recovery_rising to CP	0.0112	0.0112
SN ↑	removal_rising to CP	0.0260	0.0260

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P16	9.004e-07	1.000e-20
X30_P16	1.072e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

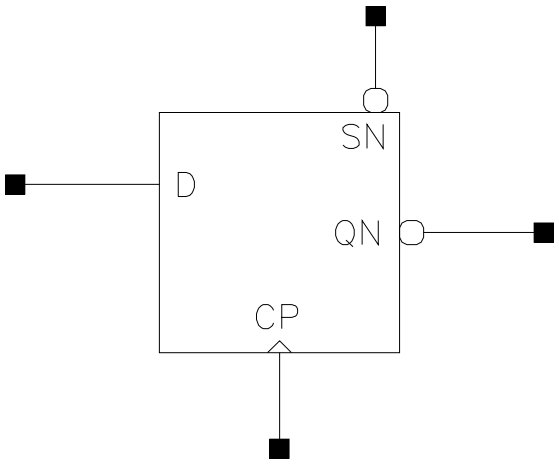
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	9.599e-03	9.586e-03
Clock 100Mhz Data 25Mhz	1.219e-02	1.385e-02
Clock 100Mhz Data 50Mhz	1.478e-02	1.812e-02
Clock = 0 Data 100Mhz	4.505e-03	4.504e-03
Clock = 1 Data 100Mhz	2.558e-05	2.574e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0011	0.0011
D	0.0008	0.0008
SN	0.0014	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.0711	0.0768	0.9495	0.5502
CP to QN ↑	0.0592	0.0638	1.4166	0.7938
SN to QN ↓	0.0698	0.0758	0.9497	0.5504

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0584	0.0584
CP ↑	min_pulse_width to CP	0.0346	0.0359
D ↓	hold_rising to CP	0.0053	0.0053
D ↑	hold_rising to CP	0.0081	0.0081
D ↓	setup_rising to CP	0.0392	0.0392
D ↑	setup_rising to CP	0.0200	0.0200
SN ↓	min_pulse_width to SN	0.0496	0.0522
SN ↑	recovery_rising to CP	0.0112	0.0112
SN ↑	removal_rising to CP	0.0260	0.0260

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P16	1.027e-06	1.000e-20
X30_P16	1.235e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

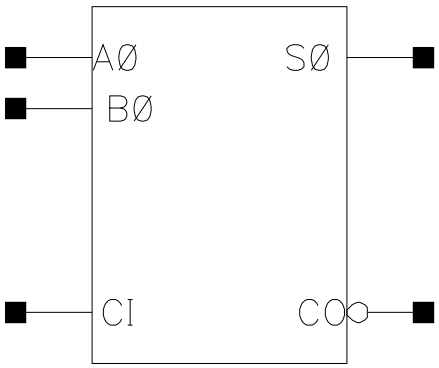
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	9.605e-03	9.604e-03
Clock 100Mhz Data 25Mhz	1.273e-02	1.414e-02
Clock 100Mhz Data 50Mhz	1.585e-02	1.867e-02
Clock = 0 Data 100Mhz	4.497e-03	4.497e-03
Clock = 1 Data 100Mhz	3.946e-05	3.952e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_-P16	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_-P16	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_-P16	1.200	3.672	4.4064
C12T28SOI_LLS1_-FA1X33_P16	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16
A0	0.0038	0.0076	0.0033	0.0064
B0	0.0034	0.0073	0.0036	0.0062
CI	0.0026	0.0056	0.0025	0.0044

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16
A0 to CO ↓	0.0482	0.0527	2.0176	0.5327
A0 to CO ↑	0.0361	0.0378	2.9559	0.7613
A0 to S0 ↓	0.0506	0.0637	1.9878	0.5192
A0 to S0 ↑	0.0517	0.0632	2.9129	0.7487
B0 to CO ↓	0.0476	0.0530	2.0258	0.5361
B0 to CO ↑	0.0372	0.0394	2.9581	0.7590
B0 to S0 ↓	0.0510	0.0647	1.9877	0.5192
B0 to S0 ↑	0.0519	0.0640	2.9131	0.7488
CI to CO ↓	0.0461	0.0518	2.0302	0.5353
CI to CO ↑	0.0368	0.0385	2.9572	0.7616
CI to S0 ↓	0.0504	0.0639	1.9879	0.5190
CI to S0 ↑	0.0518	0.0642	2.9129	0.7487
	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16
A0 to CO ↓	0.0314	0.0387	3.9374	0.6810
A0 to CO ↑	0.0274	0.0320	2.9967	0.7520
A0 to S0 ↓	0.0660	0.0818	2.1496	0.5436
A0 to S0 ↑	0.0601	0.0656	3.0345	0.7620
B0 to CO ↓	0.0323	0.0400	3.9394	0.6819
B0 to CO ↑	0.0255	0.0306	2.9935	0.7522
B0 to S0 ↓	0.0665	0.0839	2.1480	0.5434
B0 to S0 ↑	0.0606	0.0676	3.0354	0.7617
CI to CO ↓	0.0318	0.0551	3.9328	0.6905
CI to CO ↑	0.0282	0.0345	3.0796	0.7587
CI to S0 ↓	0.0384	0.0505	2.1514	0.5439
CI to S0 ↑	0.0328	0.0334	3.0343	0.7624

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_FA1X8_P16	9.128e-07	1.000e-20
C12T28SOI_LL_FA1X33_P16	2.303e-06	1.000e-20
C12T28SOI_LLS1_FA1X8_P16	1.556e-06	1.000e-20
C12T28SOI_LLS1_FA1X33_P16	3.497e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16
A0 to CO	4.247e-03	1.183e-02	6.294e-03	1.574e-02
A0 to S0	4.274e-03	1.224e-02	8.454e-03	1.957e-02
B0 to CO	4.169e-03	1.178e-02	6.351e-03	1.598e-02
B0 to S0	4.032e-03	1.186e-02	8.560e-03	1.990e-02
CI to CO	4.162e-03	1.180e-02	4.463e-03	1.404e-02
CI to S0	3.997e-03	1.182e-02	5.067e-03	1.516e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X33_P16	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X33_P16
A0	0.0013	0.0038
B0	0.0011	0.0033

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
A0 to CO ↓	0.0369	0.0338	1.9883	0.4944
A0 to CO ↑	0.0334	0.0306	2.9230	0.7542
A0 to S0 ↓	0.0478	0.0456	1.9454	0.4938
A0 to S0 ↑	0.0452	0.0504	2.8782	0.7426
B0 to CO ↓	0.0358	0.0312	1.9896	0.4906
B0 to CO ↑	0.0358	0.0318	2.9222	0.7544
B0 to S0 ↓	0.0493	0.0453	1.9451	0.4939
B0 to S0 ↑	0.0445	0.0482	2.8794	0.7428

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	4.666e-07	1.000e-20
X33_P16	1.865e-06	1.000e-20

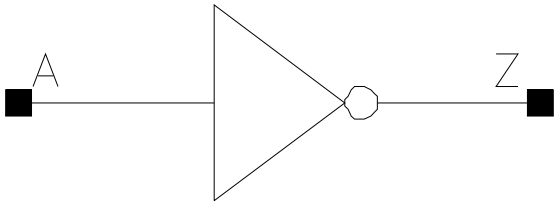
Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X33_P16
A0 to CO	3.232e-03	1.064e-02
A0 to S0	2.955e-03	1.019e-02
B0 to CO	3.240e-03	1.047e-02
B0 to S0	2.878e-03	9.659e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X8_P16	X33_P16
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.272	0.3264
X6_P16	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X13_P16	1.200	0.408	0.4896
X17_P16	1.200	0.408	0.4896
X21_P16	1.200	0.544	0.6528
X25_P16	1.200	0.544	0.6528
X29_P16	1.200	0.680	0.8160
X33_P16	1.200	0.680	0.8160
X50_P16	1.200	0.952	1.1424
X58_P16	1.200	1.088	1.3056
X67_P16	1.200	1.224	1.4688
X75_P16	1.200	1.360	1.6320
X84_P16	1.200	1.496	1.7952
X100_P16	1.200	1.768	2.1216
X134_P16	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0006	0.0008	0.0010	0.0015
	X17_P16	X21_P16	X25_P16	X29_P16
A	0.0019	0.0024	0.0028	0.0033
	X33_P16	X50_P16	X58_P16	X67_P16
A	0.0037	0.0055	0.0065	0.0074
	X75_P16	X84_P16	X100_P16	X134_P16

A	0.0084	0.0096	0.0117	0.0162

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0084	0.0079	3.7078	2.8492
A to Z ↑	0.0133	0.0122	5.7677	4.3166
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0072	0.0063	1.9596	1.2686
A to Z ↑	0.0110	0.0101	2.9535	1.9633
	X17_P16	**X21_P16**	**X17_P16**	**X21_P16**
A to Z ↓	0.0062	0.0067	0.9723	0.7855
A to Z ↑	0.0096	0.0102	1.4549	1.1784
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0066	0.0063	0.6675	0.5664
A to Z ↑	0.0098	0.0095	0.9787	0.8403
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0063	0.0065	0.5018	0.3394
A to Z ↑	0.0093	0.0093	0.7334	0.4909
	X58_P16	**X67_P16**	**X58_P16**	**X67_P16**
A to Z ↓	0.0067	0.0067	0.2946	0.2587
A to Z ↑	0.0095	0.0094	0.4236	0.3709
	X75_P16	**X84_P16**	**X75_P16**	**X84_P16**
A to Z ↓	0.0071	0.0073	0.2336	0.2114
A to Z ↑	0.0098	0.0100	0.3329	0.3012
	X100_P16	**X134_P16**	**X100_P16**	**X134_P16**
A to Z ↓	0.0081	0.0089	0.1802	0.1407
A to Z ↑	0.0107	0.0114	0.2545	0.1963

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	6.523e-08	1.000e-20
X6_P16	8.915e-08	1.000e-20
X8_P16	1.386e-07	1.000e-20
X13_P16	1.990e-07	1.000e-20
X17_P16	2.780e-07	1.000e-20
X21_P16	3.263e-07	1.000e-20
X25_P16	4.010e-07	1.000e-20
X29_P16	4.517e-07	1.000e-20
X33_P16	5.215e-07	1.000e-20
X50_P16	7.627e-07	1.000e-20
X58_P16	8.835e-07	1.000e-20
X67_P16	1.004e-06	1.000e-20
X75_P16	1.125e-06	1.000e-20
X84_P16	1.246e-06	1.000e-20
X100_P16	1.488e-06	1.000e-20
X134_P16	1.971e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16

A to Z	4.653e-04	5.592e-04	7.095e-04	9.482e-04
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	1.200e-03	1.657e-03	1.904e-03	2.071e-03
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	2.300e-03	3.445e-03	4.151e-03	4.579e-03
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	5.284e-03	5.785e-03	7.086e-03	9.804e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

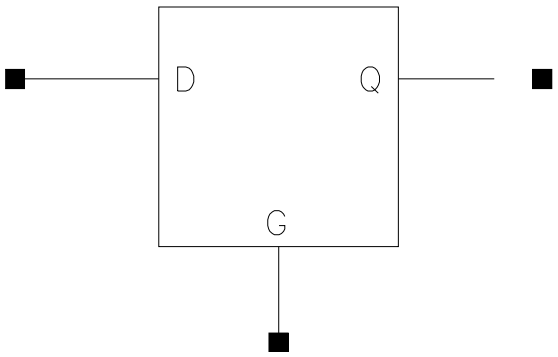
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X23_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P16	X23_P16
D	0.0006	0.0015
G	0.0013	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X23_P16	X8_P16	X23_P16
D to Q ↓	0.0546	0.0432	2.0288	0.9514
D to Q ↑	0.0356	0.0358	2.8745	0.7688
G to Q ↓	0.0574	0.0451	2.0256	0.9503
G to Q ↑	0.0347	0.0319	2.8807	0.7694

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P16	X23_P16
D ↓	hold_falling to G	-0.0143	-0.0039
D ↑	hold_falling to G	0.0007	-0.0025
D ↓	setup_falling to G	0.0537	0.0392
D ↑	setup_falling to G	0.0405	0.0425
G ↑	min_pulse_width to G	0.0496	0.0471

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	3.601e-07	1.000e-20
X23_P16	7.844e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X23_P16
D (output stable)	1.716e-05	8.051e-05
G (output stable)	1.026e-03	2.006e-03
D to Q	4.998e-03	9.738e-03
G to Q	4.506e-03	8.448e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

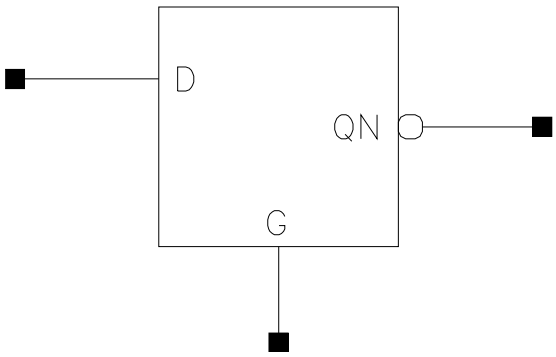
Pin Cycle (vdds)	X8_P16	X23_P16
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P16
D	0.0007
G	0.0016

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P16	X17_P16
D to QN ↓	0.0474	0.9524
D to QN ↑	0.0605	1.4101
G to QN ↓	0.0457	0.9525
G to QN ↑	0.0611	1.4101

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P16
D ↓	hold_falling to G	-0.0191
D ↑	hold_falling to G	-0.0056
D ↓	setup_falling to G	0.0440
D ↑	setup_falling to G	0.0302
G ↑	min_pulse_width to G	0.0375

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P16	5.513e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X17_P16
D (output stable)	2.967e-05
G (output stable)	1.149e-03
D to QN	6.414e-03
G to QN	5.757e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

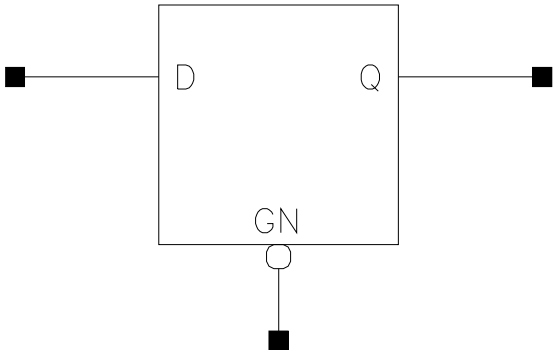
Pin Cycle (vdds)	X17_P16
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
D	0.0006	0.0009	0.0020
GN	0.0013	0.0016	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D to Q ↓	0.0551	0.0475	2.0357	1.0002
D to Q ↑	0.0363	0.0344	2.8831	1.4793
GN to Q ↓	0.0496	0.0424	2.0362	1.0013
GN to Q ↑	0.0525	0.0500	2.8776	1.4778

	X33_P16		X33_P16	
D to Q ↓	0.0464		0.5120	
D to Q ↑	0.0299		0.7409	
GN to Q ↓	0.0402		0.5122	
GN to Q ↑	0.0392		0.7400	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X33_P16
D ↓	hold_rising to GN	-0.0162	-0.0123	-0.0123
D ↑	hold_rising to GN	0.0010	0.0036	0.0053
D ↓	setup_rising to GN	0.0618	0.0517	0.0521
D ↑	setup_rising to GN	0.0335	0.0318	0.0265
GN ↓	min_pulse_width to GN	0.0646	0.0590	0.0546

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	3.610e-07	1.000e-20
X17_P16	5.678e-07	1.000e-20
X33_P16	9.724e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
D (output stable)	1.890e-05	3.084e-05	8.256e-05
GN (output stable)	1.022e-03	1.396e-03	1.694e-03
D to Q	5.008e-03	7.080e-03	1.161e-02
GN to Q	7.091e-03	9.699e-03	1.444e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

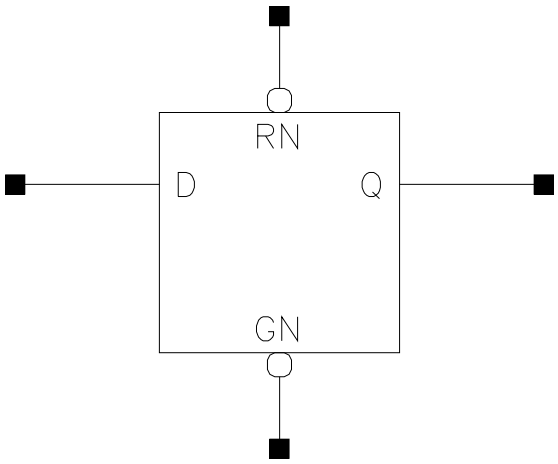
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.496	1.7952
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X33_P16
D	0.0006	0.0016
GN	0.0014	0.0027
RN	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
D to Q ↓	0.0516	0.0466	1.9841	0.5147
D to Q ↑	0.0467	0.0601	2.9475	0.7709

GN to Q ↓	0.0470	0.0429	1.9853	0.5149
GN to Q ↑	0.0599	0.0624	2.9499	0.7712
RN to Q ↓	0.0421	0.0784	1.9187	0.5589
RN to Q ↑	0.0494	0.0653	2.9501	0.7706

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P16	X33_P16
D ↓	hold_rising to GN	-0.0171	-0.0096
D ↑	hold_rising to GN	-0.0088	-0.0266
D ↓	setup_rising to GN	0.0575	0.0501
D ↑	setup_rising to GN	0.0465	0.0659
GN ↓	min_pulse_width to GN	0.0600	0.0635
RN ↓	min_pulse_width to RN	0.0491	0.0876
RN ↑	recovery_rising to GN	0.0492	0.0729
RN ↑	removal_rising to GN	-0.0320	-0.0484

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	4.055e-07	1.000e-20
X33_P16	9.853e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X33_P16
D (output stable)	8.260e-05	1.125e-04
GN (output stable)	1.190e-03	1.815e-03
RN (output stable)	2.249e-05	4.332e-05
D to Q	5.009e-03	1.279e-02
GN to Q	7.241e-03	1.614e-02
RN to Q	4.004e-03	1.000e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

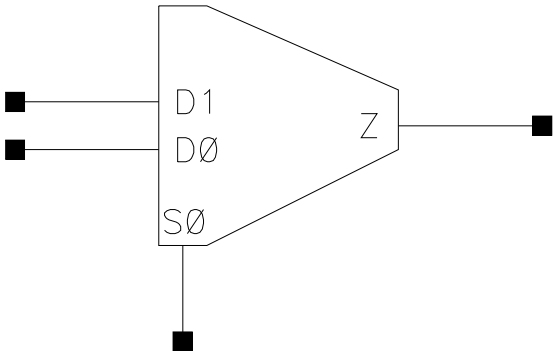
Pin Cycle (vdds)	X8_P16	X33_P16
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
D0	0.0008	0.0013	0.0016	0.0023
D1	0.0008	0.0012	0.0016	0.0023
S0	0.0015	0.0017	0.0019	0.0028

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D0 to Z ↓	0.0421	0.0373	1.9848	0.9737
D0 to Z ↑	0.0335	0.0309	2.9509	1.4410
D1 to Z ↓	0.0403	0.0369	1.9805	0.9713
D1 to Z ↑	0.0306	0.0291	2.9415	1.4367
S0 to Z ↓	0.0365	0.0353	1.9769	0.9706
S0 to Z ↑	0.0343	0.0345	2.9445	1.4387

	X25_P16	X33_P16	X25_P16	X33_P16
D0 to Z ↓	0.0403	0.0362	0.6719	0.5036
D0 to Z ↑	0.0332	0.0307	0.9697	0.7252
D1 to Z ↓	0.0433	0.0379	0.6751	0.5045
D1 to Z ↑	0.0319	0.0296	0.9688	0.7251
S0 to Z ↓	0.0405	0.0371	0.6716	0.5029
S0 to Z ↑	0.0383	0.0351	0.9692	0.7255

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	3.906e-07	1.000e-20
X17_P16	7.205e-07	1.000e-20
X25_P16	9.627e-07	1.000e-20
X33_P16	1.413e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	8.812e-04	1.292e-03	1.401e-03	1.908e-03
D1 (output stable)	7.176e-04	1.191e-03	1.572e-03	2.002e-03
S0 (output stable)	1.217e-03	1.401e-03	1.841e-03	2.263e-03
D0 to Z	3.406e-03	5.552e-03	8.658e-03	1.088e-02
D1 to Z	3.151e-03	5.383e-03	8.731e-03	1.078e-02
S0 to Z	3.885e-03	5.931e-03	9.678e-03	1.186e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

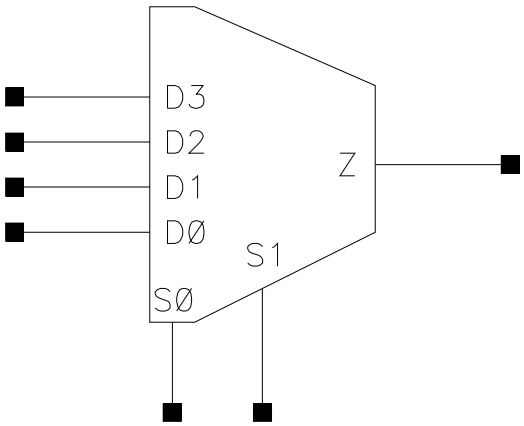
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.312	2.7744
X31_P16	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P16	X31_P16
D0	0.0006	0.0017
D1	0.0006	0.0016
D2	0.0006	0.0017
D3	0.0006	0.0017
S0	0.0022	0.0044
S1	0.0014	0.0027

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X31_P16	X8_P16	X31_P16

D0 to Z ↓	0.0718	0.0736	2.0800	0.5793
D0 to Z ↑	0.0478	0.0509	2.9744	0.8050
D1 to Z ↓	0.0712	0.0736	2.0776	0.5791
D1 to Z ↑	0.0480	0.0507	2.9763	0.8049
D2 to Z ↓	0.0768	0.0697	2.0908	0.5740
D2 to Z ↑	0.0503	0.0470	2.9829	0.7990
D3 to Z ↓	0.0765	0.0690	2.0908	0.5729
D3 to Z ↑	0.0497	0.0487	2.9821	0.8027
S0 to Z ↓	0.0789	0.0806	2.0810	0.5756
S0 to Z ↑	0.0590	0.0632	2.9789	0.8036
S1 to Z ↓	0.0554	0.0559	2.0841	0.5762
S1 to Z ↑	0.0443	0.0467	2.9759	0.8029

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	4.924e-07	1.000e-20
X31_P16	1.515e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X31_P16
D0 (output stable)	4.717e-05	1.962e-04
D1 (output stable)	4.809e-05	2.088e-04
D2 (output stable)	4.106e-05	8.221e-05
D3 (output stable)	4.713e-05	1.800e-04
S0 (output stable)	1.977e-03	4.744e-03
S1 (output stable)	1.210e-03	2.568e-03
D0 to Z	3.734e-03	1.268e-02
D1 to Z	3.726e-03	1.274e-02
D2 to Z	3.998e-03	1.195e-02
D3 to Z	3.982e-03	1.194e-02
S0 to Z	5.918e-03	1.757e-02
S1 to Z	4.012e-03	1.155e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

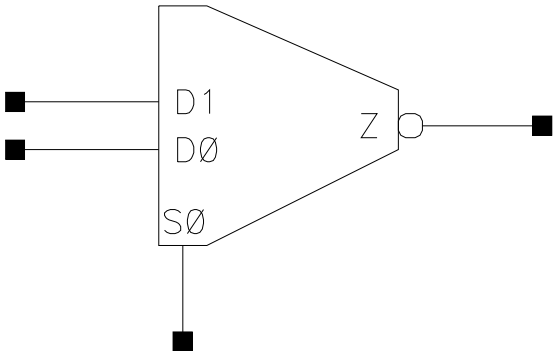
Pin Cycle (vdds)	X8_P16	X31_P16
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.816	0.9792
X5_P16	1.200	0.952	1.1424
X10_P16	1.200	1.768	2.1216
X16_P16	1.200	2.448	2.9376
X21_P16	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P16	X5_P16	X10_P16	X16_P16
D0	0.0006	0.0009	0.0020	0.0030
D1	0.0006	0.0010	0.0019	0.0029
S0	0.0013	0.0023	0.0030	0.0045
	X21_P16			
D0	0.0039			
D1	0.0039			
S0	0.0052			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X5_P16	X3_P16	X5_P16
D0 to Z ↓	0.0148	0.0150	6.2809	3.9267

D0 to Z ↑	0.0242	0.0217	12.0918	6.1399
D1 to Z ↓	0.0145	0.0142	6.2331	3.7203
D1 to Z ↑	0.0251	0.0228	12.1046	6.3875
S0 to Z ↓	0.0220	0.0183	6.2484	3.8229
S0 to Z ↑	0.0235	0.0195	12.0728	6.2641
	X10_P16	**X16_P16**	**X10_P16**	**X16_P16**
D0 to Z ↓	0.0168	0.0157	1.8488	1.2078
D0 to Z ↑	0.0235	0.0225	2.8655	1.8877
D1 to Z ↓	0.0151	0.0149	1.7858	1.1779
D1 to Z ↑	0.0238	0.0232	2.9183	1.9093
S0 to Z ↓	0.0225	0.0195	1.8151	1.1928
S0 to Z ↑	0.0232	0.0201	2.8927	1.8996
	X21_P16		**X21_P16**	
D0 to Z ↓	0.0156		0.9230	
D0 to Z ↑	0.0221		1.4319	
D1 to Z ↓	0.0149		0.8941	
D1 to Z ↑	0.0233		1.4247	
S0 to Z ↓	0.0205		0.9077	
S0 to Z ↑	0.0208		1.4286	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.686e-07	1.000e-20
X5_P16	3.605e-07	1.000e-20
X10_P16	6.599e-07	1.000e-20
X16_P16	1.048e-06	1.000e-20
X21_P16	1.303e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	1.911e-05	4.230e-05	1.753e-04	2.466e-04
D1 (output stable)	3.002e-05	1.580e-04	1.643e-04	2.718e-04
S0 (output stable)	1.031e-03	1.502e-03	2.662e-03	4.090e-03
D0 to Z	1.035e-03	1.733e-03	4.314e-03	6.106e-03
D1 to Z	1.030e-03	1.717e-03	4.094e-03	5.998e-03
S0 to Z	1.759e-03	2.509e-03	5.281e-03	7.394e-03
	X21_P16			
D0 (output stable)	3.089e-04			
D1 (output stable)	4.077e-04			
S0 (output stable)	4.621e-03			
D0 to Z	7.869e-03			
D1 to Z	7.913e-03			
S0 to Z	9.102e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

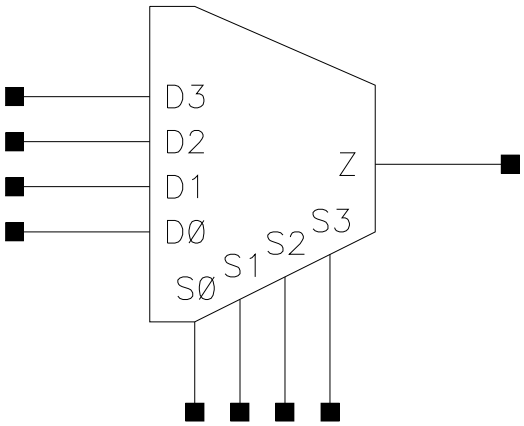
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P16			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	1.768	2.1216
X27_P16	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P16	X27_P16
D0	0.0007	0.0023
D1	0.0008	0.0024
D2	0.0007	0.0023
D3	0.0008	0.0024
S0	0.0007	0.0022
S1	0.0008	0.0022
S2	0.0008	0.0022
S3	0.0008	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	X27_P16	X7_P16	X27_P16
D0 to Z ↓	0.0547	0.0465	3.2622	0.8943
D0 to Z ↑	0.0396	0.0345	2.8926	0.7210
D1 to Z ↓	0.0501	0.0428	3.2603	0.8938
D1 to Z ↑	0.0356	0.0302	2.8817	0.7181
D2 to Z ↓	0.0553	0.0444	3.2710	0.8956
D2 to Z ↑	0.0387	0.0323	2.9068	0.7246
D3 to Z ↓	0.0508	0.0408	3.2642	0.8944
D3 to Z ↑	0.0347	0.0281	2.8952	0.7211
S0 to Z ↓	0.0526	0.0438	3.2621	0.8944
S0 to Z ↑	0.0424	0.0363	2.8920	0.7211
S1 to Z ↓	0.0484	0.0401	3.2595	0.8941
S1 to Z ↑	0.0380	0.0316	2.8818	0.7184
S2 to Z ↓	0.0532	0.0416	3.2692	0.8952
S2 to Z ↑	0.0414	0.0340	2.9059	0.7247
S3 to Z ↓	0.0491	0.0380	3.2637	0.8938
S3 to Z ↑	0.0371	0.0294	2.8968	0.7219

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X7_P16	4.420e-07	1.000e-20
X27_P16	1.759e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X7_P16	X27_P16
D0 (output stable)	5.854e-04	1.875e-03
D1 (output stable)	4.567e-04	1.419e-03
D2 (output stable)	5.673e-04	1.781e-03
D3 (output stable)	4.229e-04	1.301e-03
S0 (output stable)	5.960e-04	1.858e-03
S1 (output stable)	4.486e-04	1.386e-03
S2 (output stable)	5.334e-04	1.629e-03
S3 (output stable)	4.017e-04	1.203e-03
D0 to Z	4.390e-03	1.393e-02
D1 to Z	3.839e-03	1.195e-02
D2 to Z	4.196e-03	1.207e-02
D3 to Z	3.653e-03	1.010e-02
S0 to Z	4.256e-03	1.317e-02
S1 to Z	3.705e-03	1.123e-02
S2 to Z	4.058e-03	1.128e-02
S3 to Z	3.516e-03	9.381e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

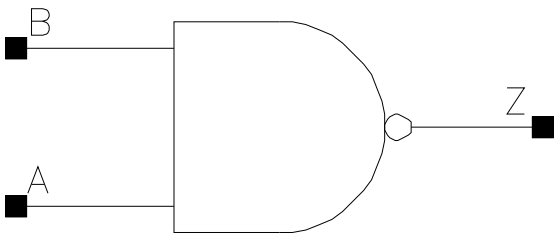
Pin Cycle (vdds)	X7_P16	X27_P16
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P16	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P16	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P16	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P16	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P16	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P16	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P16	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P16	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P16	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P16	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P16	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P16	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P16	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P16	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P16	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P16	C12T28SOI_LL_-NAND2X5_P16	C12T28SOI_LL_-NAND2X7_P16	C12T28SOI_LL_-NAND2X10_P16
A	0.0006	0.0008	0.0010	0.0016
B	0.0006	0.0008	0.0009	0.0014
	C12T28SOI_LL_-NAND2X13_P16	C12T28SOI_LL_-NAND2X17_P16	C12T28SOI_LL_-NAND2X20_P16	C12T28SOI_LL_-NAND2X24_P16
A	0.0019	0.0025	0.0028	0.0035
B	0.0018	0.0023	0.0027	0.0032
	C12T28SOI_LL_-NAND2X27_P16	C12T28SOI_LL_-NAND2X42_P16	C12T28SOI_LL_-NAND2X47_P16	C12T28SOI_LL_-NAND2X50_P16
A	0.0038	0.0012	0.0012	0.0012
B	0.0035	0.0012	0.0012	0.0012
	C12T28SOI_LL_-NAND2X58_P16	C12T28SOI_LL_-NAND2X67_P16	C12T28SOI_-LLBR0D8_-NAND2X7_P16	C12T28SOI_-LLBR0D8_-NAND2X14_P16
A	0.0012	0.0012	0.0009	0.0019
B	0.0012	0.0012	0.0009	0.0018
	C12T28SOI_LLS_-NAND2X40_P16	C12T28SOI_LLS_-NAND2X54_P16		
A	0.0057	0.0076		
B	0.0053	0.0070		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P16	**C12T28SOI_LL_-NAND2X5_P16**	**C12T28SOI_LL_-NAND2X3_P16**	**C12T28SOI_LL_-NAND2X5_P16**
A to Z ↓	0.0111	0.0103	6.1309	3.9850
A to Z ↑	0.0162	0.0147	5.7817	3.6604
B to Z ↓	0.0119	0.0107	6.2160	4.0387
B to Z ↑	0.0144	0.0126	5.8247	3.6894
	C12T28SOI_LL_-NAND2X7_P16	**C12T28SOI_LL_-NAND2X10_P16**	**C12T28SOI_LL_-NAND2X7_P16**	**C12T28SOI_LL_-NAND2X10_P16**
A to Z ↓	0.0102	0.0118	3.3449	2.2167
A to Z ↑	0.0142	0.0154	2.9410	1.9422
B to Z ↓	0.0105	0.0105	3.3846	2.2485
B to Z ↑	0.0120	0.0120	2.9689	1.9606
	C12T28SOI_LL_-NAND2X13_P16	**C12T28SOI_LL_-NAND2X17_P16**	**C12T28SOI_LL_-NAND2X13_P16**	**C12T28SOI_LL_-NAND2X17_P16**
A to Z ↓	0.0114	0.0112	1.7118	1.3623

A to Z ↑	0.0145	0.0147	1.4442	1.1717
B to Z ↓	0.0100	0.0106	1.7350	1.3799
B to Z ↑	0.0112	0.0119	1.4585	1.1825
	C12T28SOI_LL_-NAND2X20_P16	**C12T28SOI_LL_-NAND2X24_P16**	**C12T28SOI_LL_-NAND2X20_P16**	**C12T28SOI_LL_-NAND2X24_P16**
A to Z ↓	0.0110	0.0115	1.1721	0.9953
A to Z ↑	0.0142	0.0146	0.9729	0.8345
B to Z ↓	0.0105	0.0102	1.1875	1.0082
B to Z ↑	0.0114	0.0113	0.9825	0.8427
	C12T28SOI_LL_-NAND2X27_P16	**C12T28SOI_LL_-NAND2X42_P16**	**C12T28SOI_LL_-NAND2X27_P16**	**C12T28SOI_LL_-NAND2X42_P16**
A to Z ↓	0.0113	0.0402	0.8896	0.3998
A to Z ↑	0.0142	0.0408	0.7293	0.5727
B to Z ↓	0.0101	0.0415	0.9013	0.3999
B to Z ↑	0.0110	0.0391	0.7356	0.5732
	C12T28SOI_LL_-NAND2X47_P16	**C12T28SOI_LL_-NAND2X50_P16**	**C12T28SOI_LL_-NAND2X47_P16**	**C12T28SOI_LL_-NAND2X50_P16**
A to Z ↓	0.0413	0.0418	0.3551	0.3339
A to Z ↑	0.0415	0.0419	0.5005	0.4788
B to Z ↓	0.0427	0.0432	0.3553	0.3340
B to Z ↑	0.0398	0.0402	0.4998	0.4790
	C12T28SOI_LL_-NAND2X58_P16	**C12T28SOI_LL_-NAND2X67_P16**	**C12T28SOI_LL_-NAND2X58_P16**	**C12T28SOI_LL_-NAND2X67_P16**
A to Z ↓	0.0438	0.0453	0.2895	0.2551
A to Z ↑	0.0434	0.0444	0.4124	0.3628
B to Z ↓	0.0451	0.0467	0.2898	0.2549
B to Z ↑	0.0417	0.0428	0.4122	0.3628
	C12T28SOI_-LLBR0D8_-NAND2X7_P16	**C12T28SOI_-LLBR0D8_-NAND2X14_P16**	**C12T28SOI_-LLBR0D8_-NAND2X7_P16**	**C12T28SOI_-LLBR0D8_-NAND2X14_P16**
A to Z ↓	0.0086	0.0099	2.5274	1.3338
A to Z ↑	0.0173	0.0177	3.9179	1.9114
B to Z ↓	0.0082	0.0077	2.5722	1.3628
B to Z ↑	0.0140	0.0126	4.0532	1.9553
	C12T28SOI_LLS_-NAND2X40_P16	**C12T28SOI_LLS_-NAND2X54_P16**	**C12T28SOI_LLS_-NAND2X40_P16**	**C12T28SOI_LLS_-NAND2X54_P16**
A to Z ↓	0.0112	0.0113	0.6028	0.4566
A to Z ↑	0.0141	0.0141	0.4888	0.3686
B to Z ↓	0.0102	0.0104	0.6111	0.4627
B to Z ↑	0.0110	0.0111	0.4933	0.3726

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P16	7.864e-08	1.000e-20
C12T28SOI_LL_NAND2X5_P16	1.323e-07	1.000e-20
C12T28SOI_LL_NAND2X7_P16	1.647e-07	1.000e-20
C12T28SOI_LL_NAND2X10_P16	2.320e-07	1.000e-20
C12T28SOI_LL_NAND2X13_P16	3.220e-07	1.000e-20
C12T28SOI_LL_NAND2X17_P16	3.848e-07	1.000e-20
C12T28SOI_LL_NAND2X20_P16	4.707e-07	1.000e-20
C12T28SOI_LL_NAND2X24_P16	5.371e-07	1.000e-20
C12T28SOI_LL_NAND2X27_P16	6.196e-07	1.000e-20

C12T28SOI_LL_NAND2X42_P16	9.795e-07	1.000e-20
C12T28SOI_LL_NAND2X47_P16	1.051e-06	1.000e-20
C12T28SOI_LL_NAND2X50_P16	1.081e-06	1.000e-20
C12T28SOI_LL_NAND2X58_P16	1.182e-06	1.000e-20
C12T28SOI_LL_NAND2X67_P16	1.283e-06	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_-P16	1.706e-07	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_-P16	3.276e-07	1.000e-20
C12T28SOI_LLS_NAND2X40_P16	9.176e-07	1.000e-20
C12T28SOI_LLS_NAND2X54_P16	1.216e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND2X3_P16	C12T28SOI_LL_-NAND2X5_P16	C12T28SOI_LL_-NAND2X7_P16	C12T28SOI_LL_-NAND2X10_P16
A (output stable)	1.099e-05	1.699e-05	2.022e-05	5.154e-05
B (output stable)	4.055e-05	6.343e-05	7.670e-05	3.514e-04
A to Z	7.031e-04	9.436e-04	1.127e-03	1.988e-03
B to Z	5.589e-04	7.169e-04	8.483e-04	1.278e-03
	C12T28SOI_LL_-NAND2X13_P16	C12T28SOI_LL_-NAND2X17_P16	C12T28SOI_LL_-NAND2X20_P16	C12T28SOI_LL_-NAND2X24_P16
A (output stable)	6.352e-05	8.116e-05	9.231e-05	1.197e-04
B (output stable)	4.106e-04	4.152e-04	4.582e-04	6.905e-04
A to Z	2.447e-03	3.053e-03	3.479e-03	4.266e-03
B to Z	1.561e-03	2.076e-03	2.375e-03	2.738e-03
	C12T28SOI_LL_-NAND2X27_P16	C12T28SOI_LL_-NAND2X42_P16	C12T28SOI_LL_-NAND2X47_P16	C12T28SOI_LL_-NAND2X50_P16
A (output stable)	1.301e-04	2.203e-05	2.218e-05	2.212e-05
B (output stable)	7.466e-04	8.298e-05	8.246e-05	8.309e-05
A to Z	4.684e-03	1.238e-02	1.333e-02	1.380e-02
B to Z	3.026e-03	1.209e-02	1.305e-02	1.351e-02
	C12T28SOI_LL_-NAND2X58_P16	C12T28SOI_LL_-NAND2X67_P16	C12T28SOI_-LLBR0D8_-NAND2X7_P16	C12T28SOI_-LLBR0D8_-NAND2X14_P16
A (output stable)	2.223e-05	2.234e-05	2.587e-05	7.960e-05
B (output stable)	8.320e-05	8.316e-05	1.022e-04	5.138e-04
A to Z	1.567e-02	1.717e-02	1.184e-03	2.569e-03
B to Z	1.539e-02	1.689e-02	7.952e-04	1.410e-03
	C12T28SOI_LLS_-NAND2X40_P16	C12T28SOI_LLS_-NAND2X54_P16		
A (output stable)	1.870e-04	2.501e-04		
B (output stable)	1.024e-03	1.314e-03		
A to Z	6.917e-03	9.137e-03		
B to Z	4.540e-03	6.037e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND2X3_P16	C12T28SOI_LL_-NAND2X5_P16	C12T28SOI_LL_-NAND2X7_P16	C12T28SOI_LL_-NAND2X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

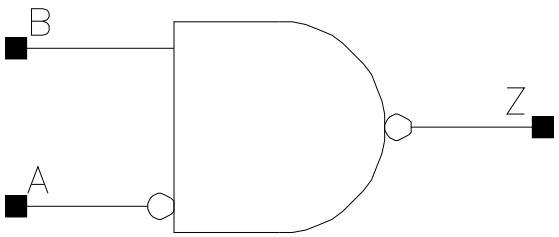
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X13_P16	C12T28SOI_LL_-NAND2X17_P16	C12T28SOI_LL_-NAND2X20_P16	C12T28SOI_LL_-NAND2X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P16	C12T28SOI_LL_-NAND2X42_P16	C12T28SOI_LL_-NAND2X47_P16	C12T28SOI_LL_-NAND2X50_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P16	C12T28SOI_LL_-NAND2X67_P16	C12T28SOI_-LLBR0D8_-NAND2X7_P16	C12T28SOI_-LLBR0D8_-NAND2X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P16	C12T28SOI_LLS_-NAND2X54_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X7_P16	1.200	0.544	0.6528
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X40_P16	1.200	2.312	2.7744
X54_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P16	X7_P16	X13_P16	X27_P16
A	0.0009	0.0009	0.0013	0.0023
B	0.0006	0.0009	0.0017	0.0035
	X40_P16	X54_P16		
A	0.0035	0.0046		
B	0.0052	0.0070		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0289	0.0310	6.0950	3.3273
A to Z ↑	0.0231	0.0243	5.6093	2.8890
B to Z ↓	0.0123	0.0105	6.2745	3.4043
B to Z ↑	0.0145	0.0120	5.8243	2.9971
	X13_P16	**X27_P16**	**X13_P16**	**X27_P16**

A to Z ↓	0.0288	0.0279	1.7925	0.8902
A to Z ↑	0.0233	0.0227	1.4910	0.7203
B to Z ↓	0.0099	0.0099	1.8402	0.9143
B to Z ↑	0.0111	0.0108	1.4957	0.7374
	X40_P16	**X54_P16**	**X40_P16**	**X54_P16**
A to Z ↓	0.0284	0.0283	0.5947	0.4512
A to Z ↑	0.0233	0.0231	0.4793	0.3619
B to Z ↓	0.0099	0.0100	0.6104	0.4630
B to Z ↑	0.0108	0.0108	0.4959	0.3745

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.357e-07	1.000e-20
X7_P16	2.225e-07	1.000e-20
X13_P16	4.570e-07	1.000e-20
X27_P16	8.909e-07	1.000e-20
X40_P16	1.310e-06	1.000e-20
X54_P16	1.729e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	1.132e-03	1.477e-03	2.526e-03	4.868e-03
B (output stable)	4.110e-05	7.677e-05	3.771e-04	6.594e-04
A to Z	1.926e-03	2.714e-03	4.993e-03	9.792e-03
B to Z	5.659e-04	8.425e-04	1.526e-03	3.026e-03
	X40_P16	X54_P16		
A (output stable)	7.500e-03	9.852e-03		
B (output stable)	9.540e-04	1.268e-03		
A to Z	1.476e-02	1.942e-02		
B to Z	4.381e-03	5.773e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

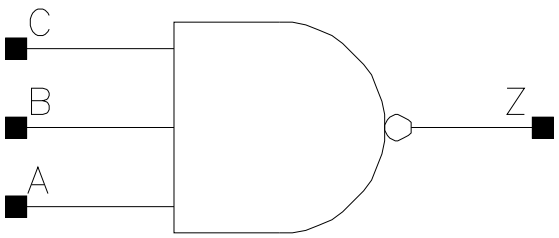
Pin Cycle (vdds)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P16	X54_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P16	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P16	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P16	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P16	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P16	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P16	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P16	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P16	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P16	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P16	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P16	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P16	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P16	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P16	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P16	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A	0.0008	0.0010	0.0016	0.0019
B	0.0008	0.0010	0.0015	0.0018
C	0.0007	0.0009	0.0014	0.0018
	C12T28SOI_LL_-NAND3X15_P16	C12T28SOI_LL_-NAND3X18_P16	C12T28SOI_LL_-NAND3X21_P16	C12T28SOI_LL_-NAND3X24_P16
A	0.0025	0.0029	0.0034	0.0038
B	0.0024	0.0027	0.0032	0.0036
C	0.0023	0.0026	0.0031	0.0035
	C12T28SOI_LL_-NAND3X35_P16	C12T28SOI_LL_-NAND3X47_P16	C12T28SOI_-LLBR0P6_-NAND3X6_P16	C12T28SOI_-LLBR0P6_-NAND3X12_P16
A	0.0057	0.0076	0.0010	0.0020
B	0.0055	0.0073	0.0010	0.0018
C	0.0052	0.0070	0.0009	0.0017
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	C12T28SOI_-LLBR0P6_-NAND3X24_P16	C12T28SOI_-LLBR0P6_-NAND3X35_P16	C12T28SOI_-LLBR0P6_-NAND3X47_P16
A	0.0029	0.0038	0.0057	0.0076
B	0.0027	0.0036	0.0054	0.0072
C	0.0025	0.0034	0.0050	0.0067
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16			
A	0.0030			
B	0.0028			
C	0.0026			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16
A to Z ↓	0.0178	0.0163	6.4678	4.6578
A to Z ↑	0.0204	0.0185	4.1769	2.8548
B to Z ↓	0.0188	0.0169	6.4911	4.6726
B to Z ↑	0.0193	0.0173	4.1872	2.8612
C to Z ↓	0.0165	0.0150	6.5271	4.6998
C to Z ↑	0.0165	0.0145	4.1895	2.8829

	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A to Z ↓	0.0180	0.0170	3.1560	2.4644
A to Z ↑	0.0194	0.0181	1.9556	1.4622
B to Z ↓	0.0170	0.0160	3.1680	2.4737
B to Z ↑	0.0175	0.0164	1.9596	1.4654
C to Z ↓	0.0150	0.0141	3.1877	2.4884
C to Z ↑	0.0146	0.0134	1.9544	1.4535
	C12T28SOI_LL_-NAND3X15_P16	**C12T28SOI_LL_-NAND3X18_P16**	**C12T28SOI_LL_-NAND3X15_P16**	**C12T28SOI_LL_-NAND3X18_P16**
A to Z ↓	0.0163	0.0160	1.9875	1.7048
A to Z ↑	0.0179	0.0173	1.1711	0.9710
B to Z ↓	0.0160	0.0157	1.9953	1.7117
B to Z ↑	0.0161	0.0156	1.1742	0.9737
C to Z ↓	0.0144	0.0140	2.0074	1.7211
C to Z ↑	0.0134	0.0128	1.1842	0.9820
	C12T28SOI_LL_-NAND3X21_P16	**C12T28SOI_LL_-NAND3X24_P16**	**C12T28SOI_LL_-NAND3X21_P16**	**C12T28SOI_LL_-NAND3X24_P16**
A to Z ↓	0.0168	0.0165	1.4372	1.2883
A to Z ↑	0.0180	0.0175	0.8400	0.7353
B to Z ↓	0.0160	0.0158	1.4438	1.2936
B to Z ↑	0.0162	0.0158	0.8418	0.7366
C to Z ↓	0.0143	0.0141	1.4517	1.3015
C to Z ↑	0.0134	0.0129	0.8438	0.7376
	C12T28SOI_LL_-NAND3X35_P16	**C12T28SOI_LL_-NAND3X47_P16**	**C12T28SOI_LL_-NAND3X35_P16**	**C12T28SOI_LL_-NAND3X47_P16**
A to Z ↓	0.0160	0.0163	0.8792	0.6688
A to Z ↑	0.0172	0.0174	0.4923	0.3722
B to Z ↓	0.0157	0.0157	0.8826	0.6718
B to Z ↑	0.0154	0.0155	0.4924	0.3713
C to Z ↓	0.0140	0.0141	0.8883	0.6759
C to Z ↑	0.0126	0.0126	0.4959	0.3738
	C12T28SOI_-LLBR0P6_-NAND3X6_P16	**C12T28SOI_-LLBR0P6_-NAND3X12_P16**	**C12T28SOI_-LLBR0P6_-NAND3X6_P16**	**C12T28SOI_-LLBR0P6_-NAND3X12_P16**
A to Z ↓	0.0133	0.0140	3.1571	1.6745
A to Z ↑	0.0259	0.0258	4.5171	2.3049
B to Z ↓	0.0132	0.0125	3.1798	1.6882
B to Z ↑	0.0232	0.0220	4.5281	2.3113
C to Z ↓	0.0105	0.0095	3.2206	1.7109
C to Z ↑	0.0177	0.0160	4.5613	2.3204
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	**C12T28SOI_-LLBR0P6_-NAND3X24_P16**	**C12T28SOI_-LLBR0P6_-NAND3X18_P16**	**C12T28SOI_-LLBR0P6_-NAND3X24_P16**
A to Z ↓	0.0131	0.0136	1.1617	0.8791
A to Z ↑	0.0245	0.0249	1.5320	1.1577
B to Z ↓	0.0122	0.0123	1.1705	0.8865
B to Z ↑	0.0208	0.0212	1.5373	1.1606
C to Z ↓	0.0096	0.0094	1.1853	0.8982
C to Z ↑	0.0154	0.0154	1.5510	1.1639
	C12T28SOI_-LLBR0P6_-NAND3X35_P16	**C12T28SOI_-LLBR0P6_-NAND3X47_P16**	**C12T28SOI_-LLBR0P6_-NAND3X35_P16**	**C12T28SOI_-LLBR0P6_-NAND3X47_P16**

A to Z ↓	0.0132	0.0135	0.6020	0.4603
A to Z ↑	0.0249	0.0250	0.7970	0.6031
B to Z ↓	0.0123	0.0125	0.6071	0.4643
B to Z ↑	0.0211	0.0211	0.7984	0.6034
C to Z ↓	0.0094	0.0098	0.6156	0.4703
C to Z ↑	0.0153	0.0156	0.8096	0.6070
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P16**	
A to Z ↓	0.0142		1.1383	
A to Z ↑	0.0246		1.4376	
B to Z ↓	0.0125		1.1465	
B to Z ↑	0.0209		1.4411	
C to Z ↓	0.0093		1.1621	
C to Z ↑	0.0151		1.4313	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P16	1.162e-07	1.000e-20
C12T28SOI_LL_NAND3X6_P16	1.732e-07	1.000e-20
C12T28SOI_LL_NAND3X9_P16	2.394e-07	1.000e-20
C12T28SOI_LL_NAND3X12_P16	3.277e-07	1.000e-20
C12T28SOI_LL_NAND3X15_P16	3.841e-07	1.000e-20
C12T28SOI_LL_NAND3X18_P16	4.673e-07	1.000e-20
C12T28SOI_LL_NAND3X21_P16	5.476e-07	1.000e-20
C12T28SOI_LL_NAND3X24_P16	6.294e-07	1.000e-20
C12T28SOI_LL_NAND3X35_P16	9.335e-07	1.000e-20
C12T28SOI_LL_NAND3X47_P16	1.235e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_-P16	1.875e-07	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P16	3.490e-07	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P16	4.880e-07	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P16	6.607e-07	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P16	9.759e-07	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P16	1.287e-06	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P16	5.648e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A (output stable)	1.729e-05	2.359e-05	4.305e-05	5.561e-05
B (output stable)	8.418e-05	1.082e-04	1.897e-04	2.291e-04
C (output stable)	8.824e-05	1.100e-04	1.496e-04	1.795e-04
A to Z	1.614e-03	2.000e-03	3.225e-03	3.842e-03
B to Z	1.424e-03	1.719e-03	2.567e-03	3.056e-03
C to Z	1.070e-03	1.284e-03	1.859e-03	2.199e-03

	C12T28SOI_LL_-NAND3X15_P16	C12T28SOI_LL_-NAND3X18_P16	C12T28SOI_LL_-NAND3X21_P16	C12T28SOI_LL_-NAND3X24_P16
A (output stable)	4.476e-05	5.035e-05	8.242e-05	9.222e-05
B (output stable)	2.647e-04	3.054e-04	3.805e-04	4.195e-04
C (output stable)	1.901e-04	2.209e-04	2.892e-04	3.102e-04
A to Z	4.601e-03	5.228e-03	6.565e-03	7.187e-03
B to Z	3.655e-03	4.141e-03	5.200e-03	5.703e-03
C to Z	2.686e-03	3.018e-03	3.771e-03	4.098e-03
	C12T28SOI_LL_-NAND3X35_P16	C12T28SOI_LL_-NAND3X47_P16	C12T28SOI_-LLBR0P6_-NAND3X6_P16	C12T28SOI_-LLBR0P6_-NAND3X12_P16
A (output stable)	1.029e-04	1.404e-04	3.034e-05	6.899e-05
B (output stable)	6.051e-04	7.815e-04	1.549e-04	3.384e-04
C (output stable)	4.588e-04	5.831e-04	1.539e-04	2.641e-04
A to Z	1.039e-02	1.375e-02	2.202e-03	4.328e-03
B to Z	8.187e-03	1.079e-02	1.771e-03	3.148e-03
C to Z	5.799e-03	7.732e-03	1.118e-03	1.821e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	C12T28SOI_-LLBR0P6_-NAND3X24_P16	C12T28SOI_-LLBR0P6_-NAND3X35_P16	C12T28SOI_-LLBR0P6_-NAND3X47_P16
A (output stable)	6.768e-05	1.207e-04	1.415e-04	1.884e-04
B (output stable)	4.451e-04	6.195e-04	8.867e-04	1.136e-03
C (output stable)	3.085e-04	4.639e-04	6.917e-04	8.803e-04
A to Z	5.865e-03	8.071e-03	1.171e-02	1.536e-02
B to Z	4.233e-03	5.851e-03	8.461e-03	1.116e-02
C to Z	2.536e-03	3.392e-03	4.782e-03	6.391e-03
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16			
A (output stable)	9.968e-05			
B (output stable)	5.127e-04			
C (output stable)	3.985e-04			
A to Z	6.398e-03			
B to Z	4.651e-03			
C to Z	2.667e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P16	C12T28SOI_LL_-NAND3X18_P16	C12T28SOI_LL_-NAND3X21_P16	C12T28SOI_LL_-NAND3X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

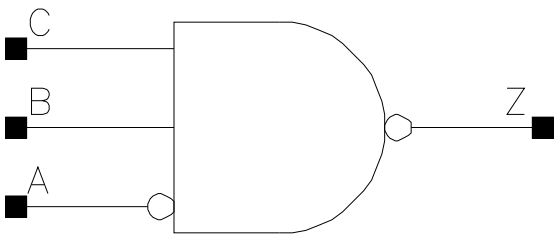
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P16	C12T28SOI_LL_-NAND3X47_P16	C12T28SOI_-LLBR0P6_-NAND3X6_P16	C12T28SOI_-LLBR0P6_-NAND3X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	C12T28SOI_-LLBR0P6_-NAND3X24_P16	C12T28SOI_-LLBR0P6_-NAND3X35_P16	C12T28SOI_-LLBR0P6_-NAND3X47_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.816	0.9792
X12_P16	1.200	1.224	1.4688
X18_P16	1.200	1.496	1.7952
X24_P16	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0009	0.0013	0.0013	0.0023
B	0.0009	0.0019	0.0027	0.0036
C	0.0009	0.0018	0.0026	0.0034

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X12_P16**	**X6_P16**	**X12_P16**
A to Z ↓	0.0351	0.0338	4.6554	2.4851
A to Z ↑	0.0260	0.0255	2.8064	1.4084
B to Z ↓	0.0145	0.0155	4.6997	2.5075
B to Z ↑	0.0156	0.0156	2.8717	1.4449
C to Z ↓	0.0144	0.0132	4.7281	2.5220
C to Z ↑	0.0136	0.0125	2.8913	1.4574
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0387	0.0328	1.7035	1.2903

A to Z ↑	0.0294	0.0243	0.9494	0.7113
B to Z ↓	0.0156	0.0152	1.7153	1.3015
B to Z ↑	0.0155	0.0152	0.9740	0.7325
C to Z ↓	0.0141	0.0132	1.7250	1.3096
C to Z ↑	0.0129	0.0122	0.9826	0.7394

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P16	2.239e-07	1.000e-20
X12_P16	4.621e-07	1.000e-20
X18_P16	5.970e-07	1.000e-20
X24_P16	9.103e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	1.429e-03	2.539e-03	3.504e-03	4.757e-03
B (output stable)	3.015e-05	1.035e-04	1.587e-04	2.381e-04
C (output stable)	7.572e-05	2.596e-04	3.076e-04	4.957e-04
A to Z	3.299e-03	6.517e-03	9.378e-03	1.246e-02
B to Z	1.407e-03	2.827e-03	4.155e-03	5.314e-03
C to Z	1.120e-03	1.940e-03	3.012e-03	3.649e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

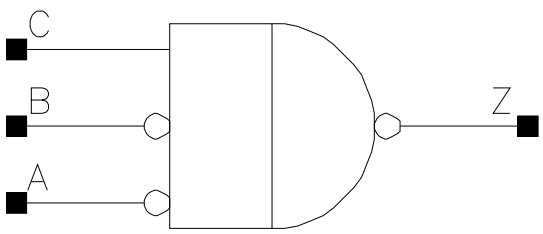
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	0.816	0.9792
X13_P16	1.200	1.088	1.3056
X20_P16	1.200	1.632	1.9584
X27_P16	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P16	X13_P16	X20_P16	X27_P16
A	0.0011	0.0011	0.0023	0.0021
B	0.0013	0.0012	0.0023	0.0022
C	0.0009	0.0018	0.0026	0.0035

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	**X13_P16**	**X7_P16**	**X13_P16**
A to Z ↓	0.0324	0.0397	3.2015	1.7071
A to Z ↑	0.0226	0.0261	2.7795	1.4000
B to Z ↓	0.0326	0.0402	3.2014	1.7075
B to Z ↑	0.0211	0.0247	2.7745	1.3991
C to Z ↓	0.0104	0.0098	3.2710	1.7377
C to Z ↑	0.0119	0.0110	2.8840	1.4569
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0366	0.0400	1.1632	0.8856
A to Z ↑	0.0242	0.0289	0.9445	0.7094
B to Z ↓	0.0345	0.0389	1.1632	0.8860

B to Z ↑	0.0221	0.0272	0.9436	0.7082
C to Z ↓	0.0108	0.0103	1.1871	0.9018
C to Z ↑	0.0117	0.0113	0.9818	0.7378

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X7_P16	3.105e-07	1.000e-20
X13_P16	4.223e-07	1.000e-20
X20_P16	6.919e-07	1.000e-20
X27_P16	7.636e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	8.193e-04	1.152e-03	1.932e-03	2.280e-03
B (output stable)	6.628e-04	9.604e-04	1.419e-03	1.802e-03
C (output stable)	7.329e-05	2.332e-04	2.771e-04	3.633e-04
A to Z	3.640e-03	5.995e-03	9.521e-03	1.182e-02
B to Z	3.252e-03	5.617e-03	8.275e-03	1.076e-02
C to Z	8.741e-04	1.528e-03	2.507e-03	3.277e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

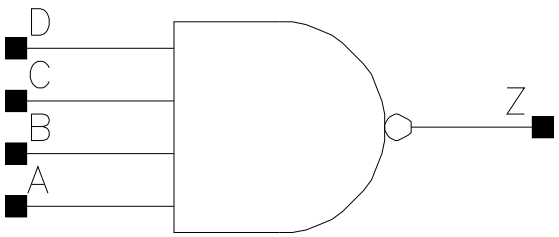
Pin Cycle (vdds)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0008	0.0007	0.0009	0.0011
B	0.0008	0.0008	0.0010	0.0013
C	0.0007	0.0008	0.0010	0.0012
D	0.0008	0.0008	0.0010	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0517	0.0511	1.9381	0.9693
A to Z ↑	0.0418	0.0453	2.8411	1.4112
B to Z ↓	0.0532	0.0535	1.9359	0.9682
B to Z ↑	0.0400	0.0445	2.8443	1.4122
C to Z ↓	0.0517	0.0505	1.9375	0.9680
C to Z ↑	0.0425	0.0468	2.8436	1.4094

D to Z ↓	0.0536	0.0522	1.9376	0.9686
D to Z ↑	0.0413	0.0450	2.8440	1.4106
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0545	0.0505	0.6697	0.5008
A to Z ↑	0.0439	0.0432	0.9519	0.7139
B to Z ↓	0.0563	0.0520	0.6696	0.5011
B to Z ↑	0.0425	0.0417	0.9518	0.7143
C to Z ↓	0.0503	0.0466	0.6698	0.5006
C to Z ↑	0.0441	0.0430	0.9502	0.7124
D to Z ↓	0.0521	0.0482	0.6694	0.5006
D to Z ↑	0.0423	0.0414	0.9512	0.7127

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	3.382e-07	1.000e-20
X17_P16	5.075e-07	1.000e-20
X25_P16	7.561e-07	1.000e-20
X33_P16	9.822e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	5.783e-04	7.276e-04	1.091e-03	1.278e-03
B (output stable)	5.283e-04	6.846e-04	1.013e-03	1.184e-03
C (output stable)	5.678e-04	6.932e-04	1.060e-03	1.212e-03
D (output stable)	5.168e-04	6.364e-04	9.367e-04	1.069e-03
A to Z	4.249e-03	6.489e-03	1.010e-02	1.244e-02
B to Z	4.099e-03	6.347e-03	9.879e-03	1.215e-02
C to Z	4.321e-03	6.337e-03	9.399e-03	1.149e-02
D to Z	4.179e-03	6.182e-03	9.173e-03	1.121e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

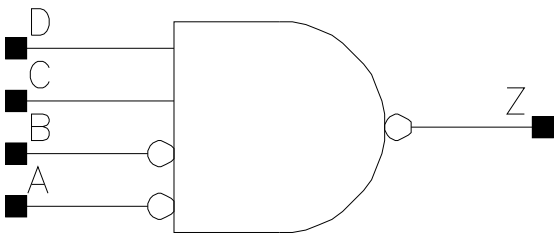
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X12_P16	1.200	1.496	1.7952
X18_P16	1.200	2.040	2.4480
X24_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0012	0.0012	0.0023	0.0021
B	0.0012	0.0016	0.0023	0.0022
C	0.0009	0.0019	0.0027	0.0037
D	0.0009	0.0018	0.0025	0.0035

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X12_P16	X6_P16	X12_P16
A to Z ↓	0.0347	0.0466	4.8017	2.4915
A to Z ↑	0.0239	0.0291	2.7818	1.4028
B to Z ↓	0.0342	0.0461	4.8038	2.4925
B to Z ↑	0.0215	0.0274	2.7797	1.4015
C to Z ↓	0.0146	0.0154	4.8456	2.5050
C to Z ↑	0.0158	0.0156	3.0704	1.4446

D to Z ↓	0.0142	0.0133	4.8724	2.5203
D to Z ↑	0.0137	0.0125	3.0911	1.4573
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0406	0.0451	1.6996	1.2926
A to Z ↑	0.0257	0.0325	0.9451	0.7104
B to Z ↓	0.0387	0.0438	1.7000	1.2930
B to Z ↑	0.0236	0.0304	0.9445	0.7094
C to Z ↓	0.0153	0.0157	1.7117	1.2995
C to Z ↑	0.0154	0.0156	0.9782	0.7306
D to Z ↓	0.0138	0.0139	1.7211	1.3074
D to Z ↑	0.0128	0.0127	1.0017	0.7378

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P16	2.893e-07	1.000e-20
X12_P16	4.255e-07	1.000e-20
X18_P16	6.897e-07	1.000e-20
X24_P16	7.510e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	9.252e-04	1.571e-03	2.370e-03	2.862e-03
B (output stable)	7.377e-04	1.312e-03	1.839e-03	2.357e-03
C (output stable)	6.012e-05	1.655e-04	2.371e-04	3.286e-04
D (output stable)	6.714e-05	2.218e-04	2.538e-04	3.733e-04
A to Z	3.904e-03	7.459e-03	1.102e-02	1.440e-02
B to Z	3.519e-03	6.902e-03	9.851e-03	1.326e-02
C to Z	1.364e-03	2.811e-03	4.048e-03	5.635e-03
D to Z	1.074e-03	1.926e-03	2.963e-03	3.985e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

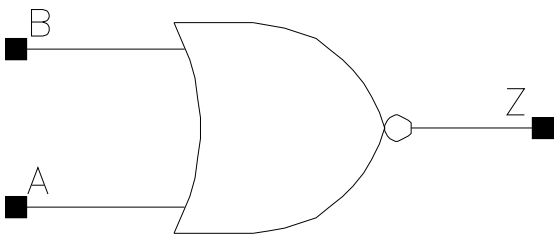
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.408	0.4896
X5_P16	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X10_P16	1.200	0.680	0.8160
X14_P16	1.200	0.680	0.8160
X17_P16	1.200	0.952	1.1424
X21_P16	1.200	0.952	1.1424
X24_P16	1.200	1.224	1.4688
X27_P16	1.200	1.224	1.4688
X34_P16	1.200	1.496	1.7952
X40_P16	1.200	1.360	1.6320
X41_P16	1.200	1.768	2.1216
X49_P16	1.200	1.496	1.7952
X53_P16	1.200	1.904	2.2848
X55_P16	1.200	2.312	2.7744
X57_P16	1.200	1.904	2.2848
X65_P16	1.200	2.040	2.4480
X84_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P16	X5_P16	X7_P16	X10_P16
A	0.0006	0.0008	0.0010	0.0016
B	0.0006	0.0007	0.0010	0.0014
	X14_P16	X17_P16	X21_P16	X24_P16

A	0.0020	0.0026	0.0029	0.0034
B	0.0018	0.0023	0.0027	0.0032
	X27_P16	X34_P16	X40_P16	X41_P16
A	0.0038	0.0048	0.0011	0.0059
B	0.0035	0.0044	0.0012	0.0053
	X49_P16	X53_P16	X55_P16	X57_P16
A	0.0011	0.0012	0.0078	0.0012
B	0.0012	0.0011	0.0070	0.0011
	X65_P16	X84_P16		
A	0.0012	0.0013		
B	0.0011	0.0012		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X5_P16**	**X3_P16**	**X5_P16**
A to Z ↓	0.0107	0.0102	3.7073	2.6917
A to Z ↑	0.0183	0.0169	10.9002	7.9133
B to Z ↓	0.0093	0.0085	3.8023	2.7167
B to Z ↑	0.0178	0.0161	10.9765	7.9554
	X7_P16	**X10_P16**	**X7_P16**	**X10_P16**
A to Z ↓	0.0100	0.0105	1.9848	1.2859
A to Z ↑	0.0159	0.0184	5.5587	3.7296
B to Z ↓	0.0082	0.0075	2.0122	1.3024
B to Z ↑	0.0149	0.0140	5.5915	3.7596
	X14_P16	**X17_P16**	**X14_P16**	**X17_P16**
A to Z ↓	0.0103	0.0104	0.9804	0.7892
A to Z ↑	0.0171	0.0172	2.7534	2.2334
B to Z ↓	0.0073	0.0081	0.9938	0.7986
B to Z ↑	0.0131	0.0143	2.7765	2.2502
	X21_P16	**X24_P16**	**X21_P16**	**X24_P16**
A to Z ↓	0.0104	0.0103	0.6708	0.5712
A to Z ↑	0.0165	0.0169	1.8552	1.6253
B to Z ↓	0.0080	0.0076	0.6790	0.5790
B to Z ↑	0.0138	0.0136	1.8682	1.6377
	X27_P16	**X34_P16**	**X27_P16**	**X34_P16**
A to Z ↓	0.0102	0.0106	0.5075	0.4101
A to Z ↑	0.0165	0.0166	1.4270	1.1353
B to Z ↓	0.0076	0.0079	0.5148	0.4155
B to Z ↑	0.0132	0.0137	1.4384	1.1438
	X40_P16	**X41_P16**	**X40_P16**	**X41_P16**
A to Z ↓	0.0360	0.0104	0.4084	0.3415
A to Z ↑	0.0488	0.0165	0.5871	0.9395
B to Z ↓	0.0346	0.0077	0.4079	0.3464
B to Z ↑	0.0495	0.0131	0.5869	0.9470
	X49_P16	**X53_P16**	**X49_P16**	**X53_P16**
A to Z ↓	0.0377	0.0393	0.3394	0.3107
A to Z ↑	0.0505	0.0574	0.4878	0.4515
B to Z ↓	0.0362	0.0378	0.3395	0.3105
B to Z ↑	0.0511	0.0578	0.4879	0.4517
	X55_P16	**X57_P16**	**X55_P16**	**X57_P16**
A to Z ↓	0.0105	0.0396	0.2582	0.2924
A to Z ↑	0.0165	0.0576	0.7078	0.4199

B to Z ↓	0.0077	0.0381	0.2624	0.2925
B to Z ↑	0.0132	0.0580	0.7141	0.4200
	X65_P16	**X84_P16**	**X65_P16**	**X84_P16**
A to Z ↓	0.0405	0.0423	0.2567	0.2043
A to Z ↑	0.0584	0.0593	0.3677	0.2915
B to Z ↓	0.0390	0.0408	0.2566	0.2042
B to Z ↑	0.0588	0.0597	0.3678	0.2917

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	8.218e-08	1.000e-20
X5_P16	1.185e-07	1.000e-20
X7_P16	1.726e-07	1.000e-20
X10_P16	2.443e-07	1.000e-20
X14_P16	3.396e-07	1.000e-20
X17_P16	4.062e-07	1.000e-20
X21_P16	4.976e-07	1.000e-20
X24_P16	5.677e-07	1.000e-20
X27_P16	6.560e-07	1.000e-20
X34_P16	8.143e-07	1.000e-20
X40_P16	1.070e-06	1.000e-20
X41_P16	9.727e-07	1.000e-20
X49_P16	1.208e-06	1.000e-20
X53_P16	1.399e-06	1.000e-20
X55_P16	1.289e-06	1.000e-20
X57_P16	1.479e-06	1.000e-20
X65_P16	1.618e-06	1.000e-20
X84_P16	1.930e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	2.535e-05	3.276e-05	4.518e-05	1.354e-04
B (output stable)	4.781e-06	5.890e-06	8.534e-06	6.244e-05
A to Z	7.357e-04	9.031e-04	1.195e-03	2.109e-03
B to Z	5.310e-04	6.283e-04	8.133e-04	1.121e-03
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	1.611e-04	1.909e-04	2.175e-04	2.639e-04
B (output stable)	7.131e-05	8.425e-05	9.010e-05	9.918e-05
A to Z	2.607e-03	3.263e-03	3.760e-03	4.436e-03
B to Z	1.403e-03	1.944e-03	2.231e-03	2.510e-03
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	2.894e-04	3.473e-04	4.611e-05	4.517e-04
B (output stable)	1.038e-04	1.086e-04	8.463e-06	1.732e-04
A to Z	4.907e-03	6.173e-03	1.207e-02	7.415e-03
B to Z	2.767e-03	3.674e-03	1.171e-02	4.148e-03
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	4.642e-05	4.699e-05	5.892e-04	4.698e-05
B (output stable)	8.412e-06	8.525e-06	2.279e-04	8.516e-06
A to Z	1.365e-02	1.678e-02	9.814e-03	1.727e-02
B to Z	1.329e-02	1.638e-02	5.527e-03	1.687e-02
	X65_P16	X84_P16		

A (output stable)	4.707e-05	4.842e-05		
B (output stable)	8.622e-06	9.528e-06		
A to Z	1.868e-02	2.214e-02		
B to Z	1.828e-02	2.167e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

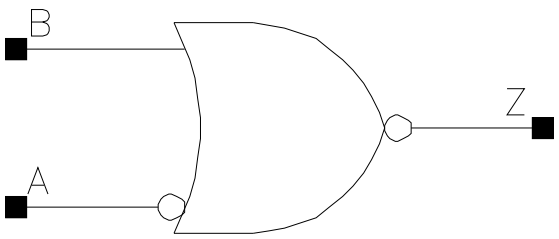
Pin Cycle (vdds)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P16	X84_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X7_P16	1.200	0.680	0.8160
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X41_P16	1.200	2.312	2.7744
X55_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X7_P16	X13_P16
A	0.0009	0.0009	0.0009	0.0013
B	0.0006	0.0009	0.0009	0.0017
	X27_P16	X41_P16	X55_P16	
A	0.0024	0.0035	0.0046	
B	0.0036	0.0053	0.0070	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0274	0.0306	3.5421	2.3330
A to Z ↑	0.0260	0.0263	10.7826	5.5158
B to Z ↓	0.0096	0.0094	3.7726	2.5014
B to Z ↑	0.0179	0.0148	10.9499	5.6083

	X7_P16	X13_P16	X7_P16	X13_P16
A to Z ↓	0.0310	0.0278	1.8576	1.0143
A to Z ↑	0.0285	0.0273	5.4666	2.9195
B to Z ↓	0.0087	0.0078	1.9256	1.0456
B to Z ↑	0.0161	0.0144	5.5371	2.9613
	X27_P16	**X41_P16**	**X27_P16**	**X41_P16**
A to Z ↓	0.0270	0.0275	0.4842	0.3280
A to Z ↑	0.0262	0.0265	1.3911	0.9342
B to Z ↓	0.0076	0.0077	0.5174	0.3488
B to Z ↑	0.0136	0.0134	1.4128	0.9485
	X55_P16		**X55_P16**	
A to Z ↓	0.0272		0.2482	
A to Z ↑	0.0263		0.7050	
B to Z ↓	0.0077		0.2642	
B to Z ↑	0.0133		0.7160	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.394e-07	1.000e-20
X6_P16	2.150e-07	1.000e-20
X7_P16	2.492e-07	1.000e-20
X13_P16	4.710e-07	1.000e-20
X27_P16	9.272e-07	1.000e-20
X41_P16	1.365e-06	1.000e-20
X55_P16	1.803e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	1.116e-03	1.429e-03	1.534e-03	2.488e-03
B (output stable)	8.719e-06	2.596e-05	2.423e-05	4.984e-05
A to Z	1.932e-03	2.703e-03	3.144e-03	5.277e-03
B to Z	5.428e-04	7.973e-04	9.842e-04	1.549e-03
	X27_P16	X41_P16	X55_P16	
A (output stable)	4.888e-03	7.429e-03	9.745e-03	
B (output stable)	1.123e-04	1.708e-04	2.312e-04	
A to Z	1.049e-02	1.564e-02	2.064e-02	
B to Z	2.979e-03	4.336e-03	5.700e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

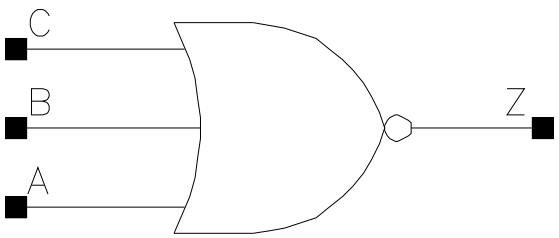
Pin Cycle (vdds)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P16	X41_P16	X55_P16	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X9_P16	1.200	0.952	1.1424
X13_P16	1.200	0.952	1.1424
X16_P16	1.200	1.360	1.6320
X19_P16	1.200	1.496	1.7952
X22_P16	1.200	1.768	2.1216
X25_P16	1.200	1.904	2.2848
X37_P16	1.200	2.584	3.1008
X49_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P16	X6_P16	X9_P16	X13_P16
A	0.0008	0.0010	0.0015	0.0019
B	0.0008	0.0009	0.0017	0.0020
C	0.0008	0.0009	0.0014	0.0017
	X16_P16	X19_P16	X22_P16	X25_P16
A	0.0025	0.0029	0.0034	0.0038
B	0.0025	0.0033	0.0036	0.0043
C	0.0022	0.0026	0.0031	0.0034
	X37_P16	X49_P16		
A	0.0057	0.0077		
B	0.0059	0.0078		

C	0.0051	0.0070		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0125	0.0120	2.7252	2.0112
A to Z ↑	0.0252	0.0231	11.6999	8.2395
B to Z ↓	0.0116	0.0111	2.7312	2.0149
B to Z ↑	0.0236	0.0214	11.7222	8.2567
C to Z ↓	0.0101	0.0093	2.7569	2.0370
C to Z ↑	0.0215	0.0190	11.7602	8.2843
	X9_P16	**X13_P16**	**X9_P16**	**X13_P16**
A to Z ↓	0.0124	0.0122	1.3260	1.0211
A to Z ↑	0.0256	0.0240	5.5002	4.0909
B to Z ↓	0.0115	0.0111	1.2929	0.9793
B to Z ↑	0.0253	0.0231	5.5109	4.0995
C to Z ↓	0.0088	0.0085	1.3058	0.9980
C to Z ↑	0.0178	0.0166	5.5292	4.1133
	X16_P16	**X19_P16**	**X16_P16**	**X19_P16**
A to Z ↓	0.0123	0.0120	0.7938	0.6706
A to Z ↑	0.0245	0.0240	3.3197	2.7404
B to Z ↓	0.0117	0.0115	0.7965	0.6563
B to Z ↑	0.0235	0.0237	3.3236	2.7448
C to Z ↓	0.0091	0.0089	0.8022	0.6845
C to Z ↑	0.0185	0.0175	3.3364	2.7557
	X22_P16	**X25_P16**	**X22_P16**	**X25_P16**
A to Z ↓	0.0123	0.0121	0.5820	0.5111
A to Z ↑	0.0243	0.0241	2.3686	2.0596
B to Z ↓	0.0114	0.0113	0.5724	0.4920
B to Z ↑	0.0234	0.0238	2.3726	2.0631
C to Z ↓	0.0086	0.0086	0.5793	0.5123
C to Z ↑	0.0172	0.0167	2.3824	2.0711
	X37_P16	**X49_P16**	**X37_P16**	**X49_P16**
A to Z ↓	0.0122	0.0123	0.3520	0.2664
A to Z ↑	0.0234	0.0235	1.3813	1.0406
B to Z ↓	0.0113	0.0114	0.3483	0.2639
B to Z ↑	0.0224	0.0223	1.3837	1.0420
C to Z ↓	0.0089	0.0091	0.3533	0.2677
C to Z ↑	0.0168	0.0171	1.3885	1.0463

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	1.250e-07	1.000e-20
X6_P16	1.801e-07	1.000e-20
X9_P16	2.614e-07	1.000e-20
X13_P16	3.607e-07	1.000e-20
X16_P16	4.363e-07	1.000e-20
X19_P16	5.452e-07	1.000e-20
X22_P16	6.111e-07	1.000e-20
X25_P16	7.197e-07	1.000e-20
X37_P16	1.045e-06	1.000e-20

X49_P16	1.389e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	1.461e-04	1.994e-04	4.337e-04	5.398e-04
B (output stable)	-4.714e-06	-1.137e-05	1.347e-04	1.302e-04
C (output stable)	3.803e-06	5.517e-06	2.884e-05	3.212e-05
A to Z	1.371e-03	1.752e-03	2.963e-03	3.684e-03
B to Z	1.089e-03	1.363e-03	2.438e-03	2.954e-03
C to Z	8.077e-04	9.674e-04	1.375e-03	1.685e-03
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	6.123e-04	7.616e-04	9.169e-04	1.071e-03
B (output stable)	9.481e-05	1.341e-04	1.994e-04	2.408e-04
C (output stable)	3.258e-05	3.921e-05	5.090e-05	5.749e-05
A to Z	4.670e-03	5.529e-03	6.453e-03	7.376e-03
B to Z	3.740e-03	4.499e-03	5.176e-03	6.011e-03
C to Z	2.388e-03	2.682e-03	3.055e-03	3.390e-03
	X37_P16	X49_P16		
A (output stable)	1.499e-03	1.975e-03		
B (output stable)	2.512e-04	3.113e-04		
C (output stable)	8.509e-05	1.094e-04		
A to Z	1.065e-02	1.418e-02		
B to Z	8.440e-03	1.119e-02		
C to Z	4.951e-03	6.687e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

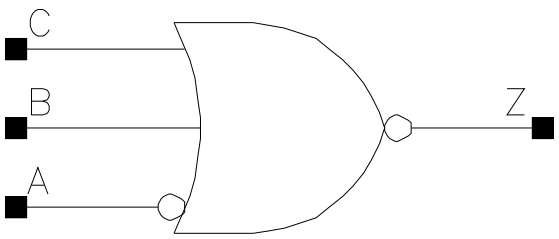
Pin Cycle (vdds)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P16	X49_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.680	0.8160
X13_P16	1.200	1.224	1.4688
X19_P16	1.200	1.496	1.7952
X25_P16	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0009	0.0013	0.0013	0.0024
B	0.0010	0.0020	0.0029	0.0039
C	0.0010	0.0018	0.0026	0.0035

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X13_P16**	**X6_P16**	**X13_P16**
A to Z ↓	0.0309	0.0295	1.9341	1.0867
A to Z ↑	0.0339	0.0337	8.3208	4.0841
B to Z ↓	0.0113	0.0112	2.0241	0.9850
B to Z ↑	0.0217	0.0231	8.3632	4.0994
C to Z ↓	0.0095	0.0084	2.0384	0.9988
C to Z ↑	0.0194	0.0166	8.3918	4.1135
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0336	0.0294	0.6570	0.4989

A to Z ↑	0.0368	0.0337	2.7518	2.0633
B to Z ↓	0.0115	0.0113	0.6853	0.5111
B to Z ↑	0.0222	0.0224	2.7641	2.0722
C to Z ↓	0.0089	0.0085	0.6857	0.5157
C to Z ↑	0.0176	0.0167	2.7739	2.0802

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P16	2.393e-07	1.000e-20
X13_P16	5.071e-07	1.000e-20
X19_P16	6.651e-07	1.000e-20
X25_P16	9.860e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	1.642e-03	3.104e-03	4.145e-03	6.054e-03
B (output stable)	9.293e-07	4.581e-05	4.005e-05	7.256e-05
C (output stable)	8.475e-06	3.889e-05	3.855e-05	6.549e-05
A to Z	3.353e-03	6.684e-03	9.236e-03	1.291e-02
B to Z	1.377e-03	2.963e-03	4.206e-03	5.652e-03
C to Z	9.864e-04	1.687e-03	2.662e-03	3.342e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

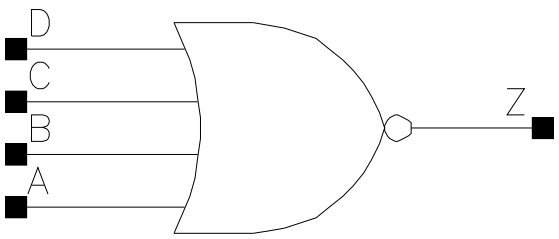
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	1.904	2.2848
X32_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X32_P16
A	0.0008	0.0008	0.0009	0.0011
B	0.0008	0.0008	0.0010	0.0013
C	0.0007	0.0007	0.0009	0.0011
D	0.0007	0.0007	0.0009	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0370	0.0366	1.8978	0.9347
A to Z ↑	0.0532	0.0572	2.8968	1.4308
B to Z ↓	0.0354	0.0355	1.8987	0.9345
B to Z ↑	0.0532	0.0576	2.9019	1.4315
C to Z ↓	0.0361	0.0364	1.8975	0.9323
C to Z ↑	0.0536	0.0584	2.8996	1.4305

D to Z ↓	0.0353	0.0358	1.8968	0.9328
D to Z ↑	0.0541	0.0593	2.9002	1.4307
	X25_P16	**X32_P16**	**X25_P16**	**X32_P16**
A to Z ↓	0.0379	0.0398	0.6503	0.5120
A to Z ↑	0.0567	0.0547	0.9822	0.7433
B to Z ↓	0.0368	0.0385	0.6509	0.5115
B to Z ↑	0.0573	0.0550	0.9824	0.7432
C to Z ↓	0.0367	0.0393	0.6486	0.5104
C to Z ↑	0.0562	0.0550	0.9802	0.7432
D to Z ↓	0.0354	0.0372	0.6483	0.5106
D to Z ↑	0.0568	0.0552	0.9811	0.7434

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	3.664e-07	1.000e-20
X17_P16	5.829e-07	1.000e-20
X25_P16	8.777e-07	1.000e-20
X32_P16	1.118e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	5.897e-04	7.369e-04	1.016e-03	1.278e-03
B (output stable)	4.883e-04	6.382e-04	8.886e-04	1.100e-03
C (output stable)	5.526e-04	6.748e-04	1.041e-03	1.325e-03
D (output stable)	4.470e-04	5.740e-04	8.961e-04	1.137e-03
A to Z	4.095e-03	6.220e-03	9.570e-03	1.195e-02
B to Z	3.884e-03	6.026e-03	9.274e-03	1.160e-02
C to Z	4.110e-03	6.154e-03	9.004e-03	1.130e-02
D to Z	3.892e-03	5.962e-03	8.733e-03	1.092e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

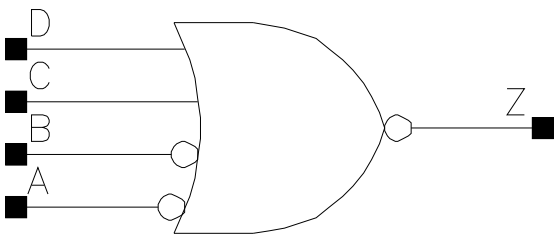
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X13_P16	1.200	1.496	1.7952
X19_P16	1.200	2.040	2.4480
X25_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0012	0.0012	0.0023	0.0023
B	0.0012	0.0017	0.0024	0.0024
C	0.0010	0.0019	0.0028	0.0037
D	0.0009	0.0018	0.0026	0.0034

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X13_P16	X6_P16	X13_P16
A to Z ↓	0.0266	0.0333	1.8859	0.9434
A to Z ↑	0.0336	0.0423	8.0155	4.1544
B to Z ↓	0.0246	0.0317	1.8854	0.9432
B to Z ↑	0.0343	0.0434	8.0156	4.1564
C to Z ↓	0.0117	0.0112	2.0644	0.9840
C to Z ↑	0.0219	0.0231	8.0595	4.1722

D to Z ↓	0.0096	0.0085	2.0683	0.9959
D to Z ↑	0.0192	0.0170	8.0846	4.1855
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0294	0.0323	0.6483	0.4881
A to Z ↑	0.0380	0.0415	2.7514	2.0800
B to Z ↓	0.0269	0.0302	0.6474	0.4878
B to Z ↑	0.0382	0.0423	2.7514	2.0801
C to Z ↓	0.0115	0.0115	0.6849	0.5127
C to Z ↑	0.0221	0.0225	2.7628	2.0870
D to Z ↓	0.0089	0.0086	0.6860	0.5151
D to Z ↑	0.0175	0.0168	2.7722	2.0941

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P16	3.298e-07	1.000e-20
X13_P16	5.108e-07	1.000e-20
X19_P16	8.183e-07	1.000e-20
X25_P16	9.799e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	9.684e-04	1.772e-03	2.645e-03	3.291e-03
B (output stable)	8.688e-04	1.622e-03	2.338e-03	3.007e-03
C (output stable)	1.521e-06	4.091e-05	5.938e-05	1.046e-04
D (output stable)	1.735e-05	7.085e-05	8.874e-05	1.556e-04
A to Z	4.009e-03	7.651e-03	1.137e-02	1.476e-02
B to Z	3.727e-03	7.225e-03	1.051e-02	1.396e-02
C to Z	1.431e-03	2.935e-03	4.190e-03	5.623e-03
D to Z	1.022e-03	1.726e-03	2.664e-03	3.341e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

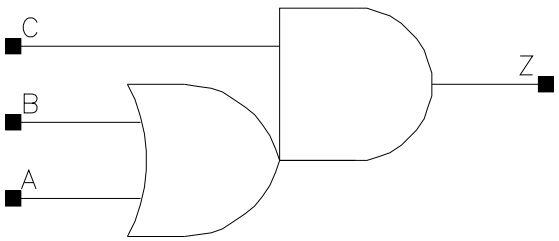
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0011	0.0011	0.0021
B	0.0012	0.0012	0.0024
C	0.0012	0.0012	0.0023

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0292	0.0339	1.9581	0.9775
A to Z ↑	0.0259	0.0290	2.9152	1.4348
B to Z ↓	0.0291	0.0343	1.9597	0.9787
B to Z ↑	0.0233	0.0266	2.9122	1.4336
C to Z ↓	0.0265	0.0293	1.9356	0.9602
C to Z ↑	0.0243	0.0270	2.9100	1.4323
	X33_P16		**X33_P16**	
A to Z ↓	0.0354		0.4976	
A to Z ↑	0.0312		0.7210	

B to Z ↓	0.0358		0.4980	
B to Z ↑	0.0283		0.7203	
C to Z ↓	0.0300		0.4874	
C to Z ↑	0.0281		0.7199	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	3.370e-07	1.000e-20
X17_P16	4.833e-07	1.000e-20
X33_P16	9.655e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.273e-04	1.269e-04	2.554e-04
B (output stable)	3.542e-05	3.448e-05	6.255e-05
C (output stable)	7.959e-05	8.171e-05	1.615e-04
A to Z	3.032e-03	4.450e-03	9.351e-03
B to Z	2.642e-03	4.055e-03	8.580e-03
C to Z	3.326e-03	4.691e-03	9.701e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

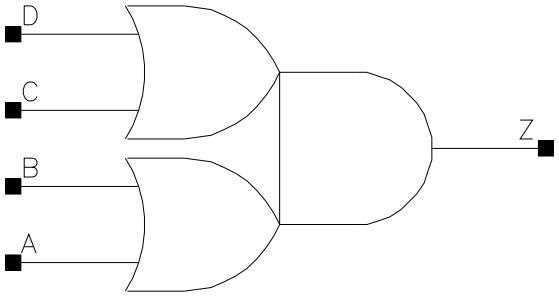
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0011	0.0022
B	0.0008	0.0012	0.0022
C	0.0008	0.0012	0.0022
D	0.0007	0.0011	0.0023

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0493	0.0418	1.9088	0.9701
A to Z ↑	0.0347	0.0310	2.8599	1.4289
B to Z ↓	0.0503	0.0425	1.9085	0.9700
B to Z ↑	0.0332	0.0292	2.8537	1.4273

C to Z ↓	0.0428	0.0366	1.8977	0.9662
C to Z ↑	0.0337	0.0310	2.8572	1.4283
D to Z ↓	0.0429	0.0368	1.8983	0.9666
D to Z ↑	0.0316	0.0284	2.8542	1.4256
	X33_P16		**X33_P16**	
A to Z ↓	0.0428		0.5005	
A to Z ↑	0.0313		0.7189	
B to Z ↓	0.0418		0.5010	
B to Z ↑	0.0290		0.7176	
C to Z ↓	0.0371		0.4982	
C to Z ↑	0.0308		0.7179	
D to Z ↓	0.0356		0.4988	
D to Z ↑	0.0280		0.7168	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	2.720e-07	1.000e-20
X17_P16	5.533e-07	1.000e-20
X33_P16	1.067e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.181e-05	3.811e-05	1.233e-04
B (output stable)	1.849e-05	2.528e-05	6.880e-05
C (output stable)	3.764e-05	6.814e-05	2.719e-04
D (output stable)	7.976e-05	1.054e-04	2.540e-04
A to Z	3.546e-03	5.749e-03	1.150e-02
B to Z	3.342e-03	5.339e-03	1.038e-02
C to Z	3.055e-03	5.008e-03	1.004e-02
D to Z	2.844e-03	4.611e-03	8.861e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

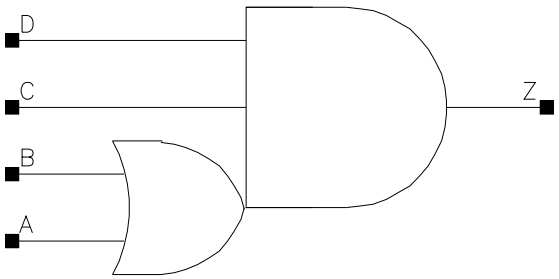
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	1.088	1.3056
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0007	0.0012	0.0018	0.0022
B	0.0007	0.0012	0.0019	0.0023
C	0.0008	0.0012	0.0019	0.0023
D	0.0007	0.0012	0.0019	0.0023

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0418	0.0396	2.0060	0.9809
A to Z ↑	0.0406	0.0388	2.9687	1.4375
B to Z ↓	0.0425	0.0391	2.0042	0.9813
B to Z ↑	0.0382	0.0353	2.9675	1.4366
C to Z ↓	0.0354	0.0329	1.9550	0.9599

C to Z ↑	0.0379	0.0360	2.9629	1.4354
D to Z ↓	0.0342	0.0317	1.9540	0.9590
D to Z ↑	0.0394	0.0372	2.9629	1.4355
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0410	0.0393	0.6677	0.4998
A to Z ↑	0.0392	0.0398	0.9762	0.7321
B to Z ↓	0.0400	0.0386	0.6677	0.4999
B to Z ↑	0.0359	0.0363	0.9753	0.7298
C to Z ↓	0.0343	0.0328	0.6534	0.4890
C to Z ↑	0.0367	0.0366	0.9744	0.7300
D to Z ↓	0.0326	0.0314	0.6522	0.4885
D to Z ↑	0.0368	0.0370	0.9749	0.7297

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	2.429e-07	1.000e-20
X17_P16	5.057e-07	1.000e-20
X25_P16	7.732e-07	1.000e-20
X33_P16	1.010e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	6.473e-05	1.363e-04	2.501e-04	2.812e-04
B (output stable)	3.872e-05	8.275e-05	1.402e-04	1.529e-04
C (output stable)	1.201e-05	2.249e-05	7.167e-05	9.441e-05
D (output stable)	2.992e-05	6.640e-05	1.706e-04	1.784e-04
A to Z	2.938e-03	5.331e-03	8.474e-03	1.050e-02
B to Z	2.742e-03	4.820e-03	7.625e-03	9.441e-03
C to Z	3.201e-03	5.725e-03	9.297e-03	1.126e-02
D to Z	3.054e-03	5.444e-03	8.613e-03	1.055e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

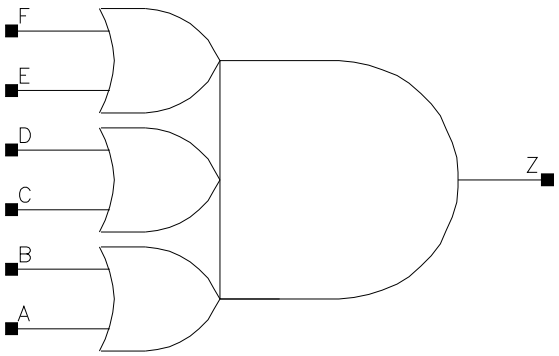
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0008	0.0011	0.0019
B	0.0007	0.0011	0.0021
C	0.0007	0.0011	0.0020
D	0.0007	0.0011	0.0021
E	0.0007	0.0011	0.0020
F	0.0007	0.0011	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0560	0.0484	2.0479	0.9972
A to Z ↑	0.0444	0.0415	2.9466	1.4502
B to Z ↓	0.0568	0.0494	2.0479	0.9976
B to Z ↑	0.0426	0.0398	2.9468	1.4505
C to Z ↓	0.0514	0.0458	2.0366	0.9959
C to Z ↑	0.0446	0.0411	2.9492	1.4502
D to Z ↓	0.0524	0.0465	2.0366	0.9963
D to Z ↑	0.0425	0.0389	2.9460	1.4496
E to Z ↓	0.0446	0.0402	2.0258	0.9921
E to Z ↑	0.0416	0.0391	2.9460	1.4494
F to Z ↓	0.0456	0.0407	2.0265	0.9926
F to Z ↑	0.0395	0.0368	2.9417	1.4472
	X33_P16		X33_P16	
A to Z ↓	0.0489		0.5101	
A to Z ↑	0.0426		0.7324	
B to Z ↓	0.0500		0.5103	
B to Z ↑	0.0397		0.7306	
C to Z ↓	0.0449		0.5071	
C to Z ↑	0.0420		0.7319	
D to Z ↓	0.0458		0.5076	
D to Z ↑	0.0393		0.7302	
E to Z ↓	0.0395		0.5052	
E to Z ↑	0.0401		0.7310	
F to Z ↓	0.0403		0.5056	
F to Z ↑	0.0372		0.7294	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	3.106e-07	1.000e-20
X17_P16	6.318e-07	1.000e-20
X33_P16	1.209e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.759e-05	3.479e-05	5.799e-05
B (output stable)	7.733e-06	1.645e-05	2.418e-05
C (output stable)	3.737e-05	5.581e-05	1.166e-04
D (output stable)	3.998e-05	6.665e-05	1.405e-04
E (output stable)	3.396e-05	5.788e-05	1.054e-04
F (output stable)	1.246e-04	1.867e-04	3.563e-04
A to Z	4.085e-03	6.867e-03	1.342e-02
B to Z	3.872e-03	6.484e-03	1.268e-02
C to Z	3.707e-03	6.301e-03	1.223e-02
D to Z	3.505e-03	5.906e-03	1.148e-02
E to Z	3.234e-03	5.575e-03	1.083e-02
F to Z	3.045e-03	5.201e-03	1.011e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

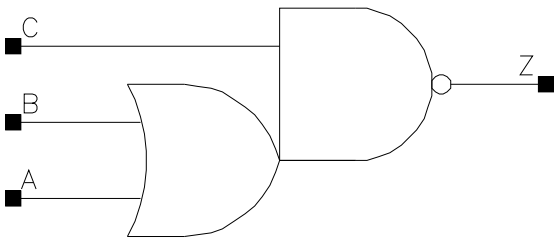
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X34_P16	1.200	2.720	3.2640
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X34_P16	X46_P16
A	0.0009	0.0027	0.0056	0.0072
B	0.0009	0.0025	0.0050	0.0067
C	0.0010	0.0029	0.0059	0.0076

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0141	0.0147	3.6745	1.2007
A to Z ↑	0.0167	0.0180	5.5572	1.8905
B to Z ↓	0.0113	0.0117	3.6148	1.2094
B to Z ↑	0.0157	0.0157	5.5967	1.9055
C to Z ↓	0.0133	0.0135	3.3359	1.0997
C to Z ↑	0.0163	0.0162	2.9492	0.9792
	X34_P16	**X46_P16**	**X34_P16**	**X46_P16**
A to Z ↓	0.0153	0.0152	0.6117	0.4667

A to Z ↑	0.0186	0.0183	0.9415	0.7250
B to Z ↓	0.0120	0.0121	0.6206	0.4755
B to Z ↑	0.0160	0.0160	0.9493	0.7305
C to Z ↓	0.0140	0.0138	0.5628	0.4300
C to Z ↑	0.0165	0.0164	0.4891	0.3742

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P16	2.055e-07	1.000e-20
X17_P16	6.047e-07	1.000e-20
X34_P16	1.206e-06	1.000e-20
X46_P16	1.594e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	1.194e-04	3.911e-04	8.181e-04	1.015e-03
B (output stable)	3.853e-05	1.105e-04	2.248e-04	2.911e-04
C (output stable)	6.635e-05	2.116e-04	4.629e-04	5.645e-04
A to Z	1.298e-03	4.250e-03	8.894e-03	1.141e-02
B to Z	9.121e-04	2.766e-03	5.725e-03	7.443e-03
C to Z	1.587e-03	4.893e-03	1.016e-02	1.310e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

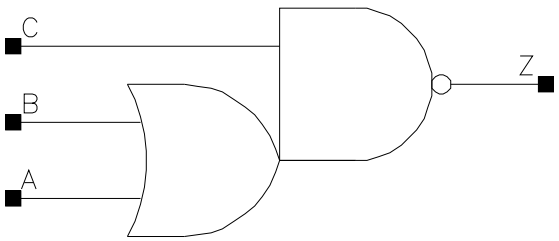
Pin Cycle (vdds)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.544	0.6528
X11_P16	1.200	0.952	1.1424
X17_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X17_P16	X23_P16
A	0.0010	0.0019	0.0029	0.0040
B	0.0009	0.0020	0.0027	0.0036
C	0.0009	0.0018	0.0027	0.0036
	X46_P16			
A	0.0079			
B	0.0072			
C	0.0073			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0149	0.0151	3.7081	1.7285
A to Z ↑	0.0212	0.0212	5.8552	2.7662
B to Z ↓	0.0127	0.0127	3.6449	1.6828

B to Z ↑	0.0207	0.0207	5.8910	2.7828
C to Z ↓	0.0115	0.0115	3.4675	1.6090
C to Z ↑	0.0123	0.0121	3.1762	1.4896
	X17_P16	**X23_P16**	**X17_P16**	**X23_P16**
A to Z ↓	0.0146	0.0153	1.2024	0.8883
A to Z ↑	0.0202	0.0222	1.8319	1.3976
B to Z ↓	0.0122	0.0127	1.1990	0.8882
B to Z ↑	0.0195	0.0202	1.8421	1.4058
C to Z ↓	0.0111	0.0114	1.1322	0.8353
C to Z ↑	0.0113	0.0117	0.9892	0.7534
	X46_P16		**X46_P16**	
A to Z ↓	0.0152		0.4634	
A to Z ↑	0.0218		0.7061	
B to Z ↓	0.0124		0.4589	
B to Z ↑	0.0198		0.7108	
C to Z ↓	0.0115		0.4341	
C to Z ↑	0.0114		0.3808	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.133e-07	1.000e-20
X11_P16	4.475e-07	1.000e-20
X17_P16	6.607e-07	1.000e-20
X23_P16	8.914e-07	1.000e-20
X46_P16	1.738e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	3.133e-05	7.173e-05	9.710e-05	2.010e-04
B (output stable)	1.058e-05	2.540e-05	3.478e-05	6.720e-05
C (output stable)	2.919e-04	6.757e-04	8.314e-04	1.304e-03
A to Z	1.739e-03	3.691e-03	5.141e-03	7.728e-03
B to Z	1.328e-03	2.850e-03	3.826e-03	5.475e-03
C to Z	9.448e-04	2.063e-03	2.795e-03	4.078e-03
	X46_P16			
A (output stable)	3.632e-04			
B (output stable)	1.287e-04			
C (output stable)	2.369e-03			
A to Z	1.489e-02			
B to Z	1.042e-02			
C to Z	7.800e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

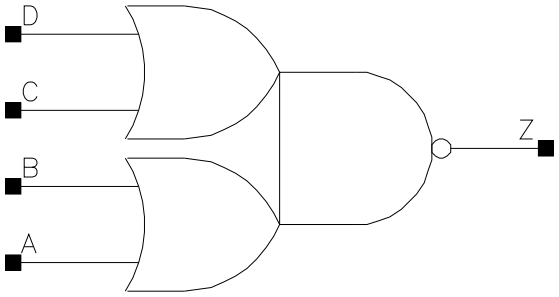
	X46_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0010	0.0019	0.0029	0.0040
B	0.0010	0.0018	0.0026	0.0036
C	0.0009	0.0018	0.0027	0.0038
D	0.0009	0.0017	0.0024	0.0034
	X42_P16			
A	0.0080			
B	0.0071			
C	0.0074			
D	0.0068			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0163	0.0174	3.4037	1.6924
A to Z ↑	0.0245	0.0248	6.1770	2.8298
B to Z ↓	0.0143	0.0149	3.3324	1.6968
B to Z ↑	0.0239	0.0227	6.2016	2.8468
C to Z ↓	0.0146	0.0158	3.4698	1.7106
C to Z ↑	0.0177	0.0193	6.0306	2.8382
D to Z ↓	0.0120	0.0124	3.3807	1.7224
D to Z ↑	0.0165	0.0157	6.0722	2.8655
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0167	0.0170	1.1589	0.8343
A to Z ↑	0.0235	0.0242	1.9052	1.4019
B to Z ↓	0.0145	0.0144	1.1635	0.8333
B to Z ↑	0.0220	0.0224	1.9176	1.4105
C to Z ↓	0.0154	0.0155	1.1735	0.8442
C to Z ↑	0.0180	0.0184	1.9124	1.4047
D to Z ↓	0.0125	0.0123	1.1872	0.8480
D to Z ↑	0.0153	0.0155	1.9309	1.4174
	X42_P16		**X42_P16**	
A to Z ↓	0.0173		0.4377	
A to Z ↑	0.0243		0.7149	
B to Z ↓	0.0147		0.4329	
B to Z ↑	0.0226		0.7189	
C to Z ↓	0.0162		0.4441	
C to Z ↑	0.0186		0.7112	
D to Z ↓	0.0128		0.4407	
D to Z ↑	0.0158		0.7177	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.621e-07	1.000e-20
X10_P16	5.414e-07	1.000e-20
X15_P16	7.820e-07	1.000e-20
X21_P16	1.088e-06	1.000e-20
X42_P16	2.142e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	3.476e-05	1.207e-04	1.551e-04	2.263e-04
B (output stable)	2.051e-05	6.193e-05	7.432e-05	1.015e-04
C (output stable)	6.472e-05	2.770e-04	3.021e-04	4.701e-04
D (output stable)	9.232e-05	2.346e-04	2.990e-04	4.296e-04
A to Z	2.106e-03	4.784e-03	6.608e-03	9.314e-03
B to Z	1.713e-03	3.619e-03	5.016e-03	7.079e-03
C to Z	1.408e-03	3.427e-03	4.644e-03	6.538e-03
D to Z	1.044e-03	2.234e-03	3.116e-03	4.345e-03
	X42_P16			
A (output stable)	4.423e-04			
B (output stable)	2.023e-04			
C (output stable)	9.084e-04			
D (output stable)	8.441e-04			

A to Z	1.845e-02			
B to Z	1.398e-02			
C to Z	1.304e-02			
D to Z	8.722e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

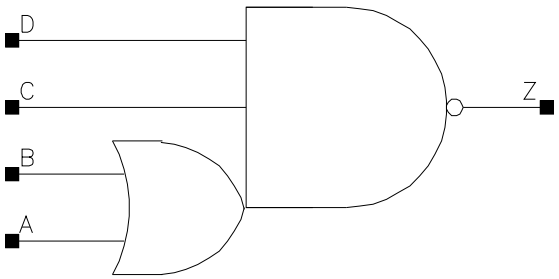
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X21_P16	1.200	2.448	2.9376
X31_P16	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X21_P16	X31_P16
A	0.0010	0.0018	0.0036	0.0054
B	0.0011	0.0017	0.0032	0.0049
C	0.0010	0.0020	0.0039	0.0058
D	0.0010	0.0019	0.0037	0.0054

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0199	0.0192	4.7000	2.5119
A to Z ↑	0.0222	0.0206	5.5587	2.8026
B to Z ↓	0.0170	0.0151	4.7556	2.5260
B to Z ↑	0.0210	0.0180	5.6134	2.8265
C to Z ↓	0.0183	0.0190	4.4354	2.3653

C to Z ↑	0.0198	0.0194	2.8741	1.4461
D to Z ↓	0.0192	0.0184	4.4540	2.3767
D to Z ↑	0.0187	0.0175	2.9119	1.4502
	X21_P16	**X31_P16**	**X21_P16**	**X31_P16**
A to Z ↓	0.0195	0.0197	1.3097	0.8890
A to Z ↑	0.0202	0.0202	1.4002	0.9400
B to Z ↓	0.0153	0.0155	1.3182	0.8978
B to Z ↑	0.0176	0.0177	1.4114	0.9484
C to Z ↓	0.0189	0.0190	1.2353	0.8397
C to Z ↑	0.0190	0.0190	0.7328	0.4945
D to Z ↓	0.0185	0.0187	1.2408	0.8435
D to Z ↑	0.0173	0.0174	0.7341	0.4943

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.098e-07	1.000e-20
X10_P16	4.056e-07	1.000e-20
X21_P16	7.848e-07	1.000e-20
X31_P16	1.164e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	1.374e-04	2.907e-04	5.519e-04	8.089e-04
B (output stable)	8.352e-05	1.570e-04	2.958e-04	4.323e-04
C (output stable)	2.495e-05	8.217e-05	1.272e-04	1.721e-04
D (output stable)	6.642e-05	1.846e-04	3.134e-04	4.560e-04
A to Z	2.003e-03	3.510e-03	6.809e-03	1.012e-02
B to Z	1.438e-03	2.361e-03	4.537e-03	6.811e-03
C to Z	2.433e-03	4.702e-03	9.011e-03	1.337e-02
D to Z	2.158e-03	3.864e-03	7.443e-03	1.108e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

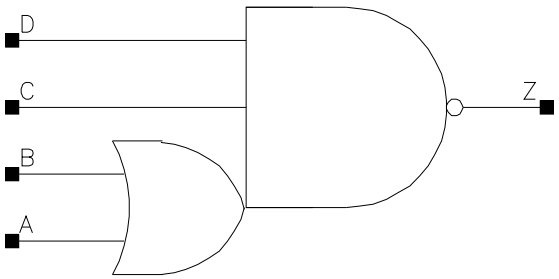
Pin Cycle (vdds)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0010	0.0020	0.0030	0.0040
B	0.0010	0.0018	0.0027	0.0036
C	0.0010	0.0019	0.0028	0.0037
D	0.0009	0.0018	0.0027	0.0035

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0193	0.0207	4.7886	2.4983
A to Z ↑	0.0245	0.0267	5.4085	2.7572
B to Z ↓	0.0167	0.0175	4.7088	2.5015
B to Z ↑	0.0243	0.0250	5.4337	2.7709
C to Z ↓	0.0150	0.0170	4.5262	2.3796

C to Z ↑	0.0155	0.0164	2.9294	1.4818
D to Z ↓	0.0149	0.0157	4.5594	2.3960
D to Z ↑	0.0134	0.0137	2.9543	1.4956
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0205	0.0206	1.7182	1.2966
A to Z ↑	0.0256	0.0262	1.8587	1.4089
B to Z ↓	0.0174	0.0174	1.7129	1.2950
B to Z ↑	0.0244	0.0249	1.8687	1.4162
C to Z ↓	0.0165	0.0169	1.6328	1.2322
C to Z ↑	0.0157	0.0160	0.9875	0.7427
D to Z ↓	0.0154	0.0159	1.6451	1.2407
D to Z ↑	0.0131	0.0135	0.9970	0.7493

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.329e-07	1.000e-20
X10_P16	4.624e-07	1.000e-20
X15_P16	6.656e-07	1.000e-20
X21_P16	9.046e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	1.962e-05	5.590e-05	7.236e-05	1.034e-04
B (output stable)	1.027e-05	3.882e-05	4.428e-05	6.239e-05
C (output stable)	7.661e-05	1.666e-04	2.280e-04	3.135e-04
D (output stable)	1.878e-04	5.923e-04	7.286e-04	1.072e-03
A to Z	2.395e-03	5.239e-03	7.430e-03	1.015e-02
B to Z	1.947e-03	4.037e-03	5.733e-03	7.815e-03
C to Z	1.498e-03	3.397e-03	4.714e-03	6.550e-03
D to Z	1.202e-03	2.587e-03	3.605e-03	4.983e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

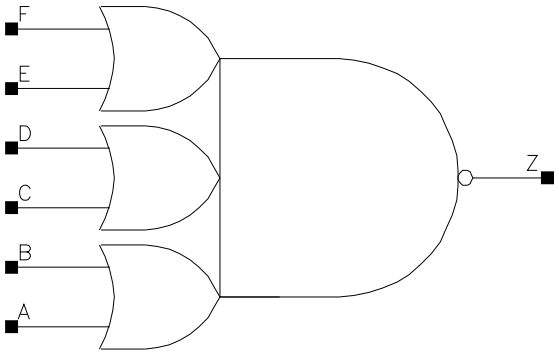
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	1.088	1.3056
X9_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X9_P16
A	0.0008	0.0020
B	0.0008	0.0018
C	0.0008	0.0020
D	0.0007	0.0018
E	0.0008	0.0019
F	0.0007	0.0017

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X9_P16	X3_P16	X9_P16
A to Z ↓	0.0241	0.0257	5.4943	2.2667
A to Z ↑	0.0325	0.0313	7.6418	2.7766
B to Z ↓	0.0224	0.0228	5.5372	2.2701
B to Z ↑	0.0332	0.0300	7.6669	2.7883
C to Z ↓	0.0232	0.0242	5.5384	2.2791
C to Z ↑	0.0281	0.0270	7.6613	2.7698
D to Z ↓	0.0211	0.0211	5.5834	2.2859
D to Z ↑	0.0285	0.0254	7.6955	2.7852
E to Z ↓	0.0199	0.0212	5.5821	2.2851
E to Z ↑	0.0217	0.0213	7.6920	2.7743
F to Z ↓	0.0178	0.0175	5.6315	2.2927
F to Z ↑	0.0216	0.0185	7.7473	2.7978

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	2.597e-07	1.000e-20
X9_P16	7.116e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X9_P16
A (output stable)	2.319e-05	1.046e-04
B (output stable)	1.009e-05	5.772e-05
C (output stable)	4.429e-05	1.947e-04
D (output stable)	6.226e-05	1.811e-04
E (output stable)	4.446e-05	1.707e-04
F (output stable)	1.697e-04	4.080e-04
A to Z	2.747e-03	7.267e-03
B to Z	2.450e-03	6.097e-03
C to Z	2.218e-03	5.877e-03
D to Z	1.928e-03	4.776e-03
E to Z	1.590e-03	4.419e-03
F to Z	1.318e-03	3.271e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

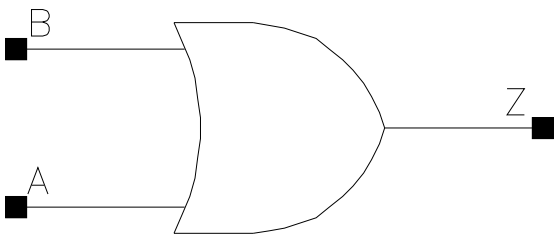
Pin Cycle (vdds)	X3_P16	X9_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X33_P16	1.200	1.360	1.6320
X50_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P16	X16_P16	X33_P16	X50_P16
A	0.0009	0.0011	0.0022	0.0022
B	0.0007	0.0011	0.0022	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0383	0.0342	1.9670	0.9938
A to Z ↑	0.0244	0.0257	2.8753	1.4520
B to Z ↓	0.0383	0.0342	1.9674	0.9950
B to Z ↑	0.0231	0.0239	2.8767	1.4519
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0354	0.0413	0.4923	0.3386
A to Z ↑	0.0257	0.0255	0.7069	0.4782
B to Z ↓	0.0339	0.0402	0.4923	0.3388
B to Z ↑	0.0234	0.0238	0.7052	0.4771

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	2.022e-07	1.000e-20
X16_P16	3.729e-07	1.000e-20
X33_P16	7.574e-07	1.000e-20
X50_P16	9.963e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	2.594e-05	4.783e-05	1.579e-04	1.476e-04
B (output stable)	5.248e-06	7.627e-06	9.438e-05	8.072e-05
A to Z	2.687e-03	4.387e-03	9.218e-03	1.235e-02
B to Z	2.472e-03	3.997e-03	8.062e-03	1.126e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

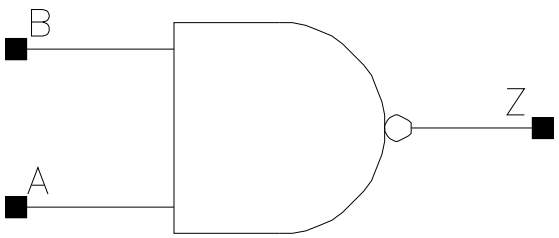
Pin Cycle (vdds)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X16_P16	1.200	0.952	1.1424
X24_P16	1.200	1.088	1.3056
X32_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P16	X16_P16	X24_P16	X32_P16
A	0.0011	0.0011	0.0012	0.0011
B	0.0012	0.0013	0.0013	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0324	0.0341	1.9073	0.9941
A to Z ↑	0.0345	0.0359	2.9088	1.4891
B to Z ↓	0.0337	0.0355	1.9058	0.9940
B to Z ↑	0.0328	0.0336	2.9089	1.4871
	X24_P16	**X32_P16**	**X24_P16**	**X32_P16**
A to Z ↓	0.0377	0.0390	0.6730	0.5057
A to Z ↑	0.0386	0.0397	0.9947	0.7422
B to Z ↓	0.0391	0.0407	0.6729	0.5057
B to Z ↑	0.0362	0.0380	0.9937	0.7418

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	4.326e-07	1.000e-20
X16_P16	5.397e-07	1.000e-20
X24_P16	6.407e-07	1.000e-20
X32_P16	8.462e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	2.048e-05	2.055e-05	2.065e-05	2.128e-05
B (output stable)	7.535e-05	7.555e-05	7.565e-05	7.561e-05
A to Z	5.171e-03	6.106e-03	7.723e-03	1.030e-02
B to Z	4.904e-03	5.851e-03	7.482e-03	1.003e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

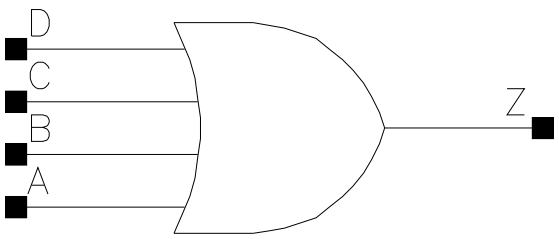
Pin Cycle (vdds)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P16	1.200	2.176	2.6112
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P16	X27_P16
A	0.0019	0.0023
B	0.0018	0.0023
C	0.0020	0.0023
D	0.0018	0.0023

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P16	X27_P16	X20_P16	X27_P16
A to Z ↓	0.0392	0.0411	1.1806	0.8826
A to Z ↑	0.0264	0.0257	0.9483	0.7063
B to Z ↓	0.0381	0.0394	1.1806	0.8824
B to Z ↑	0.0248	0.0237	0.9475	0.7053
C to Z ↓	0.0378	0.0397	1.1791	0.8810
C to Z ↑	0.0253	0.0251	0.9500	0.7087
D to Z ↓	0.0367	0.0384	1.1790	0.8812
D to Z ↑	0.0235	0.0233	0.9492	0.7082

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X20_P16	7.490e-07	1.000e-20
X27_P16	1.082e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X20_P16	X27_P16
A (output stable)	2.069e-03	2.874e-03
B (output stable)	1.684e-03	2.310e-03
C (output stable)	1.935e-03	2.806e-03
D (output stable)	1.484e-03	2.183e-03
A to Z	8.597e-03	1.208e-02
B to Z	7.788e-03	1.085e-02
C to Z	7.469e-03	1.039e-02
D to Z	6.655e-03	9.298e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

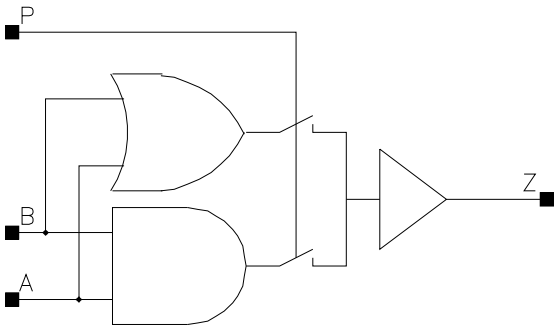
Pin Cycle (vdds)	X20_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X16_P16	1.200	1.224	1.4688
X25_P16	1.200	2.040	2.4480
X33_P16	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0014	0.0021	0.0037	0.0037
B	0.0013	0.0020	0.0041	0.0041
P	0.0007	0.0011	0.0021	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0467	0.0422	2.0032	0.9804
A to Z ↑	0.0323	0.0306	2.9264	1.4641
B to Z ↓	0.0465	0.0422	2.0163	0.9876
B to Z ↑	0.0335	0.0317	2.9287	1.4673
P to Z ↓	0.0426	0.0391	2.0175	0.9886
P to Z ↑	0.0324	0.0307	2.9261	1.4665
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**

A to Z ↓	0.0406	0.0436	0.6682	0.5060
A to Z ↑	0.0304	0.0323	0.9854	0.7385
B to Z ↓	0.0403	0.0431	0.6722	0.5089
B to Z ↑	0.0317	0.0335	0.9867	0.7399
P to Z ↓	0.0380	0.0409	0.6725	0.5092
P to Z ↑	0.0303	0.0321	0.9859	0.7383

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	2.784e-07	1.000e-20
X16_P16	5.702e-07	1.000e-20
X25_P16	9.808e-07	1.000e-20
X33_P16	1.108e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	5.541e-05	9.751e-05	1.842e-04	1.852e-04
B (output stable)	1.590e-04	2.569e-04	4.480e-04	4.536e-04
P (output stable)	1.338e-04	2.225e-04	3.857e-04	3.935e-04
A to Z	3.129e-03	5.325e-03	9.223e-03	1.078e-02
B to Z	3.021e-03	5.147e-03	8.771e-03	1.036e-02
P to Z	2.723e-03	4.708e-03	8.162e-03	9.718e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

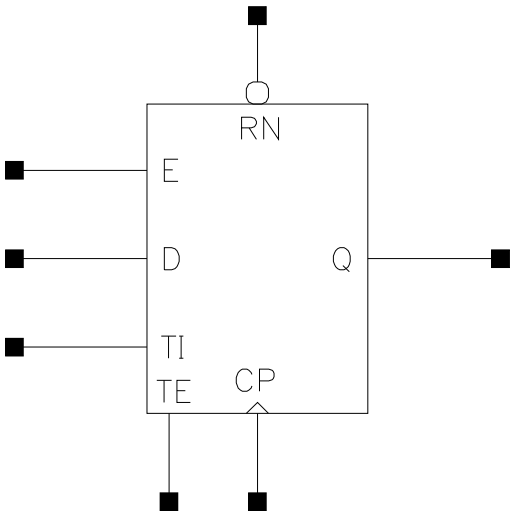
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.488	5.3856
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008
E	0.0010	0.0012	0.0012	0.0012
RN	0.0009	0.0008	0.0008	0.0009
TE	0.0011	0.0011	0.0011	0.0011

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to Q ↓	0.0862	0.0464	4.2839	1.9545
CP to Q ↑	0.0702	0.0603	6.0471	2.9014
RN to Q ↓	0.0735	0.0640	3.7049	2.0554
	X17_P16	X33_P16	X17_P16	X33_P16
CP to Q ↓	0.0790	0.0835	0.9504	0.5003
CP to Q ↑	0.0971	0.1023	1.4168	0.7241
RN to Q ↓	0.1051	0.1094	0.9492	0.4998

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1187	0.0786	0.0786	0.0786
CP ↑	min_pulse_width to CP	0.0787	0.0393	0.0346	0.0346
D ↓	hold_rising to CP	-0.1261	-0.0605	-0.0631	-0.0631
D ↑	hold_rising to CP	-0.0728	-0.0266	-0.0261	-0.0261
D ↓	setup_rising to CP	0.1729	0.1107	0.1107	0.1101
D ↑	setup_rising to CP	0.1048	0.0590	0.0590	0.0590
E ↓	hold_rising to CP	-0.0795	-0.0848	-0.0848	-0.0848
E ↑	hold_rising to CP	-0.0675	-0.0267	-0.0267	-0.0267
E ↓	setup_rising to CP	0.1485	0.1464	0.1464	0.1458
E ↑	setup_rising to CP	0.1638	0.1160	0.1150	0.1150
RN ↓	min_pulse_width to RN	0.0779	0.0876	0.0735	0.0757
RN ↑	recovery_rising to CP	0.0222	0.0173	0.0232	0.0232
RN ↑	removal_rising to CP	-0.0147	-0.0077	-0.0076	-0.0076
TE ↓	hold_rising to CP	-0.0600	-0.0409	-0.0409	-0.0409
TE ↑	hold_rising to CP	-0.0457	-0.0284	-0.0311	-0.0311
TE ↓	setup_rising to CP	0.1149	0.0901	0.0901	0.0901
TE ↑	setup_rising to CP	0.2051	0.1470	0.1496	0.1496
TI ↓	hold_rising to CP	-0.1589	-0.0843	-0.0843	-0.0836
TI ↑	hold_rising to CP	-0.0550	-0.0315	-0.0315	-0.0315
TI ↓	setup_rising to CP	0.2031	0.1336	0.1336	0.1336
TI ↑	setup_rising to CP	0.0883	0.0612	0.0612	0.0612

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	8.530e-07	1.000e-20
X8_P16	9.436e-07	1.000e-20
X17_P16	1.158e-06	1.000e-20
X33_P16	1.467e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

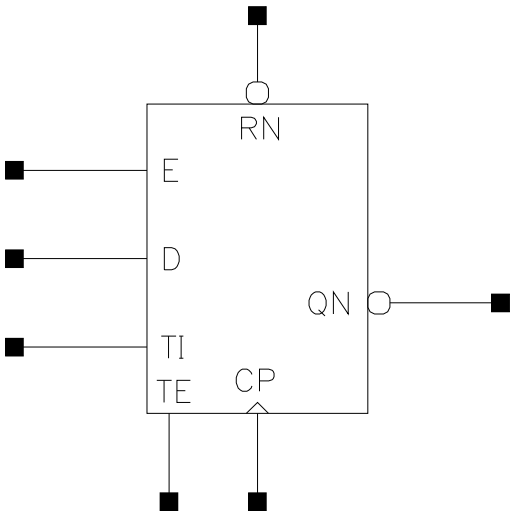
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	9.463e-03	9.550e-03	9.573e-03	9.584e-03
Clock 100Mhz Data 25Mhz	1.013e-02	1.033e-02	1.113e-02	1.208e-02
Clock 100Mhz Data 50Mhz	1.080e-02	1.112e-02	1.269e-02	1.457e-02
Clock = 0 Data 100Mhz	6.934e-03	6.782e-03	6.734e-03	6.711e-03
Clock = 1 Data 100Mhz	2.616e-03	2.676e-03	2.699e-03	2.710e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.624	5.5488
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008
E	0.0010	0.0012	0.0012	0.0012
RN	0.0009	0.0009	0.0009	0.0009
TE	0.0011	0.0011	0.0011	0.0011

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to QN ↓	0.0866	0.0817	3.6176	1.8846
CP to QN ↑	0.0951	0.0608	5.9046	2.8092
RN to QN ↑	0.0886	0.0886	5.8786	2.8083
	X17_P16	X33_P16	X17_P16	X33_P16
CP to QN ↓	0.0782	0.0828	0.9511	0.5005
CP to QN ↑	0.0637	0.0698	1.4170	0.7254
RN to QN ↑	0.0881	0.0977	1.4223	0.7272

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1187	0.0786	0.0786	0.0786
CP ↑	min_pulse_width to CP	0.0562	0.0346	0.0359	0.0405
D ↓	hold_rising to CP	-0.1261	-0.0631	-0.0605	-0.0605
D ↑	hold_rising to CP	-0.0728	-0.0261	-0.0266	-0.0266
D ↓	setup_rising to CP	0.1755	0.1107	0.1107	0.1107
D ↑	setup_rising to CP	0.1048	0.0590	0.0590	0.0590
E ↓	hold_rising to CP	-0.0821	-0.0848	-0.0848	-0.0848
E ↑	hold_rising to CP	-0.0675	-0.0267	-0.0267	-0.0267
E ↓	setup_rising to CP	0.1512	0.1464	0.1464	0.1458
E ↑	setup_rising to CP	0.1638	0.1150	0.1150	0.1150
RN ↓	min_pulse_width to RN	0.0752	0.0735	0.0850	0.0947
RN ↑	recovery_rising to CP	0.0222	0.0222	0.0232	0.0228
RN ↑	removal_rising to CP	-0.0147	-0.0131	-0.0076	-0.0076
TE ↓	hold_rising to CP	-0.0599	-0.0409	-0.0409	-0.0409
TE ↑	hold_rising to CP	-0.0457	-0.0311	-0.0284	-0.0284
TE ↓	setup_rising to CP	0.1144	0.0901	0.0901	0.0901
TE ↑	setup_rising to CP	0.2051	0.1496	0.1496	0.1492
TI ↓	hold_rising to CP	-0.1586	-0.0843	-0.0843	-0.0843
TI ↑	hold_rising to CP	-0.0550	-0.0315	-0.0315	-0.0315
TI ↓	setup_rising to CP	0.2031	0.1336	0.1336	0.1336
TI ↑	setup_rising to CP	0.0883	0.0612	0.0627	0.0627

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	8.537e-07	1.000e-20
X8_P16	9.269e-07	1.000e-20
X17_P16	1.128e-06	1.000e-20
X33_P16	1.396e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

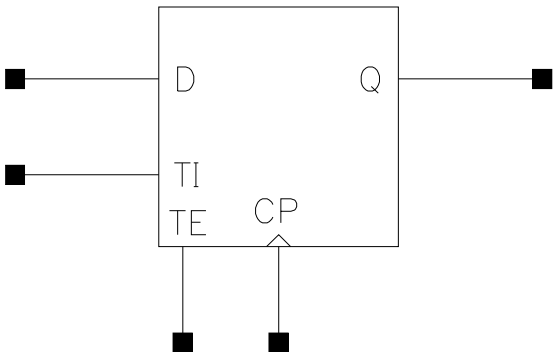
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	9.441e-03	9.527e-03	9.544e-03	9.554e-03
Clock 100Mhz Data 25Mhz	1.009e-02	1.038e-02	1.106e-02	1.198e-02
Clock 100Mhz Data 50Mhz	1.074e-02	1.123e-02	1.258e-02	1.441e-02
Clock = 0 Data 100Mhz	6.924e-03	6.772e-03	6.721e-03	6.697e-03
Clock = 1 Data 100Mhz	2.614e-03	2.680e-03	2.701e-03	2.713e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.400	4.0800
X8_P16	1.200	3.128	3.7536
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0706	0.0432	4.0402	1.9556
CP to Q ↑	0.0632	0.0552	6.0707	2.8564
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0652	0.0716	0.9335	0.4919
CP to Q ↑	0.0962	0.1020	1.4136	0.7222

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1039	0.1095	0.1088	0.1088
CP ↑	min_pulse_width to CP	0.0549	0.0346	0.0313	0.0313
D ↓	hold_rising to CP	-0.0746	-0.0289	-0.0321	-0.0321
D ↑	hold_rising to CP	-0.0284	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1144	0.0733	0.0765	0.0765
D ↑	setup_rising to CP	0.0583	0.0319	0.0319	0.0319
TE ↓	hold_rising to CP	-0.0506	-0.0289	-0.0289	-0.0289
TE ↑	hold_rising to CP	-0.0382	-0.0212	-0.0208	-0.0208
TE ↓	setup_rising to CP	0.0950	0.0734	0.0734	0.0734
TE ↑	setup_rising to CP	0.1812	0.1492	0.1492	0.1492
TI ↓	hold_rising to CP	-0.1489	-0.0905	-0.0946	-0.0905
TI ↑	hold_rising to CP	-0.0437	-0.0228	-0.0237	-0.0237
TI ↓	setup_rising to CP	0.1849	0.1449	0.1449	0.1449
TI ↑	setup_rising to CP	0.0734	0.0527	0.0527	0.0527

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	6.807e-07	1.000e-20
X8_P16	7.680e-07	1.000e-20
X17_P16	1.049e-06	1.000e-20
X33_P16	1.293e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

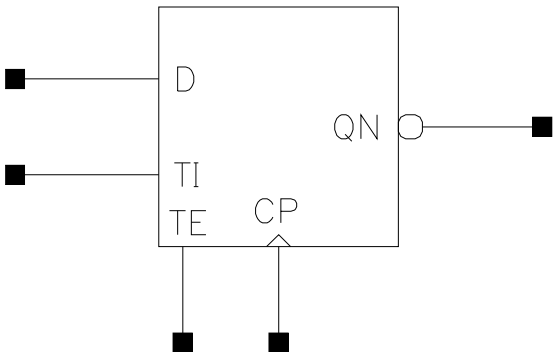
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	8.538e-03	8.599e-03	8.614e-03	8.622e-03
Clock 100Mhz Data 25Mhz	8.546e-03	8.686e-03	9.481e-03	1.025e-02
Clock 100Mhz Data 50Mhz	8.554e-03	8.773e-03	1.035e-02	1.188e-02
Clock = 0 Data 100Mhz	5.510e-03	5.220e-03	5.123e-03	5.075e-03
Clock = 1 Data 100Mhz	1.477e-03	7.806e-04	5.488e-04	4.329e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.536	4.2432
X8_P16	1.200	3.264	3.9168
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0815	0.0876	4.1021	1.9519
CP to QN ↑	0.0761	0.0557	6.0124	2.8194
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0673	0.0744	0.9334	0.4925
CP to QN ↑	0.0563	0.0623	1.4128	0.7224

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1022	0.1088	0.1088	0.1088
CP ↑	min_pulse_width to CP	0.0454	0.0313	0.0346	0.0360
D ↓	hold_rising to CP	-0.0746	-0.0321	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0305	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1144	0.0733	0.0765	0.0765
D ↑	setup_rising to CP	0.0583	0.0319	0.0319	0.0319
TE ↓	hold_rising to CP	-0.0506	-0.0289	-0.0289	-0.0289
TE ↑	hold_rising to CP	-0.0382	-0.0208	-0.0212	-0.0212
TE ↓	setup_rising to CP	0.0950	0.0734	0.0734	0.0734
TE ↑	setup_rising to CP	0.1812	0.1492	0.1492	0.1492
TI ↓	hold_rising to CP	-0.1489	-0.0905	-0.0905	-0.0905
TI ↑	hold_rising to CP	-0.0437	-0.0244	-0.0228	-0.0228
TI ↓	setup_rising to CP	0.1851	0.1449	0.1449	0.1449
TI ↑	setup_rising to CP	0.0734	0.0527	0.0527	0.0527

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	6.841e-07	1.000e-20
X8_P16	7.704e-07	1.000e-20
X17_P16	1.046e-06	1.000e-20
X33_P16	1.290e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

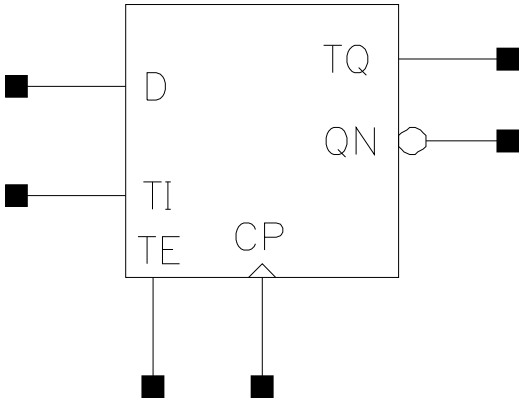
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	8.461e-03	8.557e-03	8.587e-03	8.602e-03
Clock 100Mhz Data 25Mhz	8.533e-03	8.775e-03	9.414e-03	1.020e-02
Clock 100Mhz Data 50Mhz	8.604e-03	8.993e-03	1.024e-02	1.180e-02
Clock = 0 Data 100Mhz	5.551e-03	5.253e-03	5.153e-03	5.104e-03
Clock = 1 Data 100Mhz	1.467e-03	7.934e-04	5.688e-04	4.566e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.536	4.2432
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0014	0.0011	0.0011	0.0011
D	0.0010	0.0008	0.0008	0.0008
TE	0.0010	0.0011	0.0011	0.0011

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0907	0.0788	3.7397	1.9011
CP to QN ↑	0.0931	0.0587	5.8974	2.8288
CP to TQ ↓	0.0652	0.0397	5.0980	3.5402
CP to TQ ↑	0.0649	0.0550	11.4894	8.0896
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0743	0.0803	0.9556	0.5035
CP to QN ↑	0.0607	0.0654	1.4339	0.7387
CP to TQ ↓	0.0411	0.0429	4.6674	4.6857
CP to TQ ↑	0.0558	0.0574	10.5018	11.0677

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1039	0.1088	0.1088	0.1088
CP ↑	min_pulse_width to CP	0.0548	0.0346	0.0346	0.0360
D ↓	hold_rising to CP	-0.0746	-0.0289	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0284	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1121	0.0733	0.0733	0.0733
D ↑	setup_rising to CP	0.0583	0.0319	0.0319	0.0319
TE ↓	hold_rising to CP	-0.0474	-0.0294	-0.0294	-0.0267
TE ↑	hold_rising to CP	-0.0382	-0.0208	-0.0208	-0.0208
TE ↓	setup_rising to CP	0.0950	0.0734	0.0734	0.0734
TE ↑	setup_rising to CP	0.1785	0.1492	0.1492	0.1492
TI ↓	hold_rising to CP	-0.1489	-0.0905	-0.0905	-0.0905
TI ↑	hold_rising to CP	-0.0437	-0.0228	-0.0228	-0.0228
TI ↓	setup_rising to CP	0.1851	0.1433	0.1433	0.1433
TI ↑	setup_rising to CP	0.0734	0.0527	0.0527	0.0527

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	7.226e-07	1.000e-20
X8_P16	8.490e-07	1.000e-20
X17_P16	1.001e-06	1.000e-20
X33_P16	1.288e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16

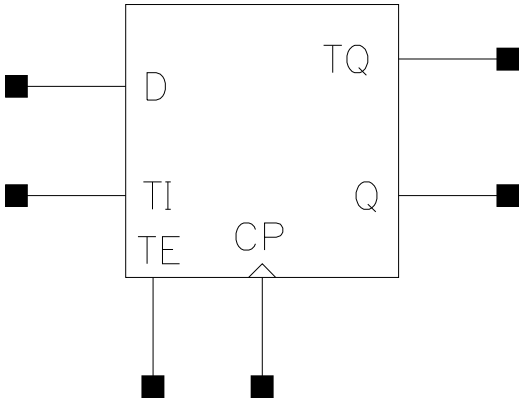
Clock 100Mhz Data 0Mhz	8.665e-03	8.653e-03	8.649e-03	8.648e-03
Clock 100Mhz Data 25Mhz	8.892e-03	9.116e-03	9.451e-03	1.034e-02
Clock 100Mhz Data 50Mhz	9.120e-03	9.580e-03	1.025e-02	1.202e-02
Clock = 0 Data 100Mhz	5.524e-03	5.231e-03	5.135e-03	5.088e-03
Clock = 1 Data 100Mhz	1.477e-03	7.621e-04	5.239e-04	4.048e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.400	4.0800
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008

TE	0.0010	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0925	0.0482	4.2885	1.9484
CP to Q ↑	0.0724	0.0586	6.1507	2.8812
CP to TQ ↓	0.0891	0.0496	4.2644	4.7769
CP to TQ ↑	0.0740	0.0641	8.1301	11.1974
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0668	0.0733	0.9620	0.5018
CP to Q ↑	0.0979	0.1035	1.4464	0.7268
CP to TQ ↓	0.0693	0.0770	4.6142	4.6977
CP to TQ ↑	0.1036	0.1115	10.9464	11.0697

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1039	0.1088	0.1088	0.1088
CP ↑	min_pulse_width to CP	0.0787	0.0360	0.0313	0.0313
D ↓	hold_rising to CP	-0.0746	-0.0289	-0.0321	-0.0321
D ↑	hold_rising to CP	-0.0284	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1144	0.0733	0.0765	0.0765
D ↑	setup_rising to CP	0.0583	0.0319	0.0319	0.0319
TE ↓	hold_rising to CP	-0.0506	-0.0267	-0.0289	-0.0289
TE ↑	hold_rising to CP	-0.0382	-0.0212	-0.0208	-0.0208
TE ↓	setup_rising to CP	0.0950	0.0734	0.0734	0.0734
TE ↑	setup_rising to CP	0.1812	0.1492	0.1492	0.1492
TI ↓	hold_rising to CP	-0.1489	-0.0905	-0.0946	-0.0903
TI ↑	hold_rising to CP	-0.0437	-0.0228	-0.0237	-0.0237
TI ↓	setup_rising to CP	0.1851	0.1433	0.1449	0.1449
TI ↑	setup_rising to CP	0.0734	0.0527	0.0527	0.0527

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	7.364e-07	1.000e-20
X8_P16	8.069e-07	1.000e-20
X17_P16	1.082e-06	1.000e-20
X33_P16	1.324e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

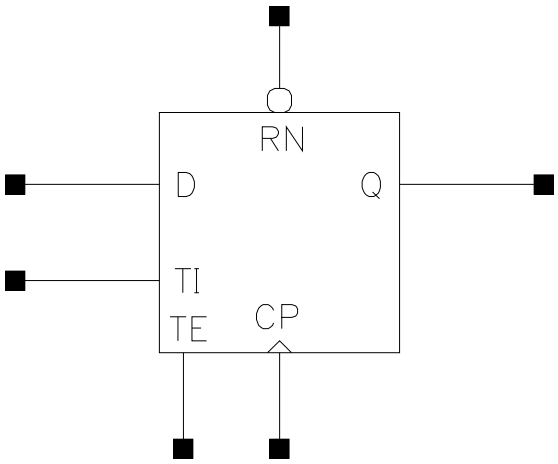
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	8.489e-03	8.567e-03	8.586e-03	8.598e-03
Clock 100Mhz Data 25Mhz	8.885e-03	8.912e-03	9.679e-03	1.050e-02
Clock 100Mhz Data 50Mhz	9.282e-03	9.257e-03	1.077e-02	1.240e-02
Clock = 0 Data 100Mhz	5.500e-03	5.213e-03	5.119e-03	5.072e-03
Clock = 1 Data 100Mhz	1.465e-03	7.564e-04	5.202e-04	4.022e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.672	4.4064
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
RN	0.0009	0.0008	0.0008	0.0008
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0847	0.0462	4.3537	1.9587
CP to Q ↑	0.0695	0.0592	6.0736	2.9006
RN to Q ↓	0.0726	0.0647	3.7549	2.0453
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0683	0.0750	0.9440	0.4994
CP to Q ↑	0.0868	0.0920	1.4120	0.7225
RN to Q ↓	0.0950	0.1017	0.9414	0.4984

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1147	0.1101	0.1141	0.1141
CP ↑	min_pulse_width to CP	0.0704	0.0359	0.0346	0.0346
D ↓	hold_rising to CP	-0.0670	-0.0191	-0.0246	-0.0246
D ↑	hold_rising to CP	-0.0359	-0.0067	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1144	0.0733	0.0733	0.0733
D ↑	setup_rising to CP	0.0658	0.0394	0.0417	0.0417
RN ↓	min_pulse_width to RN	0.0752	0.0806	0.0735	0.0735
RN ↑	recovery_rising to CP	0.0222	0.0222	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0147	-0.0131	-0.0104	-0.0104
TE ↓	hold_rising to CP	-0.0507	-0.0192	-0.0191	-0.0191
TE ↑	hold_rising to CP	-0.0457	-0.0315	-0.0315	-0.0315
TE ↓	setup_rising to CP	0.0950	0.0684	0.0716	0.0716
TE ↑	setup_rising to CP	0.1812	0.1443	0.1443	0.1443
TI ↓	hold_rising to CP	-0.1391	-0.0759	-0.0759	-0.0759
TI ↑	hold_rising to CP	-0.0501	-0.0328	-0.0326	-0.0326
TI ↓	setup_rising to CP	0.1852	0.1391	0.1400	0.1384
TI ↑	setup_rising to CP	0.0832	0.0641	0.0640	0.0640

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	7.811e-07	1.000e-20
X8_P16	8.562e-07	1.000e-20
X17_P16	1.120e-06	1.000e-20
X33_P16	1.387e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	9.480e-03	9.573e-03	9.643e-03	9.680e-03

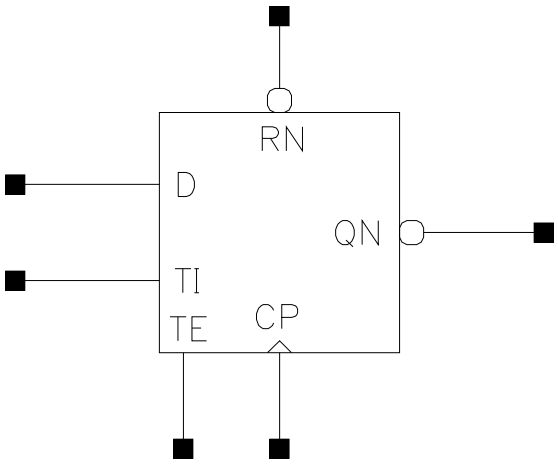
Clock 100Mhz Data 25Mhz	9.546e-03	9.589e-03	1.053e-02	1.136e-02
Clock 100Mhz Data 50Mhz	9.613e-03	9.604e-03	1.141e-02	1.305e-02
Clock = 0 Data 100Mhz	5.665e-03	5.279e-03	5.150e-03	5.086e-03
Clock = 1 Data 100Mhz	1.502e-03	8.330e-04	6.097e-04	4.984e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	3.944	4.7328
X33_P16	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
RN	0.0009	0.0009	0.0009	0.0009
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to QN ↓	0.0784	0.0732	3.5350	1.8406
CP to QN ↑	0.0869	0.0549	5.8823	2.7951
RN to QN ↑	0.0822	0.0833	5.8658	2.7919
	X17_P16	X33_P16	X17_P16	X33_P16
CP to QN ↓	0.0728	0.0801	0.9443	0.4984
CP to QN ↑	0.0614	0.0680	1.4244	0.7325
RN to QN ↑	0.0871	0.0957	1.4288	0.7332

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1147	0.1101	0.1101	0.1101
CP ↑	min_pulse_width to CP	0.0531	0.0346	0.0359	0.0406
D ↓	hold_rising to CP	-0.0702	-0.0191	-0.0191	-0.0191
D ↑	hold_rising to CP	-0.0359	-0.0088	-0.0067	-0.0067
D ↓	setup_rising to CP	0.1144	0.0733	0.0733	0.0733
D ↑	setup_rising to CP	0.0658	0.0394	0.0394	0.0394
RN ↓	min_pulse_width to RN	0.0730	0.0735	0.0872	0.0898
RN ↑	recovery_rising to CP	0.0222	0.0222	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0147	-0.0125	-0.0131	-0.0131
TE ↓	hold_rising to CP	-0.0507	-0.0192	-0.0192	-0.0192
TE ↑	hold_rising to CP	-0.0457	-0.0315	-0.0315	-0.0315
TE ↓	setup_rising to CP	0.0950	0.0684	0.0684	0.0684
TE ↑	setup_rising to CP	0.1812	0.1443	0.1443	0.1443
TI ↓	hold_rising to CP	-0.1391	-0.0759	-0.0759	-0.0759
TI ↑	hold_rising to CP	-0.0494	-0.0328	-0.0328	-0.0328
TI ↓	setup_rising to CP	0.1852	0.1391	0.1384	0.1384
TI ↑	setup_rising to CP	0.0847	0.0641	0.0640	0.0640

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	7.872e-07	1.000e-20
X8_P16	8.395e-07	1.000e-20
X17_P16	1.094e-06	1.000e-20
X33_P16	1.309e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	9.368e-03	9.339e-03	9.327e-03	9.321e-03

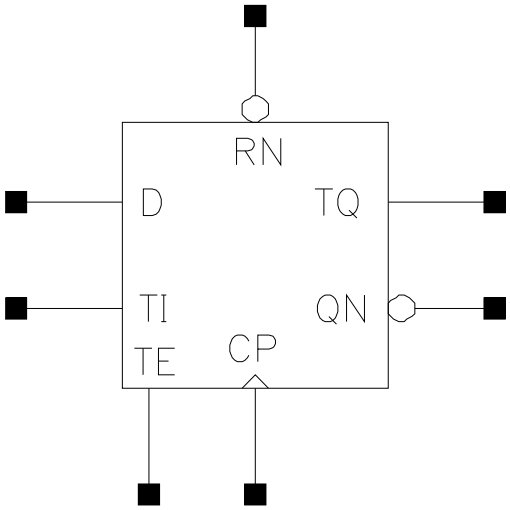
Clock 100Mhz Data 25Mhz	9.409e-03	9.483e-03	1.018e-02	1.096e-02
Clock 100Mhz Data 50Mhz	9.451e-03	9.626e-03	1.104e-02	1.261e-02
Clock = 0 Data 100Mhz	5.678e-03	5.294e-03	5.172e-03	5.111e-03
Clock = 1 Data 100Mhz	1.500e-03	7.932e-04	5.576e-04	4.401e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008

RN	0.0012	0.0008	0.0009	0.0009
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0877	0.0762	3.5403	1.9385
CP to QN ↑	0.1127	0.0616	5.2449	2.9100
CP to TQ ↓	0.0806	0.0421	4.5684	3.7095
CP to TQ ↑	0.0715	0.0595	9.1349	8.4683
RN to QN ↑	0.0817	0.0821	5.2919	2.9019
RN to TQ ↓	0.0571	0.0564	4.1163	3.8866
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0788	0.0848	0.9633	0.5099
CP to QN ↑	0.0628	0.0664	1.4534	0.7336
CP to TQ ↓	0.0437	0.0453	4.5762	4.4696
CP to TQ ↑	0.0596	0.0610	7.9289	8.0277
RN to QN ↑	0.0855	0.0916	1.4501	0.7319
RN to TQ ↓	0.0602	0.0629	4.7553	4.6842

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1147	0.1101	0.1141	0.1141
CP ↑	min_pulse_width to CP	0.0738	0.0359	0.0360	0.0359
D ↓	hold_rising to CP	-0.0670	-0.0191	-0.0191	-0.0191
D ↑	hold_rising to CP	-0.0359	-0.0061	-0.0088	-0.0088
D ↓	setup_rising to CP	0.1144	0.0733	0.0733	0.0733
D ↑	setup_rising to CP	0.0658	0.0394	0.0417	0.0417
RN ↓	min_pulse_width to RN	0.0779	0.0779	0.0801	0.0876
RN ↑	recovery_rising to CP	0.0221	0.0222	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0174	-0.0125	-0.0131	-0.0131
TE ↓	hold_rising to CP	-0.0507	-0.0192	-0.0191	-0.0192
TE ↑	hold_rising to CP	-0.0457	-0.0315	-0.0315	-0.0315
TE ↓	setup_rising to CP	0.0950	0.0684	0.0684	0.0684
TE ↑	setup_rising to CP	0.1812	0.1443	0.1443	0.1443
TI ↓	hold_rising to CP	-0.1391	-0.0759	-0.0759	-0.0759
TI ↑	hold_rising to CP	-0.0494	-0.0328	-0.0328	-0.0328
TI ↓	setup_rising to CP	0.1852	0.1391	0.1384	0.1384
TI ↑	setup_rising to CP	0.0847	0.0641	0.0640	0.0640

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	8.452e-07	1.000e-20
X8_P16	8.838e-07	1.000e-20
X17_P16	1.038e-06	1.000e-20
X33_P16	1.301e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

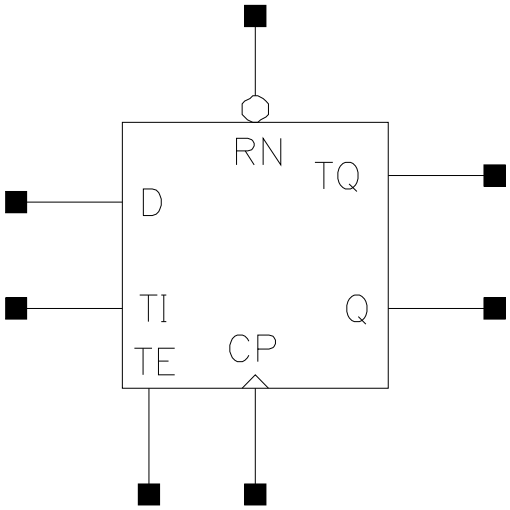
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	9.388e-03	9.389e-03	9.432e-03	9.456e-03
Clock 100Mhz Data 25Mhz	9.674e-03	9.699e-03	1.013e-02	1.104e-02
Clock 100Mhz Data 50Mhz	9.960e-03	1.001e-02	1.082e-02	1.262e-02
Clock = 0 Data 100Mhz	5.654e-03	5.273e-03	5.142e-03	5.076e-03
Clock = 1 Data 100Mhz	1.500e-03	8.136e-04	5.850e-04	4.707e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0010
D	0.0010	0.0008	0.0008	0.0008

RN	0.0009	0.0009	0.0008	0.0008
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0957	0.0501	4.5964	2.0173
CP to Q ↑	0.0742	0.0618	6.2962	3.0182
CP to TQ ↓	0.0917	0.0501	5.6447	4.8338
CP to TQ ↑	0.0766	0.0651	12.3510	11.1967
RN to Q ↓	0.0752	0.0731	3.9276	2.1114
RN to TQ ↓	0.0739	0.0721	4.9171	5.0326
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0704	0.0775	0.9564	0.5060
CP to Q ↑	0.0874	0.0930	1.4183	0.7253
CP to TQ ↓	0.0729	0.0820	4.6430	4.7240
CP to TQ ↑	0.0928	0.1014	11.0735	11.1300
RN to Q ↓	0.0971	0.1041	0.9553	0.5054
RN to TQ ↓	0.0996	0.1086	4.6400	4.7236

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1147	0.1101	0.1101	0.1101
CP ↑	min_pulse_width to CP	0.0834	0.0406	0.0346	0.0346
D ↓	hold_rising to CP	-0.0675	-0.0191	-0.0219	-0.0219
D ↑	hold_rising to CP	-0.0359	-0.0067	-0.0088	-0.0088
D ↓	setup_rising to CP	0.1144	0.0733	0.0733	0.0733
D ↑	setup_rising to CP	0.0658	0.0394	0.0394	0.0394
RN ↓	min_pulse_width to RN	0.0779	0.0898	0.0708	0.0708
RN ↑	recovery_rising to CP	0.0222	0.0222	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0121	-0.0125	-0.0131	-0.0131
TE ↓	hold_rising to CP	-0.0507	-0.0192	-0.0192	-0.0192
TE ↑	hold_rising to CP	-0.0457	-0.0315	-0.0315	-0.0315
TE ↓	setup_rising to CP	0.0950	0.0684	0.0684	0.0684
TE ↑	setup_rising to CP	0.1812	0.1443	0.1443	0.1443
TI ↓	hold_rising to CP	-0.1351	-0.0759	-0.0759	-0.0759
TI ↑	hold_rising to CP	-0.0501	-0.0285	-0.0328	-0.0328
TI ↓	setup_rising to CP	0.1852	0.1391	0.1391	0.1391
TI ↑	setup_rising to CP	0.0832	0.0641	0.0641	0.0641

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	8.178e-07	1.000e-20
X8_P16	8.897e-07	1.000e-20
X17_P16	1.145e-06	1.000e-20
X33_P16	1.412e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

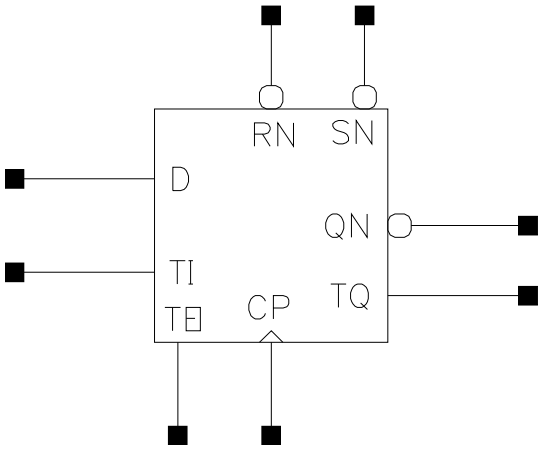
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	9.446e-03	9.544e-03	9.573e-03	9.589e-03
Clock 100Mhz Data 25Mhz	9.712e-03	9.740e-03	1.065e-02	1.151e-02
Clock 100Mhz Data 50Mhz	9.978e-03	9.937e-03	1.172e-02	1.343e-02
Clock = 0 Data 100Mhz	5.660e-03	5.277e-03	5.150e-03	5.087e-03
Clock = 1 Data 100Mhz	1.502e-03	7.725e-04	5.295e-04	4.080e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.352	5.2224
X17_P16	1.200	4.488	5.3856
X33_P16	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011
D	0.0007	0.0007	0.0007
RN	0.0009	0.0009	0.0009

SN	0.0014	0.0014	0.0014
TE	0.0012	0.0012	0.0012
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
CP to QN ↓	0.0839	0.0895	1.8778	0.9702
CP to QN ↑	0.0631	0.0664	2.8100	1.4250
CP to TQ ↓	0.0483	0.0482	5.7863	5.7950
CP to TQ ↑	0.0689	0.0689	14.7192	14.7319
RN to QN ↓	0.0909	0.0964	1.8772	0.9704
RN to QN ↑	0.0910	0.0958	2.8134	1.4259
RN to TQ ↓	0.0700	0.0697	6.2165	6.2156
RN to TQ ↑	0.0764	0.0765	14.6888	14.7067
SN to QN ↓	0.0960	0.1028	1.8855	0.9730
SN to TQ ↑	0.0790	0.0789	14.8914	14.9091
	X33_P16		X33_P16	
CP to QN ↓	0.1030		0.5183	
CP to QN ↑	0.0742		0.7322	
CP to TQ ↓	0.0483		5.8045	
CP to TQ ↑	0.0691		14.7606	
RN to QN ↓	0.1097		0.5192	
RN to QN ↑	0.1059		0.7319	
RN to TQ ↓	0.0697		6.2254	
RN to TQ ↑	0.0767		14.7277	
SN to QN ↓	0.1178		0.5187	
SN to TQ ↑	0.0792		14.9627	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1189	0.1189	0.1189
CP ↑	min_pulse_width to CP	0.0358	0.0392	0.0406
D ↓	hold_rising to CP	-0.0246	-0.0246	-0.0246
D ↑	hold_rising to CP	-0.0061	-0.0061	-0.0061
D ↓	setup_rising to CP	0.0781	0.0781	0.0781
D ↑	setup_rising to CP	0.0417	0.0417	0.0417
RN ↓	min_pulse_width to RN	0.0850	0.0898	0.0947
RN ↑	non_seq_hold_rising to SN	-0.0310	-0.0310	-0.0310
RN ↑	non_seq_setup_rising to SN	0.0739	0.0739	0.0739
RN ↑	recovery_rising to CP	0.0319	0.0319	0.0319
RN ↑	removal_rising to CP	-0.0196	-0.0196	-0.0196
SN ↓	min_pulse_width to SN	0.0696	0.0696	0.0771
SN ↑	recovery_rising to CP	0.0102	0.0102	0.0102
SN ↑	removal_rising to CP	0.0309	0.0309	0.0309

TE ↓	hold_rising to CP	-0.0192	-0.0192	-0.0192
TE ↑	hold_rising to CP	-0.0315	-0.0315	-0.0315
TE ↓	setup_rising to CP	0.0765	0.0765	0.0765
TE ↑	setup_rising to CP	0.1492	0.1492	0.1492
TI ↓	hold_rising to CP	-0.0759	-0.0759	-0.0759
TI ↑	hold_rising to CP	-0.0328	-0.0328	-0.0328
TI ↓	setup_rising to CP	0.1433	0.1433	0.1449
TI ↑	setup_rising to CP	0.0681	0.0638	0.0681

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	9.919e-07	1.000e-20
X17_P16	1.117e-06	1.000e-20
X33_P16	1.345e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

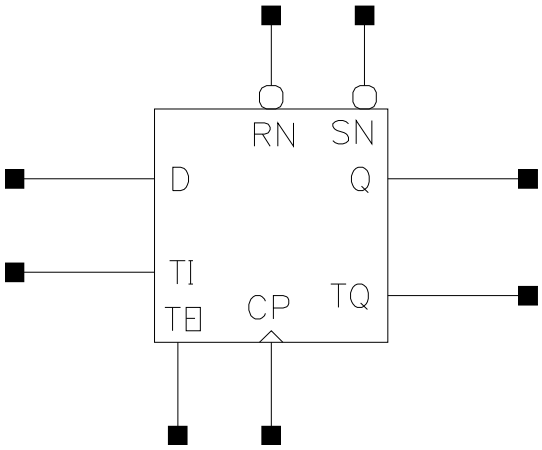
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	9.898e-03	9.898e-03	9.899e-03
Clock 100Mhz Data 25Mhz	1.015e-02	1.052e-02	1.147e-02
Clock 100Mhz Data 50Mhz	1.039e-02	1.114e-02	1.304e-02
Clock = 0 Data 100Mhz	5.091e-03	5.090e-03	5.091e-03
Clock = 1 Data 100Mhz	1.588e-04	1.589e-04	1.590e-04

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.216	5.0592
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011
D	0.0007	0.0007	0.0007
RN	0.0010	0.0010	0.0009

SN	0.0014	0.0015	0.0015
TE	0.0012	0.0012	0.0012
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
CP to Q ↓	0.0542	0.0609	1.9564	1.0191
CP to Q ↑	0.0673	0.0713	2.8977	1.4797
CP to TQ ↓	0.0555	0.0633	5.8882	5.9722
CP to TQ ↑	0.0743	0.0821	14.1622	14.2704
RN to Q ↓	0.0830	0.0967	2.2128	1.1594
RN to Q ↑	0.0600	0.0684	3.0129	1.5467
RN to TQ ↓	0.0837	0.0982	6.3880	6.5531
RN to TQ ↑	0.0707	0.0851	14.3267	14.4465
SN to Q ↑	0.0795	0.0878	3.0148	1.5466
SN to TQ ↑	0.0902	0.1045	14.3281	14.4503
	X33_P16		X33_P16	
CP to Q ↓	0.0774		0.5524	
CP to Q ↑	0.0819		0.7718	
CP to TQ ↓	0.0769		6.2110	
CP to TQ ↑	0.0965		14.4712	
RN to Q ↓	0.1296		0.6399	
RN to Q ↑	0.0890		0.8159	
RN to TQ ↓	0.1240		6.9890	
RN to TQ ↑	0.1130		14.6727	
SN to Q ↑	0.1081		0.8153	
SN to TQ ↑	0.1321		14.6772	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1189	0.1189	0.1189
CP ↑	min_pulse_width to CP	0.0406	0.0500	0.0642
D ↓	hold_rising to CP	-0.0224	-0.0192	-0.0192
D ↑	hold_rising to CP	-0.0067	-0.0067	-0.0067
D ↓	setup_rising to CP	0.0781	0.0781	0.0781
D ↑	setup_rising to CP	0.0417	0.0417	0.0417
RN ↓	min_pulse_width to RN	0.0974	0.1143	0.1506
RN ↑	non_seq_hold_rising to SN	-0.0359	-0.0457	-0.0603
RN ↑	non_seq_setup_rising to SN	0.0690	0.0692	0.0969
RN ↑	recovery_rising to CP	0.0271	0.0271	0.0271
RN ↑	removal_rising to CP	-0.0174	-0.0174	-0.0174
SN ↓	min_pulse_width to SN	0.0745	0.0869	0.1113
SN ↑	recovery_rising to CP	0.0102	0.0102	0.0102
SN ↑	removal_rising to CP	0.0309	0.0309	0.0309

TE ↓	hold_rising to CP	-0.0192	-0.0192	-0.0192
TE ↑	hold_rising to CP	-0.0315	-0.0315	-0.0289
TE ↓	setup_rising to CP	0.0765	0.0765	0.0765
TE ↑	setup_rising to CP	0.1492	0.1492	0.1492
TI ↓	hold_rising to CP	-0.0759	-0.0759	-0.0759
TI ↑	hold_rising to CP	-0.0328	-0.0285	-0.0293
TI ↓	setup_rising to CP	0.1433	0.1433	0.1449
TI ↑	setup_rising to CP	0.0681	0.0681	0.0674

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P16	9.955e-07	1.000e-20
X17_P16	1.133e-06	1.000e-20
X33_P16	1.393e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

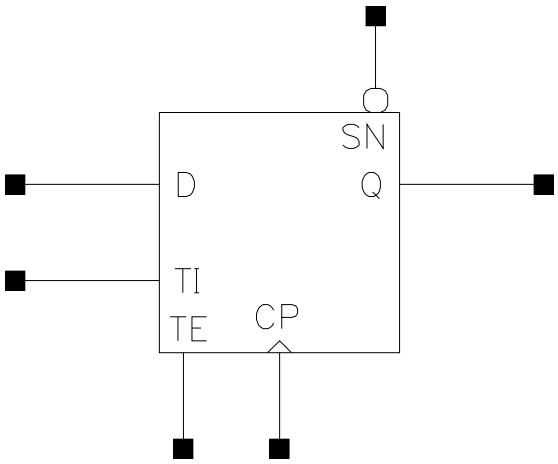
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	9.901e-03	9.903e-03	9.904e-03
Clock 100Mhz Data 25Mhz	1.004e-02	1.048e-02	1.164e-02
Clock 100Mhz Data 50Mhz	1.018e-02	1.106e-02	1.337e-02
Clock = 0 Data 100Mhz	5.086e-03	5.086e-03	5.086e-03
Clock = 1 Data 100Mhz	1.368e-04	1.369e-04	1.370e-04

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0005	0.0005	0.0005
SN	0.0016	0.0016	0.0015	0.0016
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004
	X33_P16			

CP	0.0011			
D	0.0005			
SN	0.0015			
TE	0.0011			
TI	0.0004			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0849	0.0477	4.3684	1.9423
CP to Q ↑	0.0721	0.0618	6.1212	2.8838
SN to Q ↑	0.0546	0.0620	5.9596	2.8837
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to Q ↓	0.0673	0.0712	0.9440	0.6566
CP to Q ↑	0.0873	0.0904	1.4114	0.9587
SN to Q ↑	0.0867	0.0898	1.4111	0.9601
	X33_P16		**X33_P16**	
CP to Q ↓	0.0740		0.4995	
CP to Q ↑	0.0924		0.7234	
SN to Q ↑	0.0919		0.7232	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.1181	0.1188	0.1188	0.1188
CP ↑	min_pulse_width to CP	0.0739	0.0360	0.0313	0.0313
D ↓	hold_rising to CP	-0.0702	-0.0240	-0.0240	-0.0240
D ↑	hold_rising to CP	-0.0333	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1170	0.0781	0.0781	0.0781
D ↑	setup_rising to CP	0.0632	0.0368	0.0368	0.0368
SN ↓	min_pulse_width to SN	0.0474	0.0571	0.0544	0.0544
SN ↑	recovery_rising to CP	0.0102	0.0102	0.0102	0.0102
SN ↑	removal_rising to CP	0.0238	0.0309	0.0309	0.0309
TE ↓	hold_rising to CP	-0.0506	-0.0218	-0.0240	-0.0240
TE ↑	hold_rising to CP	-0.0431	-0.0266	-0.0266	-0.0266
TE ↓	setup_rising to CP	0.0998	0.0761	0.0761	0.0761
TE ↑	setup_rising to CP	0.1834	0.1524	0.1524	0.1524
TI ↓	hold_rising to CP	-0.1391	-0.0808	-0.0841	-0.0841
TI ↑	hold_rising to CP	-0.0485	-0.0279	-0.0277	-0.0277
TI ↓	setup_rising to CP	0.1885	0.1446	0.1446	0.1446
TI ↑	setup_rising to CP	0.0798	0.0576	0.0576	0.0576
		X33_P16			

CP ↓	min_pulse_width to CP	0.1188			
CP ↑	min_pulse_width to CP	0.0313			
D ↓	hold_rising to CP	-0.0240			
D ↑	hold_rising to CP	-0.0071			
D ↓	setup_rising to CP	0.0781			
D ↑	setup_rising to CP	0.0368			
SN ↓	min_pulse_width to SN	0.0544			
SN ↑	recovery_rising to CP	0.0102			
SN ↑	removal_rising to CP	0.0309			
TE ↓	hold_rising to CP	-0.0240			
TE ↑	hold_rising to CP	-0.0266			
TE ↓	setup_rising to CP	0.0761			
TE ↑	setup_rising to CP	0.1524			
TI ↓	hold_rising to CP	-0.0841			
TI ↑	hold_rising to CP	-0.0277			
TI ↓	setup_rising to CP	0.1446			
TI ↑	setup_rising to CP	0.0576			

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	7.840e-07	1.000e-20
X8_P16	8.712e-07	1.000e-20
X17_P16	1.127e-06	1.000e-20
X25_P16	1.235e-06	1.000e-20
X33_P16	1.342e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	9.191e-03	9.314e-03	9.354e-03	9.374e-03
Clock 100Mhz Data 25Mhz	9.312e-03	9.473e-03	1.032e-02	1.077e-02
Clock 100Mhz Data 50Mhz	9.433e-03	9.631e-03	1.129e-02	1.217e-02
Clock = 0 Data 100Mhz	5.481e-03	5.209e-03	5.119e-03	5.074e-03
Clock = 1 Data 100Mhz	1.501e-03	7.974e-04	5.629e-04	4.456e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	9.386e-03			

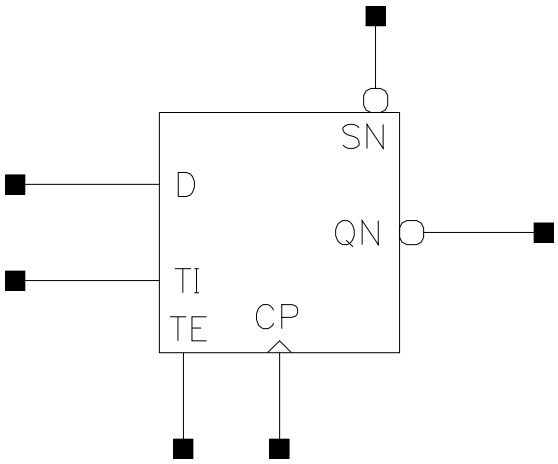
Clock 100Mhz Data 25Mhz	1.113e-02			
Clock 100Mhz Data 50Mhz	1.288e-02			
Clock = 0 Data 100Mhz	5.047e-03			
Clock = 1 Data 100Mhz	3.753e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0005	0.0005	0.0005
SN	0.0016	0.0015	0.0016	0.0016
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004
	X33_P16			

CP	0.0011			
D	0.0005			
SN	0.0016			
TE	0.0011			
TI	0.0004			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0815	0.0740	3.5356	1.8434
CP to QN ↑	0.0874	0.0546	5.8774	2.8037
SN to QN ↓	0.0653	0.0733	3.5196	1.8434
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to QN ↓	0.0773	0.0819	0.9476	0.6587
CP to QN ↑	0.0644	0.0686	1.4140	0.9606
SN to QN ↓	0.0781	0.0828	0.9484	0.6579
	X33_P16		**X33_P16**	
CP to QN ↓	0.0855		0.5013	
CP to QN ↑	0.0715		0.7245	
SN to QN ↓	0.0864		0.5004	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.1181	0.1188	0.1188	0.1188
CP ↑	min_pulse_width to CP	0.0548	0.0313	0.0360	0.0407
D ↓	hold_rising to CP	-0.0702	-0.0240	-0.0240	-0.0240
D ↑	hold_rising to CP	-0.0333	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1170	0.0781	0.0781	0.0781
D ↑	setup_rising to CP	0.0632	0.0368	0.0368	0.0368
SN ↓	min_pulse_width to SN	0.0474	0.0544	0.0571	0.0593
SN ↑	recovery_rising to CP	0.0102	0.0102	0.0102	0.0102
SN ↑	removal_rising to CP	0.0238	0.0309	0.0309	0.0309
TE ↓	hold_rising to CP	-0.0506	-0.0240	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0431	-0.0266	-0.0266	-0.0266
TE ↓	setup_rising to CP	0.0998	0.0761	0.0761	0.0761
TE ↑	setup_rising to CP	0.1834	0.1524	0.1524	0.1550
TI ↓	hold_rising to CP	-0.1391	-0.0841	-0.0808	-0.0808
TI ↑	hold_rising to CP	-0.0485	-0.0277	-0.0279	-0.0279
TI ↓	setup_rising to CP	0.1885	0.1446	0.1446	0.1446
TI ↑	setup_rising to CP	0.0798	0.0576	0.0576	0.0576
		X33_P16			

CP ↓	min_pulse_width to CP	0.1188			
CP ↑	min_pulse_width to CP	0.0407			
D ↓	hold_rising to CP	-0.0240			
D ↑	hold_rising to CP	-0.0071			
D ↓	setup_rising to CP	0.0781			
D ↑	setup_rising to CP	0.0368			
SN ↓	min_pulse_width to SN	0.0620			
SN ↑	recovery_rising to CP	0.0102			
SN ↑	removal_rising to CP	0.0309			
TE ↓	hold_rising to CP	-0.0218			
TE ↑	hold_rising to CP	-0.0266			
TE ↓	setup_rising to CP	0.0761			
TE ↑	setup_rising to CP	0.1524			
TI ↓	hold_rising to CP	-0.0808			
TI ↑	hold_rising to CP	-0.0279			
TI ↓	setup_rising to CP	0.1446			
TI ↑	setup_rising to CP	0.0576			

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	7.856e-07	1.000e-20
X8_P16	8.862e-07	1.000e-20
X17_P16	1.148e-06	1.000e-20
X25_P16	1.280e-06	1.000e-20
X33_P16	1.414e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	9.182e-03	9.296e-03	9.325e-03	9.340e-03
Clock 100Mhz Data 25Mhz	9.221e-03	9.436e-03	1.028e-02	1.073e-02
Clock 100Mhz Data 50Mhz	9.261e-03	9.576e-03	1.124e-02	1.211e-02
Clock = 0 Data 100Mhz	5.481e-03	5.213e-03	5.121e-03	5.076e-03
Clock = 1 Data 100Mhz	1.501e-03	8.082e-04	5.769e-04	4.614e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	9.349e-03			

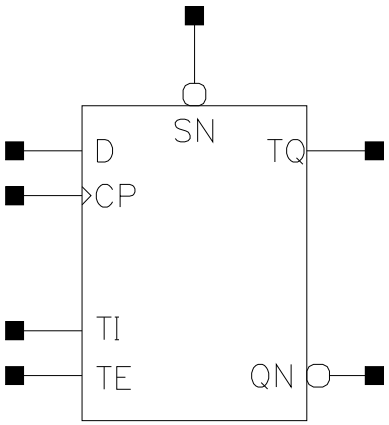
Clock 100Mhz Data 25Mhz	1.112e-02			
Clock 100Mhz Data 50Mhz	1.289e-02			
Clock = 0 Data 100Mhz	5.049e-03			
Clock = 1 Data 100Mhz	3.921e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.216	5.0592
X8_P16	1.200	4.080	4.8960
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0005	0.0005	0.0005

SN	0.0017	0.0018	0.0018	0.0018
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0937	0.0777	3.5269	1.8511
CP to QN ↑	0.1133	0.0617	5.7796	2.8604
CP to TQ ↓	0.0818	0.0426	5.1490	4.2812
CP to TQ ↑	0.0718	0.0585	8.1088	7.8749
SN to QN ↓	0.0626	0.0598	3.5238	1.8533
SN to TQ ↑	0.0435	0.0423	7.9596	7.8434
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0779	0.0860	0.9736	0.4954
CP to QN ↑	0.0697	0.0769	1.4251	0.7281
CP to TQ ↓	0.0525	0.0524	4.4609	4.4650
CP to TQ ↑	0.0656	0.0657	7.9775	7.9930
SN to QN ↓	0.0667	0.0745	0.9728	0.4944
SN to TQ ↑	0.0540	0.0540	7.9624	7.9853

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1181	0.1188	0.1188	0.1188
CP ↑	min_pulse_width to CP	0.0752	0.0346	0.0406	0.0454
D ↓	hold_rising to CP	-0.0702	-0.0240	-0.0240	-0.0240
D ↑	hold_rising to CP	-0.0333	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1170	0.0781	0.0781	0.0781
D ↑	setup_rising to CP	0.0632	0.0368	0.0368	0.0368
SN ↓	min_pulse_width to SN	0.0447	0.0447	0.0474	0.0500
SN ↑	recovery_rising to CP	0.0102	0.0102	0.0102	0.0102
SN ↑	removal_rising to CP	0.0239	0.0309	0.0309	0.0309
TE ↓	hold_rising to CP	-0.0506	-0.0240	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0431	-0.0266	-0.0266	-0.0266
TE ↓	setup_rising to CP	0.0998	0.0757	0.0757	0.0757
TE ↑	setup_rising to CP	0.1834	0.1524	0.1550	0.1550
TI ↓	hold_rising to CP	-0.1391	-0.0848	-0.0808	-0.0808
TI ↑	hold_rising to CP	-0.0485	-0.0279	-0.0279	-0.0279
TI ↓	setup_rising to CP	0.1885	0.1446	0.1446	0.1446
TI ↑	setup_rising to CP	0.0798	0.0576	0.0576	0.0576

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	8.566e-07	1.000e-20
X8_P16	9.555e-07	1.000e-20
X17_P16	1.217e-06	1.000e-20
X33_P16	1.483e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

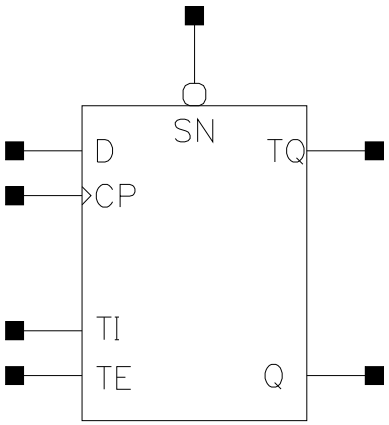
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	9.197e-03	9.431e-03	9.511e-03	9.551e-03
Clock 100Mhz Data 25Mhz	9.573e-03	9.783e-03	1.058e-02	1.141e-02
Clock 100Mhz Data 50Mhz	9.950e-03	1.013e-02	1.165e-02	1.327e-02
Clock = 0 Data 100Mhz	5.487e-03	5.217e-03	5.127e-03	5.082e-03
Clock = 1 Data 100Mhz	1.502e-03	7.768e-04	5.353e-04	4.146e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.944	4.7328
X17_P16	1.200	4.216	5.0592
X33_P16	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0005	0.0005	0.0005

SN	0.0017	0.0016	0.0015	0.0015
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0978	0.0512	4.4923	1.9869
CP to Q ↑	0.0770	0.0642	6.1622	2.9227
CP to TQ ↓	0.0972	0.0527	6.4138	4.8436
CP to TQ ↑	0.0759	0.0706	8.1796	11.2636
SN to Q ↑	0.0467	0.0649	5.9705	2.9177
SN to TQ ↑	0.0458	0.0720	7.9821	11.2385
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0689	0.0755	0.9707	0.5088
CP to Q ↑	0.0887	0.0937	1.4169	0.7260
CP to TQ ↓	0.0714	0.0801	4.6415	4.7122
CP to TQ ↑	0.0942	0.1023	11.0795	11.1537
SN to Q ↑	0.0880	0.0930	1.4191	0.7264
SN to TQ ↑	0.0935	0.1016	11.0797	11.1557

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1181	0.1188	0.1188	0.1188
CP ↑	min_pulse_width to CP	0.0834	0.0407	0.0313	0.0313
D ↓	hold_rising to CP	-0.0702	-0.0240	-0.0240	-0.0240
D ↑	hold_rising to CP	-0.0333	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1170	0.0781	0.0781	0.0781
D ↑	setup_rising to CP	0.0632	0.0368	0.0368	0.0368
SN ↓	min_pulse_width to SN	0.0447	0.0620	0.0544	0.0544
SN ↑	recovery_rising to CP	0.0102	0.0102	0.0102	0.0102
SN ↑	removal_rising to CP	0.0238	0.0309	0.0309	0.0309
TE ↓	hold_rising to CP	-0.0506	-0.0218	-0.0240	-0.0240
TE ↑	hold_rising to CP	-0.0431	-0.0266	-0.0266	-0.0266
TE ↓	setup_rising to CP	0.0998	0.0761	0.0761	0.0761
TE ↑	setup_rising to CP	0.1834	0.1524	0.1524	0.1524
TI ↓	hold_rising to CP	-0.1391	-0.0808	-0.0841	-0.0841
TI ↑	hold_rising to CP	-0.0485	-0.0279	-0.0277	-0.0277
TI ↓	setup_rising to CP	0.1885	0.1446	0.1446	0.1446
TI ↑	setup_rising to CP	0.0798	0.0576	0.0576	0.0576

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	8.367e-07	1.000e-20
X8_P16	9.075e-07	1.000e-20
X17_P16	1.158e-06	1.000e-20
X33_P16	1.373e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

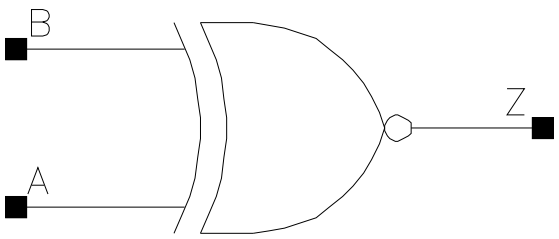
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	9.208e-03	9.443e-03	9.521e-03	9.560e-03
Clock 100Mhz Data 25Mhz	9.544e-03	9.748e-03	1.064e-02	1.150e-02
Clock 100Mhz Data 50Mhz	9.880e-03	1.005e-02	1.175e-02	1.344e-02
Clock = 0 Data 100Mhz	5.488e-03	5.212e-03	5.121e-03	5.074e-03
Clock = 1 Data 100Mhz	1.502e-03	7.768e-04	5.352e-04	4.145e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P16	X8_P16	X17_P16	X25_P16
A	0.0019	0.0008	0.0011	0.0017
B	0.0018	0.0016	0.0021	0.0028
	X33_P16			
A	0.0019			
B	0.0033			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X8_P16**	**X6_P16**	**X8_P16**
A to Z ↓	0.0227	0.0509	3.4535	1.9975
A to Z ↑	0.0237	0.0454	4.4386	2.9737
B to Z ↓	0.0212	0.0354	3.4505	1.9833
B to Z ↑	0.0238	0.0331	4.4514	2.9651
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
A to Z ↓	0.0484	0.0490	0.9855	0.6799
A to Z ↑	0.0419	0.0425	1.4597	0.9696

B to Z ↓	0.0367	0.0358	0.9826	0.6784
B to Z ↑	0.0332	0.0324	1.4567	0.9672
	X33_P16		**X33_P16**	
A to Z ↓	0.0464		0.5100	
A to Z ↑	0.0414		0.7291	
B to Z ↓	0.0344		0.5088	
B to Z ↑	0.0321		0.7279	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P16	4.155e-07	1.000e-20
X8_P16	4.353e-07	1.000e-20
X17_P16	7.311e-07	1.000e-20
X25_P16	1.135e-06	1.000e-20
X33_P16	1.539e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	2.913e-03	5.331e-03	7.601e-03	1.225e-02
B to Z	2.743e-03	3.698e-03	5.740e-03	9.060e-03
	X33_P16			
A to Z	1.499e-02			
B to Z	1.143e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

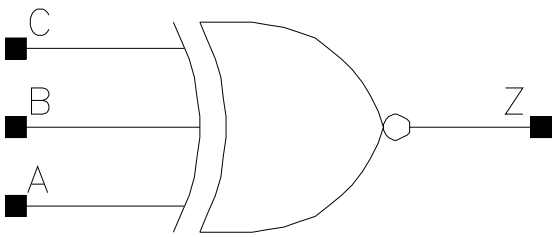
Pin Cycle (vdds)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P16			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	2.176	2.6112
X16_P16	1.200	2.720	3.2640
X25_P16	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X16_P16	X25_P16
A	0.0032	0.0027	0.0034	0.0050
B	0.0035	0.0024	0.0033	0.0045
C	0.0023	0.0008	0.0008	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0358	0.0594	4.0972	2.1231
A to Z ↑	0.0339	0.0543	6.2809	2.9424
B to Z ↓	0.0366	0.0592	4.0982	2.1229
B to Z ↑	0.0342	0.0546	6.2744	2.9429
C to Z ↓	0.0359	0.0785	4.0940	2.1218
C to Z ↑	0.0329	0.0727	6.2578	2.9425
	X16_P16	**X25_P16**	**X16_P16**	**X25_P16**
A to Z ↓	0.0595	0.0598	1.0904	0.6976
A to Z ↑	0.0586	0.0581	1.5477	0.9735
B to Z ↓	0.0596	0.0604	1.0900	0.6971

B to Z ↑	0.0589	0.0593	1.5486	0.9739
C to Z ↓	0.0832	0.0885	1.0902	0.6970
C to Z ↑	0.0811	0.0862	1.5489	0.9734

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	5.623e-07	1.000e-20
X8_P16	5.280e-07	1.000e-20
X16_P16	8.543e-07	1.000e-20
X25_P16	1.240e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	3.327e-03	4.303e-03	6.982e-03	1.051e-02
B to Z	3.031e-03	4.177e-03	6.801e-03	1.028e-02
C to Z	2.982e-03	6.455e-03	9.644e-03	1.448e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

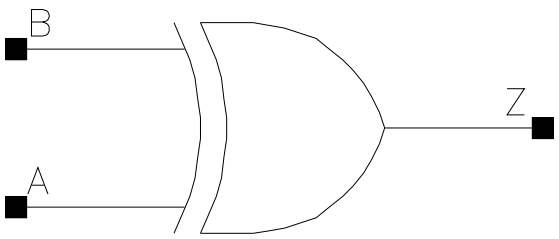
Pin Cycle (vdds)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.224	1.4688
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.224	1.4688
X16_P16	1.200	1.360	1.6320
X25_P16	1.200	2.176	2.6112
X31_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X16_P16
A	0.0008	0.0018	0.0011	0.0013
B	0.0014	0.0017	0.0017	0.0019
	X25_P16	X31_P16		
A	0.0017	0.0022		
B	0.0029	0.0038		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0455	0.0229	3.5930	2.6580
A to Z ↑	0.0425	0.0244	5.7463	5.5790
B to Z ↓	0.0326	0.0231	3.5749	2.6765
B to Z ↑	0.0325	0.0227	5.7427	5.5788
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0414	0.0433	1.9538	1.0124

A to Z ↑	0.0372	0.0394	2.8891	1.4613
B to Z ↓	0.0319	0.0334	1.9489	1.0109
B to Z ↑	0.0301	0.0321	2.8868	1.4603
	X25_P16	**X31_P16**	**X25_P16**	**X31_P16**
A to Z ↓	0.0460	0.0432	0.6750	0.5414
A to Z ↑	0.0415	0.0396	0.9675	0.7836
B to Z ↓	0.0348	0.0327	0.6741	0.5410
B to Z ↑	0.0317	0.0304	0.9670	0.7827

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	3.500e-07	1.000e-20
X6_P16	4.016e-07	1.000e-20
X8_P16	5.526e-07	1.000e-20
X16_P16	8.206e-07	1.000e-20
X25_P16	1.126e-06	1.000e-20
X31_P16	1.522e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	4.037e-03	2.932e-03	4.946e-03	7.174e-03
B to Z	3.092e-03	2.686e-03	4.035e-03	5.935e-03
	X25_P16	X31_P16		
A to Z	1.116e-02	1.371e-02		
B to Z	7.946e-03	9.729e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

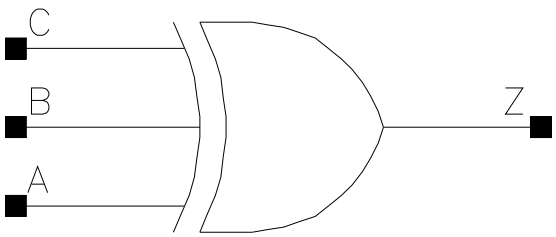
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P16	X31_P16		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X24_P16	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X24_P16
A	0.0028	0.0027	0.0034	0.0060
B	0.0028	0.0024	0.0031	0.0050
C	0.0008	0.0018	0.0026	0.0040

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0362	0.0593	4.3161	2.1220
A to Z ↑	0.0342	0.0542	6.8955	2.9399
B to Z ↓	0.0364	0.0595	4.3183	2.1223
B to Z ↑	0.0342	0.0545	6.8877	2.9400
C to Z ↓	0.0617	0.0579	4.2886	2.1227
C to Z ↑	0.0599	0.0528	6.8683	2.9387
	X17_P16	**X24_P16**	**X17_P16**	**X24_P16**
A to Z ↓	0.0545	0.0637	1.0139	0.7311
A to Z ↑	0.0541	0.0488	1.4326	0.9757
B to Z ↓	0.0547	0.0640	1.0140	0.7303

B to Z ↑	0.0542	0.0489	1.4334	0.9762
C to Z ↓	0.0538	0.0619	1.0140	0.7298
C to Z ↑	0.0534	0.0482	1.4329	0.9761

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	5.958e-07	1.000e-20
X8_P16	4.639e-07	1.000e-20
X17_P16	8.188e-07	1.000e-20
X24_P16	1.344e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	3.029e-03	4.331e-03	6.769e-03	1.160e-02
B to Z	2.889e-03	4.158e-03	6.495e-03	1.115e-02
C to Z	6.018e-03	4.036e-03	6.440e-03	1.083e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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