C28SOI_SC_12_PR_LR User Manual

12 track Standard Cell library comprising Place and Route cells

Overview

Features

- 12-track Standard Cell library
- The library consists of 64 cells
- Based on low power regular V_T transistors

Applications

- These cells are used for Place and Route.

Library Architecture

In C28SOI_SC_12_PR_LR library, all pins are located on the vertical and horizontal pin grids. Although, only some place and route tools require all pins on grids, most of the tools work more efficiently with all pins on grids.

Figure 1. Layout for Single Height Cell

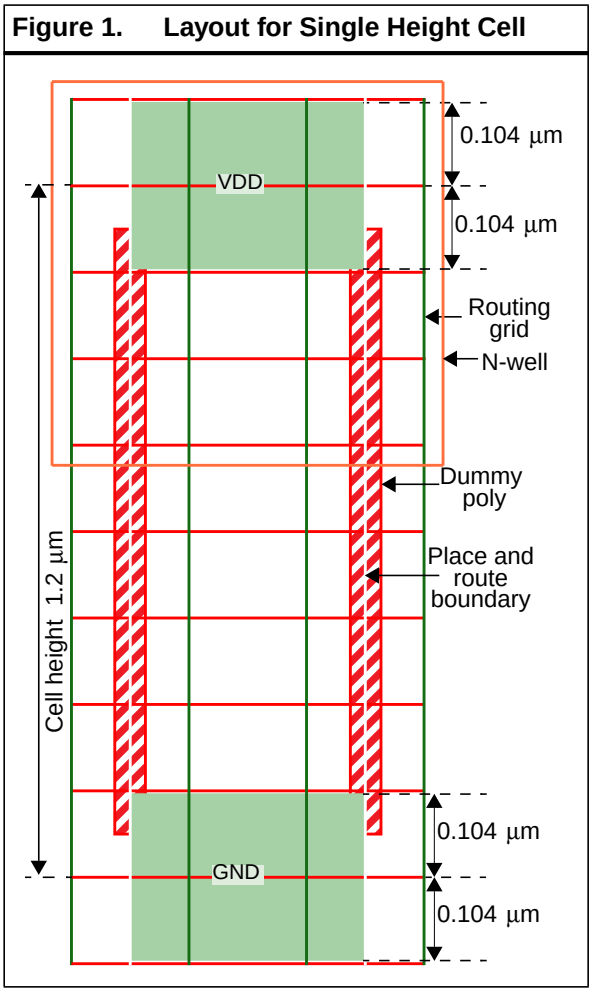

Table 1. Physical Specifications

Parameter	Measurement (µ m)
Drawn gate length	0.03
Layout grid	0.001
Vertical pin grid	0.10
Horizontal grid	0.136
Cell power and ground rail width	0.208

1 Quick References

This section provides reference information about the Standard Cell library.

	*This document is compatible for viewing with acroread 7.0 and higher versions. If opened with a lower version of acroread, there might be some color display problem.*

	*Please refer to the Naming Convention Document available in Design Package for more details regarding cell names.*

2 Functional Specifications

2.1 Cell List

The C28SOI_SC_12_PR_LR library consists of the following cells.

Table 2. Cell List

Cell Name	Number of Cells
ANTPROT	2
DECAP	15
FILLERCELL/FILLERPFOP/FILLERFLPCHKAE	15
FILLERNPW/FILLERSNPW	2
TIE High/Low	2
ANTPROTGVFILLERSNPW	1
FILLERPCEND	27

3 Library Contents

This section describes the content of this library.

3.1 Library Description by Family

This section describes the library content by presenting all families of cells.

3.1.1 Antenna Diodes

This family of cells is completely compliant with CMOS028_FDSOI process.

The ANTPROT3 cell is 3-track cell with MINUS M1 pin. The library contains the following ANTPROT3 cell:

- C12T28SOI_LR_ANTPROT3

The ANTPROT4 cell is 4-track cell with MINUS M1 pin. The library contains the following ANTPROT4 cell:

- C12T28SOI_LR_ANTPROT4

Caution: C12T28SOI_LR_ANTPROT3 is not standalone DRC clean, had to keep other cell on surroundings. To overcome this issue, there is another ANTPROT cell “C12T28SOI_LR_ANTPROT4” which is standalone DRC clean for fully isolated Designs

3.2 Supply Decoupling

Supply Decoupling cells exist for users who want to discharge power nets.

The following are decoupling cells with GO1 transistors:

- C12T28SOI_LR_DECAPXT4
- C12T28SOI_LR_DECAPXT8
- C12T28SOI_LR_DECAPXT16
- C12T28SOI_LR_DECAPXT32
- C12T28SOI_LR_DECAPXT64
- C12T28SOI_LRF_DECAPXT4
- C12T28SOI_LRF_DECAPXT8
- C12T28SOI_LRF_DECAPXT16
- C12T28SOI_LRF_DECAPXT32
- C12T28SOI_LRF_DECAPXT64

The following are decoupling cells with GO2 transistors:

- C12T28SOI_LREGLV_DECAPXT9
- C12T28SOI_LREGLV_DECAPXT12
- C12T28SOI_LREGLV_DECAPXT16
- C12T28SOI_LREGLV_DECAPXT32

- C12T28SOI_LREGLV_DECAPXT64

3.3 TIE High/Low Cells

Following are Tie high and Tie low cells:

- C12T28SOI_LR_TOHX8
- C12T28SOI_LR_TOLX8

3.4 Filler Cells with Pattern Fill

3.4.1 Filler Cells with Pattern Fill for PC

This family of cells is completely compliant with CMOS028_FDSOI process. Poly rectangles (poly on boundary) are present to fill the poly density requirement. The following are the filler cells with pattern fill for PC:

- C12T28SOI_LR_FILLERCELL1
- C12T28SOI_L_FILLERCELL1
- C12T28SOI_L_FILLERCELL2

C12T28SOI_L_FILLERCELL* are cells with no V_T and are used for abuttment with the decoupling cells with GO2 transistors (C12T28SOI_LREGLV_DECAPXT*).

3.4.2 Filler Cells with Pattern Fill for PC and RX

This family of cells is completely compliant with CMOS028_FDSOI process. Poly rectangles are present to fill the PC density requirement. RX rectangles are present to satisfy the minimum RX density requirement. The following are the filler cells with pattern fill for PC and RX:

- C12T28SOI_LR_FILLERPFOP2
- C12T28SOI_LR_FILLERPFOP4
- C12T28SOI_LR_FILLERPFOP8
- C12T28SOI_LR_FILLERPFOP16
- C12T28SOI_LR_FILLERPFOP32
- C12T28SOI_LR_FILLERPFOP64

FILLERPFOP* cells are used at the top and bottom of the design.

Above cells have an endcap of 44nm and are standalone DRC clean and will not highlight the aggressive poly EndCap DRC violations at initial floorplan level.

For the above drawback we have added below cells :

- C12T28SOI_LR_FILLERFLPCHKAE16
- C12T28SOI_LR_FILLERFLPCHKAE2
- C12T28SOI_LR_FILLERFLPCHKAE32
- C12T28SOI_LR_FILLERFLPCHKAE4

- C12T28SOI_LR_FILLERFLPCHKAE64
- C12T28SOI_LR_FILLERFLPCHKAE8

These cells when used during initial floor planning verification will represent real scenario of poly endcap(PCnes), helping designer to take corrective measure in the initial phase itself. These cells have an endcap of37nm.Also These specific cells have intentional DRC error so that it can be checked that it does not remain in final GDS.

3.5 Filler Tie Cells with RX Well-straps with Pattern Fill for PC

The maximum distance from any point inside source/drain RX area to the nearest RX of a well tie within the same NW or PW is defined in DRM to ensure the substrate polarization. RX well-straps cells are necessary to satisfy this rule because there is no substrate strap in Standard cells.

3.5.1 Non-split Filler Cells

This family of cells is completely compliant with CMOS028_FDSOI process. The FILLERNPW4 cells can be used to boost densities for RX and to improve the substrate polarization. The following filler cell with N-well and P-well straps, respectively is connected to abutting rails vdd and gnd:

- C12T28SOI_LR_FILLERNPW4

3.5.2 Split Filler Cells

This family of cells is completely compliant with CMOS028_FDSOI process. PC wires are present to fill the PO density requirement. The following filler cell with N-well and P-well straps, respectively is connected to internal pins, vdds and gnds, and with pattern fill for PC:

- C12T28SOI_LR_FILLERSNPW4

3.5.3 Split Filler Cells with Antenna Diode

This family of cells is completely compliant with CMOS028_FDSOI process, PC wires are present to fill the PO density requirement. The following are the filler cells with N-well and P-well straps, respectively connected to internal pins, vdds and gnds, and with pattern fill for PC.

- C12T28SOI_LR_ANTPROTGVFILLERSNPW8

In cell C12T28SOI_LR_ANTPROTGVFILLERSNPW8, An ANTENNA diode protection is provided between gnd-gnds and vdd-vdds both in to prevent from ANTENNA phenomena at process level.

Caution: “ANTPROTGVFILLERSNPW*, to be used for RVT RBB domains only. It should not be used for FBB domains.

3.6 Filler Cell to Avoid the Aggressive end Capacitance Violation

They are automatically inserted above last and first rows of all Standard Cells block to prevent DRC violation of aggressive PC end capacitance. Small poly rectangles are present to enlarge PC end capacitance at the top and/or at the bottom of first and last line.

- C12T28SOI_RVTFILLERPCENDB1
- C12T28SOI_RVTFILLERPCENDB16
- C12T28SOI_RVTFILLERPCENDB2
- C12T28SOI_RVTFILLERPCENDB32
- C12T28SOI_RVTFILLERPCENDB4
- C12T28SOI_RVTFILLERPCENDB64
- C12T28SOI_RVTFILLERPCENDB8
- C12T28SOI_RVTFILLERPCENDBL1
- C12T28SOI_RVTFILLERPCENDBR1
- C12T28SOI_RVTFILLERPCENDT1
- C12T28SOI_RVTFILLERPCENDT16
- C12T28SOI_RVTFILLERPCENDT2
- C12T28SOI_RVTFILLERPCENDT32
- C12T28SOI_RVTFILLERPCENDT4
- C12T28SOI_RVTFILLERPCENDT64
- C12T28SOI_RVTFILLERPCENDT8
- C12T28SOI_RVTFILLERPCENDTB1
- C12T28SOI_RVTFILLERPCENDTB16
- C12T28SOI_RVTFILLERPCENDTB2
- C12T28SOI_RVTFILLERPCENDTB32
- C12T28SOI_RVTFILLERPCENDTB4
- C12T28SOI_RVTFILLERPCENDTB64
- C12T28SOI_RVTFILLERPCENDTB8
- C12T28SOI_RVTFILLERPCENDTBL1
- C12T28SOI_RVTFILLERPCENDTBR1
- C12T28SOI_RVTFILLERPCENDTL1
- C12T28SOI_RVTFILLERPCENDTR1

3.7 Supported Flow Strategies

Different options are available for process, substrate connection, and V_T implant. For each parameter, the supported options are:

- Process options
  - Single CMOS028_FDSOI process
- Substrate connection options
  - No-split power with substrate straps connected to vdd and gnd
  - Split power with substrate straps connected to vdds and gnds
- V_T implants
  - Single V_T implant: only RVT

3.7.1 Single Process and Single V_T Implant

To illustrate the case of only one process (for example, CMOS028_FDSOI process) and only one V_T (for example, RVT implant), a possible strategy is discussed in further sections.

3.7.1.1 Gaps Filling

- C12T28SOI_LR_FILLERCELL1/FILLERPFOP2/4/8/16/32/64

3.7.1.2 Antenna Diodes

- C12T28SOI_LR_ANTPROT3/C12T28SOI_LR_ANTPROT4

3.7.1.3 No-split Power Substrate Straps (OD well-straps connected to vdd/gnd)

- C12T28SOI_LR_FILLERNPW4

3.7.1.4 Split Power Substrate Straps (OD well-straps connected to vdds/gnds)

- C12T28SOI_LR_FILLERSNPW4

3.7.1.5 Split Power Substrate Straps (OD well-straps connected to vdds and gnds for Nwell and Pwell respectively) with Antenna Protection Diode

- C12T28SOI_LR_ANTPROTGVFILLERSNPW8

4 Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

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