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C28SOI_SC_12_CLK_LR Databook

12 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

Overview

- C28SOI_SC_12_CLK_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 332 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

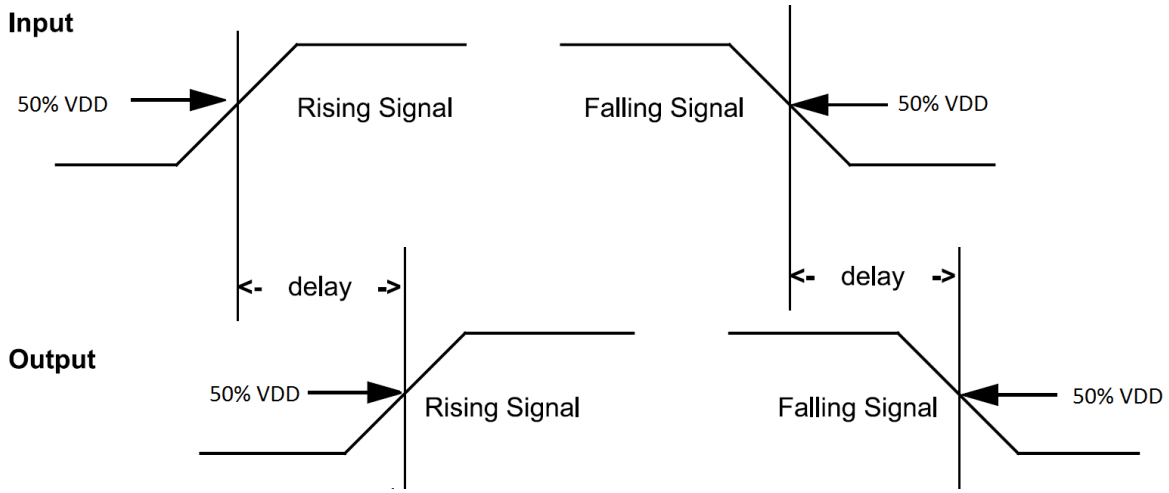


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

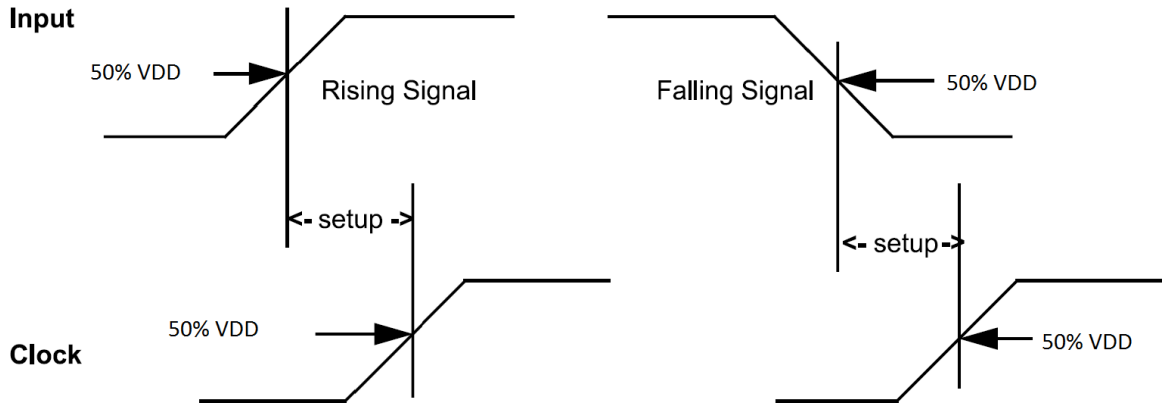


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

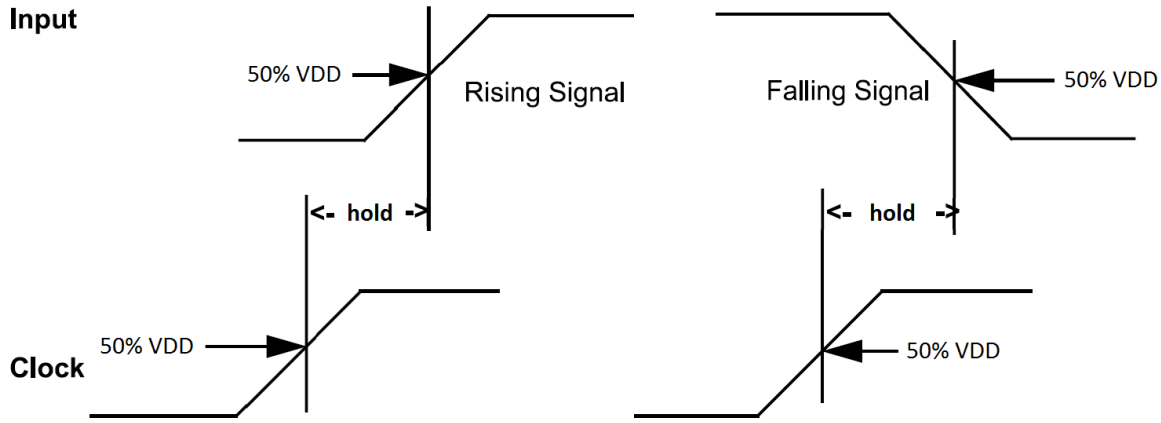


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

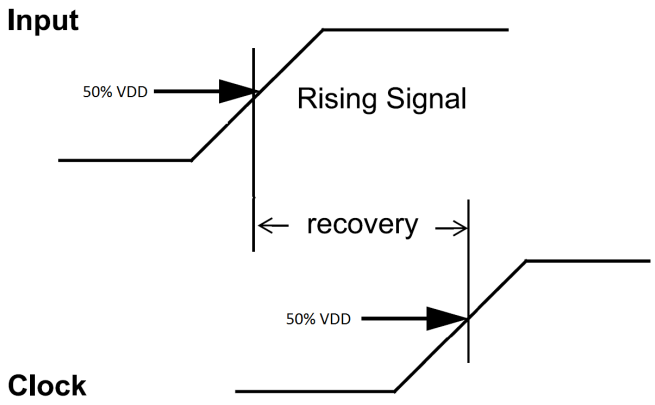


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

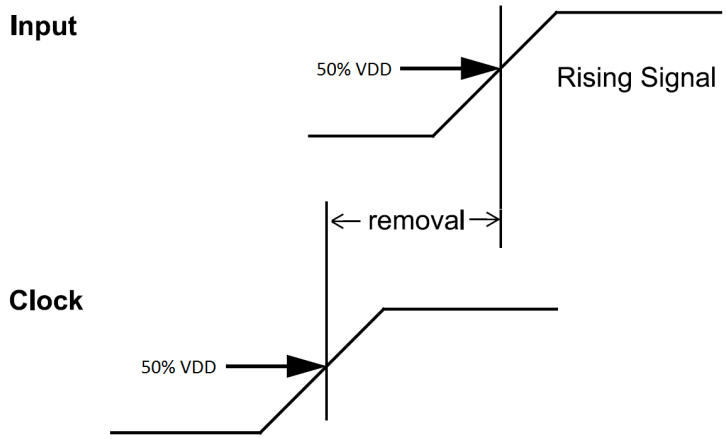


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

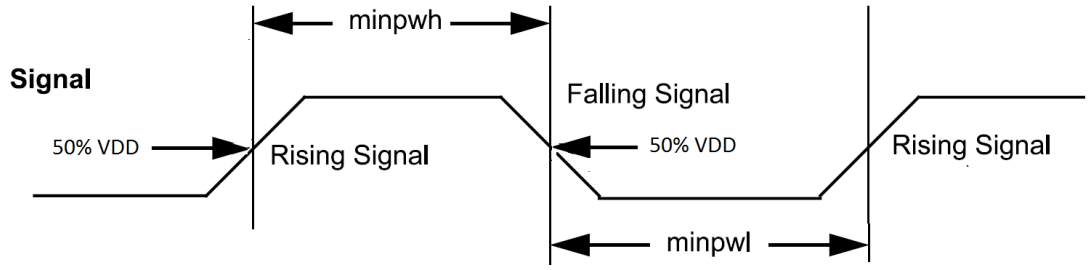


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

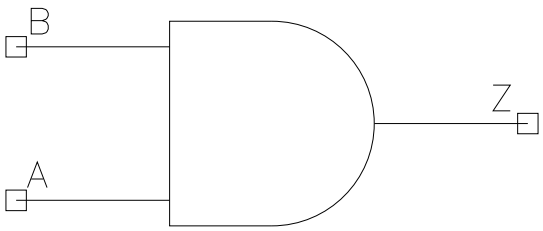
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

CNAND2

Cell Description

2 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.680	0.8160
X15_P4	1.200	0.680	0.8160
X15_P10	1.200	0.680	0.8160
X15_P16	1.200	0.680	0.8160
X20_P0	1.200	0.816	0.9792
X20_P4	1.200	0.816	0.9792
X20_P10	1.200	0.816	0.9792
X20_P16	1.200	0.816	0.9792
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0009	0.0009	0.0010	0.0010
B	0.0008	0.0009	0.0009	0.0009
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0009	0.0009	0.0009	0.0010
B	0.0008	0.0008	0.0009	0.0009
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0014	0.0015	0.0016	0.0016
B	0.0014	0.0015	0.0016	0.0016

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0298	0.0335	1.0249	1.0994
A to Z ↑	0.0234	0.0259	1.4772	1.6201
B to Z ↓	0.0285	0.0321	1.0248	1.0986
B to Z ↑	0.0240	0.0269	1.4773	1.6214
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0388	0.0440	1.2068	1.3052
A to Z ↑	0.0295	0.0333	1.8496	2.0739
B to Z ↓	0.0369	0.0420	1.2058	1.3046
B to Z ↑	0.0307	0.0347	1.8468	2.0746
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0335	0.0377	0.7609	0.8171
A to Z ↑	0.0266	0.0295	1.0934	1.2007
B to Z ↓	0.0324	0.0363	0.7606	0.8161
B to Z ↑	0.0275	0.0307	1.0935	1.2002
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0438	0.0497	0.8972	0.9708
A to Z ↑	0.0338	0.0381	1.3681	1.5379
B to Z ↓	0.0421	0.0479	0.8965	0.9704
B to Z ↑	0.0352	0.0398	1.3701	1.5397
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0326	0.0369	0.4361	0.4666
A to Z ↑	0.0234	0.0262	0.7500	0.8206
B to Z ↓	0.0301	0.0339	0.4349	0.4653
B to Z ↑	0.0235	0.0263	0.7487	0.8206
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0428	0.0487	0.5106	0.5516
A to Z ↑	0.0299	0.0337	0.9337	1.0482
B to Z ↓	0.0394	0.0446	0.5100	0.5507
B to Z ↑	0.0302	0.0340	0.9352	1.0486

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X15_P0	7.956e-07	2.022e-12
X15_P4	2.274e-07	2.023e-12
X15_P10	1.402e-07	2.023e-12
X15_P16	1.389e-07	2.026e-12
X20_P0	9.911e-07	2.275e-12
X20_P4	2.765e-07	2.275e-12
X20_P10	1.716e-07	2.275e-12
X20_P16	1.709e-07	2.275e-12
X33_P0	1.553e-06	3.284e-12
X33_P4	4.731e-07	3.282e-12
X33_P10	3.022e-07	3.282e-12
X33_P16	3.024e-07	3.283e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	2.723e-05	2.178e-05	1.642e-05	1.424e-05
B (output stable)	6.686e-05	6.650e-05	6.427e-05	6.009e-05
A to Z	3.457e-03	3.489e-03	3.584e-03	3.750e-03

B to Z	3.277e-03	3.292e-03	3.358e-03	3.519e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.739e-05	2.189e-05	1.648e-05	1.394e-05
B (output stable)	6.560e-05	6.683e-05	6.407e-05	6.196e-05
A to Z	4.625e-03	4.652e-03	4.788e-03	5.002e-03
B to Z	4.453e-03	4.449e-03	4.562e-03	4.773e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	8.589e-05	6.328e-05	4.383e-05	3.466e-05
B (output stable)	3.607e-04	3.630e-04	3.650e-04	3.645e-04
A to Z	7.051e-03	7.125e-03	7.318e-03	7.632e-03
B to Z	6.417e-03	6.437e-03	6.606e-03	6.883e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

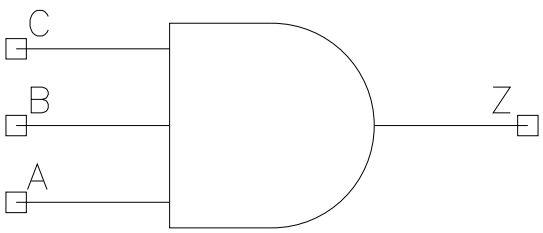
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	7.055e-08	5.080e-08	2.945e-08	7.800e-09
B (output stable)	6.048e-08	3.690e-08	1.440e-08	-1.280e-08
A to Z	-1.764e-07	6.490e-08	-1.112e-07	-4.842e-07
B to Z	-1.106e-07	-1.840e-08	-3.043e-07	-5.302e-07
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	7.351e-08	5.399e-08	2.484e-08	9.900e-09
B (output stable)	6.150e-08	3.450e-08	1.580e-08	-8.700e-09
A to Z	-1.957e-07	1.910e-08	-4.826e-07	-6.728e-07
B to Z	-1.724e-07	-1.718e-07	-3.287e-07	-4.561e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	5.600e-08	3.090e-08	4.850e-08	-8.000e-10
B (output stable)	4.640e-08	3.400e-09	-1.540e-08	-9.400e-08
A to Z	-4.686e-07	-9.920e-08	-1.021e-06	-5.913e-07
B to Z	-5.251e-07	-4.730e-08	-9.787e-07	-5.716e-07

CNAND3

Cell Description

3 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X25_P0	1.200	1.360	1.6320
X25_P4	1.200	1.360	1.6320
X25_P10	1.200	1.360	1.6320
X25_P16	1.200	1.360	1.6320
X33_P0	1.200	1.768	2.1216
X33_P4	1.200	1.768	2.1216
X33_P10	1.200	1.768	2.1216
X33_P16	1.200	1.768	2.1216

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0008	0.0009	0.0009	0.0009
B	0.0008	0.0008	0.0009	0.0009
C	0.0008	0.0008	0.0009	0.0009
	X25_P0	X25_P4	X25_P10	X25_P16
A	0.0017	0.0018	0.0018	0.0019
B	0.0015	0.0016	0.0017	0.0017
C	0.0015	0.0015	0.0016	0.0017
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0019	0.0020	0.0022	0.0022
B	0.0018	0.0019	0.0020	0.0021

C	0.0018	0.0018	0.0019	0.0021

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0385	0.0430	0.8608	0.9223
A to Z ↑	0.0334	0.0372	1.0664	1.1669
B to Z ↓	0.0375	0.0418	0.8602	0.9214
B to Z ↑	0.0344	0.0379	1.0665	1.1672
C to Z ↓	0.0362	0.0404	0.8586	0.9205
C to Z ↑	0.0345	0.0382	1.0665	1.1678
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
A to Z ↓	0.0503	0.0571	1.0113	1.0940
A to Z ↑	0.0434	0.0492	1.3320	1.4954
B to Z ↓	0.0489	0.0554	1.0115	1.0940
B to Z ↑	0.0439	0.0494	1.3323	1.4956
C to Z ↓	0.0470	0.0532	1.0113	1.0930
C to Z ↑	0.0443	0.0499	1.3334	1.4957
	X25_P0	**X25_P4**	**X25_P0**	**X25_P4**
A to Z ↓	0.0295	0.0330	0.5855	0.6266
A to Z ↑	0.0265	0.0295	1.0122	1.1072
B to Z ↓	0.0283	0.0317	0.5855	0.6262
B to Z ↑	0.0273	0.0302	1.0134	1.1084
C to Z ↓	0.0269	0.0300	0.5853	0.6258
C to Z ↑	0.0274	0.0303	1.0135	1.1085
	X25_P10	**X25_P16**	**X25_P10**	**X25_P16**
A to Z ↓	0.0383	0.0433	0.6853	0.7408
A to Z ↑	0.0342	0.0388	1.2605	1.4128
B to Z ↓	0.0368	0.0415	0.6858	0.7407
B to Z ↑	0.0348	0.0391	1.2619	1.4124
C to Z ↓	0.0347	0.0391	0.6847	0.7396
C to Z ↑	0.0351	0.0395	1.2612	1.4128
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0313	0.0349	0.4249	0.4561
A to Z ↑	0.0293	0.0325	0.5223	0.5708
B to Z ↓	0.0302	0.0337	0.4248	0.4554
B to Z ↑	0.0303	0.0333	0.5218	0.5714
C to Z ↓	0.0291	0.0324	0.4244	0.4550
C to Z ↑	0.0305	0.0337	0.5225	0.5713
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0406	0.0457	0.5009	0.5423
A to Z ↑	0.0377	0.0427	0.6498	0.7282
B to Z ↓	0.0391	0.0440	0.5006	0.5415
B to Z ↑	0.0384	0.0431	0.6508	0.7293
C to Z ↓	0.0375	0.0422	0.5003	0.5411
C to Z ↑	0.0388	0.0436	0.6502	0.7289

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P0	9.504e-07	2.528e-12
X17_P4	2.563e-07	2.528e-12

X17_P10	1.739e-07	2.527e-12
X17_P16	1.792e-07	2.526e-12
X25_P0	1.173e-06	3.283e-12
X25_P4	3.760e-07	3.282e-12
X25_P10	2.748e-07	3.284e-12
X25_P16	2.854e-07	3.283e-12
X33_P0	1.933e-06	4.040e-12
X33_P4	5.492e-07	4.038e-12
X33_P10	3.826e-07	4.039e-12
X33_P16	3.943e-07	4.040e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	1.882e-05	1.302e-05	6.918e-06	5.793e-06
B (output stable)	6.308e-05	5.594e-05	3.956e-05	2.667e-05
C (output stable)	7.979e-05	4.405e-05	2.515e-05	2.227e-05
A to Z	5.097e-03	5.035e-03	5.225e-03	5.375e-03
B to Z	4.922e-03	4.845e-03	5.017e-03	5.152e-03
C to Z	4.751e-03	4.654e-03	4.803e-03	4.932e-03
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	3.386e-05	2.088e-05	1.190e-05	8.306e-06
B (output stable)	1.238e-04	1.103e-04	7.691e-05	5.184e-05
C (output stable)	1.612e-04	8.897e-05	4.925e-05	4.413e-05
A to Z	6.368e-03	6.412e-03	6.661e-03	6.933e-03
B to Z	5.993e-03	6.010e-03	6.237e-03	6.479e-03
C to Z	5.629e-03	5.599e-03	5.793e-03	6.011e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	4.089e-05	2.569e-05	1.429e-05	1.216e-05
B (output stable)	1.501e-04	1.344e-04	9.390e-05	6.346e-05
C (output stable)	1.932e-04	1.053e-04	6.165e-05	5.537e-05
A to Z	9.917e-03	9.892e-03	1.024e-02	1.061e-02
B to Z	9.485e-03	9.418e-03	9.731e-03	1.008e-02
C to Z	9.048e-03	8.932e-03	9.186e-03	9.513e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	7.615e-08	6.226e-08	3.726e-08	1.843e-08
B (output stable)	7.048e-08	3.800e-08	3.516e-08	2.653e-08
C (output stable)	5.587e-08	2.223e-08	2.863e-08	1.753e-08
A to Z	-4.987e-07	-4.460e-08	-3.680e-08	-2.882e-07
B to Z	-9.570e-08	-3.580e-08	-6.795e-07	-3.279e-07
C to Z	-2.389e-07	-4.880e-07	-1.548e-07	-1.200e-07
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	4.637e-08	1.393e-08	-2.707e-08	-6.497e-08
B (output stable)	3.383e-08	-1.443e-08	-4.537e-08	-5.483e-08
C (output stable)	1.173e-08	-5.610e-08	-5.803e-08	-8.883e-08
A to Z	-1.650e-07	-8.558e-07	-7.816e-08	-4.542e-07
B to Z	-5.032e-07	-5.518e-07	-1.723e-07	-3.098e-07
C to Z	-1.737e-07	-3.119e-07	-4.973e-07	-2.952e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	3.673e-08	-1.303e-08	-7.063e-08	-1.039e-07

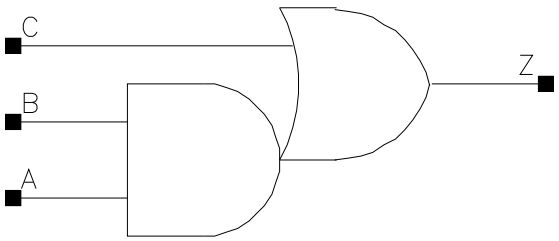
B (output stable)	2.672e-08	-4.893e-08	-8.263e-08	-1.114e-07
C (output stable)	-1.537e-08	-1.003e-07	-9.943e-08	-1.537e-07
A to Z	-4.588e-07	-5.065e-07	-1.528e-06	-1.169e-06
B to Z	-1.139e-06	-8.851e-07	-7.478e-07	-1.146e-06
C to Z	-2.317e-07	-6.963e-07	-8.494e-07	-5.609e-07

CNAO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	1.632	1.9584
X33_P4	1.200	1.632	1.9584
X33_P10	1.200	1.632	1.9584
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0018	0.0018	0.0019	0.0020
B	0.0016	0.0016	0.0017	0.0017
C	0.0015	0.0016	0.0016	0.0017

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0346	0.0396	0.4397	0.4716
A to Z ↑	0.0277	0.0310	0.7474	0.8185
B to Z ↓	0.0330	0.0376	0.4397	0.4714
B to Z ↑	0.0286	0.0321	0.7482	0.8190
C to Z ↓	0.0356	0.0403	0.4383	0.4699
C to Z ↑	0.0289	0.0322	0.7454	0.8159
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0463	0.0525	0.5171	0.5587

A to Z ↑	0.0357	0.0400	0.9340	1.0455
B to Z ↓	0.0439	0.0495	0.5170	0.5585
B to Z ↑	0.0369	0.0412	0.9337	1.0464
C to Z ↓	0.0469	0.0530	0.5150	0.5569
C to Z ↑	0.0368	0.0408	0.9297	1.0419

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X33_P0	1.848e-06	3.787e-12
X33_P4	5.883e-07	3.789e-12
X33_P10	3.314e-07	3.788e-12
X33_P16	3.089e-07	3.786e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	4.076e-05	2.066e-05	1.776e-05	1.464e-05
B (output stable)	1.250e-04	1.156e-04	1.140e-04	1.130e-04
C (output stable)	2.810e-04	2.874e-04	5.830e-04	8.073e-04
A to Z	7.316e-03	7.384e-03	7.584e-03	7.808e-03
B to Z	6.941e-03	6.953e-03	7.114e-03	7.300e-03
C to Z	8.319e-03	8.443e-03	8.711e-03	8.968e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

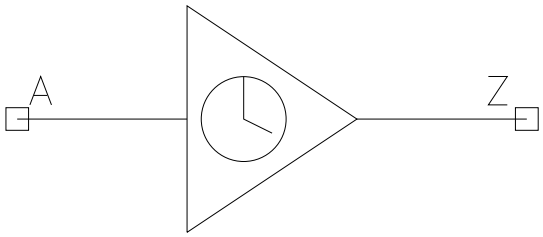
Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	2.139e-05	6.851e-06	7.031e-06	6.104e-06
B (output stable)	5.890e-05	5.009e-05	4.741e-05	4.546e-05
C (output stable)	-2.131e-05	-3.538e-05	-9.817e-05	-1.381e-04
A to Z	-1.063e-06	-7.006e-07	-9.973e-07	-1.461e-06
B to Z	-6.301e-07	-5.827e-07	-8.595e-07	-9.593e-07
C to Z	-5.778e-06	-2.295e-05	-3.042e-05	-3.093e-05

CNBF

Cell Description

Buffer with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X4_P4	1.200	0.408	0.4896
X4_P10	1.200	0.408	0.4896
X4_P16	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X15_P0	1.200	0.544	0.6528
X15_P4	1.200	0.544	0.6528
X15_P10	1.200	0.544	0.6528
X15_P16	1.200	0.544	0.6528
X22_P0	1.200	0.680	0.8160
X22_P4	1.200	0.680	0.8160
X22_P10	1.200	0.680	0.8160
X22_P16	1.200	0.680	0.8160
X30_P0	1.200	0.952	1.1424
X30_P4	1.200	0.952	1.1424
X30_P10	1.200	0.952	1.1424
X30_P16	1.200	0.952	1.1424
X38_P0	1.200	1.088	1.3056
X38_P4	1.200	1.088	1.3056
X38_P10	1.200	1.088	1.3056
X38_P16	1.200	1.088	1.3056
X44_P0	1.200	1.224	1.4688
X44_P4	1.200	1.224	1.4688
X44_P10	1.200	1.224	1.4688
X44_P16	1.200	1.224	1.4688
X52_P0	1.200	1.496	1.7952
X52_P4	1.200	1.496	1.7952
X52_P10	1.200	1.496	1.7952
X52_P16	1.200	1.496	1.7952
X59_P0	1.200	1.632	1.9584

X59_P4	1.200	1.632	1.9584
X59_P10	1.200	1.632	1.9584
X59_P16	1.200	1.632	1.9584
X70_P0	1.200	1.768	2.1216
X70_P4	1.200	1.768	2.1216
X70_P10	1.200	1.768	2.1216
X70_P16	1.200	1.768	2.1216
X94_P0	1.200	2.312	2.7744
X94_P4	1.200	2.312	2.7744
X94_P10	1.200	2.312	2.7744
X94_P16	1.200	2.312	2.7744
X133_P0	1.200	3.264	3.9168
X133_P4	1.200	3.264	3.9168
X133_P10	1.200	3.264	3.9168
X133_P16	1.200	3.264	3.9168

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X4_P4	X4_P10	X4_P16
A	0.0006	0.0007	0.0007	0.0007
	X7_P0	X7_P4	X7_P10	X7_P16
A	0.0007	0.0007	0.0007	0.0007
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0009	0.0009	0.0009	0.0010
	X22_P0	X22_P4	X22_P10	X22_P16
A	0.0010	0.0011	0.0011	0.0012
	X30_P0	X30_P4	X30_P10	X30_P16
A	0.0014	0.0015	0.0015	0.0016
	X38_P0	X38_P4	X38_P10	X38_P16
A	0.0017	0.0017	0.0018	0.0020
	X44_P0	X44_P4	X44_P10	X44_P16
A	0.0017	0.0018	0.0019	0.0020
	X52_P0	X52_P4	X52_P10	X52_P16
A	0.0023	0.0024	0.0025	0.0027
	X59_P0	X59_P4	X59_P10	X59_P16
A	0.0025	0.0027	0.0028	0.0031
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0027	0.0028	0.0029	0.0031
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0035	0.0036	0.0039	0.0041
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0052	0.0054	0.0058	0.0062

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X4_P4	X4_P0	X4_P4
A to Z ↓	0.0294	0.0331	3.6535	3.9194

A to Z ↑	0.0214	0.0239	5.3967	5.9621
	X4_P10	**X4_P16**	**X4_P10**	**X4_P16**
A to Z ↓	0.0382	0.0429	4.3139	4.6707
A to Z ↑	0.0273	0.0305	6.8481	7.7187
	X7_P0	**X7_P4**	**X7_P0**	**X7_P4**
A to Z ↓	0.0290	0.0327	1.9852	2.1258
A to Z ↑	0.0207	0.0232	3.1621	3.4710
	X7_P10	**X7_P16**	**X7_P10**	**X7_P16**
A to Z ↓	0.0380	0.0428	2.3276	2.5155
A to Z ↑	0.0266	0.0296	3.9639	4.4487
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0278	0.0314	1.0404	1.1141
A to Z ↑	0.0214	0.0238	1.4719	1.6142
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0362	0.0411	1.2217	1.3224
A to Z ↑	0.0271	0.0304	1.8421	2.0676
	X22_P0	**X22_P4**	**X22_P0**	**X22_P4**
A to Z ↓	0.0284	0.0322	0.7140	0.7648
A to Z ↑	0.0223	0.0251	0.9924	1.0860
	X22_P10	**X22_P16**	**X22_P10**	**X22_P16**
A to Z ↓	0.0369	0.0418	0.8389	0.9072
A to Z ↑	0.0283	0.0317	1.2400	1.3915
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**
A to Z ↓	0.0268	0.0301	0.4990	0.5353
A to Z ↑	0.0202	0.0226	0.7422	0.8131
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
A to Z ↓	0.0349	0.0395	0.5879	0.6361
A to Z ↑	0.0257	0.0288	0.9261	1.0395
	X38_P0	**X38_P4**	**X38_P0**	**X38_P4**
A to Z ↓	0.0267	0.0300	0.4025	0.4317
A to Z ↑	0.0204	0.0228	0.5959	0.6519
	X38_P10	**X38_P16**	**X38_P10**	**X38_P16**
A to Z ↓	0.0349	0.0395	0.4741	0.5132
A to Z ↑	0.0262	0.0293	0.7433	0.8342
	X44_P0	**X44_P4**	**X44_P0**	**X44_P4**
A to Z ↓	0.0272	0.0306	0.3476	0.3731
A to Z ↑	0.0208	0.0232	0.5237	0.5738
	X44_P10	**X44_P16**	**X44_P10**	**X44_P16**
A to Z ↓	0.0357	0.0403	0.4099	0.4435
A to Z ↑	0.0267	0.0298	0.6544	0.7348
	X52_P0	**X52_P4**	**X52_P0**	**X52_P4**
A to Z ↓	0.0267	0.0302	0.3003	0.3221
A to Z ↑	0.0218	0.0244	0.4377	0.4792
	X52_P10	**X52_P16**	**X52_P10**	**X52_P16**
A to Z ↓	0.0350	0.0395	0.3537	0.3820
A to Z ↑	0.0279	0.0311	0.5460	0.6120
	X59_P0	**X59_P4**	**X59_P0**	**X59_P4**
A to Z ↓	0.0268	0.0300	0.2629	0.2820
A to Z ↑	0.0208	0.0231	0.3879	0.4246
	X59_P10	**X59_P16**	**X59_P10**	**X59_P16**
A to Z ↓	0.0349	0.0393	0.3095	0.3352
A to Z ↑	0.0264	0.0294	0.4838	0.5430

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0281	0.0316	0.2208	0.2368
A to Z ↑	0.0215	0.0240	0.3351	0.3669
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0367	0.0414	0.2598	0.2810
A to Z ↑	0.0275	0.0306	0.4188	0.4694
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0277	0.0311	0.1689	0.1810
A to Z ↑	0.0213	0.0237	0.2551	0.2790
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0360	0.0405	0.1984	0.2148
A to Z ↑	0.0271	0.0302	0.3178	0.3560
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0278	0.0309	0.1254	0.1350
A to Z ↑	0.0216	0.0240	0.1857	0.2035
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0358	0.0403	0.1482	0.1601
A to Z ↑	0.0275	0.0307	0.2312	0.2591

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	3.063e-07	1.519e-12
X4_P4	9.383e-08	1.518e-12
X4_P10	4.662e-08	1.521e-12
X4_P16	4.147e-08	1.520e-12
X7_P0	4.682e-07	1.518e-12
X7_P4	1.378e-07	1.518e-12
X7_P10	6.827e-08	1.521e-12
X7_P16	6.095e-08	1.520e-12
X15_P0	8.240e-07	1.771e-12
X15_P4	2.323e-07	1.900e-12
X15_P10	1.182e-07	1.772e-12
X15_P16	1.073e-07	1.772e-12
X22_P0	1.154e-06	2.023e-12
X22_P4	3.200e-07	2.025e-12
X22_P10	1.654e-07	2.025e-12
X22_P16	1.516e-07	2.025e-12
X30_P0	1.527e-06	2.527e-12
X30_P4	4.391e-07	2.525e-12
X30_P10	2.322e-07	2.527e-12
X30_P16	2.144e-07	2.527e-12
X38_P0	1.886e-06	2.777e-12
X38_P4	5.379e-07	2.775e-12
X38_P10	2.859e-07	2.778e-12
X38_P16	2.648e-07	2.778e-12
X44_P0	2.158e-06	3.033e-12
X44_P4	6.062e-07	3.034e-12
X44_P10	3.214e-07	3.031e-12
X44_P16	2.978e-07	3.031e-12
X52_P0	2.494e-06	3.534e-12
X52_P4	7.140e-07	3.537e-12
X52_P10	3.837e-07	3.534e-12

X52_P16	3.568e-07	3.537e-12
X59_P0	2.923e-06	3.791e-12
X59_P4	8.235e-07	3.793e-12
X59_P10	4.404e-07	3.787e-12
X59_P16	4.096e-07	3.785e-12
X70_P0	3.282e-06	4.040e-12
X70_P4	9.458e-07	4.092e-12
X70_P10	5.102e-07	4.048e-12
X70_P16	4.755e-07	4.040e-12
X94_P0	4.326e-06	5.034e-12
X94_P4	1.248e-06	5.048e-12
X94_P10	6.762e-07	5.050e-12
X94_P16	6.315e-07	5.052e-12
X133_P0	6.099e-06	6.812e-12
X133_P4	1.773e-06	6.810e-12
X133_P10	9.677e-07	6.810e-12
X133_P16	9.056e-07	6.814e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	1.475e-03	1.489e-03	1.536e-03	1.587e-03
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	1.894e-03	1.913e-03	1.978e-03	2.056e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	3.174e-03	3.177e-03	3.275e-03	3.434e-03
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	4.660e-03	4.744e-03	4.829e-03	5.059e-03
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	5.940e-03	5.954e-03	6.138e-03	6.432e-03
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	7.518e-03	7.549e-03	7.867e-03	8.234e-03
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	8.338e-03	8.352e-03	8.682e-03	9.086e-03
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	1.036e-02	1.044e-02	1.079e-02	1.126e-02
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	1.163e-02	1.163e-02	1.207e-02	1.258e-02
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	1.358e-02	1.364e-02	1.412e-02	1.473e-02
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	1.751e-02	1.762e-02	1.820e-02	1.892e-02
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	2.592e-02	2.588e-02	2.663e-02	2.754e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	7.980e-08	1.000e-07	-2.028e-07	-3.242e-07
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	3.920e-08	9.220e-08	-3.164e-07	-2.057e-07
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	7.050e-08	-2.696e-07	-1.450e-07	-1.496e-07

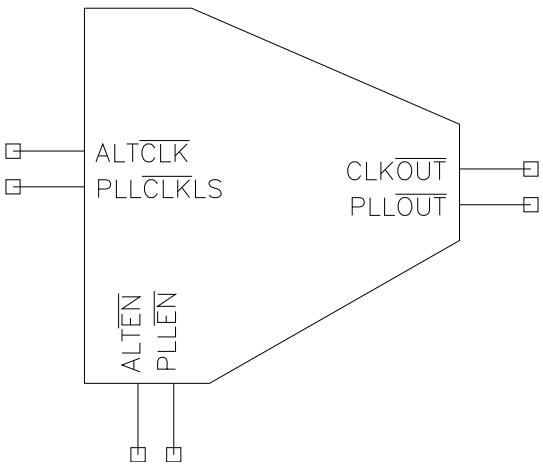
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	-4.023e-07	-2.290e-07	-8.213e-07	-1.389e-07
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	2.700e-08	-1.665e-07	-2.702e-07	-2.495e-07
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	-8.000e-08	-1.600e-07	-1.256e-06	-1.497e-06
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	2.180e-07	-3.150e-07	-1.016e-06	-4.878e-07
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	-3.400e-07	-5.340e-07	-1.441e-06	-1.037e-06
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	-9.700e-08	3.610e-07	-1.401e-06	-6.951e-07
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	2.100e-08	-3.310e-07	-1.794e-06	-2.208e-06
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	-8.250e-07	-1.149e-06	-1.010e-06	-2.707e-06
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	-1.738e-06	-1.492e-06	-2.765e-06	-2.550e-06

CNGFMUX21

Cell Description

2:1 Glitch-free MUX for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	2.400	2.856	6.8544
X15_P4	2.400	2.856	6.8544
X15_P10	2.400	2.856	6.8544
X15_P16	2.400	2.856	6.8544
X30_P0	2.400	3.944	9.4656
X30_P4	2.400	3.944	9.4656
X30_P10	2.400	3.944	9.4656
X30_P16	2.400	3.944	9.4656

Truth Table

PLL_CLK_LS	ALT_CLK	IPLL_EN_LD	IALT_EN_LD	CLK_OUT
0	-	-	0	0
0	0	-	-	0
-	0	0	-	0
PLL_CLK_LS	1	-	1	1
1	ALT_CLK	1	-	1
1	1	0	0	0

PLL_CLK_LS	PLL_OUT
PLL_CLK_LS	PLL_CLK_LS
1	1

PLL_EN	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

PLL_EN	0	-	PLL_EN
-	-	IPLL_EN_LD	IPLL_EN_LD
-	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

ALT_EN	ALT_CLK	IALT_EN_LD	IALT_EN_LD
ALT_EN	0	-	ALT_EN
-	-	IALT_EN_LD	IALT_EN_LD
-	ALT_CLK	IALT_EN_LD	IALT_EN_LD

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK	0.0023	0.0024	0.0026	0.0027
ALT_EN	0.0005	0.0006	0.0006	0.0006
PLL_CLK_LS	0.0030	0.0032	0.0033	0.0035
PLL_EN	0.0005	0.0005	0.0006	0.0006
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK	0.0037	0.0038	0.0040	0.0042
ALT_EN	0.0005	0.0006	0.0006	0.0006
PLL_CLK_LS	0.0050	0.0052	0.0056	0.0058
PLL_EN	0.0005	0.0005	0.0005	0.0006

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
ALT_CLK to CLK_OUT ↓	0.0367	0.0409	1.0905	1.1677
ALT_CLK to CLK_OUT ↑	0.0261	0.0290	1.7248	1.8933
PLL_CLK_LS to CLK_OUT ↓	0.0329	0.0367	1.0980	1.1775
PLL_CLK_LS to CLK_OUT ↑	0.0246	0.0274	1.7250	1.8964
PLL_CLK_LS to PLL_OUT ↓	0.0282	0.0318	0.9893	1.0590
PLL_CLK_LS to PLL_OUT ↑	0.0217	0.0242	1.4762	1.6182
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
ALT_CLK to CLK_OUT ↓	0.0474	0.0535	1.2866	1.3971
ALT_CLK to CLK_OUT ↑	0.0338	0.0383	2.1631	2.4309
PLL_CLK_LS to CLK_OUT ↓	0.0423	0.0476	1.2947	1.4052
PLL_CLK_LS to CLK_OUT ↑	0.0316	0.0355	2.1671	2.4358
PLL_CLK_LS to PLL_OUT ↓	0.0370	0.0418	1.1589	1.2538
PLL_CLK_LS to PLL_OUT ↑	0.0277	0.0309	1.8459	2.0713
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**

ALT_CLK to CLK_OUT ↓	0.0357	0.0398	0.5662	0.6066
ALT_CLK to CLK_OUT ↑	0.0265	0.0296	0.7751	0.8489
PLL_CLK_LS to CLK_OUT ↓	0.0324	0.0360	0.5737	0.6137
PLL_CLK_LS to CLK_OUT ↑	0.0255	0.0283	0.7794	0.8543
PLL_CLK_LS to PLL_OUT ↓	0.0246	0.0279	0.5070	0.5429
PLL_CLK_LS to PLL_OUT ↑	0.0190	0.0213	0.7423	0.8132
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
ALT_CLK to CLK_OUT ↓	0.0459	0.0513	0.6664	0.7233
ALT_CLK to CLK_OUT ↑	0.0344	0.0386	0.9678	1.0852
PLL_CLK_LS to CLK_OUT ↓	0.0413	0.0462	0.6742	0.7304
PLL_CLK_LS to CLK_OUT ↑	0.0324	0.0362	0.9730	1.0917
PLL_CLK_LS to PLL_OUT ↓	0.0320	0.0363	0.5953	0.6411
PLL_CLK_LS to PLL_OUT ↑	0.0242	0.0272	0.9267	1.0400

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0626	0.0684	0.0789	0.0895
ALT_EN ↓	hold_rising to ALT_CLK	-0.0269	-0.0343	-0.0407	-0.0508
ALT_EN ↑	hold_rising to ALT_CLK	-0.0042	-0.0068	-0.0090	-0.0139
ALT_EN ↓	setup_rising to ALT_CLK	0.0568	0.0638	0.0756	0.0906
ALT_EN ↑	setup_rising to ALT_CLK	0.0316	0.0365	0.0438	0.0487
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0626	0.0684	0.0789	0.0895
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0290	-0.0336	-0.0459	-0.0557
PLL_EN ↑	hold_rising to PLL_CLK_LS	-0.0042	-0.0068	-0.0090	-0.0139
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0568	0.0638	0.0756	0.0906
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0316	0.0368	0.0438	0.0512
		X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0626	0.0684	0.0789	0.0884
ALT_EN ↓	hold_rising to ALT_CLK	-0.0269	-0.0343	-0.0410	-0.0511

ALT_EN ↑	hold_rising to ALT_CLK	-0.0016	-0.0068	-0.0090	-0.0139
ALT_EN ↓	setup_rising to ALT_CLK	0.0568	0.0638	0.0756	0.0906
ALT_EN ↑	setup_rising to ALT_CLK	0.0365	0.0414	0.0487	0.0588
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0626	0.0684	0.0789	0.0884
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0290	-0.0392	-0.0486	-0.0609
PLL_EN ↑	hold_rising to PLL_CLK_LS	-0.0042	-0.0068	-0.0090	-0.0139
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0568	0.0638	0.0756	0.0875
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0365	0.0417	0.0487	0.0588

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X15_P0	4.217e-06	7.921e-12
X15_P4	1.389e-06	7.920e-12
X15_P10	8.374e-07	7.921e-12
X15_P16	8.117e-07	7.922e-12
X30_P0	6.742e-06	1.036e-11
X30_P4	2.186e-06	1.035e-11
X30_P10	1.353e-06	1.036e-11
X30_P16	1.327e-06	1.036e-11

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	3.399e-03	3.438e-03	3.547e-03	3.673e-03
ALT_EN (output stable)	2.257e-03	2.251e-03	2.297e-03	2.372e-03
PLL_CLK_LS (output stable)	6.450e-03	6.400e-03	6.537e-03	6.785e-03
PLL_EN (output stable)	2.279e-03	2.312e-03	2.397e-03	2.488e-03
ALT_CLK to CLK_OUT	6.990e-03	7.099e-03	7.400e-03	7.732e-03
PLL_CLK_LS to CLK_OUT	5.781e-03	5.812e-03	6.009e-03	6.248e-03
PLL_CLK_LS to PLL_OUT	6.579e-03	6.509e-03	6.674e-03	6.920e-03
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	4.321e-03	4.393e-03	4.548e-03	4.724e-03
ALT_EN (output stable)	2.560e-03	2.561e-03	2.621e-03	2.699e-03
PLL_CLK_LS (output stable)	9.754e-03	9.770e-03	9.957e-03	1.042e-02

PLL_EN (output stable)	2.668e-03	2.722e-03	2.854e-03	2.960e-03
ALT_CLK to CLK_OUT	1.267e-02	1.292e-02	1.350e-02	1.394e-02
PLL_CLK_LS to CLK_OUT	7.671e-03	7.732e-03	7.975e-03	8.288e-03
PLL_CLK_LS to PLL_OUT	8.559e-03	8.469e-03	8.614e-03	8.937e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

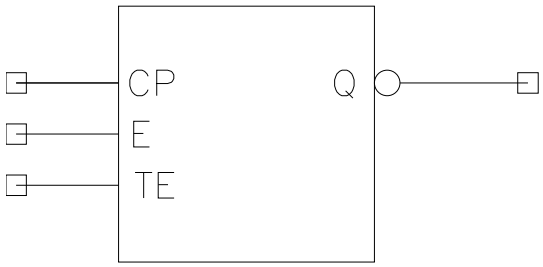
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	-9.617e-06	-1.105e-05	-1.059e-05	-9.397e-06
ALT_EN (output stable)	-3.848e-06	-7.199e-06	-7.046e-06	-7.391e-06
PLL_CLK_LS (output stable)	-8.380e-07	-2.161e-06	-3.386e-06	-5.159e-06
PLL_EN (output stable)	-3.899e-06	-7.481e-06	-7.711e-06	-7.277e-06
ALT_CLK to CLK_OUT	3.264e-05	1.939e-05	2.395e-05	1.541e-05
PLL_CLK_LS to CLK_OUT	3.325e-05	2.067e-05	1.570e-05	1.025e-05
PLL_CLK_LS to PLL_OUT	-2.238e-06	-4.902e-06	-5.424e-06	-6.134e-06
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	-2.816e-05	-2.834e-05	-2.525e-05	-2.641e-05
ALT_EN (output stable)	-3.092e-06	-7.198e-06	-8.090e-06	-7.469e-06
PLL_CLK_LS (output stable)	1.989e-05	1.429e-05	1.532e-05	1.204e-05
PLL_EN (output stable)	-3.944e-06	-7.512e-06	-7.738e-06	-7.277e-06
ALT_CLK to CLK_OUT	1.062e-04	1.037e-04	9.368e-05	9.056e-05
PLL_CLK_LS to CLK_OUT	6.906e-05	5.984e-05	5.160e-05	5.234e-05
PLL_CLK_LS to PLL_OUT	3.082e-05	2.754e-05	2.157e-05	1.808e-05

CNHLS

Cell Description

Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LRP_-CNHLSX7_P0	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX7_P4	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX7_P10	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX7_P16	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX15_P0	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX15_P4	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX15_P10	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX15_P16	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX22_P0	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX22_P4	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX22_P10	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX22_P16	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX29_P0	1.200	2.448	2.9376
C12T28SOI_LRP_-CNHLSX29_P4	1.200	2.448	2.9376
C12T28SOI_LRP_-CNHLSX29_P10	1.200	2.448	2.9376
C12T28SOI_LRP_-CNHLSX29_P16	1.200	2.448	2.9376

C12T28SOI_LRP_-CNHLSX36_P0	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX36_P4	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX36_P10	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX36_P16	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX51_P0	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX51_P4	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX51_P10	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX51_P16	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX58_P0	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX58_P4	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX58_P10	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX58_P16	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX71_P0	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX71_P4	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX71_P10	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX71_P16	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX93_P0	1.200	4.896	5.8752
C12T28SOI_LRP_-CNHLSX93_P4	1.200	4.896	5.8752
C12T28SOI_LRP_-CNHLSX93_P10	1.200	4.896	5.8752
C12T28SOI_LRP_-CNHLSX93_P16	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX29_P0	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX29_P4	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX29_P10	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX29_P16	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX36_P0	1.200	3.128	3.7536
C12T28SOI_LRPHP_-CNHLSX36_P4	1.200	3.128	3.7536

C12T28SOI_LRPHP_-CNHLSX36_P10	1.200	3.128	3.7536
C12T28SOI_LRPHP_-CNHLSX36_P16	1.200	3.128	3.7536
C12T28SOI_LRPHP_-CNHLSX44_P0	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX44_P4	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX44_P10	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX44_P16	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX51_P0	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX51_P4	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX51_P10	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX51_P16	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX58_P0	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX58_P4	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX58_P10	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX58_P16	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX71_P0	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX71_P4	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX71_P10	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX71_P16	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX86_P0	1.200	5.304	6.3648
C12T28SOI_LRPHP_-CNHLSX86_P4	1.200	5.304	6.3648
C12T28SOI_LRPHP_-CNHLSX86_P10	1.200	5.304	6.3648
C12T28SOI_LRPHP_-CNHLSX86_P16	1.200	5.304	6.3648

Truth Table

CP	E	TE	OLDIE	Q
0	-	-	-	0
1	-	-	OLDIE	OLDIE

OLDIE	OLDIE
OLDIE	OLDIE

Pin Capacitance

Pin	C12T28SOI_LRP_-CNHLSX7_P0	C12T28SOI_LRP_-CNHLSX7_P4	C12T28SOI_LRP_-CNHLSX7_P10	C12T28SOI_LRP_-CNHLSX7_P16
CP	0.0019	0.0020	0.0021	0.0022
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0010	0.0010	0.0011
	C12T28SOI_LRP_-CNHLSX15_P0	C12T28SOI_LRP_-CNHLSX15_P4	C12T28SOI_LRP_-CNHLSX15_P10	C12T28SOI_LRP_-CNHLSX15_P16
CP	0.0026	0.0026	0.0027	0.0029
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0010	0.0010	0.0011
	C12T28SOI_LRP_-CNHLSX22_P0	C12T28SOI_LRP_-CNHLSX22_P4	C12T28SOI_LRP_-CNHLSX22_P10	C12T28SOI_LRP_-CNHLSX22_P16
CP	0.0027	0.0028	0.0030	0.0032
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LRP_-CNHLSX29_P0	C12T28SOI_LRP_-CNHLSX29_P4	C12T28SOI_LRP_-CNHLSX29_P10	C12T28SOI_LRP_-CNHLSX29_P16
CP	0.0029	0.0030	0.0032	0.0034
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LRP_-CNHLSX36_P0	C12T28SOI_LRP_-CNHLSX36_P4	C12T28SOI_LRP_-CNHLSX36_P10	C12T28SOI_LRP_-CNHLSX36_P16
CP	0.0032	0.0033	0.0035	0.0038
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LRP_-CNHLSX51_P0	C12T28SOI_LRP_-CNHLSX51_P4	C12T28SOI_LRP_-CNHLSX51_P10	C12T28SOI_LRP_-CNHLSX51_P16
CP	0.0038	0.0039	0.0041	0.0044
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0010	0.0010	0.0011
	C12T28SOI_LRP_-CNHLSX58_P0	C12T28SOI_LRP_-CNHLSX58_P4	C12T28SOI_LRP_-CNHLSX58_P10	C12T28SOI_LRP_-CNHLSX58_P16
CP	0.0052	0.0054	0.0057	0.0061
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LRP_-CNHLSX71_P0	C12T28SOI_LRP_-CNHLSX71_P4	C12T28SOI_LRP_-CNHLSX71_P10	C12T28SOI_LRP_-CNHLSX71_P16
CP	0.0059	0.0062	0.0066	0.0070
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_LRP_-CNHLSX93_P0	C12T28SOI_LRP_-CNHLSX93_P4	C12T28SOI_LRP_-CNHLSX93_P10	C12T28SOI_LRP_-CNHLSX93_P16
CP	0.0070	0.0073	0.0078	0.0083
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0009	0.0010	0.0010
	C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP	0.0023	0.0024	0.0026	0.0027
E	0.0006	0.0006	0.0006	0.0007
TE	0.0009	0.0009	0.0009	0.0010

	C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP	0.0025	0.0027	0.0029	0.0030
E	0.0006	0.0006	0.0006	0.0007
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP	0.0030	0.0032	0.0034	0.0035
E	0.0006	0.0006	0.0006	0.0007
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP	0.0030	0.0031	0.0034	0.0035
E	0.0006	0.0006	0.0006	0.0007
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP	0.0041	0.0043	0.0047	0.0048
E	0.0006	0.0006	0.0006	0.0007
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP	0.0051	0.0053	0.0056	0.0060
E	0.0006	0.0006	0.0006	0.0007
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP	0.0062	0.0064	0.0068	0.0072
E	0.0006	0.0006	0.0006	0.0007
TE	0.0009	0.0009	0.0009	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LRP_-CNHLSX7_P0	**C12T28SOI_LRP_-CNHLSX7_P4**	**C12T28SOI_LRP_-CNHLSX7_P0**	**C12T28SOI_LRP_-CNHLSX7_P4**
CP to Q ↓	0.0334	0.0377	2.0750	2.2230
CP to Q ↑	0.0241	0.0270	2.9585	3.2382
	C12T28SOI_LRP_-CNHLSX7_P10	**C12T28SOI_LRP_-CNHLSX7_P16**	**C12T28SOI_LRP_-CNHLSX7_P10**	**C12T28SOI_LRP_-CNHLSX7_P16**
CP to Q ↓	0.0441	0.0500	2.4435	2.6440
CP to Q ↑	0.0312	0.0349	3.7007	4.1532
	C12T28SOI_LRP_-CNHLSX15_P0	**C12T28SOI_LRP_-CNHLSX15_P4**	**C12T28SOI_LRP_-CNHLSX15_P0**	**C12T28SOI_LRP_-CNHLSX15_P4**
CP to Q ↓	0.0289	0.0322	1.0427	1.1181
CP to Q ↑	0.0225	0.0249	1.4871	1.6301
	C12T28SOI_LRP_-CNHLSX15_P10	**C12T28SOI_LRP_-CNHLSX15_P16**	**C12T28SOI_LRP_-CNHLSX15_P10**	**C12T28SOI_LRP_-CNHLSX15_P16**

CP to Q ↓	0.0374	0.0419	1.2261	1.3254
CP to Q ↑	0.0288	0.0322	1.8584	2.0822
	C12T28SOI_LRP_-CNHLSX22_P0	**C12T28SOI_LRP_-CNHLSX22_P4**	**C12T28SOI_LRP_-CNHLSX22_P0**	**C12T28SOI_LRP_-CNHLSX22_P4**
CP to Q ↓	0.0294	0.0326	0.7242	0.7759
CP to Q ↑	0.0241	0.0267	1.0029	1.1000
	C12T28SOI_LRP_-CNHLSX22_P10	**C12T28SOI_LRP_-CNHLSX22_P16**	**C12T28SOI_LRP_-CNHLSX22_P10**	**C12T28SOI_LRP_-CNHLSX22_P16**
CP to Q ↓	0.0379	0.0426	0.8525	0.9209
CP to Q ↑	0.0310	0.0346	1.2539	1.4067
	C12T28SOI_LRP_-CNHLSX29_P0	**C12T28SOI_LRP_-CNHLSX29_P4**	**C12T28SOI_LRP_-CNHLSX29_P0**	**C12T28SOI_LRP_-CNHLSX29_P4**
CP to Q ↓	0.0289	0.0325	0.5424	0.5818
CP to Q ↑	0.0237	0.0264	0.7517	0.8249
	C12T28SOI_LRP_-CNHLSX29_P10	**C12T28SOI_LRP_-CNHLSX29_P16**	**C12T28SOI_LRP_-CNHLSX29_P10**	**C12T28SOI_LRP_-CNHLSX29_P16**
CP to Q ↓	0.0375	0.0425	0.6391	0.6913
CP to Q ↑	0.0303	0.0341	0.9401	1.0537
	C12T28SOI_LRP_-CNHLSX36_P0	**C12T28SOI_LRP_-CNHLSX36_P4**	**C12T28SOI_LRP_-CNHLSX36_P0**	**C12T28SOI_LRP_-CNHLSX36_P4**
CP to Q ↓	0.0285	0.0321	0.4336	0.4650
CP to Q ↑	0.0235	0.0262	0.6028	0.6608
	C12T28SOI_LRP_-CNHLSX36_P10	**C12T28SOI_LRP_-CNHLSX36_P16**	**C12T28SOI_LRP_-CNHLSX36_P10**	**C12T28SOI_LRP_-CNHLSX36_P16**
CP to Q ↓	0.0373	0.0422	0.5094	0.5521
CP to Q ↑	0.0301	0.0339	0.7529	0.8448
	C12T28SOI_LRP_-CNHLSX51_P0	**C12T28SOI_LRP_-CNHLSX51_P4**	**C12T28SOI_LRP_-CNHLSX51_P0**	**C12T28SOI_LRP_-CNHLSX51_P4**
CP to Q ↓	0.0311	0.0350	0.3174	0.3404
CP to Q ↑	0.0241	0.0271	0.4335	0.4752
	C12T28SOI_LRP_-CNHLSX51_P10	**C12T28SOI_LRP_-CNHLSX51_P16**	**C12T28SOI_LRP_-CNHLSX51_P10**	**C12T28SOI_LRP_-CNHLSX51_P16**
CP to Q ↓	0.0404	0.0456	0.3738	0.4043
CP to Q ↑	0.0311	0.0349	0.5411	0.6071
	C12T28SOI_LRP_-CNHLSX58_P0	**C12T28SOI_LRP_-CNHLSX58_P4**	**C12T28SOI_LRP_-CNHLSX58_P0**	**C12T28SOI_LRP_-CNHLSX58_P4**
CP to Q ↓	0.0278	0.0310	0.2789	0.2989
CP to Q ↑	0.0212	0.0236	0.3807	0.4170
	C12T28SOI_LRP_-CNHLSX58_P10	**C12T28SOI_LRP_-CNHLSX58_P16**	**C12T28SOI_LRP_-CNHLSX58_P10**	**C12T28SOI_LRP_-CNHLSX58_P16**
CP to Q ↓	0.0357	0.0404	0.3277	0.3541
CP to Q ↑	0.0270	0.0305	0.4757	0.5326
	C12T28SOI_LRP_-CNHLSX71_P0	**C12T28SOI_LRP_-CNHLSX71_P4**	**C12T28SOI_LRP_-CNHLSX71_P0**	**C12T28SOI_LRP_-CNHLSX71_P4**
CP to Q ↓	0.0271	0.0305	0.2314	0.2480
CP to Q ↑	0.0215	0.0241	0.3102	0.3400
	C12T28SOI_LRP_-CNHLSX71_P10	**C12T28SOI_LRP_-CNHLSX71_P16**	**C12T28SOI_LRP_-CNHLSX71_P10**	**C12T28SOI_LRP_-CNHLSX71_P16**
CP to Q ↓	0.0351	0.0395	0.2718	0.2939
CP to Q ↑	0.0277	0.0310	0.3869	0.4334
	C12T28SOI_LRP_-CNHLSX93_P0	**C12T28SOI_LRP_-CNHLSX93_P4**	**C12T28SOI_LRP_-CNHLSX93_P0**	**C12T28SOI_LRP_-CNHLSX93_P4**
CP to Q ↓	0.0282	0.0316	0.1837	0.1969

CP to Q ↑	0.0229	0.0256	0.2450	0.2685
	C12T28SOI_LRP_-CNHLSX93_P10	**C12T28SOI_LRP_-CNHLSX93_P16**	**C12T28SOI_LRP_-CNHLSX93_P10**	**C12T28SOI_LRP_-CNHLSX93_P16**
CP to Q ↓	0.0364	0.0411	0.2159	0.2332
CP to Q ↑	0.0293	0.0330	0.3053	0.3421
	C12T28SOI_-LRPHP_-CNHLSX29_P0	**C12T28SOI_-LRPHP_-CNHLSX29_P4**	**C12T28SOI_-LRPHP_-CNHLSX29_P0**	**C12T28SOI_-LRPHP_-CNHLSX29_P4**
CP to Q ↓	0.0276	0.0312	0.5512	0.5902
CP to Q ↑	0.0225	0.0253	0.7605	0.8314
	C12T28SOI_-LRPHP_-CNHLSX29_P10	**C12T28SOI_-LRPHP_-CNHLSX29_P16**	**C12T28SOI_-LRPHP_-CNHLSX29_P10**	**C12T28SOI_-LRPHP_-CNHLSX29_P16**
CP to Q ↓	0.0359	0.0406	0.6465	0.6999
CP to Q ↑	0.0288	0.0324	0.9457	1.0600
	C12T28SOI_-LRPHP_-CNHLSX36_P0	**C12T28SOI_-LRPHP_-CNHLSX36_P4**	**C12T28SOI_-LRPHP_-CNHLSX36_P0**	**C12T28SOI_-LRPHP_-CNHLSX36_P4**
CP to Q ↓	0.0271	0.0308	0.4400	0.4713
CP to Q ↑	0.0223	0.0251	0.6126	0.6697
	C12T28SOI_-LRPHP_-CNHLSX36_P10	**C12T28SOI_-LRPHP_-CNHLSX36_P16**	**C12T28SOI_-LRPHP_-CNHLSX36_P10**	**C12T28SOI_-LRPHP_-CNHLSX36_P16**
CP to Q ↓	0.0358	0.0403	0.5160	0.5580
CP to Q ↑	0.0288	0.0323	0.7617	0.8536
	C12T28SOI_-LRPHP_-CNHLSX44_P0	**C12T28SOI_-LRPHP_-CNHLSX44_P4**	**C12T28SOI_-LRPHP_-CNHLSX44_P0**	**C12T28SOI_-LRPHP_-CNHLSX44_P4**
CP to Q ↓	0.0279	0.0310	0.3691	0.3949
CP to Q ↑	0.0219	0.0241	0.5114	0.5585
	C12T28SOI_-LRPHP_-CNHLSX44_P10	**C12T28SOI_-LRPHP_-CNHLSX44_P16**	**C12T28SOI_-LRPHP_-CNHLSX44_P10**	**C12T28SOI_-LRPHP_-CNHLSX44_P16**
CP to Q ↓	0.0355	0.0400	0.4328	0.4669
CP to Q ↑	0.0275	0.0308	0.6352	0.7114
	C12T28SOI_-LRPHP_-CNHLSX51_P0	**C12T28SOI_-LRPHP_-CNHLSX51_P4**	**C12T28SOI_-LRPHP_-CNHLSX51_P0**	**C12T28SOI_-LRPHP_-CNHLSX51_P4**
CP to Q ↓	0.0295	0.0329	0.3198	0.3425
CP to Q ↑	0.0232	0.0257	0.4412	0.4824
	C12T28SOI_-LRPHP_-CNHLSX51_P10	**C12T28SOI_-LRPHP_-CNHLSX51_P16**	**C12T28SOI_-LRPHP_-CNHLSX51_P10**	**C12T28SOI_-LRPHP_-CNHLSX51_P16**
CP to Q ↓	0.0380	0.0428	0.3756	0.4055
CP to Q ↑	0.0294	0.0329	0.5476	0.6137
	C12T28SOI_-LRPHP_-CNHLSX58_P0	**C12T28SOI_-LRPHP_-CNHLSX58_P4**	**C12T28SOI_-LRPHP_-CNHLSX58_P0**	**C12T28SOI_-LRPHP_-CNHLSX58_P4**
CP to Q ↓	0.0262	0.0292	0.2780	0.2970
CP to Q ↑	0.0202	0.0224	0.3888	0.4248
	C12T28SOI_-LRPHP_-CNHLSX58_P10	**C12T28SOI_-LRPHP_-CNHLSX58_P16**	**C12T28SOI_-LRPHP_-CNHLSX58_P10**	**C12T28SOI_-LRPHP_-CNHLSX58_P16**

CP to Q ↓	0.0337	0.0380	0.3253	0.3517
CP to Q ↑	0.0256	0.0288	0.4826	0.5401
	C12T28SOI_-LRPHP_-CNHLSX71_P0	**C12T28SOI_-LRPHP_-CNHLSX71_P4**	**C12T28SOI_-LRPHP_-CNHLSX71_P0**	**C12T28SOI_-LRPHP_-CNHLSX71_P4**
CP to Q ↓	0.0259	0.0290	0.2321	0.2482
CP to Q ↑	0.0208	0.0232	0.3159	0.3454
	C12T28SOI_-LRPHP_-CNHLSX71_P10	**C12T28SOI_-LRPHP_-CNHLSX71_P16**	**C12T28SOI_-LRPHP_-CNHLSX71_P10**	**C12T28SOI_-LRPHP_-CNHLSX71_P16**
CP to Q ↓	0.0334	0.0379	0.2719	0.2937
CP to Q ↑	0.0264	0.0300	0.3925	0.4393
	C12T28SOI_-LRPHP_-CNHLSX86_P0	**C12T28SOI_-LRPHP_-CNHLSX86_P4**	**C12T28SOI_-LRPHP_-CNHLSX86_P0**	**C12T28SOI_-LRPHP_-CNHLSX86_P4**
CP to Q ↓	0.0254	0.0285	0.1964	0.2103
CP to Q ↑	0.0207	0.0232	0.2670	0.2915
	C12T28SOI_-LRPHP_-CNHLSX86_P10	**C12T28SOI_-LRPHP_-CNHLSX86_P16**	**C12T28SOI_-LRPHP_-CNHLSX86_P10**	**C12T28SOI_-LRPHP_-CNHLSX86_P16**
CP to Q ↓	0.0330	0.0371	0.2303	0.2486
CP to Q ↑	0.0267	0.0298	0.3308	0.3697

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	C12T28SOI_-LRP_CNHLSX7_-P0	C12T28SOI_-LRP_CNHLSX7_-P4	C12T28SOI_-LRP_CNHLSX7_-P10	C12T28SOI_-LRP_CNHLSX7_-P16
CP ↓	min_pulse_width to CP	0.0376	0.0429	0.0486	0.0557
E ↓	hold_rising to CP	-0.0150	-0.0196	-0.0267	-0.0309
E ↑	hold_rising to CP	0.0089	0.0036	0.0014	0.0014
E ↓	setup_rising to CP	0.0423	0.0463	0.0564	0.0608
E ↑	setup_rising to CP	0.0267	0.0288	0.0341	0.0389
TE ↓	hold_rising to CP	-0.0156	-0.0196	-0.0294	-0.0340
TE ↑	hold_rising to CP	0.0036	0.0036	0.0014	-0.0035
TE ↓	setup_rising to CP	0.0423	0.0468	0.0535	0.0639
TE ↑	setup_rising to CP	0.0267	0.0285	0.0393	0.0442
		C12T28SOI_-LRP_-CNHLSX15_P0	C12T28SOI_-LRP_-CNHLSX15_P4	C12T28SOI_-LRP_-CNHLSX15_P10	C12T28SOI_-LRP_-CNHLSX15_P16
CP ↓	min_pulse_width to CP	0.0365	0.0418	0.0475	0.0527
E ↓	hold_rising to CP	-0.0150	-0.0196	-0.0267	-0.0365
E ↑	hold_rising to CP	0.0033	0.0036	0.0014	0.0014
E ↓	setup_rising to CP	0.0423	0.0463	0.0564	0.0608
E ↑	setup_rising to CP	0.0268	0.0285	0.0338	0.0442
TE ↓	hold_rising to CP	-0.0177	-0.0196	-0.0294	-0.0365

TE ↑	hold_rising to CP	0.0036	0.0036	0.0014	-0.0035
TE ↓	setup_rising to CP	0.0423	0.0468	0.0535	0.0639
TE ↑	setup_rising to CP	0.0267	0.0316	0.0390	0.0442
		C12T28SOI_-LRP_-CNHLSX22_P0	C12T28SOI_-LRP_-CNHLSX22_P4	C12T28SOI_-LRP_-CNHLSX22_P10	C12T28SOI_-LRP_-CNHLSX22_P16
CP ↓	min_pulse_width to CP	0.0389	0.0442	0.0499	0.0576
E ↓	hold_rising to CP	-0.0171	-0.0245	-0.0316	-0.0414
E ↑	hold_rising to CP	0.0036	0.0036	0.0014	-0.0035
E ↓	setup_rising to CP	0.0441	0.0511	0.0612	0.0682
E ↑	setup_rising to CP	0.0264	0.0341	0.0390	0.0460
TE ↓	hold_rising to CP	-0.0174	-0.0245	-0.0343	-0.0414
TE ↑	hold_rising to CP	0.0036	0.0014	-0.0038	-0.0035
TE ↓	setup_rising to CP	0.0472	0.0517	0.0608	0.0687
TE ↑	setup_rising to CP	0.0316	0.0338	0.0442	0.0491
		C12T28SOI_-LRP_-CNHLSX29_P0	C12T28SOI_-LRP_-CNHLSX29_P4	C12T28SOI_-LRP_-CNHLSX29_P10	C12T28SOI_-LRP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0395	0.0442	0.0524	0.0581
E ↓	hold_rising to CP	-0.0196	-0.0245	-0.0309	-0.0414
E ↑	hold_rising to CP	0.0036	0.0036	0.0014	-0.0035
E ↓	setup_rising to CP	0.0471	0.0542	0.0608	0.0709
E ↑	setup_rising to CP	0.0316	0.0341	0.0387	0.0491
TE ↓	hold_rising to CP	-0.0223	-0.0241	-0.0343	-0.0410
TE ↑	hold_rising to CP	0.0036	0.0014	-0.0038	-0.0035
TE ↓	setup_rising to CP	0.0471	0.0538	0.0639	0.0705
TE ↑	setup_rising to CP	0.0316	0.0369	0.0442	0.0491
		C12T28SOI_-LRP_-CNHLSX36_P0	C12T28SOI_-LRP_-CNHLSX36_P4	C12T28SOI_-LRP_-CNHLSX36_P10	C12T28SOI_-LRP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0395	0.0442	0.0524	0.0600
E ↓	hold_rising to CP	-0.0196	-0.0245	-0.0340	-0.0414
E ↑	hold_rising to CP	0.0036	0.0036	0.0014	-0.0035
E ↓	setup_rising to CP	0.0471	0.0542	0.0608	0.0709
E ↑	setup_rising to CP	0.0286	0.0341	0.0390	0.0491
TE ↓	hold_rising to CP	-0.0223	-0.0272	-0.0340	-0.0410
TE ↑	hold_rising to CP	0.0036	0.0014	-0.0038	-0.0035

TE ↓	setup_rising to CP	0.0471	0.0538	0.0639	0.0705
TE ↑	setup_rising to CP	0.0316	0.0338	0.0442	0.0491
		C12T28SOI_-LRP_-CNHLSX51_P0	C12T28SOI_-LRP_-CNHLSX51_P4	C12T28SOI_-LRP_-CNHLSX51_P10	C12T28SOI_-LRP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0370	0.0423	0.0499	0.0576
E ↓	hold_rising to CP	-0.0174	-0.0245	-0.0291	-0.0362
E ↑	hold_rising to CP	0.0036	0.0036	0.0014	-0.0038
E ↓	setup_rising to CP	0.0445	0.0493	0.0560	0.0660
E ↑	setup_rising to CP	0.0289	0.0341	0.0387	0.0491
TE ↓	hold_rising to CP	-0.0174	-0.0220	-0.0287	-0.0388
TE ↑	hold_rising to CP	0.0036	0.0011	-0.0011	-0.0035
TE ↓	setup_rising to CP	0.0447	0.0520	0.0590	0.0657
TE ↑	setup_rising to CP	0.0316	0.0338	0.0442	0.0487
		C12T28SOI_-LRP_-CNHLSX58_P0	C12T28SOI_-LRP_-CNHLSX58_P4	C12T28SOI_-LRP_-CNHLSX58_P10	C12T28SOI_-LRP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0419	0.0472	0.0567	0.0619
E ↓	hold_rising to CP	-0.0223	-0.0294	-0.0365	-0.0462
E ↑	hold_rising to CP	0.0036	0.0011	0.0014	-0.0035
E ↓	setup_rising to CP	0.0493	0.0542	0.0664	0.0730
E ↑	setup_rising to CP	0.0316	0.0365	0.0438	0.0509
TE ↓	hold_rising to CP	-0.0223	-0.0294	-0.0392	-0.0462
TE ↑	hold_rising to CP	0.0036	0.0014	-0.0035	-0.0060
TE ↓	setup_rising to CP	0.0520	0.0569	0.0639	0.0761
TE ↑	setup_rising to CP	0.0341	0.0390	0.0435	0.0539
		C12T28SOI_-LRP_-CNHLSX71_P0	C12T28SOI_-LRP_-CNHLSX71_P4	C12T28SOI_-LRP_-CNHLSX71_P10	C12T28SOI_-LRP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0419	0.0472	0.0548	0.0644
E ↓	hold_rising to CP	-0.0223	-0.0294	-0.0365	-0.0462
E ↑	hold_rising to CP	0.0036	0.0011	0.0014	-0.0035
E ↓	setup_rising to CP	0.0493	0.0542	0.0664	0.0761
E ↑	setup_rising to CP	0.0316	0.0365	0.0435	0.0540
TE ↓	hold_rising to CP	-0.0223	-0.0294	-0.0392	-0.0489
TE ↑	hold_rising to CP	0.0036	0.0014	-0.0035	-0.0060
TE ↓	setup_rising to CP	0.0520	0.0569	0.0660	0.0761

TE ↑	setup_rising to CP	0.0334	0.0390	0.0491	0.0558
		C12T28SOI_-LRP_-CNHLSX93_P0	C12T28SOI_-LRP_-CNHLSX93_P4	C12T28SOI_-LRP_-CNHLSX93_P10	C12T28SOI_-LRP_-CNHLSX93_P16
CP ↓	min_pulse_width to CP	0.0419	0.0472	0.0591	0.0668
E ↓	hold_rising to CP	-0.0245	-0.0294	-0.0388	-0.0459
E ↑	hold_rising to CP	0.0036	0.0011	0.0014	-0.0035
E ↓	setup_rising to CP	0.0489	0.0591	0.0661	0.0758
E ↑	setup_rising to CP	0.0365	0.0414	0.0487	0.0589
TE ↓	hold_rising to CP	-0.0245	-0.0321	-0.0388	-0.0486
TE ↑	hold_rising to CP	0.0036	0.0014	-0.0035	-0.0060
TE ↓	setup_rising to CP	0.0520	0.0591	0.0688	0.0788
TE ↑	setup_rising to CP	0.0365	0.0413	0.0484	0.0584
		C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0456	0.0514	0.0653	0.0729
E ↓	hold_rising to CP	-0.0042	-0.0064	-0.0142	-0.0191
E ↑	hold_rising to CP	0.0273	0.0273	0.0266	0.0318
E ↓	setup_rising to CP	0.0392	0.0410	0.0511	0.0585
E ↑	setup_rising to CP	0.0219	0.0268	0.0316	0.0390
TE ↓	hold_rising to CP	-0.0042	-0.0095	-0.0113	-0.0187
TE ↑	hold_rising to CP	0.0273	0.0273	0.0269	0.0293
TE ↓	setup_rising to CP	0.0389	0.0441	0.0507	0.0581
TE ↑	setup_rising to CP	0.0219	0.0268	0.0341	0.0390
		C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0456	0.0514	0.0646	0.0748
E ↓	hold_rising to CP	-0.0042	-0.0064	-0.0138	-0.0191
E ↑	hold_rising to CP	0.0273	0.0273	0.0266	0.0318
E ↓	setup_rising to CP	0.0389	0.0441	0.0511	0.0585
E ↑	setup_rising to CP	0.0219	0.0268	0.0316	0.0394
TE ↓	hold_rising to CP	-0.0042	-0.0095	-0.0138	-0.0187
TE ↑	hold_rising to CP	0.0273	0.0273	0.0269	0.0293
TE ↓	setup_rising to CP	0.0389	0.0441	0.0507	0.0611
TE ↑	setup_rising to CP	0.0219	0.0268	0.0341	0.0390

		C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP ↓	min_pulse_width to CP	0.0462	0.0533	0.0653	0.0748
E ↓	hold_rising to CP	-0.0042	-0.0064	-0.0138	-0.0188
E ↑	hold_rising to CP	0.0273	0.0273	0.0266	0.0318
E ↓	setup_rising to CP	0.0389	0.0463	0.0532	0.0581
E ↑	setup_rising to CP	0.0250	0.0268	0.0341	0.0390
TE ↓	hold_rising to CP	-0.0042	-0.0095	-0.0169	-0.0187
TE ↑	hold_rising to CP	0.0243	0.0273	0.0269	0.0293
TE ↓	setup_rising to CP	0.0389	0.0462	0.0507	0.0611
TE ↑	setup_rising to CP	0.0271	0.0293	0.0341	0.0442
		C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0467	0.0533	0.0653	0.0748
E ↓	hold_rising to CP	-0.0042	-0.0064	-0.0135	-0.0188
E ↑	hold_rising to CP	0.0273	0.0273	0.0266	0.0318
E ↓	setup_rising to CP	0.0389	0.0441	0.0511	0.0585
E ↑	setup_rising to CP	0.0250	0.0268	0.0341	0.0390
TE ↓	hold_rising to CP	-0.0042	-0.0095	-0.0169	-0.0184
TE ↑	hold_rising to CP	0.0243	0.0273	0.0269	0.0293
TE ↓	setup_rising to CP	0.0389	0.0437	0.0507	0.0611
TE ↑	setup_rising to CP	0.0275	0.0293	0.0341	0.0442
		C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0480	0.0557	0.0653	0.0797
E ↓	hold_rising to CP	-0.0042	-0.0120	-0.0135	-0.0184
E ↑	hold_rising to CP	0.0273	0.0273	0.0266	0.0318
E ↓	setup_rising to CP	0.0411	0.0459	0.0560	0.0630
E ↑	setup_rising to CP	0.0246	0.0268	0.0341	0.0417
TE ↓	hold_rising to CP	-0.0042	-0.0091	-0.0166	-0.0215
TE ↑	hold_rising to CP	0.0243	0.0273	0.0269	0.0293
TE ↓	setup_rising to CP	0.0438	0.0490	0.0556	0.0660
TE ↑	setup_rising to CP	0.0271	0.0293	0.0369	0.0442

		C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0510	0.0595	0.0701	0.0845
E ↓	hold_rising to CP	-0.0094	-0.0113	-0.0184	-0.0237
E ↑	hold_rising to CP	0.0243	0.0273	0.0269	0.0297
E ↓	setup_rising to CP	0.0459	0.0508	0.0609	0.0678
E ↑	setup_rising to CP	0.0268	0.0316	0.0390	0.0439
TE ↓	hold_rising to CP	-0.0091	-0.0143	-0.0217	-0.0263
TE ↑	hold_rising to CP	0.0217	0.0248	0.0269	0.0300
TE ↓	setup_rising to CP	0.0434	0.0508	0.0605	0.0709
TE ↑	setup_rising to CP	0.0268	0.0316	0.0390	0.0491
		C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP ↓	min_pulse_width to CP	0.0510	0.0600	0.0701	0.0845
E ↓	hold_rising to CP	-0.0064	-0.0117	-0.0166	-0.0240
E ↑	hold_rising to CP	0.0273	0.0273	0.0266	0.0293
E ↓	setup_rising to CP	0.0437	0.0512	0.0581	0.0682
E ↑	setup_rising to CP	0.0268	0.0317	0.0390	0.0466
TE ↓	hold_rising to CP	-0.0072	-0.0116	-0.0162	-0.0240
TE ↑	hold_rising to CP	0.0243	0.0273	0.0269	0.0300
TE ↓	setup_rising to CP	0.0437	0.0511	0.0612	0.0678
TE ↑	setup_rising to CP	0.0268	0.0316	0.0387	0.0491

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LRP_CNHLSX7_P0	1.456e-06	4.040e-12
C12T28SOI_LRP_CNHLSX7_P4	4.537e-07	4.043e-12
C12T28SOI_LRP_CNHLSX7_P10	2.598e-07	4.040e-12
C12T28SOI_LRP_CNHLSX7_P16	2.474e-07	4.040e-12
C12T28SOI_LRP_CNHLSX15_P0	1.887e-06	4.292e-12
C12T28SOI_LRP_CNHLSX15_P4	5.739e-07	4.295e-12
C12T28SOI_LRP_CNHLSX15_P10	3.323e-07	4.291e-12
C12T28SOI_LRP_CNHLSX15_P16	3.189e-07	4.293e-12
C12T28SOI_LRP_CNHLSX22_P0	2.229e-06	5.048e-12
C12T28SOI_LRP_CNHLSX22_P4	6.596e-07	5.050e-12
C12T28SOI_LRP_CNHLSX22_P10	3.863e-07	5.047e-12
C12T28SOI_LRP_CNHLSX22_P16	3.736e-07	5.048e-12
C12T28SOI_LRP_CNHLSX29_P0	2.509e-06	5.300e-12
C12T28SOI_LRP_CNHLSX29_P4	7.459e-07	5.303e-12
C12T28SOI_LRP_CNHLSX29_P10	4.406e-07	5.300e-12
C12T28SOI_LRP_CNHLSX29_P16	4.278e-07	5.300e-12

C12T28SOI_LRP_CNHLSX36_P0	2.834e-06	5.551e-12
C12T28SOI_LRP_CNHLSX36_P4	8.399e-07	5.554e-12
C12T28SOI_LRP_CNHLSX36_P10	4.989e-07	5.551e-12
C12T28SOI_LRP_CNHLSX36_P16	4.860e-07	5.551e-12
C12T28SOI_LRP_CNHLSX51_P0	3.474e-06	6.560e-12
C12T28SOI_LRP_CNHLSX51_P4	1.037e-06	6.561e-12
C12T28SOI_LRP_CNHLSX51_P10	6.193e-07	6.559e-12
C12T28SOI_LRP_CNHLSX51_P16	6.046e-07	6.561e-12
C12T28SOI_LRP_CNHLSX58_P0	4.216e-06	8.773e-12
C12T28SOI_LRP_CNHLSX58_P4	1.265e-06	8.777e-12
C12T28SOI_LRP_CNHLSX58_P10	7.488e-07	8.771e-12
C12T28SOI_LRP_CNHLSX58_P16	7.292e-07	8.774e-12
C12T28SOI_LRP_CNHLSX71_P0	4.957e-06	9.785e-12
C12T28SOI_LRP_CNHLSX71_P4	1.490e-06	9.788e-12
C12T28SOI_LRP_CNHLSX71_P10	8.843e-07	9.785e-12
C12T28SOI_LRP_CNHLSX71_P16	8.617e-07	9.787e-12
C12T28SOI_LRP_CNHLSX93_P0	5.934e-06	1.079e-11
C12T28SOI_LRP_CNHLSX93_P4	1.771e-06	1.079e-11
C12T28SOI_LRP_CNHLSX93_P10	1.061e-06	1.080e-11
C12T28SOI_LRP_CNHLSX93_P16	1.039e-06	1.079e-11
C12T28SOI_LRPHP_CNHLSX29_P0	2.993e-06	6.308e-12
C12T28SOI_LRPHP_CNHLSX29_P4	8.918e-07	6.308e-12
C12T28SOI_LRPHP_CNHLSX29_P10	5.105e-07	6.308e-12
C12T28SOI_LRPHP_CNHLSX29_P16	4.889e-07	6.308e-12
C12T28SOI_LRPHP_CNHLSX36_P0	3.314e-06	6.560e-12
C12T28SOI_LRPHP_CNHLSX36_P4	9.858e-07	6.560e-12
C12T28SOI_LRPHP_CNHLSX36_P10	5.691e-07	6.561e-12
C12T28SOI_LRPHP_CNHLSX36_P16	5.474e-07	6.560e-12
C12T28SOI_LRPHP_CNHLSX44_P0	3.703e-06	7.316e-12
C12T28SOI_LRPHP_CNHLSX44_P4	1.111e-06	7.316e-12
C12T28SOI_LRPHP_CNHLSX44_P10	6.486e-07	7.317e-12
C12T28SOI_LRPHP_CNHLSX44_P16	6.268e-07	7.316e-12
C12T28SOI_LRPHP_CNHLSX51_P0	3.949e-06	7.568e-12
C12T28SOI_LRPHP_CNHLSX51_P4	1.176e-06	7.568e-12
C12T28SOI_LRPHP_CNHLSX51_P10	6.875e-07	7.569e-12
C12T28SOI_LRPHP_CNHLSX51_P16	6.654e-07	7.568e-12
C12T28SOI_LRPHP_CNHLSX58_P0	4.660e-06	9.783e-12
C12T28SOI_LRPHP_CNHLSX58_P4	1.400e-06	9.782e-12
C12T28SOI_LRPHP_CNHLSX58_P10	8.153e-07	9.782e-12
C12T28SOI_LRPHP_CNHLSX58_P16	7.881e-07	9.782e-12
C12T28SOI_LRPHP_CNHLSX71_P0	5.486e-06	1.064e-11
C12T28SOI_LRPHP_CNHLSX71_P4	1.633e-06	1.064e-11
C12T28SOI_LRPHP_CNHLSX71_P10	9.530e-07	1.064e-11
C12T28SOI_LRPHP_CNHLSX71_P16	9.226e-07	1.064e-11
C12T28SOI_LRPHP_CNHLSX86_P0	6.142e-06	1.155e-11
C12T28SOI_LRPHP_CNHLSX86_P4	1.842e-06	1.155e-11
C12T28SOI_LRPHP_CNHLSX86_P10	1.089e-06	1.155e-11
C12T28SOI_LRPHP_CNHLSX86_P16	1.059e-06	1.155e-11

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LRP_-CNHLSX7_P0	C12T28SOI_LRP_-CNHLSX7_P4	C12T28SOI_LRP_-CNHLSX7_P10	C12T28SOI_LRP_-CNHLSX7_P16

CP (output stable)	2.268e-03	2.301e-03	2.385e-03	2.474e-03
E (output stable)	1.107e-03	1.096e-03	1.115e-03	1.142e-03
TE (output stable)	1.292e-03	1.313e-03	1.344e-03	1.377e-03
CP to Q	3.041e-03	3.048e-03	3.140e-03	3.251e-03
	C12T28SOI_LRP_-CNHLSX15_P0	C12T28SOI_LRP_-CNHLSX15_P4	C12T28SOI_LRP_-CNHLSX15_P10	C12T28SOI_LRP_-CNHLSX15_P16
CP (output stable)	2.641e-03	2.688e-03	2.784e-03	2.892e-03
E (output stable)	1.144e-03	1.136e-03	1.158e-03	1.190e-03
TE (output stable)	1.330e-03	1.352e-03	1.387e-03	1.424e-03
CP to Q	4.440e-03	4.427e-03	4.590e-03	4.742e-03
	C12T28SOI_LRP_-CNHLSX22_P0	C12T28SOI_LRP_-CNHLSX22_P4	C12T28SOI_LRP_-CNHLSX22_P10	C12T28SOI_LRP_-CNHLSX22_P16
CP (output stable)	2.977e-03	3.031e-03	3.131e-03	3.262e-03
E (output stable)	1.237e-03	1.230e-03	1.255e-03	1.289e-03
TE (output stable)	1.423e-03	1.447e-03	1.484e-03	1.522e-03
CP to Q	5.758e-03	5.700e-03	5.913e-03	6.113e-03
	C12T28SOI_LRP_-CNHLSX29_P0	C12T28SOI_LRP_-CNHLSX29_P4	C12T28SOI_LRP_-CNHLSX29_P10	C12T28SOI_LRP_-CNHLSX29_P16
CP (output stable)	3.111e-03	3.168e-03	3.301e-03	3.433e-03
E (output stable)	1.263e-03	1.256e-03	1.280e-03	1.313e-03
TE (output stable)	1.449e-03	1.473e-03	1.509e-03	1.547e-03
CP to Q	6.954e-03	6.941e-03	7.102e-03	7.445e-03
	C12T28SOI_LRP_-CNHLSX36_P0	C12T28SOI_LRP_-CNHLSX36_P4	C12T28SOI_LRP_-CNHLSX36_P10	C12T28SOI_LRP_-CNHLSX36_P16
CP (output stable)	3.331e-03	3.386e-03	3.522e-03	3.673e-03
E (output stable)	1.265e-03	1.258e-03	1.284e-03	1.319e-03
TE (output stable)	1.451e-03	1.475e-03	1.512e-03	1.553e-03
CP to Q	8.114e-03	8.109e-03	8.370e-03	8.730e-03
	C12T28SOI_LRP_-CNHLSX51_P0	C12T28SOI_LRP_-CNHLSX51_P4	C12T28SOI_LRP_-CNHLSX51_P10	C12T28SOI_LRP_-CNHLSX51_P16
CP (output stable)	3.668e-03	3.713e-03	3.853e-03	4.031e-03
E (output stable)	1.278e-03	1.273e-03	1.300e-03	1.338e-03
TE (output stable)	1.464e-03	1.490e-03	1.529e-03	1.571e-03
CP to Q	1.080e-02	1.088e-02	1.120e-02	1.167e-02
	C12T28SOI_LRP_-CNHLSX58_P0	C12T28SOI_LRP_-CNHLSX58_P4	C12T28SOI_LRP_-CNHLSX58_P10	C12T28SOI_LRP_-CNHLSX58_P16
CP (output stable)	4.766e-03	4.811e-03	4.996e-03	5.220e-03
E (output stable)	1.422e-03	1.417e-03	1.449e-03	1.492e-03
TE (output stable)	1.606e-03	1.632e-03	1.675e-03	1.723e-03
CP to Q	1.243e-02	1.235e-02	1.271e-02	1.328e-02
	C12T28SOI_LRP_-CNHLSX71_P0	C12T28SOI_LRP_-CNHLSX71_P4	C12T28SOI_LRP_-CNHLSX71_P10	C12T28SOI_LRP_-CNHLSX71_P16
CP (output stable)	5.370e-03	5.457e-03	5.639e-03	5.920e-03
E (output stable)	1.473e-03	1.471e-03	1.506e-03	1.553e-03
TE (output stable)	1.656e-03	1.685e-03	1.732e-03	1.784e-03
CP to Q	1.509e-02	1.523e-02	1.568e-02	1.631e-02
	C12T28SOI_LRP_-CNHLSX93_P0	C12T28SOI_LRP_-CNHLSX93_P4	C12T28SOI_LRP_-CNHLSX93_P10	C12T28SOI_LRP_-CNHLSX93_P16
CP (output stable)	6.114e-03	6.218e-03	6.453e-03	6.785e-03
E (output stable)	1.592e-03	1.592e-03	1.631e-03	1.682e-03
TE (output stable)	1.778e-03	1.808e-03	1.860e-03	1.916e-03
CP to Q	1.951e-02	1.952e-02	1.996e-02	2.087e-02

	C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP (output stable)	4.418e-03	4.516e-03	4.701e-03	4.888e-03
E (output stable)	1.169e-03	1.156e-03	1.175e-03	1.204e-03
TE (output stable)	1.354e-03	1.374e-03	1.405e-03	1.441e-03
CP to Q	8.744e-03	8.833e-03	9.042e-03	9.410e-03
	C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP (output stable)	4.615e-03	4.714e-03	4.921e-03	5.131e-03
E (output stable)	1.176e-03	1.165e-03	1.185e-03	1.215e-03
TE (output stable)	1.361e-03	1.382e-03	1.415e-03	1.452e-03
CP to Q	9.819e-03	9.940e-03	1.025e-02	1.062e-02
	C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP (output stable)	4.952e-03	5.072e-03	5.269e-03	5.507e-03
E (output stable)	1.222e-03	1.212e-03	1.234e-03	1.268e-03
TE (output stable)	1.407e-03	1.429e-03	1.465e-03	1.504e-03
CP to Q	1.131e-02	1.125e-02	1.147e-02	1.192e-02
	C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP (output stable)	4.992e-03	5.066e-03	5.282e-03	5.508e-03
E (output stable)	1.222e-03	1.212e-03	1.234e-03	1.268e-03
TE (output stable)	1.407e-03	1.429e-03	1.465e-03	1.505e-03
CP to Q	1.234e-02	1.232e-02	1.262e-02	1.312e-02
	C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP (output stable)	5.805e-03	5.882e-03	6.175e-03	6.417e-03
E (output stable)	1.291e-03	1.281e-03	1.306e-03	1.343e-03
TE (output stable)	1.476e-03	1.499e-03	1.537e-03	1.580e-03
CP to Q	1.354e-02	1.352e-02	1.386e-02	1.451e-02
	C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP (output stable)	6.487e-03	6.603e-03	6.873e-03	7.237e-03
E (output stable)	1.401e-03	1.393e-03	1.421e-03	1.461e-03
TE (output stable)	1.586e-03	1.610e-03	1.651e-03	1.697e-03
CP to Q	1.624e-02	1.630e-02	1.664e-02	1.754e-02
	C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP (output stable)	7.102e-03	7.179e-03	7.468e-03	7.871e-03
E (output stable)	1.434e-03	1.429e-03	1.460e-03	1.512e-03
TE (output stable)	1.619e-03	1.647e-03	1.691e-03	1.748e-03
CP to Q	1.861e-02	1.876e-02	1.941e-02	2.014e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LRP_-CNHLSX7_P0	C12T28SOI_LRP_-CNHLSX7_P4	C12T28SOI_LRP_-CNHLSX7_P10	C12T28SOI_LRP_-CNHLSX7_P16
CP (output stable)	-3.045e-05	-2.795e-05	-2.153e-05	-1.878e-05
E (output stable)	1.172e-05	1.232e-06	-5.478e-08	-2.220e-07
TE (output stable)	-3.706e-06	-8.472e-06	-9.084e-06	-8.542e-06
CP to Q	1.242e-05	1.139e-05	1.157e-05	1.173e-05
	C12T28SOI_LRP_-CNHLSX15_P0	C12T28SOI_LRP_-CNHLSX15_P4	C12T28SOI_LRP_-CNHLSX15_P10	C12T28SOI_LRP_-CNHLSX15_P16
CP (output stable)	-2.218e-05	-1.895e-05	-1.455e-05	-1.079e-05
E (output stable)	1.169e-05	1.237e-06	-6.710e-08	-3.041e-07
TE (output stable)	-3.755e-06	-8.509e-06	-9.104e-06	-8.551e-06
CP to Q	4.584e-06	2.434e-06	2.314e-06	1.854e-06
	C12T28SOI_LRP_-CNHLSX22_P0	C12T28SOI_LRP_-CNHLSX22_P4	C12T28SOI_LRP_-CNHLSX22_P10	C12T28SOI_LRP_-CNHLSX22_P16
CP (output stable)	-1.434e-06	6.189e-07	4.716e-06	9.138e-06
E (output stable)	1.168e-05	1.242e-06	-7.860e-08	-2.447e-07
TE (output stable)	-3.782e-06	-8.502e-06	-9.101e-06	-8.565e-06
CP to Q	1.735e-05	1.709e-05	1.540e-05	1.596e-05
	C12T28SOI_LRP_-CNHLSX29_P0	C12T28SOI_LRP_-CNHLSX29_P4	C12T28SOI_LRP_-CNHLSX29_P10	C12T28SOI_LRP_-CNHLSX29_P16
CP (output stable)	-1.843e-05	-1.640e-05	-1.007e-05	-4.350e-06
E (output stable)	1.165e-05	1.194e-06	-7.458e-08	-2.451e-07
TE (output stable)	-3.711e-06	-8.485e-06	-9.095e-06	-8.567e-06
CP to Q	9.979e-06	1.003e-05	8.432e-06	7.426e-06
	C12T28SOI_LRP_-CNHLSX36_P0	C12T28SOI_LRP_-CNHLSX36_P4	C12T28SOI_LRP_-CNHLSX36_P10	C12T28SOI_LRP_-CNHLSX36_P16
CP (output stable)	-6.676e-06	-4.115e-06	1.652e-06	7.665e-06
E (output stable)	1.165e-05	1.182e-06	-7.212e-08	-2.436e-07
TE (output stable)	-3.724e-06	-8.502e-06	-9.111e-06	-8.573e-06
CP to Q	3.001e-05	2.802e-05	2.534e-05	2.422e-05
	C12T28SOI_LRP_-CNHLSX51_P0	C12T28SOI_LRP_-CNHLSX51_P4	C12T28SOI_LRP_-CNHLSX51_P10	C12T28SOI_LRP_-CNHLSX51_P16
CP (output stable)	-1.486e-05	-1.151e-05	-4.834e-06	1.975e-06
E (output stable)	1.167e-05	1.220e-06	-6.677e-08	-2.360e-07
TE (output stable)	-3.762e-06	-8.511e-06	-9.116e-06	-8.562e-06
CP to Q	4.002e-05	3.547e-05	3.244e-05	2.743e-05
	C12T28SOI_LRP_-CNHLSX58_P0	C12T28SOI_LRP_-CNHLSX58_P4	C12T28SOI_LRP_-CNHLSX58_P10	C12T28SOI_LRP_-CNHLSX58_P16
CP (output stable)	-4.914e-05	-4.521e-05	-3.647e-05	-3.047e-05
E (output stable)	1.146e-05	1.182e-06	-6.340e-08	-2.257e-07
TE (output stable)	-3.746e-06	-8.405e-06	-8.890e-06	-8.422e-06
CP to Q	3.981e-05	3.766e-05	2.869e-05	2.939e-05
	C12T28SOI_LRP_-CNHLSX71_P0	C12T28SOI_LRP_-CNHLSX71_P4	C12T28SOI_LRP_-CNHLSX71_P10	C12T28SOI_LRP_-CNHLSX71_P16
CP (output stable)	-3.451e-05	-3.063e-05	-2.134e-05	-1.148e-05
E (output stable)	1.153e-05	1.300e-06	5.132e-08	-1.077e-07
TE (output stable)	-3.643e-06	-8.295e-06	-8.795e-06	-8.322e-06
CP to Q	3.649e-05	3.491e-05	2.632e-05	2.242e-05
	C12T28SOI_LRP_-CNHLSX93_P0	C12T28SOI_LRP_-CNHLSX93_P4	C12T28SOI_LRP_-CNHLSX93_P10	C12T28SOI_LRP_-CNHLSX93_P16
CP (output stable)	-3.961e-05	-3.410e-05	-2.215e-05	-1.311e-05
E (output stable)	1.172e-05	1.290e-06	5.915e-08	-1.081e-07
TE (output stable)	-3.663e-06	-8.363e-06	-8.963e-06	-8.418e-06

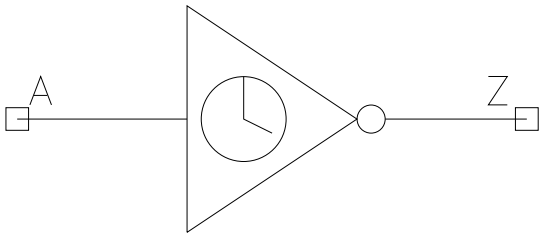
CP to Q	6.714e-05	6.128e-05	5.559e-05	4.753e-05
	C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP (output stable)	-2.983e-05	-2.562e-05	-1.966e-05	-1.369e-05
E (output stable)	1.187e-05	1.186e-06	-1.254e-07	-3.845e-08
TE (output stable)	-3.567e-06	-8.574e-06	-9.199e-06	-8.479e-06
CP to Q	1.820e-05	1.643e-05	1.309e-05	1.147e-05
	C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP (output stable)	-1.905e-05	-1.507e-05	-8.508e-06	4.891e-07
E (output stable)	1.185e-05	1.161e-06	-1.569e-07	-4.633e-08
TE (output stable)	-3.593e-06	-8.593e-06	-9.240e-06	-8.484e-06
CP to Q	2.801e-05	2.410e-05	2.405e-05	1.984e-05
	C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP (output stable)	-3.066e-05	-2.575e-05	-1.567e-05	-7.269e-06
E (output stable)	1.184e-05	1.162e-06	-1.623e-07	-6.855e-08
TE (output stable)	-3.576e-06	-8.585e-06	-9.237e-06	-8.505e-06
CP to Q	2.739e-05	2.529e-05	2.007e-05	1.822e-05
	C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP (output stable)	-2.944e-05	-2.555e-05	-1.543e-05	-8.655e-06
E (output stable)	1.184e-05	1.162e-06	-1.626e-07	-6.945e-08
TE (output stable)	-3.568e-06	-8.566e-06	-9.235e-06	-8.503e-06
CP to Q	3.727e-05	3.579e-05	2.770e-05	2.835e-05
	C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP (output stable)	-5.278e-05	-4.718e-05	-4.388e-05	-3.052e-05
E (output stable)	1.182e-05	1.159e-06	-1.563e-07	-6.057e-08
TE (output stable)	-3.570e-06	-8.550e-06	-9.231e-06	-8.500e-06
CP to Q	4.127e-05	3.829e-05	2.936e-05	2.712e-05
	C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP (output stable)	-4.392e-05	-3.350e-05	-3.325e-05	-1.372e-05
E (output stable)	1.188e-05	1.248e-06	-1.580e-07	4.997e-08
TE (output stable)	-3.522e-06	-8.466e-06	-9.230e-06	-8.370e-06
CP to Q	3.990e-05	3.774e-05	3.072e-05	2.642e-05
	C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP (output stable)	-5.011e-05	-3.304e-05	-8.924e-06	-1.848e-05
E (output stable)	1.181e-05	1.292e-06	-1.631e-07	6.844e-08
TE (output stable)	-3.582e-06	-8.442e-06	-9.236e-06	-8.336e-06
CP to Q	4.690e-05	4.334e-05	2.373e-05	2.411e-05

CNIV

Cell Description

Inverter with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.272	0.3264
X5_P4	1.200	0.272	0.3264
X5_P10	1.200	0.272	0.3264
X5_P16	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X16_P0	1.200	0.408	0.4896
X16_P4	1.200	0.408	0.4896
X16_P10	1.200	0.408	0.4896
X16_P16	1.200	0.408	0.4896
X23_P0	1.200	0.544	0.6528
X23_P4	1.200	0.544	0.6528
X23_P10	1.200	0.544	0.6528
X23_P16	1.200	0.544	0.6528
X31_P0	1.200	0.680	0.8160
X31_P4	1.200	0.680	0.8160
X31_P10	1.200	0.680	0.8160
X31_P16	1.200	0.680	0.8160
X39_P0	1.200	0.816	0.9792
X39_P4	1.200	0.816	0.9792
X39_P10	1.200	0.816	0.9792
X39_P16	1.200	0.816	0.9792
X47_P0	1.200	0.952	1.1424
X47_P4	1.200	0.952	1.1424
X47_P10	1.200	0.952	1.1424
X47_P16	1.200	0.952	1.1424
X55_P0	1.200	1.088	1.3056
X55_P4	1.200	1.088	1.3056
X55_P10	1.200	1.088	1.3056
X55_P16	1.200	1.088	1.3056
X61_P0	1.200	1.224	1.4688

X61_P4	1.200	1.224	1.4688
X61_P10	1.200	1.224	1.4688
X61_P16	1.200	1.224	1.4688
X70_P0	1.200	1.360	1.6320
X70_P4	1.200	1.360	1.6320
X70_P10	1.200	1.360	1.6320
X70_P16	1.200	1.360	1.6320
X94_P0	1.200	1.768	2.1216
X94_P4	1.200	1.768	2.1216
X94_P10	1.200	1.768	2.1216
X94_P16	1.200	1.768	2.1216
X133_P0	1.200	2.448	2.9376
X133_P4	1.200	2.448	2.9376
X133_P10	1.200	2.448	2.9376
X133_P16	1.200	2.448	2.9376

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X5_P0	X5_P4	X5_P10	X5_P16
A	0.0006	0.0006	0.0006	0.0006
	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0008	0.0008	0.0009	0.0009
	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0015	0.0015	0.0016	0.0017
	X23_P0	X23_P4	X23_P10	X23_P16
A	0.0022	0.0023	0.0024	0.0025
	X31_P0	X31_P4	X31_P10	X31_P16
A	0.0029	0.0030	0.0032	0.0033
	X39_P0	X39_P4	X39_P10	X39_P16
A	0.0036	0.0038	0.0039	0.0041
	X47_P0	X47_P4	X47_P10	X47_P16
A	0.0045	0.0046	0.0048	0.0050
	X55_P0	X55_P4	X55_P10	X55_P16
A	0.0052	0.0053	0.0055	0.0058
	X61_P0	X61_P4	X61_P10	X61_P16
A	0.0057	0.0060	0.0062	0.0065
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0068	0.0070	0.0072	0.0076
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0094	0.0096	0.0101	0.0105
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0139	0.0142	0.0149	0.0154

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X5_P4	X5_P0	X5_P4
A to Z ↓	0.0074	0.0086	3.0585	3.2628

A to Z ↑	0.0139	0.0156	5.5124	6.0685
	X5_P10	**X5_P16**	**X5_P10**	**X5_P16**
A to Z ↓	0.0101	0.0112	3.5553	3.8244
A to Z ↑	0.0178	0.0197	6.9447	7.7994
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0067	0.0076	1.9486	2.0757
A to Z ↑	0.0115	0.0130	3.0035	3.2807
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0090	0.0101	2.2574	2.4215
A to Z ↑	0.0150	0.0167	3.7297	4.1714
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0055	0.0064	0.9641	1.0266
A to Z ↑	0.0100	0.0115	1.5030	1.6404
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0077	0.0087	1.1155	1.1957
A to Z ↑	0.0133	0.0148	1.8600	2.0826
	X23_P0	**X23_P4**	**X23_P0**	**X23_P4**
A to Z ↓	0.0059	0.0069	0.6893	0.7343
A to Z ↑	0.0102	0.0117	1.0209	1.1127
	X23_P10	**X23_P16**	**X23_P10**	**X23_P16**
A to Z ↓	0.0082	0.0093	0.7983	0.8561
A to Z ↑	0.0135	0.0151	1.2620	1.4119
	X31_P0	**X31_P4**	**X31_P0**	**X31_P4**
A to Z ↓	0.0056	0.0065	0.4996	0.5322
A to Z ↑	0.0098	0.0112	0.7640	0.8338
	X31_P10	**X31_P16**	**X31_P10**	**X31_P16**
A to Z ↓	0.0077	0.0088	0.5786	0.6204
A to Z ↑	0.0129	0.0146	0.9460	1.0566
	X39_P0	**X39_P4**	**X39_P0**	**X39_P4**
A to Z ↓	0.0060	0.0070	0.4045	0.4309
A to Z ↑	0.0101	0.0116	0.6154	0.6718
	X39_P10	**X39_P16**	**X39_P10**	**X39_P16**
A to Z ↓	0.0083	0.0093	0.4686	0.5028
A to Z ↑	0.0135	0.0151	0.7617	0.8507
	X47_P0	**X47_P4**	**X47_P0**	**X47_P4**
A to Z ↓	0.0059	0.0068	0.3362	0.3583
A to Z ↑	0.0100	0.0114	0.5124	0.5592
	X47_P10	**X47_P16**	**X47_P10**	**X47_P16**
A to Z ↓	0.0081	0.0092	0.3899	0.4183
A to Z ↑	0.0133	0.0149	0.6340	0.7080
	X55_P0	**X55_P4**	**X55_P0**	**X55_P4**
A to Z ↓	0.0063	0.0072	0.2903	0.3094
A to Z ↑	0.0103	0.0118	0.4406	0.4807
	X55_P10	**X55_P16**	**X55_P10**	**X55_P16**
A to Z ↓	0.0085	0.0096	0.3368	0.3614
A to Z ↑	0.0137	0.0152	0.5450	0.6081
	X61_P0	**X61_P4**	**X61_P0**	**X61_P4**
A to Z ↓	0.0064	0.0073	0.2609	0.2782
A to Z ↑	0.0103	0.0118	0.3987	0.4352
	X61_P10	**X61_P16**	**X61_P10**	**X61_P16**
A to Z ↓	0.0086	0.0097	0.3027	0.3249
A to Z ↑	0.0138	0.0153	0.4936	0.5509

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0068	0.0077	0.2298	0.2448
A to Z ↑	0.0107	0.0122	0.3465	0.3774
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0090	0.0102	0.2660	0.2853
A to Z ↑	0.0141	0.0157	0.4276	0.4772
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0079	0.0087	0.1772	0.1886
A to Z ↑	0.0115	0.0130	0.2646	0.2878
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0101	0.0113	0.2048	0.2195
A to Z ↑	0.0150	0.0166	0.3249	0.3620
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0095	0.0102	0.1322	0.1404
A to Z ↑	0.0130	0.0142	0.1923	0.2089
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0116	0.0129	0.1523	0.1627
A to Z ↑	0.0164	0.0182	0.2355	0.2617

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P0	2.035e-07	1.267e-12
X5_P4	6.203e-08	1.268e-12
X5_P10	3.023e-08	1.269e-12
X5_P16	2.665e-08	1.268e-12
X8_P0	3.308e-07	1.268e-12
X8_P4	9.488e-08	1.268e-12
X8_P10	4.727e-08	1.268e-12
X8_P16	4.227e-08	1.267e-12
X16_P0	6.625e-07	1.519e-12
X16_P4	1.891e-07	1.519e-12
X16_P10	9.451e-08	1.519e-12
X16_P16	8.503e-08	1.521e-12
X23_P0	9.105e-07	1.771e-12
X23_P4	2.600e-07	1.769e-12
X23_P10	1.332e-07	1.768e-12
X23_P16	1.212e-07	1.773e-12
X31_P0	1.210e-06	2.023e-12
X31_P4	3.434e-07	2.021e-12
X31_P10	1.783e-07	2.025e-12
X31_P16	1.636e-07	2.025e-12
X39_P0	1.470e-06	2.274e-12
X39_P4	4.191e-07	2.272e-12
X39_P10	2.199e-07	2.273e-12
X39_P16	2.027e-07	2.278e-12
X47_P0	1.706e-06	2.527e-12
X47_P4	4.926e-07	2.524e-12
X47_P10	2.613e-07	2.529e-12
X47_P16	2.417e-07	2.530e-12
X55_P0	2.005e-06	2.779e-12
X55_P4	5.710e-07	2.777e-12
X55_P10	3.030e-07	2.763e-12

X55_P16	2.807e-07	2.782e-12
X61_P0	2.239e-06	3.031e-12
X61_P4	6.311e-07	3.029e-12
X61_P10	3.347e-07	3.017e-12
X61_P16	3.103e-07	3.035e-12
X70_P0	2.486e-06	3.287e-12
X70_P4	7.183e-07	3.287e-12
X70_P10	3.856e-07	3.289e-12
X70_P16	3.585e-07	3.282e-12
X94_P0	3.269e-06	4.041e-12
X94_P4	9.448e-07	4.042e-12
X94_P10	5.101e-07	4.040e-12
X94_P16	4.755e-07	4.041e-12
X133_P0	4.744e-06	5.297e-12
X133_P4	1.336e-06	5.298e-12
X133_P10	7.192e-07	5.294e-12
X133_P16	6.713e-07	5.295e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	4.795e-04	4.490e-04	4.381e-04	4.384e-04
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	6.661e-04	6.075e-04	5.791e-04	5.722e-04
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	1.099e-03	9.677e-04	8.914e-04	8.646e-04
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	1.717e-03	1.537e-03	1.430e-03	1.393e-03
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	2.128e-03	1.864e-03	1.676e-03	1.661e-03
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	2.759e-03	2.455e-03	2.258e-03	2.209e-03
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	3.233e-03	2.855e-03	2.630e-03	2.570e-03
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	3.885e-03	3.438e-03	3.196e-03	3.098e-03
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	4.191e-03	3.679e-03	3.400e-03	3.274e-03
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	4.954e-03	4.383e-03	4.053e-03	3.948e-03
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	6.600e-03	5.740e-03	5.249e-03	5.063e-03
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	1.020e-02	8.640e-03	7.807e-03	7.508e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	1.911e-07	2.072e-07	-1.770e-07	-9.920e-08
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	1.519e-06	9.621e-07	4.151e-07	4.200e-09
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	3.934e-07	2.876e-07	2.742e-07	9.503e-07

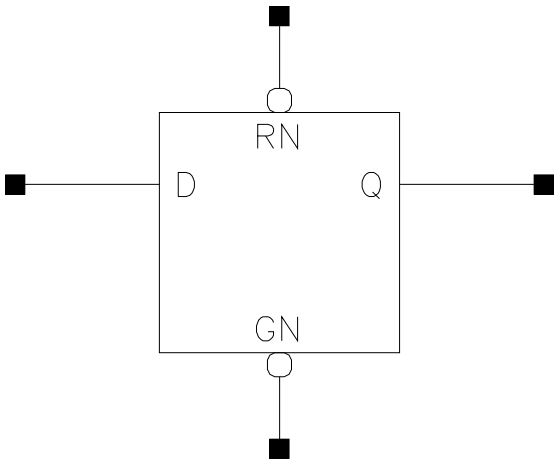
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	3.560e-06	4.969e-06	4.730e-07	8.841e-07
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	1.730e-07	4.131e-06	3.848e-06	-4.680e-07
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	1.622e-06	6.974e-06	1.801e-06	-3.500e-08
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	-1.489e-06	7.085e-06	-5.020e-07	-5.820e-07
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	7.094e-06	9.170e-07	-1.760e-06	2.181e-06
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	4.199e-06	1.920e-07	2.654e-06	2.023e-06
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	-4.260e-07	-6.600e-08	-1.822e-06	-8.430e-07
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	1.155e-06	7.700e-08	1.443e-06	-3.830e-07
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	-8.370e-07	6.730e-07	-3.493e-06	-2.761e-06

CNLDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
D	0.0011	0.0012	0.0012	0.0013
GN	0.0021	0.0022	0.0023	0.0024
RN	0.0006	0.0006	0.0007	0.0007

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	X33_P4	X33_P0	X33_P4

D to Q ↓	0.0536	0.0612	0.4738	0.5101
D to Q ↑	0.0475	0.0532	0.7819	0.8572
GN to Q ↓	0.0493	0.0559	0.4739	0.5107
GN to Q ↑	0.0541	0.0602	0.7817	0.8572
RN to Q ↓	0.0664	0.0749	0.4973	0.5380
RN to Q ↑	0.0524	0.0583	0.7820	0.8576
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D to Q ↓	0.0728	0.0844	0.5629	0.6117
D to Q ↑	0.0620	0.0708	0.9799	1.1002
GN to Q ↓	0.0659	0.0757	0.5638	0.6125
GN to Q ↑	0.0702	0.0803	0.9802	1.1004
RN to Q ↓	0.0885	0.1026	0.5972	0.6513
RN to Q ↑	0.0674	0.0765	0.9798	1.1001

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X33_P0	X33_P4	X33_P10	X33_P16
D ↓	hold_rising to GN	-0.0167	-0.0213	-0.0309	-0.0407
D ↑	hold_rising to GN	-0.0114	-0.0163	-0.0237	-0.0286
D ↓	setup_rising to GN	0.0588	0.0689	0.0805	0.0929
D ↑	setup_rising to GN	0.0511	0.0560	0.0686	0.0731
GN ↓	min_pulse_width to GN	0.0638	0.0732	0.0837	0.0943
RN ↓	min_pulse_width to RN	0.0828	0.0898	0.1067	0.1235
RN ↑	recovery_rising to GN	0.0557	0.0603	0.0703	0.0825
RN ↑	removal_rising to GN	-0.0357	-0.0410	-0.0512	-0.0557

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X33_P0	1.845e-06	5.301e-12
X33_P4	5.854e-07	5.299e-12
X33_P10	3.796e-07	5.325e-12
X33_P16	3.788e-07	5.302e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	1.110e-04	1.273e-04	1.233e-04	1.189e-04
GN (output stable)	1.649e-03	1.630e-03	1.644e-03	1.685e-03
RN (output stable)	4.787e-05	4.153e-05	3.734e-05	3.541e-05
D to Q	1.052e-02	1.034e-02	1.046e-02	1.076e-02
GN to Q	1.356e-02	1.339e-02	1.356e-02	1.395e-02
RN to Q	8.102e-03	7.835e-03	7.815e-03	7.980e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	-7.792e-06	-1.331e-05	-1.313e-05	-1.211e-05

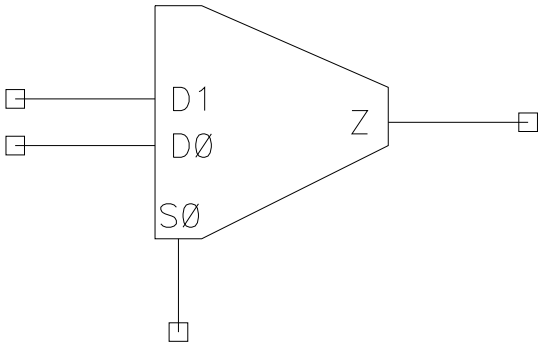
GN (output stable)	9.019e-06	6.246e-06	5.026e-06	4.416e-06
RN (output stable)	1.590e-06	2.188e-06	2.482e-06	2.441e-06
D to Q	-3.504e-06	-8.900e-06	-1.864e-05	-2.136e-05
GN to Q	5.898e-06	-6.514e-06	-1.064e-05	9.213e-07
RN to Q	-7.040e-06	-1.221e-05	-1.782e-05	-2.383e-05

CNMUX21

Cell Description

2:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320
X17_P4	1.200	1.360	1.6320
X17_P10	1.200	1.360	1.6320
X17_P16	1.200	1.360	1.6320
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0010	0.0010	0.0011	0.0011
D1	0.0010	0.0010	0.0011	0.0011
S0	0.0014	0.0014	0.0015	0.0016
	X33_P0	X33_P4	X33_P10	X33_P16
D0	0.0018	0.0019	0.0020	0.0021
D1	0.0018	0.0019	0.0020	0.0021
S0	0.0023	0.0024	0.0025	0.0027

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X17_P4	X17_P0	X17_P4

D0 to Z ↓	0.0363	0.0404	0.8680	0.9284
D0 to Z ↑	0.0273	0.0302	1.4901	1.6318
D1 to Z ↓	0.0360	0.0402	0.8668	0.9280
D1 to Z ↑	0.0259	0.0286	1.4888	1.6283
S0 to Z ↓	0.0331	0.0369	0.8641	0.9259
S0 to Z ↑	0.0317	0.0353	1.4900	1.6300
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0470	0.0531	1.0190	1.1008
D0 to Z ↑	0.0348	0.0390	1.8596	2.0817
D1 to Z ↓	0.0469	0.0532	1.0176	1.0996
D1 to Z ↑	0.0328	0.0367	1.8548	2.0798
S0 to Z ↓	0.0430	0.0487	1.0158	1.0984
S0 to Z ↑	0.0408	0.0458	1.8569	2.0828
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
D0 to Z ↓	0.0348	0.0391	0.4493	0.4816
D0 to Z ↑	0.0271	0.0302	0.7507	0.8208
D1 to Z ↓	0.0361	0.0408	0.4502	0.4823
D1 to Z ↑	0.0261	0.0290	0.7500	0.8216
S0 to Z ↓	0.0346	0.0388	0.4484	0.4811
S0 to Z ↑	0.0323	0.0361	0.7503	0.8218
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D0 to Z ↓	0.0455	0.0517	0.5287	0.5715
D0 to Z ↑	0.0349	0.0392	0.9360	1.0489
D1 to Z ↓	0.0474	0.0542	0.5295	0.5725
D1 to Z ↑	0.0332	0.0374	0.9357	1.0471
S0 to Z ↓	0.0451	0.0512	0.5283	0.5713
S0 to Z ↑	0.0416	0.0468	0.9362	1.0490

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P0	1.753e-06	3.284e-12
X17_P4	5.180e-07	3.283e-12
X17_P10	2.677e-07	3.283e-12
X17_P16	2.436e-07	3.284e-12
X33_P0	3.271e-06	5.305e-12
X33_P4	9.727e-07	5.300e-12
X33_P10	5.166e-07	5.301e-12
X33_P16	4.752e-07	5.304e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	1.250e-03	1.203e-03	1.179e-03	1.177e-03
D1 (output stable)	1.174e-03	1.122e-03	1.093e-03	1.090e-03
S0 (output stable)	1.281e-03	1.289e-03	1.324e-03	1.366e-03
D0 to Z	4.870e-03	4.797e-03	4.910e-03	5.051e-03
D1 to Z	4.731e-03	4.662e-03	4.775e-03	4.931e-03
S0 to Z	5.202e-03	5.152e-03	5.282e-03	5.446e-03
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	1.852e-03	1.739e-03	1.676e-03	1.660e-03
D1 (output stable)	1.943e-03	1.833e-03	1.773e-03	1.754e-03
S0 (output stable)	2.023e-03	2.038e-03	2.098e-03	2.177e-03

D0 to Z	9.358e-03	9.322e-03	9.521e-03	9.847e-03
D1 to Z	9.246e-03	9.200e-03	9.336e-03	9.728e-03
S0 to Z	1.023e-02	1.021e-02	1.043e-02	1.081e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

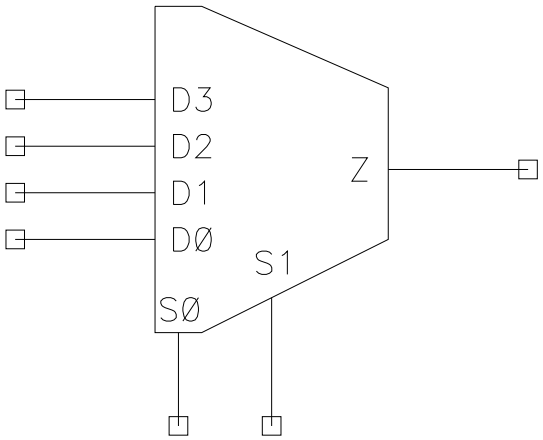
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	6.805e-07	3.354e-07	-7.000e-10	3.532e-07
D1 (output stable)	1.068e-06	7.655e-08	1.711e-07	4.959e-07
S0 (output stable)	1.208e-07	1.371e-07	-1.327e-07	-1.781e-07
D0 to Z	-2.746e-07	-2.335e-08	-3.773e-07	-5.750e-07
D1 to Z	1.002e-07	3.097e-07	3.480e-08	-6.456e-07
S0 to Z	-2.055e-07	-3.255e-08	-3.005e-07	-4.099e-07
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	6.040e-07	1.898e-07	4.691e-07	7.410e-08
D1 (output stable)	6.630e-07	1.445e-07	9.800e-08	-6.045e-07
S0 (output stable)	-1.865e-07	3.348e-07	1.998e-07	1.225e-07
D0 to Z	-2.130e-07	-6.900e-07	-6.550e-08	-1.073e-06
D1 to Z	-4.745e-07	-8.195e-07	1.125e-07	-9.180e-07
S0 to Z	-2.350e-07	-4.429e-07	-1.050e-08	-5.482e-07

CNMUX41

Cell Description

4:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	2.400	2.176	5.2224
X17_P4	2.400	2.176	5.2224
X17_P10	2.400	2.176	5.2224
X17_P16	2.400	2.176	5.2224
X27_P0	2.400	2.312	5.5488
X27_P4	2.400	2.312	5.5488
X27_P10	2.400	2.312	5.5488
X27_P16	2.400	2.312	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0015	0.0015	0.0016	0.0017
D1	0.0014	0.0015	0.0015	0.0016
D2	0.0015	0.0015	0.0016	0.0017
D3	0.0015	0.0015	0.0016	0.0017
S0	0.0038	0.0040	0.0042	0.0044
S1	0.0021	0.0022	0.0024	0.0026

	X27_P0	X27_P4	X27_P10	X27_P16
D0	0.0014	0.0014	0.0015	0.0015
D1	0.0013	0.0014	0.0014	0.0015
D2	0.0013	0.0013	0.0014	0.0015
D3	0.0013	0.0013	0.0014	0.0014
S0	0.0033	0.0035	0.0037	0.0039
S1	0.0020	0.0021	0.0022	0.0024

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
D0 to Z ↓	0.0572	0.0650	0.9085	0.9741
D0 to Z ↑	0.0380	0.0421	1.5160	1.6583
D1 to Z ↓	0.0566	0.0643	0.9090	0.9733
D1 to Z ↑	0.0376	0.0417	1.5153	1.6580
D2 to Z ↓	0.0585	0.0664	0.9091	0.9736
D2 to Z ↑	0.0375	0.0415	1.5115	1.6537
D3 to Z ↓	0.0580	0.0659	0.9086	0.9736
D3 to Z ↑	0.0373	0.0412	1.5113	1.6542
S0 to Z ↓	0.0653	0.0741	0.9066	0.9717
S0 to Z ↑	0.0512	0.0572	1.5154	1.6584
S1 to Z ↓	0.0428	0.0478	0.9098	0.9745
S1 to Z ↑	0.0382	0.0417	1.5140	1.6555
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0756	0.0863	1.0675	1.1557
D0 to Z ↑	0.0481	0.0542	1.8869	2.1169
D1 to Z ↓	0.0749	0.0854	1.0676	1.1558
D1 to Z ↑	0.0477	0.0536	1.8884	2.1173
D2 to Z ↓	0.0775	0.0885	1.0674	1.1560
D2 to Z ↑	0.0474	0.0532	1.8849	2.1133
D3 to Z ↓	0.0769	0.0878	1.0677	1.1566
D3 to Z ↑	0.0471	0.0529	1.8842	2.1120
S0 to Z ↓	0.0867	0.0993	1.0653	1.1525
S0 to Z ↑	0.0662	0.0751	1.8885	2.1168
S1 to Z ↓	0.0549	0.0627	1.0661	1.1535
S1 to Z ↑	0.0482	0.0545	1.8855	2.1133
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0646	0.0733	0.5823	0.6251
D0 to Z ↑	0.0469	0.0521	1.0217	1.1181
D1 to Z ↓	0.0583	0.0659	0.5722	0.6135
D1 to Z ↑	0.0458	0.0509	1.0211	1.1178
D2 to Z ↓	0.0677	0.0771	0.5846	0.6280
D2 to Z ↑	0.0463	0.0514	1.0200	1.1166
D3 to Z ↓	0.0672	0.0764	0.5847	0.6281
D3 to Z ↑	0.0458	0.0508	1.0204	1.1166
S0 to Z ↓	0.0724	0.0820	0.5789	0.6217
S0 to Z ↑	0.0583	0.0653	1.0227	1.1184
S1 to Z ↓	0.0475	0.0531	0.5820	0.6246
S1 to Z ↑	0.0513	0.0560	1.0211	1.1161
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.0859	0.0983	0.6886	0.7469
D0 to Z ↑	0.0603	0.0681	1.2725	1.4271

D1 to Z ↓	0.0769	0.0877	0.6746	0.7314
D1 to Z ↑	0.0589	0.0666	1.2730	1.4265
D2 to Z ↓	0.0905	0.1037	0.6923	0.7516
D2 to Z ↑	0.0592	0.0668	1.2708	1.4251
D3 to Z ↓	0.0897	0.1028	0.6922	0.7516
D3 to Z ↑	0.0586	0.0661	1.2704	1.4253
S0 to Z ↓	0.0962	0.1102	0.6844	0.7424
S0 to Z ↑	0.0760	0.0863	1.2734	1.4274
S1 to Z ↓	0.0618	0.0710	0.6860	0.7444
S1 to Z ↑	0.0653	0.0744	1.2706	1.4247

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P0	2.485e-06	6.398e-12
X17_P4	9.564e-07	6.398e-12
X17_P10	6.694e-07	6.398e-12
X17_P16	6.709e-07	6.399e-12
X27_P0	2.552e-06	6.704e-12
X27_P4	9.472e-07	6.696e-12
X27_P10	6.405e-07	6.705e-12
X27_P16	6.358e-07	6.704e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	2.025e-04	2.180e-04	2.013e-04	1.916e-04
D1 (output stable)	1.859e-04	2.094e-04	1.909e-04	1.797e-04
D2 (output stable)	1.160e-04	1.601e-04	1.553e-04	1.492e-04
D3 (output stable)	2.072e-04	2.391e-04	2.286e-04	2.237e-04
S0 (output stable)	4.011e-03	4.322e-03	4.535e-03	4.748e-03
S1 (output stable)	2.830e-03	2.664e-03	2.651e-03	2.718e-03
D0 to Z	7.878e-03	7.935e-03	8.083e-03	8.310e-03
D1 to Z	7.884e-03	7.956e-03	8.108e-03	8.332e-03
D2 to Z	8.194e-03	8.231e-03	8.377e-03	8.591e-03
D3 to Z	8.099e-03	8.143e-03	8.295e-03	8.513e-03
S0 to Z	1.240e-02	1.273e-02	1.312e-02	1.358e-02
S1 to Z	8.025e-03	7.785e-03	7.789e-03	7.989e-03
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	2.025e-04	2.187e-04	2.031e-04	1.947e-04
D1 (output stable)	1.860e-04	2.039e-04	1.854e-04	1.763e-04
D2 (output stable)	1.113e-04	1.521e-04	1.480e-04	1.432e-04
D3 (output stable)	1.985e-04	2.232e-04	2.115e-04	2.069e-04
S0 (output stable)	3.739e-03	3.998e-03	4.177e-03	4.354e-03
S1 (output stable)	2.557e-03	2.425e-03	2.424e-03	2.484e-03
D0 to Z	9.262e-03	9.137e-03	9.233e-03	9.455e-03
D1 to Z	9.150e-03	9.069e-03	9.186e-03	9.414e-03
D2 to Z	9.444e-03	9.327e-03	9.389e-03	9.606e-03
D3 to Z	9.345e-03	9.231e-03	9.300e-03	9.523e-03
S0 to Z	1.333e-02	1.344e-02	1.374e-02	1.415e-02
S1 to Z	9.238e-03	8.889e-03	8.872e-03	9.103e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

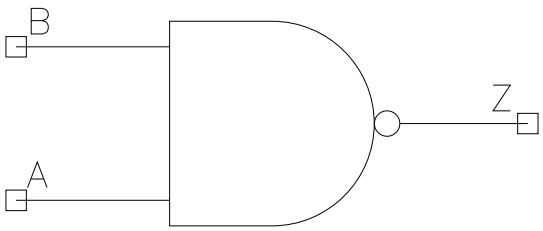
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	-7.609e-06	-1.551e-05	-1.429e-05	-1.255e-05
D1 (output stable)	-4.263e-06	-1.629e-05	-1.587e-05	-1.451e-05
D2 (output stable)	6.434e-06	-1.469e-05	-1.753e-05	-1.641e-05
D3 (output stable)	-4.034e-06	-2.063e-05	-2.136e-05	-1.963e-05
S0 (output stable)	-8.250e-05	-1.281e-04	-1.220e-04	-1.108e-04
S1 (output stable)	1.052e-04	6.117e-05	5.231e-05	4.764e-05
D0 to Z	-4.411e-06	-1.569e-05	-1.777e-05	-1.649e-05
D1 to Z	-4.887e-06	-1.774e-05	-2.086e-05	-2.002e-05
D2 to Z	-5.097e-06	-1.826e-05	-1.989e-05	-1.806e-05
D3 to Z	-3.090e-06	-1.599e-05	-1.857e-05	-1.707e-05
S0 to Z	-5.887e-05	-9.362e-05	-9.238e-05	-8.507e-05
S1 to Z	1.396e-04	7.536e-05	5.768e-05	5.071e-05
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	-8.381e-06	-1.574e-05	-1.462e-05	-1.289e-05
D1 (output stable)	-5.563e-06	-1.629e-05	-1.570e-05	-1.442e-05
D2 (output stable)	3.138e-06	-1.551e-05	-1.798e-05	-1.682e-05
D3 (output stable)	-7.484e-06	-2.110e-05	-2.090e-05	-1.908e-05
S0 (output stable)	-8.441e-05	-1.215e-04	-1.128e-04	-1.018e-04
S1 (output stable)	9.861e-05	5.856e-05	5.089e-05	4.634e-05
D0 to Z	-4.988e-06	-1.672e-05	-1.829e-05	-1.709e-05
D1 to Z	-7.647e-06	-1.915e-05	-2.130e-05	-2.051e-05
D2 to Z	-7.380e-06	-1.847e-05	-1.906e-05	-1.791e-05
D3 to Z	-4.970e-06	-1.651e-05	-1.744e-05	-1.712e-05
S0 to Z	-5.980e-05	-8.983e-05	-8.633e-05	-7.957e-05
S1 to Z	1.351e-04	7.145e-05	5.483e-05	4.791e-05

CNNAND2

Cell Description

2 input NAND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X33_P0	1.200	1.224	1.4688
X33_P4	1.200	1.224	1.4688
X33_P10	1.200	1.224	1.4688
X33_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0019	0.0020	0.0021	0.0022
B	0.0018	0.0018	0.0019	0.0020
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0008	0.0008	0.0008	0.0009
B	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0092	0.0104	1.1973	1.2803
A to Z ↑	0.0159	0.0178	1.5454	1.6881
B to Z ↓	0.0078	0.0089	1.2222	1.3067
B to Z ↑	0.0128	0.0144	1.5582	1.7003
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0120	0.0131	1.4025	1.5164
A to Z ↑	0.0205	0.0229	1.9162	2.1448
B to Z ↓	0.0104	0.0115	1.4307	1.5461
B to Z ↑	0.0165	0.0181	1.9311	2.1635
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0354	0.0395	0.4382	0.4686
A to Z ↑	0.0423	0.0474	0.7477	0.8188
B to Z ↓	0.0363	0.0406	0.4383	0.4690
B to Z ↑	0.0411	0.0460	0.7486	0.8184
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0464	0.0530	0.5135	0.5548
A to Z ↑	0.0555	0.0632	0.9319	1.0452
B to Z ↓	0.0477	0.0545	0.5139	0.5549
B to Z ↑	0.0539	0.0613	0.9336	1.0459

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X15_P0	7.565e-07	2.528e-12
X15_P4	2.641e-07	2.527e-12
X15_P10	1.656e-07	2.527e-12
X15_P16	1.609e-07	2.529e-12
X33_P0	1.884e-06	3.030e-12
X33_P4	5.679e-07	3.029e-12
X33_P10	2.960e-07	3.033e-12
X33_P16	2.674e-07	3.028e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.270e-04	1.006e-04	7.431e-05	6.346e-05
B (output stable)	3.896e-04	3.937e-04	3.953e-04	3.915e-04
A to Z	2.451e-03	2.413e-03	2.443e-03	2.500e-03
B to Z	1.669e-03	1.551e-03	1.492e-03	1.470e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	2.333e-05	1.896e-05	1.459e-05	1.249e-05
B (output stable)	5.538e-05	5.460e-05	5.206e-05	5.008e-05
A to Z	8.447e-03	8.555e-03	9.023e-03	9.461e-03
B to Z	8.294e-03	8.383e-03	8.838e-03	9.258e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

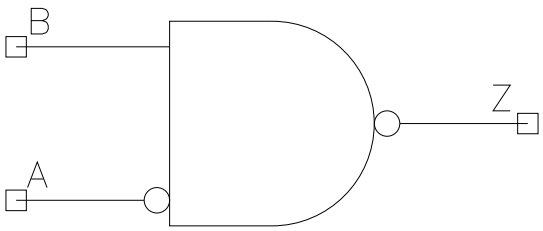
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.800e-08	-1.320e-08	-9.880e-08	-1.195e-07
B (output stable)	2.210e-08	-6.010e-08	-1.249e-07	-1.565e-07
A to Z	1.716e-06	1.256e-06	-8.922e-07	-2.138e-06
B to Z	7.250e-07	2.780e-07	2.074e-07	7.975e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	7.344e-08	5.568e-08	2.940e-08	1.321e-08
B (output stable)	6.480e-08	3.740e-08	9.500e-09	6.100e-09
A to Z	-1.030e-07	-3.517e-07	-3.776e-07	-5.427e-07
B to Z	-3.300e-09	-2.479e-07	-1.777e-07	-4.660e-08

CNNAND2A

Cell Description

2 input NAND with A input inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0008	0.0008	0.0009	0.0009
B	0.0009	0.0009	0.0010	0.0011
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0012	0.0012	0.0013	0.0013
B	0.0008	0.0009	0.0009	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0341	0.0387	0.8536	0.9160
A to Z ↑	0.0247	0.0274	1.4878	1.6298
B to Z ↓	0.0347	0.0393	0.8527	0.9133
B to Z ↑	0.0336	0.0376	1.4850	1.6273
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**

A to Z ↓	0.0458	0.0517	1.0056	1.0879
A to Z ↑	0.0315	0.0349	1.8580	2.0825
B to Z ↓	0.0472	0.0537	1.0052	1.0872
B to Z ↑	0.0439	0.0492	1.8547	2.0801
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0373	0.0421	0.5148	0.5530
A to Z ↑	0.0278	0.0309	0.9685	1.0626
B to Z ↓	0.0366	0.0414	0.5143	0.5522
B to Z ↑	0.0373	0.0419	0.9645	1.0585
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0495	0.0562	0.6082	0.6591
A to Z ↑	0.0355	0.0397	1.2133	1.3623
B to Z ↓	0.0491	0.0565	0.6078	0.6592
B to Z ↑	0.0487	0.0552	1.2104	1.3593

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P0	1.297e-06	2.529e-12
X17_P4	3.944e-07	2.528e-12
X17_P10	1.957e-07	2.528e-12
X17_P16	1.724e-07	2.524e-12
X27_P0	1.814e-06	3.536e-12
X27_P4	5.542e-07	3.537e-12
X27_P10	2.736e-07	3.535e-12
X27_P16	2.404e-07	3.535e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	8.931e-05	1.271e-04	1.226e-04	1.146e-04
B (output stable)	1.159e-03	1.131e-03	1.138e-03	1.164e-03
A to Z	3.888e-03	3.897e-03	4.069e-03	4.168e-03
B to Z	5.231e-03	5.255e-03	5.493e-03	5.642e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	3.418e-04	3.942e-04	3.486e-04	3.611e-04
B (output stable)	1.348e-03	1.334e-03	1.334e-03	1.400e-03
A to Z	6.430e-03	6.411e-03	6.651e-03	6.882e-03
B to Z	7.570e-03	7.611e-03	7.917e-03	8.233e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

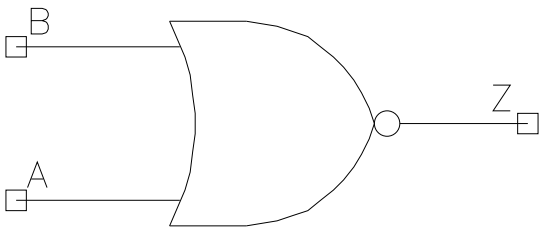
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	-1.401e-05	-3.232e-05	-3.306e-05	-3.037e-05
B (output stable)	2.926e-05	2.737e-05	2.539e-05	2.232e-05
A to Z	-1.926e-07	-3.376e-06	-5.053e-06	-5.194e-06
B to Z	2.000e-07	-3.742e-07	-3.440e-07	-5.661e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	-7.206e-05	-9.829e-05	-9.402e-05	-9.330e-05
B (output stable)	8.173e-05	7.982e-05	7.191e-05	7.213e-05
A to Z	-3.223e-06	-1.042e-05	-1.504e-05	-1.592e-05
B to Z	-6.073e-07	-6.818e-07	-5.374e-07	-7.793e-07

CNNOR2

Cell Description

2 input NOR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	0.952	1.1424
X14_P4	1.200	0.952	1.1424
X14_P10	1.200	0.952	1.1424
X14_P16	1.200	0.952	1.1424
X33_P0	1.200	1.496	1.7952
X33_P4	1.200	1.496	1.7952
X33_P10	1.200	1.496	1.7952
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0021	0.0022	0.0023	0.0024
B	0.0020	0.0020	0.0021	0.0021
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0009	0.0009	0.0009	0.0010
B	0.0009	0.0009	0.0009	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0104	0.0116	0.9732	1.0359
A to Z ↑	0.0164	0.0188	2.1689	2.3810
B to Z ↓	0.0078	0.0088	0.9851	1.0483
B to Z ↑	0.0129	0.0147	2.1941	2.4073
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**

A to Z ↓	0.0134	0.0149	1.1255	1.2070
A to Z ↑	0.0214	0.0237	2.7047	3.0199
B to Z ↓	0.0102	0.0113	1.1408	1.2240
B to Z ↑	0.0171	0.0190	2.7321	3.0474
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0385	0.0434	0.4326	0.4628
A to Z ↑	0.0425	0.0481	0.7464	0.8170
B to Z ↓	0.0367	0.0415	0.4323	0.4628
B to Z ↑	0.0419	0.0475	0.7465	0.8158
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0506	0.0581	0.5078	0.5480
A to Z ↑	0.0561	0.0643	0.9290	1.0422
B to Z ↓	0.0485	0.0560	0.5072	0.5485
B to Z ↑	0.0552	0.0634	0.9296	1.0413

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X14_P0	8.125e-07	2.527e-12
X14_P4	2.578e-07	2.528e-12
X14_P10	1.616e-07	2.527e-12
X14_P16	1.583e-07	2.531e-12
X33_P0	2.208e-06	3.535e-12
X33_P4	6.562e-07	3.535e-12
X33_P10	3.607e-07	3.534e-12
X33_P16	3.402e-07	3.535e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	2.650e-04	2.363e-04	1.883e-04	1.650e-04
B (output stable)	1.003e-04	7.668e-05	4.366e-05	1.108e-05
A to Z	2.897e-03	2.897e-03	2.922e-03	3.012e-03
B to Z	1.690e-03	1.559e-03	1.494e-03	1.477e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	6.569e-05	6.081e-05	5.100e-05	4.528e-05
B (output stable)	1.582e-05	9.353e-06	4.974e-06	1.319e-06
A to Z	9.371e-03	9.574e-03	9.881e-03	1.042e-02
B to Z	9.044e-03	9.234e-03	9.504e-03	1.004e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

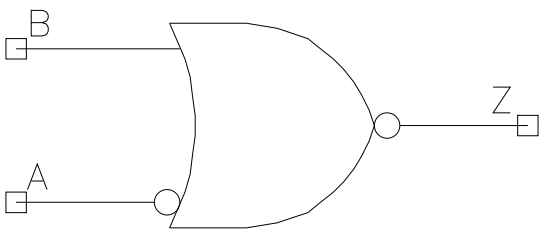
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	-1.197e-05	-1.519e-05	-1.297e-05	-1.172e-05
B (output stable)	9.638e-05	8.575e-05	5.157e-05	1.156e-05
A to Z	-7.730e-07	-1.104e-05	-1.407e-05	-1.661e-05
B to Z	-2.140e-07	-1.930e-07	2.254e-07	2.319e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	-3.218e-06	-4.712e-06	-4.491e-06	-4.109e-06
B (output stable)	2.942e-05	2.615e-05	1.594e-05	2.577e-06
A to Z	-5.190e-07	-3.295e-06	-5.286e-06	-5.583e-06
B to Z	-1.230e-07	-4.830e-07	-2.036e-07	-3.850e-07

CNNOR2A

Cell Description

2 input NOR with A input Inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	1.224	1.4688
X15_P4	1.200	1.224	1.4688
X15_P10	1.200	1.224	1.4688
X15_P16	1.200	1.224	1.4688
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0013	0.0013	0.0014	0.0014
B	0.0009	0.0009	0.0010	0.0010
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0015	0.0015	0.0016	0.0017
B	0.0009	0.0009	0.0010	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0334	0.0375	1.0510	1.1269
A to Z ↑	0.0228	0.0255	1.4901	1.6304
B to Z ↓	0.0310	0.0350	1.0463	1.1200
B to Z ↑	0.0329	0.0369	1.4861	1.6310
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0435	0.0491	1.2364	1.3357
A to Z ↑	0.0293	0.0329	1.8611	2.0880
B to Z ↓	0.0411	0.0471	1.2314	1.3317
B to Z ↑	0.0428	0.0483	1.8584	2.0858
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0291	0.0327	0.5939	0.6370
A to Z ↑	0.0243	0.0269	0.7942	0.8698
B to Z ↓	0.0313	0.0354	0.5938	0.6369
B to Z ↑	0.0356	0.0401	0.7931	0.8677
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0380	0.0427	0.6983	0.7559
A to Z ↑	0.0308	0.0345	0.9913	1.1110
B to Z ↓	0.0416	0.0476	0.6997	0.7570
B to Z ↑	0.0465	0.0525	0.9886	1.1108

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X15_P0	1.209e-06	3.032e-12
X15_P4	3.488e-07	3.031e-12
X15_P10	2.033e-07	3.029e-12
X15_P16	1.966e-07	3.026e-12
X27_P0	1.847e-06	3.528e-12
X27_P4	5.199e-07	3.533e-12
X27_P10	3.089e-07	3.532e-12
X27_P16	3.017e-07	3.532e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	6.786e-05	4.930e-05	3.274e-05	2.432e-05
B (output stable)	1.358e-03	1.267e-03	1.265e-03	1.299e-03
A to Z	4.140e-03	4.183e-03	4.320e-03	4.479e-03
B to Z	5.294e-03	5.373e-03	5.573e-03	5.795e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	8.999e-05	6.736e-05	4.610e-05	3.578e-05
B (output stable)	1.588e-03	1.527e-03	1.546e-03	1.603e-03
A to Z	6.644e-03	6.666e-03	6.920e-03	7.139e-03
B to Z	8.100e-03	8.211e-03	8.555e-03	8.909e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

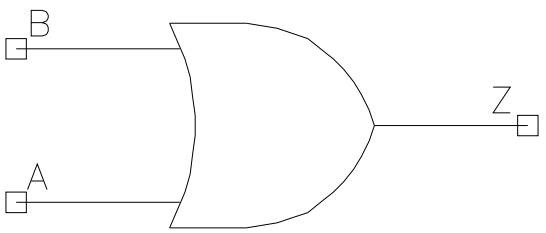
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	3.311e-07	3.682e-07	4.104e-07	4.254e-07
B (output stable)	-1.036e-06	-1.574e-07	3.190e-07	-3.765e-07
A to Z	-1.319e-07	-1.032e-07	-4.861e-07	-1.490e-07
B to Z	5.090e-08	9.450e-08	1.975e-07	2.047e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	2.830e-08	2.570e-08	6.000e-09	-1.310e-08
B (output stable)	2.770e-08	2.244e-07	1.553e-07	-4.097e-07
A to Z	-3.701e-07	-4.146e-07	-9.120e-07	-9.727e-07
B to Z	-6.130e-08	-1.453e-07	-2.609e-07	-4.848e-07

CNOR2

Cell Description

2 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X20_P0	1.200	1.360	1.6320
X20_P4	1.200	1.360	1.6320
X20_P10	1.200	1.360	1.6320
X20_P16	1.200	1.360	1.6320
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320
X37_P0	1.200	1.632	1.9584
X37_P4	1.200	1.632	1.9584
X37_P10	1.200	1.632	1.9584
X37_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0015	0.0016	0.0017	0.0018
B	0.0014	0.0015	0.0016	0.0017
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0023	0.0024	0.0026	0.0027
B	0.0024	0.0025	0.0027	0.0028
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0016	0.0017	0.0018	0.0018

B	0.0016	0.0017	0.0018	0.0018
	X37_P0	X37_P4	X37_P10	X37_P16
A	0.0023	0.0024	0.0026	0.0027
B	0.0024	0.0025	0.0026	0.0027

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0286	0.0323	0.9593	1.0286
A to Z ↑	0.0198	0.0218	1.5557	1.7057
B to Z ↓	0.0265	0.0298	0.9613	1.0297
B to Z ↑	0.0181	0.0200	1.5540	1.7021
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0377	0.0424	1.1291	1.2196
A to Z ↑	0.0250	0.0277	1.9462	2.1858
B to Z ↓	0.0350	0.0394	1.1300	1.2213
B to Z ↑	0.0230	0.0254	1.9446	2.1848
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0268	0.0305	0.7480	0.8016
A to Z ↑	0.0200	0.0222	1.0816	1.1857
B to Z ↓	0.0245	0.0280	0.7489	0.8029
B to Z ↑	0.0178	0.0199	1.0797	1.1831
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0352	0.0396	0.8796	0.9509
A to Z ↑	0.0252	0.0279	1.3500	1.5150
B to Z ↓	0.0326	0.0367	0.8806	0.9510
B to Z ↑	0.0226	0.0251	1.3495	1.5130
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0343	0.0388	0.4378	0.4687
A to Z ↑	0.0236	0.0261	0.7334	0.8039
B to Z ↓	0.0322	0.0365	0.4376	0.4692
B to Z ↑	0.0217	0.0241	0.7327	0.8032
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0453	0.0515	0.5147	0.5565
A to Z ↑	0.0298	0.0332	0.9168	1.0291
B to Z ↓	0.0426	0.0484	0.5150	0.5561
B to Z ↑	0.0275	0.0306	0.9157	1.0266
	X37_P0	**X37_P4**	**X37_P0**	**X37_P4**
A to Z ↓	0.0311	0.0355	0.4209	0.4509
A to Z ↑	0.0225	0.0251	0.5992	0.6559
B to Z ↓	0.0295	0.0337	0.4212	0.4511
B to Z ↑	0.0206	0.0230	0.5977	0.6555
	X37_P10	**X37_P16**	**X37_P10**	**X37_P16**
A to Z ↓	0.0413	0.0467	0.4952	0.5361
A to Z ↑	0.0285	0.0316	0.7464	0.8378
B to Z ↓	0.0392	0.0445	0.4956	0.5360
B to Z ↑	0.0262	0.0291	0.7467	0.8366

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X15_P0	1.080e-06	2.528e-12

X15_P4	3.412e-07	2.528e-12
X15_P10	1.833e-07	2.528e-12
X15_P16	1.676e-07	2.527e-12
X20_P0	1.675e-06	3.284e-12
X20_P4	5.171e-07	3.282e-12
X20_P10	2.775e-07	3.281e-12
X20_P16	2.538e-07	3.295e-12
X33_P0	1.819e-06	3.285e-12
X33_P4	5.799e-07	3.285e-12
X33_P10	2.989e-07	3.282e-12
X33_P16	2.661e-07	3.284e-12
X37_P0	2.257e-06	3.787e-12
X37_P4	6.998e-07	3.784e-12
X37_P10	3.653e-07	3.787e-12
X37_P16	3.288e-07	3.786e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.479e-04	1.267e-04	1.003e-04	8.717e-05
B (output stable)	7.027e-05	5.522e-05	3.064e-05	7.137e-06
A to Z	4.299e-03	4.296e-03	4.485e-03	4.625e-03
B to Z	3.581e-03	3.522e-03	3.653e-03	3.749e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.672e-04	2.305e-04	1.834e-04	1.599e-04
B (output stable)	1.054e-04	8.029e-05	4.279e-05	1.053e-05
A to Z	6.563e-03	6.680e-03	6.864e-03	7.131e-03
B to Z	5.311e-03	5.347e-03	5.465e-03	5.653e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.902e-04	1.564e-04	1.133e-04	9.463e-05
B (output stable)	1.113e-04	9.119e-05	6.127e-05	2.056e-05
A to Z	7.742e-03	7.768e-03	7.983e-03	8.315e-03
B to Z	6.807e-03	6.771e-03	6.932e-03	7.214e-03
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	2.677e-04	2.306e-04	1.834e-04	1.588e-04
B (output stable)	1.055e-04	8.015e-05	4.699e-05	9.972e-06
A to Z	9.298e-03	9.490e-03	9.755e-03	1.011e-02
B to Z	8.079e-03	8.177e-03	8.374e-03	8.690e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	-7.105e-06	-8.422e-06	-7.555e-06	-6.738e-06
B (output stable)	5.617e-05	4.903e-05	2.741e-05	6.061e-06
A to Z	-1.803e-06	-6.381e-06	-9.510e-06	-1.038e-05
B to Z	-1.187e-07	7.900e-09	-7.185e-07	-8.604e-07
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	-1.270e-05	-1.540e-05	-1.343e-05	-1.183e-05
B (output stable)	1.002e-04	8.841e-05	5.103e-05	1.072e-05
A to Z	-2.585e-06	-1.109e-05	-1.603e-05	-1.767e-05
B to Z	-2.018e-07	-4.680e-08	-1.199e-06	-1.160e-06
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	-1.360e-05	-1.562e-05	-1.362e-05	-1.202e-05

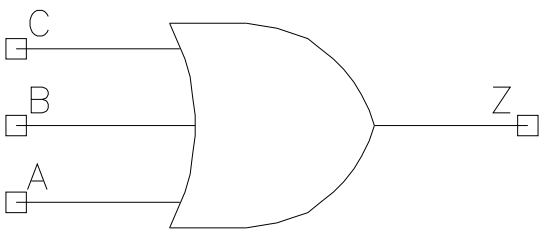
B (output stable)	1.052e-04	9.419e-05	6.338e-05	2.030e-05
A to Z	-3.547e-06	-1.267e-05	-1.864e-05	-1.971e-05
B to Z	-2.034e-07	-6.447e-07	-3.033e-07	-2.903e-07
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	-1.273e-05	-1.542e-05	-1.342e-05	-1.182e-05
B (output stable)	1.005e-04	8.869e-05	5.156e-05	9.898e-06
A to Z	-2.557e-06	-1.108e-05	-1.628e-05	-1.732e-05
B to Z	-6.689e-07	-8.213e-07	-1.125e-06	-3.396e-07

CNOR3

Cell Description

3 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	1.360	1.6320
X14_P4	1.200	1.360	1.6320
X14_P10	1.200	1.360	1.6320
X14_P16	1.200	1.360	1.6320
X20_P0	1.200	1.632	1.9584
X20_P4	1.200	1.632	1.9584
X20_P10	1.200	1.632	1.9584
X20_P16	1.200	1.632	1.9584
X27_P0	1.200	2.040	2.4480
X27_P4	1.200	2.040	2.4480
X27_P10	1.200	2.040	2.4480
X27_P16	1.200	2.040	2.4480

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0009	0.0009	0.0010	0.0010
B	0.0009	0.0009	0.0009	0.0010
C	0.0009	0.0009	0.0010	0.0010
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0009	0.0009	0.0010	0.0010
B	0.0008	0.0009	0.0009	0.0010
C	0.0009	0.0009	0.0010	0.0010
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0011	0.0012	0.0012	0.0013
B	0.0012	0.0012	0.0012	0.0013

C	0.0009	0.0010	0.0010	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0498	0.0566	1.0492	1.1260
A to Z ↑	0.0387	0.0435	1.5629	1.7160
B to Z ↓	0.0509	0.0579	1.0486	1.1256
B to Z ↑	0.0404	0.0455	1.5634	1.7158
C to Z ↓	0.0453	0.0512	1.0477	1.1254
C to Z ↑	0.0361	0.0407	1.5641	1.7120
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0665	0.0761	1.2354	1.3369
A to Z ↑	0.0507	0.0576	1.9550	2.1932
B to Z ↓	0.0681	0.0779	1.2358	1.3378
B to Z ↑	0.0529	0.0600	1.9546	2.1932
C to Z ↓	0.0598	0.0682	1.2347	1.3364
C to Z ↑	0.0474	0.0538	1.9523	2.1887
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0498	0.0561	0.7784	0.8339
A to Z ↑	0.0421	0.0473	1.1048	1.2088
B to Z ↓	0.0508	0.0574	0.7787	0.8338
B to Z ↑	0.0436	0.0489	1.1056	1.2091
C to Z ↓	0.0442	0.0496	0.7773	0.8338
C to Z ↑	0.0404	0.0453	1.1052	1.2108
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0660	0.0754	0.9148	0.9889
A to Z ↑	0.0557	0.0637	1.3782	1.5459
B to Z ↓	0.0676	0.0772	0.9144	0.9900
B to Z ↑	0.0575	0.0656	1.3790	1.5451
C to Z ↓	0.0582	0.0662	0.9142	0.9891
C to Z ↑	0.0533	0.0609	1.3773	1.5442
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0405	0.0459	0.6956	0.7466
A to Z ↑	0.0377	0.0421	0.9141	1.0041
B to Z ↓	0.0393	0.0445	0.6957	0.7458
B to Z ↑	0.0354	0.0395	0.9134	1.0026
C to Z ↓	0.0341	0.0382	0.6898	0.7397
C to Z ↑	0.0300	0.0333	0.7438	0.8152
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0537	0.0609	0.8213	0.8918
A to Z ↑	0.0485	0.0545	1.1457	1.2868
B to Z ↓	0.0520	0.0592	0.8207	0.8934
B to Z ↑	0.0454	0.0510	1.1440	1.2846
C to Z ↓	0.0440	0.0495	0.8121	0.8835
C to Z ↑	0.0380	0.0425	0.9297	1.0429

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X14_P0	1.570e-06	3.284e-12
X14_P4	4.943e-07	3.283e-12

X14_P10	2.626e-07	3.386e-12
X14_P16	2.380e-07	3.282e-12
X20_P0	1.899e-06	3.840e-12
X20_P4	5.940e-07	3.840e-12
X20_P10	3.057e-07	3.838e-12
X20_P16	2.735e-07	3.841e-12
X27_P0	1.635e-06	4.701e-12
X27_P4	5.635e-07	4.703e-12
X27_P10	3.338e-07	4.700e-12
X27_P16	3.120e-07	4.700e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	4.688e-04	4.676e-04	4.871e-04	5.092e-04
B (output stable)	6.111e-04	6.268e-04	6.511e-04	6.762e-04
C (output stable)	1.203e-03	1.186e-03	1.198e-03	1.227e-03
A to Z	6.237e-03	6.379e-03	6.632e-03	6.900e-03
B to Z	6.549e-03	6.725e-03	7.009e-03	7.294e-03
C to Z	6.138e-03	6.263e-03	6.499e-03	6.746e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	4.536e-04	4.519e-04	4.690e-04	4.897e-04
B (output stable)	5.907e-04	6.041e-04	6.266e-04	6.497e-04
C (output stable)	1.125e-03	1.101e-03	1.105e-03	1.130e-03
A to Z	7.569e-03	7.648e-03	7.972e-03	8.295e-03
B to Z	7.874e-03	7.982e-03	8.338e-03	8.677e-03
C to Z	7.441e-03	7.506e-03	7.821e-03	8.121e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.553e-03	1.624e-03	1.715e-03	1.794e-03
B (output stable)	1.319e-03	1.375e-03	1.464e-03	1.549e-03
C (output stable)	3.440e-03	3.464e-03	3.549e-03	3.703e-03
A to Z	9.097e-03	9.287e-03	9.693e-03	1.006e-02
B to Z	8.566e-03	8.723e-03	9.098e-03	9.469e-03
C to Z	7.341e-03	7.386e-03	7.558e-03	7.805e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	1.244e-05	6.385e-07	-9.333e-10	-8.533e-09
B (output stable)	-2.295e-06	-4.589e-06	-5.271e-06	-4.869e-06
C (output stable)	3.048e-07	2.858e-07	2.231e-07	-1.647e-08
A to Z	1.263e-07	2.774e-08	-2.043e-07	-1.971e-07
B to Z	-3.904e-07	-3.020e-06	-5.085e-06	-4.761e-06
C to Z	3.358e-07	2.775e-07	2.403e-07	-2.687e-07
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	1.161e-05	6.571e-07	-7.133e-09	-2.313e-08
B (output stable)	-2.175e-06	-4.411e-06	-5.016e-06	-4.794e-06
C (output stable)	3.737e-07	1.976e-07	2.329e-07	5.333e-09
A to Z	1.601e-07	5.120e-08	-5.981e-07	-2.876e-07
B to Z	3.720e-08	-3.046e-06	-5.266e-06	-5.075e-06
C to Z	3.139e-07	6.500e-09	3.270e-07	-1.950e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	-3.936e-06	-6.179e-06	-6.431e-06	-5.910e-06

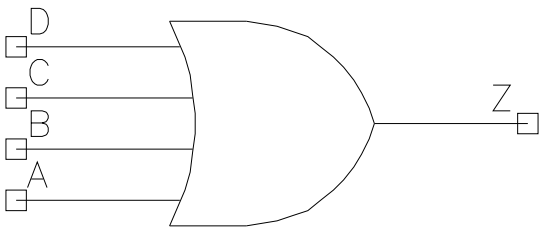
B (output stable)	2.212e-05	2.757e-06	1.091e-06	1.108e-06
C (output stable)	-2.430e-06	-1.982e-06	-1.824e-06	-1.841e-06
A to Z	-1.248e-06	-5.945e-06	-7.245e-06	-7.008e-06
B to Z	-6.800e-07	-6.330e-07	-3.470e-07	-4.070e-07
C to Z	-2.160e-07	-5.200e-07	-8.190e-07	-8.870e-07

CNOR4

Cell Description

4 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X20_P4	1.200	2.176	2.6112
X20_P10	1.200	2.176	2.6112
X20_P16	1.200	2.176	2.6112
X27_P0	1.200	2.312	2.7744
X27_P4	1.200	2.312	2.7744
X27_P10	1.200	2.312	2.7744
X27_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0013	0.0013	0.0014	0.0014
B	0.0014	0.0014	0.0015	0.0015
C	0.0013	0.0013	0.0014	0.0015
D	0.0014	0.0014	0.0015	0.0016
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0013	0.0013	0.0013	0.0014
B	0.0014	0.0014	0.0015	0.0015
C	0.0013	0.0013	0.0014	0.0014
D	0.0015	0.0015	0.0016	0.0016

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0374	0.0426	0.7888	0.8450
A to Z ↑	0.0303	0.0338	1.2894	1.4171
B to Z ↓	0.0349	0.0398	0.7880	0.8463
B to Z ↑	0.0284	0.0317	1.2897	1.4151
C to Z ↓	0.0356	0.0402	0.7864	0.8430
C to Z ↑	0.0291	0.0322	1.2814	1.4074
D to Z ↓	0.0336	0.0379	0.7874	0.8432
D to Z ↑	0.0273	0.0302	1.2790	1.4051
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0494	0.0560	0.9324	1.0124
A to Z ↑	0.0388	0.0439	1.6193	1.8184
B to Z ↓	0.0463	0.0527	0.9318	1.0147
B to Z ↑	0.0364	0.0412	1.6185	1.8184
C to Z ↓	0.0470	0.0523	0.9307	1.0083
C to Z ↑	0.0370	0.0407	1.6084	1.8078
D to Z ↓	0.0446	0.0497	0.9293	1.0085
D to Z ↑	0.0347	0.0382	1.6055	1.8058
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0408	0.0461	0.6514	0.6990
A to Z ↑	0.0321	0.0356	0.9661	1.0610
B to Z ↓	0.0384	0.0435	0.6519	0.6982
B to Z ↑	0.0303	0.0337	0.9654	1.0598
C to Z ↓	0.0368	0.0418	0.6489	0.6947
C to Z ↑	0.0294	0.0327	0.9594	1.0535
D to Z ↓	0.0347	0.0397	0.6475	0.6957
D to Z ↑	0.0271	0.0302	0.9579	1.0524
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0538	0.0607	0.7694	0.8374
A to Z ↑	0.0410	0.0459	1.2114	1.3617
B to Z ↓	0.0510	0.0577	0.7696	0.8373
B to Z ↑	0.0389	0.0435	1.2112	1.3611
C to Z ↓	0.0487	0.0553	0.7662	0.8312
C to Z ↑	0.0373	0.0418	1.2042	1.3538
D to Z ↓	0.0463	0.0526	0.7647	0.8315
D to Z ↑	0.0344	0.0386	1.2028	1.3526

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X20_P0	1.530e-06	5.001e-12
X20_P4	5.530e-07	5.002e-12
X20_P10	3.420e-07	5.001e-12
X20_P16	3.248e-07	5.002e-12
X27_P0	1.691e-06	5.262e-12
X27_P4	6.226e-07	5.262e-12
X27_P10	3.894e-07	5.259e-12
X27_P16	3.701e-07	5.264e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	1.696e-03	1.744e-03	1.799e-03	1.888e-03

B (output stable)	1.397e-03	1.440e-03	1.524e-03	1.630e-03
C (output stable)	1.750e-03	1.782e-03	1.797e-03	1.809e-03
D (output stable)	1.425e-03	1.401e-03	1.394e-03	1.398e-03
A to Z	7.806e-03	8.029e-03	8.370e-03	8.766e-03
B to Z	7.235e-03	7.414e-03	7.715e-03	8.101e-03
C to Z	6.998e-03	7.074e-03	7.361e-03	7.479e-03
D to Z	6.419e-03	6.441e-03	6.691e-03	6.799e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.982e-03	2.026e-03	2.112e-03	2.200e-03
B (output stable)	1.684e-03	1.727e-03	1.853e-03	1.957e-03
C (output stable)	1.831e-03	1.888e-03	1.885e-03	1.928e-03
D (output stable)	1.500e-03	1.502e-03	1.487e-03	1.515e-03
A to Z	9.177e-03	9.354e-03	9.768e-03	1.016e-02
B to Z	8.616e-03	8.754e-03	9.133e-03	9.512e-03
C to Z	7.722e-03	7.851e-03	8.059e-03	8.381e-03
D to Z	7.166e-03	7.256e-03	7.425e-03	7.730e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

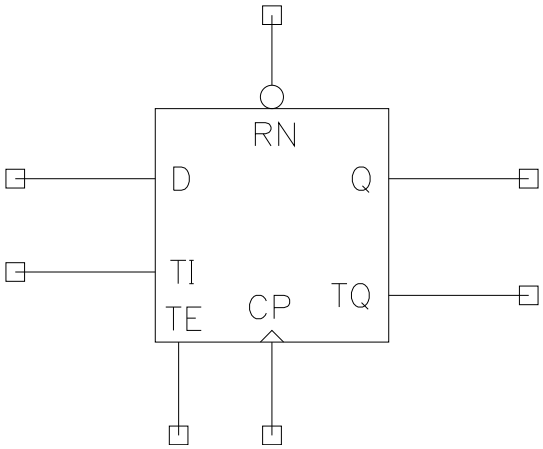
Pin Cycle (vdds)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	-4.385e-06	-6.865e-06	-7.103e-06	-6.607e-06
B (output stable)	1.851e-05	2.820e-06	8.589e-07	9.413e-07
C (output stable)	-9.757e-06	-2.183e-05	-2.319e-05	-2.161e-05
D (output stable)	2.337e-05	1.308e-05	1.128e-05	1.035e-05
A to Z	-1.869e-06	-5.934e-06	-7.807e-06	-8.003e-06
B to Z	-3.990e-07	-5.360e-07	2.840e-07	7.900e-08
C to Z	-1.771e-06	-5.500e-06	-8.699e-06	-7.533e-06
D to Z	-5.940e-07	-3.090e-07	-3.820e-07	-4.124e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	-4.351e-06	-7.029e-06	-7.160e-06	-6.632e-06
B (output stable)	1.846e-05	2.733e-06	6.760e-07	8.107e-07
C (output stable)	-9.540e-06	-2.195e-05	-2.335e-05	-2.147e-05
D (output stable)	2.365e-05	1.310e-05	1.146e-05	1.052e-05
A to Z	-1.740e-06	-6.580e-06	-7.854e-06	-7.214e-06
B to Z	-2.070e-07	-2.920e-07	-5.490e-07	2.500e-08
C to Z	-1.729e-06	-5.798e-06	-8.517e-06	-7.430e-06
D to Z	-6.000e-07	-3.710e-07	-1.550e-07	-3.380e-07

CNSDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.080	4.8960
X15_P4	1.200	4.080	4.8960
X15_P10	1.200	4.080	4.8960
X15_P16	1.200	4.080	4.8960

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0008	0.0008	0.0008	0.0009
D	0.0006	0.0006	0.0006	0.0007
RN	0.0008	0.0008	0.0008	0.0009

TE	0.0010	0.0010	0.0010	0.0011
TI	0.0003	0.0003	0.0003	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	X15_P4	X15_P0	X15_P4
CP to Q ↓	0.0720	0.0811	1.0607	1.1359
CP to Q ↑	0.0741	0.0830	1.4665	1.6059
CP to TQ ↓	0.0744	0.0840	4.9943	5.3539
CP to TQ ↑	0.0795	0.0893	13.8235	15.4948
RN to Q ↓	0.0884	0.1004	1.0574	1.1318
RN to TQ ↓	0.0908	0.1034	4.9947	5.3542
	X15_P10	X15_P16	X15_P10	X15_P16
CP to Q ↓	0.0953	0.1091	1.2462	1.3445
CP to Q ↑	0.0970	0.1106	1.8287	2.0534
CP to TQ ↓	0.0988	0.1132	5.8707	6.3281
CP to TQ ↑	0.1046	0.1195	18.0338	20.4580
RN to Q ↓	0.1193	0.1376	1.2419	1.3412
RN to TQ ↓	0.1228	0.1416	5.8675	6.3281

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.0930	0.1104	0.1349	0.1566
CP ↑	min_pulse_width to CP	0.0416	0.0426	0.0510	0.0568
D ↓	hold_rising to CP	-0.0193	-0.0267	-0.0338	-0.0436
D ↑	hold_rising to CP	-0.0117	-0.0139	-0.0192	-0.0241
D ↓	setup_rising to CP	0.0636	0.0758	0.0929	0.1075
D ↑	setup_rising to CP	0.0439	0.0491	0.0592	0.0662
RN ↓	min_pulse_width to RN	0.0681	0.0779	0.0898	0.1018
RN ↑	recovery_rising to CP	0.0226	0.0244	0.0297	0.0370
RN ↑	removal_rising to CP	-0.0074	-0.0099	-0.0152	-0.0149
TE ↓	hold_rising to CP	-0.0140	-0.0218	-0.0316	-0.0387
TE ↑	hold_rising to CP	-0.0215	-0.0268	-0.0342	-0.0388
TE ↓	setup_rising to CP	0.0654	0.0780	0.0930	0.1048
TE ↑	setup_rising to CP	0.1199	0.1447	0.1762	0.2110
TI ↓	hold_rising to CP	-0.0673	-0.0823	-0.1088	-0.1291
TI ↑	hold_rising to CP	-0.0228	-0.0282	-0.0344	-0.0408
TI ↓	setup_rising to CP	0.1206	0.1414	0.1719	0.2028
TI ↑	setup_rising to CP	0.0581	0.0642	0.0754	0.0851

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X15_P0	2.601e-06	8.325e-12
X15_P4	8.522e-07	8.324e-12
X15_P10	5.015e-07	8.323e-12
X15_P16	4.789e-07	8.325e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

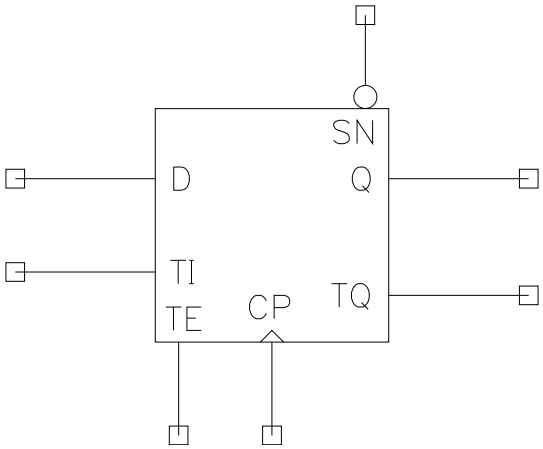
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	4.555e-03	4.581e-03	4.635e-03	4.701e-03
Clock 100Mhz Data 25Mhz	7.393e-03	7.468e-03	7.626e-03	7.800e-03
Clock 100Mhz Data 50Mhz	1.023e-02	1.035e-02	1.062e-02	1.090e-02
Clock = 0 Data 100Mhz	4.212e-03	4.242e-03	4.294e-03	4.356e-03
Clock = 1 Data 100Mhz	5.077e-05	4.358e-05	3.706e-05	3.247e-05

CNSDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.216	5.0592
X15_P4	1.200	4.216	5.0592
X15_P10	1.200	4.216	5.0592
X15_P16	1.200	4.216	5.0592

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0008	0.0008	0.0008	0.0009
D	0.0004	0.0004	0.0005	0.0005
SN	0.0015	0.0015	0.0016	0.0017

TE	0.0010	0.0010	0.0010	0.0011
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	X15_P4	X15_P0	X15_P4
CP to Q ↓	0.0723	0.0816	1.0607	1.1365
CP to Q ↑	0.0746	0.0835	1.4653	1.6063
CP to TQ ↓	0.0749	0.0845	5.0067	5.3660
CP to TQ ↑	0.0801	0.0899	13.8345	15.5007
SN to Q ↑	0.0738	0.0832	1.4654	1.6059
SN to TQ ↑	0.0793	0.0896	13.8335	15.5040
	X15_P10	X15_P16	X15_P10	X15_P16
CP to Q ↓	0.0958	0.1096	1.2471	1.3450
CP to Q ↑	0.0975	0.1112	1.8288	2.0542
CP to TQ ↓	0.0994	0.1139	5.8839	6.3431
CP to TQ ↑	0.1052	0.1202	18.0418	20.4638
SN to Q ↑	0.0977	0.1116	1.8290	2.0538
SN to TQ ↑	0.1054	0.1206	18.0412	20.4691

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.1008	0.1182	0.1446	0.1663
CP ↑	min_pulse_width to CP	0.0416	0.0463	0.0510	0.0568
D ↓	hold_rising to CP	-0.0214	-0.0285	-0.0387	-0.0485
D ↑	hold_rising to CP	-0.0090	-0.0117	-0.0165	-0.0214
D ↓	setup_rising to CP	0.0685	0.0807	0.0978	0.1124
D ↑	setup_rising to CP	0.0390	0.0443	0.0491	0.0539
SN ↓	min_pulse_width to SN	0.0496	0.0566	0.0637	0.0708
SN ↑	recovery_rising to CP	0.0027	0.0057	0.0079	0.0134
SN ↑	removal_rising to CP	0.0290	0.0283	0.0358	0.0407
TE ↓	hold_rising to CP	-0.0193	-0.0267	-0.0365	-0.0436
TE ↑	hold_rising to CP	-0.0188	-0.0240	-0.0286	-0.0335
TE ↓	setup_rising to CP	0.0688	0.0808	0.0953	0.1124
TE ↑	setup_rising to CP	0.1301	0.1514	0.1859	0.2177
TI ↓	hold_rising to CP	-0.0763	-0.0923	-0.1131	-0.1340
TI ↑	hold_rising to CP	-0.0179	-0.0241	-0.0290	-0.0352
TI ↓	setup_rising to CP	0.1263	0.1512	0.1819	0.2126
TI ↑	setup_rising to CP	0.0491	0.0539	0.0642	0.0754

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X15_P0	2.685e-06	8.584e-12
X15_P4	8.914e-07	8.576e-12
X15_P10	5.185e-07	8.576e-12
X15_P16	4.924e-07	8.577e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

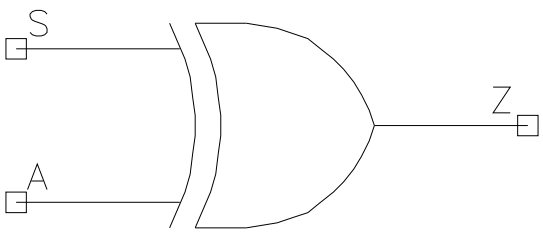
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	4.586e-03	4.599e-03	4.650e-03	4.715e-03
Clock 100Mhz Data 25Mhz	7.478e-03	7.548e-03	7.708e-03	7.882e-03
Clock 100Mhz Data 50Mhz	1.037e-02	1.050e-02	1.077e-02	1.105e-02
Clock = 0 Data 100Mhz	4.246e-03	4.278e-03	4.333e-03	4.397e-03
Clock = 1 Data 100Mhz	5.588e-05	5.093e-05	4.614e-05	4.283e-05

CNXOR2

Cell Description

2 input Exclusive OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X16_P0	1.200	1.360	1.6320
X16_P4	1.200	1.360	1.6320
X16_P10	1.200	1.360	1.6320
X16_P16	1.200	1.360	1.6320
X27_P0	1.200	2.040	2.4480
X27_P4	1.200	2.040	2.4480
X27_P10	1.200	2.040	2.4480
X27_P16	1.200	2.040	2.4480

Truth Table

A	S	Z
1	S	!S
0	S	S

Pin Capacitance

Pin	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0011	0.0011	0.0011	0.0012
S	0.0015	0.0016	0.0017	0.0018
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0015	0.0016	0.0017	0.0018
S	0.0021	0.0022	0.0023	0.0024

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0401	0.0449	0.8995	0.9632
A to Z ↑	0.0355	0.0394	1.5043	1.6478
S to Z ↓	0.0311	0.0347	0.8982	0.9616
S to Z ↑	0.0293	0.0326	1.5028	1.6476
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0526	0.0604	1.0575	1.1441

A to Z ↑	0.0454	0.0512	1.8805	2.1122
S to Z ↓	0.0406	0.0465	1.0557	1.1431
S to Z ↑	0.0376	0.0426	1.8804	2.1124
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0411	0.0463	0.6013	0.6459
A to Z ↑	0.0386	0.0433	0.8022	0.8792
S to Z ↓	0.0342	0.0386	0.6009	0.6458
S to Z ↑	0.0329	0.0370	0.8022	0.8785
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0543	0.0619	0.7105	0.7694
A to Z ↑	0.0502	0.0566	1.0015	1.1230
S to Z ↓	0.0451	0.0513	0.7104	0.7690
S to Z ↑	0.0429	0.0484	1.0015	1.1238

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X16_P0	2.094e-06	3.284e-12
X16_P4	5.880e-07	3.283e-12
X16_P10	2.833e-07	3.285e-12
X16_P16	2.507e-07	3.282e-12
X27_P0	3.096e-06	4.606e-12
X27_P4	8.395e-07	4.604e-12
X27_P10	4.128e-07	4.600e-12
X27_P16	3.699e-07	4.603e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	6.258e-03	6.212e-03	6.359e-03	6.611e-03
S to Z	5.160e-03	5.089e-03	5.207e-03	5.424e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	1.096e-02	1.092e-02	1.120e-02	1.152e-02
S to Z	8.047e-03	7.976e-03	8.137e-03	8.397e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

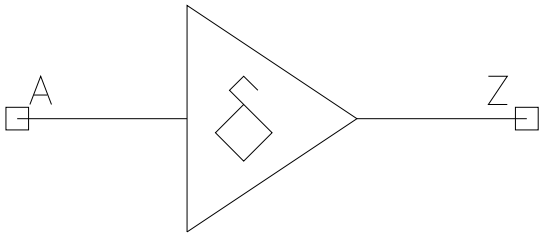
Pin Cycle (vdds)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	1.138e-07	-1.853e-07	-4.892e-07	-4.889e-07
S to Z	1.429e-07	1.610e-08	3.196e-07	-5.396e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	-1.306e-07	-4.044e-07	-6.132e-07	-1.023e-06
S to Z	-1.949e-07	-3.584e-07	-6.154e-07	-6.929e-07

DLYHF

Cell Description

Delay cell for Hold Time Fixing

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-DLYHFM4X7_P0	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X7_P4	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X7_P10	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X7_P16	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X15_P0	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM4X15_P4	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM4X15_P10	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM4X15_P16	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM8X7_P0	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X7_P4	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X7_P10	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X7_P16	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X15_P0	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X15_P4	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X15_P10	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X15_P16	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X54_P0	1.200	4.216	5.0592

C12T28SOI_LR_-DLYHFM8X54_P4	1.200	4.216	5.0592
C12T28SOI_LR_-DLYHFM8X54_P10	1.200	4.216	5.0592
C12T28SOI_LR_-DLYHFM8X54_P16	1.200	4.216	5.0592

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C12T28SOI_LR_-DLYHFM4X7_P0	C12T28SOI_LR_-DLYHFM4X7_P4	C12T28SOI_LR_-DLYHFM4X7_P10	C12T28SOI_LR_-DLYHFM4X7_P16
A	0.0008	0.0008	0.0008	0.0008
	C12T28SOI_LR_-DLYHFM4X15_P0	C12T28SOI_LR_-DLYHFM4X15_P4	C12T28SOI_LR_-DLYHFM4X15_P10	C12T28SOI_LR_-DLYHFM4X15_P16
A	0.0008	0.0008	0.0008	0.0008
	C12T28SOI_LR_-DLYHFM8X7_P0	C12T28SOI_LR_-DLYHFM8X7_P4	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A	0.0007	0.0007	0.0008	0.0008
	C12T28SOI_LR_-DLYHFM8X15_P0	C12T28SOI_LR_-DLYHFM8X15_P4	C12T28SOI_LR_-DLYHFM8X15_P10	C12T28SOI_LR_-DLYHFM8X15_P16
A	0.0007	0.0007	0.0007	0.0008
	C12T28SOI_LR_-DLYHFM8X54_P0	C12T28SOI_LR_-DLYHFM8X54_P4	C12T28SOI_LR_-DLYHFM8X54_P10	C12T28SOI_LR_-DLYHFM8X54_P16
A	0.0007	0.0007	0.0007	0.0008

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-DLYHFM4X7_P0	**C12T28SOI_LR_-DLYHFM4X7_P4**	**C12T28SOI_LR_-DLYHFM4X7_P0**	**C12T28SOI_LR_-DLYHFM4X7_P4**
A to Z ↓	0.1092	0.1250	2.0711	2.2283
A to Z ↑	0.1026	0.1167	3.4430	3.7810
	C12T28SOI_LR_-DLYHFM4X7_P10	**C12T28SOI_LR_-DLYHFM4X7_P16**	**C12T28SOI_LR_-DLYHFM4X7_P10**	**C12T28SOI_LR_-DLYHFM4X7_P16**
A to Z ↓	0.1502	0.1748	2.4619	2.6724
A to Z ↑	0.1391	0.1614	4.3230	4.8604
	C12T28SOI_LR_-DLYHFM4X15_P0	**C12T28SOI_LR_-DLYHFM4X15_P4**	**C12T28SOI_LR_-DLYHFM4X15_P0**	**C12T28SOI_LR_-DLYHFM4X15_P4**
A to Z ↓	0.1178	0.1350	1.0227	1.1031
A to Z ↑	0.1116	0.1274	1.5972	1.7538
	C12T28SOI_LR_-DLYHFM4X15_P10	**C12T28SOI_LR_-DLYHFM4X15_P16**	**C12T28SOI_LR_-DLYHFM4X15_P10**	**C12T28SOI_LR_-DLYHFM4X15_P16**
A to Z ↓	0.1629	0.1903	1.2233	1.3332
A to Z ↑	0.1525	0.1776	2.0040	2.2524
	C12T28SOI_LR_-DLYHFM8X7_P0	**C12T28SOI_LR_-DLYHFM8X7_P4**	**C12T28SOI_LR_-DLYHFM8X7_P0**	**C12T28SOI_LR_-DLYHFM8X7_P4**
A to Z ↓	0.1932	0.2225	2.0931	2.2545
A to Z ↑	0.1777	0.2028	3.1928	3.5020

	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A to Z ↓	0.2696	0.3153	2.4905	2.7105
A to Z ↑	0.2432	0.2828	3.9946	4.4899
	C12T28SOI_LR_-DLYHFM8X15_P0	**C12T28SOI_LR_-DLYHFM8X15_P4**	**C12T28SOI_LR_-DLYHFM8X15_P0**	**C12T28SOI_LR_-DLYHFM8X15_P4**
A to Z ↓	0.2003	0.2308	1.0260	1.1098
A to Z ↑	0.1866	0.2135	1.5989	1.7544
	C12T28SOI_LR_-DLYHFM8X15_P10	**C12T28SOI_LR_-DLYHFM8X15_P16**	**C12T28SOI_LR_-DLYHFM8X15_P10**	**C12T28SOI_LR_-DLYHFM8X15_P16**
A to Z ↓	0.2800	0.3283	1.2309	1.3448
A to Z ↑	0.2563	0.2989	2.0046	2.2558
	C12T28SOI_LR_-DLYHFM8X54_P0	**C12T28SOI_LR_-DLYHFM8X54_P4**	**C12T28SOI_LR_-DLYHFM8X54_P0**	**C12T28SOI_LR_-DLYHFM8X54_P4**
A to Z ↓	0.2561	0.2935	0.2696	0.2889
A to Z ↑	0.2345	0.2669	0.4590	0.5015
	C12T28SOI_LR_-DLYHFM8X54_P10	**C12T28SOI_LR_-DLYHFM8X54_P16**	**C12T28SOI_LR_-DLYHFM8X54_P10**	**C12T28SOI_LR_-DLYHFM8X54_P16**
A to Z ↓	0.3574	0.4195	0.3174	0.3432
A to Z ↑	0.3220	0.3748	0.5717	0.6409

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_DLYHFM4X7_P0	3.964e-07	2.780e-12
C12T28SOI_LR_DLYHFM4X7_P4	1.657e-07	2.779e-12
C12T28SOI_LR_DLYHFM4X7_P10	1.226e-07	2.779e-12
C12T28SOI_LR_DLYHFM4X7_P16	1.248e-07	2.782e-12
C12T28SOI_LR_DLYHFM4X15_P0	7.127e-07	3.031e-12
C12T28SOI_LR_DLYHFM4X15_P4	2.559e-07	3.032e-12
C12T28SOI_LR_DLYHFM4X15_P10	1.704e-07	3.033e-12
C12T28SOI_LR_DLYHFM4X15_P16	1.689e-07	3.029e-12
C12T28SOI_LR_DLYHFM8X7_P0	4.506e-07	4.292e-12
C12T28SOI_LR_DLYHFM8X7_P4	2.141e-07	4.289e-12
C12T28SOI_LR_DLYHFM8X7_P10	1.735e-07	4.292e-12
C12T28SOI_LR_DLYHFM8X7_P16	1.806e-07	4.294e-12
C12T28SOI_LR_DLYHFM8X15_P0	7.773e-07	4.543e-12
C12T28SOI_LR_DLYHFM8X15_P4	3.066e-07	4.542e-12
C12T28SOI_LR_DLYHFM8X15_P10	2.208e-07	4.546e-12
C12T28SOI_LR_DLYHFM8X15_P16	2.238e-07	4.546e-12
C12T28SOI_LR_DLYHFM8X54_P0	2.516e-06	8.567e-12
C12T28SOI_LR_DLYHFM8X54_P4	1.055e-06	8.588e-12
C12T28SOI_LR_DLYHFM8X54_P10	8.066e-07	8.573e-12
C12T28SOI_LR_DLYHFM8X54_P16	8.289e-07	8.568e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-DLYHFM4X7_P0	C12T28SOI_LR_-DLYHFM4X7_P4	C12T28SOI_LR_-DLYHFM4X7_P10	C12T28SOI_LR_-DLYHFM4X7_P16
A to Z	4.274e-03	4.354e-03	4.558e-03	4.753e-03
	C12T28SOI_LR_-DLYHFM4X15_P0	C12T28SOI_LR_-DLYHFM4X15_P4	C12T28SOI_LR_-DLYHFM4X15_P10	C12T28SOI_LR_-DLYHFM4X15_P16
A to Z	5.811e-03	5.781e-03	5.940e-03	6.152e-03

	C12T28SOI_LR_-DLYHFM8X7_P0	C12T28SOI_LR_-DLYHFM8X7_P4	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A to Z	6.823e-03	6.955e-03	7.267e-03	7.545e-03
	C12T28SOI_LR_-DLYHFM8X15_P0	C12T28SOI_LR_-DLYHFM8X15_P4	C12T28SOI_LR_-DLYHFM8X15_P10	C12T28SOI_LR_-DLYHFM8X15_P16
A to Z	8.331e-03	8.352e-03	8.602e-03	8.902e-03
	C12T28SOI_LR_-DLYHFM8X54_P0	C12T28SOI_LR_-DLYHFM8X54_P4	C12T28SOI_LR_-DLYHFM8X54_P10	C12T28SOI_LR_-DLYHFM8X54_P16
A to Z	2.711e-02	2.758e-02	2.915e-02	3.065e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

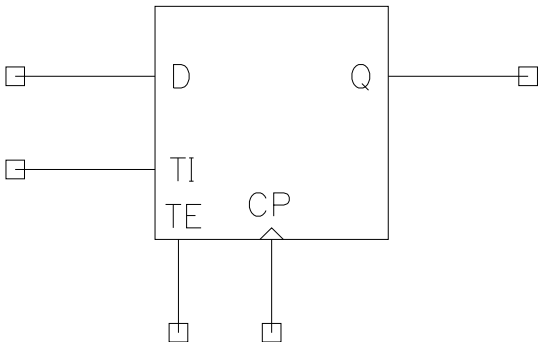
Pin Cycle (vdds)	C12T28SOI_LR_-DLYHFM4X7_P0	C12T28SOI_LR_-DLYHFM4X7_P4	C12T28SOI_LR_-DLYHFM4X7_P10	C12T28SOI_LR_-DLYHFM4X7_P16
A to Z	-4.421e-06	-9.421e-06	-1.898e-05	-2.019e-05
	C12T28SOI_LR_-DLYHFM4X15_P0	C12T28SOI_LR_-DLYHFM4X15_P4	C12T28SOI_LR_-DLYHFM4X15_P10	C12T28SOI_LR_-DLYHFM4X15_P16
A to Z	-4.415e-06	-8.963e-06	-1.998e-05	-2.164e-05
	C12T28SOI_LR_-DLYHFM8X7_P0	C12T28SOI_LR_-DLYHFM8X7_P4	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A to Z	-6.648e-06	-1.540e-05	-2.562e-05	-2.650e-05
	C12T28SOI_LR_-DLYHFM8X15_P0	C12T28SOI_LR_-DLYHFM8X15_P4	C12T28SOI_LR_-DLYHFM8X15_P10	C12T28SOI_LR_-DLYHFM8X15_P16
A to Z	-6.915e-06	-1.477e-05	-2.669e-05	-2.799e-05
	C12T28SOI_LR_-DLYHFM8X54_P0	C12T28SOI_LR_-DLYHFM8X54_P4	C12T28SOI_LR_-DLYHFM8X54_P10	C12T28SOI_LR_-DLYHFM8X54_P16
A to Z	-2.629e-05	-4.829e-05	-9.092e-05	-1.412e-04

SDFSYNCPQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.400	8.1600
X8_P4	2.400	3.400	8.1600
X8_P10	2.400	3.400	8.1600
X8_P16	2.400	3.400	8.1600

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0009	0.0009	0.0009	0.0010
D	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0010	0.0011
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X8_P4	X8_P0	X8_P4
CP to Q ↓	0.1253	0.1436	1.6584	1.7816
CP to Q ↑	0.1344	0.1526	2.9419	3.2308

	X8_P10	X8_P16	X8_P10	X8_P16
CP to Q ↓	0.1728	0.2017	1.9523	2.1106
CP to Q ↑	0.1811	0.2093	3.6831	4.1398

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1988	0.2330	0.2847	0.3364
CP ↑	min_pulse_width to CP	0.0684	0.0780	0.0935	0.1116
D ↓	hold_rising to CP	-0.0657	-0.0779	-0.0973	-0.1168
D ↑	hold_rising to CP	-0.0188	-0.0237	-0.0286	-0.0391
D ↓	setup_rising to CP	0.1224	0.1392	0.1687	0.1984
D ↑	setup_rising to CP	0.0488	0.0536	0.0584	0.0658
TE ↓	hold_rising to CP	-0.0476	-0.0574	-0.0694	-0.0844
TE ↑	hold_rising to CP	-0.0512	-0.0579	-0.0676	-0.0830
TE ↓	setup_rising to CP	0.1176	0.1375	0.1639	0.1905
TE ↑	setup_rising to CP	0.2326	0.2739	0.3324	0.3935
TI ↓	hold_rising to CP	-0.1640	-0.1948	-0.2350	-0.2805
TI ↑	hold_rising to CP	-0.0534	-0.0596	-0.0707	-0.0845
TI ↓	setup_rising to CP	0.2280	0.2684	0.3234	0.3821
TI ↑	setup_rising to CP	0.0832	0.0893	0.1046	0.1151

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	3.416e-06	9.160e-12
X8_P4	1.242e-06	9.150e-12
X8_P10	8.043e-07	9.151e-12
X8_P16	7.896e-07	9.152e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

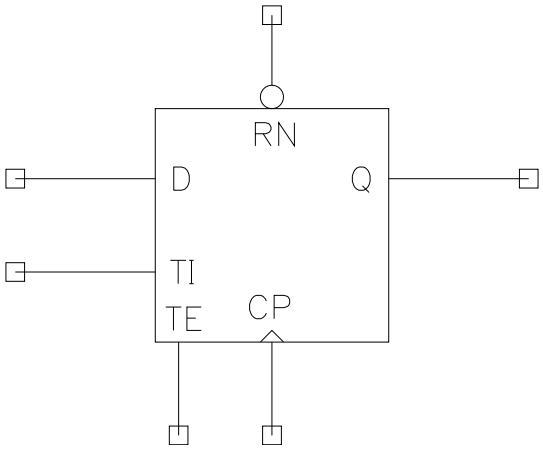
Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	9.054e-03	9.159e-03	9.339e-03	9.551e-03
Clock 100Mhz Data 25Mhz	1.368e-02	1.390e-02	1.429e-02	1.469e-02
Clock 100Mhz Data 50Mhz	1.832e-02	1.864e-02	1.924e-02	1.983e-02
Clock = 0 Data 100Mhz	8.573e-03	8.564e-03	8.582e-03	8.644e-03
Clock = 1 Data 100Mhz	6.998e-05	7.660e-05	8.000e-05	8.164e-05

SDFSYNCPRQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0008	0.0009	0.0009	0.0010
D	0.0006	0.0007	0.0007	0.0007
RN	0.0018	0.0019	0.0020	0.0022
TE	0.0010	0.0010	0.0010	0.0011
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
CP to Q ↓	0.1377	0.1579	1.6701	1.7910
CP to Q ↑	0.1359	0.1544	2.9322	3.2169
RN to Q ↓	0.1404	0.1624	1.6691	1.7916
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
CP to Q ↓	0.1900	0.2219	1.9662	2.1276
CP to Q ↑	0.1832	0.2117	3.6693	4.1206
RN to Q ↓	0.1980	0.2338	1.9686	2.1309

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1969	0.2306	0.2823	0.3364
CP ↑	min_pulse_width to CP	0.0780	0.0876	0.1068	0.1223
D ↓	hold_rising to CP	-0.0635	-0.0730	-0.0899	-0.1120
D ↑	hold_rising to CP	-0.0215	-0.0237	-0.0342	-0.0387
D ↓	setup_rising to CP	0.1175	0.1399	0.1639	0.1935
D ↑	setup_rising to CP	0.0488	0.0536	0.0584	0.0689
RN ↓	min_pulse_width to RN	0.1213	0.1360	0.1626	0.1919
RN ↑	recovery_rising to CP	0.0151	0.0150	0.0172	0.0202
RN ↑	removal_rising to CP	-0.0103	-0.0100	-0.0125	-0.0122
TE ↓	hold_rising to CP	-0.0507	-0.0574	-0.0694	-0.0844
TE ↑	hold_rising to CP	-0.0508	-0.0579	-0.0732	-0.0827
TE ↓	setup_rising to CP	0.1149	0.1347	0.1587	0.1887
TE ↑	setup_rising to CP	0.2277	0.2690	0.3275	0.3886
TI ↓	hold_rising to CP	-0.1591	-0.1849	-0.2302	-0.2741
TI ↑	hold_rising to CP	-0.0534	-0.0596	-0.0748	-0.0859
TI ↓	setup_rising to CP	0.2246	0.2636	0.3241	0.3785
TI ↑	setup_rising to CP	0.0845	0.0949	0.1059	0.1207

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	3.503e-06	1.036e-11
X8_P4	1.367e-06	1.036e-11
X8_P10	9.618e-07	1.035e-11
X8_P16	9.674e-07	1.034e-11

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	9.541e-03	9.709e-03	9.946e-03	1.021e-02

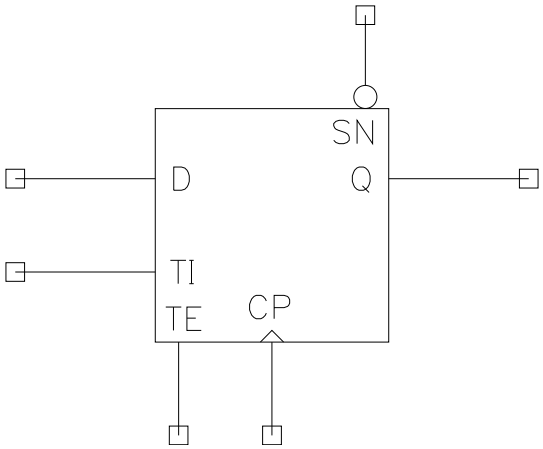
Clock 100Mhz Data 25Mhz	1.430e-02	1.458e-02	1.502e-02	1.546e-02
Clock 100Mhz Data 50Mhz	1.905e-02	1.945e-02	2.009e-02	2.071e-02
Clock = 0 Data 100Mhz	8.564e-03	8.591e-03	8.634e-03	8.712e-03
Clock = 1 Data 100Mhz	1.106e-04	1.260e-04	1.311e-04	1.323e-04

SDFSYNCPSQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0008	0.0009	0.0009	0.0010
D	0.0004	0.0005	0.0005	0.0005
SN	0.0016	0.0017	0.0018	0.0019
TE	0.0010	0.0010	0.0010	0.0011
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
CP to Q ↓	0.1036	0.1175	2.0840	2.2760
CP to Q ↑	0.1143	0.1297	3.1232	3.4270
SN to Q ↑	0.1408	0.1611	3.0255	3.3246
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
CP to Q ↓	0.1395	0.1613	2.5638	2.8334
CP to Q ↑	0.1540	0.1779	3.9240	4.4152
SN to Q ↑	0.1924	0.2235	3.7944	4.2646

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1891	0.2233	0.2720	0.3219
CP ↑	min_pulse_width to CP	0.0780	0.0876	0.1068	0.1224
D ↓	hold_rising to CP	-0.0504	-0.0631	-0.0777	-0.0948
D ↑	hold_rising to CP	-0.0188	-0.0237	-0.0286	-0.0360
D ↓	setup_rising to CP	0.1126	0.1297	0.1563	0.1837
D ↑	setup_rising to CP	0.0487	0.0540	0.0588	0.0658
SN ↓	min_pulse_width to SN	0.1348	0.1543	0.1809	0.2102
SN ↑	recovery_rising to CP	0.0036	0.0040	0.0009	0.0008
SN ↑	removal_rising to CP	0.0403	0.0452	0.0528	0.0596
TE ↓	hold_rising to CP	-0.0455	-0.0557	-0.0702	-0.0817
TE ↑	hold_rising to CP	-0.0533	-0.0579	-0.0732	-0.0827
TE ↓	setup_rising to CP	0.1075	0.1277	0.1515	0.1758
TE ↑	setup_rising to CP	0.2246	0.2641	0.3226	0.3788
TI ↓	hold_rising to CP	-0.1509	-0.1764	-0.2170	-0.2609
TI ↑	hold_rising to CP	-0.0547	-0.0609	-0.0763	-0.0853
TI ↓	setup_rising to CP	0.2190	0.2587	0.3192	0.3736
TI ↑	setup_rising to CP	0.0885	0.0942	0.1110	0.1220

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	3.540e-06	1.061e-11
X8_P4	1.403e-06	1.060e-11
X8_P10	9.579e-07	1.061e-11
X8_P16	9.549e-07	1.060e-11

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	9.344e-03	9.476e-03	9.690e-03	9.911e-03

Clock 100Mhz Data 25Mhz	1.372e-02	1.392e-02	1.430e-02	1.469e-02
Clock 100Mhz Data 50Mhz	1.809e-02	1.836e-02	1.891e-02	1.946e-02
Clock = 0 Data 100Mhz	8.738e-03	8.765e-03	8.836e-03	8.940e-03
Clock = 1 Data 100Mhz	7.146e-05	7.884e-05	7.895e-05	7.793e-05

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