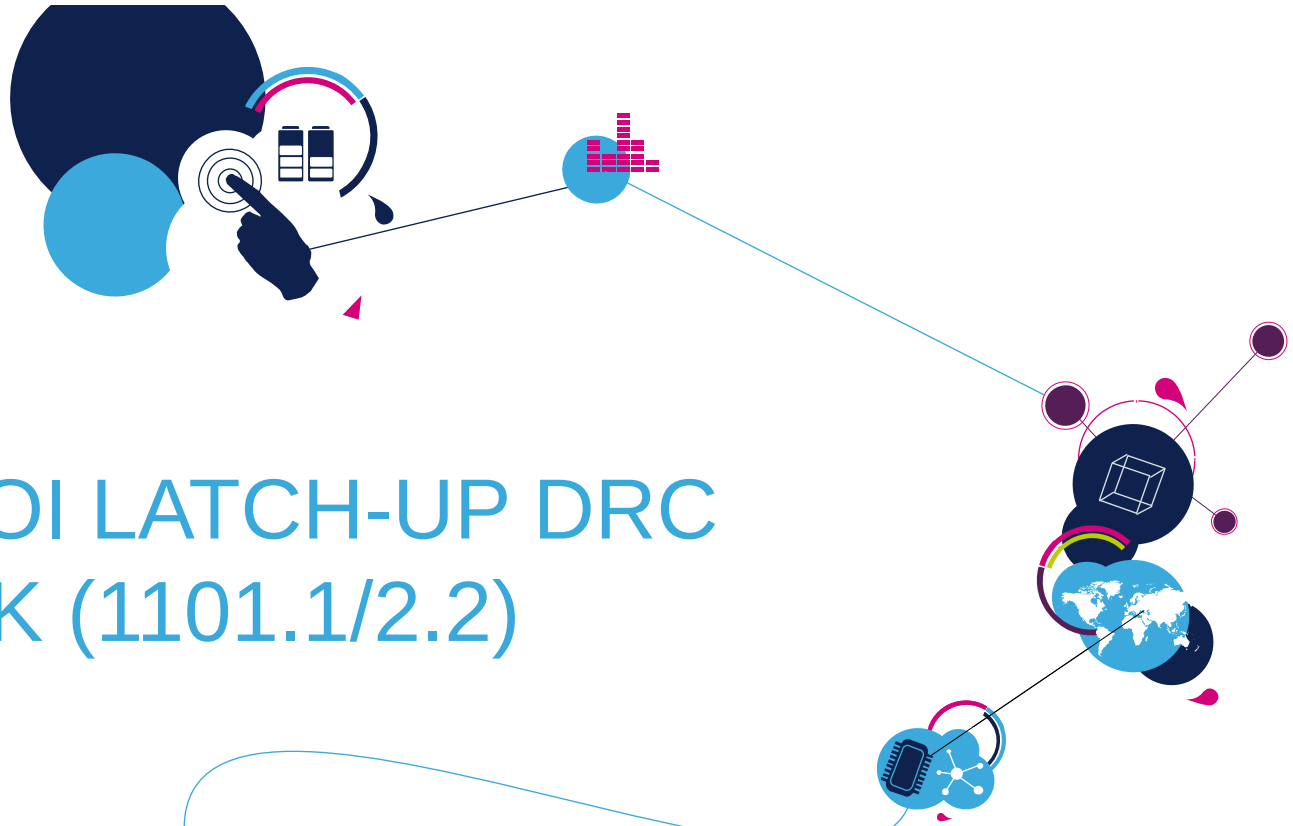

28LP/28FDSOI LATCH-UP DRC checks in PDK (1101.1/2.2)

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Crolles PDK

life.augmented

Program Management & Services / Process Design Kit

C28LP DRM requirements for LUP (1/3)

- LATCH UP rules are defined in cmos28 DRM. ADCS DOCUMENT 8307138, section
  - **7.7.3 LATCH-UP DESIGN RULES (LUP)**

- Following rules are checked by DRC :

Latch-Up Protection Design Rules for I/O Devices (DRC checked)			
LUP.W.1	RX width for all continuous PW strap or NW strap guard rings (with or without T3) must allow a good polarization of the entire guard ring (recommanded Raccess < 20 Ohm) and enable a good carrier collection, for all guard rings surrounding an Emitter		0.200
LUP.R.1	{RX N+ Diffusion [a] inside (PW less than 20um away from an Emitter)} [b] must be fully surrounded by a continuous PW strap in the same PW (guard ring) [c d]		
LUP.R.1.1	NW Emitter must be fully surrounded by a continuous PW strap in the same PW (guard ring) [c d]		
LUP.R.2	{RX P+ Diffusion [e] inside (NW less than 20um away from an Emitter)} [f] must be fully surrounded by a continuous NW strap in the same NW (guard ring) [g h]		
LUP.R.2.1	RW Emitter must be fully surrounded by a continuous NW strap in the same NW (NW guard ring) [g h].		
LUP.R.3	N+ SD Emitter and NW Emitter must be fully surrounded by a second guard ring (this second ring should be a NW guard ring) [g i]		
LUP.R.4	P+ SD Emitter and RW Emitter must be fully surrounded by a second guard ring (this second guard ring should be a PW strap) [c i]		
LUP.R.5	T3 under NW Emitter is prohibited.		
LUP.R.6	N+ SD of poly bounded diode and N+ SD of field oxide diode must be in an Isolated p-well fully surrounded by a continuous NW strap guard ring.		
LUP.R.7	P+ SD of poly bounded diode and P+ SD of field oxide diode must be fully surrounded by a continuous PW strap guard ring.		
LUP.R.8	P+ SD of ESDS device must be fully surrounded by a continuous NW strap guard ring.		

C28LP DRM requirements for LUP (2/3)

Latch-Up Protection Design Rules for I/O Devices (DRC checked)			
LUP.D.4	"Hot" NW distance to NWE for 1V [a]		1.000
LUP.D.5	"Hot" NW distance to NWE for 2.5V [a]		2.000
LUP.D.6	"Hot" NW distance to NWE for 3.3V [a]		2.500
LUP.D.7	"Hot" NW distance to NWE for 5V [a]		6.000
LUP.D.8	"Hot" NW distance to NWE for 7V [a]		12.000
LUP.D.9	"Hot" NW distance to RX N+ Diffusion for 1V [a]		1.000
LUP.D.10	N+ SD Emitter distance to NWE [b] for 1V [a]		1.000
LUP.D.11	"Hot" NW distance to RX N+ Diffusion for 2.5V [a]		2.000
LUP.D.12	N+ SD Emitter distance to NWE [b] for 2.5V [a]		2.000
LUP.D.13	"Hot" NW distance to RX N+ Diffusion for 3.3V [a]		2.500
LUP.D.14	N+ SD Emitter distance to NWE [b] for 3.3V [a]		2.500
LUP.D.15	"Hot" NW distance to RX N+ Diffusion for 5V [a]		6.000
LUP.D.16	N+ SD Emitter distance to NWE [b] for 5V [a]		6.000
LUP.D.17	"Hot" NW distance to RX N+ Diffusion for 7V [a]		12.000
LUP.D.18	N+ SD Emitter distance to NWE [b] for 7V [a]		12.000
LUP.D.19	"Hot" RW distance to PW		1.200
LUP.D.20	"Hot" PW distance to Isolated p-well		1.200

C28LP DRM requirements for LUP (3/3)

- Highlight of the LUP rules:

1. DRM defines Latch-up emitter areas in the design:
   - S/D drain RX connected to a pad
   - NW / RW well strap connected do a pad

2. DRM defines rules to protect the design from those latchup emitters:
   - Protection guardring for emitters
   - Protection guardring for devices which are less than 20µm from emitters

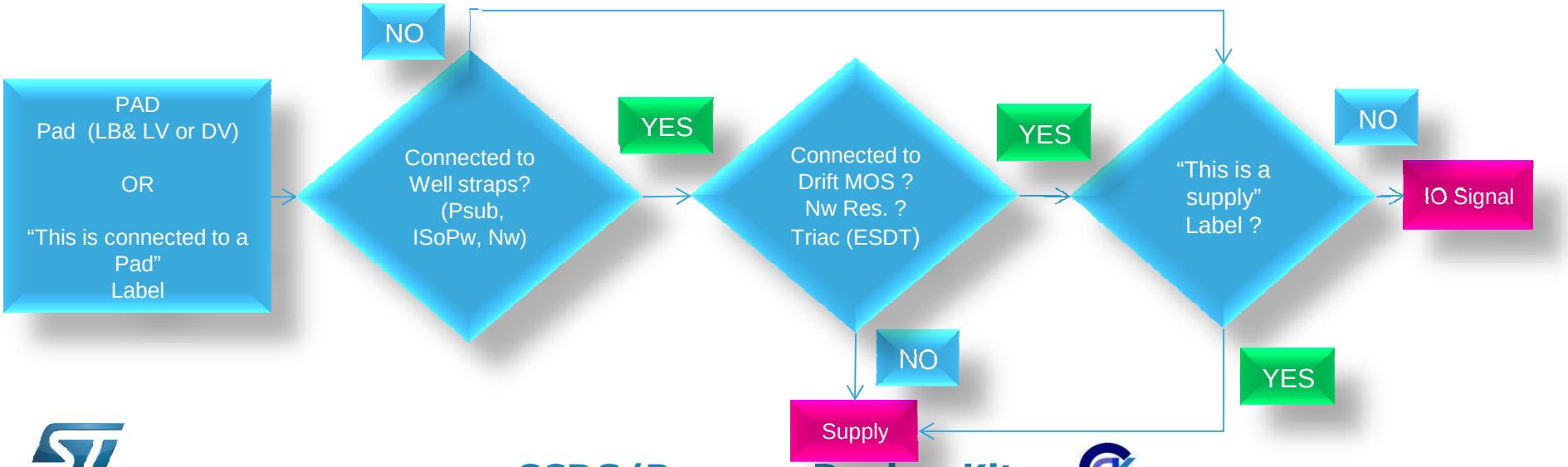
- Latch up rules applied only on signal Pads.
- Supply pads do not have to meet such latch up rules

C28LP LUP Check in DK 1101.1: Automatic Power Supplies recognition

- Problem Statement: Issue with previous LUP-check in 28nm DRM/DK which may miss some I/O Signals contacting directly the following devices:
  - Nwell resistance
  - Drift MOS
  - Triac Device (ESDT)

- New CAD implementation from 28LP 1101.1 + 28FDSOI 2.2 PDKs 

- Compulsory pre-requisite s:
  - "This is connected to a Pad" and "This is a supply" labels must be recognized in all the hierarchy, whatever the hierarchical level => DRC coding.
  - "This is connected to a Pad" must not be prioritary => DRC coding



C28LP LUP Check in previous DK : Limitation

- In previous 28LP DK (earlier 1101.1), LUP check is very dependent on:
  a. List of labels « *this is a supply* ». If one is forgotten, thousands of errors can be highlighted.
  b. LVS clean design: if there is a short between a supply and a signal, all nets are considered as signal, so thousands of errors can be highlighted.

- Aim is to converge to have a number of errors acceptable to debug:
  - Not all the design highlighted
  - Only some areas are highlighted

- If it is not the case, designers must work on « *this is a supply list* » label or to correct short. Example of errors:
  - Vsense (label for probe) not in the list
  - 2 bumps of supply connected together, with only one label on one pad.

C28LP LUP Check : New and Current DRC implementation

- In 28LP/32LP/28FDSOI PDK releases (>= 1101.1/2.2), standard supply is recognized thanks to DRC deck. So, no need anymore of the list of « this is a supply ».
- So only custom supplies should raise LUP errors
- With this new methodology, LUP-debug is easier and has to be done directly with LUP expert

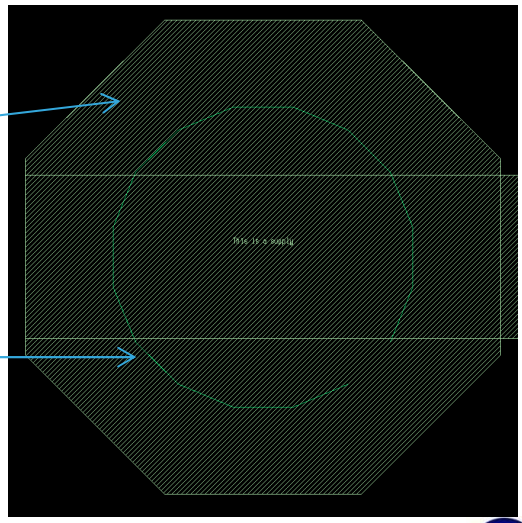
LATCH-UP CAD-Guidelines: Pads definition

- In TRD/DK-DRC, PAD check is defined as an overlap of LV layer and LB layer (as shown in below snapshot)

- To avoid false DRC errors when an active area is connected to a supply pad, a specific label called "*This is a supply*" must be drawn on all selected pads :
  - "**LB drawing**" layer has to be used for label drawing
  - Label must be added, ***by hand***, and **at SoC/top level** design
  - Label must be placed at the intersection of LB and LV layers. As shown on the picture otherwise label is not taken into account (not seen by DRC)

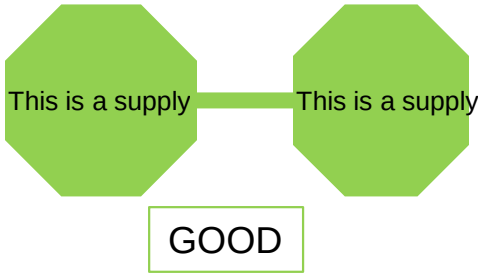
LB drawing

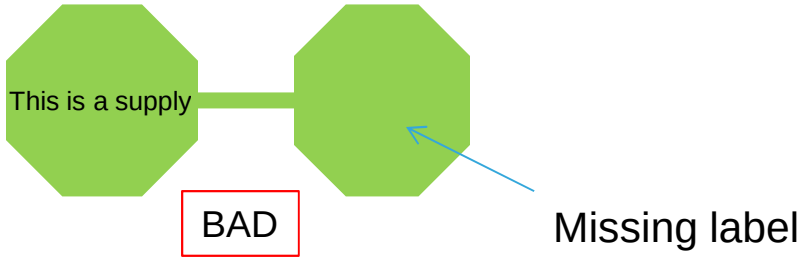
LV drawing



LATCH-UP CAD-Guidelines: Errors Debug (1/3)

- 1st Step -> To double check the labels "*This is a supply*" consistency :
  - All supply Pads must have the label "*This is a supply*" (at top level design hierarchy)
  - If 2 pads are connected together, a label is needed on each single pad





  - Label must be in « LB drawing » layer

  - If user has sense pads (not a design usage) which are shorted to supply pads, the label must be added on sense pads.

LATCH-UP CAD-Guidelines: Errors Debug (2/3)

- 2nd step -> to get an LVS clean database

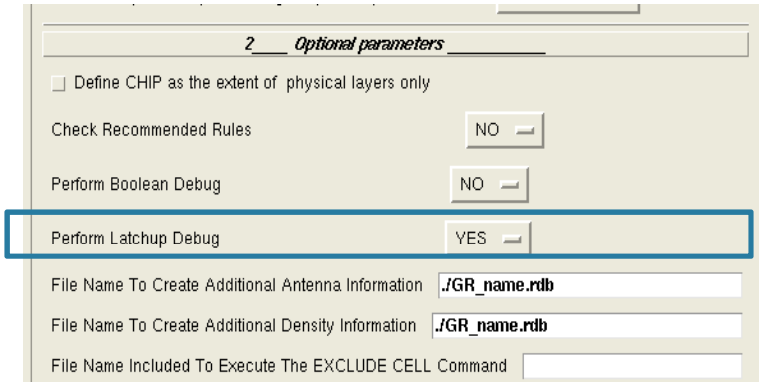
- As the DRC is checking the connectivity from the emitter to the pads, LVS should be good ‘by construction’

- If there is a short between one signal pads and one supply pads, DRC will consider both pads as not supply pads, and DRC will check Latch up rules on active areas.
  - So false errors should be raised

LATCH-UP CAD-Guidelines: Errors Debug (3/3)

- DRC deck has been developed to ease such a debugging phase:

- In *PDK/calibrerun* verification utility, there is a switch to help LUP debug



  - Highlight of emitters, 20µm area around emitters in C28LP.
  - But, there is no automatic way to highlight a net from the emitter to the pad responsible of the LUP failure.
  - **Debug rules flow is efficient only if labels « *this is a supply* » are correctly added on supply pads (top-level) and if the LVS is already clean.**