C28SOI_SC_12_PR_LL User Manual

12 track Standard Cell Library comprising Place and Route cells

Overview

Features

- 12-track Standard Cell library
- The library consists of 66 cells
- Based on low power low V_t transistors

Applications

- These cells are used for Place and Route.

Library Architecture

In C28SOI_SC_12_PR_LL library, all pins are located on the vertical and horizontal pin grids. Although only some Place and Route tools require all pins on grids, most tools work more efficiently with all pins on grids.

Figure 1. Layout for Single Height Cell

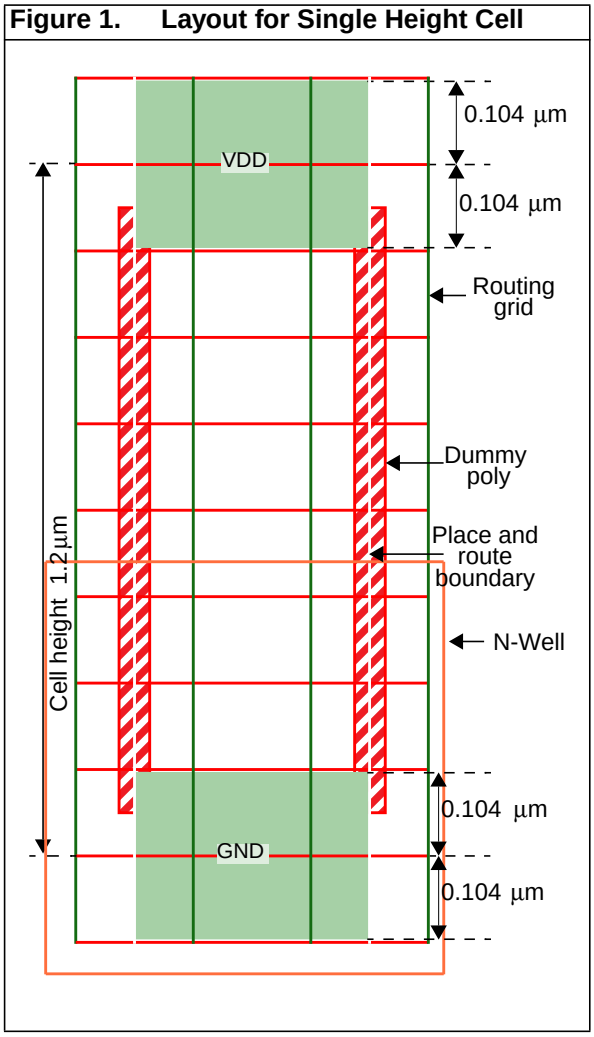
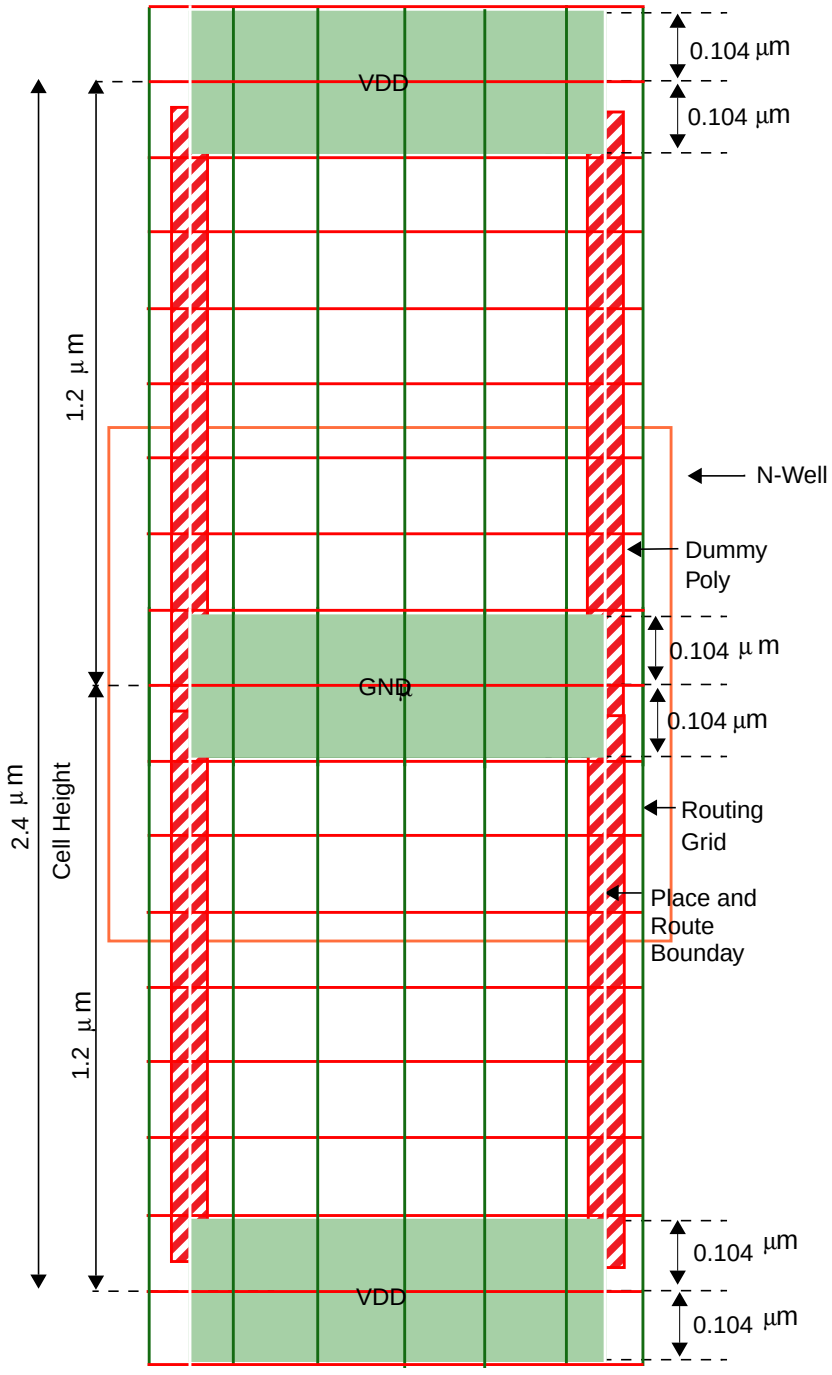


Table 1. Physical Specifications

Parameter	Measurement (µ m)
Drawn gate length	0.03
Layout grid	0.001
Vertical pin grid	0.10
Horizontal grid	0.136
Cell power and ground rail width	0.208

Figure 2. Layout for Double Height Cell with VDD Rail at Bottom



1 Quick References

	*This document is compatible for viewing with acroread 7.0 and higher versions. If opened with a lower version of acroread, there might be some color display problem.*

	*Please refer to the Naming Convention Document available in the design package for details about cell names.*

2 Functional Specifications

2.1 Cell List

C28SOI_SC_12_PR_LL library consists of the following cells.

Table 2. Cell List

Cell Name	Number of Cells
ANTPROT	2
DECAP/PDECAP	12
FILLERFLPCHKAE	6
FILLERCELL/FILLERPFOP	7
FILLERSNPW/FILLERNPW	2
ANTPROTGVFILLERNPW	2
ANTPROTFILLERSNPW	3
ANTPROTGVFILLERSNPW	3
TOH/TOL	2
FILLERCEND	27

3 Library Contents

This section describes the contents of the library.

3.1 Library Description by Family

This section details the library contents by presenting all families of cells.

3.1.1 Antenna Diodes

This family of cells is completely compliant with CMOS028_FDSOI process.

The ANTPROT3 cell is a 3-tracks cell with MINUS M1 pin. The library contains the following ANTPROT3 cell:

- C12T28SOI_LL_ANTPROT3

The ANTPROT4 cell is 4-tracks cell with MINUS M1 pin. The library contains the following ANTPROT4 cell:

- C12T28SOI_LL_ANTPROT4

Caution: C12T28SOI_LL_ANTPROT3 is not standalone DRC clean, had to keep other cell on surroundings. To overcome this issue, there is another ANTPROT cell "C12T28SOI_LL_ANTPROT4" which is standalone DRC clean for fully isolated Designs

3.2 Supply Decoupling

Supply Decoupling cells exist for users, who want to discharge power nets.

Following are decoupling cells with GO1 transistors:

- C12T28SOI_LLF_DECAPXT4
- C12T28SOI_LLF_DECAPXT8

Following are decoupling cells with large gate length (>30 nm) with GO1 transistors having only PMOS:

- C12T28SOI_LLL_PDECAP16
- C12T28SOI_LLL_PDECAP32
- C12T28SOI_LLL_PDECAP64

Following are decoupling cells with large gate length (>30 nm) with GO1 transistors having NMOS and PMOS

- C12T28SOI_LLL_DECAPXT4
- C12T28SOI_LLL_DECAPXT8

Following are decoupling cells with GO2 transistors:

- C12T28SOI_LLEGLV_DECAPXT9
- C12T28SOI_LLEGLV_DECAPXT12
- C12T28SOI_LLEGLV_DECAPXT16

- C12T28SOI_LLEGLV_DECAPXT32
- C12T28SOI_LLEGLV_DECAPXT64

3.3 TIE High/Low Cells

Following are Tie high and Tie low cells:

- C12T28SOI_LL_TOHX8
- C12T28SOI_LL_TOLX8

3.4 Filler Cells with Pattern Fill

3.4.1 Filler Cells with Pattern Fill for PC

This family of cells is completely compliant with CMOS028_FDSOI process. Poly rectangles (PolyOnBoundary) are present to fill the poly density requirement. The following is the filler cell with pattern fill for PC:

- C12T28SOI_LL_FILLERCELL1

3.4.2 Filler Cells with Pattern Fill for PC and RX

This family of cells is completely compliant with CMOS028_FDSOI process. Polyrectangles are present to fill the PC density requirement. RX rectangles are present to satisfy the minimum RX density. The following are the filler cells with pattern fill for PC and RX:

- C12T28SOI_LL_FILLERPFOP2
- C12T28SOI_LL_FILLERPFOP4
- C12T28SOI_LL_FILLERPFOP8
- C12T28SOI_LL_FILLERPFOP16
- C12T28SOI_LL_FILLERPFOP32
- C12T28SOI_LL_FILLERPFOP64

FILLERPFOP* cells have to be used at the top and bottom of the design.

Above cells have an endcap of 44nm and are standalone DRC clean and will not highlight the aggressive poly EndCap DRC violations at initial floorplan level.

For the above drawback we have added below cells :

- C12T28SOI_LL_FILLERFLPCHKAE16
- C12T28SOI_LL_FILLERFLPCHKAE2
- C12T28SOI_LL_FILLERFLPCHKAE32
- C12T28SOI_LL_FILLERFLPCHKAE4
- C12T28SOI_LL_FILLERFLPCHKAE64
- C12T28SOI_LL_FILLERFLPCHKAE8

hese FILLERFLPCHKAE* cells when used during initial floor planning verification will represent real scenario of poly endcap(PCnes), helping designer to take corrective measure

in the initial phase itself. These cells have an endcap of 37nm. Also These specific cells have intentional DRC error so that it can be checked that it does not remain in final GDS.

3.5 Filler Tie Cells with RX Well-straps with Pattern Fill for PC

The maximum distance from any point inside source/drain RX area to the nearest RX of a well tie within the same NW or PW is defined in DRM to ensure the substrate polarization. RX well-straps cells are necessary to satisfy this rule because there is no substrate strap in Standard cells.

3.5.1 Non-split Filler Cells

This family of cells is completely compliant with CMOS028_FDSOI process. The FILLERNPW4 cells can be used to boost densities for RX and to improve the substrate polarization. The following are the filler cells with N-well and P-well straps respectively connected to abutting rails gnd and vdd:

- C12T28SOI_LL_FILLERNPW4

3.5.2 Split Filler Cells

This family of cells is completely compliant with CMOS028_FDSOI process, PC wires are present to fill the PO density requirement. The following are the filler cells with N-well and P-well straps respectively connected to internal pins, gnds and vdds, and with pattern fill for PC:

- C12T28SOI_LL_FILLERSNPW4

3.5.3 Non-split Filler Cells with Antenna Diode

This family of cells is completely compliant with CMOS028_FDSOI process, PC wires are present to fill the PO density requirement. The following are the filler cells with N-well and P-well straps, i.e. gnds and vdds internally tied to gnd, and with pattern fill for PC. An ANTENNA diode protection is connected between vdd and gnd to prevent from ANTENNA phenomena at process level.

- C12T28SOI_LL_ANTPROTGVFILLERNPW6
- C12T28SOI_LL_ANTPROTGVFILLERNPW8

3.5.4 Split Filler Cells with Antenna Diode

This family of cells is completely compliant with CMOS028_FDSOI process, PC wires are present to fill the PO density requirement. The following are the filler cells with N-well and P-well straps respectively connected to internal pins, gnds and vdds, and with pattern fill for PC.

- C12T28SOI_LL_ANTPROTFILLERSNPW6
- C12T28SOI_LL_ANTPROTFILLERSNPW7
- C12T28SOI_LL_ANTPROTFILLERSNPW8
- C12T28SOI_LL_ANTPROTGVFILLERSNPW6
- C12T28SOI_LL_ANTPROTGVFILLERSNPW7
- C12T28SOI_LL_ANTPROTGVFILLERSNPW8

In cells C12T28SOI_LL_ANTPROTFILLERSNPW/6/7/8, An ANTENNA diode protection is provided between gnd and gnds.

In cells C12T28SOI_LL_ANTPROTGVFILLERSNPW6/7/8, An ANTENNA diode protection is provided between gnd-gnds and vdd-vdds both in to prevent from ANTENNA phenomena at process level.

Caution: As ANTPROTFILLERSNPW* and ANTPROTGVFILLERSNPW*, both to be used for LVT FBB domains, so for deciding which one to use should be based on below remarks -

C12T28SOI_LL_ANTPROTGVFILLERSNPW* :

- Not to be used for extreme FBB domains as there is diode between vdd/vdds which may cause breakdown (Vb>2.6V)risk when used at Extreme FBB.

C12T28SOI_LL_ANTPROTFILLERSNPW* :

- To be used in case of very high difference of potential between vdd & vdds i.e., for LVT Extreme FBB domains and where antenna ratio are not violated at design level. As in this cell, there is no diode between vdd-vdds, so no risk of huge potential difference in case of LVT Extreme FBB domains.

3.6 Filler Cell to Avoid the Aggressive end Capacitance Violation

They will be automatically inserted above last and first rows of all Standard Cell block to prevent DRC violation of Aggressive PC Endcap. Small Poly rectangles are present to enlarge PC endcap at the top and/or at the bottom of first and last line.

- C12T28SOI_LVTFILLERPCENDB1
- C12T28SOI_LVTFILLERPCENDB16
- C12T28SOI_LVTFILLERPCENDB2
- C12T28SOI_LVTFILLERPCENDB32
- C12T28SOI_LVTFILLERPCENDB4
- C12T28SOI_LVTFILLERPCENDB64
- C12T28SOI_LVTFILLERPCENDB8
- C12T28SOI_LVTFILLERPCENDBL1
- C12T28SOI_LVTFILLERPCENDBR1
- C12T28SOI_LVTFILLERPCENDT1
- C12T28SOI_LVTFILLERPCENDT16
- C12T28SOI_LVTFILLERPCENDT2
- C12T28SOI_LVTFILLERPCENDT32
- C12T28SOI_LVTFILLERPCENDT4
- C12T28SOI_LVTFILLERPCENDT64
- C12T28SOI_LVTFILLERPCENDT8
- C12T28SOI_LVTFILLERPCENDTB1
- C12T28SOI_LVTFILLERPCENDTB16

- C12T28SOI_LVTFILLERPCENDTB2
- C12T28SOI_LVTFILLERPCENDTB32
- C12T28SOI_LVTFILLERPCENDTB4
- C12T28SOI_LVTFILLERPCENDTB64
- C12T28SOI_LVTFILLERPCENDTB8
- C12T28SOI_LVTFILLERPCENDTBL1
- C12T28SOI_LVTFILLERPCENDTBR1
- C12T28SOI_LVTFILLERPCENDTL1
- C12T28SOI_LVTFILLERPCENDTR1

4 Supported Flow Strategies

Different options are available for the process, substrate connection, and V_t implant. For each parameter, the supported options are:

- Process options
  - Single CMOS028_FDSOI process
- Substrate connection options
  - No-split power with substrate straps connected to vdd and gnd
  - Split power with substrate straps connected to vdds and gnds
- V_t implants
  - Single V_t implant: only LVT

4.1 Single Process and Single V_t Implant

To illustrate the case of only one process (for example,CMOS028_FDSOI process) and only one V_t (for example, LVT implant), a possible strategy is discussed in further sections.

4.2 Gaps Filling

- C12T28SOI_LL_FILLERCELL1/FILLERPFOP2/4/8/16/32/64/FILLERFLPCHKAE2/4/8/16/32/64

4.3 Antenna Diodes

- C12T28SOI_LL_ANTPROT3/C12T28SOI_LL_ANTPROT4

4.4 Non-split Power Substrate Straps (OD Well-straps Connected to vdd/gnd)

- C12T28SOI_LL_FILLERNPW4

4.5 Split Power Substrate Straps (OD Well-straps Connected to vdds/gnds)

- C12T28SOI_LL_FILLERSNPW4

4.6 Split Power Substrate Straps (OD Well-straps Connected to vdds/gnds) with Antenna protection diode

- C12T28SOI_LL_ANTPROTFILLERSNPW6/7/8

4.7 Split Power Substrate Straps (OD Well-straps connected to vdds and gnds for Pwell and Nwell respectively) with Antenna Protection Diode

- C12T28SOI_LL_ANTPROTGVFILLERSNPW8
- C12T28SOI_LL_ANTPROTGVFILLERSNPW7
- C12T28SOI_LL_ANTPROTGVFILLERSNPW6

4.8 Non-split Power Substrate Straps (OD Well-straps connected to gnd) with Antenna Protection Diode

- C12T28SOI_LL_ANTPROTGVFILLERNPW6
- C12T28SOI_LL_ANTPROTGVFILLERNPW8

5 Contact Information

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