

1. Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library Name	C28SOI.IO_EXT_ANAF_ANA_EG
Library Version	7.1
Library Type	IO Cells
Technology	CMOS028_FDSOI
DK Version	

1.2 Impact of Product Release

For latest information, please refer to LYS (<http://col2.cro.st.com/libyield>).

1.3 Related Documentation

- C28SOI.IO_EXT_ANAF_ANA_EG User Manual
- C28SOI.IO_EXT_ANAF_ANA_EG Release Notes and Known Problems and Solutions
- C28SOI.IO_EXT_ANAF_ANA_EG_ff28_0.90V_125C_2ey_ss28_0.90V_m40C_2ey_7.0 DataBook
- C28SOI.IO_EXT_ANAF_ANA_EG_ff28_1.10V_m40C_tt28_1.00V_25C_ss28_0.90V_125C_7.0 DataBook
- C28SOI.IO_EXT_ANAF_ANA_EG_ff28_0.90V_m40C_2ey_ss28_0.90V_125C_2ey_7.0 DataBook
- C28SOI.IO_EXT_ANAF_ANA_EG_ff28_1.10V_125C_ss28_0.90V_m40C_7.0 DataBook
- IOLIB_Verilog_Common_Known_Problem_Solution_7.0 DataBook

2. Changes with respect to all Previous Versions

2.1 Changes in Version 7.1-01 w.r.t Version 7.1-00

- A. SYNOPSYS FRAM view fixed.
- B. LEF updated for CLASS attribute for special purpose fillers.

2.2 Changes in Version 7.1-00 w.r.t Version 7.0

Final MAT10 Package aligned with latest BE (7.1-BE-01)

2.3 Changes in Version 7.0 w.r.t Version 6.1

Characterization has been done with new spice models

- A. This is the Final release
- B. Major content of packages are
 - (1) HDL Models:
 - (a) Verilog (.v) is compliance with power aware flow
 - (b) Emulator (_emul.v), Tetramax(_tmax.v), Power Verilog (.allpins.v), MENTOR
 - (2) STF View is compliance with UPF flow
 - (3) Physical Views (CADENCE LEF ,Layout , Schematic, CDL, GDS, SPI, Abstract, Voltus)
 - (4) Other views(ADMS, NOVAS, CPF etc.)
 - (5) IODA Model.

Align with new DK

2.4 Changes in Version 6.1 w.r.t Version 6.0

- A. This is the Final release
- B. Updates in this version are -
 - (1) Physical Views (Layout ,LEF ,Schematic, CDL, GDS, SPI, Abstract)

Updated FILLCELL_1GRID_EXT_ANA_CL_LIN and FILLCELL_1GRID_EXT_ANA_FC_LIN for vdde/gnde pins in IB layer at top

2.5 Version 6.0

A. This is the Final release.

B. This package contains Verilog, libs, Cadence LEF, SIGNOFF LEF, SIP, SIGNOFF GDS, CDL and SYNOPSIS LAYOUT & FRAM.

(1) Verilog Models:

I. Verilog (.v) model : Compliance with power aware flow.

II. In VERILOG Pin name, Pin direction and functionality is aligned with Usermanual .

(2) Liberty NLDM (STF) :

I. STF view is compliance with UPF flow .

1. First BE release

3. Known Problems and Solutions of this release



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DRC errors

- cell level



EMET ERRORS, Ignorable, can be corrected on chip level during EMET structure development

EMET.DEN.1
EMET.DEN.10
EMET.DEN.11
EMET.DEN.12
EMET.DEN.2
EMET.DEN.3
EMET.DEN.4
EMET.DEN.5
EMET.DEN.6
EMET.DEN.7
EMET.DEN.8
EMET.DEN.9



Minimum Density Errors, Ignorable, can be corrected on chip level

RX.DEN.1
M1.DEN.1
M2.DEN.1
M3.DEN.1

M4.DEN.1**RX.DEN.8 : only on CORNERCELL_EXT_ANA_FC_LIN****M1.DEN.8 : CORNERCELL_EXT_ANA_FC_LIN****M2.DEN.8 : Only on FILLCELL_FEEDTHROUGH_EXT_ANA_CL_LIN****M3.DEN.8: FILLCELL_FEEDTHROUGH_EXT_ANA_CL_LIN****M4.DEN.8: FILLCELL_FEEDTHROUGH_EXT_ANA_CL_LIN****GR8x00_IA: All 1GRID fillers****GR8x00_IB: All 1GRID fillers****HYBRID.W.1 :All 1GRID fillers****VV.DEN.2 : All IO_20UM_* topcells only****LVS errors****- cell level****SOFTCHECK: stamping conflict Normal error on cells that cut esdsub node, to be ignore. Impacted cells**

**FILLCUTCELL_ALL_EXT_ANA_FC_LIN,
 FILLCELL_STEP_BTBTB_EXT_ANAF_TO_CSF_FC_LIN,
 FILLCELL_STEP_BTBTB_EXT_ANAF_TO_CSF_FC_2ROWS,
 FILLCELL_STEP_EXT_ANAF_TO_CSF_FC_2ROWS,
 FILLCELL_STEP_EXT_ANAF_TO_CSF_FC_LIN**

**ERC errors****ERC1a: Ignorable, can be corrected by defining the correct ground in lvs customization file**

4. Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (<http://col2.cro.st.com/helpdesk>).

Non-ST users, please contact the respective Customer Support.



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