HDL_EMUL

Emulation Model - CMOS IOs

Application Notes

July 2010

Version 1.1

Highlights

- Emulation model for MAT10 packages of IOs
- Defines all internal components of ST

Revision History

Date	Document Version	Comments
4-October-2007	1.0	First release
21-July-2010	1.1	ST_KEEPER_EN functionality added

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Table of Contents

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1. General Description

This document details the definitions of all internal components of ST that are used in emulation models provided in MAT10 packages in IO libraries. This enables the user to map these pull up/pull down devices with components from a particular technology library.

2. Functional Specification - ST Pull Primitives

The following table lists the primitives defined in the HDL_EMUL views provided in the IO library packages.

Table 1: ST Pull Primitive List

ST Pull Primitive Name	Description
ST_PULLUP	Pull up component with NO control pin
ST_PULLDOWN	Pull down component with NO control pin
ST_PULLUP_EN	Pull up component with ACTIVE LOW enable
ST_PULLDOWN_EN	Pull down component with ACTIVE LOW enable
ST_PULLUP_EN_AH	Pull up component with ACTIVE HIGH enable
ST_PULLDOWN_EN_AH	Pull down component with ACTIVE HIGH enable

2.1 ST_PULLUP

2.1.1 Functional Description

This primitive is used to model a pull up circuit.

2.1.2 Module Declaration

- ST_PULLUP (pin name)
- ST_PULLUP (IO)

where,

IO = output pin (for this primitive).

2.1.3 Primitive Description

Table 2: Primitive Description

IO
pull1

2.2 ST_PULLDOWN

2.2.1 Functional Description

This primitive is used to model a pull down circuit.

2.2.2 Module Declaration

- ST_PULLDOWN (pin name)
- ST_PULLDOWN (IO)

where,

IO = output pin (for this primitive).

2.2.3 Primitive Description

Table 3: Primitive Description

IO
pull0

2.3 ST_PULLUP_EN

2.3.1 Functional Description

This primitive is used to model a pull up circuit with active low enable (PMOS).

2.3.2 Module Declaration

- ST_PULLUP_EN (pin name)
- ST_PULLUP_EN (IO, EN)

where,

IO = output pin (for this primitive).

EN = input pin (enable pin**).**

2.3.3 Primitive Description

Table 4: Primitive Description

EN	IO
1	Z
0	pull1

2.4 ST_PULLDOWN_EN

2.4.1 Functional Description

This primitive is used to model a pull down circuit with active low enable (PMOS).

2.4.2 Module Declaration

- ST_PULLDOWN_EN (pin name)
- ST_PULLDOWN_EN (IO, EN)

where,

IO = output pin (for this primitive).

EN = input pin (enable pin**).**

2.4.3 Primitive Description

Table 5: Primitive Description

EN	IO
1	Z
0	pull0

2.5 ST_PULLUP_EN_AH

2.5.1 Functional Description

This primitive is used to model a pull up circuit with active high enable (NMOS).

2.5.2 Module Declaration

- ST_PULLUP_EN_AH (pin name)
- ST_PULLUP_EN_AH (IO, EN)

where,

IO = output pin (for this primitive).

EN = input pin (enable pin).

2.5.3 Primitive Description

Table 6: Primitive Description

EN	IO
0	Z
1	pull1

2.6 ST_PULLDOWN_EN_AH

2.6.1 Functional Description

This primitive is used to model a pull down circuit with active high enable (NMOS).

2.6.2 Module Declaration

- ST_PULLDOWN_EN_AH (pin name)
- ST_PULLDOWN_EN_AH (IO, EN)

where,

IO = output pin (for this primitive).

EN = input pin (enable pin).

2.6.3 Primitive Description

Table 7: Primitive Description

EN	IO
0	Z
1	pull0

2.7 ST_KEEPER_EN

2.7.1 Functional Description

This primitive is used to model a bus keeper circuit with active low enable.

It keeps the previous value of IO port with week strength when EN is low and it is transparent (IO will have current vaue) when EN is high.

2.7.2 Module Declaration

- ST_KEEPER_EN (pin name)
- ST_KEEPER_EN (IO, EN)

where,

IO = output pin (for this primitive).

EN = input pin (enable pin).

2.7.3 Primitive Description

Table 8: Primitive Description

EN	IO
0	IO keeps the previous value with week strength.
1	IO is transparent

3. Special Cases

3.1 Analog Cells

In cells, such as HV* and ANA* with two or more INOUT ports, the HDL_EMUL model is unidirectional. This model should not be used for functional verification. The emulation flow uses the synthesized model. The HDL_EMUL model present in package can be synthesized. The synthesized netlist from this model is functionally correct and complete (bidirectional behavior).

4. Contact Information

For more information about this document, please write to **HELPDESK.**