C28SOI_SC_12_CLK_LL

User Manual

12 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

Overview

Features

- The C28SOI_SC_12_CLK_LL Standard Cell library contains 328 cells.

Application

- Design needs in CMOS28FDSOI platform IPs.

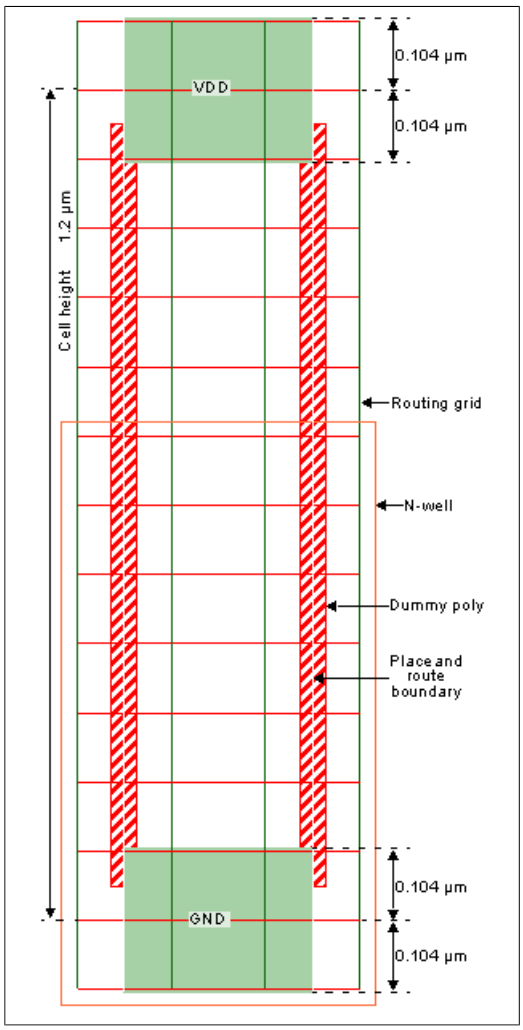
Library Architecture

This section illustrates the architecture used for C28SOI_SC_12_CLK_LL Standard Cell library.

Following table shows the Physical Specifications for this library.

Physical Specifications	
Parameter	**Measurement**
Drawn Gate Length (um)	0.030
Layout Grid (um)	0.001
Vertical Pin Grid (um)	0.1
Horizontal Pin Grid (um)	0.136
Cell Power and Ground Rail Width (um)	0.208

Figure 1: Cell Architecture



1. Quick References

	Please refer to the Naming Convention Document available in Design Package for more details regarding cell names.

	Please refer to the Standard Cells Reference Manual available in Design Package for more details on library specific information.

2. Functional Specification

2.1. Cell Info

2.1.1. LL(LP Low Vt)

2.1.1.1. Poly Bias With 0nm

Table 2: Cell List

Cell Type	Drive Strength	Cell Description
C12T28SOIDV_LL_CNMUX41	X17, X27	4:1 non-inverting Multiplexer for Clock network,Vdd rail at the bottom of the cell
C12T28SOI_LL_DLYHFM8	X15, X54, X7	Delay Cell for Hold Time Fixing
C12T28SOI_LLP_CNHLS	X15, X22, X29, X36, X51, X58, X71, X7, X93	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C12T28SOI_LL_CNAND2	X15, X20, X33	2 input AND for Clock network
C12T28SOI_LL_CNAND3	X17, X25, X33	3 input AND for Clock network
C12T28SOIDV_LL_SDFSYNCPQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only,Vdd rail at the bottom of the cell
C12T28SOIDV_LL_CNGFMUX21	X15, X30	2:1 Glitch-free MUX for Clock network,Vdd rail at the bottom of the cell
C12T28SOI_LL_CNOR2	X15, X20, X33, X37	2 input OR for Clock network
C12T28SOI_LL_CNMUX21	X17, X33	2:1 non-inverting Multiplexer for Clock network
C12T28SOI_LL_CNOR3	X14, X20	3 input OR for Clock network
C12T28SOI_LL_CNOR4	X20, X27	4 input OR for Clock network
C12T28SOI_LL_CNSDFPRQT	X15	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network
C12T28SOI_LL_CNNOR2A	X15, X27	2 input NOR with A input Inverted for Clock network
C12T28SOIDV_LL_SDFSYNCPRQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only,Vdd rail at the bottom of the cell
C12T28SOI_LLPHP_CNHLS	X29, X36, X44, X51, X58, X71, X86	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C12T28SOI_LL_CNSDFPSQT	X15	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having

Cell Type	Drive Strength	Cell Description
		non-inverted output Q and non-inverted test output TQ for Clock network
C12T28SOI_LL_CNNAND2	X15, X33	2 input NAND for Clock network
C12T28SOI_LL_CNBF	X133, X15, X22, X30, X38, X44, X4, X52, X59, X70, X7, X94	Buffer with Balanced rise and fall delays for Clock network
C12T28SOI_LL_CNAO12	X33	2 input AND into 2 input OR
C12T28SOI_LL_CNNAND2A	X17, X27	2 input NAND with A input inverted for Clock network
C12T28SOI_LL_CNNOR2	X14, X33	2 input NOR for Clock network
C12T28SOIDV_LL_SDFSYNCPSQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only,Vdd rail at the bottom of the cell
C12T28SOI_LL_CNLDLRQ	X33	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LL_DLYHFM4	X15, X7	Delay Cell for Hold Time Fixing
C12T28SOI_LL_CNXOR2	X16, X27	2 input Exclusive OR for Clock network
C12T28SOI_LL_CNIV	X133, X16, X23, X31, X39, X47, X55, X5, X61, X70, X8, X94	Inverter with Balanced rise and fall delays for Clock network

2.1.1.2. Poly Bias With 4nm

Table 3: Cell List

Cell Type	Drive Strength	Cell Description
C12T28SOIDV_LL_CNMUX41	X17, X27	4:1 non-inverting Multiplexer for Clock network,Vdd rail at the bottom of the cell
C12T28SOI_LL_DLYHFM8	X15, X54, X7	Delay Cell for Hold Time Fixing
C12T28SOI_LLP_CNHLS	X15, X22, X29, X36, X51, X58, X71, X7, X93	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C12T28SOI_LL_CNAND2	X15, X20, X33	2 input AND for Clock network
C12T28SOI_LL_CNAND3	X17, X25, X33	3 input AND for Clock network
C12T28SOIDV_LL_SDFSYNCPQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only,Vdd rail at the bottom of the cell
C12T28SOIDV_LL_CNGFMUX21	X15, X30	2:1 Glitch-free MUX for Clock network,Vdd rail at the bottom of the cell
C12T28SOI_LL_CNOR2	X15, X20, X33, X37	2 input OR for Clock network
C12T28SOI_LL_CNMUX21	X17, X33	2:1 non-inverting Multiplexer for Clock network
C12T28SOI_LL_CNOR3	X14, X20	3 input OR for Clock network
C12T28SOI_LL_CNOR4	X20, X27	4 input OR for Clock network

Cell Type	Drive Strength	Cell Description
C12T28SOI_LL_CNSDFPRQT	X15	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network
C12T28SOI_LL_CNNOR2A	X15, X27	2 input NOR with A input Inverted for Clock network
C12T28SOIDV_LL_SDFSYNCPRQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only,Vdd rail at the bottom of the cell
C12T28SOI_LLPHP_CNHLS	X29, X36, X44, X51, X58, X71, X86	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C12T28SOI_LL_CNSDFPSQT	X15	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network
C12T28SOI_LL_CNNAND2	X15, X33	2 input NAND for Clock network
C12T28SOI_LL_CNBF	X133, X15, X22, X30, X38, X44, X4, X52, X59, X70, X7, X94	Buffer with Balanced rise and fall delays for Clock network
C12T28SOI_LL_CNAO12	X33	2 input AND into 2 input OR
C12T28SOI_LL_CNNAND2A	X17, X27	2 input NAND with A input inverted for Clock network
C12T28SOI_LL_CNNOR2	X14, X33	2 input NOR for Clock network
C12T28SOIDV_LL_SDFSYNCPSQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only,Vdd rail at the bottom of the cell
C12T28SOI_LL_CNLDLRQ	X33	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LL_DLYHFM4	X15, X7	Delay Cell for Hold Time Fixing
C12T28SOI_LL_CNXOR2	X16, X27	2 input Exclusive OR for Clock network
C12T28SOI_LL_CNIV	X133, X16, X23, X31, X39, X47, X55, X5, X61, X70, X8, X94	Inverter with Balanced rise and fall delays for Clock network

2.1.1.3. Poly Bias With 10nm

Table 4: Cell List

Cell Type	Drive Strength	Cell Description
C12T28SOIDV_LL_CNMUX41	X17, X27	4:1 non-inverting Multiplexer for Clock network,Vdd rail at the bottom of the cell
C12T28SOI_LL_DLYHFM8	X15, X54, X7	Delay Cell for Hold Time Fixing
C12T28SOI_LLP_CNHLS	X15, X22, X29, X36, X51, X58, X71, X7, X93	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell;

Cell Type	Drive Strength	Cell Description
		having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C12T28SOI_LL_CNAND2	X15, X20, X33	2 input AND for Clock network
C12T28SOI_LL_CNAND3	X17, X25, X33	3 input AND for Clock network
C12T28SOIDV_LL_SDFSYNCPQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only,Vdd rail at the bottom of the cell
C12T28SOIDV_LL_CNGFMUX21	X15, X30	2:1 Glitch-free MUX for Clock network,Vdd rail at the bottom of the cell
C12T28SOI_LL_CNOR2	X15, X20, X33, X37	2 input OR for Clock network
C12T28SOI_LL_CNMUX21	X17, X33	2:1 non-inverting Multiplexer for Clock network
C12T28SOI_LL_CNOR3	X14, X20	3 input OR for Clock network
C12T28SOI_LL_CNOR4	X20, X27	4 input OR for Clock network
C12T28SOI_LL_CNSDFPRQT	X15	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network
C12T28SOI_LL_CNNOR2A	X15, X27	2 input NOR with A input Inverted for Clock network
C12T28SOIDV_LL_SDFSYNCPRQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only,Vdd rail at the bottom of the cell
C12T28SOI_LLPHP_CNHLS	X29, X36, X44, X51, X58, X71, X86	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C12T28SOI_LL_CNSDFPSQT	X15	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network
C12T28SOI_LL_CNNAND2	X15, X33	2 input NAND for Clock network
C12T28SOI_LL_CNBF	X133, X15, X22, X30, X38, X44, X4, X52, X59, X70, X7, X94	Buffer with Balanced rise and fall delays for Clock network
C12T28SOI_LL_CNAO12	X33	2 input AND into 2 input OR
C12T28SOI_LL_CNNAND2A	X17, X27	2 input NAND with A input inverted for Clock network
C12T28SOI_LL_CNNOR2	X14, X33	2 input NOR for Clock network
C12T28SOIDV_LL_SDFSYNCPSQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only,Vdd rail at the bottom of the cell

Cell Type	Drive Strength	Cell Description
C12T28SOI_LL_CNLDLRQ	X33	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LL_DLYHFM4	X15, X7	Delay Cell for Hold Time Fixing
C12T28SOI_LL_CNXOR2	X16, X27	2 input Exclusive OR for Clock network
C12T28SOI_LL_CNIV	X133, X16, X23, X31, X39, X47, X55, X5, X61, X70, X8, X94	Inverter with Balanced rise and fall delays for Clock network

2.1.1.4. Poly Bias With 16nm

Table 5: Cell List

Cell Type	Drive Strength	Cell Description
C12T28SOIDV_LL_CNMUX41	X17, X27	4:1 non-inverting Multiplexer for Clock network,Vdd rail at the bottom of the cell
C12T28SOI_LL_DLYHFM8	X15, X54, X7	Delay Cell for Hold Time Fixing
C12T28SOI_LLP_CNHLS	X15, X22, X29, X36, X51, X58, X71, X7, X93	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C12T28SOI_LL_CNAND2	X15, X20, X33	2 input AND for Clock network
C12T28SOI_LL_CNAND3	X17, X25, X33	3 input AND for Clock network
C12T28SOIDV_LL_SDFSYNCPQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only,Vdd rail at the bottom of the cell
C12T28SOIDV_LL_CNGFMUX21	X15, X30	2:1 Glitch-free MUX for Clock network,Vdd rail at the bottom of the cell
C12T28SOI_LL_CNOR2	X15, X20, X33, X37	2 input OR for Clock network
C12T28SOI_LL_CNMUX21	X17, X33	2:1 non-inverting Multiplexer for Clock network
C12T28SOI_LL_CNOR3	X14, X20	3 input OR for Clock network
C12T28SOI_LL_CNOR4	X20, X27	4 input OR for Clock network
C12T28SOI_LL_CNSDFPRQT	X15	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network
C12T28SOI_LL_CNNOR2A	X15, X27	2 input NOR with A input Inverted for Clock network
C12T28SOIDV_LL_SDFSYNCPRQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only,Vdd rail at the bottom of the cell
C12T28SOI_LLPHP_CNHLS	X29, X36, X44, X51, X58, X71, X86	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network

Cell Type	Drive Strength	Cell Description
C12T28SOI_LL_CNSDFPSQT	X15	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network
C12T28SOI_LL_CNNAND2	X15, X33	2 input NAND for Clock network
C12T28SOI_LL_CNBF	X133, X15, X22, X30, X38, X44, X4, X52, X59, X70, X7, X94	Buffer with Balanced rise and fall delays for Clock network
C12T28SOI_LL_CNAO12	X33	2 input AND into 2 input OR
C12T28SOI_LL_CNNAND2A	X17, X27	2 input NAND with A input inverted for Clock network
C12T28SOI_LL_CNNOR2	X14, X33	2 input NOR for Clock network
C12T28SOIDV_LL_SDFSYNCPSQ	X8	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only,Vdd rail at the bottom of the cell
C12T28SOI_LL_CNLDLRQ	X33	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LL_DLYHFM4	X15, X7	Delay Cell for Hold Time Fixing
C12T28SOI_LL_CNXOR2	X16, X27	2 input Exclusive OR for Clock network
C12T28SOI_LL_CNIV	X133, X16, X23, X31, X39, X47, X55, X5, X61, X70, X8, X94	Inverter with Balanced rise and fall delays for Clock network

2.2. Cell Usage

Cell names starting with CNHLS* are used for clock gating. Clock gating module is used to disable clock to parts of the design that are not in use over that period. The cells have been set as "don't use" and "don't touch" in the .lib file

- Clocktree synthesis must only use the cells from CLOCK library (except DLY cells).
- For hold correction, following cells must be used:
  - DLY (delay cells)
  - CNIV
  - CNBF
- DLY cells are specifically meant for hold fixing only and no other cells other than DLY, CNIV, and CNBF must appear in hold correction.
- For datapath, all CN* cells can be used.

2.3. Delay Cell Specifications

Delay cells present in this library has been designed with Specific Targeted Delay at Best Process, 1.15V with no FBB, -40C

Table 6: Cell Usage

Cell Type	Minimum Targeted Delay @ ff28_1.15V_0.00V_0.00V_0.00V_m40C
C12T28SOI_LL_DLYHFM4X*_P0	40 ps
C12T28SOI_LL_DLYHFM8X*_P0	80 ps

3. Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

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