C28SOI_IO_ALLF_IOSUPPLYKIT_EG User's Manual

Contains Electrostatic Discharge IPs designed in 28 nm FDSOI technology

Overview

The C28SOI_IO_ALLF_IOSUPPLYKIT_EG library is a reference library for ESD IPs. It includes all ESD IPs leaf cells needed for 28nm FDSOI libraries.

Features

- Includes ESD IPs for digital CSF and 3V3SF supplies, dedicated supplies, corners, step/esdhub/cut fillers and core cells.
- Includes ESD IPs for ANAF IOs, supplies, dedicated supplies and step/esdhub/cut fillers.

Applications

- As no TOP CELLS provided by this library, there are no direct application for this library except for IO designers.

Information Snapshot

Table 1 : Operating values

Symbol	Parameter	Min	Typ	Max	Unit
vdd	Core supply voltage	*	1.0	1.1	V
vdde	Pad supply voltage	*	1.0	1.1	V
		*	1.8	1.95	V
		*	3.3	3.6	V
$T_{junction}$	Operating junction temperature	- 40	25	125	°C

* As per Design Platform specification

For more details about electrical specifications, please refer *Section 2: Electrical Specifications*.

Process Options

- GO1: SVT
- GO2: 28 Å

Packaging

- Flip-chip

1. Quick References

The document uses the following convention to indicate logic levels:

- *L indicates logic low.*
- *H indicates logic high.*
- *X indicates don't care state.*
- *Z indicates high impedance state.*
- *'-' (Hyphen) indicates 'No activity'.*

** suffixed in library name indicates multiple metallization options.*
*** suffixed in cell name indicates multiple packages / configurations.*

1.1 Metal Stacking Convention

The metallization option supported by this library can be referred from its product package. The following is the convention that can be used to decode the segment in the library name:

- 7 metal option (5U1X2T8XLB) known as 5002 refers as follows:
  - 5U1X refers to the first 5 levels with 1X pitch (thin) metal.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 8 metal option (6U1X2T8XLB) known as 6002 refers as follows:
  - 6U1X refers to the first 6 levels with 1X pitch (thin) metal in ultra low K.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 10 metal option (6U1X2U2X2T8XLB) known as 6202 refers as follows:
  - 6U1X refers to the first 6 levels with 1x pitch (thin) metal in ultra low K.
  - 2U2X refers to the next 2 levels with 2x pitch (thin) metal in ultra low K.
  - 2T8X refers to 2 levels with 8x (thick) metal in oxide.
  - LB is the Alucap.

1.2 Reference Documentation

The following documents can be used for further study:

- CMOS028 FDSOI DRM.

1.3 Reference library

The C28SOI_IO_ALLF_IOSUPPLYKIT_EG library refers to some cells from 28nm FDSOI libraries listed below. For a correct usage, these libraries are mandatory:

- C28SOI_IO_ALLF_FRAMEKIT_EG

1.4 Acronyms and Abbreviations Used

Table 2 : Acronyms and Abbreviations

Acronym/Abbreviation	Description
B2B	Back-to-Back
CDM	Charge Device Model
DRM	Design Rule Manual
ESD	Electrostatic Discharge
HBM	Human Body Model
FC	Flip-chip
CL	Cluster
MM	Machine Model
SVT	Standard V_T
2ROWS	Two rows

2. Electrical Specifications

2.1 ESD and Latch-up Characteristics

The ESD network is designed and simulated to withstand the following levels under worst-case process conditions.

Table 3 : ESD and Latch-up Characteristics

Symbol	Parameter	Conditions	Target	Unit
V_{ESD}	Electrostatic discharge voltage	Human Body Model (HBM) [1]	2000	V
		Machine Model (MM) [1]	100	V
		Charge Device Model (CDM) [1]	500V JEDEC	V
$I_{latch-up}$	Injection current	Maximum operating junction temperature 125 °C [2]	100	mA
	Over-voltage stress		1.5 * vdde	V

[1] ESD qualification: according to Electrostatic Discharge Sensitivity Measurement

[2] Latch-up qualification: according to Latch-up Sensitivity Measurement

The level of CDM current seen at a given pre-charge voltage varies significantly with the chip size and package type. For instance, larger dies/packages generates higher CDM current.

However, this package size dependence has been considered during IO qualification, so that the above CDM commitment remains valid for any die/package size (even for large die/package sizes of hundreds of mm^2).

3. Contact Information

ST users, login to **HELPDESK**. (http://col2.cro.st.com/helpdesk) for submitting queries or support requests.

Non-ST users, contact Customer Support personnel.

Appendix A: Document Revision History

Table 4 : Document Revision History

Date	Document Version	Comments
8-February-2016	1.4	▪ Reference library added ▪ Table 1 max voltage added in “Operating values” ▪ Table 2 “acronyms and abbreviations” completed ▪ **T**able 3 “ESD and Latch-up Characteristics” improved
18-Sept-2014	1.3	▪ Alignment to new template
10-Sept-2013	1.2	▪ Confidentiality message added
04-Jan-2012	1.1	▪ Ported to the new template ▪ ESD IPs details removed
28-Jun-2012	1.0	▪ First release

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