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C28SOI_SC_8_COREPBP4_LL Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 4 nm

Overview

- C28SOI_SC_8_COREPBP4_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

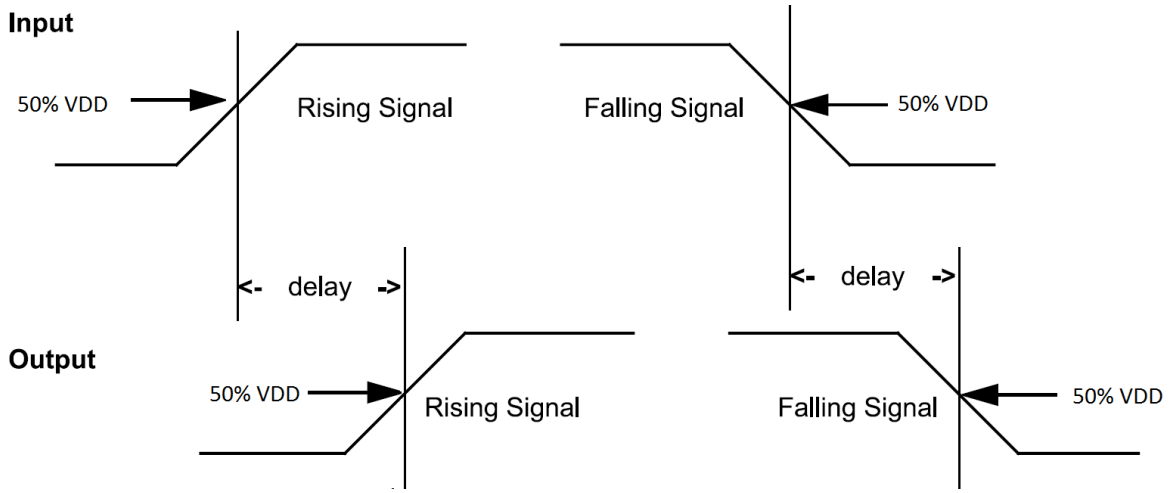


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

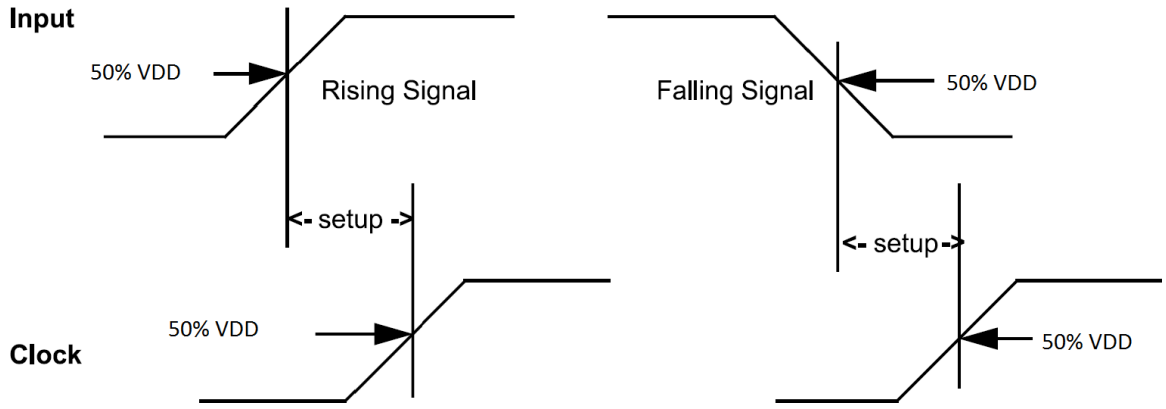


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

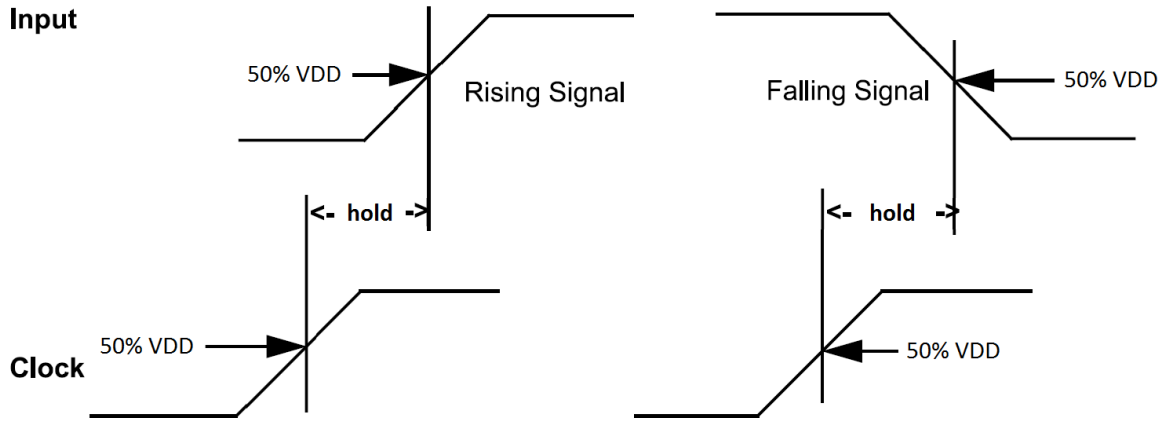


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

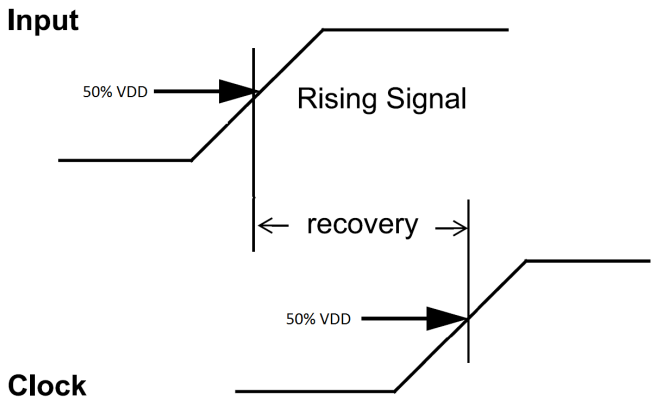


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

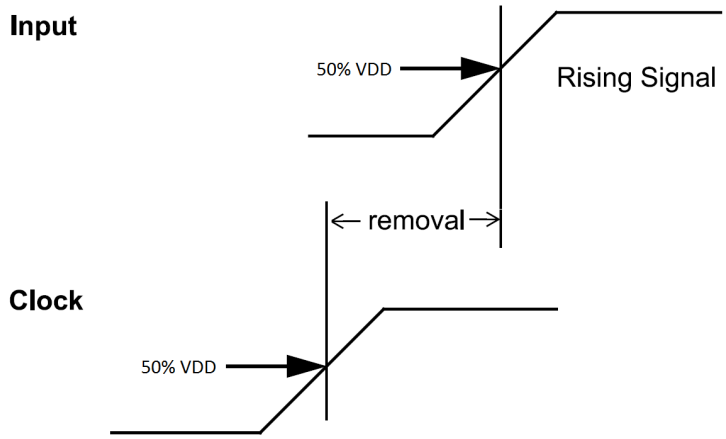


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

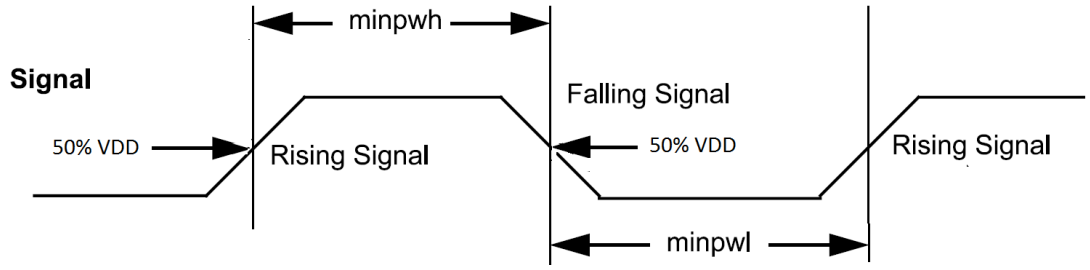


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

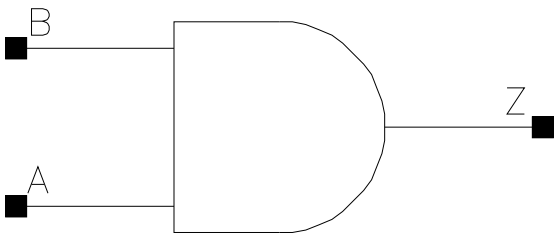
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.544	0.4352
X10_P4	0.800	0.680	0.5440
X11_P4	1.600	0.544	0.8704
X19_P4	0.800	1.224	0.9792
X24_P4	0.800	1.360	1.0880
X29_P4	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X11_P4	X19_P4
A	0.0005	0.0007	0.0009	0.0014
B	0.0004	0.0006	0.0008	0.0012
	X24_P4	X29_P4		
A	0.0013	0.0013		
B	0.0012	0.0012		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0273	0.0223	2.9985	1.4354
A to Z ↑	0.0215	0.0201	4.3931	2.1030
B to Z ↓	0.0261	0.0210	3.0004	1.4343
B to Z ↑	0.0231	0.0213	4.3891	2.1019
	X11_P4	**X19_P4**	**X11_P4**	**X19_P4**

A to Z ↓	0.0242	0.0219	1.1319	0.7389
A to Z ↑	0.0187	0.0198	2.0138	1.0601
B to Z ↓	0.0226	0.0211	1.1311	0.7400
B to Z ↑	0.0199	0.0212	2.0157	1.0592
	X24_P4	**X29_P4**	**X24_P4**	**X29_P4**
A to Z ↓	0.0236	0.0251	0.6019	0.5015
A to Z ↑	0.0215	0.0230	0.8503	0.7064
B to Z ↓	0.0230	0.0245	0.6022	0.5019
B to Z ↑	0.0231	0.0248	0.8506	0.7068

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.184e-06	1.000e-20
X10_P4	2.883e-06	1.000e-20
X11_P4	3.237e-06	1.000e-20
X19_P4	5.461e-06	1.000e-20
X24_P4	6.356e-06	1.000e-20
X29_P4	7.250e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X11_P4	X19_P4
A (output stable)	8.948e-06	1.765e-05	2.393e-05	3.325e-05
B (output stable)	2.490e-05	4.697e-05	6.746e-05	9.700e-05
A to Z	1.522e-03	2.545e-03	3.073e-03	5.019e-03
B to Z	1.454e-03	2.433e-03	2.895e-03	4.774e-03
	X24_P4	X29_P4		
A (output stable)	3.335e-05	3.344e-05		
B (output stable)	9.802e-05	9.831e-05		
A to Z	6.077e-03	7.052e-03		
B to Z	5.843e-03	6.832e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

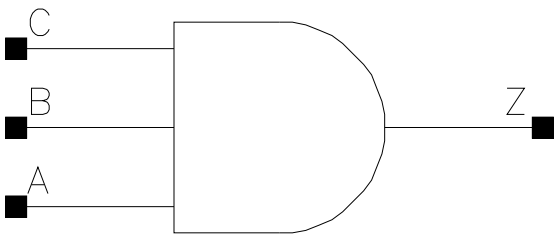
Pin Cycle (vdds)	X5_P4	X10_P4	X11_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P4	X29_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.680	0.5440
X10_P4	0.800	0.816	0.6528
X14_P4	0.800	1.360	1.0880
X19_P4	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0005	0.0007	0.0012	0.0014
B	0.0004	0.0006	0.0010	0.0013
C	0.0005	0.0007	0.0009	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0306	0.0249	3.0312	1.4439
A to Z ↑	0.0285	0.0261	4.4440	2.1319
B to Z ↓	0.0298	0.0238	3.0321	1.4435
B to Z ↑	0.0299	0.0271	4.4446	2.1318
C to Z ↓	0.0287	0.0227	3.0346	1.4420
C to Z ↑	0.0311	0.0278	4.4490	2.1298
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0251	0.0239	0.9995	0.7411

A to Z ↑	0.0250	0.0246	1.4495	1.0694
B to Z ↓	0.0240	0.0227	0.9995	0.7408
B to Z ↑	0.0261	0.0256	1.4475	1.0699
C to Z ↓	0.0229	0.0216	0.9989	0.7410
C to Z ↑	0.0271	0.0264	1.4482	1.0690

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.178e-06	1.000e-20
X10_P4	2.838e-06	1.000e-20
X14_P4	3.908e-06	1.000e-20
X19_P4	5.441e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	8.141e-06	1.607e-05	2.119e-05	2.845e-05
B (output stable)	2.546e-05	4.879e-05	6.790e-05	9.699e-05
C (output stable)	4.820e-05	9.159e-05	1.295e-04	1.875e-04
A to Z	1.776e-03	2.957e-03	4.312e-03	5.636e-03
B to Z	1.704e-03	2.828e-03	4.107e-03	5.355e-03
C to Z	1.642e-03	2.708e-03	3.934e-03	5.092e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

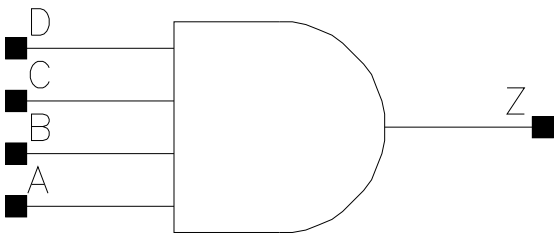
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.088	0.8704
X3_P4	0.800	1.088	0.8704
X10_P4	0.800	2.176	1.7408
X13_P4	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P4	X3_P4	X10_P4	X13_P4
A	0.0005	0.0005	0.0011	0.0012
B	0.0005	0.0004	0.0010	0.0012
C	0.0004	0.0004	0.0010	0.0012
D	0.0005	0.0005	0.0010	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	X3_P4	X2_P4	X3_P4
A to Z ↓	0.0242	0.0259	5.4809	3.6467
A to Z ↑	0.0248	0.0248	15.8720	8.4613
B to Z ↓	0.0228	0.0249	5.4853	3.6501
B to Z ↑	0.0260	0.0263	15.8877	8.4602
C to Z ↓	0.0248	0.0266	5.4803	3.6416
C to Z ↑	0.0245	0.0244	15.8980	8.4786

D to Z ↓	0.0236	0.0260	5.4821	3.6455
D to Z ↑	0.0261	0.0268	15.8966	8.4752
	X10_P4	**X13_P4**	**X10_P4**	**X13_P4**
A to Z ↓	0.0244	0.0245	1.2552	0.9347
A to Z ↑	0.0237	0.0258	2.8146	2.1611
B to Z ↓	0.0234	0.0225	1.2562	0.9336
B to Z ↑	0.0251	0.0264	2.8150	2.1624
C to Z ↓	0.0245	0.0235	1.2489	0.9377
C to Z ↑	0.0227	0.0224	2.8153	2.1599
D to Z ↓	0.0223	0.0215	1.2465	0.9357
D to Z ↑	0.0230	0.0228	2.8167	2.1602

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P4	8.287e-07	1.000e-20
X3_P4	1.189e-06	1.000e-20
X10_P4	3.862e-06	1.000e-20
X13_P4	5.494e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P4	X3_P4	X10_P4	X13_P4
A (output stable)	3.345e-04	3.978e-04	1.040e-03	1.428e-03
B (output stable)	3.142e-04	3.751e-04	9.838e-04	1.359e-03
C (output stable)	3.423e-04	3.802e-04	1.005e-03	1.282e-03
D (output stable)	3.211e-04	3.665e-04	9.540e-04	1.211e-03
A to Z	1.239e-03	1.631e-03	4.578e-03	6.243e-03
B to Z	1.171e-03	1.558e-03	4.389e-03	5.814e-03
C to Z	1.255e-03	1.600e-03	4.043e-03	5.097e-03
D to Z	1.188e-03	1.552e-03	3.684e-03	4.675e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

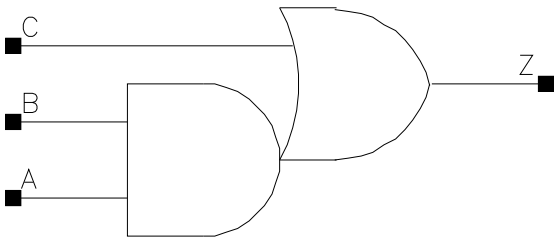
Pin Cycle (vdds)	X2_P4	X3_P4	X10_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	0.952	0.7616
X19_P4	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0004	0.0006	0.0012
B	0.0004	0.0006	0.0011
C	0.0005	0.0006	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0368	0.0325	2.8800	1.4443
A to Z ↑	0.0240	0.0219	4.0741	2.0757
B to Z ↓	0.0347	0.0305	2.8739	1.4400
B to Z ↑	0.0260	0.0237	4.0755	2.0722
C to Z ↓	0.0372	0.0315	2.8683	1.4370
C to Z ↑	0.0227	0.0206	4.0430	2.0602
	X19_P4		**X19_P4**	
A to Z ↓	0.0313		0.7541	
A to Z ↑	0.0238		1.0477	

B to Z ↓	0.0302		0.7543	
B to Z ↑	0.0257		1.0477	
C to Z ↓	0.0309		0.7521	
C to Z ↑	0.0221		1.0382	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.222e-06	1.000e-20
X10_P4	2.580e-06	1.000e-20
X19_P4	4.672e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	9.699e-06	2.213e-05	4.532e-05
B (output stable)	1.541e-05	3.124e-05	6.092e-05
C (output stable)	4.464e-05	5.915e-05	1.398e-04
A to Z	1.747e-03	2.874e-03	5.517e-03
B to Z	1.678e-03	2.752e-03	5.347e-03
C to Z	1.931e-03	3.088e-03	5.970e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

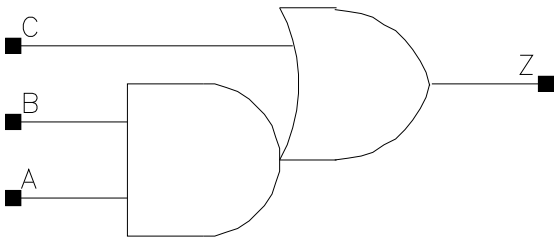
Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	0.952	0.7616
X14_P4	0.800	1.632	1.3056
X19_P4	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0004	0.0006	0.0012	0.0012
B	0.0004	0.0006	0.0012	0.0012
C	0.0005	0.0006	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0383	0.0334	2.8722	1.4526
A to Z ↑	0.0260	0.0241	4.1617	2.0976
B to Z ↓	0.0368	0.0319	2.8647	1.4518
B to Z ↑	0.0285	0.0259	4.1621	2.0984
C to Z ↓	0.0335	0.0301	2.8558	1.4471
C to Z ↑	0.0199	0.0180	4.1105	2.0770
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0305	0.0328	0.9962	0.7478

A to Z ↑	0.0223	0.0237	1.4255	1.0638
B to Z ↓	0.0278	0.0303	0.9924	0.7462
B to Z ↑	0.0232	0.0250	1.4261	1.0628
C to Z ↓	0.0253	0.0278	0.9912	0.7437
C to Z ↑	0.0158	0.0171	1.4105	1.0501

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.229e-06	1.000e-20
X10_P4	2.464e-06	1.000e-20
X14_P4	4.425e-06	1.000e-20
X19_P4	5.056e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.398e-05	1.789e-05	5.704e-05	5.717e-05
B (output stable)	2.070e-05	2.683e-05	1.145e-04	1.135e-04
C (output stable)	5.312e-05	8.460e-05	2.030e-04	2.033e-04
A to Z	1.944e-03	2.996e-03	5.289e-03	6.266e-03
B to Z	1.880e-03	2.877e-03	4.857e-03	5.848e-03
C to Z	1.632e-03	2.571e-03	4.166e-03	5.106e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

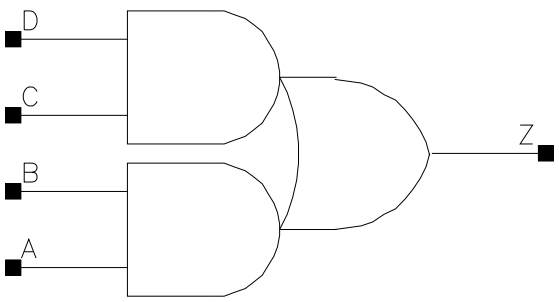
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.088	0.8704
X10_P4	0.800	1.088	0.8704
X14_P4	0.800	1.768	1.4144
X19_P4	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0005	0.0006	0.0012	0.0012
B	0.0005	0.0008	0.0011	0.0011
C	0.0005	0.0006	0.0013	0.0013
D	0.0005	0.0006	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0392	0.0332	2.8844	1.4530
A to Z ↑	0.0275	0.0254	4.1949	2.0780
B to Z ↓	0.0361	0.0305	2.8713	1.4481

B to Z ↑	0.0285	0.0265	4.1933	2.0781
C to Z ↓	0.0353	0.0304	2.8740	1.4493
C to Z ↑	0.0233	0.0213	4.1848	2.0725
D to Z ↓	0.0338	0.0290	2.8707	1.4468
D to Z ↑	0.0254	0.0230	4.1824	2.0735
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0302	0.0325	0.9957	0.7513
A to Z ↑	0.0226	0.0242	1.4329	1.0706
B to Z ↓	0.0284	0.0308	0.9950	0.7510
B to Z ↑	0.0243	0.0260	1.4318	1.0709
C to Z ↓	0.0277	0.0301	0.9933	0.7500
C to Z ↑	0.0195	0.0211	1.4268	1.0678
D to Z ↓	0.0261	0.0287	0.9935	0.7495
D to Z ↑	0.0208	0.0226	1.4260	1.0679

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.488e-06	1.000e-20
X10_P4	3.130e-06	1.000e-20
X14_P4	5.189e-06	1.000e-20
X19_P4	5.951e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	2.528e-05	3.405e-05	4.940e-05	4.952e-05
B (output stable)	1.032e-04	1.292e-04	8.232e-05	8.281e-05
C (output stable)	2.470e-05	2.850e-05	5.977e-05	5.993e-05
D (output stable)	3.016e-05	4.708e-05	9.657e-05	9.850e-05
A to Z	2.234e-03	3.398e-03	5.518e-03	6.576e-03
B to Z	2.025e-03	3.091e-03	5.212e-03	6.274e-03
C to Z	1.879e-03	2.882e-03	4.594e-03	5.642e-03
D to Z	1.804e-03	2.766e-03	4.344e-03	5.387e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

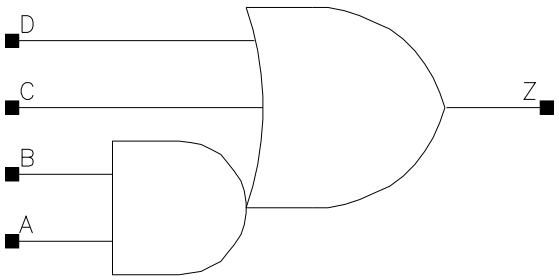
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	1.088	0.8704
X19_P4	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0004	0.0006	0.0011
B	0.0004	0.0006	0.0011
C	0.0005	0.0006	0.0012
D	0.0004	0.0006	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0455	0.0388	3.1959	1.5077
A to Z ↑	0.0250	0.0214	4.3517	2.0886
B to Z ↓	0.0438	0.0363	3.1914	1.5026
B to Z ↑	0.0270	0.0231	4.3516	2.0890
C to Z ↓	0.0474	0.0404	3.1867	1.5017
C to Z ↑	0.0232	0.0284	4.3177	2.0920

D to Z ↓	0.0475	0.0411	3.1875	1.5023
D to Z ↑	0.0230	0.0279	4.3187	2.0911
	X19_P4		**X19_P4**	
A to Z ↓	0.0385		0.7818	
A to Z ↑	0.0236		1.0383	
B to Z ↓	0.0352		0.7781	
B to Z ↑	0.0245		1.0389	
C to Z ↓	0.0392		0.7779	
C to Z ↑	0.0236		1.0312	
D to Z ↓	0.0390		0.7787	
D to Z ↑	0.0233		1.0317	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	9.191e-07	1.000e-20
X10_P4	2.150e-06	1.000e-20
X19_P4	3.938e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	1.006e-05	1.990e-05	4.921e-05
B (output stable)	1.402e-05	2.487e-05	7.696e-05
C (output stable)	3.395e-05	3.959e-05	8.326e-05
D (output stable)	1.335e-05	3.009e-05	5.390e-05
A to Z	1.844e-03	3.025e-03	5.932e-03
B to Z	1.781e-03	2.892e-03	5.511e-03
C to Z	2.082e-03	3.517e-03	6.704e-03
D to Z	1.984e-03	3.348e-03	6.313e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

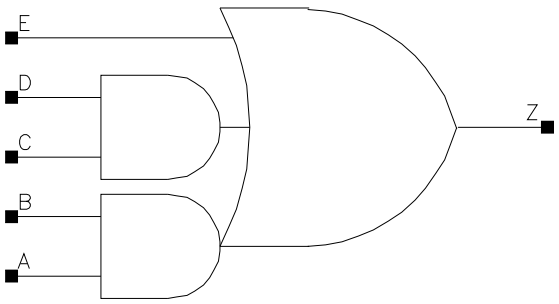
Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.088	0.8704
X10_P4	0.800	1.224	0.9792
X19_P4	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0004	0.0006	0.0012
B	0.0004	0.0006	0.0011
C	0.0004	0.0008	0.0012
D	0.0004	0.0006	0.0011
E	0.0004	0.0006	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0565	0.0449	3.0193	1.4988
A to Z ↑	0.0314	0.0267	4.2373	2.0987

B to Z ↓	0.0558	0.0431	3.0136	1.4967
B to Z ↑	0.0345	0.0286	4.2379	2.0973
C to Z ↓	0.0502	0.0404	3.0118	1.4963
C to Z ↑	0.0277	0.0228	4.2079	2.0862
D to Z ↓	0.0474	0.0369	3.0009	1.4901
D to Z ↑	0.0299	0.0242	4.2105	2.0873
E to Z ↓	0.0506	0.0401	2.9954	1.4900
E to Z ↑	0.0247	0.0211	4.1651	2.0718
	X19_P4		**X19_P4**	
A to Z ↓	0.0435		0.7739	
A to Z ↑	0.0275		1.0542	
B to Z ↓	0.0417		0.7732	
B to Z ↑	0.0297		1.0528	
C to Z ↓	0.0380		0.7713	
C to Z ↑	0.0229		1.0465	
D to Z ↓	0.0360		0.7701	
D to Z ↑	0.0248		1.0467	
E to Z ↓	0.0387		0.7694	
E to Z ↑	0.0259		1.0424	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.192e-06	1.000e-20
X10_P4	2.676e-06	1.000e-20
X19_P4	4.798e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	1.387e-05	2.384e-05	4.802e-05
B (output stable)	2.154e-05	2.936e-05	5.474e-05
C (output stable)	1.917e-05	2.880e-05	5.606e-05
D (output stable)	2.502e-05	3.694e-05	6.830e-05
E (output stable)	3.946e-05	5.975e-05	1.167e-04
A to Z	2.528e-03	3.886e-03	7.446e-03
B to Z	2.485e-03	3.744e-03	7.169e-03
C to Z	2.103e-03	3.167e-03	5.950e-03
D to Z	2.024e-03	3.008e-03	5.732e-03
E to Z	2.207e-03	3.372e-03	6.446e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

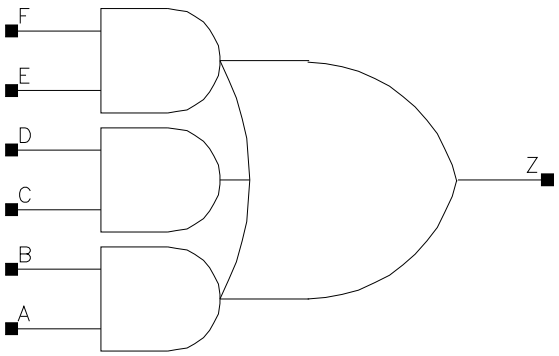
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.360	1.0880
X5_P4	0.800	1.360	1.0880
X10_P4	0.800	1.632	1.3056
X19_P4	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P4	X5_P4	X10_P4	X19_P4
A	0.0005	0.0005	0.0007	0.0012

B	0.0005	0.0005	0.0008	0.0010
C	0.0007	0.0007	0.0005	0.0011
D	0.0005	0.0005	0.0006	0.0010
E	0.0007	0.0007	0.0006	0.0012
F	0.0005	0.0005	0.0006	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	X5_P4	X2_P4	X5_P4
A to Z ↓	0.0443	0.0456	5.6613	3.0953
A to Z ↑	0.0308	0.0304	8.4095	4.4367
B to Z ↓	0.0424	0.0437	5.6445	3.0865
B to Z ↑	0.0334	0.0330	8.4042	4.4360
C to Z ↓	0.0415	0.0429	5.6569	3.0929
C to Z ↑	0.0286	0.0283	8.3371	4.4063
D to Z ↓	0.0382	0.0396	5.6425	3.0839
D to Z ↑	0.0303	0.0301	8.3321	4.4054
E to Z ↓	0.0347	0.0360	5.6348	3.0819
E to Z ↑	0.0239	0.0236	8.2921	4.3845
F to Z ↓	0.0321	0.0336	5.6204	3.0760
F to Z ↑	0.0253	0.0252	8.2931	4.3839
	X10_P4	X19_P4	X10_P4	X19_P4
A to Z ↓	0.0485	0.0452	1.4957	0.7711
A to Z ↑	0.0325	0.0296	2.1123	1.0588
B to Z ↓	0.0459	0.0436	1.4897	0.7705
B to Z ↑	0.0342	0.0319	2.1110	1.0580
C to Z ↓	0.0448	0.0422	1.4924	0.7706
C to Z ↑	0.0289	0.0273	2.1000	1.0521
D to Z ↓	0.0432	0.0408	1.4892	0.7701
D to Z ↑	0.0313	0.0295	2.0993	1.0519
E to Z ↓	0.0396	0.0383	1.4884	0.7685
E to Z ↑	0.0249	0.0239	2.0912	1.0488
F to Z ↓	0.0373	0.0362	1.4839	0.7671
F to Z ↑	0.0268	0.0258	2.0909	1.0488

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P4	1.326e-06	1.000e-20
X5_P4	1.766e-06	1.000e-20
X10_P4	3.045e-06	1.000e-20
X19_P4	5.813e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P4	X5_P4	X10_P4	X19_P4
A (output stable)	2.895e-05	2.894e-05	3.917e-05	6.296e-05
B (output stable)	3.446e-05	3.444e-05	9.338e-05	7.759e-05
C (output stable)	2.190e-05	2.195e-05	2.838e-05	4.653e-05
D (output stable)	2.911e-05	2.913e-05	3.926e-05	6.803e-05
E (output stable)	3.172e-05	3.168e-05	4.349e-05	6.816e-05
F (output stable)	3.915e-05	3.911e-05	5.185e-05	8.826e-05

A to Z	2.486e-03	2.825e-03	4.370e-03	8.016e-03
B to Z	2.387e-03	2.725e-03	4.104e-03	7.748e-03
C to Z	2.070e-03	2.406e-03	3.825e-03	7.055e-03
D to Z	1.952e-03	2.286e-03	3.715e-03	6.842e-03
E to Z	1.615e-03	1.941e-03	3.305e-03	6.225e-03
F to Z	1.524e-03	1.851e-03	3.188e-03	5.982e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

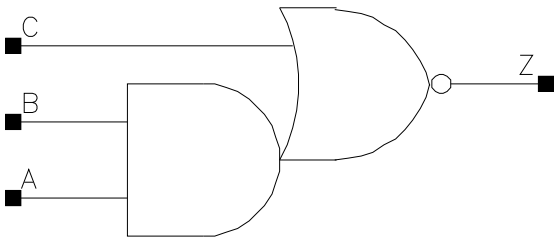
Pin Cycle (vdds)	X2_P4	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X10_P4	0.800	1.360	1.0880
X19_P4	0.800	2.584	2.0672
X25_P4	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P4	X10_P4	X19_P4	X25_P4
A	0.0006	0.0015	0.0029	0.0039
B	0.0005	0.0013	0.0027	0.0036
C	0.0006	0.0016	0.0029	0.0039

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X10_P4**	**X3_P4**	**X10_P4**
A to Z ↓	0.0085	0.0091	4.8755	1.7697
A to Z ↑	0.0157	0.0160	8.1519	2.7897
B to Z ↓	0.0089	0.0093	4.9440	1.7945
B to Z ↑	0.0132	0.0129	8.0015	2.7809
C to Z ↓	0.0090	0.0092	3.0044	1.0479
C to Z ↑	0.0158	0.0161	7.4240	2.5669
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0096	0.0096	0.9038	0.6905

A to Z ↑	0.0165	0.0163	1.4299	1.0644
B to Z ↓	0.0093	0.0094	0.9175	0.7011
B to Z ↑	0.0131	0.0131	1.4282	1.0774
C to Z ↓	0.0107	0.0108	0.6374	0.4880
C to Z ↑	0.0164	0.0162	1.3177	0.9868

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	1.127e-06	1.000e-20
X10_P4	2.967e-06	1.000e-20
X19_P4	5.673e-06	1.000e-20
X25_P4	7.496e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X10_P4	X19_P4	X25_P4
A (output stable)	2.403e-05	8.066e-05	1.644e-04	2.115e-04
B (output stable)	3.416e-05	1.498e-04	3.132e-04	4.038e-04
C (output stable)	6.239e-05	2.017e-04	3.992e-04	5.453e-04
A to Z	7.545e-04	2.350e-03	4.872e-03	6.344e-03
B to Z	6.379e-04	1.819e-03	3.704e-03	4.900e-03
C to Z	1.035e-03	3.081e-03	6.133e-03	8.158e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

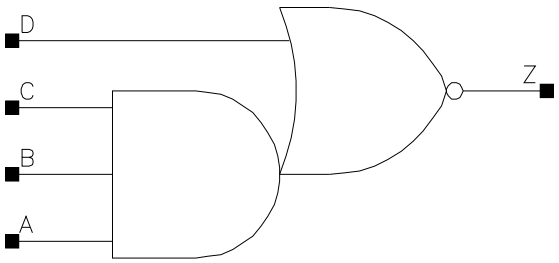
Pin Cycle (vdds)	X3_P4	X10_P4	X19_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X17_P4	0.800	3.536	2.8288
X22_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X17_P4	X22_P4
A	0.0005	0.0029	0.0040
B	0.0005	0.0027	0.0037
C	0.0006	0.0026	0.0035
D	0.0006	0.0030	0.0039

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X17_P4**	**X3_P4**	**X17_P4**
A to Z ↓	0.0128	0.0137	6.8112	1.3089
A to Z ↑	0.0204	0.0198	8.1592	1.3753
B to Z ↓	0.0135	0.0140	6.8400	1.3159
B to Z ↑	0.0185	0.0177	8.1732	1.3983
C to Z ↓	0.0145	0.0131	6.8909	1.3246
C to Z ↑	0.0174	0.0148	8.1969	1.4071
D to Z ↓	0.0111	0.0126	2.9341	0.6282

D to Z ↑	0.0200	0.0187	7.0284	1.1958
	X22_P4		**X22_P4**	
A to Z ↓	0.0136		0.9952	
A to Z ↑	0.0195		1.0287	
B to Z ↓	0.0137		1.0016	
B to Z ↑	0.0174		1.0496	
C to Z ↓	0.0131		1.0082	
C to Z ↑	0.0146		1.0592	
D to Z ↓	0.0132		0.5204	
D to Z ↑	0.0182		0.8952	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	1.189e-06	1.000e-20
X17_P4	5.552e-06	1.000e-20
X22_P4	7.210e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X17_P4	X22_P4
A (output stable)	1.662e-05	1.145e-04	1.537e-04
B (output stable)	3.071e-05	2.398e-04	3.173e-04
C (output stable)	5.403e-05	4.706e-04	6.178e-04
D (output stable)	9.062e-05	5.575e-04	7.305e-04
A to Z	1.166e-03	6.710e-03	8.723e-03
B to Z	1.025e-03	5.578e-03	7.233e-03
C to Z	9.110e-04	4.456e-03	5.768e-03
D to Z	1.485e-03	7.952e-03	1.032e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

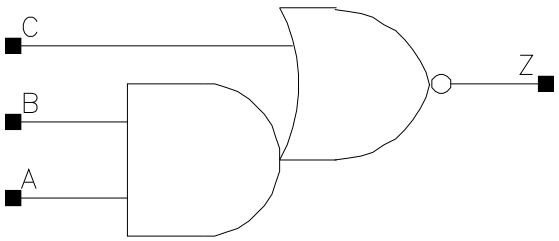
Pin Cycle (vdds)	X3_P4	X17_P4	X22_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X6_P4	0.800	1.088	0.8704
X9_P4	0.800	1.360	1.0880
X12_P4	0.800	1.904	1.5232
X25_P4	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X9_P4	X12_P4
A	0.0005	0.0011	0.0016	0.0022
B	0.0005	0.0010	0.0015	0.0020
C	0.0006	0.0009	0.0013	0.0018
	X25_P4			
A	0.0043			
B	0.0040			
C	0.0036			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0117	0.0115	6.3775	2.5756
A to Z ↑	0.0176	0.0186	9.2947	4.1417
B to Z ↓	0.0131	0.0116	6.4303	2.6070

B to Z ↑	0.0160	0.0157	9.1590	4.1551
C to Z ↓	0.0076	0.0065	3.9655	1.8913
C to Z ↑	0.0138	0.0126	8.5293	3.8372
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0110	0.0115	1.7716	1.3303
A to Z ↑	0.0174	0.0176	2.7747	2.0504
B to Z ↓	0.0115	0.0114	1.7959	1.3479
B to Z ↑	0.0145	0.0146	2.7746	2.0780
C to Z ↓	0.0065	0.0064	1.2923	0.9658
C to Z ↑	0.0119	0.0121	2.5708	1.9145
	X25_P4		**X25_P4**	
A to Z ↓	0.0113		0.6937	
A to Z ↑	0.0171		1.0421	
B to Z ↓	0.0115		0.7025	
B to Z ↑	0.0142		1.0466	
C to Z ↓	0.0063		0.4913	
C to Z ↑	0.0117		0.9695	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	8.749e-07	1.000e-20
X6_P4	2.124e-06	1.000e-20
X9_P4	2.956e-06	1.000e-20
X12_P4	3.971e-06	1.000e-20
X25_P4	7.673e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.820e-05	5.651e-05	7.475e-05	1.074e-04
B (output stable)	2.584e-05	1.135e-04	1.374e-04	2.154e-04
C (output stable)	7.617e-05	1.883e-04	2.585e-04	3.603e-04
A to Z	9.387e-04	2.306e-03	3.149e-03	4.365e-03
B to Z	8.404e-04	1.887e-03	2.548e-03	3.467e-03
C to Z	5.782e-04	1.260e-03	1.726e-03	2.399e-03
	X25_P4			
A (output stable)	2.066e-04			
B (output stable)	3.857e-04			
C (output stable)	6.767e-04			
A to Z	8.285e-03			
B to Z	6.677e-03			
C to Z	4.510e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

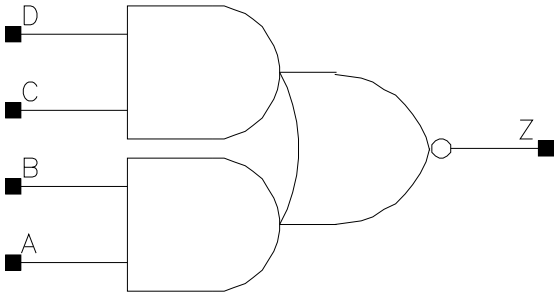
	X25_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.680	0.5440
X6_P4	0.800	1.224	0.9792
X9_P4	0.800	1.768	1.4144
X12_P4	0.800	2.448	1.9584
X24_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P4	X6_P4	X9_P4	X12_P4
A	0.0004	0.0011	0.0016	0.0021
B	0.0004	0.0010	0.0015	0.0021
C	0.0004	0.0011	0.0015	0.0020
D	0.0004	0.0009	0.0014	0.0019
	X24_P4			
A	0.0042			
B	0.0041			
C	0.0040			
D	0.0037			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X6_P4**	**X2_P4**	**X6_P4**
A to Z ↓	0.0118	0.0121	6.4919	2.4708
A to Z ↑	0.0222	0.0193	11.6520	3.7856
B to Z ↓	0.0130	0.0132	6.5679	2.4971
B to Z ↑	0.0200	0.0172	11.6132	3.8678
C to Z ↓	0.0086	0.0085	6.5149	2.4832
C to Z ↑	0.0177	0.0155	11.6109	3.7716
D to Z ↓	0.0092	0.0091	6.6132	2.5185
D to Z ↑	0.0153	0.0136	11.5661	3.8874
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0130	0.0135	1.7740	1.3357
A to Z ↑	0.0201	0.0205	2.5417	1.9108
B to Z ↓	0.0140	0.0141	1.7942	1.3512
B to Z ↑	0.0178	0.0180	2.5447	1.8870
C to Z ↓	0.0092	0.0098	1.7712	1.3387
C to Z ↑	0.0163	0.0167	2.5338	1.8901
D to Z ↓	0.0097	0.0095	1.7983	1.3598
D to Z ↑	0.0136	0.0137	2.5318	1.8971
	X24_P4		**X24_P4**	
A to Z ↓	0.0135		0.6902	
A to Z ↑	0.0203		0.9654	
B to Z ↓	0.0142		0.6981	
B to Z ↑	0.0177		0.9577	
C to Z ↓	0.0098		0.6751	
C to Z ↑	0.0168		0.9591	
D to Z ↓	0.0096		0.6863	
D to Z ↑	0.0137		0.9626	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P4	7.218e-07	1.000e-20
X6_P4	2.523e-06	1.000e-20
X9_P4	3.531e-06	1.000e-20
X12_P4	4.704e-06	1.000e-20
X24_P4	9.103e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.925e-05	4.895e-05	9.157e-05	1.325e-04
B (output stable)	2.960e-05	8.211e-05	2.122e-04	3.359e-04
C (output stable)	2.260e-05	5.651e-05	1.030e-04	1.479e-04
D (output stable)	3.494e-05	9.442e-05	2.127e-04	3.301e-04
A to Z	9.862e-04	2.588e-03	4.085e-03	5.611e-03
B to Z	8.685e-04	2.271e-03	3.502e-03	4.807e-03
C to Z	5.988e-04	1.607e-03	2.590e-03	3.623e-03
D to Z	5.035e-04	1.361e-03	2.081e-03	2.851e-03
	X24_P4			
A (output stable)	2.469e-04			
B (output stable)	5.768e-04			
C (output stable)	2.884e-04			
D (output stable)	6.593e-04			

A to Z	1.089e-02			
B to Z	9.357e-03			
C to Z	7.075e-03			
D to Z	5.617e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

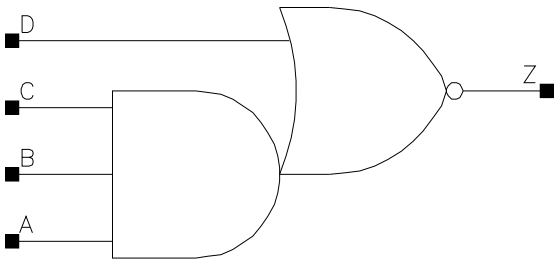
Pin Cycle (vdds)	X2_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X12_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X12_P4
A	0.0006	0.0021
B	0.0005	0.0020
C	0.0007	0.0019
D	0.0005	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X12_P4	X3_P4	X12_P4
A to Z ↓	0.0147	0.0154	6.8222	1.9417
A to Z ↑	0.0218	0.0208	7.9688	2.0816
B to Z ↓	0.0159	0.0156	6.8478	1.9497
B to Z ↑	0.0205	0.0188	8.0793	2.0822
C to Z ↓	0.0176	0.0153	6.8932	1.9597
C to Z ↑	0.0200	0.0161	8.1308	2.0958
D to Z ↓	0.0070	0.0060	3.0038	0.8186
D to Z ↑	0.0148	0.0127	6.9142	1.7865

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	1.227e-06	1.000e-20
X12_P4	4.042e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X12_P4
A (output stable)	1.376e-05	6.511e-05
B (output stable)	2.728e-05	1.537e-04
C (output stable)	5.126e-05	2.922e-04
D (output stable)	1.465e-04	5.291e-04
A to Z	1.493e-03	5.519e-03
B to Z	1.353e-03	4.679e-03
C to Z	1.257e-03	3.887e-03
D to Z	8.256e-04	2.666e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

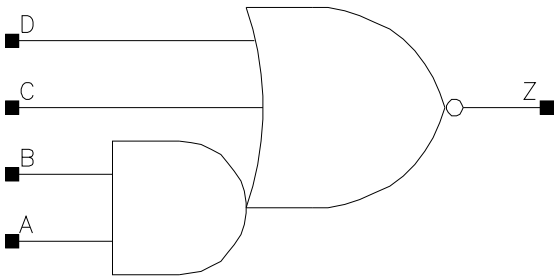
Pin Cycle (vdds)	X3_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X20_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P4	X20_P4
A	0.0005	0.0038
B	0.0005	0.0036
C	0.0005	0.0037
D	0.0006	0.0035

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X20_P4	X3_P4	X20_P4
A to Z ↓	0.0100	0.0110	4.7823	0.7812
A to Z ↑	0.0210	0.0198	11.8226	1.5380
B to Z ↓	0.0108	0.0112	4.8469	0.7934
B to Z ↑	0.0187	0.0161	11.9328	1.5391
C to Z ↓	0.0110	0.0149	2.9758	0.6214
C to Z ↑	0.0243	0.0229	11.2651	1.4539
D to Z ↓	0.0106	0.0137	2.9778	0.6207

D to Z ↑	0.0247	0.0216	11.2917	1.4594

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	1.001e-06	1.000e-20
X20_P4	6.012e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X20_P4
A (output stable)	2.304e-05	1.919e-04
B (output stable)	2.922e-05	2.715e-04
C (output stable)	3.983e-05	4.357e-04
D (output stable)	3.099e-05	2.356e-04
A to Z	9.785e-04	6.691e-03
B to Z	8.575e-04	5.346e-03
C to Z	1.483e-03	1.077e-02
D to Z	1.311e-03	8.664e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

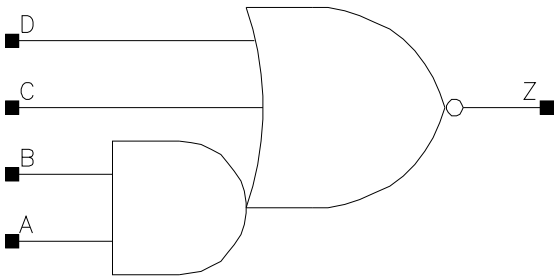
Pin Cycle (vdds)	X3_P4	X20_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.816	0.6528
X10_P4	0.800	2.448	1.9584
X19_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P4	X10_P4	X19_P4
A	0.0005	0.0020	0.0041
B	0.0005	0.0019	0.0038
C	0.0006	0.0017	0.0034
D	0.0005	0.0016	0.0031

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	X10_P4	X2_P4	X10_P4
A to Z ↓	0.0131	0.0135	5.6579	1.5152
A to Z ↑	0.0255	0.0237	12.5230	3.0645
B to Z ↓	0.0146	0.0141	5.7250	1.5321
B to Z ↑	0.0231	0.0204	12.5663	3.0725
C to Z ↓	0.0120	0.0110	4.9784	1.2536
C to Z ↑	0.0193	0.0175	11.9201	2.9082

D to Z ↓	0.0101	0.0084	5.0188	1.2676
D to Z ↑	0.0177	0.0146	11.9432	2.9211
	X19_P4		**X19_P4**	
A to Z ↓	0.0132		0.7781	
A to Z ↑	0.0231		1.5570	
B to Z ↓	0.0140		0.7878	
B to Z ↑	0.0199		1.5566	
C to Z ↓	0.0114		0.6753	
C to Z ↑	0.0169		1.4764	
D to Z ↓	0.0087		0.6828	
D to Z ↑	0.0139		1.4839	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P4	8.146e-07	1.000e-20
X10_P4	3.329e-06	1.000e-20
X19_P4	6.567e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P4	X10_P4	X19_P4
A (output stable)	2.221e-05	8.987e-05	1.781e-04
B (output stable)	2.367e-05	1.364e-04	2.541e-04
C (output stable)	9.848e-06	1.173e-04	2.300e-04
D (output stable)	3.469e-05	2.146e-04	4.054e-04
A to Z	1.418e-03	5.324e-03	1.023e-02
B to Z	1.285e-03	4.527e-03	8.717e-03
C to Z	8.790e-04	3.356e-03	6.346e-03
D to Z	7.151e-04	2.369e-03	4.408e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

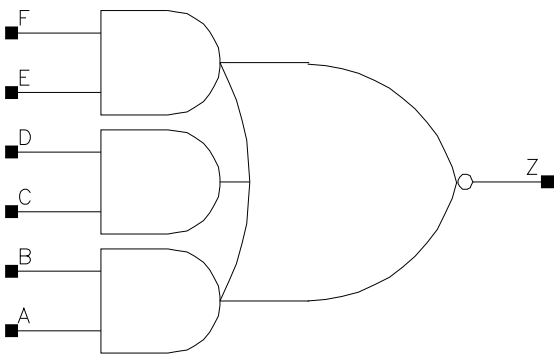
Pin Cycle (vdds)	X2_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.088	0.8704
X5_P4	0.800	2.040	1.6320
X7_P4	0.800	2.720	2.1760
X9_P4	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P4	X5_P4	X7_P4	X9_P4
A	0.0005	0.0009	0.0015	0.0020

B	0.0005	0.0011	0.0014	0.0018
C	0.0005	0.0009	0.0014	0.0021
D	0.0005	0.0010	0.0013	0.0018
E	0.0006	0.0010	0.0014	0.0018
F	0.0005	0.0008	0.0013	0.0017

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X5_P4**	**X2_P4**	**X5_P4**
A to Z ↓	0.0142	0.0171	5.0536	2.8761
A to Z ↑	0.0325	0.0305	12.1516	5.5367
B to Z ↓	0.0158	0.0190	5.1138	2.8967
B to Z ↑	0.0300	0.0288	12.1982	5.4912
C to Z ↓	0.0131	0.0155	5.0977	2.8648
C to Z ↑	0.0287	0.0274	12.2339	5.5530
D to Z ↓	0.0145	0.0170	5.1726	2.8910
D to Z ↑	0.0262	0.0258	12.2125	5.5253
E to Z ↓	0.0101	0.0119	5.1349	2.8138
E to Z ↑	0.0227	0.0223	12.1859	5.4964
F to Z ↓	0.0107	0.0128	5.2251	2.8457
F to Z ↑	0.0195	0.0199	12.1427	5.5146
	X7_P4	**X9_P4**	**X7_P4**	**X9_P4**
A to Z ↓	0.0168	0.0172	2.0015	1.5259
A to Z ↑	0.0296	0.0303	3.6292	2.7342
B to Z ↓	0.0182	0.0184	2.0191	1.5387
B to Z ↑	0.0273	0.0277	3.7095	2.7769
C to Z ↓	0.0152	0.0158	2.0101	1.5170
C to Z ↑	0.0268	0.0281	3.7041	2.7803
D to Z ↓	0.0165	0.0162	2.0318	1.5329
D to Z ↑	0.0241	0.0243	3.6709	2.7572
E to Z ↓	0.0113	0.0115	2.0084	1.5196
E to Z ↑	0.0211	0.0211	3.6531	2.7571
F to Z ↓	0.0121	0.0115	2.0381	1.5435
F to Z ↑	0.0184	0.0179	3.6844	2.7534

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P4	1.336e-06	1.000e-20
X5_P4	2.872e-06	1.000e-20
X7_P4	4.179e-06	1.000e-20
X9_P4	5.259e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P4	X5_P4	X7_P4	X9_P4
A (output stable)	3.232e-05	5.963e-05	1.030e-04	1.434e-04
B (output stable)	4.096e-05	8.523e-05	1.695e-04	2.640e-04
C (output stable)	2.784e-05	5.487e-05	8.524e-05	1.243e-04
D (output stable)	4.030e-05	7.759e-05	1.591e-04	2.268e-04
E (output stable)	3.335e-05	7.061e-05	1.202e-04	1.672e-04
F (output stable)	4.638e-05	9.103e-05	1.820e-04	2.870e-04

A to Z	1.921e-03	3.935e-03	5.733e-03	7.841e-03
B to Z	1.770e-03	3.734e-03	5.201e-03	7.054e-03
C to Z	1.456e-03	3.068e-03	4.438e-03	6.039e-03
D to Z	1.318e-03	2.873e-03	3.960e-03	5.338e-03
E to Z	9.541e-04	2.198e-03	3.039e-03	4.035e-03
F to Z	8.335e-04	1.969e-03	2.602e-03	3.353e-03

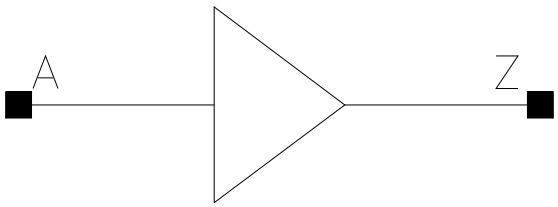
Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P4	X5_P4	X7_P4	X9_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description
Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.544	0.4352
X5_P4	0.800	0.544	0.4352
X9_P4	0.800	0.680	0.5440
X11_P4	1.600	0.408	0.6528
X13_P4	0.800	0.680	0.5440
X19_P4	0.800	0.952	0.7616
X23_P4	1.600	0.544	0.8704
X24_P4	0.800	1.088	0.8704
X29_P4	0.800	1.224	0.9792
X34_P4	1.600	0.680	1.0880
X38_P4	0.800	1.632	1.3056
X46_P4	1.600	0.952	1.5232
X57_P4	0.800	2.312	1.8496
X68_P4	1.600	1.224	1.9584
X91_P4	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P4	X5_P4	X9_P4	X11_P4
A	0.0005	0.0006	0.0006	0.0008
	X13_P4	X19_P4	X23_P4	X24_P4
A	0.0007	0.0009	0.0011	0.0011
	X29_P4	X34_P4	X38_P4	X46_P4
A	0.0013	0.0014	0.0019	0.0019
	X57_P4	X68_P4	X91_P4	
A	0.0025	0.0026	0.0035	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X5_P4**	**X2_P4**	**X5_P4**
A to Z ↓	0.0224	0.0230	5.4323	2.9637
A to Z ↑	0.0174	0.0174	8.2167	4.3039
	X9_P4	**X11_P4**	**X9_P4**	**X11_P4**
A to Z ↓	0.0274	0.0255	1.5211	1.1389
A to Z ↑	0.0207	0.0185	2.1459	2.0116
	X13_P4	**X19_P4**	**X13_P4**	**X19_P4**
A to Z ↓	0.0242	0.0242	1.0444	0.7375
A to Z ↑	0.0194	0.0181	1.4946	1.0425
	X23_P4	**X24_P4**	**X23_P4**	**X24_P4**
A to Z ↓	0.0244	0.0239	0.5513	0.6017
A to Z ↑	0.0179	0.0187	1.0142	0.8367
	X29_P4	**X34_P4**	**X29_P4**	**X34_P4**
A to Z ↓	0.0230	0.0241	0.4984	0.3799
A to Z ↑	0.0183	0.0181	0.7026	0.6935
	X38_P4	**X46_P4**	**X38_P4**	**X46_P4**
A to Z ↓	0.0225	0.0235	0.3772	0.2852
A to Z ↑	0.0181	0.0174	0.5167	0.5222
	X57_P4	**X68_P4**	**X57_P4**	**X68_P4**
A to Z ↓	0.0235	0.0231	0.2540	0.1937
A to Z ↑	0.0189	0.0174	0.3468	0.3494
	X91_P4		**X91_P4**	
A to Z ↓	0.0243		0.1495	
A to Z ↑	0.0183		0.2625	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P4	6.329e-07	1.000e-20
X5_P4	1.148e-06	1.000e-20
X9_P4	2.011e-06	1.000e-20
X11_P4	2.629e-06	1.000e-20
X13_P4	3.155e-06	1.000e-20
X19_P4	3.973e-06	1.000e-20
X23_P4	5.180e-06	1.000e-20
X24_P4	5.047e-06	1.000e-20
X29_P4	6.171e-06	1.000e-20
X34_P4	7.382e-06	1.000e-20
X38_P4	8.330e-06	1.000e-20
X46_P4	9.409e-06	1.000e-20
X57_P4	1.193e-05	1.000e-20
X68_P4	1.401e-05	1.000e-20
X91_P4	1.783e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P4	X5_P4	X9_P4	X11_P4
A to Z	1.092e-03	1.398e-03	2.230e-03	2.679e-03
	X13_P4	X19_P4	X23_P4	X24_P4
A to Z	3.253e-03	4.374e-03	4.913e-03	5.445e-03
	X29_P4	X34_P4	X38_P4	X46_P4

A to Z	6.358e-03	7.386e-03	8.719e-03	9.400e-03
	X57_P4	X68_P4	X91_P4	
A to Z	1.290e-02	1.375e-02	1.850e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

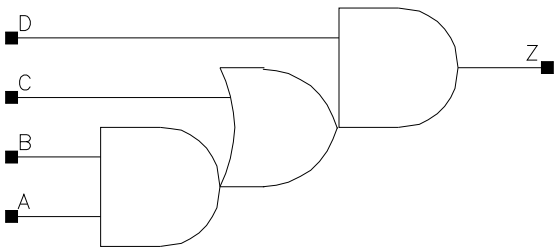
Pin Cycle (vdds)	X2_P4	X5_P4	X9_P4	X11_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P4	X19_P4	X23_P4	X24_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P4	X34_P4	X38_P4	X46_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P4	X68_P4	X91_P4	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.952	0.7616
X10_P4	0.800	1.632	1.3056
X14_P4	0.800	1.768	1.4144
X19_P4	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0006	0.0013	0.0013	0.0013
B	0.0006	0.0012	0.0011	0.0011
C	0.0006	0.0014	0.0014	0.0014
D	0.0010	0.0012	0.0013	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0299	0.0273	3.0229	1.4278
A to Z ↑	0.0279	0.0254	4.4043	2.0957
B to Z ↓	0.0280	0.0254	3.0168	1.4281
B to Z ↑	0.0287	0.0259	4.4032	2.0953
C to Z ↓	0.0259	0.0234	3.0135	1.4251
C to Z ↑	0.0212	0.0190	4.3679	2.0752

D to Z ↓	0.0251	0.0216	2.9876	1.4126
D to Z ↑	0.0241	0.0205	4.3728	2.0780
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0303	0.0326	0.9990	0.7495
A to Z ↑	0.0282	0.0303	1.4065	1.0552
B to Z ↓	0.0285	0.0309	0.9980	0.7488
B to Z ↑	0.0288	0.0311	1.4065	1.0554
C to Z ↓	0.0263	0.0287	0.9953	0.7460
C to Z ↑	0.0212	0.0230	1.3889	1.0416
D to Z ↓	0.0235	0.0250	0.9828	0.7352
D to Z ↑	0.0226	0.0242	1.3925	1.0439

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.981e-06	1.000e-20
X10_P4	3.998e-06	1.000e-20
X14_P4	4.847e-06	1.000e-20
X19_P4	5.697e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	6.059e-05	1.159e-04	1.154e-04	1.166e-04
B (output stable)	7.448e-05	1.404e-04	1.410e-04	1.416e-04
C (output stable)	2.027e-04	3.452e-04	3.442e-04	3.464e-04
D (output stable)	5.999e-05	8.453e-05	8.623e-05	8.563e-05
A to Z	2.323e-03	4.209e-03	5.377e-03	6.453e-03
B to Z	2.190e-03	3.892e-03	5.058e-03	6.133e-03
C to Z	1.871e-03	3.246e-03	4.341e-03	5.348e-03
D to Z	2.371e-03	4.130e-03	5.189e-03	6.136e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

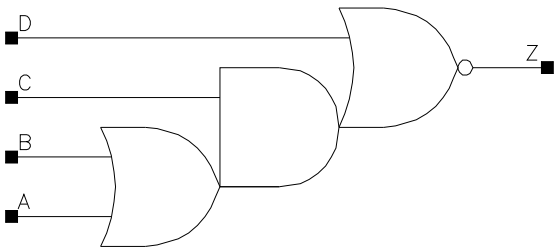
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X6_P4	0.800	1.496	1.1968
X9_P4	0.800	1.768	1.4144
X12_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X9_P4	X12_P4
A	0.0005	0.0011	0.0016	0.0021
B	0.0006	0.0010	0.0016	0.0021
C	0.0005	0.0010	0.0015	0.0020
D	0.0007	0.0010	0.0014	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0136	0.0124	4.9780	2.5476
A to Z ↑	0.0262	0.0258	11.8446	6.2542
B to Z ↓	0.0129	0.0123	4.8275	2.5648
B to Z ↑	0.0263	0.0252	11.8611	6.2667
C to Z ↓	0.0122	0.0115	4.6144	2.3996
C to Z ↑	0.0172	0.0162	8.1543	4.2254

D to Z ↓	0.0072	0.0057	3.0224	1.5409
D to Z ↑	0.0163	0.0139	8.6802	4.5194
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0126	0.0130	1.7510	1.3659
A to Z ↑	0.0240	0.0254	4.0264	3.1047
B to Z ↓	0.0120	0.0122	1.7684	1.3672
B to Z ↑	0.0241	0.0247	4.0334	3.1116
C to Z ↓	0.0117	0.0118	1.6615	1.2842
C to Z ↑	0.0156	0.0158	2.7447	2.0896
D to Z ↓	0.0059	0.0058	1.0730	0.8226
D to Z ↑	0.0130	0.0129	2.9264	2.2370

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	1.192e-06	1.000e-20
X6_P4	2.257e-06	1.000e-20
X9_P4	3.148e-06	1.000e-20
X12_P4	4.119e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.737e-05	4.324e-05	5.237e-05	8.974e-05
B (output stable)	7.738e-06	1.649e-05	2.496e-05	3.574e-05
C (output stable)	6.954e-05	1.507e-04	2.056e-04	2.841e-04
D (output stable)	6.793e-05	1.883e-04	2.441e-04	3.583e-04
A to Z	1.539e-03	2.916e-03	4.054e-03	5.643e-03
B to Z	1.350e-03	2.431e-03	3.511e-03	4.721e-03
C to Z	1.104e-03	2.007e-03	2.875e-03	3.909e-03
D to Z	7.748e-04	1.300e-03	1.814e-03	2.378e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

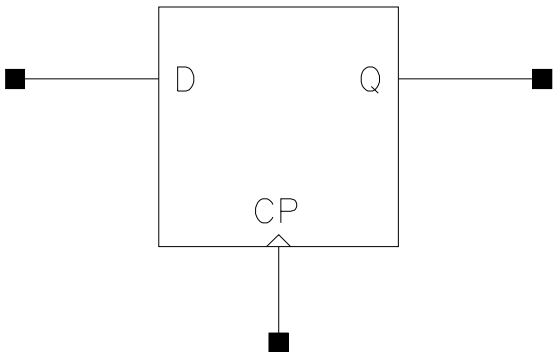
Pin Cycle (vdds)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	1.600	1.496	2.3936
X19_P4	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P4	X19_P4
CP	0.0008	0.0008
D	0.0006	0.0006

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P4	X19_P4	X10_P4	X19_P4
CP to Q ↓	0.0436	0.0582	1.4820	0.8025
CP to Q ↑	0.0503	0.0575	2.0636	1.0623

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P4	X19_P4
CP ↓	min_pulse_width to CP	0.0432	0.0432
CP ↑	min_pulse_width to CP	0.0362	0.0502
D ↓	hold_rising to CP	0.0150	0.0150
D ↑	hold_rising to CP	0.0097	0.0097
D ↓	setup_rising to CP	0.0224	0.0224
D ↑	setup_rising to CP	0.0142	0.0142

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P4	5.380e-06	1.000e-20
X19_P4	6.826e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

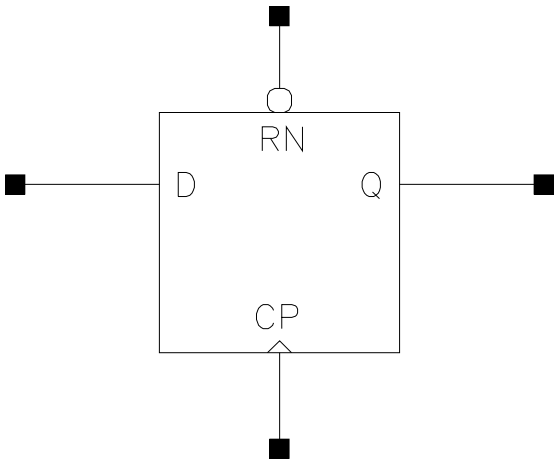
Pin Cycle	X10_P4	X19_P4
Clock 100Mhz Data 0Mhz	7.503e-03	7.508e-03
Clock 100Mhz Data 25Mhz	9.023e-03	1.066e-02
Clock 100Mhz Data 50Mhz	1.054e-02	1.381e-02
Clock = 0 Data 100Mhz	2.999e-03	2.999e-03
Clock = 1 Data 100Mhz	2.270e-05	2.280e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	1.600	1.768	2.8288
X19_P4	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P4	X19_P4
CP	0.0008	0.0008
D	0.0006	0.0006
RN	0.0008	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P4	X19_P4	X10_P4	X19_P4
CP to Q ↓	0.0474	0.0603	1.5069	0.7950
CP to Q ↑	0.0524	0.0593	2.0633	1.0551
RN to Q ↓	0.0488	0.0620	1.4776	0.7656

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P4	X19_P4
CP ↓	min_pulse_width to CP	0.0432	0.0432
CP ↑	min_pulse_width to CP	0.0409	0.0502
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0107	0.0107
D ↓	setup_rising to CP	0.0171	0.0171
D ↑	setup_rising to CP	0.0168	0.0168
RN ↓	min_pulse_width to RN	0.0588	0.0757
RN ↑	recovery_rising to CP	0.0103	0.0103
RN ↑	removal_rising to CP	-0.0028	-0.0055

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P4	6.348e-06	1.000e-20
X19_P4	8.354e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

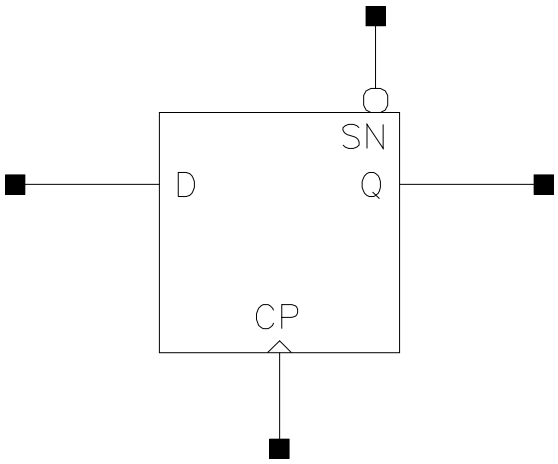
Pin Cycle	X10_P4	X19_P4
Clock 100Mhz Data 0Mhz	7.599e-03	7.601e-03
Clock 100Mhz Data 25Mhz	9.260e-03	1.088e-02
Clock 100Mhz Data 50Mhz	1.092e-02	1.415e-02
Clock = 0 Data 100Mhz	3.019e-03	3.020e-03
Clock = 1 Data 100Mhz	2.313e-05	2.324e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	1.600	1.768	2.8288
X19_P4	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P4	X19_P4
CP	0.0008	0.0008
D	0.0006	0.0006
SN	0.0010	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P4	X19_P4	X10_P4	X19_P4
CP to Q ↓	0.0446	0.0589	1.4921	0.7885
CP to Q ↑	0.0518	0.0593	2.0578	1.0564
SN to Q ↑	0.0328	0.0371	2.0203	1.0265

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P4	X19_P4
CP ↓	min_pulse_width to CP	0.0432	0.0432
CP ↑	min_pulse_width to CP	0.0362	0.0502
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0097	0.0097
D ↓	setup_rising to CP	0.0224	0.0224
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0376	0.0376
SN ↑	recovery_rising to CP	0.0005	0.0005
SN ↑	removal_rising to CP	0.0259	0.0259

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P4	6.168e-06	1.000e-20
X19_P4	7.664e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

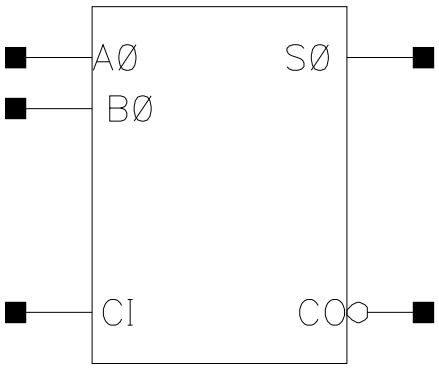
Pin Cycle	X10_P4	X19_P4
Clock 100Mhz Data 0Mhz	7.456e-03	7.460e-03
Clock 100Mhz Data 25Mhz	9.040e-03	1.073e-02
Clock 100Mhz Data 50Mhz	1.063e-02	1.399e-02
Clock = 0 Data 100Mhz	2.895e-03	2.895e-03
Clock = 1 Data 100Mhz	2.326e-05	2.336e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_-P4	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_-P4	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_-P4	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_-P4	1.600	2.720	4.3520
C8T28SOIDV_LLS1_-FA1X4_P4	1.600	2.040	3.2640
C8T28SOIDV_LLS1_-FA1X9_P4	1.600	3.128	5.0048
C8T28SOIDV_LLS1_-FA1X18_P4	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P4	C8T28SOIDV_LL_-FA1X9_P4	C8T28SOIDV_LL_-FA1X14_P4	C8T28SOIDV_LL_-FA1X19_P4
A0	0.0022	0.0023	0.0036	0.0039
B0	0.0018	0.0019	0.0033	0.0036
CI	0.0014	0.0014	0.0024	0.0027
	C8T28SOIDV_LLS1_-FA1X4_P4	C8T28SOIDV_LLS1_-FA1X9_P4	C8T28SOIDV_LLS1_-FA1X18_P4	
A0	0.0021	0.0028	0.0029	
B0	0.0020	0.0032	0.0036	
CI	0.0015	0.0023	0.0027	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P4	**C8T28SOIDV_LL_-FA1X9_P4**	**C8T28SOIDV_LL_-FA1X5_P4**	**C8T28SOIDV_LL_-FA1X9_P4**
A0 to CO ↓	0.0386	0.0413	3.0807	1.5780
A0 to CO ↑	0.0289	0.0309	4.0925	2.0919
A0 to S0 ↓	0.0417	0.0454	3.0314	1.5633
A0 to S0 ↑	0.0429	0.0462	4.1068	2.0582
B0 to CO ↓	0.0386	0.0415	3.0912	1.5853
B0 to CO ↑	0.0300	0.0319	4.0939	2.0940
B0 to S0 ↓	0.0421	0.0460	3.0318	1.5631
B0 to S0 ↑	0.0435	0.0470	4.1100	2.0582
CI to CO ↓	0.0369	0.0396	3.0948	1.5863
CI to CO ↑	0.0296	0.0316	4.0934	2.0918
CI to S0 ↓	0.0418	0.0458	3.0332	1.5635
CI to S0 ↑	0.0433	0.0468	4.1086	2.0579
	C8T28SOIDV_LL_-FA1X14_P4	**C8T28SOIDV_LL_-FA1X19_P4**	**C8T28SOIDV_LL_-FA1X14_P4**	**C8T28SOIDV_LL_-FA1X19_P4**
A0 to CO ↓	0.0395	0.0431	1.0332	0.7864
A0 to CO ↑	0.0296	0.0306	1.4420	1.0758
A0 to S0 ↓	0.0478	0.0483	1.0270	0.7630
A0 to S0 ↑	0.0488	0.0503	1.3905	1.0378
B0 to CO ↓	0.0388	0.0424	1.0360	0.7884
B0 to CO ↑	0.0300	0.0310	1.4415	1.0751
B0 to S0 ↓	0.0481	0.0486	1.0271	0.7631
B0 to S0 ↑	0.0491	0.0505	1.3910	1.0384
CI to CO ↓	0.0371	0.0405	1.0352	0.7878
CI to CO ↑	0.0295	0.0306	1.4418	1.0755
CI to S0 ↓	0.0476	0.0481	1.0269	0.7628
CI to S0 ↑	0.0484	0.0500	1.3907	1.0380
	C8T28SOIDV_-LLS1_FA1X4_P4	**C8T28SOIDV_-LLS1_FA1X9_P4**	**C8T28SOIDV_-LLS1_FA1X4_P4**	**C8T28SOIDV_-LLS1_FA1X9_P4**
A0 to CO ↓	0.0269	0.0244	5.7280	1.9120
A0 to CO ↑	0.0242	0.0223	4.1537	2.0941
A0 to S0 ↓	0.0556	0.0598	3.2365	1.1789
A0 to S0 ↑	0.0524	0.0511	4.3388	2.0469
B0 to CO ↓	0.0251	0.0252	5.7227	1.9137
B0 to CO ↑	0.0202	0.0210	4.1402	2.0927
B0 to S0 ↓	0.0559	0.0624	3.2359	1.1791
B0 to S0 ↑	0.0528	0.0537	4.3335	2.0470
CI to CO ↓	0.0256	0.0346	5.7238	1.9273
CI to CO ↑	0.0220	0.0204	4.1547	2.1091

CI to S0 ↓	0.0320	0.0379	3.2408	1.1811
CI to S0 ↑	0.0281	0.0284	4.3395	2.0480
	C8T28SOIDV_-LLS1_FA1X18_P4		**C8T28SOIDV_-LLS1_FA1X18_P4**	
A0 to CO ↓	0.0306		1.0121	
A0 to CO ↑	0.0231		1.0294	
A0 to S0 ↓	0.0636		0.6108	
A0 to S0 ↑	0.0519		1.0295	
B0 to CO ↓	0.0320		1.0129	
B0 to CO ↑	0.0219		1.0281	
B0 to S0 ↓	0.0650		0.6109	
B0 to S0 ↑	0.0534		1.0289	
CI to CO ↓	0.0427		1.0214	
CI to CO ↑	0.0242		1.0312	
CI to S0 ↓	0.0390		0.6113	
CI to S0 ↑	0.0263		1.0295	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P4	4.631e-06	1.000e-20
C8T28SOIDV_LL_FA1X9_P4	6.386e-06	1.000e-20
C8T28SOIDV_LL_FA1X14_P4	9.339e-06	1.000e-20
C8T28SOIDV_LL_FA1X19_P4	1.179e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P4	1.016e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P4	1.495e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P4	2.267e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P4	C8T28SOIDV_LL_-FA1X9_P4	C8T28SOIDV_LL_-FA1X14_P4	C8T28SOIDV_LL_-FA1X19_P4
A0 to CO	2.545e-03	3.539e-03	5.853e-03	7.082e-03
A0 to S0	2.617e-03	3.492e-03	5.995e-03	7.266e-03
B0 to CO	2.552e-03	3.565e-03	5.855e-03	7.114e-03
B0 to S0	2.548e-03	3.444e-03	5.888e-03	7.145e-03
CI to CO	2.511e-03	3.505e-03	5.800e-03	7.086e-03
CI to S0	2.524e-03	3.417e-03	5.820e-03	7.069e-03
	C8T28SOIDV_LLS1_-FA1X4_P4	C8T28SOIDV_LLS1_-FA1X9_P4	C8T28SOIDV_LLS1_-FA1X18_P4	
A0 to CO	4.010e-03	6.100e-03	9.612e-03	
A0 to S0	5.444e-03	7.911e-03	1.203e-02	
B0 to CO	4.246e-03	6.195e-03	9.682e-03	
B0 to S0	5.834e-03	8.111e-03	1.220e-02	
CI to CO	2.879e-03	5.031e-03	8.427e-03	
CI to S0	3.245e-03	5.590e-03	9.181e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P4	C8T28SOIDV_LL_-FA1X9_P4	C8T28SOIDV_LL_-FA1X14_P4	C8T28SOIDV_LL_-FA1X19_P4
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P4	C8T28SOIDV_LLS1_-FA1X9_P4	C8T28SOIDV_LLS1_-FA1X18_P4	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P4	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P4	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P4	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P4	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P4	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P4	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P4	C8T28SOI_LL_-HA1X9_P4	C8T28SOI_LLS1_-HA1X5_P4	C8T28SOIDV_LL_-HA1X14_P4
A0	0.0007	0.0010	0.0012	0.0015
B0	0.0006	0.0011	0.0011	0.0013
	C8T28SOIDV_LL_-HA1X19_P4	C8T28SOIDV_LLS1_-HA1X11_P4		
A0	0.0018	0.0018		
B0	0.0015	0.0018		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P4	**C8T28SOI_LL_-HA1X9_P4**	**C8T28SOI_LL_-HA1X5_P4**	**C8T28SOI_LL_-HA1X9_P4**
A0 to CO ↓	0.0308	0.0263	3.0505	1.5006
A0 to CO ↑	0.0281	0.0246	4.3760	2.1114
A0 to S0 ↓	0.0386	0.0352	2.9164	1.4836
A0 to S0 ↑	0.0369	0.0338	4.2467	2.1065
B0 to CO ↓	0.0300	0.0257	3.0492	1.5002
B0 to CO ↑	0.0302	0.0268	4.3760	2.1115
B0 to S0 ↓	0.0401	0.0362	2.9156	1.4846
B0 to S0 ↑	0.0363	0.0332	4.2468	2.1074
	C8T28SOI_LLS1_-HA1X5_P4	**C8T28SOIDV_LL_-HA1X14_P4**	**C8T28SOI_LLS1_-HA1X5_P4**	**C8T28SOIDV_LL_-HA1X14_P4**
A0 to CO ↓	0.0249	0.0271	2.9898	1.0217
A0 to CO ↑	0.0224	0.0243	4.3229	1.4200
A0 to S0 ↓	0.0336	0.0389	2.9785	1.0339
A0 to S0 ↑	0.0376	0.0371	4.3501	1.3979
B0 to CO ↓	0.0237	0.0252	2.9896	1.0191
B0 to CO ↑	0.0240	0.0251	4.3226	1.4193
B0 to S0 ↓	0.0353	0.0386	2.9804	1.0337
B0 to S0 ↑	0.0370	0.0354	4.3518	1.3987
	C8T28SOIDV_LL_-HA1X19_P4	**C8T28SOIDV_-LLS1_HA1X11_P4**	**C8T28SOIDV_LL_-HA1X19_P4**	**C8T28SOIDV_-LLS1_HA1X11_P4**
A0 to CO ↓	0.0254	0.0240	0.7527	1.0769
A0 to CO ↑	0.0237	0.0240	1.0754	2.0729
A0 to S0 ↓	0.0359	0.0301	0.7483	1.0914
A0 to S0 ↑	0.0345	0.0318	1.0494	2.0914
B0 to CO ↓	0.0237	0.0227	0.7504	1.0752
B0 to CO ↑	0.0246	0.0259	1.0757	2.0730
B0 to S0 ↓	0.0362	0.0312	0.7480	1.0899
B0 to S0 ↑	0.0330	0.0319	1.0493	2.0894

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_HA1X5_P4	2.569e-06	1.000e-20
C8T28SOI_LL_HA1X9_P4	6.134e-06	1.000e-20
C8T28SOI_LLS1_HA1X5_P4	3.168e-06	1.000e-20
C8T28SOIDV_LL_HA1X14_P4	8.757e-06	1.000e-20
C8T28SOIDV_LL_HA1X19_P4	1.235e-05	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P4	8.167e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

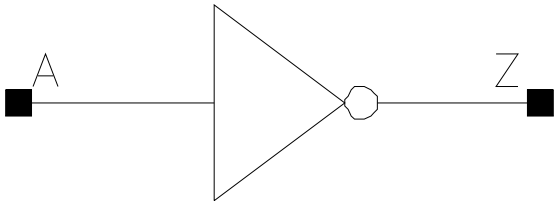
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P4	C8T28SOI_LL_-HA1X9_P4	C8T28SOI_LLS1_-HA1X5_P4	C8T28SOIDV_LL_-HA1X14_P4
A0 to CO	1.931e-03	3.103e-03	2.331e-03	4.995e-03
A0 to S0	1.749e-03	3.000e-03	2.064e-03	5.042e-03
B0 to CO	1.945e-03	3.173e-03	2.349e-03	4.914e-03
B0 to S0	1.723e-03	2.924e-03	2.014e-03	4.889e-03
	C8T28SOIDV_LL_-HA1X19_P4	C8T28SOIDV_LLS1_-HA1X11_P4		
A0 to CO	6.055e-03	4.310e-03		
A0 to S0	6.081e-03	3.947e-03		

B0 to CO	5.982e-03	4.063e-03		
B0 to S0	5.934e-03	4.104e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P4	C8T28SOI_LL_-HA1X9_P4	C8T28SOI_LLS1_-HA1X5_P4	C8T28SOIDV_LL_-HA1X14_P4
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P4	C8T28SOIDV_LLS1_-HA1X11_P4		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P4	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P4	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P4	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P4	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P4	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P4	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P4	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P4	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P4	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P4	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P4	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P4	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P4	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P4	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P4	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P4	C8T28SOI_LL_IVX3_-P4	C8T28SOI_LL_IVX5_-P4	C8T28SOI_LL_-IVX10_P4

A	0.0004	0.0004	0.0005	0.0010
	C8T28SOI_LL_-IVX14_P4	C8T28SOI_LL_-IVX19_P4	C8T28SOI_LL_-IVX29_P4	C8T28SOI_LL_-IVX34_P4
A	0.0016	0.0020	0.0030	0.0035
	C8T28SOI_LL_-IVX38_P4	C8T28SOIDV_LL_-IVX11_P4	C8T28SOIDV_LL_-IVX23_P4	C8T28SOIDV_LL_-IVX34_P4
A	0.0040	0.0011	0.0022	0.0032
	C8T28SOIDV_LL_-IVX46_P4	C8T28SOIDV_LL_-IVX68_P4	C8T28SOIDV_LL_-IVX91_P4	
A	0.0043	0.0065	0.0090	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P4	**C8T28SOI_LL_-IVX3_P4**	**C8T28SOI_LL_-IVX2_P4**	**C8T28SOI_LL_-IVX3_P4**
A to Z ↓	0.0067	0.0063	5.6934	4.4334
A to Z ↑	0.0120	0.0110	8.4848	6.4275
	C8T28SOI_LL_-IVX5_P4	**C8T28SOI_LL_-IVX10_P4**	**C8T28SOI_LL_-IVX5_P4**	**C8T28SOI_LL_-IVX10_P4**
A to Z ↓	0.0057	0.0045	3.0846	1.4848
A to Z ↑	0.0098	0.0081	4.4523	2.1177
	C8T28SOI_LL_-IVX14_P4	**C8T28SOI_LL_-IVX19_P4**	**C8T28SOI_LL_-IVX14_P4**	**C8T28SOI_LL_-IVX19_P4**
A to Z ↓	0.0047	0.0051	1.0320	0.7886
A to Z ↑	0.0081	0.0083	1.4243	1.0945
	C8T28SOI_LL_-IVX29_P4	**C8T28SOI_LL_-IVX34_P4**	**C8T28SOI_LL_-IVX29_P4**	**C8T28SOI_LL_-IVX34_P4**
A to Z ↓	0.0050	0.0047	0.5275	0.4494
A to Z ↑	0.0081	0.0077	0.7242	0.6182
	C8T28SOI_LL_-IVX38_P4	**C8T28SOIDV_LL_-IVX11_P4**	**C8T28SOI_LL_-IVX38_P4**	**C8T28SOIDV_LL_-IVX11_P4**
A to Z ↓	0.0049	0.0044	0.3991	1.1817
A to Z ↑	0.0079	0.0095	0.5485	2.1443
	C8T28SOIDV_LL_-IVX23_P4	**C8T28SOIDV_LL_-IVX34_P4**	**C8T28SOIDV_LL_-IVX23_P4**	**C8T28SOIDV_LL_-IVX34_P4**
A to Z ↓	0.0037	0.0041	0.5769	0.3958
A to Z ↑	0.0084	0.0085	1.0461	0.7022
	C8T28SOIDV_LL_-IVX46_P4	**C8T28SOIDV_LL_-IVX68_P4**	**C8T28SOIDV_LL_-IVX46_P4**	**C8T28SOIDV_LL_-IVX68_P4**
A to Z ↓	0.0040	0.0040	0.2980	0.2034
A to Z ↑	0.0083	0.0081	0.5269	0.3542
	C8T28SOIDV_LL_-IVX91_P4		**C8T28SOIDV_LL_-IVX91_P4**	
A to Z ↓	0.0045		0.1580	
A to Z ↑	0.0085		0.2695	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_IVX2_P4	3.325e-07	1.000e-20
C8T28SOI_LL_IVX3_P4	5.043e-07	1.000e-20
C8T28SOI_LL_IVX5_P4	8.065e-07	1.000e-20
C8T28SOI_LL_IVX10_P4	1.732e-06	1.000e-20

C8T28SOI_LL_IVX14_P4	2.460e-06	1.000e-20
C8T28SOI_LL_IVX19_P4	3.178e-06	1.000e-20
C8T28SOI_LL_IVX29_P4	4.617e-06	1.000e-20
C8T28SOI_LL_IVX34_P4	5.337e-06	1.000e-20
C8T28SOI_LL_IVX38_P4	6.057e-06	1.000e-20
C8T28SOIDV_LL_IVX11_P4	2.024e-06	1.000e-20
C8T28SOIDV_LL_IVX23_P4	4.053e-06	1.000e-20
C8T28SOIDV_LL_IVX34_P4	5.796e-06	1.000e-20
C8T28SOIDV_LL_IVX46_P4	7.507e-06	1.000e-20
C8T28SOIDV_LL_IVX68_P4	1.093e-05	1.000e-20
C8T28SOIDV_LL_IVX91_P4	1.436e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P4	C8T28SOI_LL_IVX3_-P4	C8T28SOI_LL_IVX5_-P4	C8T28SOI_LL_-IVX10_P4
A to Z	3.518e-04	4.287e-04	5.398e-04	9.827e-04
	C8T28SOI_LL_-IVX14_P4	C8T28SOI_LL_-IVX19_P4	C8T28SOI_LL_-IVX29_P4	C8T28SOI_LL_-IVX34_P4
A to Z	1.505e-03	2.048e-03	2.963e-03	3.318e-03
	C8T28SOI_LL_-IVX38_P4	C8T28SOIDV_LL_-IVX11_P4	C8T28SOIDV_LL_-IVX23_P4	C8T28SOIDV_LL_-IVX34_P4
A to Z	3.849e-03	1.184e-03	2.160e-03	3.293e-03
	C8T28SOIDV_LL_-IVX46_P4	C8T28SOIDV_LL_-IVX68_P4	C8T28SOIDV_LL_-IVX91_P4	
A to Z	4.187e-03	6.211e-03	8.266e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

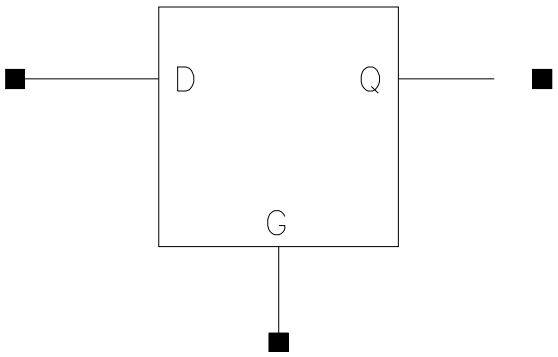
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P4	C8T28SOI_LL_IVX3_-P4	C8T28SOI_LL_IVX5_-P4	C8T28SOI_LL_-IVX10_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P4	C8T28SOI_LL_-IVX19_P4	C8T28SOI_LL_-IVX29_P4	C8T28SOI_LL_-IVX34_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P4	C8T28SOIDV_LL_-IVX11_P4	C8T28SOIDV_LL_-IVX23_P4	C8T28SOIDV_LL_-IVX34_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P4	C8T28SOIDV_LL_-IVX68_P4	C8T28SOIDV_LL_-IVX91_P4	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.360	1.0880
X9_P4	1.600	0.952	1.5232
X19_P4	1.600	1.224	1.9584
X28_P4	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4	X28_P4
D	0.0004	0.0006	0.0009	0.0015
G	0.0009	0.0008	0.0017	0.0016

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D to Q ↓	0.0431	0.0416	3.0994	1.5795
D to Q ↑	0.0250	0.0294	4.2365	2.0664
G to Q ↓	0.0453	0.0431	3.0919	1.5766

G to Q ↑	0.0244	0.0277	4.2457	2.0667
	X19_P4	**X28_P4**	**X19_P4**	**X28_P4**
D to Q ↓	0.0338	0.0356	0.7559	0.5098
D to Q ↑	0.0255	0.0258	1.0397	0.6999
G to Q ↓	0.0374	0.0340	0.7536	0.5084
G to Q ↑	0.0236	0.0239	1.0416	0.6998

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P4	X9_P4	X19_P4	X28_P4
D ↓	hold_falling to G	-0.0040	-0.0040	0.0026	0.0036
D ↑	hold_falling to G	0.0068	0.0019	0.0068	0.0068
D ↓	setup_falling to G	0.0391	0.0392	0.0289	0.0317
D ↑	setup_falling to G	0.0254	0.0302	0.0279	0.0279
G ↑	min_pulse_width to G	0.0364	0.0363	0.0318	0.0318

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.907e-06	1.000e-20
X9_P4	3.341e-06	1.000e-20
X19_P4	5.739e-06	1.000e-20
X28_P4	7.883e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	1.199e-05	3.046e-05	3.713e-05	1.005e-04
G (output stable)	7.986e-04	9.526e-04	1.565e-03	1.453e-03
D to Q	2.906e-03	4.578e-03	6.829e-03	9.953e-03
G to Q	2.713e-03	4.290e-03	6.290e-03	8.626e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

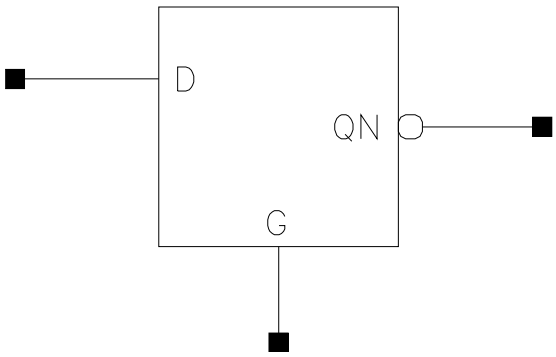
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P4
D	0.0004
G	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P4	X10_P4
D to QN ↓	0.0377	1.4356
D to QN ↑	0.0508	2.0583
G to QN ↓	0.0368	1.4370
G to QN ↑	0.0525	2.0590

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P4
D ↓	hold_falling to G	-0.0120
D ↑	hold_falling to G	0.0019
D ↓	setup_falling to G	0.0365
D ↑	setup_falling to G	0.0232
G ↑	min_pulse_width to G	0.0330

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P4	3.023e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X10_P4
D (output stable)	1.188e-05
G (output stable)	8.594e-04
D to QN	3.861e-03
G to QN	3.635e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

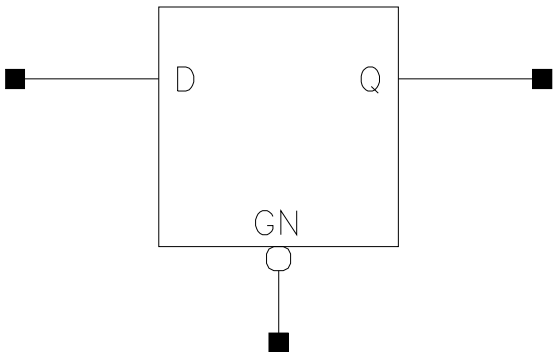
Pin Cycle (vdds)	X10_P4
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.360	1.0880
X9_P4	1.600	0.952	1.5232
X19_P4	1.600	1.224	1.9584
X28_P4	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4	X28_P4
D	0.0004	0.0007	0.0009	0.0014
GN	0.0008	0.0009	0.0013	0.0017

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D to Q ↓	0.0435	0.0410	3.1060	1.5864
D to Q ↑	0.0252	0.0291	4.2347	2.0668
GN to Q ↓	0.0393	0.0392	3.1087	1.5881

GN to Q ↑	0.0429	0.0409	4.2312	2.0598
	X19_P4	**X28_P4**	**X19_P4**	**X28_P4**
D to Q ↓	0.0343	0.0342	0.7524	0.5084
D to Q ↑	0.0267	0.0263	1.0348	0.6932
GN to Q ↓	0.0308	0.0297	0.7532	0.5088
GN to Q ↑	0.0366	0.0365	1.0311	0.6916

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P4	X9_P4	X19_P4	X28_P4
D ↓	hold_rising to GN	-0.0101	-0.0052	0.0002	-0.0003
D ↑	hold_rising to GN	0.0106	0.0053	0.0081	0.0107
D ↓	setup_rising to GN	0.0471	0.0423	0.0374	0.0374
D ↑	setup_rising to GN	0.0217	0.0265	0.0239	0.0248
GN ↓	min_pulse_width to GN	0.0506	0.0511	0.0437	0.0392

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.876e-06	1.000e-20
X9_P4	3.376e-06	1.000e-20
X19_P4	6.230e-06	1.000e-20
X28_P4	8.233e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	1.206e-05	2.113e-05	3.945e-05	8.891e-05
GN (output stable)	7.991e-04	9.318e-04	1.339e-03	1.414e-03
D to Q	2.903e-03	4.587e-03	7.040e-03	9.742e-03
GN to Q	4.391e-03	6.207e-03	9.077e-03	1.161e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

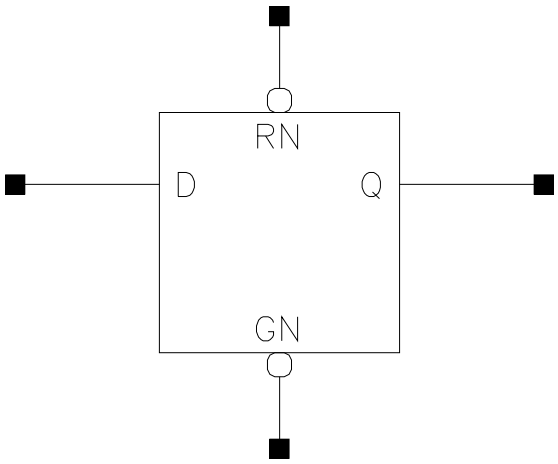
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.632	1.3056
X9_P4	1.600	1.224	1.9584
X19_P4	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4
D	0.0004	0.0006	0.0011
GN	0.0010	0.0010	0.0014
RN	0.0004	0.0005	0.0005

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D to Q ↓	0.0448	0.0427	3.0467	1.5328

D to Q ↑	0.0404	0.0443	4.3917	2.1380
GN to Q ↓	0.0414	0.0398	3.0506	1.5353
GN to Q ↑	0.0551	0.0520	4.3928	2.1447
RN to Q ↓	0.0370	0.0460	2.9412	1.5327
RN to Q ↑	0.0433	0.0470	4.3919	2.1406
	X19_P4		**X19_P4**	
D to Q ↓	0.0356		0.7566	
D to Q ↑	0.0470		1.0818	
GN to Q ↓	0.0324		0.7585	
GN to Q ↑	0.0495		1.0842	
RN to Q ↓	0.0585		0.8090	
RN to Q ↑	0.0517		1.0817	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P4	X9_P4	X19_P4
D ↓	hold_rising to GN	-0.0101	-0.0068	-0.0025
D ↑	hold_rising to GN	-0.0013	-0.0061	-0.0114
D ↓	setup_rising to GN	0.0494	0.0472	0.0402
D ↑	setup_rising to GN	0.0416	0.0465	0.0508
GN ↓	min_pulse_width to GN	0.0555	0.0527	0.0495
RN ↓	min_pulse_width to RN	0.0469	0.0540	0.0686
RN ↑	recovery_rising to GN	0.0444	0.0488	0.0584
RN ↑	removal_rising to GN	-0.0239	-0.0314	-0.0365

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	2.055e-06	1.000e-20
X9_P4	3.476e-06	1.000e-20
X19_P4	6.151e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4
D (output stable)	6.050e-05	4.859e-05	5.949e-05
GN (output stable)	8.989e-04	9.264e-04	1.149e-03
RN (output stable)	2.164e-05	2.604e-05	3.391e-05
D to Q	3.619e-03	5.109e-03	7.802e-03
GN to Q	5.217e-03	6.667e-03	9.640e-03
RN to Q	2.796e-03	3.948e-03	6.275e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

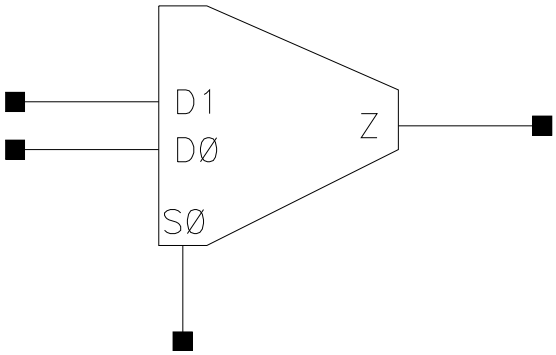
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.360	1.0880
X9_P4	0.800	1.496	1.1968
X14_P4	0.800	2.176	1.7408
X19_P4	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P4	X9_P4	X14_P4	X19_P4
D0	0.0006	0.0007	0.0009	0.0012
D1	0.0005	0.0007	0.0009	0.0012
S0	0.0010	0.0009	0.0012	0.0015

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D0 to Z ↓	0.0332	0.0311	3.0751	1.5557
D0 to Z ↑	0.0261	0.0256	4.3339	2.2089
D1 to Z ↓	0.0335	0.0302	3.0706	1.5522
D1 to Z ↑	0.0257	0.0242	4.3468	2.2059
S0 to Z ↓	0.0315	0.0274	3.0623	1.5485
S0 to Z ↑	0.0297	0.0271	4.3399	2.2061

	X14_P4	X19_P4	X14_P4	X19_P4
D0 to Z ↓	0.0336	0.0296	1.0767	0.7766
D0 to Z ↑	0.0269	0.0248	1.4937	1.0815
D1 to Z ↓	0.0341	0.0305	1.0758	0.7769
D1 to Z ↑	0.0257	0.0241	1.4937	1.0813
S0 to Z ↓	0.0326	0.0300	1.0716	0.7743
S0 to Z ↑	0.0315	0.0287	1.4931	1.0802

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	2.290e-06	1.000e-20
X9_P4	4.240e-06	1.000e-20
X14_P4	5.478e-06	1.000e-20
X19_P4	8.363e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X9_P4	X14_P4	X19_P4
D0 (output stable)	5.588e-04	1.025e-03	1.171e-03	1.461e-03
D1 (output stable)	5.339e-04	8.669e-04	1.224e-03	1.554e-03
S0 (output stable)	8.350e-04	7.501e-04	1.207e-03	1.429e-03
D0 to Z	2.165e-03	3.386e-03	5.373e-03	6.553e-03
D1 to Z	2.109e-03	3.161e-03	5.225e-03	6.491e-03
S0 to Z	2.656e-03	3.317e-03	5.902e-03	7.101e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

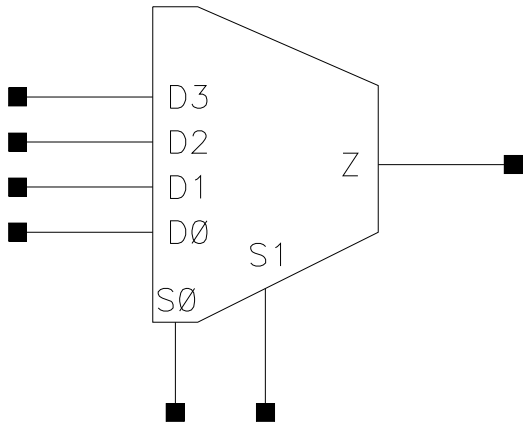
Pin Cycle (vdds)	X5_P4	X9_P4	X14_P4	X19_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.600	1.496	2.3936
X9_P4	1.600	1.768	2.8288
X13_P4	1.600	2.312	3.6992
X18_P4	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P4	X9_P4	X13_P4	X18_P4
D0	0.0004	0.0007	0.0009	0.0009
D1	0.0004	0.0005	0.0009	0.0009
D2	0.0004	0.0006	0.0009	0.0009
D3	0.0004	0.0005	0.0009	0.0009
S0	0.0012	0.0016	0.0021	0.0021
S1	0.0007	0.0008	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X9_P4	X4_P4	X9_P4
D0 to Z ↓	0.0701	0.0583	3.3221	1.6310
D0 to Z ↑	0.0434	0.0396	4.4648	2.2098
D1 to Z ↓	0.0691	0.0580	3.3195	1.6323
D1 to Z ↑	0.0434	0.0394	4.4565	2.2088
D2 to Z ↓	0.0639	0.0587	3.2737	1.6352
D2 to Z ↑	0.0420	0.0393	4.4365	2.2073
D3 to Z ↓	0.0647	0.0578	3.2797	1.6340
D3 to Z ↑	0.0427	0.0393	4.4361	2.2055
S0 to Z ↓	0.0721	0.0640	3.2972	1.6317
S0 to Z ↑	0.0513	0.0490	4.4596	2.2123
S1 to Z ↓	0.0465	0.0437	3.2932	1.6317
S1 to Z ↑	0.0392	0.0382	4.4486	2.2081
	X13_P4	X18_P4	X13_P4	X18_P4
D0 to Z ↓	0.0575	0.0623	1.1474	0.8585
D0 to Z ↑	0.0360	0.0388	1.4810	1.1208
D1 to Z ↓	0.0579	0.0627	1.1483	0.8594
D1 to Z ↑	0.0370	0.0398	1.4814	1.1218
D2 to Z ↓	0.0523	0.0565	1.1293	0.8442
D2 to Z ↑	0.0359	0.0387	1.4776	1.1185
D3 to Z ↓	0.0520	0.0562	1.1283	0.8432
D3 to Z ↑	0.0362	0.0390	1.4759	1.1183
S0 to Z ↓	0.0607	0.0653	1.1376	0.8511
S0 to Z ↑	0.0450	0.0478	1.4804	1.1209
S1 to Z ↓	0.0424	0.0469	1.1376	0.8506
S1 to Z ↑	0.0349	0.0377	1.4790	1.1196

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	2.212e-06	1.000e-20
X9_P4	3.747e-06	1.000e-20
X13_P4	6.411e-06	1.000e-20
X18_P4	7.231e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X9_P4	X13_P4	X18_P4
D0 (output stable)	6.984e-05	4.527e-05	9.796e-05	9.680e-05
D1 (output stable)	7.699e-05	6.857e-05	8.642e-05	8.604e-05
D2 (output stable)	4.399e-05	5.308e-05	7.732e-05	7.681e-05
D3 (output stable)	4.637e-05	5.867e-05	7.558e-05	7.556e-05
S0 (output stable)	1.087e-03	1.304e-03	2.129e-03	2.131e-03
S1 (output stable)	1.020e-03	1.178e-03	1.898e-03	1.899e-03
D0 to Z	2.748e-03	4.011e-03	6.529e-03	7.946e-03
D1 to Z	2.715e-03	3.999e-03	6.602e-03	8.021e-03
D2 to Z	2.577e-03	3.983e-03	6.235e-03	7.593e-03
D3 to Z	2.606e-03	3.980e-03	6.249e-03	7.604e-03
S0 to Z	3.923e-03	5.528e-03	8.859e-03	1.026e-02
S1 to Z	2.843e-03	4.085e-03	6.530e-03	7.904e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

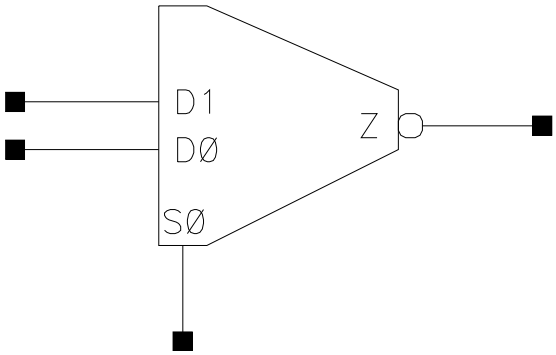
Pin Cycle (vdds)	X4_P4	X9_P4	X13_P4	X18_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P4	0.800	0.952	0.7616
X2_P4	0.800	0.952	0.7616
X6_P4	0.800	1.904	1.5232
X9_P4	0.800	2.448	1.9584
X12_P4	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P4	X2_P4	X6_P4	X9_P4
D0	0.0004	0.0005	0.0011	0.0016
D1	0.0004	0.0005	0.0010	0.0016
S0	0.0009	0.0013	0.0017	0.0025
	X12_P4			
D0	0.0021			
D1	0.0021			
S0	0.0029			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P4	X2_P4	X1_P4	X2_P4
D0 to Z ↓	0.0118	0.0111	8.5006	5.7921

D0 to Z ↑	0.0227	0.0178	18.2860	9.9169
D1 to Z ↓	0.0113	0.0105	8.3976	5.6627
D1 to Z ↑	0.0230	0.0184	18.3170	10.0830
S0 to Z ↓	0.0207	0.0145	8.4099	5.7262
S0 to Z ↑	0.0234	0.0155	18.2143	9.9816
	X6_P4	**X9_P4**	**X6_P4**	**X9_P4**
D0 to Z ↓	0.0125	0.0116	2.6158	1.7607
D0 to Z ↑	0.0186	0.0177	4.1303	2.8883
D1 to Z ↓	0.0121	0.0117	2.5626	1.7713
D1 to Z ↑	0.0197	0.0182	4.2737	2.8176
S0 to Z ↓	0.0171	0.0147	2.5856	1.7645
S0 to Z ↑	0.0179	0.0157	4.1945	2.8515
	X12_P4		**X12_P4**	
D0 to Z ↓	0.0121		1.3497	
D0 to Z ↑	0.0178		2.1790	
D1 to Z ↓	0.0116		1.3434	
D1 to Z ↑	0.0181		2.1242	
S0 to Z ↓	0.0160		1.3451	
S0 to Z ↑	0.0168		2.1498	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X1_P4	7.189e-07	1.000e-20
X2_P4	1.676e-06	1.000e-20
X6_P4	3.410e-06	1.000e-20
X9_P4	5.293e-06	1.000e-20
X12_P4	6.375e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X1_P4	X2_P4	X6_P4	X9_P4
D0 (output stable)	1.207e-05	2.364e-05	7.576e-05	1.108e-04
D1 (output stable)	1.144e-05	2.816e-05	7.673e-05	1.155e-04
S0 (output stable)	8.282e-04	9.270e-04	1.652e-03	2.505e-03
D0 to Z	7.062e-04	9.156e-04	2.419e-03	3.277e-03
D1 to Z	7.044e-04	9.081e-04	2.451e-03	3.347e-03
S0 to Z	1.407e-03	1.482e-03	3.170e-03	4.444e-03
	X12_P4			
D0 (output stable)	1.442e-04			
D1 (output stable)	1.439e-04			
S0 (output stable)	2.970e-03			
D0 to Z	4.434e-03			
D1 to Z	4.403e-03			
S0 to Z	5.643e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X1_P4	X2_P4	X6_P4	X9_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

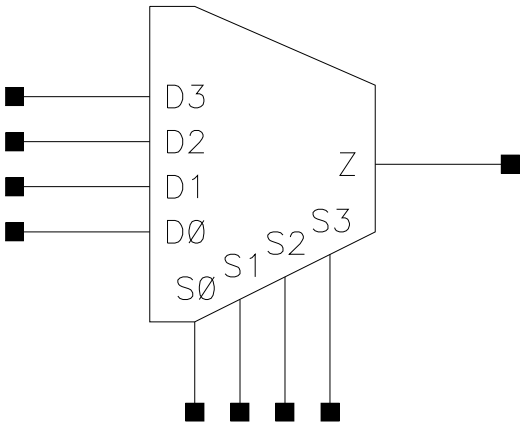
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P4			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.600	0.952	1.5232
X15_P4	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P4	X15_P4
D0	0.0005	0.0014
D1	0.0006	0.0011
D2	0.0006	0.0014
D3	0.0005	0.0011
S0	0.0005	0.0012
S1	0.0005	0.0014
S2	0.0006	0.0012
S3	0.0006	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X15_P4	X4_P4	X15_P4
D0 to Z ↓	0.0369	0.0390	4.9407	1.3060
D0 to Z ↑	0.0303	0.0292	4.0745	1.0326
D1 to Z ↓	0.0340	0.0354	4.9404	1.3054
D1 to Z ↑	0.0263	0.0256	4.0532	1.0273
D2 to Z ↓	0.0359	0.0377	4.9510	1.3081
D2 to Z ↑	0.0296	0.0279	4.0873	1.0376
D3 to Z ↓	0.0327	0.0342	4.9457	1.3060
D3 to Z ↑	0.0256	0.0244	4.0705	1.0323
S0 to Z ↓	0.0352	0.0358	4.9402	1.3049
S0 to Z ↑	0.0324	0.0298	4.0736	1.0317
S1 to Z ↓	0.0320	0.0327	4.9394	1.3041
S1 to Z ↑	0.0280	0.0262	4.0547	1.0271
S2 to Z ↓	0.0348	0.0348	4.9491	1.3062
S2 to Z ↑	0.0317	0.0287	4.0898	1.0371
S3 to Z ↓	0.0319	0.0315	4.9464	1.3047
S3 to Z ↑	0.0277	0.0249	4.0690	1.0318

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	2.958e-06	1.000e-20
X15_P4	8.754e-06	1.000e-20

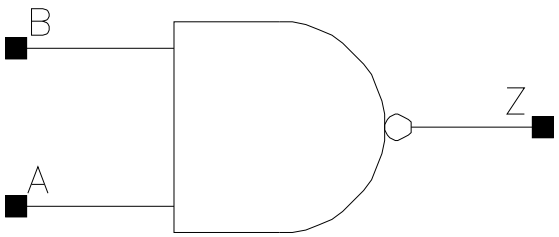
Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X15_P4
D0 (output stable)	3.906e-04	1.090e-03
D1 (output stable)	3.067e-04	8.469e-04
D2 (output stable)	3.956e-04	1.101e-03
D3 (output stable)	3.148e-04	8.608e-04
S0 (output stable)	3.763e-04	1.083e-03
S1 (output stable)	2.982e-04	8.686e-04
S2 (output stable)	3.906e-04	1.100e-03
S3 (output stable)	3.103e-04	8.873e-04
D0 to Z	2.930e-03	8.296e-03
D1 to Z	2.493e-03	7.103e-03
D2 to Z	2.682e-03	7.374e-03
D3 to Z	2.259e-03	6.213e-03
S0 to Z	2.819e-03	7.745e-03
S1 to Z	2.398e-03	6.627e-03
S2 to Z	2.599e-03	6.876e-03
S3 to Z	2.184e-03	5.721e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X4_P4	X15_P4
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description	Logical Symbol
2 input NAND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P4	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P4	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P4	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P4	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P4	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P4	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P4	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P4	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P4	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P4	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P4	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P4	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P4	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P4	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P4	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P4	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P4	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P4	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P4	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P4	C8T28SOI_LL_-NAND2X4_P4	C8T28SOI_LL_-NAND2X8_P4	C8T28SOI_LL_-NAND2X12_P4
A	0.0004	0.0005	0.0011	0.0015
B	0.0004	0.0005	0.0010	0.0014
	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X24_P4	C8T28SOI_-LLBR0P8_-NAND2X4_P4
A	0.0020	0.0026	0.0007	0.0006
B	0.0019	0.0024	0.0006	0.0005
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	C8T28SOI_-LLBR0P8_-NAND2X12_P4	C8T28SOI_-LLBR0P8_-NAND2X16_P4	C8T28SOI_LLS_-NAND2X8_P4
A	0.0011	0.0016	0.0021	0.0010
B	0.0009	0.0014	0.0018	0.0009
	C8T28SOI_LLS_-NAND2X15_P4	C8T28SOI_LLS_-NAND2X23_P4	C8T28SOI_LLS_-NAND2X31_P4	C8T28SOIDV_LL_-NAND2X9_P4
A	0.0021	0.0032	0.0042	0.0011
B	0.0019	0.0029	0.0039	0.0011
	C8T28SOIDV_LL_-NAND2X18_P4	C8T28SOIDV_LL_-NAND2X27_P4	C8T28SOIDV_LL_-NAND2X36_P4	
A	0.0022	0.0032	0.0044	
B	0.0020	0.0031	0.0041	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND2X2_P4	**C8T28SOI_LL_-NAND2X4_P4**	**C8T28SOI_LL_-NAND2X2_P4**	**C8T28SOI_LL_-NAND2X4_P4**
A to Z ↓	0.0091	0.0079	9.0967	5.0101
A to Z ↑	0.0139	0.0116	8.4260	4.4465
B to Z ↓	0.0103	0.0086	9.1916	5.0665
B to Z ↑	0.0129	0.0103	8.4718	4.5039
	C8T28SOI_LL_-NAND2X8_P4	**C8T28SOI_LL_-NAND2X12_P4**	**C8T28SOI_LL_-NAND2X8_P4**	**C8T28SOI_LL_-NAND2X12_P4**
A to Z ↓	0.0088	0.0084	2.5569	1.7534
A to Z ↑	0.0117	0.0114	2.1154	1.4456
B to Z ↓	0.0080	0.0084	2.5880	1.7751
B to Z ↑	0.0091	0.0093	2.1322	1.4671

	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4
A to Z ↓	0.0086	0.0085	1.3294	1.0746
A to Z ↑	0.0115	0.0115	1.0883	0.8821
B to Z ↓	0.0081	0.0085	1.3478	1.0894
B to Z ↑	0.0089	0.0092	1.1034	0.8953
	C8T28SOI_LL_-NAND2X24_P4	**C8T28SOI_-LLBR0P8_-NAND2X4_P4**	**C8T28SOI_LL_-NAND2X24_P4**	**C8T28SOI_-LLBR0P8_-NAND2X4_P4**
A to Z ↓	0.0310	0.0065	0.6019	3.5581
A to Z ↑	0.0322	0.0148	0.8561	5.6274
B to Z ↓	0.0321	0.0066	0.6023	3.6216
B to Z ↑	0.0308	0.0126	0.8572	5.6575
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	**C8T28SOI_-LLBR0P8_-NAND2X12_P4**	**C8T28SOI_-LLBR0P8_-NAND2X8_P4**	**C8T28SOI_-LLBR0P8_-NAND2X12_P4**
A to Z ↓	0.0072	0.0071	1.9682	1.3489
A to Z ↑	0.0148	0.0148	2.8338	1.9200
B to Z ↓	0.0057	0.0064	2.0079	1.3747
B to Z ↑	0.0110	0.0115	2.8581	1.9355
	C8T28SOI_-LLBR0P8_-NAND2X16_P4	**C8T28SOI_LLS_-NAND2X8_P4**	**C8T28SOI_-LLBR0P8_-NAND2X16_P4**	**C8T28SOI_LLS_-NAND2X8_P4**
A to Z ↓	0.0069	0.0088	1.0309	2.5503
A to Z ↑	0.0143	0.0118	1.4360	2.1444
B to Z ↓	0.0056	0.0080	1.0513	2.5815
B to Z ↑	0.0106	0.0092	1.4527	2.1745
	C8T28SOI_LLS_-NAND2X15_P4	**C8T28SOI_LLS_-NAND2X23_P4**	**C8T28SOI_LLS_-NAND2X15_P4**	**C8T28SOI_LLS_-NAND2X23_P4**
A to Z ↓	0.0087	0.0087	1.3261	0.8958
A to Z ↑	0.0115	0.0114	1.0701	0.7138
B to Z ↓	0.0082	0.0084	1.3446	0.9079
B to Z ↑	0.0089	0.0090	1.0793	0.7204
	C8T28SOI_LLS_-NAND2X31_P4	**C8T28SOIDV_LL_-NAND2X9_P4**	**C8T28SOI_LLS_-NAND2X31_P4**	**C8T28SOIDV_LL_-NAND2X9_P4**
A to Z ↓	0.0087	0.0074	0.6788	1.9592
A to Z ↑	0.0114	0.0121	0.5374	2.0659
B to Z ↓	0.0085	0.0076	0.6877	1.9831
B to Z ↑	0.0090	0.0104	0.5424	2.1057
	C8T28SOIDV_LL_-NAND2X18_P4	**C8T28SOIDV_LL_-NAND2X27_P4**	**C8T28SOIDV_LL_-NAND2X18_P4**	**C8T28SOIDV_LL_-NAND2X27_P4**
A to Z ↓	0.0080	0.0080	1.0008	0.6827
A to Z ↑	0.0124	0.0124	1.0389	0.7020
B to Z ↓	0.0071	0.0078	1.0155	0.6927
B to Z ↑	0.0096	0.0101	1.0472	0.7073
	C8T28SOIDV_LL_-NAND2X36_P4		**C8T28SOIDV_LL_-NAND2X36_P4**	
A to Z ↓	0.0081		0.5143	
A to Z ↑	0.0123		0.5256	
B to Z ↓	0.0073		0.5224	
B to Z ↑	0.0095		0.5302	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P4	3.272e-07	1.000e-20
C8T28SOI_LL_NAND2X4_P4	8.380e-07	1.000e-20
C8T28SOI_LL_NAND2X8_P4	1.691e-06	1.000e-20
C8T28SOI_LL_NAND2X12_P4	2.427e-06	1.000e-20
C8T28SOI_LL_NAND2X15_P4	3.167e-06	1.000e-20
C8T28SOI_LL_NAND2X19_P4	3.906e-06	1.000e-20
C8T28SOI_LL_NAND2X24_P4	5.789e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P4	8.009e-07	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P4	1.418e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_P4	2.007e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_P4	2.600e-06	1.000e-20
C8T28SOI_LLS_NAND2X8_P4	1.691e-06	1.000e-20
C8T28SOI_LLS_NAND2X15_P4	3.167e-06	1.000e-20
C8T28SOI_LLS_NAND2X23_P4	4.646e-06	1.000e-20
C8T28SOI_LLS_NAND2X31_P4	6.126e-06	1.000e-20
C8T28SOIDV_LL_NAND2X9_P4	2.074e-06	1.000e-20
C8T28SOIDV_LL_NAND2X18_P4	3.931e-06	1.000e-20
C8T28SOIDV_LL_NAND2X27_P4	5.692e-06	1.000e-20
C8T28SOIDV_LL_NAND2X36_P4	7.456e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P4	C8T28SOI_LL_-NAND2X4_P4	C8T28SOI_LL_-NAND2X8_P4	C8T28SOI_LL_-NAND2X12_P4
A (output stable)	8.579e-06	1.555e-05	6.364e-05	8.300e-05
B (output stable)	2.261e-05	4.152e-05	2.615e-04	2.825e-04
A to Z	4.577e-04	7.005e-04	1.545e-03	2.216e-03
B to Z	3.968e-04	5.840e-04	1.118e-03	1.721e-03
	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X24_P4	C8T28SOI_-LLBR0P8_-NAND2X4_P4
A (output stable)	1.200e-04	1.370e-04	1.825e-05	2.250e-05
B (output stable)	4.626e-04	4.519e-04	4.734e-05	5.918e-05
A to Z	2.977e-03	3.660e-03	6.912e-03	7.878e-04
B to Z	2.198e-03	2.830e-03	6.797e-03	6.242e-04
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	C8T28SOI_-LLBR0P8_-NAND2X12_P4	C8T28SOI_-LLBR0P8_-NAND2X16_P4	C8T28SOI_LLS_-NAND2X8_P4
A (output stable)	7.822e-05	9.768e-05	1.523e-04	6.453e-05
B (output stable)	3.176e-04	3.446e-04	5.629e-04	2.686e-04
A to Z	1.617e-03	2.392e-03	3.029e-03	1.554e-03
B to Z	1.047e-03	1.697e-03	1.988e-03	1.127e-03
	C8T28SOI_LLS_-NAND2X15_P4	C8T28SOI_LLS_-NAND2X23_P4	C8T28SOI_LLS_-NAND2X31_P4	C8T28SOIDV_LL_-NAND2X9_P4
A (output stable)	1.249e-04	1.843e-04	2.402e-04	4.029e-05
B (output stable)	4.757e-04	6.529e-04	8.353e-04	1.063e-04
A to Z	3.012e-03	4.486e-03	5.947e-03	1.647e-03
B to Z	2.225e-03	3.358e-03	4.487e-03	1.352e-03
	C8T28SOIDV_LL_-NAND2X18_P4	C8T28SOIDV_LL_-NAND2X27_P4	C8T28SOIDV_LL_-NAND2X36_P4	
A (output stable)	1.389e-04	1.782e-04	2.784e-04	
B (output stable)	6.014e-04	5.596e-04	1.167e-03	
A to Z	3.425e-03	5.061e-03	6.749e-03	

B to Z	2.465e-03	3.970e-03	4.883e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

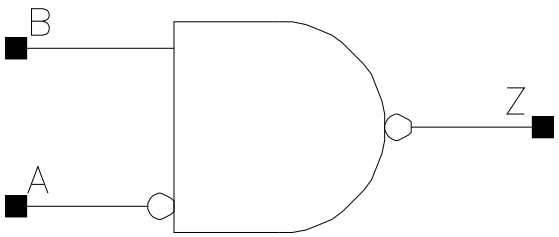
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P4	C8T28SOI_LL_-NAND2X4_P4	C8T28SOI_LL_-NAND2X8_P4	C8T28SOI_LL_-NAND2X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X24_P4	C8T28SOI_-LLBR0P8_-NAND2X4_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	C8T28SOI_-LLBR0P8_-NAND2X12_P4	C8T28SOI_-LLBR0P8_-NAND2X16_P4	C8T28SOI_LLS_-NAND2X8_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P4	C8T28SOI_LLS_-NAND2X23_P4	C8T28SOI_LLS_-NAND2X31_P4	C8T28SOIDV_LL_-NAND2X9_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P4	C8T28SOIDV_LL_-NAND2X27_P4	C8T28SOIDV_LL_-NAND2X36_P4	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.544	0.4352
X4_P4	0.800	0.680	0.5440
X9_P4	1.600	0.544	0.8704
X13_P4	1.600	0.816	1.3056
X17_P4	1.600	0.816	1.3056
X23_P4	0.800	2.312	1.8496
X27_P4	1.600	1.088	1.7408
X31_P4	0.800	2.992	2.3936
X36_P4	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P4	X4_P4	X9_P4	X13_P4
A	0.0005	0.0005	0.0009	0.0009
B	0.0004	0.0005	0.0010	0.0016
	X17_P4	X23_P4	X27_P4	X31_P4
A	0.0009	0.0019	0.0015	0.0025
B	0.0020	0.0029	0.0031	0.0037
	X36_P4			
A	0.0014			
B	0.0041			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X4_P4**	**X2_P4**	**X4_P4**
A to Z ↓	0.0236	0.0243	9.0476	5.0335
A to Z ↑	0.0180	0.0184	8.1904	4.2806
B to Z ↓	0.0106	0.0088	9.2960	5.1712
B to Z ↑	0.0129	0.0102	8.4759	4.5002
	X9_P4	**X13_P4**	**X9_P4**	**X13_P4**
A to Z ↓	0.0240	0.0289	1.9894	1.2613
A to Z ↑	0.0178	0.0216	2.0181	1.3628
B to Z ↓	0.0079	0.0077	2.0547	1.3029
B to Z ↑	0.0104	0.0107	2.1206	1.4503
	X17_P4	**X23_P4**	**X17_P4**	**X23_P4**
A to Z ↓	0.0313	0.0232	0.9952	0.8852
A to Z ↑	0.0225	0.0184	1.0354	0.7076
B to Z ↓	0.0075	0.0082	1.0252	0.9126
B to Z ↑	0.0101	0.0090	1.1074	0.7417
	X27_P4	**X31_P4**	**X27_P4**	**X31_P4**
A to Z ↓	0.0267	0.0231	0.6738	0.6697
A to Z ↑	0.0202	0.0184	0.6890	0.5155
B to Z ↓	0.0074	0.0084	0.6965	0.6897
B to Z ↑	0.0097	0.0091	0.7111	0.5579
	X36_P4		**X36_P4**	
A to Z ↓	0.0304		0.5096	
A to Z ↑	0.0229		0.5170	
B to Z ↓	0.0073		0.5248	
B to Z ↑	0.0094		0.5341	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P4	6.050e-07	1.000e-20
X4_P4	1.165e-06	1.000e-20
X9_P4	3.065e-06	1.000e-20
X13_P4	3.554e-06	1.000e-20
X17_P4	4.694e-06	1.000e-20
X23_P4	7.058e-06	1.000e-20
X27_P4	7.603e-06	1.000e-20
X31_P4	9.259e-06	1.000e-20
X36_P4	9.428e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P4	X4_P4	X9_P4	X13_P4
A (output stable)	6.701e-04	8.365e-04	1.602e-03	2.316e-03
B (output stable)	2.333e-05	4.206e-05	1.110e-04	2.895e-04
A to Z	1.131e-03	1.522e-03	3.235e-03	5.102e-03
B to Z	3.988e-04	5.805e-04	1.366e-03	2.079e-03
	X17_P4	X23_P4	X27_P4	X31_P4
A (output stable)	2.606e-03	4.151e-03	4.130e-03	5.538e-03
B (output stable)	3.472e-04	5.996e-04	5.685e-04	8.074e-04
A to Z	6.085e-03	8.727e-03	9.002e-03	1.166e-02
B to Z	2.569e-03	3.350e-03	3.762e-03	4.435e-03
	X36_P4			
A (output stable)	5.305e-03			

B (output stable)	8.814e-04			
A to Z	1.186e-02			
B to Z	4.835e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

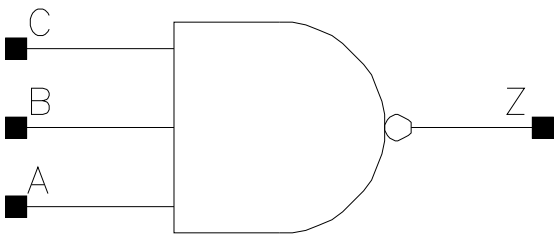
Pin Cycle (vdds)	X2_P4	X4_P4	X9_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P4	X23_P4	X27_P4	X31_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P4	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P4	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P4	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P4	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P4	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P4	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P4	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P4	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P4	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P4	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P4	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P4	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P4	C8T28SOI_LL_-NAND3X7_P4	C8T28SOI_LL_-NAND3X10_P4	C8T28SOI_LL_-NAND3X14_P4
A	0.0005	0.0010	0.0016	0.0020
B	0.0005	0.0010	0.0015	0.0019
C	0.0005	0.0010	0.0014	0.0019
	C8T28SOI_LL_-NAND3X20_P4	C8T28SOI_LL_-NAND3X27_P4	C8T28SOI_-LLBR0P6_-NAND3X3_P4	C8T28SOI_-LLBR0P6_-NAND3X7_P4
A	0.0030	0.0042	0.0007	0.0011
B	0.0029	0.0039	0.0005	0.0010
C	0.0028	0.0037	0.0005	0.0009
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	C8T28SOI_-LLBR0P6_-NAND3X14_P4	C8T28SOI_-LLBR0P6_-NAND3X20_P4	C8T28SOI_-LLBR0P6_-NAND3X27_P4
A	0.0016	0.0021	0.0031	0.0041
B	0.0014	0.0019	0.0028	0.0038
C	0.0014	0.0019	0.0028	0.0037

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND3X3_P4	**C8T28SOI_LL_-NAND3X7_P4**	**C8T28SOI_LL_-NAND3X3_P4**	**C8T28SOI_LL_-NAND3X7_P4**
A to Z ↓	0.0118	0.0134	7.2310	3.6686
A to Z ↑	0.0144	0.0149	4.4920	2.2011
B to Z ↓	0.0125	0.0132	7.2686	3.6877
B to Z ↑	0.0133	0.0135	4.5166	2.2069
C to Z ↓	0.0128	0.0121	7.3061	3.7065
C to Z ↑	0.0120	0.0111	4.5594	2.1369
	C8T28SOI_LL_-NAND3X10_P4	**C8T28SOI_LL_-NAND3X14_P4**	**C8T28SOI_LL_-NAND3X10_P4**	**C8T28SOI_LL_-NAND3X14_P4**
A to Z ↓	0.0127	0.0131	2.5317	1.9153
A to Z ↑	0.0140	0.0143	1.4177	1.1107
B to Z ↓	0.0131	0.0129	2.5452	1.9253
B to Z ↑	0.0128	0.0129	1.4665	1.1112
C to Z ↓	0.0122	0.0121	2.5596	1.9366
C to Z ↑	0.0108	0.0107	1.4777	1.1008
	C8T28SOI_LL_-NAND3X20_P4	**C8T28SOI_LL_-NAND3X27_P4**	**C8T28SOI_LL_-NAND3X20_P4**	**C8T28SOI_LL_-NAND3X27_P4**
A to Z ↓	0.0127	0.0128	1.3046	0.9932
A to Z ↑	0.0138	0.0138	0.7146	0.5397
B to Z ↓	0.0131	0.0131	1.3116	0.9985
B to Z ↑	0.0126	0.0125	0.7153	0.5386
C to Z ↓	0.0121	0.0122	1.3193	1.0043
C to Z ↑	0.0105	0.0105	0.7370	0.5554
	C8T28SOI_-LLBR0P6_-NAND3X3_P4	**C8T28SOI_-LLBR0P6_-NAND3X7_P4**	**C8T28SOI_-LLBR0P6_-NAND3X3_P4**	**C8T28SOI_-LLBR0P6_-NAND3X7_P4**
A to Z ↓	0.0087	0.0108	4.5625	2.5817
A to Z ↑	0.0199	0.0214	6.6505	3.3911
B to Z ↓	0.0086	0.0100	4.6215	2.6064
B to Z ↑	0.0175	0.0186	6.6554	3.4006

C to Z ↓	0.0081	0.0081	4.6829	2.6387
C to Z ↑	0.0148	0.0145	6.7065	3.3682
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	**C8T28SOI_-LLBR0P6_-NAND3X14_P4**	**C8T28SOI_-LLBR0P6_-NAND3X10_P4**	**C8T28SOI_-LLBR0P6_-NAND3X14_P4**
A to Z ↓	0.0097	0.0104	1.7217	1.3116
A to Z ↑	0.0202	0.0207	2.2617	1.7150
B to Z ↓	0.0092	0.0093	1.7408	1.3259
B to Z ↑	0.0173	0.0177	2.2709	1.7179
C to Z ↓	0.0077	0.0075	1.7640	1.3444
C to Z ↑	0.0137	0.0135	2.2891	1.7157
	C8T28SOI_-LLBR0P6_-NAND3X20_P4	**C8T28SOI_-LLBR0P6_-NAND3X27_P4**	**C8T28SOI_-LLBR0P6_-NAND3X20_P4**	**C8T28SOI_-LLBR0P6_-NAND3X27_P4**
A to Z ↓	0.0099	0.0100	0.8872	0.6813
A to Z ↑	0.0202	0.0202	1.1410	0.8617
B to Z ↓	0.0094	0.0093	0.8969	0.6886
B to Z ↑	0.0174	0.0173	1.1433	0.8614
C to Z ↓	0.0074	0.0075	0.9097	0.6981
C to Z ↑	0.0131	0.0131	1.1513	0.8663

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P4	6.520e-07	1.000e-20
C8T28SOI_LL_NAND3X7_P4	1.360e-06	1.000e-20
C8T28SOI_LL_NAND3X10_P4	1.892e-06	1.000e-20
C8T28SOI_LL_NAND3X14_P4	2.529e-06	1.000e-20
C8T28SOI_LL_NAND3X20_P4	3.699e-06	1.000e-20
C8T28SOI_LL_NAND3X27_P4	4.868e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P4	5.963e-07	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P4	1.133e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_P4	1.499e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_P4	2.034e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_P4	2.935e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_P4	3.835e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P4	C8T28SOI_LL_-NAND3X7_P4	C8T28SOI_LL_-NAND3X10_P4	C8T28SOI_LL_-NAND3X14_P4
A (output stable)	1.420e-05	4.718e-05	6.076e-05	8.772e-05
B (output stable)	4.509e-05	1.523e-04	2.154e-04	2.879e-04
C (output stable)	8.440e-05	3.112e-04	4.025e-04	5.642e-04
A to Z	1.006e-03	2.280e-03	3.166e-03	4.305e-03
B to Z	8.775e-04	1.887e-03	2.611e-03	3.531e-03
C to Z	7.631e-04	1.499e-03	2.096e-03	2.807e-03
	C8T28SOI_LL_-NAND3X20_P4	C8T28SOI_LL_-NAND3X27_P4	C8T28SOI_-LLBR0P6_-NAND3X3_P4	C8T28SOI_-LLBR0P6_-NAND3X7_P4
A (output stable)	1.167e-04	1.595e-04	2.309e-05	6.506e-05
B (output stable)	4.203e-04	5.549e-04	7.198e-05	2.082e-04
C (output stable)	8.459e-04	1.088e-03	1.373e-04	4.494e-04

A to Z	6.240e-03	8.295e-03	1.091e-03	2.503e-03
B to Z	5.172e-03	6.835e-03	8.831e-04	1.934e-03
C to Z	4.027e-03	5.372e-03	6.798e-04	1.348e-03
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	C8T28SOI_-LLBR0P6_-NAND3X14_P4	C8T28SOI_-LLBR0P6_-NAND3X20_P4	C8T28SOI_-LLBR0P6_-NAND3X27_P4
A (output stable)	8.303e-05	1.311e-04	1.682e-04	2.306e-04
B (output stable)	2.889e-04	4.191e-04	5.961e-04	7.924e-04
C (output stable)	5.717e-04	8.274e-04	1.216e-03	1.566e-03
A to Z	3.378e-03	4.702e-03	6.762e-03	8.959e-03
B to Z	2.543e-03	3.512e-03	5.084e-03	6.682e-03
C to Z	1.807e-03	2.373e-03	3.403e-03	4.514e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

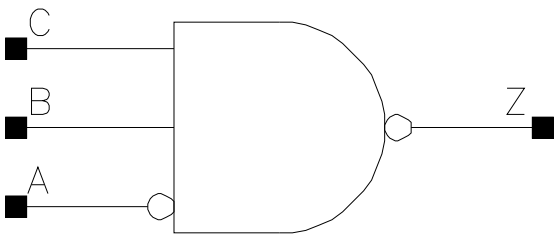
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P4	C8T28SOI_LL_-NAND3X7_P4	C8T28SOI_LL_-NAND3X10_P4	C8T28SOI_LL_-NAND3X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P4	C8T28SOI_LL_-NAND3X27_P4	C8T28SOI_-LLBR0P6_-NAND3X3_P4	C8T28SOI_-LLBR0P6_-NAND3X7_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	C8T28SOI_-LLBR0P6_-NAND3X14_P4	C8T28SOI_-LLBR0P6_-NAND3X20_P4	C8T28SOI_-LLBR0P6_-NAND3X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X7_P4	0.800	1.360	1.0880
X10_P4	0.800	1.632	1.3056
X14_P4	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X10_P4	X14_P4
A	0.0006	0.0009	0.0008	0.0008
B	0.0005	0.0010	0.0015	0.0020
C	0.0005	0.0010	0.0014	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0292	0.0285	7.2155	3.6802
A to Z ↑	0.0207	0.0211	4.2873	2.0663
B to Z ↓	0.0122	0.0130	7.3138	3.7250
B to Z ↑	0.0129	0.0130	4.5227	2.1440
C to Z ↓	0.0124	0.0117	7.3554	3.7433
C to Z ↑	0.0116	0.0106	4.5620	2.1411
	X10_P4	**X14_P4**	**X10_P4**	**X14_P4**
A to Z ↓	0.0314	0.0340	2.5160	1.9197

A to Z ↑	0.0235	0.0257	1.4157	1.0584
B to Z ↓	0.0130	0.0126	2.5436	1.9399
B to Z ↑	0.0127	0.0125	1.4684	1.0979
C to Z ↓	0.0121	0.0117	2.5578	1.9506
C to Z ↑	0.0108	0.0103	1.4809	1.1021

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	9.316e-07	1.000e-20
X7_P4	2.187e-06	1.000e-20
X10_P4	2.770e-06	1.000e-20
X14_P4	3.409e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	8.441e-04	1.548e-03	1.972e-03	2.393e-03
B (output stable)	4.507e-05	1.079e-04	1.702e-04	2.165e-04
C (output stable)	8.547e-05	3.287e-04	4.150e-04	5.788e-04
A to Z	1.816e-03	3.840e-03	5.352e-03	6.853e-03
B to Z	8.334e-04	1.805e-03	2.602e-03	3.395e-03
C to Z	7.138e-04	1.393e-03	2.083e-03	2.656e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

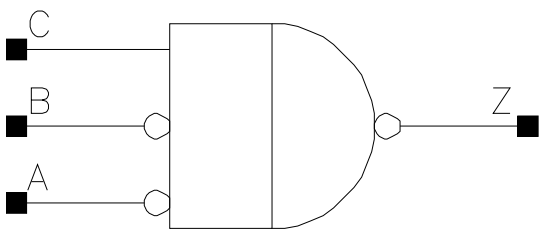
Pin Cycle (vdds)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	0.816	0.6528
X8_P4	0.800	1.088	0.8704
X12_P4	0.800	1.632	1.3056
X15_P4	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X12_P4	X15_P4
A	0.0006	0.0006	0.0012	0.0011
B	0.0007	0.0007	0.0012	0.0012
C	0.0005	0.0010	0.0014	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0260	0.0318	4.7189	2.5285
A to Z ↑	0.0178	0.0206	4.0891	2.0396
B to Z ↓	0.0267	0.0326	4.7191	2.5289
B to Z ↑	0.0166	0.0196	4.0870	2.0393
C to Z ↓	0.0089	0.0081	4.8403	2.5836
C to Z ↑	0.0103	0.0093	4.1694	2.1523
	X12_P4	**X15_P4**	**X12_P4**	**X15_P4**
A to Z ↓	0.0293	0.0321	1.7272	1.3176
A to Z ↑	0.0191	0.0225	1.3624	1.0264
B to Z ↓	0.0282	0.0312	1.7279	1.3184

B to Z ↑	0.0173	0.0207	1.3601	1.0251
C to Z ↓	0.0089	0.0081	1.7691	1.3509
C to Z ↑	0.0098	0.0089	1.4633	1.0769

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	1.594e-06	1.000e-20
X8_P4	2.094e-06	1.000e-20
X12_P4	3.312e-06	1.000e-20
X15_P4	3.715e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	4.642e-04	6.265e-04	1.068e-03	1.222e-03
B (output stable)	4.079e-04	5.667e-04	8.847e-04	1.035e-03
C (output stable)	4.567e-05	2.612e-04	2.883e-04	4.465e-04
A to Z	2.108e-03	3.467e-03	5.480e-03	6.649e-03
B to Z	1.944e-03	3.295e-03	4.900e-03	6.086e-03
C to Z	6.537e-04	1.147e-03	1.840e-03	2.235e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

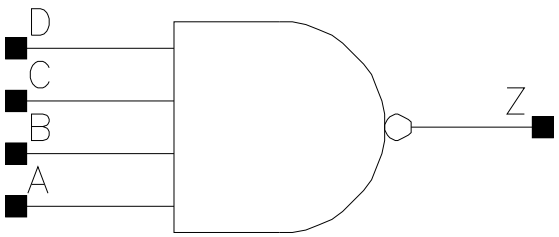
Pin Cycle (vdds)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.224	0.9792
X10_P4	0.800	1.360	1.0880
X14_P4	0.800	1.904	1.5232
X18_P4	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X18_P4
A	0.0004	0.0004	0.0005	0.0006
B	0.0005	0.0005	0.0006	0.0008
C	0.0004	0.0004	0.0005	0.0006
D	0.0005	0.0005	0.0006	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0413	0.0388	2.8793	1.4530
A to Z ↑	0.0344	0.0351	4.1258	2.0936
B to Z ↓	0.0430	0.0408	2.8784	1.4533
B to Z ↑	0.0334	0.0346	4.1267	2.0949
C to Z ↓	0.0428	0.0398	2.8807	1.4538
C to Z ↑	0.0360	0.0373	4.1215	2.0936

D to Z ↓	0.0450	0.0420	2.8796	1.4535
D to Z ↑	0.0356	0.0369	4.1247	2.0934
	X14_P4	**X18_P4**	**X14_P4**	**X18_P4**
A to Z ↓	0.0417	0.0389	1.0037	0.8087
A to Z ↑	0.0352	0.0342	1.4390	1.1363
B to Z ↓	0.0437	0.0406	1.0043	0.8093
B to Z ↑	0.0341	0.0335	1.4392	1.1355
C to Z ↓	0.0403	0.0358	1.0028	0.8092
C to Z ↑	0.0357	0.0336	1.4354	1.1340
D to Z ↓	0.0423	0.0373	1.0035	0.8090
D to Z ↑	0.0350	0.0325	1.4355	1.1325

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.452e-06	1.000e-20
X10_P4	2.330e-06	1.000e-20
X14_P4	3.340e-06	1.000e-20
X18_P4	4.631e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	3.418e-04	4.104e-04	6.063e-04	6.686e-04
B (output stable)	3.252e-04	3.929e-04	5.809e-04	6.450e-04
C (output stable)	3.721e-04	4.133e-04	6.327e-04	6.318e-04
D (output stable)	3.540e-04	3.948e-04	6.041e-04	5.985e-04
A to Z	2.546e-03	3.613e-03	5.633e-03	6.542e-03
B to Z	2.487e-03	3.553e-03	5.542e-03	6.453e-03
C to Z	2.692e-03	3.686e-03	5.333e-03	6.068e-03
D to Z	2.646e-03	3.631e-03	5.252e-03	5.963e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

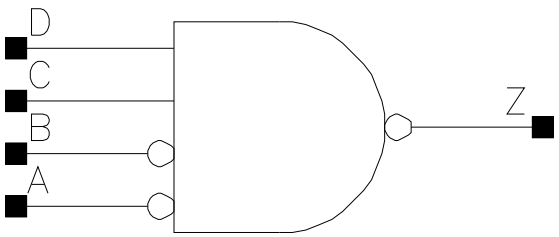
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.952	0.7616
X7_P4	0.800	1.360	1.0880
X10_P4	0.800	2.040	1.6320
X14_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P4	X7_P4	X10_P4	X14_P4
A	0.0007	0.0007	0.0012	0.0011
B	0.0007	0.0007	0.0013	0.0012
C	0.0007	0.0010	0.0015	0.0019
D	0.0005	0.0010	0.0014	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X7_P4	X3_P4	X7_P4
A to Z ↓	0.0298	0.0348	6.9318	3.6815
A to Z ↑	0.0193	0.0223	4.1362	2.0743
B to Z ↓	0.0300	0.0354	6.9377	3.6819
B to Z ↑	0.0180	0.0209	4.1360	2.0730
C to Z ↓	0.0125	0.0129	7.0366	3.7173
C to Z ↑	0.0133	0.0129	4.3243	2.1472

D to Z ↓	0.0124	0.0116	7.0632	3.7360
D to Z ↑	0.0116	0.0105	4.3240	2.1415
	X10_P4	**X14_P4**	**X10_P4**	**X14_P4**
A to Z ↓	0.0330	0.0358	2.5155	1.9250
A to Z ↑	0.0206	0.0254	1.4012	1.0347
B to Z ↓	0.0319	0.0353	2.5157	1.9248
B to Z ↑	0.0188	0.0238	1.3988	1.0328
C to Z ↓	0.0129	0.0127	2.5397	1.9424
C to Z ↑	0.0127	0.0125	1.4693	1.0994
D to Z ↓	0.0120	0.0117	2.5546	1.9533
D to Z ↑	0.0107	0.0103	1.4814	1.1042

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	1.410e-06	1.000e-20
X7_P4	1.775e-06	1.000e-20
X10_P4	2.913e-06	1.000e-20
X14_P4	3.115e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	5.647e-04	7.564e-04	1.354e-03	1.563e-03
B (output stable)	4.954e-04	6.852e-04	1.113e-03	1.337e-03
C (output stable)	8.714e-05	1.511e-04	2.323e-04	3.001e-04
D (output stable)	1.473e-04	3.570e-04	4.619e-04	6.189e-04
A to Z	2.469e-03	4.034e-03	6.381e-03	8.007e-03
B to Z	2.313e-03	3.873e-03	5.811e-03	7.479e-03
C to Z	8.962e-04	1.793e-03	2.578e-03	3.394e-03
D to Z	7.796e-04	1.382e-03	2.061e-03	2.670e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

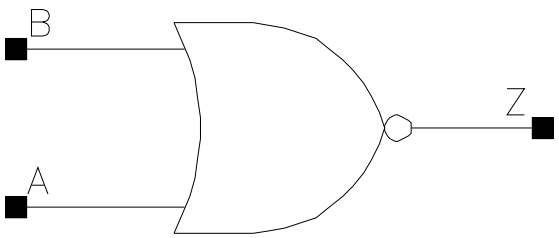
Pin Cycle (vdds)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.408	0.3264
X4_P4	0.800	0.408	0.3264
X8_P4	0.800	0.680	0.5440
X9_P4	1.600	0.408	0.6528
X12_P4	0.800	0.952	0.7616
X16_P4	0.800	1.224	0.9792
X19_P4	1.600	0.680	1.0880
X20_P4	0.800	1.496	1.1968
X23_P4	0.800	1.496	1.1968
X24_P4	0.800	1.768	1.4144
X27_P4	0.800	1.632	1.3056
X29_P4	1.600	0.952	1.5232
X31_P4	0.800	2.312	1.8496
X34_P4	0.800	2.040	1.6320
X38_P4	0.800	2.176	1.7408
X39_P4	1.600	1.224	1.9584
X46_P4	1.600	1.224	1.9584
X57_P4	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P4	X4_P4	X8_P4	X9_P4
A	0.0004	0.0005	0.0010	0.0011
B	0.0004	0.0005	0.0010	0.0011
	X12_P4	X16_P4	X19_P4	X20_P4

A	0.0016	0.0020	0.0022	0.0026
B	0.0014	0.0019	0.0021	0.0023
	X23_P4	X24_P4	X27_P4	X29_P4
A	0.0007	0.0031	0.0007	0.0033
B	0.0006	0.0029	0.0006	0.0031
	X31_P4	X34_P4	X38_P4	X39_P4
A	0.0041	0.0007	0.0007	0.0044
B	0.0038	0.0006	0.0006	0.0041
	X46_P4	X57_P4		
A	0.0007	0.0007		
B	0.0008	0.0008		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X4_P4**	**X2_P4**	**X4_P4**
A to Z ↓	0.0085	0.0080	5.6735	3.1120
A to Z ↑	0.0159	0.0142	15.9864	8.7049
B to Z ↓	0.0074	0.0067	5.7137	3.1402
B to Z ↑	0.0165	0.0144	16.0555	8.7348
	X8_P4	**X9_P4**	**X8_P4**	**X9_P4**
A to Z ↓	0.0075	0.0067	1.5042	1.1945
A to Z ↑	0.0135	0.0131	4.1306	3.9352
B to Z ↓	0.0051	0.0055	1.5076	1.2390
B to Z ↑	0.0112	0.0132	4.1528	3.9516
	X12_P4	**X16_P4**	**X12_P4**	**X16_P4**
A to Z ↓	0.0076	0.0076	1.0320	0.7671
A to Z ↑	0.0130	0.0134	2.7109	2.0736
B to Z ↓	0.0056	0.0054	1.0429	0.7761
B to Z ↑	0.0116	0.0113	2.7267	2.0857
	X19_P4	**X20_P4**	**X19_P4**	**X20_P4**
A to Z ↓	0.0073	0.0078	0.6043	0.6306
A to Z ↑	0.0148	0.0131	2.0153	1.6460
B to Z ↓	0.0056	0.0058	0.6107	0.6378
B to Z ↑	0.0131	0.0117	2.0248	1.6563
	X23_P4	**X24_P4**	**X23_P4**	**X24_P4**
A to Z ↓	0.0284	0.0077	0.6302	0.5222
A to Z ↑	0.0389	0.0131	0.8619	1.3895
B to Z ↓	0.0268	0.0055	0.6307	0.5286
B to Z ↑	0.0392	0.0113	0.8631	1.3979
	X27_P4	**X29_P4**	**X27_P4**	**X29_P4**
A to Z ↓	0.0297	0.0070	0.5259	0.3997
A to Z ↑	0.0401	0.0138	0.7210	1.3546
B to Z ↓	0.0282	0.0053	0.5259	0.4039
B to Z ↑	0.0405	0.0127	0.7214	1.3603
	X31_P4	**X34_P4**	**X31_P4**	**X34_P4**
A to Z ↓	0.0078	0.0311	0.3896	0.4317
A to Z ↑	0.0133	0.0450	1.0422	0.5903
B to Z ↓	0.0057	0.0296	0.3948	0.4313
B to Z ↑	0.0115	0.0458	1.0488	0.5907
	X38_P4	**X39_P4**	**X38_P4**	**X39_P4**
A to Z ↓	0.0318	0.0071	0.3757	0.3049
A to Z ↑	0.0456	0.0141	0.5176	1.0161

B to Z ↓	0.0303	0.0053	0.3758	0.3090
B to Z ↑	0.0463	0.0126	0.5181	1.0213
	X46_P4	**X57_P4**	**X46_P4**	**X57_P4**
A to Z ↓	0.0357	0.0385	0.2861	0.2344
A to Z ↑	0.0472	0.0494	0.5136	0.4131
B to Z ↓	0.0345	0.0373	0.2858	0.2345
B to Z ↑	0.0485	0.0507	0.5132	0.4131

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P4	3.274e-07	1.000e-20
X4_P4	8.080e-07	1.000e-20
X8_P4	1.712e-06	1.000e-20
X9_P4	2.081e-06	1.000e-20
X12_P4	2.461e-06	1.000e-20
X16_P4	3.213e-06	1.000e-20
X19_P4	3.954e-06	1.000e-20
X20_P4	3.965e-06	1.000e-20
X23_P4	6.721e-06	1.000e-20
X24_P4	4.717e-06	1.000e-20
X27_P4	7.651e-06	1.000e-20
X29_P4	5.732e-06	1.000e-20
X31_P4	6.222e-06	1.000e-20
X34_P4	9.270e-06	1.000e-20
X38_P4	1.016e-05	1.000e-20
X39_P4	7.514e-06	1.000e-20
X46_P4	1.108e-05	1.000e-20
X57_P4	1.309e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P4	X4_P4	X8_P4	X9_P4
A (output stable)	1.484e-05	2.560e-05	9.857e-05	5.602e-05
B (output stable)	8.812e-06	2.063e-05	9.254e-05	5.042e-05
A to Z	4.687e-04	7.739e-04	1.547e-03	1.593e-03
B to Z	3.873e-04	6.230e-04	1.016e-03	1.297e-03
	X12_P4	X16_P4	X19_P4	X20_P4
A (output stable)	1.380e-04	1.939e-04	2.056e-04	2.335e-04
B (output stable)	1.263e-04	1.712e-04	2.015e-04	1.989e-04
A to Z	2.277e-03	3.068e-03	3.524e-03	3.827e-03
B to Z	1.608e-03	2.079e-03	2.590e-03	2.685e-03
	X23_P4	X24_P4	X27_P4	X29_P4
A (output stable)	2.786e-05	2.833e-04	2.797e-05	2.676e-04
B (output stable)	2.355e-05	2.350e-04	2.366e-05	2.423e-04
A to Z	6.887e-03	4.529e-03	7.722e-03	4.905e-03
B to Z	6.732e-03	3.111e-03	7.570e-03	3.674e-03
	X31_P4	X34_P4	X38_P4	X39_P4
A (output stable)	3.831e-04	2.924e-05	2.933e-05	4.009e-04
B (output stable)	3.155e-04	2.596e-05	2.600e-05	3.497e-04
A to Z	6.054e-03	1.023e-02	1.109e-02	6.683e-03
B to Z	4.193e-03	1.006e-02	1.092e-02	4.854e-03
	X46_P4	X57_P4		

A (output stable)	3.043e-05	3.061e-05		
B (output stable)	2.741e-05	2.763e-05		
A to Z	1.213e-02	1.475e-02		
B to Z	1.198e-02	1.460e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

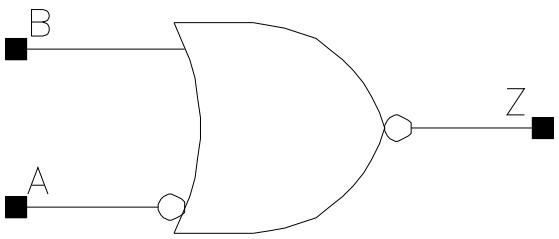
Pin Cycle (vdds)	X2_P4	X4_P4	X8_P4	X9_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P4	X16_P4	X19_P4	X20_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P4	X24_P4	X27_P4	X29_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P4	X34_P4	X38_P4	X39_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P4	X57_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.544	0.4352
X3_P4	0.800	0.544	0.4352
X4_P4	0.800	0.544	0.4352
X10_P4	1.600	0.544	0.8704
X14_P4	1.600	0.816	1.3056
X19_P4	1.600	0.816	1.3056
X29_P4	1.600	1.088	1.7408
X39_P4	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P4	X3_P4	X4_P4	X10_P4
A	0.0005	0.0005	0.0005	0.0009
B	0.0004	0.0004	0.0004	0.0010
	X14_P4	X19_P4	X29_P4	X39_P4
A	0.0009	0.0009	0.0014	0.0014
B	0.0016	0.0020	0.0031	0.0040

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	X3_P4	X2_P4	X3_P4
A to Z ↓	0.0226	0.0227	5.4382	4.1269
A to Z ↑	0.0207	0.0206	15.8572	13.4502
B to Z ↓	0.0072	0.0063	5.7528	4.3500

B to Z ↑	0.0158	0.0151	16.0482	13.5926
	X4_P4	**X10_P4**	**X4_P4**	**X10_P4**
A to Z ↓	0.0234	0.0231	3.1766	1.1536
A to Z ↑	0.0206	0.0200	9.7678	3.8660
B to Z ↓	0.0060	0.0056	3.3471	1.1825
B to Z ↑	0.0136	0.0135	9.8835	3.9142
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0278	0.0292	0.7263	0.5682
A to Z ↑	0.0232	0.0238	2.6307	1.9430
B to Z ↓	0.0052	0.0050	0.8182	0.6423
B to Z ↑	0.0127	0.0118	2.6675	1.9699
	X29_P4	**X39_P4**	**X29_P4**	**X39_P4**
A to Z ↓	0.0255	0.0292	0.3832	0.2877
A to Z ↑	0.0227	0.0244	1.3480	0.9908
B to Z ↓	0.0053	0.0049	0.4048	0.3176
B to Z ↑	0.0126	0.0116	1.3660	1.0042

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P4	6.179e-07	1.000e-20
X3_P4	7.454e-07	1.000e-20
X4_P4	1.023e-06	1.000e-20
X10_P4	3.129e-06	1.000e-20
X14_P4	3.583e-06	1.000e-20
X19_P4	4.969e-06	1.000e-20
X29_P4	7.646e-06	1.000e-20
X39_P4	9.609e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P4	X3_P4	X4_P4	X10_P4
A (output stable)	6.731e-04	7.279e-04	8.099e-04	1.639e-03
B (output stable)	1.770e-05	2.127e-05	3.100e-05	8.406e-05
A to Z	1.144e-03	1.255e-03	1.454e-03	3.295e-03
B to Z	3.642e-04	4.134e-04	5.027e-04	1.353e-03
	X14_P4	X19_P4	X29_P4	X39_P4
A (output stable)	2.423e-03	2.696e-03	4.181e-03	5.349e-03
B (output stable)	1.229e-04	1.713e-04	4.185e-04	3.317e-04
A to Z	4.828e-03	5.717e-03	9.162e-03	1.141e-02
B to Z	1.814e-03	2.264e-03	3.635e-03	4.403e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P4	X3_P4	X4_P4	X10_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P4	X19_P4	X29_P4	X39_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

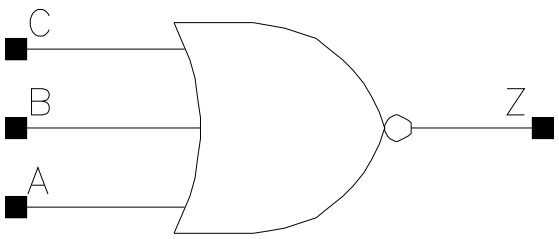
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.544	0.4352
X7_P4	0.800	0.952	0.7616
X11_P4	0.800	1.360	1.0880
X14_P4	0.800	1.768	1.4144
X21_P4	0.800	2.584	2.0672
X29_P4	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X11_P4	X14_P4
A	0.0005	0.0009	0.0016	0.0021
B	0.0005	0.0011	0.0015	0.0022
C	0.0005	0.0009	0.0014	0.0019
	X21_P4	X29_P4		
A	0.0033	0.0044		
B	0.0033	0.0043		
C	0.0028	0.0038		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X7_P4	X3_P4	X7_P4
A to Z ↓	0.0092	0.0093	3.1674	1.6582
A to Z ↑	0.0185	0.0192	12.1989	6.2952

B to Z ↓	0.0085	0.0084	3.1915	1.5961
B to Z ↑	0.0180	0.0192	12.2293	6.3104
C to Z ↓	0.0073	0.0061	3.2353	1.6163
C to Z ↑	0.0171	0.0145	12.2546	6.3200
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0092	0.0093	1.0418	0.7997
A to Z ↑	0.0195	0.0190	4.1585	3.0199
B to Z ↓	0.0086	0.0084	1.0527	0.7775
B to Z ↑	0.0181	0.0187	4.1679	3.0281
C to Z ↓	0.0066	0.0063	1.0522	0.7917
C to Z ↑	0.0158	0.0146	4.1759	3.0347
	X21_P4	**X29_P4**	**X21_P4**	**X29_P4**
A to Z ↓	0.0093	0.0094	0.5324	0.3998
A to Z ↑	0.0188	0.0189	2.0282	1.5259
B to Z ↓	0.0085	0.0086	0.5233	0.3960
B to Z ↑	0.0185	0.0185	2.0329	1.5292
C to Z ↓	0.0065	0.0066	0.5346	0.4041
C to Z ↑	0.0148	0.0149	2.0378	1.5331

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	6.804e-07	1.000e-20
X7_P4	1.339e-06	1.000e-20
X11_P4	1.998e-06	1.000e-20
X14_P4	2.740e-06	1.000e-20
X21_P4	4.008e-06	1.000e-20
X29_P4	5.308e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	2.985e-05	7.063e-05	1.292e-04	1.447e-04
B (output stable)	3.773e-06	3.344e-05	1.809e-05	5.897e-05
C (output stable)	1.987e-05	7.484e-05	8.598e-05	1.527e-04
A to Z	9.927e-04	2.012e-03	3.171e-03	4.136e-03
B to Z	8.221e-04	1.715e-03	2.471e-03	3.504e-03
C to Z	6.601e-04	1.116e-03	1.874e-03	2.353e-03
	X21_P4	X29_P4		
A (output stable)	2.128e-04	2.841e-04		
B (output stable)	8.436e-05	1.145e-04		
C (output stable)	2.256e-04	3.070e-04		
A to Z	6.130e-03	8.181e-03		
B to Z	5.155e-03	6.883e-03		
C to Z	3.521e-03	4.705e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

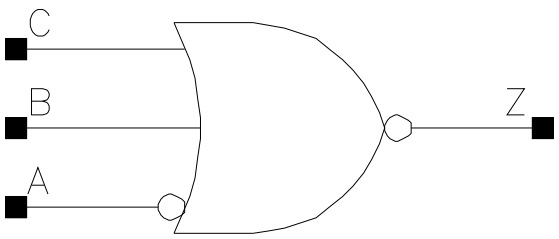
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P4	X29_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X7_P4	0.800	1.360	1.0880
X11_P4	0.800	1.632	1.3056
X14_P4	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X11_P4	X14_P4
A	0.0007	0.0007	0.0009	0.0013
B	0.0005	0.0010	0.0015	0.0019
C	0.0005	0.0010	0.0014	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0251	0.0226	3.0084	1.4182
A to Z ↑	0.0271	0.0271	12.2303	5.9839
B to Z ↓	0.0085	0.0085	3.2045	1.5184
B to Z ↑	0.0179	0.0189	12.3156	6.0219
C to Z ↓	0.0073	0.0064	3.2414	1.5300
C to Z ↑	0.0170	0.0152	12.3430	6.0320
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0274	0.0220	1.0018	0.7407

A to Z ↑	0.0304	0.0266	4.1576	3.0650
B to Z ↓	0.0085	0.0084	1.0538	0.7872
B to Z ↑	0.0179	0.0181	4.1824	3.0857
C to Z ↓	0.0065	0.0063	1.0540	0.7961
C to Z ↑	0.0155	0.0148	4.1903	3.0928

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	9.997e-07	1.000e-20
X7_P4	2.392e-06	1.000e-20
X11_P4	2.814e-06	1.000e-20
X14_P4	4.280e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	8.710e-04	1.525e-03	2.034e-03	2.809e-03
B (output stable)	1.474e-05	6.286e-05	7.426e-05	1.259e-04
C (output stable)	2.957e-05	1.309e-04	1.401e-04	2.261e-04
A to Z	1.882e-03	3.900e-03	5.316e-03	7.339e-03
B to Z	8.137e-04	1.781e-03	2.461e-03	3.343e-03
C to Z	6.530e-04	1.235e-03	1.832e-03	2.343e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

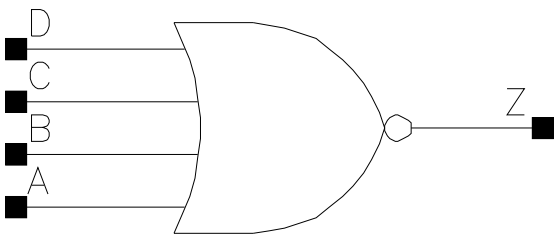
Pin Cycle (vdds)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.224	0.9792
X10_P4	0.800	1.632	1.3056
X14_P4	0.800	1.904	1.5232
X18_P4	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X18_P4
A	0.0005	0.0004	0.0005	0.0006
B	0.0005	0.0006	0.0007	0.0007
C	0.0005	0.0005	0.0005	0.0006
D	0.0005	0.0004	0.0005	0.0006

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0271	0.0311	2.9825	1.4338
A to Z ↑	0.0439	0.0492	4.3449	2.0932
B to Z ↓	0.0262	0.0312	2.9825	1.4338
B to Z ↑	0.0449	0.0517	4.3436	2.0931
C to Z ↓	0.0279	0.0317	2.9795	1.4314
C to Z ↑	0.0468	0.0531	4.3529	2.0915

D to Z ↓	0.0276	0.0306	2.9790	1.4313
D to Z ↑	0.0486	0.0538	4.3509	2.0903
	X14_P4	**X18_P4**	**X14_P4**	**X18_P4**
A to Z ↓	0.0300	0.0313	0.9891	0.7827
A to Z ↑	0.0452	0.0441	1.4431	1.0818
B to Z ↓	0.0295	0.0302	0.9896	0.7827
B to Z ↑	0.0468	0.0448	1.4422	1.0832
C to Z ↓	0.0293	0.0314	0.9864	0.7810
C to Z ↑	0.0453	0.0447	1.4418	1.0818
D to Z ↓	0.0283	0.0300	0.9865	0.7810
D to Z ↑	0.0463	0.0454	1.4411	1.0809

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	2.045e-06	1.000e-20
X10_P4	3.261e-06	1.000e-20
X14_P4	4.907e-06	1.000e-20
X18_P4	6.697e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	3.648e-04	4.703e-04	5.850e-04	7.236e-04
B (output stable)	3.259e-04	4.397e-04	5.428e-04	6.588e-04
C (output stable)	3.922e-04	4.608e-04	6.243e-04	7.936e-04
D (output stable)	3.567e-04	4.208e-04	5.705e-04	7.227e-04
A to Z	2.519e-03	3.947e-03	5.567e-03	7.075e-03
B to Z	2.434e-03	3.873e-03	5.445e-03	6.924e-03
C to Z	2.608e-03	3.878e-03	5.221e-03	6.662e-03
D to Z	2.548e-03	3.797e-03	5.109e-03	6.505e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

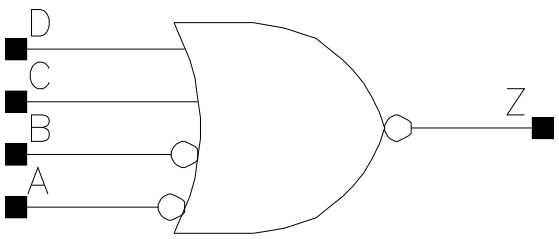
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	1.224	0.9792
X7_P4	0.800	1.496	1.1968
X11_P4	0.800	2.040	1.6320
X14_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P4	X7_P4	X11_P4	X14_P4
A	0.0007	0.0007	0.0013	0.0012
B	0.0007	0.0007	0.0013	0.0013
C	0.0005	0.0010	0.0014	0.0020
D	0.0005	0.0010	0.0014	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X7_P4	X4_P4	X7_P4
A to Z ↓	0.0251	0.0262	2.7911	1.4427
A to Z ↑	0.0336	0.0331	11.7461	6.0749
B to Z ↓	0.0233	0.0243	2.7910	1.4420
B to Z ↑	0.0339	0.0336	11.7518	6.0756
C to Z ↓	0.0087	0.0084	2.9290	1.5307
C to Z ↑	0.0188	0.0187	11.8028	6.1128

D to Z ↓	0.0075	0.0063	2.9499	1.5290
D to Z ↑	0.0180	0.0152	11.8203	6.1238
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0237	0.0260	0.9896	0.7438
A to Z ↑	0.0306	0.0333	4.1069	3.0537
B to Z ↓	0.0216	0.0242	0.9882	0.7429
B to Z ↑	0.0308	0.0341	4.1068	3.0542
C to Z ↓	0.0086	0.0086	1.0532	0.7855
C to Z ↑	0.0178	0.0183	4.1292	3.0707
D to Z ↓	0.0065	0.0064	1.0544	0.7883
D to Z ↑	0.0155	0.0150	4.1377	3.0776

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	1.570e-06	1.000e-20
X7_P4	2.080e-06	1.000e-20
X11_P4	3.300e-06	1.000e-20
X14_P4	3.788e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X7_P4	X11_P4	X14_P4
A (output stable)	7.218e-04	8.344e-04	1.345e-03	1.617e-03
B (output stable)	6.944e-04	8.076e-04	1.265e-03	1.552e-03
C (output stable)	5.565e-05	4.853e-05	7.907e-05	1.179e-04
D (output stable)	7.277e-05	1.285e-04	1.644e-04	2.649e-04
A to Z	3.102e-03	4.219e-03	6.438e-03	8.352e-03
B to Z	2.876e-03	4.000e-03	5.977e-03	7.915e-03
C to Z	9.205e-04	1.753e-03	2.472e-03	3.392e-03
D to Z	7.645e-04	1.228e-03	1.847e-03	2.405e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

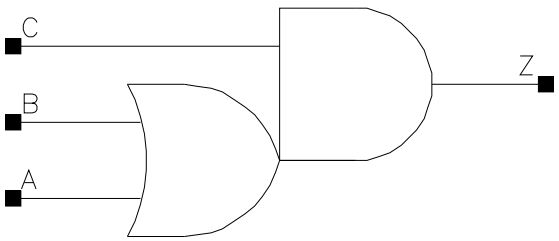
Pin Cycle (vdds)	X4_P4	X7_P4	X11_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.680	0.5440
X10_P4	0.800	0.952	0.7616
X19_P4	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0006	0.0006	0.0011
B	0.0006	0.0007	0.0013
C	0.0007	0.0008	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0246	0.0278	2.8797	1.4417
A to Z ↑	0.0204	0.0242	4.7861	2.0913
B to Z ↓	0.0252	0.0286	2.8821	1.4437
B to Z ↑	0.0188	0.0223	4.7839	2.0892
C to Z ↓	0.0227	0.0245	2.8461	1.4212
C to Z ↑	0.0194	0.0222	4.7817	2.0864
	X19_P4		**X19_P4**	
A to Z ↓	0.0289		0.7522	
A to Z ↑	0.0254		1.0699	

B to Z ↓	0.0298		0.7521	
B to Z ↑	0.0232		1.0661	
C to Z ↓	0.0247		0.7391	
C to Z ↑	0.0226		1.0667	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.699e-06	1.000e-20
X10_P4	2.981e-06	1.000e-20
X19_P4	5.600e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	7.238e-05	7.528e-05	1.485e-04
B (output stable)	7.061e-05	7.409e-05	1.421e-04
C (output stable)	3.664e-05	3.798e-05	7.549e-05
A to Z	1.725e-03	2.835e-03	5.739e-03
B to Z	1.585e-03	2.674e-03	5.435e-03
C to Z	1.909e-03	2.948e-03	5.867e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

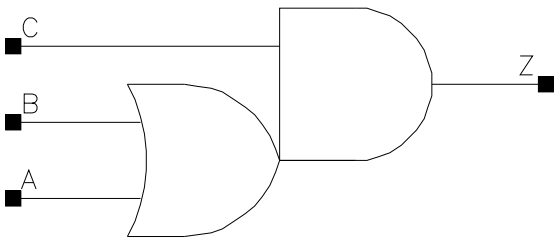
Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	1.360	1.0880
X14_P4	0.800	1.496	1.1968
X19_P4	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0006	0.0013	0.0013	0.0012
B	0.0006	0.0012	0.0012	0.0012
C	0.0007	0.0012	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0301	0.0252	2.8166	1.4289
A to Z ↑	0.0210	0.0193	4.1450	2.0303
B to Z ↓	0.0308	0.0256	2.8182	1.4280
B to Z ↑	0.0195	0.0179	4.1419	2.0269
C to Z ↓	0.0208	0.0172	2.7697	1.4100
C to Z ↑	0.0194	0.0176	4.1409	2.0267
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0279	0.0304	0.9963	0.7515

A to Z ↑	0.0211	0.0227	1.3749	1.0332
B to Z ↓	0.0284	0.0311	0.9966	0.7513
B to Z ↑	0.0198	0.0215	1.3756	1.0330
C to Z ↓	0.0192	0.0210	0.9793	0.7364
C to Z ↑	0.0196	0.0214	1.3721	1.0312

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.942e-06	1.000e-20
X10_P4	4.009e-06	1.000e-20
X14_P4	4.822e-06	1.000e-20
X19_P4	5.628e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.861e-05	3.807e-05	3.822e-05	3.804e-05
B (output stable)	1.575e-05	3.639e-05	3.629e-05	3.685e-05
C (output stable)	1.973e-04	3.909e-04	3.933e-04	3.933e-04
A to Z	2.195e-03	3.877e-03	4.925e-03	5.985e-03
B to Z	2.037e-03	3.504e-03	4.550e-03	5.621e-03
C to Z	1.795e-03	3.063e-03	4.041e-03	5.012e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

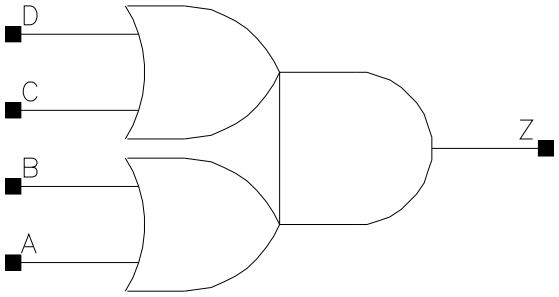
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.952	0.7616
X10_P4	0.800	1.088	0.8704
X14_P4	0.800	1.904	1.5232
X19_P4	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0004	0.0006	0.0012	0.0012
B	0.0004	0.0006	0.0012	0.0012
C	0.0005	0.0007	0.0012	0.0012
D	0.0004	0.0007	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0415	0.0337	2.9139	1.4521
A to Z ↑	0.0286	0.0248	4.1637	2.0767
B to Z ↓	0.0426	0.0345	2.9141	1.4525

B to Z ↑	0.0274	0.0235	4.1598	2.0743
C to Z ↓	0.0355	0.0299	2.8948	1.4464
C to Z ↑	0.0278	0.0250	4.1607	2.0754
D to Z ↓	0.0364	0.0304	2.8947	1.4464
D to Z ↑	0.0263	0.0233	4.1582	2.0732
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0323	0.0340	1.0103	0.7572
A to Z ↑	0.0237	0.0247	1.3806	1.0375
B to Z ↓	0.0318	0.0337	1.0107	0.7579
B to Z ↑	0.0218	0.0229	1.3778	1.0352
C to Z ↓	0.0276	0.0295	1.0061	0.7541
C to Z ↑	0.0232	0.0243	1.3789	1.0367
D to Z ↓	0.0267	0.0288	1.0068	0.7546
D to Z ↑	0.0209	0.0222	1.3759	1.0348

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.323e-06	1.000e-20
X10_P4	2.985e-06	1.000e-20
X14_P4	4.921e-06	1.000e-20
X19_P4	5.596e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.615e-05	2.644e-05	7.866e-05	7.842e-05
B (output stable)	1.305e-05	2.288e-05	7.315e-05	7.297e-05
C (output stable)	5.240e-05	7.456e-05	1.741e-04	1.743e-04
D (output stable)	5.607e-05	7.182e-05	1.712e-04	1.711e-04
A to Z	2.198e-03	3.416e-03	5.791e-03	6.617e-03
B to Z	2.102e-03	3.232e-03	5.267e-03	6.096e-03
C to Z	1.900e-03	3.035e-03	5.006e-03	5.823e-03
D to Z	1.812e-03	2.870e-03	4.481e-03	5.295e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

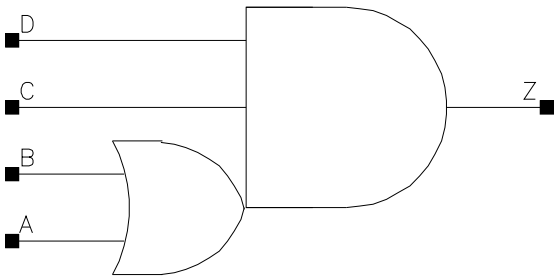
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	0.816	0.6528
X10_P4	0.800	1.088	0.8704
X14_P4	0.800	1.904	1.5232
X19_P4	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P4	X10_P4	X14_P4	X19_P4
A	0.0004	0.0009	0.0010	0.0012
B	0.0005	0.0007	0.0010	0.0013
C	0.0005	0.0007	0.0010	0.0012
D	0.0005	0.0006	0.0010	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X10_P4	X4_P4	X10_P4
A to Z ↓	0.0352	0.0341	3.1644	1.4802
A to Z ↑	0.0320	0.0333	4.4205	2.1179
B to Z ↓	0.0367	0.0326	3.1678	1.4806
B to Z ↑	0.0308	0.0293	4.4189	2.1153
C to Z ↓	0.0301	0.0269	3.0865	1.4509

C to Z ↑	0.0299	0.0291	4.4133	2.1119
D to Z ↓	0.0295	0.0260	3.0862	1.4497
D to Z ↑	0.0318	0.0304	4.4144	2.1121
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0335	0.0320	1.0117	0.7517
A to Z ↑	0.0321	0.0327	1.4090	1.0552
B to Z ↓	0.0328	0.0314	1.0115	0.7519
B to Z ↑	0.0293	0.0299	1.4055	1.0514
C to Z ↓	0.0281	0.0269	0.9917	0.7386
C to Z ↑	0.0292	0.0294	1.4043	1.0520
D to Z ↓	0.0266	0.0256	0.9896	0.7372
D to Z ↑	0.0297	0.0300	1.4051	1.0519

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	1.268e-06	1.000e-20
X10_P4	2.970e-06	1.000e-20
X14_P4	4.273e-06	1.000e-20
X19_P4	5.706e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X10_P4	X14_P4	X19_P4
A (output stable)	6.405e-05	1.032e-04	1.753e-04	1.998e-04
B (output stable)	6.341e-05	1.037e-04	1.674e-04	1.916e-04
C (output stable)	1.015e-05	2.186e-05	4.800e-05	5.501e-05
D (output stable)	2.321e-05	4.081e-05	1.468e-04	1.636e-04
A to Z	1.848e-03	3.356e-03	5.128e-03	6.391e-03
B to Z	1.773e-03	3.036e-03	4.700e-03	5.853e-03
C to Z	2.017e-03	3.424e-03	5.462e-03	6.711e-03
D to Z	1.936e-03	3.293e-03	5.104e-03	6.311e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

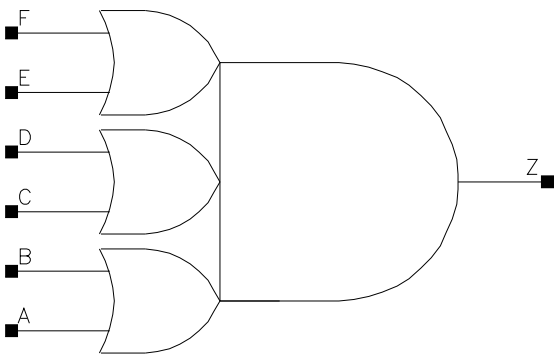
Pin Cycle (vdds)	X4_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	1.360	1.0880
X9_P4	0.800	1.496	1.1968
X19_P4	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P4	X9_P4	X19_P4
A	0.0005	0.0006	0.0010
B	0.0006	0.0008	0.0012
C	0.0004	0.0006	0.0010
D	0.0004	0.0006	0.0012
E	0.0005	0.0006	0.0011
F	0.0005	0.0006	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X9_P4	X4_P4	X9_P4
A to Z ↓	0.0489	0.0406	3.2216	1.5915
A to Z ↑	0.0368	0.0346	4.5390	2.2278
B to Z ↓	0.0513	0.0426	3.2232	1.5920
B to Z ↑	0.0365	0.0336	4.5420	2.2272
C to Z ↓	0.0450	0.0371	3.2024	1.5834
C to Z ↑	0.0375	0.0343	4.5445	2.2271
D to Z ↓	0.0459	0.0379	3.2037	1.5843
D to Z ↑	0.0357	0.0324	4.5382	2.2259
E to Z ↓	0.0386	0.0329	3.1774	1.5757
E to Z ↑	0.0346	0.0327	4.5372	2.2258
F to Z ↓	0.0400	0.0341	3.1790	1.5759
F to Z ↑	0.0334	0.0313	4.5328	2.2237
	X19_P4		X19_P4	
A to Z ↓	0.0398		0.7649	
A to Z ↑	0.0334		1.0549	
B to Z ↓	0.0411		0.7652	
B to Z ↑	0.0312		1.0515	
C to Z ↓	0.0367		0.7607	
C to Z ↑	0.0335		1.0544	
D to Z ↓	0.0378		0.7611	
D to Z ↑	0.0316		1.0516	
E to Z ↓	0.0325		0.7574	
E to Z ↑	0.0322		1.0529	
F to Z ↓	0.0336		0.7574	
F to Z ↑	0.0302		1.0504	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	1.361e-06	1.000e-20
X9_P4	3.149e-06	1.000e-20
X19_P4	6.125e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X9_P4	X19_P4
A (output stable)	1.236e-05	2.157e-05	3.943e-05
B (output stable)	1.480e-05	2.331e-05	3.446e-05
C (output stable)	3.880e-05	5.462e-05	1.106e-04
D (output stable)	3.673e-05	5.593e-05	1.104e-04
E (output stable)	8.540e-05	1.180e-04	2.292e-04
F (output stable)	9.884e-05	1.297e-04	2.454e-04
A to Z	2.604e-03	4.081e-03	7.951e-03
B to Z	2.539e-03	3.944e-03	7.619e-03
C to Z	2.358e-03	3.723e-03	7.303e-03
D to Z	2.260e-03	3.545e-03	6.967e-03
E to Z	2.036e-03	3.335e-03	6.546e-03
F to Z	1.961e-03	3.189e-03	6.248e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

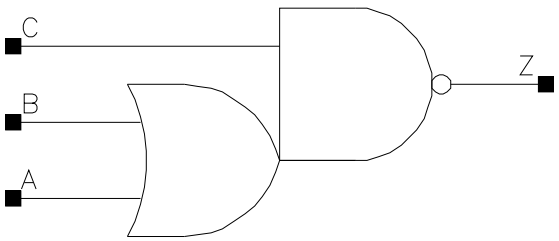
Pin Cycle (vdds)	X4_P4	X9_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.544	0.4352
X10_P4	0.800	1.360	1.0880
X20_P4	0.800	2.720	2.1760
X26_P4	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P4	X10_P4	X20_P4	X26_P4
A	0.0005	0.0015	0.0029	0.0039
B	0.0005	0.0013	0.0027	0.0036
C	0.0005	0.0015	0.0032	0.0043

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X10_P4**	**X3_P4**	**X10_P4**
A to Z ↓	0.0105	0.0116	5.6758	1.7919
A to Z ↑	0.0143	0.0144	9.8913	2.7523
B to Z ↓	0.0087	0.0093	5.5574	1.8005
B to Z ↑	0.0143	0.0131	9.9311	2.7691
C to Z ↓	0.0099	0.0104	5.1442	1.6418
C to Z ↑	0.0141	0.0130	5.2605	1.4692
	X20_P4	**X26_P4**	**X20_P4**	**X26_P4**
A to Z ↓	0.0122	0.0123	0.9166	0.6945

A to Z ↑	0.0150	0.0150	1.4118	1.0622
B to Z ↓	0.0098	0.0099	0.9261	0.7050
B to Z ↑	0.0138	0.0138	1.4198	1.0683
C to Z ↓	0.0110	0.0110	0.8426	0.6397
C to Z ↑	0.0134	0.0133	0.7226	0.5432

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	8.436e-07	1.000e-20
X10_P4	3.000e-06	1.000e-20
X20_P4	5.864e-06	1.000e-20
X26_P4	7.713e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X10_P4	X20_P4	X26_P4
A (output stable)	6.566e-05	2.361e-04	4.812e-04	6.237e-04
B (output stable)	6.369e-05	2.267e-04	4.560e-04	5.899e-04
C (output stable)	3.312e-05	1.177e-04	2.539e-04	3.355e-04
A to Z	6.738e-04	2.545e-03	5.269e-03	6.995e-03
B to Z	5.439e-04	1.844e-03	3.929e-03	5.250e-03
C to Z	8.499e-04	2.918e-03	6.115e-03	8.077e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

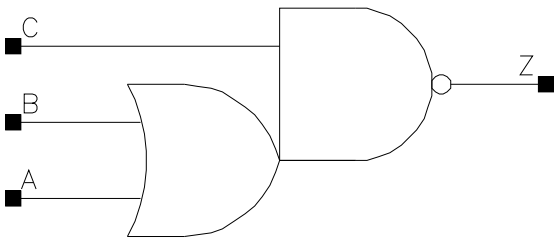
Pin Cycle (vdds)	X3_P4	X10_P4	X20_P4	X26_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X7_P4	0.800	0.952	0.7616
X10_P4	0.800	1.360	1.0880
X13_P4	0.800	1.904	1.5232
X26_P4	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X10_P4	X13_P4
A	0.0006	0.0010	0.0016	0.0021
B	0.0005	0.0011	0.0015	0.0019
C	0.0007	0.0010	0.0014	0.0019
	X26_P4			
A	0.0042			
B	0.0038			
C	0.0039			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X7_P4	X3_P4	X7_P4
A to Z ↓	0.0127	0.0114	4.9574	2.5795
A to Z ↑	0.0190	0.0168	7.9122	4.0718
B to Z ↓	0.0112	0.0096	4.9685	2.5049

B to Z ↑	0.0194	0.0169	7.9479	4.0861
C to Z ↓	0.0107	0.0091	4.7080	2.3966
C to Z ↑	0.0119	0.0101	4.3241	2.2591
	X10_P4	**X13_P4**	**X10_P4**	**X13_P4**
A to Z ↓	0.0111	0.0118	1.7438	1.3342
A to Z ↑	0.0163	0.0178	2.6861	2.0686
B to Z ↓	0.0093	0.0096	1.7355	1.3365
B to Z ↑	0.0162	0.0164	2.6983	2.0783
C to Z ↓	0.0089	0.0090	1.6458	1.2566
C to Z ↑	0.0096	0.0096	1.4889	1.1285
	X26_P4		**X26_P4**	
A to Z ↓	0.0117		0.6893	
A to Z ↑	0.0174		1.0443	
B to Z ↓	0.0094		0.6872	
B to Z ↑	0.0161		1.0497	
C to Z ↓	0.0092		0.6480	
C to Z ↑	0.0094		0.5697	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	1.175e-06	1.000e-20
X7_P4	2.137e-06	1.000e-20
X10_P4	3.104e-06	1.000e-20
X13_P4	4.081e-06	1.000e-20
X26_P4	7.831e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X7_P4	X10_P4	X13_P4
A (output stable)	2.093e-05	3.886e-05	5.743e-05	1.051e-04
B (output stable)	1.800e-05	3.421e-05	5.012e-05	8.516e-05
C (output stable)	2.106e-04	3.904e-04	5.343e-04	7.662e-04
A to Z	1.282e-03	2.070e-03	3.000e-03	4.362e-03
B to Z	1.092e-03	1.717e-03	2.448e-03	3.304e-03
C to Z	8.301e-04	1.380e-03	1.951e-03	2.712e-03
	X26_P4			
A (output stable)	2.049e-04			
B (output stable)	1.621e-04			
C (output stable)	1.413e-03			
A to Z	8.446e-03			
B to Z	6.325e-03			
C to Z	5.220e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P4	X7_P4	X10_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

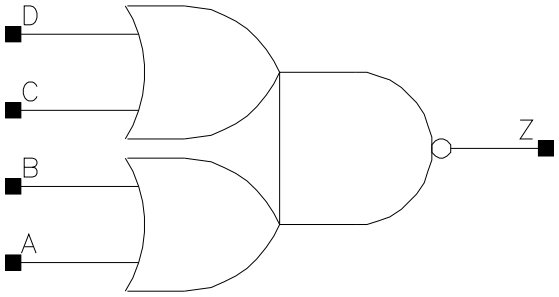
	X26_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X6_P4	0.800	1.360	1.0880
X8_P4	0.800	1.768	1.4144
X11_P4	0.800	2.448	1.9584
X24_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X8_P4	X11_P4
A	0.0005	0.0010	0.0015	0.0020
B	0.0005	0.0009	0.0014	0.0018
C	0.0005	0.0010	0.0014	0.0019
D	0.0005	0.0009	0.0013	0.0018
	X24_P4			
A	0.0043			
B	0.0039			
C	0.0041			
D	0.0037			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X6_P4**	**X3_P4**	**X6_P4**
A to Z ↓	0.0119	0.0140	4.6638	2.5381
A to Z ↑	0.0208	0.0208	9.7756	4.3005
B to Z ↓	0.0107	0.0120	4.6198	2.5452
B to Z ↑	0.0212	0.0195	9.7961	4.3178
C to Z ↓	0.0101	0.0123	4.7561	2.5563
C to Z ↑	0.0147	0.0157	9.8104	4.3252
D to Z ↓	0.0086	0.0097	4.7093	2.5848
D to Z ↑	0.0148	0.0135	9.8452	4.3532
	X8_P4	**X11_P4**	**X8_P4**	**X11_P4**
A to Z ↓	0.0134	0.0135	1.7381	1.3185
A to Z ↑	0.0194	0.0196	2.8832	2.1637
B to Z ↓	0.0116	0.0115	1.7479	1.3209
B to Z ↑	0.0187	0.0186	2.8992	2.1754
C to Z ↓	0.0120	0.0123	1.7619	1.3352
C to Z ↑	0.0146	0.0151	2.8812	2.1813
D to Z ↓	0.0099	0.0098	1.7829	1.3413
D to Z ↑	0.0133	0.0133	2.9022	2.1979
	X24_P4		**X24_P4**	
A to Z ↓	0.0137		0.6490	
A to Z ↑	0.0196		1.0457	
B to Z ↓	0.0117		0.6440	
B to Z ↑	0.0188		1.0512	
C to Z ↓	0.0127		0.6579	
C to Z ↑	0.0150		1.0469	
D to Z ↓	0.0101		0.6553	
D to Z ↑	0.0135		1.0550	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	1.066e-06	1.000e-20
X6_P4	2.502e-06	1.000e-20
X8_P4	3.607e-06	1.000e-20
X11_P4	4.851e-06	1.000e-20
X24_P4	9.370e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X6_P4	X8_P4	X11_P4
A (output stable)	2.330e-05	8.116e-05	1.027e-04	1.444e-04
B (output stable)	1.822e-05	7.661e-05	9.358e-05	1.372e-04
C (output stable)	7.328e-05	1.801e-04	2.354e-04	3.216e-04
D (output stable)	7.072e-05	1.764e-04	2.278e-04	3.111e-04
A to Z	1.177e-03	2.757e-03	3.797e-03	5.129e-03
B to Z	1.019e-03	2.207e-03	3.053e-03	4.111e-03
C to Z	7.581e-04	1.974e-03	2.708e-03	3.761e-03
D to Z	6.284e-04	1.437e-03	2.038e-03	2.789e-03
	X24_P4			
A (output stable)	2.962e-04			
B (output stable)	2.609e-04			
C (output stable)	6.408e-04			
D (output stable)	5.998e-04			

A to Z	1.057e-02			
B to Z	8.483e-03			
C to Z	7.753e-03			
D to Z	5.785e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

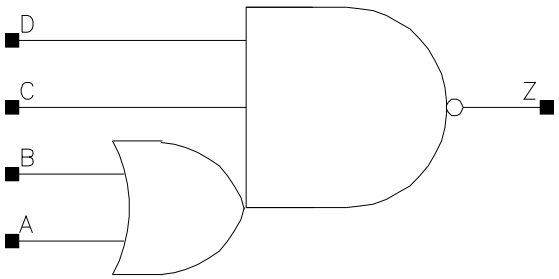
Pin Cycle (vdds)	X3_P4	X6_P4	X8_P4	X11_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X6_P4	0.800	1.360	1.0880
X12_P4	0.800	2.448	1.9584
X18_P4	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X12_P4	X18_P4
A	0.0007	0.0010	0.0019	0.0028
B	0.0005	0.0009	0.0018	0.0026
C	0.0005	0.0011	0.0020	0.0032
D	0.0005	0.0010	0.0020	0.0029

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0186	0.0159	6.9094	3.7350
A to Z ↑	0.0206	0.0169	8.2139	4.1302
B to Z ↓	0.0141	0.0128	6.9471	3.7519
B to Z ↑	0.0179	0.0154	8.2306	4.1552
C to Z ↓	0.0152	0.0153	6.5056	3.5183

C to Z ↑	0.0166	0.0159	4.1607	2.1476
D to Z ↓	0.0166	0.0152	6.5450	3.5388
D to Z ↑	0.0160	0.0145	4.2800	2.1539
	X12_P4	**X18_P4**	**X12_P4**	**X18_P4**
A to Z ↓	0.0162	0.0165	1.9476	1.3183
A to Z ↑	0.0167	0.0167	2.0722	1.3904
B to Z ↓	0.0130	0.0133	1.9585	1.3277
B to Z ↑	0.0151	0.0153	2.0868	1.3998
C to Z ↓	0.0151	0.0153	1.8351	1.2435
C to Z ↑	0.0156	0.0155	1.0969	0.7223
D to Z ↓	0.0153	0.0154	1.8458	1.2504
D to Z ↑	0.0142	0.0142	1.0934	0.7309

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	9.538e-07	1.000e-20
X6_P4	1.741e-06	1.000e-20
X12_P4	3.266e-06	1.000e-20
X18_P4	4.794e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X6_P4	X12_P4	X18_P4
A (output stable)	1.043e-04	2.150e-04	4.029e-04	5.874e-04
B (output stable)	1.098e-04	2.109e-04	3.850e-04	5.503e-04
C (output stable)	1.705e-05	5.201e-05	9.645e-05	1.534e-04
D (output stable)	4.627e-05	1.467e-04	2.510e-04	4.020e-04
A to Z	1.310e-03	2.081e-03	4.082e-03	6.089e-03
B to Z	9.792e-04	1.566e-03	3.031e-03	4.571e-03
C to Z	1.500e-03	2.767e-03	5.258e-03	7.887e-03
D to Z	1.376e-03	2.335e-03	4.473e-03	6.647e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

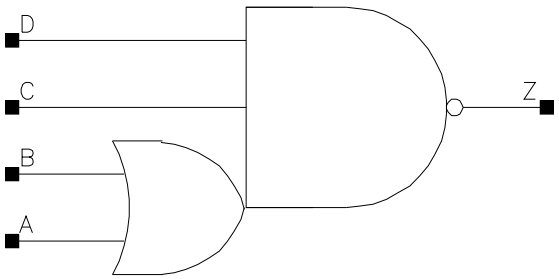
Pin Cycle (vdds)	X3_P4	X6_P4	X12_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X6_P4	0.800	1.360	1.0880
X9_P4	0.800	1.768	1.4144
X12_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X9_P4	X12_P4
A	0.0005	0.0011	0.0016	0.0021
B	0.0005	0.0010	0.0014	0.0022
C	0.0005	0.0010	0.0015	0.0020
D	0.0005	0.0010	0.0014	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0154	0.0159	7.4471	3.6863
A to Z ↑	0.0201	0.0213	8.3072	4.1254
B to Z ↓	0.0135	0.0135	7.2930	3.7028
B to Z ↑	0.0204	0.0204	8.3410	4.1431
C to Z ↓	0.0126	0.0134	7.0333	3.5250

C to Z ↑	0.0129	0.0131	4.5202	2.2360
D to Z ↓	0.0129	0.0127	7.0754	3.5473
D to Z ↑	0.0116	0.0111	4.5579	2.2521
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0161	0.0162	2.5355	1.9286
A to Z ↑	0.0206	0.0211	2.7213	2.1248
B to Z ↓	0.0138	0.0138	2.5344	1.9325
B to Z ↑	0.0200	0.0206	2.7343	2.1359
C to Z ↓	0.0133	0.0135	2.4168	1.8398
C to Z ↑	0.0127	0.0129	1.4754	1.1202
D to Z ↓	0.0129	0.0128	2.4324	1.8521
D to Z ↑	0.0109	0.0107	1.4871	1.1322

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P4	8.460e-07	1.000e-20
X6_P4	1.780e-06	1.000e-20
X9_P4	2.506e-06	1.000e-20
X12_P4	3.331e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.344e-05	3.064e-05	4.741e-05	6.046e-05
B (output stable)	1.151e-05	2.834e-05	4.192e-05	6.110e-05
C (output stable)	5.954e-05	1.279e-04	1.904e-04	2.470e-04
D (output stable)	1.011e-04	3.557e-04	4.203e-04	6.596e-04
A to Z	1.321e-03	2.879e-03	4.192e-03	5.613e-03
B to Z	1.131e-03	2.318e-03	3.366e-03	4.499e-03
C to Z	8.936e-04	1.984e-03	2.817e-03	3.834e-03
D to Z	7.744e-04	1.615e-03	2.342e-03	3.094e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

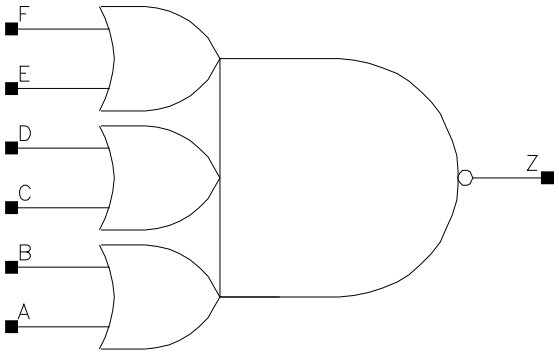
Pin Cycle (vdds)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.224	0.9792
X3_P4	0.800	1.224	0.9792
X5_P4	0.800	2.040	1.6320
X8_P4	0.800	2.720	2.1760
X10_P4	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P4	X3_P4	X5_P4	X8_P4
A	0.0005	0.0005	0.0011	0.0016
B	0.0004	0.0005	0.0010	0.0014
C	0.0004	0.0005	0.0010	0.0015
D	0.0005	0.0005	0.0010	0.0014

E	0.0004	0.0005	0.0010	0.0014
F	0.0004	0.0005	0.0009	0.0013
	X10_P4			
A	0.0021			
B	0.0019			
C	0.0020			
D	0.0018			
E	0.0019			
F	0.0018			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X3_P4**	**X2_P4**	**X3_P4**
A to Z ↓	0.0200	0.0192	8.1317	6.3416
A to Z ↑	0.0283	0.0247	11.2965	7.8236
B to Z ↓	0.0188	0.0179	8.1521	6.3772
B to Z ↑	0.0294	0.0257	11.3197	7.8438
C to Z ↓	0.0198	0.0193	8.1817	6.3684
C to Z ↑	0.0248	0.0221	11.3036	7.9522
D to Z ↓	0.0188	0.0174	8.2630	6.4519
D to Z ↑	0.0264	0.0225	11.3467	7.9751
E to Z ↓	0.0172	0.0168	8.2251	6.3943
E to Z ↑	0.0197	0.0176	11.3217	7.9733
F to Z ↓	0.0160	0.0152	8.2989	6.4854
F to Z ↑	0.0205	0.0179	11.3677	8.0095
	X5_P4	**X8_P4**	**X5_P4**	**X8_P4**
A to Z ↓	0.0204	0.0201	3.3949	2.3144
A to Z ↑	0.0257	0.0248	4.1253	2.7303
B to Z ↓	0.0182	0.0179	3.4128	2.3162
B to Z ↑	0.0249	0.0246	4.1400	2.7399
C to Z ↓	0.0189	0.0196	3.4221	2.3304
C to Z ↑	0.0218	0.0215	4.1689	2.7957
D to Z ↓	0.0166	0.0172	3.4324	2.3361
D to Z ↑	0.0211	0.0215	4.1887	2.8076
E to Z ↓	0.0178	0.0176	3.4482	2.3422
E to Z ↑	0.0178	0.0172	4.1756	2.8053
F to Z ↓	0.0151	0.0150	3.4638	2.3442
F to Z ↑	0.0165	0.0167	4.2009	2.8229
	X10_P4		**X10_P4**	
A to Z ↓	0.0205		1.7594	
A to Z ↑	0.0251		2.0761	
B to Z ↓	0.0182		1.7627	
B to Z ↑	0.0247		2.0840	
C to Z ↓	0.0193		1.7708	
C to Z ↑	0.0216		2.1175	
D to Z ↓	0.0170		1.7752	
D to Z ↑	0.0212		2.1281	
E to Z ↓	0.0179		1.7799	
E to Z ↑	0.0175		2.1133	
F to Z ↓	0.0155		1.7903	
F to Z ↑	0.0166		2.1272	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P4	9.524e-07	1.000e-20
X3_P4	1.599e-06	1.000e-20
X5_P4	2.935e-06	1.000e-20
X8_P4	4.171e-06	1.000e-20
X10_P4	5.518e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P4	X3_P4	X5_P4	X8_P4
A (output stable)	1.667e-05	2.162e-05	6.454e-05	8.563e-05
B (output stable)	1.408e-05	2.035e-05	6.076e-05	7.725e-05
C (output stable)	4.659e-05	5.913e-05	1.383e-04	1.915e-04
D (output stable)	4.777e-05	5.745e-05	1.427e-04	1.909e-04
E (output stable)	1.062e-04	1.337e-04	2.372e-04	3.477e-04
F (output stable)	1.160e-04	1.430e-04	2.650e-04	3.892e-04
A to Z	1.646e-03	1.995e-03	4.029e-03	5.793e-03
B to Z	1.512e-03	1.814e-03	3.454e-03	5.000e-03
C to Z	1.351e-03	1.662e-03	3.197e-03	4.679e-03
D to Z	1.241e-03	1.476e-03	2.714e-03	4.039e-03
E to Z	1.022e-03	1.268e-03	2.555e-03	3.618e-03
F to Z	9.135e-04	1.108e-03	2.071e-03	3.021e-03
	X10_P4			
A (output stable)	1.216e-04			
B (output stable)	1.137e-04			
C (output stable)	2.644e-04			
D (output stable)	2.738e-04			
E (output stable)	4.457e-04			
F (output stable)	5.060e-04			
A to Z	7.826e-03			
B to Z	6.712e-03			
C to Z	6.251e-03			
D to Z	5.319e-03			
E to Z	4.944e-03			
F to Z	4.067e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P4	X3_P4	X5_P4	X8_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P4			

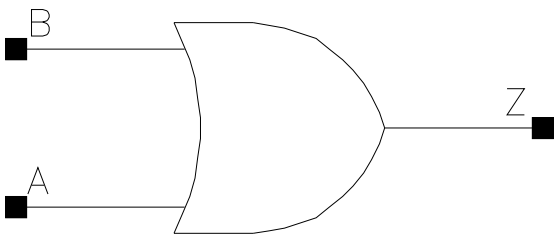
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.544	0.4352
X9_P4	0.800	0.680	0.5440
X19_P4	0.800	1.360	1.0880
X29_P4	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4	X29_P4
A	0.0005	0.0006	0.0011	0.0011
B	0.0005	0.0006	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X9_P4**	**X5_P4**	**X9_P4**
A to Z ↓	0.0312	0.0275	3.0483	1.5376
A to Z ↑	0.0195	0.0204	4.3035	2.1735
B to Z ↓	0.0318	0.0277	3.0520	1.5380
B to Z ↑	0.0185	0.0190	4.3083	2.1697
	X19_P4	**X29_P4**	**X19_P4**	**X29_P4**
A to Z ↓	0.0281	0.0330	0.7391	0.5061
A to Z ↑	0.0203	0.0231	1.0277	0.6901
B to Z ↓	0.0271	0.0322	0.7392	0.5063
B to Z ↑	0.0184	0.0213	1.0278	0.6895

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	9.967e-07	1.000e-20
X9_P4	2.076e-06	1.000e-20
X19_P4	4.162e-06	1.000e-20
X29_P4	5.251e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4	X29_P4
A (output stable)	1.605e-05	2.918e-05	1.022e-04	1.024e-04
B (output stable)	1.062e-05	2.191e-05	1.035e-04	1.039e-04
A to Z	1.597e-03	2.549e-03	5.402e-03	7.589e-03
B to Z	1.507e-03	2.393e-03	4.856e-03	7.033e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

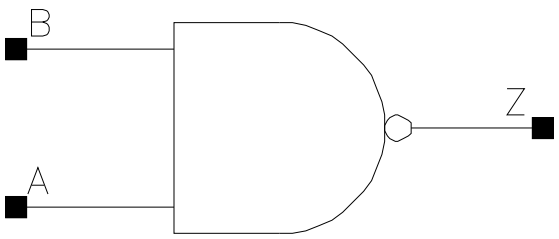
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4	X29_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X9_P4	0.800	0.952	0.7616
X14_P4	0.800	1.088	0.8704
X18_P4	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P4	X9_P4	X14_P4	X18_P4
A	0.0007	0.0006	0.0006	0.0006
B	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X9_P4**	**X5_P4**	**X9_P4**
A to Z ↓	0.0246	0.0282	2.7562	1.5079
A to Z ↑	0.0270	0.0298	4.1273	2.1789
B to Z ↓	0.0256	0.0298	2.7566	1.5084
B to Z ↑	0.0254	0.0287	4.1289	2.1805
	X14_P4	**X18_P4**	**X14_P4**	**X18_P4**
A to Z ↓	0.0310	0.0331	1.0451	0.7909
A to Z ↑	0.0318	0.0328	1.4394	1.1190
B to Z ↓	0.0326	0.0345	1.0450	0.7905
B to Z ↑	0.0307	0.0317	1.4404	1.1186

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	2.771e-06	1.000e-20
X9_P4	3.202e-06	1.000e-20
X14_P4	3.787e-06	1.000e-20
X18_P4	4.041e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X9_P4	X14_P4	X18_P4
A (output stable)	1.707e-05	1.614e-05	1.623e-05	1.649e-05
B (output stable)	4.692e-05	4.271e-05	4.282e-05	4.170e-05
A to Z	2.896e-03	3.724e-03	4.765e-03	5.381e-03
B to Z	2.778e-03	3.617e-03	4.658e-03	5.273e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

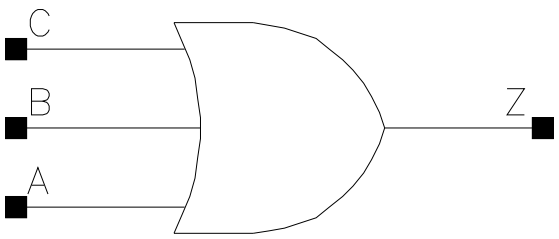
Pin Cycle (vdds)	X5_P4	X9_P4	X14_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.680	0.5440
X10_P4	0.800	0.952	0.7616
X14_P4	0.800	1.496	1.1968
X19_P4	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0005	0.0007	0.0011	0.0017
B	0.0004	0.0006	0.0013	0.0017
C	0.0005	0.0006	0.0012	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0412	0.0366	3.1550	1.5010
A to Z ↑	0.0226	0.0200	4.3288	2.0509
B to Z ↓	0.0410	0.0364	3.1568	1.5025
B to Z ↑	0.0221	0.0191	4.3307	2.0492
C to Z ↓	0.0410	0.0357	3.1588	1.5025
C to Z ↑	0.0212	0.0179	4.3260	2.0472
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0347	0.0336	1.0077	0.7723

A to Z ↑	0.0186	0.0184	1.4041	1.0781
B to Z ↓	0.0352	0.0328	1.0085	0.7723
B to Z ↑	0.0175	0.0177	1.4007	1.0755
C to Z ↓	0.0315	0.0310	1.0078	0.7725
C to Z ↑	0.0159	0.0160	1.3974	1.0753

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	8.677e-07	1.000e-20
X10_P4	1.883e-06	1.000e-20
X14_P4	3.136e-06	1.000e-20
X19_P4	4.233e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.970e-05	3.367e-05	7.002e-05	1.297e-04
B (output stable)	1.078e-06	5.901e-06	3.652e-05	1.835e-05
C (output stable)	8.976e-06	2.234e-05	9.651e-05	8.396e-05
A to Z	1.893e-03	3.105e-03	5.138e-03	7.315e-03
B to Z	1.788e-03	2.923e-03	4.841e-03	6.613e-03
C to Z	1.699e-03	2.756e-03	4.246e-03	5.974e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

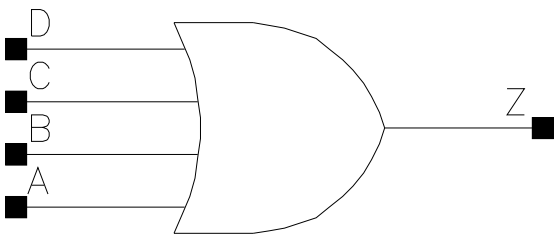
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	1.224	0.9792
X8_P4	0.800	1.496	1.1968
X12_P4	0.800	2.176	1.7408
X15_P4	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X12_P4	X15_P4
A	0.0004	0.0006	0.0011	0.0012
B	0.0005	0.0007	0.0010	0.0012
C	0.0004	0.0006	0.0011	0.0012
D	0.0005	0.0007	0.0010	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0325	0.0310	4.7537	2.5260
A to Z ↑	0.0199	0.0205	4.0109	2.1500
B to Z ↓	0.0338	0.0320	4.7533	2.5268
B to Z ↑	0.0191	0.0195	4.0131	2.1496
C to Z ↓	0.0346	0.0302	4.7648	2.5223
C to Z ↑	0.0207	0.0200	4.1198	2.1589

D to Z ↓	0.0363	0.0314	4.7627	2.5228
D to Z ↑	0.0201	0.0191	4.1155	2.1569
	X12_P4	**X15_P4**	**X12_P4**	**X15_P4**
A to Z ↓	0.0315	0.0320	1.7488	1.3126
A to Z ↑	0.0208	0.0200	1.3721	1.0545
B to Z ↓	0.0312	0.0312	1.7484	1.3125
B to Z ↑	0.0197	0.0183	1.3713	1.0533
C to Z ↓	0.0304	0.0305	1.7470	1.3105
C to Z ↑	0.0198	0.0191	1.3655	1.0617
D to Z ↓	0.0302	0.0300	1.7461	1.3103
D to Z ↑	0.0187	0.0177	1.3664	1.0601

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	1.114e-06	1.000e-20
X8_P4	2.655e-06	1.000e-20
X12_P4	3.223e-06	1.000e-20
X15_P4	4.828e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	4.214e-04	7.419e-04	1.145e-03	1.570e-03
B (output stable)	3.839e-04	6.711e-04	9.963e-04	1.337e-03
C (output stable)	4.190e-04	7.399e-04	1.084e-03	1.478e-03
D (output stable)	3.827e-04	6.702e-04	9.353e-04	1.281e-03
A to Z	1.755e-03	3.484e-03	4.935e-03	6.626e-03
B to Z	1.678e-03	3.330e-03	4.599e-03	6.063e-03
C to Z	1.781e-03	3.081e-03	4.376e-03	5.661e-03
D to Z	1.709e-03	2.932e-03	4.042e-03	5.202e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

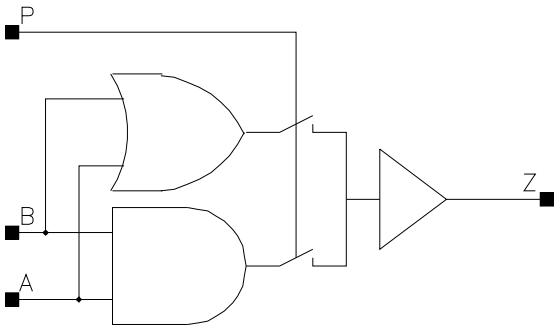
Pin Cycle (vdds)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.952	0.7616
X10_P4	1.600	0.816	1.3056
X14_P4	1.600	1.224	1.9584
X19_P4	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0009	0.0011	0.0021	0.0020
B	0.0009	0.0012	0.0021	0.0022
P	0.0005	0.0007	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0386	0.0351	3.0973	1.4425
A to Z ↑	0.0221	0.0256	4.3340	2.0679
B to Z ↓	0.0384	0.0358	3.1090	1.4491
B to Z ↑	0.0230	0.0269	4.3388	2.0691
P to Z ↓	0.0351	0.0339	3.1090	1.4494
P to Z ↑	0.0221	0.0264	4.3377	2.0683
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**

A to Z ↓	0.0325	0.0347	0.9954	0.7423
A to Z ↑	0.0248	0.0258	1.4185	1.0595
B to Z ↓	0.0310	0.0331	1.0058	0.7480
B to Z ↑	0.0245	0.0258	1.4203	1.0612
P to Z ↓	0.0302	0.0326	1.0081	0.7498
P to Z ↑	0.0247	0.0262	1.4195	1.0603

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.349e-06	1.000e-20
X10_P4	3.267e-06	1.000e-20
X14_P4	5.265e-06	1.000e-20
X19_P4	6.247e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	4.130e-05	5.983e-05	1.645e-04	1.565e-04
B (output stable)	4.926e-05	8.456e-05	2.928e-04	2.854e-04
P (output stable)	1.153e-04	1.726e-04	3.012e-04	2.949e-04
A to Z	1.933e-03	3.610e-03	5.842e-03	6.887e-03
B to Z	1.866e-03	3.547e-03	5.449e-03	6.496e-03
P to Z	1.683e-03	3.314e-03	5.283e-03	6.385e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

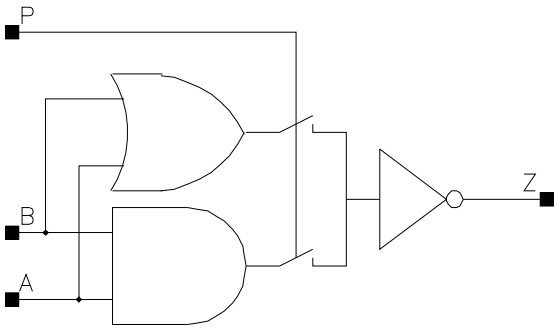
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.600	0.544	0.8704
X10_P4	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P4	X10_P4
A	0.0010	0.0019
B	0.0009	0.0017
P	0.0007	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0136	0.0128	4.8246	2.5273
A to Z ↑	0.0211	0.0197	7.9334	4.0293
B to Z ↓	0.0143	0.0123	4.7700	2.5364
B to Z ↑	0.0211	0.0178	7.9072	4.0821
P to Z ↓	0.0141	0.0117	4.8955	2.5627
P to Z ↑	0.0198	0.0160	7.9950	4.0578

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	1.488e-06	1.000e-20
X10_P4	2.731e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4
A (output stable)	5.816e-05	1.624e-04
B (output stable)	7.605e-05	2.792e-04
P (output stable)	1.473e-04	3.364e-04
A to Z	1.458e-03	2.592e-03
B to Z	1.356e-03	2.153e-03
P to Z	1.148e-03	1.886e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

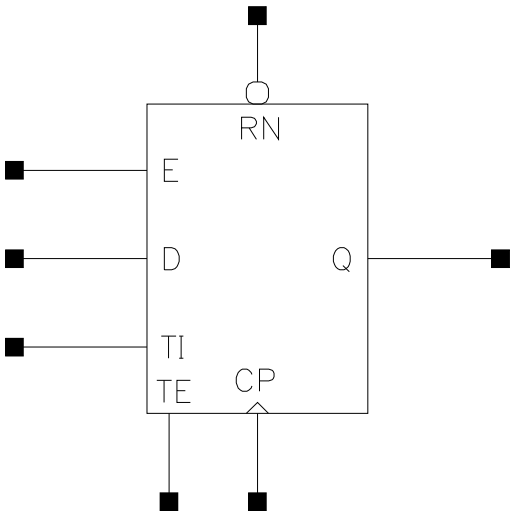
Pin Cycle (vdds)	X5_P4	X10_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.600	2.992	4.7872
X10_P4	1.600	3.128	5.0048
X19_P4	1.600	3.264	5.2224
X23_P4	1.600	3.264	5.2224
X29_P4	1.600	3.536	5.6576
X34_P4	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4	X23_P4
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0011	0.0011	0.0011	0.0011

RN	0.0009	0.0008	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P4	X34_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0011	0.0011		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
CP to Q ↓	0.0484	0.0770	2.8326	1.4207
CP to Q ↑	0.0654	0.1015	4.0703	2.0682
RN to Q ↓	0.0414	0.0748	2.8383	1.4201
	X19_P4	**X23_P4**	**X19_P4**	**X23_P4**
CP to Q ↓	0.0828	0.0836	0.7365	0.5544
CP to Q ↑	0.1053	0.1040	1.0450	1.0198
RN to Q ↓	0.0758	0.0766	0.7339	0.5525
	X29_P4	**X34_P4**	**X29_P4**	**X34_P4**
CP to Q ↓	0.0710	0.0705	0.4856	0.3835
CP to Q ↑	0.0856	0.0864	0.6920	0.6914
RN to Q ↓	0.0653	0.0647	0.4860	0.3836

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P4	X10_P4	X19_P4	X23_P4
CP ↓	min_pulse_width to CP	0.0594	0.0594	0.0594	0.0594
CP ↑	min_pulse_width to CP	0.0439	0.0439	0.0439	0.0439
D ↓	hold_rising to CP	-0.0365	-0.0365	-0.0365	-0.0365
D ↑	hold_rising to CP	-0.0094	-0.0094	-0.0094	-0.0094
D ↓	setup_rising to CP	0.0711	0.0711	0.0711	0.0711
D ↑	setup_rising to CP	0.0395	0.0395	0.0395	0.0395
E ↓	hold_rising to CP	-0.0337	-0.0332	-0.0337	-0.0337
E ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120	-0.0120
E ↓	setup_rising to CP	0.1008	0.1008	0.0949	0.0949
E ↑	setup_rising to CP	0.0737	0.0737	0.0737	0.0737
RN ↓	min_pulse_width to RN	0.0566	0.0496	0.0518	0.0540
RN ↑	recovery_rising to CP	0.0005	0.0005	0.0005	0.0005
RN ↑	removal_rising to CP	0.0091	0.0091	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0191	-0.0191	-0.0191	-0.0191

TE ↑	hold_rising to CP	-0.0071	-0.0071	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0586	0.0586	0.0586	0.0586
TE ↑	setup_rising to CP	0.0689	0.0689	0.0689	0.0689
TI ↓	hold_rising to CP	-0.0326	-0.0342	-0.0326	-0.0326
TI ↑	hold_rising to CP	-0.0058	-0.0058	-0.0058	-0.0058
TI ↓	setup_rising to CP	0.0689	0.0689	0.0689	0.0689
TI ↑	setup_rising to CP	0.0299	0.0299	0.0299	0.0299
		X29_P4	X34_P4		
CP ↓	min_pulse_width to CP	0.0601	0.0601		
CP ↑	min_pulse_width to CP	0.0439	0.0439		
D ↓	hold_rising to CP	-0.0365	-0.0365		
D ↑	hold_rising to CP	-0.0094	-0.0094		
D ↓	setup_rising to CP	0.0711	0.0711		
D ↑	setup_rising to CP	0.0395	0.0395		
E ↓	hold_rising to CP	-0.0337	-0.0337		
E ↑	hold_rising to CP	-0.0120	-0.0120		
E ↓	setup_rising to CP	0.1008	0.1008		
E ↑	setup_rising to CP	0.0737	0.0737		
RN ↓	min_pulse_width to RN	0.0566	0.0566		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0165	-0.0165		
TE ↑	hold_rising to CP	-0.0071	-0.0071		
TE ↓	setup_rising to CP	0.0586	0.0586		
TE ↑	setup_rising to CP	0.0689	0.0689		
TI ↓	hold_rising to CP	-0.0326	-0.0326		
TI ↑	hold_rising to CP	-0.0058	-0.0058		
TI ↓	setup_rising to CP	0.0689	0.0689		
TI ↑	setup_rising to CP	0.0299	0.0299		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	5.341e-06	1.000e-20
X10_P4	6.664e-06	1.000e-20
X19_P4	9.212e-06	1.000e-20
X23_P4	9.621e-06	1.000e-20

X29_P4	1.245e-05	1.000e-20
X34_P4	1.299e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

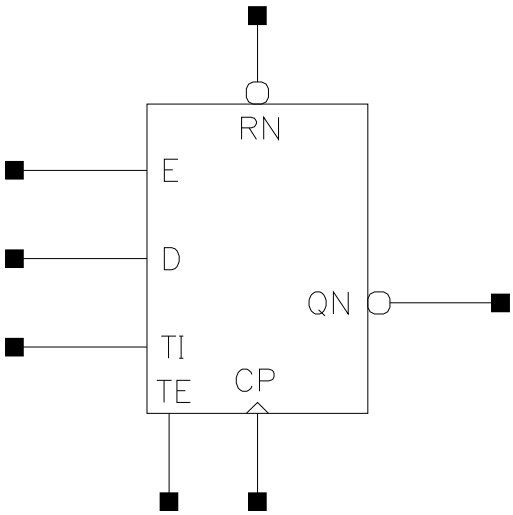
Pin Cycle	X5_P4	X10_P4	X19_P4	X23_P4
Clock 100Mhz Data 0Mhz	7.750e-03	7.742e-03	7.748e-03	7.752e-03
Clock 100Mhz Data 25Mhz	7.995e-03	8.432e-03	9.105e-03	9.160e-03
Clock 100Mhz Data 50Mhz	8.240e-03	9.123e-03	1.046e-02	1.057e-02
Clock = 0 Data 100Mhz	4.466e-03	4.466e-03	4.465e-03	4.465e-03
Clock = 1 Data 100Mhz	1.850e-03	1.849e-03	1.849e-03	1.849e-03
	X29_P4	X34_P4		
Clock 100Mhz Data 0Mhz	7.751e-03	7.752e-03		
Clock 100Mhz Data 25Mhz	9.853e-03	1.005e-02		
Clock 100Mhz Data 50Mhz	1.195e-02	1.235e-02		
Clock = 0 Data 100Mhz	4.466e-03	4.466e-03		
Clock = 1 Data 100Mhz	1.850e-03	1.851e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.600	2.992	4.7872
X10_P4	1.600	3.128	5.0048
X19_P4	1.600	3.264	5.2224
X23_P4	1.600	3.264	5.2224
X29_P4	1.600	3.536	5.6576
X34_P4	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4	X23_P4
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0011	0.0012	0.0012	0.0012

RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P4	X34_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0012	0.0011		
RN	0.0008	0.0009		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
CP to QN ↓	0.0895	0.0778	2.8378	1.4189
CP to QN ↑	0.0651	0.0607	4.0675	2.0663
RN to QN ↑	0.0626	0.0548	4.0634	2.0689
	X19_P4	**X23_P4**	**X19_P4**	**X23_P4**
CP to QN ↓	0.0817	0.0822	0.7301	0.5548
CP to QN ↑	0.0660	0.0641	1.0452	1.0209
RN to QN ↑	0.0605	0.0582	1.0445	1.0216
	X29_P4	**X34_P4**	**X29_P4**	**X34_P4**
CP to QN ↓	0.1109	0.1086	0.4858	0.3774
CP to QN ↑	0.0862	0.0849	0.6925	0.6913
RN to QN ↑	0.0835	0.0828	0.6926	0.6908

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P4	X10_P4	X19_P4	X23_P4
CP ↓	min_pulse_width to CP	0.0594	0.0601	0.0618	0.0601
CP ↑	min_pulse_width to CP	0.0439	0.0438	0.0439	0.0438
D ↓	hold_rising to CP	-0.0365	-0.0365	-0.0365	-0.0365
D ↑	hold_rising to CP	-0.0094	-0.0094	-0.0094	-0.0094
D ↓	setup_rising to CP	0.0711	0.0711	0.0711	0.0711
D ↑	setup_rising to CP	0.0395	0.0395	0.0395	0.0395
E ↓	hold_rising to CP	-0.0332	-0.0332	-0.0337	-0.0337
E ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120	-0.0120
E ↓	setup_rising to CP	0.1008	0.1003	0.1003	0.1003
E ↑	setup_rising to CP	0.0737	0.0737	0.0737	0.0737
RN ↓	min_pulse_width to RN	0.0496	0.0540	0.0588	0.0588
RN ↑	recovery_rising to CP	0.0005	0.0005	0.0005	0.0005
RN ↑	removal_rising to CP	0.0091	0.0091	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0191	-0.0165	-0.0165	-0.0165

TE ↑	hold_rising to CP	-0.0071	-0.0071	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0586	0.0586	0.0586	0.0586
TE ↑	setup_rising to CP	0.0689	0.0689	0.0689	0.0689
TI ↓	hold_rising to CP	-0.0326	-0.0326	-0.0326	-0.0326
TI ↑	hold_rising to CP	-0.0058	-0.0058	-0.0058	-0.0058
TI ↓	setup_rising to CP	0.0689	0.0689	0.0689	0.0689
TI ↑	setup_rising to CP	0.0299	0.0299	0.0299	0.0299
		X29_P4	X34_P4		
CP ↓	min_pulse_width to CP	0.0594	0.0594		
CP ↑	min_pulse_width to CP	0.0439	0.0423		
D ↓	hold_rising to CP	-0.0365	-0.0365		
D ↑	hold_rising to CP	-0.0094	-0.0094		
D ↓	setup_rising to CP	0.0711	0.0711		
D ↑	setup_rising to CP	0.0395	0.0395		
E ↓	hold_rising to CP	-0.0332	-0.0332		
E ↑	hold_rising to CP	-0.0120	-0.0120		
E ↓	setup_rising to CP	0.1003	0.0975		
E ↑	setup_rising to CP	0.0737	0.0737		
RN ↓	min_pulse_width to RN	0.0518	0.0496		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0191	-0.0191		
TE ↑	hold_rising to CP	-0.0071	-0.0071		
TE ↓	setup_rising to CP	0.0586	0.0586		
TE ↑	setup_rising to CP	0.0689	0.0689		
TI ↓	hold_rising to CP	-0.0326	-0.0326		
TI ↑	hold_rising to CP	-0.0058	-0.0058		
TI ↓	setup_rising to CP	0.0689	0.0689		
TI ↑	setup_rising to CP	0.0299	0.0299		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P4	5.180e-06	1.000e-20
X10_P4	6.336e-06	1.000e-20
X19_P4	8.625e-06	1.000e-20
X23_P4	9.291e-06	1.000e-20

X29_P4	1.136e-05	1.000e-20
X34_P4	1.219e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

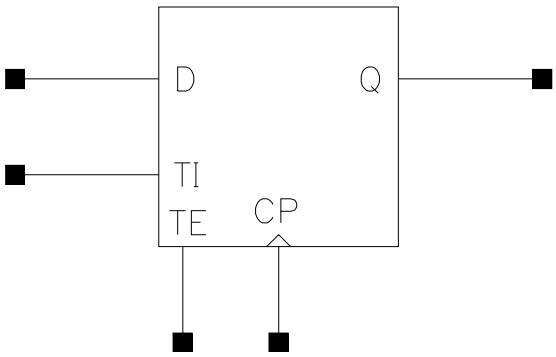
Pin Cycle	X5_P4	X10_P4	X19_P4	X23_P4
Clock 100Mhz Data 0Mhz	7.693e-03	7.704e-03	7.707e-03	7.708e-03
Clock 100Mhz Data 25Mhz	8.018e-03	8.379e-03	9.094e-03	9.132e-03
Clock 100Mhz Data 50Mhz	8.342e-03	9.055e-03	1.048e-02	1.056e-02
Clock = 0 Data 100Mhz	4.466e-03	4.466e-03	4.466e-03	4.466e-03
Clock = 1 Data 100Mhz	1.850e-03	1.849e-03	1.849e-03	1.850e-03
	X29_P4	X34_P4		
Clock 100Mhz Data 0Mhz	7.709e-03	7.708e-03		
Clock 100Mhz Data 25Mhz	9.879e-03	1.003e-02		
Clock 100Mhz Data 50Mhz	1.205e-02	1.235e-02		
Clock = 0 Data 100Mhz	4.467e-03	4.466e-03		
Clock = 1 Data 100Mhz	1.851e-03	1.851e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P4	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P4	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P4	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P4	C8T28SOI_LLHF_-SDFPQX3_P4	C8T28SOIDV_LL_-SDFPQX5_P4	C8T28SOIDV_LL_-SDFPQX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P4	C8T28SOIDV_LL_-SDFPQX23_P4	C8T28SOIDV_LL_-SDFPQX29_P4	
CP	0.0005	0.0005	0.0005	
D	0.0005	0.0005	0.0005	
TE	0.0009	0.0009	0.0009	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P4	**C8T28SOI_LLHF_-SDFPQX3_P4**	**C8T28SOI_LL_-SDFPQX5_P4**	**C8T28SOI_LLHF_-SDFPQX3_P4**
CP to Q ↓	0.0503	0.0429	2.9768	4.5585
CP to Q ↑	0.0481	0.0553	4.1102	6.3085
	C8T28SOIDV_LL_-SDFPQX5_P4	**C8T28SOIDV_LL_-SDFPQX10_P4**	**C8T28SOIDV_LL_-SDFPQX5_P4**	**C8T28SOIDV_LL_-SDFPQX10_P4**
CP to Q ↓	0.0449	0.0624	2.8284	1.3751
CP to Q ↑	0.0558	0.0797	4.0675	2.0403
	C8T28SOIDV_LL_-SDFPQX19_P4	**C8T28SOIDV_LL_-SDFPQX23_P4**	**C8T28SOIDV_LL_-SDFPQX19_P4**	**C8T28SOIDV_LL_-SDFPQX23_P4**
CP to Q ↓	0.0676	0.0697	0.7161	0.5508
CP to Q ↑	0.0844	0.0864	1.0314	1.0217
	C8T28SOIDV_LL_-SDFPQX29_P4		**C8T28SOIDV_LL_-SDFPQX29_P4**	
CP to Q ↓	0.0667		0.4808	
CP to Q ↑	0.0807		0.6843	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P4	C8T28SOI_-LLHF_-SDFPQX3_P4	C8T28SOIDV_-LL_SDFPQX5_-P4	C8T28SOIDV_-LL_SDFPQX10_-P4
CP ↓	min_pulse_width to CP	0.0796	0.0768	0.0658	0.0658
CP ↑	min_pulse_width to CP	0.0408	0.0363	0.0393	0.0360
D ↓	hold_rising to CP	-0.0338	-0.0746	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0071	-0.0045	0.0032	0.0032
D ↓	setup_rising to CP	0.0684	0.1143	0.0440	0.0440
D ↑	setup_rising to CP	0.0314	0.0343	0.0249	0.0249
TE ↓	hold_rising to CP	-0.0181	-0.0235	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0044	-0.0013	-0.0049	-0.0049
TE ↓	setup_rising to CP	0.0663	0.0927	0.0419	0.0419
TE ↑	setup_rising to CP	0.0786	0.1079	0.0786	0.0786

TI ↓	hold_rising to CP	-0.0475	-0.0716	-0.0391	-0.0391
TI ↑	hold_rising to CP	-0.0056	-0.0043	-0.0056	-0.0056
TI ↓	setup_rising to CP	0.0822	0.1055	0.0786	0.0793
TI ↑	setup_rising to CP	0.0297	0.0291	0.0312	0.0312
		C8T28SOIDV_-LL_SDFPQX19_-P4	C8T28SOIDV_-LL_SDFPQX23_-P4	C8T28SOIDV_-LL_SDFPQX29_-P4	
CP ↓	min_pulse_width to CP	0.0658	0.0658	0.0675	
CP ↑	min_pulse_width to CP	0.0359	0.0359	0.0359	
D ↓	hold_rising to CP	-0.0045	-0.0045	-0.0077	
D ↑	hold_rising to CP	0.0032	0.0032	0.0032	
D ↓	setup_rising to CP	0.0440	0.0440	0.0440	
D ↑	setup_rising to CP	0.0249	0.0249	0.0249	
TE ↓	hold_rising to CP	-0.0023	-0.0023	-0.0023	
TE ↑	hold_rising to CP	-0.0049	-0.0049	-0.0049	
TE ↓	setup_rising to CP	0.0419	0.0419	0.0419	
TE ↑	setup_rising to CP	0.0786	0.0786	0.0786	
TI ↓	hold_rising to CP	-0.0391	-0.0391	-0.0391	
TI ↑	hold_rising to CP	-0.0056	-0.0056	-0.0056	
TI ↓	setup_rising to CP	0.0793	0.0793	0.0786	
TI ↑	setup_rising to CP	0.0297	0.0297	0.0312	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P4	4.475e-06	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P4	3.771e-06	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P4	4.188e-06	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P4	5.932e-06	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P4	7.479e-06	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P4	8.081e-06	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P4	1.003e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P4	C8T28SOI_LLHF_-SDFPQX3_P4	C8T28SOIDV_LL_-SDFPQX5_P4	C8T28SOIDV_LL_-SDFPQX10_P4
Clock 100Mhz Data 0Mhz	7.471e-03	7.176e-03	6.882e-03	6.730e-03
Clock 100Mhz Data 25Mhz	7.147e-03	6.870e-03	6.702e-03	7.015e-03
Clock 100Mhz Data 50Mhz	6.822e-03	6.563e-03	6.522e-03	7.299e-03

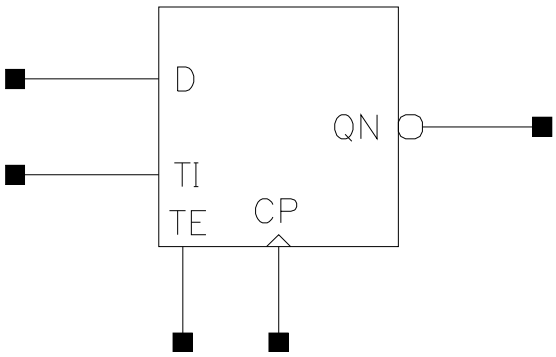
Clock = 0 Data 100Mhz	3.512e-03	3.654e-03	3.467e-03	3.371e-03
Clock = 1 Data 100Mhz	3.623e-05	4.840e-04	3.359e-04	2.619e-04
	C8T28SOIDV_LL_-SDFPQX19_P4	C8T28SOIDV_LL_-SDFPQX23_P4	C8T28SOIDV_LL_-SDFPQX29_P4	
Clock 100Mhz Data 0Mhz	6.642e-03	6.584e-03	6.543e-03	
Clock 100Mhz Data 25Mhz	7.501e-03	7.523e-03	8.054e-03	
Clock 100Mhz Data 50Mhz	8.361e-03	8.463e-03	9.564e-03	
Clock = 0 Data 100Mhz	3.312e-03	3.272e-03	3.246e-03	
Clock = 1 Data 100Mhz	2.176e-04	1.880e-04	1.669e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P4	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P4	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P4	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P4	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P4	C8T28SOI_LLHF_-SDFPQNX3_P4	C8T28SOIDV_LL_-SDFPQNX5_P4	C8T28SOIDV_LL_-SDFPQNX10_P4

CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P4	C8T28SOIDV_LL_-SDFPQNX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P4	**C8T28SOI_LLHF_-SDFPQNX3_P4**	**C8T28SOI_LL_-SDFPQNX5_P4**	**C8T28SOI_LLHF_-SDFPQNX3_P4**
CP to QN ↓	0.0622	0.0665	2.8676	4.2979
CP to QN ↑	0.0551	0.0523	4.4463	6.1346
	C8T28SOIDV_LL_-SDFPQNX5_P4	**C8T28SOIDV_LL_-SDFPQNX10_P4**	**C8T28SOIDV_LL_-SDFPQNX5_P4**	**C8T28SOIDV_LL_-SDFPQNX10_P4**
CP to QN ↓	0.0684	0.0647	2.7781	1.3861
CP to QN ↑	0.0510	0.0550	4.0218	2.0419
	C8T28SOIDV_LL_-SDFPQNX19_P4	**C8T28SOIDV_LL_-SDFPQNX29_P4**	**C8T28SOIDV_LL_-SDFPQNX19_P4**	**C8T28SOIDV_LL_-SDFPQNX29_P4**
CP to QN ↓	0.0723	0.0841	0.7237	0.4908
CP to QN ↑	0.0645	0.0724	1.0504	0.6887

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P4	C8T28SOI_-LLHF_-SDFPQNX3_P4	C8T28SOIDV_-LL_SDFPQNX5_-P4	C8T28SOIDV_-LL_-SDFPQNX10_P4
CP ↓	min_pulse_width to CP	0.0796	0.0762	0.0658	0.0658
CP ↑	min_pulse_width to CP	0.0347	0.0316	0.0360	0.0392
D ↓	hold_rising to CP	-0.0338	-0.0750	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0071	-0.0040	0.0032	0.0032
D ↓	setup_rising to CP	0.0684	0.1143	0.0440	0.0440
D ↑	setup_rising to CP	0.0310	0.0343	0.0249	0.0249
TE ↓	hold_rising to CP	-0.0181	-0.0235	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0044	-0.0013	-0.0049	-0.0049
TE ↓	setup_rising to CP	0.0663	0.0927	0.0419	0.0419
TE ↑	setup_rising to CP	0.0786	0.1053	0.0786	0.0786
TI ↓	hold_rising to CP	-0.0475	-0.0707	-0.0391	-0.0391
TI ↑	hold_rising to CP	-0.0056	-0.0043	-0.0058	-0.0056
TI ↓	setup_rising to CP	0.0822	0.1055	0.0786	0.0786
TI ↑	setup_rising to CP	0.0297	0.0291	0.0306	0.0312

		C8T28SOIDV_-LL_-SDFPQNX19_P4	C8T28SOIDV_-LL_-SDFPQNX29_P4		
CP ↓	min_pulse_width to CP	0.0658	0.0658		
CP ↑	min_pulse_width to CP	0.0405	0.0359		
D ↓	hold_rising to CP	-0.0045	-0.0045		
D ↑	hold_rising to CP	0.0032	0.0032		
D ↓	setup_rising to CP	0.0440	0.0440		
D ↑	setup_rising to CP	0.0249	0.0249		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0049	-0.0049		
TE ↓	setup_rising to CP	0.0419	0.0419		
TE ↑	setup_rising to CP	0.0786	0.0786		
TI ↓	hold_rising to CP	-0.0391	-0.0391		
TI ↑	hold_rising to CP	-0.0056	-0.0056		
TI ↓	setup_rising to CP	0.0786	0.0786		
TI ↑	setup_rising to CP	0.0297	0.0312		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P4	4.417e-06	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P4	3.830e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P4	4.227e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P4	5.817e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P4	7.511e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P4	1.198e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P4	C8T28SOI_LLHF_-SDFPQNX3_P4	C8T28SOIDV_LL_-SDFPQNX5_P4	C8T28SOIDV_LL_-SDFPQNX10_P4
Clock 100Mhz Data 0Mhz	7.479e-03	7.252e-03	6.942e-03	6.775e-03
Clock 100Mhz Data 25Mhz	7.115e-03	6.957e-03	6.681e-03	6.985e-03
Clock 100Mhz Data 50Mhz	6.752e-03	6.661e-03	6.419e-03	7.196e-03
Clock = 0 Data 100Mhz	3.513e-03	3.668e-03	3.482e-03	3.384e-03
Clock = 1 Data 100Mhz	4.511e-05	4.916e-04	3.423e-04	2.677e-04
	C8T28SOIDV_LL_-SDFPQNX19_P4	C8T28SOIDV_LL_-SDFPQNX29_P4		
Clock 100Mhz Data 0Mhz	6.679e-03	6.612e-03		

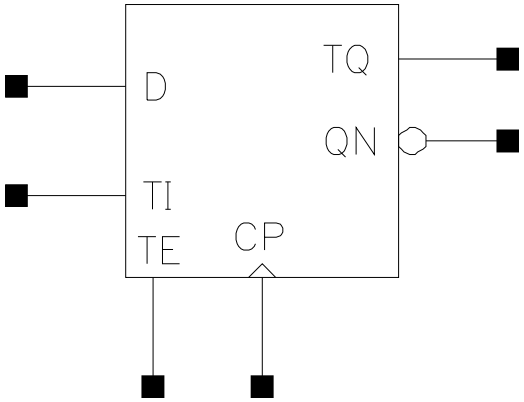
Clock 100Mhz Data 25Mhz	7.593e-03	8.544e-03		
Clock 100Mhz Data 50Mhz	8.507e-03	1.048e-02		
Clock = 0 Data 100Mhz	3.320e-03	3.282e-03		
Clock = 1 Data 100Mhz	2.230e-04	1.932e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P4	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P4	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P4	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P4	C8T28SOI_LLHF_-SDFPQNTX3_P4	C8T28SOIDV_LL_-SDFPQNTX5_P4	C8T28SOIDV_LL_-SDFPQNTX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P4	C8T28SOIDV_LL_-SDFPQNTX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNTX5_P4	**C8T28SOI_LLHF_-SDFPQNTX3_P4**	**C8T28SOI_LL_-SDFPQNTX5_P4**	**C8T28SOI_LLHF_-SDFPQNTX3_P4**
CP to QN ↓	0.0701	0.0725	2.9769	4.3702
CP to QN ↑	0.0698	0.0641	4.4548	6.1625
CP to TQ ↓	0.0585	0.0452	7.7165	5.0608
CP to TQ ↑	0.0602	0.0547	20.5211	10.9984
	C8T28SOIDV_LL_-SDFPQNTX5_P4	**C8T28SOIDV_LL_-SDFPQNTX10_P4**	**C8T28SOIDV_LL_-SDFPQNTX5_P4**	**C8T28SOIDV_LL_-SDFPQNTX10_P4**
CP to QN ↓	0.0735	0.0715	2.7328	1.3972
CP to QN ↑	0.0597	0.0600	4.0267	2.0461
CP to TQ ↓	0.0423	0.0440	5.0630	5.2447
CP to TQ ↑	0.0557	0.0569	8.7469	9.0846
	C8T28SOIDV_LL_-SDFPQNTX19_P4	**C8T28SOIDV_LL_-SDFPQNTX29_P4**	**C8T28SOIDV_LL_-SDFPQNTX19_P4**	**C8T28SOIDV_LL_-SDFPQNTX29_P4**
CP to QN ↓	0.0735	0.0861	0.7203	0.4927
CP to QN ↑	0.0650	0.0769	1.0420	0.6880
CP to TQ ↓	0.0458	0.0444	5.1769	5.2846
CP to TQ ↑	0.0587	0.0590	9.3225	11.7422

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_P4	C8T28SOI_-LLHF_-SDFPQNTX3_P4	C8T28SOIDV_-LL_-SDFPQNTX5_P4	C8T28SOIDV_-LL_-SDFPQNTX10_-P4
CP ↓	min_pulse_width to CP	0.0796	0.0762	0.0658	0.0658
CP ↑	min_pulse_width to CP	0.0455	0.0409	0.0392	0.0392
D ↓	hold_rising to CP	-0.0338	-0.0750	-0.0077	-0.0045
D ↑	hold_rising to CP	-0.0071	-0.0040	0.0032	0.0032
D ↓	setup_rising to CP	0.0684	0.1115	0.0440	0.0440

D ↑	setup_rising to CP	0.0310	0.0343	0.0249	0.0249
TE ↓	hold_rising to CP	-0.0181	-0.0235	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0049	-0.0013	-0.0049	-0.0049
TE ↓	setup_rising to CP	0.0663	0.0895	0.0419	0.0419
TE ↑	setup_rising to CP	0.0786	0.1053	0.0786	0.0786
TI ↓	hold_rising to CP	-0.0475	-0.0707	-0.0391	-0.0391
TI ↑	hold_rising to CP	-0.0056	-0.0043	-0.0058	-0.0056
TI ↓	setup_rising to CP	0.0822	0.1055	0.0786	0.0786
TI ↑	setup_rising to CP	0.0297	0.0284	0.0306	0.0312
		C8T28SOIDV_-LL_-SDFPQNTX19_-P4	C8T28SOIDV_-LL_-SDFPQNTX29_-P4		
CP ↓	min_pulse_width to CP	0.0658	0.0658		
CP ↑	min_pulse_width to CP	0.0405	0.0392		
D ↓	hold_rising to CP	-0.0045	-0.0045		
D ↑	hold_rising to CP	0.0032	0.0032		
D ↓	setup_rising to CP	0.0440	0.0440		
D ↑	setup_rising to CP	0.0249	0.0249		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0049	-0.0049		
TE ↓	setup_rising to CP	0.0419	0.0419		
TE ↑	setup_rising to CP	0.0786	0.0786		
TI ↓	hold_rising to CP	-0.0391	-0.0391		
TI ↑	hold_rising to CP	-0.0056	-0.0056		
TI ↓	setup_rising to CP	0.0786	0.0786		
TI ↑	setup_rising to CP	0.0297	0.0312		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P4	4.387e-06	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P4	4.069e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P4	4.492e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P4	5.440e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P4	7.426e-06	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P4	1.189e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

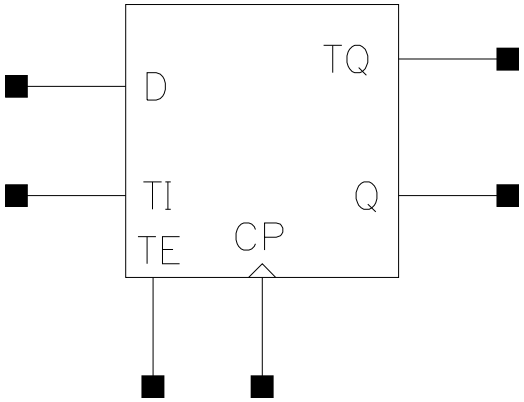
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P4	C8T28SOI_LLHF_-SDFPQNTX3_P4	C8T28SOIDV_LL_-SDFPQNTX5_P4	C8T28SOIDV_LL_-SDFPQNTX10_P4
Clock 100Mhz Data 0Mhz	7.475e-03	7.248e-03	6.934e-03	6.768e-03
Clock 100Mhz Data 25Mhz	7.400e-03	7.169e-03	6.888e-03	6.973e-03
Clock 100Mhz Data 50Mhz	7.326e-03	7.089e-03	6.842e-03	7.178e-03
Clock = 0 Data 100Mhz	3.513e-03	3.667e-03	3.483e-03	3.384e-03
Clock = 1 Data 100Mhz	3.644e-05	4.896e-04	3.396e-04	2.647e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P4	C8T28SOIDV_LL_-SDFPQNTX29_P4		
Clock 100Mhz Data 0Mhz	6.669e-03	6.601e-03		
Clock 100Mhz Data 25Mhz	7.520e-03	8.696e-03		
Clock 100Mhz Data 50Mhz	8.371e-03	1.079e-02		
Clock = 0 Data 100Mhz	3.324e-03	3.285e-03		
Clock = 1 Data 100Mhz	2.198e-04	1.899e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P4	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P4	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P4	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P4	C8T28SOI_LLHF_-SDFPQTX3_P4	C8T28SOIDV_LL_-SDFPQTX5_P4	C8T28SOIDV_LL_-SDFPQTX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P4	C8T28SOIDV_LL_-SDFPQTX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQTX5_P4	**C8T28SOI_LLHF_-SDFPQTX3_P4**	**C8T28SOI_LL_-SDFPQTX5_P4**	**C8T28SOI_LLHF_-SDFPQTX3_P4**
CP to Q ↓	0.0590	0.0545	3.1629	4.7321
CP to Q ↑	0.0521	0.0557	4.1410	6.4098
CP to TQ ↓	0.0713	0.0536	8.4303	5.2248
CP to TQ ↑	0.0664	0.0588	20.7674	11.1826
	C8T28SOIDV_LL_-SDFPQTX5_P4	**C8T28SOIDV_LL_-SDFPQTX10_P4**	**C8T28SOIDV_LL_-SDFPQTX5_P4**	**C8T28SOIDV_LL_-SDFPQTX10_P4**
CP to Q ↓	0.0487	0.0640	2.8985	1.3817
CP to Q ↑	0.0576	0.0811	4.1270	2.0415
CP to TQ ↓	0.0486	0.0660	5.2184	5.2864
CP to TQ ↑	0.0594	0.0843	9.5940	9.4365
	C8T28SOIDV_LL_-SDFPQTX19_P4	**C8T28SOIDV_LL_-SDFPQTX29_P4**	**C8T28SOIDV_LL_-SDFPQTX19_P4**	**C8T28SOIDV_LL_-SDFPQTX29_P4**
CP to Q ↓	0.0691	0.0752	0.7188	0.4686
CP to Q ↑	0.0851	0.0842	1.0340	0.6819
CP to TQ ↓	0.0722	0.0470	5.3326	5.4450
CP to TQ ↑	0.0900	0.0604	9.4685	11.7561

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P4	C8T28SOI_-LLHF_-SDFPQTX3_P4	C8T28SOIDV_-LL_SDFPQTX5_-P4	C8T28SOIDV_-LL_-SDFPQTX10_P4
CP ↓	min_pulse_width to CP	0.0796	0.0762	0.0658	0.0658
CP ↑	min_pulse_width to CP	0.0501	0.0409	0.0406	0.0360
D ↓	hold_rising to CP	-0.0338	-0.0750	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0071	-0.0040	0.0032	0.0032
D ↓	setup_rising to CP	0.0684	0.1143	0.0440	0.0440

D ↑	setup_rising to CP	0.0314	0.0343	0.0249	0.0249
TE ↓	hold_rising to CP	-0.0181	-0.0235	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0044	-0.0013	-0.0049	-0.0049
TE ↓	setup_rising to CP	0.0663	0.0895	0.0419	0.0419
TE ↑	setup_rising to CP	0.0813	0.1053	0.0786	0.0786
TI ↓	hold_rising to CP	-0.0475	-0.0707	-0.0391	-0.0391
TI ↑	hold_rising to CP	-0.0056	-0.0043	-0.0056	-0.0056
TI ↓	setup_rising to CP	0.0822	0.1055	0.0786	0.0793
TI ↑	setup_rising to CP	0.0297	0.0291	0.0312	0.0312
		C8T28SOIDV_-LL_-SDFPQTX19_P4	C8T28SOIDV_-LL_-SDFPQTX29_P4		
CP ↓	min_pulse_width to CP	0.0658	0.0658		
CP ↑	min_pulse_width to CP	0.0359	0.0407		
D ↓	hold_rising to CP	-0.0045	-0.0077		
D ↑	hold_rising to CP	0.0032	0.0032		
D ↓	setup_rising to CP	0.0440	0.0440		
D ↑	setup_rising to CP	0.0249	0.0249		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0049	-0.0049		
TE ↓	setup_rising to CP	0.0419	0.0419		
TE ↑	setup_rising to CP	0.0786	0.0786		
TI ↓	hold_rising to CP	-0.0391	-0.0391		
TI ↑	hold_rising to CP	-0.0056	-0.0056		
TI ↓	setup_rising to CP	0.0793	0.0786		
TI ↑	setup_rising to CP	0.0312	0.0312		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P4	4.503e-06	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P4	4.068e-06	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P4	4.464e-06	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P4	6.193e-06	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P4	7.804e-06	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P4	1.050e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

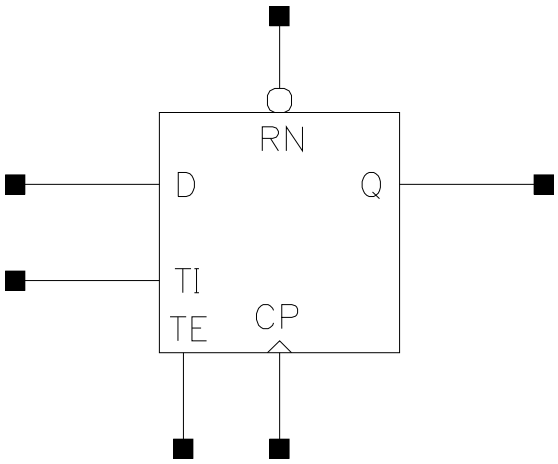
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P4	C8T28SOI_LLHF_-SDFPQTX3_P4	C8T28SOIDV_LL_-SDFPQTX5_P4	C8T28SOIDV_LL_-SDFPQTX10_P4
Clock 100Mhz Data 0Mhz	7.475e-03	7.240e-03	6.926e-03	6.762e-03
Clock 100Mhz Data 25Mhz	7.414e-03	7.157e-03	6.899e-03	7.197e-03
Clock 100Mhz Data 50Mhz	7.354e-03	7.075e-03	6.873e-03	7.632e-03
Clock = 0 Data 100Mhz	3.521e-03	3.673e-03	3.481e-03	3.382e-03
Clock = 1 Data 100Mhz	3.642e-05	4.879e-04	3.386e-04	2.640e-04
	C8T28SOIDV_LL_-SDFPQTX19_P4	C8T28SOIDV_LL_-SDFPQTX29_P4		
Clock 100Mhz Data 0Mhz	6.668e-03	6.609e-03		
Clock 100Mhz Data 25Mhz	7.706e-03	8.295e-03		
Clock 100Mhz Data 50Mhz	8.744e-03	9.980e-03		
Clock = 0 Data 100Mhz	3.321e-03	3.284e-03		
Clock = 1 Data 100Mhz	2.192e-04	1.894e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P4	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P4	C8T28SOI_LLHF_-SDFPRQX3_P4	C8T28SOIDV_LL_-SDFPRQX5_P4	C8T28SOIDV_LL_-SDFPRQX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0009	0.0009
TE	0.0010	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P4	C8T28SOIDV_LL_-SDFPRQX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0009	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P4	**C8T28SOI_LLHF_-SDFPRQX3_P4**	**C8T28SOI_LL_-SDFPRQX5_P4**	**C8T28SOI_LLHF_-SDFPRQX3_P4**
CP to Q ↓	0.0571	0.0521	2.9939	4.5874
CP to Q ↑	0.0501	0.0554	4.1074	6.2342
RN to Q ↓	0.0519	0.0509	2.7903	4.3161
	C8T28SOIDV_LL_-SDFPRQX5_P4	**C8T28SOIDV_LL_-SDFPRQX10_P4**	**C8T28SOIDV_LL_-SDFPRQX5_P4**	**C8T28SOIDV_LL_-SDFPRQX10_P4**
CP to Q ↓	0.0456	0.0640	2.8207	1.3914
CP to Q ↑	0.0583	0.0828	4.0624	2.0461
RN to Q ↓	0.0428	0.0657	2.7980	1.3893
	C8T28SOIDV_LL_-SDFPRQX19_P4	**C8T28SOIDV_LL_-SDFPRQX29_P4**	**C8T28SOIDV_LL_-SDFPRQX19_P4**	**C8T28SOIDV_LL_-SDFPRQX29_P4**
CP to Q ↓	0.0683	0.0694	0.7174	0.4909
CP to Q ↑	0.0869	0.0901	1.0487	0.7143
RN to Q ↓	0.0702	0.0712	0.7174	0.4903

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P4	C8T28SOI_-LLHF_-SDFPRQX3_P4	C8T28SOIDV_-LL_SDFPRQX5_-P4	C8T28SOIDV_-LL_-SDFPRQX10_P4
CP ↓	min_pulse_width to CP	0.0796	0.0762	0.0699	0.0699
CP ↑	min_pulse_width to CP	0.0455	0.0409	0.0393	0.0359
D ↓	hold_rising to CP	-0.0338	-0.0718	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0066	-0.0066	0.0004	0.0004
D ↓	setup_rising to CP	0.0684	0.1094	0.0440	0.0440
D ↑	setup_rising to CP	0.0369	0.0363	0.0245	0.0245
RN ↓	min_pulse_width to RN	0.0544	0.0544	0.0518	0.0469
RN ↑	recovery_rising to CP	0.0054	0.0054	0.0032	0.0054
RN ↑	removal_rising to CP	0.0042	0.0043	0.0043	0.0043

TE ↓	hold_rising to CP	-0.0240	-0.0230	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0039	-0.0071	-0.0039	-0.0066
TE ↓	setup_rising to CP	0.0663	0.0878	0.0419	0.0419
TE ↑	setup_rising to CP	0.0813	0.1057	0.0786	0.0786
TI ↓	hold_rising to CP	-0.0475	-0.0707	-0.0391	-0.0391
TI ↑	hold_rising to CP	-0.0049	-0.0043	-0.0107	-0.0107
TI ↓	setup_rising to CP	0.0822	0.1055	0.0786	0.0786
TI ↑	setup_rising to CP	0.0355	0.0299	0.0355	0.0355
		C8T28SOIDV_-LL_-SDFPRQX19_P4	C8T28SOIDV_-LL_-SDFPRQX29_P4		
CP ↓	min_pulse_width to CP	0.0699	0.0699		
CP ↑	min_pulse_width to CP	0.0360	0.0359		
D ↓	hold_rising to CP	-0.0045	-0.0045		
D ↑	hold_rising to CP	0.0004	0.0004		
D ↓	setup_rising to CP	0.0440	0.0440		
D ↑	setup_rising to CP	0.0245	0.0245		
RN ↓	min_pulse_width to RN	0.0469	0.0469		
RN ↑	recovery_rising to CP	0.0054	0.0037		
RN ↑	removal_rising to CP	0.0043	0.0043		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0066	-0.0066		
TE ↓	setup_rising to CP	0.0419	0.0419		
TE ↑	setup_rising to CP	0.0786	0.0786		
TI ↓	hold_rising to CP	-0.0391	-0.0391		
TI ↑	hold_rising to CP	-0.0107	-0.0107		
TI ↓	setup_rising to CP	0.0786	0.0786		
TI ↑	setup_rising to CP	0.0355	0.0355		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P4	4.748e-06	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P4	4.120e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P4	4.527e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P4	6.143e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQX19_P4	8.004e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P4	1.026e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

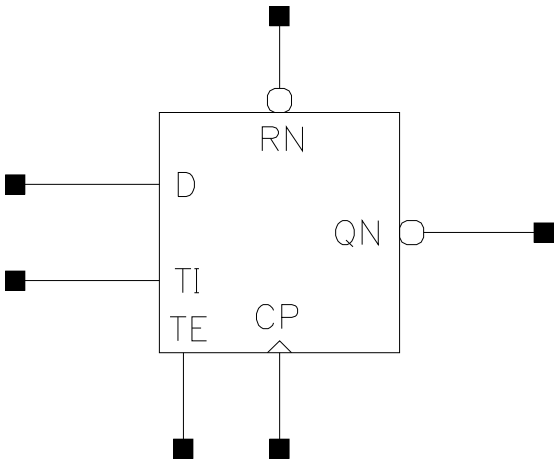
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P4	C8T28SOI_LLHF_-SDFPRQX3_P4	C8T28SOIDV_LL_-SDFPRQX5_P4	C8T28SOIDV_LL_-SDFPRQX10_P4
Clock 100Mhz Data 0Mhz	7.757e-03	7.462e-03	7.123e-03	6.954e-03
Clock 100Mhz Data 25Mhz	7.420e-03	7.180e-03	6.877e-03	7.221e-03
Clock 100Mhz Data 50Mhz	7.083e-03	6.897e-03	6.630e-03	7.488e-03
Clock = 0 Data 100Mhz	3.392e-03	3.574e-03	3.447e-03	3.385e-03
Clock = 1 Data 100Mhz	4.443e-05	4.953e-04	3.439e-04	2.683e-04
	C8T28SOIDV_LL_-SDFPRQX19_P4	C8T28SOIDV_LL_-SDFPRQX29_P4		
Clock 100Mhz Data 0Mhz	6.852e-03	6.785e-03		
Clock 100Mhz Data 25Mhz	7.687e-03	8.361e-03		
Clock 100Mhz Data 50Mhz	8.522e-03	9.936e-03		
Clock = 0 Data 100Mhz	3.347e-03	3.324e-03		
Clock = 1 Data 100Mhz	2.229e-04	1.927e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P4	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P4	C8T28SOI_LLHF_-SDFPRQNX3_P4	C8T28SOIDV_LL_-SDFPRQNX5_P4	C8T28SOIDV_LL_-SDFPRQNX10_P4
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0009	0.0008
TE	0.0010	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P4	C8T28SOIDV_LL_-SDFPRQNX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0007	0.0007		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNX5_P4	**C8T28SOI_LLHF_-SDFPRQNX3_P4**	**C8T28SOI_LL_-SDFPRQNX5_P4**	**C8T28SOI_LLHF_-SDFPRQNX3_P4**
CP to QN ↓	0.0655	0.0695	2.9406	4.3039
CP to QN ↑	0.0608	0.0572	4.2490	6.1313
RN to QN ↑	0.0605	0.0595	4.2361	6.1282
	C8T28SOIDV_LL_-SDFPRQNX5_P4	**C8T28SOIDV_LL_-SDFPRQNX10_P4**	**C8T28SOIDV_LL_-SDFPRQNX5_P4**	**C8T28SOIDV_LL_-SDFPRQNX10_P4**
CP to QN ↓	0.0741	0.0674	2.7208	1.3919
CP to QN ↑	0.0567	0.0557	4.0194	2.0443
RN to QN ↑	0.0536	0.0532	4.0134	2.0448
	C8T28SOIDV_LL_-SDFPRQNX19_P4	**C8T28SOIDV_LL_-SDFPRQNX29_P4**	**C8T28SOIDV_LL_-SDFPRQNX19_P4**	**C8T28SOIDV_LL_-SDFPRQNX29_P4**
CP to QN ↓	0.0747	0.0798	0.7352	0.4937
CP to QN ↑	0.0615	0.0689	1.0537	0.7100
RN to QN ↑	0.0575	0.0663	1.0533	0.7102

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P4	C8T28SOI_-LLHF_-SDFPRQNX3_-P4	C8T28SOIDV_-LL_-SDFPRQNX5_-P4	C8T28SOIDV_-LL_-SDFPRQNX10_-P4
CP ↓	min_pulse_width to CP	0.0796	0.0762	0.0699	0.0699
CP ↑	min_pulse_width to CP	0.0360	0.0362	0.0359	0.0392
D ↓	hold_rising to CP	-0.0338	-0.0697	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0066	-0.0066	-0.0000	0.0004
D ↓	setup_rising to CP	0.0684	0.1094	0.0440	0.0440
D ↑	setup_rising to CP	0.0369	0.0363	0.0245	0.0245
RN ↓	min_pulse_width to RN	0.0544	0.0544	0.0469	0.0540
RN ↑	recovery_rising to CP	0.0054	0.0054	0.0032	0.0032

RN ↑	removal_rising to CP	0.0042	0.0043	0.0043	0.0043
TE ↓	hold_rising to CP	-0.0240	-0.0230	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0039	-0.0071	-0.0039	-0.0039
TE ↓	setup_rising to CP	0.0663	0.0878	0.0419	0.0419
TE ↑	setup_rising to CP	0.0813	0.1025	0.0786	0.0786
TI ↓	hold_rising to CP	-0.0475	-0.0710	-0.0391	-0.0391
TI ↑	hold_rising to CP	-0.0049	-0.0036	-0.0064	-0.0107
TI ↓	setup_rising to CP	0.0822	0.1012	0.0786	0.0786
TI ↑	setup_rising to CP	0.0355	0.0299	0.0355	0.0355
		C8T28SOIDV_-LL_-SDFPRQNX19_-P4	C8T28SOIDV_-LL_-SDFPRQNX29_-P4		
CP ↓	min_pulse_width to CP	0.0699	0.0705		
CP ↑	min_pulse_width to CP	0.0406	0.0452		
D ↓	hold_rising to CP	-0.0045	-0.0045		
D ↑	hold_rising to CP	-0.0000	-0.0000		
D ↓	setup_rising to CP	0.0440	0.0440		
D ↑	setup_rising to CP	0.0245	0.0245		
RN ↓	min_pulse_width to RN	0.0540	0.0659		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0043	0.0043		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0039	-0.0039		
TE ↓	setup_rising to CP	0.0419	0.0419		
TE ↑	setup_rising to CP	0.0786	0.0786		
TI ↓	hold_rising to CP	-0.0339	-0.0339		
TI ↑	hold_rising to CP	-0.0064	-0.0064		
TI ↓	setup_rising to CP	0.0786	0.0786		
TI ↑	setup_rising to CP	0.0355	0.0355		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P4	4.554e-06	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P4	4.105e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P4	4.361e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P4	5.959e-06	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P4	7.154e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P4	9.355e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

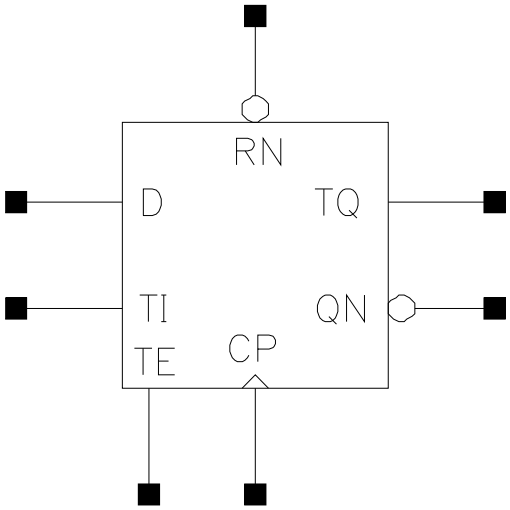
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P4	C8T28SOI_LLHF_-SDFPRQNX3_P4	C8T28SOIDV_LL_-SDFPRQNX5_P4	C8T28SOIDV_LL_-SDFPRQNX10_P4
Clock 100Mhz Data 0Mhz	7.691e-03	7.396e-03	7.070e-03	6.907e-03
Clock 100Mhz Data 25Mhz	7.328e-03	7.115e-03	6.883e-03	7.167e-03
Clock 100Mhz Data 50Mhz	6.964e-03	6.835e-03	6.695e-03	7.427e-03
Clock = 0 Data 100Mhz	3.388e-03	3.569e-03	3.448e-03	3.385e-03
Clock = 1 Data 100Mhz	3.526e-05	4.903e-04	3.393e-04	2.638e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P4	C8T28SOIDV_LL_-SDFPRQNX29_P4		
Clock 100Mhz Data 0Mhz	6.863e-03	6.859e-03		
Clock 100Mhz Data 25Mhz	7.699e-03	8.551e-03		
Clock 100Mhz Data 50Mhz	8.536e-03	1.024e-02		
Clock = 0 Data 100Mhz	3.346e-03	3.320e-03		
Clock = 1 Data 100Mhz	2.186e-04	1.884e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P4	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P4	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P4	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P4	C8T28SOI_LLHF_-SDFPRQNTX3_P4	C8T28SOIDV_LL_-SDFPRQNTX5_P4	C8T28SOIDV_LL_-SDFPRQNTX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0009	0.0009
TE	0.0010	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P4	C8T28SOIDV_LL_-SDFPRQNTX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0007		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNTX5_P4	**C8T28SOI_LLHF_-SDFPRQNTX3_P4**	**C8T28SOI_LL_-SDFPRQNTX5_P4**	**C8T28SOI_LLHF_-SDFPRQNTX3_P4**
CP to QN ↓	0.0725	0.0755	2.8994	4.3580
CP to QN ↑	0.0756	0.0695	4.4550	6.1623
CP to TQ ↓	0.0648	0.0504	8.0541	5.1033
CP to TQ ↑	0.0614	0.0574	20.5122	11.0239
RN to QN ↑	0.0664	0.0642	4.4550	6.1943
RN to TQ ↓	0.0574	0.0504	7.8207	4.8948
	C8T28SOIDV_LL_-SDFPRQNTX5_P4	**C8T28SOIDV_LL_-SDFPRQNTX10_P4**	**C8T28SOIDV_LL_-SDFPRQNTX5_P4**	**C8T28SOIDV_LL_-SDFPRQNTX10_P4**
CP to QN ↓	0.0779	0.0824	2.7603	1.4330
CP to QN ↑	0.0620	0.0653	4.0086	2.0371
CP to TQ ↓	0.0434	0.0441	5.0762	5.1083
CP to TQ ↑	0.0588	0.0588	8.7555	8.7627
RN to QN ↑	0.0593	0.0630	4.0049	2.0341
RN to TQ ↓	0.0396	0.0405	5.0782	5.1167
	C8T28SOIDV_LL_-SDFPRQNTX19_P4	**C8T28SOIDV_LL_-SDFPRQNTX29_P4**	**C8T28SOIDV_LL_-SDFPRQNTX19_P4**	**C8T28SOIDV_LL_-SDFPRQNTX29_P4**
CP to QN ↓	0.0782	0.0799	0.7229	0.4936
CP to QN ↑	0.0669	0.0745	1.0316	0.7041
CP to TQ ↓	0.0474	0.0572	5.1529	5.8107
CP to TQ ↑	0.0626	0.0693	8.7841	9.9874
RN to QN ↑	0.0627	0.0709	1.0305	0.7034
RN to TQ ↓	0.0421	0.0528	5.1399	5.7215

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P4	C8T28SOI_-LLHF_-SDFPRQNTX3_-P4	C8T28SOIDV_-LL_-SDFPRQNTX5_-P4	C8T28SOIDV_-LL_SDF-PRQNTX10_P4
CP ↓	min_pulse_width to CP	0.0796	0.0762	0.0699	0.0699
CP ↑	min_pulse_width to CP	0.0467	0.0409	0.0393	0.0407
D ↓	hold_rising to CP	-0.0338	-0.0697	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0066	-0.0066	-0.0000	0.0004
D ↓	setup_rising to CP	0.0684	0.1094	0.0440	0.0440
D ↑	setup_rising to CP	0.0369	0.0363	0.0245	0.0245
RN ↓	min_pulse_width to RN	0.0566	0.0566	0.0540	0.0566
RN ↑	recovery_rising to CP	0.0054	0.0054	0.0032	0.0054
RN ↑	removal_rising to CP	0.0042	0.0043	0.0043	0.0043
TE ↓	hold_rising to CP	-0.0240	-0.0230	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0039	-0.0071	-0.0039	-0.0066
TE ↓	setup_rising to CP	0.0663	0.0878	0.0419	0.0419
TE ↑	setup_rising to CP	0.0813	0.1025	0.0786	0.0786
TI ↓	hold_rising to CP	-0.0482	-0.0710	-0.0391	-0.0391
TI ↑	hold_rising to CP	-0.0048	-0.0034	-0.0064	-0.0107
TI ↓	setup_rising to CP	0.0822	0.1012	0.0786	0.0786
TI ↑	setup_rising to CP	0.0355	0.0299	0.0355	0.0355
		C8T28SOIDV_-LL_SDF-PRQNTX19_P4	C8T28SOIDV_-LL_SDF-PRQNTX29_P4		
CP ↓	min_pulse_width to CP	0.0699	0.0699		
CP ↑	min_pulse_width to CP	0.0439	0.0499		
D ↓	hold_rising to CP	-0.0045	-0.0045		
D ↑	hold_rising to CP	-0.0000	-0.0000		
D ↓	setup_rising to CP	0.0440	0.0440		
D ↑	setup_rising to CP	0.0245	0.0245		
RN ↓	min_pulse_width to RN	0.0588	0.0708		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0043	0.0043		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0039	-0.0039		

TE ↓	setup_rising to CP	0.0419	0.0419		
TE ↑	setup_rising to CP	0.0786	0.0786		
TI ↓	hold_rising to CP	-0.0339	-0.0398		
TI ↑	hold_rising to CP	-0.0064	-0.0064		
TI ↓	setup_rising to CP	0.0786	0.0786		
TI ↑	setup_rising to CP	0.0355	0.0355		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P4	4.523e-06	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P4	4.312e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P4	4.652e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_P4	5.271e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_P4	7.147e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_P4	9.585e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

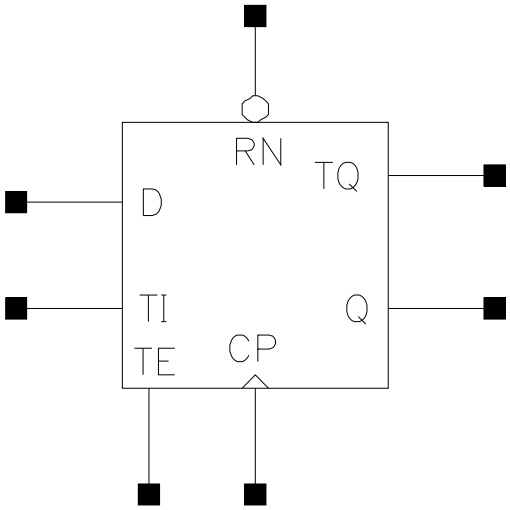
Pin Cycle	C8T28SOI_LL_SDFPRQNTX5_P4	C8T28SOI_LLHF_SDFPRQNTX3_P4	C8T28SOIDV_LL_SDFPRQNTX5_P4	C8T28SOIDV_LL_SDFPRQNTX10_P4
Clock 100Mhz Data 0Mhz	7.739e-03	7.437e-03	7.110e-03	6.938e-03
Clock 100Mhz Data 25Mhz	7.624e-03	7.355e-03	7.085e-03	7.205e-03
Clock 100Mhz Data 50Mhz	7.509e-03	7.274e-03	7.059e-03	7.473e-03
Clock = 0 Data 100Mhz	3.376e-03	3.568e-03	3.449e-03	3.387e-03
Clock = 1 Data 100Mhz	4.414e-05	4.981e-04	3.459e-04	2.697e-04
	C8T28SOIDV_LL_SDFPRQNTX19_P4	C8T28SOIDV_LL_SDFPRQNTX29_P4		
Clock 100Mhz Data 0Mhz	6.892e-03	6.853e-03		
Clock 100Mhz Data 25Mhz	7.724e-03	8.716e-03		
Clock 100Mhz Data 50Mhz	8.557e-03	1.058e-02		
Clock = 0 Data 100Mhz	3.349e-03	3.324e-03		
Clock = 1 Data 100Mhz	2.240e-04	1.936e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P4	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P4	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P4	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P4	C8T28SOI_LLHF_-SDFPRQTX3_P4	C8T28SOIDV_LL_-SDFPRQTX5_P4	C8T28SOIDV_LL_-SDFPRQTX10_P4
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0009	0.0008
TE	0.0010	0.0009	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P4	C8T28SOIDV_LL_-SDFPRQTX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0009	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQTX5_P4	**C8T28SOI_LLHF_-SDFPRQTX3_P4**	**C8T28SOI_LL_-SDFPRQTX5_P4**	**C8T28SOI_LLHF_-SDFPRQTX3_P4**
CP to Q ↓	0.0664	0.0579	3.2077	4.7542
CP to Q ↑	0.0538	0.0578	4.1467	6.4187
CP to TQ ↓	0.0791	0.0568	8.4906	5.2521
CP to TQ ↑	0.0680	0.0608	20.5674	11.1943
RN to Q ↓	0.0479	0.0534	3.0170	4.4507
RN to TQ ↓	0.0594	0.0532	8.2165	5.0056
	C8T28SOIDV_LL_-SDFPRQTX5_P4	**C8T28SOIDV_LL_-SDFPRQTX10_P4**	**C8T28SOIDV_LL_-SDFPRQTX5_P4**	**C8T28SOIDV_LL_-SDFPRQTX10_P4**
CP to Q ↓	0.0493	0.0651	2.9172	1.4155
CP to Q ↑	0.0602	0.0839	4.0988	2.0360
CP to TQ ↓	0.0498	0.0676	5.2198	5.0992
CP to TQ ↑	0.0622	0.0873	8.8931	8.8360
RN to Q ↓	0.0471	0.0674	2.8824	1.4132
RN to TQ ↓	0.0475	0.0698	5.1757	5.1011
	C8T28SOIDV_LL_-SDFPRQTX19_P4	**C8T28SOIDV_LL_-SDFPRQTX29_P4**	**C8T28SOIDV_LL_-SDFPRQTX19_P4**	**C8T28SOIDV_LL_-SDFPRQTX29_P4**
CP to Q ↓	0.0726	0.0699	0.7456	0.5004
CP to Q ↑	0.0894	0.0901	1.0382	0.7093
CP to TQ ↓	0.0761	0.0719	5.1534	5.0228
CP to TQ ↑	0.0943	0.0944	8.8328	9.0333
RN to Q ↓	0.0740	0.0717	0.7460	0.4998
RN to TQ ↓	0.0775	0.0738	5.1553	5.0213

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_P4	C8T28SOI_-LLHF_-SDFPRQTX3_P4	C8T28SOIDV_-LL_-SDFPRQTX5_P4	C8T28SOIDV_-LL_-SDFPRQTX10_-P4
CP ↓	min_pulse_width to CP	0.0796	0.0762	0.0699	0.0699
CP ↑	min_pulse_width to CP	0.0548	0.0456	0.0407	0.0360
D ↓	hold_rising to CP	-0.0338	-0.0697	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0066	-0.0066	0.0004	0.0004
D ↓	setup_rising to CP	0.0684	0.1094	0.0440	0.0440
D ↑	setup_rising to CP	0.0369	0.0363	0.0245	0.0245
RN ↓	min_pulse_width to RN	0.0610	0.0566	0.0540	0.0469
RN ↑	recovery_rising to CP	0.0054	0.0054	0.0032	0.0005
RN ↑	removal_rising to CP	0.0042	0.0043	0.0043	0.0043
TE ↓	hold_rising to CP	-0.0240	-0.0230	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0039	-0.0071	-0.0039	-0.0066
TE ↓	setup_rising to CP	0.0663	0.0878	0.0419	0.0419
TE ↑	setup_rising to CP	0.0813	0.1025	0.0786	0.0786
TI ↓	hold_rising to CP	-0.0482	-0.0710	-0.0391	-0.0391
TI ↑	hold_rising to CP	-0.0048	-0.0034	-0.0107	-0.0107
TI ↓	setup_rising to CP	0.0822	0.1055	0.0786	0.0786
TI ↑	setup_rising to CP	0.0355	0.0299	0.0355	0.0355
		C8T28SOIDV_-LL_-SDFPRQTX19_-P4	C8T28SOIDV_-LL_-SDFPRQTX29_-P4		
CP ↓	min_pulse_width to CP	0.0699	0.0699		
CP ↑	min_pulse_width to CP	0.0359	0.0359		
D ↓	hold_rising to CP	-0.0045	-0.0045		
D ↑	hold_rising to CP	0.0004	0.0004		
D ↓	setup_rising to CP	0.0440	0.0440		
D ↑	setup_rising to CP	0.0245	0.0245		
RN ↓	min_pulse_width to RN	0.0469	0.0469		
RN ↑	recovery_rising to CP	0.0032	0.0037		
RN ↑	removal_rising to CP	0.0043	0.0043		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	-0.0066	-0.0066		

TE ↓	setup_rising to CP	0.0419	0.0419		
TE ↑	setup_rising to CP	0.0786	0.0786		
TI ↓	hold_rising to CP	-0.0391	-0.0391		
TI ↑	hold_rising to CP	-0.0107	-0.0107		
TI ↓	setup_rising to CP	0.0786	0.0786		
TI ↑	setup_rising to CP	0.0355	0.0355		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P4	4.792e-06	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P4	4.348e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P4	4.823e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P4	6.366e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P4	8.044e-06	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P4	1.047e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

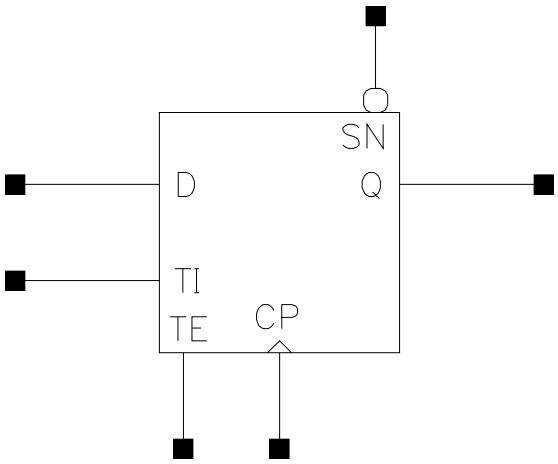
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P4	C8T28SOI_LLHF_-SDFPRQTX3_P4	C8T28SOIDV_LL_-SDFPRQTX5_P4	C8T28SOIDV_LL_-SDFPRQTX10_P4
Clock 100Mhz Data 0Mhz	7.756e-03	7.448e-03	7.115e-03	6.949e-03
Clock 100Mhz Data 25Mhz	7.678e-03	7.347e-03	7.040e-03	7.414e-03
Clock 100Mhz Data 50Mhz	7.600e-03	7.247e-03	6.965e-03	7.878e-03
Clock = 0 Data 100Mhz	3.379e-03	3.570e-03	3.447e-03	3.385e-03
Clock = 1 Data 100Mhz	3.524e-05	4.938e-04	3.416e-04	2.656e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P4	C8T28SOIDV_LL_-SDFPRQTX29_P4		
Clock 100Mhz Data 0Mhz	6.850e-03	6.783e-03		
Clock 100Mhz Data 25Mhz	7.890e-03	8.465e-03		
Clock 100Mhz Data 50Mhz	8.931e-03	1.015e-02		
Clock = 0 Data 100Mhz	3.348e-03	3.325e-03		
Clock = 1 Data 100Mhz	2.200e-04	1.897e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P4	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P4	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P4	C8T28SOI_LLHF_-SDFPSQX3_P4	C8T28SOIDV_LL_-SDFPSQX5_P4	C8T28SOIDV_LL_-SDFPSQX10_P4
CP	0.0007	0.0007	0.0005	0.0006
D	0.0003	0.0004	0.0003	0.0003
SN	0.0013	0.0013	0.0010	0.0010
TE	0.0010	0.0009	0.0009	0.0010
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQX14_P4	C8T28SOIDV_LL_-SDFPSQX19_P4	C8T28SOIDV_LL_-SDFPSQX29_P4	
CP	0.0006	0.0006	0.0006	
D	0.0003	0.0003	0.0003	
SN	0.0010	0.0010	0.0010	
TE	0.0010	0.0010	0.0010	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P4	**C8T28SOI_LLHF_-SDFPSQX3_P4**	**C8T28SOI_LL_-SDFPSQX5_P4**	**C8T28SOI_LLHF_-SDFPSQX3_P4**
CP to Q ↓	0.0593	0.0528	3.0676	4.6643
CP to Q ↑	0.0514	0.0565	4.1420	6.2550
SN to Q ↑	0.0428	0.0391	4.0896	6.1850
	C8T28SOIDV_LL_-SDFPSQX5_P4	**C8T28SOIDV_LL_-SDFPSQX10_P4**	**C8T28SOIDV_LL_-SDFPSQX5_P4**	**C8T28SOIDV_LL_-SDFPSQX10_P4**
CP to Q ↓	0.0448	0.0646	2.8151	1.3594
CP to Q ↑	0.0555	0.0884	4.0602	2.0316
SN to Q ↑	0.0390	0.0699	4.0445	2.0301
	C8T28SOIDV_LL_-SDFPSQX14_P4	**C8T28SOIDV_LL_-SDFPSQX19_P4**	**C8T28SOIDV_LL_-SDFPSQX14_P4**	**C8T28SOIDV_LL_-SDFPSQX19_P4**
CP to Q ↓	0.0649	0.0689	0.9350	0.7214
CP to Q ↑	0.0883	0.0915	1.3664	1.0309
SN to Q ↑	0.0695	0.0726	1.3665	1.0301
	C8T28SOIDV_LL_-SDFPSQX29_P4		**C8T28SOIDV_LL_-SDFPSQX29_P4**	
CP to Q ↓	0.0686		0.4899	
CP to Q ↑	0.0954		0.6846	
SN to Q ↑	0.0766		0.6842	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P4	C8T28SOI_-LLHF_-SDFPSQX3_P4	C8T28SOIDV_-LL_SDFPSQX5_-P4	C8T28SOIDV_-LL_-SDFPSQX10_P4
CP ↓	min_pulse_width to CP	0.0868	0.0857	0.0729	0.0754
CP ↑	min_pulse_width to CP	0.0501	0.0409	0.0393	0.0360
D ↓	hold_rising to CP	-0.0387	-0.0799	-0.0126	-0.0175
D ↑	hold_rising to CP	-0.0071	-0.0045	0.0004	0.0004
D ↓	setup_rising to CP	0.0733	0.1245	0.0538	0.0564
D ↑	setup_rising to CP	0.0314	0.0343	0.0271	0.0271

SN ↓	min_pulse_width to SN	0.0425	0.0354	0.0354	0.0376
SN ↑	recovery_rising to CP	0.0031	0.0053	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0212	0.0261	0.0286	0.0309
TE ↓	hold_rising to CP	-0.0181	-0.0235	-0.0072	-0.0121
TE ↑	hold_rising to CP	-0.0049	-0.0013	-0.0000	-0.0049
TE ↓	setup_rising to CP	0.0711	0.0976	0.0516	0.0512
TE ↑	setup_rising to CP	0.0884	0.1155	0.0786	0.0786
TI ↓	hold_rising to CP	-0.0524	-0.0756	-0.0391	-0.0385
TI ↑	hold_rising to CP	-0.0058	-0.0044	0.0006	-0.0058
TI ↓	setup_rising to CP	0.0868	0.1153	0.0786	0.0773
TI ↑	setup_rising to CP	0.0297	0.0291	0.0242	0.0306
		C8T28SOIDV_-LL_-SDFPSQX14_P4	C8T28SOIDV_-LL_-SDFPSQX19_P4	C8T28SOIDV_-LL_-SDFPSQX29_P4	
CP ↓	min_pulse_width to CP	0.0747	0.0747	0.0754	
CP ↑	min_pulse_width to CP	0.0360	0.0360	0.0360	
D ↓	hold_rising to CP	-0.0175	-0.0175	-0.0175	
D ↑	hold_rising to CP	0.0004	0.0004	0.0004	
D ↓	setup_rising to CP	0.0564	0.0564	0.0564	
D ↑	setup_rising to CP	0.0271	0.0271	0.0271	
SN ↓	min_pulse_width to SN	0.0354	0.0354	0.0403	
SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	
SN ↑	removal_rising to CP	0.0309	0.0309	0.0309	
TE ↓	hold_rising to CP	-0.0121	-0.0121	-0.0121	
TE ↑	hold_rising to CP	-0.0049	-0.0049	-0.0049	
TE ↓	setup_rising to CP	0.0517	0.0517	0.0517	
TE ↑	setup_rising to CP	0.0786	0.0786	0.0786	
TI ↓	hold_rising to CP	-0.0385	-0.0385	-0.0385	
TI ↑	hold_rising to CP	-0.0058	-0.0058	-0.0058	
TI ↓	setup_rising to CP	0.0773	0.0773	0.0773	
TI ↑	setup_rising to CP	0.0306	0.0306	0.0306	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQX5_P4	4.742e-06	1.000e-20

C8T28SOI_LLHF_SDFPSQX3_P4	4.257e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P4	4.508e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P4	6.215e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P4	7.136e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P4	8.166e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P4	1.019e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

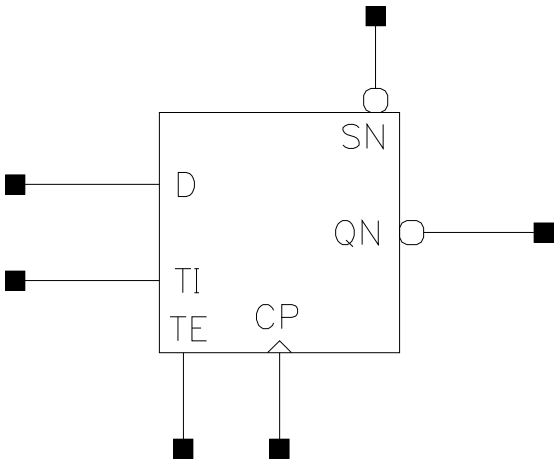
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P4	C8T28SOI_LLHF_-SDFPSQX3_P4	C8T28SOIDV_LL_-SDFPSQX5_P4	C8T28SOIDV_LL_-SDFPSQX10_P4
Clock 100Mhz Data 0Mhz	7.639e-03	7.262e-03	6.960e-03	6.811e-03
Clock 100Mhz Data 25Mhz	7.461e-03	7.074e-03	6.727e-03	7.187e-03
Clock 100Mhz Data 50Mhz	7.284e-03	6.886e-03	6.493e-03	7.562e-03
Clock = 0 Data 100Mhz	3.493e-03	3.671e-03	3.572e-03	3.547e-03
Clock = 1 Data 100Mhz	3.524e-05	4.883e-04	3.381e-04	2.635e-04
	C8T28SOIDV_LL_-SDFPSQX14_P4	C8T28SOIDV_LL_-SDFPSQX19_P4	C8T28SOIDV_LL_-SDFPSQX29_P4	
Clock 100Mhz Data 0Mhz	6.722e-03	6.662e-03	6.620e-03	
Clock 100Mhz Data 25Mhz	7.332e-03	7.683e-03	8.159e-03	
Clock 100Mhz Data 50Mhz	7.942e-03	8.704e-03	9.697e-03	
Clock = 0 Data 100Mhz	3.532e-03	3.522e-03	3.515e-03	
Clock = 1 Data 100Mhz	2.188e-04	1.890e-04	1.677e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P4	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P4	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P4	C8T28SOI_LLHF_-SDFPSQNX3_P4	C8T28SOIDV_LL_-SDFPSQNX5_P4	C8T28SOIDV_LL_-SDFPSQNX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0013	0.0013	0.0010	0.0010
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNX14_P4	C8T28SOIDV_LL_-SDFPSQNX19_P4	C8T28SOIDV_LL_-SDFPSQNX23_P4	C8T28SOIDV_LL_-SDFPSQNX29_P4
CP	0.0005	0.0005	0.0005	0.0005
D	0.0003	0.0003	0.0003	0.0003
SN	0.0010	0.0010	0.0010	0.0010
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNX5_P4	**C8T28SOI_LLHF_-SDFPSQNX3_P4**	**C8T28SOI_LL_-SDFPSQNX5_P4**	**C8T28SOI_LLHF_-SDFPSQNX3_P4**
CP to QN ↓	0.0689	0.0697	3.0220	4.2924
CP to QN ↑	0.0648	0.0597	4.3110	6.1442
SN to QN ↓	0.0611	0.0528	3.0264	4.2868
	C8T28SOIDV_LL_-SDFPSQNX5_P4	**C8T28SOIDV_LL_-SDFPSQNX10_P4**	**C8T28SOIDV_LL_-SDFPSQNX5_P4**	**C8T28SOIDV_LL_-SDFPSQNX10_P4**
CP to QN ↓	0.0738	0.0692	2.7068	1.3758
CP to QN ↑	0.0594	0.0604	4.0224	2.0132
SN to QN ↓	0.0567	0.0507	2.7076	1.3752
	C8T28SOIDV_LL_-SDFPSQNX14_P4	**C8T28SOIDV_LL_-SDFPSQNX19_P4**	**C8T28SOIDV_LL_-SDFPSQNX14_P4**	**C8T28SOIDV_LL_-SDFPSQNX19_P4**
CP to QN ↓	0.0716	0.0736	0.9213	0.7054
CP to QN ↑	0.0619	0.0641	1.3531	1.0182
SN to QN ↓	0.0519	0.0544	0.9219	0.7043
	C8T28SOIDV_LL_-SDFPSQNX23_P4	**C8T28SOIDV_LL_-SDFPSQNX29_P4**	**C8T28SOIDV_LL_-SDFPSQNX23_P4**	**C8T28SOIDV_LL_-SDFPSQNX29_P4**
CP to QN ↓	0.0747	0.0718	0.5588	0.4841
CP to QN ↑	0.0641	0.0651	1.0143	0.6837
SN to QN ↓	0.0561	0.0558	0.5582	0.4837

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P4	C8T28SOI_-LLHF_-SDFPSQNX3_-P4	C8T28SOIDV_-LL_-SDFPSQNX5_-P4	C8T28SOIDV_-LL_-SDFPSQNX10_-P4
CP ↓	min_pulse_width to CP	0.0868	0.0857	0.0729	0.0770
CP ↑	min_pulse_width to CP	0.0407	0.0362	0.0393	0.0407
D ↓	hold_rising to CP	-0.0387	-0.0799	-0.0126	-0.0094
D ↑	hold_rising to CP	-0.0071	-0.0045	0.0004	0.0004
D ↓	setup_rising to CP	0.0733	0.1213	0.0538	0.0538

D ↑	setup_rising to CP	0.0314	0.0343	0.0271	0.0271
SN ↓	min_pulse_width to SN	0.0403	0.0354	0.0354	0.0354
SN ↑	recovery_rising to CP	0.0031	0.0053	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0212	0.0261	0.0286	0.0309
TE ↓	hold_rising to CP	-0.0181	-0.0235	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0049	-0.0013	-0.0000	-0.0000
TE ↓	setup_rising to CP	0.0711	0.0976	0.0516	0.0516
TE ↑	setup_rising to CP	0.0884	0.1155	0.0845	0.0818
TI ↓	hold_rising to CP	-0.0531	-0.0756	-0.0391	-0.0391
TI ↑	hold_rising to CP	-0.0058	-0.0044	0.0006	0.0006
TI ↓	setup_rising to CP	0.0868	0.1153	0.0786	0.0786
TI ↑	setup_rising to CP	0.0297	0.0291	0.0242	0.0242
		C8T28SOIDV_-LL_-SDFPSQNX14_-P4	C8T28SOIDV_-LL_-SDFPSQNX19_-P4	C8T28SOIDV_-LL_-SDFPSQNX23_-P4	C8T28SOIDV_-LL_-SDFPSQNX29_-P4
CP ↓	min_pulse_width to CP	0.0770	0.0770	0.0770	0.0729
CP ↑	min_pulse_width to CP	0.0407	0.0407	0.0407	0.0439
D ↓	hold_rising to CP	-0.0094	-0.0094	-0.0094	-0.0126
D ↑	hold_rising to CP	0.0004	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0538	0.0538	0.0538	0.0538
D ↑	setup_rising to CP	0.0271	0.0271	0.0271	0.0271
SN ↓	min_pulse_width to SN	0.0354	0.0354	0.0403	0.0403
SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0309	0.0309	0.0309	0.0286
TE ↓	hold_rising to CP	-0.0072	-0.0072	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0000	-0.0000	-0.0000	-0.0000
TE ↓	setup_rising to CP	0.0516	0.0516	0.0516	0.0516
TE ↑	setup_rising to CP	0.0786	0.0786	0.0786	0.0845
TI ↓	hold_rising to CP	-0.0391	-0.0375	-0.0391	-0.0391
TI ↑	hold_rising to CP	0.0006	0.0006	0.0006	0.0006
TI ↓	setup_rising to CP	0.0786	0.0786	0.0786	0.0786
TI ↑	setup_rising to CP	0.0244	0.0242	0.0242	0.0242

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P4	4.876e-06	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P4	4.307e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P4	4.728e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P4	6.661e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P4	7.411e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P4	8.479e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P4	8.926e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P4	1.124e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

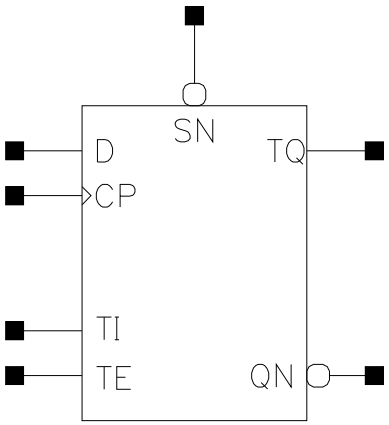
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P4	C8T28SOI_LLHF_-SDFPSQNX3_P4	C8T28SOIDV_LL_-SDFPSQNX5_P4	C8T28SOIDV_LL_-SDFPSQNX10_P4
Clock 100Mhz Data 0Mhz	7.578e-03	7.229e-03	6.927e-03	6.844e-03
Clock 100Mhz Data 25Mhz	7.345e-03	7.020e-03	6.820e-03	7.254e-03
Clock 100Mhz Data 50Mhz	7.111e-03	6.810e-03	6.713e-03	7.665e-03
Clock = 0 Data 100Mhz	3.492e-03	3.671e-03	3.573e-03	3.523e-03
Clock = 1 Data 100Mhz	3.516e-05	4.882e-04	3.380e-04	2.629e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P4	C8T28SOIDV_LL_-SDFPSQNX19_P4	C8T28SOIDV_LL_-SDFPSQNX23_P4	C8T28SOIDV_LL_-SDFPSQNX29_P4
Clock 100Mhz Data 0Mhz	6.793e-03	6.760e-03	6.737e-03	6.689e-03
Clock 100Mhz Data 25Mhz	7.434e-03	7.654e-03	7.754e-03	8.233e-03
Clock 100Mhz Data 50Mhz	8.076e-03	8.549e-03	8.772e-03	9.778e-03
Clock = 0 Data 100Mhz	3.492e-03	3.472e-03	3.458e-03	3.449e-03
Clock = 1 Data 100Mhz	2.179e-04	1.879e-04	1.665e-04	1.505e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P4	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P4	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P4	C8T28SOI_LLHF_-SDFPSQNTX3_P4	C8T28SOIDV_LL_-SDFPSQNTX5_P4	C8T28SOIDV_LL_-SDFPSQNTX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0013	0.0013	0.0010	0.0010
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNTX19_P4	C8T28SOIDV_LL_-SDFPSQNTX23_P4	C8T28SOIDV_LL_-SDFPSQNTX29_P4	
CP	0.0005	0.0005	0.0005	
D	0.0003	0.0003	0.0003	
SN	0.0010	0.0010	0.0010	
TE	0.0009	0.0009	0.0009	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P4	**C8T28SOI_LLHF_-SDFPSQNTX3_P4**	**C8T28SOI_LL_-SDFPSQNTX5_P4**	**C8T28SOI_LLHF_-SDFPSQNTX3_P4**
CP to QN ↓	0.0749	0.0747	3.0739	4.3407
CP to QN ↑	0.0752	0.0705	4.2531	6.1810
CP to TQ ↓	0.0633	0.0510	7.9593	5.1443
CP to TQ ↑	0.0628	0.0585	20.5189	11.0254
SN to QN ↓	0.0651	0.0564	3.0725	4.3348
SN to TQ ↑	0.0533	0.0409	20.4745	10.9824
	C8T28SOIDV_LL_-SDFPSQNTX5_P4	**C8T28SOIDV_LL_-SDFPSQNTX10_P4**	**C8T28SOIDV_LL_-SDFPSQNTX5_P4**	**C8T28SOIDV_LL_-SDFPSQNTX10_P4**
CP to QN ↓	0.0740	0.0697	2.7687	1.3670
CP to QN ↑	0.0612	0.0645	4.0292	2.0250
CP to TQ ↓	0.0438	0.0504	5.1285	5.1919
CP to TQ ↑	0.0565	0.0592	9.4694	9.5337
SN to QN ↓	0.0561	0.0531	2.7705	1.3682
SN to TQ ↑	0.0386	0.0426	9.4564	9.4916
	C8T28SOIDV_LL_-SDFPSQNTX19_P4	**C8T28SOIDV_LL_-SDFPSQNTX23_P4**	**C8T28SOIDV_LL_-SDFPSQNTX19_P4**	**C8T28SOIDV_LL_-SDFPSQNTX23_P4**
CP to QN ↓	0.0740	0.0758	0.7000	0.5576
CP to QN ↑	0.0688	0.0680	1.0238	1.0164
CP to TQ ↓	0.0502	0.0510	5.1846	5.2235
CP to TQ ↑	0.0592	0.0598	9.5358	9.5443
SN to QN ↓	0.0571	0.0590	0.6996	0.5572
SN to TQ ↑	0.0425	0.0432	9.4948	9.5045
	C8T28SOIDV_LL_-SDFPSQNTX29_P4		**C8T28SOIDV_LL_-SDFPSQNTX29_P4**	
CP to QN ↓	0.0753		0.4853	
CP to QN ↑	0.0701		0.6836	

CP to TQ ↓	0.0534		5.3187	
CP to TQ ↑	0.0635		10.9666	
SN to QN ↓	0.0584		0.4852	
SN to TQ ↑	0.0467		10.9110	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P4	C8T28SOI_-LLHF_-SDFPSQNTX3_-P4	C8T28SOIDV_-LL_-SDFPSQNTX5_-P4	C8T28SOIDV_-LL_SDFP-SQNTX10_P4
CP ↓	min_pulse_width to CP	0.0874	0.0857	0.0729	0.0729
CP ↑	min_pulse_width to CP	0.0467	0.0422	0.0392	0.0439
D ↓	hold_rising to CP	-0.0387	-0.0799	-0.0126	-0.0126
D ↑	hold_rising to CP	-0.0071	-0.0045	0.0004	0.0004
D ↓	setup_rising to CP	0.0759	0.1245	0.0538	0.0538
D ↑	setup_rising to CP	0.0314	0.0343	0.0271	0.0271
SN ↓	min_pulse_width to SN	0.0425	0.0376	0.0354	0.0381
SN ↑	recovery_rising to CP	0.0053	0.0053	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0216	0.0261	0.0286	0.0286
TE ↓	hold_rising to CP	-0.0181	-0.0235	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0049	-0.0013	-0.0000	-0.0000
TE ↓	setup_rising to CP	0.0733	0.0976	0.0516	0.0516
TE ↑	setup_rising to CP	0.0884	0.1155	0.0786	0.0845
TI ↓	hold_rising to CP	-0.0524	-0.0756	-0.0391	-0.0391
TI ↑	hold_rising to CP	-0.0058	-0.0044	0.0006	0.0006
TI ↓	setup_rising to CP	0.0884	0.1153	0.0786	0.0786
TI ↑	setup_rising to CP	0.0297	0.0291	0.0242	0.0242
		C8T28SOIDV_-LL_SDFP-SQNTX19_P4	C8T28SOIDV_-LL_SDFP-SQNTX23_P4	C8T28SOIDV_-LL_SDFP-SQNTX29_P4	
CP ↓	min_pulse_width to CP	0.0729	0.0729	0.0729	
CP ↑	min_pulse_width to CP	0.0452	0.0452	0.0452	
D ↓	hold_rising to CP	-0.0126	-0.0126	-0.0126	
D ↑	hold_rising to CP	0.0004	0.0004	0.0004	
D ↓	setup_rising to CP	0.0538	0.0538	0.0538	
D ↑	setup_rising to CP	0.0271	0.0271	0.0271	
SN ↓	min_pulse_width to SN	0.0403	0.0403	0.0430	

SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	
SN ↑	removal_rising to CP	0.0286	0.0286	0.0286	
TE ↓	hold_rising to CP	-0.0072	-0.0072	-0.0072	
TE ↑	hold_rising to CP	-0.0000	-0.0000	-0.0000	
TE ↓	setup_rising to CP	0.0516	0.0516	0.0516	
TE ↑	setup_rising to CP	0.0845	0.0845	0.0845	
TI ↓	hold_rising to CP	-0.0391	-0.0391	-0.0391	
TI ↑	hold_rising to CP	0.0006	0.0006	0.0006	
TI ↓	setup_rising to CP	0.0786	0.0786	0.0786	
TI ↑	setup_rising to CP	0.0242	0.0242	0.0242	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P4	4.807e-06	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P4	4.576e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P4	5.069e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_P4	6.940e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_P4	8.806e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_P4	9.297e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_P4	1.150e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

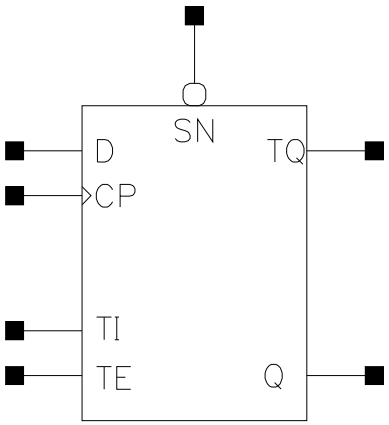
Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P4	C8T28SOI_LLHF_-SDFPSQNTX3_P4	C8T28SOIDV_LL_-SDFPSQNTX5_P4	C8T28SOIDV_LL_-SDFPSQNTX10_P4
Clock 100Mhz Data 0Mhz	7.389e-03	7.135e-03	6.878e-03	6.750e-03
Clock 100Mhz Data 25Mhz	7.431e-03	7.167e-03	6.881e-03	7.321e-03
Clock 100Mhz Data 50Mhz	7.472e-03	7.199e-03	6.884e-03	7.892e-03
Clock = 0 Data 100Mhz	3.486e-03	3.669e-03	3.571e-03	3.522e-03
Clock = 1 Data 100Mhz	3.630e-05	4.876e-04	3.379e-04	2.632e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P4	C8T28SOIDV_LL_-SDFPSQNTX23_P4	C8T28SOIDV_LL_-SDFPSQNTX29_P4	
Clock 100Mhz Data 0Mhz	6.673e-03	6.622e-03	6.586e-03	
Clock 100Mhz Data 25Mhz	7.739e-03	7.843e-03	8.349e-03	
Clock 100Mhz Data 50Mhz	8.805e-03	9.064e-03	1.011e-02	
Clock = 0 Data 100Mhz	3.492e-03	3.473e-03	3.461e-03	
Clock = 1 Data 100Mhz	2.184e-04	1.885e-04	1.672e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P4	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P4	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P4	C8T28SOI_LLHF_-SDFPSQTX3_P4	C8T28SOIDV_LL_-SDFPSQTX5_P4	C8T28SOIDV_LL_-SDFPSQTX10_P4
CP	0.0007	0.0007	0.0005	0.0006
D	0.0003	0.0004	0.0003	0.0003
SN	0.0014	0.0013	0.0010	0.0010
TE	0.0010	0.0009	0.0009	0.0010
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQTX19_P4	C8T28SOIDV_LL_-SDFPSQTX29_P4		
CP	0.0006	0.0006		
D	0.0003	0.0003		
SN	0.0010	0.0010		
TE	0.0010	0.0010		
TI	0.0004	0.0004		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQTX5_P4	**C8T28SOI_LLHF_-SDFPSQTX3_P4**	**C8T28SOI_LL_-SDFPSQTX5_P4**	**C8T28SOI_LLHF_-SDFPSQTX3_P4**
CP to Q ↓	0.0639	0.0585	3.2372	4.8170
CP to Q ↑	0.0542	0.0588	4.1471	6.4170
CP to TQ ↓	0.0767	0.0573	8.4234	5.2986
CP to TQ ↑	0.0687	0.0617	20.5392	11.2001
SN to Q ↑	0.0447	0.0409	4.0853	6.3425
SN to TQ ↑	0.0574	0.0434	20.4726	11.1397
	C8T28SOIDV_LL_-SDFPSQTX5_P4	**C8T28SOIDV_LL_-SDFPSQTX10_P4**	**C8T28SOIDV_LL_-SDFPSQTX5_P4**	**C8T28SOIDV_LL_-SDFPSQTX10_P4**
CP to Q ↓	0.0500	0.0638	2.9061	1.4010
CP to Q ↑	0.0579	0.0874	4.1173	2.0532
CP to TQ ↓	0.0507	0.0657	5.2133	5.2599
CP to TQ ↑	0.0594	0.0908	9.5941	9.4218
SN to Q ↑	0.0411	0.0686	4.1053	2.0513
SN to TQ ↑	0.0426	0.0720	9.5534	9.4272
	C8T28SOIDV_LL_-SDFPSQTX19_P4	**C8T28SOIDV_LL_-SDFPSQTX29_P4**	**C8T28SOIDV_LL_-SDFPSQTX19_P4**	**C8T28SOIDV_LL_-SDFPSQTX29_P4**
CP to Q ↓	0.0688	0.0776	0.7269	0.4780
CP to Q ↑	0.0918	0.0998	1.0549	0.6982
CP to TQ ↓	0.0693	0.0445	4.5392	4.6982
CP to TQ ↑	0.0957	0.0622	10.9190	10.9972
SN to Q ↑	0.0730	0.0808	1.0538	0.6984
SN to TQ ↑	0.0769	0.0436	10.9146	10.9830

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_P4	C8T28SOI_-LLHF_-SDFPSQTX3_P4	C8T28SOIDV_-LL_-SDFPSQTX5_P4	C8T28SOIDV_-LL_-SDFPSQTX10_-P4
CP ↓	min_pulse_width to CP	0.0874	0.0857	0.0729	0.0754
CP ↑	min_pulse_width to CP	0.0548	0.0456	0.0406	0.0360
D ↓	hold_rising to CP	-0.0387	-0.0799	-0.0126	-0.0175
D ↑	hold_rising to CP	-0.0071	-0.0045	0.0004	0.0004
D ↓	setup_rising to CP	0.0759	0.1245	0.0538	0.0564
D ↑	setup_rising to CP	0.0314	0.0343	0.0271	0.0266
SN ↓	min_pulse_width to SN	0.0452	0.0376	0.0381	0.0354
SN ↑	recovery_rising to CP	0.0053	0.0053	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0216	0.0261	0.0281	0.0309
TE ↓	hold_rising to CP	-0.0181	-0.0235	-0.0072	-0.0121
TE ↑	hold_rising to CP	-0.0049	-0.0013	-0.0000	-0.0049
TE ↓	setup_rising to CP	0.0733	0.0976	0.0516	0.0544
TE ↑	setup_rising to CP	0.0884	0.1155	0.0845	0.0786
TI ↓	hold_rising to CP	-0.0524	-0.0756	-0.0391	-0.0377
TI ↑	hold_rising to CP	-0.0058	-0.0044	0.0006	-0.0058
TI ↓	setup_rising to CP	0.0884	0.1153	0.0786	0.0771
TI ↑	setup_rising to CP	0.0297	0.0291	0.0242	0.0306
		C8T28SOIDV_-LL_-SDFPSQTX19_-P4	C8T28SOIDV_-LL_-SDFPSQTX29_-P4		
CP ↓	min_pulse_width to CP	0.0754	0.0754		
CP ↑	min_pulse_width to CP	0.0360	0.0407		
D ↓	hold_rising to CP	-0.0175	-0.0175		
D ↑	hold_rising to CP	0.0004	0.0004		
D ↓	setup_rising to CP	0.0564	0.0564		
D ↑	setup_rising to CP	0.0271	0.0271		
SN ↓	min_pulse_width to SN	0.0354	0.0430		
SN ↑	recovery_rising to CP	-0.0017	-0.0017		
SN ↑	removal_rising to CP	0.0309	0.0309		
TE ↓	hold_rising to CP	-0.0121	-0.0121		
TE ↑	hold_rising to CP	-0.0049	-0.0049		

TE ↓	setup_rising to CP	0.0517	0.0512		
TE ↑	setup_rising to CP	0.0786	0.0786		
TI ↓	hold_rising to CP	-0.0385	-0.0385		
TI ↑	hold_rising to CP	-0.0058	-0.0058		
TI ↓	setup_rising to CP	0.0773	0.0771		
TI ↑	setup_rising to CP	0.0306	0.0306		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P4	4.718e-06	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P4	4.520e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P4	4.870e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P4	6.549e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P4	8.022e-06	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P4	1.075e-05	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

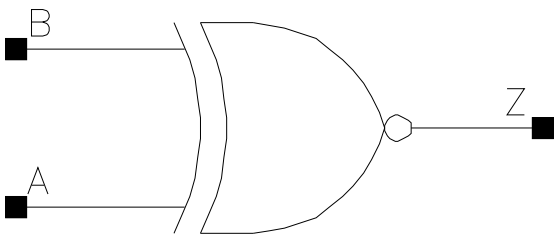
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P4	C8T28SOI_LLHF_-SDFPSQTX3_P4	C8T28SOIDV_LL_-SDFPSQTX5_P4	C8T28SOIDV_LL_-SDFPSQTX10_P4
Clock 100Mhz Data 0Mhz	7.398e-03	7.142e-03	6.884e-03	6.755e-03
Clock 100Mhz Data 25Mhz	7.452e-03	7.172e-03	6.881e-03	7.263e-03
Clock 100Mhz Data 50Mhz	7.506e-03	7.201e-03	6.878e-03	7.770e-03
Clock = 0 Data 100Mhz	3.486e-03	3.668e-03	3.570e-03	3.556e-03
Clock = 1 Data 100Mhz	3.626e-05	4.883e-04	3.384e-04	2.640e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P4	C8T28SOIDV_LL_-SDFPSQTX29_P4		
Clock 100Mhz Data 0Mhz	6.677e-03	6.627e-03		
Clock 100Mhz Data 25Mhz	7.752e-03	8.388e-03		
Clock 100Mhz Data 50Mhz	8.827e-03	1.015e-02		
Clock = 0 Data 100Mhz	3.539e-03	3.528e-03		
Clock = 1 Data 100Mhz	2.194e-04	1.897e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.600	0.544	0.8704
X5_P4	0.800	1.496	1.1968
X8_P4	1.600	1.088	1.7408
X9_P4	0.800	1.632	1.3056
X11_P4	1.600	1.360	2.1760
X14_P4	0.800	2.312	1.8496
X15_P4	1.600	1.904	3.0464
X19_P4	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P4	X5_P4	X8_P4	X9_P4
A	0.0010	0.0005	0.0016	0.0006
B	0.0009	0.0009	0.0013	0.0012
	X11_P4	X14_P4	X15_P4	X19_P4
A	0.0023	0.0009	0.0028	0.0011
B	0.0021	0.0015	0.0025	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X5_P4	X4_P4	X5_P4
A to Z ↓	0.0159	0.0441	3.8705	2.9254
A to Z ↑	0.0177	0.0398	5.9050	4.3690
B to Z ↓	0.0149	0.0333	3.8701	2.9113
B to Z ↑	0.0186	0.0304	5.9144	4.3663

	X8_P4	X9_P4	X8_P4	X9_P4
A to Z ↓	0.0189	0.0412	2.0539	1.5069
A to Z ↑	0.0215	0.0378	3.1588	2.2298
B to Z ↓	0.0180	0.0318	2.0547	1.5034
B to Z ↑	0.0216	0.0296	3.1665	2.2309
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0178	0.0389	1.4421	1.0270
A to Z ↑	0.0198	0.0352	2.0562	1.4394
B to Z ↓	0.0163	0.0297	1.4418	1.0235
B to Z ↑	0.0196	0.0278	2.0627	1.4387
	X15_P4	**X19_P4**	**X15_P4**	**X19_P4**
A to Z ↓	0.0196	0.0361	1.0949	0.7648
A to Z ↑	0.0219	0.0336	1.5688	1.0721
B to Z ↓	0.0180	0.0284	1.0947	0.7627
B to Z ↑	0.0217	0.0270	1.5734	1.0698

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P4	2.689e-06	1.000e-20
X5_P4	2.537e-06	1.000e-20
X8_P4	4.195e-06	1.000e-20
X9_P4	4.436e-06	1.000e-20
X11_P4	6.377e-06	1.000e-20
X14_P4	6.658e-06	1.000e-20
X15_P4	8.002e-06	1.000e-20
X19_P4	9.718e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P4	X5_P4	X8_P4	X9_P4
A to Z	1.632e-03	3.451e-03	3.196e-03	4.817e-03
B to Z	1.605e-03	2.757e-03	3.071e-03	3.870e-03
	X11_P4	X14_P4	X15_P4	X19_P4
A to Z	4.579e-03	7.589e-03	6.182e-03	9.184e-03
B to Z	4.395e-03	5.965e-03	5.921e-03	7.387e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

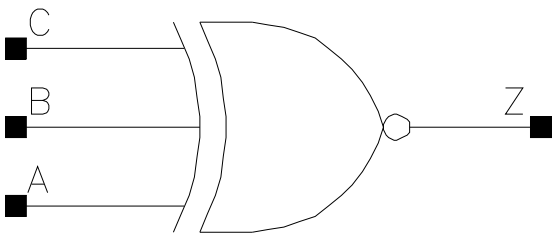
Pin Cycle (vdds)	X4_P4	X5_P4	X8_P4	X9_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P4	X14_P4	X15_P4	X19_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P4	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P4	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P4	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P4	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P4	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P4	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P4	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P4	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P4	C8T28SOIDV_LL_-XNOR3X4_P4	C8T28SOIDV_LL_-XNOR3X9_P4	C8T28SOIDV_LL_-XNOR3X13_P4
A	0.0015	0.0015	0.0019	0.0025
B	0.0015	0.0014	0.0018	0.0024
C	0.0007	0.0006	0.0006	0.0006
	C8T28SOIDV_LLS_-XNOR3X1_P4	C8T28SOIDV_LLS_-XNOR3X2_P4	C8T28SOIDV_LLS_-XNOR3X5_P4	C8T28SOIDV_LLS_-XNOR3X7_P4

A	0.0014	0.0016	0.0036	0.0054
B	0.0015	0.0017	0.0033	0.0050
C	0.0010	0.0012	0.0024	0.0034

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XNOR3X2_P4	**C8T28SOIDV_LL_-XNOR3X4_P4**	**C8T28SOIDV_LL_-XNOR3X2_P4**	**C8T28SOIDV_LL_-XNOR3X4_P4**
A to Z ↓	0.0447	0.0472	5.8515	3.1591
A to Z ↑	0.0425	0.0432	8.0735	4.4234
B to Z ↓	0.0453	0.0479	5.8510	3.1605
B to Z ↑	0.0431	0.0439	8.0773	4.4242
C to Z ↓	0.0599	0.0634	5.8449	3.1590
C to Z ↑	0.0578	0.0594	8.0764	4.4235
	C8T28SOIDV_LL_-XNOR3X9_P4	**C8T28SOIDV_LL_-XNOR3X13_P4**	**C8T28SOIDV_LL_-XNOR3X9_P4**	**C8T28SOIDV_LL_-XNOR3X13_P4**
A to Z ↓	0.0408	0.0467	1.5970	1.0979
A to Z ↑	0.0424	0.0484	2.1641	1.5105
B to Z ↓	0.0415	0.0475	1.5966	1.0979
B to Z ↑	0.0433	0.0495	2.1638	1.5112
C to Z ↓	0.0585	0.0703	1.5955	1.0969
C to Z ↑	0.0599	0.0723	2.1637	1.5104
	C8T28SOIDV_LLS_-XNOR3X1_P4	**C8T28SOIDV_LLS_-XNOR3X2_P4**	**C8T28SOIDV_LLS_-XNOR3X1_P4**	**C8T28SOIDV_LLS_-XNOR3X2_P4**
A to Z ↓	0.0276	0.0306	10.6689	5.9256
A to Z ↑	0.0288	0.0284	17.5370	9.2993
B to Z ↓	0.0283	0.0315	10.6885	5.9337
B to Z ↑	0.0295	0.0292	17.5280	9.2960
C to Z ↓	0.0274	0.0299	10.7034	5.9514
C to Z ↑	0.0289	0.0281	17.5221	9.2985
	C8T28SOIDV_LLS_-XNOR3X5_P4	**C8T28SOIDV_LLS_-XNOR3X7_P4**	**C8T28SOIDV_LLS_-XNOR3X5_P4**	**C8T28SOIDV_LLS_-XNOR3X7_P4**
A to Z ↓	0.0314	0.0269	2.8650	1.9859
A to Z ↑	0.0303	0.0263	4.5886	3.0732
B to Z ↓	0.0310	0.0261	2.8717	1.9922
B to Z ↑	0.0300	0.0259	4.5890	3.0743
C to Z ↓	0.0296	0.0253	2.8719	1.9955
C to Z ↑	0.0287	0.0247	4.5847	3.0734

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P4	1.697e-06	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P4	2.119e-06	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P4	3.972e-06	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P4	5.707e-06	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P4	1.117e-06	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P4	2.181e-06	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P4	5.353e-06	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P4	8.187e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P4	C8T28SOIDV_LL_-XNOR3X4_P4	C8T28SOIDV_LL_-XNOR3X9_P4	C8T28SOIDV_LL_-XNOR3X13_P4
A to Z	2.164e-03	2.541e-03	3.773e-03	6.269e-03
B to Z	2.122e-03	2.502e-03	3.756e-03	6.245e-03
C to Z	3.380e-03	3.811e-03	5.358e-03	8.705e-03
	C8T28SOIDV_LLS_-XNOR3X1_P4	C8T28SOIDV_LLS_-XNOR3X2_P4	C8T28SOIDV_LLS_-XNOR3X5_P4	C8T28SOIDV_LLS_-XNOR3X7_P4
A to Z	1.300e-03	1.874e-03	4.124e-03	5.652e-03
B to Z	1.265e-03	1.860e-03	4.019e-03	5.388e-03
C to Z	1.224e-03	1.811e-03	3.886e-03	5.212e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

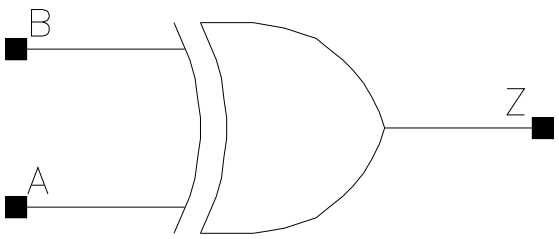
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P4	C8T28SOIDV_LL_-XNOR3X4_P4	C8T28SOIDV_LL_-XNOR3X9_P4	C8T28SOIDV_LL_-XNOR3X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P4	C8T28SOIDV_LLS_-XNOR3X2_P4	C8T28SOIDV_LLS_-XNOR3X5_P4	C8T28SOIDV_LLS_-XNOR3X7_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.360	1.0880
X4_P4	1.600	0.544	0.8704
X5_P4	0.800	1.360	1.0880
X8_P4	1.600	1.088	1.7408
X9_P4	0.800	1.496	1.1968
X12_P4	1.600	1.360	2.1760
X13_P4	0.800	2.176	1.7408
X15_P4	1.600	1.904	3.0464
X17_P4	0.800	2.312	1.8496
X18_P4	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P4	X4_P4	X5_P4	X8_P4
A	0.0005	0.0010	0.0007	0.0015
B	0.0010	0.0009	0.0011	0.0015
	X9_P4	X12_P4	X13_P4	X15_P4
A	0.0007	0.0024	0.0012	0.0028
B	0.0014	0.0019	0.0021	0.0023
	X17_P4	X18_P4		
A	0.0012	0.0016		
B	0.0022	0.0019		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X4_P4**	**X2_P4**	**X4_P4**
A to Z ↓	0.0379	0.0161	5.5916	2.9609
A to Z ↑	0.0361	0.0195	8.3141	7.8555
B to Z ↓	0.0294	0.0165	5.5552	2.9886
B to Z ↑	0.0298	0.0181	8.3070	7.8525
	X5_P4	**X8_P4**	**X5_P4**	**X8_P4**
A to Z ↓	0.0355	0.0207	3.0235	1.6171
A to Z ↑	0.0323	0.0234	4.2633	4.1324
B to Z ↓	0.0273	0.0217	3.0112	1.6348
B to Z ↑	0.0264	0.0221	4.2623	4.1306
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0347	0.0189	1.5857	1.0870
A to Z ↑	0.0326	0.0211	2.2245	2.7700
B to Z ↓	0.0270	0.0184	1.5806	1.0983
B to Z ↑	0.0262	0.0192	2.2262	2.7694
	X13_P4	**X15_P4**	**X13_P4**	**X15_P4**
A to Z ↓	0.0320	0.0205	1.0865	0.8487
A to Z ↑	0.0300	0.0242	1.5426	2.4711
B to Z ↓	0.0230	0.0198	1.0828	0.8584
B to Z ↑	0.0216	0.0220	1.5401	2.4692
	X17_P4	**X18_P4**	**X17_P4**	**X18_P4**
A to Z ↓	0.0337	0.0377	0.8221	0.8208
A to Z ↑	0.0313	0.0338	1.1535	1.1186
B to Z ↓	0.0249	0.0304	0.8201	0.8205
B to Z ↑	0.0231	0.0269	1.1530	1.1168

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P4	1.889e-06	1.000e-20
X4_P4	2.566e-06	1.000e-20
X5_P4	3.247e-06	1.000e-20
X8_P4	4.004e-06	1.000e-20
X9_P4	5.696e-06	1.000e-20
X12_P4	6.156e-06	1.000e-20
X13_P4	9.104e-06	1.000e-20
X15_P4	7.293e-06	1.000e-20
X17_P4	9.812e-06	1.000e-20
X18_P4	9.440e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P4	X4_P4	X5_P4	X8_P4
A to Z	2.558e-03	1.658e-03	3.218e-03	3.275e-03
B to Z	2.240e-03	1.591e-03	2.761e-03	3.237e-03
	X9_P4	X12_P4	X13_P4	X15_P4
A to Z	4.601e-03	4.631e-03	7.508e-03	6.022e-03
B to Z	4.030e-03	4.368e-03	5.032e-03	5.741e-03
	X17_P4	X18_P4		
A to Z	8.446e-03	9.379e-03		
B to Z	5.941e-03	7.264e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

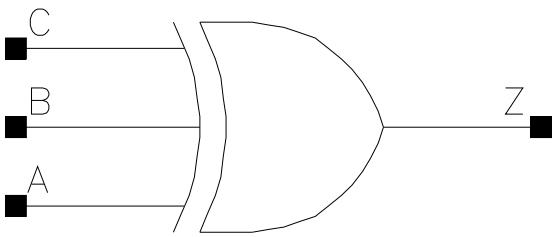
Pin Cycle (vdds)	X2_P4	X4_P4	X5_P4	X8_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P4	X12_P4	X13_P4	X15_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P4	X18_P4		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P4	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P4	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P4	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P4	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P4	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P4	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P4	C8T28SOIDV_LL_-XOR3X4_P4	C8T28SOIDV_LL_-XOR3X9_P4	C8T28SOIDV_LL_-XOR3X13_P4
A	0.0016	0.0014	0.0017	0.0025
B	0.0015	0.0016	0.0018	0.0024
C	0.0009	0.0010	0.0012	0.0020
	C8T28SOIDV_LLS_-XOR3X1_P4	C8T28SOIDV_LLS_-XOR3X2_P4	C8T28SOIDV_LLS_-XOR3X5_P4	C8T28SOIDV_LLS_-XOR3X7_P4

A	0.0016	0.0017	0.0028	0.0044
B	0.0017	0.0017	0.0028	0.0045
C	0.0006	0.0005	0.0005	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P4	**C8T28SOIDV_LL_-XOR3X4_P4**	**C8T28SOIDV_LL_-XOR3X2_P4**	**C8T28SOIDV_LL_-XOR3X4_P4**
A to Z ↓	0.0435	0.0474	5.8771	3.1722
A to Z ↑	0.0416	0.0445	8.3188	4.4309
B to Z ↓	0.0438	0.0483	5.8794	3.1727
B to Z ↑	0.0421	0.0456	8.3170	4.4326
C to Z ↓	0.0433	0.0476	5.8794	3.1720
C to Z ↑	0.0414	0.0446	8.3185	4.4331
	C8T28SOIDV_LL_-XOR3X9_P4	**C8T28SOIDV_LL_-XOR3X13_P4**	**C8T28SOIDV_LL_-XOR3X9_P4**	**C8T28SOIDV_LL_-XOR3X13_P4**
A to Z ↓	0.0431	0.0479	1.5846	1.0758
A to Z ↑	0.0435	0.0492	2.1797	1.4676
B to Z ↓	0.0441	0.0486	1.5842	1.0763
B to Z ↑	0.0446	0.0503	2.1802	1.4689
C to Z ↓	0.0431	0.0482	1.5844	1.0764
C to Z ↑	0.0431	0.0500	2.1801	1.4681
	C8T28SOIDV_LLS_-XOR3X1_P4	**C8T28SOIDV_LLS_-XOR3X2_P4**	**C8T28SOIDV_LLS_-XOR3X1_P4**	**C8T28SOIDV_LLS_-XOR3X2_P4**
A to Z ↓	0.0287	0.0317	7.6124	6.0490
A to Z ↑	0.0290	0.0284	12.6676	8.8808
B to Z ↓	0.0296	0.0323	7.6381	6.0586
B to Z ↑	0.0298	0.0289	12.6728	8.8788
C to Z ↓	0.0450	0.0484	7.5733	6.0127
C to Z ↑	0.0460	0.0458	12.6289	8.8265
	C8T28SOIDV_LLS_-XOR3X5_P4	**C8T28SOIDV_LLS_-XOR3X7_P4**	**C8T28SOIDV_LLS_-XOR3X5_P4**	**C8T28SOIDV_LLS_-XOR3X7_P4**
A to Z ↓	0.0419	0.0359	3.1425	2.1801
A to Z ↑	0.0354	0.0306	4.6279	3.1318
B to Z ↓	0.0399	0.0357	3.1534	2.1860
B to Z ↑	0.0347	0.0308	4.6304	3.1333
C to Z ↓	0.0668	0.0558	3.1479	2.1741
C to Z ↑	0.0620	0.0512	4.6132	3.1171

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P4	1.367e-06	1.000e-20
C8T28SOIDV_LL_XOR3X4_P4	1.848e-06	1.000e-20
C8T28SOIDV_LL_XOR3X9_P4	3.651e-06	1.000e-20
C8T28SOIDV_LL_XOR3X13_P4	5.440e-06	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P4	2.113e-06	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P4	2.604e-06	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P4	4.493e-06	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P4	6.692e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P4	C8T28SOIDV_LL_-XOR3X4_P4	C8T28SOIDV_LL_-XOR3X9_P4	C8T28SOIDV_LL_-XOR3X13_P4
A to Z	2.058e-03	2.537e-03	3.804e-03	6.620e-03
B to Z	2.008e-03	2.507e-03	3.785e-03	6.577e-03
C to Z	1.965e-03	2.456e-03	3.734e-03	6.540e-03
	C8T28SOIDV_LLS_-XOR3X1_P4	C8T28SOIDV_LLS_-XOR3X2_P4	C8T28SOIDV_LLS_-XOR3X5_P4	C8T28SOIDV_LLS_-XOR3X7_P4
A to Z	1.583e-03	1.923e-03	3.823e-03	5.334e-03
B to Z	1.560e-03	1.908e-03	3.763e-03	5.261e-03
C to Z	2.982e-03	3.400e-03	6.256e-03	8.760e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P4	C8T28SOIDV_LL_-XOR3X4_P4	C8T28SOIDV_LL_-XOR3X9_P4	C8T28SOIDV_LL_-XOR3X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P4	C8T28SOIDV_LLS_-XOR3X2_P4	C8T28SOIDV_LLS_-XOR3X5_P4	C8T28SOIDV_LLS_-XOR3X7_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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