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C28SOI_SC_12_COREPBP16_LR Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 16 nm

Overview

- C28SOI_SC_12_COREPBP16_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

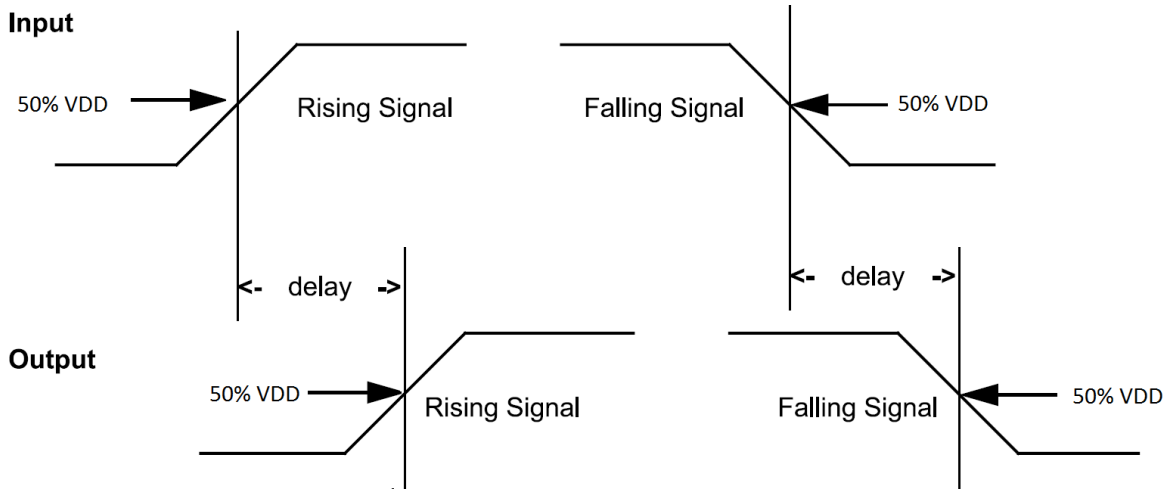


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

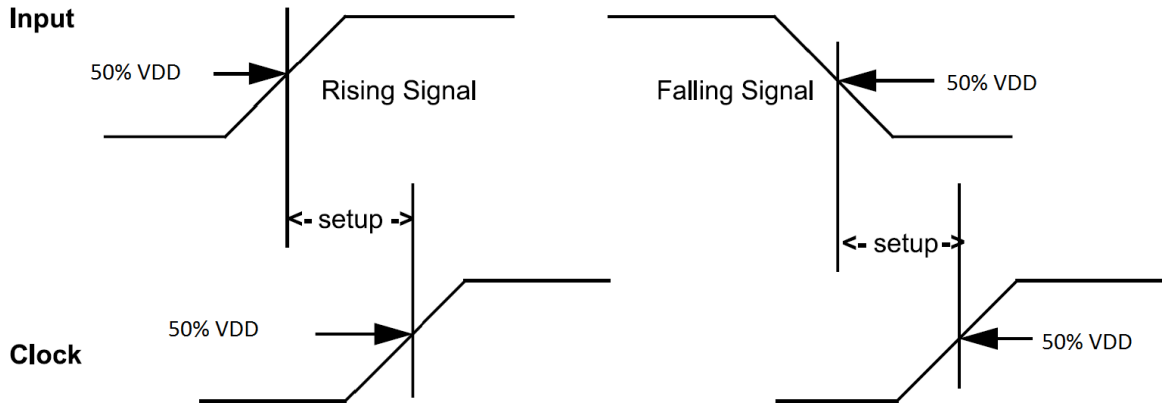


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

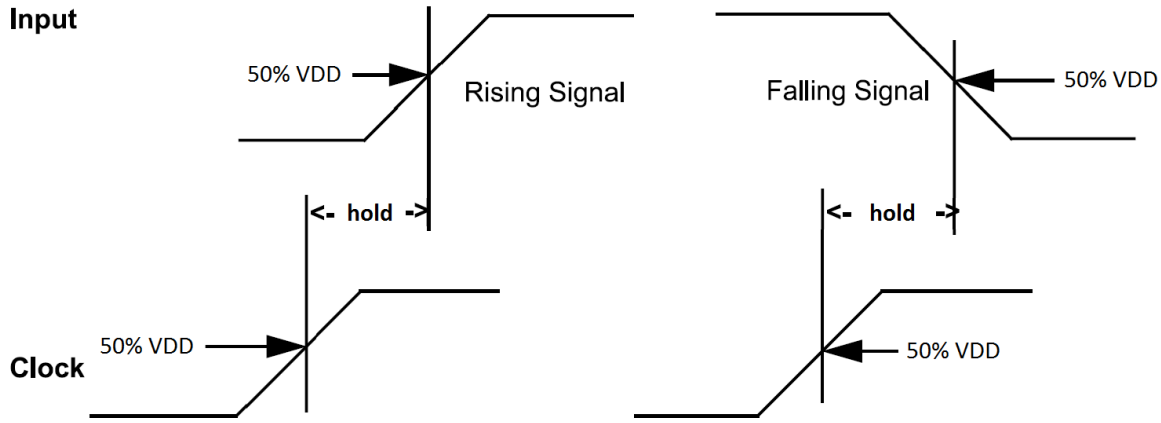


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

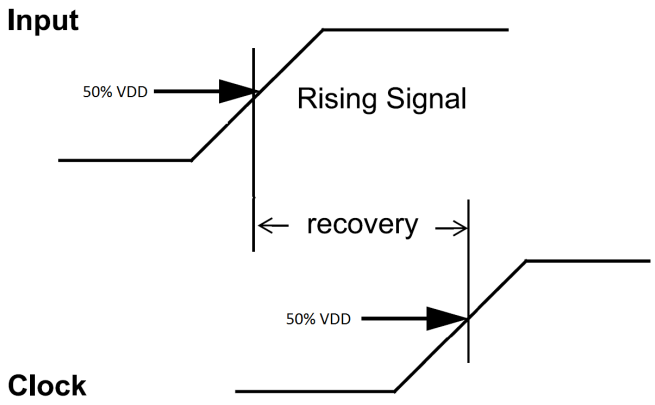


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

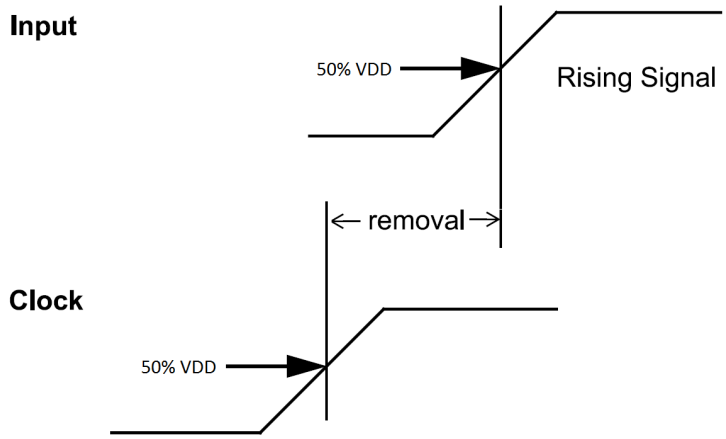


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

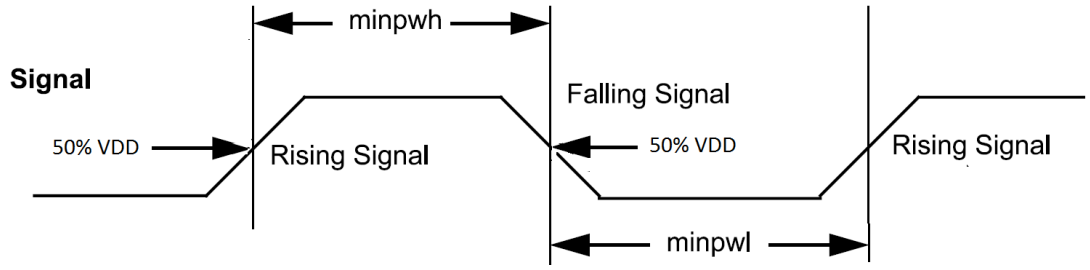


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

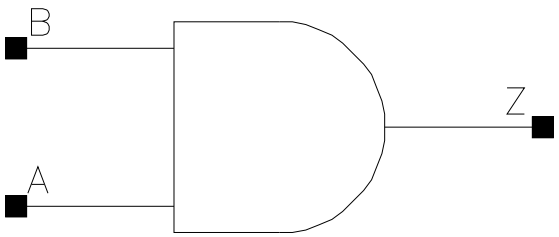
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X25_P16	1.200	1.088	1.3056
X33_P16	1.200	1.360	1.6320
X42_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0008	0.0012	0.0018	0.0022
B	0.0007	0.0011	0.0017	0.0022
	X42_P16			
A	0.0022			
B	0.0022			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0465	0.0386	2.1690	1.1018
A to Z ↑	0.0348	0.0319	4.3224	2.1003
B to Z ↓	0.0443	0.0365	2.1705	1.1018
B to Z ↑	0.0363	0.0331	4.3268	2.1021
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0399	0.0387	0.7332	0.5434

A to Z ↑	0.0319	0.0326	1.3857	1.0454
B to Z ↓	0.0379	0.0357	0.7325	0.5424
B to Z ↑	0.0331	0.0329	1.3878	1.0458
	X42_P16		**X42_P16**	
A to Z ↓	0.0414		0.4422	
A to Z ↑	0.0351		0.8380	
B to Z ↓	0.0385		0.4419	
B to Z ↑	0.0356		0.8379	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	8.585e-08	1.773e-12
X16_P16	1.620e-07	2.026e-12
X25_P16	2.473e-07	2.781e-12
X33_P16	3.342e-07	3.286e-12
X42_P16	3.816e-07	3.536e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	8.936e-06	1.662e-05	2.578e-05	4.412e-05
B (output stable)	4.020e-05	7.469e-05	1.153e-04	4.061e-04
A to Z	2.463e-03	3.966e-03	6.190e-03	8.105e-03
B to Z	2.303e-03	3.681e-03	5.751e-03	7.237e-03
	X42_P16			
A (output stable)	4.476e-05			
B (output stable)	4.016e-04			
A to Z	9.582e-03			
B to Z	8.726e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

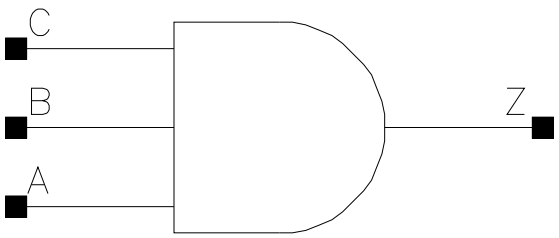
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	2.720e-08	-2.127e-08	-4.620e-08	-7.040e-08
B (output stable)	3.300e-08	-4.660e-08	-1.205e-07	-1.945e-07
A to Z	-2.604e-07	-2.066e-07	-4.416e-07	-6.116e-07
B to Z	-2.539e-07	-2.507e-07	-1.960e-07	-6.721e-07
	X42_P16			
A (output stable)	-6.830e-08			
B (output stable)	-1.952e-07			
A to Z	-1.253e-06			
B to Z	-8.457e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X25_P16	1.200	1.360	1.6320
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0007	0.0012	0.0019	0.0023
B	0.0006	0.0011	0.0017	0.0021
C	0.0007	0.0011	0.0016	0.0021

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0502	0.0424	2.1965	1.0737
A to Z ↑	0.0454	0.0417	4.3572	2.0781
B to Z ↓	0.0486	0.0406	2.1961	1.0737
B to Z ↑	0.0454	0.0418	4.3589	2.0785
C to Z ↓	0.0465	0.0385	2.1952	1.0726
C to Z ↑	0.0464	0.0420	4.3585	2.0783
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0427	0.0406	0.7413	0.5532

A to Z ↑	0.0415	0.0395	1.4190	1.0625
B to Z ↓	0.0410	0.0388	0.7410	0.5523
B to Z ↑	0.0417	0.0398	1.4184	1.0630
C to Z ↓	0.0388	0.0368	0.7406	0.5523
C to Z ↑	0.0420	0.0401	1.4184	1.0621

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	9.500e-08	2.024e-12
X17_P16	1.875e-07	2.277e-12
X25_P16	2.771e-07	3.283e-12
X33_P16	3.700e-07	3.535e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	3.934e-06	6.537e-06	7.830e-06	1.132e-05
B (output stable)	1.698e-05	3.310e-05	4.794e-05	6.423e-05
C (output stable)	1.420e-05	2.732e-05	4.009e-05	5.487e-05
A to Z	2.697e-03	4.636e-03	6.792e-03	8.620e-03
B to Z	2.542e-03	4.360e-03	6.380e-03	8.069e-03
C to Z	2.415e-03	4.079e-03	5.953e-03	7.497e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

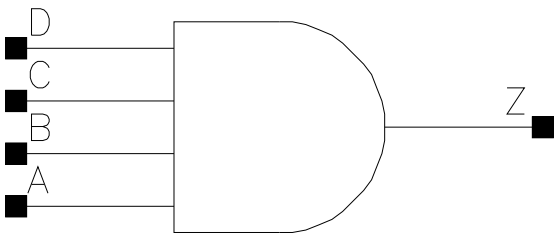
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	5.177e-08	-1.122e-08	-7.207e-08	-1.123e-07
B (output stable)	4.625e-08	-8.990e-09	-5.343e-08	-1.152e-07
C (output stable)	4.143e-08	-3.080e-08	-8.777e-08	-1.577e-07
A to Z	-3.306e-07	-2.837e-07	-4.609e-07	-7.335e-07
B to Z	-3.639e-07	-2.603e-07	-1.282e-07	-6.962e-07
C to Z	-1.755e-07	-4.918e-07	-4.928e-07	-4.171e-07

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X6_P16	1.200	1.088	1.3056
X20_P16	1.200	2.312	2.7744
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P16	X6_P16	X20_P16	X27_P16
A	0.0006	0.0009	0.0019	0.0022
B	0.0005	0.0008	0.0019	0.0022
C	0.0005	0.0008	0.0019	0.0022
D	0.0005	0.0008	0.0019	0.0022

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X6_P16	X4_P16	X6_P16
A to Z ↓	0.0533	0.0450	4.0744	2.6490
A to Z ↑	0.0501	0.0384	16.4872	8.8057
B to Z ↓	0.0518	0.0423	4.0789	2.6485
B to Z ↑	0.0516	0.0393	16.4855	8.8123
C to Z ↓	0.0550	0.0478	4.0585	2.6745
C to Z ↑	0.0482	0.0366	16.4945	8.8309

D to Z ↓	0.0534	0.0444	4.0590	2.6739
D to Z ↑	0.0507	0.0376	16.5223	8.8270
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0434	0.0409	0.7767	0.5494
A to Z ↑	0.0392	0.0435	2.9323	2.2232
B to Z ↓	0.0399	0.0380	0.7758	0.5487
B to Z ↑	0.0391	0.0437	2.9319	2.2236
C to Z ↓	0.0426	0.0395	0.7847	0.5531
C to Z ↑	0.0340	0.0365	2.9346	2.2229
D to Z ↓	0.0388	0.0367	0.7843	0.5534
D to Z ↑	0.0340	0.0370	2.9362	2.2224

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	9.348e-08	2.780e-12
X6_P16	1.619e-07	2.780e-12
X20_P16	4.902e-07	5.047e-12
X27_P16	6.134e-07	5.557e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	4.694e-04	7.178e-04	2.107e-03	2.622e-03
B (output stable)	4.294e-04	6.292e-04	1.783e-03	2.279e-03
C (output stable)	4.365e-04	7.038e-04	1.780e-03	2.190e-03
D (output stable)	4.014e-04	6.125e-04	1.474e-03	1.811e-03
A to Z	1.852e-03	2.843e-03	8.412e-03	1.090e-02
B to Z	1.754e-03	2.640e-03	7.643e-03	1.009e-02
C to Z	1.782e-03	2.813e-03	7.066e-03	8.764e-03
D to Z	1.689e-03	2.597e-03	6.264e-03	7.949e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

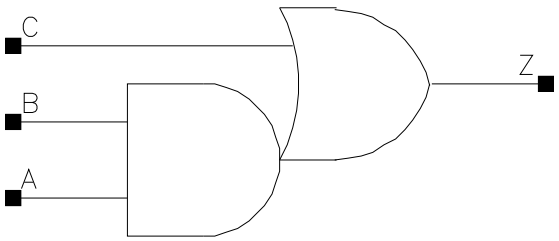
Pin Cycle (vdds)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	-5.119e-06	-9.261e-06	-3.282e-05	-5.438e-05
B (output stable)	-4.868e-06	-8.285e-06	-2.890e-05	-4.810e-05
C (output stable)	5.105e-06	9.191e-06	3.546e-05	5.907e-05
D (output stable)	8.547e-08	3.784e-08	-1.318e-06	-1.369e-06
A to Z	-1.969e-06	-3.897e-06	-1.197e-05	-1.985e-05
B to Z	-1.884e-06	-3.583e-06	-1.212e-05	-1.984e-05
C to Z	-2.363e-07	-4.309e-07	-1.246e-06	-1.834e-06
D to Z	-1.989e-07	-3.268e-07	-1.146e-06	-1.357e-06

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0010	0.0021
B	0.0007	0.0011	0.0020
C	0.0008	0.0012	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0617	0.0551	2.2538	1.1036
A to Z ↑	0.0360	0.0320	4.2179	2.0621
B to Z ↓	0.0571	0.0509	2.2479	1.1002
B to Z ↑	0.0378	0.0339	4.2176	2.0636
C to Z ↓	0.0610	0.0550	2.2408	1.0978
C to Z ↑	0.0320	0.0299	4.1916	2.0538
	X33_P16		**X33_P16**	
A to Z ↓	0.0551		0.5600	
A to Z ↑	0.0326		1.0398	

B to Z ↓	0.0508		0.5601	
B to Z ↑	0.0337		1.0392	
C to Z ↓	0.0547		0.5580	
C to Z ↑	0.0294		1.0348	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	9.668e-08	2.024e-12
X17_P16	1.817e-07	2.276e-12
X33_P16	3.642e-07	3.787e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	4.378e-06	7.091e-06	1.820e-05
B (output stable)	2.305e-05	3.558e-05	1.289e-04
C (output stable)	2.437e-04	3.781e-04	8.097e-04
A to Z	2.469e-03	4.157e-03	8.228e-03
B to Z	2.321e-03	3.877e-03	7.520e-03
C to Z	2.774e-03	4.720e-03	9.277e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

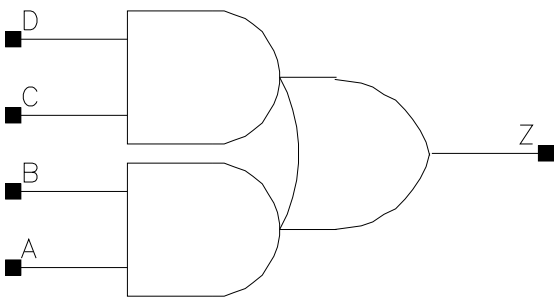
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	2.191e-06	4.385e-06	6.323e-06
B (output stable)	1.470e-05	2.393e-05	4.537e-05
C (output stable)	-4.843e-05	-7.334e-05	-1.374e-04
A to Z	-3.586e-07	-6.559e-07	-1.265e-06
B to Z	-3.213e-07	-2.373e-07	-1.018e-06
C to Z	-1.002e-05	-1.694e-05	-3.074e-05

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0006	0.0010	0.0021
B	0.0007	0.0011	0.0019
C	0.0006	0.0010	0.0021
D	0.0007	0.0011	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0708	0.0618	2.1700	1.0908
A to Z ↑	0.0443	0.0400	4.1506	2.0627
B to Z ↓	0.0660	0.0575	2.1640	1.0884
B to Z ↑	0.0455	0.0415	4.1530	2.0636

C to Z ↓	0.0631	0.0558	2.1621	1.0872
C to Z ↑	0.0388	0.0349	4.1442	2.0585
D to Z ↓	0.0601	0.0528	2.1576	1.0857
D to Z ↑	0.0410	0.0367	4.1464	2.0577
	X33_P16		**X33_P16**	
A to Z ↓	0.0593		0.5603	
A to Z ↑	0.0369		1.0435	
B to Z ↓	0.0561		0.5603	
B to Z ↑	0.0388		1.0433	
C to Z ↓	0.0534		0.5591	
C to Z ↑	0.0328		1.0409	
D to Z ↓	0.0503		0.5586	
D to Z ↑	0.0344		1.0406	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.195e-07	2.527e-12
X17_P16	2.257e-07	2.779e-12
X33_P16	4.382e-07	4.294e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.309e-05	3.651e-05	4.345e-05
B (output stable)	4.372e-05	5.877e-05	4.726e-05
C (output stable)	5.226e-06	1.097e-05	1.913e-05
D (output stable)	2.401e-05	4.405e-05	8.880e-05
A to Z	3.244e-03	5.358e-03	1.009e-02
B to Z	3.023e-03	5.005e-03	9.551e-03
C to Z	2.726e-03	4.505e-03	8.354e-03
D to Z	2.595e-03	4.245e-03	7.791e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

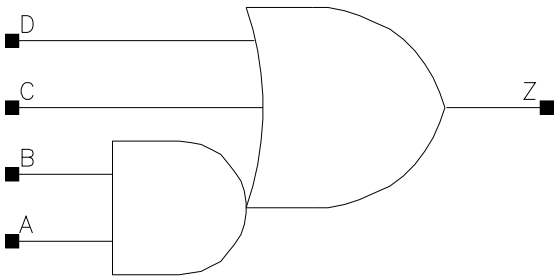
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	4.255e-07	-1.079e-06	-3.099e-06
B (output stable)	-7.919e-07	-1.077e-06	-2.378e-06
C (output stable)	8.435e-08	7.648e-08	1.990e-07
D (output stable)	8.256e-07	1.440e-06	2.014e-06
A to Z	-3.552e-06	-7.886e-06	-1.978e-05
B to Z	-6.509e-06	-1.219e-05	-3.117e-05
C to Z	-1.949e-07	-3.299e-07	-1.328e-06
D to Z	-1.164e-07	-4.042e-07	-9.561e-07

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	0.952	1.1424
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0010	0.0019
B	0.0007	0.0010	0.0019
C	0.0007	0.0010	0.0020
D	0.0007	0.0010	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0829	0.0718	2.3942	1.1795
A to Z ↑	0.0384	0.0345	4.1987	2.1344
B to Z ↓	0.0786	0.0666	2.3920	1.1773
B to Z ↑	0.0405	0.0359	4.2024	2.1378
C to Z ↓	0.0882	0.0768	2.3852	1.1761
C to Z ↑	0.0342	0.0316	4.1790	2.1263

D to Z ↓	0.0863	0.0760	2.3874	1.1764
D to Z ↑	0.0340	0.0317	4.1778	2.1254
	X33_P16		**X33_P16**	
A to Z ↓	0.0727		0.5901	
A to Z ↑	0.0345		1.0410	
B to Z ↓	0.0647		0.5873	
B to Z ↑	0.0351		1.0406	
C to Z ↓	0.0779		0.5876	
C to Z ↑	0.0310		1.0372	
D to Z ↓	0.0756		0.5877	
D to Z ↑	0.0302		1.0348	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.065e-07	2.276e-12
X17_P16	1.989e-07	2.527e-12
X33_P16	4.046e-07	4.543e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.008e-06	3.116e-06	1.379e-05
B (output stable)	7.186e-06	1.294e-05	6.129e-05
C (output stable)	1.321e-04	2.476e-04	6.678e-04
D (output stable)	1.282e-06	1.228e-06	3.588e-06
A to Z	2.664e-03	4.363e-03	8.686e-03
B to Z	2.539e-03	4.079e-03	7.854e-03
C to Z	3.129e-03	5.212e-03	1.049e-02
D to Z	2.933e-03	4.877e-03	9.577e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

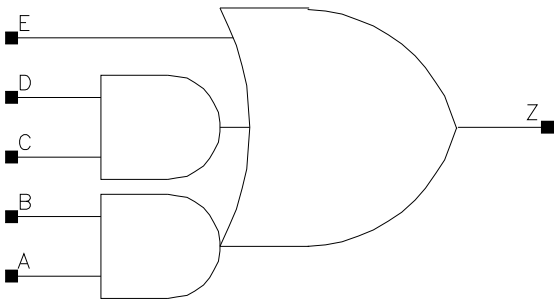
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	1.421e-06	2.233e-06	4.341e-06
B (output stable)	6.228e-06	1.035e-05	2.054e-05
C (output stable)	-2.295e-05	-4.240e-05	-1.099e-04
D (output stable)	4.177e-06	9.057e-06	3.025e-05
A to Z	-3.697e-07	-4.035e-07	-1.009e-06
B to Z	-3.107e-07	-5.326e-07	-1.113e-06
C to Z	-8.553e-06	-1.552e-05	-3.327e-05
D to Z	-6.159e-06	-1.066e-05	-1.917e-05

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.088	1.3056
X17_P16	1.200	1.224	1.4688
X33_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0010	0.0021
B	0.0007	0.0010	0.0019
C	0.0008	0.0012	0.0020
D	0.0007	0.0010	0.0019
E	0.0007	0.0010	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.1020	0.0874	2.2909	1.1404
A to Z ↑	0.0461	0.0397	4.1178	2.0736

B to Z ↓	0.0979	0.0829	2.2841	1.1384
B to Z ↑	0.0489	0.0419	4.1154	2.0742
C to Z ↓	0.0860	0.0745	2.2751	1.1346
C to Z ↑	0.0405	0.0346	4.0885	2.0619
D to Z ↓	0.0797	0.0677	2.2663	1.1301
D to Z ↑	0.0425	0.0362	4.0895	2.0637
E to Z ↓	0.0896	0.0766	2.2630	1.1301
E to Z ↑	0.0358	0.0313	4.0617	2.0512
	X33_P16		**X33_P16**	
A to Z ↓	0.0855		0.5887	
A to Z ↑	0.0408		1.0467	
B to Z ↓	0.0798		0.5882	
B to Z ↑	0.0425		1.0471	
C to Z ↓	0.0718		0.5857	
C to Z ↑	0.0347		1.0406	
D to Z ↓	0.0655		0.5840	
D to Z ↑	0.0360		1.0406	
E to Z ↓	0.0742		0.5838	
E to Z ↑	0.0312		1.0343	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.320e-07	2.778e-12
X17_P16	2.447e-07	3.032e-12
X33_P16	4.735e-07	5.048e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	9.769e-06	2.521e-05	5.628e-05
B (output stable)	6.020e-05	8.822e-05	2.002e-04
C (output stable)	1.016e-05	1.140e-05	3.134e-05
D (output stable)	4.735e-06	8.745e-06	2.216e-05
E (output stable)	9.385e-05	1.252e-04	2.984e-04
A to Z	3.671e-03	5.837e-03	1.145e-02
B to Z	3.576e-03	5.592e-03	1.078e-02
C to Z	2.867e-03	4.552e-03	8.818e-03
D to Z	2.715e-03	4.244e-03	8.123e-03
E to Z	3.197e-03	5.062e-03	9.759e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-9.496e-07	-3.166e-06	-6.763e-06
B (output stable)	-9.625e-06	-1.483e-05	-3.029e-05
C (output stable)	5.822e-06	9.383e-06	2.068e-05
D (output stable)	5.498e-07	1.095e-06	3.667e-07
E (output stable)	-2.663e-06	-4.872e-06	-1.723e-05
A to Z	-9.861e-06	-1.524e-05	-3.231e-05
B to Z	-1.238e-05	-2.010e-05	-4.365e-05
C to Z	-3.091e-07	-4.768e-07	-1.648e-06
D to Z	-1.778e-07	-4.355e-07	-1.202e-06

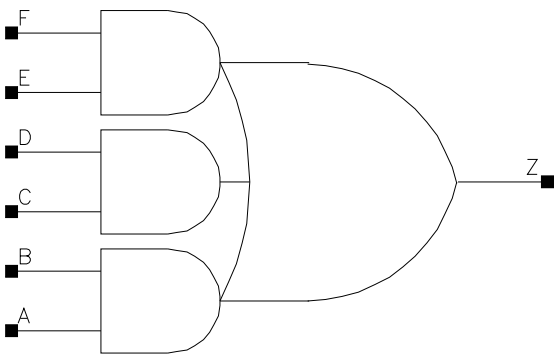
E to Z	-6.419e-06	-1.061e-05	-2.116e-05

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.360	1.6320
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
A	0.0007	0.0008	0.0010	0.0020

B	0.0007	0.0008	0.0013	0.0019
C	0.0006	0.0007	0.0010	0.0020
D	0.0006	0.0008	0.0010	0.0018
E	0.0007	0.0008	0.0010	0.0020
F	0.0007	0.0008	0.0010	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.1005	0.0951	4.3060	2.2634
A to Z ↑	0.0484	0.0464	8.2438	4.1881
B to Z ↓	0.0923	0.0881	4.2878	2.2547
B to Z ↑	0.0492	0.0477	8.2432	4.1866
C to Z ↓	0.0919	0.0877	4.2914	2.2575
C to Z ↑	0.0445	0.0427	8.1963	4.1653
D to Z ↓	0.0873	0.0833	4.2802	2.2507
D to Z ↑	0.0469	0.0452	8.1977	4.1662
E to Z ↓	0.0762	0.0742	4.2645	2.2454
E to Z ↑	0.0389	0.0375	8.1679	4.1511
F to Z ↓	0.0707	0.0689	4.2534	2.2384
F to Z ↑	0.0406	0.0392	8.1669	4.1513
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
A to Z ↓	0.0919	0.0884	1.1427	0.5874
A to Z ↑	0.0430	0.0435	2.0793	1.0498
B to Z ↓	0.0864	0.0832	1.1372	0.5869
B to Z ↑	0.0453	0.0453	2.0786	1.0502
C to Z ↓	0.0855	0.0830	1.1394	0.5867
C to Z ↑	0.0397	0.0410	2.0689	1.0450
D to Z ↓	0.0806	0.0780	1.1354	0.5860
D to Z ↑	0.0420	0.0428	2.0689	1.0449
E to Z ↓	0.0720	0.0730	1.1328	0.5840
E to Z ↑	0.0347	0.0365	2.0627	1.0423
F to Z ↓	0.0670	0.0673	1.1295	0.5826
F to Z ↑	0.0365	0.0383	2.0622	1.0427

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	1.310e-07	3.284e-12
X8_P16	1.790e-07	3.283e-12
X17_P16	2.830e-07	3.535e-12
X33_P16	5.388e-07	5.550e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	5.436e-05	6.654e-05	8.134e-05	1.659e-04
B (output stable)	2.011e-04	2.426e-04	3.099e-04	5.896e-04
C (output stable)	2.393e-05	2.987e-05	4.260e-05	7.300e-05
D (output stable)	3.348e-05	4.231e-05	5.308e-05	1.083e-04
E (output stable)	2.492e-05	2.659e-05	2.974e-05	3.973e-05
F (output stable)	2.287e-05	2.605e-05	3.419e-05	7.303e-05

A to Z	3.424e-03	4.418e-03	6.504e-03	1.245e-02
B to Z	3.171e-03	4.126e-03	6.131e-03	1.175e-02
C to Z	2.918e-03	3.815e-03	5.695e-03	1.093e-02
D to Z	2.784e-03	3.645e-03	5.416e-03	1.025e-02
E to Z	2.342e-03	3.169e-03	4.734e-03	9.372e-03
F to Z	2.194e-03	2.976e-03	4.451e-03	8.725e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

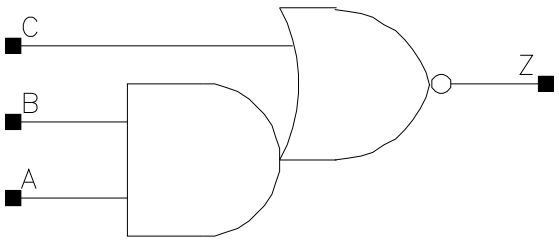
Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	-5.584e-06	-7.065e-06	-9.950e-06	-2.084e-05
B (output stable)	-2.253e-05	-2.793e-05	-3.957e-05	-8.191e-05
C (output stable)	-2.467e-06	-2.966e-06	-3.966e-06	-3.873e-06
D (output stable)	-1.109e-06	-1.350e-06	-1.619e-06	8.165e-06
E (output stable)	1.462e-05	1.803e-05	2.504e-05	4.190e-05
F (output stable)	1.006e-05	1.235e-05	1.735e-05	3.420e-05
A to Z	-1.109e-05	-1.413e-05	-1.990e-05	-3.727e-05
B to Z	-1.170e-05	-1.418e-05	-2.019e-05	-3.858e-05
C to Z	-8.696e-06	-1.052e-05	-1.428e-05	-2.261e-05
D to Z	-7.261e-06	-8.950e-06	-1.190e-05	-1.705e-05
E to Z	-4.202e-07	-4.903e-07	-7.808e-07	-1.680e-06
F to Z	-3.105e-07	-3.983e-07	-5.781e-07	-1.070e-06

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008
X44_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X33_P16	X44_P16
A	0.0008	0.0025	0.0050	0.0068
B	0.0008	0.0024	0.0047	0.0062
C	0.0009	0.0027	0.0052	0.0068

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0141	0.0149	3.9898	1.3568
A to Z ↑	0.0281	0.0288	8.9492	2.9783
B to Z ↓	0.0138	0.0142	4.0270	1.3771
B to Z ↑	0.0230	0.0230	8.8531	2.9866
C to Z ↓	0.0142	0.0145	2.2035	0.7586
C to Z ↑	0.0297	0.0298	8.1955	2.7501
	X33_P16	**X44_P16**	**X33_P16**	**X44_P16**
A to Z ↓	0.0153	0.0152	0.6907	0.5234

A to Z ↑	0.0289	0.0289	1.4892	1.1279
B to Z ↓	0.0141	0.0140	0.7005	0.5311
B to Z ↑	0.0228	0.0226	1.4915	1.1276
C to Z ↓	0.0160	0.0162	0.4518	0.3523
C to Z ↑	0.0303	0.0301	1.3727	1.0381

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P16	1.007e-07	1.772e-12
X17_P16	2.997e-07	3.290e-12
X33_P16	5.719e-07	5.557e-12
X44_P16	7.542e-07	7.054e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	7.299e-06	2.706e-05	5.585e-05	7.446e-05
B (output stable)	3.727e-05	1.718e-04	3.925e-04	5.068e-04
C (output stable)	3.727e-04	1.120e-03	2.441e-03	3.211e-03
A to Z	1.105e-03	3.543e-03	7.170e-03	9.478e-03
B to Z	8.140e-04	2.406e-03	4.758e-03	6.264e-03
C to Z	1.633e-03	4.918e-03	1.007e-02	1.328e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

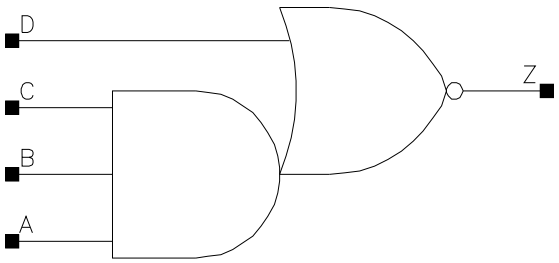
Pin Cycle (vdds)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	3.232e-06	9.838e-06	1.773e-05	2.377e-05
B (output stable)	2.155e-05	4.892e-05	1.106e-04	1.409e-04
C (output stable)	-6.685e-05	-1.604e-04	-3.564e-04	-4.546e-04
A to Z	-7.656e-07	-2.836e-06	-2.220e-06	-2.975e-06
B to Z	-1.769e-07	-1.688e-06	-1.670e-06	-2.085e-06
C to Z	-1.478e-05	-3.814e-05	-8.040e-05	-1.036e-04

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X29_P16	1.200	3.536	4.2432
X38_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X29_P16	X38_P16
A	0.0009	0.0052	0.0067
B	0.0008	0.0049	0.0064
C	0.0008	0.0047	0.0061
D	0.0009	0.0052	0.0065

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X29_P16	X5_P16	X29_P16
A to Z ↓	0.0199	0.0214	5.7984	1.0045
A to Z ↑	0.0355	0.0357	8.9371	1.4764
B to Z ↓	0.0198	0.0205	5.8106	1.0074
B to Z ↑	0.0316	0.0314	8.9399	1.4860
C to Z ↓	0.0190	0.0187	5.8361	1.0141
C to Z ↑	0.0269	0.0259	8.8606	1.4986
D to Z ↓	0.0165	0.0184	2.2496	0.4553

D to Z ↑	0.0335	0.0341	7.6494	1.2756
	X38_P16		**X38_P16**	
A to Z ↓	0.0210		0.7756	
A to Z ↑	0.0349		1.1115	
B to Z ↓	0.0204		0.7781	
B to Z ↑	0.0309		1.1215	
C to Z ↓	0.0185		0.7840	
C to Z ↑	0.0254		1.1346	
D to Z ↓	0.0192		0.3774	
D to Z ↑	0.0333		0.9617	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P16	1.193e-07	2.024e-12
X29_P16	6.870e-07	7.312e-12
X38_P16	8.940e-07	9.335e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P16	X29_P16	X38_P16
A (output stable)	6.908e-06	7.133e-05	8.592e-05
B (output stable)	1.372e-05	9.060e-05	1.176e-04
C (output stable)	3.097e-05	3.789e-04	4.827e-04
D (output stable)	5.077e-04	3.817e-03	4.993e-03
A to Z	1.721e-03	1.090e-02	1.386e-02
B to Z	1.449e-03	8.709e-03	1.116e-02
C to Z	1.155e-03	6.325e-03	7.992e-03
D to Z	2.148e-03	1.314e-02	1.689e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

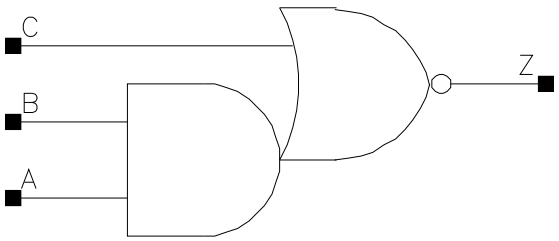
Pin Cycle (vdds)	X5_P16	X29_P16	X38_P16
A (output stable)	1.052e-05	8.013e-05	1.026e-04
B (output stable)	1.484e-06	1.080e-05	1.356e-05
C (output stable)	1.151e-06	5.426e-06	6.486e-06
D (output stable)	-6.744e-05	-5.665e-04	-7.169e-04
A to Z	-9.230e-07	-9.190e-07	-5.122e-06
B to Z	1.700e-08	-4.790e-07	-6.570e-07
C to Z	2.120e-07	-1.385e-06	-1.721e-06
D to Z	-1.186e-05	-8.481e-05	-1.094e-04

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X11_P16	1.200	1.088	1.3056
X16_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X11_P16	X16_P16	X23_P16
A	0.0009	0.0019	0.0028	0.0037
B	0.0009	0.0018	0.0026	0.0034
C	0.0009	0.0016	0.0024	0.0034
	X46_P16			
A	0.0071			
B	0.0066			
C	0.0066			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X11_P16	X6_P16	X11_P16
A to Z ↓	0.0162	0.0175	3.8475	1.9568
A to Z ↑	0.0323	0.0339	8.9206	4.3585
B to Z ↓	0.0169	0.0171	3.8833	1.9774

B to Z ↑	0.0283	0.0290	8.8427	4.3771
C to Z ↓	0.0107	0.0111	2.2663	1.3361
C to Z ↑	0.0230	0.0226	8.1508	4.0046
	X16_P16	**X23_P16**	**X16_P16**	**X23_P16**
A to Z ↓	0.0169	0.0172	1.3571	1.0194
A to Z ↑	0.0323	0.0327	2.9282	2.2164
B to Z ↓	0.0171	0.0170	1.3724	1.0300
B to Z ↑	0.0274	0.0277	2.9340	2.2273
C to Z ↓	0.0112	0.0102	0.9336	0.5842
C to Z ↑	0.0219	0.0222	2.6889	2.0384
	X46_P16		**X46_P16**	
A to Z ↓	0.0169		0.5240	
A to Z ↑	0.0319		1.1451	
B to Z ↓	0.0167		0.5298	
B to Z ↑	0.0268		1.1444	
C to Z ↓	0.0105		0.3000	
C to Z ↑	0.0222		1.0501	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P16	1.067e-07	1.771e-12
X11_P16	2.102e-07	2.781e-12
X16_P16	3.035e-07	3.286e-12
X23_P16	4.286e-07	4.295e-12
X46_P16	8.447e-07	7.319e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	2.126e-05	5.207e-05	7.447e-05	1.004e-04
B (output stable)	1.707e-04	4.678e-04	5.627e-04	7.826e-04
C (output stable)	2.476e-05	6.791e-05	8.847e-05	1.378e-04
A to Z	1.681e-03	3.727e-03	5.107e-03	6.954e-03
B to Z	1.393e-03	2.924e-03	3.956e-03	5.342e-03
C to Z	7.817e-04	1.581e-03	2.182e-03	2.970e-03
	X46_P16			
A (output stable)	1.926e-04			
B (output stable)	1.350e-03			
C (output stable)	1.981e-04			
A to Z	1.289e-02			
B to Z	9.813e-03			
C to Z	5.590e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	-2.111e-06	-4.894e-06	-6.063e-06	-6.669e-06
B (output stable)	-2.733e-05	-7.036e-05	-6.843e-05	-9.481e-05
C (output stable)	3.745e-05	1.011e-04	9.553e-05	1.302e-04
A to Z	-8.118e-06	-2.043e-05	-2.218e-05	-2.653e-05
B to Z	-7.721e-06	-1.987e-05	-1.888e-05	-2.629e-05
C to Z	-1.247e-08	-1.979e-07	-2.248e-07	-1.368e-07

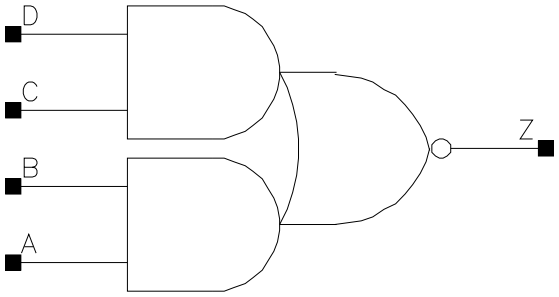
	X46_P16			
A (output stable)	-1.364e-05			
B (output stable)	-1.595e-04			
C (output stable)	2.149e-04			
A to Z	-5.112e-05			
B to Z	-4.561e-05			
C to Z	-5.500e-08			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P16	X10_P16	X16_P16	X21_P16
A	0.0008	0.0019	0.0028	0.0036
B	0.0008	0.0017	0.0026	0.0034
C	0.0007	0.0018	0.0026	0.0034
D	0.0007	0.0016	0.0024	0.0032
	X42_P16			
A	0.0071			
B	0.0067			
C	0.0068			
D	0.0063			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X10_P16**	**X4_P16**	**X10_P16**
A to Z ↓	0.0179	0.0177	4.8010	1.8841
A to Z ↑	0.0402	0.0349	12.2985	4.0308
B to Z ↓	0.0189	0.0188	4.8445	1.9031
B to Z ↑	0.0359	0.0318	12.2648	4.1166
C to Z ↓	0.0145	0.0138	4.9033	1.8898
C to Z ↑	0.0320	0.0282	12.1609	4.0043
D to Z ↓	0.0146	0.0138	4.9687	1.9195
D to Z ↑	0.0273	0.0241	12.1444	4.0584
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0192	0.0192	1.3654	1.0240
A to Z ↑	0.0364	0.0365	2.7108	2.0895
B to Z ↓	0.0198	0.0194	1.3779	1.0337
B to Z ↑	0.0320	0.0319	2.7120	2.0929
C to Z ↓	0.0150	0.0153	1.3601	1.0231
C to Z ↑	0.0292	0.0299	2.6811	2.0638
D to Z ↓	0.0144	0.0141	1.3814	1.0381
D to Z ↑	0.0241	0.0244	2.6882	2.0698
	X42_P16		**X42_P16**	
A to Z ↓	0.0200		0.5321	
A to Z ↑	0.0368		1.0460	
B to Z ↓	0.0200		0.5369	
B to Z ↑	0.0320		1.0433	
C to Z ↓	0.0159		0.5249	
C to Z ↑	0.0301		1.0352	
D to Z ↓	0.0148		0.5326	
D to Z ↑	0.0247		1.0345	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	9.992e-08	2.024e-12
X10_P16	2.643e-07	3.284e-12
X16_P16	3.865e-07	4.039e-12
X21_P16	5.179e-07	5.302e-12
X42_P16	1.025e-06	9.338e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	1.465e-05	3.943e-05	7.771e-05	1.080e-04
B (output stable)	1.745e-05	4.700e-05	1.108e-04	1.697e-04
C (output stable)	7.777e-06	2.034e-05	5.696e-05	8.321e-05
D (output stable)	3.369e-05	8.566e-05	2.421e-04	3.820e-04
A to Z	1.722e-03	4.214e-03	6.657e-03	8.755e-03
B to Z	1.498e-03	3.674e-03	5.604e-03	7.286e-03
C to Z	1.008e-03	2.453e-03	3.927e-03	5.331e-03
D to Z	7.771e-04	1.865e-03	2.780e-03	3.688e-03
	X42_P16			
A (output stable)	2.061e-04			
B (output stable)	3.008e-04			
C (output stable)	1.548e-04			
D (output stable)	6.780e-04			

A to Z	1.721e-02			
B to Z	1.441e-02			
C to Z	1.046e-02			
D to Z	7.370e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

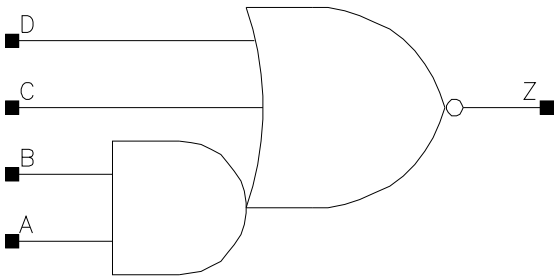
Pin Cycle (vdds)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	-1.010e-06	-2.563e-06	-3.563e-06	-4.063e-06
B (output stable)	-7.362e-07	-2.259e-06	-3.837e-06	-5.755e-06
C (output stable)	1.339e-07	1.733e-07	3.052e-07	3.279e-06
D (output stable)	7.800e-07	2.365e-06	3.780e-06	3.470e-06
A to Z	-9.453e-06	-1.934e-05	-2.832e-05	-3.841e-05
B to Z	-1.389e-05	-3.064e-05	-4.379e-05	-5.661e-05
C to Z	-5.440e-07	-1.625e-06	-2.616e-06	-1.136e-06
D to Z	-2.189e-07	-7.215e-07	-6.807e-07	-1.041e-06
	X42_P16			
A (output stable)	-7.878e-06			
B (output stable)	-1.052e-05			
C (output stable)	4.722e-06			
D (output stable)	7.993e-06			
A to Z	-6.927e-05			
B to Z	-1.058e-04			
C to Z	-6.078e-06			
D to Z	-2.207e-06			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X35_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P16	X35_P16
A	0.0008	0.0065
B	0.0009	0.0060
C	0.0009	0.0063
D	0.0009	0.0060

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X35_P16	X5_P16	X35_P16
A to Z ↓	0.0159	0.0166	4.0259	0.5944
A to Z ↑	0.0367	0.0348	13.5982	1.7243
B to Z ↓	0.0161	0.0161	4.0796	0.6027
B to Z ↑	0.0303	0.0275	13.5329	1.7231
C to Z ↓	0.0166	0.0205	2.3605	0.4528
C to Z ↑	0.0431	0.0424	12.8632	1.6326
D to Z ↓	0.0161	0.0193	2.3770	0.4514

D to Z ↑	0.0416	0.0398	12.8823	1.6350

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P16	1.262e-07	2.026e-12
X35_P16	8.179e-07	9.328e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P16	X35_P16
A (output stable)	3.267e-06	4.034e-05
B (output stable)	1.289e-05	1.620e-04
C (output stable)	2.397e-04	2.424e-03
D (output stable)	6.628e-07	3.490e-05
A to Z	1.356e-03	9.884e-03
B to Z	1.070e-03	7.056e-03
C to Z	2.216e-03	1.744e-02
D to Z	1.860e-03	1.372e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

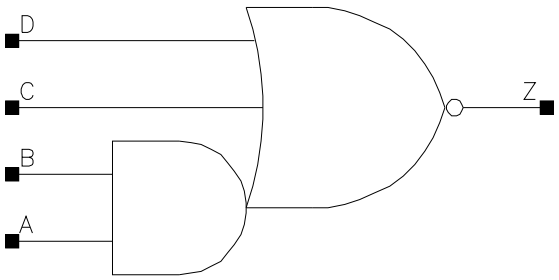
Pin Cycle (vdds)	X5_P16	X35_P16
A (output stable)	2.578e-06	2.244e-05
B (output stable)	1.001e-05	6.358e-05
C (output stable)	-4.079e-05	-3.181e-04
D (output stable)	8.786e-06	7.476e-05
A to Z	-7.423e-07	-7.019e-06
B to Z	-2.112e-07	-1.929e-06
C to Z	-1.473e-05	-1.028e-04
D to Z	-1.027e-05	-6.497e-05

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X17_P16	1.200	2.448	2.9376
X34_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P16	X17_P16	X34_P16
A	0.0009	0.0036	0.0073
B	0.0009	0.0034	0.0068
C	0.0008	0.0031	0.0061
D	0.0008	0.0028	0.0055

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X17_P16	X4_P16	X17_P16
A to Z ↓	0.0183	0.0198	4.3747	1.1608
A to Z ↑	0.0435	0.0456	13.6665	3.3579
B to Z ↓	0.0198	0.0202	4.4128	1.1702
B to Z ↑	0.0383	0.0390	13.5477	3.3621
C to Z ↓	0.0175	0.0172	3.7574	0.9195
C to Z ↑	0.0330	0.0347	12.8362	3.1667

D to Z ↓	0.0148	0.0136	3.8592	0.9257
D to Z ↑	0.0284	0.0263	12.8799	3.1795
	X34_P16		**X34_P16**	
A to Z ↓	0.0196		0.5953	
A to Z ↑	0.0450		1.7050	
B to Z ↓	0.0203		0.6002	
B to Z ↑	0.0385		1.7007	
C to Z ↓	0.0174		0.4861	
C to Z ↑	0.0339		1.6048	
D to Z ↓	0.0137		0.4916	
D to Z ↑	0.0258		1.6120	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	1.121e-07	2.024e-12
X17_P16	4.486e-07	5.298e-12
X34_P16	8.701e-07	9.324e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P16	X17_P16	X34_P16
A (output stable)	2.330e-05	1.044e-04	2.117e-04
B (output stable)	8.053e-05	3.836e-04	7.355e-04
C (output stable)	8.249e-05	5.896e-04	1.112e-03
D (output stable)	1.140e-06	6.786e-05	1.140e-04
A to Z	2.120e-03	9.171e-03	1.776e-02
B to Z	1.874e-03	7.742e-03	1.505e-02
C to Z	1.283e-03	5.547e-03	1.056e-02
D to Z	8.614e-04	3.168e-03	6.008e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

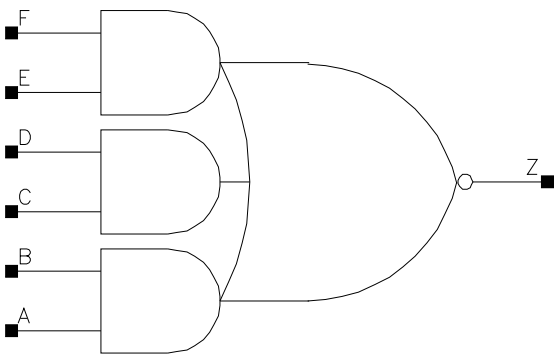
Pin Cycle (vdds)	X4_P16	X17_P16	X34_P16
A (output stable)	-3.121e-06	-8.337e-06	-1.729e-05
B (output stable)	-1.388e-05	-4.168e-05	-8.175e-05
C (output stable)	-9.799e-07	-5.823e-05	-9.451e-05
D (output stable)	8.862e-06	6.329e-05	1.091e-04
A to Z	-1.182e-05	-3.991e-05	-8.305e-05
B to Z	-1.383e-05	-5.240e-05	-9.855e-05
C to Z	-4.470e-06	-2.529e-05	-4.561e-05
D to Z	-4.540e-07	-1.118e-06	-2.204e-06

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X8_P16	1.200	2.176	2.6112
X13_P16	1.200	2.720	3.2640
X17_P16	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P16	X8_P16	X13_P16	X17_P16
A	0.0009	0.0018	0.0028	0.0036

B	0.0009	0.0017	0.0025	0.0033
C	0.0009	0.0017	0.0026	0.0033
D	0.0009	0.0016	0.0024	0.0032
E	0.0011	0.0017	0.0024	0.0032
F	0.0008	0.0016	0.0023	0.0030

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0205	0.0244	3.8800	2.2488
A to Z ↑	0.0599	0.0590	13.1063	6.0486
B to Z ↓	0.0224	0.0253	3.9085	2.2612
B to Z ↑	0.0547	0.0531	13.0975	6.0615
C to Z ↓	0.0193	0.0226	3.8370	2.2565
C to Z ↑	0.0534	0.0537	13.1278	6.0550
D to Z ↓	0.0208	0.0235	3.8764	2.2751
D to Z ↑	0.0480	0.0478	13.0832	6.0541
E to Z ↓	0.0153	0.0180	3.7562	2.2527
E to Z ↑	0.0402	0.0402	12.9717	5.9929
F to Z ↓	0.0157	0.0178	3.8167	2.2854
F to Z ↑	0.0345	0.0340	13.0553	6.0001
	X13_P16	**X17_P16**	**X13_P16**	**X17_P16**
A to Z ↓	0.0235	0.0237	1.5332	1.1693
A to Z ↑	0.0554	0.0556	4.0014	3.0513
B to Z ↓	0.0250	0.0246	1.5413	1.1757
B to Z ↑	0.0502	0.0496	4.0132	3.0520
C to Z ↓	0.0220	0.0220	1.5431	1.1546
C to Z ↑	0.0500	0.0503	4.0100	3.0622
D to Z ↓	0.0232	0.0224	1.5549	1.1642
D to Z ↑	0.0447	0.0444	4.0148	3.0578
E to Z ↓	0.0175	0.0175	1.5350	1.1549
E to Z ↑	0.0380	0.0381	3.9723	3.0229
F to Z ↓	0.0174	0.0166	1.5557	1.1707
F to Z ↑	0.0323	0.0318	3.9812	3.0359

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	1.897e-07	2.776e-12
X8_P16	3.621e-07	4.797e-12
X13_P16	5.252e-07	5.804e-12
X17_P16	7.012e-07	7.564e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

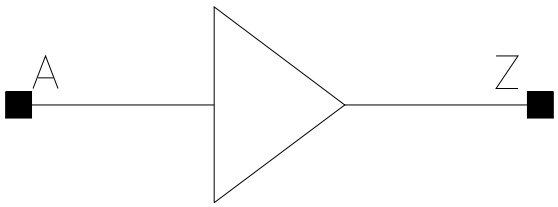
Pin Cycle (vdd)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	7.568e-05	1.751e-04	2.512e-04	3.289e-04
B (output stable)	3.020e-04	6.778e-04	9.054e-04	1.187e-03
C (output stable)	3.908e-05	9.231e-05	1.225e-04	1.638e-04
D (output stable)	5.179e-05	1.405e-04	1.703e-04	2.532e-04
E (output stable)	1.922e-05	5.636e-05	7.349e-05	9.794e-05
F (output stable)	2.733e-05	9.770e-05	1.211e-04	1.928e-04

A to Z	3.324e-03	7.023e-03	9.790e-03	1.291e-02
B to Z	3.046e-03	6.276e-03	8.827e-03	1.146e-02
C to Z	2.535e-03	5.534e-03	7.507e-03	9.945e-03
D to Z	2.237e-03	4.801e-03	6.530e-03	8.482e-03
E to Z	1.578e-03	3.577e-03	4.834e-03	6.376e-03
F to Z	1.297e-03	2.855e-03	3.843e-03	4.904e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	-1.116e-05	-2.522e-05	-2.937e-05	-3.830e-05
B (output stable)	-4.920e-05	-1.013e-04	-1.144e-04	-1.519e-04
C (output stable)	-4.107e-06	-1.018e-05	-9.948e-06	-1.302e-05
D (output stable)	1.962e-06	-2.678e-06	-1.974e-06	-6.503e-06
E (output stable)	2.589e-05	6.089e-05	6.698e-05	9.279e-05
F (output stable)	2.152e-05	4.554e-05	5.157e-05	6.834e-05
A to Z	-2.336e-05	-4.757e-05	-5.377e-05	-7.142e-05
B to Z	-2.536e-05	-5.017e-05	-5.560e-05	-7.567e-05
C to Z	-1.700e-05	-3.656e-05	-4.046e-05	-5.316e-05
D to Z	-1.161e-05	-2.837e-05	-3.040e-05	-4.245e-05
E to Z	-8.167e-07	-2.228e-06	-3.081e-06	-1.726e-06
F to Z	-5.879e-07	-1.404e-06	-1.796e-06	-1.427e-06

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.408	0.4896
X6_P16	1.200	0.408	0.4896
X8_P16	1.200	0.408	0.4896
X13_P16	1.200	0.544	0.6528
X16_P16	1.200	0.544	0.6528
X21_P16	1.200	0.680	0.8160
X25_P16	1.200	0.680	0.8160
X29_P16	1.200	0.952	1.1424
X33_P16	1.200	0.952	1.1424
X42_P16	1.200	1.088	1.3056
X50_P16	1.200	1.224	1.4688
X58_P16	1.200	1.496	1.7952
X67_P16	1.200	1.632	1.9584
X75_P16	1.200	1.768	2.1216
X84_P16	1.200	1.904	2.2848
X100_P16	1.200	2.312	2.7744
X134_P16	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0009	0.0009	0.0009	0.0009
	X16_P16	X21_P16	X25_P16	X29_P16
A	0.0008	0.0012	0.0012	0.0016
	X33_P16	X42_P16	X50_P16	X58_P16
A	0.0016	0.0019	0.0022	0.0032

	X67_P16	X75_P16	X84_P16	X100_P16
A	0.0032	0.0032	0.0032	0.0042
	X134_P16			
A	0.0053			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0371	0.0374	3.9565	2.8904
A to Z ↑	0.0273	0.0270	8.1148	5.9188
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0390	0.0441	2.1404	1.3877
A to Z ↑	0.0278	0.0311	4.2112	2.7561
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0474	0.0396	1.1063	0.8533
A to Z ↑	0.0328	0.0284	2.1065	1.6544
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0413	0.0397	0.7353	0.6218
A to Z ↑	0.0293	0.0276	1.3868	1.1815
	X33_P16	**X42_P16**	**X33_P16**	**X42_P16**
A to Z ↓	0.0416	0.0406	0.5506	0.4482
A to Z ↑	0.0288	0.0289	1.0361	0.8333
	X50_P16	**X58_P16**	**X50_P16**	**X58_P16**
A to Z ↓	0.0398	0.0370	0.3720	0.3206
A to Z ↑	0.0283	0.0267	0.6921	0.5947
	X67_P16	**X75_P16**	**X67_P16**	**X75_P16**
A to Z ↓	0.0389	0.0408	0.2818	0.2549
A to Z ↑	0.0279	0.0292	0.5208	0.4663
	X84_P16	**X100_P16**	**X84_P16**	**X100_P16**
A to Z ↓	0.0425	0.0400	0.2311	0.1944
A to Z ↑	0.0303	0.0288	0.4207	0.3521
	X134_P16		**X134_P16**	
A to Z ↓	0.0417		0.1517	
A to Z ↑	0.0303		0.2692	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	4.943e-08	1.520e-12
X6_P16	5.846e-08	1.518e-12
X8_P16	7.024e-08	1.519e-12
X13_P16	9.392e-08	1.770e-12
X16_P16	1.121e-07	1.775e-12
X21_P16	1.555e-07	2.004e-12
X25_P16	1.747e-07	2.023e-12
X29_P16	2.108e-07	2.528e-12
X33_P16	2.301e-07	2.527e-12
X42_P16	2.843e-07	2.778e-12
X50_P16	3.412e-07	3.029e-12
X58_P16	4.245e-07	3.533e-12
X67_P16	4.662e-07	3.783e-12
X75_P16	5.078e-07	4.035e-12

X84_P16	5.494e-07	4.292e-12
X100_P16	6.744e-07	5.046e-12
X134_P16	8.826e-07	6.314e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	1.698e-03	1.893e-03	2.235e-03	2.938e-03
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	3.463e-03	4.769e-03	5.261e-03	5.937e-03
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	6.531e-03	8.259e-03	9.683e-03	1.186e-02
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	1.318e-02	1.469e-02	1.598e-02	1.914e-02
	X134_P16			
A to Z	2.557e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

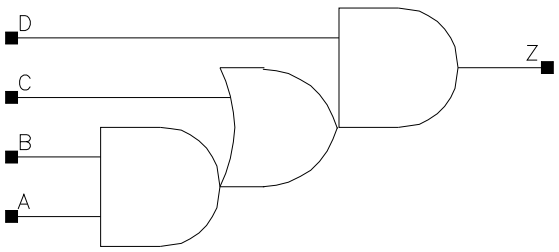
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	-3.749e-07	-9.950e-08	-2.847e-07	-2.777e-07
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	-2.151e-07	-1.225e-06	-8.502e-07	-3.811e-07
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	-5.842e-07	-6.510e-07	-5.402e-07	-1.328e-06
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	-7.901e-07	-1.464e-06	-1.774e-06	-1.692e-06
	X134_P16			
A to Z	-2.348e-06			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.632	1.9584
X25_P16	1.200	1.768	2.1216
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0010	0.0022	0.0022	0.0021
B	0.0011	0.0020	0.0020	0.0019
C	0.0011	0.0024	0.0023	0.0023
D	0.0016	0.0021	0.0021	0.0021

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0535	0.0507	2.1938	1.0909
A to Z ↑	0.0416	0.0392	4.2514	2.0677
B to Z ↓	0.0494	0.0462	2.1893	1.0908
B to Z ↑	0.0417	0.0385	4.2546	2.0666
C to Z ↓	0.0445	0.0411	2.1843	1.0876
C to Z ↑	0.0318	0.0290	4.2235	2.0547

D to Z ↓	0.0415	0.0369	2.1557	1.0738
D to Z ↑	0.0367	0.0321	4.2249	2.0553
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0560	0.0596	0.7455	0.5636
A to Z ↑	0.0432	0.0455	1.3995	1.0505
B to Z ↓	0.0516	0.0559	0.7454	0.5635
B to Z ↑	0.0427	0.0456	1.3999	1.0517
C to Z ↓	0.0464	0.0505	0.7427	0.5607
C to Z ↑	0.0323	0.0346	1.3883	1.0411
D to Z ↓	0.0400	0.0421	0.7305	0.5490
D to Z ↑	0.0352	0.0370	1.3906	1.0429

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.628e-07	2.529e-12
X17_P16	3.216e-07	3.787e-12
X25_P16	3.676e-07	4.041e-12
X33_P16	4.136e-07	4.299e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	2.212e-05	5.516e-05	5.581e-05	5.568e-05
B (output stable)	6.496e-05	1.020e-04	1.013e-04	1.039e-04
C (output stable)	3.076e-04	5.236e-04	5.269e-04	4.984e-04
D (output stable)	5.396e-05	6.892e-05	6.457e-05	7.047e-05
A to Z	3.753e-03	6.817e-03	8.441e-03	9.593e-03
B to Z	3.459e-03	6.075e-03	7.696e-03	8.948e-03
C to Z	2.871e-03	4.857e-03	6.490e-03	7.739e-03
D to Z	3.864e-03	6.552e-03	8.180e-03	9.352e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

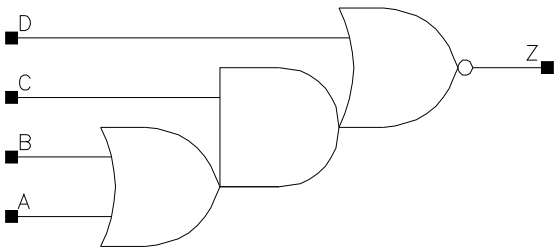
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	-2.124e-06	-4.217e-06	-4.301e-06	-4.349e-06
B (output stable)	-2.885e-06	-4.500e-06	-4.367e-06	-4.413e-06
C (output stable)	-3.127e-06	-5.784e-06	-5.845e-06	-5.200e-06
D (output stable)	3.591e-06	5.183e-06	5.151e-06	4.017e-06
A to Z	-8.602e-06	-1.580e-05	-1.618e-05	-1.562e-05
B to Z	-8.118e-06	-1.481e-05	-1.558e-05	-1.621e-05
C to Z	-4.210e-07	-7.254e-07	-9.776e-07	-8.522e-07
D to Z	-2.384e-06	-3.943e-06	-4.032e-06	-4.221e-06

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.952	1.1424
X11_P16	1.200	1.496	1.7952
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X16_P16	X21_P16
A	0.0010	0.0018	0.0027	0.0036
B	0.0010	0.0017	0.0027	0.0035
C	0.0009	0.0017	0.0026	0.0035
D	0.0012	0.0017	0.0026	0.0034

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0192	0.0186	3.7835	1.9973
A to Z ↑	0.0515	0.0483	13.3703	6.9285
B to Z ↓	0.0188	0.0184	3.6825	1.9592
B to Z ↑	0.0490	0.0464	13.3770	6.9319
C to Z ↓	0.0176	0.0169	3.4804	1.8408
C to Z ↑	0.0316	0.0294	8.7724	4.4964

D to Z ↓	0.0118	0.0103	2.1727	1.1029
D to Z ↑	0.0276	0.0242	9.4350	4.8444
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0185	0.0188	1.3554	1.0419
A to Z ↑	0.0455	0.0476	4.4689	3.4339
B to Z ↓	0.0180	0.0184	1.3605	1.0415
B to Z ↑	0.0446	0.0455	4.4761	3.4365
C to Z ↓	0.0172	0.0172	1.2708	0.9717
C to Z ↑	0.0289	0.0291	2.9718	2.2285
D to Z ↓	0.0104	0.0104	0.7749	0.5920
D to Z ↑	0.0230	0.0229	3.1796	2.4022

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P16	1.492e-07	2.528e-12
X11_P16	2.914e-07	3.539e-12
X16_P16	4.175e-07	4.043e-12
X21_P16	5.614e-07	5.302e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	2.980e-05	5.816e-05	7.735e-05	1.216e-04
B (output stable)	5.477e-05	1.172e-04	1.659e-04	2.293e-04
C (output stable)	2.623e-04	5.154e-04	7.129e-04	1.022e-03
D (output stable)	3.012e-05	6.181e-05	6.996e-05	1.284e-04
A to Z	2.682e-03	4.709e-03	6.629e-03	9.313e-03
B to Z	2.198e-03	3.883e-03	5.638e-03	7.609e-03
C to Z	1.798e-03	3.070e-03	4.458e-03	6.130e-03
D to Z	9.947e-04	1.621e-03	2.174e-03	2.892e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

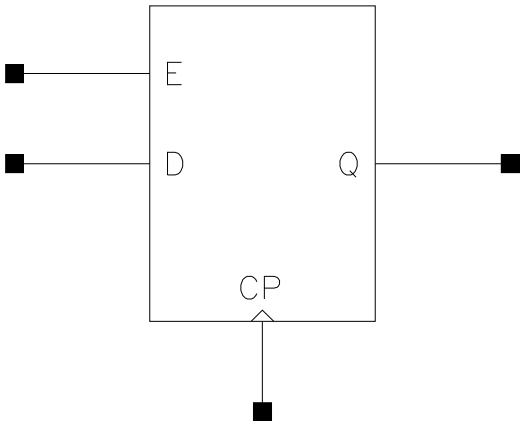
Pin Cycle (vdds)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	-4.848e-06	-7.398e-06	-1.069e-05	-1.664e-05
B (output stable)	-3.659e-06	-1.022e-05	-9.373e-06	-1.344e-05
C (output stable)	-3.002e-05	-5.563e-05	-7.794e-05	-1.157e-04
D (output stable)	3.856e-05	8.263e-05	1.051e-04	1.551e-04
A to Z	-1.304e-05	-2.175e-05	-3.269e-05	-4.854e-05
B to Z	-8.163e-06	-1.939e-05	-2.648e-05	-3.434e-05
C to Z	-1.019e-05	-1.931e-05	-2.531e-05	-3.695e-05
D to Z	-3.122e-08	-3.934e-07	-8.842e-08	-3.161e-07

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.128	3.7536
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0012	0.0012	0.0011

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0599	0.0700	2.2112	1.1538
CP to Q ↑	0.0696	0.0741	4.2733	2.1367
	X33_P16		**X33_P16**	
CP to Q ↓	0.1004		0.5608	
CP to Q ↑	0.1202		1.0587	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0892	0.0892	0.0892
CP ↑	min_pulse_width to CP	0.0452	0.0586	0.0416
D ↓	hold_rising to CP	-0.0435	-0.0435	-0.0432
D ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.0974	0.0974	0.0974
D ↑	setup_rising to CP	0.0438	0.0438	0.0438
E ↓	hold_rising to CP	-0.0334	-0.0334	-0.0334
E ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
E ↓	setup_rising to CP	0.0819	0.0819	0.0819
E ↑	setup_rising to CP	0.1029	0.1029	0.1029

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	3.719e-07	6.308e-12
X17_P16	4.151e-07	6.560e-12
X33_P16	5.507e-07	7.569e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

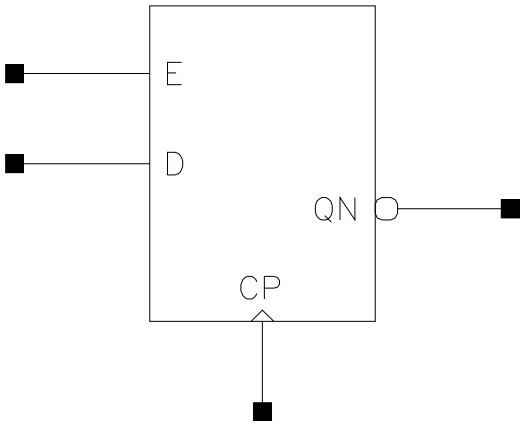
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.090e-03	4.091e-03	4.097e-03
Clock 100Mhz Data 25Mhz	8.717e-03	9.294e-03	1.214e-02
Clock 100Mhz Data 50Mhz	1.334e-02	1.450e-02	2.019e-02
Clock = 0 Data 100Mhz	5.223e-03	5.224e-03	5.225e-03
Clock = 1 Data 100Mhz	1.418e-03	1.418e-03	1.418e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.264	3.9168
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0012	0.0012	0.0012

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.0998	0.0928	2.2578	1.0771
CP to QN ↑	0.0771	0.0807	4.3141	2.0725
	X33_P16		**X33_P16**	
CP to QN ↓	0.0992		0.5636	
CP to QN ↑	0.0901		1.0618	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0892	0.0892	0.0892
CP ↑	min_pulse_width to CP	0.0416	0.0452	0.0501
D ↓	hold_rising to CP	-0.0432	-0.0435	-0.0435
D ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.0974	0.0974	0.0974
D ↑	setup_rising to CP	0.0438	0.0438	0.0438
E ↓	hold_rising to CP	-0.0334	-0.0334	-0.0334
E ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
E ↓	setup_rising to CP	0.0819	0.0819	0.0819
E ↑	setup_rising to CP	0.1029	0.1029	0.1029

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	3.692e-07	6.311e-12
X17_P16	4.350e-07	6.812e-12
X33_P16	5.411e-07	7.569e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

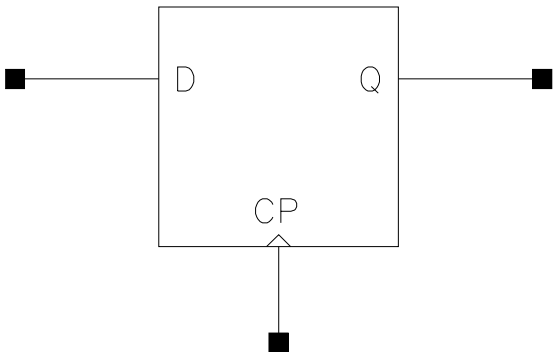
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.092e-03	4.094e-03	4.095e-03
Clock 100Mhz Data 25Mhz	8.786e-03	1.001e-02	1.187e-02
Clock 100Mhz Data 50Mhz	1.348e-02	1.593e-02	1.965e-02
Clock = 0 Data 100Mhz	5.250e-03	5.250e-03	5.251e-03
Clock = 1 Data 100Mhz	1.418e-03	1.418e-03	1.418e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.176	2.6112
X17_P16	1.200	2.448	2.9376
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0623	0.0694	2.2087	1.1433
CP to Q ↑	0.0704	0.0779	4.1398	2.1015
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to Q ↓	0.0891	0.0927	0.6927	0.6297
CP to Q ↑	0.0875	0.0891	1.1843	1.0779

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0757	0.0806	0.0806	0.0806
CP ↑	min_pulse_width to CP	0.0452	0.0549	0.0780	0.0829
D ↓	hold_rising to CP	-0.0020	-0.0045	-0.0020	-0.0020
D ↑	hold_rising to CP	0.0056	0.0056	0.0056	0.0056
D ↓	setup_rising to CP	0.0539	0.0562	0.0562	0.0562
D ↑	setup_rising to CP	0.0219	0.0219	0.0219	0.0219

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	2.895e-07	4.797e-12
X17_P16	3.359e-07	5.298e-12
X30_P16	4.039e-07	5.804e-12
X33_P16	4.199e-07	5.803e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

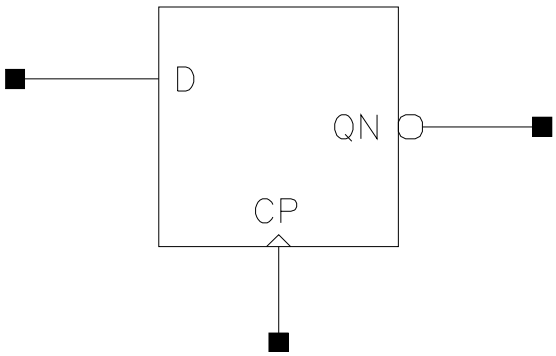
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.301e-03	4.328e-03	4.336e-03	4.340e-03
Clock 100Mhz Data 25Mhz	7.755e-03	8.721e-03	9.931e-03	1.016e-02
Clock 100Mhz Data 50Mhz	1.121e-02	1.311e-02	1.553e-02	1.598e-02
Clock = 0 Data 100Mhz	3.595e-03	3.713e-03	3.749e-03	3.768e-03
Clock = 1 Data 100Mhz	3.729e-05	3.732e-05	3.734e-05	3.739e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.0601	0.0730	2.2838	1.1897
CP to QN ↑	0.0628	0.0665	4.1319	2.0984
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to QN ↓	0.0997	0.0996	0.6201	0.5617
CP to QN ↑	0.0828	0.0971	1.1449	1.0596

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0671	0.0671	0.0806	0.0757
CP ↑	min_pulse_width to CP	0.0452	0.0586	0.0453	0.0549
D ↓	hold_rising to CP	0.0078	0.0078	-0.0045	-0.0020
D ↑	hold_rising to CP	0.0078	0.0078	0.0056	0.0056
D ↓	setup_rising to CP	0.0336	0.0367	0.0562	0.0539
D ↑	setup_rising to CP	0.0267	0.0271	0.0219	0.0219

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	2.604e-07	4.292e-12
X17_P16	3.039e-07	4.545e-12
X30_P16	4.325e-07	5.804e-12
X33_P16	4.605e-07	6.056e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

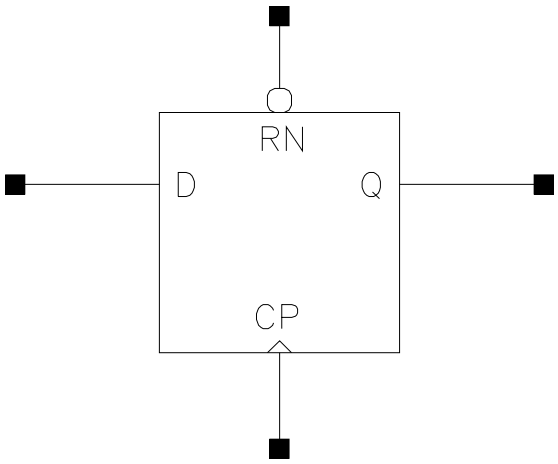
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.162e-03	4.162e-03	4.236e-03	4.266e-03
Clock 100Mhz Data 25Mhz	7.342e-03	7.968e-03	1.047e-02	1.087e-02
Clock 100Mhz Data 50Mhz	1.052e-02	1.177e-02	1.671e-02	1.748e-02
Clock = 0 Data 100Mhz	3.111e-03	3.111e-03	3.353e-03	3.417e-03
Clock = 1 Data 100Mhz	3.696e-05	3.701e-05	3.714e-05	3.725e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0008	0.0008
RN	0.0010	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0725	0.0918	1.1560	0.7044
CP to Q ↑	0.0802	0.0895	2.1066	1.1883
RN to Q ↓	0.1153	0.1529	1.2628	0.7780

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0843	0.0854
CP ↑	min_pulse_width to CP	0.0597	0.0780
D ↓	hold_rising to CP	-0.0045	-0.0045
D ↑	hold_rising to CP	0.0029	0.0029
D ↓	setup_rising to CP	0.0584	0.0584
D ↑	setup_rising to CP	0.0323	0.0323
RN ↓	min_pulse_width to RN	0.1480	0.1919
RN ↑	recovery_rising to CP	0.0292	0.0292
RN ↑	removal_rising to CP	-0.0149	-0.0149

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P16	3.991e-07	6.560e-12
X30_P16	4.729e-07	7.064e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

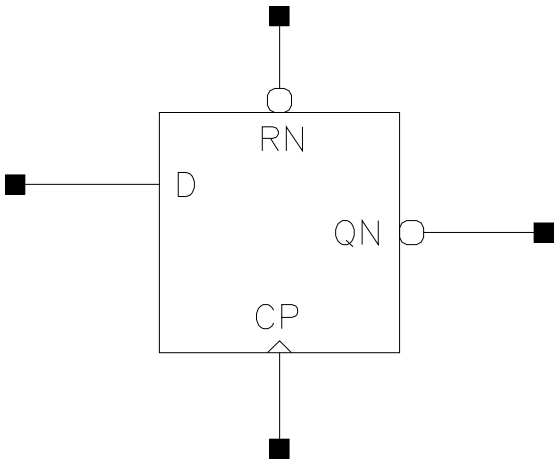
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	4.646e-03	4.645e-03
Clock 100Mhz Data 25Mhz	9.321e-03	1.050e-02
Clock 100Mhz Data 50Mhz	1.400e-02	1.635e-02
Clock = 0 Data 100Mhz	4.380e-03	4.383e-03
Clock = 1 Data 100Mhz	3.826e-05	3.850e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0008	0.0008
RN	0.0010	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.0948	0.1027	1.0641	0.6217
CP to QN ↑	0.0807	0.0863	2.0610	1.1496
RN to QN ↑	0.1212	0.1283	2.0682	1.1533

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0854	0.0854
CP ↑	min_pulse_width to CP	0.0463	0.0501
D ↓	hold_rising to CP	-0.0045	-0.0045
D ↑	hold_rising to CP	0.0029	0.0029
D ↓	setup_rising to CP	0.0584	0.0584
D ↑	setup_rising to CP	0.0323	0.0292
RN ↓	min_pulse_width to RN	0.1182	0.1182
RN ↑	recovery_rising to CP	0.0296	0.0296
RN ↑	removal_rising to CP	-0.0149	-0.0149

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P16	4.129e-07	6.561e-12
X30_P16	4.747e-07	7.064e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

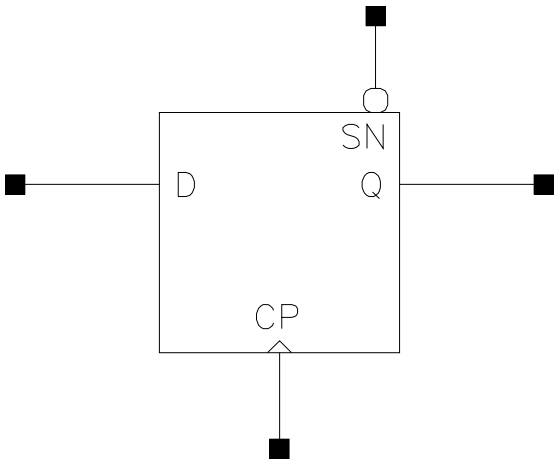
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	4.654e-03	4.653e-03
Clock 100Mhz Data 25Mhz	1.000e-02	1.123e-02
Clock 100Mhz Data 50Mhz	1.535e-02	1.780e-02
Clock = 0 Data 100Mhz	4.445e-03	4.428e-03
Clock = 1 Data 100Mhz	5.249e-05	5.258e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0008	0.0008
SN	0.0013	0.0013

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0726	0.0928	1.1578	0.7008
CP to Q ↑	0.0795	0.0893	2.1079	1.1886
SN to Q ↑	0.0811	0.0930	2.1166	1.1934

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0891	0.0891
CP ↑	min_pulse_width to CP	0.0597	0.0780
D ↓	hold_rising to CP	-0.0045	-0.0045
D ↑	hold_rising to CP	0.0025	0.0056
D ↓	setup_rising to CP	0.0633	0.0636
D ↑	setup_rising to CP	0.0274	0.0274
SN ↓	min_pulse_width to SN	0.0789	0.0891
SN ↑	recovery_rising to CP	0.0177	0.0177
SN ↑	removal_rising to CP	0.0359	0.0359

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P16	3.994e-07	6.560e-12
X30_P16	4.609e-07	7.064e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

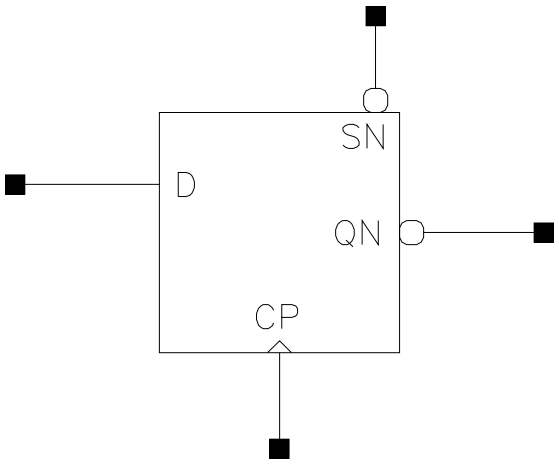
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	4.687e-03	4.677e-03
Clock 100Mhz Data 25Mhz	9.372e-03	1.056e-02
Clock 100Mhz Data 50Mhz	1.406e-02	1.644e-02
Clock = 0 Data 100Mhz	4.367e-03	4.367e-03
Clock = 1 Data 100Mhz	3.694e-05	3.704e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0008	0.0008
SN	0.0013	0.0013

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.0940	0.1020	1.0675	0.6232
CP to QN ↑	0.0812	0.0866	2.0587	1.1476
SN to QN ↓	0.0953	0.1036	1.0674	0.6231

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0891	0.0891
CP ↑	min_pulse_width to CP	0.0463	0.0501
D ↓	hold_rising to CP	-0.0045	-0.0045
D ↑	hold_rising to CP	0.0025	0.0025
D ↓	setup_rising to CP	0.0633	0.0633
D ↑	setup_rising to CP	0.0274	0.0274
SN ↓	min_pulse_width to SN	0.0686	0.0713
SN ↑	recovery_rising to CP	0.0177	0.0177
SN ↑	removal_rising to CP	0.0359	0.0359

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P16	4.412e-07	6.560e-12
X30_P16	5.153e-07	7.064e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

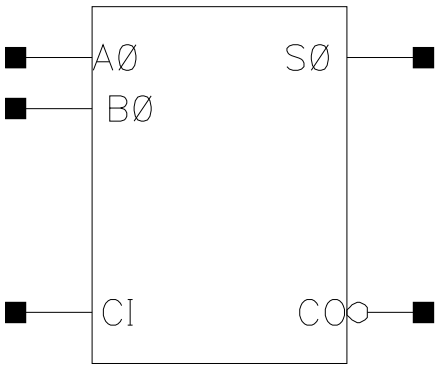
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	4.698e-03	4.698e-03
Clock 100Mhz Data 25Mhz	1.002e-02	1.125e-02
Clock 100Mhz Data 50Mhz	1.535e-02	1.781e-02
Clock = 0 Data 100Mhz	4.367e-03	4.367e-03
Clock = 1 Data 100Mhz	3.738e-05	3.753e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_-P16	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_-P16	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_-P16	1.200	3.672	4.4064
C12T28SOI_LRS1_-FA1X33_P16	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16
A0	0.0035	0.0072	0.0031	0.0061
B0	0.0032	0.0068	0.0034	0.0059
CI	0.0024	0.0053	0.0024	0.0042

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P16	**C12T28SOI_LR_-FA1X33_P16**	**C12T28SOI_LR_-FA1X8_P16**	**C12T28SOI_LR_-FA1X33_P16**
A0 to CO ↓	0.0717	0.0782	2.2976	0.6137
A0 to CO ↑	0.0448	0.0463	4.2624	1.0967
A0 to S0 ↓	0.0700	0.0885	2.2503	0.5961
A0 to S0 ↑	0.0715	0.0865	4.2166	1.0759
B0 to CO ↓	0.0699	0.0779	2.3111	0.6189
B0 to CO ↑	0.0461	0.0482	4.2651	1.0920
B0 to S0 ↓	0.0699	0.0892	2.2490	0.5956
B0 to S0 ↑	0.0710	0.0871	4.2197	1.0765
CI to CO ↓	0.0666	0.0748	2.3206	0.6193
CI to CO ↑	0.0455	0.0469	4.2643	1.0972
CI to S0 ↓	0.0691	0.0883	2.2488	0.5956
CI to S0 ↑	0.0702	0.0866	4.2178	1.0761
	C12T28SOI_LRS1_-FA1X8_P16	**C12T28SOI_LRS1_-FA1X33_P16**	**C12T28SOI_LRS1_-FA1X8_P16**	**C12T28SOI_LRS1_-FA1X33_P16**
A0 to CO ↓	0.0446	0.0556	4.5241	0.7869
A0 to CO ↑	0.0341	0.0393	4.3174	1.0830
A0 to S0 ↓	0.0918	0.1127	2.4255	0.6217
A0 to S0 ↑	0.0816	0.0885	4.3981	1.0992
B0 to CO ↓	0.0451	0.0563	4.5258	0.7895
B0 to CO ↑	0.0322	0.0381	4.3142	1.0830
B0 to S0 ↓	0.0921	0.1150	2.4245	0.6213
B0 to S0 ↑	0.0820	0.0909	4.3991	1.0992
CI to CO ↓	0.0429	0.0746	4.5152	0.8008
CI to CO ↑	0.0354	0.0424	4.4260	1.0913
CI to S0 ↓	0.0529	0.0692	2.4272	0.6230
CI to S0 ↑	0.0433	0.0436	4.3968	1.0993

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_FA1X8_P16	4.332e-07	4.794e-12
C12T28SOI_LR_FA1X33_P16	1.033e-06	9.833e-12
C12T28SOI_LRS1_FA1X8_P16	5.359e-07	7.570e-12
C12T28SOI_LRS1_FA1X33_P16	1.402e-06	1.563e-11

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16
A0 to CO	4.014e-03	1.069e-02	6.008e-03	1.462e-02
A0 to S0	4.010e-03	1.100e-02	8.060e-03	1.814e-02
B0 to CO	3.945e-03	1.064e-02	6.066e-03	1.485e-02
B0 to S0	3.770e-03	1.062e-02	8.162e-03	1.846e-02
CI to CO	3.897e-03	1.055e-02	4.233e-03	1.279e-02
CI to S0	3.746e-03	1.060e-02	4.802e-03	1.385e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P16	C12T28SOI_LR_-FA1X33_P16	C12T28SOI_LRS1_-FA1X8_P16	C12T28SOI_LRS1_-FA1X33_P16
A0 to CO	-2.605e-05	-5.105e-05	2.989e-06	7.157e-06
A0 to S0	-1.973e-05	-3.909e-05	5.198e-06	1.088e-05
B0 to CO	-1.151e-05	-2.162e-05	-9.005e-06	-1.916e-05
B0 to S0	8.034e-07	5.530e-07	-1.243e-05	-2.572e-05
CI to CO	9.860e-06	1.846e-05	-1.450e-06	-2.409e-06
CI to S0	1.414e-06	4.011e-07	-1.398e-06	8.994e-07

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X33_P16	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X33_P16
A0	0.0012	0.0035
B0	0.0011	0.0031

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
A0 to CO ↓	0.0504	0.0462	2.2439	0.5567
A0 to CO ↑	0.0426	0.0381	4.2239	1.0854
A0 to S0 ↓	0.0654	0.0619	2.1931	0.5572
A0 to S0 ↑	0.0594	0.0646	4.1740	1.0707
B0 to CO ↓	0.0491	0.0429	2.2467	0.5524
B0 to CO ↑	0.0448	0.0390	4.2239	1.0856
B0 to S0 ↓	0.0663	0.0604	2.1933	0.5577
B0 to S0 ↑	0.0587	0.0621	4.1728	1.0714

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.832e-07	3.032e-12
X33_P16	6.573e-07	6.307e-12

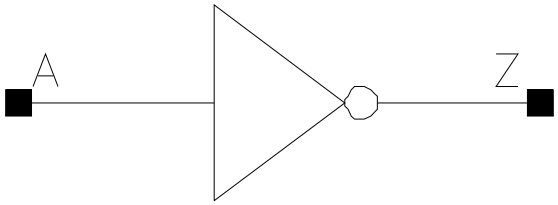
Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X33_P16
A0 to CO	3.088e-03	1.000e-02
A0 to S0	2.790e-03	9.419e-03
B0 to CO	3.064e-03	9.635e-03
B0 to S0	2.702e-03	8.821e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X8_P16	X33_P16
A0 to CO	-7.580e-06	-4.685e-05
A0 to S0	-4.910e-06	-2.898e-05
B0 to CO	5.766e-06	3.684e-05
B0 to S0	2.718e-06	1.789e-05

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.272	0.3264
X6_P16	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X13_P16	1.200	0.408	0.4896
X17_P16	1.200	0.408	0.4896
X21_P16	1.200	0.544	0.6528
X25_P16	1.200	0.544	0.6528
X29_P16	1.200	0.680	0.8160
X33_P16	1.200	0.680	0.8160
X50_P16	1.200	0.952	1.1424
X58_P16	1.200	1.088	1.3056
X67_P16	1.200	1.224	1.4688
X75_P16	1.200	1.360	1.6320
X84_P16	1.200	1.496	1.7952
X100_P16	1.200	1.768	2.1216
X134_P16	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0006	0.0007	0.0009	0.0014
	X17_P16	X21_P16	X25_P16	X29_P16
A	0.0017	0.0023	0.0026	0.0031
	X33_P16	X50_P16	X58_P16	X67_P16
A	0.0034	0.0051	0.0060	0.0069
	X75_P16	X84_P16	X100_P16	X134_P16

A	0.0078	0.0088	0.0107	0.0149

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0113	0.0106	4.1191	3.1810
A to Z ↑	0.0197	0.0184	8.2411	6.1806
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0096	0.0086	2.1679	1.4068
A to Z ↑	0.0168	0.0156	4.2528	2.8114
	X17_P16	**X21_P16**	**X17_P16**	**X21_P16**
A to Z ↓	0.0083	0.0090	1.0781	0.8703
A to Z ↑	0.0149	0.0158	2.0894	1.6854
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0088	0.0084	0.7420	0.6307
A to Z ↑	0.0153	0.0149	1.4068	1.2036
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0084	0.0086	0.5579	0.3779
A to Z ↑	0.0146	0.0148	1.0533	0.7042
	X58_P16	**X67_P16**	**X58_P16**	**X67_P16**
A to Z ↓	0.0088	0.0088	0.3283	0.2882
A to Z ↑	0.0150	0.0148	0.6077	0.5321
	X75_P16	**X84_P16**	**X75_P16**	**X84_P16**
A to Z ↓	0.0092	0.0093	0.2603	0.2353
A to Z ↑	0.0152	0.0153	0.4763	0.4301
	X100_P16	**X134_P16**	**X100_P16**	**X134_P16**
A to Z ↓	0.0100	0.0107	0.2002	0.1560
A to Z ↑	0.0158	0.0164	0.3616	0.2773

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	2.524e-08	1.267e-12
X6_P16	3.171e-08	1.267e-12
X8_P16	4.517e-08	1.258e-12
X13_P16	7.008e-08	1.521e-12
X17_P16	9.071e-08	1.521e-12
X21_P16	1.129e-07	1.772e-12
X25_P16	1.330e-07	1.772e-12
X29_P16	1.551e-07	2.025e-12
X33_P16	1.747e-07	2.025e-12
X50_P16	2.580e-07	2.463e-12
X58_P16	2.996e-07	2.779e-12
X67_P16	3.413e-07	3.029e-12
X75_P16	3.829e-07	3.282e-12
X84_P16	4.246e-07	3.538e-12
X100_P16	5.078e-07	4.027e-12
X134_P16	6.744e-07	5.045e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16

A to Z	4.128e-04	4.801e-04	5.722e-04	7.239e-04
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	8.792e-04	1.291e-03	1.446e-03	1.535e-03
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	1.677e-03	2.516e-03	3.116e-03	3.333e-03
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	3.866e-03	4.155e-03	4.973e-03	6.625e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

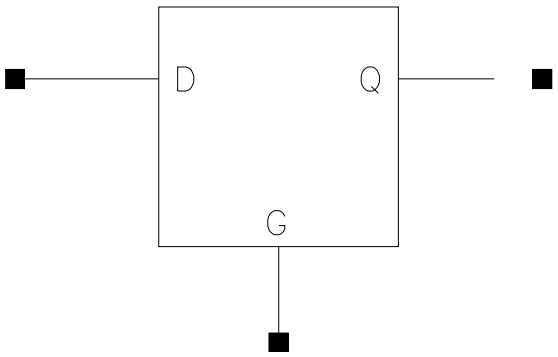
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	-3.630e-08	-2.280e-08	1.179e-07	7.687e-07
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	1.573e-06	8.490e-07	2.608e-06	2.065e-06
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	2.776e-06	-1.015e-06	-1.052e-06	-7.700e-08
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	1.600e-08	4.340e-07	-9.900e-08	4.640e-07

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X23_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P16	X23_P16
D	0.0006	0.0014
G	0.0013	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X23_P16	X8_P16	X23_P16
D to Q ↓	0.0812	0.0636	2.3566	1.0858
D to Q ↑	0.0449	0.0451	4.1595	1.0982
G to Q ↓	0.0833	0.0627	2.3520	1.0837
G to Q ↑	0.0438	0.0409	4.1602	1.1005

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P16	X23_P16
D ↓	hold_falling to G	-0.0335	-0.0184
D ↑	hold_falling to G	-0.0070	-0.0096
D ↓	setup_falling to G	0.0835	0.0584
D ↑	setup_falling to G	0.0471	0.0520
G ↑	min_pulse_width to G	0.0685	0.0532

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.512e-07	3.033e-12
X23_P16	2.854e-07	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X23_P16
D (output stable)	1.573e-05	6.868e-05
G (output stable)	9.802e-04	1.887e-03
D to Q	4.594e-03	8.884e-03
G to Q	4.165e-03	7.687e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

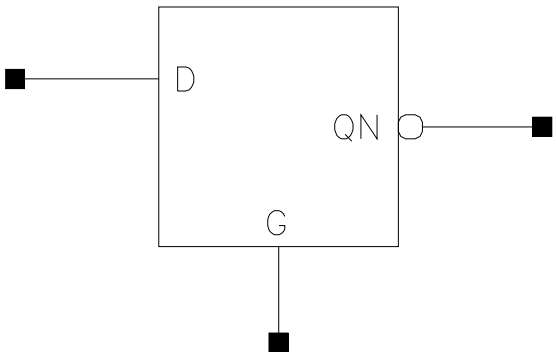
Pin Cycle (vdds)	X8_P16	X23_P16
D (output stable)	-1.884e-06	-6.018e-06
G (output stable)	2.370e-08	-3.385e-07
D to Q	-4.010e-06	-8.843e-06
G to Q	2.692e-05	2.056e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P16
D	0.0006
G	0.0015

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P16	X17_P16
D to QN ↓	0.0618	1.0728
D to QN ↑	0.0871	2.0491
G to QN ↓	0.0601	1.0731
G to QN ↑	0.0861	2.0484

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P16
D ↓	hold_falling to G	-0.0387
D ↑	hold_falling to G	-0.0125
D ↓	setup_falling to G	0.0685
D ↑	setup_falling to G	0.0430
G ↑	min_pulse_width to G	0.0537

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P16	2.126e-07	3.284e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X17_P16
D (output stable)	3.403e-05
G (output stable)	1.056e-03
D to QN	5.998e-03
G to QN	5.380e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

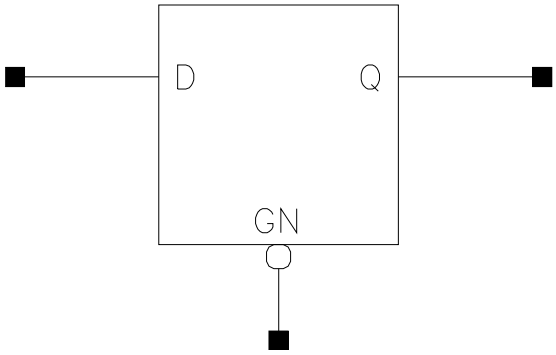
Pin Cycle (vdds)	X17_P16
D (output stable)	-7.863e-06
G (output stable)	-2.059e-07
D to QN	-3.839e-06
G to QN	5.988e-05

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
D	0.0006	0.0008	0.0019
GN	0.0012	0.0016	0.0021

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D to Q ↓	0.0820	0.0707	2.3681	1.1479
D to Q ↑	0.0460	0.0426	4.1675	2.1340
GN to Q ↓	0.0724	0.0617	2.3683	1.1494
GN to Q ↑	0.0707	0.0668	4.1632	2.1315

	X33_P16		X33_P16	
D to Q ↓	0.0679		0.5842	
D to Q ↑	0.0369		1.0707	
GN to Q ↓	0.0577		0.5846	
GN to Q ↑	0.0528		1.0687	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X33_P16
D ↓	hold_rising to GN	-0.0407	-0.0309	-0.0284
D ↑	hold_rising to GN	-0.0042	-0.0042	0.0011
D ↓	setup_rising to GN	0.0905	0.0808	0.0756
D ↑	setup_rising to GN	0.0442	0.0389	0.0341
GN ↓	min_pulse_width to GN	0.0931	0.0837	0.0778

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.558e-07	3.032e-12
X17_P16	2.250e-07	3.536e-12
X33_P16	3.756e-07	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
D (output stable)	1.924e-05	3.354e-05	7.506e-05
GN (output stable)	9.774e-04	1.330e-03	1.540e-03
D to Q	4.595e-03	6.388e-03	1.039e-02
GN to Q	6.614e-03	8.912e-03	1.302e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

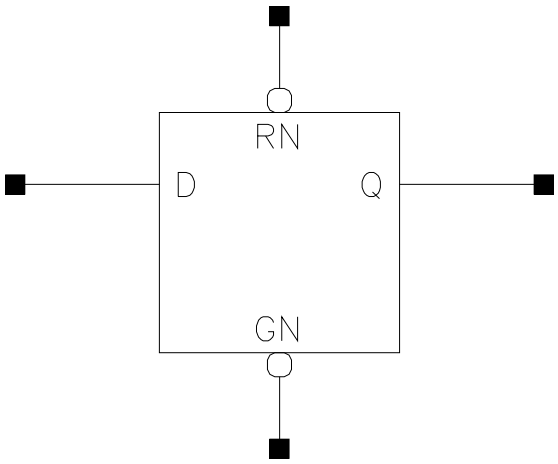
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
D (output stable)	-1.833e-06	-3.222e-06	-6.528e-06
GN (output stable)	2.475e-08	6.614e-08	-3.066e-07
D to Q	-3.896e-06	-5.347e-06	-9.538e-06
GN to Q	-4.180e-05	-2.071e-05	-2.109e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.496	1.7952
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X33_P16
D	0.0006	0.0015
GN	0.0014	0.0026
RN	0.0007	0.0007

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
D to Q ↓	0.0767	0.0687	2.2788	0.5895
D to Q ↑	0.0590	0.0735	4.2396	1.1014

GN to Q ↓	0.0684	0.0623	2.2797	0.5895
GN to Q ↑	0.0796	0.0802	4.2421	1.1008
RN to Q ↓	0.0566	0.1036	2.1758	0.6597
RN to Q ↑	0.0627	0.0786	4.2408	1.1017

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P16	X33_P16
D ↓	hold_rising to GN	-0.0358	-0.0256
D ↑	hold_rising to GN	-0.0164	-0.0334
D ↓	setup_rising to GN	0.0804	0.0735
D ↑	setup_rising to GN	0.0535	0.0779
GN ↓	min_pulse_width to GN	0.0836	0.0826
RN ↓	min_pulse_width to RN	0.0676	0.1235
RN ↑	recovery_rising to GN	0.0584	0.0853
RN ↑	removal_rising to GN	-0.0388	-0.0582

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.790e-07	3.536e-12
X33_P16	3.870e-07	5.301e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X33_P16
D (output stable)	8.780e-05	1.432e-04
GN (output stable)	1.130e-03	1.683e-03
RN (output stable)	1.897e-05	3.584e-05
D to Q	4.579e-03	1.104e-02
GN to Q	6.725e-03	1.420e-02
RN to Q	3.715e-03	8.123e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

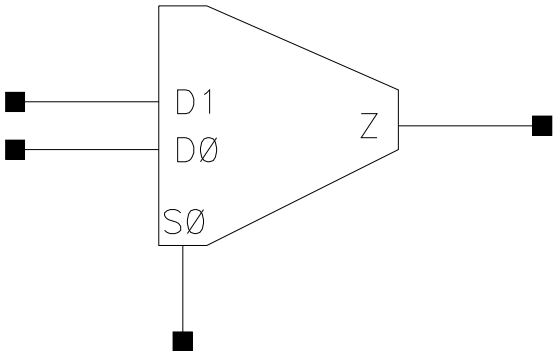
Pin Cycle (vdds)	X8_P16	X33_P16
D (output stable)	-5.687e-06	-1.635e-05
GN (output stable)	1.379e-06	6.310e-06
RN (output stable)	2.324e-06	2.573e-06
D to Q	-1.776e-05	-2.381e-05
GN to Q	-5.685e-05	1.009e-05
RN to Q	4.310e-06	-3.637e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
D0	0.0008	0.0012	0.0015	0.0021
D1	0.0008	0.0011	0.0015	0.0021
S0	0.0014	0.0016	0.0019	0.0027

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D0 to Z ↓	0.0599	0.0533	2.2464	1.1012
D0 to Z ↑	0.0427	0.0391	4.2657	2.0834
D1 to Z ↓	0.0577	0.0530	2.2399	1.0991
D1 to Z ↑	0.0391	0.0366	4.2594	2.0801
S0 to Z ↓	0.0508	0.0486	2.2375	1.0982
S0 to Z ↑	0.0461	0.0458	4.2612	2.0825

	X25_P16	X33_P16	X25_P16	X33_P16
D0 to Z ↓	0.0572	0.0516	0.7634	0.5714
D0 to Z ↑	0.0430	0.0391	1.4017	1.0489
D1 to Z ↓	0.0617	0.0542	0.7679	0.5725
D1 to Z ↑	0.0405	0.0374	1.4003	1.0471
S0 to Z ↓	0.0560	0.0511	0.7649	0.5712
S0 to Z ↑	0.0514	0.0468	1.4005	1.0490

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.460e-07	3.031e-12
X17_P16	2.435e-07	3.289e-12
X25_P16	3.463e-07	5.051e-12
X33_P16	4.752e-07	5.304e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	8.441e-04	1.190e-03	1.264e-03	1.658e-03
D1 (output stable)	6.688e-04	1.080e-03	1.441e-03	1.754e-03
S0 (output stable)	1.193e-03	1.362e-03	1.788e-03	2.176e-03
D0 to Z	3.182e-03	5.065e-03	7.855e-03	9.844e-03
D1 to Z	2.935e-03	4.900e-03	7.911e-03	9.726e-03
S0 to Z	3.655e-03	5.435e-03	8.821e-03	1.081e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

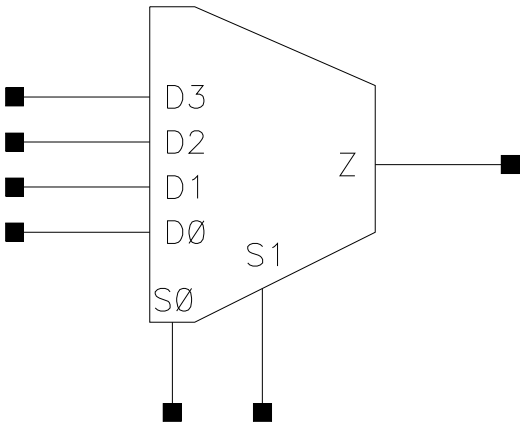
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	-1.798e-07	4.165e-07	2.154e-07	1.150e-07
D1 (output stable)	2.554e-07	5.026e-07	5.858e-07	-6.110e-07
S0 (output stable)	-4.275e-08	-1.868e-07	-1.284e-07	1.148e-07
D0 to Z	-3.780e-07	-5.905e-07	-8.617e-07	-1.072e-06
D1 to Z	-3.744e-07	-7.242e-07	-1.101e-06	-9.230e-07
S0 to Z	-8.157e-08	-3.409e-07	-7.048e-07	-4.352e-07

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.312	2.7744
X31_P16	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P16	X31_P16
D0	0.0006	0.0016
D1	0.0006	0.0015
D2	0.0006	0.0016
D3	0.0006	0.0015
S0	0.0021	0.0041
S1	0.0013	0.0026

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X31_P16	X8_P16	X31_P16

D0 to Z ↓	0.1089	0.1103	2.3941	0.6679
D0 to Z ↑	0.0595	0.0613	4.2843	1.1516
D1 to Z ↓	0.1081	0.1104	2.3915	0.6684
D1 to Z ↑	0.0599	0.0611	4.2846	1.1516
D2 to Z ↓	0.1161	0.1043	2.4096	0.6618
D2 to Z ↑	0.0621	0.0568	4.2949	1.1439
D3 to Z ↓	0.1156	0.1033	2.4086	0.6602
D3 to Z ↑	0.0613	0.0586	4.2895	1.1481
S0 to Z ↓	0.1175	0.1171	2.3959	0.6634
S0 to Z ↑	0.0762	0.0798	4.2910	1.1507
S1 to Z ↓	0.0795	0.0780	2.3999	0.6641
S1 to Z ↑	0.0577	0.0583	4.2814	1.1483

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	2.490e-07	5.049e-12
X31_P16	7.316e-07	9.332e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X31_P16
D0 (output stable)	4.463e-05	1.907e-04
D1 (output stable)	4.415e-05	1.966e-04
D2 (output stable)	5.100e-05	1.586e-04
D3 (output stable)	4.099e-05	1.809e-04
S0 (output stable)	1.952e-03	4.685e-03
S1 (output stable)	1.126e-03	2.307e-03
D0 to Z	3.320e-03	1.094e-02
D1 to Z	3.315e-03	1.101e-02
D2 to Z	3.542e-03	1.034e-02
D3 to Z	3.527e-03	1.031e-02
S0 to Z	5.437e-03	1.567e-02
S1 to Z	3.537e-03	9.699e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

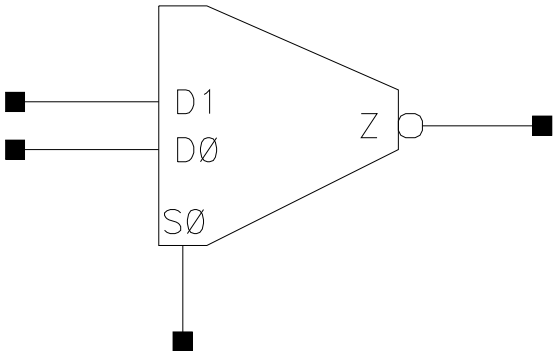
Pin Cycle (vdds)	X8_P16	X31_P16
D0 (output stable)	-4.286e-06	-1.843e-05
D1 (output stable)	-4.754e-06	-2.102e-05
D2 (output stable)	-7.670e-06	-2.430e-05
D3 (output stable)	-5.082e-06	-1.893e-05
S0 (output stable)	-2.892e-05	-9.773e-05
S1 (output stable)	1.696e-05	6.574e-05
D0 to Z	-5.134e-06	-2.034e-05
D1 to Z	-5.834e-06	-2.231e-05
D2 to Z	-5.680e-06	-1.768e-05
D3 to Z	-5.697e-06	-1.710e-05
S0 to Z	-2.356e-05	-7.840e-05
S1 to Z	1.470e-05	6.547e-05

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.816	0.9792
X5_P16	1.200	0.952	1.1424
X10_P16	1.200	1.768	2.1216
X16_P16	1.200	2.448	2.9376
X21_P16	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P16	X5_P16	X10_P16	X16_P16
D0	0.0006	0.0009	0.0018	0.0027
D1	0.0006	0.0009	0.0018	0.0027
S0	0.0013	0.0022	0.0029	0.0044
	X21_P16			
D0	0.0036			
D1	0.0036			
S0	0.0050			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X5_P16	X3_P16	X5_P16
D0 to Z ↓	0.0184	0.0183	7.3228	4.4835

D0 to Z ↑	0.0363	0.0328	19.1269	9.6846
D1 to Z ↓	0.0181	0.0173	7.2449	4.2535
D1 to Z ↑	0.0377	0.0343	19.1299	10.0096
S0 to Z ↓	0.0295	0.0245	7.2648	4.3547
S0 to Z ↑	0.0331	0.0271	19.0890	9.8387
	X10_P16	**X16_P16**	**X10_P16**	**X16_P16**
D0 to Z ↓	0.0204	0.0190	2.1022	1.3747
D0 to Z ↑	0.0353	0.0337	4.5052	2.9606
D1 to Z ↓	0.0182	0.0180	2.0308	1.3441
D1 to Z ↑	0.0359	0.0349	4.5678	2.9880
S0 to Z ↓	0.0296	0.0258	2.0615	1.3574
S0 to Z ↑	0.0317	0.0276	4.5278	2.9678
	X21_P16		**X21_P16**	
D0 to Z ↓	0.0189		1.0494	
D0 to Z ↑	0.0331		2.2421	
D1 to Z ↓	0.0179		1.0195	
D1 to Z ↑	0.0350		2.2303	
S0 to Z ↓	0.0269		1.0322	
S0 to Z ↑	0.0282		2.2303	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P16	8.539e-08	2.276e-12
X5_P16	1.505e-07	2.528e-12
X10_P16	2.807e-07	4.042e-12
X16_P16	4.460e-07	5.295e-12
X21_P16	5.634e-07	6.548e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	2.038e-05	4.520e-05	1.722e-04	2.280e-04
D1 (output stable)	3.742e-05	1.973e-04	2.164e-04	3.336e-04
S0 (output stable)	9.901e-04	1.385e-03	2.478e-03	3.757e-03
D0 to Z	9.972e-04	1.653e-03	4.099e-03	5.753e-03
D1 to Z	9.958e-04	1.636e-03	3.897e-03	5.657e-03
S0 to Z	1.701e-03	2.339e-03	4.973e-03	6.805e-03
	X21_P16			
D0 (output stable)	3.078e-04			
D1 (output stable)	4.794e-04			
S0 (output stable)	4.191e-03			
D0 to Z	7.396e-03			
D1 to Z	7.484e-03			
S0 to Z	8.344e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	-2.099e-06	-4.026e-06	-8.081e-06	-1.707e-05
D1 (output stable)	-9.198e-06	-4.370e-05	-3.791e-05	-6.215e-05
S0 (output stable)	4.918e-06	3.149e-05	2.070e-05	3.086e-05
D0 to Z	-2.082e-06	-3.776e-06	-8.673e-06	-2.099e-05

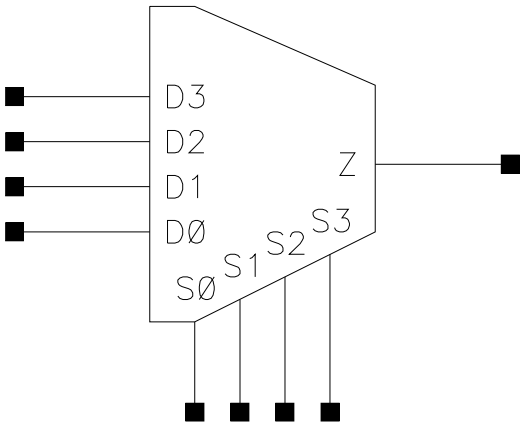
D1 to Z	-1.978e-06	-6.882e-06	-8.766e-06	-1.612e-05
S0 to Z	4.425e-06	7.982e-06	1.764e-05	4.587e-05
	X21_P16			
D0 (output stable)	-2.183e-05			
D1 (output stable)	-1.035e-04			
S0 (output stable)	5.703e-05			
D0 to Z	-2.291e-05			
D1 to Z	-2.506e-05			
S0 to Z	5.144e-05			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	1.768	2.1216
X27_P16	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P16	X27_P16
D0	0.0007	0.0021
D1	0.0007	0.0021
D2	0.0007	0.0021
D3	0.0007	0.0021
S0	0.0007	0.0020
S1	0.0007	0.0020
S2	0.0007	0.0020
S3	0.0007	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	X27_P16	X7_P16	X27_P16
D0 to Z ↓	0.0790	0.0668	3.7498	1.0312
D0 to Z ↑	0.0496	0.0422	4.1810	1.0416
D1 to Z ↓	0.0718	0.0608	3.7479	1.0306
D1 to Z ↑	0.0456	0.0380	4.1695	1.0383
D2 to Z ↓	0.0796	0.0638	3.7675	1.0344
D2 to Z ↑	0.0485	0.0394	4.2003	1.0466
D3 to Z ↓	0.0724	0.0579	3.7635	1.0317
D3 to Z ↑	0.0446	0.0353	4.1889	1.0434
S0 to Z ↓	0.0761	0.0630	3.7526	1.0306
S0 to Z ↑	0.0523	0.0438	4.1818	1.0416
S1 to Z ↓	0.0693	0.0567	3.7434	1.0297
S1 to Z ↑	0.0480	0.0391	4.1711	1.0385
S2 to Z ↓	0.0767	0.0599	3.7623	1.0329
S2 to Z ↑	0.0511	0.0410	4.1994	1.0461
S3 to Z ↓	0.0700	0.0539	3.7537	1.0316
S3 to Z ↑	0.0469	0.0364	4.1910	1.0431

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X7_P16	2.169e-07	4.040e-12
X27_P16	7.989e-07	7.568e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X7_P16	X27_P16
D0 (output stable)	5.526e-04	1.755e-03
D1 (output stable)	4.373e-04	1.329e-03
D2 (output stable)	5.438e-04	1.705e-03
D3 (output stable)	4.033e-04	1.211e-03
S0 (output stable)	5.651e-04	1.733e-03
S1 (output stable)	4.271e-04	1.276e-03
S2 (output stable)	5.021e-04	1.489e-03
S3 (output stable)	3.746e-04	1.062e-03
D0 to Z	4.161e-03	1.302e-02
D1 to Z	3.668e-03	1.126e-02
D2 to Z	3.974e-03	1.116e-02
D3 to Z	3.483e-03	9.401e-03
S0 to Z	4.047e-03	1.232e-02
S1 to Z	3.544e-03	1.055e-02
S2 to Z	3.856e-03	1.045e-02
S3 to Z	3.361e-03	8.707e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

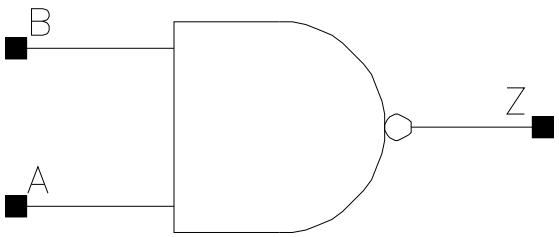
Pin Cycle (vdds)	X7_P16	X27_P16
D0 (output stable)	-3.676e-06	-1.178e-05
D1 (output stable)	1.736e-07	5.678e-07
D2 (output stable)	-9.326e-06	-2.807e-05
D3 (output stable)	6.877e-06	1.985e-05
S0 (output stable)	-8.617e-06	-2.435e-05
S1 (output stable)	6.345e-06	1.723e-05
S2 (output stable)	-5.847e-06	-1.705e-05
S3 (output stable)	1.997e-06	5.645e-06
D0 to Z	-7.811e-06	-2.160e-05
D1 to Z	-3.594e-07	-9.447e-07
D2 to Z	-7.954e-06	-2.312e-05
D3 to Z	-1.324e-07	-6.109e-07
S0 to Z	-8.366e-06	-2.443e-05
S1 to Z	-2.274e-07	-8.352e-07
S2 to Z	-7.651e-06	-2.244e-05
S3 to Z	8.604e-09	-4.371e-07

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P16	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P16	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P16	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P16	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P16	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P16	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P16	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P16	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P16	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P16	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P16	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P16	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P16	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P16	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P16	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P16	C12T28SOI_LR_-NAND2X5_P16	C12T28SOI_LR_-NAND2X7_P16	C12T28SOI_LR_-NAND2X10_P16
A	0.0006	0.0008	0.0009	0.0015
B	0.0006	0.0008	0.0009	0.0014
	C12T28SOI_LR_-NAND2X13_P16	C12T28SOI_LR_-NAND2X17_P16	C12T28SOI_LR_-NAND2X20_P16	C12T28SOI_LR_-NAND2X24_P16
A	0.0018	0.0023	0.0026	0.0032
B	0.0017	0.0022	0.0025	0.0030
	C12T28SOI_LR_-NAND2X27_P16	C12T28SOI_LR_-NAND2X42_P16	C12T28SOI_LR_-NAND2X47_P16	C12T28SOI_LR_-NAND2X50_P16
A	0.0036	0.0011	0.0011	0.0011
B	0.0033	0.0012	0.0012	0.0012
	C12T28SOI_LR_-NAND2X58_P16	C12T28SOI_LR_-NAND2X67_P16	C12T28SOI_-LRBR0D8_-NAND2X7_P16	C12T28SOI_-LRBR0D8_-NAND2X14_P16
A	0.0011	0.0011	0.0009	0.0018
B	0.0012	0.0012	0.0009	0.0016
	C12T28SOI_LRS_-NAND2X40_P16	C12T28SOI_LRS_-NAND2X54_P16		
A	0.0053	0.0071		
B	0.0049	0.0066		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P16	**C12T28SOI_LR_-NAND2X5_P16**	**C12T28SOI_LR_-NAND2X3_P16**	**C12T28SOI_LR_-NAND2X5_P16**
A to Z ↓	0.0144	0.0131	7.0940	4.5367
A to Z ↑	0.0231	0.0213	8.2315	5.2283
B to Z ↓	0.0151	0.0132	7.1912	4.6020
B to Z ↑	0.0210	0.0187	8.2916	5.2640
	C12T28SOI_LR_-NAND2X7_P16	**C12T28SOI_LR_-NAND2X10_P16**	**C12T28SOI_LR_-NAND2X7_P16**	**C12T28SOI_LR_-NAND2X10_P16**
A to Z ↓	0.0129	0.0151	3.8112	2.5503
A to Z ↑	0.0207	0.0222	4.2266	2.7761
B to Z ↓	0.0130	0.0132	3.8486	2.5793
B to Z ↑	0.0180	0.0182	4.2657	2.7982
	C12T28SOI_LR_-NAND2X13_P16	**C12T28SOI_LR_-NAND2X17_P16**	**C12T28SOI_LR_-NAND2X13_P16**	**C12T28SOI_LR_-NAND2X17_P16**
A to Z ↓	0.0145	0.0143	1.9556	1.5565

A to Z ↑	0.0212	0.0214	2.0718	1.6748
B to Z ↓	0.0125	0.0131	1.9811	1.5758
B to Z ↑	0.0171	0.0178	2.0882	1.6880
	C12T28SOI_LR_-NAND2X20_P16	**C12T28SOI_LR_-NAND2X24_P16**	**C12T28SOI_LR_-NAND2X20_P16**	**C12T28SOI_LR_-NAND2X24_P16**
A to Z ↓	0.0141	0.0147	1.3428	1.1433
A to Z ↑	0.0209	0.0213	1.3949	1.1932
B to Z ↓	0.0130	0.0127	1.3567	1.1585
B to Z ↑	0.0174	0.0172	1.4079	1.2031
	C12T28SOI_LR_-NAND2X27_P16	**C12T28SOI_LR_-NAND2X42_P16**	**C12T28SOI_LR_-NAND2X27_P16**	**C12T28SOI_LR_-NAND2X42_P16**
A to Z ↓	0.0144	0.0512	1.0163	0.4512
A to Z ↑	0.0209	0.0547	1.0454	0.8313
B to Z ↓	0.0126	0.0525	1.0303	0.4511
B to Z ↑	0.0168	0.0527	1.0544	0.8325
	C12T28SOI_LR_-NAND2X47_P16	**C12T28SOI_LR_-NAND2X50_P16**	**C12T28SOI_LR_-NAND2X47_P16**	**C12T28SOI_LR_-NAND2X50_P16**
A to Z ↓	0.0529	0.0533	0.4014	0.3768
A to Z ↑	0.0556	0.0559	0.7239	0.6937
B to Z ↓	0.0542	0.0546	0.4011	0.3771
B to Z ↑	0.0536	0.0539	0.7234	0.6947
	C12T28SOI_LR_-NAND2X58_P16	**C12T28SOI_LR_-NAND2X67_P16**	**C12T28SOI_LR_-NAND2X58_P16**	**C12T28SOI_LR_-NAND2X67_P16**
A to Z ↓	0.0561	0.0582	0.3276	0.2885
A to Z ↑	0.0579	0.0592	0.5977	0.5249
B to Z ↓	0.0574	0.0595	0.3275	0.2885
B to Z ↑	0.0558	0.0571	0.5969	0.5251
	C12T28SOI_-LRBR0D8_-NAND2X7_P16	**C12T28SOI_-LRBR0D8_-NAND2X14_P16**	**C12T28SOI_-LRBR0D8_-NAND2X7_P16**	**C12T28SOI_-LRBR0D8_-NAND2X14_P16**
A to Z ↓	0.0114	0.0129	2.8514	1.5113
A to Z ↑	0.0244	0.0249	5.6492	2.7512
B to Z ↓	0.0108	0.0102	2.9061	1.5427
B to Z ↑	0.0202	0.0186	5.8323	2.8051
	C12T28SOI_LRS_-NAND2X40_P16	**C12T28SOI_LRS_-NAND2X54_P16**	**C12T28SOI_LRS_-NAND2X40_P16**	**C12T28SOI_LRS_-NAND2X54_P16**
A to Z ↓	0.0143	0.0144	0.6898	0.5226
A to Z ↑	0.0208	0.0208	0.6999	0.5276
B to Z ↓	0.0127	0.0129	0.6996	0.5296
B to Z ↑	0.0169	0.0170	0.7067	0.5330

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P16	3.775e-08	1.520e-12
C12T28SOI_LR_NAND2X5_P16	5.698e-08	1.520e-12
C12T28SOI_LR_NAND2X7_P16	6.804e-08	1.520e-12
C12T28SOI_LR_NAND2X10_P16	1.040e-07	2.024e-12
C12T28SOI_LR_NAND2X13_P16	1.355e-07	2.024e-12
C12T28SOI_LR_NAND2X17_P16	1.696e-07	2.527e-12
C12T28SOI_LR_NAND2X20_P16	2.006e-07	2.527e-12
C12T28SOI_LR_NAND2X24_P16	2.350e-07	3.031e-12
C12T28SOI_LR_NAND2X27_P16	2.656e-07	3.031e-12

C12T28SOI_LR_NAND2X42_P16	3.455e-07	3.275e-12
C12T28SOI_LR_NAND2X47_P16	3.703e-07	3.525e-12
C12T28SOI_LR_NAND2X50_P16	3.814e-07	3.534e-12
C12T28SOI_LR_NAND2X58_P16	4.173e-07	3.784e-12
C12T28SOI_LR_NAND2X67_P16	4.532e-07	4.056e-12
C12T28SOI_LRBR0D8_NAND2X7_-P16	7.538e-08	2.774e-12
C12T28SOI_LRBR0D8_NAND2X14_-P16	1.492e-07	3.307e-12
C12T28SOI_LRS_NAND2X40_P16	3.957e-07	4.039e-12
C12T28SOI_LRS_NAND2X54_P16	5.258e-07	5.045e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P16	C12T28SOI_LR_-NAND2X5_P16	C12T28SOI_LR_-NAND2X7_P16	C12T28SOI_LR_-NAND2X10_P16
A (output stable)	9.282e-06	1.370e-05	1.624e-05	3.696e-05
B (output stable)	3.642e-05	5.686e-05	6.894e-05	3.336e-04
A to Z	6.554e-04	8.541e-04	1.005e-03	1.823e-03
B to Z	5.089e-04	6.153e-04	7.175e-04	1.114e-03
	C12T28SOI_LR_-NAND2X13_P16	C12T28SOI_LR_-NAND2X17_P16	C12T28SOI_LR_-NAND2X20_P16	C12T28SOI_LR_-NAND2X24_P16
A (output stable)	4.625e-05	6.450e-05	7.348e-05	9.198e-05
B (output stable)	3.824e-04	3.910e-04	4.333e-04	6.502e-04
A to Z	2.197e-03	2.783e-03	3.145e-03	3.886e-03
B to Z	1.319e-03	1.779e-03	2.003e-03	2.325e-03
	C12T28SOI_LR_-NAND2X27_P16	C12T28SOI_LR_-NAND2X42_P16	C12T28SOI_LR_-NAND2X47_P16	C12T28SOI_LR_-NAND2X50_P16
A (output stable)	9.686e-05	1.798e-05	1.801e-05	1.806e-05
B (output stable)	6.934e-04	7.503e-05	7.535e-05	7.518e-05
A to Z	4.234e-03	1.166e-02	1.247e-02	1.278e-02
B to Z	2.530e-03	1.137e-02	1.219e-02	1.249e-02
	C12T28SOI_LR_-NAND2X58_P16	C12T28SOI_LR_-NAND2X67_P16	C12T28SOI_-LRBR0D8_-NAND2X7_P16	C12T28SOI_-LRBR0D8_-NAND2X14_P16
A (output stable)	1.818e-05	1.841e-05	2.034e-05	5.534e-05
B (output stable)	7.528e-05	7.483e-05	9.144e-05	4.839e-04
A to Z	1.449e-02	1.570e-02	1.065e-03	2.316e-03
B to Z	1.420e-02	1.542e-02	6.768e-04	1.175e-03
	C12T28SOI_LRS_-NAND2X40_P16	C12T28SOI_LRS_-NAND2X54_P16		
A (output stable)	1.473e-04	1.899e-04		
B (output stable)	9.756e-04	1.238e-03		
A to Z	6.288e-03	8.291e-03		
B to Z	3.813e-03	5.069e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P16	C12T28SOI_LR_-NAND2X5_P16	C12T28SOI_LR_-NAND2X7_P16	C12T28SOI_LR_-NAND2X10_P16
A (output stable)	5.010e-08	-1.580e-08	-3.530e-08	-8.150e-08
B (output stable)	1.220e-08	5.200e-09	-3.000e-08	-7.580e-08
A to Z	-2.098e-07	-4.618e-07	-5.469e-07	-1.957e-07

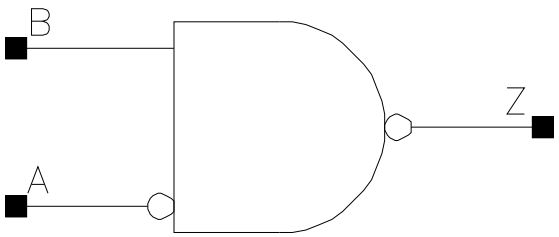
B to Z	1.361e-07	1.232e-07	1.041e-07	1.488e-07
	C12T28SOI_LR_-NAND2X13_P16	C12T28SOI_LR_-NAND2X17_P16	C12T28SOI_LR_-NAND2X20_P16	C12T28SOI_LR_-NAND2X24_P16
A (output stable)	4.700e-07	3.768e-07	-2.591e-07	8.164e-07
B (output stable)	-2.489e-06	-2.266e-06	-2.914e-07	-4.566e-06
A to Z	6.600e-09	-1.154e-06	-5.290e-07	-1.320e-07
B to Z	-3.540e-07	-6.010e-07	-7.240e-07	-9.500e-08
	C12T28SOI_LR_-NAND2X27_P16	C12T28SOI_LR_-NAND2X42_P16	C12T28SOI_LR_-NAND2X47_P16	C12T28SOI_LR_-NAND2X50_P16
A (output stable)	6.658e-07	-1.739e-08	-1.675e-08	-1.678e-08
B (output stable)	-4.270e-06	-2.210e-08	-2.290e-08	-2.190e-08
A to Z	-2.789e-06	-4.080e-07	-5.230e-07	-6.230e-07
B to Z	2.100e-08	-1.009e-06	-7.140e-07	-4.980e-07
	C12T28SOI_LR_-NAND2X58_P16	C12T28SOI_LR_-NAND2X67_P16	C12T28SOI_-LRBR0D8_-NAND2X7_P16	C12T28SOI_-LRBR0D8_-NAND2X14_P16
A (output stable)	-1.714e-08	-1.628e-08	9.000e-10	2.205e-06
B (output stable)	-2.310e-08	-2.300e-08	-9.900e-09	-9.418e-06
A to Z	-1.510e-07	-7.530e-07	-4.617e-07	6.412e-07
B to Z	-1.025e-06	-6.830e-07	3.060e-08	-2.287e-07
	C12T28SOI_LRS_-NAND2X40_P16	C12T28SOI_LRS_-NAND2X54_P16		
A (output stable)	7.062e-07	9.681e-07		
B (output stable)	-5.602e-06	-7.484e-06		
A to Z	-3.640e-07	-5.977e-06		
B to Z	4.210e-07	7.090e-07		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X7_P16	1.200	0.544	0.6528
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X40_P16	1.200	2.312	2.7744
X54_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P16	X7_P16	X13_P16	X27_P16
A	0.0009	0.0009	0.0012	0.0022
B	0.0006	0.0009	0.0016	0.0032
	X40_P16	X54_P16		
A	0.0033	0.0043		
B	0.0048	0.0065		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0396	0.0421	7.0905	3.8051
A to Z ↑	0.0295	0.0305	8.0850	4.1966
B to Z ↓	0.0154	0.0129	7.2697	3.8799
B to Z ↑	0.0211	0.0180	8.2917	4.3015
	X13_P16	**X27_P16**	**X13_P16**	**X27_P16**

A to Z ↓	0.0391	0.0379	2.0475	1.0201
A to Z ↑	0.0290	0.0281	2.1536	1.0433
B to Z ↓	0.0123	0.0123	2.0914	1.0436
B to Z ↑	0.0169	0.0167	2.1401	1.0556
	X40_P16	**X54_P16**	**X40_P16**	**X54_P16**
A to Z ↓	0.0384	0.0385	0.6834	0.5188
A to Z ↑	0.0287	0.0287	0.6947	0.5241
B to Z ↓	0.0122	0.0123	0.6980	0.5294
B to Z ↑	0.0165	0.0165	0.7095	0.5355

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P16	6.121e-08	1.772e-12
X7_P16	9.213e-08	1.772e-12
X13_P16	1.776e-07	2.528e-12
X27_P16	3.550e-07	3.789e-12
X40_P16	5.268e-07	5.050e-12
X54_P16	6.986e-07	6.309e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	1.092e-03	1.426e-03	2.355e-03	4.507e-03
B (output stable)	3.706e-05	6.928e-05	3.578e-04	6.356e-04
A to Z	1.856e-03	2.587e-03	4.719e-03	9.176e-03
B to Z	5.183e-04	7.129e-04	1.275e-03	2.521e-03
	X40_P16	X54_P16		
A (output stable)	6.942e-03	9.194e-03		
B (output stable)	9.394e-04	1.224e-03		
A to Z	1.380e-02	1.827e-02		
B to Z	3.603e-03	4.746e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

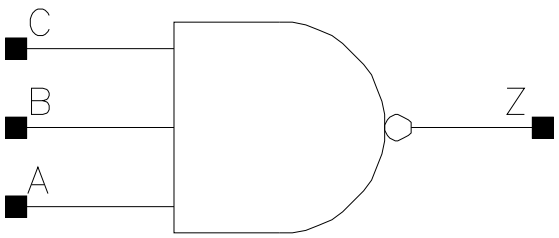
Pin Cycle (vdds)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	-1.967e-07	-2.154e-07	-4.525e-07	2.742e-06
B (output stable)	1.180e-08	-3.510e-08	-1.571e-07	-2.956e-06
A to Z	-2.045e-07	-3.200e-08	-5.920e-08	-3.800e-08
B to Z	-7.320e-08	4.129e-07	7.898e-07	2.350e-07
	X40_P16	X54_P16		
A (output stable)	3.574e-06	7.047e-06		
B (output stable)	-4.706e-06	-7.268e-06		
A to Z	-1.006e-06	-1.117e-06		
B to Z	3.600e-07	6.950e-07		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P16	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P16	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P16	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P16	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P16	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P16	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P16	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P16	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P16	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P16	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P16	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P16	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P16	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P16	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P16	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P16	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A	0.0007	0.0009	0.0015	0.0018
B	0.0008	0.0009	0.0014	0.0017
C	0.0007	0.0009	0.0013	0.0016
	C12T28SOI_LR_-NAND3X15_P16	C12T28SOI_LR_-NAND3X18_P16	C12T28SOI_LR_-NAND3X21_P16	C12T28SOI_LR_-NAND3X24_P16
A	0.0023	0.0026	0.0032	0.0035
B	0.0022	0.0025	0.0030	0.0034
C	0.0021	0.0024	0.0029	0.0032
	C12T28SOI_LR_-NAND3X35_P16	C12T28SOI_LR_-NAND3X47_P16	C12T28SOI_-LRBR0P6_-NAND3X6_P16	C12T28SOI_-LRBR0P6_-NAND3X12_P16
A	0.0053	0.0071	0.0009	0.0018
B	0.0050	0.0067	0.0010	0.0017
C	0.0048	0.0064	0.0009	0.0016
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	C12T28SOI_-LRBR0P6_-NAND3X24_P16	C12T28SOI_-LRBR0P6_-NAND3X35_P16	C12T28SOI_-LRBR0P6_-NAND3X47_P16
A	0.0026	0.0036	0.0053	0.0070
B	0.0025	0.0033	0.0050	0.0066
C	0.0023	0.0031	0.0046	0.0062
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16			
A	0.0028			
B	0.0026			
C	0.0024			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16
A to Z ↓	0.0218	0.0198	7.5387	5.3709
A to Z ↑	0.0284	0.0261	5.9719	4.1027
B to Z ↓	0.0226	0.0202	7.5556	5.3816
B to Z ↑	0.0271	0.0245	5.9825	4.1114
C to Z ↓	0.0199	0.0178	7.5962	5.4111
C to Z ↑	0.0234	0.0211	5.9909	4.1395

	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A to Z ↓	0.0221	0.0206	3.6690	2.8455
A to Z ↑	0.0274	0.0258	2.7950	2.0962
B to Z ↓	0.0207	0.0195	3.6788	2.8536
B to Z ↑	0.0249	0.0235	2.8001	2.1002
C to Z ↓	0.0180	0.0170	3.7007	2.8720
C to Z ↑	0.0211	0.0198	2.7911	2.0832
	C12T28SOI_LR_-NAND3X15_P16	**C12T28SOI_LR_-NAND3X18_P16**	**C12T28SOI_LR_-NAND3X15_P16**	**C12T28SOI_LR_-NAND3X18_P16**
A to Z ↓	0.0202	0.0198	2.3068	1.9776
A to Z ↑	0.0255	0.0248	1.6729	1.3921
B to Z ↓	0.0197	0.0193	2.3125	1.9853
B to Z ↑	0.0232	0.0226	1.6774	1.3954
C to Z ↓	0.0175	0.0169	2.3267	1.9949
C to Z ↑	0.0199	0.0191	1.6893	1.4052
	C12T28SOI_LR_-NAND3X21_P16	**C12T28SOI_LR_-NAND3X24_P16**	**C12T28SOI_LR_-NAND3X21_P16**	**C12T28SOI_LR_-NAND3X24_P16**
A to Z ↓	0.0207	0.0202	1.6725	1.4917
A to Z ↑	0.0256	0.0251	1.1998	1.0528
B to Z ↓	0.0197	0.0194	1.6781	1.4960
B to Z ↑	0.0233	0.0229	1.2020	1.0550
C to Z ↓	0.0173	0.0169	1.6879	1.5054
C to Z ↑	0.0197	0.0192	1.2034	1.0551
	C12T28SOI_LR_-NAND3X35_P16	**C12T28SOI_LR_-NAND3X47_P16**	**C12T28SOI_LR_-NAND3X35_P16**	**C12T28SOI_LR_-NAND3X47_P16**
A to Z ↓	0.0198	0.0201	1.0188	0.7754
A to Z ↑	0.0247	0.0249	0.7038	0.5316
B to Z ↓	0.0192	0.0193	1.0221	0.7781
B to Z ↑	0.0224	0.0225	0.7045	0.5306
C to Z ↓	0.0168	0.0170	1.0287	0.7827
C to Z ↑	0.0189	0.0189	0.7088	0.5336
	C12T28SOI_-LRBR0P6_-NAND3X6_P16	**C12T28SOI_-LRBR0P6_-NAND3X12_P16**	**C12T28SOI_-LRBR0P6_-NAND3X6_P16**	**C12T28SOI_-LRBR0P6_-NAND3X12_P16**
A to Z ↓	0.0164	0.0173	3.6186	1.9148
A to Z ↑	0.0352	0.0352	6.5187	3.3229
B to Z ↓	0.0163	0.0156	3.6391	1.9266
B to Z ↑	0.0317	0.0302	6.5363	3.3307
C to Z ↓	0.0132	0.0121	3.6814	1.9509
C to Z ↑	0.0247	0.0225	6.5743	3.3383
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	**C12T28SOI_-LRBR0P6_-NAND3X24_P16**	**C12T28SOI_-LRBR0P6_-NAND3X18_P16**	**C12T28SOI_-LRBR0P6_-NAND3X24_P16**
A to Z ↓	0.0164	0.0169	1.3305	1.0030
A to Z ↑	0.0337	0.0341	2.2086	1.6675
B to Z ↓	0.0154	0.0154	1.3394	1.0109
B to Z ↑	0.0289	0.0293	2.2157	1.6719
C to Z ↓	0.0123	0.0120	1.3546	1.0223
C to Z ↑	0.0220	0.0218	2.2345	1.6745
	C12T28SOI_-LRBR0P6_-NAND3X35_P16	**C12T28SOI_-LRBR0P6_-NAND3X47_P16**	**C12T28SOI_-LRBR0P6_-NAND3X35_P16**	**C12T28SOI_-LRBR0P6_-NAND3X47_P16**

A to Z ↓	0.0164	0.0167	0.6863	0.5245
A to Z ↑	0.0341	0.0341	1.1441	0.8647
B to Z ↓	0.0153	0.0154	0.6909	0.5280
B to Z ↑	0.0291	0.0292	1.1461	0.8659
C to Z ↓	0.0120	0.0124	0.7000	0.5343
C to Z ↑	0.0217	0.0219	1.1607	0.8705
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P16**	
A to Z ↓	0.0170		1.2829	
A to Z ↑	0.0337		2.0780	
B to Z ↓	0.0153		1.2895	
B to Z ↑	0.0288		2.0821	
C to Z ↓	0.0116		1.3061	
C to Z ↑	0.0212		2.0668	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P16	6.229e-08	2.024e-12
C12T28SOI_LR_NAND3X6_P16	8.672e-08	2.024e-12
C12T28SOI_LR_NAND3X9_P16	1.294e-07	2.779e-12
C12T28SOI_LR_NAND3X12_P16	1.691e-07	2.780e-12
C12T28SOI_LR_NAND3X15_P16	2.084e-07	3.284e-12
C12T28SOI_LR_NAND3X18_P16	2.475e-07	3.284e-12
C12T28SOI_LR_NAND3X21_P16	2.928e-07	4.292e-12
C12T28SOI_LR_NAND3X24_P16	3.315e-07	4.292e-12
C12T28SOI_LR_NAND3X35_P16	4.958e-07	5.804e-12
C12T28SOI_LR_NAND3X47_P16	6.581e-07	7.317e-12
C12T28SOI_LRBR0P6_NAND3X6_-P16	9.673e-08	3.444e-12
C12T28SOI_LRBR0P6_NAND3X12_-P16	1.888e-07	4.260e-12
C12T28SOI_LRBR0P6_NAND3X18_-P16	2.753e-07	4.804e-12
C12T28SOI_LRBR0P6_NAND3X24_-P16	3.709e-07	5.891e-12
C12T28SOI_LRBR0P6_NAND3X35_-P16	5.562e-07	7.521e-12
C12T28SOI_LRBR0P6_NAND3X47_-P16	7.386e-07	9.154e-12
C12T28SOIDV_LRBR0P6_-NAND3X18_P16	2.932e-07	3.964e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A (output stable)	1.188e-05	1.608e-05	1.837e-05	2.560e-05
B (output stable)	3.649e-05	4.694e-05	9.270e-05	1.087e-04
C (output stable)	6.509e-05	7.584e-05	1.082e-04	1.247e-04
A to Z	1.515e-03	1.844e-03	3.048e-03	3.585e-03
B to Z	1.343e-03	1.584e-03	2.420e-03	2.836e-03
C to Z	9.958e-04	1.159e-03	1.702e-03	1.966e-03

	C12T28SOI_LR_-NAND3X15_P16	C12T28SOI_LR_-NAND3X18_P16	C12T28SOI_LR_-NAND3X21_P16	C12T28SOI_LR_-NAND3X24_P16
A (output stable)	2.509e-05	2.639e-05	4.134e-05	4.699e-05
B (output stable)	1.191e-04	1.328e-04	1.739e-04	1.886e-04
C (output stable)	1.309e-04	1.499e-04	2.024e-04	2.185e-04
A to Z	4.337e-03	4.904e-03	6.155e-03	6.708e-03
B to Z	3.446e-03	3.884e-03	4.871e-03	5.301e-03
C to Z	2.456e-03	2.703e-03	3.387e-03	3.652e-03
	C12T28SOI_LR_-NAND3X35_P16	C12T28SOI_LR_-NAND3X47_P16	C12T28SOI_-LRBR0P6_-NAND3X6_P16	C12T28SOI_-LRBR0P6_-NAND3X12_P16
A (output stable)	5.274e-05	7.556e-05	2.040e-05	3.344e-05
B (output stable)	2.535e-04	3.333e-04	6.632e-05	1.561e-04
C (output stable)	3.169e-04	4.015e-04	1.002e-04	1.774e-04
A to Z	9.691e-03	1.283e-02	2.017e-03	3.974e-03
B to Z	7.616e-03	1.006e-02	1.628e-03	2.891e-03
C to Z	5.178e-03	6.914e-03	1.005e-03	1.598e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	C12T28SOI_-LRBR0P6_-NAND3X24_P16	C12T28SOI_-LRBR0P6_-NAND3X35_P16	C12T28SOI_-LRBR0P6_-NAND3X47_P16
A (output stable)	3.324e-05	6.088e-05	6.945e-05	9.644e-05
B (output stable)	1.893e-04	2.729e-04	3.719e-04	4.709e-04
C (output stable)	2.038e-04	3.154e-04	4.618e-04	5.948e-04
A to Z	5.427e-03	7.440e-03	1.079e-02	1.418e-02
B to Z	3.930e-03	5.384e-03	7.764e-03	1.028e-02
C to Z	2.248e-03	2.965e-03	4.206e-03	5.593e-03
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16			
A (output stable)	4.435e-05			
B (output stable)	2.336e-04			
C (output stable)	2.550e-04			
A to Z	5.810e-03			
B to Z	4.209e-03			
C to Z	2.260e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P16	C12T28SOI_LR_-NAND3X6_P16	C12T28SOI_LR_-NAND3X9_P16	C12T28SOI_LR_-NAND3X12_P16
A (output stable)	2.933e-08	-7.600e-09	8.402e-07	-9.147e-08
B (output stable)	4.027e-08	3.413e-09	1.208e-06	-1.817e-07
C (output stable)	8.667e-09	-4.823e-08	-1.058e-06	-1.857e-07
A to Z	-8.420e-07	-1.751e-06	-3.470e-07	2.540e-07
B to Z	-9.560e-07	-8.340e-07	-5.520e-07	-1.088e-06
C to Z	2.330e-07	2.940e-07	2.940e-07	1.270e-07
	C12T28SOI_LR_-NAND3X15_P16	C12T28SOI_LR_-NAND3X18_P16	C12T28SOI_LR_-NAND3X21_P16	C12T28SOI_LR_-NAND3X24_P16
A (output stable)	6.705e-07	5.845e-07	1.360e-06	1.217e-06
B (output stable)	8.762e-07	7.558e-07	1.928e-06	1.636e-06
C (output stable)	-1.067e-06	-1.090e-06	-2.031e-06	-1.909e-06
A to Z	-1.839e-06	7.400e-07	-1.765e-06	-2.438e-06
B to Z	5.070e-07	6.500e-07	-1.471e-06	1.376e-06

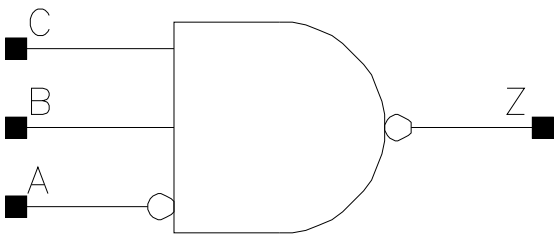
C to Z	5.590e-07	4.310e-07	5.380e-07	3.170e-07
	C12T28SOI_LR_-NAND3X35_P16	C12T28SOI_LR_-NAND3X47_P16	C12T28SOI_-LRBR0P6_-NAND3X6_P16	C12T28SOI_-LRBR0P6_-NAND3X12_P16
A (output stable)	1.800e-06	2.171e-06	1.611e-06	5.942e-06
B (output stable)	2.502e-06	2.950e-06	2.632e-06	1.415e-06
C (output stable)	-2.879e-06	-3.600e-06	-2.044e-06	-2.475e-06
A to Z	-3.121e-06	2.412e-06	-1.132e-06	-3.070e-07
B to Z	-2.161e-06	2.246e-06	-2.580e-07	-8.380e-07
C to Z	4.530e-07	-3.100e-08	6.690e-08	7.910e-07
	C12T28SOI_-LRBR0P6_-NAND3X18_P16	C12T28SOI_-LRBR0P6_-NAND3X24_P16	C12T28SOI_-LRBR0P6_-NAND3X35_P16	C12T28SOI_-LRBR0P6_-NAND3X47_P16
A (output stable)	-8.677e-08	6.664e-06	2.642e-06	3.744e-06
B (output stable)	-1.548e-07	2.310e-06	3.521e-06	4.787e-06
C (output stable)	-1.383e-07	-3.314e-06	-3.265e-06	-4.384e-06
A to Z	-4.181e-06	1.486e-06	-5.121e-06	1.323e-06
B to Z	-3.880e-07	1.037e-06	7.160e-07	1.122e-06
C to Z	-3.400e-08	1.722e-06	-1.250e-07	-2.116e-06
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P16			
A (output stable)	-3.657e-08			
B (output stable)	-1.565e-07			
C (output stable)	-1.834e-07			
A to Z	-3.488e-06			
B to Z	-3.790e-07			
C to Z	-6.810e-07			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.816	0.9792
X12_P16	1.200	1.224	1.4688
X18_P16	1.200	1.496	1.7952
X24_P16	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0008	0.0012	0.0012	0.0022
B	0.0009	0.0017	0.0025	0.0033
C	0.0009	0.0016	0.0024	0.0032

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X12_P16**	**X6_P16**	**X12_P16**
A to Z ↓	0.0470	0.0450	5.4080	2.8789
A to Z ↑	0.0331	0.0318	4.0787	2.0448
B to Z ↓	0.0180	0.0188	5.4412	2.8971
B to Z ↑	0.0226	0.0225	4.1207	2.0723
C to Z ↓	0.0174	0.0161	5.4711	2.9148
C to Z ↑	0.0202	0.0187	4.1474	2.0875
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0515	0.0435	1.9806	1.4969

A to Z ↑	0.0363	0.0303	1.3776	1.0314
B to Z ↓	0.0192	0.0187	1.9907	1.5062
B to Z ↑	0.0226	0.0222	1.3957	1.0485
C to Z ↓	0.0169	0.0160	2.0013	1.5159
C to Z ↑	0.0192	0.0183	1.4061	1.0567

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P16	1.082e-07	2.276e-12
X12_P16	2.135e-07	3.033e-12
X18_P16	2.896e-07	3.535e-12
X24_P16	4.243e-07	5.049e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	1.372e-03	2.399e-03	3.337e-03	4.422e-03
B (output stable)	2.469e-05	8.209e-05	1.355e-04	2.010e-04
C (output stable)	3.467e-05	1.605e-04	1.913e-04	3.157e-04
A to Z	3.155e-03	6.150e-03	8.904e-03	1.166e-02
B to Z	1.321e-03	2.601e-03	3.884e-03	4.933e-03
C to Z	1.020e-03	1.724e-03	2.702e-03	3.226e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

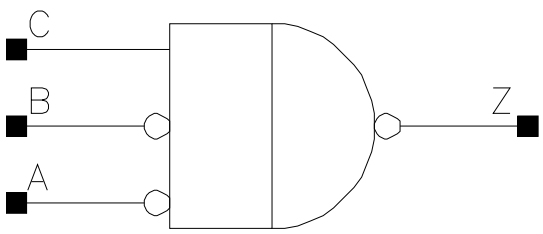
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	-2.231e-07	-8.677e-08	-1.733e-08	1.772e-06
B (output stable)	-8.083e-09	1.031e-06	-3.176e-07	-5.670e-08
C (output stable)	-4.417e-08	-1.064e-06	-2.395e-07	-1.796e-06
A to Z	6.470e-08	-7.200e-08	2.080e-07	1.200e-07
B to Z	3.650e-07	-4.110e-07	2.430e-07	-2.154e-06
C to Z	6.000e-08	9.190e-07	4.560e-07	1.911e-06

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	0.816	0.9792
X13_P16	1.200	1.088	1.3056
X20_P16	1.200	1.632	1.9584
X27_P16	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P16	X13_P16	X20_P16	X27_P16
A	0.0011	0.0010	0.0021	0.0019
B	0.0012	0.0011	0.0021	0.0019
C	0.0009	0.0017	0.0024	0.0032

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	**X13_P16**	**X7_P16**	**X13_P16**
A to Z ↓	0.0473	0.0581	3.6577	1.9594
A to Z ↑	0.0277	0.0317	4.0458	2.0341
B to Z ↓	0.0463	0.0575	3.6692	1.9624
B to Z ↑	0.0263	0.0304	4.0456	2.0324
C to Z ↓	0.0128	0.0122	3.7191	1.9823
C to Z ↑	0.0179	0.0168	4.1402	2.0868
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0523	0.0579	1.3361	1.0172
A to Z ↑	0.0295	0.0349	1.3725	1.0293
B to Z ↓	0.0488	0.0554	1.3358	1.0190

B to Z ↑	0.0274	0.0334	1.3697	1.0284
C to Z ↓	0.0133	0.0127	1.3570	1.0295
C to Z ↑	0.0178	0.0172	1.4072	1.0564

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X7_P16	1.319e-07	2.276e-12
X13_P16	1.837e-07	2.780e-12
X20_P16	3.072e-07	3.788e-12
X27_P16	3.372e-07	4.291e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	7.822e-04	1.102e-03	1.795e-03	2.144e-03
B (output stable)	6.140e-04	8.957e-04	1.286e-03	1.671e-03
C (output stable)	2.807e-05	1.395e-04	1.479e-04	1.957e-04
A to Z	3.436e-03	5.643e-03	8.959e-03	1.111e-02
B to Z	3.043e-03	5.265e-03	7.762e-03	1.012e-02
C to Z	7.346e-04	1.273e-03	2.158e-03	2.767e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

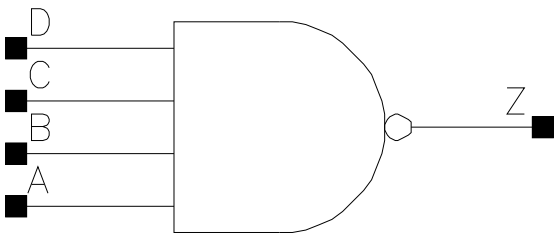
Pin Cycle (vdds)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	-4.436e-06	-4.399e-06	-1.350e-05	-1.314e-05
B (output stable)	-4.777e-08	-2.860e-08	-1.525e-07	-2.167e-09
C (output stable)	-1.480e-08	-1.344e-07	-1.614e-07	-3.209e-07
A to Z	-4.695e-06	-4.679e-06	-1.320e-05	-1.413e-05
B to Z	-4.909e-07	-5.099e-07	-1.013e-06	-6.370e-07
C to Z	1.886e-07	2.613e-07	-8.440e-07	3.550e-07

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0007	0.0007	0.0009	0.0010
B	0.0008	0.0008	0.0009	0.0012
C	0.0007	0.0008	0.0009	0.0011
D	0.0007	0.0007	0.0009	0.0012

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0730	0.0712	2.1980	1.0968
A to Z ↑	0.0562	0.0605	4.1188	2.0502
B to Z ↓	0.0744	0.0737	2.1982	1.0961
B to Z ↑	0.0541	0.0596	4.1202	2.0488
C to Z ↓	0.0727	0.0693	2.1981	1.0972
C to Z ↑	0.0576	0.0628	4.1229	2.0494

D to Z ↓	0.0746	0.0707	2.1980	1.0968
D to Z ↑	0.0562	0.0605	4.1208	2.0500
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0747	0.0683	0.7593	0.5681
A to Z ↑	0.0587	0.0569	1.3834	1.0359
B to Z ↓	0.0762	0.0695	0.7600	0.5678
B to Z ↑	0.0571	0.0551	1.3832	1.0354
C to Z ↓	0.0680	0.0626	0.7590	0.5680
C to Z ↑	0.0595	0.0576	1.3815	1.0348
D to Z ↓	0.0697	0.0641	0.7594	0.5679
D to Z ↑	0.0573	0.0556	1.3825	1.0345

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.572e-07	3.032e-12
X17_P16	2.172e-07	3.536e-12
X25_P16	3.417e-07	4.290e-12
X33_P16	4.082e-07	4.545e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	5.596e-04	7.128e-04	1.058e-03	1.236e-03
B (output stable)	4.990e-04	6.614e-04	9.679e-04	1.111e-03
C (output stable)	5.434e-04	6.670e-04	1.011e-03	1.144e-03
D (output stable)	4.887e-04	5.962e-04	8.563e-04	9.589e-04
A to Z	4.033e-03	6.054e-03	9.390e-03	1.136e-02
B to Z	3.883e-03	5.923e-03	9.185e-03	1.108e-02
C to Z	4.127e-03	5.944e-03	8.801e-03	1.063e-02
D to Z	3.989e-03	5.787e-03	8.578e-03	1.035e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

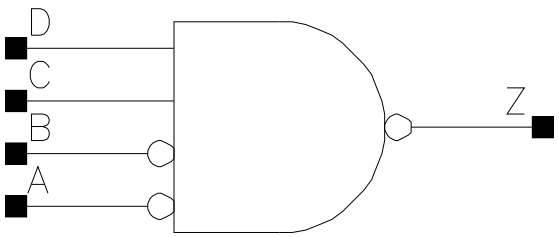
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	-4.799e-06	-9.268e-06	-2.413e-05	-2.985e-05
B (output stable)	-4.625e-06	-8.305e-06	-2.213e-05	-2.671e-05
C (output stable)	4.491e-06	9.232e-06	2.534e-05	3.093e-05
D (output stable)	5.280e-08	6.041e-08	1.216e-07	1.094e-07
A to Z	-2.137e-06	-3.826e-06	-8.857e-06	-1.113e-05
B to Z	-1.827e-06	-3.478e-06	-8.581e-06	-1.095e-05
C to Z	-3.343e-07	-5.126e-07	-5.380e-07	-1.178e-06
D to Z	-1.628e-07	-1.113e-07	-5.190e-07	-4.267e-07

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X12_P16	1.200	1.496	1.7952
X18_P16	1.200	2.040	2.4480
X24_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0011	0.0011	0.0021	0.0019
B	0.0011	0.0015	0.0021	0.0020
C	0.0009	0.0017	0.0025	0.0034
D	0.0008	0.0016	0.0024	0.0033

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X12_P16	X6_P16	X12_P16
A to Z ↓	0.0497	0.0665	5.5818	2.8897
A to Z ↑	0.0297	0.0355	4.0475	2.0361
B to Z ↓	0.0479	0.0651	5.5849	2.8897
B to Z ↑	0.0274	0.0339	4.0442	2.0342
C to Z ↓	0.0181	0.0189	5.6146	2.8936
C to Z ↑	0.0229	0.0226	4.3770	2.0720

D to Z ↓	0.0172	0.0160	5.6463	2.9124
D to Z ↑	0.0201	0.0187	4.4021	2.0871
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0573	0.0643	1.9762	1.5026
A to Z ↑	0.0318	0.0397	1.3725	1.0310
B to Z ↓	0.0540	0.0618	1.9762	1.5032
B to Z ↑	0.0298	0.0380	1.3708	1.0296
C to Z ↓	0.0189	0.0193	1.9853	1.5049
C to Z ↑	0.0224	0.0227	1.4012	1.0472
D to Z ↓	0.0167	0.0169	1.9954	1.5143
D to Z ↑	0.0191	0.0190	1.4308	1.0558

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P16	1.397e-07	2.528e-12
X12_P16	2.107e-07	3.536e-12
X18_P16	3.454e-07	4.545e-12
X24_P16	3.817e-07	5.300e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	8.815e-04	1.468e-03	2.209e-03	2.689e-03
B (output stable)	6.857e-04	1.241e-03	1.700e-03	2.230e-03
C (output stable)	4.824e-05	1.130e-04	1.733e-04	2.369e-04
D (output stable)	2.657e-05	1.122e-04	1.239e-04	1.917e-04
A to Z	3.703e-03	7.017e-03	1.041e-02	1.364e-02
B to Z	3.309e-03	6.525e-03	9.309e-03	1.263e-02
C to Z	1.279e-03	2.594e-03	3.774e-03	5.243e-03
D to Z	9.730e-04	1.707e-03	2.652e-03	3.582e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

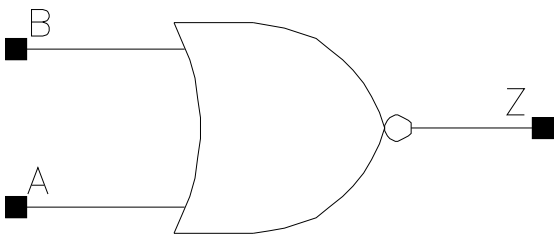
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	-4.135e-06	-7.766e-06	-1.319e-05	-1.281e-05
B (output stable)	-1.524e-07	4.716e-07	3.334e-07	9.713e-07
C (output stable)	-4.879e-09	5.173e-07	2.764e-07	9.397e-07
D (output stable)	-2.959e-08	-9.548e-07	-9.591e-07	-2.091e-06
A to Z	-3.523e-06	-7.895e-06	-1.122e-05	-1.210e-05
B to Z	-5.692e-07	-1.280e-07	-5.200e-08	1.890e-07
C to Z	4.180e-07	-6.100e-07	4.910e-07	-1.411e-06
D to Z	4.610e-07	4.660e-07	2.800e-08	6.090e-07

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.408	0.4896
X5_P16	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X10_P16	1.200	0.680	0.8160
X14_P16	1.200	0.680	0.8160
X17_P16	1.200	0.952	1.1424
X21_P16	1.200	0.952	1.1424
X24_P16	1.200	1.224	1.4688
X27_P16	1.200	1.224	1.4688
X34_P16	1.200	1.496	1.7952
X40_P16	1.200	1.360	1.6320
X41_P16	1.200	1.768	2.1216
X49_P16	1.200	1.496	1.7952
X53_P16	1.200	1.904	2.2848
X55_P16	1.200	2.312	2.7744
X57_P16	1.200	1.904	2.2848
X65_P16	1.200	2.040	2.4480
X84_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P16	X5_P16	X7_P16	X10_P16
A	0.0006	0.0007	0.0009	0.0015
B	0.0006	0.0007	0.0009	0.0013
	X14_P16	X17_P16	X21_P16	X24_P16

A	0.0019	0.0024	0.0027	0.0032
B	0.0017	0.0021	0.0025	0.0030
	X27_P16	X34_P16	X40_P16	X41_P16
A	0.0035	0.0045	0.0010	0.0055
B	0.0033	0.0041	0.0011	0.0050
	X49_P16	X53_P16	X55_P16	X57_P16
A	0.0010	0.0011	0.0072	0.0011
B	0.0011	0.0010	0.0067	0.0010
	X65_P16	X84_P16		
A	0.0011	0.0012		
B	0.0010	0.0011		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X5_P16**	**X3_P16**	**X5_P16**
A to Z ↓	0.0135	0.0128	4.1129	2.9860
A to Z ↑	0.0277	0.0259	17.2121	12.5016
B to Z ↓	0.0121	0.0111	4.2187	3.0141
B to Z ↑	0.0262	0.0238	17.2911	12.5429
	X7_P16	**X10_P16**	**X7_P16**	**X10_P16**
A to Z ↓	0.0124	0.0130	2.1971	1.4285
A to Z ↑	0.0246	0.0274	8.8082	5.8774
B to Z ↓	0.0105	0.0100	2.2275	1.4451
B to Z ↑	0.0222	0.0210	8.8425	5.9118
	X14_P16	**X17_P16**	**X14_P16**	**X17_P16**
A to Z ↓	0.0126	0.0129	1.0872	0.8751
A to Z ↑	0.0260	0.0262	4.3505	3.5186
B to Z ↓	0.0097	0.0104	1.1007	0.8852
B to Z ↑	0.0200	0.0214	4.3770	3.5332
	X21_P16	**X24_P16**	**X21_P16**	**X24_P16**
A to Z ↓	0.0128	0.0127	0.7460	0.6363
A to Z ↑	0.0255	0.0258	2.9263	2.5497
B to Z ↓	0.0103	0.0100	0.7548	0.6445
B to Z ↑	0.0208	0.0206	2.9397	2.5614
	X27_P16	**X34_P16**	**X27_P16**	**X34_P16**
A to Z ↓	0.0126	0.0130	0.5642	0.4565
A to Z ↑	0.0253	0.0256	2.2399	1.7843
B to Z ↓	0.0099	0.0103	0.5718	0.4624
B to Z ↑	0.0201	0.0207	2.2515	1.7923
	X40_P16	**X41_P16**	**X40_P16**	**X41_P16**
A to Z ↓	0.0453	0.0128	0.4605	0.3801
A to Z ↑	0.0703	0.0255	0.8510	1.4783
B to Z ↓	0.0438	0.0100	0.4606	0.3854
B to Z ↑	0.0698	0.0201	0.8506	1.4859
	X49_P16	**X53_P16**	**X49_P16**	**X53_P16**
A to Z ↓	0.0477	0.0489	0.3833	0.3507
A to Z ↑	0.0722	0.0837	0.7065	0.6545
B to Z ↓	0.0462	0.0474	0.3833	0.3504
B to Z ↑	0.0716	0.0825	0.7076	0.6545
	X55_P16	**X57_P16**	**X55_P16**	**X57_P16**
A to Z ↓	0.0129	0.0492	0.2875	0.3301
A to Z ↑	0.0255	0.0838	1.1134	0.6083

B to Z ↓	0.0101	0.0477	0.2920	0.3293
B to Z ↑	0.0202	0.0826	1.1185	0.6083
	X65_P16	**X84_P16**	**X65_P16**	**X84_P16**
A to Z ↓	0.0506	0.0530	0.2900	0.2314
A to Z ↑	0.0847	0.0847	0.5325	0.4218
B to Z ↓	0.0491	0.0517	0.2895	0.2314
B to Z ↑	0.0835	0.0840	0.5321	0.4218

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P16	4.214e-08	1.520e-12
X5_P16	5.597e-08	1.520e-12
X7_P16	7.496e-08	1.520e-12
X10_P16	1.150e-07	2.025e-12
X14_P16	1.490e-07	2.024e-12
X17_P16	1.870e-07	2.529e-12
X21_P16	2.203e-07	2.528e-12
X24_P16	2.584e-07	3.030e-12
X27_P16	2.915e-07	3.030e-12
X34_P16	3.628e-07	3.534e-12
X40_P16	3.764e-07	3.286e-12
X41_P16	4.341e-07	4.048e-12
X49_P16	4.223e-07	3.538e-12
X53_P16	4.900e-07	4.294e-12
X55_P16	5.766e-07	5.059e-12
X57_P16	5.094e-07	4.294e-12
X65_P16	5.554e-07	4.546e-12
X84_P16	6.669e-07	5.042e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	2.259e-05	3.096e-05	4.322e-05	8.726e-05
B (output stable)	1.127e-07	1.971e-07	4.699e-07	9.564e-06
A to Z	6.933e-04	8.407e-04	1.098e-03	1.958e-03
B to Z	4.822e-04	5.491e-04	6.855e-04	9.460e-04
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	1.111e-04	1.421e-04	1.727e-04	1.914e-04
B (output stable)	1.484e-05	1.079e-05	1.318e-05	1.171e-05
A to Z	2.397e-03	3.040e-03	3.487e-03	4.111e-03
B to Z	1.152e-03	1.646e-03	1.853e-03	2.095e-03
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	2.148e-04	2.865e-04	4.348e-05	3.458e-04
B (output stable)	1.548e-05	1.405e-05	1.042e-06	2.397e-05
A to Z	4.534e-03	5.738e-03	1.133e-02	6.888e-03
B to Z	2.279e-03	3.063e-03	1.096e-02	3.416e-03
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	4.405e-05	4.469e-05	4.592e-04	4.469e-05
B (output stable)	1.118e-06	1.445e-06	2.956e-05	1.445e-06
A to Z	1.269e-02	1.574e-02	9.115e-03	1.605e-02
B to Z	1.232e-02	1.534e-02	4.556e-03	1.565e-02
	X65_P16	X84_P16		

A (output stable)	4.477e-05	4.553e-05		
B (output stable)	1.544e-06	1.841e-06		
A to Z	1.725e-02	2.029e-02		
B to Z	1.684e-02	1.981e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

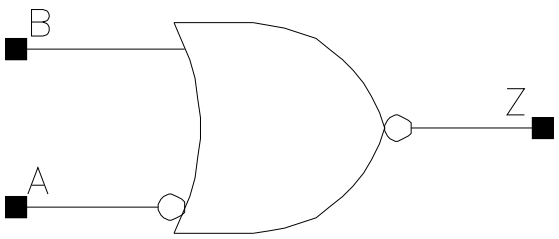
Pin Cycle (vdds)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	-2.183e-06	-2.926e-06	-4.031e-06	-1.071e-05
B (output stable)	2.252e-07	5.382e-07	1.484e-06	1.307e-05
A to Z	-2.779e-06	-3.233e-06	-4.589e-06	-1.612e-05
B to Z	-2.694e-07	1.412e-07	1.953e-07	-1.370e-08
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	-1.369e-05	-1.079e-05	-1.277e-05	-2.040e-05
B (output stable)	2.257e-05	9.874e-06	1.331e-05	1.763e-05
A to Z	-1.927e-05	-1.555e-05	-1.772e-05	-2.812e-05
B to Z	3.656e-07	-2.537e-07	2.017e-07	4.846e-07
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	-2.286e-05	-2.040e-05	-4.032e-06	-3.144e-05
B (output stable)	2.539e-05	1.658e-05	1.391e-06	3.109e-05
A to Z	-3.109e-05	-2.548e-05	-5.492e-06	-4.237e-05
B to Z	7.772e-07	3.510e-07	-6.320e-07	8.290e-07
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	-3.987e-06	-4.058e-06	-4.007e-05	-4.058e-06
B (output stable)	1.337e-06	2.406e-06	3.683e-05	2.406e-06
A to Z	-6.062e-06	-5.662e-06	-5.434e-05	-5.800e-06
B to Z	-7.100e-07	-8.590e-07	8.900e-07	-1.290e-06
	X65_P16	X84_P16		
A (output stable)	-4.056e-06	-4.181e-06		
B (output stable)	2.402e-06	2.503e-06		
A to Z	-6.526e-06	-5.539e-06		
B to Z	-1.653e-06	-6.690e-07		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X7_P16	1.200	0.680	0.8160
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X41_P16	1.200	2.312	2.7744
X55_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X7_P16	X13_P16
A	0.0009	0.0009	0.0009	0.0012
B	0.0006	0.0009	0.0009	0.0016
	X27_P16	X41_P16	X55_P16	
A	0.0022	0.0033	0.0043	
B	0.0033	0.0050	0.0066	

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0377	0.0415	3.9816	2.6111
A to Z ↑	0.0346	0.0343	17.1242	8.7735
B to Z ↓	0.0124	0.0118	4.1917	2.7765
B to Z ↑	0.0265	0.0223	17.2676	8.8528

	X7_P16	X13_P16	X7_P16	X13_P16
A to Z ↓	0.0419	0.0380	2.0781	1.1360
A to Z ↑	0.0372	0.0352	8.6706	4.5858
B to Z ↓	0.0109	0.0101	2.1272	1.1572
B to Z ↑	0.0234	0.0214	8.7293	4.6293
	X27_P16	**X41_P16**	**X27_P16**	**X41_P16**
A to Z ↓	0.0368	0.0375	0.5439	0.3686
A to Z ↑	0.0338	0.0341	2.2001	1.4745
B to Z ↓	0.0100	0.0100	0.5737	0.3875
B to Z ↑	0.0206	0.0203	2.2189	1.4869
	X55_P16		**X55_P16**	
A to Z ↓	0.0372		0.2791	
A to Z ↑	0.0339		1.1115	
B to Z ↓	0.0100		0.2937	
B to Z ↑	0.0203		1.1212	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P16	6.539e-08	1.771e-12
X6_P16	8.973e-08	1.771e-12
X7_P16	1.037e-07	2.023e-12
X13_P16	1.914e-07	2.527e-12
X27_P16	3.821e-07	3.786e-12
X41_P16	5.664e-07	5.046e-12
X55_P16	7.506e-07	6.305e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	1.064e-03	1.357e-03	1.428e-03	2.276e-03
B (output stable)	2.287e-07	2.880e-07	3.507e-07	6.480e-07
A to Z	1.853e-03	2.569e-03	2.981e-03	4.987e-03
B to Z	4.965e-04	6.853e-04	8.155e-04	1.281e-03
	X27_P16	X41_P16	X55_P16	
A (output stable)	4.425e-03	6.739e-03	8.904e-03	
B (output stable)	1.240e-06	1.905e-06	2.584e-06	
A to Z	9.861e-03	1.468e-02	1.947e-02	
B to Z	2.455e-03	3.570e-03	4.701e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

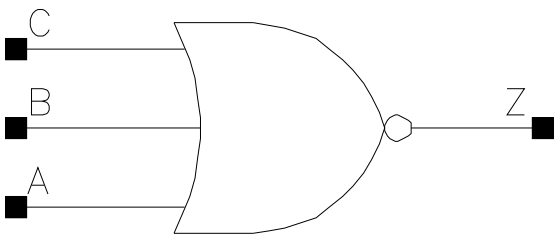
Pin Cycle (vdds)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	-2.311e-06	-4.004e-06	-7.701e-06	-1.300e-05
B (output stable)	1.479e-07	1.766e-07	2.348e-07	3.666e-07
A to Z	-2.661e-06	-5.132e-06	-1.124e-05	-1.867e-05
B to Z	-2.456e-07	-5.534e-07	4.360e-08	1.045e-07
	X27_P16	X41_P16	X55_P16	
A (output stable)	-2.151e-05	-3.111e-05	-3.980e-05	
B (output stable)	4.410e-07	6.920e-07	8.490e-07	
A to Z	-3.086e-05	-4.473e-05	-5.747e-05	
B to Z	5.685e-07	8.170e-07	9.890e-07	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X9_P16	1.200	0.952	1.1424
X13_P16	1.200	0.952	1.1424
X16_P16	1.200	1.360	1.6320
X19_P16	1.200	1.496	1.7952
X22_P16	1.200	1.768	2.1216
X25_P16	1.200	1.904	2.2848
X37_P16	1.200	2.584	3.1008
X49_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P16	X6_P16	X9_P16	X13_P16
A	0.0007	0.0009	0.0014	0.0017
B	0.0007	0.0009	0.0016	0.0019
C	0.0007	0.0009	0.0013	0.0017
	X16_P16	X19_P16	X22_P16	X25_P16
A	0.0024	0.0027	0.0032	0.0035
B	0.0024	0.0031	0.0033	0.0041
C	0.0022	0.0024	0.0030	0.0032
	X37_P16	X49_P16		
A	0.0053	0.0072		
B	0.0055	0.0073		

C	0.0048	0.0066		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0150	0.0143	3.0348	2.2338
A to Z ↑	0.0388	0.0358	19.0633	13.4704
B to Z ↓	0.0143	0.0136	3.0348	2.2328
B to Z ↑	0.0367	0.0336	19.0760	13.4553
C to Z ↓	0.0128	0.0118	3.0645	2.2581
C to Z ↑	0.0321	0.0285	19.1289	13.4921
	X9_P16	**X13_P16**	**X9_P16**	**X13_P16**
A to Z ↓	0.0147	0.0144	1.4806	1.1393
A to Z ↑	0.0386	0.0364	8.9508	6.6508
B to Z ↓	0.0140	0.0135	1.4388	1.0886
B to Z ↑	0.0386	0.0357	8.9550	6.6685
C to Z ↓	0.0113	0.0109	1.4503	1.1060
C to Z ↑	0.0266	0.0250	8.9628	6.6837
	X16_P16	**X19_P16**	**X16_P16**	**X19_P16**
A to Z ↓	0.0146	0.0143	0.8840	0.7460
A to Z ↑	0.0375	0.0368	5.3854	4.4543
B to Z ↓	0.0142	0.0139	0.8856	0.7283
B to Z ↑	0.0365	0.0367	5.3819	4.4576
C to Z ↓	0.0117	0.0113	0.8889	0.7595
C to Z ↑	0.0278	0.0262	5.3955	4.4645
	X22_P16	**X25_P16**	**X22_P16**	**X25_P16**
A to Z ↓	0.0145	0.0143	0.6509	0.5692
A to Z ↑	0.0369	0.0368	3.8399	3.3439
B to Z ↓	0.0139	0.0138	0.6384	0.5460
B to Z ↑	0.0361	0.0368	3.8391	3.3452
C to Z ↓	0.0111	0.0110	0.6444	0.5686
C to Z ↑	0.0259	0.0251	3.8565	3.3601
	X37_P16	**X49_P16**	**X37_P16**	**X49_P16**
A to Z ↓	0.0144	0.0146	0.3917	0.2973
A to Z ↑	0.0359	0.0360	2.2423	1.6846
B to Z ↓	0.0137	0.0139	0.3867	0.2939
B to Z ↑	0.0348	0.0348	2.2397	1.6858
C to Z ↓	0.0113	0.0115	0.3921	0.2977
C to Z ↑	0.0252	0.0256	2.2465	1.6915

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	7.447e-08	1.772e-12
X6_P16	9.949e-08	1.771e-12
X9_P16	1.540e-07	2.529e-12
X13_P16	1.992e-07	2.529e-12
X16_P16	2.512e-07	3.282e-12
X19_P16	3.012e-07	3.534e-12
X22_P16	3.485e-07	4.038e-12
X25_P16	3.986e-07	4.290e-12
X37_P16	5.779e-07	5.554e-12

X49_P16	7.687e-07	7.081e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	1.506e-04	2.126e-04	4.206e-04	5.402e-04
B (output stable)	8.260e-06	1.076e-05	1.581e-04	1.718e-04
C (output stable)	1.837e-06	2.374e-06	2.267e-05	2.334e-05
A to Z	1.301e-03	1.651e-03	2.742e-03	3.395e-03
B to Z	1.040e-03	1.288e-03	2.288e-03	2.752e-03
C to Z	7.490e-04	8.681e-04	1.218e-03	1.455e-03
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	6.242e-04	7.846e-04	9.144e-04	1.083e-03
B (output stable)	1.511e-04	2.205e-04	2.699e-04	3.464e-04
C (output stable)	2.273e-05	2.725e-05	3.561e-05	4.028e-05
A to Z	4.387e-03	5.170e-03	6.005e-03	6.844e-03
B to Z	3.551e-03	4.255e-03	4.871e-03	5.657e-03
C to Z	2.136e-03	2.355e-03	2.678e-03	2.929e-03
	X37_P16	X49_P16		
A (output stable)	1.529e-03	2.027e-03		
B (output stable)	3.918e-04	5.055e-04		
C (output stable)	5.839e-05	7.514e-05		
A to Z	9.902e-03	1.319e-02		
B to Z	7.905e-03	1.052e-02		
C to Z	4.270e-03	5.792e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

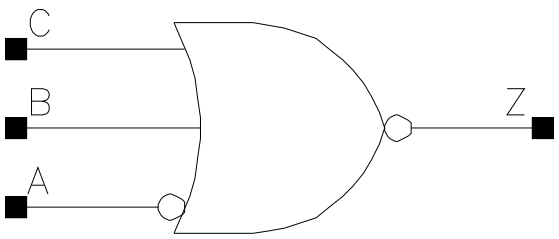
Pin Cycle (vdds)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	-2.211e-05	-3.099e-05	-6.461e-05	-8.329e-05
B (output stable)	6.809e-06	9.623e-06	-1.255e-06	5.330e-07
C (output stable)	9.304e-06	1.289e-05	4.855e-05	5.912e-05
A to Z	-6.405e-06	-8.772e-06	-2.002e-05	-2.541e-05
B to Z	-3.643e-06	-5.205e-06	-1.823e-05	-2.152e-05
C to Z	-3.760e-07	-7.980e-08	-3.030e-07	-2.983e-07
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	-8.016e-05	-1.063e-04	-1.277e-04	-1.561e-04
B (output stable)	1.713e-05	2.418e-05	1.620e-05	2.537e-05
C (output stable)	4.219e-05	6.026e-05	7.805e-05	9.793e-05
A to Z	-2.326e-05	-3.109e-05	-3.870e-05	-4.597e-05
B to Z	-1.673e-05	-2.345e-05	-2.991e-05	-3.612e-05
C to Z	-2.489e-07	-2.705e-07	-4.333e-07	-4.228e-07
	X37_P16	X49_P16		
A (output stable)	-2.105e-04	-2.747e-04		
B (output stable)	3.606e-05	4.881e-05		
C (output stable)	1.197e-04	1.536e-04		
A to Z	-6.247e-05	-7.978e-05		
B to Z	-4.655e-05	-5.893e-05		
C to Z	-8.900e-07	-1.517e-06		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.680	0.8160
X13_P16	1.200	1.224	1.4688
X19_P16	1.200	1.496	1.7952
X25_P16	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0009	0.0012	0.0012	0.0022
B	0.0009	0.0019	0.0027	0.0036
C	0.0009	0.0017	0.0024	0.0033

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X13_P16**	**X6_P16**	**X13_P16**
A to Z ↓	0.0417	0.0397	2.1733	1.2237
A to Z ↑	0.0464	0.0457	13.5898	6.6559
B to Z ↓	0.0138	0.0135	2.2454	1.0951
B to Z ↑	0.0340	0.0353	13.6214	6.6563
C to Z ↓	0.0120	0.0108	2.2623	1.1070
C to Z ↑	0.0291	0.0250	13.6546	6.6810
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0453	0.0398	0.7413	0.5621

A to Z ↑	0.0489	0.0455	4.4691	3.3491
B to Z ↓	0.0140	0.0137	0.7632	0.5684
B to Z ↑	0.0344	0.0344	4.4762	3.3558
C to Z ↓	0.0113	0.0109	0.7608	0.5726
C to Z ↑	0.0263	0.0251	4.4894	3.3652

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P16	1.232e-07	2.024e-12
X13_P16	2.456e-07	3.033e-12
X19_P16	3.382e-07	3.536e-12
X25_P16	4.834e-07	4.809e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	1.630e-03	3.058e-03	4.143e-03	6.019e-03
B (output stable)	-1.184e-05	3.713e-06	-5.454e-06	-2.780e-07
C (output stable)	3.813e-06	3.034e-05	2.228e-05	4.465e-05
A to Z	3.182e-03	6.215e-03	8.637e-03	1.205e-02
B to Z	1.297e-03	2.732e-03	3.932e-03	5.234e-03
C to Z	8.896e-04	1.458e-03	2.338e-03	2.883e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

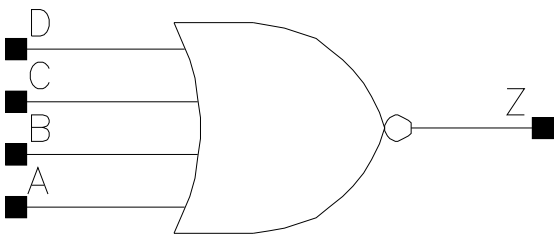
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	-4.393e-05	-1.169e-04	-1.427e-04	-2.114e-04
B (output stable)	1.548e-05	3.306e-05	5.190e-05	6.896e-05
C (output stable)	7.560e-06	3.401e-05	3.047e-05	5.267e-05
A to Z	-6.719e-06	-1.930e-05	-2.207e-05	-3.312e-05
B to Z	-3.721e-06	-1.275e-05	-1.249e-05	-1.830e-05
C to Z	-5.712e-07	-6.051e-07	-2.567e-07	-1.104e-06

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	1.904	2.2848
X32_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X32_P16
A	0.0007	0.0007	0.0008	0.0010
B	0.0008	0.0007	0.0009	0.0012
C	0.0007	0.0007	0.0009	0.0010
D	0.0007	0.0007	0.0009	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0480	0.0471	2.1338	1.0497
A to Z ↑	0.0764	0.0826	4.2047	2.0704
B to Z ↓	0.0464	0.0461	2.1344	1.0500
B to Z ↑	0.0752	0.0817	4.2063	2.0716
C to Z ↓	0.0470	0.0468	2.1335	1.0480
C to Z ↑	0.0770	0.0844	4.2085	2.0721

D to Z ↓	0.0465	0.0464	2.1295	1.0490
D to Z ↑	0.0765	0.0843	4.2073	2.0725
	X25_P16	**X32_P16**	**X25_P16**	**X32_P16**
A to Z ↓	0.0483	0.0505	0.7327	0.5764
A to Z ↑	0.0813	0.0784	1.4175	1.0753
B to Z ↓	0.0472	0.0495	0.7323	0.5762
B to Z ↑	0.0809	0.0778	1.4186	1.0749
C to Z ↓	0.0461	0.0491	0.7301	0.5758
C to Z ↑	0.0803	0.0789	1.4171	1.0753
D to Z ↓	0.0448	0.0469	0.7310	0.5758
D to Z ↑	0.0796	0.0778	1.4163	1.0739

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.655e-07	3.033e-12
X17_P16	2.450e-07	3.295e-12
X25_P16	3.583e-07	4.292e-12
X32_P16	4.361e-07	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	5.652e-04	7.034e-04	9.665e-04	1.211e-03
B (output stable)	4.671e-04	6.114e-04	8.595e-04	1.060e-03
C (output stable)	5.390e-04	6.501e-04	9.626e-04	1.241e-03
D (output stable)	4.225e-04	5.416e-04	7.952e-04	1.015e-03
A to Z	3.914e-03	5.905e-03	8.982e-03	1.131e-02
B to Z	3.702e-03	5.713e-03	8.693e-03	1.098e-02
C to Z	3.956e-03	5.858e-03	8.424e-03	1.067e-02
D to Z	3.739e-03	5.665e-03	8.151e-03	1.029e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

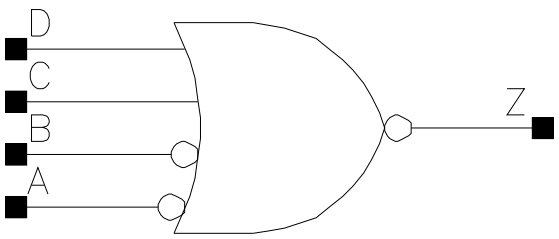
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	-2.098e-06	-1.997e-06	-2.809e-06	-3.796e-06
B (output stable)	-4.489e-08	-2.226e-08	-2.224e-08	4.487e-08
C (output stable)	-6.283e-06	-6.038e-06	-8.807e-06	-1.181e-05
D (output stable)	3.170e-06	3.150e-06	4.487e-06	5.955e-06
A to Z	-2.414e-06	-2.419e-06	-3.423e-06	-4.774e-06
B to Z	-9.600e-09	-4.158e-07	-3.071e-07	-1.787e-07
C to Z	-2.173e-06	-2.329e-06	-3.603e-06	-4.547e-06
D to Z	9.300e-09	-1.672e-07	-5.459e-07	-4.993e-07

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X13_P16	1.200	1.496	1.7952
X19_P16	1.200	2.040	2.4480
X25_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0011	0.0012	0.0022	0.0021
B	0.0012	0.0016	0.0022	0.0022
C	0.0009	0.0018	0.0026	0.0035
D	0.0009	0.0017	0.0024	0.0032

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X13_P16	X6_P16	X13_P16
A to Z ↓	0.0359	0.0447	2.1215	1.0585
A to Z ↑	0.0463	0.0566	13.0944	6.7357
B to Z ↓	0.0335	0.0430	2.1203	1.0579
B to Z ↑	0.0463	0.0572	13.0971	6.7340
C to Z ↓	0.0143	0.0136	2.2938	1.0910
C to Z ↑	0.0342	0.0354	13.1299	6.7584

D to Z ↓	0.0121	0.0109	2.2947	1.1031
D to Z ↑	0.0288	0.0256	13.1616	6.7718
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0394	0.0431	0.7288	0.5498
A to Z ↑	0.0513	0.0552	4.4675	3.3709
B to Z ↓	0.0364	0.0403	0.7279	0.5492
B to Z ↑	0.0507	0.0550	4.4707	3.3710
C to Z ↓	0.0140	0.0137	0.7628	0.5716
C to Z ↑	0.0343	0.0342	4.4760	3.3774
D to Z ↓	0.0113	0.0108	0.7611	0.5724
D to Z ↑	0.0263	0.0246	4.4885	3.3850

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P16	1.681e-07	2.528e-12
X13_P16	2.760e-07	3.537e-12
X19_P16	4.358e-07	4.545e-12
X25_P16	5.340e-07	5.308e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	9.403e-04	1.749e-03	2.596e-03	3.244e-03
B (output stable)	7.940e-04	1.537e-03	2.168e-03	2.802e-03
C (output stable)	-3.368e-06	1.709e-05	3.396e-05	5.614e-05
D (output stable)	1.781e-06	2.186e-05	1.856e-05	4.390e-05
A to Z	3.774e-03	7.157e-03	1.067e-02	1.369e-02
B to Z	3.490e-03	6.840e-03	9.902e-03	1.301e-02
C to Z	1.352e-03	2.712e-03	3.913e-03	5.107e-03
D to Z	9.203e-04	1.498e-03	2.338e-03	2.764e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

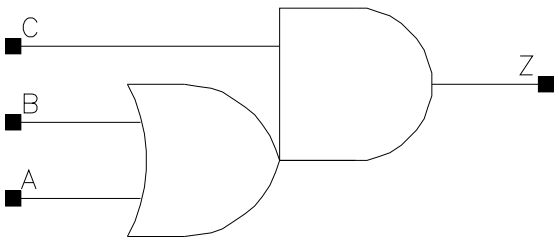
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	-2.234e-05	-5.352e-05	-7.117e-05	-1.014e-04
B (output stable)	-1.816e-05	-4.444e-05	-5.720e-05	-8.229e-05
C (output stable)	1.820e-05	2.917e-05	4.965e-05	6.432e-05
D (output stable)	6.952e-06	2.711e-05	2.616e-05	4.376e-05
A to Z	-8.543e-06	-2.307e-05	-2.785e-05	-4.146e-05
B to Z	-1.140e-05	-3.482e-05	-3.966e-05	-6.084e-05
C to Z	-3.855e-06	-1.112e-05	-1.236e-05	-1.977e-05
D to Z	-5.860e-07	-3.101e-07	-2.946e-07	-5.739e-07

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0010	0.0010	0.0019
B	0.0012	0.0011	0.0022
C	0.0011	0.0012	0.0021

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0430	0.0507	2.2059	1.1041
A to Z ↑	0.0316	0.0353	4.2273	2.0759
B to Z ↓	0.0418	0.0500	2.2084	1.1038
B to Z ↑	0.0288	0.0330	4.2187	2.0717
C to Z ↓	0.0360	0.0402	2.1739	1.0784
C to Z ↑	0.0302	0.0334	4.2200	2.0722
	X33_P16		**X33_P16**	
A to Z ↓	0.0524		0.5634	
A to Z ↑	0.0376		1.0433	

B to Z ↓	0.0516		0.5638	
B to Z ↑	0.0347		1.0422	
C to Z ↓	0.0410		0.5483	
C to Z ↑	0.0346		1.0409	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.343e-07	2.024e-12
X17_P16	1.830e-07	2.276e-12
X33_P16	3.676e-07	3.787e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.144e-04	1.156e-04	2.370e-04
B (output stable)	1.087e-05	1.147e-05	2.037e-05
C (output stable)	4.719e-05	4.553e-05	9.814e-05
A to Z	2.826e-03	4.068e-03	8.400e-03
B to Z	2.433e-03	3.689e-03	7.656e-03
C to Z	3.099e-03	4.352e-03	8.890e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

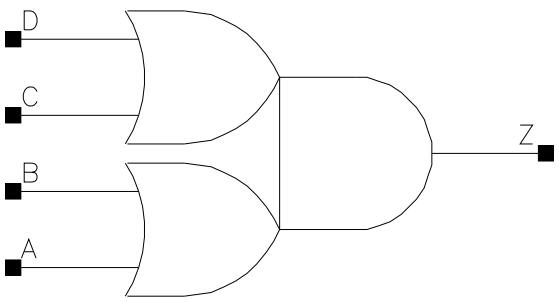
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-3.236e-06	-3.377e-06	-6.805e-06
B (output stable)	-1.497e-06	-1.563e-06	-3.178e-06
C (output stable)	2.151e-06	2.531e-06	4.408e-06
A to Z	-3.795e-06	-3.934e-06	-8.018e-06
B to Z	-3.045e-07	-4.178e-07	-1.029e-06
C to Z	-1.814e-06	-1.664e-06	-3.872e-06

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0010	0.0020
B	0.0007	0.0011	0.0020
C	0.0007	0.0011	0.0020
D	0.0007	0.0010	0.0021

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0730	0.0618	2.1700	1.0987
A to Z ↑	0.0432	0.0377	4.1381	2.0687
B to Z ↓	0.0729	0.0612	2.1715	1.0995
B to Z ↑	0.0418	0.0359	4.1362	2.0680

C to Z ↓	0.0637	0.0545	2.1594	1.0955
C to Z ↑	0.0419	0.0376	4.1364	2.0691
D to Z ↓	0.0622	0.0531	2.1611	1.0960
D to Z ↑	0.0397	0.0348	4.1339	2.0647
	X33_P16		**X33_P16**	
A to Z ↓	0.0624		0.5679	
A to Z ↑	0.0378		1.0406	
B to Z ↓	0.0596		0.5684	
B to Z ↑	0.0354		1.0387	
C to Z ↓	0.0542		0.5655	
C to Z ↑	0.0368		1.0392	
D to Z ↓	0.0510		0.5662	
D to Z ↑	0.0341		1.0375	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.183e-07	2.528e-12
X17_P16	2.230e-07	2.781e-12
X33_P16	4.398e-07	4.546e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.827e-05	3.507e-05	8.617e-05
B (output stable)	1.625e-05	2.191e-05	4.430e-05
C (output stable)	4.150e-05	8.093e-05	2.829e-04
D (output stable)	7.474e-05	9.299e-05	2.273e-04
A to Z	3.257e-03	5.189e-03	1.034e-02
B to Z	3.076e-03	4.813e-03	9.278e-03
C to Z	2.840e-03	4.556e-03	9.036e-03
D to Z	2.633e-03	4.165e-03	7.946e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

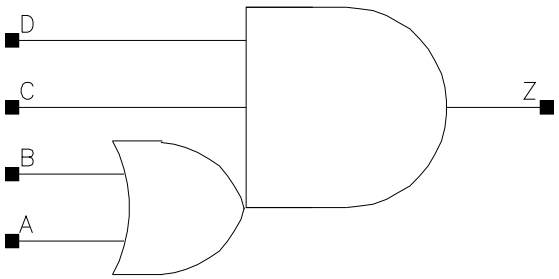
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-1.637e-06	-3.261e-06	-1.010e-05
B (output stable)	2.059e-07	-1.050e-06	-1.928e-06
C (output stable)	-6.967e-06	-1.334e-05	-4.751e-05
D (output stable)	3.217e-06	7.400e-06	2.959e-05
A to Z	-2.281e-06	-4.818e-06	-1.647e-05
B to Z	-4.714e-07	-1.585e-06	-4.687e-06
C to Z	-2.908e-06	-5.672e-06	-1.783e-05
D to Z	-9.626e-07	-1.857e-06	-6.100e-06

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	1.088	1.3056
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0007	0.0011	0.0017	0.0020
B	0.0007	0.0011	0.0017	0.0021
C	0.0008	0.0011	0.0018	0.0021
D	0.0007	0.0011	0.0018	0.0021

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0620	0.0580	2.2782	1.1115
A to Z ↑	0.0509	0.0470	4.2775	2.0755
B to Z ↓	0.0616	0.0557	2.2797	1.1124
B to Z ↑	0.0484	0.0431	4.2748	2.0736
C to Z ↓	0.0480	0.0446	2.2015	1.0805

C to Z ↑	0.0491	0.0446	4.2744	2.0719
D to Z ↓	0.0466	0.0430	2.2012	1.0793
D to Z ↑	0.0501	0.0455	4.2726	2.0709
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0603	0.0576	0.7573	0.5663
A to Z ↑	0.0480	0.0482	1.4072	1.0541
B to Z ↓	0.0578	0.0554	0.7583	0.5672
B to Z ↑	0.0445	0.0446	1.4040	1.0525
C to Z ↓	0.0468	0.0447	0.7357	0.5503
C to Z ↑	0.0460	0.0454	1.4043	1.0521
D to Z ↓	0.0444	0.0428	0.7339	0.5495
D to Z ↑	0.0457	0.0456	1.4049	1.0521

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.061e-07	2.275e-12
X17_P16	2.045e-07	2.783e-12
X25_P16	3.233e-07	4.293e-12
X33_P16	4.116e-07	4.537e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	5.232e-05	1.069e-04	1.979e-04	2.259e-04
B (output stable)	3.920e-05	9.510e-05	1.472e-04	1.698e-04
C (output stable)	9.013e-06	1.418e-05	5.074e-05	6.718e-05
D (output stable)	1.645e-05	3.888e-05	1.121e-04	1.155e-04
A to Z	2.714e-03	4.783e-03	7.674e-03	9.345e-03
B to Z	2.529e-03	4.275e-03	6.906e-03	8.388e-03
C to Z	3.006e-03	5.212e-03	8.556e-03	1.024e-02
D to Z	2.865e-03	4.948e-03	7.927e-03	9.583e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

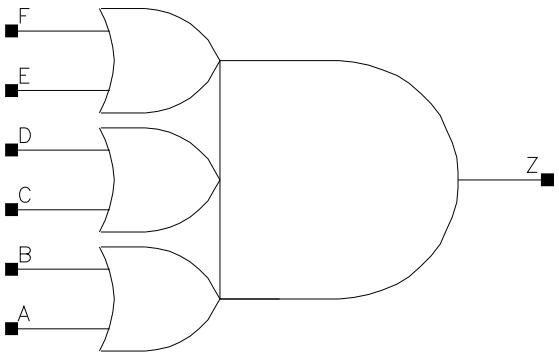
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	-1.537e-06	-4.198e-06	-4.205e-06	-5.982e-06
B (output stable)	-1.636e-06	-4.806e-06	-5.216e-06	-6.768e-06
C (output stable)	5.733e-07	5.939e-07	-2.836e-08	8.700e-09
D (output stable)	7.567e-07	7.422e-07	1.420e-09	-4.916e-08
A to Z	-2.377e-06	-7.507e-06	-9.542e-06	-1.272e-05
B to Z	-2.676e-07	-4.449e-07	-8.863e-07	-8.270e-07
C to Z	-8.030e-07	-2.318e-06	-3.655e-06	-4.538e-06
D to Z	-6.132e-07	-2.932e-06	-4.230e-06	-5.133e-06

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0010	0.0018
B	0.0007	0.0010	0.0019
C	0.0007	0.0010	0.0018
D	0.0007	0.0010	0.0020
E	0.0007	0.0010	0.0018
F	0.0007	0.0010	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0832	0.0714	2.3437	1.1380
A to Z ↑	0.0561	0.0508	4.2486	2.0877
B to Z ↓	0.0824	0.0712	2.3433	1.1380
B to Z ↑	0.0543	0.0491	4.2531	2.0888
C to Z ↓	0.0760	0.0672	2.3293	1.1359
C to Z ↑	0.0559	0.0502	4.2516	2.0881
D to Z ↓	0.0758	0.0667	2.3293	1.1364
D to Z ↑	0.0537	0.0481	4.2493	2.0876
E to Z ↓	0.0656	0.0587	2.3142	1.1303
E to Z ↑	0.0518	0.0474	4.2507	2.0862
F to Z ↓	0.0656	0.0579	2.3155	1.1311
F to Z ↑	0.0496	0.0449	4.2465	2.0853
	X33_P16		X33_P16	
A to Z ↓	0.0717		0.5829	
A to Z ↑	0.0520		1.0544	
B to Z ↓	0.0718		0.5830	
B to Z ↑	0.0490		1.0524	
C to Z ↓	0.0660		0.5793	
C to Z ↑	0.0512		1.0540	
D to Z ↓	0.0657		0.5796	
D to Z ↑	0.0484		1.0521	
E to Z ↓	0.0579		0.5767	
E to Z ↑	0.0485		1.0525	
F to Z ↓	0.0575		0.5770	
F to Z ↑	0.0455		1.0511	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.505e-07	3.033e-12
X17_P16	2.778e-07	3.292e-12
X33_P16	5.361e-07	5.554e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.685e-05	3.554e-05	5.837e-05
B (output stable)	6.686e-06	1.331e-05	2.168e-05
C (output stable)	2.967e-05	5.434e-05	1.076e-04
D (output stable)	3.116e-05	5.248e-05	1.092e-04
E (output stable)	2.610e-05	4.881e-05	9.136e-05
F (output stable)	1.023e-04	1.524e-04	2.922e-04
A to Z	3.740e-03	6.163e-03	1.192e-02
B to Z	3.542e-03	5.813e-03	1.129e-02
C to Z	3.401e-03	5.660e-03	1.091e-02
D to Z	3.218e-03	5.298e-03	1.024e-02
E to Z	2.962e-03	4.981e-03	9.641e-03
F to Z	2.786e-03	4.619e-03	8.973e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

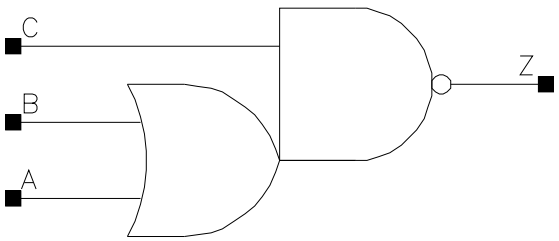
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	-1.213e-06	-2.877e-06	-3.953e-06
B (output stable)	-4.985e-07	-1.371e-06	-2.134e-06
C (output stable)	-3.290e-06	-6.994e-06	-1.316e-05
D (output stable)	9.599e-07	1.387e-06	2.201e-06
E (output stable)	-3.717e-06	-7.025e-06	-1.348e-05
F (output stable)	-1.109e-08	1.164e-06	7.706e-07
A to Z	-2.941e-06	-6.177e-06	-1.107e-05
B to Z	-1.332e-06	-3.103e-06	-5.276e-06
C to Z	-3.114e-06	-6.588e-06	-1.250e-05
D to Z	-1.229e-06	-2.663e-06	-5.732e-06
E to Z	-3.772e-06	-7.391e-06	-1.432e-05
F to Z	-1.704e-06	-3.259e-06	-6.364e-06

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X34_P16	1.200	2.720	3.2640
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X34_P16	X46_P16
A	0.0008	0.0026	0.0052	0.0067
B	0.0009	0.0024	0.0047	0.0063
C	0.0009	0.0027	0.0054	0.0070

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0168	0.0175	4.1858	1.3711
A to Z ↑	0.0258	0.0275	8.8020	2.9703
B to Z ↓	0.0139	0.0144	4.1169	1.3845
B to Z ↑	0.0235	0.0237	8.8363	2.9850
C to Z ↓	0.0164	0.0166	3.7899	1.2550
C to Z ↑	0.0234	0.0233	4.2319	1.4011
	X34_P16	**X46_P16**	**X34_P16**	**X46_P16**
A to Z ↓	0.0182	0.0181	0.6993	0.5337

A to Z ↑	0.0283	0.0280	1.4805	1.1347
B to Z ↓	0.0147	0.0147	0.7095	0.5432
B to Z ↑	0.0239	0.0239	1.4880	1.1404
C to Z ↓	0.0170	0.0169	0.6427	0.4915
C to Z ↑	0.0237	0.0235	0.6999	0.5340

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P16	9.001e-08	1.772e-12
X17_P16	2.691e-07	3.284e-12
X34_P16	5.386e-07	5.802e-12
X46_P16	7.146e-07	7.324e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	1.030e-04	3.432e-04	7.066e-04	8.954e-04
B (output stable)	1.173e-05	3.799e-05	8.346e-05	1.041e-04
C (output stable)	3.785e-05	1.433e-04	2.895e-04	3.517e-04
A to Z	1.215e-03	3.994e-03	8.336e-03	1.075e-02
B to Z	8.118e-04	2.488e-03	5.164e-03	6.692e-03
C to Z	1.461e-03	4.519e-03	9.397e-03	1.213e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

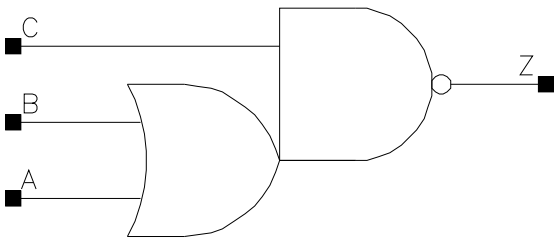
Pin Cycle (vdds)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	-2.690e-06	-9.424e-06	-2.214e-05	-2.785e-05
B (output stable)	-1.482e-06	-4.870e-06	-1.169e-05	-1.446e-05
C (output stable)	-6.000e-10	4.113e-06	1.079e-05	1.458e-05
A to Z	-3.370e-06	-1.148e-05	-2.979e-05	-3.205e-05
B to Z	-2.229e-07	-5.850e-07	-2.473e-06	-3.640e-06
C to Z	-1.861e-06	-6.383e-06	-1.520e-05	-1.860e-05

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.544	0.6528
X11_P16	1.200	0.952	1.1424
X17_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X17_P16	X23_P16
A	0.0009	0.0018	0.0027	0.0037
B	0.0009	0.0018	0.0025	0.0034
C	0.0009	0.0017	0.0025	0.0034
	X46_P16			
A	0.0074			
B	0.0068			
C	0.0068			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0178	0.0181	4.2357	1.9747
A to Z ↑	0.0318	0.0321	9.2367	4.3551
B to Z ↓	0.0157	0.0159	4.1609	1.9220

B to Z ↑	0.0301	0.0305	9.2670	4.3697
C to Z ↓	0.0141	0.0140	3.9470	1.8324
C to Z ↑	0.0182	0.0181	4.5276	2.1264
	X17_P16	**X23_P16**	**X17_P16**	**X23_P16**
A to Z ↓	0.0175	0.0183	1.3754	1.0146
A to Z ↑	0.0307	0.0333	2.8857	2.1964
B to Z ↓	0.0152	0.0158	1.3710	1.0153
B to Z ↑	0.0286	0.0297	2.8969	2.2041
C to Z ↓	0.0136	0.0139	1.2911	0.9507
C to Z ↑	0.0172	0.0176	1.4125	1.0739
	X46_P16		**X46_P16**	
A to Z ↓	0.0182		0.5302	
A to Z ↑	0.0327		1.1078	
B to Z ↓	0.0156		0.5254	
B to Z ↑	0.0292		1.1120	
C to Z ↓	0.0140		0.4949	
C to Z ↑	0.0173		0.5425	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P16	1.024e-07	1.772e-12
X11_P16	2.142e-07	2.525e-12
X17_P16	3.184e-07	3.283e-12
X23_P16	4.292e-07	4.289e-12
X46_P16	8.463e-07	7.319e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	2.977e-05	6.787e-05	9.711e-05	1.661e-04
B (output stable)	1.108e-05	2.577e-05	3.671e-05	6.941e-05
C (output stable)	2.705e-04	6.296e-04	7.769e-04	1.199e-03
A to Z	1.611e-03	3.475e-03	4.806e-03	7.240e-03
B to Z	1.212e-03	2.648e-03	3.503e-03	5.061e-03
C to Z	8.202e-04	1.786e-03	2.399e-03	3.534e-03
	X46_P16			
A (output stable)	3.191e-04			
B (output stable)	1.382e-04			
C (output stable)	2.182e-03			
A to Z	1.398e-02			
B to Z	9.646e-03			
C to Z	6.742e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	-2.591e-06	-4.508e-06	-8.409e-06	-1.149e-05
B (output stable)	-1.442e-06	-3.044e-06	-4.684e-06	-7.818e-06
C (output stable)	-1.500e-08	-2.855e-06	-2.039e-07	-6.123e-06
A to Z	-4.050e-06	-9.338e-06	-1.353e-05	-2.184e-05
B to Z	-7.253e-07	-2.586e-06	-3.082e-06	-4.356e-06
C to Z	-1.140e-06	-2.683e-06	-3.722e-06	-7.985e-06

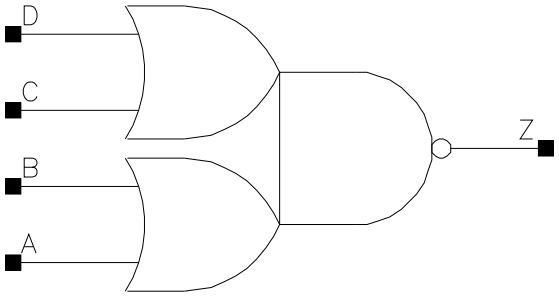
	X46_P16			
A (output stable)	-2.041e-05			
B (output stable)	-1.415e-05			
C (output stable)	-1.170e-05			
A to Z	-4.323e-05			
B to Z	-8.077e-06			
C to Z	-1.084e-05			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0009	0.0018	0.0027	0.0037
B	0.0009	0.0017	0.0024	0.0033
C	0.0008	0.0017	0.0025	0.0035
D	0.0008	0.0016	0.0023	0.0032
	X42_P16			
A	0.0074			
B	0.0067			
C	0.0070			
D	0.0064			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0193	0.0204	3.8739	1.9290
A to Z ↑	0.0364	0.0366	9.6930	4.4500
B to Z ↓	0.0174	0.0180	3.7874	1.9311
B to Z ↑	0.0343	0.0327	9.7117	4.4654
C to Z ↓	0.0173	0.0184	3.9386	1.9468
C to Z ↑	0.0270	0.0288	9.5062	4.4662
D to Z ↓	0.0147	0.0150	3.8449	1.9597
D to Z ↑	0.0244	0.0234	9.5513	4.4899
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0198	0.0201	1.3254	0.9530
A to Z ↑	0.0349	0.0359	2.9908	2.2019
B to Z ↓	0.0178	0.0176	1.3287	0.9501
B to Z ↑	0.0320	0.0324	3.0014	2.2090
C to Z ↓	0.0181	0.0181	1.3380	0.9620
C to Z ↑	0.0274	0.0278	3.0026	2.2061
D to Z ↓	0.0151	0.0149	1.3569	0.9660
D to Z ↑	0.0230	0.0231	3.0213	2.2195
	X42_P16		**X42_P16**	
A to Z ↓	0.0204		0.5005	
A to Z ↑	0.0360		1.1180	
B to Z ↓	0.0179		0.4943	
B to Z ↑	0.0327		1.1219	
C to Z ↓	0.0189		0.5062	
C to Z ↑	0.0282		1.1147	
D to Z ↓	0.0154		0.5026	
D to Z ↑	0.0235		1.1215	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P16	1.293e-07	2.022e-12
X10_P16	2.598e-07	3.285e-12
X15_P16	3.788e-07	4.042e-12
X21_P16	5.311e-07	5.302e-12
X42_P16	1.051e-06	9.336e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	3.228e-05	8.388e-05	1.263e-04	1.759e-04
B (output stable)	1.592e-05	3.798e-05	4.764e-05	6.342e-05
C (output stable)	7.974e-05	2.972e-04	3.550e-04	5.266e-04
D (output stable)	8.058e-05	2.081e-04	2.581e-04	3.682e-04
A to Z	1.963e-03	4.465e-03	6.171e-03	8.707e-03
B to Z	1.578e-03	3.336e-03	4.659e-03	6.549e-03
C to Z	1.327e-03	3.172e-03	4.358e-03	6.076e-03
D to Z	9.499e-04	2.006e-03	2.810e-03	3.892e-03
	X42_P16			
A (output stable)	3.534e-04			
B (output stable)	1.306e-04			
C (output stable)	1.041e-03			
D (output stable)	7.287e-04			

A to Z	1.727e-02			
B to Z	1.301e-02			
C to Z	1.221e-02			
D to Z	7.863e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

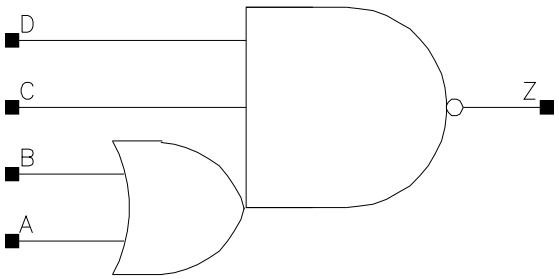
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	-2.955e-06	-9.823e-06	-9.840e-06	-1.718e-05
B (output stable)	-8.464e-07	-1.721e-06	-1.882e-06	-3.039e-06
C (output stable)	-1.265e-05	-5.099e-05	-4.359e-05	-8.000e-05
D (output stable)	6.981e-06	3.150e-05	2.480e-05	4.653e-05
A to Z	-5.025e-06	-1.481e-05	-1.764e-05	-2.558e-05
B to Z	-1.272e-06	-4.463e-06	-4.471e-06	-7.732e-06
C to Z	-4.882e-06	-1.725e-05	-1.780e-05	-3.072e-05
D to Z	-1.562e-06	-5.586e-06	-5.733e-06	-1.006e-05
	X42_P16			
A (output stable)	-3.032e-05			
B (output stable)	-5.896e-06			
C (output stable)	-1.403e-04			
D (output stable)	8.185e-05			
A to Z	-4.628e-05			
B to Z	-1.379e-05			
C to Z	-5.443e-05			
D to Z	-1.858e-05			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X21_P16	1.200	2.448	2.9376
X31_P16	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X21_P16	X31_P16
A	0.0009	0.0017	0.0034	0.0051
B	0.0011	0.0016	0.0030	0.0046
C	0.0009	0.0018	0.0036	0.0053
D	0.0009	0.0017	0.0034	0.0050

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0232	0.0223	5.4340	2.9042
A to Z ↑	0.0331	0.0309	8.7732	4.4150
B to Z ↓	0.0205	0.0182	5.4740	2.9167
B to Z ↑	0.0310	0.0266	8.8195	4.4339
C to Z ↓	0.0219	0.0226	5.1240	2.7382

C to Z ↑	0.0278	0.0272	4.1154	2.0701
D to Z ↓	0.0228	0.0220	5.1408	2.7469
D to Z ↑	0.0264	0.0249	4.1633	2.0736
	X21_P16	**X31_P16**	**X21_P16**	**X31_P16**
A to Z ↓	0.0227	0.0230	1.5175	1.0305
A to Z ↑	0.0304	0.0304	2.2058	1.4798
B to Z ↓	0.0183	0.0185	1.5260	1.0394
B to Z ↑	0.0261	0.0261	2.2165	1.4873
C to Z ↓	0.0225	0.0227	1.4324	0.9739
C to Z ↑	0.0268	0.0269	1.0482	0.7058
D to Z ↓	0.0222	0.0224	1.4369	0.9770
D to Z ↑	0.0247	0.0247	1.0496	0.7052

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P16	1.050e-07	2.276e-12
X10_P16	2.070e-07	3.283e-12
X21_P16	4.071e-07	5.302e-12
X31_P16	6.073e-07	7.321e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	1.025e-04	2.400e-04	4.618e-04	6.789e-04
B (output stable)	9.193e-05	1.842e-04	3.514e-04	5.145e-04
C (output stable)	1.748e-05	4.484e-05	7.260e-05	9.839e-05
D (output stable)	3.867e-05	1.185e-04	2.127e-04	3.120e-04
A to Z	1.894e-03	3.290e-03	6.415e-03	9.554e-03
B to Z	1.367e-03	2.179e-03	4.175e-03	6.277e-03
C to Z	2.281e-03	4.349e-03	8.377e-03	1.247e-02
D to Z	2.034e-03	3.609e-03	6.961e-03	1.038e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

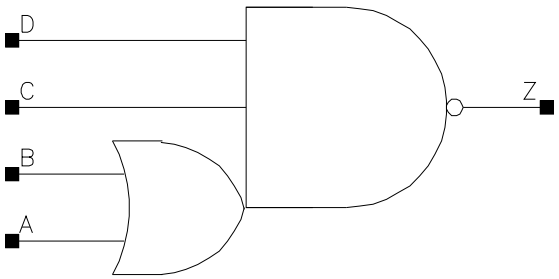
Pin Cycle (vdds)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	-3.836e-06	-7.163e-06	-1.336e-05	-1.855e-05
B (output stable)	-5.636e-06	-8.388e-06	-1.444e-05	-2.054e-05
C (output stable)	5.815e-07	9.743e-07	2.114e-06	2.580e-06
D (output stable)	8.168e-07	1.663e-06	3.311e-06	4.221e-06
A to Z	-7.754e-06	-1.131e-05	-1.898e-05	-2.924e-05
B to Z	-5.580e-08	2.930e-07	-5.800e-07	-7.320e-07
C to Z	-2.849e-06	-3.544e-06	-6.496e-06	-9.242e-06
D to Z	-2.891e-06	-3.650e-06	-4.600e-06	-9.707e-06

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0010	0.0019	0.0028	0.0037
B	0.0009	0.0017	0.0025	0.0034
C	0.0009	0.0017	0.0026	0.0034
D	0.0009	0.0017	0.0025	0.0033

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0229	0.0246	5.5499	2.8916
A to Z ↑	0.0368	0.0395	8.5440	4.3444
B to Z ↓	0.0203	0.0214	5.4548	2.8927
B to Z ↑	0.0354	0.0365	8.5644	4.3546
C to Z ↓	0.0184	0.0205	5.2275	2.7445

C to Z ↑	0.0224	0.0236	4.1810	2.1140
D to Z ↓	0.0179	0.0185	5.2645	2.7637
D to Z ↑	0.0198	0.0200	4.2125	2.1322
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0244	0.0245	1.9948	1.5030
A to Z ↑	0.0383	0.0389	2.9220	2.2119
B to Z ↓	0.0213	0.0212	1.9874	1.4997
B to Z ↑	0.0357	0.0363	2.9301	2.2176
C to Z ↓	0.0201	0.0204	1.8894	1.4240
C to Z ↑	0.0228	0.0231	1.4079	1.0605
D to Z ↓	0.0184	0.0187	1.9030	1.4334
D to Z ↑	0.0194	0.0197	1.4199	1.0690

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P16	1.291e-07	2.276e-12
X10_P16	2.588e-07	3.284e-12
X15_P16	3.780e-07	4.046e-12
X21_P16	5.138e-07	5.552e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	1.978e-05	5.180e-05	7.584e-05	1.020e-04
B (output stable)	2.810e-05	9.801e-05	1.243e-04	1.812e-04
C (output stable)	6.459e-05	1.163e-04	1.834e-04	2.364e-04
D (output stable)	1.631e-04	4.977e-04	6.240e-04	9.088e-04
A to Z	2.238e-03	4.881e-03	6.966e-03	9.461e-03
B to Z	1.814e-03	3.799e-03	5.381e-03	7.344e-03
C to Z	1.397e-03	3.172e-03	4.408e-03	6.079e-03
D to Z	1.093e-03	2.323e-03	3.267e-03	4.458e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

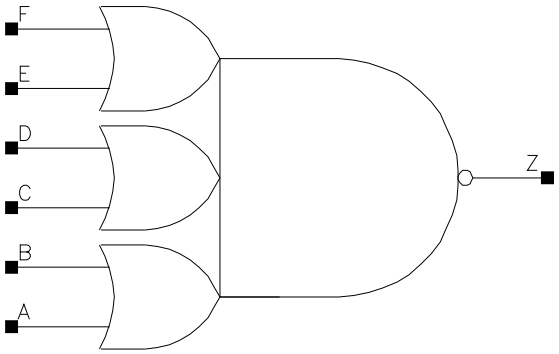
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	-2.358e-06	-6.335e-06	-6.122e-06	-1.130e-05
B (output stable)	-2.482e-06	-7.354e-06	-7.401e-06	-1.304e-05
C (output stable)	-6.268e-09	2.181e-06	1.050e-06	3.912e-06
D (output stable)	-9.240e-09	-2.246e-06	-2.685e-06	-4.261e-06
A to Z	-4.543e-06	-1.105e-05	-1.122e-05	-1.974e-05
B to Z	-8.100e-08	-1.010e-07	-8.860e-07	-1.820e-07
C to Z	-9.213e-07	-4.287e-06	-3.873e-06	-5.517e-06
D to Z	-9.690e-07	-3.387e-06	-3.382e-06	-5.930e-06

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	1.088	1.3056
X9_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X9_P16
A	0.0008	0.0019
B	0.0007	0.0017
C	0.0007	0.0018
D	0.0007	0.0016
E	0.0007	0.0017
F	0.0007	0.0016

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X9_P16	X3_P16	X9_P16
A to Z ↓	0.0283	0.0296	6.3845	2.6232
A to Z ↑	0.0483	0.0459	12.0357	4.3635
B to Z ↓	0.0267	0.0266	6.4218	2.6227
B to Z ↑	0.0480	0.0429	12.0592	4.3719
C to Z ↓	0.0272	0.0279	6.4208	2.6319
C to Z ↑	0.0418	0.0397	12.0496	4.3518
D to Z ↓	0.0251	0.0247	6.4580	2.6343
D to Z ↑	0.0411	0.0363	12.0815	4.3638
E to Z ↓	0.0233	0.0244	6.4603	2.6344
E to Z ↑	0.0325	0.0316	12.0917	4.3584
F to Z ↓	0.0212	0.0206	6.5033	2.6393
F to Z ↑	0.0313	0.0270	12.1504	4.3794

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P16	1.454e-07	2.780e-12
X9_P16	3.741e-07	4.545e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P16	X9_P16
A (output stable)	2.245e-05	7.762e-05
B (output stable)	8.575e-06	3.171e-05
C (output stable)	3.964e-05	1.756e-04
D (output stable)	4.493e-05	1.571e-04
E (output stable)	3.492e-05	1.532e-04
F (output stable)	1.402e-04	3.356e-04
A to Z	2.594e-03	6.751e-03
B to Z	2.327e-03	5.655e-03
C to Z	2.109e-03	5.492e-03
D to Z	1.839e-03	4.443e-03
E to Z	1.516e-03	4.128e-03
F to Z	1.245e-03	3.017e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

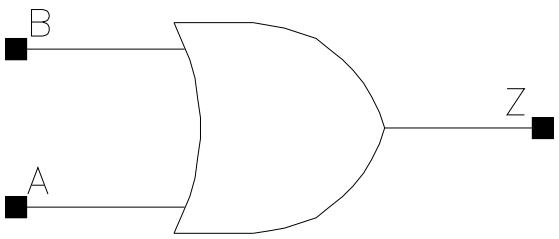
Pin Cycle (vdds)	X3_P16	X9_P16
A (output stable)	-2.065e-06	-8.283e-06
B (output stable)	-9.461e-07	-4.016e-06
C (output stable)	-5.081e-06	-2.486e-05
D (output stable)	1.070e-06	9.820e-06
E (output stable)	-5.079e-06	-2.493e-05
F (output stable)	7.960e-07	5.417e-06
A to Z	-4.091e-06	-1.822e-05
B to Z	-1.954e-06	-8.363e-06
C to Z	-4.503e-06	-1.950e-05
D to Z	-2.022e-06	-7.735e-06
E to Z	-4.900e-06	-2.279e-05
F to Z	-1.992e-06	-9.809e-06

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X33_P16	1.200	1.360	1.6320
X50_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P16	X16_P16	X33_P16	X50_P16
A	0.0008	0.0010	0.0020	0.0020
B	0.0007	0.0010	0.0020	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0571	0.0509	2.2244	1.1237
A to Z ↑	0.0302	0.0310	4.1811	2.1061
B to Z ↓	0.0553	0.0495	2.2257	1.1241
B to Z ↑	0.0288	0.0292	4.1825	2.1063
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0520	0.0613	0.5566	0.3855
A to Z ↑	0.0307	0.0308	1.0269	0.6927
B to Z ↓	0.0489	0.0584	0.5568	0.3857
B to Z ↑	0.0286	0.0290	1.0259	0.6922

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	8.028e-08	1.768e-12
X16_P16	1.355e-07	2.023e-12
X33_P16	2.785e-07	3.283e-12
X50_P16	3.715e-07	3.789e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	2.355e-05	4.540e-05	9.922e-05	9.412e-05
B (output stable)	1.984e-07	6.910e-07	2.112e-05	1.711e-05
A to Z	2.535e-03	4.021e-03	8.399e-03	1.111e-02
B to Z	2.308e-03	3.628e-03	7.290e-03	1.005e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

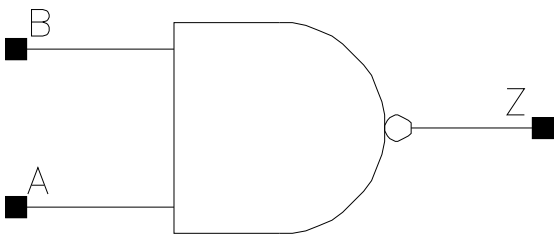
Pin Cycle (vdds)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	-2.203e-06	-4.058e-06	-1.208e-05	-1.198e-05
B (output stable)	3.227e-07	2.301e-06	2.052e-05	1.916e-05
A to Z	-2.769e-06	-5.053e-06	-1.997e-05	-1.818e-05
B to Z	-2.819e-07	-1.028e-07	-8.475e-07	-1.462e-06

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X16_P16	1.200	0.952	1.1424
X24_P16	1.200	1.088	1.3056
X32_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P16	X16_P16	X24_P16	X32_P16
A	0.0011	0.0011	0.0011	0.0010
B	0.0012	0.0012	0.0012	0.0012

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0416	0.0438	2.1327	1.1135
A to Z ↑	0.0469	0.0483	4.2161	2.1515
B to Z ↓	0.0428	0.0451	2.1320	1.1136
B to Z ↑	0.0448	0.0455	4.2160	2.1520
	X24_P16	**X32_P16**	**X24_P16**	**X32_P16**
A to Z ↓	0.0488	0.0496	0.7566	0.5703
A to Z ↑	0.0515	0.0535	1.4368	1.0741
B to Z ↓	0.0501	0.0513	0.7575	0.5704
B to Z ↑	0.0486	0.0515	1.4377	1.0734

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.564e-07	2.274e-12
X16_P16	1.918e-07	2.522e-12
X24_P16	2.268e-07	2.781e-12
X32_P16	3.020e-07	3.027e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	1.640e-05	1.651e-05	1.660e-05	1.687e-05
B (output stable)	6.798e-05	6.818e-05	6.828e-05	6.841e-05
A to Z	4.969e-03	5.753e-03	7.222e-03	9.686e-03
B to Z	4.699e-03	5.499e-03	6.980e-03	9.436e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

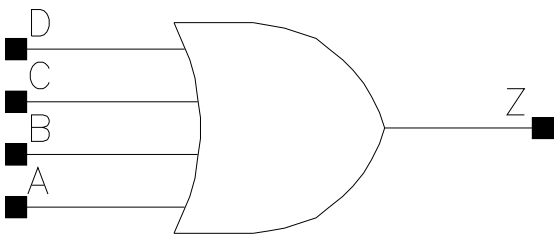
Pin Cycle (vdds)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	-3.004e-08	-2.572e-08	-2.529e-08	-3.346e-08
B (output stable)	-7.200e-09	-7.000e-09	-7.000e-09	-3.100e-09
A to Z	-6.621e-07	-6.778e-07	-9.603e-07	-5.928e-07
B to Z	-4.314e-07	-3.522e-07	-2.837e-07	-3.638e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P16	1.200	2.176	2.6112
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P16	X27_P16
A	0.0018	0.0020
B	0.0016	0.0020
C	0.0018	0.0021
D	0.0017	0.0021

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P16	X27_P16	X20_P16	X27_P16
A to Z ↓	0.0572	0.0593	1.3612	1.0193
A to Z ↑	0.0324	0.0312	1.3745	1.0256
B to Z ↓	0.0546	0.0561	1.3620	1.0178
B to Z ↑	0.0309	0.0293	1.3745	1.0246
C to Z ↓	0.0554	0.0574	1.3598	1.0174
C to Z ↑	0.0309	0.0303	1.3776	1.0286
D to Z ↓	0.0529	0.0546	1.3629	1.0187
D to Z ↑	0.0293	0.0286	1.3782	1.0270

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X20_P16	3.702e-07	4.795e-12
X27_P16	5.146e-07	5.551e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X20_P16	X27_P16
A (output stable)	1.944e-03	2.644e-03
B (output stable)	1.614e-03	2.177e-03
C (output stable)	1.834e-03	2.597e-03
D (output stable)	1.355e-03	1.938e-03
A to Z	8.142e-03	1.135e-02
B to Z	7.363e-03	1.021e-02
C to Z	7.061e-03	9.671e-03
D to Z	6.277e-03	8.645e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

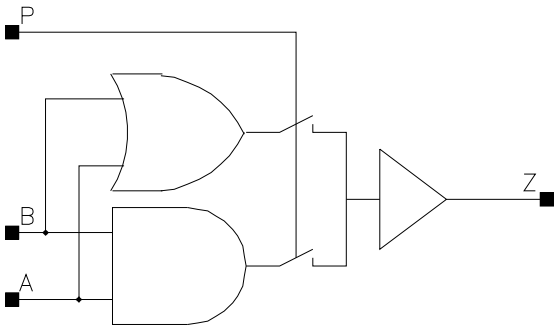
Pin Cycle (vdds)	X20_P16	X27_P16
A (output stable)	-6.361e-06	-1.205e-05
B (output stable)	-1.633e-07	6.836e-07
C (output stable)	-2.139e-05	-4.599e-05
D (output stable)	1.181e-05	2.652e-05
A to Z	-7.609e-06	-1.470e-05
B to Z	-5.910e-07	-4.200e-07
C to Z	-7.568e-06	-1.467e-05
D to Z	-2.310e-07	3.320e-07

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X16_P16	1.200	1.224	1.4688
X25_P16	1.200	2.040	2.4480
X33_P16	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0013	0.0019	0.0034	0.0034
B	0.0012	0.0018	0.0037	0.0037
P	0.0007	0.0010	0.0019	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0688	0.0625	2.2765	1.1130
A to Z ↑	0.0406	0.0376	4.2337	2.1174
B to Z ↓	0.0676	0.0616	2.2950	1.1238
B to Z ↑	0.0420	0.0390	4.2382	2.1208
P to Z ↓	0.0613	0.0561	2.3017	1.1259
P to Z ↑	0.0406	0.0378	4.2354	2.1181
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**

A to Z ↓	0.0598	0.0644	0.7575	0.5756
A to Z ↑	0.0375	0.0397	1.4238	1.0658
B to Z ↓	0.0587	0.0628	0.7633	0.5797
B to Z ↑	0.0392	0.0411	1.4254	1.0674
P to Z ↓	0.0543	0.0586	0.7656	0.5814
P to Z ↑	0.0374	0.0394	1.4231	1.0658

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	1.357e-07	2.528e-12
X16_P16	2.519e-07	3.032e-12
X25_P16	4.499e-07	4.545e-12
X33_P16	4.952e-07	4.793e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	3.441e-05	7.100e-05	1.330e-04	1.307e-04
B (output stable)	1.600e-04	2.868e-04	5.170e-04	5.253e-04
P (output stable)	1.140e-04	1.889e-04	3.320e-04	3.382e-04
A to Z	2.904e-03	4.866e-03	8.503e-03	9.750e-03
B to Z	2.809e-03	4.698e-03	8.141e-03	9.421e-03
P to Z	2.514e-03	4.256e-03	7.475e-03	8.729e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

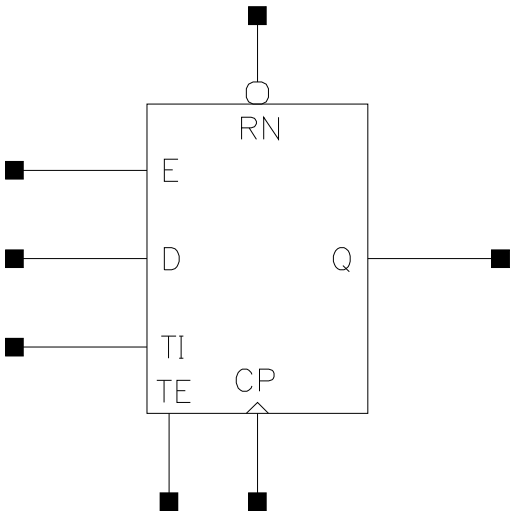
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	-1.660e-06	-4.815e-06	-8.572e-06	-8.364e-06
B (output stable)	-2.369e-05	-4.266e-05	-5.582e-05	-5.776e-05
P (output stable)	7.250e-06	2.168e-05	2.801e-05	2.875e-05
A to Z	-4.486e-06	-7.804e-06	-1.040e-05	-1.052e-05
B to Z	-3.526e-06	-6.570e-06	-7.930e-06	-9.204e-06
P to Z	-1.507e-06	-2.849e-06	-6.076e-06	-6.352e-06

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.488	5.3856
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0011	0.0011
RN	0.0009	0.0007	0.0008	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to Q ↓	0.1305	0.0639	5.1805	2.2290
CP to Q ↑	0.0939	0.0790	8.6661	4.1919
RN to Q ↓	0.1040	0.0871	4.2389	2.3989
	X17_P16	X33_P16	X17_P16	X33_P16
CP to Q ↓	0.1067	0.1129	1.0691	0.5658
CP to Q ↑	0.1304	0.1370	2.0560	1.0487
RN to Q ↓	0.1444	0.1503	1.0655	0.5640

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1997	0.1315	0.1309	0.1309
CP ↑	min_pulse_width to CP	0.1187	0.0501	0.0415	0.0453
D ↓	hold_rising to CP	-0.2132	-0.1142	-0.1142	-0.1138
D ↑	hold_rising to CP	-0.0965	-0.0365	-0.0361	-0.0361
D ↓	setup_rising to CP	0.2901	0.1803	0.1834	0.1834
D ↑	setup_rising to CP	0.1392	0.0783	0.0762	0.0762
E ↓	hold_rising to CP	-0.1186	-0.1155	-0.1186	-0.1186
E ↑	hold_rising to CP	-0.0946	-0.0390	-0.0390	-0.0390
E ↓	setup_rising to CP	0.2440	0.2412	0.2416	0.2412
E ↑	setup_rising to CP	0.2738	0.1859	0.1859	0.1859
RN ↓	min_pulse_width to RN	0.1062	0.1187	0.1018	0.1018
RN ↑	recovery_rising to CP	0.0318	0.0315	0.0321	0.0296
RN ↑	removal_rising to CP	-0.0222	-0.0149	-0.0149	-0.0149
TE ↓	hold_rising to CP	-0.0911	-0.0725	-0.0725	-0.0725
TE ↑	hold_rising to CP	-0.0654	-0.0409	-0.0406	-0.0406
TE ↓	setup_rising to CP	0.1922	0.1386	0.1390	0.1365
TE ↑	setup_rising to CP	0.3443	0.2414	0.2445	0.2445
TI ↓	hold_rising to CP	-0.2651	-0.1507	-0.1515	-0.1515
TI ↑	hold_rising to CP	-0.0761	-0.0443	-0.0441	-0.0436
TI ↓	setup_rising to CP	0.3443	0.2243	0.2258	0.2258
TI ↑	setup_rising to CP	0.1171	0.0846	0.0836	0.0836

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	4.340e-07	9.676e-12
X8_P16	4.508e-07	9.080e-12
X17_P16	5.228e-07	9.585e-12
X33_P16	6.256e-07	1.009e-11

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

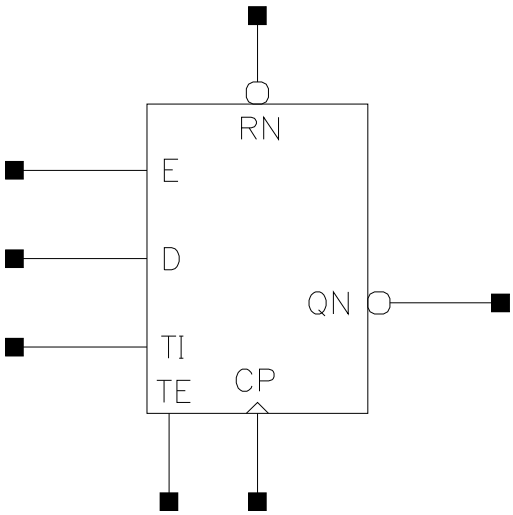
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.625e-03	4.668e-03	4.679e-03	4.685e-03
Clock 100Mhz Data 25Mhz	7.452e-03	7.664e-03	8.430e-03	9.283e-03
Clock 100Mhz Data 50Mhz	1.028e-02	1.066e-02	1.218e-02	1.388e-02
Clock = 0 Data 100Mhz	6.385e-03	6.315e-03	6.293e-03	6.283e-03
Clock = 1 Data 100Mhz	2.544e-03	2.565e-03	2.573e-03	2.577e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.624	5.5488
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0011	0.0011
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to QN ↓	0.1175	0.1094	4.1025	2.1365
CP to QN ↑	0.1403	0.0817	8.5034	4.0791
RN to QN ↑	0.1233	0.1217	8.4800	4.0759
	X17_P16	X33_P16	X17_P16	X33_P16
CP to QN ↓	0.1032	0.1093	1.0695	0.5655
CP to QN ↑	0.0878	0.0958	2.0584	1.0505
RN to QN ↑	0.1224	0.1351	2.0623	1.0535

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1997	0.1315	0.1315	0.1315
CP ↑	min_pulse_width to CP	0.0829	0.0415	0.0512	0.0549
D ↓	hold_rising to CP	-0.2156	-0.1142	-0.1142	-0.1142
D ↑	hold_rising to CP	-0.0965	-0.0361	-0.0365	-0.0365
D ↓	setup_rising to CP	0.2926	0.1831	0.1831	0.1831
D ↑	setup_rising to CP	0.1392	0.0787	0.0783	0.0783
E ↓	hold_rising to CP	-0.1182	-0.1186	-0.1155	-0.1155
E ↑	hold_rising to CP	-0.0946	-0.0390	-0.0387	-0.0390
E ↓	setup_rising to CP	0.2489	0.2416	0.2412	0.2412
E ↑	setup_rising to CP	0.2756	0.1859	0.1859	0.1859
RN ↓	min_pulse_width to RN	0.1062	0.1045	0.1182	0.1279
RN ↑	recovery_rising to CP	0.0318	0.0345	0.0314	0.0314
RN ↑	removal_rising to CP	-0.0222	-0.0174	-0.0149	-0.0149
TE ↓	hold_rising to CP	-0.0911	-0.0725	-0.0697	-0.0672
TE ↑	hold_rising to CP	-0.0654	-0.0406	-0.0409	-0.0409
TE ↓	setup_rising to CP	0.1922	0.1365	0.1365	0.1365
TE ↑	setup_rising to CP	0.3443	0.2445	0.2445	0.2445
TI ↓	hold_rising to CP	-0.2664	-0.1515	-0.1507	-0.1466
TI ↑	hold_rising to CP	-0.0756	-0.0441	-0.0443	-0.0402
TI ↓	setup_rising to CP	0.3443	0.2258	0.2258	0.2258
TI ↑	setup_rising to CP	0.1156	0.0846	0.0887	0.0887

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	4.298e-07	9.677e-12
X8_P16	4.414e-07	9.332e-12
X17_P16	5.129e-07	9.584e-12
X33_P16	6.021e-07	1.009e-11

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

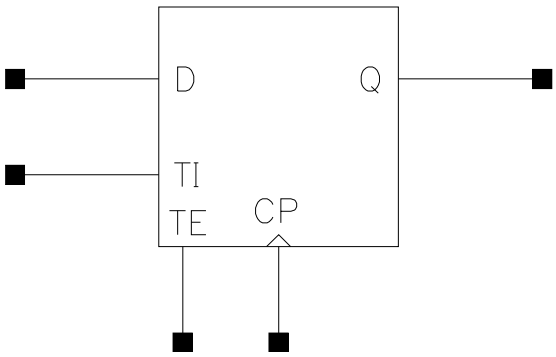
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.598e-03	4.639e-03	4.648e-03	4.653e-03
Clock 100Mhz Data 25Mhz	7.453e-03	7.706e-03	8.345e-03	9.140e-03
Clock 100Mhz Data 50Mhz	1.031e-02	1.077e-02	1.204e-02	1.363e-02
Clock = 0 Data 100Mhz	6.396e-03	6.322e-03	6.299e-03	6.288e-03
Clock = 1 Data 100Mhz	2.545e-03	2.562e-03	2.570e-03	2.573e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.400	4.0800
X8_P16	1.200	3.128	3.7536
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1051	0.0592	4.8401	2.2227
CP to Q ↑	0.0843	0.0719	8.7194	4.1448
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0877	0.0967	1.0453	0.5547
CP to Q ↑	0.1304	0.1377	2.0520	1.0448

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1707	0.1745	0.1745	0.1745
CP ↑	min_pulse_width to CP	0.0829	0.0452	0.0405	0.0405
D ↓	hold_rising to CP	-0.1305	-0.0631	-0.0631	-0.0631
D ↑	hold_rising to CP	-0.0405	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1876	0.1214	0.1214	0.1214
D ↑	setup_rising to CP	0.0728	0.0390	0.0390	0.0390
TE ↓	hold_rising to CP	-0.0716	-0.0499	-0.0496	-0.0496
TE ↑	hold_rising to CP	-0.0525	-0.0335	-0.0335	-0.0335
TE ↓	setup_rising to CP	0.1559	0.1197	0.1197	0.1197
TE ↑	setup_rising to CP	0.3031	0.2414	0.2414	0.2414
TI ↓	hold_rising to CP	-0.2509	-0.1584	-0.1577	-0.1577
TI ↑	hold_rising to CP	-0.0609	-0.0357	-0.0352	-0.0352
TI ↓	setup_rising to CP	0.3115	0.2355	0.2314	0.2314
TI ↑	setup_rising to CP	0.0961	0.0664	0.0664	0.0664

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	3.345e-07	7.064e-12
X8_P16	3.504e-07	6.560e-12
X17_P16	4.411e-07	7.317e-12
X33_P16	5.251e-07	7.820e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

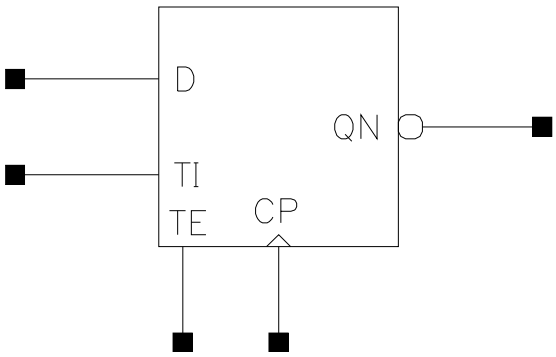
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.127e-03	4.142e-03	4.143e-03	4.144e-03
Clock 100Mhz Data 25Mhz	6.146e-03	6.278e-03	7.017e-03	7.678e-03
Clock 100Mhz Data 50Mhz	8.165e-03	8.413e-03	9.890e-03	1.121e-02
Clock = 0 Data 100Mhz	5.140e-03	4.899e-03	4.817e-03	4.777e-03
Clock = 1 Data 100Mhz	1.440e-03	7.620e-04	5.362e-04	4.232e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.536	4.2432
X8_P16	1.200	3.264	3.9168
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1111	0.1196	4.6981	2.2301
CP to QN ↑	0.1121	0.0748	8.6689	4.0953
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0882	0.0978	1.0470	0.5557
CP to QN ↑	0.0771	0.0845	2.0529	1.0450

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1707	0.1745	0.1745	0.1745
CP ↑	min_pulse_width to CP	0.0635	0.0405	0.0453	0.0501
D ↓	hold_rising to CP	-0.1305	-0.0631	-0.0631	-0.0631
D ↑	hold_rising to CP	-0.0405	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1821	0.1214	0.1214	0.1214
D ↑	setup_rising to CP	0.0728	0.0390	0.0390	0.0390
TE ↓	hold_rising to CP	-0.0716	-0.0496	-0.0499	-0.0499
TE ↑	hold_rising to CP	-0.0525	-0.0335	-0.0335	-0.0335
TE ↓	setup_rising to CP	0.1559	0.1197	0.1197	0.1197
TE ↑	setup_rising to CP	0.3031	0.2414	0.2414	0.2414
TI ↓	hold_rising to CP	-0.2509	-0.1577	-0.1569	-0.1569
TI ↑	hold_rising to CP	-0.0609	-0.0352	-0.0357	-0.0357
TI ↓	setup_rising to CP	0.3099	0.2314	0.2314	0.2314
TI ↑	setup_rising to CP	0.0971	0.0664	0.0664	0.0664

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	3.355e-07	7.316e-12
X8_P16	3.505e-07	6.812e-12
X17_P16	4.411e-07	7.316e-12
X33_P16	5.251e-07	7.820e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

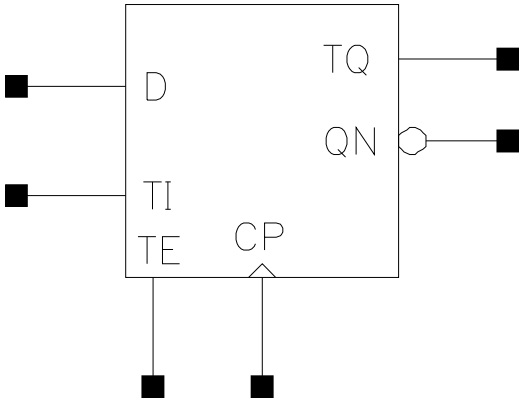
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.099e-03	4.117e-03	4.121e-03	4.123e-03
Clock 100Mhz Data 25Mhz	6.185e-03	6.350e-03	6.960e-03	7.610e-03
Clock 100Mhz Data 50Mhz	8.272e-03	8.583e-03	9.798e-03	1.110e-02
Clock = 0 Data 100Mhz	5.184e-03	4.938e-03	4.856e-03	4.815e-03
Clock = 1 Data 100Mhz	1.449e-03	7.729e-04	5.476e-04	4.349e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.536	4.2432
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0013	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
TE	0.0010	0.0011	0.0011	0.0011

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1230	0.1045	4.2348	2.1443
CP to QN ↑	0.1388	0.0801	8.5278	4.1155
CP to TQ ↓	0.0975	0.0544	6.0273	4.0972
CP to TQ ↑	0.0866	0.0717	16.7460	11.7566
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0979	0.1057	1.0744	0.5703
CP to QN ↑	0.0826	0.0885	2.0808	1.0678
CP to TQ ↓	0.0569	0.0598	5.4086	5.4330
CP to TQ ↑	0.0730	0.0749	15.3202	16.1934

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1726	0.1745	0.1745	0.1745
CP ↑	min_pulse_width to CP	0.0829	0.0453	0.0453	0.0501
D ↓	hold_rising to CP	-0.1280	-0.0631	-0.0631	-0.0631
D ↑	hold_rising to CP	-0.0405	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1821	0.1214	0.1214	0.1214
D ↑	setup_rising to CP	0.0728	0.0390	0.0387	0.0390
TE ↓	hold_rising to CP	-0.0716	-0.0499	-0.0499	-0.0499
TE ↑	hold_rising to CP	-0.0528	-0.0335	-0.0335	-0.0335
TE ↓	setup_rising to CP	0.1559	0.1197	0.1197	0.1197
TE ↑	setup_rising to CP	0.3031	0.2396	0.2389	0.2393
TI ↓	hold_rising to CP	-0.2469	-0.1569	-0.1569	-0.1569
TI ↑	hold_rising to CP	-0.0614	-0.0357	-0.0357	-0.0357
TI ↓	setup_rising to CP	0.3099	0.2314	0.2314	0.2314
TI ↑	setup_rising to CP	0.0961	0.0664	0.0703	0.0664

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	3.563e-07	7.834e-12
X8_P16	3.831e-07	7.316e-12
X17_P16	4.311e-07	7.569e-12
X33_P16	5.279e-07	8.074e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16

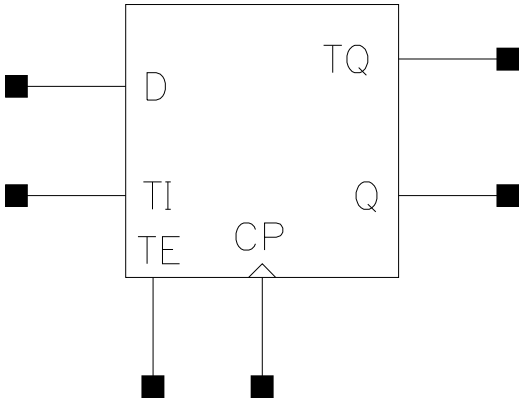
Clock 100Mhz Data 0Mhz	4.218e-03	4.190e-03	4.179e-03	4.173e-03
Clock 100Mhz Data 25Mhz	6.494e-03	6.693e-03	6.983e-03	7.724e-03
Clock 100Mhz Data 50Mhz	8.771e-03	9.195e-03	9.788e-03	1.127e-02
Clock = 0 Data 100Mhz	5.156e-03	4.911e-03	4.830e-03	4.790e-03
Clock = 1 Data 100Mhz	1.458e-03	7.418e-04	5.031e-04	3.839e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.400	4.0800
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007

TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1379	0.0666	5.2188	2.2261
CP to Q ↑	0.0965	0.0762	8.8261	4.1716
CP to TQ ↓	0.1356	0.0707	5.1778	5.5420
CP to TQ ↑	0.0990	0.0841	11.7427	16.3981
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0901	0.0992	1.0794	0.5669
CP to Q ↑	0.1328	0.1397	2.0952	1.0502
CP to TQ ↓	0.0941	0.1056	5.2587	5.3577
CP to TQ ↑	0.1404	0.1500	15.9065	16.0746

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1707	0.1745	0.1745	0.1745
CP ↑	min_pulse_width to CP	0.1168	0.0501	0.0405	0.0405
D ↓	hold_rising to CP	-0.1280	-0.0606	-0.0631	-0.0631
D ↑	hold_rising to CP	-0.0405	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1827	0.1214	0.1214	0.1214
D ↑	setup_rising to CP	0.0728	0.0390	0.0390	0.0390
TE ↓	hold_rising to CP	-0.0716	-0.0499	-0.0496	-0.0496
TE ↑	hold_rising to CP	-0.0525	-0.0335	-0.0335	-0.0335
TE ↓	setup_rising to CP	0.1532	0.1197	0.1197	0.1197
TE ↑	setup_rising to CP	0.3000	0.2393	0.2414	0.2414
TI ↓	hold_rising to CP	-0.2509	-0.1528	-0.1577	-0.1577
TI ↑	hold_rising to CP	-0.0609	-0.0357	-0.0352	-0.0352
TI ↓	setup_rising to CP	0.3099	0.2314	0.2314	0.2314
TI ↑	setup_rising to CP	0.0956	0.0664	0.0664	0.0664

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	3.580e-07	7.568e-12
X8_P16	3.684e-07	7.064e-12
X17_P16	4.583e-07	7.569e-12
X33_P16	5.419e-07	8.072e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

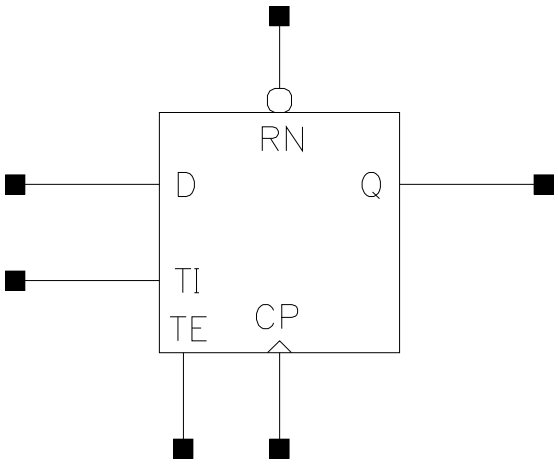
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.112e-03	4.131e-03	4.138e-03	4.141e-03
Clock 100Mhz Data 25Mhz	6.411e-03	6.493e-03	7.224e-03	7.917e-03
Clock 100Mhz Data 50Mhz	8.710e-03	8.855e-03	1.031e-02	1.169e-02
Clock = 0 Data 100Mhz	5.132e-03	4.892e-03	4.814e-03	4.775e-03
Clock = 1 Data 100Mhz	1.431e-03	7.291e-04	4.951e-04	3.781e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.672	4.4064
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
RN	0.0009	0.0007	0.0008	0.0008
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1275	0.0637	5.2980	2.2359
CP to Q ↑	0.0927	0.0776	8.7098	4.1947
RN to Q ↓	0.1025	0.0877	4.3185	2.3803
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0922	0.1019	1.0592	0.5641
CP to Q ↑	0.1154	0.1219	2.0524	1.0460
RN to Q ↓	0.1305	0.1402	1.0554	0.5621

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1919	0.1817	0.1828	0.1823
CP ↑	min_pulse_width to CP	0.1071	0.0463	0.0416	0.0416
D ↓	hold_rising to CP	-0.1183	-0.0484	-0.0477	-0.0508
D ↑	hold_rising to CP	-0.0476	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1846	0.1166	0.1196	0.1196
D ↑	setup_rising to CP	0.0856	0.0540	0.0540	0.0540
RN ↓	min_pulse_width to RN	0.1062	0.1089	0.1045	0.1045
RN ↑	recovery_rising to CP	0.0314	0.0345	0.0345	0.0345
RN ↑	removal_rising to CP	-0.0216	-0.0149	-0.0149	-0.0149
TE ↓	hold_rising to CP	-0.0791	-0.0459	-0.0459	-0.0459
TE ↑	hold_rising to CP	-0.0623	-0.0383	-0.0439	-0.0439
TE ↓	setup_rising to CP	0.1559	0.1148	0.1148	0.1148
TE ↑	setup_rising to CP	0.3031	0.2347	0.2347	0.2347
TI ↓	hold_rising to CP	-0.2322	-0.1373	-0.1387	-0.1387
TI ↑	hold_rising to CP	-0.0712	-0.0401	-0.0455	-0.0455
TI ↓	setup_rising to CP	0.3115	0.2256	0.2271	0.2271
TI ↑	setup_rising to CP	0.1122	0.0849	0.0864	0.0849

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	3.949e-07	8.071e-12
X8_P16	4.088e-07	7.569e-12
X17_P16	4.952e-07	8.324e-12
X33_P16	5.863e-07	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.624e-03	4.668e-03	4.703e-03	4.720e-03

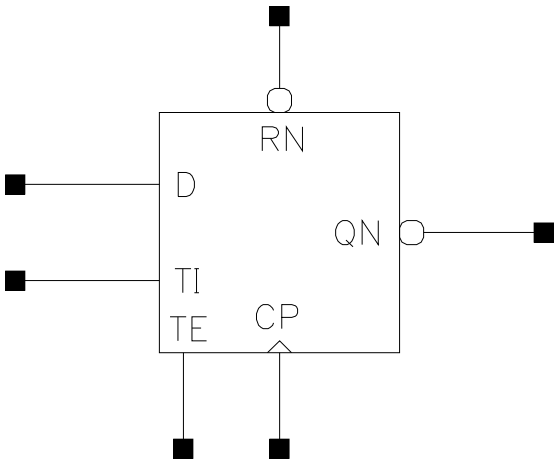
Clock 100Mhz Data 25Mhz	6.897e-03	6.951e-03	7.849e-03	8.578e-03
Clock 100Mhz Data 50Mhz	9.171e-03	9.233e-03	1.099e-02	1.244e-02
Clock = 0 Data 100Mhz	5.336e-03	4.992e-03	4.875e-03	4.817e-03
Clock = 1 Data 100Mhz	1.466e-03	8.115e-04	5.931e-04	4.843e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	3.944	4.7328
X33_P16	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1057	0.0973	3.9778	2.0721
CP to QN ↑	0.1290	0.0741	8.4891	4.0613
RN to QN ↑	0.1150	0.1151	8.4708	4.0637
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0955	0.1059	1.0596	0.5637
CP to QN ↑	0.0847	0.0935	2.0637	1.0588
RN to QN ↑	0.1205	0.1326	2.0697	1.0608

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1919	0.1817	0.1817	0.1818
CP ↑	min_pulse_width to CP	0.0780	0.0415	0.0501	0.0549
D ↓	hold_rising to CP	-0.1183	-0.0477	-0.0484	-0.0484
D ↑	hold_rising to CP	-0.0476	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1846	0.1166	0.1166	0.1166
D ↑	setup_rising to CP	0.0856	0.0540	0.0540	0.0540
RN ↓	min_pulse_width to RN	0.1062	0.1045	0.1182	0.1257
RN ↑	recovery_rising to CP	0.0318	0.0367	0.0345	0.0345
RN ↑	removal_rising to CP	-0.0216	-0.0167	-0.0149	-0.0149
TE ↓	hold_rising to CP	-0.0795	-0.0459	-0.0459	-0.0459
TE ↑	hold_rising to CP	-0.0623	-0.0383	-0.0383	-0.0383
TE ↓	setup_rising to CP	0.1559	0.1148	0.1148	0.1148
TE ↑	setup_rising to CP	0.3031	0.2347	0.2347	0.2347
TI ↓	hold_rising to CP	-0.2322	-0.1373	-0.1333	-0.1333
TI ↑	hold_rising to CP	-0.0712	-0.0416	-0.0401	-0.0401
TI ↓	setup_rising to CP	0.3115	0.2257	0.2271	0.2271
TI ↑	setup_rising to CP	0.1122	0.0849	0.0849	0.0849

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	3.920e-07	8.165e-12
X8_P16	3.994e-07	7.820e-12
X17_P16	4.844e-07	8.072e-12
X33_P16	5.599e-07	8.577e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.545e-03	4.512e-03	4.501e-03	4.495e-03

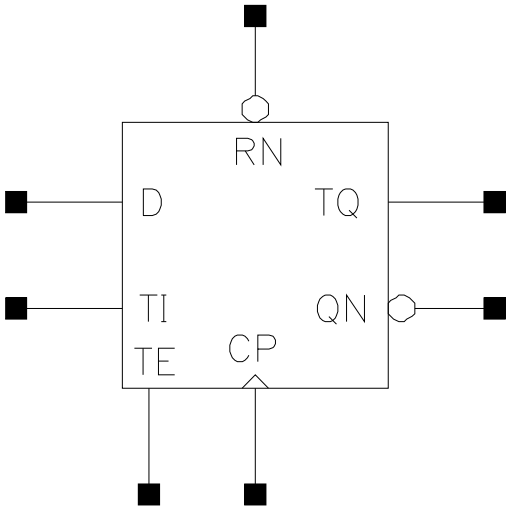
Clock 100Mhz Data 25Mhz	6.830e-03	6.900e-03	7.544e-03	8.215e-03
Clock 100Mhz Data 50Mhz	9.116e-03	9.287e-03	1.059e-02	1.193e-02
Clock = 0 Data 100Mhz	5.351e-03	5.012e-03	4.904e-03	4.850e-03
Clock = 1 Data 100Mhz	1.467e-03	7.730e-04	5.415e-04	4.260e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007

RN	0.0011	0.0008	0.0009	0.0009
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1183	0.1010	3.9788	2.1765
CP to QN ↑	0.1716	0.0847	7.5397	4.2244
CP to TQ ↓	0.1228	0.0581	5.5085	4.2587
CP to TQ ↑	0.0961	0.0783	13.2865	12.2874
RN to QN ↑	0.1146	0.1144	7.6385	4.2122
RN to TQ ↓	0.0797	0.0782	4.7682	4.5373
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.1043	0.1122	1.0835	0.5765
CP to QN ↑	0.0859	0.0905	2.1106	1.0608
CP to TQ ↓	0.0607	0.0633	5.2843	5.1742
CP to TQ ↑	0.0784	0.0803	11.5077	11.6703
RN to QN ↑	0.1182	0.1256	2.1066	1.0584
RN to TQ ↓	0.0838	0.0882	5.5679	5.4891

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1919	0.1817	0.1828	0.1823
CP ↑	min_pulse_width to CP	0.1168	0.0464	0.0501	0.0501
D ↓	hold_rising to CP	-0.1183	-0.0484	-0.0484	-0.0484
D ↑	hold_rising to CP	-0.0476	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1876	0.1166	0.1166	0.1166
D ↑	setup_rising to CP	0.0856	0.0540	0.0540	0.0540
RN ↓	min_pulse_width to RN	0.1084	0.1111	0.1111	0.1208
RN ↑	recovery_rising to CP	0.0344	0.0345	0.0345	0.0345
RN ↑	removal_rising to CP	-0.0246	-0.0170	-0.0174	-0.0174
TE ↓	hold_rising to CP	-0.0795	-0.0459	-0.0459	-0.0459
TE ↑	hold_rising to CP	-0.0623	-0.0383	-0.0408	-0.0408
TE ↓	setup_rising to CP	0.1559	0.1148	0.1148	0.1148
TE ↑	setup_rising to CP	0.3031	0.2347	0.2347	0.2347
TI ↓	hold_rising to CP	-0.2322	-0.1373	-0.1333	-0.1333
TI ↑	hold_rising to CP	-0.0712	-0.0401	-0.0416	-0.0416
TI ↓	setup_rising to CP	0.3115	0.2257	0.2271	0.2271
TI ↑	setup_rising to CP	0.1122	0.0849	0.0864	0.0864

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	4.141e-07	8.323e-12
X8_P16	4.210e-07	7.820e-12
X17_P16	4.690e-07	8.324e-12
X33_P16	5.602e-07	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

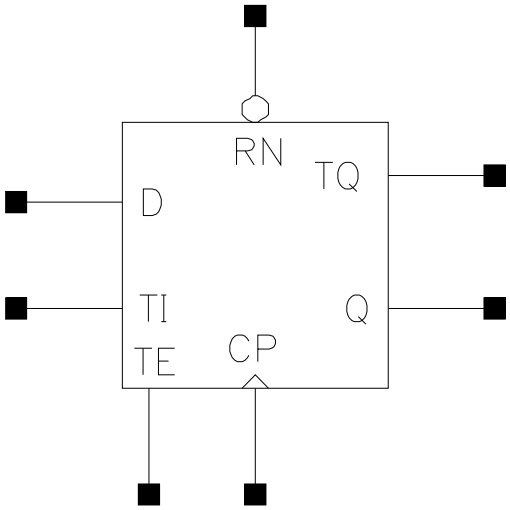
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.564e-03	4.556e-03	4.575e-03	4.585e-03
Clock 100Mhz Data 25Mhz	7.049e-03	7.106e-03	7.467e-03	8.231e-03
Clock 100Mhz Data 50Mhz	9.534e-03	9.656e-03	1.036e-02	1.188e-02
Clock = 0 Data 100Mhz	5.325e-03	4.984e-03	4.866e-03	4.807e-03
Clock = 1 Data 100Mhz	1.466e-03	7.829e-04	5.549e-04	4.411e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007

RN	0.0009	0.0009	0.0008	0.0008
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1444	0.0695	5.6537	2.3088
CP to Q ↑	0.0991	0.0808	9.0232	4.3429
CP to TQ ↓	0.1418	0.0716	6.9051	5.6259
CP to TQ ↑	0.1028	0.0855	18.0519	16.3526
RN to Q ↓	0.1066	0.0994	4.5514	2.4729
RN to TQ ↓	0.1056	0.1027	5.7450	5.9211
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0952	0.1053	1.0752	0.5733
CP to Q ↑	0.1161	0.1230	2.0611	1.0503
CP to TQ ↓	0.0992	0.1128	5.2958	5.3889
CP to TQ ↑	0.1234	0.1342	16.0774	16.1547
RN to Q ↓	0.1335	0.1436	1.0724	0.5715
RN to TQ ↓	0.1375	0.1512	5.2893	5.3873

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1913	0.1817	0.1817	0.1812
CP ↑	min_pulse_width to CP	0.1265	0.0538	0.0415	0.0416
D ↓	hold_rising to CP	-0.1183	-0.0484	-0.0508	-0.0508
D ↑	hold_rising to CP	-0.0476	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1827	0.1166	0.1166	0.1166
D ↑	setup_rising to CP	0.0856	0.0540	0.0540	0.0512
RN ↓	min_pulse_width to RN	0.1111	0.1235	0.1018	0.1018
RN ↑	recovery_rising to CP	0.0318	0.0345	0.0345	0.0345
RN ↑	removal_rising to CP	-0.0222	-0.0170	-0.0170	-0.0174
TE ↓	hold_rising to CP	-0.0791	-0.0431	-0.0459	-0.0459
TE ↑	hold_rising to CP	-0.0623	-0.0383	-0.0383	-0.0383
TE ↓	setup_rising to CP	0.1563	0.1148	0.1148	0.1148
TE ↑	setup_rising to CP	0.3031	0.2347	0.2347	0.2347
TI ↓	hold_rising to CP	-0.2307	-0.1338	-0.1388	-0.1387
TI ↑	hold_rising to CP	-0.0707	-0.0401	-0.0416	-0.0416
TI ↓	setup_rising to CP	0.3099	0.2256	0.2256	0.2257
TI ↑	setup_rising to CP	0.1122	0.0849	0.0851	0.0851

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	4.142e-07	8.323e-12
X8_P16	4.261e-07	7.820e-12
X17_P16	5.118e-07	8.325e-12
X33_P16	6.029e-07	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

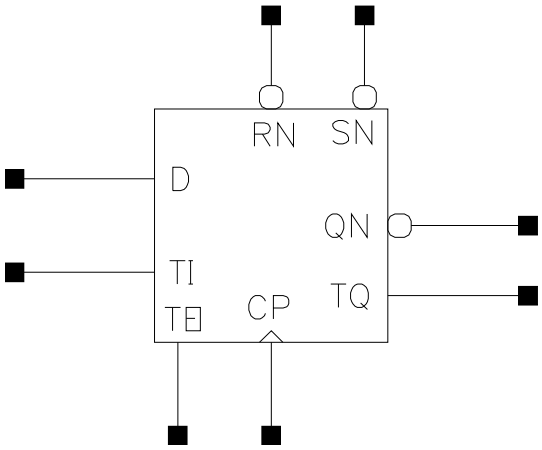
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.611e-03	4.654e-03	4.666e-03	4.673e-03
Clock 100Mhz Data 25Mhz	7.014e-03	7.090e-03	7.988e-03	8.737e-03
Clock 100Mhz Data 50Mhz	9.417e-03	9.526e-03	1.131e-02	1.280e-02
Clock = 0 Data 100Mhz	5.325e-03	4.986e-03	4.872e-03	4.816e-03
Clock = 1 Data 100Mhz	1.466e-03	7.430e-04	5.020e-04	3.815e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.352	5.2224
X17_P16	1.200	4.488	5.3856
X33_P16	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0009

SN	0.0014	0.0014	0.0014
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.1111	0.1189	2.1143	1.0976
CP to QN ↑	0.0890	0.0931	4.0783	2.0612
CP to TQ ↓	0.0679	0.0679	6.7052	6.7109
CP to TQ ↑	0.0908	0.0909	21.5487	21.5394
RN to QN ↓	0.1218	0.1293	2.1148	1.0982
RN to QN ↑	0.1290	0.1351	4.0826	2.0646
RN to TQ ↓	0.0991	0.0988	7.3470	7.3428
RN to TQ ↑	0.1020	0.1021	21.5224	21.5388
SN to QN ↓	0.1309	0.1398	2.1222	1.1003
SN to TQ ↑	0.1082	0.1081	21.7635	21.7533
	X33_P16		**X33_P16**	
CP to QN ↓	0.1372		0.5941	
CP to QN ↑	0.1028		1.0555	
CP to TQ ↓	0.0680		6.7143	
CP to TQ ↑	0.0912		21.5880	
RN to QN ↓	0.1474		0.5952	
RN to QN ↑	0.1479		1.0560	
RN to TQ ↓	0.0989		7.3510	
RN to TQ ↑	0.1023		21.5642	
SN to QN ↓	0.1597		0.5947	
SN to TQ ↑	0.1085		21.8354	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1871	0.1871	0.1871
CP ↑	min_pulse_width to CP	0.0501	0.0512	0.0549
D ↓	hold_rising to CP	-0.0484	-0.0484	-0.0484
D ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1245	0.1245	0.1245
D ↑	setup_rising to CP	0.0561	0.0561	0.0592
RN ↓	min_pulse_width to RN	0.1208	0.1257	0.1306
RN ↑	non_seq_hold_rising to SN	-0.0430	-0.0430	-0.0430
RN ↑	non_seq_setup_rising to SN	0.1055	0.1055	0.1055
RN ↑	recovery_rising to CP	0.0491	0.0491	0.0491
RN ↑	removal_rising to CP	-0.0264	-0.0264	-0.0264
SN ↓	min_pulse_width to SN	0.0979	0.1006	0.1033
SN ↑	recovery_rising to CP	0.0202	0.0202	0.0202
SN ↑	removal_rising to CP	0.0433	0.0433	0.0433

TE ↓	hold_rising to CP	-0.0459	-0.0459	-0.0459
TE ↑	hold_rising to CP	-0.0383	-0.0383	-0.0383
TE ↓	setup_rising to CP	0.1222	0.1222	0.1222
TE ↑	setup_rising to CP	0.2396	0.2396	0.2396
TI ↓	hold_rising to CP	-0.1333	-0.1373	-0.1333
TI ↑	hold_rising to CP	-0.0401	-0.0401	-0.0401
TI ↓	setup_rising to CP	0.2319	0.2319	0.2319
TI ↑	setup_rising to CP	0.0900	0.0900	0.0900

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	4.814e-07	8.846e-12
X17_P16	5.232e-07	9.097e-12
X33_P16	6.026e-07	9.601e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

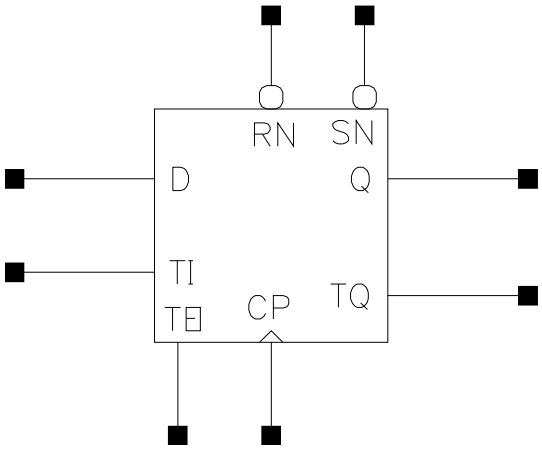
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.765e-03	4.765e-03	4.766e-03
Clock 100Mhz Data 25Mhz	7.401e-03	7.705e-03	8.431e-03
Clock 100Mhz Data 50Mhz	1.004e-02	1.064e-02	1.210e-02
Clock = 0 Data 100Mhz	4.879e-03	4.878e-03	4.878e-03
Clock = 1 Data 100Mhz	1.601e-04	1.598e-04	1.602e-04

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.216	5.0592
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0009

SN	0.0014	0.0014	0.0014
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0759	0.0857	2.2441	1.1781
CP to Q ↑	0.0881	0.0924	4.1802	2.1278
CP to TQ ↓	0.0802	0.0940	6.8331	6.9240
CP to TQ ↑	0.0979	0.1079	20.8072	20.9441
RN to Q ↓	0.1138	0.1316	2.6335	1.3943
RN to Q ↑	0.0777	0.0867	4.3316	2.2179
RN to TQ ↓	0.1205	0.1446	7.5466	7.7569
RN to TQ ↑	0.0936	0.1117	20.9995	21.1572
SN to Q ↑	0.1071	0.1160	4.3272	2.2172
SN to TQ ↑	0.1229	0.1409	21.0013	21.1649
	X33_P16		**X33_P16**	
CP to Q ↓	0.1098		0.6487	
CP to Q ↑	0.1048		1.1035	
CP to TQ ↓	0.1186		7.2151	
CP to TQ ↑	0.1262		21.1769	
RN to Q ↓	0.1747		0.7881	
RN to Q ↑	0.1103		1.1657	
RN to TQ ↓	0.1871		8.2782	
RN to TQ ↑	0.1462		21.4539	
SN to Q ↑	0.1393		1.1659	
SN to TQ ↑	0.1752		21.4574	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1871	0.1871	0.1871
CP ↑	min_pulse_width to CP	0.0586	0.0683	0.0974
D ↓	hold_rising to CP	-0.0484	-0.0484	-0.0484
D ↑	hold_rising to CP	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1245	0.1245	0.1245
D ↑	setup_rising to CP	0.0592	0.0592	0.0592
RN ↓	min_pulse_width to RN	0.1306	0.1577	0.2039
RN ↑	non_seq_hold_rising to SN	-0.0481	-0.0579	-0.0775
RN ↑	non_seq_setup_rising to SN	0.1006	0.1006	0.1234
RN ↑	recovery_rising to CP	0.0443	0.0443	0.0443
RN ↑	removal_rising to CP	-0.0246	-0.0246	-0.0246
SN ↓	min_pulse_width to SN	0.1033	0.1135	0.1455
SN ↑	recovery_rising to CP	0.0202	0.0202	0.0202
SN ↑	removal_rising to CP	0.0433	0.0433	0.0433

TE ↓	hold_rising to CP	-0.0435	-0.0435	-0.0435
TE ↑	hold_rising to CP	-0.0383	-0.0383	-0.0383
TE ↓	setup_rising to CP	0.1222	0.1222	0.1222
TE ↑	setup_rising to CP	0.2396	0.2396	0.2396
TI ↓	hold_rising to CP	-0.1338	-0.1340	-0.1325
TI ↑	hold_rising to CP	-0.0401	-0.0401	-0.0401
TI ↓	setup_rising to CP	0.2319	0.2319	0.2319
TI ↑	setup_rising to CP	0.0900	0.0900	0.0900

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P16	4.809e-07	8.585e-12
X17_P16	5.276e-07	8.837e-12
X33_P16	6.163e-07	9.341e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

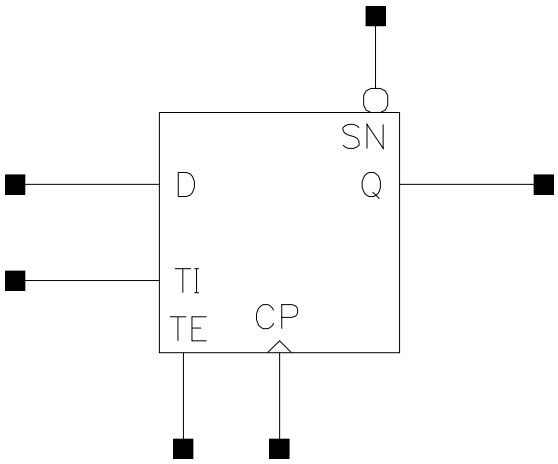
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.730e-03	4.731e-03	4.732e-03
Clock 100Mhz Data 25Mhz	7.224e-03	7.534e-03	8.274e-03
Clock 100Mhz Data 50Mhz	9.717e-03	1.034e-02	1.182e-02
Clock = 0 Data 100Mhz	4.849e-03	4.850e-03	4.849e-03
Clock = 1 Data 100Mhz	1.091e-04	1.093e-04	1.094e-04

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005
SN	0.0015	0.0015	0.0015	0.0015
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004
	X33_P16			

CP	0.0010			
D	0.0005			
SN	0.0015			
TE	0.0011			
TI	0.0004			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1281	0.0665	5.3350	2.2239
CP to Q ↑	0.0969	0.0811	8.7776	4.1649
SN to Q ↑	0.0747	0.0842	8.5863	4.1674
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to Q ↓	0.0915	0.0968	1.0608	0.7402
CP to Q ↑	0.1159	0.1197	2.0523	1.3909
SN to Q ↑	0.1187	0.1225	2.0505	1.3918
	X33_P16		**X33_P16**	
CP to Q ↓	0.1011		0.5650	
CP to Q ↑	0.1223		1.0479	
SN to Q ↑	0.1252		1.0472	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.1943	0.1877	0.1895	0.1877
CP ↑	min_pulse_width to CP	0.1071	0.0490	0.0405	0.0405
D ↓	hold_rising to CP	-0.1183	-0.0533	-0.0526	-0.0526
D ↑	hold_rising to CP	-0.0454	-0.0090	-0.0146	-0.0146
D ↓	setup_rising to CP	0.1876	0.1270	0.1270	0.1270
D ↑	setup_rising to CP	0.0804	0.0442	0.0442	0.0442
SN ↓	min_pulse_width to SN	0.0686	0.0784	0.0757	0.0757
SN ↑	recovery_rising to CP	0.0177	0.0176	0.0176	0.0176
SN ↑	removal_rising to CP	0.0310	0.0408	0.0408	0.0408
TE ↓	hold_rising to CP	-0.0765	-0.0480	-0.0508	-0.0508
TE ↑	hold_rising to CP	-0.0605	-0.0360	-0.0390	-0.0390
TE ↓	setup_rising to CP	0.1581	0.1215	0.1215	0.1215
TE ↑	setup_rising to CP	0.3031	0.2445	0.2445	0.2445
TI ↓	hold_rising to CP	-0.2322	-0.1422	-0.1435	-0.1435
TI ↑	hold_rising to CP	-0.0671	-0.0367	-0.0365	-0.0365
TI ↓	setup_rising to CP	0.3109	0.2355	0.2355	0.2355
TI ↑	setup_rising to CP	0.1058	0.0752	0.0754	0.0754
		X33_P16			

CP ↓	min_pulse_width to CP	0.1877			
CP ↑	min_pulse_width to CP	0.0405			
D ↓	hold_rising to CP	-0.0526			
D ↑	hold_rising to CP	-0.0146			
D ↓	setup_rising to CP	0.1270			
D ↑	setup_rising to CP	0.0442			
SN ↓	min_pulse_width to SN	0.0757			
SN ↑	recovery_rising to CP	0.0176			
SN ↑	removal_rising to CP	0.0408			
TE ↓	hold_rising to CP	-0.0508			
TE ↑	hold_rising to CP	-0.0390			
TE ↓	setup_rising to CP	0.1215			
TE ↑	setup_rising to CP	0.2445			
TI ↓	hold_rising to CP	-0.1430			
TI ↑	hold_rising to CP	-0.0365			
TI ↓	setup_rising to CP	0.2355			
TI ↑	setup_rising to CP	0.0754			

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	4.013e-07	8.072e-12
X8_P16	4.176e-07	7.821e-12
X17_P16	5.042e-07	8.325e-12
X25_P16	5.420e-07	8.577e-12
X33_P16	5.797e-07	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	4.482e-03	4.513e-03	4.524e-03	4.528e-03
Clock 100Mhz Data 25Mhz	6.739e-03	6.872e-03	7.692e-03	8.084e-03
Clock 100Mhz Data 50Mhz	8.996e-03	9.232e-03	1.086e-02	1.164e-02
Clock = 0 Data 100Mhz	5.207e-03	4.958e-03	4.875e-03	4.834e-03
Clock = 1 Data 100Mhz	1.466e-03	7.757e-04	5.455e-04	4.306e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	4.532e-03			

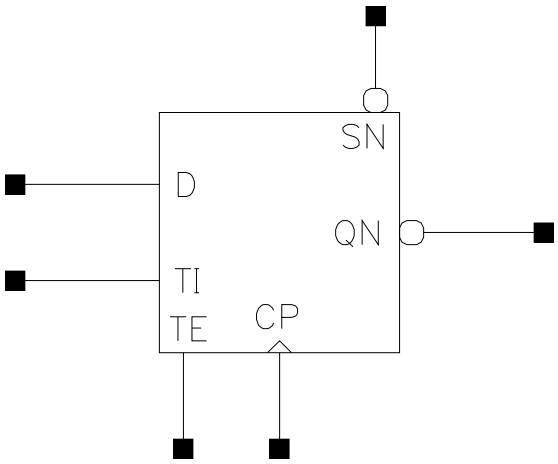
Clock 100Mhz Data 25Mhz	8.397e-03			
Clock 100Mhz Data 50Mhz	1.226e-02			
Clock = 0 Data 100Mhz	4.809e-03			
Clock = 1 Data 100Mhz	3.616e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005
SN	0.0015	0.0015	0.0015	0.0015
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004
	X33_P16			

CP	0.0010			
D	0.0005			
SN	0.0015			
TE	0.0011			
TI	0.0004			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1104	0.0984	3.9808	2.0725
CP to QN ↑	0.1305	0.0742	8.4846	4.0801
SN to QN ↓	0.0902	0.1010	3.9642	2.0710
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to QN ↓	0.1022	0.1082	1.0660	0.7433
CP to QN ↑	0.0906	0.0956	2.0543	1.3940
SN to QN ↓	0.1066	0.1128	1.0649	0.7422
	X33_P16		**X33_P16**	
CP to QN ↓	0.1131		0.5665	
CP to QN ↑	0.0992		1.0484	
SN to QN ↓	0.1175		0.5665	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.1943	0.1895	0.1877	0.1877
CP ↑	min_pulse_width to CP	0.0781	0.0405	0.0549	0.0549
D ↓	hold_rising to CP	-0.1208	-0.0530	-0.0533	-0.0533
D ↑	hold_rising to CP	-0.0454	-0.0115	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1876	0.1270	0.1270	0.1270
D ↑	setup_rising to CP	0.0807	0.0442	0.0442	0.0442
SN ↓	min_pulse_width to SN	0.0659	0.0757	0.0811	0.0833
SN ↑	recovery_rising to CP	0.0177	0.0176	0.0176	0.0176
SN ↑	removal_rising to CP	0.0310	0.0408	0.0408	0.0408
TE ↓	hold_rising to CP	-0.0765	-0.0508	-0.0480	-0.0480
TE ↑	hold_rising to CP	-0.0605	-0.0390	-0.0360	-0.0360
TE ↓	setup_rising to CP	0.1581	0.1215	0.1215	0.1215
TE ↑	setup_rising to CP	0.3031	0.2445	0.2445	0.2445
TI ↓	hold_rising to CP	-0.2322	-0.1435	-0.1422	-0.1422
TI ↑	hold_rising to CP	-0.0671	-0.0365	-0.0367	-0.0367
TI ↓	setup_rising to CP	0.3109	0.2355	0.2355	0.2355
TI ↑	setup_rising to CP	0.1058	0.0752	0.0752	0.0752
		X33_P16			

CP ↓	min_pulse_width to CP	0.1877			
CP ↑	min_pulse_width to CP	0.0587			
D ↓	hold_rising to CP	-0.0533			
D ↑	hold_rising to CP	-0.0090			
D ↓	setup_rising to CP	0.1270			
D ↑	setup_rising to CP	0.0442			
SN ↓	min_pulse_width to SN	0.0833			
SN ↑	recovery_rising to CP	0.0176			
SN ↑	removal_rising to CP	0.0408			
TE ↓	hold_rising to CP	-0.0480			
TE ↑	hold_rising to CP	-0.0360			
TE ↓	setup_rising to CP	0.1215			
TE ↑	setup_rising to CP	0.2445			
TI ↓	hold_rising to CP	-0.1422			
TI ↑	hold_rising to CP	-0.0367			
TI ↓	setup_rising to CP	0.2355			
TI ↑	setup_rising to CP	0.0752			

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	4.063e-07	8.072e-12
X8_P16	4.257e-07	7.820e-12
X17_P16	5.122e-07	8.325e-12
X25_P16	5.578e-07	8.576e-12
X33_P16	6.033e-07	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	4.469e-03	4.507e-03	4.516e-03	4.520e-03
Clock 100Mhz Data 25Mhz	6.710e-03	6.878e-03	7.658e-03	8.040e-03
Clock 100Mhz Data 50Mhz	8.952e-03	9.248e-03	1.080e-02	1.156e-02
Clock = 0 Data 100Mhz	5.206e-03	4.963e-03	4.878e-03	4.837e-03
Clock = 1 Data 100Mhz	1.468e-03	7.802e-04	5.511e-04	4.366e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	4.523e-03			

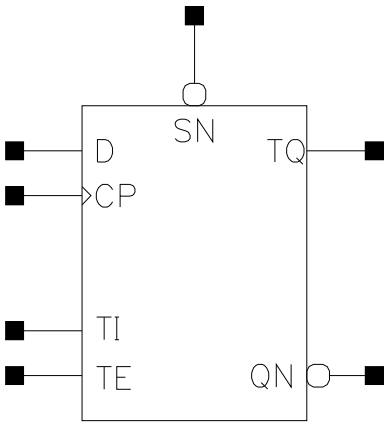
Clock 100Mhz Data 25Mhz	8.352e-03			
Clock 100Mhz Data 50Mhz	1.218e-02			
Clock = 0 Data 100Mhz	4.812e-03			
Clock = 1 Data 100Mhz	3.678e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.216	5.0592
X8_P16	1.200	4.080	4.8960
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005

SN	0.0016	0.0017	0.0016	0.0017
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1271	0.1035	3.9572	2.0763
CP to QN ↑	0.1733	0.0853	8.3203	4.1573
CP to TQ ↓	0.1247	0.0593	6.2665	4.9178
CP to TQ ↑	0.0969	0.0771	11.7221	11.4445
SN to QN ↓	0.0855	0.0886	3.9618	2.0762
SN to TQ ↑	0.0593	0.0613	11.5424	11.4777
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.1027	0.1137	1.0902	0.5593
CP to QN ↑	0.0984	0.1076	2.0626	1.0510
CP to TQ ↓	0.0750	0.0750	5.1806	5.1800
CP to TQ ↑	0.0864	0.0865	11.5176	11.5496
SN to QN ↓	0.0892	0.1000	1.0896	0.5583
SN to TQ ↑	0.0723	0.0723	11.5198	11.5557

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1943	0.1895	0.1895	0.1877
CP ↑	min_pulse_width to CP	0.1168	0.0453	0.0598	0.0635
D ↓	hold_rising to CP	-0.1183	-0.0533	-0.0533	-0.0533
D ↑	hold_rising to CP	-0.0454	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1876	0.1270	0.1270	0.1270
D ↑	setup_rising to CP	0.0804	0.0442	0.0442	0.0442
SN ↓	min_pulse_width to SN	0.0637	0.0659	0.0686	0.0686
SN ↑	recovery_rising to CP	0.0176	0.0176	0.0176	0.0176
SN ↑	removal_rising to CP	0.0310	0.0408	0.0408	0.0408
TE ↓	hold_rising to CP	-0.0765	-0.0508	-0.0484	-0.0480
TE ↑	hold_rising to CP	-0.0605	-0.0360	-0.0335	-0.0335
TE ↓	setup_rising to CP	0.1611	0.1215	0.1215	0.1215
TE ↑	setup_rising to CP	0.3031	0.2445	0.2445	0.2445
TI ↓	hold_rising to CP	-0.2322	-0.1437	-0.1422	-0.1422
TI ↑	hold_rising to CP	-0.0671	-0.0367	-0.0352	-0.0352
TI ↓	setup_rising to CP	0.3150	0.2355	0.2355	0.2355
TI ↑	setup_rising to CP	0.1058	0.0752	0.0752	0.0752

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	4.279e-07	8.543e-12
X8_P16	4.474e-07	8.324e-12
X17_P16	5.339e-07	8.829e-12
X33_P16	6.250e-07	9.333e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

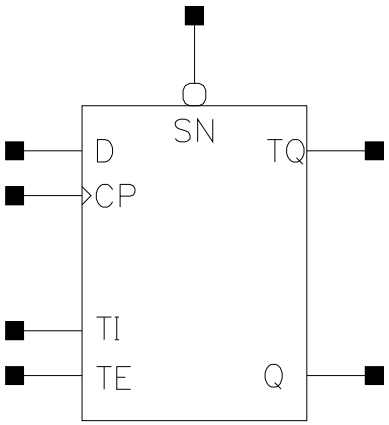
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.479e-03	4.581e-03	4.616e-03	4.634e-03
Clock 100Mhz Data 25Mhz	7.006e-03	7.180e-03	7.874e-03	8.569e-03
Clock 100Mhz Data 50Mhz	9.533e-03	9.779e-03	1.113e-02	1.250e-02
Clock = 0 Data 100Mhz	5.210e-03	4.957e-03	4.873e-03	4.831e-03
Clock = 1 Data 100Mhz	1.464e-03	7.476e-04	5.088e-04	3.894e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.944	4.7328
X17_P16	1.200	4.216	5.0592
X33_P16	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005

SN	0.0016	0.0015	0.0015	0.0015
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1484	0.0715	5.5287	2.2819
CP to Q ↑	0.1035	0.0841	8.8415	4.2143
CP to TQ ↓	0.1490	0.0762	7.8424	5.6380
CP to TQ ↑	0.1025	0.0931	11.7949	16.4663
SN to Q ↑	0.0631	0.0877	8.6188	4.2164
SN to TQ ↑	0.0621	0.0980	11.5681	16.4478
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0938	0.1033	1.0924	0.5759
CP to Q ↑	0.1176	0.1239	2.0616	1.0519
CP to TQ ↓	0.0978	0.1108	5.2931	5.3786
CP to TQ ↑	0.1251	0.1349	16.0886	16.1837
SN to Q ↑	0.1204	0.1266	2.0617	1.0509
SN to TQ ↑	0.1278	0.1376	16.0884	16.1858

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1919	0.1877	0.1895	0.1877
CP ↑	min_pulse_width to CP	0.1265	0.0538	0.0405	0.0405
D ↓	hold_rising to CP	-0.1183	-0.0533	-0.0530	-0.0526
D ↑	hold_rising to CP	-0.0454	-0.0090	-0.0146	-0.0146
D ↓	setup_rising to CP	0.1876	0.1270	0.1270	0.1270
D ↑	setup_rising to CP	0.0804	0.0442	0.0442	0.0442
SN ↓	min_pulse_width to SN	0.0583	0.0833	0.0757	0.0757
SN ↑	recovery_rising to CP	0.0177	0.0176	0.0176	0.0176
SN ↑	removal_rising to CP	0.0310	0.0408	0.0408	0.0408
TE ↓	hold_rising to CP	-0.0795	-0.0484	-0.0508	-0.0508
TE ↑	hold_rising to CP	-0.0601	-0.0360	-0.0390	-0.0390
TE ↓	setup_rising to CP	0.1585	0.1215	0.1215	0.1219
TE ↑	setup_rising to CP	0.3031	0.2445	0.2445	0.2445
TI ↓	hold_rising to CP	-0.2322	-0.1422	-0.1435	-0.1430
TI ↑	hold_rising to CP	-0.0671	-0.0367	-0.0365	-0.0365
TI ↓	setup_rising to CP	0.3115	0.2355	0.2355	0.2355
TI ↑	setup_rising to CP	0.1058	0.0752	0.0752	0.0754

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	4.179e-07	8.311e-12
X8_P16	4.327e-07	8.072e-12
X17_P16	5.186e-07	8.577e-12
X33_P16	5.942e-07	9.080e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

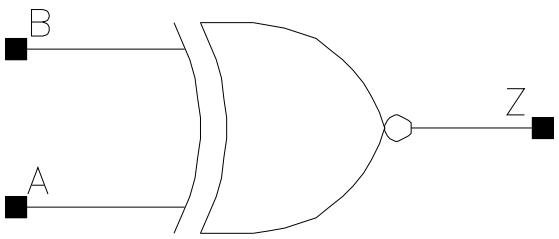
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	4.473e-03	4.580e-03	4.614e-03	4.632e-03
Clock 100Mhz Data 25Mhz	6.885e-03	7.103e-03	7.976e-03	8.715e-03
Clock 100Mhz Data 50Mhz	9.296e-03	9.626e-03	1.134e-02	1.280e-02
Clock = 0 Data 100Mhz	5.208e-03	4.951e-03	4.865e-03	4.822e-03
Clock = 1 Data 100Mhz	1.467e-03	7.492e-04	5.099e-04	3.903e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P16	X8_P16	X17_P16	X25_P16
A	0.0018	0.0007	0.0010	0.0016
B	0.0017	0.0015	0.0020	0.0027
	X33_P16			
A	0.0018			
B	0.0031			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X8_P16**	**X6_P16**	**X8_P16**
A to Z ↓	0.0295	0.0720	3.9414	2.2594
A to Z ↑	0.0326	0.0596	6.7751	4.3000
B to Z ↓	0.0278	0.0500	3.9368	2.2483
B to Z ↑	0.0319	0.0446	6.7883	4.2879
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
A to Z ↓	0.0687	0.0685	1.1200	0.7731
A to Z ↑	0.0549	0.0557	2.1081	1.4011

B to Z ↓	0.0523	0.0509	1.1183	0.7713
B to Z ↑	0.0445	0.0433	2.1058	1.3977
	X33_P16		**X33_P16**	
A to Z ↓	0.0647		0.5802	
A to Z ↑	0.0539		1.0518	
B to Z ↓	0.0489		0.5796	
B to Z ↑	0.0430		1.0499	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P16	1.626e-07	2.528e-12
X8_P16	1.499e-07	3.283e-12
X17_P16	2.361e-07	3.540e-12
X25_P16	3.824e-07	5.048e-12
X33_P16	4.843e-07	5.298e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	2.842e-03	5.043e-03	7.011e-03	1.134e-02
B to Z	2.598e-03	3.462e-03	5.203e-03	8.223e-03
	X33_P16			
A to Z	1.377e-02			
B to Z	1.030e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

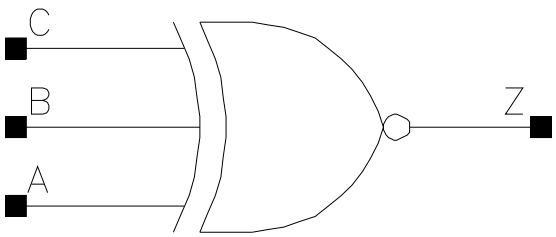
Pin Cycle (vdds)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	-1.612e-05	-3.029e-07	-4.073e-07	-7.931e-07
B to Z	1.047e-05	-1.721e-07	-3.942e-07	-8.550e-07
	X33_P16			
A to Z	-7.312e-07			
B to Z	-3.829e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	2.176	2.6112
X16_P16	1.200	2.720	3.2640
X25_P16	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X16_P16	X25_P16
A	0.0030	0.0026	0.0032	0.0047
B	0.0033	0.0023	0.0031	0.0043
C	0.0021	0.0007	0.0007	0.0008

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0492	0.0852	4.7478	2.4266
A to Z ↑	0.0465	0.0747	9.9544	4.2566
B to Z ↓	0.0500	0.0846	4.7435	2.4239
B to Z ↑	0.0466	0.0744	9.9352	4.2567
C to Z ↓	0.0486	0.1102	4.7414	2.4245
C to Z ↑	0.0448	0.0983	9.8994	4.2567
	X16_P16	**X25_P16**	**X16_P16**	**X25_P16**
A to Z ↓	0.0847	0.0843	1.2459	0.7970
A to Z ↑	0.0807	0.0800	2.2329	1.4051
B to Z ↓	0.0845	0.0849	1.2449	0.7959

B to Z ↑	0.0805	0.0813	2.2324	1.4048
C to Z ↓	0.1154	0.1218	1.2446	0.7959
C to Z ↑	0.1094	0.1164	2.2324	1.4056

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	3.045e-07	4.545e-12
X8_P16	2.737e-07	4.795e-12
X16_P16	4.065e-07	5.803e-12
X25_P16	5.941e-07	8.069e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	3.148e-03	4.030e-03	6.431e-03	9.576e-03
B to Z	2.886e-03	3.919e-03	6.259e-03	9.386e-03
C to Z	2.810e-03	6.125e-03	9.005e-03	1.345e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

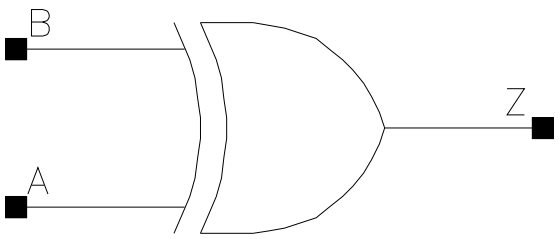
Pin Cycle (vdds)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	-4.124e-05	-1.414e-05	-2.311e-05	-3.524e-05
B to Z	-1.746e-06	-9.073e-06	-7.380e-06	-9.225e-06
C to Z	9.318e-06	4.467e-06	1.962e-06	2.683e-07

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.224	1.4688
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.224	1.4688
X16_P16	1.200	1.360	1.6320
X25_P16	1.200	2.176	2.6112
X31_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X16_P16
A	0.0008	0.0017	0.0011	0.0012
B	0.0013	0.0016	0.0016	0.0018
	X25_P16	X31_P16		
A	0.0015	0.0020		
B	0.0027	0.0035		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0639	0.0321	4.0553	3.0193
A to Z ↑	0.0561	0.0332	8.2590	8.8304
B to Z ↓	0.0453	0.0315	4.0447	3.0384
B to Z ↑	0.0439	0.0312	8.2537	8.8166
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0577	0.0604	2.2010	1.1442

A to Z ↑	0.0487	0.0512	4.1896	2.1122
B to Z ↓	0.0443	0.0465	2.1967	1.1431
B to Z ↑	0.0403	0.0426	4.1908	2.1124
	X25_P16	**X31_P16**	**X25_P16**	**X31_P16**
A to Z ↓	0.0640	0.0602	0.7663	0.6166
A to Z ↑	0.0543	0.0519	1.3970	1.1277
B to Z ↓	0.0491	0.0463	0.7659	0.6167
B to Z ↑	0.0422	0.0406	1.3982	1.1275

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	1.272e-07	3.033e-12
X6_P16	1.596e-07	2.528e-12
X8_P16	1.814e-07	3.029e-12
X16_P16	2.507e-07	3.281e-12
X25_P16	3.770e-07	4.795e-12
X31_P16	4.806e-07	5.045e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	3.901e-03	2.820e-03	4.661e-03	6.611e-03
B to Z	2.954e-03	2.518e-03	3.770e-03	5.425e-03
	X25_P16	X31_P16		
A to Z	1.018e-02	1.260e-02		
B to Z	7.018e-03	8.627e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

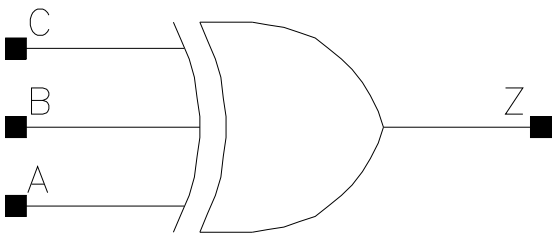
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	-3.272e-07	-2.361e-05	-3.725e-07	-4.898e-07
B to Z	8.467e-08	6.299e-06	-4.176e-07	-5.462e-07
	X25_P16	X31_P16		
A to Z	-8.335e-07	-1.093e-06		
B to Z	-2.757e-08	8.970e-08		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X24_P16	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X24_P16
A	0.0026	0.0025	0.0032	0.0057
B	0.0026	0.0023	0.0029	0.0047
C	0.0008	0.0018	0.0024	0.0038

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0500	0.0850	5.0005	2.4252
A to Z ↑	0.0469	0.0745	10.8793	4.2532
B to Z ↓	0.0499	0.0845	4.9983	2.4242
B to Z ↑	0.0467	0.0744	10.8571	4.2542
C to Z ↓	0.0829	0.0824	4.9806	2.4227
C to Z ↑	0.0801	0.0716	10.8426	4.2537
	X17_P16	**X24_P16**	**X17_P16**	**X24_P16**
A to Z ↓	0.0772	0.0903	1.1539	0.8357
A to Z ↑	0.0740	0.0662	2.0714	1.4086
B to Z ↓	0.0766	0.0901	1.1526	0.8342

B to Z ↑	0.0736	0.0660	2.0741	1.4090
C to Z ↓	0.0755	0.0869	1.1527	0.8334
C to Z ↑	0.0721	0.0645	2.0731	1.4089

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P16	3.166e-07	4.544e-12
X8_P16	2.488e-07	4.292e-12
X17_P16	3.914e-07	4.546e-12
X24_P16	6.587e-07	7.819e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	2.843e-03	4.059e-03	6.231e-03	1.059e-02
B to Z	2.728e-03	3.895e-03	5.954e-03	1.017e-02
C to Z	5.790e-03	3.769e-03	5.899e-03	9.822e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	-2.302e-05	-1.729e-05	-3.194e-05	-5.871e-05
B to Z	-1.174e-05	-3.514e-06	-3.692e-06	-2.266e-05
C to Z	3.786e-06	2.633e-06	6.706e-06	2.739e-05

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