C28SOI_SC_8_PR_LL

Release Notes and Known Problems and Solutions

8 track Standard Cell Library comprising Place and Route cells

1 Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library name	C28SOI_SC_8_PR_LL
Library version	5.3
Library type	Standard Cells
Technology	CMOS028_FDSOI

1.2 Related Documentation

- StandardCell_Notes.pdf Present in Design Package.
- User Manual C28SOI_SC_8_PR_LL_um.pdf present in doc directory of Product itself.
- Capacitance Value Decap_Info.csv present in doc directory of Product itself.

2 Release Details

2.1 Current Release Details, Version 5.3

- Previously the PC was cut asymmetric due to which some cells of this library were producing DRC errors with other cells in some configurations. Now this has been corrected in this release. PC on Boundary has been now cut symmetric to NW (45nm both sides) keeping PC to PC space of 90 nm. To support this PC cut, mos sizes have been altered too but all these moses are dummy mos. There is no change in Area or Abstract or characterized data for any Cell. Only change is in PC and RX layers for corrected cells.
- Corrected cells are 6 cells as below -
  - C8T28SOI_LL_FILLERPFOP16
  - C8T28SOI_LL_FILLERPFOP2
  - C8T28SOI_LL_FILLERPFOP32
  - C8T28SOI_LL_FILLERPFOP4
  - C8T28SOI_LL_FILLERPFOP64
  - C8T28SOI_LL_FILLERPFOP8
- The product remains aligned to DP28FDSOI 2.5.

2.2 Version 5.2

- In previous Library release, there was an issue with PCEND cells, Poly Shape got extended at left and right side of cells boundary, which can create shorts in P&R. Now in this release, this issue has been corrected. Below cells have been updated for the same -

C8T28SOI_LVTFILLERPCENDB1	C8T28SOI_LVTFILLERPCENDB16
C8T28SOI_LVTFILLERPCENDB2	C8T28SOI_LVTFILLERPCENDB32
C8T28SOI_LVTFILLERPCENDB4	C8T28SOI_LVTFILLERPCENDB64
C8T28SOI_LVTFILLERPCENDB8	C8T28SOI_LVTFILLERPCENDBL1
C8T28SOI_LVTFILLERPCENDBR1	C8T28SOI_LVTFILLERPCENDT1
C8T28SOI_LVTFILLERPCENDT16	C8T28SOI_LVTFILLERPCENDT2
C8T28SOI_LVTFILLERPCENDT32	C8T28SOI_LVTFILLERPCENDT4
C8T28SOI_LVTFILLERPCENDT64	C8T28SOI_LVTFILLERPCENDT8
C8T28SOI_LVTFILLERPCENDTB1	C8T28SOI_LVTFILLERPCENDTB16
C8T28SOI_LVTFILLERPCENDTB2	C8T28SOI_LVTFILLERPCENDTB32
C8T28SOI_LVTFILLERPCENDTB4	C8T28SOI_LVTFILLERPCENDTB64
C8T28SOI_LVTFILLERPCENDTB8	C8T28SOI_LVTFILLERPCENDTBL1
C8T28SOI_LVTFILLERPCENDTBR1	C8T28SOI_LVTFILLERPCENDTL1
C8T28SOI_LVTFILLERPCENDTR1	

- Below cells, also have been updated for Dummy PC-CUT -

C8T28SOI_LL_FILLERFLPCHKAE16	C8T28SOI_LL_FILLERFLPCHKAE2
C8T28SOI_LL_FILLERFLPCHKAE32	C8T28SOI_LL_FILLERFLPCHKAE4
C8T28SOI_LL_FILLERFLPCHKAE64	C8T28SOI_LL_FILLERFLPCHKAE8
C8T28SOI_LL_FILLERPFOP16	C8T28SOI_LL_FILLERPFOP2
C8T28SOI_LL_FILLERPFOP32	C8T28SOI_LL_FILLERPFOP4
C8T28SOI_LL_FILLERPFOP64	C8T28SOI_LL_FILLERPFOP8

- There is no change in characterized data timing/power/leakage with respect to previous version.
- The product remains aligned to DP28FDSOI 2.5.

2.3 Version 5.1

- Cells have been re-characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.
- To enable support for Cadence Voltus Flow, CCS-Power has been added.
- Characterization corners have been re-defined in-line with DP Specifications.
- The product is aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.

2.4 Version 5.0

- Dummy Poly in layout across various cells has been cut for DFM robustness.
- The Non-split Filler Cell with Antenna Diode has been added:
  - C8T28SOI_LL_ANTPROTGVFILLERNPW6
- 3 cells have been updated to fix DRC abutment issue.
  - C8T28SOI_LLL_PDECAP16
  - C8T28SOI_LLL_PDECAP32
  - C8T28SOI_LLL_PDECAP64
- 1 cell has been updated to fix SRD violations related to HYBRID.
  - C8T28SOI_LL_ANTPROTGVFILLERSNPW8
- Decap Cells mentioned below have been updated to avoid DRC violation associated with PC endcap width notches at design level when PCEND cells are placed at top and bottom of DECAP cells.
  - C8T28SOI_LLL_PDECAP16
  - C8T28SOI_LLL_PDECAP32
  - C8T28SOI_LLL_PDECAP4
  - C8T28SOI_LLL_PDECAP64
  - C8T28SOI_LLL_PDECAP8
- Cells has been characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.
- The product has been aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Global Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.5 Version 4.0

- DECAP cell offer has been re-defined.

– Total 5 cells have been added having large gate length (>30 nm) with GO1 transistors
  - Cells having only PMOS : C8T28SOI_LLL_PDECAP*

– Total 8 cells have been removed .
  - C8T28SOI_LL_DECAPXT8*
  - C8T28SOI_LLF_DECAPXT16/32/64

- TIE High/Low cells have been added :
  – C8T28SOI_LL_TOHX5
  – C8T28SOI_LL_TOLX5
- The product has been aligned to DP28FDSOI 2.4 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.6 Version 3.0

- The product has been aligned to DP28FDSOI 2.3 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.7 Version 2.1

- Total 24 cells has been re-designed to have better manufacturability. Cell Area is not changed for these cells but there are few cells for which abstract is changed. Updated Cells are -

  – Cells with Change in Abstract (5 cells)

C8T28SOI_LL_ANTPROTGVFILLERSNPW8
C8T28SOI_LL_ANTPROT6 (Abstract Change has no Impact on PnR)
C8T28SOI_LL_ANTPROTFILLERSNPW6 (Abstract Change has no Impact on PnR)
C8T28SOI_LL_ANTPROTFILLERSNPW7 (Abstract Change has no Impact on PnR)
C8T28SOI_LL_ANTPROTFILLERSNPW8 (Abstract Change has no Impact on PnR)

  – Cells without any change in Abstract (19 cells).

C8T28SOIDV_LLEGLV_DECAPXT11	C8T28SOIDV_LLEGLV_DECAPXT16
C8T28SOIDV_LLEGLV_DECAPXT32	C8T28SOIDV_LLEGLV_DECAPXT64
C8T28SOI_LL_ANTPROT4	C8T28SOI_LL_ANTPROTGVFILLERNPW8
C8T28SOI_LL_FILLERFLPCHKAE16	C8T28SOI_LL_FILLERFLPCHKAE2
C8T28SOI_LL_FILLERFLPCHKAE32	C8T28SOI_LL_FILLERFLPCHKAE4

C8T28SOI_LL_FILLERFLPCHKAE64	C8T28SOI_LL_FILLERFLPCHKAE8
C8T28SOI_LL_FILLERNPW5	C8T28SOI_LL_FILLERPFOP16
C8T28SOI_LL_FILLERPFOP32	C8T28SOI_LL_FILLERPFOP4
C8T28SOI_LL_FILLERPFOP64	C8T28SOI_LL_FILLERPFOP8
C8T28SOI_LL_FILLERSNPW5	

- There is minimal impact on cell Performance for these Updated Cells. Therefore Library has not be re-characterized for these updated cells. Timing/Power Data is same as of Previous Release.
- The Product is aligned to DP28FDSOI_7ML 1.0.

2.8 Version 2.0

- The Product is aligned to DP28FDSOI_7ML 1.0. Refer to Design Package Documents for more details.
- For Standard Cell Library Specific Features, Refer to StandardCell_Notes.pdf Present in Design Package.

3 Known Problems and Solutions

3.1 DP related Generic Problems

- For Generic Standard cell Library related problem for this DP, please refer to KPS section inside StandardCell_Notes.pdf Present in Design Package.

3.2 Dont_use and dont_touch cells

➥ Specific attributes dont_use and dont_touch in Synopsys Technology File

☞ The “dont_touch” and “dont_use” attributes are defined in the Synopsys Technology Files for few cells. Reason can be -

a) Cell has some specific custom feature. Therefore We want to ensure that Either these cells are not automatically picked during Synthesis unless the designer wishes to specically use them in the design or those are not replaced during Design Optimization.

b) Cell’s functionality is not properly understood by tools.

Cells with such attributes are as following:

– C8T28SOI_LL_ANTPROT4
– C8T28SOI_LL_ANTPROT6

3.3 Mismatch between CDL and SPI for GO2 transistor

➥ Mismatch between cdl and spi netlist due to the name of Go2 transistor

☞ C28SOI_SC_8_PR_LL.cdl has egvlvt and C28SOI_SC_8_PR_LL.spi has eglvtv. The both name are related to the same transistor, therefore it is not an issue.

3.4 C8T28SOI_LL_ANTPROT4 is not Standalone DRC clean.

- C8T28SOI_LL_ANTPROT4 is not standalone DRC clean, had to keep other cell on surroundings. To overcome this issue, there is another ANTPROT cell “C8T28SOI_LL_ANTPROT6” which is standalone DRC clean for fully isolated Designs

3.5 FILLERFLPCHKAE* cells have intentional DRC error.

- FILLERFLPCHKAE* cells have intentional DRC error : DRC : GR11 -> PFET gate minimum width >= 0.08 micron
  – This is to ensure detection & Removal of these cells during final floor plan.
  – Due to this these cells also have following SRD error:
    - RULECHECK SRD_RX_11R ==> PFET gate minimum width > = 0.100

4 Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.

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