Layout Finishing and SoC Tiling: **FE tiling**

December 12th, 2012

CMOS and derivative PDK

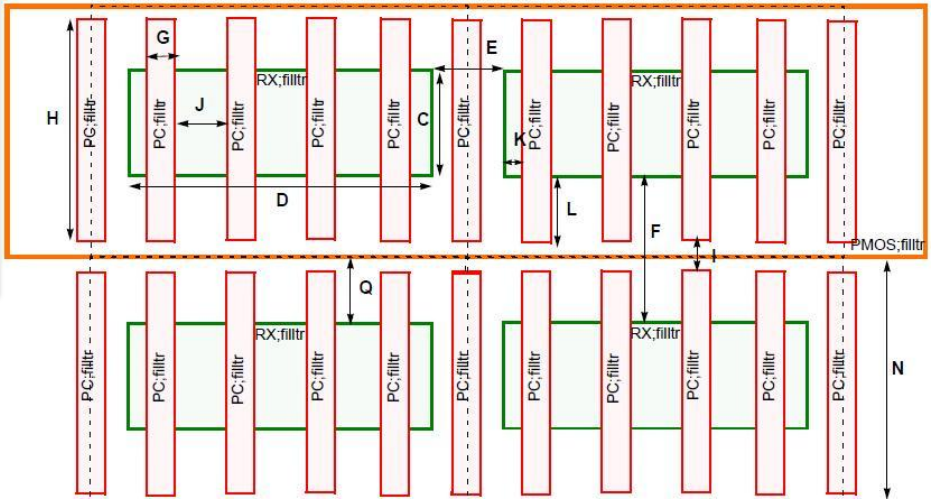
life.augmented

Program Management & Services / Process Design Kit

Dummy transistors to deal with RTA (Rapid Thermal Anneal)

- What: *Gate distribution must be uniform over the circuit/SoC*
- Why:
  - The radiation heating of the RTA process is used to achieve both the ultra-shallow junction and the maximum dopant activation rate.
  - The threshold voltage (Vth) shift and Vth variation are directly related to the RTA process.
  - The only parameter the designer can control is the uniformity of the pattern density.

- How:
  - instead of tiling independent shapes of active and poly, “RTA dummy transistors” are tiled.
  - depending on the process, the purpose is *fill* or *filltr*.



Snapshot from 28nm DRM

Warning:
You may reach correct density of active and poly, even if you disable this pass from the tiler GUI.
But in this case, your gds will be rejected at PG.

FE tiler passes

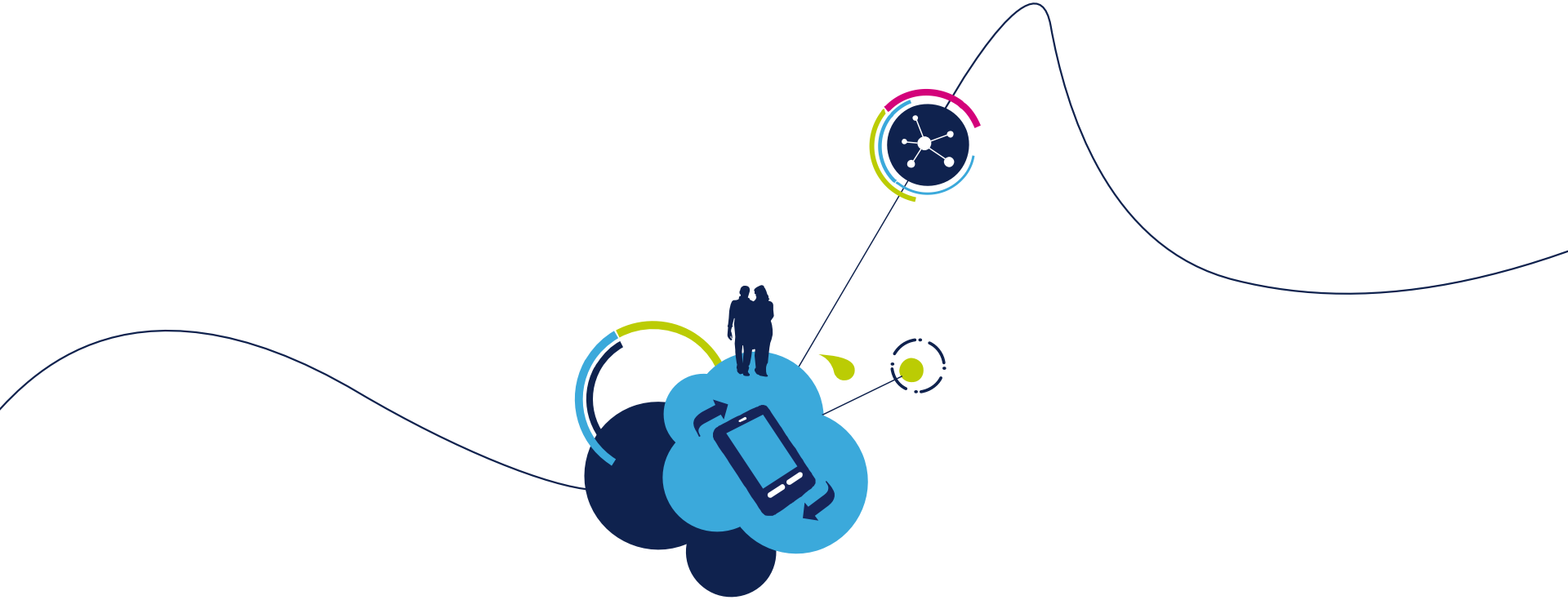
• Please refer to DRM (provided within DKs) to get accurate definition of tiler passes. They come along with targets to be reached:

1. Dummy transistors
   - tile as much as possible, but do not violate the max RX density.
2. PC;fill
   - tile as much as possible, but do not violate the max PC density.
3. RX;fill
   - tile as much as possible, but do not violate the max RX density.

Tiler GUI

Dummy transistors
PC;fill
RX;fill

• You may reach correct density of active and poly, even if you disable the dummy transistor pass from the tiler GUI…
… but in this case, your gds will be rejected at PG visual inspection



Thank You