C28SOI_SC_12_COREPBP10_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 10 nm

Overview

- C28SOI_SC_12_COREPBP10_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

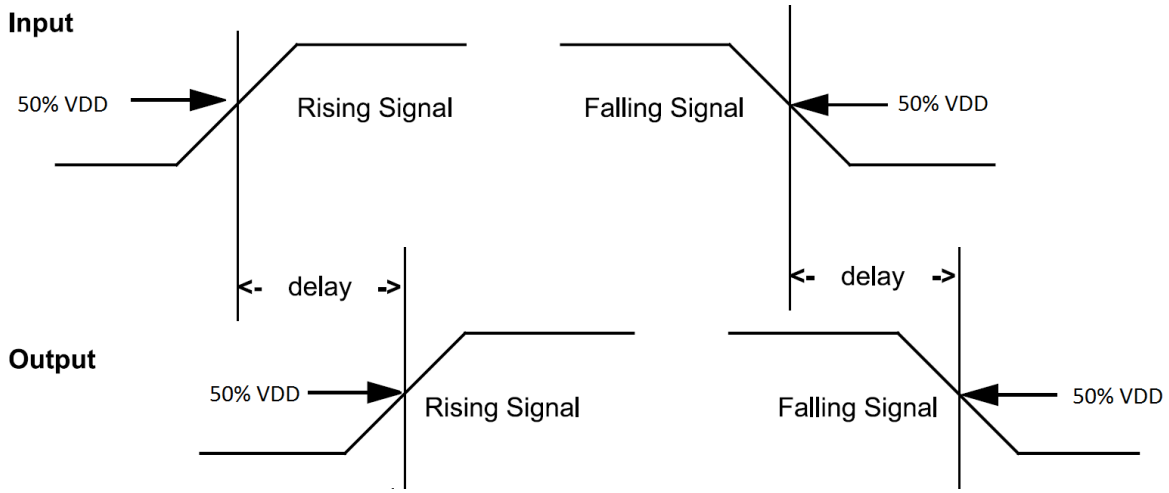


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

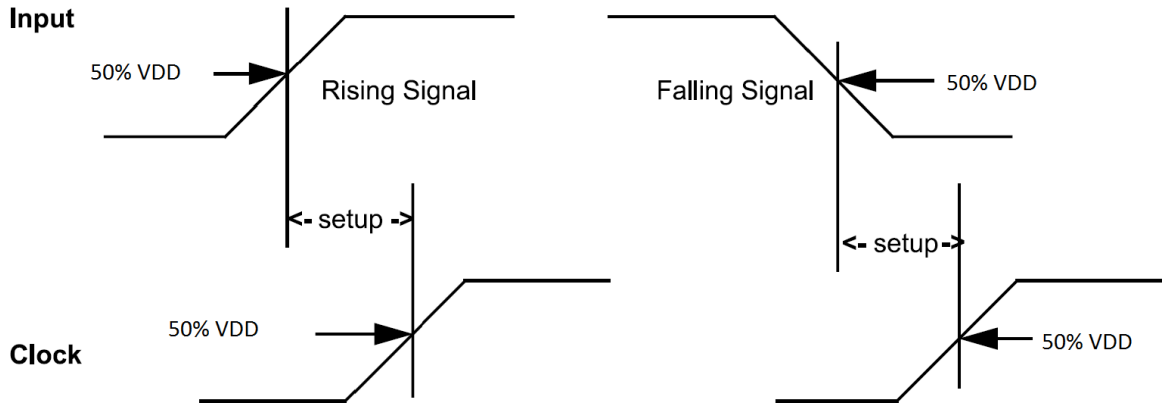


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

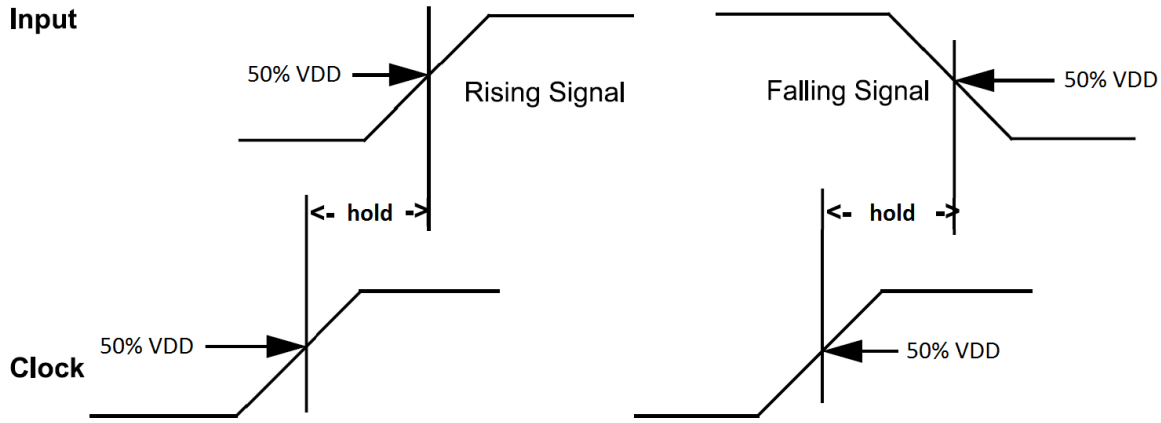


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

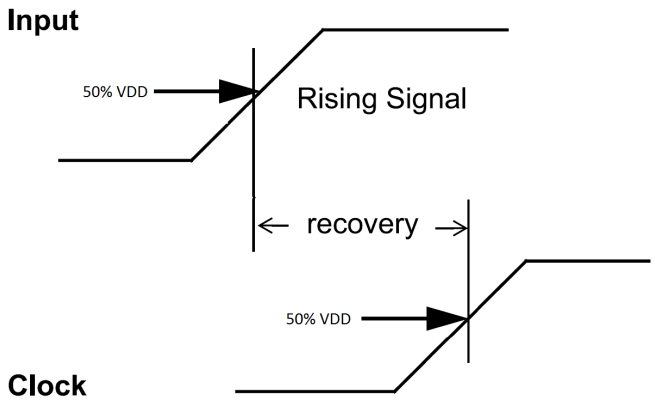


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

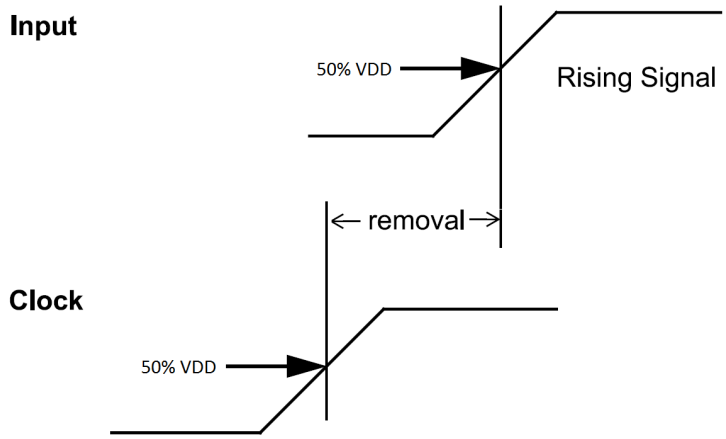


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

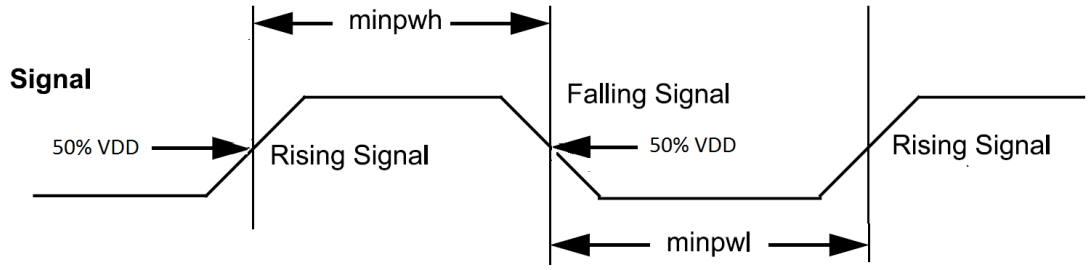


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

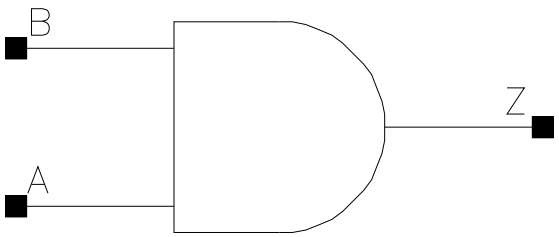
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X25_P10	1.200	1.088	1.3056
X33_P10	1.200	1.360	1.6320
X42_P10	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0009	0.0013	0.0019	0.0024
B	0.0008	0.0012	0.0019	0.0024
	X42_P10			
A	0.0024			
B	0.0024			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0247	0.0206	1.6636	0.8430
A to Z ↑	0.0193	0.0188	2.4278	1.1761
B to Z ↓	0.0233	0.0193	1.6645	0.8430
B to Z ↑	0.0212	0.0205	2.4268	1.1760
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0212	0.0206	0.5577	0.4154

A to Z ↑	0.0183	0.0190	0.7778	0.5877
B to Z ↓	0.0200	0.0186	0.5576	0.4150
B to Z ↑	0.0200	0.0203	0.7773	0.5873
	X42_P10		**X42_P10**	
A to Z ↓	0.0224		0.3370	
A to Z ↑	0.0210		0.4708	
B to Z ↓	0.0204		0.3362	
B to Z ↑	0.0223		0.4707	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	4.309e-05	1.000e-20
X16_P10	9.320e-05	1.000e-20
X25_P10	1.369e-04	1.000e-20
X33_P10	1.881e-04	1.000e-20
X42_P10	2.200e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	1.344e-05	2.602e-05	4.007e-05	9.723e-05
B (output stable)	3.123e-05	5.531e-05	8.674e-05	3.299e-04
A to Z	3.856e-03	6.732e-03	1.033e-02	1.368e-02
B to Z	3.689e-03	6.452e-03	9.887e-03	1.276e-02
	X42_P10			
A (output stable)	9.972e-05			
B (output stable)	3.260e-04			
A to Z	1.662e-02			
B to Z	1.569e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

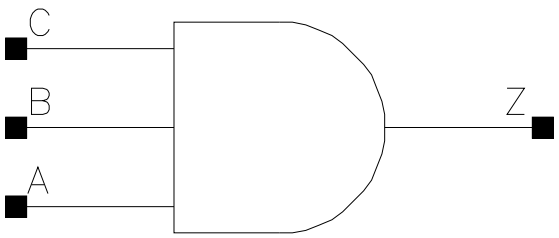
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X25_P10	1.200	1.360	1.6320
X33_P10	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0008	0.0013	0.0020	0.0025
B	0.0007	0.0012	0.0019	0.0023
C	0.0008	0.0012	0.0017	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0267	0.0228	1.6808	0.8221
A to Z ↑	0.0244	0.0239	2.4486	1.1675
B to Z ↓	0.0257	0.0216	1.6806	0.8213
B to Z ↑	0.0257	0.0252	2.4494	1.1683
C to Z ↓	0.0243	0.0203	1.6793	0.8195
C to Z ↑	0.0271	0.0262	2.4463	1.1678
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0227	0.0217	0.5634	0.4210

A to Z ↑	0.0230	0.0226	0.7985	0.5982
B to Z ↓	0.0216	0.0205	0.5626	0.4203
B to Z ↑	0.0243	0.0238	0.7982	0.5981
C to Z ↓	0.0202	0.0193	0.5621	0.4201
C to Z ↑	0.0255	0.0250	0.7973	0.5970

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	4.349e-05	1.000e-20
X17_P10	9.543e-05	1.000e-20
X25_P10	1.369e-04	1.000e-20
X33_P10	1.875e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	1.710e-05	3.407e-05	4.598e-05	6.281e-05
B (output stable)	2.621e-05	5.100e-05	7.316e-05	9.990e-05
C (output stable)	6.731e-05	1.307e-04	1.961e-04	2.721e-04
A to Z	4.280e-03	7.876e-03	1.136e-02	1.483e-02
B to Z	4.104e-03	7.565e-03	1.087e-02	1.416e-02
C to Z	3.944e-03	7.252e-03	1.039e-02	1.352e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

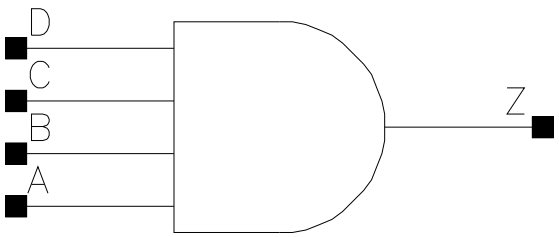
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X6_P10	1.200	1.088	1.3056
X20_P10	1.200	2.312	2.7744
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P10	X6_P10	X20_P10	X27_P10
A	0.0006	0.0009	0.0021	0.0024
B	0.0006	0.0009	0.0021	0.0024
C	0.0005	0.0009	0.0021	0.0024
D	0.0006	0.0009	0.0021	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X6_P10	X4_P10	X6_P10
A to Z ↓	0.0271	0.0243	3.0835	2.0332
A to Z ↑	0.0243	0.0195	7.5181	4.1326
B to Z ↓	0.0261	0.0226	3.0842	2.0319
B to Z ↑	0.0263	0.0208	7.5221	4.1337
C to Z ↓	0.0278	0.0258	3.0531	2.0395
C to Z ↑	0.0246	0.0196	7.5200	4.1364

D to Z ↓	0.0268	0.0238	3.0475	2.0396
D to Z ↑	0.0271	0.0211	7.5271	4.1345
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0238	0.0221	0.5944	0.4211
A to Z ↑	0.0205	0.0234	1.3861	1.0560
B to Z ↓	0.0216	0.0201	0.5935	0.4203
B to Z ↑	0.0216	0.0248	1.3857	1.0560
C to Z ↓	0.0233	0.0212	0.5978	0.4215
C to Z ↑	0.0188	0.0209	1.3849	1.0534
D to Z ↓	0.0209	0.0194	0.5960	0.4212
D to Z ↑	0.0197	0.0223	1.3844	1.0533

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	2.048e-05	1.000e-20
X6_P10	5.013e-05	1.000e-20
X20_P10	1.546e-04	1.000e-20
X27_P10	2.043e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	6.306e-04	1.030e-03	3.010e-03	3.711e-03
B (output stable)	5.883e-04	9.434e-04	2.764e-03	3.450e-03
C (output stable)	5.949e-04	1.015e-03	2.628e-03	3.227e-03
D (output stable)	5.577e-04	9.262e-04	2.362e-03	2.962e-03
A to Z	2.591e-03	4.114e-03	1.249e-02	1.619e-02
B to Z	2.480e-03	3.883e-03	1.159e-02	1.525e-02
C to Z	2.567e-03	4.174e-03	1.101e-02	1.390e-02
D to Z	2.453e-03	3.933e-03	1.008e-02	1.299e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

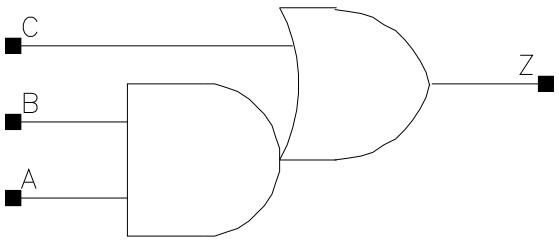
Pin Cycle (vdds)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0008	0.0012	0.0025
B	0.0008	0.0012	0.0023
C	0.0009	0.0013	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0305	0.0280	1.7023	0.8336
A to Z ↑	0.0200	0.0187	2.3623	1.1583
B to Z ↓	0.0281	0.0256	1.6976	0.8301
B to Z ↑	0.0220	0.0207	2.3605	1.1587
C to Z ↓	0.0284	0.0260	1.6959	0.8308
C to Z ↑	0.0194	0.0188	2.3447	1.1511
	X33_P10		**X33_P10**	
A to Z ↓	0.0279		0.4233	
A to Z ↑	0.0190		0.5842	

B to Z ↓	0.0259		0.4224	
B to Z ↑	0.0207		0.5841	
C to Z ↓	0.0262		0.4221	
C to Z ↑	0.0187		0.5805	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	3.903e-05	1.000e-20
X17_P10	8.395e-05	1.000e-20
X33_P10	1.665e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	5.527e-05	8.647e-05	2.025e-04
B (output stable)	6.279e-05	1.018e-04	2.558e-04
C (output stable)	6.109e-05	1.020e-04	2.356e-04
A to Z	4.060e-03	7.402e-03	1.470e-02
B to Z	3.860e-03	7.028e-03	1.390e-02
C to Z	4.286e-03	7.767e-03	1.553e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

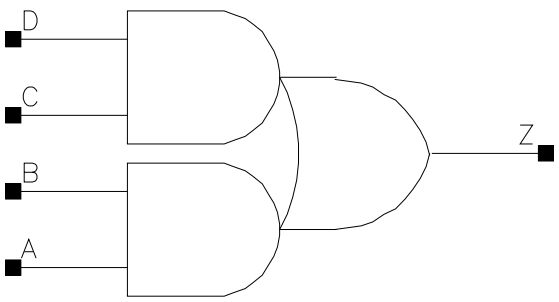
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0012	0.0023
B	0.0008	0.0012	0.0022
C	0.0007	0.0011	0.0024
D	0.0008	0.0012	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0333	0.0295	1.6473	0.8307
A to Z ↑	0.0261	0.0246	2.3302	1.1607
B to Z ↓	0.0307	0.0273	1.6404	0.8280
B to Z ↑	0.0279	0.0268	2.3292	1.1597

C to Z ↓	0.0314	0.0285	1.6414	0.8285
C to Z ↑	0.0219	0.0208	2.3233	1.1555
D to Z ↓	0.0298	0.0268	1.6377	0.8264
D to Z ↑	0.0242	0.0228	2.3222	1.1549
	X33_P10		**X33_P10**	
A to Z ↓	0.0282		0.4238	
A to Z ↑	0.0226		0.5866	
B to Z ↓	0.0265		0.4236	
B to Z ↑	0.0248		0.5865	
C to Z ↓	0.0272		0.4229	
C to Z ↑	0.0192		0.5845	
D to Z ↓	0.0256		0.4223	
D to Z ↑	0.0211		0.5844	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	4.850e-05	1.000e-20
X17_P10	1.028e-04	1.000e-20
X33_P10	1.998e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	3.610e-05	5.151e-05	7.318e-05
B (output stable)	1.456e-04	1.704e-04	1.085e-04
C (output stable)	5.155e-05	8.392e-05	1.889e-04
D (output stable)	5.967e-05	1.017e-04	2.321e-04
A to Z	5.192e-03	9.088e-03	1.697e-02
B to Z	4.836e-03	8.591e-03	1.627e-02
C to Z	4.536e-03	8.021e-03	1.487e-02
D to Z	4.360e-03	7.684e-03	1.421e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

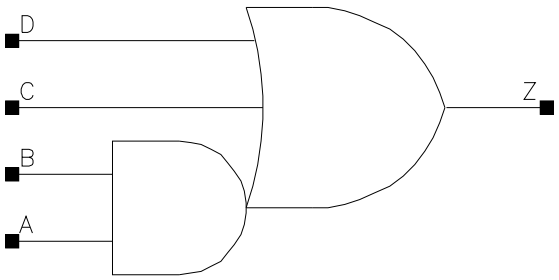
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	0.952	1.1424
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0008	0.0012	0.0022
B	0.0008	0.0012	0.0023
C	0.0008	0.0012	0.0023
D	0.0008	0.0012	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0390	0.0349	1.7650	0.8738
A to Z ↑	0.0215	0.0203	2.3513	1.2027
B to Z ↓	0.0371	0.0326	1.7594	0.8714
B to Z ↑	0.0237	0.0220	2.3504	1.2022
C to Z ↓	0.0381	0.0338	1.7599	0.8716
C to Z ↑	0.0210	0.0200	2.3353	1.1953

D to Z ↓	0.0386	0.0346	1.7596	0.8718
D to Z ↑	0.0206	0.0199	2.3348	1.1950
	X33_P10		**X33_P10**	
A to Z ↓	0.0356		0.4379	
A to Z ↑	0.0202		0.5848	
B to Z ↓	0.0319		0.4354	
B to Z ↑	0.0215		0.5846	
C to Z ↓	0.0350		0.4358	
C to Z ↑	0.0198		0.5821	
D to Z ↓	0.0348		0.4362	
D to Z ↑	0.0189		0.5808	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	3.240e-05	1.000e-20
X17_P10	7.016e-05	1.000e-20
X33_P10	1.405e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	6.783e-05	1.290e-04	2.991e-04
B (output stable)	6.841e-05	1.269e-04	3.334e-04
C (output stable)	3.289e-05	6.020e-05	1.716e-04
D (output stable)	4.627e-05	8.619e-05	3.067e-04
A to Z	4.575e-03	8.067e-03	1.625e-02
B to Z	4.396e-03	7.695e-03	1.510e-02
C to Z	5.011e-03	8.804e-03	1.798e-02
D to Z	4.779e-03	8.415e-03	1.684e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

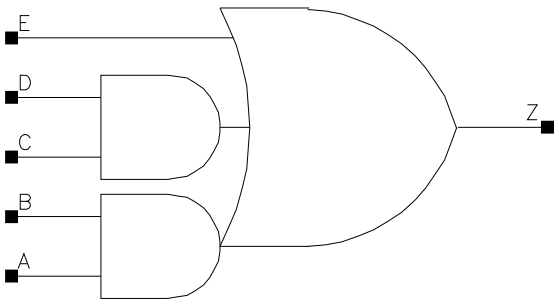
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.088	1.3056
X17_P10	1.200	1.224	1.4688
X33_P10	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0012	0.0023
B	0.0008	0.0012	0.0022
C	0.0009	0.0014	0.0024
D	0.0008	0.0012	0.0022
E	0.0008	0.0012	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0451	0.0395	1.6875	0.8524
A to Z ↑	0.0277	0.0248	2.3119	1.1655

B to Z ↓	0.0433	0.0373	1.6820	0.8502
B to Z ↑	0.0305	0.0271	2.3094	1.1646
C to Z ↓	0.0405	0.0368	1.6806	0.8499
C to Z ↑	0.0229	0.0205	2.2918	1.1579
D to Z ↓	0.0376	0.0336	1.6723	0.8455
D to Z ↑	0.0251	0.0223	2.2907	1.1576
E to Z ↓	0.0402	0.0355	1.6741	0.8467
E to Z ↑	0.0220	0.0198	2.2733	1.1499
	X33_P10		**X33_P10**	
A to Z ↓	0.0385		0.4376	
A to Z ↑	0.0255		0.5888	
B to Z ↓	0.0361		0.4367	
B to Z ↑	0.0277		0.5885	
C to Z ↓	0.0353		0.4362	
C to Z ↑	0.0205		0.5845	
D to Z ↓	0.0325		0.4345	
D to Z ↑	0.0222		0.5840	
E to Z ↓	0.0345		0.4350	
E to Z ↑	0.0198		0.5802	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	4.110e-05	1.000e-20
X17_P10	8.699e-05	1.000e-20
X33_P10	1.664e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.068e-05	3.293e-05	7.478e-05
B (output stable)	2.720e-05	3.957e-05	1.012e-04
C (output stable)	8.447e-05	1.169e-04	2.912e-04
D (output stable)	9.868e-05	1.415e-04	3.250e-04
E (output stable)	1.371e-04	1.805e-04	4.188e-04
A to Z	6.071e-03	1.026e-02	2.002e-02
B to Z	5.881e-03	9.877e-03	1.910e-02
C to Z	4.971e-03	8.605e-03	1.648e-02
D to Z	4.747e-03	8.171e-03	1.557e-02
E to Z	5.232e-03	8.916e-03	1.717e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

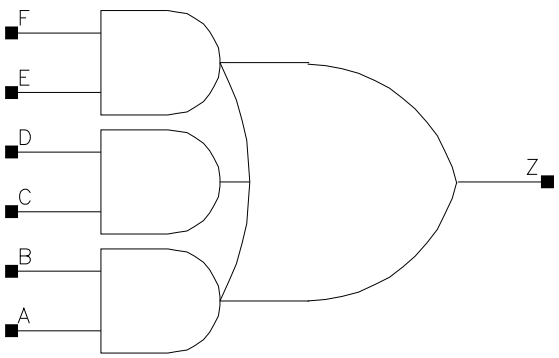
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.360	1.6320
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
A	0.0007	0.0009	0.0011	0.0023

B	0.0008	0.0009	0.0015	0.0022
C	0.0007	0.0008	0.0011	0.0023
D	0.0007	0.0009	0.0011	0.0022
E	0.0008	0.0009	0.0012	0.0023
F	0.0008	0.0009	0.0012	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0448	0.0432	3.1936	1.6964
A to Z ↑	0.0291	0.0287	4.4463	2.3601
B to Z ↓	0.0409	0.0398	3.1716	1.6854
B to Z ↑	0.0307	0.0306	4.4418	2.3569
C to Z ↓	0.0411	0.0401	3.1833	1.6912
C to Z ↑	0.0260	0.0257	4.4132	2.3440
D to Z ↓	0.0390	0.0381	3.1723	1.6854
D to Z ↑	0.0285	0.0282	4.4112	2.3431
E to Z ↓	0.0360	0.0360	3.1682	1.6840
E to Z ↑	0.0215	0.0214	4.3895	2.3324
F to Z ↓	0.0335	0.0335	3.1567	1.6775
F to Z ↑	0.0234	0.0234	4.3893	2.3317
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
A to Z ↓	0.0419	0.0403	0.8556	0.4362
A to Z ↑	0.0274	0.0274	1.1695	0.5910
B to Z ↓	0.0393	0.0380	0.8502	0.4352
B to Z ↑	0.0299	0.0297	1.1687	0.5908
C to Z ↓	0.0397	0.0381	0.8534	0.4359
C to Z ↑	0.0247	0.0251	1.1627	0.5877
D to Z ↓	0.0372	0.0360	0.8500	0.4348
D to Z ↑	0.0271	0.0273	1.1624	0.5874
E to Z ↓	0.0356	0.0357	0.8495	0.4346
E to Z ↑	0.0206	0.0214	1.1578	0.5857
F to Z ↓	0.0333	0.0331	0.8465	0.4329
F to Z ↑	0.0227	0.0236	1.1577	0.5854

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	3.372e-05	1.000e-20
X8_P10	5.816e-05	1.000e-20
X17_P10	1.050e-04	1.000e-20
X33_P10	1.998e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	3.905e-05	4.547e-05	5.762e-05	1.066e-04
B (output stable)	1.148e-04	1.235e-04	1.215e-04	1.545e-04
C (output stable)	4.821e-05	5.766e-05	7.231e-05	1.657e-04
D (output stable)	5.596e-05	6.771e-05	8.464e-05	2.231e-04
E (output stable)	1.392e-04	1.763e-04	2.250e-04	3.824e-04
F (output stable)	1.434e-04	1.789e-04	2.381e-04	4.281e-04

A to Z	5.017e-03	7.015e-03	1.128e-02	2.151e-02
B to Z	4.618e-03	6.543e-03	1.063e-02	2.057e-02
C to Z	4.307e-03	6.149e-03	1.010e-02	1.926e-02
D to Z	4.113e-03	5.900e-03	9.703e-03	1.841e-02
E to Z	3.579e-03	5.292e-03	8.817e-03	1.725e-02
F to Z	3.389e-03	5.042e-03	8.437e-03	1.640e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

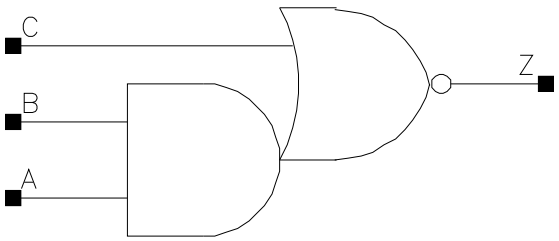
Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008
X44_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X33_P10	X44_P10
A	0.0009	0.0028	0.0057	0.0077
B	0.0009	0.0027	0.0053	0.0072
C	0.0010	0.0030	0.0059	0.0078

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0073	0.0074	2.8530	0.9652
A to Z ↑	0.0141	0.0143	4.2357	1.4226
B to Z ↓	0.0080	0.0082	2.8850	0.9791
B to Z ↑	0.0113	0.0111	4.1720	1.4239
C to Z ↓	0.0083	0.0084	1.7281	0.5912
C to Z ↑	0.0129	0.0127	3.8652	1.3098
	X33_P10	**X44_P10**	**X33_P10**	**X44_P10**
A to Z ↓	0.0076	0.0075	0.4920	0.3736

A to Z ↑	0.0143	0.0143	0.7128	0.5419
B to Z ↓	0.0082	0.0082	0.4990	0.3792
B to Z ↑	0.0111	0.0109	0.7121	0.5394
C to Z ↓	0.0099	0.0100	0.3512	0.2727
C to Z ↑	0.0127	0.0125	0.6556	0.4974

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P10	3.563e-05	1.000e-20
X17_P10	1.045e-04	1.000e-20
X33_P10	2.025e-04	1.000e-20
X44_P10	2.683e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	8.935e-05	2.581e-04	5.550e-04	7.180e-04
B (output stable)	1.003e-04	3.359e-04	7.189e-04	9.248e-04
C (output stable)	1.012e-04	3.049e-04	6.532e-04	8.502e-04
A to Z	2.048e-03	6.307e-03	1.256e-02	1.654e-02
B to Z	1.755e-03	5.089e-03	1.023e-02	1.342e-02
C to Z	2.643e-03	7.836e-03	1.542e-02	2.028e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

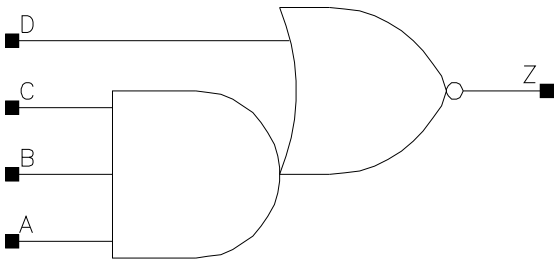
Pin Cycle (vdds)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X29_P10	1.200	3.536	4.2432
X38_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X29_P10	X38_P10
A	0.0010	0.0059	0.0076
B	0.0009	0.0055	0.0073
C	0.0009	0.0053	0.0069
D	0.0010	0.0060	0.0074

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X29_P10	X5_P10	X29_P10
A to Z ↓	0.0111	0.0117	3.9664	0.6885
A to Z ↑	0.0178	0.0178	4.2400	0.7055
B to Z ↓	0.0118	0.0119	3.9814	0.6921
B to Z ↑	0.0157	0.0155	4.2434	0.7114
C to Z ↓	0.0122	0.0120	4.0029	0.6965
C to Z ↑	0.0132	0.0126	4.1851	0.7174
D to Z ↓	0.0103	0.0121	1.7622	0.3532

D to Z ↑	0.0152	0.0153	3.6171	0.6094
	X38_P10		**X38_P10**	
A to Z ↓	0.0113		0.5340	
A to Z ↑	0.0172		0.5324	
B to Z ↓	0.0117		0.5371	
B to Z ↑	0.0150		0.5384	
C to Z ↓	0.0117		0.5404	
C to Z ↑	0.0121		0.5453	
D to Z ↓	0.0128		0.2944	
D to Z ↑	0.0146		0.4609	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.526e-05	1.000e-20
X29_P10	1.992e-04	1.000e-20
X38_P10	2.603e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X29_P10	X38_P10
A (output stable)	5.028e-05	4.174e-04	5.125e-04
B (output stable)	5.876e-05	5.106e-04	6.307e-04
C (output stable)	9.200e-05	9.350e-04	1.170e-03
D (output stable)	1.296e-04	9.591e-04	1.207e-03
A to Z	2.665e-03	1.648e-02	2.086e-02
B to Z	2.345e-03	1.392e-02	1.764e-02
C to Z	2.053e-03	1.156e-02	1.449e-02
D to Z	3.250e-03	1.944e-02	2.447e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

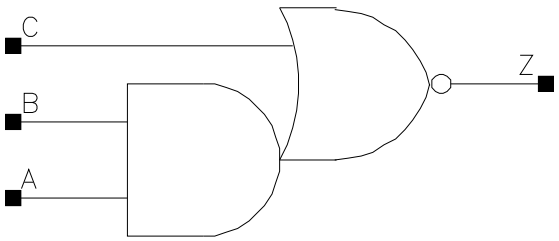
Pin Cycle (vdds)	X5_P10	X29_P10	X38_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X11_P10	1.200	1.088	1.3056
X16_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X11_P10	X16_P10	X23_P10
A	0.0010	0.0021	0.0031	0.0041
B	0.0010	0.0020	0.0029	0.0038
C	0.0010	0.0019	0.0027	0.0039
	X46_P10			
A	0.0080			
B	0.0075			
C	0.0077			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X11_P10	X6_P10	X11_P10
A to Z ↓	0.0093	0.0100	2.7541	1.4010
A to Z ↑	0.0141	0.0148	4.2280	2.0692
B to Z ↓	0.0106	0.0109	2.7823	1.4170

B to Z ↑	0.0118	0.0119	4.1728	2.0782
C to Z ↓	0.0052	0.0060	1.7794	1.0458
C to Z ↑	0.0116	0.0112	3.9081	1.9307
	X16_P10	**X23_P10**	**X16_P10**	**X23_P10**
A to Z ↓	0.0094	0.0097	0.9634	0.7260
A to Z ↑	0.0137	0.0140	1.3936	1.0569
B to Z ↓	0.0108	0.0107	0.9759	0.7344
B to Z ↑	0.0109	0.0111	1.3946	1.0620
C to Z ↓	0.0060	0.0050	0.7238	0.4564
C to Z ↑	0.0105	0.0113	1.2998	0.9854
	X46_P10		**X46_P10**	
A to Z ↓	0.0094		0.3725	
A to Z ↑	0.0136		0.5505	
B to Z ↓	0.0105		0.3772	
B to Z ↑	0.0105		0.5495	
C to Z ↓	0.0052		0.2333	
C to Z ↑	0.0113		0.5117	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P10	3.582e-05	1.000e-20
X11_P10	7.250e-05	1.000e-20
X16_P10	1.037e-04	1.000e-20
X23_P10	1.429e-04	1.000e-20
X46_P10	2.793e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	2.759e-05	7.763e-05	9.639e-05	1.379e-04
B (output stable)	3.838e-05	1.514e-04	1.630e-04	2.496e-04
C (output stable)	3.384e-04	8.588e-04	9.624e-04	1.311e-03
A to Z	2.613e-03	5.560e-03	7.738e-03	1.044e-02
B to Z	2.288e-03	4.708e-03	6.499e-03	8.733e-03
C to Z	1.862e-03	3.726e-03	5.220e-03	7.400e-03
	X46_P10			
A (output stable)	2.532e-04			
B (output stable)	4.342e-04			
C (output stable)	2.254e-03			
A to Z	1.978e-02			
B to Z	1.652e-02			
C to Z	1.411e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

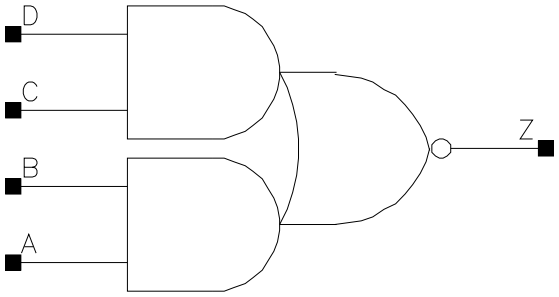
	X46_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P10	X10_P10	X16_P10	X21_P10
A	0.0008	0.0021	0.0031	0.0040
B	0.0008	0.0019	0.0029	0.0038
C	0.0008	0.0020	0.0029	0.0039
D	0.0008	0.0018	0.0027	0.0036
	X42_P10			
A	0.0081			
B	0.0076			
C	0.0077			
D	0.0073			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X10_P10**	**X4_P10**	**X10_P10**
A to Z ↓	0.0105	0.0107	3.4016	1.3466
A to Z ↑	0.0188	0.0156	5.7108	1.9103
B to Z ↓	0.0121	0.0124	3.4405	1.3628
B to Z ↑	0.0163	0.0138	5.6997	1.9611
C to Z ↓	0.0073	0.0071	3.4854	1.3570
C to Z ↑	0.0163	0.0141	5.7408	1.9325
D to Z ↓	0.0082	0.0083	3.5346	1.3772
D to Z ↑	0.0137	0.0119	5.7249	1.9644
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0116	0.0115	0.9671	0.7283
A to Z ↑	0.0163	0.0162	1.2889	0.9990
B to Z ↓	0.0131	0.0127	0.9779	0.7364
B to Z ↑	0.0137	0.0135	1.2906	1.0016
C to Z ↓	0.0076	0.0078	0.9682	0.7303
C to Z ↑	0.0144	0.0149	1.2974	1.0040
D to Z ↓	0.0087	0.0085	0.9826	0.7407
D to Z ↑	0.0116	0.0119	1.3004	1.0064
	X42_P10		**X42_P10**	
A to Z ↓	0.0122		0.3782	
A to Z ↑	0.0166		0.5016	
B to Z ↓	0.0133		0.3824	
B to Z ↑	0.0136		0.4999	
C to Z ↓	0.0084		0.3754	
C to Z ↑	0.0151		0.5051	
D to Z ↓	0.0092		0.3808	
D to Z ↑	0.0121		0.5038	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	2.710e-05	1.000e-20
X10_P10	8.761e-05	1.000e-20
X16_P10	1.249e-04	1.000e-20
X21_P10	1.673e-04	1.000e-20
X42_P10	3.287e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	3.003e-05	7.154e-05	1.362e-04	1.852e-04
B (output stable)	4.418e-05	1.093e-04	2.749e-04	4.006e-04
C (output stable)	8.657e-05	1.941e-04	3.299e-04	4.117e-04
D (output stable)	1.035e-04	2.381e-04	4.645e-04	6.262e-04
A to Z	2.495e-03	6.310e-03	9.692e-03	1.254e-02
B to Z	2.208e-03	5.600e-03	8.378e-03	1.083e-02
C to Z	1.717e-03	4.514e-03	6.803e-03	9.138e-03
D to Z	1.468e-03	3.865e-03	5.599e-03	7.525e-03
	X42_P10			
A (output stable)	3.588e-04			
B (output stable)	7.144e-04			
C (output stable)	7.977e-04			
D (output stable)	1.161e-03			

A to Z	2.490e-02			
B to Z	2.149e-02			
C to Z	1.799e-02			
D to Z	1.492e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

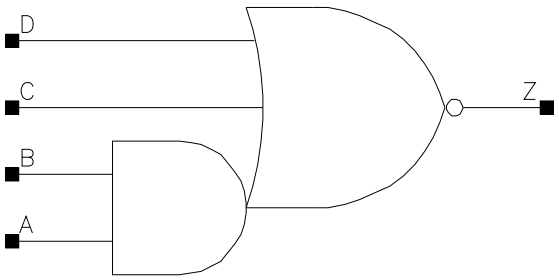
Pin Cycle (vdds)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X35_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P10	X35_P10
A	0.0009	0.0073
B	0.0009	0.0068
C	0.0010	0.0071
D	0.0010	0.0067

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X35_P10	X5_P10	X35_P10
A to Z ↓	0.0086	0.0090	2.8804	0.4247
A to Z ↑	0.0185	0.0173	6.0121	0.7767
B to Z ↓	0.0096	0.0099	2.9181	0.4313
B to Z ↑	0.0153	0.0138	5.9647	0.7761
C to Z ↓	0.0103	0.0142	1.8377	0.3506
C to Z ↑	0.0183	0.0176	5.6625	0.7333
D to Z ↓	0.0097	0.0128	1.8513	0.3506

D to Z ↑	0.0184	0.0170	5.6767	0.7364

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.066e-05	1.000e-20
X35_P10	2.262e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X35_P10
A (output stable)	1.231e-04	1.011e-03
B (output stable)	1.257e-04	1.085e-03
C (output stable)	5.810e-05	6.314e-04
D (output stable)	8.346e-05	9.616e-04
A to Z	2.263e-03	1.645e-02
B to Z	1.945e-03	1.355e-02
C to Z	3.251e-03	2.448e-02
D to Z	2.817e-03	2.017e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

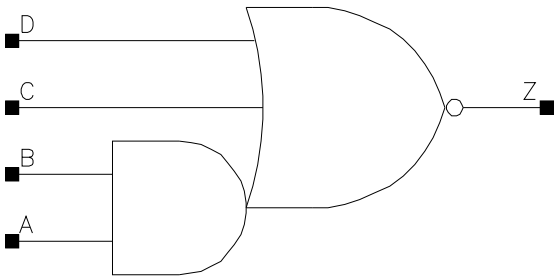
Pin Cycle (vdds)	X5_P10	X35_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X17_P10	1.200	2.448	2.9376
X34_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P10	X17_P10	X34_P10
A	0.0010	0.0040	0.0081
B	0.0010	0.0038	0.0077
C	0.0009	0.0034	0.0067
D	0.0009	0.0032	0.0063

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X17_P10	X4_P10	X17_P10
A to Z ↓	0.0110	0.0120	3.1110	0.8195
A to Z ↑	0.0184	0.0193	6.0615	1.4987
B to Z ↓	0.0128	0.0133	3.1461	0.8285
B to Z ↑	0.0157	0.0158	5.9982	1.5028
C to Z ↓	0.0108	0.0108	2.8765	0.7004
C to Z ↑	0.0136	0.0141	5.7352	1.4280

D to Z ↓	0.0087	0.0078	2.9452	0.7055
D to Z ↑	0.0134	0.0126	5.7565	1.4312
	X34_P10		**X34_P10**	
A to Z ↓	0.0118		0.4199	
A to Z ↑	0.0189		0.7661	
B to Z ↓	0.0133		0.4248	
B to Z ↑	0.0155		0.7636	
C to Z ↓	0.0112		0.3740	
C to Z ↑	0.0137		0.7281	
D to Z ↓	0.0083		0.3778	
D to Z ↑	0.0123		0.7302	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	2.907e-05	1.000e-20
X17_P10	1.166e-04	1.000e-20
X34_P10	2.287e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X17_P10	X34_P10
A (output stable)	2.641e-05	1.259e-04	2.535e-04
B (output stable)	2.979e-05	1.796e-04	3.363e-04
C (output stable)	9.032e-05	4.624e-04	8.999e-04
D (output stable)	1.842e-04	1.178e-03	2.188e-03
A to Z	3.000e-03	1.274e-02	2.472e-02
B to Z	2.686e-03	1.100e-02	2.142e-02
C to Z	2.033e-03	8.624e-03	1.645e-02
D to Z	1.655e-03	6.494e-03	1.237e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

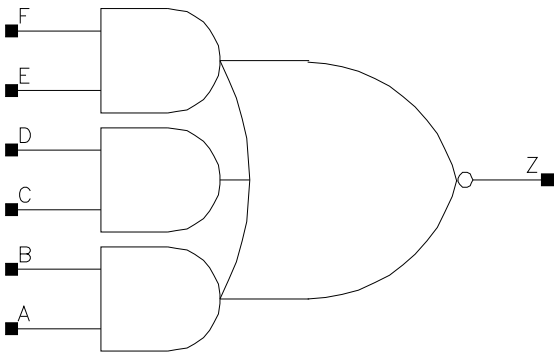
Pin Cycle (vdds)	X4_P10	X17_P10	X34_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X8_P10	1.200	2.176	2.6112
X13_P10	1.200	2.720	3.2640
X17_P10	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P10	X8_P10	X13_P10	X17_P10
A	0.0010	0.0020	0.0030	0.0040

B	0.0010	0.0019	0.0028	0.0037
C	0.0010	0.0019	0.0029	0.0037
D	0.0009	0.0018	0.0027	0.0035
E	0.0011	0.0019	0.0027	0.0036
F	0.0009	0.0017	0.0026	0.0034

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0135	0.0166	2.7593	1.5892
A to Z ↑	0.0273	0.0269	5.8110	2.7061
B to Z ↓	0.0156	0.0182	2.7892	1.6014
B to Z ↑	0.0246	0.0239	5.8079	2.7147
C to Z ↓	0.0120	0.0145	2.7390	1.6036
C to Z ↑	0.0242	0.0244	5.8517	2.7220
D to Z ↓	0.0137	0.0163	2.7769	1.6201
D to Z ↑	0.0214	0.0213	5.8226	2.7238
E to Z ↓	0.0086	0.0104	2.7167	1.6092
E to Z ↑	0.0205	0.0203	5.8068	2.7126
F to Z ↓	0.0096	0.0115	2.7662	1.6328
F to Z ↑	0.0177	0.0170	5.8547	2.7183
	X13_P10	**X17_P10**	**X13_P10**	**X17_P10**
A to Z ↓	0.0158	0.0160	1.0789	0.8225
A to Z ↑	0.0247	0.0249	1.7860	1.3715
B to Z ↓	0.0178	0.0177	1.0874	0.8289
B to Z ↑	0.0221	0.0218	1.7941	1.3730
C to Z ↓	0.0139	0.0139	1.0843	0.8157
C to Z ↑	0.0223	0.0227	1.7993	1.3834
D to Z ↓	0.0158	0.0153	1.0955	0.8241
D to Z ↑	0.0196	0.0196	1.8034	1.3814
E to Z ↓	0.0099	0.0098	1.0833	0.8188
E to Z ↑	0.0189	0.0190	1.7977	1.3758
F to Z ↓	0.0112	0.0107	1.0988	0.8303
F to Z ↑	0.0159	0.0159	1.8027	1.3829

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	4.725e-05	1.000e-20
X8_P10	9.932e-05	1.000e-20
X13_P10	1.426e-04	1.000e-20
X17_P10	1.901e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

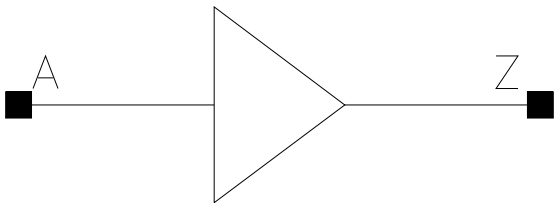
Pin Cycle (vdd)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	4.959e-05	1.163e-04	1.609e-04	2.161e-04
B (output stable)	5.903e-05	2.003e-04	2.318e-04	3.538e-04
C (output stable)	8.844e-05	1.864e-04	2.452e-04	3.292e-04
D (output stable)	9.979e-05	2.866e-04	3.245e-04	4.675e-04
E (output stable)	1.967e-04	4.738e-04	6.126e-04	8.296e-04
F (output stable)	2.270e-04	5.699e-04	6.968e-04	9.658e-04

A to Z	4.559e-03	9.551e-03	1.331e-02	1.763e-02
B to Z	4.180e-03	8.660e-03	1.211e-02	1.585e-02
C to Z	3.522e-03	7.610e-03	1.041e-02	1.383e-02
D to Z	3.184e-03	6.772e-03	9.310e-03	1.223e-02
E to Z	2.577e-03	5.583e-03	7.627e-03	1.011e-02
F to Z	2.258e-03	4.764e-03	6.544e-03	8.581e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.408	0.4896
X6_P10	1.200	0.408	0.4896
X8_P10	1.200	0.408	0.4896
X13_P10	1.200	0.544	0.6528
X16_P10	1.200	0.544	0.6528
X21_P10	1.200	0.680	0.8160
X25_P10	1.200	0.680	0.8160
X29_P10	1.200	0.952	1.1424
X33_P10	1.200	0.952	1.1424
X42_P10	1.200	1.088	1.3056
X50_P10	1.200	1.224	1.4688
X58_P10	1.200	1.496	1.7952
X67_P10	1.200	1.632	1.9584
X75_P10	1.200	1.768	2.1216
X84_P10	1.200	1.904	2.2848
X100_P10	1.200	2.312	2.7744
X134_P10	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0009	0.0009	0.0009	0.0009
	X16_P10	X21_P10	X25_P10	X29_P10
A	0.0009	0.0013	0.0013	0.0018
	X33_P10	X42_P10	X50_P10	X58_P10
A	0.0017	0.0020	0.0024	0.0036

	X67_P10	X75_P10	X84_P10	X100_P10
A	0.0036	0.0035	0.0035	0.0046
	X134_P10			
A	0.0058			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0191	0.0195	3.0139	2.2149
A to Z ↑	0.0152	0.0154	4.3421	3.2459
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0205	0.0234	1.6488	1.0577
A to Z ↑	0.0161	0.0186	2.3497	1.5209
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0254	0.0213	0.8439	0.6511
A to Z ↑	0.0200	0.0175	1.1786	0.9181
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0224	0.0213	0.5595	0.4707
A to Z ↑	0.0182	0.0166	0.7759	0.6582
	X33_P10	**X42_P10**	**X33_P10**	**X42_P10**
A to Z ↓	0.0224	0.0219	0.4187	0.3396
A to Z ↑	0.0173	0.0178	0.5803	0.4670
	X50_P10	**X58_P10**	**X50_P10**	**X58_P10**
A to Z ↓	0.0215	0.0198	0.2818	0.2429
A to Z ↑	0.0175	0.0163	0.3879	0.3335
	X67_P10	**X75_P10**	**X67_P10**	**X75_P10**
A to Z ↓	0.0209	0.0222	0.2133	0.1923
A to Z ↑	0.0172	0.0183	0.2924	0.2614
	X84_P10	**X100_P10**	**X84_P10**	**X100_P10**
A to Z ↓	0.0232	0.0219	0.1739	0.1463
A to Z ↑	0.0190	0.0181	0.2362	0.1979
	X134_P10		**X134_P10**	
A to Z ↓	0.0228		0.1133	
A to Z ↑	0.0191		0.1514	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	2.380e-05	1.000e-20
X6_P10	3.032e-05	1.000e-20
X8_P10	3.981e-05	1.000e-20
X13_P10	5.086e-05	1.000e-20
X16_P10	6.687e-05	1.000e-20
X21_P10	9.345e-05	1.000e-20
X25_P10	1.086e-04	1.000e-20
X29_P10	1.215e-04	1.000e-20
X33_P10	1.356e-04	1.000e-20
X42_P10	1.723e-04	1.000e-20
X50_P10	2.098e-04	1.000e-20
X58_P10	2.605e-04	1.000e-20
X67_P10	2.859e-04	1.000e-20
X75_P10	3.112e-04	1.000e-20

X84_P10	3.366e-04	1.000e-20
X100_P10	4.126e-04	1.000e-20
X134_P10	5.393e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	2.598e-03	2.958e-03	3.552e-03	4.944e-03
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	6.189e-03	8.090e-03	9.202e-03	1.047e-02
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	1.169e-02	1.463e-02	1.733e-02	2.064e-02
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	2.328e-02	2.631e-02	2.923e-02	3.519e-02
	X134_P10			
A to Z	4.815e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

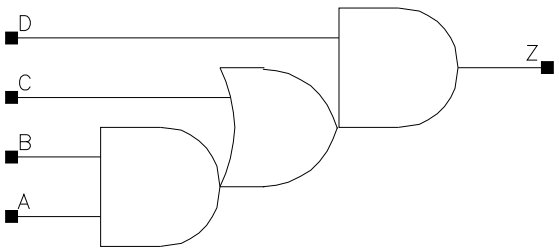
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P10			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.632	1.9584
X25_P10	1.200	1.768	2.1216
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0012	0.0025	0.0024	0.0024
B	0.0012	0.0022	0.0022	0.0022
C	0.0012	0.0027	0.0027	0.0027
D	0.0017	0.0023	0.0024	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0249	0.0236	1.6802	0.8325
A to Z ↑	0.0250	0.0238	2.3902	1.1648
B to Z ↓	0.0227	0.0212	1.6769	0.8306
B to Z ↑	0.0259	0.0244	2.3896	1.1628
C to Z ↓	0.0223	0.0209	1.6742	0.8293
C to Z ↑	0.0189	0.0175	2.3651	1.1527

D to Z ↓	0.0223	0.0199	1.6600	0.8236
D to Z ↑	0.0209	0.0185	2.3709	1.1554
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0262	0.0279	0.5647	0.4243
A to Z ↑	0.0264	0.0281	0.7887	0.5929
B to Z ↓	0.0239	0.0262	0.5639	0.4244
B to Z ↑	0.0271	0.0291	0.7878	0.5916
C to Z ↓	0.0236	0.0257	0.5623	0.4228
C to Z ↑	0.0198	0.0214	0.7792	0.5850
D to Z ↓	0.0217	0.0230	0.5568	0.4176
D to Z ↑	0.0206	0.0220	0.7816	0.5864

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	6.837e-05	1.000e-20
X17_P10	1.356e-04	1.000e-20
X25_P10	1.658e-04	1.000e-20
X33_P10	1.961e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	7.557e-05	1.609e-04	1.625e-04	1.412e-04
B (output stable)	1.208e-04	2.634e-04	2.671e-04	2.268e-04
C (output stable)	3.395e-04	5.527e-04	5.587e-04	5.277e-04
D (output stable)	1.193e-04	1.800e-04	1.823e-04	1.795e-04
A to Z	5.672e-03	1.062e-02	1.377e-02	1.681e-02
B to Z	5.303e-03	9.736e-03	1.286e-02	1.604e-02
C to Z	4.662e-03	8.431e-03	1.131e-02	1.411e-02
D to Z	5.754e-03	1.044e-02	1.318e-02	1.573e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

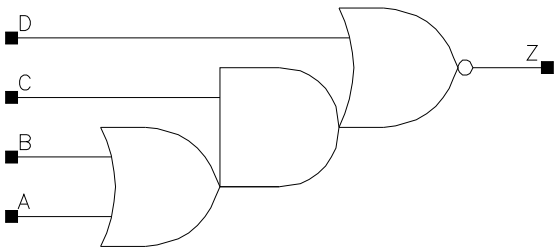
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.952	1.1424
X11_P10	1.200	1.496	1.7952
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X16_P10	X21_P10
A	0.0011	0.0020	0.0030	0.0040
B	0.0010	0.0019	0.0030	0.0039
C	0.0010	0.0019	0.0029	0.0039
D	0.0013	0.0020	0.0029	0.0039

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0115	0.0110	2.7289	1.4316
A to Z ↑	0.0223	0.0208	5.9486	3.1216
B to Z ↓	0.0108	0.0105	2.6603	1.4049
B to Z ↑	0.0216	0.0206	5.9605	3.1273
C to Z ↓	0.0112	0.0108	2.5352	1.3321
C to Z ↑	0.0137	0.0126	4.1594	2.1434

D to Z ↓	0.0059	0.0048	1.7299	0.8734
D to Z ↑	0.0140	0.0126	4.4137	2.2818
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0109	0.0112	0.9591	0.7406
A to Z ↑	0.0191	0.0203	1.9904	1.5456
B to Z ↓	0.0100	0.0104	0.9656	0.7424
B to Z ↑	0.0193	0.0199	1.9943	1.5486
C to Z ↓	0.0108	0.0109	0.9099	0.6985
C to Z ↑	0.0119	0.0121	1.4160	1.0634
D to Z ↓	0.0048	0.0049	0.6058	0.4616
D to Z ↑	0.0117	0.0117	1.4923	1.1316

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	4.043e-05	1.000e-20
X11_P10	7.782e-05	1.000e-20
X16_P10	1.112e-04	1.000e-20
X21_P10	1.478e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	3.148e-05	5.678e-05	7.424e-05	1.212e-04
B (output stable)	4.313e-05	7.177e-05	9.294e-05	1.639e-04
C (output stable)	1.007e-04	2.024e-04	2.750e-04	3.813e-04
D (output stable)	4.585e-04	9.453e-04	1.333e-03	1.925e-03
A to Z	3.728e-03	6.668e-03	9.405e-03	1.303e-02
B to Z	3.104e-03	5.619e-03	8.143e-03	1.092e-02
C to Z	2.781e-03	4.975e-03	7.128e-03	9.697e-03
D to Z	2.093e-03	3.798e-03	5.347e-03	7.097e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

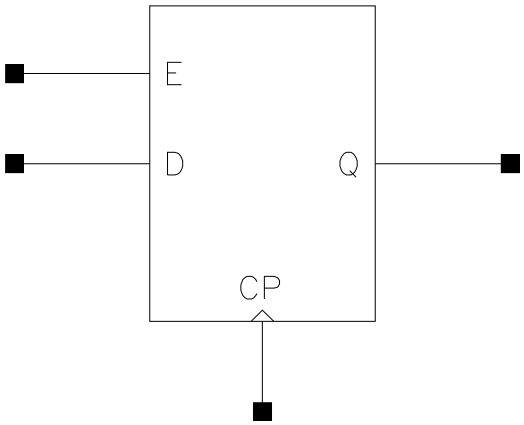
Pin Cycle (vdds)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.128	3.7536
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008
E	0.0013	0.0013	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0312	0.0362	1.6611	0.8543
CP to Q ↑	0.0395	0.0428	2.3979	1.2007
	X33_P10		**X33_P10**	
CP to Q ↓	0.0551		0.4237	
CP to Q ↑	0.0677		0.5938	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0385	0.0385	0.0385
CP ↑	min_pulse_width to CP	0.0271	0.0318	0.0224
D ↓	hold_rising to CP	-0.0071	-0.0071	-0.0071
D ↑	hold_rising to CP	0.0005	0.0005	0.0005
D ↓	setup_rising to CP	0.0361	0.0361	0.0361
D ↑	setup_rising to CP	0.0239	0.0239	0.0239
E ↓	hold_rising to CP	-0.0018	-0.0018	-0.0018
E ↑	hold_rising to CP	0.0036	0.0004	0.0036
E ↓	setup_rising to CP	0.0430	0.0430	0.0430
E ↑	setup_rising to CP	0.0418	0.0418	0.0418

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	1.459e-04	1.000e-20
X17_P10	1.720e-04	1.000e-20
X33_P10	2.566e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

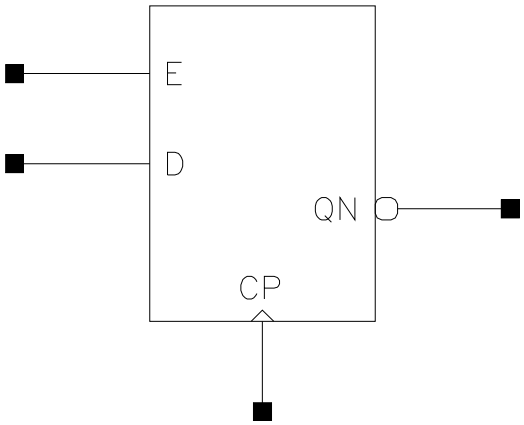
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.145e-02	1.145e-02	1.146e-02
Clock 100Mhz Data 25Mhz	1.514e-02	1.678e-02	2.060e-02
Clock 100Mhz Data 50Mhz	1.883e-02	2.211e-02	2.974e-02
Clock = 0 Data 100Mhz	7.399e-03	7.400e-03	7.400e-03
Clock = 1 Data 100Mhz	2.098e-03	2.098e-03	2.098e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.264	3.9168
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008
E	0.0010	0.0013	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0544	0.0520	1.7102	0.8201
CP to QN ↑	0.0422	0.0430	2.4262	1.1648
	X33_P10		**X33_P10**	
CP to QN ↓	0.0562		0.4250	
CP to QN ↑	0.0477		0.5958	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0385	0.0385	0.0385
CP ↑	min_pulse_width to CP	0.0224	0.0237	0.0271
D ↓	hold_rising to CP	-0.0071	-0.0071	-0.0071
D ↑	hold_rising to CP	0.0005	0.0005	0.0005
D ↓	setup_rising to CP	0.0361	0.0361	0.0361
D ↑	setup_rising to CP	0.0239	0.0239	0.0239
E ↓	hold_rising to CP	-0.0018	-0.0018	-0.0018
E ↑	hold_rising to CP	0.0004	0.0004	0.0036
E ↓	setup_rising to CP	0.0430	0.0430	0.0430
E ↑	setup_rising to CP	0.0418	0.0418	0.0418

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	1.447e-04	1.000e-20
X17_P10	1.898e-04	1.000e-20
X33_P10	2.501e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

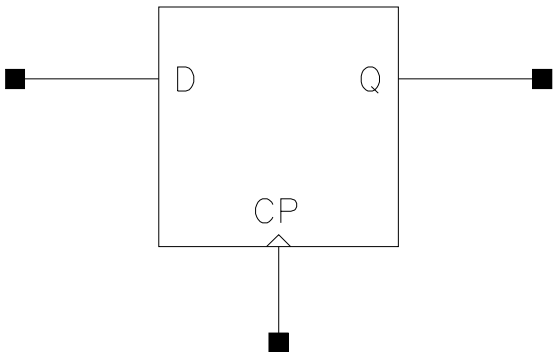
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.144e-02	1.144e-02	1.145e-02
Clock 100Mhz Data 25Mhz	1.513e-02	1.698e-02	2.054e-02
Clock 100Mhz Data 50Mhz	1.882e-02	2.252e-02	2.963e-02
Clock = 0 Data 100Mhz	7.401e-03	7.398e-03	7.398e-03
Clock = 1 Data 100Mhz	2.098e-03	2.098e-03	2.098e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.176	2.6112
X17_P10	1.200	2.448	2.9376
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0009	0.0009	0.0009

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0326	0.0364	1.6517	0.8462
CP to Q ↑	0.0396	0.0445	2.3198	1.1771
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to Q ↓	0.0465	0.0484	0.4979	0.4514
CP to Q ↑	0.0516	0.0527	0.6616	0.6037

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0385	0.0385	0.0385	0.0385
CP ↑	min_pulse_width to CP	0.0271	0.0283	0.0377	0.0377
D ↓	hold_rising to CP	0.0151	0.0124	0.0124	0.0124
D ↑	hold_rising to CP	0.0123	0.0123	0.0123	0.0123
D ↓	setup_rising to CP	0.0198	0.0197	0.0197	0.0197
D ↑	setup_rising to CP	0.0120	0.0120	0.0120	0.0120

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	1.129e-04	1.000e-20
X17_P10	1.421e-04	1.000e-20
X30_P10	1.834e-04	1.000e-20
X33_P10	1.932e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

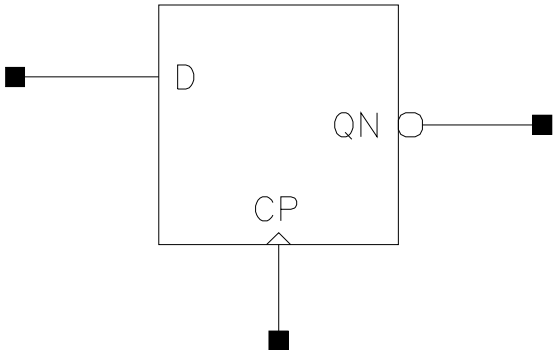
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.188e-02	1.194e-02	1.196e-02	1.196e-02
Clock 100Mhz Data 25Mhz	1.383e-02	1.586e-02	1.986e-02	2.080e-02
Clock 100Mhz Data 50Mhz	1.579e-02	1.979e-02	2.776e-02	2.964e-02
Clock = 0 Data 100Mhz	4.960e-03	5.092e-03	5.133e-03	5.154e-03
Clock = 1 Data 100Mhz	2.471e-05	2.466e-05	2.473e-05	2.480e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0009	0.0009	0.0009

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0320	0.0373	1.7017	0.8724
CP to QN ↑	0.0331	0.0358	2.3153	1.1789
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to QN ↓	0.0554	0.0561	0.4668	0.4240
CP to QN ↑	0.0446	0.0510	0.6390	0.5946

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0338	0.0337	0.0385	0.0385
CP ↑	min_pulse_width to CP	0.0237	0.0283	0.0271	0.0283
D ↓	hold_rising to CP	0.0146	0.0146	0.0124	0.0150
D ↑	hold_rising to CP	0.0178	0.0177	0.0129	0.0123
D ↓	setup_rising to CP	0.0149	0.0149	0.0197	0.0198
D ↑	setup_rising to CP	0.0120	0.0120	0.0120	0.0120

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	1.060e-04	1.000e-20
X17_P10	1.324e-04	1.000e-20
X30_P10	2.055e-04	1.000e-20
X33_P10	2.175e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

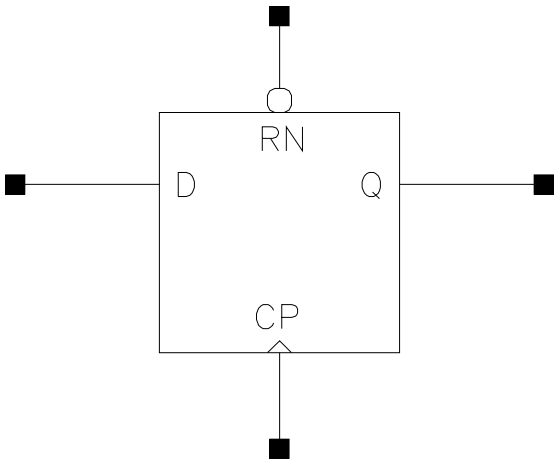
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.154e-02	1.155e-02	1.169e-02	1.175e-02
Clock 100Mhz Data 25Mhz	1.330e-02	1.501e-02	1.809e-02	1.927e-02
Clock 100Mhz Data 50Mhz	1.505e-02	1.848e-02	2.449e-02	2.679e-02
Clock = 0 Data 100Mhz	4.384e-03	4.384e-03	4.662e-03	4.737e-03
Clock = 1 Data 100Mhz	2.451e-05	2.457e-05	2.478e-05	2.498e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0011	0.0011
D	0.0009	0.0009
RN	0.0011	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0380	0.0483	0.8528	0.5048
CP to Q ↑	0.0458	0.0526	1.1822	0.6643
RN to Q ↓	0.0492	0.0557	0.8339	0.4891

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0385	0.0398
CP ↑	min_pulse_width to CP	0.0318	0.0377
D ↓	hold_rising to CP	0.0129	0.0124
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0197	0.0224
D ↑	setup_rising to CP	0.0146	0.0146
RN ↓	min_pulse_width to RN	0.0735	0.0952
RN ↑	recovery_rising to CP	0.0097	0.0097
RN ↑	removal_rising to CP	-0.0033	-0.0033

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P10	1.610e-04	1.000e-20
X30_P10	2.086e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

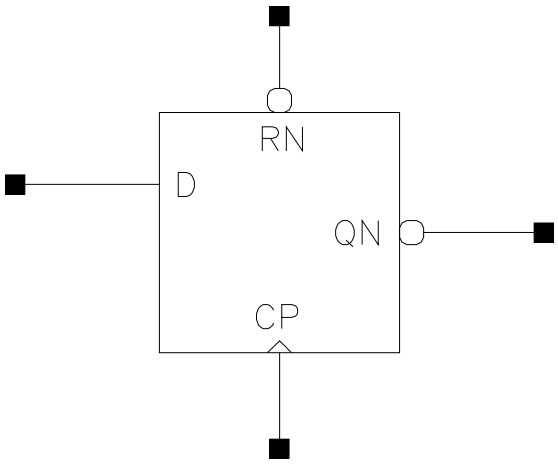
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	1.258e-02	1.258e-02
Clock 100Mhz Data 25Mhz	1.675e-02	2.073e-02
Clock 100Mhz Data 50Mhz	2.091e-02	2.889e-02
Clock = 0 Data 100Mhz	5.924e-03	5.929e-03
Clock = 1 Data 100Mhz	2.557e-05	2.545e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0011	0.0011
D	0.0009	0.0009
RN	0.0011	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.0528	0.0575	0.8152	0.4678
CP to QN ↑	0.0429	0.0468	1.1545	0.6419
RN to QN ↑	0.0560	0.0596	1.1532	0.6414

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0385	0.0385
CP ↑	min_pulse_width to CP	0.0271	0.0271
D ↓	hold_rising to CP	0.0129	0.0129
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0224	0.0224
D ↑	setup_rising to CP	0.0146	0.0146
RN ↓	min_pulse_width to RN	0.0588	0.0637
RN ↑	recovery_rising to CP	0.0097	0.0097
RN ↑	removal_rising to CP	-0.0033	-0.0033

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P10	1.731e-04	1.000e-20
X30_P10	2.073e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

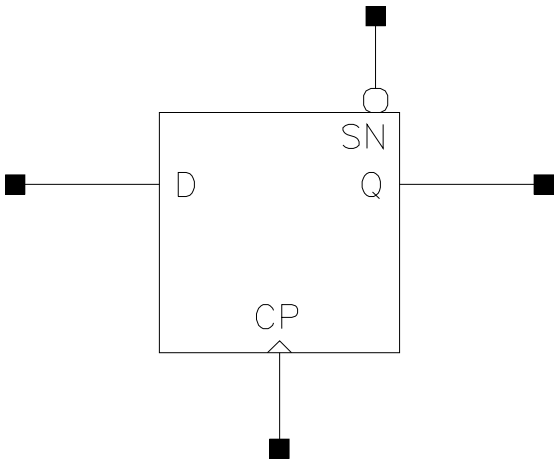
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	1.257e-02	1.257e-02
Clock 100Mhz Data 25Mhz	1.689e-02	1.935e-02
Clock 100Mhz Data 50Mhz	2.121e-02	2.613e-02
Clock = 0 Data 100Mhz	5.993e-03	5.975e-03
Clock = 1 Data 100Mhz	2.466e-05	2.517e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0011	0.0011
D	0.0009	0.0009
SN	0.0015	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0380	0.0482	0.8541	0.5013
CP to Q ↑	0.0453	0.0521	1.1818	0.6633
SN to Q ↑	0.0360	0.0401	1.1694	0.6513

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0432	0.0432
CP ↑	min_pulse_width to CP	0.0318	0.0377
D ↓	hold_rising to CP	0.0130	0.0129
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0246	0.0246
D ↑	setup_rising to CP	0.0120	0.0120
SN ↓	min_pulse_width to SN	0.0457	0.0554
SN ↑	recovery_rising to CP	0.0032	0.0032
SN ↑	removal_rising to CP	0.0217	0.0217

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P10	1.492e-04	1.000e-20
X30_P10	1.838e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

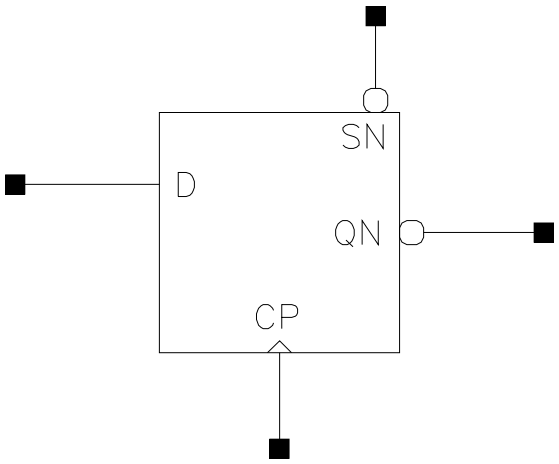
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	1.272e-02	1.268e-02
Clock 100Mhz Data 25Mhz	1.686e-02	2.071e-02
Clock 100Mhz Data 50Mhz	2.101e-02	2.873e-02
Clock = 0 Data 100Mhz	5.840e-03	5.839e-03
Clock = 1 Data 100Mhz	2.513e-05	2.522e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0011	0.0011
D	0.0009	0.0009
SN	0.0015	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.0524	0.0571	0.8171	0.4687
CP to QN ↑	0.0429	0.0467	1.1524	0.6409
SN to QN ↓	0.0438	0.0483	0.8169	0.4688

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0432	0.0432
CP ↑	min_pulse_width to CP	0.0271	0.0271
D ↓	hold_rising to CP	0.0130	0.0130
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0246	0.0246
D ↑	setup_rising to CP	0.0120	0.0120
SN ↓	min_pulse_width to SN	0.0381	0.0381
SN ↑	recovery_rising to CP	0.0032	0.0032
SN ↑	removal_rising to CP	0.0217	0.0217

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P10	1.826e-04	1.000e-20
X30_P10	2.296e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

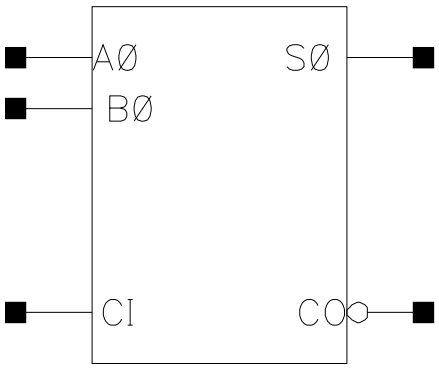
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	1.270e-02	1.269e-02
Clock 100Mhz Data 25Mhz	1.697e-02	1.941e-02
Clock 100Mhz Data 50Mhz	2.124e-02	2.614e-02
Clock = 0 Data 100Mhz	5.840e-03	5.842e-03
Clock = 1 Data 100Mhz	2.531e-05	2.517e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_-P10	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_-P10	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_-P10	1.200	3.672	4.4064
C12T28SOI_LLS1_-FA1X33_P10	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10
A0	0.0038	0.0077	0.0033	0.0065
B0	0.0034	0.0074	0.0036	0.0063
CI	0.0025	0.0056	0.0026	0.0045

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10
A0 to CO ↓	0.0333	0.0369	1.7255	0.4493
A0 to CO ↑	0.0265	0.0284	2.3951	0.6147
A0 to S0 ↓	0.0357	0.0457	1.7045	0.4388
A0 to S0 ↑	0.0367	0.0458	2.3679	0.6062
B0 to CO ↓	0.0334	0.0377	1.7302	0.4511
B0 to CO ↑	0.0277	0.0299	2.3964	0.6127
B0 to S0 ↓	0.0364	0.0468	1.7053	0.4390
B0 to S0 ↑	0.0373	0.0469	2.3684	0.6062
CI to CO ↓	0.0333	0.0380	1.7308	0.4497
CI to CO ↑	0.0278	0.0295	2.3939	0.6143
CI to S0 ↓	0.0363	0.0467	1.7064	0.4390
CI to S0 ↑	0.0377	0.0476	2.3677	0.6060
	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10
A0 to CO ↓	0.0222	0.0278	3.1885	0.5481
A0 to CO ↑	0.0206	0.0239	2.4313	0.6005
A0 to S0 ↓	0.0475	0.0595	1.8443	0.4586
A0 to S0 ↑	0.0438	0.0479	2.4567	0.6165
B0 to CO ↓	0.0235	0.0293	3.1899	0.5488
B0 to CO ↑	0.0187	0.0225	2.4283	0.6007
B0 to S0 ↓	0.0479	0.0611	1.8437	0.4585
B0 to S0 ↑	0.0442	0.0493	2.4576	0.6164
CI to CO ↓	0.0238	0.0427	3.1841	0.5541
CI to CO ↑	0.0202	0.0254	2.4941	0.6054
CI to S0 ↓	0.0279	0.0369	1.8448	0.4592
CI to S0 ↑	0.0237	0.0242	2.4577	0.6167

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_FA1X8_P10	1.479e-04	1.000e-20
C12T28SOI_LL_FA1X33_P10	3.973e-04	1.000e-20
C12T28SOI_LLS1_FA1X8_P10	3.201e-04	1.000e-20
C12T28SOI_LLS1_FA1X33_P10	6.636e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10
A0 to CO	5.949e-03	1.858e-02	8.726e-03	2.295e-02
A0 to S0	5.956e-03	1.913e-02	1.165e-02	2.817e-02
B0 to CO	6.035e-03	1.900e-02	8.814e-03	2.326e-02
B0 to S0	5.923e-03	1.916e-02	1.187e-02	2.877e-02
CI to CO	6.160e-03	1.935e-02	6.350e-03	2.149e-02
CI to S0	5.903e-03	1.916e-02	7.244e-03	2.292e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X33_P10	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X33_P10
A0	0.0013	0.0038
B0	0.0011	0.0032

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
A0 to CO ↓	0.0269	0.0250	1.7087	0.4234
A0 to CO ↑	0.0243	0.0226	2.3683	0.6096
A0 to S0 ↓	0.0337	0.0325	1.6744	0.4234
A0 to S0 ↑	0.0331	0.0384	2.3373	0.6012
B0 to CO ↓	0.0260	0.0229	1.7077	0.4201
B0 to CO ↑	0.0267	0.0244	2.3677	0.6093
B0 to S0 ↓	0.0358	0.0335	1.6742	0.4230
B0 to S0 ↑	0.0324	0.0367	2.3382	0.6011

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	9.185e-05	1.000e-20
X33_P10	3.882e-04	1.000e-20

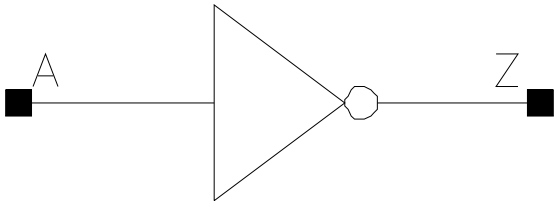
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X33_P10
A0 to CO	4.599e-03	1.585e-02
A0 to S0	4.331e-03	1.583e-02
B0 to CO	4.679e-03	1.624e-02
B0 to S0	4.276e-03	1.545e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X8_P10	X33_P10
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.272	0.3264
X6_P10	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X13_P10	1.200	0.408	0.4896
X17_P10	1.200	0.408	0.4896
X21_P10	1.200	0.544	0.6528
X25_P10	1.200	0.544	0.6528
X29_P10	1.200	0.680	0.8160
X33_P10	1.200	0.680	0.8160
X50_P10	1.200	0.952	1.1424
X58_P10	1.200	1.088	1.3056
X67_P10	1.200	1.224	1.4688
X75_P10	1.200	1.360	1.6320
X84_P10	1.200	1.496	1.7952
X100_P10	1.200	1.768	2.1216
X134_P10	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0007	0.0008	0.0010	0.0016
	X17_P10	X21_P10	X25_P10	X29_P10
A	0.0020	0.0026	0.0030	0.0036
	X33_P10	X50_P10	X58_P10	X67_P10
A	0.0039	0.0060	0.0070	0.0080
	X75_P10	X84_P10	X100_P10	X134_P10

A	0.0092	0.0104	0.0128	0.0176

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0051	0.0049	3.1966	2.4685
A to Z ↑	0.0095	0.0087	4.4686	3.4220
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0045	0.0037	1.7053	1.0979
A to Z ↑	0.0079	0.0074	2.4009	1.5672
	X17_P10	**X21_P10**	**X17_P10**	**X21_P10**
A to Z ↓	0.0038	0.0042	0.8441	0.6780
A to Z ↑	0.0069	0.0074	1.1833	0.9470
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0042	0.0040	0.5773	0.4886
A to Z ↑	0.0070	0.0069	0.7961	0.6775
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0039	0.0042	0.4337	0.2923
A to Z ↑	0.0066	0.0067	0.5967	0.3995
	X58_P10	**X67_P10**	**X58_P10**	**X67_P10**
A to Z ↓	0.0043	0.0044	0.2535	0.2227
A to Z ↑	0.0068	0.0068	0.3445	0.3021
	X75_P10	**X84_P10**	**X75_P10**	**X84_P10**
A to Z ↓	0.0048	0.0050	0.2011	0.1818
A to Z ↑	0.0071	0.0074	0.2708	0.2451
	X100_P10	**X134_P10**	**X100_P10**	**X134_P10**
A to Z ↓	0.0060	0.0068	0.1546	0.1206
A to Z ↑	0.0082	0.0090	0.2067	0.1591

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.229e-05	1.000e-20
X6_P10	1.741e-05	1.000e-20
X8_P10	2.759e-05	1.000e-20
X13_P10	3.945e-05	1.000e-20
X17_P10	5.625e-05	1.000e-20
X21_P10	6.625e-05	1.000e-20
X25_P10	8.190e-05	1.000e-20
X29_P10	9.293e-05	1.000e-20
X33_P10	1.072e-04	1.000e-20
X50_P10	1.579e-04	1.000e-20
X58_P10	1.832e-04	1.000e-20
X67_P10	2.085e-04	1.000e-20
X75_P10	2.339e-04	1.000e-20
X84_P10	2.592e-04	1.000e-20
X100_P10	3.099e-04	1.000e-20
X134_P10	4.112e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10

A to Z	1.034e-03	1.313e-03	1.806e-03	2.657e-03
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	3.493e-03	4.462e-03	5.270e-03	6.046e-03
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	6.727e-03	1.010e-02	1.183e-02	1.337e-02
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	1.524e-02	1.705e-02	2.122e-02	2.930e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

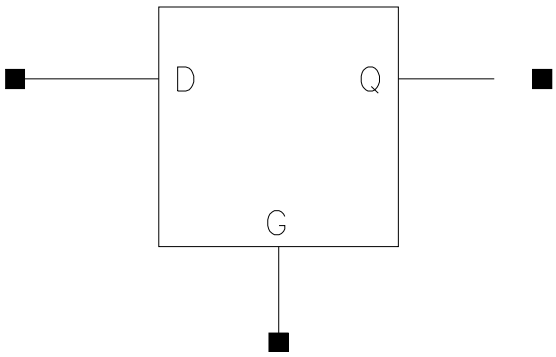
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X23_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P10	X23_P10
D	0.0007	0.0016
G	0.0013	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X23_P10	X8_P10	X23_P10
D to Q ↓	0.0379	0.0306	1.7108	0.8032
D to Q ↑	0.0261	0.0265	2.3318	0.6220
G to Q ↓	0.0402	0.0337	1.7065	0.8023
G to Q ↑	0.0258	0.0232	2.3323	0.6231

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P10	X23_P10
D ↓	hold_falling to G	0.0004	0.0057
D ↑	hold_falling to G	0.0073	0.0041
D ↓	setup_falling to G	0.0360	0.0238
D ↑	setup_falling to G	0.0280	0.0327
G ↑	min_pulse_width to G	0.0362	0.0352

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	6.385e-05	1.000e-20
X23_P10	1.632e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X23_P10
D (output stable)	1.747e-05	7.163e-05
G (output stable)	1.598e-03	3.193e-03
D to Q	7.704e-03	1.557e-02
G to Q	7.358e-03	1.443e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

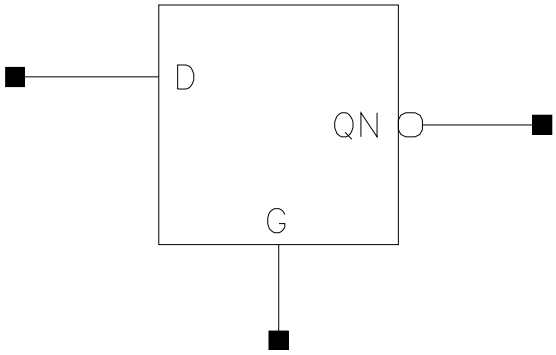
Pin Cycle (vdds)	X8_P10	X23_P10
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P10
D	0.0007
G	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P10	X17_P10
D to QN ↓	0.0346	0.8181
D to QN ↑	0.0428	1.1460
G to QN ↓	0.0336	0.8178
G to QN ↑	0.0438	1.1458

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P10
D ↓	hold_falling to G	-0.0071
D ↑	hold_falling to G	0.0015
D ↓	setup_falling to G	0.0321
D ↑	setup_falling to G	0.0231
G ↑	min_pulse_width to G	0.0283

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P10	1.035e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X17_P10
D (output stable)	1.744e-05
G (output stable)	1.982e-03
D to QN	9.319e-03
G to QN	9.021e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

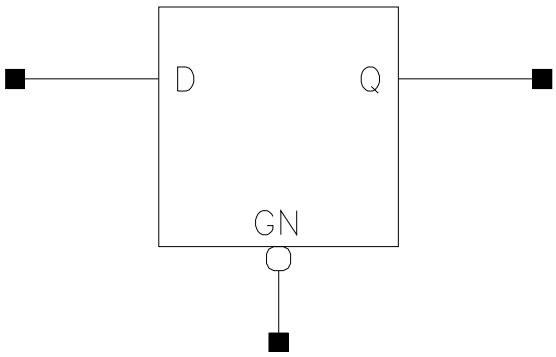
Pin Cycle (vdds)	X17_P10
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
D	0.0006	0.0009	0.0021
GN	0.0013	0.0016	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D to Q ↓	0.0383	0.0336	1.7162	0.8490
D to Q ↑	0.0265	0.0257	2.3327	1.1947
GN to Q ↓	0.0356	0.0304	1.7168	0.8505
GN to Q ↑	0.0386	0.0374	2.3296	1.1941

	X33_P10		X33_P10	
D to Q ↓	0.0327		0.4347	
D to Q ↑	0.0219		0.5998	
GN to Q ↓	0.0284		0.4351	
GN to Q ↑	0.0293		0.5995	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P10	X17_P10	X33_P10
D ↓	hold_rising to GN	-0.0025	0.0002	0.0002
D ↑	hold_rising to GN	0.0079	0.0074	0.0132
D ↓	setup_rising to GN	0.0449	0.0401	0.0352
D ↑	setup_rising to GN	0.0239	0.0239	0.0191
GN ↓	min_pulse_width to GN	0.0475	0.0435	0.0394

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	6.440e-05	1.000e-20
X17_P10	1.066e-04	1.000e-20
X33_P10	1.870e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
D (output stable)	1.730e-05	2.825e-05	7.595e-05
GN (output stable)	1.587e-03	2.139e-03	2.912e-03
D to Q	7.754e-03	1.138e-02	1.853e-02
GN to Q	1.055e-02	1.479e-02	2.233e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

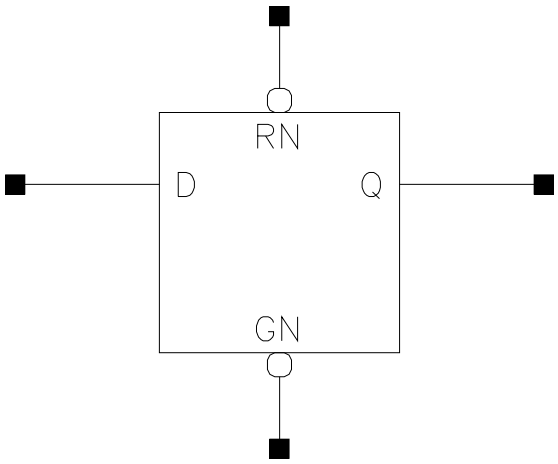
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.496	1.7952
X33_P10	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X33_P10
D	0.0007	0.0017
GN	0.0014	0.0027
RN	0.0007	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
D to Q ↓	0.0357	0.0328	1.6831	0.4363
D to Q ↑	0.0346	0.0462	2.3784	0.6185

GN to Q ↓	0.0333	0.0303	1.6857	0.4369
GN to Q ↑	0.0442	0.0476	2.3807	0.6186
RN to Q ↓	0.0306	0.0535	1.6140	0.4409
RN to Q ↑	0.0356	0.0507	2.3818	0.6186

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P10	X33_P10
D ↓	hold_rising to GN	-0.0030	0.0019
D ↑	hold_rising to GN	0.0010	-0.0147
D ↓	setup_rising to GN	0.0401	0.0328
D ↑	setup_rising to GN	0.0336	0.0507
GN ↓	min_pulse_width to GN	0.0434	0.0497
RN ↓	min_pulse_width to RN	0.0376	0.0664
RN ↑	recovery_rising to GN	0.0373	0.0563
RN ↑	removal_rising to GN	-0.0223	-0.0363

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	7.472e-05	1.000e-20
X33_P10	1.963e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X33_P10
D (output stable)	8.046e-05	1.700e-04
GN (output stable)	1.817e-03	2.954e-03
RN (output stable)	5.213e-05	1.031e-04
D to Q	7.924e-03	2.263e-02
GN to Q	1.095e-02	2.718e-02
RN to Q	5.855e-03	1.844e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

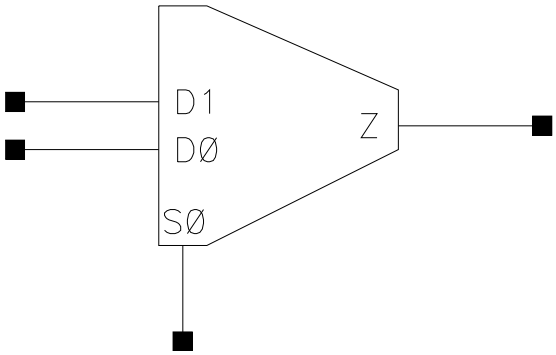
Pin Cycle (vdds)	X8_P10	X33_P10
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
D0	0.0009	0.0013	0.0017	0.0024
D1	0.0009	0.0013	0.0017	0.0023
S0	0.0015	0.0017	0.0020	0.0029

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D0 to Z ↓	0.0298	0.0271	1.7044	0.8346
D0 to Z ↑	0.0245	0.0230	2.3910	1.1708
D1 to Z ↓	0.0283	0.0266	1.7006	0.8337
D1 to Z ↑	0.0225	0.0218	2.3877	1.1692
S0 to Z ↓	0.0259	0.0256	1.6946	0.8313
S0 to Z ↑	0.0248	0.0254	2.3882	1.1691

	X25_P10	X33_P10	X25_P10	X33_P10
D0 to Z ↓	0.0290	0.0262	0.5719	0.4294
D0 to Z ↑	0.0244	0.0228	0.7871	0.5899
D1 to Z ↓	0.0308	0.0270	0.5743	0.4303
D1 to Z ↑	0.0237	0.0221	0.7857	0.5900
S0 to Z ↓	0.0291	0.0268	0.5720	0.4289
S0 to Z ↑	0.0280	0.0258	0.7856	0.5894

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	7.532e-05	1.000e-20
X17_P10	1.457e-04	1.000e-20
X25_P10	1.903e-04	1.000e-20
X33_P10	2.877e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	1.477e-03	2.402e-03	2.842e-03	4.102e-03
D1 (output stable)	1.320e-03	2.328e-03	3.003e-03	4.176e-03
S0 (output stable)	1.814e-03	2.050e-03	2.627e-03	3.385e-03
D0 to Z	5.114e-03	8.862e-03	1.374e-02	1.751e-02
D1 to Z	4.788e-03	8.656e-03	1.387e-02	1.739e-02
S0 to Z	5.854e-03	9.327e-03	1.508e-02	1.871e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

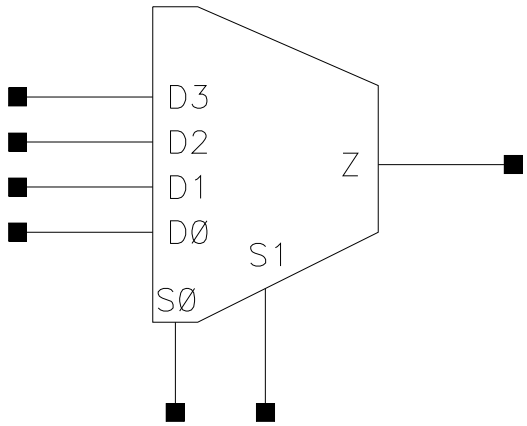
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.312	2.7744
X31_P10	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P10	X31_P10
D0	0.0007	0.0018
D1	0.0007	0.0018
D2	0.0007	0.0018
D3	0.0007	0.0018
S0	0.0022	0.0046
S1	0.0014	0.0027

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X31_P10	X8_P10	X31_P10

D0 to Z ↓	0.0486	0.0507	1.7689	0.4883
D0 to Z ↑	0.0350	0.0383	2.4076	0.6485
D1 to Z ↓	0.0481	0.0507	1.7671	0.4885
D1 to Z ↑	0.0351	0.0382	2.4089	0.6484
D2 to Z ↓	0.0517	0.0478	1.7770	0.4840
D2 to Z ↑	0.0370	0.0352	2.4156	0.6438
D3 to Z ↓	0.0516	0.0473	1.7768	0.4832
D3 to Z ↑	0.0366	0.0367	2.4141	0.6467
S0 to Z ↓	0.0538	0.0564	1.7699	0.4855
S0 to Z ↑	0.0429	0.0469	2.4120	0.6473
S1 to Z ↓	0.0397	0.0406	1.7716	0.4857
S1 to Z ↑	0.0341	0.0369	2.4103	0.6467

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	7.511e-05	1.000e-20
X31_P10	2.407e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X31_P10
D0 (output stable)	2.922e-05	1.588e-04
D1 (output stable)	2.885e-05	1.448e-04
D2 (output stable)	3.300e-05	1.524e-04
D3 (output stable)	3.302e-05	1.513e-04
S0 (output stable)	2.546e-03	5.736e-03
S1 (output stable)	2.229e-03	4.737e-03
D0 to Z	5.828e-03	2.100e-02
D1 to Z	5.807e-03	2.108e-02
D2 to Z	6.181e-03	1.971e-02
D3 to Z	6.161e-03	1.981e-02
S0 to Z	8.654e-03	2.683e-02
S1 to Z	7.135e-03	2.194e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

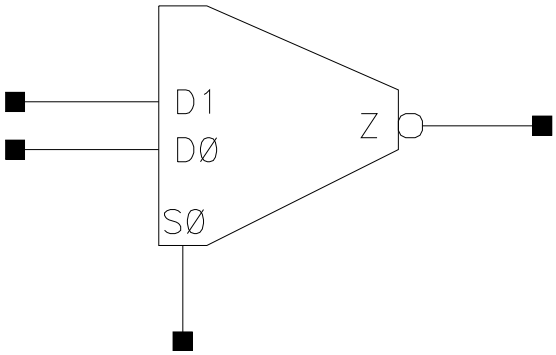
Pin Cycle (vdds)	X8_P10	X31_P10
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.816	0.9792
X5_P10	1.200	0.952	1.1424
X10_P10	1.200	1.768	2.1216
X16_P10	1.200	2.448	2.9376
X21_P10	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P10	X5_P10	X10_P10	X16_P10
D0	0.0006	0.0010	0.0020	0.0031
D1	0.0006	0.0010	0.0020	0.0030
S0	0.0013	0.0023	0.0030	0.0045
	X21_P10			
D0	0.0041			
D1	0.0041			
S0	0.0052			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X5_P10**	**X3_P10**	**X5_P10**
D0 to Z ↓	0.0098	0.0101	5.0393	3.2019

D0 to Z ↑	0.0163	0.0146	8.6515	4.5527
D1 to Z ↓	0.0096	0.0098	5.0109	3.0329
D1 to Z ↑	0.0168	0.0150	8.6615	4.7540
S0 to Z ↓	0.0156	0.0135	5.0125	3.1143
S0 to Z ↑	0.0168	0.0144	8.6390	4.6425
	X10_P10	**X16_P10**	**X10_P10**	**X16_P10**
D0 to Z ↓	0.0114	0.0106	1.5146	0.9888
D0 to Z ↑	0.0157	0.0149	2.1371	1.4117
D1 to Z ↓	0.0104	0.0102	1.4608	0.9622
D1 to Z ↑	0.0157	0.0152	2.1769	1.4289
S0 to Z ↓	0.0166	0.0143	1.4844	0.9743
S0 to Z ↑	0.0172	0.0149	2.1527	1.4186
	X21_P10		**X21_P10**	
D0 to Z ↓	0.0105		0.7561	
D0 to Z ↑	0.0146		1.0712	
D1 to Z ↓	0.0102		0.7307	
D1 to Z ↑	0.0152		1.0668	
S0 to Z ↓	0.0151		0.7424	
S0 to Z ↑	0.0154		1.0665	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	2.689e-05	1.000e-20
X5_P10	6.381e-05	1.000e-20
X10_P10	1.149e-04	1.000e-20
X16_P10	1.846e-04	1.000e-20
X21_P10	2.270e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	1.721e-05	3.862e-05	1.120e-04	1.744e-04
D1 (output stable)	1.705e-05	4.025e-05	9.567e-05	1.673e-04
S0 (output stable)	1.603e-03	2.569e-03	3.919e-03	6.572e-03
D0 to Z	1.469e-03	2.495e-03	5.958e-03	8.520e-03
D1 to Z	1.469e-03	2.466e-03	5.745e-03	8.430e-03
S0 to Z	2.707e-03	4.317e-03	8.196e-03	1.236e-02
	X21_P10			
D0 (output stable)	2.250e-04			
D1 (output stable)	2.243e-04			
S0 (output stable)	7.185e-03			
D0 to Z	1.108e-02			
D1 to Z	1.115e-02			
S0 to Z	1.494e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

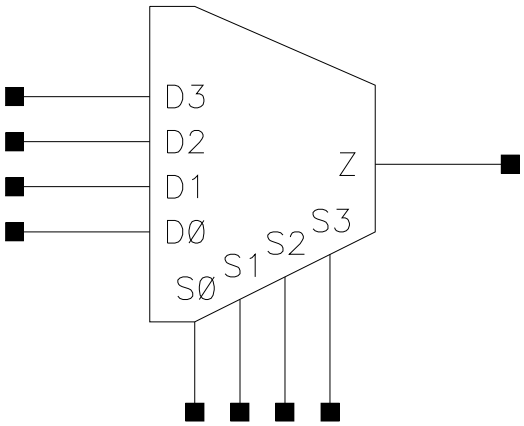
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P10			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	1.768	2.1216
X27_P10	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P10	X27_P10
D0	0.0008	0.0024
D1	0.0008	0.0025
D2	0.0008	0.0024
D3	0.0008	0.0025
S0	0.0008	0.0023
S1	0.0008	0.0023
S2	0.0008	0.0023
S3	0.0008	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	X27_P10	X7_P10	X27_P10
D0 to Z ↓	0.0377	0.0321	2.6528	0.7253
D0 to Z ↑	0.0291	0.0255	2.3484	0.5876
D1 to Z ↓	0.0358	0.0309	2.6494	0.7246
D1 to Z ↑	0.0256	0.0220	2.3403	0.5853
D2 to Z ↓	0.0386	0.0313	2.6582	0.7253
D2 to Z ↑	0.0284	0.0239	2.3580	0.5898
D3 to Z ↓	0.0368	0.0301	2.6532	0.7241
D3 to Z ↑	0.0250	0.0204	2.3489	0.5870
S0 to Z ↓	0.0362	0.0301	2.6517	0.7251
S0 to Z ↑	0.0318	0.0276	2.3484	0.5875
S1 to Z ↓	0.0345	0.0289	2.6486	0.7244
S1 to Z ↑	0.0280	0.0237	2.3399	0.5846
S2 to Z ↓	0.0370	0.0292	2.6567	0.7248
S2 to Z ↑	0.0310	0.0260	2.3568	0.5896
S3 to Z ↓	0.0355	0.0280	2.6523	0.7235
S3 to Z ↑	0.0274	0.0222	2.3493	0.5862

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X7_P10	7.053e-05	1.000e-20
X27_P10	2.998e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X7_P10	X27_P10
D0 (output stable)	7.247e-04	2.355e-03
D1 (output stable)	6.451e-04	2.039e-03
D2 (output stable)	6.664e-04	2.143e-03
D3 (output stable)	5.859e-04	1.833e-03
S0 (output stable)	7.004e-04	2.240e-03
S1 (output stable)	6.202e-04	1.939e-03
S2 (output stable)	6.419e-04	2.032e-03
S3 (output stable)	5.615e-04	1.737e-03
D0 to Z	6.015e-03	1.929e-02
D1 to Z	5.384e-03	1.708e-02
D2 to Z	5.829e-03	1.736e-02
D3 to Z	5.206e-03	1.520e-02
S0 to Z	5.850e-03	1.844e-02
S1 to Z	5.221e-03	1.628e-02
S2 to Z	5.661e-03	1.648e-02
S3 to Z	5.049e-03	1.439e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

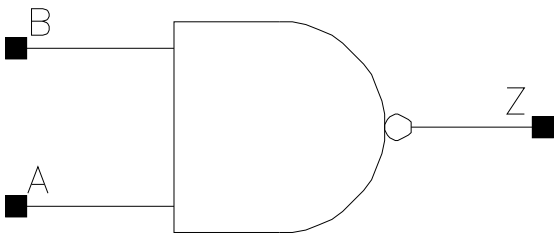
Pin Cycle (vdds)	X7_P10	X27_P10
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P10	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P10	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P10	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P10	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P10	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P10	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P10	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P10	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P10	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P10	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P10	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P10	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P10	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P10	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P10	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P10	C12T28SOI_LL_-NAND2X5_P10	C12T28SOI_LL_-NAND2X7_P10	C12T28SOI_LL_-NAND2X10_P10
A	0.0007	0.0009	0.0010	0.0016
B	0.0007	0.0009	0.0010	0.0015
	C12T28SOI_LL_-NAND2X13_P10	C12T28SOI_LL_-NAND2X17_P10	C12T28SOI_LL_-NAND2X20_P10	C12T28SOI_LL_-NAND2X24_P10
A	0.0020	0.0026	0.0030	0.0036
B	0.0019	0.0025	0.0028	0.0034
	C12T28SOI_LL_-NAND2X27_P10	C12T28SOI_LL_-NAND2X42_P10	C12T28SOI_LL_-NAND2X47_P10	C12T28SOI_LL_-NAND2X50_P10
A	0.0041	0.0012	0.0012	0.0012
B	0.0038	0.0013	0.0013	0.0013
	C12T28SOI_LL_-NAND2X58_P10	C12T28SOI_LL_-NAND2X67_P10	C12T28SOI_-LLBR0D8_-NAND2X7_P10	C12T28SOI_-LLBR0D8_-NAND2X14_P10
A	0.0012	0.0012	0.0010	0.0020
B	0.0013	0.0013	0.0010	0.0019
	C12T28SOI_LLS_-NAND2X40_P10	C12T28SOI_LLS_-NAND2X54_P10		
A	0.0061	0.0081		
B	0.0056	0.0076		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P10	**C12T28SOI_LL_-NAND2X5_P10**	**C12T28SOI_LL_-NAND2X3_P10**	**C12T28SOI_LL_-NAND2X5_P10**
A to Z ↓	0.0072	0.0067	4.9481	3.2484
A to Z ↑	0.0114	0.0104	4.4958	2.9418
B to Z ↓	0.0086	0.0078	5.0180	3.2915
B to Z ↑	0.0099	0.0086	4.5301	2.9689
	C12T28SOI_LL_-NAND2X7_P10	**C12T28SOI_LL_-NAND2X10_P10**	**C12T28SOI_LL_-NAND2X7_P10**	**C12T28SOI_LL_-NAND2X10_P10**
A to Z ↓	0.0068	0.0074	2.7350	1.8012
A to Z ↑	0.0101	0.0108	2.3939	1.5567
B to Z ↓	0.0079	0.0077	2.7670	1.8230
B to Z ↑	0.0082	0.0081	2.4207	1.5714
	C12T28SOI_LL_-NAND2X13_P10	**C12T28SOI_LL_-NAND2X17_P10**	**C12T28SOI_LL_-NAND2X13_P10**	**C12T28SOI_LL_-NAND2X17_P10**
A to Z ↓	0.0072	0.0071	1.3985	1.1059

A to Z ↑	0.0102	0.0103	1.1807	0.9453
B to Z ↓	0.0075	0.0080	1.4149	1.1190
B to Z ↑	0.0074	0.0080	1.1921	0.9535
	C12T28SOI_LL_-NAND2X20_P10	**C12T28SOI_LL_-NAND2X24_P10**	**C12T28SOI_LL_-NAND2X20_P10**	**C12T28SOI_LL_-NAND2X24_P10**
A to Z ↓	0.0071	0.0072	0.9544	0.8084
A to Z ↑	0.0100	0.0102	0.7947	0.6757
B to Z ↓	0.0081	0.0078	0.9657	0.8177
B to Z ↑	0.0077	0.0076	0.8028	0.6819
	C12T28SOI_LL_-NAND2X27_P10	**C12T28SOI_LL_-NAND2X42_P10**	**C12T28SOI_LL_-NAND2X27_P10**	**C12T28SOI_LL_-NAND2X42_P10**
A to Z ↓	0.0071	0.0296	0.7244	0.3415
A to Z ↑	0.0099	0.0303	0.5962	0.4666
B to Z ↓	0.0077	0.0313	0.7328	0.3418
B to Z ↑	0.0073	0.0289	0.6019	0.4659
	C12T28SOI_LL_-NAND2X47_P10	**C12T28SOI_LL_-NAND2X50_P10**	**C12T28SOI_LL_-NAND2X47_P10**	**C12T28SOI_LL_-NAND2X50_P10**
A to Z ↓	0.0306	0.0310	0.3031	0.2847
A to Z ↑	0.0309	0.0313	0.4053	0.3890
B to Z ↓	0.0323	0.0327	0.3033	0.2850
B to Z ↑	0.0295	0.0299	0.4052	0.3891
	C12T28SOI_LL_-NAND2X58_P10	**C12T28SOI_LL_-NAND2X67_P10**	**C12T28SOI_LL_-NAND2X58_P10**	**C12T28SOI_LL_-NAND2X67_P10**
A to Z ↓	0.0325	0.0340	0.2467	0.2169
A to Z ↑	0.0324	0.0336	0.3350	0.2945
B to Z ↓	0.0341	0.0357	0.2468	0.2168
B to Z ↑	0.0310	0.0322	0.3350	0.2946
	C12T28SOI_-LLBR0D8_-NAND2X7_P10	**C12T28SOI_-LLBR0D8_-NAND2X14_P10**	**C12T28SOI_-LLBR0D8_-NAND2X7_P10**	**C12T28SOI_-LLBR0D8_-NAND2X14_P10**
A to Z ↓	0.0045	0.0052	2.0879	1.0991
A to Z ↑	0.0132	0.0133	3.1233	1.5295
B to Z ↓	0.0050	0.0048	2.1250	1.1200
B to Z ↑	0.0107	0.0096	3.2317	1.5613
	C12T28SOI_LLS_-NAND2X40_P10	**C12T28SOI_LLS_-NAND2X54_P10**	**C12T28SOI_LLS_-NAND2X40_P10**	**C12T28SOI_LLS_-NAND2X54_P10**
A to Z ↓	0.0071	0.0071	0.4907	0.3714
A to Z ↑	0.0098	0.0098	0.3997	0.3013
B to Z ↓	0.0078	0.0079	0.4965	0.3758
B to Z ↑	0.0071	0.0073	0.4037	0.3046

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P10	1.261e-05	1.000e-20
C12T28SOI_LL_NAND2X5_P10	2.249e-05	1.000e-20
C12T28SOI_LL_NAND2X7_P10	2.861e-05	1.000e-20
C12T28SOI_LL_NAND2X10_P10	3.967e-05	1.000e-20
C12T28SOI_LL_NAND2X13_P10	5.664e-05	1.000e-20
C12T28SOI_LL_NAND2X17_P10	6.713e-05	1.000e-20
C12T28SOI_LL_NAND2X20_P10	8.297e-05	1.000e-20
C12T28SOI_LL_NAND2X24_P10	9.464e-05	1.000e-20
C12T28SOI_LL_NAND2X27_P10	1.093e-04	1.000e-20

C12T28SOI_LL_NAND2X42_P10	1.926e-04	1.000e-20
C12T28SOI_LL_NAND2X47_P10	2.078e-04	1.000e-20
C12T28SOI_LL_NAND2X50_P10	2.114e-04	1.000e-20
C12T28SOI_LL_NAND2X58_P10	2.302e-04	1.000e-20
C12T28SOI_LL_NAND2X67_P10	2.491e-04	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_-P10	2.530e-05	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_-P10	4.921e-05	1.000e-20
C12T28SOI_LLS_NAND2X40_P10	1.621e-04	1.000e-20
C12T28SOI_LLS_NAND2X54_P10	2.148e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND2X3_P10	C12T28SOI_LL_-NAND2X5_P10	C12T28SOI_LL_-NAND2X7_P10	C12T28SOI_LL_-NAND2X10_P10
A (output stable)	1.312e-05	2.015e-05	2.403e-05	8.124e-05
B (output stable)	2.800e-05	4.297e-05	5.241e-05	2.729e-04
A to Z	1.230e-03	1.764e-03	2.127e-03	3.437e-03
B to Z	1.066e-03	1.514e-03	1.821e-03	2.757e-03
	C12T28SOI_LL_-NAND2X13_P10	C12T28SOI_LL_-NAND2X17_P10	C12T28SOI_LL_-NAND2X20_P10	C12T28SOI_LL_-NAND2X24_P10
A (output stable)	9.712e-05	1.138e-04	1.268e-04	1.745e-04
B (output stable)	3.166e-04	3.043e-04	3.374e-04	5.176e-04
A to Z	4.335e-03	5.470e-03	6.373e-03	7.597e-03
B to Z	3.488e-03	4.516e-03	5.278e-03	6.152e-03
	C12T28SOI_LL_-NAND2X27_P10	C12T28SOI_LL_-NAND2X42_P10	C12T28SOI_LL_-NAND2X47_P10	C12T28SOI_LL_-NAND2X50_P10
A (output stable)	1.884e-04	2.694e-05	2.754e-05	2.664e-05
B (output stable)	5.542e-04	5.561e-05	5.611e-05	5.581e-05
A to Z	8.427e-03	1.773e-02	1.947e-02	2.030e-02
B to Z	6.848e-03	1.743e-02	1.917e-02	2.000e-02
	C12T28SOI_LL_-NAND2X58_P10	C12T28SOI_LL_-NAND2X67_P10	C12T28SOI_-LLBR0D8_-NAND2X7_P10	C12T28SOI_-LLBR0D8_-NAND2X14_P10
A (output stable)	2.754e-05	2.706e-05	3.111e-05	1.186e-04
B (output stable)	5.611e-05	5.647e-05	6.855e-05	3.918e-04
A to Z	2.331e-02	2.651e-02	2.129e-03	4.385e-03
B to Z	2.302e-02	2.621e-02	1.717e-03	3.278e-03
	C12T28SOI_LLS_-NAND2X40_P10	C12T28SOI_LLS_-NAND2X54_P10		
A (output stable)	2.690e-04	3.513e-04		
B (output stable)	7.610e-04	9.731e-04		
A to Z	1.246e-02	1.648e-02		
B to Z	1.015e-02	1.350e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND2X3_P10	C12T28SOI_LL_-NAND2X5_P10	C12T28SOI_LL_-NAND2X7_P10	C12T28SOI_LL_-NAND2X10_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

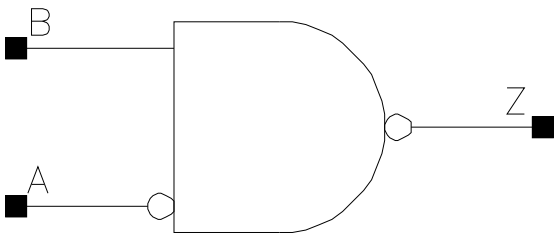
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X13_P10	C12T28SOI_LL_-NAND2X17_P10	C12T28SOI_LL_-NAND2X20_P10	C12T28SOI_LL_-NAND2X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P10	C12T28SOI_LL_-NAND2X42_P10	C12T28SOI_LL_-NAND2X47_P10	C12T28SOI_LL_-NAND2X50_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P10	C12T28SOI_LL_-NAND2X67_P10	C12T28SOI_-LLBR0D8_-NAND2X7_P10	C12T28SOI_-LLBR0D8_-NAND2X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P10	C12T28SOI_LLS_-NAND2X54_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X7_P10	1.200	0.544	0.6528
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X40_P10	1.200	2.312	2.7744
X54_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P10	X7_P10	X13_P10	X27_P10
A	0.0009	0.0009	0.0013	0.0024
B	0.0007	0.0010	0.0019	0.0038
	X40_P10	X54_P10		
A	0.0036	0.0046		
B	0.0056	0.0075		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0207	0.0224	4.8941	2.7118
A to Z ↑	0.0166	0.0177	4.3300	2.3484
B to Z ↓	0.0088	0.0079	5.0550	2.7830
B to Z ↑	0.0100	0.0082	4.5320	2.4414
	X13_P10	**X27_P10**	**X13_P10**	**X27_P10**

A to Z ↓	0.0209	0.0205	1.4644	0.7252
A to Z ↑	0.0173	0.0170	1.2085	0.5856
B to Z ↓	0.0076	0.0076	1.5041	0.7451
B to Z ↑	0.0074	0.0071	1.2196	0.6028
	X40_P10	**X54_P10**	**X40_P10**	**X54_P10**
A to Z ↓	0.0207	0.0206	0.4833	0.3664
A to Z ↑	0.0173	0.0172	0.3901	0.2945
B to Z ↓	0.0077	0.0078	0.4964	0.3763
B to Z ↑	0.0072	0.0072	0.4050	0.3058

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	2.377e-05	1.000e-20
X7_P10	3.974e-05	1.000e-20
X13_P10	8.437e-05	1.000e-20
X27_P10	1.648e-04	1.000e-20
X40_P10	2.429e-04	1.000e-20
X54_P10	3.210e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	1.736e-03	2.124e-03	3.629e-03	7.176e-03
B (output stable)	2.871e-05	5.246e-05	2.880e-04	4.951e-04
A to Z	2.766e-03	3.837e-03	7.083e-03	1.405e-02
B to Z	1.070e-03	1.801e-03	3.433e-03	6.839e-03
	X40_P10	X54_P10		
A (output stable)	1.086e-02	1.420e-02		
B (output stable)	7.154e-04	9.168e-04		
A to Z	2.114e-02	2.779e-02		
B to Z	1.016e-02	1.346e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

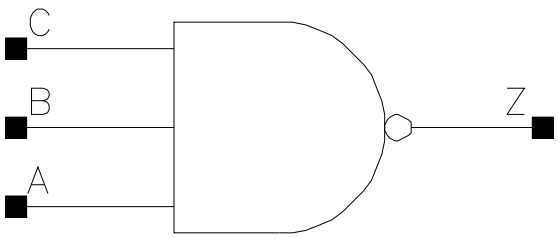
Pin Cycle (vdds)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P10	X54_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P10	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P10	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P10	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P10	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P10	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P10	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P10	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P10	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P10	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P10	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P10	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P10	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P10	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P10	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P10	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A	0.0008	0.0010	0.0017	0.0020
B	0.0008	0.0011	0.0016	0.0019
C	0.0008	0.0010	0.0015	0.0019
	C12T28SOI_LL_-NAND3X15_P10	C12T28SOI_LL_-NAND3X18_P10	C12T28SOI_LL_-NAND3X21_P10	C12T28SOI_LL_-NAND3X24_P10
A	0.0026	0.0030	0.0036	0.0040
B	0.0025	0.0029	0.0035	0.0039
C	0.0024	0.0027	0.0033	0.0037
	C12T28SOI_LL_-NAND3X35_P10	C12T28SOI_LL_-NAND3X47_P10	C12T28SOI_-LLBR0P6_-NAND3X6_P10	C12T28SOI_-LLBR0P6_-NAND3X12_P10
A	0.0061	0.0081	0.0010	0.0020
B	0.0058	0.0077	0.0011	0.0019
C	0.0056	0.0075	0.0010	0.0018
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	C12T28SOI_-LLBR0P6_-NAND3X24_P10	C12T28SOI_-LLBR0P6_-NAND3X35_P10	C12T28SOI_-LLBR0P6_-NAND3X47_P10
A	0.0030	0.0040	0.0061	0.0080
B	0.0028	0.0038	0.0057	0.0077
C	0.0026	0.0036	0.0054	0.0072
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10			
A	0.0031			
B	0.0029			
C	0.0028			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10
A to Z ↓	0.0119	0.0110	5.1274	3.7217
A to Z ↑	0.0145	0.0131	3.3345	2.3324
B to Z ↓	0.0132	0.0120	5.1512	3.7384
B to Z ↑	0.0136	0.0121	3.3453	2.3392
C to Z ↓	0.0128	0.0118	5.1733	3.7544
C to Z ↑	0.0114	0.0099	3.3474	2.3576

	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A to Z ↓	0.0119	0.0114	2.5046	1.9694
A to Z ↑	0.0137	0.0128	1.5693	1.1950
B to Z ↓	0.0119	0.0115	2.5149	1.9767
B to Z ↑	0.0122	0.0114	1.5730	1.1983
C to Z ↓	0.0117	0.0114	2.5256	1.9855
C to Z ↑	0.0099	0.0090	1.5695	1.1909
	C12T28SOI_LL_-NAND3X15_P10	**C12T28SOI_LL_-NAND3X18_P10**	**C12T28SOI_LL_-NAND3X15_P10**	**C12T28SOI_LL_-NAND3X18_P10**
A to Z ↓	0.0107	0.0104	1.5712	1.3547
A to Z ↑	0.0125	0.0119	0.9471	0.7950
B to Z ↓	0.0114	0.0111	1.5787	1.3607
B to Z ↑	0.0111	0.0105	0.9500	0.7978
C to Z ↓	0.0114	0.0110	1.5862	1.3665
C to Z ↑	0.0089	0.0083	0.9581	0.8044
	C12T28SOI_LL_-NAND3X21_P10	**C12T28SOI_LL_-NAND3X24_P10**	**C12T28SOI_LL_-NAND3X21_P10**	**C12T28SOI_LL_-NAND3X24_P10**
A to Z ↓	0.0111	0.0110	1.1422	1.0273
A to Z ↑	0.0126	0.0123	0.6810	0.6015
B to Z ↓	0.0115	0.0114	1.1467	1.0314
B to Z ↑	0.0112	0.0109	0.6827	0.6029
C to Z ↓	0.0115	0.0114	1.1517	1.0359
C to Z ↑	0.0089	0.0086	0.6845	0.6040
	C12T28SOI_LL_-NAND3X35_P10	**C12T28SOI_LL_-NAND3X47_P10**	**C12T28SOI_LL_-NAND3X35_P10**	**C12T28SOI_LL_-NAND3X47_P10**
A to Z ↓	0.0103	0.0106	0.6997	0.5326
A to Z ↑	0.0119	0.0121	0.4032	0.3050
B to Z ↓	0.0110	0.0112	0.7029	0.5351
B to Z ↑	0.0104	0.0105	0.4037	0.3042
C to Z ↓	0.0111	0.0112	0.7062	0.5376
C to Z ↑	0.0081	0.0080	0.4063	0.3061
	C12T28SOI_-LLBR0P6_-NAND3X6_P10	**C12T28SOI_-LLBR0P6_-NAND3X12_P10**	**C12T28SOI_-LLBR0P6_-NAND3X6_P10**	**C12T28SOI_-LLBR0P6_-NAND3X12_P10**
A to Z ↓	0.0076	0.0082	2.5515	1.3524
A to Z ↑	0.0197	0.0196	3.5623	1.8214
B to Z ↓	0.0080	0.0074	2.5762	1.3664
B to Z ↑	0.0176	0.0167	3.5744	1.8259
C to Z ↓	0.0068	0.0062	2.6074	1.3833
C to Z ↑	0.0135	0.0124	3.5968	1.8325
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	**C12T28SOI_-LLBR0P6_-NAND3X24_P10**	**C12T28SOI_-LLBR0P6_-NAND3X18_P10**	**C12T28SOI_-LLBR0P6_-NAND3X24_P10**
A to Z ↓	0.0073	0.0078	0.9329	0.7081
A to Z ↑	0.0185	0.0188	1.2121	0.9160
B to Z ↓	0.0071	0.0072	0.9426	0.7155
B to Z ↑	0.0156	0.0160	1.2164	0.9182
C to Z ↓	0.0062	0.0062	0.9531	0.7240
C to Z ↑	0.0118	0.0118	1.2256	0.9188
	C12T28SOI_-LLBR0P6_-NAND3X35_P10	**C12T28SOI_-LLBR0P6_-NAND3X47_P10**	**C12T28SOI_-LLBR0P6_-NAND3X35_P10**	**C12T28SOI_-LLBR0P6_-NAND3X47_P10**

A to Z ↓	0.0073	0.0075	0.4845	0.3703
A to Z ↑	0.0188	0.0188	0.6302	0.4769
B to Z ↓	0.0070	0.0071	0.4901	0.3745
B to Z ↑	0.0158	0.0158	0.6312	0.4772
C to Z ↓	0.0060	0.0064	0.4960	0.3786
C to Z ↑	0.0115	0.0118	0.6372	0.4791
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P10**	
A to Z ↓	0.0084		0.9239	
A to Z ↑	0.0189		1.1689	
B to Z ↓	0.0075		0.9321	
B to Z ↑	0.0160		1.1727	
C to Z ↓	0.0063		0.9430	
C to Z ↑	0.0117		1.1651	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P10	1.553e-05	1.000e-20
C12T28SOI_LL_NAND3X6_P10	2.447e-05	1.000e-20
C12T28SOI_LL_NAND3X9_P10	3.254e-05	1.000e-20
C12T28SOI_LL_NAND3X12_P10	4.604e-05	1.000e-20
C12T28SOI_LL_NAND3X15_P10	5.335e-05	1.000e-20
C12T28SOI_LL_NAND3X18_P10	6.567e-05	1.000e-20
C12T28SOI_LL_NAND3X21_P10	7.658e-05	1.000e-20
C12T28SOI_LL_NAND3X24_P10	8.823e-05	1.000e-20
C12T28SOI_LL_NAND3X35_P10	1.304e-04	1.000e-20
C12T28SOI_LL_NAND3X47_P10	1.726e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_-P10	2.143e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P10	3.927e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P10	5.422e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P10	7.349e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P10	1.077e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P10	1.418e-04	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P10	6.726e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A (output stable)	2.891e-05	3.868e-05	9.313e-05	1.096e-04
B (output stable)	5.337e-05	6.608e-05	1.638e-04	1.902e-04
C (output stable)	2.589e-04	3.046e-04	4.983e-04	5.689e-04
A to Z	2.302e-03	2.961e-03	4.633e-03	5.667e-03
B to Z	2.068e-03	2.627e-03	3.900e-03	4.817e-03
C to Z	1.736e-03	2.227e-03	3.262e-03	4.042e-03

	C12T28SOI_LL_-NAND3X15_P10	C12T28SOI_LL_-NAND3X18_P10	C12T28SOI_LL_-NAND3X21_P10	C12T28SOI_LL_-NAND3X24_P10
A (output stable)	1.189e-04	1.344e-04	1.855e-04	2.037e-04
B (output stable)	2.131e-04	2.436e-04	3.276e-04	3.586e-04
C (output stable)	5.825e-04	6.669e-04	9.416e-04	1.022e-03
A to Z	6.876e-03	7.805e-03	9.722e-03	1.075e-02
B to Z	5.819e-03	6.577e-03	8.248e-03	9.125e-03
C to Z	4.937e-03	5.562e-03	6.927e-03	7.667e-03
	C12T28SOI_LL_-NAND3X35_P10	C12T28SOI_LL_-NAND3X47_P10	C12T28SOI_-LLBR0P6_-NAND3X6_P10	C12T28SOI_-LLBR0P6_-NAND3X12_P10
A (output stable)	2.664e-04	3.503e-04	5.452e-05	1.538e-04
B (output stable)	4.760e-04	6.210e-04	9.219e-05	2.708e-04
C (output stable)	1.424e-03	1.833e-03	3.989e-04	7.966e-04
A to Z	1.549e-02	2.046e-02	3.124e-03	6.090e-03
B to Z	1.307e-02	1.731e-02	2.620e-03	4.781e-03
C to Z	1.077e-02	1.440e-02	1.988e-03	3.523e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	C12T28SOI_-LLBR0P6_-NAND3X24_P10	C12T28SOI_-LLBR0P6_-NAND3X35_P10	C12T28SOI_-LLBR0P6_-NAND3X47_P10
A (output stable)	1.870e-04	2.833e-04	3.792e-04	4.973e-04
B (output stable)	3.290e-04	5.085e-04	6.792e-04	8.972e-04
C (output stable)	8.893e-04	1.444e-03	2.064e-03	2.594e-03
A to Z	8.378e-03	1.151e-02	1.660e-02	2.183e-02
B to Z	6.557e-03	9.012e-03	1.299e-02	1.711e-02
C to Z	4.986e-03	6.682e-03	9.405e-03	1.257e-02
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10			
A (output stable)	2.262e-04			
B (output stable)	3.995e-04			
C (output stable)	1.131e-03			
A to Z	9.137e-03			
B to Z	7.195e-03			
C to Z	5.333e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P10	C12T28SOI_LL_-NAND3X18_P10	C12T28SOI_LL_-NAND3X21_P10	C12T28SOI_LL_-NAND3X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

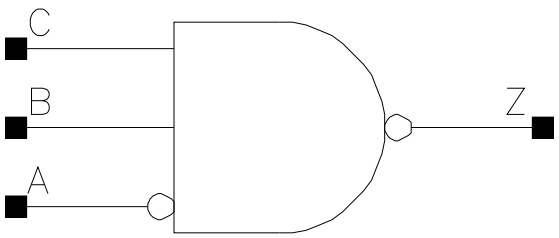
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P10	C12T28SOI_LL_-NAND3X47_P10	C12T28SOI_-LLBR0P6_-NAND3X6_P10	C12T28SOI_-LLBR0P6_-NAND3X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	C12T28SOI_-LLBR0P6_-NAND3X24_P10	C12T28SOI_-LLBR0P6_-NAND3X35_P10	C12T28SOI_-LLBR0P6_-NAND3X47_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.816	0.9792
X12_P10	1.200	1.224	1.4688
X18_P10	1.200	1.496	1.7952
X24_P10	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0009	0.0013	0.0013	0.0024
B	0.0010	0.0019	0.0029	0.0039
C	0.0010	0.0019	0.0027	0.0037

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X12_P10**	**X6_P10**	**X12_P10**
A to Z ↓	0.0253	0.0245	3.6978	1.9803
A to Z ↑	0.0190	0.0191	2.2806	1.1473
B to Z ↓	0.0107	0.0109	3.7316	1.9992
B to Z ↑	0.0108	0.0107	2.3485	1.1844
C to Z ↓	0.0114	0.0107	3.7541	2.0079
C to Z ↑	0.0091	0.0082	2.3650	1.1951
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0282	0.0239	1.3527	1.0273

A to Z ↑	0.0221	0.0181	0.7723	0.5795
B to Z ↓	0.0111	0.0109	1.3638	1.0365
B to Z ↑	0.0105	0.0104	0.7984	0.6002
C to Z ↓	0.0112	0.0108	1.3693	1.0411
C to Z ↑	0.0085	0.0079	0.8048	0.6054

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P10	3.476e-05	1.000e-20
X12_P10	7.390e-05	1.000e-20
X18_P10	9.312e-05	1.000e-20
X24_P10	1.446e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	2.085e-03	3.830e-03	4.928e-03	7.287e-03
B (output stable)	4.803e-05	1.588e-04	2.634e-04	3.647e-04
C (output stable)	1.256e-04	5.625e-04	6.791e-04	1.048e-03
A to Z	4.453e-03	8.781e-03	1.238e-02	1.697e-02
B to Z	2.330e-03	4.529e-03	6.618e-03	8.704e-03
C to Z	2.041e-03	3.716e-03	5.611e-03	7.192e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

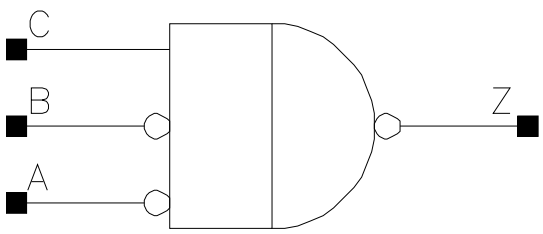
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	0.816	0.9792
X13_P10	1.200	1.088	1.3056
X20_P10	1.200	1.632	1.9584
X27_P10	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P10	X13_P10	X20_P10	X27_P10
A	0.0012	0.0012	0.0023	0.0022
B	0.0013	0.0013	0.0024	0.0023
C	0.0010	0.0019	0.0028	0.0038

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	**X13_P10**	**X7_P10**	**X13_P10**
A to Z ↓	0.0224	0.0274	2.6130	1.3869
A to Z ↑	0.0167	0.0194	2.2640	1.1408
B to Z ↓	0.0237	0.0290	2.6130	1.3873
B to Z ↑	0.0152	0.0182	2.2597	1.1392
C to Z ↓	0.0078	0.0073	2.6768	1.4167
C to Z ↑	0.0082	0.0072	2.3520	1.1913
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0249	0.0274	0.9442	0.7193
A to Z ↑	0.0180	0.0220	0.7697	0.5780
B to Z ↓	0.0251	0.0280	0.9441	0.7188

B to Z ↑	0.0160	0.0204	0.7675	0.5770
C to Z ↓	0.0083	0.0080	0.9659	0.7347
C to Z ↑	0.0079	0.0076	0.8025	0.6026

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X7_P10	5.153e-05	1.000e-20
X13_P10	6.908e-05	1.000e-20
X20_P10	1.143e-04	1.000e-20
X27_P10	1.282e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	1.163e-03	1.498e-03	2.554e-03	2.929e-03
B (output stable)	1.063e-03	1.399e-03	2.364e-03	2.759e-03
C (output stable)	5.611e-05	3.326e-04	3.292e-04	3.738e-04
A to Z	5.182e-03	8.354e-03	1.307e-02	1.640e-02
B to Z	4.782e-03	7.980e-03	1.186e-02	1.530e-02
C to Z	1.887e-03	3.438e-03	5.412e-03	7.139e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

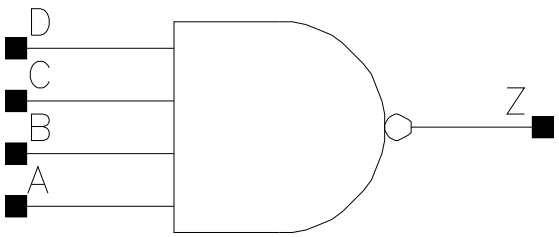
Pin Cycle (vdds)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0008	0.0007	0.0009	0.0012
B	0.0008	0.0008	0.0010	0.0013
C	0.0008	0.0008	0.0010	0.0012
D	0.0008	0.0008	0.0010	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0359	0.0363	1.6562	0.8296
A to Z ↑	0.0307	0.0338	2.3181	1.1497
B to Z ↓	0.0376	0.0386	1.6573	0.8294
B to Z ↑	0.0293	0.0329	2.3151	1.1495
C to Z ↓	0.0365	0.0365	1.6564	0.8291
C to Z ↑	0.0313	0.0348	2.3147	1.1471

D to Z ↓	0.0385	0.0384	1.6561	0.8292
D to Z ↑	0.0302	0.0333	2.3152	1.1466
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0387	0.0362	0.5706	0.4272
A to Z ↑	0.0327	0.0326	0.7747	0.5815
B to Z ↓	0.0406	0.0379	0.5706	0.4269
B to Z ↑	0.0315	0.0312	0.7746	0.5818
C to Z ↓	0.0363	0.0340	0.5702	0.4268
C to Z ↑	0.0327	0.0323	0.7731	0.5796
D to Z ↓	0.0382	0.0358	0.5703	0.4268
D to Z ↑	0.0312	0.0309	0.7736	0.5800

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	5.156e-05	1.000e-20
X17_P10	8.149e-05	1.000e-20
X25_P10	1.174e-04	1.000e-20
X33_P10	1.649e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	8.281e-04	1.003e-03	1.463e-03	1.785e-03
B (output stable)	7.666e-04	9.437e-04	1.373e-03	1.673e-03
C (output stable)	8.143e-04	9.479e-04	1.424e-03	1.671e-03
D (output stable)	7.498e-04	8.814e-04	1.326e-03	1.552e-03
A to Z	6.012e-03	9.433e-03	1.440e-02	1.802e-02
B to Z	5.844e-03	9.274e-03	1.415e-02	1.771e-02
C to Z	6.101e-03	9.272e-03	1.355e-02	1.687e-02
D to Z	5.941e-03	9.098e-03	1.329e-02	1.656e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

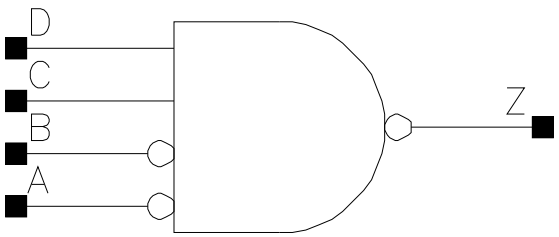
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X12_P10	1.200	1.496	1.7952
X18_P10	1.200	2.040	2.4480
X24_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0012	0.0013	0.0023	0.0021
B	0.0012	0.0017	0.0024	0.0022
C	0.0010	0.0020	0.0028	0.0039
D	0.0010	0.0019	0.0027	0.0038

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X12_P10	X6_P10	X12_P10
A to Z ↓	0.0238	0.0319	3.8081	1.9831
A to Z ↑	0.0177	0.0219	2.2655	1.1429
B to Z ↓	0.0248	0.0331	3.8077	1.9835
B to Z ↑	0.0156	0.0203	2.2641	1.1421
C to Z ↓	0.0108	0.0108	3.8407	1.9989
C to Z ↑	0.0110	0.0106	2.4905	1.1844

D to Z ↓	0.0112	0.0105	3.8615	2.0070
D to Z ↑	0.0092	0.0080	2.5089	1.1950
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0278	0.0308	1.3507	1.0273
A to Z ↑	0.0192	0.0248	0.7701	0.5785
B to Z ↓	0.0281	0.0311	1.3504	1.0273
B to Z ↑	0.0173	0.0229	0.7691	0.5781
C to Z ↓	0.0108	0.0112	1.3607	1.0342
C to Z ↑	0.0103	0.0106	0.8014	0.5986
D to Z ↓	0.0108	0.0111	1.3669	1.0391
D to Z ↑	0.0082	0.0082	0.8189	0.6047

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P10	4.488e-05	1.000e-20
X12_P10	6.097e-05	1.000e-20
X18_P10	1.016e-04	1.000e-20
X24_P10	1.107e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	1.350e-03	2.074e-03	3.278e-03	3.758e-03
B (output stable)	1.217e-03	1.933e-03	2.967e-03	3.464e-03
C (output stable)	5.755e-05	1.753e-04	2.617e-04	3.720e-04
D (output stable)	1.503e-04	6.169e-04	7.272e-04	1.147e-03
A to Z	5.365e-03	9.795e-03	1.462e-02	1.886e-02
B to Z	4.998e-03	9.270e-03	1.348e-02	1.772e-02
C to Z	2.261e-03	4.489e-03	6.461e-03	8.963e-03
D to Z	1.974e-03	3.680e-03	5.489e-03	7.439e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

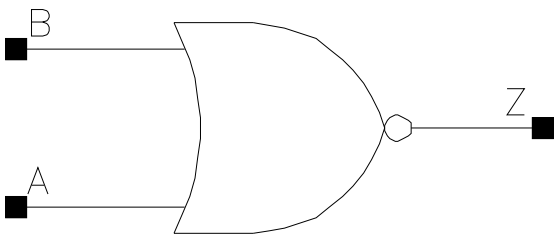
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.408	0.4896
X5_P10	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X10_P10	1.200	0.680	0.8160
X14_P10	1.200	0.680	0.8160
X17_P10	1.200	0.952	1.1424
X21_P10	1.200	0.952	1.1424
X24_P10	1.200	1.224	1.4688
X27_P10	1.200	1.224	1.4688
X34_P10	1.200	1.496	1.7952
X40_P10	1.200	1.360	1.6320
X41_P10	1.200	1.768	2.1216
X49_P10	1.200	1.496	1.7952
X53_P10	1.200	1.904	2.2848
X55_P10	1.200	2.312	2.7744
X57_P10	1.200	1.904	2.2848
X65_P10	1.200	2.040	2.4480
X84_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P10	X5_P10	X7_P10	X10_P10
A	0.0007	0.0008	0.0010	0.0017
B	0.0007	0.0008	0.0010	0.0015
	X14_P10	X17_P10	X21_P10	X24_P10

A	0.0021	0.0026	0.0031	0.0036
B	0.0019	0.0024	0.0029	0.0034
	X27_P10	X34_P10	X40_P10	X41_P10
A	0.0040	0.0051	0.0012	0.0062
B	0.0038	0.0047	0.0013	0.0058
	X49_P10	X53_P10	X55_P10	X57_P10
A	0.0011	0.0012	0.0083	0.0012
B	0.0013	0.0011	0.0076	0.0011
	X65_P10	X84_P10		
A	0.0012	0.0013		
B	0.0011	0.0012		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X5_P10**	**X3_P10**	**X5_P10**
A to Z ↓	0.0068	0.0065	3.2111	2.3394
A to Z ↑	0.0122	0.0113	7.8489	5.7964
B to Z ↓	0.0054	0.0049	3.2894	2.3627
B to Z ↑	0.0132	0.0121	7.8966	5.8263
	X7_P10	**X10_P10**	**X7_P10**	**X10_P10**
A to Z ↓	0.0065	0.0067	1.7294	1.1155
A to Z ↑	0.0105	0.0114	4.1339	2.7548
B to Z ↓	0.0048	0.0042	1.7528	1.1300
B to Z ↑	0.0113	0.0107	4.1569	2.7664
	X14_P10	**X17_P10**	**X14_P10**	**X17_P10**
A to Z ↓	0.0067	0.0067	0.8530	0.6831
A to Z ↑	0.0106	0.0108	2.0590	1.6559
B to Z ↓	0.0042	0.0048	0.8641	0.6904
B to Z ↑	0.0101	0.0110	2.0685	1.6638
	X21_P10	**X24_P10**	**X21_P10**	**X24_P10**
A to Z ↓	0.0067	0.0066	0.5819	0.4945
A to Z ↑	0.0103	0.0105	1.3854	1.2083
B to Z ↓	0.0048	0.0043	0.5880	0.5005
B to Z ↑	0.0107	0.0104	1.3921	1.2142
	X27_P10	**X34_P10**	**X27_P10**	**X34_P10**
A to Z ↓	0.0065	0.0069	0.4400	0.3551
A to Z ↑	0.0101	0.0104	1.0677	0.8493
B to Z ↓	0.0043	0.0047	0.4456	0.3592
B to Z ↑	0.0101	0.0105	1.0731	0.8536
	X40_P10	**X41_P10**	**X40_P10**	**X41_P10**
A to Z ↓	0.0273	0.0067	0.3489	0.2959
A to Z ↑	0.0347	0.0100	0.4758	0.7032
B to Z ↓	0.0259	0.0044	0.3491	0.2996
B to Z ↑	0.0364	0.0101	0.4760	0.7068
	X49_P10	**X53_P10**	**X49_P10**	**X53_P10**
A to Z ↓	0.0284	0.0297	0.2903	0.2656
A to Z ↑	0.0358	0.0405	0.3958	0.3645
B to Z ↓	0.0271	0.0284	0.2901	0.2655
B to Z ↑	0.0375	0.0421	0.3959	0.3643
	X55_P10	**X57_P10**	**X55_P10**	**X57_P10**
A to Z ↓	0.0068	0.0299	0.2236	0.2498
A to Z ↑	0.0101	0.0407	0.5303	0.3404

B to Z ↓	0.0045	0.0287	0.2268	0.2499
B to Z ↑	0.0100	0.0423	0.5331	0.3400
	X65_P10	**X84_P10**	**X65_P10**	**X84_P10**
A to Z ↓	0.0309	0.0322	0.2190	0.1735
A to Z ↑	0.0417	0.0422	0.2977	0.2367
B to Z ↓	0.0296	0.0309	0.2191	0.1735
B to Z ↑	0.0432	0.0438	0.2979	0.2366

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.289e-05	1.000e-20
X5_P10	1.950e-05	1.000e-20
X7_P10	2.982e-05	1.000e-20
X10_P10	4.131e-05	1.000e-20
X14_P10	5.939e-05	1.000e-20
X17_P10	7.021e-05	1.000e-20
X21_P10	8.721e-05	1.000e-20
X24_P10	9.921e-05	1.000e-20
X27_P10	1.151e-04	1.000e-20
X34_P10	1.429e-04	1.000e-20
X40_P10	2.283e-04	1.000e-20
X41_P10	1.708e-04	1.000e-20
X49_P10	2.603e-04	1.000e-20
X53_P10	2.961e-04	1.000e-20
X55_P10	2.265e-04	1.000e-20
X57_P10	3.162e-04	1.000e-20
X65_P10	3.483e-04	1.000e-20
X84_P10	4.135e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	2.229e-05	2.929e-05	4.037e-05	1.213e-04
B (output stable)	4.271e-05	5.622e-05	7.823e-05	3.543e-04
A to Z	1.211e-03	1.551e-03	2.110e-03	3.375e-03
B to Z	1.016e-03	1.286e-03	1.736e-03	2.520e-03
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	1.432e-04	1.686e-04	1.862e-04	2.333e-04
B (output stable)	4.117e-04	4.184e-04	4.238e-04	5.945e-04
A to Z	4.329e-03	5.430e-03	6.342e-03	7.415e-03
B to Z	3.281e-03	4.274e-03	5.013e-03	5.725e-03
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	2.498e-04	3.050e-04	4.150e-05	3.834e-04
B (output stable)	6.159e-04	6.738e-04	7.850e-05	9.087e-04
A to Z	8.195e-03	1.043e-02	1.750e-02	1.235e-02
B to Z	6.354e-03	8.205e-03	1.716e-02	9.536e-03
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	4.168e-05	4.250e-05	5.109e-04	4.250e-05
B (output stable)	7.768e-05	8.268e-05	1.196e-03	8.400e-05
A to Z	2.007e-02	2.436e-02	1.638e-02	2.533e-02
B to Z	1.973e-02	2.399e-02	1.261e-02	2.496e-02
	X65_P10	X84_P10		

A (output stable)	4.300e-05	4.336e-05		
B (output stable)	8.318e-05	8.450e-05		
A to Z	2.799e-02	3.345e-02		
B to Z	2.762e-02	3.302e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

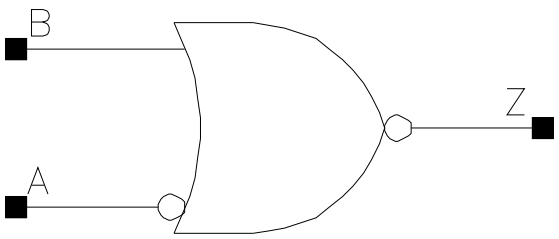
Pin Cycle (vdds)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P10	X84_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X7_P10	1.200	0.680	0.8160
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X41_P10	1.200	2.312	2.7744
X55_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X7_P10	X13_P10
A	0.0009	0.0009	0.0009	0.0013
B	0.0007	0.0010	0.0010	0.0019
	X27_P10	X41_P10	X55_P10	
A	0.0024	0.0036	0.0047	
B	0.0038	0.0057	0.0076	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0196	0.0221	3.0343	2.0094
A to Z ↑	0.0182	0.0186	7.7595	4.1016
B to Z ↓	0.0056	0.0061	3.2624	2.1614
B to Z ↑	0.0133	0.0108	7.8803	4.1711

	X7_P10	X13_P10	X7_P10	X13_P10
A to Z ↓	0.0224	0.0204	1.6078	0.8721
A to Z ↑	0.0204	0.0199	4.0755	2.1755
B to Z ↓	0.0052	0.0045	1.6818	0.9082
B to Z ↑	0.0122	0.0111	4.1228	2.2045
	X27_P10	**X41_P10**	**X27_P10**	**X41_P10**
A to Z ↓	0.0198	0.0202	0.4166	0.2820
A to Z ↑	0.0190	0.0192	1.0394	0.6982
B to Z ↓	0.0044	0.0045	0.4481	0.3018
B to Z ↑	0.0105	0.0104	1.0539	0.7079
	X55_P10		**X55_P10**	
A to Z ↓	0.0198		0.2134	
A to Z ↑	0.0188		0.5273	
B to Z ↓	0.0044		0.2286	
B to Z ↑	0.0101		0.5346	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	2.410e-05	1.000e-20
X6_P10	3.998e-05	1.000e-20
X7_P10	4.421e-05	1.000e-20
X13_P10	8.611e-05	1.000e-20
X27_P10	1.704e-04	1.000e-20
X41_P10	2.515e-04	1.000e-20
X55_P10	3.326e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	1.721e-03	2.076e-03	2.197e-03	3.680e-03
B (output stable)	4.265e-05	7.777e-05	2.019e-04	3.574e-04
A to Z	2.767e-03	3.756e-03	4.303e-03	7.373e-03
B to Z	1.024e-03	1.646e-03	1.936e-03	3.363e-03
	X27_P10	X41_P10	X55_P10	
A (output stable)	7.321e-03	1.103e-02	1.443e-02	
B (output stable)	6.810e-04	9.254e-04	1.196e-03	
A to Z	1.469e-02	2.189e-02	2.857e-02	
B to Z	6.664e-03	9.815e-03	1.280e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

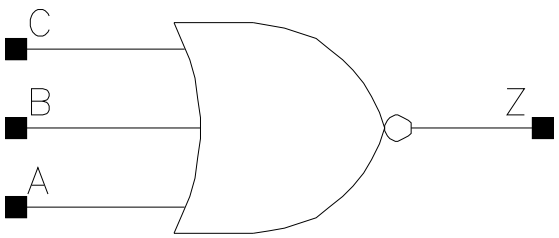
Pin Cycle (vdds)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P10	X41_P10	X55_P10	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X9_P10	1.200	0.952	1.1424
X13_P10	1.200	0.952	1.1424
X16_P10	1.200	1.360	1.6320
X19_P10	1.200	1.496	1.7952
X22_P10	1.200	1.768	2.1216
X25_P10	1.200	1.904	2.2848
X37_P10	1.200	2.584	3.1008
X49_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P10	X6_P10	X9_P10	X13_P10
A	0.0008	0.0010	0.0016	0.0020
B	0.0008	0.0010	0.0017	0.0021
C	0.0008	0.0010	0.0015	0.0018
	X16_P10	X19_P10	X22_P10	X25_P10
A	0.0026	0.0030	0.0036	0.0040
B	0.0026	0.0034	0.0038	0.0046
C	0.0024	0.0028	0.0033	0.0037
	X37_P10	X49_P10		
A	0.0060	0.0082		
B	0.0061	0.0082		

C	0.0054	0.0075		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0081	0.0079	2.3717	1.7547
A to Z ↑	0.0160	0.0146	8.3130	5.9239
B to Z ↓	0.0074	0.0071	2.3786	1.7596
B to Z ↑	0.0160	0.0145	8.3240	5.9326
C to Z ↓	0.0060	0.0056	2.4026	1.7795
C to Z ↑	0.0162	0.0146	8.3403	5.9433
	X9_P10	**X13_P10**	**X9_P10**	**X13_P10**
A to Z ↓	0.0081	0.0081	1.1480	0.8854
A to Z ↑	0.0159	0.0147	3.9308	2.9536
B to Z ↓	0.0073	0.0070	1.1237	0.8530
B to Z ↑	0.0160	0.0145	3.9410	2.9608
C to Z ↓	0.0050	0.0048	1.1358	0.8695
C to Z ↑	0.0138	0.0129	3.9375	2.9590
	X16_P10	**X19_P10**	**X16_P10**	**X19_P10**
A to Z ↓	0.0080	0.0080	0.6878	0.5831
A to Z ↑	0.0152	0.0149	2.3818	1.9787
B to Z ↓	0.0074	0.0073	0.6899	0.5725
B to Z ↑	0.0152	0.0152	2.3864	1.9832
C to Z ↓	0.0053	0.0053	0.6957	0.5946
C to Z ↑	0.0143	0.0136	2.3877	1.9834
	X22_P10	**X25_P10**	**X22_P10**	**X25_P10**
A to Z ↓	0.0080	0.0080	0.5042	0.4436
A to Z ↑	0.0148	0.0148	1.7037	1.4883
B to Z ↓	0.0072	0.0072	0.4970	0.4291
B to Z ↑	0.0147	0.0150	1.7080	1.4922
C to Z ↓	0.0048	0.0049	0.5035	0.4452
C to Z ↑	0.0132	0.0129	1.7078	1.4917
	X37_P10	**X49_P10**	**X37_P10**	**X49_P10**
A to Z ↓	0.0081	0.0082	0.3046	0.2305
A to Z ↑	0.0143	0.0144	0.9987	0.7527
B to Z ↓	0.0072	0.0073	0.3019	0.2286
B to Z ↑	0.0141	0.0141	1.0009	0.7542
C to Z ↓	0.0053	0.0054	0.3058	0.2316
C to Z ↑	0.0130	0.0132	1.0010	0.7547

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.622e-05	1.000e-20
X6_P10	2.511e-05	1.000e-20
X9_P10	3.472e-05	1.000e-20
X13_P10	5.066e-05	1.000e-20
X16_P10	5.935e-05	1.000e-20
X19_P10	7.615e-05	1.000e-20
X22_P10	8.422e-05	1.000e-20
X25_P10	1.006e-04	1.000e-20
X37_P10	1.480e-04	1.000e-20

X49_P10	1.967e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	3.481e-05	4.740e-05	8.711e-05	1.135e-04
B (output stable)	4.124e-05	5.770e-05	1.277e-04	1.552e-04
C (output stable)	1.106e-04	1.557e-04	4.454e-04	5.458e-04
A to Z	1.943e-03	2.547e-03	4.133e-03	5.197e-03
B to Z	1.658e-03	2.157e-03	3.550e-03	4.405e-03
C to Z	1.407e-03	1.801e-03	2.654e-03	3.339e-03
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	1.345e-04	1.633e-04	1.970e-04	2.250e-04
B (output stable)	1.883e-04	2.486e-04	2.786e-04	3.400e-04
C (output stable)	5.652e-04	7.466e-04	8.962e-04	1.073e-03
A to Z	6.628e-03	7.894e-03	9.076e-03	1.042e-02
B to Z	5.616e-03	6.761e-03	7.681e-03	8.897e-03
C to Z	4.485e-03	5.185e-03	5.887e-03	6.638e-03
	X37_P10	X49_P10		
A (output stable)	3.290e-04	4.341e-04		
B (output stable)	4.546e-04	5.969e-04		
C (output stable)	1.428e-03	1.872e-03		
A to Z	1.515e-02	2.023e-02		
B to Z	1.275e-02	1.701e-02		
C to Z	9.828e-03	1.315e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

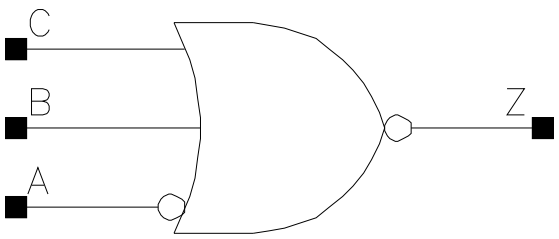
Pin Cycle (vdds)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P10	X49_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.680	0.8160
X13_P10	1.200	1.224	1.4688
X19_P10	1.200	1.496	1.7952
X25_P10	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0009	0.0013	0.0013	0.0024
B	0.0010	0.0021	0.0030	0.0041
C	0.0010	0.0019	0.0027	0.0037

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X13_P10**	**X6_P10**	**X13_P10**
A to Z ↓	0.0223	0.0217	1.6713	0.9223
A to Z ↑	0.0239	0.0239	5.9830	2.9470
B to Z ↓	0.0072	0.0070	1.7653	0.8575
B to Z ↑	0.0147	0.0145	6.0091	2.9612
C to Z ↓	0.0057	0.0047	1.7796	0.8704
C to Z ↑	0.0148	0.0128	6.0202	2.9596
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0247	0.0217	0.5637	0.4279

A to Z ↑	0.0264	0.0241	1.9870	1.4907
B to Z ↓	0.0074	0.0072	0.5936	0.4434
B to Z ↑	0.0144	0.0142	1.9976	1.4982
C to Z ↓	0.0052	0.0049	0.5955	0.4476
C to Z ↑	0.0136	0.0130	1.9985	1.4988

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P10	3.675e-05	1.000e-20
X13_P10	8.018e-05	1.000e-20
X19_P10	1.026e-04	1.000e-20
X25_P10	1.556e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	2.139e-03	3.926e-03	4.893e-03	7.709e-03
B (output stable)	5.901e-05	1.585e-04	2.222e-04	3.076e-04
C (output stable)	1.538e-04	5.550e-04	6.471e-04	9.795e-04
A to Z	4.502e-03	8.954e-03	1.221e-02	1.744e-02
B to Z	2.157e-03	4.403e-03	6.446e-03	8.573e-03
C to Z	1.814e-03	3.317e-03	5.149e-03	6.623e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

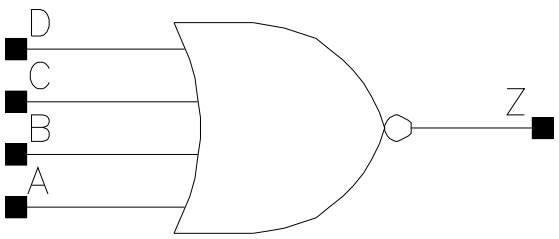
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	1.904	2.2848
X32_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X32_P10
A	0.0008	0.0008	0.0009	0.0011
B	0.0008	0.0008	0.0010	0.0014
C	0.0007	0.0007	0.0010	0.0011
D	0.0008	0.0007	0.0010	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0268	0.0272	1.6385	0.8059
A to Z ↑	0.0368	0.0401	2.3551	1.1647
B to Z ↓	0.0253	0.0261	1.6387	0.8055
B to Z ↑	0.0381	0.0417	2.3529	1.1635
C to Z ↓	0.0261	0.0271	1.6350	0.8049
C to Z ↑	0.0377	0.0415	2.3538	1.1629

D to Z ↓	0.0253	0.0264	1.6349	0.8045
D to Z ↑	0.0393	0.0434	2.3536	1.1640
	X25_P10	**X32_P10**	**X25_P10**	**X32_P10**
A to Z ↓	0.0283	0.0303	0.5585	0.4387
A to Z ↑	0.0399	0.0385	0.7969	0.6022
B to Z ↓	0.0273	0.0292	0.5586	0.4385
B to Z ↑	0.0417	0.0400	0.7972	0.6030
C to Z ↓	0.0274	0.0300	0.5560	0.4369
C to Z ↑	0.0397	0.0392	0.7961	0.6020
D to Z ↓	0.0261	0.0281	0.5564	0.4368
D to Z ↑	0.0414	0.0405	0.7964	0.6026

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	6.773e-05	1.000e-20
X17_P10	1.132e-04	1.000e-20
X25_P10	1.726e-04	1.000e-20
X32_P10	2.282e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	8.166e-04	9.826e-04	1.390e-03	1.741e-03
B (output stable)	7.428e-04	9.080e-04	1.291e-03	1.602e-03
C (output stable)	7.667e-04	8.883e-04	1.345e-03	1.695e-03
D (output stable)	6.906e-04	8.157e-04	1.240e-03	1.553e-03
A to Z	5.635e-03	8.966e-03	1.355e-02	1.707e-02
B to Z	5.432e-03	8.782e-03	1.328e-02	1.674e-02
C to Z	5.652e-03	8.904e-03	1.281e-02	1.632e-02
D to Z	5.437e-03	8.720e-03	1.255e-02	1.594e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

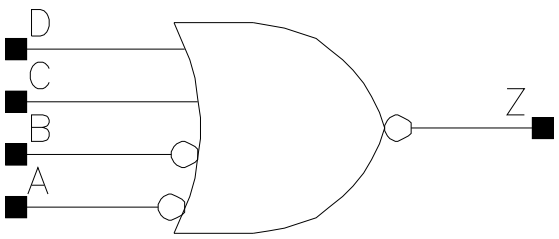
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X13_P10	1.200	1.496	1.7952
X19_P10	1.200	2.040	2.4480
X25_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0012	0.0013	0.0024	0.0023
B	0.0013	0.0017	0.0024	0.0024
C	0.0010	0.0020	0.0029	0.0039
D	0.0010	0.0019	0.0027	0.0037

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X13_P10	X6_P10	X13_P10
A to Z ↓	0.0195	0.0243	1.6255	0.8168
A to Z ↑	0.0235	0.0294	5.7686	3.0031
B to Z ↓	0.0178	0.0231	1.6235	0.8164
B to Z ↑	0.0247	0.0311	5.7697	3.0034
C to Z ↓	0.0077	0.0071	1.7867	0.8587
C to Z ↑	0.0147	0.0148	5.7992	3.0186

D to Z ↓	0.0059	0.0048	1.7936	0.8685
D to Z ↑	0.0146	0.0132	5.8056	3.0168
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0216	0.0236	0.5580	0.4207
A to Z ↑	0.0266	0.0288	1.9883	1.5050
B to Z ↓	0.0193	0.0218	0.5575	0.4201
B to Z ↑	0.0276	0.0301	1.9884	1.5051
C to Z ↓	0.0075	0.0073	0.5936	0.4447
C to Z ↑	0.0144	0.0143	1.9974	1.5114
D to Z ↓	0.0052	0.0050	0.5958	0.4472
D to Z ↑	0.0136	0.0130	1.9980	1.5111

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P10	5.058e-05	1.000e-20
X13_P10	7.278e-05	1.000e-20
X19_P10	1.197e-04	1.000e-20
X25_P10	1.399e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	1.355e-03	2.060e-03	3.272e-03	3.829e-03
B (output stable)	1.242e-03	1.940e-03	3.007e-03	3.601e-03
C (output stable)	6.654e-05	1.919e-04	2.764e-04	3.708e-04
D (output stable)	1.859e-04	5.973e-04	7.563e-04	1.121e-03
A to Z	5.556e-03	9.937e-03	1.510e-02	1.913e-02
B to Z	5.260e-03	9.489e-03	1.417e-02	1.824e-02
C to Z	2.229e-03	4.405e-03	6.421e-03	8.456e-03
D to Z	1.878e-03	3.361e-03	5.154e-03	6.562e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

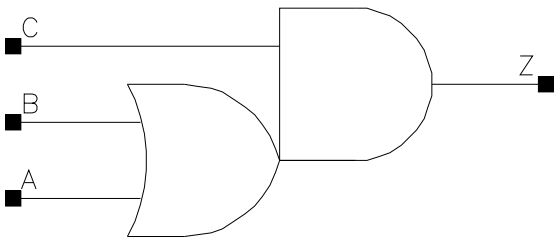
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0011	0.0012	0.0022
B	0.0013	0.0013	0.0025
C	0.0012	0.0013	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0199	0.0236	1.6836	0.8379
A to Z ↑	0.0194	0.0221	2.3679	1.1668
B to Z ↓	0.0210	0.0250	1.6838	0.8386
B to Z ↑	0.0172	0.0202	2.3652	1.1652
C to Z ↓	0.0194	0.0218	1.6669	0.8271
C to Z ↑	0.0174	0.0198	2.3672	1.1663
	X33_P10		**X33_P10**	
A to Z ↓	0.0248		0.4252	
A to Z ↑	0.0241		0.5861	

B to Z ↓	0.0263		0.4248	
B to Z ↑	0.0217		0.5846	
C to Z ↓	0.0225		0.4185	
C to Z ↑	0.0209		0.5851	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	6.422e-05	1.000e-20
X17_P10	9.631e-05	1.000e-20
X33_P10	1.907e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	8.221e-05	8.301e-05	1.737e-04
B (output stable)	9.940e-05	1.009e-04	1.982e-04
C (output stable)	7.359e-05	7.682e-05	1.434e-04
A to Z	4.511e-03	7.169e-03	1.513e-02
B to Z	4.111e-03	6.737e-03	1.428e-02
C to Z	4.884e-03	7.268e-03	1.518e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

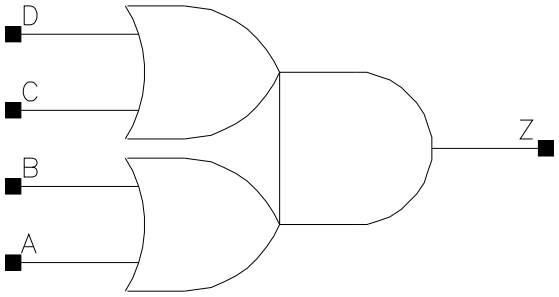
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0012	0.0023
B	0.0008	0.0012	0.0023
C	0.0008	0.0012	0.0023
D	0.0008	0.0012	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0341	0.0296	1.6369	0.8322
A to Z ↑	0.0252	0.0230	2.3245	1.1632
B to Z ↓	0.0360	0.0313	1.6363	0.8322
B to Z ↑	0.0239	0.0215	2.3215	1.1613

C to Z ↓	0.0294	0.0259	1.6237	0.8277
C to Z ↑	0.0252	0.0239	2.3206	1.1621
D to Z ↓	0.0308	0.0273	1.6233	0.8275
D to Z ↑	0.0234	0.0217	2.3179	1.1601
	X33_P10		**X33_P10**	
A to Z ↓	0.0301		0.4273	
A to Z ↑	0.0232		0.5850	
B to Z ↓	0.0308		0.4273	
B to Z ↑	0.0212		0.5838	
C to Z ↓	0.0259		0.4245	
C to Z ↑	0.0236		0.5840	
D to Z ↓	0.0263		0.4246	
D to Z ↑	0.0213		0.5826	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	4.628e-05	1.000e-20
X17_P10	9.901e-05	1.000e-20
X33_P10	1.915e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.562e-05	4.073e-05	1.199e-04
B (output stable)	3.647e-05	6.275e-05	2.996e-04
C (output stable)	7.847e-05	1.020e-04	2.385e-04
D (output stable)	9.025e-05	1.255e-04	4.185e-04
A to Z	5.251e-03	8.926e-03	1.759e-02
B to Z	5.025e-03	8.480e-03	1.642e-02
C to Z	4.627e-03	8.069e-03	1.576e-02
D to Z	4.402e-03	7.622e-03	1.458e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

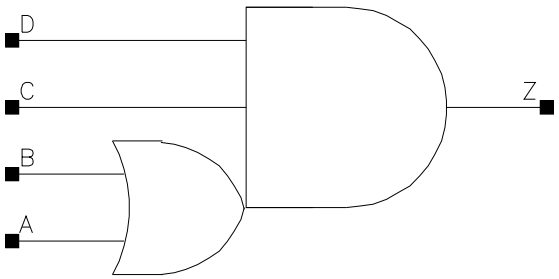
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	1.088	1.3056
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0008	0.0012	0.0019	0.0023
B	0.0008	0.0013	0.0020	0.0024
C	0.0008	0.0012	0.0020	0.0024
D	0.0008	0.0013	0.0020	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0285	0.0269	1.7135	0.8372
A to Z ↑	0.0303	0.0292	2.4042	1.1669
B to Z ↓	0.0301	0.0280	1.7132	0.8366
B to Z ↑	0.0285	0.0267	2.4004	1.1642
C to Z ↓	0.0257	0.0242	1.6809	0.8234

C to Z ↑	0.0268	0.0258	2.4009	1.1639
D to Z ↓	0.0248	0.0232	1.6811	0.8229
D to Z ↑	0.0286	0.0273	2.4002	1.1646
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0283	0.0271	0.5698	0.4261
A to Z ↑	0.0300	0.0307	0.7917	0.5938
B to Z ↓	0.0289	0.0277	0.5695	0.4262
B to Z ↑	0.0273	0.0277	0.7898	0.5914
C to Z ↓	0.0255	0.0244	0.5612	0.4198
C to Z ↑	0.0265	0.0266	0.7907	0.5924
D to Z ↓	0.0241	0.0232	0.5599	0.4191
D to Z ↑	0.0273	0.0277	0.7903	0.5922

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	4.617e-05	1.000e-20
X17_P10	9.969e-05	1.000e-20
X25_P10	1.485e-04	1.000e-20
X33_P10	1.972e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	8.703e-05	1.637e-04	2.784e-04	3.034e-04
B (output stable)	9.056e-05	1.850e-04	3.197e-04	3.468e-04
C (output stable)	2.149e-05	4.362e-05	1.056e-04	1.160e-04
D (output stable)	3.782e-05	7.368e-05	2.281e-04	2.477e-04
A to Z	4.520e-03	8.331e-03	1.331e-02	1.681e-02
B to Z	4.305e-03	7.832e-03	1.236e-02	1.556e-02
C to Z	4.709e-03	8.599e-03	1.399e-02	1.734e-02
D to Z	4.531e-03	8.268e-03	1.318e-02	1.648e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

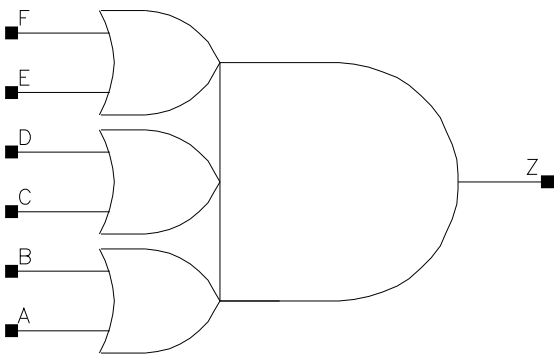
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0008	0.0012	0.0021
B	0.0008	0.0012	0.0023
C	0.0008	0.0012	0.0021
D	0.0008	0.0012	0.0023
E	0.0008	0.0012	0.0021
F	0.0008	0.0012	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0390	0.0339	1.7466	0.8494
A to Z ↑	0.0317	0.0301	2.3890	1.1777
B to Z ↓	0.0408	0.0359	1.7472	0.8494
B to Z ↑	0.0303	0.0288	2.3894	1.1774
C to Z ↓	0.0356	0.0321	1.7364	0.8478
C to Z ↑	0.0326	0.0305	2.3907	1.1777
D to Z ↓	0.0375	0.0338	1.7365	0.8478
D to Z ↑	0.0309	0.0287	2.3877	1.1772
E to Z ↓	0.0309	0.0282	1.7238	0.8431
E to Z ↑	0.0313	0.0299	2.3873	1.1763
F to Z ↓	0.0328	0.0295	1.7240	0.8430
F to Z ↑	0.0295	0.0279	2.3838	1.1744
	X33_P10		X33_P10	
A to Z ↓	0.0344		0.4337	
A to Z ↑	0.0310		0.5940	
B to Z ↓	0.0363		0.4338	
B to Z ↑	0.0286		0.5924	
C to Z ↓	0.0315		0.4313	
C to Z ↑	0.0312		0.5938	
D to Z ↓	0.0333		0.4313	
D to Z ↑	0.0290		0.5922	
E to Z ↓	0.0277		0.4289	
E to Z ↑	0.0307		0.5928	
F to Z ↓	0.0293		0.4288	
F to Z ↑	0.0282		0.5912	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	5.070e-05	1.000e-20
X17_P10	1.110e-04	1.000e-20
X33_P10	2.125e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.377e-05	4.052e-05	7.708e-05
B (output stable)	3.126e-05	5.965e-05	1.076e-04
C (output stable)	4.298e-05	6.844e-05	1.383e-04
D (output stable)	5.245e-05	8.547e-05	1.694e-04
E (output stable)	1.430e-04	2.073e-04	3.927e-04
F (output stable)	1.472e-04	2.191e-04	4.215e-04
A to Z	6.048e-03	1.045e-02	2.069e-02
B to Z	5.808e-03	1.004e-02	1.975e-02
C to Z	5.547e-03	9.767e-03	1.911e-02
D to Z	5.316e-03	9.331e-03	1.819e-02
E to Z	4.941e-03	8.877e-03	1.737e-02
F to Z	4.730e-03	8.435e-03	1.649e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

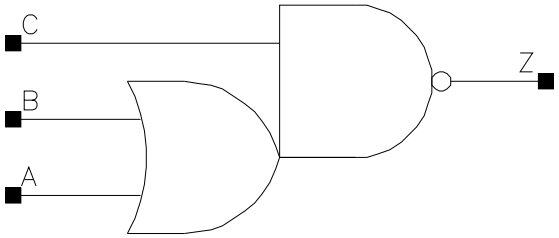
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X34_P10	1.200	2.720	3.2640
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X34_P10	X46_P10
A	0.0009	0.0029	0.0058	0.0077
B	0.0009	0.0027	0.0053	0.0072
C	0.0010	0.0031	0.0063	0.0082

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0105	0.0108	3.0013	0.9793
A to Z ↑	0.0108	0.0112	4.1362	1.4134
B to Z ↓	0.0082	0.0083	2.9469	0.9846
B to Z ↑	0.0114	0.0113	4.1600	1.4221
C to Z ↓	0.0090	0.0089	2.7255	0.8968
C to Z ↑	0.0118	0.0116	2.4058	0.8000
	X34_P10	**X46_P10**	**X34_P10**	**X46_P10**
A to Z ↓	0.0114	0.0114	0.4987	0.3806

A to Z ↑	0.0117	0.0116	0.7052	0.5430
B to Z ↓	0.0088	0.0089	0.5062	0.3878
B to Z ↑	0.0117	0.0117	0.7095	0.5463
C to Z ↓	0.0094	0.0093	0.4590	0.3507
C to Z ↑	0.0119	0.0118	0.4002	0.3060

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P10	3.527e-05	1.000e-20
X17_P10	1.046e-04	1.000e-20
X34_P10	2.077e-04	1.000e-20
X46_P10	2.748e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	7.200e-05	2.489e-04	5.378e-04	6.494e-04
B (output stable)	8.894e-05	3.239e-04	7.476e-04	8.729e-04
C (output stable)	6.606e-05	2.197e-04	4.600e-04	5.731e-04
A to Z	2.117e-03	6.538e-03	1.357e-02	1.764e-02
B to Z	1.751e-03	5.162e-03	1.068e-02	1.393e-02
C to Z	2.563e-03	7.780e-03	1.602e-02	2.085e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

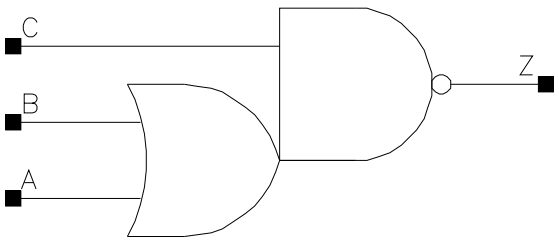
Pin Cycle (vdds)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.544	0.6528
X11_P10	1.200	0.952	1.1424
X17_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X17_P10	X23_P10
A	0.0010	0.0020	0.0030	0.0042
B	0.0009	0.0021	0.0029	0.0038
C	0.0010	0.0020	0.0029	0.0040
	X46_P10			
A	0.0083			
B	0.0076			
C	0.0080			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0099	0.0100	3.0273	1.4117
A to Z ↑	0.0142	0.0142	4.3494	2.0614
B to Z ↓	0.0080	0.0079	2.9810	1.3774

B to Z ↑	0.0151	0.0151	4.3726	2.0722
C to Z ↓	0.0086	0.0087	2.8409	1.3190
C to Z ↑	0.0085	0.0085	2.5803	1.2144
	X17_P10	**X23_P10**	**X17_P10**	**X23_P10**
A to Z ↓	0.0097	0.0102	0.9790	0.7259
A to Z ↑	0.0134	0.0146	1.3664	1.0450
B to Z ↓	0.0076	0.0078	0.9773	0.7272
B to Z ↑	0.0142	0.0147	1.3735	1.0497
C to Z ↓	0.0085	0.0086	0.9245	0.6846
C to Z ↑	0.0078	0.0081	0.8074	0.6146
	X46_P10		**X46_P10**	
A to Z ↓	0.0101		0.3780	
A to Z ↑	0.0142		0.5292	
B to Z ↓	0.0077		0.3749	
B to Z ↑	0.0145		0.5317	
C to Z ↓	0.0087		0.3552	
C to Z ↑	0.0079		0.3108	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.403e-05	1.000e-20
X11_P10	7.206e-05	1.000e-20
X17_P10	1.064e-04	1.000e-20
X23_P10	1.422e-04	1.000e-20
X46_P10	2.777e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	2.634e-05	5.853e-05	8.404e-05	1.539e-04
B (output stable)	3.652e-05	8.399e-05	1.204e-04	3.004e-04
C (output stable)	2.533e-04	5.970e-04	6.957e-04	1.123e-03
A to Z	2.502e-03	5.318e-03	7.547e-03	1.084e-02
B to Z	2.115e-03	4.537e-03	6.320e-03	8.750e-03
C to Z	1.881e-03	4.079e-03	5.769e-03	8.069e-03
	X46_P10			
A (output stable)	2.868e-04			
B (output stable)	5.465e-04			
C (output stable)	2.047e-03			
A to Z	2.101e-02			
B to Z	1.690e-02			
C to Z	1.558e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

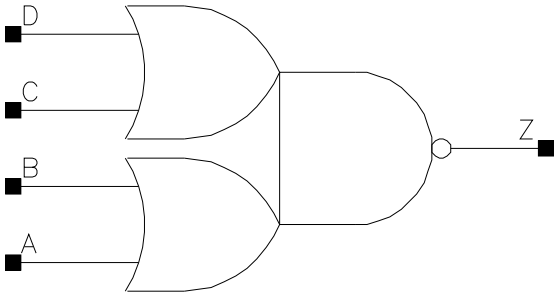
	X46_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0010	0.0020	0.0030	0.0041
B	0.0010	0.0019	0.0027	0.0038
C	0.0009	0.0019	0.0029	0.0040
D	0.0009	0.0018	0.0026	0.0037
	X42_P10			
A	0.0083			
B	0.0076			
C	0.0079			
D	0.0074			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0111	0.0121	2.7825	1.3840
A to Z ↑	0.0170	0.0168	4.5869	2.1103
B to Z ↓	0.0093	0.0099	2.7278	1.3901
B to Z ↑	0.0178	0.0169	4.6009	2.1186
C to Z ↓	0.0107	0.0118	2.8487	1.4050
C to Z ↑	0.0118	0.0123	4.4794	2.1198
D to Z ↓	0.0085	0.0090	2.7769	1.4155
D to Z ↑	0.0124	0.0118	4.5047	2.1332
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0114	0.0117	0.9448	0.6814
A to Z ↑	0.0157	0.0164	1.4214	1.0488
B to Z ↓	0.0094	0.0094	0.9491	0.6820
B to Z ↑	0.0162	0.0166	1.4283	1.0533
C to Z ↓	0.0113	0.0114	0.9618	0.6925
C to Z ↑	0.0113	0.0116	1.4286	1.0518
D to Z ↓	0.0089	0.0089	0.9710	0.6958
D to Z ↑	0.0113	0.0116	1.4387	1.0583
	X42_P10		**X42_P10**	
A to Z ↓	0.0119		0.3570	
A to Z ↑	0.0163		0.5351	
B to Z ↓	0.0096		0.3538	
B to Z ↑	0.0167		0.5376	
C to Z ↓	0.0120		0.3642	
C to Z ↑	0.0117		0.5328	
D to Z ↓	0.0092		0.3614	
D to Z ↑	0.0117		0.5365	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	4.098e-05	1.000e-20
X10_P10	8.813e-05	1.000e-20
X15_P10	1.285e-04	1.000e-20
X21_P10	1.746e-04	1.000e-20
X42_P10	3.437e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	3.674e-05	1.165e-04	1.499e-04	2.178e-04
B (output stable)	5.861e-05	2.917e-04	2.962e-04	4.797e-04
C (output stable)	8.508e-05	2.258e-04	2.844e-04	4.087e-04
D (output stable)	1.097e-04	4.010e-04	4.251e-04	6.642e-04
A to Z	2.920e-03	6.442e-03	8.984e-03	1.265e-02
B to Z	2.546e-03	5.352e-03	7.477e-03	1.054e-02
C to Z	2.216e-03	5.026e-03	6.951e-03	9.727e-03
D to Z	1.868e-03	3.960e-03	5.542e-03	7.748e-03
	X42_P10			
A (output stable)	4.256e-04			
B (output stable)	9.081e-04			
C (output stable)	7.993e-04			
D (output stable)	1.288e-03			

A to Z	2.492e-02			
B to Z	2.072e-02			
C to Z	1.922e-02			
D to Z	1.532e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

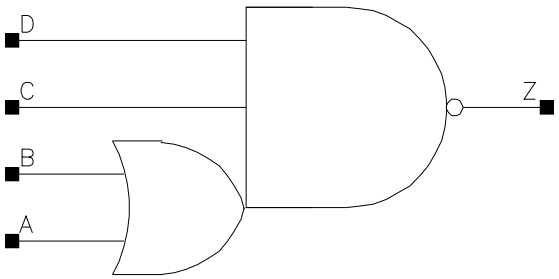
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X21_P10	1.200	2.448	2.9376
X31_P10	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X21_P10	X31_P10
A	0.0010	0.0019	0.0038	0.0056
B	0.0012	0.0018	0.0035	0.0052
C	0.0010	0.0021	0.0041	0.0062
D	0.0010	0.0020	0.0039	0.0058

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0153	0.0149	3.7400	2.0024
A to Z ↑	0.0145	0.0133	4.1592	2.0967
B to Z ↓	0.0131	0.0117	3.8037	2.0151
B to Z ↑	0.0152	0.0129	4.1932	2.1103
C to Z ↓	0.0127	0.0130	3.5321	1.8848

C to Z ↑	0.0144	0.0141	2.3521	1.1848
D to Z ↓	0.0139	0.0133	3.5543	1.8951
D to Z ↑	0.0134	0.0125	2.3828	1.1888
	X21_P10	**X31_P10**	**X21_P10**	**X31_P10**
A to Z ↓	0.0150	0.0150	1.0428	0.7078
A to Z ↑	0.0127	0.0126	1.0481	0.7044
B to Z ↓	0.0117	0.0117	1.0504	0.7155
B to Z ↑	0.0124	0.0123	1.0548	0.7095
C to Z ↓	0.0127	0.0127	0.9828	0.6679
C to Z ↑	0.0136	0.0135	0.6004	0.4057
D to Z ↓	0.0133	0.0133	0.9877	0.6715
D to Z ↑	0.0121	0.0121	0.6020	0.4057

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.104e-05	1.000e-20
X10_P10	5.958e-05	1.000e-20
X21_P10	1.150e-04	1.000e-20
X31_P10	1.705e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	1.568e-04	3.453e-04	6.375e-04	9.300e-04
B (output stable)	1.713e-04	3.808e-04	6.932e-04	1.026e-03
C (output stable)	4.123e-05	1.201e-04	2.255e-04	3.320e-04
D (output stable)	6.823e-05	2.517e-04	4.574e-04	6.614e-04
A to Z	2.816e-03	5.071e-03	9.725e-03	1.430e-02
B to Z	2.288e-03	3.979e-03	7.591e-03	1.118e-02
C to Z	3.452e-03	6.662e-03	1.267e-02	1.871e-02
D to Z	3.120e-03	5.718e-03	1.093e-02	1.617e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

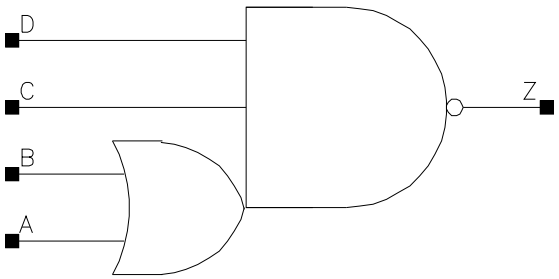
Pin Cycle (vdds)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0011	0.0021	0.0031	0.0041
B	0.0010	0.0019	0.0029	0.0038
C	0.0010	0.0020	0.0030	0.0039
D	0.0010	0.0019	0.0029	0.0038

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0131	0.0142	3.8086	1.9907
A to Z ↑	0.0165	0.0179	4.0282	2.0588
B to Z ↓	0.0110	0.0116	3.7447	1.9957
B to Z ↑	0.0175	0.0180	4.0476	2.0667
C to Z ↓	0.0110	0.0123	3.6036	1.9016

C to Z ↑	0.0109	0.0116	2.3947	1.2116
D to Z ↓	0.0117	0.0124	3.6306	1.9125
D to Z ↑	0.0092	0.0094	2.4163	1.2231
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0139	0.0140	1.3668	1.0325
A to Z ↑	0.0170	0.0175	1.3885	1.0536
B to Z ↓	0.0115	0.0114	1.3626	1.0321
B to Z ↑	0.0176	0.0180	1.3958	1.0582
C to Z ↓	0.0119	0.0122	1.3010	0.9836
C to Z ↑	0.0110	0.0113	0.8085	0.6078
D to Z ↓	0.0122	0.0126	1.3090	0.9890
D to Z ↑	0.0089	0.0092	0.8157	0.6135

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.098e-05	1.000e-20
X10_P10	6.060e-05	1.000e-20
X15_P10	8.729e-05	1.000e-20
X21_P10	1.177e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	2.359e-05	5.289e-05	7.746e-05	9.941e-05
B (output stable)	2.732e-05	9.297e-05	1.096e-04	1.636e-04
C (output stable)	7.479e-05	1.641e-04	2.423e-04	3.242e-04
D (output stable)	1.475e-04	4.839e-04	5.679e-04	8.545e-04
A to Z	3.226e-03	6.871e-03	9.776e-03	1.337e-02
B to Z	2.783e-03	5.697e-03	8.156e-03	1.110e-02
C to Z	2.441e-03	5.224e-03	7.372e-03	1.013e-02
D to Z	2.148e-03	4.450e-03	6.337e-03	8.624e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

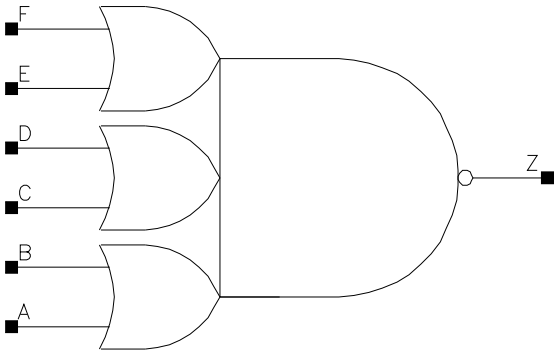
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	1.088	1.3056
X9_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X9_P10
A	0.0009	0.0021
B	0.0008	0.0019
C	0.0008	0.0020
D	0.0008	0.0018
E	0.0008	0.0019
F	0.0008	0.0018

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X9_P10	X3_P10	X9_P10
A to Z ↓	0.0168	0.0183	4.3588	1.8105
A to Z ↑	0.0231	0.0220	5.5997	2.0713
B to Z ↓	0.0153	0.0158	4.3994	1.8158
B to Z ↑	0.0248	0.0225	5.6196	2.0772
C to Z ↓	0.0166	0.0177	4.4046	1.8238
C to Z ↑	0.0197	0.0187	5.6218	2.0684
D to Z ↓	0.0148	0.0151	4.4492	1.8315
D to Z ↑	0.0213	0.0190	5.6480	2.0771
E to Z ↓	0.0150	0.0164	4.4489	1.8325
E to Z ↑	0.0149	0.0142	5.6504	2.0751
F to Z ↓	0.0133	0.0135	4.4993	1.8400
F to Z ↑	0.0160	0.0139	5.6900	2.0882

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	3.525e-05	1.000e-20
X9_P10	1.033e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X9_P10
A (output stable)	3.188e-05	1.123e-04
B (output stable)	4.231e-05	2.252e-04
C (output stable)	6.029e-05	1.722e-04
D (output stable)	7.031e-05	2.880e-04
E (output stable)	1.799e-04	4.580e-04
F (output stable)	1.926e-04	5.641e-04
A to Z	3.557e-03	9.271e-03
B to Z	3.243e-03	8.084e-03
C to Z	2.926e-03	7.641e-03
D to Z	2.634e-03	6.580e-03
E to Z	2.257e-03	6.118e-03
F to Z	1.987e-03	5.043e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

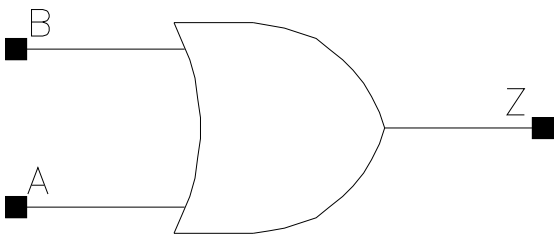
Pin Cycle (vdds)	X3_P10	X9_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X33_P10	1.200	1.360	1.6320
X50_P10	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P10	X16_P10	X33_P10	X50_P10
A	0.0009	0.0011	0.0022	0.0023
B	0.0008	0.0011	0.0023	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0262	0.0235	1.6864	0.8504
A to Z ↑	0.0179	0.0195	2.3344	1.1781
B to Z ↓	0.0275	0.0248	1.6867	0.8508
B to Z ↑	0.0167	0.0180	2.3363	1.1769
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0242	0.0293	0.4205	0.2883
A to Z ↑	0.0195	0.0196	0.5753	0.3887
B to Z ↓	0.0246	0.0302	0.4204	0.2885
B to Z ↑	0.0175	0.0181	0.5744	0.3884

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	3.459e-05	1.000e-20
X16_P10	6.922e-05	1.000e-20
X33_P10	1.396e-04	1.000e-20
X50_P10	1.801e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	2.332e-05	4.220e-05	1.419e-04	1.350e-04
B (output stable)	4.670e-05	8.156e-05	4.260e-04	3.954e-04
A to Z	3.996e-03	6.880e-03	1.426e-02	2.060e-02
B to Z	3.793e-03	6.520e-03	1.314e-02	1.954e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

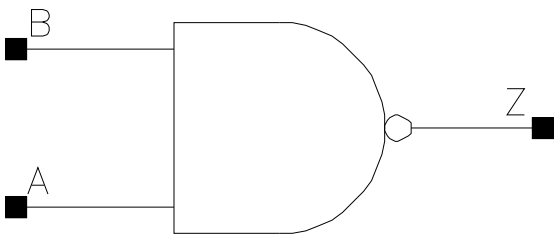
Pin Cycle (vdds)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X16_P10	1.200	0.952	1.1424
X24_P10	1.200	1.088	1.3056
X32_P10	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P10	X16_P10	X24_P10	X32_P10
A	0.0012	0.0012	0.0012	0.0012
B	0.0013	0.0013	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0238	0.0250	1.6493	0.8566
A to Z ↑	0.0257	0.0267	2.3663	1.2064
B to Z ↓	0.0254	0.0266	1.6490	0.8557
B to Z ↑	0.0241	0.0246	2.3647	1.2065
	X24_P10	**X32_P10**	**X24_P10**	**X32_P10**
A to Z ↓	0.0278	0.0288	0.5771	0.4322
A to Z ↑	0.0288	0.0295	0.8064	0.6027
B to Z ↓	0.0295	0.0307	0.5768	0.4319
B to Z ↑	0.0267	0.0280	0.8057	0.6019

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	8.271e-05	1.000e-20
X16_P10	1.028e-04	1.000e-20
X24_P10	1.220e-04	1.000e-20
X32_P10	1.688e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	2.450e-05	2.468e-05	2.481e-05	2.609e-05
B (output stable)	5.122e-05	5.152e-05	5.169e-05	5.119e-05
A to Z	7.206e-03	8.636e-03	1.116e-02	1.471e-02
B to Z	6.903e-03	8.345e-03	1.089e-02	1.443e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

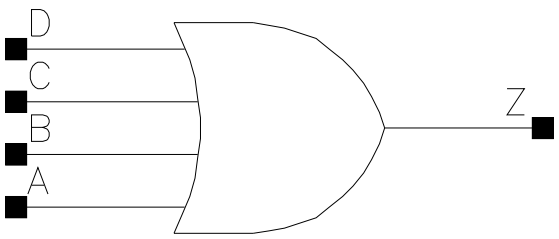
Pin Cycle (vdds)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P10	1.200	2.176	2.6112
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P10	X27_P10
A	0.0020	0.0023
B	0.0019	0.0024
C	0.0020	0.0024
D	0.0019	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P10	X27_P10	X20_P10	X27_P10
A to Z ↓	0.0267	0.0281	0.9548	0.7139
A to Z ↑	0.0199	0.0193	0.7712	0.5755
B to Z ↓	0.0274	0.0285	0.9547	0.7140
B to Z ↑	0.0184	0.0174	0.7707	0.5740
C to Z ↓	0.0262	0.0277	0.9533	0.7125
C to Z ↑	0.0188	0.0188	0.7725	0.5771
D to Z ↓	0.0268	0.0282	0.9530	0.7122
D to Z ↑	0.0174	0.0171	0.7715	0.5762

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X20_P10	1.169e-04	1.000e-20
X27_P10	1.685e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X20_P10	X27_P10
A (output stable)	2.758e-03	3.810e-03
B (output stable)	2.513e-03	3.476e-03
C (output stable)	2.447e-03	3.476e-03
D (output stable)	2.199e-03	3.190e-03
A to Z	1.206e-02	1.681e-02
B to Z	1.129e-02	1.562e-02
C to Z	1.084e-02	1.505e-02
D to Z	1.008e-02	1.399e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

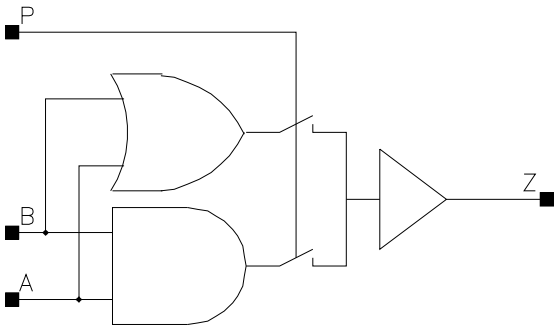
Pin Cycle (vdds)	X20_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X16_P10	1.200	1.224	1.4688
X25_P10	1.200	2.040	2.4480
X33_P10	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0014	0.0022	0.0038	0.0038
B	0.0014	0.0021	0.0043	0.0043
P	0.0008	0.0012	0.0022	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0318	0.0294	1.7151	0.8398
A to Z ↑	0.0233	0.0227	2.3757	1.1886
B to Z ↓	0.0323	0.0302	1.7229	0.8441
B to Z ↑	0.0244	0.0239	2.3787	1.1905
P to Z ↓	0.0306	0.0289	1.7196	0.8424
P to Z ↑	0.0240	0.0236	2.3758	1.1878
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**

A to Z ↓	0.0279	0.0298	0.5704	0.4305
A to Z ↑	0.0222	0.0235	0.7996	0.5982
B to Z ↓	0.0284	0.0301	0.5728	0.4324
B to Z ↑	0.0236	0.0248	0.8004	0.5989
P to Z ↓	0.0279	0.0298	0.5717	0.4315
P to Z ↑	0.0230	0.0243	0.7982	0.5973

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	4.530e-05	1.000e-20
X16_P10	9.824e-05	1.000e-20
X25_P10	1.660e-04	1.000e-20
X33_P10	1.922e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	4.957e-05	7.934e-05	1.731e-04	1.770e-04
B (output stable)	6.905e-05	1.219e-04	3.325e-04	3.374e-04
P (output stable)	2.170e-04	3.730e-04	5.545e-04	5.704e-04
A to Z	4.587e-03	8.281e-03	1.366e-02	1.648e-02
B to Z	4.492e-03	8.179e-03	1.323e-02	1.608e-02
P to Z	4.238e-03	7.800e-03	1.283e-02	1.565e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

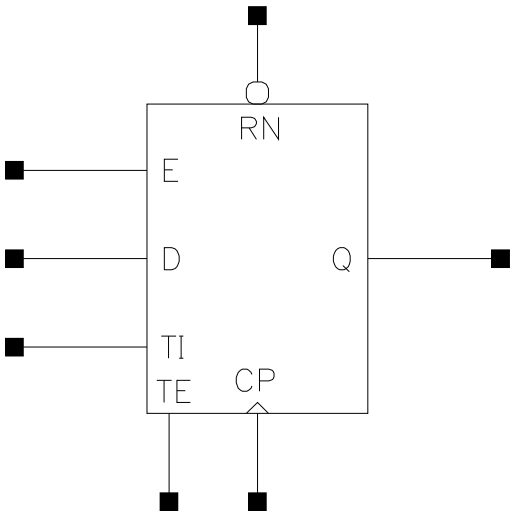
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.488	5.3856
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0008	0.0008	0.0008
E	0.0011	0.0012	0.0012	0.0012
RN	0.0010	0.0008	0.0009	0.0010
TE	0.0011	0.0011	0.0011	0.0011

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to Q ↓	0.0577	0.0334	3.4964	1.6697
CP to Q ↑	0.0512	0.0444	4.6366	2.3526
RN to Q ↓	0.0425	0.0495	3.1927	1.6307
	X17_P10	X33_P10	X17_P10	X33_P10
CP to Q ↓	0.0579	0.0615	0.8169	0.4271
CP to Q ↑	0.0711	0.0750	1.1506	0.5874
RN to Q ↓	0.0681	0.0724	0.8174	0.4270

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0722	0.0504	0.0504	0.0504
CP ↑	min_pulse_width to CP	0.0518	0.0271	0.0271	0.0271
D ↓	hold_rising to CP	-0.0718	-0.0316	-0.0316	-0.0316
D ↑	hold_rising to CP	-0.0511	-0.0115	-0.0142	-0.0142
D ↓	setup_rising to CP	0.1069	0.0689	0.0689	0.0689
D ↑	setup_rising to CP	0.0806	0.0418	0.0418	0.0418
E ↓	hold_rising to CP	-0.0523	-0.0582	-0.0582	-0.0582
E ↑	hold_rising to CP	-0.0457	-0.0122	-0.0122	-0.0122
E ↓	setup_rising to CP	0.0954	0.0931	0.0931	0.0931
E ↑	setup_rising to CP	0.1009	0.0715	0.0715	0.0715
RN ↓	min_pulse_width to RN	0.0544	0.0615	0.0518	0.0518
RN ↑	recovery_rising to CP	0.0125	0.0129	0.0129	0.0129
RN ↑	removal_rising to CP	-0.0078	-0.0029	-0.0029	-0.0029
TE ↓	hold_rising to CP	-0.0311	-0.0186	-0.0186	-0.0186
TE ↑	hold_rising to CP	-0.0311	-0.0185	-0.0185	-0.0185
TE ↓	setup_rising to CP	0.0700	0.0635	0.0635	0.0635
TE ↑	setup_rising to CP	0.1248	0.0911	0.0911	0.0911
TI ↓	hold_rising to CP	-0.0918	-0.0459	-0.0459	-0.0459
TI ↑	hold_rising to CP	-0.0354	-0.0192	-0.0190	-0.0190
TI ↓	setup_rising to CP	0.1274	0.0806	0.0806	0.0806
TI ↑	setup_rising to CP	0.0661	0.0430	0.0430	0.0430

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.289e-04	1.000e-20
X8_P10	1.494e-04	1.000e-20
X17_P10	1.946e-04	1.000e-20
X33_P10	2.627e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

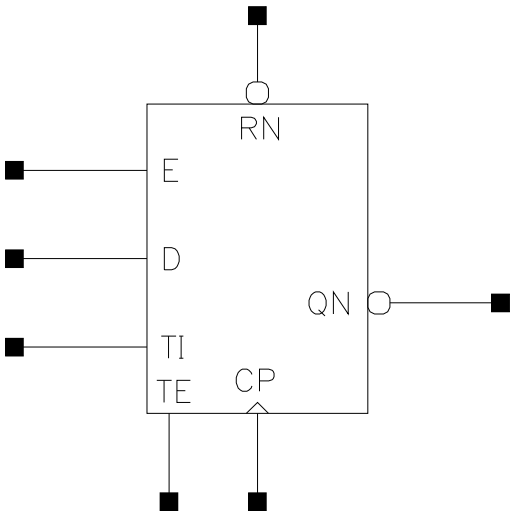
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.264e-02	1.271e-02	1.273e-02	1.274e-02
Clock 100Mhz Data 25Mhz	1.382e-02	1.385e-02	1.488e-02	1.640e-02
Clock 100Mhz Data 50Mhz	1.500e-02	1.500e-02	1.704e-02	2.006e-02
Clock = 0 Data 100Mhz	9.994e-03	9.360e-03	9.150e-03	9.047e-03
Clock = 1 Data 100Mhz	3.216e-03	3.324e-03	3.363e-03	3.382e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.624	5.5488
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0009	0.0008	0.0008	0.0008
E	0.0011	0.0012	0.0012	0.0012
RN	0.0010	0.0010	0.0010	0.0010
TE	0.0011	0.0011	0.0011	0.0011

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to QN ↓	0.0623	0.0594	3.0610	1.6168
CP to QN ↑	0.0644	0.0444	4.5287	2.2860
RN to QN ↑	0.0523	0.0555	4.5210	2.2872
	X17_P10	X33_P10	X17_P10	X33_P10
CP to QN ↓	0.0576	0.0614	0.8182	0.4263
CP to QN ↑	0.0462	0.0507	1.1528	0.5876
RN to QN ↑	0.0612	0.0646	1.1503	0.5863

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0722	0.0504	0.0504	0.0504
CP ↑	min_pulse_width to CP	0.0377	0.0271	0.0271	0.0284
D ↓	hold_rising to CP	-0.0718	-0.0316	-0.0316	-0.0316
D ↑	hold_rising to CP	-0.0511	-0.0142	-0.0142	-0.0115
D ↓	setup_rising to CP	0.1064	0.0689	0.0689	0.0689
D ↑	setup_rising to CP	0.0806	0.0418	0.0418	0.0418
E ↓	hold_rising to CP	-0.0523	-0.0582	-0.0582	-0.0582
E ↑	hold_rising to CP	-0.0457	-0.0122	-0.0122	-0.0122
E ↓	setup_rising to CP	0.0954	0.0931	0.0931	0.0931
E ↑	setup_rising to CP	0.1009	0.0715	0.0715	0.0715
RN ↓	min_pulse_width to RN	0.0496	0.0496	0.0615	0.0664
RN ↑	recovery_rising to CP	0.0125	0.0129	0.0129	0.0129
RN ↑	removal_rising to CP	-0.0078	-0.0029	-0.0029	-0.0029
TE ↓	hold_rising to CP	-0.0311	-0.0186	-0.0186	-0.0191
TE ↑	hold_rising to CP	-0.0311	-0.0185	-0.0185	-0.0185
TE ↓	setup_rising to CP	0.0700	0.0635	0.0635	0.0635
TE ↑	setup_rising to CP	0.1248	0.0911	0.0911	0.0911
TI ↓	hold_rising to CP	-0.0918	-0.0459	-0.0459	-0.0459
TI ↑	hold_rising to CP	-0.0354	-0.0190	-0.0192	-0.0192
TI ↓	setup_rising to CP	0.1274	0.0806	0.0799	0.0814
TI ↑	setup_rising to CP	0.0661	0.0430	0.0430	0.0430

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.279e-04	1.000e-20
X8_P10	1.423e-04	1.000e-20
X17_P10	1.828e-04	1.000e-20
X33_P10	2.378e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

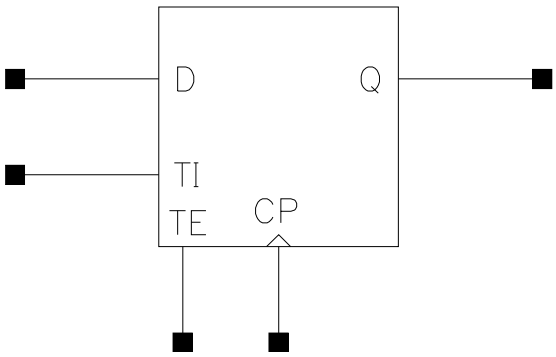
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.263e-02	1.271e-02	1.272e-02	1.272e-02
Clock 100Mhz Data 25Mhz	1.359e-02	1.387e-02	1.486e-02	1.640e-02
Clock 100Mhz Data 50Mhz	1.455e-02	1.503e-02	1.700e-02	2.008e-02
Clock = 0 Data 100Mhz	1.001e-02	9.366e-03	9.155e-03	9.051e-03
Clock = 1 Data 100Mhz	3.213e-03	3.325e-03	3.364e-03	3.385e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.400	4.0800
X8_P10	1.200	3.128	3.7536
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0479	0.0312	3.3238	1.6728
CP to Q ↑	0.0460	0.0406	4.6512	2.3213
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0479	0.0531	0.8056	0.4206
CP to Q ↑	0.0683	0.0730	1.1511	0.5872

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0669	0.0708	0.0708	0.0708
CP ↑	min_pulse_width to CP	0.0377	0.0236	0.0237	0.0237
D ↓	hold_rising to CP	-0.0425	-0.0115	-0.0147	-0.0147
D ↑	hold_rising to CP	-0.0159	0.0025	0.0025	0.0025
D ↓	setup_rising to CP	0.0727	0.0493	0.0461	0.0461
D ↑	setup_rising to CP	0.0407	0.0223	0.0223	0.0223
TE ↓	hold_rising to CP	-0.0279	-0.0098	-0.0098	-0.0098
TE ↑	hold_rising to CP	-0.0234	-0.0120	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.0610	0.0467	0.0467	0.0467
TE ↑	setup_rising to CP	0.1155	0.0927	0.0927	0.0927
TI ↓	hold_rising to CP	-0.0869	-0.0521	-0.0514	-0.0514
TI ↑	hold_rising to CP	-0.0256	-0.0098	-0.0141	-0.0141
TI ↓	setup_rising to CP	0.1166	0.0919	0.0919	0.0919
TI ↑	setup_rising to CP	0.0548	0.0404	0.0404	0.0404

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.040e-04	1.000e-20
X8_P10	1.248e-04	1.000e-20
X17_P10	1.822e-04	1.000e-20
X33_P10	2.332e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

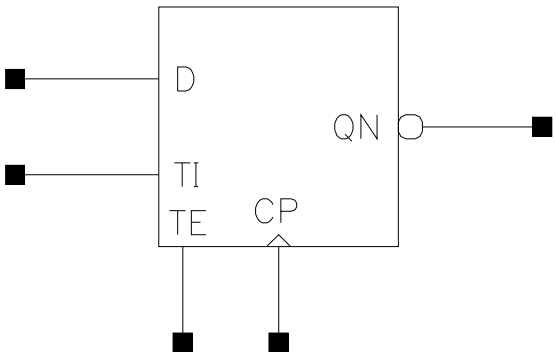
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.155e-02	1.166e-02	1.169e-02	1.171e-02
Clock 100Mhz Data 25Mhz	1.175e-02	1.182e-02	1.288e-02	1.426e-02
Clock 100Mhz Data 50Mhz	1.194e-02	1.197e-02	1.408e-02	1.682e-02
Clock = 0 Data 100Mhz	7.826e-03	7.234e-03	7.037e-03	6.938e-03
Clock = 1 Data 100Mhz	1.825e-03	9.366e-04	6.405e-04	4.926e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.536	4.2432
X8_P10	1.200	3.264	3.9168
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0580	0.0617	3.4858	1.6576
CP to QN ↑	0.0517	0.0410	4.6111	2.2875
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0498	0.0556	0.8063	0.4211
CP to QN ↑	0.0409	0.0458	1.1514	0.5872

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0669	0.0708	0.0708	0.0708
CP ↑	min_pulse_width to CP	0.0318	0.0237	0.0271	0.0271
D ↓	hold_rising to CP	-0.0425	-0.0147	-0.0115	-0.0115
D ↑	hold_rising to CP	-0.0159	0.0025	0.0025	0.0025
D ↓	setup_rising to CP	0.0727	0.0461	0.0493	0.0493
D ↑	setup_rising to CP	0.0407	0.0223	0.0223	0.0223
TE ↓	hold_rising to CP	-0.0279	-0.0098	-0.0098	-0.0098
TE ↑	hold_rising to CP	-0.0234	-0.0120	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.0610	0.0467	0.0467	0.0467
TE ↑	setup_rising to CP	0.1155	0.0901	0.0927	0.0927
TI ↓	hold_rising to CP	-0.0869	-0.0514	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0256	-0.0141	-0.0098	-0.0098
TI ↓	setup_rising to CP	0.1166	0.0919	0.0919	0.0919
TI ↑	setup_rising to CP	0.0564	0.0404	0.0404	0.0404

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.050e-04	1.000e-20
X8_P10	1.254e-04	1.000e-20
X17_P10	1.811e-04	1.000e-20
X33_P10	2.321e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

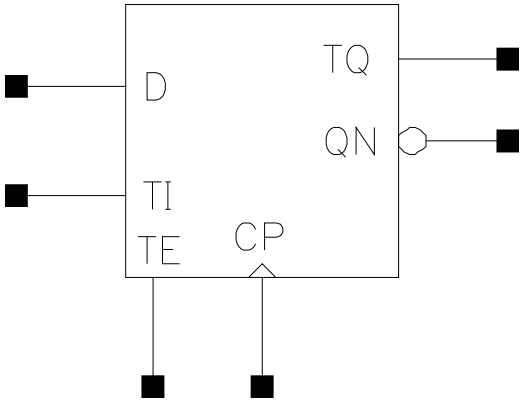
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.145e-02	1.160e-02	1.165e-02	1.168e-02
Clock 100Mhz Data 25Mhz	1.159e-02	1.194e-02	1.282e-02	1.424e-02
Clock 100Mhz Data 50Mhz	1.173e-02	1.227e-02	1.399e-02	1.680e-02
Clock = 0 Data 100Mhz	7.870e-03	7.246e-03	7.043e-03	6.942e-03
Clock = 1 Data 100Mhz	1.814e-03	9.312e-04	6.369e-04	4.899e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.536	4.2432
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0014	0.0011	0.0011	0.0011
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0012	0.0012	0.0012

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0647	0.0573	3.1774	1.6335
CP to QN ↑	0.0626	0.0425	4.5393	2.2995
CP to TQ ↓	0.0433	0.0281	4.2434	3.0154
CP to TQ ↑	0.0471	0.0402	8.1955	6.0105
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0549	0.0602	0.8223	0.4298
CP to QN ↑	0.0444	0.0483	1.1648	0.5987
CP to TQ ↓	0.0290	0.0301	3.9694	3.9831
CP to TQ ↑	0.0408	0.0420	7.6058	8.0027

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0669	0.0708	0.0708	0.0708
CP ↑	min_pulse_width to CP	0.0377	0.0236	0.0271	0.0271
D ↓	hold_rising to CP	-0.0430	-0.0115	-0.0115	-0.0115
D ↑	hold_rising to CP	-0.0159	0.0025	0.0025	0.0025
D ↓	setup_rising to CP	0.0727	0.0461	0.0461	0.0461
D ↑	setup_rising to CP	0.0407	0.0223	0.0249	0.0223
TE ↓	hold_rising to CP	-0.0279	-0.0098	-0.0098	-0.0098
TE ↑	hold_rising to CP	-0.0234	-0.0120	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.0577	0.0467	0.0467	0.0467
TE ↑	setup_rising to CP	0.1096	0.0901	0.0901	0.0901
TI ↓	hold_rising to CP	-0.0869	-0.0521	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0256	-0.0098	-0.0141	-0.0098
TI ↓	setup_rising to CP	0.1166	0.0919	0.0919	0.0919
TI ↑	setup_rising to CP	0.0564	0.0388	0.0404	0.0388

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.115e-04	1.000e-20
X8_P10	1.386e-04	1.000e-20
X17_P10	1.710e-04	1.000e-20
X33_P10	2.302e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10

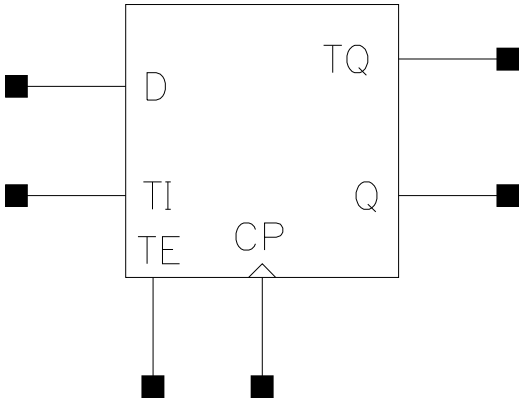
Clock 100Mhz Data 0Mhz	1.170e-02	1.173e-02	1.174e-02	1.175e-02
Clock 100Mhz Data 25Mhz	1.213e-02	1.236e-02	1.294e-02	1.455e-02
Clock 100Mhz Data 50Mhz	1.256e-02	1.299e-02	1.413e-02	1.735e-02
Clock = 0 Data 100Mhz	7.860e-03	7.259e-03	7.061e-03	6.960e-03
Clock = 1 Data 100Mhz	1.827e-03	9.377e-04	6.414e-04	4.932e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.400	4.0800
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008

TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0633	0.0349	3.4728	1.6608
CP to Q ↑	0.0532	0.0433	4.7036	2.3384
CP to TQ ↓	0.0593	0.0347	3.4733	4.0664
CP to TQ ↑	0.0546	0.0469	6.0613	8.1297
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0493	0.0545	0.8271	0.4282
CP to Q ↑	0.0696	0.0742	1.1759	0.5901
CP to TQ ↓	0.0506	0.0559	3.9393	4.0079
CP to TQ ↑	0.0735	0.0797	7.8807	7.9679

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0676	0.0708	0.0708	0.0708
CP ↑	min_pulse_width to CP	0.0552	0.0271	0.0237	0.0237
D ↓	hold_rising to CP	-0.0425	-0.0115	-0.0147	-0.0147
D ↑	hold_rising to CP	-0.0159	0.0025	0.0025	0.0025
D ↓	setup_rising to CP	0.0727	0.0461	0.0461	0.0461
D ↑	setup_rising to CP	0.0407	0.0223	0.0223	0.0223
TE ↓	hold_rising to CP	-0.0279	-0.0098	-0.0098	-0.0098
TE ↑	hold_rising to CP	-0.0234	-0.0120	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.0610	0.0467	0.0467	0.0467
TE ↑	setup_rising to CP	0.1155	0.0901	0.0927	0.0927
TI ↓	hold_rising to CP	-0.0869	-0.0521	-0.0514	-0.0514
TI ↑	hold_rising to CP	-0.0256	-0.0098	-0.0141	-0.0141
TI ↓	setup_rising to CP	0.1166	0.0919	0.0919	0.0919
TI ↑	setup_rising to CP	0.0548	0.0404	0.0404	0.0404

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.136e-04	1.000e-20
X8_P10	1.309e-04	1.000e-20
X17_P10	1.873e-04	1.000e-20
X33_P10	2.382e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

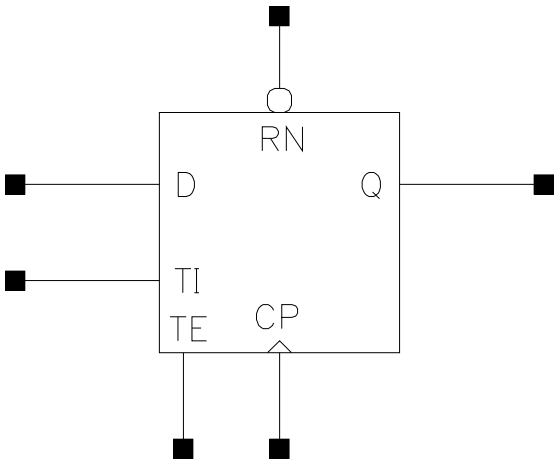
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.151e-02	1.163e-02	1.167e-02	1.169e-02
Clock 100Mhz Data 25Mhz	1.251e-02	1.220e-02	1.318e-02	1.463e-02
Clock 100Mhz Data 50Mhz	1.350e-02	1.277e-02	1.468e-02	1.756e-02
Clock = 0 Data 100Mhz	7.813e-03	7.220e-03	7.028e-03	6.931e-03
Clock = 1 Data 100Mhz	1.811e-03	9.300e-04	6.363e-04	4.895e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.672	4.4064
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0008	0.0008	0.0008
RN	0.0010	0.0008	0.0009	0.0009
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0572	0.0334	3.5304	1.6729
CP to Q ↑	0.0508	0.0436	4.6557	2.3491
RN to Q ↓	0.0422	0.0496	3.2062	1.6351
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0498	0.0554	0.8128	0.4260
CP to Q ↑	0.0634	0.0679	1.1484	0.5865
RN to Q ↓	0.0604	0.0660	0.8134	0.4262

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0740	0.0708	0.0723	0.0706
CP ↑	min_pulse_width to CP	0.0505	0.0271	0.0237	0.0237
D ↓	hold_rising to CP	-0.0381	-0.0045	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0208	0.0009	-0.0023	-0.0023
D ↓	setup_rising to CP	0.0733	0.0445	0.0440	0.0440
D ↑	setup_rising to CP	0.0514	0.0298	0.0298	0.0298
RN ↓	min_pulse_width to RN	0.0518	0.0566	0.0496	0.0496
RN ↑	recovery_rising to CP	0.0151	0.0129	0.0129	0.0129
RN ↑	removal_rising to CP	-0.0078	-0.0029	-0.0029	-0.0029
TE ↓	hold_rising to CP	-0.0262	-0.0023	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0311	-0.0169	-0.0196	-0.0196
TE ↓	setup_rising to CP	0.0635	0.0488	0.0488	0.0488
TE ↑	setup_rising to CP	0.1106	0.0862	0.0862	0.0862
TI ↓	hold_rising to CP	-0.0830	-0.0410	-0.0426	-0.0426
TI ↑	hold_rising to CP	-0.0364	-0.0205	-0.0202	-0.0202
TI ↓	setup_rising to CP	0.1160	0.0812	0.0812	0.0812
TI ↑	setup_rising to CP	0.0603	0.0443	0.0502	0.0486

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.191e-04	1.000e-20
X8_P10	1.359e-04	1.000e-20
X17_P10	1.907e-04	1.000e-20
X33_P10	2.500e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.263e-02	1.270e-02	1.277e-02	1.281e-02

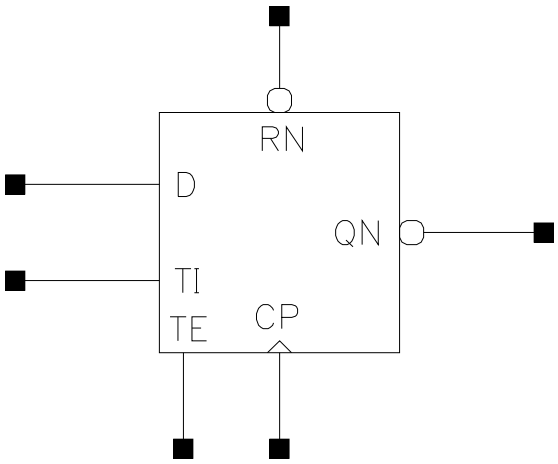
Clock 100Mhz Data 25Mhz	1.301e-02	1.283e-02	1.392e-02	1.534e-02
Clock 100Mhz Data 50Mhz	1.338e-02	1.295e-02	1.506e-02	1.787e-02
Clock = 0 Data 100Mhz	7.746e-03	7.042e-03	6.811e-03	6.695e-03
Clock = 1 Data 100Mhz	1.856e-03	9.536e-04	6.531e-04	5.030e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	3.944	4.7328
X33_P10	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0008	0.0008	0.0008
RN	0.0010	0.0009	0.0010	0.0010
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to QN ↓	0.0566	0.0534	3.0208	1.5874
CP to QN ↑	0.0589	0.0399	4.5221	2.2731
RN to QN ↑	0.0473	0.0509	4.5159	2.2746
	X17_P10	X33_P10	X17_P10	X33_P10
CP to QN ↓	0.0537	0.0594	0.8136	0.4254
CP to QN ↑	0.0443	0.0494	1.1585	0.5937
RN to QN ↑	0.0598	0.0644	1.1566	0.5935

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0740	0.0707	0.0708	0.0708
CP ↑	min_pulse_width to CP	0.0365	0.0237	0.0271	0.0271
D ↓	hold_rising to CP	-0.0381	-0.0045	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0208	-0.0023	0.0009	0.0009
D ↓	setup_rising to CP	0.0733	0.0445	0.0440	0.0440
D ↑	setup_rising to CP	0.0514	0.0298	0.0298	0.0298
RN ↓	min_pulse_width to RN	0.0469	0.0496	0.0615	0.0637
RN ↑	recovery_rising to CP	0.0151	0.0125	0.0129	0.0129
RN ↑	removal_rising to CP	-0.0078	-0.0050	-0.0029	-0.0029
TE ↓	hold_rising to CP	-0.0262	-0.0023	-0.0027	-0.0027
TE ↑	hold_rising to CP	-0.0311	-0.0196	-0.0196	-0.0196
TE ↓	setup_rising to CP	0.0635	0.0488	0.0488	0.0488
TE ↑	setup_rising to CP	0.1106	0.0862	0.0862	0.0862
TI ↓	hold_rising to CP	-0.0830	-0.0410	-0.0410	-0.0410
TI ↑	hold_rising to CP	-0.0364	-0.0205	-0.0205	-0.0205
TI ↓	setup_rising to CP	0.1160	0.0819	0.0812	0.0812
TI ↑	setup_rising to CP	0.0603	0.0443	0.0443	0.0443

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.192e-04	1.000e-20
X8_P10	1.288e-04	1.000e-20
X17_P10	1.826e-04	1.000e-20
X33_P10	2.247e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.254e-02	1.265e-02	1.269e-02	1.271e-02

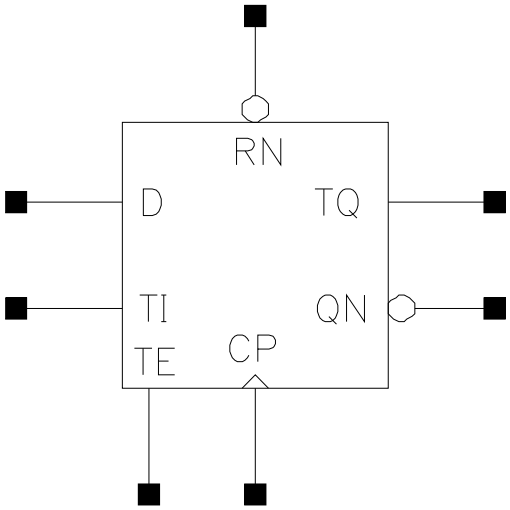
Clock 100Mhz Data 25Mhz	1.263e-02	1.273e-02	1.383e-02	1.524e-02
Clock 100Mhz Data 50Mhz	1.273e-02	1.281e-02	1.497e-02	1.778e-02
Clock = 0 Data 100Mhz	7.741e-03	7.036e-03	6.809e-03	6.695e-03
Clock = 1 Data 100Mhz	1.854e-03	9.526e-04	6.525e-04	5.025e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0008	0.0008	0.0008

RN	0.0012	0.0009	0.0010	0.0010
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0632	0.0558	3.0303	1.6725
CP to QN ↑	0.0761	0.0445	4.0705	2.3598
CP to TQ ↓	0.0532	0.0298	3.7563	3.1544
CP to TQ ↑	0.0522	0.0436	6.7345	6.2841
RN to QN ↑	0.0551	0.0578	4.1299	2.3513
RN to TQ ↓	0.0408	0.0477	3.3818	3.0889
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0581	0.0637	0.8287	0.4352
CP to QN ↑	0.0456	0.0487	1.1796	0.5952
CP to TQ ↓	0.0310	0.0320	3.8863	3.8025
CP to TQ ↑	0.0434	0.0445	5.9314	6.0153
RN to QN ↑	0.0614	0.0637	1.1805	0.5960
RN to TQ ↓	0.0485	0.0490	3.8189	3.7274

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0740	0.0707	0.0707	0.0707
CP ↑	min_pulse_width to CP	0.0518	0.0271	0.0271	0.0271
D ↓	hold_rising to CP	-0.0381	-0.0045	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0208	0.0009	-0.0023	-0.0023
D ↓	setup_rising to CP	0.0733	0.0445	0.0440	0.0440
D ↑	setup_rising to CP	0.0514	0.0298	0.0298	0.0298
RN ↓	min_pulse_width to RN	0.0566	0.0566	0.0566	0.0615
RN ↑	recovery_rising to CP	0.0151	0.0129	0.0129	0.0129
RN ↑	removal_rising to CP	-0.0098	-0.0029	-0.0029	-0.0029
TE ↓	hold_rising to CP	-0.0262	-0.0023	-0.0023	-0.0027
TE ↑	hold_rising to CP	-0.0311	-0.0196	-0.0196	-0.0196
TE ↓	setup_rising to CP	0.0635	0.0488	0.0488	0.0488
TE ↑	setup_rising to CP	0.1106	0.0862	0.0862	0.0862
TI ↓	hold_rising to CP	-0.0830	-0.0410	-0.0410	-0.0410
TI ↑	hold_rising to CP	-0.0364	-0.0205	-0.0205	-0.0205
TI ↓	setup_rising to CP	0.1176	0.0812	0.0812	0.0812
TI ↑	setup_rising to CP	0.0603	0.0443	0.0486	0.0486

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.329e-04	1.000e-20
X8_P10	1.369e-04	1.000e-20
X17_P10	1.670e-04	1.000e-20
X33_P10	2.184e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

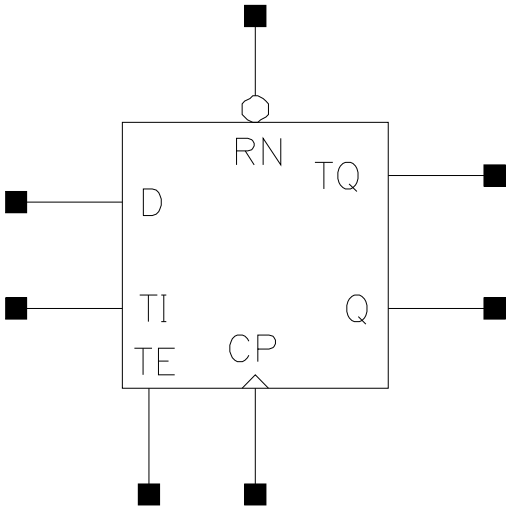
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.254e-02	1.265e-02	1.274e-02	1.279e-02
Clock 100Mhz Data 25Mhz	1.314e-02	1.301e-02	1.374e-02	1.541e-02
Clock 100Mhz Data 50Mhz	1.375e-02	1.337e-02	1.475e-02	1.804e-02
Clock = 0 Data 100Mhz	7.736e-03	7.036e-03	6.802e-03	6.685e-03
Clock = 1 Data 100Mhz	1.854e-03	9.527e-04	6.522e-04	5.022e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0008	0.0008	0.0008

RN	0.0010	0.0010	0.0009	0.0009
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0650	0.0363	3.7043	1.7143
CP to Q ↑	0.0546	0.0458	4.8251	2.4368
CP to TQ ↓	0.0599	0.0351	4.6272	4.0990
CP to TQ ↑	0.0566	0.0480	8.8388	8.0952
RN to Q ↓	0.0460	0.0519	3.3358	1.6724
RN to TQ ↓	0.0429	0.0511	4.2150	4.0135
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0520	0.0574	0.8232	0.4311
CP to Q ↑	0.0646	0.0688	1.1553	0.5892
CP to TQ ↓	0.0534	0.0595	3.9591	4.0303
CP to TQ ↑	0.0683	0.0750	7.9802	8.0147
RN to Q ↓	0.0623	0.0677	0.8226	0.4312
RN to TQ ↓	0.0636	0.0697	3.9605	4.0308

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0740	0.0708	0.0707	0.0707
CP ↑	min_pulse_width to CP	0.0565	0.0284	0.0237	0.0237
D ↓	hold_rising to CP	-0.0381	-0.0045	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0208	0.0009	-0.0023	-0.0023
D ↓	setup_rising to CP	0.0733	0.0445	0.0445	0.0445
D ↑	setup_rising to CP	0.0514	0.0298	0.0298	0.0298
RN ↓	min_pulse_width to RN	0.0566	0.0637	0.0496	0.0496
RN ↑	recovery_rising to CP	0.0125	0.0129	0.0129	0.0129
RN ↑	removal_rising to CP	-0.0078	-0.0029	-0.0029	-0.0029
TE ↓	hold_rising to CP	-0.0262	-0.0027	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0311	-0.0169	-0.0196	-0.0196
TE ↓	setup_rising to CP	0.0635	0.0488	0.0488	0.0488
TE ↑	setup_rising to CP	0.1106	0.0862	0.0862	0.0862
TI ↓	hold_rising to CP	-0.0830	-0.0410	-0.0410	-0.0410
TI ↑	hold_rising to CP	-0.0364	-0.0205	-0.0205	-0.0205
TI ↓	setup_rising to CP	0.1176	0.0812	0.0812	0.0812
TI ↑	setup_rising to CP	0.0603	0.0443	0.0443	0.0443

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.243e-04	1.000e-20
X8_P10	1.416e-04	1.000e-20
X17_P10	1.947e-04	1.000e-20
X33_P10	2.540e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

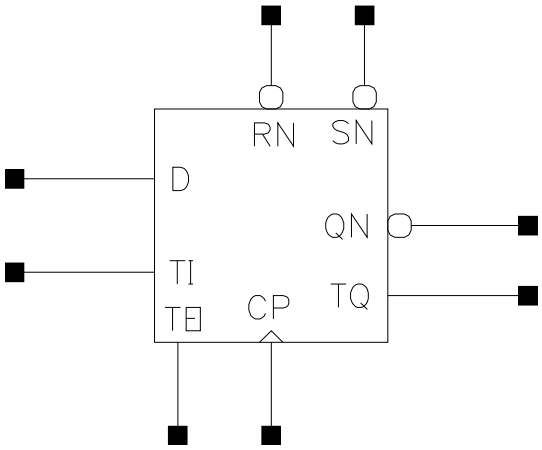
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.261e-02	1.269e-02	1.271e-02	1.272e-02
Clock 100Mhz Data 25Mhz	1.343e-02	1.313e-02	1.419e-02	1.565e-02
Clock 100Mhz Data 50Mhz	1.426e-02	1.358e-02	1.566e-02	1.857e-02
Clock = 0 Data 100Mhz	7.742e-03	7.040e-03	6.806e-03	6.690e-03
Clock = 1 Data 100Mhz	1.856e-03	9.536e-04	6.531e-04	5.029e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.352	5.2224
X17_P10	1.200	4.488	5.3856
X33_P10	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011
D	0.0007	0.0007	0.0007
RN	0.0010	0.0010	0.0010

SN	0.0015	0.0014	0.0014
TE	0.0012	0.0012	0.0012
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
CP to QN ↓	0.0616	0.0662	1.6171	0.8300
CP to QN ↑	0.0451	0.0479	2.2857	1.1583
CP to TQ ↓	0.0340	0.0339	4.8776	4.8824
CP to TQ ↑	0.0503	0.0503	10.1709	10.1819
RN to QN ↓	0.0558	0.0610	1.6219	0.8317
RN to QN ↑	0.0520	0.0544	2.2838	1.1580
RN to TQ ↓	0.0418	0.0418	4.8218	4.8234
RN to TQ ↑	0.0434	0.0432	10.2845	10.2938
SN to QN ↓	0.0599	0.0643	1.6190	0.8303
SN to TQ ↑	0.0490	0.0490	10.1583	10.1717
	X33_P10		X33_P10	
CP to QN ↓	0.0772		0.4382	
CP to QN ↑	0.0548		0.5933	
CP to TQ ↓	0.0340		4.8938	
CP to TQ ↑	0.0504		10.2057	
RN to QN ↓	0.0733		0.4384	
RN to QN ↑	0.0608		0.5937	
RN to TQ ↓	0.0419		4.8371	
RN to TQ ↑	0.0432		10.3441	
SN to QN ↓	0.0752		0.4392	
SN to TQ ↑	0.0491		10.1993	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0755	0.0755	0.0755
CP ↑	min_pulse_width to CP	0.0271	0.0271	0.0283
D ↓	hold_rising to CP	-0.0071	-0.0071	-0.0071
D ↑	hold_rising to CP	-0.0023	-0.0023	-0.0023
D ↓	setup_rising to CP	0.0493	0.0493	0.0493
D ↑	setup_rising to CP	0.0298	0.0298	0.0298
RN ↓	min_pulse_width to RN	0.0588	0.0615	0.0664
RN ↑	non_seq_hold_rising to SN	-0.0214	-0.0214	-0.0215
RN ↑	non_seq_setup_rising to SN	0.0523	0.0523	0.0523
RN ↑	recovery_rising to CP	0.0200	0.0200	0.0200
RN ↑	removal_rising to CP	-0.0119	-0.0119	-0.0119
SN ↓	min_pulse_width to SN	0.0527	0.0527	0.0576
SN ↑	recovery_rising to CP	0.0032	0.0032	0.0032
SN ↑	removal_rising to CP	0.0232	0.0232	0.0232

TE ↓	hold_rising to CP	-0.0049	-0.0049	-0.0049
TE ↑	hold_rising to CP	-0.0169	-0.0169	-0.0169
TE ↓	setup_rising to CP	0.0483	0.0483	0.0483
TE ↑	setup_rising to CP	0.0911	0.0911	0.0911
TI ↓	hold_rising to CP	-0.0426	-0.0426	-0.0426
TI ↑	hold_rising to CP	-0.0205	-0.0205	-0.0205
TI ↓	setup_rising to CP	0.0860	0.0860	0.0860
TI ↑	setup_rising to CP	0.0486	0.0486	0.0486

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	1.537e-04	1.000e-20
X17_P10	1.781e-04	1.000e-20
X33_P10	2.240e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

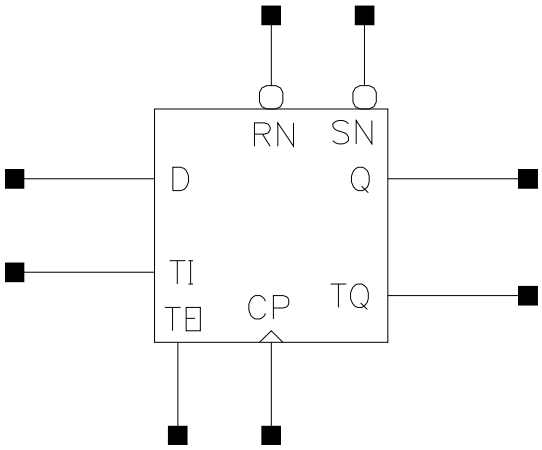
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.336e-02	1.336e-02	1.336e-02
Clock 100Mhz Data 25Mhz	1.353e-02	1.423e-02	1.626e-02
Clock 100Mhz Data 50Mhz	1.371e-02	1.510e-02	1.917e-02
Clock = 0 Data 100Mhz	6.506e-03	6.503e-03	6.504e-03
Clock = 1 Data 100Mhz	5.229e-05	5.243e-05	5.247e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.216	5.0592
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011
D	0.0007	0.0007	0.0007
RN	0.0010	0.0010	0.0010

SN	0.0015	0.0015	0.0015
TE	0.0012	0.0012	0.0012
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0391	0.0443	1.6646	0.8608
CP to Q ↑	0.0501	0.0538	2.3463	1.1954
CP to TQ ↓	0.0384	0.0432	4.9557	5.0244
CP to TQ ↑	0.0547	0.0609	9.9534	10.0321
RN to Q ↓	0.0450	0.0481	1.6223	0.8354
RN to Q ↑	0.0518	0.0544	2.3321	1.1859
RN to TQ ↓	0.0447	0.0476	4.8725	4.9129
RN to TQ ↑	0.0559	0.0604	9.9051	9.9755
SN to Q ↑	0.0483	0.0511	2.3354	1.1868
SN to TQ ↑	0.0522	0.0570	9.9271	9.9936
	X33_P10		**X33_P10**	
CP to Q ↓	0.0569		0.4590	
CP to Q ↑	0.0630		0.6202	
CP to TQ ↓	0.0519		5.2072	
CP to TQ ↑	0.0727		10.1609	
RN to Q ↓	0.0562		0.4416	
RN to Q ↑	0.0611		0.6119	
RN to TQ ↓	0.0530		5.0379	
RN to TQ ↑	0.0687		10.0895	
SN to Q ↑	0.0583		0.6124	
SN to TQ ↑	0.0657		10.1097	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0755	0.0755	0.0755
CP ↑	min_pulse_width to CP	0.0318	0.0365	0.0471
D ↓	hold_rising to CP	-0.0071	-0.0045	-0.0045
D ↑	hold_rising to CP	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0493	0.0493	0.0493
D ↑	setup_rising to CP	0.0298	0.0298	0.0298
RN ↓	min_pulse_width to RN	0.0713	0.0833	0.1077
RN ↑	non_seq_hold_rising to SN	-0.0236	-0.0335	-0.0432
RN ↑	non_seq_setup_rising to SN	0.0502	0.0525	0.0725
RN ↑	recovery_rising to CP	0.0174	0.0174	0.0174
RN ↑	removal_rising to CP	-0.0103	-0.0103	-0.0103
SN ↓	min_pulse_width to SN	0.0576	0.0674	0.0869
SN ↑	recovery_rising to CP	0.0032	0.0032	0.0032
SN ↑	removal_rising to CP	0.0232	0.0232	0.0264

TE ↓	hold_rising to CP	-0.0023	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0169	-0.0169	-0.0169
TE ↓	setup_rising to CP	0.0483	0.0483	0.0515
TE ↑	setup_rising to CP	0.0911	0.0911	0.0911
TI ↓	hold_rising to CP	-0.0426	-0.0426	-0.0426
TI ↑	hold_rising to CP	-0.0189	-0.0189	-0.0189
TI ↓	setup_rising to CP	0.0860	0.0860	0.0903
TI ↑	setup_rising to CP	0.0486	0.0486	0.0486

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P10	1.571e-04	1.000e-20
X17_P10	1.863e-04	1.000e-20
X33_P10	2.426e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

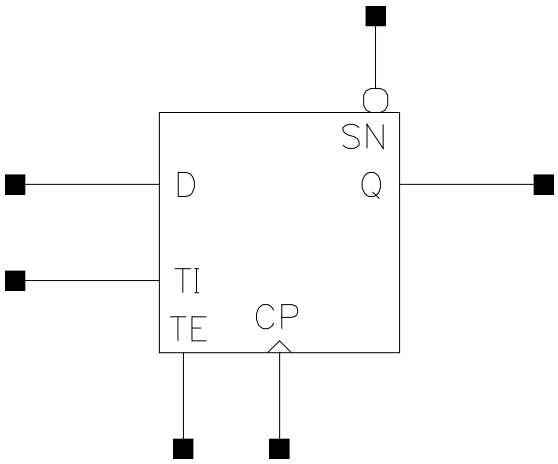
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.334e-02	1.334e-02	1.334e-02
Clock 100Mhz Data 25Mhz	1.358e-02	1.462e-02	1.754e-02
Clock 100Mhz Data 50Mhz	1.382e-02	1.590e-02	2.173e-02
Clock = 0 Data 100Mhz	6.500e-03	6.501e-03	6.501e-03
Clock = 1 Data 100Mhz	5.231e-05	5.227e-05	5.237e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0005	0.0005	0.0005
SN	0.0016	0.0016	0.0016	0.0016
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005
	X33_P10			

CP	0.0011			
D	0.0005			
SN	0.0016			
TE	0.0012			
TI	0.0005			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0573	0.0342	3.5396	1.6583
CP to Q ↑	0.0529	0.0457	4.6865	2.3385
SN to Q ↑	0.0348	0.0372	4.5606	2.3138
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
CP to Q ↓	0.0492	0.0520	0.8135	0.5618
CP to Q ↑	0.0640	0.0664	1.1489	0.7792
SN to Q ↑	0.0561	0.0585	1.1478	0.7794
	X33_P10		**X33_P10**	
CP to Q ↓	0.0543		0.4265	
CP to Q ↑	0.0681		0.5861	
SN to Q ↑	0.0602		0.5864	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.0787	0.0771	0.0771	0.0771
CP ↑	min_pulse_width to CP	0.0505	0.0271	0.0237	0.0237
D ↓	hold_rising to CP	-0.0409	-0.0098	-0.0098	-0.0098
D ↑	hold_rising to CP	-0.0218	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0755	0.0489	0.0489	0.0489
D ↑	setup_rising to CP	0.0456	0.0239	0.0239	0.0239
SN ↓	min_pulse_width to SN	0.0403	0.0452	0.0403	0.0403
SN ↑	recovery_rising to CP	0.0032	0.0032	0.0032	0.0032
SN ↑	removal_rising to CP	0.0189	0.0270	0.0270	0.0270
TE ↓	hold_rising to CP	-0.0289	-0.0044	-0.0044	-0.0044
TE ↑	hold_rising to CP	-0.0257	-0.0141	-0.0141	-0.0141
TE ↓	setup_rising to CP	0.0635	0.0489	0.0489	0.0489
TE ↑	setup_rising to CP	0.1155	0.0960	0.0960	0.0960
TI ↓	hold_rising to CP	-0.0863	-0.0475	-0.0475	-0.0475
TI ↑	hold_rising to CP	-0.0315	-0.0147	-0.0147	-0.0147
TI ↓	setup_rising to CP	0.1209	0.0919	0.0919	0.0919
TI ↑	setup_rising to CP	0.0612	0.0437	0.0437	0.0437
		X33_P10			

CP ↓	min_pulse_width to CP	0.0771			
CP ↑	min_pulse_width to CP	0.0237			
D ↓	hold_rising to CP	-0.0098			
D ↑	hold_rising to CP	0.0004			
D ↓	setup_rising to CP	0.0489			
D ↑	setup_rising to CP	0.0239			
SN ↓	min_pulse_width to SN	0.0403			
SN ↑	recovery_rising to CP	0.0032			
SN ↑	removal_rising to CP	0.0270			
TE ↓	hold_rising to CP	-0.0044			
TE ↑	hold_rising to CP	-0.0141			
TE ↓	setup_rising to CP	0.0489			
TE ↑	setup_rising to CP	0.0960			
TI ↓	hold_rising to CP	-0.0475			
TI ↑	hold_rising to CP	-0.0147			
TI ↓	setup_rising to CP	0.0919			
TI ↑	setup_rising to CP	0.0437			

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.145e-04	1.000e-20
X8_P10	1.337e-04	1.000e-20
X17_P10	1.870e-04	1.000e-20
X25_P10	2.081e-04	1.000e-20
X33_P10	2.291e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	1.233e-02	1.261e-02	1.270e-02	1.275e-02
Clock 100Mhz Data 25Mhz	1.276e-02	1.286e-02	1.387e-02	1.456e-02
Clock 100Mhz Data 50Mhz	1.320e-02	1.311e-02	1.504e-02	1.637e-02
Clock = 0 Data 100Mhz	7.374e-03	6.883e-03	6.720e-03	6.639e-03
Clock = 1 Data 100Mhz	1.855e-03	9.533e-04	6.529e-04	5.025e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	1.278e-02			

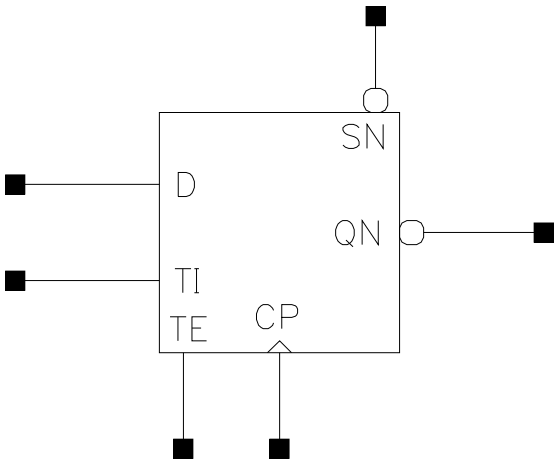
Clock 100Mhz Data 25Mhz	1.525e-02			
Clock 100Mhz Data 50Mhz	1.773e-02			
Clock = 0 Data 100Mhz	6.590e-03			
Clock = 1 Data 100Mhz	4.125e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0005	0.0005	0.0005
SN	0.0016	0.0016	0.0016	0.0016
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005
	X33_P10			

CP	0.0011			
D	0.0005			
SN	0.0016			
TE	0.0012			
TI	0.0005			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0587	0.0540	3.0218	1.5904
CP to QN ↑	0.0588	0.0394	4.5119	2.2822
SN to QN ↓	0.0424	0.0460	3.0179	1.5908
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
CP to QN ↓	0.0571	0.0605	0.8157	0.5629
CP to QN ↑	0.0463	0.0493	1.1484	0.7802
SN to QN ↓	0.0475	0.0508	0.8137	0.5621
	X33_P10		**X33_P10**	
CP to QN ↓	0.0634		0.4269	
CP to QN ↑	0.0517		0.5872	
SN to QN ↓	0.0534		0.4266	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.0770	0.0771	0.0771	0.0771
CP ↑	min_pulse_width to CP	0.0377	0.0237	0.0271	0.0271
D ↓	hold_rising to CP	-0.0409	-0.0098	-0.0098	-0.0098
D ↑	hold_rising to CP	-0.0218	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0755	0.0489	0.0489	0.0489
D ↑	setup_rising to CP	0.0456	0.0239	0.0239	0.0239
SN ↓	min_pulse_width to SN	0.0354	0.0403	0.0452	0.0452
SN ↑	recovery_rising to CP	0.0032	0.0032	0.0032	0.0032
SN ↑	removal_rising to CP	0.0189	0.0238	0.0270	0.0270
TE ↓	hold_rising to CP	-0.0289	-0.0044	-0.0044	-0.0044
TE ↑	hold_rising to CP	-0.0257	-0.0141	-0.0141	-0.0141
TE ↓	setup_rising to CP	0.0635	0.0489	0.0489	0.0489
TE ↑	setup_rising to CP	0.1155	0.0960	0.0960	0.0960
TI ↓	hold_rising to CP	-0.0863	-0.0475	-0.0475	-0.0475
TI ↑	hold_rising to CP	-0.0315	-0.0147	-0.0147	-0.0147
TI ↓	setup_rising to CP	0.1209	0.0919	0.0919	0.0919
TI ↑	setup_rising to CP	0.0612	0.0437	0.0437	0.0437
		X33_P10			

CP ↓	min_pulse_width to CP	0.0771			
CP ↑	min_pulse_width to CP	0.0284			
D ↓	hold_rising to CP	-0.0098			
D ↑	hold_rising to CP	0.0004			
D ↓	setup_rising to CP	0.0489			
D ↑	setup_rising to CP	0.0239			
SN ↓	min_pulse_width to SN	0.0452			
SN ↑	recovery_rising to CP	0.0032			
SN ↑	removal_rising to CP	0.0270			
TE ↓	hold_rising to CP	-0.0044			
TE ↑	hold_rising to CP	-0.0141			
TE ↓	setup_rising to CP	0.0489			
TE ↑	setup_rising to CP	0.0960			
TI ↓	hold_rising to CP	-0.0475			
TI ↑	hold_rising to CP	-0.0147			
TI ↓	setup_rising to CP	0.0919			
TI ↑	setup_rising to CP	0.0437			

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.158e-04	1.000e-20
X8_P10	1.407e-04	1.000e-20
X17_P10	1.949e-04	1.000e-20
X25_P10	2.245e-04	1.000e-20
X33_P10	2.542e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	1.233e-02	1.263e-02	1.271e-02	1.276e-02
Clock 100Mhz Data 25Mhz	1.239e-02	1.268e-02	1.405e-02	1.478e-02
Clock 100Mhz Data 50Mhz	1.245e-02	1.274e-02	1.538e-02	1.679e-02
Clock = 0 Data 100Mhz	7.376e-03	6.888e-03	6.723e-03	6.641e-03
Clock = 1 Data 100Mhz	1.855e-03	9.532e-04	6.528e-04	5.025e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	1.279e-02			

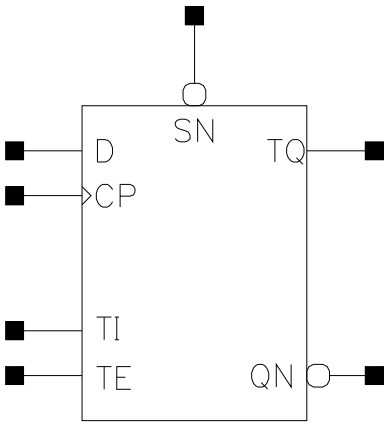
Clock 100Mhz Data 25Mhz	1.553e-02			
Clock 100Mhz Data 50Mhz	1.828e-02			
Clock = 0 Data 100Mhz	6.592e-03			
Clock = 1 Data 100Mhz	4.125e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.216	5.0592
X8_P10	1.200	4.080	4.8960
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0005	0.0005	0.0005

SN	0.0017	0.0018	0.0017	0.0017
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0675	0.0565	3.0230	1.5989
CP to QN ↑	0.0755	0.0444	4.4541	2.3241
CP to TQ ↓	0.0544	0.0300	4.2029	3.6407
CP to TQ ↑	0.0523	0.0424	6.0533	5.8918
SN to QN ↓	0.0458	0.0477	3.0199	1.5956
SN to TQ ↑	0.0322	0.0333	5.9474	5.8994
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0572	0.0635	0.8375	0.4232
CP to QN ↑	0.0499	0.0556	1.1594	0.5911
CP to TQ ↓	0.0368	0.0367	3.7714	3.7713
CP to TQ ↑	0.0480	0.0480	5.9632	5.9738
SN to QN ↓	0.0499	0.0560	0.8365	0.4227
SN to TQ ↑	0.0406	0.0405	5.9375	5.9517

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0787	0.0771	0.0788	0.0788
CP ↑	min_pulse_width to CP	0.0518	0.0236	0.0284	0.0318
D ↓	hold_rising to CP	-0.0409	-0.0098	-0.0098	-0.0098
D ↑	hold_rising to CP	-0.0218	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0755	0.0489	0.0489	0.0489
D ↑	setup_rising to CP	0.0456	0.0239	0.0239	0.0239
SN ↓	min_pulse_width to SN	0.0332	0.0354	0.0381	0.0381
SN ↑	recovery_rising to CP	0.0032	0.0032	0.0032	0.0032
SN ↑	removal_rising to CP	0.0189	0.0238	0.0238	0.0238
TE ↓	hold_rising to CP	-0.0289	-0.0044	-0.0044	-0.0044
TE ↑	hold_rising to CP	-0.0257	-0.0141	-0.0141	-0.0141
TE ↓	setup_rising to CP	0.0635	0.0489	0.0489	0.0489
TE ↑	setup_rising to CP	0.1155	0.0960	0.0960	0.0960
TI ↓	hold_rising to CP	-0.0820	-0.0475	-0.0475	-0.0475
TI ↑	hold_rising to CP	-0.0315	-0.0147	-0.0154	-0.0154
TI ↓	setup_rising to CP	0.1209	0.0919	0.0919	0.0919
TI ↑	setup_rising to CP	0.0612	0.0437	0.0437	0.0437

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.314e-04	1.000e-20
X8_P10	1.560e-04	1.000e-20
X17_P10	2.102e-04	1.000e-20
X33_P10	2.694e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

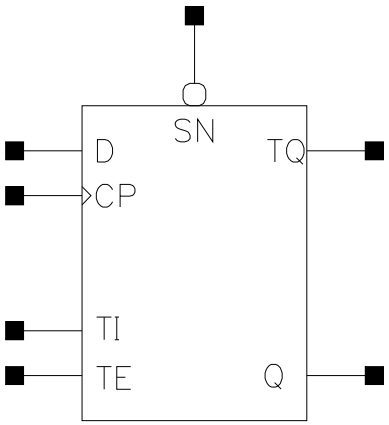
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.234e-02	1.262e-02	1.272e-02	1.276e-02
Clock 100Mhz Data 25Mhz	1.305e-02	1.306e-02	1.440e-02	1.586e-02
Clock 100Mhz Data 50Mhz	1.376e-02	1.350e-02	1.609e-02	1.895e-02
Clock = 0 Data 100Mhz	7.387e-03	6.896e-03	6.732e-03	6.651e-03
Clock = 1 Data 100Mhz	1.855e-03	9.535e-04	6.530e-04	5.029e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.944	4.7328
X17_P10	1.200	4.216	5.0592
X33_P10	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0011	0.0011	0.0011	0.0011
D	0.0010	0.0005	0.0005	0.0005

SN	0.0018	0.0016	0.0016	0.0016
TE	0.0009	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0657	0.0371	3.6160	1.6880
CP to Q ↑	0.0566	0.0478	4.7024	2.3684
CP to TQ ↓	0.0652	0.0367	5.2007	4.1167
CP to TQ ↑	0.0555	0.0521	6.1008	8.1811
SN to Q ↑	0.0349	0.0386	4.5756	2.3398
SN to TQ ↑	0.0340	0.0419	5.9666	8.1356
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0506	0.0557	0.8336	0.4335
CP to Q ↑	0.0652	0.0691	1.1555	0.5885
CP to TQ ↓	0.0519	0.0578	3.9587	4.0192
CP to TQ ↑	0.0691	0.0754	7.9862	8.0222
SN to Q ↑	0.0573	0.0613	1.1547	0.5892
SN to TQ ↑	0.0612	0.0675	7.9829	8.0231

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0787	0.0771	0.0771	0.0771
CP ↑	min_pulse_width to CP	0.0599	0.0284	0.0237	0.0237
D ↓	hold_rising to CP	-0.0409	-0.0098	-0.0098	-0.0098
D ↑	hold_rising to CP	-0.0218	0.0004	0.0004	0.0004
D ↓	setup_rising to CP	0.0755	0.0489	0.0489	0.0489
D ↑	setup_rising to CP	0.0456	0.0239	0.0239	0.0239
SN ↓	min_pulse_width to SN	0.0332	0.0500	0.0403	0.0403
SN ↑	recovery_rising to CP	0.0032	0.0032	0.0032	0.0032
SN ↑	removal_rising to CP	0.0189	0.0270	0.0270	0.0270
TE ↓	hold_rising to CP	-0.0289	-0.0044	-0.0044	-0.0044
TE ↑	hold_rising to CP	-0.0257	-0.0141	-0.0141	-0.0141
TE ↓	setup_rising to CP	0.0635	0.0489	0.0489	0.0489
TE ↑	setup_rising to CP	0.1155	0.0960	0.0960	0.0960
TI ↓	hold_rising to CP	-0.0863	-0.0475	-0.0475	-0.0475
TI ↑	hold_rising to CP	-0.0315	-0.0147	-0.0147	-0.0147
TI ↓	setup_rising to CP	0.1225	0.0919	0.0919	0.0919
TI ↑	setup_rising to CP	0.0612	0.0437	0.0437	0.0437

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	1.277e-04	1.000e-20
X8_P10	1.395e-04	1.000e-20
X17_P10	1.922e-04	1.000e-20
X33_P10	2.342e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

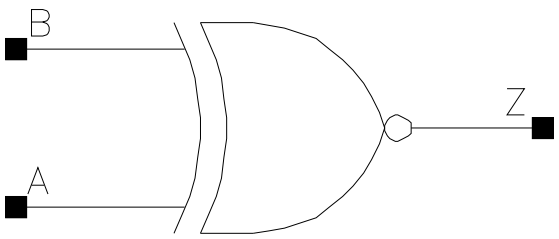
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	1.233e-02	1.261e-02	1.270e-02	1.275e-02
Clock 100Mhz Data 25Mhz	1.331e-02	1.323e-02	1.419e-02	1.566e-02
Clock 100Mhz Data 50Mhz	1.429e-02	1.386e-02	1.568e-02	1.856e-02
Clock = 0 Data 100Mhz	7.388e-03	6.891e-03	6.726e-03	6.643e-03
Clock = 1 Data 100Mhz	1.855e-03	9.535e-04	6.531e-04	5.030e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P10	X8_P10	X17_P10	X25_P10
A	0.0019	0.0008	0.0011	0.0017
B	0.0017	0.0016	0.0021	0.0029
	X33_P10			
A	0.0020			
B	0.0034			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X8_P10**	**X6_P10**	**X8_P10**
A to Z ↓	0.0166	0.0359	2.8207	1.7162
A to Z ↑	0.0167	0.0335	3.3960	2.4108
B to Z ↓	0.0154	0.0248	2.8189	1.7027
B to Z ↑	0.0178	0.0239	3.4044	2.4035
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
A to Z ↓	0.0349	0.0353	0.8430	0.5786
A to Z ↑	0.0315	0.0316	1.1828	0.7873

B to Z ↓	0.0259	0.0251	0.8399	0.5771
B to Z ↑	0.0245	0.0235	1.1804	0.7852
	X33_P10		**X33_P10**	
A to Z ↓	0.0340		0.4342	
A to Z ↑	0.0310		0.5922	
B to Z ↓	0.0244		0.4330	
B to Z ↑	0.0236		0.5908	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P10	7.805e-05	1.000e-20
X8_P10	8.766e-05	1.000e-20
X17_P10	1.517e-04	1.000e-20
X25_P10	2.353e-04	1.000e-20
X33_P10	3.284e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	4.132e-03	7.695e-03	1.186e-02	1.868e-02
B to Z	4.024e-03	5.700e-03	9.611e-03	1.480e-02
	X33_P10			
A to Z	2.333e-02			
B to Z	1.907e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

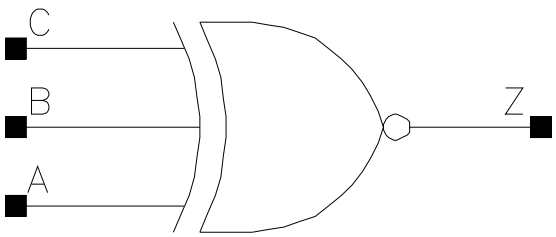
Pin Cycle (vdds)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P10			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	2.176	2.6112
X16_P10	1.200	2.720	3.2640
X25_P10	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X16_P10	X25_P10
A	0.0033	0.0027	0.0034	0.0050
B	0.0036	0.0025	0.0033	0.0046
C	0.0023	0.0008	0.0008	0.0009

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0248	0.0410	3.2917	1.8016
A to Z ↑	0.0235	0.0381	4.6413	2.3877
B to Z ↓	0.0259	0.0415	3.2950	1.8016
B to Z ↑	0.0241	0.0389	4.6420	2.3876
C to Z ↓	0.0259	0.0561	3.3032	1.8013
C to Z ↑	0.0236	0.0530	4.6462	2.3865
	X16_P10	**X25_P10**	**X16_P10**	**X25_P10**
A to Z ↓	0.0419	0.0421	0.9249	0.5906
A to Z ↑	0.0418	0.0417	1.2503	0.7895
B to Z ↓	0.0427	0.0434	0.9249	0.5909

B to Z ↑	0.0425	0.0431	1.2499	0.7898
C to Z ↓	0.0603	0.0646	0.9246	0.5906
C to Z ↑	0.0595	0.0639	1.2508	0.7895

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	7.956e-05	1.000e-20
X8_P10	8.096e-05	1.000e-20
X16_P10	1.386e-04	1.000e-20
X25_P10	2.013e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	4.212e-03	6.084e-03	1.038e-02	1.591e-02
B to Z	4.297e-03	6.062e-03	1.043e-02	1.604e-02
C to Z	4.268e-03	8.997e-03	1.392e-02	2.114e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

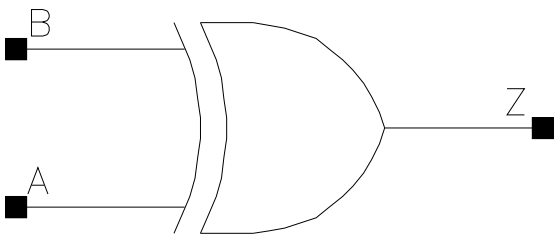
Pin Cycle (vdds)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.224	1.4688
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.224	1.4688
X16_P10	1.200	1.360	1.6320
X25_P10	1.200	2.176	2.6112
X31_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X16_P10
A	0.0009	0.0018	0.0011	0.0013
B	0.0014	0.0016	0.0017	0.0019
	X25_P10	X31_P10		
A	0.0017	0.0023		
B	0.0030	0.0038		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0320	0.0156	3.0744	2.2159
A to Z ↑	0.0312	0.0178	4.4420	4.1551
B to Z ↓	0.0231	0.0167	3.0531	2.2321
B to Z ↑	0.0234	0.0164	4.4328	4.1522
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0295	0.0312	1.6845	0.8684

A to Z ↑	0.0275	0.0295	2.3475	1.1840
B to Z ↓	0.0227	0.0239	1.6786	0.8658
B to Z ↑	0.0218	0.0235	2.3457	1.1821
	X25_P10	**X31_P10**	**X25_P10**	**X31_P10**
A to Z ↓	0.0329	0.0314	0.5749	0.4605
A to Z ↑	0.0308	0.0297	0.7852	0.6328
B to Z ↓	0.0246	0.0233	0.5744	0.4599
B to Z ↑	0.0233	0.0226	0.7850	0.6324

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	7.057e-05	1.000e-20
X6_P10	7.310e-05	1.000e-20
X8_P10	1.129e-04	1.000e-20
X16_P10	1.749e-04	1.000e-20
X25_P10	2.330e-04	1.000e-20
X31_P10	3.262e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	5.654e-03	4.100e-03	7.231e-03	1.104e-02
B to Z	4.560e-03	3.938e-03	6.196e-03	9.508e-03
	X25_P10	X31_P10		
A to Z	1.754e-02	2.181e-02		
B to Z	1.389e-02	1.737e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

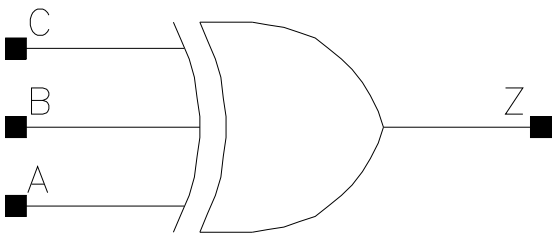
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P10	X31_P10		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X24_P10	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X24_P10
A	0.0028	0.0027	0.0034	0.0060
B	0.0028	0.0025	0.0031	0.0050
C	0.0009	0.0018	0.0025	0.0038

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0251	0.0410	3.4693	1.8010
A to Z ↑	0.0238	0.0381	5.0769	2.3854
B to Z ↓	0.0258	0.0416	3.4728	1.8014
B to Z ↑	0.0243	0.0389	5.0763	2.3866
C to Z ↓	0.0452	0.0410	3.4512	1.8016
C to Z ↑	0.0439	0.0382	5.0558	2.3854
	X17_P10	**X24_P10**	**X17_P10**	**X24_P10**
A to Z ↓	0.0386	0.0451	0.8631	0.6197
A to Z ↑	0.0387	0.0348	1.1639	0.7920
B to Z ↓	0.0392	0.0457	0.8633	0.6195

B to Z ↑	0.0393	0.0353	1.1645	0.7924
C to Z ↓	0.0390	0.0449	0.8636	0.6199
C to Z ↑	0.0392	0.0354	1.1651	0.7926

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	8.648e-05	1.000e-20
X8_P10	6.894e-05	1.000e-20
X17_P10	1.332e-04	1.000e-20
X24_P10	2.056e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	4.002e-03	6.082e-03	1.011e-02	1.682e-02
B to Z	4.073e-03	6.059e-03	1.013e-02	1.683e-02
C to Z	7.936e-03	6.000e-03	1.014e-02	1.685e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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