



Layout Finishing and SoC Tiling: BE tiling



December 11th, 2012

CMOS and derivative PDK



Program Management & Services / Process Design Kit

Company Confidential

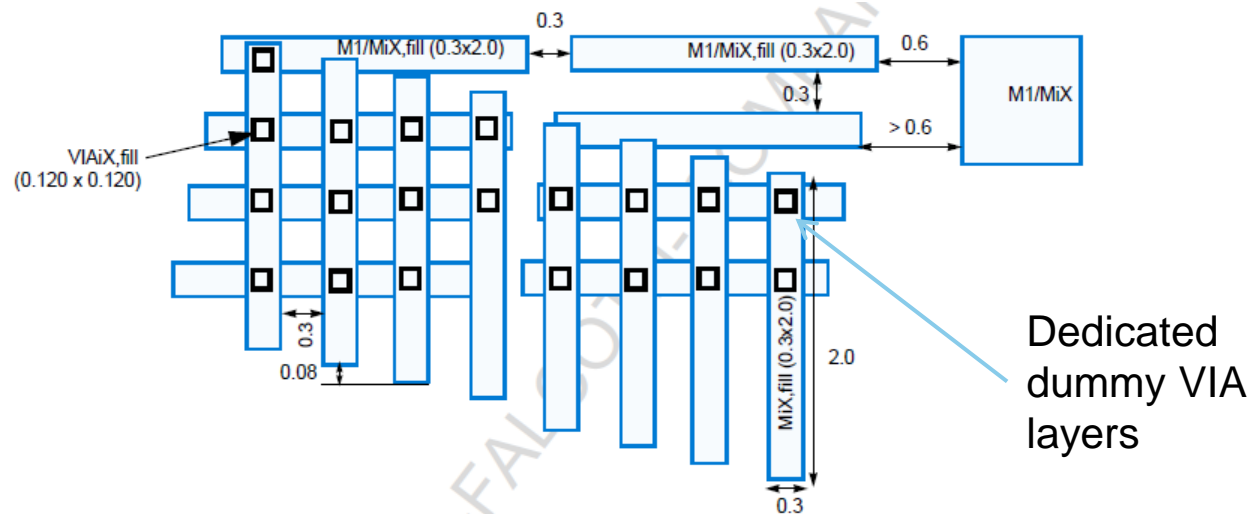


VIA-Tiling Implementation

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Metal Via-Tiling has been added in several technologies (H9A, 55/65nm, 40/45nm, 28/32nm) in order to reinforce the Flip Chip / Bumping pads robustness and so IC/circuit package-qualification.

- Via;fill are added only in the (ultra)low-K metals (M1/Mx : thin metals)
- The density on a common layer level rises from 20% to 43%
 - it brought concerns regarding impact on electrical performances, but it seems spaces are big enough : no negative feedback since 2010
 - metal fill uniformity appears to be also important : via matrix only would have lower mechanical resistance (metal stripes are required)



2

BE tiler passes

3

- Please refer to DRM (provided within DKs) to get accurate definition of tiler passes. They come along with targets to be reached:

1. Via tiling
 - tile both metal stripes and via;fill between them
 - tile with 65% as target, but do not violate max density
2. Metal;fill (squares)
 - tile with 45% as target, but do not violate max density
3. Metal;fillOPC (stripes)
 - tile with 45% as target, but do not violate max density

Tiler GUI

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The screenshot shows the Tiler GUI with the following sections and options:

- Back End layers tiling** (YES button)
 - ☒ Enable tiling for M1
 - ☒ Enable tiling for M2
 - ☒ Enable tiling for M3
 - ☒ Enable tiling for M4
 - ☒ Enable tiling for M5
 - ☒ Enable tiling for M6
 - ☒ Enable tiling for B1
 - ☒ Enable tiling for B2
 - ☒ Enable tiling for IA
 - ☒ Enable tiling for IB
- Enable tiling with squares** (checked)
- Enable tiling with stretchfill shapes** (unchecked)
- Enable tiling with fillOPC shapes** (checked)
- Enable tiling to achieve Gradient density constraints. Increases runtime (may be disabled on smooth chips facing no density gradient DRC violation)** (checked)
- Enable tiling for LB** (checked)
- Via tiling (mandatory when flipchip pads are used)** (YES button)
 - ☒ Enable tiling for V1
 - ☒ Enable tiling for V2
 - ☒ Enable tiling for V3
 - ☒ Enable tiling for V4
 - ☒ Enable tiling for V5
 - ☒ Enable tiling for W0
 - ☒ Enable tiling for W1
- Main routing direction (M1)** (HORIZ button)
- ☐ Run Via Tiling on tiles present in initial input GDS

metals

shapes

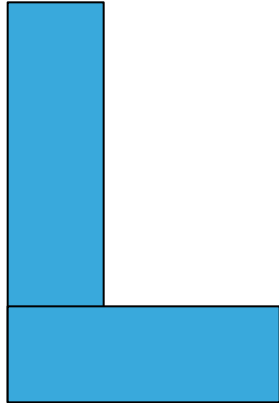
gradient (runtime)
RDL L-shapes

Via tiling (pre-requires
metals tiling to be enabled)

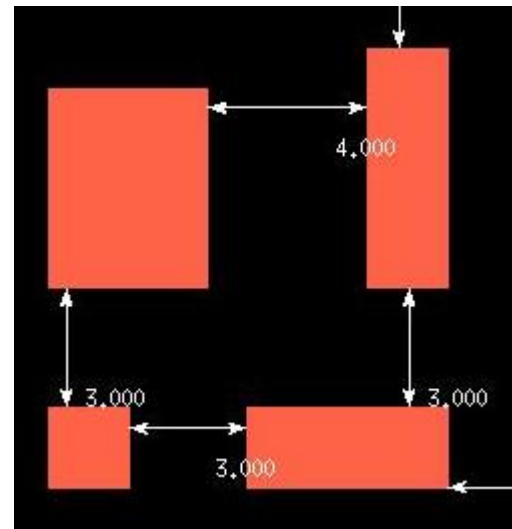
Routing direction

Via tiling to include
pre-existing metal;fill

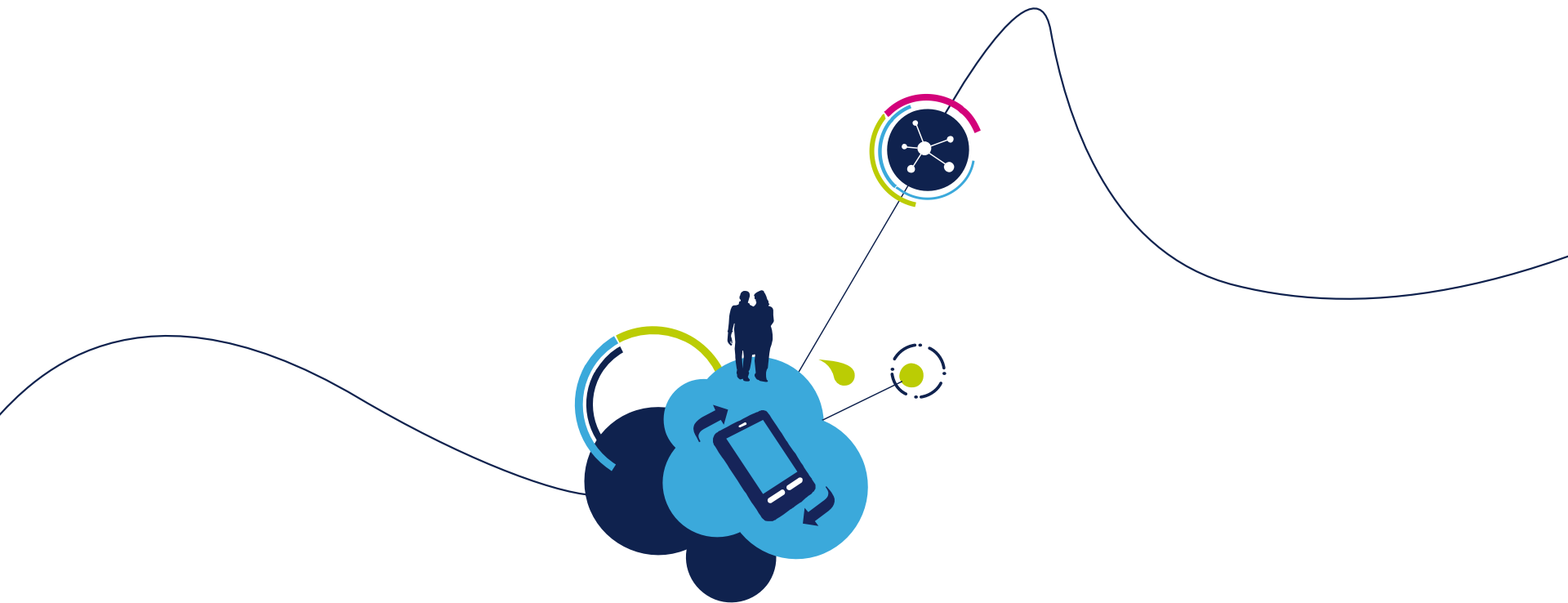
- The last level, usually Alucap, is tiled with specific shapes, named L-shapes
- They are designed to allow the FIB team to calibrate their optical tool
- The new shape takes into account extra DFM constraints in recent processes



Current shape



Future shape



Thank You