

C28SOI_IO_EXT_ALLF_DIGNEG_LR_EG_6U1X2T8XLB Release Notes and Known Problems and Solutions

1. Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library Name	C28SOI_IO_EXT_ALLF_DIGNEG_LR_EG_6U1X2T8XLB
Library Version	7.0
Library Type	IO Cells
Technology	CMOS028_FDSOI
DK Version	DK_cmos28FDSOI_RF_6U1x_2T8x_LB 2.9-38

1.2 Impact of Product Release

For latest information, please refer to LYS (http://col2.cro.st.com/libyield).

1.3 Related Documentation

- C28SOI_IO_EXT_ALLF_DIGNEG_LR_EG_7.0 User Manual
- C28SOI_IO_EXT_ALLF_DIGNEG_LR_EG_7.0 Release Notes and Known Problems and Solutions
- C28SOI_IO_EXT_ALLF_DIGNEG_LR_EG_7.0 HDL MODELS model usage guidelines
- C28SOI_IO_EXT_ALLF_DIGNEG_LR_EG_ff28_1.10V_1.95V_m40C_tt28_1.00V_1.80V_25C_ss28_0.90V_1.65V_-125C_7.0 DataBook
- C28SOI_IO_EXT_ALLF_DIGNEG_LR_EG_ff28_1.10V_1.95V_125C_ss28_0.90V_1.65V_m40C_7.0 DataBook



2. Changes with respect to all Previous Versions

2.1 Version 7.0-00

- A. This is the Final release.
- B. This package contains mainly,
- (1) Verilog Models:
- a. Verilog (.v) model : Compliance with power aware flow , Allpins, Emul, Tetramx and Formality verilog views
 - (2) Liberty NLDM (STF) for 137 Corners aligned with DP2.5:
 - I. STF view is compliance with UPF flow.
- (3) Physical : CADENCE LEF, CPF, SIP, SYNOPSYS FRAM and LAYOUT, GDS, CDL and CDSOA.
 - (4) Other: Voltus, doc file.
- C. Since there are no waiver present in this library so we are not supporting CCK waiver file.

First release



3. Known Problems and Solutions of this release



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KPS: Known Problems and Solutions:

DRC errors

- cell level

ERROR: Rule EMET.DEN.1 ERROR: Rule EMET.DEN.2 ERROR: Rule EMET.DEN.3 ERROR: Rule EMET.DEN.4 ERROR: Rule EMET.DEN.5 ERROR: Rule EMET.DEN.6 ERROR: Rule EMET.DEN.7 ERROR: Rule EMET.DEN.8 ERROR: Rule EMET.DEN.9 ERROR: Rule EMET.DEN.10 ERROR: Rule EMET.DEN.11 ERROR: Rule EMET.DEN.12 ERROR: Rule B1.DEN.1 ERROR: Rule B2.DEN.1 ERROR: Rule IA.DEN.1 ERROR: Rule IB.DEN.1

ERROR: Rule M6.DEN.1



LVS errors

- cell level

OK

- chip level



OK[We have to include the option in lvs_option->include for all FRAMECELL which
is used as rail(without any IP)]
eg : LVS FILTER "cell name" OPEN

ERC

- cell level

ERC1a

- chip level

ERC1a



4. Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact HELPDESK (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.





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