C28SOI_SC_12_CLK_LR

Release Notes and Known Problems and Solutions

12 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

1 Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library name	C28SOI_SC_12_CLK_LR
Library version	5.1
Library type	Standard Cells
Technology	CMOS028_FDSOI

1.2 Related Documentation

- StandardCell_Notes.pdf Present in Design Package
- User Manual C28SOI_SC_12_CLK_LR_um.pdf present in doc directory of Product itself.
- Datasheets C28SOI_SC_12_CLK_LR_*_ds.pdf present in doc directory of Product itself.

2 Release Details

2.1 Current Release Details, Version 5.1-05

- In previous versions 5.1-<xx>, associated with Main version 5.1, there was an issue with tags in GDS. Version and _Serial fields in tags were not good. In this release, tags in GDS has been corrected. Only change is in tags, otherwise GDS is fully backward compatible.

2.2 Version 5.1

- Dummy Poly in layout across various cells has been cut for DFM robustness.
- Total 80 cells have been updated for Robustness relative to contact punch through effect. Minimum Enclosure of 20nm for RX/CA has been ensured. There is no change in Cell Area and Abstract. Also Timing data and Footprint information in libs remains unchanged.
  - Updated cells are (including all PolyBias : P0, P4,P10, P16) -

C12T28SOIDV_LR_CNGFMUX21X30_P*	C12T28SOI_LR_CNAND3X25_P*
C12T28SOI_LR_CNBFX30_P*	C12T28SOI_LR_CNBFX59_P*
C12T28SOI_LR_CNBFX94_P*	C12T28SOI_LR_CNIVX16_P*
C12T28SOI_LR_CNNOR2AX15_P*	C12T28SOI_LR_CNOR2X15_P*
C12T28SOI_LR_CNOR3X20_P*	C12T28SOI_LR_DLYHFM8X54_P*
C12T28SOI_LRP_CNHLSX15_P*	C12T28SOI_LRP_CNHLSX22_P*
C12T28SOI_LRP_CNHLSX29_P*	C12T28SOI_LRP_CNHLSX51_P*
C12T28SOI_LRP_CNHLSX58_P*	C12T28SOI_LRP_CNHLSX71_P*
C12T28SOI_LRP_CNHLSX7_P*	C12T28SOI_LRP_CNHLSX93_P*
C12T28SOI_LRPHP_CNHLSX36_P*	C12T28SOIDV_LR_CNMUX41X17_P*

- To enable support for Cadence Voltus Flow, CCS-Power has been added.
- LVF support has been added.
- Cells has been characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.
- The product has been aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Global Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.3 Version 4.1

- Cells with PolyBias PBP16 (Poly Biased by 16 nm) have been added.
- C12T28SOIDV_LR_CNMUX41X17_P* cells have been updated due to change in DRM Rule V1_GR_553q1 at periphery to ensure clean abutment.
- The product is aligned to DP28FDSOI 2.4.

2.4 Version 4.0

- Total 9 cells have been added to further enrich the offer.
  - Balanced AND-OR Boolean Function
    - C12T28SOI_LR_CNAO12X33_P*
  - Balanced LATCH cells
    - C12T28SOI_LR_CNLDLRQX33_P*
  - High Drive DLY cells
    - C12T28SOI_LR_DLYHFM8X54_P*
- For EMG protection, In High Drive cells, routing on thin (comb) part of fatpin was blocked through Route Guide in Milkyway and obstruction in cadence LEF. In previous Library version, the pin shape was removed under obstruction from CADENCE LEF when there was an obstruction overlapping a pin. But with this method, PnR tool was not able to correctly understand the shape of pin. Therefore LEF generation algorithm has been updated not to delete obstruction under pin shape but rather to have the obstruction with "SPACING 0.0" (equivalent to zero-min-spacing route guide for FRAM). Due to this Algorithm Update, CADENCE LEF is changed).
- The product has been aligned to DP28FDSOI 2.4 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.5 Version 3.0

- Cells have been updated to have better design manufacturability, but for few cells, there is change in Abstract and Cell Area. Details are as below -

  - Cells with Change in Abstract (147 cells including all PolyBias : P0, P4,P10)

C12T28SOIDV_LR_CNGFMUX21X30_P*	C12T28SOIDV_LR_CNMUX41X27_P*
C12T28SOIDV_LR_SDFSYNCPRQX8_P*	C12T28SOIDV_LR_SDFSYNCPSQX8_P*
C12T28SOI_LR_CNAND3X25_P*	C12T28SOI_LR_CNAND3X33_P*
C12T28SOI_LR_CNBFX133_P*	C12T28SOI_LR_CNBFX38_P*
C12T28SOI_LR_CNBFX44_P*	C12T28SOI_LR_CNBFX52_P*
C12T28SOI_LR_CNBFX59_P*	C12T28SOI_LR_CNBFX70_P*
C12T28SOI_LR_CNBFX94_P*	C12T28SOI_LR_CNIVX133_P*
C12T28SOI_LR_CNIVX39_P*	C12T28SOI_LR_CNIVX47_P*
C12T28SOI_LR_CNIVX55_P*	C12T28SOI_LR_CNIVX61_P*
C12T28SOI_LR_CNIVX70_P*	C12T28SOI_LR_CNIVX94_P*
C12T28SOI_LR_CNNAND2AX27_P*	C12T28SOI_LR_CNNOR2AX27_P*
C12T28SOI_LR_CNOR2X37_P*	C12T28SOI_LR_CNOR3X14_P*
C12T28SOI_LR_CNOR3X20_P*	C12T28SOI_LR_CNOR3X27_P*
C12T28SOI_LR_CNOR4X20_P*	C12T28SOI_LR_CNOR4X27_P*
C12T28SOI_LR_CNSDFPRQTX15_P*	C12T28SOI_LR_CNSDFPSQTX15_P*

C12T28SOI_LR_CNXOR2X27_P*	C12T28SOI_LR_DLYHFM4X15_P*
C12T28SOI_LR_DLYHFM4X7_P*	C12T28SOI_LR_DLYHFM8X15_P*
C12T28SOI_LR_DLYHFM8X7_P*	C12T28SOI_LRP_CNHLSX15_P*
C12T28SOI_LRP_CNHLSX22_P*	C12T28SOI_LRP_CNHLSX29_P*
C12T28SOI_LRP_CNHLSX36_P*	C12T28SOI_LRP_CNHLSX51_P*
C12T28SOI_LRP_CNHLSX58_P*	C12T28SOI_LRP_CNHLSX71_P*
C12T28SOI_LRP_CNHLSX93_P*	C12T28SOI_LRPHP_CNHLSX36_P*
C12T28SOI_LRPHP_CNHLSX44_P*	C12T28SOI_LRPHP_CNHLSX51_P*
C12T28SOI_LRPHP_CNHLSX58_P*	C12T28SOI_LRPHP_CNHLSX71_P*
C12T28SOI_LRPHP_CNHLSX86_P*	

– Cells with Change in Area(9 cells including all PolyBias : P0, P4,P10)

C12T28SOI_LR_CNOR4X20_P*	C12T28SOI_LR_DLYHFM4X15_P*
C12T28SOI_LR_DLYHFM8X15_P*	

- For Tau Information on Metastable Flops (SDFSYNCP*), refer to Tau_Info.csv provided in doc directory of product itself.
- The product is aligned to DP28FDSOI 2.3 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.6 Version 2.1

- 18 new Cells have been added (All PolyBias : P0, P4,P10)

  – Higher Drive combinational cells (X27 Drive)
    - C12T28SOI_LR_CNNAND2AX27_P*
    - C12T28SOI_LR_CNNOR2AX27_P*
    - C12T28SOI_LR_CNOR3X27_P*
    - C12T28SOI_LR_CNOR4X27_P*
    - C12T28SOI_LR_CNXOR2X27_P*
    - C12T28SOIDV_LR_CNMUX41X27_P*

- Tau_Info.csv has been added to have Tau Information for Balanced Flops (CNSDFP*) and Metastable Flops (SDFSYNCP*)

- The Product remains aligned to DP28FDSOI_7ML 1.0.

2.7 Version 2.0

- The Product is aligned to DP28FDSOI_7ML 1.0. Refer to Design Package Documents for more details.
- For Standard Cell Library Specific Features, Refer to StandardCell_Notes.pdf Present in Design Package.

3 Known Problems and Solutions

3.1 DP related Generic Problems

- For Generic Standard cell Library related problem for this DP, please refer to KPS section inside StandardCell_Notes.pdf Present in Design Package.

3.2 Placement Restriction

➥ Specific Placement restriction due to Poly Landing pad

☞ Placement restriction has been modelled in CADENCE LEF - through “Symmetry property” and in SYNOPSYS FRAM - through “spacing_label property” for the following cells:

- C12T28SOI_LR_CNIVX5_P0/P4/P10/P16
- C12T28SOI_LR_CNIVX8_P0/P4/P10/P16

	*As mentioned above, modelling the placement constraint is different between Synopsys and Cadence. Therefore Need to be careful, if You do P&R with Synopsys and then go inside Cadence, the placement created by ICC could be declared as invalid by Encounter tool.*

3.3 Dont_use and dont_touch cells

➥ Specific attributes dont_use and dont_touch in Synopsys Technology File

☞ The “dont_touch” and “dont_use” attributes are defined in the Synopsys Technology Files for few cells. Reason can be -

a) Cell has some specific custom feature. Therefore We want to ensure that Either these cells are not automatically picked during Synthesis unless the designer

wishes to specically use them in the design or those are not replaced during Design Optimization.

b) Cell's functionality is not properly understood by tools.

Cells with such attributes are as following:

– C12T28SOIDV_LR_SDFSYNCPQX8_P0/P4/P10/P16
– C12T28SOIDV_LR_SDFSYNCPRQX8_P0/P4/P10/P16
– C12T28SOIDV_LR_SDFSYNCPSQX8_P0/P4/P10/P16
– C12T28SOI_LRP_CNHLSX15_P0/P4/P10/P16
– C12T28SOI_LRP_CNHLSX22_P0/P4/P10/P16
– C12T28SOI_LRP_CNHLSX29_P0/P4/P10/P16
– C12T28SOI_LRP_CNHLSX36_P0/P4/P10/P16
– C12T28SOI_LRP_CNHLSX51_P0/P4/P10/P16
– C12T28SOI_LRP_CNHLSX58_P0/P4/P10/P16
– C12T28SOI_LRP_CNHLSX7_P0/P4/P10/P16
– C12T28SOI_LRP_CNHLSX71_P0/P4/P10/P16
– C12T28SOI_LRP_CNHLSX93_P0/P4/P10/P16
– C12T28SOI_LRPHP_CNHLSX29_P0/P4/P10/P16
– C12T28SOI_LRPHP_CNHLSX36_P0/P4/P10/P16
– C12T28SOI_LRPHP_CNHLSX44_P0/P4/P10/P16
– C12T28SOI_LRPHP_CNHLSX51_P0/P4/P10/P16
– C12T28SOI_LRPHP_CNHLSX58_P0/P4/P10/P16
– C12T28SOI_LRPHP_CNHLSX71_P0/P4/P10/P16
– C12T28SOI_LRPHP_CNHLSX86_P0/P4/P10/P16

4 Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.

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