



cmos028fdsoi Technology

RVT models

DK1.2\_RF\_mmW

Comparison with DK1.1\_RF\_mmW model(s)

Ideal ring oscillators

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## General information on RVT models

- Maximum supply voltage is - V.
- Validity domain is defined as follows:
  - ✓ Drawn gate length varies from 30nm to 10um.
  - ✓ Drawn transistor width varies from 0.08um to 10um.
  - ✓ Device temperature varies from -40 °C to 125 °C.

# Output parameters definitions

- Model(s): nfet\_acc\_pfet\_acc

# **nfet\_acc\_pfet\_acc**

## **Electrical characteristics per geometry**

**nfet\_acc\_pfet\_acc @ w\_n=0.42e-6, l\_n=30e-9, p\_la\_n=0, nf\_n=2, sa\_n=85e9,  
sb\_n=85e-9, sd\_n=106e-9, sc\_n=56e-9, pcpastrx\_top\_n=169e-9,  
pcpastrx\_bot\_n=57e-9, w\_p=0.6e-6, l\_p=30e-9, p\_la\_p=0, nf\_p=2, sa\_p=85e9,  
sb\_p=85e-9, sd\_p=106e-9, sc\_p=113e-9, pcpastrx\_top\_p=169e-9,  
pcpastrx\_bot\_p=57e-9, vdd=0.9, temp=25.0**

DK1.2\_RF\_mmW wrt DK1.1\_RF\_mmW

	SS	TT	FF
<b>Fosc_gate [GHz]</b>	24.08 0.0%	27.92 0.0%	32.68 0.0%
<b>Idyn [μA]</b>	102.5 0.0%	122.6 0.0%	149.2 0.0%
<b>Pdyn [μW]</b>	92.22 0.0%	110.3 0.0%	134.3 0.0%
<b>Ceff [fF]</b>	4.73 0.0%	4.88 0.0%	5.07 0.0%
<b>Taup [ps]</b>	20.76 0.0%	17.91 0.0%	15.3 0.0%
<b>Istat_gate [nA]</b>	0.16 0.0%	0.48 0.0%	1.8 0.0%
<b>LogIstat_gate []</b>	-9.79 -0.0%	-9.32 -0.0%	-8.75 -0.0%

**nfet\_acc\_pfet\_acc @ w\_n=0.42e-6, l\_n=30e-9, p\_la\_n=4e-9, nf\_n=2, sa\_n=85e9,  
 sb\_n=85e-9, sd\_n=106e-9, sc\_n=56e-9, pcpastrx\_top\_n=169e-9,  
 pcpastrx\_bot\_n=57e-9, w\_p=0.6e-6, l\_p=30e-9, p\_la\_p=4e-9, nf\_p=2, sa\_p=85e9,  
 sb\_p=85e-9, sd\_p=106e-9, sc\_p=113e-9, pcpastrx\_top\_p=169e-9,  
 pcpastrx\_bot\_p=57e-9, vdd=0.9, temp=25.0**

DK1.2\_RF\_mmW wrt DK1.1\_RF\_mmW

	SS	TT	FF
<b>Fosc_gate [GHz]</b>	21.81 0.0%	25.16 0.0%	29.31 0.0%
<b>Idyn [μA]</b>	93.73 0.0%	111.8 0.0%	134.8 0.0%
<b>Pdyn [μW]</b>	84.35 0.0%	100.6 0.0%	121.3 0.0%
<b>Ceff [fF]</b>	4.77 0.0%	4.94 0.0%	5.11 0.0%
<b>Taup [ps]</b>	22.92 0.0%	19.87 0.0%	17.06 0.0%
<b>Istat_gate [nA]</b>	7.00e-02 0.0%	0.18 0.0%	0.62 0.0%
<b>LogIstat_gate []</b>	-10.15 -0.0%	-9.74 -0.0%	-9.21 -0.0%

**nfet\_acc\_pfet\_acc @ w\_n=0.42e-6, l\_n=30e-9, p\_la\_n=10e-9, nf\_n=2, sa\_n=85e9,  
sb\_n=85e-9, sd\_n=106e-9, sc\_n=56e-9, pcpastrx\_top\_n=169e-9,  
pcpastrx\_bot\_n=57e-9, w\_p=0.6e-6, l\_p=30e-9, p\_la\_p=10e-9, nf\_p=2, sa\_p=85e9,  
sb\_p=85e-9, sd\_p=106e-9, sc\_p=113e-9, pcpastrx\_top\_p=169e-9,  
pcpastrx\_bot\_p=57e-9, vdd=0.9, temp=25.0**

DK1.2\_RF\_mmW wrt DK1.1\_RF\_mmW

	SS	TT	FF
<b>Fosc_gate [GHz]</b>	18.8 0.0%	21.54 0.0%	24.97 0.0%
<b>Idyn [μA]</b>	82.77 0.0%	97.83 0.0%	117.4 0.0%
<b>Pdyn [μW]</b>	74.5 0.0%	88.05 0.0%	105.7 0.0%
<b>Ceff [fF]</b>	4.89 0.0%	5.05 0.0%	5.23 0.0%
<b>Taup [ps]</b>	26.6 0.0%	23.21 0.0%	20.03 0.0%
<b>Istat_gate [nA]</b>	2.92e-02 0.0%	7.36e-02 0.0%	0.31 0.0%
<b>LogIstat_gate []</b>	-10.53 -0.0%	-10.13 -0.0%	-9.51 -0.0%



**nfet\_acc\_pfet\_acc @ w\_n=0.42e-6, l\_n=30e-9, p\_la\_n=16e-9, nf\_n=2, sa\_n=85e9,  
sb\_n=85e-9, sd\_n=106e-9, sc\_n=56e-9, pcpastrx\_top\_n=169e-9,  
pcpastrx\_bot\_n=57e-9, w\_p=0.6e-6, l\_p=30e-9, p\_la\_p=16e-9, nf\_p=2, sa\_p=85e9,  
sb\_p=85e-9, sd\_p=106e-9, sc\_p=113e-9, pcpastrx\_top\_p=169e-9,  
pcpastrx\_bot\_p=57e-9, vdd=0.9, temp=25.0**

DK1.2\_RF\_mmW wrt DK1.1\_RF\_mmW

	SS	TT	FF
<b>Fosc_gate [GHz]</b>	16.13 0.0%	18.36 0.0%	21.18 0.0%
<b>Idyn [μA]</b>	72.99 0.0%	85.86 0.0%	102.6 0.0%
<b>Pdyn [μW]</b>	65.69 0.0%	77.28 0.0%	92.33 0.0%
<b>Ceff [fF]</b>	5.03 0.0%	5.2 0.0%	5.38 0.0%
<b>Taup [ps]</b>	31 0.0%	27.24 0.0%	23.6 0.0%
<b>Istat_gate [nA]</b>	1.80e-02 0.0%	5.08e-02 0.0%	0.28 0.0%
<b>LogIstat_gate []</b>	-10.74 -0.0%	-10.29 -0.0%	-9.56 -0.0%

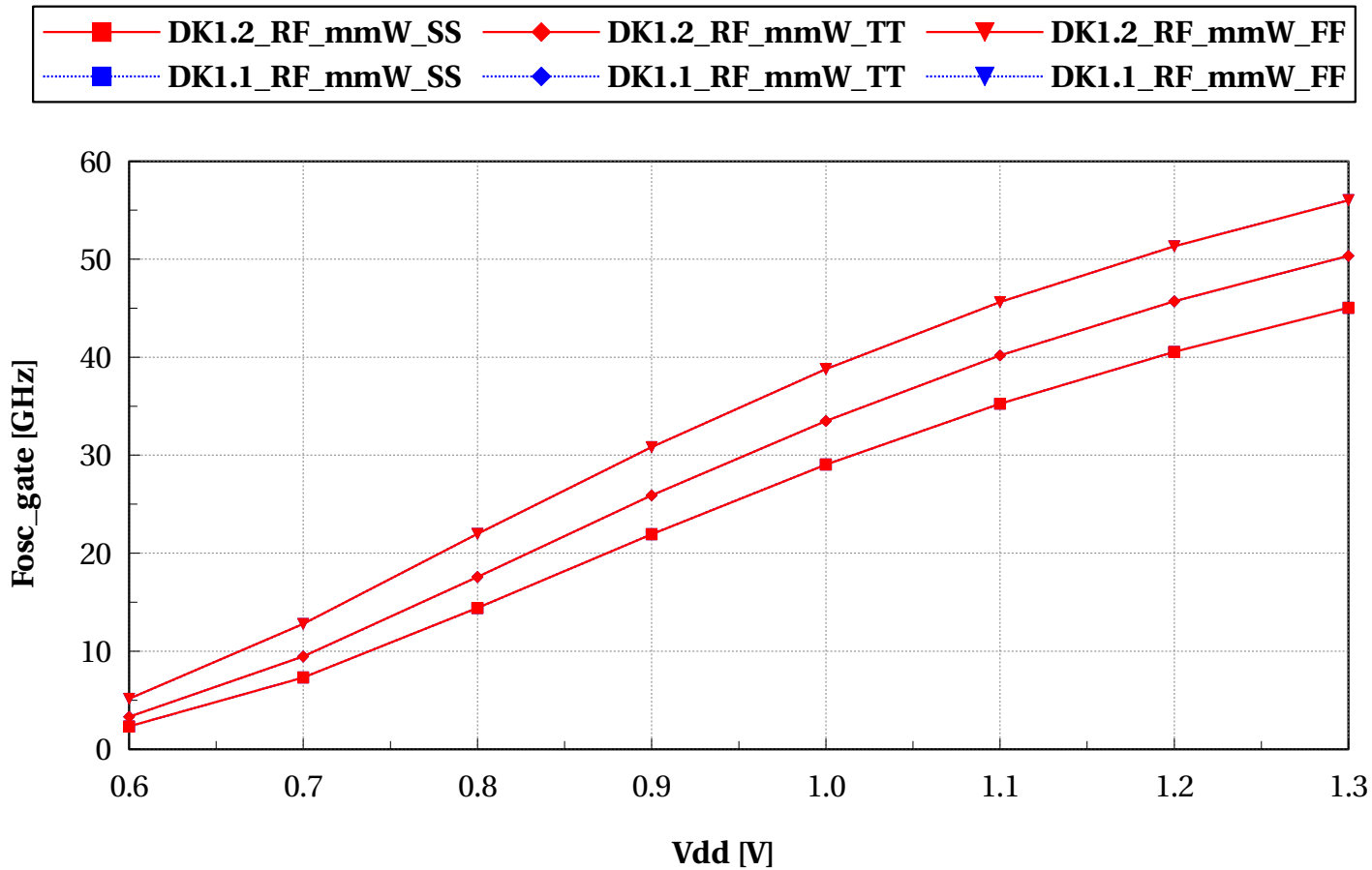
# **nfet\_acc\_pfet\_acc**

## **Electrical characteristics scaling**

## "RO FOM's vs Vdd @ T=-40C, PB=0"

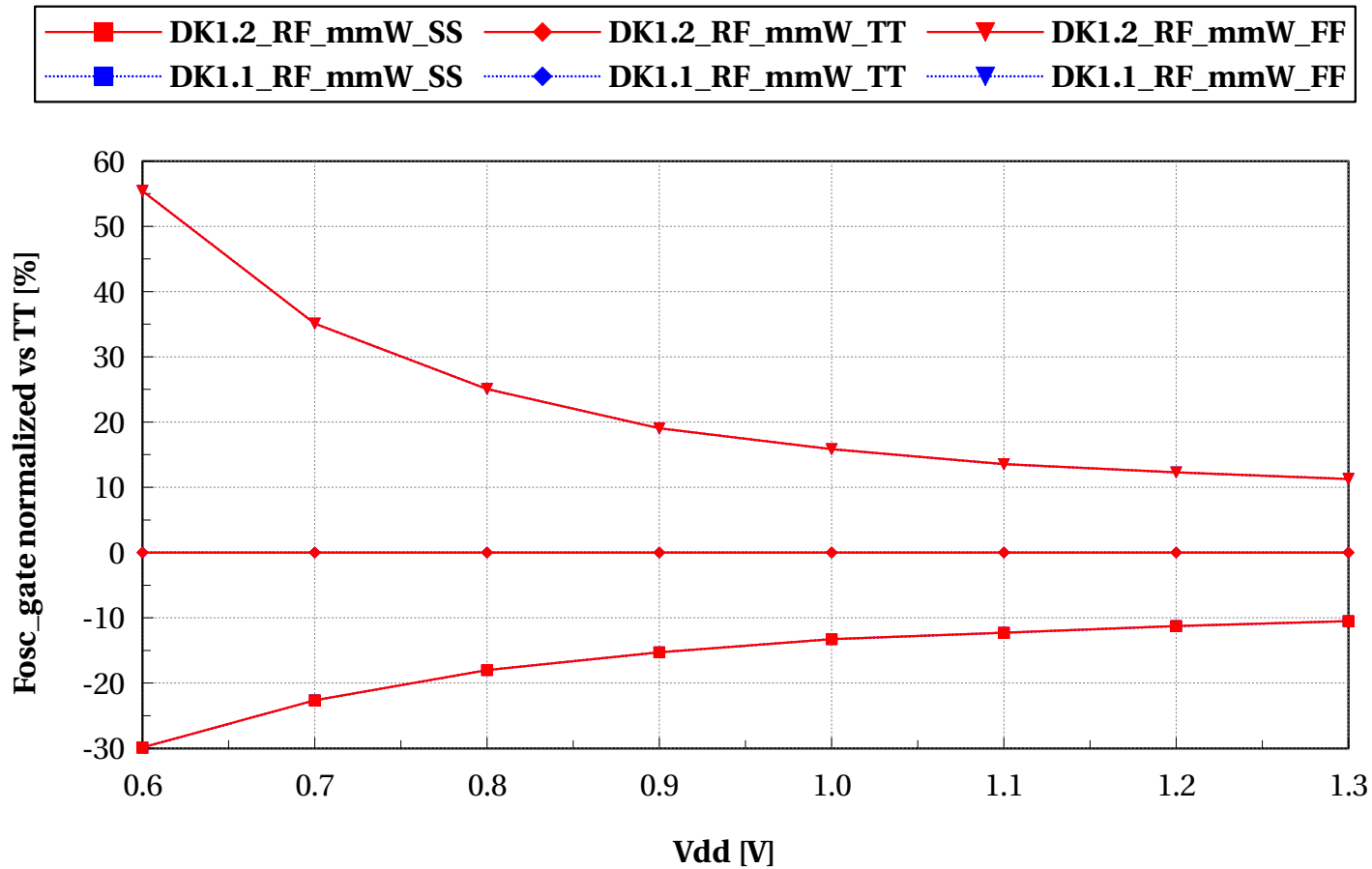
# nfet\_acc\_pfet\_acc, Fosc\_gate [GHz] vs Vdd [V]

temp=-40 and p\_la\_n=0



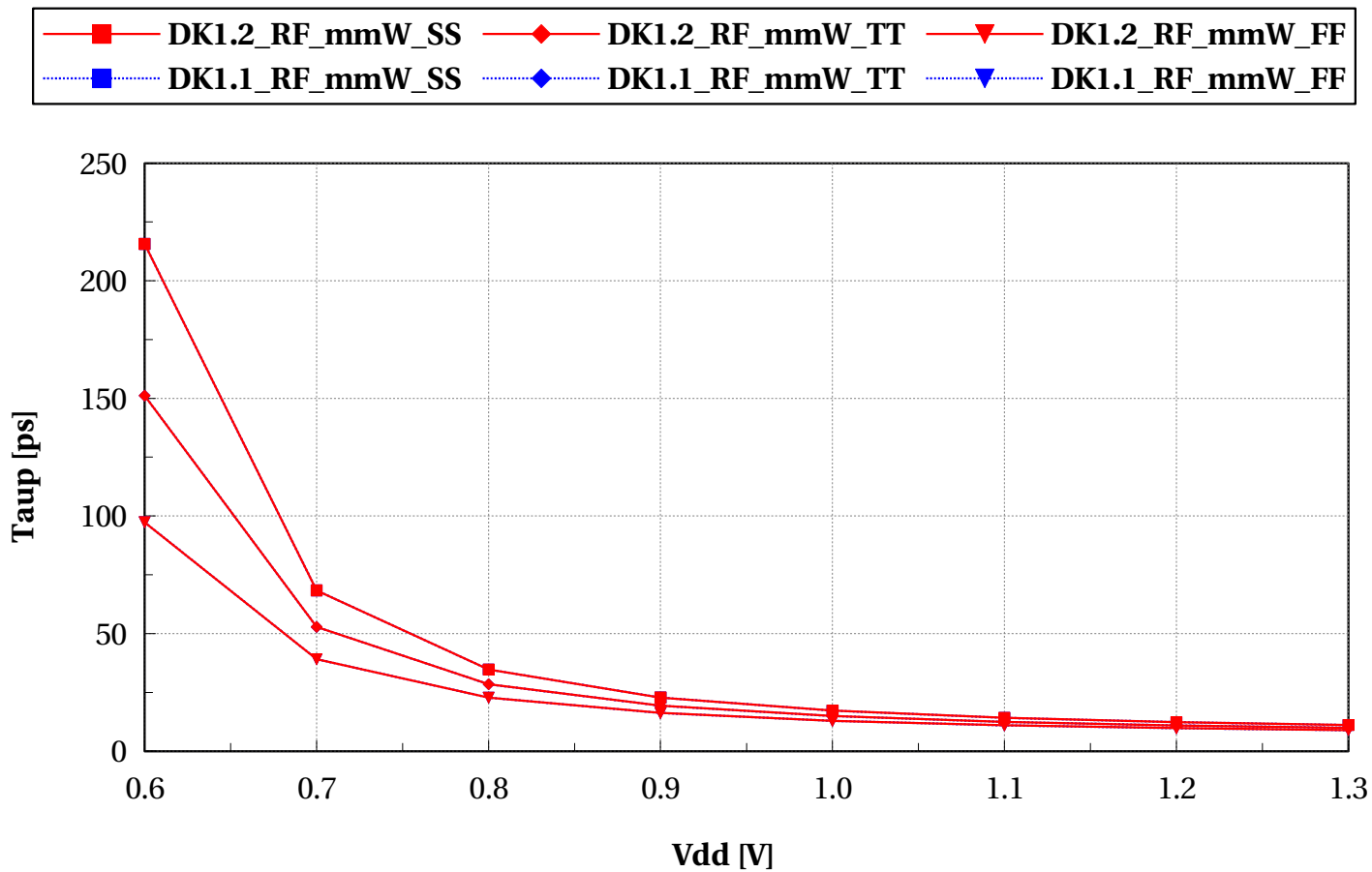
## nfet\_acc\_pfet\_acc, Fosc\_gate normalized vs TT [%] vs Vdd [V]

temp=-40 and p\_la\_n=0



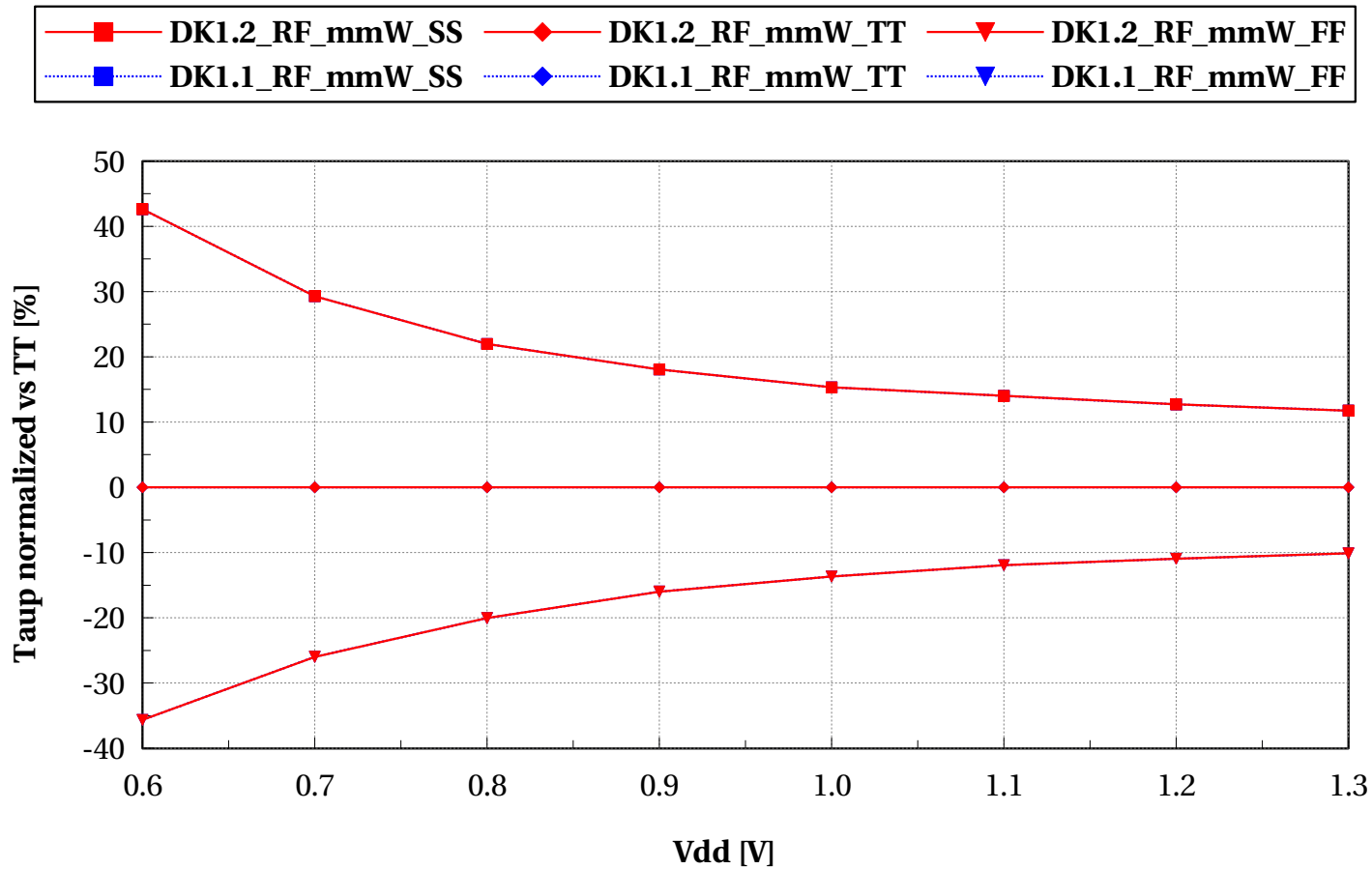
## nfet\_acc\_pfet\_acc, Taup [ps] vs Vdd [V]

temp=-40 and p\_la\_n=0



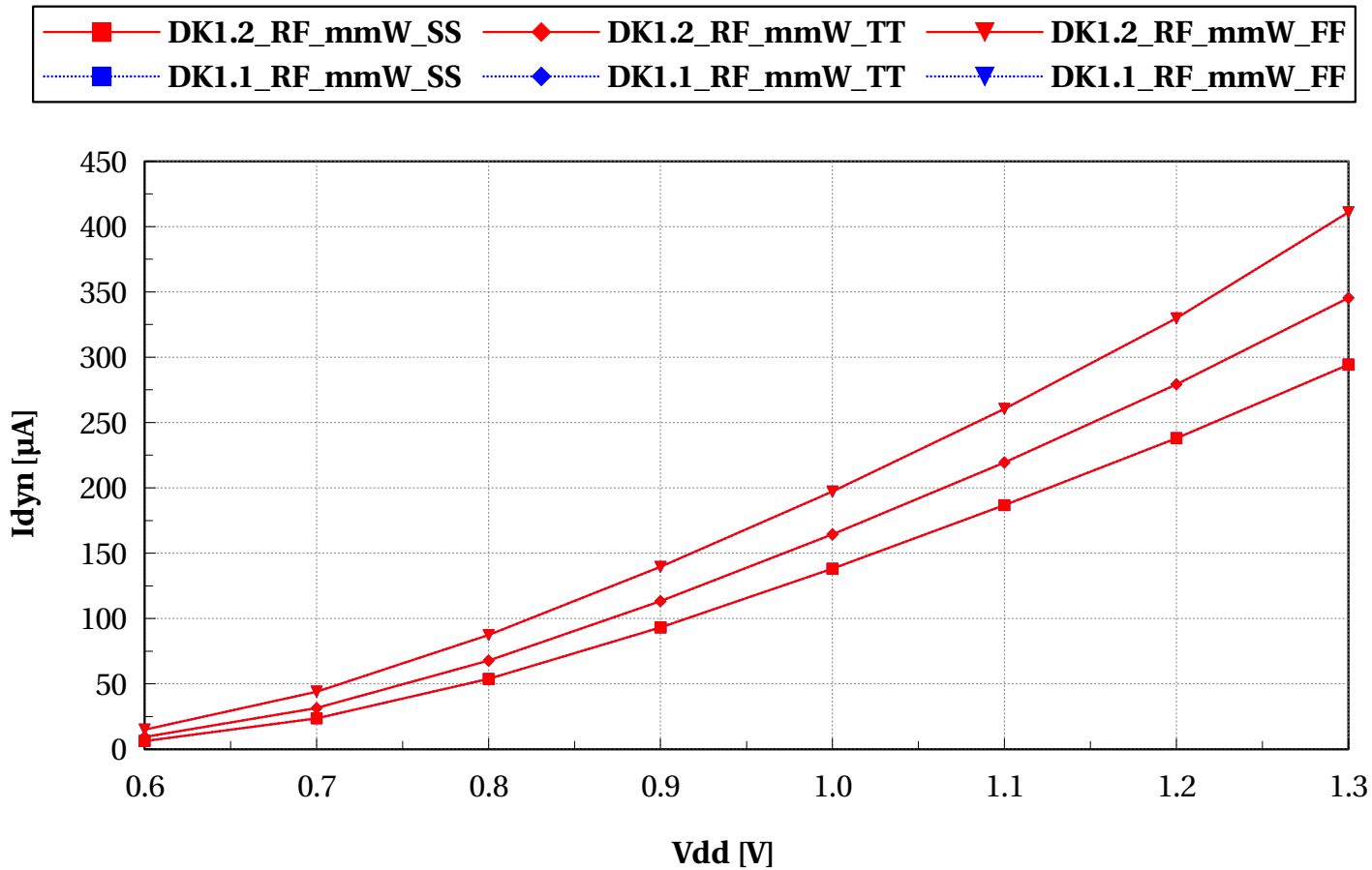
# nfet\_acc\_pfet\_acc, Taup normalized vs TT [%] vs Vdd [V]

temp=-40 and p\_la\_n=0



# nfet\_acc\_pfet\_acc, Idyn [ $\mu$ A] vs Vdd [V]

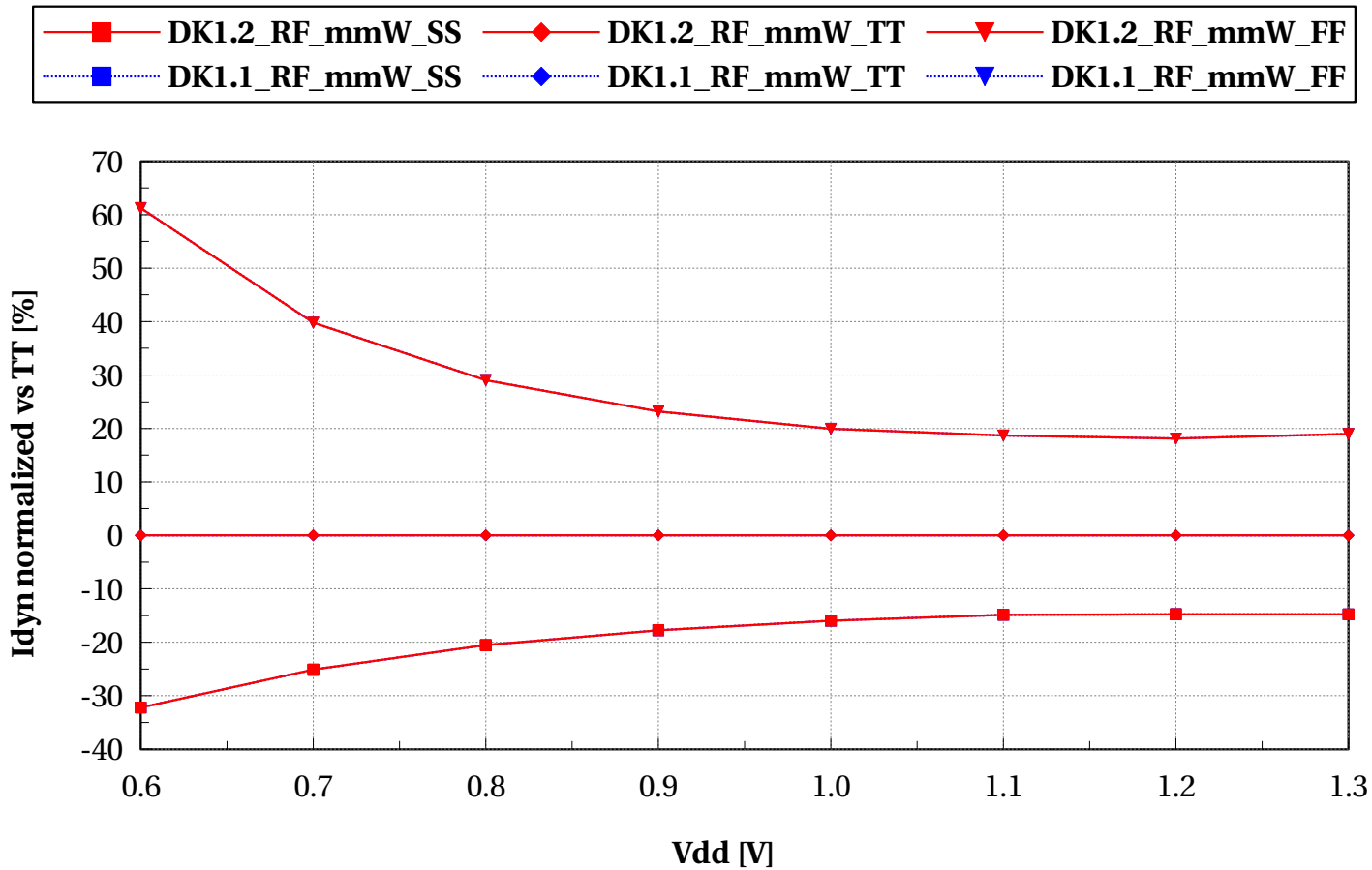
temp=-40 and p\_la\_n=0





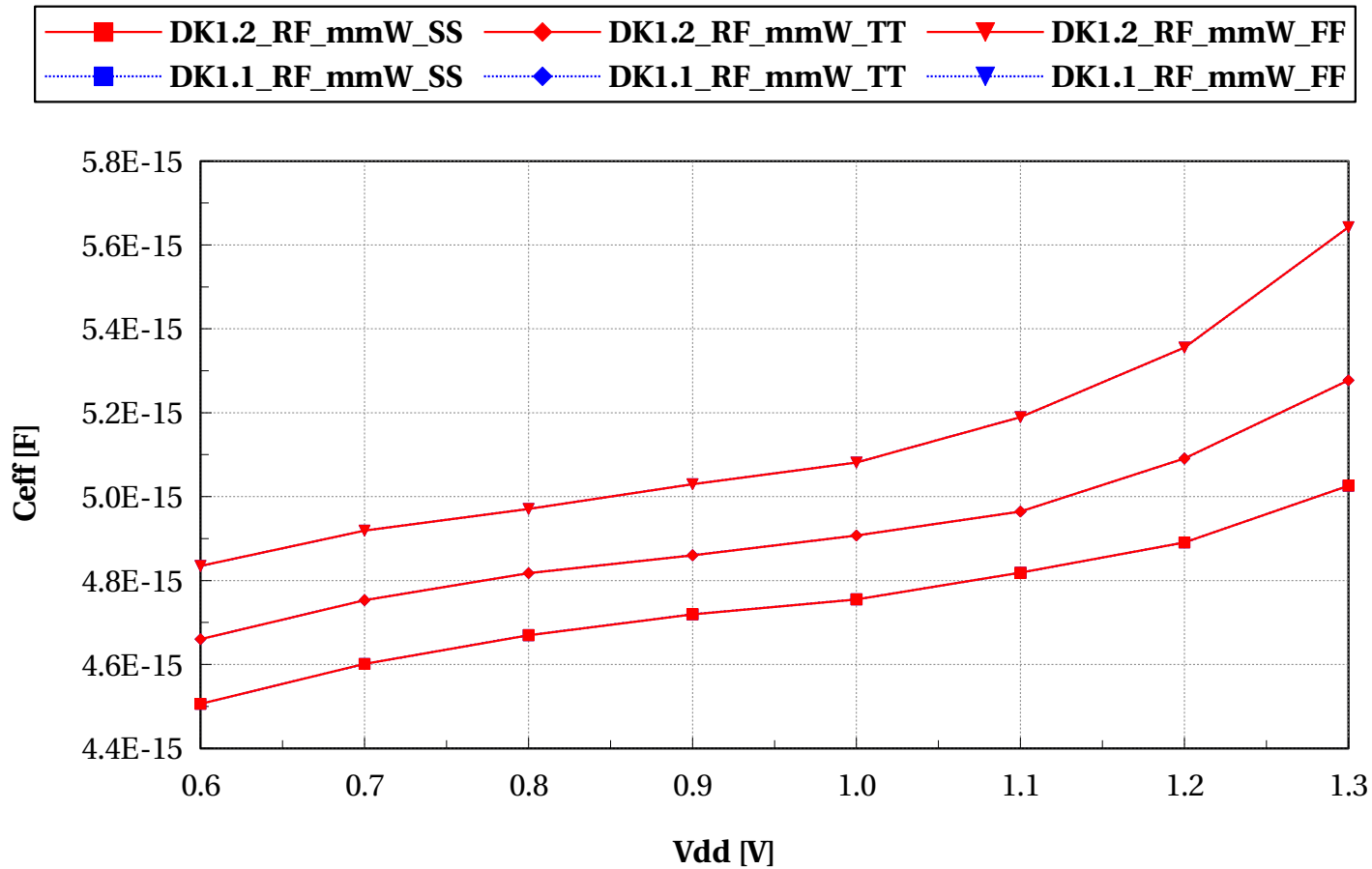
# nfet\_acc\_pfet\_acc, Idyn normalized vs TT [%] vs Vdd [V]

temp=-40 and p\_la\_n=0



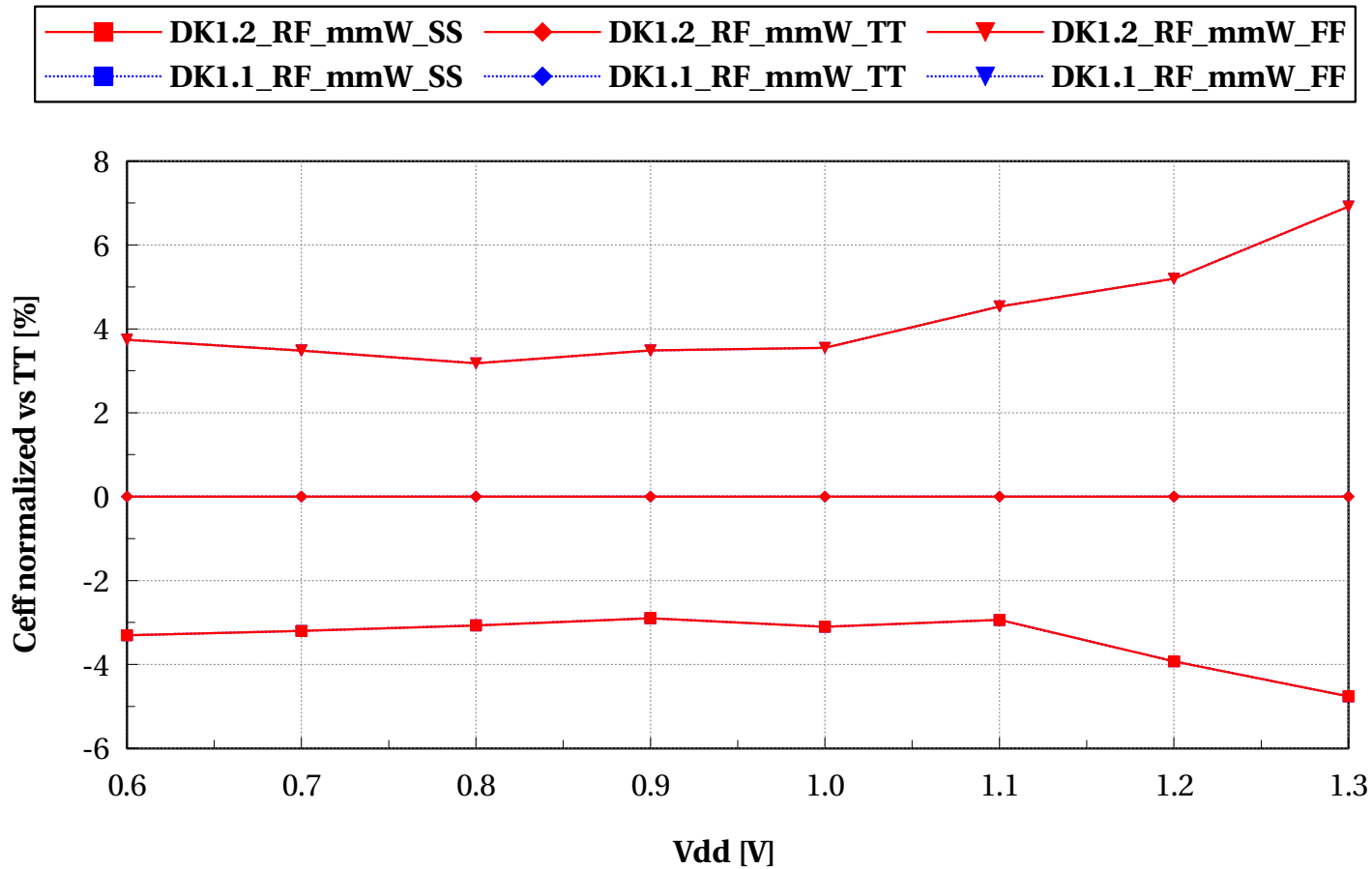
# nfet\_acc\_pfet\_acc, Ceff [F] vs Vdd [V]

temp=-40 and p\_la\_n=0



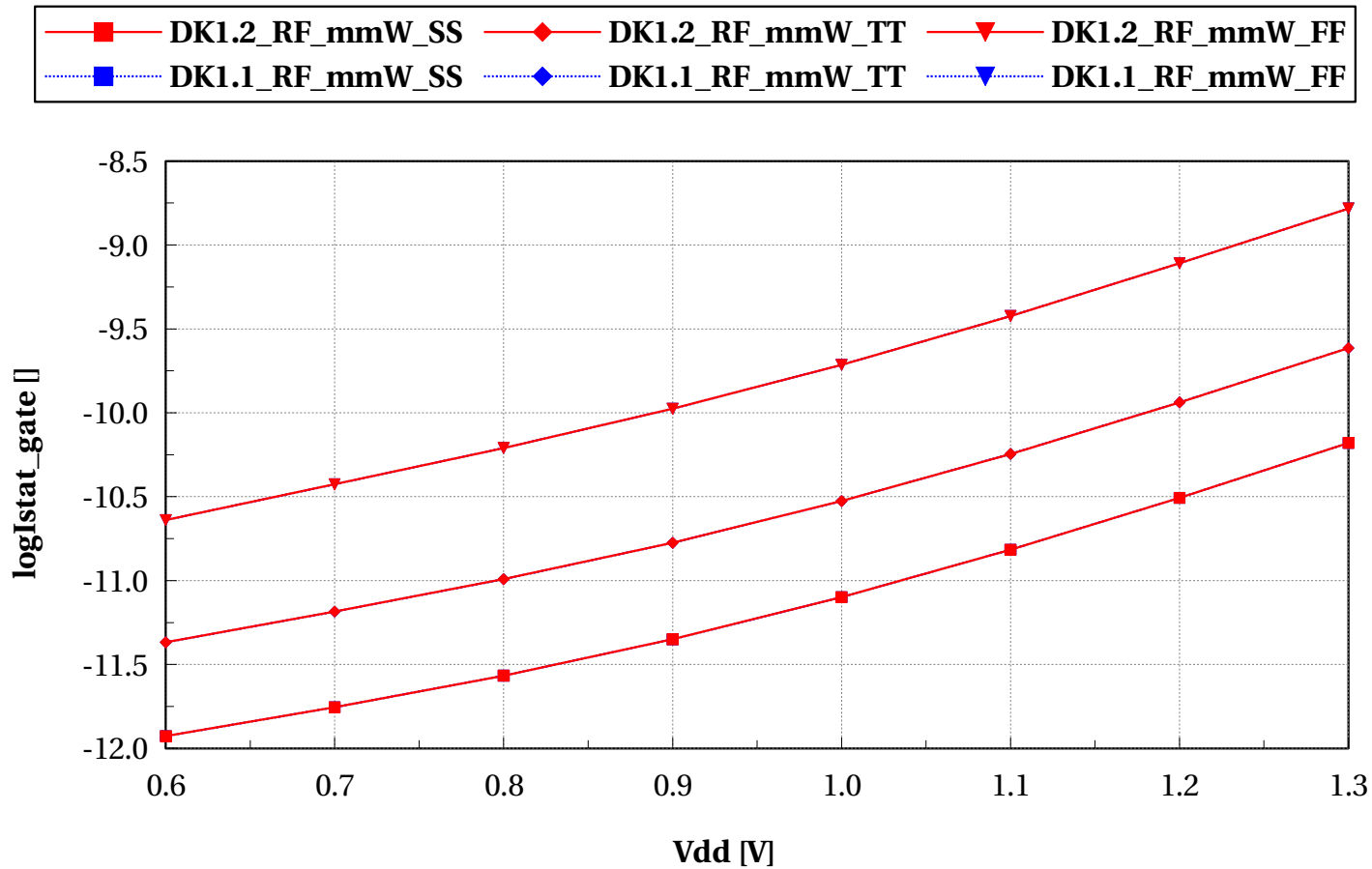
# nfet\_acc\_pfet\_acc, Ceff normalized vs TT [%] vs Vdd [V]

temp=-40 and p\_la\_n=0



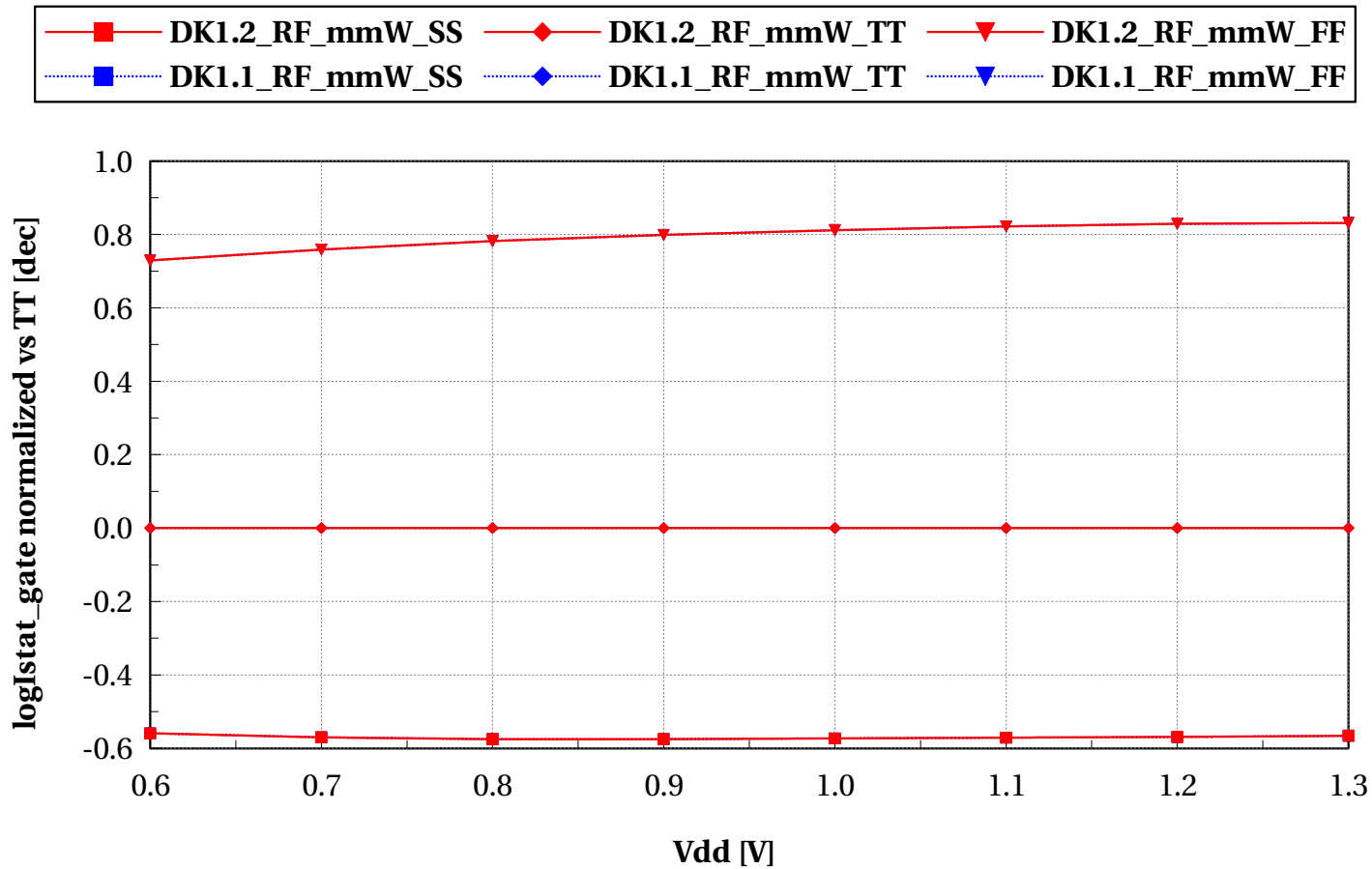
# nfet\_acc\_pfet\_acc, logIstat\_gate [] vs Vdd [V]

temp=-40 and p\_la\_n=0



# nfet\_acc\_pfet\_acc, logIstat\_gate normalized vs TT [dec] vs Vdd [V]

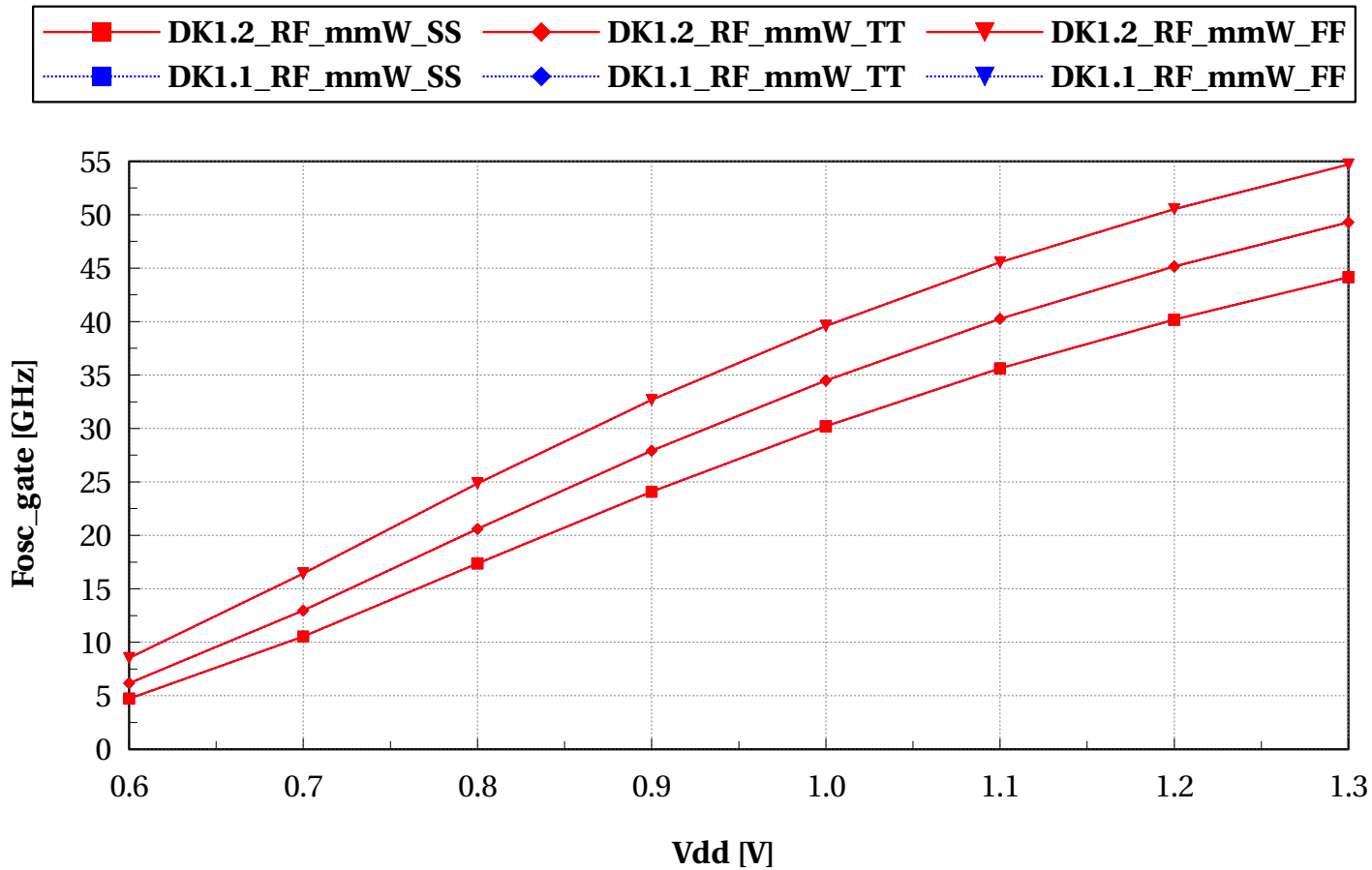
temp=-40 and p\_la\_n=0



## "RO FOM's vs Vdd @ T==25C, PB=0"

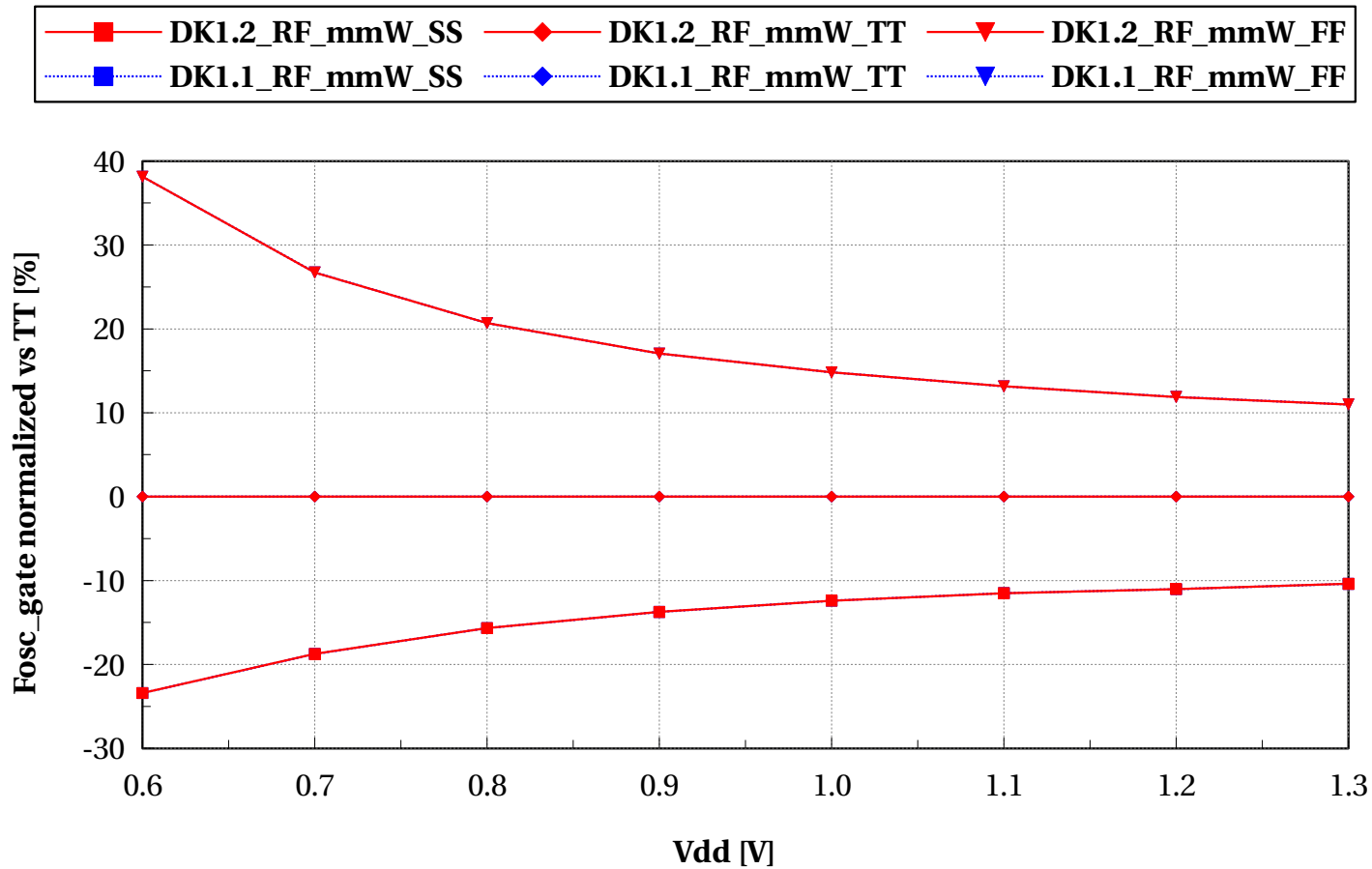
# nfet\_acc\_pfet\_acc, Fosc\_gate [GHz] vs Vdd [V]

temp==25 and p\_la\_n==0



# nfet\_acc\_pfet\_acc, Fosc\_gate normalized vs TT [%] vs Vdd [V]

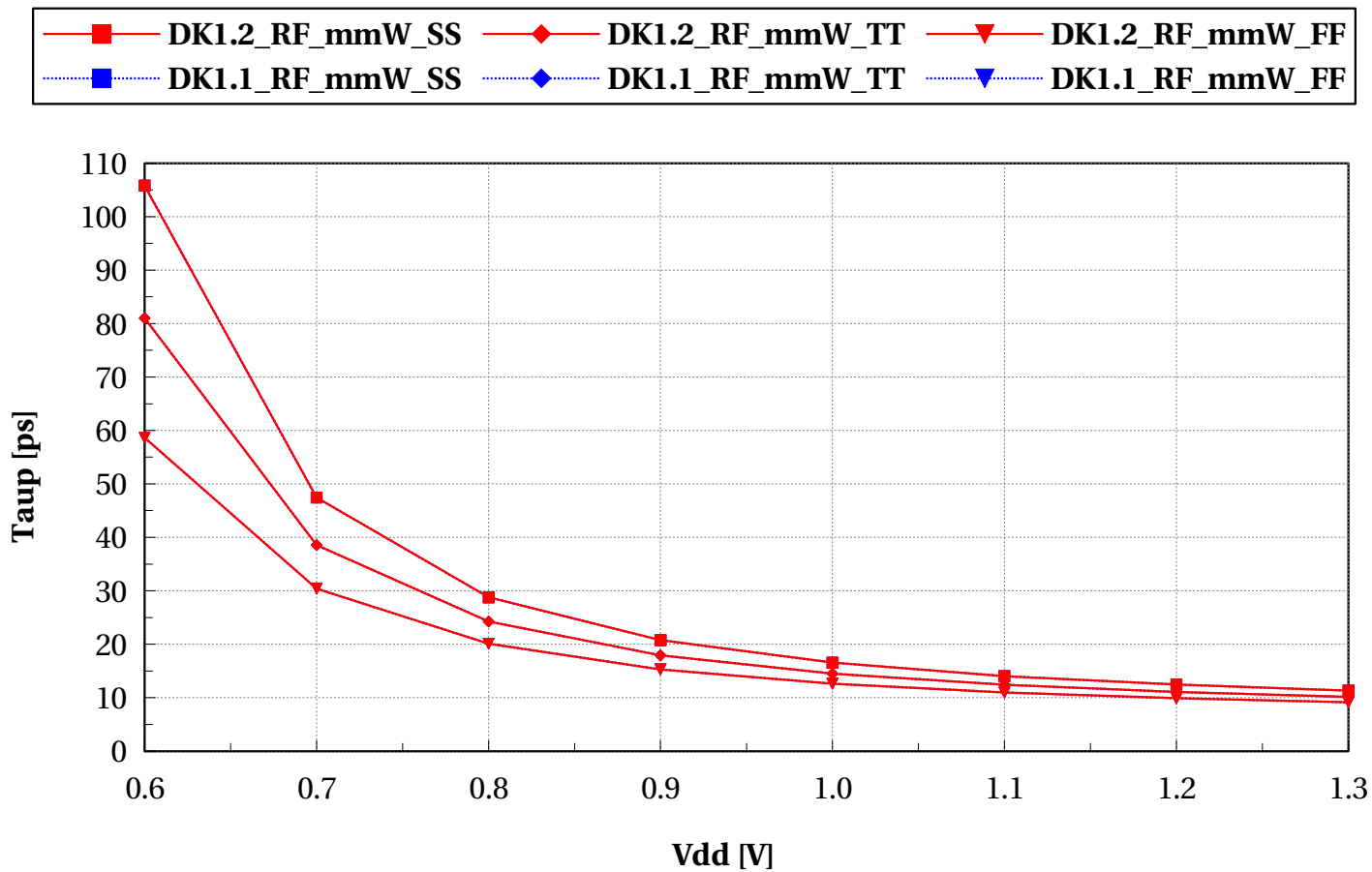
temp==25 and p\_la\_n==0





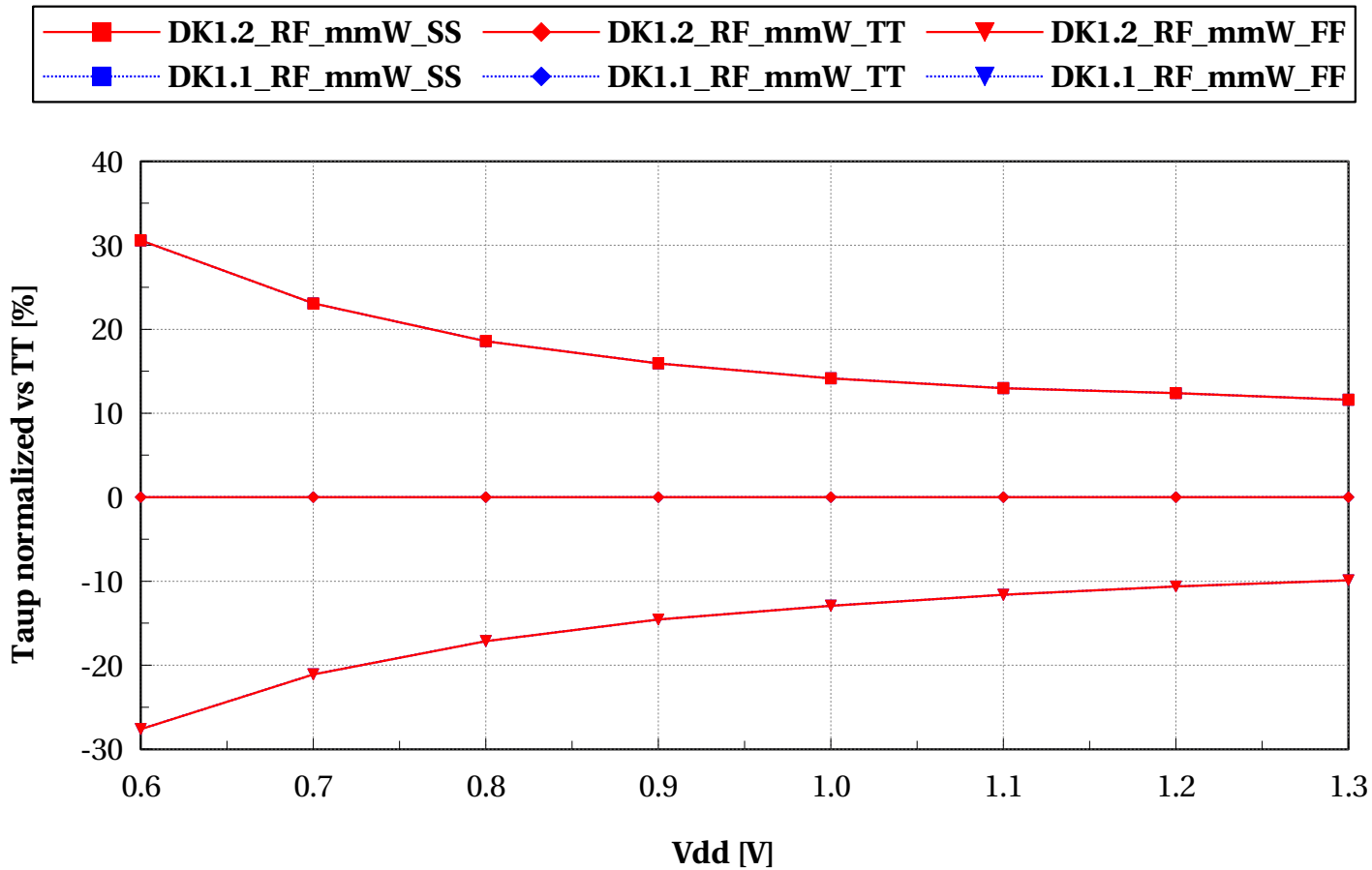
# nfet\_acc\_pfet\_acc, Taup [ps] vs Vdd [V]

temp==25 and p\_la\_n==0



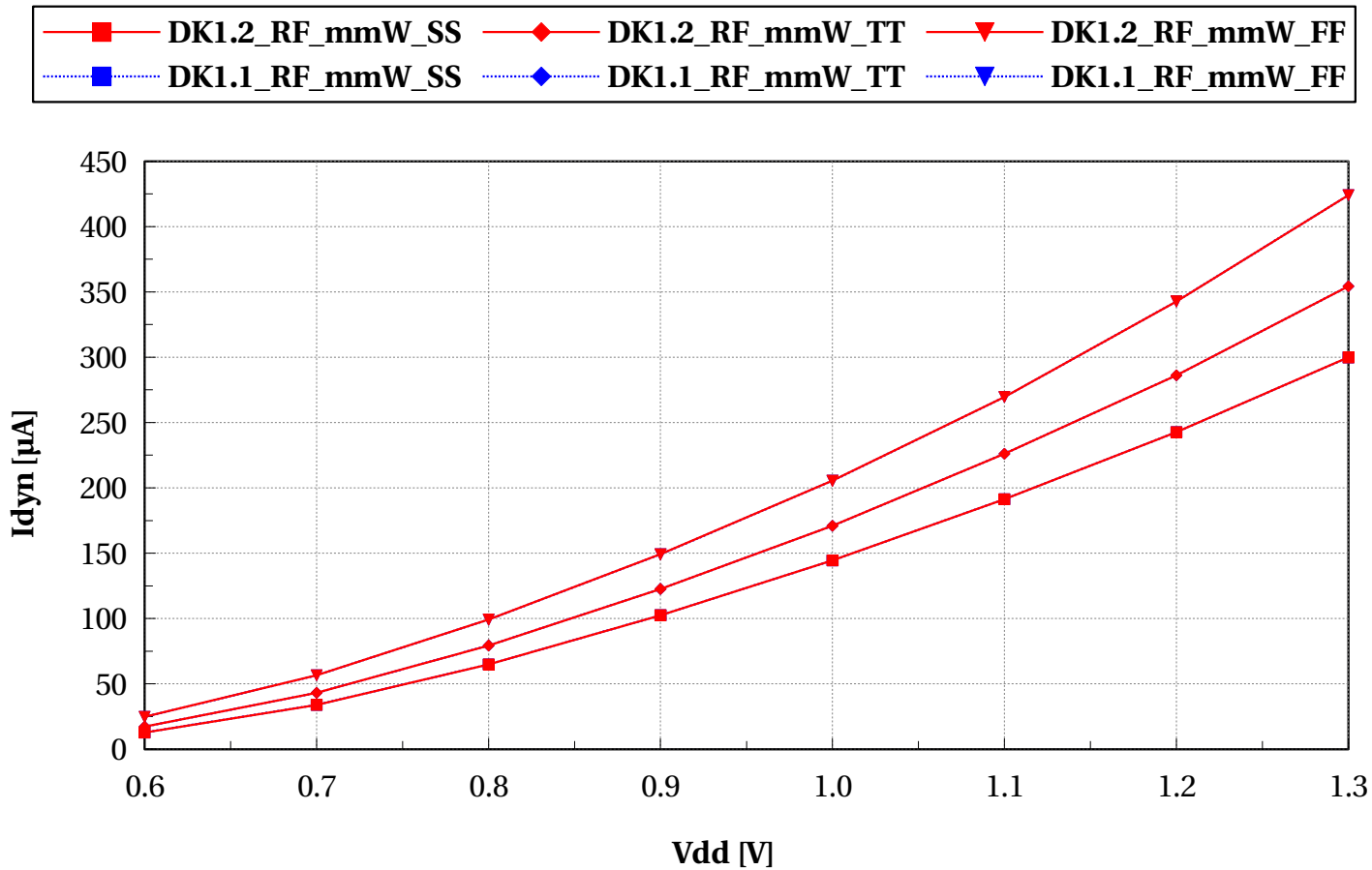
# nfet\_acc\_pfet\_acc, Taup normalized vs TT [%] vs Vdd [V]

temp==25 and p\_la\_n==0



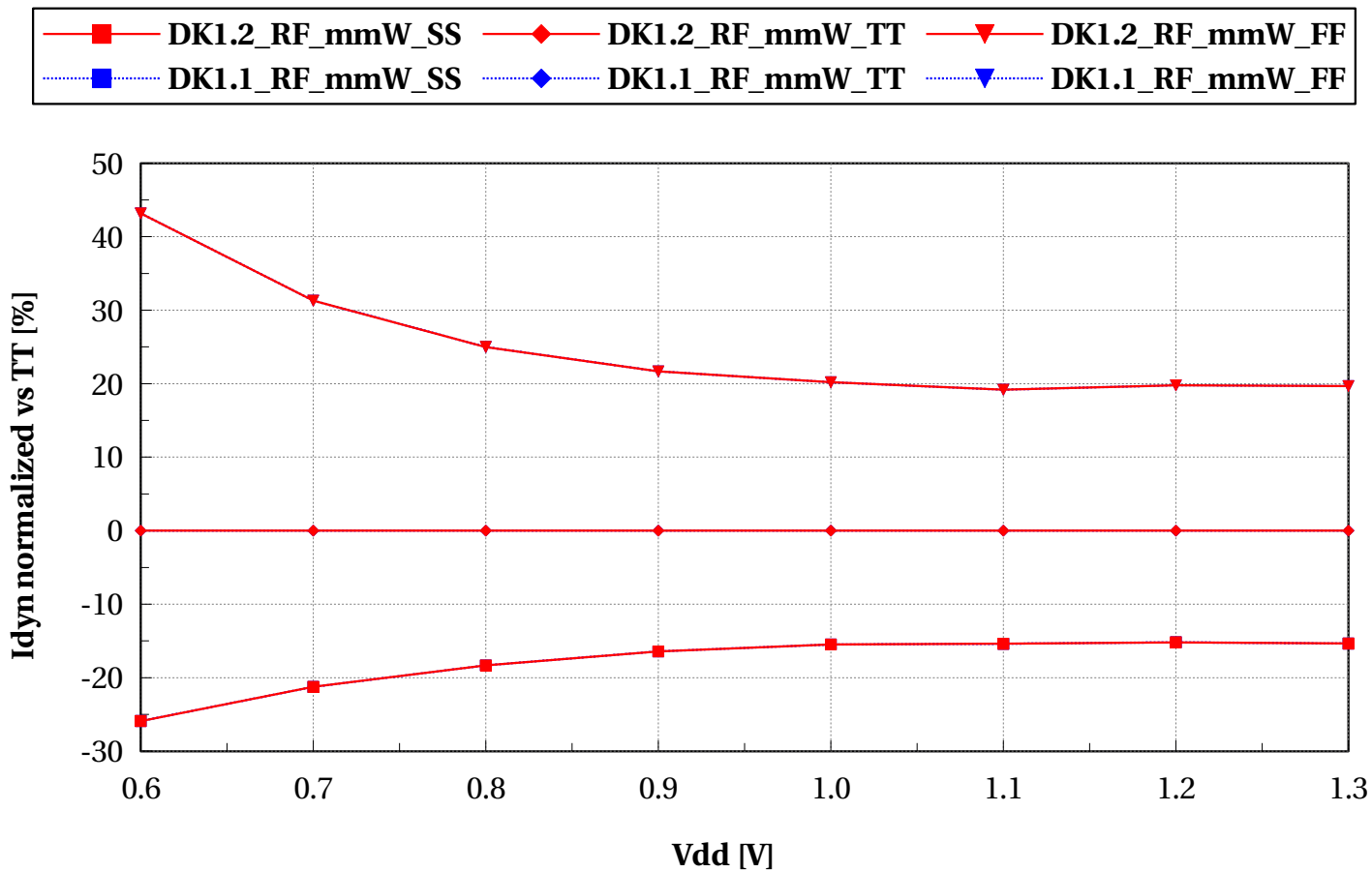
# nfet\_acc\_pfet\_acc, Idyn [ $\mu$ A] vs Vdd [V]

temp==25 and p\_la\_n==0



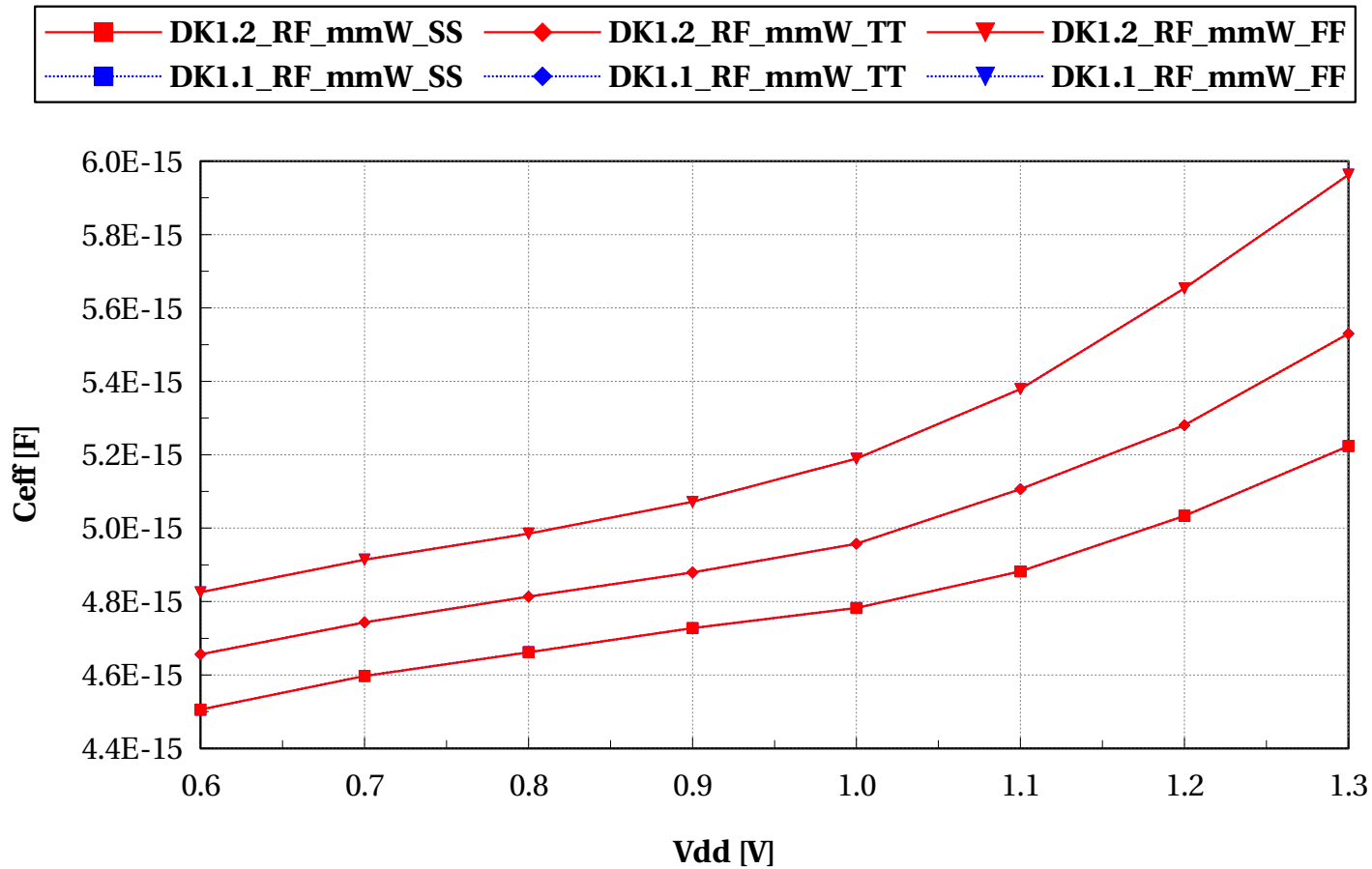
# nfet\_acc\_pfet\_acc, Idyn normalized vs TT [%] vs Vdd [V]

temp==25 and p\_la\_n==0



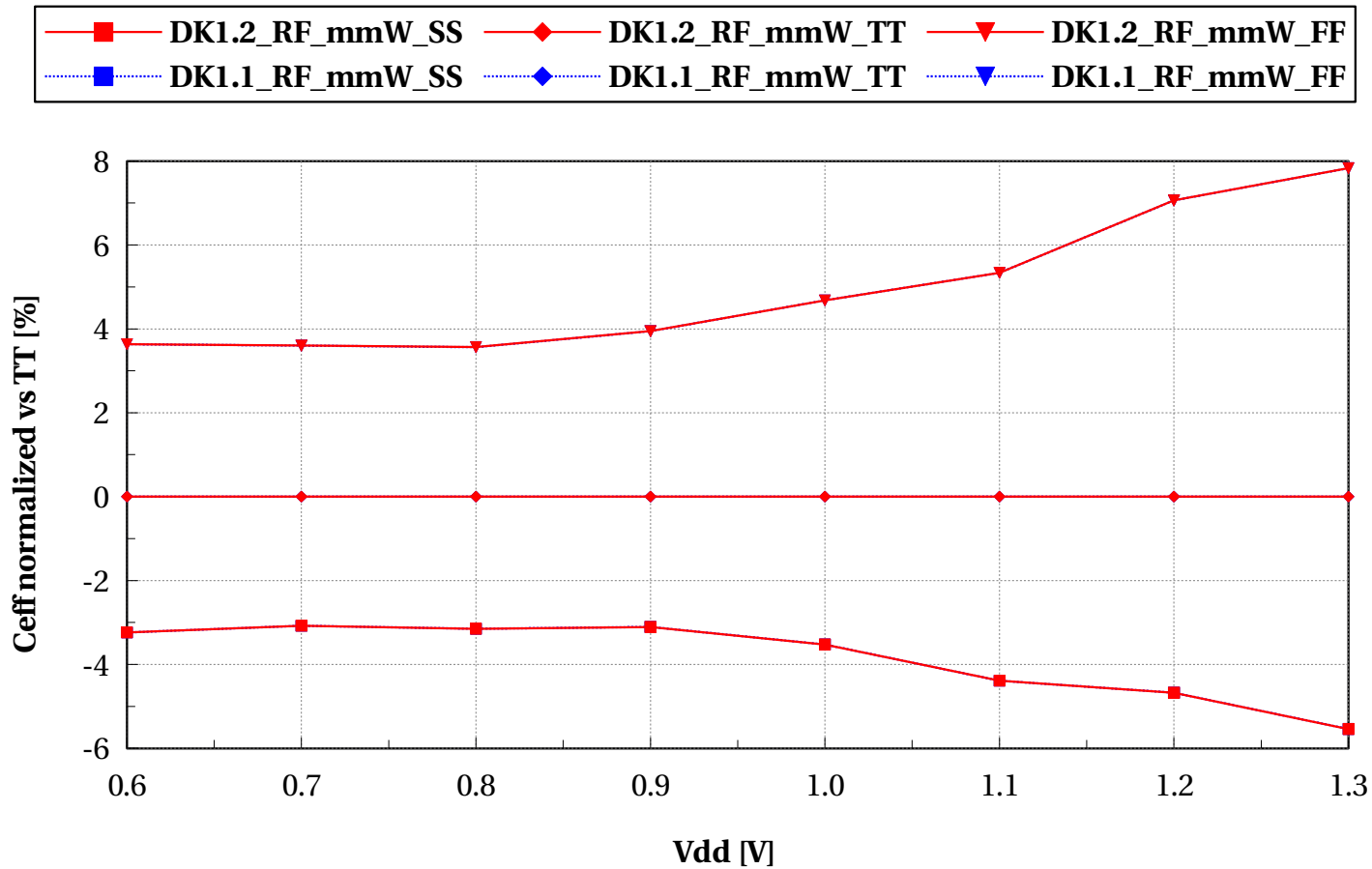
# nfet\_acc\_pfet\_acc, Ceff [F] vs Vdd [V]

temp==25 and p\_la\_n==0



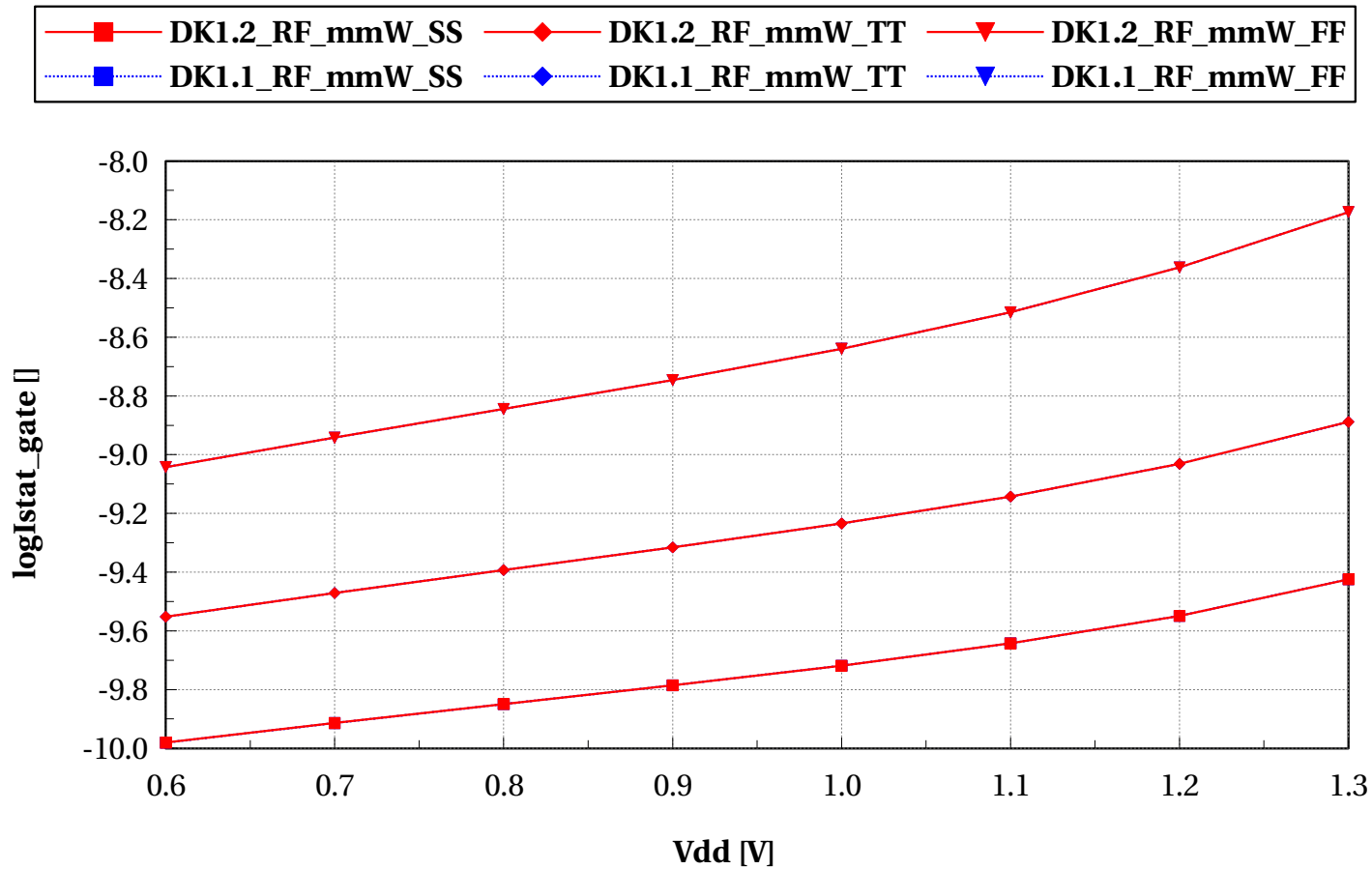
# nfet\_acc\_pfet\_acc, Ceff normalized vs TT [%] vs Vdd [V]

temp==25 and p\_la\_n==0



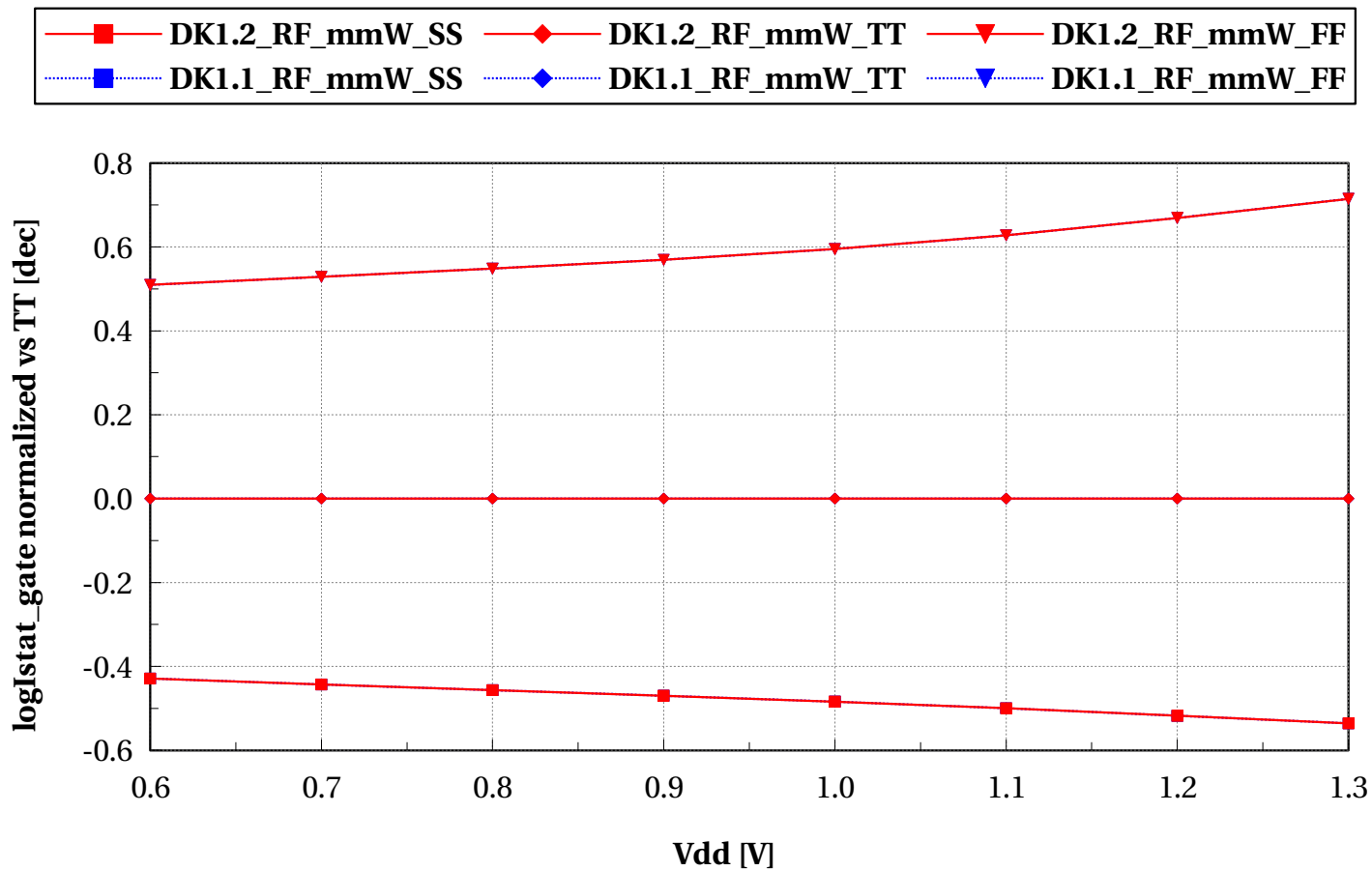
# nfet\_acc\_pfet\_acc, logIstat\_gate [] vs Vdd [V]

temp==25 and p\_la\_n==0



# nfet\_acc\_pfet\_acc, logIstat\_gate normalized vs TT [dec] vs Vdd [V]

temp==25 and p\_la\_n==0

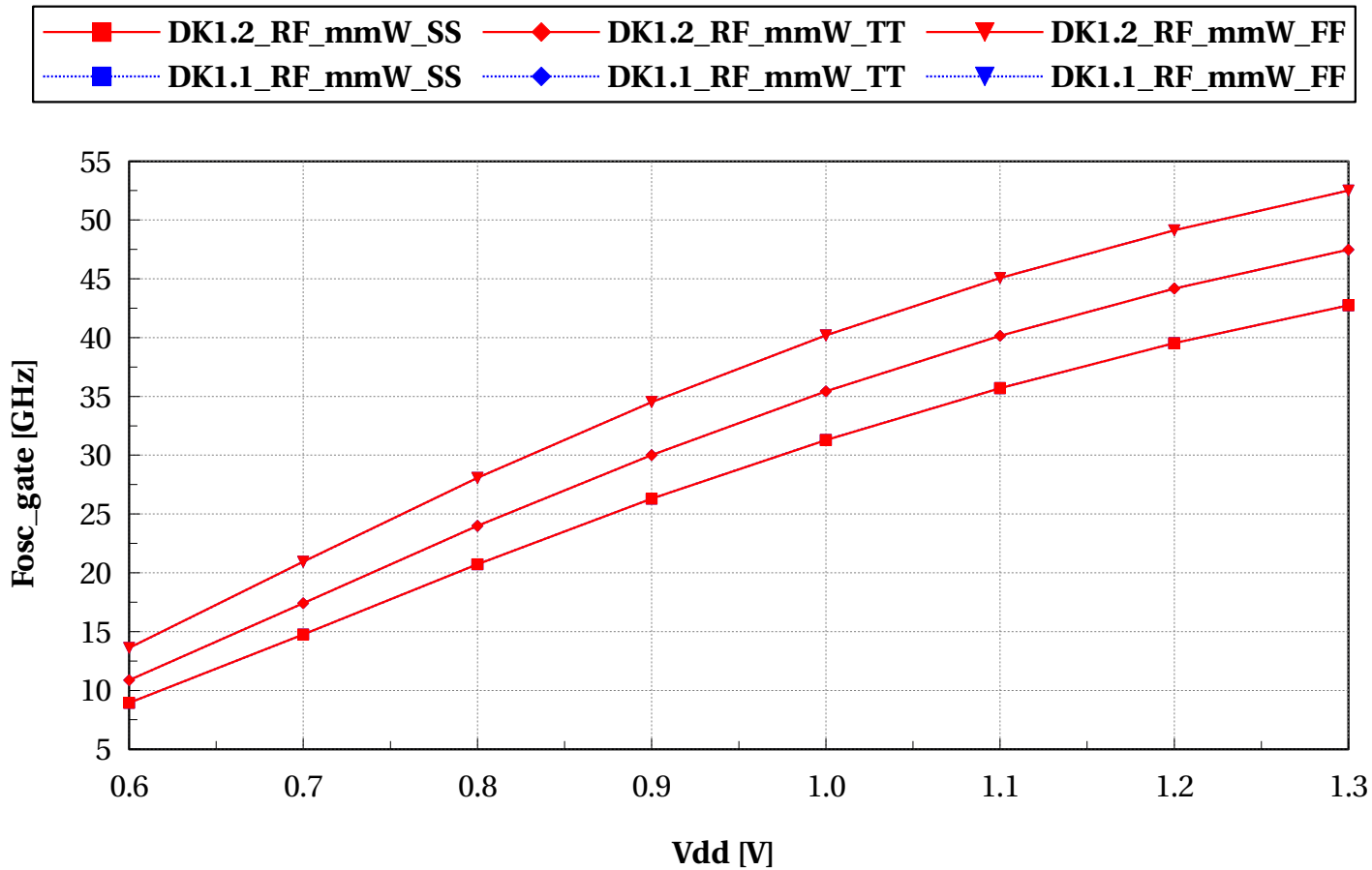




## "RO FOM's vs Vdd @ T==125C, PB=0"

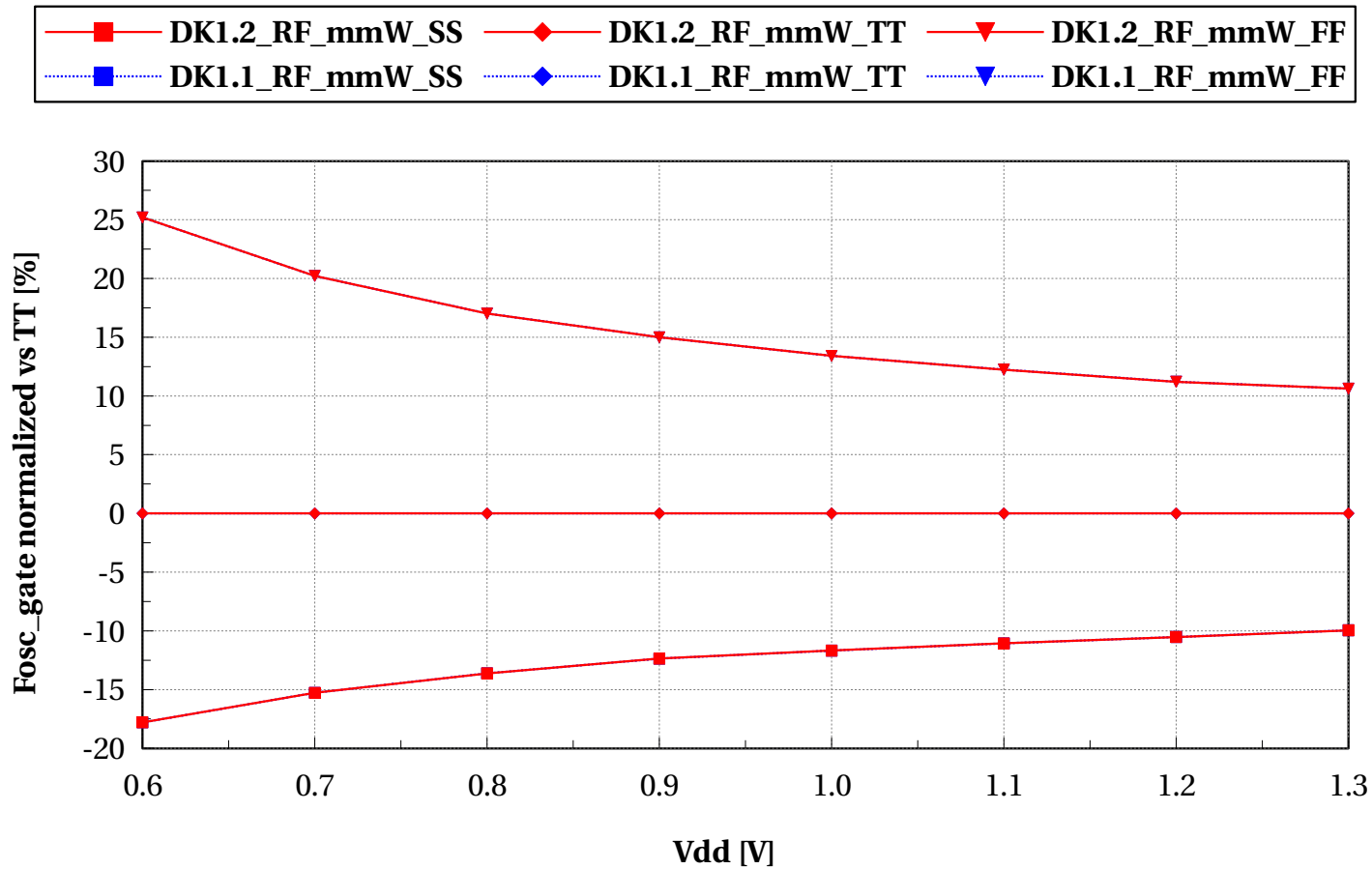
# nfet\_acc\_pfet\_acc, Fosc\_gate [GHz] vs Vdd [V]

temp==125 and p\_la\_n==0



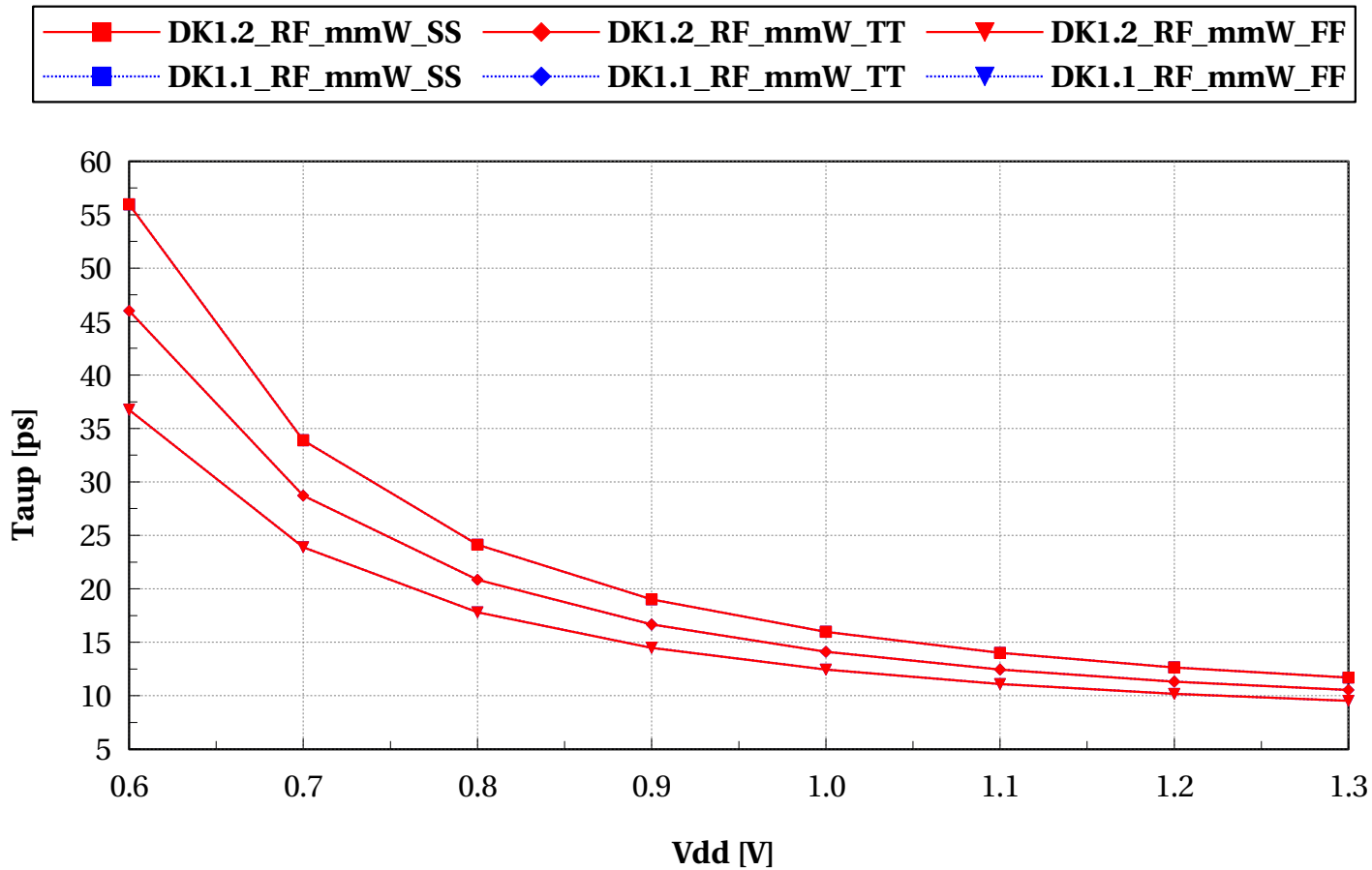
# nfet\_acc\_pfet\_acc, Fosc\_gate normalized vs TT [%] vs Vdd [V]

temp==125 and p\_la\_n==0



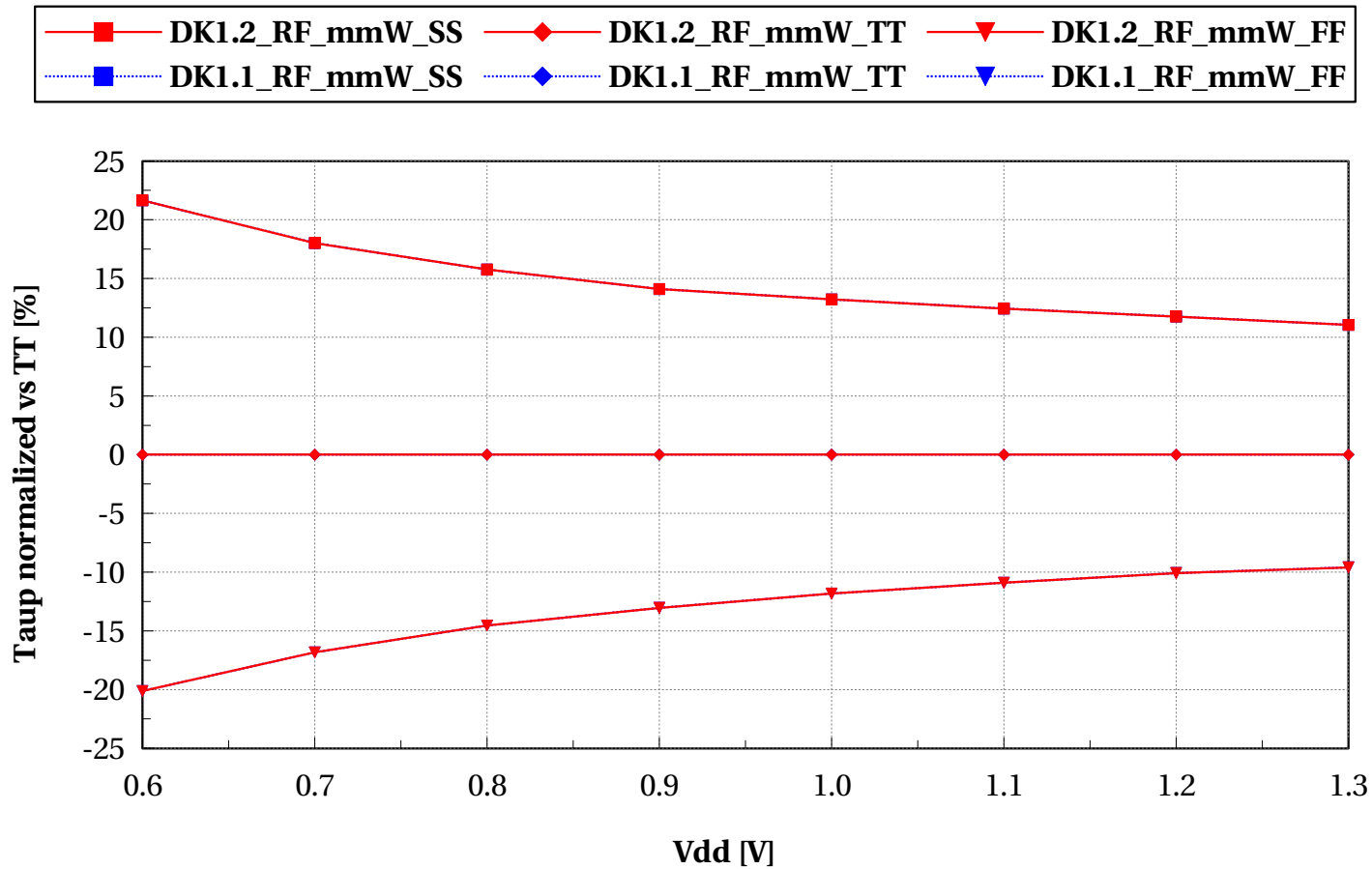
## nfet\_acc\_pfet\_acc, Taup [ps] vs Vdd [V]

temp==125 and p\_la\_n==0



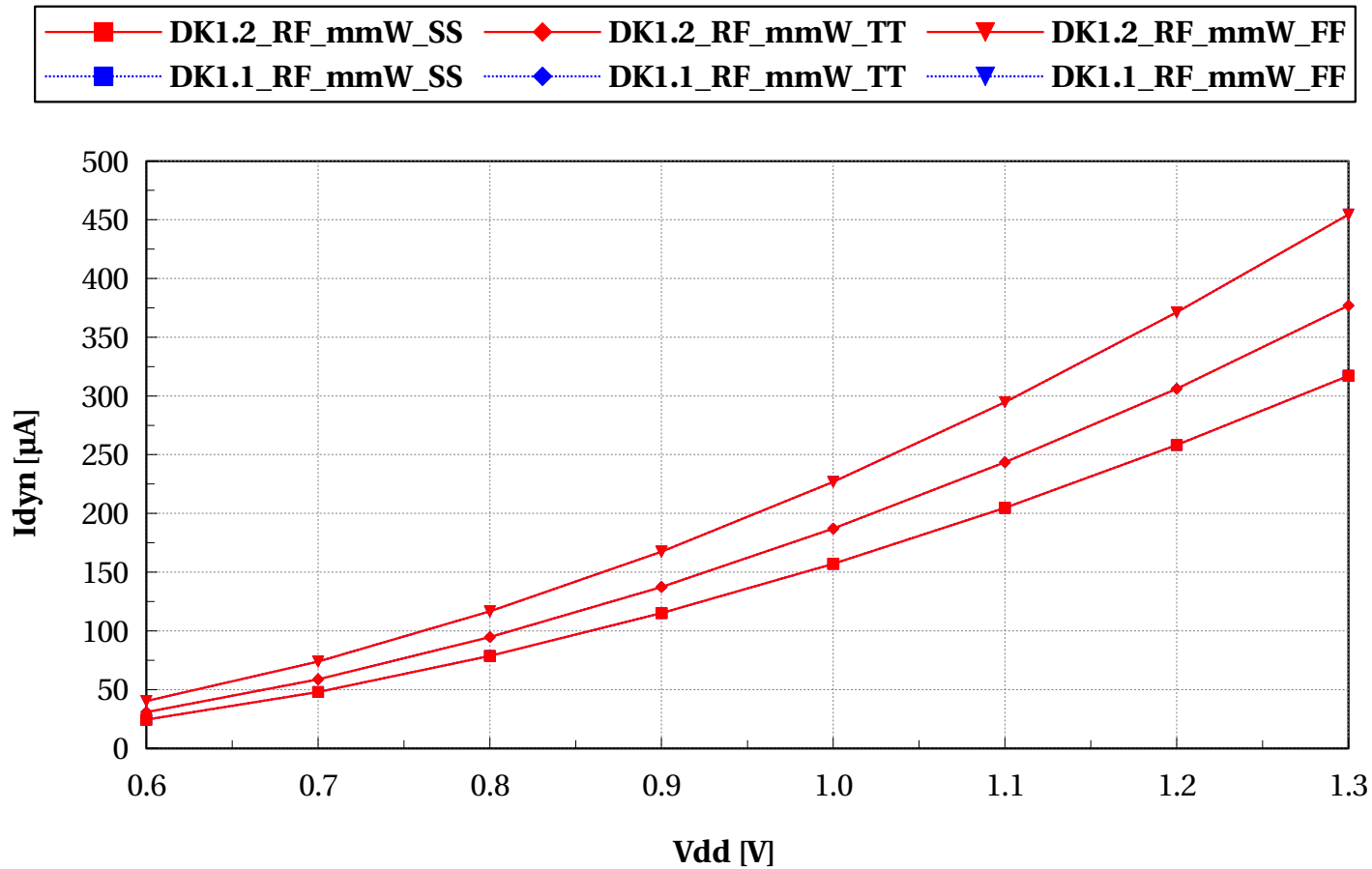
# nfet\_acc\_pfet\_acc, Taup normalized vs TT [%] vs Vdd [V]

temp==125 and p\_la\_n==0



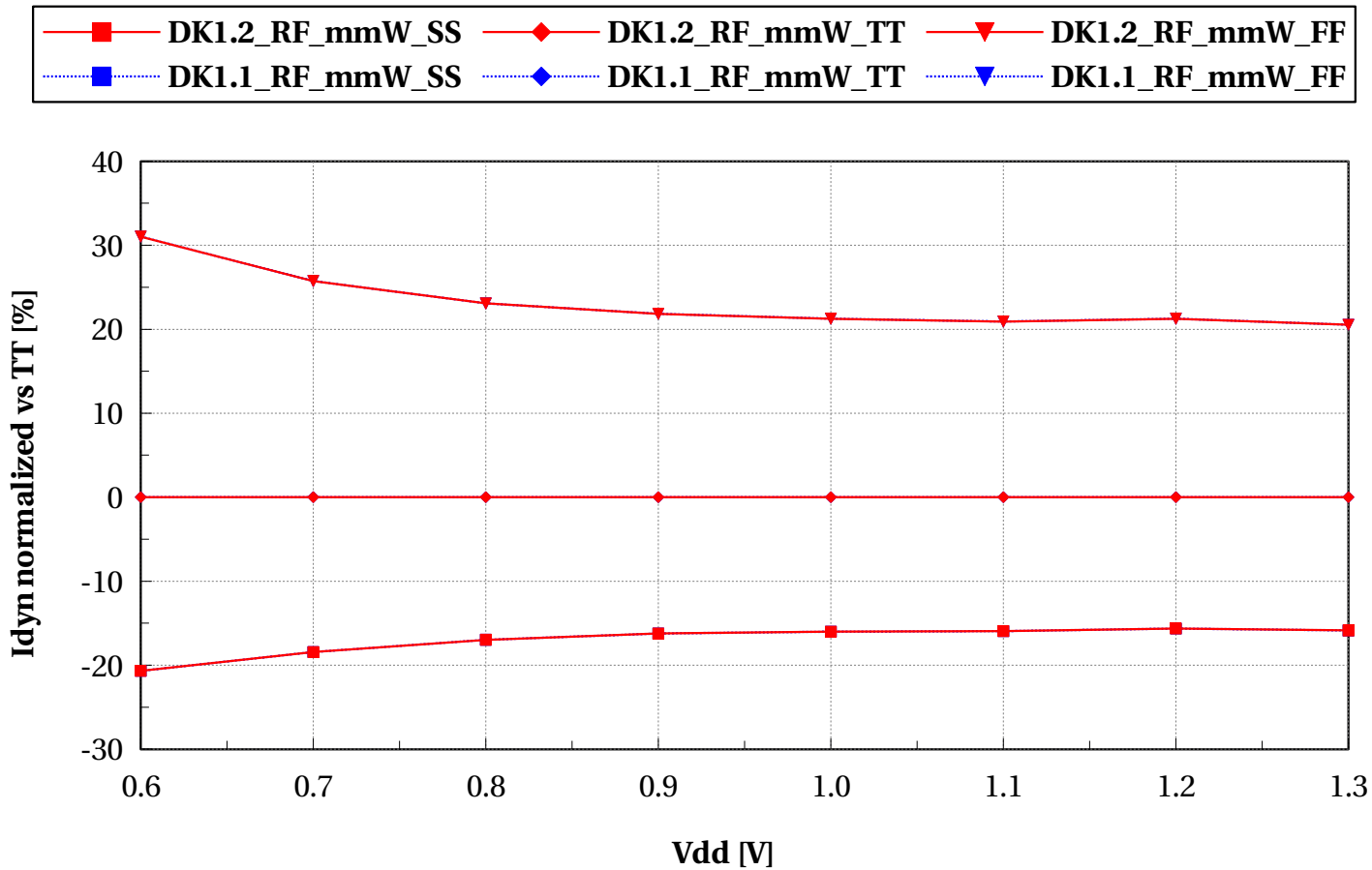
## nfet\_acc\_pfet\_acc, Idyn [ $\mu$ A] vs Vdd [V]

temp==125 and p\_la\_n==0



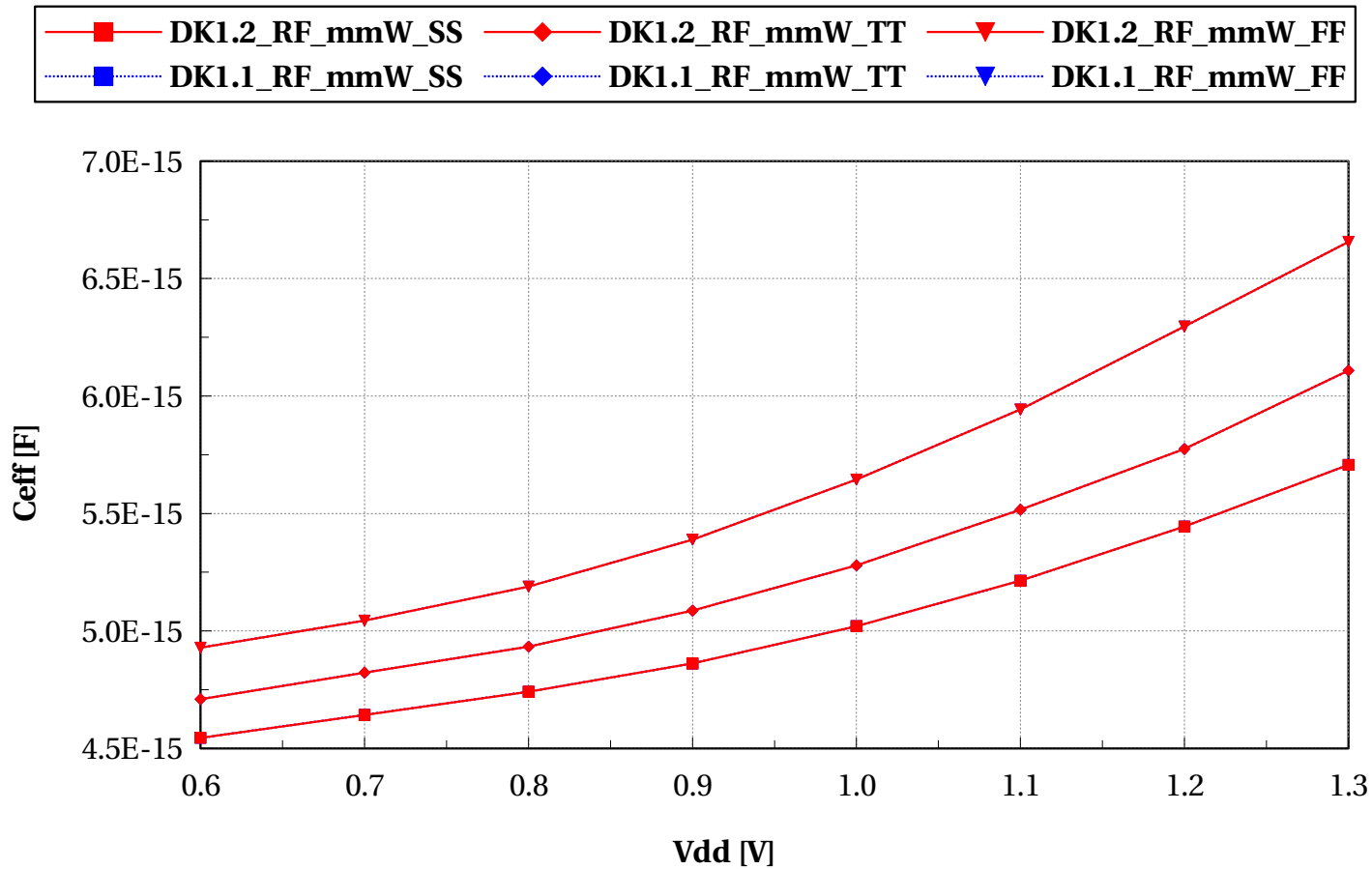
## nfet\_acc\_pfet\_acc, Idyn normalized vs TT [%] vs Vdd [V]

temp==125 and p\_la\_n==0



# nfet\_acc\_pfet\_acc, Ceff [F] vs Vdd [V]

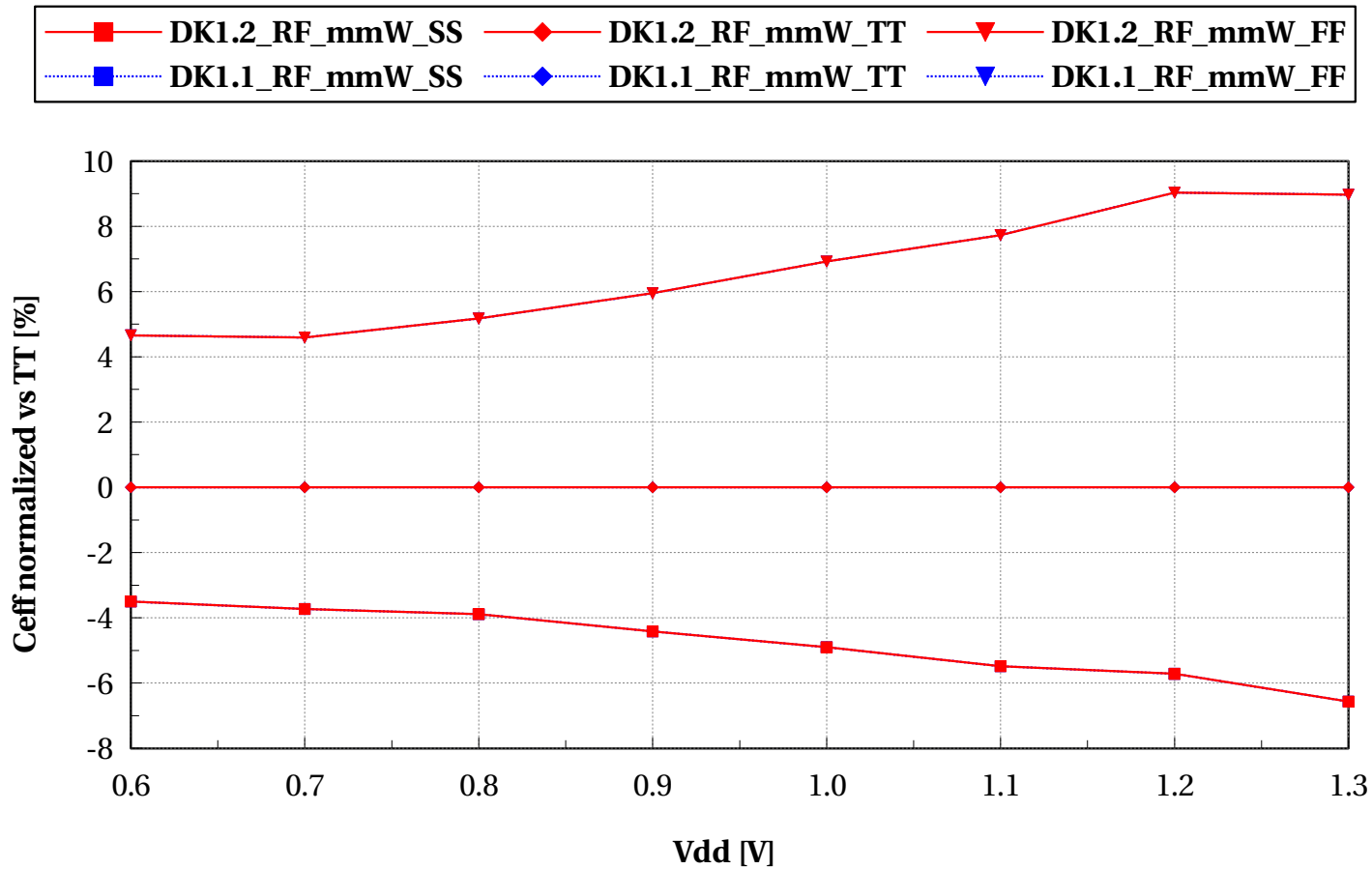
temp==125 and p\_la\_n==0





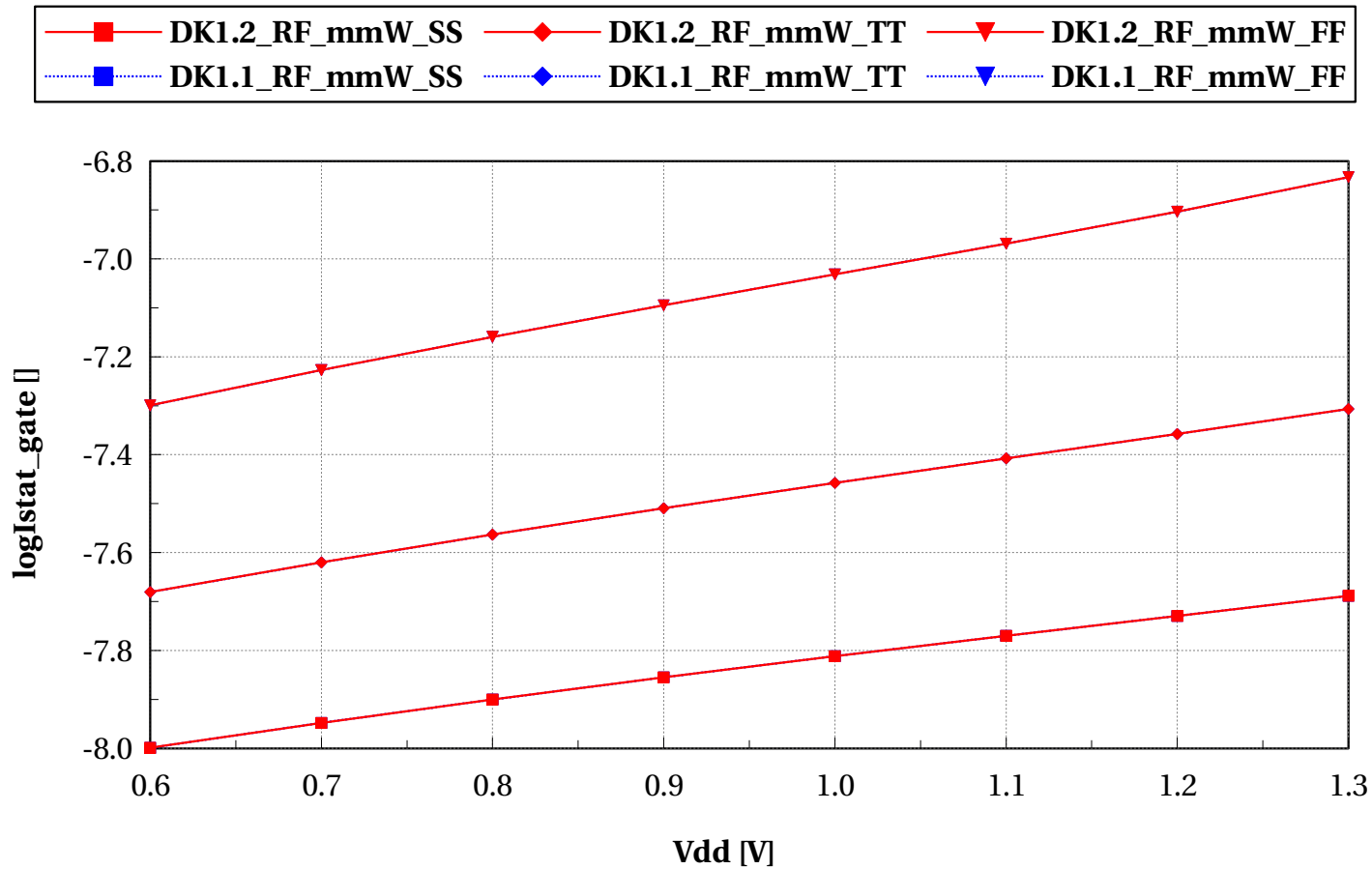
# nfet\_acc\_pfet\_acc, Ceff normalized vs TT [%] vs Vdd [V]

temp==125 and p\_la\_n==0



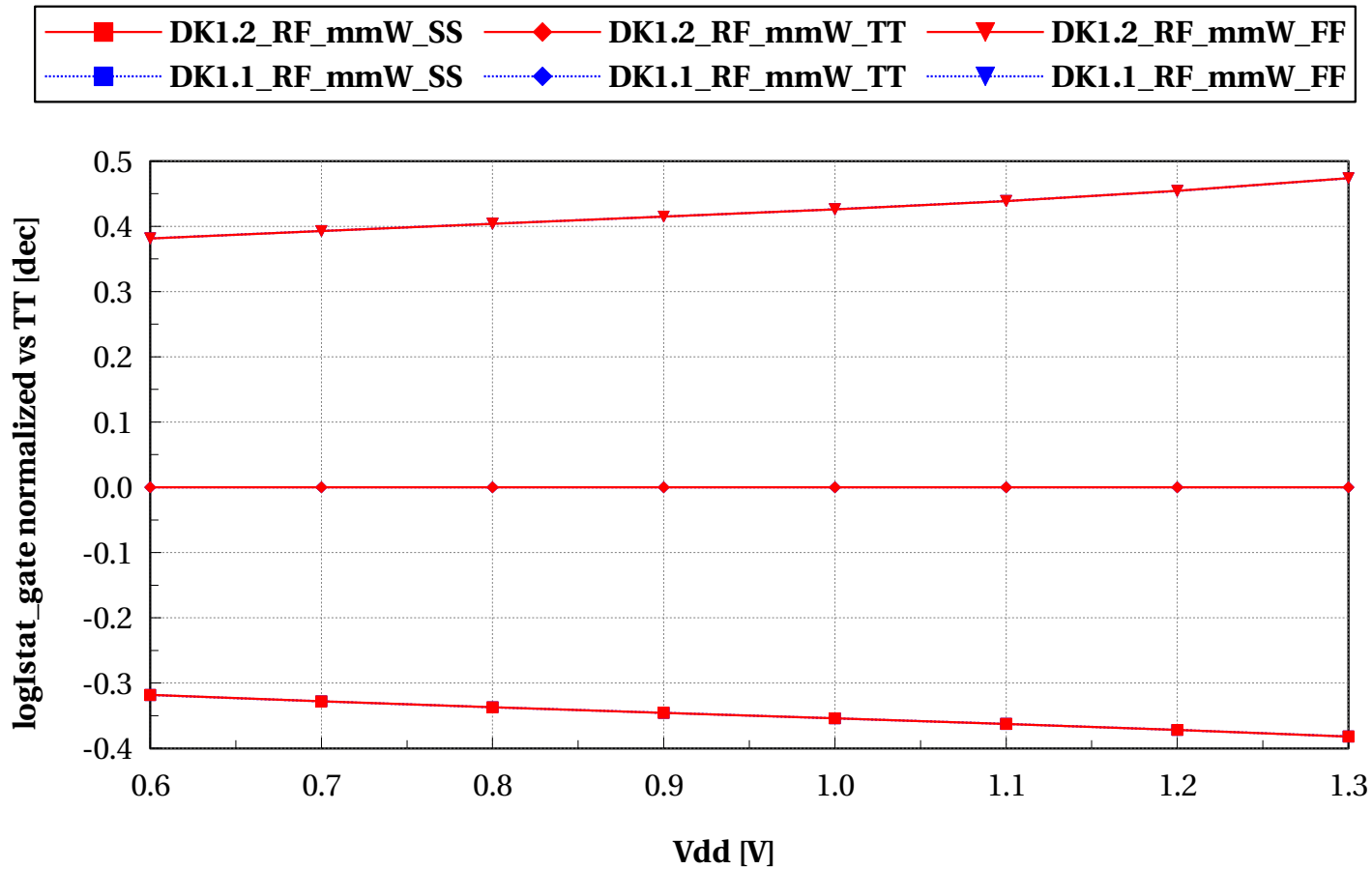
# nfet\_acc\_pfet\_acc, logIstat\_gate [] vs Vdd [V]

temp==125 and p\_la\_n==0



# nfet\_acc\_pfet\_acc, logIstat\_gate normalized vs TT [dec] vs Vdd [V]

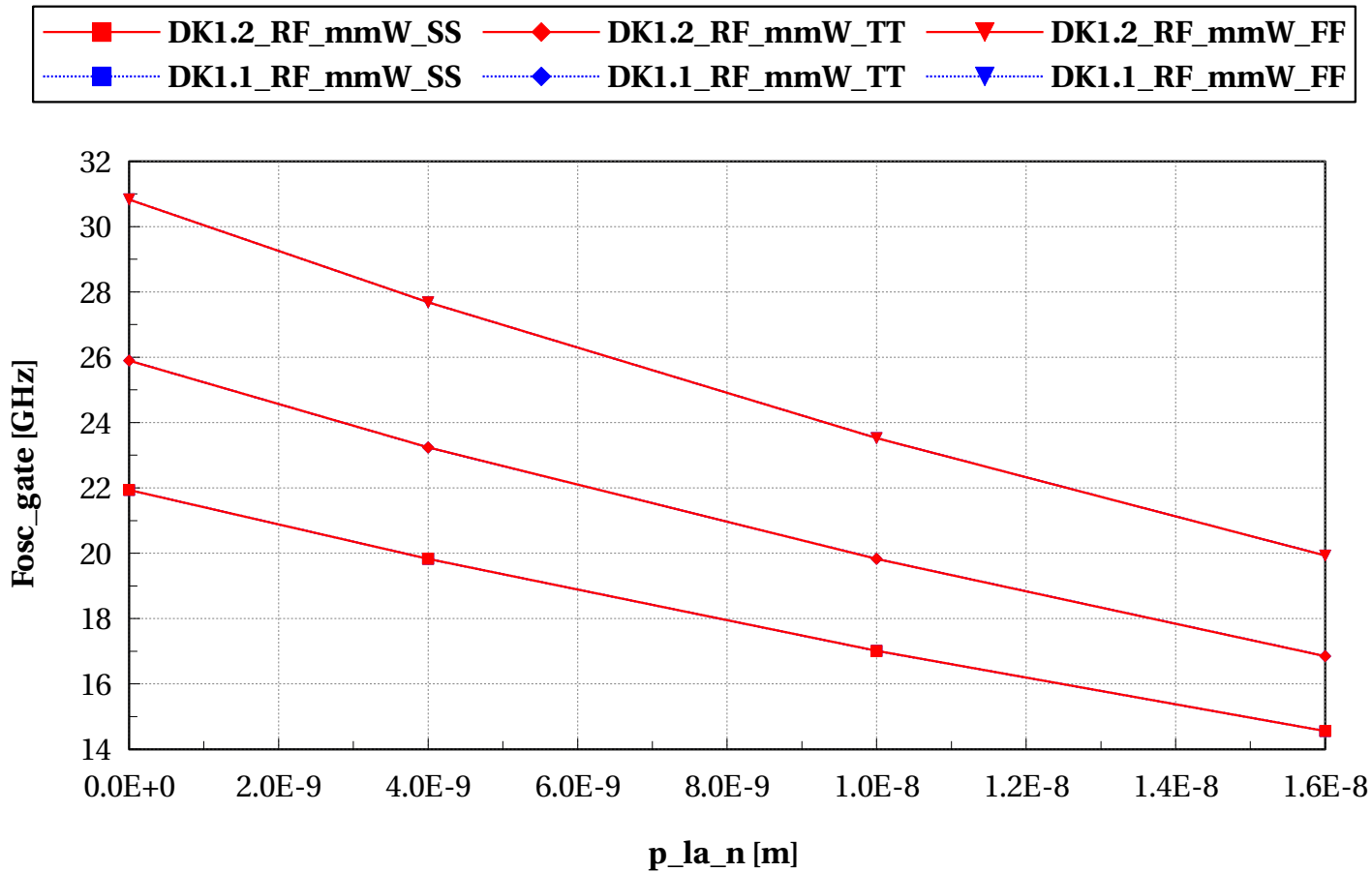
temp==125 and p\_la\_n==0



## "RO FOM's vs PB @ Vdd=0.9V, T=-40C"

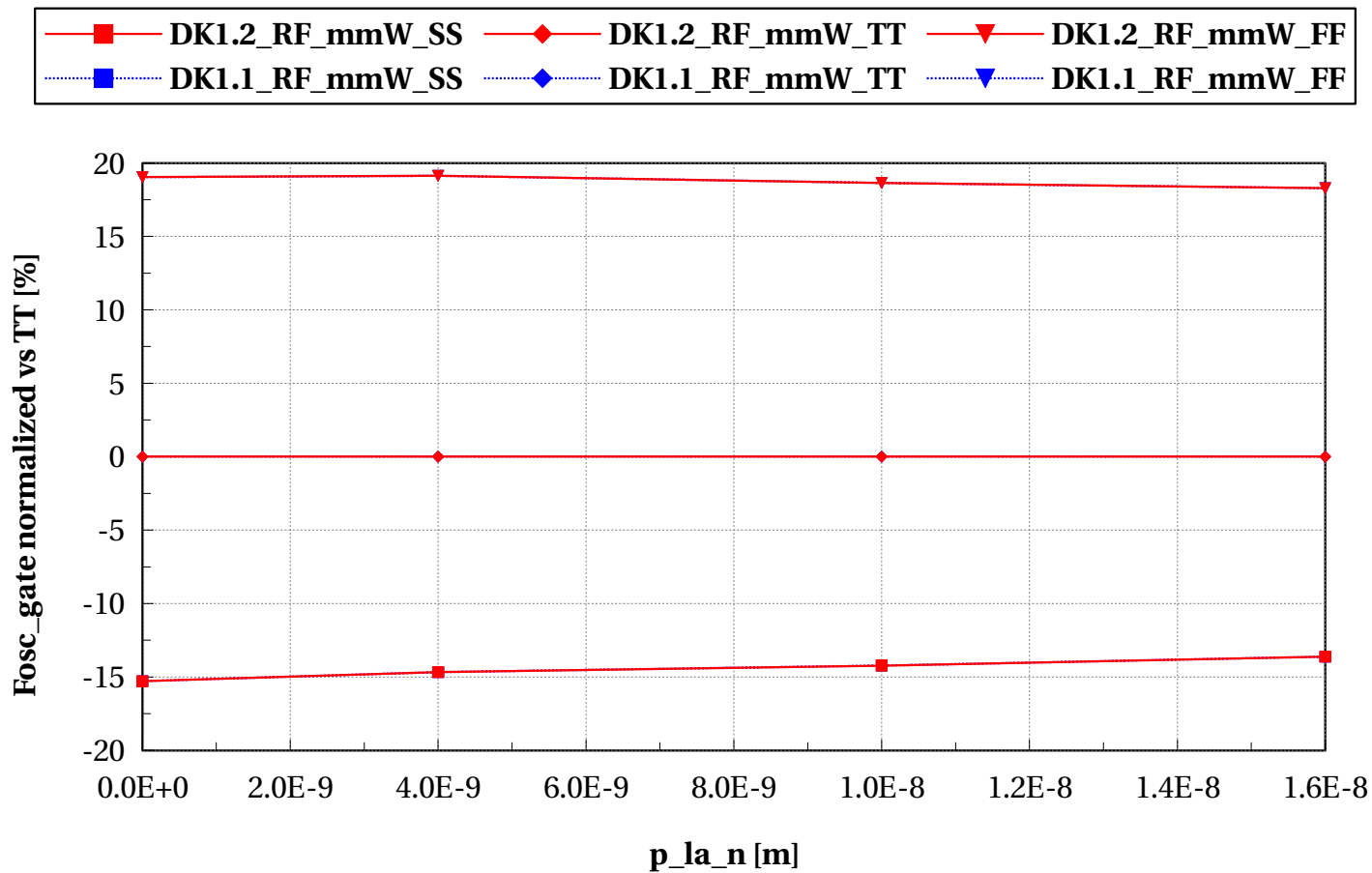
# nfet\_acc\_pfet\_acc, Fosc\_gate [GHz] vs p\_la\_n [m]

Vdd==0.9 and temp== -40



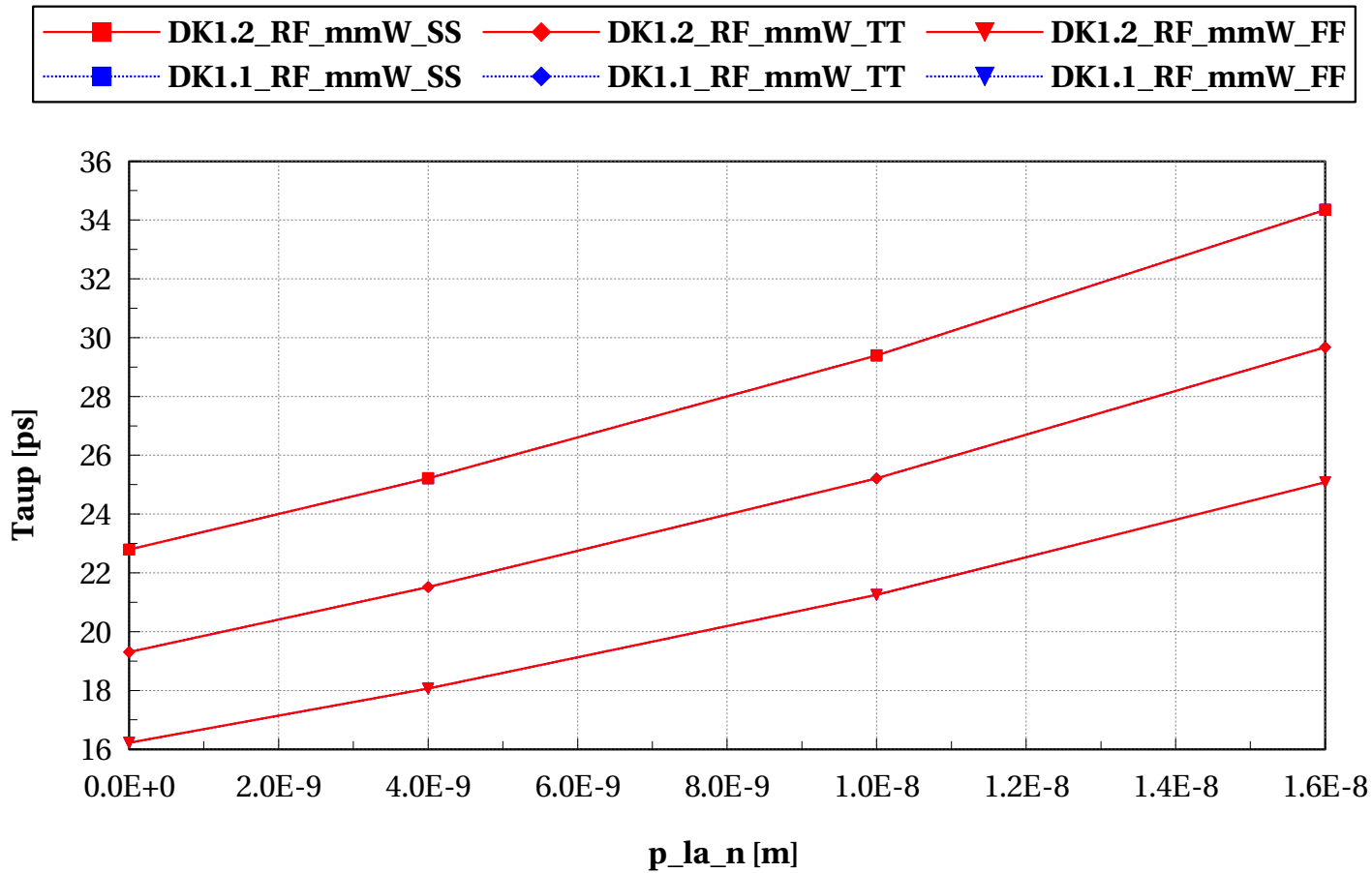
# nfet\_acc\_pfet\_acc, Fosc\_gate normalized vs TT [%] vs p\_la\_n [m]

Vdd==0.9 and temp== -40



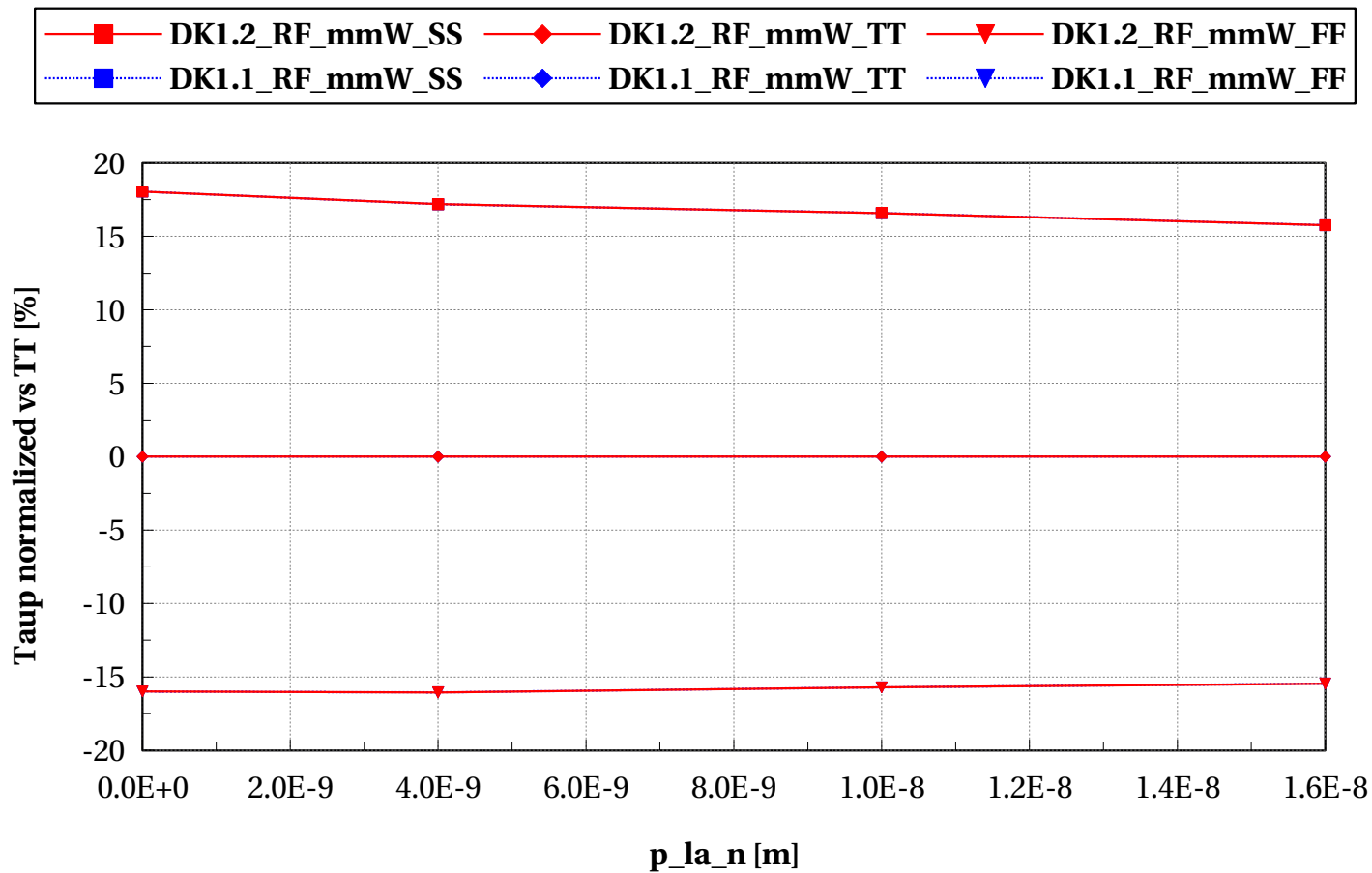
# nfet\_acc\_pfet\_acc, Taup [ps] vs p\_la\_n [m]

Vdd==0.9 and temp== -40



# nfet\_acc\_pfet\_acc, Taup normalized vs TT [%] vs p\_la\_n [m]

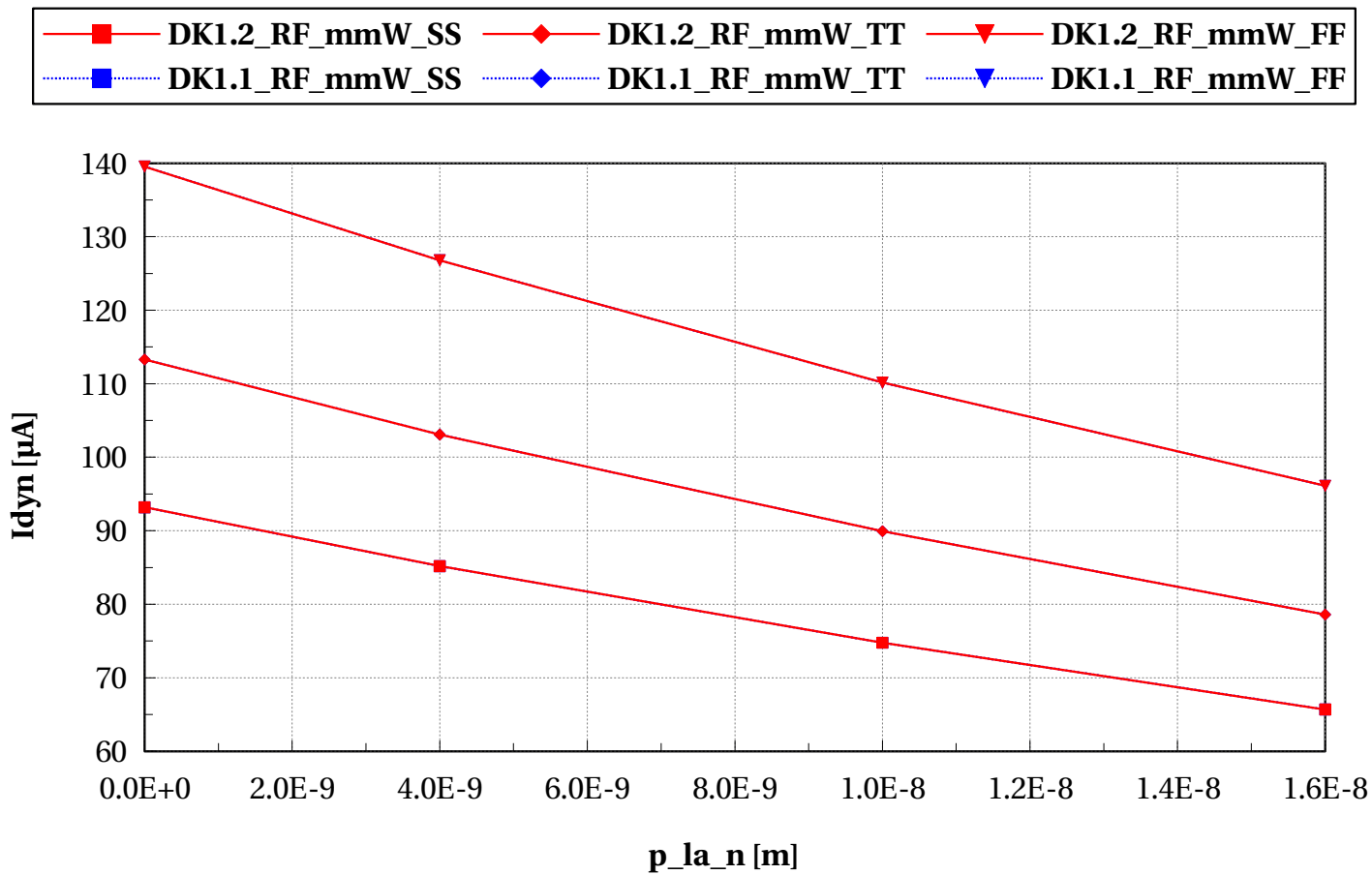
Vdd==0.9 and temp== -40





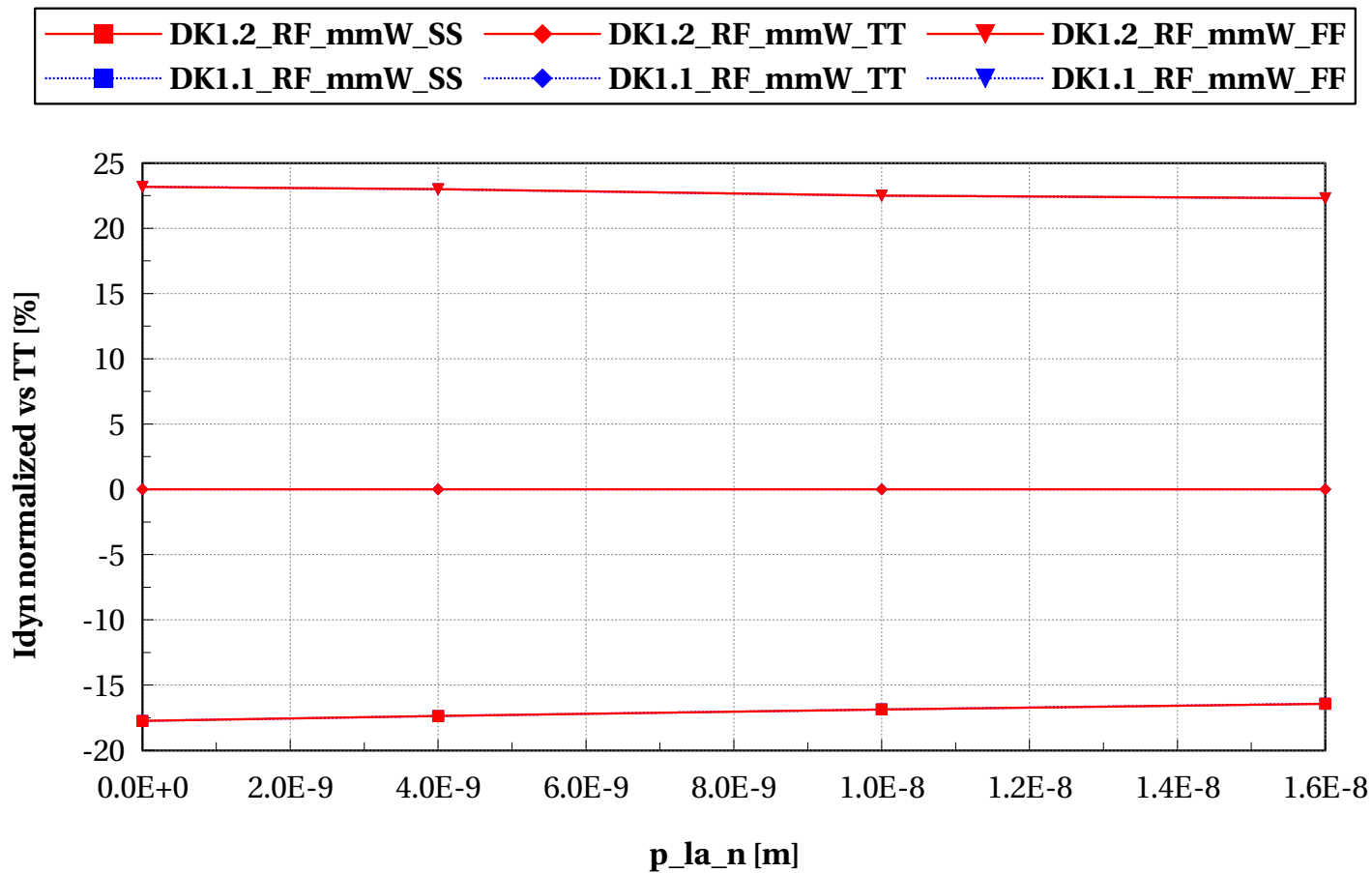
# nfet\_acc\_pfet\_acc, Idyn [ $\mu$ A] vs p\_la\_n [m]

Vdd==0.9 and temp== -40



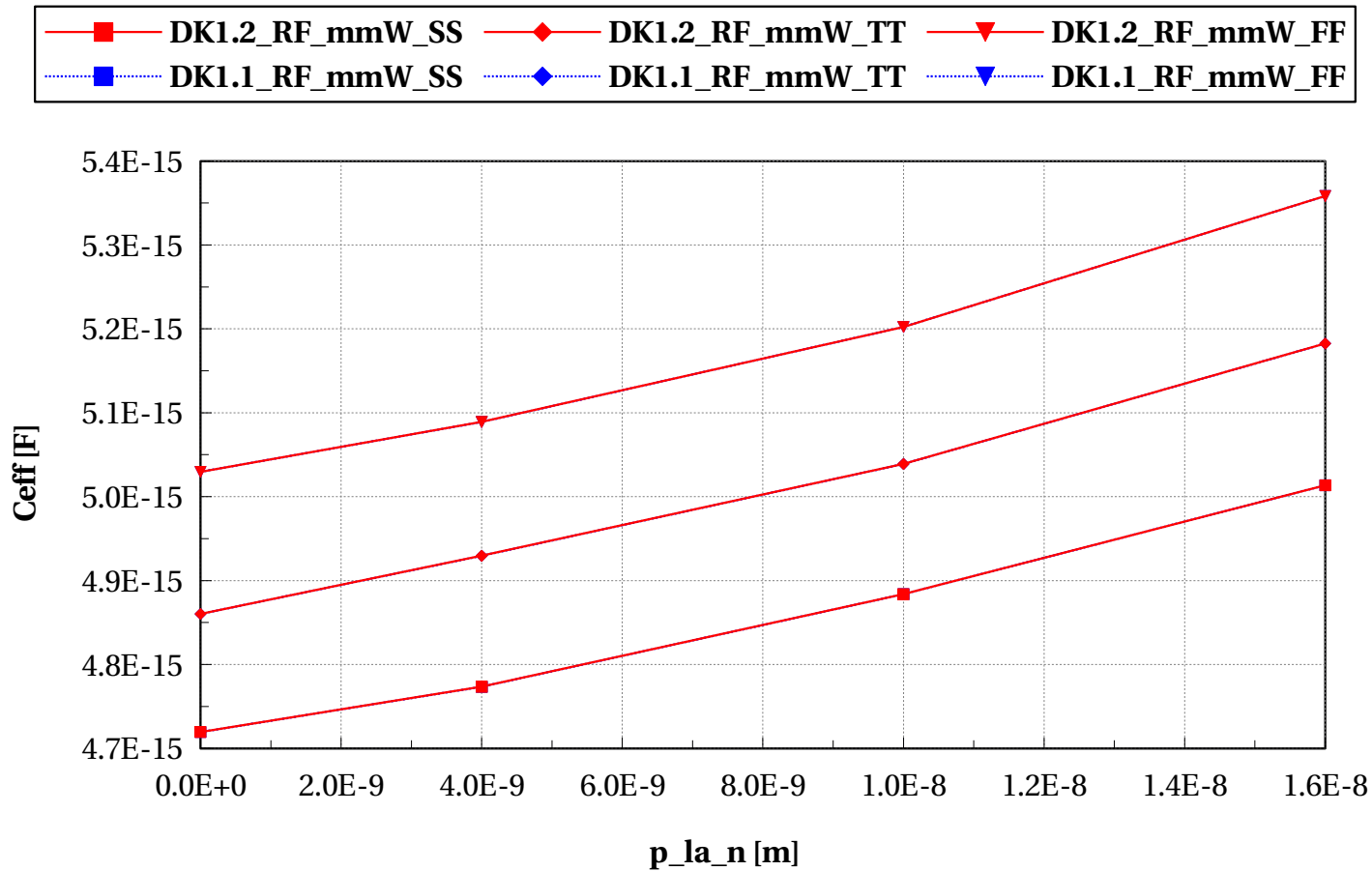
# nfet\_acc\_pfet\_acc, Idyn normalized vs TT [%] vs p\_la\_n [m]

Vdd==0.9 and temp== -40



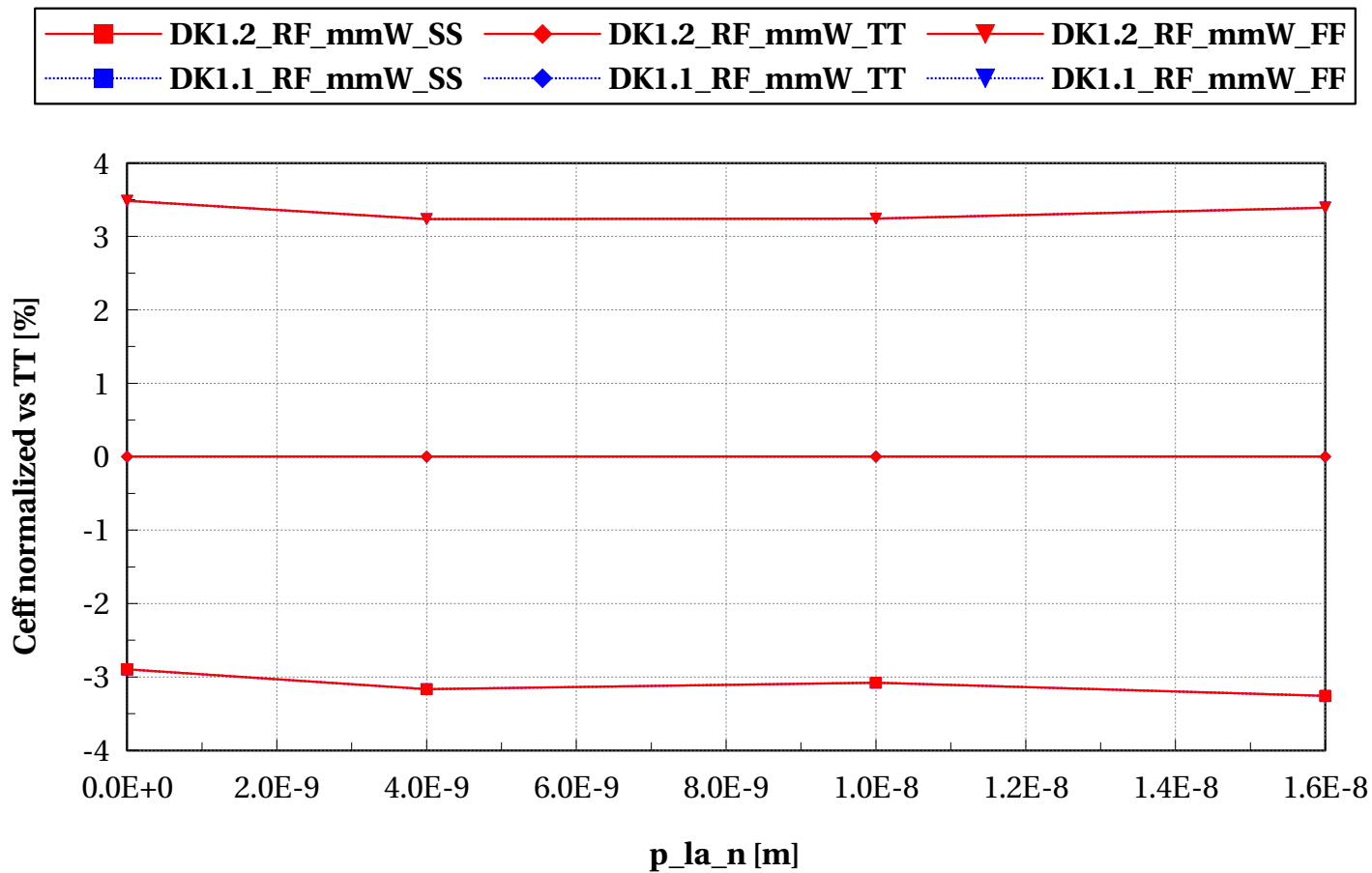
# nfet\_acc\_pfet\_acc, Ceff [F] vs p\_la\_n [m]

Vdd==0.9 and temp== -40



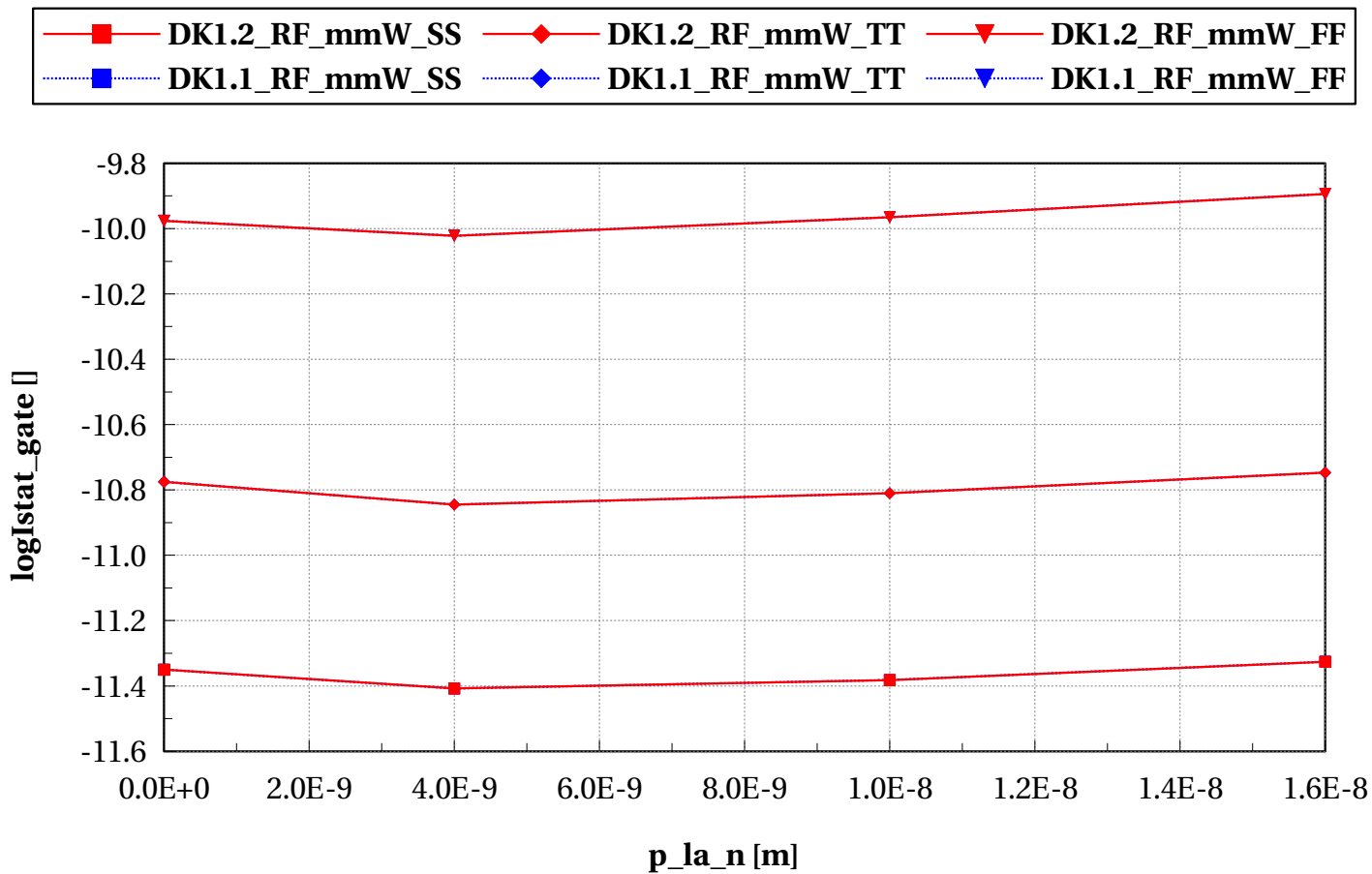
# nfet\_acc\_pfet\_acc, Ceff normalized vs TT [%] vs p\_la\_n [m]

Vdd==0.9 and temp== -40



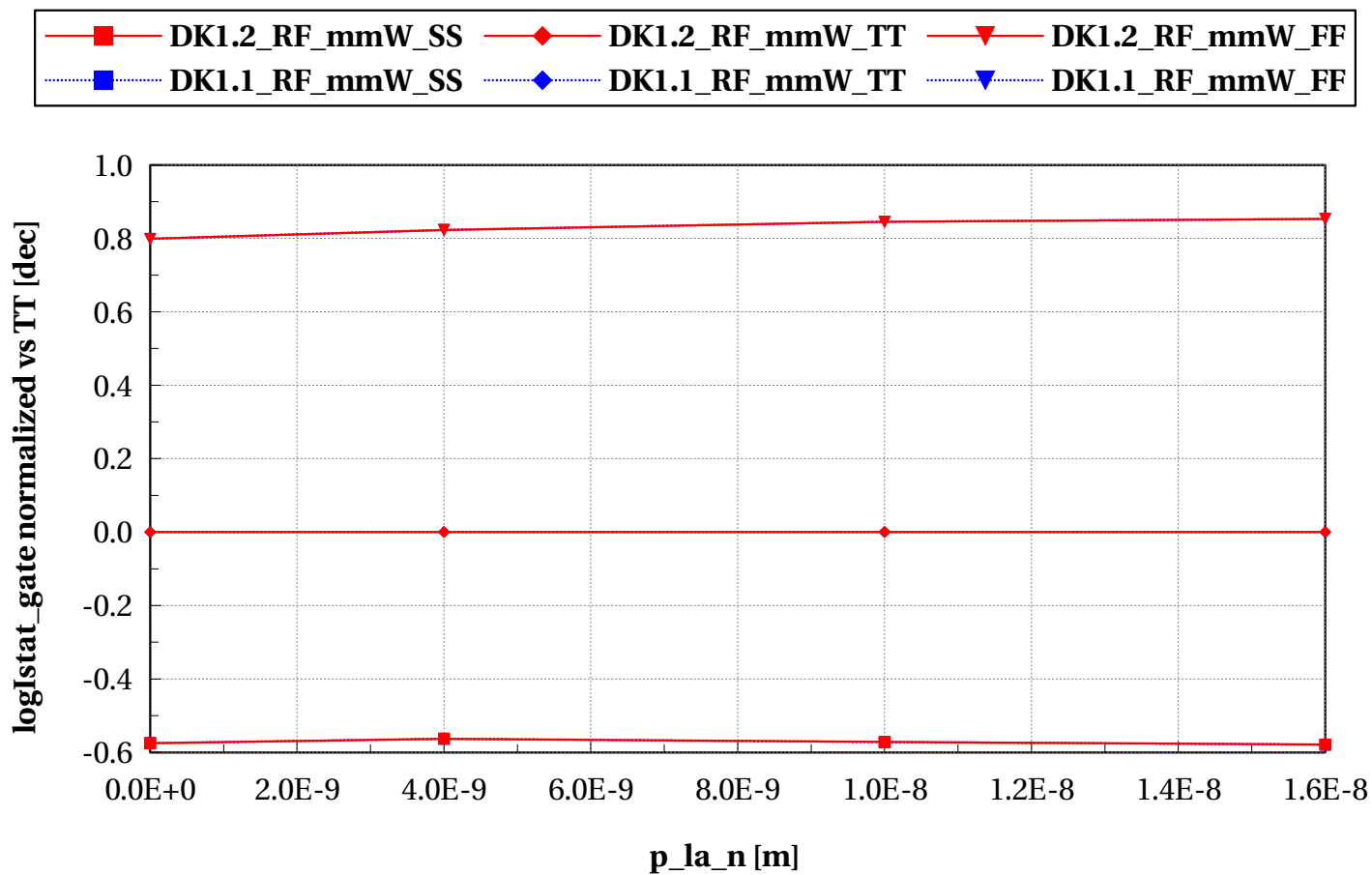
# nfet\_acc\_pfet\_acc, logIstat\_gate [] vs p\_la\_n [m]

Vdd==0.9 and temp== -40



# nfet\_acc\_pfet\_acc, logIstat\_gate normalized vs TT [dec] vs p\_la\_n [m]

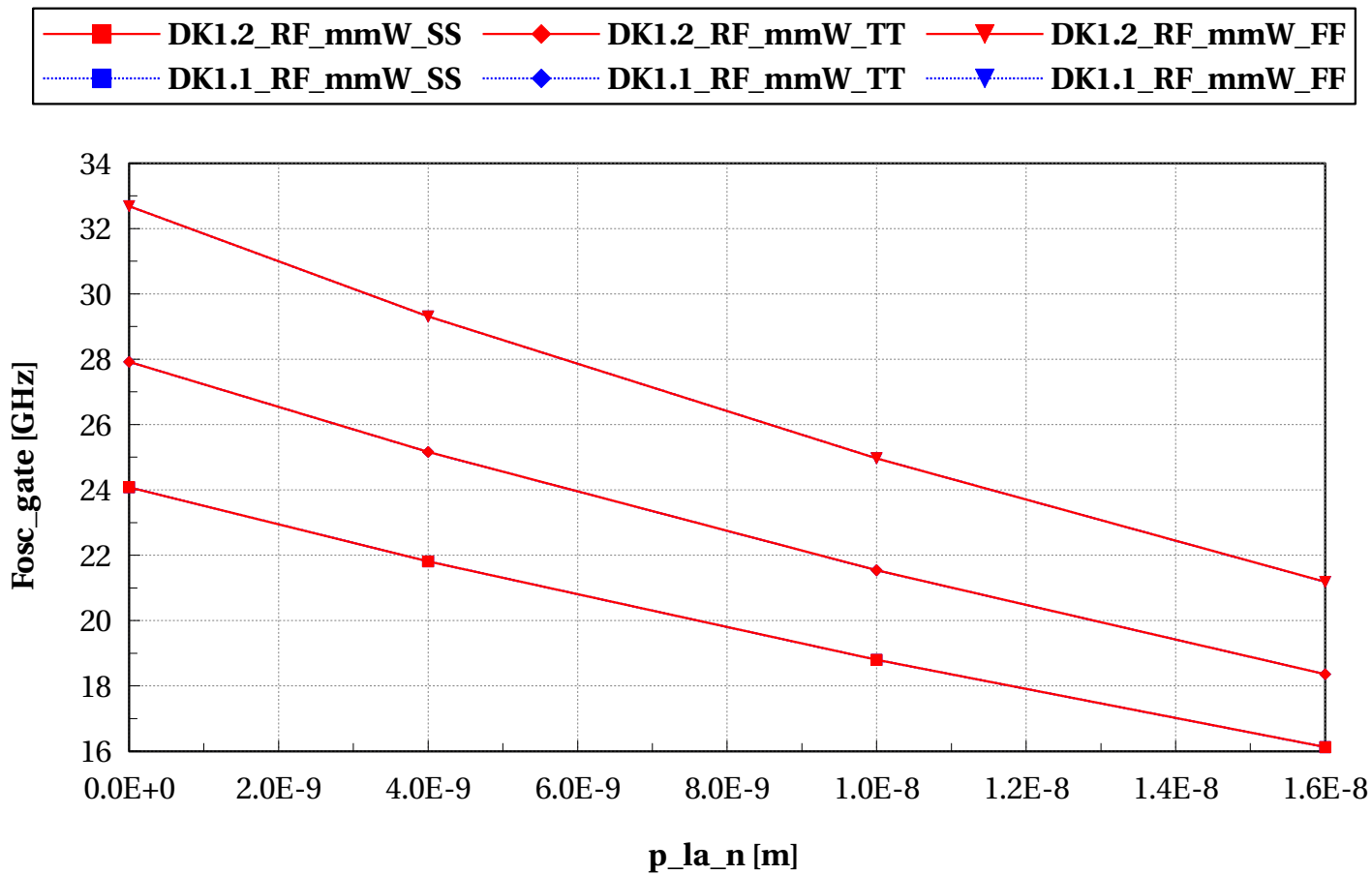
Vdd==0.9 and temp== -40



## "RO FOM's vs PB @ Vdd=0.9V, T=25C"

# nfet\_acc\_pfet\_acc, Fosc\_gate [GHz] vs p\_la\_n [m]

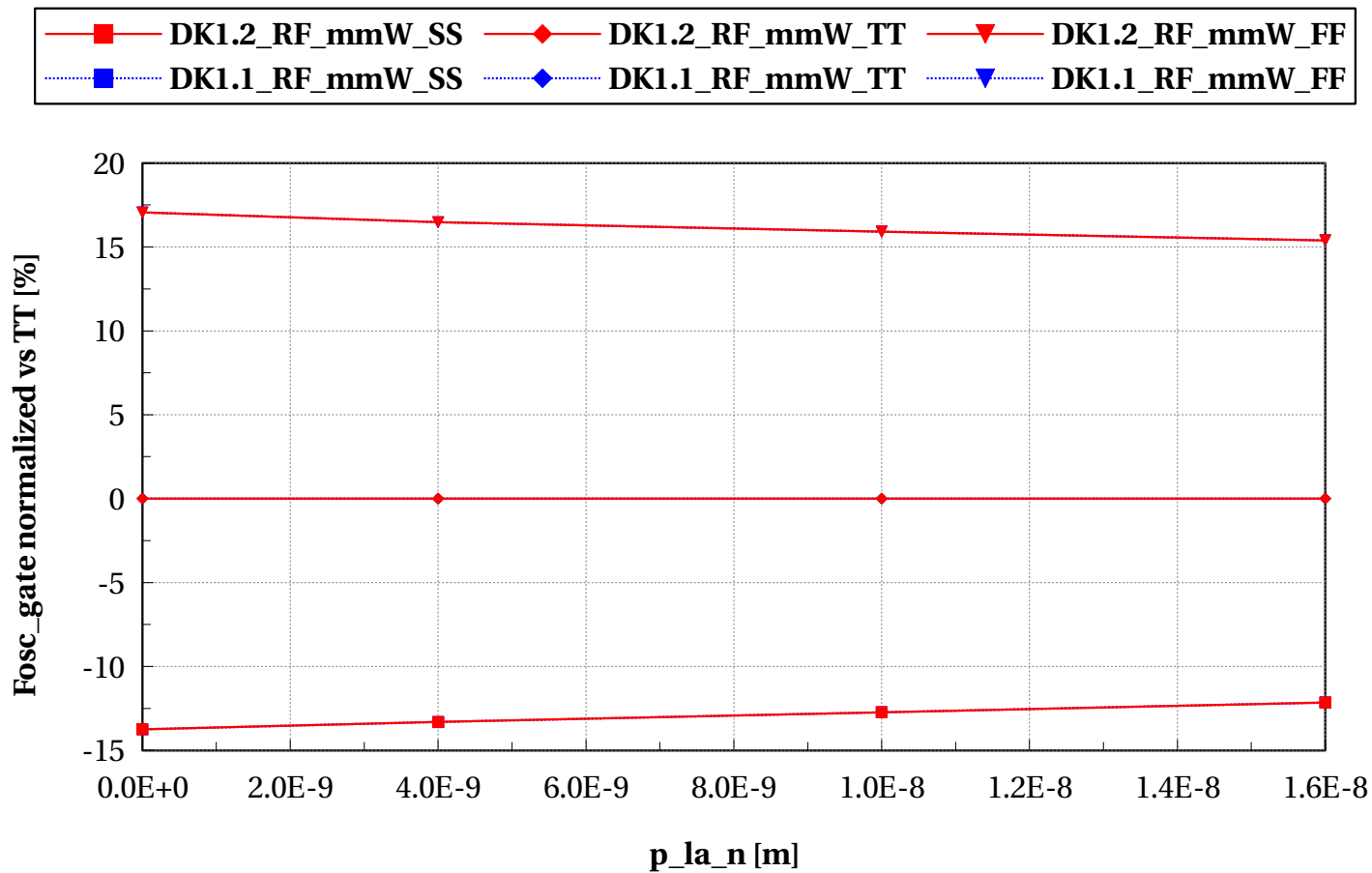
Vdd==0.9 and temp==25





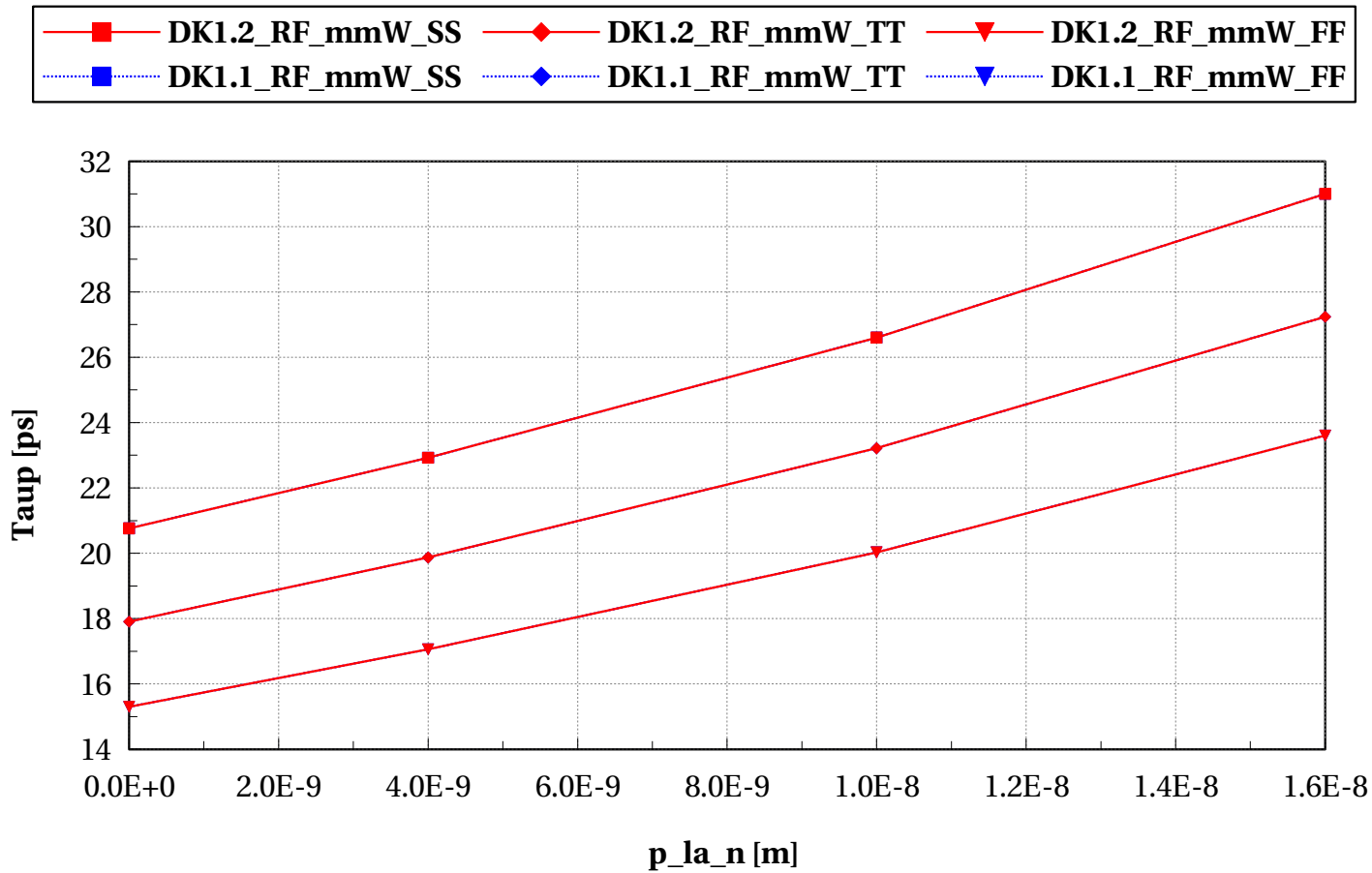
# nfet\_acc\_pfet\_acc, Fosc\_gate normalized vs TT [%] vs p\_la\_n [m]

Vdd==0.9 and temp==25



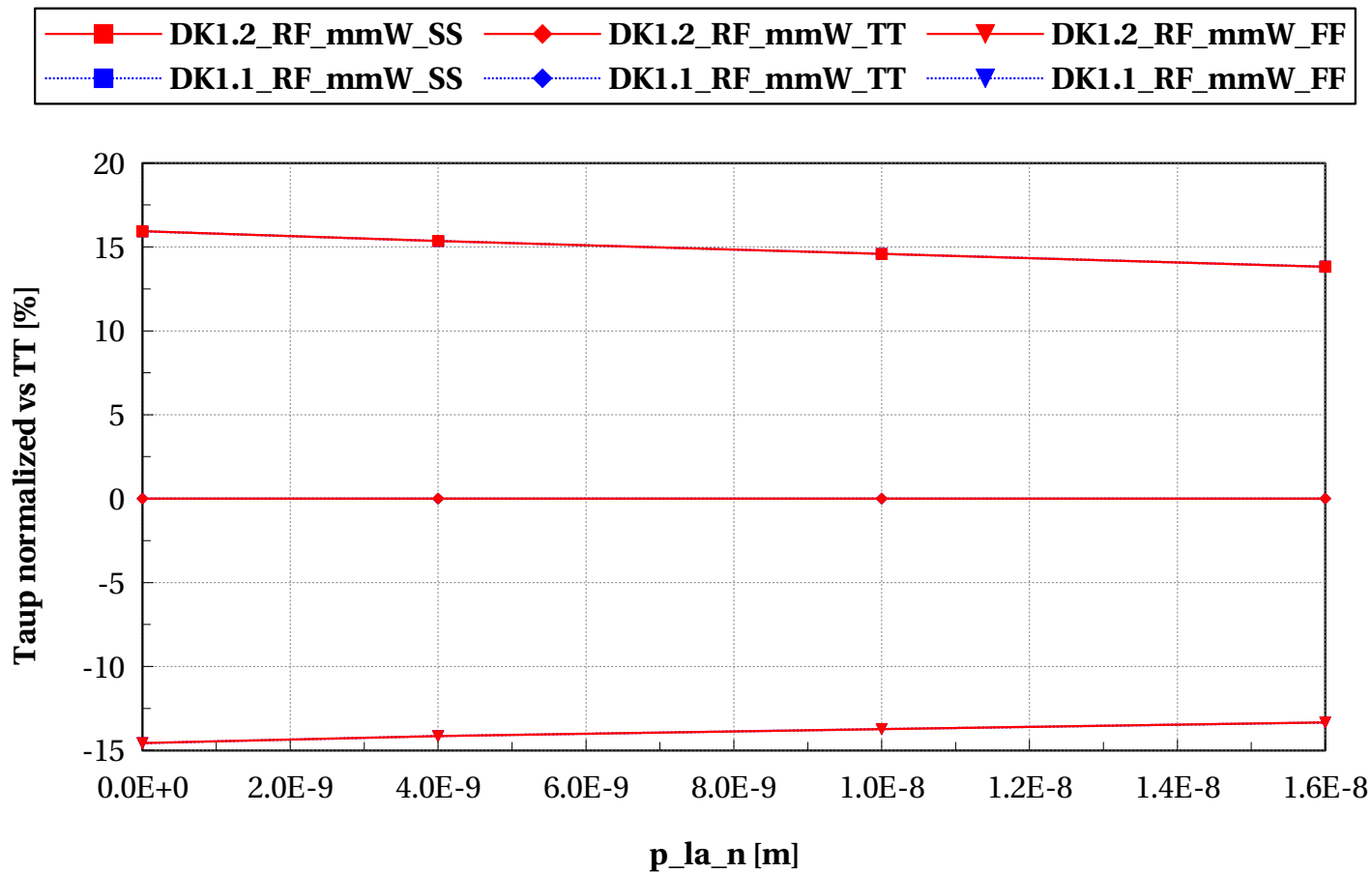
# nfet\_acc\_pfet\_acc, Taup [ps] vs p\_la\_n [m]

Vdd==0.9 and temp==25



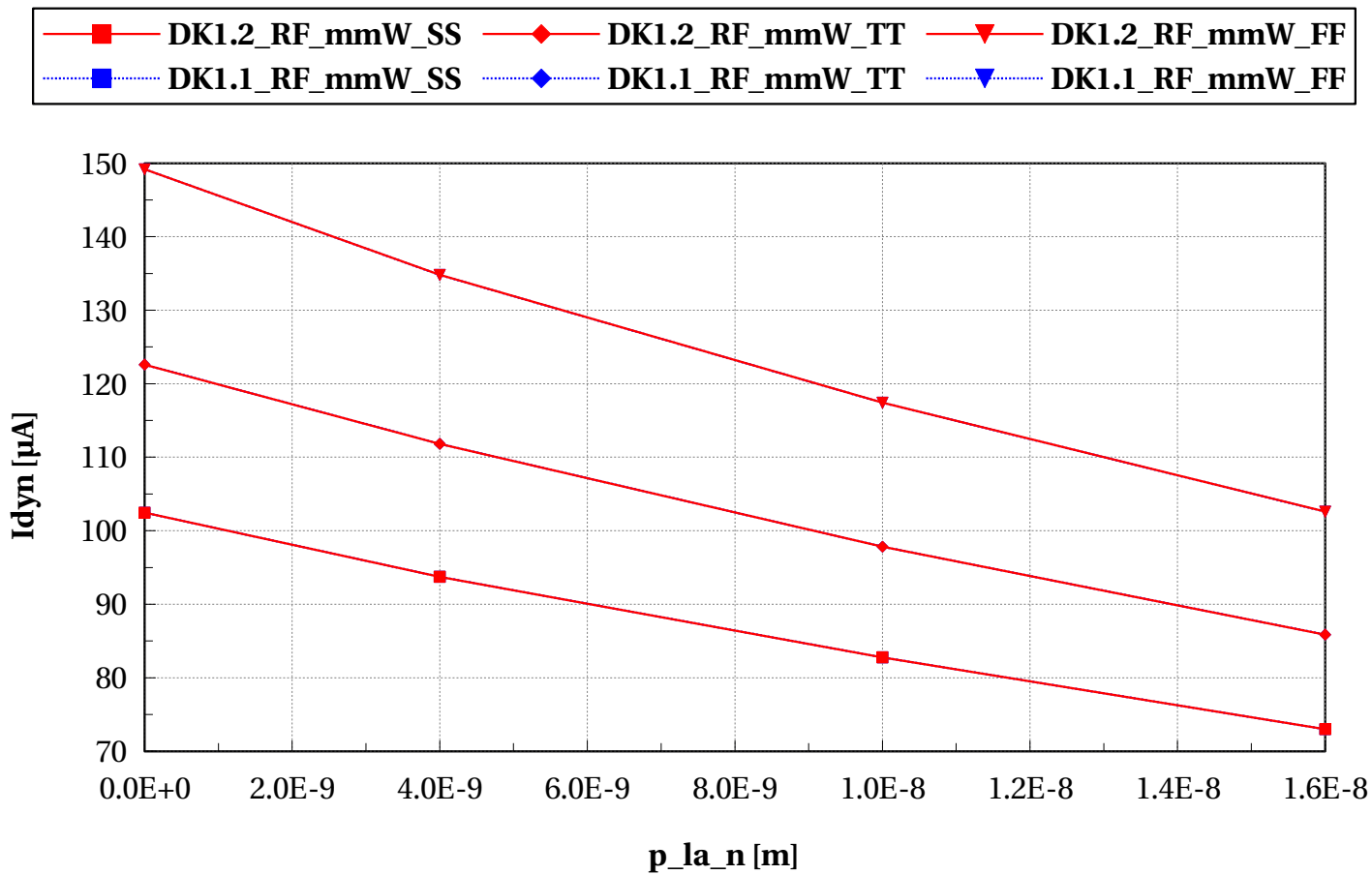
# nfet\_acc\_pfet\_acc, Taup normalized vs TT [%] vs p\_la\_n [m]

Vdd==0.9 and temp==25



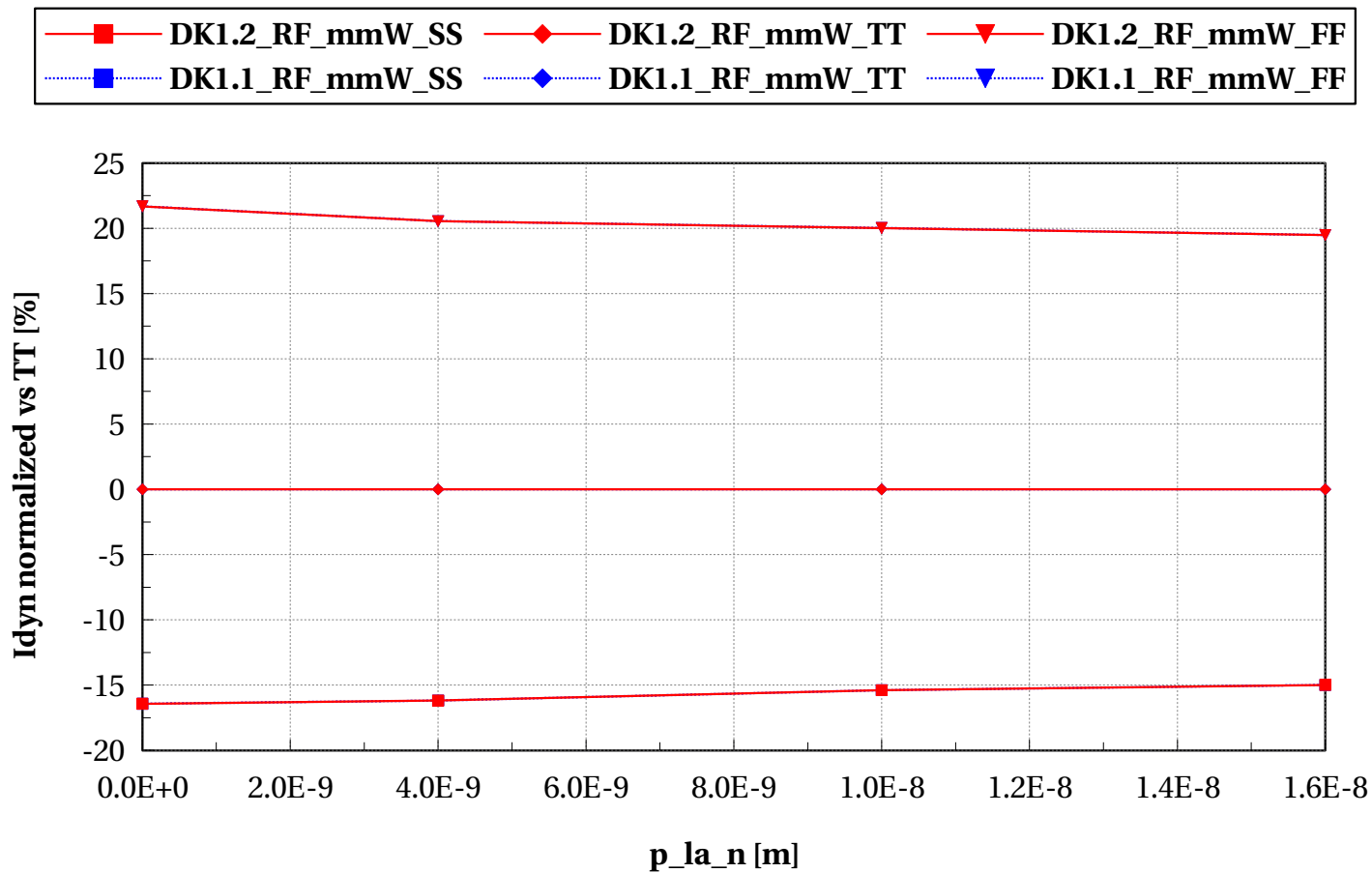
# nfet\_acc\_pfet\_acc, Idyn [ $\mu$ A] vs p\_la\_n [m]

Vdd==0.9 and temp==25



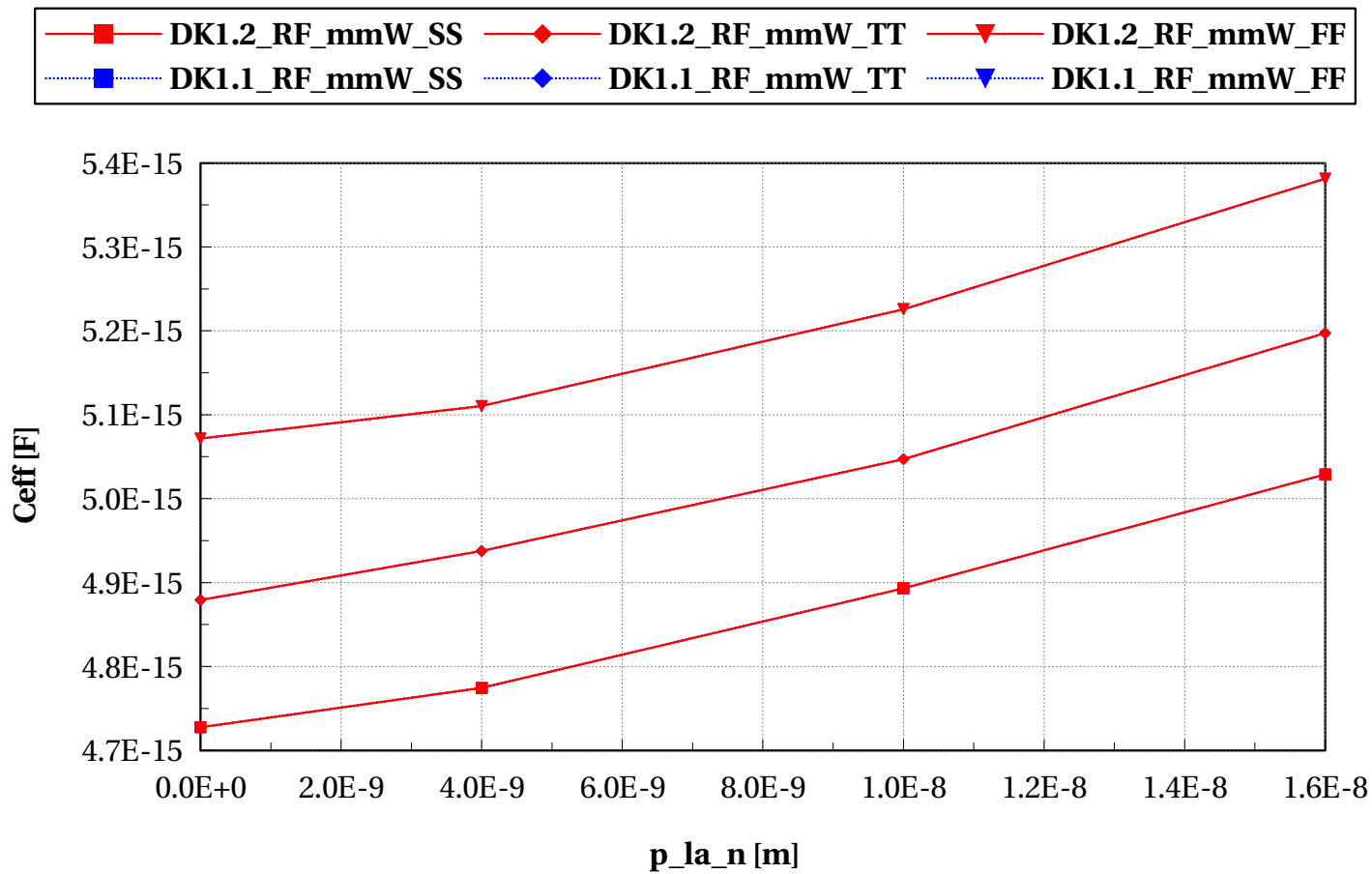
# **nfet\_acc\_pfet\_acc, Idyn normalized vs TT [%] vs p\_la\_n [m]**

Vdd==0.9 and temp==25



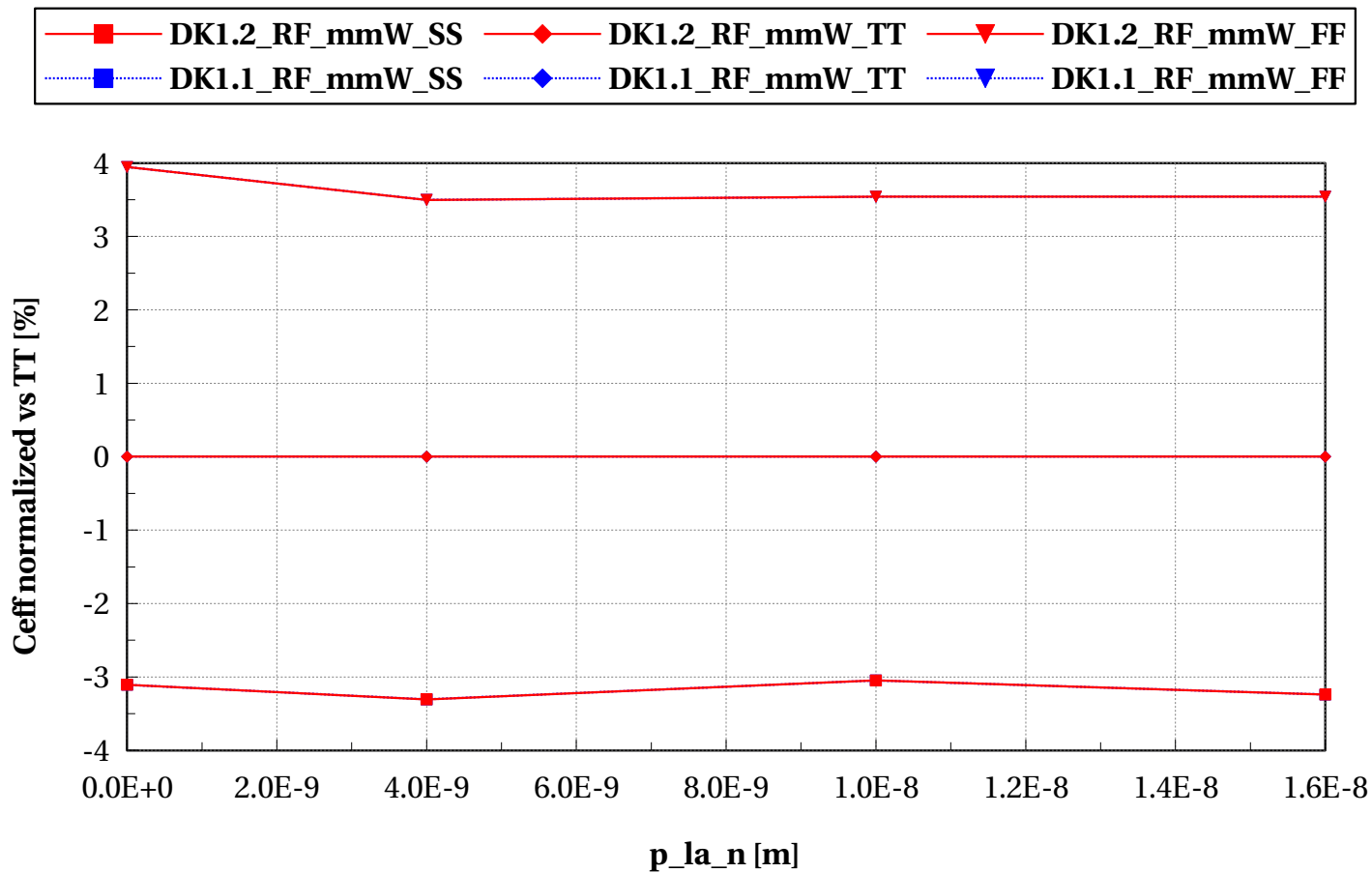
# nfet\_acc\_pfet\_acc, Ceff [F] vs p\_la\_n [m]

Vdd==0.9 and temp==25



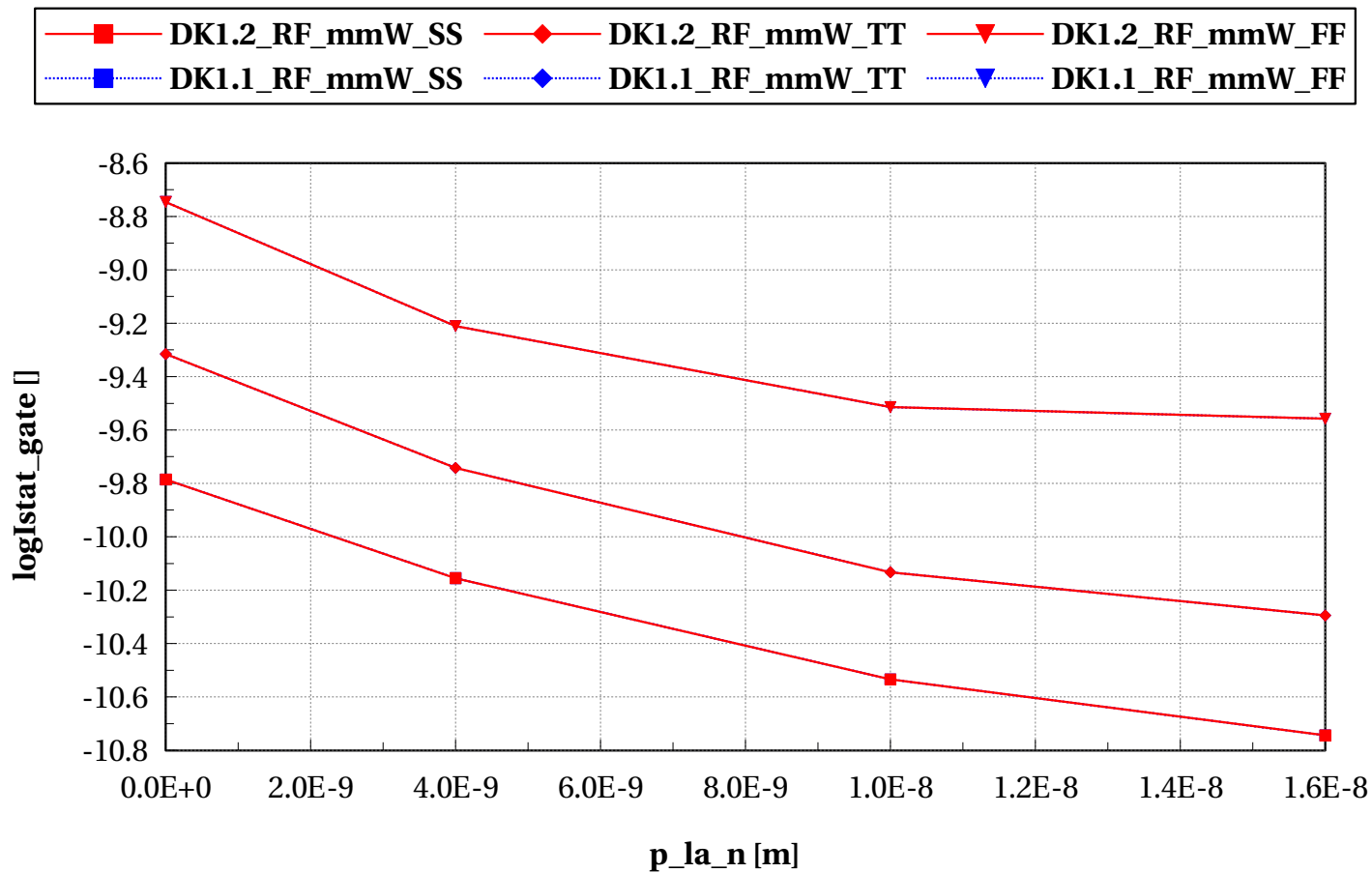
# nfet\_acc\_pfet\_acc, Ceff normalized vs TT [%] vs p\_la\_n [m]

Vdd==0.9 and temp==25



# nfet\_acc\_pfet\_acc, logIstat\_gate [] vs p\_la\_n [m]

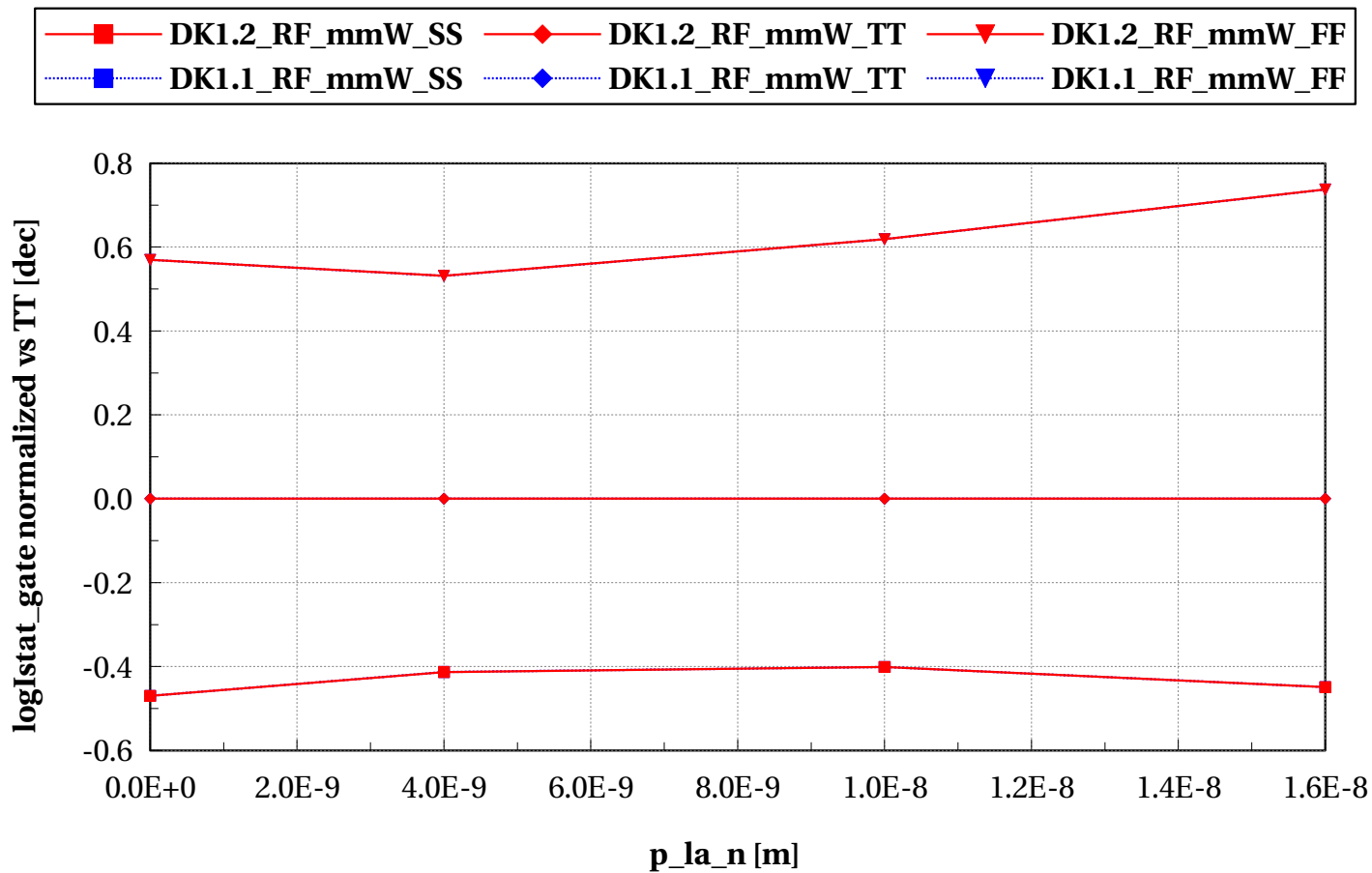
Vdd==0.9 and temp==25





# nfet\_acc\_pfet\_acc, logIstat\_gate normalized vs TT [dec] vs p\_la\_n [m]

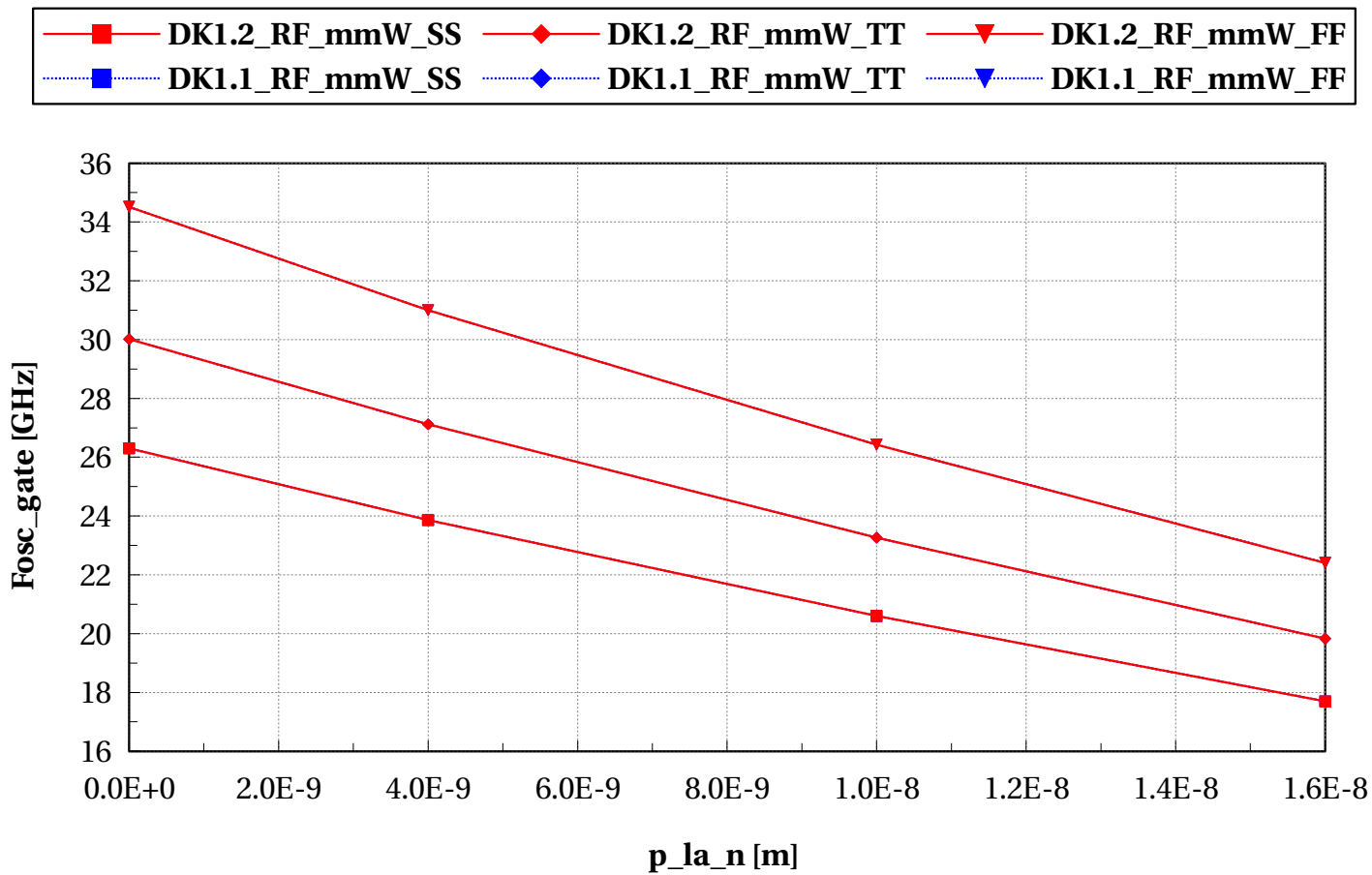
Vdd==0.9 and temp==25



## "RO FOM's vs PB @ Vdd=0.9V, T=125C"

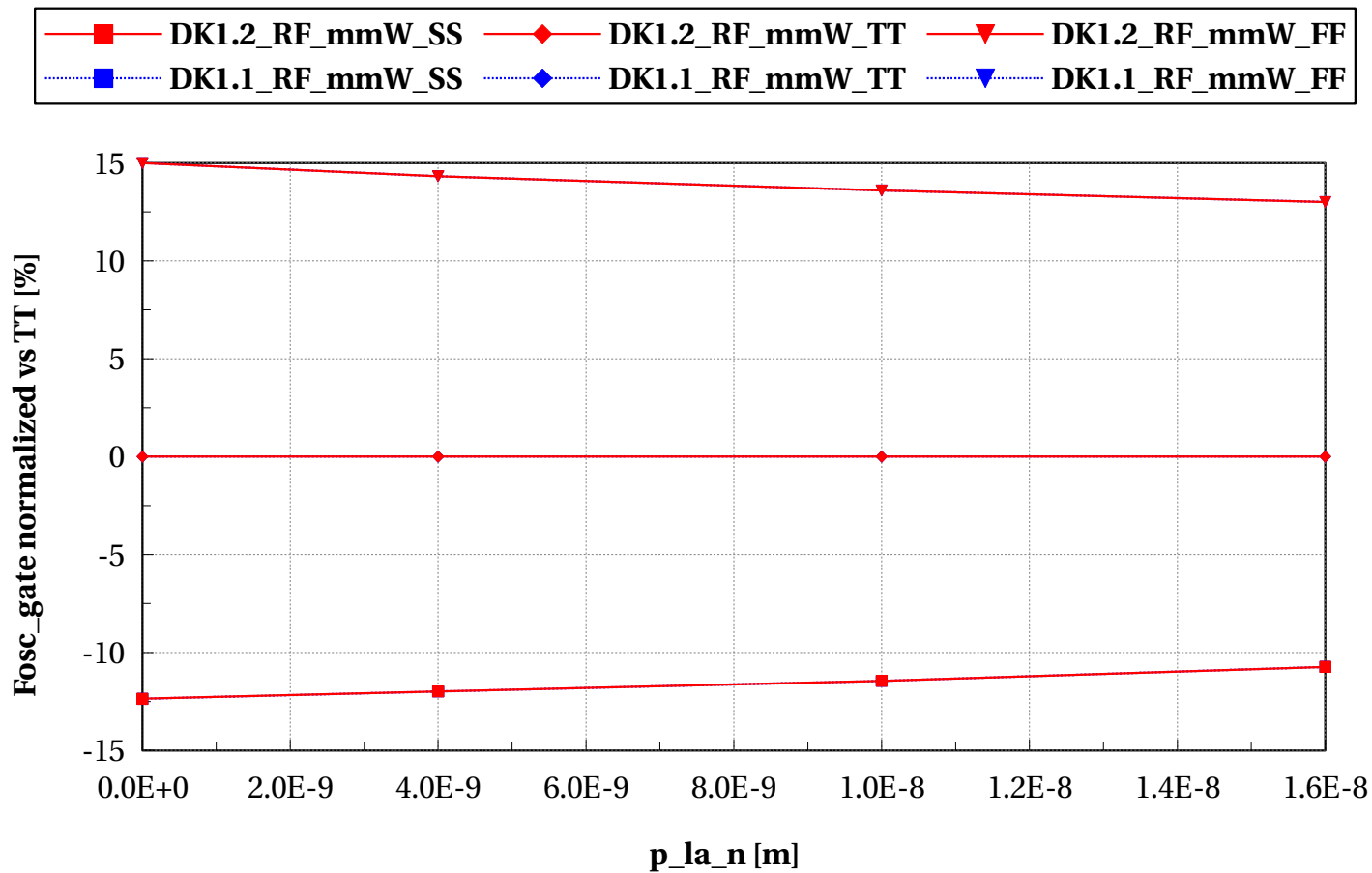
# nfet\_acc\_pfet\_acc, Fosc\_gate [GHz] vs p\_la\_n [m]

Vdd==0.9 and temp==125



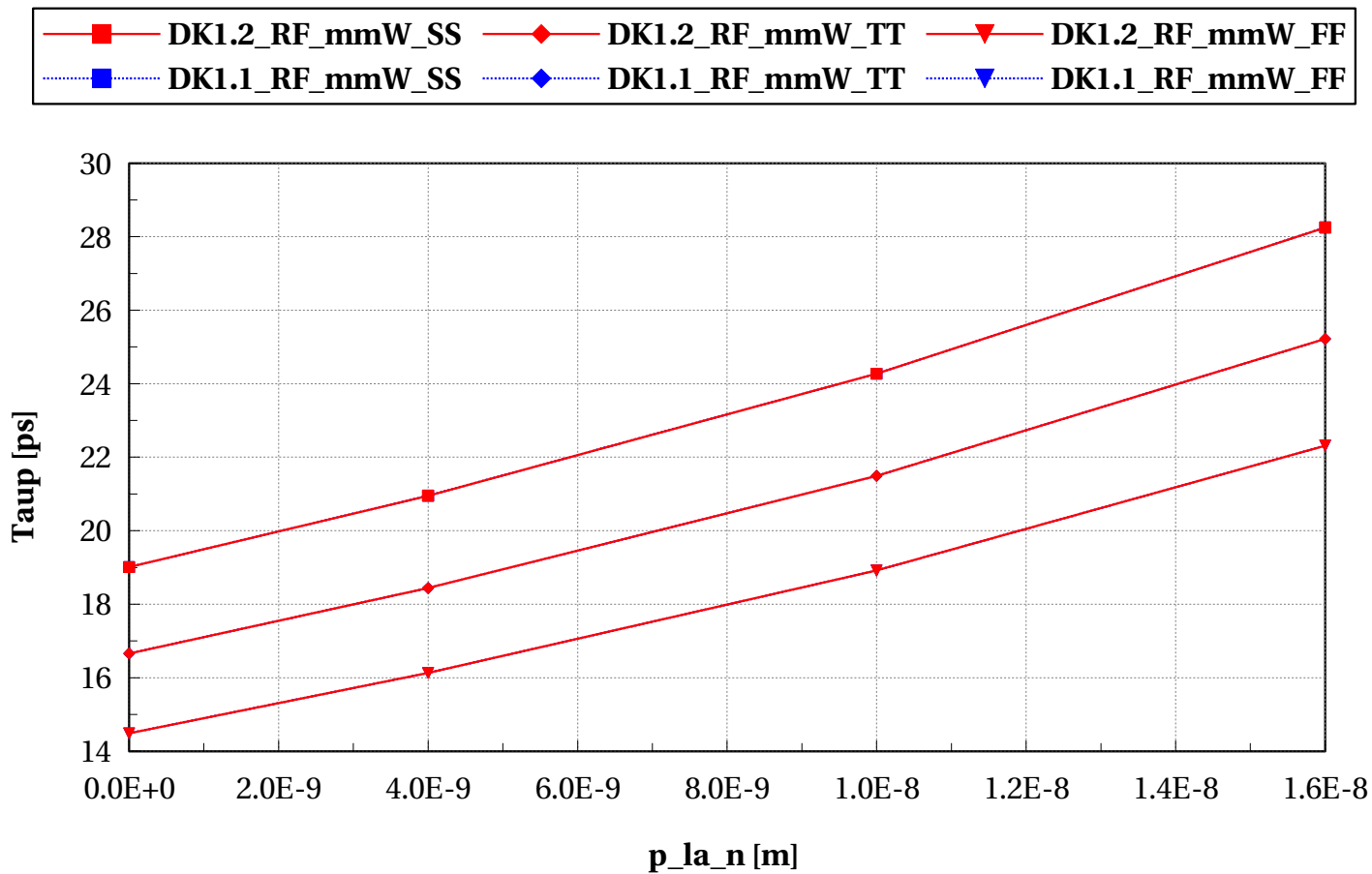
# nfet\_acc\_pfet\_acc, Fosc\_gate normalized vs TT [%] vs p\_la\_n [m]

Vdd==0.9 and temp==125



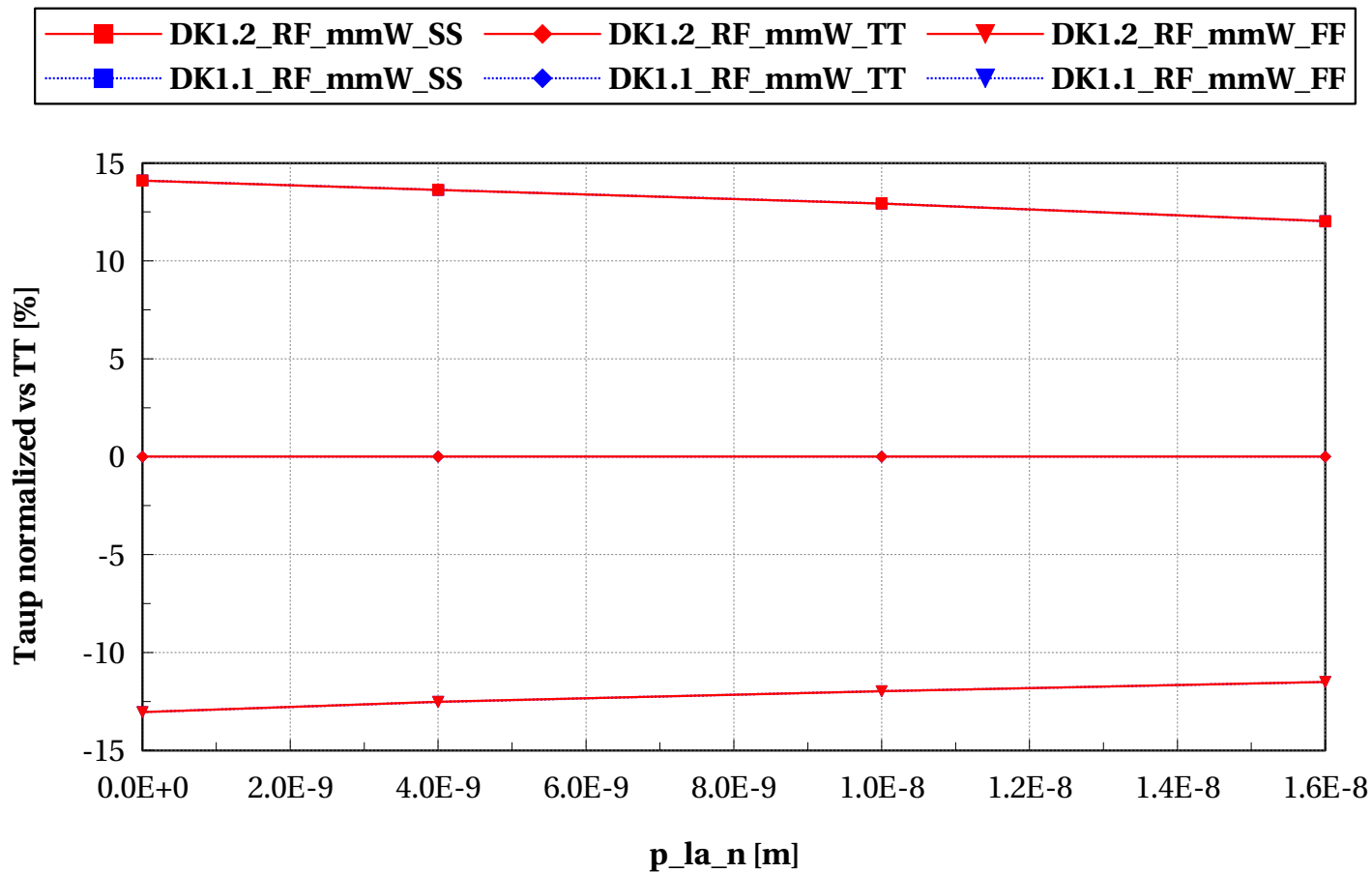
# nfet\_acc\_pfet\_acc, Taup [ps] vs p\_la\_n [m]

Vdd==0.9 and temp==125



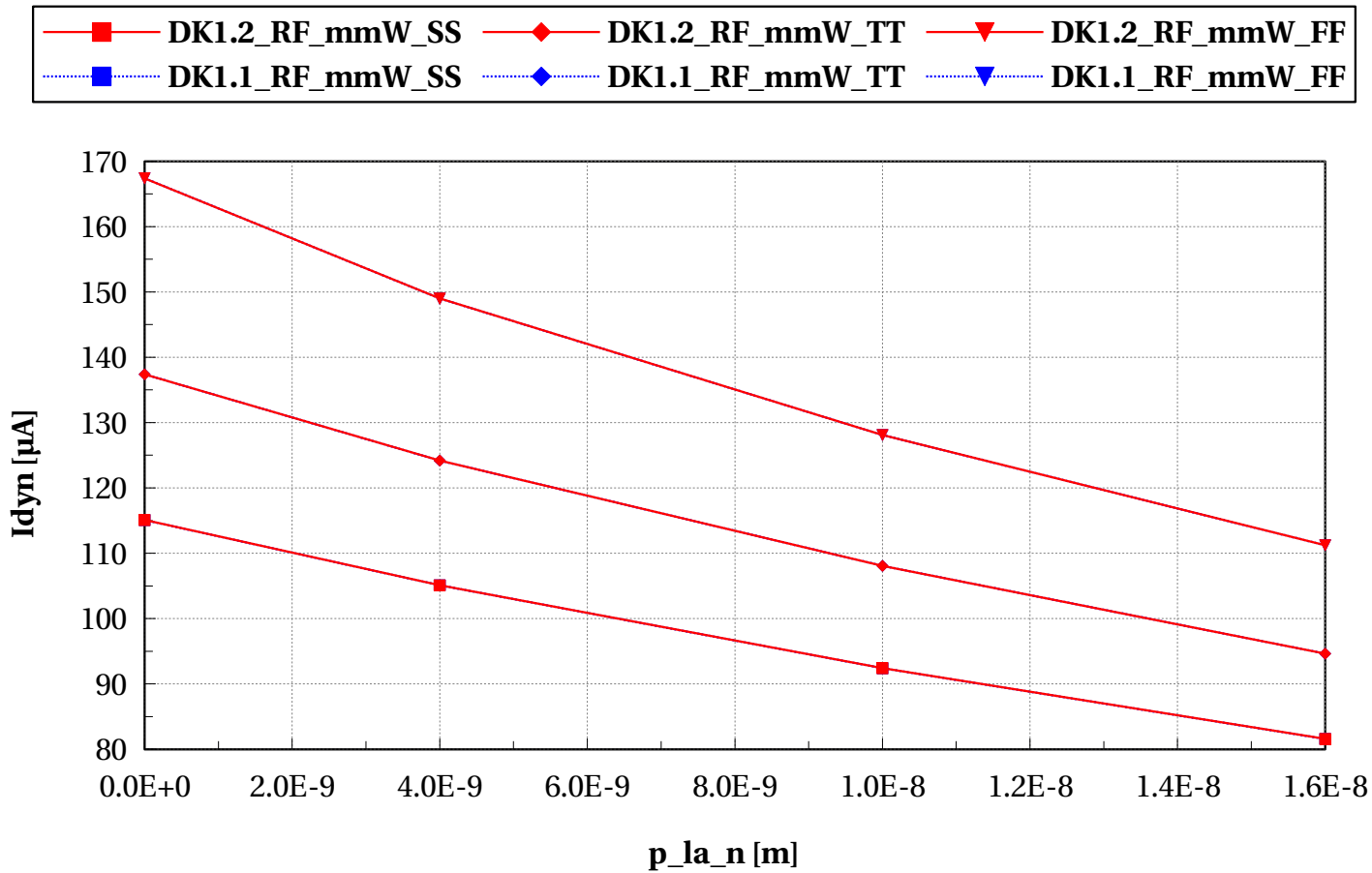
# nfet\_acc\_pfet\_acc, Taup normalized vs TT [%] vs p\_la\_n [m]

Vdd==0.9 and temp==125



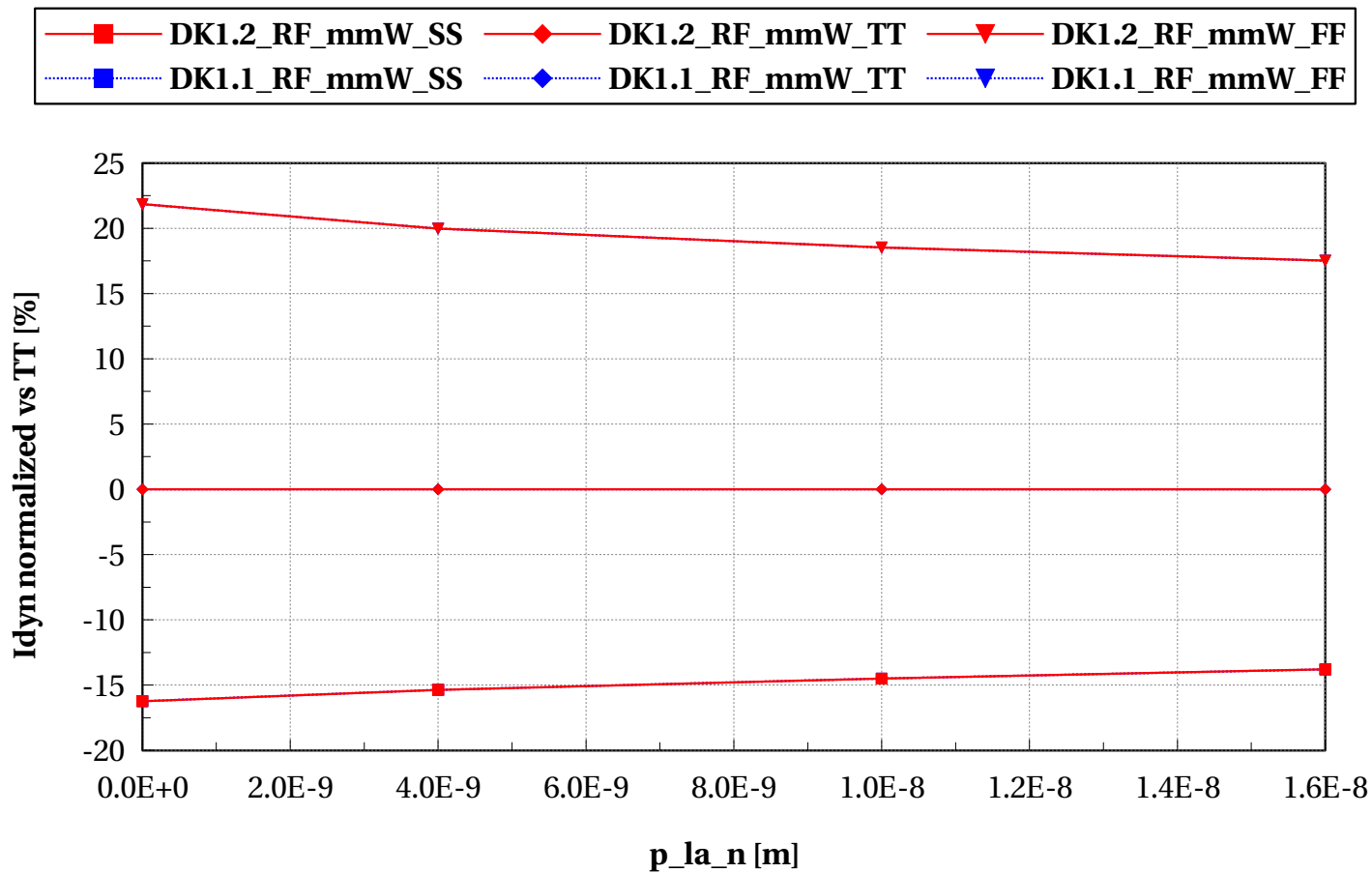
# nfet\_acc\_pfet\_acc, Idyn [ $\mu$ A] vs p\_la\_n [m]

Vdd==0.9 and temp==125



# nfet\_acc\_pfet\_acc, Idyn normalized vs TT [%] vs p\_la\_n [m]

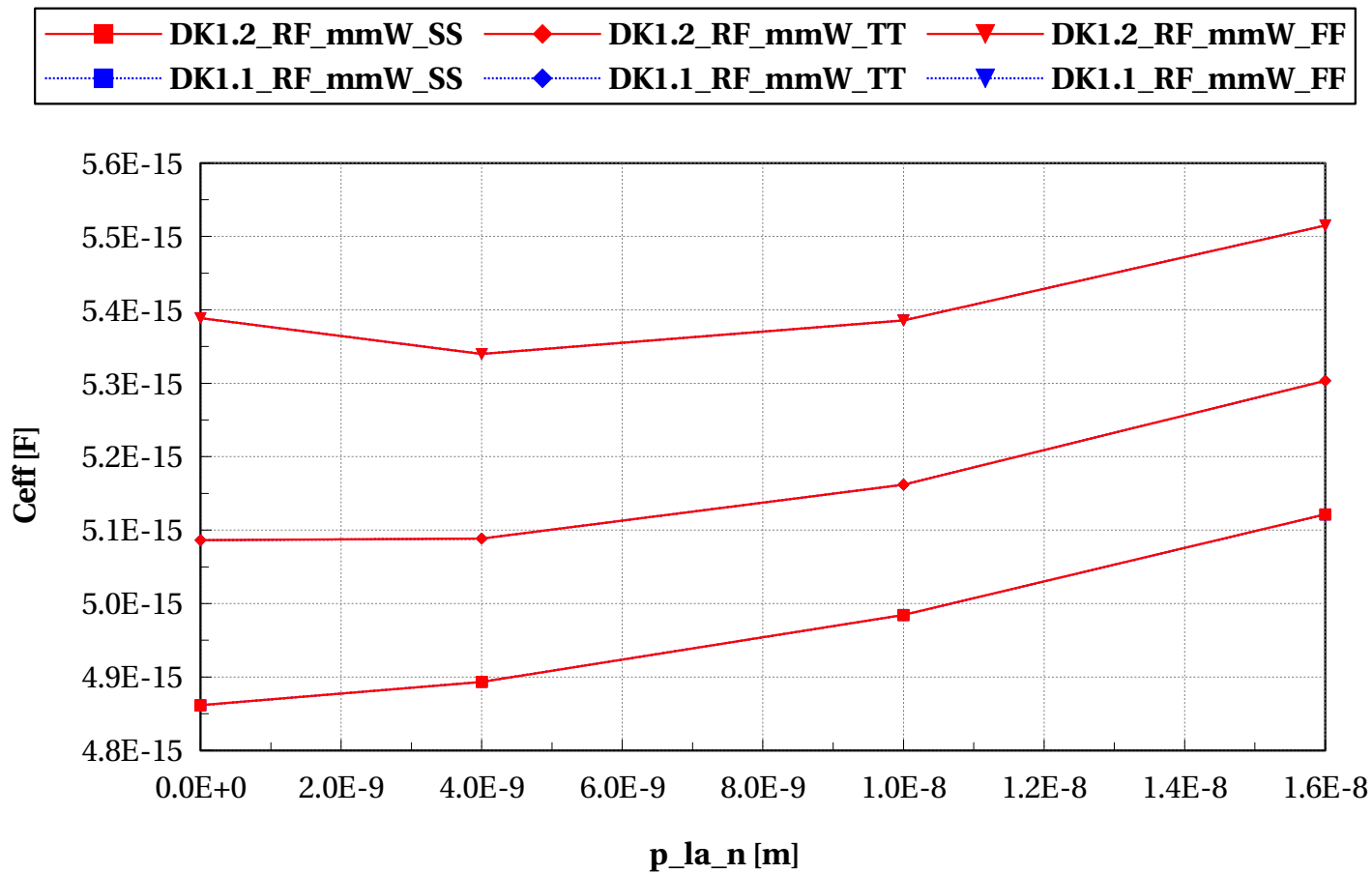
Vdd==0.9 and temp==125





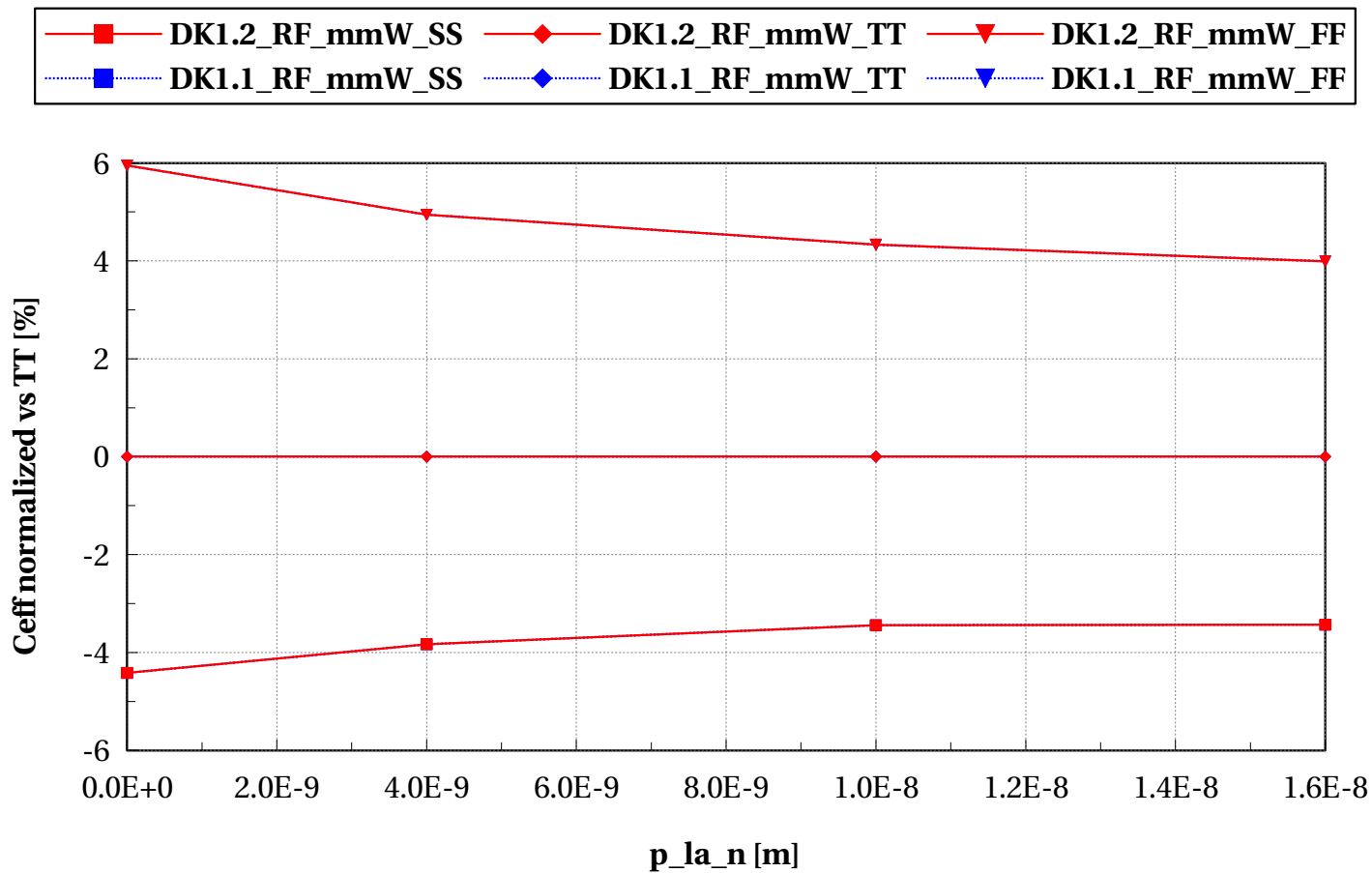
# nfet\_acc\_pfet\_acc, Ceff [F] vs p\_la\_n [m]

Vdd==0.9 and temp==125



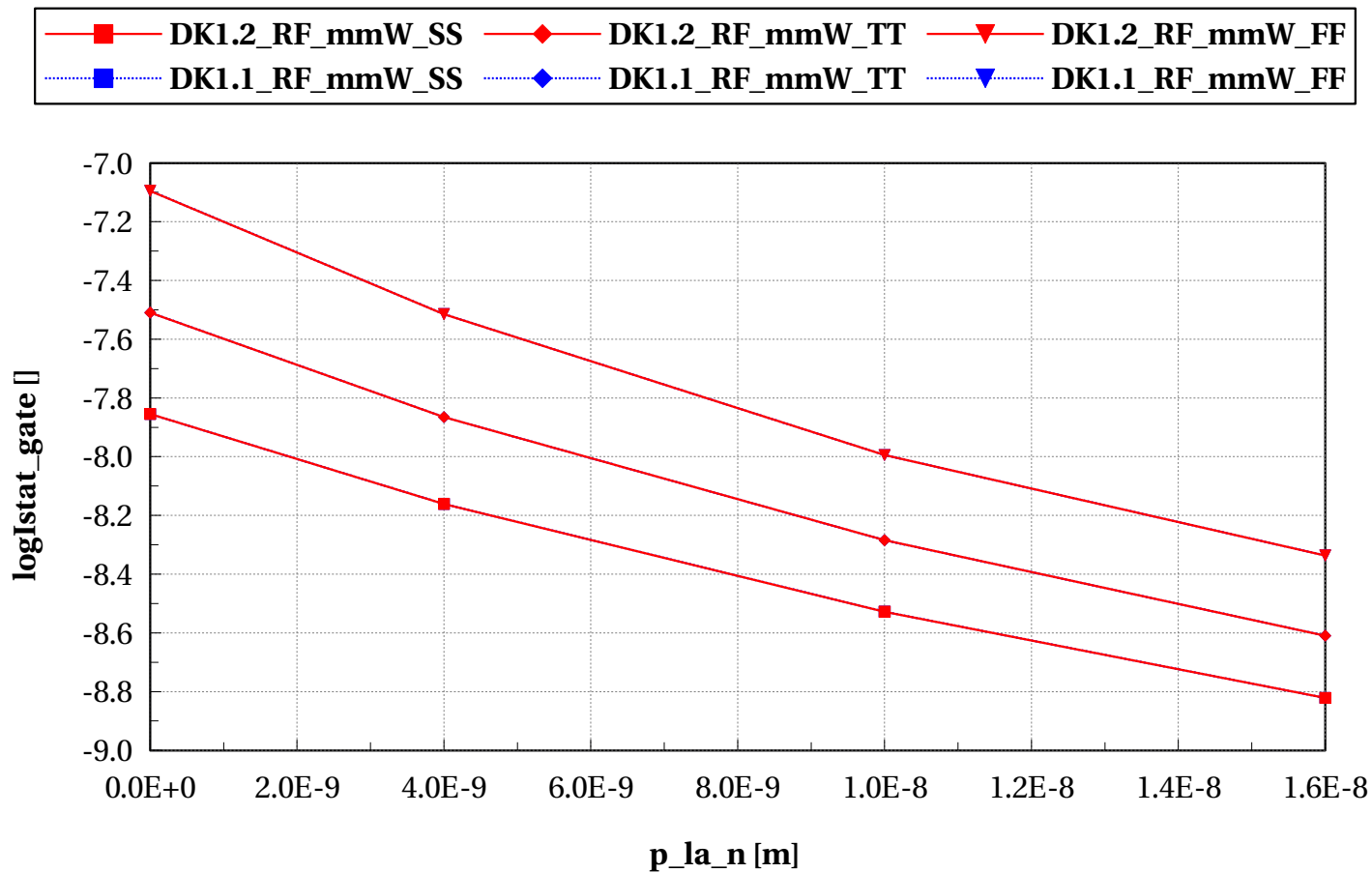
# nfet\_acc\_pfet\_acc, Ceff normalized vs TT [%] vs p\_la\_n [m]

Vdd==0.9 and temp==125



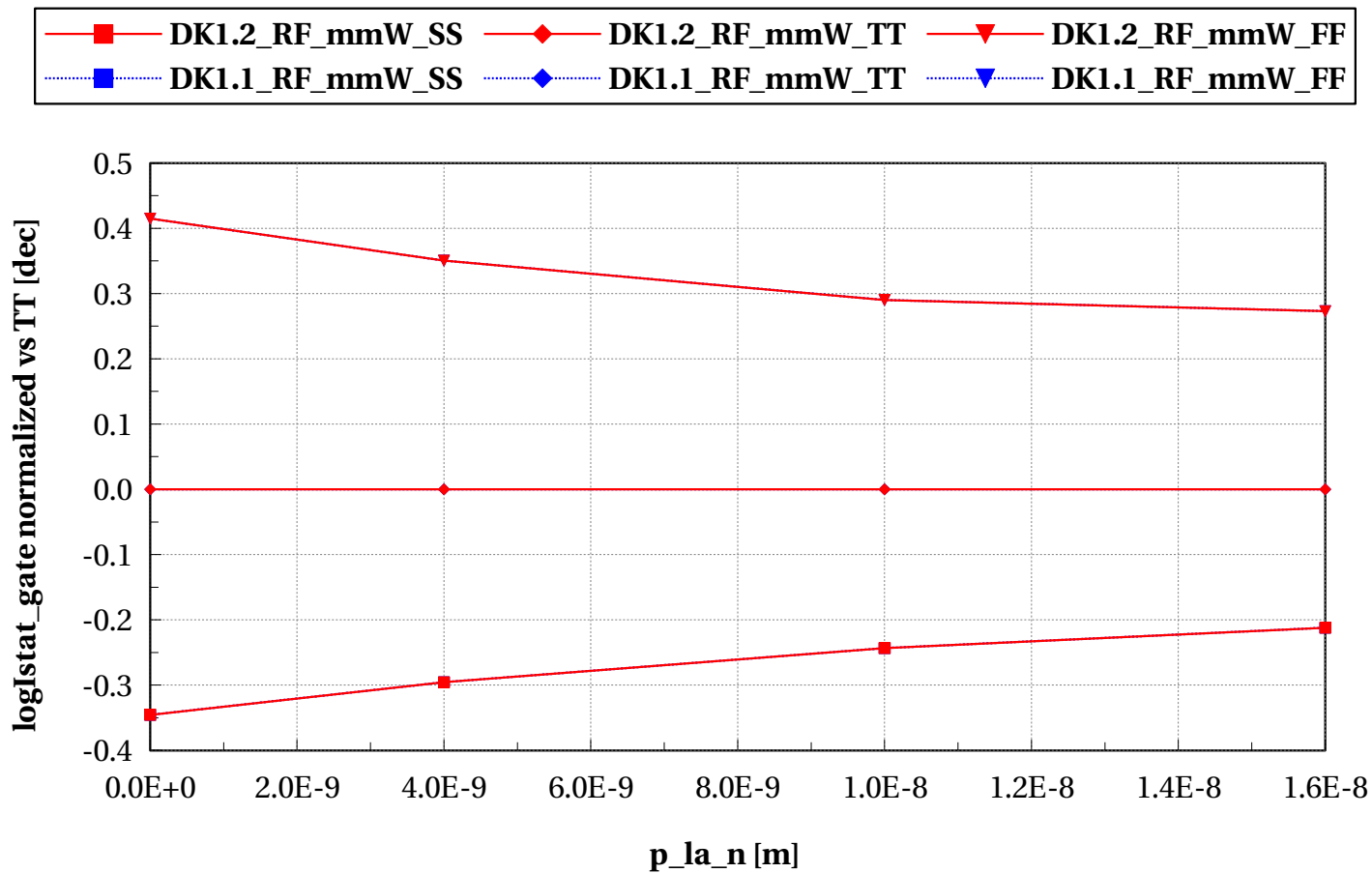
# nfet\_acc\_pfet\_acc, logIstat\_gate [] vs p\_la\_n [m]

Vdd==0.9 and temp==125



# nfet\_acc\_pfet\_acc, logIstat\_gate normalized vs TT [dec] vs p\_la\_n [m]

Vdd==0.9 and temp==125



# Annex

## Conditions of simulations

The simulations were done with SBenchLSF Alpha using Eldo simulator 2018.3.

- Model nfet\_acc\_pfet\_acc (DK1.2\_RF\_mmW)

- ✓ Input Parameters

- ✗ mc\_runs = 1000
- ✗ temp = 25 °C
- ✗ rload = 0
- ✗ vwellnfet = 0 V
- ✗ mc\_sens = 2
- ✗ cmiller = 0 F
- ✗ cload = 0 F
- ✗ sbenchlsf\_release = Alpha
- ✗ ams\_release = 2018.3
- ✗ fanout = 3
- ✗ vdd = 1 V
- ✗ nstage = 5
- ✗ vwellpfet = Vdd V
- ✗ mc\_nsigma = 3

- ✓ Sweep Parameters
  - ✗ vdd = 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3
  - ✗ temp = -40.0, 25.0, 125.0
- ✓ Extra parameters
  - ✗ lvt\_dev = 0
  - ✗ gflag\_\_noisedev\_\_rvt\_\_cmos028fdsoi = 0
  - ✗ gflag\_\_noisedev\_\_lvt\_\_cmos028fdsoi = 0
  - ✗ rvt\_dev = 0
- Model nfet\_acc\_pfet\_acc (DK1.1\_RF\_mmW)
  - ✓ Input Parameters
    - ✗ mc\_runs = 1000
    - ✗ temp = 25 °C
    - ✗ rload = 0
    - ✗ vwellnfet = 0 V
    - ✗ mc\_sens = 2
    - ✗ cmiller = 0 F
    - ✗ cload = 0 F
    - ✗ sbenchlsf\_release = Alpha
    - ✗ ams\_release = 2018.3
    - ✗ fanout = 3
    - ✗ vdd = 1 V
    - ✗ nstage = 5
    - ✗ vwellpfet = Vdd V
    - ✗ mc\_nsigma = 3
  - ✓ Sweep Parameters

- ✗ vdd = 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3
- ✗ temp = -40.0, 25.0, 125.0
- ✓ Extra parameters
  - ✗ lvt\_dev = 0
  - ✗ gflag\_\_noisedev\_\_rvt\_\_cmos028fdsoi = 0
  - ✗ gflag\_\_noisedev\_\_lvt\_\_cmos028fdsoi = 0
  - ✗ rvt\_dev = 0