Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB

3.3

User Manual

October 2018

PDK & Foundation Design Flows

Technology R&D – T&DP – Design Platform

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Revision History

Date	Product Version	Comments
01/07/2016	2.8.b	First version (aligned with DK version)
09/09/2016	2.8.c	Bug fix vc.bbview
07/10/2016	2.9	Alignment with DK 2.9 (HLVT inclusion)
13/01/2017	3.0	- technology.lef: updated routing directions for alignment with PG grid requirements & reintroduction of former vias definition - Introduction of technology_COT.lef file with systematic orthogonal metal layers - Alignment of PVS files with last DK 2.9 - Updated “overlap” strategy in dummy_layers.lef file for SignOff Extraction task => both “overlap” & “OVERLAP” layers are now defined
07/02/2017	3.0.a	Update of QRC techfiles with latest EM effects
28/03/2017	3.0.b	Added missing CORE12TEG site in sites.lef (bug fix for test chip team)
31/03/2017	3.0.c	QRC_TECHFILE bbview key alignment with latest spec Removal of former .csh env variables Addition of .cdslib file (and its bbview key) Addition of OA sites library (and its bbview key) Removal of PVS decks as agreed with TPPM (already in DK) Update of tech LEF regarding 553q1/q2 rules
06/04/2017	3.0.d	Optimization of XA double vias definition in technology_COT.lef
02/06/2017	3.1	CAP_TABLE & QRC_TECHFILE regenerated for alignment with updated PEX 28NM_STARRCXT_FDSOI_PROTOTYPE 2.3-PRELIM-00 (using ext 16.10/innovus 16.14) Renaming of technology_COT.lef in technology_alternative.lef
20/10/2017	3.2	Introduction of Via Large Array Spacing rules in tech LEF Duplication of “overlap/OVERLAP” in tech LEF (i.e. Zuma request) Aligned LPA strategy (new lpa.layer.map) with P28 FTK CDN strategy Removal of obsolete CAP_TABLE files
09/11/2017	3.2.a	[TRC #460908]: Addition of missing LEFOBS lines in Innovus map_out (required for LPA litho HS fixing) [TRC #460914]: Addition of M6 in layer list of LPA conf file [TRC #460904]: Removal of LPA MAP/ directory, transfer of LPA map file in TECH/ directory and removal of LPA map file bbview key
13/07/2018	3.3 PRELIM	Introduction of bin.tcl file for LIMA team

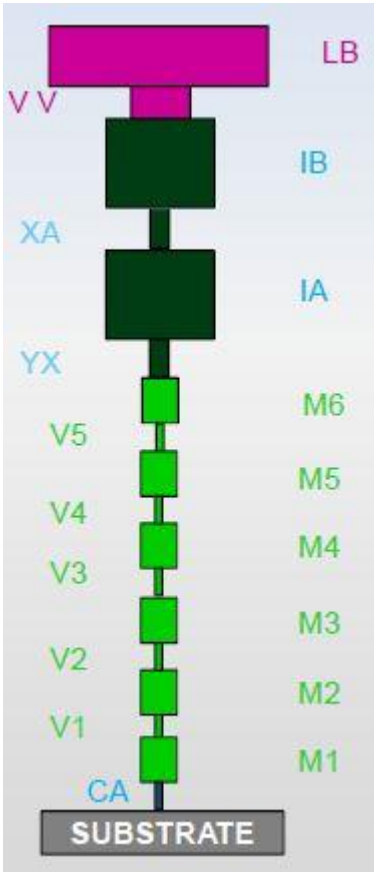
10/08/2018	3.3 INTERM	[TRC #498345]: "LEFOBS" missing in Innovus mapOut for layer above M3 [TRC #460908]: C28SOI: Missing lines in Innovus mapOut [TRC #460904]: LPA mapFile : incorrect management [TRC #460914]: C28SOI: Wrong line ine "LPA conf file" [TRC #496960 & #496961]: Antenna rules not coded for VV & LB layers EDI map_out: alignment with metal/via fillOPC purposes mappings for track-based fill
07/10/2018	3.3	Coding of new high-voltage FBB rules in tech LEF Inclusion of new VH/VL custom layers in Innovus map_out TRC #504081 Need new layers in the EDI/map_out file for SIP Wirebond flow

Table of Contents

1. Introduction

Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB is a TR&D Unicad product.

This product is aimed at providing technology enablement for CMOS028_FDSOI technology node, for the following metallization choice: 6U1x_2T8x_LB (8 metal levels out of which 6 are thin and 2 are thick).



This Foundation TechnoKit contains **techfiles and map files for P&R** (DRC clean routing) and extraction in Cadence tools, as well as decks for in-design lithography/verification. It currently only supports LEF format (no OPEN_ACCESS due to some specific syntaxes not yet available in open access). It also contains **techfiles and map files for SignOff**. No flow/automation is included in this product.

2. Module Architecture

Details below will be describing the content of each file included in this Foundation TechnoKit product:

2.1 PnR files:

a. ./LEF/technology.lef

This is the main technology file, which contains the layers definitions, routing rules and antenna rules.

Metal routing directions are aligned with ST PG grid requirements.

Dedicated PnR vias are also listed with their parameters (width / spacing / metal enclosure).

b. ./LEF/technology_alternative.lef

Alternative tech LEF where all metal layers are orthogonal one to the other. You may use the technology.lef or the technology_alternative.lef file, depending on your PG grid requirements. In ODIF flow, the technology.lef file is used by default.

c. ./LEF/viarule_generate.lef

This file contains statements defining formulas for generating via arrays.

d. ./LEF/sites.lef

This file contains the list of sites (based on standard cells heights).

e. ./LEF/dummy_layers.lef

This is the minimum subset of the technology.lef to allow mechanical loading inside Encounter, and which is compatible with LEF file used for SignOff extraction. It does not need to be loaded in P&R innovus tool.

f. ./LEF/lib_property.lef

This file indicates the intercell spacing constraints. With this kind of rules, standard cells can be placed next to each other only when they do not violate the spacing rules.

g. ./OpenAccess/cmos028_sites/

This is the open-access library containing the same information than in the sites.lef file.

h. ./EDI/map_out

This is the mapping file that must be used for GDS streamOut.

i. ./LPA/*

These files are used for in-design lithography checks and fixes, in the context of the direct launching from an innovus session of the mvs tool which looks for any litho hotspot and then may automatically perform search and repair to remove them.

The *.tcl are the configuration files, the Patterns/Lpa.xml is the deck file and the Patterns/Patterns/ directory contains the list of forbidden patterns.

2.2 Common PnR/SignOff files:

j. ./QRC_TECHFILE/*

These *.tech files are the parasitics used for extraction (binary tables storing RC coefficients). They were generated from the reference ICT files of the considered technology node.

They shall also be used for Voltus PI Analyses, Average and RMS current limits for Voltus Electromigration checks.

k. ./QUANTUS/cmos028FDSOI_6U1x_2T8x_LB.qrc.cmd.mapfile

Layer mappings file between “LEF/DEF and QRC tech files”, and between “LEF/DEF and GDS”.

Please be aware in the PNR implementation that this map file is only required in the case of the following mode considered: setExtractRCMode –effortLevel signoff, which calls another engine (I-QRC) to perform the extraction.

2.3 SignOff files:

l. ./VOLTUS/cmos028FDSOI_6U1x_2T8x_LB.eps.gds.mapfile

SignOff layer mappings file between “LEF/DEF and GDS”.

m. ./VOLTUS/cmos028FDSOI_6U1x_2T8x_LB.eps.lefdef.mapfile

SignOff layer mappings file between “LEF/DEF and QRC tech files.

2.4 Global files:

n. Others

The module also contains the standard infrastructure product files (.csh/.info/.ptbl/vc.bbview/documentation).

3. Tips

- ⇨ Please make sure to use the innovus version which was used for validation of these technology files: 16.14.000.
- ⇨ Please make sure to specify the following lef files in the “init_lef_file” variable, following this order:
  - technology.lef: must be set first to identify the all the proper items (layers, …) in the other lef files.
  - viarule_generate.lef
  - sites.lef

- Standard-cell libraries .lef

⇨ It is mandatory to set the following mode for the nanoRoute tool, in order to activate the automatic via generation:

- setNanoRouteMode –routeExpUseAutoVia true

⇨ It is recommended to set the following mode for viaGen, in order to take into account in the metal enclosure in the correct direction:

- setViaGenMode -optimize_cross_via 1

⇨ It is the command verifyLitho –techFile <LPA directory of the FoundationTechnoKit> which should be used (based on the LPA engine) to perform in-design lithography checks.

4. Contact Information

Please contact **HELPDESK** for any problems or suggestions.