C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG

Release Notes and Known Problems and Solutions

1. Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library Name	C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG
Library Version	7.1
Library Type	IO Cells
Technology	CMOS028_FDSOI
DK Version	DK_cmos28FDSOI_RF_6U1x_2T8x_LB 2.8.c-08

1.2 Impact of Product Release

For latest information, please refer to LYS *(http://col2.cro.st.com/libyield).*

1.3 Related Documentation

- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_7.1 User Manual**
- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_7.1 Release Notes and Known Problems and Solutions**
- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_ff28_1.10V_1.32V_m40C_tt28_1.00V_1.20V_25C_ss28_0.90V_-1.08V_125C_7.1 DataBook**
- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_ff28_1.05V_1.32V_125C_7y50kR_ss28_1.10V_1.08V_m40C_-7y50kR_7.1 DataBook**
- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_ff28_0.90V_1.65V_125C_2ey_ss28_0.90V_1.35V_m40C_2ey_-7.1 DataBook**

- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_ff28_0.90V_1.65V_m40C_2ey_ss28_0.90V_1.35V_125C_2ey_-7.1 DataBook**
- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_ff28_1.10V_1.95V_125C_ss28_0.90V_1.65V_m40C_7.1 Data-Book**
- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_ff28_0.90V_1.95V_125C_2ey_ss28_0.90V_1.65V_m40C_2ey_-7.1 DataBook**
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- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_ff28_1.10V_1.65V_125C_ss28_0.90V_1.35V_m40C_7.1 Data-Book**
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- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_ff28_1.05V_1.65V_125C_7y50kR_ss28_1.10V_1.35V_m40C_-7y50kR_7.1 DataBook**
- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_7.1 HDL EMUL Primitive Description**
- **C28SOI_IO_EXT_CSF_TESTMUX1V8_LR_EG_7.1 HDL MODELS model usage guidelines**

2. Changes with respect to all Previous Versions

2.1 Version 7.1

A. This is the Final release

B. Major content of packages are

(1) HDL Models:

(a) Verilog (.v) is compliance with power aware flow

(b) Emulator (_emul.v), Tetramax(_tmax.v), Power Verilog (_allpins.v)

(2) STF View is compliance with UPF flow and contains 137 corners. Characterized with spice models of DK_cmos28FDSOI_AMS_6U1x_2U2x_2T8x_LB 2.7.a-33

(3) CCS Noise

(4) Voltus view supported

BE has SPICE UPDATES

driver and predriver updated as per the new spice

3. Known Problems and Solutions of this release

This document is compatible for viewing with acroread 7.0 and later versions. If opened with a lower version of acroread, there might be some color display problem.

Ignorable DRC Errors

ERROR : Rule EMET.DEN.1
ERROR : Rule EMET.DEN.10
ERROR : Rule EMET.DEN.11
ERROR : Rule EMET.DEN.12
ERROR : Rule EMET.DEN.2
ERROR : Rule EMET.DEN.3
ERROR : Rule EMET.DEN.4
ERROR : Rule EMET.DEN.5
ERROR : Rule EMET.DEN.6
ERROR : Rule EMET.DEN.7
ERROR : Rule EMET.DEN.8
ERROR : Rule EMET.DEN.9
ERROR : Rule IA.DEN.1
ERROR : Rule IA.DEN.4
ERROR : Rule IA.DEN.4.1
ERROR : Rule IA.DEN.8
ERROR : Rule IB.DEN.1
ERROR : Rule IB.DEN.4
ERROR : Rule IB.DEN.4.1
ERROR : Rule IB.DEN.8
ERROR : Rule M1.DEN.1
ERROR : Rule M1.DEN.8
ERROR : Rule M2.DEN.1
ERROR : Rule M2.DEN.4.1
ERROR : Rule M2.DEN.8
ERROR : Rule M3.DEN.1
ERROR : Rule M3.DEN.4
ERROR : Rule M3.DEN.4.1
ERROR : Rule M3.DEN.8
ERROR : Rule M4.DEN.1
ERROR : Rule M4.DEN.4
ERROR : Rule M4.DEN.4.1

ERROR : Rule M4.DEN.8
ERROR : Rule M5.DEN.1
ERROR : Rule M5.DEN.4
ERROR : Rule M5.DEN.4.1
ERROR : Rule M5.DEN.8
ERROR : Rule M6.DEN.1
ERROR : Rule M6.DEN.4
ERROR : Rule M6.DEN.4.1
ERROR : Rule M6.DEN.8
ERROR : Rule PC.DEN.1
ERROR : Rule PC.DEN.8
ERROR : Rule RX.DEN.1
ERROR : Rule RX.DEN.8

The max transition values signify the maximum allowable input slope that can be applied to pin. Hence the output transition at a pin can be greater than max transition

In Design_simulation_result.pdf simulation values are Present for cell BD4STARODP_FS_EXT_3V3SF_3V3_CL_LIN & BT8ARODP_FS_EXT_3V3SF_3V3_CL_LIN

For rest of cells values can be mapped as following

BD2SCARUDQPCH_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD2SCARUDQPCH_EXT_CSF_1V8_FC_OUTER

BD2SCARUDQPCL_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD2SCARUDQPCH_EXT_CSF_1V8_FC_OUTER

BD2SCARUDQPCZ_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD2SCARUDQPCH_EXT_CSF_1V8_FC_OUTER

BD4SCARUDQPCH_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD4SCARUDQPCH_EXT_CSF_1V8_FC_OUTER

BD4SCARUDQPCL_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD4SCARUDQPCH_EXT_CSF_1V8_FC_OUTER

BD4SCARUDQPCZ_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD4SCARUDQPCH_EXT_CSF_1V8_FC_OUTER

BD4SCARUDQPCZ_IL_EXT_CSF_1V8_FC_(INNER/LIN/OUTER) –> BD4SCARUDQPCH_EXT_CSF_1V8_FC_OUTER

	BD6SCARUDQPCH_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD6SCARUDQPCH_EXT_CSF_1V8_FC_OUTER BD6SCARUDQPCL_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD6SCARUDQPCH_EXT_CSF_1V8_FC_OUTER BD6SCARUDQPCZ_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD6SCARUDQPCH_EXT_CSF_1V8_FC_OUTER BD8SCARUDQPCH_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD8SCARUDQPCH_EXT_CSF_1V8_FC_OUTER BD8SCARUDQPCL_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD8SCARUDQPCH_EXT_CSF_1V8_FC_OUTER BD8SCARUDQPCZ_EXT_CSF_1V8_(FC_INNER/FC_LIN/CL_LIN) –> BD8SCARUDQPCH_EXT_CSF_1V8_FC_OUTER

4. Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact HELPDESK (http://col2.cro.st.com/helpdesk).

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