C28SOI_SC_8_CLK_LL

User Manual

8 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

Overview

Features

- The C28SOI_SC_8_CLK_LL Standard Cell library contains 388 cells.

Application

- Design needs in CMOS28FDSOI platform IPs.

Library Architecture

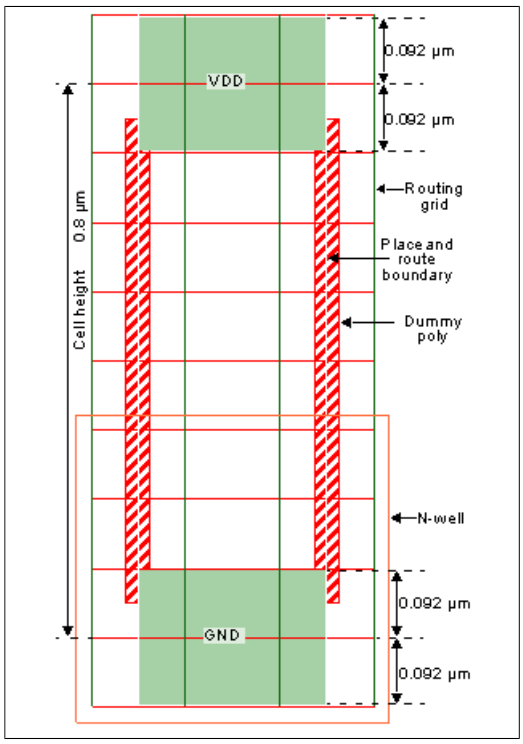
This section illustrates the architecture used for C28SOI_SC_8_CLK_LL Standard Cell library.

Following table shows the Physical Specifications for this library.

Table 1: Physical Specifications

Parameter	Value	Unit
Drawn Gate Length	0.030	µm
Layout Grid	0.001	µm
Vertical Pin Grid	0.1	µm
Horizontal Pin Grid	0.136	µm
Cell Power and Ground Rail Width	0.184	µm

Figure 1: Cell Architecture



1. Quick References

	Refer to the Naming Convention Document available in Design Package for more details regarding cell names.

	Refer to the Standard Cells Reference Manual available in Design Package for more details on library specific information.

2. Functional Specifications

2.1. Cell List

2.1.1. LL(LP Low Vt)

2.1.1.1. Poly Bias With 0 nm

Table 2: Cell List

Cell Name	Drive Strength	Description
C8T28SOIDV_LL1_SDFSYNCPQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL1_SDFSYNCPRQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL1_SDFSYNCPSQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNBF	X18, X28, X37, X55, X74	Buffer with Balanced rise and fall delays for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNGFMUX21	X30	2:1 Glitch-free MUX for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNIV	X18, X28, X37, X55, X74	Inverter with Balanced rise and fall delays for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNLDLRQ	X19	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNMUX41	X9, X27	4:1 non-inverting Multiplexer for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNOR3	X27	3 input OR for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNOR4	X27	4 input OR for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNSDFPRQT	X9	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNSDFPSQT	X9	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network, Vdd rail at the bottom of the cell

Cell Name	Drive Strength	Description
C8T28SOIDV_LL_SDFSYNCPQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFSYNCPRQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFSYNCPSQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOI_LLP1_CNHLS	X10, X14, X19, X24, X29, X34, X38, X57	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C8T28SOI_LLP_CNHLS	X4, X9, X13, X17, X21, X27, X30, X38, X54	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C8T28SOI_LL_CNAND2	X14, X19, X27	2 input AND for Clock network
C8T28SOI_LL_CNAND3	X10, X14, X19, X27	3 input AND for Clock network
C8T28SOI_LL_CNAO12	X19	2 input AND into 2 input OR
C8T28SOI_LL_CNBF	X4, X8, X12, X18, X23, X28, X32, X37, X54	Buffer with Balanced rise and fall delays for Clock network
C8T28SOI_LL_CNIV	X4, X9, X14, X18, X22, X27, X32, X37, X74	Inverter with Balanced rise and fall delays for Clock network
C8T28SOI_LL_CNMUX21	X9, X15, X27	2:1 non-inverting Multiplexer for Clock network
C8T28SOI_LL_CNNAND2	X8, X15, X27	2 input NAND for Clock network
C8T28SOI_LL_CNNAND2A	X9, X15, X27	2 input NAND with A input inverted for Clock network
C8T28SOI_LL_CNNOR2	X8, X15, X27	2 input NOR for Clock network
C8T28SOI_LL_CNNOR2A	X9, X15, X27	2 input NOR with A input Inverted for Clock network
C8T28SOI_LL_CNOR2	X19, X37	2 input OR for Clock network
C8T28SOI_LL_CNOR3	X14, X19	3 input OR for Clock network
C8T28SOI_LL_CNOR4	X19	4 input OR for Clock network
C8T28SOI_LL_CNXOR2	X9, X15, X27	2 input Exclusive OR for Clock network
C8T28SOI_LL_DLYHFM4	X4, X12	Delay Cell for Hold Time Fixing
C8T28SOI_LL_DLYHFM8	X4, X12, X30	Delay Cell for Hold Time Fixing

2.1.1.2. Poly Bias With 4 nm

Table 3: Cell List

Cell Name	Drive Strength	Description
C8T28SOIDV_LL1_SDFSYNCPQ	X5	Error - Wrong Optimization, Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL1_SDFSYNCPRQ	X5	Error - Wrong Optimization, Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL1_SDFSYNCPSQ	X5	Error - Wrong Optimization, Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNBF	X18, X28, X37, X55, X74	Buffer with Balanced rise and fall delays for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNGFMUX21	X30	2:1 Glitch-free MUX for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNIV	X18, X28, X37, X55, X74	Inverter with Balanced rise and fall delays for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNLDLRQ	X19	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNMUX41	X9, X27	4:1 non-inverting Multiplexer for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNOR3	X27	3 input OR for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNOR4	X27	4 input OR for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNSDFPRQT	X9	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNSDFPSQT	X9	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFSYNCPQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFSYNCPRQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell

Cell Name	Drive Strength	Description
C8T28SOIDV_LL_SDFSYNCPSQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOI_LLP1_CNHLS	X10, X14, X19, X24, X29, X34, X38, X57	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C8T28SOI_LLP_CNHLS	X4, X9, X13, X17, X21, X27, X30, X38, X54	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C8T28SOI_LL_CNAND2	X14, X19, X27	2 input AND for Clock network
C8T28SOI_LL_CNAND3	X10, X14, X19, X27	3 input AND for Clock network
C8T28SOI_LL_CNAO12	X19	2 input AND into 2 input OR
C8T28SOI_LL_CNBF	X4, X8, X12, X18, X23, X28, X32, X37, X54	Buffer with Balanced rise and fall delays for Clock network
C8T28SOI_LL_CNIV	X4, X9, X14, X18, X22, X27, X32, X37, X74	Inverter with Balanced rise and fall delays for Clock network
C8T28SOI_LL_CNMUX21	X9, X15, X27	2:1 non-inverting Multiplexer for Clock network
C8T28SOI_LL_CNNAND2	X8, X15, X27	2 input NAND for Clock network
C8T28SOI_LL_CNNAND2A	X9, X15, X27	2 input NAND with A input inverted for Clock network
C8T28SOI_LL_CNNOR2	X8, X15, X27	2 input NOR for Clock network
C8T28SOI_LL_CNNOR2A	X9, X15, X27	2 input NOR with A input Inverted for Clock network
C8T28SOI_LL_CNOR2	X19, X37	2 input OR for Clock network
C8T28SOI_LL_CNOR3	X14, X19	3 input OR for Clock network
C8T28SOI_LL_CNOR4	X19	4 input OR for Clock network
C8T28SOI_LL_CNXOR2	X9, X15, X27	2 input Exclusive OR for Clock network
C8T28SOI_LL_DLYHFM4	X4, X12	Delay Cell for Hold Time Fixing
C8T28SOI_LL_DLYHFM8	X4, X12, X30	Delay Cell for Hold Time Fixing

2.1.1.3. Poly Bias With 10 nm

Table 4: Cell List

Cell Name	Drive Strength	Description
C8T28SOIDV_LL1_SDFSYNCPQ	X5	Error - Wrong Optimization, Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL1_SDFSYNCPRQ	X5	Error - Wrong Optimization, Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset;

Cell Name	Drive Strength	Description
		having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL1_SDFSYNCPSQ	X5	Error - Wrong Optimization, Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNBF	X18, X28, X37, X55, X74	Buffer with Balanced rise and fall delays for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNGFMUX21	X30	2:1 Glitch-free MUX for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNIV	X18, X28, X37, X55, X74	Inverter with Balanced rise and fall delays for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNLDLRQ	X19	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNMUX41	X9, X27	4:1 non-inverting Multiplexer for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNOR3	X27	3 input OR for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNOR4	X27	4 input OR for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNSDFPRQT	X9	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNSDFPSQT	X9	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFSYNCPQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFSYNCPRQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFSYNCPSQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOI_LLP1_CNHLS	X10, X14, X19, X24, X29, X34, X38, X57	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent

Cell Name	Drive Strength	Description
		and active low enable clock hold low; with scan functionality for Clock network
C8T28SOI_LLP_CNHLS	X4, X9, X13, X17, X21, X27, X30, X38, X54	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C8T28SOI_LL_CNAND2	X14, X19, X27	2 input AND for Clock network
C8T28SOI_LL_CNAND3	X10, X14, X19, X27	3 input AND for Clock network
C8T28SOI_LL_CNAO12	X19	2 input AND into 2 input OR
C8T28SOI_LL_CNBF	X4, X8, X12, X18, X23, X28, X32, X37, X54	Buffer with Balanced rise and fall delays for Clock network
C8T28SOI_LL_CNIV	X4, X9, X14, X18, X22, X27, X32, X37, X74	Inverter with Balanced rise and fall delays for Clock network
C8T28SOI_LL_CNMUX21	X9, X15, X27	2:1 non-inverting Multiplexer for Clock network
C8T28SOI_LL_CNNAND2	X8, X15, X27	2 input NAND for Clock network
C8T28SOI_LL_CNNAND2A	X9, X15, X27	2 input NAND with A input inverted for Clock network
C8T28SOI_LL_CNNOR2	X8, X15, X27	2 input NOR for Clock network
C8T28SOI_LL_CNNOR2A	X9, X15, X27	2 input NOR with A input Inverted for Clock network
C8T28SOI_LL_CNOR2	X19, X37	2 input OR for Clock network
C8T28SOI_LL_CNOR3	X14, X19	3 input OR for Clock network
C8T28SOI_LL_CNOR4	X19	4 input OR for Clock network
C8T28SOI_LL_CNXOR2	X9, X15, X27	2 input Exclusive OR for Clock network
C8T28SOI_LL_DLYHFM4	X4, X12	Delay Cell for Hold Time Fixing
C8T28SOI_LL_DLYHFM8	X4, X12, X30	Delay Cell for Hold Time Fixing

2.1.1.4. Poly Bias With 16 nm

Table 5: Cell List

Cell Name	Drive Strength	Description
C8T28SOIDV_LL1_SDFSYNCPQ	X5	Error - Wrong Optimization, Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL1_SDFSYNCPRQ	X5	Error - Wrong Optimization, Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL1_SDFSYNCPSQ	X5	Error - Wrong Optimization, Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only, Vdd rail at the bottom of the cell

Cell Name	Drive Strength	Description
C8T28SOIDV_LL_CNBF	X18, X28, X37, X55, X74	Buffer with Balanced rise and fall delays for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNGFMUX21	X30	2:1 Glitch-free MUX for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNIV	X18, X28, X37, X55, X74	Inverter with Balanced rise and fall delays for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNLDLRQ	X19	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNMUX41	X9, X27	4:1 non-inverting Multiplexer for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNOR3	X27	3 input OR for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNOR4	X27	4 input OR for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNSDFPRQT	X9	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_CNSDFPSQT	X9	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFSYNCPQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFSYNCPRQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFSYNCPSQ	X5	Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOI_LLP1_CNHLS	X10, X14, X19, X24, X29, X34, X38, X57	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C8T28SOI_LLP_CNHLS	X4, X9, X13, X17, X21, X27, X30, X38, X54	Design optimized to reduce dynamic power, Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network
C8T28SOI_LL_CNAND2	X14, X19, X27	2 input AND for Clock network

Cell Name	Drive Strength	Description
C8T28SOI_LL_CNAND3	X10, X14, X19, X27	3 input AND for Clock network
C8T28SOI_LL_CNAO12	X19	2 input AND into 2 input OR
C8T28SOI_LL_CNBF	X4, X8, X12, X18, X23, X28, X32, X37, X54	Buffer with Balanced rise and fall delays for Clock network
C8T28SOI_LL_CNIV	X4, X9, X14, X18, X22, X27, X32, X37, X74	Inverter with Balanced rise and fall delays for Clock network
C8T28SOI_LL_CNMUX21	X9, X15, X27	2:1 non-inverting Multiplexer for Clock network
C8T28SOI_LL_CNNAND2	X8, X15, X27	2 input NAND for Clock network
C8T28SOI_LL_CNNAND2A	X9, X15, X27	2 input NAND with A input inverted for Clock network
C8T28SOI_LL_CNNOR2	X8, X15, X27	2 input NOR for Clock network
C8T28SOI_LL_CNNOR2A	X9, X15, X27	2 input NOR with A input Inverted for Clock network
C8T28SOI_LL_CNOR2	X19, X37	2 input OR for Clock network
C8T28SOI_LL_CNOR3	X14, X19	3 input OR for Clock network
C8T28SOI_LL_CNOR4	X19	4 input OR for Clock network
C8T28SOI_LL_CNXOR2	X9, X15, X27	2 input Exclusive OR for Clock network
C8T28SOI_LL_DLYHFM4	X4, X12	Delay Cell for Hold Time Fixing
C8T28SOI_LL_DLYHFM8	X4, X12, X30	Delay Cell for Hold Time Fixing

2.2. Cell Usage

Cell names starting with CNHLS* are used for clock gating. Clock gating module is used to disable clock to parts of the design that are not in use over that period. The cells have been set as "don't use" and "don't touch" in the .lib file

- Clocktree synthesis must only use the cells from CLOCK library (except DLY cells).
- For hold correction, following cells must be used:
  - DLY (delay cells)
  - CNIV
  - CNBF
- DLY cells are specifically meant for hold fixing only and no other cells other than DLY, CNIV, and CNBF must appear in hold correction.
- For datapath, all CN* cells can be used.

2.3. Delay Cell Specifications

Delay cells present in this library has been designed with Specific Targeted Delay at Best Process, 1.15V with no FBB, -40C

Table 6: Cell Usage

Cell Type	Minimum Targeted Delay @ ff28_1.15V_0.00V_0.00V_0.00V_m40C
C8T28SOI_LL_DLYHFM4X*_P0	40 ps
C8T28SOI_LL_DLYHFM8X*_P0	80 ps

3. Contact Information

ST users, login to **HELPDESK** (http://col2.cro.st.com/helpdesk) for submitting queries or support requests.
Non-ST users, contact Customer Support personnel.

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