C28SOI_SC_12_COREPBP4_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 4 nm

Overview

- C28SOI_SC_12_COREPBP4_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

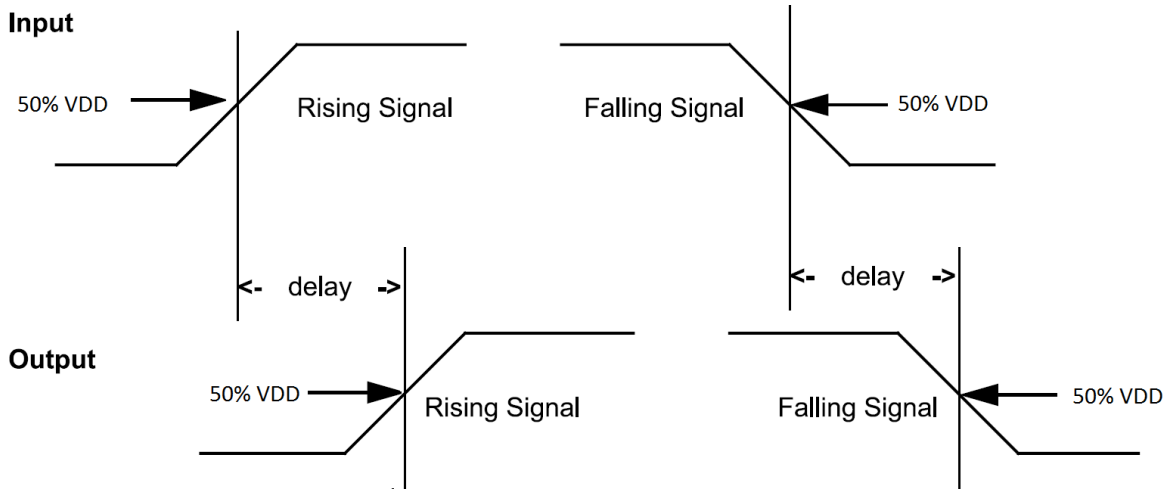


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

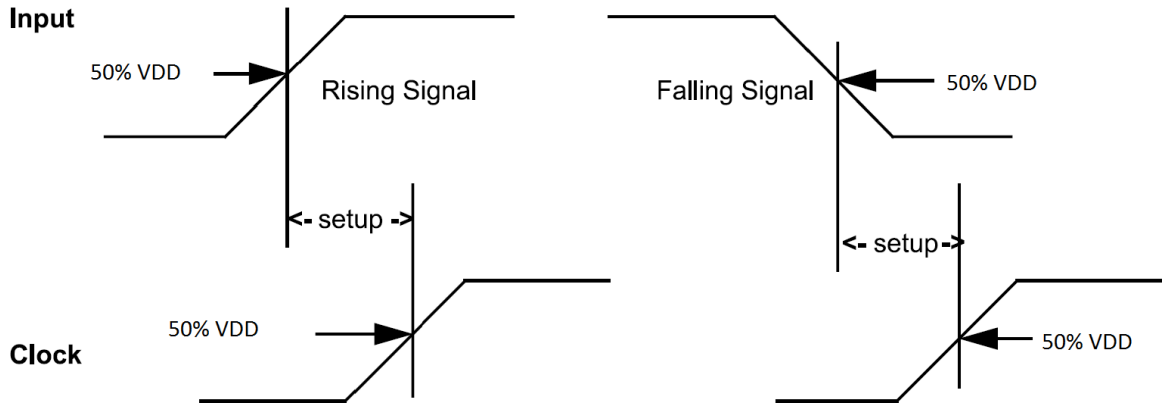


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

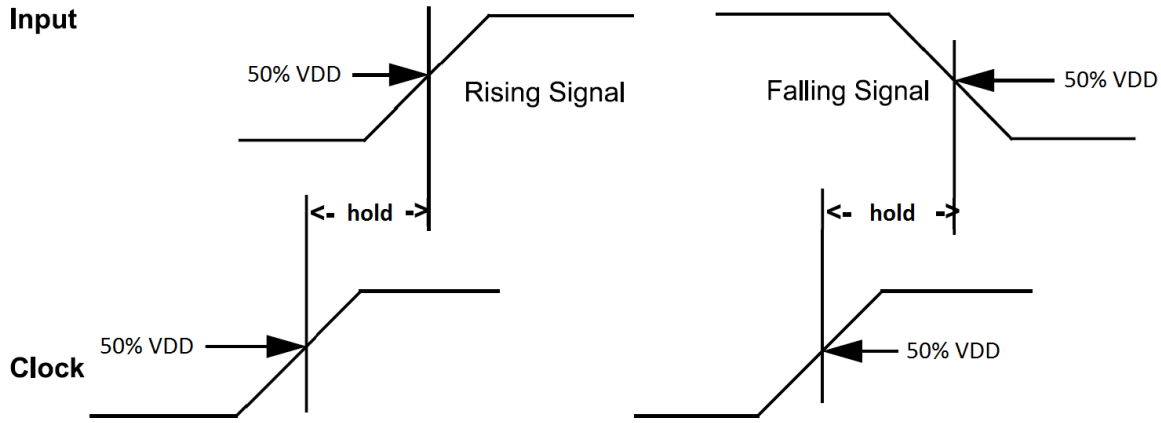


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

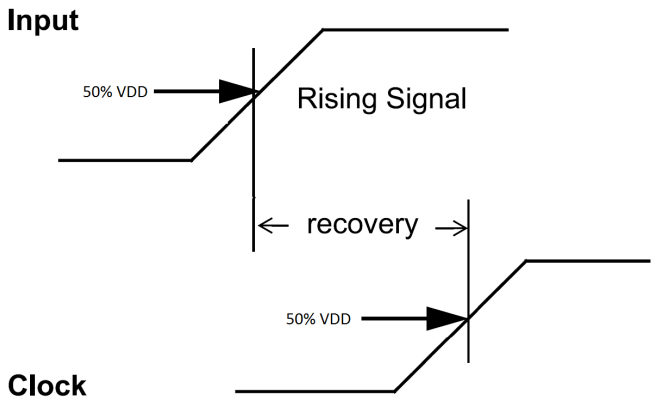


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

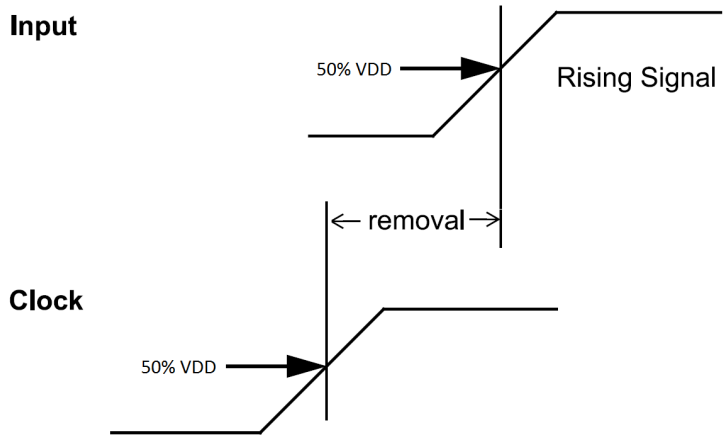


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

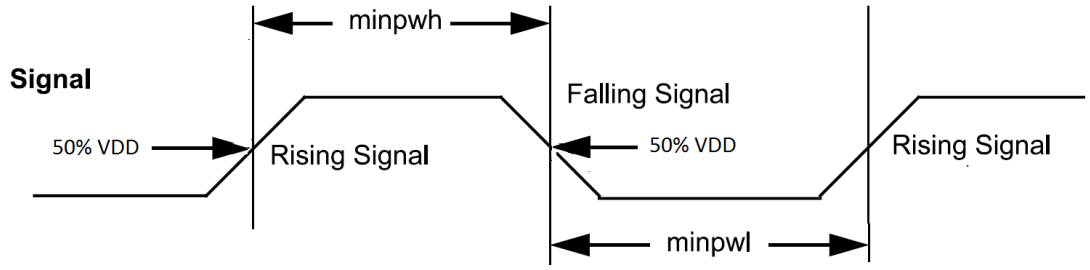


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

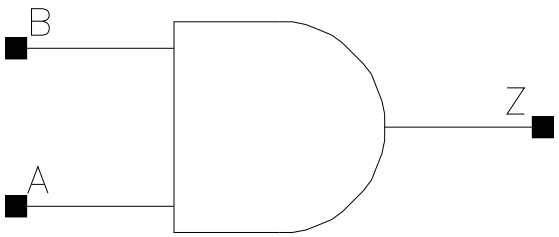
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X25_P4	1.200	1.088	1.3056
X33_P4	1.200	1.360	1.6320
X42_P4	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0007	0.0011	0.0015	0.0019
B	0.0006	0.0010	0.0015	0.0019
	X42_P4			
A	0.0019			
B	0.0019			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0312	0.0253	2.2174	1.1255
A to Z ↑	0.0254	0.0237	3.4451	1.6737
B to Z ↓	0.0297	0.0239	2.2182	1.1239
B to Z ↑	0.0269	0.0248	3.4422	1.6742
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0260	0.0251	0.7422	0.5533

A to Z ↑	0.0231	0.0237	1.1026	0.8326
B to Z ↓	0.0247	0.0229	0.7425	0.5520
B to Z ↑	0.0244	0.0242	1.1038	0.8324
	X42_P4		**X42_P4**	
A to Z ↓	0.0270		0.4482	
A to Z ↑	0.0257		0.6663	
B to Z ↓	0.0250		0.4472	
B to Z ↑	0.0264		0.6668	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	3.251e-05	1.000e-20
X16_P4	7.071e-05	1.000e-20
X25_P4	1.029e-04	1.000e-20
X33_P4	1.421e-04	1.000e-20
X42_P4	1.653e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	9.377e-06	1.843e-05	2.827e-05	7.330e-05
B (output stable)	1.920e-05	3.453e-05	5.394e-05	2.079e-04
A to Z	1.999e-03	3.367e-03	5.157e-03	6.821e-03
B to Z	1.920e-03	3.228e-03	4.946e-03	6.295e-03
	X42_P4			
A (output stable)	7.355e-05			
B (output stable)	2.063e-04			
A to Z	8.184e-03			
B to Z	7.670e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

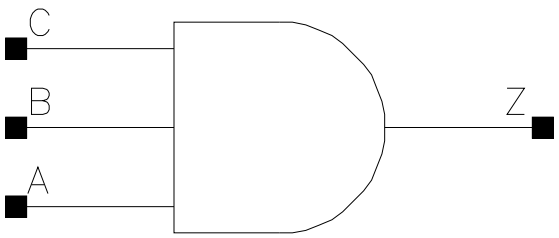
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X25_P4	1.200	1.360	1.6320
X33_P4	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0007	0.0010	0.0016	0.0020
B	0.0006	0.0010	0.0015	0.0018
C	0.0006	0.0010	0.0013	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0337	0.0276	2.2435	1.0947
A to Z ↑	0.0328	0.0302	3.4787	1.6575
B to Z ↓	0.0325	0.0264	2.2436	1.0942
B to Z ↑	0.0337	0.0311	3.4771	1.6576
C to Z ↓	0.0313	0.0251	2.2394	1.0926
C to Z ↑	0.0348	0.0315	3.4715	1.6577
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0277	0.0262	0.7506	0.5606

A to Z ↑	0.0294	0.0284	1.1270	0.8448
B to Z ↓	0.0266	0.0250	0.7488	0.5613
B to Z ↑	0.0304	0.0294	1.1283	0.8454
C to Z ↓	0.0252	0.0238	0.7480	0.5604
C to Z ↑	0.0310	0.0300	1.1290	0.8453

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	3.157e-05	1.000e-20
X17_P4	6.993e-05	1.000e-20
X25_P4	9.939e-05	1.000e-20
X33_P4	1.367e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	1.099e-05	2.290e-05	3.033e-05	4.146e-05
B (output stable)	1.347e-05	2.596e-05	3.709e-05	5.098e-05
C (output stable)	3.252e-05	6.237e-05	9.407e-05	1.315e-04
A to Z	2.219e-03	3.905e-03	5.629e-03	7.282e-03
B to Z	2.130e-03	3.745e-03	5.384e-03	6.956e-03
C to Z	2.060e-03	3.591e-03	5.155e-03	6.645e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

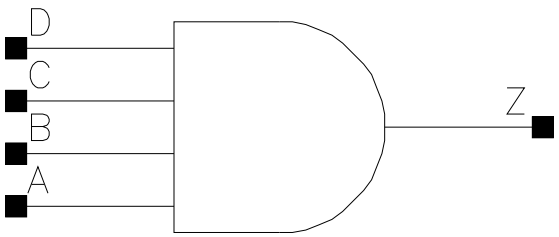
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X6_P4	1.200	1.088	1.3056
X20_P4	1.200	2.312	2.7744
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P4	X6_P4	X20_P4	X27_P4
A	0.0005	0.0007	0.0017	0.0019
B	0.0005	0.0007	0.0017	0.0019
C	0.0004	0.0007	0.0016	0.0019
D	0.0005	0.0007	0.0016	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X6_P4	X4_P4	X6_P4
A to Z ↓	0.0354	0.0303	4.2390	2.7404
A to Z ↑	0.0342	0.0262	11.9271	6.3094
B to Z ↓	0.0345	0.0286	4.2420	2.7381
B to Z ↑	0.0360	0.0272	11.9253	6.3094
C to Z ↓	0.0368	0.0327	4.2120	2.7478
C to Z ↑	0.0345	0.0262	11.9331	6.3166

D to Z ↓	0.0359	0.0306	4.2048	2.7439
D to Z ↑	0.0370	0.0273	11.9420	6.3160
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0291	0.0267	0.7925	0.5595
A to Z ↑	0.0269	0.0300	2.0974	1.5915
B to Z ↓	0.0266	0.0246	0.7908	0.5589
B to Z ↑	0.0272	0.0306	2.0975	1.5921
C to Z ↓	0.0284	0.0259	0.7975	0.5610
C to Z ↑	0.0240	0.0264	2.0974	1.5903
D to Z ↓	0.0256	0.0240	0.7954	0.5607
D to Z ↑	0.0241	0.0271	2.0963	1.5907

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.461e-05	1.000e-20
X6_P4	3.873e-05	1.000e-20
X20_P4	1.194e-04	1.000e-20
X27_P4	1.548e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	3.300e-04	5.229e-04	1.545e-03	1.883e-03
B (output stable)	3.113e-04	4.833e-04	1.410e-03	1.742e-03
C (output stable)	3.237e-04	5.433e-04	1.361e-03	1.686e-03
D (output stable)	3.089e-04	5.009e-04	1.211e-03	1.543e-03
A to Z	1.386e-03	2.166e-03	6.551e-03	8.443e-03
B to Z	1.334e-03	2.059e-03	6.047e-03	7.925e-03
C to Z	1.394e-03	2.239e-03	5.684e-03	7.173e-03
D to Z	1.341e-03	2.124e-03	5.162e-03	6.685e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

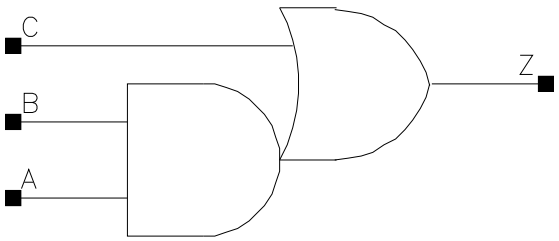
Pin Cycle (vdds)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0019
B	0.0006	0.0010	0.0018
C	0.0007	0.0010	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0388	0.0339	2.2733	1.1102
A to Z ↑	0.0262	0.0233	3.3614	1.6439
B to Z ↓	0.0362	0.0316	2.2669	1.1082
B to Z ↑	0.0280	0.0250	3.3601	1.6452
C to Z ↓	0.0382	0.0335	2.2637	1.1066
C to Z ↑	0.0240	0.0224	3.3427	1.6368
	X33_P4		**X33_P4**	
A to Z ↓	0.0334		0.5629	
A to Z ↑	0.0234		0.8282	

B to Z ↓	0.0311		0.5616	
B to Z ↑	0.0245		0.8281	
C to Z ↓	0.0332		0.5611	
C to Z ↑	0.0218		0.8247	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	3.200e-05	1.000e-20
X17_P4	6.910e-05	1.000e-20
X33_P4	1.368e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	3.397e-05	5.358e-05	1.268e-04
B (output stable)	3.817e-05	6.243e-05	1.582e-04
C (output stable)	4.297e-05	7.283e-05	1.684e-04
A to Z	2.080e-03	3.635e-03	7.074e-03
B to Z	1.992e-03	3.464e-03	6.665e-03
C to Z	2.240e-03	3.911e-03	7.662e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

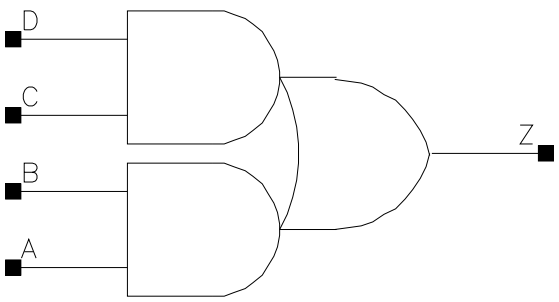
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0018
B	0.0007	0.0010	0.0017
C	0.0006	0.0009	0.0019
D	0.0006	0.0010	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0447	0.0379	2.1893	1.1030
A to Z ↑	0.0337	0.0301	3.3134	1.6477
B to Z ↓	0.0417	0.0352	2.1789	1.0995
B to Z ↑	0.0347	0.0313	3.3116	1.6467

C to Z ↓	0.0401	0.0347	2.1819	1.0999
C to Z ↑	0.0286	0.0256	3.3052	1.6432
D to Z ↓	0.0386	0.0331	2.1768	1.0980
D to Z ↑	0.0307	0.0273	3.3045	1.6415
	X33_P4		**X33_P4**	
A to Z ↓	0.0362		0.5637	
A to Z ↑	0.0278		0.8320	
B to Z ↓	0.0343		0.5630	
B to Z ↑	0.0295		0.8319	
C to Z ↓	0.0330		0.5623	
C to Z ↑	0.0239		0.8287	
D to Z ↓	0.0312		0.5615	
D to Z ↑	0.0254		0.8288	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	3.821e-05	1.000e-20
X17_P4	8.151e-05	1.000e-20
X33_P4	1.570e-04	1.000e-20

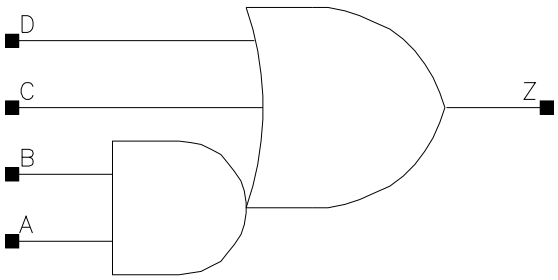
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.682e-05	3.769e-05	5.265e-05
B (output stable)	8.434e-05	1.083e-04	7.094e-05
C (output stable)	3.214e-05	5.274e-05	1.229e-04
D (output stable)	3.638e-05	6.257e-05	1.479e-04
A to Z	2.742e-03	4.572e-03	8.551e-03
B to Z	2.545e-03	4.280e-03	8.186e-03
C to Z	2.349e-03	3.955e-03	7.297e-03
D to Z	2.272e-03	3.804e-03	6.980e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description	Logical Symbol
2 input AND into 3 input OR	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	0.952	1.1424
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0017
B	0.0006	0.0009	0.0018
C	0.0006	0.0009	0.0018
D	0.0006	0.0009	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0508	0.0434	2.3671	1.1630
A to Z ↑	0.0284	0.0254	3.3568	1.6950
B to Z ↓	0.0490	0.0408	2.3609	1.1604
B to Z ↑	0.0303	0.0266	3.3556	1.6957
C to Z ↓	0.0532	0.0451	2.3568	1.1595
C to Z ↑	0.0260	0.0239	3.3310	1.6871

D to Z ↓	0.0526	0.0451	2.3560	1.1603
D to Z ↑	0.0256	0.0237	3.3316	1.6868
	X33_P4		**X33_P4**	
A to Z ↓	0.0440		0.5829	
A to Z ↑	0.0253		0.8286	
B to Z ↓	0.0398		0.5798	
B to Z ↑	0.0260		0.8294	
C to Z ↓	0.0465		0.5800	
C to Z ↑	0.0234		0.8259	
D to Z ↓	0.0452		0.5801	
D to Z ↑	0.0226		0.8244	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	2.791e-05	1.000e-20
X17_P4	6.060e-05	1.000e-20
X33_P4	1.213e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	4.042e-05	7.586e-05	1.787e-04
B (output stable)	4.058e-05	7.400e-05	1.989e-04
C (output stable)	2.193e-05	4.124e-05	1.211e-04
D (output stable)	2.843e-05	5.346e-05	1.921e-04
A to Z	2.363e-03	4.005e-03	8.034e-03
B to Z	2.287e-03	3.828e-03	7.450e-03
C to Z	2.628e-03	4.466e-03	9.109e-03
D to Z	2.502e-03	4.253e-03	8.472e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

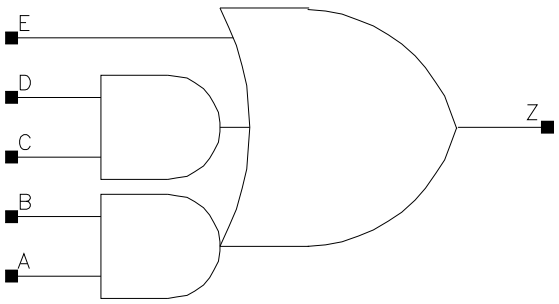
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.088	1.3056
X17_P4	1.200	1.224	1.4688
X33_P4	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0018
B	0.0006	0.0009	0.0017
C	0.0007	0.0011	0.0018
D	0.0006	0.0009	0.0017
E	0.0006	0.0009	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0621	0.0517	2.2528	1.1313
A to Z ↑	0.0354	0.0306	3.2949	1.6562

B to Z ↓	0.0603	0.0494	2.2454	1.1286
B to Z ↑	0.0379	0.0324	3.2943	1.6555
C to Z ↓	0.0528	0.0455	2.2445	1.1285
C to Z ↑	0.0301	0.0259	3.2649	1.6458
D to Z ↓	0.0495	0.0417	2.2352	1.1234
D to Z ↑	0.0320	0.0273	3.2640	1.6444
E to Z ↓	0.0549	0.0459	2.2329	1.1240
E to Z ↑	0.0272	0.0238	3.2407	1.6343
	X33_P4		**X33_P4**	
A to Z ↓	0.0511		0.5826	
A to Z ↑	0.0314		0.8359	
B to Z ↓	0.0480		0.5807	
B to Z ↑	0.0331		0.8355	
C to Z ↓	0.0437		0.5808	
C to Z ↑	0.0258		0.8294	
D to Z ↓	0.0405		0.5783	
D to Z ↑	0.0272		0.8286	
E to Z ↓	0.0448		0.5785	
E to Z ↑	0.0237		0.8243	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	3.463e-05	1.000e-20
X17_P4	7.331e-05	1.000e-20
X33_P4	1.384e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	1.395e-05	2.261e-05	5.191e-05
B (output stable)	1.829e-05	2.599e-05	6.576e-05
C (output stable)	5.019e-05	6.897e-05	1.749e-04
D (output stable)	5.939e-05	8.444e-05	1.946e-04
E (output stable)	8.762e-05	1.147e-04	2.681e-04
A to Z	3.186e-03	5.170e-03	1.016e-02
B to Z	3.105e-03	4.984e-03	9.657e-03
C to Z	2.570e-03	4.261e-03	8.176e-03
D to Z	2.471e-03	4.052e-03	7.731e-03
E to Z	2.754e-03	4.502e-03	8.672e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

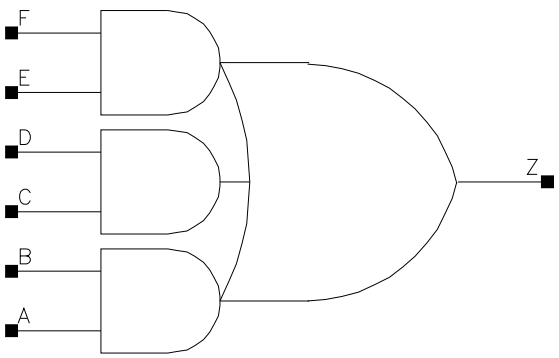
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.360	1.6320
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
A	0.0006	0.0007	0.0009	0.0018

B	0.0006	0.0007	0.0012	0.0016
C	0.0006	0.0006	0.0009	0.0018
D	0.0006	0.0007	0.0009	0.0016
E	0.0006	0.0007	0.0009	0.0018
F	0.0006	0.0007	0.0009	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0626	0.0588	4.4049	2.2555
A to Z ↑	0.0380	0.0362	6.5987	3.3491
B to Z ↓	0.0577	0.0546	4.3743	2.2406
B to Z ↑	0.0387	0.0372	6.5928	3.3486
C to Z ↓	0.0566	0.0538	4.3889	2.2481
C to Z ↑	0.0343	0.0327	6.5530	3.3299
D to Z ↓	0.0544	0.0517	4.3760	2.2408
D to Z ↑	0.0366	0.0349	6.5530	3.3286
E to Z ↓	0.0472	0.0461	4.3715	2.2400
E to Z ↑	0.0290	0.0279	6.5164	3.3133
F to Z ↓	0.0444	0.0434	4.3581	2.2325
F to Z ↑	0.0307	0.0296	6.5194	3.3118
	X17_P4	X33_P4	X17_P4	X33_P4
A to Z ↓	0.0553	0.0530	1.1363	0.5805
A to Z ↑	0.0336	0.0335	1.6610	0.8389
B to Z ↓	0.0521	0.0502	1.1285	0.5792
B to Z ↑	0.0352	0.0352	1.6602	0.8382
C to Z ↓	0.0513	0.0492	1.1328	0.5803
C to Z ↑	0.0305	0.0310	1.6525	0.8337
D to Z ↓	0.0487	0.0466	1.1289	0.5787
D to Z ↑	0.0324	0.0326	1.6526	0.8334
E to Z ↓	0.0437	0.0443	1.1289	0.5790
E to Z ↑	0.0257	0.0270	1.6450	0.8311
F to Z ↓	0.0412	0.0411	1.1247	0.5767
F to Z ↑	0.0273	0.0285	1.6450	0.8304

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	2.655e-05	1.000e-20
X8_P4	4.699e-05	1.000e-20
X17_P4	8.552e-05	1.000e-20
X33_P4	1.603e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	2.756e-05	3.196e-05	4.059e-05	7.445e-05
B (output stable)	6.801e-05	7.490e-05	7.850e-05	1.001e-04
C (output stable)	3.011e-05	3.601e-05	4.575e-05	1.045e-04
D (output stable)	3.467e-05	4.209e-05	5.266e-05	1.383e-04
E (output stable)	8.491e-05	1.062e-04	1.337e-04	2.230e-04
F (output stable)	8.693e-05	1.070e-04	1.409e-04	2.518e-04

A to Z	2.754e-03	3.746e-03	5.764e-03	1.090e-02
B to Z	2.536e-03	3.488e-03	5.415e-03	1.042e-02
C to Z	2.346e-03	3.257e-03	5.108e-03	9.671e-03
D to Z	2.260e-03	3.145e-03	4.922e-03	9.238e-03
E to Z	1.912e-03	2.765e-03	4.366e-03	8.561e-03
F to Z	1.827e-03	2.650e-03	4.189e-03	8.129e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

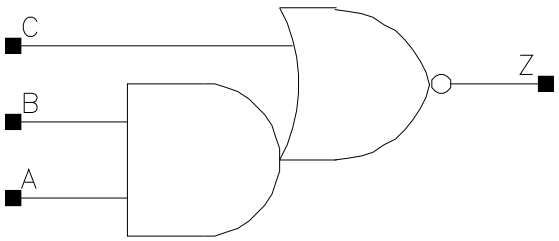
Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008
X44_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X33_P4	X44_P4
A	0.0007	0.0021	0.0043	0.0058
B	0.0007	0.0020	0.0039	0.0053
C	0.0008	0.0023	0.0045	0.0059

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0101	0.0105	4.0084	1.3548
A to Z ↑	0.0173	0.0176	6.4242	2.1378
B to Z ↓	0.0104	0.0106	4.0355	1.3676
B to Z ↑	0.0145	0.0143	6.3412	2.1372
C to Z ↓	0.0103	0.0104	2.2701	0.7748
C to Z ↑	0.0177	0.0175	5.8785	1.9704
	X33_P4	**X44_P4**	**X33_P4**	**X44_P4**
A to Z ↓	0.0108	0.0107	0.6876	0.5218

A to Z ↑	0.0177	0.0176	1.0710	0.8115
B to Z ↓	0.0106	0.0106	0.6940	0.5264
B to Z ↑	0.0142	0.0141	1.0688	0.8077
C to Z ↓	0.0120	0.0121	0.4614	0.3591
C to Z ↑	0.0178	0.0177	0.9859	0.7459

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P4	2.834e-05	1.000e-20
X17_P4	8.174e-05	1.000e-20
X33_P4	1.568e-04	1.000e-20
X44_P4	2.079e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	5.537e-05	1.607e-04	3.685e-04	4.770e-04
B (output stable)	6.153e-05	2.058e-04	4.578e-04	5.878e-04
C (output stable)	7.187e-05	2.165e-04	4.782e-04	6.286e-04
A to Z	9.962e-04	3.132e-03	6.310e-03	8.326e-03
B to Z	8.531e-04	2.511e-03	5.014e-03	6.614e-03
C to Z	1.341e-03	3.991e-03	8.067e-03	1.061e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

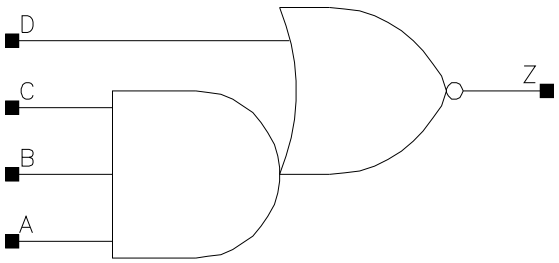
Pin Cycle (vdds)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X29_P4	1.200	3.536	4.2432
X38_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X29_P4	X38_P4
A	0.0008	0.0044	0.0058
B	0.0007	0.0042	0.0055
C	0.0007	0.0040	0.0052
D	0.0008	0.0045	0.0056

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X29_P4	X5_P4	X29_P4
A to Z ↓	0.0152	0.0160	5.7615	0.9886
A to Z ↑	0.0222	0.0220	6.4228	1.0620
B to Z ↓	0.0156	0.0158	5.7758	0.9920
B to Z ↑	0.0200	0.0196	6.4175	1.0678
C to Z ↓	0.0155	0.0150	5.7870	0.9953
C to Z ↑	0.0174	0.0165	6.3467	1.0739
D to Z ↓	0.0125	0.0143	2.3097	0.4650

D to Z ↑	0.0206	0.0209	5.4848	0.9153
	X38_P4		**X38_P4**	
A to Z ↓	0.0157		0.7616	
A to Z ↑	0.0215		0.8001	
B to Z ↓	0.0156		0.7645	
B to Z ↑	0.0191		0.8061	
C to Z ↓	0.0148		0.7669	
C to Z ↑	0.0160		0.8132	
D to Z ↓	0.0151		0.3881	
D to Z ↑	0.0203		0.6905	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.790e-05	1.000e-20
X29_P4	1.529e-04	1.000e-20
X38_P4	1.985e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X29_P4	X38_P4
A (output stable)	3.060e-05	2.615e-04	3.361e-04
B (output stable)	3.364e-05	2.791e-04	3.597e-04
C (output stable)	4.926e-05	4.614e-04	5.830e-04
D (output stable)	9.121e-05	6.894e-04	8.997e-04
A to Z	1.404e-03	8.749e-03	1.118e-02
B to Z	1.242e-03	7.360e-03	9.446e-03
C to Z	1.092e-03	6.043e-03	7.725e-03
D to Z	1.715e-03	1.039e-02	1.331e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

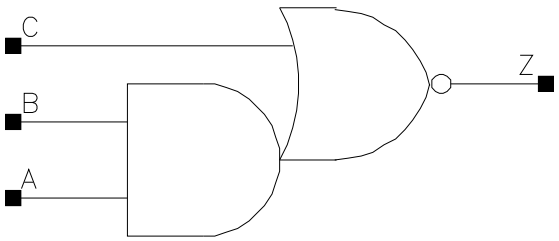
Pin Cycle (vdds)	X5_P4	X29_P4	X38_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X11_P4	1.200	1.088	1.3056
X16_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X11_P4	X16_P4	X23_P4
A	0.0008	0.0016	0.0024	0.0031
B	0.0008	0.0015	0.0022	0.0029
C	0.0008	0.0014	0.0020	0.0029
	X46_P4			
A	0.0059			
B	0.0056			
C	0.0057			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X11_P4	X6_P4	X11_P4
A to Z ↓	0.0121	0.0130	3.9032	1.9689
A to Z ↑	0.0191	0.0201	6.4195	3.1345
B to Z ↓	0.0130	0.0131	3.9260	1.9832

B to Z ↑	0.0168	0.0171	6.3549	3.1419
C to Z ↓	0.0073	0.0078	2.3273	1.3732
C to Z ↑	0.0144	0.0138	5.8966	2.8977
	X16_P4	**X23_P4**	**X16_P4**	**X23_P4**
A to Z ↓	0.0124	0.0127	1.3560	1.0188
A to Z ↑	0.0187	0.0191	2.1063	1.5930
B to Z ↓	0.0129	0.0128	1.3665	1.0265
B to Z ↑	0.0157	0.0159	2.1050	1.5976
C to Z ↓	0.0079	0.0068	0.9578	0.5939
C to Z ↑	0.0131	0.0138	1.9467	1.4726
	X46_P4		**X46_P4**	
A to Z ↓	0.0122		0.5215	
A to Z ↑	0.0182		0.8215	
B to Z ↓	0.0125		0.5254	
B to Z ↑	0.0150		0.8196	
C to Z ↓	0.0071		0.3038	
C to Z ↑	0.0137		0.7578	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P4	2.830e-05	1.000e-20
X11_P4	5.685e-05	1.000e-20
X16_P4	8.004e-05	1.000e-20
X23_P4	1.117e-04	1.000e-20
X46_P4	2.168e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	1.890e-05	5.460e-05	6.983e-05	1.000e-04
B (output stable)	2.529e-05	9.782e-05	1.041e-04	1.615e-04
C (output stable)	2.116e-04	5.399e-04	6.219e-04	8.490e-04
A to Z	1.346e-03	2.939e-03	4.009e-03	5.470e-03
B to Z	1.187e-03	2.465e-03	3.339e-03	4.501e-03
C to Z	8.597e-04	1.732e-03	2.390e-03	3.376e-03
	X46_P4			
A (output stable)	1.775e-04			
B (output stable)	2.807e-04			
C (output stable)	1.404e-03			
A to Z	1.010e-02			
B to Z	8.326e-03			
C to Z	6.442e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

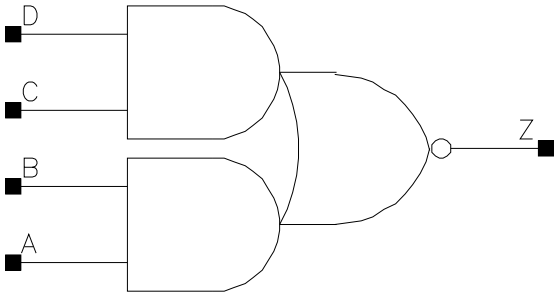
	X46_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P4	X10_P4	X16_P4	X21_P4
A	0.0006	0.0016	0.0024	0.0030
B	0.0006	0.0014	0.0022	0.0029
C	0.0006	0.0015	0.0022	0.0029
D	0.0006	0.0013	0.0020	0.0027
	X42_P4			
A	0.0061			
B	0.0057			
C	0.0057			
D	0.0054			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X10_P4**	**X4_P4**	**X10_P4**
A to Z ↓	0.0137	0.0136	4.8761	1.9075
A to Z ↑	0.0255	0.0210	8.8759	2.8882
B to Z ↓	0.0148	0.0148	4.9048	1.9212
B to Z ↑	0.0229	0.0191	8.8529	2.9460
C to Z ↓	0.0102	0.0098	4.9568	1.9158
C to Z ↑	0.0202	0.0172	8.8554	2.8981
D to Z ↓	0.0108	0.0105	4.9996	1.9325
D to Z ↑	0.0175	0.0149	8.8308	2.9328
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0147	0.0145	1.3612	1.0219
A to Z ↑	0.0220	0.0216	1.9449	1.4961
B to Z ↓	0.0155	0.0150	1.3698	1.0290
B to Z ↑	0.0192	0.0189	1.9448	1.4977
C to Z ↓	0.0107	0.0108	1.3590	1.0217
C to Z ↑	0.0178	0.0181	1.9429	1.4929
D to Z ↓	0.0110	0.0106	1.3712	1.0311
D to Z ↑	0.0148	0.0149	1.9441	1.4943
	X42_P4		**X42_P4**	
A to Z ↓	0.0151		0.5281	
A to Z ↑	0.0218		0.7512	
B to Z ↓	0.0154		0.5318	
B to Z ↑	0.0188		0.7485	
C to Z ↓	0.0112		0.5239	
C to Z ↑	0.0182		0.7507	
D to Z ↓	0.0111		0.5286	
D to Z ↑	0.0151		0.7487	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	2.168e-05	1.000e-20
X10_P4	6.954e-05	1.000e-20
X16_P4	9.769e-05	1.000e-20
X21_P4	1.310e-04	1.000e-20
X42_P4	2.561e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	2.139e-05	4.954e-05	1.000e-04	1.364e-04
B (output stable)	2.880e-05	7.061e-05	1.770e-04	2.585e-04
C (output stable)	5.436e-05	1.215e-04	2.111e-04	2.708e-04
D (output stable)	6.389e-05	1.467e-04	2.907e-04	3.885e-04
A to Z	1.349e-03	3.306e-03	5.179e-03	6.663e-03
B to Z	1.205e-03	2.957e-03	4.477e-03	5.764e-03
C to Z	8.508e-04	2.183e-03	3.404e-03	4.557e-03
D to Z	7.312e-04	1.880e-03	2.776e-03	3.670e-03
	X42_P4			
A (output stable)	2.606e-04			
B (output stable)	4.636e-04			
C (output stable)	5.134e-04			
D (output stable)	7.178e-04			

A to Z	1.311e-02			
B to Z	1.130e-02			
C to Z	8.894e-03			
D to Z	7.229e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

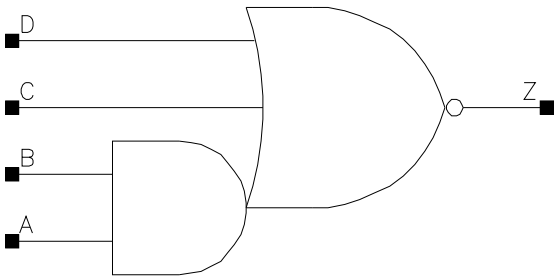
Pin Cycle (vdds)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X35_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P4	X35_P4
A	0.0007	0.0056
B	0.0007	0.0050
C	0.0008	0.0054
D	0.0008	0.0050

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X35_P4	X5_P4	X35_P4
A to Z ↓	0.0120	0.0123	4.0494	0.5918
A to Z ↑	0.0233	0.0216	9.4057	1.1944
B to Z ↓	0.0126	0.0125	4.0795	0.5970
B to Z ↑	0.0199	0.0177	9.3504	1.1931
C to Z ↓	0.0125	0.0164	2.3925	0.4617
C to Z ↑	0.0259	0.0250	8.8882	1.1300
D to Z ↓	0.0121	0.0151	2.4136	0.4610

D to Z ↑	0.0255	0.0235	8.8980	1.1327

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.352e-05	1.000e-20
X35_P4	1.681e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X35_P4
A (output stable)	7.210e-05	5.784e-04
B (output stable)	7.325e-05	6.246e-04
C (output stable)	3.940e-05	4.329e-04
D (output stable)	5.152e-05	5.764e-04
A to Z	1.181e-03	8.527e-03
B to Z	1.027e-03	6.970e-03
C to Z	1.747e-03	1.327e-02
D to Z	1.519e-03	1.088e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

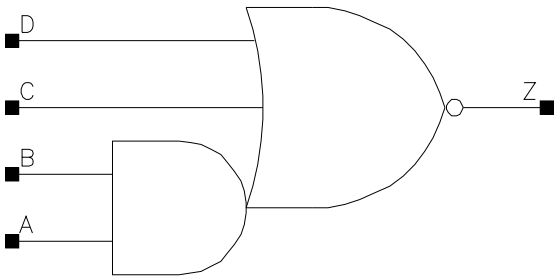
Pin Cycle (vdds)	X5_P4	X35_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X17_P4	1.200	2.448	2.9376
X34_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P4	X17_P4	X34_P4
A	0.0008	0.0031	0.0061
B	0.0007	0.0029	0.0057
C	0.0007	0.0026	0.0051
D	0.0007	0.0024	0.0047

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X17_P4	X4_P4	X17_P4
A to Z ↓	0.0141	0.0153	4.4170	1.1563
A to Z ↑	0.0254	0.0267	9.4577	2.3270
B to Z ↓	0.0154	0.0157	4.4471	1.1630
B to Z ↑	0.0226	0.0228	9.3787	2.3297
C to Z ↓	0.0132	0.0130	3.8971	0.9476
C to Z ↑	0.0186	0.0197	8.9285	2.2063

D to Z ↓	0.0112	0.0100	3.9686	0.9509
D to Z ↑	0.0173	0.0158	8.9465	2.2109
	X34_P4		**X34_P4**	
A to Z ↓	0.0150		0.5911	
A to Z ↑	0.0261		1.1827	
B to Z ↓	0.0157		0.5947	
B to Z ↑	0.0224		1.1788	
C to Z ↓	0.0133		0.4993	
C to Z ↑	0.0191		1.1192	
D to Z ↓	0.0104		0.5026	
D to Z ↑	0.0155		1.1219	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	2.156e-05	1.000e-20
X17_P4	8.598e-05	1.000e-20
X34_P4	1.685e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X17_P4	X34_P4
A (output stable)	1.764e-05	8.720e-05	1.707e-04
B (output stable)	1.964e-05	1.164e-04	2.187e-04
C (output stable)	5.634e-05	2.986e-04	5.794e-04
D (output stable)	1.066e-04	7.106e-04	1.295e-03
A to Z	1.600e-03	6.918e-03	1.332e-02
B to Z	1.445e-03	5.943e-03	1.152e-02
C to Z	1.035e-03	4.493e-03	8.527e-03
D to Z	8.241e-04	3.153e-03	6.007e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

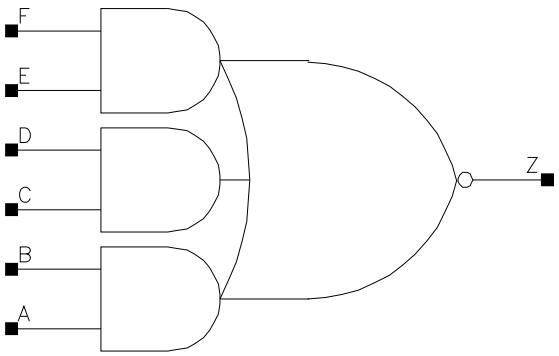
Pin Cycle (vdds)	X4_P4	X17_P4	X34_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X8_P4	1.200	2.176	2.6112
X13_P4	1.200	2.720	3.2640
X17_P4	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P4	X8_P4	X13_P4	X17_P4
A	0.0008	0.0015	0.0023	0.0030

B	0.0007	0.0014	0.0021	0.0028
C	0.0007	0.0015	0.0022	0.0028
D	0.0007	0.0014	0.0020	0.0026
E	0.0009	0.0014	0.0021	0.0027
F	0.0007	0.0013	0.0019	0.0025

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0169	0.0203	3.9011	2.2487
A to Z ↑	0.0372	0.0364	9.0856	4.1843
B to Z ↓	0.0187	0.0212	3.9213	2.2578
B to Z ↑	0.0343	0.0331	9.0774	4.1916
C to Z ↓	0.0153	0.0182	3.8722	2.2563
C to Z ↑	0.0324	0.0327	9.1270	4.2002
D to Z ↓	0.0167	0.0193	3.8982	2.2690
D to Z ↑	0.0295	0.0292	9.0879	4.1977
E to Z ↓	0.0117	0.0139	3.8097	2.2577
E to Z ↑	0.0254	0.0253	9.0471	4.1742
F to Z ↓	0.0124	0.0143	3.8467	2.2766
F to Z ↑	0.0224	0.0216	9.0959	4.1768
	X13_P4	X17_P4	X13_P4	X17_P4
A to Z ↓	0.0193	0.0195	1.5253	1.1613
A to Z ↑	0.0337	0.0339	2.7695	2.1132
B to Z ↓	0.0207	0.0204	1.5312	1.1661
B to Z ↑	0.0307	0.0304	2.7772	2.1134
C to Z ↓	0.0174	0.0174	1.5357	1.1517
C to Z ↑	0.0297	0.0301	2.7832	2.1255
D to Z ↓	0.0186	0.0181	1.5434	1.1582
D to Z ↑	0.0268	0.0267	2.7859	2.1218
E to Z ↓	0.0133	0.0132	1.5314	1.1528
E to Z ↑	0.0235	0.0235	2.7710	2.1090
F to Z ↓	0.0138	0.0132	1.5434	1.1625
F to Z ↑	0.0201	0.0200	2.7740	2.1157

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	3.742e-05	1.000e-20
X8_P4	7.717e-05	1.000e-20
X13_P4	1.095e-04	1.000e-20
X17_P4	1.460e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

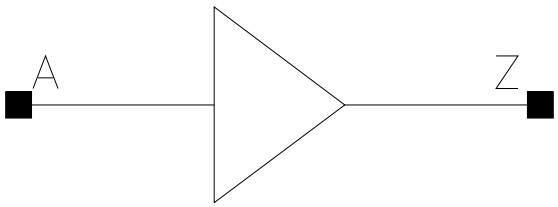
Pin Cycle (vdd)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	3.400e-05	8.097e-05	1.125e-04	1.520e-04
B (output stable)	3.891e-05	1.301e-04	1.516e-04	2.331e-04
C (output stable)	5.574e-05	1.200e-04	1.582e-04	2.119e-04
D (output stable)	6.210e-05	1.790e-04	2.033e-04	2.917e-04
E (output stable)	1.156e-04	2.846e-04	3.649e-04	4.955e-04
F (output stable)	1.345e-04	3.409e-04	4.129e-04	5.718e-04

A to Z	2.542e-03	5.341e-03	7.369e-03	9.787e-03
B to Z	2.356e-03	4.858e-03	6.736e-03	8.813e-03
C to Z	1.938e-03	4.250e-03	5.690e-03	7.590e-03
D to Z	1.775e-03	3.804e-03	5.124e-03	6.725e-03
E to Z	1.336e-03	3.001e-03	3.996e-03	5.309e-03
F to Z	1.187e-03	2.553e-03	3.434e-03	4.476e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.408	0.4896
X6_P4	1.200	0.408	0.4896
X8_P4	1.200	0.408	0.4896
X13_P4	1.200	0.544	0.6528
X16_P4	1.200	0.544	0.6528
X21_P4	1.200	0.680	0.8160
X25_P4	1.200	0.680	0.8160
X29_P4	1.200	0.952	1.1424
X33_P4	1.200	0.952	1.1424
X42_P4	1.200	1.088	1.3056
X50_P4	1.200	1.224	1.4688
X58_P4	1.200	1.496	1.7952
X67_P4	1.200	1.632	1.9584
X75_P4	1.200	1.768	2.1216
X84_P4	1.200	1.904	2.2848
X100_P4	1.200	2.312	2.7744
X134_P4	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0008	0.0008	0.0008	0.0008
	X16_P4	X21_P4	X25_P4	X29_P4
A	0.0008	0.0011	0.0011	0.0014
	X33_P4	X42_P4	X50_P4	X58_P4
A	0.0014	0.0016	0.0019	0.0028

	X67_P4	X75_P4	X84_P4	X100_P4
A	0.0028	0.0028	0.0028	0.0037
	X134_P4			
A	0.0046			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0248	0.0250	4.1631	2.9880
A to Z ↑	0.0200	0.0197	6.4447	4.7171
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0260	0.0290	2.1923	1.4247
A to Z ↑	0.0204	0.0229	3.3515	2.1975
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0312	0.0256	1.1232	0.8725
A to Z ↑	0.0241	0.0208	1.6773	1.3168
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0271	0.0258	0.7432	0.6302
A to Z ↑	0.0218	0.0199	1.1020	0.9403
	X33_P4	**X42_P4**	**X33_P4**	**X42_P4**
A to Z ↓	0.0272	0.0263	0.5575	0.4523
A to Z ↑	0.0208	0.0211	0.8242	0.6625
	X50_P4	**X58_P4**	**X50_P4**	**X58_P4**
A to Z ↓	0.0255	0.0238	0.3755	0.3241
A to Z ↑	0.0206	0.0195	0.5503	0.4727
	X67_P4	**X75_P4**	**X67_P4**	**X75_P4**
A to Z ↓	0.0249	0.0264	0.2845	0.2556
A to Z ↑	0.0202	0.0215	0.4145	0.3700
	X84_P4	**X100_P4**	**X84_P4**	**X100_P4**
A to Z ↓	0.0275	0.0258	0.2312	0.1942
A to Z ↑	0.0222	0.0210	0.3342	0.2795
	X134_P4		**X134_P4**	
A to Z ↓	0.0271		0.1500	
A to Z ↑	0.0222		0.2133	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.899e-05	1.000e-20
X6_P4	2.446e-05	1.000e-20
X8_P4	3.217e-05	1.000e-20
X13_P4	4.088e-05	1.000e-20
X16_P4	5.407e-05	1.000e-20
X21_P4	7.531e-05	1.000e-20
X25_P4	8.725e-05	1.000e-20
X29_P4	9.728e-05	1.000e-20
X33_P4	1.079e-04	1.000e-20
X42_P4	1.370e-04	1.000e-20
X50_P4	1.670e-04	1.000e-20
X58_P4	2.068e-04	1.000e-20
X67_P4	2.268e-04	1.000e-20
X75_P4	2.468e-04	1.000e-20

X84_P4	2.667e-04	1.000e-20
X100_P4	3.266e-04	1.000e-20
X134_P4	4.264e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	1.369e-03	1.536e-03	1.831e-03	2.453e-03
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	3.012e-03	3.960e-03	4.559e-03	5.054e-03
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	5.660e-03	7.112e-03	8.273e-03	1.011e-02
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	1.122e-02	1.273e-02	1.395e-02	1.657e-02
	X134_P4			
A to Z	2.271e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

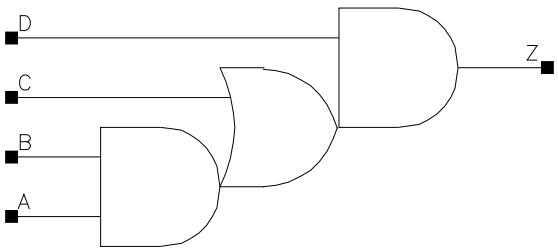
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P4			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.632	1.9584
X25_P4	1.200	1.768	2.1216
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0009	0.0019	0.0019	0.0019
B	0.0009	0.0017	0.0017	0.0017
C	0.0010	0.0022	0.0022	0.0022
D	0.0014	0.0018	0.0018	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0330	0.0311	2.2376	1.1076
A to Z ↑	0.0315	0.0296	3.3997	1.6534
B to Z ↓	0.0306	0.0283	2.2321	1.1047
B to Z ↑	0.0319	0.0294	3.3971	1.6507
C to Z ↓	0.0283	0.0259	2.2271	1.1034
C to Z ↑	0.0236	0.0214	3.3654	1.6374

D to Z ↓	0.0277	0.0241	2.2116	1.0970
D to Z ↑	0.0274	0.0236	3.3726	1.6408
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0340	0.0361	0.7516	0.5665
A to Z ↑	0.0324	0.0343	1.1164	0.8390
B to Z ↓	0.0314	0.0340	0.7507	0.5659
B to Z ↑	0.0323	0.0347	1.1168	0.8396
C to Z ↓	0.0290	0.0315	0.7490	0.5640
C to Z ↑	0.0238	0.0256	1.1048	0.8291
D to Z ↓	0.0261	0.0276	0.7422	0.5572
D to Z ↑	0.0258	0.0274	1.1074	0.8309

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	5.325e-05	1.000e-20
X17_P4	1.044e-04	1.000e-20
X25_P4	1.268e-04	1.000e-20
X33_P4	1.492e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	3.999e-05	8.429e-05	8.464e-05	7.351e-05
B (output stable)	5.100e-05	1.101e-04	1.113e-04	9.308e-05
C (output stable)	1.732e-04	2.769e-04	2.758e-04	2.644e-04
D (output stable)	8.935e-05	1.303e-04	1.318e-04	1.296e-04
A to Z	3.012e-03	5.523e-03	6.979e-03	8.360e-03
B to Z	2.831e-03	5.045e-03	6.496e-03	7.970e-03
C to Z	2.435e-03	4.242e-03	5.607e-03	6.925e-03
D to Z	3.076e-03	5.340e-03	6.645e-03	7.859e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

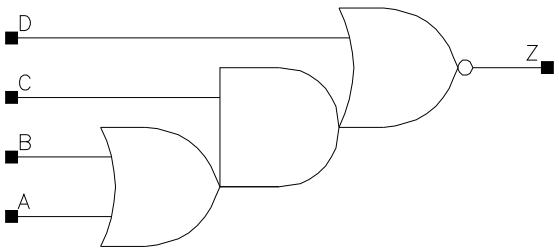
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.952	1.1424
X11_P4	1.200	1.496	1.7952
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X16_P4	X21_P4
A	0.0008	0.0015	0.0023	0.0030
B	0.0008	0.0015	0.0023	0.0030
C	0.0008	0.0015	0.0022	0.0030
D	0.0010	0.0015	0.0022	0.0029

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0150	0.0142	3.8125	1.9973
A to Z ↑	0.0312	0.0285	9.2503	4.7897
B to Z ↓	0.0144	0.0138	3.7353	1.9709
B to Z ↑	0.0295	0.0275	9.2613	4.7940
C to Z ↓	0.0137	0.0129	3.5153	1.8460
C to Z ↑	0.0193	0.0176	6.2853	3.2154

D to Z ↓	0.0082	0.0068	2.2345	1.1324
D to Z ↑	0.0178	0.0154	6.7032	3.4360
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0141	0.0144	1.3519	1.0349
A to Z ↑	0.0263	0.0279	3.0933	2.3786
B to Z ↓	0.0133	0.0137	1.3576	1.0365
B to Z ↑	0.0260	0.0267	3.0969	2.3823
C to Z ↓	0.0130	0.0131	1.2667	0.9659
C to Z ↑	0.0167	0.0170	2.1295	1.5986
D to Z ↓	0.0068	0.0069	0.7883	0.6005
D to Z ↑	0.0143	0.0143	2.2596	1.7084

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	3.188e-05	1.000e-20
X11_P4	6.060e-05	1.000e-20
X16_P4	8.523e-05	1.000e-20
X21_P4	1.132e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	2.146e-05	3.824e-05	4.997e-05	8.260e-05
B (output stable)	2.727e-05	4.571e-05	5.966e-05	1.043e-04
C (output stable)	6.493e-05	1.306e-04	1.770e-04	2.491e-04
D (output stable)	2.724e-04	5.651e-04	7.983e-04	1.136e-03
A to Z	2.075e-03	3.613e-03	5.034e-03	7.059e-03
B to Z	1.721e-03	3.045e-03	4.363e-03	5.904e-03
C to Z	1.492e-03	2.586e-03	3.670e-03	5.029e-03
D to Z	1.031e-03	1.792e-03	2.460e-03	3.276e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

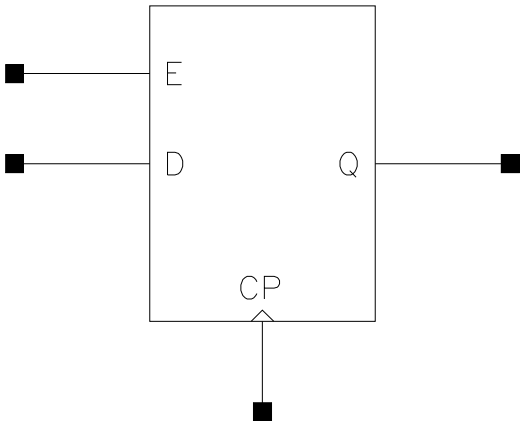
Pin Cycle (vdds)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.128	3.7536
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0011	0.0009	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0398	0.0455	2.2078	1.1373
CP to Q ↑	0.0501	0.0535	3.3859	1.6978
	X33_P4		**X33_P4**	
CP to Q ↓	0.0693		0.5639	
CP to Q ↑	0.0856		0.8400	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0524	0.0524	0.0524
CP ↑	min_pulse_width to CP	0.0317	0.0377	0.0317
D ↓	hold_rising to CP	-0.0169	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0045	-0.0045	-0.0045
D ↓	setup_rising to CP	0.0538	0.0538	0.0538
D ↑	setup_rising to CP	0.0314	0.0314	0.0314
E ↓	hold_rising to CP	-0.0089	-0.0089	-0.0089
E ↑	hold_rising to CP	-0.0071	-0.0071	-0.0071
E ↓	setup_rising to CP	0.0582	0.0582	0.0582
E ↑	setup_rising to CP	0.0591	0.0591	0.0591

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	1.178e-04	1.000e-20
X17_P4	1.386e-04	1.000e-20
X33_P4	2.060e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

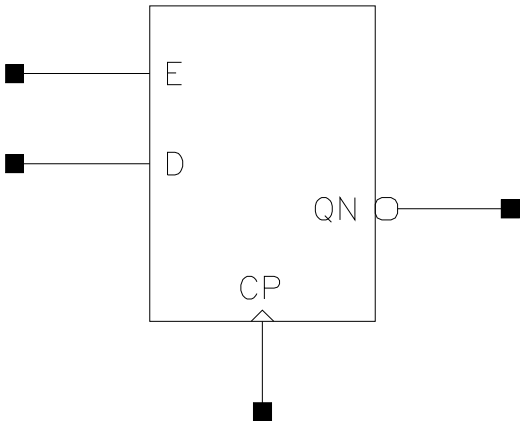
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	6.280e-03	6.280e-03	6.287e-03
Clock 100Mhz Data 25Mhz	8.301e-03	9.012e-03	1.112e-02
Clock 100Mhz Data 50Mhz	1.032e-02	1.174e-02	1.596e-02
Clock = 0 Data 100Mhz	4.026e-03	4.025e-03	4.025e-03
Clock = 1 Data 100Mhz	1.117e-03	1.117e-03	1.118e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.264	3.9168
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0009	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0703	0.0660	2.2774	1.0919
CP to QN ↑	0.0542	0.0551	3.4401	1.6524
	X33_P4		**X33_P4**	
CP to QN ↓	0.0705		0.5662	
CP to QN ↑	0.0603		0.8421	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0524	0.0524	0.0524
CP ↑	min_pulse_width to CP	0.0270	0.0317	0.0363
D ↓	hold_rising to CP	-0.0169	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0039	-0.0045	-0.0045
D ↓	setup_rising to CP	0.0538	0.0538	0.0538
D ↑	setup_rising to CP	0.0314	0.0314	0.0314
E ↓	hold_rising to CP	-0.0116	-0.0089	-0.0089
E ↑	hold_rising to CP	-0.0071	-0.0071	-0.0071
E ↓	setup_rising to CP	0.0582	0.0582	0.0582
E ↑	setup_rising to CP	0.0591	0.0591	0.0591

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	1.167e-04	1.000e-20
X17_P4	1.530e-04	1.000e-20
X33_P4	2.007e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

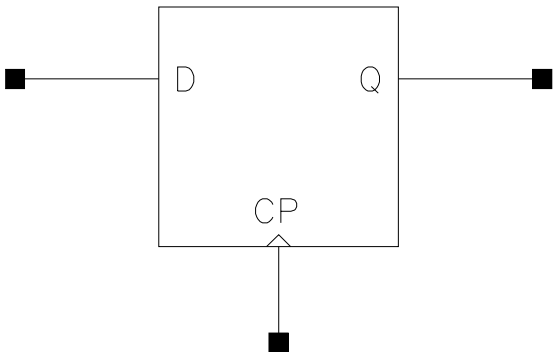
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	6.275e-03	6.277e-03	6.279e-03
Clock 100Mhz Data 25Mhz	8.321e-03	9.298e-03	1.106e-02
Clock 100Mhz Data 50Mhz	1.037e-02	1.232e-02	1.583e-02
Clock = 0 Data 100Mhz	4.025e-03	4.025e-03	4.025e-03
Clock = 1 Data 100Mhz	1.117e-03	1.117e-03	1.117e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.176	2.6112
X17_P4	1.200	2.448	2.9376
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0415	0.0456	2.1976	1.1293
CP to Q ↑	0.0510	0.0566	3.2967	1.6710
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to Q ↓	0.0573	0.0593	0.6647	0.6021
CP to Q ↑	0.0639	0.0655	0.9403	0.8546

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0477	0.0490	0.0490	0.0490
CP ↑	min_pulse_width to CP	0.0317	0.0364	0.0470	0.0504
D ↓	hold_rising to CP	0.0124	0.0128	0.0128	0.0124
D ↑	hold_rising to CP	0.0103	0.0103	0.0103	0.0103
D ↓	setup_rising to CP	0.0272	0.0268	0.0268	0.0268
D ↑	setup_rising to CP	0.0146	0.0142	0.0142	0.0142

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	9.234e-05	1.000e-20
X17_P4	1.155e-04	1.000e-20
X30_P4	1.485e-04	1.000e-20
X33_P4	1.559e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

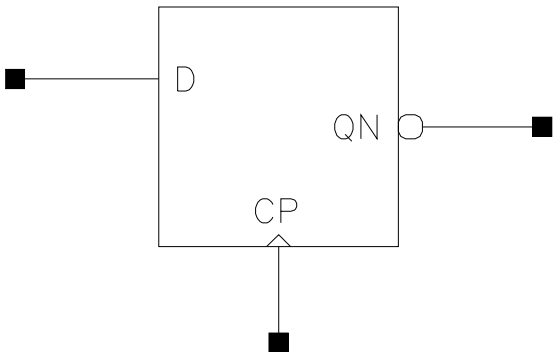
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	6.582e-03	6.616e-03	6.630e-03	6.636e-03
Clock 100Mhz Data 25Mhz	7.599e-03	8.591e-03	1.028e-02	1.069e-02
Clock 100Mhz Data 50Mhz	8.616e-03	1.056e-02	1.392e-02	1.475e-02
Clock = 0 Data 100Mhz	2.626e-03	2.709e-03	2.735e-03	2.747e-03
Clock = 1 Data 100Mhz	1.685e-05	1.674e-05	1.690e-05	1.699e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0403	0.0472	2.2547	1.1591
CP to QN ↑	0.0432	0.0459	3.2906	1.6710
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to QN ↓	0.0706	0.0710	0.6233	0.5650
CP to QN ↑	0.0563	0.0648	0.9107	0.8420

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0430	0.0463	0.0490	0.0477
CP ↑	min_pulse_width to CP	0.0316	0.0363	0.0316	0.0375
D ↓	hold_rising to CP	0.0146	0.0178	0.0134	0.0124
D ↑	hold_rising to CP	0.0123	0.0123	0.0103	0.0103
D ↓	setup_rising to CP	0.0170	0.0197	0.0268	0.0272
D ↑	setup_rising to CP	0.0200	0.0200	0.0142	0.0146

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	8.662e-05	1.000e-20
X17_P4	1.077e-04	1.000e-20
X30_P4	1.659e-04	1.000e-20
X33_P4	1.755e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

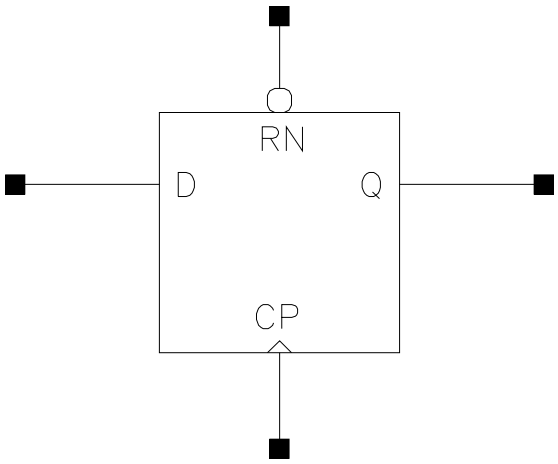
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	6.345e-03	6.346e-03	6.444e-03	6.485e-03
Clock 100Mhz Data 25Mhz	7.262e-03	8.040e-03	9.764e-03	1.035e-02
Clock 100Mhz Data 50Mhz	8.179e-03	9.733e-03	1.308e-02	1.422e-02
Clock = 0 Data 100Mhz	2.344e-03	2.345e-03	2.493e-03	2.527e-03
Clock = 1 Data 100Mhz	1.668e-05	1.673e-05	1.680e-05	1.686e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0008	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0476	0.0591	1.1386	0.6743
CP to Q ↑	0.0586	0.0656	1.6757	0.9443
RN to Q ↓	0.0798	0.1051	1.1879	0.7012

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0523	0.0523
CP ↑	min_pulse_width to CP	0.0376	0.0504
D ↓	hold_rising to CP	0.0128	0.0128
D ↑	hold_rising to CP	0.0107	0.0107
D ↓	setup_rising to CP	0.0321	0.0321
D ↑	setup_rising to CP	0.0200	0.0200
RN ↓	min_pulse_width to RN	0.0952	0.1218
RN ↑	recovery_rising to CP	0.0151	0.0147
RN ↑	removal_rising to CP	-0.0023	-0.0055

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P4	1.277e-04	1.000e-20
X30_P4	1.635e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

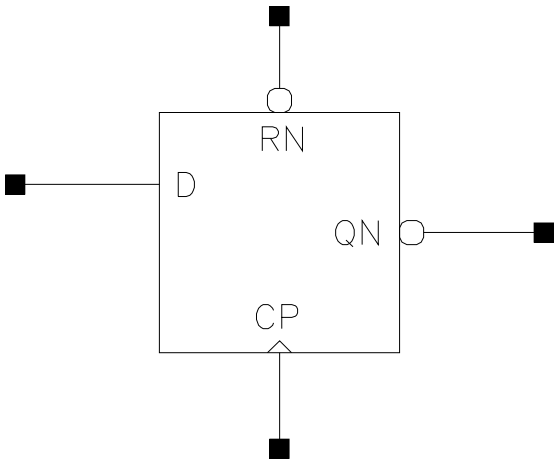
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	7.047e-03	7.046e-03
Clock 100Mhz Data 25Mhz	9.165e-03	1.082e-02
Clock 100Mhz Data 50Mhz	1.128e-02	1.460e-02
Clock = 0 Data 100Mhz	3.235e-03	3.238e-03
Clock = 1 Data 100Mhz	1.719e-05	1.713e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0683	0.0737	1.0846	0.6253
CP to QN ↑	0.0547	0.0591	1.6407	0.9147
RN to QN ↑	0.0821	0.0877	1.6435	0.9178

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0537	0.0523
CP ↑	min_pulse_width to CP	0.0316	0.0316
D ↓	hold_rising to CP	0.0107	0.0107
D ↑	hold_rising to CP	0.0107	0.0107
D ↓	setup_rising to CP	0.0321	0.0321
D ↑	setup_rising to CP	0.0200	0.0200
RN ↓	min_pulse_width to RN	0.0779	0.0828
RN ↑	recovery_rising to CP	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0023	-0.0002

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P4	1.423e-04	1.000e-20
X30_P4	1.717e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

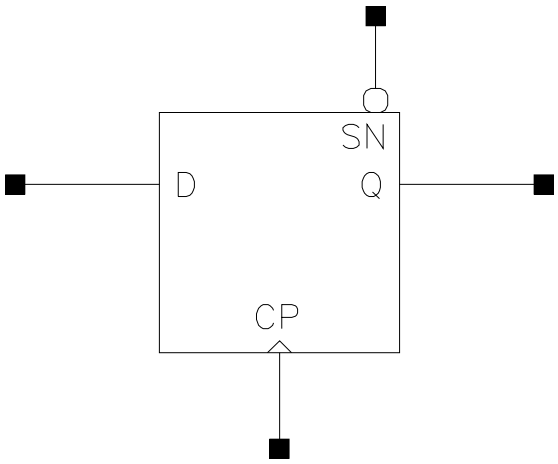
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	7.048e-03	7.047e-03
Clock 100Mhz Data 25Mhz	9.395e-03	1.056e-02
Clock 100Mhz Data 50Mhz	1.174e-02	1.408e-02
Clock = 0 Data 100Mhz	3.276e-03	3.265e-03
Clock = 1 Data 100Mhz	1.670e-05	1.700e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0478	0.0600	1.1402	0.6716
CP to Q ↑	0.0581	0.0655	1.6763	0.9441
SN to Q ↑	0.0593	0.0691	1.6836	0.9456

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0571	0.0571
CP ↑	min_pulse_width to CP	0.0411	0.0503
D ↓	hold_rising to CP	0.0075	0.0107
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0375	0.0343
D ↑	setup_rising to CP	0.0200	0.0200
SN ↓	min_pulse_width to SN	0.0576	0.0696
SN ↑	recovery_rising to CP	0.0054	0.0054
SN ↑	removal_rising to CP	0.0286	0.0286

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P4	1.224e-04	1.000e-20
X30_P4	1.523e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

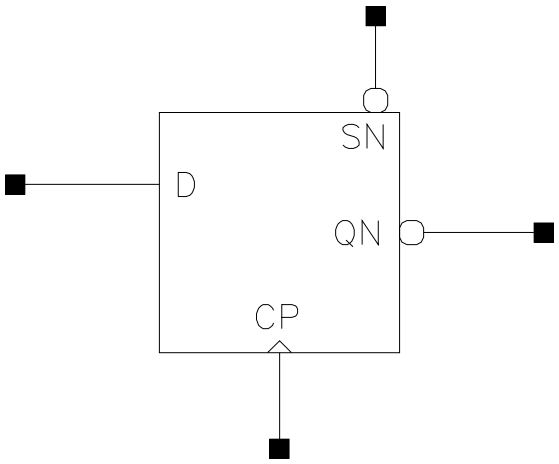
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	7.122e-03	7.109e-03
Clock 100Mhz Data 25Mhz	9.236e-03	1.090e-02
Clock 100Mhz Data 50Mhz	1.135e-02	1.469e-02
Clock = 0 Data 100Mhz	3.208e-03	3.206e-03
Clock = 1 Data 100Mhz	1.719e-05	1.729e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0678	0.0733	1.0876	0.6263
CP to QN ↑	0.0553	0.0595	1.6368	0.9132
SN to QN ↓	0.0681	0.0737	1.0878	0.6269

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0571	0.0571
CP ↑	min_pulse_width to CP	0.0316	0.0349
D ↓	hold_rising to CP	0.0075	0.0075
D ↑	hold_rising to CP	0.0107	0.0107
D ↓	setup_rising to CP	0.0375	0.0375
D ↑	setup_rising to CP	0.0200	0.0200
SN ↓	min_pulse_width to SN	0.0474	0.0500
SN ↑	recovery_rising to CP	0.0054	0.0054
SN ↑	removal_rising to CP	0.0286	0.0286

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P4	1.443e-04	1.000e-20
X30_P4	1.793e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

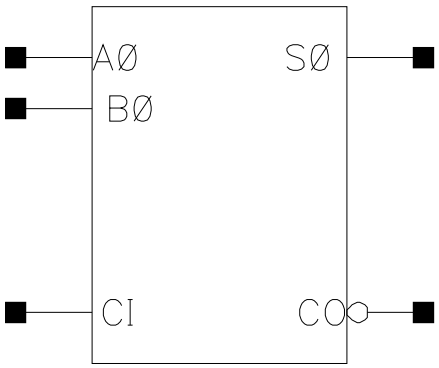
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	7.121e-03	7.116e-03
Clock 100Mhz Data 25Mhz	9.446e-03	1.061e-02
Clock 100Mhz Data 50Mhz	1.177e-02	1.410e-02
Clock = 0 Data 100Mhz	3.208e-03	3.208e-03
Clock = 1 Data 100Mhz	1.748e-05	1.743e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_P4	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_-P4	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_-P4	1.200	3.672	4.4064
C12T28SOI_LLS1_-FA1X33_P4	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4
A0	0.0030	0.0061	0.0027	0.0054
B0	0.0027	0.0060	0.0030	0.0052
CI	0.0020	0.0046	0.0021	0.0037

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4
A0 to CO ↓	0.0441	0.0476	2.2905	0.6006
A0 to CO ↑	0.0340	0.0349	3.4004	0.8703
A0 to S0 ↓	0.0464	0.0583	2.2768	0.5884
A0 to S0 ↑	0.0478	0.0582	3.3682	0.8593
B0 to CO ↓	0.0433	0.0480	2.2969	0.6028
B0 to CO ↑	0.0347	0.0363	3.4010	0.8679
B0 to S0 ↓	0.0466	0.0592	2.2778	0.5887
B0 to S0 ↑	0.0479	0.0591	3.3689	0.8595
CI to CO ↓	0.0421	0.0469	2.2978	0.6011
CI to CO ↑	0.0343	0.0351	3.3975	0.8699
CI to S0 ↓	0.0461	0.0585	2.2775	0.5888
CI to S0 ↑	0.0478	0.0592	3.3683	0.8592
	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4
A0 to CO ↓	0.0290	0.0354	4.5519	0.7855
A0 to CO ↑	0.0254	0.0290	3.4312	0.8602
A0 to S0 ↓	0.0625	0.0765	2.4429	0.6109
A0 to S0 ↑	0.0576	0.0618	3.5022	0.8704
B0 to CO ↓	0.0298	0.0366	4.5515	0.7864
B0 to CO ↑	0.0237	0.0279	3.4293	0.8601
B0 to S0 ↓	0.0626	0.0781	2.4423	0.6109
B0 to S0 ↑	0.0577	0.0633	3.5027	0.8709
CI to CO ↓	0.0298	0.0512	4.5444	0.7944
CI to CO ↑	0.0263	0.0315	3.5029	0.8657
CI to S0 ↓	0.0355	0.0458	2.4432	0.6113
CI to S0 ↑	0.0306	0.0305	3.5023	0.8709

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_FA1X8_P4	1.161e-04	1.000e-20
C12T28SOI_LL_FA1X33_P4	3.123e-04	1.000e-20
C12T28SOI_LLS1_FA1X8_P4	2.540e-04	1.000e-20
C12T28SOI_LLS1_FA1X33_P4	5.250e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4
A0 to CO	3.163e-03	9.414e-03	4.790e-03	1.210e-02
A0 to S0	3.159e-03	9.735e-03	6.415e-03	1.496e-02
B0 to CO	3.200e-03	9.609e-03	4.810e-03	1.223e-02
B0 to S0	3.134e-03	9.744e-03	6.489e-03	1.523e-02
CI to CO	3.254e-03	9.747e-03	3.421e-03	1.097e-02
CI to S0	3.133e-03	9.736e-03	3.868e-03	1.176e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00

A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X33_P4	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X33_P4
A0	0.0010	0.0030
B0	0.0009	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
A0 to CO ↓	0.0337	0.0301	2.2782	0.5635
A0 to CO ↑	0.0314	0.0281	3.3772	0.8616
A0 to S0 ↓	0.0442	0.0410	2.2356	0.5625
A0 to S0 ↑	0.0421	0.0464	3.3339	0.8527
B0 to CO ↓	0.0328	0.0280	2.2775	0.5594
B0 to CO ↑	0.0335	0.0293	3.3766	0.8615
B0 to S0 ↓	0.0457	0.0408	2.2342	0.5630
B0 to S0 ↑	0.0416	0.0446	3.3330	0.8531

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	7.059e-05	1.000e-20
X33_P4	3.004e-04	1.000e-20

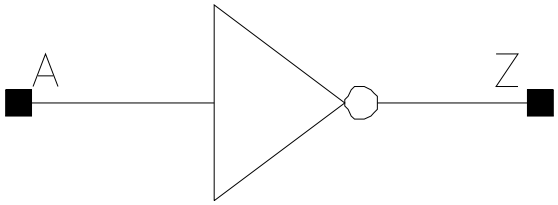
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X33_P4
A0 to CO	2.428e-03	8.100e-03
A0 to S0	2.260e-03	7.986e-03
B0 to CO	2.473e-03	8.313e-03
B0 to S0	2.236e-03	7.762e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X8_P4	X33_P4
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.272	0.3264
X6_P4	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X13_P4	1.200	0.408	0.4896
X17_P4	1.200	0.408	0.4896
X21_P4	1.200	0.544	0.6528
X25_P4	1.200	0.544	0.6528
X29_P4	1.200	0.680	0.8160
X33_P4	1.200	0.680	0.8160
X50_P4	1.200	0.952	1.1424
X58_P4	1.200	1.088	1.3056
X67_P4	1.200	1.224	1.4688
X75_P4	1.200	1.360	1.6320
X84_P4	1.200	1.496	1.7952
X100_P4	1.200	1.768	2.1216
X134_P4	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0005	0.0006	0.0008	0.0012
	X17_P4	X21_P4	X25_P4	X29_P4
A	0.0015	0.0019	0.0022	0.0026
	X33_P4	X50_P4	X58_P4	X67_P4
A	0.0029	0.0044	0.0051	0.0059
	X75_P4	X84_P4	X100_P4	X134_P4

A	0.0067	0.0075	0.0093	0.0128

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0073	0.0069	4.3272	3.3008
A to Z ↑	0.0124	0.0113	6.5819	4.9474
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0062	0.0052	2.2368	1.4577
A to Z ↑	0.0101	0.0093	3.3978	2.2470
	X17_P4	**X21_P4**	**X17_P4**	**X21_P4**
A to Z ↓	0.0052	0.0056	1.1080	0.8965
A to Z ↑	0.0087	0.0093	1.6707	1.3483
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0056	0.0053	0.7580	0.6455
A to Z ↑	0.0089	0.0086	1.1226	0.9606
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0052	0.0053	0.5707	0.3851
A to Z ↑	0.0082	0.0082	0.8408	0.5626
	X58_P4	**X67_P4**	**X58_P4**	**X67_P4**
A to Z ↓	0.0057	0.0055	0.3336	0.2932
A to Z ↑	0.0085	0.0082	0.4844	0.4245
	X75_P4	**X84_P4**	**X75_P4**	**X84_P4**
A to Z ↓	0.0060	0.0061	0.2639	0.2385
A to Z ↑	0.0088	0.0087	0.3805	0.3440
	X100_P4	**X134_P4**	**X100_P4**	**X134_P4**
A to Z ↓	0.0068	0.0074	0.2026	0.1570
A to Z ↑	0.0093	0.0100	0.2892	0.2220

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	9.901e-06	1.000e-20
X6_P4	1.408e-05	1.000e-20
X8_P4	2.254e-05	1.000e-20
X13_P4	3.204e-05	1.000e-20
X17_P4	4.571e-05	1.000e-20
X21_P4	5.355e-05	1.000e-20
X25_P4	6.597e-05	1.000e-20
X29_P4	7.487e-05	1.000e-20
X33_P4	8.592e-05	1.000e-20
X50_P4	1.258e-04	1.000e-20
X58_P4	1.457e-04	1.000e-20
X67_P4	1.657e-04	1.000e-20
X75_P4	1.856e-04	1.000e-20
X84_P4	2.055e-04	1.000e-20
X100_P4	2.454e-04	1.000e-20
X134_P4	3.252e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4

A to Z	4.529e-04	5.643e-04	7.579e-04	1.062e-03
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	1.382e-03	1.822e-03	2.128e-03	2.377e-03
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	2.637e-03	3.936e-03	4.735e-03	5.197e-03
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	6.061e-03	6.603e-03	8.072e-03	1.104e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

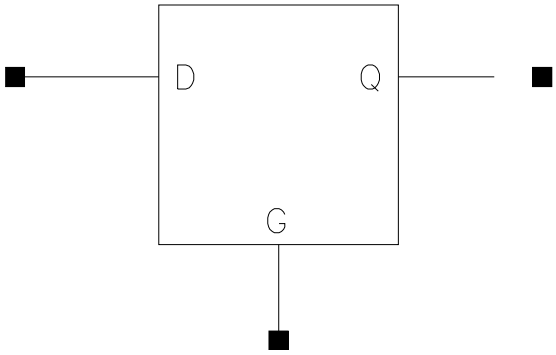
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X23_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P4	X23_P4
D	0.0005	0.0012
G	0.0011	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X23_P4	X8_P4	X23_P4
D to Q ↓	0.0502	0.0384	2.2896	1.1102
D to Q ↑	0.0334	0.0326	3.3206	0.8797
G to Q ↓	0.0534	0.0413	2.2834	1.1094
G to Q ↑	0.0323	0.0287	3.3173	0.8794

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P4	X23_P4
D ↓	hold_falling to G	-0.0067	0.0004
D ↑	hold_falling to G	0.0019	0.0019
D ↓	setup_falling to G	0.0489	0.0312
D ↑	setup_falling to G	0.0350	0.0402
G ↑	min_pulse_width to G	0.0458	0.0443

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	5.175e-05	1.000e-20
X23_P4	1.265e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X23_P4
D (output stable)	1.165e-05	5.117e-05
G (output stable)	8.244e-04	1.645e-03
D to Q	3.973e-03	7.589e-03
G to Q	3.764e-03	6.921e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

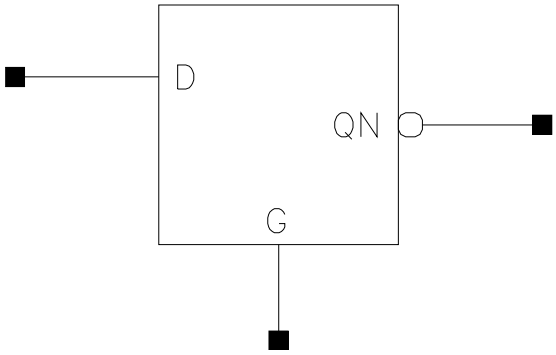
Pin Cycle (vdds)	X8_P4	X23_P4
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P4
D	0.0006
G	0.0013

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P4	X17_P4
D to QN ↓	0.0440	1.0890
D to QN ↑	0.0557	1.6312
G to QN ↓	0.0424	1.0890
G to QN ↑	0.0570	1.6288

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P4
D ↓	hold_falling to G	-0.0116
D ↑	hold_falling to G	-0.0030
D ↓	setup_falling to G	0.0386
D ↑	setup_falling to G	0.0306
G ↑	min_pulse_width to G	0.0364

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P4	8.401e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X17_P4
D (output stable)	1.182e-05
G (output stable)	9.708e-04
D to QN	4.818e-03
G to QN	4.572e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

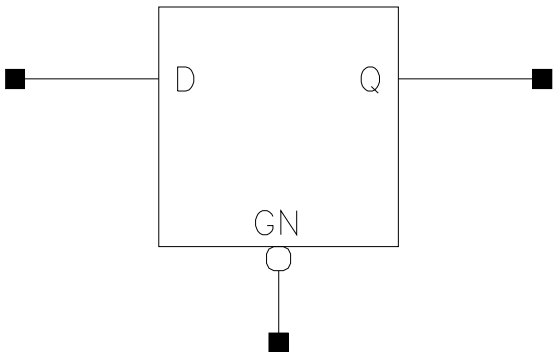
Pin Cycle (vdds)	X17_P4
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
D	0.0005	0.0007	0.0016
GN	0.0011	0.0014	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D to Q ↓	0.0508	0.0430	2.2949	1.1335
D to Q ↑	0.0339	0.0317	3.3234	1.7007
GN to Q ↓	0.0460	0.0381	2.2956	1.1350
GN to Q ↑	0.0500	0.0476	3.3174	1.6983

	X33_P4		X33_P4	
D to Q ↓	0.0417		0.5791	
D to Q ↑	0.0270		0.8517	
GN to Q ↓	0.0360		0.5801	
GN to Q ↑	0.0363		0.8503	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P4	X17_P4	X33_P4
D ↓	hold_rising to GN	-0.0117	-0.0042	-0.0046
D ↑	hold_rising to GN	0.0032	0.0058	0.0106
D ↓	setup_rising to GN	0.0569	0.0504	0.0445
D ↑	setup_rising to GN	0.0314	0.0293	0.0239
GN ↓	min_pulse_width to GN	0.0599	0.0513	0.0484

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	5.085e-05	1.000e-20
X17_P4	8.462e-05	1.000e-20
X33_P4	1.483e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
D (output stable)	1.163e-05	1.939e-05	5.479e-05
GN (output stable)	8.213e-04	1.137e-03	1.457e-03
D to Q	3.996e-03	5.682e-03	9.220e-03
GN to Q	5.550e-03	7.634e-03	1.137e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

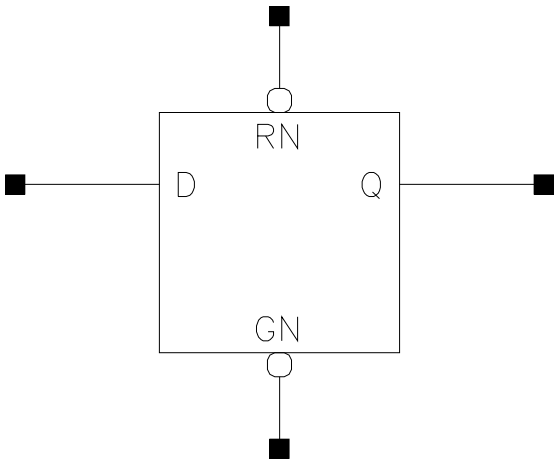
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.496	1.7952
X33_P4	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X33_P4
D	0.0005	0.0013
GN	0.0012	0.0023
RN	0.0005	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
D to Q ↓	0.0472	0.0418	2.2462	0.5820
D to Q ↑	0.0440	0.0565	3.3834	0.8771

GN to Q ↓	0.0431	0.0386	2.2468	0.5829
GN to Q ↑	0.0574	0.0595	3.3811	0.8777
RN to Q ↓	0.0386	0.0724	2.1818	0.6223
RN to Q ↑	0.0465	0.0621	3.3826	0.8773

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P4	X33_P4
D ↓	hold_rising to GN	-0.0101	-0.0052
D ↑	hold_rising to GN	-0.0045	-0.0191
D ↓	setup_rising to GN	0.0494	0.0446
D ↑	setup_rising to GN	0.0411	0.0637
GN ↓	min_pulse_width to GN	0.0556	0.0623
RN ↓	min_pulse_width to RN	0.0447	0.0833
RN ↑	recovery_rising to GN	0.0433	0.0676
RN ↑	removal_rising to GN	-0.0298	-0.0430

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	5.592e-05	1.000e-20
X33_P4	1.476e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X33_P4
D (output stable)	3.888e-05	6.655e-05
GN (output stable)	9.161e-04	1.449e-03
RN (output stable)	3.700e-05	7.311e-05
D to Q	4.008e-03	1.093e-02
GN to Q	5.690e-03	1.352e-02
RN to Q	2.984e-03	8.866e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

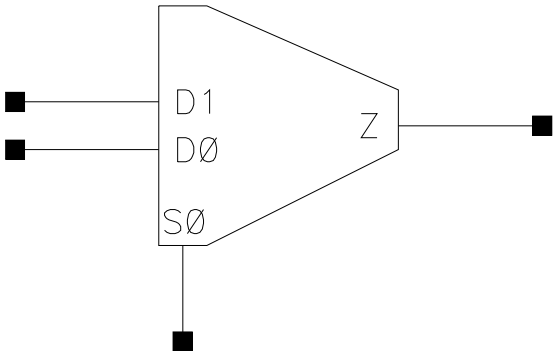
Pin Cycle (vdds)	X8_P4	X33_P4
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
D0	0.0007	0.0010	0.0013	0.0018
D1	0.0007	0.0010	0.0013	0.0018
S0	0.0013	0.0014	0.0016	0.0024

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D0 to Z ↓	0.0390	0.0341	2.2668	1.1096
D0 to Z ↑	0.0315	0.0285	3.3993	1.6607
D1 to Z ↓	0.0367	0.0334	2.2607	1.1084
D1 to Z ↑	0.0286	0.0267	3.3962	1.6566
S0 to Z ↓	0.0334	0.0319	2.2562	1.1058
S0 to Z ↑	0.0319	0.0316	3.3945	1.6574

	X25_P4	X33_P4	X25_P4	X33_P4
D0 to Z ↓	0.0368	0.0327	0.7612	0.5712
D0 to Z ↑	0.0305	0.0280	1.1148	0.8344
D1 to Z ↓	0.0390	0.0338	0.7634	0.5718
D1 to Z ↑	0.0294	0.0271	1.1151	0.8353
S0 to Z ↓	0.0366	0.0333	0.7603	0.5705
S0 to Z ↑	0.0352	0.0319	1.1147	0.8348

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	6.047e-05	1.000e-20
X17_P4	1.177e-04	1.000e-20
X25_P4	1.530e-04	1.000e-20
X33_P4	2.315e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	7.697e-04	1.191e-03	1.324e-03	1.875e-03
D1 (output stable)	6.459e-04	1.124e-03	1.450e-03	1.946e-03
S0 (output stable)	9.681e-04	1.090e-03	1.399e-03	1.763e-03
D0 to Z	2.690e-03	4.473e-03	6.955e-03	8.721e-03
D1 to Z	2.473e-03	4.330e-03	7.018e-03	8.648e-03
S0 to Z	3.076e-03	4.741e-03	7.739e-03	9.460e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

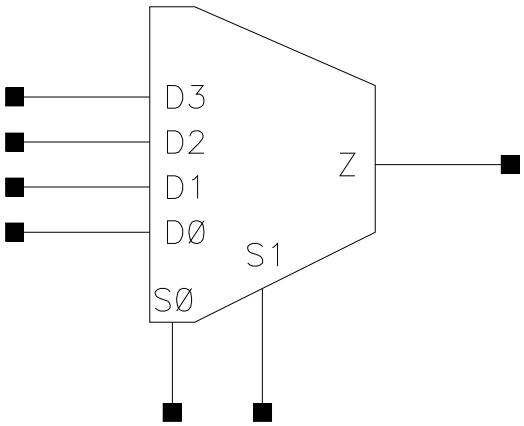
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.312	2.7744
X31_P4	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P4	X31_P4
D0	0.0005	0.0014
D1	0.0005	0.0013
D2	0.0005	0.0014
D3	0.0005	0.0013
S0	0.0018	0.0035
S1	0.0011	0.0023

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X31_P4	X8_P4	X31_P4

D0 to Z ↓	0.0662	0.0665	2.3657	0.6520
D0 to Z ↑	0.0454	0.0471	3.4348	0.9200
D1 to Z ↓	0.0656	0.0666	2.3629	0.6523
D1 to Z ↑	0.0457	0.0470	3.4347	0.9205
D2 to Z ↓	0.0712	0.0623	2.3794	0.6461
D2 to Z ↑	0.0483	0.0436	3.4463	0.9147
D3 to Z ↓	0.0710	0.0618	2.3793	0.6452
D3 to Z ↑	0.0478	0.0446	3.4429	0.9174
S0 to Z ↓	0.0733	0.0727	2.3704	0.6486
S0 to Z ↑	0.0561	0.0579	3.4409	0.9191
S1 to Z ↓	0.0533	0.0512	2.3739	0.6488
S1 to Z ↑	0.0439	0.0448	3.4398	0.9181

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	5.862e-05	1.000e-20
X31_P4	1.895e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X31_P4
D0 (output stable)	1.846e-05	1.008e-04
D1 (output stable)	1.815e-05	9.206e-05
D2 (output stable)	2.091e-05	9.580e-05
D3 (output stable)	2.098e-05	9.538e-05
S0 (output stable)	1.358e-03	3.044e-03
S1 (output stable)	1.153e-03	2.547e-03
D0 to Z	3.025e-03	1.052e-02
D1 to Z	3.015e-03	1.058e-02
D2 to Z	3.248e-03	9.831e-03
D3 to Z	3.238e-03	9.839e-03
S0 to Z	4.539e-03	1.358e-02
S1 to Z	3.697e-03	1.101e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

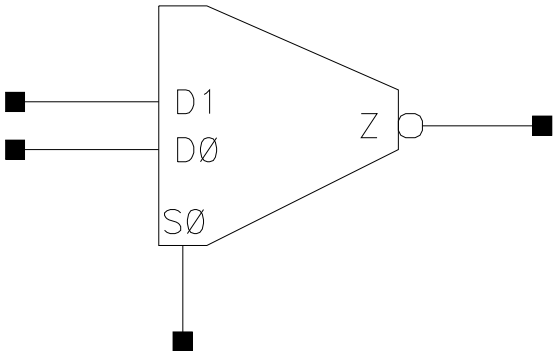
Pin Cycle (vdds)	X8_P4	X31_P4
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.816	0.9792
X5_P4	1.200	0.952	1.1424
X10_P4	1.200	1.768	2.1216
X16_P4	1.200	2.448	2.9376
X21_P4	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P4	X5_P4	X10_P4	X16_P4
D0	0.0005	0.0008	0.0016	0.0024
D1	0.0005	0.0008	0.0015	0.0023
S0	0.0011	0.0019	0.0025	0.0037
	X21_P4			
D0	0.0031			
D1	0.0031			
S0	0.0043			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X5_P4	X3_P4	X5_P4
D0 to Z ↓	0.0133	0.0134	7.4617	4.4666

D0 to Z ↑	0.0223	0.0196	13.8410	6.9741
D1 to Z ↓	0.0132	0.0129	7.4002	4.2897
D1 to Z ↑	0.0231	0.0204	13.8652	7.1983
S0 to Z ↓	0.0207	0.0171	7.4047	4.3681
S0 to Z ↑	0.0224	0.0184	13.8185	7.0705
	X10_P4	**X16_P4**	**X10_P4**	**X16_P4**
D0 to Z ↓	0.0151	0.0140	2.0939	1.3687
D0 to Z ↑	0.0214	0.0202	3.2329	2.1264
D1 to Z ↓	0.0137	0.0134	2.0386	1.3457
D1 to Z ↑	0.0213	0.0205	3.2771	2.1458
S0 to Z ↓	0.0208	0.0178	2.0586	1.3531
S0 to Z ↑	0.0219	0.0187	3.2472	2.1327
	X21_P4		**X21_P4**	
D0 to Z ↓	0.0139		1.0421	
D0 to Z ↑	0.0198		1.6089	
D1 to Z ↓	0.0134		1.0201	
D1 to Z ↑	0.0206		1.6025	
S0 to Z ↓	0.0187		1.0271	
S0 to Z ↑	0.0192		1.6022	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	2.098e-05	1.000e-20
X5_P4	5.127e-05	1.000e-20
X10_P4	9.184e-05	1.000e-20
X16_P4	1.462e-04	1.000e-20
X21_P4	1.793e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	1.155e-05	2.738e-05	8.198e-05	1.273e-04
D1 (output stable)	1.144e-05	2.863e-05	6.860e-05	1.203e-04
S0 (output stable)	8.271e-04	1.268e-03	2.067e-03	3.319e-03
D0 to Z	7.602e-04	1.294e-03	3.211e-03	4.504e-03
D1 to Z	7.618e-04	1.283e-03	3.047e-03	4.433e-03
S0 to Z	1.432e-03	2.213e-03	4.425e-03	6.406e-03
	X21_P4			
D0 (output stable)	1.645e-04			
D1 (output stable)	1.632e-04			
S0 (output stable)	3.648e-03			
D0 to Z	5.811e-03			
D1 to Z	5.878e-03			
S0 to Z	7.784e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

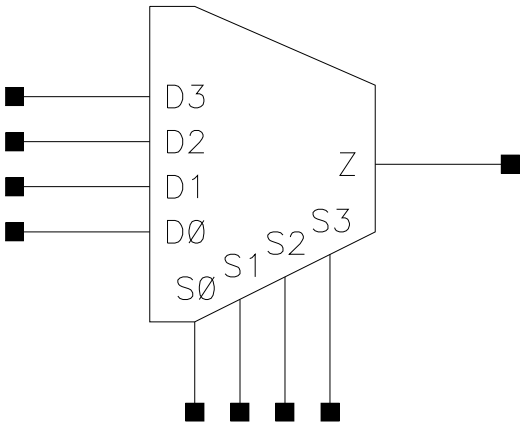
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P4			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	1.768	2.1216
X27_P4	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P4	X27_P4
D0	0.0006	0.0019
D1	0.0006	0.0019
D2	0.0006	0.0019
D3	0.0006	0.0019
S0	0.0006	0.0017
S1	0.0007	0.0018
S2	0.0006	0.0018
S3	0.0007	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	X27_P4	X7_P4	X27_P4
D0 to Z ↓	0.0513	0.0416	3.7620	1.0207
D0 to Z ↑	0.0380	0.0315	3.3458	0.8328
D1 to Z ↓	0.0469	0.0383	3.7599	1.0200
D1 to Z ↑	0.0341	0.0275	3.3313	0.8287
D2 to Z ↓	0.0522	0.0401	3.7677	1.0204
D2 to Z ↑	0.0374	0.0297	3.3567	0.8358
D3 to Z ↓	0.0479	0.0368	3.7615	1.0192
D3 to Z ↑	0.0335	0.0257	3.3451	0.8313
S0 to Z ↓	0.0498	0.0393	3.7609	1.0205
S0 to Z ↑	0.0403	0.0330	3.3447	0.8328
S1 to Z ↓	0.0457	0.0359	3.7578	1.0197
S1 to Z ↑	0.0363	0.0286	3.3304	0.8287
S2 to Z ↓	0.0507	0.0377	3.7646	1.0197
S2 to Z ↑	0.0397	0.0311	3.3576	0.8356
S3 to Z ↓	0.0467	0.0344	3.7621	1.0186
S3 to Z ↑	0.0357	0.0269	3.3431	0.8312

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X7_P4	5.502e-05	1.000e-20
X27_P4	2.345e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X7_P4	X27_P4
D0 (output stable)	4.029e-04	1.265e-03
D1 (output stable)	3.556e-04	1.072e-03
D2 (output stable)	3.775e-04	1.178e-03
D3 (output stable)	3.295e-04	9.859e-04
S0 (output stable)	3.940e-04	1.206e-03
S1 (output stable)	3.455e-04	1.023e-03
S2 (output stable)	3.686e-04	1.119e-03
S3 (output stable)	3.195e-04	9.402e-04
D0 to Z	3.290e-03	1.008e-02
D1 to Z	2.927e-03	8.807e-03
D2 to Z	3.228e-03	9.042e-03
D3 to Z	2.869e-03	7.786e-03
S0 to Z	3.219e-03	9.629e-03
S1 to Z	2.858e-03	8.397e-03
S2 to Z	3.156e-03	8.575e-03
S3 to Z	2.800e-03	7.378e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

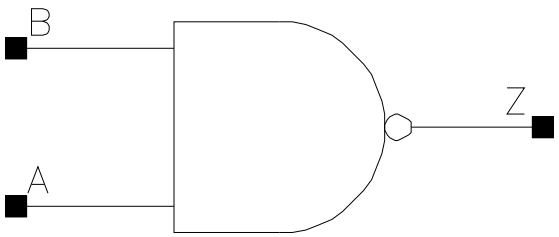
Pin Cycle (vdds)	X7_P4	X27_P4
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P4	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P4	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P4	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P4	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P4	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P4	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P4	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P4	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P4	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P4	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P4	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P4	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P4	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P4	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P4	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P4	C12T28SOI_LL_-NAND2X5_P4	C12T28SOI_LL_-NAND2X7_P4	C12T28SOI_LL_-NAND2X10_P4
A	0.0005	0.0007	0.0008	0.0012
B	0.0005	0.0007	0.0008	0.0011
	C12T28SOI_LL_-NAND2X13_P4	C12T28SOI_LL_-NAND2X17_P4	C12T28SOI_LL_-NAND2X20_P4	C12T28SOI_LL_-NAND2X24_P4
A	0.0015	0.0020	0.0023	0.0027
B	0.0014	0.0018	0.0021	0.0025
	C12T28SOI_LL_-NAND2X27_P4	C12T28SOI_LL_-NAND2X42_P4	C12T28SOI_LL_-NAND2X47_P4	C12T28SOI_LL_-NAND2X50_P4
A	0.0030	0.0010	0.0010	0.0010
B	0.0028	0.0010	0.0010	0.0010
	C12T28SOI_LL_-NAND2X58_P4	C12T28SOI_LL_-NAND2X67_P4	C12T28SOI_-LLBR0D8_-NAND2X7_P4	C12T28SOI_-LLBR0D8_-NAND2X14_P4
A	0.0010	0.0010	0.0007	0.0015
B	0.0010	0.0010	0.0008	0.0014
	C12T28SOI_LLS_-NAND2X40_P4	C12T28SOI_LLS_-NAND2X54_P4		
A	0.0045	0.0060		
B	0.0042	0.0056		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P4	**C12T28SOI_LL_-NAND2X5_P4**	**C12T28SOI_LL_-NAND2X3_P4**	**C12T28SOI_LL_-NAND2X5_P4**
A to Z ↓	0.0101	0.0092	7.2658	4.6291
A to Z ↑	0.0147	0.0131	6.5975	4.1934
B to Z ↓	0.0112	0.0099	7.3229	4.6656
B to Z ↑	0.0134	0.0115	6.6318	4.2140
	C12T28SOI_LL_-NAND2X7_P4	**C12T28SOI_LL_-NAND2X10_P4**	**C12T28SOI_LL_-NAND2X7_P4**	**C12T28SOI_LL_-NAND2X10_P4**
A to Z ↓	0.0091	0.0104	3.8681	2.5690
A to Z ↑	0.0126	0.0137	3.3847	2.2293
B to Z ↓	0.0099	0.0097	3.8942	2.5883
B to Z ↑	0.0110	0.0109	3.4140	2.2430
	C12T28SOI_LL_-NAND2X13_P4	**C12T28SOI_LL_-NAND2X17_P4**	**C12T28SOI_LL_-NAND2X13_P4**	**C12T28SOI_LL_-NAND2X17_P4**
A to Z ↓	0.0100	0.0098	1.9663	1.5695

A to Z ↑	0.0128	0.0129	1.6624	1.3438
B to Z ↓	0.0094	0.0098	1.9815	1.5816
B to Z ↑	0.0101	0.0107	1.6726	1.3510
	C12T28SOI_LL_-NAND2X20_P4	**C12T28SOI_LL_-NAND2X24_P4**	**C12T28SOI_LL_-NAND2X20_P4**	**C12T28SOI_LL_-NAND2X24_P4**
A to Z ↓	0.0097	0.0100	1.3407	1.1418
A to Z ↑	0.0124	0.0127	1.1182	0.9578
B to Z ↓	0.0098	0.0095	1.3507	1.1510
B to Z ↑	0.0103	0.0101	1.1259	0.9631
	C12T28SOI_LL_-NAND2X27_P4	**C12T28SOI_LL_-NAND2X42_P4**	**C12T28SOI_LL_-NAND2X27_P4**	**C12T28SOI_LL_-NAND2X42_P4**
A to Z ↓	0.0097	0.0364	1.0164	0.4543
A to Z ↑	0.0122	0.0366	0.8392	0.6610
B to Z ↓	0.0093	0.0377	1.0250	0.4541
B to Z ↑	0.0097	0.0353	0.8442	0.6607
	C12T28SOI_LL_-NAND2X47_P4	**C12T28SOI_LL_-NAND2X50_P4**	**C12T28SOI_LL_-NAND2X47_P4**	**C12T28SOI_LL_-NAND2X50_P4**
A to Z ↓	0.0375	0.0378	0.4046	0.3792
A to Z ↑	0.0373	0.0375	0.5748	0.5517
B to Z ↓	0.0388	0.0390	0.4047	0.3792
B to Z ↑	0.0359	0.0361	0.5760	0.5523
	C12T28SOI_LL_-NAND2X58_P4	**C12T28SOI_LL_-NAND2X67_P4**	**C12T28SOI_LL_-NAND2X58_P4**	**C12T28SOI_LL_-NAND2X67_P4**
A to Z ↓	0.0396	0.0410	0.3282	0.2887
A to Z ↑	0.0389	0.0399	0.4744	0.4168
B to Z ↓	0.0409	0.0423	0.3284	0.2886
B to Z ↑	0.0375	0.0385	0.4748	0.4167
	C12T28SOI_-LLBR0D8_-NAND2X7_P4	**C12T28SOI_-LLBR0D8_-NAND2X14_P4**	**C12T28SOI_-LLBR0D8_-NAND2X7_P4**	**C12T28SOI_-LLBR0D8_-NAND2X14_P4**
A to Z ↓	0.0070	0.0080	2.9072	1.5153
A to Z ↑	0.0158	0.0160	4.4995	2.1980
B to Z ↓	0.0071	0.0065	2.9376	1.5351
B to Z ↑	0.0134	0.0120	4.6280	2.2336
	C12T28SOI_LLS_-NAND2X40_P4	**C12T28SOI_LLS_-NAND2X54_P4**	**C12T28SOI_LLS_-NAND2X40_P4**	**C12T28SOI_LLS_-NAND2X54_P4**
A to Z ↓	0.0097	0.0098	0.6880	0.5201
A to Z ↑	0.0122	0.0122	0.5620	0.4232
B to Z ↓	0.0093	0.0096	0.6934	0.5242
B to Z ↑	0.0096	0.0097	0.5657	0.4265

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P4	9.983e-06	1.000e-20
C12T28SOI_LL_NAND2X5_P4	1.822e-05	1.000e-20
C12T28SOI_LL_NAND2X7_P4	2.318e-05	1.000e-20
C12T28SOI_LL_NAND2X10_P4	3.167e-05	1.000e-20
C12T28SOI_LL_NAND2X13_P4	4.535e-05	1.000e-20
C12T28SOI_LL_NAND2X17_P4	5.353e-05	1.000e-20
C12T28SOI_LL_NAND2X20_P4	6.598e-05	1.000e-20
C12T28SOI_LL_NAND2X24_P4	7.538e-05	1.000e-20
C12T28SOI_LL_NAND2X27_P4	8.665e-05	1.000e-20

C12T28SOI_LL_NAND2X42_P4	1.593e-04	1.000e-20
C12T28SOI_LL_NAND2X47_P4	1.735e-04	1.000e-20
C12T28SOI_LL_NAND2X50_P4	1.760e-04	1.000e-20
C12T28SOI_LL_NAND2X58_P4	1.927e-04	1.000e-20
C12T28SOI_LL_NAND2X67_P4	2.094e-04	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_P4	2.194e-05	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_-P4	4.200e-05	1.000e-20
C12T28SOI_LLS_NAND2X40_P4	1.280e-04	1.000e-20
C12T28SOI_LLS_NAND2X54_P4	1.694e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND2X3_P4	C12T28SOI_LL_-NAND2X5_P4	C12T28SOI_LL_-NAND2X7_P4	C12T28SOI_LL_-NAND2X10_P4
A (output stable)	9.187e-06	1.451e-05	1.744e-05	6.009e-05
B (output stable)	1.689e-05	2.636e-05	3.237e-05	1.722e-04
A to Z	5.799e-04	8.109e-04	9.741e-04	1.645e-03
B to Z	5.087e-04	6.951e-04	8.328e-04	1.248e-03
	C12T28SOI_LL_-NAND2X13_P4	C12T28SOI_LL_-NAND2X17_P4	C12T28SOI_LL_-NAND2X20_P4	C12T28SOI_LL_-NAND2X24_P4
A (output stable)	7.134e-05	8.416e-05	9.215e-05	1.287e-04
B (output stable)	1.998e-04	1.872e-04	2.074e-04	3.170e-04
A to Z	2.058e-03	2.549e-03	2.948e-03	3.558e-03
B to Z	1.580e-03	2.049e-03	2.382e-03	2.751e-03
	C12T28SOI_LL_-NAND2X27_P4	C12T28SOI_LL_-NAND2X42_P4	C12T28SOI_LL_-NAND2X47_P4	C12T28SOI_LL_-NAND2X50_P4
A (output stable)	1.379e-04	1.920e-05	2.002e-05	1.964e-05
B (output stable)	3.442e-04	3.500e-05	3.540e-05	3.508e-05
A to Z	3.886e-03	9.127e-03	9.926e-03	1.022e-02
B to Z	3.010e-03	8.988e-03	9.788e-03	1.008e-02
	C12T28SOI_LL_-NAND2X58_P4	C12T28SOI_LL_-NAND2X67_P4	C12T28SOI_-LLBR0D8_-NAND2X7_P4	C12T28SOI_-LLBR0D8_-NAND2X14_P4
A (output stable)	1.972e-05	1.980e-05	2.297e-05	8.931e-05
B (output stable)	3.510e-05	3.520e-05	4.274e-05	2.479e-04
A to Z	1.173e-02	1.294e-02	9.869e-04	2.092e-03
B to Z	1.159e-02	1.280e-02	7.841e-04	1.444e-03
	C12T28SOI_LLS_-NAND2X40_P4	C12T28SOI_LLS_-NAND2X54_P4		
A (output stable)	2.023e-04	2.631e-04		
B (output stable)	4.809e-04	5.975e-04		
A to Z	5.752e-03	7.652e-03		
B to Z	4.478e-03	5.989e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND2X3_P4	C12T28SOI_LL_-NAND2X5_P4	C12T28SOI_LL_-NAND2X7_P4	C12T28SOI_LL_-NAND2X10_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

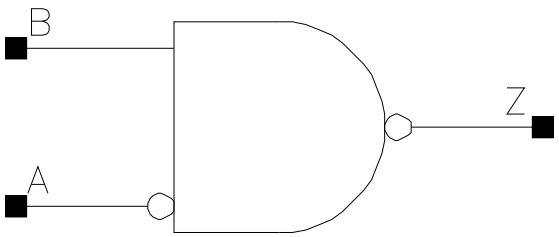
	C12T28SOI_LL_-NAND2X13_P4	C12T28SOI_LL_-NAND2X17_P4	C12T28SOI_LL_-NAND2X20_P4	C12T28SOI_LL_-NAND2X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P4	C12T28SOI_LL_-NAND2X42_P4	C12T28SOI_LL_-NAND2X47_P4	C12T28SOI_LL_-NAND2X50_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P4	C12T28SOI_LL_-NAND2X67_P4	C12T28SOI_-LLBR0D8_-NAND2X7_P4	C12T28SOI_-LLBR0D8_-NAND2X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P4	C12T28SOI_LLS_-NAND2X54_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X7_P4	1.200	0.544	0.6528
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X40_P4	1.200	2.312	2.7744
X54_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P4	X7_P4	X13_P4	X27_P4
A	0.0008	0.0008	0.0010	0.0019
B	0.0005	0.0008	0.0014	0.0028
	X40_P4	X54_P4		
A	0.0028	0.0037		
B	0.0041	0.0055		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0270	0.0286	7.2497	3.8599
A to Z ↑	0.0214	0.0221	6.4360	3.3456
B to Z ↓	0.0116	0.0099	7.3955	3.9244
B to Z ↑	0.0135	0.0109	6.6336	3.4383
	X13_P4	**X27_P4**	**X13_P4**	**X27_P4**

A to Z ↓	0.0260	0.0253	2.0427	1.0140
A to Z ↑	0.0209	0.0205	1.7105	0.8294
B to Z ↓	0.0092	0.0092	2.0818	1.0344
B to Z ↑	0.0100	0.0097	1.7139	0.8452
	X40_P4	**X54_P4**	**X40_P4**	**X54_P4**
A to Z ↓	0.0254	0.0253	0.6784	0.5140
A to Z ↑	0.0207	0.0205	0.5522	0.4162
B to Z ↓	0.0092	0.0092	0.6915	0.5239
B to Z ↑	0.0096	0.0095	0.5676	0.4282

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.875e-05	1.000e-20
X7_P4	3.180e-05	1.000e-20
X13_P4	6.838e-05	1.000e-20
X27_P4	1.315e-04	1.000e-20
X40_P4	1.929e-04	1.000e-20
X54_P4	2.542e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	8.664e-04	1.068e-03	1.764e-03	3.472e-03
B (output stable)	1.728e-05	3.241e-05	1.821e-04	3.095e-04
A to Z	1.455e-03	2.012e-03	3.697e-03	7.288e-03
B to Z	5.138e-04	8.252e-04	1.549e-03	3.053e-03
	X40_P4	X54_P4		
A (output stable)	5.241e-03	6.839e-03		
B (output stable)	4.556e-04	5.859e-04		
A to Z	1.082e-02	1.421e-02		
B to Z	4.467e-03	5.912e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

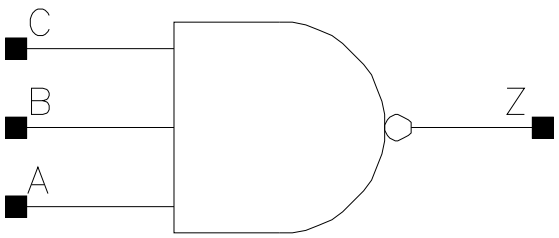
Pin Cycle (vdds)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P4	X54_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P4	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P4	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P4	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P4	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P4	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P4	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P4	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P4	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P4	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P4	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P4	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P4	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P4	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P4	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P4	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A	0.0006	0.0008	0.0012	0.0015
B	0.0007	0.0008	0.0012	0.0015
C	0.0006	0.0007	0.0011	0.0014
	C12T28SOI_LL_-NAND3X15_P4	C12T28SOI_LL_-NAND3X18_P4	C12T28SOI_LL_-NAND3X21_P4	C12T28SOI_LL_-NAND3X24_P4
A	0.0020	0.0022	0.0027	0.0030
B	0.0019	0.0022	0.0026	0.0029
C	0.0018	0.0020	0.0025	0.0028
	C12T28SOI_LL_-NAND3X35_P4	C12T28SOI_LL_-NAND3X47_P4	C12T28SOI_-LLBR0P6_-NAND3X6_P4	C12T28SOI_-LLBR0P6_-NAND3X12_P4
A	0.0046	0.0061	0.0008	0.0015
B	0.0044	0.0058	0.0008	0.0014
C	0.0041	0.0055	0.0007	0.0014
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	C12T28SOI_-LLBR0P6_-NAND3X24_P4	C12T28SOI_-LLBR0P6_-NAND3X35_P4	C12T28SOI_-LLBR0P6_-NAND3X47_P4
A	0.0023	0.0030	0.0045	0.0060
B	0.0021	0.0029	0.0042	0.0056
C	0.0020	0.0027	0.0040	0.0053
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4			
A	0.0024			
B	0.0023			
C	0.0021			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4
A to Z ↓	0.0167	0.0151	7.5602	5.3717
A to Z ↑	0.0186	0.0165	4.7857	3.2848
B to Z ↓	0.0179	0.0160	7.5808	5.3866
B to Z ↑	0.0178	0.0156	4.7952	3.2900
C to Z ↓	0.0162	0.0146	7.5946	5.3989
C to Z ↑	0.0154	0.0134	4.7953	3.3063

	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A to Z ↓	0.0165	0.0155	3.6636	2.8252
A to Z ↑	0.0174	0.0161	2.2401	1.6764
B to Z ↓	0.0159	0.0150	3.6743	2.8343
B to Z ↑	0.0158	0.0147	2.2422	1.6775
C to Z ↓	0.0145	0.0138	3.6831	2.8411
C to Z ↑	0.0134	0.0123	2.2346	1.6681
	C12T28SOI_LL_-NAND3X15_P4	**C12T28SOI_LL_-NAND3X18_P4**	**C12T28SOI_LL_-NAND3X15_P4**	**C12T28SOI_LL_-NAND3X18_P4**
A to Z ↓	0.0148	0.0143	2.2903	1.9498
A to Z ↑	0.0158	0.0152	1.3418	1.1161
B to Z ↓	0.0148	0.0145	2.2969	1.9558
B to Z ↑	0.0142	0.0137	1.3448	1.1180
C to Z ↓	0.0139	0.0136	2.3037	1.9605
C to Z ↑	0.0122	0.0116	1.3521	1.1238
	C12T28SOI_LL_-NAND3X21_P4	**C12T28SOI_LL_-NAND3X24_P4**	**C12T28SOI_LL_-NAND3X21_P4**	**C12T28SOI_LL_-NAND3X24_P4**
A to Z ↓	0.0152	0.0150	1.6489	1.4702
A to Z ↑	0.0159	0.0154	0.9621	0.8435
B to Z ↓	0.0149	0.0147	1.6543	1.4750
B to Z ↑	0.0144	0.0140	0.9627	0.8440
C to Z ↓	0.0139	0.0137	1.6580	1.4788
C to Z ↑	0.0122	0.0118	0.9632	0.8445
	C12T28SOI_LL_-NAND3X35_P4	**C12T28SOI_LL_-NAND3X47_P4**	**C12T28SOI_LL_-NAND3X35_P4**	**C12T28SOI_LL_-NAND3X47_P4**
A to Z ↓	0.0145	0.0146	1.0011	0.7605
A to Z ↑	0.0151	0.0152	0.5647	0.4266
B to Z ↓	0.0145	0.0145	1.0043	0.7629
B to Z ↑	0.0136	0.0136	0.5649	0.4252
C to Z ↓	0.0136	0.0137	1.0070	0.7650
C to Z ↑	0.0113	0.0113	0.5673	0.4269
	C12T28SOI_-LLBR0P6_-NAND3X6_P4	**C12T28SOI_-LLBR0P6_-NAND3X12_P4**	**C12T28SOI_-LLBR0P6_-NAND3X6_P4**	**C12T28SOI_-LLBR0P6_-NAND3X12_P4**
A to Z ↓	0.0114	0.0119	3.6107	1.9026
A to Z ↑	0.0239	0.0235	5.1842	2.6439
B to Z ↓	0.0116	0.0107	3.6349	1.9159
B to Z ↑	0.0218	0.0203	5.1977	2.6477
C to Z ↓	0.0093	0.0082	3.6610	1.9312
C to Z ↑	0.0173	0.0156	5.2201	2.6534
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	**C12T28SOI_-LLBR0P6_-NAND3X24_P4**	**C12T28SOI_-LLBR0P6_-NAND3X18_P4**	**C12T28SOI_-LLBR0P6_-NAND3X24_P4**
A to Z ↓	0.0109	0.0115	1.3161	0.9932
A to Z ↑	0.0221	0.0226	1.7606	1.3284
B to Z ↓	0.0103	0.0104	1.3260	1.0004
B to Z ↑	0.0190	0.0195	1.7644	1.3308
C to Z ↓	0.0083	0.0082	1.3352	1.0084
C to Z ↑	0.0149	0.0149	1.7748	1.3325
	C12T28SOI_-LLBR0P6_-NAND3X35_P4	**C12T28SOI_-LLBR0P6_-NAND3X47_P4**	**C12T28SOI_-LLBR0P6_-NAND3X35_P4**	**C12T28SOI_-LLBR0P6_-NAND3X47_P4**

A to Z ↓	0.0110	0.0112	0.6785	0.5172
A to Z ↑	0.0224	0.0225	0.9084	0.6859
B to Z ↓	0.0102	0.0104	0.6836	0.5212
B to Z ↑	0.0192	0.0193	0.9091	0.6859
C to Z ↓	0.0081	0.0085	0.6893	0.5252
C to Z ↑	0.0146	0.0149	0.9159	0.6877
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P4**	
A to Z ↓	0.0120		1.2683	
A to Z ↑	0.0224		1.6532	
B to Z ↓	0.0106		1.2772	
B to Z ↑	0.0193		1.6565	
C to Z ↓	0.0082		1.2871	
C to Z ↑	0.0145		1.6463	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P4	1.248e-05	1.000e-20
C12T28SOI_LL_NAND3X6_P4	1.991e-05	1.000e-20
C12T28SOI_LL_NAND3X9_P4	2.593e-05	1.000e-20
C12T28SOI_LL_NAND3X12_P4	3.683e-05	1.000e-20
C12T28SOI_LL_NAND3X15_P4	4.211e-05	1.000e-20
C12T28SOI_LL_NAND3X18_P4	5.175e-05	1.000e-20
C12T28SOI_LL_NAND3X21_P4	6.082e-05	1.000e-20
C12T28SOI_LL_NAND3X24_P4	6.971e-05	1.000e-20
C12T28SOI_LL_NAND3X35_P4	1.026e-04	1.000e-20
C12T28SOI_LL_NAND3X47_P4	1.354e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_P4	1.923e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P4	3.466e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P4	4.704e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P4	6.401e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P4	9.331e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P4	1.225e-04	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P4	5.975e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A (output stable)	2.010e-05	2.701e-05	6.614e-05	7.738e-05
B (output stable)	3.015e-05	3.780e-05	8.724e-05	1.009e-04
C (output stable)	1.284e-04	1.490e-04	2.290e-04	2.606e-04
A to Z	1.236e-03	1.548e-03	2.459e-03	2.955e-03
B to Z	1.130e-03	1.393e-03	2.053e-03	2.484e-03
C to Z	9.274e-04	1.154e-03	1.666e-03	2.025e-03

	C12T28SOI_LL_-NAND3X15_P4	C12T28SOI_LL_-NAND3X18_P4	C12T28SOI_LL_-NAND3X21_P4	C12T28SOI_LL_-NAND3X24_P4
A (output stable)	8.512e-05	9.421e-05	1.330e-04	1.431e-04
B (output stable)	1.068e-04	1.210e-04	1.666e-04	1.821e-04
C (output stable)	2.682e-04	3.023e-04	4.167e-04	4.536e-04
A to Z	3.519e-03	4.009e-03	5.023e-03	5.524e-03
B to Z	2.951e-03	3.370e-03	4.215e-03	4.644e-03
C to Z	2.455e-03	2.795e-03	3.445e-03	3.798e-03
	C12T28SOI_LL_-NAND3X35_P4	C12T28SOI_LL_-NAND3X47_P4	C12T28SOI_-LLBR0P6_-NAND3X6_P4	C12T28SOI_-LLBR0P6_-NAND3X12_P4
A (output stable)	1.952e-04	2.535e-04	3.856e-05	1.100e-04
B (output stable)	2.458e-04	3.155e-04	5.270e-05	1.463e-04
C (output stable)	6.540e-04	8.315e-04	1.938e-04	3.641e-04
A to Z	7.990e-03	1.054e-02	1.639e-03	3.195e-03
B to Z	6.674e-03	8.805e-03	1.388e-03	2.463e-03
C to Z	5.402e-03	7.185e-03	1.013e-03	1.704e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	C12T28SOI_-LLBR0P6_-NAND3X24_P4	C12T28SOI_-LLBR0P6_-NAND3X35_P4	C12T28SOI_-LLBR0P6_-NAND3X47_P4
A (output stable)	1.323e-04	2.023e-04	2.704e-04	3.550e-04
B (output stable)	1.689e-04	2.579e-04	3.400e-04	4.486e-04
C (output stable)	4.139e-04	6.445e-04	9.307e-04	1.207e-03
A to Z	4.271e-03	5.932e-03	8.549e-03	1.129e-02
B to Z	3.297e-03	4.573e-03	6.580e-03	8.715e-03
C to Z	2.387e-03	3.196e-03	4.539e-03	6.052e-03
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4			
A (output stable)	1.608e-04			
B (output stable)	2.182e-04			
C (output stable)	5.171e-04			
A to Z	4.768e-03			
B to Z	3.691e-03			
C to Z	2.569e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P4	C12T28SOI_LL_-NAND3X18_P4	C12T28SOI_LL_-NAND3X21_P4	C12T28SOI_LL_-NAND3X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

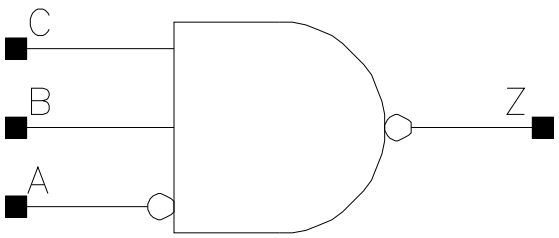
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P4	C12T28SOI_LL_-NAND3X47_P4	C12T28SOI_-LLBR0P6_-NAND3X6_P4	C12T28SOI_-LLBR0P6_-NAND3X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	C12T28SOI_-LLBR0P6_-NAND3X24_P4	C12T28SOI_-LLBR0P6_-NAND3X35_P4	C12T28SOI_-LLBR0P6_-NAND3X47_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.816	0.9792
X12_P4	1.200	1.224	1.4688
X18_P4	1.200	1.496	1.7952
X24_P4	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0007	0.0011	0.0011	0.0018
B	0.0008	0.0015	0.0022	0.0029
C	0.0007	0.0014	0.0020	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X12_P4**	**X6_P4**	**X12_P4**
A to Z ↓	0.0325	0.0305	5.3960	2.8493
A to Z ↑	0.0236	0.0227	3.2435	1.6292
B to Z ↓	0.0138	0.0141	5.4344	2.8703
B to Z ↑	0.0139	0.0137	3.3012	1.6628
C to Z ↓	0.0141	0.0127	5.4511	2.8779
C to Z ↑	0.0124	0.0111	3.3164	1.6737
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0351	0.0299	1.9499	1.4731

A to Z ↑	0.0264	0.0218	1.0953	0.8213
B to Z ↓	0.0145	0.0141	1.9623	1.4839
B to Z ↑	0.0136	0.0134	1.1190	0.8409
C to Z ↓	0.0137	0.0129	1.9663	1.4880
C to Z ↑	0.0116	0.0110	1.1251	0.8460

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P4	2.778e-05	1.000e-20
X12_P4	5.935e-05	1.000e-20
X18_P4	7.389e-05	1.000e-20
X24_P4	1.155e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	1.039e-03	1.856e-03	2.465e-03	3.530e-03
B (output stable)	2.531e-05	8.428e-05	1.276e-04	1.904e-04
C (output stable)	6.238e-05	2.628e-04	3.039e-04	4.824e-04
A to Z	2.379e-03	4.638e-03	6.668e-03	9.014e-03
B to Z	1.168e-03	2.264e-03	3.373e-03	4.370e-03
C to Z	1.024e-03	1.779e-03	2.791e-03	3.458e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

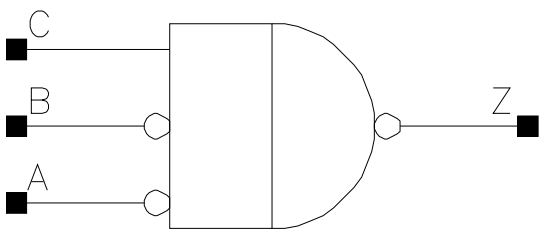
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	0.816	0.9792
X13_P4	1.200	1.088	1.3056
X20_P4	1.200	1.632	1.9584
X27_P4	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P4	X13_P4	X20_P4	X27_P4
A	0.0009	0.0009	0.0018	0.0017
B	0.0010	0.0010	0.0019	0.0018
C	0.0008	0.0014	0.0021	0.0028

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	**X13_P4**	**X7_P4**	**X13_P4**
A to Z ↓	0.0296	0.0359	3.7002	1.9580
A to Z ↑	0.0204	0.0234	3.2256	1.6215
B to Z ↓	0.0302	0.0367	3.7016	1.9569
B to Z ↑	0.0192	0.0223	3.2234	1.6213
C to Z ↓	0.0097	0.0091	3.7591	1.9836
C to Z ↑	0.0109	0.0098	3.3098	1.6714
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0328	0.0357	1.3317	1.0094
A to Z ↑	0.0218	0.0261	1.0915	0.8202
B to Z ↓	0.0314	0.0348	1.3302	1.0099

B to Z ↑	0.0198	0.0245	1.0907	0.8191
C to Z ↓	0.0101	0.0097	1.3512	1.0237
C to Z ↑	0.0105	0.0102	1.1253	0.8449

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X7_P4	4.276e-05	1.000e-20
X13_P4	5.766e-05	1.000e-20
X20_P4	9.376e-05	1.000e-20
X27_P4	1.048e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	5.968e-04	7.792e-04	1.339e-03	1.535e-03
B (output stable)	5.458e-04	7.269e-04	1.216e-03	1.429e-03
C (output stable)	3.508e-05	2.092e-04	2.061e-04	2.555e-04
A to Z	2.699e-03	4.417e-03	6.928e-03	8.586e-03
B to Z	2.501e-03	4.220e-03	6.210e-03	7.938e-03
C to Z	8.624e-04	1.553e-03	2.478e-03	3.261e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

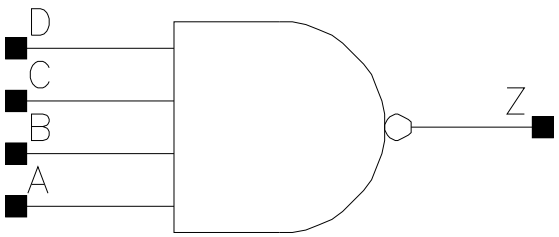
Pin Cycle (vdds)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0006	0.0006	0.0007	0.0009
B	0.0007	0.0007	0.0008	0.0010
C	0.0006	0.0007	0.0008	0.0010
D	0.0006	0.0006	0.0008	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0485	0.0470	2.2038	1.1041
A to Z ↑	0.0389	0.0416	3.2897	1.6321
B to Z ↓	0.0500	0.0493	2.2044	1.1042
B to Z ↑	0.0375	0.0411	3.2883	1.6334
C to Z ↓	0.0494	0.0473	2.2071	1.1039
C to Z ↑	0.0401	0.0435	3.2864	1.6286

D to Z ↓	0.0513	0.0488	2.2046	1.1043
D to Z ↑	0.0393	0.0419	3.2852	1.6323
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0497	0.0458	0.7600	0.5690
A to Z ↑	0.0399	0.0391	1.0997	0.8253
B to Z ↓	0.0514	0.0471	0.7600	0.5690
B to Z ↑	0.0389	0.0378	1.0989	0.8249
C to Z ↓	0.0465	0.0425	0.7596	0.5688
C to Z ↑	0.0405	0.0392	1.0983	0.8228
D to Z ↓	0.0481	0.0440	0.7597	0.5690
D to Z ↑	0.0390	0.0379	1.0969	0.8237

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	4.403e-05	1.000e-20
X17_P4	7.108e-05	1.000e-20
X25_P4	1.021e-04	1.000e-20
X33_P4	1.425e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	4.205e-04	5.175e-04	7.476e-04	9.053e-04
B (output stable)	3.941e-04	4.954e-04	7.085e-04	8.528e-04
C (output stable)	4.267e-04	5.121e-04	7.608e-04	8.837e-04
D (output stable)	3.993e-04	4.818e-04	7.156e-04	8.300e-04
A to Z	3.216e-03	4.861e-03	7.531e-03	9.261e-03
B to Z	3.140e-03	4.792e-03	7.416e-03	9.109e-03
C to Z	3.312e-03	4.821e-03	7.105e-03	8.632e-03
D to Z	3.244e-03	4.739e-03	6.986e-03	8.486e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

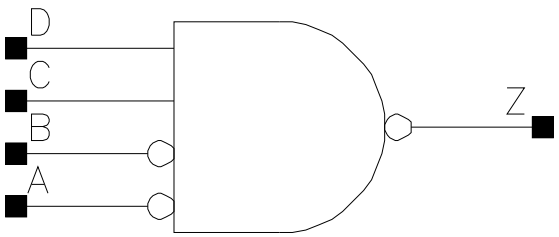
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X12_P4	1.200	1.496	1.7952
X18_P4	1.200	2.040	2.4480
X24_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0010	0.0010	0.0018	0.0017
B	0.0010	0.0014	0.0019	0.0018
C	0.0007	0.0015	0.0021	0.0029
D	0.0007	0.0014	0.0020	0.0028

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X12_P4	X6_P4	X12_P4
A to Z ↓	0.0317	0.0423	5.5311	2.8549
A to Z ↑	0.0215	0.0263	3.2221	1.6248
B to Z ↓	0.0318	0.0422	5.5328	2.8554
B to Z ↑	0.0196	0.0248	3.2183	1.6232
C to Z ↓	0.0139	0.0140	5.5712	2.8700
C to Z ↑	0.0140	0.0137	3.4595	1.6626

D to Z ↓	0.0139	0.0127	5.5857	2.8770
D to Z ↑	0.0124	0.0111	3.4754	1.6734
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0368	0.0410	1.9454	1.4758
A to Z ↑	0.0232	0.0297	1.0922	0.8218
B to Z ↓	0.0354	0.0399	1.9461	1.4758
B to Z ↑	0.0213	0.0279	1.0909	0.8206
C to Z ↓	0.0142	0.0146	1.9563	1.4830
C to Z ↑	0.0135	0.0138	1.1223	0.8390
D to Z ↓	0.0134	0.0135	1.9616	1.4867
D to Z ↑	0.0115	0.0114	1.1408	0.8450

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P4	3.622e-05	1.000e-20
X12_P4	5.004e-05	1.000e-20
X18_P4	8.192e-05	1.000e-20
X24_P4	8.828e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	6.798e-04	1.108e-03	1.697e-03	2.004e-03
B (output stable)	6.124e-04	1.020e-03	1.499e-03	1.824e-03
C (output stable)	2.742e-05	8.800e-05	1.230e-04	1.714e-04
D (output stable)	6.926e-05	2.725e-04	3.166e-04	4.964e-04
A to Z	2.826e-03	5.305e-03	7.883e-03	1.031e-02
B to Z	2.645e-03	4.986e-03	7.203e-03	9.639e-03
C to Z	1.133e-03	2.256e-03	3.297e-03	4.573e-03
D to Z	9.882e-04	1.772e-03	2.752e-03	3.691e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

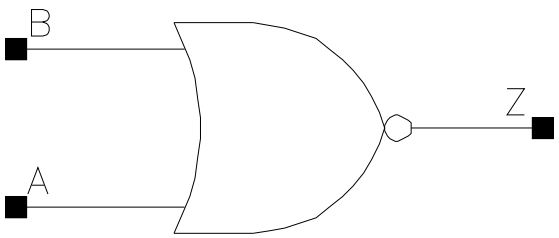
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.408	0.4896
X5_P4	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X10_P4	1.200	0.680	0.8160
X14_P4	1.200	0.680	0.8160
X17_P4	1.200	0.952	1.1424
X21_P4	1.200	0.952	1.1424
X24_P4	1.200	1.224	1.4688
X27_P4	1.200	1.224	1.4688
X34_P4	1.200	1.496	1.7952
X40_P4	1.200	1.360	1.6320
X41_P4	1.200	1.768	2.1216
X49_P4	1.200	1.496	1.7952
X53_P4	1.200	1.904	2.2848
X55_P4	1.200	2.312	2.7744
X57_P4	1.200	1.904	2.2848
X65_P4	1.200	2.040	2.4480
X84_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P4	X5_P4	X7_P4	X10_P4
A	0.0005	0.0006	0.0008	0.0013
B	0.0005	0.0006	0.0008	0.0011
	X14_P4	X17_P4	X21_P4	X24_P4

A	0.0016	0.0020	0.0023	0.0027
B	0.0014	0.0018	0.0021	0.0025
	X27_P4	X34_P4	X40_P4	X41_P4
A	0.0030	0.0038	0.0009	0.0046
B	0.0028	0.0034	0.0010	0.0043
	X49_P4	X53_P4	X55_P4	X57_P4
A	0.0009	0.0010	0.0061	0.0010
B	0.0010	0.0009	0.0056	0.0009
	X65_P4	X84_P4		
A	0.0010	0.0010		
B	0.0009	0.0009		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X5_P4**	**X3_P4**	**X5_P4**
A to Z ↓	0.0091	0.0086	4.3456	3.1068
A to Z ↑	0.0168	0.0152	12.4687	9.0156
B to Z ↓	0.0080	0.0073	4.4250	3.1267
B to Z ↑	0.0172	0.0154	12.5178	9.0389
	X7_P4	**X10_P4**	**X7_P4**	**X10_P4**
A to Z ↓	0.0084	0.0087	2.2646	1.4801
A to Z ↑	0.0141	0.0161	6.3175	4.2385
B to Z ↓	0.0070	0.0063	2.2910	1.4935
B to Z ↑	0.0141	0.0132	6.3369	4.2512
	X14_P4	**X17_P4**	**X14_P4**	**X17_P4**
A to Z ↓	0.0086	0.0086	1.1198	0.9028
A to Z ↑	0.0148	0.0149	3.1240	2.5325
B to Z ↓	0.0061	0.0068	1.1305	0.9092
B to Z ↑	0.0124	0.0135	3.1331	2.5390
	X21_P4	**X24_P4**	**X21_P4**	**X24_P4**
A to Z ↓	0.0087	0.0085	0.7640	0.6523
A to Z ↑	0.0143	0.0146	2.0974	1.8331
B to Z ↓	0.0068	0.0063	0.7694	0.6579
B to Z ↑	0.0130	0.0128	2.1031	1.8383
	X27_P4	**X34_P4**	**X27_P4**	**X34_P4**
A to Z ↓	0.0085	0.0088	0.5777	0.4663
A to Z ↑	0.0140	0.0143	1.6053	1.2797
B to Z ↓	0.0062	0.0067	0.5833	0.4697
B to Z ↑	0.0123	0.0129	1.6113	1.2834
	X40_P4	**X41_P4**	**X40_P4**	**X41_P4**
A to Z ↓	0.0325	0.0086	0.4650	0.3888
A to Z ↑	0.0438	0.0140	0.6760	1.0604
B to Z ↓	0.0311	0.0063	0.4650	0.3921
B to Z ↑	0.0447	0.0121	0.6748	1.0644
	X49_P4	**X53_P4**	**X49_P4**	**X53_P4**
A to Z ↓	0.0338	0.0352	0.3874	0.3551
A to Z ↑	0.0449	0.0511	0.5614	0.5198
B to Z ↓	0.0325	0.0338	0.3867	0.3553
B to Z ↑	0.0459	0.0516	0.5624	0.5199
	X55_P4	**X57_P4**	**X55_P4**	**X57_P4**
A to Z ↓	0.0087	0.0355	0.2937	0.3329
A to Z ↑	0.0140	0.0513	0.7988	0.4828

B to Z ↓	0.0064	0.0341	0.2967	0.3331
B to Z ↑	0.0122	0.0518	0.8016	0.4826
	X65_P4	**X84_P4**	**X65_P4**	**X84_P4**
A to Z ↓	0.0365	0.0380	0.2920	0.2315
A to Z ↑	0.0523	0.0528	0.4230	0.3351
B to Z ↓	0.0352	0.0366	0.2923	0.2313
B to Z ↑	0.0529	0.0534	0.4229	0.3350

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.001e-05	1.000e-20
X5_P4	1.542e-05	1.000e-20
X7_P4	2.372e-05	1.000e-20
X10_P4	3.236e-05	1.000e-20
X14_P4	4.670e-05	1.000e-20
X17_P4	5.497e-05	1.000e-20
X21_P4	6.813e-05	1.000e-20
X24_P4	7.762e-05	1.000e-20
X27_P4	8.960e-05	1.000e-20
X34_P4	1.111e-04	1.000e-20
X40_P4	1.757e-04	1.000e-20
X41_P4	1.325e-04	1.000e-20
X49_P4	1.992e-04	1.000e-20
X53_P4	2.294e-04	1.000e-20
X55_P4	1.755e-04	1.000e-20
X57_P4	2.447e-04	1.000e-20
X65_P4	2.682e-04	1.000e-20
X84_P4	3.144e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	1.507e-05	2.017e-05	2.775e-05	8.711e-05
B (output stable)	2.666e-05	3.529e-05	4.922e-05	2.244e-04
A to Z	5.858e-04	7.318e-04	9.870e-04	1.662e-03
B to Z	4.864e-04	6.006e-04	7.974e-04	1.117e-03
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	1.030e-04	1.216e-04	1.333e-04	1.686e-04
B (output stable)	2.612e-04	2.662e-04	2.706e-04	3.831e-04
A to Z	2.093e-03	2.607e-03	3.026e-03	3.552e-03
B to Z	1.444e-03	1.925e-03	2.246e-03	2.541e-03
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	1.800e-04	2.135e-04	2.807e-05	2.831e-04
B (output stable)	4.137e-04	4.201e-04	4.917e-05	6.154e-04
A to Z	3.922e-03	4.960e-03	8.975e-03	5.891e-03
B to Z	2.801e-03	3.695e-03	8.788e-03	4.164e-03
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	2.808e-05	2.941e-05	3.653e-04	2.891e-05
B (output stable)	4.940e-05	5.250e-05	8.089e-04	5.218e-05
A to Z	1.012e-02	1.251e-02	7.790e-03	1.299e-02
B to Z	9.939e-03	1.231e-02	5.566e-03	1.278e-02
	X65_P4	X84_P4		

A (output stable)	2.877e-05	3.009e-05		
B (output stable)	5.350e-05	5.418e-05		
A to Z	1.417e-02	1.692e-02		
B to Z	1.396e-02	1.666e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

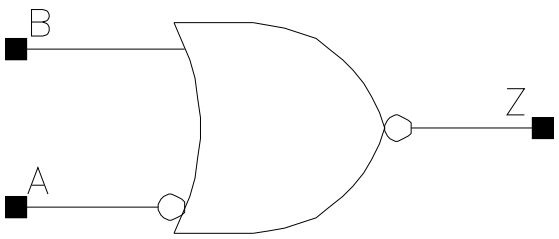
Pin Cycle (vdds)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P4	X84_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X7_P4	1.200	0.680	0.8160
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X41_P4	1.200	2.312	2.7744
X55_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X7_P4	X13_P4
A	0.0008	0.0007	0.0008	0.0011
B	0.0005	0.0008	0.0008	0.0014
	X27_P4	X41_P4	X55_P4	
A	0.0019	0.0028	0.0037	
B	0.0028	0.0043	0.0056	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0252	0.0278	4.2016	2.6988
A to Z ↑	0.0242	0.0241	12.3592	6.2758
B to Z ↓	0.0083	0.0084	4.4055	2.8469
B to Z ↑	0.0173	0.0139	12.4976	6.3539

	X7_P4	X13_P4	X7_P4	X13_P4
A to Z ↓	0.0282	0.0249	2.1279	1.1519
A to Z ↑	0.0265	0.0248	6.1933	3.2737
B to Z ↓	0.0075	0.0066	2.1860	1.1808
B to Z ↑	0.0154	0.0136	6.2440	3.3069
	X27_P4	X41_P4	X27_P4	X41_P4
A to Z ↓	0.0239	0.0244	0.5552	0.3756
A to Z ↑	0.0237	0.0240	1.5725	1.0550
B to Z ↓	0.0064	0.0065	0.5843	0.3937
B to Z ↑	0.0129	0.0127	1.5892	1.0654
	X55_P4		X55_P4	
A to Z ↓	0.0239		0.2839	
A to Z ↑	0.0236		0.7949	
B to Z ↓	0.0065		0.2982	
B to Z ↑	0.0125		0.8033	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	1.881e-05	1.000e-20
X6_P4	3.129e-05	1.000e-20
X7_P4	3.549e-05	1.000e-20
X13_P4	6.876e-05	1.000e-20
X27_P4	1.343e-04	1.000e-20
X41_P4	1.973e-04	1.000e-20
X55_P4	2.602e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	8.527e-04	1.041e-03	1.109e-03	1.820e-03
B (output stable)	2.655e-05	4.896e-05	1.292e-04	2.266e-04
A to Z	1.449e-03	1.987e-03	2.320e-03	3.890e-03
B to Z	4.939e-04	7.677e-04	9.350e-04	1.542e-03
	X27_P4	X41_P4	X55_P4	
A (output stable)	3.548e-03	5.386e-03	6.994e-03	
B (output stable)	4.362e-04	6.168e-04	8.012e-04	
A to Z	7.715e-03	1.148e-02	1.499e-02	
B to Z	2.997e-03	4.391e-03	5.780e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

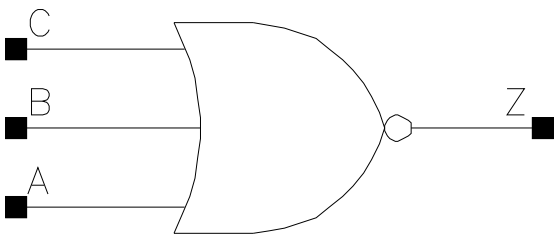
Pin Cycle (vdds)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P4	X41_P4	X55_P4	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X9_P4	1.200	0.952	1.1424
X13_P4	1.200	0.952	1.1424
X16_P4	1.200	1.360	1.6320
X19_P4	1.200	1.496	1.7952
X22_P4	1.200	1.768	2.1216
X25_P4	1.200	1.904	2.2848
X37_P4	1.200	2.584	3.1008
X49_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P4	X6_P4	X9_P4	X13_P4
A	0.0006	0.0008	0.0012	0.0015
B	0.0006	0.0008	0.0014	0.0016
C	0.0006	0.0008	0.0011	0.0014
	X16_P4	X19_P4	X22_P4	X25_P4
A	0.0020	0.0023	0.0027	0.0030
B	0.0020	0.0027	0.0029	0.0036
C	0.0018	0.0021	0.0025	0.0027
	X37_P4	X49_P4		
A	0.0046	0.0061		
B	0.0046	0.0062		

C	0.0040	0.0056		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0106	0.0102	3.1447	2.2954
A to Z ↑	0.0228	0.0206	13.2948	9.3112
B to Z ↓	0.0100	0.0094	3.1509	2.3010
B to Z ↑	0.0219	0.0195	13.3097	9.3231
C to Z ↓	0.0088	0.0081	3.1676	2.3224
C to Z ↑	0.0211	0.0186	13.3227	9.3312
	X9_P4	**X13_P4**	**X9_P4**	**X13_P4**
A to Z ↓	0.0104	0.0103	1.5199	1.1602
A to Z ↑	0.0229	0.0211	6.2290	4.6061
B to Z ↓	0.0098	0.0093	1.4878	1.1184
B to Z ↑	0.0228	0.0204	6.2377	4.6122
C to Z ↓	0.0074	0.0071	1.4988	1.1363
C to Z ↑	0.0173	0.0160	6.2382	4.6135
	X16_P4	**X19_P4**	**X16_P4**	**X19_P4**
A to Z ↓	0.0104	0.0102	0.9077	0.7618
A to Z ↑	0.0217	0.0212	3.7395	3.0805
B to Z ↓	0.0099	0.0097	0.9104	0.7489
B to Z ↑	0.0212	0.0213	3.7439	3.0845
C to Z ↓	0.0077	0.0076	0.9136	0.7755
C to Z ↑	0.0179	0.0169	3.7465	3.0861
	X22_P4	**X25_P4**	**X22_P4**	**X25_P4**
A to Z ↓	0.0103	0.0101	0.6632	0.5803
A to Z ↑	0.0214	0.0210	2.6669	2.3167
B to Z ↓	0.0096	0.0094	0.6538	0.5619
B to Z ↑	0.0209	0.0210	2.6704	2.3193
C to Z ↓	0.0073	0.0071	0.6594	0.5819
C to Z ↑	0.0167	0.0158	2.6720	2.3207
	X37_P4	**X49_P4**	**X37_P4**	**X49_P4**
A to Z ↓	0.0102	0.0103	0.3995	0.3020
A to Z ↑	0.0204	0.0204	1.5513	1.1673
B to Z ↓	0.0095	0.0096	0.3958	0.2996
B to Z ↑	0.0196	0.0196	1.5532	1.1692
C to Z ↓	0.0075	0.0076	0.3996	0.3024
C to Z ↑	0.0159	0.0162	1.5545	1.1703

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.227e-05	1.000e-20
X6_P4	1.924e-05	1.000e-20
X9_P4	2.612e-05	1.000e-20
X13_P4	3.850e-05	1.000e-20
X16_P4	4.476e-05	1.000e-20
X19_P4	5.794e-05	1.000e-20
X22_P4	6.354e-05	1.000e-20
X25_P4	7.629e-05	1.000e-20
X37_P4	1.117e-04	1.000e-20

X49_P4	1.483e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	2.246e-05	3.093e-05	5.806e-05	7.532e-05
B (output stable)	2.365e-05	3.312e-05	8.032e-05	9.633e-05
C (output stable)	6.055e-05	8.605e-05	2.654e-04	3.219e-04
A to Z	1.011e-03	1.305e-03	2.167e-03	2.699e-03
B to Z	8.529e-04	1.087e-03	1.872e-03	2.280e-03
C to Z	7.175e-04	8.914e-04	1.275e-03	1.578e-03
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	8.919e-05	1.080e-04	1.288e-04	1.496e-04
B (output stable)	1.160e-04	1.557e-04	1.748e-04	2.154e-04
C (output stable)	3.294e-04	4.363e-04	5.212e-04	6.326e-04
A to Z	3.432e-03	4.090e-03	4.730e-03	5.380e-03
B to Z	2.910e-03	3.518e-03	4.024e-03	4.616e-03
C to Z	2.205e-03	2.518e-03	2.872e-03	3.136e-03
	X37_P4	X49_P4		
A (output stable)	2.190e-04	2.893e-04		
B (output stable)	2.775e-04	3.653e-04		
C (output stable)	8.272e-04	1.081e-03		
A to Z	7.800e-03	1.038e-02		
B to Z	6.518e-03	8.672e-03		
C to Z	4.638e-03	6.230e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

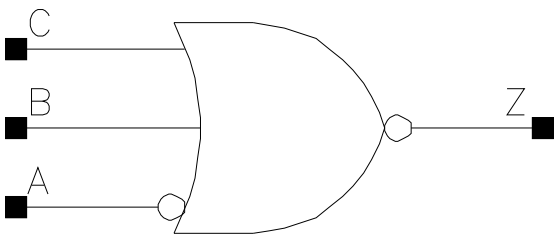
Pin Cycle (vdds)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P4	X49_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.680	0.8160
X13_P4	1.200	1.224	1.4688
X19_P4	1.200	1.496	1.7952
X25_P4	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0008	0.0010	0.0011	0.0019
B	0.0008	0.0016	0.0023	0.0031
C	0.0008	0.0014	0.0021	0.0028

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X13_P4**	**X6_P4**	**X13_P4**
A to Z ↓	0.0281	0.0260	2.2246	1.2092
A to Z ↑	0.0314	0.0305	9.4033	4.5974
B to Z ↓	0.0096	0.0093	2.3114	1.1238
B to Z ↑	0.0198	0.0203	9.4394	4.6128
C to Z ↓	0.0083	0.0069	2.3238	1.1368
C to Z ↑	0.0190	0.0158	9.4476	4.6135
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0299	0.0261	0.7497	0.5682

A to Z ↑	0.0334	0.0305	3.0882	2.3176
B to Z ↓	0.0097	0.0094	0.7778	0.5806
B to Z ↑	0.0198	0.0197	3.1005	2.3258
C to Z ↓	0.0076	0.0072	0.7764	0.5846
C to Z ↑	0.0170	0.0161	3.1025	2.3281

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P4	2.838e-05	1.000e-20
X13_P4	6.282e-05	1.000e-20
X19_P4	7.901e-05	1.000e-20
X25_P4	1.208e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	1.071e-03	1.910e-03	2.454e-03	3.769e-03
B (output stable)	3.382e-05	9.807e-05	1.349e-04	1.885e-04
C (output stable)	8.501e-05	3.277e-04	3.753e-04	5.741e-04
A to Z	2.409e-03	4.742e-03	6.521e-03	9.215e-03
B to Z	1.094e-03	2.268e-03	3.299e-03	4.392e-03
C to Z	9.034e-04	1.570e-03	2.503e-03	3.158e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

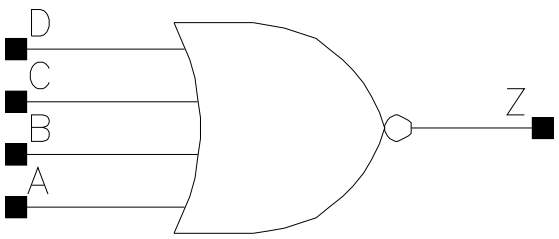
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	1.904	2.2848
X32_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X32_P4
A	0.0006	0.0006	0.0007	0.0009
B	0.0007	0.0006	0.0008	0.0011
C	0.0006	0.0006	0.0007	0.0009
D	0.0006	0.0006	0.0008	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0340	0.0336	2.1849	1.0726
A to Z ↑	0.0496	0.0529	3.3552	1.6521
B to Z ↓	0.0326	0.0325	2.1868	1.0728
B to Z ↑	0.0500	0.0536	3.3592	1.6536
C to Z ↓	0.0335	0.0336	2.1825	1.0725
C to Z ↑	0.0506	0.0545	3.3596	1.6510

D to Z ↓	0.0329	0.0330	2.1830	1.0719
D to Z ↑	0.0515	0.0556	3.3567	1.6526
	X25_P4	**X32_P4**	**X25_P4**	**X32_P4**
A to Z ↓	0.0343	0.0363	0.7427	0.5854
A to Z ↑	0.0512	0.0495	1.1243	0.8551
B to Z ↓	0.0333	0.0351	0.7432	0.5849
B to Z ↑	0.0521	0.0500	1.1249	0.8538
C to Z ↓	0.0332	0.0359	0.7407	0.5836
C to Z ↑	0.0509	0.0499	1.1232	0.8546
D to Z ↓	0.0320	0.0341	0.7407	0.5830
D to Z ↑	0.0517	0.0504	1.1241	0.8549

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	5.023e-05	1.000e-20
X17_P4	8.379e-05	1.000e-20
X25_P4	1.284e-04	1.000e-20
X32_P4	1.694e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	4.203e-04	5.076e-04	7.065e-04	9.008e-04
B (output stable)	3.814e-04	4.687e-04	6.551e-04	8.264e-04
C (output stable)	3.982e-04	4.697e-04	7.130e-04	9.088e-04
D (output stable)	3.605e-04	4.339e-04	6.589e-04	8.337e-04
A to Z	3.013e-03	4.682e-03	7.035e-03	8.838e-03
B to Z	2.905e-03	4.581e-03	6.882e-03	8.653e-03
C to Z	3.063e-03	4.696e-03	6.658e-03	8.444e-03
D to Z	2.951e-03	4.598e-03	6.520e-03	8.244e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

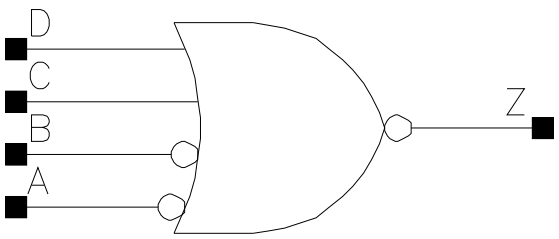
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X13_P4	1.200	1.496	1.7952
X19_P4	1.200	2.040	2.4480
X25_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0010	0.0010	0.0019	0.0018
B	0.0010	0.0014	0.0019	0.0019
C	0.0008	0.0015	0.0022	0.0029
D	0.0007	0.0014	0.0021	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X13_P4	X6_P4	X13_P4
A to Z ↓	0.0240	0.0299	2.1675	1.0847
A to Z ↑	0.0315	0.0390	9.0501	4.6601
B to Z ↓	0.0224	0.0287	2.1661	1.0825
B to Z ↑	0.0322	0.0400	9.0512	4.6608
C to Z ↓	0.0100	0.0095	2.3256	1.1235
C to Z ↑	0.0200	0.0206	9.0866	4.6768

D to Z ↓	0.0084	0.0072	2.3231	1.1333
D to Z ↑	0.0187	0.0165	9.0903	4.6779
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0262	0.0286	0.7417	0.5594
A to Z ↑	0.0348	0.0376	3.0914	2.3348
B to Z ↓	0.0239	0.0268	0.7407	0.5590
B to Z ↑	0.0350	0.0383	3.0921	2.3350
C to Z ↓	0.0098	0.0096	0.7789	0.5840
C to Z ↑	0.0197	0.0197	3.1033	2.3421
D to Z ↓	0.0076	0.0072	0.7772	0.5843
D to Z ↑	0.0169	0.0160	3.1047	2.3435

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P4	3.886e-05	1.000e-20
X13_P4	5.510e-05	1.000e-20
X19_P4	9.027e-05	1.000e-20
X25_P4	1.046e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	6.725e-04	1.088e-03	1.659e-03	1.976e-03
B (output stable)	6.211e-04	1.021e-03	1.515e-03	1.861e-03
C (output stable)	3.721e-05	1.131e-04	1.597e-04	2.156e-04
D (output stable)	1.016e-04	3.458e-04	4.299e-04	6.457e-04
A to Z	2.925e-03	5.429e-03	8.065e-03	1.030e-02
B to Z	2.784e-03	5.176e-03	7.550e-03	9.840e-03
C to Z	1.139e-03	2.296e-03	3.274e-03	4.334e-03
D to Z	9.396e-04	1.639e-03	2.503e-03	3.126e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

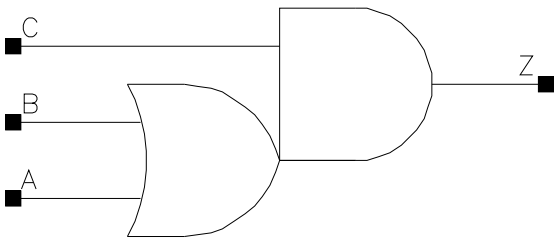
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0009	0.0009	0.0017
B	0.0010	0.0010	0.0020
C	0.0010	0.0010	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0264	0.0304	2.2456	1.1161
A to Z ↑	0.0237	0.0263	3.3725	1.6560
B to Z ↓	0.0267	0.0311	2.2469	1.1162
B to Z ↑	0.0216	0.0244	3.3654	1.6522
C to Z ↓	0.0241	0.0263	2.2266	1.1016
C to Z ↑	0.0225	0.0247	3.3676	1.6525
	X33_P4		**X33_P4**	
A to Z ↓	0.0318		0.5655	
A to Z ↑	0.0281		0.8298	

B to Z ↓	0.0324		0.5655	
B to Z ↑	0.0258		0.8295	
C to Z ↓	0.0268		0.5559	
C to Z ↑	0.0254		0.8295	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	5.012e-05	1.000e-20
X17_P4	7.466e-05	1.000e-20
X33_P4	1.476e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	5.071e-05	5.082e-05	1.076e-04
B (output stable)	6.082e-05	6.081e-05	1.218e-04
C (output stable)	5.406e-05	5.636e-05	1.066e-04
A to Z	2.331e-03	3.539e-03	7.409e-03
B to Z	2.124e-03	3.324e-03	6.992e-03
C to Z	2.531e-03	3.622e-03	7.444e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

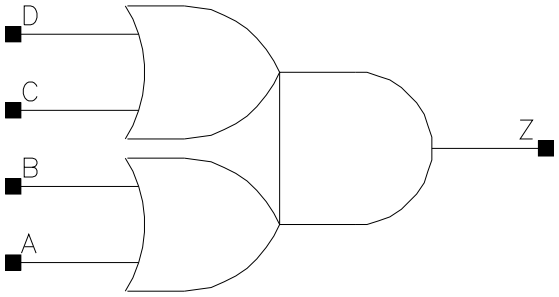
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0018
B	0.0006	0.0010	0.0018
C	0.0006	0.0009	0.0018
D	0.0006	0.0009	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0457	0.0380	2.1821	1.1074
A to Z ↑	0.0326	0.0285	3.3039	1.6519
B to Z ↓	0.0467	0.0388	2.1814	1.1072
B to Z ↑	0.0314	0.0270	3.2997	1.6500

C to Z ↓	0.0399	0.0336	2.1632	1.1007
C to Z ↑	0.0315	0.0284	3.2999	1.6500
D to Z ↓	0.0401	0.0339	2.1631	1.1012
D to Z ↑	0.0297	0.0262	3.2954	1.6482
	X33_P4		**X33_P4**	
A to Z ↓	0.0386		0.5693	
A to Z ↑	0.0286		0.8299	
B to Z ↓	0.0378		0.5694	
B to Z ↑	0.0264		0.8281	
C to Z ↓	0.0336		0.5655	
C to Z ↑	0.0280		0.8284	
D to Z ↓	0.0324		0.5658	
D to Z ↑	0.0255		0.8266	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	3.739e-05	1.000e-20
X17_P4	8.024e-05	1.000e-20
X33_P4	1.537e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	1.817e-05	2.916e-05	8.727e-05
B (output stable)	2.420e-05	4.119e-05	1.941e-04
C (output stable)	4.774e-05	6.509e-05	1.562e-04
D (output stable)	5.472e-05	7.841e-05	2.634e-04
A to Z	2.767e-03	4.515e-03	8.916e-03
B to Z	2.650e-03	4.282e-03	8.243e-03
C to Z	2.418e-03	4.037e-03	7.938e-03
D to Z	2.299e-03	3.807e-03	7.234e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

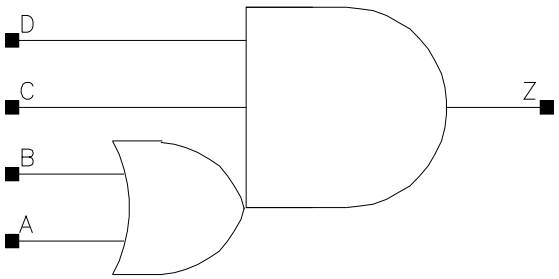
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	1.088	1.3056
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0006	0.0010	0.0015	0.0018
B	0.0006	0.0010	0.0015	0.0018
C	0.0007	0.0009	0.0016	0.0018
D	0.0006	0.0010	0.0015	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0387	0.0358	2.2941	1.1178
A to Z ↑	0.0384	0.0358	3.4267	1.6584
B to Z ↓	0.0395	0.0355	2.2920	1.1173
B to Z ↑	0.0365	0.0327	3.4194	1.6535
C to Z ↓	0.0324	0.0295	2.2460	1.0991

C to Z ↑	0.0360	0.0331	3.4207	1.6549
D to Z ↓	0.0315	0.0285	2.2453	1.0986
D to Z ↑	0.0375	0.0343	3.4187	1.6555
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0375	0.0358	0.7576	0.5675
A to Z ↑	0.0364	0.0369	1.1227	0.8414
B to Z ↓	0.0367	0.0351	0.7574	0.5679
B to Z ↑	0.0334	0.0337	1.1199	0.8394
C to Z ↓	0.0311	0.0296	0.7449	0.5585
C to Z ↑	0.0340	0.0337	1.1201	0.8390
D to Z ↓	0.0296	0.0283	0.7434	0.5578
D to Z ↑	0.0342	0.0343	1.1198	0.8391

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	3.385e-05	1.000e-20
X17_P4	7.421e-05	1.000e-20
X25_P4	1.105e-04	1.000e-20
X33_P4	1.464e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	4.075e-05	7.542e-05	1.270e-04	1.367e-04
B (output stable)	4.273e-05	8.843e-05	1.525e-04	1.627e-04
C (output stable)	1.474e-05	3.081e-05	7.610e-05	8.372e-05
D (output stable)	2.094e-05	4.021e-05	1.296e-04	1.436e-04
A to Z	2.355e-03	4.271e-03	6.796e-03	8.545e-03
B to Z	2.245e-03	3.981e-03	6.280e-03	7.876e-03
C to Z	2.457e-03	4.385e-03	7.153e-03	8.782e-03
D to Z	2.372e-03	4.222e-03	6.715e-03	8.342e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

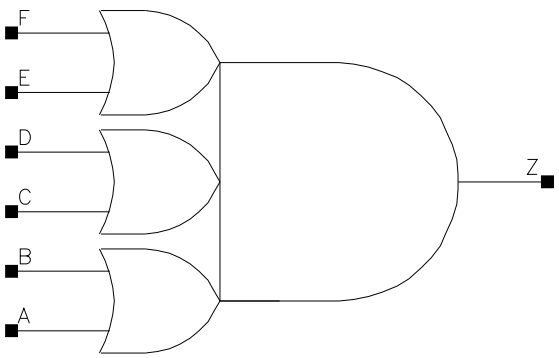
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0009	0.0016
B	0.0006	0.0009	0.0017
C	0.0006	0.0009	0.0016
D	0.0006	0.0009	0.0018
E	0.0006	0.0009	0.0016
F	0.0006	0.0009	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0521	0.0439	2.3372	1.1354
A to Z ↑	0.0418	0.0381	3.4056	1.6706
B to Z ↓	0.0528	0.0448	2.3368	1.1356
B to Z ↑	0.0401	0.0366	3.4039	1.6693
C to Z ↓	0.0480	0.0415	2.3225	1.1319
C to Z ↑	0.0422	0.0379	3.4066	1.6705
D to Z ↓	0.0490	0.0423	2.3227	1.1324
D to Z ↑	0.0403	0.0360	3.4013	1.6687
E to Z ↓	0.0419	0.0366	2.3050	1.1261
E to Z ↑	0.0391	0.0359	3.4036	1.6699
F to Z ↓	0.0430	0.0373	2.3053	1.1258
F to Z ↑	0.0374	0.0339	3.3962	1.6671
	X33_P4		X33_P4	
A to Z ↓	0.0440		0.5784	
A to Z ↑	0.0387		0.8417	
B to Z ↓	0.0451		0.5786	
B to Z ↑	0.0363		0.8396	
C to Z ↓	0.0406		0.5751	
C to Z ↑	0.0384		0.8412	
D to Z ↓	0.0415		0.5753	
D to Z ↑	0.0361		0.8394	
E to Z ↓	0.0360		0.5721	
E to Z ↑	0.0366		0.8406	
F to Z ↓	0.0369		0.5720	
F to Z ↑	0.0342		0.8387	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	3.907e-05	1.000e-20
X17_P4	8.654e-05	1.000e-20
X33_P4	1.647e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	1.641e-05	2.850e-05	5.327e-05
B (output stable)	2.067e-05	3.995e-05	7.120e-05
C (output stable)	2.666e-05	4.302e-05	8.637e-05
D (output stable)	3.222e-05	5.287e-05	1.047e-04
E (output stable)	7.342e-05	1.054e-04	1.980e-04
F (output stable)	7.589e-05	1.124e-04	2.158e-04
A to Z	3.175e-03	5.350e-03	1.045e-02
B to Z	3.048e-03	5.125e-03	9.989e-03
C to Z	2.914e-03	4.975e-03	9.635e-03
D to Z	2.795e-03	4.747e-03	9.175e-03
E to Z	2.578e-03	4.485e-03	8.714e-03
F to Z	2.473e-03	4.274e-03	8.287e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

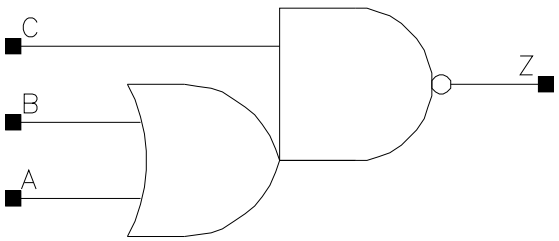
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X34_P4	1.200	2.720	3.2640
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X34_P4	X46_P4
A	0.0007	0.0022	0.0044	0.0057
B	0.0007	0.0020	0.0039	0.0053
C	0.0008	0.0023	0.0047	0.0061

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0126	0.0131	4.1651	1.3654
A to Z ↑	0.0149	0.0159	6.3098	2.1261
B to Z ↓	0.0105	0.0108	4.0966	1.3740
B to Z ↑	0.0148	0.0147	6.3297	2.1345
C to Z ↓	0.0119	0.0120	3.8021	1.2562
C to Z ↑	0.0146	0.0144	3.3984	1.1241
	X34_P4	**X46_P4**	**X34_P4**	**X46_P4**
A to Z ↓	0.0137	0.0136	0.6947	0.5290

A to Z ↑	0.0165	0.0162	1.0619	0.8127
B to Z ↓	0.0111	0.0112	0.7019	0.5362
B to Z ↑	0.0149	0.0150	1.0659	0.8155
C to Z ↓	0.0125	0.0123	0.6406	0.4888
C to Z ↑	0.0147	0.0145	0.5623	0.4286

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P4	2.799e-05	1.000e-20
X17_P4	8.189e-05	1.000e-20
X34_P4	1.623e-04	1.000e-20
X46_P4	2.142e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	4.536e-05	1.580e-04	3.360e-04	4.105e-04
B (output stable)	5.536e-05	2.033e-04	4.591e-04	5.377e-04
C (output stable)	4.924e-05	1.615e-04	3.411e-04	4.274e-04
A to Z	1.047e-03	3.357e-03	7.002e-03	9.017e-03
B to Z	8.542e-04	2.569e-03	5.290e-03	6.910e-03
C to Z	1.266e-03	3.864e-03	8.002e-03	1.033e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

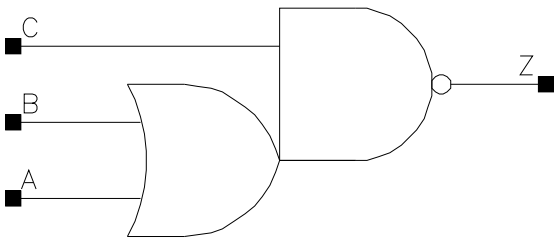
Pin Cycle (vdds)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.544	0.6528
X11_P4	1.200	0.952	1.1424
X17_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X17_P4	X23_P4
A	0.0008	0.0015	0.0023	0.0032
B	0.0007	0.0016	0.0021	0.0028
C	0.0007	0.0015	0.0021	0.0029
	X46_P4			
A	0.0063			
B	0.0057			
C	0.0058			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0131	0.0132	4.2513	1.9836
A to Z ↑	0.0189	0.0187	6.6503	3.1265
B to Z ↓	0.0112	0.0113	4.1910	1.9405

B to Z ↑	0.0189	0.0188	6.6678	3.1364
C to Z ↓	0.0106	0.0106	3.9483	1.8363
C to Z ↑	0.0112	0.0111	3.6273	1.7004
	X17_P4	**X23_P4**	**X17_P4**	**X23_P4**
A to Z ↓	0.0127	0.0134	1.3675	1.0147
A to Z ↑	0.0177	0.0196	2.0755	1.5798
B to Z ↓	0.0107	0.0111	1.3644	1.0142
B to Z ↑	0.0175	0.0183	2.0810	1.5843
C to Z ↓	0.0102	0.0104	1.2787	0.9475
C to Z ↑	0.0103	0.0106	1.1313	0.8591
	X46_P4		**X46_P4**	
A to Z ↓	0.0133		0.5265	
A to Z ↑	0.0191		0.7973	
B to Z ↓	0.0109		0.5222	
B to Z ↑	0.0178		0.7998	
C to Z ↓	0.0105		0.4901	
C to Z ↑	0.0103		0.4337	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.699e-05	1.000e-20
X11_P4	5.665e-05	1.000e-20
X17_P4	8.322e-05	1.000e-20
X23_P4	1.114e-04	1.000e-20
X46_P4	2.160e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	1.893e-05	4.106e-05	5.927e-05	1.097e-04
B (output stable)	2.406e-05	5.613e-05	7.946e-05	1.963e-04
C (output stable)	1.556e-04	3.706e-04	4.448e-04	7.001e-04
A to Z	1.285e-03	2.733e-03	3.805e-03	5.672e-03
B to Z	1.071e-03	2.306e-03	3.125e-03	4.425e-03
C to Z	8.745e-04	1.908e-03	2.632e-03	3.768e-03
	X46_P4			
A (output stable)	2.106e-04			
B (output stable)	3.578e-04			
C (output stable)	1.252e-03			
A to Z	1.092e-02			
B to Z	8.448e-03			
C to Z	7.223e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

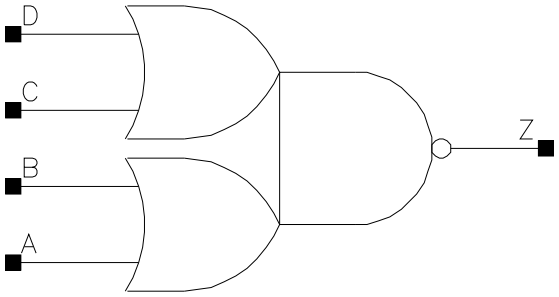
	X46_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0008	0.0015	0.0022	0.0031
B	0.0008	0.0014	0.0020	0.0028
C	0.0007	0.0015	0.0022	0.0030
D	0.0007	0.0013	0.0019	0.0027
	X42_P4			
A	0.0063			
B	0.0056			
C	0.0059			
D	0.0055			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0144	0.0155	3.8664	1.9412
A to Z ↑	0.0221	0.0223	6.9749	3.2030
B to Z ↓	0.0127	0.0133	3.8033	1.9452
B to Z ↑	0.0220	0.0207	6.9817	3.2131
C to Z ↓	0.0128	0.0141	3.9130	1.9518
C to Z ↑	0.0160	0.0172	6.8429	3.2114
D to Z ↓	0.0108	0.0113	3.8330	1.9600
D to Z ↑	0.0158	0.0148	6.8605	3.2262
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0147	0.0150	1.3255	0.9528
A to Z ↑	0.0208	0.0215	2.1526	1.5851
B to Z ↓	0.0129	0.0127	1.3313	0.9520
B to Z ↑	0.0199	0.0203	2.1588	1.5892
C to Z ↓	0.0136	0.0136	1.3344	0.9593
C to Z ↑	0.0158	0.0161	2.1585	1.5861
D to Z ↓	0.0113	0.0110	1.3479	0.9614
D to Z ↑	0.0144	0.0144	2.1677	1.5937
	X42_P4		**X42_P4**	
A to Z ↓	0.0153		0.4959	
A to Z ↑	0.0216		0.8048	
B to Z ↓	0.0131		0.4916	
B to Z ↑	0.0205		0.8069	
C to Z ↓	0.0143		0.5007	
C to Z ↑	0.0165		0.8009	
D to Z ↓	0.0116		0.4967	
D to Z ↑	0.0149		0.8044	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	3.222e-05	1.000e-20
X10_P4	6.885e-05	1.000e-20
X15_P4	9.951e-05	1.000e-20
X21_P4	1.348e-04	1.000e-20
X42_P4	2.640e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	2.584e-05	8.436e-05	1.062e-04	1.595e-04
B (output stable)	3.843e-05	1.879e-04	1.858e-04	3.048e-04
C (output stable)	5.375e-05	1.478e-04	1.850e-04	2.668e-04
D (output stable)	6.818e-05	2.513e-04	2.648e-04	4.120e-04
A to Z	1.534e-03	3.463e-03	4.751e-03	6.697e-03
B to Z	1.326e-03	2.796e-03	3.870e-03	5.423e-03
C to Z	1.110e-03	2.633e-03	3.568e-03	4.952e-03
D to Z	9.255e-04	1.968e-03	2.751e-03	3.774e-03
	X42_P4			
A (output stable)	3.112e-04			
B (output stable)	5.829e-04			
C (output stable)	5.185e-04			
D (output stable)	7.994e-04			

A to Z	1.330e-02			
B to Z	1.080e-02			
C to Z	1.003e-02			
D to Z	7.698e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

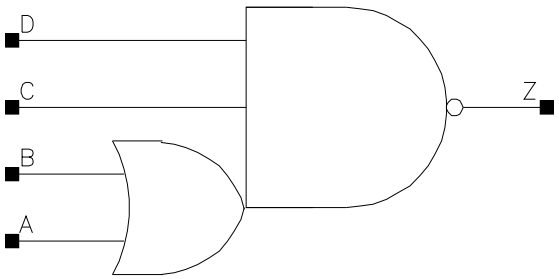
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X21_P4	1.200	2.448	2.9376
X31_P4	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X21_P4	X31_P4
A	0.0008	0.0014	0.0029	0.0043
B	0.0010	0.0013	0.0026	0.0039
C	0.0008	0.0016	0.0031	0.0046
D	0.0008	0.0015	0.0029	0.0043

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0189	0.0179	5.4220	2.8697
A to Z ↑	0.0206	0.0187	6.2807	3.1590
B to Z ↓	0.0167	0.0146	5.4618	2.8796
B to Z ↑	0.0203	0.0170	6.3145	3.1730
C to Z ↓	0.0170	0.0175	5.1305	2.7117

C to Z ↑	0.0178	0.0174	3.3055	1.6656
D to Z ↓	0.0181	0.0171	5.1495	2.7228
D to Z ↑	0.0170	0.0158	3.3401	1.6683
	X21_P4	**X31_P4**	**X21_P4**	**X31_P4**
A to Z ↓	0.0181	0.0183	1.4899	1.0091
A to Z ↑	0.0182	0.0182	1.5795	1.0592
B to Z ↓	0.0147	0.0149	1.4963	1.0160
B to Z ↑	0.0166	0.0166	1.5862	1.0642
C to Z ↓	0.0172	0.0173	1.4090	0.9553
C to Z ↑	0.0169	0.0169	0.8423	0.5675
D to Z ↓	0.0172	0.0173	1.4141	0.9588
D to Z ↑	0.0155	0.0155	0.8434	0.5670

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.475e-05	1.000e-20
X10_P4	4.695e-05	1.000e-20
X21_P4	8.969e-05	1.000e-20
X31_P4	1.325e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	7.392e-05	1.616e-04	2.878e-04	4.238e-04
B (output stable)	8.308e-05	1.825e-04	3.224e-04	4.678e-04
C (output stable)	2.876e-05	8.652e-05	1.648e-04	2.402e-04
D (output stable)	3.886e-05	1.451e-04	2.523e-04	3.609e-04
A to Z	1.566e-03	2.740e-03	5.296e-03	7.880e-03
B to Z	1.252e-03	2.090e-03	4.027e-03	6.026e-03
C to Z	1.835e-03	3.525e-03	6.739e-03	9.987e-03
D to Z	1.678e-03	3.007e-03	5.779e-03	8.599e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

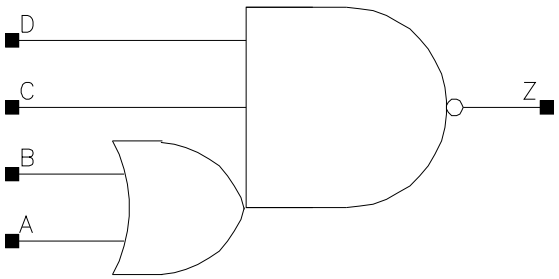
Pin Cycle (vdds)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0008	0.0016	0.0024	0.0032
B	0.0008	0.0015	0.0021	0.0029
C	0.0008	0.0015	0.0022	0.0029
D	0.0008	0.0014	0.0021	0.0028

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0174	0.0188	5.5233	2.8626
A to Z ↑	0.0218	0.0239	6.1357	3.1202
B to Z ↓	0.0152	0.0160	5.4485	2.8649
B to Z ↑	0.0219	0.0226	6.1504	3.1289
C to Z ↓	0.0140	0.0157	5.2192	2.7237

C to Z ↑	0.0139	0.0147	3.3558	1.6953
D to Z ↓	0.0142	0.0150	5.2372	2.7321
D to Z ↑	0.0123	0.0125	3.3737	1.7054
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0184	0.0186	1.9637	1.4791
A to Z ↑	0.0227	0.0234	2.0981	1.5882
B to Z ↓	0.0158	0.0158	1.9594	1.4772
B to Z ↑	0.0219	0.0224	2.1054	1.5930
C to Z ↓	0.0153	0.0156	1.8648	1.4047
C to Z ↑	0.0140	0.0143	1.1310	0.8506
D to Z ↓	0.0146	0.0151	1.8709	1.4091
D to Z ↑	0.0119	0.0123	1.1373	0.8554

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P4	2.442e-05	1.000e-20
X10_P4	4.746e-05	1.000e-20
X15_P4	6.754e-05	1.000e-20
X21_P4	9.133e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	1.668e-05	3.748e-05	5.414e-05	7.063e-05
B (output stable)	1.836e-05	6.126e-05	7.537e-05	1.066e-04
C (output stable)	4.559e-05	1.032e-04	1.521e-04	2.042e-04
D (output stable)	8.157e-05	2.766e-04	3.214e-04	4.910e-04
A to Z	1.718e-03	3.752e-03	5.287e-03	7.251e-03
B to Z	1.472e-03	3.044e-03	4.315e-03	5.894e-03
C to Z	1.213e-03	2.695e-03	3.741e-03	5.184e-03
D to Z	1.068e-03	2.256e-03	3.162e-03	4.361e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

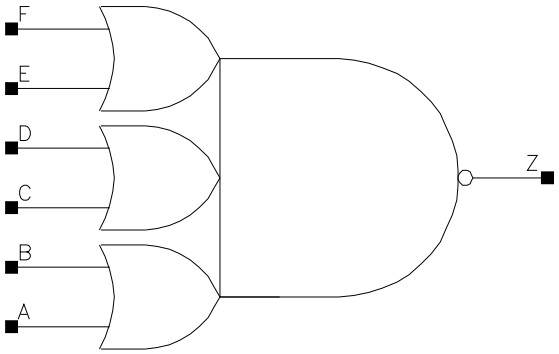
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	1.088	1.3056
X9_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X9_P4
A	0.0007	0.0016
B	0.0006	0.0015
C	0.0006	0.0015
D	0.0006	0.0014
E	0.0006	0.0015
F	0.0006	0.0014

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X9_P4	X3_P4	X9_P4
A to Z ↓	0.0221	0.0235	6.3935	2.5919
A to Z ↑	0.0303	0.0287	8.6940	3.1380
B to Z ↓	0.0207	0.0209	6.4329	2.5945
B to Z ↑	0.0312	0.0276	8.7042	3.1447
C to Z ↓	0.0214	0.0222	6.4428	2.6047
C to Z ↑	0.0263	0.0248	8.7099	3.1317
D to Z ↓	0.0196	0.0195	6.4763	2.6099
D to Z ↑	0.0270	0.0236	8.7294	3.1405
E to Z ↓	0.0183	0.0195	6.4615	2.6032
E to Z ↑	0.0205	0.0196	8.7318	3.1359
F to Z ↓	0.0168	0.0164	6.4957	2.6077
F to Z ↑	0.0211	0.0177	8.7653	3.1492

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P4	2.733e-05	1.000e-20
X9_P4	7.996e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P4	X9_P4
A (output stable)	2.250e-05	8.081e-05
B (output stable)	2.831e-05	1.475e-04
C (output stable)	3.754e-05	1.099e-04
D (output stable)	4.319e-05	1.794e-04
E (output stable)	9.152e-05	2.351e-04
F (output stable)	9.877e-05	2.988e-04
A to Z	1.955e-03	5.152e-03
B to Z	1.790e-03	4.452e-03
C to Z	1.611e-03	4.228e-03
D to Z	1.457e-03	3.602e-03
E to Z	1.213e-03	3.331e-03
F to Z	1.074e-03	2.679e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

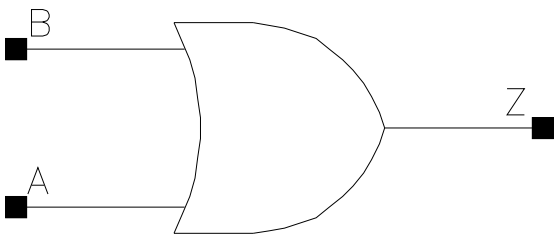
Pin Cycle (vdds)	X3_P4	X9_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X33_P4	1.200	1.360	1.6320
X50_P4	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P4	X16_P4	X33_P4	X50_P4
A	0.0007	0.0009	0.0017	0.0018
B	0.0006	0.0009	0.0018	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0352	0.0306	2.2499	1.1340
A to Z ↑	0.0224	0.0234	3.3305	1.6774
B to Z ↓	0.0353	0.0309	2.2505	1.1349
B to Z ↑	0.0211	0.0219	3.3348	1.6762
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0314	0.0372	0.5598	0.3840
A to Z ↑	0.0231	0.0230	0.8183	0.5511
B to Z ↓	0.0302	0.0364	0.5599	0.3835
B to Z ↑	0.0211	0.0214	0.8173	0.5508

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	2.977e-05	1.000e-20
X16_P4	5.937e-05	1.000e-20
X33_P4	1.189e-04	1.000e-20
X50_P4	1.554e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	1.580e-05	2.930e-05	1.017e-04	9.638e-05
B (output stable)	2.937e-05	5.180e-05	2.703e-04	2.515e-04
A to Z	2.071e-03	3.429e-03	7.128e-03	1.001e-02
B to Z	1.960e-03	3.235e-03	6.464e-03	9.388e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

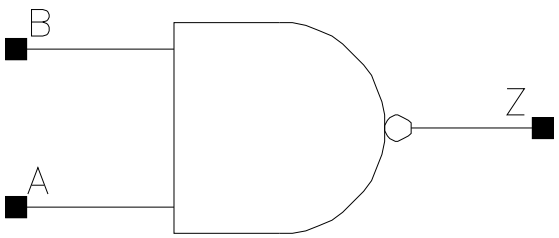
Pin Cycle (vdds)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X16_P4	1.200	0.952	1.1424
X24_P4	1.200	1.088	1.3056
X32_P4	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P4	X16_P4	X24_P4	X32_P4
A	0.0009	0.0009	0.0009	0.0009
B	0.0010	0.0010	0.0010	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0304	0.0314	2.1937	1.1365
A to Z ↑	0.0320	0.0326	3.3588	1.7097
B to Z ↓	0.0317	0.0328	2.1929	1.1352
B to Z ↑	0.0306	0.0308	3.3633	1.7092
	X24_P4	**X32_P4**	**X24_P4**	**X32_P4**
A to Z ↓	0.0347	0.0354	0.7671	0.5774
A to Z ↑	0.0351	0.0357	1.1418	0.8536
B to Z ↓	0.0361	0.0370	0.7681	0.5774
B to Z ↑	0.0332	0.0344	1.1404	0.8534

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	6.717e-05	1.000e-20
X16_P4	8.540e-05	1.000e-20
X24_P4	1.027e-04	1.000e-20
X32_P4	1.386e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	1.780e-05	1.788e-05	1.796e-05	1.908e-05
B (output stable)	3.157e-05	3.180e-05	3.180e-05	3.107e-05
A to Z	3.868e-03	4.499e-03	5.762e-03	7.556e-03
B to Z	3.733e-03	4.372e-03	5.644e-03	7.426e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

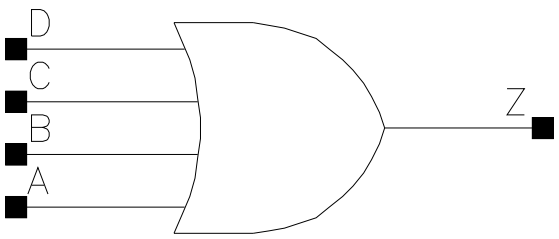
Pin Cycle (vdds)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P4	1.200	2.176	2.6112
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P4	X27_P4
A	0.0016	0.0018
B	0.0015	0.0018
C	0.0016	0.0019
D	0.0015	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P4	X27_P4	X20_P4	X27_P4
A to Z ↓	0.0353	0.0367	1.3472	1.0081
A to Z ↑	0.0240	0.0232	1.0940	0.8175
B to Z ↓	0.0346	0.0355	1.3472	1.0084
B to Z ↑	0.0225	0.0214	1.0932	0.8158
C to Z ↓	0.0342	0.0358	1.3454	1.0069
C to Z ↑	0.0228	0.0226	1.0952	0.8182
D to Z ↓	0.0335	0.0350	1.3452	1.0063
D to Z ↑	0.0214	0.0211	1.0951	0.8182

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X20_P4	9.434e-05	1.000e-20
X27_P4	1.377e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X20_P4	X27_P4
A (output stable)	1.430e-03	1.986e-03
B (output stable)	1.281e-03	1.781e-03
C (output stable)	1.290e-03	1.855e-03
D (output stable)	1.141e-03	1.695e-03
A to Z	6.268e-03	8.797e-03
B to Z	5.806e-03	8.096e-03
C to Z	5.657e-03	7.846e-03
D to Z	5.215e-03	7.251e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

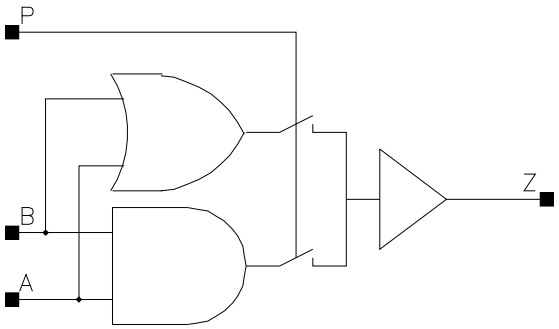
Pin Cycle (vdds)	X20_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X16_P4	1.200	1.224	1.4688
X25_P4	1.200	2.040	2.4480
X33_P4	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0011	0.0017	0.0029	0.0029
B	0.0011	0.0017	0.0033	0.0033
P	0.0006	0.0009	0.0017	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0429	0.0382	2.2951	1.1190
A to Z ↑	0.0303	0.0283	3.3837	1.6897
B to Z ↓	0.0428	0.0384	2.3009	1.1252
B to Z ↑	0.0313	0.0293	3.3867	1.6920
P to Z ↓	0.0391	0.0356	2.3008	1.1238
P to Z ↑	0.0300	0.0282	3.3836	1.6890
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**

A to Z ↓	0.0364	0.0387	0.7600	0.5747
A to Z ↑	0.0278	0.0292	1.1336	0.8497
B to Z ↓	0.0363	0.0383	0.7628	0.5769
B to Z ↑	0.0290	0.0301	1.1346	0.8501
P to Z ↓	0.0344	0.0367	0.7629	0.5765
P to Z ↑	0.0276	0.0290	1.1330	0.8490

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	3.537e-05	1.000e-20
X16_P4	7.824e-05	1.000e-20
X25_P4	1.311e-04	1.000e-20
X33_P4	1.517e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	3.465e-05	5.633e-05	1.244e-04	1.260e-04
B (output stable)	4.570e-05	8.192e-05	2.223e-04	2.225e-04
P (output stable)	1.348e-04	2.345e-04	3.547e-04	3.634e-04
A to Z	2.406e-03	4.188e-03	7.038e-03	8.342e-03
B to Z	2.353e-03	4.118e-03	6.813e-03	8.123e-03
P to Z	2.165e-03	3.849e-03	6.481e-03	7.784e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

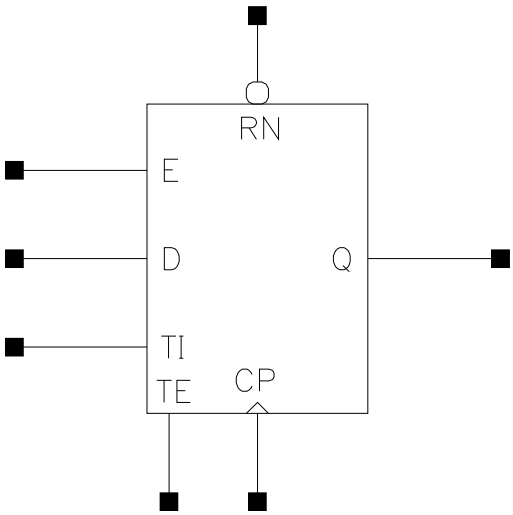
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.488	5.3856
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0006	0.0006	0.0006
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0006	0.0007	0.0008
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.0827	0.0427	4.9276	2.2169
CP to Q ↑	0.0683	0.0573	6.9037	3.3329
RN to Q ↓	0.0685	0.0590	4.3371	2.3170
	X17_P4	X33_P4	X17_P4	X33_P4
CP to Q ↓	0.0755	0.0792	1.0869	0.5688
CP to Q ↑	0.0934	0.0977	1.6365	0.8320
RN to Q ↓	0.1001	0.1036	1.0854	0.5666

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1108	0.0738	0.0738	0.0738
CP ↑	min_pulse_width to CP	0.0787	0.0364	0.0316	0.0316
D ↓	hold_rising to CP	-0.1141	-0.0501	-0.0501	-0.0533
D ↑	hold_rising to CP	-0.0724	-0.0244	-0.0235	-0.0235
D ↓	setup_rising to CP	0.1583	0.1004	0.1004	0.1004
D ↑	setup_rising to CP	0.1071	0.0532	0.0565	0.0565
E ↓	hold_rising to CP	-0.0821	-0.0838	-0.0838	-0.0838
E ↑	hold_rising to CP	-0.0728	-0.0241	-0.0241	-0.0241
E ↓	setup_rising to CP	0.1415	0.1392	0.1392	0.1392
E ↑	setup_rising to CP	0.1519	0.1026	0.1026	0.1026
RN ↓	min_pulse_width to RN	0.0708	0.0806	0.0713	0.0713
RN ↑	recovery_rising to CP	0.0200	0.0151	0.0173	0.0173
RN ↑	removal_rising to CP	-0.0126	-0.0056	-0.0056	-0.0056
TE ↓	hold_rising to CP	-0.0529	-0.0338	-0.0338	-0.0338
TE ↑	hold_rising to CP	-0.0484	-0.0311	-0.0337	-0.0337
TE ↓	setup_rising to CP	0.0993	0.0852	0.0852	0.0852
TE ↑	setup_rising to CP	0.2007	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.1481	-0.0771	-0.0771	-0.0771
TI ↑	hold_rising to CP	-0.0586	-0.0292	-0.0308	-0.0308
TI ↓	setup_rising to CP	0.1985	0.1274	0.1274	0.1274
TI ↑	setup_rising to CP	0.0917	0.0648	0.0648	0.0648

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.029e-04	1.000e-20
X8_P4	1.194e-04	1.000e-20
X17_P4	1.550e-04	1.000e-20
X33_P4	2.069e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

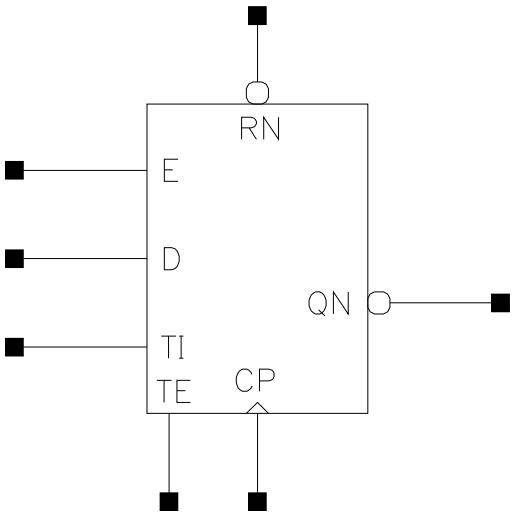
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	7.102e-03	7.143e-03	7.153e-03	7.159e-03
Clock 100Mhz Data 25Mhz	7.734e-03	7.767e-03	8.330e-03	9.061e-03
Clock 100Mhz Data 50Mhz	8.366e-03	8.392e-03	9.507e-03	1.096e-02
Clock = 0 Data 100Mhz	5.505e-03	5.169e-03	5.058e-03	5.003e-03
Clock = 1 Data 100Mhz	1.888e-03	1.922e-03	1.934e-03	1.940e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.624	5.5488
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0006	0.0006	0.0006
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.0844	0.0785	4.2557	2.1576
CP to QN ↑	0.0929	0.0578	6.7530	3.2570
RN to QN ↑	0.0846	0.0842	6.7415	3.2553
	X17_P4	X33_P4	X17_P4	X33_P4
CP to QN ↓	0.0742	0.0780	1.0888	0.5679
CP to QN ↑	0.0592	0.0642	1.6383	0.8334
RN to QN ↑	0.0819	0.0902	1.6414	0.8329

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1108	0.0738	0.0738	0.0738
CP ↑	min_pulse_width to CP	0.0565	0.0316	0.0363	0.0363
D ↓	hold_rising to CP	-0.1136	-0.0501	-0.0501	-0.0501
D ↑	hold_rising to CP	-0.0724	-0.0235	-0.0244	-0.0244
D ↓	setup_rising to CP	0.1636	0.1004	0.1004	0.1004
D ↑	setup_rising to CP	0.1071	0.0565	0.0565	0.0565
E ↓	hold_rising to CP	-0.0848	-0.0838	-0.0838	-0.0838
E ↑	hold_rising to CP	-0.0728	-0.0241	-0.0241	-0.0241
E ↓	setup_rising to CP	0.1409	0.1392	0.1392	0.1392
E ↑	setup_rising to CP	0.1514	0.1026	0.1026	0.1026
RN ↓	min_pulse_width to RN	0.0681	0.0713	0.0806	0.0876
RN ↑	recovery_rising to CP	0.0200	0.0200	0.0147	0.0147
RN ↑	removal_rising to CP	-0.0126	-0.0051	-0.0056	-0.0056
TE ↓	hold_rising to CP	-0.0550	-0.0338	-0.0338	-0.0338
TE ↑	hold_rising to CP	-0.0484	-0.0337	-0.0279	-0.0279
TE ↓	setup_rising to CP	0.0993	0.0852	0.0852	0.0852
TE ↑	setup_rising to CP	0.2007	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.1524	-0.0771	-0.0771	-0.0771
TI ↑	hold_rising to CP	-0.0586	-0.0308	-0.0292	-0.0292
TI ↓	setup_rising to CP	0.1985	0.1274	0.1274	0.1274
TI ↑	setup_rising to CP	0.0917	0.0648	0.0648	0.0648

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.037e-04	1.000e-20
X8_P4	1.171e-04	1.000e-20
X17_P4	1.497e-04	1.000e-20
X33_P4	1.954e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

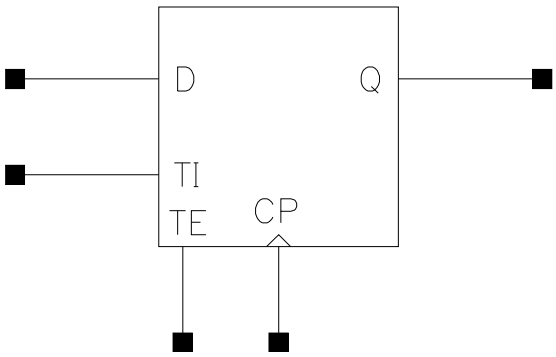
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	7.100e-03	7.142e-03	7.146e-03	7.150e-03
Clock 100Mhz Data 25Mhz	7.645e-03	7.796e-03	8.300e-03	9.041e-03
Clock 100Mhz Data 50Mhz	8.190e-03	8.451e-03	9.453e-03	1.093e-02
Clock = 0 Data 100Mhz	5.509e-03	5.173e-03	5.062e-03	5.006e-03
Clock = 1 Data 100Mhz	1.886e-03	1.925e-03	1.937e-03	1.943e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.400	4.0800
X8_P4	1.200	3.128	3.7536
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0676	0.0398	4.6298	2.2155
CP to Q ↑	0.0609	0.0518	6.9244	3.2991
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0614	0.0671	1.0694	0.5595
CP to Q ↑	0.0898	0.0948	1.6369	0.8322

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0991	0.1047	0.1047	0.1047
CP ↑	min_pulse_width to CP	0.0552	0.0316	0.0316	0.0316
D ↓	hold_rising to CP	-0.0701	-0.0267	-0.0267	-0.0267
D ↑	hold_rising to CP	-0.0289	-0.0017	-0.0049	-0.0049
D ↓	setup_rising to CP	0.1047	0.0684	0.0684	0.0684
D ↑	setup_rising to CP	0.0584	0.0294	0.0294	0.0294
TE ↓	hold_rising to CP	-0.0447	-0.0218	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0386	-0.0244	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.0879	0.0664	0.0664	0.0664
TE ↑	setup_rising to CP	0.1757	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.1442	-0.0876	-0.0892	-0.0892
TI ↑	hold_rising to CP	-0.0432	-0.0208	-0.0251	-0.0251
TI ↓	setup_rising to CP	0.1823	0.1371	0.1371	0.1371
TI ↑	setup_rising to CP	0.0728	0.0505	0.0505	0.0521

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	8.401e-05	1.000e-20
X8_P4	1.010e-04	1.000e-20
X17_P4	1.479e-04	1.000e-20
X33_P4	1.881e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

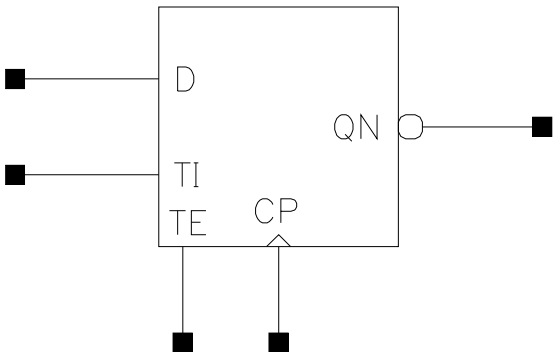
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	6.388e-03	6.423e-03	6.430e-03	6.434e-03
Clock 100Mhz Data 25Mhz	6.462e-03	6.489e-03	7.064e-03	7.692e-03
Clock 100Mhz Data 50Mhz	6.536e-03	6.556e-03	7.699e-03	8.950e-03
Clock = 0 Data 100Mhz	4.251e-03	3.939e-03	3.837e-03	3.786e-03
Clock = 1 Data 100Mhz	1.069e-03	5.519e-04	3.797e-04	2.935e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.536	4.2432
X8_P4	1.200	3.264	3.9168
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0783	0.0826	4.8592	2.2151
CP to QN ↑	0.0734	0.0533	6.8815	3.2611
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0628	0.0691	1.0712	0.5598
CP to QN ↑	0.0517	0.0570	1.6354	0.8317

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0991	0.1047	0.1047	0.1047
CP ↑	min_pulse_width to CP	0.0423	0.0316	0.0316	0.0316
D ↓	hold_rising to CP	-0.0701	-0.0267	-0.0267	-0.0267
D ↑	hold_rising to CP	-0.0283	-0.0049	-0.0017	-0.0017
D ↓	setup_rising to CP	0.1047	0.0684	0.0716	0.0684
D ↑	setup_rising to CP	0.0584	0.0294	0.0294	0.0294
TE ↓	hold_rising to CP	-0.0480	-0.0218	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0376	-0.0244	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.0879	0.0664	0.0664	0.0664
TE ↑	setup_rising to CP	0.1763	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.1442	-0.0892	-0.0876	-0.0876
TI ↑	hold_rising to CP	-0.0432	-0.0251	-0.0208	-0.0208
TI ↓	setup_rising to CP	0.1780	0.1371	0.1371	0.1371
TI ↑	setup_rising to CP	0.0728	0.0505	0.0505	0.0505

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	8.494e-05	1.000e-20
X8_P4	1.017e-04	1.000e-20
X17_P4	1.468e-04	1.000e-20
X33_P4	1.870e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

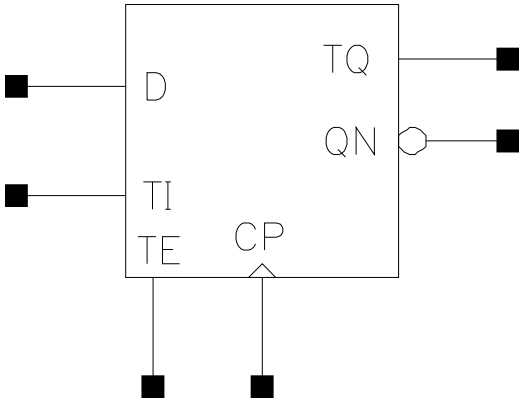
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	6.322e-03	6.388e-03	6.407e-03	6.418e-03
Clock 100Mhz Data 25Mhz	6.401e-03	6.570e-03	7.013e-03	7.655e-03
Clock 100Mhz Data 50Mhz	6.479e-03	6.752e-03	7.619e-03	8.892e-03
Clock = 0 Data 100Mhz	4.269e-03	3.948e-03	3.842e-03	3.788e-03
Clock = 1 Data 100Mhz	1.062e-03	5.482e-04	3.771e-04	2.915e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.536	4.2432
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0012	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006
TE	0.0009	0.0010	0.0010	0.0010

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0871	0.0738	4.3717	2.1696
CP to QN ↑	0.0884	0.0545	6.7445	3.2664
CP to TQ ↓	0.0615	0.0364	6.0298	4.1440
CP to TQ ↑	0.0630	0.0518	12.9995	9.2028
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0693	0.0746	1.0918	0.5702
CP to QN ↑	0.0560	0.0600	1.6535	0.8450
CP to TQ ↓	0.0376	0.0390	5.6360	5.6493
CP to TQ ↑	0.0528	0.0542	11.9936	12.6972

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0991	0.1047	0.1047	0.1047
CP ↑	min_pulse_width to CP	0.0551	0.0316	0.0316	0.0329
D ↓	hold_rising to CP	-0.0701	-0.0267	-0.0267	-0.0267
D ↑	hold_rising to CP	-0.0289	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.1047	0.0684	0.0684	0.0684
D ↑	setup_rising to CP	0.0584	0.0294	0.0294	0.0294
TE ↓	hold_rising to CP	-0.0447	-0.0218	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0386	-0.0244	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.0879	0.0664	0.0664	0.0664
TE ↑	setup_rising to CP	0.1763	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.1426	-0.0876	-0.0876	-0.0876
TI ↑	hold_rising to CP	-0.0432	-0.0208	-0.0208	-0.0208
TI ↓	setup_rising to CP	0.1780	0.1371	0.1371	0.1371
TI ↑	setup_rising to CP	0.0728	0.0521	0.0505	0.0505

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	9.023e-05	1.000e-20
X8_P4	1.127e-04	1.000e-20
X17_P4	1.383e-04	1.000e-20
X33_P4	1.857e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4

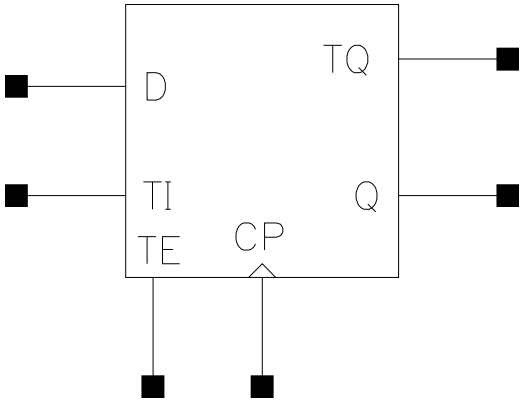
Clock 100Mhz Data 0Mhz	6.492e-03	6.475e-03	6.470e-03	6.468e-03
Clock 100Mhz Data 25Mhz	6.705e-03	6.810e-03	7.064e-03	7.804e-03
Clock 100Mhz Data 50Mhz	6.917e-03	7.144e-03	7.658e-03	9.140e-03
Clock = 0 Data 100Mhz	4.266e-03	3.953e-03	3.850e-03	3.799e-03
Clock = 1 Data 100Mhz	1.069e-03	5.521e-04	3.797e-04	2.936e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.400	4.0800
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006

TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0900	0.0446	4.8731	2.2075
CP to Q ↑	0.0702	0.0550	7.0146	3.3181
CP to TQ ↓	0.0849	0.0456	4.8632	5.7581
CP to TQ ↑	0.0723	0.0612	9.2770	12.9022
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0630	0.0688	1.0962	0.5693
CP to Q ↑	0.0913	0.0963	1.6628	0.8361
CP to TQ ↓	0.0653	0.0719	5.5730	5.6556
CP to TQ ↑	0.0974	0.1048	12.4998	12.6189

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0998	0.1047	0.1047	0.1047
CP ↑	min_pulse_width to CP	0.0787	0.0363	0.0316	0.0316
D ↓	hold_rising to CP	-0.0701	-0.0267	-0.0267	-0.0267
D ↑	hold_rising to CP	-0.0289	-0.0017	-0.0049	-0.0049
D ↓	setup_rising to CP	0.1047	0.0684	0.0684	0.0684
D ↑	setup_rising to CP	0.0584	0.0294	0.0294	0.0294
TE ↓	hold_rising to CP	-0.0447	-0.0218	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0386	-0.0244	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.0879	0.0664	0.0664	0.0664
TE ↑	setup_rising to CP	0.1757	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.1442	-0.0879	-0.0892	-0.0892
TI ↑	hold_rising to CP	-0.0432	-0.0208	-0.0251	-0.0251
TI ↓	setup_rising to CP	0.1823	0.1371	0.1371	0.1371
TI ↑	setup_rising to CP	0.0728	0.0521	0.0521	0.0521

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	9.205e-05	1.000e-20
X8_P4	1.061e-04	1.000e-20
X17_P4	1.518e-04	1.000e-20
X33_P4	1.919e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

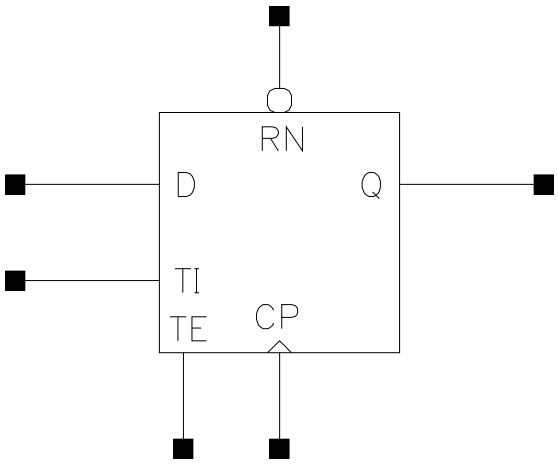
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	6.367e-03	6.411e-03	6.422e-03	6.427e-03
Clock 100Mhz Data 25Mhz	6.830e-03	6.688e-03	7.218e-03	7.896e-03
Clock 100Mhz Data 50Mhz	7.293e-03	6.965e-03	8.015e-03	9.364e-03
Clock = 0 Data 100Mhz	4.244e-03	3.936e-03	3.836e-03	3.786e-03
Clock = 1 Data 100Mhz	1.060e-03	5.473e-04	3.767e-04	2.913e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.672	4.4064
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006
RN	0.0008	0.0006	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0817	0.0425	4.9977	2.2229
CP to Q ↑	0.0674	0.0560	6.9374	3.3321
RN to Q ↓	0.0677	0.0599	4.3907	2.2976
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0644	0.0705	1.0822	0.5675
CP to Q ↑	0.0826	0.0873	1.6337	0.8314
RN to Q ↓	0.0895	0.0956	1.0803	0.5662

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1115	0.1070	0.1093	0.1093
CP ↑	min_pulse_width to CP	0.0705	0.0316	0.0317	0.0317
D ↓	hold_rising to CP	-0.0594	-0.0169	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0327	-0.0066	-0.0098	-0.0098
D ↓	setup_rising to CP	0.1047	0.0662	0.0662	0.0662
D ↑	setup_rising to CP	0.0686	0.0363	0.0396	0.0396
RN ↓	min_pulse_width to RN	0.0708	0.0757	0.0713	0.0713
RN ↑	recovery_rising to CP	0.0200	0.0168	0.0168	0.0200
RN ↑	removal_rising to CP	-0.0126	-0.0051	-0.0051	-0.0051
TE ↓	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0484	-0.0289	-0.0342	-0.0342
TE ↓	setup_rising to CP	0.0879	0.0656	0.0656	0.0656
TE ↑	setup_rising to CP	0.1709	0.1323	0.1323	0.1323
TI ↓	hold_rising to CP	-0.1286	-0.0681	-0.0697	-0.0697
TI ↑	hold_rising to CP	-0.0537	-0.0313	-0.0321	-0.0321
TI ↓	setup_rising to CP	0.1787	0.1287	0.1287	0.1287
TI ↑	setup_rising to CP	0.0868	0.0661	0.0661	0.0661

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	9.478e-05	1.000e-20
X8_P4	1.085e-04	1.000e-20
X17_P4	1.528e-04	1.000e-20
X33_P4	1.969e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	7.101e-03	7.115e-03	7.153e-03	7.173e-03

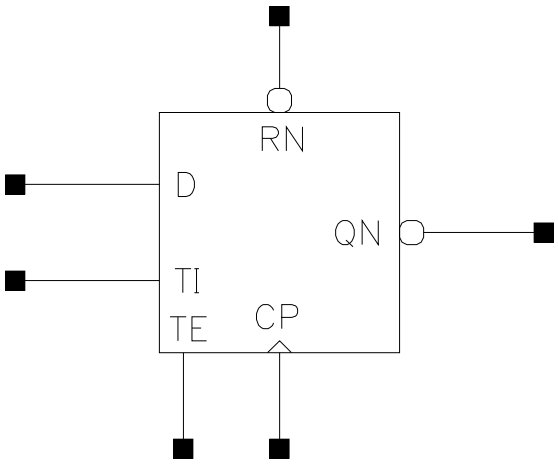
Clock 100Mhz Data 25Mhz	7.267e-03	7.147e-03	7.786e-03	8.449e-03
Clock 100Mhz Data 50Mhz	7.433e-03	7.178e-03	8.419e-03	9.724e-03
Clock = 0 Data 100Mhz	4.284e-03	3.909e-03	3.787e-03	3.726e-03
Clock = 1 Data 100Mhz	1.089e-03	5.631e-04	3.879e-04	3.004e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	3.944	4.7328
X33_P4	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0757	0.0696	4.1680	2.1110
CP to QN ↑	0.0842	0.0516	6.7459	3.2356
RN to QN ↑	0.0778	0.0787	6.7251	3.2327
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0685	0.0749	1.0832	0.5669
CP to QN ↑	0.0564	0.0620	1.6450	0.8398
RN to QN ↑	0.0803	0.0877	1.6464	0.8409

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1098	0.1053	0.1070	0.1070
CP ↑	min_pulse_width to CP	0.0517	0.0316	0.0363	0.0363
D ↓	hold_rising to CP	-0.0594	-0.0169	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0328	-0.0066	-0.0066	-0.0066
D ↓	setup_rising to CP	0.1047	0.0662	0.0662	0.0662
D ↑	setup_rising to CP	0.0686	0.0363	0.0363	0.0363
RN ↓	min_pulse_width to RN	0.0681	0.0691	0.0801	0.0828
RN ↑	recovery_rising to CP	0.0200	0.0200	0.0200	0.0200
RN ↑	removal_rising to CP	-0.0126	-0.0109	-0.0051	-0.0051
TE ↓	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0484	-0.0310	-0.0289	-0.0289
TE ↓	setup_rising to CP	0.0879	0.0656	0.0656	0.0656
TE ↑	setup_rising to CP	0.1704	0.1323	0.1323	0.1323
TI ↓	hold_rising to CP	-0.1286	-0.0697	-0.0681	-0.0681
TI ↑	hold_rising to CP	-0.0537	-0.0313	-0.0313	-0.0313
TI ↓	setup_rising to CP	0.1787	0.1289	0.1287	0.1287
TI ↑	setup_rising to CP	0.0868	0.0661	0.0661	0.0661

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	9.652e-05	1.000e-20
X8_P4	1.063e-04	1.000e-20
X17_P4	1.490e-04	1.000e-20
X33_P4	1.847e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	7.038e-03	7.082e-03	7.096e-03	7.103e-03

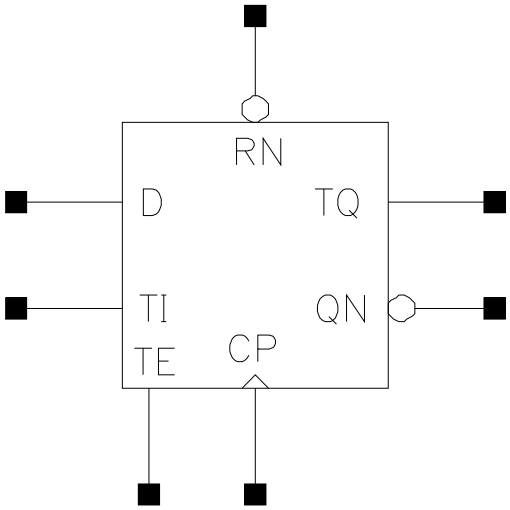
Clock 100Mhz Data 25Mhz	7.086e-03	7.120e-03	7.679e-03	8.330e-03
Clock 100Mhz Data 50Mhz	7.134e-03	7.159e-03	8.263e-03	9.557e-03
Clock = 0 Data 100Mhz	4.280e-03	3.905e-03	3.785e-03	3.726e-03
Clock = 1 Data 100Mhz	1.087e-03	5.621e-04	3.872e-04	2.999e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006

RN	0.0010	0.0007	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0844	0.0721	4.1881	2.2208
CP to QN ↑	0.1089	0.0575	6.0363	3.3550
CP to TQ ↓	0.0769	0.0387	5.3147	4.3498
CP to TQ ↑	0.0702	0.0569	10.4677	9.6896
RN to QN ↑	0.0763	0.0764	6.0863	3.3474
RN to TQ ↓	0.0523	0.0515	4.8242	4.5272
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0742	0.0797	1.0992	0.5768
CP to QN ↑	0.0579	0.0611	1.6712	0.8420
CP to TQ ↓	0.0403	0.0417	5.4769	5.3593
CP to TQ ↑	0.0569	0.0582	9.0703	9.1876
RN to QN ↑	0.0788	0.0842	1.6678	0.8401
RN to TQ ↓	0.0553	0.0579	5.6455	5.5533

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1098	0.1070	0.1093	0.1093
CP ↑	min_pulse_width to CP	0.0740	0.0316	0.0316	0.0363
D ↓	hold_rising to CP	-0.0598	-0.0169	-0.0169	-0.0137
D ↑	hold_rising to CP	-0.0328	-0.0066	-0.0098	-0.0098
D ↓	setup_rising to CP	0.1047	0.0662	0.0662	0.0662
D ↑	setup_rising to CP	0.0686	0.0363	0.0396	0.0396
RN ↓	min_pulse_width to RN	0.0708	0.0708	0.0757	0.0806
RN ↑	recovery_rising to CP	0.0222	0.0200	0.0200	0.0200
RN ↑	removal_rising to CP	-0.0147	-0.0051	-0.0051	-0.0051
TE ↓	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0484	-0.0315	-0.0310	-0.0310
TE ↓	setup_rising to CP	0.0879	0.0657	0.0656	0.0656
TE ↑	setup_rising to CP	0.1737	0.1323	0.1323	0.1323
TI ↓	hold_rising to CP	-0.1286	-0.0681	-0.0681	-0.0681
TI ↑	hold_rising to CP	-0.0537	-0.0313	-0.0305	-0.0305
TI ↓	setup_rising to CP	0.1787	0.1289	0.1287	0.1287
TI ↑	setup_rising to CP	0.0884	0.0661	0.0661	0.0661

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.060e-04	1.000e-20
X8_P4	1.120e-04	1.000e-20
X17_P4	1.376e-04	1.000e-20
X33_P4	1.808e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

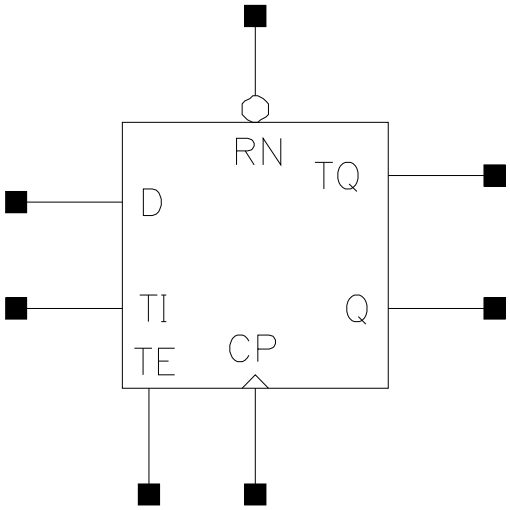
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	7.041e-03	7.081e-03	7.132e-03	7.158e-03
Clock 100Mhz Data 25Mhz	7.340e-03	7.263e-03	7.614e-03	8.385e-03
Clock 100Mhz Data 50Mhz	7.639e-03	7.445e-03	8.097e-03	9.611e-03
Clock = 0 Data 100Mhz	4.280e-03	3.906e-03	3.781e-03	3.719e-03
Clock = 1 Data 100Mhz	1.087e-03	5.622e-04	3.872e-04	2.998e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006

RN	0.0008	0.0008	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0918	0.0461	5.2175	2.2719
CP to Q ↑	0.0720	0.0585	7.1525	3.4331
CP to TQ ↓	0.0854	0.0454	6.6279	5.7875
CP to TQ ↑	0.0752	0.0623	14.1342	12.8138
RN to Q ↓	0.0698	0.0681	4.5571	2.3562
RN to TQ ↓	0.0679	0.0650	5.8771	5.9854
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0662	0.0728	1.0946	0.5741
CP to Q ↑	0.0829	0.0881	1.6404	0.8345
CP to TQ ↓	0.0684	0.0767	5.6015	5.6801
CP to TQ ↑	0.0885	0.0969	12.6241	12.6750
RN to Q ↓	0.0913	0.0980	1.0937	0.5731
RN to TQ ↓	0.0936	0.1019	5.5989	5.6760

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1098	0.1070	0.1070	0.1070
CP ↑	min_pulse_width to CP	0.0834	0.0363	0.0317	0.0317
D ↓	hold_rising to CP	-0.0604	-0.0142	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0327	-0.0066	-0.0098	-0.0098
D ↓	setup_rising to CP	0.1047	0.0662	0.0662	0.0662
D ↑	setup_rising to CP	0.0686	0.0363	0.0363	0.0363
RN ↓	min_pulse_width to RN	0.0735	0.0854	0.0686	0.0686
RN ↑	recovery_rising to CP	0.0200	0.0200	0.0200	0.0200
RN ↑	removal_rising to CP	-0.0126	-0.0077	-0.0051	-0.0051
TE ↓	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0484	-0.0289	-0.0310	-0.0310
TE ↓	setup_rising to CP	0.0879	0.0656	0.0656	0.0656
TE ↑	setup_rising to CP	0.1709	0.1323	0.1323	0.1323
TI ↓	hold_rising to CP	-0.1296	-0.0681	-0.0697	-0.0697
TI ↑	hold_rising to CP	-0.0537	-0.0313	-0.0313	-0.0313
TI ↓	setup_rising to CP	0.1790	0.1287	0.1289	0.1287
TI ↑	setup_rising to CP	0.0868	0.0661	0.0661	0.0661

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	9.842e-05	1.000e-20
X8_P4	1.126e-04	1.000e-20
X17_P4	1.552e-04	1.000e-20
X33_P4	1.993e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

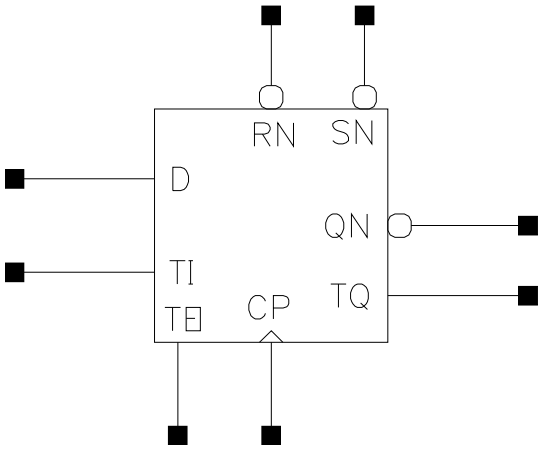
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	7.089e-03	7.106e-03	7.111e-03	7.113e-03
Clock 100Mhz Data 25Mhz	7.448e-03	7.289e-03	7.875e-03	8.586e-03
Clock 100Mhz Data 50Mhz	7.806e-03	7.471e-03	8.638e-03	1.006e-02
Clock = 0 Data 100Mhz	4.283e-03	3.908e-03	3.783e-03	3.721e-03
Clock = 1 Data 100Mhz	1.089e-03	5.631e-04	3.879e-04	3.004e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.352	5.2224
X17_P4	1.200	4.488	5.3856
X33_P4	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0005	0.0005	0.0005
RN	0.0007	0.0007	0.0007

SN	0.0012	0.0012	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
CP to QN ↓	0.0801	0.0849	2.1445	1.1047
CP to QN ↑	0.0596	0.0625	3.2515	1.6479
CP to TQ ↓	0.0454	0.0453	7.0731	7.0773
CP to TQ ↑	0.0670	0.0669	16.7215	16.7246
RN to QN ↓	0.0874	0.0921	2.1478	1.1046
RN to QN ↑	0.0851	0.0895	3.2597	1.6503
RN to TQ ↓	0.0647	0.0644	7.5047	7.5111
RN to TQ ↑	0.0745	0.0745	16.6794	16.6900
SN to QN ↓	0.0936	0.0994	2.1576	1.1091
SN to TQ ↑	0.0791	0.0789	16.8796	16.8922
	X33_P4		X33_P4	
CP to QN ↓	0.0969		0.5841	
CP to QN ↑	0.0699		0.8415	
CP to TQ ↓	0.0453		7.0875	
CP to TQ ↑	0.0671		16.7540	
RN to QN ↓	0.1039		0.5839	
RN to QN ↑	0.0992		0.8415	
RN to TQ ↓	0.0643		7.5202	
RN to TQ ↑	0.0747		16.7206	
SN to QN ↓	0.1130		0.5846	
SN to TQ ↑	0.0789		16.9478	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1141	0.1141	0.1141
CP ↑	min_pulse_width to CP	0.0363	0.0363	0.0376
D ↓	hold_rising to CP	-0.0169	-0.0169	-0.0169
D ↑	hold_rising to CP	-0.0066	-0.0066	-0.0066
D ↓	setup_rising to CP	0.0711	0.0711	0.0711
D ↑	setup_rising to CP	0.0391	0.0391	0.0391
RN ↓	min_pulse_width to RN	0.0779	0.0828	0.0876
RN ↑	non_seq_hold_rising to SN	-0.0309	-0.0309	-0.0309
RN ↑	non_seq_setup_rising to SN	0.0719	0.0719	0.0719
RN ↑	recovery_rising to CP	0.0297	0.0297	0.0297
RN ↑	removal_rising to CP	-0.0174	-0.0174	-0.0174
SN ↓	min_pulse_width to SN	0.0696	0.0696	0.0745
SN ↑	recovery_rising to CP	0.0081	0.0081	0.0081
SN ↑	removal_rising to CP	0.0361	0.0361	0.0361

TE ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0289	-0.0289	-0.0289
TE ↓	setup_rising to CP	0.0710	0.0710	0.0710
TE ↑	setup_rising to CP	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.0697	-0.0697	-0.0697
TI ↑	hold_rising to CP	-0.0313	-0.0313	-0.0313
TI ↓	setup_rising to CP	0.1371	0.1371	0.1371
TI ↑	setup_rising to CP	0.0661	0.0661	0.0661

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	1.239e-04	1.000e-20
X17_P4	1.443e-04	1.000e-20
X33_P4	1.821e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

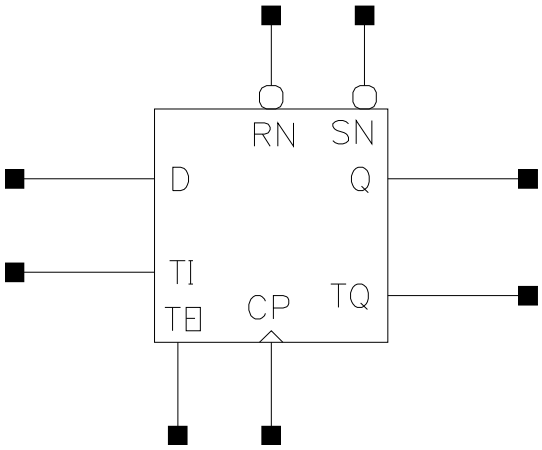
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	7.522e-03	7.522e-03	7.523e-03
Clock 100Mhz Data 25Mhz	7.618e-03	7.938e-03	8.834e-03
Clock 100Mhz Data 50Mhz	7.715e-03	8.354e-03	1.015e-02
Clock = 0 Data 100Mhz	3.661e-03	3.661e-03	3.662e-03
Clock = 1 Data 100Mhz	3.745e-05	3.753e-05	3.742e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.216	5.0592
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0008

SN	0.0012	0.0012	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
CP to Q ↓	0.0505	0.0563	2.2183	1.1487
CP to Q ↑	0.0643	0.0679	3.3313	1.6932
CP to TQ ↓	0.0510	0.0574	7.1655	7.2413
CP to TQ ↑	0.0718	0.0792	16.3335	16.4137
RN to Q ↓	0.0775	0.0900	2.4678	1.2830
RN to Q ↑	0.0587	0.0667	3.4445	1.7569
RN to TQ ↓	0.0752	0.0869	7.6786	7.8400
RN to TQ ↑	0.0712	0.0856	16.4667	16.5612
SN to Q ↑	0.0784	0.0862	3.4454	1.7545
SN to TQ ↑	0.0908	0.1051	16.4778	16.5653
	X33_P4		X33_P4	
CP to Q ↓	0.0710		0.6137	
CP to Q ↑	0.0774		0.8749	
CP to TQ ↓	0.0687		7.4546	
CP to TQ ↑	0.0930		16.5741	
RN to Q ↓	0.1196		0.6960	
RN to Q ↑	0.0863		0.9146	
RN to TQ ↓	0.1081		8.2498	
RN to TQ ↑	0.1137		16.7265	
SN to Q ↑	0.1055		0.9148	
SN to TQ ↑	0.1330		16.7295	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1141	0.1141	0.1141
CP ↑	min_pulse_width to CP	0.0410	0.0456	0.0598
D ↓	hold_rising to CP	-0.0169	-0.0169	-0.0142
D ↑	hold_rising to CP	-0.0066	-0.0066	-0.0066
D ↓	setup_rising to CP	0.0711	0.0711	0.0711
D ↑	setup_rising to CP	0.0391	0.0391	0.0391
RN ↓	min_pulse_width to RN	0.0925	0.1072	0.1414
RN ↑	non_seq_hold_rising to SN	-0.0335	-0.0405	-0.0552
RN ↑	non_seq_setup_rising to SN	0.0670	0.0693	0.0945
RN ↑	recovery_rising to CP	0.0249	0.0245	0.0245
RN ↑	removal_rising to CP	-0.0125	-0.0120	-0.0120
SN ↓	min_pulse_width to SN	0.0745	0.0891	0.1135
SN ↑	recovery_rising to CP	0.0081	0.0081	0.0081
SN ↑	removal_rising to CP	0.0361	0.0361	0.0361

TE ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0289	-0.0289	-0.0289
TE ↓	setup_rising to CP	0.0710	0.0710	0.0710
TE ↑	setup_rising to CP	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.0697	-0.0681	-0.0681
TI ↑	hold_rising to CP	-0.0315	-0.0315	-0.0315
TI ↓	setup_rising to CP	0.1371	0.1371	0.1371
TI ↑	setup_rising to CP	0.0661	0.0659	0.0659

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P4	1.249e-04	1.000e-20
X17_P4	1.474e-04	1.000e-20
X33_P4	1.903e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

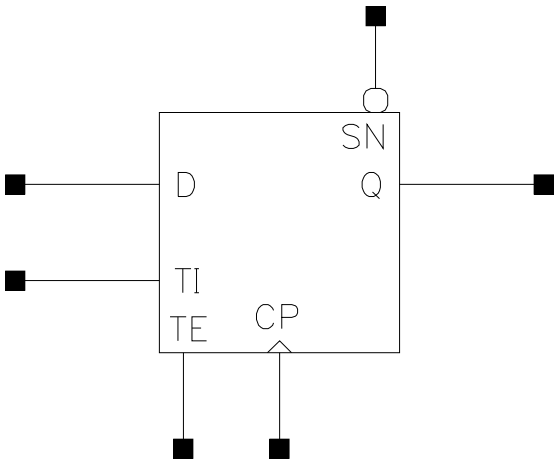
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	7.509e-03	7.510e-03	7.512e-03
Clock 100Mhz Data 25Mhz	7.584e-03	8.028e-03	9.248e-03
Clock 100Mhz Data 50Mhz	7.659e-03	8.546e-03	1.099e-02
Clock = 0 Data 100Mhz	3.659e-03	3.659e-03	3.659e-03
Clock = 1 Data 100Mhz	3.755e-05	3.745e-05	3.772e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004
SN	0.0014	0.0013	0.0013	0.0013
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0009			
D	0.0004			
SN	0.0013			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.0823	0.0443	5.0024	2.2081
CP to Q ↑	0.0708	0.0589	6.9998	3.3187
SN to Q ↑	0.0533	0.0607	6.8122	3.3185
	X17_P4	X25_P4	X17_P4	X25_P4
CP to Q ↓	0.0633	0.0667	1.0808	0.7474
CP to Q ↑	0.0829	0.0856	1.6331	1.1045
SN to Q ↑	0.0839	0.0867	1.6327	1.1038
	X33_P4		X33_P4	
CP to Q ↓	0.0693		0.5675	
CP to Q ↑	0.0875		0.8318	
SN to Q ↑	0.0884		0.8317	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.1138	0.1157	0.1157	0.1157
CP ↑	min_pulse_width to CP	0.0740	0.0330	0.0317	0.0317
D ↓	hold_rising to CP	-0.0653	-0.0186	-0.0218	-0.0218
D ↑	hold_rising to CP	-0.0337	-0.0045	-0.0045	-0.0045
D ↓	setup_rising to CP	0.1095	0.0710	0.0710	0.0710
D ↑	setup_rising to CP	0.0633	0.0347	0.0347	0.0347
SN ↓	min_pulse_width to SN	0.0474	0.0571	0.0544	0.0544
SN ↑	recovery_rising to CP	0.0080	0.0081	0.0081	0.0081
SN ↑	removal_rising to CP	0.0260	0.0362	0.0362	0.0362
TE ↓	hold_rising to CP	-0.0484	-0.0169	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0425	-0.0261	-0.0261	-0.0261
TE ↓	setup_rising to CP	0.0928	0.0686	0.0686	0.0686
TE ↑	setup_rising to CP	0.1785	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.1344	-0.0779	-0.0779	-0.0779
TI ↑	hold_rising to CP	-0.0481	-0.0257	-0.0257	-0.0257
TI ↓	setup_rising to CP	0.1836	0.1384	0.1384	0.1384
TI ↑	setup_rising to CP	0.0835	0.0570	0.0570	0.0570
		X33_P4			

CP ↓	min_pulse_width to CP	0.1157			
CP ↑	min_pulse_width to CP	0.0317			
D ↓	hold_rising to CP	-0.0218			
D ↑	hold_rising to CP	-0.0045			
D ↓	setup_rising to CP	0.0710			
D ↑	setup_rising to CP	0.0347			
SN ↓	min_pulse_width to SN	0.0544			
SN ↑	recovery_rising to CP	0.0081			
SN ↑	removal_rising to CP	0.0362			
TE ↓	hold_rising to CP	-0.0169			
TE ↑	hold_rising to CP	-0.0261			
TE ↓	setup_rising to CP	0.0686			
TE ↑	setup_rising to CP	0.1421			
TI ↓	hold_rising to CP	-0.0779			
TI ↑	hold_rising to CP	-0.0257			
TI ↓	setup_rising to CP	0.1384			
TI ↑	setup_rising to CP	0.0570			

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	9.299e-05	1.000e-20
X8_P4	1.093e-04	1.000e-20
X17_P4	1.518e-04	1.000e-20
X25_P4	1.697e-04	1.000e-20
X33_P4	1.875e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	6.891e-03	7.042e-03	7.092e-03	7.117e-03
Clock 100Mhz Data 25Mhz	7.097e-03	7.152e-03	7.724e-03	8.076e-03
Clock 100Mhz Data 50Mhz	7.303e-03	7.261e-03	8.356e-03	9.036e-03
Clock = 0 Data 100Mhz	4.086e-03	3.823e-03	3.736e-03	3.693e-03
Clock = 1 Data 100Mhz	1.088e-03	5.627e-04	3.876e-04	3.001e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	7.132e-03			

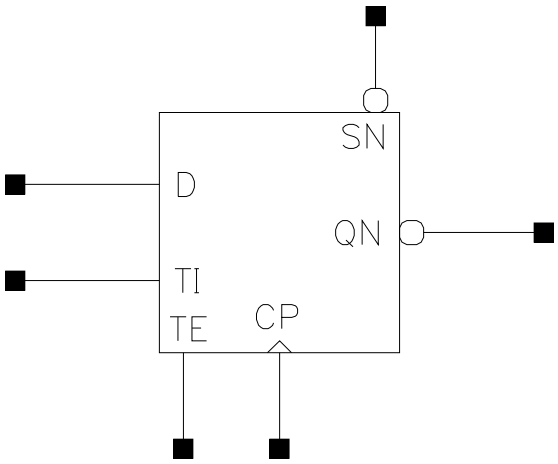
Clock 100Mhz Data 25Mhz	8.394e-03			
Clock 100Mhz Data 50Mhz	9.655e-03			
Clock = 0 Data 100Mhz	3.666e-03			
Clock = 1 Data 100Mhz	2.476e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004
SN	0.0014	0.0013	0.0013	0.0013
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0009			
D	0.0004			
SN	0.0013			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.0792	0.0703	4.1718	2.1125
CP to QN ↑	0.0851	0.0513	6.7313	3.2468
SN to QN ↓	0.0630	0.0712	4.1557	2.1112
	X17_P4	X25_P4	X17_P4	X25_P4
CP to QN ↓	0.0730	0.0770	1.0860	0.7487
CP to QN ↑	0.0599	0.0635	1.6357	1.1056
SN to QN ↓	0.0756	0.0797	1.0864	0.7486
	X33_P4		X33_P4	
CP to QN ↓	0.0802		0.5690	
CP to QN ↑	0.0660		0.8327	
SN to QN ↓	0.0828		0.5692	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.1138	0.1157	0.1157	0.1164
CP ↑	min_pulse_width to CP	0.0517	0.0317	0.0363	0.0363
D ↓	hold_rising to CP	-0.0653	-0.0218	-0.0191	-0.0191
D ↑	hold_rising to CP	-0.0337	-0.0045	-0.0045	-0.0045
D ↓	setup_rising to CP	0.1095	0.0710	0.0710	0.0710
D ↑	setup_rising to CP	0.0633	0.0347	0.0347	0.0347
SN ↓	min_pulse_width to SN	0.0474	0.0544	0.0571	0.0593
SN ↑	recovery_rising to CP	0.0081	0.0081	0.0081	0.0081
SN ↑	removal_rising to CP	0.0260	0.0362	0.0362	0.0362
TE ↓	hold_rising to CP	-0.0484	-0.0169	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0425	-0.0261	-0.0261	-0.0261
TE ↓	setup_rising to CP	0.0928	0.0686	0.0713	0.0713
TE ↑	setup_rising to CP	0.1785	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.1344	-0.0779	-0.0781	-0.0781
TI ↑	hold_rising to CP	-0.0481	-0.0257	-0.0257	-0.0257
TI ↓	setup_rising to CP	0.1836	0.1384	0.1384	0.1384
TI ↑	setup_rising to CP	0.0835	0.0570	0.0613	0.0613
		X33_P4			

CP ↓	min_pulse_width to CP	0.1164			
CP ↑	min_pulse_width to CP	0.0363			
D ↓	hold_rising to CP	-0.0191			
D ↑	hold_rising to CP	-0.0045			
D ↓	setup_rising to CP	0.0710			
D ↑	setup_rising to CP	0.0347			
SN ↓	min_pulse_width to SN	0.0593			
SN ↑	recovery_rising to CP	0.0081			
SN ↑	removal_rising to CP	0.0362			
TE ↓	hold_rising to CP	-0.0169			
TE ↑	hold_rising to CP	-0.0261			
TE ↓	setup_rising to CP	0.0713			
TE ↑	setup_rising to CP	0.1421			
TI ↓	hold_rising to CP	-0.0781			
TI ↑	hold_rising to CP	-0.0257			
TI ↓	setup_rising to CP	0.1384			
TI ↑	setup_rising to CP	0.0613			

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	9.249e-05	1.000e-20
X8_P4	1.116e-04	1.000e-20
X17_P4	1.552e-04	1.000e-20
X25_P4	1.772e-04	1.000e-20
X33_P4	1.992e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	6.894e-03	7.054e-03	7.101e-03	7.125e-03
Clock 100Mhz Data 25Mhz	6.934e-03	7.085e-03	7.788e-03	8.146e-03
Clock 100Mhz Data 50Mhz	6.974e-03	7.115e-03	8.475e-03	9.168e-03
Clock = 0 Data 100Mhz	4.087e-03	3.826e-03	3.738e-03	3.694e-03
Clock = 1 Data 100Mhz	1.088e-03	5.628e-04	3.877e-04	3.001e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	7.139e-03			

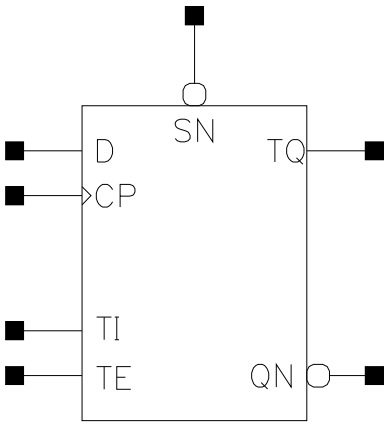
Clock 100Mhz Data 25Mhz	8.481e-03			
Clock 100Mhz Data 50Mhz	9.823e-03			
Clock = 0 Data 100Mhz	3.668e-03			
Clock = 1 Data 100Mhz	2.476e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.216	5.0592
X8_P4	1.200	4.080	4.8960
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004

SN	0.0014	0.0015	0.0015	0.0015
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0912	0.0739	4.1699	2.1216
CP to QN ↑	0.1093	0.0578	6.6461	3.2963
CP to TQ ↓	0.0788	0.0394	6.0034	5.1207
CP to TQ ↑	0.0706	0.0558	9.2642	9.0182
SN to QN ↓	0.0600	0.0565	4.1592	2.1197
SN to TQ ↑	0.0421	0.0400	9.0972	8.9893
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0728	0.0805	1.1112	0.5640
CP to QN ↑	0.0637	0.0709	1.6447	0.8362
CP to TQ ↓	0.0483	0.0482	5.2753	5.2856
CP to TQ ↑	0.0627	0.0627	9.1101	9.1292
SN to QN ↓	0.0630	0.0707	1.1107	0.5638
SN to TQ ↑	0.0527	0.0526	9.0956	9.1176

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1145	0.1164	0.1164	0.1164
CP ↑	min_pulse_width to CP	0.0739	0.0317	0.0376	0.0410
D ↓	hold_rising to CP	-0.0653	-0.0218	-0.0191	-0.0191
D ↑	hold_rising to CP	-0.0337	-0.0045	-0.0045	-0.0045
D ↓	setup_rising to CP	0.1095	0.0710	0.0710	0.0710
D ↑	setup_rising to CP	0.0633	0.0347	0.0347	0.0347
SN ↓	min_pulse_width to SN	0.0425	0.0425	0.0452	0.0479
SN ↑	recovery_rising to CP	0.0080	0.0081	0.0081	0.0080
SN ↑	removal_rising to CP	0.0260	0.0362	0.0362	0.0362
TE ↓	hold_rising to CP	-0.0484	-0.0169	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0425	-0.0261	-0.0235	-0.0235
TE ↓	setup_rising to CP	0.0928	0.0686	0.0713	0.0713
TE ↑	setup_rising to CP	0.1785	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.1344	-0.0779	-0.0779	-0.0781
TI ↑	hold_rising to CP	-0.0481	-0.0257	-0.0264	-0.0264
TI ↓	setup_rising to CP	0.1836	0.1384	0.1384	0.1384
TI ↑	setup_rising to CP	0.0833	0.0570	0.0613	0.0613

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.050e-04	1.000e-20
X8_P4	1.238e-04	1.000e-20
X17_P4	1.674e-04	1.000e-20
X33_P4	2.114e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

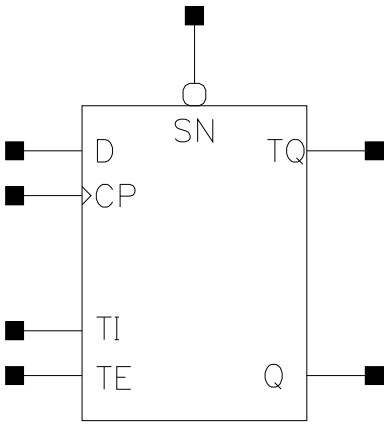
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	6.901e-03	7.053e-03	7.103e-03	7.129e-03
Clock 100Mhz Data 25Mhz	7.269e-03	7.291e-03	7.931e-03	8.648e-03
Clock 100Mhz Data 50Mhz	7.638e-03	7.529e-03	8.758e-03	1.017e-02
Clock = 0 Data 100Mhz	4.096e-03	3.832e-03	3.744e-03	3.700e-03
Clock = 1 Data 100Mhz	1.088e-03	5.626e-04	3.875e-04	3.000e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.944	4.7328
X17_P4	1.200	4.216	5.0592
X33_P4	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004

SN	0.0014	0.0013	0.0013	0.0013
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0935	0.0476	5.1191	2.2484
CP to Q ↑	0.0752	0.0610	7.0251	3.3496
CP to TQ ↓	0.0928	0.0484	7.5986	5.8225
CP to TQ ↑	0.0741	0.0680	9.3322	12.9630
SN to Q ↑	0.0448	0.0634	6.8165	3.3522
SN to TQ ↑	0.0440	0.0715	9.1195	12.9305
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0646	0.0709	1.1078	0.5758
CP to Q ↑	0.0839	0.0887	1.6410	0.8337
CP to TQ ↓	0.0668	0.0748	5.6014	5.6706
CP to TQ ↑	0.0896	0.0977	12.6332	12.6783
SN to Q ↑	0.0849	0.0897	1.6407	0.8340
SN to TQ ↑	0.0906	0.0986	12.6259	12.6829

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1145	0.1157	0.1157	0.1157
CP ↑	min_pulse_width to CP	0.0834	0.0364	0.0317	0.0317
D ↓	hold_rising to CP	-0.0653	-0.0191	-0.0218	-0.0218
D ↑	hold_rising to CP	-0.0337	-0.0045	-0.0045	-0.0045
D ↓	setup_rising to CP	0.1095	0.0710	0.0710	0.0710
D ↑	setup_rising to CP	0.0633	0.0347	0.0347	0.0347
SN ↓	min_pulse_width to SN	0.0425	0.0620	0.0544	0.0544
SN ↑	recovery_rising to CP	0.0080	0.0081	0.0081	0.0081
SN ↑	removal_rising to CP	0.0260	0.0362	0.0362	0.0362
TE ↓	hold_rising to CP	-0.0484	-0.0169	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0425	-0.0261	-0.0261	-0.0261
TE ↓	setup_rising to CP	0.0928	0.0686	0.0686	0.0686
TE ↑	setup_rising to CP	0.1785	0.1421	0.1421	0.1421
TI ↓	hold_rising to CP	-0.1344	-0.0781	-0.0779	-0.0779
TI ↑	hold_rising to CP	-0.0481	-0.0257	-0.0257	-0.0257
TI ↓	setup_rising to CP	0.1836	0.1384	0.1384	0.1384
TI ↑	setup_rising to CP	0.0833	0.0570	0.0570	0.0570

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	1.028e-04	1.000e-20
X8_P4	1.142e-04	1.000e-20
X17_P4	1.561e-04	1.000e-20
X33_P4	1.918e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

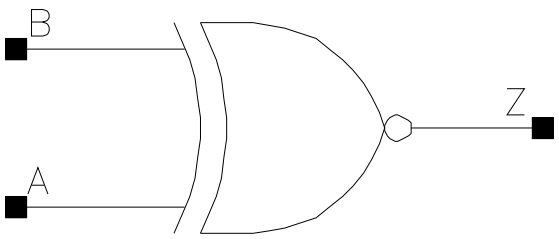
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	6.893e-03	7.044e-03	7.094e-03	7.118e-03
Clock 100Mhz Data 25Mhz	7.335e-03	7.323e-03	7.875e-03	8.600e-03
Clock 100Mhz Data 50Mhz	7.778e-03	7.601e-03	8.657e-03	1.008e-02
Clock = 0 Data 100Mhz	4.096e-03	3.828e-03	3.739e-03	3.695e-03
Clock = 1 Data 100Mhz	1.089e-03	5.629e-04	3.876e-04	3.000e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P4	X8_P4	X17_P4	X25_P4
A	0.0015	0.0006	0.0009	0.0013
B	0.0015	0.0014	0.0017	0.0023
	X33_P4			
A	0.0015			
B	0.0027			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X8_P4**	**X6_P4**	**X8_P4**
A to Z ↓	0.0210	0.0474	3.9715	2.2853
A to Z ↑	0.0218	0.0434	4.9975	3.4324
B to Z ↓	0.0199	0.0322	3.9691	2.2677
B to Z ↑	0.0224	0.0308	5.0012	3.4213
	X17_P4	**X25_P4**	**X17_P4**	**X25_P4**
A to Z ↓	0.0445	0.0448	1.1219	0.7702
A to Z ↑	0.0394	0.0395	1.6738	1.1153

B to Z ↓	0.0328	0.0318	1.1178	0.7676
B to Z ↑	0.0304	0.0293	1.6701	1.1131
	X33_P4		**X33_P4**	
A to Z ↓	0.0421		0.5780	
A to Z ↑	0.0381		0.8383	
B to Z ↓	0.0303		0.5767	
B to Z ↑	0.0288		0.8371	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P4	6.179e-05	1.000e-20
X8_P4	7.075e-05	1.000e-20
X17_P4	1.230e-04	1.000e-20
X25_P4	1.894e-04	1.000e-20
X33_P4	2.646e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	2.205e-03	4.188e-03	6.150e-03	9.670e-03
B to Z	2.165e-03	2.945e-03	4.754e-03	7.310e-03
	X33_P4			
A to Z	1.187e-02			
B to Z	9.285e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

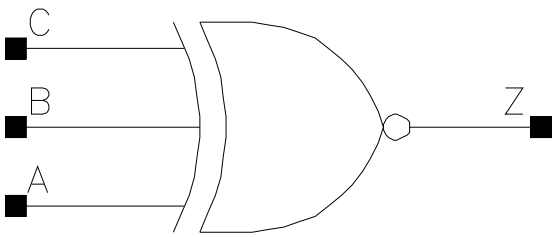
Pin Cycle (vdds)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P4			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	2.176	2.6112
X16_P4	1.200	2.720	3.2640
X25_P4	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X16_P4	X25_P4
A	0.0026	0.0022	0.0027	0.0040
B	0.0029	0.0020	0.0027	0.0037
C	0.0018	0.0006	0.0006	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0330	0.0552	4.6967	2.3995
A to Z ↑	0.0312	0.0511	7.0632	3.3992
B to Z ↓	0.0339	0.0554	4.6992	2.3998
B to Z ↑	0.0314	0.0515	7.0609	3.3999
C to Z ↓	0.0332	0.0733	4.7025	2.3996
C to Z ↑	0.0304	0.0689	7.0630	3.3996
	X16_P4	**X25_P4**	**X16_P4**	**X25_P4**
A to Z ↓	0.0551	0.0553	1.2341	0.7866
A to Z ↑	0.0550	0.0544	1.7817	1.1195
B to Z ↓	0.0555	0.0566	1.2345	0.7866

B to Z ↑	0.0553	0.0558	1.7825	1.1198
C to Z ↓	0.0770	0.0821	1.2346	0.7867
C to Z ↑	0.0759	0.0809	1.7819	1.1190

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	6.103e-05	1.000e-20
X8_P4	6.249e-05	1.000e-20
X16_P4	1.092e-04	1.000e-20
X25_P4	1.573e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	2.298e-03	3.254e-03	5.423e-03	8.285e-03
B to Z	2.344e-03	3.237e-03	5.434e-03	8.370e-03
C to Z	2.327e-03	4.842e-03	7.347e-03	1.118e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

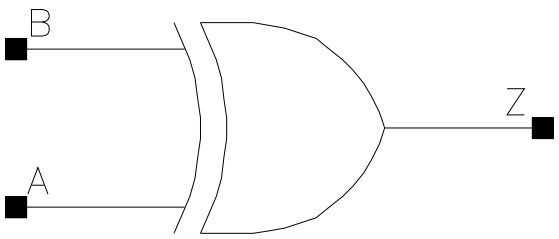
Pin Cycle (vdds)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.224	1.4688
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.224	1.4688
X16_P4	1.200	1.360	1.6320
X25_P4	1.200	2.176	2.6112
X31_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X16_P4
A	0.0007	0.0014	0.0009	0.0011
B	0.0012	0.0014	0.0014	0.0015
	X25_P4	X31_P4		
A	0.0013	0.0018		
B	0.0024	0.0031		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0422	0.0207	4.2256	3.0667
A to Z ↑	0.0405	0.0225	6.5706	6.3312
B to Z ↓	0.0300	0.0213	4.2081	3.0795
B to Z ↑	0.0305	0.0212	6.5601	6.3246
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0377	0.0392	2.2322	1.1544

A to Z ↑	0.0345	0.0364	3.3444	1.6836
B to Z ↓	0.0289	0.0298	2.2254	1.1512
B to Z ↑	0.0276	0.0291	3.3409	1.6823
	X25_P4	**X31_P4**	**X25_P4**	**X31_P4**
A to Z ↓	0.0417	0.0390	0.7636	0.6142
A to Z ↑	0.0383	0.0362	1.1118	0.8980
B to Z ↓	0.0308	0.0287	0.7629	0.6140
B to Z ↑	0.0287	0.0272	1.1131	0.8969

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	5.634e-05	1.000e-20
X6_P4	5.948e-05	1.000e-20
X8_P4	9.211e-05	1.000e-20
X16_P4	1.418e-04	1.000e-20
X25_P4	1.879e-04	1.000e-20
X31_P4	2.633e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	3.068e-03	2.175e-03	3.791e-03	5.675e-03
B to Z	2.402e-03	2.102e-03	3.184e-03	4.803e-03
	X25_P4	X31_P4		
A to Z	8.943e-03	1.094e-02		
B to Z	6.698e-03	8.193e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

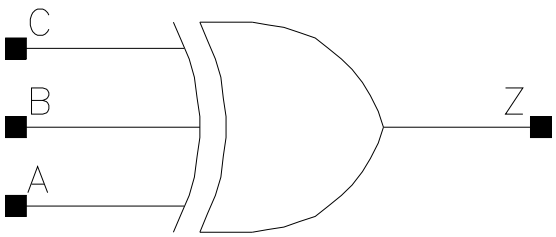
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P4	X31_P4		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X24_P4	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X24_P4
A	0.0022	0.0022	0.0027	0.0049
B	0.0022	0.0020	0.0025	0.0040
C	0.0007	0.0015	0.0021	0.0032

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0334	0.0552	4.9079	2.3974
A to Z ↑	0.0315	0.0511	7.7131	3.3979
B to Z ↓	0.0340	0.0554	4.9106	2.3991
B to Z ↑	0.0320	0.0515	7.7120	3.3966
C to Z ↓	0.0580	0.0540	4.8900	2.3988
C to Z ↑	0.0562	0.0499	7.6895	3.3973
	X17_P4	**X24_P4**	**X17_P4**	**X24_P4**
A to Z ↓	0.0500	0.0587	1.1475	0.8271
A to Z ↑	0.0501	0.0447	1.6529	1.1216
B to Z ↓	0.0502	0.0589	1.1478	0.8268

B to Z ↑	0.0504	0.0449	1.6538	1.1217
C to Z ↓	0.0494	0.0571	1.1483	0.8268
C to Z ↑	0.0495	0.0442	1.6540	1.1215

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P4	6.679e-05	1.000e-20
X8_P4	5.279e-05	1.000e-20
X17_P4	1.039e-04	1.000e-20
X24_P4	1.639e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	2.176e-03	3.254e-03	5.190e-03	8.819e-03
B to Z	2.218e-03	3.237e-03	5.192e-03	8.817e-03
C to Z	4.378e-03	3.192e-03	5.198e-03	8.821e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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