CMOS028 FDSOI MODEL FOR MICROSTRIP TRANSMISSION LINE

(microstrip_tline_6U1x_2T8x_LB)

Developer:
RF Team, October 2017

Maturity:
microstrip_tline_6U1x_2T8x_LB: Preliminary data

I Measurement and Parameter Extraction/ Estimation of Typical Model Parameters:

microstrip_tline_6U1x_2T8x_LB:
8ML is silicon based. (Q727126 Wafer 10, MPW 1722)

Test structure reference:
N/A.

Device Selection:
N/A.

Characterization domain:
N/A.

II. Best/Worst Case:

Statistical and Best/Worst case simulations are available.
Some approximations have been made for the definition of Min and Max:

Min defined with: Zc min, R max
Max defined with: Zc max, R min
FOR ANY FREQUENCY (approximation).

User corners are also available.

III. Simulation with temperature:

Available from -40 to 125 Celsius Degree.

IV. Model Application guidelines:

Layout & Model:

- Signal line: in LB
- Ground shield: in M1/M2/M3 (bar shield).
- Lateral vertical ground shields around line: in M1 to IB.
- Distributed RLCG cells model.
- 3 pins: in / out / sub.
- The model takes into account the proximity effects by the use of frequency dependent resistances.

Model Call:

- Scalable microstrip transmission line model.
- Characteristic impedance versus signal line width is given for indication only. Designer has to make the simulation with the desired width and extract the Zc more accurately. (Zc =40.55 to 73.11 Ohms)
- Ground has to be connected by the designer to the lateral walls rather than to the 1st bar of the bar shield to guarantee a better ground return.

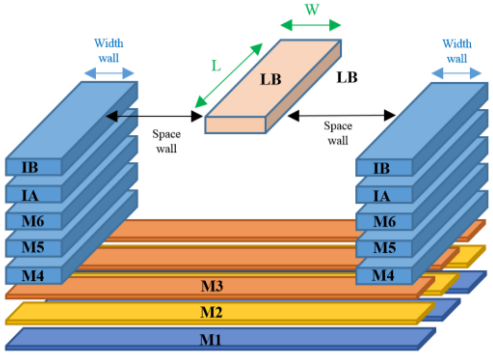
- Input parameters for **microstrip_tline** :

  l: line length
  from 5e-6 m to 1e-3 m

  w: width of signal line
  from 4e-6 m to 20e-6 m

- Default instantiation is in m.

- The structure of the microstrip line is the following:



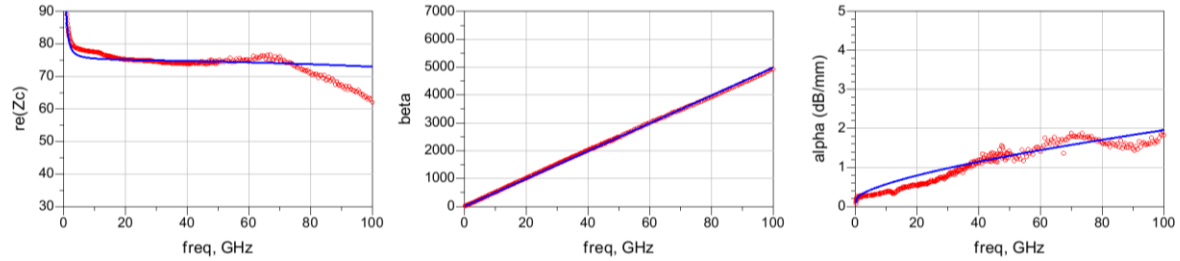
Single TL 3D View

The wall width is fixed to 5 µm, resulting of a tradeoff between size and grounding quality. It is also the best case to be equal to the mesh Pcell dimension.
The spacing between walls and line is fixed to 13.3 µm to guarantee a microstrip mode (not coplanar one), by minimizing the lateral capacitance versus the vertical one and because of density DRC check.
To build the shield, bars have the maximum width allowed by DRM (0.7 µm) and the considered spacing is 0.3 µm.

V. Model vs Simulations:

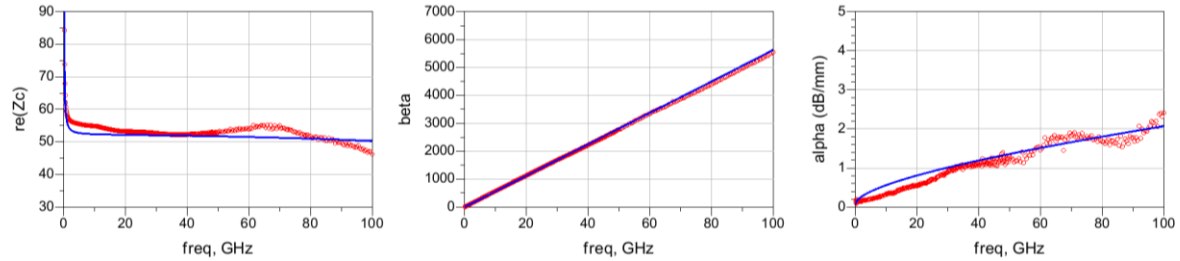
Configuration 1: w=4e-6m, l=100e-6m

Model (TYP) **Measurement**



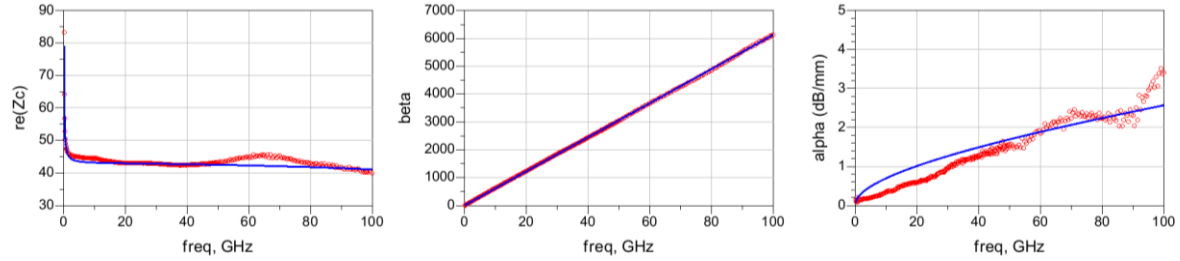
Configuration 2: w=12e-6m, l=100e-6m

Model (TYP) **Measurement**



Configuration 3: w=20e-6m, l=100e-6m

Model (TYP) **Measurement**



VI. Corner evaluation:

Example of corners evaluation for configuration 2 (w=12e-6m, l=100e-6m).

Model (MIN/TYP/MAX) **Measurement (11 dies)**