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C28SOI_SC_12_CORE_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells

Overview

- C28SOI_SC_12_CORE_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

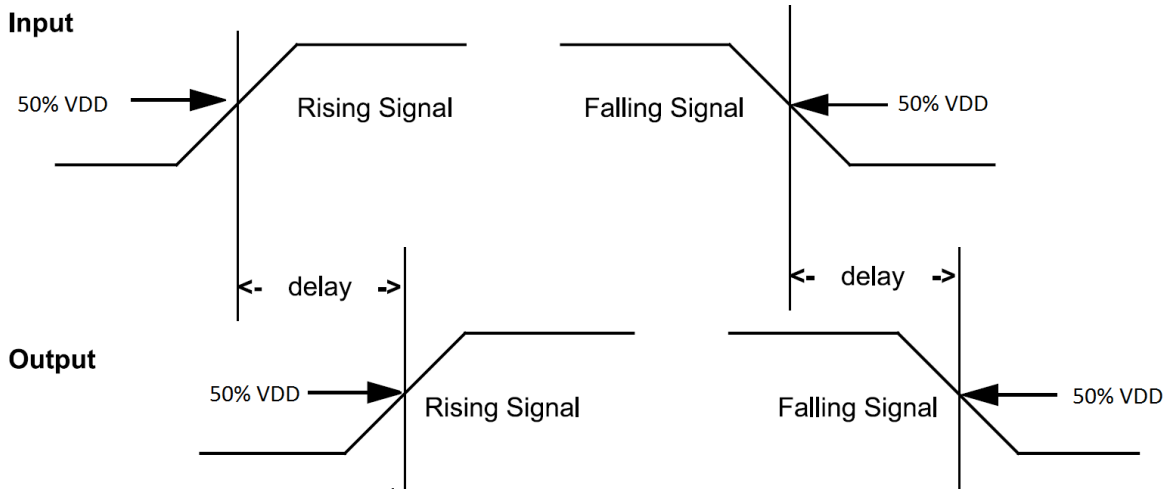


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

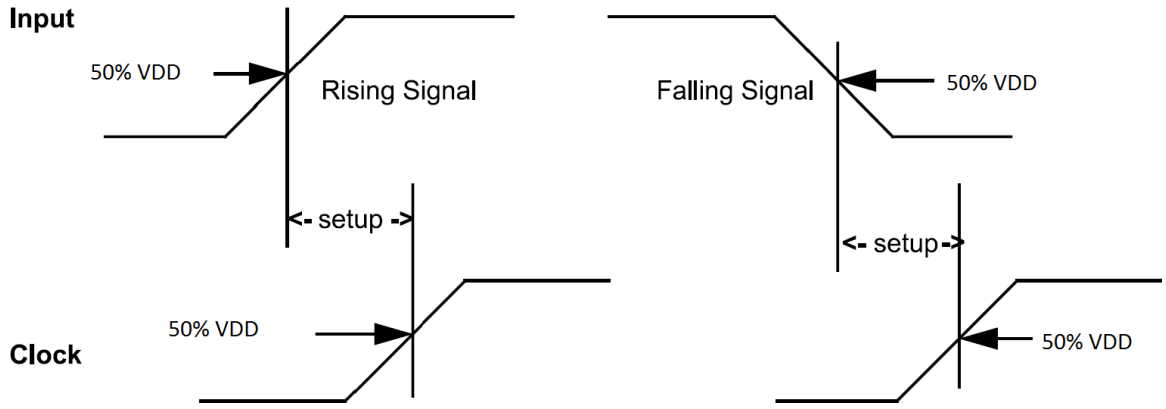


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

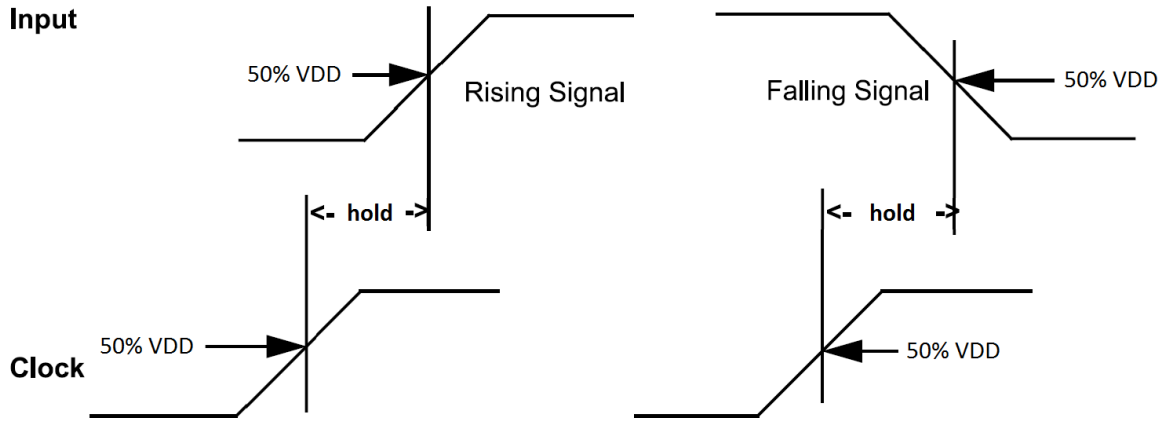


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

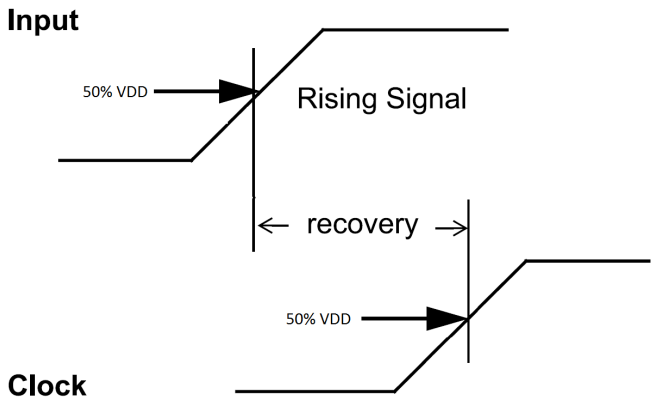


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

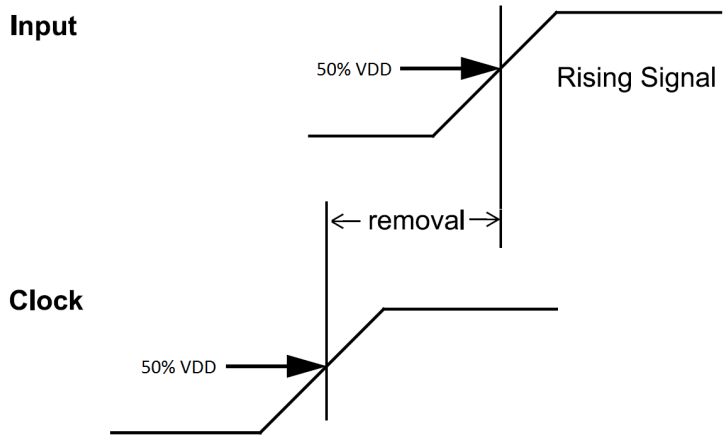


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

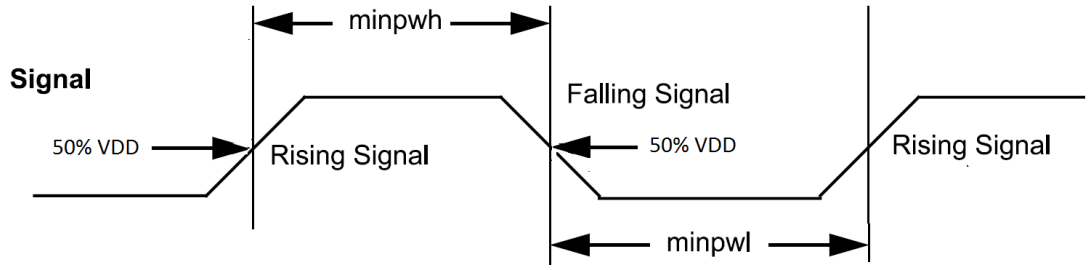


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

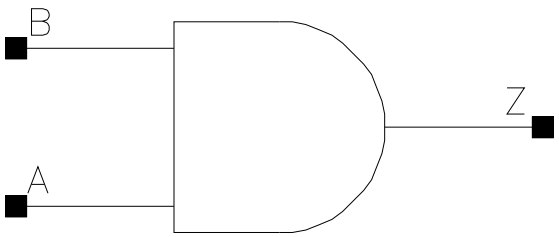
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X25_P0	1.200	1.088	1.3056
X33_P0	1.200	1.360	1.6320
X42_P0	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0008	0.0011	0.0017	0.0021
B	0.0007	0.0010	0.0016	0.0021
	X42_P0			
A	0.0021			
B	0.0021			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0180	0.0145	1.4207	0.7194
A to Z ↑	0.0144	0.0145	1.8106	0.8712
B to Z ↓	0.0169	0.0136	1.4183	0.7185
B to Z ↑	0.0160	0.0160	1.8086	0.8687
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0151	0.0145	0.4755	0.3551

A to Z ↑	0.0139	0.0146	0.5789	0.4383
B to Z ↓	0.0143	0.0130	0.4759	0.3548
B to Z ↑	0.0154	0.0159	0.5777	0.4384
	X42_P0		**X42_P0**	
A to Z ↓	0.0159		0.2876	
A to Z ↑	0.0162		0.3516	
B to Z ↓	0.0145		0.2874	
B to Z ↑	0.0175		0.3509	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	7.508e-04	1.000e-20
X16_P0	1.693e-03	1.000e-20
X25_P0	2.441e-03	1.000e-20
X33_P0	3.324e-03	1.000e-20
X42_P0	3.906e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	1.886e-05	3.554e-05	5.682e-05	1.250e-04
B (output stable)	3.018e-05	5.536e-05	8.682e-05	3.268e-04
A to Z	4.611e-03	8.433e-03	1.279e-02	1.702e-02
B to Z	4.495e-03	8.254e-03	1.249e-02	1.633e-02
	X42_P0			
A (output stable)	1.250e-04			
B (output stable)	3.250e-04			
A to Z	2.061e-02			
B to Z	1.991e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

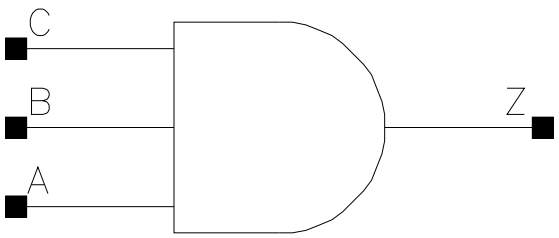
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X25_P0	1.200	1.360	1.6320
X33_P0	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0007	0.0011	0.0018	0.0022
B	0.0006	0.0011	0.0016	0.0020
C	0.0007	0.0011	0.0015	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0190	0.0158	1.4339	0.7010
A to Z ↑	0.0181	0.0183	1.8285	0.8691
B to Z ↓	0.0183	0.0150	1.4334	0.7006
B to Z ↑	0.0197	0.0198	1.8291	0.8690
C to Z ↓	0.0174	0.0140	1.4324	0.7005
C to Z ↑	0.0210	0.0208	1.8270	0.8685
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0159	0.0150	0.4810	0.3593

A to Z ↑	0.0175	0.0171	0.5982	0.4477
B to Z ↓	0.0151	0.0140	0.4808	0.3592
B to Z ↑	0.0191	0.0187	0.5973	0.4477
C to Z ↓	0.0141	0.0132	0.4809	0.3589
C to Z ↑	0.0202	0.0198	0.5973	0.4477

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	7.807e-04	1.000e-20
X17_P0	1.745e-03	1.000e-20
X25_P0	2.492e-03	1.000e-20
X33_P0	3.406e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	2.103e-05	3.933e-05	5.348e-05	7.455e-05
B (output stable)	3.023e-05	5.545e-05	8.121e-05	1.089e-04
C (output stable)	5.791e-05	1.067e-04	1.606e-04	2.223e-04
A to Z	5.027e-03	9.534e-03	1.381e-02	1.799e-02
B to Z	4.882e-03	9.280e-03	1.337e-02	1.739e-02
C to Z	4.777e-03	9.081e-03	1.303e-02	1.690e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

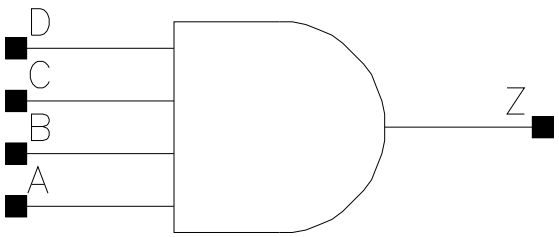
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X6_P0	1.200	1.088	1.3056
X20_P0	1.200	2.312	2.7744
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P0	X6_P0	X20_P0	X27_P0
A	0.0006	0.0008	0.0018	0.0020
B	0.0005	0.0008	0.0018	0.0021
C	0.0005	0.0008	0.0018	0.0020
D	0.0005	0.0008	0.0018	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X6_P0	X4_P0	X6_P0
A to Z ↓	0.0193	0.0176	2.6365	1.7336
A to Z ↑	0.0180	0.0139	5.8287	3.1976
B to Z ↓	0.0185	0.0164	2.6383	1.7326
B to Z ↑	0.0198	0.0152	5.8262	3.1951
C to Z ↓	0.0200	0.0190	2.6025	1.7358
C to Z ↑	0.0187	0.0147	5.8275	3.1983

D to Z ↓	0.0193	0.0176	2.6029	1.7353
D to Z ↑	0.0210	0.0161	5.8281	3.1958
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0170	0.0154	0.5078	0.3596
A to Z ↑	0.0146	0.0175	1.0798	0.8281
B to Z ↓	0.0154	0.0138	0.5068	0.3592
B to Z ↑	0.0158	0.0189	1.0790	0.8278
C to Z ↓	0.0167	0.0149	0.5098	0.3599
C to Z ↑	0.0139	0.0164	1.0778	0.8257
D to Z ↓	0.0150	0.0135	0.5085	0.3594
D to Z ↑	0.0150	0.0177	1.0767	0.8251

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	3.122e-04	1.000e-20
X6_P0	7.879e-04	1.000e-20
X20_P0	2.482e-03	1.000e-20
X27_P0	3.310e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	6.964e-04	1.199e-03	3.452e-03	4.189e-03
B (output stable)	6.548e-04	1.124e-03	3.261e-03	3.967e-03
C (output stable)	6.794e-04	1.221e-03	3.179e-03	3.873e-03
D (output stable)	6.432e-04	1.144e-03	2.975e-03	3.668e-03
A to Z	2.856e-03	4.640e-03	1.392e-02	1.807e-02
B to Z	2.762e-03	4.470e-03	1.321e-02	1.729e-02
C to Z	2.913e-03	4.875e-03	1.297e-02	1.657e-02
D to Z	2.821e-03	4.691e-03	1.223e-02	1.585e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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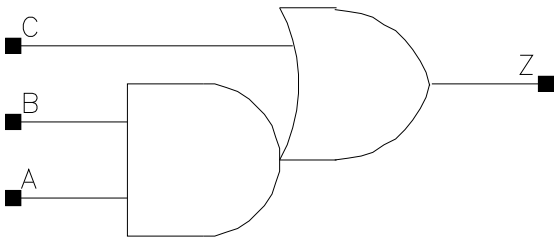
AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0007	0.0010	0.0021
B	0.0007	0.0011	0.0020
C	0.0008	0.0011	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0227	0.0207	1.4458	0.7074
A to Z ↑	0.0146	0.0137	1.7484	0.8608
B to Z ↓	0.0209	0.0189	1.4420	0.7053
B to Z ↑	0.0164	0.0155	1.7437	0.8598
C to Z ↓	0.0206	0.0186	1.4408	0.7061
C to Z ↑	0.0140	0.0137	1.7317	0.8541
	X33_P0		**X33_P0**	
A to Z ↓	0.0206		0.3602	
A to Z ↑	0.0141		0.4353	

B to Z ↓	0.0193		0.3595	
B to Z ↑	0.0157		0.4342	
C to Z ↓	0.0189		0.3593	
C to Z ↑	0.0137		0.4320	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	6.061e-04	1.000e-20
X17_P0	1.349e-03	1.000e-20
X33_P0	2.633e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	5.824e-05	8.856e-05	2.042e-04
B (output stable)	6.326e-05	1.014e-04	2.509e-04
C (output stable)	8.000e-05	1.458e-04	3.149e-04
A to Z	4.840e-03	9.053e-03	1.800e-02
B to Z	4.690e-03	8.770e-03	1.741e-02
C to Z	5.016e-03	9.335e-03	1.874e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

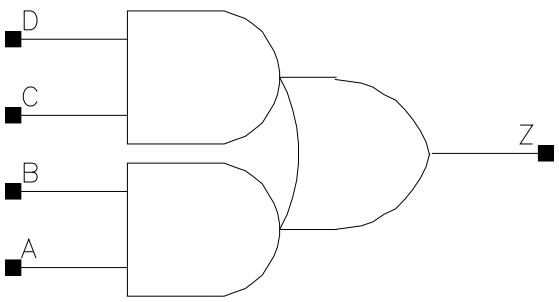
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0010	0.0020
B	0.0007	0.0011	0.0019
C	0.0006	0.0010	0.0021
D	0.0007	0.0011	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0237	0.0211	1.3995	0.7077
A to Z ↑	0.0193	0.0186	1.7255	0.8614
B to Z ↓	0.0219	0.0194	1.3946	0.7058
B to Z ↑	0.0211	0.0207	1.7234	0.8599

C to Z ↓	0.0232	0.0211	1.3942	0.7056
C to Z ↑	0.0164	0.0159	1.7178	0.8583
D to Z ↓	0.0220	0.0199	1.3919	0.7048
D to Z ↑	0.0184	0.0176	1.7178	0.8571
	X33_P0		**X33_P0**	
A to Z ↓	0.0198		0.3605	
A to Z ↑	0.0169		0.4363	
B to Z ↓	0.0187		0.3602	
B to Z ↑	0.0187		0.4358	
C to Z ↓	0.0199		0.3599	
C to Z ↑	0.0143		0.4353	
D to Z ↓	0.0188		0.3594	
D to Z ↑	0.0159		0.4345	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	7.892e-04	1.000e-20
X17_P0	1.694e-03	1.000e-20
X33_P0	3.336e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	4.819e-05	6.886e-05	1.045e-04
B (output stable)	1.380e-04	1.790e-04	1.241e-04
C (output stable)	5.266e-05	8.172e-05	1.944e-04
D (output stable)	5.781e-05	9.366e-05	2.234e-04
A to Z	5.924e-03	1.078e-02	1.994e-02
B to Z	5.650e-03	1.041e-02	1.950e-02
C to Z	5.397e-03	9.863e-03	1.812e-02
D to Z	5.271e-03	9.633e-03	1.766e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

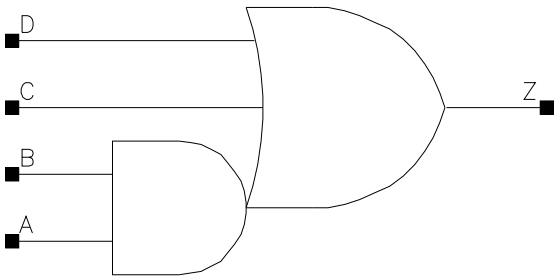
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	0.952	1.1424
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0007	0.0011	0.0020
B	0.0007	0.0010	0.0020
C	0.0007	0.0010	0.0020
D	0.0007	0.0011	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0292	0.0262	1.4869	0.7390
A to Z ↑	0.0156	0.0150	1.7374	0.9024
B to Z ↓	0.0281	0.0247	1.4854	0.7374
B to Z ↑	0.0174	0.0164	1.7378	0.9012
C to Z ↓	0.0271	0.0239	1.4846	0.7373
C to Z ↑	0.0151	0.0145	1.7224	0.8951

D to Z ↓	0.0282	0.0253	1.4846	0.7375
D to Z ↑	0.0147	0.0144	1.7209	0.8960
	X33_P0		**X33_P0**	
A to Z ↓	0.0271		0.3702	
A to Z ↑	0.0150		0.4354	
B to Z ↓	0.0246		0.3685	
B to Z ↑	0.0162		0.4357	
C to Z ↓	0.0250		0.3689	
C to Z ↑	0.0145		0.4326	
D to Z ↓	0.0259		0.3690	
D to Z ↑	0.0138		0.4320	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	4.552e-04	1.000e-20
X17_P0	1.024e-03	1.000e-20
X33_P0	2.004e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	7.282e-05	1.265e-04	2.954e-04
B (output stable)	7.283e-05	1.222e-04	3.272e-04
C (output stable)	4.164e-05	8.139e-05	2.085e-04
D (output stable)	5.044e-05	9.373e-05	3.098e-04
A to Z	5.433e-03	9.821e-03	2.007e-02
B to Z	5.312e-03	9.576e-03	1.914e-02
C to Z	5.747e-03	1.037e-02	2.139e-02
D to Z	5.556e-03	1.007e-02	2.047e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

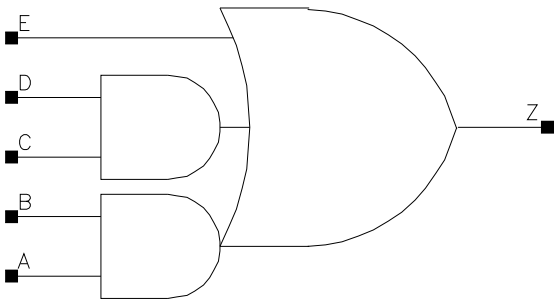
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.088	1.3056
X17_P0	1.200	1.224	1.4688
X33_P0	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0010	0.0020
B	0.0007	0.0010	0.0019
C	0.0008	0.0013	0.0021
D	0.0007	0.0010	0.0020
E	0.0007	0.0010	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0310	0.0272	1.4192	0.7203
A to Z ↑	0.0204	0.0182	1.7048	0.8628

B to Z ↓	0.0299	0.0260	1.4163	0.7192
B to Z ↑	0.0227	0.0202	1.7018	0.8626
C to Z ↓	0.0302	0.0277	1.4155	0.7189
C to Z ↑	0.0168	0.0151	1.6914	0.8588
D to Z ↓	0.0281	0.0253	1.4095	0.7156
D to Z ↑	0.0186	0.0167	1.6887	0.8579
E to Z ↓	0.0291	0.0260	1.4103	0.7166
E to Z ↑	0.0160	0.0143	1.6745	0.8514
	X33_P0		**X33_P0**	
A to Z ↓	0.0268		0.3702	
A to Z ↑	0.0190		0.4374	
B to Z ↓	0.0252		0.3694	
B to Z ↑	0.0210		0.4369	
C to Z ↓	0.0267		0.3692	
C to Z ↑	0.0152		0.4344	
D to Z ↓	0.0248		0.3680	
D to Z ↑	0.0169		0.4339	
E to Z ↓	0.0255		0.3684	
E to Z ↑	0.0146		0.4313	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	5.975e-04	1.000e-20
X17_P0	1.302e-03	1.000e-20
X33_P0	2.518e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	2.595e-05	4.322e-05	9.488e-05
B (output stable)	3.098e-05	4.764e-05	1.157e-04
C (output stable)	8.302e-05	1.118e-04	2.791e-04
D (output stable)	9.776e-05	1.348e-04	3.090e-04
E (output stable)	1.347e-04	1.816e-04	4.169e-04
A to Z	6.792e-03	1.182e-02	2.331e-02
B to Z	6.669e-03	1.159e-02	2.266e-02
C to Z	5.895e-03	1.045e-02	2.032e-02
D to Z	5.715e-03	1.011e-02	1.960e-02
E to Z	6.048e-03	1.066e-02	2.082e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

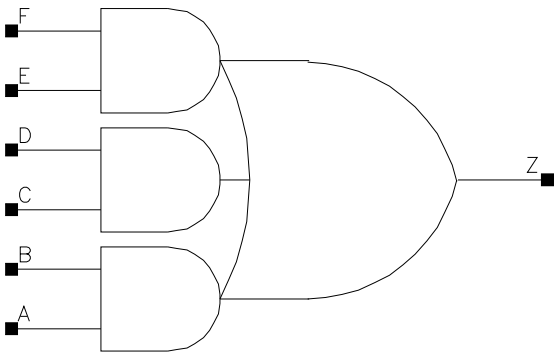
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.360	1.6320
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
A	0.0006	0.0007	0.0010	0.0020

B	0.0007	0.0008	0.0013	0.0019
C	0.0006	0.0007	0.0010	0.0020
D	0.0007	0.0008	0.0010	0.0019
E	0.0007	0.0008	0.0010	0.0021
F	0.0007	0.0008	0.0010	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0309	0.0298	2.7044	1.4353
A to Z ↑	0.0214	0.0212	3.3106	1.7532
B to Z ↓	0.0282	0.0274	2.6878	1.4277
B to Z ↑	0.0231	0.0231	3.3067	1.7507
C to Z ↓	0.0293	0.0286	2.6959	1.4313
C to Z ↑	0.0193	0.0191	3.2878	1.7419
D to Z ↓	0.0279	0.0273	2.6884	1.4276
D to Z ↑	0.0214	0.0212	3.2858	1.7405
E to Z ↓	0.0270	0.0270	2.6845	1.4264
E to Z ↑	0.0157	0.0158	3.2732	1.7337
F to Z ↓	0.0254	0.0253	2.6768	1.4221
F to Z ↑	0.0175	0.0176	3.2703	1.7338
	X17_P0	X33_P0	X17_P0	X33_P0
A to Z ↓	0.0288	0.0277	0.7237	0.3686
A to Z ↑	0.0202	0.0204	0.8670	0.4397
B to Z ↓	0.0270	0.0262	0.7199	0.3680
B to Z ↑	0.0225	0.0224	0.8660	0.4389
C to Z ↓	0.0283	0.0273	0.7219	0.3684
C to Z ↑	0.0183	0.0187	0.8620	0.4370
D to Z ↓	0.0267	0.0260	0.7197	0.3677
D to Z ↑	0.0204	0.0206	0.8616	0.4364
E to Z ↓	0.0266	0.0267	0.7192	0.3674
E to Z ↑	0.0152	0.0159	0.8593	0.4358
F to Z ↓	0.0249	0.0248	0.7171	0.3662
F to Z ↑	0.0169	0.0179	0.8585	0.4353

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	4.962e-04	1.000e-20
X8_P0	8.893e-04	1.000e-20
X17_P0	1.636e-03	1.000e-20
X33_P0	3.158e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	5.005e-05	5.868e-05	7.596e-05	1.358e-04
B (output stable)	1.110e-04	1.261e-04	1.340e-04	1.778e-04
C (output stable)	5.197e-05	6.202e-05	7.904e-05	1.783e-04
D (output stable)	5.737e-05	6.998e-05	8.824e-05	2.298e-04
E (output stable)	1.398e-04	1.687e-04	2.087e-04	3.514e-04
F (output stable)	1.413e-04	1.678e-04	2.183e-04	3.913e-04

A to Z	5.241e-03	7.651e-03	1.279e-02	2.445e-02
B to Z	4.915e-03	7.270e-03	1.225e-02	2.381e-02
C to Z	4.679e-03	6.947e-03	1.179e-02	2.260e-02
D to Z	4.526e-03	6.758e-03	1.152e-02	2.200e-02
E to Z	4.107e-03	6.241e-03	1.068e-02	2.091e-02
F to Z	3.956e-03	6.049e-03	1.039e-02	2.023e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

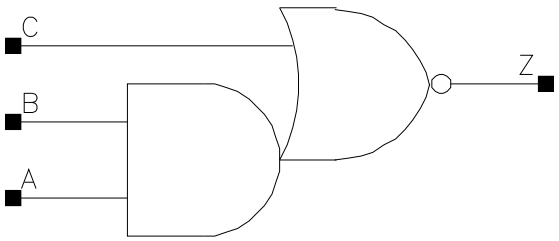
Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008
X44_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X33_P0	X44_P0
A	0.0008	0.0025	0.0051	0.0069
B	0.0008	0.0024	0.0048	0.0066
C	0.0009	0.0027	0.0053	0.0070

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0051	0.0051	2.4104	0.8166
A to Z ↑	0.0110	0.0112	3.2845	1.1109
B to Z ↓	0.0061	0.0062	2.4333	0.8273
B to Z ↑	0.0088	0.0086	3.2173	1.1110
C to Z ↓	0.0056	0.0058	1.4926	0.5118
C to Z ↑	0.0096	0.0095	2.9939	1.0248
	X33_P0	**X44_P0**	**X33_P0**	**X44_P0**
A to Z ↓	0.0053	0.0053	0.4172	0.3171

A to Z ↑	0.0112	0.0112	0.5581	0.4257
B to Z ↓	0.0064	0.0064	0.4226	0.3213
B to Z ↑	0.0087	0.0087	0.5562	0.4224
C to Z ↓	0.0075	0.0075	0.3032	0.2351
C to Z ↑	0.0092	0.0091	0.5147	0.3917

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P0	5.631e-04	1.000e-20
X17_P0	1.641e-03	1.000e-20
X33_P0	3.186e-03	1.000e-20
X44_P0	4.239e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	8.948e-05	2.613e-04	5.905e-04	7.355e-04
B (output stable)	9.642e-05	3.241e-04	7.236e-04	8.810e-04
C (output stable)	1.390e-04	4.210e-04	9.015e-04	1.152e-03
A to Z	2.865e-03	8.702e-03	1.734e-02	2.286e-02
B to Z	2.670e-03	7.717e-03	1.554e-02	2.048e-02
C to Z	3.563e-03	1.049e-02	2.027e-02	2.662e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

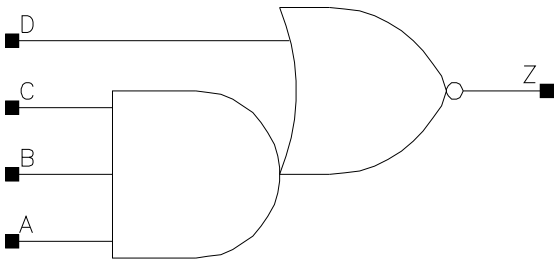
Pin Cycle (vdds)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X29_P0	1.200	3.536	4.2432
X38_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X29_P0	X38_P0
A	0.0009	0.0052	0.0069
B	0.0008	0.0050	0.0065
C	0.0008	0.0048	0.0064
D	0.0009	0.0054	0.0066

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X29_P0	X5_P0	X29_P0
A to Z ↓	0.0083	0.0086	3.3025	0.5771
A to Z ↑	0.0133	0.0133	3.2745	0.5492
B to Z ↓	0.0096	0.0096	3.3171	0.5807
B to Z ↑	0.0118	0.0117	3.2782	0.5544
C to Z ↓	0.0101	0.0101	3.3309	0.5837
C to Z ↑	0.0099	0.0095	3.2210	0.5595
D to Z ↓	0.0073	0.0092	1.5230	0.3050

D to Z ↑	0.0112	0.0107	2.8068	0.4793
	X38_P0		**X38_P0**	
A to Z ↓	0.0083		0.4490	
A to Z ↑	0.0129		0.4152	
B to Z ↓	0.0094		0.4520	
B to Z ↑	0.0112		0.4206	
C to Z ↓	0.0099		0.4545	
C to Z ↑	0.0091		0.4265	
D to Z ↓	0.0101		0.2542	
D to Z ↑	0.0102		0.3636	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	5.517e-04	1.000e-20
X29_P0	3.096e-03	1.000e-20
X38_P0	4.068e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X29_P0	X38_P0
A (output stable)	5.264e-05	4.369e-04	5.599e-04
B (output stable)	6.131e-05	4.897e-04	6.344e-04
C (output stable)	8.189e-05	7.402e-04	9.455e-04
D (output stable)	1.797e-04	1.285e-03	1.684e-03
A to Z	3.254e-03	1.970e-02	2.531e-02
B to Z	2.991e-03	1.760e-02	2.252e-02
C to Z	2.781e-03	1.582e-02	2.019e-02
D to Z	4.032e-03	2.312e-02	2.949e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

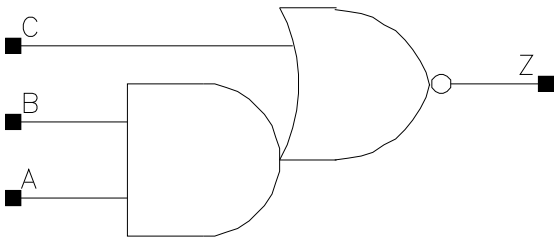
Pin Cycle (vdds)	X5_P0	X29_P0	X38_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X11_P0	1.200	1.088	1.3056
X16_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X11_P0	X16_P0	X23_P0
A	0.0009	0.0018	0.0027	0.0036
B	0.0009	0.0017	0.0026	0.0034
C	0.0009	0.0017	0.0025	0.0036
	X46_P0			
A	0.0070			
B	0.0067			
C	0.0070			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X11_P0	X6_P0	X11_P0
A to Z ↓	0.0067	0.0072	2.3227	1.1863
A to Z ↑	0.0101	0.0104	3.2752	1.6064
B to Z ↓	0.0081	0.0084	2.3434	1.1975

B to Z ↑	0.0083	0.0082	3.2254	1.6145
C to Z ↓	0.0032	0.0041	1.5396	0.9011
C to Z ↑	0.0094	0.0088	3.0186	1.4962
	X16_P0	**X23_P0**	**X16_P0**	**X23_P0**
A to Z ↓	0.0068	0.0070	0.8148	0.6152
A to Z ↑	0.0097	0.0100	1.0833	0.8236
B to Z ↓	0.0083	0.0083	0.8243	0.6216
B to Z ↑	0.0074	0.0077	1.0841	0.8285
C to Z ↓	0.0042	0.0031	0.6232	0.3955
C to Z ↑	0.0083	0.0092	1.0095	0.7662
	X46_P0		**X46_P0**	
A to Z ↓	0.0067		0.3160	
A to Z ↑	0.0097		0.4324	
B to Z ↓	0.0081		0.3196	
B to Z ↑	0.0073		0.4312	
C to Z ↓	0.0034		0.2021	
C to Z ↑	0.0094		0.4013	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P0	5.637e-04	1.000e-20
X11_P0	1.148e-03	1.000e-20
X16_P0	1.661e-03	1.000e-20
X23_P0	2.241e-03	1.000e-20
X46_P0	4.387e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	3.696e-05	9.957e-05	1.251e-04	1.882e-04
B (output stable)	4.340e-05	1.613e-04	1.748e-04	2.742e-04
C (output stable)	2.896e-04	7.389e-04	8.034e-04	1.174e-03
A to Z	3.352e-03	6.905e-03	9.883e-03	1.324e-02
B to Z	3.098e-03	6.267e-03	8.864e-03	1.193e-02
C to Z	2.925e-03	5.801e-03	8.246e-03	1.169e-02
	X46_P0			
A (output stable)	3.317e-04			
B (output stable)	4.695e-04			
C (output stable)	1.921e-03			
A to Z	2.547e-02			
B to Z	2.287e-02			
C to Z	2.253e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

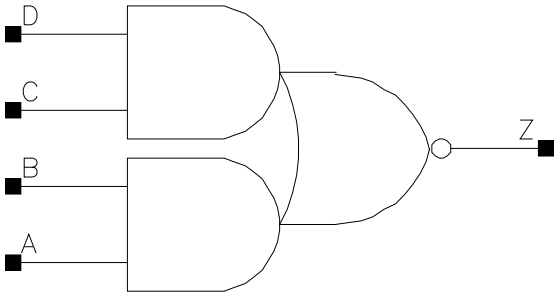
	X46_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P0	X10_P0	X16_P0	X21_P0
A	0.0007	0.0019	0.0027	0.0035
B	0.0007	0.0017	0.0026	0.0034
C	0.0007	0.0018	0.0026	0.0035
D	0.0007	0.0016	0.0025	0.0033
	X42_P0			
A	0.0071			
B	0.0068			
C	0.0069			
D	0.0067			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X10_P0**	**X4_P0**	**X10_P0**
A to Z ↓	0.0075	0.0079	2.8664	1.1355
A to Z ↑	0.0133	0.0110	4.4369	1.4825
B to Z ↓	0.0090	0.0096	2.8975	1.1489
B to Z ↑	0.0116	0.0097	4.4196	1.5300
C to Z ↓	0.0049	0.0051	2.9425	1.1450
C to Z ↑	0.0127	0.0108	4.4323	1.4932
D to Z ↓	0.0060	0.0064	2.9812	1.1613
D to Z ↑	0.0108	0.0092	4.4137	1.5233
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0087	0.0086	0.8170	0.6169
A to Z ↑	0.0113	0.0114	1.0057	0.7834
B to Z ↓	0.0104	0.0101	0.8255	0.6231
B to Z ↑	0.0093	0.0094	1.0069	0.7853
C to Z ↓	0.0055	0.0057	0.8183	0.6186
C to Z ↑	0.0110	0.0114	1.0067	0.7837
D to Z ↓	0.0069	0.0068	0.8291	0.6262
D to Z ↑	0.0087	0.0091	1.0088	0.7850
	X42_P0		**X42_P0**	
A to Z ↓	0.0093		0.3211	
A to Z ↑	0.0117		0.3947	
B to Z ↓	0.0106		0.3245	
B to Z ↑	0.0094		0.3929	
C to Z ↓	0.0063		0.3184	
C to Z ↑	0.0117		0.3956	
D to Z ↓	0.0074		0.3225	
D to Z ↑	0.0093		0.3939	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	4.050e-04	1.000e-20
X10_P0	1.362e-03	1.000e-20
X16_P0	1.938e-03	1.000e-20
X21_P0	2.574e-03	1.000e-20
X42_P0	5.058e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	3.931e-05	9.740e-05	1.775e-04	2.429e-04
B (output stable)	4.763e-05	1.207e-04	2.886e-04	4.154e-04
C (output stable)	8.476e-05	1.846e-04	3.223e-04	4.105e-04
D (output stable)	9.590e-05	2.163e-04	4.316e-04	5.827e-04
A to Z	2.855e-03	7.610e-03	1.136e-02	1.478e-02
B to Z	2.634e-03	6.972e-03	1.027e-02	1.348e-02
C to Z	2.295e-03	6.278e-03	9.234e-03	1.226e-02
D to Z	2.096e-03	5.691e-03	8.246e-03	1.102e-02
	X42_P0			
A (output stable)	4.674e-04			
B (output stable)	7.483e-04			
C (output stable)	7.928e-04			
D (output stable)	1.075e-03			

A to Z	2.933e-02			
B to Z	2.664e-02			
C to Z	2.423e-02			
D to Z	2.183e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

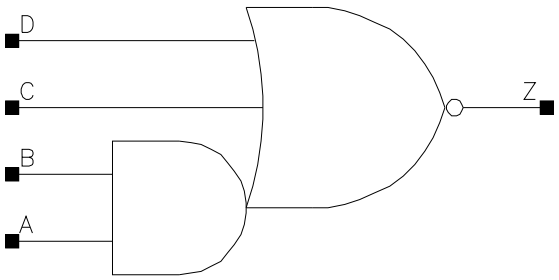
Pin Cycle (vdds)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X35_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P0	X35_P0
A	0.0008	0.0066
B	0.0009	0.0063
C	0.0009	0.0063
D	0.0009	0.0059

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X35_P0	X5_P0	X35_P0
A to Z ↓	0.0059	0.0063	2.4358	0.3612
A to Z ↑	0.0149	0.0140	4.7277	0.6174
B to Z ↓	0.0070	0.0075	2.4659	0.3666
B to Z ↑	0.0126	0.0113	4.6798	0.6163
C to Z ↓	0.0069	0.0109	1.5904	0.3028
C to Z ↑	0.0133	0.0118	4.4567	0.5858
D to Z ↓	0.0065	0.0097	1.6052	0.3031

D to Z ↑	0.0142	0.0125	4.4724	0.5883

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	4.613e-04	1.000e-20
X35_P0	3.469e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X35_P0
A (output stable)	1.196e-04	9.596e-04
B (output stable)	1.199e-04	1.019e-03
C (output stable)	7.731e-05	7.605e-04
D (output stable)	9.070e-05	9.735e-04
A to Z	2.884e-03	2.107e-02
B to Z	2.641e-03	1.882e-02
C to Z	3.787e-03	2.695e-02
D to Z	3.397e-03	2.366e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X5_P0	X35_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

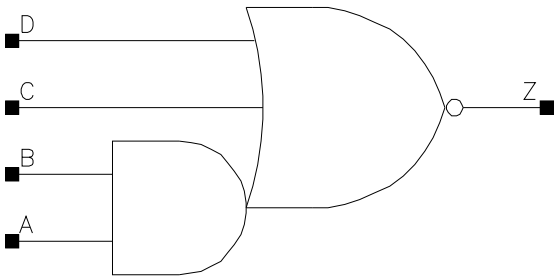
life.augmented

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X17_P0	1.200	2.448	2.9376
X34_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P0	X17_P0	X34_P0
A	0.0009	0.0035	0.0070
B	0.0008	0.0034	0.0068
C	0.0008	0.0030	0.0060
D	0.0008	0.0029	0.0056

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X17_P0	X4_P0	X17_P0
A to Z ↓	0.0077	0.0085	2.6275	0.6935
A to Z ↑	0.0126	0.0129	4.7624	1.1836
B to Z ↓	0.0094	0.0100	2.6543	0.7001
B to Z ↑	0.0108	0.0105	4.6969	1.1861
C to Z ↓	0.0080	0.0079	2.4875	0.6030
C to Z ↑	0.0103	0.0104	4.5045	1.1292

D to Z ↓	0.0063	0.0056	2.5355	0.6069
D to Z ↑	0.0107	0.0101	4.5231	1.1311
	X34_P0		**X34_P0**	
A to Z ↓	0.0084		0.3562	
A to Z ↑	0.0127		0.6076	
B to Z ↓	0.0100		0.3599	
B to Z ↑	0.0102		0.6048	
C to Z ↓	0.0084		0.3218	
C to Z ↑	0.0099		0.5784	
D to Z ↓	0.0062		0.3246	
D to Z ↑	0.0098		0.5797	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	4.579e-04	1.000e-20
X17_P0	1.816e-03	1.000e-20
X34_P0	3.568e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X17_P0	X34_P0
A (output stable)	3.220e-05	1.569e-04	3.041e-04
B (output stable)	3.436e-05	1.967e-04	3.708e-04
C (output stable)	9.861e-05	4.987e-04	9.741e-04
D (output stable)	1.527e-04	1.013e-03	1.888e-03
A to Z	3.374e-03	1.388e-02	2.702e-02
B to Z	3.136e-03	1.259e-02	2.456e-02
C to Z	2.651e-03	1.094e-02	2.084e-02
D to Z	2.360e-03	9.428e-03	1.792e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

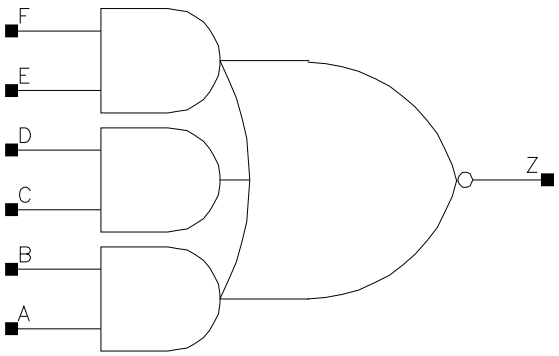
Pin Cycle (vdds)	X4_P0	X17_P0	X34_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X8_P0	1.200	2.176	2.6112
X13_P0	1.200	2.720	3.2640
X17_P0	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P0	X8_P0	X13_P0	X17_P0
A	0.0009	0.0017	0.0026	0.0035

B	0.0008	0.0016	0.0025	0.0033
C	0.0008	0.0017	0.0025	0.0033
D	0.0008	0.0016	0.0023	0.0031
E	0.0010	0.0017	0.0025	0.0032
F	0.0008	0.0016	0.0023	0.0031

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0098	0.0125	2.3254	1.3401
A to Z ↑	0.0184	0.0181	4.5859	2.1448
B to Z ↓	0.0117	0.0141	2.3505	1.3500
B to Z ↑	0.0166	0.0160	4.5754	2.1506
C to Z ↓	0.0086	0.0108	2.3132	1.3547
C to Z ↑	0.0176	0.0176	4.6122	2.1554
D to Z ↓	0.0102	0.0127	2.3435	1.3690
D to Z ↑	0.0156	0.0153	4.5782	2.1541
E to Z ↓	0.0059	0.0077	2.2995	1.3599
E to Z ↑	0.0162	0.0158	4.5477	2.1361
F to Z ↓	0.0069	0.0091	2.3385	1.3789
F to Z ↑	0.0143	0.0133	4.5874	2.1400
	X13_P0	X17_P0	X13_P0	X17_P0
A to Z ↓	0.0119	0.0120	0.9102	0.6951
A to Z ↑	0.0165	0.0167	1.4144	1.0905
B to Z ↓	0.0138	0.0138	0.9174	0.7003
B to Z ↑	0.0147	0.0146	1.4205	1.0907
C to Z ↓	0.0103	0.0104	0.9146	0.6901
C to Z ↑	0.0160	0.0164	1.4240	1.0996
D to Z ↓	0.0122	0.0119	0.9240	0.6965
D to Z ↑	0.0140	0.0142	1.4267	1.0968
E to Z ↓	0.0073	0.0073	0.9139	0.6925
E to Z ↑	0.0147	0.0148	1.4162	1.0878
F to Z ↓	0.0087	0.0084	0.9259	0.7011
F to Z ↑	0.0124	0.0125	1.4194	1.0937

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	6.973e-04	1.000e-20
X8_P0	1.489e-03	1.000e-20
X13_P0	2.155e-03	1.000e-20
X17_P0	2.858e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	6.285e-05	1.474e-04	2.010e-04	2.738e-04
B (output stable)	6.766e-05	2.160e-04	2.565e-04	3.858e-04
C (output stable)	9.142e-05	1.959e-04	2.574e-04	3.534e-04
D (output stable)	9.829e-05	2.800e-04	3.210e-04	4.670e-04
E (output stable)	1.756e-04	4.329e-04	5.565e-04	7.528e-04
F (output stable)	2.024e-04	5.122e-04	6.227e-04	8.622e-04

A to Z	4.581e-03	9.490e-03	1.342e-02	1.776e-02
B to Z	4.293e-03	8.818e-03	1.251e-02	1.643e-02
C to Z	3.823e-03	8.106e-03	1.129e-02	1.494e-02
D to Z	3.565e-03	7.442e-03	1.039e-02	1.375e-02
E to Z	3.174e-03	6.684e-03	9.337e-03	1.233e-02
F to Z	2.926e-03	5.997e-03	8.430e-03	1.114e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

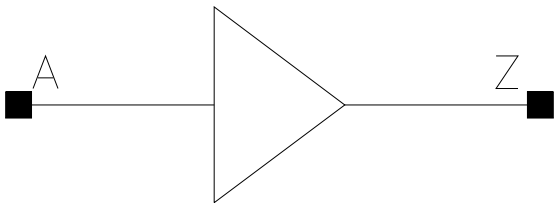
Pin Cycle (vdds)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X6_P0	1.200	0.408	0.4896
X8_P0	1.200	0.408	0.4896
X13_P0	1.200	0.544	0.6528
X16_P0	1.200	0.544	0.6528
X21_P0	1.200	0.680	0.8160
X25_P0	1.200	0.680	0.8160
X29_P0	1.200	0.952	1.1424
X33_P0	1.200	0.952	1.1424
X42_P0	1.200	1.088	1.3056
X50_P0	1.200	1.224	1.4688
X58_P0	1.200	1.496	1.7952
X67_P0	1.200	1.632	1.9584
X75_P0	1.200	1.768	2.1216
X84_P0	1.200	1.904	2.2848
X100_P0	1.200	2.312	2.7744
X134_P0	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0008	0.0008	0.0008	0.0008
	X16_P0	X21_P0	X25_P0	X29_P0
A	0.0008	0.0011	0.0011	0.0015
	X33_P0	X42_P0	X50_P0	X58_P0
A	0.0015	0.0018	0.0021	0.0031

	X67_P0	X75_P0	X84_P0	X100_P0
A	0.0031	0.0030	0.0030	0.0040
	X134_P0			
A	0.0051			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0143	0.0145	2.5780	1.8932
A to Z ↑	0.0113	0.0113	3.2292	2.4092
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0152	0.0169	1.4084	0.9018
A to Z ↑	0.0119	0.0139	1.7424	1.1295
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0184	0.0154	0.7177	0.5556
A to Z ↑	0.0149	0.0131	0.8714	0.6826
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0162	0.0156	0.4768	0.4007
A to Z ↑	0.0136	0.0122	0.5762	0.4877
	X33_P0	**X42_P0**	**X33_P0**	**X42_P0**
A to Z ↓	0.0163	0.0158	0.3566	0.2898
A to Z ↑	0.0128	0.0134	0.4311	0.3474
	X50_P0	**X58_P0**	**X50_P0**	**X58_P0**
A to Z ↓	0.0155	0.0145	0.2404	0.2074
A to Z ↑	0.0132	0.0123	0.2882	0.2483
	X67_P0	**X75_P0**	**X67_P0**	**X75_P0**
A to Z ↓	0.0152	0.0161	0.1819	0.1637
A to Z ↑	0.0130	0.0139	0.2174	0.1945
	X84_P0	**X100_P0**	**X84_P0**	**X100_P0**
A to Z ↓	0.0169	0.0157	0.1477	0.1242
A to Z ↑	0.0146	0.0136	0.1756	0.1471
	X134_P0		**X134_P0**	
A to Z ↓	0.0168		0.0957	
A to Z ↑	0.0148		0.1127	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	3.878e-04	1.000e-20
X6_P0	4.980e-04	1.000e-20
X8_P0	6.526e-04	1.000e-20
X13_P0	8.527e-04	1.000e-20
X16_P0	1.134e-03	1.000e-20
X21_P0	1.604e-03	1.000e-20
X25_P0	1.839e-03	1.000e-20
X29_P0	2.089e-03	1.000e-20
X33_P0	2.285e-03	1.000e-20
X42_P0	2.923e-03	1.000e-20
X50_P0	3.553e-03	1.000e-20
X58_P0	4.409e-03	1.000e-20
X67_P0	4.838e-03	1.000e-20
X75_P0	5.268e-03	1.000e-20

X84_P0	5.697e-03	1.000e-20
X100_P0	6.983e-03	1.000e-20
X134_P0	9.128e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	3.331e-03	3.757e-03	4.456e-03	6.127e-03
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	7.669e-03	1.013e-02	1.146e-02	1.331e-02
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	1.472e-02	1.839e-02	2.191e-02	2.653e-02
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	2.970e-02	3.318e-02	3.691e-02	4.372e-02
	X134_P0			
A to Z	6.109e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

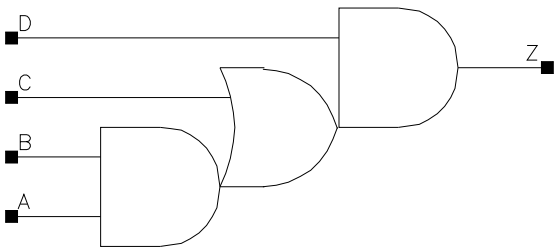
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P0			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.632	1.9584
X25_P0	1.200	1.768	2.1216
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0010	0.0021	0.0021	0.0021
B	0.0010	0.0019	0.0019	0.0019
C	0.0011	0.0024	0.0024	0.0024
D	0.0015	0.0020	0.0020	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0174	0.0163	1.4345	0.7103
A to Z ↑	0.0192	0.0183	1.7774	0.8676
B to Z ↓	0.0159	0.0148	1.4312	0.7095
B to Z ↑	0.0203	0.0191	1.7753	0.8664
C to Z ↓	0.0165	0.0156	1.4290	0.7085
C to Z ↑	0.0145	0.0136	1.7572	0.8565

D to Z ↓	0.0158	0.0141	1.4198	0.7041
D to Z ↑	0.0158	0.0140	1.7599	0.8592
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0181	0.0193	0.4814	0.3607
A to Z ↑	0.0202	0.0215	0.5883	0.4416
B to Z ↓	0.0167	0.0183	0.4807	0.3607
B to Z ↑	0.0211	0.0226	0.5878	0.4410
C to Z ↓	0.0175	0.0189	0.4793	0.3595
C to Z ↑	0.0153	0.0165	0.5807	0.4351
D to Z ↓	0.0153	0.0162	0.4755	0.3560
D to Z ↑	0.0156	0.0166	0.5824	0.4366

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.150e-03	1.000e-20
X17_P0	2.295e-03	1.000e-20
X25_P0	2.841e-03	1.000e-20
X33_P0	3.386e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	7.349e-05	1.524e-04	1.565e-04	1.391e-04
B (output stable)	9.155e-05	1.934e-04	1.939e-04	1.732e-04
C (output stable)	2.753e-04	4.340e-04	4.382e-04	4.289e-04
D (output stable)	1.421e-04	2.233e-04	2.241e-04	2.197e-04
A to Z	6.574e-03	1.246e-02	1.615e-02	2.001e-02
B to Z	6.300e-03	1.180e-02	1.551e-02	1.949e-02
C to Z	5.814e-03	1.083e-02	1.415e-02	1.761e-02
D to Z	6.755e-03	1.266e-02	1.572e-02	1.885e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

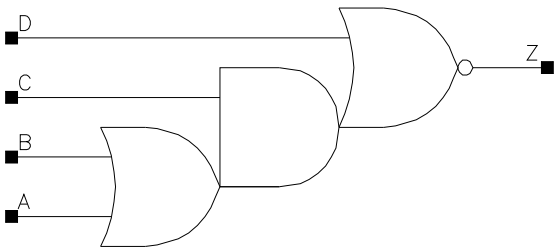
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.952	1.1424
X11_P0	1.200	1.496	1.7952
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X16_P0	X21_P0
A	0.0009	0.0017	0.0026	0.0035
B	0.0009	0.0017	0.0027	0.0034
C	0.0009	0.0017	0.0026	0.0035
D	0.0012	0.0018	0.0026	0.0035

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0080	0.0074	2.3064	1.2138
A to Z ↑	0.0156	0.0146	4.6779	2.4709
B to Z ↓	0.0074	0.0070	2.2482	1.1918
B to Z ↑	0.0162	0.0155	4.6882	2.4788
C to Z ↓	0.0084	0.0081	2.1426	1.1286
C to Z ↑	0.0098	0.0089	3.2245	1.6719

D to Z ↓	0.0035	0.0026	1.5018	0.7588
D to Z ↑	0.0116	0.0106	3.4343	1.7865
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0074	0.0077	0.8112	0.6282
A to Z ↑	0.0133	0.0140	1.5667	1.2258
B to Z ↓	0.0067	0.0070	0.8181	0.6308
B to Z ↑	0.0142	0.0148	1.5705	1.2288
C to Z ↓	0.0082	0.0084	0.7698	0.5927
C to Z ↑	0.0082	0.0083	1.1036	0.8302
D to Z ↓	0.0028	0.0028	0.5252	0.4003
D to Z ↑	0.0097	0.0097	1.1651	0.8872

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	6.174e-04	1.000e-20
X11_P0	1.190e-03	1.000e-20
X16_P0	1.736e-03	1.000e-20
X21_P0	2.278e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	3.931e-05	7.223e-05	9.581e-05	1.497e-04
B (output stable)	5.006e-05	8.813e-05	1.204e-04	1.933e-04
C (output stable)	1.093e-04	2.202e-04	3.042e-04	4.222e-04
D (output stable)	3.823e-04	8.046e-04	1.140e-03	1.621e-03
A to Z	4.031e-03	7.363e-03	1.056e-02	1.426e-02
B to Z	3.554e-03	6.501e-03	9.578e-03	1.264e-02
C to Z	3.535e-03	6.470e-03	9.339e-03	1.257e-02
D to Z	3.120e-03	5.850e-03	8.401e-03	1.110e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

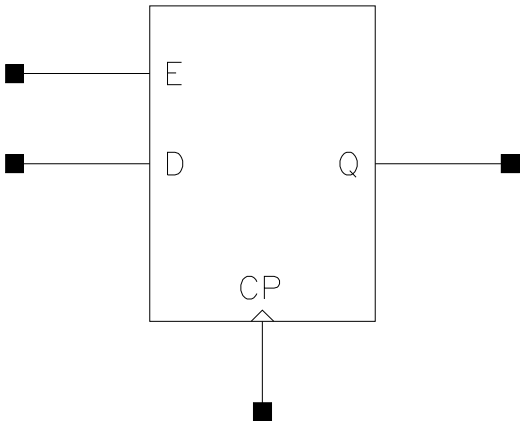
Pin Cycle (vdds)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.128	3.7536
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0011	0.0011	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0222	0.0256	1.4081	0.7209
CP to Q ↑	0.0285	0.0309	1.7854	0.8957
	X33_P0		**X33_P0**	
CP to Q ↓	0.0389		0.3612	
CP to Q ↑	0.0481		0.4441	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0294	0.0294	0.0294
CP ↑	min_pulse_width to CP	0.0189	0.0224	0.0190
D ↓	hold_rising to CP	-0.0000	-0.0000	-0.0000
D ↑	hold_rising to CP	0.0080	0.0080	0.0080
D ↓	setup_rising to CP	0.0241	0.0237	0.0241
D ↑	setup_rising to CP	0.0191	0.0195	0.0195
E ↓	hold_rising to CP	0.0027	0.0027	0.0027
E ↑	hold_rising to CP	0.0058	0.0054	0.0054
E ↓	setup_rising to CP	0.0311	0.0311	0.0311
E ↑	setup_rising to CP	0.0266	0.0266	0.0266

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	2.293e-03	1.000e-20
X17_P0	2.732e-03	1.000e-20
X33_P0	4.183e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

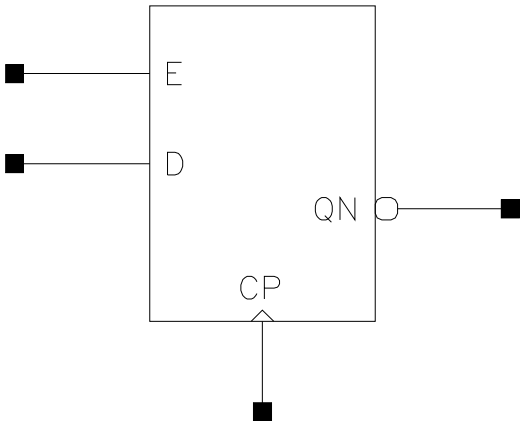
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.288e-02	1.288e-02	1.289e-02
Clock 100Mhz Data 25Mhz	1.667e-02	1.865e-02	2.236e-02
Clock 100Mhz Data 50Mhz	2.045e-02	2.443e-02	3.183e-02
Clock = 0 Data 100Mhz	7.884e-03	7.884e-03	7.885e-03
Clock = 1 Data 100Mhz	2.569e-03	2.568e-03	2.569e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.264	3.9168
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0011	0.0011	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0384	0.0368	1.4546	0.6991
CP to QN ↑	0.0304	0.0308	1.8183	0.8689
	X33_P0		**X33_P0**	
CP to QN ↓	0.0398		0.3617	
CP to QN ↑	0.0340		0.4466	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0294	0.0294	0.0294
CP ↑	min_pulse_width to CP	0.0177	0.0189	0.0189
D ↓	hold_rising to CP	0.0004	-0.0000	-0.0000
D ↑	hold_rising to CP	0.0054	0.0080	0.0080
D ↓	setup_rising to CP	0.0241	0.0237	0.0237
D ↑	setup_rising to CP	0.0191	0.0191	0.0195
E ↓	hold_rising to CP	0.0032	0.0027	0.0027
E ↑	hold_rising to CP	0.0058	0.0058	0.0054
E ↓	setup_rising to CP	0.0311	0.0311	0.0311
E ↑	setup_rising to CP	0.0266	0.0266	0.0266

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	2.278e-03	1.000e-20
X17_P0	3.058e-03	1.000e-20
X33_P0	4.075e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

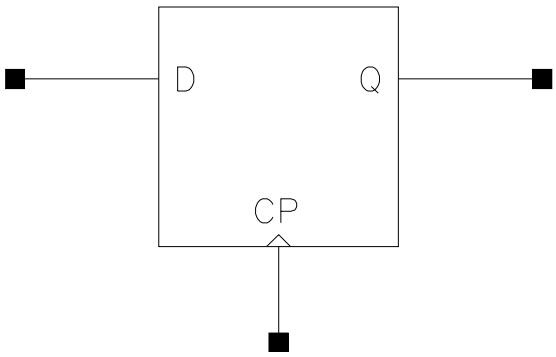
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.288e-02	1.288e-02	1.288e-02
Clock 100Mhz Data 25Mhz	1.656e-02	1.851e-02	2.255e-02
Clock 100Mhz Data 50Mhz	2.024e-02	2.415e-02	3.222e-02
Clock = 0 Data 100Mhz	7.883e-03	7.880e-03	7.882e-03
Clock = 1 Data 100Mhz	2.563e-03	2.565e-03	2.566e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.176	2.6112
X17_P0	1.200	2.448	2.9376
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0233	0.0259	1.3982	0.7152
CP to Q ↑	0.0285	0.0321	1.7152	0.8739
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to Q ↓	0.0325	0.0339	0.4156	0.3775
CP to Q ↑	0.0371	0.0379	0.4892	0.4473

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0293	0.0293	0.0293	0.0293
CP ↑	min_pulse_width to CP	0.0189	0.0224	0.0283	0.0283
D ↓	hold_rising to CP	0.0146	0.0146	0.0146	0.0146
D ↑	hold_rising to CP	0.0177	0.0177	0.0177	0.0177
D ↓	setup_rising to CP	0.0095	0.0117	0.0117	0.0117
D ↑	setup_rising to CP	0.0071	0.0103	0.0071	0.0071

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.749e-03	1.000e-20
X17_P0	2.249e-03	1.000e-20
X30_P0	3.009e-03	1.000e-20
X33_P0	3.119e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

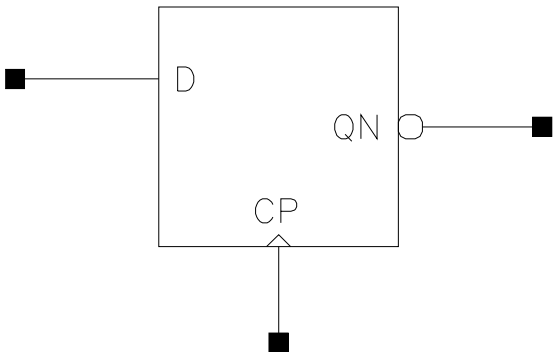
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.324e-02	1.327e-02	1.327e-02	1.328e-02
Clock 100Mhz Data 25Mhz	1.526e-02	1.759e-02	2.244e-02	2.359e-02
Clock 100Mhz Data 50Mhz	1.727e-02	2.192e-02	3.161e-02	3.391e-02
Clock = 0 Data 100Mhz	5.355e-03	5.475e-03	5.514e-03	5.533e-03
Clock = 1 Data 100Mhz	3.282e-05	3.414e-05	3.541e-05	3.425e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0227	0.0263	1.4398	0.7345
CP to QN ↑	0.0233	0.0252	1.7134	0.8777
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to QN ↓	0.0391	0.0395	0.3971	0.3610
CP to QN ↑	0.0321	0.0364	0.4732	0.4444

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0293	0.0293	0.0293	0.0293
CP ↑	min_pulse_width to CP	0.0190	0.0224	0.0189	0.0224
D ↓	hold_rising to CP	0.0173	0.0201	0.0146	0.0146
D ↑	hold_rising to CP	0.0177	0.0177	0.0177	0.0177
D ↓	setup_rising to CP	0.0095	0.0121	0.0117	0.0095
D ↑	setup_rising to CP	0.0071	0.0129	0.0071	0.0071

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.663e-03	1.000e-20
X17_P0	2.110e-03	1.000e-20
X30_P0	3.391e-03	1.000e-20
X33_P0	3.536e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

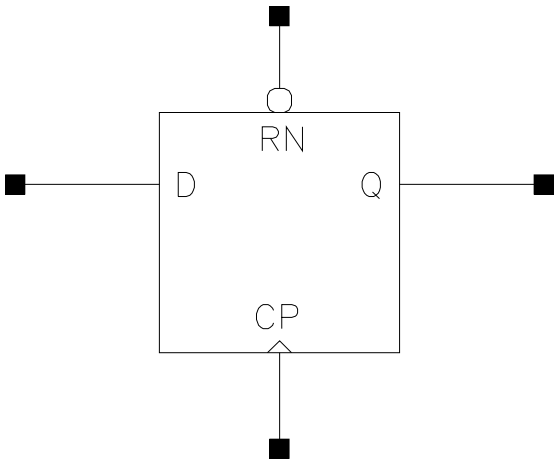
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.290e-02	1.291e-02	1.303e-02	1.309e-02
Clock 100Mhz Data 25Mhz	1.479e-02	1.687e-02	1.977e-02	2.119e-02
Clock 100Mhz Data 50Mhz	1.668e-02	2.084e-02	2.651e-02	2.929e-02
Clock = 0 Data 100Mhz	4.915e-03	4.920e-03	5.143e-03	5.196e-03
Clock = 1 Data 100Mhz	3.605e-05	3.586e-05	3.808e-05	3.668e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0010	0.0010
D	0.0007	0.0007
RN	0.0010	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0269	0.0336	0.7208	0.4215
CP to Q ↑	0.0331	0.0378	0.8769	0.4914
RN to Q ↓	0.0355	0.0398	0.7082	0.4118

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0294	0.0294
CP ↑	min_pulse_width to CP	0.0224	0.0283
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0119	0.0119
D ↓	setup_rising to CP	0.0149	0.0149
D ↑	setup_rising to CP	0.0124	0.0124
RN ↓	min_pulse_width to RN	0.0544	0.0664
RN ↑	recovery_rising to CP	0.0081	0.0081
RN ↑	removal_rising to CP	0.0025	0.0025

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P0	2.605e-03	1.000e-20
X30_P0	3.533e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

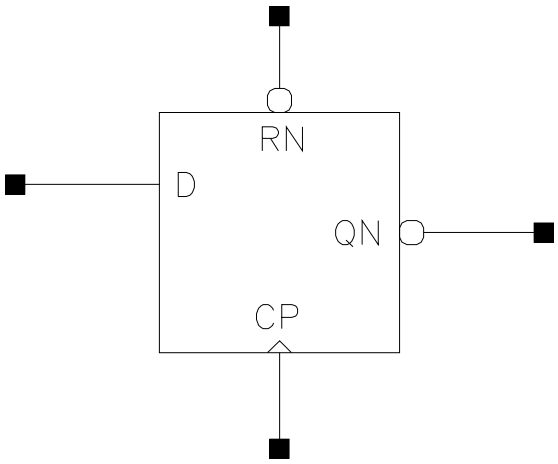
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	1.384e-02	1.384e-02
Clock 100Mhz Data 25Mhz	1.842e-02	2.324e-02
Clock 100Mhz Data 50Mhz	2.299e-02	3.264e-02
Clock = 0 Data 100Mhz	6.257e-03	6.263e-03
Clock = 1 Data 100Mhz	3.750e-05	4.000e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0010	0.0010
D	0.0007	0.0007
RN	0.0010	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0376	0.0408	0.6967	0.3982
CP to QN ↑	0.0306	0.0333	0.8569	0.4760
RN to QN ↑	0.0406	0.0432	0.8552	0.4755

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0294	0.0295
CP ↑	min_pulse_width to CP	0.0189	0.0189
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0119	0.0119
D ↓	setup_rising to CP	0.0149	0.0149
D ↑	setup_rising to CP	0.0124	0.0124
RN ↓	min_pulse_width to RN	0.0447	0.0447
RN ↑	recovery_rising to CP	0.0081	0.0081
RN ↑	removal_rising to CP	0.0025	0.0025

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P0	2.721e-03	1.000e-20
X30_P0	3.290e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

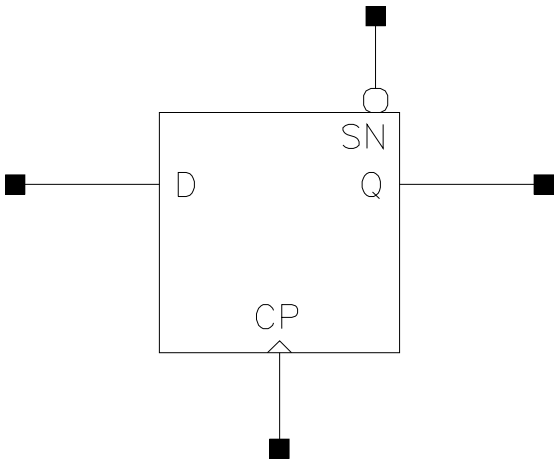
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	1.384e-02	1.382e-02
Clock 100Mhz Data 25Mhz	1.819e-02	2.092e-02
Clock 100Mhz Data 50Mhz	2.254e-02	2.801e-02
Clock = 0 Data 100Mhz	6.326e-03	6.310e-03
Clock = 1 Data 100Mhz	3.909e-05	3.955e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0270	0.0342	0.7218	0.4190
CP to Q ↑	0.0327	0.0377	0.8783	0.4915
SN to Q ↑	0.0266	0.0296	0.8681	0.4836

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0307	0.0308
CP ↑	min_pulse_width to CP	0.0224	0.0283
D ↓	hold_rising to CP	0.0151	0.0151
D ↑	hold_rising to CP	0.0177	0.0177
D ↓	setup_rising to CP	0.0143	0.0143
D ↑	setup_rising to CP	0.0129	0.0103
SN ↓	min_pulse_width to SN	0.0359	0.0430
SN ↑	recovery_rising to CP	-0.0027	-0.0027
SN ↑	removal_rising to CP	0.0136	0.0136

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P0	2.301e-03	1.000e-20
X30_P0	2.893e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

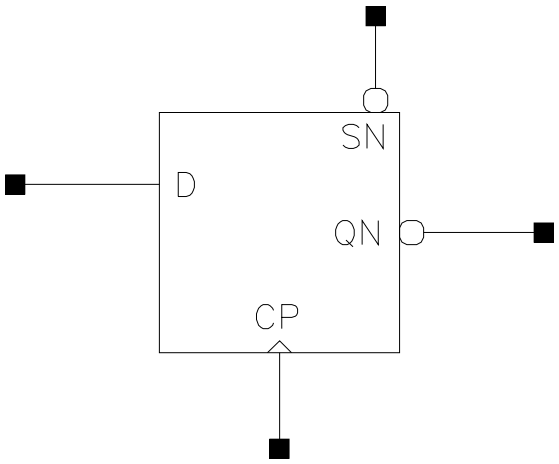
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	1.400e-02	1.395e-02
Clock 100Mhz Data 25Mhz	1.858e-02	2.340e-02
Clock 100Mhz Data 50Mhz	2.315e-02	3.286e-02
Clock = 0 Data 100Mhz	6.158e-03	6.159e-03
Clock = 1 Data 100Mhz	3.318e-05	3.330e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0371	0.0402	0.6971	0.3989
CP to QN ↑	0.0307	0.0334	0.8539	0.4753
SN to QN ↓	0.0317	0.0345	0.6973	0.3986

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0307	0.0307
CP ↑	min_pulse_width to CP	0.0189	0.0189
D ↓	hold_rising to CP	0.0156	0.0156
D ↑	hold_rising to CP	0.0177	0.0177
D ↓	setup_rising to CP	0.0143	0.0143
D ↑	setup_rising to CP	0.0129	0.0129
SN ↓	min_pulse_width to SN	0.0283	0.0283
SN ↑	recovery_rising to CP	-0.0022	-0.0022
SN ↑	removal_rising to CP	0.0136	0.0136

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P0	3.000e-03	1.000e-20
X30_P0	3.901e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

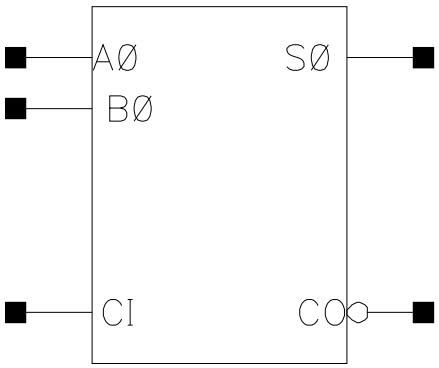
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	1.400e-02	1.399e-02
Clock 100Mhz Data 25Mhz	1.830e-02	2.097e-02
Clock 100Mhz Data 50Mhz	2.261e-02	2.794e-02
Clock = 0 Data 100Mhz	6.157e-03	6.158e-03
Clock = 1 Data 100Mhz	3.341e-05	3.545e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_P0	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_-P0	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_-P0	1.200	3.672	4.4064
C12T28SOI_LLS1_-FA1X33_P0	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0	0.0032	0.0067	0.0029	0.0058
B0	0.0030	0.0064	0.0032	0.0056
CI	0.0022	0.0047	0.0022	0.0040

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0
A0 to CO ↓	0.0237	0.0262	1.4589	0.3791
A0 to CO ↑	0.0198	0.0213	1.7723	0.4560
A0 to S0 ↓	0.0257	0.0328	1.4502	0.3712
A0 to S0 ↑	0.0264	0.0331	1.7608	0.4536
B0 to CO ↓	0.0239	0.0269	1.4621	0.3801
B0 to CO ↑	0.0207	0.0224	1.7730	0.4544
B0 to S0 ↓	0.0264	0.0339	1.4513	0.3715
B0 to S0 ↑	0.0271	0.0341	1.7611	0.4531
CI to CO ↓	0.0242	0.0277	1.4616	0.3781
CI to CO ↑	0.0209	0.0222	1.7723	0.4555
CI to S0 ↓	0.0265	0.0339	1.4518	0.3715
CI to S0 ↑	0.0275	0.0348	1.7609	0.4531
	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0 to CO ↓	0.0164	0.0204	2.6782	0.4585
A0 to CO ↑	0.0158	0.0178	1.8162	0.4461
A0 to S0 ↓	0.0352	0.0438	1.5751	0.3892
A0 to S0 ↑	0.0324	0.0351	1.8213	0.4607
B0 to CO ↓	0.0176	0.0217	2.6781	0.4589
B0 to CO ↑	0.0142	0.0166	1.8147	0.4467
B0 to S0 ↓	0.0353	0.0447	1.5748	0.3890
B0 to S0 ↑	0.0325	0.0360	1.8211	0.4606
CI to CO ↓	0.0175	0.0310	2.6736	0.4618
CI to CO ↑	0.0153	0.0184	1.8715	0.4495
CI to S0 ↓	0.0212	0.0274	1.5766	0.3896
CI to S0 ↑	0.0173	0.0176	1.8207	0.4610

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_FA1X8_P0	2.417e-03	1.000e-20
C12T28SOI_LL_FA1X33_P0	6.648e-03	1.000e-20
C12T28SOI_LLS1_FA1X8_P0	5.453e-03	1.000e-20
C12T28SOI_LLS1_FA1X33_P0	1.135e-02	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0 to CO	6.631e-03	2.167e-02	9.735e-03	2.557e-02
A0 to S0	6.720e-03	2.236e-02	1.289e-02	3.093e-02
B0 to CO	6.689e-03	2.214e-02	9.806e-03	2.575e-02
B0 to S0	6.688e-03	2.246e-02	1.307e-02	3.131e-02
CI to CO	6.790e-03	2.249e-02	7.324e-03	2.425e-02
CI to S0	6.669e-03	2.250e-02	8.454e-03	2.609e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P0	C12T28SOI_LL_-FA1X33_P0	C12T28SOI_LLS1_-FA1X8_P0	C12T28SOI_LLS1_-FA1X33_P0
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00

A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X33_P0	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X33_P0
A0	0.0011	0.0033
B0	0.0010	0.0028

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
A0 to CO ↓	0.0193	0.0179	1.4529	0.3617
A0 to CO ↑	0.0183	0.0174	1.7477	0.4536
A0 to S0 ↓	0.0243	0.0232	1.4265	0.3612
A0 to S0 ↑	0.0241	0.0287	1.7261	0.4463
B0 to CO ↓	0.0185	0.0162	1.4516	0.3582
B0 to CO ↑	0.0204	0.0192	1.7462	0.4533
B0 to S0 ↓	0.0262	0.0246	1.4263	0.3610
B0 to S0 ↑	0.0234	0.0273	1.7255	0.4461

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.577e-03	1.000e-20
X33_P0	6.880e-03	1.000e-20

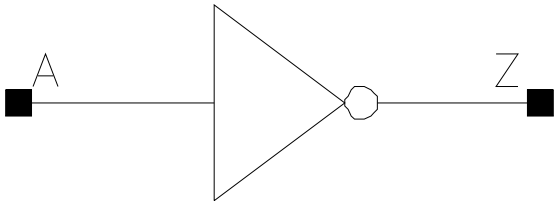
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X33_P0
A0 to CO	5.108e-03	1.824e-02
A0 to S0	4.995e-03	1.885e-02
B0 to CO	5.192e-03	1.870e-02
B0 to S0	4.953e-03	1.854e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X8_P0	X33_P0
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.272	0.3264
X6_P0	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X13_P0	1.200	0.408	0.4896
X17_P0	1.200	0.408	0.4896
X21_P0	1.200	0.544	0.6528
X25_P0	1.200	0.544	0.6528
X29_P0	1.200	0.680	0.8160
X33_P0	1.200	0.680	0.8160
X50_P0	1.200	0.952	1.1424
X58_P0	1.200	1.088	1.3056
X67_P0	1.200	1.224	1.4688
X75_P0	1.200	1.360	1.6320
X84_P0	1.200	1.496	1.7952
X100_P0	1.200	1.768	2.1216
X134_P0	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0006	0.0007	0.0009	0.0014
	X17_P0	X21_P0	X25_P0	X29_P0
A	0.0018	0.0024	0.0027	0.0032
	X33_P0	X50_P0	X58_P0	X67_P0
A	0.0036	0.0054	0.0063	0.0073
	X75_P0	X84_P0	X100_P0	X134_P0

A	0.0084	0.0095	0.0115	0.0157

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0035	0.0034	2.7568	2.1248
A to Z ↑	0.0073	0.0066	3.3528	2.5560
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0032	0.0024	1.4672	0.9445
A to Z ↑	0.0059	0.0055	1.7891	1.1734
	X17_P0	**X21_P0**	**X17_P0**	**X21_P0**
A to Z ↓	0.0027	0.0028	0.7267	0.5828
A to Z ↑	0.0052	0.0055	0.8842	0.7082
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0030	0.0027	0.4970	0.4199
A to Z ↑	0.0052	0.0051	0.5963	0.5061
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0028	0.0029	0.3733	0.2518
A to Z ↑	0.0049	0.0049	0.4471	0.2998
	X58_P0	**X67_P0**	**X58_P0**	**X67_P0**
A to Z ↓	0.0032	0.0032	0.2182	0.1916
A to Z ↑	0.0050	0.0050	0.2588	0.2269
	X75_P0	**X84_P0**	**X75_P0**	**X84_P0**
A to Z ↓	0.0037	0.0039	0.1730	0.1564
A to Z ↑	0.0054	0.0056	0.2039	0.1847
	X100_P0	**X134_P0**	**X100_P0**	**X134_P0**
A to Z ↓	0.0046	0.0054	0.1332	0.1037
A to Z ↑	0.0063	0.0070	0.1560	0.1205

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.972e-04	1.000e-20
X6_P0	2.861e-04	1.000e-20
X8_P0	4.504e-04	1.000e-20
X13_P0	6.582e-04	1.000e-20
X17_P0	9.333e-04	1.000e-20
X21_P0	1.124e-03	1.000e-20
X25_P0	1.363e-03	1.000e-20
X29_P0	1.592e-03	1.000e-20
X33_P0	1.791e-03	1.000e-20
X50_P0	2.646e-03	1.000e-20
X58_P0	3.074e-03	1.000e-20
X67_P0	3.502e-03	1.000e-20
X75_P0	3.929e-03	1.000e-20
X84_P0	4.357e-03	1.000e-20
X100_P0	5.212e-03	1.000e-20
X134_P0	6.922e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0

A to Z	1.782e-03	2.296e-03	3.248e-03	4.942e-03
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	6.470e-03	8.172e-03	9.575e-03	1.122e-02
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	1.252e-02	1.855e-02	2.163e-02	2.468e-02
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	2.794e-02	3.119e-02	3.830e-02	5.231e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

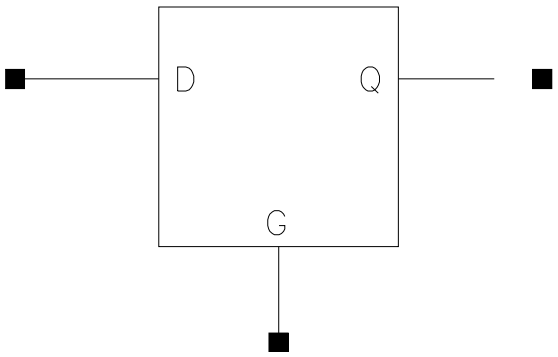
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X23_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P0	X23_P0
D	0.0006	0.0014
G	0.0012	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X23_P0	X8_P0	X23_P0
D to Q ↓	0.0275	0.0217	1.4373	0.6827
D to Q ↑	0.0193	0.0198	1.7167	0.4612
G to Q ↓	0.0286	0.0246	1.4329	0.6822
G to Q ↑	0.0193	0.0166	1.7173	0.4616

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X23_P0
D ↓	hold_falling to G	0.0048	0.0127
D ↑	hold_falling to G	0.0115	0.0090
D ↓	setup_falling to G	0.0263	0.0169
D ↑	setup_falling to G	0.0231	0.0287
G ↑	min_pulse_width to G	0.0271	0.0271

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.010e-03	1.000e-20
X23_P0	2.814e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X23_P0
D (output stable)	2.334e-05	1.006e-04
G (output stable)	2.151e-03	4.284e-03
D to Q	8.940e-03	1.831e-02
G to Q	9.082e-03	1.763e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

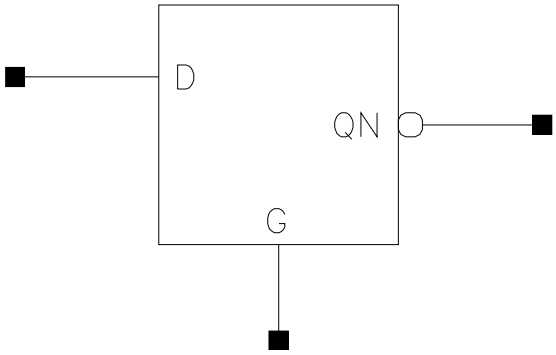
Pin Cycle (vdds)	X8_P0	X23_P0
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P0
D	0.0006
G	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P0	X17_P0
D to QN ↓	0.0245	0.6978
D to QN ↑	0.0311	0.8464
G to QN ↓	0.0240	0.6970
G to QN ↑	0.0314	0.8454

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P0
D ↓	hold_falling to G	0.0032
D ↑	hold_falling to G	0.0089
D ↓	setup_falling to G	0.0247
D ↑	setup_falling to G	0.0160
G ↑	min_pulse_width to G	0.0189

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P0	1.679e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X17_P0
D (output stable)	2.343e-05
G (output stable)	2.899e-03
D to QN	1.019e-02
G to QN	1.080e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

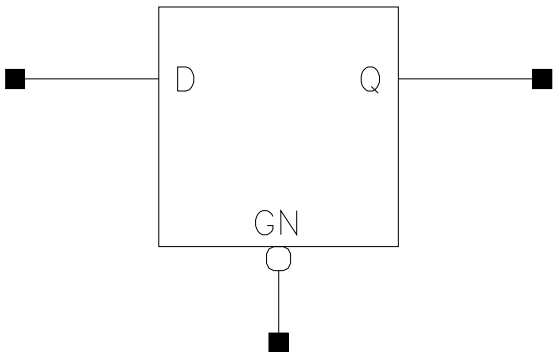
Pin Cycle (vdds)	X17_P0
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
D	0.0006	0.0008	0.0018
GN	0.0011	0.0015	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D to Q ↓	0.0278	0.0242	1.4395	0.7173
D to Q ↑	0.0196	0.0192	1.7201	0.8824
GN to Q ↓	0.0265	0.0220	1.4411	0.7184
GN to Q ↑	0.0286	0.0277	1.7147	0.8813

	X33_P0		X33_P0	
D to Q ↓	0.0238		0.3678	
D to Q ↑	0.0161		0.4438	
GN to Q ↓	0.0201		0.3680	
GN to Q ↑	0.0217		0.4435	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X17_P0	X33_P0
D ↓	hold_rising to GN	0.0078	0.0068	0.0068
D ↑	hold_rising to GN	0.0127	0.0128	0.0148
D ↓	setup_rising to GN	0.0329	0.0276	0.0286
D ↑	setup_rising to GN	0.0195	0.0168	0.0178
GN ↓	min_pulse_width to GN	0.0384	0.0312	0.0271

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.051e-03	1.000e-20
X17_P0	1.775e-03	1.000e-20
X33_P0	3.152e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
D (output stable)	2.534e-05	4.441e-05	1.080e-04
GN (output stable)	2.129e-03	2.814e-03	4.035e-03
D to Q	8.996e-03	1.349e-02	2.221e-02
GN to Q	1.195e-02	1.689e-02	2.576e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

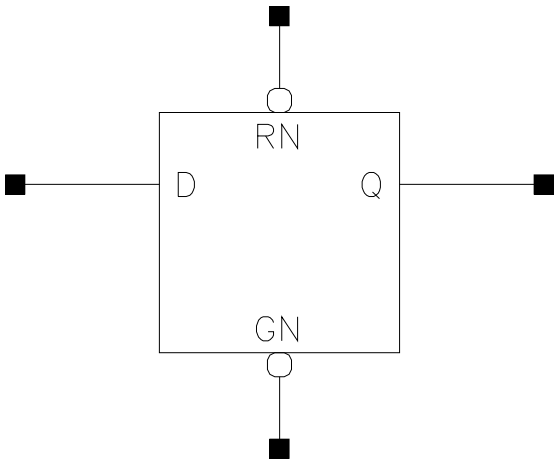
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.496	1.7952
X33_P0	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X33_P0
D	0.0006	0.0015
GN	0.0013	0.0024
RN	0.0006	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
D to Q ↓	0.0254	0.0230	1.4177	0.3689
D to Q ↑	0.0260	0.0353	1.7528	0.4575

GN to Q ↓	0.0242	0.0211	1.4192	0.3693
GN to Q ↑	0.0327	0.0354	1.7548	0.4572
RN to Q ↓	0.0217	0.0379	1.3646	0.3691
RN to Q ↑	0.0259	0.0382	1.7561	0.4580

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X33_P0
D ↓	hold_rising to GN	0.0068	0.0114
D ↑	hold_rising to GN	0.0081	-0.0049
D ↓	setup_rising to GN	0.0277	0.0263
D ↑	setup_rising to GN	0.0271	0.0387
GN ↓	min_pulse_width to GN	0.0344	0.0357
RN ↓	min_pulse_width to RN	0.0261	0.0474
RN ↑	recovery_rising to GN	0.0264	0.0411
RN ↑	removal_rising to GN	-0.0120	-0.0239

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.283e-03	1.000e-20
X33_P0	3.429e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X33_P0
D (output stable)	6.952e-05	1.300e-04
GN (output stable)	2.382e-03	4.017e-03
RN (output stable)	6.355e-05	1.223e-04
D to Q	9.242e-03	2.759e-02
GN to Q	1.250e-02	3.236e-02
RN to Q	6.380e-03	2.139e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

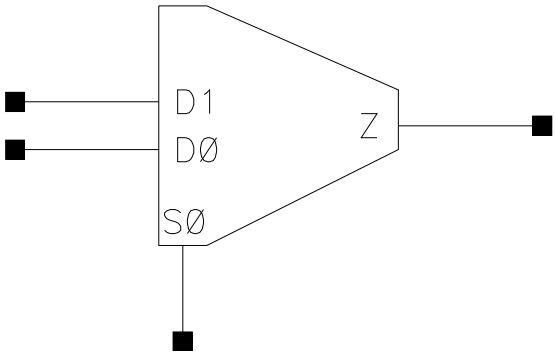
Pin Cycle (vdds)	X8_P0	X33_P0
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
D0	0.0008	0.0011	0.0015	0.0020
D1	0.0008	0.0011	0.0015	0.0020
S0	0.0014	0.0015	0.0017	0.0026

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D0 to Z ↓	0.0219	0.0198	1.4474	0.7097
D0 to Z ↑	0.0185	0.0174	1.7735	0.8694
D1 to Z ↓	0.0207	0.0192	1.4451	0.7089
D1 to Z ↑	0.0169	0.0165	1.7722	0.8689
S0 to Z ↓	0.0194	0.0190	1.4405	0.7075
S0 to Z ↑	0.0182	0.0188	1.7702	0.8693

	X25_P0	X33_P0	X25_P0	X33_P0
D0 to Z ↓	0.0213	0.0191	0.4855	0.3651
D0 to Z ↑	0.0183	0.0173	0.5850	0.4390
D1 to Z ↓	0.0227	0.0198	0.4876	0.3658
D1 to Z ↑	0.0179	0.0170	0.5839	0.4389
S0 to Z ↓	0.0218	0.0201	0.4855	0.3648
S0 to Z ↑	0.0206	0.0190	0.5844	0.4388

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.229e-03	1.000e-20
X17_P0	2.446e-03	1.000e-20
X25_P0	3.164e-03	1.000e-20
X33_P0	4.852e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	2.145e-03	3.690e-03	4.593e-03	6.816e-03
D1 (output stable)	2.024e-03	3.682e-03	4.681e-03	6.816e-03
S0 (output stable)	2.358e-03	2.589e-03	3.193e-03	4.329e-03
D0 to Z	6.033e-03	1.080e-02	1.644e-02	2.127e-02
D1 to Z	5.694e-03	1.058e-02	1.659e-02	2.120e-02
S0 to Z	7.068e-03	1.127e-02	1.784e-02	2.236e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

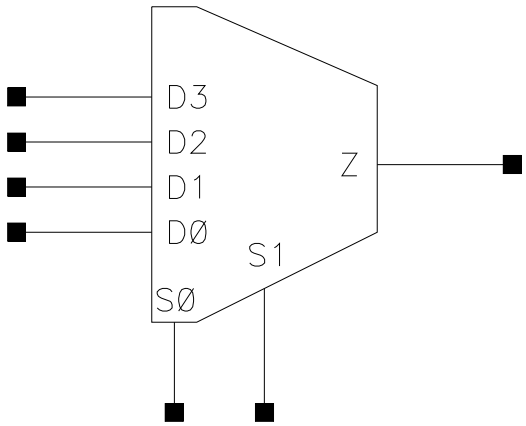
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.312	2.7744
X31_P0	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P0	X31_P0
D0	0.0006	0.0016
D1	0.0006	0.0016
D2	0.0006	0.0016
D3	0.0006	0.0016
S0	0.0020	0.0039
S1	0.0012	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X31_P0	X8_P0	X31_P0

D0 to Z ↓	0.0344	0.0359	1.4878	0.4105
D0 to Z ↑	0.0258	0.0286	1.7796	0.4826
D1 to Z ↓	0.0340	0.0359	1.4866	0.4107
D1 to Z ↑	0.0259	0.0285	1.7810	0.4825
D2 to Z ↓	0.0364	0.0337	1.4942	0.4074
D2 to Z ↑	0.0274	0.0262	1.7872	0.4787
D3 to Z ↓	0.0362	0.0333	1.4940	0.4066
D3 to Z ↑	0.0271	0.0275	1.7859	0.4808
S0 to Z ↓	0.0374	0.0392	1.4888	0.4084
S0 to Z ↑	0.0310	0.0337	1.7859	0.4820
S1 to Z ↓	0.0292	0.0300	1.4908	0.4086
S1 to Z ↑	0.0256	0.0278	1.7839	0.4815

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.181e-03	1.000e-20
X31_P0	3.920e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X31_P0
D0 (output stable)	3.620e-05	1.831e-04
D1 (output stable)	3.576e-05	1.684e-04
D2 (output stable)	4.099e-05	1.740e-04
D3 (output stable)	4.088e-05	1.756e-04
S0 (output stable)	2.898e-03	5.960e-03
S1 (output stable)	2.780e-03	5.452e-03
D0 to Z	6.721e-03	2.499e-02
D1 to Z	6.689e-03	2.507e-02
D2 to Z	7.058e-03	2.336e-02
D3 to Z	7.034e-03	2.357e-02
S0 to Z	9.661e-03	3.014e-02
S1 to Z	8.612e-03	2.649e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

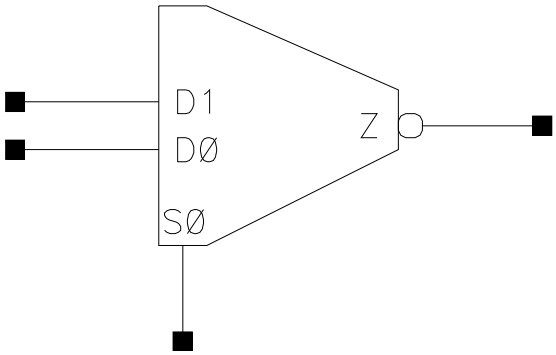
Pin Cycle (vdds)	X8_P0	X31_P0
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.816	0.9792
X5_P0	1.200	0.952	1.1424
X10_P0	1.200	1.768	2.1216
X16_P0	1.200	2.448	2.9376
X21_P0	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P0	X5_P0	X10_P0	X16_P0
D0	0.0006	0.0009	0.0018	0.0027
D1	0.0006	0.0009	0.0017	0.0026
S0	0.0012	0.0020	0.0026	0.0039
	X21_P0			
D0	0.0036			
D1	0.0035			
S0	0.0044			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X5_P0	X3_P0	X5_P0
D0 to Z ↓	0.0069	0.0073	4.2447	2.7100

D0 to Z ↑	0.0125	0.0109	6.6630	3.5056
D1 to Z ↓	0.0068	0.0072	4.2240	2.5625
D1 to Z ↑	0.0128	0.0110	6.6752	3.6940
S0 to Z ↓	0.0116	0.0102	4.2191	2.6289
S0 to Z ↑	0.0128	0.0111	6.6736	3.6019
	X10_P0	**X16_P0**	**X10_P0**	**X16_P0**
D0 to Z ↓	0.0084	0.0077	1.2847	0.8401
D0 to Z ↑	0.0116	0.0110	1.6532	1.0989
D1 to Z ↓	0.0077	0.0075	1.2373	0.8153
D1 to Z ↑	0.0116	0.0111	1.6899	1.1153
S0 to Z ↓	0.0125	0.0108	1.2584	0.8264
S0 to Z ↑	0.0132	0.0114	1.6727	1.1094
	X21_P0		**X21_P0**	
D0 to Z ↓	0.0077		0.6436	
D0 to Z ↑	0.0107		0.8355	
D1 to Z ↓	0.0076		0.6200	
D1 to Z ↑	0.0110		0.8327	
S0 to Z ↓	0.0113		0.6310	
S0 to Z ↑	0.0117		0.8347	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	4.165e-04	1.000e-20
X5_P0	1.023e-03	1.000e-20
X10_P0	1.819e-03	1.000e-20
X16_P0	2.917e-03	1.000e-20
X21_P0	3.572e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	2.384e-05	5.559e-05	1.492e-04	2.243e-04
D1 (output stable)	2.364e-05	5.643e-05	1.252e-04	2.194e-04
S0 (output stable)	2.156e-03	3.668e-03	4.885e-03	8.836e-03
D0 to Z	1.816e-03	3.187e-03	7.331e-03	1.063e-02
D1 to Z	1.827e-03	3.141e-03	7.166e-03	1.052e-02
S0 to Z	3.477e-03	5.813e-03	1.006e-02	1.604e-02
	X21_P0			
D0 (output stable)	2.984e-04			
D1 (output stable)	2.953e-04			
S0 (output stable)	9.307e-03			
D0 to Z	1.388e-02			
D1 to Z	1.391e-02			
S0 to Z	1.892e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

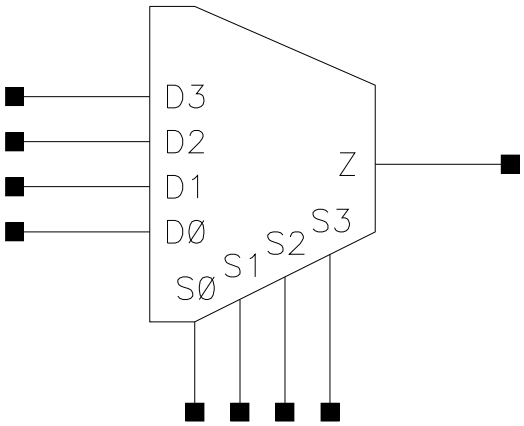
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P0			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	1.768	2.1216
X27_P0	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P0	X27_P0
D0	0.0007	0.0021
D1	0.0007	0.0021
D2	0.0007	0.0020
D3	0.0007	0.0021
S0	0.0007	0.0019
S1	0.0008	0.0020
S2	0.0007	0.0019
S3	0.0007	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	X27_P0	X7_P0	X27_P0
D0 to Z ↓	0.0273	0.0227	2.2217	0.6103
D0 to Z ↑	0.0215	0.0186	1.7289	0.4361
D1 to Z ↓	0.0269	0.0227	2.2194	0.6098
D1 to Z ↑	0.0189	0.0160	1.7208	0.4348
D2 to Z ↓	0.0281	0.0225	2.2240	0.6098
D2 to Z ↑	0.0211	0.0177	1.7340	0.4373
D3 to Z ↓	0.0277	0.0225	2.2198	0.6090
D3 to Z ↑	0.0186	0.0151	1.7272	0.4354
S0 to Z ↓	0.0263	0.0214	2.2215	0.6102
S0 to Z ↑	0.0237	0.0205	1.7245	0.4354
S1 to Z ↓	0.0260	0.0214	2.2187	0.6096
S1 to Z ↑	0.0209	0.0175	1.7185	0.4342
S2 to Z ↓	0.0270	0.0211	2.2236	0.6095
S2 to Z ↑	0.0233	0.0195	1.7307	0.4365
S3 to Z ↓	0.0269	0.0211	2.2195	0.6086
S3 to Z ↑	0.0207	0.0167	1.7253	0.4347

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X7_P0	1.122e-03	1.000e-20
X27_P0	4.879e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X7_P0	X27_P0
D0 (output stable)	7.228e-04	2.394e-03
D1 (output stable)	6.685e-04	2.156e-03
D2 (output stable)	6.812e-04	2.257e-03
D3 (output stable)	6.268e-04	2.022e-03
S0 (output stable)	7.021e-04	2.296e-03
S1 (output stable)	6.468e-04	2.067e-03
S2 (output stable)	6.604e-04	2.160e-03
S3 (output stable)	6.042e-04	1.935e-03
D0 to Z	6.549e-03	2.116e-02
D1 to Z	6.027e-03	1.928e-02
D2 to Z	6.457e-03	1.975e-02
D3 to Z	5.948e-03	1.789e-02
S0 to Z	6.442e-03	2.054e-02
S1 to Z	5.917e-03	1.866e-02
S2 to Z	6.351e-03	1.911e-02
S3 to Z	5.841e-03	1.729e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

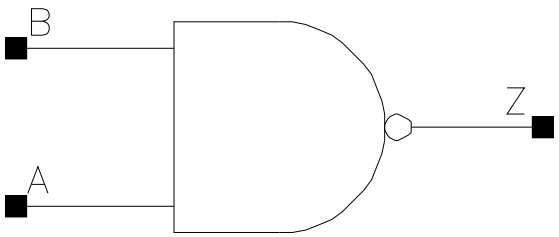
Pin Cycle (vdds)	X7_P0	X27_P0
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P0	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P0	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P0	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P0	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P0	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P0	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P0	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P0	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P0	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P0	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P0	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P0	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P0	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P0	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P0	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P0	C12T28SOI_LL_-NAND2X5_P0	C12T28SOI_LL_-NAND2X7_P0	C12T28SOI_LL_-NAND2X10_P0
A	0.0006	0.0008	0.0009	0.0015
B	0.0006	0.0008	0.0009	0.0014
	C12T28SOI_LL_-NAND2X13_P0	C12T28SOI_LL_-NAND2X17_P0	C12T28SOI_LL_-NAND2X20_P0	C12T28SOI_LL_-NAND2X24_P0
A	0.0018	0.0023	0.0027	0.0033
B	0.0017	0.0022	0.0026	0.0031
	C12T28SOI_LL_-NAND2X27_P0	C12T28SOI_LL_-NAND2X42_P0	C12T28SOI_LL_-NAND2X47_P0	C12T28SOI_LL_-NAND2X50_P0
A	0.0037	0.0011	0.0011	0.0011
B	0.0034	0.0011	0.0011	0.0011
	C12T28SOI_LL_-NAND2X58_P0	C12T28SOI_LL_-NAND2X67_P0	C12T28SOI_-LLBR0D8_-NAND2X7_P0	C12T28SOI_-LLBR0D8_-NAND2X14_P0
A	0.0011	0.0011	0.0009	0.0018
B	0.0011	0.0011	0.0009	0.0017
	C12T28SOI_LLS_-NAND2X40_P0	C12T28SOI_LLS_-NAND2X54_P0		
A	0.0055	0.0073		
B	0.0051	0.0069		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P0	**C12T28SOI_LL_-NAND2X5_P0**	**C12T28SOI_LL_-NAND2X3_P0**	**C12T28SOI_LL_-NAND2X5_P0**
A to Z ↓	0.0055	0.0053	4.1661	2.7348
A to Z ↑	0.0083	0.0074	3.3763	2.1992
B to Z ↓	0.0069	0.0065	4.2223	2.7663
B to Z ↑	0.0070	0.0059	3.4151	2.2228
	C12T28SOI_LL_-NAND2X7_P0	**C12T28SOI_LL_-NAND2X10_P0**	**C12T28SOI_LL_-NAND2X7_P0**	**C12T28SOI_LL_-NAND2X10_P0**
A to Z ↓	0.0054	0.0057	2.3033	1.5190
A to Z ↑	0.0070	0.0076	1.7795	1.1634
B to Z ↓	0.0066	0.0065	2.3280	1.5346
B to Z ↑	0.0055	0.0054	1.8050	1.1756
	C12T28SOI_LL_-NAND2X13_P0	**C12T28SOI_LL_-NAND2X17_P0**	**C12T28SOI_LL_-NAND2X13_P0**	**C12T28SOI_LL_-NAND2X17_P0**
A to Z ↓	0.0058	0.0055	1.1804	0.9320

A to Z ↑	0.0070	0.0071	0.8820	0.7070
B to Z ↓	0.0066	0.0068	1.1922	0.9415
B to Z ↑	0.0049	0.0053	0.8913	0.7146
	C12T28SOI_LL_-NAND2X20_P0	**C12T28SOI_LL_-NAND2X24_P0**	**C12T28SOI_LL_-NAND2X20_P0**	**C12T28SOI_LL_-NAND2X24_P0**
A to Z ↓	0.0057	0.0057	0.8054	0.6823
A to Z ↑	0.0068	0.0069	0.5952	0.5056
B to Z ↓	0.0070	0.0067	0.8138	0.6887
B to Z ↑	0.0050	0.0049	0.6026	0.5107
	C12T28SOI_LL_-NAND2X27_P0	**C12T28SOI_LL_-NAND2X42_P0**	**C12T28SOI_LL_-NAND2X27_P0**	**C12T28SOI_LL_-NAND2X42_P0**
A to Z ↓	0.0057	0.0219	0.6121	0.2919
A to Z ↑	0.0067	0.0216	0.4473	0.3471
B to Z ↓	0.0067	0.0234	0.6182	0.2916
B to Z ↑	0.0046	0.0206	0.4520	0.3473
	C12T28SOI_LL_-NAND2X47_P0	**C12T28SOI_LL_-NAND2X50_P0**	**C12T28SOI_LL_-NAND2X47_P0**	**C12T28SOI_LL_-NAND2X50_P0**
A to Z ↓	0.0225	0.0227	0.2582	0.2431
A to Z ↑	0.0220	0.0222	0.3005	0.2896
B to Z ↓	0.0240	0.0242	0.2586	0.2432
B to Z ↑	0.0209	0.0212	0.3006	0.2897
	C12T28SOI_LL_-NAND2X58_P0	**C12T28SOI_LL_-NAND2X67_P0**	**C12T28SOI_LL_-NAND2X58_P0**	**C12T28SOI_LL_-NAND2X67_P0**
A to Z ↓	0.0238	0.0248	0.2103	0.1845
A to Z ↑	0.0231	0.0239	0.2490	0.2190
B to Z ↓	0.0252	0.0263	0.2101	0.1844
B to Z ↑	0.0220	0.0229	0.2495	0.2191
	C12T28SOI_-LLBR0D8_-NAND2X7_P0	**C12T28SOI_-LLBR0D8_-NAND2X14_P0**	**C12T28SOI_-LLBR0D8_-NAND2X7_P0**	**C12T28SOI_-LLBR0D8_-NAND2X14_P0**
A to Z ↓	0.0025	0.0031	1.7665	0.9330
A to Z ↑	0.0102	0.0102	2.3187	1.1436
B to Z ↓	0.0033	0.0032	1.7956	0.9474
B to Z ↑	0.0085	0.0075	2.4199	1.1708
	C12T28SOI_LLS_-NAND2X40_P0	**C12T28SOI_LLS_-NAND2X54_P0**	**C12T28SOI_LLS_-NAND2X40_P0**	**C12T28SOI_LLS_-NAND2X54_P0**
A to Z ↓	0.0057	0.0058	0.4149	0.3141
A to Z ↑	0.0066	0.0067	0.3005	0.2269
B to Z ↓	0.0068	0.0070	0.4192	0.3174
B to Z ↑	0.0045	0.0046	0.3038	0.2296

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P0	1.946e-04	1.000e-20
C12T28SOI_LL_NAND2X5_P0	3.600e-04	1.000e-20
C12T28SOI_LL_NAND2X7_P0	4.592e-04	1.000e-20
C12T28SOI_LL_NAND2X10_P0	6.461e-04	1.000e-20
C12T28SOI_LL_NAND2X13_P0	9.200e-04	1.000e-20
C12T28SOI_LL_NAND2X17_P0	1.110e-03	1.000e-20
C12T28SOI_LL_NAND2X20_P0	1.349e-03	1.000e-20
C12T28SOI_LL_NAND2X24_P0	1.576e-03	1.000e-20
C12T28SOI_LL_NAND2X27_P0	1.779e-03	1.000e-20

C12T28SOI_LL_NAND2X42_P0	3.142e-03	1.000e-20
C12T28SOI_LL_NAND2X47_P0	3.427e-03	1.000e-20
C12T28SOI_LL_NAND2X50_P0	3.419e-03	1.000e-20
C12T28SOI_LL_NAND2X58_P0	3.697e-03	1.000e-20
C12T28SOI_LL_NAND2X67_P0	3.974e-03	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_P0	3.634e-04	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_-P0	7.206e-04	1.000e-20
C12T28SOI_LLS_NAND2X40_P0	2.637e-03	1.000e-20
C12T28SOI_LLS_NAND2X54_P0	3.496e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND2X3_P0	C12T28SOI_LL_-NAND2X5_P0	C12T28SOI_LL_-NAND2X7_P0	C12T28SOI_LL_-NAND2X10_P0
A (output stable)	1.833e-05	2.766e-05	3.211e-05	1.022e-04
B (output stable)	2.570e-05	3.932e-05	4.876e-05	2.633e-04
A to Z	1.822e-03	2.720e-03	3.296e-03	5.111e-03
B to Z	1.680e-03	2.493e-03	2.993e-03	4.555e-03
	C12T28SOI_LL_-NAND2X13_P0	C12T28SOI_LL_-NAND2X17_P0	C12T28SOI_LL_-NAND2X20_P0	C12T28SOI_LL_-NAND2X24_P0
A (output stable)	1.218e-04	1.414e-04	1.554e-04	2.183e-04
B (output stable)	3.055e-04	3.051e-04	3.298e-04	4.957e-04
A to Z	6.626e-03	8.297e-03	9.739e-03	1.153e-02
B to Z	5.918e-03	7.486e-03	8.753e-03	1.029e-02
	C12T28SOI_LL_-NAND2X27_P0	C12T28SOI_LL_-NAND2X42_P0	C12T28SOI_LL_-NAND2X47_P0	C12T28SOI_LL_-NAND2X50_P0
A (output stable)	2.349e-04	3.500e-05	3.682e-05	3.500e-05
B (output stable)	5.240e-04	5.500e-05	5.682e-05	5.500e-05
A to Z	1.283e-02	1.973e-02	2.175e-02	2.243e-02
B to Z	1.142e-02	1.952e-02	2.155e-02	2.222e-02
	C12T28SOI_LL_-NAND2X58_P0	C12T28SOI_LL_-NAND2X67_P0	C12T28SOI_-LLBR0D8_-NAND2X7_P0	C12T28SOI_-LLBR0D8_-NAND2X14_P0
A (output stable)	4.500e-05	3.500e-05	4.245e-05	1.505e-04
B (output stable)	5.500e-05	4.682e-05	6.310e-05	3.779e-04
A to Z	2.600e-02	2.952e-02	3.193e-03	6.403e-03
B to Z	2.578e-02	2.930e-02	2.837e-03	5.594e-03
	C12T28SOI_LLS_-NAND2X40_P0	C12T28SOI_LLS_-NAND2X54_P0		
A (output stable)	3.366e-04	4.307e-04		
B (output stable)	7.243e-04	9.420e-04		
A to Z	1.899e-02	2.529e-02		
B to Z	1.691e-02	2.250e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND2X3_P0	C12T28SOI_LL_-NAND2X5_P0	C12T28SOI_LL_-NAND2X7_P0	C12T28SOI_LL_-NAND2X10_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

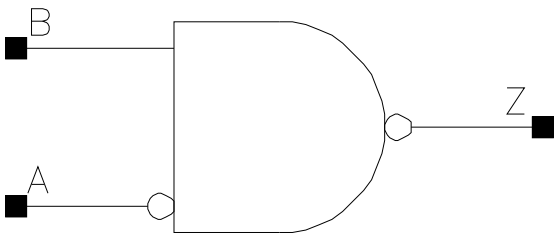
	C12T28SOI_LL_-NAND2X13_P0	C12T28SOI_LL_-NAND2X17_P0	C12T28SOI_LL_-NAND2X20_P0	C12T28SOI_LL_-NAND2X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P0	C12T28SOI_LL_-NAND2X42_P0	C12T28SOI_LL_-NAND2X47_P0	C12T28SOI_LL_-NAND2X50_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P0	C12T28SOI_LL_-NAND2X67_P0	C12T28SOI_-LLBR0D8_-NAND2X7_P0	C12T28SOI_-LLBR0D8_-NAND2X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P0	C12T28SOI_LLS_-NAND2X54_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X7_P0	1.200	0.544	0.6528
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X40_P0	1.200	2.312	2.7744
X54_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P0	X7_P0	X13_P0	X27_P0
A	0.0008	0.0008	0.0011	0.0021
B	0.0006	0.0009	0.0017	0.0034
	X40_P0	X54_P0		
A	0.0031	0.0040		
B	0.0051	0.0069		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0155	0.0166	4.1116	2.2808
A to Z ↑	0.0120	0.0127	3.2168	1.7316
B to Z ↓	0.0071	0.0067	4.2503	2.3419
B to Z ↑	0.0070	0.0055	3.4170	1.8236
	X13_P0	**X27_P0**	**X13_P0**	**X27_P0**

A to Z ↓	0.0154	0.0151	1.2374	0.6133
A to Z ↑	0.0126	0.0123	0.8996	0.4360
B to Z ↓	0.0067	0.0067	1.2707	0.6300
B to Z ↑	0.0047	0.0045	0.9108	0.4526
	X40_P0	**X54_P0**	**X40_P0**	**X54_P0**
A to Z ↓	0.0152	0.0153	0.4083	0.3097
A to Z ↑	0.0127	0.0126	0.2899	0.2193
B to Z ↓	0.0068	0.0068	0.4193	0.3180
B to Z ↑	0.0046	0.0046	0.3049	0.2308

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	3.823e-04	1.000e-20
X7_P0	6.396e-04	1.000e-20
X13_P0	1.401e-03	1.000e-20
X27_P0	2.707e-03	1.000e-20
X40_P0	3.996e-03	1.000e-20
X54_P0	5.284e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	2.283e-03	2.568e-03	4.512e-03	8.979e-03
B (output stable)	2.668e-05	4.836e-05	2.809e-04	4.720e-04
A to Z	3.387e-03	4.503e-03	8.383e-03	1.666e-02
B to Z	1.664e-03	2.969e-03	5.782e-03	1.144e-02
	X40_P0	X54_P0		
A (output stable)	1.340e-02	1.766e-02		
B (output stable)	6.918e-04	8.836e-04		
A to Z	2.494e-02	3.297e-02		
B to Z	1.704e-02	2.250e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

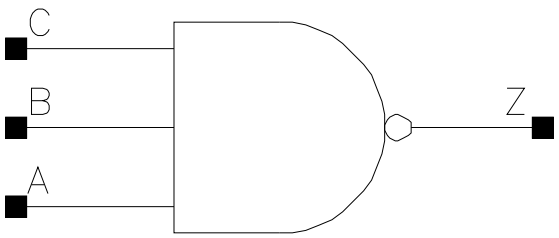
Pin Cycle (vdds)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P0	X54_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P0	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P0	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P0	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P0	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P0	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P0	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P0	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P0	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P0	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P0	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P0	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P0	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P0	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P0	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P0	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P0	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A	0.0007	0.0009	0.0015	0.0018
B	0.0008	0.0009	0.0014	0.0017
C	0.0007	0.0009	0.0014	0.0017
	C12T28SOI_LL_-NAND3X15_P0	C12T28SOI_LL_-NAND3X18_P0	C12T28SOI_LL_-NAND3X21_P0	C12T28SOI_LL_-NAND3X24_P0
A	0.0023	0.0027	0.0033	0.0036
B	0.0022	0.0026	0.0031	0.0035
C	0.0022	0.0025	0.0031	0.0034
	C12T28SOI_LL_-NAND3X35_P0	C12T28SOI_LL_-NAND3X47_P0	C12T28SOI_-LLBR0P6_-NAND3X6_P0	C12T28SOI_-LLBR0P6_-NAND3X12_P0
A	0.0055	0.0074	0.0009	0.0018
B	0.0052	0.0070	0.0010	0.0017
C	0.0051	0.0068	0.0009	0.0017
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	C12T28SOI_-LLBR0P6_-NAND3X24_P0	C12T28SOI_-LLBR0P6_-NAND3X35_P0	C12T28SOI_-LLBR0P6_-NAND3X47_P0
A	0.0027	0.0036	0.0054	0.0072
B	0.0025	0.0034	0.0051	0.0068
C	0.0024	0.0033	0.0050	0.0067
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0			
A	0.0027			
B	0.0027			
C	0.0025			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0
A to Z ↓	0.0093	0.0087	4.2726	3.1030
A to Z ↑	0.0102	0.0089	2.4892	1.7301
B to Z ↓	0.0108	0.0101	4.2972	3.1186
B to Z ↑	0.0095	0.0080	2.4970	1.7359
C to Z ↓	0.0110	0.0105	4.3086	3.1284
C to Z ↑	0.0076	0.0063	2.5048	1.7533

	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A to Z ↓	0.0091	0.0089	2.0927	1.6492
A to Z ↑	0.0094	0.0086	1.1704	0.8921
B to Z ↓	0.0101	0.0099	2.1007	1.6557
B to Z ↑	0.0082	0.0074	1.1750	0.8949
C to Z ↓	0.0103	0.0103	2.1080	1.6612
C to Z ↑	0.0063	0.0055	1.1740	0.8905
	C12T28SOI_LL_-NAND3X15_P0	**C12T28SOI_LL_-NAND3X18_P0**	**C12T28SOI_LL_-NAND3X15_P0**	**C12T28SOI_LL_-NAND3X18_P0**
A to Z ↓	0.0084	0.0084	1.3106	1.1325
A to Z ↑	0.0084	0.0080	0.7074	0.5935
B to Z ↓	0.0098	0.0098	1.3174	1.1381
B to Z ↑	0.0071	0.0067	0.7113	0.5961
C to Z ↓	0.0102	0.0102	1.3226	1.1419
C to Z ↑	0.0055	0.0051	0.7182	0.6021
	C12T28SOI_LL_-NAND3X21_P0	**C12T28SOI_LL_-NAND3X24_P0**	**C12T28SOI_LL_-NAND3X21_P0**	**C12T28SOI_LL_-NAND3X24_P0**
A to Z ↓	0.0087	0.0087	0.9563	0.8616
A to Z ↑	0.0084	0.0082	0.5089	0.4507
B to Z ↓	0.0098	0.0099	0.9603	0.8653
B to Z ↑	0.0072	0.0069	0.5102	0.4519
C to Z ↓	0.0104	0.0104	0.9635	0.8683
C to Z ↑	0.0055	0.0052	0.5124	0.4534
	C12T28SOI_LL_-NAND3X35_P0	**C12T28SOI_LL_-NAND3X47_P0**	**C12T28SOI_LL_-NAND3X35_P0**	**C12T28SOI_LL_-NAND3X47_P0**
A to Z ↓	0.0083	0.0085	0.5872	0.4478
A to Z ↑	0.0079	0.0080	0.3033	0.2300
B to Z ↓	0.0097	0.0099	0.5902	0.4501
B to Z ↑	0.0066	0.0066	0.3038	0.2293
C to Z ↓	0.0102	0.0103	0.5924	0.4519
C to Z ↑	0.0048	0.0047	0.3060	0.2308
	C12T28SOI_-LLBR0P6_-NAND3X6_P0	**C12T28SOI_-LLBR0P6_-NAND3X12_P0**	**C12T28SOI_-LLBR0P6_-NAND3X6_P0**	**C12T28SOI_-LLBR0P6_-NAND3X12_P0**
A to Z ↓	0.0044	0.0047	2.1371	1.1373
A to Z ↑	0.0148	0.0147	2.6432	1.3603
B to Z ↓	0.0052	0.0048	2.1610	1.1492
B to Z ↑	0.0134	0.0126	2.6519	1.3645
C to Z ↓	0.0049	0.0044	2.1816	1.1607
C to Z ↑	0.0106	0.0097	2.6672	1.3700
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	**C12T28SOI_-LLBR0P6_-NAND3X24_P0**	**C12T28SOI_-LLBR0P6_-NAND3X18_P0**	**C12T28SOI_-LLBR0P6_-NAND3X24_P0**
A to Z ↓	0.0041	0.0044	0.7833	0.5963
A to Z ↑	0.0139	0.0141	0.9062	0.6865
B to Z ↓	0.0047	0.0048	0.7918	0.6026
B to Z ↑	0.0118	0.0121	0.9101	0.6884
C to Z ↓	0.0045	0.0046	0.7991	0.6085
C to Z ↑	0.0092	0.0093	0.9171	0.6895
	C12T28SOI_-LLBR0P6_-NAND3X35_P0	**C12T28SOI_-LLBR0P6_-NAND3X47_P0**	**C12T28SOI_-LLBR0P6_-NAND3X35_P0**	**C12T28SOI_-LLBR0P6_-NAND3X47_P0**

A to Z ↓	0.0041	0.0042	0.4084	0.3126
A to Z ↑	0.0142	0.0142	0.4760	0.3613
B to Z ↓	0.0047	0.0048	0.4132	0.3163
B to Z ↑	0.0121	0.0120	0.4764	0.3612
C to Z ↓	0.0045	0.0048	0.4174	0.3191
C to Z ↑	0.0091	0.0093	0.4812	0.3620
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P0**	
A to Z ↓	0.0051		0.7779	
A to Z ↑	0.0141		0.8653	
B to Z ↓	0.0051		0.7850	
B to Z ↑	0.0121		0.8678	
C to Z ↓	0.0048		0.7923	
C to Z ↑	0.0090		0.8609	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P0	2.303e-04	1.000e-20
C12T28SOI_LL_NAND3X6_P0	3.755e-04	1.000e-20
C12T28SOI_LL_NAND3X9_P0	4.970e-04	1.000e-20
C12T28SOI_LL_NAND3X12_P0	7.047e-04	1.000e-20
C12T28SOI_LL_NAND3X15_P0	8.419e-04	1.000e-20
C12T28SOI_LL_NAND3X18_P0	1.020e-03	1.000e-20
C12T28SOI_LL_NAND3X21_P0	1.204e-03	1.000e-20
C12T28SOI_LL_NAND3X24_P0	1.357e-03	1.000e-20
C12T28SOI_LL_NAND3X35_P0	2.009e-03	1.000e-20
C12T28SOI_LL_NAND3X47_P0	2.661e-03	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_P0	2.692e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P0	4.903e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P0	6.899e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P0	9.230e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P0	1.354e-03	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P0	1.785e-03	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P0	8.851e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A (output stable)	3.725e-05	4.912e-05	1.105e-04	1.291e-04
B (output stable)	5.605e-05	7.120e-05	1.564e-04	1.843e-04
C (output stable)	1.889e-04	2.293e-04	3.528e-04	4.114e-04
A to Z	2.851e-03	3.827e-03	5.780e-03	7.267e-03
B to Z	2.633e-03	3.524e-03	5.180e-03	6.528e-03
C to Z	2.395e-03	3.221e-03	4.724e-03	5.986e-03

	C12T28SOI_LL_-NAND3X15_P0	C12T28SOI_LL_-NAND3X18_P0	C12T28SOI_LL_-NAND3X21_P0	C12T28SOI_LL_-NAND3X24_P0
A (output stable)	1.388e-04	1.577e-04	2.210e-04	2.379e-04
B (output stable)	2.028e-04	2.306e-04	3.058e-04	3.347e-04
C (output stable)	4.318e-04	4.879e-04	6.571e-04	7.253e-04
A to Z	8.998e-03	1.044e-02	1.257e-02	1.396e-02
B to Z	8.004e-03	9.236e-03	1.125e-02	1.249e-02
C to Z	7.353e-03	8.505e-03	1.031e-02	1.141e-02
	C12T28SOI_LL_-NAND3X35_P0	C12T28SOI_LL_-NAND3X47_P0	C12T28SOI_-LLBR0P6_-NAND3X6_P0	C12T28SOI_-LLBR0P6_-NAND3X12_P0
A (output stable)	3.252e-04	4.274e-04	6.889e-05	1.820e-04
B (output stable)	4.618e-04	6.081e-04	1.005e-04	2.665e-04
C (output stable)	1.040e-03	1.328e-03	3.040e-04	5.771e-04
A to Z	2.044e-02	2.712e-02	3.767e-03	7.237e-03
B to Z	1.816e-02	2.408e-02	3.376e-03	6.242e-03
C to Z	1.640e-02	2.169e-02	2.946e-03	5.416e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	C12T28SOI_-LLBR0P6_-NAND3X24_P0	C12T28SOI_-LLBR0P6_-NAND3X35_P0	C12T28SOI_-LLBR0P6_-NAND3X47_P0
A (output stable)	2.230e-04	3.340e-04	4.550e-04	5.985e-04
B (output stable)	3.217e-04	4.834e-04	6.518e-04	8.645e-04
C (output stable)	6.538e-04	1.028e-03	1.492e-03	1.915e-03
A to Z	1.023e-02	1.377e-02	2.019e-02	2.649e-02
B to Z	8.779e-03	1.191e-02	1.733e-02	2.279e-02
C to Z	7.763e-03	1.038e-02	1.495e-02	1.975e-02
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0			
A (output stable)	2.673e-04			
B (output stable)	3.970e-04			
C (output stable)	8.261e-04			
A to Z	1.107e-02			
B to Z	9.598e-03			
C to Z	8.389e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P0	C12T28SOI_LL_-NAND3X6_P0	C12T28SOI_LL_-NAND3X9_P0	C12T28SOI_LL_-NAND3X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P0	C12T28SOI_LL_-NAND3X18_P0	C12T28SOI_LL_-NAND3X21_P0	C12T28SOI_LL_-NAND3X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

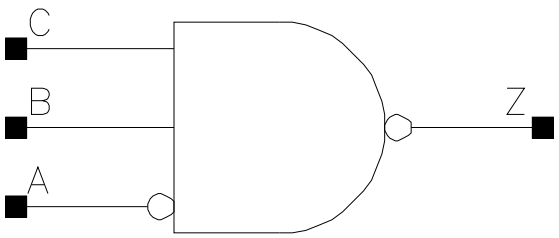
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P0	C12T28SOI_LL_-NAND3X47_P0	C12T28SOI_-LLBR0P6_-NAND3X6_P0	C12T28SOI_-LLBR0P6_-NAND3X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P0	C12T28SOI_-LLBR0P6_-NAND3X24_P0	C12T28SOI_-LLBR0P6_-NAND3X35_P0	C12T28SOI_-LLBR0P6_-NAND3X47_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.816	0.9792
X12_P0	1.200	1.224	1.4688
X18_P0	1.200	1.496	1.7952
X24_P0	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0008	0.0011	0.0011	0.0020
B	0.0009	0.0017	0.0026	0.0035
C	0.0009	0.0017	0.0025	0.0033

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X12_P0**	**X6_P0**	**X12_P0**
A to Z ↓	0.0187	0.0179	3.0762	1.6603
A to Z ↑	0.0134	0.0137	1.6710	0.8423
B to Z ↓	0.0093	0.0095	3.1011	1.6742
B to Z ↑	0.0070	0.0068	1.7461	0.8852
C to Z ↓	0.0101	0.0097	3.1164	1.6794
C to Z ↑	0.0057	0.0048	1.7609	0.8949
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0207	0.0177	1.1330	0.8638

A to Z ↑	0.0160	0.0131	0.5685	0.4274
B to Z ↓	0.0098	0.0096	1.1415	0.8698
B to Z ↑	0.0067	0.0066	0.5972	0.4502
C to Z ↓	0.0104	0.0100	1.1449	0.8727
C to Z ↑	0.0052	0.0047	0.6030	0.4547

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P0	5.541e-04	1.000e-20
X12_P0	1.186e-03	1.000e-20
X18_P0	1.498e-03	1.000e-20
X24_P0	2.293e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	2.506e-03	4.703e-03	5.540e-03	9.158e-03
B (output stable)	5.422e-05	1.561e-04	2.420e-04	3.511e-04
C (output stable)	1.040e-04	4.109e-04	4.923e-04	7.444e-04
A to Z	4.917e-03	9.589e-03	1.329e-02	1.883e-02
B to Z	3.284e-03	6.284e-03	9.266e-03	1.222e-02
C to Z	3.059e-03	5.671e-03	8.541e-03	1.099e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

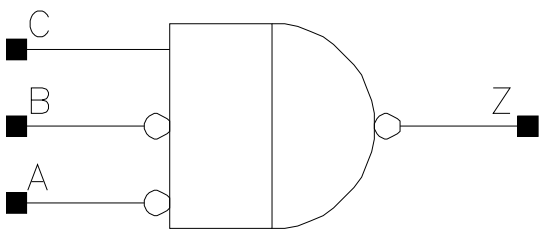
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	0.816	0.9792
X13_P0	1.200	1.088	1.3056
X20_P0	1.200	1.632	1.9584
X27_P0	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P0	X13_P0	X20_P0	X27_P0
A	0.0010	0.0010	0.0020	0.0019
B	0.0011	0.0011	0.0021	0.0020
C	0.0009	0.0017	0.0025	0.0034

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	**X13_P0**	**X7_P0**	**X13_P0**
A to Z ↓	0.0171	0.0207	2.1970	1.1662
A to Z ↑	0.0118	0.0138	1.6647	0.8411
B to Z ↓	0.0185	0.0223	2.1957	1.1663
B to Z ↑	0.0106	0.0129	1.6660	0.8403
C to Z ↓	0.0066	0.0065	2.2503	1.1932
C to Z ↑	0.0054	0.0047	1.7475	0.8902
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0186	0.0200	0.7958	0.6067
A to Z ↑	0.0128	0.0160	0.5697	0.4280
B to Z ↓	0.0194	0.0211	0.7953	0.6064

B to Z ↑	0.0111	0.0148	0.5691	0.4279
C to Z ↓	0.0072	0.0070	0.8148	0.6208
C to Z ↑	0.0052	0.0049	0.6022	0.4526

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X7_P0	7.872e-04	1.000e-20
X13_P0	1.044e-03	1.000e-20
X20_P0	1.738e-03	1.000e-20
X27_P0	1.959e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	1.440e-03	1.702e-03	2.978e-03	3.198e-03
B (output stable)	1.329e-03	1.594e-03	2.810e-03	3.037e-03
C (output stable)	5.265e-05	3.194e-04	3.125e-04	3.891e-04
A to Z	6.232e-03	9.655e-03	1.516e-02	1.861e-02
B to Z	5.877e-03	9.306e-03	1.413e-02	1.763e-02
C to Z	3.128e-03	5.914e-03	8.868e-03	1.173e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

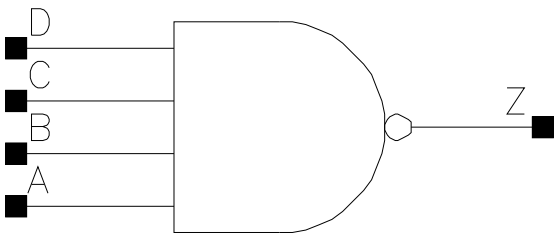
Pin Cycle (vdds)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0007	0.0006	0.0008	0.0010
B	0.0007	0.0007	0.0009	0.0011
C	0.0007	0.0007	0.0009	0.0011
D	0.0007	0.0007	0.0009	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0261	0.0262	1.4091	0.7055
A to Z ↑	0.0221	0.0244	1.7250	0.8505
B to Z ↓	0.0277	0.0282	1.4086	0.7058
B to Z ↑	0.0211	0.0237	1.7290	0.8511
C to Z ↓	0.0272	0.0269	1.4089	0.7055
C to Z ↑	0.0228	0.0252	1.7284	0.8489

D to Z ↓	0.0289	0.0286	1.4089	0.7055
D to Z ↑	0.0220	0.0241	1.7273	0.8496
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0277	0.0261	0.4857	0.3635
A to Z ↑	0.0232	0.0231	0.5761	0.4315
B to Z ↓	0.0293	0.0276	0.4856	0.3634
B to Z ↑	0.0223	0.0221	0.5751	0.4319
C to Z ↓	0.0268	0.0250	0.4859	0.3633
C to Z ↑	0.0233	0.0230	0.5747	0.4310
D to Z ↓	0.0285	0.0266	0.4860	0.3634
D to Z ↑	0.0222	0.0220	0.5749	0.4312

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	7.349e-04	1.000e-20
X17_P0	1.155e-03	1.000e-20
X25_P0	1.677e-03	1.000e-20
X33_P0	2.418e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	1.004e-03	1.145e-03	1.637e-03	2.078e-03
B (output stable)	9.486e-04	1.087e-03	1.556e-03	1.975e-03
C (output stable)	1.011e-03	1.122e-03	1.664e-03	2.037e-03
D (output stable)	9.464e-04	1.060e-03	1.573e-03	1.924e-03
A to Z	6.668e-03	1.036e-02	1.546e-02	1.955e-02
B to Z	6.527e-03	1.022e-02	1.525e-02	1.929e-02
C to Z	6.826e-03	1.031e-02	1.495e-02	1.868e-02
D to Z	6.687e-03	1.015e-02	1.473e-02	1.840e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

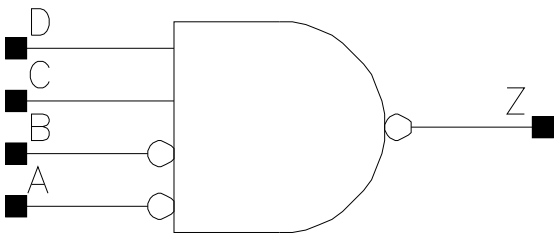
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X12_P0	1.200	1.496	1.7952
X18_P0	1.200	2.040	2.4480
X24_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0010	0.0011	0.0020	0.0019
B	0.0011	0.0015	0.0021	0.0019
C	0.0009	0.0018	0.0025	0.0035
D	0.0009	0.0017	0.0025	0.0035

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X12_P0	X6_P0	X12_P0
A to Z ↓	0.0181	0.0235	3.1690	1.6613
A to Z ↑	0.0124	0.0154	1.6552	0.8387
B to Z ↓	0.0194	0.0252	3.1691	1.6609
B to Z ↑	0.0107	0.0142	1.6572	0.8380
C to Z ↓	0.0094	0.0095	3.1940	1.6740
C to Z ↑	0.0072	0.0068	1.8666	0.8847

D to Z ↓	0.0100	0.0097	3.2080	1.6789
D to Z ↑	0.0059	0.0048	1.8822	0.8940
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0206	0.0225	1.1315	0.8617
A to Z ↑	0.0134	0.0181	0.5668	0.4267
B to Z ↓	0.0214	0.0235	1.1315	0.8615
B to Z ↑	0.0118	0.0166	0.5666	0.4254
C to Z ↓	0.0095	0.0099	1.1391	0.8671
C to Z ↑	0.0065	0.0068	0.5999	0.4480
D to Z ↓	0.0099	0.0103	1.1434	0.8702
D to Z ↑	0.0049	0.0050	0.6151	0.4535

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P0	6.999e-04	1.000e-20
X12_P0	8.970e-04	1.000e-20
X18_P0	1.527e-03	1.000e-20
X24_P0	1.671e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	1.706e-03	2.259e-03	3.781e-03	4.051e-03
B (output stable)	1.588e-03	2.144e-03	3.508e-03	3.801e-03
C (output stable)	6.133e-05	1.689e-04	2.431e-04	3.371e-04
D (output stable)	1.186e-04	4.316e-04	5.173e-04	7.839e-04
A to Z	6.192e-03	1.045e-02	1.597e-02	2.017e-02
B to Z	5.926e-03	1.006e-02	1.497e-02	1.914e-02
C to Z	3.171e-03	6.290e-03	9.092e-03	1.245e-02
D to Z	2.960e-03	5.672e-03	8.351e-03	1.127e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

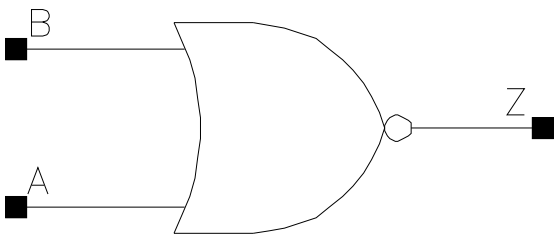
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.408	0.4896
X5_P0	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X10_P0	1.200	0.680	0.8160
X14_P0	1.200	0.680	0.8160
X17_P0	1.200	0.952	1.1424
X21_P0	1.200	0.952	1.1424
X24_P0	1.200	1.224	1.4688
X27_P0	1.200	1.224	1.4688
X34_P0	1.200	1.496	1.7952
X40_P0	1.200	1.360	1.6320
X41_P0	1.200	1.768	2.1216
X49_P0	1.200	1.496	1.7952
X53_P0	1.200	1.904	2.2848
X55_P0	1.200	2.312	2.7744
X57_P0	1.200	1.904	2.2848
X65_P0	1.200	2.040	2.4480
X84_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P0	X5_P0	X7_P0	X10_P0
A	0.0006	0.0007	0.0009	0.0015
B	0.0006	0.0007	0.0009	0.0013
	X14_P0	X17_P0	X21_P0	X24_P0

A	0.0018	0.0023	0.0027	0.0031
B	0.0017	0.0022	0.0026	0.0031
	X27_P0	X34_P0	X40_P0	X41_P0
A	0.0036	0.0045	0.0010	0.0055
B	0.0034	0.0042	0.0011	0.0052
	X49_P0	X53_P0	X55_P0	X57_P0
A	0.0010	0.0011	0.0072	0.0011
B	0.0011	0.0010	0.0069	0.0010
	X65_P0	X84_P0		
A	0.0011	0.0011		
B	0.0010	0.0011		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X5_P0**	**X3_P0**	**X5_P0**
A to Z ↓	0.0041	0.0039	2.7849	2.0249
A to Z ↑	0.0098	0.0091	6.0587	4.4773
B to Z ↓	0.0030	0.0026	2.8544	2.0444
B to Z ↑	0.0109	0.0101	6.1042	4.5024
	X7_P0	**X10_P0**	**X7_P0**	**X10_P0**
A to Z ↓	0.0041	0.0040	1.4941	0.9650
A to Z ↑	0.0083	0.0087	3.1894	2.1379
B to Z ↓	0.0027	0.0020	1.5172	0.9772
B to Z ↑	0.0094	0.0090	3.2092	2.1455
	X14_P0	**X17_P0**	**X14_P0**	**X17_P0**
A to Z ↓	0.0042	0.0041	0.7380	0.5902
A to Z ↑	0.0082	0.0083	1.5980	1.2839
B to Z ↓	0.0021	0.0026	0.7475	0.5965
B to Z ↑	0.0085	0.0092	1.6048	1.2908
	X21_P0	**X24_P0**	**X21_P0**	**X24_P0**
A to Z ↓	0.0043	0.0040	0.5031	0.4276
A to Z ↑	0.0080	0.0081	1.0770	0.9415
B to Z ↓	0.0027	0.0022	0.5084	0.4327
B to Z ↑	0.0089	0.0088	1.0829	0.9465
	X27_P0	**X34_P0**	**X27_P0**	**X34_P0**
A to Z ↓	0.0041	0.0044	0.3811	0.3073
A to Z ↑	0.0078	0.0081	0.8350	0.6638
B to Z ↓	0.0022	0.0026	0.3859	0.3107
B to Z ↑	0.0085	0.0088	0.8398	0.6678
	X40_P0	**X41_P0**	**X40_P0**	**X41_P0**
A to Z ↓	0.0193	0.0043	0.2973	0.2561
A to Z ↑	0.0251	0.0077	0.3530	0.5492
B to Z ↓	0.0183	0.0024	0.2973	0.2592
B to Z ↑	0.0268	0.0084	0.3529	0.5524
	X49_P0	**X53_P0**	**X49_P0**	**X53_P0**
A to Z ↓	0.0201	0.0212	0.2471	0.2266
A to Z ↑	0.0260	0.0292	0.2933	0.2704
B to Z ↓	0.0190	0.0201	0.2474	0.2268
B to Z ↑	0.0276	0.0308	0.2932	0.2707
	X55_P0	**X57_P0**	**X55_P0**	**X57_P0**
A to Z ↓	0.0044	0.0215	0.1936	0.2130
A to Z ↑	0.0078	0.0294	0.4147	0.2520

B to Z ↓	0.0025	0.0203	0.1963	0.2131
B to Z ↑	0.0085	0.0309	0.4173	0.2521
	X65_P0	**X84_P0**	**X65_P0**	**X84_P0**
A to Z ↓	0.0221	0.0232	0.1865	0.1477
A to Z ↑	0.0302	0.0308	0.2206	0.1764
B to Z ↓	0.0210	0.0220	0.1866	0.1477
B to Z ↑	0.0317	0.0324	0.2207	0.1764

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	1.982e-04	1.000e-20
X5_P0	3.058e-04	1.000e-20
X7_P0	4.712e-04	1.000e-20
X10_P0	6.626e-04	1.000e-20
X14_P0	9.461e-04	1.000e-20
X17_P0	1.139e-03	1.000e-20
X21_P0	1.388e-03	1.000e-20
X24_P0	1.618e-03	1.000e-20
X27_P0	1.829e-03	1.000e-20
X34_P0	2.272e-03	1.000e-20
X40_P0	4.098e-03	1.000e-20
X41_P0	2.715e-03	1.000e-20
X49_P0	4.705e-03	1.000e-20
X53_P0	5.289e-03	1.000e-20
X55_P0	3.599e-03	1.000e-20
X57_P0	5.674e-03	1.000e-20
X65_P0	6.284e-03	1.000e-20
X84_P0	7.267e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	3.113e-05	4.380e-05	6.074e-05	1.554e-04
B (output stable)	3.990e-05	5.140e-05	6.939e-05	3.270e-04
A to Z	1.753e-03	2.307e-03	3.196e-03	4.893e-03
B to Z	1.568e-03	2.059e-03	2.808e-03	4.203e-03
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	1.863e-04	2.230e-04	2.517e-04	3.100e-04
B (output stable)	3.771e-04	3.816e-04	3.919e-04	5.304e-04
A to Z	6.402e-03	8.019e-03	9.417e-03	1.101e-02
B to Z	5.521e-03	7.032e-03	8.253e-03	9.563e-03
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	3.433e-04	4.085e-04	6.500e-05	5.148e-04
B (output stable)	5.755e-04	6.000e-04	7.500e-05	8.905e-04
A to Z	1.225e-02	1.542e-02	1.944e-02	1.845e-02
B to Z	1.062e-02	1.345e-02	1.914e-02	1.594e-02
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	6.000e-05	6.500e-05	6.704e-04	6.500e-05
B (output stable)	7.182e-05	8.000e-05	1.051e-03	7.500e-05
A to Z	2.228e-02	2.732e-02	2.445e-02	2.843e-02
B to Z	2.197e-02	2.697e-02	2.109e-02	2.808e-02
	X65_P0	X84_P0		

A (output stable)	7.318e-05	7.000e-05		
B (output stable)	7.364e-05	7.182e-05		
A to Z	3.139e-02	3.806e-02		
B to Z	3.106e-02	3.772e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

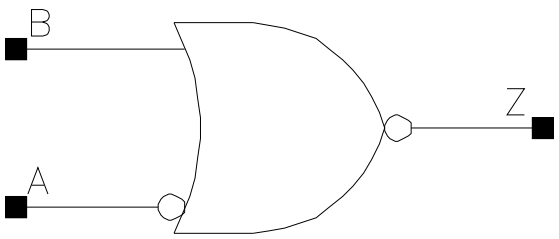
Pin Cycle (vdds)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P0	X84_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X7_P0	1.200	0.680	0.8160
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X41_P0	1.200	2.312	2.7744
X55_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X7_P0	X13_P0
A	0.0008	0.0008	0.0008	0.0011
B	0.0006	0.0009	0.0009	0.0017
	X27_P0	X41_P0	X55_P0	
A	0.0021	0.0031	0.0040	
B	0.0034	0.0051	0.0068	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0144	0.0160	2.6001	1.7208
A to Z ↑	0.0131	0.0132	6.0062	3.1717
B to Z ↓	0.0031	0.0041	2.8278	1.8625
B to Z ↑	0.0110	0.0087	6.0892	3.2248

	X7_P0	X13_P0	X7_P0	X13_P0
A to Z ↓	0.0162	0.0144	1.3770	0.7460
A to Z ↑	0.0146	0.0144	3.1625	1.7001
B to Z ↓	0.0029	0.0023	1.4551	0.7869
B to Z ↑	0.0102	0.0094	3.1951	1.7200
	X27_P0	**X41_P0**	**X27_P0**	**X41_P0**
A to Z ↓	0.0141	0.0144	0.3567	0.2417
A to Z ↑	0.0137	0.0141	0.8121	0.5469
B to Z ↓	0.0024	0.0025	0.3885	0.2615
B to Z ↑	0.0088	0.0087	0.8222	0.5535
	X55_P0		**X55_P0**	
A to Z ↓	0.0141		0.1830	
A to Z ↑	0.0138		0.4136	
B to Z ↓	0.0025		0.1982	
B to Z ↑	0.0086		0.4188	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	3.859e-04	1.000e-20
X6_P0	6.518e-04	1.000e-20
X7_P0	7.076e-04	1.000e-20
X13_P0	1.400e-03	1.000e-20
X27_P0	2.759e-03	1.000e-20
X41_P0	4.072e-03	1.000e-20
X55_P0	5.386e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	2.278e-03	2.547e-03	2.661e-03	4.515e-03
B (output stable)	4.002e-05	6.977e-05	1.846e-04	3.226e-04
A to Z	3.339e-03	4.329e-03	4.846e-03	8.345e-03
B to Z	1.570e-03	2.646e-03	3.036e-03	5.487e-03
	X27_P0	X41_P0	X55_P0	
A (output stable)	9.150e-03	1.362e-02	1.791e-02	
B (output stable)	6.330e-04	8.834e-04	1.089e-03	
A to Z	1.689e-02	2.520e-02	3.318e-02	
B to Z	1.097e-02	1.619e-02	2.137e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

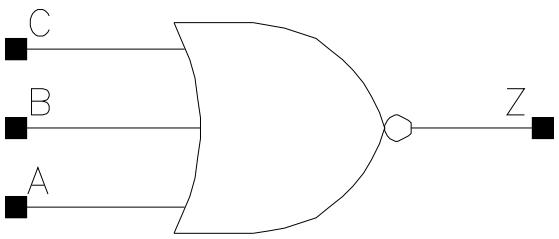
Pin Cycle (vdds)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X41_P0	X55_P0	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X9_P0	1.200	0.952	1.1424
X13_P0	1.200	0.952	1.1424
X16_P0	1.200	1.360	1.6320
X19_P0	1.200	1.496	1.7952
X22_P0	1.200	1.768	2.1216
X25_P0	1.200	1.904	2.2848
X37_P0	1.200	2.584	3.1008
X49_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P0	X6_P0	X9_P0	X13_P0
A	0.0007	0.0009	0.0014	0.0017
B	0.0007	0.0009	0.0016	0.0018
C	0.0007	0.0009	0.0013	0.0016
	X16_P0	X19_P0	X22_P0	X25_P0
A	0.0023	0.0027	0.0032	0.0035
B	0.0023	0.0031	0.0033	0.0041
C	0.0021	0.0025	0.0029	0.0033
	X37_P0	X49_P0		
A	0.0053	0.0072		
B	0.0054	0.0073		

C	0.0049	0.0067		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0049	0.0048	2.0584	1.5203
A to Z ↑	0.0123	0.0112	6.5091	4.6434
B to Z ↓	0.0042	0.0041	2.0670	1.5267
B to Z ↑	0.0132	0.0120	6.5229	4.6539
C to Z ↓	0.0031	0.0029	2.0844	1.5446
C to Z ↑	0.0138	0.0124	6.5380	4.6649
	X9_P0	**X13_P0**	**X9_P0**	**X13_P0**
A to Z ↓	0.0049	0.0050	0.9944	0.7670
A to Z ↑	0.0117	0.0108	3.0920	2.3299
B to Z ↓	0.0041	0.0039	0.9745	0.7387
B to Z ↑	0.0126	0.0117	3.1029	2.3352
C to Z ↓	0.0023	0.0022	0.9863	0.7544
C to Z ↑	0.0121	0.0113	3.0961	2.3340
	X16_P0	**X19_P0**	**X16_P0**	**X19_P0**
A to Z ↓	0.0048	0.0048	0.5952	0.5056
A to Z ↑	0.0114	0.0112	1.8769	1.5606
B to Z ↓	0.0043	0.0042	0.5974	0.4969
B to Z ↑	0.0123	0.0122	1.8814	1.5650
C to Z ↓	0.0026	0.0026	0.6030	0.5161
C to Z ↑	0.0123	0.0118	1.8824	1.5655
	X22_P0	**X25_P0**	**X22_P0**	**X25_P0**
A to Z ↓	0.0049	0.0049	0.4368	0.3847
A to Z ↑	0.0111	0.0110	1.3436	1.1762
B to Z ↓	0.0041	0.0041	0.4307	0.3722
B to Z ↑	0.0120	0.0120	1.3471	1.1790
C to Z ↓	0.0023	0.0024	0.4367	0.3863
C to Z ↑	0.0117	0.0113	1.3468	1.1790
	X37_P0	**X49_P0**	**X37_P0**	**X49_P0**
A to Z ↓	0.0050	0.0051	0.2639	0.1999
A to Z ↑	0.0106	0.0106	0.7900	0.5957
B to Z ↓	0.0042	0.0043	0.2615	0.1982
B to Z ↑	0.0114	0.0114	0.7921	0.5973
C to Z ↓	0.0028	0.0028	0.2651	0.2010
C to Z ↑	0.0115	0.0115	0.7922	0.5978

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	2.432e-04	1.000e-20
X6_P0	3.812e-04	1.000e-20
X9_P0	5.290e-04	1.000e-20
X13_P0	7.731e-04	1.000e-20
X16_P0	9.085e-04	1.000e-20
X19_P0	1.153e-03	1.000e-20
X22_P0	1.296e-03	1.000e-20
X25_P0	1.524e-03	1.000e-20
X37_P0	2.259e-03	1.000e-20

X49_P0	3.001e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	4.311e-05	5.998e-05	1.096e-04	1.424e-04
B (output stable)	5.277e-05	7.292e-05	1.532e-04	1.846e-04
C (output stable)	9.575e-05	1.334e-04	4.067e-04	4.841e-04
A to Z	2.449e-03	3.296e-03	5.093e-03	6.525e-03
B to Z	2.199e-03	2.949e-03	4.607e-03	5.921e-03
C to Z	2.003e-03	2.644e-03	3.991e-03	5.107e-03
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	1.676e-04	2.050e-04	2.419e-04	2.812e-04
B (output stable)	2.340e-04	3.052e-04	3.416e-04	4.144e-04
C (output stable)	5.033e-04	6.648e-04	7.946e-04	9.558e-04
A to Z	8.363e-03	9.994e-03	1.150e-02	1.315e-02
B to Z	7.473e-03	9.019e-03	1.035e-02	1.192e-02
C to Z	6.647e-03	7.755e-03	9.055e-03	1.013e-02
	X37_P0	X49_P0		
A (output stable)	4.092e-04	5.431e-04		
B (output stable)	5.560e-04	7.289e-04		
C (output stable)	1.259e-03	1.637e-03		
A to Z	1.926e-02	2.562e-02		
B to Z	1.729e-02	2.298e-02		
C to Z	1.503e-02	1.996e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

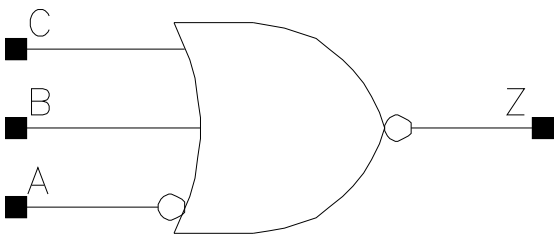
Pin Cycle (vdds)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P0	X49_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.680	0.8160
X13_P0	1.200	1.224	1.4688
X19_P0	1.200	1.496	1.7952
X25_P0	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0008	0.0011	0.0011	0.0021
B	0.0009	0.0018	0.0026	0.0036
C	0.0009	0.0017	0.0025	0.0033

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X13_P0**	**X6_P0**	**X13_P0**
A to Z ↓	0.0160	0.0156	1.4250	0.7874
A to Z ↑	0.0169	0.0170	4.7162	2.3348
B to Z ↓	0.0042	0.0039	1.5309	0.7424
B to Z ↑	0.0122	0.0117	4.7180	2.3363
C to Z ↓	0.0030	0.0022	1.5437	0.7548
C to Z ↑	0.0126	0.0113	4.7284	2.3348
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0172	0.0154	0.4806	0.3659

A to Z ↑	0.0188	0.0171	1.5756	1.1838
B to Z ↓	0.0043	0.0041	0.5142	0.3844
B to Z ↑	0.0117	0.0115	1.5777	1.1845
C to Z ↓	0.0026	0.0023	0.5168	0.3885
C to Z ↑	0.0118	0.0113	1.5797	1.1856

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P0	5.763e-04	1.000e-20
X13_P0	1.269e-03	1.000e-20
X19_P0	1.622e-03	1.000e-20
X25_P0	2.448e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	2.597e-03	4.888e-03	5.508e-03	9.411e-03
B (output stable)	7.377e-05	1.883e-04	2.680e-04	3.661e-04
C (output stable)	1.315e-04	4.953e-04	5.732e-04	8.536e-04
A to Z	4.871e-03	9.715e-03	1.269e-02	1.874e-02
B to Z	2.933e-03	5.945e-03	8.725e-03	1.158e-02
C to Z	2.643e-03	5.107e-03	7.715e-03	1.004e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

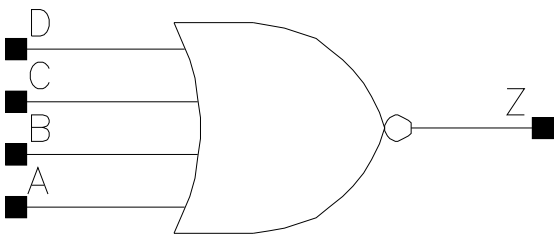
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	1.904	2.2848
X32_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X32_P0
A	0.0007	0.0007	0.0008	0.0009
B	0.0007	0.0007	0.0009	0.0012
C	0.0006	0.0006	0.0008	0.0010
D	0.0007	0.0006	0.0009	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0188	0.0191	1.3960	0.6883
A to Z ↑	0.0274	0.0296	1.7434	0.8687
B to Z ↓	0.0176	0.0181	1.3972	0.6879
B to Z ↑	0.0287	0.0312	1.7427	0.8678
C to Z ↓	0.0185	0.0191	1.3959	0.6868
C to Z ↑	0.0283	0.0308	1.7404	0.8678

D to Z ↓	0.0178	0.0185	1.3941	0.6862
D to Z ↑	0.0298	0.0326	1.7415	0.8672
	X25_P0	**X32_P0**	**X25_P0**	**X32_P0**
A to Z ↓	0.0199	0.0219	0.4770	0.3740
A to Z ↑	0.0292	0.0279	0.5970	0.4493
B to Z ↓	0.0191	0.0210	0.4767	0.3739
B to Z ↑	0.0309	0.0294	0.5968	0.4495
C to Z ↓	0.0194	0.0218	0.4758	0.3732
C to Z ↑	0.0293	0.0287	0.5967	0.4490
D to Z ↓	0.0184	0.0204	0.4756	0.3729
D to Z ↑	0.0309	0.0301	0.5963	0.4483

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.161e-03	1.000e-20
X17_P0	1.999e-03	1.000e-20
X25_P0	3.033e-03	1.000e-20
X32_P0	4.092e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	9.762e-04	1.094e-03	1.541e-03	1.929e-03
B (output stable)	9.085e-04	1.022e-03	1.444e-03	1.801e-03
C (output stable)	9.541e-04	1.032e-03	1.563e-03	1.947e-03
D (output stable)	8.769e-04	9.629e-04	1.459e-03	1.819e-03
A to Z	6.192e-03	9.877e-03	1.477e-02	1.871e-02
B to Z	6.023e-03	9.714e-03	1.453e-02	1.844e-02
C to Z	6.281e-03	9.914e-03	1.423e-02	1.829e-02
D to Z	6.080e-03	9.749e-03	1.398e-02	1.792e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

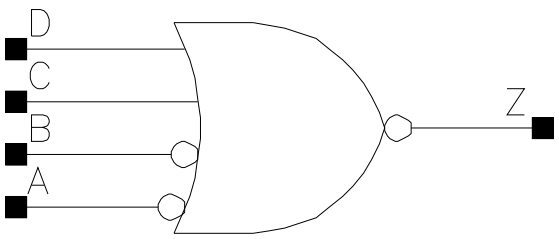
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X13_P0	1.200	1.496	1.7952
X19_P0	1.200	2.040	2.4480
X25_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0011	0.0011	0.0020	0.0020
B	0.0011	0.0015	0.0021	0.0021
C	0.0009	0.0017	0.0025	0.0034
D	0.0009	0.0017	0.0025	0.0033

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X13_P0	X6_P0	X13_P0
A to Z ↓	0.0136	0.0168	1.3860	0.6991
A to Z ↑	0.0172	0.0215	4.5481	2.3876
B to Z ↓	0.0124	0.0160	1.3849	0.6977
B to Z ↑	0.0184	0.0231	4.5476	2.3883
C to Z ↓	0.0046	0.0041	1.5457	0.7453
C to Z ↑	0.0121	0.0122	4.5526	2.3915

D to Z ↓	0.0032	0.0023	1.5521	0.7531
D to Z ↑	0.0125	0.0118	4.5581	2.3907
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0149	0.0163	0.4778	0.3597
A to Z ↑	0.0194	0.0211	1.5809	1.1985
B to Z ↓	0.0133	0.0149	0.4769	0.3594
B to Z ↑	0.0204	0.0225	1.5807	1.1987
C to Z ↓	0.0044	0.0043	0.5148	0.3858
C to Z ↑	0.0117	0.0116	1.5807	1.1992
D to Z ↓	0.0026	0.0024	0.5173	0.3882
D to Z ↑	0.0118	0.0114	1.5821	1.1993

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P0	8.165e-04	1.000e-20
X13_P0	1.128e-03	1.000e-20
X19_P0	1.870e-03	1.000e-20
X25_P0	2.169e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	1.745e-03	2.290e-03	3.869e-03	4.314e-03
B (output stable)	1.650e-03	2.188e-03	3.652e-03	4.125e-03
C (output stable)	8.155e-05	2.147e-04	3.116e-04	4.171e-04
D (output stable)	1.586e-04	5.268e-04	6.592e-04	9.849e-04
A to Z	6.319e-03	1.036e-02	1.619e-02	2.000e-02
B to Z	6.086e-03	9.984e-03	1.537e-02	1.925e-02
C to Z	3.017e-03	5.916e-03	8.636e-03	1.139e-02
D to Z	2.747e-03	5.167e-03	7.726e-03	1.002e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

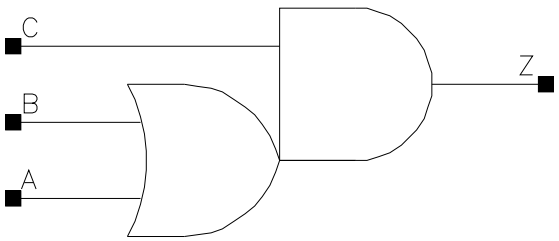
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0010	0.0010	0.0019
B	0.0011	0.0011	0.0022
C	0.0011	0.0011	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0145	0.0170	1.4365	0.7154
A to Z ↑	0.0149	0.0169	1.7609	0.8697
B to Z ↓	0.0157	0.0185	1.4372	0.7154
B to Z ↑	0.0131	0.0154	1.7593	0.8694
C to Z ↓	0.0138	0.0154	1.4253	0.7080
C to Z ↑	0.0132	0.0151	1.7603	0.8701
	X33_P0		**X33_P0**	
A to Z ↓	0.0177		0.3616	
A to Z ↑	0.0184		0.4360	

B to Z ↓	0.0192		0.3611	
B to Z ↑	0.0164		0.4346	
C to Z ↓	0.0159		0.3570	
C to Z ↑	0.0159		0.4354	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.093e-03	1.000e-20
X17_P0	1.674e-03	1.000e-20
X33_P0	3.266e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	9.294e-05	9.206e-05	1.917e-04
B (output stable)	1.005e-04	1.008e-04	2.035e-04
C (output stable)	9.323e-05	9.755e-05	1.868e-04
A to Z	5.638e-03	8.947e-03	1.847e-02
B to Z	5.270e-03	8.540e-03	1.774e-02
C to Z	5.991e-03	8.880e-03	1.829e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

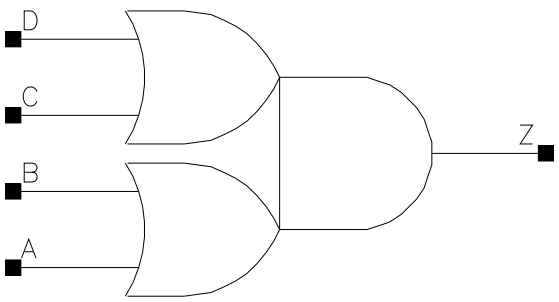
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0007	0.0010	0.0020
B	0.0007	0.0011	0.0020
C	0.0007	0.0010	0.0020
D	0.0007	0.0010	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0246	0.0213	1.3853	0.7077
A to Z ↑	0.0185	0.0172	1.7214	0.8648
B to Z ↓	0.0265	0.0231	1.3853	0.7076
B to Z ↑	0.0176	0.0161	1.7201	0.8636

C to Z ↓	0.0215	0.0188	1.3760	0.7044
C to Z ↑	0.0189	0.0183	1.7177	0.8631
D to Z ↓	0.0229	0.0203	1.3751	0.7043
D to Z ↑	0.0175	0.0165	1.7157	0.8619
	X33_P0		**X33_P0**	
A to Z ↓	0.0216		0.3627	
A to Z ↑	0.0174		0.4353	
B to Z ↓	0.0229		0.3627	
B to Z ↑	0.0159		0.4345	
C to Z ↓	0.0187		0.3608	
C to Z ↑	0.0181		0.4342	
D to Z ↓	0.0198		0.3605	
D to Z ↑	0.0163		0.4334	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	7.283e-04	1.000e-20
X17_P0	1.588e-03	1.000e-20
X33_P0	3.073e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	3.515e-05	5.978e-05	1.574e-04
B (output stable)	3.965e-05	6.505e-05	2.889e-04
C (output stable)	8.380e-05	1.182e-04	2.692e-04
D (output stable)	8.955e-05	1.229e-04	4.072e-04
A to Z	6.015e-03	1.058e-02	2.076e-02
B to Z	5.828e-03	1.019e-02	1.981e-02
C to Z	5.494e-03	9.890e-03	1.933e-02
D to Z	5.298e-03	9.476e-03	1.830e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

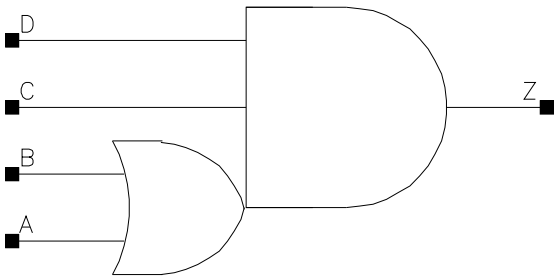
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	1.088	1.3056
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0007	0.0011	0.0017	0.0020
B	0.0007	0.0011	0.0017	0.0021
C	0.0007	0.0010	0.0017	0.0020
D	0.0007	0.0011	0.0017	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0204	0.0190	1.4553	0.7116
A to Z ↑	0.0232	0.0228	1.7808	0.8656
B to Z ↓	0.0220	0.0205	1.4558	0.7112
B to Z ↑	0.0220	0.0208	1.7821	0.8644
C to Z ↓	0.0182	0.0169	1.4350	0.7021

C to Z ↑	0.0200	0.0196	1.7814	0.8646
D to Z ↓	0.0175	0.0162	1.4349	0.7019
D to Z ↑	0.0219	0.0213	1.7798	0.8644
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0199	0.0192	0.4852	0.3629
A to Z ↑	0.0231	0.0241	0.5905	0.4424
B to Z ↓	0.0211	0.0203	0.4850	0.3626
B to Z ↑	0.0211	0.0220	0.5886	0.4414
C to Z ↓	0.0179	0.0172	0.4789	0.3581
C to Z ↑	0.0197	0.0203	0.5894	0.4417
D to Z ↓	0.0169	0.0163	0.4782	0.3578
D to Z ↑	0.0210	0.0217	0.5896	0.4414

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	8.179e-04	1.000e-20
X17_P0	1.790e-03	1.000e-20
X25_P0	2.625e-03	1.000e-20
X33_P0	3.486e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	6.323e-05	1.186e-04	2.051e-04	2.270e-04
B (output stable)	6.583e-05	1.356e-04	2.385e-04	2.625e-04
C (output stable)	2.763e-05	5.531e-05	1.282e-04	1.435e-04
D (output stable)	3.725e-05	7.033e-05	2.170e-04	2.401e-04
A to Z	5.394e-03	1.024e-02	1.593e-02	2.060e-02
B to Z	5.223e-03	9.810e-03	1.513e-02	1.952e-02
C to Z	5.459e-03	1.024e-02	1.624e-02	2.065e-02
D to Z	5.306e-03	9.982e-03	1.559e-02	1.996e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

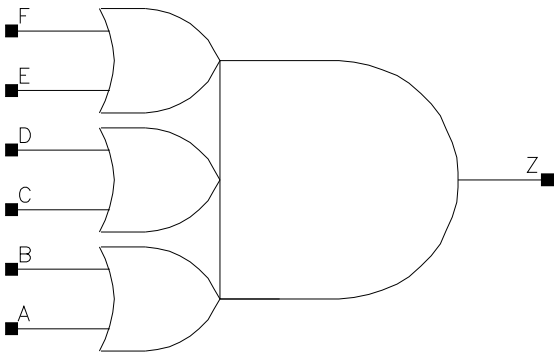
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0007	0.0010	0.0017
B	0.0007	0.0010	0.0020
C	0.0007	0.0010	0.0018
D	0.0007	0.0010	0.0020
E	0.0007	0.0010	0.0018
F	0.0007	0.0010	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0278	0.0240	1.4769	0.7200
A to Z ↑	0.0228	0.0222	1.7676	0.8786
B to Z ↓	0.0297	0.0259	1.4768	0.7202
B to Z ↑	0.0219	0.0213	1.7677	0.8789
C to Z ↓	0.0254	0.0229	1.4687	0.7190
C to Z ↑	0.0244	0.0232	1.7669	0.8781
D to Z ↓	0.0274	0.0246	1.4689	0.7187
D to Z ↑	0.0232	0.0219	1.7661	0.8782
E to Z ↓	0.0222	0.0202	1.4593	0.7152
E to Z ↑	0.0238	0.0231	1.7647	0.8767
F to Z ↓	0.0241	0.0218	1.4593	0.7153
F to Z ↑	0.0226	0.0218	1.7627	0.8764
	X33_P0		X33_P0	
A to Z ↓	0.0243		0.3674	
A to Z ↑	0.0229		0.4425	
B to Z ↓	0.0263		0.3674	
B to Z ↑	0.0211		0.4418	
C to Z ↓	0.0224		0.3656	
C to Z ↑	0.0237		0.4422	
D to Z ↓	0.0242		0.3656	
D to Z ↑	0.0221		0.4411	
E to Z ↓	0.0197		0.3639	
E to Z ↑	0.0238		0.4412	
F to Z ↓	0.0214		0.3637	
F to Z ↑	0.0219		0.4402	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	8.222e-04	1.000e-20
X17_P0	1.855e-03	1.000e-20
X33_P0	3.540e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	3.264e-05	5.669e-05	1.072e-04
B (output stable)	3.671e-05	6.535e-05	1.205e-04
C (output stable)	4.906e-05	8.083e-05	1.604e-04
D (output stable)	5.476e-05	8.754e-05	1.738e-04
E (output stable)	1.244e-04	1.852e-04	3.463e-04
F (output stable)	1.257e-04	1.874e-04	3.580e-04
A to Z	6.752e-03	1.203e-02	2.387e-02
B to Z	6.566e-03	1.171e-02	2.310e-02
C to Z	6.314e-03	1.149e-02	2.253e-02
D to Z	6.136e-03	1.116e-02	2.175e-02
E to Z	5.805e-03	1.076e-02	2.110e-02
F to Z	5.634e-03	1.041e-02	2.033e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

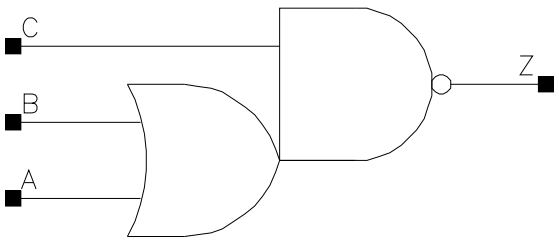
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X34_P0	1.200	2.720	3.2640
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X34_P0	X46_P0
A	0.0008	0.0025	0.0052	0.0069
B	0.0008	0.0024	0.0049	0.0066
C	0.0009	0.0028	0.0057	0.0074

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0083	0.0086	2.5370	0.8288
A to Z ↑	0.0077	0.0081	3.1767	1.0967
B to Z ↓	0.0063	0.0065	2.4824	0.8321
B to Z ↑	0.0088	0.0089	3.1965	1.1050
C to Z ↓	0.0070	0.0070	2.3055	0.7593
C to Z ↑	0.0083	0.0082	1.7965	0.6010
	X34_P0	**X46_P0**	**X34_P0**	**X46_P0**
A to Z ↓	0.0090	0.0090	0.4227	0.3231

A to Z ↑	0.0083	0.0083	0.5487	0.4244
B to Z ↓	0.0069	0.0070	0.4295	0.3297
B to Z ↑	0.0090	0.0092	0.5522	0.4270
C to Z ↓	0.0074	0.0073	0.3897	0.2982
C to Z ↑	0.0084	0.0083	0.3015	0.2316

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P0	5.667e-04	1.000e-20
X17_P0	1.688e-03	1.000e-20
X34_P0	3.328e-03	1.000e-20
X46_P0	4.406e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	8.149e-05	2.761e-04	5.822e-04	7.079e-04
B (output stable)	8.818e-05	3.240e-04	7.114e-04	8.377e-04
C (output stable)	8.651e-05	2.687e-04	5.629e-04	7.115e-04
A to Z	2.970e-03	9.051e-03	1.822e-02	2.383e-02
B to Z	2.676e-03	7.872e-03	1.587e-02	2.073e-02
C to Z	3.532e-03	1.077e-02	2.174e-02	2.842e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

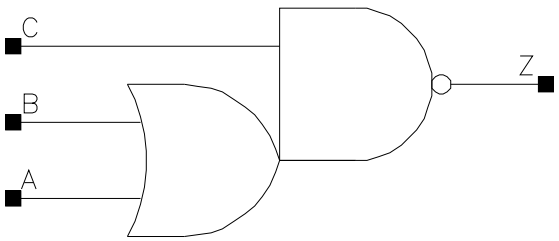
Pin Cycle (vdds)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.544	0.6528
X11_P0	1.200	0.952	1.1424
X17_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X17_P0	X23_P0
A	0.0009	0.0017	0.0026	0.0037
B	0.0008	0.0018	0.0025	0.0034
C	0.0009	0.0018	0.0026	0.0036
	X46_P0			
A	0.0073			
B	0.0068			
C	0.0073			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0071	0.0072	2.5619	1.1962
A to Z ↑	0.0105	0.0105	3.3413	1.5912
B to Z ↓	0.0055	0.0054	2.5197	1.1661

B to Z ↑	0.0117	0.0116	3.3626	1.6005
C to Z ↓	0.0071	0.0071	2.3930	1.1125
C to Z ↑	0.0059	0.0059	1.9323	0.9123
	X17_P0	**X23_P0**	**X17_P0**	**X23_P0**
A to Z ↓	0.0069	0.0074	0.8285	0.6162
A to Z ↑	0.0098	0.0105	1.0543	0.8113
B to Z ↓	0.0053	0.0054	0.8267	0.6174
B to Z ↑	0.0109	0.0114	1.0613	0.8158
C to Z ↓	0.0071	0.0072	0.7805	0.5794
C to Z ↑	0.0052	0.0055	0.6077	0.4640
	X46_P0		**X46_P0**	
A to Z ↓	0.0073		0.3214	
A to Z ↑	0.0102		0.4128	
B to Z ↓	0.0053		0.3186	
B to Z ↑	0.0112		0.4151	
C to Z ↓	0.0074		0.3011	
C to Z ↑	0.0053		0.2356	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	5.499e-04	1.000e-20
X11_P0	1.164e-03	1.000e-20
X17_P0	1.717e-03	1.000e-20
X23_P0	2.260e-03	1.000e-20
X46_P0	4.427e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	3.786e-05	8.251e-05	1.184e-04	2.004e-04
B (output stable)	3.888e-05	8.895e-05	1.240e-04	2.984e-04
C (output stable)	2.274e-04	5.491e-04	6.612e-04	1.043e-03
A to Z	3.214e-03	6.801e-03	9.856e-03	1.356e-02
B to Z	2.892e-03	6.200e-03	8.826e-03	1.192e-02
C to Z	2.970e-03	6.372e-03	9.132e-03	1.251e-02
	X46_P0			
A (output stable)	3.875e-04			
B (output stable)	5.451e-04			
C (output stable)	1.870e-03			
A to Z	2.647e-02			
B to Z	2.318e-02			
C to Z	2.419e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

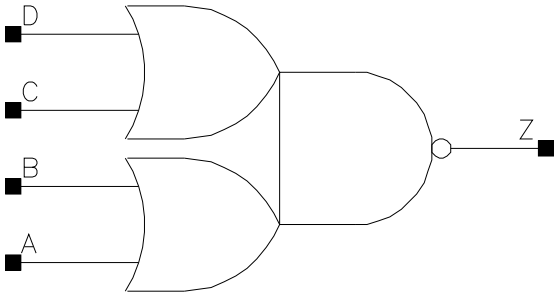
	X46_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0009	0.0017	0.0026	0.0036
B	0.0009	0.0016	0.0024	0.0034
C	0.0008	0.0017	0.0025	0.0035
D	0.0008	0.0016	0.0024	0.0033
	X42_P0			
A	0.0073			
B	0.0068			
C	0.0070			
D	0.0067			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0078	0.0088	2.3657	1.1766
A to Z ↑	0.0127	0.0121	3.5498	1.6291
B to Z ↓	0.0065	0.0070	2.3182	1.1827
B to Z ↑	0.0138	0.0130	3.5662	1.6361
C to Z ↓	0.0081	0.0090	2.4158	1.1905
C to Z ↑	0.0089	0.0089	3.4502	1.6370
D to Z ↓	0.0062	0.0068	2.3499	1.1998
D to Z ↑	0.0099	0.0093	3.4721	1.6474
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0082	0.0085	0.8026	0.5801
A to Z ↑	0.0114	0.0119	1.0985	0.8151
B to Z ↓	0.0067	0.0066	0.8063	0.5809
B to Z ↑	0.0124	0.0129	1.1052	0.8197
C to Z ↓	0.0086	0.0088	0.8153	0.5882
C to Z ↑	0.0081	0.0084	1.1051	0.8176
D to Z ↓	0.0067	0.0067	0.8220	0.5913
D to Z ↑	0.0089	0.0092	1.1138	0.8229
	X42_P0		**X42_P0**	
A to Z ↓	0.0087		0.3048	
A to Z ↑	0.0119		0.4179	
B to Z ↓	0.0068		0.3019	
B to Z ↑	0.0129		0.4202	
C to Z ↓	0.0094		0.3105	
C to Z ↑	0.0085		0.4152	
D to Z ↓	0.0071		0.3075	
D to Z ↑	0.0093		0.4183	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	6.421e-04	1.000e-20
X10_P0	1.409e-03	1.000e-20
X15_P0	2.080e-03	1.000e-20
X21_P0	2.730e-03	1.000e-20
X42_P0	5.369e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	5.382e-05	1.525e-04	1.994e-04	2.850e-04
B (output stable)	5.958e-05	2.780e-04	2.760e-04	4.601e-04
C (output stable)	9.497e-05	2.480e-04	3.165e-04	4.526e-04
D (output stable)	1.044e-04	3.747e-04	3.962e-04	6.146e-04
A to Z	3.503e-03	7.540e-03	1.079e-02	1.492e-02
B to Z	3.192e-03	6.716e-03	9.527e-03	1.327e-02
C to Z	3.000e-03	6.521e-03	9.264e-03	1.275e-02
D to Z	2.703e-03	5.690e-03	8.078e-03	1.120e-02
	X42_P0			
A (output stable)	5.659e-04			
B (output stable)	8.698e-04			
C (output stable)	8.877e-04			
D (output stable)	1.205e-03			

A to Z	2.934e-02			
B to Z	2.606e-02			
C to Z	2.514e-02			
D to Z	2.202e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

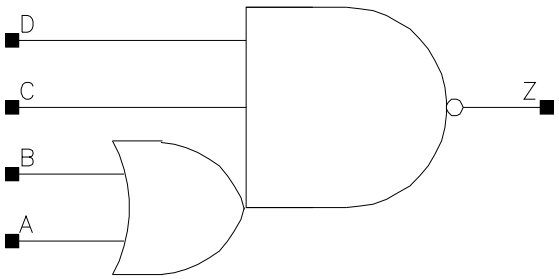
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X21_P0	1.200	2.448	2.9376
X31_P0	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X21_P0	X31_P0
A	0.0009	0.0016	0.0033	0.0050
B	0.0011	0.0016	0.0031	0.0047
C	0.0009	0.0019	0.0037	0.0055
D	0.0009	0.0018	0.0035	0.0053

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0125	0.0123	3.1116	1.6762
A to Z ↑	0.0101	0.0091	3.2027	1.6182
B to Z ↓	0.0108	0.0099	3.1761	1.6867
B to Z ↑	0.0116	0.0096	3.2324	1.6283
C to Z ↓	0.0100	0.0101	2.9430	1.5780

C to Z ↑	0.0100	0.0096	1.7495	0.8858
D to Z ↓	0.0114	0.0111	2.9654	1.5874
D to Z ↑	0.0092	0.0083	1.7808	0.8897
	X21_P0	**X31_P0**	**X21_P0**	**X31_P0**
A to Z ↓	0.0126	0.0128	0.8749	0.5945
A to Z ↑	0.0087	0.0087	0.8094	0.5448
B to Z ↓	0.0102	0.0104	0.8813	0.6011
B to Z ↑	0.0093	0.0093	0.8148	0.5488
C to Z ↓	0.0101	0.0101	0.8246	0.5611
C to Z ↑	0.0093	0.0093	0.4507	0.3061
D to Z ↓	0.0113	0.0115	0.8292	0.5644
D to Z ↑	0.0081	0.0081	0.4526	0.3060

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	4.873e-04	1.000e-20
X10_P0	9.277e-04	1.000e-20
X21_P0	1.793e-03	1.000e-20
X31_P0	2.659e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	1.181e-04	2.471e-04	4.467e-04	6.522e-04
B (output stable)	1.277e-04	2.720e-04	4.863e-04	7.110e-04
C (output stable)	5.146e-05	1.433e-04	2.695e-04	3.948e-04
D (output stable)	6.798e-05	2.377e-04	4.154e-04	5.923e-04
A to Z	3.457e-03	6.341e-03	1.233e-02	1.831e-02
B to Z	3.042e-03	5.508e-03	1.068e-02	1.587e-02
C to Z	4.190e-03	8.015e-03	1.548e-02	2.296e-02
D to Z	3.872e-03	7.240e-03	1.398e-02	2.074e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

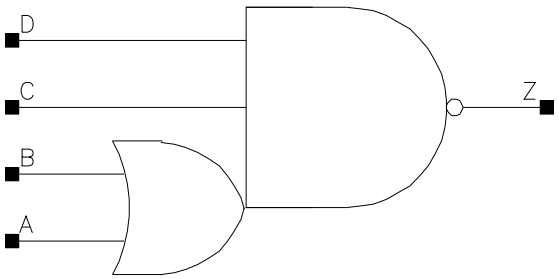
Pin Cycle (vdds)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0009	0.0018	0.0028	0.0036
B	0.0009	0.0017	0.0025	0.0034
C	0.0009	0.0018	0.0027	0.0036
D	0.0009	0.0017	0.0026	0.0034

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0096	0.0105	3.1762	1.6676
A to Z ↑	0.0117	0.0125	3.0721	1.5819
B to Z ↓	0.0080	0.0084	3.1149	1.6722
B to Z ↑	0.0130	0.0134	3.0902	1.5886
C to Z ↓	0.0094	0.0103	2.9987	1.5926

C to Z ↑	0.0073	0.0078	1.7917	0.9083
D to Z ↓	0.0101	0.0109	3.0177	1.5998
D to Z ↑	0.0060	0.0060	1.8098	0.9180
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0102	0.0104	1.1455	0.8667
A to Z ↑	0.0119	0.0122	1.0697	0.8138
B to Z ↓	0.0084	0.0083	1.1408	0.8666
B to Z ↑	0.0130	0.0134	1.0758	0.8181
C to Z ↓	0.0101	0.0104	1.0887	0.8254
C to Z ↑	0.0072	0.0075	0.6082	0.4573
D to Z ↓	0.0107	0.0111	1.0946	0.8292
D to Z ↑	0.0056	0.0058	0.6141	0.4617

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	4.877e-04	1.000e-20
X10_P0	9.328e-04	1.000e-20
X15_P0	1.357e-03	1.000e-20
X21_P0	1.808e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	3.118e-05	6.828e-05	1.009e-04	1.311e-04
B (output stable)	3.154e-05	9.779e-05	1.175e-04	1.719e-04
C (output stable)	7.680e-05	1.719e-04	2.513e-04	3.414e-04
D (output stable)	1.270e-04	4.244e-04	5.012e-04	7.510e-04
A to Z	3.769e-03	7.724e-03	1.113e-02	1.509e-02
B to Z	3.412e-03	6.864e-03	9.837e-03	1.337e-02
C to Z	3.365e-03	6.877e-03	9.845e-03	1.336e-02
D to Z	3.139e-03	6.278e-03	9.085e-03	1.220e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

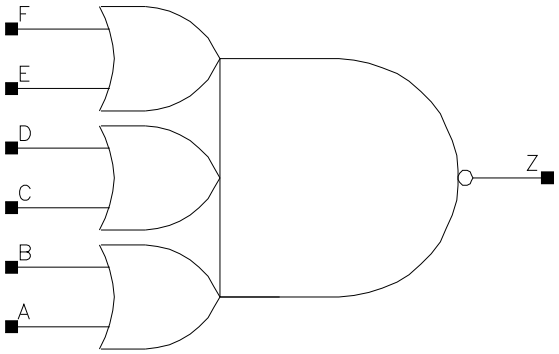
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	1.088	1.3056
X9_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X9_P0
A	0.0007	0.0018
B	0.0007	0.0017
C	0.0007	0.0018
D	0.0007	0.0016
E	0.0007	0.0017
F	0.0007	0.0016

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X9_P0	X3_P0	X9_P0
A to Z ↓	0.0120	0.0135	3.6471	1.5227
A to Z ↑	0.0168	0.0156	4.2943	1.5956
B to Z ↓	0.0109	0.0116	3.6825	1.5270
B to Z ↑	0.0185	0.0168	4.3143	1.6007
C to Z ↓	0.0125	0.0137	3.6926	1.5360
C to Z ↑	0.0144	0.0133	4.3188	1.5927
D to Z ↓	0.0112	0.0118	3.7316	1.5423
D to Z ↑	0.0160	0.0143	4.3416	1.6004
E to Z ↓	0.0118	0.0132	3.7157	1.5393
E to Z ↑	0.0111	0.0101	4.3384	1.5983
F to Z ↓	0.0105	0.0109	3.7633	1.5459
F to Z ↑	0.0124	0.0107	4.3726	1.6090

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	5.330e-04	1.000e-20
X9_P0	1.586e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X9_P0
A (output stable)	4.424e-05	1.455e-04
B (output stable)	4.726e-05	2.256e-04
C (output stable)	6.682e-05	1.920e-04
D (output stable)	6.966e-05	2.761e-04
E (output stable)	1.502e-04	3.855e-04
F (output stable)	1.549e-04	4.613e-04
A to Z	3.711e-03	9.576e-03
B to Z	3.465e-03	8.704e-03
C to Z	3.201e-03	8.318e-03
D to Z	2.977e-03	7.531e-03
E to Z	2.719e-03	7.235e-03
F to Z	2.500e-03	6.406e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

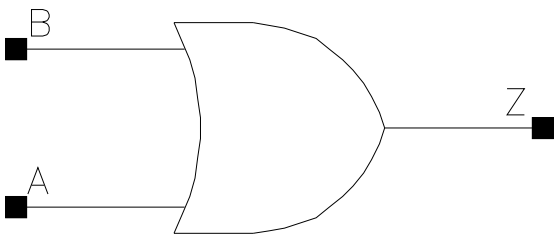
Pin Cycle (vdds)	X3_P0	X9_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X33_P0	1.200	1.360	1.6320
X50_P0	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P0	X16_P0	X33_P0	X50_P0
A	0.0008	0.0010	0.0019	0.0020
B	0.0007	0.0010	0.0020	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0195	0.0170	1.4353	0.7227
A to Z ↑	0.0129	0.0146	1.7237	0.8696
B to Z ↓	0.0209	0.0184	1.4349	0.7223
B to Z ↑	0.0118	0.0134	1.7249	0.8717
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0175	0.0213	0.3580	0.2448
A to Z ↑	0.0146	0.0144	0.4256	0.2889
B to Z ↓	0.0185	0.0226	0.3577	0.2447
B to Z ↑	0.0130	0.0130	0.4256	0.2889

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	5.076e-04	1.000e-20
X16_P0	1.070e-03	1.000e-20
X33_P0	2.122e-03	1.000e-20
X50_P0	2.703e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	3.200e-05	6.314e-05	1.839e-04	1.837e-04
B (output stable)	4.405e-05	7.459e-05	3.879e-04	3.612e-04
A to Z	4.818e-03	8.491e-03	1.759e-02	2.530e-02
B to Z	4.636e-03	8.199e-03	1.662e-02	2.439e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

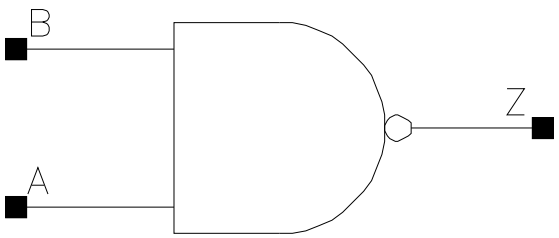
Pin Cycle (vdds)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X16_P0	1.200	0.952	1.1424
X24_P0	1.200	1.088	1.3056
X32_P0	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P0	X16_P0	X24_P0	X32_P0
A	0.0010	0.0010	0.0010	0.0010
B	0.0011	0.0011	0.0011	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0180	0.0186	1.4134	0.7337
A to Z ↑	0.0186	0.0194	1.7659	0.9034
B to Z ↓	0.0195	0.0202	1.4127	0.7336
B to Z ↑	0.0174	0.0177	1.7670	0.9030
	X24_P0	**X32_P0**	**X24_P0**	**X32_P0**
A to Z ↓	0.0205	0.0214	0.4938	0.3685
A to Z ↑	0.0209	0.0210	0.6033	0.4508
B to Z ↓	0.0220	0.0230	0.4938	0.3682
B to Z ↑	0.0192	0.0200	0.6029	0.4507

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	1.357e-03	1.000e-20
X16_P0	1.658e-03	1.000e-20
X24_P0	1.950e-03	1.000e-20
X32_P0	2.837e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	3.455e-05	3.154e-05	3.354e-05	3.182e-05
B (output stable)	4.986e-05	4.636e-05	4.854e-05	5.000e-05
A to Z	8.309e-03	9.879e-03	1.256e-02	1.644e-02
B to Z	8.040e-03	9.637e-03	1.233e-02	1.624e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

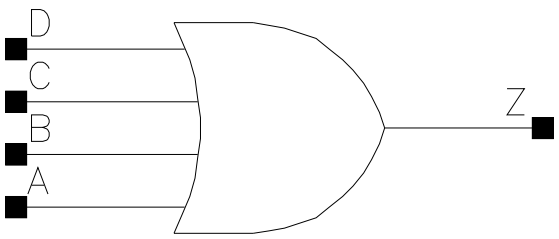
Pin Cycle (vdds)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X27_P0
A	0.0017	0.0020
B	0.0016	0.0020
C	0.0017	0.0020
D	0.0016	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0196	0.0208	0.8026	0.5999
A to Z ↑	0.0143	0.0137	0.5701	0.4240
B to Z ↓	0.0207	0.0218	0.8023	0.5997
B to Z ↑	0.0132	0.0123	0.5707	0.4237
C to Z ↓	0.0195	0.0208	0.8013	0.5984
C to Z ↑	0.0136	0.0137	0.5715	0.4260
D to Z ↓	0.0205	0.0218	0.8007	0.5983
D to Z ↑	0.0125	0.0123	0.5708	0.4254

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X20_P0	1.782e-03	1.000e-20
X27_P0	2.519e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X20_P0	X27_P0
A (output stable)	3.061e-03	4.209e-03
B (output stable)	2.843e-03	3.929e-03
C (output stable)	2.854e-03	4.018e-03
D (output stable)	2.639e-03	3.778e-03
A to Z	1.380e-02	1.916e-02
B to Z	1.312e-02	1.812e-02
C to Z	1.297e-02	1.793e-02
D to Z	1.228e-02	1.702e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

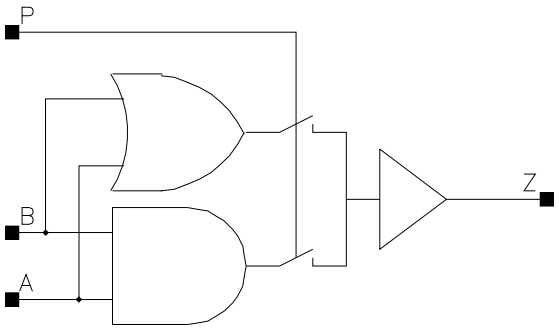
Pin Cycle (vdds)	X20_P0	X27_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X16_P0	1.200	1.224	1.4688
X25_P0	1.200	2.040	2.4480
X33_P0	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0013	0.0018	0.0032	0.0033
B	0.0012	0.0019	0.0037	0.0038
P	0.0007	0.0010	0.0019	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0228	0.0210	1.4552	0.7126
A to Z ↑	0.0171	0.0170	1.7627	0.8798
B to Z ↓	0.0233	0.0217	1.4596	0.7159
B to Z ↑	0.0181	0.0179	1.7615	0.8804
P to Z ↓	0.0225	0.0212	1.4568	0.7137
P to Z ↑	0.0179	0.0178	1.7595	0.8785
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**

A to Z ↓	0.0199	0.0215	0.4850	0.3654
A to Z ↑	0.0165	0.0178	0.5940	0.4436
B to Z ↓	0.0205	0.0220	0.4865	0.3669
B to Z ↑	0.0178	0.0189	0.5946	0.4441
P to Z ↓	0.0206	0.0222	0.4852	0.3656
P to Z ↑	0.0174	0.0186	0.5926	0.4425

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	7.257e-04	1.000e-20
X16_P0	1.613e-03	1.000e-20
X25_P0	2.728e-03	1.000e-20
X33_P0	3.188e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	6.759e-05	1.137e-04	2.445e-04	2.415e-04
B (output stable)	7.893e-05	1.368e-04	3.644e-04	3.576e-04
P (output stable)	1.999e-04	3.428e-04	5.128e-04	5.291e-04
A to Z	5.315e-03	9.886e-03	1.612e-02	1.994e-02
B to Z	5.239e-03	9.861e-03	1.574e-02	1.964e-02
P to Z	5.056e-03	9.562e-03	1.548e-02	1.933e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

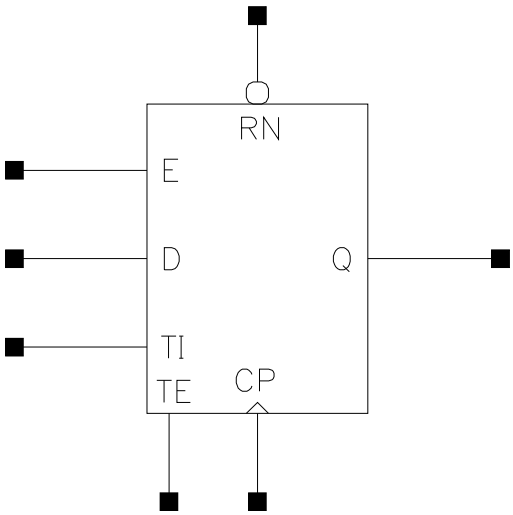
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.488	5.3856
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0010	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0011	0.0011
RN	0.0009	0.0007	0.0008	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
CP to Q ↓	0.0404	0.0239	2.8907	1.4124
CP to Q ↑	0.0374	0.0323	3.4483	1.7443
RN to Q ↓	0.0302	0.0356	2.6807	1.3858
	X17_P0	X33_P0	X17_P0	X33_P0
CP to Q ↓	0.0415	0.0439	0.6977	0.3638
CP to Q ↑	0.0511	0.0538	0.8535	0.4372
RN to Q ↓	0.0486	0.0514	0.6981	0.3638

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0487	0.0364	0.0364	0.0363
CP ↑	min_pulse_width to CP	0.0377	0.0224	0.0189	0.0189
D ↓	hold_rising to CP	-0.0430	-0.0141	-0.0141	-0.0141
D ↑	hold_rising to CP	-0.0359	-0.0051	-0.0051	-0.0051
D ↓	setup_rising to CP	0.0723	0.0435	0.0435	0.0435
D ↑	setup_rising to CP	0.0601	0.0319	0.0319	0.0319
E ↓	hold_rising to CP	-0.0354	-0.0359	-0.0359	-0.0359
E ↑	hold_rising to CP	-0.0310	-0.0016	-0.0016	-0.0016
E ↓	setup_rising to CP	0.0662	0.0657	0.0657	0.0657
E ↑	setup_rising to CP	0.0661	0.0466	0.0466	0.0466
RN ↓	min_pulse_width to RN	0.0403	0.0447	0.0376	0.0376
RN ↑	recovery_rising to CP	0.0071	0.0054	0.0054	0.0054
RN ↑	removal_rising to CP	-0.0024	-0.0008	-0.0008	-0.0008
TE ↓	hold_rising to CP	-0.0159	-0.0071	-0.0066	-0.0066
TE ↑	hold_rising to CP	-0.0186	-0.0114	-0.0114	-0.0114
TE ↓	setup_rising to CP	0.0560	0.0457	0.0457	0.0457
TE ↑	setup_rising to CP	0.0836	0.0591	0.0591	0.0591
TI ↓	hold_rising to CP	-0.0565	-0.0250	-0.0250	-0.0250
TI ↑	hold_rising to CP	-0.0244	-0.0070	-0.0070	-0.0070
TI ↓	setup_rising to CP	0.0868	0.0562	0.0562	0.0562
TI ↑	setup_rising to CP	0.0492	0.0378	0.0378	0.0378

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.965e-03	1.000e-20
X8_P0	2.307e-03	1.000e-20
X17_P0	3.088e-03	1.000e-20
X33_P0	4.295e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

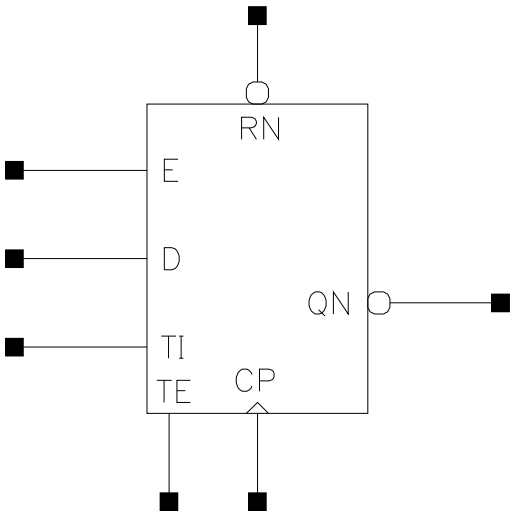
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.421e-02	1.421e-02	1.421e-02	1.420e-02
Clock 100Mhz Data 25Mhz	1.530e-02	1.512e-02	1.610e-02	1.779e-02
Clock 100Mhz Data 50Mhz	1.639e-02	1.603e-02	1.799e-02	2.137e-02
Clock = 0 Data 100Mhz	1.075e-02	9.751e-03	9.418e-03	9.252e-03
Clock = 1 Data 100Mhz	3.026e-03	3.210e-03	3.271e-03	3.301e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.624	5.5488
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0010	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0011	0.0011
RN	0.0009	0.0009	0.0009	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
CP to QN ↓	0.0448	0.0427	2.6087	1.3721
CP to QN ↑	0.0460	0.0323	3.3709	1.6855
RN to QN ↑	0.0377	0.0399	3.3675	1.6860
	X17_P0	X33_P0	X17_P0	X33_P0
CP to QN ↓	0.0413	0.0438	0.6985	0.3634
CP to QN ↑	0.0330	0.0362	0.8544	0.4375
RN to QN ↑	0.0440	0.0464	0.8524	0.4369

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0487	0.0363	0.0364	0.0364
CP ↑	min_pulse_width to CP	0.0283	0.0189	0.0224	0.0224
D ↓	hold_rising to CP	-0.0430	-0.0141	-0.0141	-0.0141
D ↑	hold_rising to CP	-0.0359	-0.0047	-0.0051	-0.0051
D ↓	setup_rising to CP	0.0723	0.0435	0.0435	0.0435
D ↑	setup_rising to CP	0.0606	0.0319	0.0319	0.0319
E ↓	hold_rising to CP	-0.0354	-0.0359	-0.0359	-0.0359
E ↑	hold_rising to CP	-0.0310	-0.0016	-0.0016	-0.0016
E ↓	setup_rising to CP	0.0656	0.0657	0.0657	0.0657
E ↑	setup_rising to CP	0.0661	0.0466	0.0466	0.0466
RN ↓	min_pulse_width to RN	0.0354	0.0376	0.0447	0.0496
RN ↑	recovery_rising to CP	0.0071	0.0075	0.0054	0.0054
RN ↑	removal_rising to CP	-0.0024	-0.0007	-0.0008	-0.0008
TE ↓	hold_rising to CP	-0.0159	-0.0066	-0.0071	-0.0071
TE ↑	hold_rising to CP	-0.0186	-0.0114	-0.0114	-0.0114
TE ↓	setup_rising to CP	0.0560	0.0457	0.0457	0.0457
TE ↑	setup_rising to CP	0.0836	0.0591	0.0591	0.0591
TI ↓	hold_rising to CP	-0.0565	-0.0250	-0.0250	-0.0250
TI ↑	hold_rising to CP	-0.0244	-0.0070	-0.0070	-0.0070
TI ↓	setup_rising to CP	0.0868	0.0562	0.0562	0.0562
TI ↑	setup_rising to CP	0.0492	0.0378	0.0378	0.0378

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.906e-03	1.000e-20
X8_P0	2.123e-03	1.000e-20
X17_P0	2.792e-03	1.000e-20
X33_P0	3.693e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

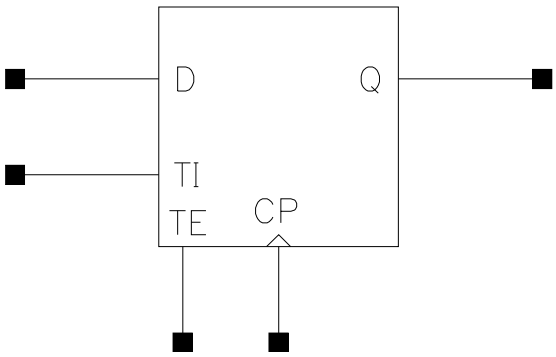
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.421e-02	1.421e-02	1.420e-02	1.419e-02
Clock 100Mhz Data 25Mhz	1.494e-02	1.508e-02	1.613e-02	1.786e-02
Clock 100Mhz Data 50Mhz	1.567e-02	1.595e-02	1.806e-02	2.153e-02
Clock = 0 Data 100Mhz	1.075e-02	9.758e-03	9.424e-03	9.259e-03
Clock = 1 Data 100Mhz	3.022e-03	3.206e-03	3.269e-03	3.303e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.400	4.0800
X8_P0	1.200	3.128	3.7536
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0340	0.0224	2.7676	1.4207
CP to Q ↑	0.0335	0.0294	3.4639	1.7156
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0343	0.0375	0.6897	0.3587
CP to Q ↑	0.0480	0.0512	0.8562	0.4380

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0481	0.0473	0.0473	0.0473
CP ↑	min_pulse_width to CP	0.0283	0.0189	0.0190	0.0190
D ↓	hold_rising to CP	-0.0262	-0.0049	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0061	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0506	0.0315	0.0315	0.0315
D ↑	setup_rising to CP	0.0342	0.0168	0.0168	0.0168
TE ↓	hold_rising to CP	-0.0163	0.0005	0.0005	0.0005
TE ↑	hold_rising to CP	-0.0110	-0.0017	-0.0017	-0.0017
TE ↓	setup_rising to CP	0.0408	0.0311	0.0311	0.0311
TE ↑	setup_rising to CP	0.0787	0.0612	0.0586	0.0612
TI ↓	hold_rising to CP	-0.0563	-0.0305	-0.0305	-0.0305
TI ↑	hold_rising to CP	-0.0146	-0.0021	-0.0021	-0.0021
TI ↓	setup_rising to CP	0.0812	0.0603	0.0603	0.0603
TI ↑	setup_rising to CP	0.0394	0.0286	0.0286	0.0286

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.575e-03	1.000e-20
X8_P0	1.937e-03	1.000e-20
X17_P0	2.905e-03	1.000e-20
X33_P0	3.767e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

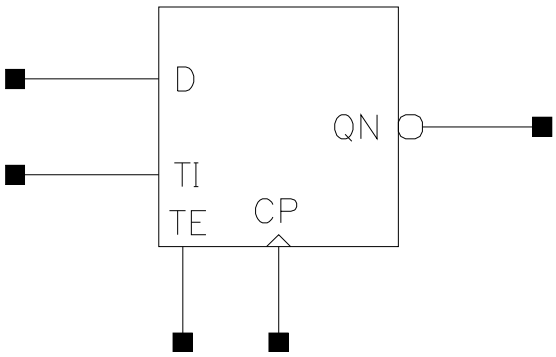
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.309e-02	1.316e-02	1.318e-02	1.319e-02
Clock 100Mhz Data 25Mhz	1.313e-02	1.311e-02	1.416e-02	1.566e-02
Clock 100Mhz Data 50Mhz	1.317e-02	1.305e-02	1.514e-02	1.813e-02
Clock = 0 Data 100Mhz	8.387e-03	7.686e-03	7.454e-03	7.343e-03
Clock = 1 Data 100Mhz	1.793e-03	9.303e-04	6.416e-04	4.983e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.536	4.2432
X8_P0	1.200	3.264	3.9168
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0415	0.0435	2.9706	1.3983
CP to QN ↑	0.0370	0.0299	3.4309	1.6884
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0355	0.0392	0.6893	0.3589
CP to QN ↑	0.0291	0.0326	0.8578	0.4388

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0482	0.0473	0.0473	0.0473
CP ↑	min_pulse_width to CP	0.0236	0.0190	0.0189	0.0189
D ↓	hold_rising to CP	-0.0262	-0.0045	-0.0049	-0.0049
D ↑	hold_rising to CP	-0.0061	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0506	0.0315	0.0347	0.0343
D ↑	setup_rising to CP	0.0336	0.0168	0.0168	0.0168
TE ↓	hold_rising to CP	-0.0163	0.0005	0.0005	0.0005
TE ↑	hold_rising to CP	-0.0110	-0.0017	-0.0017	-0.0017
TE ↓	setup_rising to CP	0.0408	0.0311	0.0311	0.0311
TE ↑	setup_rising to CP	0.0787	0.0586	0.0612	0.0612
TI ↓	hold_rising to CP	-0.0570	-0.0305	-0.0305	-0.0305
TI ↑	hold_rising to CP	-0.0146	-0.0021	-0.0021	-0.0021
TI ↓	setup_rising to CP	0.0812	0.0603	0.0603	0.0603
TI ↑	setup_rising to CP	0.0394	0.0286	0.0286	0.0286

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.596e-03	1.000e-20
X8_P0	1.946e-03	1.000e-20
X17_P0	2.874e-03	1.000e-20
X33_P0	3.736e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

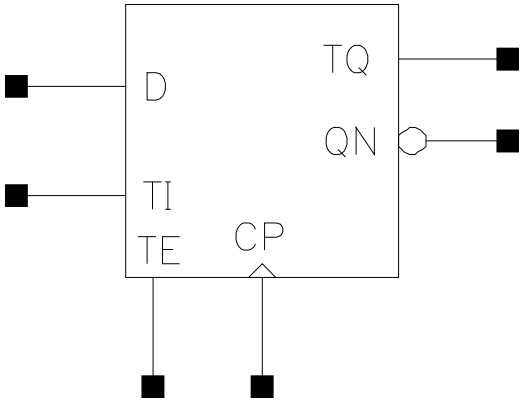
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.299e-02	1.311e-02	1.315e-02	1.317e-02
Clock 100Mhz Data 25Mhz	1.290e-02	1.322e-02	1.412e-02	1.567e-02
Clock 100Mhz Data 50Mhz	1.280e-02	1.333e-02	1.508e-02	1.818e-02
Clock = 0 Data 100Mhz	8.452e-03	7.714e-03	7.475e-03	7.358e-03
Clock = 1 Data 100Mhz	1.782e-03	9.226e-04	6.375e-04	4.942e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.536	4.2432
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0012	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0463	0.0408	2.7085	1.3896
CP to QN ↑	0.0442	0.0305	3.3881	1.6999
CP to TQ ↓	0.0307	0.0202	3.5712	2.5708
CP to TQ ↑	0.0344	0.0292	6.1197	4.4797
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0391	0.0427	0.7017	0.3655
CP to QN ↑	0.0319	0.0345	0.8671	0.4471
CP to TQ ↓	0.0207	0.0214	3.4123	3.4158
CP to TQ ↑	0.0296	0.0304	5.7155	6.0411

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0482	0.0473	0.0473	0.0473
CP ↑	min_pulse_width to CP	0.0283	0.0189	0.0189	0.0189
D ↓	hold_rising to CP	-0.0266	-0.0049	-0.0049	-0.0049
D ↑	hold_rising to CP	-0.0061	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0506	0.0315	0.0315	0.0315
D ↑	setup_rising to CP	0.0342	0.0168	0.0168	0.0168
TE ↓	hold_rising to CP	-0.0169	0.0005	0.0032	0.0032
TE ↑	hold_rising to CP	-0.0110	-0.0017	-0.0017	-0.0017
TE ↓	setup_rising to CP	0.0408	0.0311	0.0311	0.0311
TE ↑	setup_rising to CP	0.0759	0.0586	0.0586	0.0586
TI ↓	hold_rising to CP	-0.0572	-0.0315	-0.0315	-0.0315
TI ↑	hold_rising to CP	-0.0146	-0.0021	-0.0021	-0.0021
TI ↓	setup_rising to CP	0.0812	0.0603	0.0603	0.0603
TI ↑	setup_rising to CP	0.0394	0.0286	0.0286	0.0286

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.698e-03	1.000e-20
X8_P0	2.150e-03	1.000e-20
X17_P0	2.699e-03	1.000e-20
X33_P0	3.683e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0

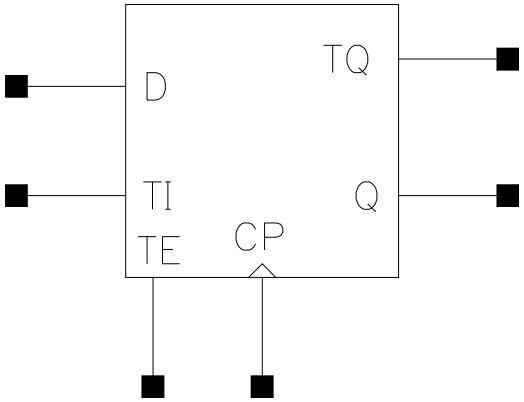
Clock 100Mhz Data 0Mhz	1.323e-02	1.323e-02	1.324e-02	1.324e-02
Clock 100Mhz Data 25Mhz	1.349e-02	1.364e-02	1.426e-02	1.610e-02
Clock 100Mhz Data 50Mhz	1.376e-02	1.404e-02	1.528e-02	1.896e-02
Clock = 0 Data 100Mhz	8.439e-03	7.730e-03	7.493e-03	7.374e-03
Clock = 1 Data 100Mhz	1.796e-03	9.289e-04	6.420e-04	4.976e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.400	4.0800
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0449	0.0251	2.8630	1.4044
CP to Q ↑	0.0390	0.0315	3.5011	1.7291
CP to TQ ↓	0.0415	0.0247	2.8586	3.4981
CP to TQ ↑	0.0402	0.0343	4.5346	6.1678
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0352	0.0385	0.7067	0.3652
CP to Q ↑	0.0489	0.0520	0.8783	0.4418
CP to TQ ↓	0.0360	0.0393	3.4033	3.4555
CP to TQ ↑	0.0517	0.0561	5.9346	6.0129

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0481	0.0473	0.0473	0.0473
CP ↑	min_pulse_width to CP	0.0377	0.0189	0.0190	0.0190
D ↓	hold_rising to CP	-0.0262	-0.0049	-0.0045	-0.0045
D ↑	hold_rising to CP	-0.0061	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0506	0.0315	0.0315	0.0347
D ↑	setup_rising to CP	0.0342	0.0168	0.0168	0.0168
TE ↓	hold_rising to CP	-0.0163	0.0032	0.0005	0.0005
TE ↑	hold_rising to CP	-0.0110	-0.0017	-0.0017	-0.0017
TE ↓	setup_rising to CP	0.0408	0.0311	0.0311	0.0311
TE ↑	setup_rising to CP	0.0787	0.0586	0.0612	0.0612
TI ↓	hold_rising to CP	-0.0563	-0.0315	-0.0305	-0.0305
TI ↑	hold_rising to CP	-0.0146	-0.0021	-0.0021	-0.0021
TI ↓	setup_rising to CP	0.0812	0.0603	0.0603	0.0603
TI ↑	setup_rising to CP	0.0394	0.0286	0.0286	0.0286

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.722e-03	1.000e-20
X8_P0	2.015e-03	1.000e-20
X17_P0	2.974e-03	1.000e-20
X33_P0	3.834e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

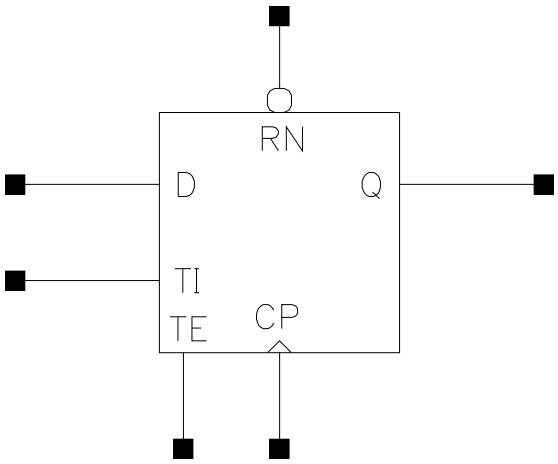
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.304e-02	1.314e-02	1.316e-02	1.318e-02
Clock 100Mhz Data 25Mhz	1.411e-02	1.356e-02	1.446e-02	1.610e-02
Clock 100Mhz Data 50Mhz	1.518e-02	1.399e-02	1.576e-02	1.903e-02
Clock = 0 Data 100Mhz	8.386e-03	7.689e-03	7.460e-03	7.345e-03
Clock = 1 Data 100Mhz	1.778e-03	9.225e-04	6.373e-04	4.928e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.672	4.4064
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0010	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
RN	0.0009	0.0007	0.0008	0.0008
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0405	0.0238	2.9095	1.4162
CP to Q ↑	0.0373	0.0317	3.4717	1.7422
RN to Q ↓	0.0302	0.0357	2.6902	1.3909
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0356	0.0391	0.6949	0.3630
CP to Q ↑	0.0454	0.0485	0.8526	0.4372
RN to Q ↓	0.0430	0.0465	0.6955	0.3627

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0495	0.0472	0.0489	0.0489
CP ↑	min_pulse_width to CP	0.0364	0.0189	0.0190	0.0190
D ↓	hold_rising to CP	-0.0218	0.0032	0.0032	0.0032
D ↑	hold_rising to CP	-0.0110	0.0025	0.0025	0.0025
D ↓	setup_rising to CP	0.0516	0.0294	0.0294	0.0294
D ↑	setup_rising to CP	0.0390	0.0223	0.0217	0.0217
RN ↓	min_pulse_width to RN	0.0376	0.0425	0.0376	0.0376
RN ↑	recovery_rising to CP	0.0103	0.0075	0.0075	0.0075
RN ↑	removal_rising to CP	-0.0024	-0.0008	-0.0008	-0.0008
TE ↓	hold_rising to CP	-0.0114	0.0080	0.0080	0.0080
TE ↑	hold_rising to CP	-0.0213	-0.0092	-0.0088	-0.0088
TE ↓	setup_rising to CP	0.0457	0.0360	0.0359	0.0359
TE ↑	setup_rising to CP	0.0710	0.0547	0.0543	0.0543
TI ↓	hold_rising to CP	-0.0465	-0.0217	-0.0217	-0.0217
TI ↑	hold_rising to CP	-0.0195	-0.0085	-0.0085	-0.0085
TI ↓	setup_rising to CP	0.0763	0.0565	0.0565	0.0562
TI ↑	setup_rising to CP	0.0492	0.0375	0.0375	0.0375

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.845e-03	1.000e-20
X8_P0	2.122e-03	1.000e-20
X17_P0	3.056e-03	1.000e-20
X33_P0	4.116e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.417e-02	1.420e-02	1.427e-02	1.430e-02

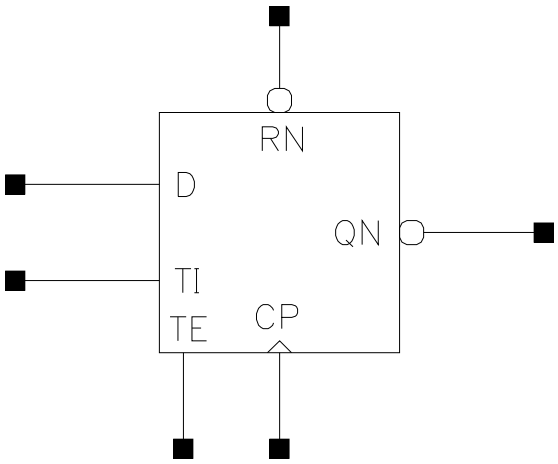
Clock 100Mhz Data 25Mhz	1.442e-02	1.409e-02	1.509e-02	1.663e-02
Clock 100Mhz Data 50Mhz	1.468e-02	1.398e-02	1.592e-02	1.897e-02
Clock = 0 Data 100Mhz	8.016e-03	7.210e-03	6.948e-03	6.818e-03
Clock = 1 Data 100Mhz	1.823e-03	9.452e-04	6.538e-04	5.067e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	3.944	4.7328
X33_P0	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
RN	0.0009	0.0009	0.0009	0.0009
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0408	0.0383	2.5850	1.3520
CP to QN ↑	0.0419	0.0288	3.3800	1.6746
RN to QN ↑	0.0339	0.0364	3.3761	1.6768
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0385	0.0424	0.6948	0.3627
CP to QN ↑	0.0315	0.0352	0.8638	0.4433
RN to QN ↑	0.0428	0.0461	0.8619	0.4426

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0495	0.0472	0.0473	0.0473
CP ↑	min_pulse_width to CP	0.0271	0.0190	0.0189	0.0224
D ↓	hold_rising to CP	-0.0213	0.0032	0.0058	0.0058
D ↑	hold_rising to CP	-0.0110	0.0025	0.0025	0.0025
D ↓	setup_rising to CP	0.0516	0.0294	0.0294	0.0294
D ↑	setup_rising to CP	0.0390	0.0217	0.0217	0.0217
RN ↓	min_pulse_width to RN	0.0354	0.0354	0.0447	0.0447
RN ↑	recovery_rising to CP	0.0071	0.0075	0.0075	0.0075
RN ↑	removal_rising to CP	-0.0024	-0.0034	-0.0007	-0.0007
TE ↓	hold_rising to CP	-0.0114	0.0080	0.0080	0.0080
TE ↑	hold_rising to CP	-0.0213	-0.0092	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0457	0.0360	0.0360	0.0360
TE ↑	setup_rising to CP	0.0710	0.0547	0.0543	0.0543
TI ↓	hold_rising to CP	-0.0465	-0.0217	-0.0202	-0.0202
TI ↑	hold_rising to CP	-0.0195	-0.0085	-0.0085	-0.0085
TI ↓	setup_rising to CP	0.0763	0.0565	0.0565	0.0565
TI ↑	setup_rising to CP	0.0492	0.0375	0.0375	0.0375

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.803e-03	1.000e-20
X8_P0	1.937e-03	1.000e-20
X17_P0	2.870e-03	1.000e-20
X33_P0	3.527e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.408e-02	1.415e-02	1.418e-02	1.419e-02

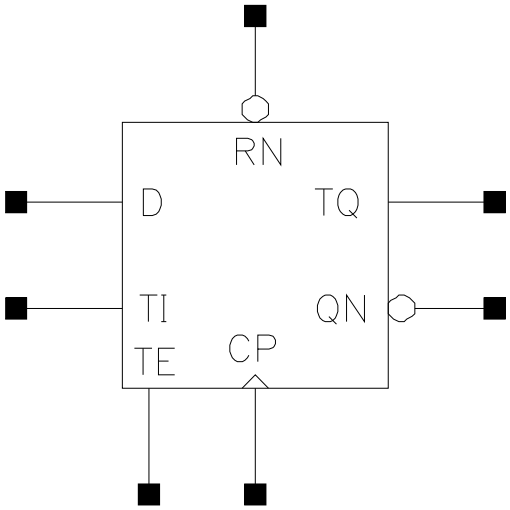
Clock 100Mhz Data 25Mhz	1.389e-02	1.389e-02	1.511e-02	1.671e-02
Clock 100Mhz Data 50Mhz	1.371e-02	1.363e-02	1.604e-02	1.923e-02
Clock = 0 Data 100Mhz	8.000e-03	7.199e-03	6.939e-03	6.810e-03
Clock = 1 Data 100Mhz	1.823e-03	9.450e-04	6.514e-04	5.055e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

RN	0.0010	0.0007	0.0008	0.0008
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0456	0.0399	2.5898	1.4294
CP to QN ↑	0.0536	0.0319	3.0376	1.7439
CP to TQ ↓	0.0373	0.0212	3.1215	2.6802
CP to TQ ↑	0.0386	0.0317	5.0625	4.7093
RN to QN ↑	0.0395	0.0409	3.0755	1.7371
RN to TQ ↓	0.0291	0.0272	2.8753	2.7412
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0415	0.0453	0.7077	0.3704
CP to QN ↑	0.0325	0.0345	0.8781	0.4452
CP to TQ ↓	0.0221	0.0227	3.3332	3.2591
CP to TQ ↑	0.0315	0.0322	4.4501	4.5269
RN to QN ↑	0.0425	0.0454	0.8751	0.4435
RN to TQ ↓	0.0295	0.0351	3.3854	3.2088

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0495	0.0472	0.0489	0.0489
CP ↑	min_pulse_width to CP	0.0377	0.0189	0.0189	0.0189
D ↓	hold_rising to CP	-0.0218	0.0032	0.0032	0.0058
D ↑	hold_rising to CP	-0.0110	0.0025	0.0025	0.0025
D ↓	setup_rising to CP	0.0516	0.0294	0.0294	0.0294
D ↑	setup_rising to CP	0.0390	0.0217	0.0217	0.0217
RN ↓	min_pulse_width to RN	0.0398	0.0398	0.0425	0.0447
RN ↑	recovery_rising to CP	0.0124	0.0075	0.0075	0.0075
RN ↑	removal_rising to CP	-0.0076	-0.0007	-0.0007	-0.0007
TE ↓	hold_rising to CP	-0.0114	0.0080	0.0080	0.0080
TE ↑	hold_rising to CP	-0.0213	-0.0092	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0457	0.0360	0.0359	0.0359
TE ↑	setup_rising to CP	0.0710	0.0547	0.0543	0.0543
TI ↓	hold_rising to CP	-0.0465	-0.0202	-0.0202	-0.0202
TI ↑	hold_rising to CP	-0.0195	-0.0085	-0.0085	-0.0085
TI ↓	setup_rising to CP	0.0763	0.0565	0.0565	0.0565
TI ↑	setup_rising to CP	0.0492	0.0375	0.0375	0.0375

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	2.060e-03	1.000e-20
X8_P0	2.082e-03	1.000e-20
X17_P0	2.542e-03	1.000e-20
X33_P0	3.348e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

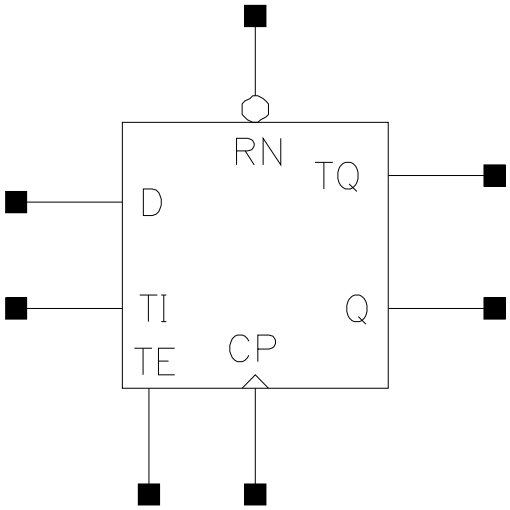
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.409e-02	1.416e-02	1.424e-02	1.428e-02
Clock 100Mhz Data 25Mhz	1.455e-02	1.421e-02	1.502e-02	1.692e-02
Clock 100Mhz Data 50Mhz	1.502e-02	1.427e-02	1.581e-02	1.955e-02
Clock = 0 Data 100Mhz	8.003e-03	7.202e-03	6.939e-03	6.807e-03
Clock = 1 Data 100Mhz	1.825e-03	9.463e-04	6.533e-04	5.067e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

RN	0.0009	0.0009	0.0008	0.0008
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
CP to Q ↓	0.0455	0.0259	3.0525	1.4497
CP to Q ↑	0.0401	0.0333	3.6300	1.8170
CP to TQ ↓	0.0414	0.0246	3.8712	3.5146
CP to TQ ↑	0.0418	0.0350	6.6923	6.1302
RN to Q ↓	0.0327	0.0374	2.8070	1.4208
RN to TQ ↓	0.0300	0.0366	3.5913	3.4530
	X17_P0	X33_P0	X17_P0	X33_P0
CP to Q ↓	0.0371	0.0406	0.7032	0.3672
CP to Q ↑	0.0462	0.0493	0.8588	0.4397
CP to TQ ↓	0.0379	0.0417	3.4201	3.4739
CP to TQ ↑	0.0490	0.0537	6.0294	6.0500
RN to Q ↓	0.0443	0.0478	0.7028	0.3669
RN to TQ ↓	0.0451	0.0489	3.4202	3.4743

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0495	0.0472	0.0472	0.0472
CP ↑	min_pulse_width to CP	0.0424	0.0224	0.0190	0.0190
D ↓	hold_rising to CP	-0.0218	0.0058	0.0032	0.0032
D ↑	hold_rising to CP	-0.0110	0.0025	0.0025	0.0025
D ↓	setup_rising to CP	0.0516	0.0294	0.0294	0.0294
D ↑	setup_rising to CP	0.0385	0.0217	0.0217	0.0217
RN ↓	min_pulse_width to RN	0.0425	0.0474	0.0376	0.0376
RN ↑	recovery_rising to CP	0.0075	0.0075	0.0075	0.0075
RN ↑	removal_rising to CP	-0.0024	-0.0007	-0.0008	-0.0008
TE ↓	hold_rising to CP	-0.0114	0.0080	0.0080	0.0080
TE ↑	hold_rising to CP	-0.0213	-0.0092	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0457	0.0360	0.0360	0.0360
TE ↑	setup_rising to CP	0.0710	0.0547	0.0547	0.0547
TI ↓	hold_rising to CP	-0.0465	-0.0202	-0.0217	-0.0217
TI ↑	hold_rising to CP	-0.0195	-0.0085	-0.0085	-0.0085
TI ↓	setup_rising to CP	0.0763	0.0565	0.0565	0.0565
TI ↑	setup_rising to CP	0.0492	0.0375	0.0375	0.0375

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.908e-03	1.000e-20
X8_P0	2.223e-03	1.000e-20
X17_P0	3.121e-03	1.000e-20
X33_P0	4.182e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

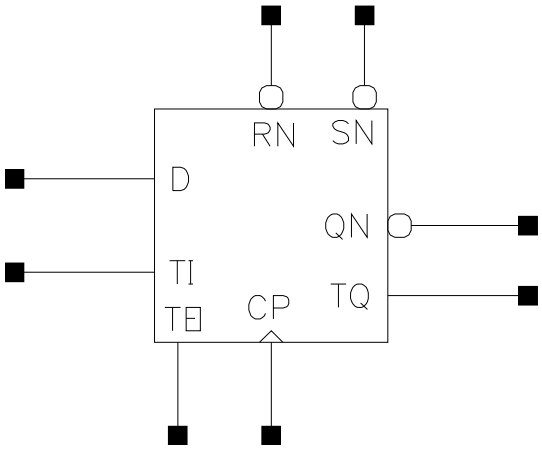
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.414e-02	1.419e-02	1.420e-02	1.420e-02
Clock 100Mhz Data 25Mhz	1.495e-02	1.445e-02	1.535e-02	1.699e-02
Clock 100Mhz Data 50Mhz	1.576e-02	1.471e-02	1.651e-02	1.977e-02
Clock = 0 Data 100Mhz	8.016e-03	7.211e-03	6.941e-03	6.808e-03
Clock = 1 Data 100Mhz	1.827e-03	9.481e-04	6.538e-04	5.064e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.352	5.2224
X17_P0	1.200	4.488	5.3856
X33_P0	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0009

SN	0.0013	0.0013	0.0013
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0447	0.0476	1.3777	0.7058
CP to QN ↑	0.0323	0.0343	1.6871	0.8593
CP to TQ ↓	0.0244	0.0243	4.1775	4.1813
CP to TQ ↑	0.0370	0.0369	7.5867	7.5977
RN to QN ↓	0.0412	0.0446	1.3789	0.7063
RN to QN ↑	0.0372	0.0390	1.6862	0.8589
RN to TQ ↓	0.0299	0.0299	4.1365	4.1387
RN to TQ ↑	0.0327	0.0325	7.6499	7.6610
SN to QN ↓	0.0444	0.0473	1.3782	0.7062
SN to TQ ↑	0.0368	0.0367	7.5781	7.5864
	X33_P0		**X33_P0**	
CP to QN ↓	0.0546		0.3693	
CP to QN ↑	0.0391		0.4412	
CP to TQ ↓	0.0244		4.1923	
CP to TQ ↑	0.0370		7.6157	
RN to QN ↓	0.0523		0.3688	
RN to QN ↑	0.0434		0.4413	
RN to TQ ↓	0.0299		4.1524	
RN to TQ ↑	0.0325		7.6928	
SN to QN ↓	0.0542		0.3696	
SN to TQ ↑	0.0368		7.6065	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0519	0.0519	0.0519
CP ↑	min_pulse_width to CP	0.0224	0.0224	0.0237
D ↓	hold_rising to CP	-0.0000	-0.0000	-0.0000
D ↑	hold_rising to CP	0.0025	0.0025	0.0025
D ↓	setup_rising to CP	0.0315	0.0315	0.0315
D ↑	setup_rising to CP	0.0217	0.0217	0.0217
RN ↓	min_pulse_width to RN	0.0425	0.0447	0.0474
RN ↑	non_seq_hold_rising to SN	-0.0166	-0.0166	-0.0166
RN ↑	non_seq_setup_rising to SN	0.0376	0.0376	0.0376
RN ↑	recovery_rising to CP	0.0145	0.0145	0.0145
RN ↑	removal_rising to CP	-0.0076	-0.0076	-0.0076
SN ↓	min_pulse_width to SN	0.0430	0.0430	0.0452
SN ↑	recovery_rising to CP	0.0010	0.0010	0.0010
SN ↑	removal_rising to CP	0.0209	0.0209	0.0209

TE ↓	hold_rising to CP	0.0080	0.0080	0.0080
TE ↑	hold_rising to CP	-0.0092	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0360	0.0360	0.0360
TE ↑	setup_rising to CP	0.0596	0.0596	0.0596
TI ↓	hold_rising to CP	-0.0208	-0.0208	-0.0208
TI ↑	hold_rising to CP	-0.0085	-0.0085	-0.0085
TI ↓	setup_rising to CP	0.0613	0.0613	0.0613
TI ↑	setup_rising to CP	0.0375	0.0375	0.0375

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	2.340e-03	1.000e-20
X17_P0	2.723e-03	1.000e-20
X33_P0	3.464e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

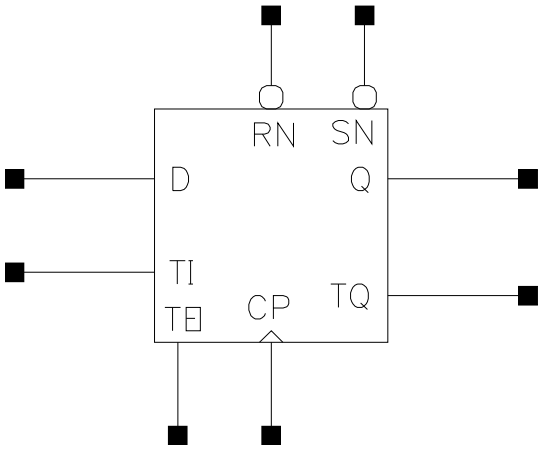
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.480e-02	1.479e-02	1.480e-02
Clock 100Mhz Data 25Mhz	1.464e-02	1.545e-02	1.783e-02
Clock 100Mhz Data 50Mhz	1.449e-02	1.610e-02	2.087e-02
Clock = 0 Data 100Mhz	6.490e-03	6.491e-03	6.491e-03
Clock = 1 Data 100Mhz	6.841e-05	6.557e-05	6.568e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.216	5.0592
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0009

SN	0.0013	0.0013	0.0013
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
CP to Q ↓	0.0280	0.0316	1.4044	0.7237
CP to Q ↑	0.0369	0.0397	1.7373	0.8872
CP to TQ ↓	0.0270	0.0301	4.2350	4.2770
CP to TQ ↑	0.0403	0.0447	7.5349	7.5939
RN to Q ↓	0.0326	0.0347	1.3768	0.7076
RN to Q ↑	0.0379	0.0399	1.7213	0.8784
RN to TQ ↓	0.0319	0.0338	4.1754	4.2010
RN to TQ ↑	0.0410	0.0442	7.4992	7.5530
SN to Q ↑	0.0364	0.0386	1.7270	0.8805
SN to TQ ↑	0.0393	0.0428	7.5151	7.5716
	X33_P0		X33_P0	
CP to Q ↓	0.0404		0.3826	
CP to Q ↑	0.0466		0.4606	
CP to TQ ↓	0.0354		4.4042	
CP to TQ ↑	0.0531		7.6978	
RN to Q ↓	0.0404		0.3711	
RN to Q ↑	0.0451		0.4550	
RN to TQ ↓	0.0370		4.2870	
RN to TQ ↑	0.0501		7.6450	
SN to Q ↑	0.0440		0.4557	
SN to TQ ↑	0.0490		7.6579	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0519	0.0520	0.0520
CP ↑	min_pulse_width to CP	0.0237	0.0271	0.0330
D ↓	hold_rising to CP	-0.0000	-0.0000	-0.0000
D ↑	hold_rising to CP	0.0025	0.0025	0.0057
D ↓	setup_rising to CP	0.0315	0.0315	0.0347
D ↑	setup_rising to CP	0.0217	0.0217	0.0217
RN ↓	min_pulse_width to RN	0.0496	0.0593	0.0762
RN ↑	non_seq_hold_rising to SN	-0.0164	-0.0214	-0.0284
RN ↑	non_seq_setup_rising to SN	0.0354	0.0376	0.0528
RN ↑	recovery_rising to CP	0.0129	0.0125	0.0125
RN ↑	removal_rising to CP	-0.0048	-0.0048	-0.0048
SN ↓	min_pulse_width to SN	0.0452	0.0527	0.0674
SN ↑	recovery_rising to CP	0.0010	0.0010	0.0010
SN ↑	removal_rising to CP	0.0209	0.0209	0.0209

TE ↓	hold_rising to CP	0.0080	0.0080	0.0080
TE ↑	hold_rising to CP	-0.0092	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0360	0.0360	0.0360
TE ↑	setup_rising to CP	0.0596	0.0596	0.0596
TI ↓	hold_rising to CP	-0.0208	-0.0208	-0.0210
TI ↑	hold_rising to CP	-0.0085	-0.0085	-0.0085
TI ↓	setup_rising to CP	0.0613	0.0613	0.0613
TI ↑	setup_rising to CP	0.0375	0.0375	0.0375

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	2.445e-03	1.000e-20
X17_P0	2.950e-03	1.000e-20
X33_P0	3.942e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

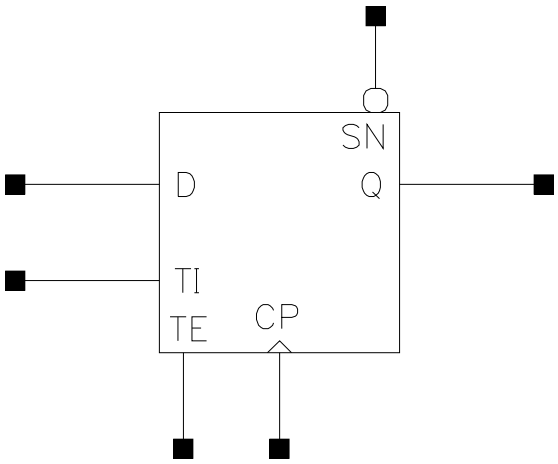
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.479e-02	1.478e-02	1.478e-02
Clock 100Mhz Data 25Mhz	1.484e-02	1.617e-02	1.995e-02
Clock 100Mhz Data 50Mhz	1.490e-02	1.756e-02	2.513e-02
Clock = 0 Data 100Mhz	6.486e-03	6.488e-03	6.491e-03
Clock = 1 Data 100Mhz	6.523e-05	6.682e-05	6.765e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0009	0.0010	0.0010	0.0010
D	0.0008	0.0004	0.0004	0.0004
SN	0.0014	0.0014	0.0014	0.0014
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0010			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0405	0.0245	2.9136	1.4025
CP to Q ↑	0.0388	0.0335	3.4882	1.7271
SN to Q ↑	0.0258	0.0277	3.4005	1.7090
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
CP to Q ↓	0.0350	0.0368	0.6955	0.4799
CP to Q ↑	0.0459	0.0475	0.8514	0.5801
SN to Q ↑	0.0407	0.0423	0.8512	0.5803
	X33_P0		**X33_P0**	
CP to Q ↓	0.0383		0.3633	
CP to Q ↑	0.0488		0.4366	
SN to Q ↑	0.0436		0.4369	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.0552	0.0518	0.0518	0.0518
CP ↑	min_pulse_width to CP	0.0377	0.0189	0.0190	0.0190
D ↓	hold_rising to CP	-0.0208	0.0010	0.0010	0.0010
D ↑	hold_rising to CP	-0.0088	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0506	0.0343	0.0343	0.0343
D ↑	setup_rising to CP	0.0363	0.0168	0.0168	0.0168
SN ↓	min_pulse_width to SN	0.0305	0.0354	0.0305	0.0305
SN ↑	recovery_rising to CP	0.0006	0.0005	-0.0027	-0.0027
SN ↑	removal_rising to CP	0.0140	0.0189	0.0189	0.0189
TE ↓	hold_rising to CP	-0.0142	0.0022	0.0022	0.0022
TE ↑	hold_rising to CP	-0.0159	-0.0039	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0462	0.0343	0.0343	0.0343
TE ↑	setup_rising to CP	0.0787	0.0612	0.0612	0.0612
TI ↓	hold_rising to CP	-0.0514	-0.0264	-0.0256	-0.0256
TI ↑	hold_rising to CP	-0.0195	-0.0037	-0.0037	-0.0037
TI ↓	setup_rising to CP	0.0812	0.0603	0.0603	0.0603
TI ↑	setup_rising to CP	0.0443	0.0319	0.0319	0.0319
		X33_P0			

CP ↓	min_pulse_width to CP	0.0518			
CP ↑	min_pulse_width to CP	0.0190			
D ↓	hold_rising to CP	0.0010			
D ↑	hold_rising to CP	0.0079			
D ↓	setup_rising to CP	0.0343			
D ↑	setup_rising to CP	0.0168			
SN ↓	min_pulse_width to SN	0.0305			
SN ↑	recovery_rising to CP	-0.0027			
SN ↑	removal_rising to CP	0.0189			
TE ↓	hold_rising to CP	0.0022			
TE ↑	hold_rising to CP	-0.0071			
TE ↓	setup_rising to CP	0.0343			
TE ↑	setup_rising to CP	0.0612			
TI ↓	hold_rising to CP	-0.0256			
TI ↑	hold_rising to CP	-0.0037			
TI ↓	setup_rising to CP	0.0603			
TI ↑	setup_rising to CP	0.0319			

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.703e-03	1.000e-20
X8_P0	2.027e-03	1.000e-20
X17_P0	2.932e-03	1.000e-20
X25_P0	3.260e-03	1.000e-20
X33_P0	3.588e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	1.390e-02	1.416e-02	1.425e-02	1.429e-02
Clock 100Mhz Data 25Mhz	1.421e-02	1.421e-02	1.509e-02	1.580e-02
Clock 100Mhz Data 50Mhz	1.453e-02	1.427e-02	1.593e-02	1.730e-02
Clock = 0 Data 100Mhz	7.582e-03	7.038e-03	6.859e-03	6.769e-03
Clock = 1 Data 100Mhz	1.823e-03	9.432e-04	6.494e-04	5.046e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	1.432e-02			

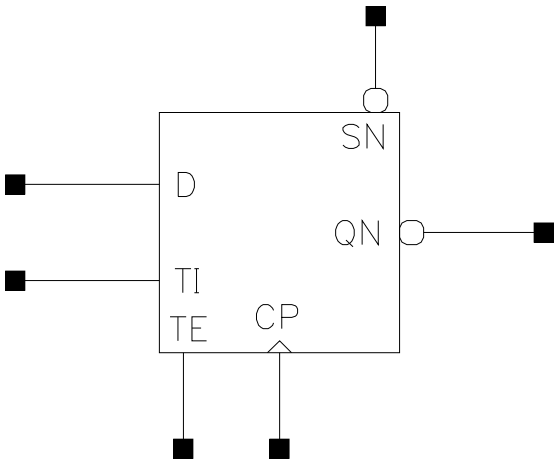
Clock 100Mhz Data 25Mhz	1.660e-02			
Clock 100Mhz Data 50Mhz	1.887e-02			
Clock = 0 Data 100Mhz	6.715e-03			
Clock = 1 Data 100Mhz	4.168e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0009	0.0010	0.0010	0.0010
D	0.0008	0.0004	0.0004	0.0004
SN	0.0014	0.0014	0.0014	0.0014
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0010			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0424	0.0387	2.5859	1.3536
CP to QN ↑	0.0418	0.0283	3.3656	1.6844
SN to QN ↓	0.0310	0.0335	2.5775	1.3549
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
CP to QN ↓	0.0412	0.0434	0.6977	0.4809
CP to QN ↑	0.0331	0.0352	0.8521	0.5805
SN to QN ↓	0.0348	0.0369	0.6961	0.4800
	X33_P0		**X33_P0**	
CP to QN ↓	0.0451		0.3641	
CP to QN ↑	0.0368		0.4363	
SN to QN ↓	0.0385		0.3636	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.0552	0.0518	0.0535	0.0535
CP ↑	min_pulse_width to CP	0.0283	0.0190	0.0189	0.0189
D ↓	hold_rising to CP	-0.0234	0.0010	0.0010	0.0010
D ↑	hold_rising to CP	-0.0088	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0506	0.0343	0.0343	0.0343
D ↑	setup_rising to CP	0.0363	0.0168	0.0168	0.0168
SN ↓	min_pulse_width to SN	0.0305	0.0305	0.0354	0.0354
SN ↑	recovery_rising to CP	-0.0027	-0.0027	0.0005	0.0005
SN ↑	removal_rising to CP	0.0140	0.0189	0.0189	0.0189
TE ↓	hold_rising to CP	-0.0142	0.0022	0.0022	0.0022
TE ↑	hold_rising to CP	-0.0159	-0.0071	-0.0039	-0.0039
TE ↓	setup_rising to CP	0.0462	0.0343	0.0343	0.0343
TE ↑	setup_rising to CP	0.0787	0.0612	0.0612	0.0612
TI ↓	hold_rising to CP	-0.0514	-0.0256	-0.0264	-0.0264
TI ↑	hold_rising to CP	-0.0202	-0.0037	-0.0037	-0.0037
TI ↓	setup_rising to CP	0.0812	0.0603	0.0603	0.0603
TI ↑	setup_rising to CP	0.0443	0.0319	0.0319	0.0319
		X33_P0			

CP ↓	min_pulse_width to CP	0.0535			
CP ↑	min_pulse_width to CP	0.0189			
D ↓	hold_rising to CP	0.0010			
D ↑	hold_rising to CP	0.0079			
D ↓	setup_rising to CP	0.0343			
D ↑	setup_rising to CP	0.0168			
SN ↓	min_pulse_width to SN	0.0354			
SN ↑	recovery_rising to CP	0.0005			
SN ↑	removal_rising to CP	0.0189			
TE ↓	hold_rising to CP	0.0022			
TE ↑	hold_rising to CP	-0.0039			
TE ↓	setup_rising to CP	0.0343			
TE ↑	setup_rising to CP	0.0612			
TI ↓	hold_rising to CP	-0.0264			
TI ↑	hold_rising to CP	-0.0037			
TI ↓	setup_rising to CP	0.0603			
TI ↑	setup_rising to CP	0.0326			

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.763e-03	1.000e-20
X8_P0	2.216e-03	1.000e-20
X17_P0	3.141e-03	1.000e-20
X25_P0	3.670e-03	1.000e-20
X33_P0	4.201e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	1.390e-02	1.418e-02	1.427e-02	1.431e-02
Clock 100Mhz Data 25Mhz	1.367e-02	1.389e-02	1.548e-02	1.626e-02
Clock 100Mhz Data 50Mhz	1.344e-02	1.360e-02	1.669e-02	1.822e-02
Clock = 0 Data 100Mhz	7.589e-03	7.049e-03	6.867e-03	6.776e-03
Clock = 1 Data 100Mhz	1.818e-03	9.435e-04	6.496e-04	5.047e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	1.433e-02			

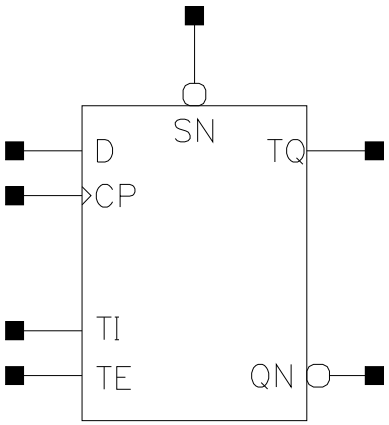
Clock 100Mhz Data 25Mhz	1.711e-02			
Clock 100Mhz Data 50Mhz	1.988e-02			
Clock = 0 Data 100Mhz	6.721e-03			
Clock = 1 Data 100Mhz	4.169e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.216	5.0592
X8_P0	1.200	4.080	4.8960
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0010	0.0010	0.0010
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0016	0.0015	0.0015
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0488	0.0403	2.5833	1.3642
CP to QN ↑	0.0528	0.0318	3.3280	1.7244
CP to TQ ↓	0.0384	0.0214	3.4929	3.1190
CP to TQ ↑	0.0384	0.0307	4.5318	4.4112
SN to QN ↓	0.0333	0.0345	2.5786	1.3619
SN to TQ ↑	0.0238	0.0247	4.4546	4.4101
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0409	0.0449	0.7190	0.3603
CP to QN ↑	0.0354	0.0393	0.8669	0.4429
CP to TQ ↓	0.0261	0.0260	3.2037	3.2074
CP to TQ ↑	0.0348	0.0347	4.4578	4.4702
SN to QN ↓	0.0363	0.0401	0.7178	0.3597
SN to TQ ↑	0.0303	0.0301	4.4323	4.4470

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0552	0.0518	0.0553	0.0553
CP ↑	min_pulse_width to CP	0.0377	0.0189	0.0224	0.0224
D ↓	hold_rising to CP	-0.0208	0.0010	0.0010	0.0010
D ↑	hold_rising to CP	-0.0088	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0506	0.0343	0.0343	0.0343
D ↑	setup_rising to CP	0.0363	0.0168	0.0168	0.0168
SN ↓	min_pulse_width to SN	0.0261	0.0261	0.0261	0.0261
SN ↑	recovery_rising to CP	-0.0028	-0.0027	-0.0027	-0.0027
SN ↑	removal_rising to CP	0.0140	0.0189	0.0189	0.0189
TE ↓	hold_rising to CP	-0.0142	0.0022	0.0022	0.0022
TE ↑	hold_rising to CP	-0.0159	-0.0039	-0.0039	-0.0039
TE ↓	setup_rising to CP	0.0462	0.0343	0.0343	0.0343
TE ↑	setup_rising to CP	0.0787	0.0612	0.0612	0.0612
TI ↓	hold_rising to CP	-0.0514	-0.0256	-0.0256	-0.0256
TI ↑	hold_rising to CP	-0.0195	-0.0037	-0.0037	-0.0037
TI ↓	setup_rising to CP	0.0812	0.0603	0.0603	0.0603
TI ↑	setup_rising to CP	0.0443	0.0319	0.0319	0.0319

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	2.019e-03	1.000e-20
X8_P0	2.469e-03	1.000e-20
X17_P0	3.393e-03	1.000e-20
X33_P0	4.453e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

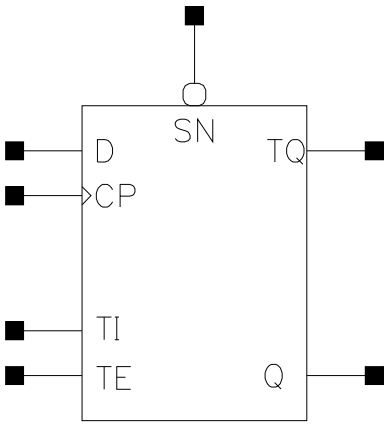
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.392e-02	1.418e-02	1.427e-02	1.431e-02
Clock 100Mhz Data 25Mhz	1.450e-02	1.431e-02	1.588e-02	1.751e-02
Clock 100Mhz Data 50Mhz	1.509e-02	1.444e-02	1.748e-02	2.072e-02
Clock = 0 Data 100Mhz	7.603e-03	7.057e-03	6.874e-03	6.785e-03
Clock = 1 Data 100Mhz	1.823e-03	9.466e-04	6.542e-04	5.073e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.944	4.7328
X17_P0	1.200	4.216	5.0592
X33_P0	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0010	0.0010	0.0010
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0014	0.0014	0.0014
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0459	0.0266	2.9618	1.4257
CP to Q ↑	0.0415	0.0350	3.4930	1.7508
CP to TQ ↓	0.0457	0.0260	4.3362	3.5361
CP to TQ ↑	0.0404	0.0384	4.5694	6.2001
SN to Q ↑	0.0258	0.0288	3.3976	1.7326
SN to TQ ↑	0.0250	0.0313	4.4728	6.1788
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0357	0.0392	0.7125	0.3692
CP to Q ↑	0.0465	0.0496	0.8586	0.4393
CP to TQ ↓	0.0365	0.0404	3.4160	3.4678
CP to TQ ↑	0.0493	0.0540	6.0313	6.0597
SN to Q ↑	0.0412	0.0444	0.8581	0.4390
SN to TQ ↑	0.0440	0.0488	6.0317	6.0619

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0552	0.0535	0.0518	0.0518
CP ↑	min_pulse_width to CP	0.0424	0.0224	0.0190	0.0190
D ↓	hold_rising to CP	-0.0208	0.0010	0.0010	0.0010
D ↑	hold_rising to CP	-0.0088	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0506	0.0343	0.0343	0.0343
D ↑	setup_rising to CP	0.0363	0.0168	0.0168	0.0168
SN ↓	min_pulse_width to SN	0.0261	0.0403	0.0305	0.0305
SN ↑	recovery_rising to CP	-0.0028	0.0005	-0.0027	-0.0027
SN ↑	removal_rising to CP	0.0140	0.0189	0.0189	0.0189
TE ↓	hold_rising to CP	-0.0142	0.0022	0.0022	0.0022
TE ↑	hold_rising to CP	-0.0159	-0.0039	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0462	0.0343	0.0343	0.0343
TE ↑	setup_rising to CP	0.0787	0.0612	0.0612	0.0612
TI ↓	hold_rising to CP	-0.0514	-0.0264	-0.0256	-0.0256
TI ↑	hold_rising to CP	-0.0195	-0.0037	-0.0037	-0.0037
TI ↓	setup_rising to CP	0.0812	0.0603	0.0603	0.0603
TI ↑	setup_rising to CP	0.0443	0.0319	0.0319	0.0319

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.938e-03	1.000e-20
X8_P0	2.092e-03	1.000e-20
X17_P0	2.995e-03	1.000e-20
X33_P0	3.652e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

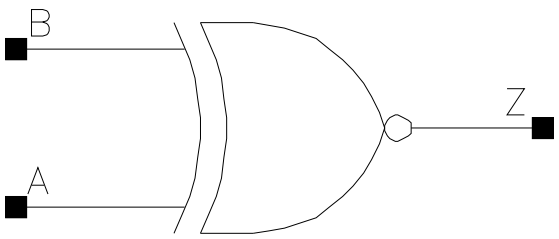
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	1.390e-02	1.416e-02	1.425e-02	1.429e-02
Clock 100Mhz Data 25Mhz	1.492e-02	1.467e-02	1.536e-02	1.704e-02
Clock 100Mhz Data 50Mhz	1.594e-02	1.517e-02	1.647e-02	1.980e-02
Clock = 0 Data 100Mhz	7.604e-03	7.053e-03	6.867e-03	6.777e-03
Clock = 1 Data 100Mhz	1.823e-03	9.440e-04	6.529e-04	5.066e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P0	X8_P0	X17_P0	X25_P0
A	0.0016	0.0007	0.0010	0.0015
B	0.0015	0.0015	0.0019	0.0025
	X33_P0			
A	0.0017			
B	0.0029			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X8_P0**	**X6_P0**	**X8_P0**
A to Z ↓	0.0123	0.0264	2.3803	1.4582
A to Z ↑	0.0124	0.0252	2.5916	1.7878
B to Z ↓	0.0114	0.0186	2.3822	1.4484
B to Z ↑	0.0137	0.0176	2.6002	1.7810
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
A to Z ↓	0.0255	0.0258	0.7151	0.4916
A to Z ↑	0.0237	0.0235	0.8790	0.5863

B to Z ↓	0.0193	0.0186	0.7125	0.4903
B to Z ↑	0.0180	0.0173	0.8758	0.5840
	X33_P0		**X33_P0**	
A to Z ↓	0.0249		0.3688	
A to Z ↑	0.0232		0.4414	
B to Z ↓	0.0181		0.3681	
B to Z ↑	0.0175		0.4405	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P0	1.305e-03	1.000e-20
X8_P0	1.437e-03	1.000e-20
X17_P0	2.553e-03	1.000e-20
X25_P0	3.947e-03	1.000e-20
X33_P0	5.586e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	5.010e-03	8.751e-03	1.390e-02	2.154e-02
B to Z	4.848e-03	7.027e-03	1.209e-02	1.837e-02
	X33_P0			
A to Z	2.715e-02			
B to Z	2.384e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

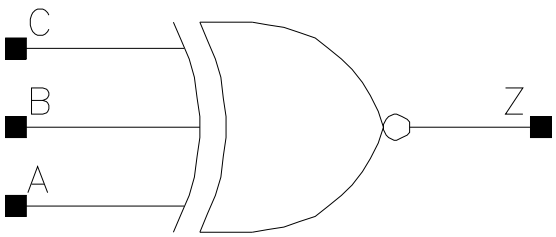
Pin Cycle (vdds)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	2.176	2.6112
X16_P0	1.200	2.720	3.2640
X25_P0	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X16_P0	X25_P0
A	0.0028	0.0024	0.0029	0.0043
B	0.0031	0.0022	0.0029	0.0040
C	0.0019	0.0007	0.0007	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0180	0.0293	2.7526	1.5249
A to Z ↑	0.0169	0.0276	3.6060	1.7678
B to Z ↓	0.0190	0.0300	2.7567	1.5253
B to Z ↑	0.0177	0.0284	3.6116	1.7684
C to Z ↓	0.0191	0.0401	2.7644	1.5249
C to Z ↑	0.0173	0.0383	3.6197	1.7684
	X16_P0	**X25_P0**	**X16_P0**	**X25_P0**
A to Z ↓	0.0299	0.0304	0.7827	0.5007
A to Z ↑	0.0305	0.0305	0.9268	0.5872
B to Z ↓	0.0308	0.0316	0.7829	0.5010

B to Z ↑	0.0312	0.0318	0.9266	0.5871
C to Z ↓	0.0430	0.0464	0.7828	0.5007
C to Z ↑	0.0429	0.0463	0.9264	0.5871

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.250e-03	1.000e-20
X8_P0	1.292e-03	1.000e-20
X16_P0	2.265e-03	1.000e-20
X25_P0	3.277e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	4.597e-03	6.728e-03	1.180e-02	1.826e-02
B to Z	4.683e-03	6.724e-03	1.187e-02	1.843e-02
C to Z	4.636e-03	9.572e-03	1.495e-02	2.284e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

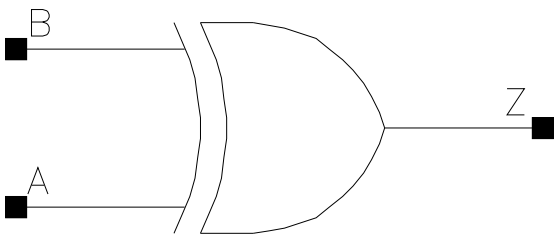
Pin Cycle (vdds)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.224	1.4688
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.224	1.4688
X16_P0	1.200	1.360	1.6320
X25_P0	1.200	2.176	2.6112
X31_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X16_P0
A	0.0008	0.0015	0.0010	0.0012
B	0.0012	0.0014	0.0015	0.0016
	X25_P0	X31_P0		
A	0.0015	0.0019		
B	0.0026	0.0034		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0234	0.0113	2.6224	1.8803
A to Z ↑	0.0234	0.0132	3.3203	3.2169
B to Z ↓	0.0174	0.0126	2.6062	1.8930
B to Z ↑	0.0173	0.0121	3.3126	3.2178
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0214	0.0228	1.4358	0.7397

A to Z ↑	0.0205	0.0222	1.7352	0.8759
B to Z ↓	0.0169	0.0179	1.4314	0.7374
B to Z ↑	0.0161	0.0175	1.7336	0.8749
	X25_P0	**X31_P0**	**X25_P0**	**X31_P0**
A to Z ↓	0.0242	0.0230	0.4887	0.3904
A to Z ↑	0.0230	0.0221	0.5843	0.4705
B to Z ↓	0.0184	0.0171	0.4882	0.3901
B to Z ↑	0.0174	0.0169	0.5837	0.4705

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.157e-03	1.000e-20
X6_P0	1.165e-03	1.000e-20
X8_P0	1.871e-03	1.000e-20
X16_P0	2.993e-03	1.000e-20
X25_P0	3.926e-03	1.000e-20
X31_P0	5.654e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	6.380e-03	4.894e-03	8.350e-03	1.307e-02
B to Z	5.570e-03	4.703e-03	7.709e-03	1.205e-02
	X25_P0	X31_P0		
A to Z	2.079e-02	2.600e-02		
B to Z	1.813e-02	2.297e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

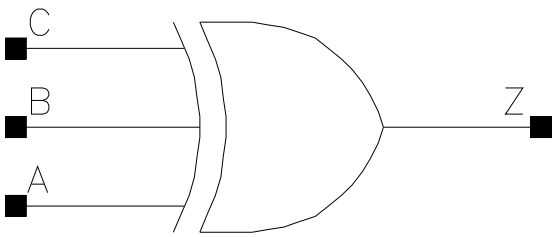
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P0	X31_P0		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X24_P0	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X24_P0
A	0.0024	0.0024	0.0029	0.0052
B	0.0025	0.0022	0.0027	0.0043
C	0.0008	0.0016	0.0022	0.0034

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0183	0.0293	2.9037	1.5245
A to Z ↑	0.0174	0.0276	3.9484	1.7663
B to Z ↓	0.0191	0.0300	2.9087	1.5250
B to Z ↑	0.0181	0.0284	3.9530	1.7668
C to Z ↓	0.0329	0.0297	2.8835	1.5263
C to Z ↑	0.0320	0.0281	3.9381	1.7668
	X17_P0	**X24_P0**	**X17_P0**	**X24_P0**
A to Z ↓	0.0275	0.0323	0.7317	0.5242
A to Z ↑	0.0280	0.0250	0.8642	0.5905
B to Z ↓	0.0282	0.0330	0.7322	0.5244

B to Z ↑	0.0287	0.0256	0.8645	0.5902
C to Z ↓	0.0282	0.0327	0.7326	0.5247
C to Z ↑	0.0288	0.0258	0.8642	0.5905

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	1.365e-03	1.000e-20
X8_P0	1.099e-03	1.000e-20
X17_P0	2.193e-03	1.000e-20
X24_P0	3.276e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	4.426e-03	6.721e-03	1.149e-02	1.886e-02
B to Z	4.479e-03	6.717e-03	1.155e-02	1.893e-02
C to Z	8.079e-03	6.663e-03	1.154e-02	1.892e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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