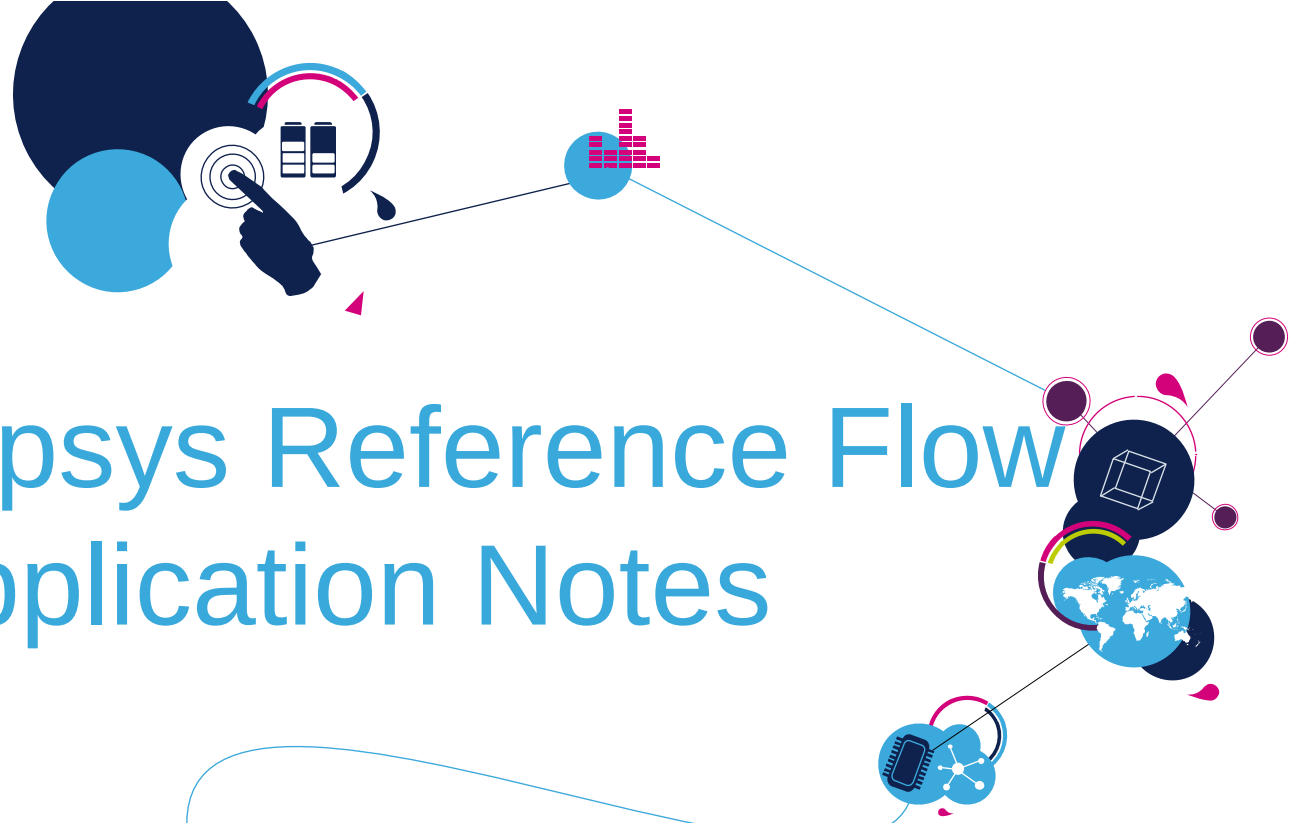


28nm FD-SOI Synopsys Reference Flow Place-and-Route Application Notes

Version 3.1

Digital Design Flows & Methodologies

January 2019

life.augmented

ST Confidential

Revisions

Version	Date	Comment
3.1	January 2019	Add place legalize option to avoid placement DRC
3.0	October 2018	Add Voltage Spacing Rules
2.0	March 2018	Add IP/memory implementation guidelines
1.0	June 2017	Initial Version

Prerequisites : Documentation

- Please refer to the **Foundation_Synopsys_TechnoKit_cmos028FDSOI** User Manual for the description of the technology files

- Please refer to the **28nm FD-SOI Synopsys Reference Flow Sign-Off Application Notes** for
  - Description of 28nm-FDSOI Sign-Off RC extraction scenarios
  - Description of 28nm-FDSOI Sign-Off STA scenarios
  - Description of clock tree implementation rules
  - On-Chip-Variation derating factors

Prerequisites : Technology

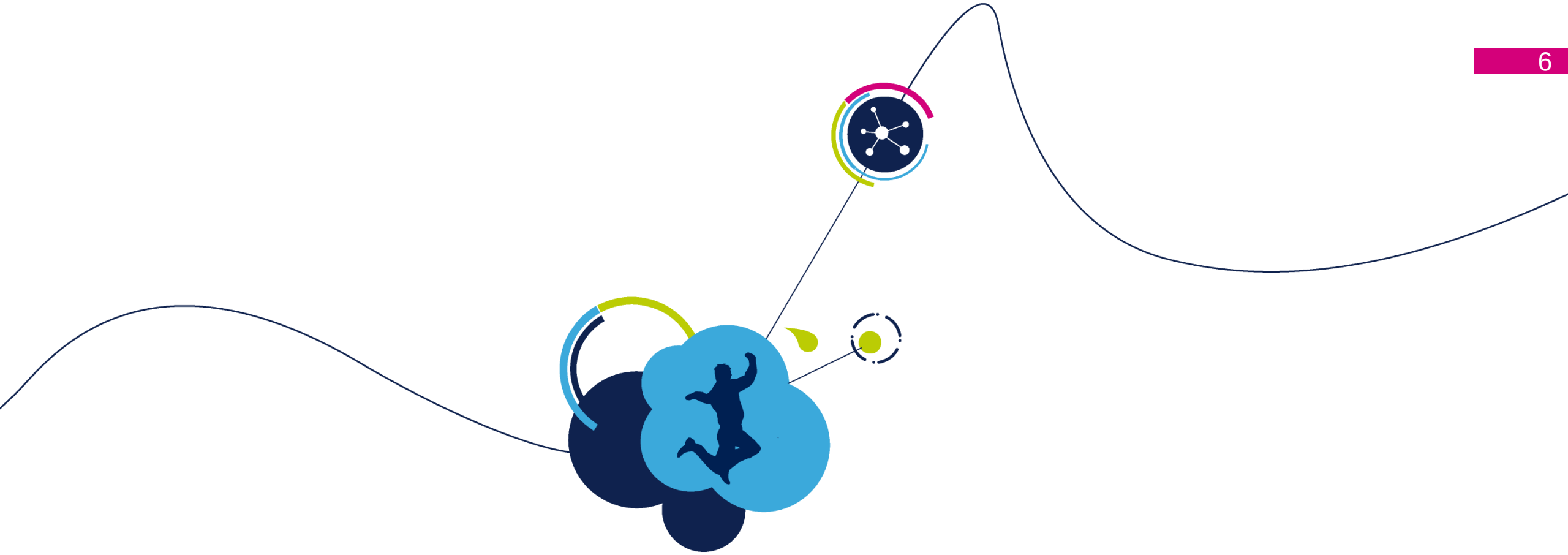
- In P&R, **only dominant STA scenarios** for setup, hold and worst leakage corner are sufficient (identified from a first Signoff loop)
- Clock tree must follow “**Clock Tree Implementation Rules**” from Sign-Off Application Notes
- Place-and-Route **OCV** values must be taken from Signoff Application Notes
- **RVT and LVT standard-cells cannot be mixed** in the same standard-cell placement area, due to LVT being flip-well architecture

EDA Tools Versions

- The 28nm FD-SOI Synopsys Reference Flow has been qualified with the following EDA tools

Place-and-Route Step	EDA Tool & Version
Place-and-Route	Synopsys ICCII 2017.09-SP6-0
Incremental DRC Fixing	Synopsys IC_Validator 2017.12

- EDA tools versions used for flow execution are left up to user discretion



ICCII: Static Timing Analysis Settings

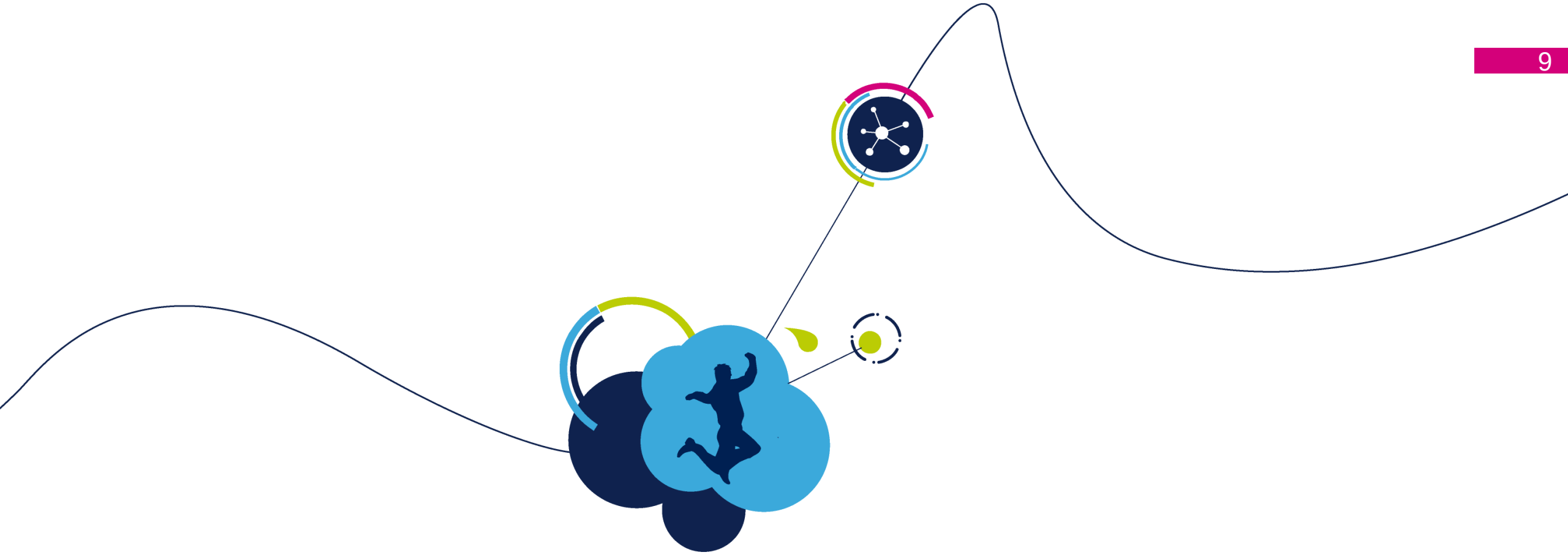
Required Settings for ICCII

- The following variables have to be set in ICCII for static timing analysis in 28nm-FDSOI:
  - set_app_options -name time.remove_clock_reconvergence_pessimism -value true
  - set_app_options -name time.clock_reconvergence_pessimism -value same_transition
  - set_app_options -name time.si_enable_analysis -value true
- CCS libraries mandatory

Setting STA 0y/2ey in ICCII

- The following lines describe how to mix fresh (0y) and aged (2ey) libraries using process_labels in ICCII:

```
During libraries generation:
    read_db -process_label ss28 / ff28 / ss28_2ey / ff28_2ey <timingFile>
During P&R:
    create_mode
    create_corner
    create_scenario -mode -corner -name
    set_target_library_subset <list libraries> -top/-objects
    Foreach corner:
        set_process_number
        set_temperature
        set_parasitics_parameters \
            -library <generated tech lib containing .tf, TLU+, sites> -early_spec \
            -early_temperature -late_spec -late_temperature -corners
        set_process_label -early ss28 / ff28 -late ss28_2ey / ff28_2ey  \
            -library ${libName}.ndm:$libName
        set_voltage
    Foreach scenario :
        source <constraint files>
        set_timing_derate …
```



ICCII Place-and-Route Flow

LVT vdds logic connection

- The following statements must be included in the UPF file

```
set_design_attributes -elements {.} -attribute enable_bias true
create_supply_set .... -function {pwell gnd} -function {nwell gnd}
```

Placement Settings -1-

- The following lines avoid DRC errors due to wrong abutment or spacing between cells, by using “LEF58_EDGETYPE” properties and applying spacing rules:

```
# Extracting spacing labels from LEF58_EDGETYPE
remove_placement_spacing_rules -all
define_user_attribute -persistent -type string -class lib_cell LEF58_EDGETYPE
set fileId [open "set_placement_spacing_label.tcl" w]
foreach_in_collection libCellFramePtr [get_lib_cells -quiet -filter "defined(LEF58_EDGETYPE)" */*/frame] {
      set libCellName [get_attribute $libCellFramePtr lib_name]/[get_attribute $libCellFramePtr name]
      set LEF58_EDGETYPE [get_attribute $libCellFramePtr LEF58_EDGETYPE]
      puts $fileId "\n# Lib cell: $libCellName \n#   LEF58_EDGETYPE = '$LEF58_EDGETYPE'"
 foreach item [split $LEF58_EDGETYPE ";"] {
          if { [regexp {EDGETYPE\s+(\S+)\s+(\S+)} $item m side label] } then {
```

Placement Settings -2-


```
switch -exact -- $side {
                  "LEFT" -
                  "RIGHT" {
                      puts $fileId "set_placement_spacing_label -name $label -side [string tolower $side] -
lib_cell \[get_lib_cells $libCellName\]"
                  }
                  default {
                      puts "Unknown LEF58_EDGETYPE element '$item' on lib cell '$libCellName'."
}}}}}
close $fileId
source "set_placement_spacing_label.tcl"
source ${Foundation_Synopsys_TechnoKitTRoot}/ICCOMPILERII/spacing_label_rule_setup.tcl
set_app_options -name place.legalize.enable_allowable_orient              -value true
```

Routing Settings -1-

- The following line defines routing pitches:

```
source ${Foundation_Synopsys_TechnoKitTRoot}/ICCOMPILERII/layers_setup_COT.tcl
```

- The following lines ensure multi-cut vias usage:

```
source ${Foundation_Synopsys_TechnoKitTRoot}/ICCOMPILERII/define_optimized_vias.tcl
```

To be called/tuned at different steps (runtime/QOR trade-off):

```
set_app_options -name route.common.concurrent_redundant_via_mode -value reserve_space
set_app_options -name route.common.eco_route_concurrent_redundant_via_mode -value off / reserve_space
set_app_options -name route.common.post_detail_route_redundant_via_insertion -value off / low / medium
add_redundant_vias -effort medium
```

Routing Settings -2-

- The following lines improve ICCII standard-cell pins access for non-default rules:

  To be called/tuned at different steps (routing convergence/ routing QOR trade-off):

```
set_app_options  -name route.detail.use_wide_wire_effort_level  -value off / low
set_app_options  -name route.detail.use_wide_wire_to_input_pin  -value true / false
set_app_options  -name route.detail.use_wide_wire_to_output_pin -value true / false
```

- The following line improve convergence:

```
set_app_options  -name route.common.route_soft_rule_effort_level -value off / min / medium
```

- The following line allows diodes antenna fixing:

```
source ${Foundation_Synopsys_TechnoKitTRoot}/ICCOMPILERII/antenna_rules.tcl

set_app_options -name route.detail.insert_diodes_during_routing   -value true
```

Routing Settings -3-

- IC Compiler II tech file does not natively support negative voltages for FBB. The following lines will make the router comply with voltage spacings rules, when negative voltage is lower than -0.6V :

```
source ${Foundation_Synopsys_TechnoKitTRoot}/ICCOMPILERII/define_non_default_rules.tcl

set_routing_rule -rule HighVoltageFBBLowerThan600mVvsGO1 [get_nets -all vdds]
```

Timing Convergence -1-

- The following lines improve convergence by limiting the length of the wires, and manage delay cells:
  - `set_app_options -name opt.common.max_net_length -value 900`
  - `set_app_options -name cts.common.max_net_length -value 300`
  - `setDontUse <delay cells> true ; setOptMode -holdFixingCells <delay cells, buffers cells, inverter cells>`

Timing Convergence -2-

- It is recommended to create a tcl script defining a double space shield rule and apply it to clock-tree nets using command : *set_clock_routing_rules*… :

```
create_routing_rule \
    -default_reference_rule \
    -taper_over_pin_layers 1 \
    -cuts {{V1 {Vv 1}} {V1 {Vh 1}} {V2 {Vh 1}} {V2 {Vv 1}} {V3 {Vv 1}} {V3 {Vh 1}} {V4 {Vh 1}} {V4 {Vv 1}} {V5 {Vv 1}} {V5 {Vh 1}}} \
ctsDoubleCut
```

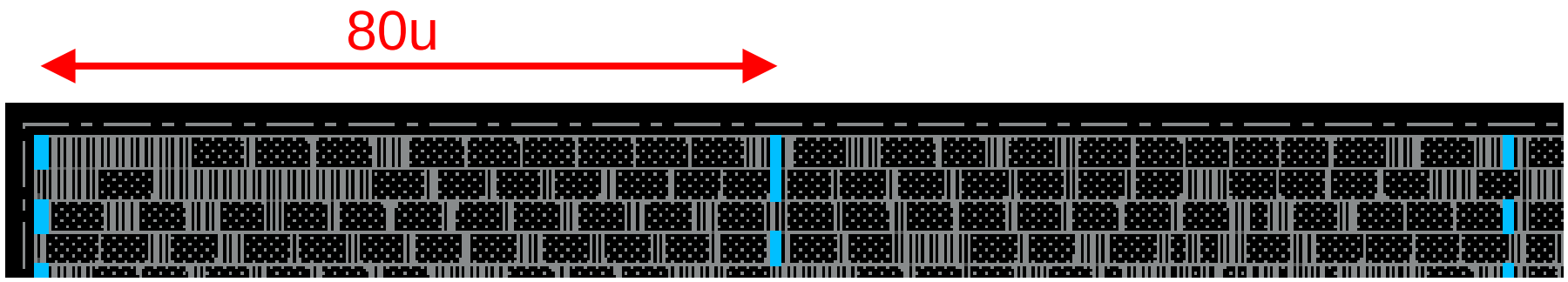
Timing Convergence -3-


```
create_routing_rule \
    -reference_rule_name ctsDoubleCut \
    -spacings {M2 {0.100 0.150} M3 {0.100 0.150} M4 {0.100 0.150} M5 {0.100 0.150} M6 {0.100 0.150}} \
    -spacing_weight_levels {M2 {medium low } M3 {high medium} M4 {high medium} M5 {high high } M6 {high high }} \
    -spacing_length_thresholds {M2 {2.000  2.000} M3 {2.000 2.000 } M4 {2.000 2.000 } M5 {2.000 2.000} M6 {2.000
2.000}} \
ctsDoubleCutDoubleSpacing
create_routing_rule \
    -reference_rule_name ctsDoubleCutDoubleSpacing \
    -shield \
    -shield_spacings {M1 0.000 M2 0.000 M3 0.000 M4 0.000 M5 0.150 M6 0.150} \
    -shield_widths {M1 0.000 M2 0.000 M3 0.000 M4 0.000 M5 0.050 M6 0.050} \
    -snap_to_track \
ctsDoubleCutDoubleSpacingShield
```

Welltaps Insertion Flow

- The following lines ensure DRC-clean welltaps insertion: every standard-cell is at maximum 40u from a welltap:

```
create_cell_array -lib_cell <welltap cell> -voltage_area <voltage area>  \
        -x_offset 10 -x_pitch 80 -y_pitch 1.2 -secondary_x_offset 0 \
        -secondary_x_pitch 40 -drc_tap_distance 40 \
        -fill_tap_gap_with_pattern stagger  -snap_to_site_row true \
        -preserve_boundary_row_lib_cells <welltap cell> -checkerboard odd \
        -prefix WELLTAP_
```



Top/Bottom/Left/Right Endcaps Insertion Flow

- The following lines insert :
  - Top and bottom endcap standard-cells on the first bottom and the last top standard-cell row, to be avoid GR111_or DRC violations:

```
create_boundary_cells -top_boundary_cells <list of lib/cell/frame> \
      -bottom_boundary_cells <list of lib/cell/frame> -at_va_boundary \
      -prefix TOP_BOTTOM_
```

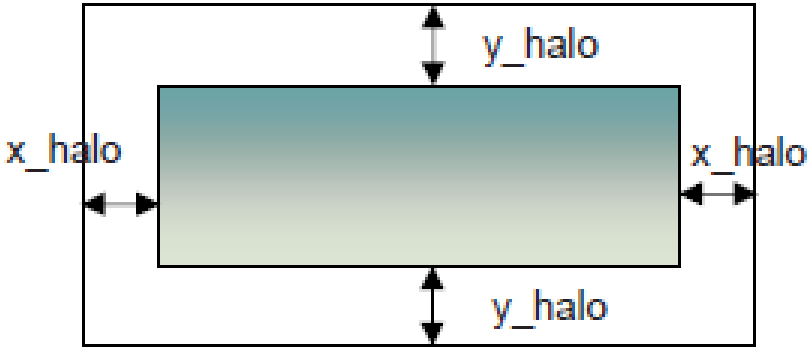
  - Left and right endcap standard-cells, to ensure P&R context is the same as the one used during library timing characterization. Minimum size must be FILLERPFOP2:

```
create_boundary_cells \
      -left_boundary_cell C28SOI_SC_12_PR_LL/C12T28SOI_LL_FILLERPFOP2/frame \
      -right_boundary_cell C28SOI_SC_12_PR_LL/C12T28SOI_LL_FILLERPFOP2/frame \
      -at_va_boundary -prefix LEFT_RIGHT_
```

CTS Halos

- The following lines define CTS halos, to avoid electromigration/IR-Drop issues, by keeping a certain minimum distance between clock inverters and/or gating cells…
- Recommended value: x_halo=4u for drives<=X55 or 8u for drives>X55 (to be refined depending on power grid pattern); y_halo=0.1u
- Example:

```
set_clock_cell_spacing
      -lib_cells <libname/cellname> \
      -x_spacing 4
      -y_spacing 0.1
```



Memories, IPs -1-

- Memory pins are drawn with vertical M4 shapes (non-preferential direction)
- To connect memory cuts to the PG grid, vias are stacked at each intersection between memory M4 pins and PG grid stripes.
- At floorplan-level, a 1 um hard halo is generally defined around the IPs
- Around memories/IPs, soft placement blockages may be defined to get easier pin access

Memories, IPs -2-

- Full metal obstructions are generally defined in the LEF file of the digital IPs
  - This avoids top-level routing over the IP
  - During top-level routing, the IP is seen as large metal shape, which forces the router to respect fat layer spacing rules (typically around 0.5um, which corresponds to 5 tracks)
- Routing blockages may be defined inside the digital IP at the boundary in order to avoid long nets in the preferentials directions. This will limit coupling effects between top-level routing and block-level routing.

Keep out distance between RVT and LVT

- LVT being a flip-well architecture, it cannot be mixed with RVT cells on a same standard cells area

- Some dedicated islands have to be created in case RVT and LVT are used for digital sections on the same chip, since both cannot be merged inside a standard cells row

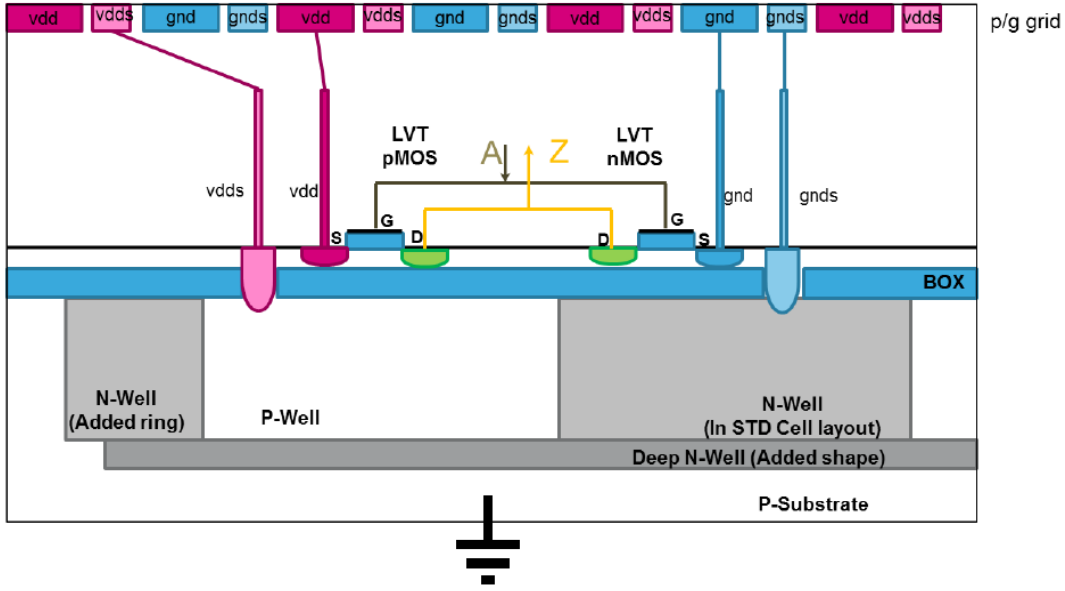
- **DRM** rules have to be honored for such configurations

Top level placement of Deep NWell/ Block Construction level guidelines -1-

- To apply a body bias voltage to the P-Well, it is required to isolate the P-Well areas from the P-Substrate.
- This typically occurs in case of a single VT (LVT or RVT) design where we want to apply Back Bias (BB) voltages to some design portions
- The isolation is implemented using a

deep n-type implant (Deep N-Well) and

an N-Well ring.



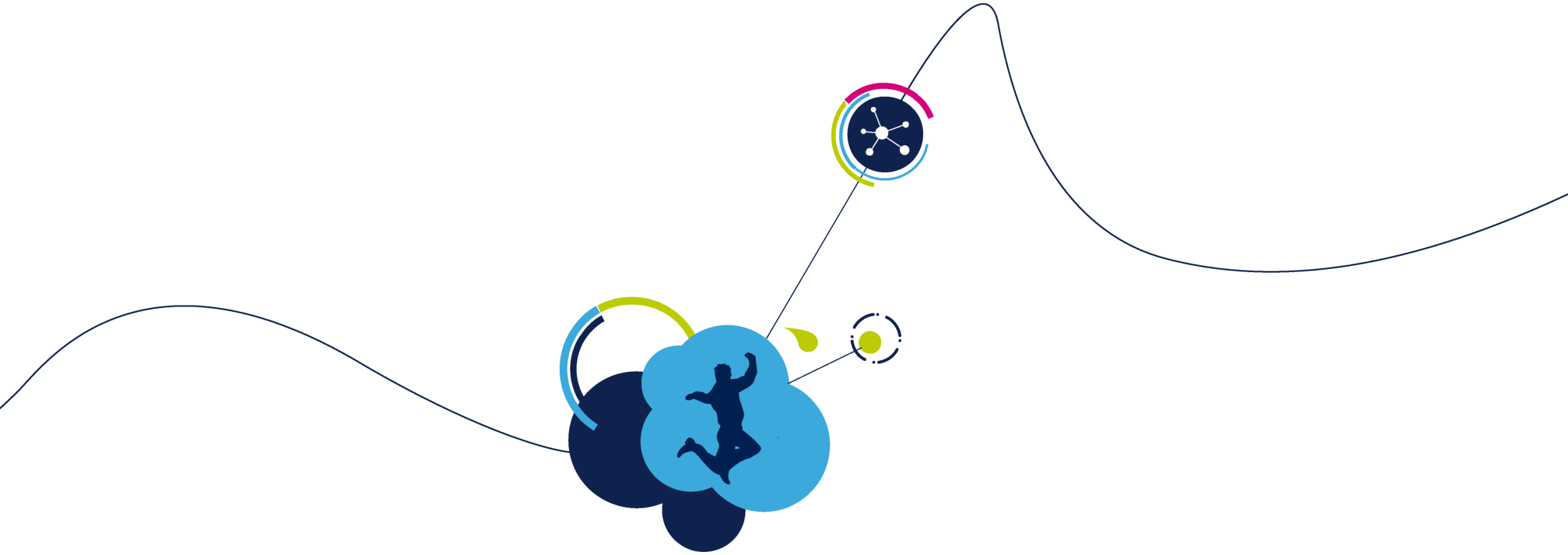
LVT Body biased configuration with deep N-Well

Top level placement of Deep NWell/ Block Construction level guidelines -2-

- It is required to implement a power grid that distributes supply (vdd), ground (gnd) and substrates polarization (gnds, vdds)

- **To isolate the P-Well from P-Substrate it is required to:**
  - Add an N-Well ring around the biased region to side-isolate P-Well
  - Add under the biased region a deep N-Well layer (T3) with boundary over N-Well ring

- **Please refer to DRM for**
  - Deep-NWell/T3 – Deep-NWell/T3 spacing rules
  - Deep-NWell/T3 – NW spacing rules
  - T3 – NW overlap rule



IC Validator DRC Fixing Flow

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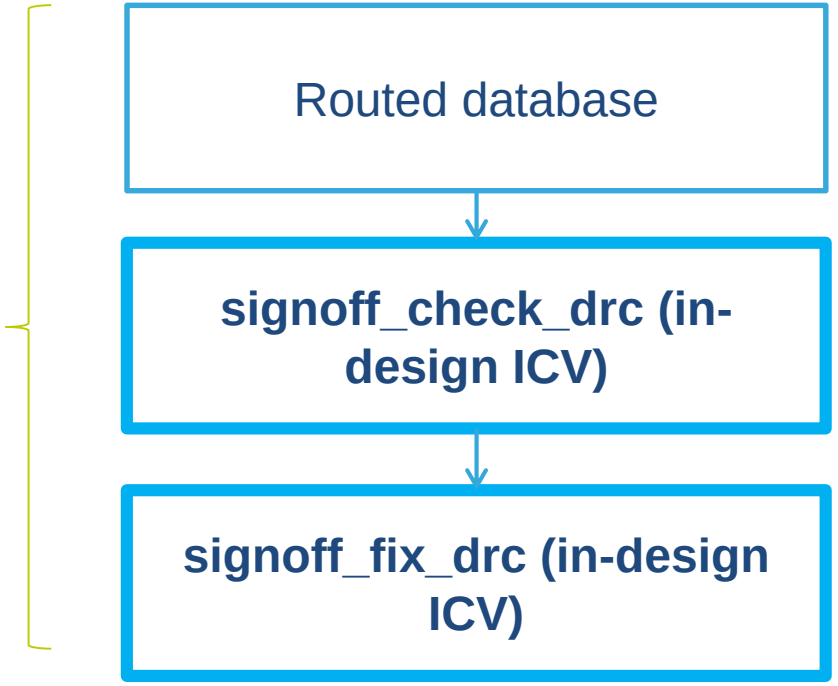
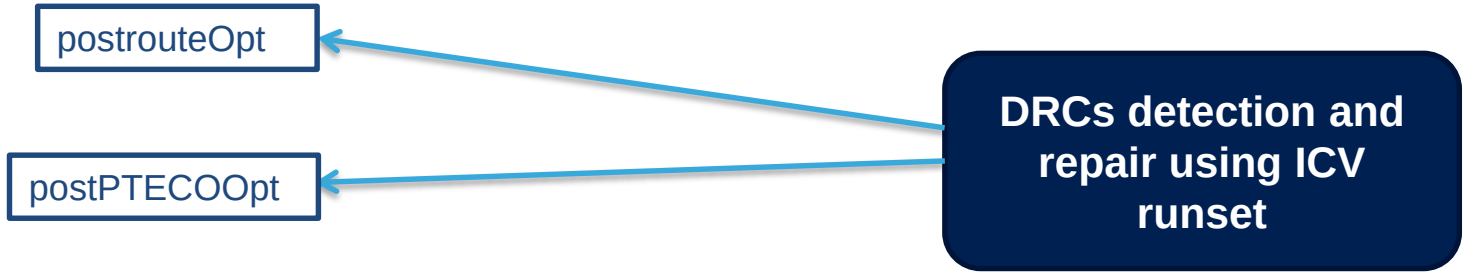
ICV DRC Fixing

IC Validator DRC fixing flow allows to fix last DRC violations which are not described in ICCII techfile, but only in ICV runset.





Mini deck ICV for DRC repair -1-

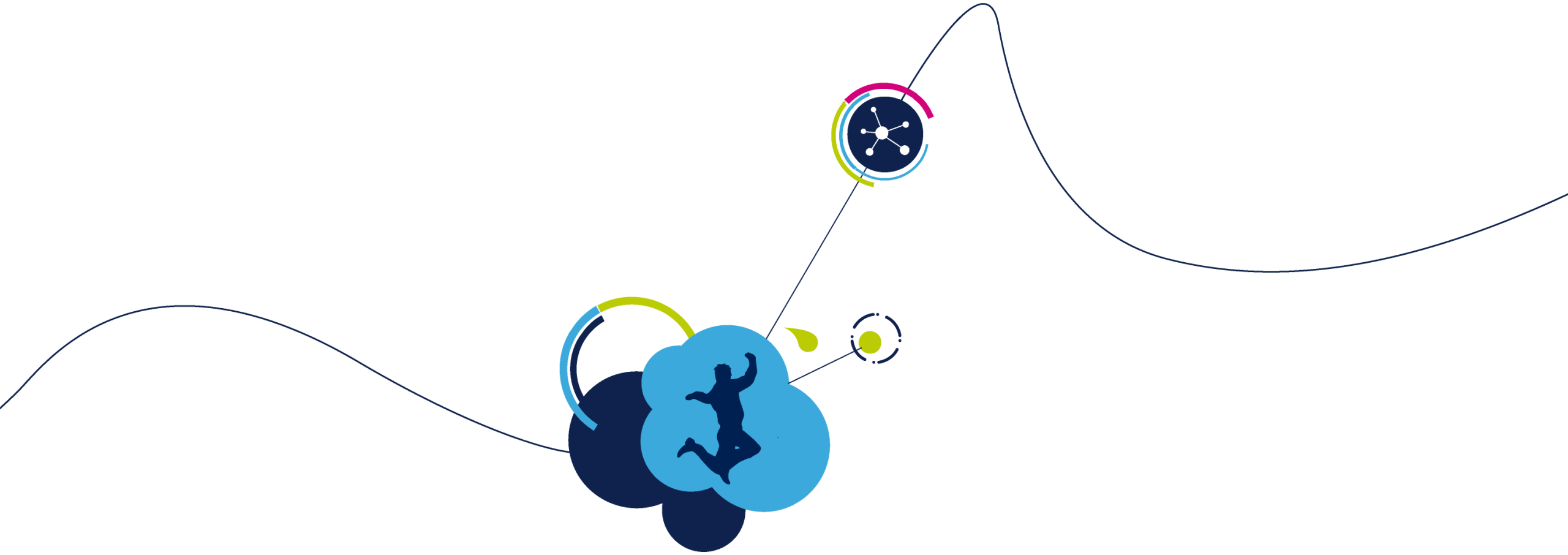

```
# Work directory & variables management

file delete -force ./ICV/auto_fix.postrouteOpt_${route_pass_number}-run_dir

file mkdir ./ICV/auto_fix-postrouteOpt_${route_pass_number}-run_dir/checks

file mkdir ./ICV/auto_fix-postrouteOpt_${route_pass_number}-run_dir/autofix

set_app_options -name route.global.timing_driven                -value false

set_app_options -name route.global.crosstalk_driven             -value false

set_app_options -name route.track.timing_driven                 -value false

set_app_options -name route.track.crosstalk_driven              -value false

set_app_options -name route.detail.timing_driven                -value false

set_app_options -name route.detail.antenna                      -value false

set_app_options -name route.common.post_detail_route_redundant_via_insertion -value off

set_app_options -name route.common.net_max_layer_mode           -value soft
```

Mini deck ICV for DRC repair -2-


```
set_app_options -name route.common.single_connection_to_pins     -value off

# Perform IC Validator DRC checks

set_app_options -name signoff.check_drc.fill_view_data           -value discard

set_app_options -name signoff.check_drc.ignore_blockages_in_cells -value true

set_app_options -name signoff.check_drc.max_errors_per_rule      -value 1000

set_app_options -name signoff.check_drc.runset                   -value
${Foundation_Synopsys_TechnoKitTRoot}/ICV/drc_autofix_runset.rs

set_app_options -name signoff.check_drc.run_dir                  -value ./ICV/auto_fix-
postrouteOpt_${route_pass_number}-run_dir/checks

set_app_options -name signoff.physical.layer_map_file            -value
${Foundation_Synopsys_TechnoKitTRoot}/ICCOMPILERII/map_out


signoff_check_drc -error_data [get_attribute [current_block] name]@ICV_DRC_AUTOFIX.err
```

Mini deck ICV for DRC repair -3-


```
 # Perform IC Validator DRC autofix
set_app_options -name signoff.fix_drc.config_file              -value auto
set_app_options -name signoff.fix_drc.init_drc_error_db        -value ./ICV/auto_fix-
postrouteOpt_${route_pass_number}-run_dir/checks
set_app_options -name signoff.fix_drc.max_errors_per_rule      -value 1000
set_app_options -name signoff.fix_drc.run_dir                  -value ./ICV/auto_fix-
postrouteOpt_${route_pass_number}-run_dir/autofix
set_app_options -name signoff.fix_drc.target_clock_nets        -value true


signoff_fix_drc
(then restore orignal settings…)
```



IC Validator Litho Fixing Flow

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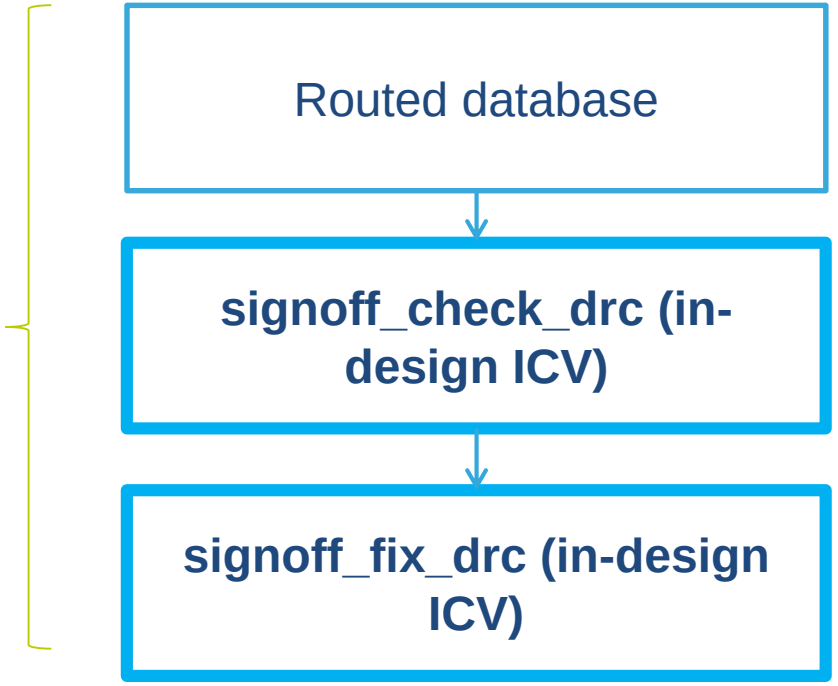
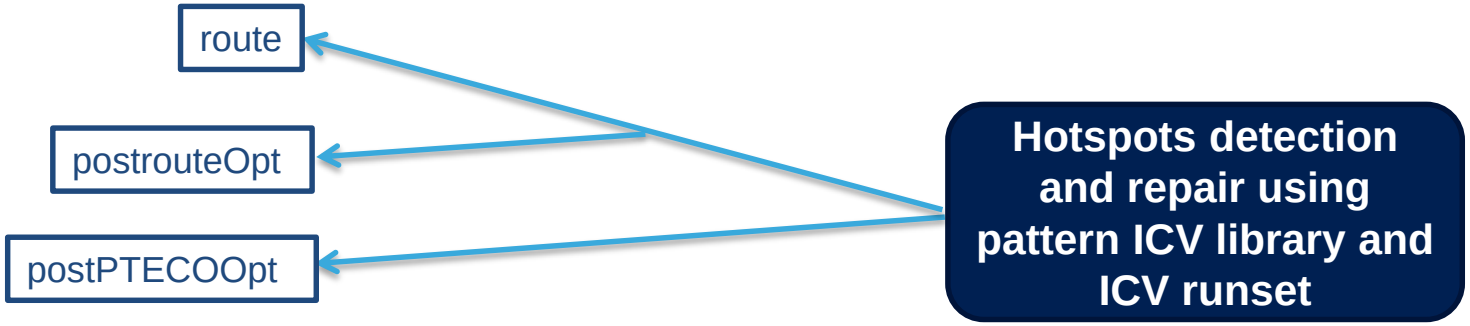
ICV Lithography Hotspots Fixing

Can be done at each route step for better results





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Mini deck ICV for litho repair -1-


```
#configuration
 set env(ICC2_INDESIGN_INTERNAL_ADR__LARGE_AMA_THRESHOLD_PITCH_MULTIPLIER) 20
 set env(PM_LIB_PATH) ${Foundation_Synopsys_TechnoKitTRoot}/ICV/litho.libraries
 set env(PM_LIB_NAME1) Library1
 set env(PM_LIB_NAME2) Library2


# Work directory & variables management
file delete -force ./ICV/litho_pattern_matching.postrouteOpt_${route_pass_number}-run_dir
file mkdir ./ICV/litho_pattern_matching-postrouteOpt_${route_pass_number}-run_dir/checks
file mkdir ./ICV/litho_pattern_matching-postrouteOpt_${route_pass_number} -run_dir/autofix
set_app_options -name route.global.timing_driven        -value false
```

Mini deck ICV for litho repair -2-


```
set_app_options -name route.global.crosstalk_driven     -value false

set_app_options -name route.track.timing_driven         -value false

set_app_options -name route.track.crosstalk_driven      -value false

set_app_options -name route.detail.timing_driven        -value false

set_app_options -name route.detail.antenna              -value false

set_app_options -name route.common.post_detail_route_redundant_via_insertion        -value off

set_app_options -name route.common.net_max_layer_mode   -value soft

set_app_options -name route.common.single_connection_to_pins -value off



# Perform IC Validator lithography checks

set_app_options -name signoff.check_drc.fill_view_data            -value discard
```

Mini deck ICV for litho repair -3-


```
set_app_options -name signoff.check_drc.ignore_blockages_in_cells -value true

set_app_options -name signoff.check_drc.ignore_child_cell_errors -value true

set_app_options -name signoff.check_drc.max_errors_per_rule      -value 100000

set_app_options -name signoff.check_drc.read_design_views   -value *

set_app_options -name signoff.check_drc.runset                   -value
${Foundation_Synopsys_TechnoKitTRoot}/ICV/litho.runset

set_app_options -name signoff.check_drc.run_dir                  -value
./ICV/litho_pattern_matchingpostrouteOpt_${route_pass_number}-run_dir/checks

set_app_options -name signoff.check_drc.user_defined_options     -value {-D d_SNPSINDESIGN=dx_YES -D
d_BEOL_STACK=dx_6U1X_2U2X_2T8X_LB}

                                    # dx_6U1X_2T8X_LB for 8ML

set_app_options -name signoff.physical.layer_map_file            -value
${Foundation_Synopsys_TechnoKitTRoot}/ICCOMPILERII/map_out


signoff_check_drc -error_data [get_attribute [current_block] name]@ICV_LITHO.err
```

Mini deck ICV for litho repair -4-


```
# Perform IC Validator lithography autofix

set_app_options -name signoff.fix_drc.config_file                -value
${Foundation_Synopsys_TechnoKitTRoot}/ICV/litho.cfg

set_app_options -name signoff.fix_drc.init_drc_error_db          -value ./ICV/litho_pattern_matching-
postrouteOpt_${route_pass_number}-run_dir/checks

set_app_options -name signoff.fix_drc.max_errors_per_rule        -value 100000

set_app_options -name signoff.fix_drc.run_dir                    -value ./ICV/litho_pattern_matching-
postrouteOpt_${route_pass_number}-run_dir/autofix

set_app_options -name signoff.fix_drc.target_clock_nets          -value true

set_app_options -name signoff.fix_drc.user_defined_options       -value {-D
d_BEOL_STACK=dx_6U1X_2U2X_2T8X_LB}

             # dx_6U1X_2T8X_LB for 8ML

signoff_fix_drc -start_repair_loop 1 -max_number_repair_loop 2

(then restore orignal settings…)
```