PDK_STM_cmos28FDSOI_RF_mmW_6U1x_2T8x_LB
Known Problems and Solutions

- This document is listing the known problems of the DK 1.2 and proposes solutions whenever they are available.
  The Design Kit new features are described in the release notes document.

- Compliancy with ERC_MG_KIT@3.0-01
  - The following error is displayed in Virtuoso when STECCK is loaded after the Design-Kit :
    - *ERROR: Invalid calibre version*
    - \o *- current version: v2018.2_24.18*
    - \o *- required version: 2017.3_29.23*
    - \o *-> calibre version for ERC verification flow is not OK. Expected version: 2017.3_29.23*
  - You can safely ignore this error message.

- Mosfet Matching:
  - The extraction of parameters (xpos/ypos) flattens the layout hierarchy during LVS. If matching simulations are not required, the switch "*Do not extract XPOS/YPOS*" is available to disable the extraction of such parameters if needed.

- Monte-Carlo simulations:
  - With ELDO ams>15.4 and DATAFLOW=1, a syntax problem in mc extract exists.
    - In order to ensure good Monte Carlo analysis results:
      - Don't use mc extract (as mcavg, mcstd etc.) in the same line, break down in several lines.
        Ex with DATAFLOW=1 (in MC Analysis Definition form / MC Advanced Output):
        - Syntax NOT TO BE USED
          - *.EXTRACT mc label=Adids abs(sqrt(m*w*l)*(1e6)*100*__mcstd__(extract_intern_dids)/__mcavg__(extract_intern_ids))*
          - *.EXTRACT mc label=sigma_dioi abs(100*__mcstd__(extract_intern_dids)/__mcavg__(extract_intern_ids)*
        - Syntax TO USE
          - *.EXTRACT mc LABEL=STD_extract_intern_dids __mcstd__(extract_intern_dids)*
          - *.EXTRACT mc LABEL=AVG_extract_intern_ids __mcavg__(extract_intern_ids)*
          - *.EXTRACT LABEL=Adids2 abs(sqrt(m*w*l)*(1e6)*100*EXTRACT(STD_extract_intern_dids)/ EXTRACT(AVG_extract_intern_ids))*

- *.EXTRACT label=sigma_dioi2 abs(100*EXTRACT(STD_extract_intern_dids)/ EXTRACT(AVG_extract_intern_ids))*

- or set DATAFLOW=0 in MC Analysis Definition form / MC Advanced Output

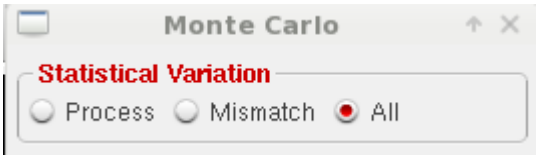
- Nota bene: in ams 16.1 release, this compact syntax won't be allowed and it will lead to warning message: Warning 1053: COMMAND .EXTRACT: ADIDS is ignored. An .EXTRACT MC cannot contain multiple functions.

- Selection of statistical variations (**global process** and/or **local mismatch**)
  - The selection of the statistical variations involved during a monte-carlo analysis **MUST** be done using the following features of the models:
    - Use the **stat** corner for involving Global **Process** variations
    - Set the **<family>_dev** (ex: rvt_dev, eg_dev) parameters to **1** for involving Local **Mismatch** variations

      The ArtistKit *Setup Corners* GUI helps you doing these selections

      - Set the GLOBAL VARIATIONS to **stat** for all or some device families
      - Set the LOCAL VARIATIONS to **monte-carlo** for all or some device families

  - The selection of the statistical variations **MUST NOT** be done using the monte-carlo analysis definitions of the simulators. So please do not use the following simulator statements:
    - Spectre
      - In stand-alone, **always** set the *variations=**all*** flag on the *montecarlo* analysis statement. Per default only process variations are involved.
      - From ADE-XL, in *Monte-Carlo* form, always keep the *Statistical Variations* field to **All** value



    - Hspice
      - In stand-alone, do not use the .VARIATION Block Control Options and the Ignore_Global_Variation, Ignore_Local_Variations associated otpions.
      - From *ADE-XL, in Monte-Carlo* form, always keep the *Statistical Variations* field to **All** value (same as Spectre)

    - Eldo
      - In stand-alone netlist, **never** set the **VARY** argument on the .MC command. Per default all statistical variations are involved.
      - From ADE-L, in *Choosing Analyses* **mc** form, always keep the *Apply Variations Using* field to **Both Device/Lot** value.

- From ADE-XL, *in Monte Carlo* form, always keep the *Statistical Variations* field to **All** value (same as spectre simulator).

  - Summary table

Simulator statistical variation selection	Corner Model settings	Matching model settings	Global contributions (process)	Local contributions (mismatch)
All	TT, SS, SFA, …, USER (any corner except statmotherfab)	<family>_dev = 0 or mismatch = 0	Worst-Case Corner	None
All	TT, SS, SFA, …, USER (any corner except statmotherfab)	<family>_dev = 1 and mismatch = 1	None	All
All	STATMOTHERFAB	<family>_dev = 0 or mismatch = 0	All	None
All	STATMOTHERFAB	<family>_dev = 1 and mismatch = 1	All	All

- RF-MOS:
  - Number of gate fingers (n) parameter cannot be parameterized.
  - DC Annotation on segmented simulation level takes into account a single transistor instance.
  - MOS RF devices are not supported within Cadence LDE flow yet.
  - The “Add Labels (partial layout XL)” option in PLS GUI is only working with analog MOS, not with RF MOS

- Other simulation items:
  - Poly resistors: Inaccurate non-linearity modeling when sbar (series stripes) >1.
    - Workaround:
      - Use series resistors in schematic
      - Run Post-Layout Simulation for a correct modeling
  - LF noise corners in post-layout :
    - Models: SG and EG MOS transistors
    - The corners defined for the LF noise do not take into account the variation reduction due to the multiplicity of the devices in post-layout simulation because LVS cannot extract the mult instance parameter
  - Modeling inaccuracy of EGRVT PFET capacitances :

        - Models: egpfet_acc, egvpfet_acc
        - EG/EGV RVT PFET models do not simulate the Cg-ds capacitances around the threshold voltage inside the modeling accuracy tolerance of 5%.
    - Saturation current of RPO mosfets :
        - The modeling of the RPO mosfets for the I/O applications are performed in the design-kit through the association of the mosfets accurate models with the corresponding unsalicided resistance (sblkndres/sblkpdres) models
        - The correlation between the simulation and the measurement shows an under-estimation of the saturation current by 7%.
    - Wpe default values :
        - Models: *pfet_acc, eglvtnfet_acc, eglvtvnfet_acc, egpfet_acc, egvpfet_acc, pfet_rf, eglvtnfet_rf, eglvtvnfet_rf, pfet_rfseg, eglvtnfet_rfseg, eglvtvnfet_rfseg*
        - The default value of the models in pre-layout assumes no WPE effect whereas the P-cell adds Nwell layer at the minimum DRM distance.
    - Modeling inaccuracy of LOD effect :
        - Models: *egnfet_acc, egvnfet_acc, eglvtpfet_acc, eglvtvpfet_acc, eglvtpfet_rf, eglvtvpfet_rf, eglvtpfet_rfseg, eglvtvpfet_rfseg*
            - The models under-estimate the linear and saturation currents by 5% at small SA and SB values (<0.4um) for narrow-short devices (W<0.3um, L< 0.5 um)
        - Models: eglvtnfet_acc, eglvtvnfet_acc, eglvtnfet_rf, eglvtvnfet_rf, , eglvtnfet_rfseg, eglvtvnfet_rfseg, egpfet_acc, egvpfet_acc
            - Inaccurate stress STI modeling when nf>1 in pre-layout mode for large L. Please use post-layout simulation to recover accuracy
    - Leakage in CMIM16acc :
        - Models: *cmim16acc, cmim16acc_acc, cmim16acc_sh, cmim16acc_sh_acc, cmim16acc_2p, cmim16acc_2p_acc*
            - The minimum leakage in CMIM16acc device is wrongly setup. We recommend to use the typical and maximum values
    - ESD models:
        - Models: *esdnfet_nova, esdegnfet_nova, esdvnpn_eg_nova, esdvpnp_eg_nova, esdndsx_eg_nova, esdvnpn_nova, esdvpnp_nova , esdndsx_nova, esdnfet, esdegnfet, esdvnpn_eg, esdvpnp_eg, esdndsx_eg, esdvnpn, esdvpnp , esdndsx*
            - Non-veriloga models are dedicated to SST simulation using Spectre or GoldenGate only. Veriloga models are strongly recommended for other simulators and other simulation analysis.
            - The SOA is implemented for the non-Verilog-a models
    - ESD Diodes:
        - Models: *esdvnpn_eg_va, esdvpnp_eg_va, esdndsx_eg_va, esdvnpn_va, esdvpnp_va , esdndsx_va*
            - Models were historically developed for ESD diodes PCELLs
            - Reference layouts for diodes are now the ones from ESDKIT library and ESD models are optimized for best describing diodes with these layouts.

- Diodes layouts have diverged from PCELLs, and there might now be a miscorrelation between models and PCELLs for ESD behaviour.

- ESD Low Cap:
  - Models: *esd_lowcap*
    - In AC signals, voltage dependence of capacitance is not accurately modeled. Model to measurement error is overestimated, by up to 40% at 1V.
    - Current is underestimated in Spectre / Hspice versus Eldo, especially for low temperature.
- ESD Ultra Low Cap EG:
  - Current is underestimated in spectre and hspice vs eldo, especially for low temperatures
- Inductors and Varactors :
  - R($freq) expression is not considered during transient simulation with spectre. Issue has been reported to Cadence (CCR1769638).
- VNPN Bipolar:
  - Collector current oscillates around the correct behavior (reproduced with AFS and ADS) at high frequency (F > 1 GHz).
- SG & EG Varactors:
  - Access resistance is overestimated at lower frequency in AFS and ADS. Support of voltage dependent resistors is missing in these simulators.
- Ageing models are available in Eldo, Hspice and Spectre :
  - Ageing models for xa –hspice are not provided in this PDK
- Due to R3 implementation issue in Goldengate, flicker noise for discrete resistors is 10% under-estimated (Golden Gate 4.10.0). This issue has been reported to Keysight
- Missing parameters in DCOP Back-Annotation with GoldenGate for utsoi 2.20 models (egnfet_acc,lvtnfet_rf ….) :
  - *–Id, -Is, -Ig, -Vdsat_marg, -vdsat, -vth_drive, -FT, -Dtsh*
- Minor problems identified during hspice soa validation :
  - With hcdgated/esdndsx_eg, NF1 rule is not properly detected.
  - With eglvt fet family, possible bad detection on MO4 rule, further analysis on-going
  - With rvt pfet_rf NF1 rule is not properly detected.

- <u>Calibre DRC:</u>
  - MTFlex run cannot start with LSF (whereas it does in MT with LSF) or when CI was launched from Virtuoso (whereas it does when directly launched from a terminal).
    - Workaround: Set this environment variable (supported by any Calibre release) as follows: CALIBRE_CI_REMOTE_COMMAND_USE_BASH 1

- <u>PVS DRC is not supported in this PDK release</u>

- <u>LVS:</u>

- When defining mconbot == mcontop == (3 or 5) with shielded MOM capacitor, the psub pin is considered as NWELL, and so is the same as shap.
  - To achieve correct LVS, connection of psub to shap is required
- Lvsres devices on M1, M2 or M3 are not extracted for PEX flows over esd devices (ie, under MKR_esd_local or ESDIMP_dg or ESD;CDM or ESD;HBM layers).
- Transistors : nfing comparison (when enabled) is not working when parallel reduction if disabled (HD tickets #83421, #8359)

- General PEX:
  - Please note that stack description for PEX tools (StarRCXT and QuantusQRC) is not fully aligned on DRM description regarding passivation layers above Alucap (AP). This is considered negligible for common PEX applications. EMAG tools (Momentum, EMX) are fully aligned on DRM description in order to provide the best-in-class accuracy for electromagnetic simulations of RF structures.

- QRC:
  - The following warnings are expected during QRC extraction and can be ignored :
    - *WARNING (CAPGEN-41475): Via layer 'V1FILL' resistance value is <= 0.*
    - *Ignoring via definition in p2lvsfile, via will be shorted*
    - *WARNING (CAPGEN-41475): Via layer 'V2FILL' resistance value is <= 0.*
    - *Ignoring via definition in p2lvsfile, via will be shorted*
    - *…*

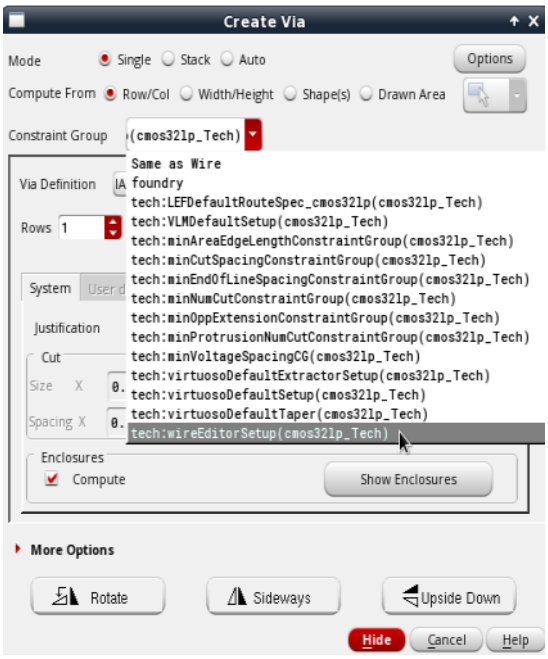
- EMX:
  - With default settings, performing EM simulations on a MOM topology is not accurate, since there are many fingers of metal which have a theoretical rectangular shape, which is not the real life in process (shapes non manhattan, OPC and so on …).
  - It is not possible to define a conformal layer in the proc file.
    - Workaround: Conformal layer are approximated by a planar layers in the proc files.
    - For the cmim description, an equivalent dielectric mim layer thickness is re-computed and defined in the proc file.
  - Description of resistivity of M1 & Mx layers are not fully aligned with latest DRM values. It is considered negligible.

- EMIR:
  - Ipeak values in EMIR tools (Totem, Voltus, CustomSimRA) are not aligned with latest 28FDSOI Design-Rule Manual

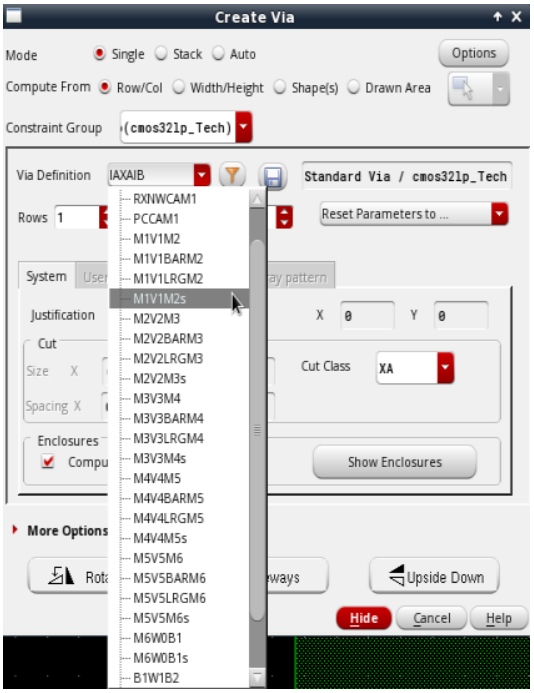
- Virtuoso Library:
  - Update PCell issue when changing ctkrev to previous version 1_0_RF. Re-opening 1_0_RF designs is working properly and updating to 1_1_RF ctkrev is also correct. But when changing back to previous 1_0_RF version, there is a pcell eval failed error with following message: “Pcell does not exist in version "1_0_rf".

- Workaround: force ctkrev device parameter in CIW (or with a skill script) to 1_0_RF.

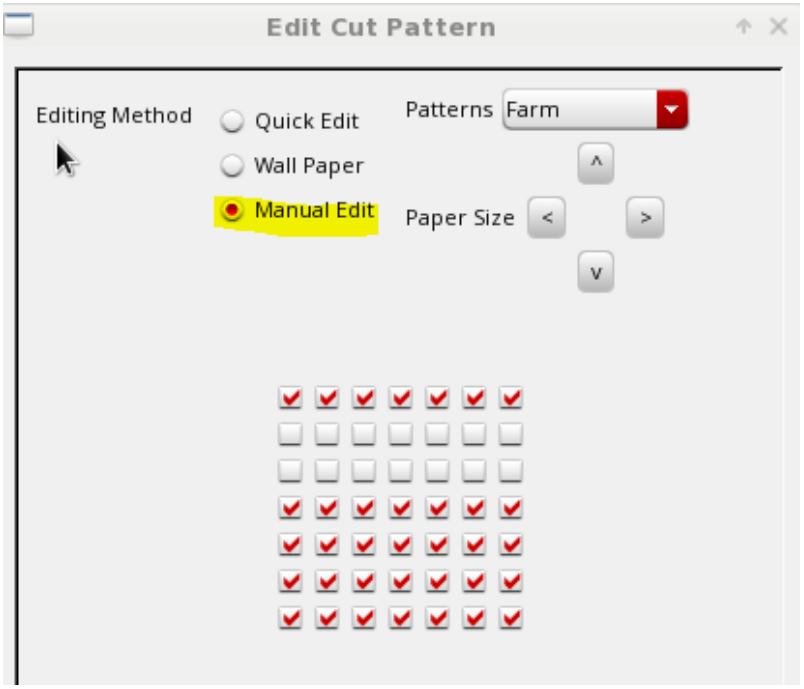
- Some warnings and errors are displayed in CIW during Virtuoso due to a setup issue with AFS simulator. They can be ignored.
  - *WARNING (ADE-5033): Cannot find the environment variable 'ignoreToLoadComponentsString' for tool 'afs.envOpts'.*
  - *Its internal default value will be used.*
  - *WARNING (ADE-5034): Unable to access the default environment variables in the simulator's*
  - *global .cdsenv file ('<your_install_dir>/tools/dfII/etc/tools/afs/.cdsenv')*
  - *because the file is missing or out-of-date. Till this problem exists, internal*
  - *default values will be used for these environment variables during this session.*
  - **WARNING* envGetVal: Could not find variable 'nport_default_passivity'*
  - *in tool[.partition] 'afs.opts'.*
  - *ERROR (ADE-5007): Variable 'nport_default_passivity': Invalid value specified. Value should be a string.*
- Multiplicity is not working with VXL for EDMOS
- In order to avoid unexpected netlisting issues due to a known Virtuoso limitation, the change of device name in symbol property and in Find&Replace is not allowed anymore.
  - Work-around : Use the dedicated “Schematic Cell Replacement” utility available from Right-Click Mouse on schematic
- Standard vias ‘s’ are not available when TAFKit is loaded in the environment. By default, via constraint group is “VirtuosoDefaultSetup” (same as wire) then available vias are:



Available vias are now the following ones:



- CreateVia seems to give bad number of contacts with large spacing of arrays (example DRM rule 2x51d). This is the correct behavior of Virtuoso.
    - If you select the property of the via, then “Edit Cut Pattern” > “Manual Edit”, you will see the description of the array of via.



        - In this example, matrix 7x7 is requested, but due to DRM rule spacing of large array of via (example 2x51d), 2 columns of via are removed from the matrix.
    - For all resistors, in order to remap the old parameter ‘m’ (multiplicity) on ‘pbar’ (parallel stripes), both parameters ‘ser’ and ‘pbar’ can be at the same time more than 1 only in schematic views. Then if you create a layout using the command “Generate all from source”, as the pcell cannot support ‘ser’ and ‘pbar’ both more than 1, the pcell is drawn with “pbar=1”
        - The parameters ‘ser’ and ‘pbar’ should be both more than 1 only when you migrate a previous design with a multiplicity different than 1. With a new instance, we strongly recommend to have one of ‘ser’ or ‘pbar’ equal to 1
    - Gate spacing has no effect on computation of source and drain areas (as/ad)
        - Workaround : Designer can modify the as/ad values according to its design using “Drain/Source Contact Selection = user” or rely on Post-Layout Extraction
    - When opening an old design in DK 2.7 or 2.7.a, some pcells could change: it is possible that your original design is not preserved. This is due to the change of pcell code from MGEN (DK 2.5 and before) to skill (DK from 2.7).
        - Workaround: If you need to preserve your design, run the procedure UpdatePcell with ctkrev version 2.5.
    - Layers unsupported in metal stack still have type “cut” in order to keep the cutsizes in the layer map table. In this way we are able to streamOut existing designs containing these eventual layers, but some warnings can appear during streamOut.
    - Some width and area rules are not respected on devices. Here is the list of rules which could be flash on some devices :
        - NGATE.B.1, NGATE.B.3, NW.EN.2, NW.EX.1, PWB.W.1, FD_GEN.5, PLDDSOI.B.2, NLDDSOI.B.3, HSSOI.W.1, HSSOI.EN.1.2, HSSOI.EN.4.1, GRB_BH03, GRB_PH03, GRB_BV03, GRB_CV03, GRB_XW03, GRB_LW03, GRB_BF01, GRB_BF03, GRB_BN03, GRB_BP03, GRB_MY01, GRB_MY03, GRB_N301, GRB_NW01, GRB_NW03, GR51, GR51a, GR101a, GR101aa, GRLVT10_noNW, GRLVT10_NW, GRRVT10_noNW, GRRVT10_NW, GR351a, GR250, GR251a, GR260a, GREG11a, GREG21, GREG30, GREG34, GREG260, GR3T02, GR3T18, GR3T18b, GR501a, GR501aSE, GR501d, HSSOI.A.1, HSSOI.EX.11, EGLVT.EX.2
        - Workaround: Designers have to extend those layers or simply connect the device in metal to remove the corresponding rule.
    - Some width and area rules are not respected on techfile vias. Here is the list of rules waived per default standards vias :
        - GRB_BH03, GRB_PH03, GRB_BF01, GRB_BF03, GRB_BN03, GRB_BP03, GRB_MY01, GRB_MY03, GRB_NW01, GRB_NW03, GR51, GR51a, GR101a, GR101aa, GR351a, GR250, GR251a, GR209_or, GR2x01a_B1, GR2x01a_B2, GR8x01a_IA, GR8x00b_IB, GR8x01a_IB, GR999aa_BP, GR999aa_NW, GR999aa_VV, GR999aa_RX, GR999aa_PC, GR999aa_M1, GR999aa_M2, GR999aa_M3, GR999aa_M4, GR999aa_M5, GR999aa_M6, GR999aa_B1, GR999aa_B2, GR999aa_IA, GR999aa_IB, GR999aa_LB, GR999aa_CA, GR999aa_V1, GR999aa_V1BAR, GR999aa_V1LRG, GR999aa_V2, GR999aa_V2BAR, GR999aa_V2LRG, GR999aa_V3, GR999aa_V3BAR, GR999aa_V3LRG, GR999aa_V4, GR999aa_V4BAR, GR999aa_V4LRG, GR999aa_V5, GR999aa_V5BAR, GR999aa_V5LRG, GR999aa_W0, GR999aa_W1, GR999aa_XA, GR999aa_YZ, GRGUARDEDG, GR501a,

GR501aSE, GR501d, GR601a_M2, GR601aSE_M2, GR601a_M3, GR601aSE_M3, GR601a_M4, GR601aSE_M4, GR601a_M5, GR601aSE_M5, GR601a_M6, GR601aSE_M6, ID.IP.2, PWB.W.1, LUP.D.1.2, FC44S.R.2, PLDDSOI.B.2, NLDDSOI.B.3, HYBRID.A.1, HYBRID.R.1, DTPC.R.2, ID.MPW.1, ID.BEOL.1, ST_268b_FD, EMET.DEN.1, EMET.DEN.2, EMET.DEN.3, EMET.DEN.4, EMET.DEN.5, EMET.DEN.6, EMET.DEN.7, EMET.DEN.8, EMET.DEN.9, EMET.DEN.10, EMET.DEN.11, EMET.DEN.12, RX.DEN.1, PC.DEN.1, M1.DEN.1, M2.DEN.1, M3.DEN.1, M4.DEN.1, M5.DEN.1, M6.DEN.1, B1.DEN.1, B2.DEN.1, IA.DEN.1, IB.DEN.1, LB.DEN.1, DV.DEN.1

    - Workaround: Designers have to stretch all requested layers.

- For mosfet core with small gate length, the DRC requires poly dummies on both side of the gate, rule (ST_105_or). But dummies are not automatic activated by callbacks.
    - Workaround: Designers have to activate the parameter “ACLV PC fill” with option Both. The Pcell will draw PC dummies on both side of the gate.
- Egncap/Egpcap: When designer selects “Default” button, capacitance value depletion is reset to nil
    - Workaround: value is re-computed when some other parameters are changed
- Automatic routing with VSR does not respect the minimum MLAST enclosure on W0 (rule ST_2x60_or).
    - The rule 2x60f, with smaller enclosures, is used instead.
    - The issue is confirmed by Cadence, we are waiting for the CCR resolution.
    - Workaround: Modify the enclosure with via options.
- Warning during EM/IR TOTEM simulation
    - The following warnings still appears during TOTEM simulation:
        - WARNING(TEC-126): Missing Via definition between metal layer: IA and HKBOTMIMD!
        - WARNING(TEC-126): Missing Via definition between metal layer: HKBOTMIMD and HKTOPMIMD!
    - Indeed, these vias are not present in the EM techfiles and the connectivity is assumed by LVS.
    - So there is no issue during the simulation, these warnings can be waived and they will be discussed with ANSYS for removal.
- Due to a limitation in Virtuoso, Fluid guardrings drawn with wrap mode around mos fets are not DRC clean.
    - GRSE3, GR352, GR352a , GREG207, NLDDSOI.B.1.2, NLDDSOI.B.2, PLDDGO2.B.1.1, PLDDGO2.B.1.2, HSSOI.D.12
    - Workaround: Use path or rectangle modes.
- Some rules are not respected on techfile vias, they are considered as fixed in design :
    - GRB_BF03, GRB_NW03, GR51, GR51a, GR101a, GR101aa, GR351a, GR251a, GRCABAR.R.1, GR204_or, GR209_or, GR2x01a_B1, GR2x01a_B2, GR2x51d_W0, GR2x93_W0BAR, GR2x51d_W1, GR2x93_W1BAR, GR8x01a_IA, GR8x01a_IB, GR501a, GR501aSE, GR501d, GR551_V1LRGd, GR553q2_V1, GR551_V2LRGd, GR553q2_V2, GR551_V3LRGd, GR553q2_V3, GR551_V4LRGd, GR553q2_V4, GR551_V5LRGd, GR553q2_V5, GR601a_M2,

GR601aSE_M2, GR601a_M3, GR601aSE_M3, GR601a_M4, GR601aSE_M4, GR601a_M5, GR601aSE_M5, GR601a_M6, GR601aSE_M6, ID.IP.2, ID.MPW.1, LUP.D.1.2, RX.DEN.1, PC.DEN.1, M1.DEN.1, M2.DEN.1, M3.DEN.1, M4.DEN.1, M5.DEN.1, M6.DEN.1, B1.DEN.1, B2.DEN.1, IA.DEN.1, IB.DEN.1, LB.DEN.1, DV.DEN.1, EMET.DEN.6, EMET.DEN.7, FC.R.2.V1, FC.R.2.V2, FC.R.2.V3, FC.R.2.V4, FC.R.2.V5, FC.R.2.W0, FC.R.2.W1, ST_8x93_YZ, ST_8Bx93, ST_LB93, FDSOI.R.1, PLDDSOI.B.2, NLDDSOI.B.3, HYBRID.A.1, HYBRID.R.1, DTPC.R.2, ID.BEOL.1, CA.EX.1, ST_268b_FD, ST_B_BN03, ST_B_BN07, ST_B_BP03, ST_B_BH03, ST_B_PH03

    - Workaround: stretch all requested layers.
- Routing done with techfile is not always DRC clean.
    - Workaround: Run DRC as soon as possible. Automatic routing is different from a run to another, so you can run several times.
- All mos types : fets, sram, ED, RF, esd : Parameters ps and pd cannot be parametrized
- List of known DRC violations in pcells. Most of these violation can be cleaned during design integration :

Device	**DRC error**	**configuration**
hlvtnfet_b hlvtnfetnp hlvtnfet hlvtpfet_b hlvtpfet hlvtpfettw lvtnfet_b lvtnfetnp lvtnfet lvtpfet_b lvtpfet lvtpfettw nfet_b nfet nfettw pfet_b pfetnp pfet	ST_102_or GR101b	1 finger , small length , pc dummies and CA with 96nm <gatespacing =< 114nm PC enclosed area for small size of device and when top and bottom gate contacts.
egnexti	FDSOI.R.1	
egpext	GR3T18 GR3T18b NWED.EN.1	

egpfet egpfet_b egpfetnp egvlvtnfet egvlvtnfetnp egvlvtnfet_b eglvtpspfet_b eglvtnfet_b eglvtnfetnp egvpfet egvpfet_b egvpfetnp egvnfettw egvnfet egvnfet_b	GREG207	
esdlvtnfet_fdsoi	B_OP03	
	SB729a	
esdlvtpfet_fdsoi	B_OP03	
	SB729a	
esdpfet_fdsoi	B_OP03	
	SB729a	
esdnfet_fdsoi	B_OP03	
	SB729a	
esdvpnp esdvnpn	604d_{M2-M3} 604e_{M2-M3}	
esdndsx	GR604d_{M2-M3}	
	GR604e_{M2-M3}	
esdndsx_eg esdvnpn_eg esdvpnp_eg	GR504c1/c2/c3 GR504d GR504e GR604c1/c2/c3_{M2-M3} GR604d__{M2-M3} GR604e__{M2-M3}	
ind_hq_6U1x_2T8x_LB	I_DUM.DEN.2.2_{M2-M6/IA} I_DUM.DEN.4.2_IB	
ind_lohq_6U1x_2T8x_LB	I_DUM.DEN.2.2_{M2-M6/IA} I_DUM.DEN.2_{M2-M6/IA/IB}	
ind_lohq_high_perf_6U1x_2T8x_LB	I_DUM.DEN.2_{M2-M6IA/IB} I_DUM.DEN.2.2_{M2-M6/IA} I_DUM.DEN.4.2_IB	default
inddif_hq_6U1x_2T8x_LB	I_DUM.DEN.2.2_{M2-M6/IA} I_DUM.DEN.4.2_IB	

inddif_lohq_6U1x_2T8x_LB	I_DUM.DEN.2.2_{M2-M6/IA} I_DUM.DEN.2_{M2-M6/IA/IB}	
inddif_lohq_high_perf_6U1x_2T8x_LB	I_DUM.DEN.2_{M2-M6IA/IB} I_DUM.DEN.2.2_{M2-M6/IA} I_DUM.DEN.4.2_IB	
cmom_5U1x_2T8x_LB_sh cmom_5U1x_2T8x_LB_2p	2x61 2x60 555j 611	Top metal connection=7
cmom_6U1x_2T8x_LB_sh cmom_6U1x_2T8x_LB_wo_via_sh cmom_6U1x_2U2x_2T8x_LB_sh cmom_6U1x_2U2x_2T8x_LB_wo_via_sh	MOM.D.5.or	
mesh	GR8x60a_YX	

Contact Information

<This section contains information on how the users can contact the provider. If link to an application is given for example, CAD HelpDesk, guiding steps should be provided for selecting the relevant category.>

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

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