C28SOI_SC_12_COREPBP4_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 4 nm

Overview

- C28SOI_SC_12_COREPBP4_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

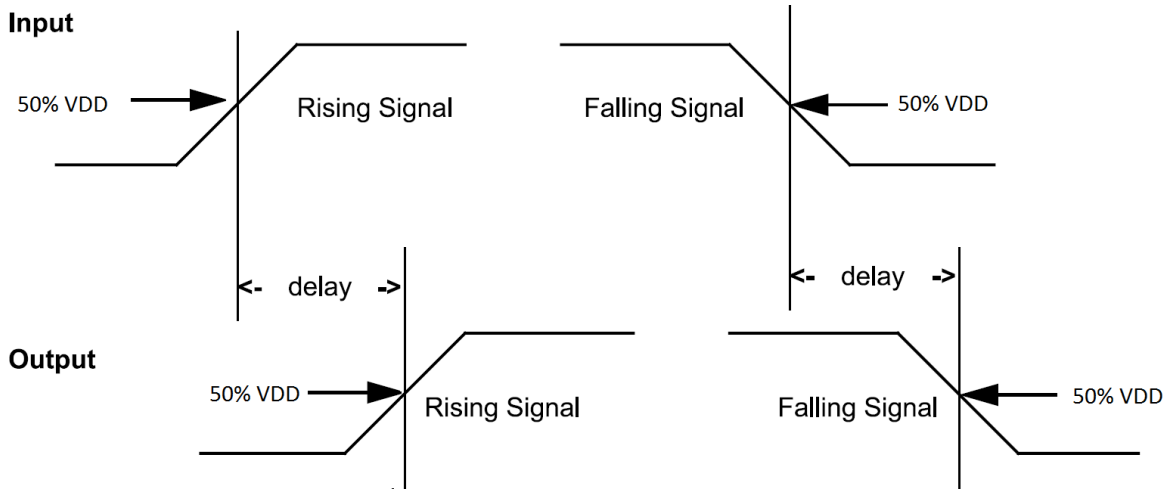


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

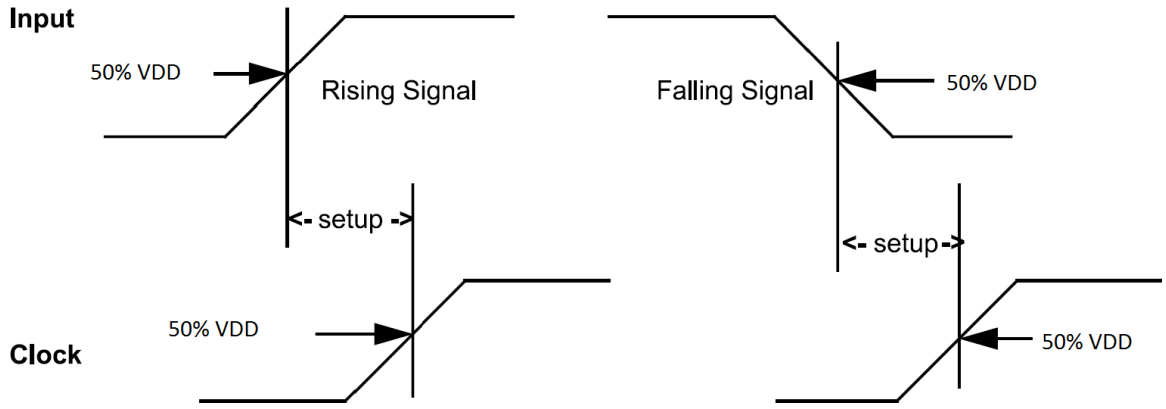


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

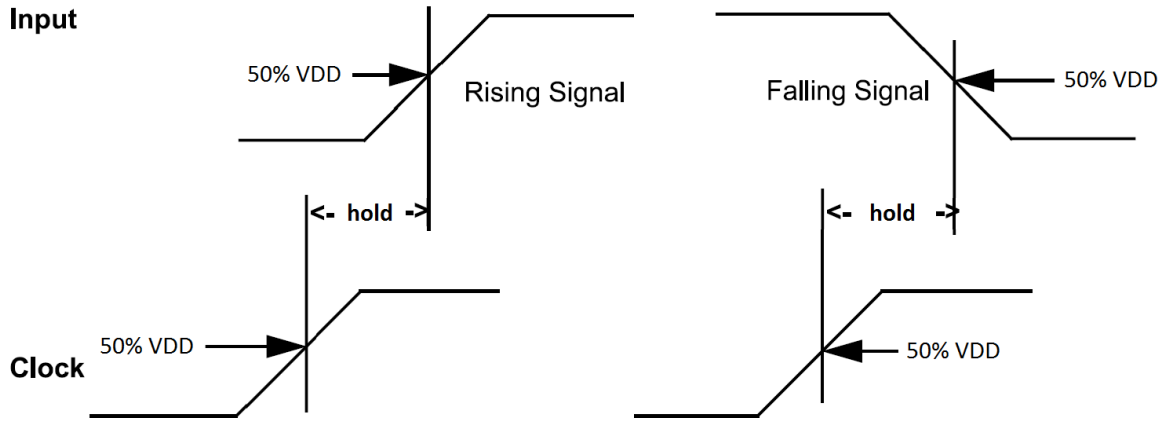


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

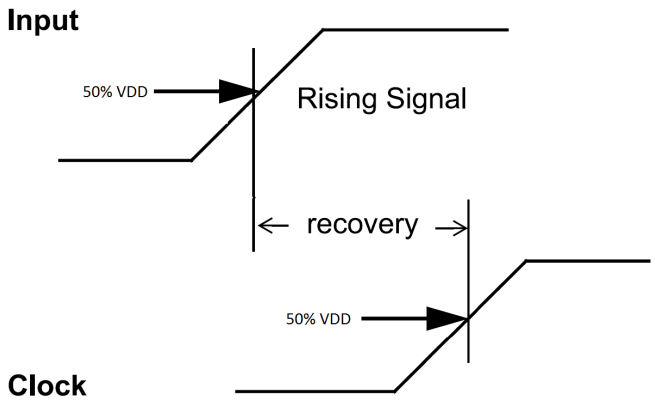


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

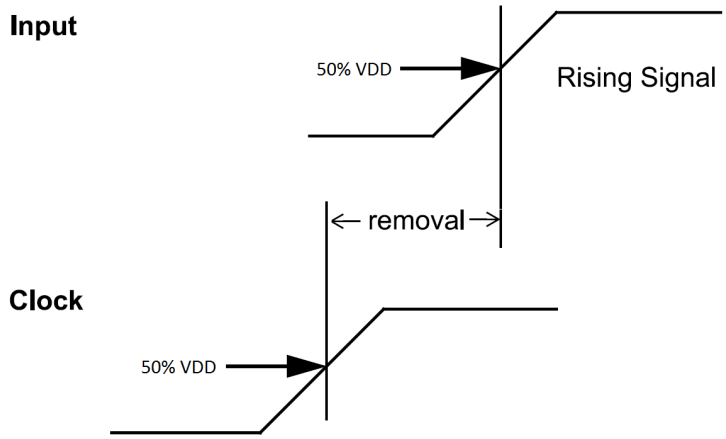


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

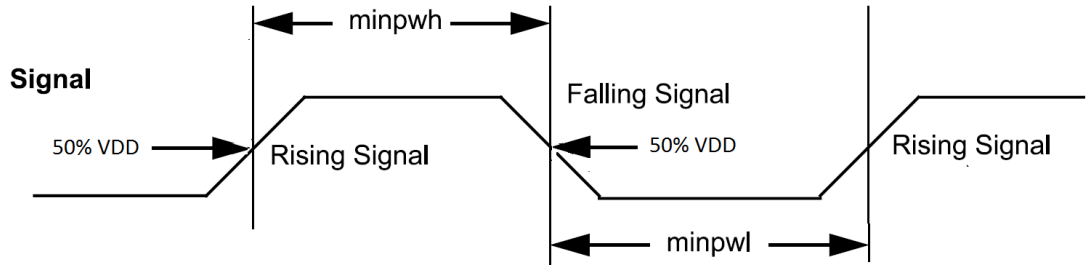


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

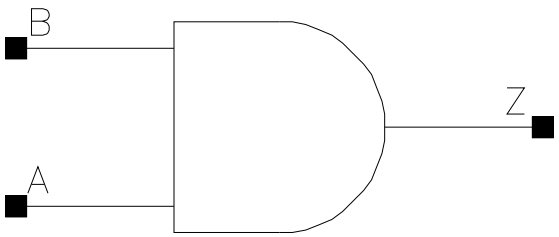
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X25_P4	1.200	1.088	1.3056
X33_P4	1.200	1.360	1.6320
X42_P4	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0008	0.0012	0.0018	0.0022
B	0.0007	0.0011	0.0017	0.0022
	X42_P4			
A	0.0022			
B	0.0022			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0207	0.0171	1.5214	0.7698
A to Z ↑	0.0163	0.0163	2.0572	0.9937
B to Z ↓	0.0195	0.0160	1.5204	0.7700
B to Z ↑	0.0180	0.0178	2.0564	0.9926
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0177	0.0171	0.5099	0.3799

A to Z ↑	0.0157	0.0165	0.6581	0.4978
B to Z ↓	0.0167	0.0155	0.5090	0.3791
B to Z ↑	0.0172	0.0178	0.6576	0.4977
	X42_P4		**X42_P4**	
A to Z ↓	0.0185		0.3082	
A to Z ↑	0.0180		0.3992	
B to Z ↓	0.0170		0.3074	
B to Z ↑	0.0194		0.3991	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	1.919e-04	1.000e-20
X16_P4	4.278e-04	1.000e-20
X25_P4	6.216e-04	1.000e-20
X33_P4	8.514e-04	1.000e-20
X42_P4	9.988e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	1.610e-05	2.891e-05	4.577e-05	1.104e-04
B (output stable)	3.178e-05	5.568e-05	8.786e-05	3.284e-04
A to Z	4.114e-03	7.406e-03	1.128e-02	1.504e-02
B to Z	3.977e-03	7.177e-03	1.093e-02	1.423e-02
	X42_P4			
A (output stable)	1.097e-04			
B (output stable)	3.259e-04			
A to Z	1.810e-02			
B to Z	1.733e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

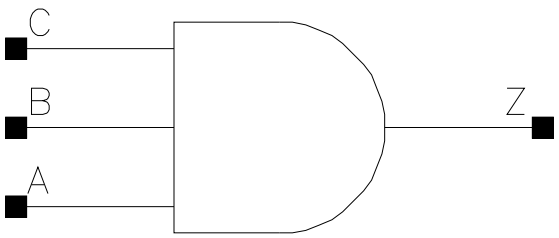
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X25_P4	1.200	1.360	1.6320
X33_P4	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0008	0.0012	0.0019	0.0023
B	0.0007	0.0011	0.0017	0.0021
C	0.0007	0.0011	0.0016	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0221	0.0186	1.5354	0.7510
A to Z ↑	0.0205	0.0202	2.0776	0.9873
B to Z ↓	0.0213	0.0177	1.5356	0.7509
B to Z ↑	0.0219	0.0216	2.0764	0.9871
C to Z ↓	0.0202	0.0165	1.5349	0.7493
C to Z ↑	0.0233	0.0226	2.0740	0.9869
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0186	0.0178	0.5154	0.3848

A to Z ↑	0.0194	0.0192	0.6776	0.5076
B to Z ↓	0.0177	0.0168	0.5146	0.3844
B to Z ↑	0.0209	0.0207	0.6768	0.5071
C to Z ↓	0.0166	0.0158	0.5143	0.3842
C to Z ↑	0.0221	0.0219	0.6771	0.5072

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	1.974e-04	1.000e-20
X17_P4	4.402e-04	1.000e-20
X25_P4	6.288e-04	1.000e-20
X33_P4	8.623e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	1.893e-05	3.702e-05	4.982e-05	6.809e-05
B (output stable)	2.757e-05	5.150e-05	7.479e-05	1.001e-04
C (output stable)	5.993e-05	1.119e-04	1.696e-04	2.335e-04
A to Z	4.529e-03	8.398e-03	1.216e-02	1.597e-02
B to Z	4.376e-03	8.132e-03	1.171e-02	1.538e-02
C to Z	4.246e-03	7.884e-03	1.132e-02	1.484e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

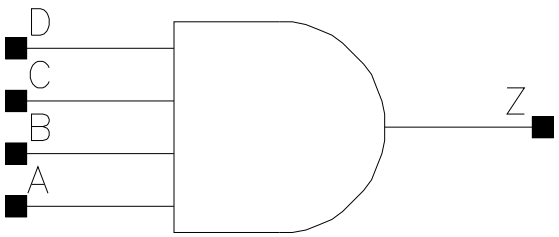
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X6_P4	1.200	1.088	1.3056
X20_P4	1.200	2.312	2.7744
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P4	X6_P4	X20_P4	X27_P4
A	0.0006	0.0008	0.0019	0.0022
B	0.0005	0.0008	0.0019	0.0022
C	0.0005	0.0008	0.0019	0.0022
D	0.0006	0.0008	0.0019	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X6_P4	X4_P4	X6_P4
A to Z ↓	0.0225	0.0203	2.8238	1.8562
A to Z ↑	0.0204	0.0162	6.5043	3.5730
B to Z ↓	0.0216	0.0189	2.8235	1.8563
B to Z ↑	0.0223	0.0174	6.5018	3.5740
C to Z ↓	0.0232	0.0218	2.7893	1.8613
C to Z ↑	0.0210	0.0166	6.5055	3.5746

D to Z ↓	0.0223	0.0201	2.7862	1.8596
D to Z ↑	0.0233	0.0181	6.5082	3.5721
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0198	0.0180	0.5434	0.3851
A to Z ↑	0.0170	0.0197	1.2029	0.9183
B to Z ↓	0.0180	0.0164	0.5428	0.3843
B to Z ↑	0.0182	0.0211	1.2026	0.9182
C to Z ↓	0.0194	0.0175	0.5458	0.3859
C to Z ↑	0.0158	0.0181	1.2009	0.9157
D to Z ↓	0.0174	0.0160	0.5444	0.3847
D to Z ↑	0.0168	0.0195	1.1997	0.9154

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	8.139e-05	1.000e-20
X6_P4	2.086e-04	1.000e-20
X20_P4	6.550e-04	1.000e-20
X27_P4	8.764e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	6.450e-04	1.081e-03	3.142e-03	3.824e-03
B (output stable)	6.048e-04	1.004e-03	2.940e-03	3.593e-03
C (output stable)	6.212e-04	1.088e-03	2.820e-03	3.458e-03
D (output stable)	5.863e-04	1.011e-03	2.594e-03	3.240e-03
A to Z	2.651e-03	4.260e-03	1.288e-02	1.660e-02
B to Z	2.553e-03	4.059e-03	1.208e-02	1.574e-02
C to Z	2.673e-03	4.413e-03	1.165e-02	1.487e-02
D to Z	2.572e-03	4.205e-03	1.083e-02	1.408e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

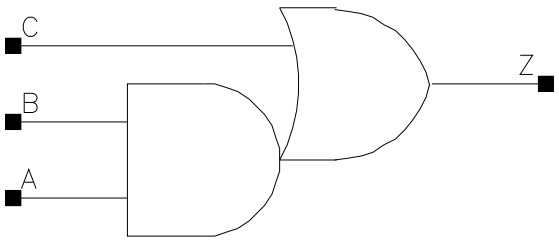
Pin Cycle (vdds)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0011	0.0023
B	0.0007	0.0011	0.0021
C	0.0008	0.0012	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0257	0.0235	1.5505	0.7596
A to Z ↑	0.0168	0.0157	1.9938	0.9791
B to Z ↓	0.0238	0.0215	1.5464	0.7571
B to Z ↑	0.0187	0.0176	1.9910	0.9792
C to Z ↓	0.0236	0.0214	1.5461	0.7571
C to Z ↑	0.0163	0.0158	1.9789	0.9739
	X33_P4		**X33_P4**	
A to Z ↓	0.0231		0.3856	
A to Z ↑	0.0158		0.4940	

B to Z ↓	0.0216		0.3849	
B to Z ↑	0.0174		0.4940	
C to Z ↓	0.0214		0.3848	
C to Z ↑	0.0156		0.4917	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	1.622e-04	1.000e-20
X17_P4	3.593e-04	1.000e-20
X33_P4	7.064e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	5.768e-05	9.026e-05	2.106e-04
B (output stable)	6.457e-05	1.050e-04	2.625e-04
C (output stable)	6.636e-05	1.132e-04	2.555e-04
A to Z	4.336e-03	8.008e-03	1.567e-02
B to Z	4.160e-03	7.682e-03	1.498e-02
C to Z	4.513e-03	8.303e-03	1.643e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

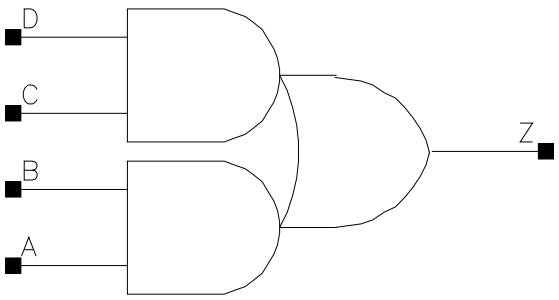
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0011	0.0022
B	0.0008	0.0011	0.0020
C	0.0007	0.0010	0.0022
D	0.0007	0.0011	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0275	0.0241	1.5012	0.7579
A to Z ↑	0.0220	0.0207	1.9675	0.9801
B to Z ↓	0.0254	0.0222	1.4960	0.7553
B to Z ↑	0.0238	0.0228	1.9676	0.9803

C to Z ↓	0.0264	0.0237	1.4961	0.7558
C to Z ↑	0.0186	0.0176	1.9600	0.9764
D to Z ↓	0.0251	0.0224	1.4934	0.7542
D to Z ↑	0.0207	0.0194	1.9599	0.9752
	X33_P4		**X33_P4**	
A to Z ↓	0.0232		0.3865	
A to Z ↑	0.0192		0.4967	
B to Z ↓	0.0218		0.3864	
B to Z ↑	0.0212		0.4961	
C to Z ↓	0.0228		0.3858	
C to Z ↑	0.0164		0.4948	
D to Z ↓	0.0216		0.3853	
D to Z ↑	0.0180		0.4943	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	2.071e-04	1.000e-20
X17_P4	4.464e-04	1.000e-20
X33_P4	8.747e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	4.088e-05	5.823e-05	8.349e-05
B (output stable)	1.325e-04	1.722e-04	1.149e-04
C (output stable)	5.327e-05	8.582e-05	1.984e-04
D (output stable)	6.040e-05	1.020e-04	2.395e-04
A to Z	5.420e-03	9.525e-03	1.804e-02
B to Z	5.112e-03	9.075e-03	1.747e-02
C to Z	4.848e-03	8.570e-03	1.613e-02
D to Z	4.698e-03	8.298e-03	1.558e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

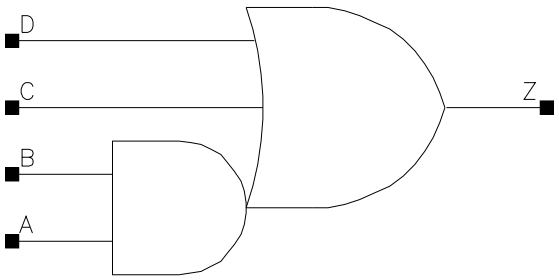
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	0.952	1.1424
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0011	0.0021
B	0.0007	0.0011	0.0021
C	0.0007	0.0011	0.0021
D	0.0007	0.0011	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0330	0.0294	1.6013	0.7940
A to Z ↑	0.0180	0.0171	1.9852	1.0234
B to Z ↓	0.0316	0.0277	1.5972	0.7912
B to Z ↑	0.0199	0.0186	1.9818	1.0216
C to Z ↓	0.0312	0.0276	1.5964	0.7920
C to Z ↑	0.0176	0.0168	1.9695	1.0158

D to Z ↓	0.0322	0.0287	1.5971	0.7924
D to Z ↑	0.0172	0.0167	1.9685	1.0160
	X33_P4		**X33_P4**	
A to Z ↓	0.0302		0.3973	
A to Z ↑	0.0170		0.4948	
B to Z ↓	0.0273		0.3954	
B to Z ↑	0.0184		0.4950	
C to Z ↓	0.0286		0.3961	
C to Z ↑	0.0167		0.4926	
D to Z ↓	0.0291		0.3964	
D to Z ↑	0.0160		0.4916	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	1.270e-04	1.000e-20
X17_P4	2.841e-04	1.000e-20
X33_P4	5.618e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	7.452e-05	1.320e-04	3.065e-04
B (output stable)	7.467e-05	1.289e-04	3.403e-04
C (output stable)	3.503e-05	6.595e-05	1.804e-04
D (output stable)	4.918e-05	9.133e-05	3.140e-04
A to Z	4.886e-03	8.710e-03	1.764e-02
B to Z	4.740e-03	8.400e-03	1.663e-02
C to Z	5.237e-03	9.306e-03	1.908e-02
D to Z	5.035e-03	8.981e-03	1.810e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

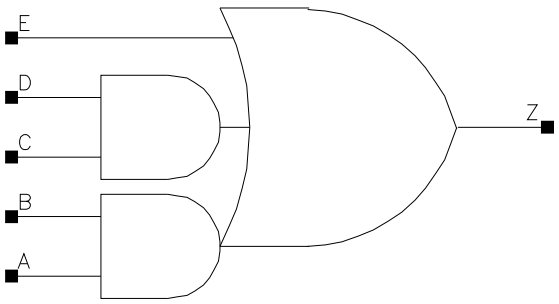
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.088	1.3056
X17_P4	1.200	1.224	1.4688
X33_P4	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0011	0.0022
B	0.0007	0.0011	0.0020
C	0.0008	0.0013	0.0022
D	0.0007	0.0011	0.0021
E	0.0007	0.0011	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0365	0.0320	1.5284	0.7742
A to Z ↑	0.0233	0.0209	1.9488	0.9848

B to Z ↓	0.0351	0.0304	1.5245	0.7726
B to Z ↑	0.0258	0.0230	1.9472	0.9840
C to Z ↓	0.0342	0.0313	1.5239	0.7725
C to Z ↑	0.0193	0.0174	1.9319	0.9787
D to Z ↓	0.0318	0.0286	1.5170	0.7683
D to Z ↑	0.0213	0.0190	1.9318	0.9780
E to Z ↓	0.0333	0.0296	1.5173	0.7698
E to Z ↑	0.0186	0.0167	1.9155	0.9718
	X33_P4		**X33_P4**	
A to Z ↓	0.0313		0.3976	
A to Z ↑	0.0216		0.4981	
B to Z ↓	0.0294		0.3969	
B to Z ↑	0.0237		0.4975	
C to Z ↓	0.0300		0.3965	
C to Z ↑	0.0174		0.4942	
D to Z ↓	0.0278		0.3949	
D to Z ↑	0.0191		0.4940	
E to Z ↓	0.0289		0.3954	
E to Z ↑	0.0168		0.4908	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	1.643e-04	1.000e-20
X17_P4	3.573e-04	1.000e-20
X33_P4	6.879e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.254e-05	3.607e-05	8.093e-05
B (output stable)	2.875e-05	4.166e-05	1.054e-04
C (output stable)	8.602e-05	1.174e-04	2.918e-04
D (output stable)	1.013e-04	1.421e-04	3.243e-04
E (output stable)	1.364e-04	1.818e-04	4.197e-04
A to Z	6.275e-03	1.077e-02	2.107e-02
B to Z	6.119e-03	1.046e-02	2.029e-02
C to Z	5.304e-03	9.321e-03	1.793e-02
D to Z	5.106e-03	8.926e-03	1.714e-02
E to Z	5.495e-03	9.545e-03	1.846e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

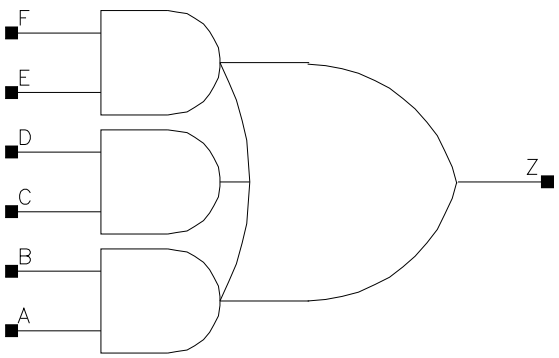
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.360	1.6320
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
A	0.0007	0.0008	0.0010	0.0022

B	0.0007	0.0008	0.0014	0.0020
C	0.0007	0.0008	0.0010	0.0021
D	0.0007	0.0008	0.0010	0.0020
E	0.0007	0.0009	0.0011	0.0022
F	0.0007	0.0008	0.0011	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0364	0.0351	2.9050	1.5419
A to Z ↑	0.0245	0.0242	3.7582	1.9964
B to Z ↓	0.0333	0.0323	2.8854	1.5330
B to Z ↑	0.0262	0.0261	3.7545	1.9941
C to Z ↓	0.0339	0.0331	2.8952	1.5378
C to Z ↑	0.0220	0.0218	3.7327	1.9837
D to Z ↓	0.0322	0.0315	2.8859	1.5328
D to Z ↑	0.0243	0.0241	3.7302	1.9815
E to Z ↓	0.0305	0.0305	2.8827	1.5321
E to Z ↑	0.0181	0.0181	3.7132	1.9730
F to Z ↓	0.0286	0.0285	2.8737	1.5267
F to Z ↑	0.0199	0.0200	3.7109	1.9726
	X17_P4	X33_P4	X17_P4	X33_P4
A to Z ↓	0.0338	0.0327	0.7774	0.3962
A to Z ↑	0.0231	0.0232	0.9882	0.5002
B to Z ↓	0.0317	0.0309	0.7728	0.3955
B to Z ↑	0.0254	0.0254	0.9874	0.4996
C to Z ↓	0.0326	0.0315	0.7755	0.3959
C to Z ↑	0.0209	0.0213	0.9828	0.4972
D to Z ↓	0.0307	0.0299	0.7725	0.3951
D to Z ↑	0.0230	0.0233	0.9823	0.4971
E to Z ↓	0.0300	0.0302	0.7724	0.3949
E to Z ↑	0.0174	0.0182	0.9784	0.4957
F to Z ↓	0.0281	0.0281	0.7696	0.3935
F to Z ↑	0.0192	0.0203	0.9784	0.4952

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	1.341e-04	1.000e-20
X8_P4	2.401e-04	1.000e-20
X17_P4	4.412e-04	1.000e-20
X33_P4	8.475e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	4.329e-05	5.069e-05	6.458e-05	1.168e-04
B (output stable)	1.067e-04	1.193e-04	1.251e-04	1.615e-04
C (output stable)	5.044e-05	6.007e-05	7.650e-05	1.733e-04
D (output stable)	5.754e-05	6.964e-05	8.776e-05	2.285e-04
E (output stable)	1.459e-04	1.772e-04	2.210e-04	3.723e-04
F (output stable)	1.488e-04	1.784e-04	2.329e-04	4.197e-04

A to Z	5.018e-03	7.167e-03	1.173e-02	2.240e-02
B to Z	4.661e-03	6.746e-03	1.114e-02	2.163e-02
C to Z	4.391e-03	6.395e-03	1.067e-02	2.040e-02
D to Z	4.221e-03	6.182e-03	1.033e-02	1.970e-02
E to Z	3.758e-03	5.639e-03	9.509e-03	1.863e-02
F to Z	3.590e-03	5.421e-03	9.178e-03	1.786e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

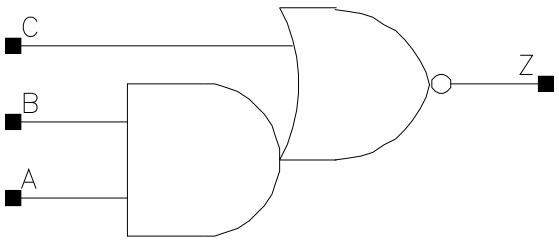
Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008
X44_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X33_P4	X44_P4
A	0.0009	0.0026	0.0054	0.0072
B	0.0008	0.0025	0.0050	0.0068
C	0.0010	0.0028	0.0055	0.0073

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0060	0.0061	2.5908	0.8770
A to Z ↑	0.0122	0.0125	3.6727	1.2370
B to Z ↓	0.0069	0.0072	2.6191	0.8894
B to Z ↑	0.0099	0.0098	3.6075	1.2375
C to Z ↓	0.0068	0.0070	1.5906	0.5447
C to Z ↑	0.0108	0.0108	3.3494	1.1400
	X33_P4	**X44_P4**	**X33_P4**	**X44_P4**
A to Z ↓	0.0063	0.0062	0.4477	0.3402

A to Z ↑	0.0125	0.0125	0.6207	0.4727
B to Z ↓	0.0072	0.0072	0.4539	0.3451
B to Z ↑	0.0097	0.0097	0.6190	0.4695
C to Z ↓	0.0085	0.0087	0.3232	0.2508
C to Z ↑	0.0106	0.0105	0.5717	0.4344

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P4	1.512e-04	1.000e-20
X17_P4	4.427e-04	1.000e-20
X33_P4	8.594e-04	1.000e-20
X44_P4	1.142e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	9.260e-05	2.661e-04	6.081e-04	7.876e-04
B (output stable)	1.023e-04	3.400e-04	7.548e-04	9.707e-04
C (output stable)	1.118e-04	3.340e-04	7.261e-04	9.604e-04
A to Z	2.391e-03	7.341e-03	1.462e-02	1.929e-02
B to Z	2.153e-03	6.292e-03	1.258e-02	1.659e-02
C to Z	2.992e-03	8.909e-03	1.737e-02	2.285e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

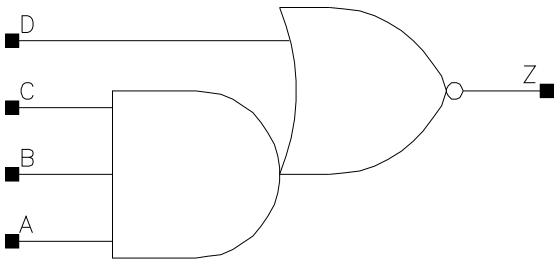
Pin Cycle (vdds)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X29_P4	1.200	3.536	4.2432
X38_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X29_P4	X38_P4
A	0.0009	0.0054	0.0072
B	0.0008	0.0052	0.0068
C	0.0008	0.0050	0.0066
D	0.0010	0.0056	0.0069

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X29_P4	X5_P4	X29_P4
A to Z ↓	0.0094	0.0098	3.5706	0.6222
A to Z ↑	0.0151	0.0151	3.6739	0.6135
B to Z ↓	0.0105	0.0105	3.5868	0.6257
B to Z ↑	0.0134	0.0132	3.6777	0.6191
C to Z ↓	0.0110	0.0109	3.6042	0.6296
C to Z ↑	0.0113	0.0109	3.6196	0.6245
D to Z ↓	0.0086	0.0104	1.6236	0.3251

D to Z ↑	0.0127	0.0125	3.1386	0.5321
	X38_P4		**X38_P4**	
A to Z ↓	0.0097		0.4832	
A to Z ↑	0.0148		0.4633	
B to Z ↓	0.0105		0.4862	
B to Z ↑	0.0129		0.4687	
C to Z ↓	0.0109		0.4892	
C to Z ↑	0.0106		0.4751	
D to Z ↓	0.0113		0.2709	
D to Z ↑	0.0121		0.4030	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.485e-04	1.000e-20
X29_P4	8.378e-04	1.000e-20
X38_P4	1.099e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X29_P4	X38_P4
A (output stable)	5.325e-05	4.356e-04	5.631e-04
B (output stable)	6.160e-05	4.927e-04	6.383e-04
C (output stable)	8.716e-05	7.778e-04	9.923e-04
D (output stable)	1.435e-04	1.051e-03	1.375e-03
A to Z	2.898e-03	1.767e-02	2.287e-02
B to Z	2.617e-03	1.544e-02	1.998e-02
C to Z	2.368e-03	1.343e-02	1.735e-02
D to Z	3.524e-03	2.063e-02	2.647e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

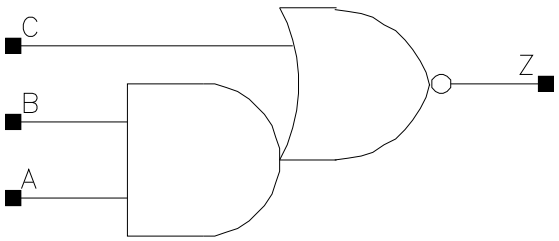
Pin Cycle (vdds)	X5_P4	X29_P4	X38_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X11_P4	1.200	1.088	1.3056
X16_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X11_P4	X16_P4	X23_P4
A	0.0010	0.0019	0.0029	0.0038
B	0.0009	0.0018	0.0027	0.0036
C	0.0010	0.0017	0.0026	0.0037
	X46_P4			
A	0.0073			
B	0.0070			
C	0.0073			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X11_P4	X6_P4	X11_P4
A to Z ↓	0.0078	0.0084	2.4992	1.2740
A to Z ↑	0.0116	0.0121	3.6659	1.7959
B to Z ↓	0.0091	0.0094	2.5246	1.2881

B to Z ↑	0.0097	0.0097	3.6129	1.8040
C to Z ↓	0.0041	0.0049	1.6392	0.9625
C to Z ↑	0.0102	0.0097	3.3798	1.6726
	X16_P4	**X23_P4**	**X16_P4**	**X23_P4**
A to Z ↓	0.0079	0.0081	0.8757	0.6607
A to Z ↑	0.0113	0.0115	1.2100	0.9188
B to Z ↓	0.0093	0.0093	0.8869	0.6680
B to Z ↑	0.0089	0.0090	1.2100	0.9235
C to Z ↓	0.0050	0.0040	0.6659	0.4211
C to Z ↑	0.0092	0.0100	1.1272	0.8547
	X46_P4		**X46_P4**	
A to Z ↓	0.0078		0.3392	
A to Z ↑	0.0112		0.4803	
B to Z ↓	0.0091		0.3433	
B to Z ↑	0.0087		0.4793	
C to Z ↓	0.0044		0.2150	
C to Z ↑	0.0103		0.4459	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P4	1.515e-04	1.000e-20
X11_P4	3.081e-04	1.000e-20
X16_P4	4.439e-04	1.000e-20
X23_P4	6.041e-04	1.000e-20
X46_P4	1.183e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	3.038e-05	8.438e-05	1.082e-04	1.549e-04
B (output stable)	4.025e-05	1.542e-04	1.654e-04	2.551e-04
C (output stable)	3.260e-04	8.255e-04	9.584e-04	1.305e-03
A to Z	2.881e-03	6.029e-03	8.558e-03	1.150e-02
B to Z	2.606e-03	5.310e-03	7.476e-03	1.005e-02
C to Z	2.318e-03	4.604e-03	6.514e-03	9.233e-03
	X46_P4			
A (output stable)	2.790e-04			
B (output stable)	4.446e-04			
C (output stable)	2.176e-03			
A to Z	2.195e-02			
B to Z	1.918e-02			
C to Z	1.788e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

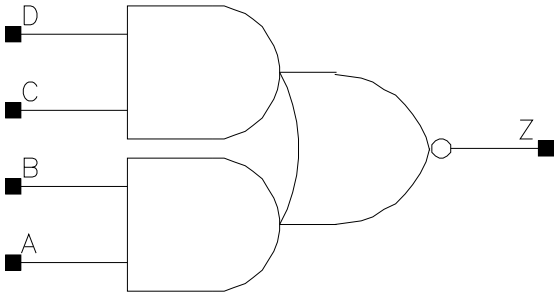
	X46_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P4	X10_P4	X16_P4	X21_P4
A	0.0008	0.0020	0.0029	0.0037
B	0.0008	0.0018	0.0027	0.0036
C	0.0007	0.0019	0.0027	0.0036
D	0.0008	0.0017	0.0025	0.0034
	X42_P4			
A	0.0075			
B	0.0071			
C	0.0072			
D	0.0069			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X10_P4**	**X4_P4**	**X10_P4**
A to Z ↓	0.0088	0.0091	3.0860	1.2221
A to Z ↑	0.0154	0.0128	4.9598	1.6591
B to Z ↓	0.0103	0.0107	3.1221	1.2371
B to Z ↑	0.0134	0.0113	4.9432	1.7064
C to Z ↓	0.0059	0.0060	3.1653	1.2319
C to Z ↑	0.0141	0.0121	4.9641	1.6741
D to Z ↓	0.0070	0.0072	3.2105	1.2503
D to Z ↑	0.0120	0.0103	4.9476	1.7038
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0099	0.0098	0.8781	0.6625
A to Z ↑	0.0133	0.0133	1.1213	0.8716
B to Z ↓	0.0116	0.0112	0.8881	0.6698
B to Z ↑	0.0111	0.0111	1.1221	0.8738
C to Z ↓	0.0065	0.0066	0.8795	0.6644
C to Z ↑	0.0125	0.0128	1.1250	0.8731
D to Z ↓	0.0078	0.0075	0.8918	0.6733
D to Z ↑	0.0101	0.0103	1.1268	0.8747
	X42_P4		**X42_P4**	
A to Z ↓	0.0105		0.3446	
A to Z ↑	0.0136		0.4384	
B to Z ↓	0.0117		0.3484	
B to Z ↑	0.0111		0.4365	
C to Z ↓	0.0072		0.3418	
C to Z ↑	0.0130		0.4403	
D to Z ↓	0.0082		0.3465	
D to Z ↑	0.0105		0.4387	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	1.098e-04	1.000e-20
X10_P4	3.686e-04	1.000e-20
X16_P4	5.254e-04	1.000e-20
X21_P4	7.004e-04	1.000e-20
X42_P4	1.377e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	3.381e-05	7.995e-05	1.537e-04	2.089e-04
B (output stable)	4.566e-05	1.134e-04	2.790e-04	4.078e-04
C (output stable)	8.757e-05	1.960e-04	3.338e-04	4.268e-04
D (output stable)	1.027e-04	2.353e-04	4.630e-04	6.206e-04
A to Z	2.592e-03	6.738e-03	1.022e-02	1.327e-02
B to Z	2.349e-03	6.102e-03	9.082e-03	1.185e-02
C to Z	1.948e-03	5.240e-03	7.872e-03	1.041e-02
D to Z	1.731e-03	4.650e-03	6.821e-03	9.047e-03
	X42_P4			
A (output stable)	3.965e-04			
B (output stable)	7.265e-04			
C (output stable)	8.086e-04			
D (output stable)	1.147e-03			

A to Z	2.628e-02			
B to Z	2.337e-02			
C to Z	2.057e-02			
D to Z	1.791e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

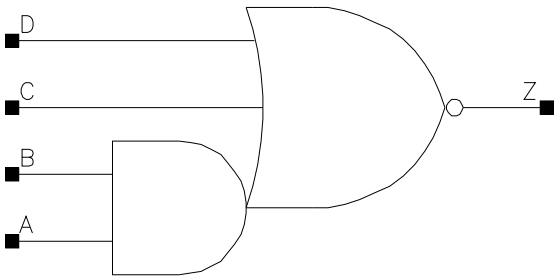
Pin Cycle (vdds)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X35_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P4	X35_P4
A	0.0009	0.0069
B	0.0009	0.0063
C	0.0009	0.0066
D	0.0009	0.0062

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X35_P4	X5_P4	X35_P4
A to Z ↓	0.0071	0.0075	2.6187	0.3870
A to Z ↑	0.0163	0.0153	5.2497	0.6822
B to Z ↓	0.0081	0.0085	2.6531	0.3932
B to Z ↑	0.0137	0.0123	5.2021	0.6810
C to Z ↓	0.0084	0.0123	1.6940	0.3227
C to Z ↑	0.0151	0.0140	4.9479	0.6456
D to Z ↓	0.0079	0.0111	1.7079	0.3227

D to Z ↑	0.0157	0.0141	4.9621	0.6484

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.263e-04	1.000e-20
X35_P4	9.468e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X35_P4
A (output stable)	1.253e-04	9.987e-04
B (output stable)	1.269e-04	1.075e-03
C (output stable)	6.288e-05	6.536e-04
D (output stable)	8.824e-05	9.677e-04
A to Z	2.526e-03	1.841e-02
B to Z	2.247e-03	1.590e-02
C to Z	3.408e-03	2.494e-02
D to Z	3.020e-03	2.132e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

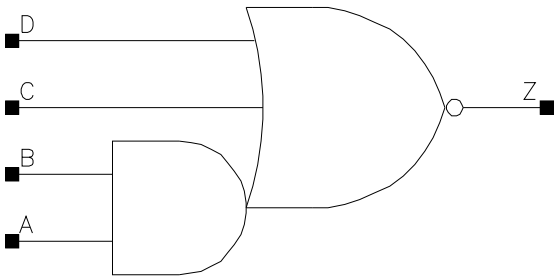
Pin Cycle (vdds)	X5_P4	X35_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X17_P4	1.200	2.448	2.9376
X34_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P4	X17_P4	X34_P4
A	0.0009	0.0037	0.0074
B	0.0009	0.0035	0.0071
C	0.0008	0.0032	0.0062
D	0.0008	0.0030	0.0059

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X17_P4	X4_P4	X17_P4
A to Z ↓	0.0091	0.0100	2.8233	0.7450
A to Z ↑	0.0147	0.0153	5.2974	1.3128
B to Z ↓	0.0108	0.0113	2.8576	0.7530
B to Z ↑	0.0126	0.0125	5.2318	1.3154
C to Z ↓	0.0092	0.0091	2.6522	0.6437
C to Z ↑	0.0116	0.0117	5.0061	1.2498

D to Z ↓	0.0074	0.0066	2.7084	0.6481
D to Z ↑	0.0118	0.0111	5.0251	1.2523
	X34_P4		**X34_P4**	
A to Z ↓	0.0098		0.3822	
A to Z ↑	0.0150		0.6726	
B to Z ↓	0.0114		0.3866	
B to Z ↑	0.0123		0.6696	
C to Z ↓	0.0096		0.3436	
C to Z ↑	0.0113		0.6389	
D to Z ↓	0.0071		0.3470	
D to Z ↑	0.0108		0.6404	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	1.230e-04	1.000e-20
X17_P4	4.913e-04	1.000e-20
X34_P4	9.654e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X17_P4	X34_P4
A (output stable)	2.814e-05	1.356e-04	2.676e-04
B (output stable)	3.136e-05	1.831e-04	3.456e-04
C (output stable)	9.354e-05	4.738e-04	9.250e-04
D (output stable)	1.735e-04	1.128e-03	2.064e-03
A to Z	3.083e-03	1.290e-02	2.504e-02
B to Z	2.819e-03	1.144e-02	2.229e-02
C to Z	2.272e-03	9.470e-03	1.806e-02
D to Z	1.954e-03	7.741e-03	1.473e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

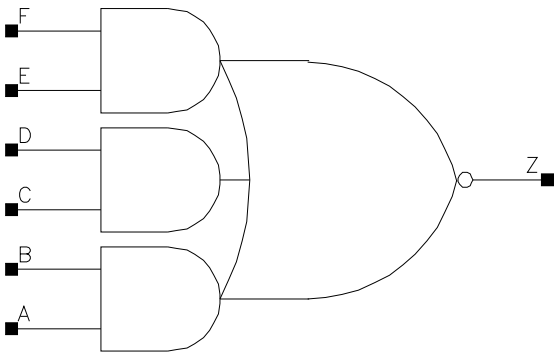
Pin Cycle (vdds)	X4_P4	X17_P4	X34_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X8_P4	1.200	2.176	2.6112
X13_P4	1.200	2.720	3.2640
X17_P4	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P4	X8_P4	X13_P4	X17_P4
A	0.0009	0.0018	0.0028	0.0037

B	0.0009	0.0017	0.0026	0.0034
C	0.0009	0.0018	0.0026	0.0034
D	0.0009	0.0017	0.0025	0.0032
E	0.0011	0.0017	0.0026	0.0033
F	0.0009	0.0016	0.0024	0.0032

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0114	0.0142	2.5025	1.4421
A to Z ↑	0.0219	0.0216	5.0891	2.3747
B to Z ↓	0.0134	0.0158	2.5316	1.4534
B to Z ↑	0.0197	0.0192	5.0810	2.3817
C to Z ↓	0.0101	0.0124	2.4877	1.4568
C to Z ↑	0.0201	0.0202	5.1228	2.3879
D to Z ↓	0.0117	0.0142	2.5230	1.4728
D to Z ↑	0.0178	0.0176	5.0906	2.3880
E to Z ↓	0.0071	0.0089	2.4709	1.4621
E to Z ↑	0.0179	0.0175	5.0640	2.3718
F to Z ↓	0.0081	0.0101	2.5155	1.4840
F to Z ↑	0.0156	0.0148	5.1068	2.3760
	X13_P4	X17_P4	X13_P4	X17_P4
A to Z ↓	0.0135	0.0137	0.9794	0.7471
A to Z ↑	0.0198	0.0200	1.5663	1.2053
B to Z ↓	0.0155	0.0154	0.9874	0.7532
B to Z ↑	0.0177	0.0175	1.5729	1.2058
C to Z ↓	0.0118	0.0118	0.9841	0.7415
C to Z ↑	0.0184	0.0187	1.5775	1.2155
D to Z ↓	0.0137	0.0134	0.9946	0.7490
D to Z ↑	0.0161	0.0162	1.5806	1.2129
E to Z ↓	0.0084	0.0084	0.9834	0.7443
E to Z ↑	0.0163	0.0164	1.5718	1.2049
F to Z ↓	0.0097	0.0094	0.9972	0.7544
F to Z ↑	0.0138	0.0139	1.5754	1.2112

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	1.924e-04	1.000e-20
X8_P4	4.106e-04	1.000e-20
X13_P4	5.925e-04	1.000e-20
X17_P4	7.877e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	5.413e-05	1.272e-04	1.752e-04	2.378e-04
B (output stable)	6.226e-05	2.056e-04	2.401e-04	3.692e-04
C (output stable)	9.123e-05	1.941e-04	2.587e-04	3.459e-04
D (output stable)	1.012e-04	2.876e-04	3.322e-04	4.753e-04
E (output stable)	1.908e-04	4.641e-04	6.002e-04	8.142e-04
F (output stable)	2.207e-04	5.537e-04	6.784e-04	9.394e-04

A to Z	4.465e-03	9.309e-03	1.307e-02	1.731e-02
B to Z	4.143e-03	8.549e-03	1.205e-02	1.580e-02
C to Z	3.581e-03	7.671e-03	1.057e-02	1.403e-02
D to Z	3.293e-03	6.948e-03	9.606e-03	1.268e-02
E to Z	2.815e-03	6.011e-03	8.304e-03	1.098e-02
F to Z	2.540e-03	5.278e-03	7.332e-03	9.659e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

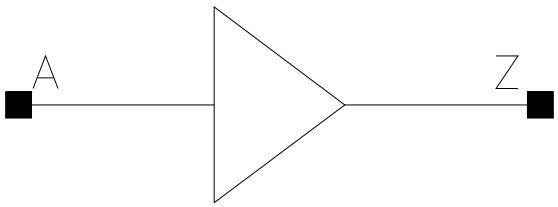
Pin Cycle (vdds)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.408	0.4896
X6_P4	1.200	0.408	0.4896
X8_P4	1.200	0.408	0.4896
X13_P4	1.200	0.544	0.6528
X16_P4	1.200	0.544	0.6528
X21_P4	1.200	0.680	0.8160
X25_P4	1.200	0.680	0.8160
X29_P4	1.200	0.952	1.1424
X33_P4	1.200	0.952	1.1424
X42_P4	1.200	1.088	1.3056
X50_P4	1.200	1.224	1.4688
X58_P4	1.200	1.496	1.7952
X67_P4	1.200	1.632	1.9584
X75_P4	1.200	1.768	2.1216
X84_P4	1.200	1.904	2.2848
X100_P4	1.200	2.312	2.7744
X134_P4	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0008	0.0009	0.0009	0.0009
	X16_P4	X21_P4	X25_P4	X29_P4
A	0.0009	0.0012	0.0012	0.0016
	X33_P4	X42_P4	X50_P4	X58_P4
A	0.0016	0.0019	0.0022	0.0033

	X67_P4	X75_P4	X84_P4	X100_P4
A	0.0033	0.0033	0.0032	0.0043
	X134_P4			
A	0.0054			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0162	0.0165	2.7541	2.0255
A to Z ↑	0.0129	0.0129	3.6686	2.7414
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0173	0.0195	1.5088	0.9665
A to Z ↑	0.0136	0.0158	1.9852	1.2852
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0211	0.0176	0.7699	0.5951
A to Z ↑	0.0169	0.0147	0.9957	0.7777
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0188	0.0178	0.5112	0.4299
A to Z ↑	0.0156	0.0139	0.6568	0.5562
	X33_P4	**X42_P4**	**X33_P4**	**X42_P4**
A to Z ↓	0.0188	0.0183	0.3821	0.3103
A to Z ↑	0.0147	0.0152	0.4911	0.3955
	X50_P4	**X58_P4**	**X50_P4**	**X58_P4**
A to Z ↓	0.0178	0.0167	0.2575	0.2220
A to Z ↑	0.0149	0.0140	0.3281	0.2824
	X67_P4	**X75_P4**	**X67_P4**	**X75_P4**
A to Z ↓	0.0175	0.0187	0.1947	0.1753
A to Z ↑	0.0147	0.0157	0.2474	0.2215
	X84_P4	**X100_P4**	**X84_P4**	**X100_P4**
A to Z ↓	0.0195	0.0181	0.1584	0.1331
A to Z ↑	0.0164	0.0154	0.1999	0.1676
	X134_P4		**X134_P4**	
A to Z ↓	0.0193		0.1030	
A to Z ↑	0.0166		0.1282	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	1.004e-04	1.000e-20
X6_P4	1.293e-04	1.000e-20
X8_P4	1.712e-04	1.000e-20
X13_P4	2.203e-04	1.000e-20
X16_P4	2.938e-04	1.000e-20
X21_P4	4.137e-04	1.000e-20
X25_P4	4.793e-04	1.000e-20
X29_P4	5.369e-04	1.000e-20
X33_P4	5.948e-04	1.000e-20
X42_P4	7.604e-04	1.000e-20
X50_P4	9.269e-04	1.000e-20
X58_P4	1.151e-03	1.000e-20
X67_P4	1.263e-03	1.000e-20
X75_P4	1.375e-03	1.000e-20

X84_P4	1.487e-03	1.000e-20
X100_P4	1.823e-03	1.000e-20
X134_P4	2.383e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	2.879e-03	3.245e-03	3.884e-03	5.370e-03
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	6.699e-03	8.738e-03	1.011e-02	1.146e-02
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	1.286e-02	1.610e-02	1.898e-02	2.294e-02
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	2.571e-02	2.902e-02	3.227e-02	3.822e-02
	X134_P4			
A to Z	5.353e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

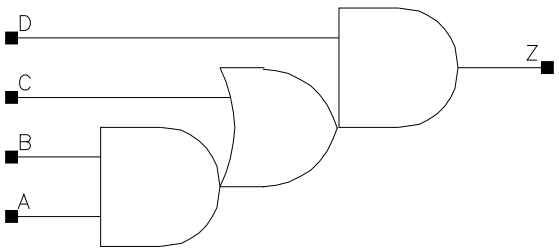
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P4			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.632	1.9584
X25_P4	1.200	1.768	2.1216
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0011	0.0023	0.0023	0.0022
B	0.0011	0.0020	0.0020	0.0020
C	0.0011	0.0025	0.0025	0.0025
D	0.0016	0.0021	0.0021	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0204	0.0192	1.5364	0.7610
A to Z ↑	0.0215	0.0204	2.0200	0.9853
B to Z ↓	0.0186	0.0174	1.5317	0.7606
B to Z ↑	0.0224	0.0211	2.0205	0.9846
C to Z ↓	0.0189	0.0177	1.5295	0.7580
C to Z ↑	0.0163	0.0152	1.9995	0.9749

D to Z ↓	0.0185	0.0165	1.5187	0.7533
D to Z ↑	0.0178	0.0157	2.0048	0.9777
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0213	0.0228	0.5150	0.3871
A to Z ↑	0.0225	0.0240	0.6681	0.5020
B to Z ↓	0.0195	0.0215	0.5151	0.3868
B to Z ↑	0.0233	0.0252	0.6674	0.5005
C to Z ↓	0.0199	0.0217	0.5134	0.3855
C to Z ↑	0.0170	0.0185	0.6596	0.4949
D to Z ↓	0.0179	0.0190	0.5090	0.3813
D to Z ↑	0.0174	0.0187	0.6614	0.4961

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	2.998e-04	1.000e-20
X17_P4	5.974e-04	1.000e-20
X25_P4	7.361e-04	1.000e-20
X33_P4	8.748e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	7.127e-05	1.482e-04	1.489e-04	1.321e-04
B (output stable)	9.129e-05	1.907e-04	1.918e-04	1.688e-04
C (output stable)	2.822e-04	4.573e-04	4.539e-04	4.409e-04
D (output stable)	1.291e-04	1.963e-04	1.985e-04	1.946e-04
A to Z	5.951e-03	1.121e-02	1.444e-02	1.792e-02
B to Z	5.642e-03	1.046e-02	1.368e-02	1.729e-02
C to Z	5.098e-03	9.363e-03	1.229e-02	1.545e-02
D to Z	6.081e-03	1.120e-02	1.394e-02	1.681e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

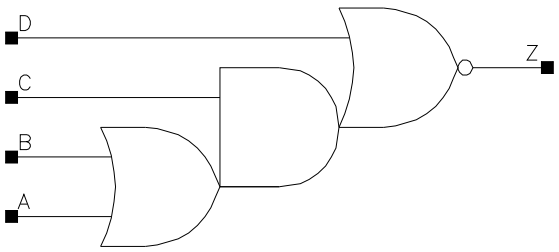
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.952	1.1424
X11_P4	1.200	1.496	1.7952
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X16_P4	X21_P4
A	0.0010	0.0018	0.0028	0.0037
B	0.0010	0.0018	0.0028	0.0036
C	0.0009	0.0018	0.0027	0.0037
D	0.0012	0.0019	0.0027	0.0037

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0095	0.0090	2.4790	1.3025
A to Z ↑	0.0181	0.0168	5.2016	2.7386
B to Z ↓	0.0088	0.0085	2.4172	1.2789
B to Z ↑	0.0182	0.0174	5.2128	2.7441
C to Z ↓	0.0096	0.0092	2.3053	1.2128
C to Z ↑	0.0114	0.0103	3.6070	1.8642

D to Z ↓	0.0046	0.0036	1.5978	0.8071
D to Z ↑	0.0126	0.0114	3.8320	1.9871
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0089	0.0092	0.8715	0.6741
A to Z ↑	0.0154	0.0163	1.7405	1.3569
B to Z ↓	0.0081	0.0085	0.8785	0.6764
B to Z ↑	0.0160	0.0166	1.7448	1.3595
C to Z ↓	0.0093	0.0095	0.8277	0.6365
C to Z ↑	0.0096	0.0098	1.2305	0.9250
D to Z ↓	0.0037	0.0038	0.5590	0.4260
D to Z ↑	0.0105	0.0104	1.2977	0.9859

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.679e-04	1.000e-20
X11_P4	3.237e-04	1.000e-20
X16_P4	4.681e-04	1.000e-20
X21_P4	6.178e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	3.366e-05	6.126e-05	8.181e-05	1.302e-04
B (output stable)	4.715e-05	8.070e-05	1.063e-04	1.806e-04
C (output stable)	1.030e-04	2.067e-04	2.805e-04	3.947e-04
D (output stable)	4.299e-04	8.945e-04	1.269e-03	1.799e-03
A to Z	3.770e-03	6.806e-03	9.666e-03	1.323e-02
B to Z	3.240e-03	5.898e-03	8.587e-03	1.145e-02
C to Z	3.064e-03	5.548e-03	7.971e-03	1.080e-02
D to Z	2.534e-03	4.681e-03	6.659e-03	8.822e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

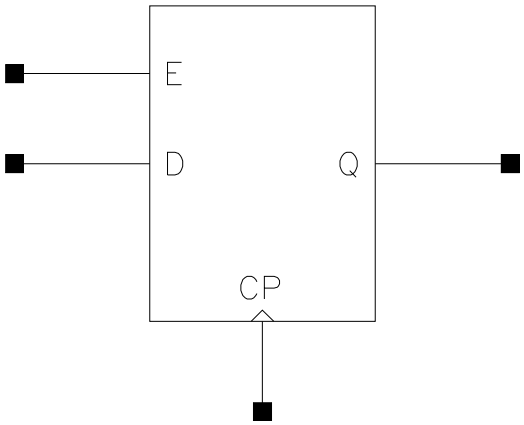
Pin Cycle (vdds)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.128	3.7536
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0012	0.0012	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0258	0.0297	1.5106	0.7758
CP to Q ↑	0.0328	0.0356	2.0311	1.0180
	X33_P4		**X33_P4**	
CP to Q ↓	0.0453		0.3869	
CP to Q ↑	0.0557		0.5047	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0339	0.0339	0.0339
CP ↑	min_pulse_width to CP	0.0224	0.0237	0.0189
D ↓	hold_rising to CP	-0.0017	-0.0017	-0.0017
D ↑	hold_rising to CP	0.0058	0.0058	0.0058
D ↓	setup_rising to CP	0.0295	0.0295	0.0295
D ↑	setup_rising to CP	0.0223	0.0223	0.0223
E ↓	hold_rising to CP	0.0010	0.0010	0.0010
E ↑	hold_rising to CP	0.0058	0.0058	0.0058
E ↓	setup_rising to CP	0.0360	0.0360	0.0360
E ↑	setup_rising to CP	0.0315	0.0315	0.0315

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	6.071e-04	1.000e-20
X17_P4	7.220e-04	1.000e-20
X33_P4	1.098e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

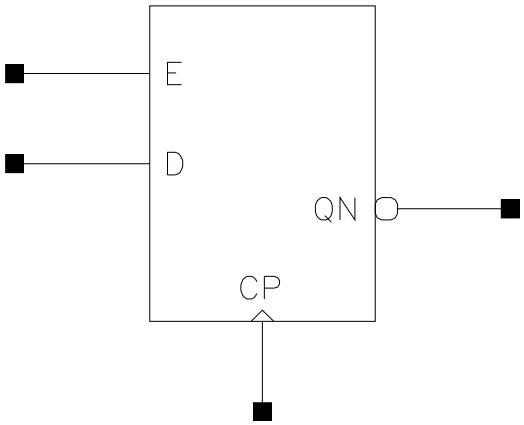
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.188e-02	1.188e-02	1.189e-02
Clock 100Mhz Data 25Mhz	1.555e-02	1.732e-02	2.105e-02
Clock 100Mhz Data 50Mhz	1.922e-02	2.276e-02	3.020e-02
Clock = 0 Data 100Mhz	7.479e-03	7.478e-03	7.478e-03
Clock = 1 Data 100Mhz	2.274e-03	2.275e-03	2.274e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.264	3.9168
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0012	0.0012	0.0009

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0447	0.0427	1.5606	0.7487
CP to QN ↑	0.0351	0.0356	2.0608	0.9866
	X33_P4		**X33_P4**	
CP to QN ↓	0.0462		0.3878	
CP to QN ↑	0.0394		0.5060	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0339	0.0339	0.0339
CP ↑	min_pulse_width to CP	0.0189	0.0224	0.0237
D ↓	hold_rising to CP	-0.0017	-0.0017	-0.0017
D ↑	hold_rising to CP	0.0058	0.0058	0.0058
D ↓	setup_rising to CP	0.0295	0.0295	0.0295
D ↑	setup_rising to CP	0.0223	0.0223	0.0223
E ↓	hold_rising to CP	0.0010	0.0010	0.0010
E ↑	hold_rising to CP	0.0058	0.0058	0.0058
E ↓	setup_rising to CP	0.0360	0.0360	0.0360
E ↑	setup_rising to CP	0.0315	0.0315	0.0315

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	6.027e-04	1.000e-20
X17_P4	8.053e-04	1.000e-20
X33_P4	1.070e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

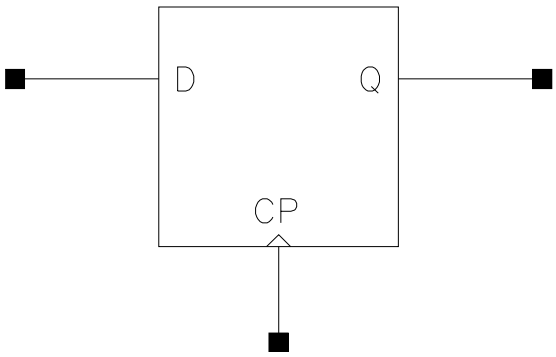
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.187e-02	1.188e-02	1.188e-02
Clock 100Mhz Data 25Mhz	1.550e-02	1.737e-02	2.111e-02
Clock 100Mhz Data 50Mhz	1.913e-02	2.286e-02	3.035e-02
Clock = 0 Data 100Mhz	7.478e-03	7.478e-03	7.478e-03
Clock = 1 Data 100Mhz	2.274e-03	2.274e-03	2.274e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.176	2.6112
X17_P4	1.200	2.448	2.9376
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0270	0.0300	1.5019	0.7686
CP to Q ↑	0.0329	0.0370	1.9608	0.9955
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to Q ↓	0.0379	0.0393	0.4483	0.4071
CP to Q ↑	0.0424	0.0436	0.5577	0.5100

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0305	0.0339	0.0339	0.0339
CP ↑	min_pulse_width to CP	0.0224	0.0236	0.0318	0.0330
D ↓	hold_rising to CP	0.0146	0.0151	0.0151	0.0151
D ↑	hold_rising to CP	0.0145	0.0119	0.0145	0.0119
D ↓	setup_rising to CP	0.0149	0.0149	0.0149	0.0149
D ↑	setup_rising to CP	0.0129	0.0129	0.0129	0.0129

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	4.655e-04	1.000e-20
X17_P4	5.952e-04	1.000e-20
X30_P4	7.846e-04	1.000e-20
X33_P4	8.214e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

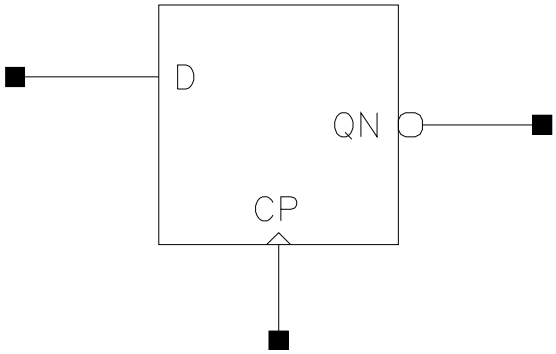
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.228e-02	1.232e-02	1.233e-02	1.234e-02
Clock 100Mhz Data 25Mhz	1.422e-02	1.637e-02	2.060e-02	2.163e-02
Clock 100Mhz Data 50Mhz	1.616e-02	2.041e-02	2.887e-02	3.093e-02
Clock = 0 Data 100Mhz	5.020e-03	5.148e-03	5.188e-03	5.207e-03
Clock = 1 Data 100Mhz	2.714e-05	2.718e-05	2.700e-05	2.733e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0264	0.0306	1.5480	0.7900
CP to QN ↑	0.0272	0.0294	1.9569	0.9975
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to QN ↓	0.0454	0.0459	0.4254	0.3869
CP to QN ↑	0.0370	0.0421	0.5401	0.5053

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0292	0.0292	0.0305	0.0305
CP ↑	min_pulse_width to CP	0.0224	0.0236	0.0224	0.0237
D ↓	hold_rising to CP	0.0146	0.0173	0.0151	0.0146
D ↑	hold_rising to CP	0.0177	0.0177	0.0119	0.0145
D ↓	setup_rising to CP	0.0121	0.0117	0.0149	0.0149
D ↑	setup_rising to CP	0.0124	0.0124	0.0129	0.0129

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	4.401e-04	1.000e-20
X17_P4	5.562e-04	1.000e-20
X30_P4	8.849e-04	1.000e-20
X33_P4	9.298e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

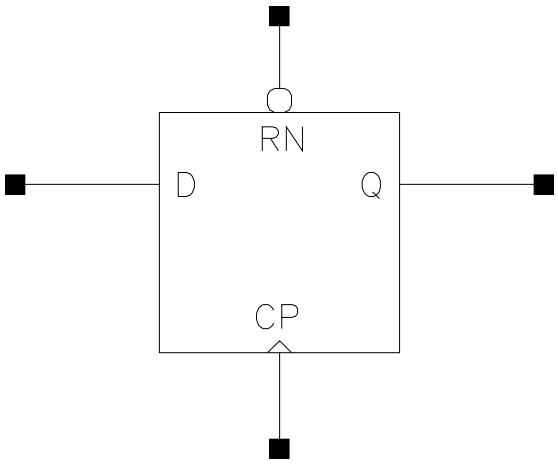
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.194e-02	1.195e-02	1.208e-02	1.214e-02
Clock 100Mhz Data 25Mhz	1.372e-02	1.557e-02	1.851e-02	1.982e-02
Clock 100Mhz Data 50Mhz	1.550e-02	1.920e-02	2.495e-02	2.750e-02
Clock = 0 Data 100Mhz	4.533e-03	4.533e-03	4.779e-03	4.841e-03
Clock = 1 Data 100Mhz	2.723e-05	2.714e-05	2.739e-05	2.736e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0008	0.0008
RN	0.0010	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0312	0.0390	0.7749	0.4547
CP to Q ↑	0.0381	0.0434	0.9999	0.5609
RN to Q ↓	0.0409	0.0458	0.7598	0.4433

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0340	0.0340
CP ↑	min_pulse_width to CP	0.0271	0.0318
D ↓	hold_rising to CP	0.0151	0.0151
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0143	0.0170
D ↑	setup_rising to CP	0.0120	0.0120
RN ↓	min_pulse_width to RN	0.0615	0.0762
RN ↑	recovery_rising to CP	0.0081	0.0081
RN ↑	removal_rising to CP	-0.0007	-0.0007

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P4	6.824e-04	1.000e-20
X30_P4	9.083e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

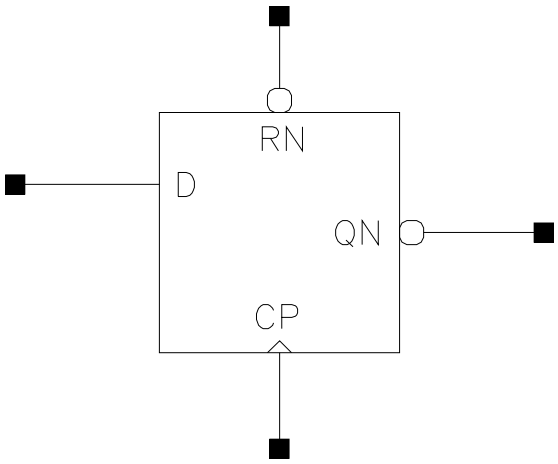
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	1.293e-02	1.292e-02
Clock 100Mhz Data 25Mhz	1.721e-02	2.141e-02
Clock 100Mhz Data 50Mhz	2.150e-02	2.989e-02
Clock = 0 Data 100Mhz	5.955e-03	5.959e-03
Clock = 1 Data 100Mhz	2.789e-05	2.723e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0008	0.0008
RN	0.0010	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0436	0.0472	0.7450	0.4270
CP to QN ↑	0.0354	0.0386	0.9771	0.5432
RN to QN ↑	0.0466	0.0496	0.9752	0.5426

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0340	0.0340
CP ↑	min_pulse_width to CP	0.0224	0.0224
D ↓	hold_rising to CP	0.0151	0.0151
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0170	0.0170
D ↑	setup_rising to CP	0.0120	0.0120
RN ↓	min_pulse_width to RN	0.0496	0.0518
RN ↑	recovery_rising to CP	0.0081	0.0081
RN ↑	removal_rising to CP	-0.0007	-0.0007

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P4	7.234e-04	1.000e-20
X30_P4	8.718e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

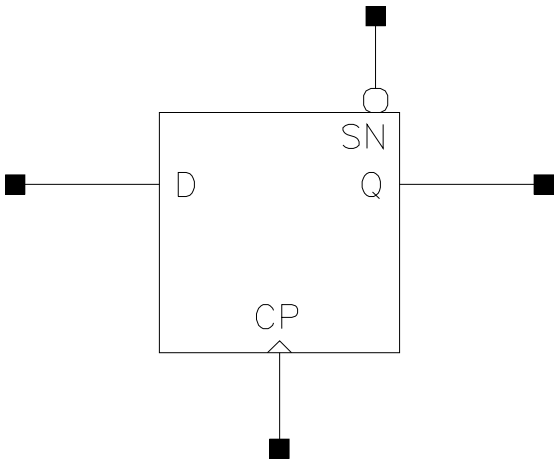
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	1.293e-02	1.293e-02
Clock 100Mhz Data 25Mhz	1.719e-02	1.972e-02
Clock 100Mhz Data 50Mhz	2.145e-02	2.650e-02
Clock = 0 Data 100Mhz	6.025e-03	6.007e-03
Clock = 1 Data 100Mhz	2.764e-05	2.801e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0008	0.0008
SN	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0312	0.0396	0.7752	0.4525
CP to Q ↑	0.0377	0.0434	0.9999	0.5601
SN to Q ↑	0.0304	0.0338	0.9877	0.5508

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0340	0.0340
CP ↑	min_pulse_width to CP	0.0271	0.0330
D ↓	hold_rising to CP	0.0156	0.0156
D ↑	hold_rising to CP	0.0119	0.0119
D ↓	setup_rising to CP	0.0198	0.0198
D ↑	setup_rising to CP	0.0124	0.0124
SN ↓	min_pulse_width to SN	0.0381	0.0479
SN ↑	recovery_rising to CP	0.0006	0.0006
SN ↑	removal_rising to CP	0.0189	0.0189

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P4	6.132e-04	1.000e-20
X30_P4	7.651e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

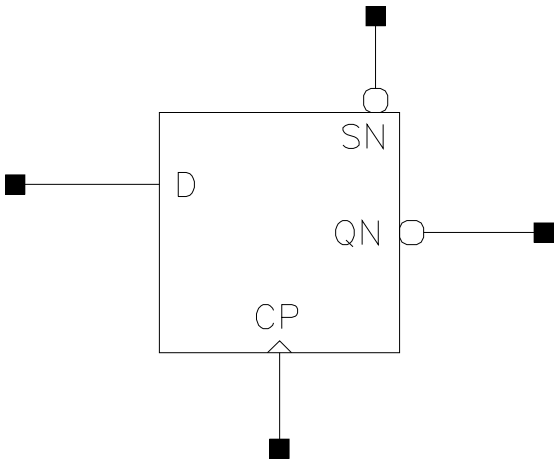
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	1.307e-02	1.304e-02
Clock 100Mhz Data 25Mhz	1.735e-02	2.155e-02
Clock 100Mhz Data 50Mhz	2.162e-02	3.006e-02
Clock = 0 Data 100Mhz	5.867e-03	5.866e-03
Clock = 1 Data 100Mhz	2.805e-05	2.709e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0010	0.0010
D	0.0008	0.0008
SN	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0431	0.0468	0.7464	0.4277
CP to QN ↑	0.0356	0.0387	0.9748	0.5418
SN to QN ↓	0.0365	0.0400	0.7465	0.4275

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0340	0.0340
CP ↑	min_pulse_width to CP	0.0224	0.0224
D ↓	hold_rising to CP	0.0156	0.0156
D ↑	hold_rising to CP	0.0119	0.0119
D ↓	setup_rising to CP	0.0198	0.0198
D ↑	setup_rising to CP	0.0124	0.0124
SN ↓	min_pulse_width to SN	0.0332	0.0332
SN ↑	recovery_rising to CP	-0.0027	0.0006
SN ↑	removal_rising to CP	0.0189	0.0189

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P4	7.822e-04	1.000e-20
X30_P4	1.003e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

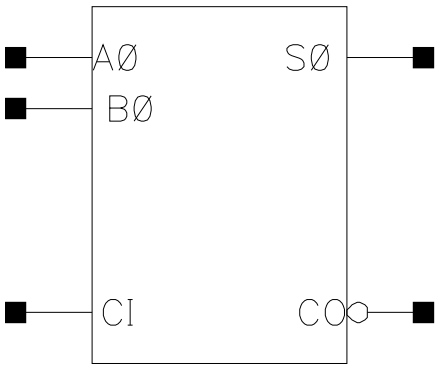
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	1.307e-02	1.306e-02
Clock 100Mhz Data 25Mhz	1.728e-02	1.980e-02
Clock 100Mhz Data 50Mhz	2.149e-02	2.654e-02
Clock = 0 Data 100Mhz	5.868e-03	5.868e-03
Clock = 1 Data 100Mhz	2.805e-05	2.822e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_P4	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_-P4	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_-P4	1.200	3.672	4.4064
C12T28SOI_LLS1_-FA1X33_P4	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4
A0	0.0035	0.0070	0.0031	0.0060
B0	0.0032	0.0068	0.0033	0.0059
CI	0.0023	0.0050	0.0024	0.0042

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4
A0 to CO ↓	0.0275	0.0305	1.5688	0.4080
A0 to CO ↑	0.0225	0.0241	2.0229	0.5200
A0 to S0 ↓	0.0296	0.0379	1.5551	0.3989
A0 to S0 ↑	0.0305	0.0381	2.0023	0.5146
B0 to CO ↓	0.0276	0.0313	1.5725	0.4095
B0 to CO ↑	0.0234	0.0255	2.0238	0.5180
B0 to S0 ↓	0.0303	0.0390	1.5561	0.3989
B0 to S0 ↑	0.0311	0.0392	2.0038	0.5144
CI to CO ↓	0.0279	0.0319	1.5726	0.4075
CI to CO ↑	0.0237	0.0253	2.0209	0.5195
CI to S0 ↓	0.0304	0.0390	1.5571	0.3992
CI to S0 ↑	0.0316	0.0399	2.0030	0.5143
	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4
A0 to CO ↓	0.0188	0.0234	2.8850	0.4948
A0 to CO ↑	0.0177	0.0203	2.0660	0.5084
A0 to S0 ↓	0.0401	0.0498	1.6848	0.4174
A0 to S0 ↑	0.0370	0.0402	2.0768	0.5234
B0 to CO ↓	0.0200	0.0248	2.8859	0.4955
B0 to CO ↑	0.0160	0.0191	2.0636	0.5087
B0 to S0 ↓	0.0403	0.0511	1.6851	0.4173
B0 to S0 ↑	0.0372	0.0413	2.0773	0.5236
CI to CO ↓	0.0201	0.0356	2.8804	0.4993
CI to CO ↑	0.0172	0.0212	2.1235	0.5123
CI to S0 ↓	0.0239	0.0311	1.6856	0.4178
CI to S0 ↑	0.0199	0.0204	2.0778	0.5236

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_FA1X8_P4	6.366e-04	1.000e-20
C12T28SOI_LL_FA1X33_P4	1.733e-03	1.000e-20
C12T28SOI_LLS1_FA1X8_P4	1.413e-03	1.000e-20
C12T28SOI_LLS1_FA1X33_P4	2.920e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4
A0 to CO	6.146e-03	1.972e-02	9.053e-03	2.377e-02
A0 to S0	6.172e-03	2.027e-02	1.204e-02	2.898e-02
B0 to CO	6.214e-03	2.018e-02	9.128e-03	2.402e-02
B0 to S0	6.149e-03	2.036e-02	1.224e-02	2.948e-02
CI to CO	6.335e-03	2.052e-02	6.691e-03	2.236e-02
CI to S0	6.142e-03	2.038e-02	7.657e-03	2.393e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P4	C12T28SOI_LL_-FA1X33_P4	C12T28SOI_LLS1_-FA1X8_P4	C12T28SOI_LLS1_-FA1X33_P4
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00

A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X33_P4	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X33_P4
A0	0.0012	0.0035
B0	0.0010	0.0030

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
A0 to CO ↓	0.0223	0.0208	1.5577	0.3875
A0 to CO ↑	0.0206	0.0195	1.9967	0.5161
A0 to S0 ↓	0.0280	0.0269	1.5296	0.3868
A0 to S0 ↑	0.0276	0.0325	1.9708	0.5083
B0 to CO ↓	0.0216	0.0190	1.5571	0.3843
B0 to CO ↑	0.0229	0.0213	1.9954	0.5158
B0 to S0 ↓	0.0299	0.0281	1.5289	0.3865
B0 to S0 ↑	0.0270	0.0311	1.9717	0.5084

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	4.047e-04	1.000e-20
X33_P4	1.756e-03	1.000e-20

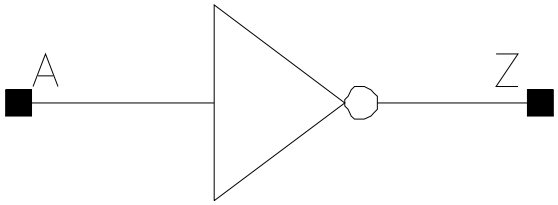
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X33_P4
A0 to CO	4.737e-03	1.667e-02
A0 to S0	4.542e-03	1.691e-02
B0 to CO	4.817e-03	1.710e-02
B0 to S0	4.498e-03	1.660e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X8_P4	X33_P4
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.272	0.3264
X6_P4	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X13_P4	1.200	0.408	0.4896
X17_P4	1.200	0.408	0.4896
X21_P4	1.200	0.544	0.6528
X25_P4	1.200	0.544	0.6528
X29_P4	1.200	0.680	0.8160
X33_P4	1.200	0.680	0.8160
X50_P4	1.200	0.952	1.1424
X58_P4	1.200	1.088	1.3056
X67_P4	1.200	1.224	1.4688
X75_P4	1.200	1.360	1.6320
X84_P4	1.200	1.496	1.7952
X100_P4	1.200	1.768	2.1216
X134_P4	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0006	0.0008	0.0010	0.0015
	X17_P4	X21_P4	X25_P4	X29_P4
A	0.0019	0.0024	0.0028	0.0034
	X33_P4	X50_P4	X58_P4	X67_P4
A	0.0037	0.0056	0.0066	0.0076
	X75_P4	X84_P4	X100_P4	X134_P4

A	0.0087	0.0098	0.0120	0.0164

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0041	0.0040	2.9413	2.2699
A to Z ↑	0.0082	0.0075	3.7975	2.9046
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0037	0.0030	1.5663	1.0092
A to Z ↑	0.0068	0.0063	2.0394	1.3315
	X17_P4	**X21_P4**	**X17_P4**	**X21_P4**
A to Z ↓	0.0031	0.0034	0.7764	0.6230
A to Z ↑	0.0059	0.0063	1.0051	0.8049
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0035	0.0032	0.5310	0.4491
A to Z ↑	0.0060	0.0059	0.6773	0.5758
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0033	0.0034	0.3989	0.2689
A to Z ↑	0.0056	0.0056	0.5077	0.3402
	X58_P4	**X67_P4**	**X58_P4**	**X67_P4**
A to Z ↓	0.0037	0.0037	0.2331	0.2048
A to Z ↑	0.0058	0.0058	0.2935	0.2574
	X75_P4	**X84_P4**	**X75_P4**	**X84_P4**
A to Z ↓	0.0042	0.0043	0.1847	0.1672
A to Z ↑	0.0062	0.0064	0.2308	0.2089
	X100_P4	**X134_P4**	**X100_P4**	**X134_P4**
A to Z ↓	0.0052	0.0060	0.1422	0.1109
A to Z ↑	0.0071	0.0079	0.1766	0.1362

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	5.143e-05	1.000e-20
X6_P4	7.454e-05	1.000e-20
X8_P4	1.192e-04	1.000e-20
X13_P4	1.710e-04	1.000e-20
X17_P4	2.455e-04	1.000e-20
X21_P4	2.910e-04	1.000e-20
X25_P4	3.583e-04	1.000e-20
X29_P4	4.113e-04	1.000e-20
X33_P4	4.702e-04	1.000e-20
X50_P4	6.939e-04	1.000e-20
X58_P4	8.058e-04	1.000e-20
X67_P4	9.177e-04	1.000e-20
X75_P4	1.030e-03	1.000e-20
X84_P4	1.141e-03	1.000e-20
X100_P4	1.365e-03	1.000e-20
X134_P4	1.813e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4

A to Z	1.345e-03	1.733e-03	2.433e-03	3.648e-03
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	4.764e-03	6.066e-03	7.099e-03	8.250e-03
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	9.226e-03	1.371e-02	1.608e-02	1.827e-02
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	2.086e-02	2.325e-02	2.862e-02	3.942e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

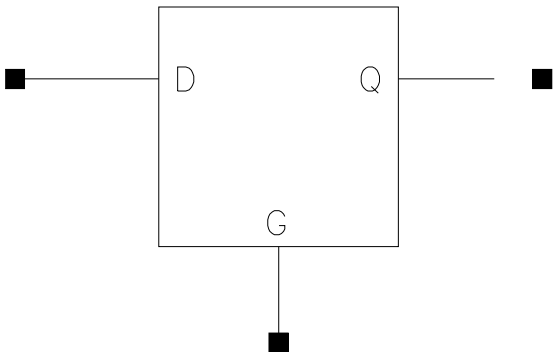
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X23_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P4	X23_P4
D	0.0006	0.0015
G	0.0012	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X23_P4	X8_P4	X23_P4
D to Q ↓	0.0315	0.0249	1.5502	0.7315
D to Q ↑	0.0220	0.0222	1.9649	0.5258
G to Q ↓	0.0330	0.0278	1.5458	0.7310
G to Q ↑	0.0218	0.0193	1.9642	0.5261

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P4	X23_P4
D ↓	hold_falling to G	0.0058	0.0106
D ↑	hold_falling to G	0.0089	0.0090
D ↓	setup_falling to G	0.0316	0.0222
D ↑	setup_falling to G	0.0231	0.0278
G ↑	min_pulse_width to G	0.0317	0.0318

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	2.668e-04	1.000e-20
X23_P4	7.237e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X23_P4
D (output stable)	1.964e-05	7.841e-05
G (output stable)	1.817e-03	3.634e-03
D to Q	8.124e-03	1.629e-02
G to Q	8.018e-03	1.542e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

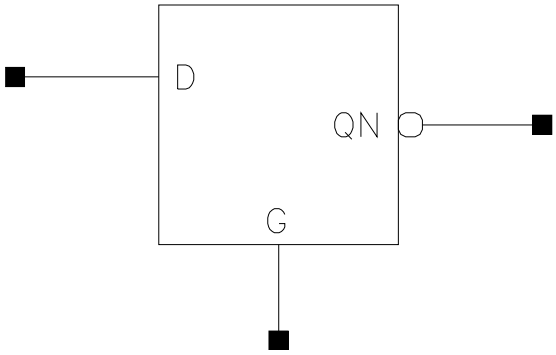
Pin Cycle (vdds)	X8_P4	X23_P4
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P4
D	0.0007
G	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P4	X17_P4
D to QN ↓	0.0283	0.7470
D to QN ↑	0.0355	0.9666
G to QN ↓	0.0277	0.7466
G to QN ↑	0.0361	0.9658

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P4
D ↓	hold_falling to G	0.0004
D ↑	hold_falling to G	0.0063
D ↓	setup_falling to G	0.0267
D ↑	setup_falling to G	0.0215
G ↑	min_pulse_width to G	0.0237

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P4	4.419e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X17_P4
D (output stable)	2.005e-05
G (output stable)	2.359e-03
D to QN	9.490e-03
G to QN	9.612e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

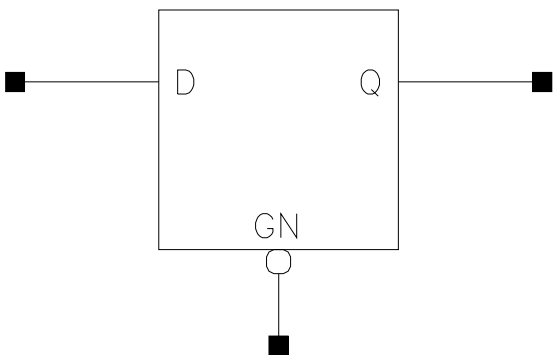
Pin Cycle (vdds)	X17_P4
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
D	0.0006	0.0009	0.0019
GN	0.0012	0.0015	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D to Q ↓	0.0319	0.0278	1.5521	0.7716
D to Q ↑	0.0224	0.0218	1.9634	1.0087
GN to Q ↓	0.0301	0.0253	1.5539	0.7721
GN to Q ↑	0.0326	0.0316	1.9636	1.0069

	X33_P4		X33_P4	
D to Q ↓	0.0273		0.3954	
D to Q ↑	0.0185		0.5073	
GN to Q ↓	0.0236		0.3957	
GN to Q ↑	0.0248		0.5063	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P4	X17_P4	X33_P4
D ↓	hold_rising to GN	0.0019	0.0046	0.0046
D ↑	hold_rising to GN	0.0132	0.0128	0.0127
D ↓	setup_rising to GN	0.0351	0.0330	0.0302
D ↑	setup_rising to GN	0.0223	0.0190	0.0169
GN ↓	min_pulse_width to GN	0.0416	0.0344	0.0318

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	2.734e-04	1.000e-20
X17_P4	4.607e-04	1.000e-20
X33_P4	8.172e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
D (output stable)	1.911e-05	3.173e-05	8.657e-05
GN (output stable)	1.800e-03	2.408e-03	3.370e-03
D to Q	8.175e-03	1.211e-02	1.995e-02
GN to Q	1.100e-02	1.548e-02	2.363e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

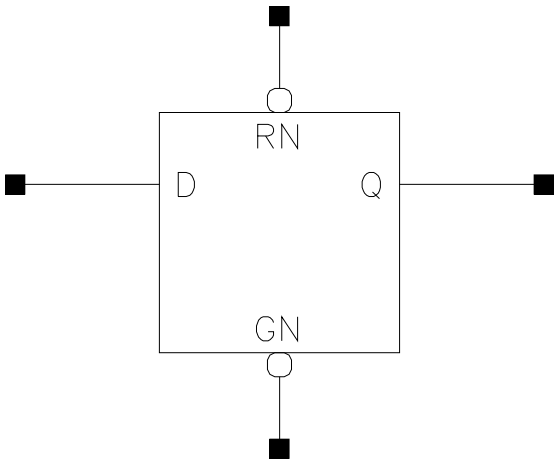
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.496	1.7952
X33_P4	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X33_P4
D	0.0006	0.0016
GN	0.0014	0.0025
RN	0.0006	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
D to Q ↓	0.0295	0.0269	1.5263	0.3966
D to Q ↑	0.0293	0.0393	2.0024	0.5220

GN to Q ↓	0.0279	0.0249	1.5282	0.3969
GN to Q ↑	0.0371	0.0402	2.0026	0.5212
RN to Q ↓	0.0253	0.0442	1.4684	0.3983
RN to Q ↑	0.0296	0.0431	2.0045	0.5220

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P4	X33_P4
D ↓	hold_rising to GN	0.0019	0.0067
D ↑	hold_rising to GN	0.0058	-0.0039
D ↓	setup_rising to GN	0.0326	0.0279
D ↑	setup_rising to GN	0.0287	0.0436
GN ↓	min_pulse_width to GN	0.0388	0.0403
RN ↓	min_pulse_width to RN	0.0305	0.0544
RN ↑	recovery_rising to GN	0.0323	0.0460
RN ↑	removal_rising to GN	-0.0168	-0.0294

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	3.275e-04	1.000e-20
X33_P4	8.781e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X33_P4
D (output stable)	6.366e-05	1.131e-04
GN (output stable)	2.016e-03	3.337e-03
RN (output stable)	5.686e-05	1.118e-04
D to Q	8.369e-03	2.450e-02
GN to Q	1.146e-02	2.913e-02
RN to Q	5.976e-03	1.956e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

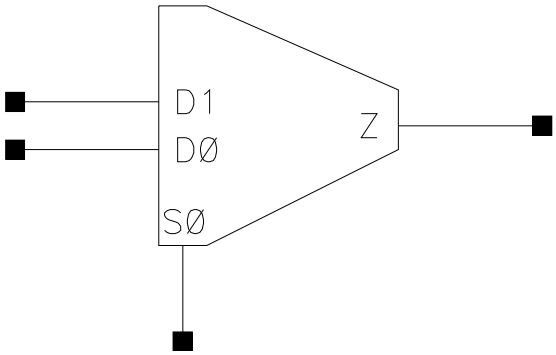
Pin Cycle (vdds)	X8_P4	X33_P4
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
D0	0.0008	0.0012	0.0015	0.0022
D1	0.0008	0.0012	0.0016	0.0021
S0	0.0014	0.0016	0.0018	0.0027

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D0 to Z ↓	0.0250	0.0227	1.5529	0.7606
D0 to Z ↑	0.0209	0.0196	2.0222	0.9906
D1 to Z ↓	0.0237	0.0221	1.5504	0.7594
D1 to Z ↑	0.0191	0.0186	2.0181	0.9885
S0 to Z ↓	0.0220	0.0216	1.5446	0.7578
S0 to Z ↑	0.0209	0.0215	2.0178	0.9888

	X25_P4	X33_P4	X25_P4	X33_P4
D0 to Z ↓	0.0244	0.0220	0.5210	0.3913
D0 to Z ↑	0.0207	0.0194	0.6660	0.4990
D1 to Z ↓	0.0259	0.0227	0.5228	0.3921
D1 to Z ↑	0.0202	0.0190	0.6654	0.4989
S0 to Z ↓	0.0247	0.0227	0.5204	0.3907
S0 to Z ↑	0.0235	0.0218	0.6647	0.4992

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	3.206e-04	1.000e-20
X17_P4	6.379e-04	1.000e-20
X25_P4	8.235e-04	1.000e-20
X33_P4	1.265e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	1.756e-03	2.954e-03	3.592e-03	5.268e-03
D1 (output stable)	1.615e-03	2.911e-03	3.715e-03	5.331e-03
S0 (output stable)	2.026e-03	2.252e-03	2.830e-03	3.748e-03
D0 to Z	5.436e-03	9.586e-03	1.471e-02	1.885e-02
D1 to Z	5.103e-03	9.356e-03	1.486e-02	1.880e-02
S0 to Z	6.295e-03	1.004e-02	1.606e-02	2.001e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

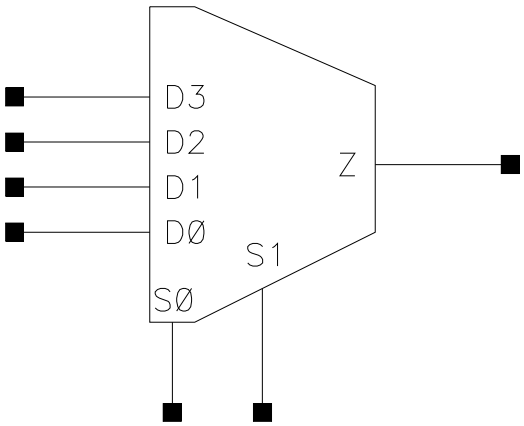
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.312	2.7744
X31_P4	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P4	X31_P4
D0	0.0006	0.0017
D1	0.0006	0.0017
D2	0.0006	0.0017
D3	0.0006	0.0017
S0	0.0021	0.0042
S1	0.0013	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X31_P4	X8_P4	X31_P4

D0 to Z ↓	0.0400	0.0417	1.6026	0.4425
D0 to Z ↑	0.0294	0.0324	2.0326	0.5487
D1 to Z ↓	0.0396	0.0418	1.6012	0.4426
D1 to Z ↑	0.0296	0.0323	2.0316	0.5487
D2 to Z ↓	0.0425	0.0393	1.6090	0.4390
D2 to Z ↑	0.0312	0.0298	2.0390	0.5449
D3 to Z ↓	0.0423	0.0388	1.6091	0.4381
D3 to Z ↑	0.0309	0.0312	2.0375	0.5473
S0 to Z ↓	0.0439	0.0460	1.6035	0.4401
S0 to Z ↑	0.0357	0.0389	2.0358	0.5483
S1 to Z ↓	0.0333	0.0342	1.6053	0.4401
S1 to Z ↑	0.0289	0.0314	2.0343	0.5475

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	3.115e-04	1.000e-20
X31_P4	1.029e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X31_P4
D0 (output stable)	3.251e-05	1.694e-04
D1 (output stable)	3.202e-05	1.546e-04
D2 (output stable)	3.644e-05	1.617e-04
D3 (output stable)	3.648e-05	1.605e-04
S0 (output stable)	2.645e-03	5.694e-03
S1 (output stable)	2.418e-03	4.960e-03
D0 to Z	6.130e-03	2.248e-02
D1 to Z	6.106e-03	2.257e-02
D2 to Z	6.474e-03	2.105e-02
D3 to Z	6.453e-03	2.121e-02
S0 to Z	8.962e-03	2.790e-02
S1 to Z	7.699e-03	2.373e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

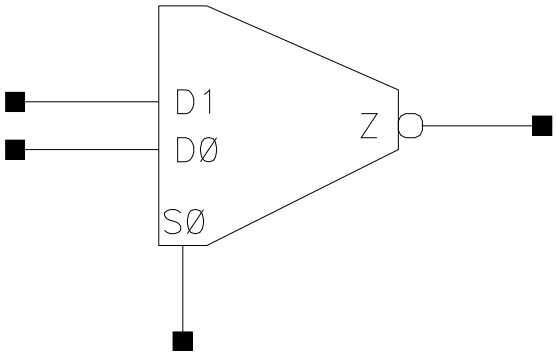
Pin Cycle (vdds)	X8_P4	X31_P4
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.816	0.9792
X5_P4	1.200	0.952	1.1424
X10_P4	1.200	1.768	2.1216
X16_P4	1.200	2.448	2.9376
X21_P4	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P4	X5_P4	X10_P4	X16_P4
D0	0.0006	0.0009	0.0019	0.0029
D1	0.0006	0.0009	0.0018	0.0028
S0	0.0012	0.0021	0.0027	0.0041
	X21_P4			
D0	0.0038			
D1	0.0038			
S0	0.0047			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X5_P4	X3_P4	X5_P4
D0 to Z ↓	0.0081	0.0084	4.5714	2.9112

D0 to Z ↑	0.0140	0.0124	7.4726	3.9339
D1 to Z ↓	0.0080	0.0083	4.5474	2.7560
D1 to Z ↑	0.0143	0.0125	7.4874	4.1312
S0 to Z ↓	0.0132	0.0116	4.5458	2.8275
S0 to Z ↑	0.0144	0.0124	7.4691	4.0270
	X10_P4	**X16_P4**	**X10_P4**	**X16_P4**
D0 to Z ↓	0.0096	0.0089	1.3789	0.9011
D0 to Z ↑	0.0132	0.0125	1.8522	1.2273
D1 to Z ↓	0.0088	0.0086	1.3293	0.8754
D1 to Z ↑	0.0132	0.0126	1.8888	1.2435
S0 to Z ↓	0.0141	0.0122	1.3513	0.8867
S0 to Z ↑	0.0148	0.0128	1.8694	1.2348
	X21_P4		**X21_P4**	
D0 to Z ↓	0.0088		0.6898	
D0 to Z ↑	0.0122		0.9317	
D1 to Z ↓	0.0087		0.6653	
D1 to Z ↑	0.0126		0.9285	
S0 to Z ↓	0.0129		0.6765	
S0 to Z ↑	0.0132		0.9285	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	1.097e-04	1.000e-20
X5_P4	2.719e-04	1.000e-20
X10_P4	4.877e-04	1.000e-20
X16_P4	7.839e-04	1.000e-20
X21_P4	9.617e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	1.927e-05	4.318e-05	1.240e-04	1.925e-04
D1 (output stable)	1.908e-05	4.453e-05	1.050e-04	1.821e-04
S0 (output stable)	1.821e-03	3.020e-03	4.299e-03	7.491e-03
D0 to Z	1.591e-03	2.755e-03	6.453e-03	9.282e-03
D1 to Z	1.596e-03	2.715e-03	6.267e-03	9.171e-03
S0 to Z	3.002e-03	4.924e-03	8.913e-03	1.382e-02
	X21_P4			
D0 (output stable)	2.480e-04			
D1 (output stable)	2.484e-04			
S0 (output stable)	8.025e-03			
D0 to Z	1.210e-02			
D1 to Z	1.216e-02			
S0 to Z	1.648e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

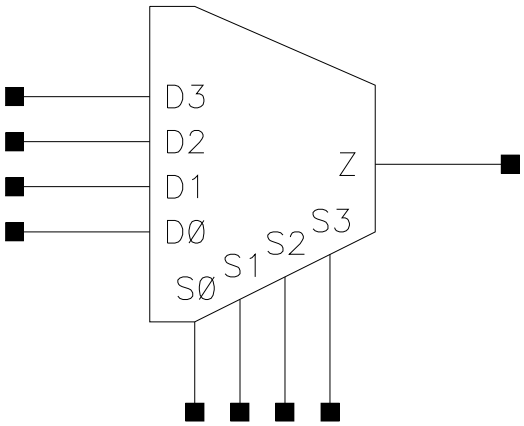
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P4			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	1.768	2.1216
X27_P4	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P4	X27_P4
D0	0.0007	0.0022
D1	0.0007	0.0023
D2	0.0007	0.0022
D3	0.0007	0.0022
S0	0.0007	0.0021
S1	0.0008	0.0021
S2	0.0007	0.0021
S3	0.0008	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	X27_P4	X7_P4	X27_P4
D0 to Z ↓	0.0313	0.0263	2.3963	0.6570
D0 to Z ↑	0.0245	0.0213	1.9797	0.4971
D1 to Z ↓	0.0304	0.0259	2.3935	0.6564
D1 to Z ↑	0.0216	0.0183	1.9713	0.4951
D2 to Z ↓	0.0322	0.0259	2.4002	0.6567
D2 to Z ↑	0.0240	0.0201	1.9870	0.4989
D3 to Z ↓	0.0313	0.0255	2.3963	0.6556
D3 to Z ↑	0.0212	0.0173	1.9779	0.4962
S0 to Z ↓	0.0302	0.0247	2.3957	0.6568
S0 to Z ↑	0.0269	0.0233	1.9785	0.4972
S1 to Z ↓	0.0294	0.0243	2.3929	0.6561
S1 to Z ↑	0.0238	0.0200	1.9704	0.4949
S2 to Z ↓	0.0310	0.0242	2.3996	0.6564
S2 to Z ↑	0.0265	0.0221	1.9858	0.4987
S3 to Z ↓	0.0303	0.0238	2.3954	0.6553
S3 to Z ↑	0.0234	0.0189	1.9774	0.4960

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X7_P4	2.959e-04	1.000e-20
X27_P4	1.293e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X7_P4	X27_P4
D0 (output stable)	7.078e-04	2.306e-03
D1 (output stable)	6.460e-04	2.053e-03
D2 (output stable)	6.598e-04	2.141e-03
D3 (output stable)	5.970e-04	1.893e-03
S0 (output stable)	6.872e-04	2.208e-03
S1 (output stable)	6.238e-04	1.966e-03
S2 (output stable)	6.391e-04	2.045e-03
S3 (output stable)	5.747e-04	1.808e-03
D0 to Z	6.141e-03	1.965e-02
D1 to Z	5.584e-03	1.771e-02
D2 to Z	6.013e-03	1.806e-02
D3 to Z	5.466e-03	1.616e-02
S0 to Z	6.008e-03	1.893e-02
S1 to Z	5.451e-03	1.701e-02
S2 to Z	5.879e-03	1.732e-02
S3 to Z	5.336e-03	1.546e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

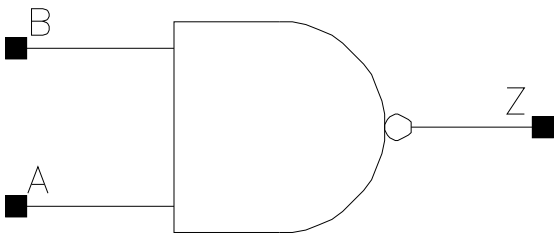
Pin Cycle (vdds)	X7_P4	X27_P4
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P4	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P4	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P4	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P4	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P4	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P4	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P4	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P4	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P4	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P4	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P4	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P4	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P4	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P4	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P4	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P4	C12T28SOI_LL_-NAND2X5_P4	C12T28SOI_LL_-NAND2X7_P4	C12T28SOI_LL_-NAND2X10_P4
A	0.0006	0.0008	0.0009	0.0015
B	0.0006	0.0008	0.0009	0.0014
	C12T28SOI_LL_-NAND2X13_P4	C12T28SOI_LL_-NAND2X17_P4	C12T28SOI_LL_-NAND2X20_P4	C12T28SOI_LL_-NAND2X24_P4
A	0.0019	0.0024	0.0028	0.0034
B	0.0018	0.0023	0.0027	0.0032
	C12T28SOI_LL_-NAND2X27_P4	C12T28SOI_LL_-NAND2X42_P4	C12T28SOI_LL_-NAND2X47_P4	C12T28SOI_LL_-NAND2X50_P4
A	0.0038	0.0011	0.0011	0.0011
B	0.0036	0.0012	0.0012	0.0012
	C12T28SOI_LL_-NAND2X58_P4	C12T28SOI_LL_-NAND2X67_P4	C12T28SOI_-LLBR0D8_-NAND2X7_P4	C12T28SOI_-LLBR0D8_-NAND2X14_P4
A	0.0011	0.0011	0.0009	0.0019
B	0.0012	0.0012	0.0009	0.0018
	C12T28SOI_LLS_-NAND2X40_P4	C12T28SOI_LLS_-NAND2X54_P4		
A	0.0057	0.0076		
B	0.0053	0.0072		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P4	**C12T28SOI_LL_-NAND2X5_P4**	**C12T28SOI_LL_-NAND2X3_P4**	**C12T28SOI_LL_-NAND2X5_P4**
A to Z ↓	0.0062	0.0058	4.4891	2.9458
A to Z ↑	0.0097	0.0087	3.8291	2.5041
B to Z ↓	0.0075	0.0070	4.5529	2.9837
B to Z ↑	0.0083	0.0072	3.8619	2.5267
	C12T28SOI_LL_-NAND2X7_P4	**C12T28SOI_LL_-NAND2X10_P4**	**C12T28SOI_LL_-NAND2X7_P4**	**C12T28SOI_LL_-NAND2X10_P4**
A to Z ↓	0.0059	0.0063	2.4807	1.6354
A to Z ↑	0.0083	0.0090	2.0308	1.3235
B to Z ↓	0.0071	0.0070	2.5086	1.6539
B to Z ↑	0.0067	0.0066	2.0546	1.3367
	C12T28SOI_LL_-NAND2X13_P4	**C12T28SOI_LL_-NAND2X17_P4**	**C12T28SOI_LL_-NAND2X13_P4**	**C12T28SOI_LL_-NAND2X17_P4**
A to Z ↓	0.0063	0.0061	1.2700	1.0036

A to Z ↑	0.0084	0.0085	1.0035	0.8039
B to Z ↓	0.0070	0.0072	1.2839	1.0148
B to Z ↑	0.0061	0.0065	1.0140	0.8111
	C12T28SOI_LL_-NAND2X20_P4	**C12T28SOI_LL_-NAND2X24_P4**	**C12T28SOI_LL_-NAND2X20_P4**	**C12T28SOI_LL_-NAND2X24_P4**
A to Z ↓	0.0062	0.0062	0.8665	0.7342
A to Z ↑	0.0082	0.0083	0.6758	0.5751
B to Z ↓	0.0074	0.0071	0.8763	0.7419
B to Z ↑	0.0063	0.0061	0.6837	0.5801
	C12T28SOI_LL_-NAND2X27_P4	**C12T28SOI_LL_-NAND2X42_P4**	**C12T28SOI_LL_-NAND2X27_P4**	**C12T28SOI_LL_-NAND2X42_P4**
A to Z ↓	0.0062	0.0249	0.6583	0.3124
A to Z ↑	0.0080	0.0251	0.5077	0.3947
B to Z ↓	0.0071	0.0264	0.6654	0.3120
B to Z ↑	0.0058	0.0239	0.5126	0.3950
	C12T28SOI_LL_-NAND2X47_P4	**C12T28SOI_LL_-NAND2X50_P4**	**C12T28SOI_LL_-NAND2X47_P4**	**C12T28SOI_LL_-NAND2X50_P4**
A to Z ↓	0.0257	0.0259	0.2770	0.2603
A to Z ↑	0.0256	0.0258	0.3423	0.3297
B to Z ↓	0.0272	0.0274	0.2770	0.2603
B to Z ↑	0.0244	0.0247	0.3425	0.3293
	C12T28SOI_LL_-NAND2X58_P4	**C12T28SOI_LL_-NAND2X67_P4**	**C12T28SOI_LL_-NAND2X58_P4**	**C12T28SOI_LL_-NAND2X67_P4**
A to Z ↓	0.0272	0.0282	0.2254	0.1977
A to Z ↑	0.0269	0.0277	0.2838	0.2491
B to Z ↓	0.0287	0.0298	0.2253	0.1977
B to Z ↑	0.0257	0.0266	0.2836	0.2493
	C12T28SOI_-LLBR0D8_-NAND2X7_P4	**C12T28SOI_-LLBR0D8_-NAND2X14_P4**	**C12T28SOI_-LLBR0D8_-NAND2X7_P4**	**C12T28SOI_-LLBR0D8_-NAND2X14_P4**
A to Z ↓	0.0033	0.0039	1.8990	1.0013
A to Z ↑	0.0114	0.0115	2.6425	1.2982
B to Z ↓	0.0040	0.0039	1.9319	1.0188
B to Z ↑	0.0094	0.0084	2.7434	1.3271
	C12T28SOI_LLS_-NAND2X40_P4	**C12T28SOI_LLS_-NAND2X54_P4**	**C12T28SOI_LLS_-NAND2X40_P4**	**C12T28SOI_LLS_-NAND2X54_P4**
A to Z ↓	0.0062	0.0063	0.4459	0.3375
A to Z ↑	0.0080	0.0080	0.3408	0.2570
B to Z ↓	0.0071	0.0073	0.4511	0.3415
B to Z ↑	0.0057	0.0059	0.3443	0.2598

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P4	5.136e-05	1.000e-20
C12T28SOI_LL_NAND2X5_P4	9.505e-05	1.000e-20
C12T28SOI_LL_NAND2X7_P4	1.219e-04	1.000e-20
C12T28SOI_LL_NAND2X10_P4	1.690e-04	1.000e-20
C12T28SOI_LL_NAND2X13_P4	2.435e-04	1.000e-20
C12T28SOI_LL_NAND2X17_P4	2.896e-04	1.000e-20
C12T28SOI_LL_NAND2X20_P4	3.570e-04	1.000e-20
C12T28SOI_LL_NAND2X24_P4	4.107e-04	1.000e-20
C12T28SOI_LL_NAND2X27_P4	4.707e-04	1.000e-20

C12T28SOI_LL_NAND2X42_P4	8.313e-04	1.000e-20
C12T28SOI_LL_NAND2X47_P4	9.017e-04	1.000e-20
C12T28SOI_LL_NAND2X50_P4	9.080e-04	1.000e-20
C12T28SOI_LL_NAND2X58_P4	9.847e-04	1.000e-20
C12T28SOI_LL_NAND2X67_P4	1.061e-03	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_P4	1.004e-04	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_-P4	1.976e-04	1.000e-20
C12T28SOI_LLS_NAND2X40_P4	6.980e-04	1.000e-20
C12T28SOI_LLS_NAND2X54_P4	9.254e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND2X3_P4	C12T28SOI_LL_-NAND2X5_P4	C12T28SOI_LL_-NAND2X7_P4	C12T28SOI_LL_-NAND2X10_P4
A (output stable)	1.517e-05	2.354e-05	2.776e-05	9.019e-05
B (output stable)	2.749e-05	4.207e-05	5.137e-05	2.703e-04
A to Z	1.473e-03	2.159e-03	2.615e-03	4.122e-03
B to Z	1.323e-03	1.941e-03	2.329e-03	3.528e-03
	C12T28SOI_LL_-NAND2X13_P4	C12T28SOI_LL_-NAND2X17_P4	C12T28SOI_LL_-NAND2X20_P4	C12T28SOI_LL_-NAND2X24_P4
A (output stable)	1.069e-04	1.240e-04	1.364e-04	1.918e-04
B (output stable)	3.129e-04	2.956e-04	3.269e-04	5.009e-04
A to Z	5.320e-03	6.658e-03	7.789e-03	9.233e-03
B to Z	4.575e-03	5.804e-03	6.801e-03	7.941e-03
	C12T28SOI_LL_-NAND2X27_P4	C12T28SOI_LL_-NAND2X42_P4	C12T28SOI_LL_-NAND2X47_P4	C12T28SOI_LL_-NAND2X50_P4
A (output stable)	2.061e-04	3.041e-05	3.091e-05	3.091e-05
B (output stable)	5.405e-04	5.568e-05	5.668e-05	5.618e-05
A to Z	1.025e-02	1.825e-02	2.015e-02	2.084e-02
B to Z	8.817e-03	1.801e-02	1.991e-02	2.059e-02
	C12T28SOI_LL_-NAND2X58_P4	C12T28SOI_LL_-NAND2X67_P4	C12T28SOI_-LLBR0D8_-NAND2X7_P4	C12T28SOI_-LLBR0D8_-NAND2X14_P4
A (output stable)	3.173e-05	3.141e-05	3.572e-05	1.326e-04
B (output stable)	5.636e-05	5.650e-05	6.739e-05	3.879e-04
A to Z	2.413e-02	2.724e-02	2.562e-03	5.199e-03
B to Z	2.388e-02	2.698e-02	2.199e-03	4.265e-03
	C12T28SOI_LLS_-NAND2X40_P4	C12T28SOI_LLS_-NAND2X54_P4		
A (output stable)	3.007e-04	3.915e-04		
B (output stable)	7.556e-04	9.440e-04		
A to Z	1.516e-02	2.016e-02		
B to Z	1.307e-02	1.741e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND2X3_P4	C12T28SOI_LL_-NAND2X5_P4	C12T28SOI_LL_-NAND2X7_P4	C12T28SOI_LL_-NAND2X10_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

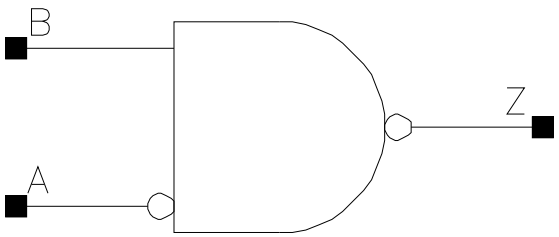
	C12T28SOI_LL_-NAND2X13_P4	C12T28SOI_LL_-NAND2X17_P4	C12T28SOI_LL_-NAND2X20_P4	C12T28SOI_LL_-NAND2X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P4	C12T28SOI_LL_-NAND2X42_P4	C12T28SOI_LL_-NAND2X47_P4	C12T28SOI_LL_-NAND2X50_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P4	C12T28SOI_LL_-NAND2X67_P4	C12T28SOI_-LLBR0D8_-NAND2X7_P4	C12T28SOI_-LLBR0D8_-NAND2X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P4	C12T28SOI_LLS_-NAND2X54_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X7_P4	1.200	0.544	0.6528
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X40_P4	1.200	2.312	2.7744
X54_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P4	X7_P4	X13_P4	X27_P4
A	0.0009	0.0009	0.0012	0.0022
B	0.0007	0.0009	0.0017	0.0036
	X40_P4	X54_P4		
A	0.0033	0.0043		
B	0.0052	0.0071		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0175	0.0189	4.4292	2.4567
A to Z ↑	0.0138	0.0147	3.6592	1.9830
B to Z ↓	0.0078	0.0071	4.5838	2.5235
B to Z ↑	0.0083	0.0067	3.8643	2.0746
	X13_P4	**X27_P4**	**X13_P4**	**X27_P4**

A to Z ↓	0.0176	0.0174	1.3299	0.6587
A to Z ↑	0.0145	0.0143	1.0246	0.4973
B to Z ↓	0.0070	0.0070	1.3667	0.6773
B to Z ↑	0.0060	0.0057	1.0365	0.5133
	X40_P4	**X54_P4**	**X40_P4**	**X54_P4**
A to Z ↓	0.0174	0.0174	0.4387	0.3328
A to Z ↑	0.0145	0.0143	0.3305	0.2498
B to Z ↓	0.0071	0.0071	0.4511	0.3421
B to Z ↑	0.0058	0.0057	0.3453	0.2610

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	9.928e-05	1.000e-20
X7_P4	1.687e-04	1.000e-20
X13_P4	3.669e-04	1.000e-20
X27_P4	7.138e-04	1.000e-20
X40_P4	1.053e-03	1.000e-20
X54_P4	1.393e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	1.943e-03	2.270e-03	3.933e-03	7.841e-03
B (output stable)	2.815e-05	5.139e-05	2.871e-04	4.916e-04
A to Z	2.982e-03	4.039e-03	7.489e-03	1.492e-02
B to Z	1.319e-03	2.299e-03	4.472e-03	8.866e-03
	X40_P4	X54_P4		
A (output stable)	1.174e-02	1.541e-02		
B (output stable)	7.170e-04	9.204e-04		
A to Z	2.226e-02	2.929e-02		
B to Z	1.314e-02	1.734e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

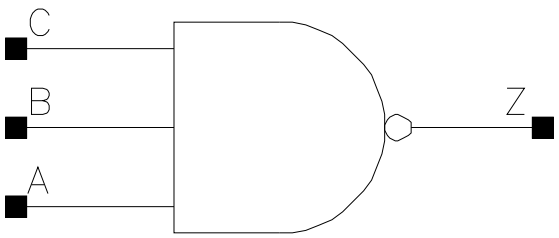
Pin Cycle (vdds)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P4	X54_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P4	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P4	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P4	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P4	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P4	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P4	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P4	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P4	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P4	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P4	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P4	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P4	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P4	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P4	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P4	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P4	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A	0.0008	0.0010	0.0015	0.0019
B	0.0008	0.0010	0.0015	0.0018
C	0.0007	0.0009	0.0014	0.0018
	C12T28SOI_LL_-NAND3X15_P4	C12T28SOI_LL_-NAND3X18_P4	C12T28SOI_LL_-NAND3X21_P4	C12T28SOI_LL_-NAND3X24_P4
A	0.0025	0.0028	0.0034	0.0038
B	0.0023	0.0027	0.0033	0.0036
C	0.0023	0.0026	0.0032	0.0035
	C12T28SOI_LL_-NAND3X35_P4	C12T28SOI_LL_-NAND3X47_P4	C12T28SOI_-LLBR0P6_-NAND3X6_P4	C12T28SOI_-LLBR0P6_-NAND3X12_P4
A	0.0058	0.0076	0.0010	0.0019
B	0.0055	0.0073	0.0010	0.0018
C	0.0052	0.0071	0.0009	0.0017
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	C12T28SOI_-LLBR0P6_-NAND3X24_P4	C12T28SOI_-LLBR0P6_-NAND3X35_P4	C12T28SOI_-LLBR0P6_-NAND3X47_P4
A	0.0028	0.0038	0.0056	0.0075
B	0.0026	0.0036	0.0053	0.0071
C	0.0025	0.0034	0.0051	0.0068
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4			
A	0.0029			
B	0.0028			
C	0.0026			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4
A to Z ↓	0.0102	0.0095	4.6190	3.3529
A to Z ↑	0.0121	0.0108	2.8345	1.9795
B to Z ↓	0.0116	0.0107	4.6450	3.3700
B to Z ↑	0.0113	0.0099	2.8441	1.9865
C to Z ↓	0.0116	0.0110	4.6613	3.3828
C to Z ↑	0.0093	0.0080	2.8501	2.0033

	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A to Z ↓	0.0101	0.0098	2.2601	1.7786
A to Z ↑	0.0113	0.0105	1.3348	1.0168
B to Z ↓	0.0107	0.0104	2.2690	1.7857
B to Z ↑	0.0100	0.0092	1.3383	1.0205
C to Z ↓	0.0108	0.0106	2.2780	1.7928
C to Z ↑	0.0080	0.0071	1.3366	1.0143
	C12T28SOI_LL_-NAND3X15_P4	**C12T28SOI_LL_-NAND3X18_P4**	**C12T28SOI_LL_-NAND3X15_P4**	**C12T28SOI_LL_-NAND3X18_P4**
A to Z ↓	0.0092	0.0091	1.4167	1.2220
A to Z ↑	0.0102	0.0098	0.8062	0.6766
B to Z ↓	0.0103	0.0103	1.4235	1.2278
B to Z ↑	0.0089	0.0085	0.8099	0.6790
C to Z ↓	0.0105	0.0105	1.4298	1.2327
C to Z ↑	0.0071	0.0066	0.8172	0.6854
	C12T28SOI_LL_-NAND3X21_P4	**C12T28SOI_LL_-NAND3X24_P4**	**C12T28SOI_LL_-NAND3X21_P4**	**C12T28SOI_LL_-NAND3X24_P4**
A to Z ↓	0.0095	0.0095	1.0317	0.9286
A to Z ↑	0.0103	0.0100	0.5798	0.5129
B to Z ↓	0.0104	0.0103	1.0360	0.9324
B to Z ↑	0.0090	0.0087	0.5814	0.5142
C to Z ↓	0.0107	0.0107	1.0401	0.9362
C to Z ↑	0.0071	0.0068	0.5837	0.5156
	C12T28SOI_LL_-NAND3X35_P4	**C12T28SOI_LL_-NAND3X47_P4**	**C12T28SOI_LL_-NAND3X35_P4**	**C12T28SOI_LL_-NAND3X47_P4**
A to Z ↓	0.0091	0.0094	0.6327	0.4821
A to Z ↑	0.0098	0.0099	0.3445	0.2609
B to Z ↓	0.0103	0.0104	0.6357	0.4843
B to Z ↑	0.0084	0.0085	0.3450	0.2602
C to Z ↓	0.0107	0.0108	0.6384	0.4866
C to Z ↑	0.0065	0.0064	0.3472	0.2617
	C12T28SOI_-LLBR0P6_-NAND3X6_P4	**C12T28SOI_-LLBR0P6_-NAND3X12_P4**	**C12T28SOI_-LLBR0P6_-NAND3X6_P4**	**C12T28SOI_-LLBR0P6_-NAND3X12_P4**
A to Z ↓	0.0057	0.0061	2.3063	1.2248
A to Z ↑	0.0168	0.0166	3.0128	1.5463
B to Z ↓	0.0063	0.0059	2.3310	1.2381
B to Z ↑	0.0151	0.0143	3.0236	1.5491
C to Z ↓	0.0057	0.0051	2.3567	1.2522
C to Z ↑	0.0118	0.0109	3.0414	1.5545
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	**C12T28SOI_-LLBR0P6_-NAND3X24_P4**	**C12T28SOI_-LLBR0P6_-NAND3X18_P4**	**C12T28SOI_-LLBR0P6_-NAND3X24_P4**
A to Z ↓	0.0054	0.0058	0.8443	0.6420
A to Z ↑	0.0157	0.0160	1.0298	0.7790
B to Z ↓	0.0057	0.0058	0.8536	0.6489
B to Z ↑	0.0133	0.0137	1.0331	0.7804
C to Z ↓	0.0052	0.0052	0.8623	0.6560
C to Z ↑	0.0103	0.0103	1.0408	0.7815
	C12T28SOI_-LLBR0P6_-NAND3X35_P4	**C12T28SOI_-LLBR0P6_-NAND3X47_P4**	**C12T28SOI_-LLBR0P6_-NAND3X35_P4**	**C12T28SOI_-LLBR0P6_-NAND3X47_P4**

A to Z ↓	0.0054	0.0057	0.4394	0.3362
A to Z ↑	0.0160	0.0162	0.5381	0.4081
B to Z ↓	0.0057	0.0058	0.4446	0.3401
B to Z ↑	0.0136	0.0136	0.5383	0.4078
C to Z ↓	0.0052	0.0056	0.4496	0.3434
C to Z ↑	0.0102	0.0105	0.5442	0.4086
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P4**	
A to Z ↓	0.0064		0.8372	
A to Z ↑	0.0160		0.9898	
B to Z ↓	0.0061		0.8451	
B to Z ↑	0.0137		0.9917	
C to Z ↓	0.0054		0.8541	
C to Z ↑	0.0102		0.9852	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P4	6.218e-05	1.000e-20
C12T28SOI_LL_NAND3X6_P4	1.012e-04	1.000e-20
C12T28SOI_LL_NAND3X9_P4	1.329e-04	1.000e-20
C12T28SOI_LL_NAND3X12_P4	1.902e-04	1.000e-20
C12T28SOI_LL_NAND3X15_P4	2.228e-04	1.000e-20
C12T28SOI_LL_NAND3X18_P4	2.737e-04	1.000e-20
C12T28SOI_LL_NAND3X21_P4	3.197e-04	1.000e-20
C12T28SOI_LL_NAND3X24_P4	3.658e-04	1.000e-20
C12T28SOI_LL_NAND3X35_P4	5.413e-04	1.000e-20
C12T28SOI_LL_NAND3X47_P4	7.167e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_P4	7.818e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P4	1.428e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P4	1.992e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P4	2.682e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P4	3.933e-04	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P4	5.182e-04	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P4	2.544e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A (output stable)	3.229e-05	4.305e-05	9.981e-05	1.169e-04
B (output stable)	5.247e-05	6.625e-05	1.502e-04	1.760e-04
C (output stable)	1.956e-04	2.374e-04	3.640e-04	4.266e-04
A to Z	2.502e-03	3.295e-03	5.046e-03	6.275e-03
B to Z	2.292e-03	2.989e-03	4.415e-03	5.529e-03
C to Z	2.012e-03	2.654e-03	3.890e-03	4.900e-03

	C12T28SOI_LL_-NAND3X15_P4	C12T28SOI_LL_-NAND3X18_P4	C12T28SOI_LL_-NAND3X21_P4	C12T28SOI_LL_-NAND3X24_P4
A (output stable)	1.283e-04	1.431e-04	2.015e-04	2.163e-04
B (output stable)	1.927e-04	2.180e-04	2.945e-04	3.231e-04
C (output stable)	4.539e-04	5.112e-04	6.909e-04	7.524e-04
A to Z	7.681e-03	8.885e-03	1.080e-02	1.198e-02
B to Z	6.711e-03	7.774e-03	9.499e-03	1.054e-02
C to Z	5.993e-03	6.910e-03	8.405e-03	9.308e-03
	C12T28SOI_LL_-NAND3X35_P4	C12T28SOI_LL_-NAND3X47_P4	C12T28SOI_-LLBR0P6_-NAND3X6_P4	C12T28SOI_-LLBR0P6_-NAND3X12_P4
A (output stable)	2.942e-04	3.865e-04	6.061e-05	1.649e-04
B (output stable)	4.404e-04	5.688e-04	9.256e-05	2.536e-04
C (output stable)	1.092e-03	1.396e-03	3.158e-04	5.996e-04
A to Z	1.762e-02	2.332e-02	3.340e-03	6.456e-03
B to Z	1.539e-02	2.039e-02	2.909e-03	5.352e-03
C to Z	1.346e-02	1.785e-02	2.393e-03	4.333e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	C12T28SOI_-LLBR0P6_-NAND3X24_P4	C12T28SOI_-LLBR0P6_-NAND3X35_P4	C12T28SOI_-LLBR0P6_-NAND3X47_P4
A (output stable)	2.014e-04	3.047e-04	4.096e-04	5.388e-04
B (output stable)	3.038e-04	4.554e-04	6.050e-04	8.038e-04
C (output stable)	7.045e-04	1.076e-03	1.553e-03	2.018e-03
A to Z	8.996e-03	1.224e-02	1.787e-02	2.363e-02
B to Z	7.431e-03	1.015e-02	1.473e-02	1.950e-02
C to Z	6.175e-03	8.270e-03	1.187e-02	1.584e-02
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4			
A (output stable)	2.405e-04			
B (output stable)	3.772e-04			
C (output stable)	8.579e-04			
A to Z	9.784e-03			
B to Z	8.135e-03			
C to Z	6.650e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P4	C12T28SOI_LL_-NAND3X6_P4	C12T28SOI_LL_-NAND3X9_P4	C12T28SOI_LL_-NAND3X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P4	C12T28SOI_LL_-NAND3X18_P4	C12T28SOI_LL_-NAND3X21_P4	C12T28SOI_LL_-NAND3X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

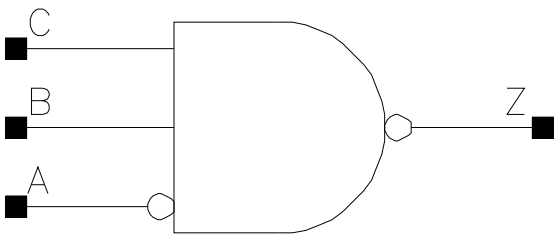
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P4	C12T28SOI_LL_-NAND3X47_P4	C12T28SOI_-LLBR0P6_-NAND3X6_P4	C12T28SOI_-LLBR0P6_-NAND3X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P4	C12T28SOI_-LLBR0P6_-NAND3X24_P4	C12T28SOI_-LLBR0P6_-NAND3X35_P4	C12T28SOI_-LLBR0P6_-NAND3X47_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.816	0.9792
X12_P4	1.200	1.224	1.4688
X18_P4	1.200	1.496	1.7952
X24_P4	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0008	0.0012	0.0012	0.0022
B	0.0009	0.0018	0.0027	0.0036
C	0.0009	0.0018	0.0026	0.0035

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X12_P4**	**X6_P4**	**X12_P4**
A to Z ↓	0.0214	0.0205	3.3258	1.7881
A to Z ↑	0.0157	0.0157	1.9232	0.9674
B to Z ↓	0.0098	0.0099	3.3557	1.8061
B to Z ↑	0.0087	0.0085	1.9958	1.0093
C to Z ↓	0.0105	0.0099	3.3754	1.8128
C to Z ↑	0.0073	0.0064	2.0104	1.0190
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0236	0.0202	1.2208	0.9297

A to Z ↑	0.0184	0.0152	0.6524	0.4900
B to Z ↓	0.0102	0.0100	1.2311	0.9372
B to Z ↑	0.0085	0.0083	0.6804	0.5121
C to Z ↓	0.0107	0.0102	1.2357	0.9410
C to Z ↑	0.0068	0.0063	0.6862	0.5168

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P4	1.461e-04	1.000e-20
X12_P4	3.145e-04	1.000e-20
X18_P4	3.969e-04	1.000e-20
X24_P4	6.117e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	2.219e-03	4.104e-03	5.050e-03	7.988e-03
B (output stable)	5.011e-05	1.490e-04	2.286e-04	3.330e-04
C (output stable)	1.106e-04	4.303e-04	5.130e-04	7.970e-04
A to Z	4.578e-03	8.893e-03	1.251e-02	1.746e-02
B to Z	2.728e-03	5.247e-03	7.760e-03	1.023e-02
C to Z	2.476e-03	4.562e-03	6.936e-03	8.880e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

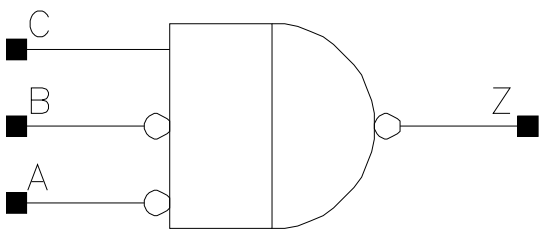
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	0.816	0.9792
X13_P4	1.200	1.088	1.3056
X20_P4	1.200	1.632	1.9584
X27_P4	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P4	X13_P4	X20_P4	X27_P4
A	0.0011	0.0011	0.0021	0.0020
B	0.0012	0.0012	0.0022	0.0021
C	0.0009	0.0018	0.0026	0.0036

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	**X13_P4**	**X7_P4**	**X13_P4**
A to Z ↓	0.0191	0.0232	2.3646	1.2559
A to Z ↑	0.0137	0.0162	1.9071	0.9622
B to Z ↓	0.0205	0.0249	2.3647	1.2552
B to Z ↑	0.0125	0.0151	1.9086	0.9613
C to Z ↓	0.0070	0.0068	2.4257	1.2850
C to Z ↑	0.0067	0.0059	1.9943	1.0128
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0210	0.0227	0.8564	0.6522
A to Z ↑	0.0150	0.0184	0.6505	0.4889
B to Z ↓	0.0217	0.0236	0.8560	0.6520

B to Z ↑	0.0132	0.0170	0.6499	0.4879
C to Z ↓	0.0076	0.0073	0.8770	0.6677
C to Z ↑	0.0064	0.0061	0.6834	0.5134

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X7_P4	2.139e-04	1.000e-20
X13_P4	2.848e-04	1.000e-20
X20_P4	4.735e-04	1.000e-20
X27_P4	5.323e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	1.260e-03	1.551e-03	2.690e-03	2.953e-03
B (output stable)	1.169e-03	1.461e-03	2.548e-03	2.817e-03
C (output stable)	5.522e-05	3.282e-04	3.248e-04	4.041e-04
A to Z	5.528e-03	8.776e-03	1.376e-02	1.695e-02
B to Z	5.183e-03	8.453e-03	1.269e-02	1.596e-02
C to Z	2.423e-03	4.546e-03	6.916e-03	9.140e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

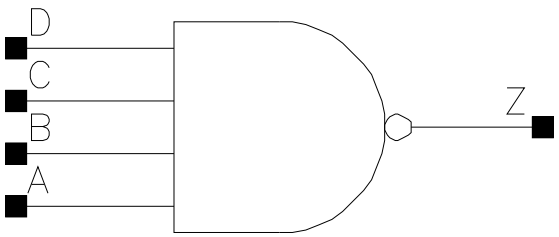
Pin Cycle (vdds)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0007	0.0007	0.0009	0.0011
B	0.0008	0.0008	0.0009	0.0012
C	0.0007	0.0008	0.0010	0.0011
D	0.0007	0.0007	0.0010	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0299	0.0299	1.5105	0.7559
A to Z ↑	0.0256	0.0280	1.9619	0.9715
B to Z ↓	0.0314	0.0320	1.5120	0.7561
B to Z ↑	0.0244	0.0272	1.9645	0.9699
C to Z ↓	0.0307	0.0303	1.5098	0.7562
C to Z ↑	0.0263	0.0289	1.9649	0.9695

D to Z ↓	0.0326	0.0321	1.5097	0.7560
D to Z ↑	0.0253	0.0276	1.9628	0.9689
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0319	0.0299	0.5208	0.3891
A to Z ↑	0.0270	0.0269	0.6565	0.4918
B to Z ↓	0.0337	0.0315	0.5209	0.3892
B to Z ↑	0.0260	0.0257	0.6560	0.4917
C to Z ↓	0.0305	0.0284	0.5208	0.3895
C to Z ↑	0.0271	0.0267	0.6538	0.4903
D to Z ↓	0.0323	0.0301	0.5203	0.3895
D to Z ↑	0.0259	0.0255	0.6545	0.4907

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	2.023e-04	1.000e-20
X17_P4	3.218e-04	1.000e-20
X25_P4	4.656e-04	1.000e-20
X33_P4	6.692e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	8.886e-04	1.043e-03	1.505e-03	1.871e-03
B (output stable)	8.336e-04	9.883e-04	1.423e-03	1.768e-03
C (output stable)	8.883e-04	1.009e-03	1.505e-03	1.810e-03
D (output stable)	8.267e-04	9.488e-04	1.417e-03	1.699e-03
A to Z	6.198e-03	9.574e-03	1.461e-02	1.835e-02
B to Z	6.049e-03	9.428e-03	1.439e-02	1.807e-02
C to Z	6.327e-03	9.459e-03	1.397e-02	1.733e-02
D to Z	6.179e-03	9.300e-03	1.375e-02	1.704e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

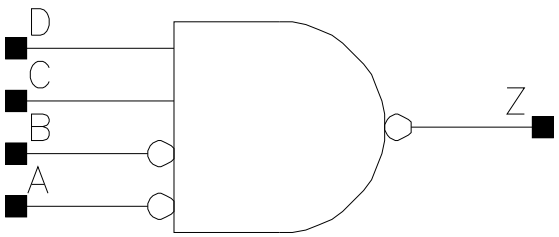
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X12_P4	1.200	1.496	1.7952
X18_P4	1.200	2.040	2.4480
X24_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0011	0.0011	0.0021	0.0020
B	0.0011	0.0016	0.0022	0.0021
C	0.0009	0.0018	0.0027	0.0036
D	0.0009	0.0018	0.0026	0.0036

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X12_P4	X6_P4	X12_P4
A to Z ↓	0.0204	0.0266	3.4248	1.7903
A to Z ↑	0.0145	0.0181	1.9079	0.9642
B to Z ↓	0.0215	0.0282	3.4263	1.7902
B to Z ↑	0.0128	0.0167	1.9055	0.9635
C to Z ↓	0.0099	0.0099	3.4544	1.8054
C to Z ↑	0.0089	0.0085	2.1266	1.0088

D to Z ↓	0.0104	0.0099	3.4726	1.8121
D to Z ↑	0.0074	0.0063	2.1409	1.0184
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0236	0.0258	1.2192	0.9280
A to Z ↑	0.0160	0.0209	0.6501	0.4892
B to Z ↓	0.0242	0.0266	1.2193	0.9280
B to Z ↑	0.0142	0.0193	0.6499	0.4883
C to Z ↓	0.0101	0.0103	1.2281	0.9346
C to Z ↑	0.0084	0.0086	0.6827	0.5099
D to Z ↓	0.0104	0.0105	1.2336	0.9386
D to Z ↑	0.0066	0.0065	0.6988	0.5158

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P4	1.883e-04	1.000e-20
X12_P4	2.469e-04	1.000e-20
X18_P4	4.172e-04	1.000e-20
X24_P4	4.552e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	1.482e-03	2.102e-03	3.426e-03	3.809e-03
B (output stable)	1.374e-03	1.994e-03	3.172e-03	3.570e-03
C (output stable)	5.689e-05	1.609e-04	2.322e-04	3.187e-04
D (output stable)	1.253e-04	4.528e-04	5.447e-04	8.283e-04
A to Z	5.617e-03	9.878e-03	1.504e-02	1.918e-02
B to Z	5.348e-03	9.431e-03	1.401e-02	1.814e-02
C to Z	2.643e-03	5.243e-03	7.678e-03	1.046e-02
D to Z	2.401e-03	4.561e-03	6.858e-03	9.161e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

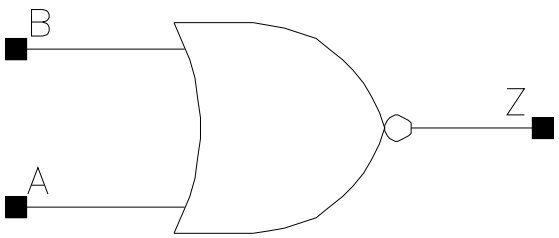
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.408	0.4896
X5_P4	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X10_P4	1.200	0.680	0.8160
X14_P4	1.200	0.680	0.8160
X17_P4	1.200	0.952	1.1424
X21_P4	1.200	0.952	1.1424
X24_P4	1.200	1.224	1.4688
X27_P4	1.200	1.224	1.4688
X34_P4	1.200	1.496	1.7952
X40_P4	1.200	1.360	1.6320
X41_P4	1.200	1.768	2.1216
X49_P4	1.200	1.496	1.7952
X53_P4	1.200	1.904	2.2848
X55_P4	1.200	2.312	2.7744
X57_P4	1.200	1.904	2.2848
X65_P4	1.200	2.040	2.4480
X84_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P4	X5_P4	X7_P4	X10_P4
A	0.0006	0.0007	0.0009	0.0015
B	0.0006	0.0007	0.0010	0.0014
	X14_P4	X17_P4	X21_P4	X24_P4

A	0.0019	0.0025	0.0029	0.0034
B	0.0018	0.0023	0.0027	0.0032
	X27_P4	X34_P4	X40_P4	X41_P4
A	0.0037	0.0047	0.0011	0.0057
B	0.0036	0.0043	0.0012	0.0054
	X49_P4	X53_P4	X55_P4	X57_P4
A	0.0011	0.0011	0.0076	0.0011
B	0.0012	0.0011	0.0072	0.0011
	X65_P4	X84_P4		
A	0.0011	0.0012		
B	0.0011	0.0011		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X5_P4**	**X3_P4**	**X5_P4**
A to Z ↓	0.0053	0.0051	2.9665	2.1587
A to Z ↑	0.0107	0.0099	6.7795	5.0107
B to Z ↓	0.0041	0.0036	3.0394	2.1795
B to Z ↑	0.0118	0.0109	6.8325	5.0385
	X7_P4	**X10_P4**	**X7_P4**	**X10_P4**
A to Z ↓	0.0051	0.0052	1.5933	1.0288
A to Z ↑	0.0092	0.0097	3.5708	2.3878
B to Z ↓	0.0037	0.0030	1.6167	1.0413
B to Z ↑	0.0101	0.0097	3.5930	2.3973
	X14_P4	**X17_P4**	**X14_P4**	**X17_P4**
A to Z ↓	0.0053	0.0052	0.7868	0.6295
A to Z ↑	0.0090	0.0092	1.7845	1.4358
B to Z ↓	0.0031	0.0036	0.7967	0.6361
B to Z ↑	0.0092	0.0099	1.7932	1.4424
	X21_P4	**X24_P4**	**X21_P4**	**X24_P4**
A to Z ↓	0.0054	0.0052	0.5360	0.4559
A to Z ↑	0.0088	0.0090	1.2016	1.0500
B to Z ↓	0.0036	0.0032	0.5415	0.4613
B to Z ↑	0.0096	0.0095	1.2078	1.0553
	X27_P4	**X34_P4**	**X27_P4**	**X34_P4**
A to Z ↓	0.0052	0.0055	0.4059	0.3272
A to Z ↑	0.0087	0.0089	0.9286	0.7387
B to Z ↓	0.0032	0.0036	0.4111	0.3309
B to Z ↑	0.0092	0.0095	0.9338	0.7426
	X40_P4	**X41_P4**	**X40_P4**	**X41_P4**
A to Z ↓	0.0225	0.0053	0.3188	0.2727
A to Z ↑	0.0288	0.0086	0.4025	0.6113
B to Z ↓	0.0213	0.0033	0.3187	0.2761
B to Z ↑	0.0305	0.0090	0.4025	0.6146
	X49_P4	**X53_P4**	**X49_P4**	**X53_P4**
A to Z ↓	0.0234	0.0246	0.2647	0.2426
A to Z ↑	0.0296	0.0335	0.3346	0.3087
B to Z ↓	0.0222	0.0234	0.2649	0.2426
B to Z ↑	0.0314	0.0351	0.3342	0.3085
	X55_P4	**X57_P4**	**X55_P4**	**X57_P4**
A to Z ↓	0.0054	0.0248	0.2061	0.2284
A to Z ↑	0.0086	0.0337	0.4613	0.2879

B to Z ↓	0.0034	0.0237	0.2090	0.2282
B to Z ↑	0.0091	0.0353	0.4639	0.2879
	X65_P4	**X84_P4**	**X65_P4**	**X84_P4**
A to Z ↓	0.0256	0.0268	0.1999	0.1584
A to Z ↑	0.0344	0.0351	0.2517	0.2007
B to Z ↓	0.0244	0.0255	0.2001	0.1583
B to Z ↑	0.0361	0.0367	0.2518	0.2006

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	5.264e-05	1.000e-20
X5_P4	8.144e-05	1.000e-20
X7_P4	1.265e-04	1.000e-20
X10_P4	1.753e-04	1.000e-20
X14_P4	2.535e-04	1.000e-20
X17_P4	3.009e-04	1.000e-20
X21_P4	3.723e-04	1.000e-20
X24_P4	4.273e-04	1.000e-20
X27_P4	4.910e-04	1.000e-20
X34_P4	6.099e-04	1.000e-20
X40_P4	1.042e-03	1.000e-20
X41_P4	7.288e-04	1.000e-20
X49_P4	1.193e-03	1.000e-20
X53_P4	1.345e-03	1.000e-20
X55_P4	9.666e-04	1.000e-20
X57_P4	1.442e-03	1.000e-20
X65_P4	1.594e-03	1.000e-20
X84_P4	1.868e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	2.435e-05	3.314e-05	4.538e-05	1.295e-04
B (output stable)	4.367e-05	5.718e-05	7.886e-05	3.510e-04
A to Z	1.430e-03	1.862e-03	2.559e-03	3.982e-03
B to Z	1.248e-03	1.618e-03	2.198e-03	3.243e-03
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	1.522e-04	1.824e-04	2.023e-04	2.554e-04
B (output stable)	4.082e-04	4.190e-04	4.246e-04	6.010e-04
A to Z	5.172e-03	6.475e-03	7.606e-03	8.870e-03
B to Z	4.250e-03	5.459e-03	6.409e-03	7.376e-03
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	2.732e-04	3.266e-04	4.509e-05	4.264e-04
B (output stable)	6.487e-04	6.603e-04	7.936e-05	9.622e-04
A to Z	9.910e-03	1.247e-02	1.807e-02	1.485e-02
B to Z	8.220e-03	1.049e-02	1.776e-02	1.231e-02
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	4.609e-05	4.909e-05	5.570e-04	4.727e-05
B (output stable)	8.036e-05	8.836e-05	1.268e-03	8.636e-05
A to Z	2.065e-02	2.517e-02	1.976e-02	2.626e-02
B to Z	2.035e-02	2.485e-02	1.635e-02	2.594e-02
	X65_P4	X84_P4		

A (output stable)	4.709e-05	4.364e-05		
B (output stable)	8.136e-05	8.000e-05		
A to Z	2.891e-02	3.505e-02		
B to Z	2.859e-02	3.468e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

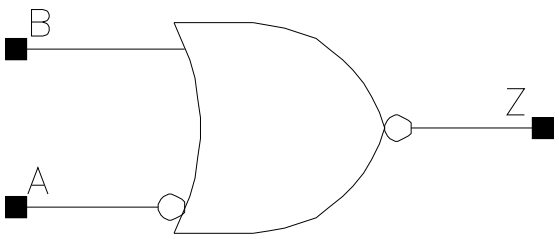
Pin Cycle (vdds)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P4	X84_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X7_P4	1.200	0.680	0.8160
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X41_P4	1.200	2.312	2.7744
X55_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X7_P4	X13_P4
A	0.0008	0.0008	0.0008	0.0012
B	0.0006	0.0010	0.0009	0.0017
	X27_P4	X41_P4	X55_P4	
A	0.0022	0.0033	0.0043	
B	0.0035	0.0054	0.0071	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0165	0.0185	2.7780	1.8411
A to Z ↑	0.0150	0.0154	6.7113	3.5474
B to Z ↓	0.0043	0.0050	3.0127	1.9861
B to Z ↑	0.0118	0.0096	6.8140	3.6093

	X7_P4	X13_P4	X7_P4	X13_P4
A to Z ↓	0.0187	0.0169	1.4724	0.7979
A to Z ↑	0.0169	0.0167	3.5321	1.8923
B to Z ↓	0.0039	0.0033	1.5516	0.8386
B to Z ↑	0.0110	0.0101	3.5730	1.9170
	X27_P4	**X41_P4**	**X27_P4**	**X41_P4**
A to Z ↓	0.0164	0.0168	0.3817	0.2584
A to Z ↑	0.0158	0.0161	0.9028	0.6074
B to Z ↓	0.0033	0.0034	0.4138	0.2783
B to Z ↑	0.0094	0.0094	0.9158	0.6157
	X55_P4		**X55_P4**	
A to Z ↓	0.0164		0.1954	
A to Z ↑	0.0158		0.4589	
B to Z ↓	0.0034		0.2108	
B to Z ↑	0.0093		0.4654	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	1.006e-04	1.000e-20
X6_P4	1.716e-04	1.000e-20
X7_P4	1.878e-04	1.000e-20
X13_P4	3.713e-04	1.000e-20
X27_P4	7.339e-04	1.000e-20
X41_P4	1.084e-03	1.000e-20
X55_P4	1.434e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	1.932e-03	2.238e-03	2.352e-03	3.991e-03
B (output stable)	4.361e-05	7.823e-05	2.013e-04	3.535e-04
A to Z	2.955e-03	3.921e-03	4.457e-03	7.669e-03
B to Z	1.252e-03	2.079e-03	2.410e-03	4.285e-03
	X27_P4	X41_P4	X55_P4	
A (output stable)	7.971e-03	1.195e-02	1.566e-02	
B (output stable)	6.825e-04	9.657e-04	1.255e-03	
A to Z	1.540e-02	2.294e-02	3.005e-02	
B to Z	8.528e-03	1.258e-02	1.659e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

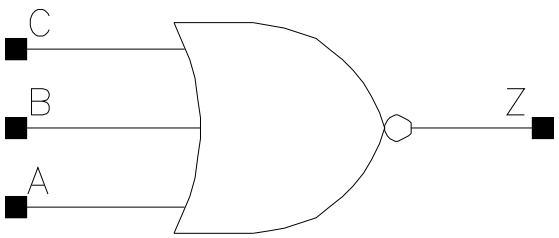
Pin Cycle (vdds)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P4	X41_P4	X55_P4	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X9_P4	1.200	0.952	1.1424
X13_P4	1.200	0.952	1.1424
X16_P4	1.200	1.360	1.6320
X19_P4	1.200	1.496	1.7952
X22_P4	1.200	1.768	2.1216
X25_P4	1.200	1.904	2.2848
X37_P4	1.200	2.584	3.1008
X49_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P4	X6_P4	X9_P4	X13_P4
A	0.0008	0.0009	0.0014	0.0018
B	0.0007	0.0009	0.0016	0.0019
C	0.0008	0.0009	0.0014	0.0017
	X16_P4	X19_P4	X22_P4	X25_P4
A	0.0024	0.0028	0.0033	0.0037
B	0.0024	0.0032	0.0035	0.0043
C	0.0022	0.0026	0.0031	0.0034
	X37_P4	X49_P4		
A	0.0056	0.0075		
B	0.0056	0.0076		

C	0.0051	0.0070		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0064	0.0062	2.1908	1.6187
A to Z ↑	0.0135	0.0123	7.2436	5.1625
B to Z ↓	0.0057	0.0055	2.1991	1.6230
B to Z ↑	0.0142	0.0129	7.2518	5.1717
C to Z ↓	0.0045	0.0041	2.2184	1.6419
C to Z ↑	0.0147	0.0133	7.2681	5.1816
	X9_P4	**X13_P4**	**X9_P4**	**X13_P4**
A to Z ↓	0.0064	0.0064	1.0588	0.8161
A to Z ↑	0.0131	0.0122	3.4336	2.5831
B to Z ↓	0.0055	0.0053	1.0366	0.7866
B to Z ↑	0.0137	0.0127	3.4430	2.5886
C to Z ↓	0.0035	0.0034	1.0490	0.8028
C to Z ↑	0.0127	0.0119	3.4383	2.5868
	X16_P4	**X19_P4**	**X16_P4**	**X19_P4**
A to Z ↓	0.0063	0.0063	0.6337	0.5378
A to Z ↑	0.0127	0.0124	2.0815	1.7299
B to Z ↓	0.0057	0.0057	0.6364	0.5284
B to Z ↑	0.0133	0.0133	2.0864	1.7343
C to Z ↓	0.0038	0.0039	0.6417	0.5488
C to Z ↑	0.0130	0.0124	2.0872	1.7345
	X22_P4	**X25_P4**	**X22_P4**	**X25_P4**
A to Z ↓	0.0063	0.0063	0.4648	0.4092
A to Z ↑	0.0124	0.0122	1.4902	1.3024
B to Z ↓	0.0055	0.0054	0.4581	0.3961
B to Z ↑	0.0130	0.0129	1.4935	1.3058
C to Z ↓	0.0035	0.0035	0.4642	0.4112
C to Z ↑	0.0123	0.0118	1.4933	1.3053
	X37_P4	**X49_P4**	**X37_P4**	**X49_P4**
A to Z ↓	0.0064	0.0064	0.2808	0.2126
A to Z ↑	0.0118	0.0118	0.8746	0.6593
B to Z ↓	0.0056	0.0057	0.2786	0.2111
B to Z ↑	0.0123	0.0123	0.8764	0.6605
C to Z ↓	0.0039	0.0040	0.2824	0.2140
C to Z ↑	0.0120	0.0121	0.8764	0.6611

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	6.579e-05	1.000e-20
X6_P4	1.038e-04	1.000e-20
X9_P4	1.425e-04	1.000e-20
X13_P4	2.104e-04	1.000e-20
X16_P4	2.453e-04	1.000e-20
X19_P4	3.149e-04	1.000e-20
X22_P4	3.498e-04	1.000e-20
X25_P4	4.162e-04	1.000e-20
X37_P4	6.152e-04	1.000e-20

X49_P4	8.176e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	3.650e-05	4.977e-05	9.344e-05	1.204e-04
B (output stable)	4.720e-05	6.545e-05	1.402e-04	1.710e-04
C (output stable)	1.053e-04	1.481e-04	4.379e-04	5.267e-04
A to Z	2.123e-03	2.822e-03	4.446e-03	5.671e-03
B to Z	1.877e-03	2.479e-03	3.943e-03	5.013e-03
C to Z	1.664e-03	2.164e-03	3.224e-03	4.110e-03
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	1.432e-04	1.729e-04	2.067e-04	2.392e-04
B (output stable)	2.114e-04	2.781e-04	3.123e-04	3.807e-04
C (output stable)	5.484e-04	7.193e-04	8.598e-04	1.037e-03
A to Z	7.225e-03	8.639e-03	9.961e-03	1.133e-02
B to Z	6.347e-03	7.655e-03	8.779e-03	1.005e-02
C to Z	5.412e-03	6.310e-03	7.306e-03	8.131e-03
	X37_P4	X49_P4		
A (output stable)	3.477e-04	4.601e-04		
B (output stable)	5.005e-04	6.622e-04		
C (output stable)	1.366e-03	1.789e-03		
A to Z	1.658e-02	2.206e-02		
B to Z	1.452e-02	1.932e-02		
C to Z	1.207e-02	1.605e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

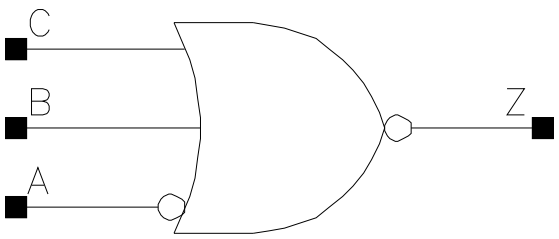
Pin Cycle (vdds)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P4	X49_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.680	0.8160
X13_P4	1.200	1.224	1.4688
X19_P4	1.200	1.496	1.7952
X25_P4	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0009	0.0012	0.0012	0.0022
B	0.0009	0.0019	0.0028	0.0038
C	0.0010	0.0017	0.0026	0.0035

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X13_P4**	**X6_P4**	**X13_P4**
A to Z ↓	0.0186	0.0179	1.5288	0.8434
A to Z ↑	0.0197	0.0196	5.2264	2.5798
B to Z ↓	0.0056	0.0053	1.6280	0.7910
B to Z ↑	0.0131	0.0126	5.2417	2.5888
C to Z ↓	0.0042	0.0033	1.6414	0.8036
C to Z ↑	0.0135	0.0118	5.2507	2.5871
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0203	0.0180	0.5152	0.3915

A to Z ↑	0.0219	0.0199	1.7412	1.3064
B to Z ↓	0.0057	0.0055	0.5476	0.4092
B to Z ↑	0.0126	0.0124	1.7477	1.3115
C to Z ↓	0.0038	0.0035	0.5497	0.4133
C to Z ↑	0.0125	0.0120	1.7490	1.3119

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P4	1.537e-04	1.000e-20
X13_P4	3.400e-04	1.000e-20
X19_P4	4.348e-04	1.000e-20
X25_P4	6.581e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	2.292e-03	4.231e-03	5.049e-03	8.286e-03
B (output stable)	6.653e-05	1.735e-04	2.472e-04	3.384e-04
C (output stable)	1.464e-04	5.356e-04	6.244e-04	9.459e-04
A to Z	4.567e-03	9.040e-03	1.218e-02	1.762e-02
B to Z	2.472e-03	4.995e-03	7.351e-03	9.772e-03
C to Z	2.172e-03	4.101e-03	6.270e-03	8.138e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

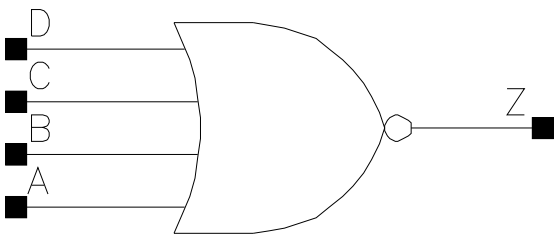
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	1.904	2.2848
X32_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X32_P4
A	0.0007	0.0007	0.0008	0.0010
B	0.0008	0.0008	0.0009	0.0012
C	0.0007	0.0007	0.0009	0.0010
D	0.0007	0.0007	0.0009	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0219	0.0224	1.4957	0.7359
A to Z ↑	0.0309	0.0336	1.9835	0.9860
B to Z ↓	0.0207	0.0214	1.4955	0.7363
B to Z ↑	0.0323	0.0353	1.9854	0.9855
C to Z ↓	0.0215	0.0223	1.4938	0.7358
C to Z ↑	0.0319	0.0348	1.9851	0.9858

D to Z ↓	0.0208	0.0218	1.4943	0.7354
D to Z ↑	0.0334	0.0368	1.9852	0.9869
	X25_P4	**X32_P4**	**X25_P4**	**X32_P4**
A to Z ↓	0.0233	0.0253	0.5104	0.4007
A to Z ↑	0.0332	0.0319	0.6759	0.5105
B to Z ↓	0.0223	0.0242	0.5106	0.4006
B to Z ↑	0.0350	0.0335	0.6757	0.5103
C to Z ↓	0.0226	0.0251	0.5088	0.3995
C to Z ↑	0.0332	0.0326	0.6753	0.5105
D to Z ↓	0.0215	0.0234	0.5091	0.3992
D to Z ↑	0.0349	0.0341	0.6756	0.5098

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	2.980e-04	1.000e-20
X17_P4	5.094e-04	1.000e-20
X25_P4	7.763e-04	1.000e-20
X32_P4	1.041e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	8.676e-04	1.006e-03	1.419e-03	1.781e-03
B (output stable)	8.041e-04	9.396e-04	1.331e-03	1.661e-03
C (output stable)	8.348e-04	9.326e-04	1.412e-03	1.771e-03
D (output stable)	7.648e-04	8.682e-04	1.319e-03	1.650e-03
A to Z	5.767e-03	9.227e-03	1.380e-02	1.740e-02
B to Z	5.596e-03	9.064e-03	1.355e-02	1.711e-02
C to Z	5.823e-03	9.200e-03	1.315e-02	1.682e-02
D to Z	5.627e-03	9.039e-03	1.291e-02	1.647e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

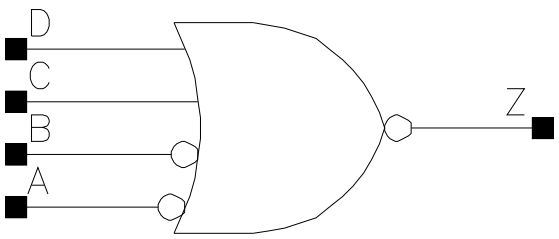
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X13_P4	1.200	1.496	1.7952
X19_P4	1.200	2.040	2.4480
X25_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0011	0.0012	0.0022	0.0021
B	0.0011	0.0016	0.0022	0.0022
C	0.0009	0.0018	0.0027	0.0036
D	0.0009	0.0017	0.0026	0.0034

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X13_P4	X6_P4	X13_P4
A to Z ↓	0.0161	0.0199	1.4844	0.7479
A to Z ↑	0.0197	0.0246	5.0388	2.6338
B to Z ↓	0.0148	0.0189	1.4856	0.7470
B to Z ↑	0.0209	0.0263	5.0387	2.6345
C to Z ↓	0.0060	0.0055	1.6458	0.7930
C to Z ↑	0.0131	0.0131	5.0576	2.6438

D to Z ↓	0.0044	0.0035	1.6515	0.8014
D to Z ↑	0.0133	0.0124	5.0629	2.6422
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0177	0.0193	0.5109	0.3852
A to Z ↑	0.0222	0.0241	1.7433	1.3208
B to Z ↓	0.0159	0.0178	0.5102	0.3842
B to Z ↑	0.0233	0.0254	1.7431	1.3206
C to Z ↓	0.0058	0.0057	0.5480	0.4107
C to Z ↑	0.0126	0.0125	1.7487	1.3246
D to Z ↓	0.0038	0.0036	0.5501	0.4132
D to Z ↑	0.0124	0.0120	1.7495	1.3242

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P4	2.163e-04	1.000e-20
X13_P4	3.039e-04	1.000e-20
X19_P4	5.025e-04	1.000e-20
X25_P4	5.848e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	1.506e-03	2.114e-03	3.460e-03	3.950e-03
B (output stable)	1.408e-03	2.015e-03	3.237e-03	3.759e-03
C (output stable)	7.538e-05	2.069e-04	2.994e-04	3.995e-04
D (output stable)	1.756e-04	5.711e-04	7.200e-04	1.072e-03
A to Z	5.791e-03	9.926e-03	1.528e-02	1.910e-02
B to Z	5.533e-03	9.544e-03	1.444e-02	1.829e-02
C to Z	2.548e-03	5.028e-03	7.301e-03	9.636e-03
D to Z	2.251e-03	4.178e-03	6.275e-03	8.087e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

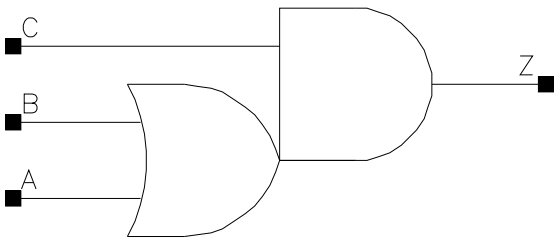
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0010	0.0011	0.0020
B	0.0012	0.0012	0.0023
C	0.0011	0.0012	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0167	0.0196	1.5389	0.7655
A to Z ↑	0.0167	0.0190	2.0048	0.9906
B to Z ↓	0.0179	0.0211	1.5398	0.7658
B to Z ↑	0.0148	0.0173	2.0010	0.9871
C to Z ↓	0.0162	0.0180	1.5246	0.7569
C to Z ↑	0.0148	0.0169	2.0023	0.9878
	X33_P4		**X33_P4**	
A to Z ↓	0.0205		0.3875	
A to Z ↑	0.0206		0.4954	

B to Z ↓	0.0220		0.3875	
B to Z ↑	0.0185		0.4951	
C to Z ↓	0.0185		0.3823	
C to Z ↑	0.0177		0.4951	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	2.838e-04	1.000e-20
X17_P4	4.313e-04	1.000e-20
X33_P4	8.471e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	8.515e-05	8.538e-05	1.791e-04
B (output stable)	1.004e-04	1.013e-04	2.020e-04
C (output stable)	8.145e-05	8.464e-05	1.595e-04
A to Z	4.927e-03	7.816e-03	1.624e-02
B to Z	4.567e-03	7.425e-03	1.550e-02
C to Z	5.282e-03	7.822e-03	1.614e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

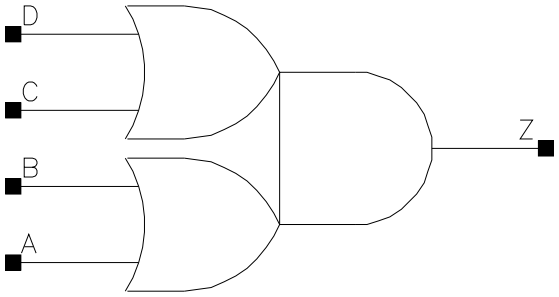
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0011	0.0021
B	0.0008	0.0011	0.0021
C	0.0007	0.0011	0.0021
D	0.0007	0.0011	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0283	0.0245	1.4880	0.7586
A to Z ↑	0.0212	0.0195	1.9621	0.9832
B to Z ↓	0.0303	0.0263	1.4883	0.7587
B to Z ↑	0.0201	0.0183	1.9615	0.9822

C to Z ↓	0.0246	0.0216	1.4783	0.7548
C to Z ↑	0.0214	0.0205	1.9604	0.9822
D to Z ↓	0.0260	0.0230	1.4777	0.7549
D to Z ↑	0.0199	0.0186	1.9575	0.9814
	X33_P4		**X33_P4**	
A to Z ↓	0.0249		0.3893	
A to Z ↑	0.0198		0.4950	
B to Z ↓	0.0261		0.3894	
B to Z ↑	0.0181		0.4940	
C to Z ↓	0.0216		0.3871	
C to Z ↑	0.0203		0.4942	
D to Z ↓	0.0224		0.3869	
D to Z ↑	0.0183		0.4931	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	1.936e-04	1.000e-20
X17_P4	4.229e-04	1.000e-20
X33_P4	8.185e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.839e-05	4.647e-05	1.307e-04
B (output stable)	3.925e-05	6.591e-05	3.037e-04
C (output stable)	7.765e-05	1.063e-04	2.465e-04
D (output stable)	8.964e-05	1.274e-04	4.198e-04
A to Z	5.489e-03	9.493e-03	1.868e-02
B to Z	5.296e-03	9.103e-03	1.769e-02
C to Z	4.927e-03	8.732e-03	1.710e-02
D to Z	4.729e-03	8.325e-03	1.604e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

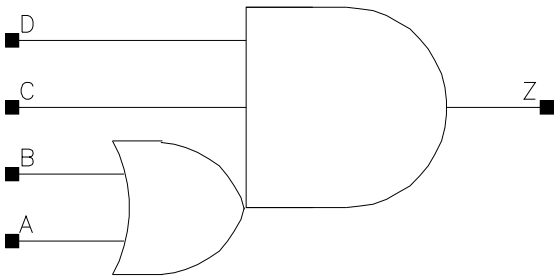
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	1.088	1.3056
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0007	0.0011	0.0018	0.0021
B	0.0007	0.0012	0.0019	0.0022
C	0.0008	0.0011	0.0018	0.0022
D	0.0007	0.0011	0.0018	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0236	0.0223	1.5624	0.7636
A to Z ↑	0.0260	0.0254	2.0308	0.9852
B to Z ↓	0.0253	0.0236	1.5605	0.7630
B to Z ↑	0.0246	0.0232	2.0289	0.9836
C to Z ↓	0.0213	0.0199	1.5370	0.7525

C to Z ↑	0.0226	0.0219	2.0286	0.9836
D to Z ↓	0.0205	0.0191	1.5360	0.7520
D to Z ↑	0.0245	0.0236	2.0286	0.9835
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0233	0.0225	0.5198	0.3891
A to Z ↑	0.0258	0.0267	0.6700	0.5024
B to Z ↓	0.0243	0.0235	0.5197	0.3888
B to Z ↑	0.0235	0.0243	0.6684	0.5008
C to Z ↓	0.0210	0.0202	0.5127	0.3836
C to Z ↑	0.0223	0.0227	0.6687	0.5014
D to Z ↓	0.0198	0.0192	0.5119	0.3829
D to Z ↑	0.0234	0.0240	0.6691	0.5012

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	2.076e-04	1.000e-20
X17_P4	4.548e-04	1.000e-20
X25_P4	6.695e-04	1.000e-20
X33_P4	8.917e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	6.262e-05	1.154e-04	2.002e-04	2.217e-04
B (output stable)	6.598e-05	1.364e-04	2.400e-04	2.642e-04
C (output stable)	2.413e-05	4.785e-05	1.143e-04	1.261e-04
D (output stable)	3.616e-05	6.797e-05	2.146e-04	2.374e-04
A to Z	4.831e-03	9.097e-03	1.423e-02	1.835e-02
B to Z	4.646e-03	8.651e-03	1.340e-02	1.724e-02
C to Z	4.949e-03	9.184e-03	1.470e-02	1.856e-02
D to Z	4.792e-03	8.905e-03	1.400e-02	1.783e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

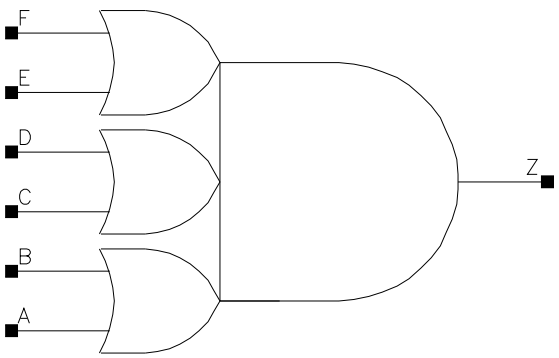
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0008	0.0011	0.0019
B	0.0007	0.0011	0.0021
C	0.0007	0.0011	0.0019
D	0.0007	0.0011	0.0021
E	0.0007	0.0011	0.0019
F	0.0007	0.0011	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0322	0.0281	1.5879	0.7735
A to Z ↑	0.0263	0.0253	2.0163	0.9979
B to Z ↓	0.0342	0.0300	1.5878	0.7735
B to Z ↑	0.0252	0.0243	2.0159	0.9981
C to Z ↓	0.0295	0.0267	1.5788	0.7720
C to Z ↑	0.0276	0.0261	2.0166	0.9977
D to Z ↓	0.0315	0.0285	1.5787	0.7720
D to Z ↑	0.0262	0.0247	2.0148	0.9970
E to Z ↓	0.0257	0.0235	1.5675	0.7678
E to Z ↑	0.0267	0.0258	2.0135	0.9958
F to Z ↓	0.0276	0.0251	1.5681	0.7677
F to Z ↑	0.0253	0.0243	2.0113	0.9952
	X33_P4		X33_P4	
A to Z ↓	0.0284		0.3947	
A to Z ↑	0.0261		0.5029	
B to Z ↓	0.0304		0.3947	
B to Z ↑	0.0241		0.5015	
C to Z ↓	0.0261		0.3925	
C to Z ↑	0.0267		0.5026	
D to Z ↓	0.0279		0.3925	
D to Z ↑	0.0248		0.5010	
E to Z ↓	0.0230		0.3906	
E to Z ↑	0.0266		0.5016	
F to Z ↓	0.0248		0.3905	
F to Z ↑	0.0245		0.5003	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	2.153e-04	1.000e-20
X17_P4	4.849e-04	1.000e-20
X33_P4	9.262e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.688e-05	4.601e-05	8.669e-05
B (output stable)	3.408e-05	6.409e-05	1.155e-04
C (output stable)	4.461e-05	7.231e-05	1.442e-04
D (output stable)	5.387e-05	8.791e-05	1.738e-04
E (output stable)	1.207e-04	1.776e-04	3.341e-04
F (output stable)	1.257e-04	1.893e-04	3.630e-04
A to Z	6.250e-03	1.101e-02	2.177e-02
B to Z	6.045e-03	1.066e-02	2.097e-02
C to Z	5.790e-03	1.041e-02	2.034e-02
D to Z	5.595e-03	1.004e-02	1.953e-02
E to Z	5.240e-03	9.602e-03	1.883e-02
F to Z	5.059e-03	9.239e-03	1.805e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

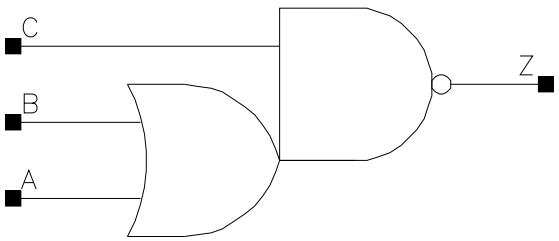
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X34_P4	1.200	2.720	3.2640
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X34_P4	X46_P4
A	0.0009	0.0027	0.0055	0.0072
B	0.0009	0.0025	0.0050	0.0067
C	0.0010	0.0029	0.0059	0.0077

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0092	0.0095	2.7287	0.8909
A to Z ↑	0.0090	0.0094	3.5725	1.2268
B to Z ↓	0.0071	0.0073	2.6734	0.8946
B to Z ↑	0.0099	0.0100	3.5951	1.2345
C to Z ↓	0.0078	0.0078	2.4777	0.8156
C to Z ↑	0.0098	0.0097	2.0448	0.6824
	X34_P4	**X46_P4**	**X34_P4**	**X46_P4**
A to Z ↓	0.0100	0.0100	0.4539	0.3467

A to Z ↑	0.0096	0.0096	0.6125	0.4727
B to Z ↓	0.0077	0.0078	0.4610	0.3536
B to Z ↑	0.0102	0.0103	0.6163	0.4759
C to Z ↓	0.0081	0.0081	0.4183	0.3199
C to Z ↑	0.0099	0.0098	0.3417	0.2620

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P4	1.507e-04	1.000e-20
X17_P4	4.488e-04	1.000e-20
X34_P4	8.878e-04	1.000e-20
X46_P4	1.175e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	7.614e-05	2.582e-04	5.496e-04	6.731e-04
B (output stable)	9.104e-05	3.307e-04	7.456e-04	8.762e-04
C (output stable)	7.451e-05	2.391e-04	5.049e-04	6.292e-04
A to Z	2.468e-03	7.592e-03	1.542e-02	2.013e-02
B to Z	2.149e-03	6.374e-03	1.294e-02	1.691e-02
C to Z	2.949e-03	9.010e-03	1.827e-02	2.385e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

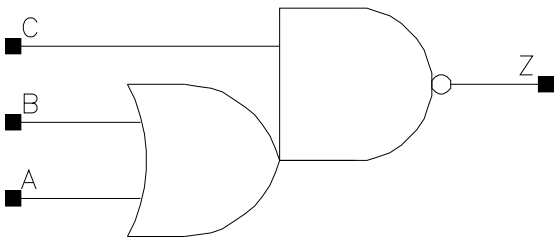
Pin Cycle (vdds)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.544	0.6528
X11_P4	1.200	0.952	1.1424
X17_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X17_P4	X23_P4
A	0.0009	0.0018	0.0028	0.0039
B	0.0009	0.0019	0.0027	0.0035
C	0.0009	0.0019	0.0027	0.0037
	X46_P4			
A	0.0077			
B	0.0071			
C	0.0075			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0082	0.0083	2.7534	1.2845
A to Z ↑	0.0120	0.0120	3.7575	1.7841
B to Z ↓	0.0065	0.0064	2.7082	1.2527

B to Z ↑	0.0131	0.0130	3.7797	1.7951
C to Z ↓	0.0076	0.0077	2.5782	1.1981
C to Z ↑	0.0071	0.0071	2.1978	1.0351
	X17_P4	**X23_P4**	**X17_P4**	**X23_P4**
A to Z ↓	0.0080	0.0085	0.8902	0.6611
A to Z ↑	0.0112	0.0121	1.1831	0.9072
B to Z ↓	0.0062	0.0064	0.8880	0.6622
B to Z ↑	0.0122	0.0128	1.1899	0.9115
C to Z ↓	0.0076	0.0077	0.8400	0.6229
C to Z ↑	0.0064	0.0067	0.6890	0.5252
	X46_P4		**X46_P4**	
A to Z ↓	0.0084		0.3447	
A to Z ↑	0.0118		0.4603	
B to Z ↓	0.0063		0.3418	
B to Z ↑	0.0125		0.4627	
C to Z ↓	0.0079		0.3234	
C to Z ↑	0.0065		0.2662	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.454e-04	1.000e-20
X11_P4	3.089e-04	1.000e-20
X17_P4	4.558e-04	1.000e-20
X23_P4	6.040e-04	1.000e-20
X46_P4	1.182e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	2.977e-05	6.590e-05	9.459e-05	1.690e-04
B (output stable)	3.855e-05	8.847e-05	1.265e-04	3.076e-04
C (output stable)	2.414e-04	5.746e-04	6.939e-04	1.088e-03
A to Z	2.766e-03	5.867e-03	8.427e-03	1.180e-02
B to Z	2.430e-03	5.212e-03	7.344e-03	1.006e-02
C to Z	2.339e-03	5.057e-03	7.214e-03	9.968e-03
	X46_P4			
A (output stable)	3.195e-04			
B (output stable)	5.607e-04			
C (output stable)	1.952e-03			
A to Z	2.296e-02			
B to Z	1.946e-02			
C to Z	1.928e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

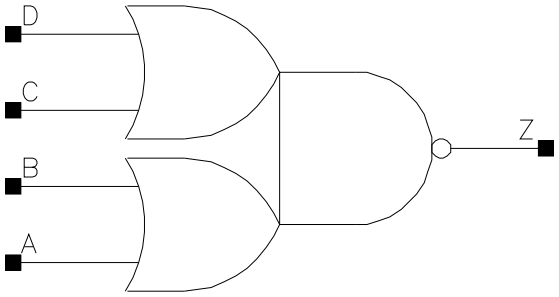
	X46_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0010	0.0019	0.0027	0.0038
B	0.0009	0.0017	0.0025	0.0035
C	0.0009	0.0018	0.0027	0.0037
D	0.0008	0.0017	0.0025	0.0034
	X42_P4			
A	0.0077			
B	0.0071			
C	0.0073			
D	0.0070			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0092	0.0102	2.5368	1.2615
A to Z ↑	0.0144	0.0139	3.9748	1.8280
B to Z ↓	0.0077	0.0082	2.4859	1.2677
B to Z ↑	0.0154	0.0145	3.9898	1.8357
C to Z ↓	0.0092	0.0102	2.5952	1.2792
C to Z ↑	0.0101	0.0102	3.8721	1.8360
D to Z ↓	0.0072	0.0077	2.5259	1.2889
D to Z ↑	0.0110	0.0104	3.8955	1.8473
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0096	0.0098	0.8609	0.6218
A to Z ↑	0.0132	0.0136	1.2313	0.9111
B to Z ↓	0.0079	0.0077	0.8645	0.6223
B to Z ↑	0.0140	0.0143	1.2387	0.9152
C to Z ↓	0.0098	0.0098	0.8758	0.6315
C to Z ↑	0.0095	0.0097	1.2380	0.9132
D to Z ↓	0.0077	0.0076	0.8832	0.6346
D to Z ↑	0.0100	0.0102	1.2474	0.9191
	X42_P4		**X42_P4**	
A to Z ↓	0.0101		0.3262	
A to Z ↑	0.0137		0.4658	
B to Z ↓	0.0081		0.3230	
B to Z ↑	0.0146		0.4680	
C to Z ↓	0.0106		0.3326	
C to Z ↑	0.0099		0.4632	
D to Z ↓	0.0081		0.3296	
D to Z ↑	0.0105		0.4663	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.723e-04	1.000e-20
X10_P4	3.758e-04	1.000e-20
X15_P4	5.523e-04	1.000e-20
X21_P4	7.366e-04	1.000e-20
X42_P4	1.450e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	4.160e-05	1.264e-04	1.629e-04	2.396e-04
B (output stable)	6.104e-05	2.927e-04	2.911e-04	4.756e-04
C (output stable)	8.741e-05	2.323e-04	2.939e-04	4.206e-04
D (output stable)	1.099e-04	3.977e-04	4.220e-04	6.544e-04
A to Z	3.116e-03	6.774e-03	9.631e-03	1.334e-02
B to Z	2.791e-03	5.869e-03	8.318e-03	1.157e-02
C to Z	2.530e-03	5.595e-03	7.927e-03	1.087e-02
D to Z	2.222e-03	4.693e-03	6.685e-03	9.196e-03
	X42_P4			
A (output stable)	4.685e-04			
B (output stable)	9.111e-04			
C (output stable)	8.170e-04			
D (output stable)	1.274e-03			

A to Z	2.645e-02			
B to Z	2.293e-02			
C to Z	2.171e-02			
D to Z	1.839e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

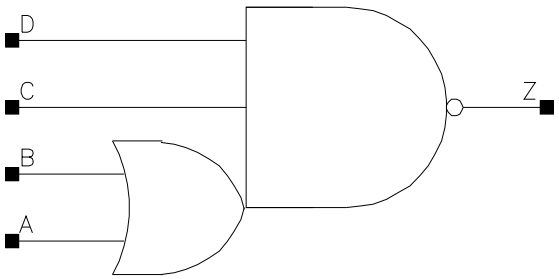
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X21_P4	1.200	2.448	2.9376
X31_P4	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X21_P4	X31_P4
A	0.0009	0.0017	0.0035	0.0052
B	0.0011	0.0016	0.0032	0.0049
C	0.0009	0.0019	0.0039	0.0058
D	0.0009	0.0018	0.0037	0.0054

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0136	0.0133	3.3671	1.8089
A to Z ↑	0.0119	0.0109	3.6033	1.8178
B to Z ↓	0.0117	0.0106	3.4310	1.8201
B to Z ↑	0.0132	0.0111	3.6331	1.8306
C to Z ↓	0.0109	0.0112	3.1823	1.7025

C to Z ↑	0.0119	0.0115	1.9998	1.0093
D to Z ↓	0.0123	0.0118	3.2050	1.7125
D to Z ↑	0.0110	0.0102	2.0300	1.0133
	X21_P4	**X31_P4**	**X21_P4**	**X31_P4**
A to Z ↓	0.0135	0.0138	0.9431	0.6405
A to Z ↑	0.0104	0.0105	0.9088	0.6110
B to Z ↓	0.0108	0.0110	0.9498	0.6474
B to Z ↑	0.0108	0.0108	0.9148	0.6157
C to Z ↓	0.0111	0.0111	0.8888	0.6044
C to Z ↑	0.0112	0.0112	0.5125	0.3468
D to Z ↓	0.0120	0.0122	0.8936	0.6078
D to Z ↑	0.0100	0.0100	0.5137	0.3467

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.303e-04	1.000e-20
X10_P4	2.492e-04	1.000e-20
X21_P4	4.817e-04	1.000e-20
X31_P4	7.144e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	1.158e-04	2.462e-04	4.426e-04	6.510e-04
B (output stable)	1.309e-04	2.801e-04	4.999e-04	7.257e-04
C (output stable)	4.513e-05	1.291e-04	2.461e-04	3.591e-04
D (output stable)	6.598e-05	2.378e-04	4.192e-04	6.004e-04
A to Z	3.063e-03	5.572e-03	1.082e-02	1.610e-02
B to Z	2.617e-03	4.649e-03	9.015e-03	1.342e-02
C to Z	3.715e-03	7.128e-03	1.375e-02	2.040e-02
D to Z	3.407e-03	6.308e-03	1.219e-02	1.812e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

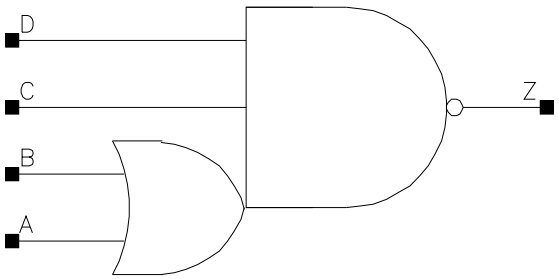
Pin Cycle (vdds)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0010	0.0019	0.0029	0.0038
B	0.0009	0.0018	0.0026	0.0036
C	0.0009	0.0018	0.0028	0.0037
D	0.0009	0.0018	0.0027	0.0036

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0109	0.0119	3.4324	1.7982
A to Z ↑	0.0136	0.0146	3.4744	1.7816
B to Z ↓	0.0092	0.0097	3.3692	1.8029
B to Z ↑	0.0149	0.0153	3.4934	1.7896
C to Z ↓	0.0099	0.0110	3.2445	1.7180

C to Z ↑	0.0089	0.0095	2.0429	1.0338
D to Z ↓	0.0107	0.0114	3.2676	1.7274
D to Z ↑	0.0075	0.0076	2.0611	1.0440
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0116	0.0118	1.2352	0.9339
A to Z ↑	0.0140	0.0144	1.2030	0.9143
B to Z ↓	0.0096	0.0095	1.2303	0.9334
B to Z ↑	0.0149	0.0153	1.2099	0.9186
C to Z ↓	0.0108	0.0110	1.1750	0.8897
C to Z ↑	0.0089	0.0091	0.6906	0.5191
D to Z ↓	0.0112	0.0116	1.1820	0.8943
D to Z ↑	0.0071	0.0074	0.6970	0.5237

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.300e-04	1.000e-20
X10_P4	2.512e-04	1.000e-20
X15_P4	3.640e-04	1.000e-20
X21_P4	4.875e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	2.618e-05	5.786e-05	8.513e-05	1.103e-04
B (output stable)	2.953e-05	9.679e-05	1.196e-04	1.696e-04
C (output stable)	7.511e-05	1.659e-04	2.453e-04	3.255e-04
D (output stable)	1.357e-04	4.464e-04	5.287e-04	7.954e-04
A to Z	3.395e-03	7.095e-03	1.018e-02	1.384e-02
B to Z	3.016e-03	6.121e-03	8.767e-03	1.194e-02
C to Z	2.818e-03	5.887e-03	8.395e-03	1.144e-02
D to Z	2.570e-03	5.237e-03	7.524e-03	1.016e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

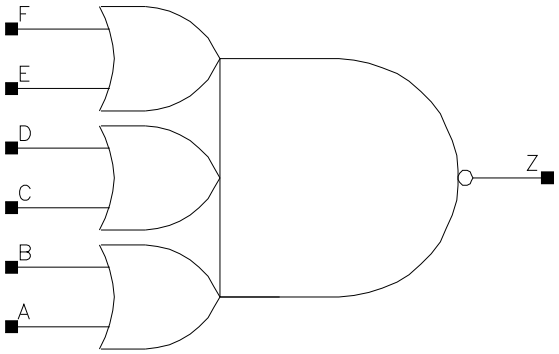
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	1.088	1.3056
X9_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X9_P4
A	0.0008	0.0019
B	0.0008	0.0018
C	0.0008	0.0019
D	0.0007	0.0017
E	0.0008	0.0018
F	0.0008	0.0017

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X9_P4	X3_P4	X9_P4
A to Z ↓	0.0139	0.0154	3.9375	1.6396
A to Z ↑	0.0193	0.0182	4.8348	1.7921
B to Z ↓	0.0127	0.0133	3.9742	1.6441
B to Z ↑	0.0211	0.0192	4.8552	1.7992
C to Z ↓	0.0141	0.0153	3.9842	1.6530
C to Z ↑	0.0166	0.0155	4.8578	1.7900
D to Z ↓	0.0126	0.0131	4.0244	1.6599
D to Z ↑	0.0182	0.0163	4.8825	1.7982
E to Z ↓	0.0131	0.0144	4.0180	1.6592
E to Z ↑	0.0127	0.0118	4.8797	1.7960
F to Z ↓	0.0116	0.0119	4.0657	1.6661
F to Z ↑	0.0140	0.0121	4.9169	1.8075

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	1.437e-04	1.000e-20
X9_P4	4.300e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X9_P4
A (output stable)	3.612e-05	1.229e-04
B (output stable)	4.553e-05	2.303e-04
C (output stable)	6.178e-05	1.769e-04
D (output stable)	7.124e-05	2.873e-04
E (output stable)	1.508e-04	3.825e-04
F (output stable)	1.619e-04	4.845e-04
A to Z	3.546e-03	9.198e-03
B to Z	3.281e-03	8.218e-03
C to Z	2.992e-03	7.785e-03
D to Z	2.745e-03	6.907e-03
E to Z	2.429e-03	6.517e-03
F to Z	2.196e-03	5.605e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

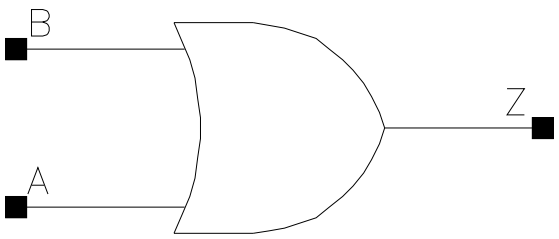
Pin Cycle (vdds)	X3_P4	X9_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X33_P4	1.200	1.360	1.6320
X50_P4	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P4	X16_P4	X33_P4	X50_P4
A	0.0008	0.0010	0.0020	0.0021
B	0.0007	0.0010	0.0021	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0221	0.0196	1.5399	0.7759
A to Z ↑	0.0149	0.0167	1.9707	0.9950
B to Z ↓	0.0235	0.0211	1.5380	0.7757
B to Z ↑	0.0139	0.0154	1.9711	0.9952
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0200	0.0244	0.3835	0.2626
A to Z ↑	0.0166	0.0166	0.4858	0.3290
B to Z ↓	0.0209	0.0256	0.3835	0.2625
B to Z ↑	0.0149	0.0152	0.4849	0.3286

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	1.393e-04	1.000e-20
X16_P4	2.897e-04	1.000e-20
X33_P4	5.794e-04	1.000e-20
X50_P4	7.418e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	2.563e-05	4.793e-05	1.520e-04	1.451e-04
B (output stable)	4.811e-05	8.272e-05	4.224e-04	3.935e-04
A to Z	4.272e-03	7.479e-03	1.547e-02	2.235e-02
B to Z	4.100e-03	7.180e-03	1.450e-02	2.143e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

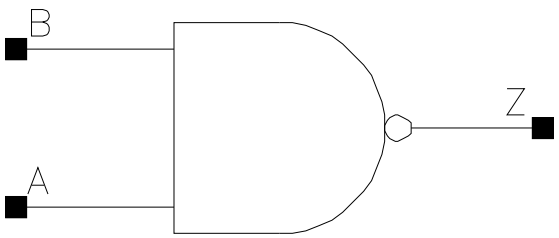
Pin Cycle (vdds)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X16_P4	1.200	0.952	1.1424
X24_P4	1.200	1.088	1.3056
X32_P4	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P4	X16_P4	X24_P4	X32_P4
A	0.0011	0.0011	0.0011	0.0011
B	0.0012	0.0012	0.0012	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0201	0.0210	1.5106	0.7848
A to Z ↑	0.0214	0.0223	2.0096	1.0252
B to Z ↓	0.0217	0.0226	1.5100	0.7838
B to Z ↑	0.0201	0.0205	2.0077	1.0246
	X24_P4	**X32_P4**	**X24_P4**	**X32_P4**
A to Z ↓	0.0233	0.0242	0.5284	0.3945
A to Z ↑	0.0241	0.0244	0.6852	0.5117
B to Z ↓	0.0249	0.0259	0.5283	0.3947
B to Z ↑	0.0223	0.0232	0.6850	0.5118

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	3.576e-04	1.000e-20
X16_P4	4.402e-04	1.000e-20
X24_P4	5.198e-04	1.000e-20
X32_P4	7.403e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	2.823e-05	2.841e-05	2.873e-05	3.055e-05
B (output stable)	5.018e-05	5.086e-05	5.068e-05	5.086e-05
A to Z	7.561e-03	9.032e-03	1.162e-02	1.515e-02
B to Z	7.290e-03	8.776e-03	1.138e-02	1.491e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

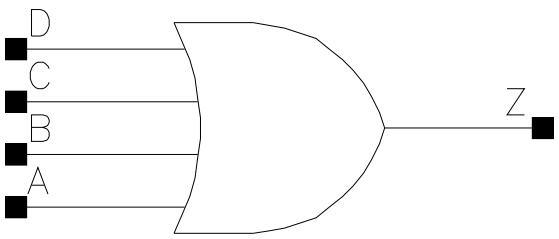
Pin Cycle (vdds)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P4	1.200	2.176	2.6112
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P4	X27_P4
A	0.0018	0.0021
B	0.0017	0.0022
C	0.0018	0.0022
D	0.0017	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P4	X27_P4	X20_P4	X27_P4
A to Z ↓	0.0223	0.0235	0.8643	0.6458
A to Z ↑	0.0166	0.0161	0.6517	0.4858
B to Z ↓	0.0233	0.0244	0.8641	0.6457
B to Z ↑	0.0153	0.0145	0.6511	0.4851
C to Z ↓	0.0220	0.0234	0.8629	0.6445
C to Z ↑	0.0159	0.0158	0.6524	0.4872
D to Z ↓	0.0230	0.0244	0.8624	0.6444
D to Z ↑	0.0146	0.0144	0.6522	0.4862

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X20_P4	4.811e-04	1.000e-20
X27_P4	6.907e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X20_P4	X27_P4
A (output stable)	2.818e-03	3.877e-03
B (output stable)	2.609e-03	3.613e-03
C (output stable)	2.571e-03	3.628e-03
D (output stable)	2.362e-03	3.418e-03
A to Z	1.255e-02	1.748e-02
B to Z	1.185e-02	1.646e-02
C to Z	1.162e-02	1.606e-02
D to Z	1.092e-02	1.517e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

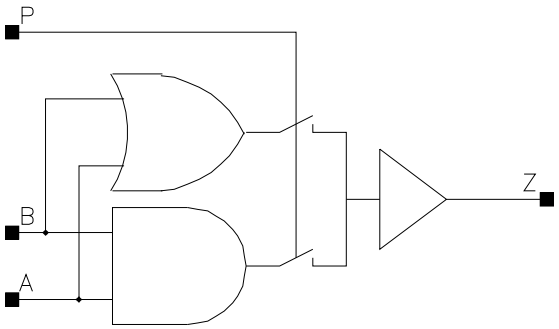
Pin Cycle (vdds)	X20_P4	X27_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X16_P4	1.200	1.224	1.4688
X25_P4	1.200	2.040	2.4480
X33_P4	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0013	0.0020	0.0035	0.0035
B	0.0013	0.0020	0.0040	0.0040
P	0.0007	0.0011	0.0020	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0263	0.0242	1.5623	0.7646
A to Z ↑	0.0195	0.0192	2.0081	1.0033
B to Z ↓	0.0268	0.0250	1.5681	0.7688
B to Z ↑	0.0206	0.0202	2.0085	1.0044
P to Z ↓	0.0258	0.0243	1.5646	0.7664
P to Z ↑	0.0204	0.0201	2.0059	1.0026
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**

A to Z ↓	0.0230	0.0247	0.5198	0.3923
A to Z ↑	0.0188	0.0201	0.6766	0.5059
B to Z ↓	0.0237	0.0252	0.5222	0.3935
B to Z ↑	0.0202	0.0213	0.6770	0.5064
P to Z ↓	0.0235	0.0253	0.5208	0.3923
P to Z ↑	0.0197	0.0209	0.6751	0.5046

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	1.911e-04	1.000e-20
X16_P4	4.239e-04	1.000e-20
X25_P4	7.168e-04	1.000e-20
X33_P4	8.345e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	5.524e-05	9.079e-05	1.978e-04	1.990e-04
B (output stable)	7.394e-05	1.302e-04	3.498e-04	3.510e-04
P (output stable)	2.097e-04	3.629e-04	5.534e-04	5.673e-04
A to Z	4.815e-03	8.811e-03	1.446e-02	1.774e-02
B to Z	4.736e-03	8.755e-03	1.409e-02	1.741e-02
P to Z	4.528e-03	8.443e-03	1.378e-02	1.706e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

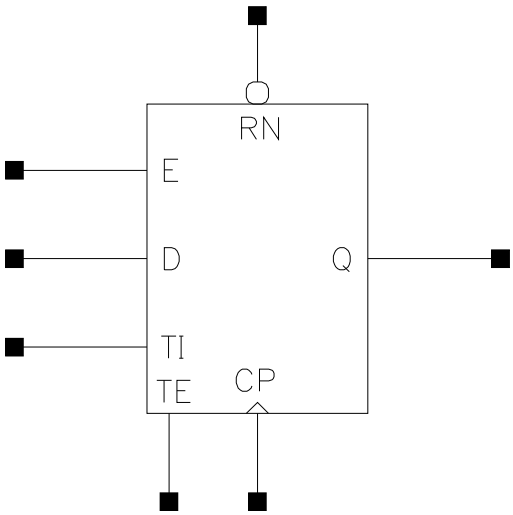
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.488	5.3856
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0012	0.0011
RN	0.0009	0.0007	0.0008	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.0472	0.0277	3.1358	1.5186
CP to Q ↑	0.0429	0.0370	3.9126	1.9887
RN to Q ↓	0.0351	0.0411	2.8930	1.4863
	X17_P4	X33_P4	X17_P4	X33_P4
CP to Q ↓	0.0479	0.0508	0.7470	0.3902
CP to Q ↑	0.0588	0.0620	0.9737	0.4972
RN to Q ↓	0.0563	0.0596	0.7469	0.3901

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0581	0.0399	0.0399	0.0399
CP ↑	min_pulse_width to CP	0.0424	0.0236	0.0224	0.0224
D ↓	hold_rising to CP	-0.0555	-0.0186	-0.0218	-0.0218
D ↑	hold_rising to CP	-0.0403	-0.0067	-0.0067	-0.0067
D ↓	setup_rising to CP	0.0874	0.0543	0.0537	0.0537
D ↑	setup_rising to CP	0.0709	0.0374	0.0374	0.0374
E ↓	hold_rising to CP	-0.0430	-0.0457	-0.0457	-0.0457
E ↑	hold_rising to CP	-0.0354	-0.0074	-0.0074	-0.0074
E ↓	setup_rising to CP	0.0750	0.0752	0.0752	0.0752
E ↑	setup_rising to CP	0.0813	0.0569	0.0569	0.0569
RN ↓	min_pulse_width to RN	0.0447	0.0518	0.0447	0.0447
RN ↑	recovery_rising to CP	0.0129	0.0081	0.0081	0.0081
RN ↑	removal_rising to CP	-0.0082	-0.0008	-0.0007	-0.0007
TE ↓	hold_rising to CP	-0.0266	-0.0116	-0.0116	-0.0116
TE ↑	hold_rising to CP	-0.0240	-0.0110	-0.0136	-0.0136
TE ↓	setup_rising to CP	0.0608	0.0532	0.0532	0.0532
TE ↑	setup_rising to CP	0.1003	0.0710	0.0710	0.0710
TI ↓	hold_rising to CP	-0.0716	-0.0305	-0.0305	-0.0305
TI ↑	hold_rising to CP	-0.0299	-0.0128	-0.0121	-0.0121
TI ↓	setup_rising to CP	0.1007	0.0660	0.0660	0.0660
TI ↑	setup_rising to CP	0.0557	0.0384	0.0384	0.0384

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	5.203e-04	1.000e-20
X8_P4	6.120e-04	1.000e-20
X17_P4	8.132e-04	1.000e-20
X33_P4	1.123e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

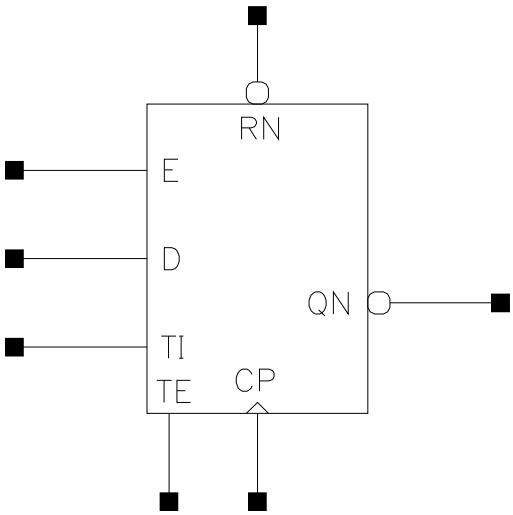
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.314e-02	1.317e-02	1.318e-02	1.318e-02
Clock 100Mhz Data 25Mhz	1.426e-02	1.420e-02	1.518e-02	1.674e-02
Clock 100Mhz Data 50Mhz	1.539e-02	1.522e-02	1.718e-02	2.029e-02
Clock = 0 Data 100Mhz	1.019e-02	9.384e-03	9.119e-03	8.986e-03
Clock = 1 Data 100Mhz	3.094e-03	3.222e-03	3.267e-03	3.288e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.624	5.5488
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0012	0.0012	0.0012
RN	0.0009	0.0009	0.0009	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.0517	0.0492	2.7957	1.4735
CP to QN ↑	0.0533	0.0371	3.8251	1.9262
RN to QN ↑	0.0436	0.0462	3.8247	1.9271
	X17_P4	X33_P4	X17_P4	X33_P4
CP to QN ↓	0.0477	0.0507	0.7475	0.3897
CP to QN ↑	0.0383	0.0420	0.9744	0.4981
RN to QN ↑	0.0507	0.0536	0.9713	0.4967

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0575	0.0399	0.0399	0.0399
CP ↑	min_pulse_width to CP	0.0330	0.0224	0.0237	0.0236
D ↓	hold_rising to CP	-0.0555	-0.0218	-0.0186	-0.0186
D ↑	hold_rising to CP	-0.0403	-0.0067	-0.0067	-0.0067
D ↓	setup_rising to CP	0.0874	0.0537	0.0537	0.0537
D ↑	setup_rising to CP	0.0677	0.0374	0.0374	0.0374
E ↓	hold_rising to CP	-0.0430	-0.0457	-0.0457	-0.0457
E ↑	hold_rising to CP	-0.0354	-0.0074	-0.0074	-0.0074
E ↓	setup_rising to CP	0.0750	0.0752	0.0752	0.0752
E ↑	setup_rising to CP	0.0813	0.0569	0.0569	0.0564
RN ↓	min_pulse_width to RN	0.0398	0.0425	0.0518	0.0566
RN ↑	recovery_rising to CP	0.0129	0.0071	0.0081	0.0081
RN ↑	removal_rising to CP	-0.0082	-0.0029	-0.0007	-0.0007
TE ↓	hold_rising to CP	-0.0261	-0.0116	-0.0116	-0.0120
TE ↑	hold_rising to CP	-0.0240	-0.0136	-0.0110	-0.0110
TE ↓	setup_rising to CP	0.0608	0.0532	0.0532	0.0532
TE ↑	setup_rising to CP	0.1008	0.0710	0.0710	0.0710
TI ↓	hold_rising to CP	-0.0716	-0.0305	-0.0305	-0.0305
TI ↑	hold_rising to CP	-0.0299	-0.0121	-0.0128	-0.0128
TI ↓	setup_rising to CP	0.1007	0.0660	0.0660	0.0660
TI ↑	setup_rising to CP	0.0557	0.0384	0.0384	0.0384

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	5.102e-04	1.000e-20
X8_P4	5.706e-04	1.000e-20
X17_P4	7.457e-04	1.000e-20
X33_P4	9.849e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

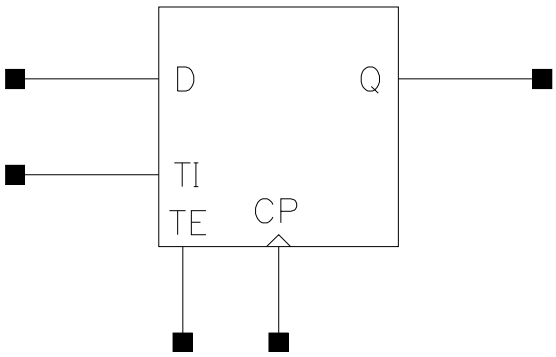
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.313e-02	1.317e-02	1.317e-02	1.317e-02
Clock 100Mhz Data 25Mhz	1.398e-02	1.419e-02	1.518e-02	1.680e-02
Clock 100Mhz Data 50Mhz	1.483e-02	1.521e-02	1.720e-02	2.043e-02
Clock = 0 Data 100Mhz	1.020e-02	9.393e-03	9.126e-03	8.992e-03
Clock = 1 Data 100Mhz	3.091e-03	3.225e-03	3.269e-03	3.291e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.400	4.0800
X8_P4	1.200	3.128	3.7536
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0395	0.0259	2.9938	1.5231
CP to Q ↑	0.0384	0.0338	3.9392	1.9601
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0397	0.0436	0.7373	0.3841
CP to Q ↑	0.0559	0.0595	0.9756	0.4977

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0558	0.0584	0.0584	0.0584
CP ↑	min_pulse_width to CP	0.0330	0.0224	0.0224	0.0224
D ↓	hold_rising to CP	-0.0332	-0.0066	-0.0066	-0.0066
D ↑	hold_rising to CP	-0.0114	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0609	0.0396	0.0396	0.0396
D ↑	setup_rising to CP	0.0363	0.0195	0.0195	0.0195
TE ↓	hold_rising to CP	-0.0213	-0.0023	-0.0049	-0.0023
TE ↑	hold_rising to CP	-0.0159	-0.0071	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0512	0.0359	0.0359	0.0359
TE ↑	setup_rising to CP	0.0901	0.0738	0.0738	0.0738
TI ↓	hold_rising to CP	-0.0673	-0.0410	-0.0410	-0.0410
TI ↑	hold_rising to CP	-0.0195	-0.0077	-0.0077	-0.0092
TI ↓	setup_rising to CP	0.0974	0.0717	0.0717	0.0717
TI ↑	setup_rising to CP	0.0443	0.0342	0.0342	0.0342

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	4.197e-04	1.000e-20
X8_P4	5.145e-04	1.000e-20
X17_P4	7.669e-04	1.000e-20
X33_P4	9.921e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

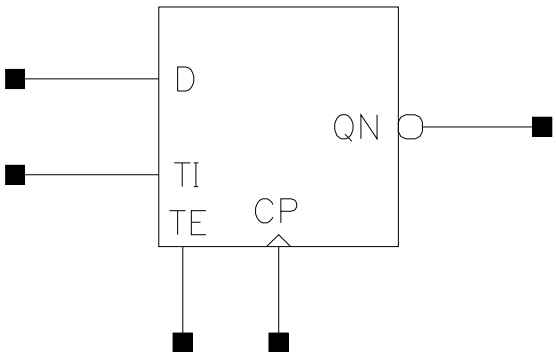
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.204e-02	1.213e-02	1.215e-02	1.216e-02
Clock 100Mhz Data 25Mhz	1.217e-02	1.219e-02	1.324e-02	1.463e-02
Clock 100Mhz Data 50Mhz	1.230e-02	1.225e-02	1.433e-02	1.711e-02
Clock = 0 Data 100Mhz	7.953e-03	7.303e-03	7.091e-03	6.987e-03
Clock = 1 Data 100Mhz	1.788e-03	9.217e-04	6.326e-04	4.877e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.536	4.2432
X8_P4	1.200	3.264	3.9168
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0479	0.0505	3.1833	1.5033
CP to QN ↑	0.0428	0.0344	3.9008	1.9314
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0411	0.0455	0.7380	0.3842
CP to QN ↑	0.0338	0.0377	0.9747	0.4978

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0552	0.0584	0.0584	0.0584
CP ↑	min_pulse_width to CP	0.0271	0.0224	0.0224	0.0224
D ↓	hold_rising to CP	-0.0332	-0.0066	-0.0066	-0.0066
D ↑	hold_rising to CP	-0.0114	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0609	0.0396	0.0396	0.0396
D ↑	setup_rising to CP	0.0358	0.0195	0.0195	0.0195
TE ↓	hold_rising to CP	-0.0208	-0.0023	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0159	-0.0071	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0512	0.0359	0.0359	0.0359
TE ↑	setup_rising to CP	0.0905	0.0738	0.0738	0.0738
TI ↓	hold_rising to CP	-0.0673	-0.0410	-0.0410	-0.0410
TI ↑	hold_rising to CP	-0.0195	-0.0077	-0.0077	-0.0077
TI ↓	setup_rising to CP	0.0958	0.0717	0.0717	0.0717
TI ↑	setup_rising to CP	0.0459	0.0342	0.0342	0.0342

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	4.246e-04	1.000e-20
X8_P4	5.169e-04	1.000e-20
X17_P4	7.605e-04	1.000e-20
X33_P4	9.856e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

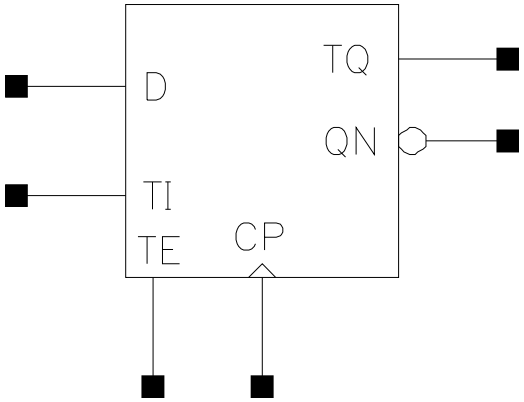
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.194e-02	1.207e-02	1.211e-02	1.213e-02
Clock 100Mhz Data 25Mhz	1.197e-02	1.231e-02	1.318e-02	1.462e-02
Clock 100Mhz Data 50Mhz	1.201e-02	1.254e-02	1.426e-02	1.710e-02
Clock = 0 Data 100Mhz	7.996e-03	7.324e-03	7.104e-03	6.992e-03
Clock = 1 Data 100Mhz	1.777e-03	9.157e-04	6.286e-04	4.852e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.536	4.2432
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0013	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0535	0.0472	2.9021	1.4896
CP to QN ↑	0.0514	0.0353	3.8399	1.9413
CP to TQ ↓	0.0357	0.0234	3.8476	2.7543
CP to TQ ↑	0.0394	0.0335	6.9301	5.0765
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0452	0.0495	0.7515	0.3919
CP to QN ↑	0.0368	0.0400	0.9870	0.5082
CP to TQ ↓	0.0240	0.0249	3.6459	3.6540
CP to TQ ↑	0.0340	0.0350	6.4552	6.8007

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0558	0.0584	0.0584	0.0584
CP ↑	min_pulse_width to CP	0.0318	0.0224	0.0224	0.0224
D ↓	hold_rising to CP	-0.0306	-0.0066	-0.0066	-0.0066
D ↑	hold_rising to CP	-0.0114	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0609	0.0396	0.0396	0.0396
D ↑	setup_rising to CP	0.0363	0.0195	0.0195	0.0195
TE ↓	hold_rising to CP	-0.0213	-0.0023	-0.0023	-0.0023
TE ↑	hold_rising to CP	-0.0159	-0.0071	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0480	0.0359	0.0359	0.0359
TE ↑	setup_rising to CP	0.0905	0.0738	0.0738	0.0738
TI ↓	hold_rising to CP	-0.0676	-0.0367	-0.0367	-0.0370
TI ↑	hold_rising to CP	-0.0195	-0.0077	-0.0077	-0.0077
TI ↓	setup_rising to CP	0.0965	0.0717	0.0717	0.0717
TI ↑	setup_rising to CP	0.0443	0.0342	0.0342	0.0335

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	4.508e-04	1.000e-20
X8_P4	5.706e-04	1.000e-20
X17_P4	7.139e-04	1.000e-20
X33_P4	9.735e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4

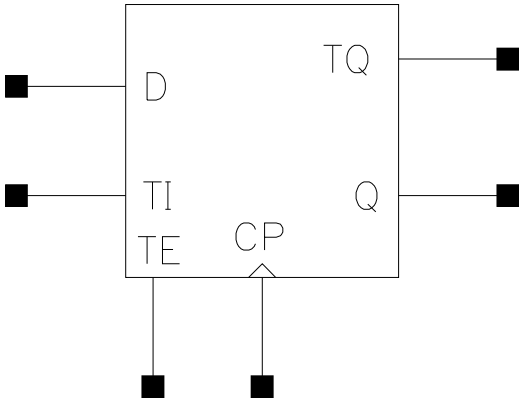
Clock 100Mhz Data 0Mhz	1.219e-02	1.220e-02	1.220e-02	1.221e-02
Clock 100Mhz Data 25Mhz	1.254e-02	1.272e-02	1.330e-02	1.501e-02
Clock 100Mhz Data 50Mhz	1.289e-02	1.324e-02	1.440e-02	1.780e-02
Clock = 0 Data 100Mhz	7.991e-03	7.341e-03	7.124e-03	7.019e-03
Clock = 1 Data 100Mhz	1.788e-03	9.210e-04	6.324e-04	4.881e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.400	4.0800
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008

TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.0521	0.0290	3.1094	1.5088
CP to Q ↑	0.0446	0.0361	3.9808	1.9722
CP to TQ ↓	0.0485	0.0287	3.1081	3.7336
CP to TQ ↑	0.0458	0.0392	5.1371	6.9256
	X17_P4	X33_P4	X17_P4	X33_P4
CP to Q ↓	0.0408	0.0448	0.7569	0.3913
CP to Q ↑	0.0569	0.0605	0.9981	0.5010
CP to TQ ↓	0.0418	0.0459	3.6251	3.6863
CP to TQ ↑	0.0602	0.0653	6.6985	6.7778

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0558	0.0584	0.0584	0.0584
CP ↑	min_pulse_width to CP	0.0458	0.0237	0.0224	0.0224
D ↓	hold_rising to CP	-0.0332	-0.0066	-0.0066	-0.0066
D ↑	hold_rising to CP	-0.0114	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0609	0.0396	0.0396	0.0396
D ↑	setup_rising to CP	0.0363	0.0195	0.0195	0.0195
TE ↓	hold_rising to CP	-0.0213	-0.0023	-0.0049	-0.0049
TE ↑	hold_rising to CP	-0.0159	-0.0071	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0512	0.0359	0.0359	0.0359
TE ↑	setup_rising to CP	0.0901	0.0738	0.0738	0.0738
TI ↓	hold_rising to CP	-0.0673	-0.0370	-0.0410	-0.0410
TI ↑	hold_rising to CP	-0.0195	-0.0077	-0.0092	-0.0092
TI ↓	setup_rising to CP	0.0974	0.0717	0.0717	0.0717
TI ↑	setup_rising to CP	0.0443	0.0342	0.0342	0.0342

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	4.583e-04	1.000e-20
X8_P4	5.370e-04	1.000e-20
X17_P4	7.858e-04	1.000e-20
X33_P4	1.010e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

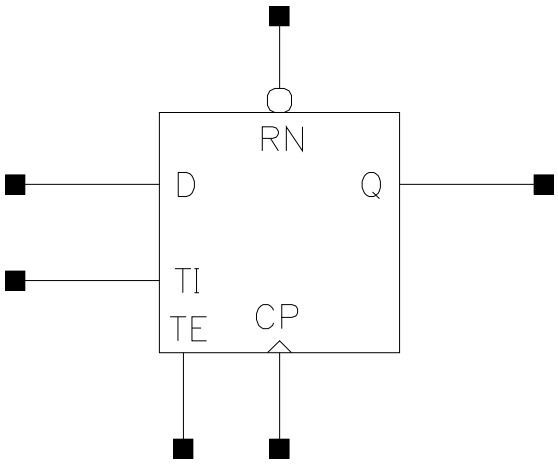
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.200e-02	1.210e-02	1.213e-02	1.215e-02
Clock 100Mhz Data 25Mhz	1.302e-02	1.260e-02	1.353e-02	1.504e-02
Clock 100Mhz Data 50Mhz	1.405e-02	1.311e-02	1.492e-02	1.793e-02
Clock = 0 Data 100Mhz	7.941e-03	7.301e-03	7.094e-03	6.990e-03
Clock = 1 Data 100Mhz	1.775e-03	9.144e-04	6.278e-04	4.841e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.672	4.4064
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
RN	0.0009	0.0007	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0471	0.0276	3.1642	1.5209
CP to Q ↑	0.0426	0.0363	3.9376	1.9875
RN to Q ↓	0.0351	0.0411	2.9028	1.4921
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0414	0.0456	0.7437	0.3890
CP to Q ↑	0.0526	0.0561	0.9709	0.4962
RN to Q ↓	0.0501	0.0543	0.7439	0.3891

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0599	0.0567	0.0582	0.0582
CP ↑	min_pulse_width to CP	0.0424	0.0224	0.0224	0.0224
D ↓	hold_rising to CP	-0.0257	0.0004	0.0004	0.0004
D ↑	hold_rising to CP	-0.0163	0.0025	0.0031	0.0031
D ↓	setup_rising to CP	0.0581	0.0343	0.0343	0.0343
D ↑	setup_rising to CP	0.0439	0.0244	0.0244	0.0244
RN ↓	min_pulse_width to RN	0.0447	0.0496	0.0425	0.0425
RN ↑	recovery_rising to CP	0.0129	0.0075	0.0075	0.0075
RN ↑	removal_rising to CP	-0.0082	-0.0034	-0.0034	-0.0034
TE ↓	hold_rising to CP	-0.0165	0.0022	0.0022	0.0022
TE ↑	hold_rising to CP	-0.0234	-0.0120	-0.0141	-0.0141
TE ↓	setup_rising to CP	0.0532	0.0414	0.0414	0.0414
TE ↑	setup_rising to CP	0.0852	0.0661	0.0661	0.0661
TI ↓	hold_rising to CP	-0.0619	-0.0272	-0.0315	-0.0272
TI ↑	hold_rising to CP	-0.0259	-0.0141	-0.0134	-0.0134
TI ↓	setup_rising to CP	0.0909	0.0659	0.0659	0.0659
TI ↑	setup_rising to CP	0.0548	0.0381	0.0397	0.0397

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	4.860e-04	1.000e-20
X8_P4	5.607e-04	1.000e-20
X17_P4	8.034e-04	1.000e-20
X33_P4	1.074e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.310e-02	1.316e-02	1.322e-02	1.326e-02

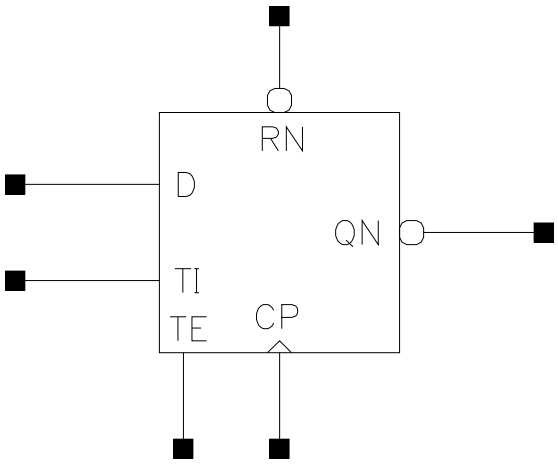
Clock 100Mhz Data 25Mhz	1.343e-02	1.317e-02	1.423e-02	1.567e-02
Clock 100Mhz Data 50Mhz	1.377e-02	1.319e-02	1.524e-02	1.809e-02
Clock = 0 Data 100Mhz	7.741e-03	6.994e-03	6.751e-03	6.629e-03
Clock = 1 Data 100Mhz	1.817e-03	9.371e-04	6.440e-04	4.970e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	3.944	4.7328
X33_P4	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008
RN	0.0009	0.0009	0.0009	0.0009
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0470	0.0442	2.7664	1.4482
CP to QN ↑	0.0486	0.0333	3.8337	1.9170
RN to QN ↑	0.0393	0.0423	3.8235	1.9167
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0445	0.0489	0.7440	0.3883
CP to QN ↑	0.0366	0.0407	0.9814	0.5034
RN to QN ↑	0.0496	0.0533	0.9812	0.5032

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0599	0.0567	0.0567	0.0567
CP ↑	min_pulse_width to CP	0.0318	0.0224	0.0224	0.0237
D ↓	hold_rising to CP	-0.0283	0.0004	0.0004	0.0004
D ↑	hold_rising to CP	-0.0163	0.0031	0.0025	0.0025
D ↓	setup_rising to CP	0.0581	0.0343	0.0343	0.0343
D ↑	setup_rising to CP	0.0439	0.0244	0.0244	0.0244
RN ↓	min_pulse_width to RN	0.0398	0.0425	0.0518	0.0518
RN ↑	recovery_rising to CP	0.0129	0.0103	0.0071	0.0071
RN ↑	removal_rising to CP	-0.0082	-0.0029	-0.0030	-0.0029
TE ↓	hold_rising to CP	-0.0159	0.0022	0.0022	0.0022
TE ↑	hold_rising to CP	-0.0234	-0.0120	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.0532	0.0414	0.0414	0.0414
TE ↑	setup_rising to CP	0.0852	0.0661	0.0661	0.0661
TI ↓	hold_rising to CP	-0.0619	-0.0272	-0.0257	-0.0257
TI ↑	hold_rising to CP	-0.0259	-0.0141	-0.0141	-0.0141
TI ↓	setup_rising to CP	0.0909	0.0659	0.0659	0.0659
TI ↑	setup_rising to CP	0.0548	0.0381	0.0397	0.0397

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	4.804e-04	1.000e-20
X8_P4	5.193e-04	1.000e-20
X17_P4	7.596e-04	1.000e-20
X33_P4	9.369e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.302e-02	1.311e-02	1.314e-02	1.315e-02

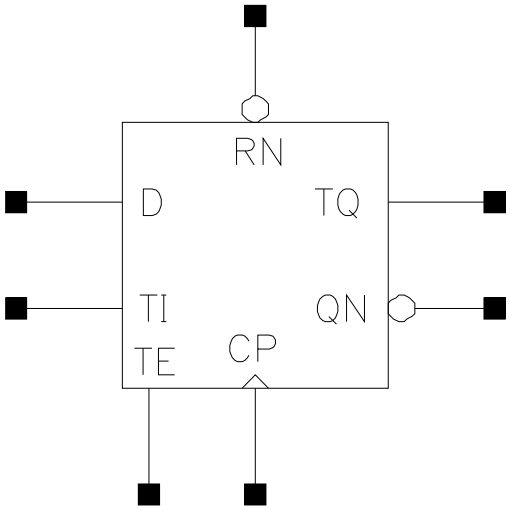
Clock 100Mhz Data 25Mhz	1.299e-02	1.304e-02	1.419e-02	1.564e-02
Clock 100Mhz Data 50Mhz	1.297e-02	1.296e-02	1.523e-02	1.813e-02
Clock = 0 Data 100Mhz	7.738e-03	6.989e-03	6.748e-03	6.627e-03
Clock = 1 Data 100Mhz	1.815e-03	9.363e-04	6.435e-04	4.972e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008

RN	0.0011	0.0008	0.0009	0.0009
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0525	0.0461	2.7688	1.5294
CP to QN ↑	0.0624	0.0369	3.4483	1.9937
CP to TQ ↓	0.0436	0.0247	3.3797	2.8750
CP to TQ ↑	0.0439	0.0363	5.7119	5.3263
RN to QN ↑	0.0457	0.0476	3.4921	1.9852
RN to TQ ↓	0.0338	0.0395	3.0829	2.8222
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0480	0.0524	0.7579	0.3972
CP to QN ↑	0.0377	0.0401	0.9997	0.5055
CP to TQ ↓	0.0256	0.0264	3.5618	3.4865
CP to TQ ↑	0.0362	0.0370	5.0294	5.1085
RN to QN ↑	0.0496	0.0527	0.9963	0.5057
RN to TQ ↓	0.0402	0.0406	3.5109	3.4292

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0599	0.0566	0.0582	0.0583
CP ↑	min_pulse_width to CP	0.0424	0.0224	0.0224	0.0224
D ↓	hold_rising to CP	-0.0257	0.0004	0.0004	0.0004
D ↑	hold_rising to CP	-0.0163	0.0031	0.0031	0.0031
D ↓	setup_rising to CP	0.0581	0.0343	0.0343	0.0343
D ↑	setup_rising to CP	0.0439	0.0244	0.0244	0.0244
RN ↓	min_pulse_width to RN	0.0447	0.0469	0.0496	0.0518
RN ↑	recovery_rising to CP	0.0151	0.0071	0.0071	0.0071
RN ↑	removal_rising to CP	-0.0103	-0.0030	-0.0034	-0.0034
TE ↓	hold_rising to CP	-0.0159	0.0022	0.0022	0.0022
TE ↑	hold_rising to CP	-0.0234	-0.0120	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.0532	0.0414	0.0414	0.0414
TE ↑	setup_rising to CP	0.0852	0.0661	0.0661	0.0661
TI ↓	hold_rising to CP	-0.0619	-0.0272	-0.0257	-0.0257
TI ↑	hold_rising to CP	-0.0259	-0.0141	-0.0141	-0.0141
TI ↓	setup_rising to CP	0.0925	0.0659	0.0659	0.0659
TI ↑	setup_rising to CP	0.0548	0.0381	0.0397	0.0397

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	5.434e-04	1.000e-20
X8_P4	5.543e-04	1.000e-20
X17_P4	6.800e-04	1.000e-20
X33_P4	8.980e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

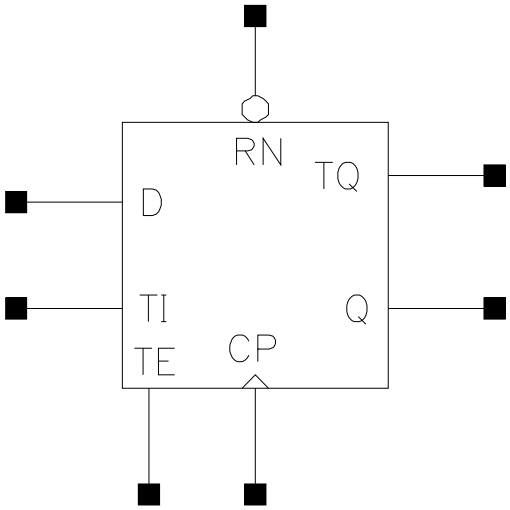
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.301e-02	1.311e-02	1.319e-02	1.323e-02
Clock 100Mhz Data 25Mhz	1.356e-02	1.332e-02	1.408e-02	1.582e-02
Clock 100Mhz Data 50Mhz	1.410e-02	1.354e-02	1.498e-02	1.840e-02
Clock = 0 Data 100Mhz	7.738e-03	6.991e-03	6.743e-03	6.619e-03
Clock = 1 Data 100Mhz	1.816e-03	9.365e-04	6.435e-04	4.971e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0010	0.0008	0.0008	0.0008

RN	0.0009	0.0009	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0531	0.0300	3.3178	1.5580
CP to Q ↑	0.0457	0.0382	4.0964	2.0660
CP to TQ ↓	0.0486	0.0288	4.1807	3.7564
CP to TQ ↑	0.0476	0.0401	7.5281	6.8929
RN to Q ↓	0.0380	0.0431	3.0218	1.5241
RN to TQ ↓	0.0352	0.0423	3.8508	3.6854
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0427	0.0472	0.7520	0.3935
CP to Q ↑	0.0530	0.0568	0.9765	0.4989
CP to TQ ↓	0.0437	0.0488	3.6419	3.7071
CP to TQ ↑	0.0561	0.0620	6.7882	6.8262
RN to Q ↓	0.0510	0.0556	0.7525	0.3935
RN to TQ ↓	0.0520	0.0572	3.6438	3.7047

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0599	0.0567	0.0566	0.0566
CP ↑	min_pulse_width to CP	0.0471	0.0236	0.0224	0.0224
D ↓	hold_rising to CP	-0.0257	0.0004	0.0004	0.0004
D ↑	hold_rising to CP	-0.0163	0.0025	0.0031	0.0031
D ↓	setup_rising to CP	0.0581	0.0343	0.0343	0.0343
D ↑	setup_rising to CP	0.0407	0.0244	0.0244	0.0244
RN ↓	min_pulse_width to RN	0.0496	0.0544	0.0425	0.0425
RN ↑	recovery_rising to CP	0.0129	0.0103	0.0071	0.0071
RN ↑	removal_rising to CP	-0.0056	-0.0029	-0.0030	-0.0030
TE ↓	hold_rising to CP	-0.0165	0.0022	0.0022	0.0022
TE ↑	hold_rising to CP	-0.0234	-0.0120	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.0532	0.0414	0.0414	0.0414
TE ↑	setup_rising to CP	0.0852	0.0661	0.0661	0.0661
TI ↓	hold_rising to CP	-0.0619	-0.0257	-0.0272	-0.0272
TI ↑	hold_rising to CP	-0.0259	-0.0141	-0.0141	-0.0141
TI ↓	setup_rising to CP	0.0909	0.0659	0.0659	0.0659
TI ↑	setup_rising to CP	0.0548	0.0381	0.0381	0.0381

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	5.042e-04	1.000e-20
X8_P4	5.852e-04	1.000e-20
X17_P4	8.194e-04	1.000e-20
X33_P4	1.090e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

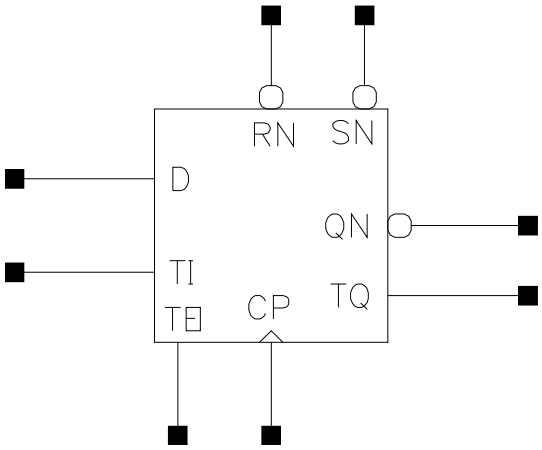
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.308e-02	1.314e-02	1.316e-02	1.317e-02
Clock 100Mhz Data 25Mhz	1.390e-02	1.350e-02	1.442e-02	1.598e-02
Clock 100Mhz Data 50Mhz	1.471e-02	1.386e-02	1.568e-02	1.880e-02
Clock = 0 Data 100Mhz	7.738e-03	6.992e-03	6.743e-03	6.620e-03
Clock = 1 Data 100Mhz	1.817e-03	9.374e-04	6.441e-04	4.973e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.352	5.2224
X17_P4	1.200	4.488	5.3856
X33_P4	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0009

SN	0.0014	0.0014	0.0014
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
CP to QN ↓	0.0513	0.0548	1.4769	0.7569
CP to QN ↑	0.0374	0.0397	1.9295	0.9788
CP to TQ ↓	0.0283	0.0282	4.4661	4.4687
CP to TQ ↑	0.0422	0.0422	8.5929	8.6052
RN to QN ↓	0.0468	0.0508	1.4786	0.7578
RN to QN ↑	0.0431	0.0451	1.9268	0.9788
RN to TQ ↓	0.0347	0.0347	4.4195	4.4240
RN to TQ ↑	0.0369	0.0366	8.6780	8.6932
SN to QN ↓	0.0504	0.0538	1.4772	0.7575
SN to TQ ↑	0.0415	0.0415	8.5814	8.5923
	X33_P4		X33_P4	
CP to QN ↓	0.0632		0.3971	
CP to QN ↑	0.0452		0.5023	
CP to TQ ↓	0.0282		4.4809	
CP to TQ ↑	0.0423		8.6227	
RN to QN ↓	0.0600		0.3968	
RN to QN ↑	0.0502		0.5022	
RN to TQ ↓	0.0348		4.4362	
RN to TQ ↑	0.0366		8.7280	
SN to QN ↓	0.0620		0.3975	
SN to TQ ↑	0.0416		8.6166	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0614	0.0614	0.0613
CP ↑	min_pulse_width to CP	0.0237	0.0237	0.0254
D ↓	hold_rising to CP	-0.0017	-0.0017	-0.0017
D ↑	hold_rising to CP	0.0031	0.0031	0.0031
D ↓	setup_rising to CP	0.0396	0.0396	0.0396
D ↑	setup_rising to CP	0.0244	0.0244	0.0244
RN ↓	min_pulse_width to RN	0.0496	0.0518	0.0544
RN ↑	non_seq_hold_rising to SN	-0.0164	-0.0164	-0.0164
RN ↑	non_seq_setup_rising to SN	0.0425	0.0425	0.0425
RN ↑	recovery_rising to CP	0.0141	0.0141	0.0141
RN ↑	removal_rising to CP	-0.0103	-0.0103	-0.0103
SN ↓	min_pulse_width to SN	0.0452	0.0479	0.0500
SN ↑	recovery_rising to CP	0.0006	0.0006	0.0006
SN ↑	removal_rising to CP	0.0241	0.0241	0.0241

TE ↓	hold_rising to CP	0.0026	0.0026	0.0026
TE ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.0414	0.0414	0.0414
TE ↑	setup_rising to CP	0.0715	0.0710	0.0710
TI ↓	hold_rising to CP	-0.0315	-0.0315	-0.0315
TI ↑	hold_rising to CP	-0.0141	-0.0141	-0.0141
TI ↓	setup_rising to CP	0.0708	0.0708	0.0708
TI ↑	setup_rising to CP	0.0397	0.0397	0.0397

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	6.230e-04	1.000e-20
X17_P4	7.262e-04	1.000e-20
X33_P4	9.233e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

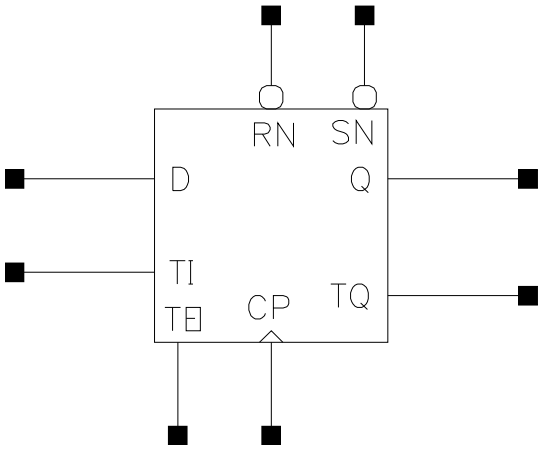
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.379e-02	1.379e-02	1.379e-02
Clock 100Mhz Data 25Mhz	1.381e-02	1.455e-02	1.669e-02
Clock 100Mhz Data 50Mhz	1.384e-02	1.532e-02	1.959e-02
Clock = 0 Data 100Mhz	6.381e-03	6.380e-03	6.381e-03
Clock = 1 Data 100Mhz	5.764e-05	5.743e-05	5.803e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.216	5.0592
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0009

SN	0.0014	0.0014	0.0014
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
CP to Q ↓	0.0324	0.0367	1.5109	0.7803
CP to Q ↑	0.0421	0.0453	1.9812	1.0106
CP to TQ ↓	0.0316	0.0353	4.5321	4.5859
CP to TQ ↑	0.0460	0.0511	8.4739	8.5395
RN to Q ↓	0.0375	0.0400	1.4776	0.7598
RN to Q ↑	0.0433	0.0455	1.9687	1.0008
RN to TQ ↓	0.0370	0.0392	4.4636	4.4945
RN to TQ ↑	0.0467	0.0504	8.4309	8.4932
SN to Q ↑	0.0410	0.0434	1.9706	1.0032
SN to TQ ↑	0.0443	0.0482	8.4470	8.5097
	X33_P4		X33_P4	
CP to Q ↓	0.0467		0.4137	
CP to Q ↑	0.0529		0.5240	
CP to TQ ↓	0.0419		4.7320	
CP to TQ ↑	0.0607		8.6526	
RN to Q ↓	0.0465		0.4000	
RN to Q ↑	0.0511		0.5176	
RN to TQ ↓	0.0433		4.5957	
RN to TQ ↑	0.0572		8.5946	
SN to Q ↑	0.0494		0.5185	
SN to TQ ↑	0.0554		8.6079	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0614	0.0614	0.0614
CP ↑	min_pulse_width to CP	0.0271	0.0283	0.0377
D ↓	hold_rising to CP	0.0004	0.0004	0.0004
D ↑	hold_rising to CP	0.0025	0.0025	0.0025
D ↓	setup_rising to CP	0.0396	0.0396	0.0392
D ↑	setup_rising to CP	0.0244	0.0244	0.0244
RN ↓	min_pulse_width to RN	0.0593	0.0664	0.0881
RN ↑	non_seq_hold_rising to SN	-0.0215	-0.0264	-0.0332
RN ↑	non_seq_setup_rising to SN	0.0402	0.0425	0.0628
RN ↑	recovery_rising to CP	0.0151	0.0146	0.0146
RN ↑	removal_rising to CP	-0.0081	-0.0081	-0.0081
SN ↓	min_pulse_width to SN	0.0500	0.0576	0.0745
SN ↑	recovery_rising to CP	0.0006	0.0006	0.0006
SN ↑	removal_rising to CP	0.0241	0.0241	0.0241

TE ↓	hold_rising to CP	0.0026	0.0026	0.0022
TE ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120
TE ↓	setup_rising to CP	0.0414	0.0414	0.0414
TE ↑	setup_rising to CP	0.0710	0.0710	0.0710
TI ↓	hold_rising to CP	-0.0315	-0.0315	-0.0315
TI ↑	hold_rising to CP	-0.0141	-0.0141	-0.0141
TI ↓	setup_rising to CP	0.0708	0.0708	0.0708
TI ↑	setup_rising to CP	0.0397	0.0397	0.0397

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P4	6.456e-04	1.000e-20
X17_P4	7.759e-04	1.000e-20
X33_P4	1.030e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

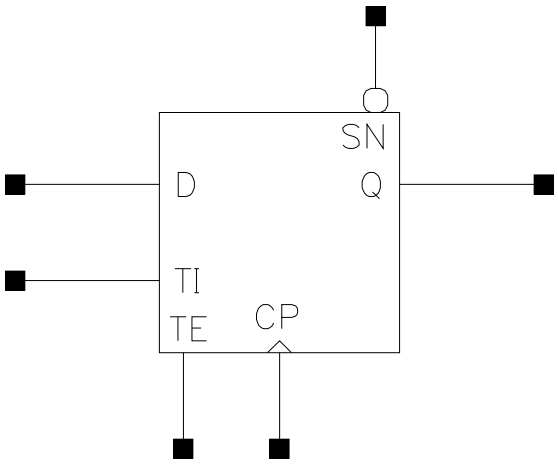
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.377e-02	1.377e-02	1.377e-02
Clock 100Mhz Data 25Mhz	1.393e-02	1.509e-02	1.835e-02
Clock 100Mhz Data 50Mhz	1.409e-02	1.641e-02	2.292e-02
Clock = 0 Data 100Mhz	6.378e-03	6.379e-03	6.379e-03
Clock = 1 Data 100Mhz	5.814e-05	5.818e-05	5.770e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005
SN	0.0015	0.0015	0.0015	0.0015
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0010			
D	0.0005			
SN	0.0015			
TE	0.0011			
TI	0.0004			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.0471	0.0284	3.1676	1.5075
CP to Q ↑	0.0444	0.0383	3.9652	1.9693
SN to Q ↑	0.0294	0.0314	3.8614	1.9523
	X17_P4	X25_P4	X17_P4	X25_P4
CP to Q ↓	0.0405	0.0428	0.7435	0.5139
CP to Q ↑	0.0529	0.0549	0.9700	0.6603
SN to Q ↑	0.0466	0.0486	0.9704	0.6599
	X33_P4		X33_P4	
CP to Q ↓	0.0446		0.3893	
CP to Q ↑	0.0564		0.4968	
SN to Q ↑	0.0500		0.4967	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.0629	0.0636	0.0630	0.0636
CP ↑	min_pulse_width to CP	0.0424	0.0224	0.0207	0.0207
D ↓	hold_rising to CP	-0.0311	-0.0049	-0.0049	-0.0049
D ↑	hold_rising to CP	-0.0142	0.0057	0.0057	0.0057
D ↓	setup_rising to CP	0.0609	0.0392	0.0392	0.0392
D ↑	setup_rising to CP	0.0411	0.0223	0.0223	0.0223
SN ↓	min_pulse_width to SN	0.0354	0.0403	0.0354	0.0354
SN ↑	recovery_rising to CP	0.0006	0.0006	0.0006	0.0006
SN ↑	removal_rising to CP	0.0168	0.0217	0.0217	0.0217
TE ↓	hold_rising to CP	-0.0218	0.0005	0.0005	0.0005
TE ↑	hold_rising to CP	-0.0213	-0.0092	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0511	0.0391	0.0391	0.0391
TE ↑	setup_rising to CP	0.0901	0.0738	0.0738	0.0738
TI ↓	hold_rising to CP	-0.0667	-0.0361	-0.0361	-0.0377
TI ↑	hold_rising to CP	-0.0251	-0.0085	-0.0085	-0.0085
TI ↓	setup_rising to CP	0.0974	0.0717	0.0717	0.0717
TI ↑	setup_rising to CP	0.0492	0.0332	0.0332	0.0332
		X33_P4			

CP ↓	min_pulse_width to CP	0.0630			
CP ↑	min_pulse_width to CP	0.0224			
D ↓	hold_rising to CP	-0.0049			
D ↑	hold_rising to CP	0.0057			
D ↓	setup_rising to CP	0.0392			
D ↑	setup_rising to CP	0.0223			
SN ↓	min_pulse_width to SN	0.0354			
SN ↑	recovery_rising to CP	0.0006			
SN ↑	removal_rising to CP	0.0217			
TE ↓	hold_rising to CP	0.0005			
TE ↑	hold_rising to CP	-0.0092			
TE ↓	setup_rising to CP	0.0391			
TE ↑	setup_rising to CP	0.0738			
TI ↓	hold_rising to CP	-0.0377			
TI ↑	hold_rising to CP	-0.0085			
TI ↓	setup_rising to CP	0.0717			
TI ↑	setup_rising to CP	0.0332			

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	4.563e-04	1.000e-20
X8_P4	5.416e-04	1.000e-20
X17_P4	7.775e-04	1.000e-20
X25_P4	8.663e-04	1.000e-20
X33_P4	9.547e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	1.282e-02	1.309e-02	1.317e-02	1.322e-02
Clock 100Mhz Data 25Mhz	1.321e-02	1.325e-02	1.417e-02	1.488e-02
Clock 100Mhz Data 50Mhz	1.360e-02	1.342e-02	1.516e-02	1.654e-02
Clock = 0 Data 100Mhz	7.348e-03	6.833e-03	6.662e-03	6.577e-03
Clock = 1 Data 100Mhz	1.817e-03	9.371e-04	6.439e-04	4.968e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	1.325e-02			

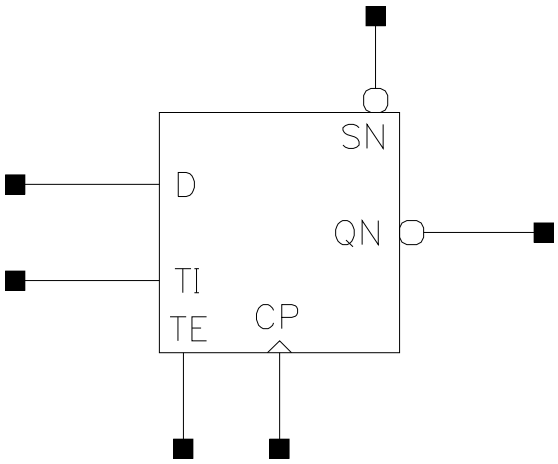
Clock 100Mhz Data 25Mhz	1.562e-02			
Clock 100Mhz Data 50Mhz	1.799e-02			
Clock = 0 Data 100Mhz	6.525e-03			
Clock = 1 Data 100Mhz	4.093e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005
SN	0.0015	0.0015	0.0015	0.0015
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0010			
D	0.0005			
SN	0.0015			
TE	0.0011			
TI	0.0004			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.0488	0.0446	2.7649	1.4511
CP to QN ↑	0.0485	0.0327	3.8173	1.9242
SN to QN ↓	0.0355	0.0384	2.7575	1.4515
	X17_P4	X25_P4	X17_P4	X25_P4
CP to QN ↓	0.0474	0.0501	0.7463	0.5148
CP to QN ↑	0.0383	0.0408	0.9718	0.6602
SN to QN ↓	0.0398	0.0423	0.7445	0.5142
	X33_P4		X33_P4	
CP to QN ↓	0.0524		0.3898	
CP to QN ↑	0.0427		0.4970	
SN to QN ↓	0.0444		0.3898	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.0629	0.0636	0.0636	0.0636
CP ↑	min_pulse_width to CP	0.0318	0.0189	0.0237	0.0237
D ↓	hold_rising to CP	-0.0311	-0.0049	-0.0049	-0.0049
D ↑	hold_rising to CP	-0.0142	0.0057	0.0057	0.0057
D ↓	setup_rising to CP	0.0609	0.0392	0.0392	0.0392
D ↑	setup_rising to CP	0.0411	0.0223	0.0223	0.0223
SN ↓	min_pulse_width to SN	0.0305	0.0354	0.0403	0.0403
SN ↑	recovery_rising to CP	0.0006	0.0006	0.0032	0.0032
SN ↑	removal_rising to CP	0.0168	0.0217	0.0217	0.0217
TE ↓	hold_rising to CP	-0.0218	0.0005	0.0005	0.0005
TE ↑	hold_rising to CP	-0.0213	-0.0092	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0511	0.0391	0.0391	0.0391
TE ↑	setup_rising to CP	0.0901	0.0738	0.0738	0.0738
TI ↓	hold_rising to CP	-0.0667	-0.0377	-0.0361	-0.0361
TI ↑	hold_rising to CP	-0.0251	-0.0085	-0.0085	-0.0085
TI ↓	setup_rising to CP	0.0974	0.0717	0.0757	0.0757
TI ↑	setup_rising to CP	0.0492	0.0332	0.0332	0.0332
		X33_P4			

CP ↓	min_pulse_width to CP	0.0636			
CP ↑	min_pulse_width to CP	0.0237			
D ↓	hold_rising to CP	-0.0049			
D ↑	hold_rising to CP	0.0057			
D ↓	setup_rising to CP	0.0392			
D ↑	setup_rising to CP	0.0223			
SN ↓	min_pulse_width to SN	0.0403			
SN ↑	recovery_rising to CP	0.0032			
SN ↑	removal_rising to CP	0.0217			
TE ↓	hold_rising to CP	0.0005			
TE ↑	hold_rising to CP	-0.0092			
TE ↓	setup_rising to CP	0.0391			
TE ↑	setup_rising to CP	0.0738			
TI ↓	hold_rising to CP	-0.0361			
TI ↑	hold_rising to CP	-0.0085			
TI ↓	setup_rising to CP	0.0757			
TI ↑	setup_rising to CP	0.0332			

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	4.672e-04	1.000e-20
X8_P4	5.837e-04	1.000e-20
X17_P4	8.237e-04	1.000e-20
X25_P4	9.589e-04	1.000e-20
X33_P4	1.094e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	1.282e-02	1.310e-02	1.319e-02	1.323e-02
Clock 100Mhz Data 25Mhz	1.276e-02	1.300e-02	1.445e-02	1.520e-02
Clock 100Mhz Data 50Mhz	1.270e-02	1.291e-02	1.572e-02	1.717e-02
Clock = 0 Data 100Mhz	7.350e-03	6.837e-03	6.665e-03	6.579e-03
Clock = 1 Data 100Mhz	1.816e-03	9.368e-04	6.437e-04	4.974e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	1.326e-02			

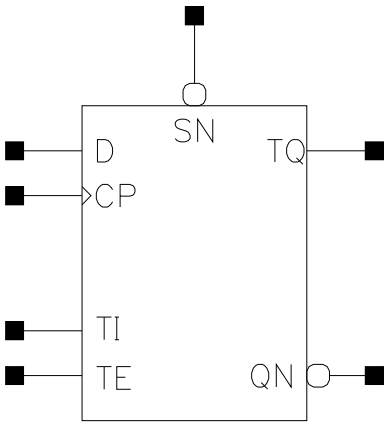
Clock 100Mhz Data 25Mhz	1.599e-02			
Clock 100Mhz Data 50Mhz	1.873e-02			
Clock = 0 Data 100Mhz	6.527e-03			
Clock = 1 Data 100Mhz	4.093e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.216	5.0592
X8_P4	1.200	4.080	4.8960
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005

SN	0.0015	0.0016	0.0016	0.0016
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0560	0.0466	2.7631	1.4606
CP to QN ↑	0.0615	0.0368	3.7734	1.9662
CP to TQ ↓	0.0447	0.0249	3.7818	3.3323
CP to TQ ↑	0.0439	0.0353	5.1293	4.9918
SN to QN ↓	0.0382	0.0398	2.7615	1.4587
SN to TQ ↑	0.0272	0.0282	5.0424	4.9977
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0471	0.0523	0.7680	0.3865
CP to QN ↑	0.0408	0.0458	0.9839	0.5024
CP to TQ ↓	0.0303	0.0303	3.4347	3.4441
CP to TQ ↑	0.0399	0.0399	5.0479	5.0598
SN to QN ↓	0.0415	0.0464	0.7669	0.3859
SN to TQ ↑	0.0343	0.0342	5.0239	5.0395

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0629	0.0636	0.0636	0.0636
CP ↑	min_pulse_width to CP	0.0424	0.0224	0.0237	0.0271
D ↓	hold_rising to CP	-0.0311	-0.0049	-0.0049	-0.0049
D ↑	hold_rising to CP	-0.0142	0.0057	0.0057	0.0057
D ↓	setup_rising to CP	0.0609	0.0392	0.0392	0.0392
D ↑	setup_rising to CP	0.0411	0.0223	0.0223	0.0223
SN ↓	min_pulse_width to SN	0.0283	0.0305	0.0310	0.0310
SN ↑	recovery_rising to CP	0.0005	-0.0027	0.0032	0.0006
SN ↑	removal_rising to CP	0.0168	0.0217	0.0217	0.0217
TE ↓	hold_rising to CP	-0.0218	0.0005	0.0005	0.0005
TE ↑	hold_rising to CP	-0.0213	-0.0092	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0511	0.0391	0.0391	0.0391
TE ↑	setup_rising to CP	0.0901	0.0738	0.0764	0.0764
TI ↓	hold_rising to CP	-0.0667	-0.0361	-0.0361	-0.0361
TI ↑	hold_rising to CP	-0.0251	-0.0085	-0.0085	-0.0085
TI ↓	setup_rising to CP	0.0974	0.0717	0.0757	0.0757
TI ↑	setup_rising to CP	0.0492	0.0332	0.0332	0.0332

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	5.337e-04	1.000e-20
X8_P4	6.493e-04	1.000e-20
X17_P4	8.890e-04	1.000e-20
X33_P4	1.160e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

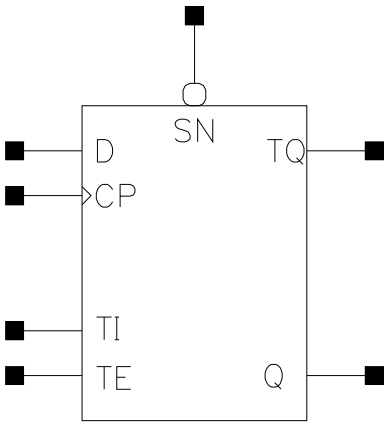
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.283e-02	1.310e-02	1.319e-02	1.323e-02
Clock 100Mhz Data 25Mhz	1.348e-02	1.340e-02	1.479e-02	1.637e-02
Clock 100Mhz Data 50Mhz	1.413e-02	1.370e-02	1.639e-02	1.950e-02
Clock = 0 Data 100Mhz	7.363e-03	6.847e-03	6.675e-03	6.589e-03
Clock = 1 Data 100Mhz	1.817e-03	9.369e-04	6.438e-04	4.967e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.944	4.7328
X17_P4	1.200	4.216	5.0592
X33_P4	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005

SN	0.0016	0.0015	0.0015	0.0015
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0536	0.0307	3.2282	1.5340
CP to Q ↑	0.0473	0.0401	3.9738	1.9980
CP to TQ ↓	0.0533	0.0302	4.6888	3.7757
CP to TQ ↑	0.0463	0.0438	5.1724	6.9697
SN to Q ↑	0.0294	0.0326	3.8652	1.9778
SN to TQ ↑	0.0286	0.0355	5.0612	6.9366
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0414	0.0457	0.7623	0.3957
CP to Q ↑	0.0537	0.0573	0.9769	0.4986
CP to TQ ↓	0.0424	0.0473	3.6429	3.6992
CP to TQ ↑	0.0569	0.0625	6.7964	6.8354
SN to Q ↑	0.0474	0.0510	0.9775	0.4994
SN to TQ ↑	0.0506	0.0562	6.7963	6.8316

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0629	0.0636	0.0636	0.0636
CP ↑	min_pulse_width to CP	0.0471	0.0236	0.0224	0.0224
D ↓	hold_rising to CP	-0.0311	-0.0049	-0.0049	-0.0049
D ↑	hold_rising to CP	-0.0142	0.0057	0.0057	0.0057
D ↓	setup_rising to CP	0.0609	0.0392	0.0392	0.0392
D ↑	setup_rising to CP	0.0411	0.0223	0.0223	0.0223
SN ↓	min_pulse_width to SN	0.0283	0.0403	0.0354	0.0354
SN ↑	recovery_rising to CP	0.0005	0.0032	0.0006	0.0006
SN ↑	removal_rising to CP	0.0168	0.0217	0.0217	0.0217
TE ↓	hold_rising to CP	-0.0218	0.0005	0.0005	0.0005
TE ↑	hold_rising to CP	-0.0213	-0.0092	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0511	0.0391	0.0391	0.0391
TE ↑	setup_rising to CP	0.0901	0.0738	0.0738	0.0738
TI ↓	hold_rising to CP	-0.0667	-0.0361	-0.0377	-0.0361
TI ↑	hold_rising to CP	-0.0251	-0.0085	-0.0085	-0.0085
TI ↓	setup_rising to CP	0.0974	0.0717	0.0717	0.0717
TI ↑	setup_rising to CP	0.0492	0.0332	0.0332	0.0332

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	5.153e-04	1.000e-20
X8_P4	5.616e-04	1.000e-20
X17_P4	7.960e-04	1.000e-20
X33_P4	9.731e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

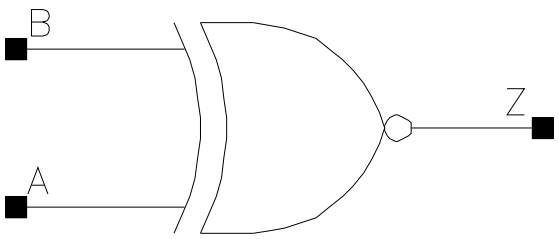
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	1.282e-02	1.309e-02	1.318e-02	1.322e-02
Clock 100Mhz Data 25Mhz	1.381e-02	1.366e-02	1.445e-02	1.604e-02
Clock 100Mhz Data 50Mhz	1.481e-02	1.422e-02	1.573e-02	1.885e-02
Clock = 0 Data 100Mhz	7.363e-03	6.840e-03	6.667e-03	6.581e-03
Clock = 1 Data 100Mhz	1.816e-03	9.369e-04	6.439e-04	4.974e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P4	X8_P4	X17_P4	X25_P4
A	0.0018	0.0007	0.0010	0.0016
B	0.0016	0.0015	0.0019	0.0027
	X33_P4			
A	0.0018			
B	0.0031			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X8_P4**	**X6_P4**	**X8_P4**
A to Z ↓	0.0141	0.0301	2.5602	1.5637
A to Z ↑	0.0141	0.0285	2.9184	2.0383
B to Z ↓	0.0131	0.0210	2.5609	1.5503
B to Z ↑	0.0153	0.0201	2.9273	2.0315
	X17_P4	**X25_P4**	**X17_P4**	**X25_P4**
A to Z ↓	0.0291	0.0295	0.7673	0.5270
A to Z ↑	0.0268	0.0267	1.0010	0.6665

B to Z ↓	0.0219	0.0211	0.7644	0.5254
B to Z ↑	0.0206	0.0197	0.9981	0.6643
	X33_P4		**X33_P4**	
A to Z ↓	0.0283		0.3954	
A to Z ↑	0.0263		0.5015	
B to Z ↓	0.0204		0.3941	
B to Z ↑	0.0198		0.5006	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P4	3.418e-04	1.000e-20
X8_P4	3.736e-04	1.000e-20
X17_P4	6.627e-04	1.000e-20
X25_P4	1.022e-03	1.000e-20
X33_P4	1.448e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	4.449e-03	8.054e-03	1.259e-02	1.963e-02
B to Z	4.325e-03	6.192e-03	1.054e-02	1.609e-02
	X33_P4			
A to Z	2.456e-02			
B to Z	2.074e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

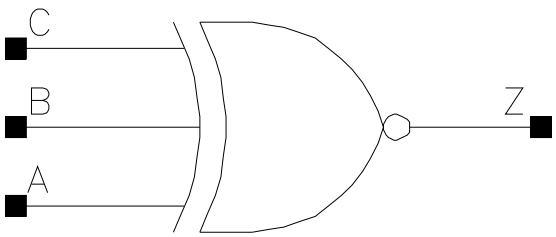
Pin Cycle (vdds)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P4			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	2.176	2.6112
X16_P4	1.200	2.720	3.2640
X25_P4	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X16_P4	X25_P4
A	0.0030	0.0025	0.0031	0.0046
B	0.0033	0.0023	0.0031	0.0042
C	0.0021	0.0007	0.0008	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0207	0.0338	2.9722	1.6386
A to Z ↑	0.0194	0.0317	4.0342	2.0159
B to Z ↓	0.0217	0.0344	2.9762	1.6392
B to Z ↑	0.0202	0.0324	4.0355	2.0161
C to Z ↓	0.0218	0.0463	2.9839	1.6377
C to Z ↑	0.0198	0.0440	4.0416	2.0157
	X16_P4	**X25_P4**	**X16_P4**	**X25_P4**
A to Z ↓	0.0346	0.0350	0.8410	0.5374
A to Z ↑	0.0349	0.0349	1.0557	0.6680
B to Z ↓	0.0354	0.0363	0.8411	0.5379

B to Z ↑	0.0356	0.0362	1.0560	0.6683
C to Z ↓	0.0498	0.0536	0.8408	0.5375
C to Z ↑	0.0494	0.0533	1.0556	0.6679

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	3.339e-04	1.000e-20
X8_P4	3.385e-04	1.000e-20
X16_P4	5.931e-04	1.000e-20
X25_P4	8.594e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	4.290e-03	6.253e-03	1.083e-02	1.674e-02
B to Z	4.388e-03	6.246e-03	1.089e-02	1.691e-02
C to Z	4.362e-03	9.096e-03	1.414e-02	2.163e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

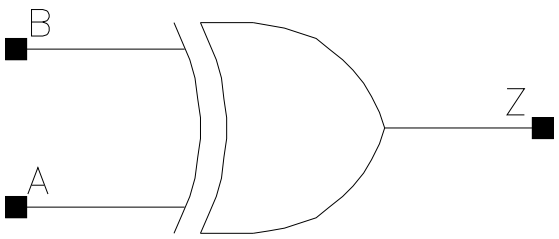
Pin Cycle (vdds)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.224	1.4688
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.224	1.4688
X16_P4	1.200	1.360	1.6320
X25_P4	1.200	2.176	2.6112
X31_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X16_P4
A	0.0008	0.0016	0.0011	0.0012
B	0.0013	0.0015	0.0016	0.0017
	X25_P4	X31_P4		
A	0.0016	0.0021		
B	0.0027	0.0036		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0268	0.0130	2.8072	2.0180
A to Z ↑	0.0265	0.0151	3.7621	3.5974
B to Z ↓	0.0197	0.0143	2.7883	2.0329
B to Z ↑	0.0197	0.0139	3.7575	3.5974
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0246	0.0262	1.5374	0.7924

A to Z ↑	0.0233	0.0251	1.9798	0.9996
B to Z ↓	0.0193	0.0204	1.5307	0.7901
B to Z ↑	0.0184	0.0200	1.9777	0.9988
	X25_P4	**X31_P4**	**X25_P4**	**X31_P4**
A to Z ↓	0.0276	0.0263	0.5241	0.4189
A to Z ↑	0.0260	0.0251	0.6648	0.5358
B to Z ↓	0.0209	0.0196	0.5235	0.4182
B to Z ↑	0.0198	0.0191	0.6641	0.5354

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	2.991e-04	1.000e-20
X6_P4	3.122e-04	1.000e-20
X8_P4	4.875e-04	1.000e-20
X16_P4	7.741e-04	1.000e-20
X25_P4	1.016e-03	1.000e-20
X31_P4	1.455e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	5.886e-03	4.375e-03	7.609e-03	1.183e-02
B to Z	4.927e-03	4.219e-03	6.761e-03	1.053e-02
	X25_P4	X31_P4		
A to Z	1.872e-02	2.330e-02		
B to Z	1.556e-02	1.950e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

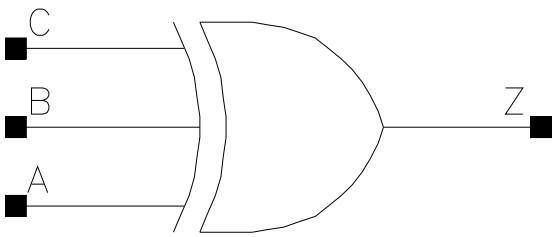
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P4	X31_P4		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X24_P4	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X24_P4
A	0.0026	0.0025	0.0031	0.0055
B	0.0026	0.0023	0.0029	0.0046
C	0.0008	0.0017	0.0023	0.0036

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0210	0.0338	3.1337	1.6377
A to Z ↑	0.0199	0.0317	4.4145	2.0143
B to Z ↓	0.0217	0.0345	3.1383	1.6388
B to Z ↑	0.0205	0.0324	4.4150	2.0150
C to Z ↓	0.0378	0.0341	3.1134	1.6387
C to Z ↑	0.0367	0.0320	4.3975	2.0150
	X17_P4	**X24_P4**	**X17_P4**	**X24_P4**
A to Z ↓	0.0318	0.0373	0.7853	0.5632
A to Z ↑	0.0321	0.0290	0.9843	0.6713
B to Z ↓	0.0324	0.0379	0.7857	0.5634

B to Z ↑	0.0328	0.0295	0.9845	0.6714
C to Z ↓	0.0324	0.0375	0.7861	0.5636
C to Z ↑	0.0328	0.0297	0.9842	0.6712

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	3.623e-04	1.000e-20
X8_P4	2.883e-04	1.000e-20
X17_P4	5.750e-04	1.000e-20
X24_P4	8.676e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	4.113e-03	6.247e-03	1.052e-02	1.746e-02
B to Z	4.185e-03	6.240e-03	1.056e-02	1.751e-02
C to Z	7.868e-03	6.191e-03	1.057e-02	1.753e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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