C28SOI_SC_8_COREPBP4_LL

Release Notes and Known Problems and Solutions

8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 4 nm

1 Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library name	C28SOI_SC_8_COREPBP4_LL
Library version	5.1-02
Library type	Standard Cells
Technology	CMOS028_FDSOI

1.2 Related Documentation

- StandardCell_Notes.pdf Present in Design Package
- User Manual C28SOI_SC_8_COREPBP4_LL_um.pdf present in doc directory of Product itself.
- Datasheets C28SOI_SC_8_COREPBP4_LL_*_ds.pdf present in doc directory of Product itself.

2 Release Details

2.1 Current Release Details, Version 5.1-02

- Verilog Model for below cells have been updated to enable proper checking of E-CP timing checks.

C8T28SOIDV_LL_SDFPHRQNX10_P4	C8T28SOIDV_LL_SDFPHRQNX19_P4
C8T28SOIDV_LL_SDFPHRQNX23_P4	C8T28SOIDV_LL_SDFPHRQNX29_P4
C8T28SOIDV_LL_SDFPHRQNX34_P4	C8T28SOIDV_LL_SDFPHRQNX5_P4
C8T28SOIDV_LL_SDFPHRQX10_P4	C8T28SOIDV_LL_SDFPHRQX19_P4
C8T28SOIDV_LL_SDFPHRQX23_P4	C8T28SOIDV_LL_SDFPHRQX29_P4
C8T28SOIDV_LL_SDFPHRQX34_P4	C8T28SOIDV_LL_SDFPHRQX5_P4

2.2 Version 5.1

- Cells have been re-characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.
- To enable support for Cadence Voltus Flow, CCS-Power has been added.
- Characterization corners have been re-defined in-line with DP Specifications.
- The product is aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.

2.3 Version 5.0

- Dummy Poly in layout across various cells has been cut for DFM robustness.
- Below 38 cells, earlier part of this library now have been moved to another library C28SOI_SC_8_CORESPLPBP4_LL -

C8T28SOIDV_LL_MX41X8_P4	C8T28SOIDV_LL_SDFPRSQNTX10_P4
C8T28SOIDV_LL_SDFPRSQNTX19_P4	C8T28SOIDV_LL_SDFPRSQNTX5_P4
C8T28SOIDV_LL_SDFPRSQNX10_P4	C8T28SOIDV_LL_SDFPRSQNX19_P4
C8T28SOIDV_LL_SDFPRSQNX5_P4	C8T28SOIDV_LL_SDFPRSQTX10_P4
C8T28SOIDV_LL_SDFPRSQTX19_P4	C8T28SOIDV_LL_SDFPRSQTX5_P4
C8T28SOIDV_LL_SDFPRSQX10_P4	C8T28SOIDV_LL_SDFPRSQX19_P4
C8T28SOIDV_LL_SDFPRSQX5_P4	C8T28SOI_LL_AOI211X5_P4
C8T28SOI_LL_AOI21X5_P4	C8T28SOI_LL_AOI22X5_P4
C8T28SOI_LL_AOI31X23_P4	C8T28SOI_LL_AOI31X6_P4
C8T28SOI_LL_BFX34_P4	C8T28SOI_LL_BFX3_P4
C8T28SOI_LL_NAND2AX12_P4	C8T28SOI_LL_NAND2AX15_P4
C8T28SOI_LL_NAND2AX3_P4	C8T28SOI_LL_NAND2AX6_P4
C8T28SOI_LL_NAND2X6_P4	C8T28SOI_LL_NAND3X5_P4
C8T28SOI_LL_NOR2AX12_P4	C8T28SOI_LL_NOR2AX6_P4
C8T28SOI_LL_NOR2X6_P4	C8T28SOI_LL_NOR3X6_P4
C8T28SOI_LL_OAI211X24_P4	C8T28SOI_LL_OAI21X5_P4
C8T28SOI_LL_OAI22X5_P4	C8T28SOI_LL_OAI31X12_P4
C8T28SOI_LL_OAI31X24_P4	C8T28SOI_LL_OAI31X3_P4
C8T28SOI_LL_OAI31X6_P4	C8T28SOI_LL_PAOI2X20_P4

- Total 5 cells have been updated for DFM SEC -LUP and Pin Accessibility . There is no area change for these cells, but there is change in abstract.
  - **Cells Updated for DFM SEC -LUP**
    - C8T28SOIDV_LL_SDFPHRQNX23_P4
    - C8T28SOI_LLHF_SDFPQNX3_P4
    - C8T28SOI_LLHF_SDFPRQTX3_P4
    - C8T28SOI_LL_SDFPSQX5_P4
  - **Cell Updated for Pin Accessibility**
    - C8T28SOIDV_LLS1_FA1X4_P4
- Total 77 cells have been updated for Robustness relative to contact punch through effect. Minimum Enclosure of 20nm for RX/CA has been ensured. There is no change in Cell Area and Abstract because of contact robustness update.
  - Updated cells are -

C8T28SOIDV_LL_DFPQX10_P4	C8T28SOIDV_LL_DFPQX19_P4
C8T28SOIDV_LL_DFPRQX10_P4	C8T28SOIDV_LL_DFPRQX19_P4
C8T28SOIDV_LL_DFPSQX10_P4	C8T28SOIDV_LL_DFPSQX19_P4
C8T28SOIDV_LL_FA1X14_P4	C8T28SOIDV_LL_LDLQX28_P4
C8T28SOIDV_LL_LDLQX9_P4	C8T28SOIDV_LL_LDLRQX19_P4
C8T28SOIDV_LL_NOR2AX14_P4	C8T28SOIDV_LLS1_FA1X9_P4
C8T28SOIDV_LL_SDFPHRQNX10_P4	C8T28SOIDV_LL_SDFPHRQNX19_P4
C8T28SOIDV_LL_SDFPHRQNX29_P4	C8T28SOIDV_LL_SDFPHRQNX34_P4
C8T28SOIDV_LL_SDFPHRQNX5_P4	C8T28SOIDV_LL_SDFPHRQX10_P4
C8T28SOIDV_LL_SDFPHRQX19_P4	C8T28SOIDV_LL_SDFPHRQX23_P4
C8T28SOIDV_LL_SDFPHRQX29_P4	C8T28SOIDV_LL_SDFPHRQX34_P4
C8T28SOIDV_LL_SDFPHRQX5_P4	C8T28SOIDV_LL_SDFPQNTX10_P4
C8T28SOIDV_LL_SDFPQNTX19_P4	C8T28SOIDV_LL_SDFPQNTX29_P4
C8T28SOIDV_LL_SDFPQNTX5_P4	C8T28SOIDV_LL_SDFPQNX19_P4
C8T28SOIDV_LL_SDFPQNX29_P4	C8T28SOIDV_LL_SDFPQNX5_P4
C8T28SOIDV_LL_SDFPQTX10_P4	C8T28SOIDV_LL_SDFPQTX19_P4
C8T28SOIDV_LL_SDFPQTX29_P4	C8T28SOIDV_LL_SDFPQTX5_P4
C8T28SOIDV_LL_SDFPQX10_P4	C8T28SOIDV_LL_SDFPQX19_P4
C8T28SOIDV_LL_SDFPQX23_P4	C8T28SOIDV_LL_SDFPQX29_P4
C8T28SOIDV_LL_SDFPQX5_P4	C8T28SOIDV_LL_SDFPRQNTX10_P4
C8T28SOIDV_LL_SDFPRQNTX19_P4	C8T28SOIDV_LL_SDFPRQNTX29_P4
C8T28SOIDV_LL_SDFPRQNTX5_P4	C8T28SOIDV_LL_SDFPRQNX10_P4
C8T28SOIDV_LL_SDFPRQNX19_P4	C8T28SOIDV_LL_SDFPRQNX29_P4
C8T28SOIDV_LL_SDFPRQNX5_P4	C8T28SOIDV_LL_SDFPRQTX10_P4
C8T28SOIDV_LL_SDFPRQTX19_P4	C8T28SOIDV_LL_SDFPRQTX29_P4
C8T28SOIDV_LL_SDFPRQTX5_P4	C8T28SOIDV_LL_SDFPRQX10_P4
C8T28SOIDV_LL_SDFPRQX19_P4	C8T28SOIDV_LL_SDFPRQX29_P4
C8T28SOIDV_LL_SDFPRQX5_P4	C8T28SOIDV_LL_SDFPSQNTX29_P4
C8T28SOIDV_LL_SDFPSQNX10_P4	C8T28SOIDV_LL_SDFPSQNX14_P4
C8T28SOIDV_LL_SDFPSQNX19_P4	C8T28SOIDV_LL_SDFPSQNX23_P4
C8T28SOIDV_LL_SDFPSQTX19_P4	C8T28SOIDV_LL_SDFPSQTX29_P4
C8T28SOIDV_LL_SDFPSQX10_P4	C8T28SOIDV_LL_SDFPSQX14_P4
C8T28SOIDV_LL_SDFPSQX19_P4	C8T28SOIDV_LL_SDFPSQX29_P4
C8T28SOIDV_LL_XOR3X4_P4	C8T28SOI_LL_AO21X14_P4
C8T28SOI_LL_AO21X19_P4	C8T28SOI_LL_AOI112X20_P4

C8T28SOI_LL_AOI222X7_P4	C8T28SOI_LL_IVX19_P4
C8T28SOI_LL_NAND3ABX12_P4	C8T28SOI_LL_NAND3ABX4_P4
C8T28SOI_LL_NOR2X27_P4	C8T28SOI_LL_OAI12X20_P4
C8T28SOI_LL_OAI211X3_P4	

- Cells has been characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.
- The product has been aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Global Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.4 Version 4.0

- Total 45 cells have been added to further enrich the offer.
  - Addition of Combinational Cells for new functionality and better drive granularity.

C8T28SOIDV_LL_MX41X8_P4	C8T28SOIDV_LL_NAND2AX13_P4
C8T28SOIDV_LL_NOR2AX14_P4	C8T28SOIDV_LL_PAOI2X10_P4
C8T28SOIDV_LL_PAOI2X5_P4	C8T28SOI_LL_AOI211X5_P4
C8T28SOI_LL_AOI21X5_P4	C8T28SOI_LL_AOI22X5_P4
C8T28SOI_LL_AOI31X12_P4	C8T28SOI_LL_AOI31X23_P4
C8T28SOI_LL_AOI31X3_P4	C8T28SOI_LL_AOI31X6_P4
C8T28SOI_LL_BFX34_P4	C8T28SOI_LL_BFX3_P4
C8T28SOI_LL_NAND2AX12_P4	C8T28SOI_LL_NAND2AX15_P4
C8T28SOI_LL_NAND2AX3_P4	C8T28SOI_LL_NAND2AX6_P4
C8T28SOI_LL_NAND2X19_P4	C8T28SOI_LL_NAND2X6_P4
C8T28SOI_LL_NAND3X5_P4	C8T28SOI_LL_NOR2AX12_P4
C8T28SOI_LL_NOR2AX6_P4	C8T28SOI_LL_NOR2X6_P4
C8T28SOI_LL_NOR3X6_P4	C8T28SOI_LL_OAI211X24_P4
C8T28SOI_LL_OAI21X5_P4	C8T28SOI_LL_OAI22X5_P4
C8T28SOI_LL_OAI31X12_P4	C8T28SOI_LL_OAI31X24_P4
C8T28SOI_LL_OAI31X3_P4	C8T28SOI_LL_OAI31X6_P4
C8T28SOI_LL_PAOI2X20_P4	

  - Addition of New Sequential Cells : Set-Reset Flip Flops

C8T28SOIDV_LL_SDFPRSQNTX10_P4	C8T28SOIDV_LL_SDFPRSQNTX19_P4
C8T28SOIDV_LL_SDFPRSQNTX5_P4	C8T28SOIDV_LL_SDFPRSQNX10_P4
C8T28SOIDV_LL_SDFPRSQNX19_P4	C8T28SOIDV_LL_SDFPRSQNX5_P4
C8T28SOIDV_LL_SDFPRSQTX10_P4	C8T28SOIDV_LL_SDFPRSQTX19_P4
C8T28SOIDV_LL_SDFPRSQTX5_P4	C8T28SOIDV_LL_SDFPRSQX10_P4
C8T28SOIDV_LL_SDFPRSQX19_P4	C8T28SOIDV_LL_SDFPRSQX5_P4

- The product has been aligned to DP28FDSOI 2.4 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.5 Version 3.0

- The product has been aligned to DP28FDSOI 2.3 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.6 Version 2.1

- Total 94 cells has been updated to have better manufacturability. Abstract is changed for all these cells. Updated Cells are -

C8T28SOIDV_LL_DFPQX10_P4	C8T28SOIDV_LL_DFPQX19_P4
C8T28SOIDV_LL_DFPRQX10_P4	C8T28SOIDV_LL_DFPRQX19_P4
C8T28SOIDV_LL_LDLRQX9_P4	C8T28SOIDV_LL_PAO2X19_P4
C8T28SOIDV_LLS1_FA1X4_P4	C8T28SOIDV_LL_SDFPHRQNX10_P4
C8T28SOIDV_LL_SDFPHRQNX19_P4	C8T28SOIDV_LL_SDFPHRQNX23_P4
C8T28SOIDV_LL_SDFPHRQNX29_P4	C8T28SOIDV_LL_SDFPHRQNX34_P4
C8T28SOIDV_LL_SDFPHRQNX5_P4	C8T28SOIDV_LL_SDFPHRQX10_P4
C8T28SOIDV_LL_SDFPHRQX19_P4	C8T28SOIDV_LL_SDFPHRQX23_P4
C8T28SOIDV_LL_SDFPHRQX29_P4	C8T28SOIDV_LL_SDFPHRQX34_P4
C8T28SOIDV_LL_SDFPHRQX5_P4	C8T28SOIDV_LL_SDFPQNX19_P4
C8T28SOIDV_LL_SDFPSQTX10_P4	C8T28SOIDV_LL_SDFPSQTX19_P4
C8T28SOIDV_LL_SDFPSQTX29_P4	C8T28SOIDV_LL_SDFPSQX10_P4
C8T28SOIDV_LL_SDFPSQX14_P4	C8T28SOIDV_LL_SDFPSQX19_P4
C8T28SOIDV_LL_SDFPSQX29_P4	C8T28SOIDV_LL_XNOR3X9_P4
C8T28SOI_LL_AND4X3_P4	C8T28SOI_LL_AO12X19_P4
C8T28SOI_LL_AO212X10_P4	C8T28SOI_LL_AO212X19_P4
C8T28SOI_LL_AO212X5_P4	C8T28SOI_LL_AO21X14_P4
C8T28SOI_LL_AO21X19_P4	C8T28SOI_LL_AO222X19_P4
C8T28SOI_LL_AO222X2_P4	C8T28SOI_LL_AO222X5_P4
C8T28SOI_LL_AO22X10_P4	C8T28SOI_LL_AOI112X20_P4
C8T28SOI_LL_AOI12X19_P4	C8T28SOI_LL_AOI12X25_P4
C8T28SOI_LL_AOI211X2_P4	C8T28SOI_LL_AOI21X6_P4
C8T28SOI_LL_CBI4I6X9_P4	C8T28SOI_LLHF_SDFPQNTX3_P4
C8T28SOI_LLHF_SDFPQNX3_P4	C8T28SOI_LLHF_SDFPQTX3_P4

C8T28SOI_LLHF_SDFPQX3_P4	C8T28SOI_LLHF_SDFPRQNTX3_P4
C8T28SOI_LLHF_SDFPRQNX3_P4	C8T28SOI_LLHF_SDFPRQTX3_P4
C8T28SOI_LLHF_SDFPRQX3_P4	C8T28SOI_LLHF_SDFPSQNTX3_P4
C8T28SOI_LLHF_SDFPSQNX3_P4	C8T28SOI_LLHF_SDFPSQTX3_P4
C8T28SOI_LLHF_SDFPSQX3_P4	C8T28SOI_LL_LDHQNX10_P4
C8T28SOI_LL_LDHQX5_P4	C8T28SOI_LL_LDLQX5_P4
C8T28SOI_LL_MUX21X5_P4	C8T28SOI_LL_MUXI21X1_P4
C8T28SOI_LL_NAND2AX2_P4	C8T28SOI_LL_NAND2X15_P4
C8T28SOI_LL_NAND2X24_P4	C8T28SOI_LL_NAND3X10_P4
C8T28SOI_LL_NAND4X10_P4	C8T28SOI_LL_NAND4X18_P4
C8T28SOI_LL_NOR2X16_P4	C8T28SOI_LL_NOR3X14_P4
C8T28SOI_LL_NOR3X21_P4	C8T28SOI_LL_NOR4ABX11_P4
C8T28SOI_LL_NOR4ABX7_P4	C8T28SOI_LL_OA112X10_P4
C8T28SOI_LL_OA112X4_P4	C8T28SOI_LL_OA21X5_P4
C8T28SOI_LL_OAI21X7_P4	C8T28SOI_LL_OAI222X5_P4
C8T28SOI_LL_PAO2X5_P4	C8T28SOI_LL_SDFPQNTX5_P4
C8T28SOI_LL_SDFPQNX5_P4	C8T28SOI_LL_SDFPQTX5_P4
C8T28SOI_LL_SDFPQX5_P4	C8T28SOI_LL_SDFPRQNTX5_P4
C8T28SOI_LL_SDFPRQNX5_P4	C8T28SOI_LL_SDFPRQTX5_P4
C8T28SOI_LL_SDFPRQX5_P4	C8T28SOI_LL_SDFPSQNTX5_P4
C8T28SOI_LL_SDFPSQNX5_P4	C8T28SOI_LL_SDFPSQTX5_P4
C8T28SOI_LL_SDFPSQX5_P4	C8T28SOI_LLS_NOR2X31_P4
C8T28SOI_LL_XNOR2X5_P4	C8T28SOI_LL_XOR2X9_P4

- Out of these total 94 cells, there are 31 cells for which Cell Area is also Impacted. Cells are -

C8T28SOIDV_LL_SDFPSQTX10_P4	C8T28SOIDV_LL_SDFPSQTX29_P4
C8T28SOIDV_LL_SDFPSQX10_P4	C8T28SOIDV_LL_SDFPSQX14_P4
C8T28SOIDV_LL_SDFPSQX19_P4	C8T28SOI_LL_AOI12X25_P4
C8T28SOI_LLHF_SDFPQNTX3_P4	C8T28SOI_LLHF_SDFPQNX3_P4
C8T28SOI_LLHF_SDFPQTX3_P4	C8T28SOI_LLHF_SDFPQX3_P4
C8T28SOI_LLHF_SDFPRQNTX3_P4	C8T28SOI_LLHF_SDFPRQNX3_P4
C8T28SOI_LLHF_SDFPRQTX3_P4	C8T28SOI_LLHF_SDFPRQX3_P4
C8T28SOI_LLHF_SDFPSQNTX3_P4	C8T28SOI_LLHF_SDFPSQNX3_P4
C8T28SOI_LLHF_SDFPSQTX3_P4	C8T28SOI_LLHF_SDFPSQX3_P4
C8T28SOI_LL_LDHQNX10_P4	C8T28SOI_LL_LDHQX5_P4
C8T28SOI_LL_LDLQX5_P4	C8T28SOI_LL_SDFPQNTX5_P4
C8T28SOI_LL_SDFPQNX5_P4	C8T28SOI_LL_SDFPQTX5_P4
C8T28SOI_LL_SDFPQX5_P4	C8T28SOI_LL_SDFPRQNTX5_P4
C8T28SOI_LL_SDFPRQTX5_P4	C8T28SOI_LL_SDFPSQNTX5_P4
C8T28SOI_LL_SDFPSQNX5_P4	C8T28SOI_LL_SDFPSQTX5_P4
C8T28SOI_LL_SDFPSQX5_P4	

- Library has been re-characterized only for these updated 94 cells and all views has been updated accordingly.
- The Product remains aligned to DP28FDSOI_7ML 1.0

2.7 Version 2.0

- The Product is aligned to DP28FDSOI_7ML 1.0. Refer to Design Package Documents for more details.
- For Standard Cell Library Specific Features, Refer to StandardCell_Notes.pdf Present in Design Package.

3 Known Problems and Solutions

3.1 DP related Generic Problems

- For Generic Standard cell Library related problem for this DP, please refer to KPS section inside StandardCell_Notes.pdf Present in Design Package.

3.2 Placement Restriction

➥ Specific Placement restriction due to Poly Landing pad

☞ Placement restriction has been modelled in CADENCE LEF - through “Symmetry property” and in SYNOPSYS FRAM - through “spacing_label property” for the following cells:

- C8T28SOI_LL_IVX2_P4
- C8T28SOI_LL_IVX3_P4
- C8T28SOI_LL_IVX5_P4
- C8T28SOIDV_LL_IVX11_P4

	*As mentioned above, modelling the placement constraint is different between Synopsys and Cadence. Therefore Need to be careful, if You do P&R with Synopsys and then go inside Cadence, the placement created by ICC could be declared as invalid by Encounter tool.*

3.3 Dont_use cells

➥ Specific attributes dont_use in Synopsys Technology File

☞ The “dont_use” attributes are defined in the Synopsys Technology Files for few cells. Reason can be -

a) Cell has some specific custom feature. Therefore We want to ensure that Either these cells are not automatically picked during Synthesis unless the designer wishes to specically use them in the design or those are not replaced during Design Optimization.

b) Cell’s functionality is not properly understood by tools.

Cells with such attributes are as following:

- C8T28SOI_LL_MUXI21X1_P4
- C8T28SOIDV_LLS_XNOR3X1_P4
- C8T28SOIDV_LL_XNOR3X2_P4
- C8T28SOIDV_LLS_XOR3X1_P4
- C8T28SOIDV_LL_XOR3X2_P4

4 Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.

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