C28SOI_SC_8_COREPBP10_LL

User Manual

8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 10 nm

Overview

Features

- The C28SOI_SC_8_COREPBP10_LL Standard Cell library contains 437 cells.

Application

- Design needs in CMOS28FDSOI platform IPs.

Library Architecture

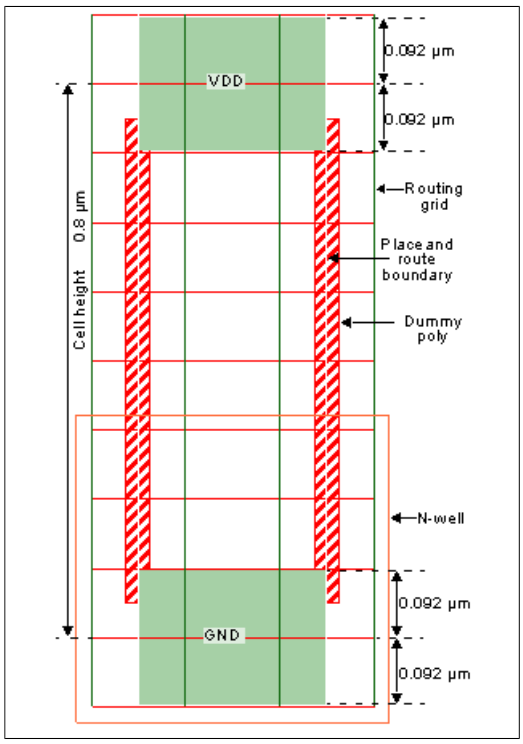
This section illustrates the architecture used for C28SOI_SC_8_COREPBP10_LL Standard Cell library.

Following table shows the Physical Specifications for this library.

Table 1: Physical Specifications

Parameter	Value	Unit
Drawn Gate Length	0.030	µm
Layout Grid	0.001	µm
Vertical Pin Grid	0.1	µm
Horizontal Pin Grid	0.136	µm
Cell Power and Ground Rail Width	0.184	µm

Figure 1: Cell Architecture



1. Quick References

	Refer to the Naming Convention Document available in Design Package for more details regarding cell names.

	Refer to the Standard Cells Reference Manual available in Design Package for more details on library specific information.

2. Functional Specifications

2.1. Cell List

2.1.1. LL(LP Low Vt)

2.1.1.1. Poly Bias With 10 nm

Table 2: Cell List

Cell Name	Drive Strength	Description
C8T28SOIDV_LLS1_FA1	X4, X9, X18	Design optimized for speed, Full-adder having 1 bit input operand, Vdd rail at the bottom of the cell
C8T28SOIDV_LLS1_HA1	X11	Design optimized for speed, Half-adder having 1 bit input operand, Vdd rail at the bottom of the cell
C8T28SOIDV_LLS_XNOR2	X4, X8, X11, X15	Design optimized for speed, 2 input Exclusive NOR, Vdd rail at the bottom of the cell
C8T28SOIDV_LLS_XNOR3	X1, X2, X5, X7	Design optimized for speed, 3 input Exclusive NOR, Vdd rail at the bottom of the cell
C8T28SOIDV_LLS_XOR2	X4, X8, X12, X15	Design optimized for speed, 2 input Exclusive OR, Vdd rail at the bottom of the cell
C8T28SOIDV_LLS_XOR3	X1, X2, X5, X7	Design optimized for speed, 3 input Exclusive OR, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_AND2	X11	2 input AND, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_BF	X11, X23, X34, X46, X68, X91	Buffer, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_DFPQ	X10, X19	Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_DFPRQ	X10, X19	Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_DFPSQ	X10, X19	Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_FA1	X5, X9, X14, X19	Full-adder having 1 bit input operand, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_HA1	X14, X19	Half-adder having 1 bit input operand, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_IV	X11, X23, X34, X46, X68, X91	Inverter, Vdd rail at the bottom of the cell

Cell Name	Drive Strength	Description
C8T28SOIDV_LL_LDHQ	X9, X19, X28	Active High transparent Latch; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_LDLQ	X9, X19, X28	Active Low transparent Latch; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_LDLRQ	X9, X19	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_MUX41	X4, X9, X13, X18	4:1 non-inverting Multiplexer with coded selects, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_MX41	X4, X15	4:1 non-inverting Multiplexer with individual selects, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_NAND2	X9, X18, X27, X36	2 input NAND, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_NAND2A	X9, X13, X17, X27, X36	2 input NAND with A input inverted, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_NOR2	X9, X19, X29, X39, X46, X57	2 input NOR, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_NOR2A	X10, X14, X19, X29, X39	2 input NOR with A input inverted, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_PAO2	X10, X14, X19	2 bit programmable AND/OR logic, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_PAOI2	X5, X10	2 bit programmable NAND/NOR logic, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPHRQ	X5, X10, X19, X23, X29, X34	Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPHRQN	X5, X10, X19, X23, X29, X34	Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPQ	X5, X10, X19, X23, X29	Positive edge triggered Scan D flip-flop; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPQN	X5, X10, X19, X29	Positive edge triggered Scan D flip-flop; having inverted output QN only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPQNT	X5, X10, X19, X29	Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPQT	X5, X10, X19, X29	Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPRQ	X5, X10, X19, X29	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-

Cell Name	Drive Strength	Description
		inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPRQN	X5, X10, X19, X29	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPRQNT	X5, X10, X19, X29	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPRQT	X5, X10, X19, X29	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPSQ	X5, X10, X14, X19, X29	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPSQN	X5, X10, X14, X19, X23, X29	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPSQNT	X5, X10, X19, X23, X29	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_SDFPSQT	X5, X10, X19, X29	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_XNOR3	X2, X4, X9, X13	3 input Exclusive NOR, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_XOR2	X18	2 input Exclusive OR, Vdd rail at the bottom of the cell
C8T28SOIDV_LL_XOR3	X2, X4, X9, X13	3 input Exclusive OR, Vdd rail at the bottom of the cell
C8T28SOI_LLBR0P6_NAND3	X3, X7, X10, X14, X20, X27	Beta ratio optimization 0.6, 3 input NAND
C8T28SOI_LLBR0P8_NAND2	X4, X8, X12, X16	Beta ratio optimization 0.8, 2 input NAND
C8T28SOI_LLHF_SDFPQ	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having non-inverted output Q only
C8T28SOI_LLHF_SDFPQN	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having inverted output QN only
C8T28SOI_LLHF_SDFPQNT	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ
C8T28SOI_LLHF_SDFPQT	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having non-

Cell Name	Drive Strength	Description
		inverted output Q and non-inverted test output TQ
C8T28SOI_LLHF_SDFPRQ	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only
C8T28SOI_LLHF_SDFPRQN	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only
C8T28SOI_LLHF_SDFPRQNT	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ
C8T28SOI_LLHF_SDFPRQT	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ
C8T28SOI_LLHF_SDFPSQ	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only
C8T28SOI_LLHF_SDFPSQN	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only
C8T28SOI_LLHF_SDFPSQNT	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ
C8T28SOI_LLHF_SDFPSQT	X3	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ
C8T28SOI_LLS1_HA1	X5	Design optimized for speed, Half-adder having 1 bit input operand
C8T28SOI_LLS_NAND2	X8, X15, X23, X31	Design optimized for speed, 2 input NAND
C8T28SOI_LLS_NOR2	X20, X24, X31	Design optimized for speed, 2 input NOR
C8T28SOI_LL_AND2	X5, X10, X19, X24, X29	2 input AND
C8T28SOI_LL_AND3	X5, X10, X14, X19	3 input AND
C8T28SOI_LL_AND4	X2, X3, X10, X13	4 input AND
C8T28SOI_LL_AO112	X5, X10, X19	2 input AND into 3 input OR
C8T28SOI_LL_AO12	X5, X10, X19	2 input AND into 2 input OR
C8T28SOI_LL_AO21	X5, X10, X14, X19	2 input AND into 2 input OR
C8T28SOI_LL_AO212	X5, X10, X19	Double 2 input AND into 3 input OR
C8T28SOI_LL_AO22	X5, X10, X14, X19	Double 2 input AND into 2 input OR
C8T28SOI_LL_AO222	X2, X5, X10, X19	Triple 2 input AND into 3 input OR
C8T28SOI_LL_AOI112	X3, X20	2 input AND into 3 input NOR

Cell Name	Drive Strength	Description
C8T28SOI_LL_AOI12	X3, X10, X19, X25	2 input AND into 2 input NOR
C8T28SOI_LL_AOI13	X3, X17, X22	3 input AND into 2 input NOR
C8T28SOI_LL_AOI21	X3, X6, X9, X12, X25	2 input AND into 2 input NOR
C8T28SOI_LL_AOI211	X2, X10, X19	2 input AND into 3 input NOR
C8T28SOI_LL_AOI22	X6, X9, X12, X24	Double 2 input AND into 2 input NOR
C8T28SOI_LL_AOI222	X2, X5, X7, X9	Triple 2 input AND into 3 input NOR
C8T28SOI_LL_AOI31	X3, X12	3 input AND into 2 input NOR
C8T28SOI_LL_BF	X9, X13, X19, X24, X29, X38, X57	Buffer
C8T28SOI_LL_CB4I1	X5, X10, X14, X19	4 input multi stage compound Boolean with non-inverting last stage
C8T28SOI_LL_CBI4I6	X3, X6, X9, X12	4 input multi stage compound Boolean with inverting last stage
C8T28SOI_LL_HA1	X5, X9	Half-adder having 1 bit input operand
C8T28SOI_LL_IV	X5, X10, X14, X19, X29, X34, X38	Inverter
C8T28SOI_LL_LDHQ	X5	Active High transparent Latch; having non-inverted output Q only
C8T28SOI_LL_LDHQN	X10	Active High transparent Latch; having inverted output QN only
C8T28SOI_LL_LDLQ	X5	Active Low transparent Latch; having non-inverted output Q only
C8T28SOI_LL_LDLRQ	X5	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only
C8T28SOI_LL_MUX21	X5, X9, X14, X19	2:1 non-inverting Multiplexer with coded selects
C8T28SOI_LL_MUXI21	X2, X6, X9, X12	2:1 inverting Multiplexer with coded selects
C8T28SOI_LL_NAND2	X4, X8, X12, X15, X19, X24	2 input NAND
C8T28SOI_LL_NAND2A	X4, X23, X31	2 input NAND with A input inverted
C8T28SOI_LL_NAND3	X3, X7, X10, X14, X20, X27	3 input NAND
C8T28SOI_LL_NAND3A	X3, X7, X10, X14	3 input NAND with A input inverted
C8T28SOI_LL_NAND3AB	X4, X8, X12, X15	3 input NAND with A and B inputs inverted
C8T28SOI_LL_NAND4	X5, X10, X14, X18	4 input NAND
C8T28SOI_LL_NAND4AB	X3, X7, X10, X14	4 input NAND with A and B inputs inverted
C8T28SOI_LL_NOR2	X4, X8, X12, X16, X23, X27, X34, X38	2 input NOR
C8T28SOI_LL_NOR2A	X2, X3, X4	2 input NOR with A input inverted
C8T28SOI_LL_NOR3	X3, X7, X11, X14, X21, X29	3 input NOR
C8T28SOI_LL_NOR3A	X3, X7, X11, X14	3 input NOR with A input inverted
C8T28SOI_LL_NOR4	X5, X10, X14, X18	4 input NOR
C8T28SOI_LL_NOR4AB	X4, X7, X11, X14	4 input NOR with A and B inputs inverted

Cell Name	Drive Strength	Description
C8T28SOI_LL_OA112	X4, X10, X14, X19	2 input OR into 3 input AND
C8T28SOI_LL_OA12	X5, X10, X19	2 input OR into 2 input AND
C8T28SOI_LL_OA21	X5, X10, X14, X19	2 input OR into 2 input AND
C8T28SOI_LL_OA22	X5, X10, X14, X19	Double 2 input OR into 2 input AND
C8T28SOI_LL_OA222	X4, X9, X19	Triple 2 input OR into 3 input AND
C8T28SOI_LL_OAI112	X3, X6, X12, X18	2 input OR into 3 input NAND
C8T28SOI_LL_OAI12	X3, X10, X20, X26	2 input OR into 2 input NAND
C8T28SOI_LL_OAI21	X3, X7, X10, X13, X26	2 input OR into 2 input NAND
C8T28SOI_LL_OAI211	X3, X6, X9, X12	2 input OR into 3 input NAND
C8T28SOI_LL_OAI22	X3, X6, X8, X11, X24	Double 2 input OR into 2 input NAND
C8T28SOI_LL_OAI222	X2, X3, X5, X8, X10	Triple 2 input OR into 3 input NAND
C8T28SOI_LL_OR2	X5, X9, X19, X29	2 input OR
C8T28SOI_LL_OR2AB	X5, X9, X14, X18	2 input OR with A and B inputs inverted
C8T28SOI_LL_OR3	X5, X10, X14, X19	3 input OR
C8T28SOI_LL_OR4	X4, X8, X12, X15	4 input OR
C8T28SOI_LL_PAO2	X5	2 bit programmable AND/OR logic
C8T28SOI_LL_SDFPQ	X5	Positive edge triggered Scan D flip-flop; having non-inverted output Q only
C8T28SOI_LL_SDFPQN	X5	Positive edge triggered Scan D flip-flop; having inverted output QN only
C8T28SOI_LL_SDFPQNT	X5	Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ
C8T28SOI_LL_SDFPQT	X5	Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ
C8T28SOI_LL_SDFPRQ	X5	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only
C8T28SOI_LL_SDFPRQN	X5	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only
C8T28SOI_LL_SDFPRQNT	X5	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ
C8T28SOI_LL_SDFPRQT	X5	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ
C8T28SOI_LL_SDFPSQ	X5	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only
C8T28SOI_LL_SDFPSQN	X5	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Cell Name	Drive Strength	Description
C8T28SOI_LL_SDFPSQNT	X5	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ
C8T28SOI_LL_SDFPSQT	X5	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ
C8T28SOI_LL_XNOR2	X5, X9, X14, X19	2 input Exclusive NOR
C8T28SOI_LL_XOR2	X2, X5, X9, X13, X17	2 input Exclusive OR

3. Contact Information

ST users, login to **HELPDESK** (http://col2.cro.st.com/helpdesk) for submitting queries or support requests.
Non-ST users, contact Customer Support personnel.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.