Release Notes

Product Release Information

Parameter	Description
Product name	PDK_STM_cmos28FDSOI_RF_mmW_6U1x_2T8x_LB
Product version	1.2
Product type	Process Design Kit
Technology	CMOS028_FDSOI

Impact of Product Release

- DRC / LVS Signoff verification to be re-analysed

Related documentation

- CMOS028FDSOI DESIGN RULES MANUAL REV 0.4.8 (DMS 8343474)
- CMOS028FDSOI DEVICES MATURITY TABLE (DMS 8384858)
- CMOS028FDSOI RF DEVICES MATURITY TABLE (DMS DM00388106)

Sealring management

- A dedicated documentation is available in *$DKITROOT/doc/MANUALS/DESIGN_FINISHING/SEALRING* directory
- Please refer to the Design Rules Manual regarding the placement of the sealring around the Chip

- **Tools**

TOOL	VERSION
ESDCheckKit	3.1-01
ERC_MGC_KIT	3.0-01
ic	06.17.721
ams	2018.3_1
spectre	17.10.307
hspice	n-2017.12-sp1
afs	2018.3_1
ads	2017_update1.0
goldengate	2017-update-0.1
customsim	o-2018.09
xcelium	18.03.009
calibre	2018.2_24.18
pvs	16.12.000
star-rcxt	n-2017.12-sp3-1
ext	17.21.000
mvs	17.10.000
totem	19.0.2p4
emx	5.0

- **Supported Operating System:**

This Design Kit is qualified to work with OS:

- Redhat 6.0 64bits version

• Changes with respect to all Previous Versions

○ Changes in Version 1.2 Production released on 10-19-2018 versus Version 1.1 Production released on 07-27-2018

- ST packages references

MODEL	UPT DELIVERABLE
Front-End	Models_C028FDSOI_RF_mmW 1.2-01
Back-End	PEX_models_28FDSOI 2.4-00

BITCELL NAME	RELEASE	UPT DELIVERABLE
memcell_sp0126_SW_28SOI	1.1	memcell_sp0126_SW_28SOI@1.1-PRELIM-02
memcell_sp0120_LL_28	1.3	memcell_sp0120_LL_28@1.3@20110905.0
memcell_sp0120_SW_LL_28SOI	1.0	memcell_sp0120_SW_LL_28SOI@1.0@20130123.1
memcell_sp0152_SW_28SOI	1.0	memcell_sp0152_SW_28SOI@1.0@20140129.1
memcell_rf0251_BB_28SOI	1.0	memcell_rf0251_BB_28SOI@1.0@20141022.1
memcell_dp0316_SW_28SOI	1.0	memcell_dp0316_SW_28SOI@1.0@20140217.0
memcell_dp0316_SW_28SOI	1.1	memcell_dp0316_SW_28SOI@1.1@20140515.1
memcell_cam0711_LVT_28SOI	1.0	memcell_cam0711_LVT_28SOI@1.0@20131008.2
memcell_rom0110_LVT_28SOI	1.2	memcell_rom0110_LVT_28SOI@1.2@20140929.0
memcell_otp2P4_28SOI_EG	1.0	memcell_otp2P4_28SOI_EG@1.0@20120524.0
memcell_otp0P95_28SOI	1.0	memcell_otp0P95_28SOI@1.0@20141024.0

- General changes:
  - Introduction of Sealring with Crack-Sensor
    - Support of new pcells and devices in Virtuoso Library, category *LayoutFinishing*:
      - *rcs_6U1x_2U2x_2T8x_LB*
      - *rcs_6U1x_2T8x_LB*
      - *sealringCS_6U1x_2U2x_2T8x_LB*
      - *sealringCS_6U1x_2T8x_LB*
    - Addition of related DRC rules, layers and LVS extraction
    - Please refer to the dedicated documentation in *$DKITROOT/doc/MANUALS/DESIGN_FINISHING/SEALRING/SealringCS_28FD_AN.pdf*

- Simulation changes:
  - SG varactor MAT30 model:
    - Improvement of temperature behavior (leakage, capacitance)
    - Corners calibration
  - EG varactor model: poly resistance adjustment vs DRM values
  - ESD Diodes model: Add option and default behavior of (back-end) instance parameter + SOA

- ESD ULC model: C(f) and leakage accuracy improvements, fix of over-estimated capacitance
- ESD LC mode: fix of over-estimated capacitance
- Update of encrypted matching model architecture in order to improve compliancy with Wicked optimization features
- First support of SOA checks for Goldengate simulator

- DRC changes:
  - Alignment on DRM rev0.4.8:
    - Improved High-Voltage management & Body-Bias support
      - Voltage Assessment algorithm update
      - HV rules addition (NW.D.7, NW.D.9, NW.R.1-7, T3.S.2, T3.D.1, PC.D.12-20, VL.R.1-10, M1.S.i, Vx.D.i & Mx.S.i)
      - Obsolete TDDB rules removal (RX.D.3-5, PC.D.4-7, 552a1-4, 602k1-4, Mx.D.2.1, Mx.D.2.2 and Mx.D.3).
      - Please refer to the dedicated documentation in *$DKITROOT/doc/MANUALS/DESIGN_VERIFICATION/DRC/Voltage_Dependent_Checking_Methodology_AN.pdf*
    - Cleaning and improvement of sealring-related rules
      - Removal of MOB_4a and MOB_4b rules
      - This update may highlight new real errors (GR600b*) in existing connections to sealring (ESDHUB)
    - Removal of LOGOBND exception in CABAR.W.1, CABAR.L.1, CABAR.R.1, 230, 232, 233 design rules
    - Removal of obsolete 229 design rule
    - Addition of EMET.D.1 design rule
    - Forbid CT;filltr, W0;fillOPC and W1;fillOPC layers

- Virtuoso Library changes:
  - OA Techfile update:
    - Addition of new HV rules (minVoltageSpacing)
    - Addition of W0;emet, W1;emet, B1;emet, B2;emet layers
  - Increase of lvsres max dimensions in order to be used over Ix or LB layers
  - Update of cvar_sg callback equation (alignment with spice model)
  - Improved management of standard multiplicity parameter (m) versus advanced multiplicity parameters (mx, my):
    - “mx” automatically inherits value from “m” when switching ON advanced matching feature in CDF
    - “m” automatically inherits value from “mx*my” when switching OFF advanced matching feature in CDF
  - Addition of new CDF switch “*Advanced matching simulation*” to include mismatch, mx, my, deltax, deltay parameters

- Gate resistance (swrg) and self-heating (swshe) parameters remain in existing switch "*Simulation option expert*"

- Addition of definition of capacitors and resistors in ciRegister file
- Update of Back-End configuration management (bkeuser parameter) for ESD STI diodes (*esdndsx, esdvpnp, esdvnpn*):
  - Addition of new value "Automatic" set by default (bkeuser =3) for spice model alignment

- LVS changes:
  - New switch to control reduction of lvsres (separated from other metal resistors)

- EMIR changes:
  - Fix of paths in TOTEM.ini file

- **Changes in Version 1.1 Production released on 07-27-2018 versus Version 1.0.a Production released on 11-17-2017**
  - ST packages references

MODEL	UPT DELIVERABLE
Front-End	Models_C028FDSOI_RF_mmW 1.1-02
Back-End	PEX_models_28FDSOI 2.4-00

BITCELL NAME	RELEASE	UPT DELIVERABLE
memcell_sp0126_SW_28SOI	1.1	memcell_sp0126_SW_28SOI@1.1-PRELIM-02
memcell_sp0120_LL_28	1.3	memcell_sp0120_LL_28@1.3@20110905.0
memcell_sp0120_SW_LL_28SOI	1.0	memcell_sp0120_SW_LL_28SOI@1.0@20130123.1
memcell_sp0152_SW_28SOI	1.0	memcell_sp0152_SW_28SOI@1.0@20140129.1
memcell_rf0251_BB_28SOI	1.0	memcell_rf0251_BB_28SOI@1.0@20141022.1
memcell_dp0316_SW_28SOI	1.0	memcell_dp0316_SW_28SOI@1.0@20140217.0
memcell_dp0316_SW_28SOI	1.1	memcell_dp0316_SW_28SOI@1.1@20140515.1
memcell_cam0711_LVT_28SOI	1.0	memcell_cam0711_LVT_28SOI@1.0@20131008.2
memcell_rom0110_LVT_28SOI	1.2	memcell_rom0110_LVT_28SOI@1.2@20140929.0
memcell_otp2P4_28SOI_EG	1.0	memcell_otp2P4_28SOI_EG@1.0@20120524.0
memcell_otp0P95_28SOI	1.0	memcell_otp0P95_28SOI@1.0@20141024.0

- Documentation changes
  - A collection of guidelines for RF & mmW design are available in the following directory : *$DKITROOT/doc/RF_mmW_GUIDELINES/*

- General changes :
  - Introduction of new single-ended SG varactor single : *cvar_sg* (*ST_C32_addon_DP* CDS Library)

- Introduction of new ESD devices (*cmos32lp* CDS Library) :
  - Low-cap SCR : *esd_lowcap*
  - SG Ultra-Low Cap : *esd_ulc_rvt*
  - EG Ultra-Low Cap : *esd_ulc_eg*
- Calibrerun phase-out :
  - This PDK release introduces the first step of calibrerun utility phase-out, and its replacement by native Calibre commands
  - With this version, calibrerun utility is still available. It translates into native Calibre commands, launch the run and provides details on how to migrate.

- Simulation changes :
  - Fix for multi-fingers simulation in post-layout of matching, LF noise and self-heating, based on new plsnf parameter
  - Addition of best corner for LF-Noise
  - Improvement of post-layout simulation accuracy of RF-transistors when contacts are removed in inner source-drain areas
  - Removal of resistance in diodetwx (Niso/psub) + diodepwtw (Pwell/Niso) diodes
  - SOA: Vdd-max extended to 1.15V for GO1
  - ESD diodes :
    - MHC improvement for overshoot effect
    - Add soa for non-verilogA models
  - ESD MOS : MHC improvement
  - ESD Verilog-A management update :
    - The default spice model is now without Verilog-A
    - A new spice model "*_va*" is added with Verilog-A
    - The existing spice model "*_nova*" without Verilog-A is kept for legacy purpose
  - Addition of lvsres dummy model for Nanotime compliancy
  - User-defined mismatch is not available anymore in Artistkit
    - Please get in touch with your PDK support interface in case of usage
  - Finesim simulator is not supported anymore

- Virtuoso Library changes :
  - Addition of nsig_dnoise parameter for accurate and RF transistors (editable)
  - Addition of mm_nsig_dl mm_nsig_dmob mm_nsig_drs mm_nsig_dtsi mm_nsig_dvfb mm_param parameters for accurate and RF transistors (non-editable)
  - Allow ncrd = 0 in RF-Transistors pcell to remove all contacts in inner source-drain areas
  - New sim-level for ESD spice models with Verilog-A
  - Addition of new layers in OA Techfile :
    - VL & VH purposes for each conductor

        - Slot purpose for each conductor
        - TrLineM6_flex & TrShield_flex markers
        - InOutRegion markers for IA/IB/LB and mmW_line marker
        - ESD_LC and ESD_ULC markers
        - PDV markers
    - Other changes in OA Techfile :
        - Addition of Ix max density rules in OA techfile for Cadence slotting utility enablement
        - Updated routing direction for digital compliancy
        - Added min spacing on large via array
        - Added data.dm in techlib for digital compliancy
    - Removal of eMetro library
    - Update of lvsres netlisting for eldo/spectre/hspice to account for spice model addition
    - Update ctkrev default choice to Current for schematic views
    - Fix useless redundancy of ptwell parameters between symbols and pcells of transistors
    - Update of cfrm*, rm* and esdfets_fdsoi CDF to avoid unexpected variable definition in ADE
    - Improvement of accuracy of resistor callback value vs spice model
    - Fix of pcell abutment issue of MOS
    - Addition of soa parameter on cmom_rf from C28FDSOI_MMW_8ML

- <u>DRC changes :</u>
    - Alignment on DRM rev0.4.7:
        - Update of inductor design rules :
            - New rules to secure placement of indST marker (IND.R.2/3, IND.L.1, IND.S.1)
            - Update of ground rules filtering under indST marker (I-500b, I-799a, I-*.W.1, I-*.S.1)
            - New rules to identify InOut region and transition ring and related density checks
            - New rules to check fill shapes (dummies) under indST marker (I-*.W.3, I-*.S.2)
            - New rules related to mmW marker
        - New rule to check HYBRID-to-Gate min space (55nm) : HYBRID.D.2.1
        - New rule to prevent Gate over HYBRID : HYBRID.R.7
        - Removal of useless and obsolete recommended rules : 102R, 102mR, 102sR, 102tR & 102uR
        - Update of Drift_MOS_Drain derived geometry to secure verification of Drift MOS
        - Filtering of LUP.W.1 rule under MKR;esdt and MKR;esds

- Filtering of IP_*.DEN.8.1 rules under MOB
- Update of CMIM.ANT.6 to consider antenna diodes >= 0.027u in Via_antenna_ratio (similar approach as CMIM.ANT8/9)
- MOM_Mx.DEN.1.1_M* checked only if chip area is >= 200umx200um
- Update of CSR.L.2 to check min=max corner length

- Fix of LUP.R.8 rule under marker esdt
- PVS-DRC is not supported in this PDK release

- FILL changes:
  - smart_tilingRundir/smart_tiling_summary are replaced by fillRunDir/fill_summary
  - New step introduced to manage RX fill inside BFMOAT

- LVS/PEX changes :
  - Support of Custom Transmission Line
  - Addition of switches to disable series & parallel metal resistors reduction
  - Fix of devices recognition issue under marker logo
  - Prevent extraction of opndres & nwres resistors under ESD markers (alignment with DRM truth table). No change to opppcres and opreres resistors
  - Update of Poly Resistor LVS code to comply with the EXTRACT_RES_BODY_COUPLING command of StarRCXT
  - Update of StarRCXT version for Nanotime compliancy
  - Extraction of plsnf parameter for accurate transistors
  - Keep lvsres model in extracted netlists for Nanotime compliancy
  - Fill management update :
    - LVS switch to account for fill connectivity cannot be disabled in LVS for PEX anymore
    - Removal of GDS Fill options in StarRCXT command file
    - Addition of TRANSLATE_VIA_FILLS command set to NO by default
  - Update of Calibre Query control file for Nanotime compliancy (command order, new options)
  - Other updates of StarRCXT command file :
    - Addition of INSTANCE_PORT :command, set to SUPERCONDUCTIVE by default, set to CONDUCTIVE in case of Skipped-Pcells flow with PLSkit
    - Addition of EXTRACT_RES_BODY_COUPLING command, set to YES by default
    - Addition of REMOVE_FLOATING_NETS: YES & REMOVE_FLOATING_PORTS: YES
  - Improvement of parasitic extraction accuracy with QRC (boundaries vs spice model)

- Electro-magnetic changes :
  - Momentum / EMX:
    - Improvement of W-dependency of conductivity for Ix layers

- Momentum :
  - Improvement of W-dependency of conductivity for M1/Mx layers
  - Account for temperature based on latest ads 2017 version

- Electro-migration changes :
  - Totem :
    - Fix of missing devices pins in device_model_config_file
    - Cleaning of warnings

Changes in Version 1.0 Production released on 10-20-2017 versus Version 0.9.a Production released on 09-18-2017

- ST packages references

MODEL	UPT DELIVERABLE
Front-End	Models_C028FDSOI_RF_mmW 1.0-02
Back-End	28NM_STARRCXT_FDSOI_PROTOTYPE 2.3-PRELIM-00

BITCELL NAME	RELEASE	UPT DELIVERABLE
memcell_sp0126_SW_28SOI	1.1	memcell_sp0126_SW_28SOI@1.1-PRELIM-02
memcell_sp0120_LL_28	1.3	memcell_sp0120_LL_28@1.3@20110905.0
memcell_sp0120_SW_LL_28SOI	1.0	memcell_sp0120_SW_LL_28SOI@1.0@20130123.1
memcell_sp0152_SW_28SOI	1.0	memcell_sp0152_SW_28SOI@1.0@20140129.1
memcell_rf0251_BB_28SOI	1.0	memcell_rf0251_BB_28SOI@1.0@20141022.1
memcell_dp0316_SW_28SOI	1.0	memcell_dp0316_SW_28SOI@1.0@20140217.0
memcell_dp0316_SW_28SOI	1.1	memcell_dp0316_SW_28SOI@1.1@20140515.1
memcell_cam0711_LVT_28SOI	1.0	memcell_cam0711_LVT_28SOI@1.0@20131008.2
memcell_rom0110_LVT_28SOI	1.2	memcell_rom0110_LVT_28SOI@1.2@20140929.0
memcell_otp2P4_28SOI_EG	1.0	memcell_otp2P4_28SOI_EG@1.0@20120524.0
memcell_otp0P95_28SOI	1.0	memcell_otp0P95_28SOI@1.0@20141024.0

- General changes :
  - Define EG atto-farad varactor as “Natural” device
  - Define Transmission line as “Natural” device

- Simulation changes :
  - SG/EG RVT Transistor model update (RF and accurate)
    - MHC & accuracy improvement thanks to Local Layout Effects update (WPE, PC-Past-RX, STI-stress)
  - SG/EG LVT Transistor model update (RF and accurate)
    - SG LVT PFET : LF-noise correction

        - EG LVT NFET : STI-stress improvement
    - CMOM-RF frozen views model update (resistance and parasitic capacitance)
    - CMIM model update (leakage, linearity, temperature dependency)
    - EG N/P Poly capacitor model update (MHC)
    - ESD sblk resistors model update
    - VPNP model update (MHC)
    - ESD diode and ESD FET model update
    - Fix of inductor model syntax to avoid crash with Nanotime
    - EG varactor model update (temperature dependency, cut frequency alignment with silicon)
    - High-Perf loHQ inductors model update (MAT30)

- Virtuoso Library changes :
    - The file device.cdl is removed from the Design-kit and therefore not included anymore during the CDL netlisting.
        - Existing CDL netlists are not usable anymore in LVS, and must be re-generated with this Design-Kit.
    - Mesh generator improvements :
        - New option to propose a reduced pattern 1um x 1um
        - New layout view to propose a simplified structure for electromagnetic simulator compliancy
        - Additional options for metal selection
    - ESD diode CDF improvements :
        - Alignment of area/perim equation with model
        - Addition of new parameters spgr_h and spgr_v
        - Update of bke_user display
    - MIM capacitor CDF/Callback update (alignment with model)
        - Removal of useless “C” instance parameter
        - Change of default value of pre_layout_local (-1)
    - Cleaning of un-necessary sim views (eldoD, hspiceD, spectre and ams) in fets, mosRF and resistors
    - Update of simrc to improve CDL netlisting for Bus mapping
    - Update of gateSpacing default value for SG transistors (96nm -> 114nm)
    - Change default netlisting value for pcpastrx_top and pcpastrx_bot (-1)
    - Add callback to sealring to check integer value
    - Cleaning of ptwell parameter for mos and mosRF (removed for non-relevant pcell cases)
    - Improvement of transistor pcell abutments
    - Removal of useless rsx instance parameter for all resistors (alignment with spice model)
    - Update of High-Perf LoHQ inductor pcells (alignment of oout parameter with spice model)

- Transmission Lines pcells :
  - Addition of LVS labels
  - Addition of OPSD, BFMOAT and OP markers
- Update of MACROMOS schematic cells to set ptwell to 1 for LVS consistency
  - A check&Save of existing schematics is therefore required at customer end
- Addition of Hspice and AdvanceMS CDF for CMOMRF devices
- Update of cmos32lp.macroCDLlisting.cdl in order to include all .subckt devices
- Removal of depnfet_b and depnfettw cells

- DRC changes :
  - Alignment on DRM rev0.4.6
    - Update of Flip-Chip rules to comply with packaging requirements (FC44S*, FCA*)
    - Removal of FC61A.EX.1 rule
    - Addition of Perimeter/Area Design Rules (M1.PA.1, Mx.PA.1, Bx.PA.1, Ix.PA.1)
    - Addition of Vx.DEN.2 and Wx.DEN.2 rules
    - Update of DFY_Mx.S.3/4 rules for improved compliancy with Digital Implementation tools
    - Removal of DFY_Mx.S.5 rule
    - Addition of DFY_M1.L.1 under DFY marker
    - Several other updates of rules under DFY marker
    - Update of NW1V and NW2V derived layers
    - Cleaning of recommended design rules (including removal of obsolete ones)
  - Fix of antenna design rules between LB and MIM
  - Fix of ID.MPW.1 rule
  - Fix of 506a/b/c/d rules for improved compliancy with Digital Implementation tools
  - Enablement of EMET.DEN rules under IP-Validation switch. A criteria of 20mm2 has been added to these rules

- TILING changes :
  - Update of exclusions regarding Pad and EDMOS

- LVS/PEX changes :
  - Improvement of RF-MOS property extraction in case of cascoded configuration
  - Filtering of diodepwtw extraction inside ESD Diodes
  - New commands for Calibre-Star-Nanotime flow
  - Ptwell parameter is now compared by default for RF-MOS
  - Fix of via current computation in Cadence EAD (addition of em_via_area_unit option)

- Update of transmission lines in order to account with pcell requirements (BFMOAT and OPSD layers)
- Update of StarRC mapping file in order to enable SMC flow

Changes in Version 0.9.a Production released on 09-18-2017 versus Version 0.9 Production released on 06-16-2017

- ST packages references

MODEL	UPT DELIVERABLE
Front-End	Models_C028FDSOI_RF_mmW 0.9.a-PRELIM-00
Back-End	28NM_STARRCXT_FDSOI_PROTOTYPE 2.3-PRELIM-00

BITCELL NAME	RELEASE	UPT DELIVERABLE
memcell_sp0126_SW_28SOI	1.1	memcell_sp0126_SW_28SOI@1.1-PRELIM-02
memcell_sp0120_LL_28	1.3	memcell_sp0120_LL_28@1.3@20110905.0
memcell_sp0120_SW_LL_28SOI	1.0	memcell_sp0120_SW_LL_28SOI@1.0@20130123.1
memcell_sp0152_SW_28SOI	1.0	memcell_sp0152_SW_28SOI@1.0@20140129.1
memcell_rf0251_BB_28SOI	1.0	memcell_rf0251_BB_28SOI@1.0@20141022.1
memcell_dp0316_SW_28SOI	1.0	memcell_dp0316_SW_28SOI@1.0@20140217.0
memcell_dp0316_SW_28SOI	1.1	memcell_dp0316_SW_28SOI@1.1@20140515.1
memcell_cam0711_LVT_28SOI	1.0	memcell_cam0711_LVT_28SOI@1.0@20131008.2
memcell_rom0110_LVT_28SOI	1.2	memcell_rom0110_LVT_28SOI@1.2@20140929.0
memcell_otp2P4_28SOI_EG	1.0	memcell_otp2P4_28SOI_EG@1.0@20120524.0
memcell_otp0P95_28SOI	1.0	memcell_otp0P95_28SOI@1.0@20141024.0

- Simulation changes :
  - SG/EG LVT Transistor model update (RF and accurate) :
    - SG LVT N/P FET : STI stress effect adjustment for small transistor width
    - EG LVT PFET : pre and post layout gate length extraction alignment
  - Removal of Finesim support

- Virtuoso Library changes :
  - Re-introduction of M6 to IA via in WireEditorSetup constraint group

- Totem :
  - Alignment of techfiles with PEX tools (Alucap description)

- EMX :
  - Fix of diffusion resistivity in techfiles

○ Changes in Version 0.9 Production released on 06-16-2017 versus Version 2.9 Production released on 11-15-2016

■ ST packages references

MODEL	UPT DELIVERABLE
Front-End	Models_C028FDSOI_RF_mmW 0.9-00
Back-End	28NM_STARRCXT_FDSOI_PROTOTYPE 2.3-PRELIM-00

BITCELL NAME	RELEASE	UPT DELIVERABLE
memcell_sp0126_SW_28SOI	1.1	memcell_sp0126_SW_28SOI@1.1-PRELIM-02
memcell_sp0120_LL_28	1.3	memcell_sp0120_LL_28@1.3@20110905.0
memcell_sp0120_SW_LL_28SOI	1.0	memcell_sp0120_SW_LL_28SOI@1.0@20130123.1
memcell_sp0152_SW_28SOI	1.0	memcell_sp0152_SW_28SOI@1.0@20140129.1
memcell_rf0251_BB_28SOI	1.0	memcell_rf0251_BB_28SOI@1.0@20141022.1
memcell_dp0316_SW_28SOI	1.0	memcell_dp0316_SW_28SOI@1.0@20140217.0
memcell_dp0316_SW_28SOI	1.1	memcell_dp0316_SW_28SOI@1.1@20140515.1
memcell_cam0711_LVT_28SOI	1.0	memcell_cam0711_LVT_28SOI@1.0@20131008.2
memcell_rom0110_LVT_28SOI	1.2	memcell_rom0110_LVT_28SOI@1.2@20140929.0
memcell_otp2P4_28SOI_EG	1.0	memcell_otp2P4_28SOI_EG@1.0@20120524.0
memcell_otp0P95_28SOI	1.0	memcell_otp0P95_28SOI@1.0@20141024.0

■ General changes :

- ○ Introduction of new passive devices :
  - ▪ Pcells are available in Virtuoso library *ST_C32_addon_AMS* :
    - Single and differential transmission lines (*differential_tline_6U1x_2T8x_LB, microstrip_tline_6U1x_2T8x_LB*)
    - Single and differential High-Performance Low-HQ inductors (*inddif_lohq_high_perf_6U1x_2T8x_LB,inddif_lohq_high_perf_6U1x_2T8x_LB)*
  - ▪ Related DRC, LVS, simulation support
- ○ Update of ST-specific devices usage restriction :
  - ▪ RF-transistors and opppcres_lc resistor are no more restricted
  - ▪ Devices from ULP perimeter (*egnexti, egpext, SP126 SRAM, HLVT transistors*) are still restricted. Please contact your ST-support in case of interest.
- ○ Atto-Farad varactor support :
  - ▪ This device is now considered as “natural”. Therefore, its spice model is removed from Design-Kit. Please contact your ST-support in case of interest.

■ Simulation changes :

- ○ Removal of “core” SG/EG transistor spice models
  - ▪ Standard simulation level is not available anymore

- Transistor model update (RF and accurate)
  - EG LVT silicon based (W-scaling)
  - Accuracy improvement thanks to Local Layout Effects update (deep-nwell, WPE, PC-Past-RX)
- EG LVT powerswitch model update
- EDMOS model update (v0.1)
- MOM capacitor model update (C0, Corners and matching)
- VNPN model update (Corner and matching improvement)
- Resistors model update (Centering, Mismatch, Corners, L-scaling)
- New simulation level without Verilog-A for ESD devices
- Support of TID feature on EGLVTPS ageing model
- Re-introduction of AFS and ADS simulators

- DRC changes :
  - Renaming of DRC switch : IP-Validation, Chip SignOff, Custom
    - ST_107a/ST_PDPCa/VV.DEN.2 rules are now enabled under Chip SignOff only
  - Alignment on DRM re0.4.5:
    - OPSD rules updates
    - Removal of 724 and 791 rules
    - EDMOS rules update :
      - P+ Diffusion update for 5V recognition on drain
      - Addition of Isolation EDMOS Design Rules
      - 710 rule removal inside EDMOS
    - Replacement of MKR;not4V by MKR;not8V in Drift-MOS rules
    - Update of FD_GEN.5 rule to account for BFMOAT and other EDMOS layers
    - New rule FCRF.R.1 to identify RF flip-chip pads
    - New optional density rules for advanced pad verification
  - Removal of GR999aa rules
  - Fix of 204b/CA.EX.1 rules

- TILING changes :
  - Addition of TCDcleaning post-trigger to avoid issues during eMetro tiles generation
  - Increase of uAIM5 spacing to T3 (1.05u)

- Virtuoso Library changes :
  - Addition of C28FDSOI_MMW_8ML Virtuoso Library
  - Transistors :
    - Fix of CDF ptwell parameter on hierarchical devices (tw, np)
    - Removal of transistor standard simLevel (SimMosfetStandard)

- Fix of user-defined sa/sb management and computation w.r.t to other transistor properties
- Addition of new instance parameters for improved multiplicity management at schematic level (mx, my, deltax, deltay).
  - The usage of this feature is restricted under an “expert” conditional switch.

- Resistors :
  - Callback alignment with spice model
  - Removal of resistor series warning pop-up
- MOM capacitor :
  - Callback alignment with spice model
  - Fix of callback issues for some metal configurations
  - Removal of mult CDF parameter
- RF-MOM capacitor (fixed views) :
  - Displayed capacitance value alignment with spice model
- EDMOS :
  - Egnexti pcell update w.r.t. new Isolation Design Rules
  - Change of Lext of NEDMOS to 222n
  - Change of minimum length of PEDMOS to 222n
  - Change of default width of PEDMOS to 2.222n
  - Addition of CDF self-heating and mismatch parameters
  - Fix of term order for spectre netlist
- Inductors :
  - Minimum value of diameter updated to 88um for ind_hd/inddif_hq
  - Multiple improvement of the callback, including wmp and ls values
- ESD devices :
  - Addition of SimEsddiodeStandard & SimEsddiodeNova views to handle new simulation level without Verilog-A
  - Addition of mkr;sdi over diffusion for improved compliancy with LVS
- OA Techfile :
  - New layers added
  - Added cut size on via;fillOPC
  - Fix spacing rules on Wx, WxBAR, VxLRG, CA, CABAR arrays
  - Added standard via BARLINE
  - Removal of LV blockage from layer map and addition of LV;net in techfile
  - Addition of rules 2x53a & 2x51d and DFY_Mx.S.2_M2, DFY_Mx.L.1_M3/4/5/6 to enable Virtuoso Analog Router capability
  - Fix of standard via array when number of columns > 5

- LVS/PEX changes :
  - Disable of parallel reduction for MIM capacitor by default

- New switch to control LVS EXPAND SEED PROMOTIONS command
- Addition of new ERC rule checking the connection of sealring to a ground net
- Extraction of new instance parameters for “PC-Past-RX” modeling effect
- Increase of maximum search distance for STI-stress parameters (sa,sb) to 3u
- EDMOS :
  - Fix of sa/sb and pre_layout_local computation for EDMOS
- Update of parasitic extraction with StarRC
  - Improvement of alucap description (MHC)
  - Improvement of MOM substrate capacitance accuracy
  - Update of diffusion resistance extraction feature to allow better parasitic reduction
  - Improvement of capacitance accuracy w.r.t. fill shape layers (metal + vias)
- Update of parasitic extraction with Quantus-QRC
  - Improvement of alucap description (MHC)
  - Improvement of capacitance accuracy extraction related to transistors
  - Improvement of MOM-capacitor parasitic management with QRCFS (no more double-counting)
- Update of electromagnetic simulations with Momentum and EMX
  - Improvement of alucap and passivation description and (MHC)
  - Additional techfiles (nominal corner only) to handle specific inductor configurations :
    - Large VV
    - Substrate without BFMOAT
- Calibre xRC/xACT is not supported in this Design-Kit
- Fix of via current computation in Cadence EAD (addition of em_via_area_unit option)

- Helpdesk tickets :

Helpdesk tickets	Description
81830	esdndsx diode extraction
81630	CMOS28FDSOI@2.8c; LVS CMIM reverse "W" ,"L" properties
81453	connection between shape and psub in cmom_6U1x_2T8x_LB_sh
80347	Teckfile missing rule
81183	LVS error when cmom rf used under T3 with LVS1 marker : local sub not found
81743	Mesh Pcell failed
82995	LV net & boundary absence in tech.db
81031	Troubles with change stiStress estimation
84029	pb callback and netlisting with STI parameters sa and sb
83034	PDK2.9-09 potential error in DRC versus new rules 204b/CA.EX.1
83119	inddif_hq_6U1x_2T8x_LB nb of turn
82611	Problem call back on capacitor

81997	finger nb netlisting issue
80082	missing layer on pcell
81697	C28FDSOI_MMW_8ML_beta_fix/TL_ustrip_* are empty!
80255	eMetro batch mode
83230	Info in techfile for EAD tool?
84974	Tiling with PDK leads to DRC errors on EMET structures
84165	Update of PDK_STM_cmos28FDSOI_RF_6U1x_2T8x_LB.v2.9-07 for mmW support

○ Changes in Version 2.9 Production released on 11-15-2016 versus Version 2.8.c Production released on 07-01-2016

■ ST packages references

MODEL	UPT DELIVERABLE
Front-End	Models_C028FDSOI@2.9-00
Back-End	28NM_STARRCXT_FDSOI_PROTOTYPE 2.1-PRELIM-00

BITCELL NAME	RELEASE	UPT DELIVERABLE
memcell_sp0126_SW_28SOI	1.1	memcell_sp0126_SW_28SOI@1.1-PRELIM-02
memcell_sp0120_LL_28	1.3	memcell_sp0120_LL_28@1.3@20110905.0
memcell_sp0120_SW_LL_28SOI	1.0	memcell_sp0120_SW_LL_28SOI@1.0@20130123.1
memcell_sp0152_SW_28SOI	1.0	memcell_sp0152_SW_28SOI@1.0@20140129.1
memcell_rf0251_BB_28SOI	1.0	memcell_rf0251_BB_28SOI@1.0@20141022.1
memcell_dp0316_SW_28SOI	1.0	memcell_dp0316_SW_28SOI@1.0@20140217.0
memcell_dp0316_SW_28SOI	1.1	memcell_dp0316_SW_28SOI@1.1@20140515.1
memcell_cam0711_LVT_28SOI	1.0	memcell_cam0711_LVT_28SOI@1.0@20131008.2
memcell_rom0110_LVT_28SOI	1.2	memcell_rom0110_LVT_28SOI@1.2@20140929.0
memcell_otp2P4_28SOI_EG	1.0	memcell_otp2P4_28SOI_EG@1.0@20120524.0
memcell_otp0P95_28SOI	1.0	memcell_otp0P95_28SOI@1.0@20141024.0
memcell_otp0P95_28SOI	1.0	memcell_otp0P95_28SO@1.0-01

■ Supported simulators :

EDA tools	Simulators	Supported in DK 2.9
ams	Eldo	yes
	Advance-MS	yes
mmsim	Spectre	yes
incisive	AMS-Designer	yes
hspice	hspice	yes
goldengate	goldengate	yes
customsim	xa-eldo	yes
	xa-hspice	yes
	xa-spectre	yes
finesim	finesim-eldo	yes
	finesim-hspice	yes

	finesim-spectre	yes
afs	afs-eldo	no
	afs-hspice	no
	afs-spectre	no
ads	ads	no

- General updates :
  - Addition of new devices of ULPv1 perimeter :
    - Extended-Drain N/P transistors : *egnexti, egpext (Virtuoso library : ST_C32_addon_DP)*
    - HLVT N/P transistors : *hlvtnfet, hlvtpfet (Virtuoso Library : cmos32lp)*
    - SP126SW bitcell transistors : *dsxpfetpu_b, dsxnfetpd_b, dsxnfetwl_b (Virtuoso Library : cmos32lp)*
    - Please note that these devices are specific to ST-foundry. Please contact your ST support in case of interest.
  - Poly-resistors changes :
    - Existing *opppcres* resistance value has been changed to 440ohms/sq. Please note that it requires now an additional mask
    - Addition of new *opppcres_lc* resistor, with a value of 370ohms/sq, not requiring any additional mask. This resistor is categorized as a ST-specific device.

- Simulation updates :
  - Update of “Accurate” LVT and “RF” LVT spice models
  - Update of inductors and EG-varactors spice models
  - Update of ageing models
    - First support of spectre in addition to eldo/hspice
  - Encryption of accurate spice models
  - Pre-defined spectre simulation corners in Maestro

- DRC updates :
  - Fix of GR102n and GR203R code
  - Addition of EDMOS and HLVT related rules
  - Support of new wirebonding padClass : WB57SR_POC
  - Robust rules update under MKR;DFY
  - Update of density rules at IP level in order to ease insertion of IP in final chip
  - 45deg design-rule update
  - Improvement of CalibreDRV : layer connectivity

- Tiling updates :

- Tiling allowed under MKR;wb
- RX tiling allowed inside BFMOAT
- Change of MIM fill shapes from drawing to fill purposes

- LVS/PEX updates:
  - Comparison of p_la parameter in LVS for PEX
  - Improvement of capacitance parasitic extraction of CMOM with QuantusQRC
  - Improvement of spice output format with QuantusQRC
  - New procedure to secure usage of ST-specific devices. This is applied to ULPv1 devices (see previously), new opppcres_lc resistor and RF-transistors.
    - In order to use these devices, please contact your ST support

- Virtuoso Library updates :
  - Addition of new stretch-handles options in SG transistor pcells
    - User-defined values for RX-enclosure on CA
    - User-defined values for CA to CA space
    - PC endcap and dummy PC
    - New option to control BP enclosure of RX under robust rules switch
  - New procedure to secure usage of ST-specific devices. This is applied to ULPv1 devices (see previously), new opppcres_lc resistor and RF-transistors.
    - In order to use these devices, please contact your ST support
  - Update of eMetro cells in cmos28_emetro library
  - Fix of poly resistor netlisting issue with pbar parameter
  - Callback update of inductors, varactors and opppcres, aligned with spice model change
  - Freeze width of inductors to 11u when nbturns=3
  - Fix of nf netlisting in case of fingerWidth mode
  - Diodes :
    - Update computation of area, peri, w and h with parameter Rectangular Shape
    - Alignment of min area/perim with models
  - ESD fets:
    - Alignment of ldop default value with models
    - Removal of soa parameter from CDL netlist
  - Callback update to limit transistor PC-pitch in case of length > 48nm
  - OA Techfile
    - Addition of layers :

MKR	EXT_N	204	245
MKR	EXT_P	204	246
MKR	NEDMOS	201	113
MKR	OPPPCRES_LC	204	247

MKR	PEDMOS	201	114

- Hidding of FBB layers from LSW
- Update of functions & techDerivedLayers section to fix connectivity warning issues in layoutXL
- Loadability of techfile in the digital Cadence innovus tool restored
- Modification of minOppExtension for upper via layers (introduction of 'cutClass parameter to be in-line with existing defined cut classes)
- Update of M1 pitch + introduction of M1 offset
- Addition of minCutClassSpacing table for CA
- Clean-up of minCutClassSpacing tables for vias to cover all existing configurations (via large introduction - 3 tables per configuration (parallel overlap < 0 - parallel overlap = 0 - parallel overlap > 0) - shortEdge vs longEdge)
- Pessimism removal on minProtrusionNumCut (only applied on below metal layers)
- Optimism removal on minNumCut (applied on both top and bottom metal layers)
- Alignment of IA/IB spacing tables with 8x04c DRM rule

- Electro-Migration changes :
  - Several improvements of CustomSim-RA and Voltus-FI

Changes in Version 2.8.c Production released on 07-01-2016 versus Version 2.8.b Production released on 06-10-2016

- Simulation updates :
  - Encryption of accurate spice models
  - ADS and AFS formats are not supported

- LVS/PEX updates:
  - Fix of missing pre_layout_local parameter in extracted netlists
  - Fix of incorrect accurate model suffix from StarRC and QuantusQRC extracted views

Changes in Version 2.8.b Production released on 06-17-2016 versus Version 2.8.a Production released on 05-27-2016

- Simulation updates :
  - Support of ageing+ models with accurate spice models
  - Addition of missing spice model documentation (inductors, CMOM, varactors)

- LVS/PEX updates:
  - Code update to ensure connection of vias LARGE on RF-Transistors

- Virtuoso Library updates :
  - Fix of V3 minCutClassSpacing in techfile
  - Change order of drawing and VIA BAR in layer map to ensure correct streamin/streamout

o Changes in Version 2.8.a Production released on 05-27-2016 versus Version 2.8 Production released on 04-06-2016

- Simulation updates :
  - Update of self-heating SOA check

- Virtuoso Library updates:
  - Addition of multiplicity for RF-Transistors and diodes
  - Support of robust rules for RF-Transistors and EG-varactors pcells
  - Addition of layers for Veloce-RF support
  - Update of mim_rf parameter management to comply with existing designs
  - Improvement of maximum number of contacts on RF-Transistors pcell (new switch)
  - Update of pop-up window related to gate-spacing limitation to avoid unwanted occurrences
  - Addition of cfrmx netlisting for simulators

- DRC updates:
  - Support of new version of HD-OTP Bitcell
  - Fix of iPVS issue due to hard-coded local paths

- LVS/PEX updates:
  - Code update to force connection of the floating 5th pin of RF-transistors
  - Output “acc” model in extracted netlists for all PEX tools
  - Improvement of parasitic capacitance extraction accuracy for RF-transistors with QuantusQRC
  - Improvement of parasitic capacitance extraction accuracy for CMOM with QuantusQRC and Calibre xRC/xACT
  - Bug fix of LVS signature generation
  - Bug fix of inductor nbturns property computation

- Electro-Migration changes :

- Update totem techfile to take into account diffusion resistivity
- Correction on CustomSim-RA EM Blech rules to have the correct value on boundaries according to DRM

■ New Layers :

text	PC	63	1
text	M1	63	2
text	M2	63	3
text	M3	63	4
text	M4	63	5
text	M5	63	6
text	M6	63	7
text	IA	63	8
text	IB	63	9
text	LB	63	10
text	vlc	63	11
HYBRID	emet	204	220
INDdumVlcRF	drawing	204	221
vlcTransmis	drawing	204	222
vlccn	drawing	204	223
vlccn	PC	204	224
vlccn	M1	204	225
vlccn	M2	204	226
vlccn	M3	204	227
vlccn	M4	204	228
vlccn	M5	204	229
vlccn	M6	204	230
vlccn	IA	204	231
vlccn	IB	204	232
vlccn	LB	204	233
vlcdummy	drawing	204	234
vlcdummy	PC	204	235
vlcdummy	M1	204	236
vlcdummy	M2	204	237
vlcdummy	M3	204	238
vlcdummy	M4	204	239
vlcdummy	M5	204	240
vlcdummy	M6	204	241
vlcdummy	IA	204	242
vlcdummy	IB	204	243

vlcdummy	LB	204	244

o Changes in Version 2.8 Production released on 04-18-2016 versus Version 2.7.a Production released on 12-21-2015

- Common new features :
  - This Design-Kit v2.8 introduces the support of the following **new transistors**, improved for **RF-applications** :
    - *nfet_rf, lvtpfet_rf, eglvtpfet_rf, egvlvtpfet_rf*
      - The 5th pin of these devices may remain as floating in schematic if they are not placed inside a triple-well
    - *pfet_rf, lvtnfet_rf,, eglvtnfet_rf, egvlvtnfet_rf*
      - These device have are 4-pin only and must be placed inside a triple-well
    - These devices have dedicated spice models, pcells and DRC/LVS rules
    - A specific **segmented simulation level** is also available
  - Spice models of all transistors except SRAM have been improved in order to take into account the **matching variation due to geometrical location**.
    - For standard transistors, a **new simulation level** suffixed with"_**acc**" has been added to enable this effect. This simulation level is **defined by default** during netlisting of schematic views.
    - Complementary to this model update, new extracted parameters (**xpos,ypos,plorient**) are required for accurate Post-Layout Simulation
    - This effect is accounted by default in the new RF-transistors spice models
    - It is possible to use the former spice models (identical to DK 2.7.a) by selecting the non "_acc" simulation level
  - The original **MOM capacitor** has been improved in order to properly take into account the access connection during simulation.
    - In case of a **rectangle MOM capacitor** (nfdirx≠nfdiry), designer must be aware of the way it will be connected on layout. If the device will be connected through the short side of the bus, it is **mandatory to enable** the new switch "**short_bus**" on both schematic and layout, in order to not underestimate the access resistance.
    - This parameter is compared by LVS
    - Connection on both sides of the same bus is prohibited
  - The **MIM capacitor** device has been improved for the RF-applications :
    - A new switch "**RF-configuration**" is available on pcell to provide a less-resistive configuration. This configuration is defined by default.

- This switch is also available in schematic. When it is disabled, a SOA is displayed during simulation to warn designers
- This parameter is compared by LVS

- Simulation updates:
  - Poly resistors :
    - Reduction of corner spread (no change to typical)
    - A width of 50nm is now allowed for opereres for RF-switch application. This is the only value authorized below 150nm.
      - A SOA rule has been added to secure such usage
  - Updated ageing models :
    - Addition of ageing+ models for eldo only
    - Addition of EGCAP ageing model
  - Improvement of series effect on self-heating of resistors
  - Support of AdvanceMS

- Virtuoso Library updates:
  - In order **to avoid unexpected netlisting issues** due to a known Virtuoso limitation, the change of device name in symbol property is **not allowed anymore**
  - Transistors :
    - Increase maximum finger width to 35u
    - Alignment of as, ad, ps, pd values to spice models and pcells
    - New pop-up to warn users about limitation with gate spacing during schematic simulation
    - Fix of abutment issues in case of different width and length
    - Replacement of “Simulation Options Accurate” by “Simulation Options Expert”
  - Resistors :
    - Increase maximum width to 35u, under the condition of a dedicated switch
    - New pop-up to warn users about limitation with sbar during simulation
  - New pcell configuration for all transistors, EG capacitors, diodes and bipolars to comply with robust rules.
    - This configuration is defined by default when creating a new instance
    - The standard pcell configuration is preserved for existing designs.
  - ESD Gate diodes :
    - Replacement of of sac parameter by l (length)
    - Change maximum length value to 0.64um
  - Bipolars:
    - Removal of useless sizedup parameter for both vpnp and vnpn
    - Addition of mult and mismatch parameters for vpnp

- Addition of layers in techfile (see dedicated section below)
- Support of DC annotation with resistors
- Change of enclosures on connect_MIM pcell
- Fix of several parameter netlisting for macro-transistors
- Update of techfile to have Vx instead of VxBar in stacked vias
- Fix of pcell issue when changing nf parameter for RPO transistors (esd*_fdsoi)

- DRC updates:
  - Alignment on DRM rev0.4.3
  - Code improvement to avoid false violations :
    - CMOM bus-related errors
    - DFY_Mx* errrors on P&R blocks
    - GR604k2 errors on SPREG compilers
    - XA via BAR errors
    - LOGO errors
  - Code improvement to detect new violations :
    - 553q1_V2
  - New rules for eMetro post swap securization
  - Abutment of BFMOAT and NW is now authorized
  - Update of opreres rule to allow a 50nm-width
  - Update of CMOM rules to support new RF configuration with enlarged access and improved shield
  - New rules to secure placement of MOSRF marker on pcell
  - Code update to support new ESD structure, under marker esdt_adv
  - Some robust rules have been added for R&D purpose under WYS marker
    - These rules allow to draw with PC cut and CA BAR layers

- FILL updates:
  - Code improvement in order to reduce runtime
  - Bug fixes regarding eMetro placement and regarding switch combination

- LVS/PEX updates:
  - Support of new devices (MOSRF, MOMRF, Transmission lines)
  - Code update to support new ESD structure, under marker esdt_res
  - Fix of diffusion sheet resistance value in StarRCXT (corner inversion)
  - Improvement of parasitic diode extraction
  - Alignment of ps, ps computation for all transistors with spice models
  - Alignment of opppcres sheet resistance with spice models
  - Alignment with DRM truth table regarding extraction of resistors

- Removal of switch to enable custom MIM capacitor supported. These device is now supported under the dedicated marker FlexibleMIM
- Increase of tolerance for inductor diameter comparison
- Fix of Calibre signature feature
- Fix of sac parameter extraction for some ESD structures
- Improvement of user-defined diffusion resistance script in order to comply with StarRC's Temperature Sensitivity Flow
- First support of Calibre xACT
- Alignment of Momentum techfile with latest technology data

- BulkChecker support has been deprecated
  - STECCK must be used as of now.

- New layers :

M1	FBB1V0	15	130
M1	FBB1V8	15	133
M2	FBB1V0	17	130
M2	FBB1V8	17	133
M3	FBB1V0	19	130
M3	FBB1V8	19	133
M4	FBB1V0	21	130
M4	FBB1V8	21	133
M5	FBB1V0	31	130
M5	FBB1V8	31	133
M6	FBB1V0	44	130
M6	FBB1V8	44	133
M7	FBB1V0	46	130
M7	FBB1V8	46	133
B1	FBB1V0	79	130
B1	FBB1V8	79	133
B2	FBB1V0	81	130
B2	FBB1V8	81	133
IA	FBB1V0	136	130
IA	FBB1V8	136	133
IB	FBB1V0	137	130
IB	FBB1V8	137	133
CT	filltr	204	165
CT	exclude	204	166
MKR	WYS	204	182
MKR	RF	204	183
V1	emet	204	192

M2	emet	204	193
V2	emet	204	194
M3	emet	204	195
V3	emet	204	196
M4	emet	204	197
V4	emet	204	198
M5	emet	204	199
V5	emet	204	200
M6	emet	204	201
MKR	esdt_adv	204	202
MKR	esdt_res	204	203
CT	drawing	247	0
M1	lrg_mombus	204	204
M2	lrg_mombus	204	205
M3	lrg_mombus	204	206
M4	lrg_mombus	204	207
M5	lrg_mombus	204	208
M6	lrg_mombus	204	209
B1	lrg_mombus	204	210
B2	lrg_mombus	204	211
IA	lrg_mombus	204	212
IB	lrg_mombus	204	213
LB	lrg_mombus	204	214
TrLine	mkr	204	215
TLdiff	mkr	204	216
TrShield	mkr	204	217
TL_M1	mkr	204	218
RFCMOMST	mkr	204	219

- **Changes in Version 2.7.a Production released on 12-22-2015 versus Version 2.5.f released on 02-20-2015**

- Simulation changes :
  - Support of new spice models v1.1 with UTSOI2.1
    - All devices are updated except SRAM transistors
    - Alignment on latest silicon measurements
  - Removal of accurateRgate simulation level of SG/EG transistors
  - Addition of SSF/FFF corners
  - Removal of obsolete SRAM devices : lscnfet, lscpfet, lsrnfetwl_b, lsrnfetpd_b, lsrpfetpu_b
  - CMOM :
    - Support of metal6 option
    - Alignment of monte-carlo on pre-defined corners

- CMIM : Alignment of monte-carlo on pre-defined corners
- Simulators :
  - Addition of ADS, AFS-hspice, finesim-hspice and finesim-spectre spice models
  - Support of AMS-designer (incisive)
  - Support of MOSRA ageing models (hspice/xa)

- DRC changes :
  - Alignment on DRM rev0.4.2
    - Merge of 28LP DRM and 28FDSOI Addon DRM into a single document
  - The following DRC updates may require re-work of existing designs :
    - New CA-punch-through rule (CA.EX.1)
    - New rules for SRAM securization
    - New rules to support HD-OTP Bitcell
    - New rules to secure ESD designs
    - Update of passivation rules (LV/DV)
    - Addition of Robust Design Rules : DFY_Mx.S.1, DFY_Mx.L.1, DFY_Mx.S.2, DFY_Mx.S.3, DFY_Mx.S.4, DFY_Mx.S.5
    - Forbid usage of wimpy marker under SRM;peri marker :
      - Allow 40nm-gate length under SRM-peri marker
      - Removal of 102peri rule
      - Removal of POB_207/POB_207peri/POB_102peri.
      - Addition of rule DFY_SRM.CA.D.1 under SRM-peri marker to secure distance between contact and poly U-shape
    - Fix of rules : GR207a, ST_IND895
  - Multiple minor rule fixes
  - Support of flexible MIM under dedicated marker
    - Update of CTM.W.2/CMT.A.3 rules to be waived under marker FlexibleMIM
  - Addition of AFSD rules
  - Update of BFMOAT rules
  - Update of density rule for very large inductor
  - Antenna rules :
    - Fix of check in case of MIM layer
    - Relaxation of FD_131xc from 0.1 to 10
  - Improvement of ID.BEOL rule to check forbidden layers
  - Improvement of DRC code to avoid false errors on BUMP, LUP, EMET related rules
  - Support of Calibre Realtime (see dedicated section below)
  - Update of 613a/613b/613c/2x73a/2x73b/2x73c rules in the way via distance should be evaluated (shortest path) for Place&Route tool alignment
  - Removal of PN4a/PN4b rules in order to secure checks under LOGOBND

- MOM capacitor :
  - Support of bus and fingers on metal6
  - Addition of MOMbus marker rules and related code improvement to avoid false error in some configurations
  - Fix of MOM.D.4.or rule
- Inductor_Area sizing reduced to 50um

- FILL changes :
  - New constraints with respect to markers AFSD and HD-OTP on both FEOL/BEOL parameters
  - Support of PVS-FILL

- Bitcell changes :
  - Removal of the following bitcells : SP152LVT, RF298LL, ROM136RVT, SP197LL, TCAM793, OTP_EG_FW

- Virtuoso Library changes :
  - Replacement of mgen by skill for pcells of library cmos32lp
  - Support of new devices (pcells and symbols) :
    - Elementary fringe capacitors
    - Metal resistors
    - Depnfet/depnfettw
  - Removal of obsolete SRAM devices : lscnfet, lscpfet, lsrnfetwl_b, lsrnfetpd_b, lsrpfetpu_b
  - Support of all cmom* pcells and symbols to improve IP-development across different metal options
  - Alignment on new spice models v1.1
    - Update of FET instance parameters
    - Update of DC annotation
    - Callback update (resistors, varactors, capacitors)
    - Removal of accurateRgate simulation level and CDF options
  - MOM capacitor:
    - Support of metal6 option (pcell, CDF, Capacitor value)
    - Update of CMOM layer names in pcells :
      - **Please note that it is mandatory to run updatePCell skill function when opening an existing layout view with this DK 2.7.a, before running any DRC/LVS verification**
      - **From Layout View *: PDK -> cmos32lp -> Check/Update PCELL parameters*, select cmom devices on left tab, and layout views on right tab.**
    - Callback update for cmom w/o vias to limit bus metal level to fringe metal level

- Addition of check for integer input value of nfing
- New option of CMOM shielded pcell to allow abutment

- Inductors pcells :
  - Removal of forbidden layers in 8ML
  - Enable IB dummies in center of coil
  - Fix of asymmetric fill shapes
  - New option to select connection on shield
- Transistors :
  - Addition of CA_PITCH_126 option
  - Support of parametrisation of nf and gatesplitstripes
  - CDF fetbulk property renamed as lSup/hSup to ensure compliancy with existing schematics
  - Hide CDF parameters u0_mult and p_vta
  - Second guardring not allowed for pfet GPF and nfet flipwell
  - Second guardring allowed only with first guardring for nfet GPF and pfet flipwell.
  - Change of default values of following CDF parameters :
    - psw_acv_sign p_vta u0_mult stress_vt (SRAM transistors)
    - Swrg (logic transistors)
  - Parameters as/ad not updated when defined by users
  - Addition of M1Route, PolyRoute and DFM_Pcell parameters in symbols to improve modgen usage
  - New parameters for RPO FETs pcells
  - Fix of sd netlisting to “default”
  - Parametric width management
  - Aligmnent of as/ad/ps/pd symbol values on pcell dimensions
  - Addition of source_first parameter allowing to change as/ad accordingly
  - Update of min/max values (EGVLVT)
- EG varactor :
  - Callback update to align on model change
- ESD Devices :
  - Review CDF minimum values
  - Add finger length in symbol of Gated diodes
  - Remove ESD;f markers from pcells
  - Addition of soa parameter
  - Fix pcell evaluation failure of esdndsx
- CMIM :
  - Fix of error due to multiplicity
  - callback to avoid forbidden pcell configuration
  - Addition of connect_mim pcell allowing to easily connect MIM layers to IB

- Resistor callbacks updates :
  - Removal of multiplicity parameter for resistor. Parallel stripes parameter has to be used from now on
  - Management of pbar and s in resistance value
  - Allow variable input for pbar and s
  - Callback update to align on model change
- SRAM :
  - Fix of callback error when changing the length
- Update of min/max values of diodes
- UpdateCDF procedure improvements
- Fix HSSOI.D.9 error on pcell
- Addition of layers in techfile (see dedicated section below)
- Bug fixes and other improvements :
  - STLib (remove warning and .pak files, add hspice views)
  - Update of cmos32lp.macroCDLlisting.cdl to align on CDL netlisting
  - Empty default value of macro-devices
  - Hspice term-mapping

- LVS and PEX changes :
  - Cfringe devices support
  - Metal resistors devices support
  - Depnfet device support
  - Support of non-rectangular MIM decap, with holes through dedicated switch
  - Change in ESD devices extraction
    - Removal of ESD_hbm and ESD_cdm requirement for RPO transistors and gated diodes
    - Addition of requirement of MKR;foxd for ESD STI diode extraction and POLYB for ESD gated diodes
  - New ERC rule advising the usage of LVS1 drawing8 marker to check substrate diode connection
  - Improvement of short detection in case of EG capacitor below CMOM
  - Improvement of short detection in case of vias over lvsres
  - Improvement of devices recognition : Alignment on DRM truth table for devices :
    - SRAM transistors : HYBRID layer is forbidden
    - Logic transistors and resistors : NBIP layer is forbidden
    - EG varactors : several layers are forbidden
    - Vertical PNP bipolar : PC and NBIP layers are forbidden
  - Fix of ERC2_ST to avoid false error under resistor
  - Addition of specific tolerances for MIM capacitor
  - New switches to disable parallel reduction
  - Bug fix in inductor and MIM capacitor property computation

- Alignment of parasitic extraction on latest silicon measurements :
  - Gate stack update
  - Update of poly and contact resistance values
  - Update of diffusion sheet resistance value
  - Update of silicon length for SG transistors (28nm)
  - Update of Poly-Bias management (avoiding shrink effect)
- Ignore gate resistance for all transistors (including SRAMs), now managed inside spice models
- Addition of sigma corners
- Update of EG varactor code to allow length larger than 1um
- Improvement of Quantus-QRC gate-to-contact capacitance accuracy
- StarRC : Use of new RSD post-processing to support Temperature Coefficient and simultaneous multi-corners flow
- Update of pre_layout_local management for all PEX tools :
  - Addition of keyword “PINOPERATION OR” to avoid too pessimistic post-layout simulations
  - Addition of pre_layout_local parameter for missing devices such as cmom_6U1x_2U2x_2T8x_LB*
  - Removal of non-supported parameter botcap

- Electro-Migration changes :
  - Addition of derating factors for VxBAR/VxLRG Electro-Migration rules
  - Improvements of Voltus-FI

Change in Version 2.5.f released on 02-20-2015 w.r.t Version 2.5.d

- LVS changes :
  - Improvement to detect substrate connection in SRAM when contact interacts with SRPU marker
  - Bug fix in inductor property computation

Change in Version 2.5.d released on 27-10-2014 w.r.t Version 2.5

- Devices and technology changes :
  - Removal of all EG2 devices and related features (symbols, pcells, DRC, LVS and simulation models)
  - The following devices are no more supported :
    - egnfet2, egnfet2_b, egnfet2tw, eglvtnfet2, eglvtnfet2_b, eglvtnfet2np, esdegnfet2_fdsoi, esdeglvtnfet2_fdsoi

- DRC changes :

- Alignment on DRM 28FDSOI rev 0.3.7
- Support of mixed POBIAS for retention flip-flop standard cells
- Rule update to remove false voltage errors on CMOM with small pitches

- TILING changes :
  - Update of expert switches default values in SVRF comments
  - Update of tiling algorithm to avoid GR3T17 DRC errors during EMET generation

- SRAM changes :
  - Support of new RF0251BB and ROM LVT Bitcells

- Virtuoso Library changes :
  - Support of back-annotation on vnpn, varactors and inductors
  - Inductor callback improvement
  - UpdateCDF procedure improvement for resistor netlisting
  - Fix of gatespacing parameter netlisting for macro-FETs
  - Addition of pcells for ESD devices (RPO mosfets)
  - Min and max dimension checks improved for resistors
  - RuleSet selection has now to be selected from Expert parameter
  - Fix of T3 ruleSet in case of length = 34nm
  - Poly Contact option removal
  - Default value added for Wf in case of FingerWidth
  - Macro-Devices improvements :
    - Fix of Radio buttons parameters
    - Back-Annotation Support

- Simulation changes :
  - Improvement of stress effect in case of asymmetric sa/sb configurations for SG and EG transistors
  - Removal of self-heating from soa checks
  - Update EG reliability model to have 10% degradation end of life
  - Resistor SOA on self-heating: fix bug when s > 1
  - CMOM SOA bug fix : removal of false warnings
  - Bug fix on ESDBC corner: corners will be reduced
  - Change to new hspice version to improve simulation runtime in some configurations

- BULKCHECKER changes :
  - Correction of compilation error in rule net_pRVTSRAM_pRVT

- PEX changes :
  - VPS is not more supported and replaced by Voltus-FI.

Change in Version 2.5 released on 16-05-2014 w.r.t Version 2.4.2

- Devices and technology changes :
  - Addition of new EG2 transistors :
    - egnfet2
    - eglvtnfet2
  - Addition of new Vertical NPN bipolar:
    - vnpn
  - Addition of new EG Atto-Farrad varactor:
    - cvar_eg_atto
  - Addition of new ESD devices:
    - esdegnfet2_fdsoi
    - esdeglvtnfet2_fdsoi
    - esdegpfet_fdsoi
    - esdeglvtpfet_fdsoi
    - esdegvpfet_fdsoi
    - esdegvlvtpfet_fdsoi
    - esdpfet_fdsoi
    - esdlvtpfet_fdsoi
    - esdegvnfet_fdsoi
    - esdegvlvtnfet_fdsoi
    - sblkpdres_fdsoi

- SRAM changes :
  - Addition of BRL memcell_rf0298_LL_28SOI v1.1
  - Please refer to dedicated BRL section for the full list of supported BRLs.

- DRC changes :
  - DRC is aligned on DRM 28FDSOI rev 0.3.4
  - MOB exclusions for density checks
  - Straps definition correction
  - NGATE mask and boolean rules removal
  - Specific SRAM redundancy rule for 120um2 bitcells
  - High voltage management 5V/8V and related rules
  - NW and Vx spacing rule for different nets related to strap definition correction
  - RX/PC spacing rules for 1V5 and 1V8
  - Update of GR203c rule code

- Addition of EG2 rules
- Update of NLDDIO2/ NLDDGO2 boolean rules
- Update of MACC rules
- Update of ESDI.R.3 and ESDI.D.6 rules
- Fix of ST_102_or rule
- Support of BRL flow with PVS

- FILL changes :
  - Removal of NGATE exclusion
  - Updated IP-tiling targets
  - Update of RX fill spacing rule (0.3um to 0.4um) to be consistent with DRC rule DRX.S.1
  - Support of RTA GO2 fill transistor

- Virtuoso Library changes :
  - **Techfile updates and fixes** to improve VSR/DRD capabilities and ensure compliancy with new IC616 virtuoso version
  - Pcells have been updated to provide **DRC clean configurations**
    - New Rulesets have been implemented for this purpose (EXTENDED_T3, EXTENDED_EG, NW_EG_extensions, NW_extension_OD)
  - Addition of new categories of standard vias (*s)
  - Dimensions of parasitic diodes are now editable on schematic
  - Fix of T3 backplane on opreres pcell
  - Addition of views for accurate level simulation
  - **Update of callbacks** on resistors and EG poly capacitors
  - Addition of ruleSet CA_PITCH_126
  - Fix of pgtext cell to avoid DRC error
  - Update of middle-path of inductors
  - Back-Annotation improvements

- Models and simulation changes :
  - SG gate current model in strong overdrive update (1.1V up to 2.5V)
  - Local Layout Effects model update for EG (Well Proximity Effect and LOD=STI stress)
  - Creation of **accurate_rgate simlevel** for MOS EG and SG
  - SRAM TCAM711 and DP316 model updates
  - Poly resistors statistical model update
  - Poly resistors accurate model update
  - Removal of useless instance parameters
  - **Finesim** simulator is no more supported

- First support of **AFS** and **Goldengate** simulators

- LVS and PEX changes :
  - Improvement of connectivity check of fill layers
  - ERC-based rules for reduced runtime
  - Several bug fixes :
  - WPE parameters extraction under Accurate marker
  - Shielded CMOM extraction
  - Parasitic management of M1 over poly capacitors
  - New StarRC version prevents extraction failure due to diffusion resistance extraction in some configurations
  - Fix of coupling capacitance extraction to isolated-pwell with QRC
  - First support of **VPS** (EM / IR drop)

- Mentor Fast-XOR is now supported.
  - Please refer to the related documentation for more details $DKITROOT/doc/Manuals/DKShared/calibrerun_10_00_00.pdf

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Mentor Graphics		Tool : Eldo Required license : eldo Tool : AFS Required license : AFS
cadence	Tool: IC616 Required licenses : 111, ADE L/XL, VSE L/XL Optional license for LDE : Virtuoso_Variation_Analysis_Op	Tool : Spectre (mmsim) Required license : Virtuoso_Multi_mode_Simulation
SYNOPSYS		Tool : Hspice Required license : hspice Tool : xa Required license : xa
KEYSIGHT TECHNOLOGIES		Tool : Goldengate Required license : goldengate Tool : ADS Required license : ADS
MunEDA		Tool : Wicked Required license : wicked

EDA vendor	DRC	LVS	TILING
Mentor Graphics	Tool : Calibre Required licenses : calibrehdrc, calibreqdb Optional license for RealTime : calrealtime	Tool : Calibre Required licenses : calibrehlvs, calibrelvs, calibreqdb Optional licenses for PLS : calibreci, calibreadp	Tool : Calibre Required licenses : calibredrc, calibrehdrc, calyieldenhance, caldesignrev
cadence	Tool : PVS Required licenses : Phys_Ver_Sys_DRC_XL Phys_Ver_Sys_Results_Mgr Optional license for iPVS : Virtuoso_DRC_Opt Optional license for waiver flow : Phys_Ver_Sys_Design_Ana	Tool : PVS Required licenses : Phys_Ver_Sys_LVS_XL Phys_Ver_Sys_Results_Mgr Optional license for Interactive Short Locator: Phys_Ver_Sys_Int_Short_Loc_Opt Optional license for signature: Phys_Ver_Sys_Adv_Device Optional license for derived layer viewer: Phys_Ver_Sys_Design_Ana	Tool : PVS Required licenses : Phys_Ver_Sys_DRC_XL, Phys_Ver_Sys_Adv_Ana_Opt,Layout_Data (K2_viewer)

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