

# Analog Flow PDK 28FDSOI

M3- Parasitic Extraction

**FD-SOI**

CMOS & Derivative PDK



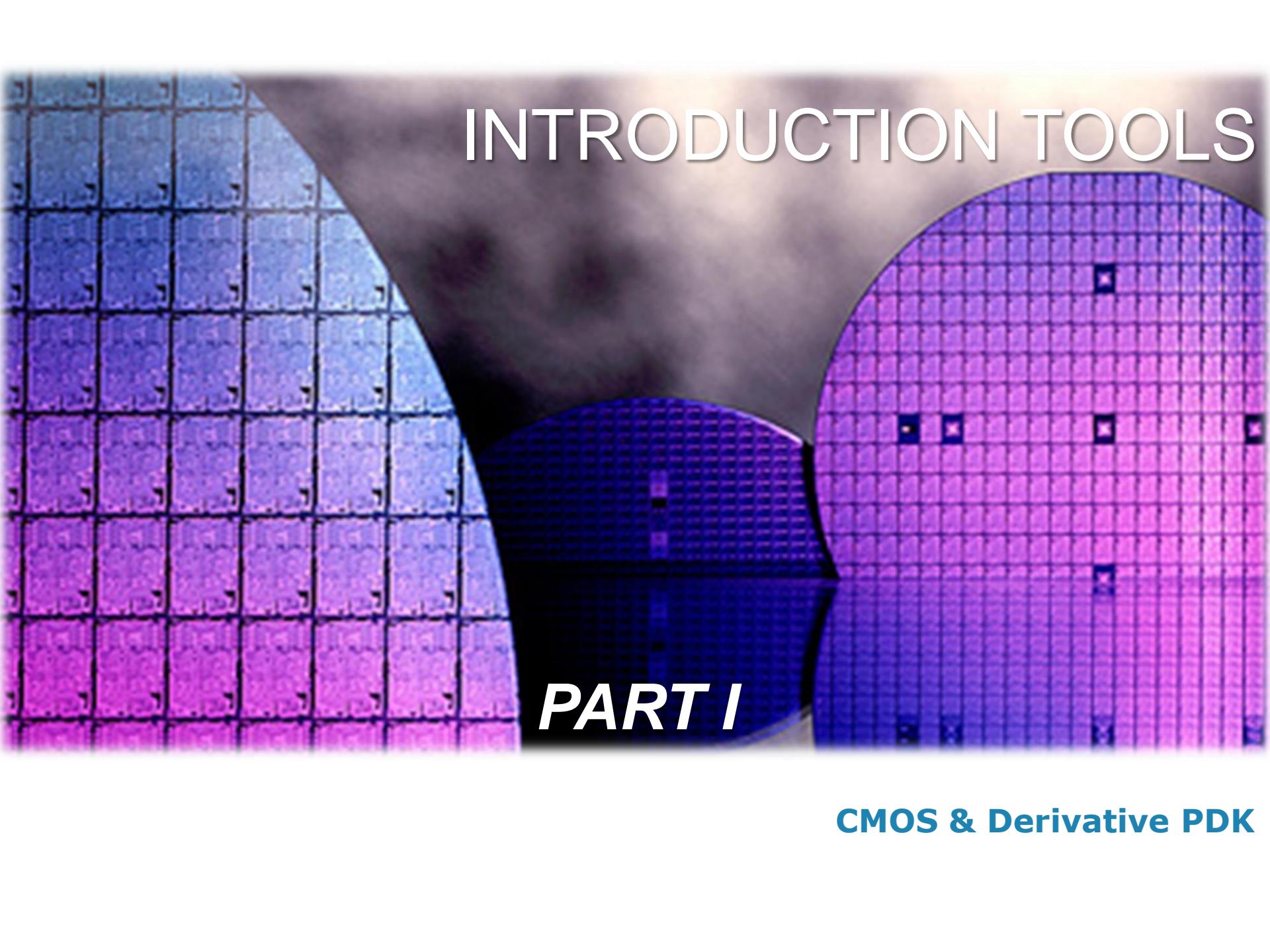


- Identify the layout extraction flows
- Configure the PLS extraction settings
- Perform parasitic extraction



# AGENDA





# INTRODUCTION TOOLS

*PART I*

**CMOS & Derivative PDK**

Intro Tools

PLS Flow



- PLS acronym for Post Layout Simulation
- Be able to run PLS Flow with :
  - Star-RCXT
  - Cadence QRC



- Choose adapted PLS Extraction settings

Intro Tools

PLS Flow



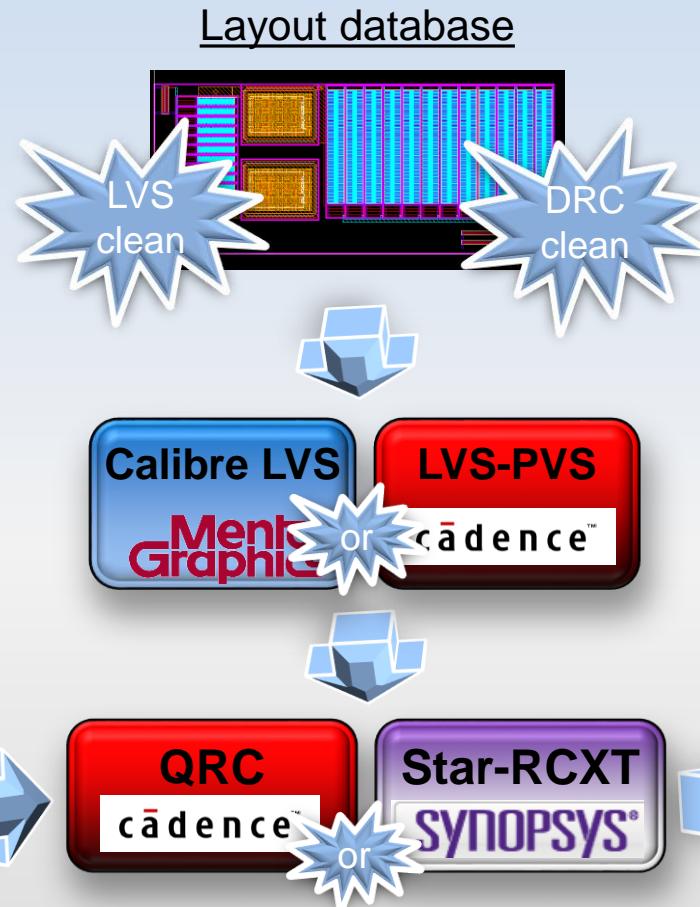
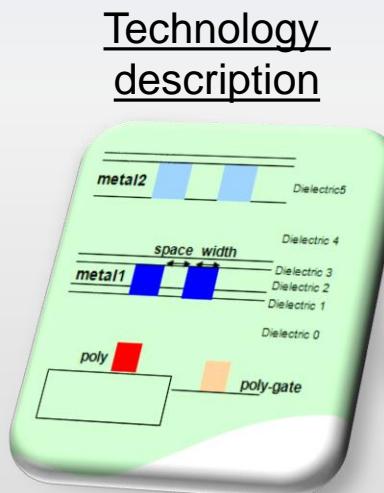
- Interconnects = Wires used to connect devices
  - Described as ideal connections at schematic level
  - Described as metal shapes in the layout
  - Interconnects present electrical losses that need to be taken into account during performances estimation
- Interconnects model
  - Electrical models based on resistances, capacitances and inductances including coupling elements
  - Electrical Models Based on inductances ( QuantusQRC)

# INTRODUCTION TOOLS

*Tools and Flow*

**CMOS & Derivative PDK**

# PLS Flow Overview

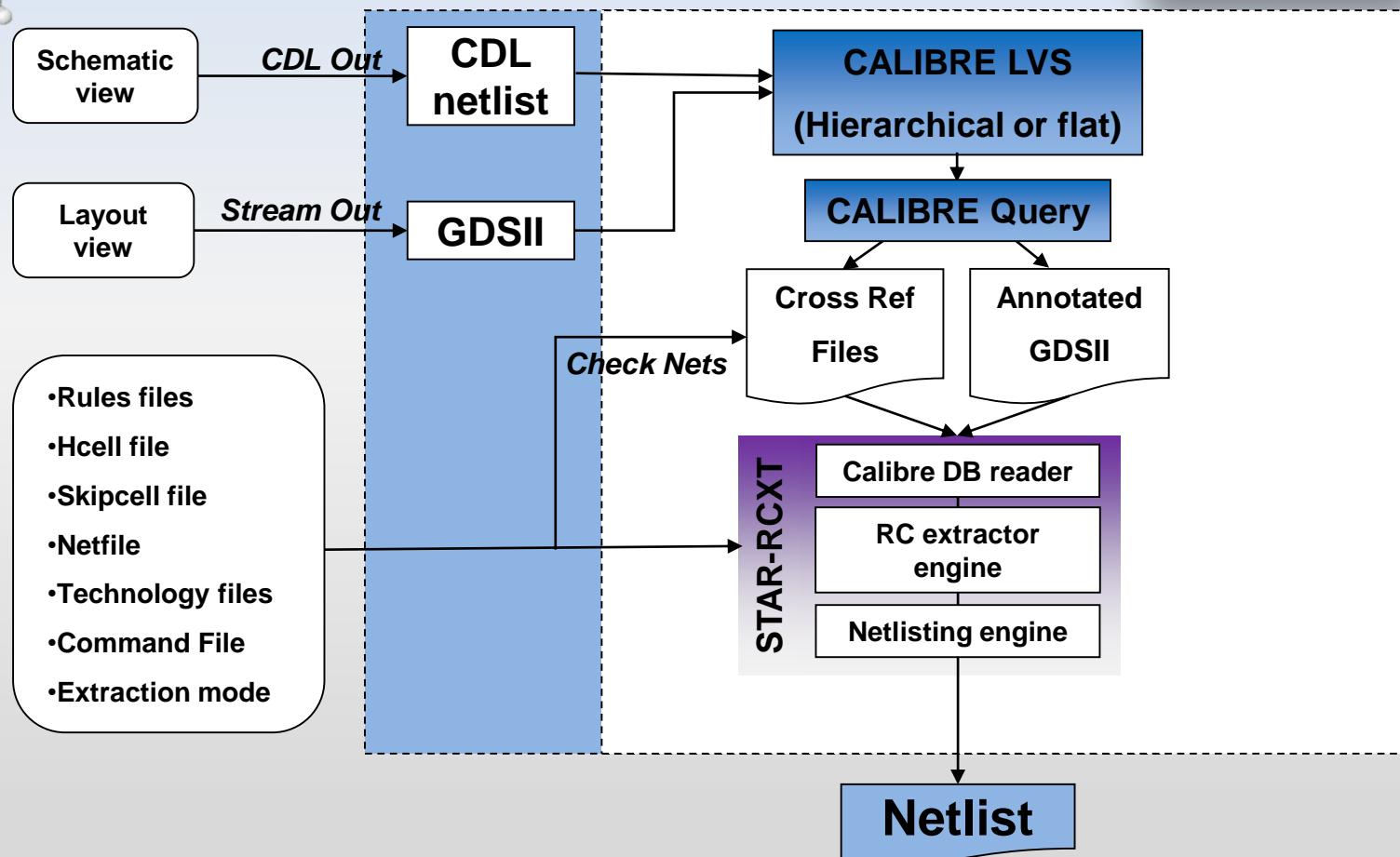


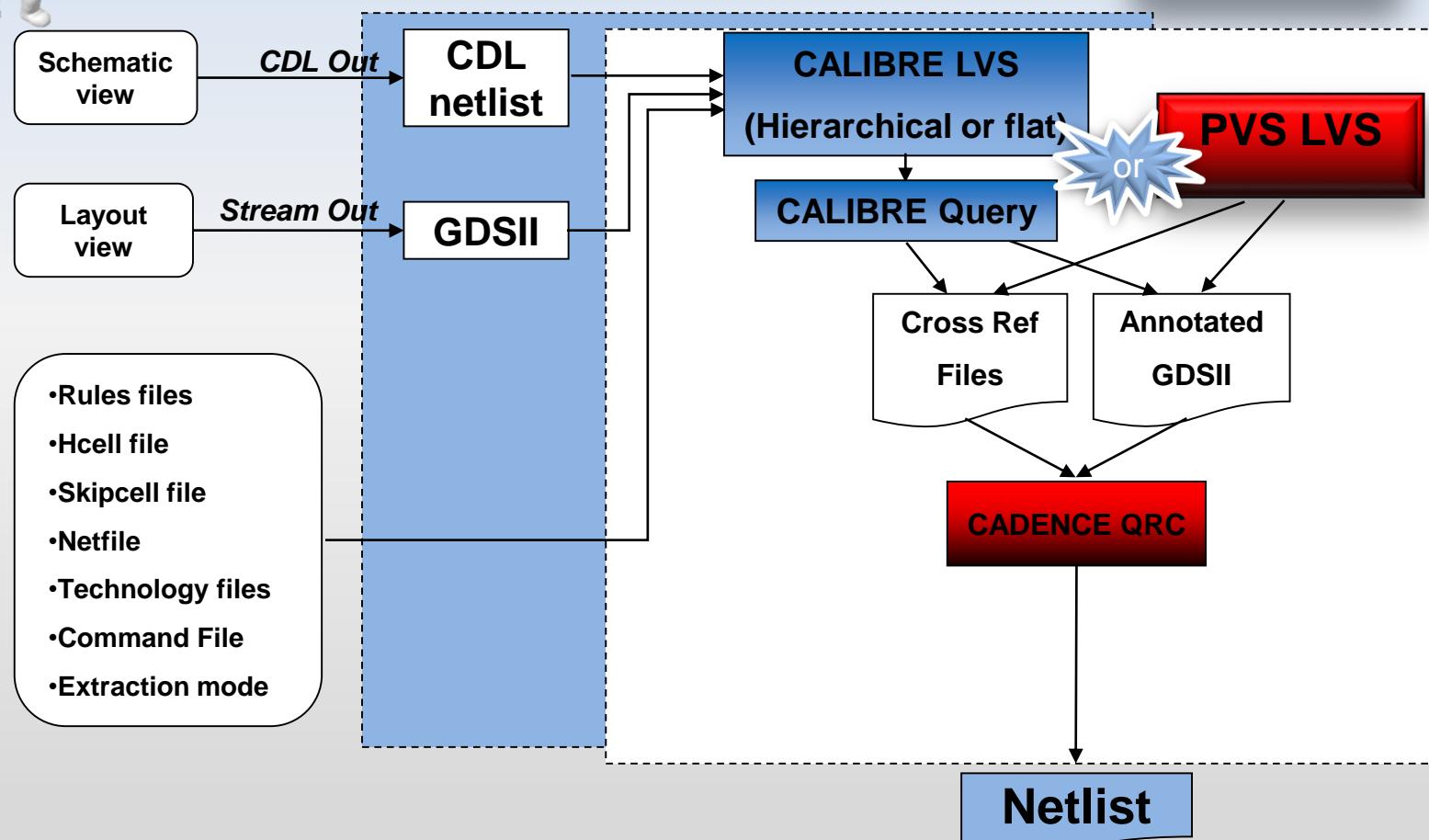
## NOTE

Main differences between LVS & LVS for PLS

- No ERC checks
- Parasitic Diode extraction
- Layout dependant parameters

# PLS Flow overview with Star-RCXT





Intro Tools

PLS Flow



For LVS part

**Calibre**  
**pvs**Mentor Graphics  
Cadence

For extraction part

**Star-RCXT**  
Or **QRC**Synopsys  
Or Cadence**Opus** to get all integrated features

Cadence

**PDK** for all techno dependant files

STMicroelectronics

**Simulator** eldo/spectre/hspice/ADS/...

Use recommended Versions (PDK Release Notes)

# INTRODUCTION TOOLS

*Extraction Mode*

**CMOS & Derivative PDK**

Intro Tools

PLS Flow



- Full chip extractors are based on Pattern Matching approach
  - Pre-computed analytical RCmodels on a basic patterns library
  - RC extraction starts by the parsing of a design parsing to identify basic patterns and apply the analytical models



- For capacitances computation
  - Line's width, length and space (drawing)
  - Conductor thickness
  - Dielectric's thickness and permittivity
  
- For resistances computation
  - Line's width and length (drawing)
  - Conductor sheet resistance (function of Silicon width if applicable)
  - Conductor temperature coefficient (if applicable)



<b>ST</b>	<b>Definition</b>	
Nominal	typical values for all C's and R's	Process target
FuncCmin	best C's, worst $R_{\text{wire}}$ and best $R_{\text{via}}$	-3 $\sigma$ on BEOL parameters
SigCmin		3 $\sigma$ on output RC
FuncCmax	worst C's, best $R_{\text{wire}}$ and worst $R_{\text{via}}$	+3 $\sigma$ on BEOL parameters
SigCmax		3 $\sigma$ on output RC
FuncRCmin	worst lateral C and best R's	-3 $\sigma$ on BEOL parameters
SigRCmin		3 $\sigma$ on output RC
FuncRCmax	best lateral C and worst R's	+3 $\sigma$ on BEOL parameters
SigRCmax		3 $\sigma$ on output RC



## **noRC**

Check devices netlist validity

- More useful for critical design
- to highlight WPE parameters
- Recommended before any other extraction mode

Impact of extra devices : diodes

Impact of extra parameters :  
as;ad;ps;pd;po2act ...

## **C**

Net-to-ground coupling

Filtering for very small capacitances

## **R**

Net resistances

## **Cc**

Net-to-net coupling

Threshold to lump small cap vs grounded cap

## **RC**

Sub node-to-ground coupling

## **RCc**

Subnode-to-Subnode coupling



## Mixed Cc\_RCc

All nets are extracted with Cc  
Resistor is extracted for the subset of nets given in netfile

Specific Mixed mode dedicated to RF most used applications

## Mixed

Combines the 6 first modes

## FS extract

Field solver extraction mode

Coupling capacitances only  
Dedicated to a very limited number of nets  
Accurate but slow!

- No more RC models
- Basic patterns matching
- Directly extraction from ITF with the Field Solver tool: extract only coupling capacitor
- More accurate but not with big design because very long

# POST LAYOUT SIMULATION - FLOW

**PART II**

**CMOS & Derivative PDK**

# POST LAYOUT SIMULATION - FLOW

*Start RCXT*



**CMOS & Derivative PDK**



- Refer to the README documentation:
  - `$PDKROOT/DATA/PEX/STAR/README`
- LVS for PEX
  - `$PDKROOT/DATA/PEX/STAR/LVS_pex.ctrl`
    - Retrieve and copy the file in the working directory
    - Update it with the appropriate gds path and Topcell name “myCell” fields to changed
- Launch calibre LVS
  - `calibre -hier -lvs LVS_pex.ctrl > lvs_star.log`

Intro Tools

PLS Flow



- Refer to the README documentation:
  - `$PDKITROOT/DATA/PEX/STAR/README`
  
- `mkdir AGF`
  - `cp $PDKITROOT/DATA/PEX/STAR/calibrestarrcxt.query.ctrl .`
  - Update `calibrestarrcxt.query.ctrl`
    - replace `myCell` by your actual design cell
  - Launch `calibre query`:
    - `calibre -query svdb < calibrestarrcxt.query.ctrl >& calibre_ci.log`
  
- **`cp $PDKITROOT/DATA/PEX/STAR/starrcxt.cmd`**
- Update `starrcxt.cmd` as follows :
  - replace `myCell` by your actual design cell
  - replace `CORNER` by the required extraction corner (`FuncCmax FuncCmin FuncRCmax FuncRCmin nominal`)
  - replace `PDKITROOT` by the actual path defined by the value of `$PDKITROOT`
  - select the proper options for the required output format (Transistor DSPF or extracted view)
  
- Launch: **`StarXtract -clean starrcxt.cmd >& starRCXT.log`**

# POST LAYOUT SIMULATION - FLOW

**QRC**



**CMOS & Derivative PDK**

Intro Tools

PLS Flow



- Refer to the README documentation:
  - \$PDKITROOT/DATA/PEX/QRC/README
- LVS for PEX
  - \$PDKITROOT/DATA/PEX/QRC/calibreqrc.ctrl
    - Retrieve and copy the file in the working directory
    - Update it with the appropriate gds path and Topcell name “myCell” fields to changed
- Launch QRC LVS
  - `calibre -hier -lvs calibreqrc.ctrl >& lvs_qrc.log`

Intro Tools

PLS Flow



- Refer to the README documentation:
  - `$PDKITROOT/DATA/PEX/STAR/README`
  
- `mkdir AGFLVS`
  - `cp $PDKITROOT/DATA/PEX/QRC/calibreQRC.query.ctrl.`
  - Update `calibreQRC.query.ctrl`
    - replace myCell by your actual design cell
  - Launch `calibre query`:
    - `calibre -query svdb < calibreQRC.query.ctrl >& calibre_ci.log`
  
- `cp $PDKITROOT/DATA/PEX/QRC/qrc.ccl`
- Update `qrc.ccl` as follows :
  - replace myCell by your actual design cell
  - replace CORNER by the required extraction corner (FuncCmax FuncCmin FuncRCmax FuncRCmin nominal)
- Launch: `qrc -cmd qrc.ccl >& qrc.log`

# POST LAYOUT SIMULATION - FLOW

*PLASMA*

**CMOS & Derivative PDK**

Intro Tools

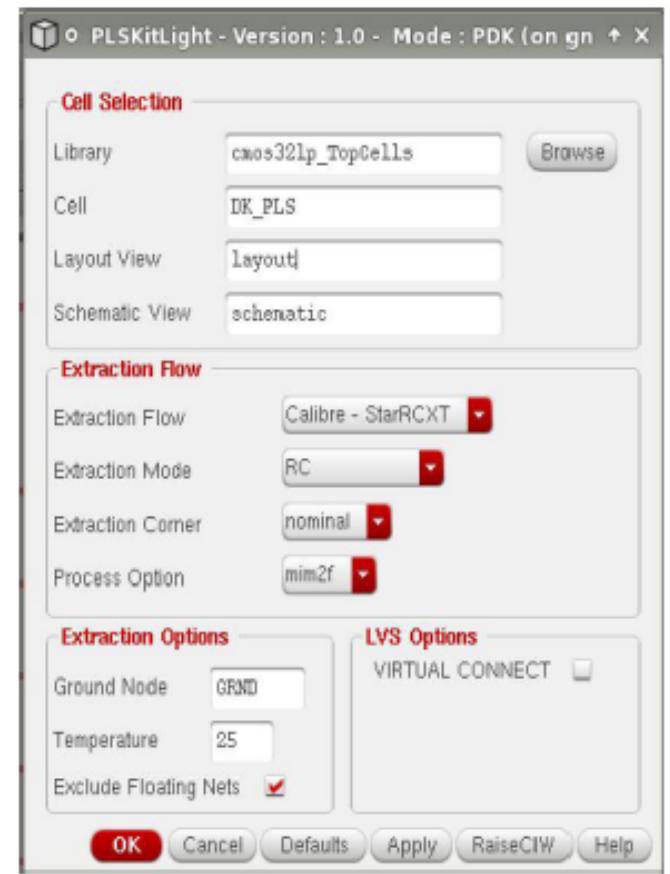
PLS Flow



- PLASMa stands for : [P]ost [La]ayout [S]i[m]ul[a]tion
- Support all major CAD-vendor flows
  - Calibre – StarRCXT
  - Calibre – qRC
  - Calibre – xRC...
- Support only schematic extracted flow
- Can be launched 2 ways:
  - From CIW
  - from virtuoso-layout editor



- Based upon Cyclic Fields for simplicity (1 schematic View at a time)



Intro Tools

PLS Flow



Virtuoso® 6.1.5 - Log: /home/dc43/CDS.log (on gnx5390)

File Tools Options C2 Util CORAIL Help

cadence

```
-- [DKD] : Using "/prj/dkinfra/users/dc43/c28fdsoi_pdk/pdkRegistry.xml" DKD file.
-- Processing PLaSma_Osc
-- Processing PLaSma_Osc - Export GDS [OA]
-- Processing PLaSma_Osc - Cdl Netlist
-- [WARNING] : Loading PDK .sinrc file: "/work/dkdm/upf_prods/upf/PDK_STM_cmos28FDSoI"
-- Processing PLaSma_Osc - LVS - StarRCXT
-- Processing PLaSma_Osc - Query - StarRCXT
-- Processing PLaSma_Osc - StarView [PDK]
-- [WARNING] : Workaround for star-rcxt version : "h-2012.12"
StarRC is running in blocking mode
Running StarRC ...
Please click "View Run Log" to see StarRC summary
StarRC process finished successfully! function RSD_postProc redefined
function dKMKCDL redefined
function PDK_gen_starview redefined

-- [WARNING] : Starview post-processing : RSD_postProc
-- Processing PLaSma_Osc done
-- Start Global tasks
-- [DKD] : PDK Version: 2.4
-- [INFO] : Creating XML_Flow_Report_2.4
-- End of Global tasks
```

mouse L: M: R:

1 >



# PLaSma Outputs

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The screenshot shows the Cadence Library Manager interface. The title bar reads "Library Manager: Directory .../kinfra/users/dc43/c28fdsoi\_pdk (on gnx5390)". The menu bar includes File, Edit, View, Design Manager, and Help. The interface has three main sections: Library, Cell, and View.

- Library:** A list of available libraries:
  - Demo\_PLaSma\_c28fdsoi\_pdk
  - ST\_C32\_addon\_AMS
  - ST\_C32\_addon\_DP
  - aambx
  - aatest
  - analogLib
  - basic
  - cdsDefTechLib
  - cmos28\_emetro
  - cmos32lp
  - cmos32lp\_Tech
  - mgcLib
  - sbalib
- Cell:** A list of cells under the PLaSma\_Osc library:
  - Global\_Report\_2\_4
  - PLaSma\_Osc
  - PLaSma\_Osc\_testbench
- View:** A table showing the contents of the selected cell (PLaSma\_Osc).

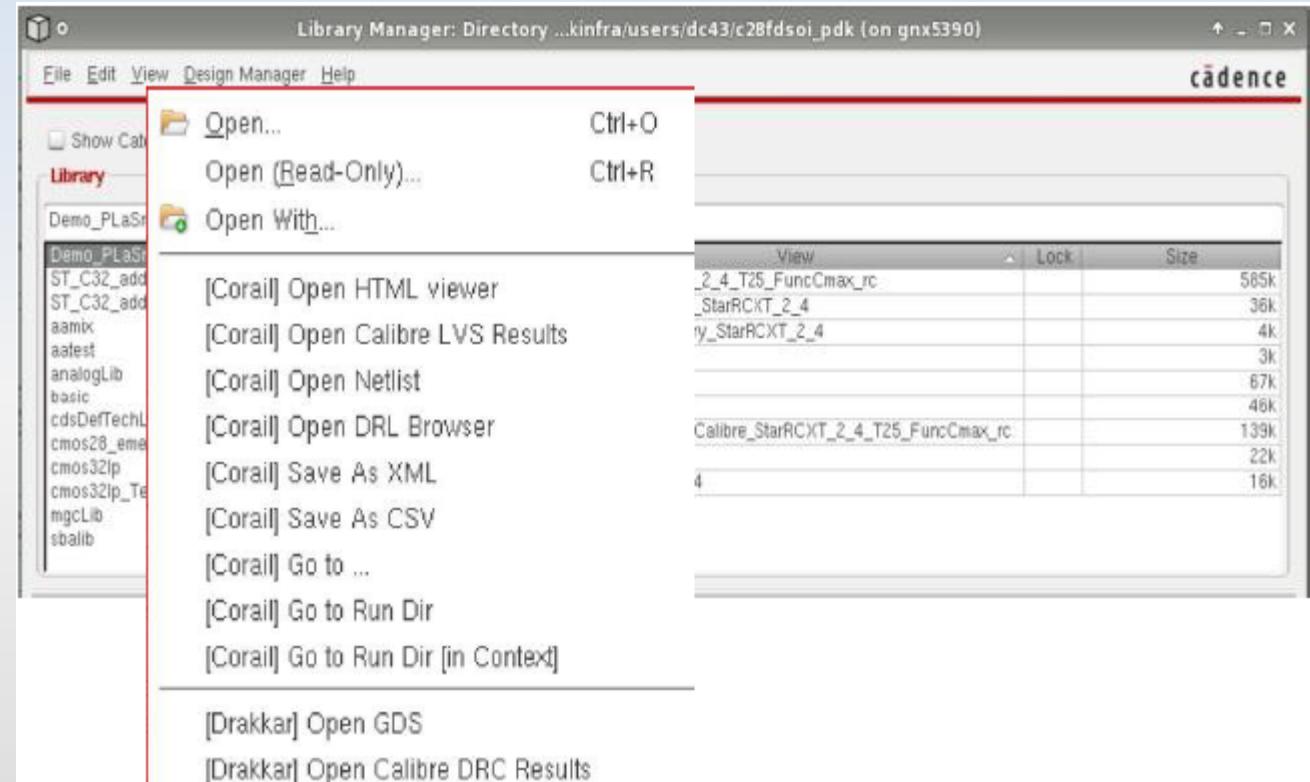
View	Lock	Size
C_starview_2_4_T25_FuncCmax_rc		585k
calibreLVS_StarRCXT_2_4		38k
calibreQuery_StarRCXT_2_4		4k
cell_2_4		3k
layout		67k
schematic		46k
schematic_Calibre_StarRCXT_2_4_T25_FuncCmax_rc		139k
symbol		22k
xstream_2_4		16k

# Library Manager Customization

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Intro Tools

PLS Flow





Intro Tools

PLS Flow



- Output description for Calibre - StarRCXT :
  - xstream\_<PDKversion>
  - cdl\_<PDKversion>
  - calibreLVS\_StarRCXT\_<PDKversion>
  - calibreQuery\_StarRCXT\_<PDKversion>
  - C\_starview\_<PDKversion>\_<Corner>\_<**ProcessOption**>\_<Mode>
- Extracted Schematic View :
  - schematic\_<Flow>\_<Temperature>\_<Corner>\_<**ProcessOption**>\_<Mode>
  - Example : **schematic\_C\_StarRCXT\_T25\_RCMAX\_mim2f\_c**

Note: Negative temperature : T=-25°C → T\_25

Intro Tools

PLS Flow



**Library Manager: Directory ...kinfra/users/dc43/c28fdsoi\_pdk (on gnx5390)**

File Edit View Design Manager Help

cadence

Show Categories Show Files

Library	Cell	View
Demo_PLaSma_c28fdsoi_pdk	Global_Reports_2_4	XML_Flow_Report_2_4
Demo_PLaSma_c28fdsoi_pdk	Global_Reports_2_4	View
ST_C32_addon_AMS	PLaSma_Osc	Lock
ST_C32_addon_DP	PLaSma_Osc_testbench	Size
aamix		3k

Open... Ctrl+O  
Open (Read-Only)... Ctrl+R  
Open With...

[Coral] Open HTML viewer  
[Coral] Open Calibre LVS Results  
[Coral] Open Netlist  
[Coral] Open DRL Browser  
[Coral] Save As XML  
[Coral] Save As CSV  
[Coral] Go to ...  
[Coral] Go to Run Dir  
[Coral] Go to Run Dir [In Context]  
[Drakkar] Open GDS  
[Drakkar] Open Calibre DRC Results

**Flow Results for Library :**

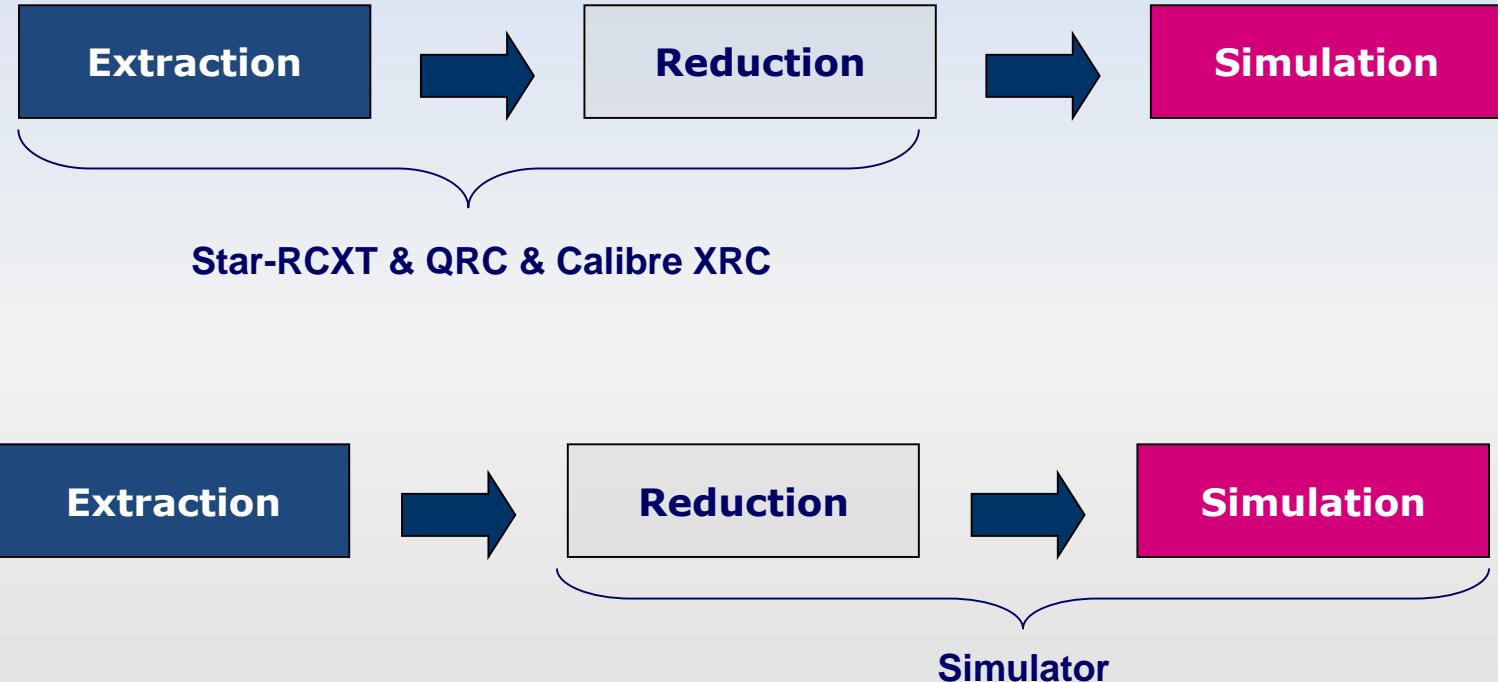
Cell	Tool	Task	Corner	Mode	Warning(s)	Soft Error(s)	Fatal Error(s)	Status
PLaSma_Osc	strmout	streamOut ( 02s )			32	0	0	
	si	cdl ( 03s )			0	0	0	
	calibre	calibreLVSextraction ( 11s )		hier	0	0	0	PASS
	calibre	calibreLVScomparison ( 11s )		hier	0	0	0	PASS
	calibre	calibreQuery ( 15s )			0	0	0	
	StarExtract	C_starview ( 45s )	FuncCmax	rc	21466	0	0	

# POST LAYOUT SIMULATION - FLOW

*LPE Flag*

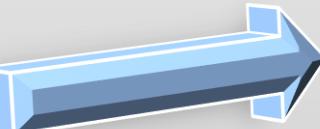
**CMOS & Derivative PDK**

# Reduction in the Post-Layout flow



## Objective:

Decrease the simulation runtime by keeping the best possible accuracy



# LPE Flag values vs. Extraction Modes

Intro Tools

PLS Flow



	Ipe	Body	Access R	Access C
Pre layout or NoRC	1	Model computes gate&CA resistances and capacitances	Model computes M1&CA resistances	Model computes M1&CA capacitances
C or Cc	3	Model computes gate capacitance & resistance <b>PLS computes CA capacitance</b>	Model computes M1&CA resistances	<b>PLS computes M1&amp;CA capacitances</b>
R	2	Model computes gate&CA capacitance <b>PLS computes gate&amp;CA resistances</b>	<b>PLS computes M1&amp;CA resistances</b>	Model computes M1&CA capacitances
RC or RCc	0	<b>PLS computes everything except gate capacitance</b>	<b>PLS computes M1&amp;CA resistances</b>	<b>PLS computes M1&amp;CA capacitances</b>



**Thanks for your Attention**