cmos028fdsoi Technology

PDC vs MC Noise report for RVT models

DK1.1_RF_mmW

Please use the bookmark to navigate

General information on PDC vs MC Noise report for RVT models

- Maximum supply voltage is - V.
- Validity domain is defined as follows:
  - ✔ Drawn gate length varies from 30nm to 10um.
  - ✔ Drawn transistor width varies from 80nm to 10um.
  - ✔ Device temperature varies from -40 °C to 125 °C.

Output parameters definitions

- Model(s): nfet_acc, pfet_acc

nfet_acc
Electrical characteristics per geometry

nfet_acc @ w=20e-6, l=2.0e-6, pre_layout_local=1, nf=4, sa=8.500e-08, sb=8.500e-08, sd=1.140e-07, pcpastrx_top=1.050e-07, pcpastrx_bot=1.050e-07, devtype=PCELLwoWPE, as=4.25e-13, ad=4.25e-13, ps=1.017e-05, pd=1.017e-05, vbs=0, vdd=1, temp=25

	TT_Noisedev=4	TT_Noisedev=0	TT_Noisedev=2	PRO_MC_PARAM_TT_1_MC_AVG-3S	PRO_MC_PARAM_TT_1_MC_AVG	PRO_MC_PARAM_TT_1_MC_AVG+3S
logSi2@1Hz [log10(A²/Hz)]	-18.15	-17.99	-17.82	-18.15	-17.99	-17.82
logSi2ovId2@1Hz [log10(1/Hz)]	-9.55	-9.39	-9.22	-9.55	-9.39	-9.22
logSv2@1Hz [log10(V²/Hz)]	-11.71	-11.55	-11.38	-11.71	-11.55	-11.38

pfet_acc
Electrical characteristics per geometry

pfet_acc @ w=0.30e-6, l=0.030e-6, pre_layout_local=1, nf=1, sa=8.500e-08, sb=8.500e-08, sd=1.140e-07, pcpastrx_top=5.700e-08, pcpastrx_bot=8.000e-08, devtype=PCELLwoWPE, as=2.55e-14, ad=2.55e-14, ps=7.7e-07, pd=7.7e-07, vbs=0, vdd=1, temp=25

	TT_Noisedev=4	TT_Noisedev=0	TT_Noisedev=2	PRO_MC_PARAM_TT_1_MC_AVG-3S	PRO_MC_PARAM_TT_1_MC_AVG	PRO_MC_PARAM_TT_1_MC_AVG+3S
logSi2@1Hz [log10(A²/Hz)]	-16.51	-15.5	-14.48	-16.51	-15.5	-14.48
logSi2ovId2@1Hz [log10(1/Hz)]	-7.11	-6.1	-5.09	-7.11	-6.1	-5.09
logSv2@1Hz [log10(V²/Hz)]	-8.71	-7.7	-6.69	-8.71	-7.7	-6.69

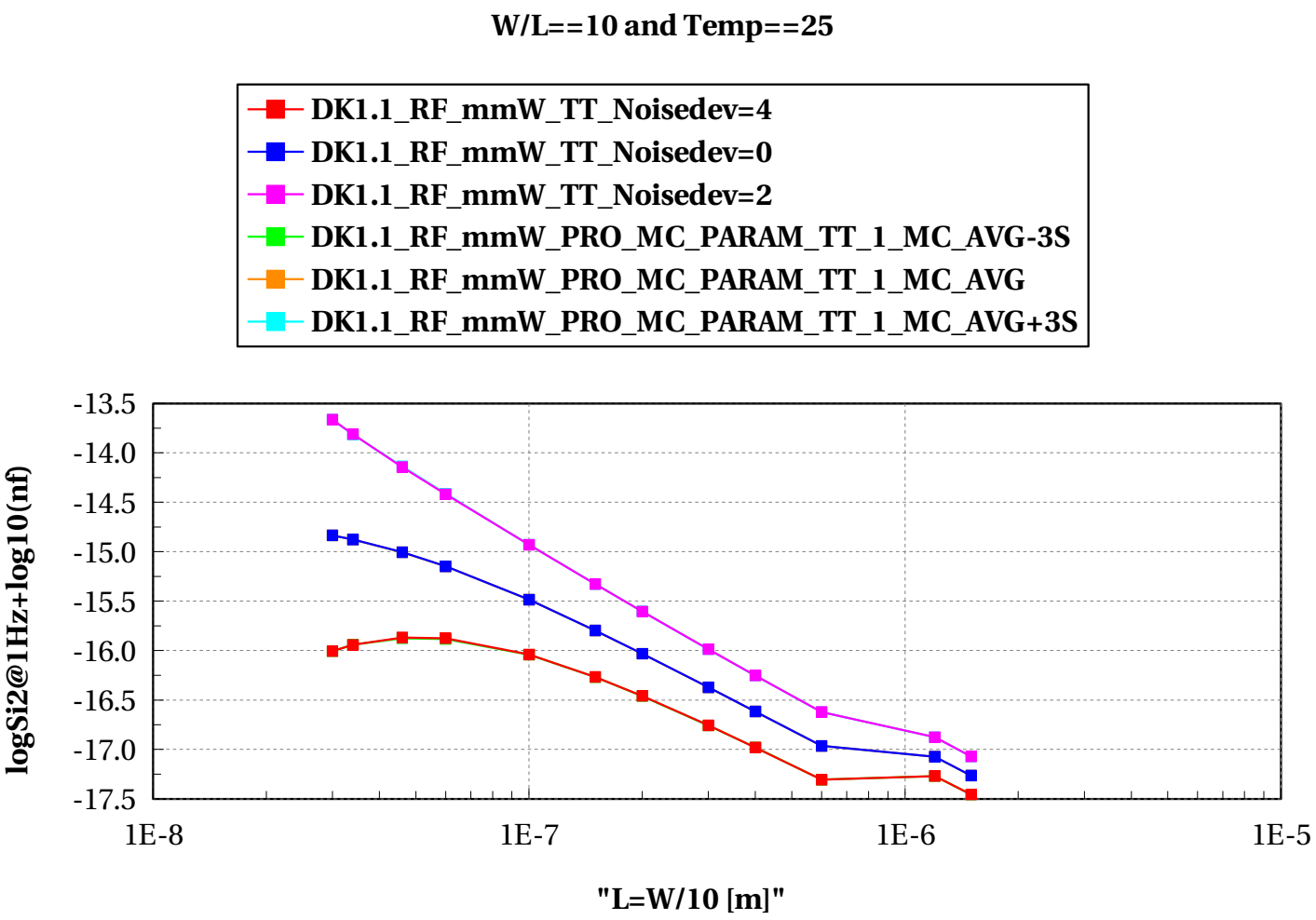
pfet_acc @ w=20e-6, l=2.0e-6, pre_layout_local=1, nf=4, sa=8.500e-08, sb=8.500e-08, sd=1.140e-07, pcpastrx_top=1.050e-07, pcpastrx_bot=1.050e-07, devtype=PCELLwoWPE, as=4.25e-13, ad=4.25e-13, ps=1.017e-05, pd=1.017e-05, vbs=0, vdd=1, temp=25

	TT_Noisedev=4	TT_Noisedev=0	TT_Noisedev=2	PRO_MC_PARAM_TT_1_MC_AVG-3S	PRO_MC_PARAM_TT_1_MC_AVG	PRO_MC_PARAM_TT_1_MC_AVG+3S
logSi2@1Hz [log10(A²/Hz)]	-18.95	-18.71	-18.48	-18.95	-18.71	-18.48
logSi2ovId2@1Hz [log10(1/Hz)]	-9.56	-9.32	-9.08	-9.56	-9.32	-9.08
logSv2@1Hz [log10(V²/Hz)]	-11.6	-11.36	-11.12	-11.6	-11.36	-11.12

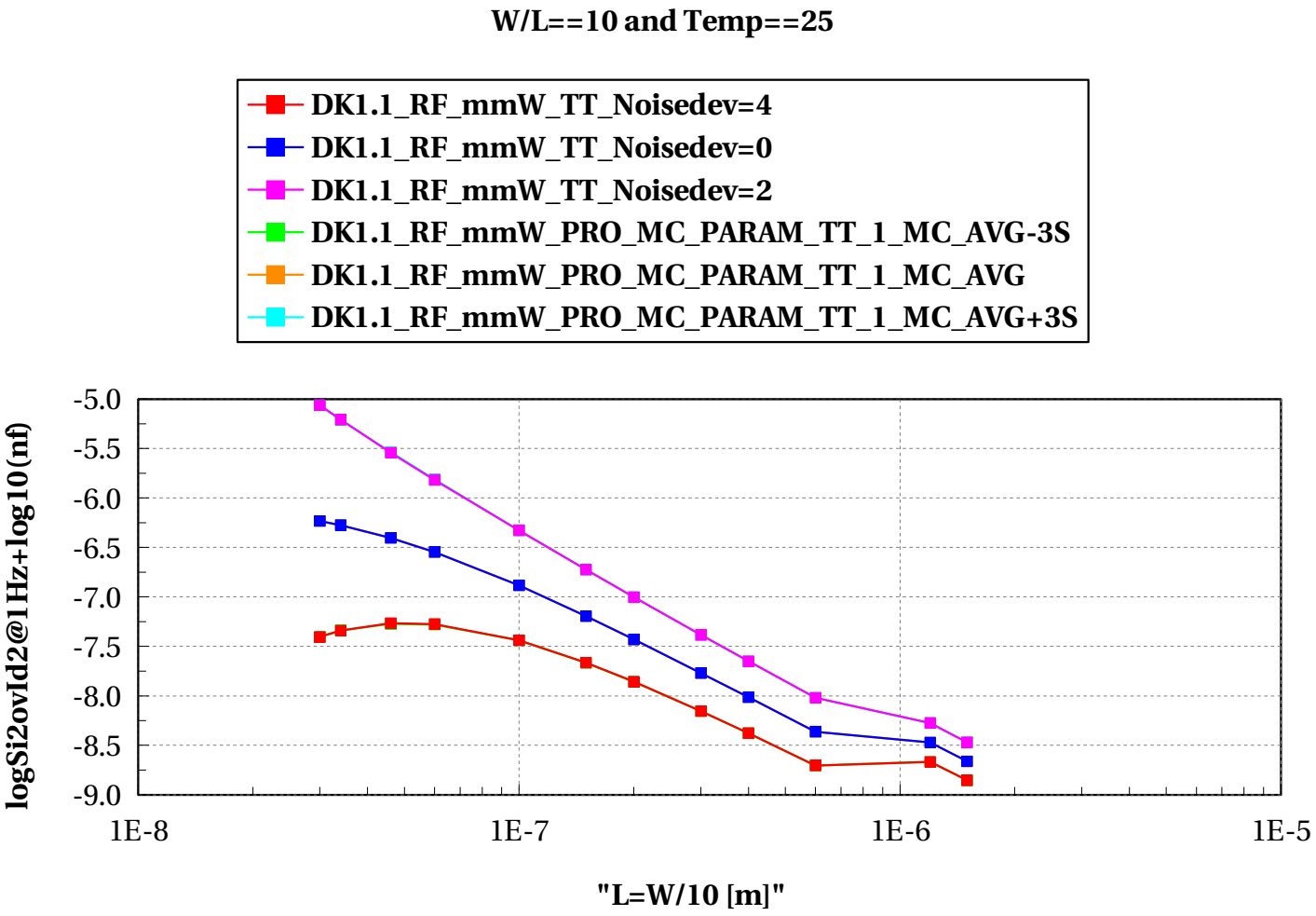
nfet_acc
Electrical characteristics scaling

Scaling versus Length @ W/L=10 and W/NF<5e-6

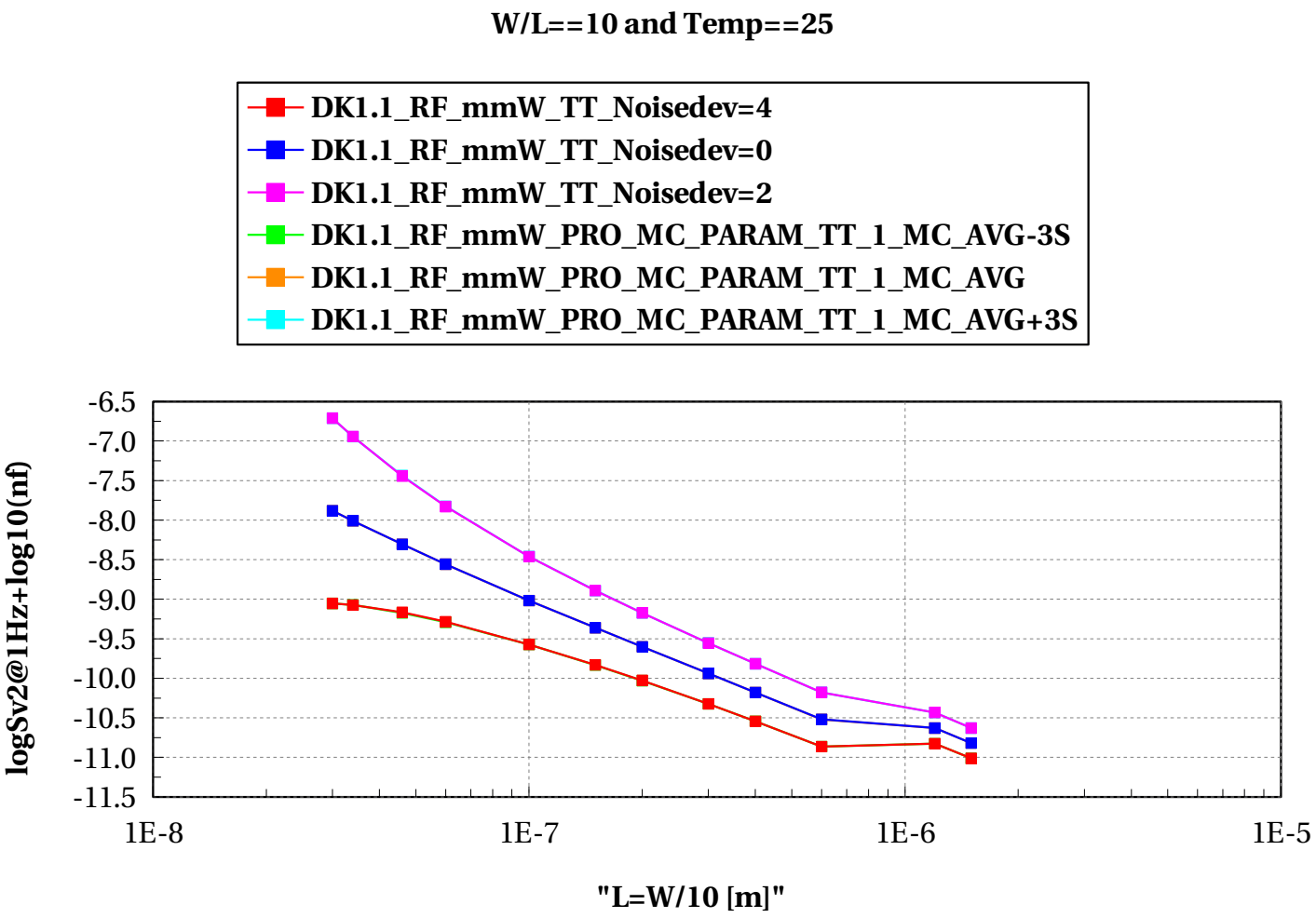
nfet_acc, logSi2@1Hz+log10(nf) vs "L=W/10 [m]"



nfet_acc, logSi2ovId2@1Hz+log10(nf) vs "L=W/10 [m]"



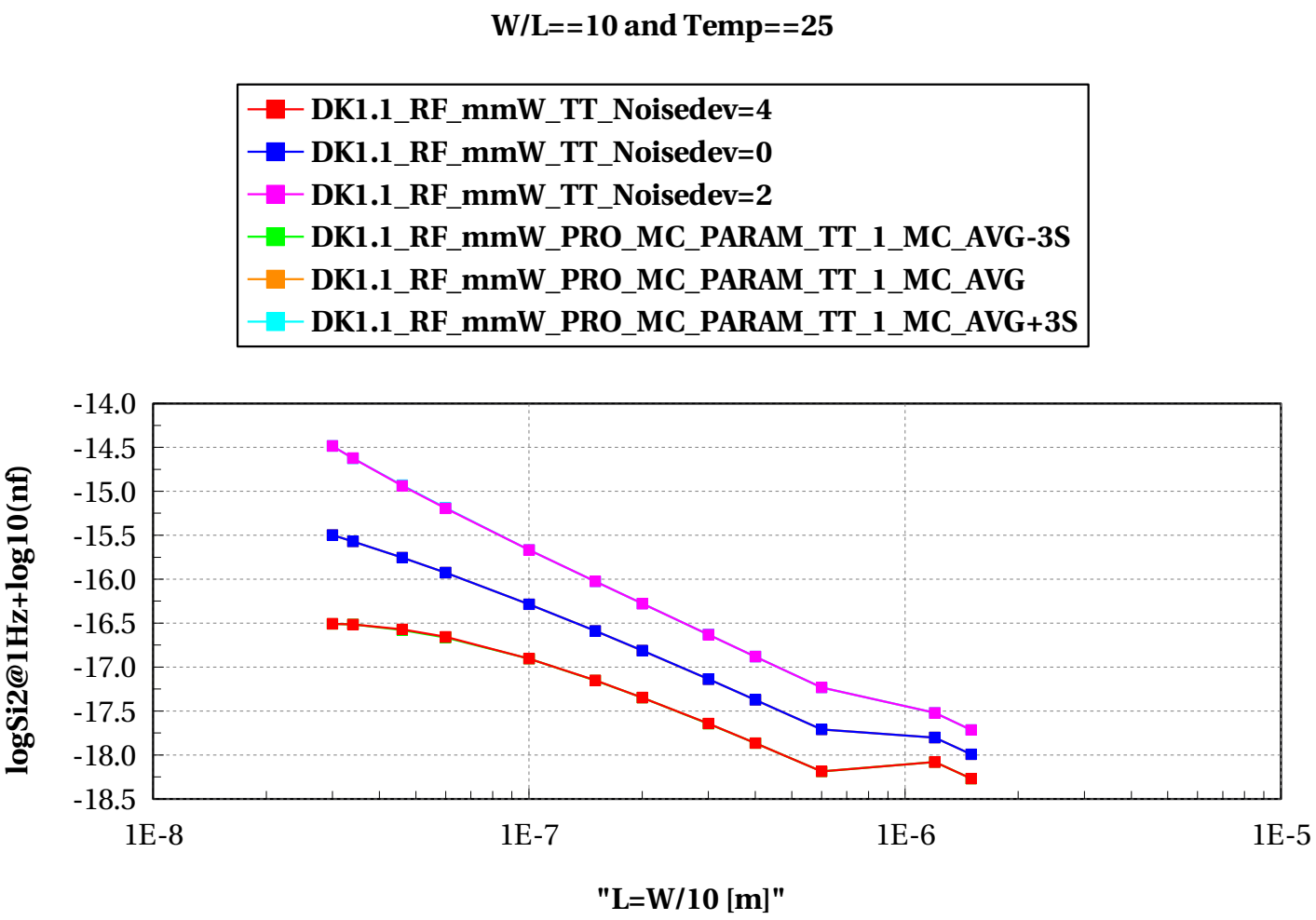
nfet_acc, logSv2@1Hz+log10(nf) vs "L=W/10 [m]"



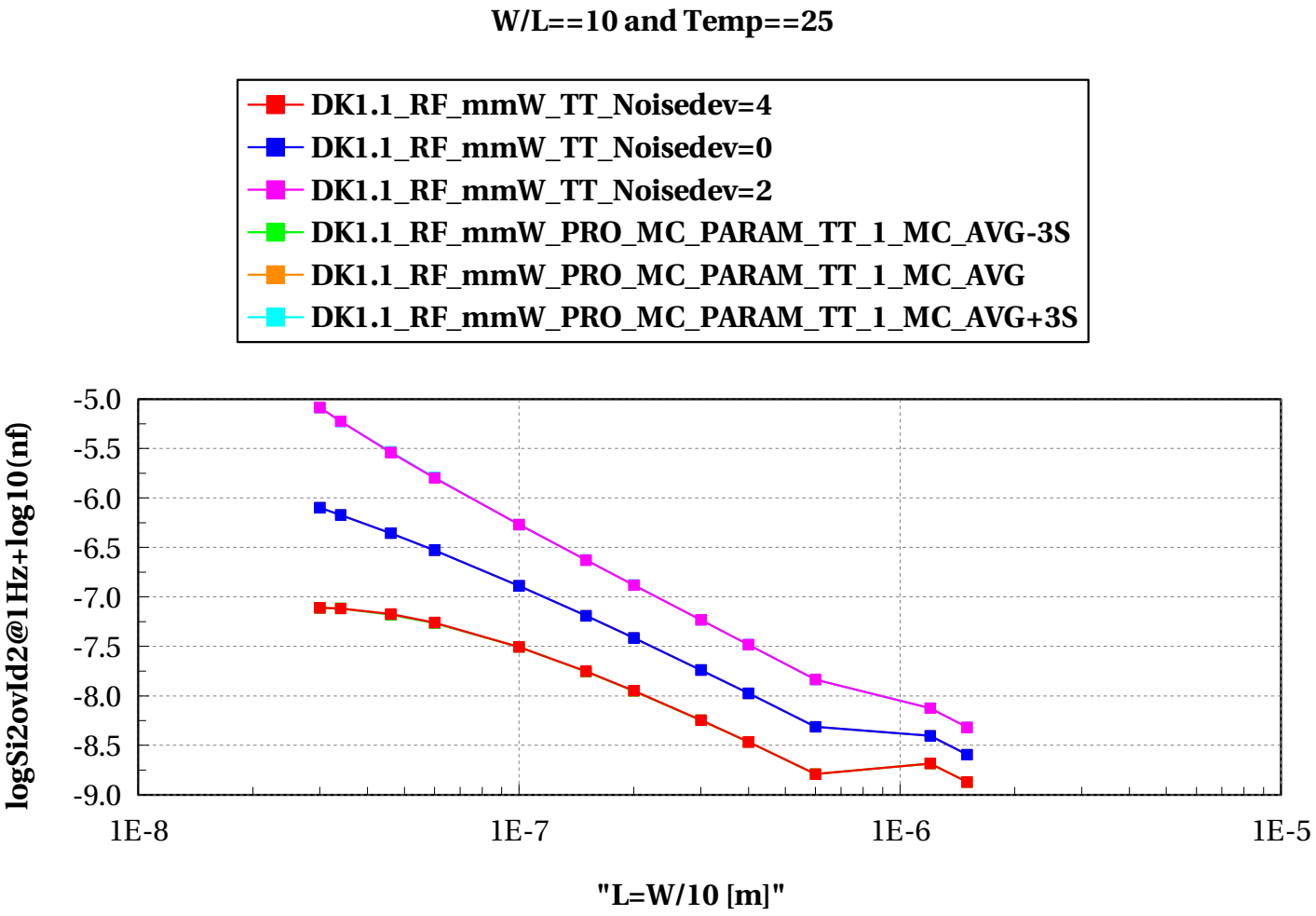
pfet_acc
Electrical characteristics scaling

Scaling versus Length @ W/L=10 and W/NF<5e-6

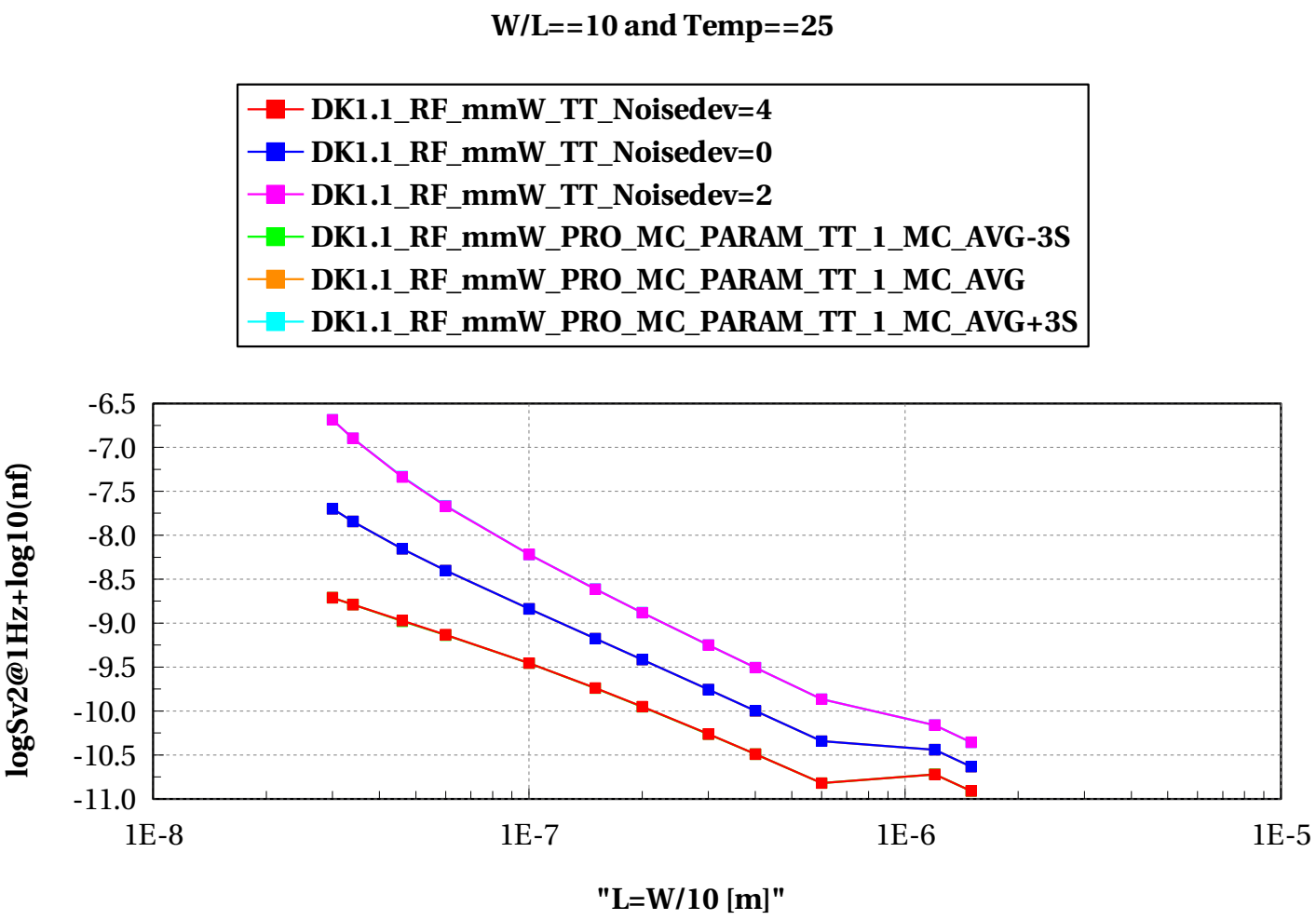
pfet_acc, logSi2@1Hz+log10(nf) vs "L=W/10 [m]"



pfet_acc, logSi2ovId2@1Hz+log10(nf) vs "L=W/10 [m]"



pfet_acc, logSv2@1Hz+log10(nf) vs "L=W/10 [m]"



Annex

Conditions of simulations

The simulations were done with SBenchLSF Alpha using Eldo simulator 2018.3.

- Model nfet_acc (DK1.1_RF_mmW)
  - ✔ Input Parameters
    - ✘ ams_release = 2018.3
    - ✘ mc_runs = 500
    - ✘ iana = 5e-6 A
    - ✘ temp = 25 °C
    - ✘ mc_sens = 0
    - ✘ f_ext = 100k Hz
    - ✘ sbenchlsf_release = Alpha
    - ✘ vbs = 0 V
    - ✘ model_version = 1.2.c
    - ✘ vds_ana = Vdd/4 V
    - ✘ mc_nsigma = 3
    - ✘ vdd = 1 V
  - ✔ Sweep Parameters
  - ✔ Extra parameters

- ✘ rvt_dev = 0

- Model pfet_acc (DK1.1_RF_mmW)
  - ✔ Input Parameters
    - ✘ ams_release = 2018.3
    - ✘ mc_runs = 500
    - ✘ iana = 2e-6 A
    - ✘ temp = 25 °C
    - ✘ mc_sens = 0
    - ✘ f_ext = 100k Hz
    - ✘ sbenchlsf_release = Alpha
    - ✘ vbs = 0 V
    - ✘ model_version = 1.2.c
    - ✘ vds_ana = Vdd/4 V
    - ✘ mc_nsigma = 3
    - ✘ vdd = 1 V
  - ✔ Sweep Parameters
  - ✔ Extra parameters
    - ✘ rvt_dev = 0