C28SOI_SC_12_CORE_LR
Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells

Overview

- C28SOI_SC_12_CORE_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

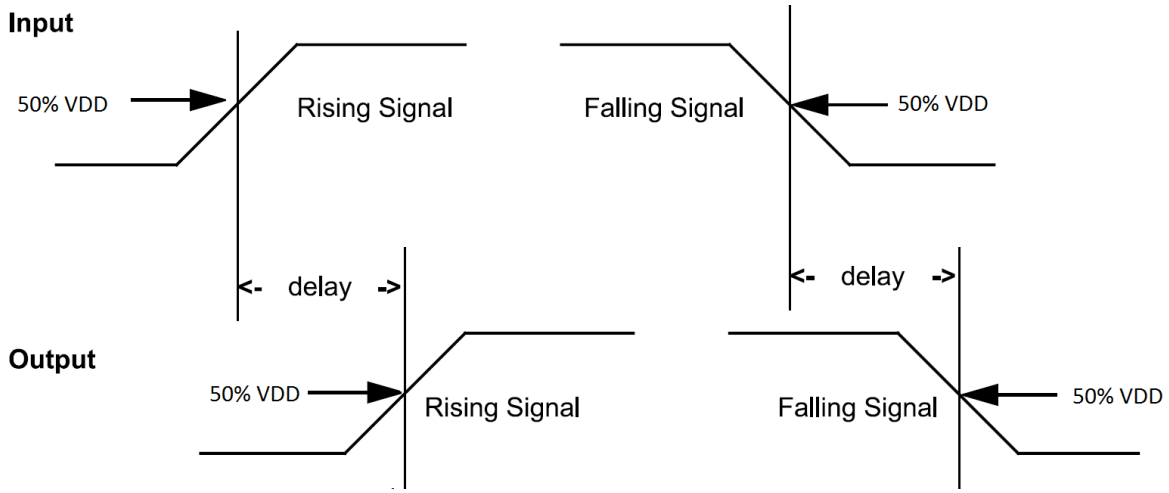


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

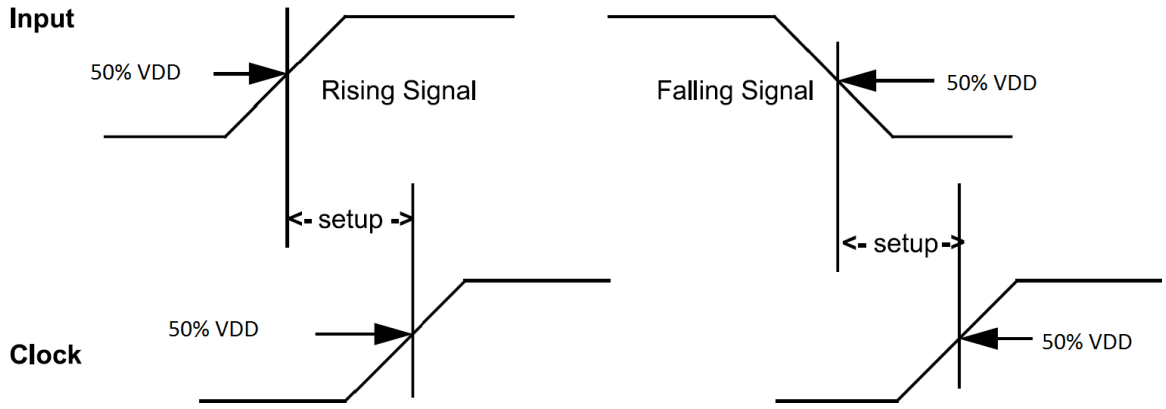


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

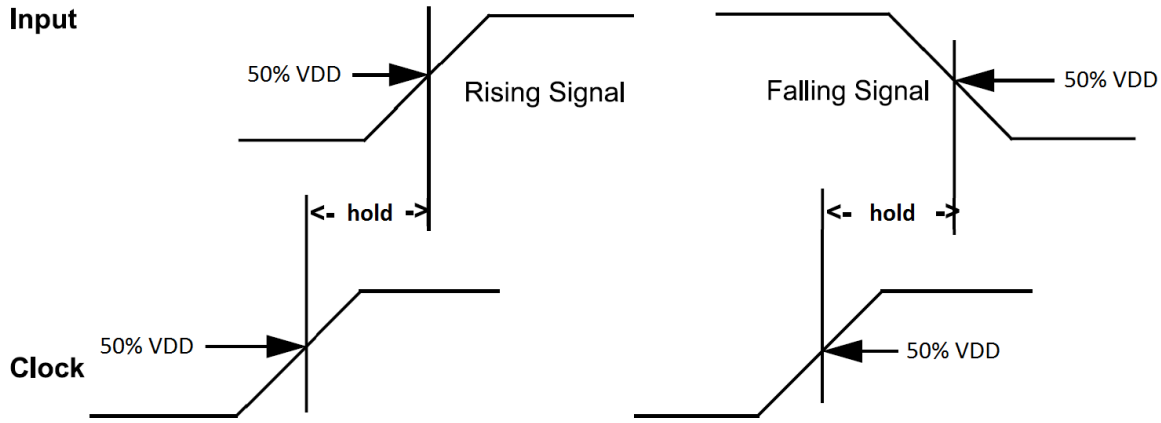


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

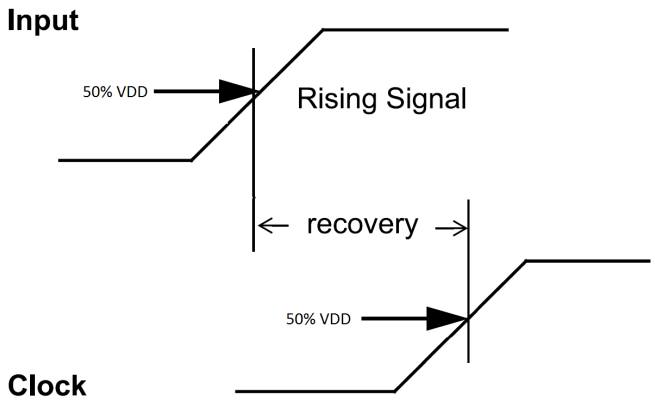


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

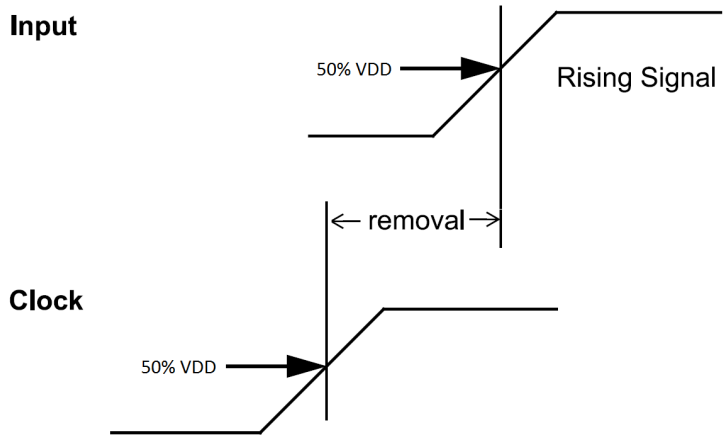


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

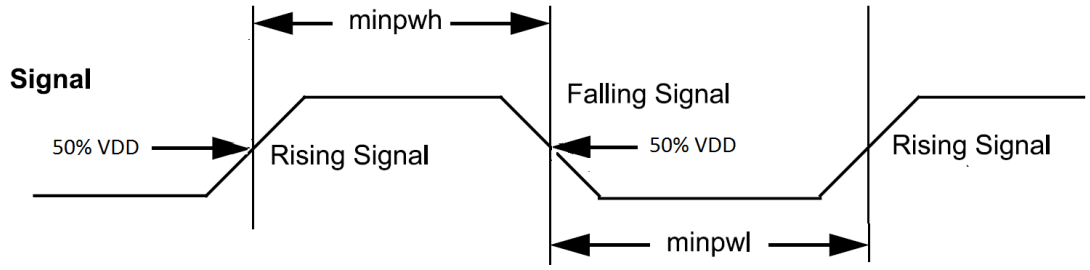


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

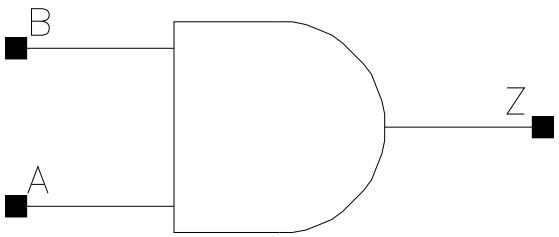
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X25_P0	1.200	1.088	1.3056
X33_P0	1.200	1.360	1.6320
X42_P0	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0007	0.0010	0.0015	0.0019
B	0.0006	0.0010	0.0015	0.0019
	X42_P0			
A	0.0018			
B	0.0019			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0314	0.0265	1.7150	0.8702
A to Z ↑	0.0243	0.0227	3.0989	1.4967
B to Z ↓	0.0300	0.0253	1.7164	0.8694
B to Z ↑	0.0251	0.0233	3.1007	1.4970
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0272	0.0265	0.5784	0.4309

A to Z ↑	0.0225	0.0230	0.9899	0.7485
B to Z ↓	0.0260	0.0245	0.5790	0.4298
B to Z ↑	0.0231	0.0230	0.9909	0.7487
	X42_P0		**X42_P0**	
A to Z ↓	0.0284		0.3502	
A to Z ↑	0.0248		0.5996	
B to Z ↓	0.0265		0.3501	
B to Z ↑	0.0250		0.5984	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	4.452e-07	1.771e-12
X16_P0	8.946e-07	2.024e-12
X25_P0	1.267e-06	2.779e-12
X33_P0	1.708e-06	3.273e-12
X42_P0	1.953e-06	3.536e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	1.806e-05	3.257e-05	5.014e-05	9.802e-05
B (output stable)	4.303e-05	8.083e-05	1.268e-04	3.993e-04
A to Z	2.254e-03	3.680e-03	5.695e-03	7.412e-03
B to Z	2.136e-03	3.468e-03	5.362e-03	6.716e-03
	X42_P0			
A (output stable)	9.815e-05			
B (output stable)	4.021e-04			
A to Z	8.910e-03			
B to Z	8.189e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

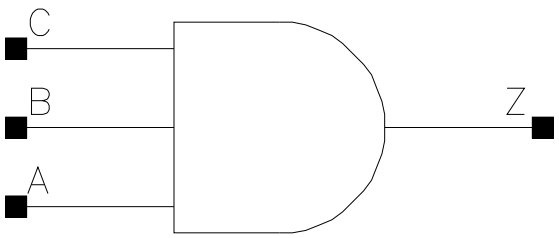
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	9.968e-08	6.033e-08	4.750e-08	3.062e-08
B (output stable)	6.780e-08	5.354e-08	3.200e-08	2.210e-08
A to Z	-5.840e-08	1.352e-07	-4.370e-07	-2.744e-07
B to Z	-4.600e-09	1.511e-07	-5.020e-08	-1.217e-07
	X42_P0			
A (output stable)	3.349e-08			
B (output stable)	3.500e-08			
A to Z	-1.773e-07			
B to Z	2.143e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X25_P0	1.200	1.360	1.6320
X33_P0	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0007	0.0010	0.0016	0.0020
B	0.0006	0.0010	0.0015	0.0018
C	0.0006	0.0010	0.0014	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0339	0.0291	1.7381	0.8498
A to Z ↑	0.0308	0.0286	3.1184	1.4836
B to Z ↓	0.0329	0.0280	1.7376	0.8486
B to Z ↑	0.0316	0.0295	3.1201	1.4836
C to Z ↓	0.0317	0.0267	1.7337	0.8491
C to Z ↑	0.0320	0.0293	3.1223	1.4844
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0291	0.0278	0.5864	0.4374

A to Z ↑	0.0282	0.0271	1.0150	0.7597
B to Z ↓	0.0281	0.0266	0.5862	0.4371
B to Z ↑	0.0291	0.0279	1.0167	0.7611
C to Z ↓	0.0267	0.0255	0.5859	0.4368
C to Z ↑	0.0291	0.0280	1.0167	0.7608

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	3.918e-07	2.024e-12
X17_P0	8.030e-07	2.276e-12
X25_P0	1.151e-06	3.284e-12
X33_P0	1.530e-06	3.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	1.202e-05	2.277e-05	3.033e-05	4.072e-05
B (output stable)	3.950e-05	7.659e-05	1.119e-04	1.504e-04
C (output stable)	5.484e-05	9.482e-05	1.466e-04	1.922e-04
A to Z	2.489e-03	4.283e-03	6.266e-03	7.943e-03
B to Z	2.367e-03	4.069e-03	5.935e-03	7.499e-03
C to Z	2.266e-03	3.853e-03	5.602e-03	7.060e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

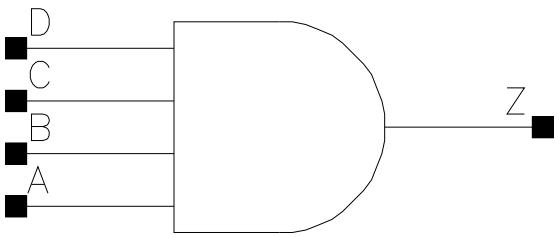
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	7.508e-08	6.352e-08	4.553e-08	3.400e-08
B (output stable)	8.539e-08	5.929e-08	2.677e-08	2.387e-08
C (output stable)	7.353e-08	4.127e-08	1.463e-08	-1.681e-08
A to Z	-1.270e-07	-5.030e-08	-6.094e-08	-5.773e-07
B to Z	-1.916e-07	-1.994e-07	-5.529e-07	-5.846e-07
C to Z	-1.904e-07	-1.871e-07	-1.162e-07	-7.510e-08

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X6_P0	1.200	1.088	1.3056
X20_P0	1.200	2.312	2.7744
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P0	X6_P0	X20_P0	X27_P0
A	0.0005	0.0007	0.0016	0.0018
B	0.0005	0.0007	0.0016	0.0018
C	0.0005	0.0007	0.0016	0.0018
D	0.0005	0.0007	0.0016	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X6_P0	X4_P0	X6_P0
A to Z ↓	0.0355	0.0305	3.1979	2.0862
A to Z ↑	0.0342	0.0268	11.5140	6.2766
B to Z ↓	0.0345	0.0288	3.2004	2.0855
B to Z ↑	0.0352	0.0271	11.5234	6.2745
C to Z ↓	0.0367	0.0327	3.1631	2.0993
C to Z ↑	0.0333	0.0259	11.5250	6.2902

D to Z ↓	0.0357	0.0307	3.1640	2.0983
D to Z ↑	0.0349	0.0264	11.5481	6.2920
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0296	0.0281	0.6146	0.4354
A to Z ↑	0.0273	0.0304	2.0956	1.5934
B to Z ↓	0.0274	0.0262	0.6136	0.4351
B to Z ↑	0.0271	0.0305	2.0972	1.5950
C to Z ↓	0.0290	0.0273	0.6195	0.4379
C to Z ↑	0.0240	0.0259	2.0964	1.5953
D to Z ↓	0.0265	0.0254	0.6189	0.4370
D to Z ↑	0.0236	0.0260	2.0973	1.5945

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	2.983e-07	2.780e-12
X6_P0	5.978e-07	2.781e-12
X20_P0	1.658e-06	5.050e-12
X27_P0	1.976e-06	5.554e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	4.145e-04	6.308e-04	1.848e-03	2.287e-03
B (output stable)	3.906e-04	5.827e-04	1.686e-03	2.118e-03
C (output stable)	4.053e-04	6.547e-04	1.631e-03	2.024e-03
D (output stable)	3.814e-04	5.983e-04	1.452e-03	1.801e-03
A to Z	1.693e-03	2.584e-03	7.688e-03	1.002e-02
B to Z	1.617e-03	2.431e-03	7.031e-03	9.352e-03
C to Z	1.659e-03	2.607e-03	6.473e-03	8.113e-03
D to Z	1.582e-03	2.443e-03	5.793e-03	7.427e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

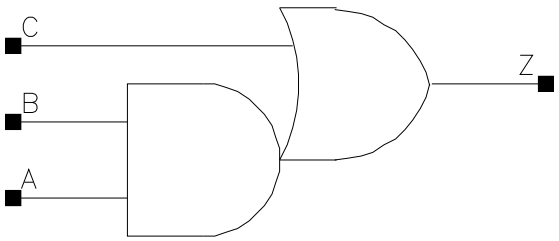
Pin Cycle (vdds)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	-1.039e-06	-1.428e-06	-6.194e-06	-1.381e-05
B (output stable)	-9.848e-07	-1.310e-06	-6.234e-06	-1.501e-05
C (output stable)	6.679e-06	1.207e-05	4.075e-05	7.148e-05
D (output stable)	4.380e-06	9.191e-06	2.392e-05	3.835e-05
A to Z	-2.699e-07	4.690e-08	-1.154e-06	-2.949e-06
B to Z	-1.287e-07	2.492e-07	-7.070e-07	-3.514e-06
C to Z	-2.616e-07	-4.824e-07	-8.262e-07	-5.151e-07
D to Z	-1.368e-07	-3.348e-07	-1.061e-06	-1.003e-06

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0019
B	0.0006	0.0010	0.0018
C	0.0007	0.0010	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0403	0.0363	1.7683	0.8667
A to Z ↑	0.0251	0.0226	3.0040	1.4744
B to Z ↓	0.0376	0.0339	1.7636	0.8634
B to Z ↑	0.0262	0.0237	2.9980	1.4737
C to Z ↓	0.0403	0.0366	1.7575	0.8620
C to Z ↑	0.0227	0.0214	2.9852	1.4672
	X33_P0		**X33_P0**	
A to Z ↓	0.0364		0.4412	
A to Z ↑	0.0230		0.7438	

B to Z ↓	0.0340		0.4409	
B to Z ↑	0.0237		0.7435	
C to Z ↓	0.0368		0.4393	
C to Z ↑	0.0211		0.7399	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	5.391e-07	2.024e-12
X17_P0	1.021e-06	2.276e-12
X33_P0	2.005e-06	3.790e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	1.015e-05	1.947e-05	4.712e-05
B (output stable)	2.782e-05	4.415e-05	1.429e-04
C (output stable)	7.265e-05	1.262e-04	2.820e-04
A to Z	2.297e-03	3.890e-03	7.675e-03
B to Z	2.178e-03	3.665e-03	7.134e-03
C to Z	2.555e-03	4.341e-03	8.576e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

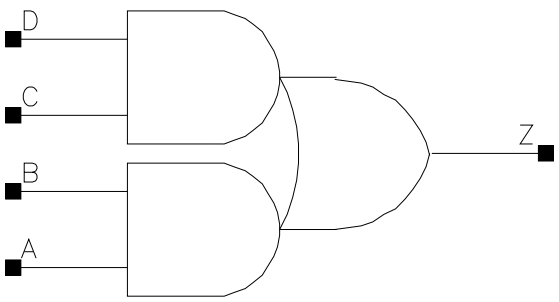
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	5.239e-06	1.344e-05	2.116e-05
B (output stable)	1.867e-05	3.141e-05	5.904e-05
C (output stable)	-7.687e-06	-1.072e-05	-2.118e-05
A to Z	-1.757e-07	-9.299e-08	-1.010e-06
B to Z	-1.423e-07	-1.982e-07	-8.037e-07
C to Z	-2.324e-06	-2.523e-06	-5.640e-06

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0018
B	0.0007	0.0010	0.0017
C	0.0006	0.0009	0.0018
D	0.0007	0.0010	0.0017

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0467	0.0418	1.7061	0.8618
A to Z ↑	0.0311	0.0286	2.9588	1.4731
B to Z ↓	0.0438	0.0393	1.7002	0.8602
B to Z ↑	0.0319	0.0299	2.9611	1.4735

C to Z ↓	0.0415	0.0377	1.7019	0.8602
C to Z ↑	0.0272	0.0252	2.9546	1.4689
D to Z ↓	0.0398	0.0360	1.6990	0.8590
D to Z ↑	0.0286	0.0263	2.9544	1.4692
	X33_P0		**X33_P0**	
A to Z ↓	0.0392		0.4408	
A to Z ↑	0.0260		0.7461	
B to Z ↓	0.0374		0.4404	
B to Z ↑	0.0271		0.7460	
C to Z ↓	0.0350		0.4402	
C to Z ↑	0.0230		0.7435	
D to Z ↓	0.0332		0.4397	
D to Z ↑	0.0238		0.7437	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	5.992e-07	2.528e-12
X17_P0	1.130e-06	2.779e-12
X33_P0	2.112e-06	4.294e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	4.109e-05	6.314e-05	9.599e-05
B (output stable)	9.069e-05	1.267e-04	1.433e-04
C (output stable)	1.683e-05	3.205e-05	6.322e-05
D (output stable)	3.177e-05	6.152e-05	1.257e-04
A to Z	3.074e-03	5.144e-03	9.309e-03
B to Z	2.843e-03	4.828e-03	8.824e-03
C to Z	2.573e-03	4.361e-03	7.708e-03
D to Z	2.469e-03	4.150e-03	7.268e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

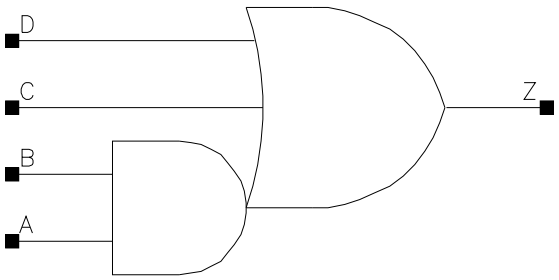
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	-4.432e-07	-1.518e-06	-3.769e-06
B (output stable)	-1.643e-06	-1.539e-06	-3.810e-06
C (output stable)	3.426e-06	9.549e-06	2.000e-05
D (output stable)	3.687e-06	9.678e-06	1.972e-05
A to Z	-1.063e-06	-1.286e-06	-2.576e-06
B to Z	-1.077e-06	-9.353e-07	-2.744e-06
C to Z	-1.495e-07	-1.430e-07	-4.209e-07
D to Z	-1.450e-08	-1.023e-07	-3.859e-07

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	0.952	1.1424
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0017
B	0.0006	0.0009	0.0017
C	0.0006	0.0009	0.0017
D	0.0006	0.0009	0.0017

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0527	0.0464	1.8596	0.9198
A to Z ↑	0.0270	0.0246	2.9856	1.5313
B to Z ↓	0.0507	0.0436	1.8547	0.9180
B to Z ↑	0.0282	0.0252	2.9869	1.5315
C to Z ↓	0.0568	0.0503	1.8506	0.9158
C to Z ↑	0.0245	0.0228	2.9705	1.5252

D to Z ↓	0.0560	0.0500	1.8507	0.9161
D to Z ↑	0.0242	0.0227	2.9704	1.5249
	X33_P0		**X33_P0**	
A to Z ↓	0.0473		0.4604	
A to Z ↑	0.0245		0.7439	
B to Z ↓	0.0428		0.4586	
B to Z ↑	0.0248		0.7437	
C to Z ↓	0.0516		0.4579	
C to Z ↑	0.0224		0.7413	
D to Z ↓	0.0502		0.4582	
D to Z ↑	0.0217		0.7396	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	5.232e-07	2.276e-12
X17_P0	1.000e-06	2.527e-12
X33_P0	2.001e-06	4.547e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	5.104e-06	1.046e-05	3.294e-05
B (output stable)	1.065e-05	2.031e-05	8.616e-05
C (output stable)	1.134e-04	1.934e-04	5.379e-04
D (output stable)	1.626e-05	2.860e-05	6.923e-05
A to Z	2.534e-03	4.183e-03	8.409e-03
B to Z	2.433e-03	3.956e-03	7.694e-03
C to Z	2.951e-03	4.929e-03	1.001e-02
D to Z	2.774e-03	4.632e-03	9.189e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

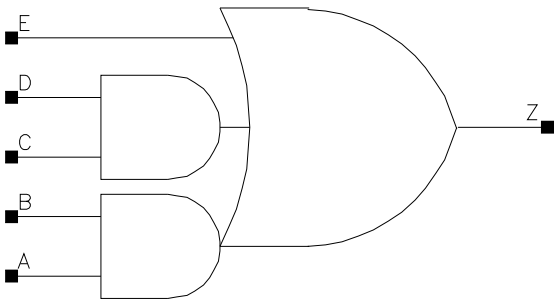
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	5.005e-06	1.190e-05	1.923e-05
B (output stable)	1.118e-05	2.313e-05	3.991e-05
C (output stable)	-2.060e-05	-3.284e-05	-9.022e-05
D (output stable)	7.763e-06	1.653e-05	4.492e-05
A to Z	-1.606e-07	-2.310e-07	-8.329e-07
B to Z	-1.139e-07	-3.238e-07	-6.031e-07
C to Z	-3.210e-06	-4.091e-06	-1.110e-05
D to Z	-2.175e-06	-2.156e-06	-5.534e-06

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.088	1.3056
X17_P0	1.200	1.224	1.4688
X33_P0	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0018
B	0.0006	0.0009	0.0017
C	0.0007	0.0011	0.0018
D	0.0006	0.0009	0.0018
E	0.0006	0.0009	0.0017

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0658	0.0571	1.7708	0.8891
A to Z ↑	0.0324	0.0284	2.9300	1.4795

B to Z ↓	0.0638	0.0547	1.7666	0.8876
B to Z ↑	0.0342	0.0298	2.9316	1.4796
C to Z ↓	0.0546	0.0483	1.7643	0.8874
C to Z ↑	0.0284	0.0247	2.9086	1.4721
D to Z ↓	0.0510	0.0443	1.7568	0.8831
D to Z ↑	0.0296	0.0256	2.9090	1.4722
E to Z ↓	0.0579	0.0503	1.7532	0.8829
E to Z ↑	0.0255	0.0226	2.8895	1.4639
	X33_P0		**X33_P0**	
A to Z ↓	0.0561		0.4596	
A to Z ↑	0.0289		0.7483	
B to Z ↓	0.0530		0.4588	
B to Z ↑	0.0302		0.7482	
C to Z ↓	0.0467		0.4582	
C to Z ↑	0.0246		0.7432	
D to Z ↓	0.0432		0.4566	
D to Z ↑	0.0255		0.7436	
E to Z ↓	0.0492		0.4561	
E to Z ↑	0.0225		0.7390	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	6.355e-07	2.780e-12
X17_P0	1.189e-06	3.032e-12
X33_P0	2.169e-06	5.035e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	2.762e-05	4.983e-05	1.089e-04
B (output stable)	5.694e-05	7.074e-05	1.680e-04
C (output stable)	1.670e-05	2.417e-05	6.065e-05
D (output stable)	1.989e-05	3.685e-05	9.379e-05
E (output stable)	9.432e-05	1.096e-04	2.737e-04
A to Z	3.520e-03	5.603e-03	1.099e-02
B to Z	3.424e-03	5.373e-03	1.038e-02
C to Z	2.729e-03	4.398e-03	8.510e-03
D to Z	2.606e-03	4.147e-03	7.946e-03
E to Z	3.034e-03	4.837e-03	9.362e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	-3.525e-06	-5.733e-06	-1.256e-05
B (output stable)	-8.149e-06	-8.610e-06	-1.927e-05
C (output stable)	9.208e-06	1.840e-05	3.962e-05
D (output stable)	8.960e-06	2.297e-05	4.438e-05
E (output stable)	3.292e-06	1.243e-05	1.694e-05
A to Z	-4.329e-06	-3.276e-06	-7.413e-06
B to Z	-4.245e-06	-2.759e-06	-7.650e-06
C to Z	-2.366e-07	-2.479e-07	-7.774e-07
D to Z	-7.957e-08	-1.752e-07	-1.064e-07

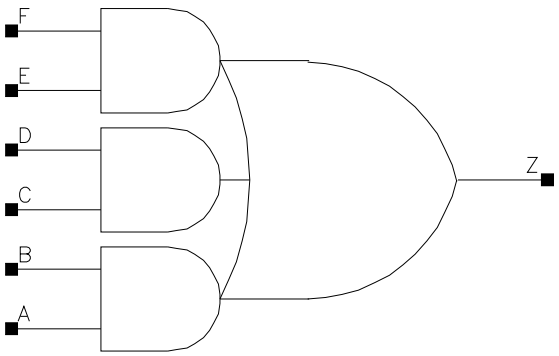
E to Z	-2.306e-06	-2.016e-06	-5.059e-06

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.360	1.6320
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
A	0.0006	0.0007	0.0009	0.0018

B	0.0006	0.0007	0.0012	0.0017
C	0.0006	0.0007	0.0008	0.0017
D	0.0006	0.0007	0.0009	0.0017
E	0.0006	0.0007	0.0009	0.0018
F	0.0006	0.0007	0.0009	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0663	0.0629	3.3255	1.7701
A to Z ↑	0.0341	0.0330	5.7600	2.9976
B to Z ↓	0.0617	0.0589	3.3102	1.7628
B to Z ↑	0.0348	0.0340	5.7558	2.9970
C to Z ↓	0.0604	0.0577	3.3177	1.7664
C to Z ↑	0.0315	0.0304	5.7285	2.9814
D to Z ↓	0.0580	0.0554	3.3076	1.7609
D to Z ↑	0.0331	0.0321	5.7250	2.9798
E to Z ↓	0.0491	0.0481	3.3019	1.7592
E to Z ↑	0.0273	0.0265	5.7006	2.9676
F to Z ↓	0.0461	0.0452	3.2916	1.7538
F to Z ↑	0.0284	0.0277	5.6995	2.9675
	X17_P0	X33_P0	X17_P0	X33_P0
A to Z ↓	0.0607	0.0579	0.8927	0.4577
A to Z ↑	0.0307	0.0305	1.4846	0.7505
B to Z ↓	0.0575	0.0551	0.8883	0.4569
B to Z ↑	0.0322	0.0319	1.4845	0.7505
C to Z ↓	0.0562	0.0538	0.8909	0.4574
C to Z ↑	0.0283	0.0288	1.4775	0.7466
D to Z ↓	0.0535	0.0513	0.8878	0.4566
D to Z ↑	0.0298	0.0301	1.4778	0.7468
E to Z ↓	0.0466	0.0470	0.8868	0.4561
E to Z ↑	0.0246	0.0255	1.4725	0.7449
F to Z ↓	0.0438	0.0438	0.8841	0.4548
F to Z ↑	0.0257	0.0267	1.4726	0.7450

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	5.288e-07	3.284e-12
X8_P0	7.787e-07	3.284e-12
X17_P0	1.293e-06	3.536e-12
X33_P0	2.325e-06	5.552e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	6.708e-05	8.073e-05	1.032e-04	2.056e-04
B (output stable)	1.893e-04	2.144e-04	2.475e-04	4.258e-04
C (output stable)	3.656e-05	4.459e-05	5.800e-05	9.810e-05
D (output stable)	5.176e-05	6.396e-05	8.070e-05	1.677e-04
E (output stable)	3.654e-05	4.173e-05	5.200e-05	7.723e-05
F (output stable)	4.042e-05	4.870e-05	6.750e-05	1.338e-04

A to Z	3.282e-03	4.247e-03	6.296e-03	1.182e-02
B to Z	3.041e-03	3.967e-03	5.916e-03	1.121e-02
C to Z	2.777e-03	3.648e-03	5.484e-03	1.033e-02
D to Z	2.670e-03	3.511e-03	5.259e-03	9.799e-03
E to Z	2.205e-03	3.014e-03	4.547e-03	8.887e-03
F to Z	2.090e-03	2.865e-03	4.323e-03	8.362e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

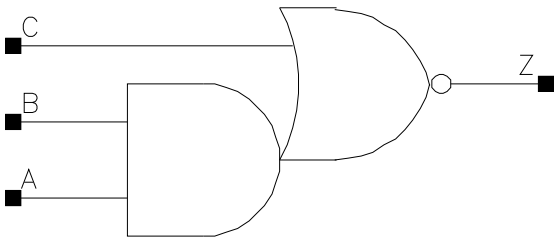
Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	-7.833e-06	-9.739e-06	-1.288e-05	-2.549e-05
B (output stable)	-2.114e-05	-2.295e-05	-2.576e-05	-5.598e-05
C (output stable)	-1.574e-06	-1.114e-06	1.129e-06	7.457e-06
D (output stable)	1.755e-06	3.159e-06	5.575e-06	2.289e-05
E (output stable)	2.092e-05	2.696e-05	4.027e-05	7.165e-05
F (output stable)	1.699e-05	2.247e-05	3.386e-05	6.317e-05
A to Z	-5.758e-06	-5.850e-06	-6.323e-06	-1.043e-05
B to Z	-6.012e-06	-5.806e-06	-5.825e-06	-1.046e-05
C to Z	-2.863e-06	-2.650e-06	-2.294e-06	-2.321e-06
D to Z	-2.637e-06	-2.456e-06	-1.926e-06	-1.788e-06
E to Z	-4.707e-07	-4.646e-07	-6.107e-07	-1.358e-06
F to Z	-2.805e-07	-3.410e-07	-4.309e-07	-5.547e-07

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008
X44_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X33_P0	X44_P0
A	0.0007	0.0022	0.0044	0.0059
B	0.0007	0.0020	0.0041	0.0056
C	0.0008	0.0023	0.0046	0.0061

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0106	0.0110	3.1409	1.0725
A to Z ↑	0.0195	0.0197	6.4315	2.1539
B to Z ↓	0.0100	0.0101	3.1791	1.0903
B to Z ↑	0.0164	0.0160	6.3319	2.1527
C to Z ↓	0.0100	0.0101	1.7768	0.6153
C to Z ↑	0.0211	0.0209	5.8701	1.9830
	X33_P0	**X44_P0**	**X33_P0**	**X44_P0**
A to Z ↓	0.0113	0.0113	0.5468	0.4152

A to Z ↑	0.0199	0.0199	1.0790	0.8191
B to Z ↓	0.0102	0.0102	0.5562	0.4223
B to Z ↑	0.0162	0.0161	1.0761	0.8143
C to Z ↓	0.0115	0.0116	0.3656	0.2844
C to Z ↑	0.0216	0.0213	0.9914	0.7518

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P0	4.194e-07	1.772e-12
X17_P0	1.119e-06	3.285e-12
X33_P0	2.091e-06	5.556e-12
X44_P0	2.809e-06	7.070e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	2.005e-05	6.744e-05	1.442e-04	1.935e-04
B (output stable)	4.655e-05	1.955e-04	4.293e-04	5.540e-04
C (output stable)	1.232e-04	3.771e-04	8.356e-04	1.075e-03
A to Z	1.090e-03	3.416e-03	6.997e-03	9.245e-03
B to Z	8.823e-04	2.523e-03	5.160e-03	6.806e-03
C to Z	1.551e-03	4.555e-03	9.487e-03	1.234e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

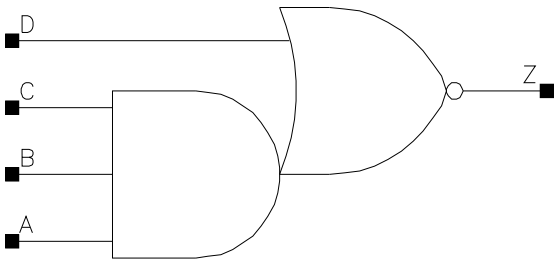
Pin Cycle (vdds)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	1.149e-05	2.964e-05	5.674e-05	7.192e-05
B (output stable)	2.893e-05	7.090e-05	1.548e-04	1.836e-04
C (output stable)	-9.945e-06	-2.431e-05	-5.578e-05	-6.527e-05
A to Z	-3.740e-08	-5.310e-07	-2.150e-07	-1.970e-07
B to Z	-1.310e-07	-3.130e-07	-7.940e-07	-1.090e-06
C to Z	-2.010e-06	-4.749e-06	-1.382e-05	-1.628e-05

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X29_P0	1.200	3.536	4.2432
X38_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X29_P0	X38_P0
A	0.0008	0.0045	0.0058
B	0.0007	0.0043	0.0056
C	0.0007	0.0041	0.0054
D	0.0008	0.0046	0.0058

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X29_P0	X5_P0	X29_P0
A to Z ↓	0.0149	0.0160	4.5281	0.7899
A to Z ↑	0.0245	0.0246	6.4266	1.0665
B to Z ↓	0.0153	0.0157	4.5444	0.7950
B to Z ↑	0.0222	0.0220	6.4273	1.0755
C to Z ↓	0.0143	0.0142	4.5737	0.8013
C to Z ↑	0.0194	0.0187	6.3394	1.0819
D to Z ↓	0.0119	0.0135	1.8192	0.3680

D to Z ↑	0.0240	0.0245	5.4841	0.9213
	X38_P0		**X38_P0**	
A to Z ↓	0.0156		0.6140	
A to Z ↑	0.0238		0.8042	
B to Z ↓	0.0153		0.6183	
B to Z ↑	0.0212		0.8124	
C to Z ↓	0.0137		0.6231	
C to Z ↑	0.0179		0.8220	
D to Z ↓	0.0141		0.3072	
D to Z ↑	0.0239		0.6960	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P0	4.279e-07	2.024e-12
X29_P0	2.124e-06	7.324e-12
X38_P0	2.713e-06	9.328e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P0	X29_P0	X38_P0
A (output stable)	1.711e-05	1.395e-04	1.718e-04
B (output stable)	3.414e-05	2.620e-04	3.336e-04
C (output stable)	6.482e-05	5.903e-04	7.660e-04
D (output stable)	4.564e-04	3.559e-03	4.705e-03
A to Z	1.635e-03	1.031e-02	1.286e-02
B to Z	1.419e-03	8.499e-03	1.060e-02
C to Z	1.204e-03	6.654e-03	8.127e-03
D to Z	2.033e-03	1.240e-02	1.581e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

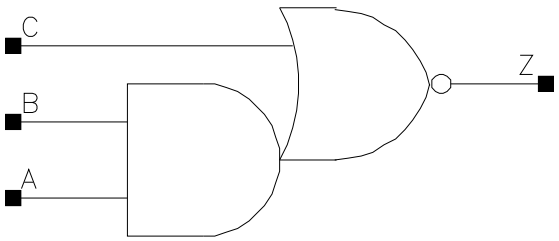
Pin Cycle (vdds)	X5_P0	X29_P0	X38_P0
A (output stable)	1.582e-05	1.069e-04	1.379e-04
B (output stable)	6.418e-06	3.918e-05	5.163e-05
C (output stable)	7.188e-06	3.821e-05	4.935e-05
D (output stable)	-6.108e-05	-5.209e-04	-6.677e-04
A to Z	-1.920e-07	-9.940e-07	-6.470e-07
B to Z	-1.820e-07	-2.556e-06	-3.506e-06
C to Z	-1.330e-07	-1.610e-06	4.950e-07
D to Z	-2.590e-06	-2.507e-05	-3.179e-05

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X11_P0	1.200	1.088	1.3056
X16_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X11_P0	X16_P0	X23_P0
A	0.0008	0.0016	0.0024	0.0032
B	0.0008	0.0015	0.0022	0.0030
C	0.0008	0.0014	0.0021	0.0030
	X46_P0			
A	0.0061			
B	0.0058			
C	0.0059			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X11_P0	X6_P0	X11_P0
A to Z ↓	0.0121	0.0130	3.0190	1.5455
A to Z ↑	0.0226	0.0237	6.4100	3.1368
B to Z ↓	0.0120	0.0123	3.0547	1.5662

B to Z ↑	0.0203	0.0208	6.3284	3.1427
C to Z ↓	0.0072	0.0075	1.8351	1.0787
C to Z ↑	0.0160	0.0156	5.8561	2.8876
	X16_P0	**X23_P0**	**X16_P0**	**X23_P0**
A to Z ↓	0.0124	0.0128	1.0711	0.8065
A to Z ↑	0.0224	0.0229	2.1114	1.5982
B to Z ↓	0.0122	0.0122	1.0865	0.8173
B to Z ↑	0.0194	0.0199	2.1080	1.6022
C to Z ↓	0.0076	0.0068	0.7519	0.4758
C to Z ↑	0.0150	0.0154	1.9419	1.4719
	X46_P0		**X46_P0**	
A to Z ↓	0.0124		0.4154	
A to Z ↑	0.0221		0.8296	
B to Z ↓	0.0119		0.4213	
B to Z ↑	0.0190		0.8266	
C to Z ↓	0.0070		0.2445	
C to Z ↑	0.0152		0.7619	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P0	4.180e-07	1.772e-12
X11_P0	8.345e-07	2.781e-12
X16_P0	1.116e-06	3.286e-12
X23_P0	1.566e-06	4.293e-12
X46_P0	2.969e-06	7.319e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	4.189e-05	1.055e-04	1.428e-04	2.008e-04
B (output stable)	1.175e-04	3.563e-04	3.969e-04	5.874e-04
C (output stable)	6.906e-05	1.704e-04	2.204e-04	3.436e-04
A to Z	1.590e-03	3.523e-03	4.759e-03	6.583e-03
B to Z	1.372e-03	2.876e-03	3.847e-03	5.274e-03
C to Z	8.349e-04	1.691e-03	2.337e-03	3.224e-03
	X46_P0			
A (output stable)	3.651e-04			
B (output stable)	9.884e-04			
C (output stable)	5.372e-04			
A to Z	1.206e-02			
B to Z	9.618e-03			
C to Z	6.005e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	-2.551e-06	-6.865e-06	-6.277e-06	-9.369e-06
B (output stable)	-1.539e-05	-4.483e-05	-3.704e-05	-5.924e-05
C (output stable)	7.747e-05	1.987e-04	1.817e-04	2.759e-04
A to Z	-7.560e-07	-1.602e-06	-9.550e-07	-2.550e-06
B to Z	-7.770e-07	-2.636e-06	-1.869e-06	-3.486e-06
C to Z	5.546e-07	1.571e-07	1.001e-06	1.543e-06

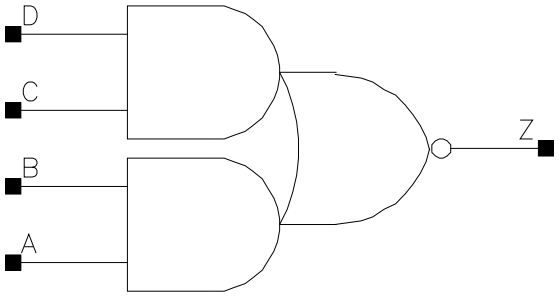
	X46_P0			
A (output stable)	-1.576e-05			
B (output stable)	-9.168e-05			
C (output stable)	4.647e-04			
A to Z	-1.813e-06			
B to Z	-2.660e-06			
C to Z	2.307e-06			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P0	X10_P0	X16_P0	X21_P0
A	0.0007	0.0016	0.0024	0.0031
B	0.0007	0.0015	0.0022	0.0030
C	0.0006	0.0016	0.0022	0.0030
D	0.0007	0.0014	0.0021	0.0028
	X42_P0			
A	0.0062			
B	0.0059			
C	0.0059			
D	0.0056			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X10_P0**	**X4_P0**	**X10_P0**
A to Z ↓	0.0135	0.0133	3.7420	1.4806
A to Z ↑	0.0283	0.0246	8.7101	2.8992
B to Z ↓	0.0138	0.0137	3.7866	1.5004
B to Z ↑	0.0258	0.0229	8.6784	2.9645
C to Z ↓	0.0108	0.0103	3.8393	1.4901
C to Z ↑	0.0220	0.0193	8.6315	2.8889
D to Z ↓	0.0104	0.0100	3.8957	1.5134
D to Z ↑	0.0192	0.0169	8.5979	2.9287
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0144	0.0143	1.0768	0.8105
A to Z ↑	0.0256	0.0254	1.9547	1.5101
B to Z ↓	0.0145	0.0140	1.0903	0.8210
B to Z ↑	0.0229	0.0226	1.9524	1.5106
C to Z ↓	0.0110	0.0113	1.0755	0.8109
C to Z ↑	0.0199	0.0204	1.9382	1.4952
D to Z ↓	0.0103	0.0101	1.0941	0.8248
D to Z ↑	0.0167	0.0169	1.9388	1.4965
	X42_P0		**X42_P0**	
A to Z ↓	0.0150		0.4231	
A to Z ↑	0.0258		0.7587	
B to Z ↓	0.0145		0.4284	
B to Z ↑	0.0227		0.7550	
C to Z ↓	0.0117		0.4173	
C to Z ↑	0.0205		0.7530	
D to Z ↓	0.0106		0.4246	
D to Z ↑	0.0170		0.7505	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	3.660e-07	2.024e-12
X10_P0	9.877e-07	3.284e-12
X16_P0	1.328e-06	4.031e-12
X21_P0	1.792e-06	5.306e-12
X42_P0	3.451e-06	9.334e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	3.854e-05	9.249e-05	1.695e-04	2.261e-04
B (output stable)	5.848e-05	1.463e-04	2.895e-04	3.936e-04
C (output stable)	2.165e-05	5.907e-05	1.147e-04	1.708e-04
D (output stable)	4.424e-05	1.193e-04	3.014e-04	4.396e-04
A to Z	1.641e-03	3.982e-03	6.294e-03	8.105e-03
B to Z	1.444e-03	3.517e-03	5.334e-03	6.813e-03
C to Z	9.655e-04	2.382e-03	3.734e-03	5.071e-03
D to Z	7.982e-04	1.962e-03	2.831e-03	3.792e-03
	X42_P0			
A (output stable)	4.360e-04			
B (output stable)	7.281e-04			
C (output stable)	3.079e-04			
D (output stable)	8.111e-04			

A to Z	1.601e-02			
B to Z	1.349e-02			
C to Z	9.861e-03			
D to Z	7.466e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

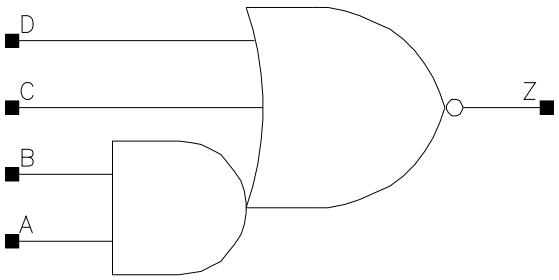
Pin Cycle (vdds)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	-2.091e-06	-4.297e-06	-6.388e-06	-7.224e-06
B (output stable)	-2.068e-06	-4.299e-06	-6.431e-06	-8.757e-06
C (output stable)	6.601e-06	2.096e-05	2.772e-05	3.910e-05
D (output stable)	6.321e-06	2.057e-05	2.743e-05	3.572e-05
A to Z	-2.542e-06	-3.002e-06	-4.101e-06	-4.166e-06
B to Z	-2.147e-06	-3.060e-06	-4.418e-06	-5.407e-06
C to Z	-1.514e-07	-7.050e-07	-4.653e-07	-5.180e-07
D to Z	-1.649e-07	-1.193e-07	-2.290e-07	3.297e-07
	X42_P0			
A (output stable)	-1.374e-05			
B (output stable)	-1.680e-05			
C (output stable)	7.241e-05			
D (output stable)	6.793e-05			
A to Z	-1.209e-05			
B to Z	-1.168e-05			
C to Z	-6.577e-07			
D to Z	-8.083e-07			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X35_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P0	X35_P0
A	0.0007	0.0058
B	0.0008	0.0054
C	0.0008	0.0055
D	0.0008	0.0053

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X35_P0	X5_P0	X35_P0
A to Z ↓	0.0121	0.0126	3.1742	0.4722
A to Z ↑	0.0255	0.0242	9.7508	1.2471
B to Z ↓	0.0119	0.0119	3.2179	0.4802
B to Z ↑	0.0219	0.0199	9.6839	1.2456
C to Z ↓	0.0120	0.0153	1.9020	0.3658
C to Z ↑	0.0305	0.0300	9.2058	1.1792
D to Z ↓	0.0116	0.0142	1.9200	0.3653

D to Z ↑	0.0296	0.0282	9.2214	1.1819

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P0	3.503e-07	2.023e-12
X35_P0	2.181e-06	9.331e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P0	X35_P0
A (output stable)	1.028e-05	1.109e-04
B (output stable)	2.064e-05	2.337e-04
C (output stable)	1.868e-04	1.916e-03
D (output stable)	2.713e-05	2.603e-04
A to Z	1.323e-03	9.669e-03
B to Z	1.112e-03	7.489e-03
C to Z	2.097e-03	1.626e-02
D to Z	1.782e-03	1.299e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

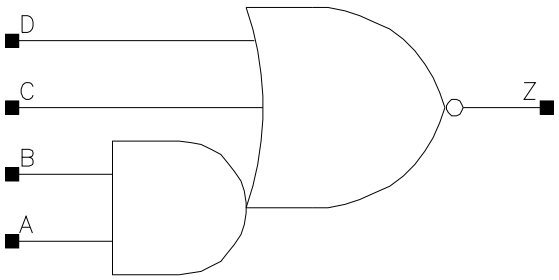
Pin Cycle (vdds)	X5_P0	X35_P0
A (output stable)	1.162e-05	7.538e-05
B (output stable)	2.169e-05	1.313e-04
C (output stable)	-3.191e-05	-2.569e-04
D (output stable)	1.560e-05	1.237e-04
A to Z	-3.650e-07	-2.062e-06
B to Z	-1.846e-07	-3.492e-06
C to Z	-3.793e-06	-3.217e-05
D to Z	-2.430e-06	-1.551e-05

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X17_P0	1.200	2.448	2.9376
X34_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P0	X17_P0	X34_P0
A	0.0008	0.0031	0.0062
B	0.0008	0.0030	0.0059
C	0.0007	0.0027	0.0053
D	0.0007	0.0025	0.0049

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X17_P0	X4_P0	X17_P0
A to Z ↓	0.0138	0.0148	3.4268	0.9127
A to Z ↑	0.0301	0.0316	9.7881	2.4162
B to Z ↓	0.0144	0.0147	3.4685	0.9229
B to Z ↑	0.0273	0.0278	9.6862	2.4174
C to Z ↓	0.0125	0.0123	3.0230	0.7346
C to Z ↑	0.0228	0.0241	9.1956	2.2810

D to Z ↓	0.0107	0.0096	3.0774	0.7388
D to Z ↑	0.0198	0.0182	9.2325	2.2912
	X34_P0		**X34_P0**	
A to Z ↓	0.0147		0.4693	
A to Z ↑	0.0312		1.2313	
B to Z ↓	0.0148		0.4748	
B to Z ↑	0.0274		1.2247	
C to Z ↓	0.0125		0.3896	
C to Z ↑	0.0234		1.1594	
D to Z ↓	0.0098		0.3932	
D to Z ↑	0.0178		1.1648	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	3.155e-07	2.025e-12
X17_P0	1.206e-06	5.303e-12
X34_P0	2.286e-06	9.305e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X17_P0	X34_P0
A (output stable)	4.405e-05	2.018e-04	4.038e-04
B (output stable)	6.117e-05	3.318e-04	6.352e-04
C (output stable)	6.267e-05	4.717e-04	8.829e-04
D (output stable)	1.880e-05	1.737e-04	3.161e-04
A to Z	1.976e-03	8.569e-03	1.655e-02
B to Z	1.772e-03	7.321e-03	1.419e-02
C to Z	1.216e-03	5.268e-03	1.000e-02
D to Z	8.823e-04	3.293e-03	6.253e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

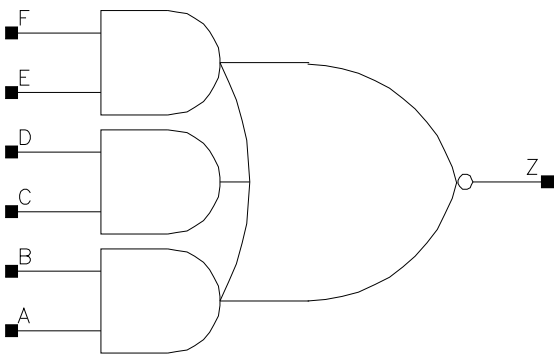
Pin Cycle (vdds)	X4_P0	X17_P0	X34_P0
A (output stable)	-5.152e-06	-1.904e-05	-3.716e-05
B (output stable)	-8.104e-06	-3.274e-05	-6.363e-05
C (output stable)	1.079e-05	-6.468e-06	-2.679e-07
D (output stable)	3.744e-05	1.657e-04	3.081e-04
A to Z	-1.217e-06	-8.918e-06	-1.167e-05
B to Z	-7.040e-07	-6.049e-06	-1.645e-05
C to Z	-2.560e-07	-4.975e-06	-8.101e-06
D to Z	5.263e-08	-1.933e-08	-5.460e-07

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X8_P0	1.200	2.176	2.6112
X13_P0	1.200	2.720	3.2640
X17_P0	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P0	X8_P0	X13_P0	X17_P0
A	0.0008	0.0015	0.0023	0.0030

B	0.0008	0.0014	0.0022	0.0029
C	0.0007	0.0015	0.0022	0.0029
D	0.0007	0.0014	0.0021	0.0027
E	0.0009	0.0014	0.0021	0.0028
F	0.0007	0.0014	0.0020	0.0026

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0159	0.0186	3.0365	1.7638
A to Z ↑	0.0419	0.0414	9.3710	4.3505
B to Z ↓	0.0169	0.0190	3.0705	1.7789
B to Z ↑	0.0391	0.0380	9.3505	4.3557
C to Z ↓	0.0148	0.0171	3.0130	1.7797
C to Z ↑	0.0369	0.0373	9.4043	4.3594
D to Z ↓	0.0153	0.0175	3.0556	1.8010
D to Z ↑	0.0339	0.0338	9.3499	4.3548
E to Z ↓	0.0117	0.0136	2.9657	1.7807
E to Z ↑	0.0274	0.0276	9.2793	4.3165
F to Z ↓	0.0114	0.0133	3.0216	1.8100
F to Z ↑	0.0242	0.0239	9.3330	4.3188
	X13_P0	X17_P0	X13_P0	X17_P0
A to Z ↓	0.0178	0.0180	1.2027	0.9193
A to Z ↑	0.0385	0.0390	2.8775	2.2001
B to Z ↓	0.0186	0.0184	1.2126	0.9271
B to Z ↑	0.0356	0.0355	2.8847	2.1987
C to Z ↓	0.0164	0.0165	1.2118	0.9100
C to Z ↑	0.0344	0.0349	2.8877	2.2097
D to Z ↓	0.0171	0.0165	1.2251	0.9204
D to Z ↑	0.0314	0.0314	2.8890	2.2041
E to Z ↓	0.0132	0.0132	1.2067	0.9109
E to Z ↑	0.0260	0.0261	2.8634	2.1828
F to Z ↓	0.0129	0.0123	1.2251	0.9256
F to Z ↑	0.0225	0.0224	2.8660	2.1904

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	5.836e-07	2.779e-12
X8_P0	1.141e-06	4.796e-12
X13_P0	1.561e-06	5.804e-12
X17_P0	2.088e-06	7.560e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	1.019e-04	2.258e-04	3.135e-04	4.186e-04
B (output stable)	2.270e-04	5.265e-04	6.650e-04	9.120e-04
C (output stable)	5.312e-05	1.225e-04	1.624e-04	2.302e-04
D (output stable)	7.690e-05	2.199e-04	2.597e-04	3.849e-04
E (output stable)	3.755e-05	9.381e-05	1.320e-04	1.810e-04
F (output stable)	5.394e-05	1.704e-04	2.097e-04	3.168e-04

A to Z	3.158e-03	6.643e-03	9.127e-03	1.219e-02
B to Z	2.920e-03	5.993e-03	8.304e-03	1.094e-02
C to Z	2.369e-03	5.199e-03	6.966e-03	9.298e-03
D to Z	2.154e-03	4.608e-03	6.218e-03	8.129e-03
E to Z	1.499e-03	3.426e-03	4.615e-03	6.099e-03
F to Z	1.298e-03	2.854e-03	3.839e-03	4.954e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

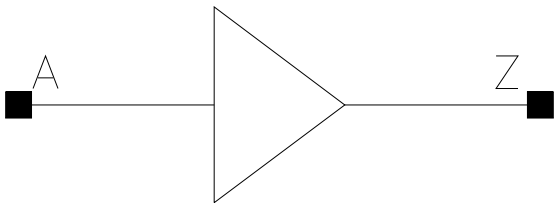
Pin Cycle (vdds)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	-1.499e-05	-3.284e-05	-3.736e-05	-5.054e-05
B (output stable)	-3.696e-05	-7.477e-05	-8.228e-05	-1.124e-04
C (output stable)	9.498e-07	-3.123e-07	3.104e-06	4.553e-06
D (output stable)	9.481e-06	1.417e-05	1.902e-05	2.332e-05
E (output stable)	4.362e-05	9.623e-05	1.106e-04	1.521e-04
F (output stable)	3.758e-05	8.330e-05	9.603e-05	1.308e-04
A to Z	-7.699e-06	-1.619e-05	-1.717e-05	-2.378e-05
B to Z	-8.169e-06	-1.590e-05	-1.687e-05	-2.234e-05
C to Z	-2.117e-06	-4.034e-06	-5.639e-06	-8.150e-06
D to Z	-2.115e-06	-4.982e-06	-5.063e-06	-7.249e-06
E to Z	-5.278e-07	-1.091e-06	-1.348e-06	-2.166e-06
F to Z	-4.763e-07	-1.040e-06	-8.330e-07	-1.812e-06

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X6_P0	1.200	0.408	0.4896
X8_P0	1.200	0.408	0.4896
X13_P0	1.200	0.544	0.6528
X16_P0	1.200	0.544	0.6528
X21_P0	1.200	0.680	0.8160
X25_P0	1.200	0.680	0.8160
X29_P0	1.200	0.952	1.1424
X33_P0	1.200	0.952	1.1424
X42_P0	1.200	1.088	1.3056
X50_P0	1.200	1.224	1.4688
X58_P0	1.200	1.496	1.7952
X67_P0	1.200	1.632	1.9584
X75_P0	1.200	1.768	2.1216
X84_P0	1.200	1.904	2.2848
X100_P0	1.200	2.312	2.7744
X134_P0	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0007	0.0008	0.0007	0.0008
	X16_P0	X21_P0	X25_P0	X29_P0
A	0.0007	0.0010	0.0010	0.0014
	X33_P0	X42_P0	X50_P0	X58_P0
A	0.0014	0.0016	0.0019	0.0027

	X67_P0	X75_P0	X84_P0	X100_P0
A	0.0028	0.0027	0.0027	0.0036
	X134_P0			
A	0.0046			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0256	0.0258	3.0890	2.2755
A to Z ↑	0.0191	0.0189	5.6517	4.1783
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0267	0.0297	1.6961	1.0915
A to Z ↑	0.0195	0.0217	3.0024	1.9511
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0316	0.0271	0.8726	0.6731
A to Z ↑	0.0228	0.0201	1.5025	1.1774
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0284	0.0270	0.5812	0.4890
A to Z ↑	0.0209	0.0194	0.9910	0.8406
	X33_P0	**X42_P0**	**X33_P0**	**X42_P0**
A to Z ↓	0.0281	0.0276	0.4354	0.3542
A to Z ↑	0.0202	0.0204	0.7399	0.5958
	X50_P0	**X58_P0**	**X50_P0**	**X58_P0**
A to Z ↓	0.0271	0.0254	0.2934	0.2537
A to Z ↑	0.0198	0.0189	0.4946	0.4257
	X67_P0	**X75_P0**	**X67_P0**	**X75_P0**
A to Z ↓	0.0264	0.0278	0.2226	0.2012
A to Z ↑	0.0196	0.0206	0.3730	0.3332
	X84_P0	**X100_P0**	**X84_P0**	**X100_P0**
A to Z ↓	0.0287	0.0273	0.1820	0.1534
A to Z ↑	0.0212	0.0203	0.3006	0.2520
	X134_P0		**X134_P0**	
A to Z ↓	0.0285		0.1193	
A to Z ↑	0.0214		0.1929	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	3.628e-07	1.519e-12
X6_P0	4.372e-07	1.518e-12
X8_P0	5.151e-07	1.519e-12
X13_P0	6.854e-07	1.772e-12
X16_P0	8.345e-07	1.771e-12
X21_P0	1.129e-06	2.022e-12
X25_P0	1.207e-06	2.022e-12
X29_P0	1.480e-06	2.526e-12
X33_P0	1.501e-06	2.526e-12
X42_P0	1.859e-06	2.777e-12
X50_P0	2.221e-06	3.030e-12
X58_P0	2.729e-06	3.541e-12
X67_P0	2.983e-06	3.788e-12
X75_P0	3.238e-06	4.040e-12

X84_P0	3.493e-06	4.290e-12
X100_P0	4.256e-06	5.053e-12
X134_P0	5.529e-06	6.306e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	1.590e-03	1.758e-03	2.061e-03	2.708e-03
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	3.204e-03	4.379e-03	4.909e-03	5.529e-03
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	6.038e-03	7.632e-03	8.872e-03	1.098e-02
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	1.201e-02	1.355e-02	1.457e-02	1.767e-02
	X134_P0			
A to Z	2.381e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

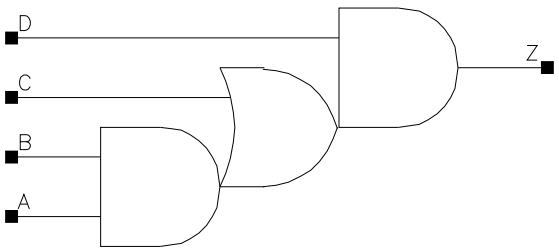
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	-1.509e-07	1.180e-07	8.740e-08	-6.284e-08
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	6.100e-08	1.494e-07	-2.070e-07	1.744e-07
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	2.130e-08	4.500e-08	1.060e-07	-7.900e-08
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	-2.130e-07	-1.068e-06	-5.880e-07	-4.700e-07
	X134_P0			
A to Z	-7.930e-07			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.632	1.9584
X25_P0	1.200	1.768	2.1216
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0009	0.0019	0.0019	0.0018
B	0.0009	0.0017	0.0017	0.0017
C	0.0010	0.0022	0.0022	0.0022
D	0.0014	0.0018	0.0018	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0362	0.0344	1.7348	0.8620
A to Z ↑	0.0297	0.0280	3.0312	1.4788
B to Z ↓	0.0339	0.0319	1.7300	0.8616
B to Z ↑	0.0296	0.0275	3.0303	1.4776
C to Z ↓	0.0303	0.0281	1.7271	0.8595
C to Z ↑	0.0226	0.0207	3.0104	1.4660

D to Z ↓	0.0288	0.0256	1.7086	0.8516
D to Z ↑	0.0261	0.0230	3.0125	1.4675
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0375	0.0392	0.5881	0.4434
A to Z ↑	0.0305	0.0316	1.0004	0.7517
B to Z ↓	0.0349	0.0373	0.5870	0.4427
B to Z ↑	0.0299	0.0316	1.0003	0.7519
C to Z ↓	0.0313	0.0336	0.5855	0.4411
C to Z ↑	0.0228	0.0241	0.9922	0.7444
D to Z ↓	0.0275	0.0288	0.5776	0.4336
D to Z ↑	0.0249	0.0259	0.9930	0.7455

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	7.377e-07	2.527e-12
X17_P0	1.373e-06	3.788e-12
X25_P0	1.620e-06	4.040e-12
X33_P0	1.868e-06	4.293e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	8.210e-05	1.612e-04	1.597e-04	1.592e-04
B (output stable)	1.023e-04	1.919e-04	1.964e-04	1.835e-04
C (output stable)	2.975e-04	4.927e-04	4.964e-04	4.783e-04
D (output stable)	9.774e-05	1.270e-04	1.241e-04	1.200e-04
A to Z	3.500e-03	6.386e-03	7.874e-03	8.884e-03
B to Z	3.265e-03	5.779e-03	7.231e-03	8.373e-03
C to Z	2.716e-03	4.640e-03	6.105e-03	7.186e-03
D to Z	3.562e-03	6.069e-03	7.512e-03	8.519e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

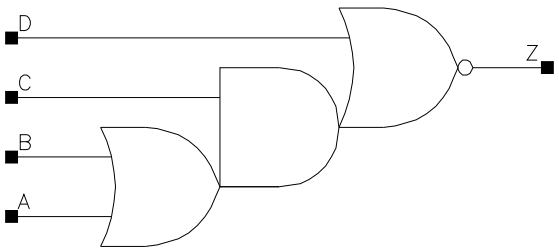
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	-2.479e-06	-4.873e-06	-4.889e-06	-4.705e-06
B (output stable)	-2.447e-06	-4.628e-06	-4.635e-06	-4.539e-06
C (output stable)	5.772e-06	8.617e-06	8.672e-06	9.097e-06
D (output stable)	1.814e-06	2.843e-06	2.882e-06	2.212e-06
A to Z	-1.148e-06	-1.193e-06	-1.001e-06	-2.446e-06
B to Z	-8.970e-07	-1.749e-06	-2.646e-06	-2.160e-06
C to Z	-2.793e-07	-4.440e-08	-6.277e-07	-1.738e-07
D to Z	-5.522e-07	-6.779e-07	-7.078e-07	-7.833e-07

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.952	1.1424
X11_P0	1.200	1.496	1.7952
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X16_P0	X21_P0
A	0.0008	0.0015	0.0023	0.0031
B	0.0008	0.0015	0.0024	0.0030
C	0.0008	0.0015	0.0022	0.0030
D	0.0011	0.0015	0.0023	0.0030

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0144	0.0139	2.9810	1.5790
A to Z ↑	0.0359	0.0334	9.6002	4.9918
B to Z ↓	0.0140	0.0136	2.8968	1.5488
B to Z ↑	0.0341	0.0321	9.6140	4.9972
C to Z ↓	0.0128	0.0121	2.7567	1.4629
C to Z ↑	0.0229	0.0212	6.2935	3.2312

D to Z ↓	0.0080	0.0068	1.7719	0.8982
D to Z ↑	0.0196	0.0170	6.7869	3.4935
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0139	0.0142	1.0653	0.8235
A to Z ↑	0.0313	0.0331	3.2109	2.4761
B to Z ↓	0.0133	0.0137	1.0734	0.8260
B to Z ↑	0.0307	0.0315	3.2149	2.4803
C to Z ↓	0.0123	0.0124	1.0068	0.7738
C to Z ↑	0.0206	0.0209	2.1351	1.6032
D to Z ↓	0.0069	0.0069	0.6292	0.4810
D to Z ↑	0.0159	0.0160	2.2909	1.7345

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P0	4.955e-07	2.528e-12
X11_P0	9.087e-07	3.537e-12
X16_P0	1.218e-06	4.040e-12
X21_P0	1.613e-06	5.300e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	5.273e-05	9.486e-05	1.227e-04	2.093e-04
B (output stable)	4.518e-05	9.466e-05	1.306e-04	1.930e-04
C (output stable)	2.369e-04	4.644e-04	6.374e-04	9.289e-04
D (output stable)	5.821e-05	1.184e-04	1.539e-04	2.399e-04
A to Z	2.539e-03	4.428e-03	6.212e-03	8.750e-03
B to Z	2.082e-03	3.663e-03	5.291e-03	7.183e-03
C to Z	1.759e-03	2.994e-03	4.321e-03	5.962e-03
D to Z	1.049e-03	1.756e-03	2.376e-03	3.165e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

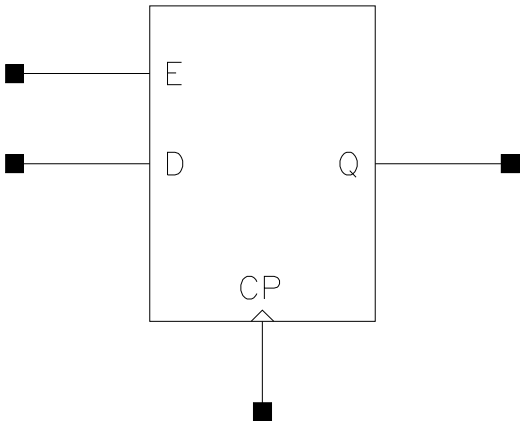
Pin Cycle (vdds)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	-6.916e-06	-1.002e-05	-1.264e-05	-2.277e-05
B (output stable)	4.850e-06	2.637e-06	1.140e-05	1.118e-05
C (output stable)	-2.670e-05	-4.805e-05	-6.596e-05	-1.012e-04
D (output stable)	6.120e-05	1.282e-04	1.738e-04	2.451e-04
A to Z	-3.174e-06	-3.270e-06	-6.146e-06	-9.388e-06
B to Z	-9.030e-07	-2.517e-06	-2.132e-06	-4.369e-06
C to Z	-1.609e-06	-3.470e-06	-3.415e-06	-6.247e-06
D to Z	-1.170e-07	2.804e-06	2.103e-06	1.209e-06

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.128	3.7536
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0011	0.0011	0.0011

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0391	0.0448	1.7275	0.8960
CP to Q ↑	0.0468	0.0494	3.0513	1.5277
	X33_P0		**X33_P0**	
CP to Q ↓	0.0654		0.4423	
CP to Q ↑	0.0788		0.7584	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0557	0.0557	0.0557
CP ↑	min_pulse_width to CP	0.0311	0.0396	0.0300
D ↓	hold_rising to CP	-0.0213	-0.0188	-0.0210
D ↑	hold_rising to CP	-0.0012	-0.0012	-0.0038
D ↓	setup_rising to CP	0.0583	0.0583	0.0583
D ↑	setup_rising to CP	0.0316	0.0316	0.0316
E ↓	hold_rising to CP	-0.0162	-0.0165	-0.0162
E ↑	hold_rising to CP	-0.0038	-0.0038	-0.0038
E ↓	setup_rising to CP	0.0553	0.0553	0.0553
E ↑	setup_rising to CP	0.0610	0.0610	0.0610

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	2.016e-06	6.309e-12
X17_P0	2.289e-06	6.560e-12
X33_P0	3.195e-06	7.569e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

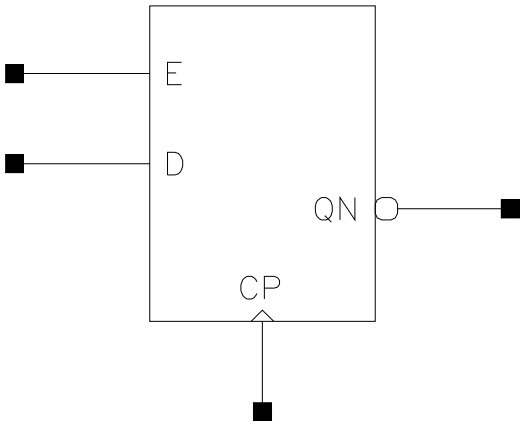
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.779e-03	3.780e-03	3.784e-03
Clock 100Mhz Data 25Mhz	8.061e-03	8.660e-03	1.121e-02
Clock 100Mhz Data 50Mhz	1.234e-02	1.354e-02	1.865e-02
Clock = 0 Data 100Mhz	4.821e-03	4.821e-03	4.821e-03
Clock = 1 Data 100Mhz	1.371e-03	1.371e-03	1.371e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.264	3.9168
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0011	0.0011	0.0011

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0648	0.0611	1.7746	0.8491
CP to QN ↑	0.0514	0.0532	3.0891	1.4844
	X33_P0		**X33_P0**	
CP to QN ↓	0.0649		0.4434	
CP to QN ↑	0.0585		0.7609	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0557	0.0557	0.0557
CP ↑	min_pulse_width to CP	0.0300	0.0311	0.0348
D ↓	hold_rising to CP	-0.0210	-0.0188	-0.0188
D ↑	hold_rising to CP	-0.0038	-0.0012	-0.0012
D ↓	setup_rising to CP	0.0583	0.0583	0.0583
D ↑	setup_rising to CP	0.0316	0.0316	0.0316
E ↓	hold_rising to CP	-0.0162	-0.0162	-0.0162
E ↑	hold_rising to CP	-0.0038	-0.0038	-0.0038
E ↓	setup_rising to CP	0.0553	0.0553	0.0553
E ↑	setup_rising to CP	0.0610	0.0610	0.0610

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	2.014e-06	6.308e-12
X17_P0	2.465e-06	6.812e-12
X33_P0	3.122e-06	7.569e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

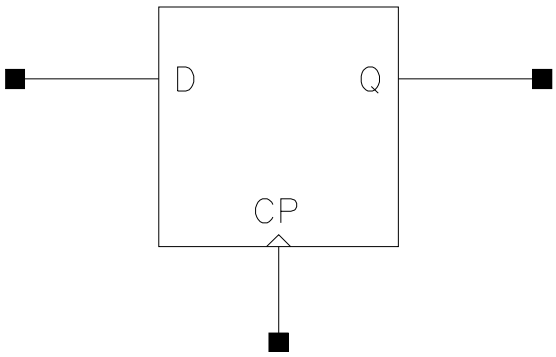
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.778e-03	3.778e-03	3.778e-03
Clock 100Mhz Data 25Mhz	8.117e-03	9.213e-03	1.101e-02
Clock 100Mhz Data 50Mhz	1.246e-02	1.465e-02	1.824e-02
Clock = 0 Data 100Mhz	4.827e-03	4.827e-03	4.826e-03
Clock = 1 Data 100Mhz	1.370e-03	1.370e-03	1.370e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.176	2.6112
X17_P0	1.200	2.448	2.9376
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0404	0.0447	1.7205	0.8897
CP to Q ↑	0.0472	0.0518	2.9520	1.4988
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to Q ↓	0.0567	0.0584	0.5327	0.4840
CP to Q ↑	0.0576	0.0588	0.8428	0.7692

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0509	0.0509	0.0509	0.0509
CP ↑	min_pulse_width to CP	0.0311	0.0359	0.0493	0.0493
D ↓	hold_rising to CP	0.0052	0.0056	0.0056	0.0056
D ↑	hold_rising to CP	0.0100	0.0103	0.0103	0.0103
D ↓	setup_rising to CP	0.0291	0.0347	0.0347	0.0347
D ↑	setup_rising to CP	0.0145	0.0167	0.0171	0.0171

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	1.610e-06	4.797e-12
X17_P0	1.912e-06	5.300e-12
X30_P0	2.432e-06	5.804e-12
X33_P0	2.427e-06	5.805e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

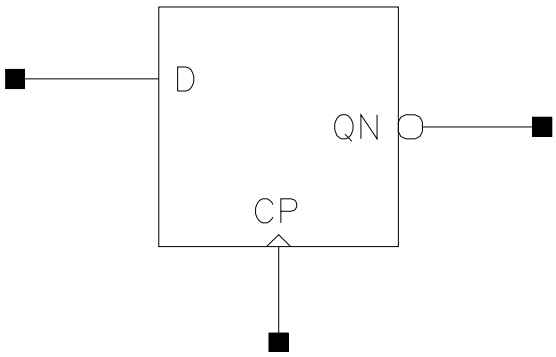
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.977e-03	3.999e-03	4.006e-03	4.010e-03
Clock 100Mhz Data 25Mhz	7.149e-03	8.101e-03	9.479e-03	9.724e-03
Clock 100Mhz Data 50Mhz	1.032e-02	1.220e-02	1.495e-02	1.544e-02
Clock = 0 Data 100Mhz	3.229e-03	3.331e-03	3.363e-03	3.379e-03
Clock = 1 Data 100Mhz	4.072e-05	4.089e-05	4.101e-05	4.107e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0390	0.0464	1.7802	0.9195
CP to QN ↑	0.0414	0.0437	2.9445	1.4990
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to QN ↓	0.0648	0.0650	0.4868	0.4417
CP to QN ↑	0.0542	0.0626	0.8146	0.7598

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0472	0.0472	0.0509	0.0509
CP ↑	min_pulse_width to CP	0.0311	0.0348	0.0311	0.0359
D ↓	hold_rising to CP	0.0105	0.0127	0.0056	0.0052
D ↑	hold_rising to CP	0.0100	0.0131	0.0103	0.0100
D ↓	setup_rising to CP	0.0246	0.0246	0.0347	0.0291
D ↑	setup_rising to CP	0.0167	0.0167	0.0167	0.0145

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	1.502e-06	4.293e-12
X17_P0	1.780e-06	4.545e-12
X30_P0	2.617e-06	5.805e-12
X33_P0	2.716e-06	6.080e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

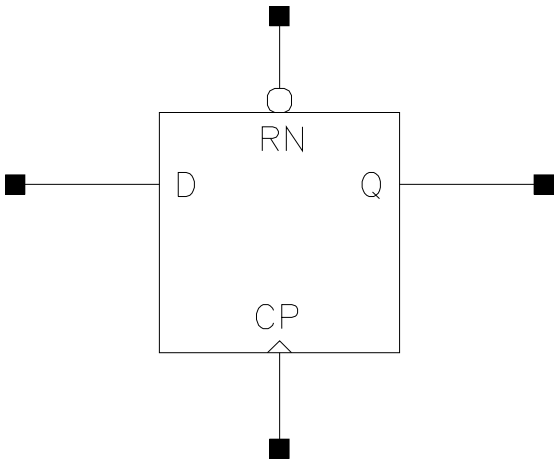
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.812e-03	3.813e-03	3.884e-03	3.914e-03
Clock 100Mhz Data 25Mhz	6.752e-03	7.416e-03	9.594e-03	1.005e-02
Clock 100Mhz Data 50Mhz	9.693e-03	1.102e-02	1.530e-02	1.619e-02
Clock = 0 Data 100Mhz	2.861e-03	2.861e-03	3.050e-03	3.096e-03
Clock = 1 Data 100Mhz	4.047e-05	4.051e-05	4.082e-05	4.099e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0465	0.0579	0.8991	0.5399
CP to Q ↑	0.0535	0.0590	1.5035	0.8459
RN to Q ↓	0.0721	0.0936	0.9518	0.5719

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0557	0.0557
CP ↑	min_pulse_width to CP	0.0396	0.0493
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0078	0.0078
D ↓	setup_rising to CP	0.0340	0.0340
D ↑	setup_rising to CP	0.0219	0.0219
RN ↓	min_pulse_width to RN	0.0925	0.1165
RN ↑	recovery_rising to CP	0.0201	0.0201
RN ↑	removal_rising to CP	-0.0073	-0.0073

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P0	2.064e-06	6.561e-12
X30_P0	2.558e-06	7.064e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

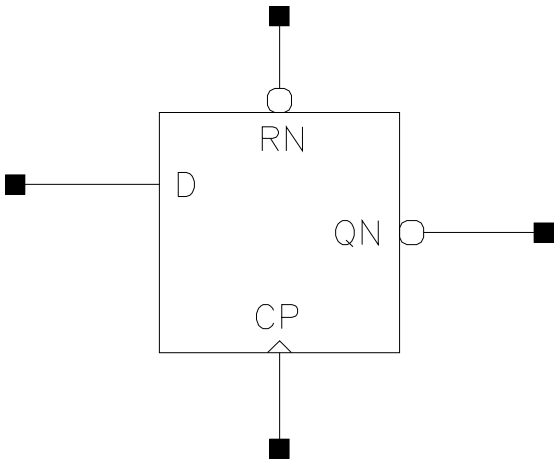
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	4.274e-03	4.274e-03
Clock 100Mhz Data 25Mhz	8.666e-03	1.000e-02
Clock 100Mhz Data 50Mhz	1.306e-02	1.573e-02
Clock = 0 Data 100Mhz	3.983e-03	3.986e-03
Clock = 1 Data 100Mhz	4.145e-05	4.166e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0626	0.0676	0.8410	0.4888
CP to QN ↑	0.0530	0.0568	1.4725	0.8192
RN to QN ↑	0.0769	0.0819	1.4776	0.8230

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0557	0.0557
CP ↑	min_pulse_width to CP	0.0311	0.0311
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0078	0.0078
D ↓	setup_rising to CP	0.0340	0.0340
D ↑	setup_rising to CP	0.0219	0.0219
RN ↓	min_pulse_width to RN	0.0774	0.0801
RN ↑	recovery_rising to CP	0.0171	0.0171
RN ↑	removal_rising to CP	-0.0073	-0.0073

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P0	2.362e-06	6.561e-12
X30_P0	2.880e-06	7.065e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

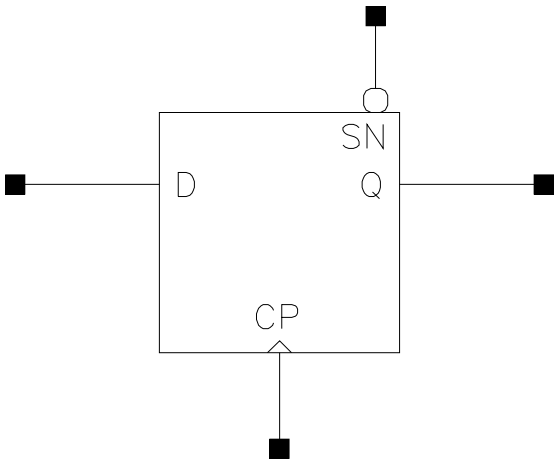
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	4.287e-03	4.286e-03
Clock 100Mhz Data 25Mhz	9.171e-03	1.038e-02
Clock 100Mhz Data 50Mhz	1.406e-02	1.647e-02
Clock = 0 Data 100Mhz	4.030e-03	4.017e-03
Clock = 1 Data 100Mhz	4.145e-05	4.154e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0011	0.0011

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0470	0.0588	0.8996	0.5374
CP to Q ↑	0.0530	0.0588	1.5038	0.8458
SN to Q ↑	0.0551	0.0622	1.5067	0.8469

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0557	0.0557
CP ↑	min_pulse_width to CP	0.0396	0.0492
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0392	0.0392
D ↑	setup_rising to CP	0.0167	0.0167
SN ↓	min_pulse_width to SN	0.0522	0.0598
SN ↑	recovery_rising to CP	0.0107	0.0076
SN ↑	removal_rising to CP	0.0241	0.0238

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P0	2.150e-06	6.560e-12
X30_P0	2.679e-06	7.064e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

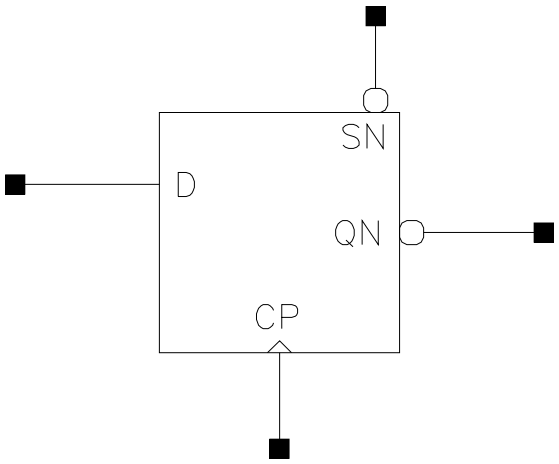
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	4.315e-03	4.307e-03
Clock 100Mhz Data 25Mhz	8.727e-03	1.004e-02
Clock 100Mhz Data 50Mhz	1.314e-02	1.577e-02
Clock = 0 Data 100Mhz	3.962e-03	3.961e-03
Clock = 1 Data 100Mhz	3.377e-05	3.385e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0011	0.0011

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0621	0.0670	0.8442	0.4897
CP to QN ↑	0.0534	0.0572	1.4694	0.8186
SN to QN ↓	0.0640	0.0691	0.8441	0.4899

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0557	0.0557
CP ↑	min_pulse_width to CP	0.0311	0.0311
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0392	0.0392
D ↑	setup_rising to CP	0.0167	0.0167
SN ↓	min_pulse_width to SN	0.0496	0.0496
SN ↑	recovery_rising to CP	0.0107	0.0107
SN ↑	removal_rising to CP	0.0241	0.0238

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P0	2.265e-06	6.561e-12
X30_P0	2.738e-06	7.065e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

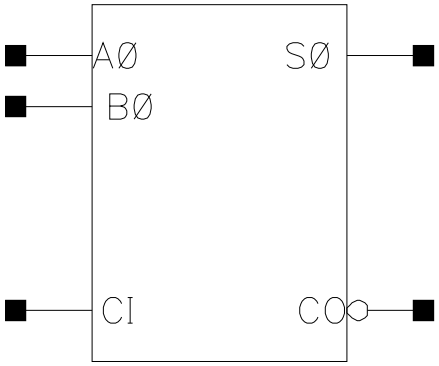
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	4.336e-03	4.334e-03
Clock 100Mhz Data 25Mhz	9.204e-03	1.040e-02
Clock 100Mhz Data 50Mhz	1.407e-02	1.647e-02
Clock = 0 Data 100Mhz	3.958e-03	3.958e-03
Clock = 1 Data 100Mhz	4.142e-05	4.149e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_P0	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_-P0	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_-P0	1.200	3.672	4.4064
C12T28SOI_LRS1_-FA1X33_P0	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0
A0	0.0030	0.0061	0.0027	0.0054
B0	0.0027	0.0059	0.0029	0.0052
CI	0.0020	0.0045	0.0020	0.0036

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0
A0 to CO ↓	0.0469	0.0505	1.7928	0.4767
A0 to CO ↑	0.0315	0.0323	3.0354	0.7833
A0 to S0 ↓	0.0466	0.0585	1.7683	0.4649
A0 to S0 ↑	0.0478	0.0573	3.0093	0.7721
B0 to CO ↓	0.0458	0.0503	1.8009	0.4795
B0 to CO ↑	0.0321	0.0333	3.0366	0.7795
B0 to S0 ↓	0.0467	0.0590	1.7689	0.4649
B0 to S0 ↑	0.0476	0.0577	3.0134	0.7726
CI to CO ↓	0.0438	0.0486	1.8077	0.4795
CI to CO ↑	0.0317	0.0323	3.0359	0.7832
CI to S0 ↓	0.0458	0.0580	1.7682	0.4646
CI to S0 ↑	0.0472	0.0575	3.0112	0.7723
	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0
A0 to CO ↓	0.0310	0.0374	3.4994	0.6075
A0 to CO ↑	0.0242	0.0272	3.0937	0.7694
A0 to S0 ↓	0.0614	0.0745	1.9146	0.4873
A0 to S0 ↑	0.0558	0.0601	3.1328	0.7877
B0 to CO ↓	0.0313	0.0381	3.4986	0.6086
B0 to CO ↑	0.0229	0.0265	3.0914	0.7695
B0 to S0 ↓	0.0616	0.0762	1.9151	0.4875
B0 to S0 ↑	0.0560	0.0617	3.1328	0.7881
CI to CO ↓	0.0304	0.0502	3.4943	0.6180
CI to CO ↑	0.0256	0.0300	3.1757	0.7750
CI to S0 ↓	0.0361	0.0459	1.9173	0.4877
CI to S0 ↑	0.0304	0.0304	3.1342	0.7883

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_FA1X8_P0	1.728e-06	4.796e-12
C12T28SOI_LR_FA1X33_P0	4.485e-06	9.835e-12
C12T28SOI_LRS1_FA1X8_P0	3.764e-06	7.568e-12
C12T28SOI_LRS1_FA1X33_P0	7.739e-06	1.563e-11

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0
A0 to CO	3.664e-03	1.006e-02	5.634e-03	1.368e-02
A0 to S0	3.711e-03	1.052e-02	7.568e-03	1.702e-02
B0 to CO	3.599e-03	1.001e-02	5.661e-03	1.386e-02
B0 to S0	3.530e-03	1.022e-02	7.634e-03	1.728e-02
CI to CO	3.566e-03	9.981e-03	4.002e-03	1.211e-02
CI to S0	3.481e-03	1.014e-02	4.497e-03	1.304e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0
A0 to CO	-1.562e-05	-3.041e-05	5.443e-06	1.219e-05

A0 to S0	-1.230e-05	-2.326e-05	7.878e-06	1.724e-05
B0 to CO	4.000e-06	7.756e-06	-1.632e-06	-4.561e-06
B0 to S0	1.494e-05	2.887e-05	1.170e-06	9.517e-07
CI to CO	2.119e-05	4.079e-05	-2.070e-08	-7.795e-07
CI to S0	1.588e-05	2.802e-05	-2.148e-07	3.837e-07

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X33_P0	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X33_P0
A0	0.0010	0.0030
B0	0.0009	0.0026

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
A0 to CO ↓	0.0339	0.0316	1.7658	0.4403
A0 to CO ↑	0.0294	0.0269	2.9982	0.7741
A0 to S0 ↓	0.0426	0.0413	1.7316	0.4406
A0 to S0 ↑	0.0404	0.0444	2.9668	0.7645
B0 to CO ↓	0.0330	0.0295	1.7658	0.4370
B0 to CO ↑	0.0309	0.0276	2.9992	0.7741
B0 to S0 ↓	0.0434	0.0405	1.7323	0.4407
B0 to S0 ↑	0.0397	0.0426	2.9681	0.7646

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	1.031e-06	3.030e-12
X33_P0	3.910e-06	6.307e-12

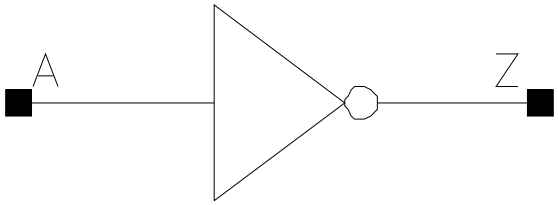
Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X33_P0
A0 to CO	2.781e-03	9.111e-03
A0 to S0	2.559e-03	8.777e-03
B0 to CO	2.784e-03	8.957e-03
B0 to S0	2.494e-03	8.311e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X8_P0	X33_P0
A0 to CO	-3.082e-06	-2.446e-05
A0 to S0	-1.630e-06	-1.359e-05
B0 to CO	7.393e-06	4.389e-05
B0 to S0	3.742e-06	2.161e-05

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.272	0.3264
X6_P0	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X13_P0	1.200	0.408	0.4896
X17_P0	1.200	0.408	0.4896
X21_P0	1.200	0.544	0.6528
X25_P0	1.200	0.544	0.6528
X29_P0	1.200	0.680	0.8160
X33_P0	1.200	0.680	0.8160
X50_P0	1.200	0.952	1.1424
X58_P0	1.200	1.088	1.3056
X67_P0	1.200	1.224	1.4688
X75_P0	1.200	1.360	1.6320
X84_P0	1.200	1.496	1.7952
X100_P0	1.200	1.768	2.1216
X134_P0	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0005	0.0006	0.0008	0.0012
	X17_P0	X21_P0	X25_P0	X29_P0
A	0.0015	0.0020	0.0023	0.0028
	X33_P0	X50_P0	X58_P0	X67_P0
A	0.0030	0.0046	0.0054	0.0062
	X75_P0	X84_P0	X100_P0	X134_P0

A	0.0071	0.0079	0.0097	0.0134

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0074	0.0069	3.2926	2.5515
A to Z ↑	0.0138	0.0127	5.8167	4.4062
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0061	0.0052	1.7481	1.1314
A to Z ↑	0.0116	0.0106	3.0621	2.0136
	X17_P0	**X21_P0**	**X17_P0**	**X21_P0**
A to Z ↓	0.0051	0.0056	0.8720	0.7000
A to Z ↑	0.0102	0.0107	1.5097	1.2123
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0055	0.0052	0.5998	0.5081
A to Z ↑	0.0104	0.0100	1.0162	0.8675
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0051	0.0053	0.4510	0.3052
A to Z ↑	0.0097	0.0097	0.7621	0.5105
	X58_P0	**X67_P0**	**X58_P0**	**X67_P0**
A to Z ↓	0.0057	0.0056	0.2650	0.2329
A to Z ↑	0.0101	0.0099	0.4403	0.3858
	X75_P0	**X84_P0**	**X75_P0**	**X84_P0**
A to Z ↓	0.0060	0.0061	0.2105	0.1906
A to Z ↑	0.0103	0.0103	0.3462	0.3137
	X100_P0	**X134_P0**	**X100_P0**	**X134_P0**
A to Z ↓	0.0067	0.0074	0.1629	0.1277
A to Z ↑	0.0107	0.0113	0.2647	0.2041

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.923e-07	1.268e-12
X6_P0	2.401e-07	1.268e-12
X8_P0	3.375e-07	1.268e-12
X13_P0	5.301e-07	1.519e-12
X17_P0	6.588e-07	1.519e-12
X21_P0	8.344e-07	1.772e-12
X25_P0	9.192e-07	1.770e-12
X29_P0	1.127e-06	2.023e-12
X33_P0	1.173e-06	2.023e-12
X50_P0	1.680e-06	2.528e-12
X58_P0	1.935e-06	2.781e-12
X67_P0	2.189e-06	3.035e-12
X75_P0	2.444e-06	3.284e-12
X84_P0	2.698e-06	3.537e-12
X100_P0	3.208e-06	4.036e-12
X134_P0	4.226e-06	5.048e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0

A to Z	4.532e-04	5.364e-04	6.669e-04	9.058e-04
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	1.124e-03	1.577e-03	1.783e-03	1.958e-03
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	2.116e-03	3.139e-03	3.891e-03	4.183e-03
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	4.923e-03	5.274e-03	6.338e-03	8.668e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

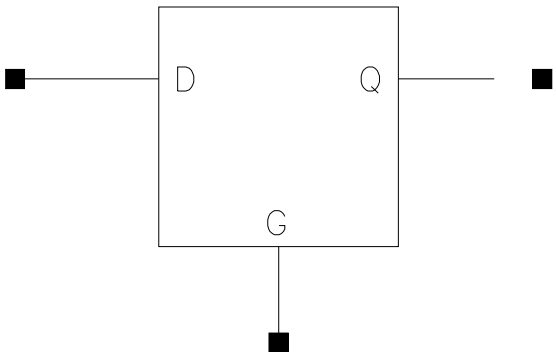
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	1.419e-07	1.009e-06	5.675e-07	2.061e-07
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	9.700e-08	5.600e-07	9.140e-07	5.300e-08
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	-4.730e-07	-7.440e-07	-1.525e-06	-3.357e-06
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	2.423e-06	1.391e-06	1.192e-05	1.667e-06

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X23_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P0	X23_P0
D	0.0005	0.0012
G	0.0011	0.0017

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X23_P0	X8_P0	X23_P0
D to Q ↓	0.0518	0.0416	1.8146	0.8438
D to Q ↑	0.0311	0.0312	2.9599	0.7855
G to Q ↓	0.0517	0.0410	1.8100	0.8419
G to Q ↑	0.0300	0.0280	2.9606	0.7860

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X23_P0
D ↓	hold_falling to G	-0.0113	-0.0042
D ↑	hold_falling to G	-0.0006	-0.0002
D ↓	setup_falling to G	0.0511	0.0362
D ↑	setup_falling to G	0.0320	0.0350
G ↑	min_pulse_width to G	0.0443	0.0418

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	8.886e-07	3.032e-12
X23_P0	1.838e-06	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X23_P0
D (output stable)	2.457e-05	1.018e-04
G (output stable)	9.505e-04	1.833e-03
D to Q	4.342e-03	8.450e-03
G to Q	4.005e-03	7.502e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

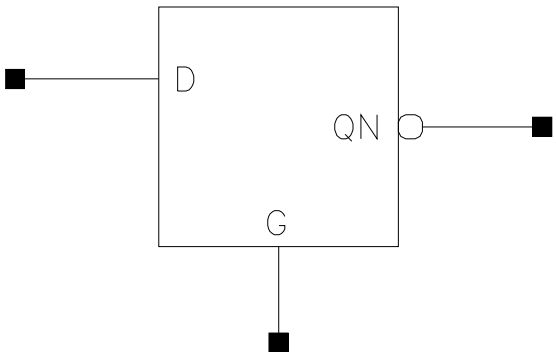
Pin Cycle (vdds)	X8_P0	X23_P0
D (output stable)	-1.594e-06	-6.092e-06
G (output stable)	5.441e-06	1.397e-05
D to Q	-2.445e-06	-3.994e-06
G to Q	4.503e-05	2.337e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P0
D	0.0006
G	0.0013

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P0	X17_P0
D to QN ↓	0.0408	0.8460
D to QN ↑	0.0566	1.4591
G to QN ↓	0.0391	0.8458
G to QN ↑	0.0545	1.4595

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P0
D ↓	hold_falling to G	-0.0140
D ↑	hold_falling to G	-0.0006
D ↓	setup_falling to G	0.0410
D ↑	setup_falling to G	0.0250
G ↑	min_pulse_width to G	0.0348

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P0	1.330e-06	3.284e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X17_P0
D (output stable)	3.591e-05
G (output stable)	1.068e-03
D to QN	5.489e-03
G to QN	5.042e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

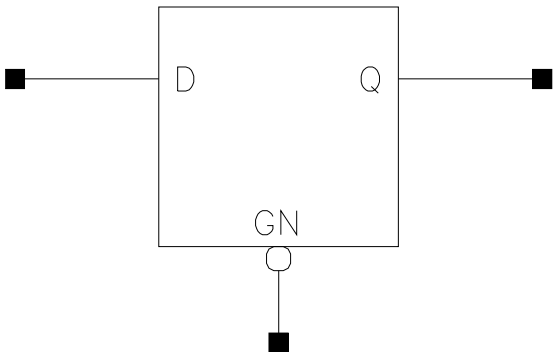
Pin Cycle (vdds)	X17_P0
D (output stable)	-5.539e-06
G (output stable)	9.660e-06
D to QN	-2.259e-06
G to QN	8.091e-05

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
D	0.0005	0.0007	0.0016
GN	0.0011	0.0014	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D to Q ↓	0.0523	0.0459	1.8200	0.8930
D to Q ↑	0.0318	0.0296	2.9618	1.5194
GN to Q ↓	0.0469	0.0404	1.8223	0.8950
GN to Q ↑	0.0474	0.0457	2.9593	1.5178

	X33_P0		X33_P0	
D to Q ↓	0.0441		0.4569	
D to Q ↑	0.0256		0.7627	
GN to Q ↓	0.0381		0.4574	
GN to Q ↑	0.0361		0.7615	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X33_P0
D ↓	hold_rising to GN	-0.0171	-0.0118	-0.0121
D ↑	hold_rising to GN	0.0029	0.0029	0.0082
D ↓	setup_rising to GN	0.0567	0.0518	0.0466
D ↑	setup_rising to GN	0.0286	0.0267	0.0212
GN ↓	min_pulse_width to GN	0.0626	0.0568	0.0521

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	8.391e-07	3.032e-12
X17_P0	1.304e-06	3.537e-12
X33_P0	2.116e-06	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
D (output stable)	2.705e-05	4.486e-05	1.147e-04
GN (output stable)	9.486e-04	1.302e-03	1.552e-03
D to Q	4.352e-03	6.068e-03	9.796e-03
GN to Q	6.207e-03	8.408e-03	1.227e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

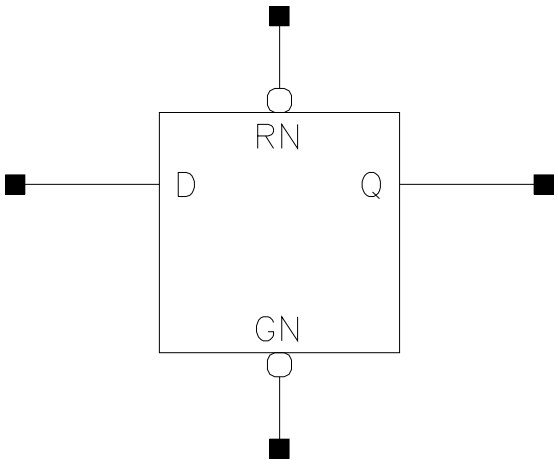
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
D (output stable)	-1.575e-06	-2.346e-06	-6.005e-06
GN (output stable)	5.220e-06	1.031e-05	1.468e-05
D to Q	-2.454e-06	-2.706e-06	-4.162e-06
GN to Q	-5.291e-05	-3.133e-05	-4.549e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.496	1.7952
X33_P0	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X33_P0
D	0.0005	0.0013
GN	0.0012	0.0023
RN	0.0005	0.0006

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
D to Q ↓	0.0491	0.0446	1.7658	0.4602
D to Q ↑	0.0401	0.0493	3.0067	0.7831

GN to Q ↓	0.0444	0.0411	1.7673	0.4609
GN to Q ↑	0.0533	0.0544	3.0077	0.7826
RN to Q ↓	0.0383	0.0673	1.7001	0.5018
RN to Q ↑	0.0418	0.0538	3.0088	0.7837

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X33_P0
D ↓	hold_rising to GN	-0.0118	-0.0070
D ↑	hold_rising to GN	-0.0038	-0.0135
D ↓	setup_rising to GN	0.0518	0.0470
D ↑	setup_rising to GN	0.0365	0.0536
GN ↓	min_pulse_width to GN	0.0578	0.0570
RN ↓	min_pulse_width to RN	0.0464	0.0828
RN ↑	recovery_rising to GN	0.0417	0.0581
RN ↑	removal_rising to GN	-0.0268	-0.0385

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	8.373e-07	3.536e-12
X33_P0	1.879e-06	5.301e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X33_P0
D (output stable)	8.286e-05	1.226e-04
GN (output stable)	1.103e-03	1.646e-03
RN (output stable)	2.645e-05	4.830e-05
D to Q	4.286e-03	1.060e-02
GN to Q	6.285e-03	1.361e-02
RN to Q	3.387e-03	8.267e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

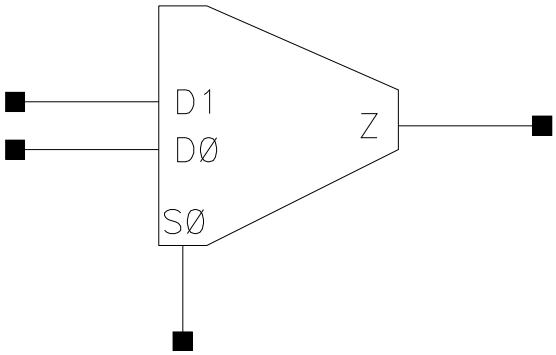
Pin Cycle (vdds)	X8_P0	X33_P0
D (output stable)	-3.957e-06	-9.054e-06
GN (output stable)	4.423e-06	1.183e-05
RN (output stable)	1.303e-06	1.656e-06
D to Q	-2.512e-06	-3.398e-06
GN to Q	-5.001e-05	2.562e-05
RN to Q	2.723e-06	-2.134e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
D0	0.0007	0.0010	0.0013	0.0018
D1	0.0007	0.0010	0.0013	0.0018
S0	0.0013	0.0014	0.0016	0.0023

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D0 to Z ↓	0.0401	0.0362	1.7673	0.8677
D0 to Z ↑	0.0297	0.0273	3.0393	1.4899
D1 to Z ↓	0.0383	0.0358	1.7621	0.8665
D1 to Z ↑	0.0273	0.0258	3.0374	1.4884
S0 to Z ↓	0.0340	0.0329	1.7570	0.8638
S0 to Z ↑	0.0316	0.0316	3.0356	1.4886

	X25_P0	X33_P0	X25_P0	X33_P0
D0 to Z ↓	0.0381	0.0347	0.6000	0.4493
D0 to Z ↑	0.0294	0.0271	1.0026	0.7506
D1 to Z ↓	0.0407	0.0361	0.6026	0.4501
D1 to Z ↑	0.0281	0.0261	1.0004	0.7502
S0 to Z ↓	0.0376	0.0346	0.5993	0.4485
S0 to Z ↑	0.0352	0.0323	1.0007	0.7503

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	1.051e-06	3.032e-12
X17_P0	1.754e-06	3.284e-12
X25_P0	2.421e-06	5.050e-12
X33_P0	3.290e-06	5.301e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	8.741e-04	1.264e-03	1.380e-03	1.851e-03
D1 (output stable)	7.086e-04	1.164e-03	1.550e-03	1.944e-03
S0 (output stable)	1.132e-03	1.276e-03	1.654e-03	2.022e-03
D0 to Z	3.015e-03	4.854e-03	7.467e-03	9.358e-03
D1 to Z	2.759e-03	4.702e-03	7.531e-03	9.247e-03
S0 to Z	3.461e-03	5.169e-03	8.384e-03	1.023e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

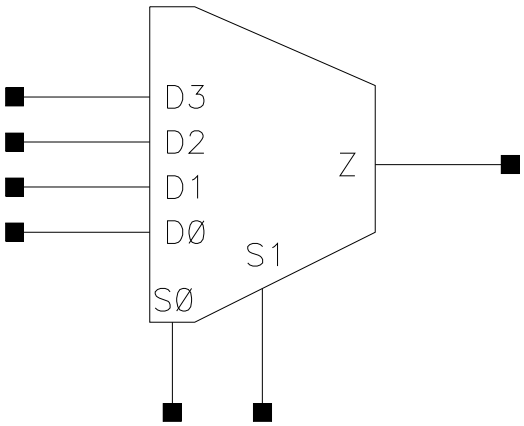
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	2.700e-09	4.210e-07	3.570e-07	6.060e-07
D1 (output stable)	4.005e-08	1.098e-06	-5.200e-08	6.615e-07
S0 (output stable)	6.940e-08	1.238e-07	4.640e-08	-1.908e-07
D0 to Z	-3.018e-07	-3.039e-07	-4.770e-07	-2.075e-07
D1 to Z	2.410e-08	5.475e-08	-1.760e-07	-4.155e-07
S0 to Z	-9.942e-08	-2.872e-07	-4.501e-07	-2.463e-07

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.312	2.7744
X31_P0	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P0	X31_P0
D0	0.0005	0.0014
D1	0.0005	0.0014
D2	0.0005	0.0014
D3	0.0005	0.0014
S0	0.0018	0.0036
S1	0.0011	0.0023

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X31_P0	X8_P0	X31_P0

D0 to Z ↓	0.0698	0.0718	1.8564	0.5175
D0 to Z ↑	0.0411	0.0427	3.0510	0.8231
D1 to Z ↓	0.0692	0.0720	1.8538	0.5175
D1 to Z ↑	0.0413	0.0425	3.0507	0.8231
D2 to Z ↓	0.0748	0.0672	1.8682	0.5119
D2 to Z ↑	0.0431	0.0395	3.0585	0.8175
D3 to Z ↓	0.0746	0.0668	1.8677	0.5112
D3 to Z ↑	0.0426	0.0408	3.0567	0.8207
S0 to Z ↓	0.0747	0.0755	1.8585	0.5139
S0 to Z ↑	0.0516	0.0537	3.0564	0.8219
S1 to Z ↓	0.0536	0.0522	1.8614	0.5145
S1 to Z ↑	0.0396	0.0408	3.0522	0.8207

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	1.035e-06	5.048e-12
X31_P0	2.940e-06	9.333e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X31_P0
D0 (output stable)	5.001e-05	2.087e-04
D1 (output stable)	5.153e-05	2.239e-04
D2 (output stable)	4.364e-05	1.133e-04
D3 (output stable)	4.799e-05	1.942e-04
S0 (output stable)	1.740e-03	3.970e-03
S1 (output stable)	1.162e-03	2.462e-03
D0 to Z	3.229e-03	1.083e-02
D1 to Z	3.220e-03	1.088e-02
D2 to Z	3.470e-03	1.012e-02
D3 to Z	3.459e-03	1.011e-02
S0 to Z	5.124e-03	1.479e-02
S1 to Z	3.615e-03	1.008e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

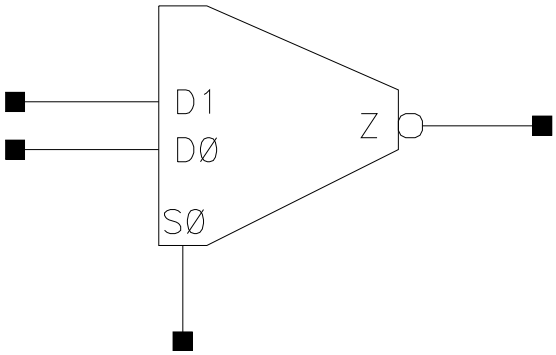
Pin Cycle (vdds)	X8_P0	X31_P0
D0 (output stable)	-3.504e-06	-1.605e-05
D1 (output stable)	-2.945e-06	-1.172e-05
D2 (output stable)	-2.763e-06	8.037e-07
D3 (output stable)	-3.270e-06	-7.154e-06
S0 (output stable)	-2.319e-05	-7.407e-05
S1 (output stable)	2.975e-05	1.249e-04
D0 to Z	-1.966e-06	-6.713e-06
D1 to Z	-2.121e-06	-6.796e-06
D2 to Z	-2.136e-06	-3.769e-06
D3 to Z	-2.042e-06	-3.964e-06
S0 to Z	-1.621e-05	-5.000e-05
S1 to Z	3.810e-05	1.617e-04

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.816	0.9792
X5_P0	1.200	0.952	1.1424
X10_P0	1.200	1.768	2.1216
X16_P0	1.200	2.448	2.9376
X21_P0	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P0	X5_P0	X10_P0	X16_P0
D0	0.0005	0.0008	0.0016	0.0024
D1	0.0005	0.0008	0.0015	0.0023
S0	0.0011	0.0019	0.0024	0.0036
	X21_P0			
D0	0.0031			
D1	0.0031			
S0	0.0041			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X5_P0	X3_P0	X5_P0
D0 to Z ↓	0.0136	0.0135	5.6313	3.5449

D0 to Z ↑	0.0250	0.0229	13.3331	6.9269
D1 to Z ↓	0.0134	0.0130	5.5819	3.3464
D1 to Z ↑	0.0258	0.0239	13.3484	7.1835
S0 to Z ↓	0.0205	0.0171	5.5940	3.4469
S0 to Z ↑	0.0226	0.0189	13.3201	7.0512
	X10_P0	**X16_P0**	**X10_P0**	**X16_P0**
D0 to Z ↓	0.0149	0.0140	1.6735	1.0951
D0 to Z ↑	0.0248	0.0237	3.2354	2.1366
D1 to Z ↓	0.0137	0.0135	1.6106	1.0655
D1 to Z ↑	0.0248	0.0243	3.2879	2.1575
S0 to Z ↓	0.0209	0.0181	1.6404	1.0802
S0 to Z ↑	0.0223	0.0194	3.2609	2.1479
	X21_P0		**X21_P0**	
D0 to Z ↓	0.0139		0.8389	
D0 to Z ↑	0.0232		1.6200	
D1 to Z ↓	0.0135		0.8102	
D1 to Z ↑	0.0243		1.6104	
S0 to Z ↓	0.0190		0.8241	
S0 to Z ↑	0.0199		1.6149	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P0	3.874e-07	2.276e-12
X5_P0	7.704e-07	2.528e-12
X10_P0	1.308e-06	4.042e-12
X16_P0	1.968e-06	5.300e-12
X21_P0	2.401e-06	6.560e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	2.743e-05	5.583e-05	1.877e-04	2.864e-04
D1 (output stable)	3.627e-05	1.507e-04	1.891e-04	3.076e-04
S0 (output stable)	9.521e-04	1.359e-03	2.387e-03	3.669e-03
D0 to Z	9.348e-04	1.558e-03	3.862e-03	5.413e-03
D1 to Z	9.343e-04	1.542e-03	3.672e-03	5.356e-03
S0 to Z	1.626e-03	2.286e-03	4.793e-03	6.685e-03
	X21_P0			
D0 (output stable)	3.678e-04			
D1 (output stable)	4.533e-04			
S0 (output stable)	4.090e-03			
D0 to Z	6.942e-03			
D1 to Z	7.069e-03			
S0 to Z	8.163e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	-1.636e-06	-2.570e-06	-7.191e-06	-1.580e-05
D1 (output stable)	-5.780e-06	-2.847e-05	-2.289e-05	-3.987e-05
S0 (output stable)	1.023e-05	4.279e-05	4.242e-05	6.619e-05
D0 to Z	-3.555e-07	5.180e-07	-7.155e-07	-2.148e-06

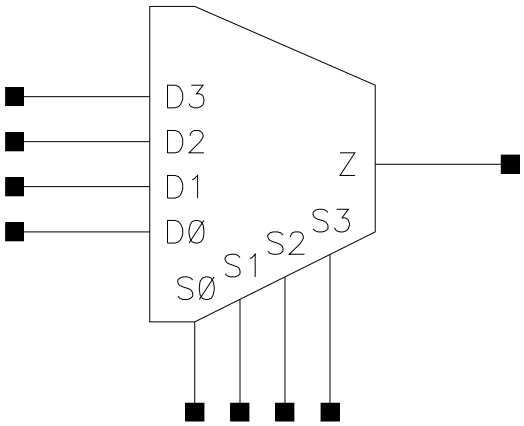
D1 to Z	-4.692e-07	-1.296e-06	-1.529e-06	-3.697e-06
S0 to Z	1.159e-05	3.223e-05	4.846e-05	8.898e-05
	X21_P0			
D0 (output stable)	-1.943e-05			
D1 (output stable)	-6.979e-05			
S0 (output stable)	1.014e-04			
D0 to Z	1.546e-06			
D1 to Z	-5.170e-06			
S0 to Z	1.125e-04			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	1.768	2.1216
X27_P0	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P0	X27_P0
D0	0.0006	0.0018
D1	0.0006	0.0019
D2	0.0006	0.0018
D3	0.0006	0.0019
S0	0.0006	0.0017
S1	0.0007	0.0018
S2	0.0006	0.0017
S3	0.0007	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	X27_P0	X7_P0	X27_P0
D0 to Z ↓	0.0534	0.0450	2.9187	0.8071
D0 to Z ↑	0.0349	0.0296	2.9789	0.7451
D1 to Z ↓	0.0483	0.0407	2.9150	0.8069
D1 to Z ↑	0.0319	0.0265	2.9673	0.7418
D2 to Z ↓	0.0534	0.0430	2.9263	0.8098
D2 to Z ↑	0.0344	0.0279	2.9906	0.7482
D3 to Z ↓	0.0483	0.0386	2.9239	0.8078
D3 to Z ↑	0.0315	0.0249	2.9793	0.7448
S0 to Z ↓	0.0518	0.0428	2.9157	0.8072
S0 to Z ↑	0.0366	0.0306	2.9784	0.7447
S1 to Z ↓	0.0470	0.0384	2.9149	0.8073
S1 to Z ↑	0.0334	0.0272	2.9688	0.7422
S2 to Z ↓	0.0518	0.0408	2.9256	0.8089
S2 to Z ↑	0.0361	0.0290	2.9890	0.7481
S3 to Z ↓	0.0471	0.0364	2.9225	0.8074
S3 to Z ↑	0.0329	0.0256	2.9821	0.7449

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X7_P0	8.904e-07	4.040e-12
X27_P0	3.147e-06	7.570e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X7_P0	X27_P0
D0 (output stable)	5.144e-04	1.595e-03
D1 (output stable)	4.011e-04	1.211e-03
D2 (output stable)	5.043e-04	1.569e-03
D3 (output stable)	3.810e-04	1.159e-03
S0 (output stable)	5.278e-04	1.592e-03
S1 (output stable)	3.982e-04	1.198e-03
S2 (output stable)	4.828e-04	1.477e-03
S3 (output stable)	3.665e-04	1.113e-03
D0 to Z	3.883e-03	1.184e-02
D1 to Z	3.400e-03	1.019e-02
D2 to Z	3.771e-03	1.039e-02
D3 to Z	3.294e-03	8.698e-03
S0 to Z	3.785e-03	1.124e-02
S1 to Z	3.300e-03	9.632e-03
S2 to Z	3.673e-03	9.764e-03
S3 to Z	3.193e-03	8.149e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

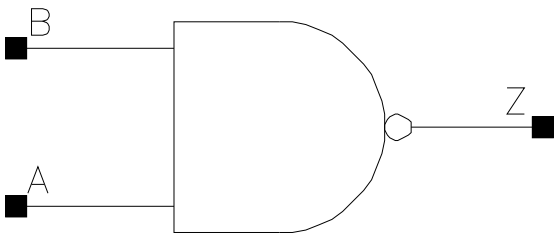
Pin Cycle (vdds)	X7_P0	X27_P0
D0 (output stable)	-2.774e-06	-6.124e-06
D1 (output stable)	2.802e-06	1.550e-05
D2 (output stable)	-6.119e-06	-1.225e-05
D3 (output stable)	9.500e-06	3.144e-05
S0 (output stable)	-6.520e-06	-1.464e-05
S1 (output stable)	9.458e-06	3.155e-05
S2 (output stable)	-3.106e-06	-6.006e-06
S3 (output stable)	5.773e-06	2.445e-05
D0 to Z	-2.767e-06	-3.926e-06
D1 to Z	-1.190e-07	-6.481e-07
D2 to Z	-2.349e-06	-3.536e-06
D3 to Z	7.009e-08	-3.644e-07
S0 to Z	-2.582e-06	-3.630e-06
S1 to Z	-1.078e-07	-2.858e-07
S2 to Z	-2.156e-06	-3.106e-06
S3 to Z	-8.348e-09	1.278e-08

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P0	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P0	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P0	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P0	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P0	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P0	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P0	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P0	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P0	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P0	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P0	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P0	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P0	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P0	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P0	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P0	C12T28SOI_LR_-NAND2X5_P0	C12T28SOI_LR_-NAND2X7_P0	C12T28SOI_LR_-NAND2X10_P0
A	0.0005	0.0007	0.0008	0.0013
B	0.0006	0.0007	0.0008	0.0012
	C12T28SOI_LR_-NAND2X13_P0	C12T28SOI_LR_-NAND2X17_P0	C12T28SOI_LR_-NAND2X20_P0	C12T28SOI_LR_-NAND2X24_P0
A	0.0015	0.0020	0.0023	0.0028
B	0.0015	0.0019	0.0022	0.0026
	C12T28SOI_LR_-NAND2X27_P0	C12T28SOI_LR_-NAND2X42_P0	C12T28SOI_LR_-NAND2X47_P0	C12T28SOI_LR_-NAND2X50_P0
A	0.0031	0.0009	0.0009	0.0009
B	0.0029	0.0010	0.0010	0.0010
	C12T28SOI_LR_-NAND2X58_P0	C12T28SOI_LR_-NAND2X67_P0	C12T28SOI_-LRBR0D8_-NAND2X7_P0	C12T28SOI_-LRBR0D8_-NAND2X14_P0
A	0.0009	0.0009	0.0007	0.0015
B	0.0010	0.0010	0.0008	0.0014
	C12T28SOI_LRS_-NAND2X40_P0	C12T28SOI_LRS_-NAND2X54_P0		
A	0.0046	0.0062		
B	0.0043	0.0059		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P0	**C12T28SOI_LR_-NAND2X5_P0**	**C12T28SOI_LR_-NAND2X3_P0**	**C12T28SOI_LR_-NAND2X5_P0**
A to Z ↓	0.0106	0.0096	5.4948	3.5580
A to Z ↑	0.0161	0.0147	5.8332	3.7648
B to Z ↓	0.0106	0.0093	5.5717	3.6110
B to Z ↑	0.0148	0.0132	5.8702	3.7904
	C12T28SOI_LR_-NAND2X7_P0	**C12T28SOI_LR_-NAND2X10_P0**	**C12T28SOI_LR_-NAND2X7_P0**	**C12T28SOI_LR_-NAND2X10_P0**
A to Z ↓	0.0095	0.0109	2.9997	1.9970
A to Z ↑	0.0143	0.0153	3.0488	1.9920
B to Z ↓	0.0092	0.0092	3.0332	2.0282
B to Z ↑	0.0128	0.0127	3.0770	2.0078
	C12T28SOI_LR_-NAND2X13_P0	**C12T28SOI_LR_-NAND2X17_P0**	**C12T28SOI_LR_-NAND2X13_P0**	**C12T28SOI_LR_-NAND2X17_P0**
A to Z ↓	0.0105	0.0103	1.5448	1.2236

A to Z ↑	0.0146	0.0147	1.5009	1.2070
B to Z ↓	0.0089	0.0092	1.5692	1.2385
B to Z ↑	0.0119	0.0123	1.5135	1.2156
	C12T28SOI_LR_-NAND2X20_P0	**C12T28SOI_LR_-NAND2X24_P0**	**C12T28SOI_LR_-NAND2X20_P0**	**C12T28SOI_LR_-NAND2X24_P0**
A to Z ↓	0.0102	0.0105	1.0594	0.9015
A to Z ↑	0.0143	0.0146	1.0117	0.8613
B to Z ↓	0.0092	0.0090	1.0733	0.9149
B to Z ↑	0.0121	0.0119	1.0199	0.8684
	C12T28SOI_LR_-NAND2X27_P0	**C12T28SOI_LR_-NAND2X42_P0**	**C12T28SOI_LR_-NAND2X27_P0**	**C12T28SOI_LR_-NAND2X42_P0**
A to Z ↓	0.0104	0.0341	0.8061	0.3559
A to Z ↑	0.0143	0.0369	0.7586	0.5943
B to Z ↓	0.0088	0.0347	0.8164	0.3559
B to Z ↑	0.0115	0.0357	0.7652	0.5952
	C12T28SOI_LR_-NAND2X47_P0	**C12T28SOI_LR_-NAND2X50_P0**	**C12T28SOI_LR_-NAND2X47_P0**	**C12T28SOI_LR_-NAND2X50_P0**
A to Z ↓	0.0352	0.0355	0.3154	0.2967
A to Z ↑	0.0376	0.0378	0.5168	0.4964
B to Z ↓	0.0358	0.0361	0.3158	0.2966
B to Z ↑	0.0363	0.0365	0.5166	0.4968
	C12T28SOI_LR_-NAND2X58_P0	**C12T28SOI_LR_-NAND2X67_P0**	**C12T28SOI_LR_-NAND2X58_P0**	**C12T28SOI_LR_-NAND2X67_P0**
A to Z ↓	0.0371	0.0383	0.2577	0.2268
A to Z ↑	0.0390	0.0397	0.4273	0.3755
B to Z ↓	0.0377	0.0389	0.2575	0.2266
B to Z ↑	0.0377	0.0384	0.4273	0.3756
	C12T28SOI_-LRBR0D8_-NAND2X7_P0	**C12T28SOI_-LRBR0D8_-NAND2X14_P0**	**C12T28SOI_-LRBR0D8_-NAND2X7_P0**	**C12T28SOI_-LRBR0D8_-NAND2X14_P0**
A to Z ↓	0.0080	0.0090	2.2672	1.2044
A to Z ↑	0.0170	0.0173	4.0326	1.9734
B to Z ↓	0.0071	0.0066	2.3082	1.2307
B to Z ↑	0.0146	0.0133	4.1755	2.0156
	C12T28SOI_LRS_-NAND2X40_P0	**C12T28SOI_LRS_-NAND2X54_P0**	**C12T28SOI_LRS_-NAND2X40_P0**	**C12T28SOI_LRS_-NAND2X54_P0**
A to Z ↓	0.0103	0.0104	0.5475	0.4148
A to Z ↑	0.0142	0.0142	0.5087	0.3837
B to Z ↓	0.0089	0.0091	0.5543	0.4202
B to Z ↑	0.0115	0.0117	0.5135	0.3876

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P0	1.849e-07	1.518e-12
C12T28SOI_LR_NAND2X5_P0	2.903e-07	1.519e-12
C12T28SOI_LR_NAND2X7_P0	3.401e-07	1.520e-12
C12T28SOI_LR_NAND2X10_P0	4.973e-07	2.023e-12
C12T28SOI_LR_NAND2X13_P0	6.294e-07	2.025e-12
C12T28SOI_LR_NAND2X17_P0	8.039e-07	2.527e-12
C12T28SOI_LR_NAND2X20_P0	8.969e-07	2.528e-12
C12T28SOI_LR_NAND2X24_P0	1.110e-06	3.034e-12
C12T28SOI_LR_NAND2X27_P0	1.166e-06	3.033e-12

C12T28SOI_LR_NAND2X42_P0	2.292e-06	3.284e-12
C12T28SOI_LR_NAND2X47_P0	2.630e-06	3.535e-12
C12T28SOI_LR_NAND2X50_P0	2.555e-06	3.535e-12
C12T28SOI_LR_NAND2X58_P0	2.818e-06	3.788e-12
C12T28SOI_LR_NAND2X67_P0	3.082e-06	4.042e-12
C12T28SOI_LRBR0D8_NAND2X7_P0	3.503e-07	2.774e-12
C12T28SOI_LRBR0D8_NAND2X14_-P0	6.377e-07	3.307e-12
C12T28SOI_LRS_NAND2X40_P0	1.704e-06	4.036e-12
C12T28SOI_LRS_NAND2X54_P0	2.242e-06	5.049e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P0	C12T28SOI_LR_-NAND2X5_P0	C12T28SOI_LR_-NAND2X7_P0	C12T28SOI_LR_-NAND2X10_P0
A (output stable)	1.757e-05	2.693e-05	3.139e-05	8.130e-05
B (output stable)	3.949e-05	6.142e-05	7.428e-05	3.278e-04
A to Z	6.420e-04	8.473e-04	9.996e-04	1.788e-03
B to Z	5.399e-04	6.830e-04	8.037e-04	1.242e-03
	C12T28SOI_LR_-NAND2X13_P0	C12T28SOI_LR_-NAND2X17_P0	C12T28SOI_LR_-NAND2X20_P0	C12T28SOI_LR_-NAND2X24_P0
A (output stable)	9.715e-05	1.258e-04	1.405e-04	1.856e-04
B (output stable)	3.778e-04	4.069e-04	4.450e-04	6.440e-04
A to Z	2.169e-03	2.736e-03	3.098e-03	3.810e-03
B to Z	1.506e-03	1.995e-03	2.267e-03	2.654e-03
	C12T28SOI_LR_-NAND2X27_P0	C12T28SOI_LR_-NAND2X42_P0	C12T28SOI_LR_-NAND2X47_P0	C12T28SOI_LR_-NAND2X50_P0
A (output stable)	2.006e-04	3.431e-05	3.425e-05	3.438e-05
B (output stable)	6.867e-04	8.085e-05	8.087e-05	8.120e-05
A to Z	4.132e-03	1.038e-02	1.121e-02	1.150e-02
B to Z	2.808e-03	1.017e-02	1.100e-02	1.128e-02
	C12T28SOI_LR_-NAND2X58_P0	C12T28SOI_LR_-NAND2X67_P0	C12T28SOI_-LRBR0D8_-NAND2X7_P0	C12T28SOI_-LRBR0D8_-NAND2X14_P0
A (output stable)	3.449e-05	3.445e-05	4.128e-05	1.220e-04
B (output stable)	8.120e-05	8.110e-05	9.855e-05	4.814e-04
A to Z	1.304e-02	1.407e-02	1.035e-03	2.239e-03
B to Z	1.282e-02	1.386e-02	7.556e-04	1.352e-03
	C12T28SOI_LRS_-NAND2X40_P0	C12T28SOI_LRS_-NAND2X54_P0		
A (output stable)	2.904e-04	3.763e-04		
B (output stable)	9.540e-04	1.239e-03		
A to Z	6.100e-03	8.085e-03		
B to Z	4.240e-03	5.645e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P0	C12T28SOI_LR_-NAND2X5_P0	C12T28SOI_LR_-NAND2X7_P0	C12T28SOI_LR_-NAND2X10_P0
A (output stable)	8.880e-08	6.791e-08	5.112e-08	2.907e-07
B (output stable)	6.550e-08	5.815e-08	5.007e-08	-2.250e-06
A to Z	-1.900e-08	2.273e-07	1.978e-07	5.874e-07
B to Z	1.378e-07	1.952e-07	3.080e-08	5.900e-08

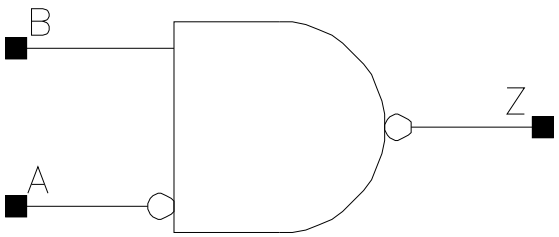
	C12T28SOI_LR_-NAND2X13_P0	C12T28SOI_LR_-NAND2X17_P0	C12T28SOI_LR_-NAND2X20_P0	C12T28SOI_LR_-NAND2X24_P0
A (output stable)	2.728e-07	2.258e-07	-3.030e-08	4.272e-07
B (output stable)	-2.229e-06	-2.092e-06	-3.420e-08	-4.188e-06
A to Z	6.750e-07	1.650e-06	9.880e-07	1.300e-06
B to Z	7.270e-07	6.310e-07	1.079e-06	7.100e-07
	C12T28SOI_LR_-NAND2X27_P0	C12T28SOI_LR_-NAND2X42_P0	C12T28SOI_LR_-NAND2X47_P0	C12T28SOI_LR_-NAND2X50_P0
A (output stable)	3.776e-07	6.173e-08	6.114e-08	6.163e-08
B (output stable)	-3.776e-06	5.382e-08	5.387e-08	5.432e-08
A to Z	1.642e-06	-5.400e-07	-4.000e-09	-5.880e-07
B to Z	1.639e-06	-1.430e-07	-1.250e-07	-1.230e-07
	C12T28SOI_LR_-NAND2X58_P0	C12T28SOI_LR_-NAND2X67_P0	C12T28SOI_-LRBR0D8_-NAND2X7_P0	C12T28SOI_-LRBR0D8_-NAND2X14_P0
A (output stable)	6.161e-08	6.248e-08	7.053e-08	1.066e-06
B (output stable)	5.434e-08	5.495e-08	4.960e-08	-8.823e-06
A to Z	-5.320e-07	-1.108e-06	1.596e-07	4.500e-07
B to Z	-2.850e-07	-2.410e-07	7.692e-07	2.756e-06
	C12T28SOI_LRS_-NAND2X40_P0	C12T28SOI_LRS_-NAND2X54_P0		
A (output stable)	5.048e-07	6.775e-07		
B (output stable)	-4.930e-06	-6.857e-06		
A to Z	2.862e-06	2.810e-07		
B to Z	1.770e-06	2.357e-06		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X7_P0	1.200	0.544	0.6528
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X40_P0	1.200	2.312	2.7744
X54_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P0	X7_P0	X13_P0	X27_P0
A	0.0008	0.0008	0.0010	0.0019
B	0.0006	0.0008	0.0014	0.0029
	X40_P0	X54_P0		
A	0.0027	0.0036		
B	0.0043	0.0058		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0276	0.0292	5.4362	2.9717
A to Z ↑	0.0203	0.0210	5.6468	2.9960
B to Z ↓	0.0109	0.0092	5.6215	3.0574
B to Z ↑	0.0149	0.0127	5.8708	3.1057
	X13_P0	**X27_P0**	**X13_P0**	**X27_P0**

A to Z ↓	0.0273	0.0266	1.6155	0.8045
A to Z ↑	0.0201	0.0196	1.5426	0.7463
B to Z ↓	0.0087	0.0086	1.6628	0.8289
B to Z ↑	0.0118	0.0115	1.5485	0.7666
	X40_P0	**X54_P0**	**X40_P0**	**X54_P0**
A to Z ↓	0.0269	0.0268	0.5374	0.4083
A to Z ↑	0.0200	0.0198	0.4974	0.3759
B to Z ↓	0.0088	0.0088	0.5536	0.4204
B to Z ↑	0.0115	0.0115	0.5156	0.3895

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P0	3.464e-07	1.772e-12
X7_P0	4.945e-07	1.772e-12
X13_P0	1.008e-06	2.529e-12
X27_P0	1.797e-06	3.788e-12
X40_P0	2.591e-06	5.049e-12
X54_P0	3.384e-06	6.309e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	1.002e-03	1.251e-03	2.064e-03	3.995e-03
B (output stable)	4.018e-05	7.467e-05	3.575e-04	6.269e-04
A to Z	1.718e-03	2.344e-03	4.294e-03	8.355e-03
B to Z	5.473e-04	7.943e-04	1.476e-03	2.855e-03
	X40_P0	X54_P0		
A (output stable)	6.096e-03	7.936e-03		
B (output stable)	9.203e-04	1.203e-03		
A to Z	1.258e-02	1.652e-02		
B to Z	4.209e-03	5.579e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

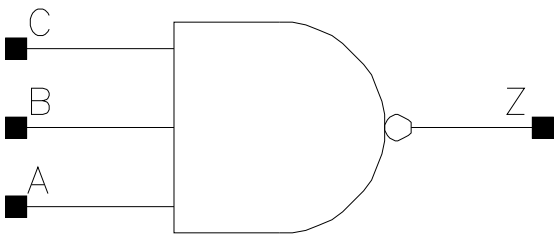
Pin Cycle (vdds)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	2.241e-07	8.190e-08	3.030e-08	1.308e-06
B (output stable)	6.380e-08	3.795e-08	3.410e-08	-2.457e-06
A to Z	2.736e-07	1.374e-07	3.010e-07	1.152e-06
B to Z	1.291e-07	2.761e-07	-3.180e-07	2.950e-07
	X40_P0	X54_P0		
A (output stable)	2.062e-06	3.126e-06		
B (output stable)	-4.032e-06	-6.107e-06		
A to Z	6.900e-08	-9.700e-08		
B to Z	5.180e-07	2.419e-06		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P0	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P0	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P0	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P0	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P0	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P0	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P0	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P0	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P0	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P0	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P0	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P0	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P0	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P0	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P0	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A	0.0006	0.0008	0.0013	0.0015
B	0.0007	0.0008	0.0012	0.0015
C	0.0006	0.0008	0.0012	0.0015
	C12T28SOI_LR_-NAND3X15_P0	C12T28SOI_LR_-NAND3X18_P0	C12T28SOI_LR_-NAND3X21_P0	C12T28SOI_LR_-NAND3X24_P0
A	0.0020	0.0023	0.0028	0.0031
B	0.0019	0.0022	0.0026	0.0030
C	0.0019	0.0021	0.0026	0.0028
	C12T28SOI_LR_-NAND3X35_P0	C12T28SOI_LR_-NAND3X47_P0	C12T28SOI_-LRBR0P6_-NAND3X6_P0	C12T28SOI_-LRBR0P6_-NAND3X12_P0
A	0.0046	0.0062	0.0008	0.0015
B	0.0044	0.0059	0.0008	0.0014
C	0.0043	0.0058	0.0008	0.0014
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	C12T28SOI_-LRBR0P6_-NAND3X24_P0	C12T28SOI_-LRBR0P6_-NAND3X35_P0	C12T28SOI_-LRBR0P6_-NAND3X47_P0
A	0.0023	0.0030	0.0045	0.0061
B	0.0021	0.0029	0.0043	0.0058
C	0.0020	0.0028	0.0041	0.0055
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0			
A	0.0023			
B	0.0023			
C	0.0021			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0
A to Z ↓	0.0161	0.0147	5.8563	4.2066
A to Z ↑	0.0201	0.0184	4.2696	2.9620
B to Z ↓	0.0171	0.0153	5.8890	4.2273
B to Z ↑	0.0193	0.0174	4.2792	2.9698
C to Z ↓	0.0148	0.0133	5.9150	4.2505
C to Z ↑	0.0169	0.0152	4.2786	2.9882

	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A to Z ↓	0.0162	0.0153	2.8650	2.2418
A to Z ↑	0.0192	0.0182	2.0053	1.5180
B to Z ↓	0.0156	0.0148	2.8768	2.2515
B to Z ↑	0.0176	0.0166	2.0104	1.5218
C to Z ↓	0.0134	0.0128	2.8960	2.2670
C to Z ↑	0.0151	0.0142	2.0015	1.5073
	C12T28SOI_LR_-NAND3X15_P0	**C12T28SOI_LR_-NAND3X18_P0**	**C12T28SOI_LR_-NAND3X15_P0**	**C12T28SOI_LR_-NAND3X18_P0**
A to Z ↓	0.0147	0.0145	1.7990	1.5528
A to Z ↑	0.0178	0.0173	1.2061	1.0088
B to Z ↓	0.0148	0.0146	1.8074	1.5623
B to Z ↑	0.0162	0.0158	1.2098	1.0118
C to Z ↓	0.0130	0.0127	1.8185	1.5696
C to Z ↑	0.0142	0.0136	1.2176	1.0192
	C12T28SOI_LR_-NAND3X21_P0	**C12T28SOI_LR_-NAND3X24_P0**	**C12T28SOI_LR_-NAND3X21_P0**	**C12T28SOI_LR_-NAND3X24_P0**
A to Z ↓	0.0152	0.0150	1.3130	1.1766
A to Z ↑	0.0179	0.0176	0.8663	0.7641
B to Z ↓	0.0149	0.0147	1.3212	1.1822
B to Z ↑	0.0163	0.0161	0.8683	0.7657
C to Z ↓	0.0130	0.0128	1.3286	1.1899
C to Z ↑	0.0141	0.0138	0.8693	0.7659
	C12T28SOI_LR_-NAND3X35_P0	**C12T28SOI_LR_-NAND3X47_P0**	**C12T28SOI_LR_-NAND3X35_P0**	**C12T28SOI_LR_-NAND3X47_P0**
A to Z ↓	0.0145	0.0147	0.8053	0.6135
A to Z ↑	0.0171	0.0173	0.5123	0.3876
B to Z ↓	0.0144	0.0146	0.8100	0.6167
B to Z ↑	0.0156	0.0156	0.5125	0.3865
C to Z ↓	0.0125	0.0127	0.8146	0.6209
C to Z ↑	0.0133	0.0133	0.5155	0.3884
	C12T28SOI_-LRBR0P6_-NAND3X6_P0	**C12T28SOI_-LRBR0P6_-NAND3X12_P0**	**C12T28SOI_-LRBR0P6_-NAND3X6_P0**	**C12T28SOI_-LRBR0P6_-NAND3X12_P0**
A to Z ↓	0.0120	0.0125	2.8665	1.5216
A to Z ↑	0.0245	0.0244	4.6257	2.3652
B to Z ↓	0.0120	0.0113	2.8957	1.5379
B to Z ↑	0.0224	0.0212	4.6411	2.3728
C to Z ↓	0.0093	0.0083	2.9304	1.5585
C to Z ↑	0.0181	0.0165	4.6678	2.3799
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	**C12T28SOI_-LRBR0P6_-NAND3X24_P0**	**C12T28SOI_-LRBR0P6_-NAND3X18_P0**	**C12T28SOI_-LRBR0P6_-NAND3X24_P0**
A to Z ↓	0.0118	0.0122	1.0538	0.7974
A to Z ↑	0.0232	0.0236	1.5728	1.1896
B to Z ↓	0.0111	0.0111	1.0660	0.8062
B to Z ↑	0.0201	0.0205	1.5792	1.1922
C to Z ↓	0.0085	0.0083	1.0796	0.8173
C to Z ↑	0.0160	0.0159	1.5914	1.1952
	C12T28SOI_-LRBR0P6_-NAND3X35_P0	**C12T28SOI_-LRBR0P6_-NAND3X47_P0**	**C12T28SOI_-LRBR0P6_-NAND3X35_P0**	**C12T28SOI_-LRBR0P6_-NAND3X47_P0**

A to Z ↓	0.0118	0.0119	0.5460	0.4179
A to Z ↑	0.0235	0.0234	0.8193	0.6206
B to Z ↓	0.0110	0.0110	0.5520	0.4226
B to Z ↑	0.0204	0.0202	0.8207	0.6211
C to Z ↓	0.0083	0.0084	0.5604	0.4287
C to Z ↑	0.0158	0.0157	0.8294	0.6236
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P0**	
A to Z ↓	0.0125		1.0228	
A to Z ↑	0.0235		1.4937	
B to Z ↓	0.0112		1.0326	
B to Z ↑	0.0204		1.4982	
C to Z ↓	0.0081		1.0478	
C to Z ↑	0.0156		1.4866	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P0	2.182e-07	2.024e-12
C12T28SOI_LR_NAND3X6_P0	3.087e-07	2.024e-12
C12T28SOI_LR_NAND3X9_P0	4.348e-07	2.780e-12
C12T28SOI_LR_NAND3X12_P0	5.496e-07	2.780e-12
C12T28SOI_LR_NAND3X15_P0	6.656e-07	3.285e-12
C12T28SOI_LR_NAND3X18_P0	7.495e-07	3.284e-12
C12T28SOI_LR_NAND3X21_P0	9.575e-07	4.292e-12
C12T28SOI_LR_NAND3X24_P0	1.014e-06	4.292e-12
C12T28SOI_LR_NAND3X35_P0	1.475e-06	5.804e-12
C12T28SOI_LR_NAND3X47_P0	1.939e-06	7.317e-12
C12T28SOI_LRBR0P6_NAND3X6_P0	3.184e-07	3.444e-12
C12T28SOI_LRBR0P6_NAND3X12_-P0	5.756e-07	4.260e-12
C12T28SOI_LRBR0P6_NAND3X18_-P0	7.733e-07	4.805e-12
C12T28SOI_LRBR0P6_NAND3X24_-P0	1.073e-06	5.890e-12
C12T28SOI_LRBR0P6_NAND3X35_-P0	1.569e-06	7.519e-12
C12T28SOI_LRBR0P6_NAND3X47_-P0	2.067e-06	9.152e-12
C12T28SOIDV_LRBR0P6_-NAND3X18_P0	9.413e-07	3.963e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A (output stable)	2.000e-05	2.708e-05	5.202e-05	6.213e-05
B (output stable)	7.701e-05	9.650e-05	1.828e-04	2.174e-04
C (output stable)	1.406e-04	1.708e-04	2.576e-04	2.958e-04
A to Z	1.444e-03	1.757e-03	2.895e-03	3.407e-03
B to Z	1.308e-03	1.552e-03	2.360e-03	2.785e-03
C to Z	1.025e-03	1.221e-03	1.800e-03	2.122e-03

	C12T28SOI_LR_-NAND3X15_P0	C12T28SOI_LR_-NAND3X18_P0	C12T28SOI_LR_-NAND3X21_P0	C12T28SOI_LR_-NAND3X24_P0
A (output stable)	7.372e-05	8.212e-05	1.129e-04	1.198e-04
B (output stable)	2.565e-04	2.932e-04	3.749e-04	4.120e-04
C (output stable)	3.354e-04	3.596e-04	4.907e-04	5.091e-04
A to Z	4.105e-03	4.622e-03	5.842e-03	6.371e-03
B to Z	3.371e-03	3.795e-03	4.786e-03	5.207e-03
C to Z	2.628e-03	2.927e-03	3.659e-03	3.963e-03
	C12T28SOI_LR_-NAND3X35_P0	C12T28SOI_LR_-NAND3X47_P0	C12T28SOI_-LRBR0P6_-NAND3X6_P0	C12T28SOI_-LRBR0P6_-NAND3X12_P0
A (output stable)	1.607e-04	2.131e-04	3.862e-05	8.751e-05
B (output stable)	5.901e-04	7.702e-04	1.407e-04	3.183e-04
C (output stable)	7.505e-04	9.629e-04	2.286e-04	4.244e-04
A to Z	9.051e-03	1.204e-02	1.874e-03	3.673e-03
B to Z	7.338e-03	9.745e-03	1.560e-03	2.768e-03
C to Z	5.498e-03	7.350e-03	1.062e-03	1.735e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	C12T28SOI_-LRBR0P6_-NAND3X24_P0	C12T28SOI_-LRBR0P6_-NAND3X35_P0	C12T28SOI_-LRBR0P6_-NAND3X47_P0
A (output stable)	1.199e-04	1.684e-04	2.370e-04	3.104e-04
B (output stable)	4.223e-04	5.963e-04	8.537e-04	1.122e-03
C (output stable)	4.905e-04	7.560e-04	1.114e-03	1.448e-03
A to Z	4.966e-03	6.846e-03	9.909e-03	1.286e-02
B to Z	3.716e-03	5.145e-03	7.431e-03	9.627e-03
C to Z	2.455e-03	3.258e-03	4.636e-03	5.941e-03
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0			
A (output stable)	1.284e-04			
B (output stable)	4.823e-04			
C (output stable)	6.254e-04			
A to Z	5.394e-03			
B to Z	4.050e-03			
C to Z	2.505e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A (output stable)	7.823e-08	3.342e-07	6.807e-07	2.507e-08
B (output stable)	6.386e-08	1.101e-07	3.519e-07	1.116e-08
C (output stable)	6.567e-08	-9.740e-07	-1.750e-06	-8.433e-09
A to Z	-4.650e-07	-8.600e-07	7.510e-07	1.006e-06
B to Z	-5.700e-08	1.000e-07	2.400e-08	-1.200e-08
C to Z	5.620e-07	4.310e-07	-3.730e-07	-3.050e-07
	C12T28SOI_LR_-NAND3X15_P0	C12T28SOI_LR_-NAND3X18_P0	C12T28SOI_LR_-NAND3X21_P0	C12T28SOI_LR_-NAND3X24_P0
A (output stable)	5.802e-07	5.627e-07	1.932e-06	1.090e-06
B (output stable)	1.329e-07	1.015e-07	-7.673e-07	2.636e-07
C (output stable)	-1.596e-06	-1.475e-06	-3.627e-06	-2.845e-06
A to Z	-1.318e-06	-2.450e-07	1.596e-06	1.905e-06
B to Z	3.760e-07	1.690e-07	7.300e-07	-5.600e-08

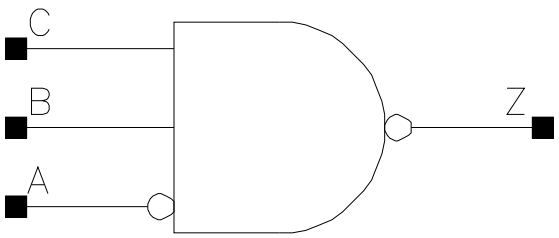
C to Z	4.870e-07	7.880e-07	-5.260e-07	2.493e-06
	C12T28SOI_LR_-NAND3X35_P0	C12T28SOI_LR_-NAND3X47_P0	C12T28SOI_-LRBR0P6_-NAND3X6_P0	C12T28SOI_-LRBR0P6_-NAND3X12_P0
A (output stable)	1.468e-06	2.007e-06	1.271e-06	3.091e-06
B (output stable)	2.922e-07	3.030e-07	2.922e-07	-1.402e-06
C (output stable)	-4.097e-06	-5.453e-06	-3.852e-06	-4.982e-06
A to Z	1.953e-06	3.570e-07	3.350e-07	5.730e-07
B to Z	2.260e-07	4.827e-06	-1.010e-07	6.210e-07
C to Z	2.900e-08	-1.747e-06	8.200e-08	7.540e-07
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	C12T28SOI_-LRBR0P6_-NAND3X24_P0	C12T28SOI_-LRBR0P6_-NAND3X35_P0	C12T28SOI_-LRBR0P6_-NAND3X47_P0
A (output stable)	2.253e-08	3.757e-06	2.247e-06	2.769e-06
B (output stable)	-2.533e-08	-1.768e-06	4.186e-07	3.864e-07
C (output stable)	-1.667e-08	-6.238e-06	-5.952e-06	-7.458e-06
A to Z	2.940e-07	5.130e-07	1.703e-06	4.390e-07
B to Z	5.750e-07	7.550e-07	-6.400e-08	8.630e-07
C to Z	2.120e-07	6.120e-07	-9.230e-07	1.631e-06
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0			
A (output stable)	2.500e-08			
B (output stable)	-5.567e-09			
C (output stable)	-6.353e-08			
A to Z	1.140e-07			
B to Z	3.960e-07			
C to Z	2.464e-06			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.816	0.9792
X12_P0	1.200	1.224	1.4688
X18_P0	1.200	1.496	1.7952
X24_P0	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0007	0.0010	0.0010	0.0018
B	0.0008	0.0015	0.0022	0.0030
C	0.0008	0.0014	0.0021	0.0028

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X12_P0**	**X6_P0**	**X12_P0**
A to Z ↓	0.0324	0.0312	4.2044	2.2591
A to Z ↑	0.0227	0.0218	2.9097	1.4604
B to Z ↓	0.0138	0.0142	4.2538	2.2870
B to Z ↑	0.0159	0.0157	2.9807	1.5021
C to Z ↓	0.0130	0.0120	4.2776	2.3009
C to Z ↑	0.0144	0.0132	2.9963	1.5133
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0357	0.0305	1.5514	1.1773

A to Z ↑	0.0250	0.0208	0.9838	0.7375
B to Z ↓	0.0146	0.0142	1.5680	1.1907
B to Z ↑	0.0158	0.0155	1.0131	0.7618
C to Z ↓	0.0128	0.0121	1.5763	1.1985
C to Z ↑	0.0137	0.0130	1.0210	0.7678

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P0	4.423e-07	2.276e-12
X12_P0	8.710e-07	3.032e-12
X18_P0	1.064e-06	3.537e-12
X24_P0	1.671e-06	5.048e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	1.199e-03	2.088e-03	2.830e-03	3.863e-03
B (output stable)	4.233e-05	1.044e-04	1.694e-04	2.483e-04
C (output stable)	9.662e-05	3.277e-04	3.912e-04	5.913e-04
A to Z	2.844e-03	5.529e-03	7.997e-03	1.059e-02
B to Z	1.298e-03	2.526e-03	3.792e-03	4.875e-03
C to Z	1.088e-03	1.846e-03	2.922e-03	3.555e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

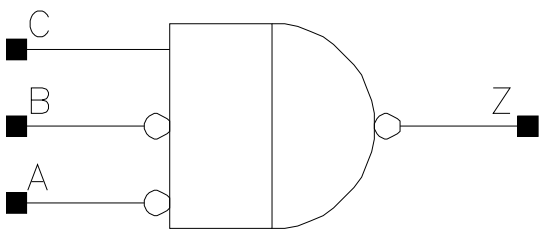
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	3.793e-08	3.600e-07	9.540e-08	9.007e-07
B (output stable)	6.599e-08	2.164e-07	-2.830e-08	-6.603e-07
C (output stable)	3.385e-08	-1.435e-06	-8.383e-08	-2.658e-06
A to Z	2.890e-07	1.930e-07	4.260e-07	2.181e-06
B to Z	4.850e-07	1.030e-07	2.050e-07	1.880e-07
C to Z	4.570e-07	3.990e-07	9.130e-07	1.264e-06

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	0.816	0.9792
X13_P0	1.200	1.088	1.3056
X20_P0	1.200	1.632	1.9584
X27_P0	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P0	X13_P0	X20_P0	X27_P0
A	0.0009	0.0009	0.0018	0.0017
B	0.0010	0.0010	0.0019	0.0018
C	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	**X13_P0**	**X7_P0**	**X13_P0**
A to Z ↓	0.0325	0.0391	2.8574	1.5332
A to Z ↑	0.0194	0.0223	2.8816	1.4510
B to Z ↓	0.0320	0.0391	2.8604	1.5348
B to Z ↑	0.0184	0.0213	2.8817	1.4490
C to Z ↓	0.0091	0.0086	2.9375	1.5703
C to Z ↑	0.0126	0.0117	2.9893	1.5122
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0358	0.0393	1.0484	0.7996
A to Z ↑	0.0207	0.0246	0.9801	0.7359
B to Z ↓	0.0333	0.0376	1.0480	0.8005

B to Z ↑	0.0191	0.0235	0.9792	0.7353
C to Z ↓	0.0096	0.0092	1.0735	0.8175
C to Z ↑	0.0124	0.0121	1.0193	0.7665

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X7_P0	6.500e-07	2.276e-12
X13_P0	8.685e-07	2.781e-12
X20_P0	1.351e-06	3.788e-12
X27_P0	1.504e-06	4.295e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	7.204e-04	9.652e-04	1.640e-03	1.930e-03
B (output stable)	5.792e-04	8.173e-04	1.210e-03	1.536e-03
C (output stable)	7.885e-05	3.250e-04	3.774e-04	4.758e-04
A to Z	3.139e-03	5.161e-03	8.168e-03	1.015e-02
B to Z	2.817e-03	4.847e-03	7.105e-03	9.265e-03
C to Z	8.266e-04	1.471e-03	2.409e-03	3.136e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

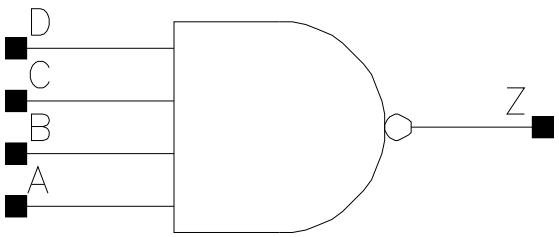
Pin Cycle (vdds)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	-2.284e-06	-2.263e-06	-9.777e-06	-9.662e-06
B (output stable)	1.529e-05	1.533e-05	4.006e-05	3.897e-05
C (output stable)	-2.293e-07	-2.948e-07	-9.845e-07	-1.044e-06
A to Z	-8.990e-08	-3.254e-07	-2.529e-06	-3.374e-06
B to Z	2.781e-07	-7.550e-08	1.287e-06	-1.860e-07
C to Z	4.870e-08	4.810e-07	6.390e-07	1.231e-06

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0006	0.0006	0.0007	0.0009
B	0.0007	0.0007	0.0008	0.0010
C	0.0006	0.0007	0.0008	0.0010
D	0.0007	0.0007	0.0008	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0474	0.0470	1.7244	0.8618
A to Z ↑	0.0383	0.0412	2.9526	1.4634
B to Z ↓	0.0482	0.0485	1.7249	0.8619
B to Z ↑	0.0370	0.0407	2.9488	1.4634
C to Z ↓	0.0476	0.0459	1.7253	0.8615
C to Z ↑	0.0396	0.0429	2.9531	1.4606

D to Z ↓	0.0487	0.0467	1.7249	0.8617
D to Z ↑	0.0388	0.0414	2.9495	1.4612
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0485	0.0451	0.5966	0.4461
A to Z ↑	0.0398	0.0388	0.9882	0.7400
B to Z ↓	0.0495	0.0457	0.5965	0.4456
B to Z ↑	0.0387	0.0376	0.9880	0.7395
C to Z ↓	0.0445	0.0413	0.5965	0.4461
C to Z ↑	0.0405	0.0392	0.9865	0.7395
D to Z ↓	0.0454	0.0422	0.5967	0.4459
D to Z ↑	0.0390	0.0380	0.9877	0.7396

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	8.339e-07	3.032e-12
X17_P0	1.259e-06	3.537e-12
X25_P0	1.773e-06	4.292e-12
X33_P0	2.267e-06	4.545e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	5.066e-04	6.355e-04	9.181e-04	1.083e-03
B (output stable)	4.748e-04	6.095e-04	8.702e-04	1.022e-03
C (output stable)	5.132e-04	6.215e-04	9.293e-04	1.062e-03
D (output stable)	4.768e-04	5.791e-04	8.362e-04	9.556e-04
A to Z	3.738e-03	5.588e-03	8.576e-03	1.041e-02
B to Z	3.625e-03	5.488e-03	8.414e-03	1.020e-02
C to Z	3.836e-03	5.497e-03	8.009e-03	9.662e-03
D to Z	3.735e-03	5.379e-03	7.836e-03	9.452e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

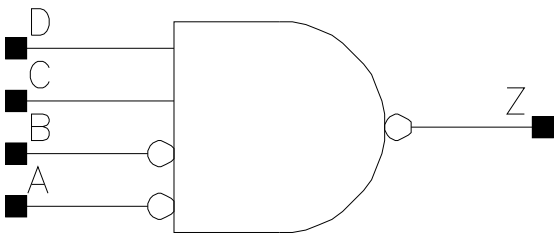
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	-1.032e-06	-1.466e-06	-8.587e-06	-8.150e-06
B (output stable)	-9.295e-07	-1.380e-06	-7.866e-06	-8.161e-06
C (output stable)	6.062e-06	1.216e-05	2.970e-05	3.678e-05
D (output stable)	3.957e-06	9.232e-06	1.485e-05	2.046e-05
A to Z	-2.488e-07	-1.030e-07	-2.411e-06	-2.368e-06
B to Z	7.110e-08	-1.195e-07	-2.192e-06	-2.815e-06
C to Z	-2.214e-07	-4.553e-07	-3.640e-07	-1.315e-06
D to Z	1.090e-08	-1.027e-07	-2.150e-07	-1.172e-06

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X12_P0	1.200	1.496	1.7952
X18_P0	1.200	2.040	2.4480
X24_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0009	0.0010	0.0018	0.0017
B	0.0009	0.0014	0.0019	0.0018
C	0.0008	0.0015	0.0022	0.0030
D	0.0007	0.0015	0.0021	0.0029

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X12_P0	X6_P0	X12_P0
A to Z ↓	0.0341	0.0450	4.3405	2.2666
A to Z ↑	0.0205	0.0248	2.8836	1.4537
B to Z ↓	0.0330	0.0442	4.3345	2.2653
B to Z ↑	0.0188	0.0236	2.8810	1.4521
C to Z ↓	0.0138	0.0142	4.3845	2.2860
C to Z ↑	0.0161	0.0157	3.1668	1.5016

D to Z ↓	0.0128	0.0119	4.4070	2.2993
D to Z ↑	0.0144	0.0131	3.1845	1.5125
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0391	0.0438	1.5475	1.1787
A to Z ↑	0.0219	0.0277	0.9806	0.7366
B to Z ↓	0.0367	0.0420	1.5477	1.1788
B to Z ↑	0.0204	0.0264	0.9797	0.7354
C to Z ↓	0.0141	0.0146	1.5637	1.1894
C to Z ↑	0.0154	0.0159	1.0179	0.7595
D to Z ↓	0.0124	0.0128	1.5723	1.1950
D to Z ↑	0.0134	0.0135	1.0406	0.7660

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P0	5.358e-07	2.528e-12
X12_P0	7.685e-07	3.535e-12
X18_P0	1.205e-06	4.544e-12
X24_P0	1.289e-06	5.300e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	8.028e-04	1.338e-03	2.027e-03	2.451e-03
B (output stable)	6.372e-04	1.102e-03	1.543e-03	1.998e-03
C (output stable)	7.050e-05	1.686e-04	2.533e-04	3.362e-04
D (output stable)	1.034e-04	3.493e-04	4.034e-04	5.857e-04
A to Z	3.363e-03	6.358e-03	9.340e-03	1.242e-02
B to Z	3.044e-03	5.904e-03	8.341e-03	1.150e-02
C to Z	1.261e-03	2.522e-03	3.609e-03	5.133e-03
D to Z	1.048e-03	1.828e-03	2.793e-03	3.870e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

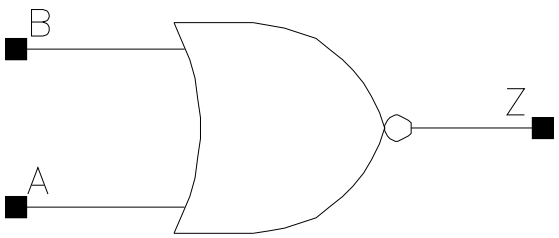
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	-2.043e-06	-6.065e-06	-8.743e-06	-8.863e-06
B (output stable)	1.381e-05	2.110e-05	3.736e-05	3.648e-05
C (output stable)	-6.083e-09	3.738e-07	5.170e-08	8.825e-07
D (output stable)	-1.407e-07	-2.170e-06	-2.200e-06	-4.348e-06
A to Z	1.279e-07	-2.105e-06	-2.459e-06	-2.685e-06
B to Z	1.392e-06	1.040e-07	1.460e-06	2.170e-07
C to Z	-1.360e-07	8.500e-08	1.735e-06	1.730e-07
D to Z	7.000e-07	4.620e-07	8.010e-07	1.163e-06

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.408	0.4896
X5_P0	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X10_P0	1.200	0.680	0.8160
X14_P0	1.200	0.680	0.8160
X17_P0	1.200	0.952	1.1424
X21_P0	1.200	0.952	1.1424
X24_P0	1.200	1.224	1.4688
X27_P0	1.200	1.224	1.4688
X34_P0	1.200	1.496	1.7952
X40_P0	1.200	1.360	1.6320
X41_P0	1.200	1.768	2.1216
X49_P0	1.200	1.496	1.7952
X53_P0	1.200	1.904	2.2848
X55_P0	1.200	2.312	2.7744
X57_P0	1.200	1.904	2.2848
X65_P0	1.200	2.040	2.4480
X84_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P0	X5_P0	X7_P0	X10_P0
A	0.0005	0.0006	0.0008	0.0013
B	0.0005	0.0006	0.0008	0.0012
	X14_P0	X17_P0	X21_P0	X24_P0

A	0.0016	0.0021	0.0024	0.0028
B	0.0015	0.0019	0.0022	0.0027
	X27_P0	X34_P0	X40_P0	X41_P0
A	0.0031	0.0039	0.0009	0.0048
B	0.0029	0.0036	0.0010	0.0045
	X49_P0	X53_P0	X55_P0	X57_P0
A	0.0009	0.0010	0.0063	0.0010
B	0.0010	0.0009	0.0059	0.0009
	X65_P0	X84_P0		
A	0.0010	0.0010		
B	0.0009	0.0010		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X5_P0**	**X3_P0**	**X5_P0**
A to Z ↓	0.0092	0.0086	3.3017	2.4070
A to Z ↑	0.0194	0.0182	12.0535	8.8377
B to Z ↓	0.0082	0.0074	3.3866	2.4287
B to Z ↑	0.0185	0.0168	12.1184	8.8835
	X7_P0	**X10_P0**	**X7_P0**	**X10_P0**
A to Z ↓	0.0083	0.0087	1.7760	1.1502
A to Z ↑	0.0173	0.0193	6.2890	4.1839
B to Z ↓	0.0070	0.0065	1.8024	1.1642
B to Z ↑	0.0157	0.0147	6.3255	4.2084
	X14_P0	**X17_P0**	**X14_P0**	**X17_P0**
A to Z ↓	0.0085	0.0086	0.8796	0.7042
A to Z ↑	0.0183	0.0183	3.1232	2.5114
B to Z ↓	0.0063	0.0068	0.8911	0.7122
B to Z ↑	0.0139	0.0149	3.1433	2.5272
	X21_P0	**X24_P0**	**X21_P0**	**X24_P0**
A to Z ↓	0.0086	0.0085	0.6031	0.5131
A to Z ↑	0.0178	0.0180	2.1022	1.8262
B to Z ↓	0.0068	0.0065	0.6095	0.5196
B to Z ↑	0.0145	0.0143	2.1153	1.8395
	X27_P0	**X34_P0**	**X27_P0**	**X34_P0**
A to Z ↓	0.0084	0.0088	0.4569	0.3693
A to Z ↑	0.0175	0.0179	1.6149	1.2860
B to Z ↓	0.0063	0.0068	0.4631	0.3736
B to Z ↑	0.0137	0.0145	1.6260	1.2942
	X40_P0	**X41_P0**	**X40_P0**	**X41_P0**
A to Z ↓	0.0305	0.0086	0.3626	0.3076
A to Z ↑	0.0462	0.0177	0.6066	1.0649
B to Z ↓	0.0293	0.0065	0.3621	0.3117
B to Z ↑	0.0462	0.0138	0.6074	1.0721
	X49_P0	**X53_P0**	**X49_P0**	**X53_P0**
A to Z ↓	0.0316	0.0326	0.3014	0.2760
A to Z ↑	0.0472	0.0536	0.5042	0.4665
B to Z ↓	0.0305	0.0315	0.3016	0.2759
B to Z ↑	0.0472	0.0533	0.5050	0.4658
	X55_P0	**X57_P0**	**X55_P0**	**X57_P0**
A to Z ↓	0.0087	0.0331	0.2329	0.2599
A to Z ↑	0.0176	0.0541	0.8028	0.4341

B to Z ↓	0.0066	0.0320	0.2364	0.2599
B to Z ↑	0.0139	0.0537	0.8079	0.4342
	X65_P0	**X84_P0**	**X65_P0**	**X84_P0**
A to Z ↓	0.0337	0.0354	0.2277	0.1817
A to Z ↑	0.0545	0.0551	0.3795	0.3020
B to Z ↓	0.0327	0.0343	0.2278	0.1816
B to Z ↑	0.0541	0.0549	0.3792	0.3019

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P0	1.923e-07	1.520e-12
X5_P0	2.614e-07	1.520e-12
X7_P0	3.482e-07	1.520e-12
X10_P0	5.105e-07	2.024e-12
X14_P0	6.421e-07	2.024e-12
X17_P0	8.242e-07	2.528e-12
X21_P0	9.142e-07	2.528e-12
X24_P0	1.133e-06	3.033e-12
X27_P0	1.188e-06	3.033e-12
X34_P0	1.461e-06	3.537e-12
X40_P0	2.269e-06	3.284e-12
X41_P0	1.735e-06	4.041e-12
X49_P0	2.536e-06	3.535e-12
X53_P0	3.071e-06	4.291e-12
X55_P0	2.283e-06	5.049e-12
X57_P0	3.219e-06	4.290e-12
X65_P0	3.487e-06	4.544e-12
X84_P0	3.789e-06	5.053e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	3.427e-05	4.589e-05	6.300e-05	1.674e-04
B (output stable)	8.322e-06	1.045e-05	1.468e-05	7.658e-05
A to Z	6.726e-04	8.173e-04	1.074e-03	1.884e-03
B to Z	5.100e-04	5.978e-04	7.595e-04	1.074e-03
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	2.008e-04	2.448e-04	2.788e-04	3.363e-04
B (output stable)	8.746e-05	1.052e-04	1.046e-04	1.247e-04
A to Z	2.318e-03	2.922e-03	3.341e-03	3.964e-03
B to Z	1.332e-03	1.842e-03	2.099e-03	2.396e-03
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	3.662e-04	4.530e-04	6.408e-05	5.763e-04
B (output stable)	1.286e-04	1.429e-04	1.454e-05	2.178e-04
A to Z	4.254e-03	5.522e-03	1.022e-02	6.560e-03
B to Z	2.536e-03	3.471e-03	9.912e-03	3.853e-03
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	6.377e-05	6.576e-05	7.448e-04	6.576e-05
B (output stable)	1.438e-05	1.531e-05	2.571e-04	1.531e-05
A to Z	1.135e-02	1.405e-02	8.538e-03	1.464e-02
B to Z	1.104e-02	1.372e-02	5.095e-03	1.430e-02
	X65_P0	X84_P0		

A (output stable)	6.589e-05	6.800e-05		
B (output stable)	1.542e-05	1.582e-05		
A to Z	1.557e-02	1.844e-02		
B to Z	1.524e-02	1.805e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

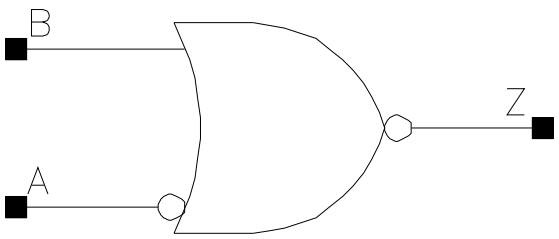
Pin Cycle (vdds)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	-1.984e-06	-2.467e-06	-3.212e-06	-1.197e-05
B (output stable)	1.513e-05	2.017e-05	2.721e-05	9.051e-05
A to Z	-1.277e-07	1.703e-07	5.360e-07	-1.163e-06
B to Z	-1.930e-08	5.985e-07	1.393e-06	1.182e-06
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	-1.415e-05	-1.140e-05	-1.260e-05	-2.079e-05
B (output stable)	1.124e-04	8.885e-05	9.800e-05	1.563e-04
A to Z	-2.117e-06	3.080e-07	-1.664e-06	5.800e-07
B to Z	1.997e-06	3.555e-06	4.407e-06	3.748e-06
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	-2.032e-05	-2.089e-05	-3.301e-06	-3.203e-05
B (output stable)	1.523e-04	1.576e-04	2.711e-05	2.450e-04
A to Z	-2.381e-06	-2.278e-06	-4.900e-07	-4.056e-06
B to Z	2.608e-06	6.182e-06	-2.390e-07	4.479e-06
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	-3.239e-06	-3.254e-06	-3.692e-05	-3.254e-06
B (output stable)	2.700e-05	2.877e-05	2.776e-04	2.877e-05
A to Z	-5.770e-07	-5.710e-07	-4.351e-06	-5.580e-07
B to Z	-2.630e-07	-2.490e-07	5.751e-06	-1.840e-07
	X65_P0	X84_P0		
A (output stable)	-3.254e-06	-3.418e-06		
B (output stable)	2.879e-05	2.953e-05		
A to Z	-7.280e-07	-1.012e-06		
B to Z	-2.820e-07	-8.210e-07		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X7_P0	1.200	0.680	0.8160
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X41_P0	1.200	2.312	2.7744
X55_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X7_P0	X13_P0
A	0.0007	0.0007	0.0007	0.0010
B	0.0006	0.0008	0.0008	0.0014
	X27_P0	X41_P0	X55_P0	
A	0.0019	0.0028	0.0036	
B	0.0030	0.0044	0.0058	

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X6_P0**	**X3_P0**	**X6_P0**
A to Z ↓	0.0259	0.0282	3.1213	2.0658
A to Z ↑	0.0238	0.0239	11.9311	6.2518
B to Z ↓	0.0084	0.0081	3.3546	2.2271
B to Z ↑	0.0187	0.0156	12.0932	6.3447

	X7_P0	X13_P0	X7_P0	X13_P0
A to Z ↓	0.0285	0.0260	1.6521	0.9009
A to Z ↑	0.0259	0.0246	6.2001	3.2866
B to Z ↓	0.0072	0.0066	1.7235	0.9389
B to Z ↑	0.0166	0.0150	6.2649	3.3319
	X27_P0	**X41_P0**	**X27_P0**	**X41_P0**
A to Z ↓	0.0252	0.0256	0.4315	0.2927
A to Z ↑	0.0235	0.0238	1.5770	1.0589
B to Z ↓	0.0065	0.0066	0.4657	0.3141
B to Z ↑	0.0144	0.0142	1.5987	1.0734
	X55_P0		**X55_P0**	
A to Z ↓	0.0253		0.2218	
A to Z ↑	0.0236		0.7986	
B to Z ↓	0.0066		0.2383	
B to Z ↑	0.0142		0.8102	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P0	3.517e-07	1.771e-12
X6_P0	4.860e-07	1.772e-12
X7_P0	5.706e-07	2.024e-12
X13_P0	9.997e-07	2.529e-12
X27_P0	1.818e-06	3.789e-12
X41_P0	2.621e-06	5.048e-12
X55_P0	3.424e-06	6.307e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	9.942e-04	1.233e-03	1.314e-03	2.103e-03
B (output stable)	1.256e-05	3.060e-05	3.915e-05	8.237e-05
A to Z	1.720e-03	2.348e-03	2.722e-03	4.564e-03
B to Z	5.216e-04	7.458e-04	8.869e-04	1.451e-03
	X27_P0	X41_P0	X55_P0	
A (output stable)	4.090e-03	6.195e-03	8.126e-03	
B (output stable)	1.580e-04	2.310e-04	3.129e-04	
A to Z	8.959e-03	1.333e-02	1.755e-02	
B to Z	2.796e-03	4.080e-03	5.373e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

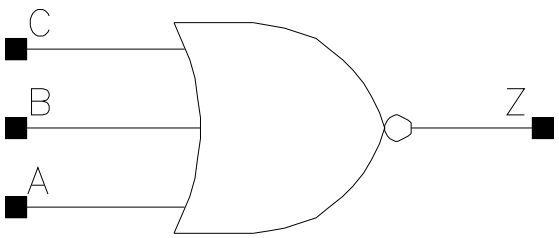
Pin Cycle (vdds)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	-1.896e-06	-2.512e-06	-6.578e-06	-1.121e-05
B (output stable)	6.838e-06	1.688e-05	2.374e-05	3.939e-05
A to Z	-2.142e-07	1.717e-07	-7.630e-07	-1.405e-06
B to Z	2.300e-08	1.666e-07	1.240e-06	1.813e-06
	X27_P0	X41_P0	X55_P0	
A (output stable)	-1.881e-05	-2.902e-05	-3.149e-05	
B (output stable)	6.348e-05	9.012e-05	1.106e-04	
A to Z	1.524e-06	-4.122e-06	-4.481e-06	
B to Z	4.164e-06	6.611e-06	8.273e-06	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X9_P0	1.200	0.952	1.1424
X13_P0	1.200	0.952	1.1424
X16_P0	1.200	1.360	1.6320
X19_P0	1.200	1.496	1.7952
X22_P0	1.200	1.768	2.1216
X25_P0	1.200	1.904	2.2848
X37_P0	1.200	2.584	3.1008
X49_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P0	X6_P0	X9_P0	X13_P0
A	0.0006	0.0008	0.0012	0.0015
B	0.0006	0.0008	0.0014	0.0016
C	0.0007	0.0008	0.0012	0.0014
	X16_P0	X19_P0	X22_P0	X25_P0
A	0.0021	0.0023	0.0028	0.0031
B	0.0021	0.0028	0.0030	0.0037
C	0.0019	0.0021	0.0026	0.0029
	X37_P0	X49_P0		
A	0.0046	0.0063		
B	0.0048	0.0064		

C	0.0042	0.0059		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0105	0.0101	2.4403	1.8026
A to Z ↑	0.0271	0.0252	13.4991	9.6211
B to Z ↓	0.0099	0.0094	2.4479	1.8079
B to Z ↑	0.0256	0.0235	13.5123	9.6333
C to Z ↓	0.0088	0.0081	2.4646	1.8279
C to Z ↑	0.0229	0.0205	13.5550	9.6605
	X9_P0	**X13_P0**	**X9_P0**	**X13_P0**
A to Z ↓	0.0104	0.0101	1.1883	0.9195
A to Z ↑	0.0272	0.0257	6.3502	4.7724
B to Z ↓	0.0097	0.0091	1.1556	0.8779
B to Z ↑	0.0267	0.0245	6.3611	4.7819
C to Z ↓	0.0075	0.0071	1.1676	0.8966
C to Z ↑	0.0189	0.0175	6.3790	4.7932
	X16_P0	**X19_P0**	**X16_P0**	**X19_P0**
A to Z ↓	0.0103	0.0101	0.7091	0.6026
A to Z ↑	0.0263	0.0261	3.8388	3.1950
B to Z ↓	0.0098	0.0096	0.7115	0.5891
B to Z ↑	0.0253	0.0257	3.8418	3.1960
C to Z ↓	0.0078	0.0077	0.7166	0.6157
C to Z ↑	0.0197	0.0187	3.8539	3.2077
	X22_P0	**X25_P0**	**X22_P0**	**X25_P0**
A to Z ↓	0.0102	0.0101	0.5240	0.4603
A to Z ↑	0.0260	0.0260	2.7443	2.4022
B to Z ↓	0.0096	0.0094	0.5142	0.4416
B to Z ↑	0.0251	0.0255	2.7485	2.4066
C to Z ↓	0.0074	0.0073	0.5207	0.4611
C to Z ↑	0.0184	0.0177	2.7564	2.4131
	X37_P0	**X49_P0**	**X37_P0**	**X49_P0**
A to Z ↓	0.0102	0.0102	0.3169	0.2401
A to Z ↑	0.0254	0.0254	1.6100	1.2126
B to Z ↓	0.0095	0.0095	0.3132	0.2376
B to Z ↑	0.0242	0.0241	1.6118	1.2142
C to Z ↓	0.0077	0.0077	0.3176	0.2410
C to Z ↑	0.0178	0.0180	1.6170	1.2180

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	2.107e-07	1.772e-12
X6_P0	2.848e-07	1.774e-12
X9_P0	4.224e-07	2.529e-12
X13_P0	5.422e-07	2.529e-12
X16_P0	6.834e-07	3.286e-12
X19_P0	8.202e-07	3.537e-12
X22_P0	9.483e-07	4.042e-12
X25_P0	1.068e-06	4.294e-12
X37_P0	1.541e-06	5.556e-12

X49_P0	2.040e-06	7.068e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	1.248e-04	1.690e-04	3.708e-04	4.643e-04
B (output stable)	1.490e-05	1.659e-05	1.532e-04	1.582e-04
C (output stable)	6.968e-06	9.865e-06	3.730e-05	4.266e-05
A to Z	1.231e-03	1.561e-03	2.604e-03	3.181e-03
B to Z	1.001e-03	1.244e-03	2.186e-03	2.587e-03
C to Z	7.762e-04	9.215e-04	1.312e-03	1.536e-03
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	5.287e-04	6.632e-04	7.835e-04	9.293e-04
B (output stable)	1.590e-04	2.161e-04	2.687e-04	3.270e-04
C (output stable)	4.675e-05	5.655e-05	6.954e-05	7.793e-05
A to Z	4.140e-03	4.898e-03	5.668e-03	6.456e-03
B to Z	3.401e-03	4.088e-03	4.670e-03	5.373e-03
C to Z	2.283e-03	2.545e-03	2.913e-03	3.133e-03
	X37_P0	X49_P0		
A (output stable)	1.292e-03	1.710e-03		
B (output stable)	3.788e-04	4.898e-04		
C (output stable)	1.141e-04	1.489e-04		
A to Z	9.344e-03	1.243e-02		
B to Z	7.551e-03	1.002e-02		
C to Z	4.638e-03	6.182e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

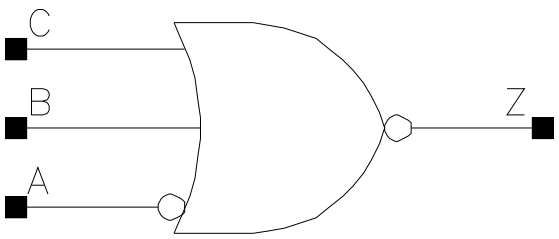
Pin Cycle (vdds)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	-1.964e-05	-2.607e-05	-6.230e-05	-7.736e-05
B (output stable)	1.134e-05	1.693e-05	1.256e-05	1.973e-05
C (output stable)	1.625e-05	2.316e-05	6.480e-05	8.149e-05
A to Z	-1.341e-06	-1.237e-06	-5.579e-06	-6.113e-06
B to Z	-2.886e-07	-1.250e-07	-2.855e-06	-2.327e-06
C to Z	-5.280e-08	-4.150e-08	6.225e-07	1.655e-06
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	-7.456e-05	-9.802e-05	-1.192e-04	-1.449e-04
B (output stable)	3.743e-05	5.276e-05	4.700e-05	6.597e-05
C (output stable)	6.760e-05	9.135e-05	1.162e-04	1.392e-04
A to Z	-5.301e-06	-6.951e-06	-8.016e-06	-1.132e-05
B to Z	-1.868e-06	-2.464e-06	-3.423e-06	-5.327e-06
C to Z	1.484e-06	-1.920e-07	2.691e-06	4.587e-06
	X37_P0	X49_P0		
A (output stable)	-1.944e-04	-2.535e-04		
B (output stable)	8.923e-05	1.171e-04		
C (output stable)	1.804e-04	2.341e-04		
A to Z	-1.409e-05	-1.599e-05		
B to Z	-4.566e-06	-5.908e-06		
C to Z	3.585e-06	5.321e-06		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.680	0.8160
X13_P0	1.200	1.224	1.4688
X19_P0	1.200	1.496	1.7952
X25_P0	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0008	0.0010	0.0010	0.0019
B	0.0008	0.0016	0.0024	0.0032
C	0.0008	0.0015	0.0021	0.0029

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X13_P0**	**X6_P0**	**X13_P0**
A to Z ↓	0.0285	0.0274	1.7184	0.9656
A to Z ↑	0.0319	0.0315	9.7099	4.7665
B to Z ↓	0.0096	0.0093	1.8157	0.8830
B to Z ↑	0.0239	0.0248	9.7498	4.7783
C to Z ↓	0.0083	0.0072	1.8285	0.8969
C to Z ↑	0.0208	0.0177	9.7770	4.7928
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0310	0.0273	0.5848	0.4444

A to Z ↑	0.0340	0.0314	3.2049	2.4048
B to Z ↓	0.0097	0.0094	0.6155	0.4593
B to Z ↑	0.0242	0.0242	3.2156	2.4138
C to Z ↓	0.0077	0.0073	0.6165	0.4639
C to Z ↑	0.0188	0.0178	3.2264	2.4208

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P0	4.509e-07	2.026e-12
X13_P0	9.129e-07	3.032e-12
X19_P0	1.102e-06	3.533e-12
X25_P0	1.693e-06	4.794e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	1.382e-03	2.581e-03	3.402e-03	5.019e-03
B (output stable)	2.633e-05	1.023e-04	1.260e-04	1.864e-04
C (output stable)	1.354e-05	5.640e-05	5.763e-05	8.991e-05
A to Z	2.900e-03	5.721e-03	7.896e-03	1.102e-02
B to Z	1.257e-03	2.633e-03	3.808e-03	5.064e-03
C to Z	9.394e-04	1.571e-03	2.532e-03	3.134e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

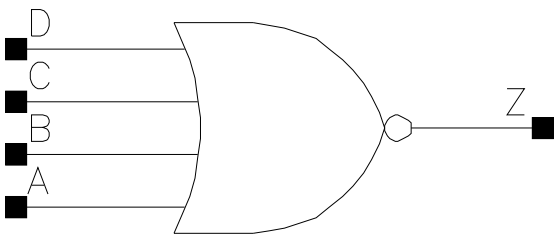
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	-2.882e-05	-7.689e-05	-9.832e-05	-1.440e-04
B (output stable)	1.842e-05	4.101e-05	6.532e-05	8.704e-05
C (output stable)	2.466e-05	6.452e-05	7.225e-05	1.081e-04
A to Z	-3.940e-07	-2.793e-06	-4.443e-06	-8.696e-06
B to Z	-2.330e-07	-2.814e-06	-1.693e-06	-3.587e-06
C to Z	2.254e-07	1.562e-06	2.239e-06	3.191e-06

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	1.904	2.2848
X32_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X32_P0
A	0.0006	0.0007	0.0007	0.0009
B	0.0007	0.0007	0.0008	0.0011
C	0.0006	0.0006	0.0008	0.0009
D	0.0006	0.0006	0.0008	0.0009

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0317	0.0313	1.6794	0.8283
A to Z ↑	0.0504	0.0537	2.9873	1.4821
B to Z ↓	0.0305	0.0305	1.6801	0.8278
B to Z ↑	0.0499	0.0536	2.9891	1.4811
C to Z ↓	0.0313	0.0315	1.6797	0.8274
C to Z ↑	0.0511	0.0553	2.9936	1.4798

D to Z ↓	0.0308	0.0310	1.6757	0.8269
D to Z ↑	0.0511	0.0556	2.9945	1.4804
	X25_P0	**X32_P0**	**X25_P0**	**X32_P0**
A to Z ↓	0.0322	0.0341	0.5793	0.4545
A to Z ↑	0.0532	0.0518	1.0139	0.7676
B to Z ↓	0.0313	0.0331	0.5784	0.4545
B to Z ↑	0.0532	0.0514	1.0149	0.7676
C to Z ↓	0.0310	0.0333	0.5776	0.4531
C to Z ↑	0.0525	0.0519	1.0157	0.7675
D to Z ↓	0.0300	0.0317	0.5777	0.4533
D to Z ↑	0.0524	0.0515	1.0153	0.7669

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	7.265e-07	3.032e-12
X17_P0	1.080e-06	3.284e-12
X25_P0	1.615e-06	4.293e-12
X32_P0	2.042e-06	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	5.208e-04	6.268e-04	8.679e-04	1.106e-03
B (output stable)	4.310e-04	5.409e-04	7.481e-04	9.397e-04
C (output stable)	5.028e-04	6.002e-04	9.304e-04	1.186e-03
D (output stable)	4.110e-04	5.107e-04	8.012e-04	1.016e-03
A to Z	3.557e-03	5.306e-03	8.122e-03	1.018e-02
B to Z	3.379e-03	5.147e-03	7.877e-03	9.870e-03
C to Z	3.617e-03	5.318e-03	7.642e-03	9.597e-03
D to Z	3.434e-03	5.154e-03	7.412e-03	9.283e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

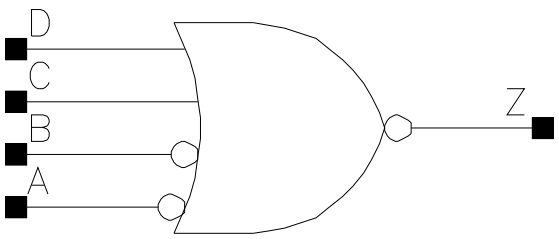
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	-1.242e-06	-1.236e-06	-1.557e-06	-1.961e-06
B (output stable)	5.779e-06	5.549e-06	9.165e-06	1.318e-05
C (output stable)	-2.640e-06	-2.605e-06	-3.056e-06	-3.562e-06
D (output stable)	7.316e-06	6.933e-06	1.091e-05	1.464e-05
A to Z	-2.590e-07	-4.379e-07	-4.330e-07	-4.312e-07
B to Z	-2.030e-08	-1.180e-08	-2.200e-09	-1.358e-07
C to Z	-3.227e-07	-2.761e-07	-8.300e-08	-2.740e-07
D to Z	-2.900e-09	1.381e-07	2.448e-07	-1.092e-07

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X13_P0	1.200	1.496	1.7952
X19_P0	1.200	2.040	2.4480
X25_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0010	0.0010	0.0018	0.0018
B	0.0010	0.0014	0.0019	0.0019
C	0.0008	0.0016	0.0023	0.0030
D	0.0008	0.0014	0.0022	0.0029

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X13_P0	X6_P0	X13_P0
A to Z ↓	0.0250	0.0308	1.6752	0.8400
A to Z ↑	0.0324	0.0393	9.3616	4.8367
B to Z ↓	0.0235	0.0297	1.6745	0.8395
B to Z ↑	0.0324	0.0401	9.3650	4.8398
C to Z ↓	0.0100	0.0094	1.8485	0.8835
C to Z ↑	0.0241	0.0250	9.4079	4.8552

D to Z ↓	0.0084	0.0074	1.8498	0.8940
D to Z ↑	0.0206	0.0183	9.4307	4.8666
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0271	0.0296	0.5774	0.4354
A to Z ↑	0.0356	0.0383	3.2088	2.4249
B to Z ↓	0.0251	0.0280	0.5765	0.4350
B to Z ↑	0.0353	0.0386	3.2092	2.4255
C to Z ↓	0.0097	0.0096	0.6163	0.4618
C to Z ↑	0.0240	0.0241	3.2216	2.4330
D to Z ↓	0.0077	0.0074	0.6171	0.4638
D to Z ↑	0.0188	0.0177	3.2292	2.4389

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P0	5.350e-07	2.530e-12
X13_P0	7.593e-07	3.536e-12
X19_P0	1.201e-06	4.545e-12
X25_P0	1.377e-06	5.299e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	8.296e-04	1.496e-03	2.226e-03	2.746e-03
B (output stable)	7.641e-04	1.409e-03	2.032e-03	2.575e-03
C (output stable)	2.127e-05	7.800e-05	1.195e-04	1.654e-04
D (output stable)	2.280e-05	8.816e-05	1.095e-04	1.755e-04
A to Z	3.460e-03	6.545e-03	9.695e-03	1.245e-02
B to Z	3.256e-03	6.222e-03	8.988e-03	1.184e-02
C to Z	1.312e-03	2.646e-03	3.774e-03	4.990e-03
D to Z	9.761e-04	1.642e-03	2.532e-03	3.076e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

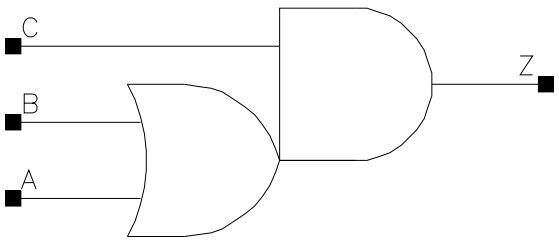
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	-1.419e-05	-4.276e-05	-5.400e-05	-7.538e-05
B (output stable)	-1.321e-05	-4.088e-05	-5.035e-05	-6.943e-05
C (output stable)	2.146e-05	3.759e-05	6.058e-05	7.712e-05
D (output stable)	3.651e-05	8.840e-05	1.059e-04	1.485e-04
A to Z	-1.004e-06	-6.448e-06	-6.972e-06	-1.176e-05
B to Z	-7.290e-07	-6.772e-06	-6.610e-06	-1.103e-05
C to Z	-1.860e-07	-2.582e-06	-1.887e-06	-4.279e-06
D to Z	-9.310e-08	1.369e-06	2.349e-06	3.253e-06

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0009	0.0009	0.0017
B	0.0010	0.0010	0.0019
C	0.0010	0.0010	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0294	0.0338	1.7391	0.8717
A to Z ↑	0.0225	0.0249	3.0129	1.4857
B to Z ↓	0.0287	0.0335	1.7405	0.8718
B to Z ↑	0.0206	0.0232	3.0153	1.4828
C to Z ↓	0.0251	0.0277	1.7185	0.8553
C to Z ↑	0.0218	0.0238	3.0117	1.4834
	X33_P0		**X33_P0**	
A to Z ↓	0.0351		0.4432	
A to Z ↑	0.0267		0.7455	

B to Z ↓	0.0347		0.4437	
B to Z ↑	0.0245		0.7434	
C to Z ↓	0.0283		0.4342	
C to Z ↑	0.0248		0.7443	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	6.789e-07	2.024e-12
X17_P0	9.698e-07	2.276e-12
X33_P0	1.893e-06	3.788e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	1.332e-04	1.356e-04	2.730e-04
B (output stable)	6.757e-05	6.667e-05	1.305e-04
C (output stable)	7.278e-05	7.304e-05	1.399e-04
A to Z	2.662e-03	3.846e-03	7.981e-03
B to Z	2.343e-03	3.529e-03	7.354e-03
C to Z	2.876e-03	4.024e-03	8.291e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

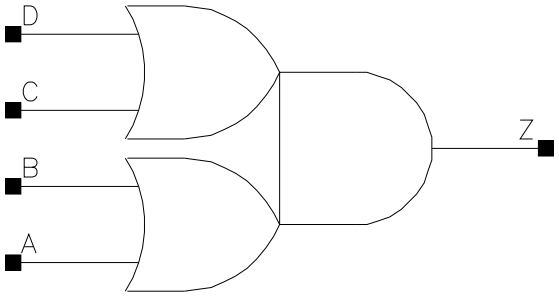
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	-2.448e-06	-2.593e-06	-5.258e-06
B (output stable)	4.703e-06	4.836e-06	9.434e-06
C (output stable)	1.180e-06	1.404e-06	2.424e-06
A to Z	-2.992e-07	-2.478e-07	-1.126e-06
B to Z	-1.404e-07	-7.789e-08	-2.857e-07
C to Z	-2.996e-07	-1.914e-07	-2.235e-07

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0018
B	0.0007	0.0010	0.0018
C	0.0006	0.0009	0.0018
D	0.0006	0.0009	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0474	0.0412	1.6986	0.8657
A to Z ↑	0.0304	0.0271	2.9563	1.4789
B to Z ↓	0.0478	0.0412	1.7005	0.8660
B to Z ↑	0.0295	0.0260	2.9540	1.4776

C to Z ↓	0.0418	0.0369	1.6873	0.8621
C to Z ↑	0.0293	0.0269	2.9540	1.4792
D to Z ↓	0.0413	0.0362	1.6889	0.8633
D to Z ↑	0.0278	0.0249	2.9520	1.4765
	X33_P0		**X33_P0**	
A to Z ↓	0.0416		0.4468	
A to Z ↑	0.0271		0.7431	
B to Z ↓	0.0399		0.4471	
B to Z ↑	0.0254		0.7417	
C to Z ↓	0.0366		0.4441	
C to Z ↑	0.0262		0.7430	
D to Z ↓	0.0345		0.4450	
D to Z ↑	0.0242		0.7413	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	6.167e-07	2.528e-12
X17_P0	1.164e-06	2.780e-12
X33_P0	2.157e-06	4.543e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	3.134e-05	5.526e-05	1.602e-04
B (output stable)	1.832e-05	2.696e-05	7.434e-05
C (output stable)	6.781e-05	1.095e-04	3.379e-04
D (output stable)	7.870e-05	1.035e-04	2.610e-04
A to Z	3.086e-03	4.972e-03	9.805e-03
B to Z	2.919e-03	4.644e-03	8.850e-03
C to Z	2.679e-03	4.395e-03	8.572e-03
D to Z	2.503e-03	4.062e-03	7.613e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

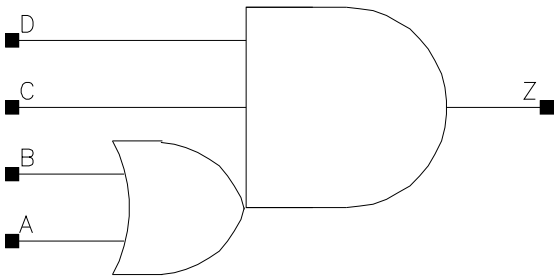
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	-1.412e-06	-2.433e-06	-1.056e-05
B (output stable)	5.662e-06	1.236e-05	3.096e-05
C (output stable)	-3.817e-06	-4.678e-06	-2.947e-05
D (output stable)	6.576e-06	1.476e-05	4.466e-05
A to Z	-6.889e-07	-1.372e-07	-2.576e-06
B to Z	-2.721e-07	3.700e-08	-4.641e-07
C to Z	-4.422e-07	-2.217e-07	-3.110e-06
D to Z	1.897e-08	-1.417e-07	-1.022e-06

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	1.088	1.3056
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0006	0.0009	0.0015	0.0018
B	0.0006	0.0010	0.0016	0.0019
C	0.0007	0.0009	0.0016	0.0018
D	0.0006	0.0010	0.0015	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0408	0.0386	1.7877	0.8721
A to Z ↑	0.0350	0.0326	3.0522	1.4795
B to Z ↓	0.0409	0.0372	1.7886	0.8731
B to Z ↑	0.0334	0.0299	3.0529	1.4781
C to Z ↓	0.0328	0.0306	1.7390	0.8533

C to Z ↑	0.0335	0.0309	3.0460	1.4759
D to Z ↓	0.0319	0.0296	1.7388	0.8530
D to Z ↑	0.0349	0.0320	3.0471	1.4764
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0402	0.0389	0.5963	0.4463
A to Z ↑	0.0334	0.0340	1.0050	0.7537
B to Z ↓	0.0386	0.0374	0.5969	0.4463
B to Z ↑	0.0310	0.0313	1.0035	0.7519
C to Z ↓	0.0319	0.0308	0.5827	0.4362
C to Z ↑	0.0317	0.0316	1.0041	0.7520
D to Z ↓	0.0305	0.0296	0.5817	0.4356
D to Z ↑	0.0320	0.0323	1.0041	0.7518

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	4.427e-07	2.276e-12
X17_P0	8.948e-07	2.780e-12
X25_P0	1.382e-06	4.291e-12
X33_P0	1.736e-06	4.543e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	7.456e-05	1.467e-04	2.585e-04	2.928e-04
B (output stable)	5.973e-05	1.150e-04	1.955e-04	2.173e-04
C (output stable)	1.421e-05	2.717e-05	7.201e-05	8.343e-05
D (output stable)	3.000e-05	6.855e-05	1.780e-04	1.875e-04
A to Z	2.570e-03	4.511e-03	7.306e-03	8.984e-03
B to Z	2.412e-03	4.074e-03	6.622e-03	8.106e-03
C to Z	2.781e-03	4.801e-03	7.937e-03	9.567e-03
D to Z	2.668e-03	4.582e-03	7.381e-03	8.985e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

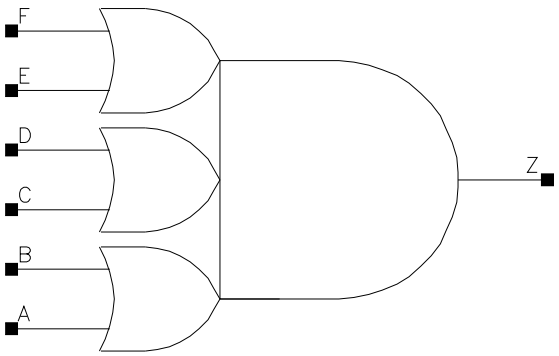
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	-1.530e-06	-4.364e-06	-5.929e-06	-6.015e-06
B (output stable)	1.050e-06	5.250e-06	5.534e-06	8.837e-06
C (output stable)	4.280e-07	3.819e-07	4.326e-07	-1.988e-07
D (output stable)	4.770e-07	4.253e-07	8.171e-07	4.206e-08
A to Z	-2.540e-07	-1.629e-06	-2.752e-06	-3.048e-06
B to Z	-9.610e-08	-2.294e-07	-2.950e-07	-3.100e-07
C to Z	-1.492e-07	-3.987e-08	-1.733e-08	6.100e-08
D to Z	6.770e-08	5.729e-07	8.398e-07	8.190e-07

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0007	0.0009	0.0015
B	0.0006	0.0009	0.0018
C	0.0006	0.0009	0.0016
D	0.0006	0.0009	0.0018
E	0.0006	0.0009	0.0016
F	0.0006	0.0009	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0538	0.0462	1.8292	0.8885
A to Z ↑	0.0385	0.0348	3.0247	1.4934
B to Z ↓	0.0540	0.0466	1.8299	0.8889
B to Z ↑	0.0373	0.0338	3.0257	1.4930
C to Z ↓	0.0495	0.0440	1.8177	0.8875
C to Z ↑	0.0390	0.0350	3.0275	1.4934
D to Z ↓	0.0499	0.0440	1.8192	0.8876
D to Z ↑	0.0375	0.0335	3.0254	1.4927
E to Z ↓	0.0433	0.0389	1.8051	0.8824
E to Z ↑	0.0359	0.0329	3.0254	1.4922
F to Z ↓	0.0437	0.0386	1.8076	0.8833
F to Z ↑	0.0344	0.0311	3.0227	1.4913
	X33_P0		X33_P0	
A to Z ↓	0.0470		0.4561	
A to Z ↑	0.0360		0.7533	
B to Z ↓	0.0475		0.4562	
B to Z ↑	0.0339		0.7519	
C to Z ↓	0.0437		0.4537	
C to Z ↑	0.0360		0.7532	
D to Z ↓	0.0438		0.4539	
D to Z ↑	0.0340		0.7516	
E to Z ↓	0.0387		0.4514	
E to Z ↑	0.0340		0.7527	
F to Z ↓	0.0388		0.4518	
F to Z ↑	0.0318		0.7512	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	6.115e-07	3.032e-12
X17_P0	1.177e-06	3.285e-12
X33_P0	2.221e-06	5.553e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	2.395e-05	4.306e-05	7.748e-05
B (output stable)	1.219e-05	2.472e-05	3.842e-05
C (output stable)	5.028e-05	7.857e-05	1.613e-04
D (output stable)	4.544e-05	7.238e-05	1.543e-04
E (output stable)	7.714e-05	1.184e-04	2.210e-04
F (output stable)	1.221e-04	1.795e-04	3.453e-04
A to Z	3.539e-03	5.759e-03	1.135e-02
B to Z	3.365e-03	5.450e-03	1.076e-02
C to Z	3.225e-03	5.326e-03	1.042e-02
D to Z	3.060e-03	5.003e-03	9.805e-03
E to Z	2.808e-03	4.698e-03	9.216e-03
F to Z	2.655e-03	4.380e-03	8.637e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

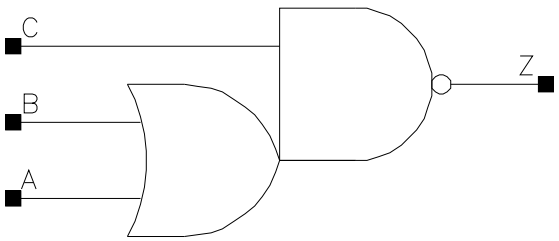
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	-1.054e-06	-1.999e-06	-3.207e-06
B (output stable)	5.052e-06	1.035e-05	1.998e-05
C (output stable)	-2.162e-06	-3.483e-06	-7.162e-06
D (output stable)	4.686e-06	9.967e-06	1.817e-05
E (output stable)	-2.036e-06	-2.257e-06	-5.243e-06
F (output stable)	3.151e-06	8.877e-06	1.501e-05
A to Z	-7.542e-07	-1.508e-06	-2.270e-06
B to Z	-3.442e-08	-1.147e-06	-1.784e-06
C to Z	-8.864e-07	-9.717e-07	-1.955e-06
D to Z	-4.678e-07	-5.462e-07	-9.922e-07
E to Z	-5.719e-07	-6.018e-07	-1.234e-06
F to Z	-2.372e-07	-4.116e-07	-8.892e-07

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X34_P0	1.200	2.720	3.2640
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X34_P0	X46_P0
A	0.0007	0.0022	0.0046	0.0059
B	0.0007	0.0021	0.0042	0.0056
C	0.0008	0.0023	0.0048	0.0062

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0121	0.0125	3.3195	1.0890
A to Z ↑	0.0183	0.0195	6.2864	2.1351
B to Z ↓	0.0100	0.0104	3.2416	1.0965
B to Z ↑	0.0168	0.0168	6.3202	2.1493
C to Z ↓	0.0121	0.0123	3.0011	0.9963
C to Z ↑	0.0164	0.0162	3.0596	1.0182
	X34_P0	**X46_P0**	**X34_P0**	**X46_P0**
A to Z ↓	0.0131	0.0131	0.5563	0.4258

A to Z ↑	0.0202	0.0199	1.0654	0.8190
B to Z ↓	0.0108	0.0108	0.5654	0.4343
B to Z ↑	0.0172	0.0171	1.0727	0.8241
C to Z ↓	0.0127	0.0126	0.5118	0.3925
C to Z ↑	0.0166	0.0164	0.5091	0.3901

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P0	3.990e-07	1.772e-12
X17_P0	1.094e-06	3.282e-12
X34_P0	2.154e-06	5.804e-12
X46_P0	2.823e-06	7.317e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	1.244e-04	4.143e-04	8.714e-04	1.092e-03
B (output stable)	6.841e-05	2.013e-04	4.162e-04	5.250e-04
C (output stable)	6.310e-05	2.180e-04	4.600e-04	5.648e-04
A to Z	1.196e-03	3.878e-03	8.134e-03	1.044e-02
B to Z	8.819e-04	2.676e-03	5.548e-03	7.197e-03
C to Z	1.407e-03	4.317e-03	9.017e-03	1.161e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

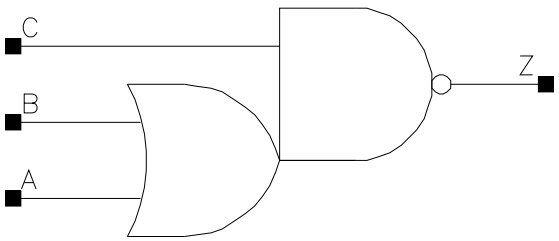
Pin Cycle (vdds)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	-1.813e-06	-8.968e-06	-2.234e-05	-2.600e-05
B (output stable)	5.083e-06	9.761e-06	1.881e-05	2.529e-05
C (output stable)	7.771e-08	2.199e-06	5.888e-06	7.315e-06
A to Z	-1.660e-07	-2.500e-06	-6.829e-06	-7.320e-06
B to Z	-8.270e-08	-1.013e-06	-2.374e-06	-1.313e-06
C to Z	4.573e-08	9.367e-07	-6.027e-07	3.947e-07

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.544	0.6528
X11_P0	1.200	0.952	1.1424
X17_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X17_P0	X23_P0
A	0.0008	0.0015	0.0023	0.0032
B	0.0007	0.0016	0.0022	0.0029
C	0.0008	0.0015	0.0022	0.0031
	X46_P0			
A	0.0064			
B	0.0058			
C	0.0061			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0131	0.0133	3.3394	1.5612
A to Z ↑	0.0220	0.0223	6.6163	3.1323
B to Z ↓	0.0115	0.0116	3.2770	1.5150

B to Z ↑	0.0209	0.0211	6.6448	3.1467
C to Z ↓	0.0100	0.0100	3.1215	1.4527
C to Z ↑	0.0129	0.0128	3.2798	1.5448
	X17_P0	**X23_P0**	**X17_P0**	**X23_P0**
A to Z ↓	0.0128	0.0135	1.0874	0.8048
A to Z ↑	0.0212	0.0232	2.0749	1.5839
B to Z ↓	0.0112	0.0116	1.0831	0.8051
B to Z ↑	0.0197	0.0206	2.0854	1.5918
C to Z ↓	0.0096	0.0099	1.0248	0.7575
C to Z ↑	0.0120	0.0124	1.0263	0.7821
	X46_P0		**X46_P0**	
A to Z ↓	0.0134		0.4219	
A to Z ↑	0.0228		0.8005	
B to Z ↓	0.0115		0.4173	
B to Z ↑	0.0202		0.8049	
C to Z ↓	0.0100		0.3953	
C to Z ↑	0.0121		0.3958	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P0	4.106e-07	1.772e-12
X11_P0	8.009e-07	2.526e-12
X17_P0	1.158e-06	3.283e-12
X23_P0	1.557e-06	4.292e-12
X46_P0	2.953e-06	7.315e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	3.965e-05	8.674e-05	1.273e-04	2.391e-04
B (output stable)	1.932e-05	4.474e-05	6.401e-05	1.122e-04
C (output stable)	2.673e-04	6.215e-04	7.846e-04	1.170e-03
A to Z	1.514e-03	3.267e-03	4.504e-03	6.814e-03
B to Z	1.181e-03	2.585e-03	3.441e-03	4.953e-03
C to Z	8.774e-04	1.907e-03	2.603e-03	3.783e-03
	X46_P0			
A (output stable)	4.579e-04			
B (output stable)	2.152e-04			
C (output stable)	2.184e-03			
A to Z	1.315e-02			
B to Z	9.453e-03			
C to Z	7.246e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	-1.743e-06	-3.342e-06	-6.001e-06	-1.258e-05
B (output stable)	4.796e-06	1.026e-05	1.529e-05	1.402e-05
C (output stable)	6.451e-08	-3.992e-06	-1.200e-09	-5.539e-06
A to Z	-5.360e-07	-1.944e-06	-1.741e-06	-6.831e-06
B to Z	-1.267e-07	-2.080e-07	3.670e-07	1.100e-08
C to Z	1.828e-07	4.933e-08	7.340e-07	6.890e-07

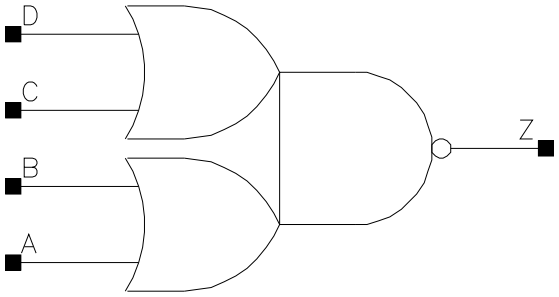
	X46_P0			
A (output stable)	-2.234e-05			
B (output stable)	2.564e-05			
C (output stable)	-9.428e-06			
A to Z	-1.183e-05			
B to Z	3.800e-07			
C to Z	3.187e-06			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0008	0.0015	0.0023	0.0032
B	0.0008	0.0014	0.0021	0.0029
C	0.0007	0.0015	0.0022	0.0031
D	0.0007	0.0014	0.0020	0.0028
	X42_P0			
A	0.0064			
B	0.0058			
C	0.0061			
D	0.0057			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0143	0.0152	3.0752	1.5299
A to Z ↑	0.0253	0.0255	6.9544	3.1966
B to Z ↓	0.0130	0.0133	2.9981	1.5329
B to Z ↑	0.0239	0.0227	6.9737	3.2144
C to Z ↓	0.0124	0.0133	3.1360	1.5467
C to Z ↑	0.0193	0.0206	6.8010	3.2025
D to Z ↓	0.0105	0.0108	3.0443	1.5562
D to Z ↑	0.0176	0.0167	6.8338	3.2293
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0145	0.0149	1.0510	0.7584
A to Z ↑	0.0240	0.0249	2.1524	1.5893
B to Z ↓	0.0131	0.0130	1.0534	0.7567
B to Z ↑	0.0220	0.0225	2.1628	1.5975
C to Z ↓	0.0127	0.0129	1.0645	0.7674
C to Z ↑	0.0191	0.0197	2.1569	1.5903
D to Z ↓	0.0107	0.0106	1.0754	0.7703
D to Z ↑	0.0161	0.0162	2.1740	1.6024
	X42_P0		**X42_P0**	
A to Z ↓	0.0152		0.4002	
A to Z ↑	0.0249		0.8097	
B to Z ↓	0.0133		0.3946	
B to Z ↑	0.0226		0.8133	
C to Z ↓	0.0136		0.4061	
C to Z ↑	0.0199		0.8045	
D to Z ↓	0.0110		0.4020	
D to Z ↑	0.0165		0.8107	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P0	4.708e-07	2.024e-12
X10_P0	9.757e-07	3.285e-12
X15_P0	1.370e-06	4.040e-12
X21_P0	1.787e-06	5.300e-12
X42_P0	3.444e-06	9.333e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	5.065e-05	1.578e-04	2.072e-04	2.998e-04
B (output stable)	2.216e-05	7.125e-05	8.991e-05	1.228e-04
C (output stable)	1.016e-04	3.362e-04	3.950e-04	6.091e-04
D (output stable)	9.036e-05	2.348e-04	2.978e-04	4.329e-04
A to Z	1.841e-03	4.196e-03	5.703e-03	8.116e-03
B to Z	1.518e-03	3.206e-03	4.404e-03	6.235e-03
C to Z	1.292e-03	3.076e-03	4.087e-03	5.792e-03
D to Z	9.930e-04	2.099e-03	2.853e-03	3.967e-03
	X42_P0			
A (output stable)	5.942e-04			
B (output stable)	2.511e-04			
C (output stable)	1.183e-03			
D (output stable)	8.493e-04			

A to Z	1.603e-02			
B to Z	1.233e-02			
C to Z	1.161e-02			
D to Z	7.988e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

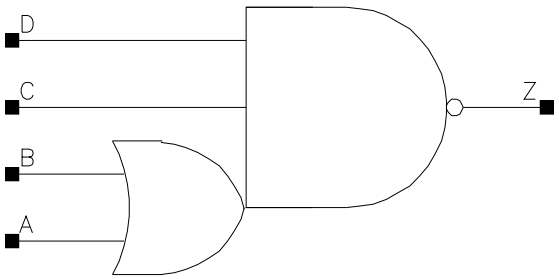
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	-2.329e-06	-1.023e-05	-8.801e-06	-1.699e-05
B (output stable)	1.139e-05	3.134e-05	3.158e-05	5.186e-05
C (output stable)	-4.714e-06	-3.027e-05	-2.142e-05	-4.718e-05
D (output stable)	1.305e-05	4.751e-05	4.118e-05	7.637e-05
A to Z	-7.473e-07	-2.092e-06	-3.240e-06	-3.458e-06
B to Z	-1.433e-08	-3.763e-07	3.067e-07	-3.470e-07
C to Z	-2.250e-07	-2.646e-06	-1.494e-06	-4.584e-06
D to Z	1.473e-08	-7.207e-07	5.967e-07	-3.580e-07
	X42_P0			
A (output stable)	-3.032e-05			
B (output stable)	9.357e-05			
C (output stable)	-8.378e-05			
D (output stable)	1.349e-04			
A to Z	-6.500e-06			
B to Z	-6.530e-07			
C to Z	-7.693e-06			
D to Z	5.297e-07			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X21_P0	1.200	2.448	2.9376
X31_P0	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X21_P0	X31_P0
A	0.0008	0.0014	0.0029	0.0044
B	0.0010	0.0014	0.0027	0.0041
C	0.0008	0.0016	0.0031	0.0047
D	0.0008	0.0015	0.0030	0.0044

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0173	0.0166	4.2539	2.2916
A to Z ↑	0.0241	0.0223	6.3039	3.1717
B to Z ↓	0.0155	0.0137	4.3093	2.3029
B to Z ↑	0.0226	0.0193	6.3524	3.1938
C to Z ↓	0.0165	0.0169	4.0147	2.1573

C to Z ↑	0.0197	0.0192	2.9799	1.5014
D to Z ↓	0.0174	0.0167	4.0401	2.1709
D to Z ↑	0.0189	0.0177	3.0228	1.5055
	X21_P0	**X31_P0**	**X21_P0**	**X31_P0**
A to Z ↓	0.0169	0.0172	1.2000	0.8161
A to Z ↑	0.0219	0.0219	1.5859	1.0643
B to Z ↓	0.0139	0.0141	1.2066	0.8237
B to Z ↑	0.0189	0.0189	1.5953	1.0718
C to Z ↓	0.0169	0.0171	1.1309	0.7704
C to Z ↑	0.0189	0.0189	0.7620	0.5147
D to Z ↓	0.0169	0.0171	1.1373	0.7747
D to Z ↑	0.0174	0.0175	0.7630	0.5141

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P0	3.707e-07	2.276e-12
X10_P0	6.810e-07	3.284e-12
X21_P0	1.271e-06	5.300e-12
X31_P0	1.863e-06	7.317e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	1.472e-04	3.042e-04	5.799e-04	8.534e-04
B (output stable)	1.172e-04	2.261e-04	4.246e-04	6.199e-04
C (output stable)	2.827e-05	7.647e-05	1.432e-04	2.075e-04
D (output stable)	6.423e-05	1.881e-04	3.209e-04	4.716e-04
A to Z	1.868e-03	3.244e-03	6.294e-03	9.361e-03
B to Z	1.416e-03	2.297e-03	4.417e-03	6.629e-03
C to Z	2.167e-03	4.111e-03	7.893e-03	1.175e-02
D to Z	1.966e-03	3.481e-03	6.704e-03	9.999e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

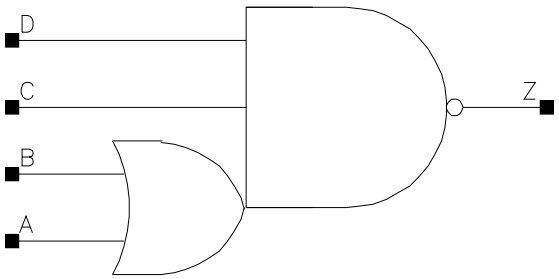
Pin Cycle (vdds)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	-4.850e-06	-7.365e-06	-1.324e-05	-1.837e-05
B (output stable)	4.349e-06	8.825e-06	1.358e-05	1.898e-05
C (output stable)	3.566e-07	5.318e-07	1.254e-06	1.511e-06
D (output stable)	4.508e-07	1.087e-06	2.268e-06	2.854e-06
A to Z	-1.724e-06	-2.330e-06	-3.818e-06	-4.894e-06
B to Z	-1.530e-07	2.740e-07	-5.920e-07	-7.470e-07
C to Z	7.067e-08	5.770e-07	1.259e-06	1.628e-06
D to Z	4.083e-07	8.600e-08	-4.563e-07	-7.130e-07

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0008	0.0016	0.0024	0.0032
B	0.0008	0.0015	0.0022	0.0030
C	0.0008	0.0015	0.0023	0.0030
D	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0167	0.0180	4.3465	2.2769
A to Z ↑	0.0254	0.0274	6.1219	3.1215
B to Z ↓	0.0150	0.0158	4.2506	2.2743
B to Z ↑	0.0245	0.0253	6.1435	3.1345
C to Z ↓	0.0140	0.0155	4.0952	2.1665

C to Z ↑	0.0158	0.0166	3.0427	1.5377
D to Z ↓	0.0132	0.0139	4.1267	2.1833
D to Z ↑	0.0142	0.0144	3.0637	1.5500
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0177	0.0179	1.5716	1.1864
A to Z ↑	0.0264	0.0270	2.1033	1.5950
B to Z ↓	0.0158	0.0157	1.5610	1.1833
B to Z ↑	0.0246	0.0252	2.1120	1.6017
C to Z ↓	0.0152	0.0154	1.4905	1.1265
C to Z ↑	0.0160	0.0163	1.0258	0.7717
D to Z ↓	0.0136	0.0140	1.5022	1.1343
D to Z ↑	0.0139	0.0142	1.0336	0.7773

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P0	3.780e-07	2.276e-12
X10_P0	7.215e-07	3.283e-12
X15_P0	1.004e-06	4.040e-12
X21_P0	1.364e-06	5.554e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	2.589e-05	7.158e-05	9.806e-05	1.366e-04
B (output stable)	1.733e-05	5.497e-05	6.679e-05	9.810e-05
C (output stable)	8.059e-05	1.572e-04	2.382e-04	3.181e-04
D (output stable)	1.636e-04	5.304e-04	6.507e-04	9.530e-04
A to Z	2.090e-03	4.571e-03	6.443e-03	8.841e-03
B to Z	1.728e-03	3.605e-03	5.081e-03	6.969e-03
C to Z	1.363e-03	3.077e-03	4.253e-03	5.900e-03
D to Z	1.147e-03	2.420e-03	3.407e-03	4.661e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

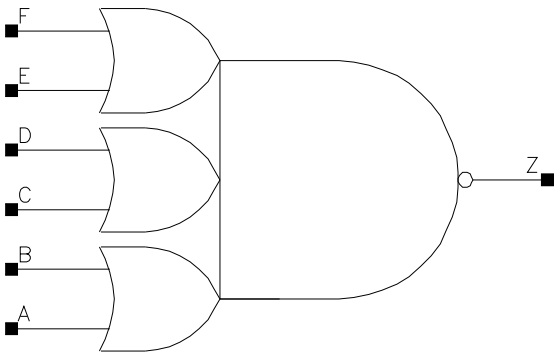
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	-1.432e-06	-6.270e-06	-5.290e-06	-1.035e-05
B (output stable)	3.152e-06	9.683e-06	9.510e-06	1.622e-05
C (output stable)	5.602e-08	8.727e-07	7.214e-08	1.572e-06
D (output stable)	5.528e-08	-2.448e-06	-2.770e-06	-4.687e-06
A to Z	-8.100e-07	-4.271e-06	-4.111e-06	-7.290e-06
B to Z	-7.350e-07	-1.824e-06	-2.512e-06	-3.535e-06
C to Z	7.767e-08	4.730e-07	1.304e-06	3.553e-07
D to Z	3.893e-07	7.103e-07	5.620e-07	-2.187e-07

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	1.088	1.3056
X9_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X9_P0
A	0.0007	0.0016
B	0.0006	0.0015
C	0.0006	0.0016
D	0.0006	0.0014
E	0.0006	0.0015
F	0.0006	0.0014

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X9_P0	X3_P0	X9_P0
A to Z ↓	0.0208	0.0220	4.9754	2.0719
A to Z ↑	0.0331	0.0318	8.5389	3.1397
B to Z ↓	0.0197	0.0199	5.0095	2.0715
B to Z ↑	0.0332	0.0298	8.5606	3.1506
C to Z ↓	0.0203	0.0210	5.0222	2.0839
C to Z ↑	0.0291	0.0280	8.5633	3.1335
D to Z ↓	0.0188	0.0187	5.0575	2.0875
D to Z ↑	0.0289	0.0256	8.5956	3.1482
E to Z ↓	0.0170	0.0180	5.0539	2.0854
E to Z ↑	0.0233	0.0229	8.5848	3.1354
F to Z ↓	0.0156	0.0154	5.0934	2.0900
F to Z ↑	0.0227	0.0197	8.6377	3.1573

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P0	4.492e-07	2.780e-12
X9_P0	1.123e-06	4.543e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P0	X9_P0
A (output stable)	3.121e-05	1.236e-04
B (output stable)	1.682e-05	7.475e-05
C (output stable)	6.727e-05	2.362e-04
D (output stable)	6.730e-05	2.002e-04
E (output stable)	1.013e-04	2.859e-04
F (output stable)	1.631e-04	3.923e-04
A to Z	2.431e-03	6.331e-03
B to Z	2.191e-03	5.333e-03
C to Z	1.996e-03	5.195e-03
D to Z	1.762e-03	4.269e-03
E to Z	1.460e-03	3.988e-03
F to Z	1.242e-03	3.051e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

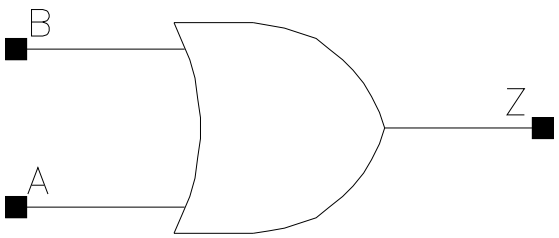
Pin Cycle (vdds)	X3_P0	X9_P0
A (output stable)	-1.401e-06	-8.455e-06
B (output stable)	7.196e-06	3.326e-05
C (output stable)	-2.693e-06	-1.820e-05
D (output stable)	7.088e-06	3.277e-05
E (output stable)	-2.194e-06	-1.435e-05
F (output stable)	5.241e-06	2.194e-05
A to Z	-1.419e-06	-1.982e-06
B to Z	-1.219e-06	3.631e-07
C to Z	-8.436e-07	-3.378e-06
D to Z	-2.483e-07	-6.046e-07
E to Z	-2.022e-07	-2.980e-06
F to Z	-2.609e-07	-1.764e-06

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X33_P0	1.200	1.360	1.6320
X50_P0	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P0	X16_P0	X33_P0	X50_P0
A	0.0007	0.0009	0.0017	0.0018
B	0.0006	0.0009	0.0018	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0373	0.0335	1.7476	0.8814
A to Z ↑	0.0213	0.0220	2.9779	1.5007
B to Z ↓	0.0365	0.0328	1.7488	0.8817
B to Z ↑	0.0202	0.0206	2.9763	1.5004
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0347	0.0404	0.4378	0.3025
A to Z ↑	0.0219	0.0219	0.7321	0.4955
B to Z ↓	0.0327	0.0388	0.4376	0.3024
B to Z ↑	0.0202	0.0206	0.7317	0.4953

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	5.384e-07	1.772e-12
X16_P0	9.711e-07	2.024e-12
X33_P0	1.862e-06	3.284e-12
X50_P0	2.433e-06	3.789e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	3.568e-05	6.708e-05	1.946e-04	1.869e-04
B (output stable)	9.342e-06	1.429e-05	1.132e-04	1.008e-04
A to Z	2.335e-03	3.727e-03	7.849e-03	1.051e-02
B to Z	2.155e-03	3.409e-03	6.894e-03	9.630e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

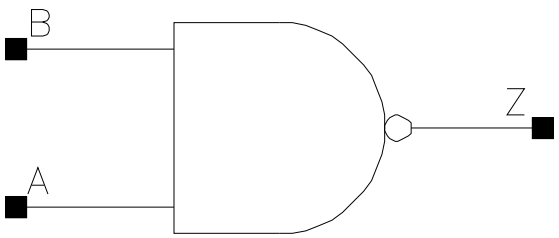
Pin Cycle (vdds)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	-2.018e-06	-3.372e-06	-1.355e-05	-1.331e-05
B (output stable)	1.598e-05	2.886e-05	1.054e-04	1.036e-04
A to Z	-4.523e-07	-5.566e-07	-3.285e-06	-3.405e-06
B to Z	-5.550e-08	3.943e-08	-3.342e-07	-3.530e-07

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X16_P0	1.200	0.952	1.1424
X24_P0	1.200	1.088	1.3056
X32_P0	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P0	X16_P0	X24_P0	X32_P0
A	0.0009	0.0009	0.0009	0.0009
B	0.0010	0.0010	0.0010	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0288	0.0299	1.6903	0.8835
A to Z ↑	0.0326	0.0334	3.0174	1.5422
B to Z ↓	0.0294	0.0306	1.6908	0.8837
B to Z ↑	0.0313	0.0316	3.0182	1.5413
	X24_P0	**X32_P0**	**X24_P0**	**X32_P0**
A to Z ↓	0.0327	0.0335	0.5986	0.4481
A to Z ↑	0.0353	0.0364	1.0301	0.7690
B to Z ↓	0.0335	0.0343	0.5984	0.4484
B to Z ↑	0.0335	0.0352	1.0296	0.7690

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	9.880e-07	2.276e-12
X16_P0	1.304e-06	2.531e-12
X24_P0	1.594e-06	2.780e-12
X32_P0	2.032e-06	3.035e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	3.213e-05	3.219e-05	3.142e-05	3.276e-05
B (output stable)	7.255e-05	7.281e-05	7.293e-05	7.463e-05
A to Z	4.522e-03	5.230e-03	6.564e-03	8.687e-03
B to Z	4.328e-03	5.047e-03	6.387e-03	8.489e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

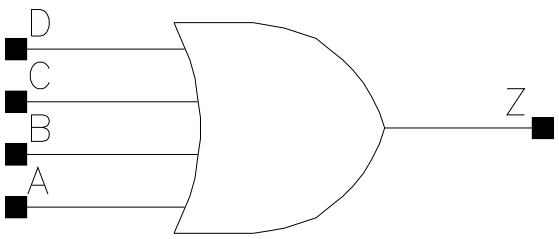
Pin Cycle (vdds)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	6.144e-08	6.326e-08	5.842e-08	6.356e-08
B (output stable)	4.003e-08	4.020e-08	4.044e-08	3.844e-08
A to Z	-6.270e-08	-2.871e-07	-2.850e-07	-2.500e-07
B to Z	-1.528e-07	1.100e-07	-7.200e-08	-1.580e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X27_P0
A	0.0016	0.0018
B	0.0015	0.0018
C	0.0016	0.0018
D	0.0015	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0383	0.0401	1.0620	0.7946
A to Z ↑	0.0228	0.0221	0.9821	0.7315
B to Z ↓	0.0367	0.0380	1.0624	0.7949
B to Z ↑	0.0216	0.0206	0.9808	0.7302
C to Z ↓	0.0368	0.0385	1.0624	0.7943
C to Z ↑	0.0218	0.0217	0.9829	0.7333
D to Z ↓	0.0352	0.0368	1.0627	0.7943
D to Z ↑	0.0207	0.0203	0.9827	0.7331

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X20_P0	1.492e-06	4.797e-12
X27_P0	2.028e-06	5.553e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X20_P0	X27_P0
A (output stable)	1.775e-03	2.434e-03
B (output stable)	1.426e-03	1.942e-03
C (output stable)	1.700e-03	2.438e-03
D (output stable)	1.324e-03	1.917e-03
A to Z	7.376e-03	1.028e-02
B to Z	6.686e-03	9.282e-03
C to Z	6.512e-03	8.964e-03
D to Z	5.857e-03	8.070e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

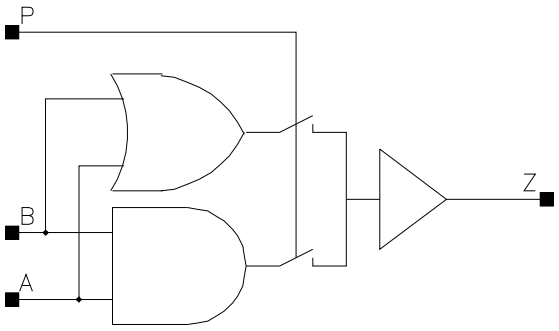
Pin Cycle (vdds)	X20_P0	X27_P0
A (output stable)	-4.590e-06	-8.857e-06
B (output stable)	1.928e-05	3.763e-05
C (output stable)	-1.083e-05	-2.620e-05
D (output stable)	2.429e-05	4.711e-05
A to Z	-1.501e-06	-2.832e-06
B to Z	5.000e-08	-2.810e-07
C to Z	-1.225e-06	-2.937e-06
D to Z	-1.340e-07	4.780e-07

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X16_P0	1.200	1.224	1.4688
X25_P0	1.200	2.040	2.4480
X33_P0	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0011	0.0017	0.0029	0.0029
B	0.0011	0.0016	0.0033	0.0034
P	0.0006	0.0009	0.0017	0.0017

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0448	0.0411	1.7844	0.8725
A to Z ↑	0.0284	0.0266	3.0215	1.5091
B to Z ↓	0.0443	0.0408	1.7945	0.8792
B to Z ↑	0.0292	0.0272	3.0219	1.5116
P to Z ↓	0.0402	0.0374	1.7972	0.8807
P to Z ↑	0.0281	0.0264	3.0177	1.5093
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**

A to Z ↓	0.0396	0.0422	0.5948	0.4507
A to Z ↑	0.0266	0.0279	1.0164	0.7609
B to Z ↓	0.0391	0.0414	0.5981	0.4529
B to Z ↑	0.0276	0.0286	1.0177	0.7616
P to Z ↓	0.0364	0.0389	0.5997	0.4541
P to Z ↑	0.0262	0.0274	1.0171	0.7606

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	5.603e-07	2.525e-12
X16_P0	1.138e-06	3.033e-12
X25_P0	1.876e-06	4.544e-12
X33_P0	2.145e-06	4.796e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	7.064e-05	1.201e-04	2.497e-04	2.524e-04
B (output stable)	1.513e-04	2.397e-04	4.418e-04	4.478e-04
P (output stable)	1.305e-04	2.184e-04	3.773e-04	3.899e-04
A to Z	2.721e-03	4.588e-03	7.944e-03	9.156e-03
B to Z	2.629e-03	4.433e-03	7.585e-03	8.791e-03
P to Z	2.362e-03	4.044e-03	7.027e-03	8.227e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

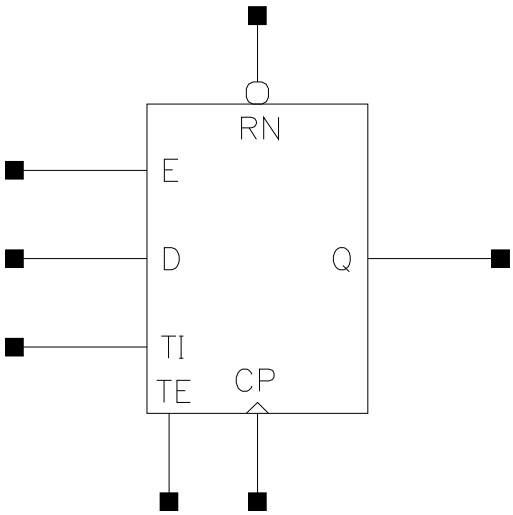
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	-3.496e-06	-5.698e-06	-9.289e-06	-9.293e-06
B (output stable)	-1.196e-05	-1.431e-05	-2.630e-06	-3.748e-06
P (output stable)	2.227e-05	4.224e-05	5.617e-05	5.778e-05
A to Z	-2.111e-06	-2.270e-06	-3.989e-06	-4.261e-06
B to Z	-1.669e-06	-2.291e-06	-3.626e-06	-3.629e-06
P to Z	-1.438e-07	-1.249e-07	-8.970e-07	-8.198e-07

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.488	5.3856
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0007	0.0007	0.0008
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0784	0.0418	3.8429	1.7402
CP to Q ↑	0.0622	0.0530	6.0269	2.9908
RN to Q ↓	0.0660	0.0553	3.2564	1.8289
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0703	0.0738	0.8451	0.4461
CP to Q ↑	0.0860	0.0896	1.4679	0.7497
RN to Q ↓	0.0932	0.0965	0.8421	0.4446

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1162	0.0794	0.0794	0.0794
CP ↑	min_pulse_width to CP	0.0686	0.0348	0.0311	0.0311
D ↓	hold_rising to CP	-0.1227	-0.0628	-0.0628	-0.0628
D ↑	hold_rising to CP	-0.0598	-0.0190	-0.0215	-0.0215
D ↓	setup_rising to CP	0.1755	0.1071	0.1097	0.1097
D ↑	setup_rising to CP	0.0947	0.0512	0.0512	0.0512
E ↓	hold_rising to CP	-0.0720	-0.0720	-0.0716	-0.0716
E ↑	hold_rising to CP	-0.0579	-0.0215	-0.0215	-0.0215
E ↓	setup_rising to CP	0.1434	0.1434	0.1437	0.1434
E ↑	setup_rising to CP	0.1639	0.1098	0.1098	0.1098
RN ↓	min_pulse_width to RN	0.0703	0.0779	0.0708	0.0708
RN ↑	recovery_rising to CP	0.0226	0.0171	0.0201	0.0201
RN ↑	removal_rising to CP	-0.0122	-0.0074	-0.0074	-0.0074
TE ↓	hold_rising to CP	-0.0522	-0.0406	-0.0406	-0.0406
TE ↑	hold_rising to CP	-0.0380	-0.0237	-0.0234	-0.0234
TE ↓	setup_rising to CP	0.1149	0.0898	0.0898	0.0898
TE ↑	setup_rising to CP	0.2002	0.1391	0.1391	0.1391
TI ↓	hold_rising to CP	-0.1499	-0.0789	-0.0789	-0.0804
TI ↑	hold_rising to CP	-0.0457	-0.0223	-0.0263	-0.0263
TI ↓	setup_rising to CP	0.2007	0.1299	0.1299	0.1299
TI ↑	setup_rising to CP	0.0795	0.0575	0.0575	0.0575

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	2.018e-06	9.677e-12
X8_P0	2.183e-06	9.081e-12
X17_P0	2.685e-06	9.585e-12
X33_P0	3.283e-06	1.009e-11

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

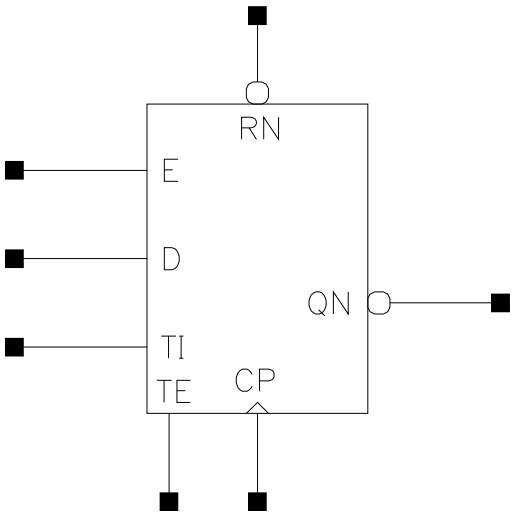
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	4.292e-03	4.324e-03	4.332e-03	4.337e-03
Clock 100Mhz Data 25Mhz	7.010e-03	7.150e-03	7.830e-03	8.595e-03
Clock 100Mhz Data 50Mhz	9.728e-03	9.976e-03	1.133e-02	1.285e-02
Clock = 0 Data 100Mhz	6.177e-03	6.000e-03	5.942e-03	5.914e-03
Clock = 1 Data 100Mhz	2.402e-03	2.428e-03	2.438e-03	2.444e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.624	5.5488
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
CP to QN ↓	0.0770	0.0719	3.1870	1.6751
CP to QN ↑	0.0877	0.0549	5.9230	2.9068
RN to QN ↑	0.0798	0.0793	5.9068	2.9017
	X17_P0	X33_P0	X17_P0	X33_P0
CP to QN ↓	0.0682	0.0720	0.8455	0.4458
CP to QN ↑	0.0578	0.0626	1.4686	0.7513
RN to QN ↑	0.0778	0.0850	1.4746	0.7545

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1162	0.0794	0.0794	0.0794
CP ↑	min_pulse_width to CP	0.0530	0.0311	0.0359	0.0358
D ↓	hold_rising to CP	-0.1258	-0.0628	-0.0628	-0.0628
D ↑	hold_rising to CP	-0.0598	-0.0215	-0.0190	-0.0190
D ↓	setup_rising to CP	0.1751	0.1097	0.1097	0.1097
D ↑	setup_rising to CP	0.0947	0.0512	0.0512	0.0512
E ↓	hold_rising to CP	-0.0720	-0.0716	-0.0720	-0.0720
E ↑	hold_rising to CP	-0.0579	-0.0215	-0.0215	-0.0215
E ↓	setup_rising to CP	0.1455	0.1437	0.1434	0.1434
E ↑	setup_rising to CP	0.1635	0.1098	0.1098	0.1098
RN ↓	min_pulse_width to RN	0.0703	0.0708	0.0774	0.0850
RN ↑	recovery_rising to CP	0.0226	0.0223	0.0201	0.0201
RN ↑	removal_rising to CP	-0.0122	-0.0073	-0.0074	-0.0074
TE ↓	hold_rising to CP	-0.0522	-0.0406	-0.0406	-0.0406
TE ↑	hold_rising to CP	-0.0380	-0.0234	-0.0237	-0.0237
TE ↓	setup_rising to CP	0.1149	0.0898	0.0898	0.0898
TE ↑	setup_rising to CP	0.2002	0.1391	0.1391	0.1391
TI ↓	hold_rising to CP	-0.1514	-0.0789	-0.0789	-0.0789
TI ↑	hold_rising to CP	-0.0457	-0.0263	-0.0223	-0.0223
TI ↓	setup_rising to CP	0.2007	0.1299	0.1299	0.1299
TI ↑	setup_rising to CP	0.0795	0.0575	0.0573	0.0573

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	2.085e-06	9.677e-12
X8_P0	2.257e-06	9.333e-12
X17_P0	2.742e-06	9.585e-12
X33_P0	3.362e-06	1.009e-11

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

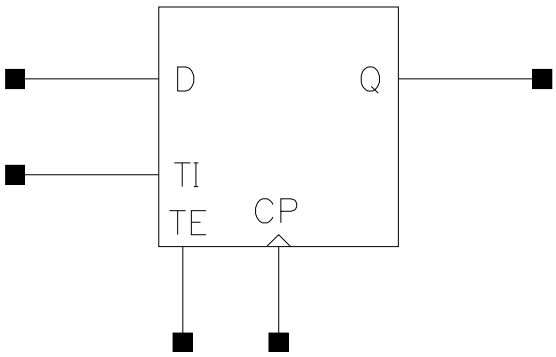
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	4.295e-03	4.326e-03	4.332e-03	4.335e-03
Clock 100Mhz Data 25Mhz	6.988e-03	7.194e-03	7.780e-03	8.545e-03
Clock 100Mhz Data 50Mhz	9.682e-03	1.006e-02	1.123e-02	1.275e-02
Clock = 0 Data 100Mhz	6.168e-03	5.993e-03	5.935e-03	5.907e-03
Clock = 1 Data 100Mhz	2.401e-03	2.430e-03	2.441e-03	2.446e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.400	4.0800
X8_P0	1.200	3.128	3.7536
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0642	0.0389	3.6166	1.7425
CP to Q ↑	0.0558	0.0482	6.0684	2.9480
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0577	0.0629	0.8282	0.4373
CP to Q ↑	0.0821	0.0864	1.4654	0.7488

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1017	0.1061	0.1061	0.1061
CP ↑	min_pulse_width to CP	0.0493	0.0311	0.0300	0.0300
D ↓	hold_rising to CP	-0.0769	-0.0308	-0.0339	-0.0339
D ↑	hold_rising to CP	-0.0234	-0.0019	-0.0019	-0.0019
D ↓	setup_rising to CP	0.1114	0.0755	0.0755	0.0755
D ↑	setup_rising to CP	0.0504	0.0261	0.0261	0.0261
TE ↓	hold_rising to CP	-0.0402	-0.0259	-0.0259	-0.0259
TE ↑	hold_rising to CP	-0.0304	-0.0163	-0.0163	-0.0163
TE ↓	setup_rising to CP	0.0947	0.0734	0.0734	0.0734
TE ↑	setup_rising to CP	0.1760	0.1391	0.1391	0.1391
TI ↓	hold_rising to CP	-0.1451	-0.0907	-0.0902	-0.0902
TI ↑	hold_rising to CP	-0.0345	-0.0177	-0.0177	-0.0177
TI ↓	setup_rising to CP	0.1848	0.1400	0.1400	0.1400
TI ↑	setup_rising to CP	0.0649	0.0476	0.0476	0.0476

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.592e-06	7.064e-12
X8_P0	1.796e-06	6.560e-12
X17_P0	2.490e-06	7.316e-12
X33_P0	3.004e-06	7.820e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

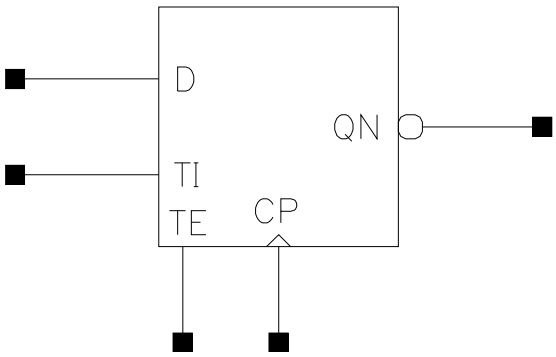
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.841e-03	3.862e-03	3.866e-03	3.868e-03
Clock 100Mhz Data 25Mhz	5.740e-03	5.825e-03	6.487e-03	7.113e-03
Clock 100Mhz Data 50Mhz	7.639e-03	7.789e-03	9.108e-03	1.036e-02
Clock = 0 Data 100Mhz	4.859e-03	4.585e-03	4.495e-03	4.450e-03
Clock = 1 Data 100Mhz	1.369e-03	7.218e-04	5.062e-04	3.985e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.536	4.2432
X8_P0	1.200	3.264	3.9168
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0717	0.0750	3.6543	1.7304
CP to QN ↑	0.0706	0.0502	6.0371	2.9137
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0581	0.0636	0.8287	0.4374
CP to QN ↑	0.0503	0.0548	1.4658	0.7486

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1011	0.1061	0.1061	0.1061
CP ↑	min_pulse_width to CP	0.0396	0.0300	0.0311	0.0311
D ↓	hold_rising to CP	-0.0769	-0.0339	-0.0308	-0.0308
D ↑	hold_rising to CP	-0.0234	-0.0019	-0.0019	-0.0019
D ↓	setup_rising to CP	0.1114	0.0755	0.0755	0.0755
D ↑	setup_rising to CP	0.0501	0.0261	0.0261	0.0261
TE ↓	hold_rising to CP	-0.0402	-0.0259	-0.0259	-0.0259
TE ↑	hold_rising to CP	-0.0304	-0.0163	-0.0163	-0.0163
TE ↓	setup_rising to CP	0.0947	0.0734	0.0734	0.0734
TE ↑	setup_rising to CP	0.1733	0.1391	0.1422	0.1391
TI ↓	hold_rising to CP	-0.1451	-0.0902	-0.0907	-0.0907
TI ↑	hold_rising to CP	-0.0345	-0.0177	-0.0177	-0.0177
TI ↓	setup_rising to CP	0.1812	0.1400	0.1394	0.1400
TI ↑	setup_rising to CP	0.0647	0.0476	0.0476	0.0476

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.624e-06	7.317e-12
X8_P0	1.822e-06	6.812e-12
X17_P0	2.455e-06	7.316e-12
X33_P0	2.969e-06	7.820e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

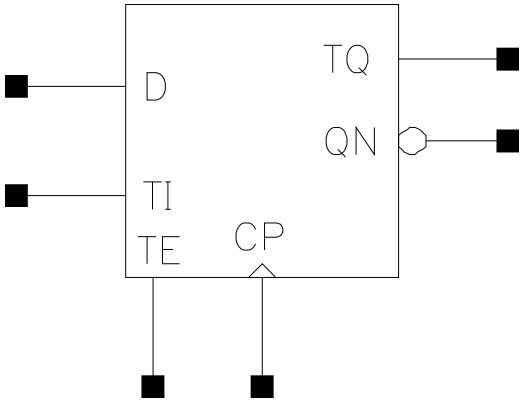
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.802e-03	3.868e-03	3.888e-03	3.899e-03
Clock 100Mhz Data 25Mhz	5.745e-03	5.931e-03	6.468e-03	7.095e-03
Clock 100Mhz Data 50Mhz	7.687e-03	7.995e-03	9.047e-03	1.029e-02
Clock = 0 Data 100Mhz	4.881e-03	4.601e-03	4.508e-03	4.462e-03
Clock = 1 Data 100Mhz	1.361e-03	7.312e-04	5.215e-04	4.166e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.536	4.2432
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0012	0.0008	0.0008	0.0008
D	0.0008	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0788	0.0674	3.2970	1.6892
CP to QN ↑	0.0852	0.0528	5.9795	2.9373
CP to TQ ↓	0.0598	0.0361	4.5663	3.1892
CP to TQ ↑	0.0574	0.0480	11.2905	8.0739
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0638	0.0686	0.8500	0.4480
CP to QN ↑	0.0541	0.0577	1.4886	0.7658
CP to TQ ↓	0.0376	0.0391	4.2353	4.2483
CP to TQ ↑	0.0487	0.0500	10.5140	11.1350

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1017	0.1061	0.1061	0.1061
CP ↑	min_pulse_width to CP	0.0493	0.0311	0.0311	0.0311
D ↓	hold_rising to CP	-0.0769	-0.0311	-0.0311	-0.0311
D ↑	hold_rising to CP	-0.0234	-0.0019	-0.0019	-0.0019
D ↓	setup_rising to CP	0.1114	0.0755	0.0730	0.0755
D ↑	setup_rising to CP	0.0508	0.0261	0.0261	0.0261
TE ↓	hold_rising to CP	-0.0402	-0.0259	-0.0259	-0.0259
TE ↑	hold_rising to CP	-0.0304	-0.0163	-0.0163	-0.0163
TE ↓	setup_rising to CP	0.0947	0.0734	0.0734	0.0734
TE ↑	setup_rising to CP	0.1733	0.1391	0.1391	0.1391
TI ↓	hold_rising to CP	-0.1411	-0.0907	-0.0907	-0.0907
TI ↑	hold_rising to CP	-0.0345	-0.0177	-0.0177	-0.0177
TI ↓	setup_rising to CP	0.1812	0.1400	0.1400	0.1400
TI ↑	setup_rising to CP	0.0649	0.0476	0.0476	0.0476

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.795e-06	7.834e-12
X8_P0	2.015e-06	7.316e-12
X17_P0	2.350e-06	7.568e-12
X33_P0	2.961e-06	8.072e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0

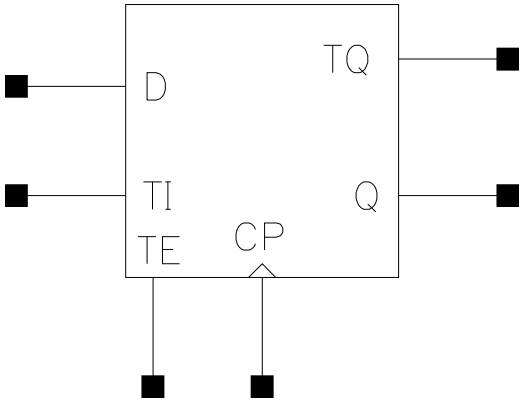
Clock 100Mhz Data 0Mhz	3.917e-03	3.903e-03	3.896e-03	3.896e-03
Clock 100Mhz Data 25Mhz	6.044e-03	6.203e-03	6.467e-03	7.174e-03
Clock 100Mhz Data 50Mhz	8.171e-03	8.502e-03	9.038e-03	1.045e-02
Clock = 0 Data 100Mhz	4.872e-03	4.598e-03	4.506e-03	4.460e-03
Clock = 1 Data 100Mhz	1.368e-03	7.112e-04	4.921e-04	3.826e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.400	4.0800
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0008	0.0007	0.0007	0.0007

TE	0.0008	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0841	0.0436	3.8341	1.7358
CP to Q ↑	0.0635	0.0510	6.1546	2.9711
CP to TQ ↓	0.0817	0.0460	3.8126	4.3646
CP to TQ ↑	0.0651	0.0560	8.1561	11.3231
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0591	0.0645	0.8547	0.4475
CP to Q ↑	0.0835	0.0878	1.4997	0.7537
CP to TQ ↓	0.0616	0.0681	4.1534	4.2348
CP to TQ ↑	0.0883	0.0943	10.8868	11.0151

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1017	0.1061	0.1061	0.1061
CP ↑	min_pulse_width to CP	0.0723	0.0348	0.0300	0.0300
D ↓	hold_rising to CP	-0.0769	-0.0311	-0.0339	-0.0339
D ↑	hold_rising to CP	-0.0234	-0.0019	-0.0019	-0.0019
D ↓	setup_rising to CP	0.1114	0.0755	0.0755	0.0755
D ↑	setup_rising to CP	0.0501	0.0261	0.0261	0.0261
TE ↓	hold_rising to CP	-0.0402	-0.0259	-0.0259	-0.0259
TE ↑	hold_rising to CP	-0.0304	-0.0163	-0.0163	-0.0163
TE ↓	setup_rising to CP	0.0947	0.0734	0.0734	0.0734
TE ↑	setup_rising to CP	0.1760	0.1391	0.1391	0.1391
TI ↓	hold_rising to CP	-0.1451	-0.0907	-0.0902	-0.0902
TI ↑	hold_rising to CP	-0.0345	-0.0177	-0.0177	-0.0177
TI ↓	setup_rising to CP	0.1848	0.1400	0.1400	0.1400
TI ↑	setup_rising to CP	0.0649	0.0476	0.0476	0.0476

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.781e-06	7.568e-12
X8_P0	1.918e-06	7.064e-12
X17_P0	2.577e-06	7.568e-12
X33_P0	3.087e-06	8.072e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

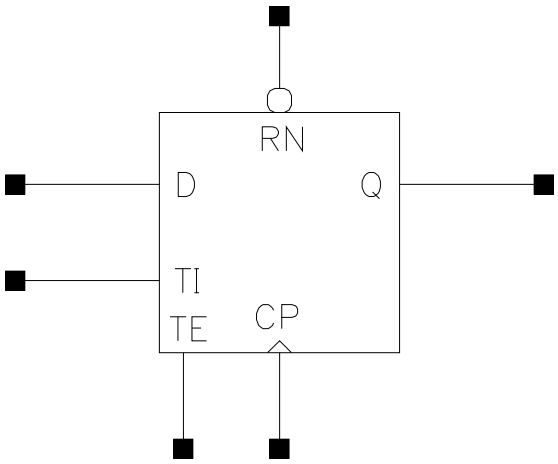
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.825e-03	3.855e-03	3.861e-03	3.865e-03
Clock 100Mhz Data 25Mhz	6.049e-03	6.040e-03	6.676e-03	7.342e-03
Clock 100Mhz Data 50Mhz	8.272e-03	8.225e-03	9.491e-03	1.082e-02
Clock = 0 Data 100Mhz	4.852e-03	4.580e-03	4.492e-03	4.448e-03
Clock = 1 Data 100Mhz	1.358e-03	7.062e-04	4.889e-04	3.803e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.672	4.4064
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
RN	0.0008	0.0007	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0773	0.0416	3.9081	1.7446
CP to Q ↑	0.0615	0.0518	6.0686	2.9893
RN to Q ↓	0.0652	0.0557	3.3097	1.8225
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0606	0.0662	0.8387	0.4444
CP to Q ↑	0.0757	0.0799	1.4649	0.7481
RN to Q ↓	0.0840	0.0897	0.8368	0.4433

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1132	0.1103	0.1109	0.1109
CP ↑	min_pulse_width to CP	0.0637	0.0311	0.0311	0.0311
D ↓	hold_rising to CP	-0.0672	-0.0210	-0.0241	-0.0241
D ↑	hold_rising to CP	-0.0283	-0.0038	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1114	0.0706	0.0734	0.0734
D ↑	setup_rising to CP	0.0606	0.0366	0.0366	0.0366
RN ↓	min_pulse_width to RN	0.0703	0.0730	0.0686	0.0686
RN ↑	recovery_rising to CP	0.0223	0.0223	0.0226	0.0226
RN ↑	removal_rising to CP	-0.0122	-0.0104	-0.0104	-0.0104
TE ↓	hold_rising to CP	-0.0451	-0.0188	-0.0188	-0.0188
TE ↑	hold_rising to CP	-0.0383	-0.0212	-0.0237	-0.0237
TE ↓	setup_rising to CP	0.0947	0.0682	0.0682	0.0682
TE ↑	setup_rising to CP	0.1733	0.1342	0.1373	0.1373
TI ↓	hold_rising to CP	-0.1304	-0.0761	-0.0756	-0.0756
TI ↑	hold_rising to CP	-0.0449	-0.0241	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.1812	0.1353	0.1351	0.1351
TI ↑	setup_rising to CP	0.0762	0.0574	0.0589	0.0589

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.788e-06	8.073e-12
X8_P0	1.930e-06	7.569e-12
X17_P0	2.563e-06	8.325e-12
X33_P0	3.054e-06	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	4.296e-03	4.333e-03	4.365e-03	4.382e-03

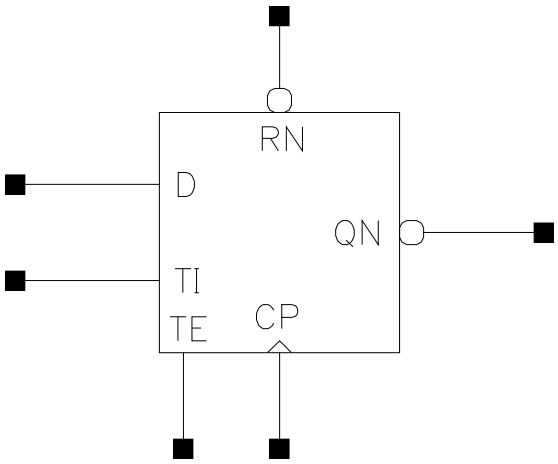
Clock 100Mhz Data 25Mhz	6.466e-03	6.454e-03	7.240e-03	7.915e-03
Clock 100Mhz Data 50Mhz	8.636e-03	8.574e-03	1.011e-02	1.145e-02
Clock = 0 Data 100Mhz	5.014e-03	4.658e-03	4.542e-03	4.484e-03
Clock = 1 Data 100Mhz	1.394e-03	7.629e-04	5.528e-04	4.476e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	3.944	4.7328
X33_P0	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0695	0.0639	3.1062	1.6309
CP to QN ↑	0.0803	0.0496	5.9269	2.8931
RN to QN ↑	0.0741	0.0747	5.9087	2.8894
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0630	0.0688	0.8383	0.4437
CP to QN ↑	0.0551	0.0601	1.4787	0.7584
RN to QN ↑	0.0754	0.0820	1.4825	0.7605

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1132	0.1103	0.1103	0.1103
CP ↑	min_pulse_width to CP	0.0492	0.0311	0.0348	0.0359
D ↓	hold_rising to CP	-0.0672	-0.0241	-0.0210	-0.0210
D ↑	hold_rising to CP	-0.0283	-0.0068	-0.0038	-0.0038
D ↓	setup_rising to CP	0.1114	0.0706	0.0734	0.0734
D ↑	setup_rising to CP	0.0606	0.0366	0.0366	0.0366
RN ↓	min_pulse_width to RN	0.0681	0.0686	0.0774	0.0823
RN ↑	recovery_rising to CP	0.0223	0.0219	0.0219	0.0219
RN ↑	removal_rising to CP	-0.0122	-0.0126	-0.0129	-0.0129
TE ↓	hold_rising to CP	-0.0451	-0.0188	-0.0188	-0.0188
TE ↑	hold_rising to CP	-0.0383	-0.0237	-0.0212	-0.0237
TE ↓	setup_rising to CP	0.0947	0.0682	0.0682	0.0682
TE ↑	setup_rising to CP	0.1733	0.1342	0.1373	0.1373
TI ↓	hold_rising to CP	-0.1319	-0.0761	-0.0756	-0.0761
TI ↑	hold_rising to CP	-0.0449	-0.0241	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.1812	0.1353	0.1351	0.1351
TI ↑	setup_rising to CP	0.0762	0.0574	0.0574	0.0589

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.871e-06	8.167e-12
X8_P0	2.004e-06	7.821e-12
X17_P0	2.577e-06	8.073e-12
X33_P0	3.098e-06	8.577e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	4.242e-03	4.244e-03	4.244e-03	4.243e-03

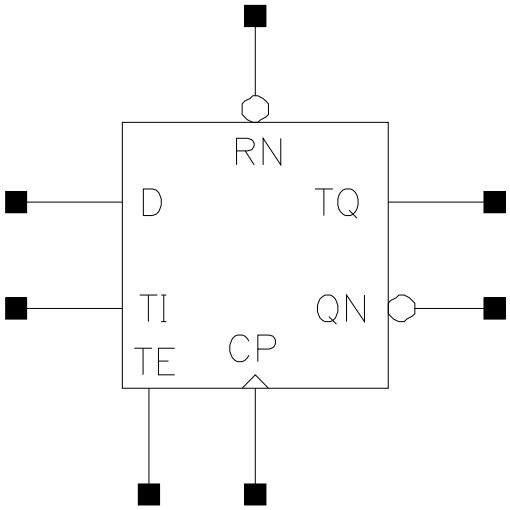
Clock 100Mhz Data 25Mhz	6.366e-03	6.421e-03	7.018e-03	7.632e-03
Clock 100Mhz Data 50Mhz	8.490e-03	8.597e-03	9.792e-03	1.102e-02
Clock = 0 Data 100Mhz	5.023e-03	4.666e-03	4.553e-03	4.497e-03
Clock = 1 Data 100Mhz	1.393e-03	7.366e-04	5.180e-04	4.088e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006

RN	0.0010	0.0007	0.0008	0.0008
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0772	0.0662	3.1138	1.7199
CP to QN ↑	0.1041	0.0556	5.3121	3.0146
CP to TQ ↓	0.0743	0.0384	4.1194	3.2957
CP to TQ ↑	0.0639	0.0525	9.1840	8.4954
RN to QN ↑	0.0731	0.0728	5.3612	3.0098
RN to TQ ↓	0.0509	0.0502	3.6527	3.4557
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0682	0.0732	0.8578	0.4553
CP to QN ↑	0.0561	0.0588	1.5129	0.7618
CP to TQ ↓	0.0399	0.0413	4.1387	4.0537
CP to TQ ↑	0.0524	0.0536	7.9841	8.1165
RN to QN ↑	0.0748	0.0790	1.5116	0.7614
RN to TQ ↓	0.0533	0.0556	4.3024	4.2301

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1132	0.1103	0.1109	0.1109
CP ↑	min_pulse_width to CP	0.0686	0.0311	0.0311	0.0348
D ↓	hold_rising to CP	-0.0672	-0.0210	-0.0210	-0.0210
D ↑	hold_rising to CP	-0.0283	-0.0038	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1114	0.0706	0.0734	0.0734
D ↑	setup_rising to CP	0.0606	0.0366	0.0366	0.0366
RN ↓	min_pulse_width to RN	0.0703	0.0703	0.0752	0.0774
RN ↑	recovery_rising to CP	0.0219	0.0219	0.0223	0.0223
RN ↑	removal_rising to CP	-0.0175	-0.0104	-0.0104	-0.0104
TE ↓	hold_rising to CP	-0.0451	-0.0188	-0.0188	-0.0188
TE ↑	hold_rising to CP	-0.0383	-0.0237	-0.0237	-0.0237
TE ↓	setup_rising to CP	0.0947	0.0682	0.0682	0.0682
TE ↑	setup_rising to CP	0.1733	0.1342	0.1342	0.1342
TI ↓	hold_rising to CP	-0.1304	-0.0761	-0.0756	-0.0761
TI ↑	hold_rising to CP	-0.0449	-0.0241	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.1812	0.1353	0.1351	0.1351
TI ↑	setup_rising to CP	0.0762	0.0574	0.0589	0.0589

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.999e-06	8.325e-12
X8_P0	2.120e-06	7.821e-12
X17_P0	2.497e-06	8.325e-12
X33_P0	3.099e-06	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

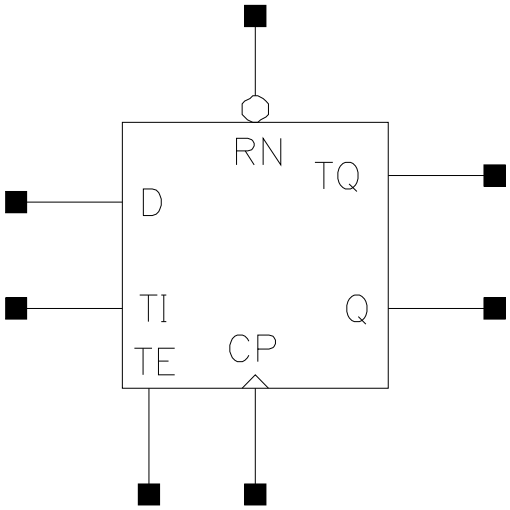
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	4.258e-03	4.282e-03	4.312e-03	4.327e-03
Clock 100Mhz Data 25Mhz	6.599e-03	6.618e-03	6.963e-03	7.705e-03
Clock 100Mhz Data 50Mhz	8.940e-03	8.955e-03	9.615e-03	1.108e-02
Clock = 0 Data 100Mhz	5.006e-03	4.653e-03	4.534e-03	4.475e-03
Clock = 1 Data 100Mhz	1.392e-03	7.526e-04	5.394e-04	4.328e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0008	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006

RN	0.0008	0.0008	0.0007	0.0007
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0870	0.0452	4.1739	1.8025
CP to Q ↑	0.0654	0.0540	6.3194	3.1020
CP to TQ ↓	0.0840	0.0459	5.2098	4.4144
CP to TQ ↑	0.0675	0.0567	12.3895	11.2607
RN to Q ↓	0.0674	0.0629	3.5079	1.8853
RN to TQ ↓	0.0665	0.0633	4.4894	4.5794
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0630	0.0685	0.8518	0.4520
CP to Q ↑	0.0768	0.0808	1.4721	0.7520
CP to TQ ↓	0.0656	0.0728	4.1862	4.2654
CP to TQ ↑	0.0814	0.0879	11.0203	11.0829
RN to Q ↓	0.0864	0.0919	0.8492	0.4505
RN to TQ ↓	0.0891	0.0962	4.1839	4.2628

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1132	0.1103	0.1103	0.1103
CP ↑	min_pulse_width to CP	0.0734	0.0348	0.0311	0.0311
D ↓	hold_rising to CP	-0.0672	-0.0210	-0.0241	-0.0241
D ↑	hold_rising to CP	-0.0283	-0.0038	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1114	0.0706	0.0737	0.0737
D ↑	setup_rising to CP	0.0606	0.0366	0.0366	0.0366
RN ↓	min_pulse_width to RN	0.0703	0.0801	0.0659	0.0659
RN ↑	recovery_rising to CP	0.0226	0.0219	0.0219	0.0219
RN ↑	removal_rising to CP	-0.0122	-0.0126	-0.0104	-0.0104
TE ↓	hold_rising to CP	-0.0451	-0.0188	-0.0188	-0.0188
TE ↑	hold_rising to CP	-0.0383	-0.0212	-0.0237	-0.0237
TE ↓	setup_rising to CP	0.0947	0.0682	0.0682	0.0682
TE ↑	setup_rising to CP	0.1733	0.1342	0.1342	0.1342
TI ↓	hold_rising to CP	-0.1304	-0.0761	-0.0761	-0.0761
TI ↑	hold_rising to CP	-0.0449	-0.0241	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.1812	0.1353	0.1353	0.1353
TI ↑	setup_rising to CP	0.0762	0.0574	0.0574	0.0574

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.849e-06	8.325e-12
X8_P0	2.013e-06	7.821e-12
X17_P0	2.602e-06	8.325e-12
X33_P0	3.094e-06	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

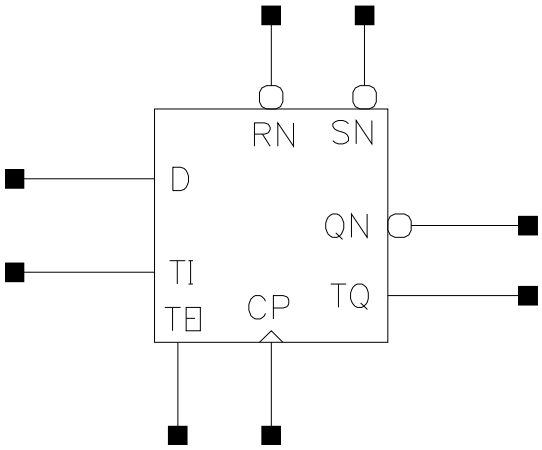
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	4.293e-03	4.331e-03	4.343e-03	4.349e-03
Clock 100Mhz Data 25Mhz	6.606e-03	6.598e-03	7.405e-03	8.080e-03
Clock 100Mhz Data 50Mhz	8.920e-03	8.865e-03	1.047e-02	1.181e-02
Clock = 0 Data 100Mhz	5.010e-03	4.657e-03	4.539e-03	4.480e-03
Clock = 1 Data 100Mhz	1.394e-03	7.246e-04	5.016e-04	3.902e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.352	5.2224
X17_P0	1.200	4.488	5.3856
X33_P0	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0008

SN	0.0012	0.0012	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0734	0.0777	1.6676	0.8630
CP to QN ↑	0.0587	0.0611	2.9119	1.4753
CP to TQ ↓	0.0451	0.0450	5.1942	5.1975
CP to TQ ↑	0.0609	0.0610	14.2693	14.2915
RN to QN ↓	0.0806	0.0848	1.6665	0.8631
RN to QN ↑	0.0816	0.0851	2.9158	1.4789
RN to TQ ↓	0.0626	0.0624	5.5836	5.5908
RN to TQ ↑	0.0684	0.0684	14.2530	14.2637
SN to QN ↓	0.0858	0.0909	1.6758	0.8662
SN to TQ ↑	0.0717	0.0716	14.4051	14.4120
	X33_P0		**X33_P0**	
CP to QN ↓	0.0883		0.4625	
CP to QN ↑	0.0670		0.7568	
CP to TQ ↓	0.0451		5.2095	
CP to TQ ↑	0.0612		14.3145	
RN to QN ↓	0.0951		0.4623	
RN to QN ↑	0.0930		0.7577	
RN to TQ ↓	0.0623		5.6002	
RN to TQ ↑	0.0686		14.2954	
SN to QN ↓	0.1026		0.4624	
SN to TQ ↑	0.0717		14.4741	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1157	0.1157	0.1157
CP ↑	min_pulse_width to CP	0.0359	0.0359	0.0358
D ↓	hold_rising to CP	-0.0241	-0.0241	-0.0241
D ↑	hold_rising to CP	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.0755	0.0755	0.0755
D ↑	setup_rising to CP	0.0366	0.0366	0.0366
RN ↓	min_pulse_width to RN	0.0774	0.0823	0.0872
RN ↑	non_seq_hold_rising to SN	-0.0282	-0.0282	-0.0282
RN ↑	non_seq_setup_rising to SN	0.0691	0.0691	0.0691
RN ↑	recovery_rising to CP	0.0320	0.0320	0.0320
RN ↑	removal_rising to CP	-0.0196	-0.0196	-0.0196
SN ↓	min_pulse_width to SN	0.0642	0.0669	0.0696
SN ↑	recovery_rising to CP	0.0104	0.0104	0.0103
SN ↑	removal_rising to CP	0.0290	0.0290	0.0290

TE ↓	hold_rising to CP	-0.0188	-0.0188	-0.0188
TE ↑	hold_rising to CP	-0.0237	-0.0237	-0.0237
TE ↓	setup_rising to CP	0.0730	0.0730	0.0730
TE ↑	setup_rising to CP	0.1391	0.1391	0.1391
TI ↓	hold_rising to CP	-0.0761	-0.0761	-0.0761
TI ↑	hold_rising to CP	-0.0241	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.1401	0.1401	0.1401
TI ↑	setup_rising to CP	0.0589	0.0589	0.0589

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	2.361e-06	8.856e-12
X17_P0	2.662e-06	9.107e-12
X33_P0	3.185e-06	9.611e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

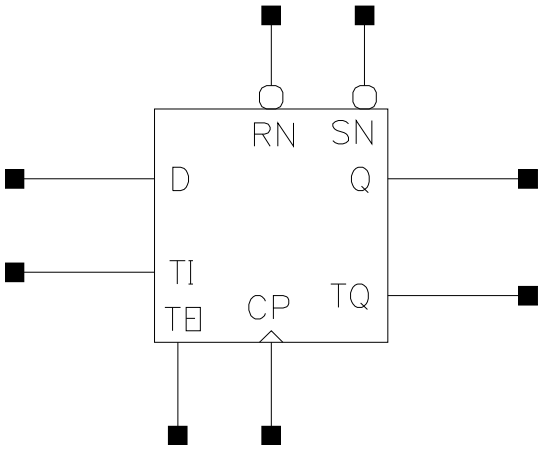
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	4.568e-03	4.568e-03	4.569e-03
Clock 100Mhz Data 25Mhz	6.961e-03	7.255e-03	8.000e-03
Clock 100Mhz Data 50Mhz	9.354e-03	9.943e-03	1.143e-02
Clock = 0 Data 100Mhz	4.492e-03	4.491e-03	4.492e-03
Clock = 1 Data 100Mhz	1.314e-04	1.312e-04	1.313e-04

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.216	5.0592
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0008

SN	0.0013	0.0013	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0495	0.0552	1.7441	0.9107
CP to Q ↑	0.0592	0.0617	2.9774	1.5173
CP to TQ ↓	0.0512	0.0582	5.2863	5.3580
CP to TQ ↑	0.0650	0.0710	14.1556	14.2562
RN to Q ↓	0.0711	0.0811	1.9723	1.0337
RN to Q ↑	0.0524	0.0580	3.0787	1.5757
RN to TQ ↓	0.0726	0.0839	5.7366	5.8738
RN to TQ ↑	0.0618	0.0726	14.2860	14.3882
SN to Q ↑	0.0710	0.0763	3.0757	1.5728
SN to TQ ↑	0.0803	0.0909	14.2803	14.3876
	X33_P0		**X33_P0**	
CP to Q ↓	0.0696		0.4948	
CP to Q ↑	0.0693		0.7885	
CP to TQ ↓	0.0705		5.5735	
CP to TQ ↑	0.0822		14.4275	
RN to Q ↓	0.1059		0.5709	
RN to Q ↑	0.0728		0.8257	
RN to TQ ↓	0.1043		6.2417	
RN to TQ ↑	0.0933		14.5828	
SN to Q ↑	0.0908		0.8257	
SN to TQ ↑	0.1113		14.5904	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1157	0.1157	0.1157
CP ↑	min_pulse_width to CP	0.0396	0.0444	0.0589
D ↓	hold_rising to CP	-0.0241	-0.0210	-0.0213
D ↑	hold_rising to CP	-0.0068	-0.0038	-0.0038
D ↓	setup_rising to CP	0.0755	0.0755	0.0755
D ↑	setup_rising to CP	0.0366	0.0366	0.0366
RN ↓	min_pulse_width to RN	0.0850	0.0996	0.1262
RN ↑	non_seq_hold_rising to SN	-0.0309	-0.0381	-0.0479
RN ↑	non_seq_setup_rising to SN	0.0641	0.0641	0.0767
RN ↑	recovery_rising to CP	0.0268	0.0268	0.0268
RN ↑	removal_rising to CP	-0.0178	-0.0178	-0.0178
SN ↓	min_pulse_width to SN	0.0669	0.0745	0.0940
SN ↑	recovery_rising to CP	0.0103	0.0103	0.0103
SN ↑	removal_rising to CP	0.0290	0.0290	0.0290

TE ↓	hold_rising to CP	-0.0188	-0.0188	-0.0188
TE ↑	hold_rising to CP	-0.0237	-0.0212	-0.0212
TE ↓	setup_rising to CP	0.0730	0.0730	0.0730
TE ↑	setup_rising to CP	0.1391	0.1391	0.1391
TI ↓	hold_rising to CP	-0.0761	-0.0761	-0.0761
TI ↑	hold_rising to CP	-0.0241	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.1401	0.1401	0.1401
TI ↑	setup_rising to CP	0.0589	0.0589	0.0587

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P0	2.297e-06	8.595e-12
X17_P0	2.577e-06	8.814e-12
X33_P0	3.084e-06	9.350e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

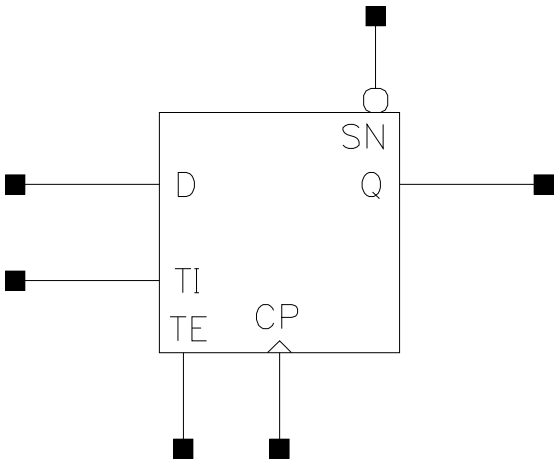
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	4.493e-03	4.493e-03	4.494e-03
Clock 100Mhz Data 25Mhz	6.796e-03	7.137e-03	8.020e-03
Clock 100Mhz Data 50Mhz	9.100e-03	9.781e-03	1.155e-02
Clock = 0 Data 100Mhz	4.488e-03	4.488e-03	4.488e-03
Clock = 1 Data 100Mhz	1.189e-04	1.188e-04	1.190e-04

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004
SN	0.0013	0.0013	0.0013	0.0013
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0009			
D	0.0004			
SN	0.0013			
TE	0.0010			
TI	0.0004			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
CP to Q ↓	0.0777	0.0435	3.9255	1.7318
CP to Q ↑	0.0640	0.0545	6.1237	2.9676
SN to Q ↑	0.0502	0.0570	5.9872	2.9650
	X17_P0	X25_P0	X17_P0	X25_P0
CP to Q ↓	0.0604	0.0633	0.8401	0.5848
CP to Q ↑	0.0765	0.0787	1.4644	0.9951
SN to Q ↑	0.0789	0.0810	1.4647	0.9954
	X33_P0		X33_P0	
CP to Q ↓	0.0655		0.4455	
CP to Q ↑	0.0801		0.7482	
SN to Q ↑	0.0824		0.7490	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.1162	0.1157	0.1157	0.1157
CP ↑	min_pulse_width to CP	0.0638	0.0348	0.0300	0.0300
D ↓	hold_rising to CP	-0.0669	-0.0262	-0.0259	-0.0259
D ↑	hold_rising to CP	-0.0255	-0.0016	-0.0016	-0.0016
D ↓	setup_rising to CP	0.1166	0.0782	0.0782	0.0782
D ↑	setup_rising to CP	0.0557	0.0317	0.0317	0.0317
SN ↓	min_pulse_width to SN	0.0447	0.0544	0.0518	0.0518
SN ↑	recovery_rising to CP	0.0103	0.0103	0.0103	0.0103
SN ↑	removal_rising to CP	0.0211	0.0290	0.0290	0.0290
TE ↓	hold_rising to CP	-0.0454	-0.0241	-0.0237	-0.0237
TE ↑	hold_rising to CP	-0.0356	-0.0184	-0.0215	-0.0215
TE ↓	setup_rising to CP	0.1003	0.0730	0.0730	0.0730
TE ↑	setup_rising to CP	0.1785	0.1447	0.1447	0.1447
TI ↓	hold_rising to CP	-0.1319	-0.0810	-0.0805	-0.0805
TI ↑	hold_rising to CP	-0.0399	-0.0187	-0.0187	-0.0187
TI ↓	setup_rising to CP	0.1846	0.1394	0.1394	0.1394
TI ↑	setup_rising to CP	0.0711	0.0525	0.0525	0.0525
		X33_P0			

CP ↓	min_pulse_width to CP	0.1157			
CP ↑	min_pulse_width to CP	0.0300			
D ↓	hold_rising to CP	-0.0259			
D ↑	hold_rising to CP	-0.0016			
D ↓	setup_rising to CP	0.0782			
D ↑	setup_rising to CP	0.0317			
SN ↓	min_pulse_width to SN	0.0518			
SN ↑	recovery_rising to CP	0.0103			
SN ↑	removal_rising to CP	0.0290			
TE ↓	hold_rising to CP	-0.0237			
TE ↑	hold_rising to CP	-0.0215			
TE ↓	setup_rising to CP	0.0730			
TE ↑	setup_rising to CP	0.1447			
TI ↓	hold_rising to CP	-0.0805			
TI ↑	hold_rising to CP	-0.0187			
TI ↓	setup_rising to CP	0.1394			
TI ↑	setup_rising to CP	0.0525			

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.871e-06	8.073e-12
X8_P0	2.054e-06	7.821e-12
X17_P0	2.628e-06	8.325e-12
X25_P0	2.890e-06	8.577e-12
X33_P0	3.149e-06	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	4.168e-03	4.252e-03	4.279e-03	4.292e-03
Clock 100Mhz Data 25Mhz	6.322e-03	6.442e-03	7.177e-03	7.533e-03
Clock 100Mhz Data 50Mhz	8.475e-03	8.632e-03	1.008e-02	1.077e-02
Clock = 0 Data 100Mhz	4.860e-03	4.599e-03	4.513e-03	4.470e-03
Clock = 1 Data 100Mhz	1.394e-03	7.383e-04	5.200e-04	4.108e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	4.300e-03			

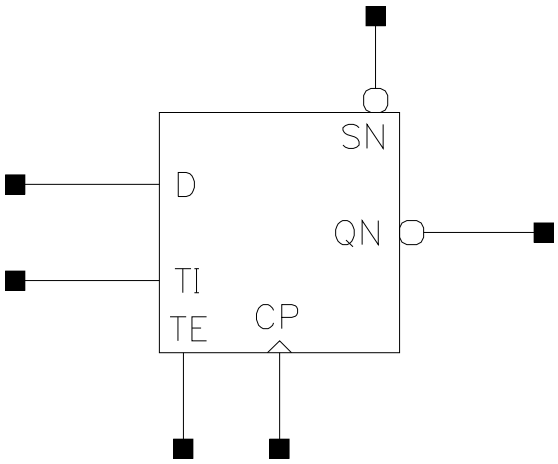
Clock 100Mhz Data 25Mhz	7.810e-03			
Clock 100Mhz Data 50Mhz	1.132e-02			
Clock = 0 Data 100Mhz	4.444e-03			
Clock = 1 Data 100Mhz	3.453e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004
SN	0.0014	0.0013	0.0013	0.0013
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0009			
D	0.0004			
SN	0.0013			
TE	0.0010			
TI	0.0004			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0725	0.0648	3.1064	1.6323
CP to QN ↑	0.0810	0.0495	5.9167	2.9016
SN to QN ↓	0.0597	0.0670	3.0973	1.6325
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
CP to QN ↓	0.0676	0.0711	0.8428	0.5870
CP to QN ↑	0.0590	0.0621	1.4646	0.9961
SN to QN ↓	0.0708	0.0745	0.8430	0.5859
	X33_P0		**X33_P0**	
CP to QN ↓	0.0739		0.4470	
CP to QN ↑	0.0641		0.7499	
SN to QN ↓	0.0772		0.4467	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.1162	0.1157	0.1157	0.1157
CP ↑	min_pulse_width to CP	0.0493	0.0300	0.0349	0.0359
D ↓	hold_rising to CP	-0.0694	-0.0259	-0.0262	-0.0262
D ↑	hold_rising to CP	-0.0255	-0.0016	-0.0016	-0.0016
D ↓	setup_rising to CP	0.1166	0.0782	0.0782	0.0782
D ↑	setup_rising to CP	0.0557	0.0317	0.0317	0.0317
SN ↓	min_pulse_width to SN	0.0447	0.0518	0.0566	0.0566
SN ↑	recovery_rising to CP	0.0103	0.0103	0.0103	0.0103
SN ↑	removal_rising to CP	0.0211	0.0290	0.0290	0.0290
TE ↓	hold_rising to CP	-0.0454	-0.0237	-0.0241	-0.0241
TE ↑	hold_rising to CP	-0.0356	-0.0215	-0.0184	-0.0184
TE ↓	setup_rising to CP	0.1003	0.0730	0.0730	0.0730
TE ↑	setup_rising to CP	0.1785	0.1447	0.1447	0.1447
TI ↓	hold_rising to CP	-0.1314	-0.0805	-0.0810	-0.0810
TI ↑	hold_rising to CP	-0.0399	-0.0187	-0.0187	-0.0187
TI ↓	setup_rising to CP	0.1861	0.1394	0.1394	0.1394
TI ↑	setup_rising to CP	0.0711	0.0484	0.0525	0.0525
		X33_P0			

CP ↓	min_pulse_width to CP	0.1157			
CP ↑	min_pulse_width to CP	0.0359			
D ↓	hold_rising to CP	-0.0262			
D ↑	hold_rising to CP	-0.0016			
D ↓	setup_rising to CP	0.0782			
D ↑	setup_rising to CP	0.0317			
SN ↓	min_pulse_width to SN	0.0566			
SN ↑	recovery_rising to CP	0.0103			
SN ↑	removal_rising to CP	0.0290			
TE ↓	hold_rising to CP	-0.0241			
TE ↑	hold_rising to CP	-0.0184			
TE ↓	setup_rising to CP	0.0730			
TE ↑	setup_rising to CP	0.1447			
TI ↓	hold_rising to CP	-0.0810			
TI ↑	hold_rising to CP	-0.0187			
TI ↓	setup_rising to CP	0.1394			
TI ↑	setup_rising to CP	0.0525			

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.819e-06	8.073e-12
X8_P0	1.992e-06	7.821e-12
X17_P0	2.591e-06	8.325e-12
X25_P0	2.834e-06	8.577e-12
X33_P0	3.081e-06	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	4.154e-03	4.223e-03	4.242e-03	4.251e-03
Clock 100Mhz Data 25Mhz	6.240e-03	6.397e-03	7.132e-03	7.485e-03
Clock 100Mhz Data 50Mhz	8.325e-03	8.570e-03	1.002e-02	1.072e-02
Clock = 0 Data 100Mhz	4.860e-03	4.603e-03	4.515e-03	4.472e-03
Clock = 1 Data 100Mhz	1.394e-03	7.491e-04	5.341e-04	4.266e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	4.256e-03			

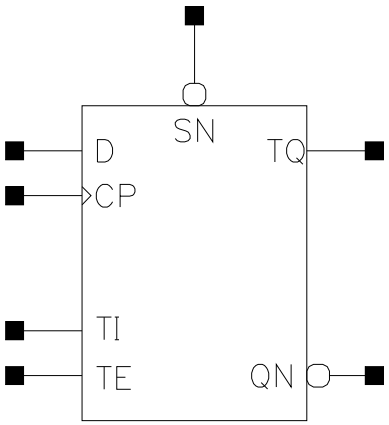
Clock 100Mhz Data 25Mhz	7.778e-03			
Clock 100Mhz Data 50Mhz	1.130e-02			
Clock = 0 Data 100Mhz	4.445e-03			
Clock = 1 Data 100Mhz	3.622e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.216	5.0592
X8_P0	1.200	4.080	4.8960
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004

SN	0.0015	0.0015	0.0014	0.0015
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0828	0.0676	3.0993	1.6420
CP to QN ↑	0.1049	0.0560	5.8437	2.9725
CP to TQ ↓	0.0755	0.0392	4.6683	3.8427
CP to TQ ↑	0.0640	0.0516	8.1334	7.9423
SN to QN ↓	0.0565	0.0538	3.0997	1.6418
SN to TQ ↑	0.0401	0.0391	8.0177	7.9225
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0674	0.0737	0.8664	0.4415
CP to QN ↑	0.0633	0.0689	1.4802	0.7552
CP to TQ ↓	0.0484	0.0482	4.0089	4.0097
CP to TQ ↑	0.0574	0.0573	7.9861	8.0064
SN to QN ↓	0.0589	0.0652	0.8669	0.4403
SN to TQ ↑	0.0485	0.0485	7.9810	8.0089

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1162	0.1157	0.1157	0.1157
CP ↑	min_pulse_width to CP	0.0686	0.0311	0.0396	0.0396
D ↓	hold_rising to CP	-0.0669	-0.0259	-0.0262	-0.0262
D ↑	hold_rising to CP	-0.0255	-0.0016	-0.0016	-0.0016
D ↓	setup_rising to CP	0.1166	0.0782	0.0782	0.0782
D ↑	setup_rising to CP	0.0557	0.0317	0.0317	0.0317
SN ↓	min_pulse_width to SN	0.0420	0.0447	0.0447	0.0474
SN ↑	recovery_rising to CP	0.0099	0.0106	0.0106	0.0106
SN ↑	removal_rising to CP	0.0211	0.0290	0.0290	0.0290
TE ↓	hold_rising to CP	-0.0454	-0.0237	-0.0241	-0.0241
TE ↑	hold_rising to CP	-0.0356	-0.0184	-0.0184	-0.0184
TE ↓	setup_rising to CP	0.1003	0.0730	0.0730	0.0730
TE ↑	setup_rising to CP	0.1785	0.1447	0.1443	0.1443
TI ↓	hold_rising to CP	-0.1319	-0.0805	-0.0810	-0.0810
TI ↑	hold_rising to CP	-0.0399	-0.0187	-0.0187	-0.0187
TI ↓	setup_rising to CP	0.1846	0.1394	0.1394	0.1394
TI ↑	setup_rising to CP	0.0747	0.0484	0.0525	0.0484

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	2.052e-06	8.577e-12
X8_P0	2.222e-06	8.325e-12
X17_P0	2.822e-06	8.829e-12
X33_P0	3.312e-06	9.333e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

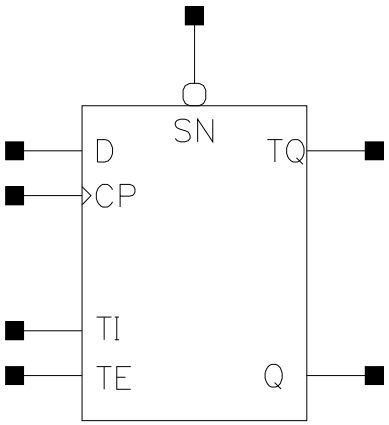
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	4.154e-03	4.256e-03	4.291e-03	4.308e-03
Clock 100Mhz Data 25Mhz	6.546e-03	6.654e-03	7.314e-03	7.973e-03
Clock 100Mhz Data 50Mhz	8.938e-03	9.051e-03	1.034e-02	1.164e-02
Clock = 0 Data 100Mhz	4.866e-03	4.605e-03	4.519e-03	4.475e-03
Clock = 1 Data 100Mhz	1.394e-03	7.266e-04	5.041e-04	3.929e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.944	4.7328
X17_P0	1.200	4.216	5.0592
X33_P0	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0004	0.0004	0.0004

SN	0.0015	0.0013	0.0013	0.0013
TE	0.0008	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0887	0.0467	4.0397	1.7749
CP to Q ↑	0.0678	0.0564	6.1578	3.0038
CP to TQ ↓	0.0884	0.0491	5.8267	4.4318
CP to TQ ↑	0.0669	0.0621	8.1922	11.3805
SN to Q ↑	0.0423	0.0592	5.9955	3.0049
SN to TQ ↑	0.0416	0.0657	8.0405	11.3639
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0614	0.0669	0.8640	0.4543
CP to Q ↑	0.0773	0.0812	1.4714	0.7515
CP to TQ ↓	0.0638	0.0711	4.1816	4.2567
CP to TQ ↑	0.0818	0.0880	11.0299	11.0900
SN to Q ↑	0.0796	0.0833	1.4723	0.7511
SN to TQ ↑	0.0841	0.0902	11.0254	11.0901

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1162	0.1157	0.1157	0.1157
CP ↑	min_pulse_width to CP	0.0772	0.0349	0.0300	0.0300
D ↓	hold_rising to CP	-0.0669	-0.0262	-0.0259	-0.0259
D ↑	hold_rising to CP	-0.0255	-0.0016	-0.0016	-0.0016
D ↓	setup_rising to CP	0.1166	0.0782	0.0782	0.0782
D ↑	setup_rising to CP	0.0557	0.0317	0.0317	0.0317
SN ↓	min_pulse_width to SN	0.0420	0.0593	0.0518	0.0518
SN ↑	recovery_rising to CP	0.0099	0.0103	0.0103	0.0103
SN ↑	removal_rising to CP	0.0211	0.0290	0.0290	0.0290
TE ↓	hold_rising to CP	-0.0454	-0.0241	-0.0237	-0.0237
TE ↑	hold_rising to CP	-0.0356	-0.0184	-0.0215	-0.0215
TE ↓	setup_rising to CP	0.1003	0.0730	0.0730	0.0730
TE ↑	setup_rising to CP	0.1785	0.1447	0.1447	0.1447
TI ↓	hold_rising to CP	-0.1319	-0.0810	-0.0805	-0.0805
TI ↑	hold_rising to CP	-0.0399	-0.0187	-0.0187	-0.0187
TI ↓	setup_rising to CP	0.1861	0.1394	0.1394	0.1394
TI ↑	setup_rising to CP	0.0747	0.0525	0.0525	0.0484

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	2.039e-06	8.324e-12
X8_P0	2.154e-06	8.073e-12
X17_P0	2.733e-06	8.577e-12
X33_P0	3.253e-06	9.059e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

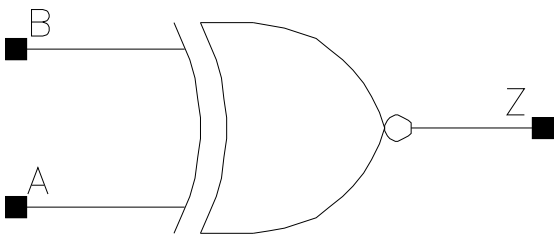
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	4.166e-03	4.277e-03	4.314e-03	4.332e-03
Clock 100Mhz Data 25Mhz	6.501e-03	6.631e-03	7.372e-03	8.066e-03
Clock 100Mhz Data 50Mhz	8.837e-03	8.986e-03	1.043e-02	1.180e-02
Clock = 0 Data 100Mhz	4.868e-03	4.601e-03	4.513e-03	4.469e-03
Clock = 1 Data 100Mhz	1.394e-03	7.266e-04	5.041e-04	3.929e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P0	X8_P0	X17_P0	X25_P0
A	0.0015	0.0006	0.0009	0.0014
B	0.0014	0.0014	0.0017	0.0023
	X33_P0			
A	0.0015			
B	0.0026			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X8_P0**	**X6_P0**	**X8_P0**
A to Z ↓	0.0210	0.0472	3.1029	1.7800
A to Z ↑	0.0229	0.0414	4.8366	3.0658
B to Z ↓	0.0199	0.0330	3.1020	1.7671
B to Z ↑	0.0225	0.0306	4.8504	3.0550
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
A to Z ↓	0.0450	0.0451	0.8783	0.6070
A to Z ↑	0.0380	0.0384	1.5023	1.0018

B to Z ↓	0.0343	0.0333	0.8754	0.6054
B to Z ↑	0.0304	0.0296	1.5000	0.9987
	X33_P0		**X33_P0**	
A to Z ↓	0.0429		0.4553	
A to Z ↑	0.0372		0.7518	
B to Z ↓	0.0322		0.4542	
B to Z ↑	0.0293		0.7519	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P0	8.662e-07	2.529e-12
X8_P0	1.245e-06	3.283e-12
X17_P0	1.869e-06	3.535e-12
X25_P0	2.967e-06	5.047e-12
X33_P0	3.827e-06	5.299e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	2.605e-03	4.794e-03	6.717e-03	1.073e-02
B to Z	2.461e-03	3.287e-03	5.011e-03	7.829e-03
	X33_P0			
A to Z	1.305e-02			
B to Z	9.833e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

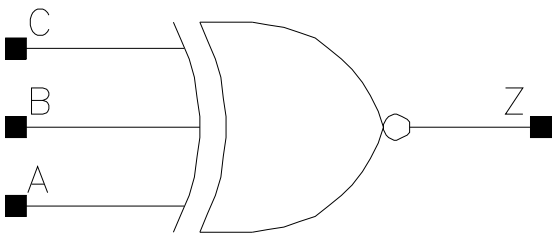
Pin Cycle (vdds)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	-3.024e-06	-2.270e-07	-3.550e-08	2.768e-07
B to Z	1.318e-05	7.220e-08	1.284e-07	1.074e-07
	X33_P0			
A to Z	-2.103e-07			
B to Z	1.084e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	2.176	2.6112
X16_P0	1.200	2.720	3.2640
X25_P0	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X16_P0	X25_P0
A	0.0026	0.0022	0.0027	0.0040
B	0.0029	0.0020	0.0027	0.0036
C	0.0018	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0332	0.0550	3.6969	1.8926
A to Z ↑	0.0325	0.0498	7.1487	3.0338
B to Z ↓	0.0337	0.0547	3.7018	1.8913
B to Z ↑	0.0323	0.0499	7.1423	3.0340
C to Z ↓	0.0328	0.0707	3.7016	1.8907
C to Z ↑	0.0309	0.0648	7.1316	3.0316
	X16_P0	**X25_P0**	**X16_P0**	**X25_P0**
A to Z ↓	0.0555	0.0554	0.9712	0.6230
A to Z ↑	0.0538	0.0536	1.5889	1.0043
B to Z ↓	0.0554	0.0559	0.9707	0.6227

B to Z ↑	0.0539	0.0546	1.5904	1.0045
C to Z ↓	0.0744	0.0790	0.9699	0.6222
C to Z ↑	0.0718	0.0769	1.5886	1.0041

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	9.609e-07	4.544e-12
X8_P0	1.079e-06	4.795e-12
X16_P0	1.747e-06	5.804e-12
X25_P0	2.441e-06	8.074e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	2.918e-03	3.761e-03	6.049e-03	9.101e-03
B to Z	2.685e-03	3.670e-03	5.924e-03	8.958e-03
C to Z	2.614e-03	5.598e-03	8.244e-03	1.242e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

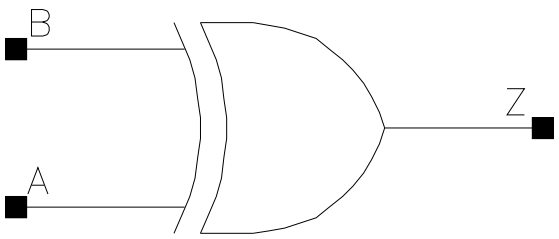
Pin Cycle (vdds)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	-2.932e-05	-1.009e-05	-1.435e-05	-2.239e-05
B to Z	2.184e-05	1.844e-06	9.284e-06	1.692e-05
C to Z	2.635e-05	1.408e-05	2.177e-05	2.869e-05

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.224	1.4688
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.224	1.4688
X16_P0	1.200	1.360	1.6320
X25_P0	1.200	2.176	2.6112
X31_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X16_P0
A	0.0007	0.0014	0.0009	0.0011
B	0.0011	0.0013	0.0014	0.0015
	X25_P0	X31_P0		
A	0.0013	0.0017		
B	0.0024	0.0031		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0426	0.0221	3.1609	2.3784
A to Z ↑	0.0389	0.0232	5.7750	6.3176
B to Z ↓	0.0307	0.0216	3.1491	2.3985
B to Z ↑	0.0302	0.0219	5.7739	6.3193
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0382	0.0401	1.7335	0.8995

A to Z ↑	0.0338	0.0355	2.9837	1.5043
B to Z ↓	0.0298	0.0311	1.7294	0.8982
B to Z ↑	0.0278	0.0293	2.9796	1.5028
	X25_P0	**X31_P0**	**X25_P0**	**X31_P0**
A to Z ↓	0.0424	0.0400	0.6024	0.4825
A to Z ↑	0.0374	0.0356	1.0003	0.8055
B to Z ↓	0.0325	0.0305	0.6017	0.4824
B to Z ↑	0.0288	0.0276	0.9989	0.8053

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.043e-06	3.032e-12
X6_P0	8.992e-07	2.527e-12
X8_P0	1.486e-06	3.033e-12
X16_P0	2.094e-06	3.284e-12
X25_P0	2.917e-06	4.796e-12
X31_P0	3.810e-06	5.050e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	3.662e-03	2.583e-03	4.355e-03	6.258e-03
B to Z	2.787e-03	2.373e-03	3.556e-03	5.160e-03
	X25_P0	X31_P0		
A to Z	9.757e-03	1.193e-02		
B to Z	6.909e-03	8.413e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

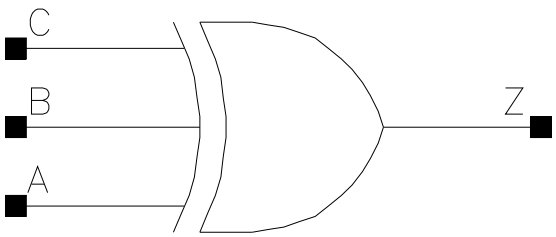
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	-1.218e-07	-7.597e-06	-1.354e-07	1.138e-07
B to Z	-6.559e-08	1.298e-05	-1.000e-07	1.464e-07
	X25_P0	X31_P0		
A to Z	-2.964e-07	-5.000e-07		
B to Z	8.947e-07	1.049e-06		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X24_P0	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X24_P0
A	0.0022	0.0022	0.0027	0.0048
B	0.0023	0.0020	0.0025	0.0040
C	0.0007	0.0015	0.0020	0.0031

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0339	0.0550	3.9025	1.8916
A to Z ↑	0.0326	0.0497	7.7921	3.0314
B to Z ↓	0.0342	0.0549	3.9068	1.8916
B to Z ↑	0.0325	0.0498	7.7883	3.0330
C to Z ↓	0.0553	0.0532	3.8772	1.8911
C to Z ↑	0.0541	0.0479	7.7622	3.0323
	X17_P0	**X24_P0**	**X17_P0**	**X24_P0**
A to Z ↓	0.0505	0.0586	0.9028	0.6524
A to Z ↑	0.0491	0.0447	1.4797	1.0081
B to Z ↓	0.0503	0.0585	0.9026	0.6516

B to Z ↑	0.0490	0.0447	1.4811	1.0081
C to Z ↓	0.0493	0.0563	0.9026	0.6515
C to Z ↑	0.0480	0.0438	1.4805	1.0085

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P0	1.113e-06	4.544e-12
X8_P0	8.890e-07	4.295e-12
X17_P0	1.529e-06	4.543e-12
X24_P0	2.593e-06	7.820e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	2.666e-03	3.784e-03	5.788e-03	9.962e-03
B to Z	2.585e-03	3.649e-03	5.588e-03	9.618e-03
C to Z	5.213e-03	3.523e-03	5.517e-03	9.315e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	-1.403e-05	-1.293e-05	-1.919e-05	-4.394e-05
B to Z	7.065e-06	6.195e-06	1.537e-05	7.841e-06
C to Z	2.514e-05	1.169e-05	2.237e-05	5.146e-05

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