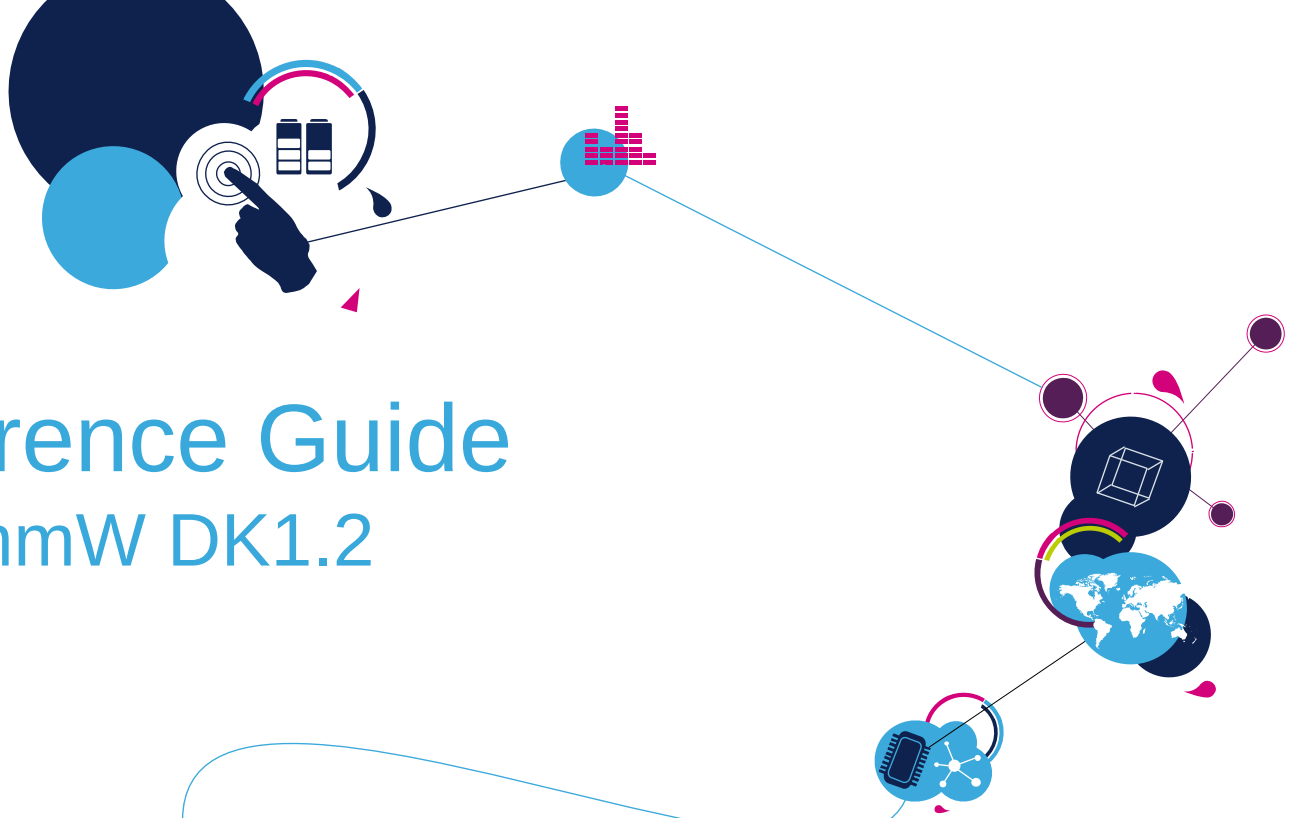

Model Reference Guide

28FDSOI RF mmW DK1.2

September 28th 2018

Spice Modeling team

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Document content

- Generalities on 28FDSOI RF mmW spice models
  - Introduction
  - Simulators
  - Safe Operating Areas (SOA)
- MOSFET models description
- Non-FET devices models description
- Netlists examples for MOSFETs and non-FETs
- General recommendations and "Known Problems and Solutions"

Introduction

- The goal of this reference guide document is to provide the user with basic description, guidelines and recommendations for 28fdsoi RF mmW models usage. Model content is an update of the standard 28FDSOI DK1.1 RF_mmW part.
- Current 28FDSOI RF mmW design platform models are silicon based.
- For recommended simulators versions please refer to the following page and for recommendations and KPS refer to the end of this document
- The FDSOI technology allows more scaling and better leakage performance with less process complexity
  - High performance and low power to ultra-low power System on chip are targeted
  - The UTSOI is the compact model for ultra thin fully depleted SOI Mosfet
    - Model is based on same surface potential as PSP
    - UTSOI model has a unique and extremely attractive characteristics
    - Model uses simplified junction models
- All models are valid in the temperature range [-40°C : 125°C]

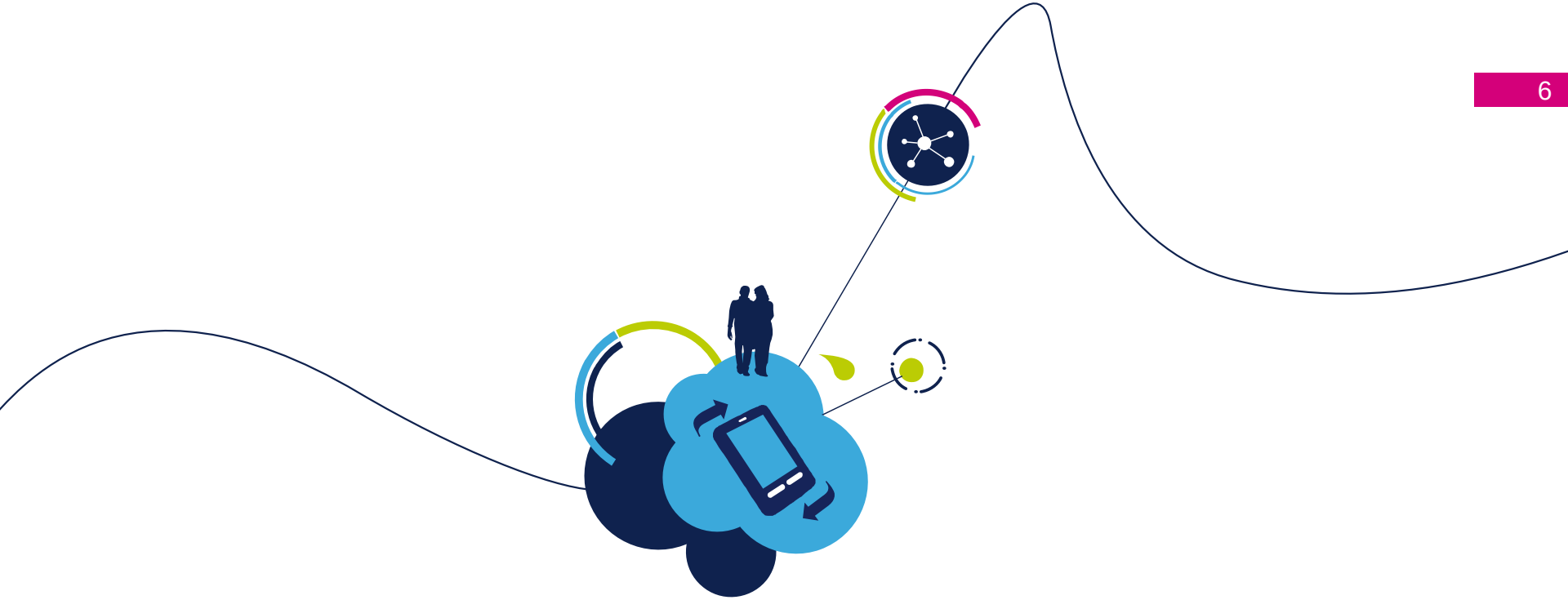
Simulators

- Recommended Simulators Versions*
  - ams: 2018.3
  - hspice: n-2017.12-sp1
  - spectre: 17.10.307
  - customsim (ex- XA): n-2017.12-sp2
  - finesim: m-2017.03-1
  - ads: 2017_update0.2
  - goldengate: 2017-update-0.1
  - afs: 2018.3
- Model validation is executed with above simulator versions
  - All corners and MC sets are executed during QA
  - Multi-simulation comparison tests are executed between all the above simulators

* Please refer to the up to date recommended versions in the Design Kit info (hotfixes might be defined)

Safe Operation Areas (SOA)

- SOA functionality is used to check if the device is properly used
- It is supported for eldo and hspice simulators
- Please refer to dedicated documents for more details
  - SOA_usage.pdf document is an introduction to SOA notions and usage
  - soa_documentation.pdf includes the description of SOA rules implemented in 28FDSOI



MOSFETs

MOS transistor offer - 1

- MOS transistor offer for generic applications is based on so-called “Standard MOS”, which have dedicated Pcell and SPICE models
  - Supported families are SGLVT, SGRVT, EGLVT and EGRVT
  - Associated SPICE models have extension “_acc”
- MOS transistors offer for RF and mm-wave applications is based on a dedicated set of MOS transistors, which have also their own PCell and SPICE models, both optimized for this kind of applications
  - Supported families are SGLVT, SGRVT and EGLVT
  - Associated SPICE models have extension “_rf” or “_rfseg”
  - “_rfseg” models are intended to describe Non Quasi-Static effects, which primarily occur on long channel transistors
    Their usage is exclusively reserved to MOS transistor with gate lengths larger than, or equal to 100nm

MOS transistor offer - 2

- There are two main sets of MOS models
  - _acc models for standard MOS transistors
  - _rf models for RF MOS transistors
    - A second simulation level also exits, _rfseg, to better describe Non Quasi-Static effects in long channel transistors. But please not that this simulation level is accurate only for devices with gate lengths larger than 100nm
- All models have the same DC behavior
  - _rfseg DC behavior may slightly differ from _acc and _rf ones due to channel segmentation effects, especially in saturation regime
  - These differences on _rfseg are minimized for channel lengths larger than 100nm
- _acc models are extracted from DC and AC data (including 1/f noise)

  They should be used for digital and (low frequency) analog designs, but NOT for RF designs
- _rf/_rfseg models are based on _acc models and further validated/tuned using S-parameters measurements in RF and mm-wave frequency ranges
  - They should be used whenever the frequency behavior of the device (starting at the RF range) is of importance
  - Parasitics description includes gate and substrate (well) impedances.
    The way the gate and well are connected has thus to be known
    Therefore, these connections are part of the RF MOS PCell (see next slide)
  - Thermal noise of _rf/_rfseg models is validated/tuned using dedicated Noise Figure measurements

MOS transistor offer - 3

- UTSOI2 based model flavors
  - SG LVT and RVT
    - lvtnfet_acc, lvtpfet_acc
    - nfet_acc, pfet_acc
  - EG LVT
    - eglvtnfet_acc, eglvtpfet_acc, eglvtvnfet_acc, eglvtvpfet_acc
    - eglvtpspfet
  - EG RVT
    - egnfet_acc, egpfet_acc, egvnfet_acc, etvpfet_acc
  - HLVT
    - hlvtnfet, hlvtpfet
  - dsxnfetpd - dsxnfetwl - dsxpfetpu
- UTSOI2 based model flavors - RF
  - SG LVT and RVT
    - lvtnfet_rf, lvtpfet_rf, lvtnfet_rfseg, lvtpfet_rfseg
    - nfet_rf, pfet_rf, nfet_rfseg, pfet_rfseg
  - EG LVT
    - eglvtnfet_rf, eglvtpfet_rf, eglvtvnfet_rf, eglvtvpfet_rf
    - eglvtnfet_rfseg, eglvtpfet_rfseg, eglvtvnfet_rfseg, eglvtvpfet_rfseg
- UTSOI1 based model flavors (SRAM)
  - dsvnfetpd - dsvnfetwl - dsvpfetpu
  - dswnfetpd - dswnfetwl - dswpfetpu
  - lslnfet
  - lsdnfetpd - lsdnfetwl - lsdpfetpu
  - lspnfetpd - lspnfetwl - lsppfetpu
  - lsvnfetpd - lsvnfetwl – lsvpfetpu
- PSP based model flavors
  - ndriftotp, egnexti, egpext
  - esdnfet, esdegnfet
- Please refer to “modelstatus.pdf” and “ageing_modelstatus.pdf” for more details
- SRAM models are not documented here
- PSP-based models are described in the "non-FETs" section

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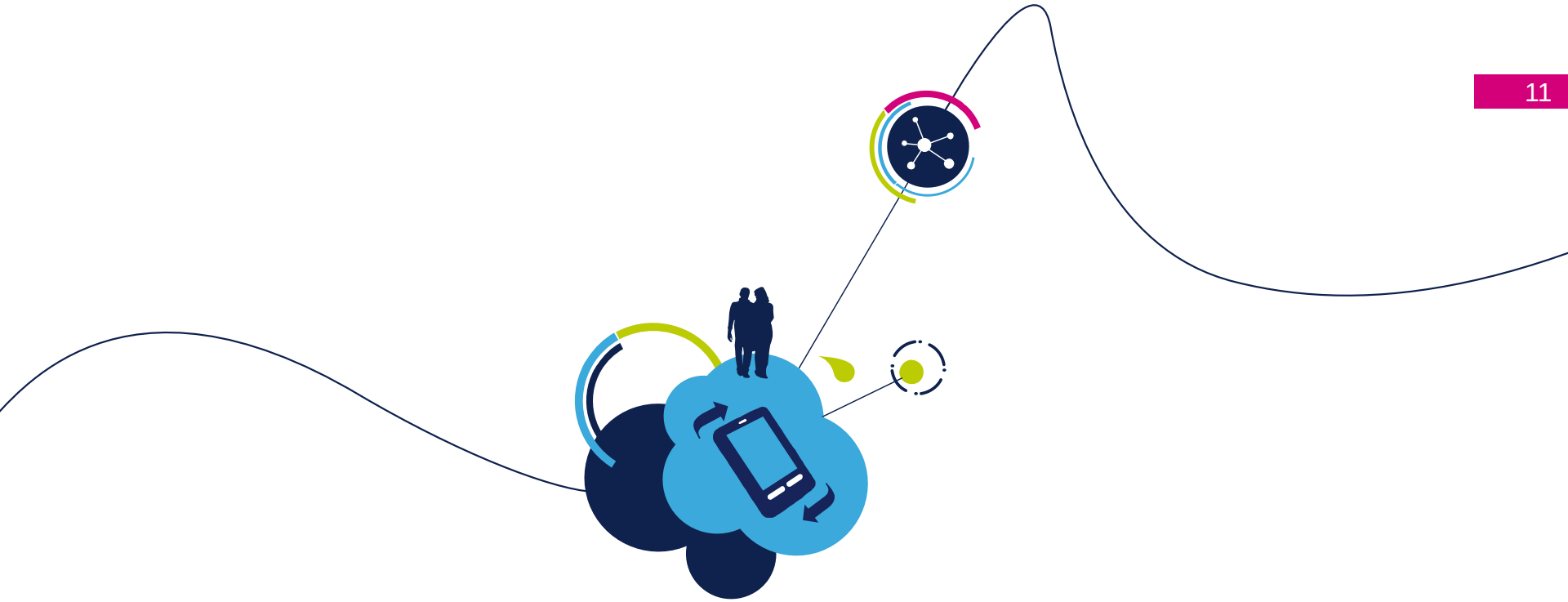
MOSFETs features accessibility

- New model releases are focus on analog/RF applications
  - Improved matching model
    - See dedicated documentation "28FD_MOS_mismatch_model_doc.pdf"
  - RF devices models aligned on dedicated PCell, with improved description of Ft/Fmax

	RF devices
PCell	Optimized for RF
Flavors	SG LVT & RVT EG[V] LVT

	Accurate simulation level	Standard simulation level	rfseg simulation level
Ex: NRVT	nfet_acc	nfet_rf	nfet_rfseg
mismatch	xypos dependent	xypos dependent	
NQS	None	Simplified model	Segmented model (nqs) for L>100nm



MOSFETs

MOSFETs instance parameters

Layout related parameters

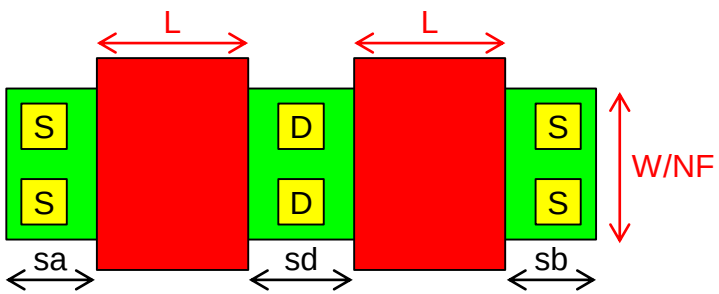
Instance parameters	Default value	Comment
w	8.00E-08	Gate width *(default value for SG MOS)*
nf	1	Number of poly Fingers
l	3.00E-08	Gate length *(default value for SG MOS*
p_la	0	Poly biasing value *(Standard Cells only)*
as	-1	Source area
ad	-1	Drain area
sa(1)	-1	Rx extension on drain side
sb(1)	-1	Rx extension on source side
sd(1)	-1	Poly space
d0(1)	-1	WPE
d1(1)	-1	WPE
sca(1)	-1	Well proximity effect first order parameter
scb(1)	-1	Well proximity effect second order parameter
scc(1)	-1	Well proximity effect third order parameter
lpccnr(1)	0	Pc corner rounding
covpccnr(1)	0	Fringe capa Correction factor due Pc corner rounding
wrxcnr(1)	0	Rx corner rounding value
ngcon(1)	1	Number of contacted pc heads
xpos, ypos(1)	-1	Gate absolute position
plorient(1)	1	Gate orientation
pcpastrx_top(1)	-1	Top PC extension on STI
pcpastrx_bot (1)	-1	Bottom PC extension on STI

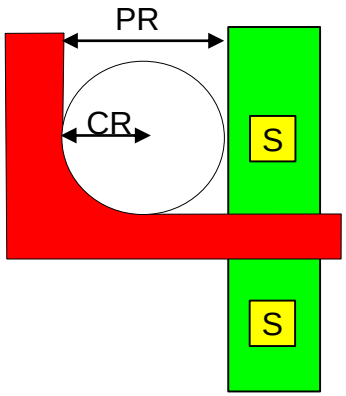
Simulation related parameters

Instance parameters	Default value	Comment
pre_layout_local	-1	Pre/post layout switch
mismatch	1	Disable mismatch
nsig_dnoise(1)	0	Mismatch noise sigma
soa	1	Soa flag
swshe(2)	0	Self-heating flag
swrg(1)	0	Rgate flag
par	1	Multiplicity factor for mismatch

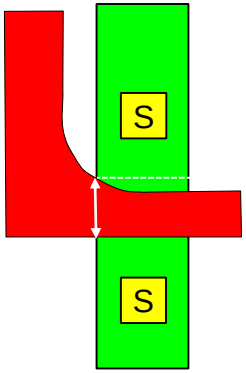
(1) : parameter not available for SRAMs

MOSFETs layout instances





Definition of PR and CR (corner radius)

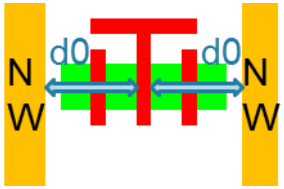


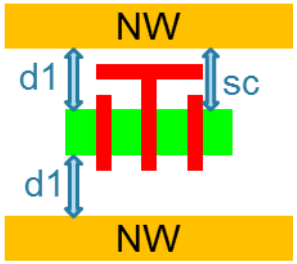
Application case: PR < CR
➔ L increase

- Primary parameters: L, W, NF
- Stress parameters: sa, sb, sd
  - sd assumes constant poly space
  - post-layout: 1 instance per gate finger
    - NF=1
    - sa, sb, different between fingers
- Well Proximity Effect parameters
  - sca, scb, scc: complex equations able to reproduce any shape (post-layout)
- Corner rounding of L-shapes
  - lpccnr, covpccnr, wrxcnr: additional effective L, capacitance, W respectively
  - No impact on regular layout

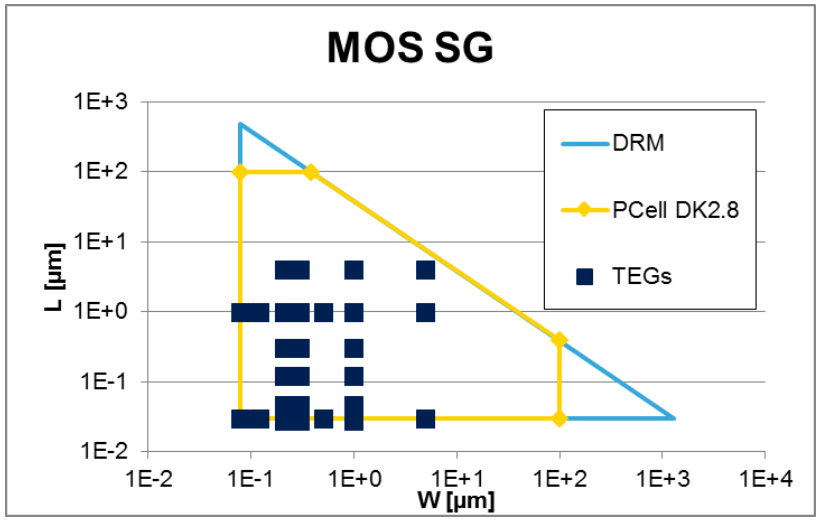
Spice instance parameters

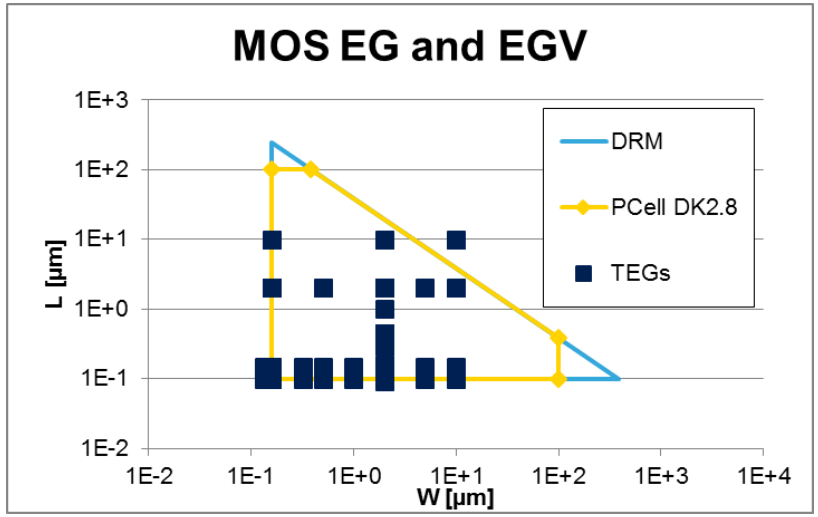
- Some instance parameters are not accessible from DK
  - They are used by the modeling team
  - However, they may be of interest for debug
- WPE layout parameters (sca+scb+scc) may be replaced
  - By d0 in case of vertical wells on both sides
  - By d1 in case of horizontal wells on both sides
  - By sc in case of horizontal wells on single side (inverter case)
- It is possible to emulate a Vt shift/a mobility modification
  - p_vta emulates a vt shift, whatever geometry/temperature/corner
    - default value 0, unit V
  - u0_mult emulates a mobility modification
    - default value 1, act as a multiplier
    - Note: it does not affect the series resistances





Geometries used for extraction





- Rule 132 is applied
  - Gate maximum area: 38.661µm²
- Maximum available geometries in TEGs
  - Wmax = 5µm
  - Lmax = 4µm
- Maximum available geometries in PCell
  - Wmax = 35µm
  - Lmax = 10µm
- Confident on extrapolation for long/wide devices up to max Pcell geometries
- RF MOS use other geometries

MOSFETs variation modeling

- Global variations are set with common_fet and common_feol section
- Local variations are set thanks to <family>_dev flag
  - <family>_dev=0: no local variations
  - <family>_dev=1: local variations in MC simulations

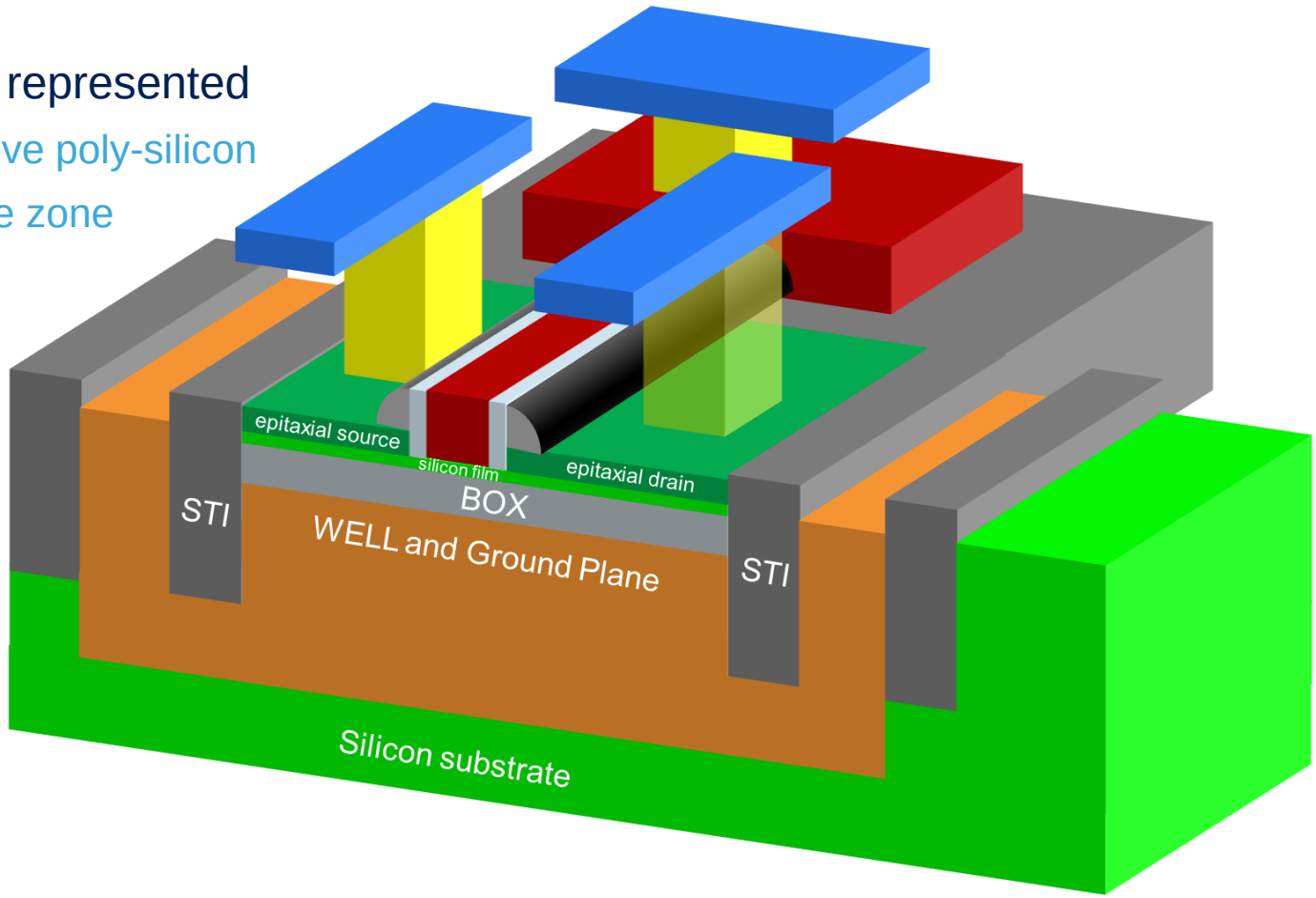
See next slides for netlist examples

- The attendance to a dedicated training on this purpose is recommended.

	Definition	Corner/<family_dev>	
MonteCarlo (MC)	MC, global + local	statmotherfab	1
	MC, global only	statmotherfab	0
Performance corners	timing, global only	SS/FF	0
Functional corners	device, global only	SSF/FFF/SF/FS	0

Simplified MOSFET representation

- As-designed shapes
  - Contacts on silicon are round
- Some elements not represented
  - spacers out of active poly-silicon
  - silicon out of active zone
  - silicide
- LVT nfet like
  - NW
  - no T3



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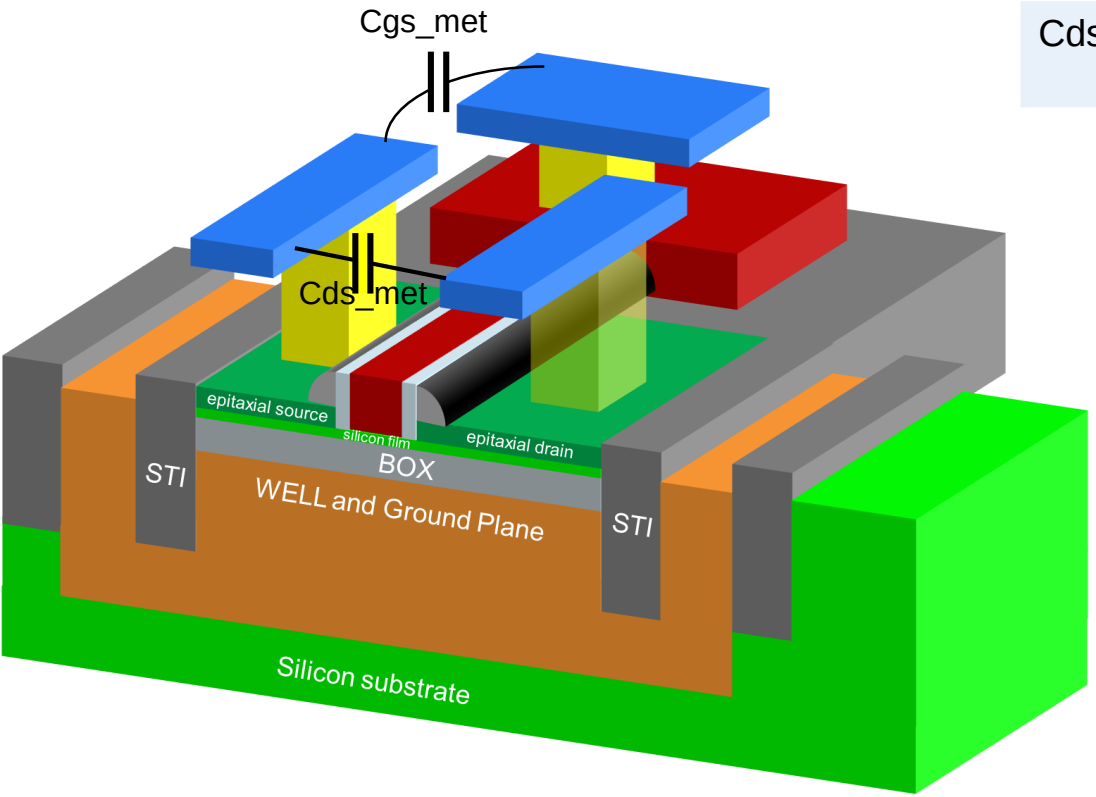
Middle-end parasitic capacitances

Capa	Description	PEX/spice*
Cgs_met Cgd_met	M1/M1	PEX
Cds_met	M1 and contacts	PEX/spice



PEX/SPICE* column description

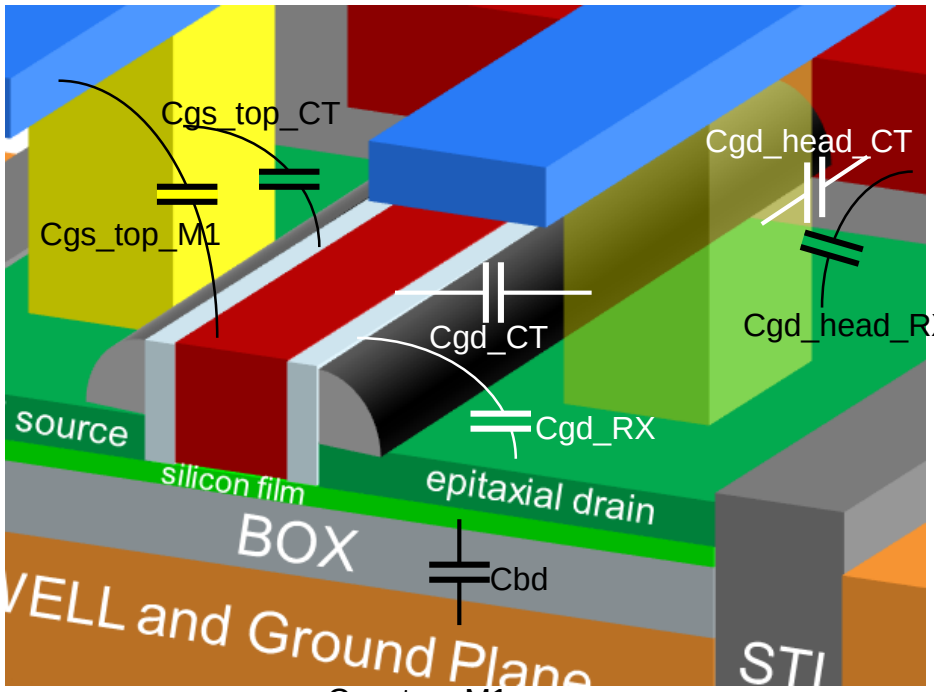
PEX: only in PEX

SPICE: only in spice

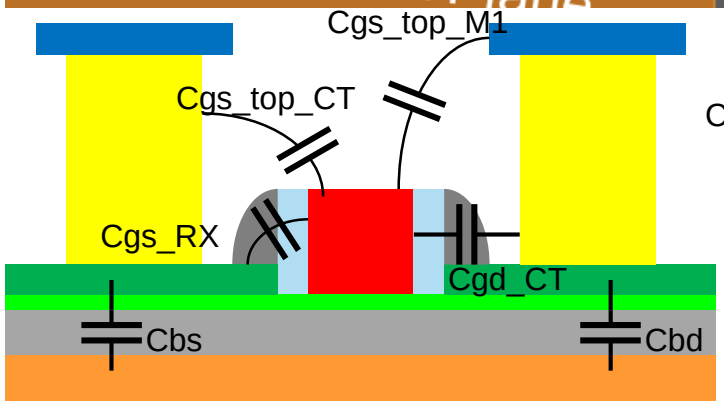
PEX/SPICE:

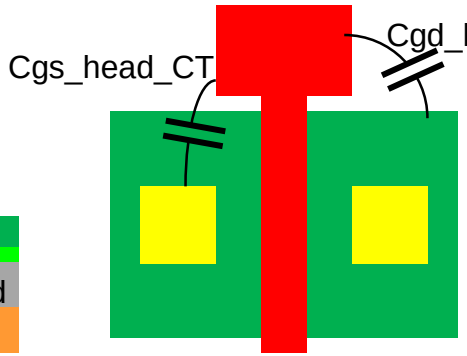
- in spice in pre-layout
  - assuming a given layout
- in PEX in post-layout

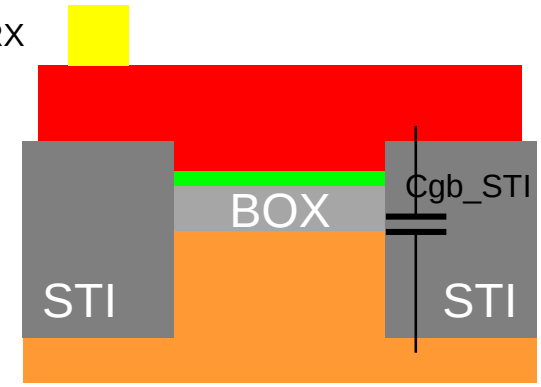
Front-end parasitic capacitances



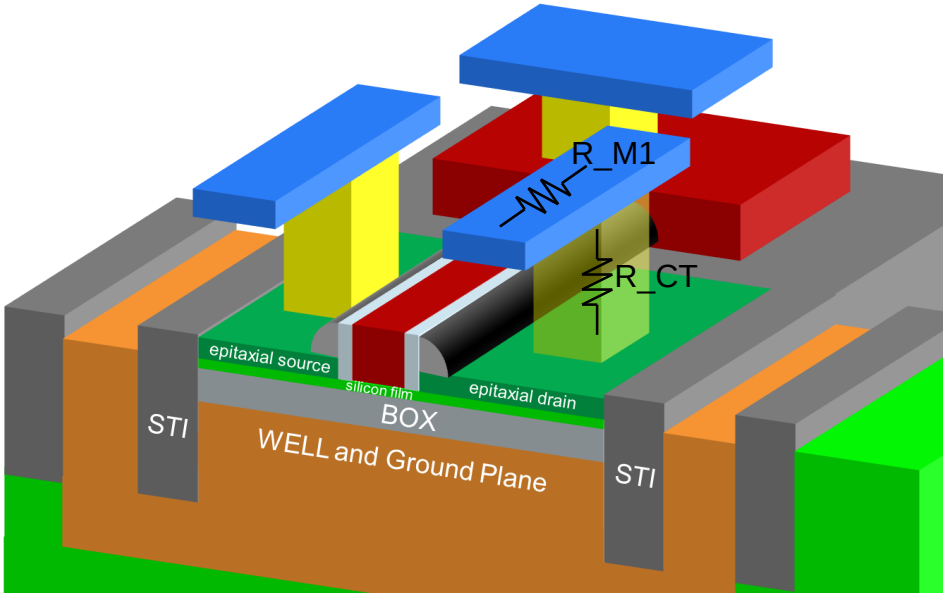
Capa	Description	PEX/spice*
Cbd, Cbs	Source/Drain through BOX	spice
Cgd_RX, Cgs_RX	Vertical poly to RX	spice
Cgd_CT, Cgs_CT	Vertical poly to CT	PEX/spice
Cgd_top_CT, Cgs_top_CT	Poly top to CT	PEX/spice
Cgd_top_M1, Cgs_top_M1	Poly top to M1	PEX/spice
Cgd_head_CT, Cgs_head_CT	Poly head to S/D	PEX/spice
Cgd_head_RX Cgs_head_RX	Poly head to contact on S/D	PEX/spice
Cgb_STI	Poly head on STI to well	PEX/spice



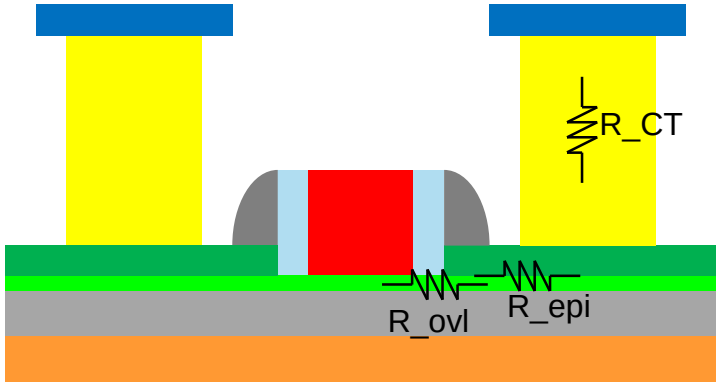


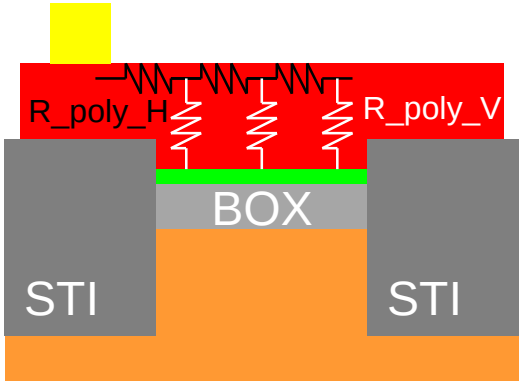


Parasitic resistances



Capa	Description	PEX/spice*
R_M1	Metal 1 resistance	PEX
R_CT	Contact resistance	PEX/spice
R_ovl	R_ovl	spice
R_epi	R_epi	spice+PEX
R_poly_H	Horizontal gate resistance	On RX: spice On STI: PEX
R_poly_V	Vertical gate resistance	spice





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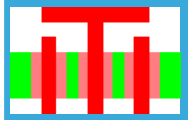
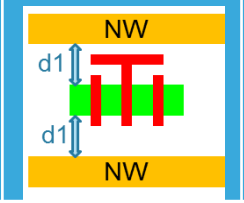
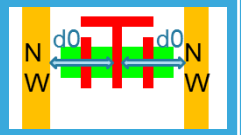
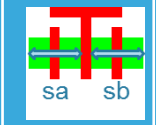
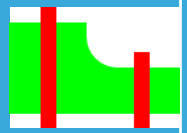
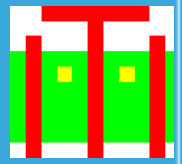
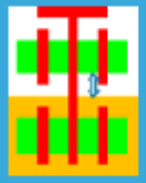
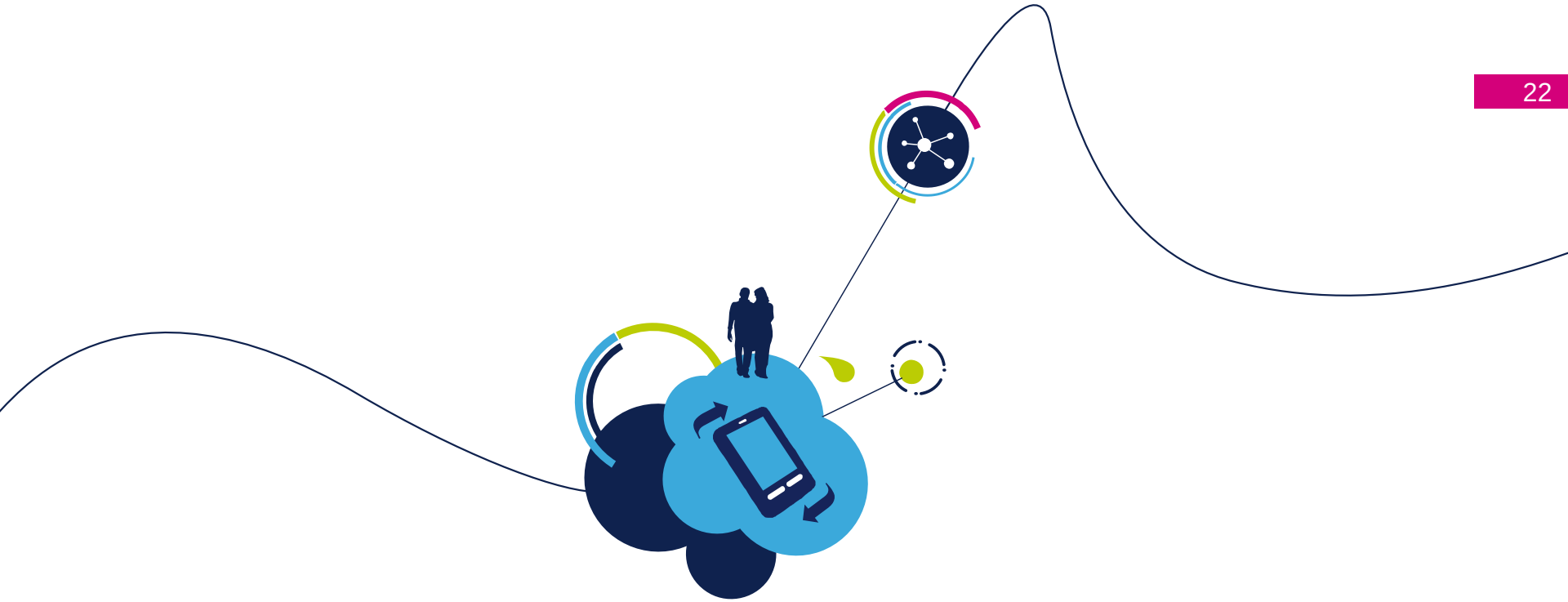
Local Layout Effects - 1

- Included in CAD
  - In some cases, effects have found negligible and then not included
  - Please refer to modelstatus.pdf for the list of active effects per device

Poly bias	WPE vertical	WPE horizontal	LOD	RX rounding	PC rounding	Contacts position	PC past RX
							
Spice				ΔW, ΔW in PLS		PEX	

- Not included in CAD

Poly pitch	OD spacing horizontal	OD spacing vertical	PG proximity
			
			Single gate stack: no effect



RF MOSFETs

RFMOS

- Devices with dedicated PCell optimized for RF are now available
  - SG LVT and RVT: nfet_rf, pfet_rf, lvtnfet_rf, lvtpfet_rf
  - EG LVT: eglvtnfet_rf, eglvtpfet_rf, egvlvtnfet_rf, egvlvtpfet_rf
- Associated RF models covers
  - Accurate modeling of parasitics: capacitive, Rgate, Rsub
  - Based on [S]-par measurement up to 110Ghz
  - Based on NF measurement up to 26GHz
- Non Quasi Static model is also available
  - With _rfseg extension
  - effective for L >= 100nm
  - With increased number of internal nodes impacting simulation time

RF MOSFETs instance parameters

Layout related parameters

Instance parameters	Default value	Comment
w	1e-6	Gate width *(default value for SG MOS)*
nf	1	Number of poly Fingers
l	3.00E-08	Gate length*(default value for SG MOS)*
as	-1	Source area
ad	-1	Drain area
ps	-1	Source perimeter
pd	-1	Drain perimeter
sa	-1	Rx extension on drain side
sb	-1	Rx extension on source side
sd	-1	Poly space
d0	-1	WPE
d1	-1	WPE
sca	-1	Well proximity effect first order parameter
scb	-1	Well proximity effect second order parameter
scc	-1	Well proximity effect third order parameter
ngcon	1	Number of contacted pc heads
xpos, ypos	-1	Gate absolute position
pl_orient	1	Gate orientation
pcpastrx_top	-1	Top PC extension on STI
pcpastrx_bot	-1	Bottom PC extension on STI

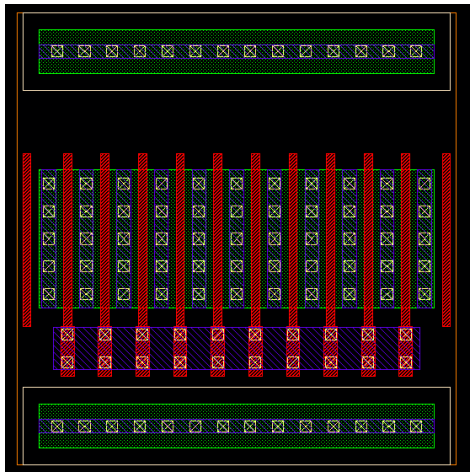
Instance parameters	Default value	Comment
strap	2	Well access configuration
wstrap	160e-9	Well access width
numcos, numcod	-1	Number of contacts on S, D
pocos, pocod	33e-9	Poly to contact distance
ptwell	1	Triple well flag

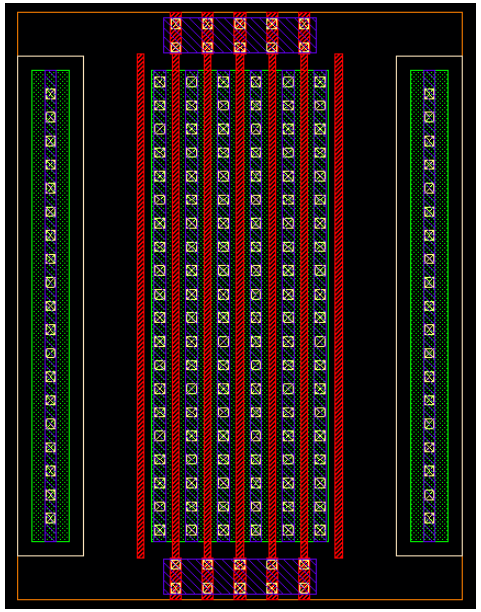
Simulation related parameters

Instance parameters	Default value	Comment
pre_layout_local	-1	Pre/post layout switch
mismatch	1	Disable mismatch
nsig_dnoise	0	Mismatch noise sigma
soa	1	Soa flag
swshe	0	Self-heating flag
par	1	Multiplicity factor for mismatch
swnqs	1	Non Quasi Static flag

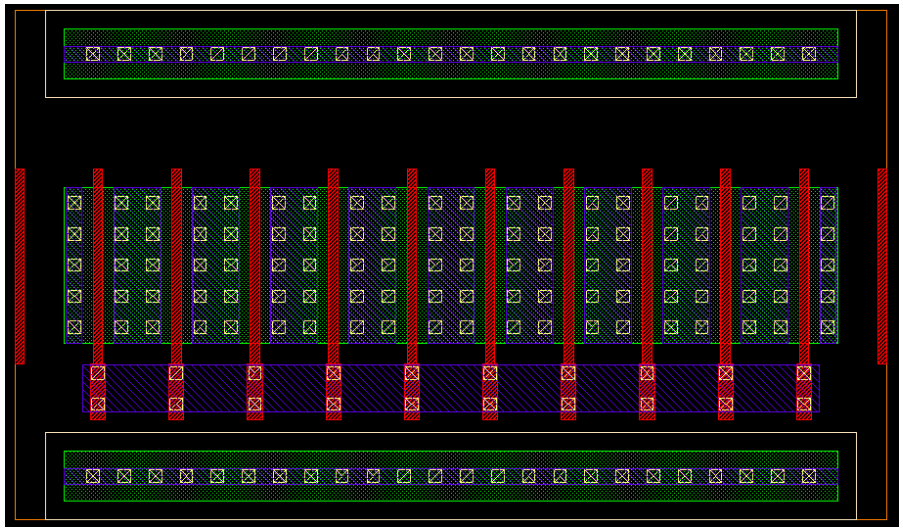
RF MOSFETs PCell features

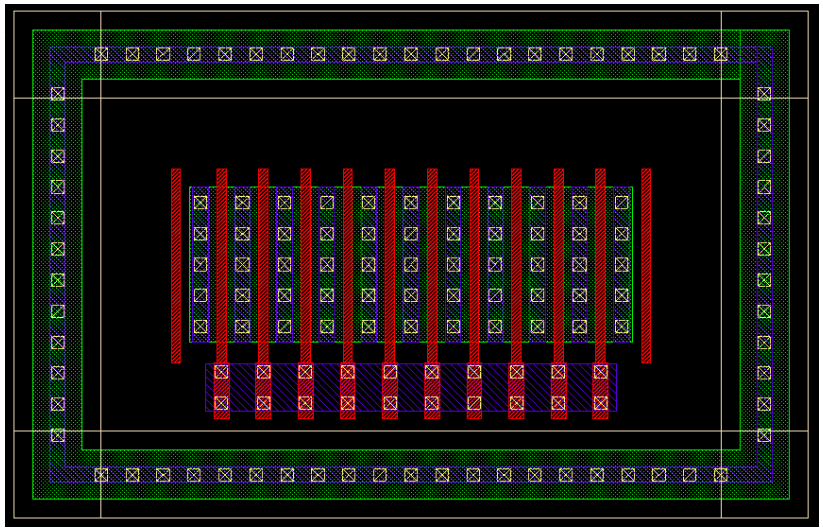
- Handle layers up to Metal1 only
  - Consistent with parasitic elements included in the model
- Access to front gate
  - As small as possible poly head(s)
  - Poly head(s) can have 1 or 2 contact rows (ncrg)
  - Front gate can be connected on both sides (ngcon)
- Flexible topology for Source/Drain accesses
  - Inner Source/Drain can have 1 or 2 contact rows (ncr[s/d])
  - Variable number of contacts per row (numco[s/d])
  - Variable distance of contacts to poly (poco[s/d])
- Access to back-gate (well strap) is always drawn
  - Allow accurate modeling of back-gate impedance
  - Flexible layout with Top/Bottom/Left/Right straps or not (strap) and variable strap width (wstrap)

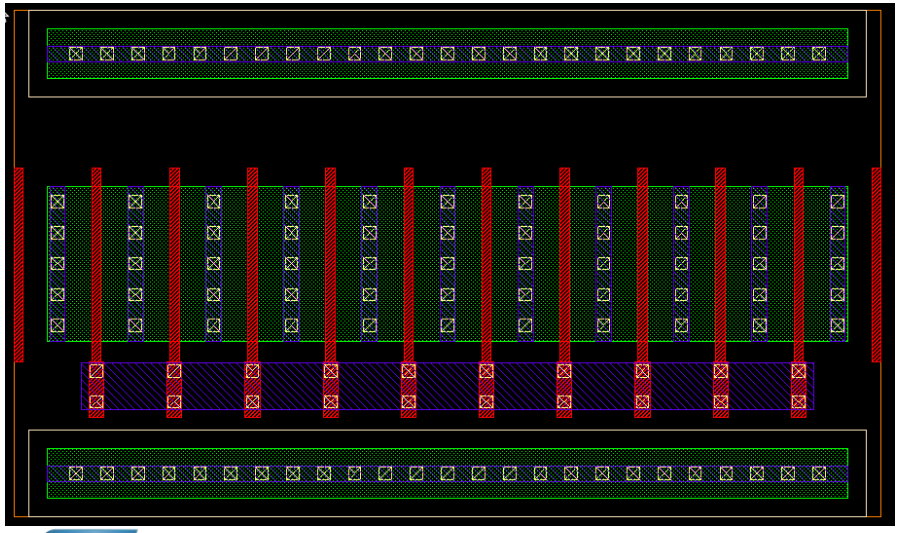


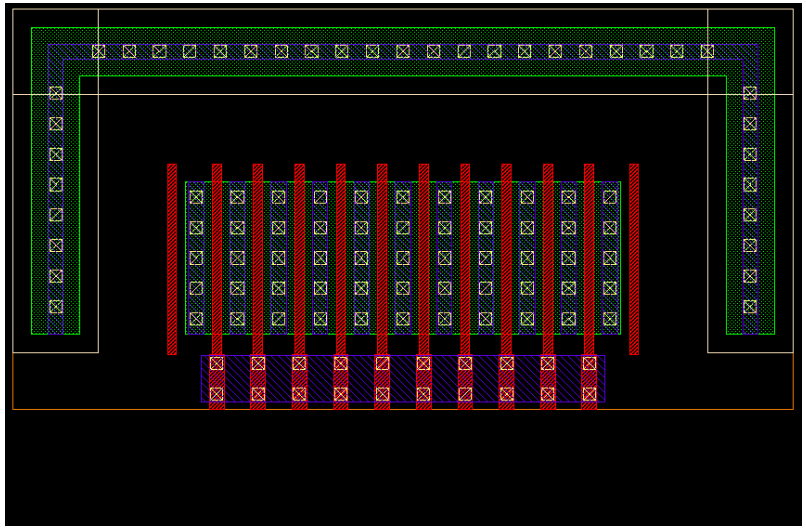


RF MOSFETs PCell-based layout examples



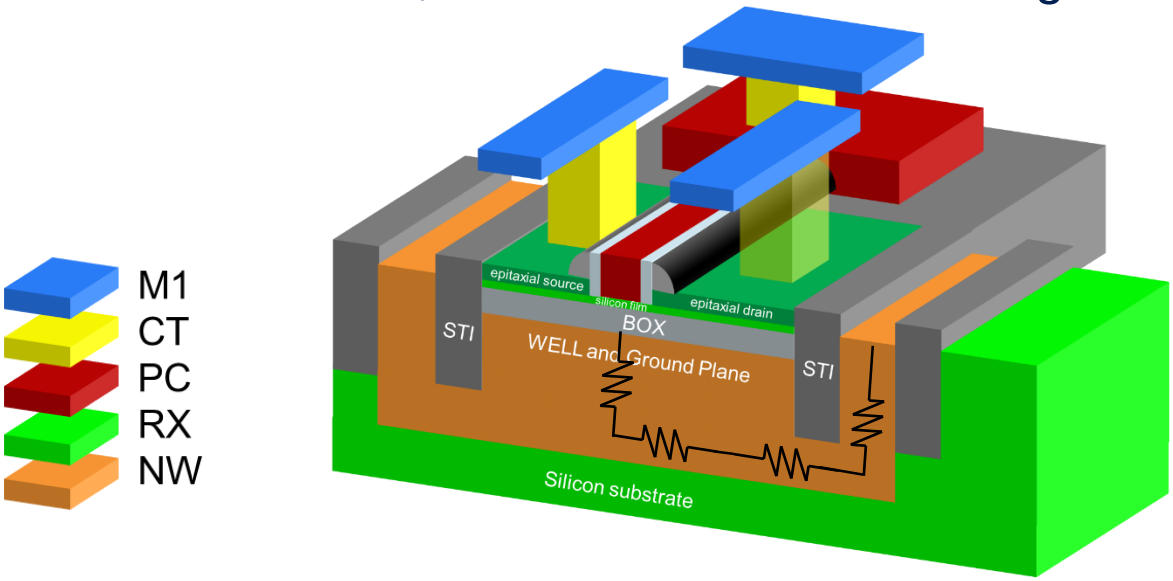


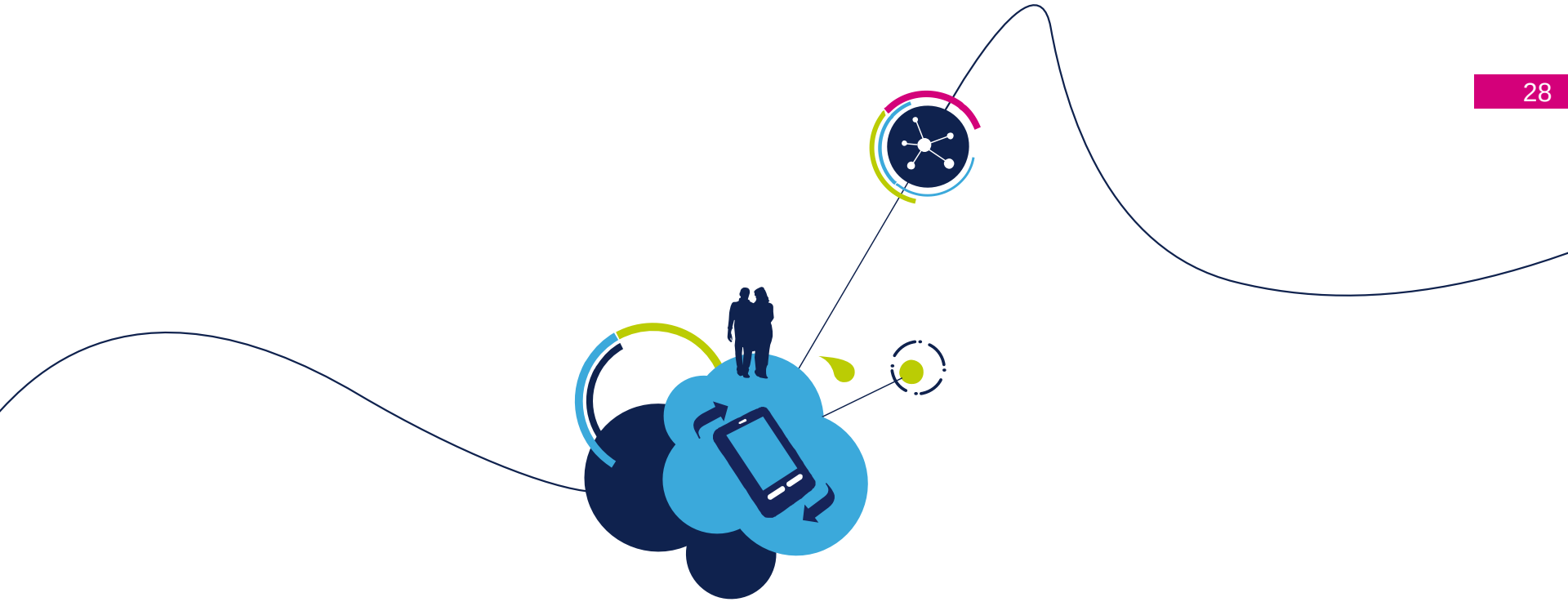




RF MOSFETs parasitics

- In accurate (_acc) MOSFETs, parasitics are mainly modeled by PEX
  - Because this is the only way to support all layout configurations
  - Please refer to dedicated section, earlier in this document
- In RF MOSFETs, parasitics are all modeled in the spice models
  - Because RFMOS PCell very regular
- Same parasitics are modeled, with addition of the back-gate resistance

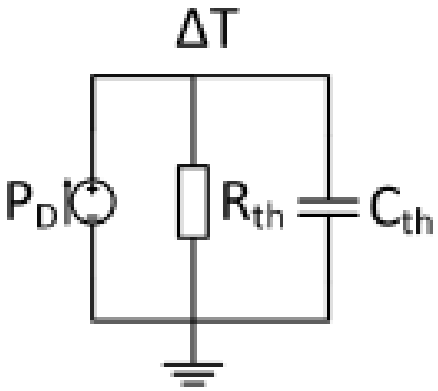


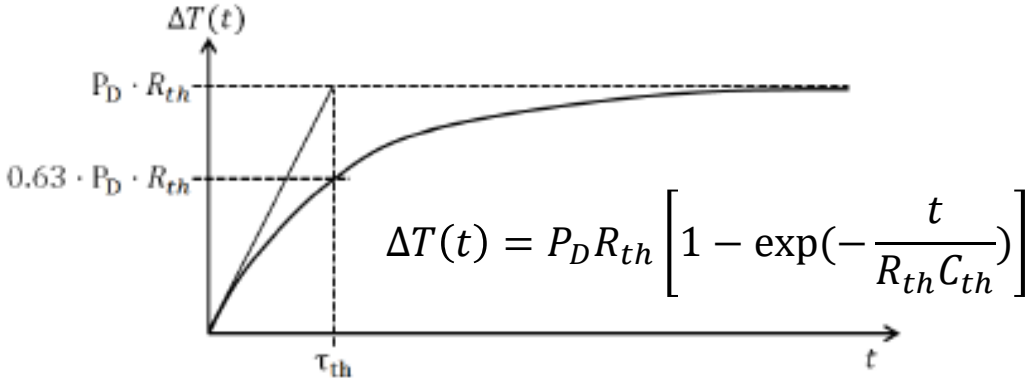


Self-Heating in MOSFETs

General considerations

- Self-Heating effect is a transient temperature rise, ΔT, of the device
- The transient temperature rise ΔT:
  - is proportional to the dissipation power, $P_D = I_{ds} x V_{ds}$, through the device thermal resistance, R_{th}
  - is getting lower when dissipation power is varying fast, due to the existence of a finite thermal capacitance, C_{th}





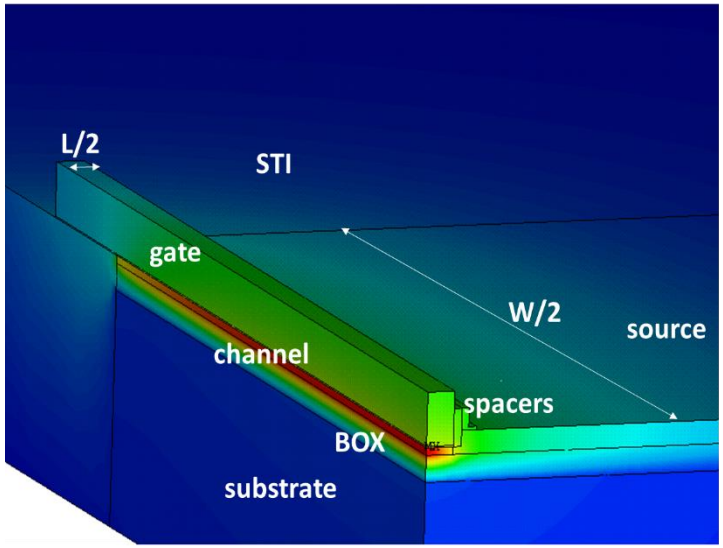
- R_{th} and C_{th} varies with device dimensions, and strongly depends on the device environment
  - Nature of surrounding materials
  - Conditions at the limits of the device environment (wafer-level, package, etc.)

Self-Heating in FD-SOI technology

- In MOS transistors, Self-Heating effect appears when dissipated power is large enough, i.e. in saturation regime (high I_{ds} and high V_{ds})
- In FD-SOI technology, Self-Heating has a limited impact on device parameters compared to the case of a Partially-Depleted (PD) SOI technology, for the following reasons [1,2]:
  - BOX is thin and allows better heat dissipation
  - MOS transistors have raised source and drain which lower their thermal resistance

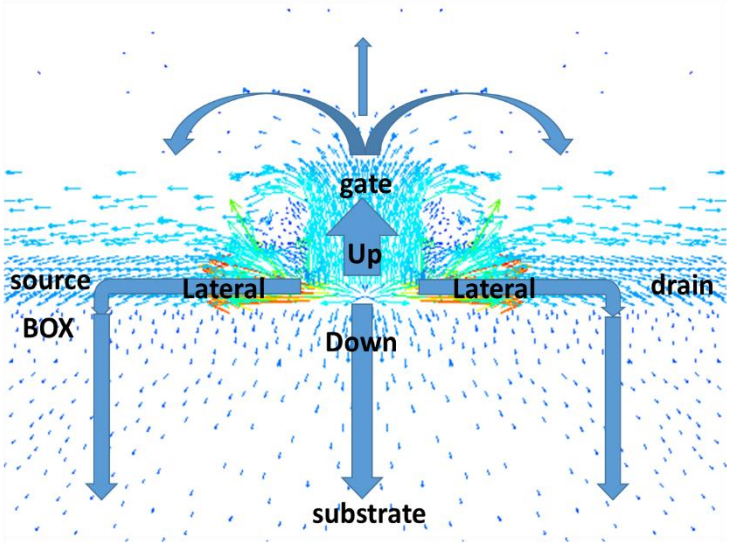
- [1] T. Takahashi, T. Matsuki, T. Shinada, Y. Inoue, and K. Uchida, “Comparison of self-heating effect (SHE) in short-channel bulk and ultra-thin BOX SOI MOSFETs: impacts of doped well, ambient temperature, and SOI/BOX thicknesses on SHE,” in IEEE International Electron Devices Meeting, 2013, pp. 184–187.
- [2] S. Makovejev, N. Planes, M. Haond, D. Flandre, J.-P. Raskin, and V. Kilchytska, “Self-heating in 28 nm bulk and FDSOI,” in Ultimate Integration on Silicon (EUROSOI-ULIS), 2015 Joint International EUROSOI Workshop and International Conference on, 2015, pp. 41–44.

Wafer-level simulations with 2D/3D steady-state thermal finite elements analysis



Temperature field in active region and STI

- Strong temperature gradients in BOX and gate oxide
- Temperature rise in the gate higher over the active zone
- Strong decrease of temperature in the STI



Heat fluxes

- Globally the heat flux is directed downwards
- Locally the BOX causes thermal confinement
- At wafer level, negligible flux goes through BEOL

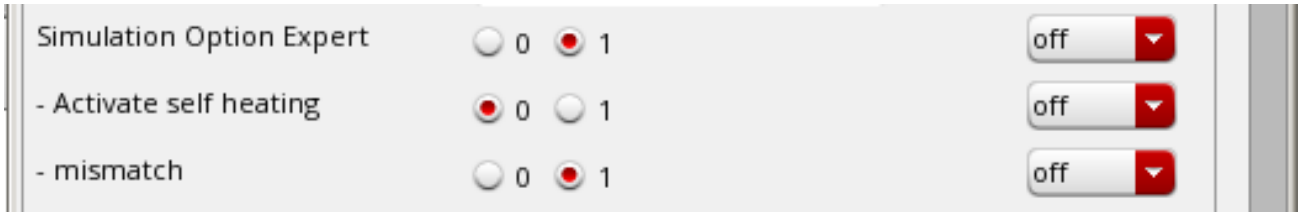
From "Wafer level measurements and numerical analysis of self-heating phenomena in nano-scale SOI MOSFETs", G. Garegnani, V. Fiori, G. Gouget, F. Monsieur and C. Tavernier, Microelectronics Reliability 63 (2016) 90-96.

Self-Heating in SPICE models

- SPICE model parameters extraction is done using MOS transistor measurements performed at wafer level
- To ensure SPICE model accuracy, Self-Heating effect is accounted for during the model parameter extraction
  - To do so, a scalable model of thermal resistance, R_{th}, is extracted from dedicated measurements, also performed at wafer level
- Thermal resistance model is part of the delivered SPICE model, but is only valid for wafer-level operating conditions as encountered during SPICE model extraction or process monitoring
  - In real circuit operation, thermal dissipation path may differ from the one in wafer-level operating conditions
  - As a result, Self-Heating effect is de-activated by default (swshe=0)

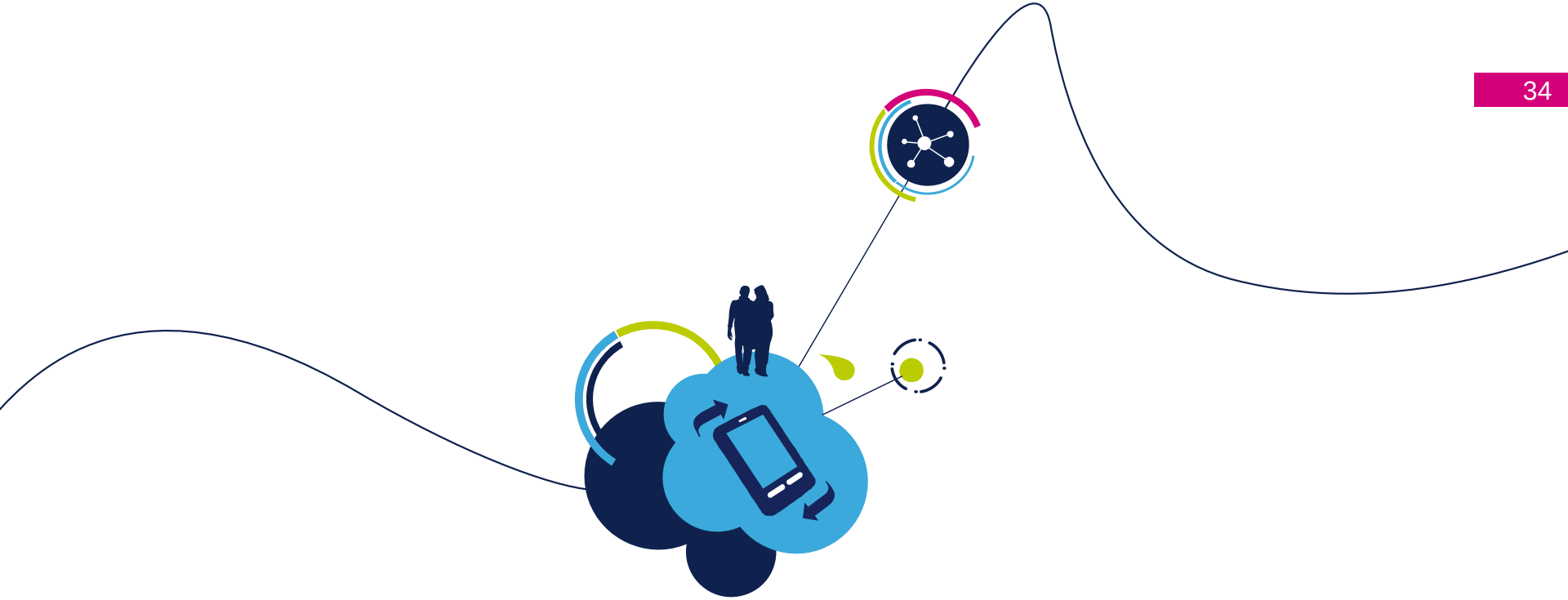
Simulation of Self-Heating

- Since Self-Heating effect is de-activated by default in SPICE model, a Safe Operating Area (SOA) feature is alerting the user in case of significant device temperature rise(1) (threshold set at 20°C)
- If desired, the user may activate the Self-Heating effect in SPICE model through the proper option in the schematic object properties window (after enabling Simulation Expert Option)



- Please note that, in this case, simulation will be performed using thermal impedance values corresponding to wafer-level device environment conditions

(1) Thermal coupling in multi-finger MOSFETs is not accounted for in this estimation



Non-FETs

Non-FETs devices list

Family	Related devices
MOSFETs	ndriftotp, egnexti, egpext *(MOSFETs section is dedicated to logic/analog/RF MOSFETs)*
bipolar	vnpn, vpnp
resistors	nwres*, nwres_std opndres*, opndres_std opppcres*, opppcres_std opppcres_lc*, opppcres_lc_std opreres*, opreres_std lvsres, rcs_<metal option>
metal capacitors	cmim16acc* cmom_<metal option>_2p, cmom_<metal option>_2p_acc cmom_<metal option>_sh, cmom_<metal option>_sh_acc cmom_<metal option>_wo_via_2p , cmom_<metal option>_wo_via_2p_acc cmom_<metal option>_wo_via_sh, cmom_<metal option>_wo_via_sh_acc cmom_rf_10f_80n, cmom_rf_10f_100n, cmom_rf_50f_80n, cmom_rf_50f_100n, cmom_rf_150f_80n, cmom_rf_150f_100n
diodes	diodenwx, diodenwx_lvs, diodenx, diodepnw, diodepwtw, diodepwtw_lvs diodetwx, diodetwx_lvs, egdiodenx, egdiodepnw, egtdndsx, egtdpdnw, tdndsx, tdpdnw
MOS varactors	egncap , egpcap, cvar_sg cvar_eg, cvar_eg_atto, cvar_eg_diff
inductors	ind_hq_<metal option>, ind_lohq_<metal option>, ind_lohq_high_perf_<metal option> inddif_hq_<metal option>, inddif_lohq_<metal option>, inddif_lohq_high_perf_<metal option>
ESD	esdegnfet, esdnfet, esdvnpn, esdvnpn_eg, esdvpnp, esdvpnp_eg, sblkndres, sblkpdres, esdndsx, esdndsx_eg, esd_ulc_rvt, esd_ulc_eg, esd_lowcap (**default models are non-Verilog-a models**)

** "acc" instance parameter can be used to switch to standard model version*

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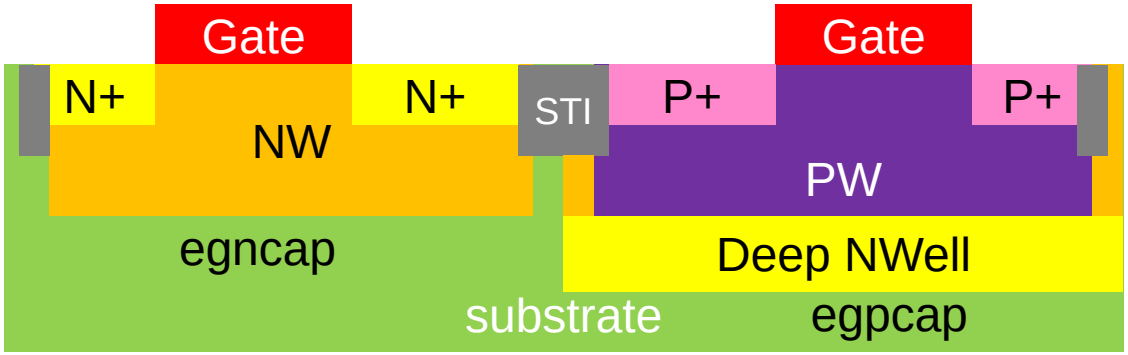
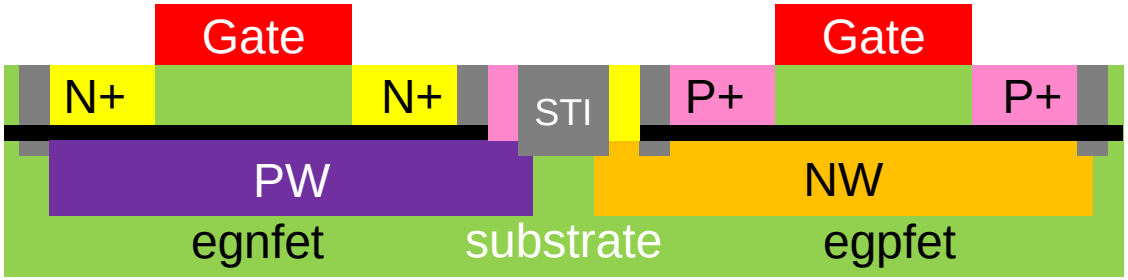
poly-well capacitors vs MOSFETs

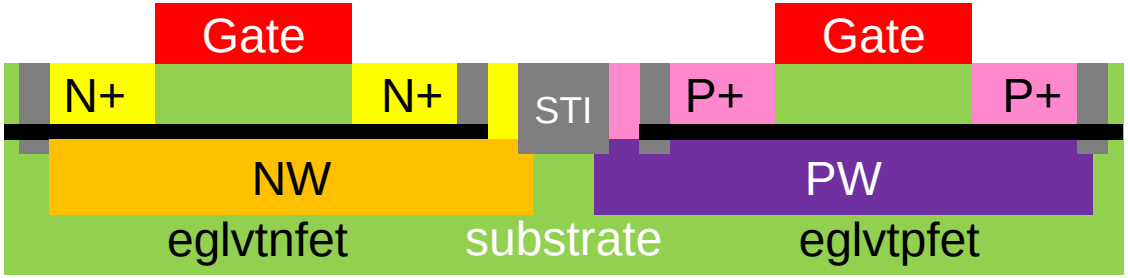
Poly-Well:
On hybrid (not SOI)



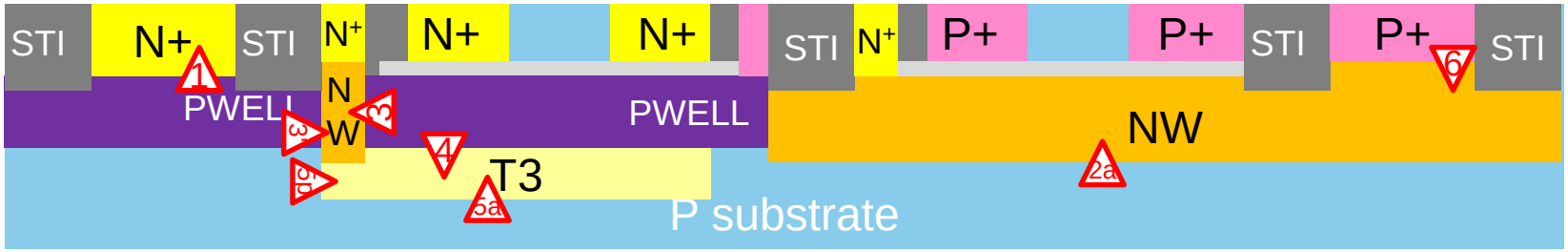
RVT MOSFET:
FDSOI
regular well = bulk like
T3 possible on egnfet



LVT MOSFET:
FDSOI
flip well
T3 possible on eglvtpfet



Diodes 1/2



Name			N	P	Breakdown voltage
diodenx	area	1	N+	PWell	6V
	peri		STI		
diodenwx	area	2	NWell	Psub	9V
	peri	3	NWell	PWell	
diodepwtw	area	4	T3	PWell	9V
	peri		T3	Psub	
diodetwx	area	5a	T3	Psub	9V
	peri	5p	T3+NW	Psub+PW	
diodepnw tdpdnw	area	6	NWell	P+	7V
	peri		STI		

Diodes 2/2
Geometries used for model extraction

- Diode models are extracted on rectangular diodes matrices
- All diodes are extracted with the same geometries

area [µm²]	perim [µm]	X [µm]	Y [µm]
1024	128	32	32
200	90	40	5
2.5	11	5	0.5

Resistors (1/3)

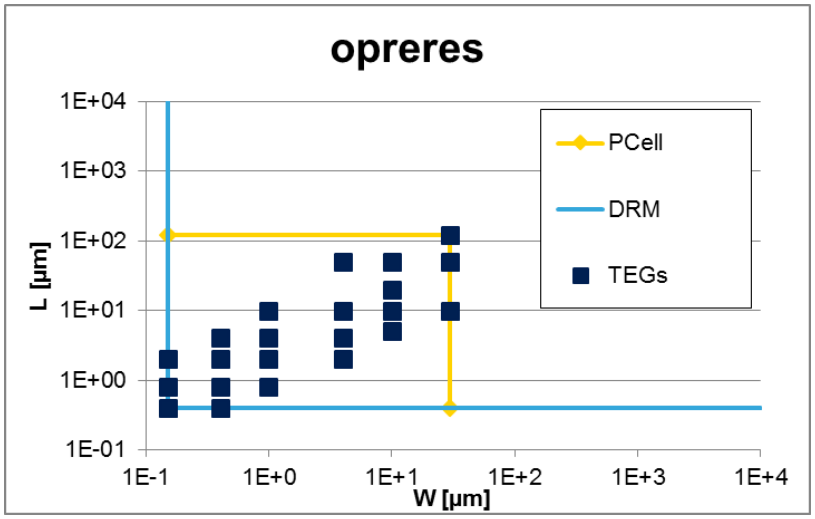
- The RESISTOR device model is physically based (not a fit model). The model accounts for the effects of geometry, temperature, noise, mismatch, and bias (nonlinearity). This three terminal resistor model has been successfully used to characterize different types of integrated resistors processed in CMOS technologies.
- The resistance value is calculated using the expression:
- $R = \frac{\rho.L}{W.t} = Rs.\frac{L}{W}$
- where:
  - R : Resistance (Ohm)
  - ρ : resistivity of the material (Ohm-m)
  - L : length of the strip (m)
  - W : width of the strip (m)
  - t : thickness of the strip (m)
  - Rs: sheet resistance that is the resistance of a square of material: L=W (W/square)

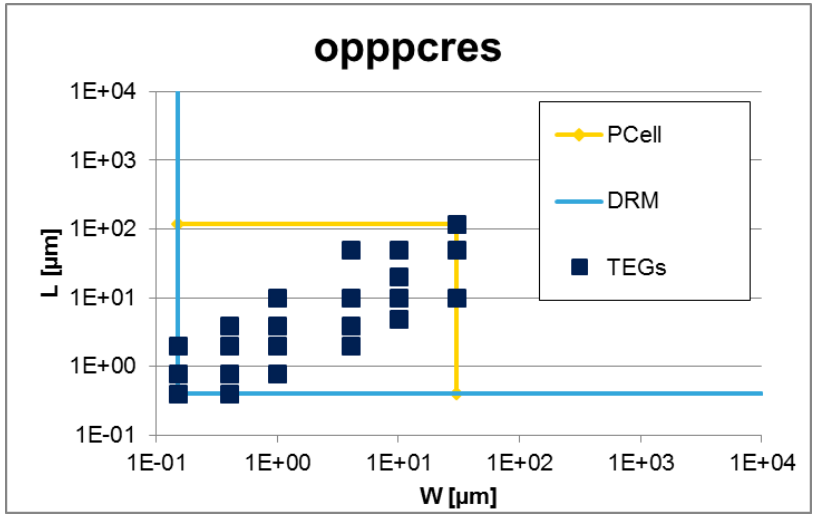
Resistors (2/3)

- Pins
  - Resistor is symmetrical and 3 pins device: Plus, Minus and one pin for substrate
  - Resistors can be built in the following flavors:
    - either Poly or OD (active), according to the layer in which they are fabricated
    - either N+ or P+, as to the doping type
    - either unsilicided or silicided, relying on the presence or not of the silicidation protection
- Model nomenclature
  - Table below contains all available models and their names. These models are related to all fully supported resistors:

Devices	Model name
N+ Non Silicided Active RESISTOR	OPNDRES
NWELL RESISTOR	NWRES
P+ Non Silicided Poly RESISTOR	OPPPCRES
	OPPPCRES_LC
RE P+ Non Silicided Poly RESISTOR	OPRERES

Resistors 3/3
Geometries used for extraction (poly res.)

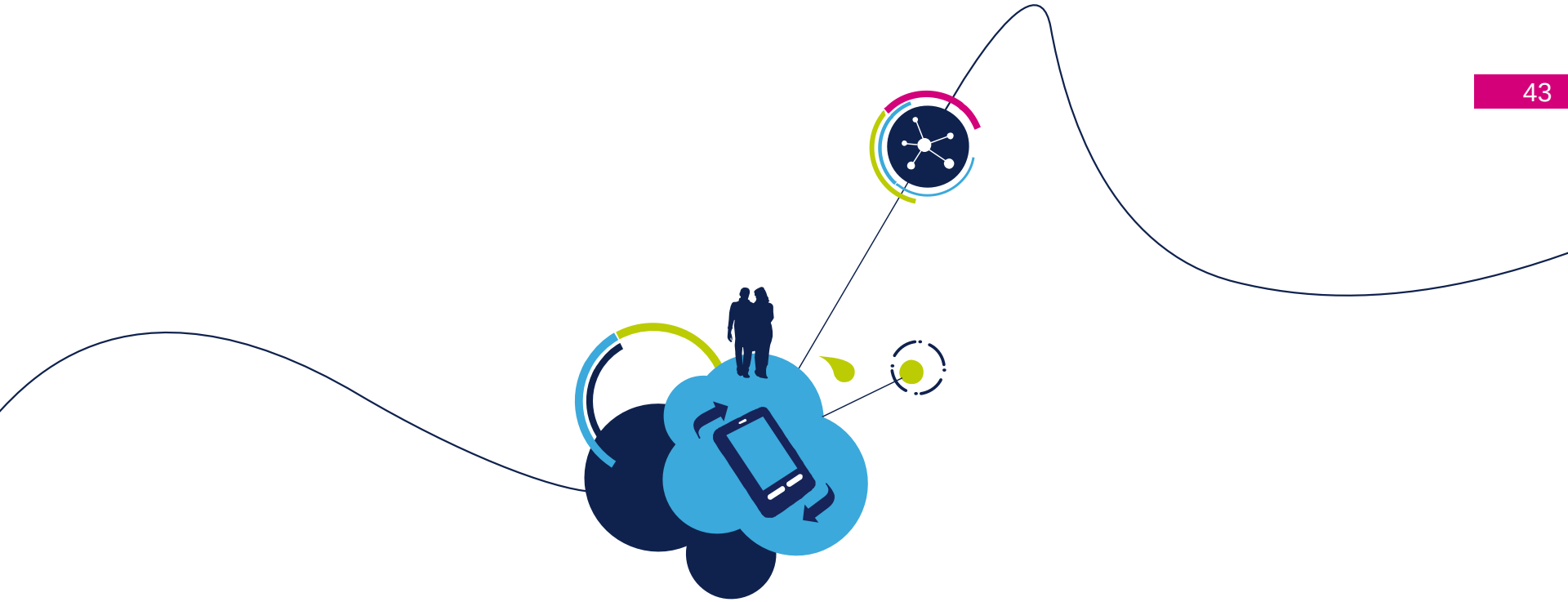




- No maximum given in DRM
- However, rule 132 may be applied
  - Gate maximum area: 38.661µm²
  - Despite poly resistor is not strictly speaking a gate
- Maximum available geometries
  - Wmax = 30µm
  - Lmax = 120µm
- Note: TEGs are test structures (Test Element Group)

Other references

- Other devices have dedicated documentation
  - Inductors: ind_hq.pdf, indsym_lohq.pdf
  - Examples of implementation of Transmission Lines: TLines.pdf
  - ESD devices: ESD_NMOS.pdf, ESD_Diodes.pdf
  - CMOM: cmom_rf_custom.pdf
- Documentation also includes comparison wrt. previous DK release



MOSFETs netlists examples

Monte Carlo simulation case (netlist example)


```
.include <eldolibpath>/soa_gflag.lib
.lib <eldolibpath>/common_feol.lib PRO_statmotherfab
.lib <eldolibpath>/common_fet.lib PRO_statmotherfab
.lib <eldolibpath>/matching.lib matching_XYPOS
.lib <eldolibpath>/RVT.lib rvt_TT
```

Library inclusion:
Stat corners are specified using common files

```
.param rvt_dev = 1
```

Flag definition for mismatch:
= 0: mismatch disabled
= 1: mismatch enabled

```
. param gflag__noisedev__rvt__cmos028fdsoi = 1
```

Flag definition for flicker noise:
= 0: LF noise variation disabled
= 1: LF noise variation enabled

```
xm1 d1 g 0 0 nfet_acc w=80e-9 l=30e-9
xm2 d2 g 0 0 nfet_acc w=80e-9 l=30e-9
vd d 0 1.0
Vd1 d1 d 0
Vd2 d2 d 0
vg g 0 1.0
.op
.mc 1000
.extract label=ion_m1 i(vd1)
.extract label=ion_m2 i(vd2)
```

Pre-defined corner case (netlist example)


```
.include <eldolibpath>/soa_gflag.lib
.lib <eldolibpath>/common_feol.lib PRO_FFF
.lib <eldolibpath>/common_fet.lib PRO_FFF
.lib <eldolibpath>/matching.lib matching_XYPOS
.lib <eldolibpath>/RVT.lib rvt_TT
```

Library inclusion:
Corners are specified using common files (see "Mosfet corners" section for all supported corners)

```
.param rvt_dev = 0
```

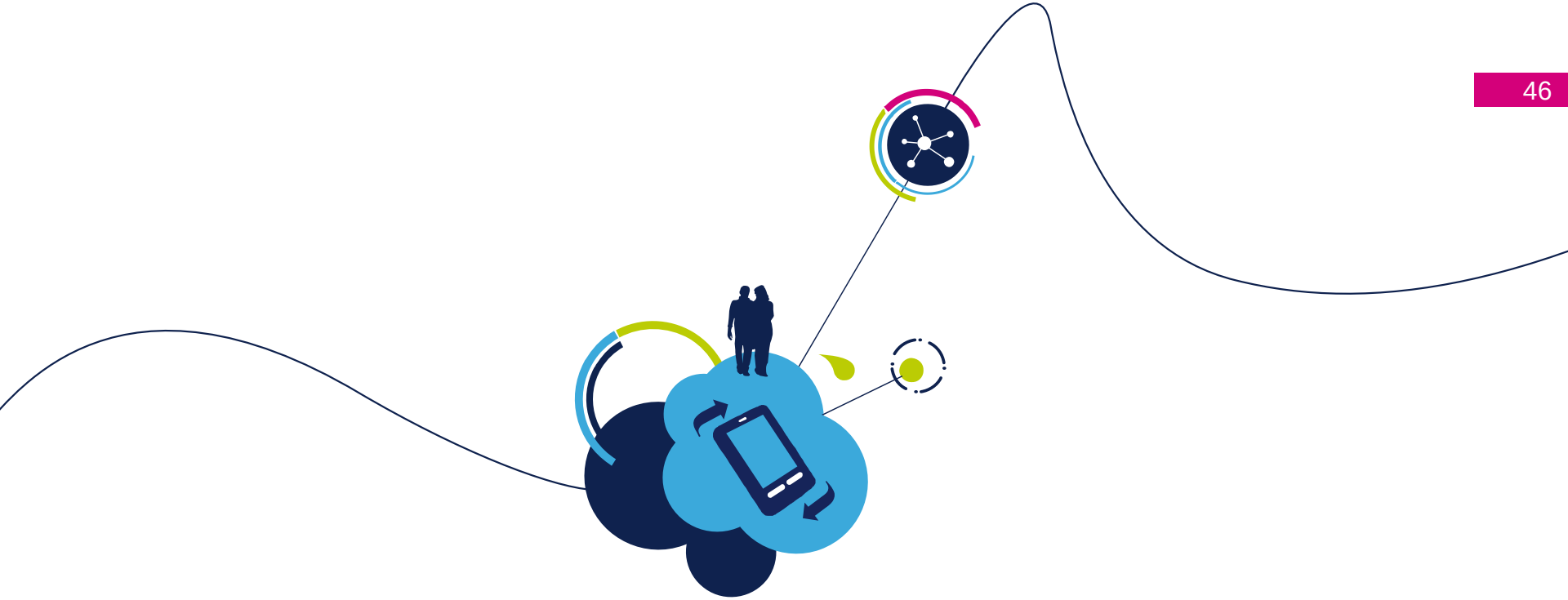
Flag definition for mismatch:
= 0: mismatch disabled
= 1: mismatch enabled (MC)

```
.param gflag__noisedev__rvt__cmos028fdsoi = 0
```

Flag definition for LF noise;
= 0: typical corner
= 1: Monte-carlo
= 2: worst case corner
= 3 : user corner
= 4: best case corner

```
xm1 d1 g 0 0 nfet_acc w=1e-6 l=30e-9
xm2 d2 g 0 0 nfet_acc w=1e-6 l=30e-9
vd d 0 1.0
Vd1 d1 d 0
Vd2 d2 d 0
vg g 0 1.0
.op
.extract label=ion_m1 i(vd1)
.extract label=ion_m2 i(vd2)
```

NOTE: all library files and switches/flags specified here are required for stand alone simulation. Please refer to previous slides for mismatch flags values



Non-FET models netlists examples

Netlist example for resistors – PDC case


```
.param .param rpolyp_dev = 1
```

Global flag definition:
= 0: mismatch disabled
= 1: mismatch enabled

```
.lib <eldolibpath>/resistor.lib rpolyp_rmin
.include <eldolibpath>/soa_gflag.lib
```

Library inclusion:
Corners are specified using resistor.lib library. Supported corners are:

- ✓ TT
- ✓ rmin
- ✓ rmax

```
xc1 110 0 0 opppcres w=1.5e-6 l=10e-6

R1  1   11    100
V1  11  110   0

vsweep 1 0 1.0

.dc temp  -38 152 5

.print dc i(V1)

.end
```

Netlist example for resistors – stat case


```
.param .param rpolyp_dev = 1
```

Global flag definition:
= 0: mismatch disabled
= 1: mismatch enabled

```
.lib <eldolibpath>/common_feol.lib PRO_statmotherfab
.lib <eldolibpath>/resistor.lib rpolyp_statmotherfab
 .include <eldolibpath>/soa_gflag.lib
```

Library inclusion:
Stat corner is specified using resistor.lib and common_feol.lib libraries.

```
xc1 110 0 0 opppcres w=1.5e-6 l=10e-6

R1  1   11     100
V1  11  110    0

vsweep 1 0 1.0

.dc temp  -38 152 5

.print dc i(V1)

.end
```

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Netlist example for CMOM – PDC case


```
.param CMOM_5U1X_2T8X_LB_DEV = 0
```

Global flag definition:
= 0: mismatch disabled

```
.lib <eldolibpath>/common_beol.lib PRO_CMIN
.lib <eldolibpath>/cmom.lib cmom_5u1x_2t8x_lb_TT
.include <eldolibpath>/soa_gflag.lib
```

Library inclusion:
Corners are specified using common_beol.lib library. Supported corners are:

- ✓ TT
- ✓ cmin
- ✓ cmax

```
xc1 11 12  cmom_5U1x_2T8x_LB_2p  nf_dirx=100.0 nf_diry=100
+ mtlfrbot=2.0 mtlfrtop=5.0 mtlconbot=2.0 mtlcontop=4.0
+ spacefinger_mx=1e-07 wfinger_mx=1e-07

V0 100 0 0

R1 1 11 1000
V1 1 100 0

R2 2 12 1000
V2 2 100 0

.dc V0 -1.8 1.8 0.1

.print dc i(V1) i(V2)
.end
```

Netlist example for CMOM – stat case


```
.param CMOM_5U1X_2T8X_LB_DEV = 1
```

Global flag definition:
= 0: mismatch disabled
= 1: mismatch enabled

```
.lib <eldolibpath>/common_beol.lib PRO_STATMOTHERFAB
.lib <eldolibpath>/cmom.lib cmom_5u1x_2t8x_lb_TT
.include <eldolibpath>/soa_gflag.lib
```

Library inclusion:
Corners are specified using common_beol.lib library. Supported corners are:

- ✓ TT
- ✓ cmin
- ✓ cmax

```
xc1 11 12  cmom_5U1x_2T8x_LB_2p  nf_dirx=100.0 nf_diry=100
+ mtlfrbot=2.0 mtlfrtop=5.0 mtlconbot=2.0 mtlcontop=4.0
+ spacefinger_mx=1e-07 wfinger_mx=1e-07

V0 100 0 0

R1 1 11 1000
V1 1 100 0

R2 2 12 1000
V2 2 100 0

.dc V0 -1.8 1.8 0.1

.print dc i(V1) i(V2)
.end
```

Netlist example for mosvar – PDC case


```
.ib <eldolibpath>/diode.lib diode_fast
.lib <eldolibpath>/EG_cpoly.lib egncap_cmin
.include <eldolibpath>/soa_gflag.lib
```

Library inclusion:
Corners are specified using EG_cpoly.lib library. Supported corners are:

- ✓ TT
- ✓ cmin
- ✓ cmax

```
xc1 11 12 0 egncap w=1e-6 l=1e-6
V0 100 0 0

R1 1 11 1000
V1 1 100 0

R2 2 12 1000
V2 2 100 0

.dc V0 -1.8 1.8 0.1

.print dc i(V1) i(V2)
.end
```

Netlist example for mosvar – stat case


```
.ib <eldolibpath>/diode.lib diode_fast
.lib <eldolibpath>/EG_cpoly.lib egncap_statmotherfab
.lib <eldolibpath>/ common_beol.lib PRO_statmotherfab
.lib <eldolibpath>/ common_feol.lib PRO_statmotherfab
.lib <eldolibpath>/ common_fet.lib PRO_statmotherfab
.include <eldolibpath>/soa_gflag.lib
```

Library inclusion:
Stat corner is specified using EG_cpoly.lib, common_beol, common_feol and common_fet libraries.

```
xc1 11 12 0 egncap w=1e-6 l=1e-6
V0 100 0 0

R1 1 11 1000
V1 1 100 0

R2 2 12 1000
V2 2 100 0

.dc V0 -1.8 1.8 0.1

.print dc i(V1) i(V2)
.end
```

life.augmented

Netlist example for diode


```
.lib <eldolibpath>/diode.lib diode_typ
.include <eldolibpath>/soa_gflag.lib
```

Library inclusion:
Corners are specified using diode.lib library. Supported corners are:

- ✓ diode_typ
- ✓ diode_fast
- ✓ diode_slow

```
XD1 1 0 diodednwx_lvs area=1e-12 perim=4e-6 dtemp=0
R1 1 2 1.0
Vd 2 0 0.0

.dc vd -1 0.8 0.05

.temp 70

.print dc i(vd)

.end
```

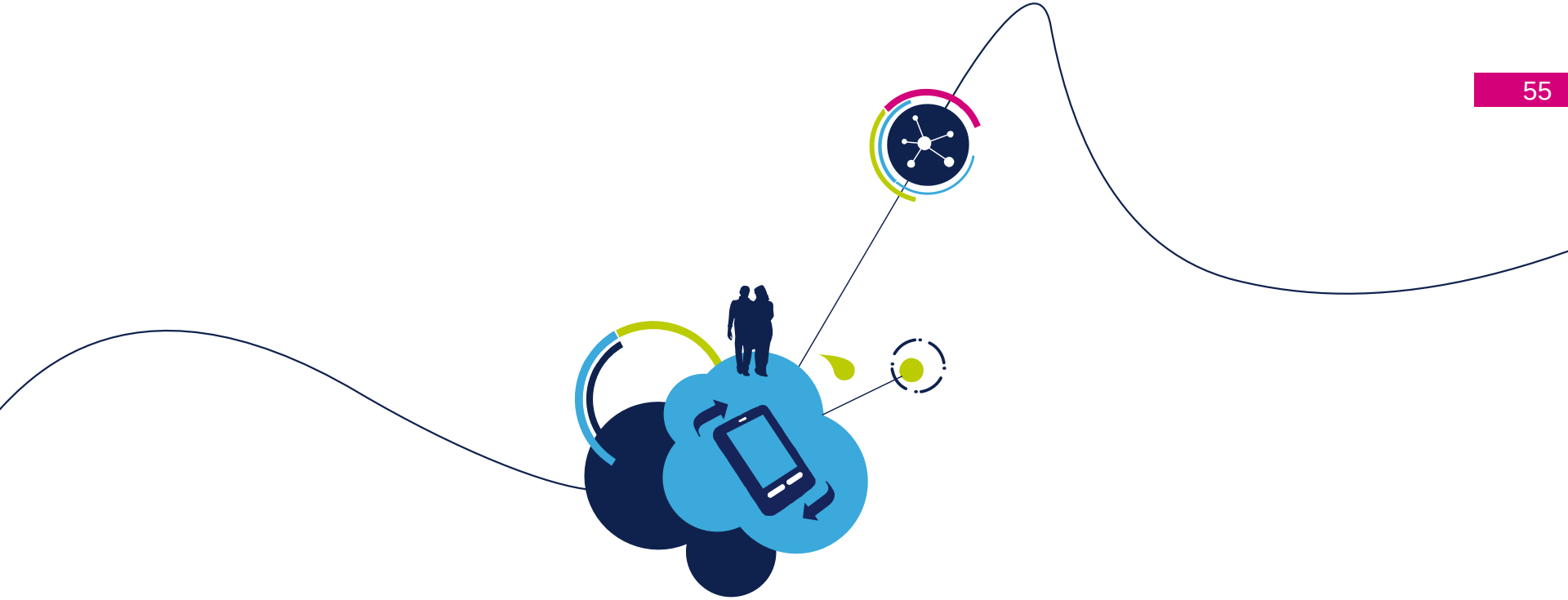
Netlist example for ESD diode


```
.lib " <eldolibpath>/esd_diode_gr_sti_hb.lib" grhcdsti_ESDBC
.lib " <eldolibpath>/common_esd.lib" PRO_ESDBC
. lib " <eldolibpath>/veriloga.lib veriloga_typ
```

Library inclusion:
Corners are specified using common_esd, library.
Supported corners are:

- ✓ TT
- ✓ ESDWC
- ✓ ESDBC
- ✓ USER
- ✓ statmotherfab

```
XD1 1 0 0 esdvpnp area=2e-12 perim=10.8e-6 w=5e-6 sac=0.077e-6 nf=10 areab=6.43e-11 perimb=3.31e-5 rwire=-1 rsx=0

R1 1 2 1.0
Vd 2 0 0.0

.dc vd -1 0.8 0.05

.temp 70

.print dc i(vd)

.end
```



Models limitations

LF noise corners in post-layout

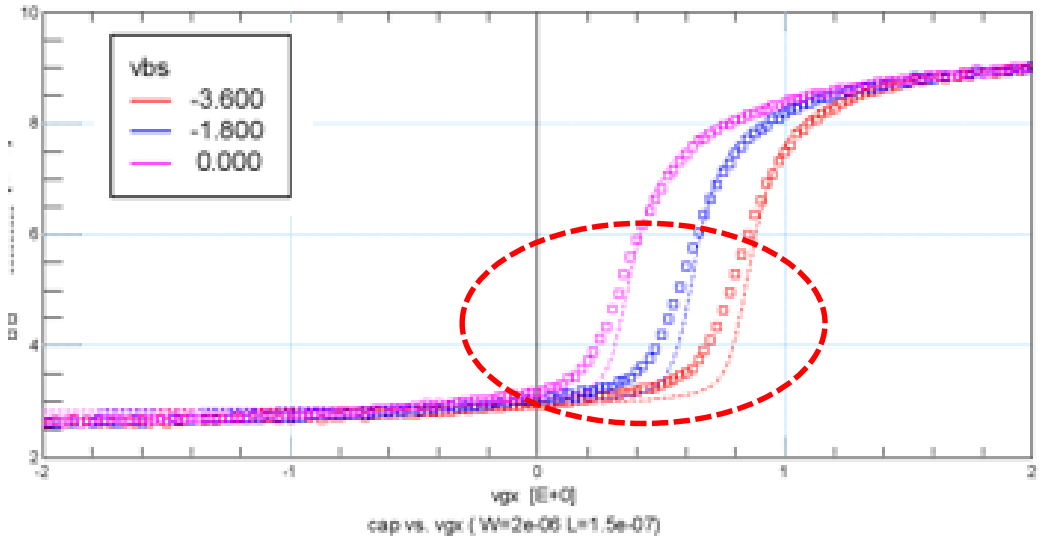
- Models: SG and EG MOS transistors

- Limitations: The corners defined for the LF noise do not take into account the variation reduction due to the multiplicity of the devices in post-layout simulation because LVS cannot extract the mult instance parameter

Limitations: modeling inaccuracy of EGRVT PFET capacitances

- Models: egpfet_acc, egvpfet_acc

- Limitations: the EG/EGV RVT pfet models do not simulate the Cg-ds capacitances around the threshold voltage inside the modeling accuracy tolerance of 5%.



Limitations: under-estimation of the saturation current for the RPO mosfets

- Context: The modeling of the RPO mosfets for the I/O applications are performed in the design-kit through the association of the mosfets accurate models with the corresponding unsalicided resistance (sblkndres/sblkpdres) models

- Limitations: The correlation between the simulation and the measurement shows an under-estimation of the saturation current by 7%.

Limitations: WPE default values are misaligned with default P-cell values

- Models: pfet_acc, eglvtnfet_acc, eglvtvnfet_acc, egpfet_acc, egvpfet_acc, pfet_rf, eglvtnfet_rf, eglvtvnfet_rf, pfet_rfseg, eglvtnfet_rfseg, eglvtvnfet_rfseg

- Limitations: the default value of the models in pre-layout assumes no WPE effect whereas the P-cell adds Nwell layer at the minimum DRM distance.

Limitations: modeling inaccuracy of LOD effect

- Models: egnfet_acc, egvnfet_acc, eglvtpfet_acc, eglvtvpfet_acc, eglvtpfet_rf, eglvtvpfet_rf, eglvtpfet_rfseg, eglvtvpfet_rfseg
- Limitation: The models under-estimate the linear and saturation currents by 5% at small SA and SB values (<0.4um) for narrow-short devices (W<0.3um, L< 0.5 um)
- Models: eglvtnfet_acc, eglvtvnfet_acc, eglvtnfet_rf, eglvtvnfet_rf, , eglvtnfet_rfseg, eglvtvnfet_rfseg, egpfet_acc, egvpfet_acc,
- Limitation: inaccurate stress STI modeling when nf>1 in pre-layout mode for large L
  - Please use post-layout simulation to recover accuracy

Limitations: Minimum leakage in CMIM16acc is wrongly setup

- Models: cmim16acc, cmim16acc_acc, cmim16acc_sh, cmim16acc_sh_acc, cmim16acc_2p, cmim16acc_2p_acc
- Limitations: the minimum leakage in CMIM16acc device is wrongly setup.
- Recommendation: We recommend to use the typical and maximum values

Limitations for non-Verilog-a ESD models

- Models: esdnfet_nova, esdegnfet_nova, esdvnpn_eg_nova, esdvpnp_eg_nova, esdndsx_eg_nova, esdvnpn_nova, esdvpnp_nova , esdndsx_nova, esdnfet, esdegnfet, esdvnpn_eg, esdvpnp_eg, esdndsx_eg, esdvnpn, esdvpnp , esdndsx

- Limitations:
  - Non-veriloga models are dedicated to SST simulation using Spectre or GoldenGate only. Veriloga models are strongly recommended for other simulators and other simulation analysis.
  - The SOA is implemented for the non-Verilog-a models

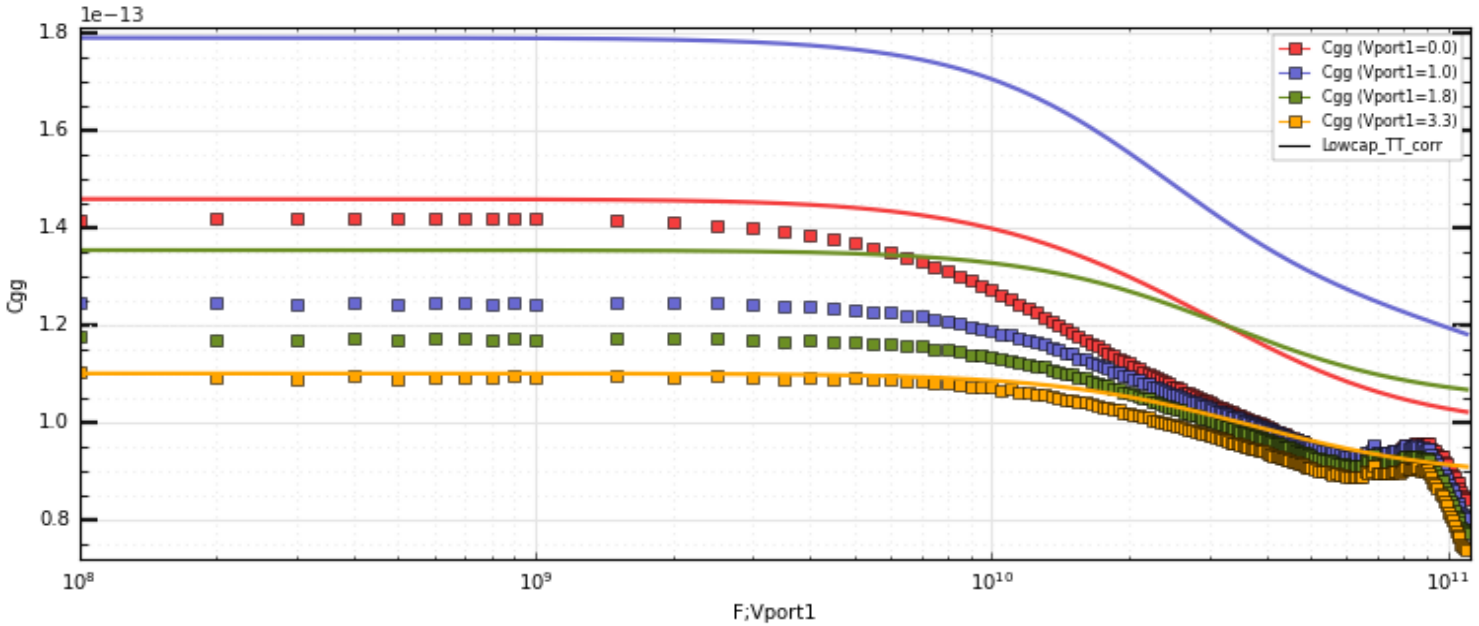
ESD diodes

- Models: esdvnpn_eg_va, esdvpnp_eg_va, esdndsx_eg_va, esdvnpn_va, esdvpnp_va , esdndsx_va,

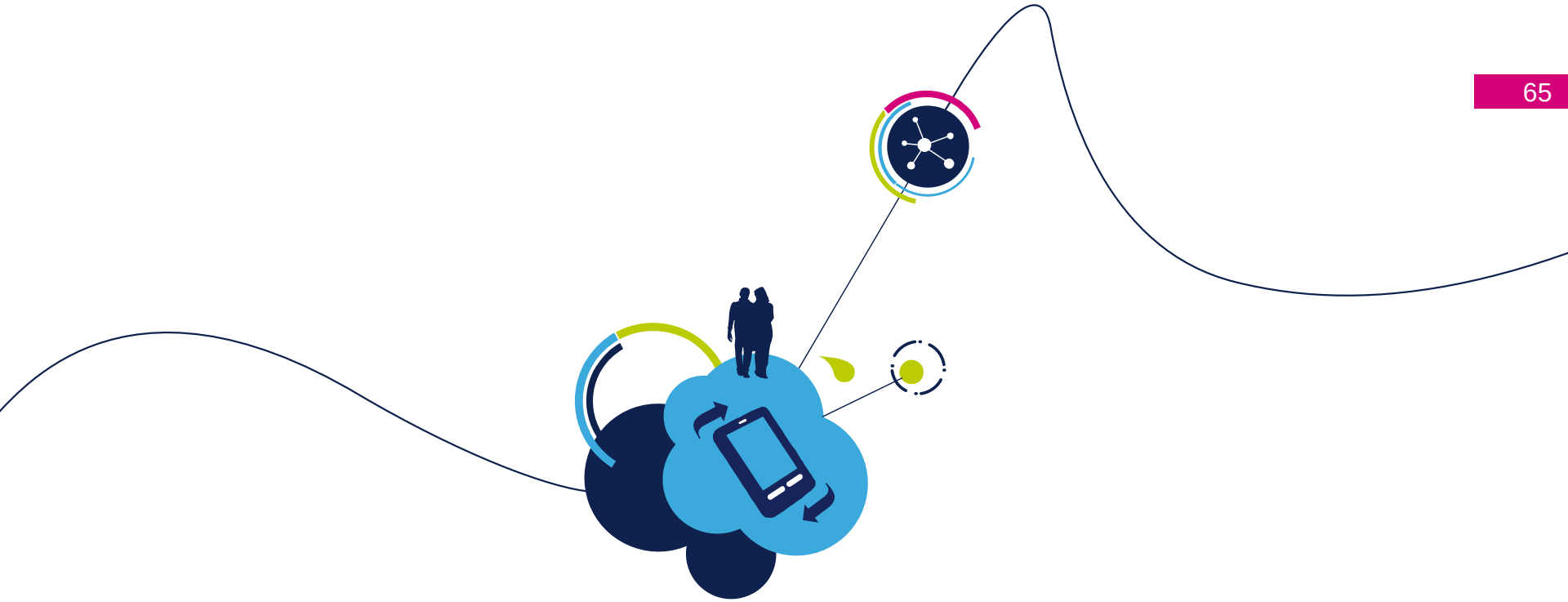
- Limitations:
  - Models were historically developed for ESD diodes PCELLs
  - Reference layouts for diodes are now the ones from ESDKIT library and ESD models are optimized for best describing diodes with these layouts.
  - Diodes layouts have diverged from PCELLs, and there might now be a miscorrelation between models and PCELLs for ESD behaviour.

ESD low-cap

- Models: esd_lowcap
- Limitations:
  - In AC signals, voltage dependence of capacitance is not accurately modeled. Model to measurement error is overestimated, by up to 40% at 1V.



Lowcap: C(f) from RF measurements for different voltage biases



Recommendations and KPS *(Known Problems and Solutions)*

KPS1: frequency dependent resistors support in Inductors and varactors using Spectre simulator

- Symptom
  - Transient (time domain) simulation limitations: incorrect parasitic resistance in inductors and varactors.
- Reason
  - Frequency dependent resistors support in Spectre ($freq based expressions).
- Workaround
  - NA
- Definitive solution
  - Cadence CCR# 1768638 (SR46133132)

KPS2: Simplified implementation of excess phase shift in VNPN bipolar in other simulators than ADS and AFS

- Symptom
  - Collector current oscillates around the correct behavior (reproduced by AFS and ADS) at high frequency (F > 1 GHz).
- Reason
  - To avoid using internal nodes (higher CPU time) in the Spice Gummel Poon model EDA vendors implemented a simplified version with above limitation at high frequency (related to excess phase shift parameter “ptf”).
- Workaround
  - NA
- Definitive solution
  - Keysight ticket:EESOFADS-7823
  - Mentor G.: Service Request 3149512361

KPS3: PSP model version control in AFS and Golden Gate simulators

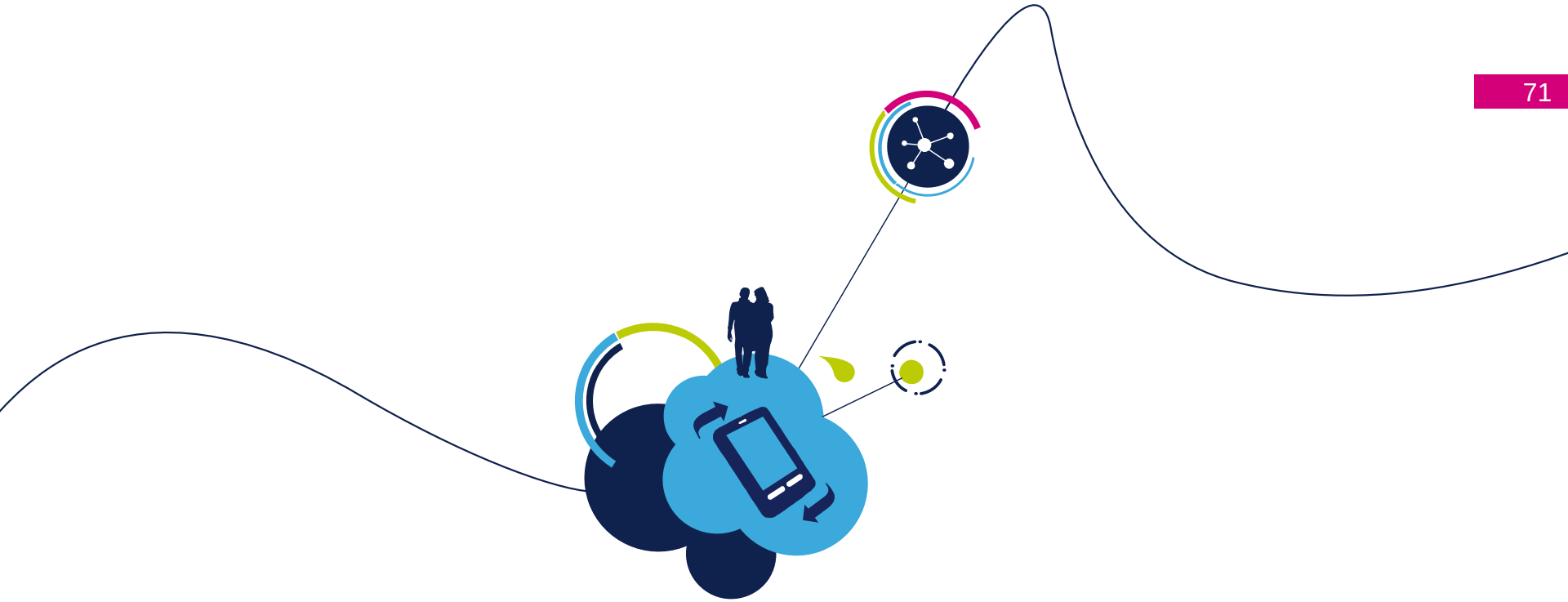
- Symptom
  - PSP 103.5 is automatically used while model card is specifying other version (103.3)
- Reason
  - AFS, ADS and Golden Gate simulators base their PSP implementation on NXP SimKit witch only includes one version of the model.
- Workaround
  - NA
- Definitive solution
  - Mentor G. and Keysight are aware of this limitations and working on a fix.
  - Keysight ticket: TFS ID 114070

KPS4: Voltage dependent resistor support in varactor in AFS and ADS simulator

- Symptom
  - Access resistance is overestimated at lower frequency.
- Reason
  - Support of voltage dependent resistors in AFS and ADS.
- Workaround:
  - NA
- Definitive solution
  - Mentor G. (AFS): TICKET SR 3147933721
  - Keysight: Ticket:EEESOFADS-7824

KPS5: ESD ULC EG temperature dependence issue makes current underestimated in Spectre and Hspice

- Symptom:
  - Current is underestimated in Spectre / Hspice versus ELDO simulator especially for low temperatures. ELDO is reproducing correct values for all temperatures.
- Workaround:
  - Investigation is ongoing to understand the temperature dependence limitation in Spectre and Hspice.
- Solution:
  - To be communicated as soon as possible.



Documentation history

Document history

Version	Date	Authors	Comments
1	July 13th, 2011	Salim EL GHOULI	Initial release (10ML metal option package)
2	September 1st, 2011	Salim EL GHOULI	Standalone package (10ML metal option package)
3	September 28th, 2011	Salim EL GHOULI	package with new Eldo fully integrated UTSOI and new XA support
4	November 4th, 2011	Salim EL GHOULI	package with new Eldo and Hspice (XA-eldo) fully integrated UTSOI v0.04b
5	December 2th , 2011	Salim EL GHOULI	package with new Eldo fully integrated UTSOI v0.05
6	December 14th , 2011	Salim EL GHOULI	package with Eldo & Hspice fully integrated UTSOI v0.05
7	February 17th, 2012	Salim EL GHOULI	package for a silicon based V0.1 model. UTSOI V1.12 (new version) has been used
8	March 11th, 2012	Salim EL GHOULI	package for a silicon based V0.2 model
9	March 13th, 2012	Salim EL GHOULI & Benoit LEGOIX	package for a silicon based V0.2 model patch1 (ESD corners issue)
10	April 13th, 2012	Salim EL GHOULI & Benoit LEGOIX	package for SRAM delivery
11	April 17th, 2012	Salim EL GHOULI & Benoit LEGOIX	SRAMs update
12	October 2nd, 2012	Salim EL GHOULI & Benoit LEGOIX	package for updated models based on new silicon (DK2_2 is targeted)
13	November 23th, 2012	Salim EL GHOULI & Benoit LEGOIX	Alignment with last hardware measurement, DSV and LSP sram devices added
14	January 30th, 2013	Salim EL GHOULI & Benoit LEGOIX	7ML model package version with Spectre models (DK2.2.1)
15	May 31th, 2013	Salim EL GHOULI & Benoit LEGOIX	new SRAM cell and model fixes (DK2.3 prod)
16	August 6th, 2013	Salim EL GHOULI & Benoit LEGOIX	for DK2.3.1
17	November 18th, 2013	Salim EL GHOULI & C. Charbuillet	for DK2.4
18	December 9th, 2013	S. EL GHOULI & C. Charbuillet	EG Mosfets, OPRE resistor and Cmim capacitor updates (DK2.4)
19	March 5th, 2014	S. EL GHOULI & C. Charbuillet	For DK2.5
20	April 23d, 2014	S. EL GHOULI	KPS and simulators update
21	May 23d, 2014	S. EL GHOULI	KPS and simulators update
22	June 6th, 2014	S. EL GHOULI & C. Charbuillet	EG2 models and Simulators list
23	July 4th, 2014	S. EL GHOULI & Jean REMY	EG, EGLVT, LVT and RVT models update + SOA update
24	September 25th, 2014	S. EL GHOULI & C. Charbuillet	Remove EG2 and LSH for DK2.5.d
25	November 28th, 2014	S. EL GHOULI, B. LEGOIX, C. CHARBUILLET	UTSOI2.00 usage – engineering models
26	December 24th, 2014	S. EL GHOULI & C. CHARBUILLET	Dc OP fix and other updates
27	January 28th, 2015	C. CHARBUILLET	Add mismatch global parameter eglvtps_dev
28	April 3rd , 2015	S. EL-GHOULI, C. CHARBUILLET, B. LEGOIX	V1.1 eng2 model package
29	May 26th , 2015	S. EL-GHOULI, C. CHARBUILLET	V1.1 eng2.1 model package
30	May 24th , 2015	S. EL-GHOULI, C. CHARBUILLET	V1.1 eng2.2 model package
31	November 20th , 2015	C. CHARBUILLET	DK2.7.a
32	Match 23rd, 2016	C. CHARBUILLET, P. SCHEER	DK2.8
33	October 2016	C. CHARBUILLET	DK2.9
34	April 14th, 2017	S. EL-GHOULI	DK3.0 pre-QA
35	April 28th, 2017	M. MINONDO	DK3.0 model package for IA
36	May 24th, 2017	S. EL GHOULI	RF mmW DK0.9 as an update of the standard 28FD DK2.9 RF part
37	August 10th ,2017	G. GOUGET	DK1.0 RF_mmW model package for IA of SG RVT

Document history (2/2)

Version	Date	Authors	Comments
38	September 1st, 2017	Gilles GOUGET	DK1.0 RF_mmW prelim model package with V1.2 SG RVT accurate model
39	October 05th 2017	S. EL-GHOULI, G. GOUGET	Update for DK1.0 RF_mmW prod model package
40	October 10th 2017	G. GOUGET	Correction for DK1.0 RF_mmW prod model package
41	June 4th 2018	G. GOUGET	First update for Dk1.1
42	July 3rd 2018	G. GOUGET	Model Limitations update
43	September 24th 2018	B. DORMIEU	Lmax anf Wmax update
44	September 28th 2018	B. DORMIEU	Update kps5