C28SOI_SC_12_COREPBP10_LR Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 10 nm

Overview

- C28SOI_SC_12_COREPBP10_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

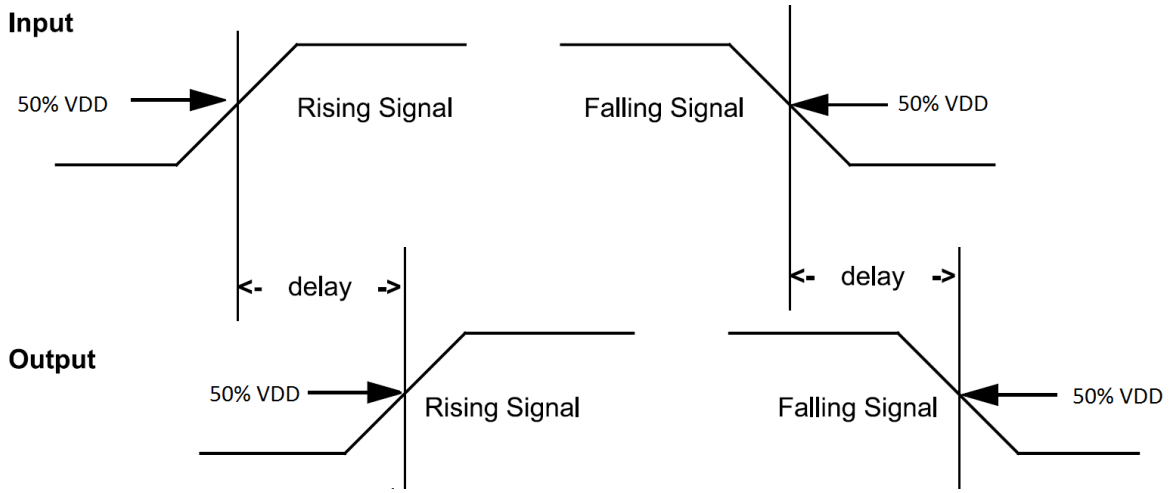


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

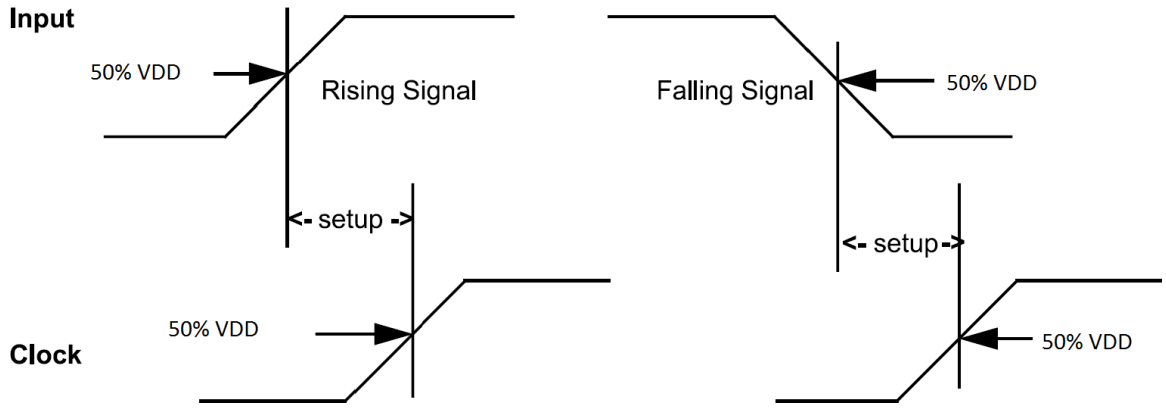


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

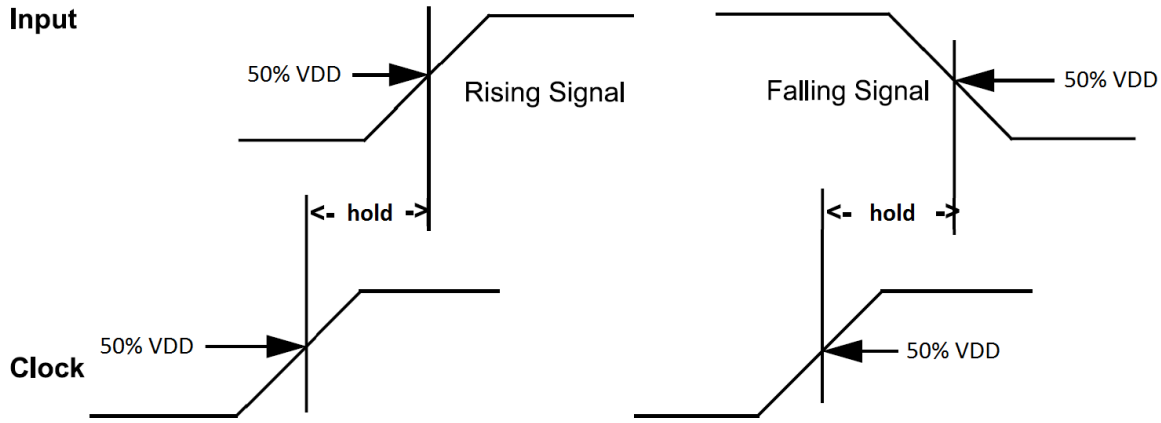


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

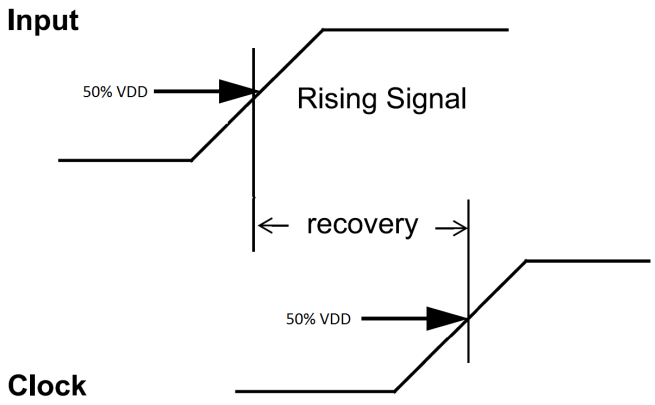


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

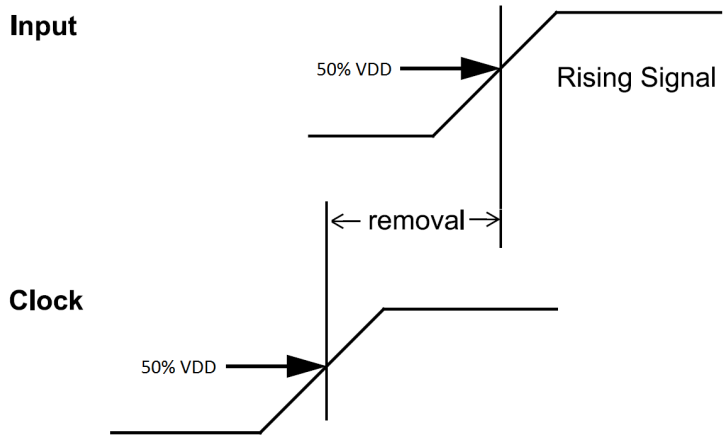


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

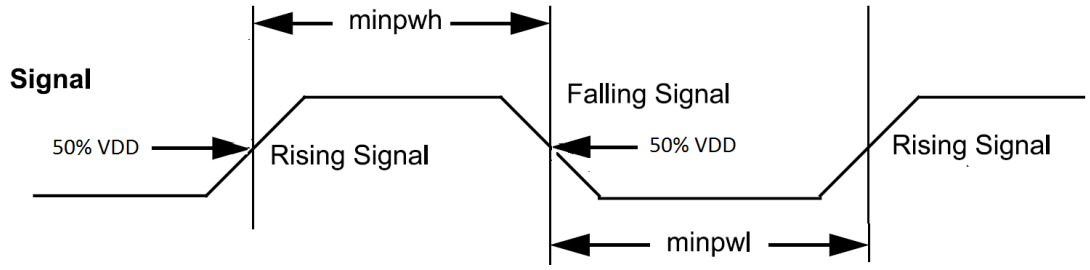


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

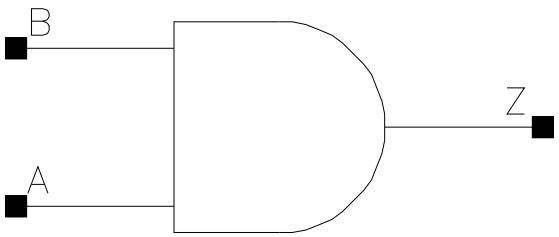
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X25_P10	1.200	1.088	1.3056
X33_P10	1.200	1.360	1.6320
X42_P10	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0007	0.0011	0.0016	0.0020
B	0.0006	0.0010	0.0015	0.0019
	X42_P10			
A	0.0019			
B	0.0019			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0484	0.0393	2.7585	1.4010
A to Z ↑	0.0393	0.0354	4.9943	2.4294
B to Z ↓	0.0462	0.0373	2.7540	1.4000
B to Z ↑	0.0405	0.0362	4.9961	2.4309
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0404	0.0388	0.9283	0.6879

A to Z ↑	0.0350	0.0353	1.6015	1.2059
B to Z ↓	0.0385	0.0360	0.9272	0.6870
B to Z ↑	0.0359	0.0351	1.6027	1.2070
	X42_P10		**X42_P10**	
A to Z ↓	0.0417		0.5600	
A to Z ↑	0.0382		0.9665	
B to Z ↓	0.0389		0.5593	
B to Z ↑	0.0382		0.9664	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	6.903e-07	8.218e-10
X16_P10	1.275e-06	9.409e-10
X25_P10	1.853e-06	1.298e-09
X33_P10	2.554e-06	1.536e-09
X42_P10	2.867e-06	1.655e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	1.118e-05	2.139e-05	3.317e-05	7.624e-05
B (output stable)	2.736e-05	5.276e-05	8.351e-05	3.180e-04
A to Z	1.855e-03	3.004e-03	4.607e-03	6.033e-03
B to Z	1.747e-03	2.805e-03	4.299e-03	5.410e-03
	X42_P10			
A (output stable)	7.658e-05			
B (output stable)	3.195e-04			
A to Z	7.194e-03			
B to Z	6.563e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

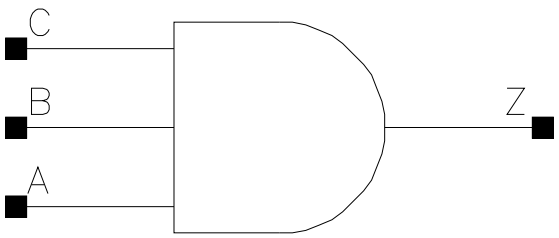
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	6.179e-08	7.230e-09	-2.880e-08	-4.420e-08
B (output stable)	2.990e-08	-1.265e-08	-6.510e-08	-1.013e-07
A to Z	-1.926e-07	-3.325e-07	-1.902e-07	-4.484e-07
B to Z	-1.083e-07	-1.714e-07	-4.878e-07	-3.637e-07
	X42_P10			
A (output stable)	-4.150e-08			
B (output stable)	-1.020e-07			
A to Z	-1.071e-06			
B to Z	-8.400e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X25_P10	1.200	1.360	1.6320
X33_P10	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0007	0.0010	0.0017	0.0020
B	0.0006	0.0010	0.0015	0.0019
C	0.0006	0.0010	0.0014	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0522	0.0427	2.7955	1.3655
A to Z ↑	0.0526	0.0465	5.0423	2.4058
B to Z ↓	0.0506	0.0411	2.7912	1.3653
B to Z ↑	0.0522	0.0467	5.0435	2.4045
C to Z ↓	0.0487	0.0391	2.7888	1.3632
C to Z ↑	0.0529	0.0462	5.0442	2.4077
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0432	0.0409	0.9384	0.7016

A to Z ↑	0.0465	0.0442	1.6366	1.2266
B to Z ↓	0.0416	0.0392	0.9372	0.7007
B to Z ↑	0.0466	0.0442	1.6368	1.2264
C to Z ↓	0.0396	0.0374	0.9365	0.7002
C to Z ↑	0.0464	0.0442	1.6380	1.2275

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	5.363e-07	9.409e-10
X17_P10	1.037e-06	1.060e-09
X25_P10	1.488e-06	1.536e-09
X33_P10	1.973e-06	1.655e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	1.107e-05	2.202e-05	2.912e-05	3.977e-05
B (output stable)	2.928e-05	5.947e-05	8.396e-05	1.154e-04
C (output stable)	5.990e-05	1.176e-04	1.724e-04	2.382e-04
A to Z	2.040e-03	3.470e-03	5.076e-03	6.495e-03
B to Z	1.930e-03	3.285e-03	4.790e-03	6.106e-03
C to Z	1.846e-03	3.083e-03	4.495e-03	5.709e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

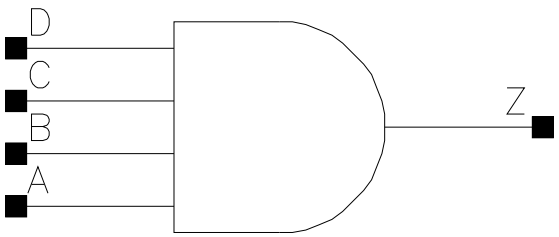
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	5.928e-08	1.042e-08	-3.830e-08	-6.050e-08
B (output stable)	4.578e-08	-1.223e-09	-3.487e-08	-7.680e-08
C (output stable)	5.393e-08	6.400e-10	-4.080e-08	-8.277e-08
A to Z	-1.115e-08	-1.857e-07	-1.616e-07	-4.920e-07
B to Z	-9.394e-08	-3.241e-07	-8.377e-07	-4.122e-07
C to Z	-7.971e-08	-1.568e-07	-2.376e-07	-7.325e-07

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X6_P10	1.200	1.088	1.3056
X20_P10	1.200	2.312	2.7744
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P10	X6_P10	X20_P10	X27_P10
A	0.0005	0.0008	0.0017	0.0019
B	0.0005	0.0007	0.0017	0.0019
C	0.0004	0.0008	0.0017	0.0019
D	0.0005	0.0007	0.0017	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X6_P10	X4_P10	X6_P10
A to Z ↓	0.0572	0.0467	5.3005	3.4042
A to Z ↑	0.0584	0.0427	19.9817	10.4960
B to Z ↓	0.0559	0.0441	5.3042	3.4022
B to Z ↑	0.0597	0.0434	20.0105	10.4894
C to Z ↓	0.0594	0.0500	5.2837	3.4262
C to Z ↑	0.0569	0.0410	20.0122	10.5156

D to Z ↓	0.0580	0.0468	5.2859	3.4229
D to Z ↑	0.0593	0.0418	20.0268	10.5219
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0444	0.0416	0.9880	0.6981
A to Z ↑	0.0427	0.0476	3.4749	2.6301
B to Z ↓	0.0407	0.0388	0.9858	0.6970
B to Z ↑	0.0423	0.0476	3.4759	2.6325
C to Z ↓	0.0435	0.0401	0.9965	0.7029
C to Z ↑	0.0371	0.0399	3.4796	2.6314
D to Z ↓	0.0398	0.0373	0.9945	0.7008
D to Z ↑	0.0367	0.0399	3.4807	2.6314

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	4.747e-07	1.298e-09
X6_P10	1.026e-06	1.298e-09
X20_P10	2.783e-06	2.370e-09
X27_P10	3.121e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	3.407e-04	5.206e-04	1.516e-03	1.878e-03
B (output stable)	3.187e-04	4.729e-04	1.396e-03	1.751e-03
C (output stable)	3.295e-04	5.348e-04	1.348e-03	1.665e-03
D (output stable)	3.123e-04	4.832e-04	1.198e-03	1.481e-03
A to Z	1.391e-03	2.134e-03	6.361e-03	8.264e-03
B to Z	1.324e-03	1.996e-03	5.765e-03	7.667e-03
C to Z	1.352e-03	2.135e-03	5.335e-03	6.590e-03
D to Z	1.290e-03	1.988e-03	4.735e-03	5.965e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

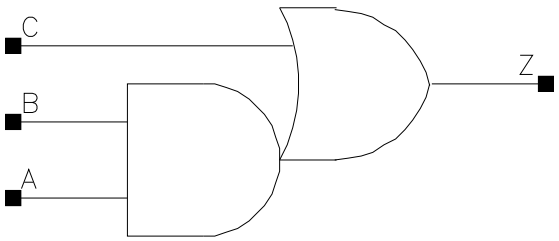
Pin Cycle (vdds)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	-5.011e-07	-7.615e-07	-3.681e-06	-6.752e-06
B (output stable)	-4.510e-07	-6.390e-07	-3.370e-06	-7.333e-06
C (output stable)	4.859e-06	8.750e-06	2.860e-05	5.182e-05
D (output stable)	4.390e-06	8.592e-06	2.176e-05	3.614e-05
A to Z	-2.780e-07	-4.489e-07	-2.355e-06	-5.283e-06
B to Z	-1.751e-07	-1.834e-07	-2.567e-06	-5.100e-06
C to Z	-1.349e-07	-3.283e-07	-1.198e-06	-1.444e-06
D to Z	-1.228e-07	-2.513e-07	-8.832e-07	-9.852e-07

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0009	0.0019
B	0.0006	0.0010	0.0017
C	0.0007	0.0010	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0644	0.0562	2.8599	1.3998
A to Z ↑	0.0407	0.0352	4.8795	2.3876
B to Z ↓	0.0601	0.0524	2.8519	1.3958
B to Z ↑	0.0423	0.0369	4.8754	2.3855
C to Z ↓	0.0652	0.0574	2.8428	1.3922
C to Z ↑	0.0350	0.0321	4.8513	2.3729
	X33_P10		**X33_P10**	
A to Z ↓	0.0560		0.7083	
A to Z ↑	0.0356		1.2007	

B to Z ↓	0.0518		0.7078	
B to Z ↑	0.0363		1.2003	
C to Z ↓	0.0567		0.7057	
C to Z ↑	0.0313		1.1948	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	9.838e-07	9.409e-10
X17_P10	1.830e-06	1.060e-09
X33_P10	3.673e-06	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	7.211e-06	1.379e-05	3.732e-05
B (output stable)	1.884e-05	2.937e-05	1.074e-04
C (output stable)	5.272e-05	9.112e-05	2.080e-04
A to Z	1.872e-03	3.149e-03	6.182e-03
B to Z	1.770e-03	2.956e-03	5.681e-03
C to Z	2.102e-03	3.563e-03	6.946e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

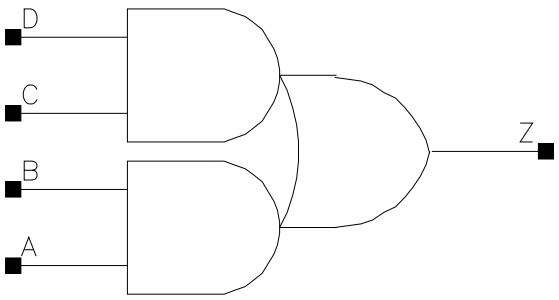
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	4.674e-06	1.246e-05	1.976e-05
B (output stable)	1.384e-05	2.335e-05	4.369e-05
C (output stable)	-5.115e-06	-6.814e-06	-1.358e-05
A to Z	-2.616e-07	-5.215e-07	-1.137e-06
B to Z	-1.133e-07	-2.148e-07	-5.614e-07
C to Z	-2.647e-06	-2.915e-06	-5.229e-06

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0009	0.0018
B	0.0007	0.0010	0.0017
C	0.0006	0.0009	0.0019
D	0.0006	0.0010	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0757	0.0648	2.7445	1.3820
A to Z ↑	0.0507	0.0444	4.8044	2.3887
B to Z ↓	0.0710	0.0609	2.7316	1.3770
B to Z ↑	0.0512	0.0455	4.8083	2.3906

C to Z ↓	0.0660	0.0576	2.7332	1.3770
C to Z ↑	0.0439	0.0387	4.7944	2.3829
D to Z ↓	0.0634	0.0549	2.7264	1.3749
D to Z ↑	0.0460	0.0404	4.7985	2.3821
	X33_P10		**X33_P10**	
A to Z ↓	0.0610		0.7089	
A to Z ↑	0.0406		1.2060	
B to Z ↓	0.0580		0.7077	
B to Z ↑	0.0422		1.2074	
C to Z ↓	0.0541		0.7072	
C to Z ↑	0.0359		1.2027	
D to Z ↓	0.0509		0.7063	
D to Z ↑	0.0371		1.2020	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.025e-06	1.179e-09
X17_P10	1.929e-06	1.298e-09
X33_P10	3.516e-06	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.702e-05	4.065e-05	6.432e-05
B (output stable)	1.187e-04	1.472e-04	1.009e-04
C (output stable)	1.234e-05	2.306e-05	4.619e-05
D (output stable)	2.201e-05	4.244e-05	8.896e-05
A to Z	2.509e-03	4.137e-03	7.583e-03
B to Z	2.318e-03	3.863e-03	7.171e-03
C to Z	2.084e-03	3.472e-03	6.269e-03
D to Z	1.998e-03	3.291e-03	5.868e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

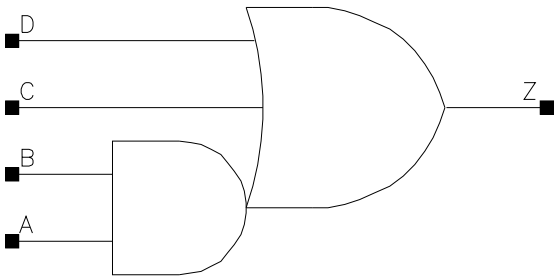
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-5.286e-07	-8.573e-07	-2.319e-06
B (output stable)	-1.669e-06	-9.127e-07	-2.363e-06
C (output stable)	3.333e-06	9.363e-06	2.011e-05
D (output stable)	3.518e-06	9.379e-06	1.968e-05
A to Z	-1.255e-06	-1.422e-06	-3.739e-06
B to Z	-1.305e-06	-1.247e-06	-3.209e-06
C to Z	-1.956e-07	-3.083e-07	-5.641e-07
D to Z	-2.206e-07	-1.305e-07	-4.501e-07

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	0.952	1.1424
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0009	0.0017
B	0.0006	0.0009	0.0017
C	0.0006	0.0009	0.0017
D	0.0006	0.0009	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0877	0.0738	3.0363	1.4857
A to Z ↑	0.0437	0.0377	4.8687	2.4593
B to Z ↓	0.0841	0.0688	3.0268	1.4814
B to Z ↑	0.0456	0.0388	4.8688	2.4563
C to Z ↓	0.0964	0.0817	3.0194	1.4796
C to Z ↑	0.0376	0.0339	4.8383	2.4472

D to Z ↓	0.0935	0.0801	3.0212	1.4800
D to Z ↑	0.0373	0.0337	4.8344	2.4436
	X33_P10		**X33_P10**	
A to Z ↓	0.0743		0.7437	
A to Z ↑	0.0376		1.2032	
B to Z ↓	0.0666		0.7392	
B to Z ↑	0.0377		1.2017	
C to Z ↓	0.0822		0.7394	
C to Z ↑	0.0329		1.1980	
D to Z ↓	0.0792		0.7396	
D to Z ↑	0.0321		1.1952	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.011e-06	1.060e-09
X17_P10	1.924e-06	1.179e-09
X33_P10	3.945e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	3.756e-06	7.804e-06	2.559e-05
B (output stable)	7.653e-06	1.460e-05	7.116e-05
C (output stable)	7.821e-05	1.304e-04	3.655e-04
D (output stable)	9.893e-06	1.640e-05	4.124e-05
A to Z	2.046e-03	3.337e-03	6.646e-03
B to Z	1.961e-03	3.133e-03	6.005e-03
C to Z	2.406e-03	3.986e-03	8.013e-03
D to Z	2.256e-03	3.730e-03	7.315e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

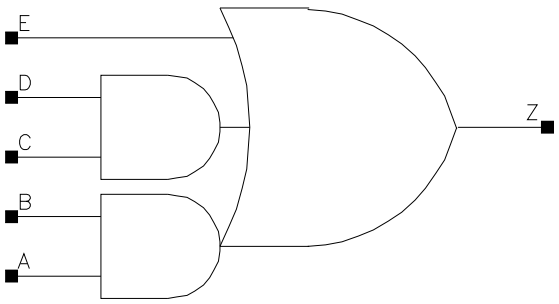
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	4.325e-06	1.095e-05	1.761e-05
B (output stable)	8.979e-06	1.978e-05	3.205e-05
C (output stable)	-1.359e-05	-2.084e-05	-5.666e-05
D (output stable)	5.966e-06	1.295e-05	3.468e-05
A to Z	-2.226e-07	-6.070e-07	-7.445e-07
B to Z	-3.100e-07	-1.612e-07	-7.209e-07
C to Z	-3.827e-06	-5.236e-06	-1.332e-05
D to Z	-2.679e-06	-3.039e-06	-6.136e-06

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.088	1.3056
X17_P10	1.200	1.224	1.4688
X33_P10	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0009	0.0018
B	0.0006	0.0009	0.0017
C	0.0007	0.0011	0.0018
D	0.0006	0.0009	0.0017
E	0.0006	0.0009	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.1115	0.0923	2.8923	1.4367
A to Z ↑	0.0530	0.0445	4.7838	2.4018

B to Z ↓	0.1078	0.0880	2.8818	1.4327
B to Z ↑	0.0556	0.0463	4.7812	2.4017
C to Z ↓	0.0909	0.0764	2.8749	1.4301
C to Z ↑	0.0462	0.0384	4.7410	2.3856
D to Z ↓	0.0848	0.0698	2.8627	1.4241
D to Z ↑	0.0478	0.0396	4.7390	2.3852
E to Z ↓	0.0970	0.0804	2.8555	1.4230
E to Z ↑	0.0393	0.0337	4.7022	2.3702
	X33_P10		**X33_P10**	
A to Z ↓	0.0901		0.7432	
A to Z ↑	0.0453		1.2124	
B to Z ↓	0.0848		0.7408	
B to Z ↑	0.0467		1.2125	
C to Z ↓	0.0733		0.7398	
C to Z ↑	0.0381		1.2024	
D to Z ↓	0.0671		0.7368	
D to Z ↑	0.0390		1.2028	
E to Z ↓	0.0780		0.7361	
E to Z ↑	0.0333		1.1948	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.187e-06	1.298e-09
X17_P10	2.215e-06	1.417e-09
X33_P10	4.017e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.996e-05	3.318e-05	7.467e-05
B (output stable)	3.520e-05	4.313e-05	1.144e-04
C (output stable)	1.207e-05	1.763e-05	4.672e-05
D (output stable)	1.598e-05	2.831e-05	8.115e-05
E (output stable)	6.329e-05	6.465e-05	1.710e-04
A to Z	2.866e-03	4.529e-03	8.809e-03
B to Z	2.790e-03	4.331e-03	8.291e-03
C to Z	2.208e-03	3.505e-03	6.718e-03
D to Z	2.102e-03	3.283e-03	6.204e-03
E to Z	2.470e-03	3.893e-03	7.466e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-2.537e-06	-3.796e-06	-8.441e-06
B (output stable)	-4.550e-06	-4.473e-06	-1.045e-05
C (output stable)	6.921e-06	1.549e-05	3.323e-05
D (output stable)	8.634e-06	2.163e-05	4.273e-05
E (output stable)	3.775e-06	1.406e-05	2.210e-05
A to Z	-5.048e-06	-4.873e-06	-9.628e-06
B to Z	-4.911e-06	-4.366e-06	-9.093e-06
C to Z	-2.813e-07	-5.551e-07	-1.176e-06
D to Z	-1.712e-07	-3.224e-07	-6.837e-07

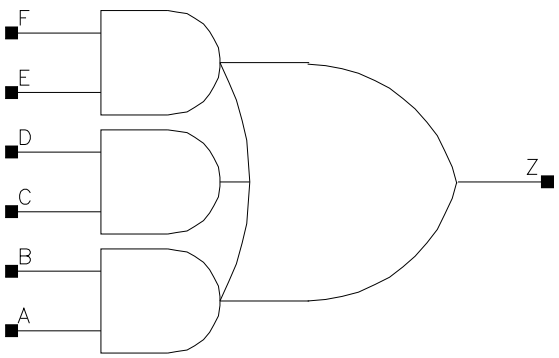
E to Z	-2.594e-06	-2.343e-06	-5.816e-06

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.360	1.6320
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
A	0.0006	0.0007	0.0009	0.0018

B	0.0006	0.0007	0.0012	0.0016
C	0.0006	0.0007	0.0009	0.0018
D	0.0006	0.0007	0.0009	0.0016
E	0.0006	0.0007	0.0009	0.0018
F	0.0006	0.0007	0.0009	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.1118	0.1037	5.5919	2.8590
A to Z ↑	0.0564	0.0530	9.7731	4.8567
B to Z ↓	0.1035	0.0965	5.5570	2.8428
B to Z ↑	0.0564	0.0535	9.7685	4.8537
C to Z ↓	0.1008	0.0942	5.5716	2.8494
C to Z ↑	0.0517	0.0486	9.7123	4.8238
D to Z ↓	0.0966	0.0903	5.5497	2.8390
D to Z ↑	0.0539	0.0508	9.7123	4.8261
E to Z ↓	0.0810	0.0775	5.5367	2.8349
E to Z ↑	0.0448	0.0423	9.6597	4.8022
F to Z ↓	0.0757	0.0725	5.5189	2.8251
F to Z ↑	0.0462	0.0438	9.6585	4.8041
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
A to Z ↓	0.0982	0.0928	1.4414	0.7409
A to Z ↑	0.0483	0.0482	2.4100	1.2162
B to Z ↓	0.0927	0.0877	1.4327	0.7390
B to Z ↑	0.0499	0.0495	2.4092	1.2165
C to Z ↓	0.0901	0.0861	1.4373	0.7400
C to Z ↑	0.0444	0.0453	2.3974	1.2093
D to Z ↓	0.0857	0.0813	1.4314	0.7381
D to Z ↑	0.0464	0.0467	2.3973	1.2093
E to Z ↓	0.0739	0.0743	1.4300	0.7372
E to Z ↑	0.0384	0.0400	2.3860	1.2058
F to Z ↓	0.0692	0.0686	1.4249	0.7345
F to Z ↑	0.0399	0.0412	2.3871	1.2054

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	9.172e-07	1.536e-09
X8_P10	1.388e-06	1.536e-09
X17_P10	2.315e-06	1.655e-09
X33_P10	4.084e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	5.137e-05	6.145e-05	7.727e-05	1.508e-04
B (output stable)	1.589e-04	1.735e-04	1.820e-04	2.803e-04
C (output stable)	2.629e-05	3.147e-05	3.941e-05	6.358e-05
D (output stable)	3.612e-05	4.431e-05	5.476e-05	1.286e-04
E (output stable)	2.781e-05	3.174e-05	3.920e-05	5.568e-05
F (output stable)	3.075e-05	3.637e-05	4.845e-05	1.039e-04

A to Z	2.691e-03	3.470e-03	5.092e-03	9.534e-03
B to Z	2.486e-03	3.231e-03	4.785e-03	9.004e-03
C to Z	2.265e-03	2.964e-03	4.421e-03	8.319e-03
D to Z	2.178e-03	2.851e-03	4.233e-03	7.847e-03
E to Z	1.793e-03	2.439e-03	3.642e-03	7.118e-03
F to Z	1.693e-03	2.306e-03	3.446e-03	6.643e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

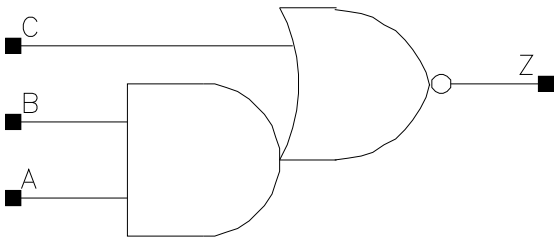
Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	-5.989e-06	-7.071e-06	-8.926e-06	-1.665e-05
B (output stable)	-1.337e-05	-1.427e-05	-1.410e-05	-2.928e-05
C (output stable)	-1.242e-06	-6.759e-07	1.891e-06	8.974e-06
D (output stable)	8.486e-07	1.893e-06	3.904e-06	1.540e-05
E (output stable)	1.656e-05	2.155e-05	3.193e-05	5.345e-05
F (output stable)	1.418e-05	1.863e-05	2.758e-05	4.807e-05
A to Z	-6.490e-06	-7.104e-06	-7.469e-06	-1.331e-05
B to Z	-6.655e-06	-6.864e-06	-7.297e-06	-1.228e-05
C to Z	-3.412e-06	-3.450e-06	-3.413e-06	-3.269e-06
D to Z	-3.262e-06	-3.327e-06	-3.126e-06	-3.376e-06
E to Z	-3.102e-07	-4.493e-07	-5.372e-07	-1.055e-06
F to Z	-2.642e-07	-3.340e-07	-3.711e-07	-8.774e-07

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008
X44_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X33_P10	X44_P10
A	0.0007	0.0022	0.0044	0.0058
B	0.0007	0.0020	0.0040	0.0054
C	0.0008	0.0023	0.0045	0.0060

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0154	0.0161	5.2633	1.7890
A to Z ↑	0.0280	0.0284	10.6318	3.5237
B to Z ↓	0.0151	0.0152	5.2970	1.8041
B to Z ↑	0.0234	0.0230	10.5250	3.5254
C to Z ↓	0.0150	0.0151	2.7765	0.9517
C to Z ↑	0.0307	0.0304	9.7365	3.2481
	X33_P10	**X44_P10**	**X33_P10**	**X44_P10**
A to Z ↓	0.0164	0.0164	0.9041	0.6852

A to Z ↑	0.0284	0.0284	1.7633	1.3331
B to Z ↓	0.0151	0.0151	0.9133	0.6915
B to Z ↑	0.0227	0.0226	1.7619	1.3295
C to Z ↓	0.0167	0.0170	0.5675	0.4429
C to Z ↑	0.0307	0.0306	1.6224	1.2252

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P10	7.083e-07	8.218e-10
X17_P10	1.900e-06	1.536e-09
X33_P10	3.517e-06	2.608e-09
X44_P10	4.629e-06	3.323e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	1.442e-05	5.219e-05	1.143e-04	1.493e-04
B (output stable)	3.102e-05	1.497e-04	3.308e-04	4.269e-04
C (output stable)	8.956e-05	2.793e-04	5.887e-04	7.898e-04
A to Z	8.571e-04	2.724e-03	5.480e-03	7.267e-03
B to Z	6.619e-04	1.888e-03	3.770e-03	4.970e-03
C to Z	1.256e-03	3.716e-03	7.535e-03	9.977e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

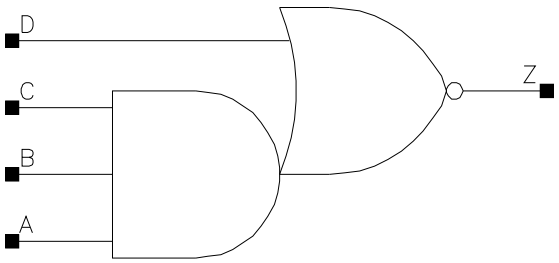
Pin Cycle (vdds)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	1.053e-05	2.809e-05	5.322e-05	6.941e-05
B (output stable)	2.140e-05	5.186e-05	1.038e-04	1.342e-04
C (output stable)	-6.326e-06	-1.513e-05	-3.160e-05	-4.076e-05
A to Z	-1.628e-07	-1.878e-06	-3.835e-06	-5.246e-06
B to Z	-1.906e-07	-5.450e-07	-4.260e-07	-4.420e-07
C to Z	-2.637e-06	-7.174e-06	-1.391e-05	-1.805e-05

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X29_P10	1.200	3.536	4.2432
X38_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X29_P10	X38_P10
A	0.0008	0.0044	0.0058
B	0.0007	0.0042	0.0056
C	0.0007	0.0040	0.0053
D	0.0008	0.0046	0.0057

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X29_P10	X5_P10	X29_P10
A to Z ↓	0.0227	0.0242	7.7927	1.3348
A to Z ↑	0.0357	0.0357	10.6237	1.7496
B to Z ↓	0.0224	0.0230	7.8049	1.3356
B to Z ↑	0.0320	0.0316	10.6235	1.7594
C to Z ↓	0.0213	0.0208	7.8160	1.3405
C to Z ↑	0.0277	0.0265	10.5310	1.7687
D to Z ↓	0.0176	0.0195	2.8272	0.5726

D to Z ↑	0.0350	0.0352	9.0710	1.5059
	X38_P10		**X38_P10**	
A to Z ↓	0.0233		1.0230	
A to Z ↑	0.0343		1.3168	
B to Z ↓	0.0224		1.0251	
B to Z ↑	0.0306		1.3264	
C to Z ↓	0.0198		1.0294	
C to Z ↑	0.0252		1.3371	
D to Z ↓	0.0201		0.4761	
D to Z ↑	0.0341		1.1344	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P10	7.116e-07	9.409e-10
X29_P10	3.500e-06	3.442e-09
X38_P10	4.399e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P10	X29_P10	X38_P10
A (output stable)	1.332e-05	1.173e-04	1.501e-04
B (output stable)	2.621e-05	2.451e-04	3.093e-04
C (output stable)	5.174e-05	5.545e-04	7.087e-04
D (output stable)	3.108e-04	2.387e-03	3.087e-03
A to Z	1.324e-03	8.445e-03	1.044e-02
B to Z	1.131e-03	6.824e-03	8.471e-03
C to Z	9.333e-04	5.110e-03	6.139e-03
D to Z	1.661e-03	1.009e-02	1.276e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

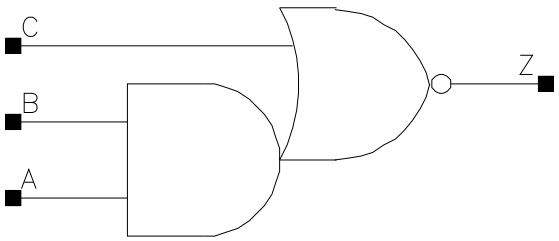
Pin Cycle (vdds)	X5_P10	X29_P10	X38_P10
A (output stable)	1.082e-05	7.008e-05	9.122e-05
B (output stable)	4.943e-06	3.004e-05	4.153e-05
C (output stable)	5.508e-06	3.015e-05	3.905e-05
D (output stable)	-3.721e-05	-3.059e-04	-3.946e-04
A to Z	-1.091e-07	-2.553e-06	-1.486e-06
B to Z	-4.380e-07	-2.671e-06	-3.816e-06
C to Z	-1.200e-07	-3.680e-07	-1.835e-06
D to Z	-2.733e-06	-2.121e-05	-2.741e-05

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X11_P10	1.200	1.088	1.3056
X16_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X11_P10	X16_P10	X23_P10
A	0.0008	0.0016	0.0024	0.0032
B	0.0008	0.0015	0.0023	0.0029
C	0.0008	0.0014	0.0021	0.0029
	X46_P10			
A	0.0061			
B	0.0058			
C	0.0057			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X11_P10	X6_P10	X11_P10
A to Z ↓	0.0176	0.0190	5.1224	2.5825
A to Z ↑	0.0331	0.0349	10.6083	5.1786
B to Z ↓	0.0182	0.0184	5.1501	2.5986

B to Z ↑	0.0295	0.0301	10.5347	5.1877
C to Z ↓	0.0114	0.0117	2.8455	1.6767
C to Z ↑	0.0230	0.0224	9.6688	4.7423
	X16_P10	**X23_P10**	**X16_P10**	**X23_P10**
A to Z ↓	0.0183	0.0187	1.7873	1.3394
A to Z ↑	0.0326	0.0333	3.4771	2.6260
B to Z ↓	0.0182	0.0181	1.7990	1.3481
B to Z ↑	0.0280	0.0284	3.4763	2.6309
C to Z ↓	0.0119	0.0107	1.1796	0.7269
C to Z ↑	0.0217	0.0220	3.1801	2.4050
	X46_P10		**X46_P10**	
A to Z ↓	0.0181		0.6863	
A to Z ↑	0.0320		1.3473	
B to Z ↓	0.0176		0.6908	
B to Z ↑	0.0272		1.3444	
C to Z ↓	0.0108		0.3738	
C to Z ↑	0.0215		1.2322	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P10	7.050e-07	8.218e-10
X11_P10	1.370e-06	1.298e-09
X16_P10	1.782e-06	1.536e-09
X23_P10	2.642e-06	2.013e-09
X46_P10	4.964e-06	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	2.687e-05	7.243e-05	9.350e-05	1.309e-04
B (output stable)	6.215e-05	2.286e-04	2.237e-04	3.359e-04
C (output stable)	4.779e-05	1.209e-04	1.519e-04	2.472e-04
A to Z	1.301e-03	2.917e-03	3.905e-03	5.365e-03
B to Z	1.104e-03	2.326e-03	3.079e-03	4.188e-03
C to Z	6.283e-04	1.270e-03	1.750e-03	2.393e-03
	X46_P10			
A (output stable)	2.393e-04			
B (output stable)	5.314e-04			
C (output stable)	3.747e-04			
A to Z	9.825e-03			
B to Z	7.637e-03			
C to Z	4.344e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	-1.453e-06	-4.136e-06	-3.445e-06	-4.876e-06
B (output stable)	-6.448e-06	-2.254e-05	-1.367e-05	-2.094e-05
C (output stable)	5.880e-05	1.526e-04	1.367e-04	1.907e-04
A to Z	-7.460e-07	-3.315e-06	-3.893e-06	-4.188e-06
B to Z	-4.650e-07	-2.395e-06	-2.903e-06	-1.696e-06
C to Z	-3.923e-07	-5.865e-07	-5.743e-07	-7.625e-07

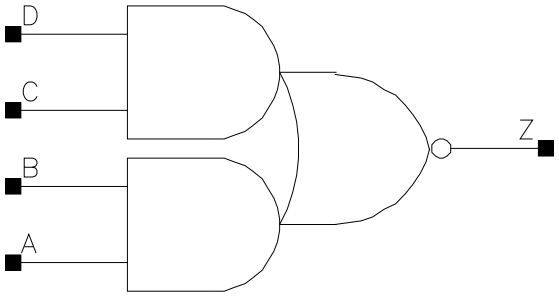
	X46_P10			
A (output stable)	-8.396e-06			
B (output stable)	-2.760e-05			
C (output stable)	3.492e-04			
A to Z	-5.406e-06			
B to Z	-4.401e-06			
C to Z	-9.670e-07			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P10	X10_P10	X16_P10	X21_P10
A	0.0007	0.0017	0.0024	0.0031
B	0.0007	0.0015	0.0022	0.0029
C	0.0006	0.0016	0.0022	0.0029
D	0.0007	0.0014	0.0021	0.0027
	X42_P10			
A	0.0062			
B	0.0059			
C	0.0058			
D	0.0055			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X10_P10**	**X4_P10**	**X10_P10**
A to Z ↓	0.0198	0.0193	6.4486	2.5088
A to Z ↑	0.0422	0.0357	14.7583	4.7774
B to Z ↓	0.0207	0.0204	6.4802	2.5235
B to Z ↑	0.0382	0.0328	14.7390	4.8603
C to Z ↓	0.0159	0.0151	6.5495	2.5151
C to Z ↑	0.0322	0.0279	14.5839	4.7421
D to Z ↓	0.0160	0.0151	6.5886	2.5347
D to Z ↑	0.0278	0.0242	14.5554	4.7907
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0209	0.0208	1.7973	1.3452
A to Z ↑	0.0374	0.0369	3.2152	2.4604
B to Z ↓	0.0212	0.0205	1.8070	1.3529
B to Z ↑	0.0331	0.0324	3.2140	2.4625
C to Z ↓	0.0161	0.0164	1.7929	1.3435
C to Z ↑	0.0286	0.0291	3.1758	2.4310
D to Z ↓	0.0153	0.0150	1.8092	1.3562
D to Z ↑	0.0238	0.0239	3.1795	2.4346
	X42_P10		**X42_P10**	
A to Z ↓	0.0216		0.6948	
A to Z ↑	0.0374		1.2342	
B to Z ↓	0.0212		0.6988	
B to Z ↑	0.0327		1.2297	
C to Z ↓	0.0169		0.6870	
C to Z ↑	0.0293		1.2201	
D to Z ↓	0.0156		0.6943	
D to Z ↑	0.0242		1.2182	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	6.743e-07	9.409e-10
X10_P10	1.746e-06	1.536e-09
X16_P10	2.333e-06	1.894e-09
X21_P10	3.180e-06	2.489e-09
X42_P10	6.093e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	2.663e-05	6.148e-05	1.204e-04	1.598e-04
B (output stable)	4.035e-05	1.008e-04	2.747e-04	3.905e-04
C (output stable)	1.521e-05	4.502e-05	8.413e-05	1.192e-04
D (output stable)	3.007e-05	8.377e-05	2.368e-04	3.590e-04
A to Z	1.349e-03	3.221e-03	5.179e-03	6.665e-03
B to Z	1.179e-03	2.809e-03	4.322e-03	5.491e-03
C to Z	7.732e-04	1.884e-03	2.980e-03	4.033e-03
D to Z	6.197e-04	1.493e-03	2.146e-03	2.854e-03
	X42_P10			
A (output stable)	3.108e-04			
B (output stable)	7.225e-04			
C (output stable)	2.343e-04			
D (output stable)	6.536e-04			

A to Z	1.324e-02			
B to Z	1.095e-02			
C to Z	7.917e-03			
D to Z	5.676e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

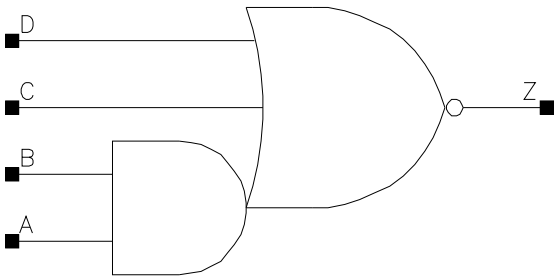
Pin Cycle (vdds)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	-1.509e-06	-2.343e-06	-3.907e-06	-4.562e-06
B (output stable)	-1.483e-06	-2.375e-06	-4.069e-06	-5.838e-06
C (output stable)	6.300e-06	1.958e-05	2.795e-05	3.966e-05
D (output stable)	6.066e-06	1.912e-05	2.764e-05	3.789e-05
A to Z	-3.225e-06	-3.053e-06	-6.699e-06	-7.904e-06
B to Z	-3.141e-06	-3.173e-06	-5.555e-06	-5.144e-06
C to Z	-1.088e-07	-4.529e-07	-1.949e-06	-2.748e-06
D to Z	-1.290e-07	-3.964e-07	-4.930e-07	-7.577e-07
	X42_P10			
A (output stable)	-8.536e-06			
B (output stable)	-1.160e-05			
C (output stable)	7.306e-05			
D (output stable)	7.010e-05			
A to Z	-1.336e-05			
B to Z	-1.059e-05			
C to Z	-5.293e-06			
D to Z	-1.113e-06			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X35_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P10	X35_P10
A	0.0007	0.0056
B	0.0008	0.0052
C	0.0008	0.0056
D	0.0008	0.0052

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X35_P10	X5_P10	X35_P10
A to Z ↓	0.0175	0.0184	5.3344	0.7763
A to Z ↑	0.0374	0.0353	16.2435	2.0423
B to Z ↓	0.0178	0.0176	5.3559	0.7832
B to Z ↑	0.0316	0.0285	16.1781	2.0425
C to Z ↓	0.0176	0.0218	2.9382	0.5691
C to Z ↑	0.0464	0.0450	15.3692	1.9336
D to Z ↓	0.0171	0.0205	2.9652	0.5672

D to Z ↑	0.0443	0.0415	15.3826	1.9359

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P10	5.512e-07	9.409e-10
X35_P10	3.245e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P10	X35_P10
A (output stable)	7.768e-06	8.962e-05
B (output stable)	1.476e-05	1.919e-04
C (output stable)	1.270e-04	1.290e-03
D (output stable)	1.568e-05	1.701e-04
A to Z	1.056e-03	7.753e-03
B to Z	8.624e-04	5.716e-03
C to Z	1.721e-03	1.340e-02
D to Z	1.455e-03	1.058e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

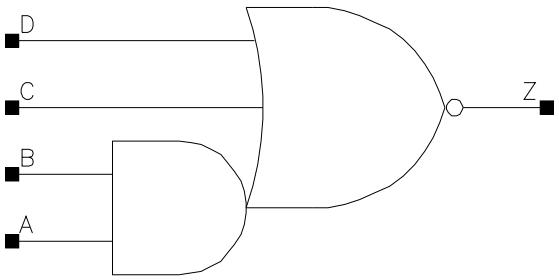
Pin Cycle (vdds)	X5_P10	X35_P10
A (output stable)	1.079e-05	6.983e-05
B (output stable)	1.847e-05	1.099e-04
C (output stable)	-2.020e-05	-1.590e-04
D (output stable)	1.220e-05	9.201e-05
A to Z	-4.918e-07	-5.476e-06
B to Z	-2.091e-07	-2.834e-06
C to Z	-4.795e-06	-3.322e-05
D to Z	-2.707e-06	-1.610e-05

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X17_P10	1.200	2.448	2.9376
X34_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P10	X17_P10	X34_P10
A	0.0008	0.0031	0.0063
B	0.0008	0.0030	0.0059
C	0.0007	0.0027	0.0053
D	0.0007	0.0025	0.0048

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X17_P10	X4_P10	X17_P10
A to Z ↓	0.0202	0.0218	5.8356	1.5316
A to Z ↑	0.0455	0.0481	16.2851	4.0008
B to Z ↓	0.0215	0.0218	5.8625	1.5383
B to Z ↑	0.0408	0.0416	16.1989	4.0051
C to Z ↓	0.0189	0.0185	4.8387	1.1824
C to Z ↑	0.0341	0.0361	15.3046	3.7702

D to Z ↓	0.0163	0.0147	4.9425	1.1873
D to Z ↑	0.0290	0.0265	15.3554	3.7821
	X34_P10		**X34_P10**	
A to Z ↓	0.0215		0.7829	
A to Z ↑	0.0471		2.0246	
B to Z ↓	0.0218		0.7863	
B to Z ↑	0.0409		2.0196	
C to Z ↓	0.0186		0.6181	
C to Z ↑	0.0351		1.9056	
D to Z ↓	0.0147		0.6229	
D to Z ↑	0.0259		1.9125	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	4.352e-07	9.409e-10
X17_P10	1.660e-06	2.489e-09
X34_P10	3.144e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P10	X17_P10	X34_P10
A (output stable)	3.017e-05	1.401e-04	2.809e-04
B (output stable)	3.484e-05	2.050e-04	3.895e-04
C (output stable)	3.682e-05	2.911e-04	5.482e-04
D (output stable)	1.432e-05	1.551e-04	2.805e-04
A to Z	1.630e-03	7.141e-03	1.377e-02
B to Z	1.451e-03	6.023e-03	1.169e-02
C to Z	9.873e-04	4.323e-03	8.210e-03
D to Z	6.874e-04	2.532e-03	4.799e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

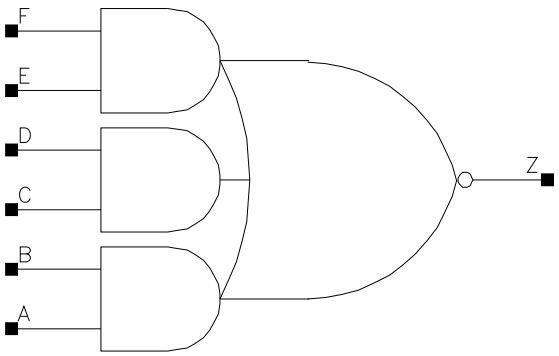
Pin Cycle (vdds)	X4_P10	X17_P10	X34_P10
A (output stable)	-3.280e-06	-1.276e-05	-2.467e-05
B (output stable)	-3.644e-06	-1.622e-05	-3.092e-05
C (output stable)	9.893e-06	5.385e-06	1.959e-05
D (output stable)	3.270e-05	1.571e-04	2.885e-04
A to Z	-2.387e-06	-8.611e-06	-2.038e-05
B to Z	-2.357e-06	-9.674e-06	-1.627e-05
C to Z	-3.447e-07	-5.349e-06	-8.072e-06
D to Z	-5.543e-08	-1.190e-06	-2.557e-06

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X8_P10	1.200	2.176	2.6112
X13_P10	1.200	2.720	3.2640
X17_P10	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P10	X8_P10	X13_P10	X17_P10
A	0.0008	0.0016	0.0024	0.0031

B	0.0008	0.0015	0.0022	0.0029
C	0.0008	0.0015	0.0023	0.0029
D	0.0008	0.0014	0.0021	0.0027
E	0.0009	0.0014	0.0021	0.0028
F	0.0007	0.0013	0.0020	0.0026

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0230	0.0276	5.1553	2.9793
A to Z ↑	0.0647	0.0634	15.6351	7.1814
B to Z ↓	0.0248	0.0279	5.1736	2.9878
B to Z ↑	0.0599	0.0575	15.6241	7.1897
C to Z ↓	0.0215	0.0254	5.1002	2.9723
C to Z ↑	0.0564	0.0567	15.6609	7.1876
D to Z ↓	0.0229	0.0259	5.1283	2.9856
D to Z ↑	0.0515	0.0509	15.6125	7.1820
E to Z ↓	0.0170	0.0200	4.9696	2.9678
E to Z ↑	0.0407	0.0407	15.4814	7.1185
F to Z ↓	0.0174	0.0196	5.0180	2.9922
F to Z ↑	0.0354	0.0348	15.5562	7.1238
	X13_P10	**X17_P10**	**X13_P10**	**X17_P10**
A to Z ↓	0.0264	0.0265	2.0249	1.5417
A to Z ↑	0.0589	0.0590	4.7610	3.6164
B to Z ↓	0.0274	0.0269	2.0303	1.5463
B to Z ↑	0.0538	0.0531	4.7711	3.6174
C to Z ↓	0.0245	0.0245	2.0409	1.5245
C to Z ↑	0.0522	0.0523	4.7653	3.6260
D to Z ↓	0.0255	0.0244	2.0495	1.5322
D to Z ↑	0.0472	0.0465	4.7694	3.6204
E to Z ↓	0.0195	0.0194	2.0321	1.5240
E to Z ↑	0.0384	0.0384	4.7252	3.5844
F to Z ↓	0.0192	0.0182	2.0452	1.5352
F to Z ↑	0.0329	0.0324	4.7336	3.5941

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	1.019e-06	1.298e-09
X8_P10	1.914e-06	2.251e-09
X13_P10	2.549e-06	2.727e-09
X17_P10	3.424e-06	3.561e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

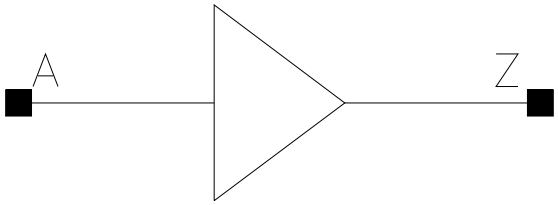
Pin Cycle (vdd)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	7.562e-05	1.697e-04	2.302e-04	3.031e-04
B (output stable)	1.513e-04	3.737e-04	4.387e-04	6.041e-04
C (output stable)	3.605e-05	8.354e-05	1.068e-04	1.516e-04
D (output stable)	5.191e-05	1.849e-04	1.997e-04	3.192e-04
E (output stable)	2.614e-05	6.694e-05	1.002e-04	1.373e-04
F (output stable)	3.727e-05	1.496e-04	1.797e-04	2.839e-04

A to Z	2.609e-03	5.520e-03	7.582e-03	1.001e-02
B to Z	2.408e-03	4.951e-03	6.860e-03	8.911e-03
C to Z	1.954e-03	4.316e-03	5.767e-03	7.645e-03
D to Z	1.768e-03	3.793e-03	5.100e-03	6.588e-03
E to Z	1.210e-03	2.792e-03	3.748e-03	4.965e-03
F to Z	1.024e-03	2.266e-03	3.037e-03	3.890e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	-1.092e-05	-2.349e-05	-2.464e-05	-3.314e-05
B (output stable)	-2.351e-05	-4.490e-05	-4.442e-05	-5.925e-05
C (output stable)	1.843e-06	2.166e-06	8.340e-06	1.206e-05
D (output stable)	7.531e-06	1.062e-05	1.647e-05	2.008e-05
E (output stable)	3.462e-05	7.803e-05	8.238e-05	1.138e-04
F (output stable)	3.043e-05	6.851e-05	7.307e-05	1.000e-04
A to Z	-9.635e-06	-1.875e-05	-1.886e-05	-2.468e-05
B to Z	-9.445e-06	-1.906e-05	-1.840e-05	-2.346e-05
C to Z	-3.112e-06	-7.800e-06	-6.361e-06	-7.249e-06
D to Z	-2.835e-06	-6.685e-06	-5.384e-06	-7.689e-06
E to Z	-3.946e-07	-1.787e-06	-2.238e-06	-2.068e-06
F to Z	-4.022e-07	-9.746e-07	-1.115e-06	-1.805e-06

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.408	0.4896
X6_P10	1.200	0.408	0.4896
X8_P10	1.200	0.408	0.4896
X13_P10	1.200	0.544	0.6528
X16_P10	1.200	0.544	0.6528
X21_P10	1.200	0.680	0.8160
X25_P10	1.200	0.680	0.8160
X29_P10	1.200	0.952	1.1424
X33_P10	1.200	0.952	1.1424
X42_P10	1.200	1.088	1.3056
X50_P10	1.200	1.224	1.4688
X58_P10	1.200	1.496	1.7952
X67_P10	1.200	1.632	1.9584
X75_P10	1.200	1.768	2.1216
X84_P10	1.200	1.904	2.2848
X100_P10	1.200	2.312	2.7744
X134_P10	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0008	0.0008	0.0008	0.0008
	X16_P10	X21_P10	X25_P10	X29_P10
A	0.0008	0.0011	0.0011	0.0014
	X33_P10	X42_P10	X50_P10	X58_P10
A	0.0014	0.0016	0.0019	0.0029

	X67_P10	X75_P10	X84_P10	X100_P10
A	0.0029	0.0028	0.0028	0.0037
	X134_P10			
A	0.0046			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0390	0.0390	5.1615	3.7049
A to Z ↑	0.0301	0.0296	9.5845	6.9001
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0404	0.0454	2.7138	1.7772
A to Z ↑	0.0303	0.0337	4.8652	3.2110
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0488	0.0402	1.4021	1.0863
A to Z ↑	0.0356	0.0303	2.4380	1.9160
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0422	0.0405	0.9293	0.7901
A to Z ↑	0.0315	0.0295	1.5999	1.3662
	X33_P10	**X42_P10**	**X33_P10**	**X42_P10**
A to Z ↓	0.0420	0.0408	0.6989	0.5663
A to Z ↑	0.0305	0.0306	1.1964	0.9611
	X50_P10	**X58_P10**	**X50_P10**	**X58_P10**
A to Z ↓	0.0397	0.0367	0.4715	0.4065
A to Z ↑	0.0296	0.0277	0.7990	0.6855
	X67_P10	**X75_P10**	**X67_P10**	**X75_P10**
A to Z ↓	0.0388	0.0406	0.3572	0.3221
A to Z ↑	0.0292	0.0304	0.6011	0.5376
	X84_P10	**X100_P10**	**X84_P10**	**X100_P10**
A to Z ↓	0.0424	0.0401	0.2919	0.2452
A to Z ↑	0.0316	0.0302	0.4845	0.4061
	X134_P10		**X134_P10**	
A to Z ↓	0.0416		0.1901	
A to Z ↑	0.0315		0.3094	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	6.149e-07	7.027e-10
X6_P10	7.469e-07	7.027e-10
X8_P10	8.986e-07	7.027e-10
X13_P10	1.158e-06	8.218e-10
X16_P10	1.402e-06	8.218e-10
X21_P10	1.875e-06	9.409e-10
X25_P10	2.060e-06	9.409e-10
X29_P10	2.445e-06	1.179e-09
X33_P10	2.581e-06	1.179e-09
X42_P10	3.166e-06	1.298e-09
X50_P10	3.790e-06	1.417e-09
X58_P10	4.657e-06	1.655e-09
X67_P10	5.090e-06	1.775e-09
X75_P10	5.524e-06	1.894e-09

X84_P10	5.958e-06	2.013e-09
X100_P10	7.259e-06	2.370e-09
X134_P10	9.428e-06	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	1.298e-03	1.440e-03	1.690e-03	2.203e-03
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	2.627e-03	3.569e-03	3.989e-03	4.436e-03
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	4.844e-03	6.133e-03	7.089e-03	8.590e-03
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	9.669e-03	1.073e-02	1.172e-02	1.422e-02
	X134_P10			
A to Z	1.879e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

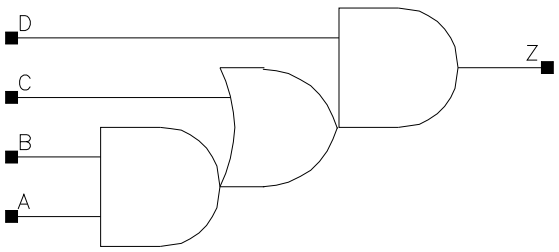
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	-2.010e-07	-2.005e-07	-1.973e-07	-2.206e-07
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	-1.140e-07	-4.811e-07	-5.363e-07	-5.599e-07
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	-4.409e-07	-8.617e-07	-6.096e-07	-1.034e-06
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	-6.057e-07	-1.161e-06	-1.310e-06	-1.295e-06
	X134_P10			
A to Z	-1.287e-06			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.632	1.9584
X25_P10	1.200	1.768	2.1216
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0009	0.0019	0.0019	0.0019
B	0.0009	0.0017	0.0017	0.0017
C	0.0010	0.0022	0.0021	0.0021
D	0.0015	0.0019	0.0019	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0563	0.0531	2.7844	1.3835
A to Z ↑	0.0468	0.0439	4.9220	2.3953
B to Z ↓	0.0525	0.0485	2.7773	1.3819
B to Z ↑	0.0466	0.0425	4.9268	2.3955
C to Z ↓	0.0462	0.0421	2.7710	1.3781
C to Z ↑	0.0348	0.0313	4.8858	2.3743

D to Z ↓	0.0425	0.0372	2.7390	1.3649
D to Z ↑	0.0412	0.0356	4.8881	2.3758
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0583	0.0615	0.9440	0.7156
A to Z ↑	0.0481	0.0502	1.6185	1.2175
B to Z ↓	0.0538	0.0581	0.9428	0.7135
B to Z ↑	0.0468	0.0499	1.6171	1.2175
C to Z ↓	0.0472	0.0512	0.9396	0.7105
C to Z ↑	0.0347	0.0370	1.6026	1.2033
D to Z ↓	0.0403	0.0423	0.9272	0.6983
D to Z ↑	0.0389	0.0407	1.6052	1.2052

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.195e-06	1.179e-09
X17_P10	2.185e-06	1.775e-09
X25_P10	2.527e-06	1.894e-09
X33_P10	2.870e-06	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	9.114e-05	1.835e-04	1.835e-04	1.717e-04
B (output stable)	9.964e-05	2.178e-04	2.190e-04	1.863e-04
C (output stable)	2.447e-04	4.049e-04	4.115e-04	3.875e-04
D (output stable)	7.845e-05	1.042e-04	1.046e-04	1.053e-04
A to Z	2.869e-03	5.230e-03	6.403e-03	7.238e-03
B to Z	2.663e-03	4.671e-03	5.846e-03	6.794e-03
C to Z	2.197e-03	3.694e-03	4.868e-03	5.796e-03
D to Z	2.966e-03	4.998e-03	6.173e-03	7.020e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

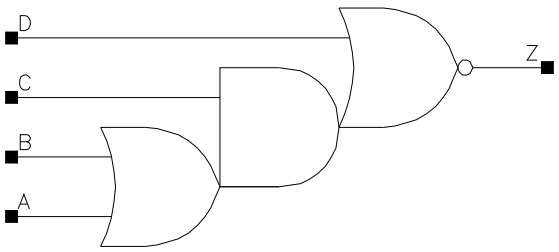
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	-1.567e-06	-3.017e-06	-3.021e-06	-2.858e-06
B (output stable)	-1.504e-06	-2.892e-06	-2.903e-06	-2.739e-06
C (output stable)	7.647e-06	1.249e-05	1.259e-05	1.291e-05
D (output stable)	1.553e-07	1.572e-07	1.738e-07	1.293e-07
A to Z	-1.051e-06	-1.949e-06	-2.685e-06	-2.399e-06
B to Z	-8.930e-07	-1.551e-06	-2.150e-06	-2.214e-06
C to Z	-2.724e-07	-5.168e-07	-6.244e-07	-5.541e-07
D to Z	-5.776e-07	-1.058e-06	-1.121e-06	-1.150e-06

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.952	1.1424
X11_P10	1.200	1.496	1.7952
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X16_P10	X21_P10
A	0.0009	0.0016	0.0024	0.0031
B	0.0008	0.0015	0.0024	0.0031
C	0.0008	0.0015	0.0023	0.0030
D	0.0010	0.0015	0.0022	0.0029

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0213	0.0203	4.9798	2.6147
A to Z ↑	0.0553	0.0509	15.9341	8.1747
B to Z ↓	0.0208	0.0201	4.8820	2.5848
B to Z ↑	0.0518	0.0482	15.9499	8.1976
C to Z ↓	0.0190	0.0181	4.5609	2.4024
C to Z ↑	0.0333	0.0305	10.3908	5.2988

D to Z ↓	0.0126	0.0109	2.7061	1.3761
D to Z ↑	0.0282	0.0243	11.1825	5.7069
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0203	0.0206	1.7881	1.3617
A to Z ↑	0.0477	0.0499	5.3241	4.0729
B to Z ↓	0.0197	0.0201	1.7911	1.3613
B to Z ↑	0.0462	0.0474	5.3258	4.0713
C to Z ↓	0.0183	0.0183	1.6615	1.2607
C to Z ↑	0.0297	0.0302	3.5114	2.6341
D to Z ↓	0.0109	0.0109	0.9666	0.7371
D to Z ↑	0.0229	0.0229	3.7623	2.8381

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P10	8.134e-07	1.179e-09
X11_P10	1.479e-06	1.655e-09
X16_P10	1.902e-06	1.894e-09
X21_P10	2.559e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	3.693e-05	6.510e-05	8.236e-05	1.384e-04
B (output stable)	1.408e-05	3.082e-05	3.208e-05	6.281e-05
C (output stable)	1.730e-04	3.331e-04	4.388e-04	6.533e-04
D (output stable)	4.649e-05	9.421e-05	1.208e-04	1.930e-04
A to Z	2.110e-03	3.674e-03	5.104e-03	7.182e-03
B to Z	1.722e-03	3.025e-03	4.328e-03	5.939e-03
C to Z	1.428e-03	2.418e-03	3.467e-03	4.793e-03
D to Z	8.052e-04	1.313e-03	1.760e-03	2.347e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

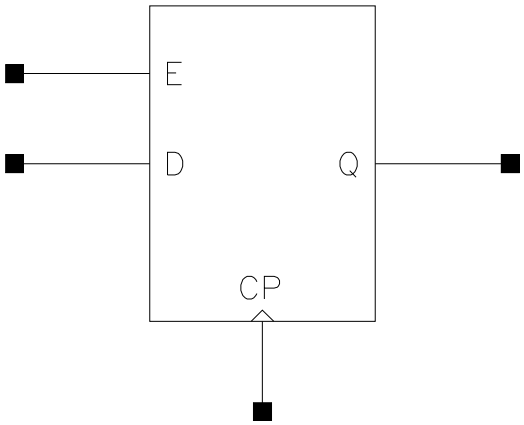
Pin Cycle (vdds)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	-4.503e-06	-6.295e-06	-7.303e-06	-1.362e-05
B (output stable)	7.268e-06	7.667e-06	1.680e-05	2.017e-05
C (output stable)	-1.757e-05	-3.057e-05	-3.823e-05	-6.257e-05
D (output stable)	5.202e-05	1.124e-04	1.455e-04	2.129e-04
A to Z	-3.514e-06	-4.938e-06	-7.074e-06	-1.141e-05
B to Z	-7.650e-07	-2.874e-06	-1.378e-06	-4.403e-06
C to Z	-1.753e-06	-2.746e-06	-3.523e-06	-3.357e-06
D to Z	-4.516e-07	-5.288e-07	-8.608e-07	-1.128e-06

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.128	3.7536
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0011	0.0011	0.0010

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0647	0.0748	2.7843	1.4514
CP to Q ↑	0.0771	0.0820	4.9198	2.4687
	X33_P10		**X33_P10**	
CP to Q ↓	0.1102		0.7093	
CP to Q ↑	0.1329		1.2180	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0990	0.0990	0.0952
CP ↑	min_pulse_width to CP	0.0501	0.0635	0.0454
D ↓	hold_rising to CP	-0.0459	-0.0459	-0.0459
D ↑	hold_rising to CP	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.1020	0.1020	0.1020
D ↑	setup_rising to CP	0.0540	0.0540	0.0484
E ↓	hold_rising to CP	-0.0356	-0.0330	-0.0386
E ↑	hold_rising to CP	-0.0188	-0.0188	-0.0188
E ↓	setup_rising to CP	0.0944	0.0944	0.0944
E ↑	setup_rising to CP	0.1126	0.1126	0.1126

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	3.627e-06	2.966e-09
X17_P10	4.109e-06	3.085e-09
X33_P10	5.614e-06	3.561e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

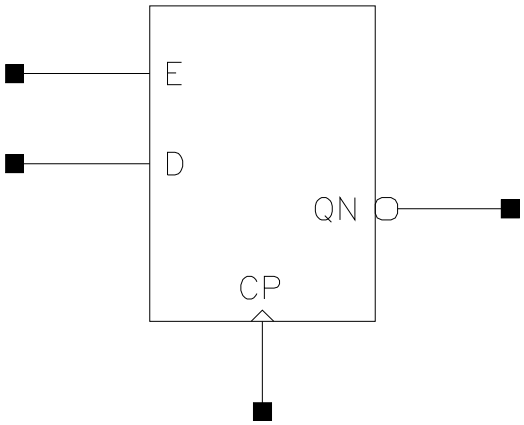
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.113e-03	3.113e-03	3.117e-03
Clock 100Mhz Data 25Mhz	6.606e-03	7.064e-03	9.148e-03
Clock 100Mhz Data 50Mhz	1.010e-02	1.102e-02	1.518e-02
Clock = 0 Data 100Mhz	3.931e-03	3.932e-03	3.932e-03
Clock = 1 Data 100Mhz	1.094e-03	1.094e-03	1.094e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.264	3.9168
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0011	0.0011	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.1105	0.1026	2.8508	1.3646
CP to QN ↑	0.0863	0.0891	4.9795	2.3975
	X33_P10		**X33_P10**	
CP to QN ↓	0.1092		0.7108	
CP to QN ↑	0.0983		1.2234	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0990	0.0990	0.0990
CP ↑	min_pulse_width to CP	0.0454	0.0501	0.0549
D ↓	hold_rising to CP	-0.0459	-0.0459	-0.0459
D ↑	hold_rising to CP	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.1020	0.1020	0.1020
D ↑	setup_rising to CP	0.0540	0.0540	0.0540
E ↓	hold_rising to CP	-0.0386	-0.0330	-0.0330
E ↑	hold_rising to CP	-0.0188	-0.0188	-0.0188
E ↓	setup_rising to CP	0.0944	0.0944	0.0944
E ↑	setup_rising to CP	0.1126	0.1126	0.1126

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	3.601e-06	2.966e-09
X17_P10	4.362e-06	3.204e-09
X33_P10	5.488e-06	3.561e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

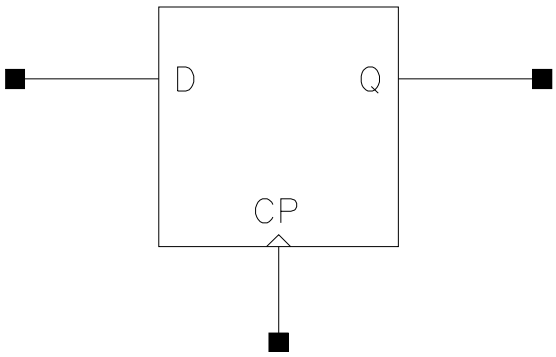
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.110e-03	3.110e-03	3.111e-03
Clock 100Mhz Data 25Mhz	6.653e-03	7.559e-03	8.968e-03
Clock 100Mhz Data 50Mhz	1.020e-02	1.201e-02	1.483e-02
Clock = 0 Data 100Mhz	3.934e-03	3.935e-03	3.935e-03
Clock = 1 Data 100Mhz	1.094e-03	1.094e-03	1.094e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.176	2.6112
X17_P10	1.200	2.448	2.9376
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0673	0.0743	2.7817	1.4410
CP to Q ↑	0.0786	0.0869	4.7893	2.4329
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to Q ↓	0.0948	0.0989	0.8699	0.7887
CP to Q ↑	0.0981	0.0996	1.3749	1.2486

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0844	0.0892	0.0892	0.0892
CP ↑	min_pulse_width to CP	0.0501	0.0635	0.0829	0.0877
D ↓	hold_rising to CP	0.0008	-0.0023	-0.0023	-0.0023
D ↑	hold_rising to CP	0.0029	0.0029	0.0029	0.0029
D ↓	setup_rising to CP	0.0563	0.0563	0.0563	0.0563
D ↑	setup_rising to CP	0.0244	0.0275	0.0275	0.0275

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	2.970e-06	2.251e-09
X17_P10	3.473e-06	2.489e-09
X30_P10	4.247e-06	2.727e-09
X33_P10	4.360e-06	2.727e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

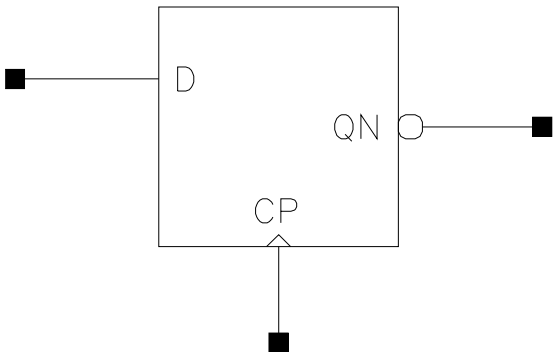
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.293e-03	3.315e-03	3.324e-03	3.327e-03
Clock 100Mhz Data 25Mhz	5.879e-03	6.639e-03	7.647e-03	7.874e-03
Clock 100Mhz Data 50Mhz	8.466e-03	9.963e-03	1.197e-02	1.242e-02
Clock = 0 Data 100Mhz	2.657e-03	2.745e-03	2.773e-03	2.787e-03
Clock = 1 Data 100Mhz	2.278e-05	2.283e-05	2.287e-05	2.291e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0644	0.0775	2.8577	1.4913
CP to QN ↑	0.0690	0.0729	4.7734	2.4262
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to QN ↓	0.1102	0.1099	0.7866	0.7102
CP to QN ↑	0.0906	0.1056	1.3248	1.2229

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0672	0.0709	0.0892	0.0844
CP ↑	min_pulse_width to CP	0.0501	0.0598	0.0501	0.0598
D ↓	hold_rising to CP	0.0100	0.0128	-0.0019	0.0008
D ↑	hold_rising to CP	0.0078	0.0078	0.0029	0.0029
D ↓	setup_rising to CP	0.0367	0.0367	0.0563	0.0563
D ↑	setup_rising to CP	0.0320	0.0323	0.0275	0.0244

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	2.752e-06	2.013e-09
X17_P10	3.248e-06	2.132e-09
X30_P10	4.551e-06	2.727e-09
X33_P10	4.834e-06	2.847e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

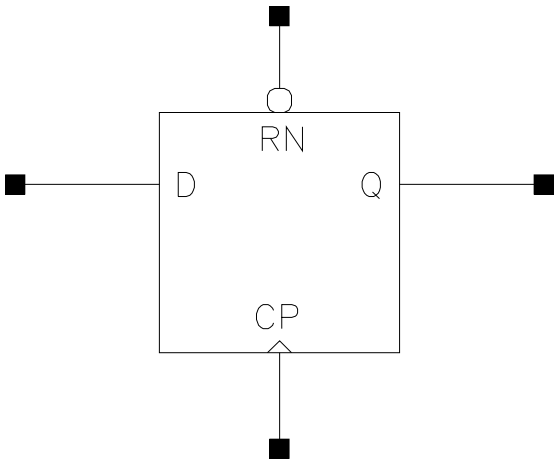
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.159e-03	3.160e-03	3.217e-03	3.240e-03
Clock 100Mhz Data 25Mhz	5.553e-03	6.056e-03	7.882e-03	8.203e-03
Clock 100Mhz Data 50Mhz	7.947e-03	8.951e-03	1.255e-02	1.317e-02
Clock = 0 Data 100Mhz	2.333e-03	2.334e-03	2.499e-03	2.539e-03
Clock = 1 Data 100Mhz	2.239e-05	2.250e-05	2.268e-05	2.279e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0772	0.0982	1.4558	0.8850
CP to Q ↑	0.0898	0.1007	2.4397	1.3806
RN to Q ↓	0.1274	0.1717	1.5919	0.9791

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0941	0.0941
CP ↑	min_pulse_width to CP	0.0646	0.0877
D ↓	hold_rising to CP	-0.0019	-0.0023
D ↑	hold_rising to CP	0.0029	0.0029
D ↓	setup_rising to CP	0.0612	0.0612
D ↑	setup_rising to CP	0.0372	0.0372
RN ↓	min_pulse_width to RN	0.1604	0.2092
RN ↑	recovery_rising to CP	0.0345	0.0345
RN ↑	removal_rising to CP	-0.0125	-0.0100

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P10	3.609e-06	3.085e-09
X30_P10	4.224e-06	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

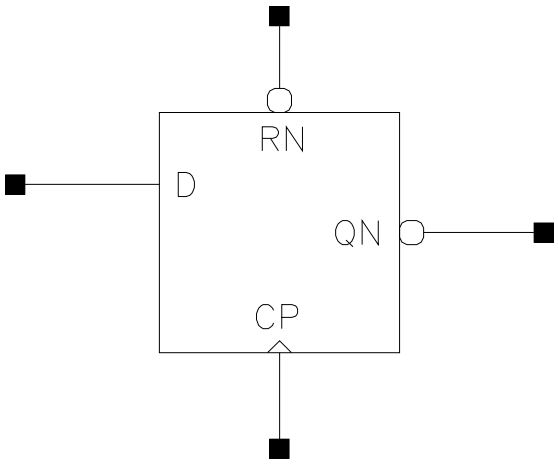
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	3.537e-03	3.540e-03
Clock 100Mhz Data 25Mhz	7.099e-03	8.113e-03
Clock 100Mhz Data 50Mhz	1.066e-02	1.269e-02
Clock = 0 Data 100Mhz	3.273e-03	3.276e-03
Clock = 1 Data 100Mhz	2.293e-05	2.306e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.1061	0.1146	1.3529	0.7894
CP to QN ↑	0.0887	0.0953	2.3803	1.3308
RN to QN ↑	0.1362	0.1451	2.3894	1.3351

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0941	0.0941
CP ↑	min_pulse_width to CP	0.0512	0.0549
D ↓	hold_rising to CP	-0.0019	-0.0019
D ↑	hold_rising to CP	0.0029	0.0029
D ↓	setup_rising to CP	0.0612	0.0612
D ↑	setup_rising to CP	0.0341	0.0341
RN ↓	min_pulse_width to RN	0.1257	0.1306
RN ↑	recovery_rising to CP	0.0345	0.0345
RN ↑	removal_rising to CP	-0.0125	-0.0100

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P10	4.337e-06	3.085e-09
X30_P10	5.243e-06	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

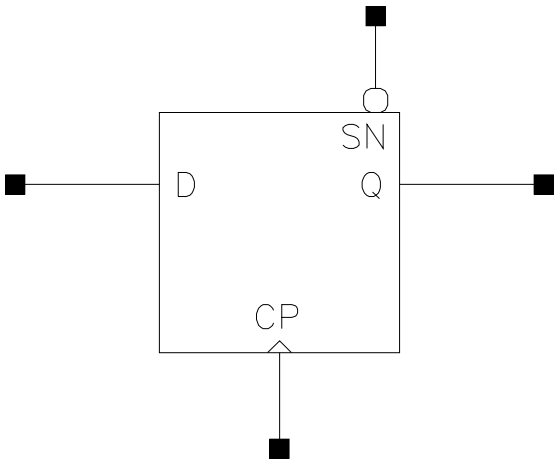
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	3.547e-03	3.546e-03
Clock 100Mhz Data 25Mhz	7.566e-03	8.516e-03
Clock 100Mhz Data 50Mhz	1.159e-02	1.349e-02
Clock = 0 Data 100Mhz	3.315e-03	3.302e-03
Clock = 1 Data 100Mhz	2.291e-05	2.305e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0011	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0780	0.0986	1.4576	0.8797
CP to Q ↑	0.0891	0.0995	2.4387	1.3795
SN to Q ↑	0.0910	0.1041	2.4559	1.3875

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.1000	0.0989
CP ↑	min_pulse_width to CP	0.0646	0.0877
D ↓	hold_rising to CP	-0.0019	-0.0023
D ↑	hold_rising to CP	0.0029	0.0029
D ↓	setup_rising to CP	0.0660	0.0660
D ↑	setup_rising to CP	0.0293	0.0293
SN ↓	min_pulse_width to SN	0.0864	0.1038
SN ↑	recovery_rising to CP	0.0177	0.0177
SN ↑	removal_rising to CP	0.0432	0.0432

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P10	3.965e-06	3.085e-09
X30_P10	4.871e-06	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

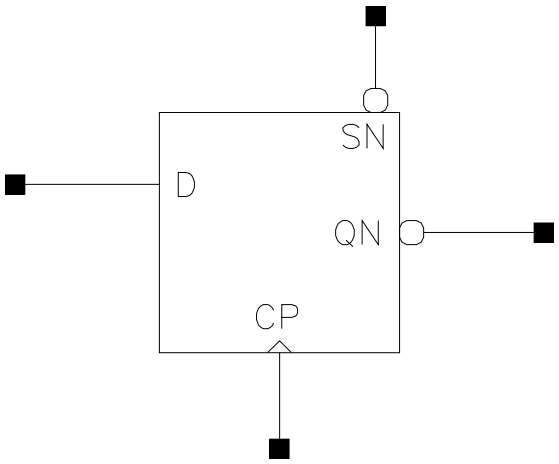
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	3.578e-03	3.571e-03
Clock 100Mhz Data 25Mhz	7.148e-03	8.112e-03
Clock 100Mhz Data 50Mhz	1.072e-02	1.265e-02
Clock = 0 Data 100Mhz	3.257e-03	3.256e-03
Clock = 1 Data 100Mhz	2.165e-05	2.174e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0011	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.1053	0.1139	1.3560	0.7904
CP to QN ↑	0.0896	0.0960	2.3752	1.3295
SN to QN ↓	0.1073	0.1164	1.3552	0.7909

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.1000	0.1000
CP ↑	min_pulse_width to CP	0.0512	0.0549
D ↓	hold_rising to CP	-0.0019	-0.0019
D ↑	hold_rising to CP	0.0029	0.0029
D ↓	setup_rising to CP	0.0660	0.0660
D ↑	setup_rising to CP	0.0293	0.0293
SN ↓	min_pulse_width to SN	0.0762	0.0789
SN ↑	recovery_rising to CP	0.0177	0.0177
SN ↑	removal_rising to CP	0.0432	0.0432

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P10	3.875e-06	3.085e-09
X30_P10	4.470e-06	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

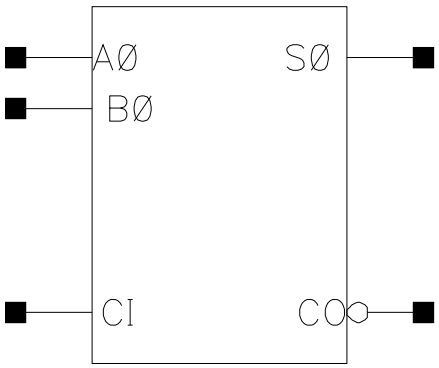
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	3.582e-03	3.580e-03
Clock 100Mhz Data 25Mhz	7.587e-03	8.540e-03
Clock 100Mhz Data 50Mhz	1.159e-02	1.350e-02
Clock = 0 Data 100Mhz	3.257e-03	3.256e-03
Clock = 1 Data 100Mhz	2.320e-05	2.317e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_-P10	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_-P10	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_-P10	1.200	3.672	4.4064
C12T28SOI_LRS1_-FA1X33_P10	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10
A0	0.0031	0.0063	0.0028	0.0055
B0	0.0028	0.0061	0.0030	0.0053
CI	0.0021	0.0048	0.0021	0.0037

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P10	**C12T28SOI_LR_-FA1X33_P10**	**C12T28SOI_LR_-FA1X8_P10**	**C12T28SOI_LR_-FA1X33_P10**
A0 to CO ↓	0.0757	0.0815	2.8920	0.7728
A0 to CO ↑	0.0507	0.0513	4.9333	1.2658
A0 to S0 ↓	0.0763	0.0956	2.8581	0.7546
A0 to S0 ↑	0.0780	0.0942	4.8785	1.2442
B0 to CO ↓	0.0735	0.0809	2.9054	0.7783
B0 to CO ↑	0.0516	0.0530	4.9366	1.2615
B0 to S0 ↓	0.0763	0.0965	2.8583	0.7540
B0 to S0 ↑	0.0774	0.0947	4.8824	1.2448
CI to CO ↓	0.0694	0.0769	2.9138	0.7778
CI to CO ↑	0.0504	0.0507	4.9340	1.2656
CI to S0 ↓	0.0749	0.0953	2.8566	0.7541
CI to S0 ↑	0.0765	0.0943	4.8803	1.2445
	C12T28SOI_LRS1_-FA1X8_P10	**C12T28SOI_LRS1_-FA1X33_P10**	**C12T28SOI_LRS1_-FA1X8_P10**	**C12T28SOI_LRS1_-FA1X33_P10**
A0 to CO ↓	0.0472	0.0581	6.0304	1.0527
A0 to CO ↑	0.0373	0.0426	4.9692	1.2540
A0 to S0 ↓	0.1011	0.1235	3.0513	0.7821
A0 to S0 ↑	0.0909	0.0977	5.0884	1.2649
B0 to CO ↓	0.0473	0.0585	6.0288	1.0535
B0 to CO ↑	0.0354	0.0414	4.9652	1.2536
B0 to S0 ↓	0.1014	0.1261	3.0511	0.7821
B0 to S0 ↑	0.0913	0.1002	5.0856	1.2645
CI to CO ↓	0.0451	0.0770	6.0214	1.0691
CI to CO ↑	0.0397	0.0466	5.0756	1.2626
CI to S0 ↓	0.0559	0.0727	3.0503	0.7821
CI to S0 ↑	0.0470	0.0466	5.0872	1.2653

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_FA1X8_P10	2.805e-06	2.251e-09
C12T28SOI_LR_FA1X33_P10	7.283e-06	4.633e-09
C12T28SOI_LRS1_FA1X8_P10	6.206e-06	3.561e-09
C12T28SOI_LRS1_FA1X33_P10	1.286e-05	7.372e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10
A0 to CO	2.983e-03	8.040e-03	4.569e-03	1.108e-02
A0 to S0	3.017e-03	8.407e-03	6.141e-03	1.380e-02
B0 to CO	2.961e-03	8.066e-03	4.593e-03	1.123e-02
B0 to S0	2.882e-03	8.194e-03	6.224e-03	1.409e-02
CI to CO	2.926e-03	8.032e-03	3.231e-03	9.766e-03
CI to S0	2.860e-03	8.191e-03	3.649e-03	1.052e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10
A0 to CO	-8.378e-06	-1.593e-05	3.867e-06	8.891e-06
A0 to S0	-7.291e-06	-1.407e-05	5.825e-06	1.249e-05
B0 to CO	3.420e-06	6.364e-06	-7.501e-07	-1.420e-06
B0 to S0	1.382e-05	2.629e-05	2.953e-06	5.309e-06
CI to CO	1.862e-05	3.562e-05	-3.778e-07	-7.319e-07
CI to S0	1.560e-05	2.734e-05	-6.310e-07	-7.199e-07

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X33_P10	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X33_P10
A0	0.0011	0.0031
B0	0.0010	0.0028

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
A0 to CO ↓	0.0522	0.0464	2.8433	0.7033
A0 to CO ↑	0.0484	0.0416	4.9036	1.2512
A0 to S0 ↓	0.0721	0.0654	2.7863	0.7049
A0 to S0 ↑	0.0653	0.0688	4.8364	1.2377
B0 to CO ↓	0.0510	0.0433	2.8455	0.6988
B0 to CO ↑	0.0503	0.0421	4.9039	1.2511
B0 to S0 ↓	0.0727	0.0631	2.7867	0.7054
B0 to S0 ↑	0.0647	0.0662	4.8366	1.2383

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.656e-06	1.417e-09
X33_P10	6.043e-06	2.966e-09

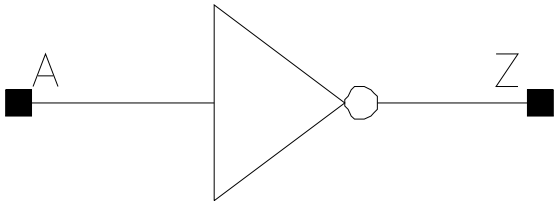
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X33_P10
A0 to CO	2.302e-03	7.304e-03
A0 to S0	2.099e-03	6.991e-03
B0 to CO	2.316e-03	7.232e-03
B0 to S0	2.048e-03	6.608e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X8_P10	X33_P10
A0 to CO	-4.248e-07	-6.524e-06
A0 to S0	-4.762e-07	-4.939e-06
B0 to CO	5.235e-06	3.247e-05
B0 to S0	2.596e-06	1.594e-05

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.272	0.3264
X6_P10	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X13_P10	1.200	0.408	0.4896
X17_P10	1.200	0.408	0.4896
X21_P10	1.200	0.544	0.6528
X25_P10	1.200	0.544	0.6528
X29_P10	1.200	0.680	0.8160
X33_P10	1.200	0.680	0.8160
X50_P10	1.200	0.952	1.1424
X58_P10	1.200	1.088	1.3056
X67_P10	1.200	1.224	1.4688
X75_P10	1.200	1.360	1.6320
X84_P10	1.200	1.496	1.7952
X100_P10	1.200	1.768	2.1216
X134_P10	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0005	0.0006	0.0008	0.0012
	X17_P10	X21_P10	X25_P10	X29_P10
A	0.0015	0.0020	0.0022	0.0026
	X33_P10	X50_P10	X58_P10	X67_P10
A	0.0029	0.0044	0.0052	0.0059
	X75_P10	X84_P10	X100_P10	X134_P10

A	0.0067	0.0075	0.0092	0.0128

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0122	0.0113	5.2937	4.0533
A to Z ↑	0.0199	0.0183	9.7067	7.1989
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0101	0.0090	2.7236	1.7804
A to Z ↑	0.0166	0.0153	4.9061	3.2587
	X17_P10	**X21_P10**	**X17_P10**	**X21_P10**
A to Z ↓	0.0087	0.0094	1.3525	1.0963
A to Z ↑	0.0145	0.0155	2.4072	1.9481
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0092	0.0088	0.9289	0.7942
A to Z ↑	0.0149	0.0143	1.6174	1.3884
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0085	0.0088	0.7009	0.4749
A to Z ↑	0.0139	0.0140	1.2111	0.8110
	X58_P10	**X67_P10**	**X58_P10**	**X67_P10**
A to Z ↓	0.0092	0.0089	0.4114	0.3612
A to Z ↑	0.0145	0.0141	0.6978	0.6115
	X75_P10	**X84_P10**	**X75_P10**	**X84_P10**
A to Z ↓	0.0093	0.0094	0.3255	0.2942
A to Z ↑	0.0144	0.0144	0.5469	0.4938
	X100_P10	**X134_P10**	**X100_P10**	**X134_P10**
A to Z ↓	0.0101	0.0107	0.2497	0.1931
A to Z ↑	0.0150	0.0155	0.4148	0.3173

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.276e-07	5.836e-10
X6_P10	4.125e-07	5.836e-10
X8_P10	5.999e-07	5.836e-10
X13_P10	9.029e-07	7.027e-10
X17_P10	1.152e-06	7.027e-10
X21_P10	1.399e-06	8.218e-10
X25_P10	1.604e-06	8.218e-10
X29_P10	1.870e-06	9.409e-10
X33_P10	2.038e-06	9.409e-10
X50_P10	2.902e-06	1.179e-09
X58_P10	3.336e-06	1.298e-09
X67_P10	3.770e-06	1.417e-09
X75_P10	4.203e-06	1.536e-09
X84_P10	4.637e-06	1.655e-09
X100_P10	5.505e-06	1.894e-09
X134_P10	7.240e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10

A to Z	3.362e-04	3.924e-04	4.723e-04	6.087e-04
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	7.421e-04	1.076e-03	1.209e-03	1.284e-03
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	1.362e-03	2.046e-03	2.614e-03	2.734e-03
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	3.129e-03	3.384e-03	4.071e-03	5.468e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

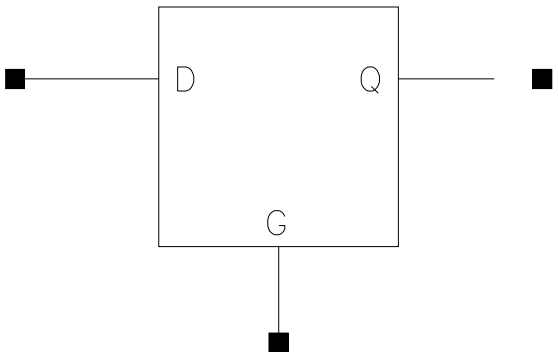
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	7.300e-08	-1.091e-07	-1.302e-07	-1.490e-07
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	3.184e-07	2.666e-07	7.670e-07	1.413e-06
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	-1.820e-08	1.280e-07	3.810e-07	5.800e-08
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	1.658e-06	1.725e-06	-6.100e-08	-1.420e-06

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X23_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P10	X23_P10
D	0.0005	0.0013
G	0.0012	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X23_P10	X8_P10	X23_P10
D to Q ↓	0.0864	0.0667	2.9581	1.4104
D to Q ↑	0.0510	0.0510	4.8348	1.2779
G to Q ↓	0.0912	0.0679	2.9584	1.4112
G to Q ↑	0.0487	0.0443	4.8293	1.2791

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P10	X23_P10
D ↓	hold_falling to G	-0.0331	-0.0184
D ↑	hold_falling to G	-0.0118	-0.0118
D ↓	setup_falling to G	0.0855	0.0581
D ↑	setup_falling to G	0.0520	0.0568
G ↑	min_pulse_width to G	0.0781	0.0618

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.596e-06	1.417e-09
X23_P10	2.888e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X23_P10
D (output stable)	1.568e-05	6.860e-05
G (output stable)	7.677e-04	1.481e-03
D to Q	3.499e-03	6.807e-03
G to Q	3.219e-03	5.959e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

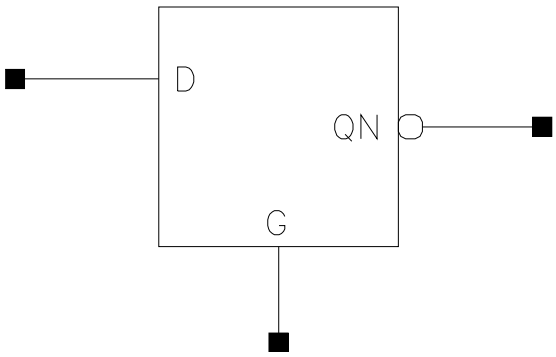
Pin Cycle (vdds)	X8_P10	X23_P10
D (output stable)	-8.629e-07	-3.549e-06
G (output stable)	7.642e-06	1.620e-05
D to Q	-1.615e-06	-3.316e-06
G to Q	2.856e-05	1.860e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P10
D	0.0006
G	0.0013

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P10	X17_P10
D to QN ↓	0.0690	1.3596
D to QN ↑	0.0948	2.3722
G to QN ↓	0.0663	1.3601
G to QN ↑	0.0958	2.3688

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P10
D ↓	hold_falling to G	-0.0410
D ↑	hold_falling to G	-0.0174
D ↓	setup_falling to G	0.0709
D ↑	setup_falling to G	0.0474
G ↑	min_pulse_width to G	0.0626

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P10	2.363e-06	1.536e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X17_P10
D (output stable)	1.903e-05
G (output stable)	8.374e-04
D to QN	4.503e-03
G to QN	4.093e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

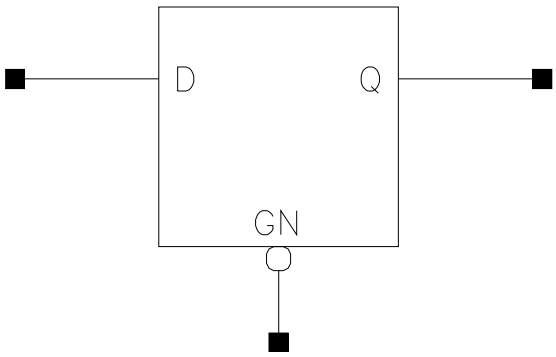
Pin Cycle (vdds)	X17_P10
D (output stable)	-1.949e-06
G (output stable)	8.962e-06
D to QN	-1.547e-06
G to QN	5.684e-05

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
D	0.0005	0.0007	0.0017
GN	0.0011	0.0014	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D to Q ↓	0.0872	0.0736	2.9731	1.4468
D to Q ↑	0.0522	0.0474	4.8408	2.4738
GN to Q ↓	0.0766	0.0635	2.9709	1.4482
GN to Q ↑	0.0784	0.0730	4.8379	2.4732

	X33_P10		X33_P10	
D to Q ↓	0.0706		0.7377	
D to Q ↑	0.0403		1.2368	
GN to Q ↓	0.0593		0.7375	
GN to Q ↑	0.0559		1.2368	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P10	X17_P10	X33_P10
D ↓	hold_rising to GN	-0.0407	-0.0284	-0.0287
D ↑	hold_rising to GN	-0.0090	-0.0042	0.0011
D ↓	setup_rising to GN	0.0951	0.0832	0.0784
D ↑	setup_rising to GN	0.0491	0.0438	0.0365
GN ↓	min_pulse_width to GN	0.0981	0.0839	0.0780

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.458e-06	1.417e-09
X17_P10	2.239e-06	1.655e-09
X33_P10	3.622e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
D (output stable)	1.694e-05	2.802e-05	7.793e-05
GN (output stable)	7.667e-04	1.052e-03	1.257e-03
D to Q	3.505e-03	4.874e-03	7.910e-03
GN to Q	5.039e-03	6.802e-03	9.884e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

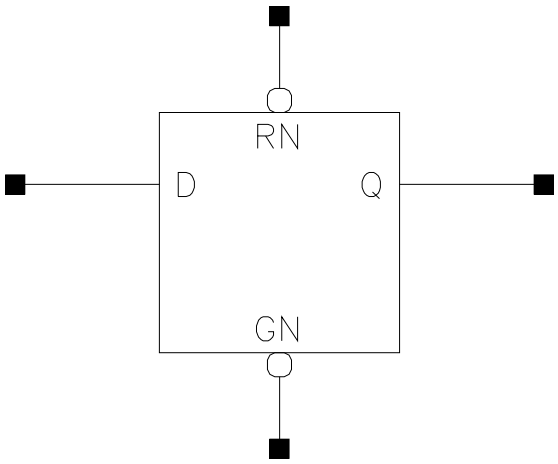
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
D (output stable)	-8.391e-07	-1.183e-06	-3.416e-06
GN (output stable)	7.325e-06	1.259e-05	1.754e-05
D to Q	-1.566e-06	-1.760e-06	-3.095e-06
GN to Q	-3.583e-05	-1.800e-05	-2.191e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.496	1.7952
X33_P10	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X33_P10
D	0.0005	0.0013
GN	0.0013	0.0024
RN	0.0006	0.0006

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
D to Q ↓	0.0812	0.0712	2.8710	0.7436
D to Q ↑	0.0678	0.0836	4.9301	1.2827

GN to Q ↓	0.0719	0.0644	2.8708	0.7440
GN to Q ↑	0.0902	0.0905	4.9307	1.2827
RN to Q ↓	0.0585	0.1076	2.7455	0.8254
RN to Q ↑	0.0730	0.0902	4.9289	1.2819

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P10	X33_P10
D ↓	hold_rising to GN	-0.0358	-0.0256
D ↑	hold_rising to GN	-0.0244	-0.0414
D ↓	setup_rising to GN	0.0857	0.0756
D ↑	setup_rising to GN	0.0633	0.0926
GN ↓	min_pulse_width to GN	0.0875	0.0905
RN ↓	min_pulse_width to RN	0.0703	0.1284
RN ↑	recovery_rising to GN	0.0713	0.0999
RN ↑	removal_rising to GN	-0.0493	-0.0679

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.296e-06	1.655e-09
X33_P10	2.849e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X33_P10
D (output stable)	6.988e-05	9.409e-05
GN (output stable)	8.943e-04	1.326e-03
RN (output stable)	2.446e-05	4.385e-05
D to Q	3.457e-03	8.490e-03
GN to Q	5.108e-03	1.094e-02
RN to Q	2.781e-03	6.446e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

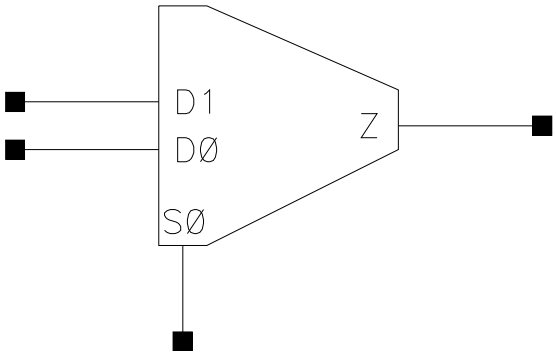
Pin Cycle (vdds)	X8_P10	X33_P10
D (output stable)	-1.703e-06	-2.761e-06
GN (output stable)	4.203e-06	9.551e-06
RN (output stable)	2.088e-07	3.198e-07
D to Q	-1.749e-06	-2.673e-06
GN to Q	-3.431e-05	3.749e-05
RN to Q	2.273e-06	-2.614e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
D0	0.0007	0.0010	0.0013	0.0019
D1	0.0007	0.0010	0.0014	0.0018
S0	0.0013	0.0014	0.0017	0.0024

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D0 to Z ↓	0.0632	0.0548	2.8433	1.3922
D0 to Z ↑	0.0479	0.0426	4.9361	2.4076
D1 to Z ↓	0.0603	0.0546	2.8323	1.3912
D1 to Z ↑	0.0436	0.0398	4.9197	2.4048
S0 to Z ↓	0.0540	0.0508	2.8304	1.3888
S0 to Z ↑	0.0499	0.0485	4.9232	2.4054

	X25_P10	X33_P10	X25_P10	X33_P10
D0 to Z ↓	0.0593	0.0528	0.9636	0.7211
D0 to Z ↑	0.0473	0.0424	1.6206	1.2128
D1 to Z ↓	0.0636	0.0550	0.9667	0.7217
D1 to Z ↑	0.0445	0.0401	1.6183	1.2102
S0 to Z ↓	0.0589	0.0529	0.9631	0.7208
S0 to Z ↑	0.0550	0.0491	1.6179	1.2108

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.806e-06	1.417e-09
X17_P10	2.993e-06	1.536e-09
X25_P10	4.167e-06	2.370e-09
X33_P10	5.646e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	6.814e-04	9.655e-04	1.022e-03	1.352e-03
D1 (output stable)	5.388e-04	8.760e-04	1.164e-03	1.429e-03
S0 (output stable)	9.234e-04	1.046e-03	1.359e-03	1.648e-03
D0 to Z	2.435e-03	3.844e-03	5.989e-03	7.435e-03
D1 to Z	2.227e-03	3.724e-03	6.035e-03	7.292e-03
S0 to Z	2.791e-03	4.123e-03	6.731e-03	8.144e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

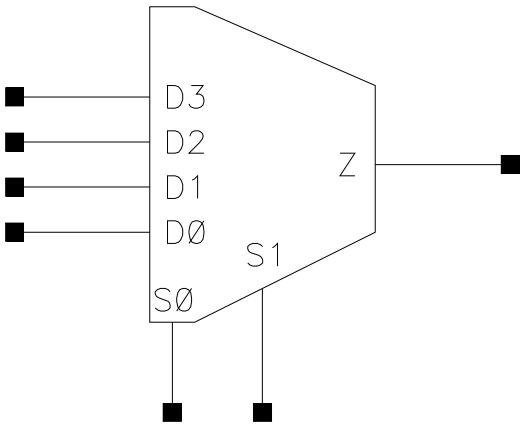
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	-1.170e-08	1.975e-07	-2.430e-07	-4.952e-07
D1 (output stable)	7.065e-08	-2.674e-07	-4.958e-07	-5.920e-07
S0 (output stable)	3.955e-08	-8.070e-08	-1.009e-07	8.900e-09
D0 to Z	-1.911e-07	-1.196e-07	-5.350e-07	-5.980e-07
D1 to Z	-8.595e-08	-1.125e-07	-3.286e-07	-8.915e-07
S0 to Z	-2.442e-08	-2.095e-07	-2.019e-07	-3.348e-07

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.312	2.7744
X31_P10	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P10	X31_P10
D0	0.0005	0.0014
D1	0.0005	0.0013
D2	0.0005	0.0014
D3	0.0005	0.0014
S0	0.0019	0.0036
S1	0.0012	0.0024

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X31_P10	X8_P10	X31_P10

D0 to Z ↓	0.1180	0.1170	3.0368	0.8413
D0 to Z ↑	0.0694	0.0687	4.9819	1.3359
D1 to Z ↓	0.1171	0.1174	3.0331	0.8415
D1 to Z ↑	0.0699	0.0685	4.9824	1.3366
D2 to Z ↓	0.1272	0.1095	3.0592	0.8327
D2 to Z ↑	0.0731	0.0639	5.0033	1.3283
D3 to Z ↓	0.1268	0.1089	3.0585	0.8316
D3 to Z ↑	0.0722	0.0651	4.9982	1.3307
S0 to Z ↓	0.1292	0.1251	3.0422	0.8362
S0 to Z ↑	0.0878	0.0876	4.9957	1.3345
S1 to Z ↓	0.0930	0.0857	3.0464	0.8367
S1 to Z ↑	0.0667	0.0654	4.9904	1.3333

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.749e-06	2.370e-09
X31_P10	4.825e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X31_P10
D0 (output stable)	3.423e-05	1.567e-04
D1 (output stable)	3.319e-05	1.696e-04
D2 (output stable)	2.167e-05	7.869e-05
D3 (output stable)	3.183e-05	1.446e-04
S0 (output stable)	1.429e-03	3.277e-03
S1 (output stable)	9.905e-04	2.126e-03
D0 to Z	2.605e-03	8.630e-03
D1 to Z	2.599e-03	8.670e-03
D2 to Z	2.806e-03	8.080e-03
D3 to Z	2.799e-03	8.062e-03
S0 to Z	4.171e-03	1.197e-02
S1 to Z	2.946e-03	8.080e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

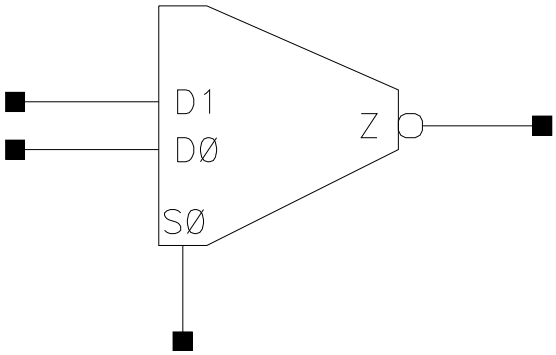
Pin Cycle (vdds)	X8_P10	X31_P10
D0 (output stable)	-2.037e-06	-1.059e-05
D1 (output stable)	-1.195e-06	-6.454e-06
D2 (output stable)	1.768e-07	5.047e-06
D3 (output stable)	-1.863e-06	-2.252e-06
S0 (output stable)	-1.357e-05	-4.385e-05
S1 (output stable)	2.671e-05	1.092e-04
D0 to Z	-2.268e-06	-7.429e-06
D1 to Z	-2.439e-06	-6.457e-06
D2 to Z	-2.275e-06	-6.027e-06
D3 to Z	-2.247e-06	-5.773e-06
S0 to Z	-1.106e-05	-3.624e-05
S1 to Z	3.470e-05	1.426e-04

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.816	0.9792
X5_P10	1.200	0.952	1.1424
X10_P10	1.200	1.768	2.1216
X16_P10	1.200	2.448	2.9376
X21_P10	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P10	X5_P10	X10_P10	X16_P10
D0	0.0005	0.0008	0.0016	0.0024
D1	0.0005	0.0008	0.0015	0.0024
S0	0.0011	0.0020	0.0026	0.0039
	X21_P10			
D0	0.0032			
D1	0.0031			
S0	0.0044			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X5_P10	X3_P10	X5_P10
D0 to Z ↓	0.0207	0.0201	10.0813	5.8516

D0 to Z ↑	0.0381	0.0337	23.3705	11.5727
D1 to Z ↓	0.0203	0.0190	9.9696	5.6416
D1 to Z ↑	0.0397	0.0354	23.3896	11.8687
S0 to Z ↓	0.0321	0.0258	9.9985	5.7478
S0 to Z ↑	0.0360	0.0287	23.3295	11.7095
	X10_P10	**X16_P10**	**X10_P10**	**X16_P10**
D0 to Z ↓	0.0225	0.0209	2.7250	1.7826
D0 to Z ↑	0.0366	0.0348	5.3383	3.5036
D1 to Z ↓	0.0201	0.0198	2.6602	1.7636
D1 to Z ↑	0.0371	0.0360	5.3984	3.5312
S0 to Z ↓	0.0312	0.0270	2.6863	1.7699
S0 to Z ↑	0.0338	0.0293	5.3642	3.5175
	X21_P10		**X21_P10**	
D0 to Z ↓	0.0207		1.3545	
D0 to Z ↑	0.0340		2.6506	
D1 to Z ↓	0.0197		1.3347	
D1 to Z ↑	0.0360		2.6402	
S0 to Z ↓	0.0282		1.3422	
S0 to Z ↑	0.0299		2.6422	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P10	6.865e-07	1.060e-09
X5_P10	1.351e-06	1.179e-09
X10_P10	2.326e-06	1.894e-09
X16_P10	3.524e-06	2.489e-09
X21_P10	4.300e-06	3.085e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	1.703e-05	3.586e-05	1.119e-04	1.797e-04
D1 (output stable)	1.925e-05	1.047e-04	1.117e-04	1.811e-04
S0 (output stable)	7.645e-04	1.072e-03	1.935e-03	2.940e-03
D0 to Z	7.588e-04	1.270e-03	3.169e-03	4.436e-03
D1 to Z	7.600e-04	1.260e-03	3.006e-03	4.395e-03
S0 to Z	1.327e-03	1.834e-03	3.918e-03	5.400e-03
	X21_P10			
D0 (output stable)	2.338e-04			
D1 (output stable)	2.707e-04			
S0 (output stable)	3.285e-03			
D0 to Z	5.672e-03			
D1 to Z	5.782e-03			
S0 to Z	6.610e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	-8.531e-07	-1.238e-06	-3.896e-06	-9.234e-06
D1 (output stable)	-2.112e-06	-1.933e-05	-9.499e-06	-1.672e-05
S0 (output stable)	9.093e-06	3.732e-05	3.594e-05	5.931e-05
D0 to Z	-2.469e-07	1.236e-07	-1.348e-06	-3.898e-06

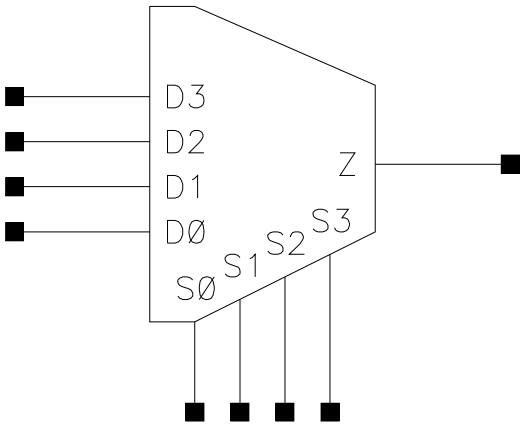
D1 to Z	-3.707e-07	-1.412e-06	-2.052e-06	-2.874e-06
S0 to Z	1.006e-05	3.021e-05	3.952e-05	7.565e-05
	X21_P10			
D0 (output stable)	-1.112e-05			
D1 (output stable)	-3.289e-05			
S0 (output stable)	8.890e-05			
D0 to Z	-2.189e-06			
D1 to Z	-4.949e-06			
S0 to Z	9.816e-05			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	1.768	2.1216
X27_P10	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P10	X27_P10
D0	0.0006	0.0019
D1	0.0006	0.0019
D2	0.0006	0.0019
D3	0.0006	0.0019
S0	0.0006	0.0017
S1	0.0007	0.0018
S2	0.0006	0.0017
S3	0.0007	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	X27_P10	X7_P10	X27_P10
D0 to Z ↓	0.0861	0.0704	4.9845	1.3546
D0 to Z ↑	0.0574	0.0467	4.8520	1.2050
D1 to Z ↓	0.0768	0.0629	4.9769	1.3543
D1 to Z ↑	0.0522	0.0416	4.8283	1.2001
D2 to Z ↓	0.0869	0.0669	4.9996	1.3585
D2 to Z ↑	0.0564	0.0437	4.8739	1.2102
D3 to Z ↓	0.0776	0.0595	4.9903	1.3557
D3 to Z ↑	0.0513	0.0387	4.8540	1.2059
S0 to Z ↓	0.0834	0.0666	4.9805	1.3546
S0 to Z ↑	0.0598	0.0479	4.8523	1.2052
S1 to Z ↓	0.0746	0.0588	4.9751	1.3533
S1 to Z ↑	0.0545	0.0423	4.8299	1.2004
S2 to Z ↓	0.0842	0.0630	4.9994	1.3549
S2 to Z ↑	0.0587	0.0448	4.8717	1.2099
S3 to Z ↓	0.0755	0.0557	4.9835	1.3541
S3 to Z ↑	0.0535	0.0396	4.8494	1.2053

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X7_P10	1.554e-06	1.894e-09
X27_P10	5.368e-06	3.561e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X7_P10	X27_P10
D0 (output stable)	4.233e-04	1.320e-03
D1 (output stable)	3.311e-04	1.007e-03
D2 (output stable)	4.075e-04	1.278e-03
D3 (output stable)	3.096e-04	9.616e-04
S0 (output stable)	4.315e-04	1.308e-03
S1 (output stable)	3.267e-04	9.818e-04
S2 (output stable)	3.903e-04	1.226e-03
S3 (output stable)	2.976e-04	9.287e-04
D0 to Z	3.183e-03	9.773e-03
D1 to Z	2.780e-03	8.374e-03
D2 to Z	3.072e-03	8.446e-03
D3 to Z	2.673e-03	7.073e-03
S0 to Z	3.106e-03	9.265e-03
S1 to Z	2.701e-03	7.865e-03
S2 to Z	2.994e-03	7.924e-03
S3 to Z	2.594e-03	6.582e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

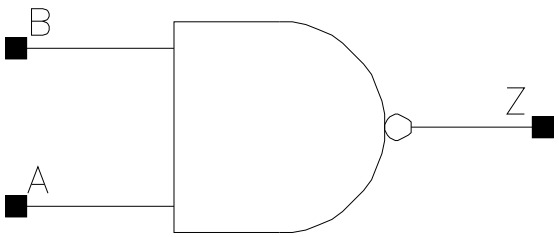
Pin Cycle (vdds)	X7_P10	X27_P10
D0 (output stable)	-2.212e-06	-4.159e-06
D1 (output stable)	2.599e-06	1.531e-05
D2 (output stable)	-4.056e-06	-6.713e-06
D3 (output stable)	7.472e-06	2.425e-05
S0 (output stable)	-4.944e-06	-8.983e-06
S1 (output stable)	7.639e-06	2.441e-05
S2 (output stable)	-2.139e-06	-3.795e-06
S3 (output stable)	5.305e-06	2.131e-05
D0 to Z	-3.604e-06	-5.540e-06
D1 to Z	-2.984e-07	-1.247e-06
D2 to Z	-3.099e-06	-4.747e-06
D3 to Z	-5.978e-08	-7.835e-07
S0 to Z	-3.440e-06	-4.921e-06
S1 to Z	-2.872e-07	-8.446e-07
S2 to Z	-2.914e-06	-3.991e-06
S3 to Z	-5.119e-08	-3.561e-07

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P10	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P10	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P10	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P10	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P10	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P10	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P10	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P10	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P10	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P10	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P10	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P10	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P10	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P10	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P10	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P10	C12T28SOI_LR_-NAND2X5_P10	C12T28SOI_LR_-NAND2X7_P10	C12T28SOI_LR_-NAND2X10_P10
A	0.0005	0.0007	0.0008	0.0013
B	0.0005	0.0007	0.0008	0.0012
	C12T28SOI_LR_-NAND2X13_P10	C12T28SOI_LR_-NAND2X17_P10	C12T28SOI_LR_-NAND2X20_P10	C12T28SOI_LR_-NAND2X24_P10
A	0.0015	0.0020	0.0023	0.0028
B	0.0014	0.0019	0.0021	0.0025
	C12T28SOI_LR_-NAND2X27_P10	C12T28SOI_LR_-NAND2X42_P10	C12T28SOI_LR_-NAND2X47_P10	C12T28SOI_LR_-NAND2X50_P10
A	0.0030	0.0010	0.0010	0.0010
B	0.0028	0.0010	0.0010	0.0010
	C12T28SOI_LR_-NAND2X58_P10	C12T28SOI_LR_-NAND2X67_P10	C12T28SOI_-LRBR0D8_-NAND2X7_P10	C12T28SOI_-LRBR0D8_-NAND2X14_P10
A	0.0010	0.0010	0.0008	0.0015
B	0.0010	0.0010	0.0008	0.0014
	C12T28SOI_LRS_-NAND2X40_P10	C12T28SOI_LRS_-NAND2X54_P10		
A	0.0046	0.0060		
B	0.0042	0.0056		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P10	**C12T28SOI_LR_-NAND2X5_P10**	**C12T28SOI_LR_-NAND2X3_P10**	**C12T28SOI_LR_-NAND2X5_P10**
A to Z ↓	0.0159	0.0142	9.7300	6.0763
A to Z ↑	0.0231	0.0209	9.6914	6.0552
B to Z ↓	0.0169	0.0144	9.8063	6.1311
B to Z ↑	0.0214	0.0186	9.7395	6.0900
	C12T28SOI_LR_-NAND2X7_P10	**C12T28SOI_LR_-NAND2X10_P10**	**C12T28SOI_LR_-NAND2X7_P10**	**C12T28SOI_LR_-NAND2X10_P10**
A to Z ↓	0.0140	0.0164	5.0562	3.4046
A to Z ↑	0.0202	0.0218	4.8743	3.2258
B to Z ↓	0.0141	0.0142	5.0974	3.4271
B to Z ↑	0.0180	0.0181	4.9123	3.2458
	C12T28SOI_LR_-NAND2X13_P10	**C12T28SOI_LR_-NAND2X17_P10**	**C12T28SOI_LR_-NAND2X13_P10**	**C12T28SOI_LR_-NAND2X17_P10**
A to Z ↓	0.0154	0.0155	2.5748	2.0655

A to Z ↑	0.0205	0.0209	2.3896	1.9373
B to Z ↓	0.0133	0.0141	2.6017	2.0825
B to Z ↑	0.0167	0.0176	2.4052	1.9487
	C12T28SOI_LR_-NAND2X20_P10	**C12T28SOI_LR_-NAND2X24_P10**	**C12T28SOI_LR_-NAND2X20_P10**	**C12T28SOI_LR_-NAND2X24_P10**
A to Z ↓	0.0151	0.0158	1.7625	1.5120
A to Z ↑	0.0203	0.0208	1.6067	1.3785
B to Z ↓	0.0139	0.0136	1.7759	1.5219
B to Z ↑	0.0171	0.0170	1.6176	1.3870
	C12T28SOI_LR_-NAND2X27_P10	**C12T28SOI_LR_-NAND2X42_P10**	**C12T28SOI_LR_-NAND2X27_P10**	**C12T28SOI_LR_-NAND2X42_P10**
A to Z ↓	0.0154	0.0554	1.3356	0.5695
A to Z ↑	0.0202	0.0565	1.2048	0.9585
B to Z ↓	0.0133	0.0564	1.3483	0.5701
B to Z ↑	0.0164	0.0545	1.2122	0.9602
	C12T28SOI_LR_-NAND2X47_P10	**C12T28SOI_LR_-NAND2X50_P10**	**C12T28SOI_LR_-NAND2X47_P10**	**C12T28SOI_LR_-NAND2X50_P10**
A to Z ↓	0.0572	0.0577	0.5082	0.4766
A to Z ↑	0.0575	0.0579	0.8364	0.8013
B to Z ↓	0.0582	0.0587	0.5088	0.4763
B to Z ↑	0.0555	0.0559	0.8361	0.8004
	C12T28SOI_LR_-NAND2X58_P10	**C12T28SOI_LR_-NAND2X67_P10**	**C12T28SOI_LR_-NAND2X58_P10**	**C12T28SOI_LR_-NAND2X67_P10**
A to Z ↓	0.0606	0.0624	0.4137	0.3644
A to Z ↑	0.0599	0.0610	0.6884	0.6052
B to Z ↓	0.0617	0.0635	0.4134	0.3646
B to Z ↑	0.0580	0.0591	0.6885	0.6056
	C12T28SOI_-LRBR0D8_-NAND2X7_P10	**C12T28SOI_-LRBR0D8_-NAND2X14_P10**	**C12T28SOI_-LRBR0D8_-NAND2X7_P10**	**C12T28SOI_-LRBR0D8_-NAND2X14_P10**
A to Z ↓	0.0121	0.0136	3.7641	1.9641
A to Z ↑	0.0240	0.0245	6.5651	3.2001
B to Z ↓	0.0116	0.0107	3.8027	1.9906
B to Z ↑	0.0204	0.0185	6.7490	3.2537
	C12T28SOI_LRS_-NAND2X40_P10	**C12T28SOI_LRS_-NAND2X54_P10**	**C12T28SOI_LRS_-NAND2X40_P10**	**C12T28SOI_LRS_-NAND2X54_P10**
A to Z ↓	0.0153	0.0152	0.9041	0.6838
A to Z ↑	0.0201	0.0200	0.8067	0.6073
B to Z ↓	0.0134	0.0135	0.9125	0.6914
B to Z ↑	0.0164	0.0164	0.8120	0.6121

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P10	3.385e-07	7.027e-10
C12T28SOI_LR_NAND2X5_P10	5.302e-07	7.027e-10
C12T28SOI_LR_NAND2X7_P10	6.274e-07	7.027e-10
C12T28SOI_LR_NAND2X10_P10	8.865e-07	9.409e-10
C12T28SOI_LR_NAND2X13_P10	1.140e-06	9.409e-10
C12T28SOI_LR_NAND2X17_P10	1.406e-06	1.179e-09
C12T28SOI_LR_NAND2X20_P10	1.617e-06	1.179e-09
C12T28SOI_LR_NAND2X24_P10	1.922e-06	1.417e-09
C12T28SOI_LR_NAND2X27_P10	2.096e-06	1.417e-09

C12T28SOI_LR_NAND2X42_P10	4.223e-06	1.536e-09
C12T28SOI_LR_NAND2X47_P10	4.710e-06	1.655e-09
C12T28SOI_LR_NAND2X50_P10	4.777e-06	1.655e-09
C12T28SOI_LR_NAND2X58_P10	5.330e-06	1.775e-09
C12T28SOI_LR_NAND2X67_P10	5.883e-06	1.894e-09
C12T28SOI_LRBR0D8_NAND2X7_-P10	7.540e-07	1.296e-09
C12T28SOI_LRBR0D8_NAND2X14_-P10	1.357e-06	1.549e-09
C12T28SOI_LRS_NAND2X40_P10	3.056e-06	1.894e-09
C12T28SOI_LRS_NAND2X54_P10	4.015e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P10	C12T28SOI_LR_-NAND2X5_P10	C12T28SOI_LR_-NAND2X7_P10	C12T28SOI_LR_-NAND2X10_P10
A (output stable)	1.077e-05	1.720e-05	2.061e-05	6.308e-05
B (output stable)	2.404e-05	3.801e-05	4.692e-05	2.657e-04
A to Z	5.043e-04	6.582e-04	7.774e-04	1.428e-03
B to Z	4.111e-04	5.026e-04	5.874e-04	9.065e-04
	C12T28SOI_LR_-NAND2X13_P10	C12T28SOI_LR_-NAND2X17_P10	C12T28SOI_LR_-NAND2X20_P10	C12T28SOI_LR_-NAND2X24_P10
A (output stable)	7.530e-05	9.457e-05	1.050e-04	1.415e-04
B (output stable)	3.067e-04	3.103e-04	3.421e-04	5.206e-04
A to Z	1.697e-03	2.170e-03	2.447e-03	3.030e-03
B to Z	1.054e-03	1.451e-03	1.643e-03	1.915e-03
	C12T28SOI_LR_-NAND2X27_P10	C12T28SOI_LR_-NAND2X42_P10	C12T28SOI_LR_-NAND2X47_P10	C12T28SOI_LR_-NAND2X50_P10
A (output stable)	1.512e-04	2.278e-05	2.287e-05	2.287e-05
B (output stable)	5.514e-04	5.394e-05	5.417e-05	5.401e-05
A to Z	3.262e-03	8.542e-03	9.186e-03	9.423e-03
B to Z	2.034e-03	8.350e-03	8.990e-03	9.229e-03
	C12T28SOI_LR_-NAND2X58_P10	C12T28SOI_LR_-NAND2X67_P10	C12T28SOI_-LRBR0D8_-NAND2X7_P10	C12T28SOI_-LRBR0D8_-NAND2X14_P10
A (output stable)	2.295e-05	2.304e-05	2.690e-05	9.441e-05
B (output stable)	5.411e-05	5.439e-05	6.259e-05	3.874e-04
A to Z	1.069e-02	1.156e-02	8.162e-04	1.805e-03
B to Z	1.050e-02	1.136e-02	5.550e-04	9.618e-04
	C12T28SOI_LRS_-NAND2X40_P10	C12T28SOI_LRS_-NAND2X54_P10		
A (output stable)	2.179e-04	2.833e-04		
B (output stable)	7.681e-04	9.776e-04		
A to Z	4.824e-03	6.307e-03		
B to Z	3.041e-03	4.010e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P10	C12T28SOI_LR_-NAND2X5_P10	C12T28SOI_LR_-NAND2X7_P10	C12T28SOI_LR_-NAND2X10_P10
A (output stable)	4.350e-08	3.050e-08	5.670e-09	2.130e-08
B (output stable)	2.270e-08	2.000e-10	-6.860e-09	-1.791e-06
A to Z	-5.340e-08	-1.702e-07	5.220e-08	-4.200e-08

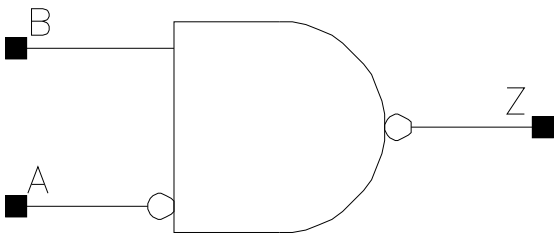
B to Z	1.587e-07	5.600e-09	2.800e-09	-8.590e-08
	C12T28SOI_LR_-NAND2X13_P10	C12T28SOI_LR_-NAND2X17_P10	C12T28SOI_LR_-NAND2X20_P10	C12T28SOI_LR_-NAND2X24_P10
A (output stable)	-2.840e-08	-5.320e-08	-1.193e-07	-8.360e-08
B (output stable)	-1.774e-06	-1.613e-06	-2.088e-07	-3.292e-06
A to Z	-1.047e-07	-1.270e-07	-1.556e-06	-2.145e-06
B to Z	-2.848e-07	3.800e-07	-4.080e-07	-6.020e-07
	C12T28SOI_LR_-NAND2X27_P10	C12T28SOI_LR_-NAND2X42_P10	C12T28SOI_LR_-NAND2X47_P10	C12T28SOI_LR_-NAND2X50_P10
A (output stable)	-1.263e-07	7.690e-09	8.320e-09	8.610e-09
B (output stable)	-3.067e-06	-1.348e-08	-1.272e-08	-1.267e-08
A to Z	-2.216e-06	-1.178e-06	-9.550e-07	-4.710e-07
B to Z	6.600e-08	-8.080e-07	-2.620e-07	-2.580e-07
	C12T28SOI_LR_-NAND2X58_P10	C12T28SOI_LR_-NAND2X67_P10	C12T28SOI_-LRBR0D8_-NAND2X7_P10	C12T28SOI_-LRBR0D8_-NAND2X14_P10
A (output stable)	8.840e-09	9.030e-09	3.126e-08	1.121e-07
B (output stable)	-1.243e-08	-1.204e-08	1.613e-08	-6.711e-06
A to Z	-9.410e-07	-7.050e-07	-6.950e-08	-1.291e-06
B to Z	-5.110e-07	-4.630e-07	1.243e-07	-9.470e-08
	C12T28SOI_LRS_-NAND2X40_P10	C12T28SOI_LRS_-NAND2X54_P10		
A (output stable)	-3.385e-07	-4.421e-07		
B (output stable)	-4.014e-06	-5.673e-06		
A to Z	-6.390e-07	-5.259e-06		
B to Z	1.480e-07	-1.630e-06		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X7_P10	1.200	0.544	0.6528
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X40_P10	1.200	2.312	2.7744
X54_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P10	X7_P10	X13_P10	X27_P10
A	0.0008	0.0008	0.0010	0.0019
B	0.0005	0.0008	0.0014	0.0028
	X40_P10	X54_P10		
A	0.0029	0.0037		
B	0.0041	0.0056		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0422	0.0441	9.7782	5.0777
A to Z ↑	0.0322	0.0330	9.5582	4.8504
B to Z ↓	0.0172	0.0141	9.9301	5.1480
B to Z ↑	0.0215	0.0179	9.7444	4.9480
	X13_P10	**X27_P10**	**X13_P10**	**X27_P10**

A to Z ↓	0.0402	0.0389	2.6730	1.3335
A to Z ↑	0.0304	0.0295	2.4801	1.2024
B to Z ↓	0.0129	0.0130	2.7162	1.3553
B to Z ↑	0.0165	0.0162	2.4651	1.2146
	X40_P10	**X54_P10**	**X40_P10**	**X54_P10**
A to Z ↓	0.0399	0.0395	0.8944	0.6782
A to Z ↑	0.0304	0.0301	0.8008	0.6034
B to Z ↓	0.0131	0.0132	0.9081	0.6898
B to Z ↑	0.0162	0.0162	0.8146	0.6144

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P10	6.048e-07	8.218e-10
X7_P10	8.914e-07	8.218e-10
X13_P10	1.764e-06	1.179e-09
X27_P10	3.197e-06	1.775e-09
X40_P10	4.593e-06	2.370e-09
X54_P10	5.987e-06	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	8.171e-04	1.042e-03	1.658e-03	3.182e-03
B (output stable)	2.535e-05	4.798e-05	2.860e-04	5.016e-04
A to Z	1.403e-03	1.935e-03	3.510e-03	6.822e-03
B to Z	4.185e-04	5.822e-04	1.018e-03	2.020e-03
	X40_P10	X54_P10		
A (output stable)	4.972e-03	6.428e-03		
B (output stable)	7.331e-04	9.551e-04		
A to Z	1.041e-02	1.366e-02		
B to Z	2.975e-03	3.950e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

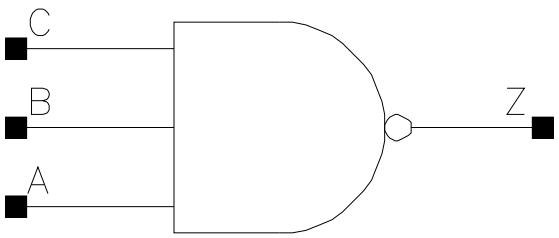
Pin Cycle (vdds)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	-1.135e-07	-1.067e-07	-1.345e-07	-3.374e-07
B (output stable)	2.340e-08	-6.160e-09	-8.800e-08	-2.059e-06
A to Z	-1.019e-07	8.300e-09	-1.824e-07	-4.060e-07
B to Z	7.620e-08	-1.500e-09	1.000e-07	-7.850e-07
	X40_P10	X54_P10		
A (output stable)	-5.690e-07	-7.810e-07		
B (output stable)	-3.280e-06	-5.175e-06		
A to Z	-6.530e-07	-9.160e-07		
B to Z	-3.880e-07	-1.480e-07		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P10	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P10	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P10	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P10	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P10	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P10	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P10	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P10	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P10	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P10	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P10	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P10	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P10	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P10	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P10	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A	0.0006	0.0008	0.0013	0.0015
B	0.0007	0.0008	0.0012	0.0015
C	0.0006	0.0008	0.0012	0.0014
	C12T28SOI_LR_-NAND3X15_P10	C12T28SOI_LR_-NAND3X18_P10	C12T28SOI_LR_-NAND3X21_P10	C12T28SOI_LR_-NAND3X24_P10
A	0.0020	0.0023	0.0027	0.0030
B	0.0019	0.0022	0.0026	0.0029
C	0.0018	0.0021	0.0025	0.0028
	C12T28SOI_LR_-NAND3X35_P10	C12T28SOI_LR_-NAND3X47_P10	C12T28SOI_-LRBR0P6_-NAND3X6_P10	C12T28SOI_-LRBR0P6_-NAND3X12_P10
A	0.0046	0.0060	0.0008	0.0016
B	0.0044	0.0058	0.0008	0.0015
C	0.0042	0.0056	0.0008	0.0014
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	C12T28SOI_-LRBR0P6_-NAND3X24_P10	C12T28SOI_-LRBR0P6_-NAND3X35_P10	C12T28SOI_-LRBR0P6_-NAND3X47_P10
A	0.0023	0.0030	0.0046	0.0060
B	0.0021	0.0029	0.0043	0.0058
C	0.0020	0.0027	0.0040	0.0054
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10			
A	0.0024			
B	0.0023			
C	0.0021			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10
A to Z ↓	0.0252	0.0224	10.2630	7.1983
A to Z ↑	0.0285	0.0258	6.9464	4.7279
B to Z ↓	0.0261	0.0229	10.2790	7.2111
B to Z ↑	0.0275	0.0245	6.9584	4.7369
C to Z ↓	0.0225	0.0199	10.3174	7.2303
C to Z ↑	0.0240	0.0214	6.9643	4.7641

	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A to Z ↓	0.0251	0.0231	4.9591	3.7919
A to Z ↑	0.0272	0.0254	3.2434	2.4120
B to Z ↓	0.0235	0.0218	4.9653	3.7991
B to Z ↑	0.0249	0.0233	3.2451	2.4147
C to Z ↓	0.0202	0.0188	4.9821	3.8081
C to Z ↑	0.0214	0.0199	3.2365	2.3974
	C12T28SOI_LR_-NAND3X15_P10	**C12T28SOI_LR_-NAND3X18_P10**	**C12T28SOI_LR_-NAND3X15_P10**	**C12T28SOI_LR_-NAND3X18_P10**
A to Z ↓	0.0228	0.0218	3.0995	2.6335
A to Z ↑	0.0251	0.0240	1.9348	1.6042
B to Z ↓	0.0221	0.0212	3.1040	2.6369
B to Z ↑	0.0230	0.0221	1.9377	1.6069
C to Z ↓	0.0194	0.0183	3.1141	2.6452
C to Z ↑	0.0200	0.0188	1.9501	1.6161
	C12T28SOI_LR_-NAND3X21_P10	**C12T28SOI_LR_-NAND3X24_P10**	**C12T28SOI_LR_-NAND3X21_P10**	**C12T28SOI_LR_-NAND3X24_P10**
A to Z ↓	0.0232	0.0227	2.2317	1.9784
A to Z ↑	0.0252	0.0246	1.3849	1.2117
B to Z ↓	0.0220	0.0216	2.2337	1.9803
B to Z ↑	0.0231	0.0226	1.3864	1.2129
C to Z ↓	0.0191	0.0187	2.2413	1.9870
C to Z ↑	0.0198	0.0193	1.3872	1.2125
	C12T28SOI_LR_-NAND3X35_P10	**C12T28SOI_LR_-NAND3X47_P10**	**C12T28SOI_LR_-NAND3X35_P10**	**C12T28SOI_LR_-NAND3X47_P10**
A to Z ↓	0.0217	0.0220	1.3473	1.0228
A to Z ↑	0.0238	0.0240	0.8102	0.6115
B to Z ↓	0.0210	0.0212	1.3495	1.0246
B to Z ↑	0.0219	0.0220	0.8099	0.6098
C to Z ↓	0.0182	0.0184	1.3549	1.0287
C to Z ↑	0.0186	0.0186	0.8145	0.6128
	C12T28SOI_-LRBR0P6_-NAND3X6_P10	**C12T28SOI_-LRBR0P6_-NAND3X12_P10**	**C12T28SOI_-LRBR0P6_-NAND3X6_P10**	**C12T28SOI_-LRBR0P6_-NAND3X12_P10**
A to Z ↓	0.0180	0.0187	4.8048	2.5207
A to Z ↑	0.0352	0.0350	7.6224	3.8831
B to Z ↓	0.0180	0.0170	4.8247	2.5326
B to Z ↑	0.0321	0.0303	7.6392	3.8893
C to Z ↓	0.0143	0.0129	4.8551	2.5512
C to Z ↑	0.0255	0.0230	7.6771	3.8977
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	**C12T28SOI_-LRBR0P6_-NAND3X24_P10**	**C12T28SOI_-LRBR0P6_-NAND3X18_P10**	**C12T28SOI_-LRBR0P6_-NAND3X24_P10**
A to Z ↓	0.0176	0.0181	1.7482	1.3114
A to Z ↑	0.0331	0.0338	2.5836	1.9494
B to Z ↓	0.0164	0.0165	1.7556	1.3171
B to Z ↑	0.0287	0.0292	2.5899	1.9527
C to Z ↓	0.0131	0.0128	1.7691	1.3279
C to Z ↑	0.0224	0.0223	2.6059	1.9555
	C12T28SOI_-LRBR0P6_-NAND3X35_P10	**C12T28SOI_-LRBR0P6_-NAND3X47_P10**	**C12T28SOI_-LRBR0P6_-NAND3X35_P10**	**C12T28SOI_-LRBR0P6_-NAND3X47_P10**

A to Z ↓	0.0176	0.0177	0.8943	0.6805
A to Z ↑	0.0334	0.0333	1.3319	1.0060
B to Z ↓	0.0163	0.0162	0.8984	0.6846
B to Z ↑	0.0288	0.0286	1.3331	1.0066
C to Z ↓	0.0124	0.0128	0.9062	0.6893
C to Z ↑	0.0216	0.0218	1.3455	1.0106
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P10**	
A to Z ↓	0.0181		1.6497	
A to Z ↑	0.0330		2.3940	
B to Z ↓	0.0163		1.6571	
B to Z ↑	0.0285		2.3980	
C to Z ↓	0.0120		1.6710	
C to Z ↑	0.0212		2.3831	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P10	4.168e-07	9.409e-10
C12T28SOI_LR_NAND3X6_P10	5.810e-07	9.409e-10
C12T28SOI_LR_NAND3X9_P10	8.046e-07	1.298e-09
C12T28SOI_LR_NAND3X12_P10	1.029e-06	1.298e-09
C12T28SOI_LR_NAND3X15_P10	1.179e-06	1.536e-09
C12T28SOI_LR_NAND3X18_P10	1.358e-06	1.536e-09
C12T28SOI_LR_NAND3X21_P10	1.710e-06	2.013e-09
C12T28SOI_LR_NAND3X24_P10	1.865e-06	2.013e-09
C12T28SOI_LR_NAND3X35_P10	2.701e-06	2.727e-09
C12T28SOI_LR_NAND3X47_P10	3.533e-06	3.442e-09
C12T28SOI_LRBR0P6_NAND3X6_-P10	7.518e-07	1.615e-09
C12T28SOI_LRBR0P6_NAND3X12_-P10	1.365e-06	2.005e-09
C12T28SOI_LRBR0P6_NAND3X18_-P10	1.806e-06	2.266e-09
C12T28SOI_LRBR0P6_NAND3X24_-P10	2.532e-06	2.786e-09
C12T28SOI_LRBR0P6_NAND3X35_-P10	3.705e-06	3.566e-09
C12T28SOI_LRBR0P6_NAND3X47_-P10	4.872e-06	4.346e-09
C12T28SOIDV_LRBR0P6_-NAND3X18_P10	2.192e-06	1.874e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A (output stable)	1.425e-05	2.172e-05	5.293e-05	6.346e-05
B (output stable)	5.509e-05	7.022e-05	1.628e-04	1.938e-04
C (output stable)	2.034e-04	2.414e-04	4.030e-04	4.660e-04
A to Z	1.183e-03	1.434e-03	2.381e-03	2.791e-03
B to Z	1.065e-03	1.252e-03	1.905e-03	2.234e-03
C to Z	8.038e-04	9.402e-04	1.375e-03	1.598e-03

	C12T28SOI_LR_-NAND3X15_P10	C12T28SOI_LR_-NAND3X18_P10	C12T28SOI_LR_-NAND3X21_P10	C12T28SOI_LR_-NAND3X24_P10
A (output stable)	7.431e-05	8.318e-05	1.119e-04	1.220e-04
B (output stable)	2.227e-04	2.560e-04	3.307e-04	3.637e-04
C (output stable)	4.989e-04	5.729e-04	7.728e-04	8.311e-04
A to Z	3.351e-03	3.706e-03	4.780e-03	5.211e-03
B to Z	2.695e-03	2.957e-03	3.825e-03	4.160e-03
C to Z	1.988e-03	2.103e-03	2.751e-03	2.977e-03
	C12T28SOI_LR_-NAND3X35_P10	C12T28SOI_LR_-NAND3X47_P10	C12T28SOI_-LRBR0P6_-NAND3X6_P10	C12T28SOI_-LRBR0P6_-NAND3X12_P10
A (output stable)	1.624e-04	2.094e-04	3.099e-05	9.046e-05
B (output stable)	4.937e-04	6.415e-04	1.031e-04	2.827e-04
C (output stable)	1.194e-03	1.533e-03	3.316e-04	6.736e-04
A to Z	7.297e-03	9.682e-03	1.555e-03	3.072e-03
B to Z	5.819e-03	7.747e-03	1.278e-03	2.260e-03
C to Z	4.048e-03	5.454e-03	8.146e-04	1.301e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	C12T28SOI_-LRBR0P6_-NAND3X24_P10	C12T28SOI_-LRBR0P6_-NAND3X35_P10	C12T28SOI_-LRBR0P6_-NAND3X47_P10
A (output stable)	1.150e-04	1.720e-04	2.339e-04	3.076e-04
B (output stable)	3.543e-04	5.245e-04	7.219e-04	9.532e-04
C (output stable)	7.775e-04	1.208e-03	1.766e-03	2.197e-03
A to Z	4.085e-03	5.711e-03	8.189e-03	1.063e-02
B to Z	3.004e-03	4.184e-03	5.960e-03	7.741e-03
C to Z	1.829e-03	2.416e-03	3.292e-03	4.373e-03
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10			
A (output stable)	1.319e-04			
B (output stable)	4.278e-04			
C (output stable)	9.848e-04			
A to Z	4.454e-03			
B to Z	3.250e-03			
C to Z	1.793e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A (output stable)	4.343e-08	1.757e-08	1.030e-07	-5.147e-08
B (output stable)	2.152e-08	3.653e-09	-3.379e-07	-7.510e-08
C (output stable)	1.917e-08	8.833e-09	-2.270e-06	-8.073e-08
A to Z	2.080e-07	2.310e-07	2.000e-07	-5.700e-07
B to Z	-2.518e-07	-2.420e-07	-3.700e-07	-3.820e-07
C to Z	5.990e-08	6.900e-08	9.100e-08	2.100e-07
	C12T28SOI_LR_-NAND3X15_P10	C12T28SOI_LR_-NAND3X18_P10	C12T28SOI_LR_-NAND3X21_P10	C12T28SOI_LR_-NAND3X24_P10
A (output stable)	-1.523e-08	-5.297e-08	1.018e-07	-1.017e-08
B (output stable)	-4.557e-07	-4.954e-07	-1.732e-06	-8.256e-07
C (output stable)	-1.946e-06	-1.880e-06	-4.897e-06	-3.688e-06
A to Z	-6.100e-08	1.000e-09	-1.165e-06	-9.460e-07
B to Z	-3.970e-07	2.810e-07	-7.230e-07	-1.194e-06

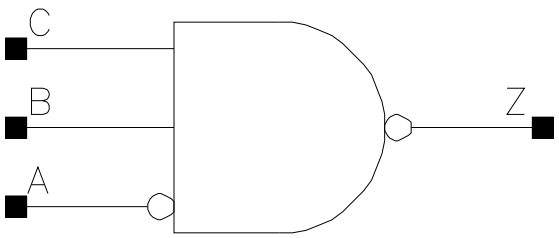
C to Z	-2.710e-07	9.390e-07	1.430e-07	-2.990e-07
	C12T28SOI_LR_-NAND3X35_P10	C12T28SOI_LR_-NAND3X47_P10	C12T28SOI_-LRBR0P6_-NAND3X6_P10	C12T28SOI_-LRBR0P6_-NAND3X12_P10
A (output stable)	-5.463e-08	-1.035e-07	2.061e-07	3.946e-07
B (output stable)	-1.372e-06	-1.780e-06	-7.357e-07	-2.619e-06
C (output stable)	-5.648e-06	-6.861e-06	-4.749e-06	-6.969e-06
A to Z	3.740e-07	5.100e-08	-3.680e-08	-9.360e-07
B to Z	-1.736e-06	-2.376e-06	-4.274e-07	2.940e-07
C to Z	2.360e-07	1.970e-07	-3.430e-08	-2.670e-07
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	C12T28SOI_-LRBR0P6_-NAND3X24_P10	C12T28SOI_-LRBR0P6_-NAND3X35_P10	C12T28SOI_-LRBR0P6_-NAND3X47_P10
A (output stable)	-5.303e-08	4.111e-07	1.801e-07	-1.028e-07
B (output stable)	-7.296e-08	-3.271e-06	-1.593e-06	-8.673e-07
C (output stable)	-1.030e-07	-8.759e-06	-7.589e-06	-3.051e-06
A to Z	-2.495e-06	-2.044e-06	-3.980e-07	-2.210e-07
B to Z	-1.388e-06	2.620e-07	-2.933e-06	-4.076e-06
C to Z	-2.420e-07	-1.050e-07	-8.460e-07	1.567e-06
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10			
A (output stable)	-5.897e-08			
B (output stable)	-1.008e-07			
C (output stable)	-1.132e-07			
A to Z	-1.612e-06			
B to Z	-1.763e-06			
C to Z	-2.590e-07			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.816	0.9792
X12_P10	1.200	1.224	1.4688
X18_P10	1.200	1.496	1.7952
X24_P10	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0008	0.0011	0.0011	0.0019
B	0.0008	0.0015	0.0022	0.0029
C	0.0007	0.0014	0.0021	0.0028

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X12_P10**	**X6_P10**	**X12_P10**
A to Z ↓	0.0502	0.0473	7.3117	3.8348
A to Z ↑	0.0356	0.0335	4.7064	2.3627
B to Z ↓	0.0200	0.0207	7.3393	3.8543
B to Z ↑	0.0224	0.0220	4.7496	2.3889
C to Z ↓	0.0195	0.0175	7.3602	3.8652
C to Z ↑	0.0203	0.0185	4.7734	2.4035
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0539	0.0458	2.6389	1.9854

A to Z ↑	0.0382	0.0318	1.5896	1.1900
B to Z ↓	0.0212	0.0207	2.6460	1.9930
B to Z ↑	0.0221	0.0218	1.6076	1.2073
C to Z ↓	0.0184	0.0175	2.6554	2.0007
C to Z ↑	0.0190	0.0182	1.6159	1.2146

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P10	7.853e-07	1.060e-09
X12_P10	1.558e-06	1.417e-09
X18_P10	1.864e-06	1.655e-09
X24_P10	3.022e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	1.015e-03	1.768e-03	2.409e-03	3.229e-03
B (output stable)	5.754e-05	1.698e-04	2.668e-04	3.718e-04
C (output stable)	1.153e-04	4.660e-04	5.832e-04	8.700e-04
A to Z	2.355e-03	4.583e-03	6.598e-03	8.734e-03
B to Z	1.026e-03	2.005e-03	2.980e-03	3.858e-03
C to Z	8.287e-04	1.363e-03	2.126e-03	2.612e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

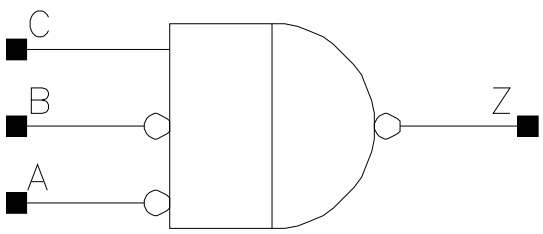
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	-1.155e-07	-7.613e-08	-2.334e-07	-1.720e-07
B (output stable)	4.360e-09	-3.899e-07	-1.609e-07	-1.735e-06
C (output stable)	3.357e-09	-2.062e-06	-1.654e-07	-3.846e-06
A to Z	2.900e-08	-1.020e-07	-4.530e-07	-2.850e-07
B to Z	4.100e-08	-4.900e-07	-9.040e-07	-1.370e-06
C to Z	1.410e-07	-3.800e-08	9.990e-07	-7.950e-07

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	0.816	0.9792
X13_P10	1.200	1.088	1.3056
X20_P10	1.200	1.632	1.9584
X27_P10	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P10	X13_P10	X20_P10	X27_P10
A	0.0009	0.0009	0.0018	0.0017
B	0.0010	0.0010	0.0019	0.0017
C	0.0008	0.0015	0.0021	0.0028

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	**X13_P10**	**X7_P10**	**X13_P10**
A to Z ↓	0.0501	0.0610	4.8666	2.5884
A to Z ↑	0.0296	0.0335	4.6752	2.3518
B to Z ↓	0.0486	0.0599	4.8677	2.5938
B to Z ↑	0.0281	0.0322	4.6779	2.3512
C to Z ↓	0.0139	0.0128	4.9201	2.6054
C to Z ↑	0.0178	0.0163	4.7667	2.4039
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0552	0.0610	1.7600	1.3344
A to Z ↑	0.0313	0.0373	1.5836	1.1899
B to Z ↓	0.0506	0.0576	1.7603	1.3360

B to Z ↑	0.0290	0.0356	1.5817	1.1886
C to Z ↓	0.0143	0.0138	1.7761	1.3430
C to Z ↑	0.0176	0.0170	1.6168	1.2147

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X7_P10	1.228e-06	1.060e-09
X13_P10	1.697e-06	1.298e-09
X20_P10	2.604e-06	1.775e-09
X27_P10	2.903e-06	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	5.865e-04	7.842e-04	1.347e-03	1.586e-03
B (output stable)	4.710e-04	6.715e-04	1.001e-03	1.277e-03
C (output stable)	5.062e-05	3.256e-04	3.372e-04	3.971e-04
A to Z	2.581e-03	4.198e-03	6.734e-03	8.302e-03
B to Z	2.301e-03	3.927e-03	5.814e-03	7.541e-03
C to Z	6.030e-04	1.006e-03	1.768e-03	2.275e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

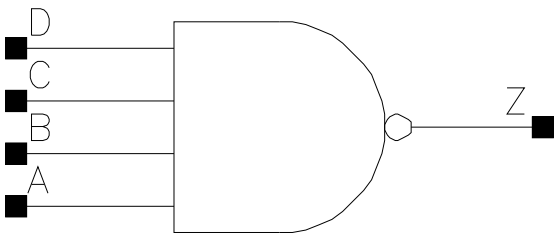
Pin Cycle (vdds)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	-1.340e-06	-1.323e-06	-6.696e-06	-6.679e-06
B (output stable)	1.318e-05	1.316e-05	4.066e-05	3.956e-05
C (output stable)	-8.572e-08	-1.590e-07	-1.164e-06	-1.256e-06
A to Z	-4.023e-07	-3.348e-07	-3.526e-06	-3.195e-06
B to Z	-1.776e-07	-2.855e-07	-5.830e-07	-7.230e-07
C to Z	2.117e-07	-3.661e-07	-3.250e-07	4.390e-07

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0006	0.0006	0.0008	0.0009
B	0.0007	0.0007	0.0008	0.0010
C	0.0006	0.0007	0.0008	0.0010
D	0.0007	0.0007	0.0008	0.0010

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0818	0.0794	2.7795	1.3885
A to Z ↑	0.0601	0.0643	4.7614	2.3719
B to Z ↓	0.0832	0.0821	2.7803	1.3897
B to Z ↑	0.0583	0.0638	4.7658	2.3694
C to Z ↓	0.0819	0.0778	2.7806	1.3883
C to Z ↑	0.0621	0.0673	4.7681	2.3687

D to Z ↓	0.0838	0.0790	2.7768	1.3895
D to Z ↑	0.0609	0.0650	4.7625	2.3678
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0823	0.0748	0.9587	0.7182
A to Z ↑	0.0616	0.0598	1.5964	1.1971
B to Z ↓	0.0840	0.0760	0.9590	0.7187
B to Z ↑	0.0602	0.0580	1.5962	1.1975
C to Z ↓	0.0749	0.0684	0.9597	0.7185
C to Z ↑	0.0625	0.0605	1.5938	1.1949
D to Z ↓	0.0763	0.0696	0.9583	0.7190
D to Z ↑	0.0604	0.0585	1.5945	1.1963

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.637e-06	1.417e-09
X17_P10	2.516e-06	1.655e-09
X25_P10	3.545e-06	2.013e-09
X33_P10	4.513e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	4.127e-04	5.188e-04	7.469e-04	8.805e-04
B (output stable)	3.817e-04	4.971e-04	7.042e-04	8.216e-04
C (output stable)	4.145e-04	5.074e-04	7.633e-04	8.683e-04
D (output stable)	3.826e-04	4.701e-04	6.845e-04	7.797e-04
A to Z	3.050e-03	4.582e-03	7.118e-03	8.600e-03
B to Z	2.952e-03	4.505e-03	6.977e-03	8.412e-03
C to Z	3.131e-03	4.512e-03	6.609e-03	7.960e-03
D to Z	3.045e-03	4.409e-03	6.456e-03	7.772e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

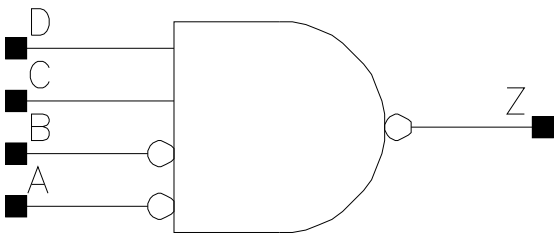
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	-4.982e-07	-7.351e-07	-3.669e-06	-3.943e-06
B (output stable)	-4.366e-07	-6.673e-07	-3.593e-06	-3.725e-06
C (output stable)	4.402e-06	8.795e-06	2.238e-05	2.787e-05
D (output stable)	3.990e-06	8.605e-06	1.361e-05	1.938e-05
A to Z	-4.164e-07	-4.741e-07	-3.555e-06	-3.838e-06
B to Z	-2.334e-07	-3.974e-07	-3.294e-06	-3.110e-06
C to Z	-2.449e-07	-2.935e-07	-4.730e-07	-5.590e-07
D to Z	-1.098e-07	-1.739e-07	-4.753e-07	-3.903e-07

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X12_P10	1.200	1.496	1.7952
X18_P10	1.200	2.040	2.4480
X24_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0010	0.0010	0.0018	0.0017
B	0.0010	0.0013	0.0019	0.0017
C	0.0008	0.0015	0.0022	0.0030
D	0.0007	0.0014	0.0021	0.0029

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X12_P10	X6_P10	X12_P10
A to Z ↓	0.0532	0.0714	7.5056	3.8480
A to Z ↑	0.0314	0.0378	4.6760	2.3549
B to Z ↓	0.0508	0.0689	7.5091	3.8495
B to Z ↑	0.0289	0.0361	4.6731	2.3528
C to Z ↓	0.0202	0.0208	7.5337	3.8527
C to Z ↑	0.0225	0.0221	4.9874	2.3885

D to Z ↓	0.0192	0.0174	7.5550	3.8637
D to Z ↑	0.0202	0.0185	5.0126	2.4029
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0607	0.0686	2.6341	1.9958
A to Z ↑	0.0332	0.0424	1.5841	1.1917
B to Z ↓	0.0563	0.0652	2.6308	1.9958
B to Z ↑	0.0310	0.0406	1.5825	1.1898
C to Z ↓	0.0206	0.0213	2.6375	1.9948
C to Z ↑	0.0218	0.0222	1.6131	1.2055
D to Z ↓	0.0182	0.0184	2.6463	2.0018
D to Z ↑	0.0188	0.0189	1.6411	1.2134

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P10	9.477e-07	1.179e-09
X12_P10	1.485e-06	1.655e-09
X18_P10	2.245e-06	2.132e-09
X24_P10	2.384e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	6.626e-04	1.129e-03	1.677e-03	2.045e-03
B (output stable)	5.201e-04	9.287e-04	1.266e-03	1.668e-03
C (output stable)	7.025e-05	1.968e-04	2.855e-04	3.924e-04
D (output stable)	1.358e-04	5.056e-04	6.074e-04	9.189e-04
A to Z	2.772e-03	5.290e-03	7.720e-03	1.021e-02
B to Z	2.490e-03	4.901e-03	6.868e-03	9.448e-03
C to Z	9.963e-04	2.012e-03	2.864e-03	4.050e-03
D to Z	7.912e-04	1.356e-03	2.088e-03	2.847e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

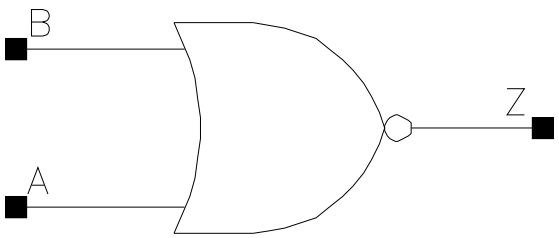
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	-1.239e-06	-4.912e-06	-6.313e-06	-6.739e-06
B (output stable)	1.193e-05	2.001e-05	3.489e-05	3.436e-05
C (output stable)	9.166e-09	-7.160e-07	-8.696e-07	-1.534e-06
D (output stable)	-5.723e-08	-2.487e-06	-2.514e-06	-5.132e-06
A to Z	-4.444e-07	-2.876e-06	-3.313e-06	-3.871e-06
B to Z	-8.360e-08	-3.400e-07	-5.580e-07	-6.580e-07
C to Z	3.820e-08	-4.490e-07	-8.100e-07	-8.980e-07
D to Z	1.812e-07	-1.200e-07	4.140e-07	2.850e-07

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.408	0.4896
X5_P10	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X10_P10	1.200	0.680	0.8160
X14_P10	1.200	0.680	0.8160
X17_P10	1.200	0.952	1.1424
X21_P10	1.200	0.952	1.1424
X24_P10	1.200	1.224	1.4688
X27_P10	1.200	1.224	1.4688
X34_P10	1.200	1.496	1.7952
X40_P10	1.200	1.360	1.6320
X41_P10	1.200	1.768	2.1216
X49_P10	1.200	1.496	1.7952
X53_P10	1.200	1.904	2.2848
X55_P10	1.200	2.312	2.7744
X57_P10	1.200	1.904	2.2848
X65_P10	1.200	2.040	2.4480
X84_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P10	X5_P10	X7_P10	X10_P10
A	0.0005	0.0006	0.0008	0.0013
B	0.0005	0.0006	0.0008	0.0012
	X14_P10	X17_P10	X21_P10	X24_P10

A	0.0016	0.0021	0.0024	0.0027
B	0.0014	0.0018	0.0022	0.0026
	X27_P10	X34_P10	X40_P10	X41_P10
A	0.0031	0.0039	0.0009	0.0047
B	0.0028	0.0035	0.0010	0.0043
	X49_P10	X53_P10	X55_P10	X57_P10
A	0.0009	0.0010	0.0063	0.0010
B	0.0010	0.0009	0.0057	0.0009
	X65_P10	X84_P10		
A	0.0010	0.0011		
B	0.0009	0.0009		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X5_P10**	**X3_P10**	**X5_P10**
A to Z ↓	0.0145	0.0134	5.2994	3.7977
A to Z ↑	0.0289	0.0266	20.9093	15.0046
B to Z ↓	0.0132	0.0118	5.4032	3.8233
B to Z ↑	0.0272	0.0243	20.9840	15.0460
	X7_P10	**X10_P10**	**X7_P10**	**X10_P10**
A to Z ↓	0.0129	0.0135	2.7621	1.8156
A to Z ↑	0.0251	0.0284	10.4900	7.0240
B to Z ↓	0.0112	0.0106	2.7980	1.8316
B to Z ↑	0.0226	0.0211	10.5238	7.0526
	X14_P10	**X17_P10**	**X14_P10**	**X17_P10**
A to Z ↓	0.0131	0.0134	1.3707	1.1068
A to Z ↑	0.0267	0.0269	5.1666	4.1881
B to Z ↓	0.0102	0.0110	1.3847	1.1169
B to Z ↑	0.0200	0.0215	5.1889	4.2025
	X21_P10	**X24_P10**	**X21_P10**	**X24_P10**
A to Z ↓	0.0132	0.0131	0.9385	0.8036
A to Z ↑	0.0261	0.0264	3.4685	3.0212
B to Z ↓	0.0109	0.0106	0.9473	0.8118
B to Z ↑	0.0209	0.0206	3.4803	3.0323
	X27_P10	**X34_P10**	**X27_P10**	**X34_P10**
A to Z ↓	0.0129	0.0134	0.7103	0.5740
A to Z ↑	0.0254	0.0260	2.6451	2.1090
B to Z ↓	0.0102	0.0108	0.7183	0.5795
B to Z ↑	0.0198	0.0208	2.6556	2.1165
	X40_P10	**X41_P10**	**X40_P10**	**X41_P10**
A to Z ↓	0.0482	0.0131	0.5828	0.4785
A to Z ↑	0.0740	0.0256	0.9801	1.7493
B to Z ↓	0.0465	0.0103	0.5832	0.4837
B to Z ↑	0.0728	0.0197	0.9810	1.7564
	X49_P10	**X53_P10**	**X49_P10**	**X53_P10**
A to Z ↓	0.0508	0.0519	0.4865	0.4462
A to Z ↑	0.0767	0.0873	0.8173	0.7567
B to Z ↓	0.0492	0.0502	0.4864	0.4460
B to Z ↑	0.0757	0.0852	0.8163	0.7567
	X55_P10	**X57_P10**	**X55_P10**	**X57_P10**
A to Z ↓	0.0132	0.0523	0.3617	0.4181
A to Z ↑	0.0256	0.0875	1.3163	0.7019

B to Z ↓	0.0104	0.0506	0.3662	0.4183
B to Z ↑	0.0197	0.0855	1.3218	0.7019
	X65_P10	**X84_P10**	**X65_P10**	**X84_P10**
A to Z ↓	0.0538	0.0562	0.3674	0.2920
A to Z ↑	0.0887	0.0894	0.6142	0.4866
B to Z ↓	0.0522	0.0546	0.3677	0.2922
B to Z ↑	0.0868	0.0878	0.6144	0.4865

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P10	3.150e-07	7.027e-10
X5_P10	4.327e-07	7.027e-10
X7_P10	5.838e-07	7.027e-10
X10_P10	8.277e-07	9.409e-10
X14_P10	1.066e-06	9.409e-10
X17_P10	1.318e-06	1.179e-09
X21_P10	1.515e-06	1.179e-09
X24_P10	1.799e-06	1.417e-09
X27_P10	1.965e-06	1.417e-09
X34_P10	2.417e-06	1.655e-09
X40_P10	3.326e-06	1.536e-09
X41_P10	2.868e-06	1.894e-09
X49_P10	3.643e-06	1.655e-09
X53_P10	4.614e-06	2.013e-09
X55_P10	3.771e-06	2.370e-09
X57_P10	4.776e-06	2.013e-09
X65_P10	5.093e-06	2.132e-09
X84_P10	5.718e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	2.197e-05	2.933e-05	4.100e-05	1.209e-04
B (output stable)	4.908e-06	6.203e-06	8.944e-06	5.534e-05
A to Z	5.350e-04	6.471e-04	8.485e-04	1.525e-03
B to Z	3.898e-04	4.463e-04	5.611e-04	7.727e-04
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	1.424e-04	1.722e-04	1.939e-04	2.369e-04
B (output stable)	6.303e-05	7.473e-05	7.155e-05	8.684e-05
A to Z	1.866e-03	2.353e-03	2.695e-03	3.183e-03
B to Z	9.529e-04	1.342e-03	1.522e-03	1.724e-03
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	2.475e-04	3.141e-04	4.143e-05	3.933e-04
B (output stable)	9.121e-05	9.906e-05	8.910e-06	1.496e-04
A to Z	3.391e-03	4.423e-03	8.393e-03	5.176e-03
B to Z	1.816e-03	2.517e-03	8.123e-03	2.721e-03
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	4.158e-05	4.237e-05	5.208e-04	4.237e-05
B (output stable)	8.845e-06	8.942e-06	1.856e-04	8.942e-06
A to Z	9.407e-03	1.161e-02	6.850e-03	1.194e-02
B to Z	9.138e-03	1.132e-02	3.608e-03	1.164e-02
	X65_P10	X84_P10		

A (output stable)	4.244e-05	4.354e-05		
B (output stable)	9.027e-06	9.815e-06		
A to Z	1.284e-02	1.503e-02		
B to Z	1.255e-02	1.468e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

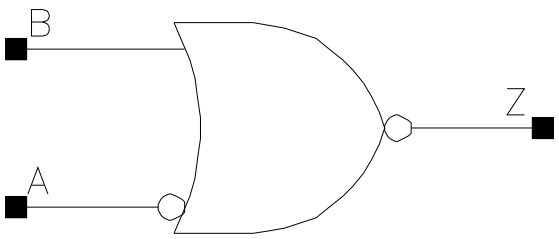
Pin Cycle (vdds)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	-1.149e-06	-1.407e-06	-1.824e-06	-8.327e-06
B (output stable)	1.102e-05	1.457e-05	1.958e-05	7.009e-05
A to Z	-8.970e-08	-3.491e-07	-5.780e-07	-3.832e-06
B to Z	1.150e-07	-2.106e-07	-3.949e-07	-1.888e-07
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	-9.447e-06	-7.256e-06	-7.495e-06	-1.350e-05
B (output stable)	8.638e-05	6.521e-05	6.764e-05	1.177e-04
A to Z	-2.693e-06	-3.062e-06	-3.577e-06	-4.386e-06
B to Z	-4.628e-07	-2.694e-07	-1.036e-06	-8.415e-07
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	-1.228e-05	-1.219e-05	-1.809e-06	-1.805e-05
B (output stable)	1.129e-04	1.137e-04	1.943e-05	1.642e-04
A to Z	-3.839e-06	-5.109e-06	-1.088e-06	-6.147e-06
B to Z	-3.935e-07	-7.490e-07	-7.610e-07	-5.150e-07
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	-1.812e-06	-1.817e-06	-2.261e-05	-1.817e-06
B (output stable)	1.935e-05	2.077e-05	2.051e-04	2.077e-05
A to Z	-6.770e-07	-1.205e-06	-8.615e-06	-1.423e-06
B to Z	-6.340e-07	-7.330e-07	-8.260e-07	-8.720e-07
	X65_P10	X84_P10		
A (output stable)	-1.816e-06	-1.882e-06		
B (output stable)	2.078e-05	2.127e-05		
A to Z	-1.878e-06	-8.800e-07		
B to Z	-1.527e-06	-8.460e-07		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X7_P10	1.200	0.680	0.8160
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X41_P10	1.200	2.312	2.7744
X55_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X7_P10	X13_P10
A	0.0008	0.0008	0.0008	0.0011
B	0.0005	0.0008	0.0008	0.0014
	X27_P10	X41_P10	X55_P10	
A	0.0020	0.0029	0.0038	
B	0.0029	0.0043	0.0057	

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0396	0.0432	5.2133	3.3399
A to Z ↑	0.0385	0.0376	20.7899	10.4578
B to Z ↓	0.0135	0.0128	5.3969	3.4920
B to Z ↑	0.0276	0.0226	20.9553	10.5391

	X7_P10	X13_P10	X7_P10	X13_P10
A to Z ↓	0.0436	0.0386	2.6269	1.4296
A to Z ↑	0.0409	0.0378	10.2944	5.4140
B to Z ↓	0.0116	0.0106	2.6613	1.4426
B to Z ↑	0.0238	0.0215	10.3497	5.4512
	X27_P10	**X41_P10**	**X27_P10**	**X41_P10**
A to Z ↓	0.0375	0.0378	0.6911	0.4681
A to Z ↑	0.0364	0.0362	2.6072	1.7457
B to Z ↓	0.0105	0.0103	0.7168	0.4847
B to Z ↑	0.0206	0.0200	2.6251	1.7581
	X55_P10		**X55_P10**	
A to Z ↓	0.0374		0.3540	
A to Z ↑	0.0359		1.3152	
B to Z ↓	0.0104		0.3672	
B to Z ↑	0.0200		1.3242	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P10	5.809e-07	8.218e-10
X6_P10	7.851e-07	8.218e-10
X7_P10	9.562e-07	9.409e-10
X13_P10	1.666e-06	1.179e-09
X27_P10	3.057e-06	1.775e-09
X41_P10	4.397e-06	2.370e-09
X55_P10	5.735e-06	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	8.076e-04	1.019e-03	1.088e-03	1.722e-03
B (output stable)	1.577e-05	3.369e-05	4.347e-05	9.391e-05
A to Z	1.406e-03	1.937e-03	2.262e-03	3.766e-03
B to Z	4.012e-04	5.589e-04	6.655e-04	1.051e-03
	X27_P10	X41_P10	X55_P10	
A (output stable)	3.373e-03	5.082e-03	6.626e-03	
B (output stable)	1.987e-04	2.960e-04	3.982e-04	
A to Z	7.462e-03	1.087e-02	1.433e-02	
B to Z	2.023e-03	2.824e-03	3.764e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

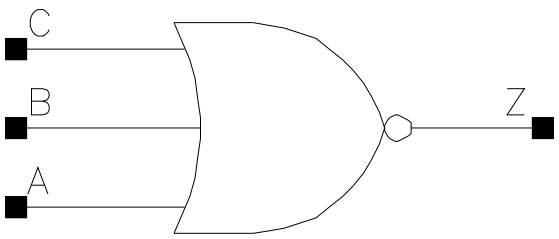
Pin Cycle (vdds)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	-1.146e-06	-1.646e-06	-4.709e-06	-7.778e-06
B (output stable)	8.856e-06	1.862e-05	2.718e-05	4.510e-05
A to Z	-5.910e-08	-3.078e-07	-1.459e-06	-2.264e-06
B to Z	-2.850e-08	1.364e-07	-1.108e-07	-5.015e-07
	X27_P10	X41_P10	X55_P10	
A (output stable)	-1.362e-05	-1.598e-05	-2.131e-05	
B (output stable)	7.625e-05	1.016e-04	1.373e-04	
A to Z	-4.315e-06	-5.355e-06	-6.774e-06	
B to Z	-8.599e-07	-6.044e-07	-8.590e-07	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X9_P10	1.200	0.952	1.1424
X13_P10	1.200	0.952	1.1424
X16_P10	1.200	1.360	1.6320
X19_P10	1.200	1.496	1.7952
X22_P10	1.200	1.768	2.1216
X25_P10	1.200	1.904	2.2848
X37_P10	1.200	2.584	3.1008
X49_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P10	X6_P10	X9_P10	X13_P10
A	0.0006	0.0008	0.0012	0.0015
B	0.0006	0.0008	0.0014	0.0017
C	0.0006	0.0008	0.0011	0.0014
	X16_P10	X19_P10	X22_P10	X25_P10
A	0.0020	0.0023	0.0028	0.0031
B	0.0021	0.0027	0.0029	0.0037
C	0.0018	0.0021	0.0025	0.0028
	X37_P10	X49_P10		
A	0.0046	0.0063		
B	0.0048	0.0064		

C	0.0041	0.0056		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0159	0.0151	3.8555	2.8087
A to Z ↑	0.0414	0.0379	22.9841	16.0802
B to Z ↓	0.0152	0.0143	3.8569	2.8090
B to Z ↑	0.0386	0.0350	23.0290	16.0913
C to Z ↓	0.0139	0.0127	3.8801	2.8376
C to Z ↑	0.0338	0.0297	23.0766	16.1472
	X9_P10	**X13_P10**	**X9_P10**	**X13_P10**
A to Z ↓	0.0155	0.0150	1.8768	1.4310
A to Z ↑	0.0415	0.0388	10.7298	7.9253
B to Z ↓	0.0149	0.0142	1.8275	1.3733
B to Z ↑	0.0407	0.0371	10.7561	7.9414
C to Z ↓	0.0120	0.0115	1.8365	1.3922
C to Z ↑	0.0274	0.0254	10.7702	7.9489
	X16_P10	**X19_P10**	**X16_P10**	**X19_P10**
A to Z ↓	0.0154	0.0150	1.1184	0.9360
A to Z ↑	0.0399	0.0392	6.4237	5.3087
B to Z ↓	0.0150	0.0146	1.1201	0.9164
B to Z ↑	0.0382	0.0384	6.4420	5.2994
C to Z ↓	0.0124	0.0120	1.1217	0.9528
C to Z ↑	0.0286	0.0269	6.4492	5.3164
	X22_P10	**X25_P10**	**X22_P10**	**X25_P10**
A to Z ↓	0.0151	0.0149	0.8210	0.7143
A to Z ↑	0.0390	0.0390	4.5830	3.9861
B to Z ↓	0.0146	0.0144	0.8062	0.6882
B to Z ↑	0.0375	0.0382	4.5866	3.9873
C to Z ↓	0.0116	0.0115	0.8117	0.7151
C to Z ↑	0.0260	0.0252	4.5947	3.9931
	X37_P10	**X49_P10**	**X37_P10**	**X49_P10**
A to Z ↓	0.0150	0.0152	0.4924	0.3731
A to Z ↑	0.0379	0.0380	2.6684	2.0016
B to Z ↓	0.0143	0.0145	0.4866	0.3691
B to Z ↑	0.0358	0.0359	2.6690	2.0035
C to Z ↓	0.0117	0.0120	0.4922	0.3731
C to Z ↑	0.0252	0.0259	2.6712	2.0093

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.194e-07	8.218e-10
X6_P10	4.349e-07	8.218e-10
X9_P10	6.270e-07	1.179e-09
X13_P10	8.150e-07	1.179e-09
X16_P10	1.009e-06	1.536e-09
X19_P10	1.248e-06	1.656e-09
X22_P10	1.393e-06	1.894e-09
X25_P10	1.620e-06	2.013e-09
X37_P10	2.283e-06	2.608e-09

X49_P10	3.018e-06	3.323e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	8.969e-05	1.208e-04	2.815e-04	3.450e-04
B (output stable)	-5.666e-06	-9.994e-06	8.813e-05	7.771e-05
C (output stable)	4.572e-06	6.500e-06	2.796e-05	3.201e-05
A to Z	9.979e-04	1.267e-03	2.133e-03	2.632e-03
B to Z	8.050e-04	9.984e-04	1.786e-03	2.128e-03
C to Z	6.036e-04	7.049e-04	9.862e-04	1.170e-03
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	3.908e-04	4.920e-04	5.867e-04	6.925e-04
B (output stable)	5.889e-05	8.986e-05	1.227e-04	1.539e-04
C (output stable)	3.462e-05	4.227e-05	5.149e-05	5.799e-05
A to Z	3.377e-03	4.000e-03	4.603e-03	5.282e-03
B to Z	2.760e-03	3.316e-03	3.743e-03	4.364e-03
C to Z	1.730e-03	1.915e-03	2.105e-03	2.314e-03
	X37_P10	X49_P10		
A (output stable)	9.558e-04	1.245e-03		
B (output stable)	1.447e-04	1.540e-04		
C (output stable)	8.720e-05	1.112e-04		
A to Z	7.593e-03	1.015e-02		
B to Z	6.053e-03	8.074e-03		
C to Z	3.379e-03	4.644e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

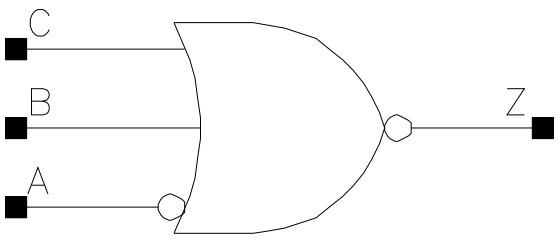
Pin Cycle (vdds)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	-1.309e-05	-1.706e-05	-4.496e-05	-5.417e-05
B (output stable)	1.136e-05	1.625e-05	1.389e-05	2.173e-05
C (output stable)	1.507e-05	2.232e-05	5.418e-05	7.023e-05
A to Z	-1.454e-06	-1.658e-06	-6.344e-06	-7.378e-06
B to Z	-2.602e-07	-4.311e-07	-3.213e-06	-3.410e-06
C to Z	-1.415e-07	-3.639e-07	-5.926e-07	-5.378e-07
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	-5.132e-05	-6.790e-05	-8.375e-05	-1.015e-04
B (output stable)	3.611e-05	5.002e-05	4.643e-05	6.455e-05
C (output stable)	5.712e-05	7.937e-05	9.908e-05	1.205e-04
A to Z	-6.804e-06	-8.366e-06	-1.038e-05	-1.324e-05
B to Z	-2.468e-06	-3.785e-06	-3.760e-06	-5.951e-06
C to Z	-1.040e-06	-1.397e-06	-8.270e-07	-9.947e-07
	X37_P10	X49_P10		
A (output stable)	-1.331e-04	-1.634e-04		
B (output stable)	8.552e-05	1.189e-04		
C (output stable)	1.588e-04	1.877e-04		
A to Z	-1.681e-05	-1.999e-05		
B to Z	-5.507e-06	-9.926e-06		
C to Z	-2.312e-06	-2.963e-06		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.680	0.8160
X13_P10	1.200	1.224	1.4688
X19_P10	1.200	1.496	1.7952
X25_P10	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0008	0.0010	0.0011	0.0020
B	0.0008	0.0016	0.0023	0.0032
C	0.0008	0.0014	0.0021	0.0028

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X13_P10**	**X6_P10**	**X13_P10**
A to Z ↓	0.0435	0.0404	2.7654	1.5179
A to Z ↑	0.0511	0.0496	16.2735	7.9364
B to Z ↓	0.0146	0.0142	2.8273	1.3803
B to Z ↑	0.0355	0.0371	16.2789	7.9408
C to Z ↓	0.0129	0.0113	2.8419	1.3933
C to Z ↑	0.0303	0.0251	16.3345	7.9491
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0462	0.0401	0.9402	0.7114

A to Z ↑	0.0529	0.0487	5.3208	3.9890
B to Z ↓	0.0147	0.0143	0.9591	0.7147
B to Z ↑	0.0360	0.0359	5.3275	3.9906
C to Z ↓	0.0120	0.0115	0.9539	0.7188
C to Z ↑	0.0270	0.0255	5.3376	4.0030

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P10	7.111e-07	9.409e-10
X13_P10	1.447e-06	1.417e-09
X19_P10	1.694e-06	1.655e-09
X25_P10	2.699e-06	2.251e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	1.127e-03	2.069e-03	2.740e-03	4.001e-03
B (output stable)	7.232e-06	5.594e-05	5.788e-05	9.394e-05
C (output stable)	1.284e-05	5.447e-05	5.729e-05	8.850e-05
A to Z	2.403e-03	4.728e-03	6.521e-03	9.040e-03
B to Z	1.011e-03	2.137e-03	3.079e-03	4.080e-03
C to Z	7.219e-04	1.150e-03	1.902e-03	2.319e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

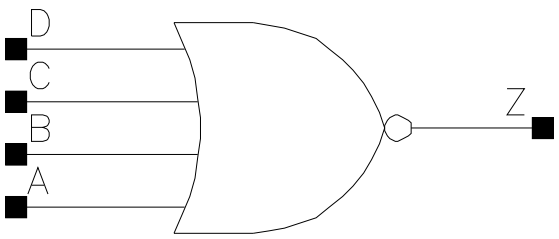
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	-1.723e-05	-4.917e-05	-5.953e-05	-8.944e-05
B (output stable)	1.556e-05	3.361e-05	5.322e-05	7.128e-05
C (output stable)	2.384e-05	6.009e-05	6.885e-05	1.037e-04
A to Z	-1.232e-06	-6.177e-06	-6.550e-06	-9.951e-06
B to Z	-2.400e-08	-3.160e-06	-2.974e-06	-4.824e-06
C to Z	-2.250e-08	-4.878e-07	-1.345e-06	-9.177e-07

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	1.904	2.2848
X32_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X32_P10
A	0.0006	0.0007	0.0007	0.0009
B	0.0007	0.0006	0.0008	0.0011
C	0.0006	0.0006	0.0008	0.0009
D	0.0006	0.0006	0.0008	0.0009

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0523	0.0507	2.7186	1.3364
A to Z ↑	0.0843	0.0893	4.8718	2.3941
B to Z ↓	0.0506	0.0495	2.7170	1.3365
B to Z ↑	0.0825	0.0878	4.8697	2.3933
C to Z ↓	0.0516	0.0507	2.7146	1.3336
C to Z ↑	0.0854	0.0918	4.8779	2.3961

D to Z ↓	0.0511	0.0502	2.7135	1.3332
D to Z ↑	0.0845	0.0911	4.8756	2.3941
	X25_P10	**X32_P10**	**X25_P10**	**X32_P10**
A to Z ↓	0.0517	0.0541	0.9287	0.7329
A to Z ↑	0.0870	0.0841	1.6335	1.2424
B to Z ↓	0.0504	0.0527	0.9288	0.7337
B to Z ↑	0.0859	0.0828	1.6333	1.2408
C to Z ↓	0.0496	0.0526	0.9251	0.7319
C to Z ↑	0.0858	0.0838	1.6324	1.2403
D to Z ↓	0.0482	0.0503	0.9239	0.7305
D to Z ↑	0.0844	0.0820	1.6303	1.2420

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.077e-06	1.417e-09
X17_P10	1.539e-06	1.536e-09
X25_P10	2.331e-06	2.013e-09
X32_P10	2.789e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	4.243e-04	5.207e-04	7.211e-04	9.260e-04
B (output stable)	3.513e-04	4.505e-04	6.303e-04	7.963e-04
C (output stable)	4.006e-04	4.823e-04	7.598e-04	9.725e-04
D (output stable)	3.292e-04	4.150e-04	6.570e-04	8.345e-04
A to Z	2.927e-03	4.365e-03	6.680e-03	8.381e-03
B to Z	2.774e-03	4.229e-03	6.471e-03	8.138e-03
C to Z	2.979e-03	4.369e-03	6.261e-03	7.860e-03
D to Z	2.823e-03	4.231e-03	6.066e-03	7.591e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

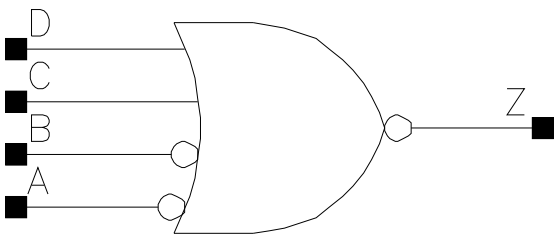
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	-8.001e-07	-7.640e-07	-9.983e-07	-1.163e-06
B (output stable)	5.381e-06	5.135e-06	8.214e-06	1.156e-05
C (output stable)	-1.053e-06	-1.103e-06	-1.162e-06	-1.325e-06
D (output stable)	5.951e-06	5.716e-06	8.631e-06	1.146e-05
A to Z	-4.068e-07	-5.412e-07	-4.611e-07	-8.999e-07
B to Z	-1.092e-07	-4.275e-07	-4.269e-07	-8.335e-07
C to Z	-3.442e-07	-4.777e-07	-7.225e-07	-6.034e-07
D to Z	-8.440e-08	-2.519e-07	-2.213e-07	-8.338e-07

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X13_P10	1.200	1.496	1.7952
X19_P10	1.200	2.040	2.4480
X25_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0010	0.0010	0.0019	0.0019
B	0.0010	0.0015	0.0019	0.0020
C	0.0008	0.0016	0.0023	0.0030
D	0.0007	0.0014	0.0021	0.0028

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X13_P10	X6_P10	X13_P10
A to Z ↓	0.0370	0.0457	2.7062	1.3461
A to Z ↑	0.0513	0.0623	15.6701	8.0102
B to Z ↓	0.0347	0.0442	2.7037	1.3441
B to Z ↑	0.0516	0.0633	15.6671	8.0039
C to Z ↓	0.0151	0.0141	2.8604	1.3752
C to Z ↑	0.0359	0.0368	15.7093	8.0120

D to Z ↓	0.0130	0.0115	2.8509	1.3883
D to Z ↑	0.0299	0.0257	15.7339	8.0347
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0402	0.0440	0.9248	0.6987
A to Z ↑	0.0564	0.0608	5.3279	4.0075
B to Z ↓	0.0371	0.0416	0.9232	0.6978
B to Z ↑	0.0558	0.0611	5.3266	4.0076
C to Z ↓	0.0148	0.0144	0.9602	0.7205
C to Z ↑	0.0359	0.0356	5.3323	4.0120
D to Z ↓	0.0120	0.0115	0.9547	0.7186
D to Z ↑	0.0270	0.0251	5.3403	4.0225

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P10	8.337e-07	1.179e-09
X13_P10	1.180e-06	1.655e-09
X19_P10	1.878e-06	2.132e-09
X25_P10	2.106e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	6.664e-04	1.224e-03	1.797e-03	2.232e-03
B (output stable)	6.004e-04	1.173e-03	1.661e-03	2.125e-03
C (output stable)	5.193e-06	4.345e-05	5.900e-05	8.899e-05
D (output stable)	2.049e-05	9.330e-05	1.091e-04	1.869e-04
A to Z	2.846e-03	5.415e-03	8.058e-03	1.037e-02
B to Z	2.652e-03	5.125e-03	7.430e-03	9.821e-03
C to Z	1.055e-03	2.101e-03	3.067e-03	4.009e-03
D to Z	7.475e-04	1.170e-03	1.901e-03	2.252e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

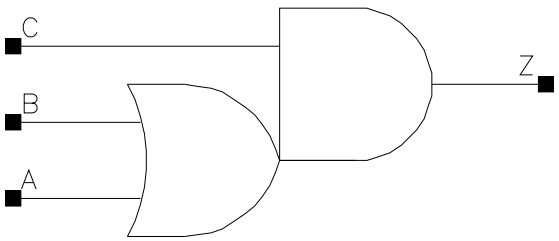
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	-8.229e-06	-2.831e-05	-3.325e-05	-4.888e-05
B (output stable)	-8.093e-06	-2.782e-05	-3.249e-05	-4.621e-05
C (output stable)	1.723e-05	2.915e-05	4.697e-05	5.984e-05
D (output stable)	3.487e-05	8.989e-05	1.024e-04	1.536e-04
A to Z	-1.587e-06	-7.234e-06	-7.445e-06	-1.304e-05
B to Z	-1.258e-06	-7.391e-06	-7.412e-06	-1.239e-05
C to Z	-2.300e-07	-3.013e-06	-2.038e-06	-4.959e-06
D to Z	-3.603e-07	-5.423e-07	-1.398e-06	-9.910e-07

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0009	0.0009	0.0017
B	0.0010	0.0010	0.0019
C	0.0010	0.0010	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0455	0.0526	2.8051	1.3996
A to Z ↑	0.0346	0.0381	4.8889	2.3990
B to Z ↓	0.0437	0.0513	2.8064	1.3995
B to Z ↑	0.0318	0.0357	4.8825	2.3963
C to Z ↓	0.0370	0.0405	2.7705	1.3709
C to Z ↑	0.0336	0.0366	4.8797	2.3956
	X33_P10		**X33_P10**	
A to Z ↓	0.0546		0.7116	
A to Z ↑	0.0406		1.2057	

B to Z ↓	0.0533		0.7114	
B to Z ↑	0.0376		1.2016	
C to Z ↓	0.0416		0.6943	
C to Z ↑	0.0380		1.2023	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.095e-06	9.409e-10
X17_P10	1.514e-06	1.060e-09
X33_P10	3.036e-06	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	9.568e-05	9.650e-05	1.953e-04
B (output stable)	8.590e-05	8.644e-05	1.717e-04
C (output stable)	4.983e-05	5.167e-05	9.850e-05
A to Z	2.164e-03	3.069e-03	6.407e-03
B to Z	1.884e-03	2.792e-03	5.866e-03
C to Z	2.378e-03	3.262e-03	6.759e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

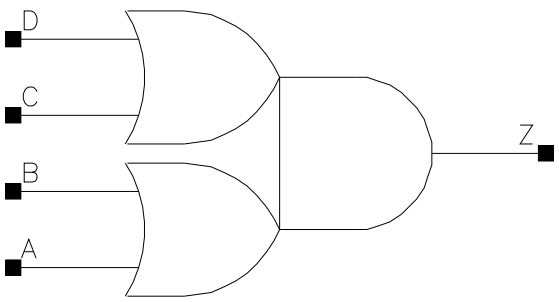
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-1.391e-06	-1.487e-06	-2.991e-06
B (output stable)	5.588e-06	5.689e-06	1.191e-05
C (output stable)	5.747e-08	7.351e-08	7.210e-08
A to Z	-2.172e-07	-4.012e-07	-1.223e-06
B to Z	-1.822e-07	-2.624e-07	-3.162e-07
C to Z	-4.972e-07	-5.282e-07	-1.231e-06

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0009	0.0018
B	0.0006	0.0009	0.0017
C	0.0006	0.0009	0.0018
D	0.0006	0.0009	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0781	0.0647	2.7527	1.3921
A to Z ↑	0.0493	0.0418	4.7897	2.3940
B to Z ↓	0.0774	0.0635	2.7553	1.3925
B to Z ↑	0.0477	0.0399	4.7847	2.3894

C to Z ↓	0.0685	0.0574	2.7307	1.3844
C to Z ↑	0.0471	0.0410	4.7891	2.3944
D to Z ↓	0.0662	0.0554	2.7324	1.3856
D to Z ↑	0.0445	0.0381	4.7838	2.3907
	X33_P10		**X33_P10**	
A to Z ↓	0.0649		0.7192	
A to Z ↑	0.0414		1.2026	
B to Z ↓	0.0610		0.7195	
B to Z ↑	0.0386		1.2001	
C to Z ↓	0.0566		0.7142	
C to Z ↑	0.0397		1.2017	
D to Z ↓	0.0522		0.7153	
D to Z ↑	0.0365		1.1998	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.094e-06	1.179e-09
X17_P10	2.063e-06	1.298e-09
X33_P10	3.820e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.203e-05	3.755e-05	1.157e-04
B (output stable)	1.049e-05	1.666e-05	5.885e-05
C (output stable)	7.431e-05	9.786e-05	2.734e-04
D (output stable)	6.159e-05	7.568e-05	1.977e-04
A to Z	2.517e-03	3.999e-03	7.889e-03
B to Z	2.384e-03	3.722e-03	7.075e-03
C to Z	2.176e-03	3.512e-03	6.845e-03
D to Z	2.024e-03	3.219e-03	6.007e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

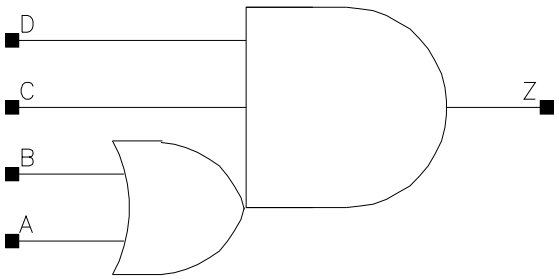
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-8.082e-07	-1.302e-06	-6.790e-06
B (output stable)	5.615e-06	1.169e-05	3.370e-05
C (output stable)	-1.776e-06	-1.518e-06	-1.506e-05
D (output stable)	5.636e-06	1.223e-05	3.742e-05
A to Z	-4.633e-07	-4.378e-07	-2.025e-06
B to Z	-2.536e-07	-1.934e-07	-9.274e-07
C to Z	-5.602e-07	-6.162e-07	-2.419e-06
D to Z	-2.167e-07	-3.189e-07	-1.376e-06

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	1.088	1.3056
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0006	0.0010	0.0015	0.0018
B	0.0006	0.0009	0.0015	0.0018
C	0.0007	0.0010	0.0016	0.0018
D	0.0006	0.0010	0.0015	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0664	0.0604	2.8951	1.4071
A to Z ↑	0.0582	0.0517	4.9730	2.4035
B to Z ↓	0.0654	0.0569	2.8935	1.4056
B to Z ↑	0.0552	0.0468	4.9686	2.4005
C to Z ↓	0.0497	0.0447	2.8019	1.3739

C to Z ↑	0.0572	0.0497	4.9618	2.3973
D to Z ↓	0.0484	0.0433	2.8024	1.3716
D to Z ↑	0.0579	0.0505	4.9591	2.3975
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0638	0.0608	0.9537	0.7165
A to Z ↑	0.0532	0.0532	1.6290	1.2200
B to Z ↓	0.0602	0.0575	0.9539	0.7160
B to Z ↑	0.0492	0.0490	1.6254	1.2173
C to Z ↓	0.0476	0.0453	0.9295	0.6983
C to Z ↑	0.0520	0.0511	1.6238	1.2175
D to Z ↓	0.0453	0.0435	0.9277	0.6969
D to Z ↑	0.0512	0.0509	1.6246	1.2174

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	6.243e-07	1.060e-09
X17_P10	1.231e-06	1.298e-09
X25_P10	1.988e-06	2.013e-09
X33_P10	2.465e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	7.305e-05	1.428e-04	2.525e-04	2.822e-04
B (output stable)	7.486e-05	1.427e-04	2.455e-04	2.718e-04
C (output stable)	1.157e-05	2.370e-05	6.014e-05	6.837e-05
D (output stable)	3.388e-05	7.216e-05	2.048e-04	2.240e-04
A to Z	2.080e-03	3.606e-03	5.913e-03	7.245e-03
B to Z	1.947e-03	3.209e-03	5.312e-03	6.478e-03
C to Z	2.286e-03	3.880e-03	6.518e-03	7.834e-03
D to Z	2.187e-03	3.694e-03	6.032e-03	7.324e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

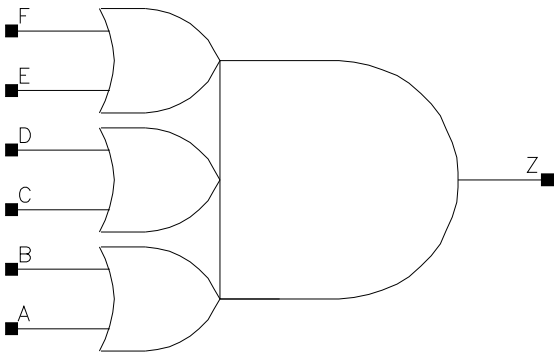
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	-1.143e-06	-2.942e-06	-4.136e-06	-3.592e-06
B (output stable)	6.544e-07	4.817e-06	5.848e-06	8.721e-06
C (output stable)	1.116e-07	7.225e-08	9.200e-08	-1.734e-08
D (output stable)	-9.528e-09	-7.352e-08	-1.006e-07	-7.304e-08
A to Z	-4.219e-07	-2.011e-06	-3.792e-06	-3.596e-06
B to Z	-5.344e-08	-2.251e-07	-3.394e-07	-3.465e-07
C to Z	-1.475e-07	-1.597e-08	6.825e-07	3.095e-07
D to Z	-2.755e-07	-1.634e-07	2.973e-07	-2.333e-07

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0009	0.0016
B	0.0006	0.0009	0.0017
C	0.0006	0.0009	0.0016
D	0.0006	0.0009	0.0017
E	0.0006	0.0009	0.0016
F	0.0006	0.0009	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0891	0.0737	2.9748	1.4404
A to Z ↑	0.0652	0.0567	4.9385	2.4174
B to Z ↓	0.0876	0.0728	2.9752	1.4401
B to Z ↑	0.0629	0.0545	4.9365	2.4175
C to Z ↓	0.0818	0.0693	2.9525	1.4356
C to Z ↑	0.0645	0.0555	4.9377	2.4188
D to Z ↓	0.0810	0.0681	2.9535	1.4359
D to Z ↑	0.0619	0.0529	4.9348	2.4163
E to Z ↓	0.0707	0.0609	2.9279	1.4259
E to Z ↑	0.0586	0.0516	4.9369	2.4171
F to Z ↓	0.0702	0.0593	2.9276	1.4272
F to Z ↑	0.0562	0.0486	4.9295	2.4141
	X33_P10		X33_P10	
A to Z ↓	0.0740		0.7364	
A to Z ↑	0.0580		1.2201	
B to Z ↓	0.0734		0.7362	
B to Z ↑	0.0547		1.2177	
C to Z ↓	0.0683		0.7315	
C to Z ↑	0.0566		1.2204	
D to Z ↓	0.0674		0.7317	
D to Z ↑	0.0535		1.2177	
E to Z ↓	0.0602		0.7265	
E to Z ↑	0.0527		1.2190	
F to Z ↓	0.0591		0.7268	
F to Z ↑	0.0494		1.2164	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.019e-06	1.417e-09
X17_P10	1.900e-06	1.536e-09
X33_P10	3.601e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.730e-05	3.081e-05	5.820e-05
B (output stable)	9.532e-06	1.982e-05	3.269e-05
C (output stable)	4.580e-05	7.128e-05	1.479e-04
D (output stable)	3.603e-05	5.652e-05	1.203e-04
E (output stable)	1.187e-04	1.741e-04	3.353e-04
F (output stable)	1.090e-04	1.576e-04	3.087e-04
A to Z	2.892e-03	4.681e-03	9.097e-03
B to Z	2.748e-03	4.419e-03	8.616e-03
C to Z	2.628e-03	4.296e-03	8.303e-03
D to Z	2.496e-03	4.025e-03	7.795e-03
E to Z	2.271e-03	3.769e-03	7.294e-03
F to Z	2.147e-03	3.493e-03	6.785e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

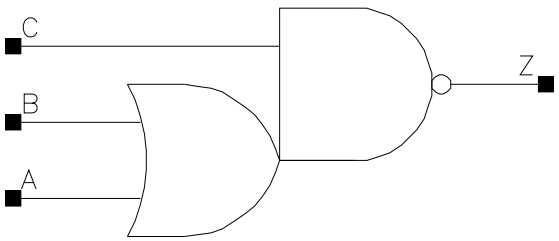
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-6.232e-07	-1.018e-06	-1.994e-06
B (output stable)	4.007e-06	8.081e-06	1.534e-05
C (output stable)	-9.789e-07	-1.158e-06	-2.913e-06
D (output stable)	3.827e-06	8.038e-06	1.468e-05
E (output stable)	-1.476e-06	-1.155e-06	-3.668e-06
F (output stable)	3.157e-06	7.898e-06	1.354e-05
A to Z	-7.187e-07	-7.042e-07	-1.460e-06
B to Z	-4.512e-07	-3.946e-07	-1.126e-06
C to Z	-9.393e-07	-9.769e-07	-2.086e-06
D to Z	-4.018e-07	-3.687e-07	-1.291e-06
E to Z	-7.716e-07	-8.694e-07	-1.708e-06
F to Z	-3.966e-07	-5.481e-07	-1.182e-06

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X34_P10	1.200	2.720	3.2640
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X34_P10	X46_P10
A	0.0007	0.0022	0.0045	0.0059
B	0.0007	0.0020	0.0040	0.0054
C	0.0008	0.0023	0.0047	0.0061

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0180	0.0184	5.4492	1.7914
A to Z ↑	0.0265	0.0278	10.4760	3.5088
B to Z ↓	0.0151	0.0153	5.3767	1.8118
B to Z ↑	0.0240	0.0235	10.5138	3.5238
C to Z ↓	0.0179	0.0179	4.9569	1.6468
C to Z ↑	0.0230	0.0226	4.8830	1.6127
	X34_P10	**X46_P10**	**X34_P10**	**X46_P10**
A to Z ↓	0.0195	0.0194	0.9115	0.6939

A to Z ↑	0.0293	0.0288	1.7525	1.3364
B to Z ↓	0.0159	0.0159	0.9211	0.7032
B to Z ↑	0.0243	0.0243	1.7589	1.3414
C to Z ↓	0.0186	0.0183	0.8389	0.6395
C to Z ↑	0.0232	0.0230	0.8059	0.6139

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P10	6.941e-07	8.218e-10
X17_P10	1.882e-06	1.536e-09
X34_P10	3.743e-06	2.727e-09
X46_P10	4.886e-06	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	8.539e-05	2.966e-04	6.260e-04	7.416e-04
B (output stable)	7.676e-05	2.531e-04	5.323e-04	6.283e-04
C (output stable)	4.630e-05	1.582e-04	3.261e-04	4.080e-04
A to Z	9.477e-04	3.025e-03	6.554e-03	8.392e-03
B to Z	6.618e-04	1.936e-03	4.182e-03	5.425e-03
C to Z	1.138e-03	3.445e-03	7.309e-03	9.332e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

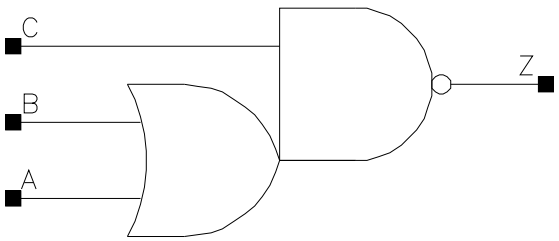
Pin Cycle (vdds)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	-9.391e-07	-5.021e-06	-1.358e-05	-1.339e-05
B (output stable)	6.107e-06	1.345e-05	2.858e-05	4.100e-05
C (output stable)	1.257e-08	-3.350e-08	-6.760e-08	-1.699e-07
A to Z	-2.411e-07	-2.808e-06	-6.519e-06	-6.620e-06
B to Z	-5.180e-08	-4.040e-07	-1.308e-06	-1.704e-06
C to Z	-2.280e-08	-3.867e-07	-1.083e-06	-2.279e-06

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.544	0.6528
X11_P10	1.200	0.952	1.1424
X17_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X17_P10	X23_P10
A	0.0008	0.0015	0.0024	0.0033
B	0.0007	0.0016	0.0022	0.0029
C	0.0007	0.0015	0.0021	0.0029
	X46_P10			
A	0.0065			
B	0.0058			
C	0.0058			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0194	0.0198	5.5732	2.6058
A to Z ↑	0.0325	0.0327	11.0205	5.1756
B to Z ↓	0.0171	0.0174	5.5097	2.5464

B to Z ↑	0.0303	0.0306	11.0549	5.1916
C to Z ↓	0.0151	0.0151	5.1570	2.4012
C to Z ↑	0.0182	0.0180	5.2079	2.4406
	X17_P10	**X23_P10**	**X17_P10**	**X23_P10**
A to Z ↓	0.0188	0.0200	1.7984	1.3300
A to Z ↑	0.0308	0.0341	3.4368	2.6067
B to Z ↓	0.0164	0.0172	1.7930	1.3273
B to Z ↑	0.0283	0.0297	3.4466	2.6159
C to Z ↓	0.0144	0.0149	1.6735	1.2353
C to Z ↑	0.0169	0.0175	1.6233	1.2320
	X46_P10		**X46_P10**	
A to Z ↓	0.0198		0.6910	
A to Z ↑	0.0334		1.3129	
B to Z ↓	0.0169		0.6844	
B to Z ↑	0.0291		1.3174	
C to Z ↓	0.0149		0.6399	
C to Z ↑	0.0171		0.6214	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P10	6.897e-07	8.218e-10
X11_P10	1.343e-06	1.179e-09
X17_P10	1.939e-06	1.536e-09
X23_P10	2.669e-06	2.013e-09
X46_P10	5.007e-06	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	2.489e-05	5.386e-05	7.999e-05	1.591e-04
B (output stable)	1.266e-05	3.075e-05	4.250e-05	8.109e-05
C (output stable)	2.095e-04	4.968e-04	5.828e-04	9.291e-04
A to Z	1.243e-03	2.689e-03	3.640e-03	5.641e-03
B to Z	9.513e-04	2.088e-03	2.687e-03	3.983e-03
C to Z	6.588e-04	1.434e-03	1.903e-03	2.841e-03
	X46_P10			
A (output stable)	3.014e-04			
B (output stable)	1.545e-04			
C (output stable)	1.732e-03			
A to Z	1.085e-02			
B to Z	7.572e-03			
C to Z	5.433e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	-8.779e-07	-1.991e-06	-3.022e-06	-7.936e-06
B (output stable)	5.826e-06	1.282e-05	1.916e-05	2.067e-05
C (output stable)	-1.986e-08	-1.978e-06	-2.264e-07	-4.203e-06
A to Z	-5.536e-07	-1.779e-06	-2.164e-06	-6.941e-06
B to Z	-3.419e-07	-1.746e-06	-1.666e-06	-3.316e-06
C to Z	6.917e-08	8.667e-09	-1.337e-06	-7.363e-07

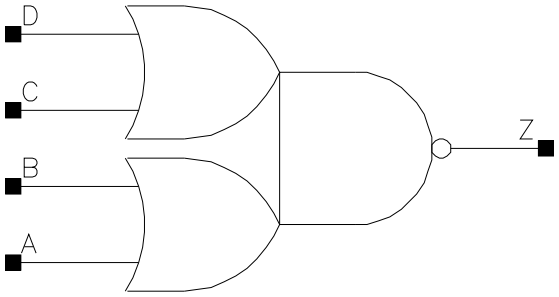
	X46_P10			
A (output stable)	-1.360e-05			
B (output stable)	3.888e-05			
C (output stable)	-7.935e-06			
A to Z	-1.199e-05			
B to Z	-6.118e-06			
C to Z	-1.158e-06			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0008	0.0016	0.0023	0.0032
B	0.0008	0.0014	0.0021	0.0029
C	0.0007	0.0015	0.0022	0.0031
D	0.0007	0.0014	0.0020	0.0027
	X42_P10			
A	0.0064			
B	0.0057			
C	0.0060			
D	0.0055			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0211	0.0224	5.0455	2.5373
A to Z ↑	0.0373	0.0378	11.5201	5.2968
B to Z ↓	0.0190	0.0197	4.9689	2.5397
B to Z ↑	0.0346	0.0329	11.5429	5.3117
C to Z ↓	0.0184	0.0198	5.0860	2.5443
C to Z ↑	0.0280	0.0300	11.3282	5.3038
D to Z ↓	0.0158	0.0163	5.0047	2.5559
D to Z ↑	0.0250	0.0238	11.3659	5.3285
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0215	0.0219	1.7401	1.2477
A to Z ↑	0.0355	0.0367	3.5533	2.6130
B to Z ↓	0.0193	0.0192	1.7495	1.2447
B to Z ↑	0.0317	0.0324	3.5640	2.6213
C to Z ↓	0.0191	0.0193	1.7444	1.2514
C to Z ↑	0.0279	0.0288	3.5587	2.6141
D to Z ↓	0.0161	0.0159	1.7701	1.2551
D to Z ↑	0.0230	0.0233	3.5769	2.6275
	X42_P10		**X42_P10**	
A to Z ↓	0.0221		0.6498	
A to Z ↑	0.0365		1.3232	
B to Z ↓	0.0194		0.6431	
B to Z ↑	0.0323		1.3275	
C to Z ↓	0.0198		0.6529	
C to Z ↑	0.0286		1.3175	
D to Z ↓	0.0162		0.6489	
D to Z ↑	0.0233		1.3248	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P10	7.948e-07	9.409e-10
X10_P10	1.596e-06	1.536e-09
X15_P10	2.178e-06	1.894e-09
X21_P10	3.001e-06	2.489e-09
X42_P10	5.758e-06	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	3.388e-05	1.133e-04	1.460e-04	2.139e-04
B (output stable)	1.466e-05	5.560e-05	7.072e-05	9.775e-05
C (output stable)	8.257e-05	2.643e-04	3.148e-04	4.744e-04
D (output stable)	6.497e-05	1.756e-04	2.206e-04	3.146e-04
A to Z	1.516e-03	3.486e-03	4.730e-03	6.730e-03
B to Z	1.234e-03	2.621e-03	3.590e-03	5.100e-03
C to Z	1.031e-03	2.496e-03	3.317e-03	4.732e-03
D to Z	7.614e-04	1.614e-03	2.186e-03	3.077e-03
	X42_P10			
A (output stable)	4.168e-04			
B (output stable)	1.995e-04			
C (output stable)	9.278e-04			
D (output stable)	6.228e-04			

A to Z	1.325e-02			
B to Z	9.981e-03			
C to Z	9.334e-03			
D to Z	6.080e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

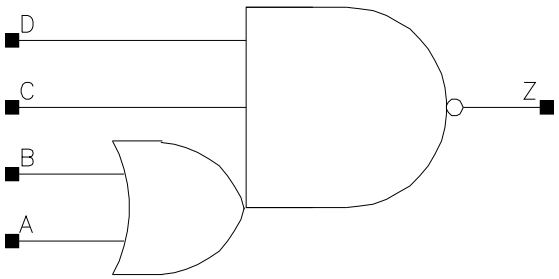
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	-1.223e-06	-6.623e-06	-5.437e-06	-1.044e-05
B (output stable)	1.120e-05	3.268e-05	3.178e-05	5.537e-05
C (output stable)	-1.708e-06	-1.580e-05	-1.022e-05	-2.240e-05
D (output stable)	1.095e-05	3.949e-05	3.396e-05	6.483e-05
A to Z	-6.825e-07	-2.772e-06	-3.729e-06	-4.993e-06
B to Z	-5.209e-07	-1.791e-06	-3.667e-08	-3.058e-06
C to Z	-2.747e-07	-2.008e-06	-2.519e-06	-3.473e-06
D to Z	-2.230e-08	-7.412e-07	2.110e-07	-5.127e-07
	X42_P10			
A (output stable)	-1.831e-05			
B (output stable)	9.931e-05			
C (output stable)	-3.913e-05			
D (output stable)	1.130e-04			
A to Z	-1.018e-05			
B to Z	-1.232e-06			
C to Z	-8.015e-06			
D to Z	-1.077e-06			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X21_P10	1.200	2.448	2.9376
X31_P10	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X21_P10	X31_P10
A	0.0008	0.0015	0.0030	0.0044
B	0.0010	0.0014	0.0026	0.0039
C	0.0008	0.0016	0.0031	0.0046
D	0.0008	0.0015	0.0029	0.0043

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0260	0.0246	7.3197	3.8597
A to Z ↑	0.0351	0.0324	10.3951	5.2247
B to Z ↓	0.0233	0.0202	7.3188	3.8658
B to Z ↑	0.0325	0.0274	10.4473	5.2454
C to Z ↓	0.0252	0.0257	6.9016	3.6461

C to Z ↑	0.0275	0.0269	4.7445	2.3867
D to Z ↓	0.0260	0.0248	6.9136	3.6541
D to Z ↑	0.0264	0.0248	4.7914	2.3898
	X21_P10	**X31_P10**	**X21_P10**	**X31_P10**
A to Z ↓	0.0246	0.0248	2.0080	1.3600
A to Z ↑	0.0314	0.0312	2.6108	1.7489
B to Z ↓	0.0199	0.0199	2.0125	1.3660
B to Z ↑	0.0263	0.0262	2.6222	1.7574
C to Z ↓	0.0253	0.0254	1.8973	1.2864
C to Z ↑	0.0261	0.0261	1.2074	0.8125
D to Z ↓	0.0245	0.0247	1.9010	1.2891
D to Z ↑	0.0241	0.0241	1.2083	0.8117

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P10	6.547e-07	1.060e-09
X10_P10	1.208e-06	1.536e-09
X21_P10	2.223e-06	2.489e-09
X31_P10	3.241e-06	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	1.423e-04	3.005e-04	5.674e-04	8.390e-04
B (output stable)	1.394e-04	2.943e-04	5.468e-04	8.087e-04
C (output stable)	2.350e-05	6.808e-05	1.295e-04	1.936e-04
D (output stable)	6.830e-05	2.231e-04	4.073e-04	5.851e-04
A to Z	1.510e-03	2.608e-03	4.942e-03	7.320e-03
B to Z	1.109e-03	1.761e-03	3.271e-03	4.837e-03
C to Z	1.773e-03	3.387e-03	6.383e-03	9.460e-03
D to Z	1.599e-03	2.833e-03	5.327e-03	7.909e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

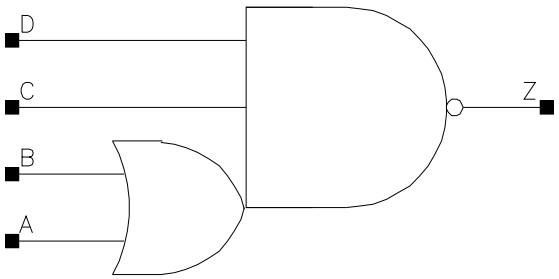
Pin Cycle (vdds)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	-3.309e-06	-4.785e-06	-8.838e-06	-1.213e-05
B (output stable)	4.316e-06	7.932e-06	1.184e-05	1.656e-05
C (output stable)	7.646e-08	6.798e-08	7.842e-08	9.412e-08
D (output stable)	-9.688e-08	-1.503e-07	-3.953e-07	-5.764e-07
A to Z	-2.086e-06	-2.637e-06	-4.051e-06	-6.247e-06
B to Z	-2.390e-08	-2.570e-07	-6.320e-07	-1.097e-06
C to Z	6.077e-07	-1.233e-07	1.007e-07	-1.390e-07
D to Z	4.567e-07	-3.193e-07	3.733e-08	-1.456e-06

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0008	0.0016	0.0024	0.0032
B	0.0008	0.0015	0.0022	0.0030
C	0.0008	0.0015	0.0023	0.0030
D	0.0008	0.0014	0.0021	0.0028

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0258	0.0278	7.4648	3.8541
A to Z ↑	0.0376	0.0406	10.1845	5.1667
B to Z ↓	0.0229	0.0242	7.3639	3.8495
B to Z ↑	0.0356	0.0367	10.2064	5.1765
C to Z ↓	0.0204	0.0228	7.0245	3.6468

C to Z ↑	0.0222	0.0233	4.8097	2.4293
D to Z ↓	0.0198	0.0205	7.0533	3.6630
D to Z ↑	0.0200	0.0201	4.8352	2.4444
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0274	0.0276	2.6520	1.9922
A to Z ↑	0.0390	0.0399	3.4689	2.6211
B to Z ↓	0.0240	0.0240	2.6465	1.9870
B to Z ↑	0.0358	0.0364	3.4768	2.6268
C to Z ↓	0.0223	0.0227	2.5065	1.8837
C to Z ↑	0.0225	0.0228	1.6180	1.2185
D to Z ↓	0.0202	0.0205	2.5174	1.8906
D to Z ↑	0.0194	0.0197	1.6282	1.2263

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P10	6.358e-07	1.060e-09
X10_P10	1.246e-06	1.536e-09
X15_P10	1.682e-06	1.894e-09
X21_P10	2.336e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	2.002e-05	5.309e-05	7.120e-05	1.002e-04
B (output stable)	1.364e-05	4.062e-05	5.264e-05	7.338e-05
C (output stable)	7.342e-05	1.550e-04	2.375e-04	3.074e-04
D (output stable)	1.261e-04	4.350e-04	5.184e-04	7.741e-04
A to Z	1.718e-03	3.793e-03	5.341e-03	7.320e-03
B to Z	1.407e-03	2.953e-03	4.178e-03	5.702e-03
C to Z	1.081e-03	2.485e-03	3.427e-03	4.744e-03
D to Z	8.793e-04	1.863e-03	2.617e-03	3.577e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

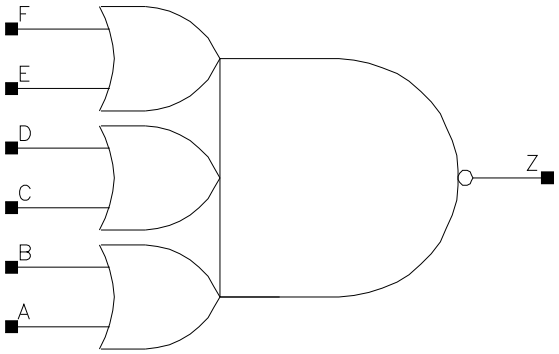
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	-6.627e-07	-3.724e-06	-3.068e-06	-6.062e-06
B (output stable)	2.596e-06	9.390e-06	7.957e-06	1.523e-05
C (output stable)	1.485e-08	-1.956e-07	-8.121e-07	-4.856e-07
D (output stable)	-3.144e-09	-1.985e-06	-2.211e-06	-3.697e-06
A to Z	2.100e-08	-2.588e-06	-2.135e-06	-3.598e-06
B to Z	1.700e-08	-1.120e-07	-9.860e-07	-3.490e-07
C to Z	7.467e-08	3.513e-07	-1.943e-07	-5.477e-07
D to Z	3.070e-08	1.059e-06	-3.233e-07	7.617e-07

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	1.088	1.3056
X9_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X9_P10
A	0.0007	0.0017
B	0.0006	0.0015
C	0.0007	0.0016
D	0.0006	0.0014
E	0.0006	0.0015
F	0.0006	0.0014

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X9_P10	X3_P10	X9_P10
A to Z ↓	0.0327	0.0337	8.6521	3.4786
A to Z ↑	0.0504	0.0475	14.4694	5.1891
B to Z ↓	0.0309	0.0302	8.6877	3.4768
B to Z ↑	0.0496	0.0435	14.4933	5.1984
C to Z ↓	0.0309	0.0313	8.6945	3.4864
C to Z ↑	0.0439	0.0414	14.4813	5.1769
D to Z ↓	0.0287	0.0278	8.7158	3.4872
D to Z ↑	0.0427	0.0371	14.5079	5.1893
E to Z ↓	0.0258	0.0268	8.7091	3.4791
E to Z ↑	0.0344	0.0332	14.5042	5.1778
F to Z ↓	0.0236	0.0226	8.7307	3.4833
F to Z ↑	0.0330	0.0279	14.5511	5.1977

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P10	7.708e-07	1.298e-09
X9_P10	1.898e-06	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P10	X9_P10
A (output stable)	2.355e-05	9.540e-05
B (output stable)	1.429e-05	6.423e-05
C (output stable)	6.195e-05	2.150e-04
D (output stable)	5.249e-05	1.578e-04
E (output stable)	1.562e-04	3.908e-04
F (output stable)	1.472e-04	3.517e-04
A to Z	2.017e-03	5.269e-03
B to Z	1.820e-03	4.424e-03
C to Z	1.644e-03	4.305e-03
D to Z	1.448e-03	3.503e-03
E to Z	1.179e-03	3.244e-03
F to Z	9.882e-04	2.408e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

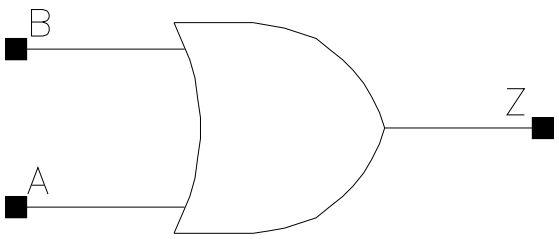
Pin Cycle (vdds)	X3_P10	X9_P10
A (output stable)	-7.766e-07	-5.477e-06
B (output stable)	5.625e-06	2.941e-05
C (output stable)	-1.056e-06	-1.071e-05
D (output stable)	5.709e-06	2.715e-05
E (output stable)	-1.561e-06	-7.668e-06
F (output stable)	4.858e-06	2.177e-05
A to Z	-2.821e-07	4.536e-07
B to Z	-1.026e-07	1.979e-07
C to Z	-5.583e-07	-3.391e-06
D to Z	-3.084e-07	-1.300e-06
E to Z	-3.832e-07	-2.758e-06
F to Z	-2.036e-07	-1.621e-06

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X33_P10	1.200	1.360	1.6320
X50_P10	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P10	X16_P10	X33_P10	X50_P10
A	0.0007	0.0009	0.0017	0.0018
B	0.0006	0.0009	0.0018	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0607	0.0524	2.8166	1.4224
A to Z ↑	0.0330	0.0332	4.8358	2.4341
B to Z ↓	0.0581	0.0503	2.8176	1.4227
B to Z ↑	0.0314	0.0311	4.8336	2.4321
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0541	0.0633	0.7034	0.4862
A to Z ↑	0.0329	0.0326	1.1856	0.7996
B to Z ↓	0.0498	0.0595	0.7039	0.4860
B to Z ↑	0.0305	0.0307	1.1854	0.7980

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.039e-06	8.218e-10
X16_P10	1.810e-06	9.409e-10
X33_P10	3.583e-06	1.536e-09
X50_P10	4.830e-06	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	2.287e-05	4.280e-05	1.406e-04	1.321e-04
B (output stable)	5.521e-06	8.643e-06	8.472e-05	7.420e-05
A to Z	1.915e-03	3.003e-03	6.345e-03	8.386e-03
B to Z	1.755e-03	2.715e-03	5.497e-03	7.585e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

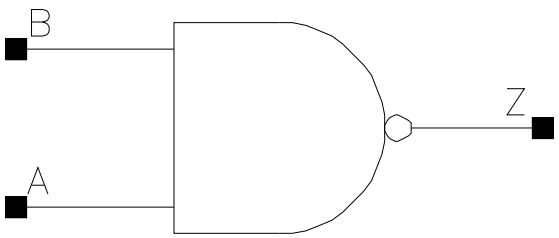
Pin Cycle (vdds)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	-1.175e-06	-1.830e-06	-9.118e-06	-8.686e-06
B (output stable)	1.159e-05	2.073e-05	8.070e-05	7.927e-05
A to Z	-4.322e-07	-4.013e-07	-3.230e-06	-3.002e-06
B to Z	-2.311e-07	-3.411e-07	-4.005e-07	-8.732e-07

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X16_P10	1.200	0.952	1.1424
X24_P10	1.200	1.088	1.3056
X32_P10	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P10	X16_P10	X24_P10	X32_P10
A	0.0009	0.0009	0.0009	0.0009
B	0.0010	0.0011	0.0011	0.0010

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0461	0.0478	2.7073	1.4091
A to Z ↑	0.0492	0.0501	4.8688	2.4788
B to Z ↓	0.0473	0.0490	2.7089	1.4094
B to Z ↑	0.0473	0.0476	4.8671	2.4778
	X24_P10	**X32_P10**	**X24_P10**	**X32_P10**
A to Z ↓	0.0532	0.0538	0.9585	0.7256
A to Z ↑	0.0538	0.0550	1.6564	1.2382
B to Z ↓	0.0545	0.0552	0.9582	0.7251
B to Z ↑	0.0513	0.0532	1.6553	1.2374

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	1.756e-06	1.060e-09
X16_P10	2.386e-06	1.179e-09
X24_P10	2.961e-06	1.298e-09
X32_P10	3.545e-06	1.417e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	2.095e-05	2.097e-05	2.106e-05	2.206e-05
B (output stable)	4.605e-05	4.624e-05	4.634e-05	4.952e-05
A to Z	3.732e-03	4.264e-03	5.397e-03	7.094e-03
B to Z	3.554e-03	4.097e-03	5.239e-03	6.921e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

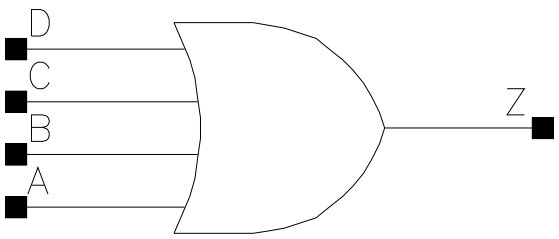
Pin Cycle (vdds)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	1.020e-08	1.227e-08	1.245e-08	8.330e-09
B (output stable)	-5.020e-09	-4.810e-09	-4.730e-09	-6.230e-09
A to Z	-1.479e-07	-2.352e-07	-3.508e-07	-6.225e-07
B to Z	-2.547e-07	-2.082e-07	-4.240e-07	-2.373e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P10	1.200	2.176	2.6112
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P10	X27_P10
A	0.0016	0.0018
B	0.0015	0.0018
C	0.0016	0.0019
D	0.0015	0.0019

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P10	X27_P10	X20_P10	X27_P10
A to Z ↓	0.0601	0.0627	1.7936	1.3416
A to Z ↑	0.0346	0.0333	1.5879	1.1848
B to Z ↓	0.0564	0.0583	1.7898	1.3406
B to Z ↑	0.0327	0.0311	1.5869	1.1833
C to Z ↓	0.0578	0.0605	1.7900	1.3413
C to Z ↑	0.0329	0.0323	1.5906	1.1891
D to Z ↓	0.0543	0.0566	1.7879	1.3388
D to Z ↑	0.0311	0.0305	1.5903	1.1879

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X20_P10	2.714e-06	2.251e-09
X27_P10	3.858e-06	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X20_P10	X27_P10
A (output stable)	1.458e-03	2.029e-03
B (output stable)	1.169e-03	1.618e-03
C (output stable)	1.382e-03	2.007e-03
D (output stable)	1.077e-03	1.593e-03
A to Z	6.006e-03	8.504e-03
B to Z	5.411e-03	7.630e-03
C to Z	5.240e-03	7.309e-03
D to Z	4.655e-03	6.519e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

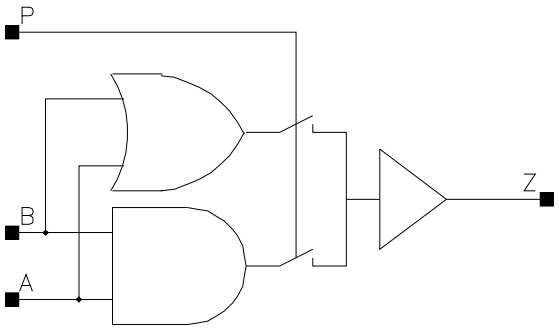
Pin Cycle (vdds)	X20_P10	X27_P10
A (output stable)	-3.064e-06	-6.466e-06
B (output stable)	1.706e-05	3.502e-05
C (output stable)	-5.441e-06	-1.454e-05
D (output stable)	1.965e-05	4.066e-05
A to Z	-1.738e-06	-3.247e-06
B to Z	-4.950e-07	-5.420e-07
C to Z	-1.233e-06	-3.106e-06
D to Z	-1.030e-07	3.900e-08

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X16_P10	1.200	1.224	1.4688
X25_P10	1.200	2.040	2.4480
X33_P10	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0012	0.0017	0.0030	0.0030
B	0.0011	0.0016	0.0033	0.0033
P	0.0006	0.0009	0.0017	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0737	0.0656	2.8938	1.4130
A to Z ↑	0.0464	0.0419	4.9075	2.4515
B to Z ↓	0.0724	0.0645	2.9123	1.4237
B to Z ↑	0.0476	0.0430	4.9115	2.4558
P to Z ↓	0.0646	0.0583	2.9190	1.4264
P to Z ↑	0.0452	0.0413	4.9042	2.4520
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**

A to Z ↓	0.0623	0.0662	0.9587	0.7285
A to Z ↑	0.0414	0.0433	1.6444	1.2322
B to Z ↓	0.0612	0.0646	0.9653	0.7325
B to Z ↑	0.0428	0.0442	1.6466	1.2337
P to Z ↓	0.0560	0.0598	0.9669	0.7340
P to Z ↑	0.0405	0.0422	1.6446	1.2323

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	9.570e-07	1.179e-09
X16_P10	1.925e-06	1.417e-09
X25_P10	3.123e-06	2.132e-09
X33_P10	3.565e-06	2.251e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	4.628e-05	7.418e-05	1.639e-04	1.652e-04
B (output stable)	9.859e-05	1.451e-04	2.622e-04	2.645e-04
P (output stable)	1.031e-04	1.702e-04	2.906e-04	2.987e-04
A to Z	2.228e-03	3.742e-03	6.491e-03	7.360e-03
B to Z	2.159e-03	3.620e-03	6.223e-03	7.105e-03
P to Z	1.914e-03	3.269e-03	5.690e-03	6.561e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

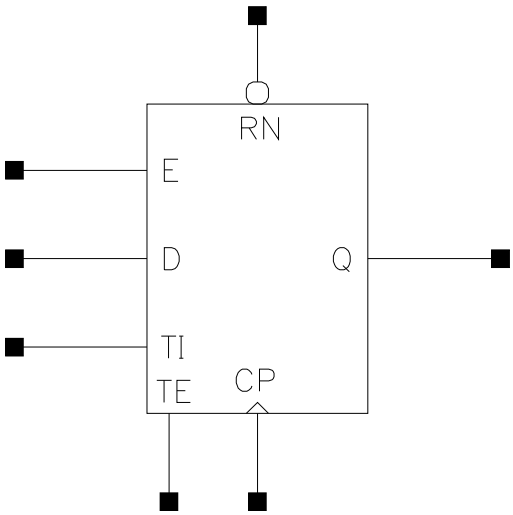
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	-2.529e-06	-3.391e-06	-5.345e-06	-5.351e-06
B (output stable)	-6.533e-06	-5.361e-06	8.885e-06	9.226e-06
P (output stable)	1.707e-05	3.219e-05	4.170e-05	4.299e-05
A to Z	-1.849e-06	-2.077e-06	-4.307e-06	-4.236e-06
B to Z	-1.418e-06	-1.677e-06	-3.762e-06	-3.765e-06
P to Z	-2.453e-07	-3.991e-07	-1.316e-06	-1.318e-06

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.488	5.3856
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0006	0.0006	0.0006
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0006	0.0007	0.0008
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to Q ↓	0.1501	0.0692	6.7110	2.8049
CP to Q ↑	0.1083	0.0884	10.2981	4.8457
RN to Q ↓	0.1144	0.0944	5.5115	3.0254
	X17_P10	X33_P10	X17_P10	X33_P10
CP to Q ↓	0.1203	0.1258	1.3558	0.7139
CP to Q ↑	0.1468	0.1530	2.3798	1.2096
RN to Q ↓	0.1621	0.1674	1.3524	0.7123

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.2214	0.1449	0.1431	0.1431
CP ↑	min_pulse_width to CP	0.1409	0.0549	0.0502	0.0502
D ↓	hold_rising to CP	-0.2305	-0.1187	-0.1236	-0.1236
D ↑	hold_rising to CP	-0.1235	-0.0459	-0.0459	-0.0484
D ↓	setup_rising to CP	0.3146	0.1981	0.1981	0.1954
D ↑	setup_rising to CP	0.1707	0.0908	0.0908	0.0908
E ↓	hold_rising to CP	-0.1475	-0.1448	-0.1475	-0.1475
E ↑	hold_rising to CP	-0.1243	-0.0481	-0.0481	-0.0481
E ↓	setup_rising to CP	0.2727	0.2705	0.2705	0.2705
E ↑	setup_rising to CP	0.3031	0.2054	0.2027	0.2027
RN ↓	min_pulse_width to RN	0.1187	0.1284	0.1169	0.1169
RN ↑	recovery_rising to CP	0.0345	0.0342	0.0345	0.0345
RN ↑	removal_rising to CP	-0.0215	-0.0152	-0.0149	-0.0149
TE ↓	hold_rising to CP	-0.1106	-0.0819	-0.0849	-0.0849
TE ↑	hold_rising to CP	-0.0845	-0.0556	-0.0552	-0.0552
TE ↓	setup_rising to CP	0.2048	0.1612	0.1612	0.1612
TE ↑	setup_rising to CP	0.3981	0.2809	0.2787	0.2787
TI ↓	hold_rising to CP	-0.3041	-0.1697	-0.1745	-0.1745
TI ↑	hold_rising to CP	-0.1000	-0.0590	-0.0583	-0.0583
TI ↓	setup_rising to CP	0.3883	0.2536	0.2538	0.2538
TI ↑	setup_rising to CP	0.1449	0.1083	0.1032	0.1032

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.584e-06	4.557e-09
X8_P10	3.889e-06	4.276e-09
X17_P10	4.710e-06	4.514e-09
X33_P10	5.605e-06	4.752e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

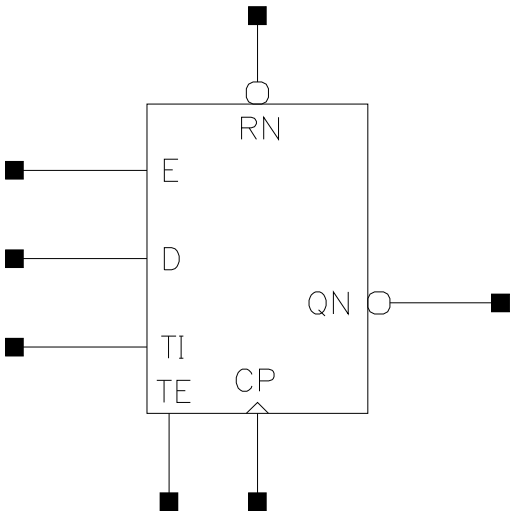
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.529e-03	3.558e-03	3.565e-03	3.569e-03
Clock 100Mhz Data 25Mhz	5.720e-03	5.857e-03	6.425e-03	7.033e-03
Clock 100Mhz Data 50Mhz	7.911e-03	8.156e-03	9.285e-03	1.050e-02
Clock = 0 Data 100Mhz	4.953e-03	4.853e-03	4.821e-03	4.805e-03
Clock = 1 Data 100Mhz	1.953e-03	1.980e-03	1.991e-03	1.996e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.624	5.5488
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0006	0.0006	0.0006
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to QN ↓	0.1351	0.1223	5.3306	2.7047
CP to QN ↑	0.1646	0.0917	10.0801	4.7224
RN to QN ↑	0.1385	0.1364	10.0374	4.7227
	X17_P10	X33_P10	X17_P10	X33_P10
CP to QN ↓	0.1153	0.1211	1.3567	0.7147
CP to QN ↑	0.0966	0.1043	2.3806	1.2115
RN to QN ↑	0.1356	0.1485	2.3908	1.2171

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.2208	0.1460	0.1449	0.1449
CP ↑	min_pulse_width to CP	0.1022	0.0501	0.0560	0.0598
D ↓	hold_rising to CP	-0.2403	-0.1240	-0.1187	-0.1187
D ↑	hold_rising to CP	-0.1261	-0.0459	-0.0459	-0.0459
D ↓	setup_rising to CP	0.3145	0.1978	0.1978	0.1978
D ↑	setup_rising to CP	0.1685	0.0908	0.0933	0.0908
E ↓	hold_rising to CP	-0.1475	-0.1479	-0.1448	-0.1448
E ↑	hold_rising to CP	-0.1243	-0.0481	-0.0481	-0.0481
E ↓	setup_rising to CP	0.2775	0.2705	0.2705	0.2705
E ↑	setup_rising to CP	0.3031	0.2054	0.2054	0.2054
RN ↓	min_pulse_width to RN	0.1160	0.1169	0.1284	0.1382
RN ↑	recovery_rising to CP	0.0314	0.0367	0.0367	0.0370
RN ↑	removal_rising to CP	-0.0246	-0.0174	-0.0149	-0.0149
TE ↓	hold_rising to CP	-0.1137	-0.0849	-0.0819	-0.0819
TE ↑	hold_rising to CP	-0.0870	-0.0556	-0.0525	-0.0525
TE ↓	setup_rising to CP	0.2048	0.1612	0.1612	0.1612
TE ↑	setup_rising to CP	0.3957	0.2809	0.2836	0.2805
TI ↓	hold_rising to CP	-0.3090	-0.1751	-0.1697	-0.1697
TI ↑	hold_rising to CP	-0.1015	-0.0583	-0.0590	-0.0575
TI ↓	setup_rising to CP	0.3883	0.2531	0.2546	0.2546
TI ↑	setup_rising to CP	0.1449	0.1083	0.1083	0.1083

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.764e-06	4.557e-09
X8_P10	4.168e-06	4.395e-09
X17_P10	5.033e-06	4.514e-09
X33_P10	6.184e-06	4.752e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

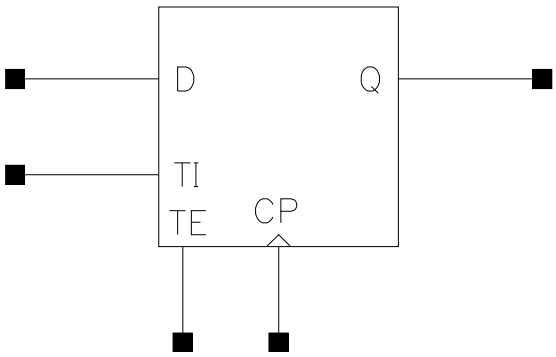
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.532e-03	3.560e-03	3.565e-03	3.568e-03
Clock 100Mhz Data 25Mhz	5.715e-03	5.899e-03	6.374e-03	6.969e-03
Clock 100Mhz Data 50Mhz	7.899e-03	8.238e-03	9.182e-03	1.037e-02
Clock = 0 Data 100Mhz	4.948e-03	4.851e-03	4.819e-03	4.804e-03
Clock = 1 Data 100Mhz	1.951e-03	1.982e-03	1.994e-03	1.999e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.400	4.0800
X8_P10	1.200	3.128	3.7536
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1203	0.0641	6.2336	2.7941
CP to Q ↑	0.0967	0.0797	10.3651	4.7897
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0979	0.1072	1.3259	0.7011
CP to Q ↑	0.1459	0.1540	2.3681	1.2054

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1914	0.1987	0.1987	0.1987
CP ↑	min_pulse_width to CP	0.0975	0.0464	0.0454	0.0454
D ↓	hold_rising to CP	-0.1427	-0.0679	-0.0706	-0.0706
D ↑	hold_rising to CP	-0.0525	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1998	0.1343	0.1343	0.1343
D ↑	setup_rising to CP	0.0874	0.0436	0.0436	0.0436
TE ↓	hold_rising to CP	-0.0889	-0.0600	-0.0597	-0.0597
TE ↑	hold_rising to CP	-0.0698	-0.0432	-0.0488	-0.0488
TE ↓	setup_rising to CP	0.1684	0.1295	0.1295	0.1295
TE ↑	setup_rising to CP	0.3470	0.2756	0.2756	0.2756
TI ↓	hold_rising to CP	-0.2900	-0.1808	-0.1862	-0.1856
TI ↑	hold_rising to CP	-0.0804	-0.0449	-0.0449	-0.0449
TI ↓	setup_rising to CP	0.3541	0.2643	0.2648	0.2648
TI ↑	setup_rising to CP	0.1205	0.0850	0.0811	0.0811

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	2.884e-06	3.323e-09
X8_P10	3.234e-06	3.085e-09
X17_P10	4.412e-06	3.442e-09
X33_P10	5.298e-06	3.680e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

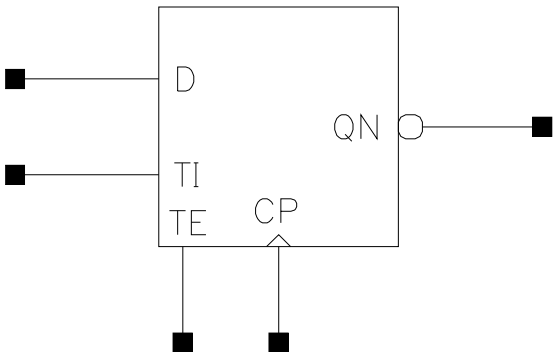
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.155e-03	3.183e-03	3.189e-03	3.192e-03
Clock 100Mhz Data 25Mhz	4.688e-03	4.781e-03	5.318e-03	5.821e-03
Clock 100Mhz Data 50Mhz	6.221e-03	6.380e-03	7.448e-03	8.450e-03
Clock = 0 Data 100Mhz	3.935e-03	3.742e-03	3.677e-03	3.645e-03
Clock = 1 Data 100Mhz	1.115e-03	5.807e-04	4.026e-04	3.136e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.536	4.2432
X8_P10	1.200	3.264	3.9168
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1281	0.1349	6.1607	2.8254
CP to QN ↑	0.1308	0.0846	10.2751	4.7414
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0970	0.1073	1.3266	0.7022
CP to QN ↑	0.0833	0.0919	2.3701	1.2072

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1876	0.1987	0.1987	0.1987
CP ↑	min_pulse_width to CP	0.0781	0.0453	0.0501	0.0512
D ↓	hold_rising to CP	-0.1427	-0.0706	-0.0654	-0.0654
D ↑	hold_rising to CP	-0.0525	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1971	0.1343	0.1343	0.1343
D ↑	setup_rising to CP	0.0874	0.0436	0.0436	0.0436
TE ↓	hold_rising to CP	-0.0889	-0.0597	-0.0600	-0.0600
TE ↑	hold_rising to CP	-0.0720	-0.0488	-0.0432	-0.0432
TE ↓	setup_rising to CP	0.1654	0.1295	0.1295	0.1295
TE ↑	setup_rising to CP	0.3470	0.2756	0.2756	0.2756
TI ↓	hold_rising to CP	-0.2895	-0.1862	-0.1813	-0.1808
TI ↑	hold_rising to CP	-0.0802	-0.0449	-0.0449	-0.0449
TI ↓	setup_rising to CP	0.3485	0.2648	0.2643	0.2643
TI ↑	setup_rising to CP	0.1205	0.0811	0.0850	0.0850

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	2.918e-06	3.442e-09
X8_P10	3.265e-06	3.204e-09
X17_P10	4.387e-06	3.442e-09
X33_P10	5.272e-06	3.680e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

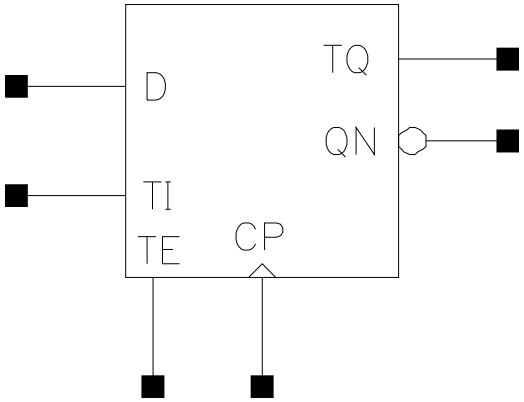
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.124e-03	3.185e-03	3.204e-03	3.213e-03
Clock 100Mhz Data 25Mhz	4.701e-03	4.865e-03	5.300e-03	5.822e-03
Clock 100Mhz Data 50Mhz	6.278e-03	6.545e-03	7.396e-03	8.431e-03
Clock = 0 Data 100Mhz	3.949e-03	3.750e-03	3.684e-03	3.650e-03
Clock = 1 Data 100Mhz	1.108e-03	5.909e-04	4.185e-04	3.323e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.536	4.2432
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0012	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006
TE	0.0009	0.0010	0.0010	0.0010

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1425	0.1161	5.4987	2.7085
CP to QN ↑	0.1601	0.0885	10.0496	4.7429
CP to TQ ↓	0.1115	0.0593	7.9333	5.3026
CP to TQ ↑	0.1003	0.0799	20.6784	14.1755
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.1077	0.1152	1.3600	0.7174
CP to QN ↑	0.0905	0.0960	2.3976	1.2265
CP to TQ ↓	0.0622	0.0651	7.1912	7.1970
CP to TQ ↑	0.0816	0.0839	18.9012	20.0808

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1913	0.1987	0.1987	0.1987
CP ↑	min_pulse_width to CP	0.0975	0.0501	0.0501	0.0550
D ↓	hold_rising to CP	-0.1430	-0.0654	-0.0654	-0.0654
D ↑	hold_rising to CP	-0.0500	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1971	0.1346	0.1346	0.1346
D ↑	setup_rising to CP	0.0849	0.0436	0.0436	0.0436
TE ↓	hold_rising to CP	-0.0889	-0.0600	-0.0600	-0.0600
TE ↑	hold_rising to CP	-0.0698	-0.0463	-0.0463	-0.0432
TE ↓	setup_rising to CP	0.1685	0.1295	0.1295	0.1295
TE ↑	setup_rising to CP	0.3470	0.2760	0.2760	0.2760
TI ↓	hold_rising to CP	-0.2844	-0.1813	-0.1813	-0.1813
TI ↑	hold_rising to CP	-0.0804	-0.0449	-0.0449	-0.0449
TI ↓	setup_rising to CP	0.3541	0.2648	0.2648	0.2648
TI ↑	setup_rising to CP	0.1205	0.0850	0.0850	0.0850

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.221e-06	3.688e-09
X8_P10	3.654e-06	3.442e-09
X17_P10	4.221e-06	3.561e-09
X33_P10	5.301e-06	3.799e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10

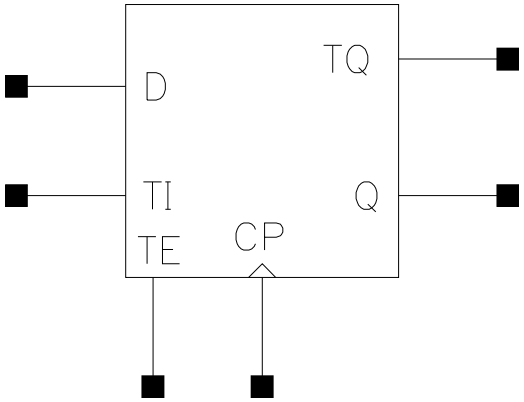
Clock 100Mhz Data 0Mhz	3.221e-03	3.217e-03	3.216e-03	3.216e-03
Clock 100Mhz Data 25Mhz	4.942e-03	5.094e-03	5.311e-03	5.868e-03
Clock 100Mhz Data 50Mhz	6.664e-03	6.970e-03	7.406e-03	8.520e-03
Clock = 0 Data 100Mhz	3.945e-03	3.750e-03	3.686e-03	3.654e-03
Clock = 1 Data 100Mhz	1.115e-03	5.768e-04	3.975e-04	3.080e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.400	4.0800
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0008	0.0008
D	0.0008	0.0006	0.0006	0.0006

TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1591	0.0721	6.7174	2.8026
CP to Q ↑	0.1114	0.0846	10.5101	4.8239
CP to TQ ↓	0.1550	0.0774	6.6888	7.3458
CP to TQ ↑	0.1151	0.0950	14.2333	20.3742
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.1007	0.1100	1.3634	0.7160
CP to Q ↑	0.1488	0.1565	2.4137	1.2120
CP to TQ ↓	0.1058	0.1175	6.9712	7.0991
CP to TQ ↑	0.1588	0.1695	19.6540	19.8187

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1895	0.1987	0.1987	0.1987
CP ↑	min_pulse_width to CP	0.1410	0.0549	0.0454	0.0454
D ↓	hold_rising to CP	-0.1427	-0.0654	-0.0706	-0.0706
D ↑	hold_rising to CP	-0.0525	-0.0139	-0.0139	-0.0139
D ↓	setup_rising to CP	0.1974	0.1346	0.1343	0.1346
D ↑	setup_rising to CP	0.0874	0.0436	0.0436	0.0436
TE ↓	hold_rising to CP	-0.0889	-0.0575	-0.0597	-0.0597
TE ↑	hold_rising to CP	-0.0720	-0.0432	-0.0488	-0.0488
TE ↓	setup_rising to CP	0.1658	0.1295	0.1295	0.1295
TE ↑	setup_rising to CP	0.3444	0.2760	0.2756	0.2760
TI ↓	hold_rising to CP	-0.2895	-0.1813	-0.1856	-0.1856
TI ↑	hold_rising to CP	-0.0802	-0.0449	-0.0449	-0.0449
TI ↓	setup_rising to CP	0.3491	0.2648	0.2648	0.2648
TI ↑	setup_rising to CP	0.1205	0.0850	0.0811	0.0811

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.218e-06	3.561e-09
X8_P10	3.460e-06	3.323e-09
X17_P10	4.586e-06	3.561e-09
X33_P10	5.461e-06	3.799e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

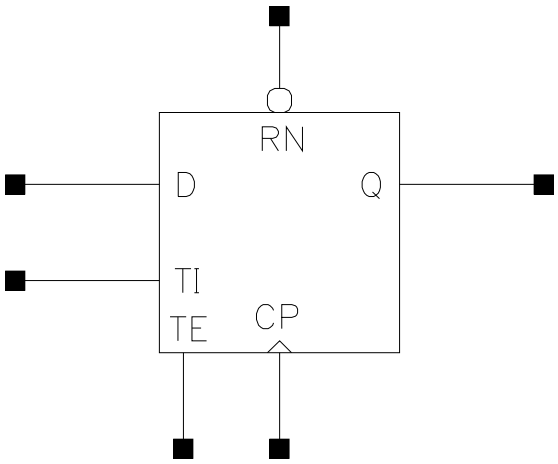
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.146e-03	3.176e-03	3.185e-03	3.190e-03
Clock 100Mhz Data 25Mhz	4.921e-03	4.951e-03	5.481e-03	6.000e-03
Clock 100Mhz Data 50Mhz	6.695e-03	6.726e-03	7.778e-03	8.809e-03
Clock = 0 Data 100Mhz	3.928e-03	3.737e-03	3.674e-03	3.643e-03
Clock = 1 Data 100Mhz	1.107e-03	5.727e-04	3.949e-04	3.060e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.672	4.4064
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006
RN	0.0008	0.0006	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1466	0.0690	6.8604	2.8149
CP to Q ↑	0.1065	0.0865	10.3611	4.8404
RN to Q ↓	0.1126	0.0952	5.6222	2.9961
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.1026	0.1125	1.3450	0.7122
CP to Q ↑	0.1288	0.1360	2.3683	1.2073
RN to Q ↓	0.1451	0.1549	1.3405	0.7105

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.2161	0.2059	0.2108	0.2108
CP ↑	min_pulse_width to CP	0.1265	0.0501	0.0453	0.0453
D ↓	hold_rising to CP	-0.1280	-0.0508	-0.0529	-0.0529
D ↑	hold_rising to CP	-0.0626	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.1971	0.1295	0.1294	0.1294
D ↑	setup_rising to CP	0.1021	0.0585	0.0585	0.0585
RN ↓	min_pulse_width to RN	0.1160	0.1187	0.1147	0.1147
RN ↑	recovery_rising to CP	0.0367	0.0394	0.0367	0.0367
RN ↑	removal_rising to CP	-0.0246	-0.0148	-0.0149	-0.0149
TE ↓	hold_rising to CP	-0.0965	-0.0459	-0.0511	-0.0511
TE ↑	hold_rising to CP	-0.0845	-0.0530	-0.0586	-0.0583
TE ↓	setup_rising to CP	0.1685	0.1246	0.1246	0.1246
TE ↑	setup_rising to CP	0.3440	0.2689	0.2686	0.2689
TI ↓	hold_rising to CP	-0.2651	-0.1569	-0.1619	-0.1618
TI ↑	hold_rising to CP	-0.0956	-0.0547	-0.0601	-0.0601
TI ↓	setup_rising to CP	0.3491	0.2544	0.2600	0.2600
TI ↑	setup_rising to CP	0.1400	0.1045	0.1045	0.1047

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.156e-06	3.799e-09
X8_P10	3.429e-06	3.561e-09
X17_P10	4.498e-06	3.918e-09
X33_P10	5.193e-06	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.536e-03	3.566e-03	3.593e-03	3.606e-03

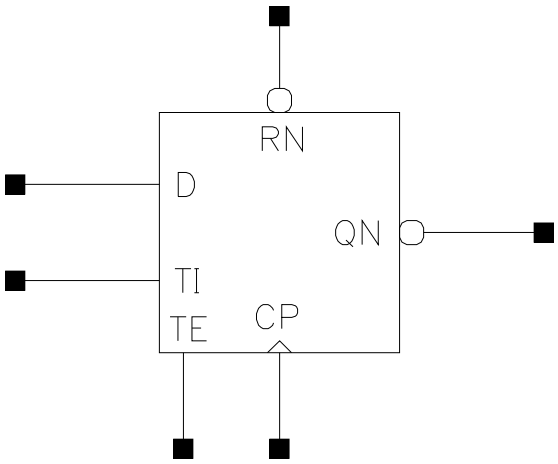
Clock 100Mhz Data 25Mhz	5.287e-03	5.295e-03	5.951e-03	6.488e-03
Clock 100Mhz Data 50Mhz	7.039e-03	7.023e-03	8.309e-03	9.370e-03
Clock = 0 Data 100Mhz	4.071e-03	3.809e-03	3.721e-03	3.678e-03
Clock = 1 Data 100Mhz	1.135e-03	6.110e-04	4.362e-04	3.488e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	3.944	4.7328
X33_P10	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1211	0.1086	5.1862	2.6255
CP to QN ↑	0.1503	0.0827	10.0578	4.7004
RN to QN ↑	0.1283	0.1284	10.0272	4.6902
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.1065	0.1167	1.3455	0.7125
CP to QN ↑	0.0924	0.1013	2.3858	1.2196
RN to QN ↑	0.1324	0.1451	2.3949	1.2225

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.2155	0.2059	0.2071	0.2059
CP ↑	min_pulse_width to CP	0.0926	0.0464	0.0549	0.0598
D ↓	hold_rising to CP	-0.1311	-0.0508	-0.0508	-0.0508
D ↑	hold_rising to CP	-0.0623	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.1971	0.1295	0.1295	0.1295
D ↑	setup_rising to CP	0.1024	0.0585	0.0641	0.0610
RN ↓	min_pulse_width to RN	0.1138	0.1147	0.1257	0.1355
RN ↑	recovery_rising to CP	0.0345	0.0419	0.0394	0.0394
RN ↑	removal_rising to CP	-0.0246	-0.0197	-0.0174	-0.0174
TE ↓	hold_rising to CP	-0.0965	-0.0480	-0.0459	-0.0459
TE ↑	hold_rising to CP	-0.0845	-0.0530	-0.0530	-0.0530
TE ↓	setup_rising to CP	0.1685	0.1246	0.1246	0.1246
TE ↑	setup_rising to CP	0.3440	0.2689	0.2689	0.2689
TI ↓	hold_rising to CP	-0.2649	-0.1569	-0.1569	-0.1569
TI ↑	hold_rising to CP	-0.0956	-0.0547	-0.0547	-0.0547
TI ↓	setup_rising to CP	0.3491	0.2544	0.2600	0.2600
TI ↑	setup_rising to CP	0.1359	0.1047	0.1045	0.1045

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.362e-06	3.844e-09
X8_P10	3.707e-06	3.680e-09
X17_P10	4.667e-06	3.799e-09
X33_P10	5.700e-06	4.038e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.499e-03	3.527e-03	3.536e-03	3.540e-03

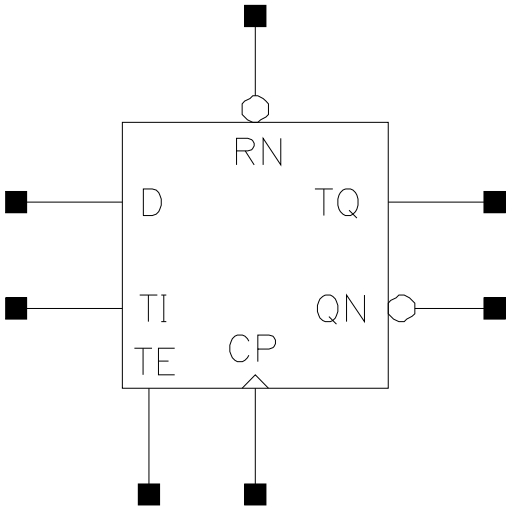
Clock 100Mhz Data 25Mhz	5.225e-03	5.301e-03	5.795e-03	6.294e-03
Clock 100Mhz Data 50Mhz	6.951e-03	7.075e-03	8.054e-03	9.047e-03
Clock = 0 Data 100Mhz	4.073e-03	3.810e-03	3.726e-03	3.685e-03
Clock = 1 Data 100Mhz	1.134e-03	5.916e-04	4.110e-04	3.208e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006

RN	0.0010	0.0007	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1363	0.1127	5.2007	2.7529
CP to QN ↑	0.1990	0.0940	8.9095	4.8720
CP to TQ ↓	0.1409	0.0635	7.1918	5.5364
CP to TQ ↑	0.1117	0.0881	16.2564	14.9258
RN to QN ↑	0.1278	0.1274	9.0135	4.8610
RN to TQ ↓	0.0867	0.0854	6.2217	5.8878
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.1157	0.1235	1.3699	0.7243
CP to QN ↑	0.0943	0.0986	2.4265	1.2209
CP to TQ ↓	0.0665	0.0693	6.9773	6.8226
CP to TQ ↑	0.0882	0.0904	13.8914	14.0843
RN to QN ↑	0.1306	0.1381	2.4239	1.2194
RN to TQ ↓	0.0921	0.0966	7.3266	7.2170

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.2155	0.2059	0.2107	0.2107
CP ↑	min_pulse_width to CP	0.1361	0.0512	0.0512	0.0550
D ↓	hold_rising to CP	-0.1280	-0.0508	-0.0508	-0.0508
D ↑	hold_rising to CP	-0.0626	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.2001	0.1295	0.1295	0.1295
D ↑	setup_rising to CP	0.1021	0.0585	0.0638	0.0638
RN ↓	min_pulse_width to RN	0.1160	0.1187	0.1235	0.1284
RN ↑	recovery_rising to CP	0.0366	0.0394	0.0394	0.0394
RN ↑	removal_rising to CP	-0.0268	-0.0170	-0.0174	-0.0174
TE ↓	hold_rising to CP	-0.0965	-0.0459	-0.0459	-0.0459
TE ↑	hold_rising to CP	-0.0845	-0.0530	-0.0586	-0.0586
TE ↓	setup_rising to CP	0.1685	0.1246	0.1246	0.1246
TE ↑	setup_rising to CP	0.3470	0.2689	0.2689	0.2689
TI ↓	hold_rising to CP	-0.2651	-0.1569	-0.1569	-0.1569
TI ↑	hold_rising to CP	-0.0956	-0.0547	-0.0562	-0.0562
TI ↓	setup_rising to CP	0.3491	0.2544	0.2600	0.2600
TI ↑	setup_rising to CP	0.1400	0.1045	0.1045	0.1060

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.520e-06	3.918e-09
X8_P10	3.881e-06	3.680e-09
X17_P10	4.631e-06	3.918e-09
X33_P10	5.824e-06	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

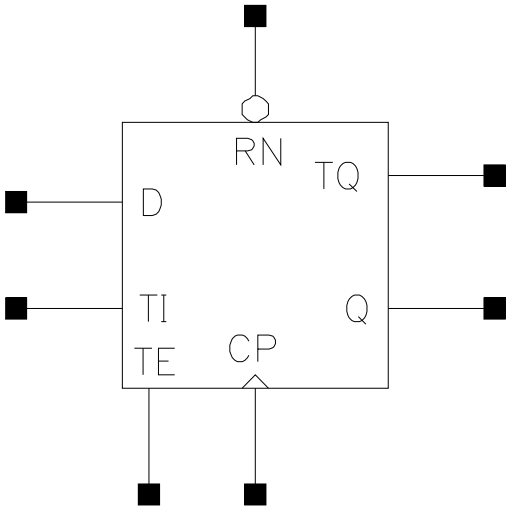
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.504e-03	3.548e-03	3.580e-03	3.597e-03
Clock 100Mhz Data 25Mhz	5.398e-03	5.455e-03	5.735e-03	6.324e-03
Clock 100Mhz Data 50Mhz	7.292e-03	7.362e-03	7.890e-03	9.051e-03
Clock = 0 Data 100Mhz	4.064e-03	3.804e-03	3.715e-03	3.671e-03
Clock = 1 Data 100Mhz	1.134e-03	6.099e-04	4.353e-04	3.481e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006

RN	0.0008	0.0008	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1656	0.0750	7.2726	2.8946
CP to Q ↑	0.1141	0.0901	10.7312	4.9971
CP to TQ ↓	0.1607	0.0776	9.0637	7.4182
CP to TQ ↑	0.1198	0.0967	22.5414	20.2700
RN to Q ↓	0.1169	0.1082	5.8925	3.1086
RN to TQ ↓	0.1155	0.1115	7.5861	7.8206
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.1067	0.1159	1.3681	0.7236
CP to Q ↑	0.1304	0.1369	2.3810	1.2111
CP to TQ ↓	0.1118	0.1248	7.0249	7.1307
CP to TQ ↑	0.1398	0.1509	19.8368	19.9096
RN to Q ↓	0.1494	0.1585	1.3618	0.7207
RN to TQ ↓	0.1545	0.1674	7.0222	7.1241

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.2136	0.2059	0.2059	0.2060
CP ↑	min_pulse_width to CP	0.1469	0.0587	0.0464	0.0459
D ↓	hold_rising to CP	-0.1280	-0.0511	-0.0533	-0.0529
D ↑	hold_rising to CP	-0.0623	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.1974	0.1295	0.1295	0.1298
D ↑	setup_rising to CP	0.1021	0.0638	0.0589	0.0589
RN ↓	min_pulse_width to RN	0.1208	0.1333	0.1121	0.1121
RN ↑	recovery_rising to CP	0.0345	0.0419	0.0367	0.0367
RN ↑	removal_rising to CP	-0.0246	-0.0174	-0.0174	-0.0174
TE ↓	hold_rising to CP	-0.0965	-0.0459	-0.0511	-0.0511
TE ↑	hold_rising to CP	-0.0845	-0.0530	-0.0530	-0.0586
TE ↓	setup_rising to CP	0.1658	0.1246	0.1246	0.1246
TE ↑	setup_rising to CP	0.3422	0.2689	0.2689	0.2689
TI ↓	hold_rising to CP	-0.2651	-0.1520	-0.1563	-0.1619
TI ↑	hold_rising to CP	-0.0956	-0.0547	-0.0547	-0.0547
TI ↓	setup_rising to CP	0.3492	0.2544	0.2544	0.2551
TI ↑	setup_rising to CP	0.1400	0.1045	0.1047	0.1047

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.289e-06	3.918e-09
X8_P10	3.558e-06	3.680e-09
X17_P10	4.564e-06	3.918e-09
X33_P10	5.263e-06	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

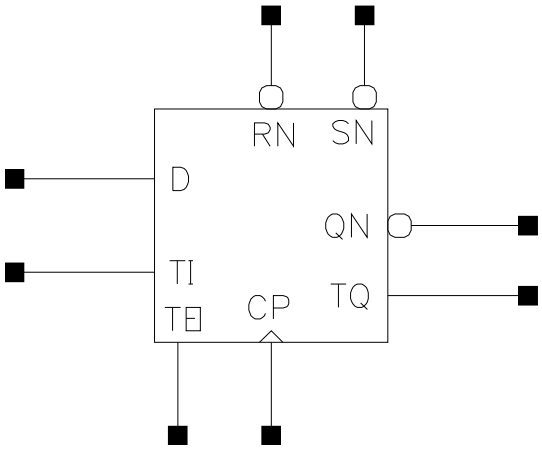
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.531e-03	3.562e-03	3.572e-03	3.577e-03
Clock 100Mhz Data 25Mhz	5.390e-03	5.407e-03	6.087e-03	6.603e-03
Clock 100Mhz Data 50Mhz	7.249e-03	7.251e-03	8.601e-03	9.629e-03
Clock = 0 Data 100Mhz	4.067e-03	3.807e-03	3.720e-03	3.677e-03
Clock = 1 Data 100Mhz	1.135e-03	5.890e-04	4.071e-04	3.162e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.352	5.2224
X17_P10	1.200	4.488	5.3856
X33_P10	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0005	0.0005	0.0005
RN	0.0007	0.0007	0.0007

SN	0.0012	0.0012	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.1247	0.1324	2.6699	1.3852
CP to QN ↑	0.0997	0.1041	4.7270	2.3885
CP to TQ ↓	0.0757	0.0756	8.9855	8.9956
CP to TQ ↑	0.1039	0.1040	27.2342	27.2335
RN to QN ↓	0.1400	0.1474	2.6697	1.3875
RN to QN ↑	0.1455	0.1524	4.7372	2.3962
RN to TQ ↓	0.1101	0.1097	9.8115	9.8153
RN to TQ ↑	0.1197	0.1198	27.2009	27.2256
SN to QN ↓	0.1512	0.1604	2.6909	1.3936
SN to TQ ↑	0.1279	0.1277	27.5007	27.5029
	X33_P10		**X33_P10**	
CP to QN ↓	0.1518		0.7481	
CP to QN ↑	0.1154		1.2233	
CP to TQ ↓	0.0758		9.0208	
CP to TQ ↑	0.1043		27.3182	
RN to QN ↓	0.1668		0.7482	
RN to QN ↑	0.1685		1.2262	
RN to TQ ↓	0.1098		9.8716	
RN to TQ ↑	0.1202		27.2824	
SN to QN ↓	0.1825		0.7491	
SN to TQ ↑	0.1280		27.6287	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.2167	0.2167	0.2167
CP ↑	min_pulse_width to CP	0.0560	0.0598	0.0646
D ↓	hold_rising to CP	-0.0508	-0.0508	-0.0508
D ↑	hold_rising to CP	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.1365	0.1368	0.1368
D ↑	setup_rising to CP	0.0690	0.0690	0.0690
RN ↓	min_pulse_width to RN	0.1306	0.1355	0.1480
RN ↑	non_seq_hold_rising to SN	-0.0530	-0.0530	-0.0530
RN ↑	non_seq_setup_rising to SN	0.1203	0.1203	0.1203
RN ↑	recovery_rising to CP	0.0562	0.0562	0.0562
RN ↑	removal_rising to CP	-0.0317	-0.0317	-0.0317
SN ↓	min_pulse_width to SN	0.1060	0.1086	0.1184
SN ↑	recovery_rising to CP	0.0226	0.0226	0.0226
SN ↑	removal_rising to CP	0.0530	0.0530	0.0530

TE ↓	hold_rising to CP	-0.0459	-0.0459	-0.0459
TE ↑	hold_rising to CP	-0.0530	-0.0530	-0.0530
TE ↓	setup_rising to CP	0.1344	0.1344	0.1344
TE ↑	setup_rising to CP	0.2787	0.2787	0.2756
TI ↓	hold_rising to CP	-0.1570	-0.1570	-0.1570
TI ↑	hold_rising to CP	-0.0547	-0.0547	-0.0547
TI ↓	setup_rising to CP	0.2648	0.2648	0.2648
TI ↑	setup_rising to CP	0.1096	0.1096	0.1096

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	4.222e-06	4.169e-09
X17_P10	4.808e-06	4.288e-09
X33_P10	5.794e-06	4.527e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

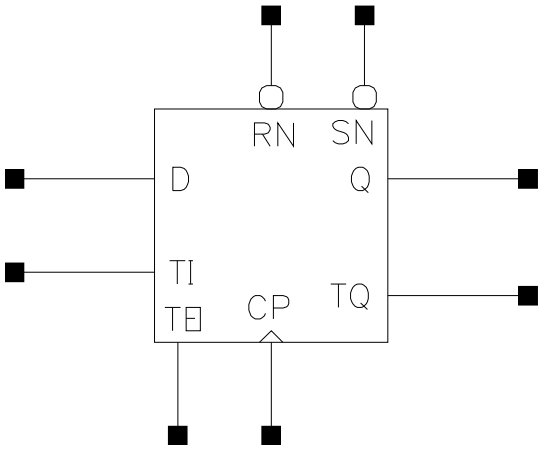
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.772e-03	3.772e-03	3.773e-03
Clock 100Mhz Data 25Mhz	5.727e-03	5.959e-03	6.545e-03
Clock 100Mhz Data 50Mhz	7.683e-03	8.146e-03	9.318e-03
Clock = 0 Data 100Mhz	3.699e-03	3.698e-03	3.698e-03
Clock = 1 Data 100Mhz	8.782e-05	8.786e-05	8.784e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.216	5.0592
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0008

SN	0.0012	0.0012	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0825	0.0923	2.8234	1.4791
CP to Q ↑	0.0988	0.1033	4.8432	2.4635
CP to TQ ↓	0.0881	0.1024	9.1263	9.2320
CP to TQ ↑	0.1117	0.1229	26.4354	26.5806
RN to Q ↓	0.1247	0.1440	3.3282	1.7556
RN to Q ↑	0.0916	0.1019	5.0518	2.5865
RN to TQ ↓	0.1321	0.1573	10.1008	10.3541
RN to TQ ↑	0.1134	0.1349	26.7056	26.8845
SN to Q ↑	0.1239	0.1341	5.0502	2.5871
SN to TQ ↑	0.1457	0.1671	26.7136	26.8841
	X33_P10		**X33_P10**	
CP to Q ↓	0.1170		0.8085	
CP to Q ↑	0.1166		1.2757	
CP to TQ ↓	0.1279		9.5620	
CP to TQ ↑	0.1439		26.8363	
RN to Q ↓	0.1917		0.9852	
RN to Q ↑	0.1293		1.3595	
RN to TQ ↓	0.2017		11.0507	
RN to TQ ↑	0.1767		27.2246	
SN to Q ↑	0.1613		1.3597	
SN to TQ ↑	0.2087		27.2318	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.2167	0.2167	0.2156
CP ↑	min_pulse_width to CP	0.0646	0.0743	0.1033
D ↓	hold_rising to CP	-0.0511	-0.0511	-0.0480
D ↑	hold_rising to CP	-0.0188	-0.0188	-0.0188
D ↓	setup_rising to CP	0.1368	0.1368	0.1343
D ↑	setup_rising to CP	0.0690	0.0690	0.0690
RN ↓	min_pulse_width to RN	0.1431	0.1724	0.2261
RN ↑	non_seq_hold_rising to SN	-0.0579	-0.0676	-0.0922
RN ↑	non_seq_setup_rising to SN	0.1127	0.1127	0.1482
RN ↑	recovery_rising to CP	0.0491	0.0517	0.0517
RN ↑	removal_rising to CP	-0.0246	-0.0246	-0.0246
SN ↓	min_pulse_width to SN	0.1184	0.1379	0.1721
SN ↑	recovery_rising to CP	0.0226	0.0226	0.0202
SN ↑	removal_rising to CP	0.0530	0.0530	0.0530

TE ↓	hold_rising to CP	-0.0459	-0.0462	-0.0462
TE ↑	hold_rising to CP	-0.0530	-0.0530	-0.0530
TE ↓	setup_rising to CP	0.1344	0.1344	0.1320
TE ↑	setup_rising to CP	0.2756	0.2756	0.2760
TI ↓	hold_rising to CP	-0.1515	-0.1520	-0.1520
TI ↑	hold_rising to CP	-0.0547	-0.0552	-0.0547
TI ↓	setup_rising to CP	0.2648	0.2648	0.2648
TI ↑	setup_rising to CP	0.1094	0.1094	0.1096

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P10	4.029e-06	4.046e-09
X17_P10	4.485e-06	4.165e-09
X33_P10	5.273e-06	4.403e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

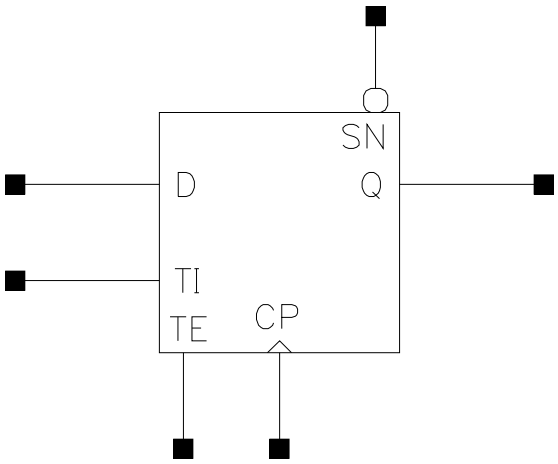
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.725e-03	3.725e-03	3.726e-03
Clock 100Mhz Data 25Mhz	5.592e-03	5.847e-03	6.480e-03
Clock 100Mhz Data 50Mhz	7.460e-03	7.968e-03	9.235e-03
Clock = 0 Data 100Mhz	3.696e-03	3.696e-03	3.695e-03
Clock = 1 Data 100Mhz	8.753e-05	8.755e-05	8.759e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0013	0.0014	0.0013	0.0013
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P10			

CP	0.0009			
D	0.0004			
SN	0.0013			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1479	0.0723	6.8857	2.8023
CP to Q ↑	0.1126	0.0907	10.4742	4.8153
SN to Q ↑	0.0845	0.0953	10.1764	4.8331
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
CP to Q ↓	0.1020	0.1072	1.3465	0.9343
CP to Q ↑	0.1297	0.1337	2.3703	1.6041
SN to Q ↑	0.1344	0.1384	2.3715	1.6058
	X33_P10		**X33_P10**	
CP to Q ↓	0.1111		0.7141	
CP to Q ↑	0.1362		1.2084	
SN to Q ↑	0.1408		1.2077	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.2185	0.2167	0.2161	0.2161
CP ↑	min_pulse_width to CP	0.1313	0.0539	0.0454	0.0454
D ↓	hold_rising to CP	-0.1311	-0.0557	-0.0608	-0.0608
D ↑	hold_rising to CP	-0.0605	-0.0170	-0.0195	-0.0195
D ↓	setup_rising to CP	0.2023	0.1392	0.1392	0.1392
D ↑	setup_rising to CP	0.0951	0.0487	0.0487	0.0487
SN ↓	min_pulse_width to SN	0.0735	0.0859	0.0833	0.0833
SN ↑	recovery_rising to CP	0.0177	0.0195	0.0195	0.0198
SN ↑	removal_rising to CP	0.0384	0.0505	0.0505	0.0505
TE ↓	hold_rising to CP	-0.0938	-0.0533	-0.0560	-0.0560
TE ↑	hold_rising to CP	-0.0796	-0.0481	-0.0512	-0.0512
TE ↓	setup_rising to CP	0.1733	0.1344	0.1344	0.1344
TE ↑	setup_rising to CP	0.3470	0.2809	0.2809	0.2809
TI ↓	hold_rising to CP	-0.2649	-0.1668	-0.1661	-0.1661
TI ↑	hold_rising to CP	-0.0902	-0.0498	-0.0498	-0.0498
TI ↓	setup_rising to CP	0.3541	0.2697	0.2697	0.2697
TI ↑	setup_rising to CP	0.1312	0.0908	0.0893	0.0899
		X33_P10			

CP ↓	min_pulse_width to CP	0.2161			
CP ↑	min_pulse_width to CP	0.0454			
D ↓	hold_rising to CP	-0.0608			
D ↑	hold_rising to CP	-0.0192			
D ↓	setup_rising to CP	0.1395			
D ↑	setup_rising to CP	0.0487			
SN ↓	min_pulse_width to SN	0.0833			
SN ↑	recovery_rising to CP	0.0202			
SN ↑	removal_rising to CP	0.0505			
TE ↓	hold_rising to CP	-0.0557			
TE ↑	hold_rising to CP	-0.0512			
TE ↓	setup_rising to CP	0.1344			
TE ↑	setup_rising to CP	0.2809			
TI ↓	hold_rising to CP	-0.1717			
TI ↑	hold_rising to CP	-0.0498			
TI ↓	setup_rising to CP	0.2697			
TI ↑	setup_rising to CP	0.0899			

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.364e-06	3.799e-09
X8_P10	3.713e-06	3.680e-09
X17_P10	4.684e-06	3.918e-09
X25_P10	5.204e-06	4.038e-09
X33_P10	5.717e-06	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	3.426e-03	3.515e-03	3.544e-03	3.559e-03
Clock 100Mhz Data 25Mhz	5.164e-03	5.296e-03	5.916e-03	6.211e-03
Clock 100Mhz Data 50Mhz	6.902e-03	7.078e-03	8.289e-03	8.864e-03
Clock = 0 Data 100Mhz	3.948e-03	3.760e-03	3.698e-03	3.667e-03
Clock = 1 Data 100Mhz	1.135e-03	5.926e-04	4.120e-04	3.217e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	3.567e-03			

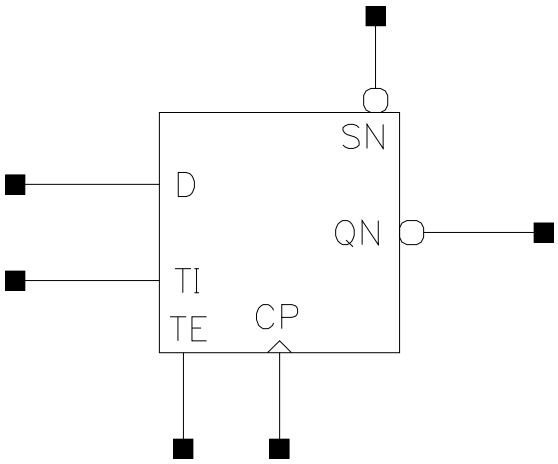
Clock 100Mhz Data 25Mhz	6.426e-03			
Clock 100Mhz Data 50Mhz	9.285e-03			
Clock = 0 Data 100Mhz	3.648e-03			
Clock = 1 Data 100Mhz	2.675e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0014	0.0013	0.0014	0.0013
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P10			

CP	0.0009			
D	0.0004			
SN	0.0013			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1277	0.1097	5.1806	2.6252
CP to QN ↑	0.1526	0.0828	10.0459	4.7187
SN to QN ↓	0.1018	0.1140	5.1618	2.6232
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
CP to QN ↓	0.1136	0.1199	1.3508	0.9385
CP to QN ↑	0.0990	0.1047	2.3724	1.6067
SN to QN ↓	0.1201	0.1266	1.3539	0.9378
	X33_P10		**X33_P10**	
CP to QN ↓	0.1245		0.7161	
CP to QN ↑	0.1082		1.2085	
SN to QN ↓	0.1313		0.7152	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.2185	0.2167	0.2167	0.2161
CP ↑	min_pulse_width to CP	0.0974	0.0453	0.0598	0.0598
D ↓	hold_rising to CP	-0.1329	-0.0578	-0.0557	-0.0556
D ↑	hold_rising to CP	-0.0605	-0.0195	-0.0139	-0.0139
D ↓	setup_rising to CP	0.2023	0.1392	0.1392	0.1392
D ↑	setup_rising to CP	0.0951	0.0487	0.0487	0.0487
SN ↓	min_pulse_width to SN	0.0735	0.0833	0.0908	0.0935
SN ↑	recovery_rising to CP	0.0177	0.0195	0.0195	0.0195
SN ↑	removal_rising to CP	0.0384	0.0505	0.0505	0.0505
TE ↓	hold_rising to CP	-0.0938	-0.0560	-0.0529	-0.0529
TE ↑	hold_rising to CP	-0.0796	-0.0481	-0.0481	-0.0481
TE ↓	setup_rising to CP	0.1703	0.1344	0.1344	0.1344
TE ↑	setup_rising to CP	0.3470	0.2809	0.2809	0.2809
TI ↓	hold_rising to CP	-0.2700	-0.1661	-0.1668	-0.1666
TI ↑	hold_rising to CP	-0.0902	-0.0498	-0.0498	-0.0498
TI ↓	setup_rising to CP	0.3541	0.2697	0.2697	0.2697
TI ↑	setup_rising to CP	0.1318	0.0893	0.0908	0.0908
		X33_P10			

CP ↓	min_pulse_width to CP	0.2161			
CP ↑	min_pulse_width to CP	0.0636			
D ↓	hold_rising to CP	-0.0556			
D ↑	hold_rising to CP	-0.0139			
D ↓	setup_rising to CP	0.1392			
D ↑	setup_rising to CP	0.0487			
SN ↓	min_pulse_width to SN	0.0935			
SN ↑	recovery_rising to CP	0.0198			
SN ↑	removal_rising to CP	0.0505			
TE ↓	hold_rising to CP	-0.0529			
TE ↑	hold_rising to CP	-0.0481			
TE ↓	setup_rising to CP	0.1344			
TE ↑	setup_rising to CP	0.2809			
TI ↓	hold_rising to CP	-0.1666			
TI ↑	hold_rising to CP	-0.0498			
TI ↓	setup_rising to CP	0.2697			
TI ↑	setup_rising to CP	0.0893			

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.204e-06	3.799e-09
X8_P10	3.434e-06	3.680e-09
X17_P10	4.458e-06	3.918e-09
X25_P10	4.803e-06	4.038e-09
X33_P10	5.154e-06	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	3.421e-03	3.505e-03	3.529e-03	3.541e-03
Clock 100Mhz Data 25Mhz	5.118e-03	5.278e-03	5.873e-03	6.167e-03
Clock 100Mhz Data 50Mhz	6.814e-03	7.051e-03	8.218e-03	8.792e-03
Clock = 0 Data 100Mhz	3.948e-03	3.764e-03	3.699e-03	3.668e-03
Clock = 1 Data 100Mhz	1.135e-03	6.047e-04	4.282e-04	3.399e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	3.549e-03			

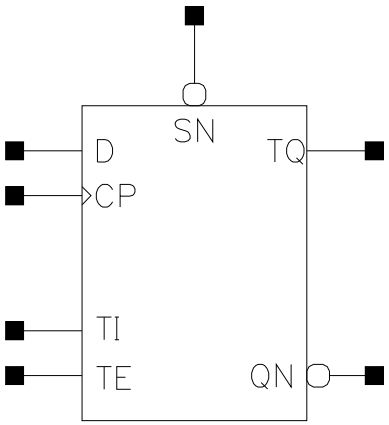
Clock 100Mhz Data 25Mhz	6.387e-03			
Clock 100Mhz Data 50Mhz	9.225e-03			
Clock = 0 Data 100Mhz	3.649e-03			
Clock = 1 Data 100Mhz	2.870e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.216	5.0592
X8_P10	1.200	4.080	4.8960
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0014	0.0016	0.0014	0.0015
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1482	0.1159	5.1651	2.6308
CP to QN ↑	0.2012	0.0947	9.8764	4.7878
CP to TQ ↓	0.1440	0.0652	8.1878	6.4715
CP to TQ ↑	0.1131	0.0868	14.2130	13.8334
SN to QN ↓	0.0961	0.0990	5.1555	2.6308
SN to TQ ↑	0.0662	0.0685	13.9416	13.8858
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.1145	0.1258	1.3782	0.7080
CP to QN ↑	0.1070	0.1171	2.3828	1.2119
CP to TQ ↓	0.0819	0.0818	6.7702	6.7686
CP to TQ ↑	0.0977	0.0977	13.9226	13.9509
SN to QN ↓	0.0992	0.1105	1.3777	0.7070
SN to TQ ↑	0.0815	0.0815	13.9273	13.9596

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.2185	0.2167	0.2185	0.2167
CP ↑	min_pulse_width to CP	0.1372	0.0502	0.0646	0.0695
D ↓	hold_rising to CP	-0.1311	-0.0582	-0.0557	-0.0557
D ↑	hold_rising to CP	-0.0605	-0.0170	-0.0139	-0.0139
D ↓	setup_rising to CP	0.2023	0.1392	0.1392	0.1392
D ↑	setup_rising to CP	0.0972	0.0487	0.0487	0.0487
SN ↓	min_pulse_width to SN	0.0664	0.0686	0.0713	0.0740
SN ↑	recovery_rising to CP	0.0177	0.0202	0.0198	0.0198
SN ↑	removal_rising to CP	0.0384	0.0505	0.0505	0.0505
TE ↓	hold_rising to CP	-0.0938	-0.0560	-0.0508	-0.0508
TE ↑	hold_rising to CP	-0.0796	-0.0481	-0.0481	-0.0481
TE ↓	setup_rising to CP	0.1733	0.1344	0.1344	0.1344
TE ↑	setup_rising to CP	0.3496	0.2809	0.2809	0.2805
TI ↓	hold_rising to CP	-0.2649	-0.1666	-0.1612	-0.1612
TI ↑	hold_rising to CP	-0.0902	-0.0498	-0.0498	-0.0498
TI ↓	setup_rising to CP	0.3541	0.2697	0.2697	0.2697
TI ↑	setup_rising to CP	0.1312	0.0908	0.0908	0.0908

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.591e-06	4.038e-09
X8_P10	3.816e-06	3.918e-09
X17_P10	4.841e-06	4.157e-09
X33_P10	5.536e-06	4.395e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

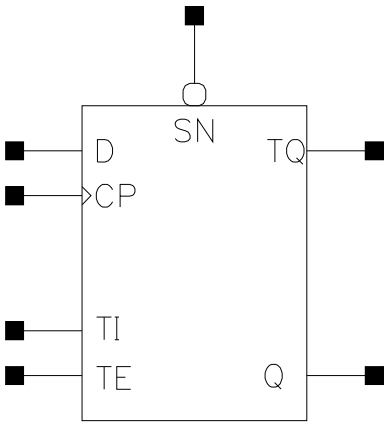
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.424e-03	3.516e-03	3.547e-03	3.562e-03
Clock 100Mhz Data 25Mhz	5.358e-03	5.476e-03	6.003e-03	6.517e-03
Clock 100Mhz Data 50Mhz	7.291e-03	7.437e-03	8.460e-03	9.472e-03
Clock = 0 Data 100Mhz	3.957e-03	3.768e-03	3.706e-03	3.674e-03
Clock = 1 Data 100Mhz	1.135e-03	5.889e-04	4.070e-04	3.161e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.944	4.7328
X17_P10	1.200	4.216	5.0592
X33_P10	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0013	0.0013	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1702	0.0775	7.1279	2.8680
CP to Q ↑	0.1203	0.0938	10.5485	4.8757
CP to TQ ↓	0.1713	0.0833	10.3762	7.4529
CP to TQ ↑	0.1193	0.1056	14.3100	20.4427
SN to Q ↑	0.0702	0.0991	10.2209	4.8821
SN to TQ ↑	0.0693	0.1129	13.9763	20.4272
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.1046	0.1135	1.3845	0.7258
CP to Q ↑	0.1318	0.1380	2.3812	1.2123
CP to TQ ↓	0.1098	0.1225	7.0215	7.1180
CP to TQ ↑	0.1414	0.1518	19.8403	19.9224
SN to Q ↑	0.1364	0.1425	2.3791	1.2114
SN to TQ ↑	0.1460	0.1563	19.8440	19.9195

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.2166	0.2167	0.2161	0.2161
CP ↑	min_pulse_width to CP	0.1506	0.0587	0.0454	0.0454
D ↓	hold_rising to CP	-0.1333	-0.0557	-0.0578	-0.0608
D ↑	hold_rising to CP	-0.0601	-0.0170	-0.0195	-0.0191
D ↓	setup_rising to CP	0.2023	0.1392	0.1392	0.1395
D ↑	setup_rising to CP	0.0951	0.0487	0.0487	0.0487
SN ↓	min_pulse_width to SN	0.0610	0.0957	0.0833	0.0833
SN ↑	recovery_rising to CP	0.0177	0.0195	0.0198	0.0202
SN ↑	removal_rising to CP	0.0384	0.0505	0.0505	0.0505
TE ↓	hold_rising to CP	-0.0960	-0.0508	-0.0557	-0.0557
TE ↑	hold_rising to CP	-0.0821	-0.0481	-0.0512	-0.0537
TE ↓	setup_rising to CP	0.1710	0.1344	0.1344	0.1344
TE ↑	setup_rising to CP	0.3470	0.2809	0.2809	0.2812
TI ↓	hold_rising to CP	-0.2649	-0.1612	-0.1661	-0.1717
TI ↑	hold_rising to CP	-0.0917	-0.0498	-0.0498	-0.0498
TI ↓	setup_rising to CP	0.3485	0.2697	0.2697	0.2697
TI ↑	setup_rising to CP	0.1312	0.0908	0.0899	0.0899

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	3.598e-06	3.918e-09
X8_P10	3.944e-06	3.799e-09
X17_P10	4.898e-06	4.038e-09
X33_P10	5.926e-06	4.276e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

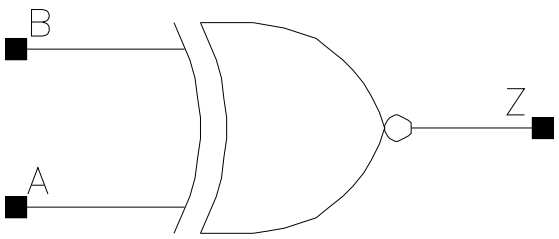
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.427e-03	3.523e-03	3.554e-03	3.569e-03
Clock 100Mhz Data 25Mhz	5.297e-03	5.436e-03	6.088e-03	6.615e-03
Clock 100Mhz Data 50Mhz	7.167e-03	7.349e-03	8.623e-03	9.661e-03
Clock = 0 Data 100Mhz	3.958e-03	3.765e-03	3.701e-03	3.668e-03
Clock = 1 Data 100Mhz	1.135e-03	5.890e-04	4.071e-04	3.162e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P10	X8_P10	X17_P10	X25_P10
A	0.0016	0.0006	0.0009	0.0014
B	0.0015	0.0014	0.0018	0.0024
	X33_P10			
A	0.0016			
B	0.0027			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X8_P10**	**X6_P10**	**X8_P10**
A to Z ↓	0.0313	0.0772	5.2183	2.8643
A to Z ↑	0.0348	0.0664	7.9153	4.9802
B to Z ↓	0.0298	0.0529	5.2088	2.8476
B to Z ↑	0.0341	0.0483	7.9274	4.9669
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
A to Z ↓	0.0721	0.0724	1.4161	0.9765
A to Z ↑	0.0599	0.0609	2.4317	1.6190

B to Z ↓	0.0541	0.0533	1.4127	0.9738
B to Z ↑	0.0472	0.0464	2.4283	1.6166
	X33_P10		**X33_P10**	
A to Z ↓	0.0675		0.7332	
A to Z ↑	0.0581		1.2155	
B to Z ↓	0.0506		0.7327	
B to Z ↑	0.0452		1.2145	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P10	1.464e-06	1.179e-09
X8_P10	2.158e-06	1.536e-09
X17_P10	3.235e-06	1.655e-09
X25_P10	5.134e-06	2.370e-09
X33_P10	6.546e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	2.135e-03	3.872e-03	5.365e-03	8.697e-03
B to Z	2.017e-03	2.640e-03	3.961e-03	6.301e-03
	X33_P10			
A to Z	1.050e-02			
B to Z	7.836e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

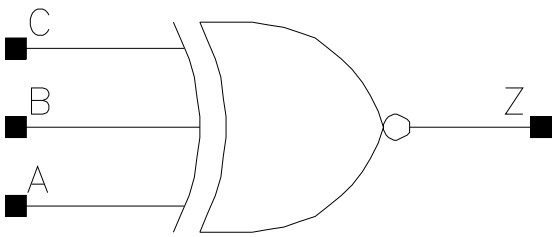
Pin Cycle (vdds)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	-7.583e-07	-1.231e-07	-1.260e-07	-5.728e-07
B to Z	9.245e-06	-1.735e-07	-1.695e-08	-4.634e-07
	X33_P10			
A to Z	-5.302e-07			
B to Z	-6.463e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	2.176	2.6112
X16_P10	1.200	2.720	3.2640
X25_P10	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X16_P10	X25_P10
A	0.0027	0.0023	0.0028	0.0041
B	0.0030	0.0021	0.0028	0.0038
C	0.0019	0.0006	0.0006	0.0007

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0539	0.0940	6.3003	3.0572
A to Z ↑	0.0510	0.0844	11.8190	4.9322
B to Z ↓	0.0545	0.0937	6.2969	3.0549
B to Z ↑	0.0510	0.0840	11.8066	4.9360
C to Z ↓	0.0528	0.1213	6.2909	3.0550
C to Z ↑	0.0487	0.1106	11.7999	4.9348
	X16_P10	**X25_P10**	**X16_P10**	**X25_P10**
A to Z ↓	0.0925	0.0918	1.5727	1.0032
A to Z ↑	0.0896	0.0885	2.5871	1.6247
B to Z ↓	0.0925	0.0931	1.5714	1.0029

B to Z ↑	0.0894	0.0901	2.5887	1.6259
C to Z ↓	0.1257	0.1323	1.5714	1.0021
C to Z ↑	0.1210	0.1284	2.5888	1.6249

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	1.538e-06	2.132e-09
X8_P10	1.785e-06	2.251e-09
X16_P10	2.862e-06	2.727e-09
X25_P10	4.028e-06	3.799e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	2.369e-03	3.069e-03	4.891e-03	7.306e-03
B to Z	2.210e-03	3.000e-03	4.809e-03	7.237e-03
C to Z	2.154e-03	4.608e-03	6.756e-03	1.013e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

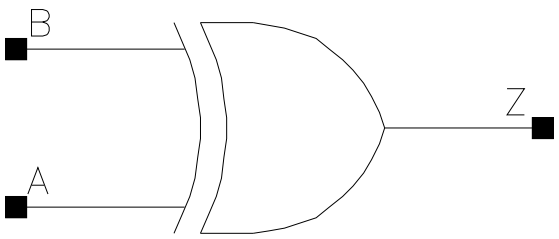
Pin Cycle (vdds)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	-1.914e-05	-6.172e-06	-7.711e-06	-1.264e-05
B to Z	1.902e-05	3.651e-06	9.534e-06	1.685e-05
C to Z	2.490e-05	1.251e-05	1.949e-05	2.645e-05

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.224	1.4688
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.224	1.4688
X16_P10	1.200	1.360	1.6320
X25_P10	1.200	2.176	2.6112
X31_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X16_P10
A	0.0007	0.0015	0.0010	0.0011
B	0.0012	0.0014	0.0014	0.0016
	X25_P10	X31_P10		
A	0.0014	0.0018		
B	0.0025	0.0032		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0690	0.0342	5.2726	3.9483
A to Z ↑	0.0624	0.0350	9.7461	10.5137
B to Z ↓	0.0487	0.0335	5.2531	3.9680
B to Z ↑	0.0478	0.0334	9.7250	10.5033
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0608	0.0627	2.7819	1.4436

A to Z ↑	0.0527	0.0549	4.8517	2.4442
B to Z ↓	0.0466	0.0476	2.7750	1.4419
B to Z ↑	0.0429	0.0446	4.8510	2.4445
	X25_P10	**X31_P10**	**X25_P10**	**X31_P10**
A to Z ↓	0.0676	0.0624	0.9650	0.7798
A to Z ↑	0.0589	0.0550	1.6159	1.3032
B to Z ↓	0.0507	0.0470	0.9648	0.7791
B to Z ↑	0.0446	0.0419	1.6146	1.3021

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	1.786e-06	1.417e-09
X6_P10	1.560e-06	1.179e-09
X8_P10	2.620e-06	1.417e-09
X16_P10	3.540e-06	1.536e-09
X25_P10	5.030e-06	2.251e-09
X31_P10	6.348e-06	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	2.962e-03	2.113e-03	3.518e-03	4.971e-03
B to Z	2.244e-03	1.957e-03	2.857e-03	4.074e-03
	X25_P10	X31_P10		
A to Z	7.791e-03	9.485e-03		
B to Z	5.390e-03	6.495e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

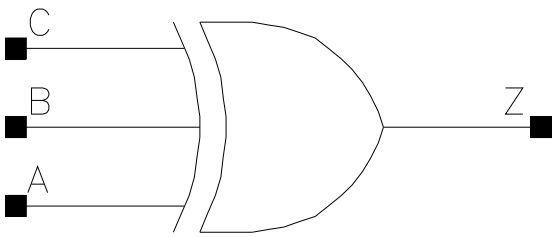
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	-1.987e-07	-2.936e-06	-2.112e-07	-1.840e-07
B to Z	-1.452e-07	8.297e-06	-2.066e-07	-1.791e-07
	X25_P10	X31_P10		
A to Z	-3.451e-07	-2.173e-07		
B to Z	-5.990e-07	-4.457e-07		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X24_P10	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X24_P10
A	0.0022	0.0023	0.0028	0.0050
B	0.0023	0.0021	0.0026	0.0042
C	0.0007	0.0016	0.0022	0.0033

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0543	0.0939	6.5773	3.0543
A to Z ↑	0.0512	0.0842	12.8829	4.9303
B to Z ↓	0.0546	0.0935	6.5763	3.0531
B to Z ↑	0.0516	0.0839	12.8703	4.9299
C to Z ↓	0.0910	0.0905	6.5647	3.0530
C to Z ↑	0.0880	0.0805	12.8580	4.9333
	X17_P10	**X24_P10**	**X17_P10**	**X24_P10**
A to Z ↓	0.0838	0.0975	1.4554	1.0546
A to Z ↑	0.0814	0.0716	2.3987	1.6269
B to Z ↓	0.0834	0.0975	1.4542	1.0533

B to Z ↑	0.0810	0.0712	2.3992	1.6260
C to Z ↓	0.0815	0.0939	1.4539	1.0521
C to Z ↑	0.0790	0.0694	2.4005	1.6266

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P10	1.794e-06	2.132e-09
X8_P10	1.461e-06	2.013e-09
X17_P10	2.468e-06	2.132e-09
X24_P10	4.417e-06	3.680e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	2.140e-03	3.087e-03	4.687e-03	8.061e-03
B to Z	2.106e-03	2.985e-03	4.541e-03	7.786e-03
C to Z	4.302e-03	2.885e-03	4.495e-03	7.597e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	-7.880e-06	-8.354e-06	-1.105e-05	-3.130e-05
B to Z	7.759e-06	6.675e-06	1.364e-05	1.062e-05
C to Z	2.225e-05	1.132e-05	2.101e-05	4.401e-05

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