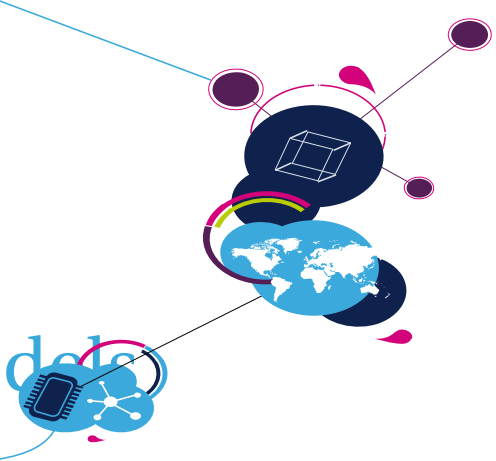
cmos028fdsoi Technology

PDC vs MC Noise report for EGLVT models

DK1.2_RF_mmW



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General information on PDC vs MC Noise report for EGLVT models

- Maximum supply voltage is 1.8 V.
- Validity domain is defined as follows:
  - ✔ Drawn gate length varies from 150nm to 10um.
  - ✔ Drawn transistor width varies from 0.16um to 10um.
  - ✔ Device temperature varies from -40 °C to 125 °C.

Output parameters definitions

- Model(s): eglvtnfet_acc, eglvtpfet_acc

eglvtnfet_acc
Electrical characteristics per geometry

eglvtnfet_acc @ w=1.5e-6, l=0.15e-6, pre_layout_local=1, nf=2, sa=1.2e-07, sb=1.2e-07, devtype=PCELLwoWPE, as=9e-14, ad=9e-14, ps=1.74e-06, pd=1.74e-06, vbs=0, vdd=1.8, temp=25

	TT_Noisedev=4	TT_Noisedev=0	TT_Noisedev=2	PRO_MC_PARAM_TT_1_MC_AVG-3S	PRO_MC_PARAM_TT_1_MC_AVG	PRO_MC_PARAM_TT_1_MC_AVG+3S
logSi2@1Hz [log10(A²/Hz)]	-17.28	-15.85	-14.43	-17.28	-15.85	-14.43
logSi2ovId2@1Hz [log10(1/Hz)]	-8.67	-7.25	-5.83	-8.68	-7.25	-5.82
logSv2@1Hz [log10(V²/Hz)]	-10.55	-9.12	-7.7	-10.55	-9.12	-7.7

eglvtpfet_acc
Electrical characteristics per geometry

eglvtpfet_acc @ w=1.5e-6, l=0.15e-6, pre_layout_local=1, nf=2, sa=1.2e-07, sb=1.2e-07, devtype=PCELLwoWPE, as=9e-14, ad=9e-14, ps=1.74e-06, pd=1.74e-06, vbs=1.8, vdd=1.8, temp=25

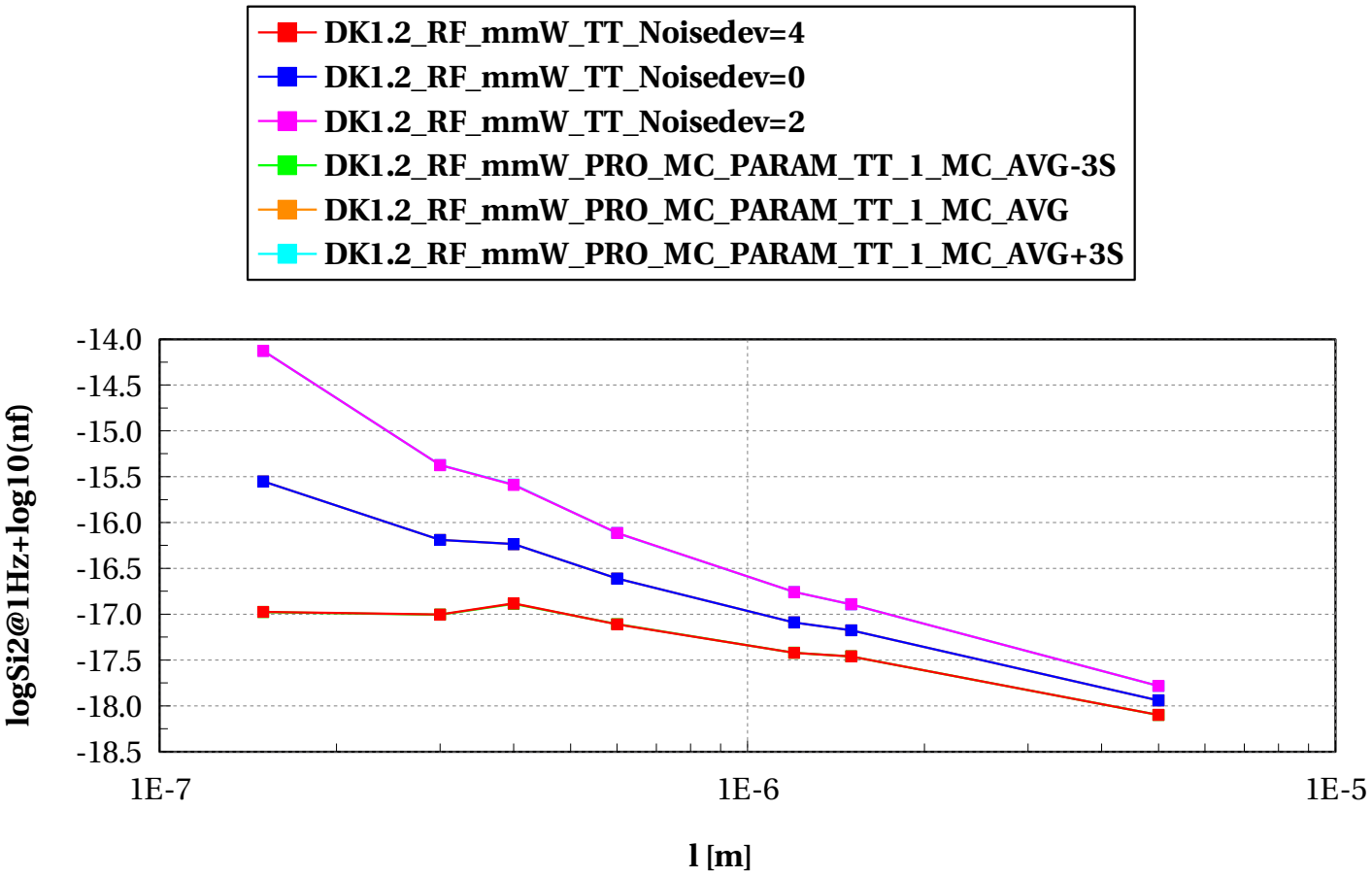
	TT_Noisedev=4	TT_Noisedev=0	TT_Noisedev=2	PRO_MC_PARAM_TT_1_MC_AVG-3S	PRO_MC_PARAM_TT_1_MC_AVG	PRO_MC_PARAM_TT_1_MC_AVG+3S
logSi2@1Hz [log10(A²/Hz)]	-17.35	-16.3	-15.26	-17.35	-16.3	-15.26
logSi2ovId2@1Hz [log10(1/Hz)]	-7.95	-6.91	-5.86	-7.95	-6.91	-5.86
logSv2@1Hz [log10(V²/Hz)]	-9.68	-8.64	-7.6	-9.69	-8.64	-7.6

eglvtnfet_acc
Electrical characteristics scaling

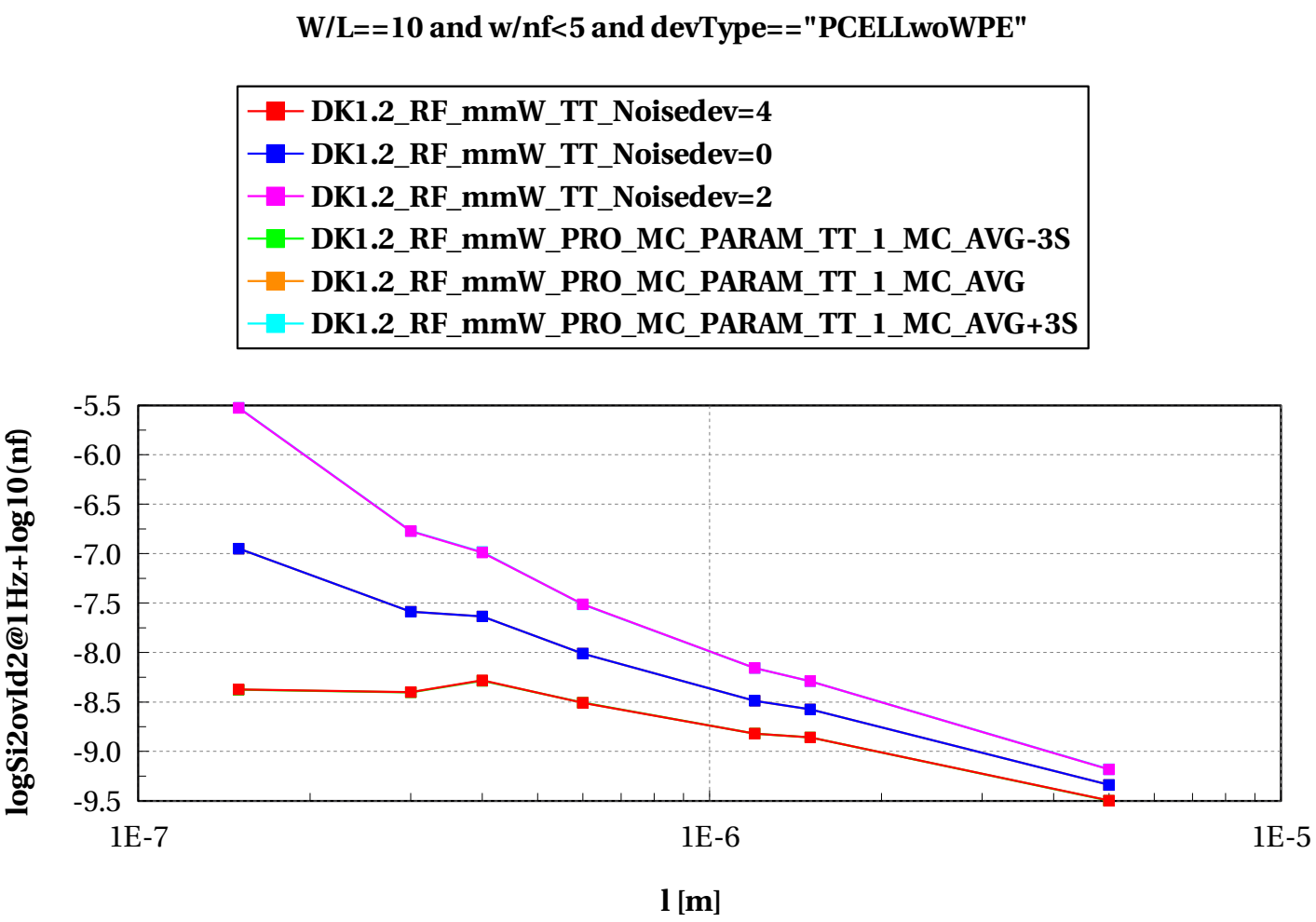
Scaling versus Length @ W/L=10&&W/nf<5um

eglvtnfet_acc, logSi2@1Hz+log10(nf) vs l [m]

W/L==10 and w/nf<5 and devType=="PCELLwoWPE"

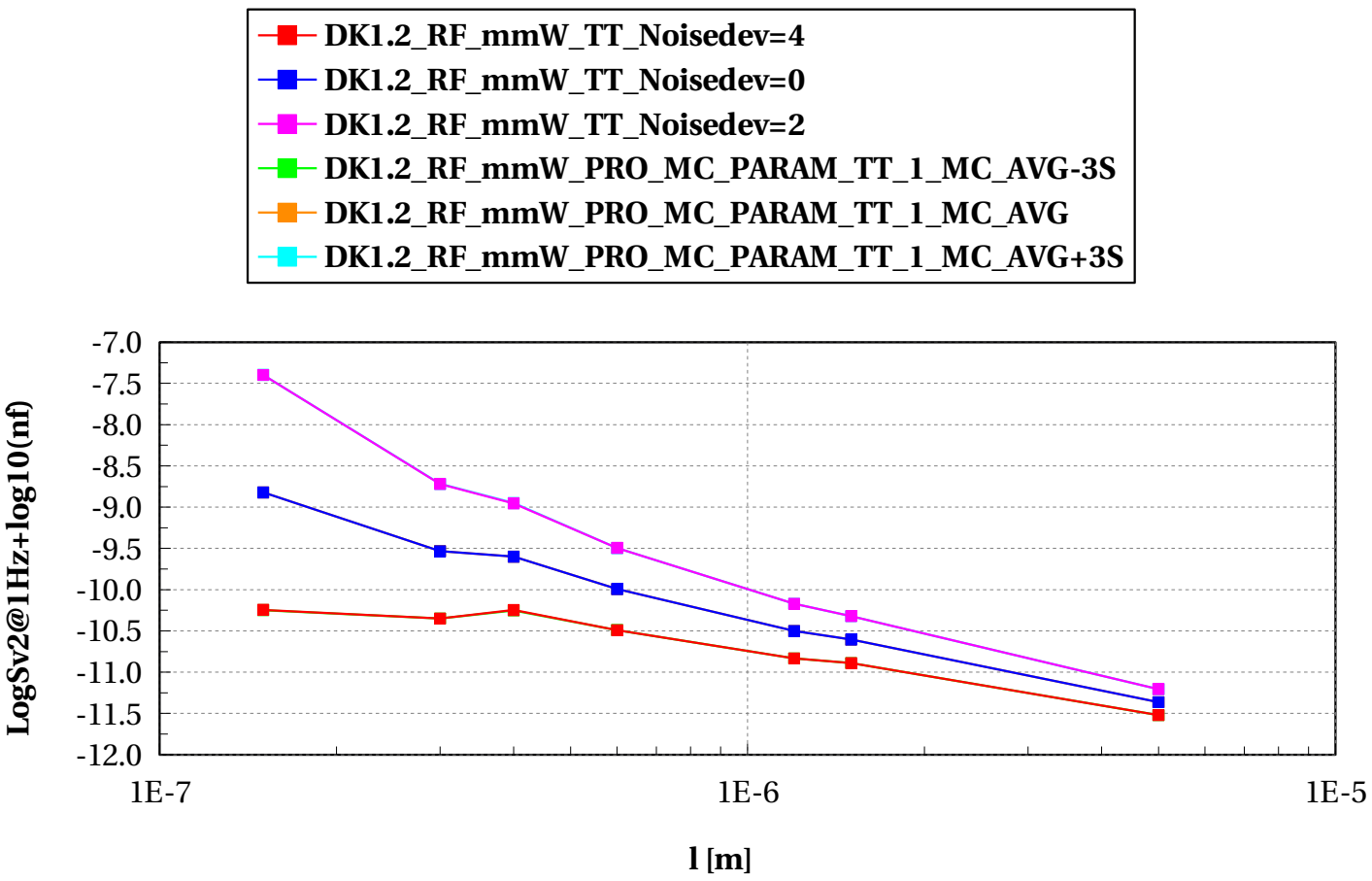


eglvtnfet_acc, logSi2ovId2@1Hz+log10(nf) vs l [m]



eglvtnfet_acc, LogSv2@1Hz+log10(nf) vs l [m]

W/L==10 and w/nf<5 and devType=="PCELLwoWPE"

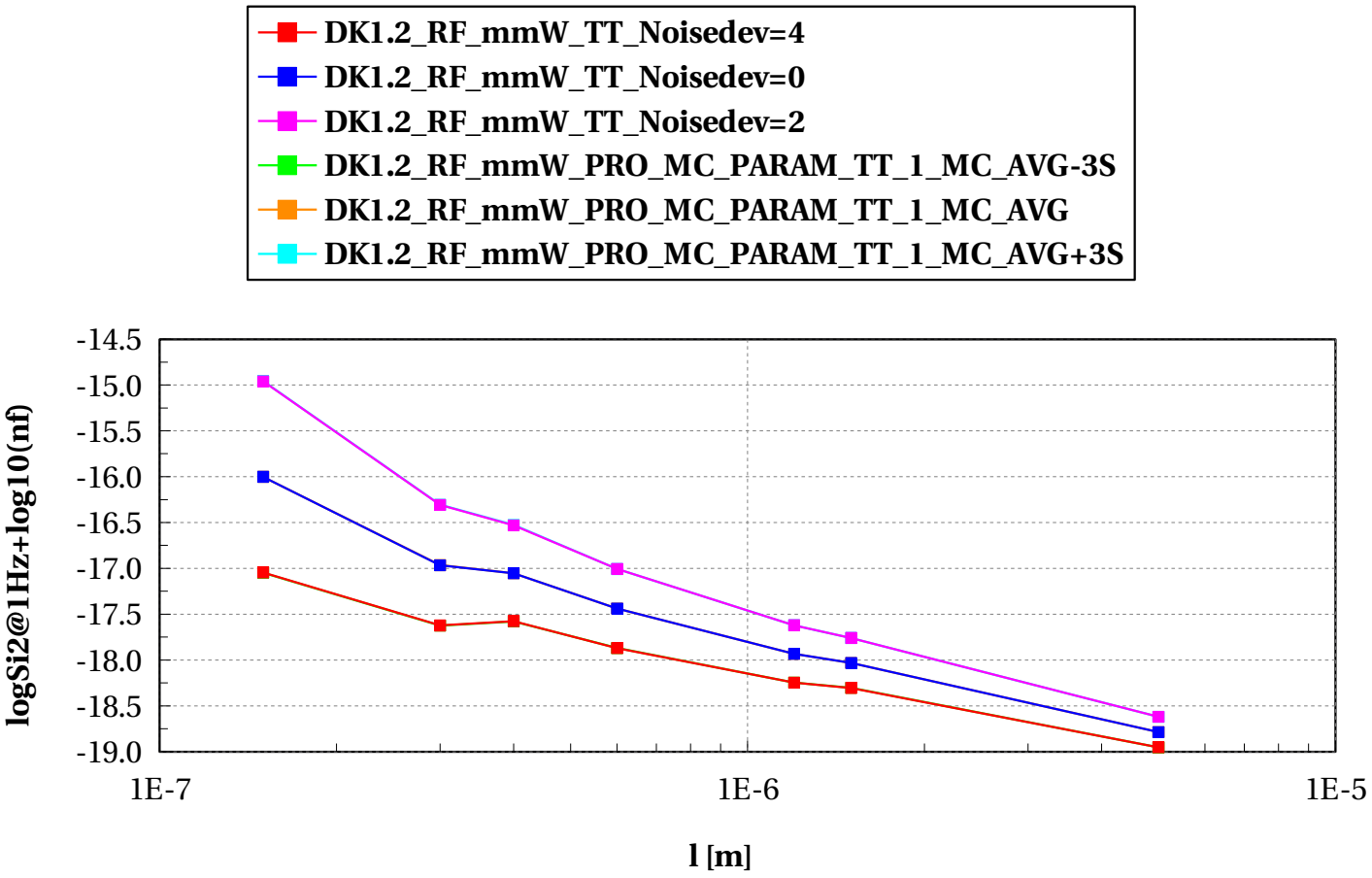


eglvtpfet_acc
Electrical characteristics scaling

Scaling versus Length @ W/L=10&&W/nf<5um

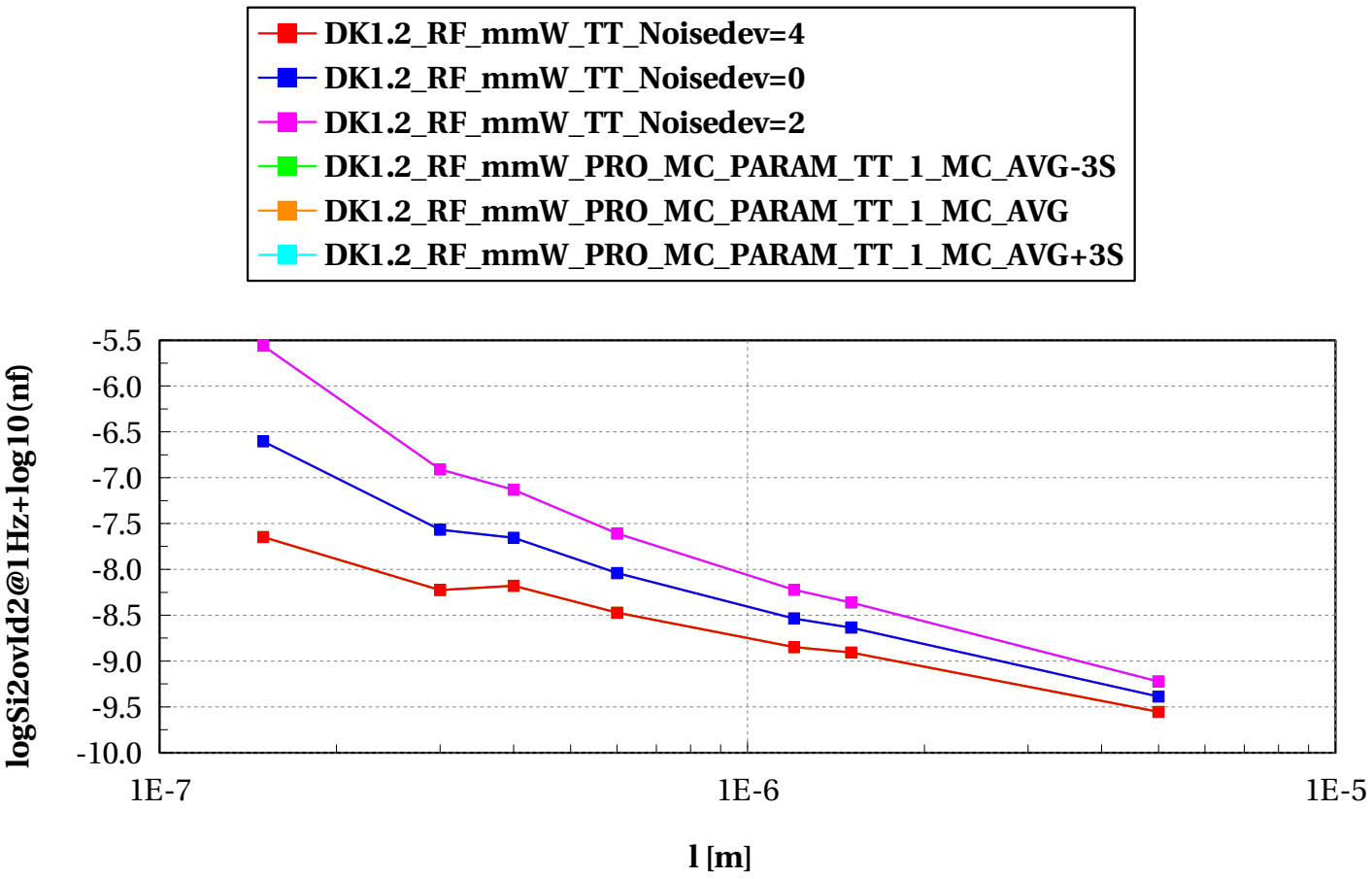
eglvtpfet_acc, logSi2@1Hz+log10(nf) vs l [m]

W/L==10 and w/nf<5 and devType=="PCELLwoWPE"



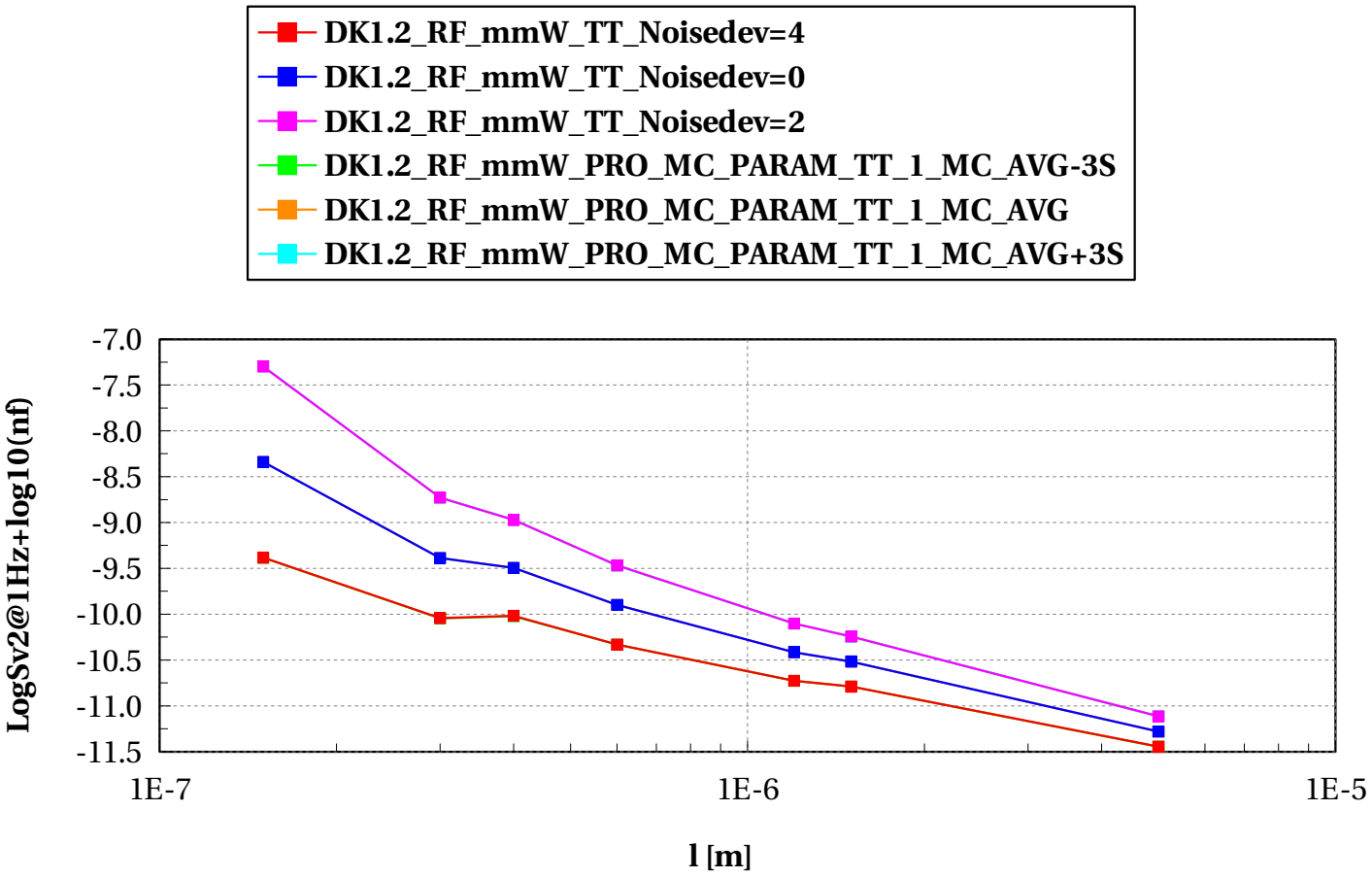
eglvtpfet_acc, logSi2ovId2@1Hz+log10(nf) vs l [m]

W/L==10 and w/nf<5 and devType=="PCELLwoWPE"



eglvtpfet_acc, LogSv2@1Hz+log10(nf) vs l [m]

W/L==10 and w/nf<5 and devType=="PCELLwoWPE"



Annex

Conditions of simulations

The simulations were done with SBenchLSF Alpha using Eldo simulator 2018.3.

- Model eglvtnfet_acc (DK1.2_RF_mmW)
  - ✔ Input Parameters
    - ✘ ams_release = 2018.3
    - ✘ mc_runs = 500
    - ✘ iana = 5e-6 A
    - ✘ temp = 25 °C
    - ✘ mc_sens = 0
    - ✘ f_ext = 100k Hz
    - ✘ sbenchlsf_release = Alpha
    - ✘ vbs = 0 V
    - ✘ model_version = 1.2.e
    - ✘ vds_ana = Vdd/4 V
    - ✘ mc_nsigma = 3
    - ✘ vdd = 1.8 V
  - ✔ Sweep Parameters
  - ✔ Extra parameters

- ✘ eglvt_dev = 0

● Model eglvtpfet_acc (DK1.2_RF_mmW)

- ✔ Input Parameters
  - ✘ ams_release = 2018.3
  - ✘ mc_runs = 500
  - ✘ iana = 2e-6 A
  - ✘ temp = 25 °C
  - ✘ mc_sens = 0
  - ✘ f_ext = 100k Hz
  - ✘ sbenchlsf_release = Alpha
  - ✘ vbs = 1.8 V
  - ✘ model_version = 1.2.e
  - ✘ vds_ana = Vdd/4 V
  - ✘ mc_nsigma = 3
  - ✘ vdd = 1.8 V
- ✔ Sweep Parameters
- ✔ Extra parameters
  - ✘ eglvt_dev = 0