C28SOI_SC_12_CORE_LR
Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells

Overview

- C28SOI_SC_12_CORE_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

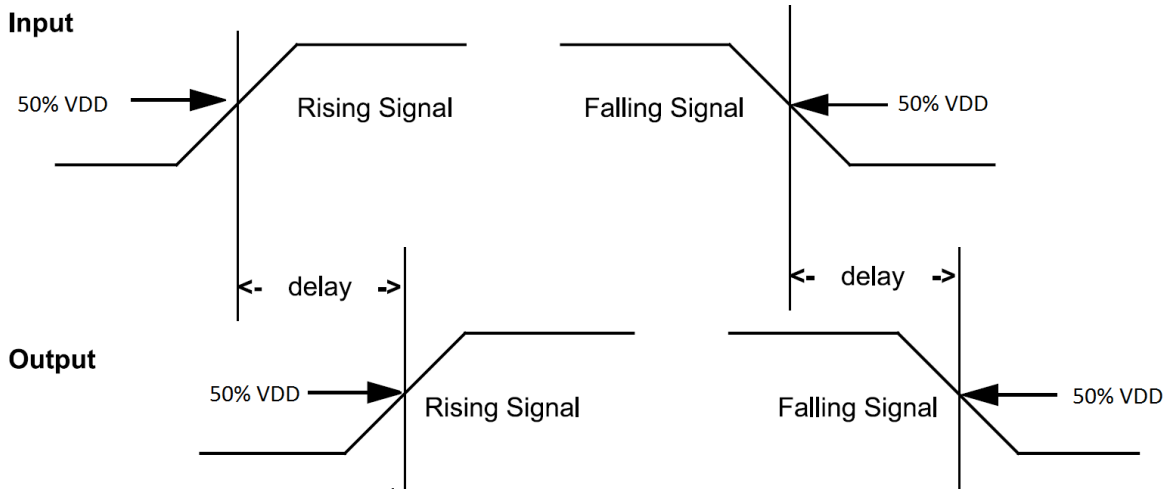


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

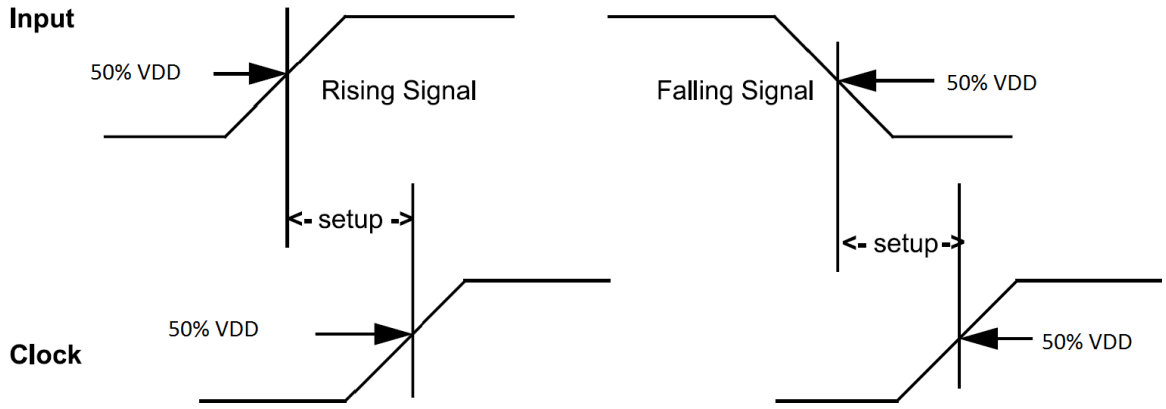


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

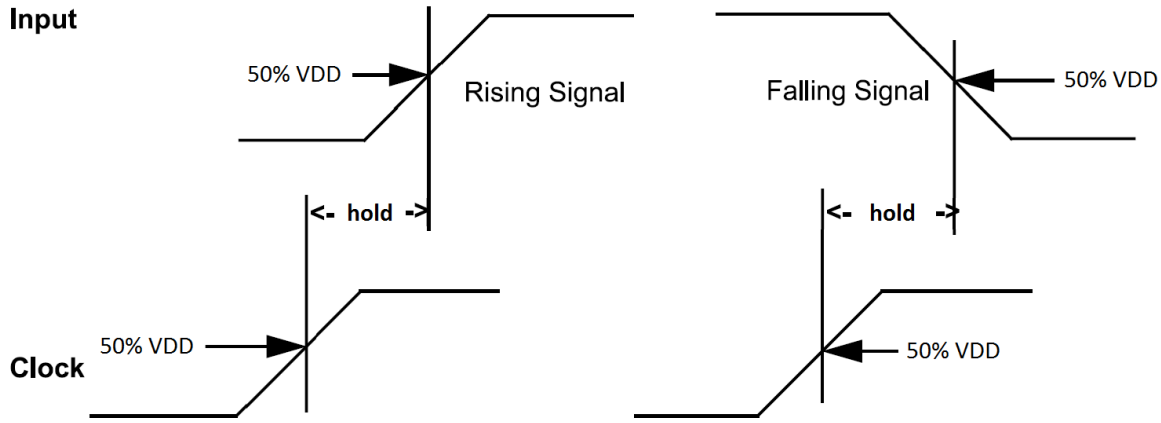


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

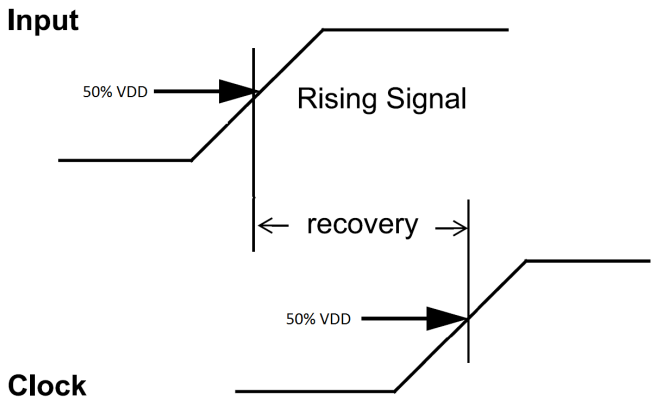


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

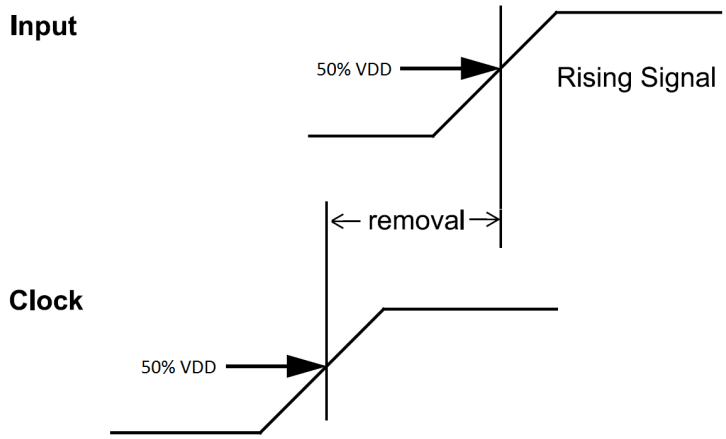


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

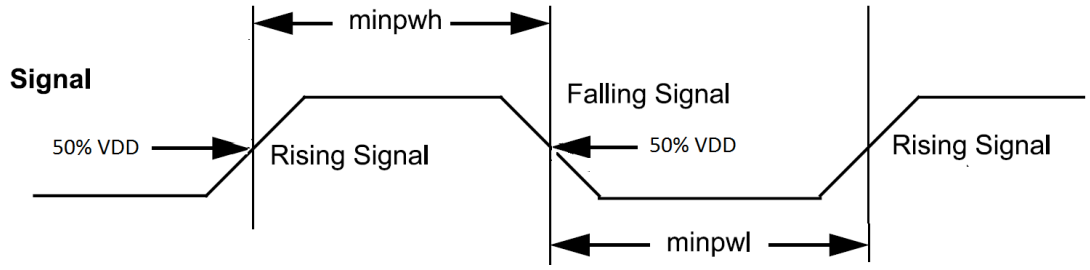


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

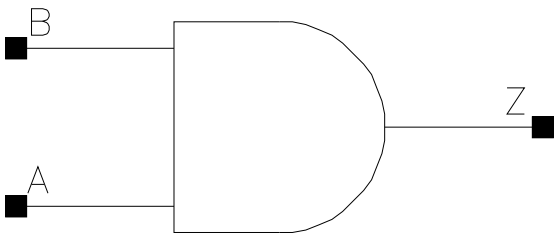
The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description	Logical Symbol
2 input AND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X25_P0	1.200	1.088	1.3056
X33_P0	1.200	1.360	1.6320
X42_P0	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0007	0.0010	0.0014	0.0018
B	0.0006	0.0009	0.0014	0.0018
	X42_P0			
A	0.0017			
B	0.0018			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0364	0.0299	2.2663	1.1499
A to Z ↑	0.0298	0.0271	3.9230	1.8998
B to Z ↓	0.0348	0.0285	2.2654	1.1490
B to Z ↑	0.0307	0.0277	3.9182	1.9018
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0308	0.0297	0.7636	0.5678

A to Z ↑	0.0269	0.0271	1.2550	0.9477
B to Z ↓	0.0295	0.0276	0.7636	0.5665
B to Z ↑	0.0275	0.0271	1.2560	0.9471
	X42_P0		**X42_P0**	
A to Z ↓	0.0320		0.4616	
A to Z ↑	0.0294		0.7592	
B to Z ↓	0.0299		0.4606	
B to Z ↑	0.0294		0.7592	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	6.512e-06	8.218e-10
X16_P0	1.301e-05	9.409e-10
X25_P0	1.869e-05	1.298e-09
X33_P0	2.532e-05	1.536e-09
X42_P0	2.897e-05	1.655e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	1.291e-05	2.536e-05	3.928e-05	9.568e-05
B (output stable)	1.739e-05	3.101e-05	4.873e-05	2.304e-04
A to Z	1.780e-03	2.892e-03	4.471e-03	5.827e-03
B to Z	1.696e-03	2.742e-03	4.238e-03	5.304e-03
	X42_P0			
A (output stable)	9.629e-05			
B (output stable)	2.290e-04			
A to Z	7.013e-03			
B to Z	6.475e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

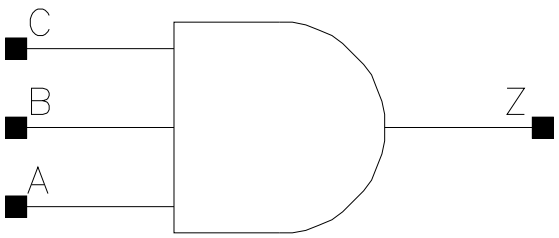
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	5.440e-08	4.671e-08	2.730e-08	1.620e-08
B (output stable)	6.960e-08	3.783e-08	1.924e-08	6.470e-09
A to Z	-8.990e-08	-1.191e-07	-4.515e-07	1.456e-07
B to Z	-5.090e-08	-7.194e-08	-2.601e-07	-2.850e-07
	X42_P0			
A (output stable)	1.730e-08			
B (output stable)	7.910e-09			
A to Z	-1.058e-06			
B to Z	-1.569e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X25_P0	1.200	1.360	1.6320
X33_P0	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0006	0.0009	0.0016	0.0018
B	0.0005	0.0009	0.0014	0.0017
C	0.0006	0.0009	0.0013	0.0016

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0393	0.0328	2.2969	1.1237
A to Z ↑	0.0390	0.0351	3.9571	1.8854
B to Z ↓	0.0381	0.0316	2.2975	1.1225
B to Z ↑	0.0394	0.0357	3.9567	1.8859
C to Z ↓	0.0369	0.0302	2.2915	1.1207
C to Z ↑	0.0398	0.0354	3.9544	1.8846
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0329	0.0312	0.7729	0.5774

A to Z ↑	0.0348	0.0330	1.2847	0.9632
B to Z ↓	0.0318	0.0299	0.7722	0.5768
B to Z ↑	0.0354	0.0336	1.2871	0.9625
C to Z ↓	0.0303	0.0287	0.7715	0.5762
C to Z ↑	0.0353	0.0336	1.2871	0.9635

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	5.533e-06	9.409e-10
X17_P0	1.133e-05	1.060e-09
X25_P0	1.629e-05	1.536e-09
X33_P0	2.172e-05	1.655e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	1.419e-05	2.905e-05	3.912e-05	5.406e-05
B (output stable)	1.645e-05	3.639e-05	5.070e-05	7.120e-05
C (output stable)	3.823e-05	7.854e-05	1.130e-04	1.621e-04
A to Z	1.967e-03	3.377e-03	4.924e-03	6.239e-03
B to Z	1.878e-03	3.220e-03	4.685e-03	5.911e-03
C to Z	1.810e-03	3.066e-03	4.450e-03	5.600e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

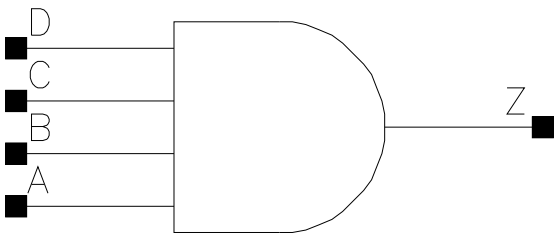
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	6.527e-08	5.054e-08	3.010e-08	2.973e-08
B (output stable)	6.176e-08	4.496e-08	2.306e-08	1.044e-08
C (output stable)	6.240e-08	4.310e-08	2.839e-08	1.543e-08
A to Z	-6.896e-08	-1.748e-07	-4.166e-07	-1.381e-07
B to Z	-1.202e-07	-2.883e-07	-5.541e-07	-2.408e-07
C to Z	-9.808e-08	-2.433e-07	-4.109e-07	-1.387e-07

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X6_P0	1.200	1.088	1.3056
X20_P0	1.200	2.312	2.7744
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P0	X6_P0	X20_P0	X27_P0
A	0.0005	0.0007	0.0015	0.0017
B	0.0005	0.0007	0.0015	0.0017
C	0.0004	0.0007	0.0015	0.0017
D	0.0005	0.0007	0.0015	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X6_P0	X4_P0	X6_P0
A to Z ↓	0.0422	0.0353	4.3119	2.7840
A to Z ↑	0.0432	0.0324	15.3273	8.1885
B to Z ↓	0.0412	0.0334	4.3108	2.7812
B to Z ↑	0.0442	0.0328	15.3337	8.1880
C to Z ↓	0.0440	0.0380	4.2768	2.7933
C to Z ↑	0.0425	0.0315	15.3416	8.2054

D to Z ↓	0.0429	0.0358	4.2705	2.7896
D to Z ↑	0.0444	0.0321	15.3454	8.2104
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0337	0.0318	0.8126	0.5752
A to Z ↑	0.0324	0.0362	2.7210	2.0643
B to Z ↓	0.0312	0.0297	0.8110	0.5744
B to Z ↑	0.0322	0.0362	2.7190	2.0643
C to Z ↓	0.0330	0.0308	0.8187	0.5779
C to Z ↑	0.0284	0.0308	2.7221	2.0622
D to Z ↓	0.0302	0.0287	0.8168	0.5763
D to Z ↑	0.0279	0.0307	2.7229	2.0644

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	3.971e-06	1.298e-09
X6_P0	8.655e-06	1.298e-09
X20_P0	2.411e-05	2.370e-09
X27_P0	2.826e-05	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	3.183e-04	4.858e-04	1.427e-03	1.757e-03
B (output stable)	2.975e-04	4.411e-04	1.295e-03	1.616e-03
C (output stable)	3.142e-04	5.082e-04	1.267e-03	1.580e-03
D (output stable)	2.977e-04	4.615e-04	1.118e-03	1.425e-03
A to Z	1.317e-03	2.013e-03	5.984e-03	7.805e-03
B to Z	1.262e-03	1.904e-03	5.497e-03	7.311e-03
C to Z	1.307e-03	2.058e-03	5.071e-03	6.354e-03
D to Z	1.253e-03	1.941e-03	4.566e-03	5.847e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

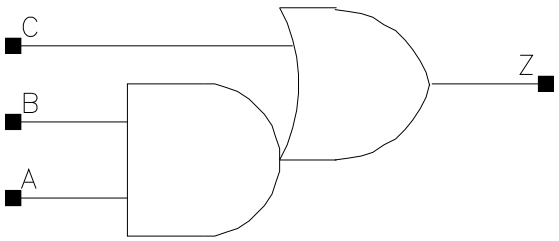
Pin Cycle (vdds)	X4_P0	X6_P0	X20_P0	X27_P0
A (output stable)	1.074e-07	1.546e-07	2.641e-07	2.632e-07
B (output stable)	1.422e-07	2.009e-07	4.045e-07	2.808e-07
C (output stable)	1.935e-06	1.999e-06	1.470e-05	3.226e-05
D (output stable)	1.966e-06	2.067e-06	1.455e-05	3.192e-05
A to Z	1.581e-07	3.446e-07	8.300e-07	1.516e-06
B to Z	2.066e-07	3.696e-07	9.630e-07	1.863e-06
C to Z	-1.154e-07	-2.899e-07	-1.039e-06	-1.194e-06
D to Z	-8.776e-08	-2.043e-07	-1.026e-06	-9.437e-07

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0008	0.0018
B	0.0006	0.0009	0.0016
C	0.0007	0.0010	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0472	0.0416	2.3394	1.1453
A to Z ↑	0.0308	0.0269	3.8161	1.8674
B to Z ↓	0.0442	0.0389	2.3300	1.1413
B to Z ↑	0.0320	0.0281	3.8148	1.8685
C to Z ↓	0.0477	0.0424	2.3246	1.1396
C to Z ↑	0.0271	0.0249	3.7945	1.8598
	X33_P0		**X33_P0**	
A to Z ↓	0.0416		0.5816	
A to Z ↑	0.0274		0.9429	

B to Z ↓	0.0389		0.5800	
B to Z ↑	0.0280		0.9418	
C to Z ↓	0.0424		0.5789	
C to Z ↑	0.0245		0.9377	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	8.100e-06	9.409e-10
X17_P0	1.560e-05	1.060e-09
X33_P0	3.082e-05	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	2.240e-05	4.020e-05	9.728e-05
B (output stable)	2.404e-05	4.345e-05	1.209e-04
C (output stable)	5.249e-05	8.927e-05	2.060e-04
A to Z	1.825e-03	3.081e-03	6.083e-03
B to Z	1.739e-03	2.922e-03	5.681e-03
C to Z	2.022e-03	3.425e-03	6.759e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

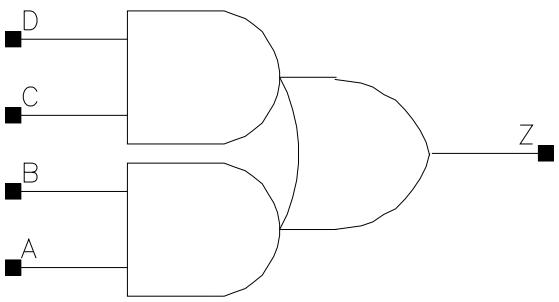
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	1.048e-05	1.372e-05	2.924e-05
B (output stable)	1.067e-05	1.452e-05	2.975e-05
C (output stable)	-3.891e-07	1.344e-08	-3.504e-07
A to Z	-1.624e-07	-2.600e-07	-7.348e-07
B to Z	-9.750e-08	-1.787e-07	-4.804e-07
C to Z	5.670e-07	6.940e-07	1.502e-06

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0005	0.0008	0.0017
B	0.0006	0.0009	0.0016
C	0.0005	0.0008	0.0017
D	0.0006	0.0009	0.0016

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0555	0.0485	2.2491	1.1355
A to Z ↑	0.0385	0.0344	3.7652	1.8733
B to Z ↓	0.0522	0.0458	2.2393	1.1321
B to Z ↑	0.0390	0.0354	3.7653	1.8729

C to Z ↓	0.0486	0.0433	2.2429	1.1328
C to Z ↑	0.0334	0.0301	3.7517	1.8682
D to Z ↓	0.0470	0.0415	2.2351	1.1299
D to Z ↑	0.0350	0.0313	3.7574	1.8665
	X33_P0		**X33_P0**	
A to Z ↓	0.0452		0.5810	
A to Z ↑	0.0311		0.9467	
B to Z ↓	0.0431		0.5803	
B to Z ↑	0.0323		0.9464	
C to Z ↓	0.0399		0.5801	
C to Z ↑	0.0274		0.9429	
D to Z ↓	0.0378		0.5792	
D to Z ↑	0.0282		0.9423	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	8.762e-06	1.179e-09
X17_P0	1.682e-05	1.298e-09
X33_P0	3.156e-05	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	3.394e-05	4.824e-05	6.889e-05
B (output stable)	1.050e-04	1.274e-04	7.404e-05
C (output stable)	2.713e-05	5.013e-05	1.064e-04
D (output stable)	2.864e-05	5.343e-05	1.168e-04
A to Z	2.444e-03	4.078e-03	7.330e-03
B to Z	2.266e-03	3.837e-03	6.977e-03
C to Z	2.049e-03	3.462e-03	6.093e-03
D to Z	1.976e-03	3.312e-03	5.776e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

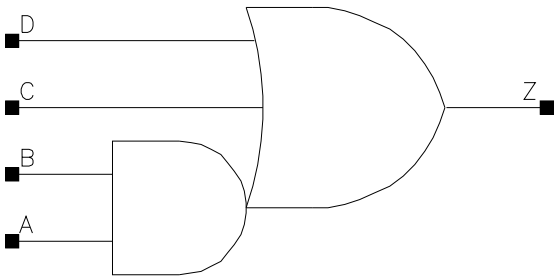
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	6.654e-08	1.158e-07	1.019e-07
B (output stable)	-5.055e-07	8.160e-08	1.312e-07
C (output stable)	4.706e-06	5.768e-06	1.522e-05
D (output stable)	4.495e-06	5.585e-06	1.543e-05
A to Z	3.088e-07	4.761e-07	1.895e-06
B to Z	4.830e-07	7.471e-07	1.875e-06
C to Z	-1.417e-07	-1.304e-07	-1.697e-07
D to Z	-1.359e-07	-1.453e-07	-3.855e-07

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	0.952	1.1424
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0009	0.0016
B	0.0006	0.0008	0.0016
C	0.0006	0.0008	0.0016
D	0.0006	0.0009	0.0016

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0630	0.0541	2.4643	1.2118
A to Z ↑	0.0332	0.0292	3.8038	1.9327
B to Z ↓	0.0609	0.0509	2.4583	1.2078
B to Z ↑	0.0346	0.0299	3.8068	1.9331
C to Z ↓	0.0690	0.0595	2.4522	1.2065
C to Z ↑	0.0292	0.0266	3.7821	1.9233

D to Z ↓	0.0674	0.0588	2.4521	1.2067
D to Z ↑	0.0289	0.0264	3.7766	1.9227
	X33_P0		**X33_P0**	
A to Z ↓	0.0549		0.6073	
A to Z ↑	0.0291		0.9428	
B to Z ↓	0.0497		0.6036	
B to Z ↑	0.0293		0.9426	
C to Z ↓	0.0608		0.6036	
C to Z ↑	0.0260		0.9392	
D to Z ↓	0.0587		0.6035	
D to Z ↑	0.0253		0.9376	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	7.848e-06	1.060e-09
X17_P0	1.531e-05	1.179e-09
X33_P0	3.072e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	1.880e-05	3.740e-05	9.970e-05
B (output stable)	1.911e-05	3.697e-05	1.210e-04
C (output stable)	2.788e-05	5.292e-05	1.485e-04
D (output stable)	2.419e-05	4.851e-05	1.342e-04
A to Z	2.037e-03	3.353e-03	6.749e-03
B to Z	1.967e-03	3.187e-03	6.194e-03
C to Z	2.350e-03	3.911e-03	7.949e-03
D to Z	2.216e-03	3.692e-03	7.326e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

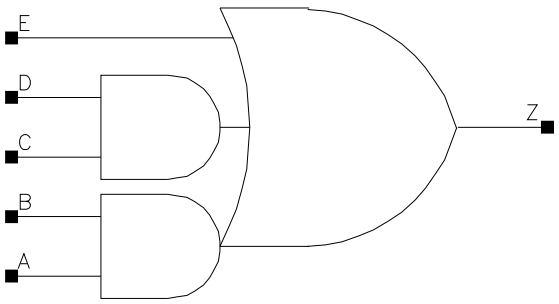
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	1.814e-05	2.915e-05	6.027e-05
B (output stable)	1.791e-05	2.792e-05	6.001e-05
C (output stable)	-8.556e-07	-8.149e-07	-2.789e-06
D (output stable)	6.057e-06	9.734e-06	4.158e-05
A to Z	-8.840e-08	-4.018e-07	-1.040e-06
B to Z	-9.610e-08	-2.163e-07	-5.425e-07
C to Z	7.067e-07	1.605e-06	3.156e-06
D to Z	4.812e-07	8.043e-07	1.771e-06

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.088	1.3056
X17_P0	1.200	1.224	1.4688
X33_P0	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0005	0.0008	0.0017
B	0.0006	0.0008	0.0015
C	0.0007	0.0011	0.0017
D	0.0006	0.0008	0.0016
E	0.0006	0.0008	0.0015

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0797	0.0670	2.3446	1.1719
A to Z ↑	0.0403	0.0342	3.7427	1.8823

B to Z ↓	0.0775	0.0644	2.3362	1.1683
B to Z ↑	0.0423	0.0356	3.7399	1.8810
C to Z ↓	0.0653	0.0559	2.3332	1.1686
C to Z ↑	0.0351	0.0296	3.7030	1.8701
D to Z ↓	0.0612	0.0514	2.3236	1.1631
D to Z ↑	0.0363	0.0305	3.7056	1.8690
E to Z ↓	0.0698	0.0588	2.3186	1.1621
E to Z ↑	0.0305	0.0264	3.6778	1.8576
	X33_P0		**X33_P0**	
A to Z ↓	0.0659		0.6059	
A to Z ↑	0.0349		0.9515	
B to Z ↓	0.0623		0.6040	
B to Z ↑	0.0361		0.9505	
C to Z ↓	0.0540		0.6041	
C to Z ↑	0.0295		0.9429	
D to Z ↓	0.0500		0.6015	
D to Z ↑	0.0303		0.9422	
E to Z ↓	0.0574		0.6011	
E to Z ↑	0.0262		0.9374	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	9.288e-06	1.298e-09
X17_P0	1.771e-05	1.417e-09
X33_P0	3.255e-05	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	1.744e-05	2.979e-05	6.734e-05
B (output stable)	2.165e-05	3.003e-05	7.545e-05
C (output stable)	3.189e-05	4.819e-05	1.175e-04
D (output stable)	3.516e-05	5.481e-05	1.312e-04
E (output stable)	6.588e-05	1.018e-04	2.306e-04
A to Z	2.812e-03	4.456e-03	8.726e-03
B to Z	2.745e-03	4.286e-03	8.265e-03
C to Z	2.200e-03	3.527e-03	6.814e-03
D to Z	2.109e-03	3.341e-03	6.386e-03
E to Z	2.430e-03	3.856e-03	7.450e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	-3.006e-07	-8.683e-08	-3.407e-07
B (output stable)	-3.413e-07	-1.131e-07	-3.725e-07
C (output stable)	1.399e-05	1.732e-05	4.356e-05
D (output stable)	1.527e-05	2.003e-05	4.383e-05
E (output stable)	1.305e-05	1.335e-05	3.087e-05
A to Z	1.092e-06	1.713e-06	2.470e-06
B to Z	1.231e-06	1.917e-06	3.780e-06
C to Z	-2.139e-07	-3.025e-07	-7.359e-07
D to Z	-1.175e-07	-2.199e-07	-6.124e-07

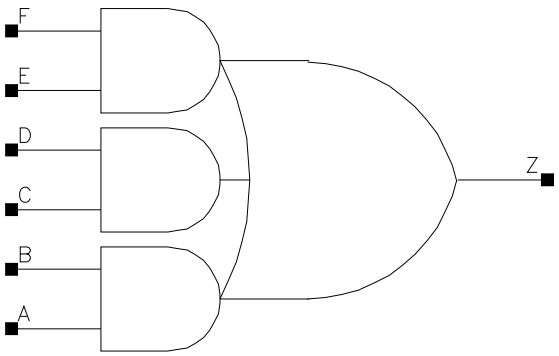
E to Z	4.949e-07	6.338e-07	1.521e-06

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.360	1.6320
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
A	0.0005	0.0006	0.0008	0.0017

B	0.0006	0.0007	0.0011	0.0015
C	0.0005	0.0006	0.0008	0.0016
D	0.0005	0.0006	0.0008	0.0015
E	0.0006	0.0007	0.0008	0.0017
F	0.0006	0.0007	0.0009	0.0016

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0807	0.0754	4.5041	2.3366
A to Z ↑	0.0429	0.0407	7.5102	3.8120
B to Z ↓	0.0750	0.0705	4.4737	2.3210
B to Z ↑	0.0432	0.0413	7.5053	3.8116
C to Z ↓	0.0729	0.0687	4.4889	2.3296
C to Z ↑	0.0395	0.0374	7.4602	3.7866
D to Z ↓	0.0703	0.0661	4.4722	2.3204
D to Z ↑	0.0413	0.0391	7.4620	3.7877
E to Z ↓	0.0587	0.0567	4.4662	2.3198
E to Z ↑	0.0340	0.0324	7.4140	3.7667
F to Z ↓	0.0553	0.0534	4.4502	2.3105
F to Z ↑	0.0351	0.0336	7.4123	3.7644
	X17_P0	X33_P0	X17_P0	X33_P0
A to Z ↓	0.0718	0.0680	1.1777	0.6045
A to Z ↑	0.0372	0.0370	1.8889	0.9544
B to Z ↓	0.0680	0.0647	1.1697	0.6026
B to Z ↑	0.0386	0.0382	1.8890	0.9537
C to Z ↓	0.0658	0.0629	1.1738	0.6039
C to Z ↑	0.0343	0.0347	1.8792	0.9481
D to Z ↓	0.0629	0.0599	1.1693	0.6020
D to Z ↑	0.0358	0.0359	1.8791	0.9481
E to Z ↓	0.0539	0.0545	1.1694	0.6021
E to Z ↑	0.0294	0.0306	1.8688	0.9445
F to Z ↓	0.0509	0.0508	1.1649	0.5997
F to Z ↑	0.0306	0.0317	1.8691	0.9452

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	7.355e-06	1.536e-09
X8_P0	1.125e-05	1.536e-09
X17_P0	1.905e-05	1.655e-09
X33_P0	3.450e-05	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	3.390e-05	3.979e-05	5.149e-05	9.446e-05
B (output stable)	8.218e-05	9.112e-05	9.381e-05	1.121e-04
C (output stable)	2.716e-05	3.380e-05	4.591e-05	9.371e-05
D (output stable)	2.957e-05	3.685e-05	4.846e-05	1.199e-04
E (output stable)	5.089e-05	6.176e-05	8.150e-05	1.363e-04
F (output stable)	5.185e-05	6.201e-05	8.485e-05	1.547e-04

A to Z	2.587e-03	3.374e-03	5.014e-03	9.379e-03
B to Z	2.400e-03	3.153e-03	4.715e-03	8.916e-03
C to Z	2.192e-03	2.904e-03	4.380e-03	8.230e-03
D to Z	2.115e-03	2.803e-03	4.215e-03	7.832e-03
E to Z	1.744e-03	2.407e-03	3.642e-03	7.117e-03
F to Z	1.662e-03	2.299e-03	3.479e-03	6.719e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

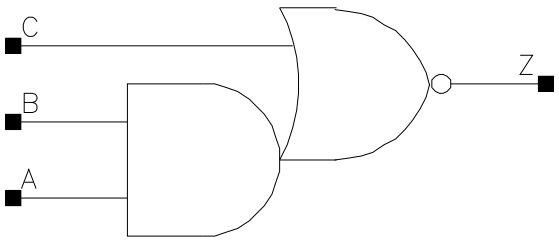
Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X33_P0
A (output stable)	-5.149e-07	-4.301e-07	-3.205e-07	-4.991e-07
B (output stable)	-9.157e-07	-4.598e-07	-1.866e-07	-5.840e-07
C (output stable)	4.305e-06	4.870e-06	5.998e-06	1.569e-05
D (output stable)	4.597e-06	5.173e-06	5.862e-06	1.591e-05
E (output stable)	1.997e-05	2.335e-05	2.909e-05	4.538e-05
F (output stable)	1.965e-05	2.257e-05	2.899e-05	4.530e-05
A to Z	1.102e-06	1.556e-06	2.247e-06	3.817e-06
B to Z	1.296e-06	1.796e-06	2.315e-06	4.571e-06
C to Z	6.313e-07	8.576e-07	1.163e-06	9.710e-07
D to Z	7.171e-07	8.584e-07	1.243e-06	1.394e-06
E to Z	-3.839e-07	-4.230e-07	-4.929e-07	-4.196e-07
F to Z	-3.006e-07	-3.080e-07	-3.946e-07	-7.393e-07

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008
X44_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X33_P0	X44_P0
A	0.0007	0.0020	0.0040	0.0054
B	0.0007	0.0019	0.0037	0.0050
C	0.0007	0.0021	0.0043	0.0056

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0123	0.0128	4.3089	1.4679
A to Z ↑	0.0217	0.0219	8.3326	2.7720
B to Z ↓	0.0119	0.0120	4.3439	1.4826
B to Z ↑	0.0184	0.0179	8.2270	2.7706
C to Z ↓	0.0116	0.0117	2.3079	0.7949
C to Z ↑	0.0237	0.0234	7.6156	2.5516
	X33_P0	**X44_P0**	**X33_P0**	**X44_P0**
A to Z ↓	0.0132	0.0131	0.7446	0.5641

A to Z ↑	0.0221	0.0221	1.3885	1.0513
B to Z ↓	0.0121	0.0121	0.7516	0.5695
B to Z ↑	0.0181	0.0180	1.3859	1.0468
C to Z ↓	0.0133	0.0134	0.4736	0.3686
C to Z ↑	0.0241	0.0238	1.2760	0.9647

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P0	6.089e-06	8.218e-10
X17_P0	1.652e-05	1.536e-09
X33_P0	3.079e-05	2.608e-09
X44_P0	4.116e-05	3.323e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	4.161e-05	1.288e-04	2.838e-04	3.672e-04
B (output stable)	4.381e-05	1.659e-04	3.681e-04	4.707e-04
C (output stable)	8.770e-05	2.700e-04	6.050e-04	7.680e-04
A to Z	8.599e-04	2.693e-03	5.529e-03	7.303e-03
B to Z	7.140e-04	2.042e-03	4.177e-03	5.506e-03
C to Z	1.220e-03	3.579e-03	7.450e-03	9.699e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

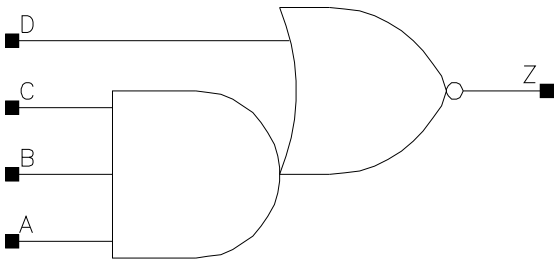
Pin Cycle (vdds)	X6_P0	X17_P0	X33_P0	X44_P0
A (output stable)	1.338e-05	3.108e-05	7.541e-05	8.474e-05
B (output stable)	1.345e-05	3.116e-05	7.446e-05	8.468e-05
C (output stable)	-4.628e-08	-2.835e-07	-7.130e-07	-7.281e-07
A to Z	-2.220e-07	-7.800e-08	-2.100e-06	-2.767e-06
B to Z	-5.560e-08	-2.500e-07	-6.350e-07	-9.060e-07
C to Z	1.235e-06	2.664e-06	6.363e-06	6.950e-06

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X29_P0	1.200	3.536	4.2432
X38_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X29_P0	X38_P0
A	0.0007	0.0041	0.0053
B	0.0007	0.0039	0.0051
C	0.0007	0.0037	0.0049
D	0.0007	0.0042	0.0053

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X29_P0	X5_P0	X29_P0
A to Z ↓	0.0180	0.0191	6.3573	1.0921
A to Z ↑	0.0275	0.0274	8.3277	1.3766
B to Z ↓	0.0182	0.0186	6.3706	1.0971
B to Z ↑	0.0249	0.0245	8.3185	1.3845
C to Z ↓	0.0172	0.0169	6.3703	1.0994
C to Z ↑	0.0219	0.0210	8.2300	1.3914
D to Z ↓	0.0138	0.0156	2.3546	0.4775

D to Z ↑	0.0272	0.0275	7.0927	1.1836
	X38_P0		**X38_P0**	
A to Z ↓	0.0185		0.8417	
A to Z ↑	0.0264		1.0369	
B to Z ↓	0.0181		0.8454	
B to Z ↑	0.0236		1.0446	
C to Z ↓	0.0162		0.8480	
C to Z ↑	0.0200		1.0531	
D to Z ↓	0.0162		0.3991	
D to Z ↑	0.0267		0.8926	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P0	6.021e-06	9.409e-10
X29_P0	3.000e-05	3.442e-09
X38_P0	3.814e-05	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P0	X29_P0	X38_P0
A (output stable)	2.563e-05	2.101e-04	2.664e-04
B (output stable)	2.842e-05	2.725e-04	3.469e-04
C (output stable)	4.635e-05	5.037e-04	6.414e-04
D (output stable)	1.112e-04	8.102e-04	1.077e-03
A to Z	1.282e-03	8.098e-03	1.008e-02
B to Z	1.123e-03	6.728e-03	8.377e-03
C to Z	9.705e-04	5.364e-03	6.551e-03
D to Z	1.601e-03	9.769e-03	1.244e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

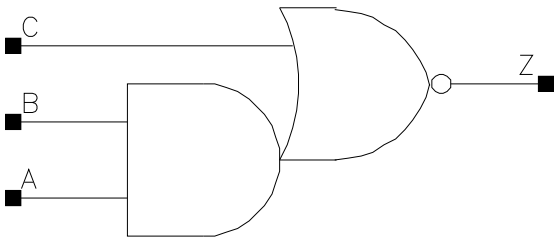
Pin Cycle (vdds)	X5_P0	X29_P0	X38_P0
A (output stable)	6.015e-06	5.193e-05	6.603e-05
B (output stable)	6.385e-06	5.138e-05	6.528e-05
C (output stable)	6.197e-06	5.038e-05	6.403e-05
D (output stable)	-2.184e-07	-3.989e-06	-4.920e-06
A to Z	5.000e-08	-3.555e-06	-1.397e-06
B to Z	-1.360e-07	-1.840e-06	-2.722e-06
C to Z	-6.000e-09	-7.450e-07	-1.711e-06
D to Z	7.197e-07	6.140e-06	8.497e-06

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X11_P0	1.200	1.088	1.3056
X16_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P0	X11_P0	X16_P0	X23_P0
A	0.0007	0.0015	0.0022	0.0029
B	0.0007	0.0014	0.0021	0.0027
C	0.0007	0.0013	0.0019	0.0027
	X46_P0			
A	0.0056			
B	0.0053			
C	0.0053			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X11_P0	X6_P0	X11_P0
A to Z ↓	0.0141	0.0151	4.1840	2.1207
A to Z ↑	0.0252	0.0266	8.3176	4.0665
B to Z ↓	0.0142	0.0144	4.2115	2.1362

B to Z ↑	0.0228	0.0232	8.2378	4.0725
C to Z ↓	0.0086	0.0090	2.3728	1.3930
C to Z ↑	0.0178	0.0173	7.5809	3.7278
	X16_P0	**X23_P0**	**X16_P0**	**X23_P0**
A to Z ↓	0.0145	0.0148	1.4663	1.1012
A to Z ↑	0.0249	0.0255	2.7290	2.0631
B to Z ↓	0.0142	0.0142	1.4783	1.1098
B to Z ↑	0.0215	0.0221	2.7256	2.0688
C to Z ↓	0.0091	0.0080	0.9771	0.6097
C to Z ↑	0.0166	0.0170	2.5023	1.8935
	X46_P0		**X46_P0**	
A to Z ↓	0.0143		0.5651	
A to Z ↑	0.0245		1.0621	
B to Z ↓	0.0139		0.5695	
B to Z ↑	0.0210		1.0593	
C to Z ↓	0.0082		0.3132	
C to Z ↑	0.0167		0.9727	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P0	6.015e-06	8.218e-10
X11_P0	1.186e-05	1.298e-09
X16_P0	1.597e-05	1.536e-09
X23_P0	2.273e-05	2.013e-09
X46_P0	4.322e-05	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	2.563e-05	7.235e-05	9.437e-05	1.374e-04
B (output stable)	2.899e-05	1.137e-04	1.195e-04	1.910e-04
C (output stable)	1.617e-04	3.639e-04	4.684e-04	6.662e-04
A to Z	1.235e-03	2.753e-03	3.695e-03	5.119e-03
B to Z	1.079e-03	2.268e-03	3.018e-03	4.156e-03
C to Z	6.751e-04	1.360e-03	1.879e-03	2.601e-03
	X46_P0			
A (output stable)	2.470e-04			
B (output stable)	3.237e-04			
C (output stable)	1.158e-03			
A to Z	9.371e-03			
B to Z	7.558e-03			
C to Z	4.835e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X6_P0	X11_P0	X16_P0	X23_P0
A (output stable)	1.225e-07	1.324e-07	2.384e-07	2.957e-07
B (output stable)	1.097e-07	1.016e-07	1.090e-07	5.773e-08
C (output stable)	2.457e-05	7.900e-05	5.695e-05	9.483e-05
A to Z	1.094e-06	2.282e-06	2.751e-06	2.630e-06
B to Z	1.088e-06	3.060e-06	2.650e-06	3.283e-06
C to Z	8.583e-08	6.180e-08	4.480e-07	5.923e-07

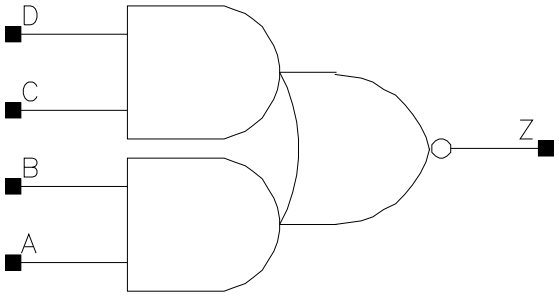
	X46_P0			
A (output stable)	4.102e-07			
B (output stable)	2.315e-07			
C (output stable)	1.318e-04			
A to Z	2.848e-06			
B to Z	6.719e-06			
C to Z	1.316e-06			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P0	X10_P0	X16_P0	X21_P0
A	0.0006	0.0015	0.0022	0.0028
B	0.0006	0.0013	0.0020	0.0027
C	0.0006	0.0014	0.0020	0.0027
D	0.0006	0.0013	0.0019	0.0025
	X42_P0			
A	0.0057			
B	0.0054			
C	0.0053			
D	0.0051			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X10_P0**	**X4_P0**	**X10_P0**
A to Z ↓	0.0159	0.0156	5.2324	2.0513
A to Z ↑	0.0322	0.0275	11.4213	3.7464
B to Z ↓	0.0163	0.0162	5.2655	2.0657
B to Z ↑	0.0294	0.0256	11.3921	3.8150
C to Z ↓	0.0126	0.0121	5.3262	2.0569
C to Z ↑	0.0246	0.0214	11.3040	3.7254
D to Z ↓	0.0125	0.0119	5.3735	2.0775
D to Z ↑	0.0216	0.0188	11.2710	3.7669
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0167	0.0166	1.4740	1.1057
A to Z ↑	0.0288	0.0284	2.5221	1.9371
B to Z ↓	0.0169	0.0163	1.4837	1.1135
B to Z ↑	0.0257	0.0252	2.5193	1.9370
C to Z ↓	0.0129	0.0131	1.4706	1.1048
C to Z ↑	0.0220	0.0225	2.4987	1.9167
D to Z ↓	0.0122	0.0119	1.4865	1.1169
D to Z ↑	0.0185	0.0187	2.5001	1.9181
	X42_P0		**X42_P0**	
A to Z ↓	0.0172		0.5730	
A to Z ↑	0.0287		0.9729	
B to Z ↓	0.0168		0.5768	
B to Z ↑	0.0253		0.9688	
C to Z ↓	0.0135		0.5661	
C to Z ↑	0.0225		0.9639	
D to Z ↓	0.0124		0.5724	
D to Z ↑	0.0189		0.9610	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	5.342e-06	9.409e-10
X10_P0	1.443e-05	1.536e-09
X16_P0	1.954e-05	1.894e-09
X21_P0	2.637e-05	2.489e-09
X42_P0	5.087e-05	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	2.804e-05	6.571e-05	1.313e-04	1.784e-04
B (output stable)	2.976e-05	7.388e-05	1.988e-04	2.918e-04
C (output stable)	3.932e-05	1.033e-04	1.839e-04	2.477e-04
D (output stable)	4.332e-05	1.152e-04	2.517e-04	3.562e-04
A to Z	1.279e-03	3.093e-03	4.897e-03	6.295e-03
B to Z	1.137e-03	2.759e-03	4.183e-03	5.339e-03
C to Z	7.575e-04	1.872e-03	2.933e-03	3.983e-03
D to Z	6.396e-04	1.577e-03	2.272e-03	3.047e-03
	X42_P0			
A (output stable)	3.413e-04			
B (output stable)	5.162e-04			
C (output stable)	4.715e-04			
D (output stable)	6.568e-04			

A to Z	1.243e-02			
B to Z	1.057e-02			
C to Z	7.745e-03			
D to Z	5.998e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

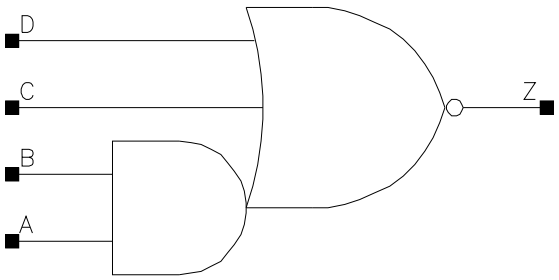
Pin Cycle (vdds)	X4_P0	X10_P0	X16_P0	X21_P0
A (output stable)	3.906e-08	1.239e-07	1.023e-07	1.723e-07
B (output stable)	1.456e-08	1.247e-07	8.401e-08	-1.784e-07
C (output stable)	1.074e-05	1.765e-05	2.735e-05	3.040e-05
D (output stable)	1.100e-05	1.803e-05	2.729e-05	3.010e-05
A to Z	1.658e-06	3.036e-06	3.487e-06	3.607e-06
B to Z	1.409e-06	2.770e-06	3.896e-06	5.101e-06
C to Z	-1.221e-07	-7.200e-08	-1.890e-07	-1.414e-06
D to Z	2.190e-08	-2.733e-07	-3.537e-07	-1.800e-07
	X42_P0			
A (output stable)	3.597e-07			
B (output stable)	-3.188e-07			
C (output stable)	5.738e-05			
D (output stable)	5.581e-05			
A to Z	7.487e-06			
B to Z	9.100e-06			
C to Z	-3.094e-06			
D to Z	-1.492e-06			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X35_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P0	X35_P0
A	0.0007	0.0053
B	0.0007	0.0048
C	0.0007	0.0051
D	0.0007	0.0048

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X35_P0	X5_P0	X35_P0
A to Z ↓	0.0142	0.0148	4.3615	0.6403
A to Z ↑	0.0289	0.0272	12.6811	1.6038
B to Z ↓	0.0141	0.0141	4.4026	0.6472
B to Z ↑	0.0250	0.0225	12.6165	1.6022
C to Z ↓	0.0138	0.0176	2.4453	0.4743
C to Z ↑	0.0352	0.0344	11.9932	1.5175
D to Z ↓	0.0135	0.0164	2.4727	0.4734

D to Z ↑	0.0339	0.0320	11.9979	1.5202

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P0	4.770e-06	9.409e-10
X35_P0	2.979e-05	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P0	X35_P0
A (output stable)	3.636e-05	3.210e-04
B (output stable)	3.706e-05	3.569e-04
C (output stable)	5.004e-05	5.606e-04
D (output stable)	4.668e-05	4.476e-04
A to Z	1.047e-03	7.655e-03
B to Z	8.966e-04	6.051e-03
C to Z	1.638e-03	1.270e-02
D to Z	1.405e-03	1.022e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

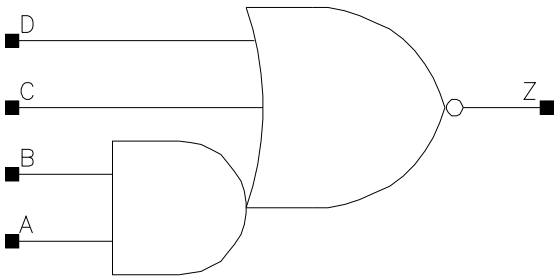
Pin Cycle (vdds)	X5_P0	X35_P0
A (output stable)	2.773e-05	1.779e-04
B (output stable)	2.717e-05	1.779e-04
C (output stable)	-8.155e-07	-7.481e-06
D (output stable)	9.410e-06	1.069e-04
A to Z	-3.538e-07	-3.819e-06
B to Z	-3.210e-07	-3.076e-06
C to Z	2.039e-06	1.012e-05
D to Z	1.152e-06	3.327e-06

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.680	0.8160
X17_P0	1.200	2.448	2.9376
X34_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P0	X17_P0	X34_P0
A	0.0007	0.0028	0.0057
B	0.0007	0.0027	0.0054
C	0.0006	0.0025	0.0049
D	0.0006	0.0023	0.0044

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X17_P0	X4_P0	X17_P0
A to Z ↓	0.0161	0.0173	4.7552	1.2519
A to Z ↑	0.0343	0.0361	12.7240	3.1321
B to Z ↓	0.0169	0.0172	4.7844	1.2590
B to Z ↑	0.0312	0.0317	12.6254	3.1339
C to Z ↓	0.0148	0.0144	3.9971	0.9722
C to Z ↑	0.0258	0.0272	11.9523	2.9539

D to Z ↓	0.0128	0.0115	4.0572	0.9757
D to Z ↑	0.0224	0.0203	11.9842	2.9631
	X34_P0		**X34_P0**	
A to Z ↓	0.0171		0.6409	
A to Z ↑	0.0355		1.5883	
B to Z ↓	0.0171		0.6447	
B to Z ↑	0.0311		1.5829	
C to Z ↓	0.0145		0.5107	
C to Z ↑	0.0264		1.4962	
D to Z ↓	0.0117		0.5144	
D to Z ↑	0.0198		1.5007	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	4.095e-06	9.409e-10
X17_P0	1.574e-05	2.489e-09
X34_P0	3.005e-05	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X17_P0	X34_P0
A (output stable)	2.326e-05	1.168e-04	2.310e-04
B (output stable)	2.414e-05	1.454e-04	2.703e-04
C (output stable)	4.676e-05	2.618e-04	4.951e-04
D (output stable)	7.049e-05	4.226e-04	8.000e-04
A to Z	1.525e-03	6.642e-03	1.281e-02
B to Z	1.378e-03	5.702e-03	1.104e-02
C to Z	9.546e-04	4.143e-03	7.859e-03
D to Z	7.094e-04	2.640e-03	5.014e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

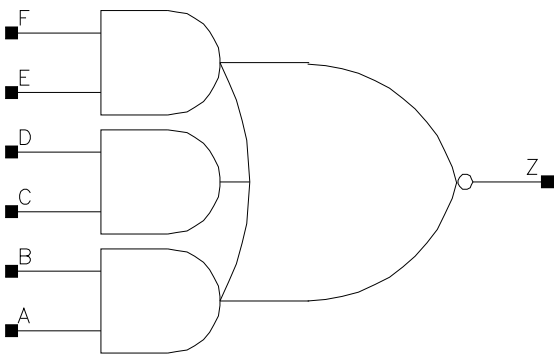
Pin Cycle (vdds)	X4_P0	X17_P0	X34_P0
A (output stable)	1.071e-08	-6.561e-07	-1.245e-06
B (output stable)	-7.004e-09	-7.994e-07	-1.442e-06
C (output stable)	8.825e-06	3.521e-05	6.916e-05
D (output stable)	1.721e-05	1.292e-04	2.316e-04
A to Z	1.973e-06	5.778e-06	1.239e-05
B to Z	1.945e-06	6.617e-06	1.206e-05
C to Z	3.097e-07	1.528e-06	1.873e-06
D to Z	-3.063e-07	-7.585e-07	-1.866e-06

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.088	1.3056
X8_P0	1.200	2.176	2.6112
X13_P0	1.200	2.720	3.2640
X17_P0	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P0	X8_P0	X13_P0	X17_P0
A	0.0007	0.0014	0.0021	0.0028

B	0.0007	0.0013	0.0020	0.0026
C	0.0007	0.0014	0.0020	0.0026
D	0.0007	0.0013	0.0019	0.0025
E	0.0009	0.0013	0.0019	0.0025
F	0.0007	0.0012	0.0018	0.0024

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0187	0.0221	4.2009	2.4292
A to Z ↑	0.0486	0.0479	12.1813	5.6200
B to Z ↓	0.0199	0.0224	4.2220	2.4390
B to Z ↑	0.0454	0.0439	12.1683	5.6265
C to Z ↓	0.0174	0.0203	4.1637	2.4336
C to Z ↑	0.0424	0.0429	12.2121	5.6283
D to Z ↓	0.0182	0.0207	4.1933	2.4480
D to Z ↑	0.0391	0.0388	12.1602	5.6219
E to Z ↓	0.0137	0.0160	4.0760	2.4307
E to Z ↑	0.0310	0.0313	12.0713	5.5772
F to Z ↓	0.0137	0.0158	4.1189	2.4539
F to Z ↑	0.0275	0.0271	12.1251	5.5786
	X13_P0	X17_P0	X13_P0	X17_P0
A to Z ↓	0.0211	0.0213	1.6524	1.2599
A to Z ↑	0.0444	0.0448	3.7260	2.8363
B to Z ↓	0.0219	0.0216	1.6582	1.2646
B to Z ↑	0.0410	0.0408	3.7333	2.8352
C to Z ↓	0.0195	0.0195	1.6660	1.2474
C to Z ↑	0.0393	0.0398	3.7343	2.8450
D to Z ↓	0.0202	0.0195	1.6747	1.2549
D to Z ↑	0.0359	0.0358	3.7363	2.8397
E to Z ↓	0.0156	0.0155	1.6587	1.2472
E to Z ↑	0.0293	0.0293	3.7045	2.8139
F to Z ↓	0.0154	0.0146	1.6732	1.2592
F to Z ↑	0.0254	0.0251	3.7065	2.8211

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	8.173e-06	1.298e-09
X8_P0	1.587e-05	2.251e-09
X13_P0	2.175e-05	2.727e-09
X17_P0	2.911e-05	3.561e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	4.281e-05	1.022e-04	1.419e-04	1.947e-04
B (output stable)	4.346e-05	1.507e-04	1.734e-04	2.702e-04
C (output stable)	4.570e-05	1.057e-04	1.419e-04	2.035e-04
D (output stable)	4.825e-05	1.623e-04	1.793e-04	2.801e-04
E (output stable)	6.260e-05	1.551e-04	2.174e-04	2.964e-04
F (output stable)	6.908e-05	2.018e-04	2.531e-04	3.730e-04

A to Z	2.450e-03	5.155e-03	7.064e-03	9.436e-03
B to Z	2.279e-03	4.667e-03	6.455e-03	8.506e-03
C to Z	1.849e-03	4.063e-03	5.426e-03	7.240e-03
D to Z	1.697e-03	3.626e-03	4.876e-03	6.379e-03
E to Z	1.179e-03	2.697e-03	3.623e-03	4.786e-03
F to Z	1.038e-03	2.272e-03	3.054e-03	3.945e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

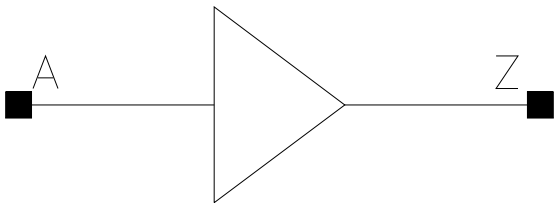
Pin Cycle (vdds)	X4_P0	X8_P0	X13_P0	X17_P0
A (output stable)	-5.427e-07	-1.079e-06	-1.075e-06	-1.494e-06
B (output stable)	-5.526e-07	-1.163e-06	-1.182e-06	-1.932e-06
C (output stable)	9.816e-06	1.780e-05	1.996e-05	2.682e-05
D (output stable)	9.781e-06	1.772e-05	1.992e-05	2.621e-05
E (output stable)	2.930e-05	6.945e-05	7.509e-05	1.032e-04
F (output stable)	3.204e-05	7.007e-05	7.569e-05	1.024e-04
A to Z	3.331e-06	6.320e-06	7.435e-06	1.008e-05
B to Z	3.465e-06	6.756e-06	7.687e-06	1.059e-05
C to Z	1.247e-06	2.746e-06	2.572e-06	3.773e-06
D to Z	1.304e-06	2.907e-06	2.699e-06	4.071e-06
E to Z	-6.207e-07	-1.402e-06	-1.763e-06	-2.495e-06
F to Z	-4.572e-07	-1.225e-06	-1.476e-06	-2.088e-06

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X6_P0	1.200	0.408	0.4896
X8_P0	1.200	0.408	0.4896
X13_P0	1.200	0.544	0.6528
X16_P0	1.200	0.544	0.6528
X21_P0	1.200	0.680	0.8160
X25_P0	1.200	0.680	0.8160
X29_P0	1.200	0.952	1.1424
X33_P0	1.200	0.952	1.1424
X42_P0	1.200	1.088	1.3056
X50_P0	1.200	1.224	1.4688
X58_P0	1.200	1.496	1.7952
X67_P0	1.200	1.632	1.9584
X75_P0	1.200	1.768	2.1216
X84_P0	1.200	1.904	2.2848
X100_P0	1.200	2.312	2.7744
X134_P0	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0007	0.0007	0.0007	0.0007
	X16_P0	X21_P0	X25_P0	X29_P0
A	0.0007	0.0010	0.0010	0.0013
	X33_P0	X42_P0	X50_P0	X58_P0
A	0.0013	0.0015	0.0018	0.0026

	X67_P0	X75_P0	X84_P0	X100_P0
A	0.0026	0.0026	0.0025	0.0034
	X134_P0			
A	0.0043			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0298	0.0298	4.1828	3.0283
A to Z ↑	0.0231	0.0228	7.3515	5.3565
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0307	0.0341	2.2335	1.4508
A to Z ↑	0.0233	0.0258	3.8103	2.4974
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0363	0.0306	1.1505	0.8906
A to Z ↑	0.0270	0.0234	1.9093	1.4968
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0321	0.0306	0.7645	0.6477
A to Z ↑	0.0243	0.0227	1.2545	1.0688
	X33_P0	**X42_P0**	**X33_P0**	**X42_P0**
A to Z ↓	0.0318	0.0311	0.5743	0.4663
A to Z ↑	0.0236	0.0237	0.9373	0.7545
	X50_P0	**X58_P0**	**X50_P0**	**X58_P0**
A to Z ↓	0.0304	0.0284	0.3872	0.3340
A to Z ↑	0.0230	0.0219	0.6259	0.5382
	X67_P0	**X75_P0**	**X67_P0**	**X75_P0**
A to Z ↓	0.0296	0.0312	0.2936	0.2647
A to Z ↑	0.0226	0.0238	0.4712	0.4217
	X84_P0	**X100_P0**	**X84_P0**	**X100_P0**
A to Z ↓	0.0321	0.0306	0.2395	0.2013
A to Z ↑	0.0244	0.0234	0.3803	0.3183
	X134_P0		**X134_P0**	
A to Z ↓	0.0320		0.1560	
A to Z ↑	0.0246		0.2428	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	5.300e-06	7.027e-10
X6_P0	6.440e-06	7.027e-10
X8_P0	7.713e-06	7.027e-10
X13_P0	1.022e-05	8.218e-10
X16_P0	1.250e-05	8.218e-10
X21_P0	1.706e-05	9.409e-10
X25_P0	1.854e-05	9.409e-10
X29_P0	2.243e-05	1.179e-09
X33_P0	2.322e-05	1.179e-09
X42_P0	2.879e-05	1.298e-09
X50_P0	3.452e-05	1.417e-09
X58_P0	4.252e-05	1.655e-09
X67_P0	4.652e-05	1.775e-09
X75_P0	5.053e-05	1.894e-09

X84_P0	5.454e-05	2.013e-09
X100_P0	6.655e-05	2.370e-09
X134_P0	8.658e-05	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	1.260e-03	1.394e-03	1.633e-03	2.139e-03
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	2.543e-03	3.454e-03	3.875e-03	4.348e-03
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	4.758e-03	6.001e-03	6.980e-03	8.633e-03
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	9.448e-03	1.066e-02	1.146e-02	1.388e-02
	X134_P0			
A to Z	1.869e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

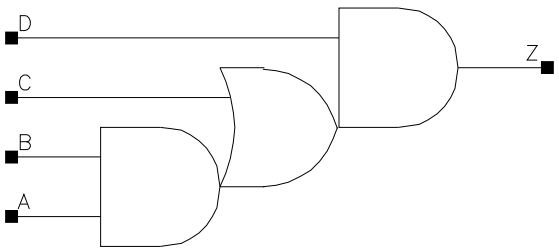
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	-1.248e-07	-9.400e-08	5.200e-09	-4.434e-08
	X16_P0	X21_P0	X25_P0	X29_P0
A to Z	-1.266e-07	-2.048e-07	-2.700e-07	-1.152e-07
	X33_P0	X42_P0	X50_P0	X58_P0
A to Z	-1.134e-07	-2.600e-07	-5.618e-07	-1.840e-07
	X67_P0	X75_P0	X84_P0	X100_P0
A to Z	-3.740e-07	-4.180e-07	-8.120e-07	-1.041e-06
	X134_P0			
A to Z	-1.121e-06			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.632	1.9584
X25_P0	1.200	1.768	2.1216
X33_P0	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0008	0.0018	0.0018	0.0017
B	0.0008	0.0016	0.0016	0.0015
C	0.0009	0.0020	0.0020	0.0020
D	0.0014	0.0017	0.0017	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0421	0.0397	2.2887	1.1376
A to Z ↑	0.0361	0.0338	3.8605	1.8784
B to Z ↓	0.0395	0.0367	2.2815	1.1361
B to Z ↑	0.0359	0.0329	3.8585	1.8759
C to Z ↓	0.0350	0.0320	2.2776	1.1338
C to Z ↑	0.0270	0.0244	3.8227	1.8600

D to Z ↓	0.0328	0.0287	2.2548	1.1243
D to Z ↑	0.0318	0.0275	3.8274	1.8625
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0434	0.0454	0.7760	0.5861
A to Z ↑	0.0368	0.0382	1.2702	0.9548
B to Z ↓	0.0403	0.0431	0.7738	0.5848
B to Z ↑	0.0360	0.0380	1.2700	0.9535
C to Z ↓	0.0358	0.0383	0.7721	0.5829
C to Z ↑	0.0269	0.0284	1.2573	0.9431
D to Z ↓	0.0310	0.0323	0.7628	0.5736
D to Z ↑	0.0299	0.0310	1.2586	0.9455

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	1.062e-05	1.179e-09
X17_P0	1.992e-05	1.775e-09
X25_P0	2.365e-05	1.894e-09
X33_P0	2.740e-05	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	6.258e-05	1.284e-04	1.296e-04	1.170e-04
B (output stable)	7.561e-05	1.606e-04	1.629e-04	1.402e-04
C (output stable)	2.226e-04	3.502e-04	3.542e-04	3.390e-04
D (output stable)	1.073e-04	1.533e-04	1.537e-04	1.530e-04
A to Z	2.752e-03	5.003e-03	6.203e-03	7.037e-03
B to Z	2.581e-03	4.553e-03	5.723e-03	6.662e-03
C to Z	2.161e-03	3.669e-03	4.840e-03	5.711e-03
D to Z	2.819e-03	4.769e-03	5.910e-03	6.710e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

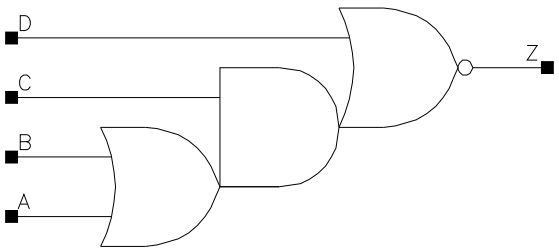
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	-1.182e-07	-2.574e-07	-2.610e-07	-1.705e-07
B (output stable)	-1.263e-07	-2.631e-07	-2.666e-07	-1.809e-07
C (output stable)	4.740e-06	8.612e-06	8.640e-06	8.725e-06
D (output stable)	7.932e-08	3.335e-08	4.072e-08	4.647e-08
A to Z	5.760e-07	1.382e-06	1.275e-06	1.030e-06
B to Z	7.570e-07	1.514e-06	1.727e-06	1.285e-06
C to Z	-2.362e-07	-4.150e-07	-4.610e-07	-4.980e-07
D to Z	-5.458e-07	1.316e-07	-2.254e-07	-3.577e-07

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.952	1.1424
X11_P0	1.200	1.496	1.7952
X16_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X16_P0	X21_P0
A	0.0008	0.0014	0.0022	0.0029
B	0.0008	0.0014	0.0022	0.0028
C	0.0007	0.0014	0.0020	0.0028
D	0.0010	0.0014	0.0020	0.0027

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0169	0.0161	4.0815	2.1492
A to Z ↑	0.0416	0.0383	12.4566	6.4192
B to Z ↓	0.0165	0.0159	3.9968	2.1225
B to Z ↑	0.0392	0.0364	12.4615	6.4213
C to Z ↓	0.0150	0.0141	3.7462	1.9790
C to Z ↑	0.0259	0.0236	8.1436	4.1609

D to Z ↓	0.0097	0.0082	2.2663	1.1535
D to Z ↑	0.0222	0.0190	8.7659	4.4846
	X16_P0	**X21_P0**	**X16_P0**	**X21_P0**
A to Z ↓	0.0162	0.0165	1.4632	1.1196
A to Z ↑	0.0358	0.0378	4.1641	3.1934
B to Z ↓	0.0156	0.0159	1.4686	1.1209
B to Z ↑	0.0349	0.0357	4.1672	3.1956
C to Z ↓	0.0143	0.0144	1.3653	1.0404
C to Z ↑	0.0230	0.0233	2.7559	2.0696
D to Z ↓	0.0082	0.0082	0.8090	0.6175
D to Z ↑	0.0178	0.0178	2.9529	2.2312

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P0	6.785e-06	1.179e-09
X11_P0	1.250e-05	1.655e-09
X16_P0	1.680e-05	1.894e-09
X21_P0	2.228e-05	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	2.785e-05	5.197e-05	6.816e-05	1.127e-04
B (output stable)	2.000e-05	3.819e-05	5.362e-05	7.778e-05
C (output stable)	7.071e-05	1.451e-04	1.998e-04	2.822e-04
D (output stable)	1.643e-04	3.413e-04	4.938e-04	6.730e-04
A to Z	1.978e-03	3.429e-03	4.788e-03	6.773e-03
B to Z	1.629e-03	2.855e-03	4.118e-03	5.594e-03
C to Z	1.388e-03	2.349e-03	3.388e-03	4.668e-03
D to Z	8.499e-04	1.416e-03	1.920e-03	2.557e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

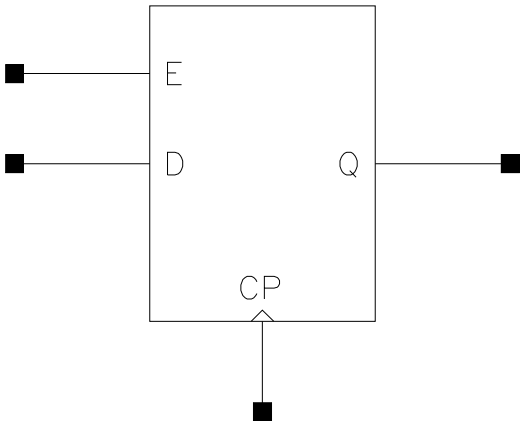
Pin Cycle (vdds)	X5_P0	X11_P0	X16_P0	X21_P0
A (output stable)	-5.515e-09	-2.523e-08	-5.289e-09	-2.426e-07
B (output stable)	6.719e-06	8.977e-06	1.138e-05	2.335e-05
C (output stable)	-7.137e-08	-8.496e-08	-1.110e-07	-3.666e-07
D (output stable)	4.301e-05	8.906e-05	1.189e-04	1.776e-04
A to Z	1.779e-06	2.674e-06	4.409e-06	7.223e-06
B to Z	6.780e-07	1.396e-06	1.802e-06	3.210e-06
C to Z	1.533e-06	2.509e-06	3.183e-06	5.613e-06
D to Z	1.144e-08	5.767e-07	4.314e-07	3.724e-07

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.128	3.7536
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0007	0.0007	0.0007
D	0.0006	0.0006	0.0006
E	0.0010	0.0010	0.0010

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0475	0.0543	2.2758	1.1813
CP to Q ↑	0.0576	0.0609	3.8536	1.9348
	X33_P0		**X33_P0**	
CP to Q ↓	0.0809		0.5828	
CP to Q ↑	0.0979		0.9586	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0702	0.0702	0.0702
CP ↑	min_pulse_width to CP	0.0396	0.0444	0.0359
D ↓	hold_rising to CP	-0.0259	-0.0259	-0.0290
D ↑	hold_rising to CP	-0.0086	-0.0086	-0.0086
D ↓	setup_rising to CP	0.0734	0.0734	0.0734
D ↑	setup_rising to CP	0.0383	0.0383	0.0383
E ↓	hold_rising to CP	-0.0210	-0.0210	-0.0210
E ↑	hold_rising to CP	-0.0086	-0.0086	-0.0086
E ↓	setup_rising to CP	0.0672	0.0672	0.0672
E ↑	setup_rising to CP	0.0782	0.0782	0.0782

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	2.988e-05	2.966e-09
X17_P0	3.418e-05	3.085e-09
X33_P0	4.820e-05	3.561e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

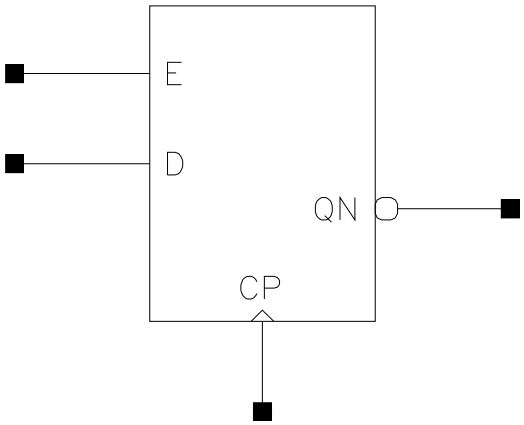
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	2.962e-03	2.963e-03	2.966e-03
Clock 100Mhz Data 25Mhz	6.328e-03	6.830e-03	8.808e-03
Clock 100Mhz Data 50Mhz	9.694e-03	1.070e-02	1.465e-02
Clock = 0 Data 100Mhz	3.777e-03	3.777e-03	3.777e-03
Clock = 1 Data 100Mhz	1.068e-03	1.068e-03	1.068e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.992	3.5904
X17_P0	1.200	3.264	3.9168
X33_P0	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0007	0.0007	0.0007
D	0.0006	0.0006	0.0006
E	0.0008	0.0010	0.0010

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0808	0.0758	2.3355	1.1212
CP to QN ↑	0.0639	0.0656	3.9123	1.8814
	X33_P0		**X33_P0**	
CP to QN ↓	0.0805		0.5846	
CP to QN ↑	0.0719		0.9609	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0702	0.0702	0.0702
CP ↑	min_pulse_width to CP	0.0359	0.0358	0.0407
D ↓	hold_rising to CP	-0.0290	-0.0259	-0.0259
D ↑	hold_rising to CP	-0.0086	-0.0086	-0.0086
D ↓	setup_rising to CP	0.0734	0.0734	0.0734
D ↑	setup_rising to CP	0.0383	0.0383	0.0383
E ↓	hold_rising to CP	-0.0210	-0.0210	-0.0210
E ↑	hold_rising to CP	-0.0086	-0.0086	-0.0086
E ↓	setup_rising to CP	0.0672	0.0672	0.0672
E ↑	setup_rising to CP	0.0782	0.0782	0.0782

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	2.977e-05	2.966e-09
X17_P0	3.683e-05	3.204e-09
X33_P0	4.707e-05	3.561e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

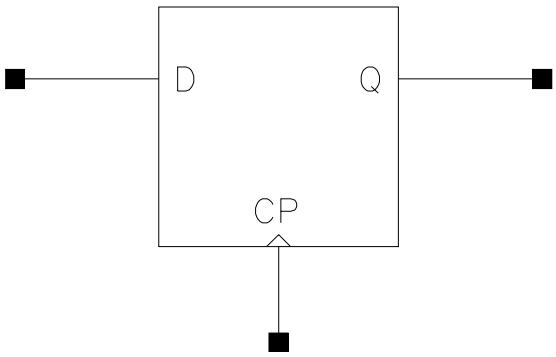
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	2.962e-03	2.962e-03	2.962e-03
Clock 100Mhz Data 25Mhz	6.368e-03	7.232e-03	8.670e-03
Clock 100Mhz Data 50Mhz	9.775e-03	1.150e-02	1.438e-02
Clock = 0 Data 100Mhz	3.777e-03	3.776e-03	3.776e-03
Clock = 1 Data 100Mhz	1.068e-03	1.068e-03	1.068e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.176	2.6112
X17_P0	1.200	2.448	2.9376
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0492	0.0541	2.2694	1.1726
CP to Q ↑	0.0586	0.0645	3.7476	1.9046
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to Q ↓	0.0689	0.0709	0.7022	0.6374
CP to Q ↑	0.0720	0.0735	1.0722	0.9763

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0605	0.0642	0.0642	0.0653
CP ↑	min_pulse_width to CP	0.0396	0.0444	0.0589	0.0626
D ↓	hold_rising to CP	0.0052	0.0056	0.0056	0.0056
D ↑	hold_rising to CP	0.0078	0.0078	0.0078	0.0078
D ↓	setup_rising to CP	0.0395	0.0392	0.0392	0.0392
D ↑	setup_rising to CP	0.0197	0.0197	0.0197	0.0197

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	2.403e-05	2.251e-09
X17_P0	2.871e-05	2.489e-09
X30_P0	3.640e-05	2.727e-09
X33_P0	3.684e-05	2.727e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

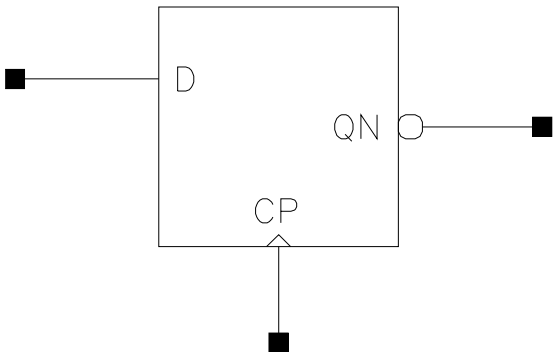
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.116e-03	3.131e-03	3.137e-03	3.139e-03
Clock 100Mhz Data 25Mhz	5.602e-03	6.384e-03	7.576e-03	7.798e-03
Clock 100Mhz Data 50Mhz	8.089e-03	9.636e-03	1.202e-02	1.246e-02
Clock = 0 Data 100Mhz	2.486e-03	2.568e-03	2.593e-03	2.605e-03
Clock = 1 Data 100Mhz	2.322e-05	2.337e-05	2.349e-05	2.355e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X30_P0	1.200	2.720	3.2640
X33_P0	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X30_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0472	0.0560	2.3317	1.2106
CP to QN ↑	0.0508	0.0535	3.7358	1.8992
	X30_P0	**X33_P0**	**X30_P0**	**X33_P0**

CP to QN ↓	0.0809	0.0809	0.6433	0.5828
CP to QN ↑	0.0666	0.0770	1.0364	0.9613

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X17_P0	X30_P0	X33_P0
CP ↓	min_pulse_width to CP	0.0519	0.0519	0.0642	0.0605
CP ↑	min_pulse_width to CP	0.0359	0.0444	0.0359	0.0455
D ↓	hold_rising to CP	0.0123	0.0123	0.0056	0.0049
D ↑	hold_rising to CP	0.0100	0.0100	0.0082	0.0078
D ↓	setup_rising to CP	0.0242	0.0267	0.0392	0.0395
D ↑	setup_rising to CP	0.0219	0.0219	0.0194	0.0197

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	2.252e-05	2.013e-09
X17_P0	2.690e-05	2.132e-09
X30_P0	3.941e-05	2.727e-09
X33_P0	4.123e-05	2.847e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

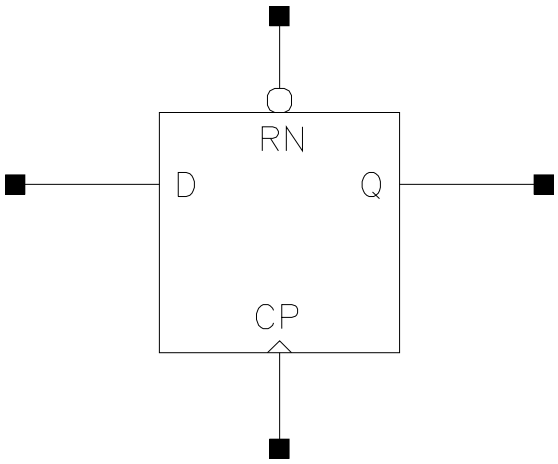
Pin Cycle	X8_P0	X17_P0	X30_P0	X33_P0
Clock 100Mhz Data 0Mhz	2.991e-03	2.992e-03	3.042e-03	3.063e-03
Clock 100Mhz Data 25Mhz	5.302e-03	5.859e-03	7.542e-03	7.922e-03
Clock 100Mhz Data 50Mhz	7.612e-03	8.725e-03	1.204e-02	1.278e-02
Clock = 0 Data 100Mhz	2.220e-03	2.220e-03	2.361e-03	2.393e-03
Clock = 1 Data 100Mhz	2.305e-05	2.310e-05	2.332e-05	2.336e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0008	0.0008
D	0.0006	0.0006
RN	0.0008	0.0008

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0564	0.0704	1.1845	0.7103
CP to Q ↑	0.0667	0.0738	1.9107	1.0761
RN to Q ↓	0.0899	0.1181	1.2636	0.7588

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0690	0.0690
CP ↑	min_pulse_width to CP	0.0455	0.0588
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0051	0.0082
D ↓	setup_rising to CP	0.0444	0.0444
D ↑	setup_rising to CP	0.0271	0.0271
RN ↓	min_pulse_width to RN	0.1143	0.1436
RN ↑	recovery_rising to CP	0.0244	0.0244
RN ↑	removal_rising to CP	-0.0077	-0.0077

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P0	3.045e-05	3.085e-09
X30_P0	3.754e-05	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

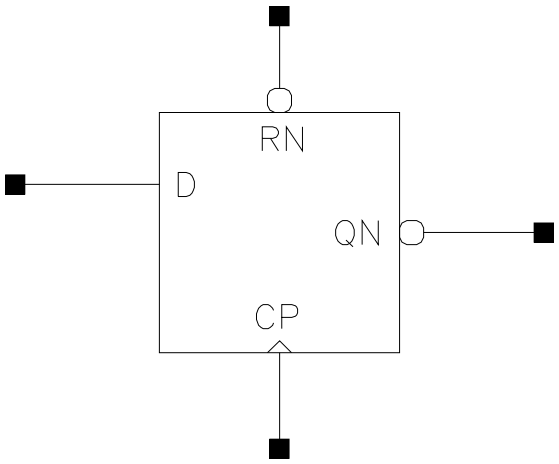
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	3.345e-03	3.345e-03
Clock 100Mhz Data 25Mhz	6.838e-03	7.998e-03
Clock 100Mhz Data 50Mhz	1.033e-02	1.265e-02
Clock = 0 Data 100Mhz	3.088e-03	3.090e-03
Clock = 1 Data 100Mhz	2.367e-05	2.376e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0008	0.0008
D	0.0006	0.0006
RN	0.0008	0.0008

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0784	0.0845	1.1116	0.6460
CP to QN ↑	0.0652	0.0700	1.8662	1.0411
RN to QN ↑	0.0964	0.1028	1.8753	1.0462

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0690	0.0690
CP ↑	min_pulse_width to CP	0.0369	0.0407
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0051	0.0051
D ↓	setup_rising to CP	0.0444	0.0444
D ↑	setup_rising to CP	0.0271	0.0271
RN ↓	min_pulse_width to RN	0.0920	0.0969
RN ↑	recovery_rising to CP	0.0219	0.0219
RN ↑	removal_rising to CP	-0.0077	-0.0077

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P0	3.552e-05	3.085e-09
X30_P0	4.351e-05	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

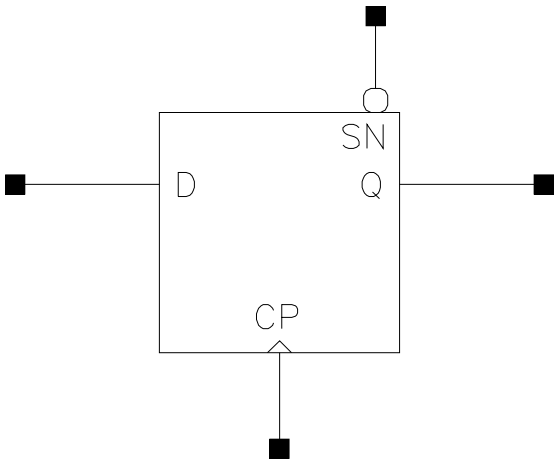
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	3.344e-03	3.343e-03
Clock 100Mhz Data 25Mhz	7.186e-03	8.157e-03
Clock 100Mhz Data 50Mhz	1.103e-02	1.297e-02
Clock = 0 Data 100Mhz	3.125e-03	3.115e-03
Clock = 1 Data 100Mhz	2.370e-05	2.377e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0008	0.0008
D	0.0006	0.0006
SN	0.0010	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to Q ↓	0.0571	0.0715	1.1864	0.7084
CP to Q ↑	0.0661	0.0735	1.9116	1.0754
SN to Q ↑	0.0679	0.0771	1.9186	1.0801

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0701	0.0701
CP ↑	min_pulse_width to CP	0.0455	0.0588
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0082	0.0082
D ↓	setup_rising to CP	0.0462	0.0462
D ↑	setup_rising to CP	0.0219	0.0219
SN ↓	min_pulse_width to SN	0.0669	0.0745
SN ↑	recovery_rising to CP	0.0099	0.0099
SN ↑	removal_rising to CP	0.0308	0.0308

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P0	3.202e-05	3.085e-09
X30_P0	4.014e-05	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

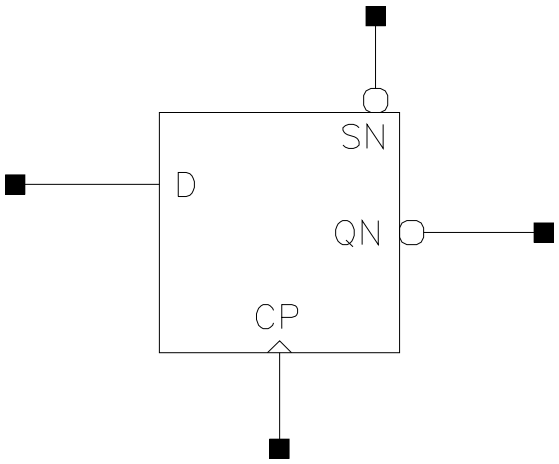
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	3.386e-03	3.379e-03
Clock 100Mhz Data 25Mhz	6.892e-03	8.030e-03
Clock 100Mhz Data 50Mhz	1.040e-02	1.268e-02
Clock = 0 Data 100Mhz	3.075e-03	3.075e-03
Clock = 1 Data 100Mhz	2.374e-05	2.380e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	3.128	3.7536
X30_P0	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P0	X30_P0
CP	0.0008	0.0008
D	0.0006	0.0006
SN	0.0011	0.0011

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X30_P0	X17_P0	X30_P0
CP to QN ↓	0.0779	0.0839	1.1144	0.6464
CP to QN ↑	0.0659	0.0706	1.8635	1.0378
SN to QN ↓	0.0797	0.0860	1.1145	0.6471

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P0	X30_P0
CP ↓	min_pulse_width to CP	0.0701	0.0701
CP ↑	min_pulse_width to CP	0.0407	0.0407
D ↓	hold_rising to CP	0.0056	0.0056
D ↑	hold_rising to CP	0.0082	0.0082
D ↓	setup_rising to CP	0.0493	0.0493
D ↑	setup_rising to CP	0.0219	0.0219
SN ↓	min_pulse_width to SN	0.0593	0.0593
SN ↑	recovery_rising to CP	0.0100	0.0100
SN ↑	removal_rising to CP	0.0308	0.0308

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P0	3.345e-05	3.085e-09
X30_P0	4.029e-05	3.323e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

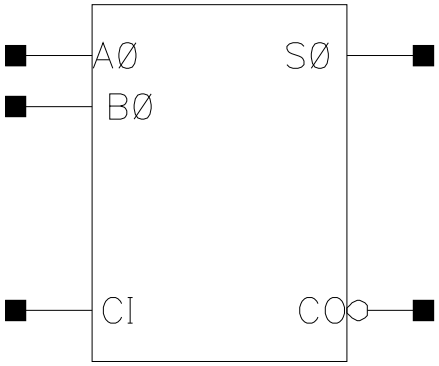
Pin Cycle	X17_P0	X30_P0
Clock 100Mhz Data 0Mhz	3.381e-03	3.380e-03
Clock 100Mhz Data 25Mhz	7.214e-03	8.177e-03
Clock 100Mhz Data 50Mhz	1.105e-02	1.297e-02
Clock = 0 Data 100Mhz	3.076e-03	3.076e-03
Clock = 1 Data 100Mhz	2.380e-05	2.388e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_P0	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_P0	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_P0	1.200	3.672	4.4064
C12T28SOI_LRS1_FA1X33_P0	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_FA1X8_P0	C12T28SOI_LR_FA1X33_P0	C12T28SOI_LRS1_FA1X8_P0	C12T28SOI_LRS1_FA1X33_P0
A0	0.0028	0.0057	0.0026	0.0051
B0	0.0026	0.0056	0.0028	0.0049
CI	0.0019	0.0043	0.0019	0.0034

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0
A0 to CO ↓	0.0555	0.0595	2.3588	0.6288
A0 to CO ↑	0.0387	0.0391	3.8592	0.9918
A0 to S0 ↓	0.0565	0.0706	2.3426	0.6155
A0 to S0 ↑	0.0579	0.0695	3.8236	0.9787
B0 to CO ↓	0.0540	0.0591	2.3664	0.6322
B0 to CO ↑	0.0393	0.0401	3.8601	0.9881
B0 to S0 ↓	0.0564	0.0711	2.3438	0.6153
B0 to S0 ↑	0.0576	0.0699	3.8251	0.9791
CI to CO ↓	0.0513	0.0566	2.3728	0.6314
CI to CO ↑	0.0385	0.0385	3.8575	0.9913
CI to S0 ↓	0.0553	0.0699	2.3425	0.6155
CI to S0 ↑	0.0570	0.0695	3.8244	0.9783
	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0
A0 to CO ↓	0.0360	0.0435	4.8829	0.8495
A0 to CO ↑	0.0288	0.0324	3.9048	0.9782
A0 to S0 ↓	0.0753	0.0913	2.5073	0.6395
A0 to S0 ↑	0.0687	0.0734	3.9795	0.9934
B0 to CO ↓	0.0363	0.0441	4.8829	0.8502
B0 to CO ↑	0.0274	0.0315	3.9015	0.9779
B0 to S0 ↓	0.0755	0.0933	2.5081	0.6395
B0 to S0 ↑	0.0688	0.0752	3.9772	0.9935
CI to CO ↓	0.0352	0.0582	4.8757	0.8620
CI to CO ↑	0.0309	0.0358	3.9928	0.9849
CI to S0 ↓	0.0424	0.0541	2.5097	0.6400
CI to S0 ↑	0.0362	0.0357	3.9744	0.9935

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_FA1X8_P0	2.464e-05	2.251e-09
C12T28SOI_LR_FA1X33_P0	6.534e-05	4.633e-09
C12T28SOI_LRS1_FA1X8_P0	5.617e-05	3.561e-09
C12T28SOI_LRS1_FA1X33_P0	1.160e-04	7.372e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0
A0 to CO	2.841e-03	7.953e-03	4.438e-03	1.079e-02
A0 to S0	2.881e-03	8.344e-03	5.958e-03	1.341e-02
B0 to CO	2.871e-03	8.081e-03	4.450e-03	1.091e-02
B0 to S0	2.828e-03	8.281e-03	6.022e-03	1.368e-02
CI to CO	2.875e-03	8.112e-03	3.149e-03	9.583e-03
CI to S0	2.804e-03	8.227e-03	3.540e-03	1.029e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P0	C12T28SOI_LR_-FA1X33_P0	C12T28SOI_LRS1_-FA1X8_P0	C12T28SOI_LRS1_-FA1X33_P0
A0 to CO	-2.360e-08	6.100e-08	-1.650e-09	2.475e-08

A0 to S0	1.008e-07	6.868e-07	-1.207e-07	-3.176e-07
B0 to CO	1.653e-07	2.920e-07	-1.845e-08	1.536e-07
B0 to S0	5.144e-06	9.707e-06	8.834e-07	2.114e-06
CI to CO	7.605e-06	1.452e-05	-3.725e-08	-4.583e-07
CI to S0	1.014e-05	1.437e-05	-2.597e-07	-6.176e-07

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X33_P0	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P0	X33_P0
A0	0.0010	0.0028
B0	0.0009	0.0025

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
A0 to CO ↓	0.0393	0.0357	2.3333	0.5805
A0 to CO ↑	0.0364	0.0322	3.8257	0.9801
A0 to S0 ↓	0.0524	0.0492	2.2899	0.5808
A0 to S0 ↑	0.0489	0.0528	3.7779	0.9699
B0 to CO ↓	0.0383	0.0333	2.3315	0.5763
B0 to CO ↑	0.0379	0.0327	3.8244	0.9802
B0 to S0 ↓	0.0531	0.0477	2.2902	0.5809
B0 to S0 ↑	0.0483	0.0508	3.7784	0.9702

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	1.524e-05	1.417e-09
X33_P0	5.823e-05	2.966e-09

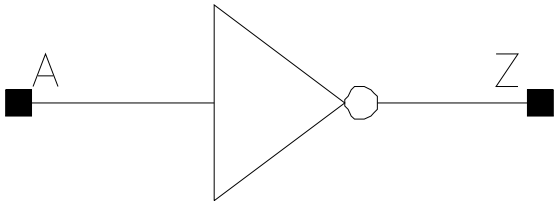
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X33_P0
A0 to CO	2.186e-03	7.114e-03
A0 to S0	2.018e-03	6.934e-03
B0 to CO	2.223e-03	7.232e-03
B0 to S0	1.983e-03	6.646e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X8_P0	X33_P0
A0 to CO	-4.636e-08	-1.243e-07
A0 to S0	-5.853e-08	6.235e-08
B0 to CO	3.020e-07	9.809e-06
B0 to S0	1.050e-07	4.701e-06

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.272	0.3264
X6_P0	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X13_P0	1.200	0.408	0.4896
X17_P0	1.200	0.408	0.4896
X21_P0	1.200	0.544	0.6528
X25_P0	1.200	0.544	0.6528
X29_P0	1.200	0.680	0.8160
X33_P0	1.200	0.680	0.8160
X50_P0	1.200	0.952	1.1424
X58_P0	1.200	1.088	1.3056
X67_P0	1.200	1.224	1.4688
X75_P0	1.200	1.360	1.6320
X84_P0	1.200	1.496	1.7952
X100_P0	1.200	1.768	2.1216
X134_P0	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X13_P0
A	0.0005	0.0006	0.0007	0.0011
	X17_P0	X21_P0	X25_P0	X29_P0
A	0.0014	0.0018	0.0021	0.0025
	X33_P0	X50_P0	X58_P0	X67_P0
A	0.0027	0.0041	0.0048	0.0055
	X75_P0	X84_P0	X100_P0	X134_P0

A	0.0063	0.0071	0.0087	0.0121

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0091	0.0084	4.3527	3.3518
A to Z ↑	0.0155	0.0142	7.4884	5.6173
	X8_P0	**X13_P0**	**X8_P0**	**X13_P0**
A to Z ↓	0.0074	0.0064	2.2684	1.4768
A to Z ↑	0.0129	0.0117	3.8573	2.5544
	X17_P0	**X21_P0**	**X17_P0**	**X21_P0**
A to Z ↓	0.0062	0.0068	1.1289	0.9103
A to Z ↑	0.0111	0.0118	1.9008	1.5310
	X25_P0	**X29_P0**	**X25_P0**	**X29_P0**
A to Z ↓	0.0067	0.0063	0.7755	0.6600
A to Z ↑	0.0114	0.0109	1.2780	1.0930
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0062	0.0063	0.5845	0.3953
A to Z ↑	0.0106	0.0106	0.9578	0.6416
	X58_P0	**X67_P0**	**X58_P0**	**X67_P0**
A to Z ↓	0.0068	0.0066	0.3429	0.3014
A to Z ↑	0.0110	0.0107	0.5526	0.4834
	X75_P0	**X84_P0**	**X75_P0**	**X84_P0**
A to Z ↓	0.0071	0.0071	0.2718	0.2458
A to Z ↑	0.0112	0.0111	0.4332	0.3919
	X100_P0	**X134_P0**	**X100_P0**	**X134_P0**
A to Z ↓	0.0076	0.0083	0.2090	0.1624
A to Z ↑	0.0115	0.0121	0.3302	0.2530

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.783e-06	5.836e-10
X6_P0	3.544e-06	5.836e-10
X8_P0	5.100e-06	5.836e-10
X13_P0	7.888e-06	7.027e-10
X17_P0	1.002e-05	7.027e-10
X21_P0	1.254e-05	8.218e-10
X25_P0	1.414e-05	8.218e-10
X29_P0	1.702e-05	9.409e-10
X33_P0	1.814e-05	9.409e-10
X50_P0	2.614e-05	1.179e-09
X58_P0	3.014e-05	1.298e-09
X67_P0	3.414e-05	1.417e-09
X75_P0	3.815e-05	1.536e-09
X84_P0	4.215e-05	1.655e-09
X100_P0	5.017e-05	1.894e-09
X134_P0	6.619e-05	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X13_P0

A to Z	3.658e-04	4.388e-04	5.486e-04	7.416e-04
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	9.222e-04	1.293e-03	1.462e-03	1.603e-03
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	1.734e-03	2.579e-03	3.199e-03	3.442e-03
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	4.044e-03	4.331e-03	5.180e-03	7.043e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

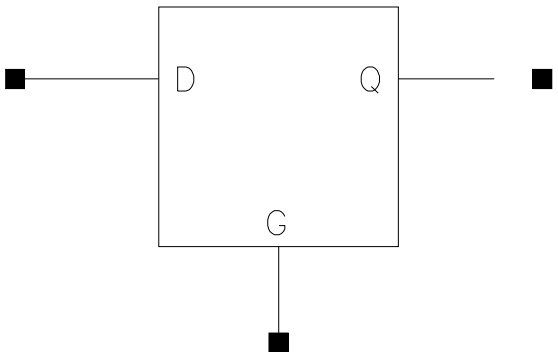
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X13_P0
A to Z	1.352e-07	3.750e-08	5.951e-07	9.232e-07
	X17_P0	X21_P0	X25_P0	X29_P0
A to Z	1.839e-06	2.300e-06	3.919e-06	2.505e-06
	X33_P0	X50_P0	X58_P0	X67_P0
A to Z	2.227e-06	3.505e-06	7.285e-06	6.709e-06
	X75_P0	X84_P0	X100_P0	X134_P0
A to Z	8.649e-06	8.256e-06	7.668e-06	7.678e-06

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X23_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P0	X23_P0
D	0.0005	0.0012
G	0.0011	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X23_P0	X8_P0	X23_P0
D to Q ↓	0.0621	0.0488	2.3937	1.1384
D to Q ↑	0.0385	0.0382	3.7742	0.9999
G to Q ↓	0.0648	0.0498	2.3900	1.1387
G to Q ↑	0.0368	0.0334	3.7776	1.0016

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X23_P0
D ↓	hold_falling to G	-0.0162	-0.0035
D ↑	hold_falling to G	-0.0024	-0.0054
D ↓	setup_falling to G	0.0608	0.0411
D ↑	setup_falling to G	0.0400	0.0448
G ↑	min_pulse_width to G	0.0541	0.0465

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	1.328e-05	1.417e-09
X23_P0	2.706e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X23_P0
D (output stable)	1.623e-05	6.787e-05
G (output stable)	7.522e-04	1.466e-03
D to Q	3.465e-03	6.690e-03
G to Q	3.237e-03	5.994e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

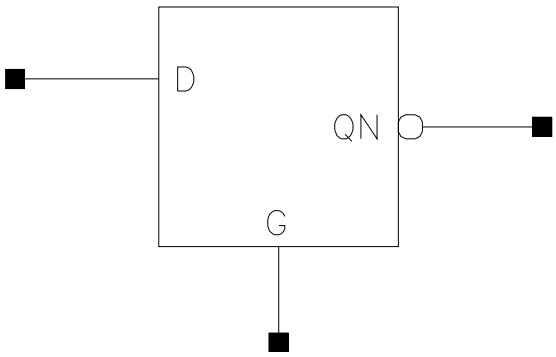
Pin Cycle (vdds)	X8_P0	X23_P0
D (output stable)	9.158e-08	1.702e-07
G (output stable)	4.547e-06	1.477e-05
D to Q	4.300e-09	-3.398e-07
G to Q	3.917e-05	1.957e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P0
D	0.0005
G	0.0012

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P0	X17_P0
D to QN ↓	0.0506	1.1162
D to QN ↑	0.0686	1.8516
G to QN ↓	0.0484	1.1163
G to QN ↑	0.0685	1.8538

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X17_P0
D ↓	hold_falling to G	-0.0241
D ↑	hold_falling to G	-0.0054
D ↓	setup_falling to G	0.0486
D ↑	setup_falling to G	0.0351
G ↑	min_pulse_width to G	0.0443

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P0	2.012e-05	1.536e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X17_P0
D (output stable)	1.646e-05
G (output stable)	8.422e-04
D to QN	4.304e-03
G to QN	3.999e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

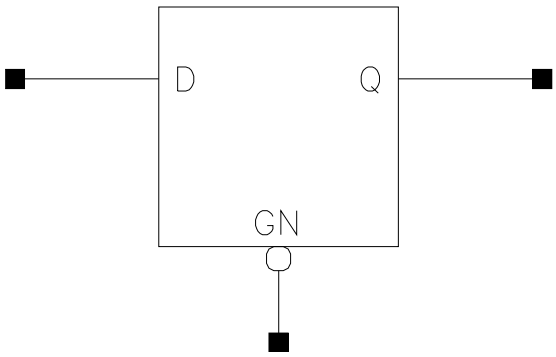
Pin Cycle (vdds)	X17_P0
D (output stable)	1.044e-07
G (output stable)	4.583e-06
D to QN	-7.230e-08
G to QN	6.825e-05

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X33_P0	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
D	0.0005	0.0007	0.0015
GN	0.0010	0.0013	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D to Q ↓	0.0628	0.0539	2.4020	1.1791
D to Q ↑	0.0393	0.0359	3.7776	1.9324
GN to Q ↓	0.0559	0.0469	2.4037	1.1798
GN to Q ↑	0.0583	0.0552	3.7754	1.9303

	X33_P0		X33_P0	
D to Q ↓	0.0515		0.6017	
D to Q ↑	0.0305		0.9677	
GN to Q ↓	0.0439		0.6026	
GN to Q ↑	0.0424		0.9679	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X17_P0	X33_P0
D ↓	hold_rising to GN	-0.0216	-0.0140	-0.0118
D ↑	hold_rising to GN	0.0011	0.0029	0.0054
D ↓	setup_rising to GN	0.0685	0.0616	0.0567
D ↑	setup_rising to GN	0.0365	0.0316	0.0264
GN ↓	min_pulse_width to GN	0.0732	0.0627	0.0580

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	1.245e-05	1.417e-09
X17_P0	1.945e-05	1.655e-09
X33_P0	3.209e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
D (output stable)	1.614e-05	2.713e-05	7.402e-05
GN (output stable)	7.512e-04	1.043e-03	1.253e-03
D to Q	3.480e-03	4.849e-03	7.783e-03
GN to Q	4.945e-03	6.697e-03	9.725e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

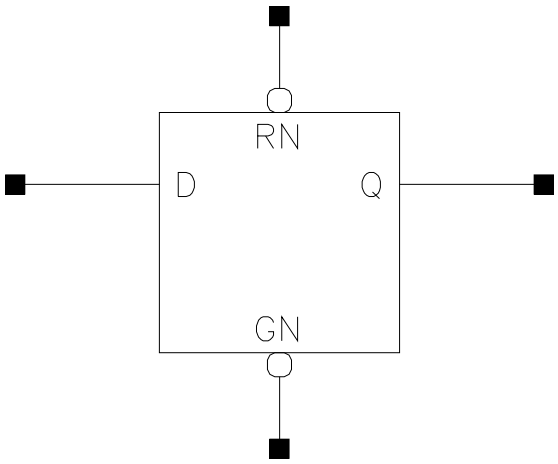
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
D (output stable)	9.899e-08	1.273e-07	2.263e-07
GN (output stable)	4.739e-06	5.211e-06	1.337e-05
D to Q	2.660e-08	-1.570e-07	-1.521e-07
GN to Q	-4.168e-05	-2.370e-05	-3.299e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.496	1.7952
X33_P0	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P0	X33_P0
D	0.0005	0.0012
GN	0.0012	0.0022
RN	0.0005	0.0006

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X33_P0	X8_P0	X33_P0
D to Q ↓	0.0586	0.0521	2.3310	0.6068
D to Q ↑	0.0504	0.0619	3.8409	1.0013

GN to Q ↓	0.0526	0.0478	2.3322	0.6072
GN to Q ↑	0.0666	0.0673	3.8467	1.0013
RN to Q ↓	0.0442	0.0795	2.2416	0.6613
RN to Q ↑	0.0536	0.0676	3.8428	1.0014

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X33_P0
D ↓	hold_rising to GN	-0.0192	-0.0118
D ↑	hold_rising to GN	-0.0086	-0.0233
D ↓	setup_rising to GN	0.0616	0.0537
D ↑	setup_rising to GN	0.0487	0.0682
GN ↓	min_pulse_width to GN	0.0674	0.0692
RN ↓	min_pulse_width to RN	0.0540	0.0947
RN ↑	recovery_rising to GN	0.0511	0.0752
RN ↑	removal_rising to GN	-0.0313	-0.0508

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	1.197e-05	1.655e-09
X33_P0	2.763e-05	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X33_P0
D (output stable)	5.977e-05	1.078e-04
GN (output stable)	8.642e-04	1.303e-03
RN (output stable)	4.230e-05	7.524e-05
D to Q	3.425e-03	8.661e-03
GN to Q	5.008e-03	1.105e-02
RN to Q	2.651e-03	6.815e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

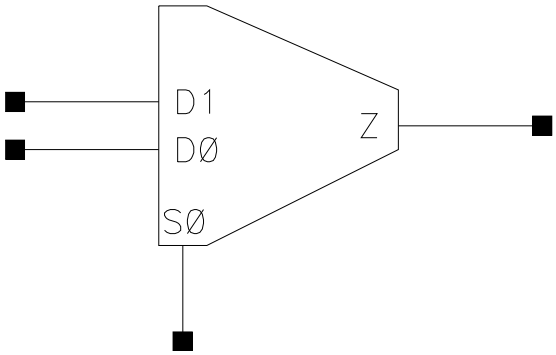
Pin Cycle (vdds)	X8_P0	X33_P0
D (output stable)	-2.269e-07	-3.084e-07
GN (output stable)	1.857e-06	3.091e-06
RN (output stable)	9.087e-08	1.354e-07
D to Q	4.274e-08	-3.713e-07
GN to Q	-3.926e-05	2.434e-05
RN to Q	2.830e-06	-1.625e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
D0	0.0007	0.0010	0.0012	0.0017
D1	0.0007	0.0009	0.0013	0.0017
S0	0.0012	0.0013	0.0015	0.0022

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
D0 to Z ↓	0.0471	0.0417	2.3295	1.1443
D0 to Z ↑	0.0365	0.0327	3.8653	1.8903
D1 to Z ↓	0.0448	0.0413	2.3224	1.1425
D1 to Z ↑	0.0333	0.0307	3.8562	1.8881
S0 to Z ↓	0.0402	0.0384	2.3178	1.1399
S0 to Z ↑	0.0377	0.0371	3.8572	1.8868

	X25_P0	X33_P0	X25_P0	X33_P0
D0 to Z ↓	0.0443	0.0399	0.7884	0.5916
D0 to Z ↑	0.0355	0.0323	1.2705	0.9501
D1 to Z ↓	0.0472	0.0415	0.7916	0.5923
D1 to Z ↑	0.0338	0.0310	1.2692	0.9506
S0 to Z ↓	0.0440	0.0401	0.7879	0.5908
S0 to Z ↑	0.0415	0.0376	1.2691	0.9506

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	1.553e-05	1.417e-09
X17_P0	2.643e-05	1.536e-09
X25_P0	3.644e-05	2.370e-09
X33_P0	5.013e-05	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	7.053e-04	1.024e-03	1.112e-03	1.501e-03
D1 (output stable)	5.687e-04	9.444e-04	1.248e-03	1.577e-03
S0 (output stable)	9.031e-04	1.013e-03	1.305e-03	1.601e-03
D0 to Z	2.401e-03	3.865e-03	5.963e-03	7.447e-03
D1 to Z	2.191e-03	3.741e-03	6.014e-03	7.357e-03
S0 to Z	2.751e-03	4.108e-03	6.685e-03	8.134e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

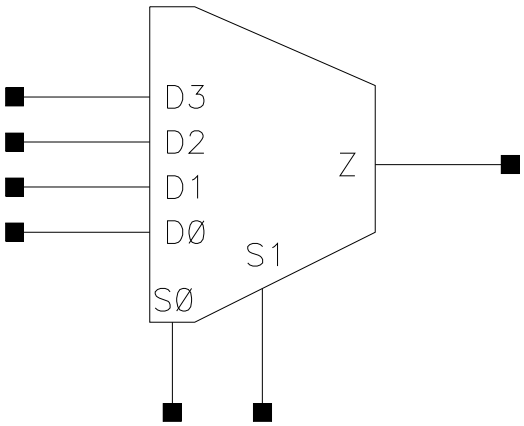
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
D0 (output stable)	7.975e-08	1.016e-07	1.680e-07	3.111e-07
D1 (output stable)	1.099e-07	1.778e-07	2.892e-07	1.540e-07
S0 (output stable)	-4.455e-08	-3.295e-08	-9.465e-08	6.820e-08
D0 to Z	-1.979e-07	-2.145e-07	-1.649e-07	-9.450e-08
D1 to Z	-1.160e-07	-1.040e-08	-1.555e-08	-2.025e-07
S0 to Z	-1.601e-07	-2.044e-07	7.005e-08	-2.022e-07

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	2.312	2.7744
X31_P0	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P0	X31_P0
D0	0.0005	0.0013
D1	0.0005	0.0012
D2	0.0005	0.0013
D3	0.0005	0.0013
S0	0.0017	0.0033
S1	0.0011	0.0022

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X31_P0	X8_P0	X31_P0

D0 to Z ↓	0.0844	0.0851	2.4647	0.6834
D0 to Z ↑	0.0520	0.0522	3.8974	1.0473
D1 to Z ↓	0.0837	0.0854	2.4626	0.6837
D1 to Z ↑	0.0523	0.0520	3.8984	1.0475
D2 to Z ↓	0.0910	0.0793	2.4833	0.6760
D2 to Z ↑	0.0549	0.0484	3.9108	1.0392
D3 to Z ↓	0.0907	0.0789	2.4829	0.6751
D3 to Z ↑	0.0543	0.0495	3.9076	1.0431
S0 to Z ↓	0.0923	0.0908	2.4695	0.6791
S0 to Z ↑	0.0651	0.0654	3.9052	1.0456
S1 to Z ↓	0.0663	0.0623	2.4731	0.6795
S1 to Z ↑	0.0505	0.0502	3.9055	1.0451

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	1.460e-05	2.370e-09
X31_P0	4.181e-05	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X31_P0
D0 (output stable)	1.625e-05	8.313e-05
D1 (output stable)	1.750e-05	9.540e-05
D2 (output stable)	2.082e-05	8.404e-05
D3 (output stable)	2.189e-05	1.037e-04
S0 (output stable)	1.298e-03	2.896e-03
S1 (output stable)	1.021e-03	2.176e-03
D0 to Z	2.600e-03	8.767e-03
D1 to Z	2.587e-03	8.817e-03
D2 to Z	2.801e-03	8.180e-03
D3 to Z	2.792e-03	8.177e-03
S0 to Z	4.030e-03	1.166e-02
S1 to Z	3.061e-03	8.637e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

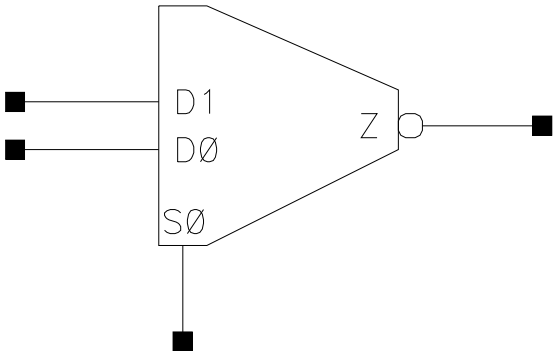
Pin Cycle (vdds)	X8_P0	X31_P0
D0 (output stable)	2.409e-06	1.011e-05
D1 (output stable)	2.376e-06	8.500e-06
D2 (output stable)	2.138e-06	1.015e-05
D3 (output stable)	2.136e-06	8.638e-06
S0 (output stable)	-2.531e-07	-9.383e-07
S1 (output stable)	4.426e-05	1.368e-04
D0 to Z	1.479e-06	2.703e-06
D1 to Z	1.437e-06	4.295e-06
D2 to Z	2.157e-06	1.815e-06
D3 to Z	2.184e-06	3.208e-06
S0 to Z	1.530e-06	2.335e-06
S1 to Z	3.299e-05	1.096e-04

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.816	0.9792
X5_P0	1.200	0.952	1.1424
X10_P0	1.200	1.768	2.1216
X16_P0	1.200	2.448	2.9376
X21_P0	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P0	X5_P0	X10_P0	X16_P0
D0	0.0005	0.0007	0.0014	0.0022
D1	0.0005	0.0007	0.0014	0.0021
S0	0.0010	0.0018	0.0024	0.0034
	X21_P0			
D0	0.0029			
D1	0.0028			
S0	0.0040			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X5_P0	X3_P0	X5_P0
D0 to Z ↓	0.0162	0.0158	8.0810	4.8107

D0 to Z ↑	0.0287	0.0259	17.8113	9.0328
D1 to Z ↓	0.0160	0.0152	7.9938	4.6150
D1 to Z ↑	0.0298	0.0270	17.8250	9.2974
S0 to Z ↓	0.0245	0.0200	8.0122	4.7079
S0 to Z ↑	0.0272	0.0221	17.7989	9.1513
	X10_P0	**X16_P0**	**X10_P0**	**X16_P0**
D0 to Z ↓	0.0176	0.0164	2.2509	1.4745
D0 to Z ↑	0.0282	0.0267	4.1860	2.7546
D1 to Z ↓	0.0161	0.0158	2.1884	1.4508
D1 to Z ↑	0.0282	0.0275	4.2373	2.7796
S0 to Z ↓	0.0243	0.0210	2.2139	1.4598
S0 to Z ↑	0.0262	0.0226	4.2075	2.7664
	X21_P0		**X21_P0**	
D0 to Z ↓	0.0162		1.1233	
D0 to Z ↑	0.0262		2.0843	
D1 to Z ↓	0.0158		1.1009	
D1 to Z ↑	0.0275		2.0747	
S0 to Z ↓	0.0219		1.1092	
S0 to Z ↑	0.0231		2.0782	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P0	5.687e-06	1.060e-09
X5_P0	1.145e-05	1.179e-09
X10_P0	1.952e-05	1.894e-09
X16_P0	2.980e-05	2.489e-09
X21_P0	3.632e-05	3.085e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	1.619e-05	3.759e-05	1.095e-04	1.687e-04
D1 (output stable)	1.611e-05	3.878e-05	9.326e-05	1.631e-04
S0 (output stable)	7.525e-04	1.087e-03	1.888e-03	2.934e-03
D0 to Z	7.245e-04	1.213e-03	3.023e-03	4.209e-03
D1 to Z	7.262e-04	1.208e-03	2.862e-03	4.175e-03
S0 to Z	1.327e-03	1.929e-03	4.012e-03	5.626e-03
	X21_P0			
D0 (output stable)	2.187e-04			
D1 (output stable)	2.164e-04			
S0 (output stable)	3.241e-03			
D0 to Z	5.387e-03			
D1 to Z	5.506e-03			
S0 to Z	6.862e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X3_P0	X5_P0	X10_P0	X16_P0
D0 (output stable)	9.482e-08	1.558e-07	2.070e-07	2.868e-07
D1 (output stable)	9.190e-08	1.889e-07	2.433e-07	2.676e-07
S0 (output stable)	4.790e-06	2.083e-05	2.260e-05	4.679e-05
D0 to Z	1.291e-07	2.629e-07	6.930e-07	9.840e-07

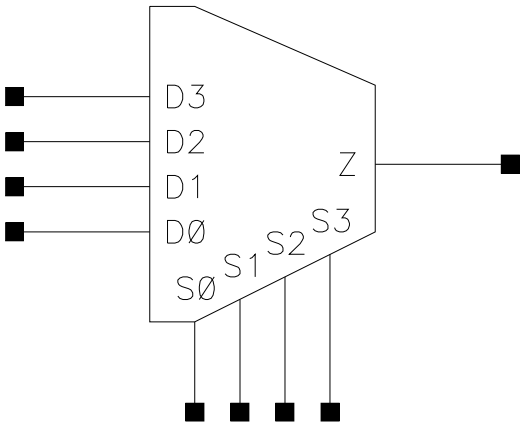
D1 to Z	4.750e-09	3.845e-07	1.028e-06	2.995e-07
S0 to Z	1.194e-06	9.972e-06	5.511e-06	1.849e-05
	X21_P0			
D0 (output stable)	2.707e-07			
D1 (output stable)	4.471e-07			
S0 (output stable)	7.026e-05			
D0 to Z	1.510e-06			
D1 to Z	7.970e-07			
S0 to Z	2.360e-05			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	1.768	2.1216
X27_P0	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P0	X27_P0
D0	0.0006	0.0017
D1	0.0006	0.0018
D2	0.0006	0.0017
D3	0.0006	0.0018
S0	0.0006	0.0016
S1	0.0006	0.0017
S2	0.0006	0.0016
S3	0.0006	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	X27_P0	X7_P0	X27_P0
D0 to Z ↓	0.0640	0.0525	4.0555	1.1077
D0 to Z ↑	0.0438	0.0357	3.7950	0.9458
D1 to Z ↓	0.0574	0.0470	4.0528	1.1070
D1 to Z ↑	0.0398	0.0318	3.7792	0.9404
D2 to Z ↓	0.0644	0.0501	4.0659	1.1100
D2 to Z ↑	0.0432	0.0337	3.8070	0.9495
D3 to Z ↓	0.0578	0.0445	4.0599	1.1080
D3 to Z ↑	0.0393	0.0297	3.7925	0.9438
S0 to Z ↓	0.0623	0.0499	4.0531	1.1074
S0 to Z ↑	0.0456	0.0367	3.7964	0.9455
S1 to Z ↓	0.0560	0.0444	4.0491	1.1068
S1 to Z ↑	0.0415	0.0324	3.7794	0.9415
S2 to Z ↓	0.0626	0.0474	4.0601	1.1083
S2 to Z ↑	0.0451	0.0346	3.8093	0.9495
S3 to Z ↓	0.0565	0.0419	4.0555	1.1069
S3 to Z ↑	0.0410	0.0304	3.7947	0.9451

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X7_P0	1.286e-05	1.894e-09
X27_P0	4.650e-05	3.561e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X7_P0	X27_P0
D0 (output stable)	3.942e-04	1.221e-03
D1 (output stable)	3.271e-04	9.889e-04
D2 (output stable)	3.689e-04	1.156e-03
D3 (output stable)	3.020e-04	9.150e-04
S0 (output stable)	3.838e-04	1.156e-03
S1 (output stable)	3.147e-04	9.338e-04
S2 (output stable)	3.587e-04	1.090e-03
S3 (output stable)	2.894e-04	8.609e-04
D0 to Z	3.057e-03	9.207e-03
D1 to Z	2.682e-03	7.937e-03
D2 to Z	2.995e-03	8.150e-03
D3 to Z	2.625e-03	6.850e-03
S0 to Z	2.990e-03	8.768e-03
S1 to Z	2.616e-03	7.532e-03
S2 to Z	2.927e-03	7.686e-03
S3 to Z	2.557e-03	6.447e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

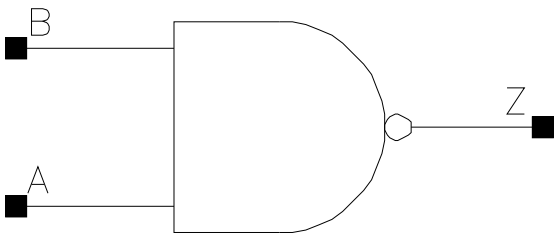
Pin Cycle (vdds)	X7_P0	X27_P0
D0 (output stable)	1.360e-07	5.611e-07
D1 (output stable)	7.140e-06	1.470e-05
D2 (output stable)	1.235e-07	5.114e-07
D3 (output stable)	6.885e-06	1.455e-05
S0 (output stable)	1.727e-07	6.054e-07
S1 (output stable)	7.254e-06	1.478e-05
S2 (output stable)	1.686e-07	6.025e-07
S3 (output stable)	7.095e-06	1.452e-05
D0 to Z	5.520e-07	1.816e-06
D1 to Z	-1.722e-07	-7.972e-07
D2 to Z	7.351e-07	2.023e-06
D3 to Z	-6.203e-08	-5.785e-07
S0 to Z	7.714e-07	2.252e-06
S1 to Z	-1.427e-07	-5.497e-07
S2 to Z	9.746e-07	2.739e-06
S3 to Z	5.175e-08	-2.292e-07

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P0	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P0	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P0	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P0	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P0	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P0	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P0	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P0	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P0	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P0	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P0	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P0	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P0	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P0	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P0	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P0	C12T28SOI_LR_-NAND2X5_P0	C12T28SOI_LR_-NAND2X7_P0	C12T28SOI_LR_-NAND2X10_P0
A	0.0005	0.0006	0.0007	0.0011
B	0.0005	0.0006	0.0007	0.0011
	C12T28SOI_LR_-NAND2X13_P0	C12T28SOI_LR_-NAND2X17_P0	C12T28SOI_LR_-NAND2X20_P0	C12T28SOI_LR_-NAND2X24_P0
A	0.0014	0.0018	0.0021	0.0026
B	0.0013	0.0017	0.0020	0.0024
	C12T28SOI_LR_-NAND2X27_P0	C12T28SOI_LR_-NAND2X42_P0	C12T28SOI_LR_-NAND2X47_P0	C12T28SOI_LR_-NAND2X50_P0
A	0.0028	0.0009	0.0009	0.0009
B	0.0026	0.0009	0.0009	0.0009
	C12T28SOI_LR_-NAND2X58_P0	C12T28SOI_LR_-NAND2X67_P0	C12T28SOI_-LRBR0D8_-NAND2X7_P0	C12T28SOI_-LRBR0D8_-NAND2X14_P0
A	0.0009	0.0009	0.0007	0.0014
B	0.0009	0.0009	0.0007	0.0013
	C12T28SOI_LRS_-NAND2X40_P0	C12T28SOI_LRS_-NAND2X54_P0		
A	0.0042	0.0056		
B	0.0039	0.0053		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P0	**C12T28SOI_LR_-NAND2X5_P0**	**C12T28SOI_LR_-NAND2X3_P0**	**C12T28SOI_LR_-NAND2X5_P0**
A to Z ↓	0.0126	0.0112	7.8238	4.9493
A to Z ↑	0.0179	0.0162	7.5046	4.7602
B to Z ↓	0.0131	0.0113	7.8986	4.9961
B to Z ↑	0.0167	0.0146	7.5397	4.7841
	C12T28SOI_LR_-NAND2X7_P0	**C12T28SOI_LR_-NAND2X10_P0**	**C12T28SOI_LR_-NAND2X7_P0**	**C12T28SOI_LR_-NAND2X10_P0**
A to Z ↓	0.0111	0.0127	4.1454	2.7713
A to Z ↑	0.0157	0.0169	3.8398	2.5270
B to Z ↓	0.0110	0.0111	4.1788	2.7970
B to Z ↑	0.0141	0.0140	3.8720	2.5434
	C12T28SOI_LR_-NAND2X13_P0	**C12T28SOI_LR_-NAND2X17_P0**	**C12T28SOI_LR_-NAND2X13_P0**	**C12T28SOI_LR_-NAND2X17_P0**
A to Z ↓	0.0122	0.0121	2.1186	1.6888

A to Z ↑	0.0160	0.0161	1.8878	1.5233
B to Z ↓	0.0106	0.0110	2.1390	1.7031
B to Z ↑	0.0131	0.0137	1.9006	1.5331
	C12T28SOI_LR_-NAND2X20_P0	**C12T28SOI_LR_-NAND2X24_P0**	**C12T28SOI_LR_-NAND2X20_P0**	**C12T28SOI_LR_-NAND2X24_P0**
A to Z ↓	0.0119	0.0123	1.4492	1.2374
A to Z ↑	0.0156	0.0159	1.2707	1.0856
B to Z ↓	0.0110	0.0107	1.4613	1.2484
B to Z ↑	0.0133	0.0131	1.2805	1.0933
	C12T28SOI_LR_-NAND2X27_P0	**C12T28SOI_LR_-NAND2X42_P0**	**C12T28SOI_LR_-NAND2X27_P0**	**C12T28SOI_LR_-NAND2X42_P0**
A to Z ↓	0.0120	0.0412	1.1000	0.4685
A to Z ↑	0.0155	0.0426	0.9532	0.7517
B to Z ↓	0.0104	0.0419	1.1107	0.4681
B to Z ↑	0.0126	0.0412	0.9600	0.7532
	C12T28SOI_LR_-NAND2X47_P0	**C12T28SOI_LR_-NAND2X50_P0**	**C12T28SOI_LR_-NAND2X47_P0**	**C12T28SOI_LR_-NAND2X50_P0**
A to Z ↓	0.0424	0.0428	0.4163	0.3912
A to Z ↑	0.0434	0.0436	0.6544	0.6277
B to Z ↓	0.0431	0.0434	0.4166	0.3915
B to Z ↑	0.0420	0.0422	0.6553	0.6288
	C12T28SOI_LR_-NAND2X58_P0	**C12T28SOI_LR_-NAND2X67_P0**	**C12T28SOI_LR_-NAND2X58_P0**	**C12T28SOI_LR_-NAND2X67_P0**
A to Z ↓	0.0447	0.0461	0.3394	0.2985
A to Z ↑	0.0451	0.0459	0.5405	0.4748
B to Z ↓	0.0454	0.0468	0.3394	0.2984
B to Z ↑	0.0437	0.0445	0.5405	0.4747
	C12T28SOI_-LRBR0D8_-NAND2X7_P0	**C12T28SOI_-LRBR0D8_-NAND2X14_P0**	**C12T28SOI_-LRBR0D8_-NAND2X7_P0**	**C12T28SOI_-LRBR0D8_-NAND2X14_P0**
A to Z ↓	0.0093	0.0104	3.0997	1.6272
A to Z ↑	0.0187	0.0191	5.1359	2.5092
B to Z ↓	0.0086	0.0079	3.1405	1.6521
B to Z ↑	0.0163	0.0147	5.2936	2.5531
	C12T28SOI_LRS_-NAND2X40_P0	**C12T28SOI_LRS_-NAND2X54_P0**	**C12T28SOI_LRS_-NAND2X40_P0**	**C12T28SOI_LRS_-NAND2X54_P0**
A to Z ↓	0.0120	0.0120	0.7454	0.5639
A to Z ↑	0.0154	0.0154	0.6387	0.4814
B to Z ↓	0.0106	0.0108	0.7523	0.5693
B to Z ↑	0.0127	0.0128	0.6435	0.4851

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P0	2.687e-06	7.027e-10
C12T28SOI_LR_NAND2X5_P0	4.289e-06	7.027e-10
C12T28SOI_LR_NAND2X7_P0	5.074e-06	7.027e-10
C12T28SOI_LR_NAND2X10_P0	7.383e-06	9.409e-10
C12T28SOI_LR_NAND2X13_P0	9.472e-06	9.409e-10
C12T28SOI_LR_NAND2X17_P0	1.196e-05	1.179e-09
C12T28SOI_LR_NAND2X20_P0	1.355e-05	1.179e-09
C12T28SOI_LR_NAND2X24_P0	1.652e-05	1.417e-09
C12T28SOI_LR_NAND2X27_P0	1.764e-05	1.417e-09

C12T28SOI_LR_NAND2X42_P0	3.605e-05	1.536e-09
C12T28SOI_LR_NAND2X47_P0	4.084e-05	1.655e-09
C12T28SOI_LR_NAND2X50_P0	4.041e-05	1.655e-09
C12T28SOI_LR_NAND2X58_P0	4.477e-05	1.775e-09
C12T28SOI_LR_NAND2X67_P0	4.912e-05	1.894e-09
C12T28SOI_LRBR0D8_NAND2X7_P0	5.480e-06	1.296e-09
C12T28SOI_LRBR0D8_NAND2X14_-P0	1.009e-05	1.549e-09
C12T28SOI_LRS_NAND2X40_P0	2.584e-05	1.894e-09
C12T28SOI_LRS_NAND2X54_P0	3.403e-05	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P0	C12T28SOI_LR_-NAND2X5_P0	C12T28SOI_LR_-NAND2X7_P0	C12T28SOI_LR_-NAND2X10_P0
A (output stable)	1.266e-05	2.007e-05	2.388e-05	7.898e-05
B (output stable)	1.512e-05	2.352e-05	2.880e-05	1.904e-04
A to Z	5.045e-04	6.689e-04	7.908e-04	1.412e-03
B to Z	4.346e-04	5.548e-04	6.519e-04	1.004e-03
	C12T28SOI_LR_-NAND2X13_P0	C12T28SOI_LR_-NAND2X17_P0	C12T28SOI_LR_-NAND2X20_P0	C12T28SOI_LR_-NAND2X24_P0
A (output stable)	9.329e-05	1.128e-04	1.254e-04	1.737e-04
B (output stable)	2.126e-04	2.116e-04	2.296e-04	3.552e-04
A to Z	1.717e-03	2.160e-03	2.450e-03	3.012e-03
B to Z	1.222e-03	1.620e-03	1.840e-03	2.148e-03
	C12T28SOI_LR_-NAND2X27_P0	C12T28SOI_LR_-NAND2X42_P0	C12T28SOI_LR_-NAND2X47_P0	C12T28SOI_LR_-NAND2X50_P0
A (output stable)	1.889e-04	2.659e-05	2.667e-05	2.672e-05
B (output stable)	3.781e-04	3.145e-05	3.155e-05	3.160e-05
A to Z	3.254e-03	8.097e-03	8.752e-03	8.978e-03
B to Z	2.280e-03	7.951e-03	8.602e-03	8.827e-03
	C12T28SOI_LR_-NAND2X58_P0	C12T28SOI_LR_-NAND2X67_P0	C12T28SOI_-LRBR0D8_-NAND2X7_P0	C12T28SOI_-LRBR0D8_-NAND2X14_P0
A (output stable)	2.669e-05	2.679e-05	3.170e-05	1.180e-04
B (output stable)	3.164e-05	3.165e-05	3.797e-05	2.733e-04
A to Z	1.020e-02	1.103e-02	8.146e-04	1.769e-03
B to Z	1.006e-02	1.089e-02	6.145e-04	1.102e-03
	C12T28SOI_LRS_-NAND2X40_P0	C12T28SOI_LRS_-NAND2X54_P0		
A (output stable)	2.681e-04	3.498e-04		
B (output stable)	5.173e-04	6.604e-04		
A to Z	4.802e-03	6.366e-03		
B to Z	3.443e-03	4.584e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P0	C12T28SOI_LR_-NAND2X5_P0	C12T28SOI_LR_-NAND2X7_P0	C12T28SOI_LR_-NAND2X10_P0
A (output stable)	4.760e-08	4.115e-08	3.735e-08	2.010e-08
B (output stable)	6.060e-08	5.094e-08	4.328e-08	-4.572e-07
A to Z	-1.970e-08	-1.200e-07	-1.479e-07	-1.045e-07
B to Z	8.090e-08	5.470e-08	1.060e-07	6.340e-08

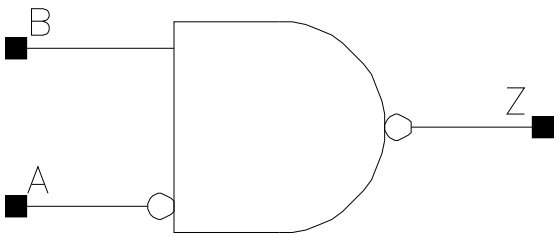
	C12T28SOI_LR_-NAND2X13_P0	C12T28SOI_LR_-NAND2X17_P0	C12T28SOI_LR_-NAND2X20_P0	C12T28SOI_LR_-NAND2X24_P0
A (output stable)	-9.600e-09	-1.500e-08	-2.930e-08	-6.230e-08
B (output stable)	-4.059e-07	-2.914e-07	-4.850e-08	-8.018e-07
A to Z	-2.310e-07	4.110e-07	-2.080e-07	-1.588e-06
B to Z	3.400e-07	-4.790e-07	4.040e-07	8.090e-07
	C12T28SOI_LR_-NAND2X27_P0	C12T28SOI_LR_-NAND2X42_P0	C12T28SOI_LR_-NAND2X47_P0	C12T28SOI_LR_-NAND2X50_P0
A (output stable)	-7.930e-08	4.806e-08	4.780e-08	4.798e-08
B (output stable)	-7.646e-07	3.828e-08	3.868e-08	3.877e-08
A to Z	-2.100e-07	-3.080e-07	-3.030e-07	-4.290e-07
B to Z	9.760e-07	-1.600e-07	-2.760e-07	-7.390e-07
	C12T28SOI_LR_-NAND2X58_P0	C12T28SOI_LR_-NAND2X67_P0	C12T28SOI_-LRBR0D8_-NAND2X7_P0	C12T28SOI_-LRBR0D8_-NAND2X14_P0
A (output stable)	4.835e-08	4.853e-08	4.907e-08	-2.499e-08
B (output stable)	3.896e-08	3.914e-08	5.275e-08	-1.613e-06
A to Z	-4.370e-07	-4.270e-07	3.747e-07	5.413e-07
B to Z	-6.310e-07	-4.140e-07	3.661e-07	2.577e-07
	C12T28SOI_LRS_-NAND2X40_P0	C12T28SOI_LRS_-NAND2X54_P0		
A (output stable)	-1.507e-07	-2.157e-07		
B (output stable)	-9.882e-07	-1.391e-06		
A to Z	4.420e-07	5.910e-07		
B to Z	1.116e-06	1.425e-06		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X7_P0	1.200	0.544	0.6528
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X40_P0	1.200	2.312	2.7744
X54_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P0	X7_P0	X13_P0	X27_P0
A	0.0007	0.0007	0.0009	0.0017
B	0.0005	0.0007	0.0013	0.0026
	X40_P0	X54_P0		
A	0.0026	0.0034		
B	0.0039	0.0052		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0324	0.0338	7.8212	4.1455
A to Z ↑	0.0245	0.0252	7.3359	3.7982
B to Z ↓	0.0134	0.0111	7.9864	4.2191
B to Z ↑	0.0168	0.0140	7.5405	3.9028
	X13_P0	**X27_P0**	**X13_P0**	**X27_P0**

A to Z ↓	0.0311	0.0302	2.1955	1.0964
A to Z ↑	0.0235	0.0228	1.9480	0.9433
B to Z ↓	0.0103	0.0103	2.2412	1.1192
B to Z ↑	0.0130	0.0126	1.9454	0.9612
	X40_P0	**X54_P0**	**X40_P0**	**X54_P0**
A to Z ↓	0.0305	0.0303	0.7346	0.5572
A to Z ↑	0.0232	0.0230	0.6289	0.4743
B to Z ↓	0.0104	0.0105	0.7495	0.5685
B to Z ↑	0.0126	0.0126	0.6455	0.4871

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P0	5.082e-06	8.218e-10
X7_P0	7.389e-06	8.218e-10
X13_P0	1.502e-05	1.179e-09
X27_P0	2.733e-05	1.775e-09
X40_P0	3.955e-05	2.370e-09
X54_P0	5.176e-05	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	7.864e-04	9.751e-04	1.579e-03	3.044e-03
B (output stable)	1.541e-05	2.884e-05	1.895e-04	3.291e-04
A to Z	1.346e-03	1.832e-03	3.349e-03	6.504e-03
B to Z	4.401e-04	6.460e-04	1.196e-03	2.318e-03
	X40_P0	X54_P0		
A (output stable)	4.640e-03	6.026e-03		
B (output stable)	4.810e-04	6.283e-04		
A to Z	9.774e-03	1.282e-02		
B to Z	3.413e-03	4.531e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

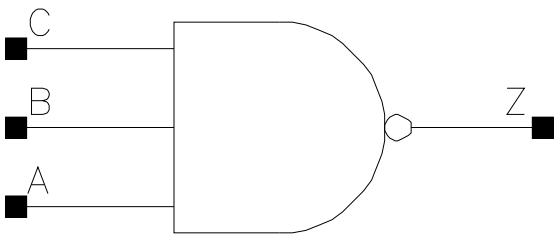
Pin Cycle (vdds)	X3_P0	X7_P0	X13_P0	X27_P0
A (output stable)	-3.100e-08	-3.010e-08	-2.470e-08	4.360e-08
B (output stable)	4.750e-08	4.480e-08	9.400e-09	-4.488e-07
A to Z	-8.120e-09	-4.790e-08	3.090e-08	1.380e-07
B to Z	8.980e-08	1.061e-07	3.785e-07	-1.420e-07
	X40_P0	X54_P0		
A (output stable)	-7.500e-08	-1.260e-07		
B (output stable)	-7.908e-07	-1.175e-06		
A to Z	1.470e-07	1.280e-07		
B to Z	1.088e-06	1.475e-06		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P0	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P0	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P0	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P0	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P0	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P0	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P0	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P0	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P0	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P0	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P0	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P0	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P0	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P0	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P0	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P0	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A	0.0006	0.0007	0.0012	0.0014
B	0.0006	0.0008	0.0011	0.0013
C	0.0006	0.0007	0.0011	0.0013
	C12T28SOI_LR_-NAND3X15_P0	C12T28SOI_LR_-NAND3X18_P0	C12T28SOI_LR_-NAND3X21_P0	C12T28SOI_LR_-NAND3X24_P0
A	0.0018	0.0021	0.0025	0.0028
B	0.0018	0.0020	0.0024	0.0027
C	0.0017	0.0019	0.0023	0.0026
	C12T28SOI_LR_-NAND3X35_P0	C12T28SOI_LR_-NAND3X47_P0	C12T28SOI_-LRBR0P6_-NAND3X6_P0	C12T28SOI_-LRBR0P6_-NAND3X12_P0
A	0.0042	0.0056	0.0007	0.0014
B	0.0040	0.0054	0.0008	0.0013
C	0.0039	0.0053	0.0007	0.0013
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	C12T28SOI_-LRBR0P6_-NAND3X24_P0	C12T28SOI_-LRBR0P6_-NAND3X35_P0	C12T28SOI_-LRBR0P6_-NAND3X47_P0
A	0.0021	0.0028	0.0041	0.0055
B	0.0019	0.0026	0.0039	0.0052
C	0.0018	0.0025	0.0037	0.0050
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0			
A	0.0022			
B	0.0021			
C	0.0019			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0
A to Z ↓	0.0197	0.0177	8.3160	5.8791
A to Z ↑	0.0223	0.0202	5.4309	3.7301
B to Z ↓	0.0208	0.0183	8.3462	5.8927
B to Z ↑	0.0216	0.0193	5.4390	3.7371
C to Z ↓	0.0181	0.0161	8.3557	5.9205
C to Z ↑	0.0190	0.0170	5.4360	3.7556

	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A to Z ↓	0.0196	0.0183	4.0301	3.1043
A to Z ↑	0.0212	0.0199	2.5418	1.9062
B to Z ↓	0.0187	0.0175	4.0393	3.1191
B to Z ↑	0.0195	0.0182	2.5464	1.9096
C to Z ↓	0.0162	0.0153	4.0592	3.1289
C to Z ↑	0.0169	0.0157	2.5366	1.8946
	C12T28SOI_LR_-NAND3X15_P0	**C12T28SOI_LR_-NAND3X18_P0**	**C12T28SOI_LR_-NAND3X15_P0**	**C12T28SOI_LR_-NAND3X18_P0**
A to Z ↓	0.0177	0.0173	2.5243	2.1524
A to Z ↑	0.0194	0.0189	1.5229	1.2677
B to Z ↓	0.0176	0.0172	2.5292	2.1624
B to Z ↑	0.0178	0.0173	1.5266	1.2707
C to Z ↓	0.0156	0.0151	2.5386	2.1669
C to Z ↑	0.0157	0.0151	1.5349	1.2781
	C12T28SOI_LR_-NAND3X21_P0	**C12T28SOI_LR_-NAND3X24_P0**	**C12T28SOI_LR_-NAND3X21_P0**	**C12T28SOI_LR_-NAND3X24_P0**
A to Z ↓	0.0182	0.0179	1.8218	1.6231
A to Z ↑	0.0196	0.0192	1.0911	0.9589
B to Z ↓	0.0176	0.0173	1.8270	1.6257
B to Z ↑	0.0180	0.0176	1.0929	0.9604
C to Z ↓	0.0155	0.0152	1.8337	1.6325
C to Z ↑	0.0156	0.0153	1.0940	0.9602
	C12T28SOI_LR_-NAND3X35_P0	**C12T28SOI_LR_-NAND3X47_P0**	**C12T28SOI_LR_-NAND3X35_P0**	**C12T28SOI_LR_-NAND3X47_P0**
A to Z ↓	0.0172	0.0175	1.1058	0.8407
A to Z ↑	0.0186	0.0188	0.6425	0.4855
B to Z ↓	0.0170	0.0171	1.1100	0.8433
B to Z ↑	0.0171	0.0171	0.6424	0.4842
C to Z ↓	0.0149	0.0150	1.1131	0.8461
C to Z ↑	0.0146	0.0146	0.6455	0.4861
	C12T28SOI_-LRBR0P6_-NAND3X6_P0	**C12T28SOI_-LRBR0P6_-NAND3X12_P0**	**C12T28SOI_-LRBR0P6_-NAND3X6_P0**	**C12T28SOI_-LRBR0P6_-NAND3X12_P0**
A to Z ↓	0.0141	0.0146	3.9560	2.0797
A to Z ↑	0.0274	0.0271	5.9318	3.0265
B to Z ↓	0.0141	0.0132	3.9862	2.0937
B to Z ↑	0.0252	0.0237	5.9467	3.0320
C to Z ↓	0.0110	0.0099	4.0126	2.1116
C to Z ↑	0.0205	0.0185	5.9725	3.0384
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	**C12T28SOI_-LRBR0P6_-NAND3X24_P0**	**C12T28SOI_-LRBR0P6_-NAND3X18_P0**	**C12T28SOI_-LRBR0P6_-NAND3X24_P0**
A to Z ↓	0.0137	0.0141	1.4405	1.0826
A to Z ↑	0.0257	0.0262	2.0139	1.5210
B to Z ↓	0.0127	0.0128	1.4523	1.0911
B to Z ↑	0.0224	0.0229	2.0197	1.5242
C to Z ↓	0.0100	0.0098	1.4601	1.0997
C to Z ↑	0.0180	0.0179	2.0318	1.5256
	C12T28SOI_-LRBR0P6_-NAND3X35_P0	**C12T28SOI_-LRBR0P6_-NAND3X47_P0**	**C12T28SOI_-LRBR0P6_-NAND3X35_P0**	**C12T28SOI_-LRBR0P6_-NAND3X47_P0**

A to Z ↓	0.0137	0.0137	0.7386	0.5629
A to Z ↑	0.0260	0.0258	1.0424	0.7885
B to Z ↓	0.0127	0.0126	0.7445	0.5675
B to Z ↑	0.0226	0.0224	1.0434	0.7884
C to Z ↓	0.0097	0.0098	0.7509	0.5714
C to Z ↑	0.0176	0.0175	1.0509	0.7904
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P0**	
A to Z ↓	0.0143		1.3684	
A to Z ↑	0.0259		1.8827	
B to Z ↓	0.0128		1.3790	
B to Z ↑	0.0226		1.8876	
C to Z ↓	0.0094		1.3903	
C to Z ↑	0.0174		1.8741	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P0	3.067e-06	9.409e-10
C12T28SOI_LR_NAND3X6_P0	4.363e-06	9.409e-10
C12T28SOI_LR_NAND3X9_P0	6.109e-06	1.298e-09
C12T28SOI_LR_NAND3X12_P0	7.792e-06	1.298e-09
C12T28SOI_LR_NAND3X15_P0	9.321e-06	1.536e-09
C12T28SOI_LR_NAND3X18_P0	1.058e-05	1.536e-09
C12T28SOI_LR_NAND3X21_P0	1.344e-05	2.013e-09
C12T28SOI_LR_NAND3X24_P0	1.434e-05	2.013e-09
C12T28SOI_LR_NAND3X35_P0	2.086e-05	2.727e-09
C12T28SOI_LR_NAND3X47_P0	2.740e-05	3.442e-09
C12T28SOI_LRBR0P6_NAND3X6_P0	4.901e-06	1.615e-09
C12T28SOI_LRBR0P6_NAND3X12_-P0	8.918e-06	2.005e-09
C12T28SOI_LRBR0P6_NAND3X18_-P0	1.200e-05	2.266e-09
C12T28SOI_LRBR0P6_NAND3X24_-P0	1.667e-05	2.786e-09
C12T28SOI_LRBR0P6_NAND3X35_-P0	2.441e-05	3.566e-09
C12T28SOI_LRBR0P6_NAND3X47_-P0	3.217e-05	4.346e-09
C12T28SOIDV_LRBR0P6_-NAND3X18_P0	1.460e-05	1.874e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A (output stable)	2.456e-05	3.332e-05	7.980e-05	9.320e-05
B (output stable)	4.221e-05	5.228e-05	1.279e-04	1.484e-04
C (output stable)	1.648e-04	1.924e-04	3.132e-04	3.579e-04
A to Z	1.140e-03	1.385e-03	2.280e-03	2.684e-03
B to Z	1.042e-03	1.237e-03	1.872e-03	2.209e-03
C to Z	8.283e-04	9.899e-04	1.450e-03	1.715e-03

	C12T28SOI_LR_-NAND3X15_P0	C12T28SOI_LR_-NAND3X18_P0	C12T28SOI_LR_-NAND3X21_P0	C12T28SOI_LR_-NAND3X24_P0
A (output stable)	1.045e-04	1.185e-04	1.636e-04	1.760e-04
B (output stable)	1.595e-04	1.857e-04	2.504e-04	2.795e-04
C (output stable)	3.825e-04	4.296e-04	5.816e-04	6.343e-04
A to Z	3.211e-03	3.629e-03	4.585e-03	5.003e-03
B to Z	2.656e-03	3.005e-03	3.774e-03	4.127e-03
C to Z	2.125e-03	2.374e-03	2.953e-03	3.205e-03
	C12T28SOI_LR_-NAND3X35_P0	C12T28SOI_LR_-NAND3X47_P0	C12T28SOI_-LRBR0P6_-NAND3X6_P0	C12T28SOI_-LRBR0P6_-NAND3X12_P0
A (output stable)	2.426e-04	3.197e-04	4.836e-05	1.344e-04
B (output stable)	3.825e-04	5.017e-04	7.665e-05	2.194e-04
C (output stable)	9.186e-04	1.175e-03	2.634e-04	5.149e-04
A to Z	7.097e-03	9.410e-03	1.469e-03	2.880e-03
B to Z	5.805e-03	7.721e-03	1.237e-03	2.184e-03
C to Z	4.424e-03	5.915e-03	8.588e-04	1.406e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	C12T28SOI_-LRBR0P6_-NAND3X24_P0	C12T28SOI_-LRBR0P6_-NAND3X35_P0	C12T28SOI_-LRBR0P6_-NAND3X47_P0
A (output stable)	1.729e-04	2.512e-04	3.468e-04	4.567e-04
B (output stable)	2.584e-04	3.994e-04	5.311e-04	7.019e-04
C (output stable)	5.619e-04	9.130e-04	1.310e-03	1.689e-03
A to Z	3.870e-03	5.344e-03	7.718e-03	1.001e-02
B to Z	2.920e-03	4.051e-03	5.828e-03	7.552e-03
C to Z	1.983e-03	2.637e-03	3.747e-03	4.813e-03
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0			
A (output stable)	1.973e-04			
B (output stable)	3.193e-04			
C (output stable)	7.160e-04			
A to Z	4.227e-03			
B to Z	3.201e-03			
C to Z	2.042e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P0	C12T28SOI_LR_-NAND3X6_P0	C12T28SOI_LR_-NAND3X9_P0	C12T28SOI_LR_-NAND3X12_P0
A (output stable)	5.140e-08	4.824e-08	4.913e-08	2.433e-08
B (output stable)	5.571e-08	-3.116e-08	-1.947e-07	5.877e-09
C (output stable)	5.484e-08	-5.956e-07	-1.152e-06	1.564e-08
A to Z	-2.240e-07	-4.570e-07	-4.970e-07	-6.630e-07
B to Z	-1.140e-07	5.830e-07	3.330e-07	1.300e-07
C to Z	2.450e-07	4.090e-07	5.550e-07	3.490e-07
	C12T28SOI_LR_-NAND3X15_P0	C12T28SOI_LR_-NAND3X18_P0	C12T28SOI_LR_-NAND3X21_P0	C12T28SOI_LR_-NAND3X24_P0
A (output stable)	1.133e-09	5.133e-09	1.467e-09	-1.460e-08
B (output stable)	-2.266e-07	-2.429e-07	-7.714e-07	-4.964e-07
C (output stable)	-9.009e-07	-8.598e-07	-2.411e-06	-1.810e-06
A to Z	6.590e-07	6.420e-07	-1.167e-06	-1.444e-06
B to Z	1.630e-07	-1.530e-07	2.180e-07	-3.250e-07

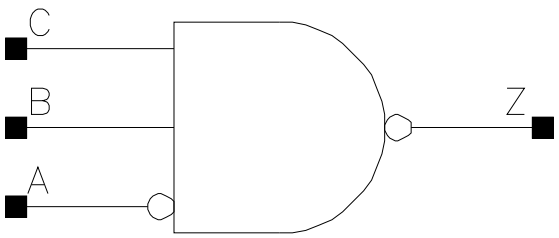
C to Z	8.500e-07	-6.410e-07	2.940e-07	1.450e-07
	C12T28SOI_LR_-NAND3X35_P0	C12T28SOI_LR_-NAND3X47_P0	C12T28SOI_-LRBR0P6_-NAND3X6_P0	C12T28SOI_-LRBR0P6_-NAND3X12_P0
A (output stable)	-6.570e-08	-1.263e-07	7.034e-08	6.766e-08
B (output stable)	-7.605e-07	-1.059e-06	-2.936e-07	-1.090e-06
C (output stable)	-2.572e-06	-3.409e-06	-2.433e-06	-3.510e-06
A to Z	8.870e-07	1.011e-06	1.520e-07	-1.252e-06
B to Z	-7.020e-07	-3.019e-06	-4.512e-07	-3.680e-07
C to Z	2.755e-06	3.786e-06	2.308e-07	4.120e-07
	C12T28SOI_-LRBR0P6_-NAND3X18_P0	C12T28SOI_-LRBR0P6_-NAND3X24_P0	C12T28SOI_-LRBR0P6_-NAND3X35_P0	C12T28SOI_-LRBR0P6_-NAND3X47_P0
A (output stable)	3.147e-08	3.260e-08	-5.467e-09	-2.853e-08
B (output stable)	-1.917e-09	-1.402e-06	-9.187e-07	-1.180e-06
C (output stable)	1.240e-08	-4.196e-06	-3.452e-06	-4.280e-06
A to Z	9.200e-08	-2.219e-06	-2.100e-08	6.400e-07
B to Z	-3.360e-07	-6.910e-07	-6.920e-07	-1.125e-06
C to Z	5.850e-07	3.330e-07	1.774e-06	1.603e-06
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P0			
A (output stable)	1.980e-08			
B (output stable)	1.033e-09			
C (output stable)	4.000e-09			
A to Z	-1.845e-06			
B to Z	-4.460e-07			
C to Z	8.930e-07			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.816	0.9792
X12_P0	1.200	1.224	1.4688
X18_P0	1.200	1.496	1.7952
X24_P0	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0007	0.0010	0.0010	0.0017
B	0.0007	0.0014	0.0020	0.0027
C	0.0007	0.0013	0.0019	0.0026

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X12_P0**	**X6_P0**	**X12_P0**
A to Z ↓	0.0382	0.0363	5.9344	3.1366
A to Z ↑	0.0271	0.0255	3.6892	1.8500
B to Z ↓	0.0163	0.0167	5.9835	3.1578
B to Z ↑	0.0175	0.0173	3.7494	1.8887
C to Z ↓	0.0157	0.0142	5.9914	3.1743
C to Z ↑	0.0160	0.0146	3.7658	1.9002
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0414	0.0353	2.1554	1.6261

A to Z ↑	0.0294	0.0243	1.2464	0.9344
B to Z ↓	0.0172	0.0167	2.1682	1.6369
B to Z ↑	0.0173	0.0170	1.2721	0.9561
C to Z ↓	0.0152	0.0143	2.1730	1.6422
C to Z ↑	0.0152	0.0143	1.2797	0.9624

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P0	6.368e-06	1.060e-09
X12_P0	1.265e-05	1.417e-09
X18_P0	1.532e-05	1.655e-09
X24_P0	2.436e-05	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	9.446e-04	1.661e-03	2.245e-03	3.077e-03
B (output stable)	3.378e-05	1.248e-04	2.006e-04	2.874e-04
C (output stable)	7.456e-05	3.600e-04	4.389e-04	6.469e-04
A to Z	2.212e-03	4.299e-03	6.213e-03	8.238e-03
B to Z	1.028e-03	2.001e-03	3.002e-03	3.856e-03
C to Z	8.813e-04	1.498e-03	2.370e-03	2.866e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

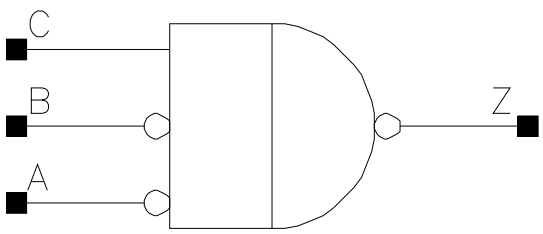
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	-3.687e-08	-3.733e-08	-1.317e-07	1.550e-08
B (output stable)	4.801e-08	-1.966e-07	-3.697e-08	-7.034e-07
C (output stable)	4.734e-08	-1.004e-06	-1.927e-08	-1.857e-06
A to Z	-3.740e-08	1.450e-07	-3.000e-08	1.870e-07
B to Z	5.830e-07	-1.660e-07	-9.000e-08	-6.380e-07
C to Z	3.600e-07	-3.300e-08	-5.920e-07	1.412e-06

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P0	1.200	0.816	0.9792
X13_P0	1.200	1.088	1.3056
X20_P0	1.200	1.632	1.9584
X27_P0	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P0	X13_P0	X20_P0	X27_P0
A	0.0008	0.0008	0.0017	0.0015
B	0.0010	0.0009	0.0018	0.0016
C	0.0007	0.0013	0.0019	0.0026

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P0	**X13_P0**	**X7_P0**	**X13_P0**
A to Z ↓	0.0379	0.0458	3.9707	2.1154
A to Z ↑	0.0229	0.0261	3.6624	1.8424
B to Z ↓	0.0371	0.0454	3.9735	2.1172
B to Z ↑	0.0217	0.0250	3.6574	1.8396
C to Z ↓	0.0109	0.0103	4.0336	2.1414
C to Z ↑	0.0139	0.0129	3.7584	1.8997
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0416	0.0458	1.4412	1.0942
A to Z ↑	0.0242	0.0289	1.2427	0.9333
B to Z ↓	0.0384	0.0436	1.4413	1.0939

B to Z ↑	0.0223	0.0276	1.2399	0.9310
C to Z ↓	0.0113	0.0109	1.4622	1.1082
C to Z ↑	0.0137	0.0133	1.2797	0.9610

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X7_P0	9.741e-06	1.060e-09
X13_P0	1.320e-05	1.298e-09
X20_P0	2.067e-05	1.775e-09
X27_P0	2.304e-05	2.013e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	5.552e-04	7.378e-04	1.258e-03	1.478e-03
B (output stable)	4.825e-04	6.672e-04	1.038e-03	1.291e-03
C (output stable)	3.142e-05	2.320e-04	2.154e-04	2.721e-04
A to Z	2.452e-03	4.027e-03	6.368e-03	7.913e-03
B to Z	2.219e-03	3.800e-03	5.563e-03	7.247e-03
C to Z	6.711e-04	1.194e-03	1.960e-03	2.546e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

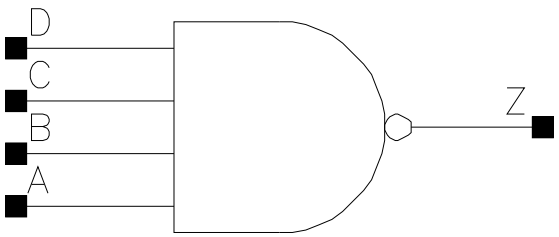
Pin Cycle (vdds)	X7_P0	X13_P0	X20_P0	X27_P0
A (output stable)	2.301e-07	1.525e-07	2.662e-07	1.817e-07
B (output stable)	3.014e-06	2.994e-06	3.381e-05	3.358e-05
C (output stable)	3.829e-08	5.233e-09	-4.793e-08	-8.500e-08
A to Z	1.987e-07	1.485e-07	1.072e-06	6.363e-07
B to Z	-6.300e-09	-9.810e-08	4.300e-08	-3.310e-07
C to Z	1.117e-07	3.777e-07	-1.240e-07	6.940e-07

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0006	0.0005	0.0007	0.0008
B	0.0006	0.0006	0.0008	0.0009
C	0.0006	0.0006	0.0008	0.0009
D	0.0006	0.0006	0.0008	0.0009

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0593	0.0581	2.2751	1.1363
A to Z ↑	0.0454	0.0485	3.7375	1.8576
B to Z ↓	0.0603	0.0599	2.2744	1.1369
B to Z ↑	0.0441	0.0480	3.7391	1.8577
C to Z ↓	0.0599	0.0571	2.2748	1.1363
C to Z ↑	0.0472	0.0508	3.7368	1.8555

D to Z ↓	0.0613	0.0580	2.2728	1.1365
D to Z ↑	0.0464	0.0491	3.7398	1.8550
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0595	0.0546	0.7855	0.5883
A to Z ↑	0.0463	0.0451	1.2492	0.9387
B to Z ↓	0.0606	0.0555	0.7857	0.5887
B to Z ↑	0.0453	0.0438	1.2504	0.9385
C to Z ↓	0.0546	0.0502	0.7853	0.5885
C to Z ↑	0.0472	0.0457	1.2470	0.9372
D to Z ↓	0.0556	0.0512	0.7855	0.5878
D to Z ↑	0.0457	0.0443	1.2506	0.9380

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	1.256e-05	1.417e-09
X17_P0	1.937e-05	1.655e-09
X25_P0	2.741e-05	2.013e-09
X33_P0	3.551e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	3.916e-04	4.895e-04	6.989e-04	8.303e-04
B (output stable)	3.622e-04	4.654e-04	6.569e-04	7.724e-04
C (output stable)	3.993e-04	4.832e-04	7.269e-04	8.296e-04
D (output stable)	3.701e-04	4.496e-04	6.771e-04	7.701e-04
A to Z	2.945e-03	4.395e-03	6.735e-03	8.168e-03
B to Z	2.868e-03	4.331e-03	6.624e-03	8.021e-03
C to Z	3.039e-03	4.348e-03	6.306e-03	7.598e-03
D to Z	2.972e-03	4.264e-03	6.185e-03	7.452e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

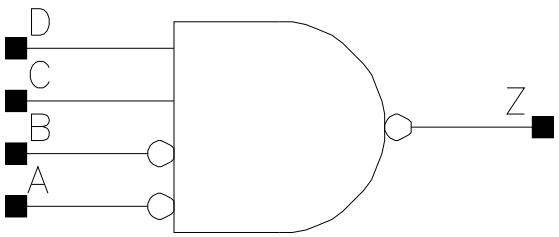
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	8.378e-08	1.658e-07	1.579e-08	1.698e-07
B (output stable)	1.336e-07	1.974e-07	1.273e-07	2.736e-07
C (output stable)	1.772e-06	2.074e-06	1.643e-05	1.761e-05
D (output stable)	1.836e-06	2.156e-06	1.655e-05	1.771e-05
A to Z	4.940e-08	3.288e-07	1.008e-06	1.338e-06
B to Z	2.784e-07	3.675e-07	1.073e-06	1.252e-06
C to Z	-1.310e-07	-2.539e-07	-3.830e-07	-2.550e-07
D to Z	-4.300e-08	-4.230e-08	-1.060e-07	-1.470e-07

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X12_P0	1.200	1.496	1.7952
X18_P0	1.200	2.040	2.4480
X24_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P0	X12_P0	X18_P0	X24_P0
A	0.0009	0.0009	0.0017	0.0016
B	0.0009	0.0013	0.0018	0.0016
C	0.0007	0.0014	0.0020	0.0027
D	0.0007	0.0013	0.0019	0.0027

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X12_P0	X6_P0	X12_P0
A to Z ↓	0.0401	0.0534	6.0960	3.1451
A to Z ↑	0.0241	0.0292	3.6605	1.8449
B to Z ↓	0.0387	0.0520	6.0982	3.1464
B to Z ↑	0.0221	0.0278	3.6572	1.8423
C to Z ↓	0.0164	0.0167	6.1438	3.1559
C to Z ↑	0.0176	0.0173	3.9486	1.8885

D to Z ↓	0.0155	0.0142	6.1653	3.1727
D to Z ↑	0.0160	0.0145	3.9660	1.8995
	X18_P0	**X24_P0**	**X18_P0**	**X24_P0**
A to Z ↓	0.0459	0.0517	2.1494	1.6307
A to Z ↑	0.0257	0.0328	1.2432	0.9342
B to Z ↓	0.0428	0.0493	2.1498	1.6309
B to Z ↑	0.0238	0.0313	1.2404	0.9328
C to Z ↓	0.0166	0.0173	2.1617	1.6367
C to Z ↑	0.0169	0.0174	1.2771	0.9537
D to Z ↓	0.0148	0.0152	2.1694	1.6434
D to Z ↑	0.0148	0.0150	1.3004	0.9605

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P0	7.773e-06	1.179e-09
X12_P0	1.114e-05	1.655e-09
X18_P0	1.754e-05	2.132e-09
X24_P0	1.857e-05	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	6.229e-04	1.051e-03	1.582e-03	1.912e-03
B (output stable)	5.283e-04	9.133e-04	1.289e-03	1.645e-03
C (output stable)	3.923e-05	1.328e-04	1.922e-04	2.832e-04
D (output stable)	9.090e-05	3.928e-04	4.622e-04	7.319e-04
A to Z	2.612e-03	4.951e-03	7.248e-03	9.654e-03
B to Z	2.380e-03	4.609e-03	6.496e-03	8.959e-03
C to Z	9.974e-04	1.997e-03	2.851e-03	4.065e-03
D to Z	8.470e-04	1.483e-03	2.260e-03	3.140e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

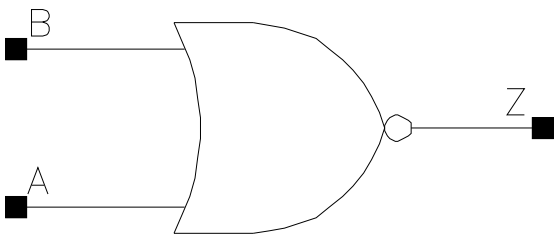
Pin Cycle (vdds)	X6_P0	X12_P0	X18_P0	X24_P0
A (output stable)	2.452e-07	2.647e-07	3.006e-07	2.419e-07
B (output stable)	2.825e-06	1.857e-05	2.857e-05	3.152e-05
C (output stable)	5.348e-08	-2.494e-07	-3.061e-07	-7.389e-07
D (output stable)	4.694e-08	-1.179e-06	-9.753e-07	-2.668e-06
A to Z	3.945e-07	6.924e-07	1.025e-06	4.040e-07
B to Z	2.907e-07	-2.630e-07	1.510e-07	-3.840e-07
C to Z	1.890e-07	-1.460e-07	-2.650e-07	-2.610e-07
D to Z	3.320e-07	3.500e-07	4.780e-07	-1.106e-06

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.408	0.4896
X5_P0	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X10_P0	1.200	0.680	0.8160
X14_P0	1.200	0.680	0.8160
X17_P0	1.200	0.952	1.1424
X21_P0	1.200	0.952	1.1424
X24_P0	1.200	1.224	1.4688
X27_P0	1.200	1.224	1.4688
X34_P0	1.200	1.496	1.7952
X40_P0	1.200	1.360	1.6320
X41_P0	1.200	1.768	2.1216
X49_P0	1.200	1.496	1.7952
X53_P0	1.200	1.904	2.2848
X55_P0	1.200	2.312	2.7744
X57_P0	1.200	1.904	2.2848
X65_P0	1.200	2.040	2.4480
X84_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P0	X5_P0	X7_P0	X10_P0
A	0.0005	0.0006	0.0007	0.0012
B	0.0005	0.0006	0.0007	0.0011
	X14_P0	X17_P0	X21_P0	X24_P0

A	0.0015	0.0019	0.0022	0.0025
B	0.0013	0.0017	0.0020	0.0024
	X27_P0	X34_P0	X40_P0	X41_P0
A	0.0028	0.0036	0.0008	0.0044
B	0.0026	0.0033	0.0010	0.0040
	X49_P0	X53_P0	X55_P0	X57_P0
A	0.0008	0.0009	0.0058	0.0009
B	0.0010	0.0008	0.0053	0.0008
	X65_P0	X84_P0		
A	0.0009	0.0010		
B	0.0008	0.0009		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X5_P0**	**X3_P0**	**X5_P0**
A to Z ↓	0.0109	0.0101	4.3659	3.1485
A to Z ↑	0.0220	0.0204	16.0140	11.6213
B to Z ↓	0.0099	0.0089	4.4560	3.1663
B to Z ↑	0.0212	0.0190	16.0781	11.6572
	X7_P0	**X10_P0**	**X7_P0**	**X10_P0**
A to Z ↓	0.0097	0.0102	2.3018	1.5046
A to Z ↑	0.0192	0.0217	8.2029	5.4618
B to Z ↓	0.0084	0.0078	2.3293	1.5179
B to Z ↑	0.0177	0.0164	8.2306	5.4873
	X14_P0	**X17_P0**	**X14_P0**	**X17_P0**
A to Z ↓	0.0099	0.0101	1.1428	0.9183
A to Z ↑	0.0204	0.0204	4.0535	3.2679
B to Z ↓	0.0075	0.0082	1.1534	0.9250
B to Z ↑	0.0156	0.0167	4.0700	3.2792
	X21_P0	**X24_P0**	**X21_P0**	**X24_P0**
A to Z ↓	0.0100	0.0099	0.7827	0.6679
A to Z ↑	0.0198	0.0201	2.7219	2.3644
B to Z ↓	0.0081	0.0077	0.7891	0.6736
B to Z ↑	0.0162	0.0160	2.7332	2.3734
	X27_P0	**X34_P0**	**X27_P0**	**X34_P0**
A to Z ↓	0.0097	0.0102	0.5928	0.4789
A to Z ↑	0.0194	0.0199	2.0805	1.6584
B to Z ↓	0.0075	0.0081	0.5983	0.4830
B to Z ↑	0.0153	0.0162	2.0891	1.6644
	X40_P0	**X41_P0**	**X40_P0**	**X41_P0**
A to Z ↓	0.0362	0.0100	0.4777	0.3992
A to Z ↑	0.0545	0.0197	0.7683	1.3752
B to Z ↓	0.0349	0.0077	0.4775	0.4032
B to Z ↑	0.0542	0.0154	0.7684	1.3818
	X49_P0	**X53_P0**	**X49_P0**	**X53_P0**
A to Z ↓	0.0376	0.0388	0.3983	0.3651
A to Z ↑	0.0557	0.0634	0.6386	0.5909
B to Z ↓	0.0363	0.0375	0.3984	0.3650
B to Z ↑	0.0554	0.0625	0.6389	0.5917
	X55_P0	**X57_P0**	**X55_P0**	**X57_P0**
A to Z ↓	0.0100	0.0394	0.3020	0.3431
A to Z ↑	0.0194	0.0640	1.0350	0.5502

B to Z ↓	0.0078	0.0381	0.3055	0.3430
B to Z ↑	0.0154	0.0630	1.0406	0.5501
	X65_P0	**X84_P0**	**X65_P0**	**X84_P0**
A to Z ↓	0.0401	0.0419	0.3007	0.2396
A to Z ↑	0.0644	0.0651	0.4809	0.3814
B to Z ↓	0.0388	0.0406	0.3008	0.2392
B to Z ↑	0.0635	0.0644	0.4806	0.3815

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P0	2.699e-06	7.027e-10
X5_P0	3.749e-06	7.027e-10
X7_P0	5.094e-06	7.027e-10
X10_P0	7.425e-06	9.409e-10
X14_P0	9.525e-06	9.409e-10
X17_P0	1.207e-05	1.179e-09
X21_P0	1.364e-05	1.179e-09
X24_P0	1.664e-05	1.417e-09
X27_P0	1.777e-05	1.417e-09
X34_P0	2.190e-05	1.655e-09
X40_P0	3.380e-05	1.536e-09
X41_P0	2.604e-05	1.894e-09
X49_P0	3.765e-05	1.655e-09
X53_P0	4.570e-05	2.013e-09
X55_P0	3.430e-05	2.370e-09
X57_P0	4.784e-05	2.013e-09
X65_P0	5.170e-05	2.132e-09
X84_P0	5.732e-05	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	2.083e-05	2.807e-05	3.842e-05	1.137e-04
B (output stable)	2.315e-05	3.257e-05	4.712e-05	1.396e-04
A to Z	5.286e-04	6.443e-04	8.443e-04	1.490e-03
B to Z	4.120e-04	4.851e-04	6.189e-04	8.681e-04
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	1.330e-04	1.623e-04	1.810e-04	2.196e-04
B (output stable)	1.746e-04	2.015e-04	2.173e-04	2.711e-04
A to Z	1.835e-03	2.310e-03	2.642e-03	3.130e-03
B to Z	1.088e-03	1.495e-03	1.711e-03	1.952e-03
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	2.382e-04	2.920e-04	3.883e-05	3.763e-04
B (output stable)	2.852e-04	3.334e-04	4.729e-05	4.546e-04
A to Z	3.361e-03	4.366e-03	7.979e-03	5.186e-03
B to Z	2.068e-03	2.834e-03	7.757e-03	3.141e-03
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	3.901e-05	4.051e-05	4.819e-04	4.053e-05
B (output stable)	4.719e-05	5.019e-05	5.600e-04	5.019e-05
A to Z	8.881e-03	1.102e-02	6.741e-03	1.149e-02
B to Z	8.657e-03	1.078e-02	4.153e-03	1.124e-02
	X65_P0	X84_P0		

A (output stable)	4.061e-05	4.199e-05		
B (output stable)	5.029e-05	5.045e-05		
A to Z	1.223e-02	1.451e-02		
B to Z	1.199e-02	1.421e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

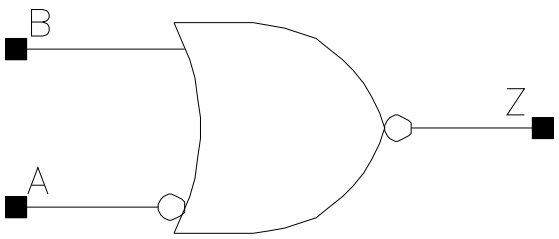
Pin Cycle (vdds)	X3_P0	X5_P0	X7_P0	X10_P0
A (output stable)	1.039e-07	1.158e-07	1.517e-07	-2.965e-07
B (output stable)	4.466e-06	4.324e-06	4.427e-06	4.892e-05
A to Z	2.378e-07	2.708e-07	3.498e-07	1.454e-06
B to Z	-4.280e-08	1.171e-07	2.672e-07	3.236e-07
	X14_P0	X17_P0	X21_P0	X24_P0
A (output stable)	-2.980e-08	-1.460e-07	2.390e-07	5.006e-08
B (output stable)	5.319e-05	3.932e-05	3.908e-05	6.809e-05
A to Z	1.458e-06	1.115e-06	1.200e-06	2.089e-06
B to Z	5.711e-07	7.683e-07	7.020e-07	9.936e-07
	X27_P0	X34_P0	X40_P0	X41_P0
A (output stable)	1.351e-07	4.344e-07	1.585e-07	1.486e-07
B (output stable)	6.260e-05	5.929e-05	4.301e-06	1.063e-04
A to Z	2.068e-06	1.323e-06	-2.890e-07	3.147e-06
B to Z	1.975e-06	1.124e-06	-2.810e-07	2.816e-06
	X49_P0	X53_P0	X55_P0	X57_P0
A (output stable)	1.599e-07	1.525e-07	1.143e-07	1.525e-07
B (output stable)	4.287e-06	4.881e-06	1.124e-04	4.881e-06
A to Z	2.900e-08	-7.600e-08	3.167e-06	-7.260e-07
B to Z	-7.710e-07	-3.570e-07	3.608e-06	-6.030e-07
	X65_P0	X84_P0		
A (output stable)	1.527e-07	1.748e-07		
B (output stable)	4.883e-06	5.442e-06		
A to Z	-7.020e-07	-1.780e-07		
B to Z	-5.350e-07	-5.050e-07		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X7_P0	1.200	0.680	0.8160
X13_P0	1.200	0.952	1.1424
X27_P0	1.200	1.632	1.9584
X41_P0	1.200	2.312	2.7744
X55_P0	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X7_P0	X13_P0
A	0.0007	0.0007	0.0007	0.0010
B	0.0005	0.0007	0.0007	0.0013
	X27_P0	X41_P0	X55_P0	
A	0.0018	0.0026	0.0034	
B	0.0027	0.0039	0.0052	

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X6_P0**	**X3_P0**	**X6_P0**
A to Z ↓	0.0301	0.0326	4.2309	2.7413
A to Z ↑	0.0290	0.0287	15.9068	8.1650
B to Z ↓	0.0102	0.0097	4.4360	2.8945
B to Z ↑	0.0214	0.0176	16.0527	8.2474

	X7_P0	X13_P0	X7_P0	X13_P0
A to Z ↓	0.0329	0.0294	2.1692	1.1790
A to Z ↑	0.0312	0.0289	8.0468	4.2398
B to Z ↓	0.0087	0.0078	2.2192	1.2042
B to Z ↑	0.0187	0.0168	8.1113	4.2788
	X27_P0	**X41_P0**	**X27_P0**	**X41_P0**
A to Z ↓	0.0284	0.0288	0.5699	0.3862
A to Z ↑	0.0278	0.0279	2.0415	1.3682
B to Z ↓	0.0078	0.0078	0.5986	0.4047
B to Z ↑	0.0161	0.0158	2.0628	1.3821
	X55_P0		**X55_P0**	
A to Z ↓	0.0286		0.2924	
A to Z ↑	0.0277		1.0324	
B to Z ↓	0.0079		0.3069	
B to Z ↑	0.0158		1.0425	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P0	5.078e-06	8.218e-10
X6_P0	7.091e-06	8.218e-10
X7_P0	8.289e-06	9.409e-10
X13_P0	1.480e-05	1.179e-09
X27_P0	2.742e-05	1.775e-09
X41_P0	3.971e-05	2.370e-09
X55_P0	5.199e-05	2.966e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	7.754e-04	9.556e-04	1.018e-03	1.617e-03
B (output stable)	2.793e-05	5.174e-05	1.081e-04	2.145e-04
A to Z	1.348e-03	1.836e-03	2.139e-03	3.567e-03
B to Z	4.216e-04	6.068e-04	7.225e-04	1.178e-03
	X27_P0	X41_P0	X55_P0	
A (output stable)	3.145e-03	4.734e-03	6.226e-03	
B (output stable)	4.259e-04	6.065e-04	7.690e-04	
A to Z	7.013e-03	1.039e-02	1.369e-02	
B to Z	2.282e-03	3.333e-03	4.381e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

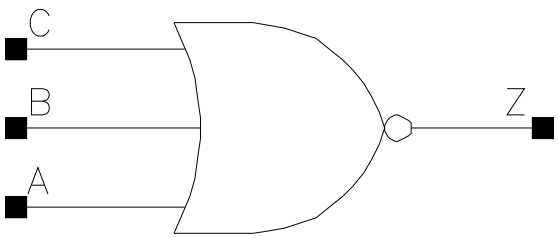
Pin Cycle (vdds)	X3_P0	X6_P0	X7_P0	X13_P0
A (output stable)	2.604e-07	3.951e-07	5.602e-07	1.018e-06
B (output stable)	4.373e-06	4.337e-06	2.628e-05	4.386e-05
A to Z	3.317e-07	5.290e-07	9.300e-07	1.681e-06
B to Z	-2.420e-08	-2.900e-09	2.698e-07	5.335e-07
	X27_P0	X41_P0	X55_P0	
A (output stable)	1.721e-06	2.460e-06	3.198e-06	
B (output stable)	7.657e-05	1.024e-04	1.142e-04	
A to Z	2.581e-06	4.488e-06	4.426e-06	
B to Z	1.113e-06	1.772e-06	3.308e-06	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.544	0.6528
X6_P0	1.200	0.544	0.6528
X9_P0	1.200	0.952	1.1424
X13_P0	1.200	0.952	1.1424
X16_P0	1.200	1.360	1.6320
X19_P0	1.200	1.496	1.7952
X22_P0	1.200	1.768	2.1216
X25_P0	1.200	1.904	2.2848
X37_P0	1.200	2.584	3.1008
X49_P0	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P0	X6_P0	X9_P0	X13_P0
A	0.0006	0.0007	0.0011	0.0014
B	0.0006	0.0007	0.0013	0.0015
C	0.0006	0.0007	0.0011	0.0013
	X16_P0	X19_P0	X22_P0	X25_P0
A	0.0019	0.0021	0.0025	0.0028
B	0.0019	0.0026	0.0027	0.0034
C	0.0017	0.0019	0.0023	0.0026
	X37_P0	X49_P0		
A	0.0043	0.0057		
B	0.0045	0.0059		

C	0.0038	0.0053		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0123	0.0116	3.1901	2.3374
A to Z ↑	0.0313	0.0288	17.7757	12.5589
B to Z ↓	0.0117	0.0109	3.1984	2.3414
B to Z ↑	0.0294	0.0267	17.7842	12.5700
C to Z ↓	0.0106	0.0097	3.2142	2.3652
C to Z ↑	0.0265	0.0234	17.8209	12.5910
	X9_P0	**X13_P0**	**X9_P0**	**X13_P0**
A to Z ↓	0.0119	0.0115	1.5532	1.1921
A to Z ↑	0.0312	0.0291	8.3245	6.2011
B to Z ↓	0.0113	0.0107	1.5122	1.1417
B to Z ↑	0.0307	0.0278	8.3317	6.2103
C to Z ↓	0.0090	0.0085	1.5227	1.1602
C to Z ↑	0.0214	0.0197	8.3438	6.2193
	X16_P0	**X19_P0**	**X16_P0**	**X19_P0**
A to Z ↓	0.0118	0.0116	0.9258	0.7800
A to Z ↑	0.0301	0.0297	5.0038	4.1480
B to Z ↓	0.0114	0.0112	0.9286	0.7636
B to Z ↑	0.0290	0.0293	5.0053	4.1509
C to Z ↓	0.0094	0.0092	0.9301	0.7946
C to Z ↑	0.0224	0.0211	5.0164	4.1581
	X22_P0	**X25_P0**	**X22_P0**	**X25_P0**
A to Z ↓	0.0117	0.0116	0.6816	0.5955
A to Z ↑	0.0296	0.0296	3.5720	3.1178
B to Z ↓	0.0112	0.0110	0.6691	0.5731
B to Z ↑	0.0286	0.0290	3.5745	3.1199
C to Z ↓	0.0088	0.0087	0.6747	0.5960
C to Z ↑	0.0208	0.0199	3.5811	3.1265
	X37_P0	**X49_P0**	**X37_P0**	**X49_P0**
A to Z ↓	0.0117	0.0117	0.4106	0.3108
A to Z ↑	0.0287	0.0287	2.0876	1.5705
B to Z ↓	0.0111	0.0111	0.4060	0.3076
B to Z ↑	0.0274	0.0273	2.0893	1.5715
C to Z ↓	0.0090	0.0091	0.4100	0.3108
C to Z ↑	0.0201	0.0202	2.0929	1.5749

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.799e-06	8.218e-10
X6_P0	3.865e-06	8.218e-10
X9_P0	5.662e-06	1.179e-09
X13_P0	7.397e-06	1.179e-09
X16_P0	9.232e-06	1.536e-09
X19_P0	1.119e-05	1.655e-09
X22_P0	1.284e-05	1.894e-09
X25_P0	1.459e-05	2.013e-09
X37_P0	2.109e-05	2.608e-09

X49_P0	2.792e-05	3.323e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	3.014e-05	4.144e-05	7.569e-05	9.876e-05
B (output stable)	1.415e-05	2.074e-05	5.744e-05	6.818e-05
C (output stable)	3.218e-05	4.845e-05	1.152e-04	1.465e-04
A to Z	9.581e-04	1.216e-03	2.029e-03	2.478e-03
B to Z	7.897e-04	9.829e-04	1.729e-03	2.045e-03
C to Z	6.278e-04	7.483e-04	1.061e-03	1.247e-03
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	1.176e-04	1.423e-04	1.689e-04	1.983e-04
B (output stable)	8.083e-05	1.042e-04	1.229e-04	1.435e-04
C (output stable)	1.645e-04	2.109e-04	2.436e-04	2.871e-04
A to Z	3.224e-03	3.821e-03	4.412e-03	5.033e-03
B to Z	2.688e-03	3.239e-03	3.691e-03	4.249e-03
C to Z	1.848e-03	2.065e-03	2.359e-03	2.541e-03
	X37_P0	X49_P0		
A (output stable)	2.866e-04	3.807e-04		
B (output stable)	1.907e-04	2.493e-04		
C (output stable)	4.053e-04	5.345e-04		
A to Z	7.269e-03	9.674e-03		
B to Z	5.966e-03	7.917e-03		
C to Z	3.762e-03	5.016e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

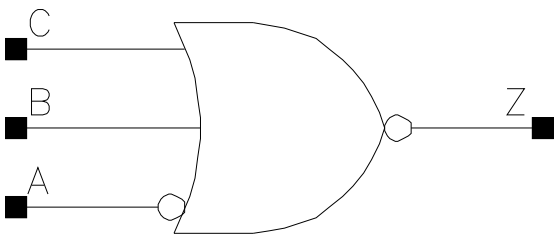
Pin Cycle (vdds)	X4_P0	X6_P0	X9_P0	X13_P0
A (output stable)	-1.836e-07	-1.514e-07	-1.536e-06	-1.507e-06
B (output stable)	8.051e-06	1.020e-05	2.133e-05	2.614e-05
C (output stable)	1.648e-05	2.125e-05	8.198e-05	9.571e-05
A to Z	7.420e-07	7.490e-07	2.637e-06	3.259e-06
B to Z	1.681e-07	2.690e-07	1.715e-06	1.812e-06
C to Z	-1.011e-07	-2.420e-08	-1.188e-07	1.900e-08
	X16_P0	X19_P0	X22_P0	X25_P0
A (output stable)	-1.158e-06	-1.652e-06	-2.208e-06	-2.871e-06
B (output stable)	2.915e-05	4.030e-05	4.428e-05	5.796e-05
C (output stable)	8.033e-05	1.124e-04	1.404e-04	1.756e-04
A to Z	2.776e-06	4.381e-06	4.532e-06	6.496e-06
B to Z	1.186e-06	2.351e-06	2.772e-06	3.650e-06
C to Z	2.281e-07	-6.600e-08	-1.410e-08	1.167e-07
	X37_P0	X49_P0		
A (output stable)	-3.378e-06	-4.383e-06		
B (output stable)	7.415e-05	9.611e-05		
C (output stable)	2.142e-04	2.757e-04		
A to Z	8.332e-06	1.132e-05		
B to Z	4.222e-06	5.305e-06		
C to Z	-1.750e-07	-2.630e-07		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.680	0.8160
X13_P0	1.200	1.224	1.4688
X19_P0	1.200	1.496	1.7952
X25_P0	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0007	0.0009	0.0010	0.0018
B	0.0007	0.0015	0.0022	0.0029
C	0.0007	0.0013	0.0019	0.0026

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X13_P0**	**X6_P0**	**X13_P0**
A to Z ↓	0.0329	0.0311	2.2714	1.2521
A to Z ↑	0.0387	0.0376	12.6823	6.1938
B to Z ↓	0.0111	0.0108	2.3546	1.1474
B to Z ↑	0.0271	0.0281	12.7154	6.2074
C to Z ↓	0.0099	0.0086	2.3676	1.1605
C to Z ↑	0.0238	0.0199	12.7365	6.2189
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0353	0.0309	0.7723	0.5855

A to Z ↑	0.0404	0.0372	4.1573	3.1209
B to Z ↓	0.0113	0.0110	0.7985	0.5952
B to Z ↑	0.0274	0.0274	4.1691	3.1281
C to Z ↓	0.0091	0.0087	0.7955	0.5991
C to Z ↑	0.0213	0.0201	4.1766	3.1342

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P0	6.335e-06	9.409e-10
X13_P0	1.291e-05	1.417e-09
X19_P0	1.553e-05	1.655e-09
X25_P0	2.417e-05	2.251e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	9.811e-04	1.729e-03	2.260e-03	3.362e-03
B (output stable)	2.742e-05	8.755e-05	1.135e-04	1.618e-04
C (output stable)	5.577e-05	1.888e-04	2.258e-04	3.324e-04
A to Z	2.261e-03	4.463e-03	6.127e-03	8.554e-03
B to Z	9.933e-04	2.080e-03	3.011e-03	4.003e-03
C to Z	7.623e-04	1.274e-03	2.055e-03	2.542e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

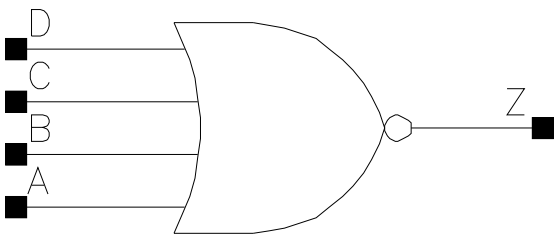
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	1.393e-08	-2.072e-07	-4.766e-07	-7.734e-07
B (output stable)	1.009e-05	2.473e-05	3.368e-05	4.824e-05
C (output stable)	2.105e-05	9.145e-05	9.014e-05	1.478e-04
A to Z	1.227e-06	3.231e-06	3.108e-06	5.780e-06
B to Z	2.380e-07	1.927e-06	7.880e-07	3.176e-06
C to Z	-1.589e-07	4.600e-09	-3.180e-07	-5.093e-07

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X25_P0	1.200	1.904	2.2848
X32_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X32_P0
A	0.0006	0.0006	0.0006	0.0008
B	0.0006	0.0006	0.0008	0.0010
C	0.0005	0.0005	0.0007	0.0008
D	0.0006	0.0005	0.0007	0.0008

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0387	0.0378	2.2264	1.0971
A to Z ↑	0.0617	0.0649	3.8108	1.8802
B to Z ↓	0.0373	0.0367	2.2283	1.0969
B to Z ↑	0.0609	0.0644	3.8133	1.8804
C to Z ↓	0.0384	0.0381	2.2250	1.0938
C to Z ↑	0.0628	0.0671	3.8088	1.8775

D to Z ↓	0.0379	0.0375	2.2232	1.0943
D to Z ↑	0.0626	0.0671	3.8115	1.8795
	X25_P0	**X32_P0**	**X25_P0**	**X32_P0**
A to Z ↓	0.0385	0.0407	0.7640	0.6005
A to Z ↑	0.0636	0.0617	1.2841	0.9743
B to Z ↓	0.0374	0.0394	0.7626	0.6010
B to Z ↑	0.0632	0.0609	1.2834	0.9732
C to Z ↓	0.0371	0.0397	0.7613	0.5989
C to Z ↑	0.0628	0.0617	1.2825	0.9731
D to Z ↓	0.0360	0.0380	0.7608	0.5984
D to Z ↑	0.0623	0.0608	1.2805	0.9725

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	1.032e-05	1.417e-09
X17_P0	1.540e-05	1.536e-09
X25_P0	2.327e-05	2.013e-09
X32_P0	2.923e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	3.996e-04	4.810e-04	6.695e-04	8.581e-04
B (output stable)	3.474e-04	4.300e-04	6.020e-04	7.632e-04
C (output stable)	3.790e-04	4.464e-04	6.846e-04	8.801e-04
D (output stable)	3.290e-04	3.993e-04	6.153e-04	7.850e-04
A to Z	2.783e-03	4.150e-03	6.340e-03	7.962e-03
B to Z	2.655e-03	4.034e-03	6.162e-03	7.739e-03
C to Z	2.846e-03	4.187e-03	5.986e-03	7.530e-03
D to Z	2.715e-03	4.068e-03	5.822e-03	7.302e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

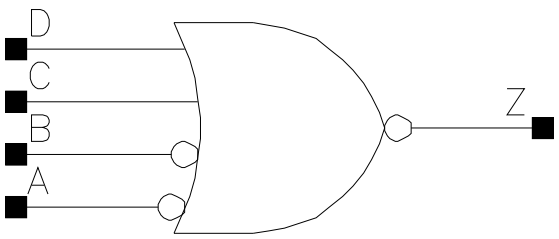
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X32_P0
A (output stable)	7.257e-08	1.281e-07	1.007e-07	1.467e-07
B (output stable)	2.360e-06	2.281e-06	2.719e-06	2.867e-06
C (output stable)	1.595e-07	6.329e-08	1.065e-07	1.107e-07
D (output stable)	2.642e-06	2.615e-06	2.676e-06	2.631e-06
A to Z	-1.490e-08	-1.504e-07	-1.139e-07	-1.734e-07
B to Z	-9.450e-08	-1.853e-07	-3.170e-07	-3.324e-07
C to Z	-1.116e-07	-1.035e-07	-3.050e-07	-1.790e-07
D to Z	5.300e-09	-3.790e-08	-2.235e-07	-1.896e-07

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X13_P0	1.200	1.496	1.7952
X19_P0	1.200	2.040	2.4480
X25_P0	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P0	X13_P0	X19_P0	X25_P0
A	0.0009	0.0009	0.0017	0.0017
B	0.0009	0.0014	0.0017	0.0018
C	0.0007	0.0014	0.0021	0.0027
D	0.0007	0.0013	0.0019	0.0026

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	X13_P0	X6_P0	X13_P0
A to Z ↓	0.0284	0.0351	2.2202	1.1090
A to Z ↑	0.0391	0.0475	12.2188	6.2675
B to Z ↓	0.0268	0.0340	2.2183	1.1072
B to Z ↑	0.0392	0.0483	12.2210	6.2693
C to Z ↓	0.0116	0.0110	2.3816	1.1466
C to Z ↑	0.0274	0.0284	12.2578	6.2852

D to Z ↓	0.0100	0.0088	2.3745	1.1563
D to Z ↑	0.0236	0.0207	12.2729	6.2932
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0308	0.0336	0.7619	0.5752
A to Z ↑	0.0427	0.0461	4.1631	3.1422
B to Z ↓	0.0285	0.0318	0.7604	0.5747
B to Z ↑	0.0423	0.0463	4.1645	3.1423
C to Z ↓	0.0113	0.0111	0.8003	0.6003
C to Z ↑	0.0272	0.0273	4.1735	3.1490
D to Z ↓	0.0091	0.0087	0.7962	0.5990
D to Z ↑	0.0213	0.0200	4.1812	3.1540

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P0	7.492e-06	1.179e-09
X13_P0	1.037e-05	1.655e-09
X19_P0	1.668e-05	2.132e-09
X25_P0	1.890e-05	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	5.975e-04	1.021e-03	1.526e-03	1.845e-03
B (output stable)	5.381e-04	9.591e-04	1.377e-03	1.730e-03
C (output stable)	2.595e-05	8.460e-05	1.190e-04	1.687e-04
D (output stable)	6.216e-05	1.962e-04	2.494e-04	3.816e-04
A to Z	2.687e-03	5.099e-03	7.520e-03	9.671e-03
B to Z	2.542e-03	4.861e-03	6.995e-03	9.217e-03
C to Z	1.037e-03	2.095e-03	2.985e-03	3.942e-03
D to Z	7.924e-04	1.332e-03	2.054e-03	2.494e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

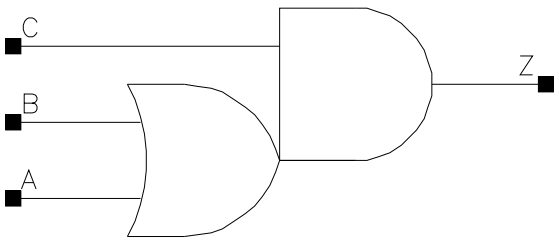
Pin Cycle (vdds)	X6_P0	X13_P0	X19_P0	X25_P0
A (output stable)	8.023e-09	-7.472e-07	-7.184e-07	-9.591e-07
B (output stable)	9.140e-08	-7.864e-07	-3.586e-07	-7.859e-07
C (output stable)	1.343e-05	3.787e-05	5.148e-05	7.076e-05
D (output stable)	2.776e-05	1.030e-04	1.100e-04	1.728e-04
A to Z	1.220e-06	2.902e-06	3.692e-06	5.216e-06
B to Z	1.383e-06	3.065e-06	3.827e-06	5.544e-06
C to Z	2.590e-07	1.954e-06	1.069e-06	2.618e-06
D to Z	2.640e-08	-1.169e-07	-6.200e-08	1.751e-07

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.680	0.8160
X17_P0	1.200	0.816	0.9792
X33_P0	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0008	0.0008	0.0016
B	0.0009	0.0010	0.0018
C	0.0009	0.0009	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
A to Z ↓	0.0341	0.0391	2.3000	1.1489
A to Z ↑	0.0267	0.0294	3.8297	1.8836
B to Z ↓	0.0331	0.0385	2.3006	1.1509
B to Z ↑	0.0246	0.0276	3.8250	1.8800
C to Z ↓	0.0285	0.0312	2.2740	1.1292
C to Z ↑	0.0260	0.0283	3.8215	1.8794
	X33_P0		**X33_P0**	
A to Z ↓	0.0406		0.5838	
A to Z ↑	0.0314		0.9443	

B to Z ↓	0.0400		0.5841	
B to Z ↑	0.0289		0.9425	
C to Z ↓	0.0319		0.5717	
C to Z ↑	0.0293		0.9431	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	1.003e-05	9.409e-10
X17_P0	1.440e-05	1.060e-09
X33_P0	2.833e-05	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	7.007e-05	7.177e-05	1.488e-04
B (output stable)	7.621e-05	7.781e-05	1.536e-04
C (output stable)	6.567e-05	6.795e-05	1.300e-04
A to Z	2.094e-03	3.041e-03	6.330e-03
B to Z	1.859e-03	2.808e-03	5.868e-03
C to Z	2.260e-03	3.161e-03	6.522e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

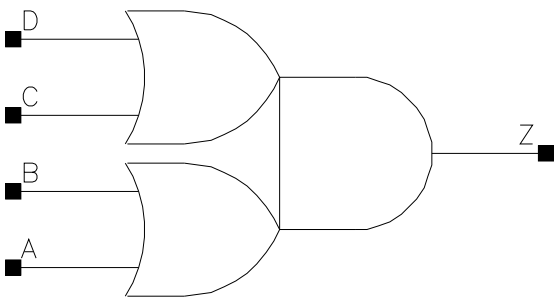
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	-7.182e-08	-1.140e-07	-2.774e-07
B (output stable)	1.374e-06	1.363e-06	3.343e-06
C (output stable)	5.155e-08	5.564e-08	4.893e-08
A to Z	1.423e-07	1.200e-08	6.400e-08
B to Z	-1.143e-07	-1.273e-07	-6.188e-07
C to Z	-5.733e-08	-2.062e-07	-6.294e-07

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X17_P0	1.200	1.088	1.3056
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0005	0.0008	0.0016
B	0.0006	0.0009	0.0016
C	0.0006	0.0009	0.0017
D	0.0006	0.0009	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0569	0.0482	2.2492	1.1420
A to Z ↑	0.0376	0.0324	3.7549	1.8763
B to Z ↓	0.0569	0.0478	2.2500	1.1422
B to Z ↑	0.0364	0.0310	3.7526	1.8753

C to Z ↓	0.0501	0.0430	2.2294	1.1355
C to Z ↑	0.0359	0.0318	3.7513	1.8767
D to Z ↓	0.0490	0.0419	2.2296	1.1360
D to Z ↑	0.0340	0.0296	3.7491	1.8734
	X33_P0		**X33_P0**	
A to Z ↓	0.0485		0.5890	
A to Z ↑	0.0322		0.9435	
B to Z ↓	0.0459		0.5895	
B to Z ↑	0.0300		0.9413	
C to Z ↓	0.0425		0.5852	
C to Z ↑	0.0309		0.9423	
D to Z ↓	0.0396		0.5860	
D to Z ↑	0.0285		0.9398	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	9.078e-06	1.179e-09
X17_P0	1.747e-05	1.298e-09
X33_P0	3.266e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	2.408e-05	3.937e-05	1.122e-04
B (output stable)	2.409e-05	4.298e-05	1.442e-04
C (output stable)	6.021e-05	7.804e-05	1.853e-04
D (output stable)	6.109e-05	8.219e-05	2.254e-04
A to Z	2.456e-03	3.940e-03	7.746e-03
B to Z	2.335e-03	3.694e-03	7.019e-03
C to Z	2.139e-03	3.496e-03	6.794e-03
D to Z	2.008e-03	3.247e-03	6.066e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

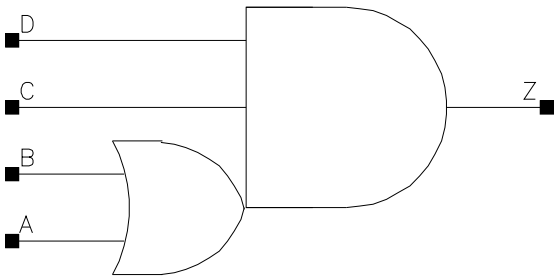
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	9.332e-08	1.331e-07	4.813e-08
B (output stable)	2.718e-06	2.758e-06	3.350e-05
C (output stable)	-1.327e-07	9.873e-08	-1.586e-07
D (output stable)	2.700e-06	3.029e-06	3.033e-05
A to Z	-1.145e-07	-2.577e-07	1.032e-06
B to Z	-1.258e-07	-2.755e-07	-2.963e-07
C to Z	7.253e-08	9.383e-08	1.759e-06
D to Z	-5.692e-08	-9.798e-08	1.361e-07

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X17_P0	1.200	1.088	1.3056
X25_P0	1.200	1.904	2.2848
X33_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P0	X17_P0	X25_P0	X33_P0
A	0.0006	0.0009	0.0014	0.0017
B	0.0006	0.0009	0.0014	0.0017
C	0.0006	0.0009	0.0015	0.0017
D	0.0006	0.0009	0.0014	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0486	0.0452	2.3644	1.1533
A to Z ↑	0.0437	0.0396	3.8914	1.8843
B to Z ↓	0.0484	0.0431	2.3672	1.1541
B to Z ↑	0.0415	0.0360	3.8863	1.8801
C to Z ↓	0.0378	0.0346	2.3014	1.1286

C to Z ↑	0.0426	0.0380	3.8786	1.8776
D to Z ↓	0.0368	0.0335	2.3007	1.1272
D to Z ↑	0.0436	0.0389	3.8812	1.8775
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**
A to Z ↓	0.0472	0.0454	0.7834	0.5871
A to Z ↑	0.0405	0.0407	1.2766	0.9561
B to Z ↓	0.0450	0.0431	0.7843	0.5882
B to Z ↑	0.0375	0.0374	1.2724	0.9552
C to Z ↓	0.0363	0.0348	0.7658	0.5747
C to Z ↑	0.0391	0.0386	1.2741	0.9543
D to Z ↓	0.0346	0.0334	0.7642	0.5735
D to Z ↑	0.0390	0.0389	1.2733	0.9541

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	6.253e-06	1.060e-09
X17_P0	1.270e-05	1.298e-09
X25_P0	1.971e-05	2.013e-09
X33_P0	2.486e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	5.899e-05	1.130e-04	1.897e-04	2.117e-04
B (output stable)	6.035e-05	1.158e-04	1.996e-04	2.202e-04
C (output stable)	1.801e-05	3.714e-05	9.084e-05	1.009e-04
D (output stable)	2.489e-05	5.207e-05	1.704e-04	1.831e-04
A to Z	2.055e-03	3.608e-03	5.851e-03	7.196e-03
B to Z	1.940e-03	3.271e-03	5.323e-03	6.521e-03
C to Z	2.197e-03	3.790e-03	6.265e-03	7.554e-03
D to Z	2.114e-03	3.627e-03	5.840e-03	7.113e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

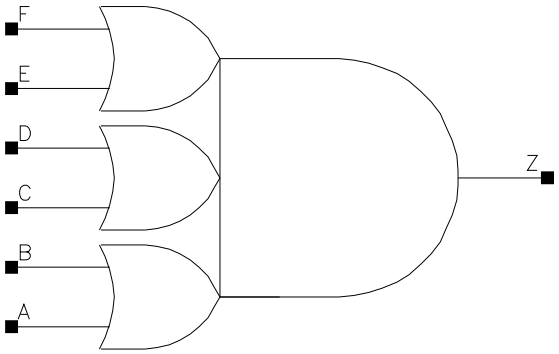
Pin Cycle (vdds)	X8_P0	X17_P0	X25_P0	X33_P0
A (output stable)	-3.297e-07	-3.778e-07	-5.579e-07	5.909e-09
B (output stable)	3.453e-07	3.994e-06	6.058e-06	7.370e-06
C (output stable)	6.821e-08	6.358e-08	5.992e-08	3.242e-08
D (output stable)	1.348e-08	-2.383e-08	-1.284e-07	2.068e-08
A to Z	-3.630e-08	4.310e-07	5.920e-07	5.850e-07
B to Z	-8.343e-08	-1.664e-07	-2.261e-07	-6.588e-07
C to Z	-6.370e-08	2.841e-07	4.395e-07	3.696e-07
D to Z	-7.090e-08	2.784e-07	8.636e-07	5.634e-07

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	1.224	1.4688
X17_P0	1.200	1.360	1.6320
X33_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
A	0.0006	0.0008	0.0014
B	0.0006	0.0008	0.0016
C	0.0006	0.0008	0.0015
D	0.0006	0.0008	0.0017
E	0.0006	0.0009	0.0015
F	0.0006	0.0009	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X17_P0	X8_P0	X17_P0
A to Z ↓	0.0649	0.0544	2.4243	1.1760
A to Z ↑	0.0487	0.0428	3.8589	1.8968
B to Z ↓	0.0645	0.0543	2.4249	1.1761
B to Z ↑	0.0471	0.0413	3.8597	1.8963
C to Z ↓	0.0598	0.0515	2.4082	1.1728
C to Z ↑	0.0486	0.0424	3.8615	1.8967
D to Z ↓	0.0597	0.0511	2.4087	1.1728
D to Z ↑	0.0467	0.0405	3.8565	1.8957
E to Z ↓	0.0520	0.0455	2.3856	1.1644
E to Z ↑	0.0443	0.0394	3.8600	1.8965
F to Z ↓	0.0521	0.0447	2.3852	1.1654
F to Z ↑	0.0424	0.0372	3.8536	1.8936
	X33_P0		X33_P0	
A to Z ↓	0.0551		0.6021	
A to Z ↑	0.0442		0.9570	
B to Z ↓	0.0552		0.6021	
B to Z ↑	0.0417		0.9547	
C to Z ↓	0.0513		0.5985	
C to Z ↑	0.0436		0.9568	
D to Z ↓	0.0510		0.5982	
D to Z ↑	0.0413		0.9544	
E to Z ↓	0.0453		0.5943	
E to Z ↑	0.0406		0.9561	
F to Z ↓	0.0451		0.5948	
F to Z ↑	0.0381		0.9541	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	8.736e-06	1.417e-09
X17_P0	1.708e-05	1.536e-09
X33_P0	3.239e-05	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X17_P0	X33_P0
A (output stable)	2.160e-05	3.705e-05	6.947e-05
B (output stable)	2.158e-05	4.323e-05	7.659e-05
C (output stable)	3.349e-05	5.546e-05	1.113e-04
D (output stable)	3.492e-05	5.889e-05	1.183e-04
E (output stable)	9.526e-05	1.373e-04	2.619e-04
F (output stable)	9.270e-05	1.375e-04	2.678e-04
A to Z	2.817e-03	4.577e-03	9.038e-03
B to Z	2.686e-03	4.344e-03	8.600e-03
C to Z	2.573e-03	4.237e-03	8.314e-03
D to Z	2.451e-03	3.998e-03	7.854e-03
E to Z	2.245e-03	3.750e-03	7.376e-03
F to Z	2.134e-03	3.512e-03	6.943e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

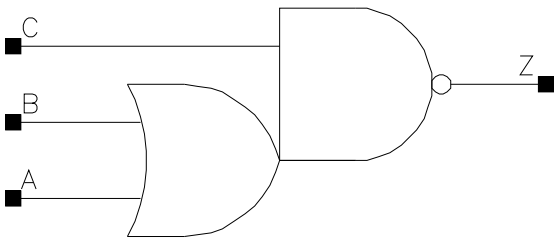
Pin Cycle (vdds)	X8_P0	X17_P0	X33_P0
A (output stable)	9.574e-08	1.193e-07	1.437e-07
B (output stable)	1.872e-06	2.098e-06	3.927e-06
C (output stable)	4.315e-08	9.373e-08	-3.415e-08
D (output stable)	1.786e-06	2.059e-06	3.835e-06
E (output stable)	-3.042e-07	6.515e-08	-5.951e-07
F (output stable)	1.620e-06	1.985e-06	3.181e-06
A to Z	-2.653e-07	2.810e-07	-8.467e-08
B to Z	-1.820e-07	1.529e-07	8.611e-08
C to Z	-1.776e-07	-1.392e-07	-2.082e-07
D to Z	-7.721e-08	-3.158e-07	-3.644e-07
E to Z	-9.944e-09	2.287e-07	3.381e-07
F to Z	3.791e-08	3.478e-09	-3.133e-08

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.544	0.6528
X17_P0	1.200	1.360	1.6320
X34_P0	1.200	2.720	3.2640
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P0	X17_P0	X34_P0	X46_P0
A	0.0007	0.0020	0.0042	0.0054
B	0.0007	0.0019	0.0038	0.0050
C	0.0007	0.0021	0.0044	0.0056

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X17_P0**	**X6_P0**	**X17_P0**
A to Z ↓	0.0140	0.0146	4.4848	1.4753
A to Z ↑	0.0205	0.0218	8.1900	2.7547
B to Z ↓	0.0119	0.0124	4.4084	1.4888
B to Z ↑	0.0189	0.0188	8.2167	2.7667
C to Z ↓	0.0142	0.0143	4.0788	1.3557
C to Z ↑	0.0180	0.0178	3.8538	1.2776
	X34_P0	**X46_P0**	**X34_P0**	**X46_P0**
A to Z ↓	0.0153	0.0152	0.7518	0.5734

A to Z ↑	0.0227	0.0222	1.3755	1.0522
B to Z ↓	0.0127	0.0127	0.7603	0.5819
B to Z ↑	0.0192	0.0191	1.3819	1.0560
C to Z ↓	0.0149	0.0147	0.6928	0.5290
C to Z ↑	0.0181	0.0180	0.6391	0.4882

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P0	5.866e-06	8.218e-10
X17_P0	1.625e-05	1.536e-09
X34_P0	3.208e-05	2.727e-09
X46_P0	4.208e-05	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	6.045e-05	2.198e-04	4.615e-04	5.695e-04
B (output stable)	6.744e-05	2.309e-04	4.955e-04	5.920e-04
C (output stable)	5.981e-05	1.984e-04	4.225e-04	5.264e-04
A to Z	9.419e-04	3.065e-03	6.435e-03	8.252e-03
B to Z	7.137e-04	2.162e-03	4.482e-03	5.824e-03
C to Z	1.108e-03	3.396e-03	7.090e-03	9.140e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

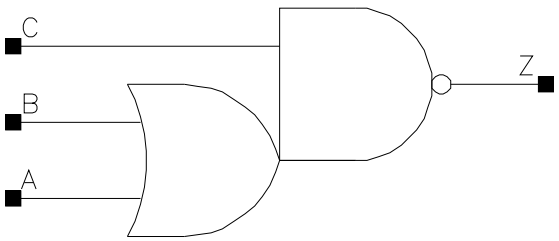
Pin Cycle (vdds)	X6_P0	X17_P0	X34_P0	X46_P0
A (output stable)	8.626e-08	-3.144e-07	-9.631e-07	-1.113e-06
B (output stable)	1.574e-06	1.307e-05	3.469e-05	3.465e-05
C (output stable)	5.491e-08	-1.130e-08	-1.002e-07	-1.753e-07
A to Z	3.957e-07	1.086e-06	1.798e-06	2.683e-06
B to Z	1.110e-08	4.580e-07	-3.190e-07	-6.760e-07
C to Z	1.477e-07	1.103e-06	1.541e-06	2.555e-06

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.544	0.6528
X11_P0	1.200	0.952	1.1424
X17_P0	1.200	1.360	1.6320
X23_P0	1.200	1.904	2.2848
X46_P0	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P0	X11_P0	X17_P0	X23_P0
A	0.0007	0.0014	0.0021	0.0029
B	0.0007	0.0015	0.0020	0.0026
C	0.0007	0.0014	0.0020	0.0027
	X46_P0			
A	0.0059			
B	0.0053			
C	0.0055			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X11_P0	X5_P0	X11_P0
A to Z ↓	0.0153	0.0156	4.5672	2.1398
A to Z ↑	0.0248	0.0250	8.6157	4.0587
B to Z ↓	0.0135	0.0137	4.5020	2.0891

B to Z ↑	0.0234	0.0236	8.6412	4.0719
C to Z ↓	0.0118	0.0118	4.2350	1.9742
C to Z ↑	0.0143	0.0141	4.1096	1.9314
	X17_P0	**X23_P0**	**X17_P0**	**X23_P0**
A to Z ↓	0.0149	0.0158	1.4781	1.0952
A to Z ↑	0.0236	0.0261	2.6937	2.0480
B to Z ↓	0.0131	0.0136	1.4735	1.0946
B to Z ↑	0.0220	0.0229	2.7024	2.0563
C to Z ↓	0.0114	0.0117	1.3783	1.0198
C to Z ↑	0.0132	0.0136	1.2854	0.9774
	X46_P0		**X46_P0**	
A to Z ↓	0.0157		0.5706	
A to Z ↑	0.0256		1.0338	
B to Z ↓	0.0134		0.5660	
B to Z ↑	0.0224		1.0372	
C to Z ↓	0.0118		0.5293	
C to Z ↑	0.0133		0.4939	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P0	5.861e-06	8.218e-10
X11_P0	1.156e-05	1.179e-09
X17_P0	1.676e-05	1.536e-09
X23_P0	2.259e-05	2.013e-09
X46_P0	4.293e-05	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	2.597e-05	5.689e-05	8.190e-05	1.493e-04
B (output stable)	2.661e-05	6.169e-05	8.738e-05	1.626e-04
C (output stable)	1.383e-04	3.514e-04	4.157e-04	6.494e-04
A to Z	1.178e-03	2.541e-03	3.493e-03	5.317e-03
B to Z	9.310e-04	2.042e-03	2.707e-03	3.905e-03
C to Z	7.059e-04	1.538e-03	2.093e-03	3.030e-03
	X46_P0			
A (output stable)	2.863e-04			
B (output stable)	3.076e-04			
C (output stable)	1.197e-03			
A to Z	1.026e-02			
B to Z	7.439e-03			
C to Z	5.804e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X5_P0	X11_P0	X17_P0	X23_P0
A (output stable)	8.900e-08	1.417e-07	1.907e-07	2.745e-08
B (output stable)	1.574e-06	3.734e-06	5.372e-06	2.678e-05
C (output stable)	4.316e-08	-4.377e-07	-5.790e-08	-6.631e-07
A to Z	1.904e-07	-1.277e-06	9.780e-07	-1.576e-06
B to Z	-4.437e-07	-5.980e-07	-8.670e-07	-1.620e-06
C to Z	1.574e-07	4.567e-08	1.284e-06	2.585e-06

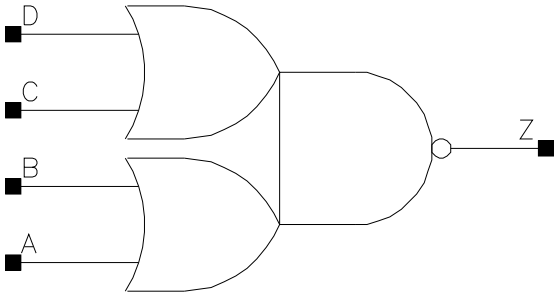
	X46_P0			
A (output stable)	1.400e-07			
B (output stable)	4.449e-05			
C (output stable)	-1.136e-06			
A to Z	1.073e-06			
B to Z	-2.888e-06			
C to Z	5.803e-06			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.680	0.8160
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.448	2.9376
X42_P0	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0008	0.0014	0.0021	0.0029
B	0.0007	0.0013	0.0019	0.0027
C	0.0007	0.0014	0.0020	0.0028
D	0.0007	0.0013	0.0018	0.0025
	X42_P0			
A	0.0059			
B	0.0053			
C	0.0056			
D	0.0051			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0167	0.0177	4.1563	2.0866
A to Z ↑	0.0286	0.0289	9.0181	4.1501
B to Z ↓	0.0151	0.0156	4.0833	2.0897
B to Z ↑	0.0269	0.0254	9.0311	4.1649
C to Z ↓	0.0144	0.0155	4.1976	2.0932
C to Z ↑	0.0217	0.0232	8.8516	4.1546
D to Z ↓	0.0124	0.0128	4.1132	2.1032
D to Z ↑	0.0198	0.0188	8.8789	4.1775
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0170	0.0173	1.4304	1.0293
A to Z ↑	0.0271	0.0281	2.7861	2.0555
B to Z ↓	0.0152	0.0152	1.4375	1.0275
B to Z ↑	0.0245	0.0251	2.7965	2.0622
C to Z ↓	0.0148	0.0150	1.4360	1.0332
C to Z ↑	0.0214	0.0221	2.7908	2.0552
D to Z ↓	0.0126	0.0124	1.4540	1.0359
D to Z ↑	0.0180	0.0181	2.8063	2.0646
	X42_P0		**X42_P0**	
A to Z ↓	0.0176		0.5379	
A to Z ↑	0.0281		1.0429	
B to Z ↓	0.0154		0.5324	
B to Z ↑	0.0251		1.0458	
C to Z ↓	0.0157		0.5413	
C to Z ↑	0.0224		1.0375	
D to Z ↓	0.0129		0.5368	
D to Z ↑	0.0185		1.0420	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P0	6.790e-06	9.409e-10
X10_P0	1.400e-05	1.536e-09
X15_P0	1.969e-05	1.894e-09
X21_P0	2.602e-05	2.489e-09
X42_P0	5.027e-05	4.395e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	3.499e-05	1.088e-04	1.431e-04	2.078e-04
B (output stable)	3.882e-05	1.402e-04	1.663e-04	2.425e-04
C (output stable)	6.178e-05	1.729e-04	2.236e-04	3.262e-04
D (output stable)	6.889e-05	2.060e-04	2.466e-04	3.588e-04
A to Z	1.429e-03	3.267e-03	4.426e-03	6.311e-03
B to Z	1.191e-03	2.515e-03	3.444e-03	4.883e-03
C to Z	1.016e-03	2.420e-03	3.209e-03	4.555e-03
D to Z	7.971e-04	1.682e-03	2.282e-03	3.178e-03
	X42_P0			
A (output stable)	4.116e-04			
B (output stable)	4.792e-04			
C (output stable)	6.422e-04			
D (output stable)	7.128e-04			

A to Z	1.246e-02			
B to Z	9.645e-03			
C to Z	9.138e-03			
D to Z	6.398e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

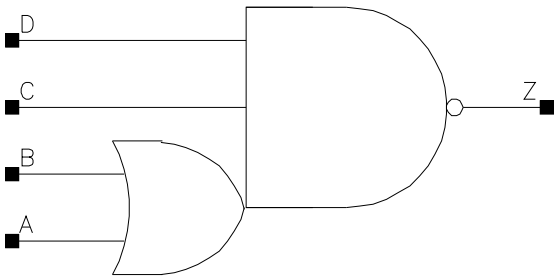
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	1.405e-07	3.802e-08	1.968e-07	-4.337e-08
B (output stable)	3.478e-06	3.207e-05	2.113e-05	4.665e-05
C (output stable)	4.170e-08	-2.076e-07	-1.784e-08	-5.278e-07
D (output stable)	2.879e-06	3.121e-05	2.030e-05	4.584e-05
A to Z	-2.543e-07	7.057e-07	-7.377e-07	-3.873e-07
B to Z	-4.378e-07	-7.377e-07	-1.518e-06	-2.167e-06
C to Z	3.565e-07	2.400e-06	1.686e-06	2.939e-06
D to Z	2.843e-08	3.587e-07	3.157e-07	5.787e-07
	X42_P0			
A (output stable)	2.069e-07			
B (output stable)	8.309e-05			
C (output stable)	-5.530e-07			
D (output stable)	8.149e-05			
A to Z	1.160e-07			
B to Z	-4.195e-06			
C to Z	4.548e-06			
D to Z	1.115e-06			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X21_P0	1.200	2.448	2.9376
X31_P0	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X21_P0	X31_P0
A	0.0007	0.0013	0.0027	0.0040
B	0.0009	0.0013	0.0024	0.0037
C	0.0007	0.0014	0.0028	0.0043
D	0.0007	0.0014	0.0027	0.0040

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0208	0.0197	5.9651	3.1649
A to Z ↑	0.0275	0.0252	8.1487	4.0978
B to Z ↓	0.0188	0.0164	5.9821	3.1684
B to Z ↑	0.0259	0.0217	8.1975	4.1178
C to Z ↓	0.0200	0.0203	5.6379	2.9881

C to Z ↑	0.0217	0.0211	3.7467	1.8880
D to Z ↓	0.0209	0.0198	5.6530	2.9994
D to Z ↑	0.0209	0.0195	3.7903	1.8903
	X21_P0	**X31_P0**	**X21_P0**	**X31_P0**
A to Z ↓	0.0200	0.0202	1.6483	1.1174
A to Z ↑	0.0248	0.0247	2.0500	1.3741
B to Z ↓	0.0165	0.0168	1.6546	1.1247
B to Z ↑	0.0213	0.0213	2.0563	1.3808
C to Z ↓	0.0202	0.0204	1.5579	1.0574
C to Z ↑	0.0207	0.0207	0.9567	0.6450
D to Z ↓	0.0200	0.0202	1.5633	1.0614
D to Z ↑	0.0191	0.0192	0.9573	0.6437

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P0	5.195e-06	1.060e-09
X10_P0	9.587e-06	1.536e-09
X21_P0	1.787e-05	2.489e-09
X31_P0	2.617e-05	3.442e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	1.099e-04	2.359e-04	4.329e-04	6.427e-04
B (output stable)	1.105e-04	2.422e-04	4.408e-04	6.553e-04
C (output stable)	3.512e-05	1.024e-04	1.982e-04	2.919e-04
D (output stable)	4.802e-05	1.881e-04	3.363e-04	4.947e-04
A to Z	1.486e-03	2.568e-03	4.986e-03	7.413e-03
B to Z	1.147e-03	1.852e-03	3.562e-03	5.345e-03
C to Z	1.699e-03	3.226e-03	6.188e-03	9.204e-03
D to Z	1.554e-03	2.746e-03	5.275e-03	7.869e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

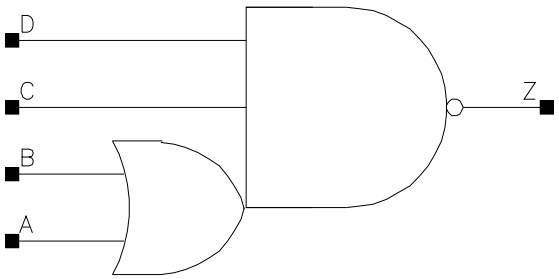
Pin Cycle (vdds)	X5_P0	X10_P0	X21_P0	X31_P0
A (output stable)	-3.592e-07	-6.218e-07	-1.618e-06	-2.144e-06
B (output stable)	3.937e-06	6.469e-06	9.963e-06	1.354e-05
C (output stable)	4.847e-08	2.595e-08	-8.840e-09	-3.794e-08
D (output stable)	-1.252e-08	-1.831e-07	-5.286e-07	-7.518e-07
A to Z	7.820e-07	1.206e-06	1.157e-06	1.436e-06
B to Z	-8.710e-08	3.180e-07	8.090e-07	1.108e-06
C to Z	5.236e-07	-1.943e-07	-1.009e-06	-1.354e-06
D to Z	6.474e-07	2.470e-07	3.500e-07	4.900e-07

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.816	0.9792
X10_P0	1.200	1.360	1.6320
X15_P0	1.200	1.768	2.1216
X21_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X15_P0	X21_P0
A	0.0008	0.0015	0.0022	0.0030
B	0.0007	0.0013	0.0020	0.0027
C	0.0007	0.0014	0.0021	0.0027
D	0.0007	0.0013	0.0020	0.0026

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0201	0.0217	6.0867	3.1576
A to Z ↑	0.0287	0.0311	7.9714	4.0518
B to Z ↓	0.0180	0.0190	5.9904	3.1526
B to Z ↑	0.0275	0.0283	7.9893	4.0618
C to Z ↓	0.0164	0.0183	5.7334	2.9945

C to Z ↑	0.0174	0.0183	3.8098	1.9246
D to Z ↓	0.0159	0.0165	5.7499	3.0036
D to Z ↑	0.0158	0.0159	3.8300	1.9368
	X15_P0	**X21_P0**	**X15_P0**	**X21_P0**
A to Z ↓	0.0213	0.0216	2.1736	1.6349
A to Z ↑	0.0298	0.0305	2.7233	2.0611
B to Z ↓	0.0188	0.0188	2.1692	1.6299
B to Z ↑	0.0274	0.0281	2.7308	2.0662
C to Z ↓	0.0179	0.0182	2.0574	1.5478
C to Z ↑	0.0175	0.0179	1.2839	0.9663
D to Z ↓	0.0162	0.0166	2.0643	1.5527
D to Z ↑	0.0153	0.0156	1.2915	0.9718

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P0	5.108e-06	1.060e-09
X10_P0	9.799e-06	1.536e-09
X15_P0	1.356e-05	1.894e-09
X21_P0	1.847e-05	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	2.210e-05	4.911e-05	7.354e-05	9.650e-05
B (output stable)	2.163e-05	5.513e-05	7.415e-05	1.016e-04
C (output stable)	4.851e-05	1.183e-04	1.776e-04	2.378e-04
D (output stable)	8.326e-05	3.177e-04	3.756e-04	5.582e-04
A to Z	1.618e-03	3.558e-03	4.998e-03	6.876e-03
B to Z	1.348e-03	2.822e-03	3.965e-03	5.447e-03
C to Z	1.073e-03	2.425e-03	3.348e-03	4.644e-03
D to Z	9.226e-04	1.935e-03	2.731e-03	3.726e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

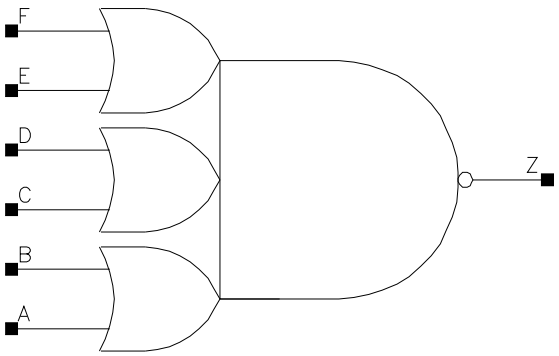
Pin Cycle (vdds)	X5_P0	X10_P0	X15_P0	X21_P0
A (output stable)	8.823e-08	1.343e-07	1.238e-07	1.238e-07
B (output stable)	7.931e-07	7.805e-06	5.656e-06	1.183e-05
C (output stable)	4.030e-08	-4.703e-08	-1.775e-07	-1.999e-07
D (output stable)	4.333e-08	-6.551e-07	-7.204e-07	-1.223e-06
A to Z	3.530e-07	1.217e-06	-7.270e-07	2.867e-06
B to Z	-1.420e-07	-2.410e-07	-2.191e-06	-2.620e-07
C to Z	4.047e-07	1.102e-06	6.130e-07	1.225e-06
D to Z	3.823e-07	1.550e-06	1.069e-06	2.086e-06

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	1.200	1.088	1.3056
X9_P0	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X9_P0
A	0.0006	0.0015
B	0.0006	0.0013
C	0.0006	0.0014
D	0.0006	0.0013
E	0.0006	0.0014
F	0.0006	0.0013

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X9_P0	X3_P0	X9_P0
A to Z ↓	0.0254	0.0265	7.0268	2.8565
A to Z ↑	0.0383	0.0364	11.2181	4.0729
B to Z ↓	0.0241	0.0239	7.0612	2.8568
B to Z ↑	0.0382	0.0337	11.2347	4.0821
C to Z ↓	0.0244	0.0249	7.0687	2.8654
C to Z ↑	0.0337	0.0319	11.2330	4.0635
D to Z ↓	0.0227	0.0222	7.0949	2.8681
D to Z ↑	0.0332	0.0290	11.2546	4.0764
E to Z ↓	0.0203	0.0213	7.0805	2.8587
E to Z ↑	0.0268	0.0260	11.2527	4.0650
F to Z ↓	0.0187	0.0182	7.1069	2.8613
F to Z ↑	0.0262	0.0223	11.2898	4.0826

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X3_P0	6.209e-06	1.298e-09
X9_P0	1.569e-05	2.132e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X3_P0	X9_P0
A (output stable)	2.931e-05	1.011e-04
B (output stable)	3.096e-05	1.200e-04
C (output stable)	4.742e-05	1.421e-04
D (output stable)	4.857e-05	1.650e-04
E (output stable)	1.212e-04	3.035e-04
F (output stable)	1.247e-04	3.190e-04
A to Z	1.889e-03	4.917e-03
B to Z	1.713e-03	4.159e-03
C to Z	1.557e-03	4.036e-03
D to Z	1.387e-03	3.349e-03
E to Z	1.148e-03	3.128e-03
F to Z	9.910e-04	2.418e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

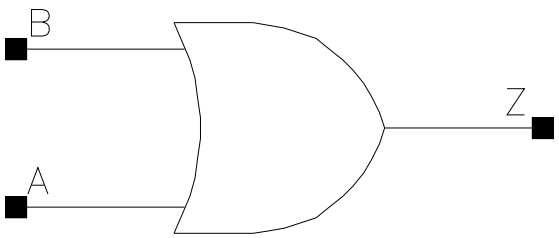
Pin Cycle (vdds)	X3_P0	X9_P0
A (output stable)	1.020e-07	8.530e-08
B (output stable)	1.847e-06	2.136e-05
C (output stable)	4.753e-08	-6.030e-10
D (output stable)	1.937e-06	2.006e-05
E (output stable)	-2.309e-07	-6.631e-07
F (output stable)	1.529e-06	2.001e-05
A to Z	2.281e-07	2.817e-06
B to Z	-2.328e-07	8.278e-07
C to Z	-4.567e-08	2.950e-06
D to Z	-1.934e-07	6.673e-07
E to Z	4.927e-07	3.563e-06
F to Z	1.166e-07	1.452e-06

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.544	0.6528
X16_P0	1.200	0.680	0.8160
X33_P0	1.200	1.360	1.6320
X50_P0	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P0	X16_P0	X33_P0	X50_P0
A	0.0007	0.0008	0.0016	0.0017
B	0.0006	0.0008	0.0017	0.0017

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0442	0.0388	2.3066	1.1648
A to Z ↑	0.0254	0.0258	3.7859	1.9057
B to Z ↓	0.0429	0.0377	2.3094	1.1643
B to Z ↑	0.0242	0.0242	3.7849	1.9050
	X33_P0	**X50_P0**	**X33_P0**	**X50_P0**
A to Z ↓	0.0401	0.0468	0.5761	0.3980
A to Z ↑	0.0256	0.0254	0.9297	0.6278
B to Z ↓	0.0374	0.0444	0.5768	0.3983
B to Z ↑	0.0237	0.0239	0.9287	0.6270

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	8.199e-06	8.218e-10
X16_P0	1.495e-05	9.409e-10
X33_P0	2.912e-05	1.536e-09
X50_P0	3.866e-05	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	2.173e-05	4.106e-05	1.322e-04	1.254e-04
B (output stable)	2.545e-05	4.813e-05	1.900e-04	1.788e-04
A to Z	1.850e-03	2.943e-03	6.201e-03	8.359e-03
B to Z	1.717e-03	2.710e-03	5.473e-03	7.686e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

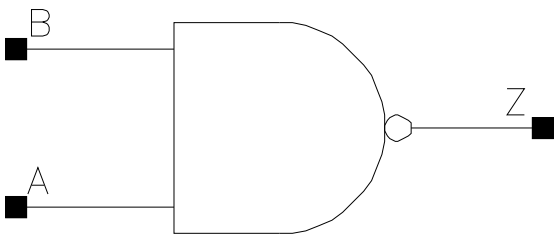
Pin Cycle (vdds)	X8_P0	X16_P0	X33_P0	X50_P0
A (output stable)	1.012e-07	1.709e-07	-4.042e-08	7.253e-08
B (output stable)	4.703e-06	5.566e-06	5.207e-05	4.887e-05
A to Z	5.416e-08	1.057e-07	1.061e-06	1.220e-07
B to Z	-1.892e-07	1.263e-08	-2.498e-07	1.389e-07

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.816	0.9792
X16_P0	1.200	0.952	1.1424
X24_P0	1.200	1.088	1.3056
X32_P0	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P0	X16_P0	X24_P0	X32_P0
A	0.0008	0.0009	0.0009	0.0008
B	0.0009	0.0010	0.0010	0.0010

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0351	0.0362	2.2312	1.1612
A to Z ↑	0.0378	0.0385	3.8195	1.9471
B to Z ↓	0.0359	0.0371	2.2289	1.1621
B to Z ↑	0.0365	0.0367	3.8264	1.9473
	X24_P0	**X32_P0**	**X24_P0**	**X32_P0**
A to Z ↓	0.0396	0.0405	0.7879	0.5939
A to Z ↑	0.0409	0.0419	1.2999	0.9708
B to Z ↓	0.0406	0.0415	0.7872	0.5940
B to Z ↑	0.0391	0.0406	1.3028	0.9736

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	1.490e-05	1.060e-09
X16_P0	1.993e-05	1.179e-09
X24_P0	2.460e-05	1.298e-09
X32_P0	3.138e-05	1.417e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	2.431e-05	2.443e-05	2.413e-05	2.588e-05
B (output stable)	2.795e-05	2.807e-05	2.825e-05	2.780e-05
A to Z	3.549e-03	4.083e-03	5.135e-03	6.761e-03
B to Z	3.413e-03	3.958e-03	5.017e-03	6.626e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

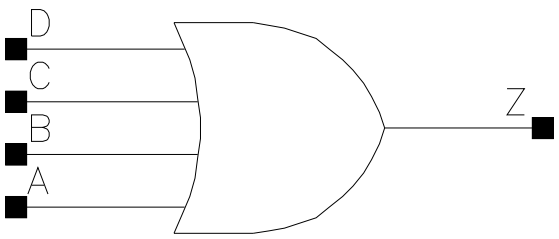
Pin Cycle (vdds)	X8_P0	X16_P0	X24_P0	X32_P0
A (output stable)	4.295e-08	4.428e-08	4.353e-08	5.123e-08
B (output stable)	4.636e-08	4.581e-08	4.604e-08	3.350e-08
A to Z	-9.720e-08	-3.733e-07	-4.401e-07	-2.451e-07
B to Z	-1.532e-07	-1.077e-07	-4.314e-07	-1.000e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X27_P0	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X27_P0
A	0.0015	0.0017
B	0.0014	0.0017
C	0.0015	0.0017
D	0.0014	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	**X27_P0**	**X20_P0**	**X27_P0**
A to Z ↓	0.0450	0.0468	1.4625	1.0940
A to Z ↑	0.0269	0.0258	1.2449	0.9283
B to Z ↓	0.0426	0.0439	1.4617	1.0943
B to Z ↑	0.0254	0.0241	1.2437	0.9267
C to Z ↓	0.0430	0.0450	1.4611	1.0935
C to Z ↑	0.0257	0.0253	1.2462	0.9309
D to Z ↓	0.0409	0.0425	1.4608	1.0927
D to Z ↑	0.0243	0.0237	1.2451	0.9305

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X20_P0	2.203e-05	2.251e-09
X27_P0	3.046e-05	2.608e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X20_P0	X27_P0
A (output stable)	1.366e-03	1.884e-03
B (output stable)	1.158e-03	1.595e-03
C (output stable)	1.236e-03	1.772e-03
D (output stable)	1.032e-03	1.515e-03
A to Z	5.740e-03	8.019e-03
B to Z	5.220e-03	7.262e-03
C to Z	5.122e-03	7.062e-03
D to Z	4.623e-03	6.392e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

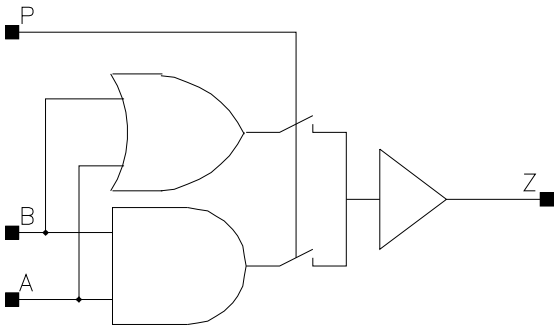
Pin Cycle (vdds)	X20_P0	X27_P0
A (output stable)	1.223e-07	2.250e-07
B (output stable)	1.335e-05	3.006e-05
C (output stable)	1.749e-07	2.335e-07
D (output stable)	1.327e-05	3.242e-05
A to Z	5.340e-08	5.188e-07
B to Z	-3.170e-07	-3.120e-07
C to Z	4.627e-07	1.677e-06
D to Z	6.800e-08	-7.800e-08

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	0.952	1.1424
X16_P0	1.200	1.224	1.4688
X25_P0	1.200	2.040	2.4480
X33_P0	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P0	X16_P0	X25_P0	X33_P0
A	0.0011	0.0016	0.0027	0.0027
B	0.0010	0.0015	0.0031	0.0031
P	0.0006	0.0008	0.0016	0.0016

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0535	0.0481	2.3640	1.1549
A to Z ↑	0.0352	0.0320	3.8424	1.9197
B to Z ↓	0.0528	0.0475	2.3780	1.1621
B to Z ↑	0.0359	0.0327	3.8437	1.9206
P to Z ↓	0.0474	0.0432	2.3774	1.1630
P to Z ↑	0.0342	0.0314	3.8412	1.9161
	X25_P0	**X33_P0**	**X25_P0**	**X33_P0**

A to Z ↓	0.0461	0.0492	0.7857	0.5963
A to Z ↑	0.0318	0.0334	1.2892	0.9661
B to Z ↓	0.0454	0.0480	0.7899	0.5987
B to Z ↑	0.0328	0.0340	1.2911	0.9662
P to Z ↓	0.0420	0.0448	0.7909	0.5997
P to Z ↑	0.0311	0.0324	1.2882	0.9648

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	8.164e-06	1.179e-09
X16_P0	1.671e-05	1.417e-09
X25_P0	2.746e-05	2.132e-09
X33_P0	3.160e-05	2.251e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	4.749e-05	7.766e-05	1.711e-04	1.737e-04
B (output stable)	5.042e-05	9.291e-05	2.320e-04	2.340e-04
P (output stable)	1.048e-04	1.932e-04	3.181e-04	3.296e-04
A to Z	2.155e-03	3.635e-03	6.267e-03	7.260e-03
B to Z	2.092e-03	3.530e-03	6.021e-03	7.007e-03
P to Z	1.883e-03	3.227e-03	5.595e-03	6.575e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

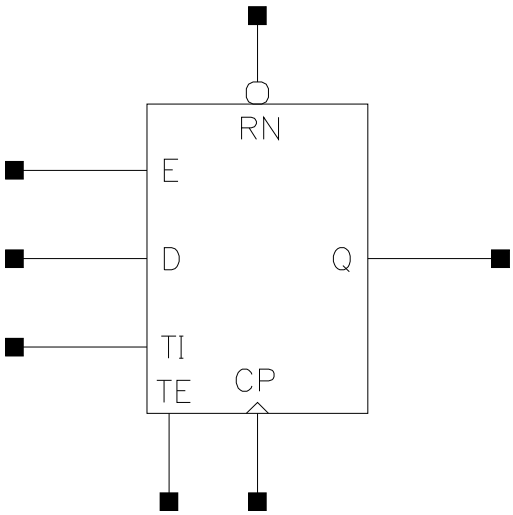
Pin Cycle (vdds)	X8_P0	X16_P0	X25_P0	X33_P0
A (output stable)	3.650e-08	1.458e-07	2.539e-07	2.635e-07
B (output stable)	2.377e-06	2.471e-06	1.109e-05	1.102e-05
P (output stable)	1.232e-05	1.727e-05	1.694e-05	1.746e-05
A to Z	2.311e-07	3.440e-07	-1.110e-07	-1.330e-07
B to Z	1.775e-07	3.118e-07	-3.186e-07	-1.925e-08
P to Z	-9.443e-08	-4.455e-08	-1.869e-07	-1.299e-07

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.488	5.3856
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
E	0.0008	0.0009	0.0009	0.0009
RN	0.0007	0.0006	0.0006	0.0007
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.1030	0.0509	5.2472	2.2927
CP to Q ↑	0.0797	0.0659	7.8906	3.7970
RN to Q ↓	0.0811	0.0674	4.4174	2.4268
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0885	0.0925	1.1151	0.5872
CP to Q ↑	0.1081	0.1124	1.8626	0.9502
RN to Q ↓	0.1169	0.1207	1.1121	0.5850

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1480	0.0992	0.0992	0.0992
CP ↑	min_pulse_width to CP	0.0970	0.0407	0.0358	0.0358
D ↓	hold_rising to CP	-0.1551	-0.0774	-0.0774	-0.0774
D ↑	hold_rising to CP	-0.0894	-0.0312	-0.0312	-0.0312
D ↓	setup_rising to CP	0.2194	0.1371	0.1371	0.1371
D ↑	setup_rising to CP	0.1292	0.0658	0.0658	0.0658
E ↓	hold_rising to CP	-0.1013	-0.1010	-0.1062	-0.1062
E ↑	hold_rising to CP	-0.0876	-0.0312	-0.0312	-0.0312
E ↓	setup_rising to CP	0.1824	0.1828	0.1802	0.1828
E ↑	setup_rising to CP	0.2075	0.1416	0.1416	0.1416
RN ↓	min_pulse_width to RN	0.0850	0.0925	0.0854	0.0854
RN ↑	recovery_rising to CP	0.0244	0.0244	0.0244	0.0244
RN ↑	removal_rising to CP	-0.0175	-0.0078	-0.0074	-0.0074
TE ↓	hold_rising to CP	-0.0769	-0.0503	-0.0534	-0.0530
TE ↑	hold_rising to CP	-0.0576	-0.0353	-0.0383	-0.0383
TE ↓	setup_rising to CP	0.1385	0.1093	0.1093	0.1093
TE ↑	setup_rising to CP	0.2686	0.1856	0.1886	0.1886
TI ↓	hold_rising to CP	-0.2003	-0.1084	-0.1082	-0.1082
TI ↑	hold_rising to CP	-0.0707	-0.0374	-0.0408	-0.0408
TI ↓	setup_rising to CP	0.2629	0.1689	0.1689	0.1730
TI ↑	setup_rising to CP	0.1088	0.0769	0.0769	0.0769

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.892e-05	4.557e-09
X8_P0	3.157e-05	4.276e-09
X17_P0	3.917e-05	4.514e-09
X33_P0	4.835e-05	4.752e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

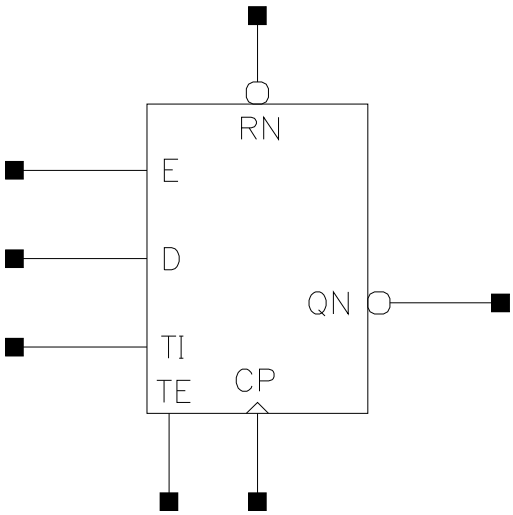
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.375e-03	3.396e-03	3.401e-03	3.404e-03
Clock 100Mhz Data 25Mhz	5.565e-03	5.641e-03	6.166e-03	6.774e-03
Clock 100Mhz Data 50Mhz	7.755e-03	7.887e-03	8.930e-03	1.014e-02
Clock = 0 Data 100Mhz	4.971e-03	4.768e-03	4.701e-03	4.669e-03
Clock = 1 Data 100Mhz	1.877e-03	1.895e-03	1.902e-03	1.906e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.760	5.7120
X8_P0	1.200	4.624	5.5488
X17_P0	1.200	4.760	5.7120
X33_P0	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
E	0.0008	0.0009	0.0009	0.0009
RN	0.0007	0.0007	0.0007	0.0007
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0988	0.0901	4.3063	2.2125
CP to QN ↑	0.1155	0.0683	7.7177	3.7000
RN to QN ↑	0.0997	0.0989	7.6961	3.6919
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0852	0.0898	1.1137	0.5868
CP to QN ↑	0.0712	0.0769	1.8638	0.9516
RN to QN ↑	0.0964	0.1053	1.8732	0.9554

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1480	0.0992	0.0992	0.0992
CP ↑	min_pulse_width to CP	0.0685	0.0358	0.0406	0.0455
D ↓	hold_rising to CP	-0.1599	-0.0774	-0.0774	-0.0774
D ↑	hold_rising to CP	-0.0894	-0.0312	-0.0312	-0.0312
D ↓	setup_rising to CP	0.2194	0.1371	0.1371	0.1371
D ↑	setup_rising to CP	0.1265	0.0658	0.0658	0.0658
E ↓	hold_rising to CP	-0.1010	-0.1062	-0.1010	-0.1013
E ↑	hold_rising to CP	-0.0876	-0.0312	-0.0312	-0.0312
E ↓	setup_rising to CP	0.1873	0.1802	0.1828	0.1828
E ↑	setup_rising to CP	0.2075	0.1416	0.1416	0.1416
RN ↓	min_pulse_width to RN	0.0850	0.0854	0.0947	0.1018
RN ↑	recovery_rising to CP	0.0244	0.0272	0.0244	0.0244
RN ↑	removal_rising to CP	-0.0175	-0.0126	-0.0078	-0.0078
TE ↓	hold_rising to CP	-0.0769	-0.0503	-0.0503	-0.0503
TE ↑	hold_rising to CP	-0.0601	-0.0383	-0.0356	-0.0356
TE ↓	setup_rising to CP	0.1389	0.1093	0.1093	0.1093
TE ↑	setup_rising to CP	0.2690	0.1886	0.1886	0.1886
TI ↓	hold_rising to CP	-0.2038	-0.1082	-0.1084	-0.1084
TI ↑	hold_rising to CP	-0.0707	-0.0408	-0.0374	-0.0374
TI ↓	setup_rising to CP	0.2634	0.1730	0.1730	0.1730
TI ↑	setup_rising to CP	0.1088	0.0769	0.0769	0.0769

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.996e-05	4.557e-09
X8_P0	3.290e-05	4.395e-09
X17_P0	4.041e-05	4.514e-09
X33_P0	5.038e-05	4.752e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

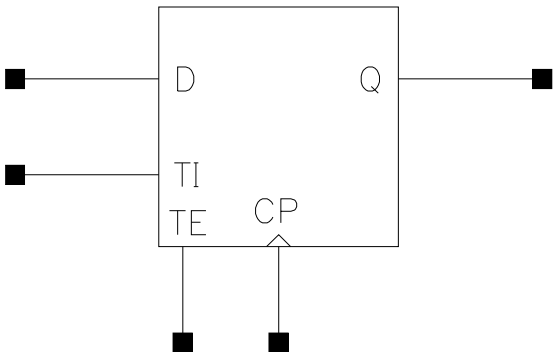
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.374e-03	3.395e-03	3.398e-03	3.400e-03
Clock 100Mhz Data 25Mhz	5.527e-03	5.674e-03	6.129e-03	6.742e-03
Clock 100Mhz Data 50Mhz	7.680e-03	7.953e-03	8.860e-03	1.008e-02
Clock = 0 Data 100Mhz	4.971e-03	4.769e-03	4.703e-03	4.670e-03
Clock = 1 Data 100Mhz	1.875e-03	1.896e-03	1.903e-03	1.908e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.400	4.0800
X8_P0	1.200	3.128	3.7536
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.0835	0.0473	4.9078	2.2884
CP to Q ↑	0.0711	0.0595	7.9237	3.7444
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0721	0.0784	1.0911	0.5766
CP to Q ↑	0.1041	0.1095	1.8595	0.9473

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1306	0.1355	0.1355	0.1355
CP ↑	min_pulse_width to CP	0.0674	0.0359	0.0359	0.0359
D ↓	hold_rising to CP	-0.0965	-0.0440	-0.0437	-0.0437
D ↑	hold_rising to CP	-0.0357	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1410	0.0932	0.0929	0.0929
D ↑	setup_rising to CP	0.0655	0.0335	0.0366	0.0366
TE ↓	hold_rising to CP	-0.0567	-0.0357	-0.0353	-0.0353
TE ↑	hold_rising to CP	-0.0481	-0.0282	-0.0312	-0.0312
TE ↓	setup_rising to CP	0.1194	0.0877	0.0877	0.0877
TE ↑	setup_rising to CP	0.2319	0.1856	0.1856	0.1856
TI ↓	hold_rising to CP	-0.1941	-0.1195	-0.1195	-0.1195
TI ↑	hold_rising to CP	-0.0545	-0.0290	-0.0285	-0.0285
TI ↓	setup_rising to CP	0.2398	0.1785	0.1785	0.1785
TI ↑	setup_rising to CP	0.0893	0.0637	0.0637	0.0637

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.308e-05	3.323e-09
X8_P0	2.623e-05	3.085e-09
X17_P0	3.665e-05	3.442e-09
X33_P0	4.477e-05	3.680e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

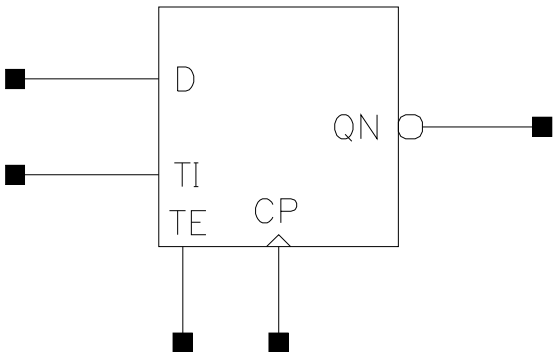
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.024e-03	3.047e-03	3.052e-03	3.054e-03
Clock 100Mhz Data 25Mhz	4.539e-03	4.587e-03	5.102e-03	5.604e-03
Clock 100Mhz Data 50Mhz	6.055e-03	6.127e-03	7.152e-03	8.153e-03
Clock = 0 Data 100Mhz	3.874e-03	3.636e-03	3.556e-03	3.517e-03
Clock = 1 Data 100Mhz	1.071e-03	5.579e-04	3.869e-04	3.014e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.536	4.2432
X8_P0	1.200	3.264	3.9168
X17_P0	1.200	3.536	4.2432
X33_P0	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0925	0.0957	4.9686	2.2891
CP to QN ↑	0.0919	0.0629	7.8639	3.6999
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0718	0.0785	1.0926	0.5766
CP to QN ↑	0.0614	0.0670	1.8558	0.9469

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1288	0.1355	0.1361	0.1355
CP ↑	min_pulse_width to CP	0.0540	0.0359	0.0359	0.0396
D ↓	hold_rising to CP	-0.0965	-0.0437	-0.0440	-0.0440
D ↑	hold_rising to CP	-0.0357	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1410	0.0932	0.0929	0.0929
D ↑	setup_rising to CP	0.0655	0.0335	0.0335	0.0335
TE ↓	hold_rising to CP	-0.0567	-0.0353	-0.0357	-0.0357
TE ↑	hold_rising to CP	-0.0478	-0.0312	-0.0282	-0.0282
TE ↓	setup_rising to CP	0.1198	0.0877	0.0877	0.0877
TE ↑	setup_rising to CP	0.2319	0.1856	0.1856	0.1856
TI ↓	hold_rising to CP	-0.1900	-0.1195	-0.1200	-0.1200
TI ↑	hold_rising to CP	-0.0545	-0.0285	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.2383	0.1785	0.1785	0.1785
TI ↑	setup_rising to CP	0.0893	0.0637	0.0637	0.0637

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.348e-05	3.442e-09
X8_P0	2.653e-05	3.204e-09
X17_P0	3.625e-05	3.442e-09
X33_P0	4.437e-05	3.680e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

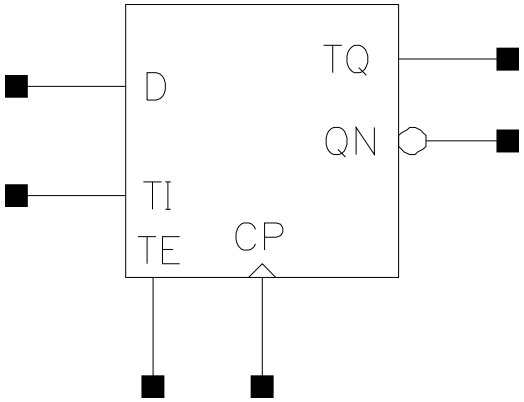
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	2.986e-03	3.026e-03	3.039e-03	3.045e-03
Clock 100Mhz Data 25Mhz	4.525e-03	4.657e-03	5.060e-03	5.560e-03
Clock 100Mhz Data 50Mhz	6.063e-03	6.287e-03	7.081e-03	8.075e-03
Clock = 0 Data 100Mhz	3.886e-03	3.640e-03	3.558e-03	3.517e-03
Clock = 1 Data 100Mhz	1.065e-03	5.547e-04	3.847e-04	2.998e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.536	4.2432
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0011	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0009

TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.1023	0.0844	4.4528	2.2201
CP to QN ↑	0.1109	0.0652	7.7432	3.7180
CP to TQ ↓	0.0773	0.0439	6.2794	4.3019
CP to TQ ↑	0.0736	0.0595	15.3366	10.7165
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0790	0.0845	1.1182	0.5884
CP to QN ↑	0.0665	0.0704	1.8827	0.9653
CP to TQ ↓	0.0458	0.0477	5.8258	5.8414
CP to TQ ↑	0.0606	0.0622	14.1980	15.1088

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1287	0.1355	0.1355	0.1355
CP ↑	min_pulse_width to CP	0.0674	0.0359	0.0359	0.0407
D ↓	hold_rising to CP	-0.0965	-0.0409	-0.0409	-0.0409
D ↑	hold_rising to CP	-0.0357	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1414	0.0932	0.0932	0.0932
D ↑	setup_rising to CP	0.0655	0.0366	0.0366	0.0366
TE ↓	hold_rising to CP	-0.0567	-0.0357	-0.0357	-0.0360
TE ↑	hold_rising to CP	-0.0481	-0.0312	-0.0312	-0.0282
TE ↓	setup_rising to CP	0.1173	0.0877	0.0877	0.0877
TE ↑	setup_rising to CP	0.2319	0.1831	0.1831	0.1831
TI ↓	hold_rising to CP	-0.1905	-0.1200	-0.1200	-0.1200
TI ↑	hold_rising to CP	-0.0545	-0.0290	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.2383	0.1787	0.1787	0.1787
TI ↑	setup_rising to CP	0.0893	0.0637	0.0637	0.0637

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.588e-05	3.689e-09
X8_P0	2.957e-05	3.442e-09
X17_P0	3.471e-05	3.561e-09
X33_P0	4.436e-05	3.799e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0

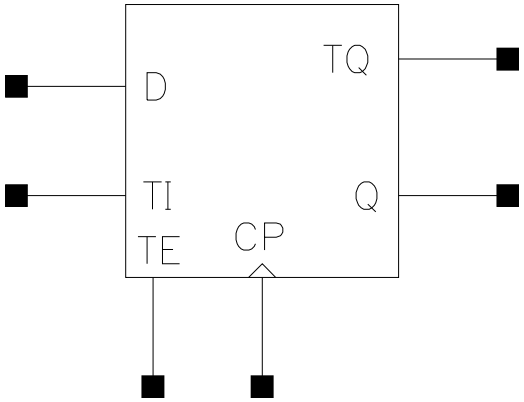
Clock 100Mhz Data 0Mhz	3.081e-03	3.075e-03	3.073e-03	3.073e-03
Clock 100Mhz Data 25Mhz	4.771e-03	4.880e-03	5.089e-03	5.658e-03
Clock 100Mhz Data 50Mhz	6.462e-03	6.685e-03	7.105e-03	8.244e-03
Clock = 0 Data 100Mhz	3.886e-03	3.645e-03	3.565e-03	3.526e-03
Clock = 1 Data 100Mhz	1.071e-03	5.578e-04	3.868e-04	3.013e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.672	4.4064
X8_P0	1.200	3.400	4.0800
X17_P0	1.200	3.672	4.4064
X33_P0	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006

TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.1105	0.0532	5.2152	2.2857
CP to Q ↑	0.0815	0.0631	8.0511	3.7690
CP to TQ ↓	0.1066	0.0565	5.2061	5.9828
CP to TQ ↑	0.0841	0.0704	10.8185	15.3788
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0739	0.0804	1.1212	0.5882
CP to Q ↑	0.1059	0.1113	1.8963	0.9526
CP to TQ ↓	0.0772	0.0852	5.6692	5.7759
CP to TQ ↑	0.1127	0.1205	14.7079	14.8455

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1306	0.1355	0.1361	0.1355
CP ↑	min_pulse_width to CP	0.0976	0.0407	0.0359	0.0359
D ↓	hold_rising to CP	-0.0965	-0.0409	-0.0437	-0.0437
D ↑	hold_rising to CP	-0.0357	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1410	0.0932	0.0929	0.0929
D ↑	setup_rising to CP	0.0655	0.0366	0.0366	0.0366
TE ↓	hold_rising to CP	-0.0567	-0.0360	-0.0353	-0.0353
TE ↑	hold_rising to CP	-0.0478	-0.0282	-0.0312	-0.0312
TE ↓	setup_rising to CP	0.1198	0.0877	0.0877	0.0877
TE ↑	setup_rising to CP	0.2319	0.1831	0.1856	0.1856
TI ↓	hold_rising to CP	-0.1905	-0.1200	-0.1195	-0.1195
TI ↑	hold_rising to CP	-0.0545	-0.0290	-0.0285	-0.0285
TI ↓	setup_rising to CP	0.2398	0.1785	0.1785	0.1785
TI ↑	setup_rising to CP	0.0893	0.0637	0.0637	0.0637

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.576e-05	3.561e-09
X8_P0	2.795e-05	3.323e-09
X17_P0	3.798e-05	3.561e-09
X33_P0	4.604e-05	3.799e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

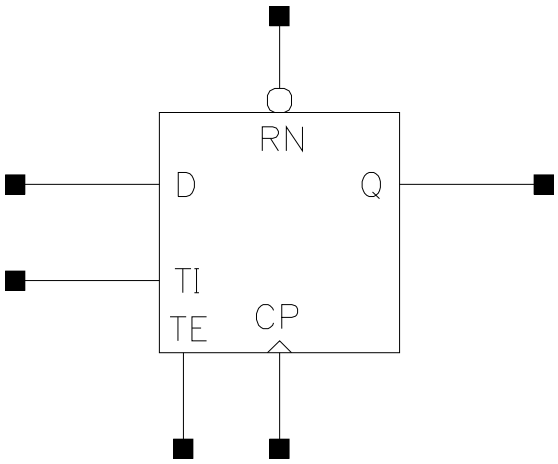
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.009e-03	3.037e-03	3.045e-03	3.049e-03
Clock 100Mhz Data 25Mhz	4.810e-03	4.758e-03	5.249e-03	5.785e-03
Clock 100Mhz Data 50Mhz	6.612e-03	6.479e-03	7.453e-03	8.521e-03
Clock = 0 Data 100Mhz	3.868e-03	3.631e-03	3.554e-03	3.515e-03
Clock = 1 Data 100Mhz	1.063e-03	5.537e-04	3.841e-04	2.993e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.672	4.4064
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
RN	0.0007	0.0006	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.1014	0.0507	5.3456	2.2974
CP to Q ↑	0.0784	0.0644	7.9434	3.7922
RN to Q ↓	0.0800	0.0682	4.4949	2.4067
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0756	0.0825	1.1053	0.5852
CP to Q ↑	0.0949	0.1001	1.8544	0.9471
RN to Q ↓	0.1046	0.1115	1.1033	0.5837

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1457	0.1428	0.1452	0.1446
CP ↑	min_pulse_width to CP	0.0879	0.0396	0.0359	0.0359
D ↓	hold_rising to CP	-0.0867	-0.0290	-0.0286	-0.0286
D ↑	hold_rising to CP	-0.0402	-0.0117	-0.0117	-0.0117
D ↓	setup_rising to CP	0.1414	0.0880	0.0901	0.0901
D ↑	setup_rising to CP	0.0752	0.0467	0.0467	0.0467
RN ↓	min_pulse_width to RN	0.0823	0.0876	0.0833	0.0833
RN ↑	recovery_rising to CP	0.0241	0.0272	0.0272	0.0272
RN ↑	removal_rising to CP	-0.0175	-0.0126	-0.0126	-0.0126
TE ↓	hold_rising to CP	-0.0625	-0.0293	-0.0293	-0.0293
TE ↑	hold_rising to CP	-0.0579	-0.0361	-0.0414	-0.0414
TE ↓	setup_rising to CP	0.1198	0.0883	0.0881	0.0881
TE ↑	setup_rising to CP	0.2319	0.1786	0.1782	0.1782
TI ↓	hold_rising to CP	-0.1745	-0.1005	-0.1005	-0.1005
TI ↑	hold_rising to CP	-0.0643	-0.0387	-0.0387	-0.0387
TI ↓	setup_rising to CP	0.2390	0.1743	0.1743	0.1743
TI ↑	setup_rising to CP	0.1044	0.0789	0.0784	0.0784

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.574e-05	3.799e-09
X8_P0	2.798e-05	3.561e-09
X17_P0	3.761e-05	3.918e-09
X33_P0	4.508e-05	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.376e-03	3.389e-03	3.409e-03	3.420e-03

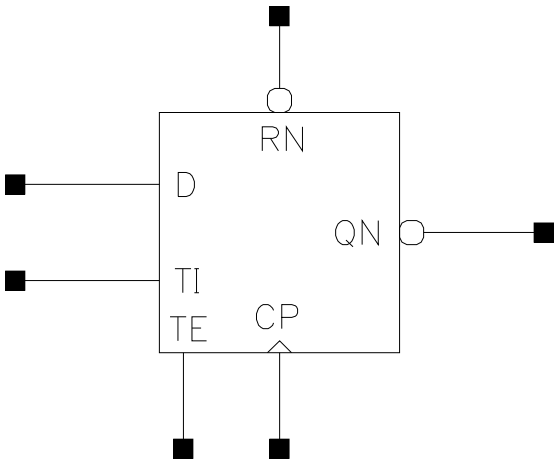
Clock 100Mhz Data 25Mhz	5.129e-03	5.064e-03	5.665e-03	6.203e-03
Clock 100Mhz Data 50Mhz	6.881e-03	6.740e-03	7.920e-03	8.986e-03
Clock = 0 Data 100Mhz	3.976e-03	3.674e-03	3.575e-03	3.526e-03
Clock = 1 Data 100Mhz	1.092e-03	5.696e-04	3.957e-04	3.088e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	3.944	4.7328
X33_P0	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0888	0.0799	4.1943	2.1495
CP to QN ↑	0.1051	0.0615	7.7120	3.6752
RN to QN ↑	0.0920	0.0929	7.6932	3.6729
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0785	0.0855	1.1075	0.5848
CP to QN ↑	0.0674	0.0736	1.8713	0.9578
RN to QN ↑	0.0930	0.1014	1.8778	0.9605

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1457	0.1409	0.1428	0.1428
CP ↑	min_pulse_width to CP	0.0637	0.0359	0.0406	0.0444
D ↓	hold_rising to CP	-0.0867	-0.0290	-0.0290	-0.0290
D ↑	hold_rising to CP	-0.0398	-0.0117	-0.0117	-0.0117
D ↓	setup_rising to CP	0.1414	0.0880	0.0876	0.0876
D ↑	setup_rising to CP	0.0752	0.0467	0.0467	0.0467
RN ↓	min_pulse_width to RN	0.0823	0.0833	0.0920	0.0969
RN ↑	recovery_rising to CP	0.0241	0.0293	0.0272	0.0272
RN ↑	removal_rising to CP	-0.0175	-0.0126	-0.0126	-0.0126
TE ↓	hold_rising to CP	-0.0650	-0.0293	-0.0262	-0.0237
TE ↑	hold_rising to CP	-0.0579	-0.0383	-0.0361	-0.0361
TE ↓	setup_rising to CP	0.1198	0.0883	0.0883	0.0883
TE ↑	setup_rising to CP	0.2319	0.1789	0.1786	0.1786
TI ↓	hold_rising to CP	-0.1743	-0.1005	-0.1005	-0.0966
TI ↑	hold_rising to CP	-0.0658	-0.0387	-0.0387	-0.0387
TI ↓	setup_rising to CP	0.2390	0.1743	0.1743	0.1743
TI ↑	setup_rising to CP	0.1044	0.0789	0.0789	0.0784

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.697e-05	3.844e-09
X8_P0	2.932e-05	3.680e-09
X17_P0	3.816e-05	3.799e-09
X33_P0	4.667e-05	4.037e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.343e-03	3.371e-03	3.380e-03	3.384e-03

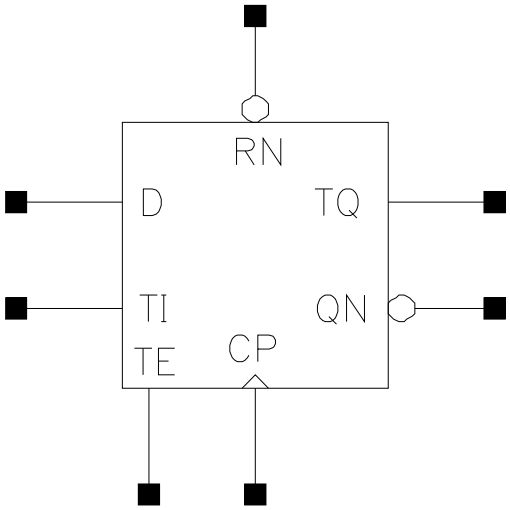
Clock 100Mhz Data 25Mhz	5.029e-03	5.071e-03	5.548e-03	6.046e-03
Clock 100Mhz Data 50Mhz	6.716e-03	6.771e-03	7.717e-03	8.708e-03
Clock = 0 Data 100Mhz	3.975e-03	3.671e-03	3.575e-03	3.527e-03
Clock = 1 Data 100Mhz	1.090e-03	5.690e-04	3.953e-04	3.085e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006

RN	0.0009	0.0006	0.0007	0.0007
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.0992	0.0828	4.2197	2.2619
CP to QN ↑	0.1370	0.0691	6.8924	3.8173
CP to TQ ↓	0.0970	0.0469	5.6544	4.4628
CP to TQ ↑	0.0823	0.0656	12.3115	11.3030
RN to QN ↑	0.0911	0.0906	6.9529	3.8125
RN to TQ ↓	0.0621	0.0612	4.9623	4.6936
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0849	0.0907	1.1265	0.5961
CP to QN ↑	0.0691	0.0722	1.9075	0.9608
CP to TQ ↓	0.0491	0.0508	5.6519	5.5405
CP to TQ ↑	0.0656	0.0671	10.5708	10.7392
RN to QN ↑	0.0925	0.0975	1.9068	0.9607
RN to TQ ↓	0.0657	0.0686	5.8638	5.7788

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1457	0.1428	0.1446	0.1446
CP ↑	min_pulse_width to CP	0.0927	0.0401	0.0407	0.0407
D ↓	hold_rising to CP	-0.0867	-0.0290	-0.0290	-0.0290
D ↑	hold_rising to CP	-0.0402	-0.0117	-0.0117	-0.0117
D ↓	setup_rising to CP	0.1410	0.0880	0.0876	0.0876
D ↑	setup_rising to CP	0.0752	0.0467	0.0467	0.0467
RN ↓	min_pulse_width to RN	0.0872	0.0850	0.0898	0.0920
RN ↑	recovery_rising to CP	0.0296	0.0272	0.0272	0.0272
RN ↑	removal_rising to CP	-0.0193	-0.0126	-0.0126	-0.0126
TE ↓	hold_rising to CP	-0.0650	-0.0293	-0.0268	-0.0237
TE ↑	hold_rising to CP	-0.0579	-0.0361	-0.0383	-0.0383
TE ↓	setup_rising to CP	0.1198	0.0883	0.0883	0.0883
TE ↑	setup_rising to CP	0.2319	0.1786	0.1786	0.1786
TI ↓	hold_rising to CP	-0.1745	-0.1005	-0.1005	-0.0966
TI ↑	hold_rising to CP	-0.0658	-0.0387	-0.0387	-0.0387
TI ↓	setup_rising to CP	0.2390	0.1743	0.1743	0.1743
TI ↑	setup_rising to CP	0.1039	0.0789	0.0784	0.0784

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.885e-05	3.918e-09
X8_P0	3.090e-05	3.680e-09
X17_P0	3.688e-05	3.918e-09
X33_P0	4.669e-05	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

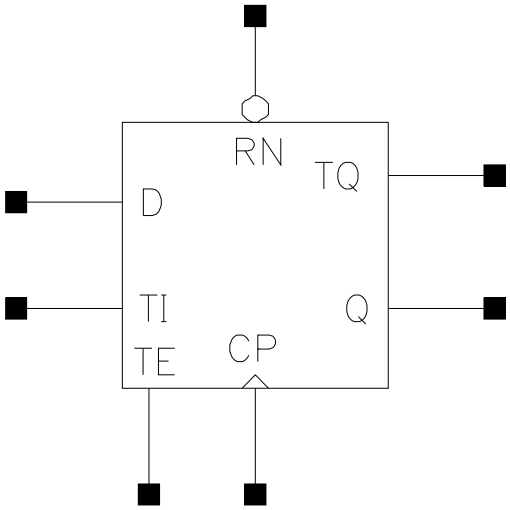
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.346e-03	3.372e-03	3.398e-03	3.412e-03
Clock 100Mhz Data 25Mhz	5.224e-03	5.205e-03	5.481e-03	6.078e-03
Clock 100Mhz Data 50Mhz	7.103e-03	7.038e-03	7.564e-03	8.745e-03
Clock = 0 Data 100Mhz	3.970e-03	3.670e-03	3.569e-03	3.519e-03
Clock = 1 Data 100Mhz	1.090e-03	5.689e-04	3.952e-04	3.084e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0006	0.0006	0.0006

RN	0.0007	0.0008	0.0006	0.0006
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.1141	0.0551	5.6728	2.3640
CP to Q ↑	0.0837	0.0671	8.2434	3.9182
CP to TQ ↓	0.1090	0.0562	7.1643	6.0232
CP to TQ ↑	0.0874	0.0713	16.9025	15.2633
RN to Q ↓	0.0828	0.0772	4.7342	2.4877
RN to TQ ↓	0.0815	0.0778	6.1358	6.2761
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0786	0.0853	1.1238	0.5943
CP to Q ↑	0.0961	0.1011	1.8669	0.9509
CP to TQ ↓	0.0822	0.0911	5.7096	5.8079
CP to TQ ↑	0.1027	0.1109	14.8725	14.9314
RN to Q ↓	0.1077	0.1144	1.1210	0.5931
RN to TQ ↓	0.1113	0.1201	5.7096	5.8044

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1457	0.1428	0.1428	0.1428
CP ↑	min_pulse_width to CP	0.1024	0.0444	0.0359	0.0359
D ↓	hold_rising to CP	-0.0867	-0.0290	-0.0290	-0.0286
D ↑	hold_rising to CP	-0.0398	-0.0117	-0.0117	-0.0117
D ↓	setup_rising to CP	0.1414	0.0876	0.0876	0.0876
D ↑	setup_rising to CP	0.0752	0.0467	0.0467	0.0467
RN ↓	min_pulse_width to RN	0.0872	0.0947	0.0833	0.0833
RN ↑	recovery_rising to CP	0.0244	0.0268	0.0272	0.0272
RN ↑	removal_rising to CP	-0.0175	-0.0126	-0.0126	-0.0126
TE ↓	hold_rising to CP	-0.0629	-0.0237	-0.0293	-0.0293
TE ↑	hold_rising to CP	-0.0579	-0.0361	-0.0383	-0.0383
TE ↓	setup_rising to CP	0.1198	0.0883	0.0883	0.0883
TE ↑	setup_rising to CP	0.2326	0.1786	0.1786	0.1786
TI ↓	hold_rising to CP	-0.1704	-0.0951	-0.1005	-0.1005
TI ↑	hold_rising to CP	-0.0658	-0.0387	-0.0387	-0.0387
TI ↓	setup_rising to CP	0.2349	0.1743	0.1743	0.1743
TI ↑	setup_rising to CP	0.1044	0.0789	0.0789	0.0789

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.663e-05	3.918e-09
X8_P0	2.914e-05	3.680e-09
X17_P0	3.823e-05	3.918e-09
X33_P0	4.572e-05	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

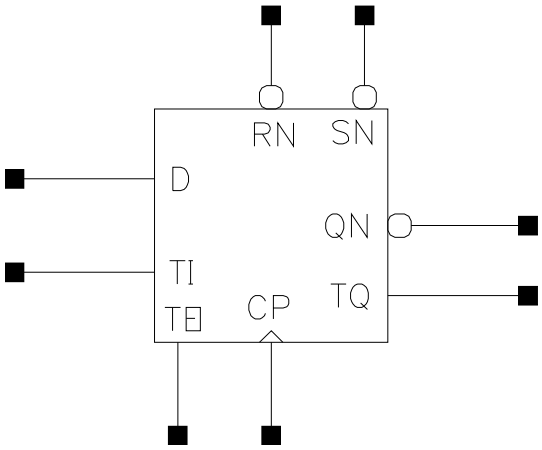
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.370e-03	3.384e-03	3.388e-03	3.390e-03
Clock 100Mhz Data 25Mhz	5.251e-03	5.183e-03	5.797e-03	6.337e-03
Clock 100Mhz Data 50Mhz	7.131e-03	6.982e-03	8.205e-03	9.283e-03
Clock = 0 Data 100Mhz	3.974e-03	3.673e-03	3.573e-03	3.523e-03
Clock = 1 Data 100Mhz	1.091e-03	5.695e-04	3.957e-04	3.088e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.352	5.2224
X17_P0	1.200	4.488	5.3856
X33_P0	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0005	0.0005	0.0005
RN	0.0007	0.0007	0.0007

SN	0.0012	0.0012	0.0012
TE	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to QN ↓	0.0921	0.0972	2.1949	1.1376
CP to QN ↑	0.0733	0.0762	3.7001	1.8725
CP to TQ ↓	0.0559	0.0558	7.1878	7.1979
CP to TQ ↑	0.0772	0.0772	19.8205	19.8448
RN to QN ↓	0.1026	0.1076	2.1944	1.1379
RN to QN ↑	0.1026	0.1071	3.7115	1.8803
RN to TQ ↓	0.0777	0.0774	7.7565	7.7624
RN to TQ ↑	0.0880	0.0880	19.8056	19.8032
SN to QN ↓	0.1101	0.1164	2.2066	1.1419
SN to TQ ↑	0.0933	0.0931	20.0150	20.0194
	X33_P0		**X33_P0**	
CP to QN ↓	0.1101		0.6088	
CP to QN ↑	0.0838		0.9590	
CP to TQ ↓	0.0559		7.2081	
CP to TQ ↑	0.0774		19.8518	
RN to QN ↓	0.1203		0.6086	
RN to QN ↑	0.1176		0.9620	
RN to TQ ↓	0.0774		7.7717	
RN to TQ ↑	0.0883		19.8319	
SN to QN ↓	0.1310		0.6098	
SN to TQ ↑	0.0933		20.0912	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1494	0.1494	0.1494
CP ↑	min_pulse_width to CP	0.0407	0.0444	0.0455
D ↓	hold_rising to CP	-0.0290	-0.0290	-0.0290
D ↑	hold_rising to CP	-0.0117	-0.0117	-0.0117
D ↓	setup_rising to CP	0.0950	0.0950	0.0950
D ↑	setup_rising to CP	0.0488	0.0488	0.0488
RN ↓	min_pulse_width to RN	0.0969	0.0969	0.1067
RN ↑	non_seq_hold_rising to SN	-0.0380	-0.0381	-0.0381
RN ↑	non_seq_setup_rising to SN	0.0888	0.0888	0.0888
RN ↑	recovery_rising to CP	0.0390	0.0390	0.0390
RN ↑	removal_rising to CP	-0.0246	-0.0246	-0.0246
SN ↓	min_pulse_width to SN	0.0815	0.0815	0.0869
SN ↑	recovery_rising to CP	0.0125	0.0125	0.0125
SN ↑	removal_rising to CP	0.0387	0.0387	0.0387

TE ↓	hold_rising to CP	-0.0293	-0.0293	-0.0293
TE ↑	hold_rising to CP	-0.0361	-0.0361	-0.0361
TE ↓	setup_rising to CP	0.0930	0.0930	0.0930
TE ↑	setup_rising to CP	0.1856	0.1856	0.1856
TI ↓	hold_rising to CP	-0.1005	-0.1005	-0.1005
TI ↑	hold_rising to CP	-0.0387	-0.0387	-0.0387
TI ↓	setup_rising to CP	0.1785	0.1785	0.1785
TI ↑	setup_rising to CP	0.0782	0.0782	0.0782

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	3.396e-05	4.169e-09
X17_P0	3.873e-05	4.288e-09
X33_P0	4.716e-05	4.527e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

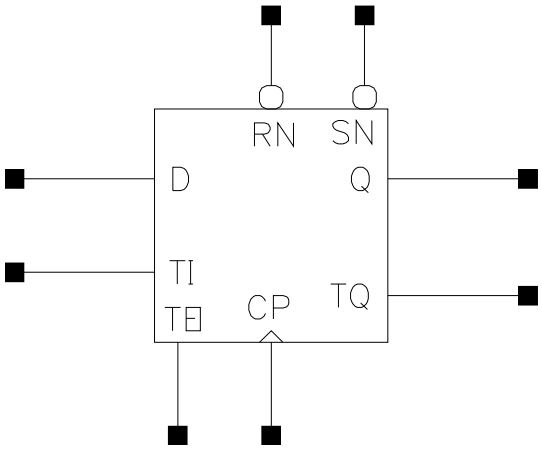
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.593e-03	3.593e-03	3.594e-03
Clock 100Mhz Data 25Mhz	5.467e-03	5.707e-03	6.334e-03
Clock 100Mhz Data 50Mhz	7.342e-03	7.821e-03	9.074e-03
Clock = 0 Data 100Mhz	3.514e-03	3.514e-03	3.514e-03
Clock = 1 Data 100Mhz	4.806e-05	4.813e-05	4.824e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	1.200	4.216	5.0592
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008
D	0.0005	0.0005	0.0005
RN	0.0007	0.0007	0.0007

SN	0.0012	0.0012	0.0012
TE	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X17_P0**	**X8_P0**	**X17_P0**
CP to Q ↓	0.0607	0.0674	2.2982	1.2010
CP to Q ↑	0.0737	0.0768	3.7895	1.9294
CP to TQ ↓	0.0634	0.0721	7.3033	7.3911
CP to TQ ↑	0.0824	0.0901	19.6314	19.7454
RN to Q ↓	0.0880	0.1008	2.6322	1.3791
RN to Q ↑	0.0676	0.0749	3.9365	2.0121
RN to TQ ↓	0.0903	0.1049	7.9665	8.1576
RN to TQ ↑	0.0819	0.0966	19.8206	19.9546
SN to Q ↑	0.0908	0.0980	3.9376	2.0133
SN to TQ ↑	0.1051	0.1196	19.8173	19.9560
	X33_P0		**X33_P0**	
CP to Q ↓	0.0849		0.6509	
CP to Q ↑	0.0863		1.0009	
CP to TQ ↓	0.0877		7.6562	
CP to TQ ↑	0.1047		19.9411	
RN to Q ↓	0.1329		0.7617	
RN to Q ↑	0.0946		1.0547	
RN to TQ ↓	0.1311		8.6614	
RN to TQ ↑	0.1255		20.1809	
SN to Q ↑	0.1175		1.0548	
SN to TQ ↑	0.1483		20.1858	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1494	0.1494	0.1495
CP ↑	min_pulse_width to CP	0.0455	0.0540	0.0734
D ↓	hold_rising to CP	-0.0290	-0.0290	-0.0290
D ↑	hold_rising to CP	-0.0117	-0.0117	-0.0117
D ↓	setup_rising to CP	0.0950	0.0950	0.0950
D ↑	setup_rising to CP	0.0488	0.0488	0.0488
RN ↓	min_pulse_width to RN	0.1045	0.1240	0.1604
RN ↑	non_seq_hold_rising to SN	-0.0408	-0.0479	-0.0625
RN ↑	non_seq_setup_rising to SN	0.0839	0.0839	0.1067
RN ↑	recovery_rising to CP	0.0372	0.0372	0.0372
RN ↑	removal_rising to CP	-0.0171	-0.0171	-0.0171
SN ↓	min_pulse_width to SN	0.0864	0.0989	0.1233
SN ↑	recovery_rising to CP	0.0125	0.0125	0.0125
SN ↑	removal_rising to CP	0.0387	0.0387	0.0387

TE ↓	hold_rising to CP	-0.0237	-0.0237	-0.0237
TE ↑	hold_rising to CP	-0.0361	-0.0361	-0.0361
TE ↓	setup_rising to CP	0.0930	0.0930	0.0930
TE ↑	setup_rising to CP	0.1856	0.1856	0.1856
TI ↓	hold_rising to CP	-0.0966	-0.0951	-0.0951
TI ↑	hold_rising to CP	-0.0387	-0.0387	-0.0372
TI ↓	setup_rising to CP	0.1785	0.1785	0.1785
TI ↑	setup_rising to CP	0.0782	0.0823	0.0838

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	3.292e-05	4.046e-09
X17_P0	3.721e-05	4.165e-09
X33_P0	4.504e-05	4.403e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

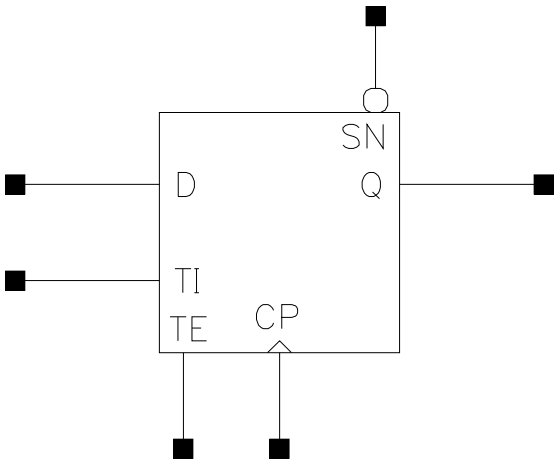
Pin Cycle	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.587e-03	3.588e-03	3.588e-03
Clock 100Mhz Data 25Mhz	5.388e-03	5.682e-03	6.468e-03
Clock 100Mhz Data 50Mhz	7.188e-03	7.776e-03	9.348e-03
Clock = 0 Data 100Mhz	3.513e-03	3.513e-03	3.514e-03
Clock = 1 Data 100Mhz	4.803e-05	4.807e-05	4.820e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004
SN	0.0012	0.0013	0.0013	0.0013
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0008			
D	0.0004			
SN	0.0013			
TE	0.0009			
TI	0.0004			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.1022	0.0533	5.3588	2.2837
CP to Q ↑	0.0825	0.0677	8.0193	3.7665
SN to Q ↑	0.0624	0.0709	7.8077	3.7776
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
CP to Q ↓	0.0752	0.0788	1.1080	0.7695
CP to Q ↑	0.0958	0.0985	1.8570	1.2596
SN to Q ↑	0.0989	0.1016	1.8568	1.2601
	X33_P0		**X33_P0**	
CP to Q ↓	0.0813		0.5866	
CP to Q ↑	0.1002		0.9473	
SN to Q ↑	0.1033		0.9469	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.1505	0.1518	0.1518	0.1518
CP ↑	min_pulse_width to CP	0.0879	0.0396	0.0359	0.0359
D ↓	hold_rising to CP	-0.0867	-0.0339	-0.0339	-0.0339
D ↑	hold_rising to CP	-0.0405	-0.0065	-0.0065	-0.0065
D ↓	setup_rising to CP	0.1463	0.0980	0.0980	0.0980
D ↑	setup_rising to CP	0.0752	0.0391	0.0391	0.0391
SN ↓	min_pulse_width to SN	0.0566	0.0664	0.0637	0.0615
SN ↑	recovery_rising to CP	0.0155	0.0124	0.0124	0.0124
SN ↑	removal_rising to CP	0.0290	0.0388	0.0388	0.0388
TE ↓	hold_rising to CP	-0.0619	-0.0311	-0.0342	-0.0342
TE ↑	hold_rising to CP	-0.0552	-0.0334	-0.0334	-0.0334
TE ↓	setup_rising to CP	0.1247	0.0926	0.0926	0.0926
TE ↑	setup_rising to CP	0.2375	0.1883	0.1883	0.1883
TI ↓	hold_rising to CP	-0.1758	-0.1049	-0.1062	-0.1062
TI ↑	hold_rising to CP	-0.0609	-0.0339	-0.0339	-0.0339
TI ↓	setup_rising to CP	0.2439	0.1841	0.1841	0.1841
TI ↑	setup_rising to CP	0.0990	0.0686	0.0686	0.0686
		X33_P0			

CP ↓	min_pulse_width to CP	0.1518			
CP ↑	min_pulse_width to CP	0.0359			
D ↓	hold_rising to CP	-0.0339			
D ↑	hold_rising to CP	-0.0065			
D ↓	setup_rising to CP	0.0980			
D ↑	setup_rising to CP	0.0391			
SN ↓	min_pulse_width to SN	0.0615			
SN ↑	recovery_rising to CP	0.0124			
SN ↑	removal_rising to CP	0.0388			
TE ↓	hold_rising to CP	-0.0342			
TE ↑	hold_rising to CP	-0.0334			
TE ↓	setup_rising to CP	0.0926			
TE ↑	setup_rising to CP	0.1883			
TI ↓	hold_rising to CP	-0.1062			
TI ↑	hold_rising to CP	-0.0339			
TI ↓	setup_rising to CP	0.1841			
TI ↑	setup_rising to CP	0.0686			

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.674e-05	3.799e-09
X8_P0	2.972e-05	3.680e-09
X17_P0	3.860e-05	3.918e-09
X25_P0	4.288e-05	4.038e-09
X33_P0	4.711e-05	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	3.272e-03	3.349e-03	3.374e-03	3.387e-03
Clock 100Mhz Data 25Mhz	5.013e-03	5.080e-03	5.644e-03	5.927e-03
Clock 100Mhz Data 50Mhz	6.754e-03	6.811e-03	7.913e-03	8.468e-03
Clock = 0 Data 100Mhz	3.835e-03	3.615e-03	3.543e-03	3.507e-03
Clock = 1 Data 100Mhz	1.091e-03	5.694e-04	3.956e-04	3.087e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	3.394e-03			

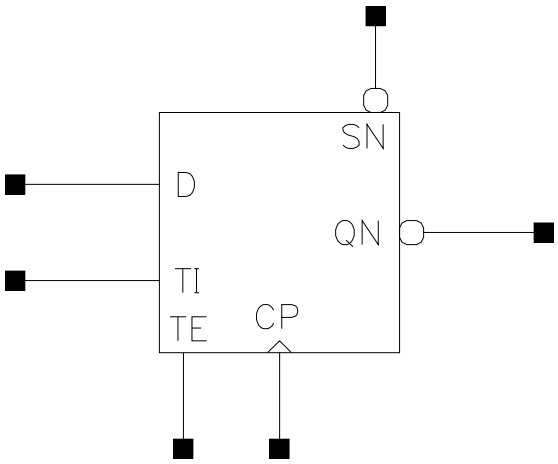
Clock 100Mhz Data 25Mhz	6.151e-03			
Clock 100Mhz Data 50Mhz	8.908e-03			
Clock = 0 Data 100Mhz	3.486e-03			
Clock = 1 Data 100Mhz	2.565e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	3.944	4.7328
X8_P0	1.200	3.808	4.5696
X17_P0	1.200	4.080	4.8960
X25_P0	1.200	4.216	5.0592
X33_P0	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X25_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004
SN	0.0013	0.0013	0.0013	0.0013
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004
	X33_P0			

CP	0.0008			
D	0.0004			
SN	0.0013			
TE	0.0009			
TI	0.0004			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
CP to QN ↓	0.0933	0.0809	4.1972	2.1541
CP to QN ↑	0.1065	0.0614	7.7095	3.6863
SN to QN ↓	0.0747	0.0839	4.1800	2.1540
	X17_P0	X25_P0	X17_P0	X25_P0
CP to QN ↓	0.0841	0.0884	1.1117	0.7716
CP to QN ↑	0.0726	0.0765	1.8604	1.2623
SN to QN ↓	0.0884	0.0929	1.1122	0.7723
	X33_P0		X33_P0	
CP to QN ↓	0.0918		0.5884	
CP to QN ↑	0.0791		0.9493	
SN to QN ↓	0.0963		0.5875	

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X25_P0
CP ↓	min_pulse_width to CP	0.1505	0.1518	0.1518	0.1518
CP ↑	min_pulse_width to CP	0.0674	0.0359	0.0444	0.0444
D ↓	hold_rising to CP	-0.0867	-0.0335	-0.0339	-0.0339
D ↑	hold_rising to CP	-0.0405	-0.0065	-0.0065	-0.0065
D ↓	setup_rising to CP	0.1463	0.0980	0.0980	0.0980
D ↑	setup_rising to CP	0.0752	0.0391	0.0391	0.0391
SN ↓	min_pulse_width to SN	0.0566	0.0615	0.0691	0.0691
SN ↑	recovery_rising to CP	0.0155	0.0124	0.0124	0.0124
SN ↑	removal_rising to CP	0.0290	0.0388	0.0388	0.0388
TE ↓	hold_rising to CP	-0.0619	-0.0342	-0.0286	-0.0286
TE ↑	hold_rising to CP	-0.0552	-0.0334	-0.0335	-0.0335
TE ↓	setup_rising to CP	0.1247	0.0926	0.0926	0.0926
TE ↑	setup_rising to CP	0.2375	0.1883	0.1880	0.1880
TI ↓	hold_rising to CP	-0.1758	-0.1103	-0.1049	-0.1049
TI ↑	hold_rising to CP	-0.0609	-0.0339	-0.0339	-0.0339
TI ↓	setup_rising to CP	0.2439	0.1841	0.1841	0.1841
TI ↑	setup_rising to CP	0.0990	0.0686	0.0684	0.0684
		X33_P0			

CP ↓	min_pulse_width to CP	0.1518			
CP ↑	min_pulse_width to CP	0.0455			
D ↓	hold_rising to CP	-0.0339			
D ↑	hold_rising to CP	-0.0065			
D ↓	setup_rising to CP	0.0980			
D ↑	setup_rising to CP	0.0391			
SN ↓	min_pulse_width to SN	0.0691			
SN ↑	recovery_rising to CP	0.0124			
SN ↑	removal_rising to CP	0.0388			
TE ↓	hold_rising to CP	-0.0286			
TE ↑	hold_rising to CP	-0.0335			
TE ↓	setup_rising to CP	0.0926			
TE ↑	setup_rising to CP	0.1880			
TI ↓	hold_rising to CP	-0.1049			
TI ↑	hold_rising to CP	-0.0339			
TI ↓	setup_rising to CP	0.1841			
TI ↑	setup_rising to CP	0.0684			

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.589e-05	3.799e-09
X8_P0	2.851e-05	3.680e-09
X17_P0	3.774e-05	3.918e-09
X25_P0	4.145e-05	4.038e-09
X33_P0	4.520e-05	4.157e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X4_P0	X8_P0	X17_P0	X25_P0
Clock 100Mhz Data 0Mhz	3.273e-03	3.355e-03	3.378e-03	3.390e-03
Clock 100Mhz Data 25Mhz	4.926e-03	5.050e-03	5.644e-03	5.931e-03
Clock 100Mhz Data 50Mhz	6.579e-03	6.746e-03	7.910e-03	8.472e-03
Clock = 0 Data 100Mhz	3.835e-03	3.619e-03	3.545e-03	3.509e-03
Clock = 1 Data 100Mhz	1.091e-03	5.693e-04	3.955e-04	3.086e-04
	X33_P0			
Clock 100Mhz Data 0Mhz	3.397e-03			

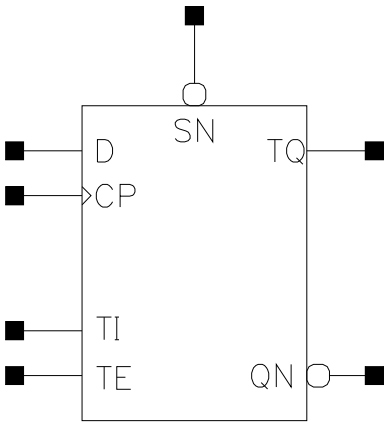
Clock 100Mhz Data 25Mhz	6.172e-03			
Clock 100Mhz Data 50Mhz	8.946e-03			
Clock = 0 Data 100Mhz	3.487e-03			
Clock = 1 Data 100Mhz	2.565e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.216	5.0592
X8_P0	1.200	4.080	4.8960
X17_P0	1.200	4.352	5.2224
X33_P0	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004

SN	0.0014	0.0015	0.0014	0.0014
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to QN ↓	0.1075	0.0850	4.1928	2.1639
CP to QN ↑	0.1381	0.0697	7.6182	3.7574
CP to TQ ↓	0.0993	0.0481	6.4120	5.2335
CP to TQ ↑	0.0828	0.0646	10.8068	10.5317
SN to QN ↓	0.0705	0.0726	4.1814	2.1596
SN to TQ ↑	0.0493	0.0512	10.6083	10.5601
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to QN ↓	0.0842	0.0921	1.1389	0.5820
CP to QN ↑	0.0777	0.0849	1.8735	0.9539
CP to TQ ↓	0.0597	0.0594	5.4467	5.4480
CP to TQ ↑	0.0722	0.0722	10.5792	10.6023
SN to QN ↓	0.0728	0.0807	1.1381	0.5808
SN to TQ ↑	0.0603	0.0602	10.5826	10.6028

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1505	0.1518	0.1524	0.1524
CP ↑	min_pulse_width to CP	0.0927	0.0396	0.0455	0.0492
D ↓	hold_rising to CP	-0.0867	-0.0339	-0.0339	-0.0339
D ↑	hold_rising to CP	-0.0405	-0.0065	-0.0065	-0.0065
D ↓	setup_rising to CP	0.1463	0.0980	0.0980	0.0980
D ↑	setup_rising to CP	0.0752	0.0391	0.0391	0.0391
SN ↓	min_pulse_width to SN	0.0496	0.0518	0.0544	0.0544
SN ↑	recovery_rising to CP	0.0155	0.0124	0.0124	0.0124
SN ↑	removal_rising to CP	0.0290	0.0388	0.0388	0.0388
TE ↓	hold_rising to CP	-0.0619	-0.0342	-0.0286	-0.0286
TE ↑	hold_rising to CP	-0.0552	-0.0334	-0.0309	-0.0309
TE ↓	setup_rising to CP	0.1247	0.0926	0.0926	0.0926
TE ↑	setup_rising to CP	0.2372	0.1883	0.1880	0.1880
TI ↓	hold_rising to CP	-0.1758	-0.1062	-0.1049	-0.1049
TI ↑	hold_rising to CP	-0.0609	-0.0339	-0.0339	-0.0339
TI ↓	setup_rising to CP	0.2439	0.1841	0.1841	0.1841
TI ↑	setup_rising to CP	0.0990	0.0686	0.0686	0.0686

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.929e-05	4.038e-09
X8_P0	3.188e-05	3.918e-09
X17_P0	4.112e-05	4.157e-09
X33_P0	4.859e-05	4.395e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

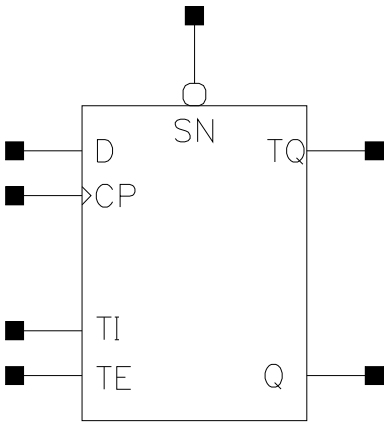
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.277e-03	3.354e-03	3.380e-03	3.393e-03
Clock 100Mhz Data 25Mhz	5.192e-03	5.236e-03	5.767e-03	6.300e-03
Clock 100Mhz Data 50Mhz	7.107e-03	7.118e-03	8.154e-03	9.208e-03
Clock = 0 Data 100Mhz	3.844e-03	3.625e-03	3.552e-03	3.515e-03
Clock = 1 Data 100Mhz	1.092e-03	5.696e-04	3.957e-04	3.087e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	4.080	4.8960
X8_P0	1.200	3.944	4.7328
X17_P0	1.200	4.216	5.0592
X33_P0	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X33_P0
CP	0.0008	0.0008	0.0008	0.0008
D	0.0007	0.0004	0.0004	0.0004

SN	0.0014	0.0013	0.0013	0.0012
TE	0.0008	0.0009	0.0009	0.0009
TI	0.0005	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
CP to Q ↓	0.1165	0.0570	5.5236	2.3339
CP to Q ↑	0.0877	0.0699	8.0605	3.8163
CP to TQ ↓	0.1168	0.0605	8.0800	6.0704
CP to TQ ↑	0.0867	0.0782	10.8905	15.4456
SN to Q ↑	0.0520	0.0735	7.8320	3.8230
SN to TQ ↑	0.0511	0.0831	10.6430	15.4268
	X17_P0	**X33_P0**	**X17_P0**	**X33_P0**
CP to Q ↓	0.0765	0.0831	1.1359	0.5974
CP to Q ↑	0.0967	0.1015	1.8664	0.9499
CP to TQ ↓	0.0797	0.0887	5.7083	5.7973
CP to TQ ↑	0.1030	0.1111	14.8734	14.9405
SN to Q ↑	0.0998	0.1045	1.8665	0.9512
SN to TQ ↑	0.1061	0.1140	14.8701	14.9408

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X4_P0	X8_P0	X17_P0	X33_P0
CP ↓	min_pulse_width to CP	0.1505	0.1518	0.1518	0.1518
CP ↑	min_pulse_width to CP	0.1024	0.0444	0.0359	0.0359
D ↓	hold_rising to CP	-0.0867	-0.0339	-0.0339	-0.0339
D ↑	hold_rising to CP	-0.0405	-0.0065	-0.0065	-0.0065
D ↓	setup_rising to CP	0.1463	0.0980	0.0980	0.0980
D ↑	setup_rising to CP	0.0752	0.0391	0.0391	0.0391
SN ↓	min_pulse_width to SN	0.0469	0.0713	0.0615	0.0615
SN ↑	recovery_rising to CP	0.0124	0.0124	0.0124	0.0124
SN ↑	removal_rising to CP	0.0290	0.0388	0.0388	0.0388
TE ↓	hold_rising to CP	-0.0619	-0.0286	-0.0342	-0.0342
TE ↑	hold_rising to CP	-0.0552	-0.0335	-0.0334	-0.0334
TE ↓	setup_rising to CP	0.1221	0.0926	0.0926	0.0926
TE ↑	setup_rising to CP	0.2375	0.1883	0.1883	0.1883
TI ↓	hold_rising to CP	-0.1758	-0.1049	-0.1062	-0.1062
TI ↑	hold_rising to CP	-0.0604	-0.0339	-0.0339	-0.0339
TI ↓	setup_rising to CP	0.2398	0.1841	0.1841	0.1841
TI ↑	setup_rising to CP	0.0990	0.0684	0.0686	0.0686

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	2.918e-05	3.918e-09
X8_P0	3.132e-05	3.799e-09
X17_P0	4.021e-05	4.037e-09
X33_P0	4.871e-05	4.276e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

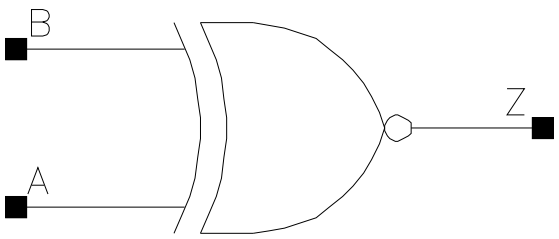
Pin Cycle	X4_P0	X8_P0	X17_P0	X33_P0
Clock 100Mhz Data 0Mhz	3.273e-03	3.349e-03	3.374e-03	3.387e-03
Clock 100Mhz Data 25Mhz	5.177e-03	5.219e-03	5.776e-03	6.332e-03
Clock 100Mhz Data 50Mhz	7.081e-03	7.089e-03	8.177e-03	9.277e-03
Clock = 0 Data 100Mhz	3.846e-03	3.622e-03	3.548e-03	3.510e-03
Clock = 1 Data 100Mhz	1.091e-03	5.696e-04	3.957e-04	3.088e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.360	1.6320
X17_P0	1.200	1.496	1.7952
X25_P0	1.200	2.312	2.7744
X33_P0	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P0	X8_P0	X17_P0	X25_P0
A	0.0014	0.0006	0.0008	0.0013
B	0.0013	0.0013	0.0016	0.0022
	X33_P0			
A	0.0014			
B	0.0025			

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P0	**X8_P0**	**X6_P0**	**X8_P0**
A to Z ↓	0.0245	0.0569	4.2719	2.3498
A to Z ↑	0.0268	0.0505	6.2009	3.8944
B to Z ↓	0.0233	0.0391	4.2650	2.3302
B to Z ↑	0.0264	0.0366	6.2113	3.8841
	X17_P0	**X25_P0**	**X17_P0**	**X25_P0**
A to Z ↓	0.0534	0.0534	1.1587	0.7987
A to Z ↑	0.0457	0.0460	1.9052	1.2688

B to Z ↓	0.0400	0.0389	1.1549	0.7968
B to Z ↑	0.0358	0.0347	1.9030	1.2675
	X33_P0		**X33_P0**	
A to Z ↓	0.0503		0.6003	
A to Z ↑	0.0442		0.9540	
B to Z ↓	0.0374		0.5990	
B to Z ↑	0.0341		0.9512	

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X6_P0	1.286e-05	1.179e-09
X8_P0	1.852e-05	1.536e-09
X17_P0	2.852e-05	1.655e-09
X25_P0	4.540e-05	2.370e-09
X33_P0	5.892e-05	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	2.041e-03	3.817e-03	5.368e-03	8.534e-03
B to Z	1.982e-03	2.610e-03	4.005e-03	6.223e-03
	X33_P0			
A to Z	1.037e-02			
B to Z	7.814e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

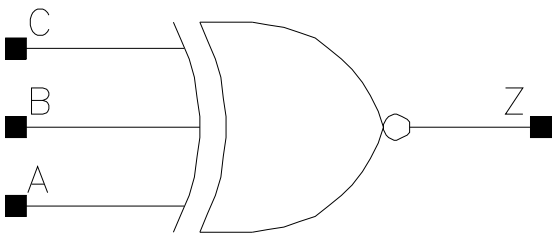
Pin Cycle (vdds)	X6_P0	X8_P0	X17_P0	X25_P0
A to Z	1.154e-07	-1.577e-07	4.624e-08	-2.221e-07
B to Z	1.259e-07	-1.595e-07	7.465e-08	9.100e-08
	X33_P0			
A to Z	-1.524e-07			
B to Z	2.223e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	2.176	2.6112
X16_P0	1.200	2.720	3.2640
X25_P0	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X16_P0	X25_P0
A	0.0024	0.0021	0.0025	0.0037
B	0.0028	0.0019	0.0026	0.0035
C	0.0017	0.0006	0.0006	0.0007

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0400	0.0680	5.1219	2.4935
A to Z ↑	0.0387	0.0620	9.2575	3.8628
B to Z ↓	0.0406	0.0676	5.1238	2.4922
B to Z ↑	0.0385	0.0619	9.2501	3.8620
C to Z ↓	0.0394	0.0875	5.1260	2.4920
C to Z ↑	0.0368	0.0813	9.2520	3.8597
	X16_P0	**X25_P0**	**X16_P0**	**X25_P0**
A to Z ↓	0.0678	0.0673	1.2808	0.8195
A to Z ↑	0.0661	0.0655	2.0231	1.2733
B to Z ↓	0.0678	0.0683	1.2808	0.8199

B to Z ↑	0.0661	0.0668	2.0243	1.2748
C to Z ↓	0.0914	0.0965	1.2806	0.8195
C to Z ↑	0.0887	0.0946	2.0246	1.2746

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	1.308e-05	2.132e-09
X8_P0	1.527e-05	2.251e-09
X16_P0	2.488e-05	2.727e-09
X25_P0	3.507e-05	3.799e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	2.175e-03	2.956e-03	4.788e-03	7.194e-03
B to Z	2.162e-03	2.917e-03	4.766e-03	7.222e-03
C to Z	2.095e-03	4.417e-03	6.542e-03	9.848e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

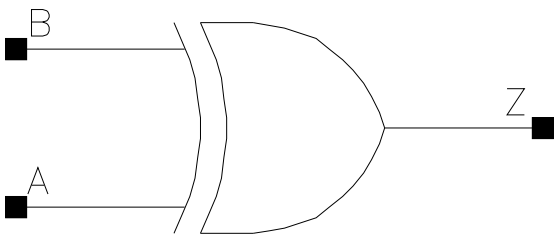
Pin Cycle (vdds)	X4_P0	X8_P0	X16_P0	X25_P0
A to Z	5.449e-07	1.445e-07	2.788e-07	4.289e-07
B to Z	1.020e-05	4.008e-06	4.781e-06	7.824e-06
C to Z	2.012e-05	9.694e-06	1.162e-05	1.677e-05

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	1.224	1.4688
X6_P0	1.200	0.952	1.1424
X8_P0	1.200	1.224	1.4688
X16_P0	1.200	1.360	1.6320
X25_P0	1.200	2.176	2.6112
X31_P0	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P0	X6_P0	X8_P0	X16_P0
A	0.0007	0.0013	0.0009	0.0010
B	0.0011	0.0013	0.0013	0.0014
	X25_P0	X31_P0		
A	0.0012	0.0016		
B	0.0023	0.0029		

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X6_P0**	**X4_P0**	**X6_P0**
A to Z ↓	0.0512	0.0259	4.2694	3.2345
A to Z ↑	0.0475	0.0270	7.4926	8.2179
B to Z ↓	0.0366	0.0254	4.2517	3.2531
B to Z ↑	0.0362	0.0257	7.4910	8.2191
	X8_P0	**X16_P0**	**X8_P0**	**X16_P0**
A to Z ↓	0.0451	0.0470	2.2848	1.1849

A to Z ↑	0.0403	0.0421	3.7932	1.9108
B to Z ↓	0.0349	0.0360	2.2784	1.1822
B to Z ↑	0.0327	0.0341	3.7896	1.9111
	X25_P0	**X31_P0**	**X25_P0**	**X31_P0**
A to Z ↓	0.0501	0.0468	0.7912	0.6372
A to Z ↑	0.0446	0.0420	1.2673	1.0209
B to Z ↓	0.0376	0.0351	0.7904	0.6367
B to Z ↑	0.0336	0.0319	1.2670	1.0196

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	1.551e-05	1.417e-09
X6_P0	1.341e-05	1.179e-09
X8_P0	2.264e-05	1.417e-09
X16_P0	3.174e-05	1.536e-09
X25_P0	4.450e-05	2.251e-09
X31_P0	5.823e-05	2.370e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	2.883e-03	2.013e-03	3.429e-03	4.959e-03
B to Z	2.200e-03	1.908e-03	2.812e-03	4.101e-03
	X25_P0	X31_P0		
A to Z	7.768e-03	9.478e-03		
B to Z	5.519e-03	6.708e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

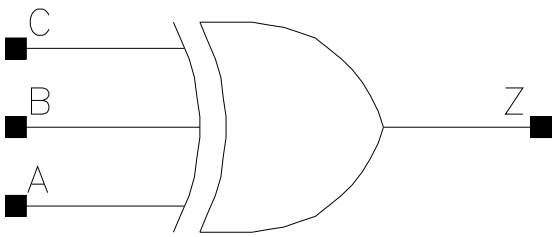
Pin Cycle (vdds)	X4_P0	X6_P0	X8_P0	X16_P0
A to Z	-1.487e-07	7.555e-07	2.956e-08	-7.300e-08
B to Z	-7.165e-08	2.617e-06	1.780e-08	1.735e-07
	X25_P0	X31_P0		
A to Z	-7.800e-08	-1.112e-07		
B to Z	6.185e-08	2.606e-07		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	2.040	2.4480
X8_P0	1.200	1.904	2.2848
X17_P0	1.200	2.040	2.4480
X24_P0	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P0	X8_P0	X17_P0	X24_P0
A	0.0020	0.0021	0.0025	0.0046
B	0.0021	0.0019	0.0024	0.0038
C	0.0007	0.0014	0.0019	0.0029

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0405	0.0679	5.3597	2.4920
A to Z ↑	0.0389	0.0619	10.0735	3.8566
B to Z ↓	0.0410	0.0676	5.3623	2.4917
B to Z ↑	0.0391	0.0619	10.0653	3.8584
C to Z ↓	0.0676	0.0656	5.3461	2.4925
C to Z ↑	0.0658	0.0595	10.0421	3.8570
	X17_P0	**X24_P0**	**X17_P0**	**X24_P0**
A to Z ↓	0.0612	0.0712	1.1887	0.8598
A to Z ↑	0.0598	0.0536	1.8810	1.2774
B to Z ↓	0.0609	0.0711	1.1887	0.8594

B to Z ↑	0.0597	0.0535	1.8817	1.2766
C to Z ↓	0.0596	0.0684	1.1890	0.8584
C to Z ↑	0.0583	0.0523	1.8795	1.2785

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	1.532e-05	2.132e-09
X8_P0	1.253e-05	2.013e-09
X17_P0	2.190e-05	2.132e-09
X24_P0	3.720e-05	3.680e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	2.039e-03	2.957e-03	4.523e-03	7.759e-03
B to Z	2.057e-03	2.917e-03	4.490e-03	7.687e-03
C to Z	4.085e-03	2.831e-03	4.454e-03	7.555e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X4_P0	X8_P0	X17_P0	X24_P0
A to Z	5.247e-07	2.265e-07	3.391e-07	5.092e-07
B to Z	5.037e-06	4.049e-06	5.106e-06	1.152e-05
C to Z	1.413e-05	1.146e-05	1.373e-05	3.506e-05

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