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Seal Ring Crack Detector/Crack Sensor (CS) Application Note

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1. Introduction

The goal of the seal ring Crack Detector also named as Crack Sensor - first developed in M40 technology - is to be able thanks to a ring of two metal lines – on internal and one external – to detect whether the searing has been damaged during sawing, and so if circuit can be exposed to some moisture. It allows to detect cracks and delamination defects in the backend on the die periphery due to the sawing.

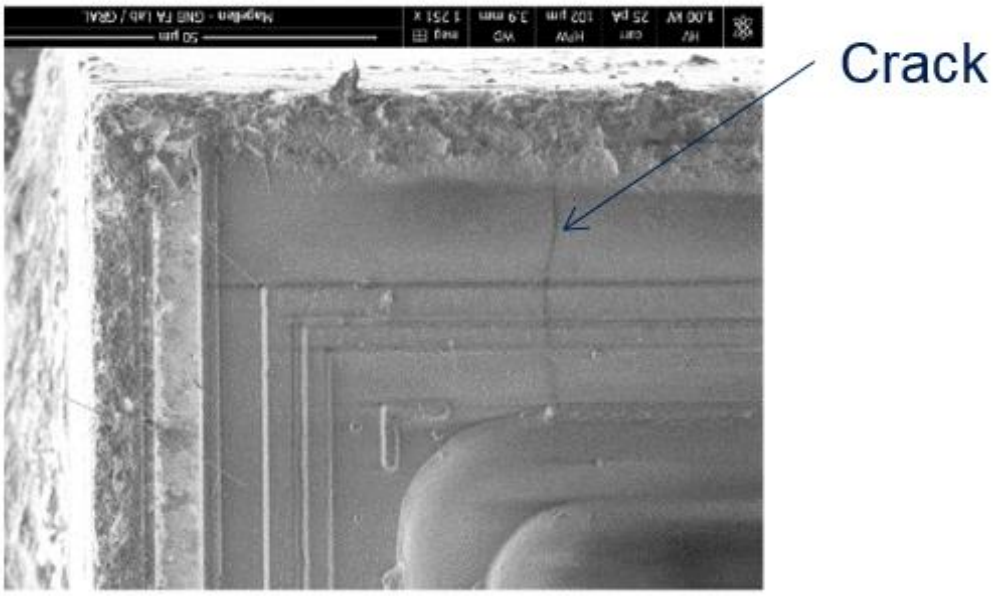


Figure 1: *Top view of a die corner with a crack*

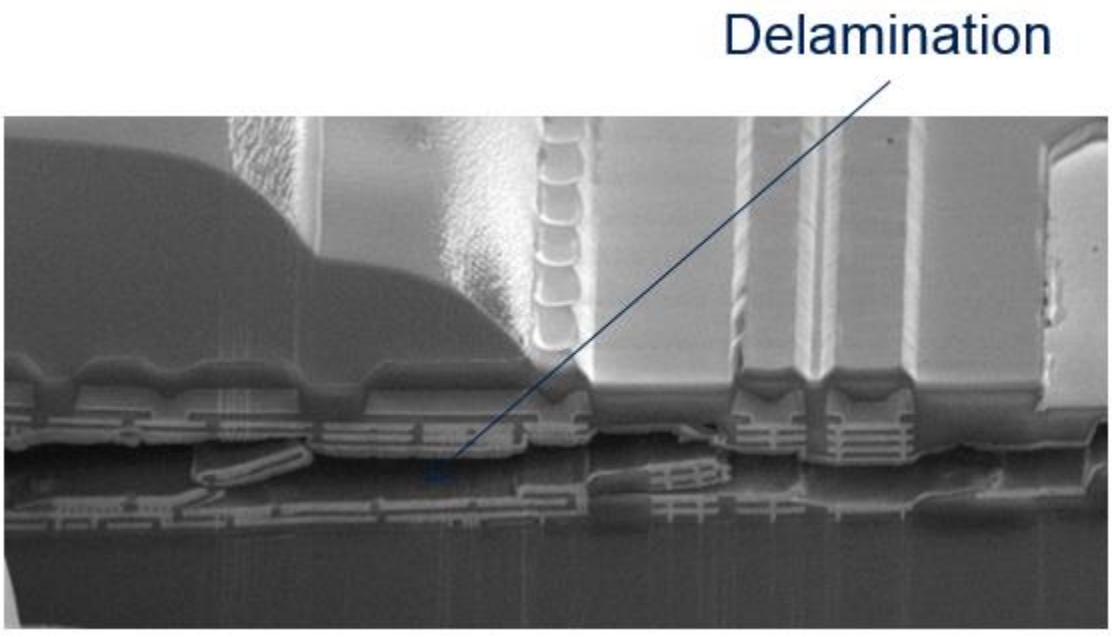


Figure 2: *Cut view of a die zone with backend delamination*

A crack detector is a resistive sensor composed of a metal wire with two electrical nodes. This metal wire is placed around the die close to seal ring. Measuring the continuity of this wire allows to detect cracks.

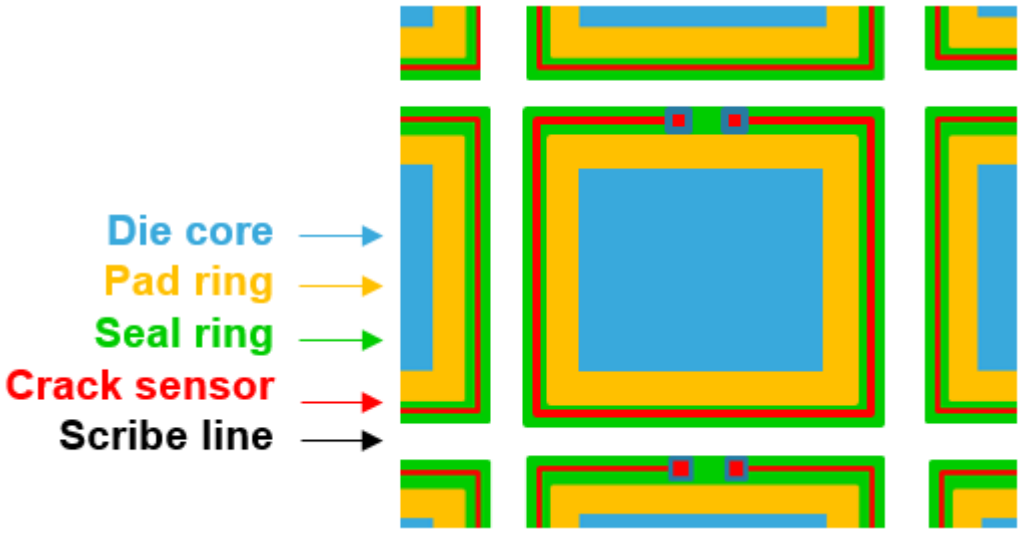


Figure 3: *Schematic view of seal ring Crack Detector implemented on wafer*

The crack detector in 28nm-FDSOI technology is composed of one crack sensor, located at the center of the seal ring.
This sensor is actually a via chain. This permits to detect delamination defects in addition to cracks. Connections to the crack-sensor (in/out terminals) are made through N-well straps to not cut the metal continuity of the seal ring.

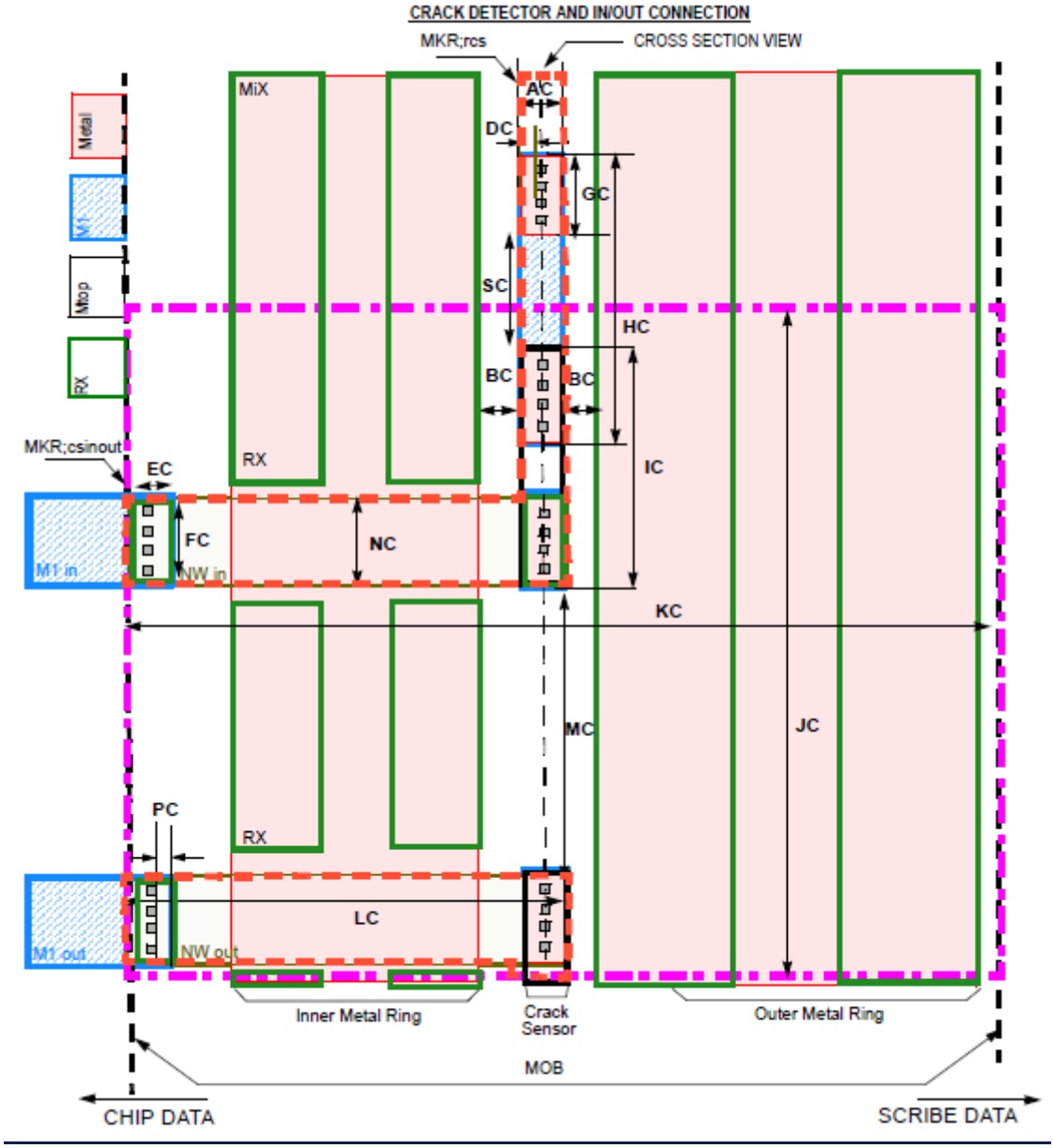


Figure 4: *Schematic view of 28FDSOI seal ring with crack sensors in/out connections*[1]

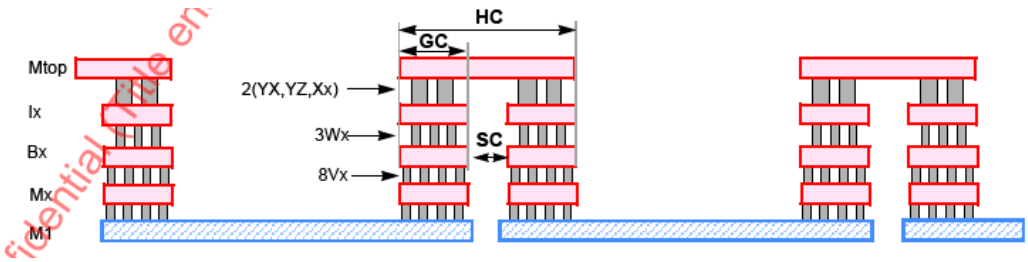


Figure 5: *Crack detector cross section view*

[1] Data extracted from Design Rules Manual (8343474)

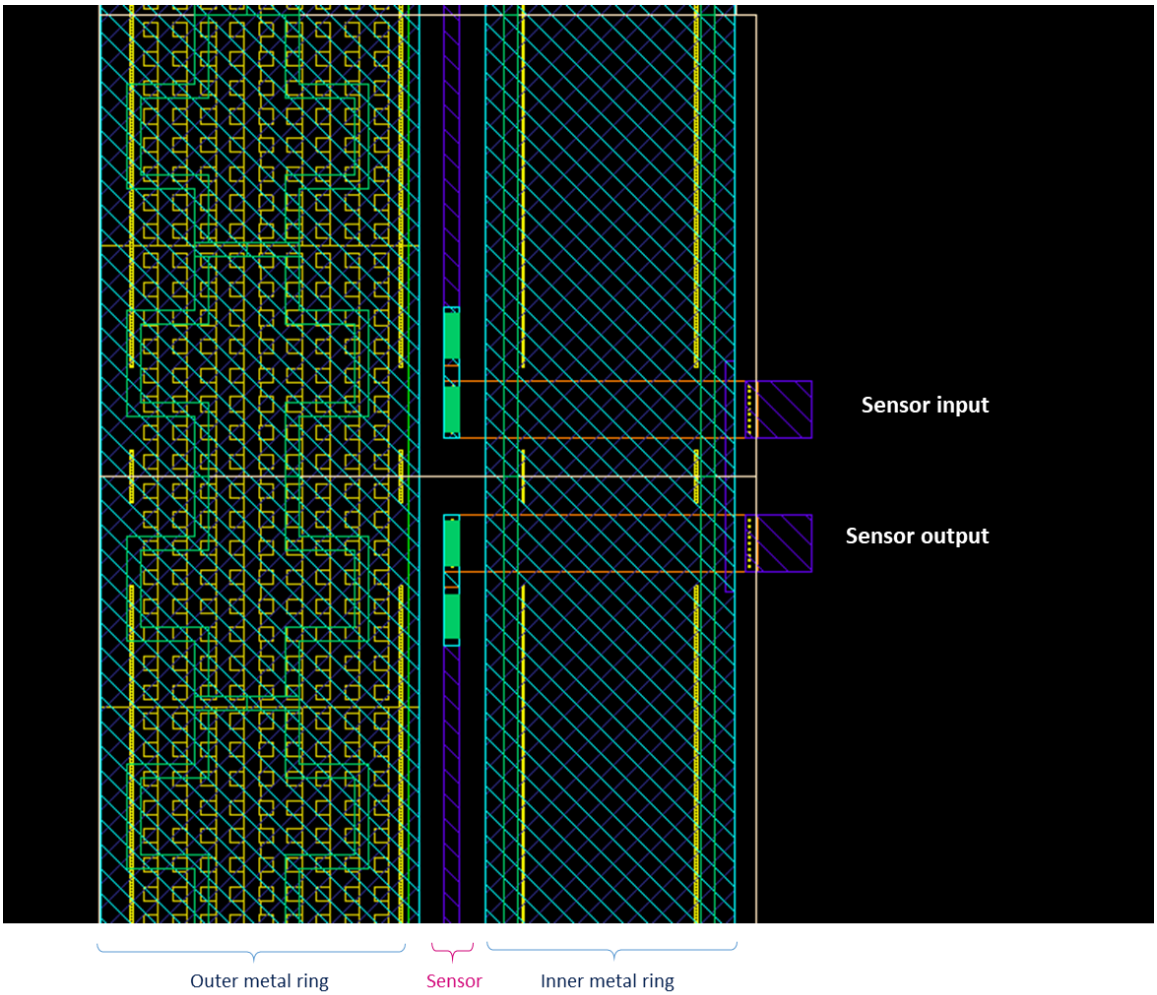


Figure 6: *Top view (layout) of 28FD seal ring with crack sensor nodes.*

2. Design Kit Pcells

The 28nm-FDSOI Process Design Kit includes two different metal stack as per the Design Rule Manual (DRM).
Consequently, the Process Design Kit provides four seal ring Pcells, two of which are implemented with Crack Sensor feature.

These Pcells are named:

- **sealringCS_6U1x_2T8x_LB**
- **sealringCS_6U1x_2U2x_2T8x_LB**

1. Metal Stack: 6U1x_2T8x_LB

a. Seal ring views of sealringCS_6U1x_2T8x_LB

The **sealringCS_6U1x_2T8x_LB** can be found in the Cadence Library Manager under the library ***ST_C32_addon_DP*** and category ***LayoutFinishing***.

Three views are available: **symbol**, **schematic** and **layout**.

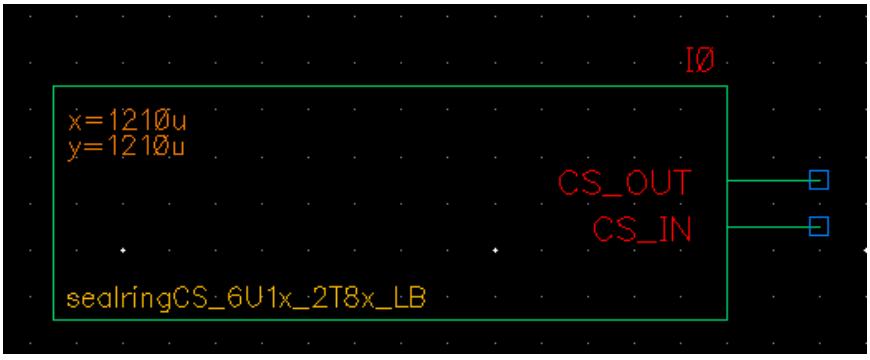


Figure 7: *symbol view of sealringCS_6U1x_2T8x_LB*

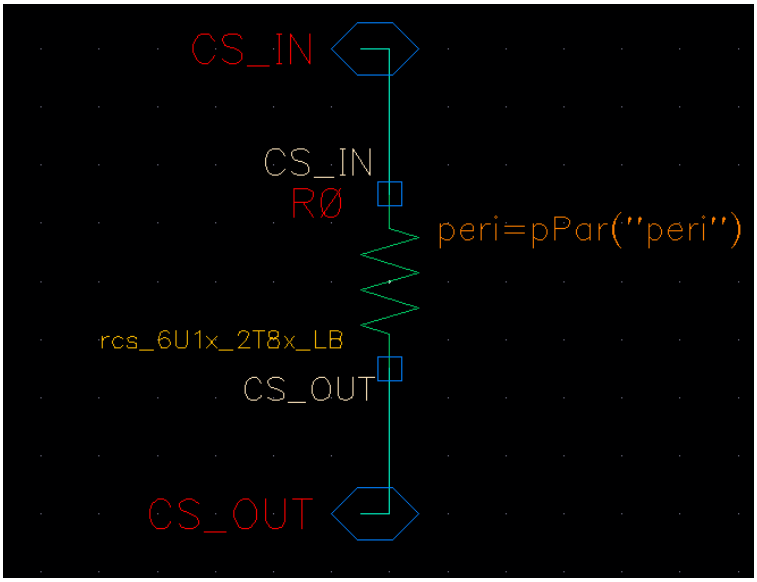


Figure 8: *schematic view of sealringCS_6U1x_2T8x_LB*

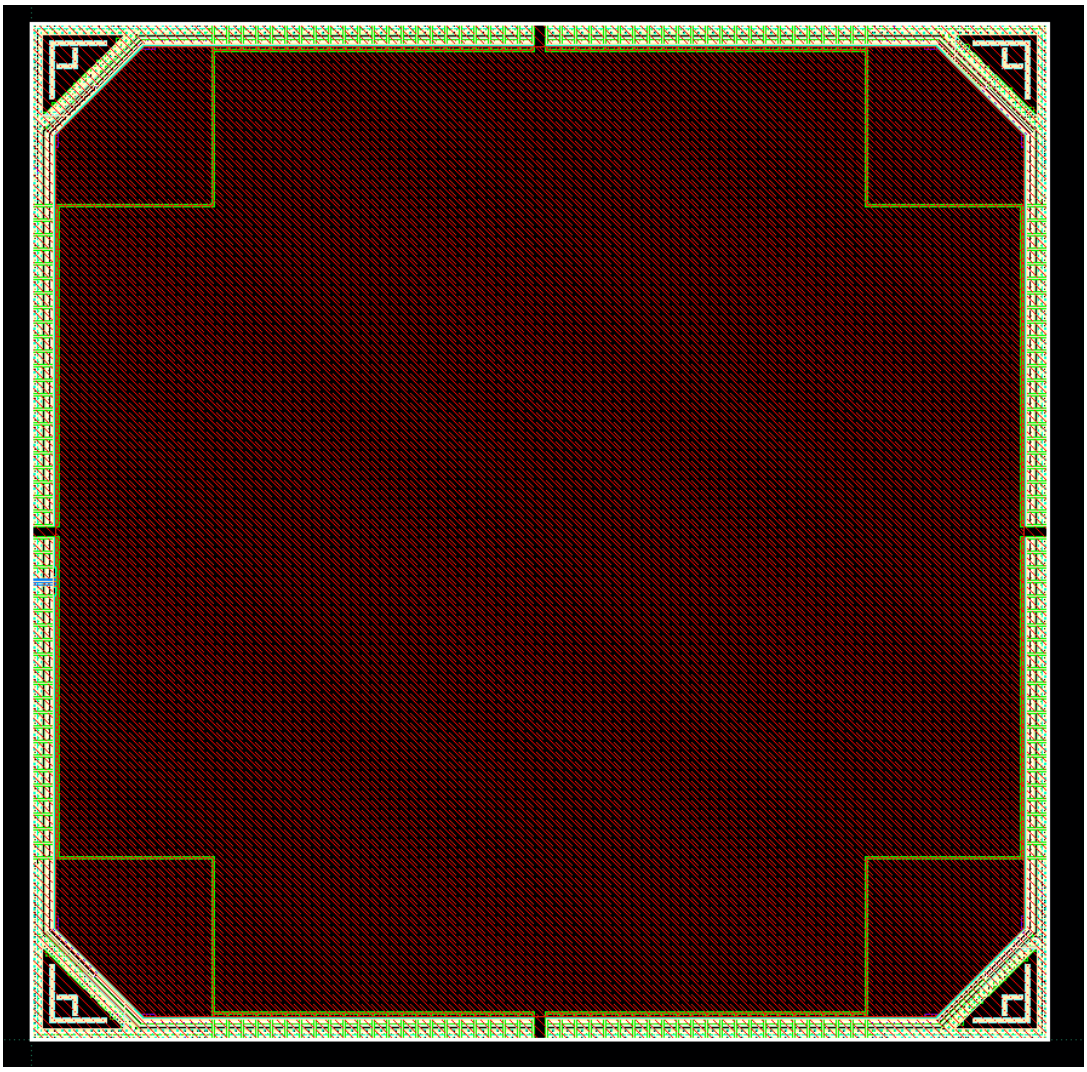


Figure 9: *layout view of sealringCS_6U1x_2T8x_LB with L=W=1000µm*

b. Pcell parameters of sealringCS_6U1x_2T8x_LB

Below are detailed all the parameters of the cell sealringCS_6U1x_2T8x_LB.

Figure 10: *sealringCS_6U1x_2T8x_LB symbol instance parameters*

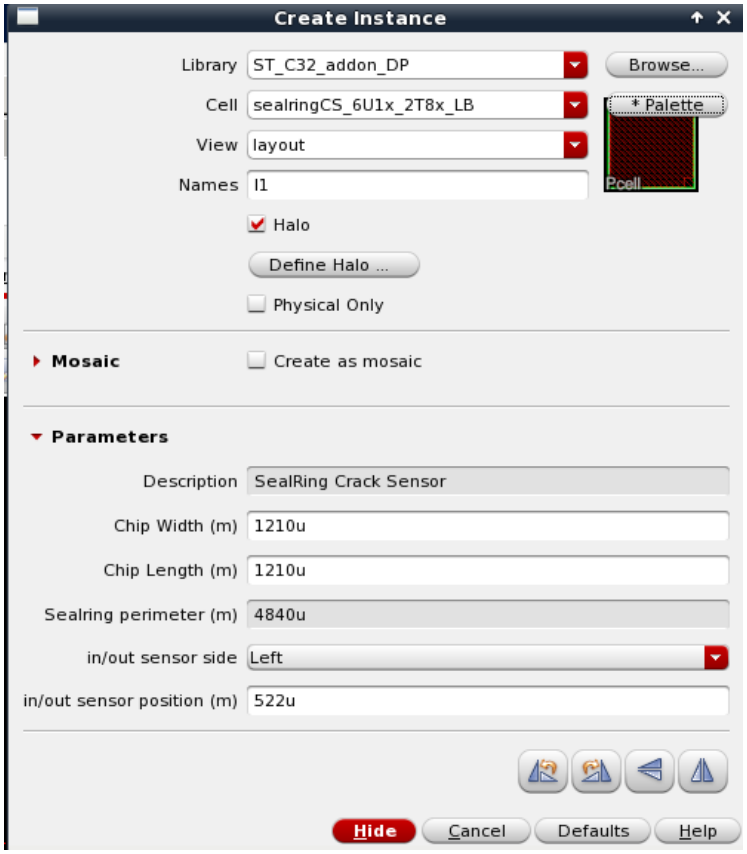


Figure 11: *sealringCS_6U1x_2T8x_LB layout instance parameters*

Chip Width (unit *m*): internal dimensions in meter of the chip in horizontal direction.
A callback corrects the value to be an integer, in order that the external dimensions are integers (DRC rule).
Default value: 1210µm
Min value: 285µm
Max value: unlimited

Chip Length (unit *m*): internal dimension in meter of the chip in vertical direction.
A callback rounds the value to be an integer, in order that the external dimensions are integers too (DRC rule).
Default value: 1210µm
Min value: 285µm
Max value: unlimited

Sealring Perimeter (unit *m*): not editable, only the information is given to the user.

In/out sensor side: multiple choices for the side of the in/out pins connections:
Default value: Left
Value: Left/Right/Top/Bottom

In/out sensor position (unit *m*): position of the pins measured from the external border of the ring (bottom border for Left and Right positions, left border for Top and Bottom positions).
Warning, for the placement of the seal ring around the Chip, please refer to the Design Rules Manual[2].
Default value: 522µm
Min value: 162µm
Max value: defined by Chip Width or Chip Length

[2] Design Rules Manual reference DM00271630.

2. Metal Stack: 6U1x_2U2x_2T8x_LB

a. Seal ring views of sealringCS_6U1x_2U2x_2T8x_LB

The **sealringCS_6U1x_2U2x_2T8x_LB** can be found in the Cadence Library Manager under the library ***ST_C32_addon_DP*** and category ***LayoutFinishing***.

Three views are available: **symbol**, **schematic** and **layout**.

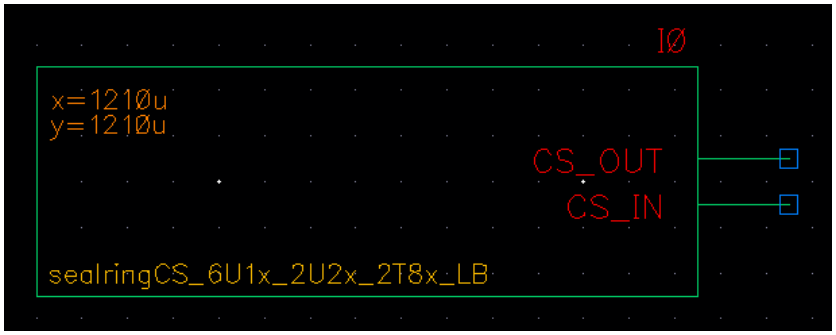


Figure 12: *symbol view of sealringCS_6U1x_2U2x_2T8x_LB*

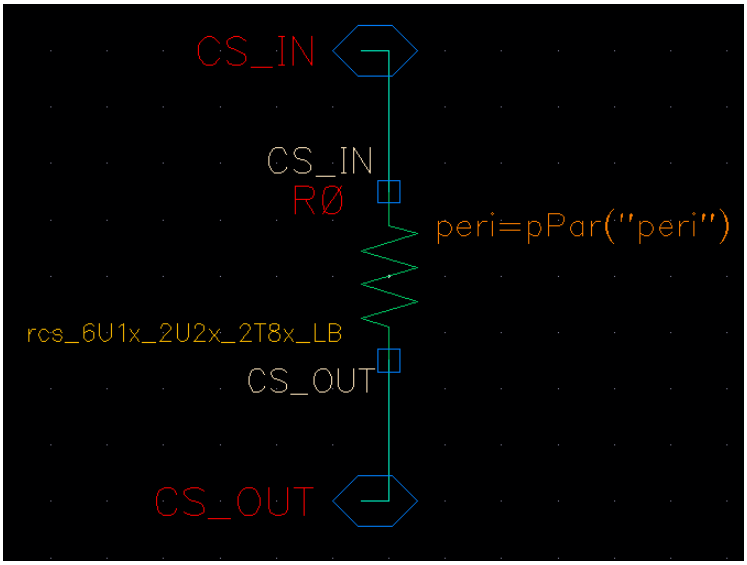


Figure 13: *schematic view of sealringCS_6U1x_2U2x_2T8x_LB*

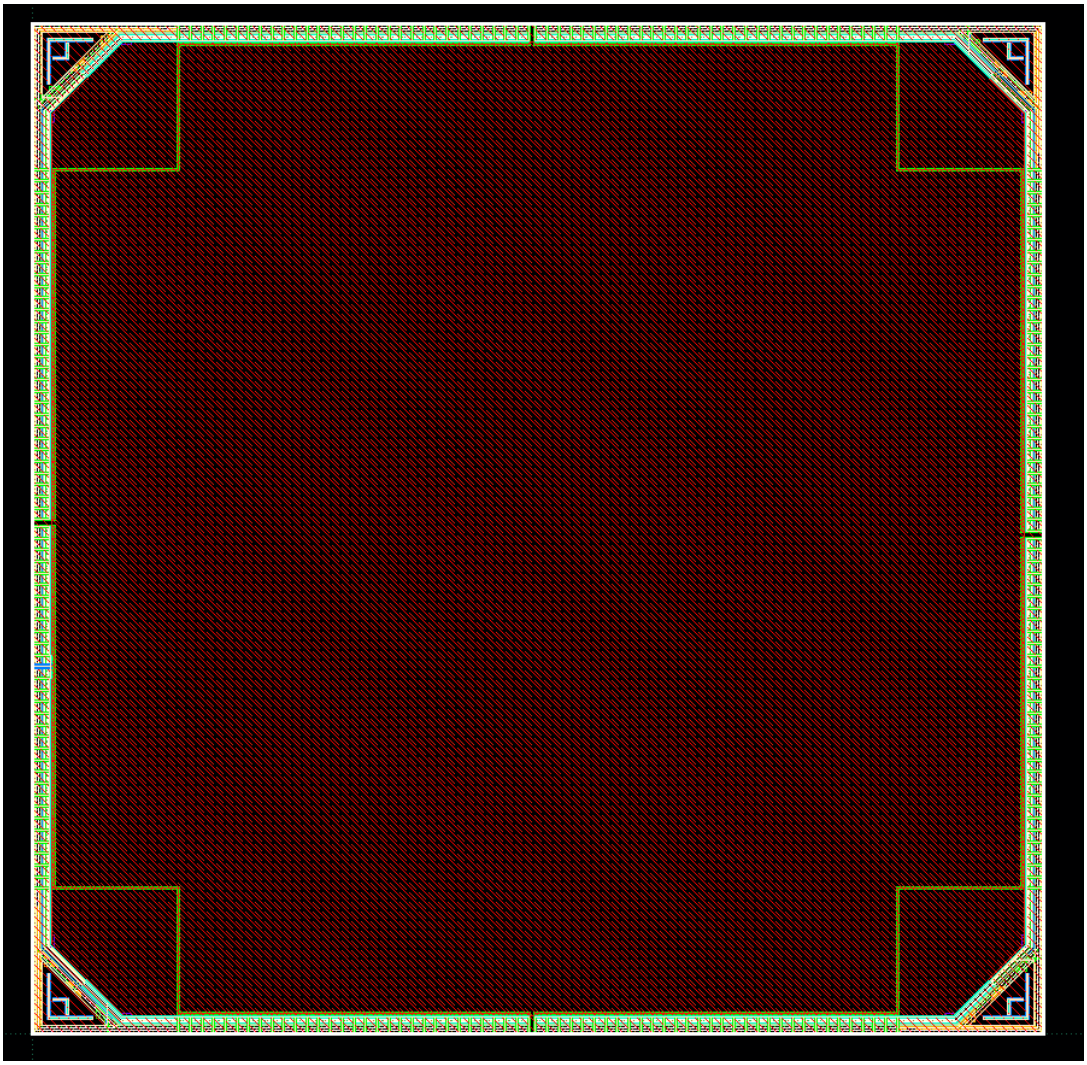


Figure 14: *layout view of sealringCS_6U1x_2U2x_2T8x_LB with L=W=1000µm*

b. Pcell parameters of sealringCS_6U1x_2U2x_2T8x_LB

Below are detailed all the parameters of the cell sealringCS_6U1x_2U2x_2T8x_LB.

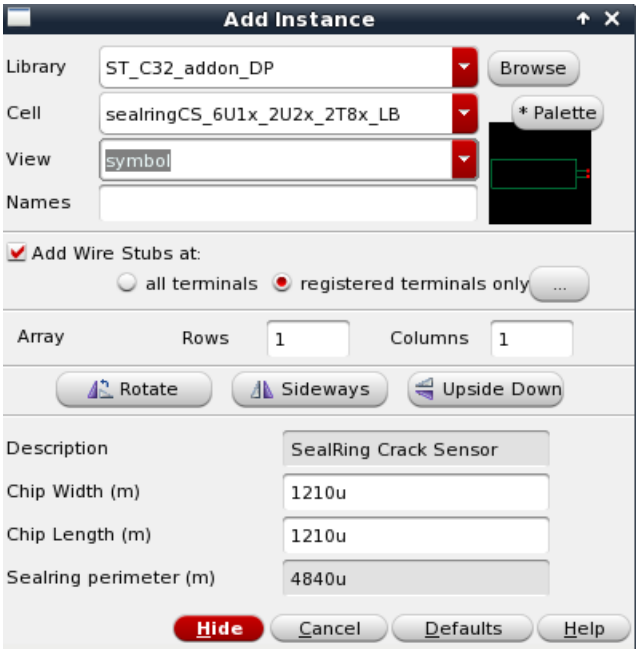


Figure 15: *sealringCS_6U1x_2U2x_2T8x_LB symbol instance parameters*

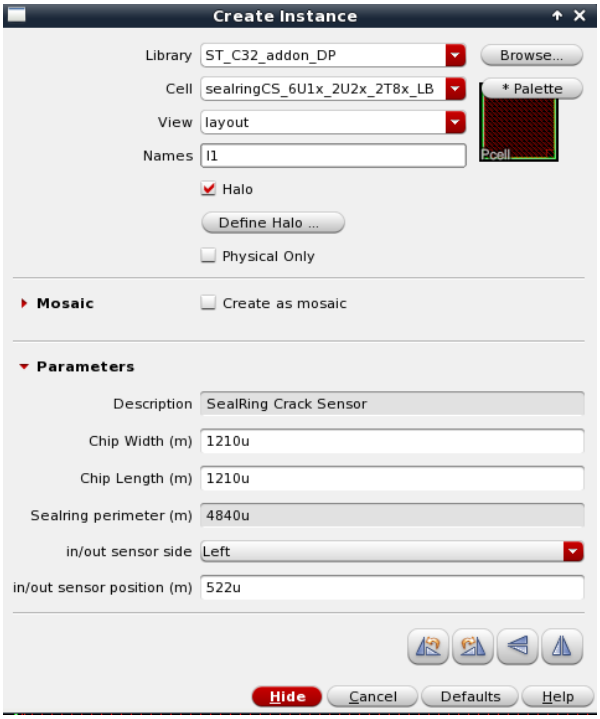


Figure 16: *sealringCS_6U1x_2U2x_2T8x_LB layout instance parameters*

Chip Width (unit *m*): internal dimensions in meter of the chip in horizontal direction.
A callback corrects the value to be an integer, in order that the external dimensions are integers (DRC rule).
Default value: 1210µm
Min value: 285µm
Max value: unlimited

Chip Length (unit *m*): internal dimension in meter of the chip in vertical direction.
A callback rounds the value to be an integer, in order that the external dimensions are integers too (DRC rule).
Default value: 1210µm
Min value: 285µm
Max value: unlimited

Sealring Perimeter (unit *m*): not editable, only the information is given to the user.

In/out sensor side: multiple choices for the side of the in/out pins connections:
Default value: Left
Value: Left/Right/Top/Bottom

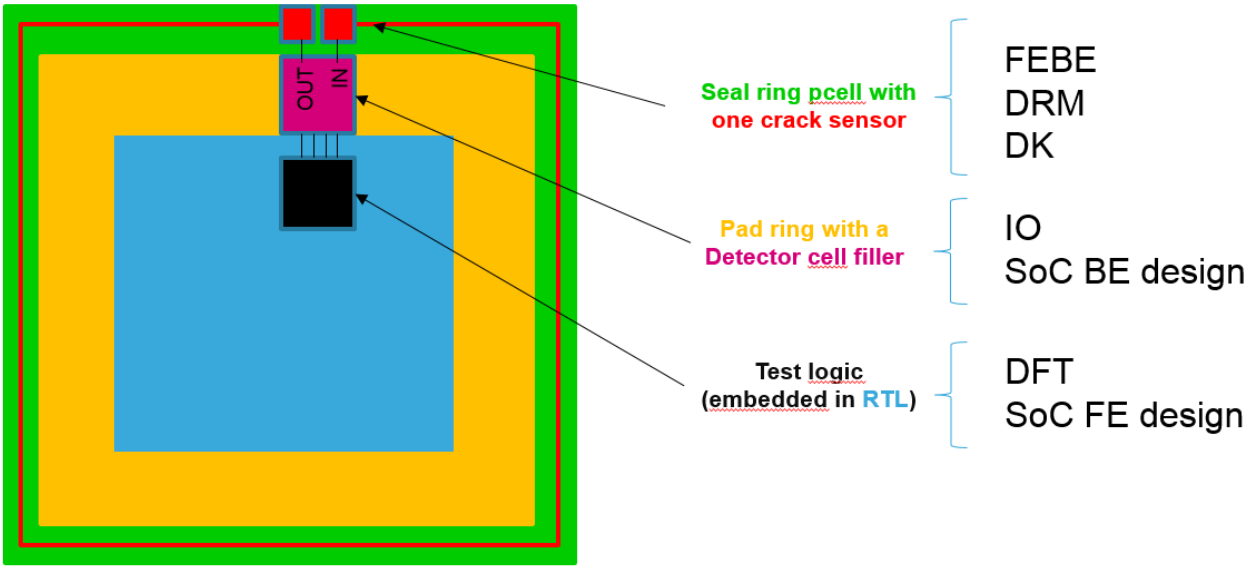
In/out sensor position (unit *m*): position of the pins measured from the external border of the ring (bottom border for Left and Right positions, left border for Top and Bottom positions).
Warning, for the placement of the seal ring around the Chip, please refer to the Design Rules Manual[3].
Default value: 522µm
Min value: 162µm
Max value: defined by Chip Width or Chip Length

[3] Design Rules Manual reference 8343474.

3. SOC Integration

1. Integration concept

Crack seal ring detection is a feature involving several teams in order to introduce it in a SoC design.
Keep in mind that for the placement of the seal ring around the Chip it is highly recommended to refer to the Design Rules Manual.



2. Identification of integration stakeholders

For each techno, the following stakeholders should be involved:

- FEBE owner
- DRM owner
- DK team
- IO team for Seal Ring Crack Detector cell (SRCD)
- SoC design team BE & FE:
  - Integration of test logic + SRCD cell in RTL
  - Integration of SRCD cell in IO ring
  - SoC layout & finishing (connections, sealring, etc…)

3. Technology and others dependences

One Pcell per metal stack in 28FD.

- Key parameters: equivalent parasitic for each SoC size
- Need to know position of sensor pins

One detector filler per IO frame (Detection Cell)

- Depending on parasitic could be either at VDD or VDDE

4. Detection Cell description

Below is a small description of the Detection Cell principle.
Please get in touch with IO team for availability of such cell in Design Platform and dedicated User Manual for correct implementation.

a. Seal Ring Crack Detector cell basics (SRCD)

- Detector supply voltage is technology dependent
- Although possible to implement testing through dedicated pad connection, it is recommended to implement the SRCD using test patterns and test registers

These are below features proposed:

- Bypass (DFT) and Isolation (Low Leakage Mode) supported
- Can be fully deactivated by one layer via/metal fix
- CDM protections embedded for sensors & detection

Note: due to sensor length, detection is slow (1 KHz max testing possible)

The IP is in form of an IO filler cell, is frame dependent, and with a width 20um to 40um.

b. SRCD schematic concept with two sensors

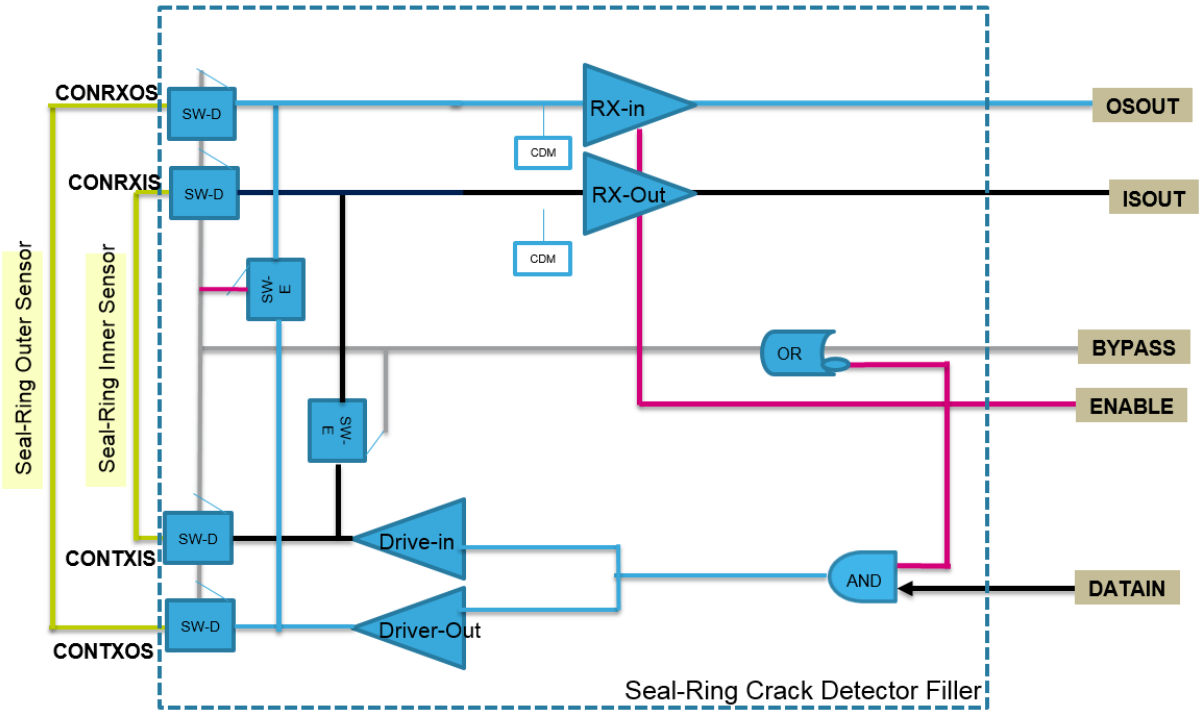


Figure 17: *Schematic concept of SRCD cell*

The main functions are the following:

- Crack detector can be used for digital testing of seal ring sensor.
- With pins ENABLE = H, BYPASS = 0 the crack detector cell is in measurement mode.
- Logic ‘H’ passed through DATAIN pin should be available on ISOUT/OSOUT pins.

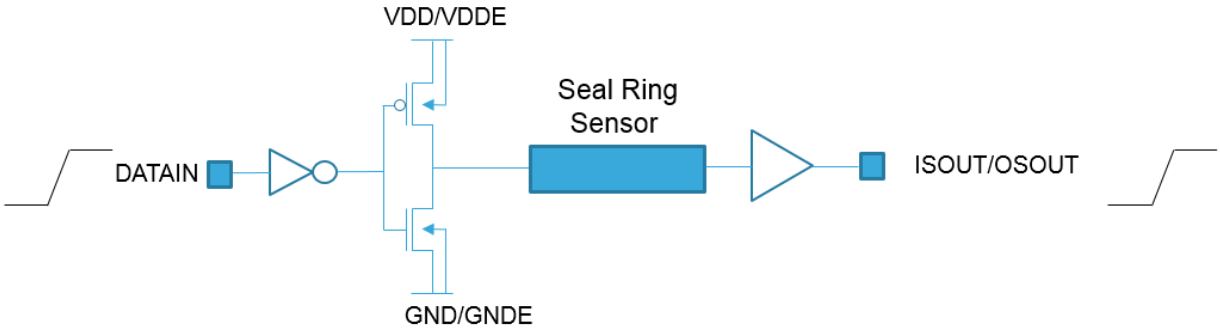


Figure 18: *functionality of SRCD filler cell*

c. SRCD Filler cell truth table

Please refer to SRCD documentation for exact data.

Digital Interface				Seal Ring Interface		Comments
Input Pins			Output Pins	Output Pins	Input Pins	
ENABLE	**BYPASS**	**DATAIN**	**ISOUT / OSOUT**	**CONTXIS/ CONTXOS**	**CONRXIS/ CONRXOS**	
0	X	X	0	Hiz	Hiz	**Isolation mode:** Seal Ring disconnected from crack detector, Seal Ring Input /Output are floating
1	0	D	D	D	D	**Measurement Mode:** Through Sensor , Crack Detector circuit is working
1	1	D	D	Hiz	Hiz	**DFT Mode:** Seal Ring disconnected from crack detector Crack Detector circuit operating internally

- Isolation mode prevents any static current flow if seal ring sensor gets shorted to any voltage between 0 / supply level.
- DFT or Bypass mode enables internal testing of the detector cell, to guarantee functionality of the detector cell vs detected fault.

5. Detection cell test methodologies

a. Implementation with digital IOs

The detector filler cell (SRCD) is connected to seal ring sensors.
Digital IOs (inputs and outputs) are observed to validate seal ring sensor integrity.

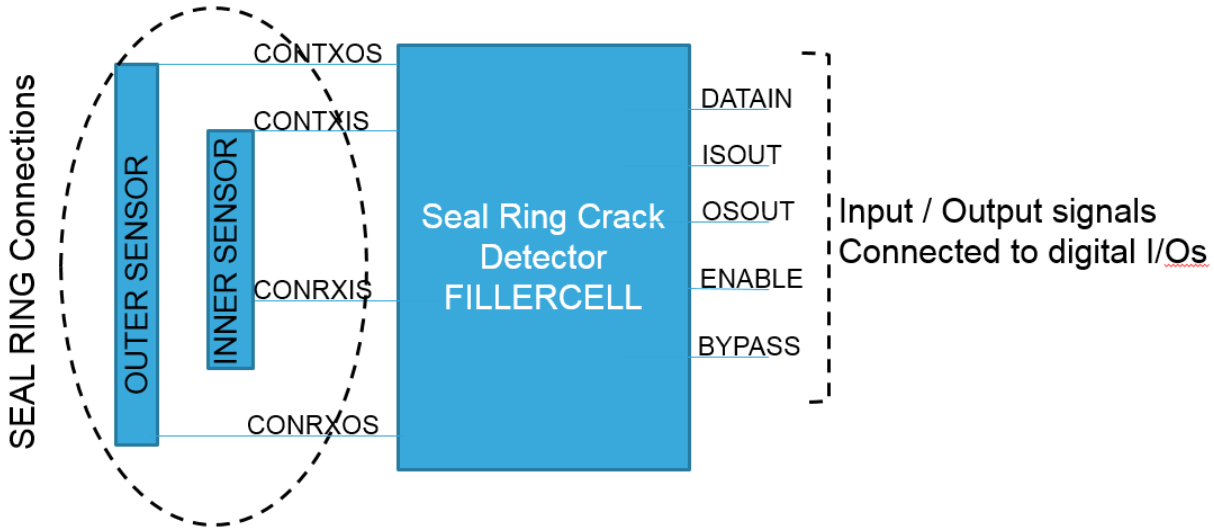


Figure 19: *scheme of SRCD implementation with Digital IOs*

b. Implementation with analog IOs

In this implementation, the detector cell pins (CONTXIS/ CONRXIS) are available externally through ANA pads.
R_{EXT} and C_{EXT} combinations are chosen to validate Crack Detector cell through emulation.
The input (DATAIN) and output (ISOUT) are characterized for each combination.

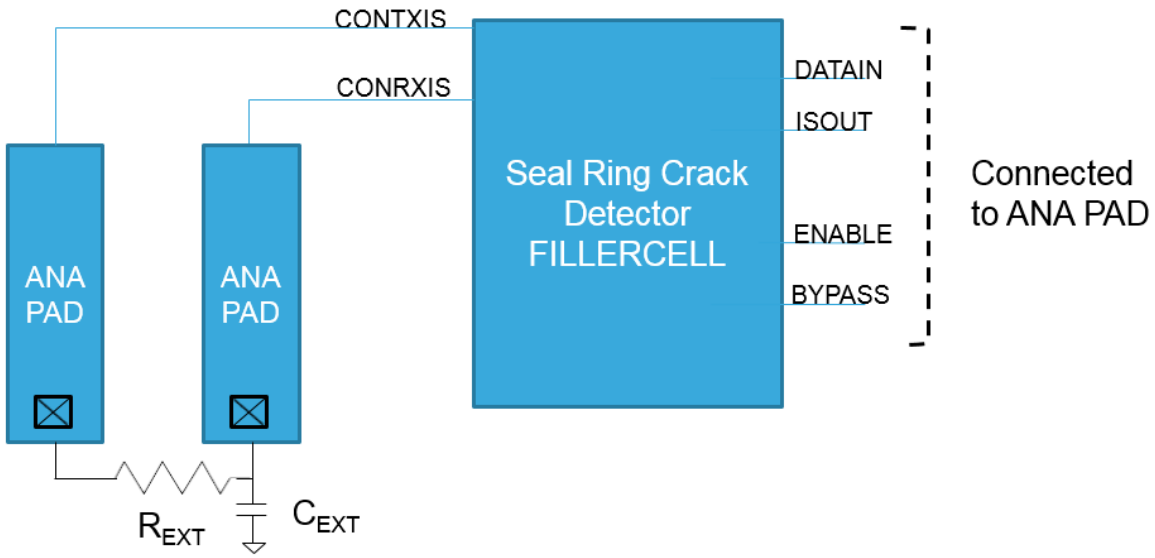


Figure 20: *scheme of SRCD implementation with Analog I/Os*

6. DRC/LVS and integration concept

During SoC implementation:

- Sensor pins towards seal ring can be left unconnected.
- No need to introduce seal ring in the SoC netlist.

The DRC and the LVS can be launched without issue without seal ring.

At chip finishing step:

- Layout/GDS: with seal ring insertion phase, CSRD filler and seal ring will be connected by abutment (providing aligned placement of filler with seal ring Pcell x/y sensor coordinates) In case seal ring is not implemented at min distance, manual connections of CSRD filler pins and seal ring pins required.
- Schematic/CDL: the CDL netlist of the seal ring must be included in the final CDL netlist. In the final CDL, CSRD filler pins towards seal ring must be manually connected to sensor pins of the seal ring schematic.

A simplest procedure is to generate a separate seal ring (layout and schematic), export cdl and make include in the final CDL.

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