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C28SOI_SC_8_COREPBP10_LL
Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 10 nm

Overview

- C28SOI_SC_8_COREPBP10_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

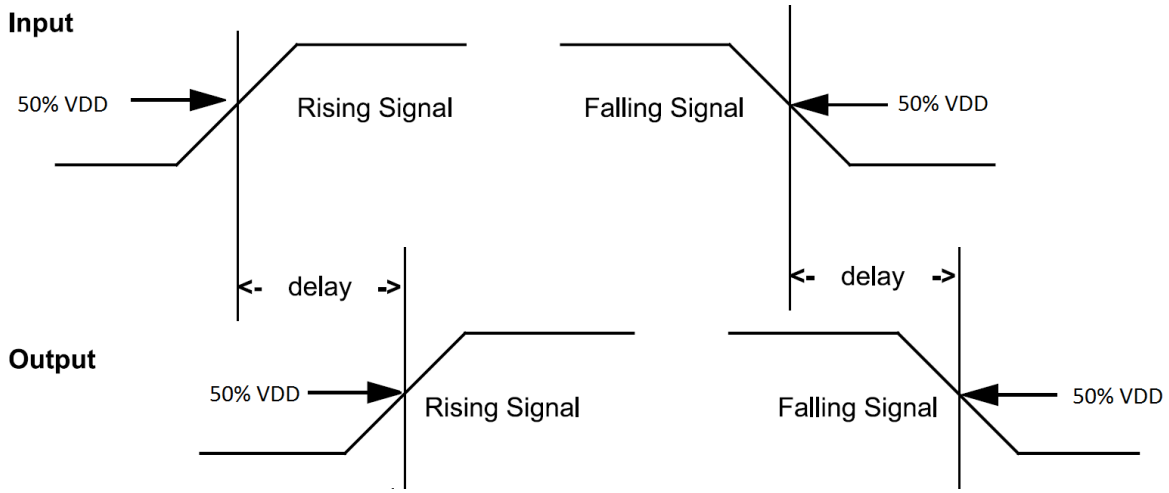


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

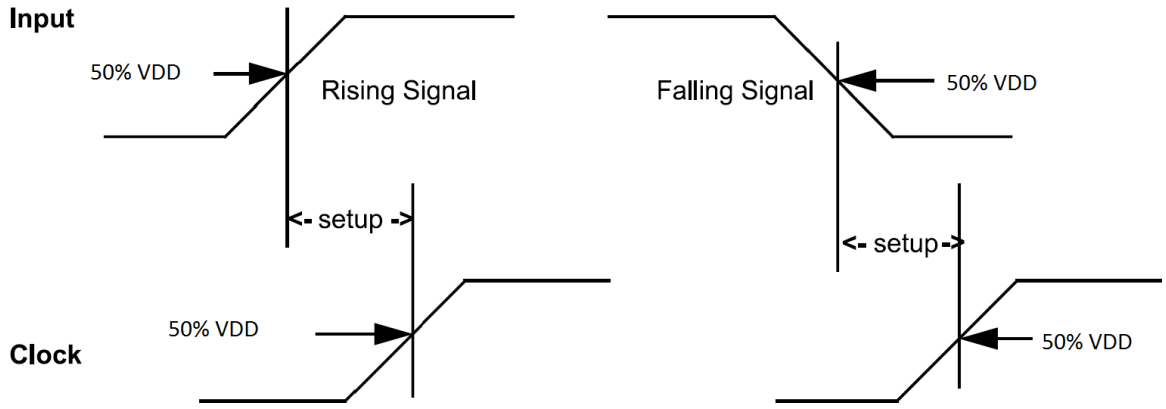


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

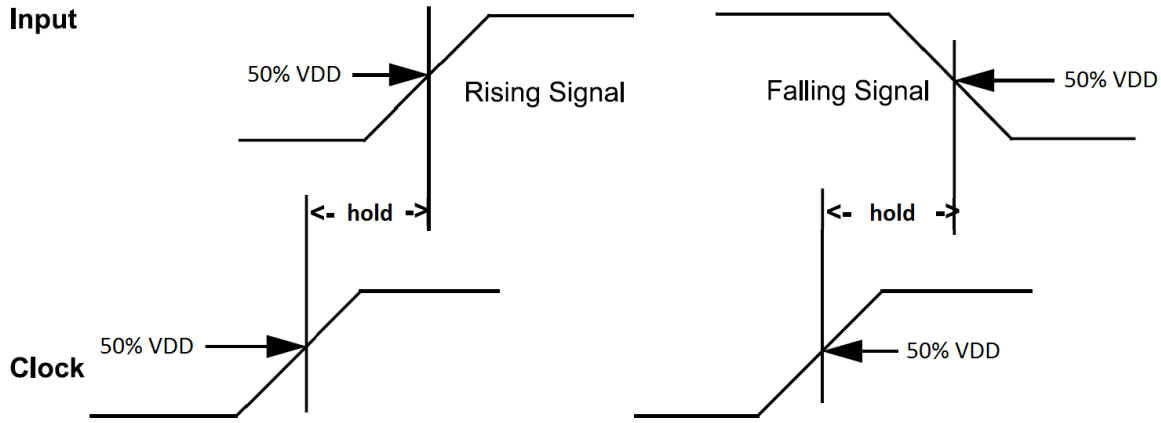


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

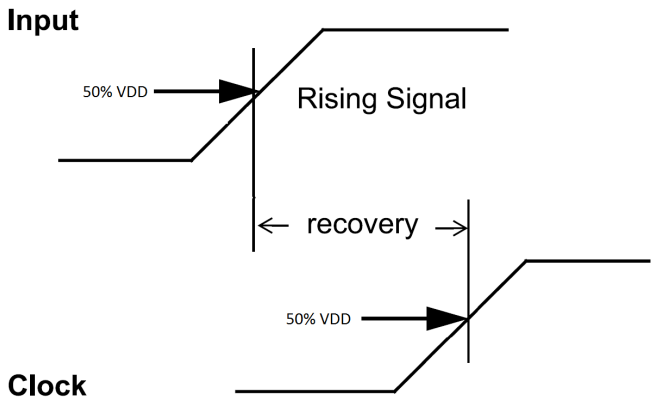


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

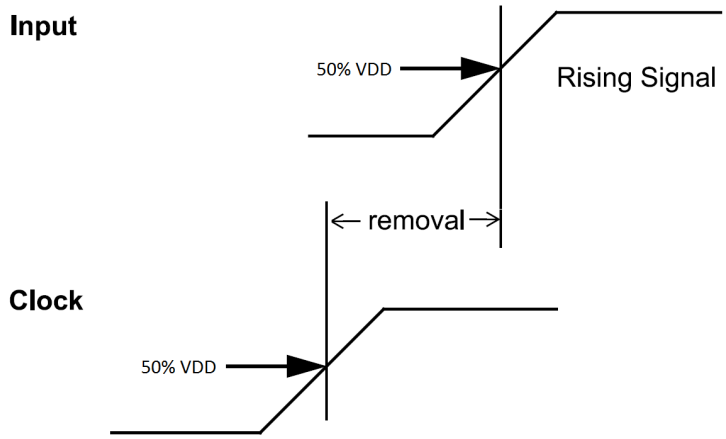


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

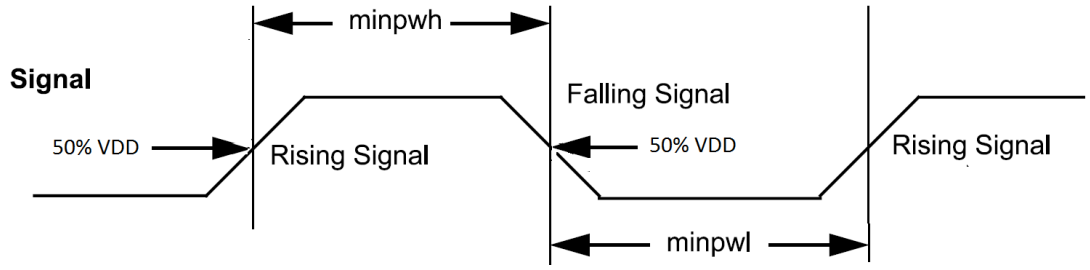


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

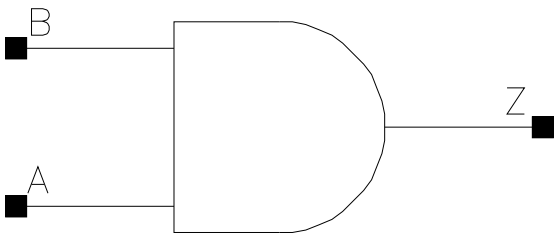
The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description	Logical Symbol
2 input AND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.544	0.4352
X10_P10	0.800	0.680	0.5440
X11_P10	1.600	0.544	0.8704
X19_P10	0.800	1.224	0.9792
X24_P10	0.800	1.360	1.0880
X29_P10	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X11_P10	X19_P10
A	0.0005	0.0007	0.0009	0.0013
B	0.0004	0.0006	0.0008	0.0012
	X24_P10	X29_P10		
A	0.0013	0.0013		
B	0.0012	0.0012		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0393	0.0312	4.5103	2.1487
A to Z ↑	0.0317	0.0284	7.2132	3.4461
B to Z ↓	0.0378	0.0293	4.5153	2.1485
B to Z ↑	0.0333	0.0297	7.2159	3.4402
	X11_P10	**X19_P10**	**X11_P10**	**X19_P10**

A to Z ↓	0.0337	0.0304	1.6615	1.1047
A to Z ↑	0.0264	0.0277	3.3458	1.7353
B to Z ↓	0.0315	0.0291	1.6586	1.1052
B to Z ↑	0.0278	0.0293	3.3478	1.7341
	X24_P10	**X29_P10**	**X24_P10**	**X29_P10**
A to Z ↓	0.0330	0.0348	0.8956	0.7485
A to Z ↑	0.0303	0.0321	1.3925	1.1584
B to Z ↓	0.0317	0.0337	0.8970	0.7488
B to Z ↑	0.0320	0.0341	1.3921	1.1582

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	4.552e-06	1.000e-20
X10_P10	1.001e-05	1.000e-20
X11_P10	1.163e-05	1.000e-20
X19_P10	1.910e-05	1.000e-20
X24_P10	2.208e-05	1.000e-20
X29_P10	2.506e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X11_P10	X19_P10
A (output stable)	4.970e-06	1.048e-05	1.405e-05	2.013e-05
B (output stable)	1.137e-05	2.156e-05	2.989e-05	4.358e-05
A to Z	1.207e-03	1.985e-03	2.412e-03	3.891e-03
B to Z	1.150e-03	1.887e-03	2.253e-03	3.680e-03
	X24_P10	X29_P10		
A (output stable)	2.020e-05	2.025e-05		
B (output stable)	4.395e-05	4.400e-05		
A to Z	4.737e-03	5.441e-03		
B to Z	4.529e-03	5.243e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

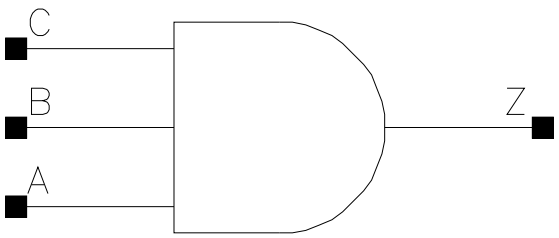
Pin Cycle (vdds)	X5_P10	X10_P10	X11_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P10	X29_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.680	0.5440
X10_P10	0.800	0.816	0.6528
X14_P10	0.800	1.360	1.0880
X19_P10	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0004	0.0007	0.0011	0.0014
B	0.0004	0.0006	0.0009	0.0012
C	0.0004	0.0006	0.0009	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0442	0.0350	4.5726	2.1648
A to Z ↑	0.0437	0.0383	7.3043	3.4865
B to Z ↓	0.0432	0.0333	4.5730	2.1620
B to Z ↑	0.0445	0.0387	7.3029	3.4860
C to Z ↓	0.0418	0.0318	4.5705	2.1607
C to Z ↑	0.0458	0.0393	7.2985	3.4867
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0351	0.0332	1.4897	1.1088

A to Z ↑	0.0369	0.0357	2.3604	1.7518
B to Z ↓	0.0335	0.0315	1.4881	1.1070
B to Z ↑	0.0374	0.0363	2.3607	1.7504
C to Z ↓	0.0320	0.0299	1.4875	1.1070
C to Z ↑	0.0384	0.0368	2.3603	1.7512

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	4.173e-06	1.000e-20
X10_P10	9.281e-06	1.000e-20
X14_P10	1.303e-05	1.000e-20
X19_P10	1.798e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	5.994e-06	1.257e-05	1.633e-05	2.269e-05
B (output stable)	8.049e-06	1.679e-05	2.279e-05	3.320e-05
C (output stable)	2.258e-05	4.600e-05	6.503e-05	9.667e-05
A to Z	1.413e-03	2.331e-03	3.369e-03	4.390e-03
B to Z	1.355e-03	2.221e-03	3.199e-03	4.162e-03
C to Z	1.308e-03	2.119e-03	3.055e-03	3.942e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

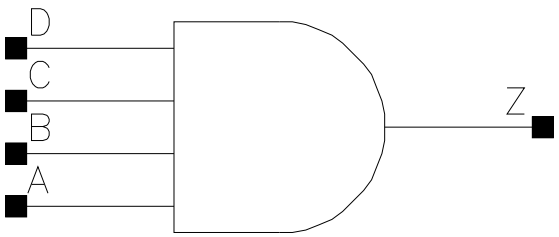
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.088	0.8704
X3_P10	0.800	1.088	0.8704
X10_P10	0.800	2.176	1.7408
X13_P10	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P10	X3_P10	X10_P10	X13_P10
A	0.0005	0.0005	0.0010	0.0012
B	0.0004	0.0004	0.0010	0.0012
C	0.0004	0.0004	0.0010	0.0012
D	0.0005	0.0005	0.0010	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	X3_P10	X2_P10	X3_P10
A to Z ↓	0.0345	0.0370	8.6872	5.5734
A to Z ↑	0.0369	0.0365	26.5642	13.6407
B to Z ↓	0.0326	0.0358	8.6863	5.5741
B to Z ↑	0.0384	0.0382	26.5959	13.6591
C to Z ↓	0.0353	0.0379	8.6878	5.5683
C to Z ↑	0.0364	0.0356	26.6177	13.6781

D to Z ↓	0.0338	0.0375	8.6779	5.5675
D to Z ↑	0.0385	0.0391	26.6249	13.6763
	X10_P10	**X13_P10**	**X10_P10**	**X13_P10**
A to Z ↓	0.0349	0.0342	1.9162	1.4234
A to Z ↑	0.0349	0.0369	4.4757	3.4298
B to Z ↓	0.0334	0.0313	1.9160	1.4222
B to Z ↑	0.0365	0.0370	4.4769	3.4324
C to Z ↓	0.0345	0.0326	1.8984	1.4281
C to Z ↑	0.0325	0.0314	4.4763	3.4304
D to Z ↓	0.0314	0.0299	1.8959	1.4241
D to Z ↑	0.0324	0.0316	4.4760	3.4303

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P10	3.914e-06	1.000e-20
X3_P10	5.125e-06	1.000e-20
X10_P10	1.533e-05	1.000e-20
X13_P10	2.108e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P10	X3_P10	X10_P10	X13_P10
A (output stable)	2.553e-04	3.079e-04	8.140e-04	1.094e-03
B (output stable)	2.362e-04	2.872e-04	7.553e-04	9.996e-04
C (output stable)	2.589e-04	2.872e-04	7.569e-04	9.596e-04
D (output stable)	2.401e-04	2.760e-04	6.786e-04	8.644e-04
A to Z	9.610e-04	1.287e-03	3.687e-03	4.909e-03
B to Z	9.072e-04	1.228e-03	3.528e-03	4.552e-03
C to Z	9.774e-04	1.254e-03	3.188e-03	3.957e-03
D to Z	9.266e-04	1.223e-03	2.878e-03	3.608e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

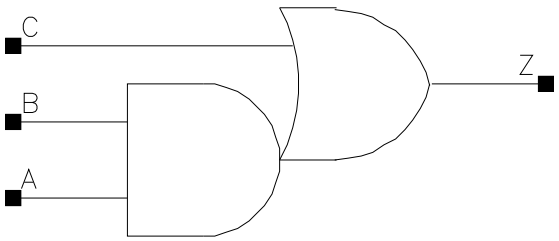
Pin Cycle (vdds)	X2_P10	X3_P10	X10_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	0.952	0.7616
X19_P10	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0004	0.0005	0.0011
B	0.0004	0.0006	0.0010
C	0.0004	0.0006	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0538	0.0457	4.3374	2.1704
A to Z ↑	0.0354	0.0311	6.7652	3.4186
B to Z ↓	0.0510	0.0431	4.3259	2.1614
B to Z ↑	0.0377	0.0332	6.7614	3.4240
C to Z ↓	0.0558	0.0456	4.3112	2.1588
C to Z ↑	0.0323	0.0285	6.7155	3.4014
	X19_P10		**X19_P10**	
A to Z ↓	0.0440		1.1269	
A to Z ↑	0.0342		1.7263	

B to Z ↓	0.0423		1.1264	
B to Z ↑	0.0363		1.7246	
C to Z ↓	0.0443		1.1236	
C to Z ↑	0.0306		1.7110	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	5.610e-06	1.000e-20
X10_P10	1.114e-05	1.000e-20
X19_P10	1.987e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	1.091e-05	2.404e-05	5.099e-05
B (output stable)	1.292e-05	2.857e-05	5.827e-05
C (output stable)	3.066e-05	4.082e-05	9.742e-05
A to Z	1.388e-03	2.256e-03	4.334e-03
B to Z	1.334e-03	2.158e-03	4.185e-03
C to Z	1.545e-03	2.444e-03	4.713e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

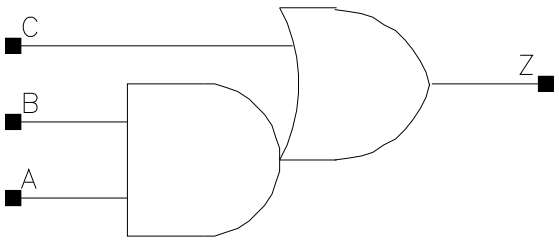
Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	0.952	0.7616
X14_P10	0.800	1.632	1.3056
X19_P10	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0004	0.0006	0.0012	0.0012
B	0.0004	0.0006	0.0012	0.0012
C	0.0005	0.0006	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0574	0.0488	4.3187	2.1909
A to Z ↑	0.0384	0.0345	6.8665	3.4441
B to Z ↓	0.0555	0.0466	4.3069	2.1870
B to Z ↑	0.0414	0.0366	6.8629	3.4398
C to Z ↓	0.0490	0.0425	4.2893	2.1786
C to Z ↑	0.0285	0.0251	6.7840	3.4066
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0440	0.0472	1.4826	1.1179

A to Z ↑	0.0316	0.0334	2.3280	1.7406
B to Z ↓	0.0401	0.0435	1.4791	1.1154
B to Z ↑	0.0324	0.0345	2.3310	1.7411
C to Z ↓	0.0355	0.0388	1.4755	1.1109
C to Z ↑	0.0221	0.0235	2.3069	1.7206

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	5.622e-06	1.000e-20
X10_P10	1.051e-05	1.000e-20
X14_P10	1.888e-05	1.000e-20
X19_P10	2.167e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	7.519e-06	1.011e-05	3.425e-05	3.431e-05
B (output stable)	1.030e-05	1.345e-05	6.183e-05	6.189e-05
C (output stable)	7.018e-05	1.149e-04	3.157e-04	3.158e-04
A to Z	1.554e-03	2.385e-03	4.236e-03	4.973e-03
B to Z	1.508e-03	2.284e-03	3.884e-03	4.623e-03
C to Z	1.293e-03	2.007e-03	3.279e-03	3.968e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

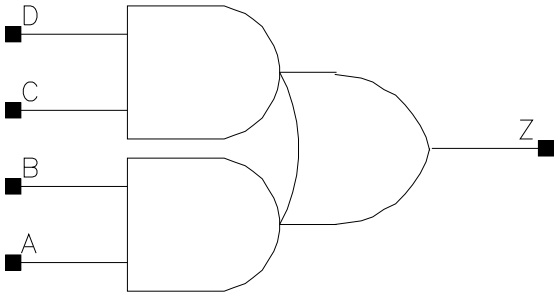
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.088	0.8704
X10_P10	0.800	1.088	0.8704
X14_P10	0.800	1.768	1.4144
X19_P10	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0005	0.0006	0.0012	0.0012
B	0.0005	0.0008	0.0011	0.0011
C	0.0004	0.0006	0.0013	0.0012
D	0.0005	0.0006	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0582	0.0483	4.3353	2.1780
A to Z ↑	0.0403	0.0364	6.8983	3.4259
B to Z ↓	0.0538	0.0444	4.3110	2.1673

B to Z ↑	0.0409	0.0372	6.8971	3.4253
C to Z ↓	0.0512	0.0432	4.3189	2.1687
C to Z ↑	0.0340	0.0304	6.8839	3.4157
D to Z ↓	0.0493	0.0412	4.3075	2.1646
D to Z ↑	0.0366	0.0325	6.8787	3.4163
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0432	0.0466	1.4836	1.1228
A to Z ↑	0.0321	0.0343	2.3370	1.7508
B to Z ↓	0.0405	0.0441	1.4813	1.1211
B to Z ↑	0.0339	0.0362	2.3357	1.7507
C to Z ↓	0.0387	0.0422	1.4803	1.1198
C to Z ↑	0.0276	0.0298	2.3253	1.7426
D to Z ↓	0.0363	0.0399	1.4785	1.1181
D to Z ↑	0.0290	0.0315	2.3255	1.7439

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	6.270e-06	1.000e-20
X10_P10	1.225e-05	1.000e-20
X14_P10	2.022e-05	1.000e-20
X19_P10	2.310e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.821e-05	2.431e-05	3.027e-05	3.037e-05
B (output stable)	8.640e-05	8.339e-05	4.185e-05	4.193e-05
C (output stable)	1.883e-05	2.889e-05	6.645e-05	6.666e-05
D (output stable)	2.206e-05	3.661e-05	8.128e-05	8.148e-05
A to Z	1.789e-03	2.733e-03	4.369e-03	5.217e-03
B to Z	1.621e-03	2.481e-03	4.118e-03	4.966e-03
C to Z	1.490e-03	2.290e-03	3.593e-03	4.425e-03
D to Z	1.428e-03	2.188e-03	3.374e-03	4.206e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

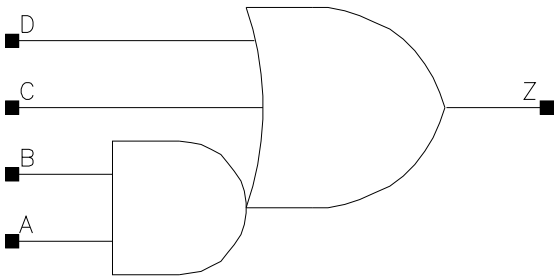
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	1.088	0.8704
X19_P10	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0004	0.0006	0.0010
B	0.0004	0.0006	0.0010
C	0.0004	0.0005	0.0012
D	0.0004	0.0005	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0677	0.0553	4.8569	2.2679
A to Z ↑	0.0368	0.0305	7.1800	3.4304
B to Z ↓	0.0654	0.0518	4.8456	2.2568
B to Z ↑	0.0393	0.0324	7.1814	3.4321
C to Z ↓	0.0732	0.0601	4.8352	2.2579
C to Z ↑	0.0328	0.0399	7.1294	3.4411

D to Z ↓	0.0720	0.0601	4.8373	2.2584
D to Z ↑	0.0327	0.0395	7.1278	3.4379
	X19_P10		**X19_P10**	
A to Z ↓	0.0546		1.1737	
A to Z ↑	0.0334		1.7137	
B to Z ↓	0.0498		1.1662	
B to Z ↑	0.0342		1.7119	
C to Z ↓	0.0578		1.1670	
C to Z ↑	0.0326		1.7039	
D to Z ↓	0.0566		1.1676	
D to Z ↑	0.0321		1.7027	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	4.696e-06	1.000e-20
X10_P10	1.005e-05	1.000e-20
X19_P10	1.845e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	1.383e-05	2.881e-05	6.001e-05
B (output stable)	1.431e-05	2.993e-05	7.345e-05
C (output stable)	1.370e-05	2.568e-05	5.490e-05
D (output stable)	1.560e-05	2.949e-05	5.686e-05
A to Z	1.471e-03	2.383e-03	4.667e-03
B to Z	1.423e-03	2.273e-03	4.312e-03
C to Z	1.671e-03	2.810e-03	5.309e-03
D to Z	1.590e-03	2.669e-03	4.984e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

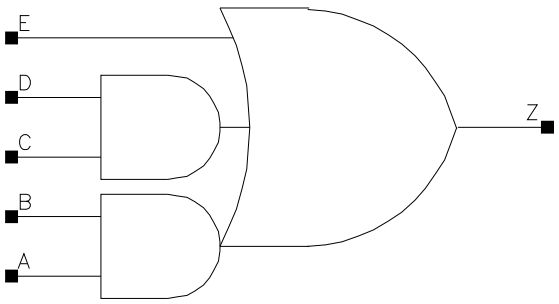
Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.088	0.8704
X10_P10	0.800	1.224	0.9792
X19_P10	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0004	0.0006	0.0011
B	0.0004	0.0006	0.0010
C	0.0004	0.0007	0.0011
D	0.0004	0.0006	0.0010
E	0.0004	0.0006	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0870	0.0664	4.5763	2.2515
A to Z ↑	0.0467	0.0380	6.9739	3.4568

B to Z ↓	0.0862	0.0637	4.5639	2.2466
B to Z ↑	0.0504	0.0403	6.9715	3.4542
C to Z ↓	0.0753	0.0575	4.5586	2.2443
C to Z ↑	0.0412	0.0324	6.9199	3.4299
D to Z ↓	0.0714	0.0526	4.5424	2.2349
D to Z ↑	0.0436	0.0340	6.9215	3.4311
E to Z ↓	0.0770	0.0583	4.5300	2.2349
E to Z ↑	0.0352	0.0291	6.8483	3.4090
	X19_P10		**X19_P10**	
A to Z ↓	0.0636		1.1598	
A to Z ↑	0.0394		1.7370	
B to Z ↓	0.0608		1.1576	
B to Z ↑	0.0418		1.7354	
C to Z ↓	0.0535		1.1555	
C to Z ↑	0.0327		1.7221	
D to Z ↓	0.0504		1.1521	
D to Z ↑	0.0347		1.7223	
E to Z ↓	0.0557		1.1517	
E to Z ↑	0.0362		1.7168	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	5.728e-06	1.000e-20
X10_P10	1.187e-05	1.000e-20
X19_P10	2.117e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	7.895e-06	1.422e-05	2.903e-05
B (output stable)	1.154e-05	1.595e-05	2.977e-05
C (output stable)	2.137e-05	3.351e-05	6.997e-05
D (output stable)	2.280e-05	3.932e-05	7.556e-05
E (output stable)	3.985e-05	7.502e-05	1.536e-04
A to Z	2.035e-03	3.101e-03	5.897e-03
B to Z	2.004e-03	2.983e-03	5.666e-03
C to Z	1.687e-03	2.499e-03	4.657e-03
D to Z	1.626e-03	2.364e-03	4.455e-03
E to Z	1.771e-03	2.673e-03	5.072e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

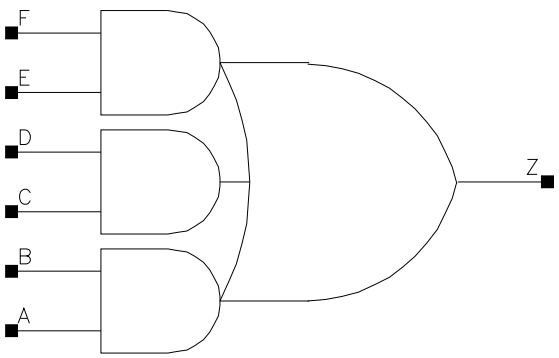
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.360	1.0880
X5_P10	0.800	1.360	1.0880
X10_P10	0.800	1.632	1.3056
X19_P10	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P10	X5_P10	X10_P10	X19_P10
A	0.0005	0.0005	0.0007	0.0011

B	0.0005	0.0005	0.0007	0.0010
C	0.0006	0.0006	0.0005	0.0011
D	0.0005	0.0005	0.0005	0.0010
E	0.0006	0.0006	0.0006	0.0011
F	0.0005	0.0005	0.0006	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X5_P10**	**X2_P10**	**X5_P10**
A to Z ↓	0.0652	0.0672	8.9359	4.6595
A to Z ↑	0.0456	0.0445	14.1564	7.3040
B to Z ↓	0.0627	0.0648	8.9060	4.6462
B to Z ↑	0.0485	0.0475	14.1495	7.3037
C to Z ↓	0.0605	0.0626	8.9225	4.6543
C to Z ↑	0.0424	0.0415	14.0241	7.2451
D to Z ↓	0.0558	0.0580	8.8965	4.6418
D to Z ↑	0.0440	0.0432	14.0198	7.2427
E to Z ↓	0.0494	0.0514	8.8872	4.6371
E to Z ↑	0.0352	0.0343	13.9321	7.2047
F to Z ↓	0.0456	0.0478	8.8674	4.6258
F to Z ↑	0.0367	0.0361	13.9398	7.2080
	X10_P10	**X19_P10**	**X10_P10**	**X19_P10**
A to Z ↓	0.0718	0.0661	2.2558	1.1580
A to Z ↑	0.0470	0.0427	3.4817	1.7443
B to Z ↓	0.0679	0.0638	2.2424	1.1565
B to Z ↑	0.0483	0.0451	3.4816	1.7434
C to Z ↓	0.0652	0.0609	2.2481	1.1571
C to Z ↑	0.0418	0.0393	3.4615	1.7332
D to Z ↓	0.0631	0.0588	2.2423	1.1550
D to Z ↑	0.0444	0.0418	3.4622	1.7321
E to Z ↓	0.0564	0.0542	2.2408	1.1536
E to Z ↑	0.0358	0.0342	3.4445	1.7259
F to Z ↓	0.0533	0.0510	2.2333	1.1508
F to Z ↑	0.0379	0.0363	3.4441	1.7256

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P10	5.964e-06	1.000e-20
X5_P10	7.663e-06	1.000e-20
X10_P10	1.278e-05	1.000e-20
X19_P10	2.394e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P10	X5_P10	X10_P10	X19_P10
A (output stable)	1.688e-05	1.687e-05	2.609e-05	3.888e-05
B (output stable)	1.830e-05	1.830e-05	5.912e-05	4.288e-05
C (output stable)	2.101e-05	2.102e-05	2.535e-05	5.057e-05
D (output stable)	2.495e-05	2.498e-05	2.996e-05	6.051e-05
E (output stable)	3.832e-05	3.835e-05	5.463e-05	8.971e-05
F (output stable)	4.265e-05	4.267e-05	5.720e-05	9.813e-05

A to Z	1.977e-03	2.258e-03	3.503e-03	6.387e-03
B to Z	1.903e-03	2.182e-03	3.283e-03	6.170e-03
C to Z	1.643e-03	1.920e-03	3.051e-03	5.602e-03
D to Z	1.549e-03	1.823e-03	2.961e-03	5.422e-03
E to Z	1.262e-03	1.530e-03	2.612e-03	4.895e-03
F to Z	1.190e-03	1.456e-03	2.513e-03	4.691e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

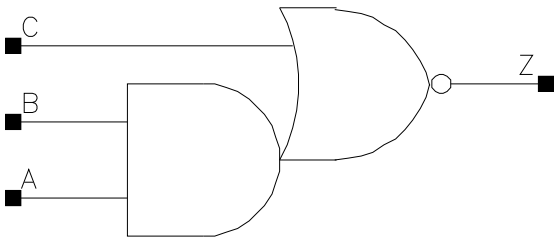
Pin Cycle (vdds)	X2_P10	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X10_P10	0.800	1.360	1.0880
X19_P10	0.800	2.584	2.0672
X25_P10	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P10	X10_P10	X19_P10	X25_P10
A	0.0006	0.0014	0.0028	0.0036
B	0.0005	0.0013	0.0025	0.0034
C	0.0005	0.0015	0.0028	0.0037

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X10_P10**	**X3_P10**	**X10_P10**
A to Z ↓	0.0116	0.0125	7.4468	2.6711
A to Z ↑	0.0210	0.0215	12.9123	4.3910
B to Z ↓	0.0123	0.0126	7.5005	2.6924
B to Z ↑	0.0178	0.0173	12.7566	4.3835
C to Z ↓	0.0123	0.0125	4.3603	1.5173
C to Z ↑	0.0223	0.0225	11.7878	4.0314
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0132	0.0130	1.3550	1.0310

A to Z ↑	0.0222	0.0218	2.2330	1.6663
B to Z ↓	0.0125	0.0126	1.3671	1.0397
B to Z ↑	0.0175	0.0175	2.2324	1.6801
C to Z ↓	0.0142	0.0145	0.9261	0.7144
C to Z ↑	0.0227	0.0226	2.0525	1.5380

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	4.511e-06	1.000e-20
X10_P10	1.215e-05	1.000e-20
X19_P10	2.307e-05	1.000e-20
X25_P10	3.036e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X10_P10	X19_P10	X25_P10
A (output stable)	2.459e-05	8.569e-05	1.722e-04	2.233e-04
B (output stable)	3.088e-05	1.158e-04	2.377e-04	3.034e-04
C (output stable)	4.325e-05	1.427e-04	2.745e-04	3.727e-04
A to Z	5.623e-04	1.771e-03	3.700e-03	4.799e-03
B to Z	4.655e-04	1.331e-03	2.722e-03	3.593e-03
C to Z	8.068e-04	2.411e-03	4.761e-03	6.356e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

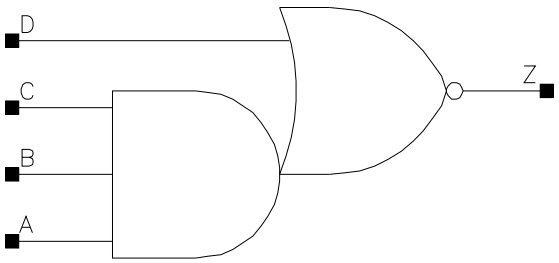
Pin Cycle (vdds)	X3_P10	X10_P10	X19_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X17_P10	0.800	3.536	2.8288
X22_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X17_P10	X22_P10
A	0.0005	0.0028	0.0037
B	0.0005	0.0026	0.0035
C	0.0006	0.0025	0.0033
D	0.0006	0.0029	0.0037

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X17_P10	X3_P10	X17_P10
A to Z ↓	0.0179	0.0191	10.6398	1.9828
A to Z ↑	0.0276	0.0268	12.9145	2.1744
B to Z ↓	0.0183	0.0187	10.6568	1.9873
B to Z ↑	0.0250	0.0239	12.9242	2.1975
C to Z ↓	0.0197	0.0173	10.7065	1.9940
C to Z ↑	0.0238	0.0199	12.9655	2.2075
D to Z ↓	0.0150	0.0167	4.2557	0.9134

D to Z ↑	0.0281	0.0262	11.0628	1.8734
	X22_P10		**X22_P10**	
A to Z ↓	0.0189		1.5031	
A to Z ↑	0.0264		1.6270	
B to Z ↓	0.0184		1.5068	
B to Z ↑	0.0235		1.6484	
C to Z ↓	0.0172		1.5123	
C to Z ↑	0.0195		1.6589	
D to Z ↓	0.0174		0.7583	
D to Z ↑	0.0255		1.4024	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	4.831e-06	1.000e-20
X17_P10	2.256e-05	1.000e-20
X22_P10	2.900e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X17_P10	X22_P10
A (output stable)	1.684e-05	1.156e-04	1.525e-04
B (output stable)	1.835e-05	1.537e-04	2.017e-04
C (output stable)	3.051e-05	3.209e-04	4.193e-04
D (output stable)	6.713e-05	4.074e-04	5.392e-04
A to Z	8.986e-04	5.194e-03	6.749e-03
B to Z	7.865e-04	4.289e-03	5.543e-03
C to Z	6.973e-04	3.345e-03	4.326e-03
D to Z	1.175e-03	6.305e-03	8.188e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

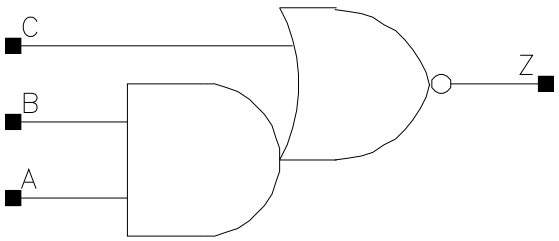
Pin Cycle (vdds)	X3_P10	X17_P10	X22_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X6_P10	0.800	1.088	0.8704
X9_P10	0.800	1.360	1.0880
X12_P10	0.800	1.904	1.5232
X25_P10	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X9_P10	X12_P10
A	0.0005	0.0011	0.0016	0.0021
B	0.0005	0.0010	0.0014	0.0019
C	0.0005	0.0009	0.0013	0.0017
	X25_P10			
A	0.0041			
B	0.0038			
C	0.0033			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0160	0.0157	9.9771	3.8947
A to Z ↑	0.0246	0.0261	14.8302	6.5367
B to Z ↓	0.0178	0.0156	10.0294	3.9205

B to Z ↑	0.0226	0.0221	14.6939	6.5517
C to Z ↓	0.0107	0.0093	5.9087	2.7673
C to Z ↑	0.0187	0.0169	13.6433	6.0434
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0150	0.0156	2.6750	2.0030
A to Z ↑	0.0244	0.0248	4.3754	3.2438
B to Z ↓	0.0154	0.0153	2.6946	2.0178
B to Z ↑	0.0205	0.0207	4.3726	3.2775
C to Z ↓	0.0093	0.0091	1.9006	1.4134
C to Z ↑	0.0160	0.0162	4.0458	3.0188
	X25_P10		**X25_P10**	
A to Z ↓	0.0153		1.0407	
A to Z ↑	0.0240		1.6415	
B to Z ↓	0.0153		1.0481	
B to Z ↑	0.0200		1.6471	
C to Z ↓	0.0089		0.7204	
C to Z ↑	0.0156		1.5234	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	3.516e-06	1.000e-20
X6_P10	8.521e-06	1.000e-20
X9_P10	1.174e-05	1.000e-20
X12_P10	1.596e-05	1.000e-20
X25_P10	3.076e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	9.970e-06	3.373e-05	4.387e-05	6.486e-05
B (output stable)	1.294e-05	6.110e-05	6.970e-05	1.146e-04
C (output stable)	1.189e-04	3.080e-04	3.965e-04	5.493e-04
A to Z	7.347e-04	1.826e-03	2.484e-03	3.448e-03
B to Z	6.572e-04	1.480e-03	1.987e-03	2.707e-03
C to Z	4.228e-04	9.134e-04	1.240e-03	1.726e-03
	X25_P10			
A (output stable)	1.227e-04			
B (output stable)	2.001e-04			
C (output stable)	1.045e-03			
A to Z	6.538e-03			
B to Z	5.183e-03			
C to Z	3.226e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

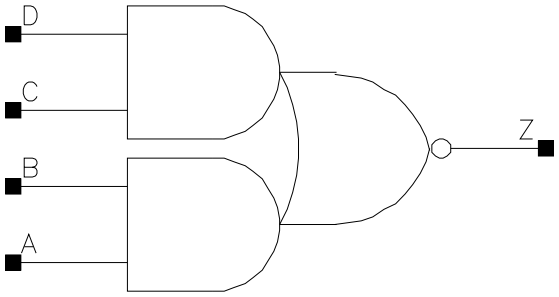
	X25_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.680	0.5440
X6_P10	0.800	1.224	0.9792
X9_P10	0.800	1.768	1.4144
X12_P10	0.800	2.448	1.9584
X24_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P10	X6_P10	X9_P10	X12_P10
A	0.0004	0.0011	0.0016	0.0021
B	0.0004	0.0009	0.0014	0.0020
C	0.0004	0.0011	0.0014	0.0019
D	0.0004	0.0008	0.0013	0.0018
	X24_P10			
A	0.0040			
B	0.0039			
C	0.0037			
D	0.0035			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X6_P10**	**X2_P10**	**X6_P10**
A to Z ↓	0.0161	0.0164	10.1371	3.7947
A to Z ↑	0.0313	0.0269	18.8269	5.9710
B to Z ↓	0.0176	0.0177	10.1925	3.8154
B to Z ↑	0.0282	0.0241	18.8117	6.0641
C to Z ↓	0.0119	0.0117	10.1371	3.8036
C to Z ↑	0.0238	0.0208	18.8061	5.9650
D to Z ↓	0.0127	0.0124	10.2209	3.8331
D to Z ↑	0.0207	0.0181	18.7703	6.0953
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0177	0.0182	2.6796	2.0114
A to Z ↑	0.0282	0.0289	4.0052	3.0089
B to Z ↓	0.0187	0.0187	2.6957	2.0229
B to Z ↑	0.0249	0.0253	4.0111	2.9827
C to Z ↓	0.0127	0.0135	2.6730	2.0103
C to Z ↑	0.0219	0.0227	4.0038	2.9922
D to Z ↓	0.0130	0.0128	2.6963	2.0295
D to Z ↑	0.0183	0.0185	4.0037	3.0009
	X24_P10		**X24_P10**	
A to Z ↓	0.0181		1.0322	
A to Z ↑	0.0283		1.5150	
B to Z ↓	0.0188		1.0381	
B to Z ↑	0.0248		1.5075	
C to Z ↓	0.0134		1.0141	
C to Z ↑	0.0225		1.5113	
D to Z ↓	0.0129		1.0237	
D to Z ↑	0.0185		1.5154	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P10	3.365e-06	1.000e-20
X6_P10	1.024e-05	1.000e-20
X9_P10	1.471e-05	1.000e-20
X12_P10	1.980e-05	1.000e-20
X24_P10	3.838e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P10	X6_P10	X9_P10	X12_P10
A (output stable)	1.158e-05	3.030e-05	5.943e-05	8.796e-05
B (output stable)	1.491e-05	4.190e-05	1.110e-04	1.849e-04
C (output stable)	2.302e-05	6.438e-05	1.126e-04	1.613e-04
D (output stable)	2.832e-05	8.086e-05	1.582e-04	2.423e-04
A to Z	7.765e-04	2.037e-03	3.243e-03	4.469e-03
B to Z	6.848e-04	1.784e-03	2.766e-03	3.796e-03
C to Z	4.479e-04	1.195e-03	1.961e-03	2.766e-03
D to Z	3.726e-04	9.978e-04	1.541e-03	2.113e-03
	X24_P10			
A (output stable)	1.598e-04			
B (output stable)	2.996e-04			
C (output stable)	3.124e-04			
D (output stable)	4.787e-04			

A to Z	8.617e-03			
B to Z	7.363e-03			
C to Z	5.376e-03			
D to Z	4.155e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

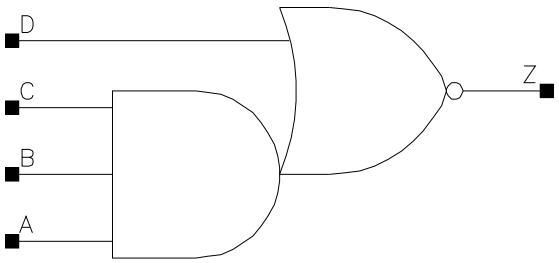
Pin Cycle (vdds)	X2_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X12_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X12_P10
A	0.0005	0.0020
B	0.0005	0.0019
C	0.0007	0.0018
D	0.0005	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X12_P10	X3_P10	X12_P10
A to Z ↓	0.0208	0.0215	10.6666	2.9480
A to Z ↑	0.0306	0.0291	12.7155	3.2838
B to Z ↓	0.0217	0.0211	10.6811	2.9530
B to Z ↑	0.0288	0.0263	12.8377	3.2805
C to Z ↓	0.0243	0.0202	10.7245	2.9605
C to Z ↑	0.0284	0.0225	12.9072	3.2965
D to Z ↓	0.0100	0.0085	4.3248	1.1742
D to Z ↑	0.0199	0.0170	10.9838	2.8133

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	4.879e-06	1.000e-20
X12_P10	1.635e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X12_P10
A (output stable)	8.555e-06	4.906e-05
B (output stable)	1.009e-05	7.921e-05
C (output stable)	2.459e-05	1.735e-04
D (output stable)	2.402e-04	8.222e-04
A to Z	1.180e-03	4.373e-03
B to Z	1.071e-03	3.694e-03
C to Z	1.000e-03	3.039e-03
D to Z	6.132e-04	1.934e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

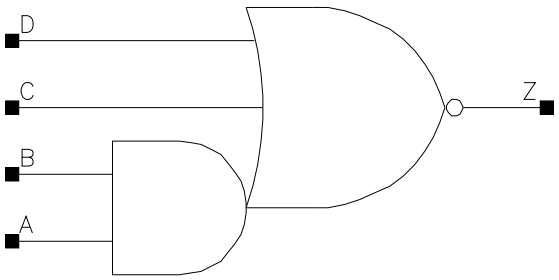
Pin Cycle (vdds)	X3_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X20_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P10	X20_P10
A	0.0005	0.0037
B	0.0005	0.0033
C	0.0005	0.0036
D	0.0005	0.0034

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X20_P10	X3_P10	X20_P10
A to Z ↓	0.0137	0.0150	7.3019	1.1662
A to Z ↑	0.0283	0.0267	18.7120	2.4065
B to Z ↓	0.0150	0.0150	7.3531	1.1762
B to Z ↑	0.0252	0.0217	18.8397	2.4084
C to Z ↓	0.0147	0.0195	4.3214	0.9053
C to Z ↑	0.0350	0.0330	17.7873	2.2745
D to Z ↓	0.0144	0.0181	4.3184	0.9031

D to Z ↑	0.0350	0.0305	17.8075	2.2782

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	4.015e-06	1.000e-20
X20_P10	2.393e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X20_P10
A (output stable)	3.044e-05	2.336e-04
B (output stable)	3.300e-05	2.636e-04
C (output stable)	2.585e-05	2.893e-04
D (output stable)	3.000e-05	3.253e-04
A to Z	7.489e-04	5.135e-03
B to Z	6.527e-04	4.025e-03
C to Z	1.180e-03	8.641e-03
D to Z	1.041e-03	6.900e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

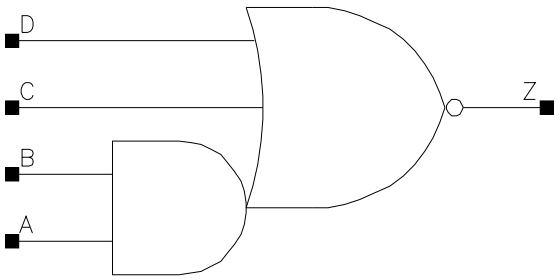
Pin Cycle (vdds)	X3_P10	X20_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.816	0.6528
X10_P10	0.800	2.448	1.9584
X19_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P10	X10_P10	X19_P10
A	0.0005	0.0020	0.0039
B	0.0005	0.0018	0.0037
C	0.0006	0.0016	0.0032
D	0.0004	0.0015	0.0029

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	X10_P10	X2_P10	X10_P10
A to Z ↓	0.0179	0.0184	8.7475	2.3135
A to Z ↑	0.0363	0.0339	19.8065	4.7943
B to Z ↓	0.0198	0.0188	8.7963	2.3261
B to Z ↑	0.0331	0.0291	19.8695	4.8079
C to Z ↓	0.0165	0.0151	7.5677	1.9085
C to Z ↑	0.0271	0.0249	18.8028	4.5454

D to Z ↓	0.0141	0.0117	7.6088	1.9236
D to Z ↑	0.0241	0.0197	18.8325	4.5594
	X19_P10		**X19_P10**	
A to Z ↓	0.0178		1.1814	
A to Z ↑	0.0328		2.4231	
B to Z ↓	0.0186		1.1888	
B to Z ↑	0.0282		2.4243	
C to Z ↓	0.0154		1.0056	
C to Z ↑	0.0238		2.2945	
D to Z ↓	0.0119		1.0139	
D to Z ↑	0.0187		2.3027	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P10	3.203e-06	1.000e-20
X10_P10	1.250e-05	1.000e-20
X19_P10	2.431e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P10	X10_P10	X19_P10
A (output stable)	1.217e-05	5.204e-05	1.010e-04
B (output stable)	1.221e-05	7.372e-05	1.386e-04
C (output stable)	2.766e-05	1.553e-04	2.999e-04
D (output stable)	5.771e-05	3.167e-04	6.019e-04
A to Z	1.126e-03	4.257e-03	8.094e-03
B to Z	1.023e-03	3.604e-03	6.893e-03
C to Z	6.894e-04	2.641e-03	4.951e-03
D to Z	5.445e-04	1.754e-03	3.253e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

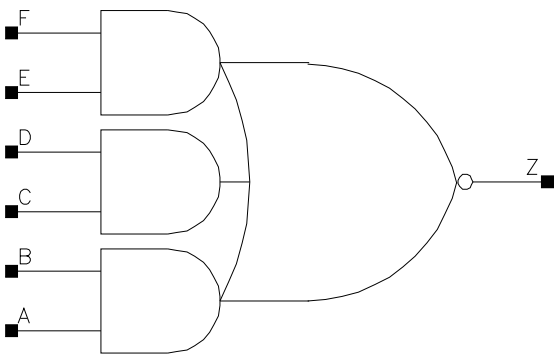
Pin Cycle (vdds)	X2_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.088	0.8704
X5_P10	0.800	2.040	1.6320
X7_P10	0.800	2.720	2.1760
X9_P10	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P10	X5_P10	X7_P10	X9_P10
A	0.0005	0.0009	0.0015	0.0020

B	0.0005	0.0010	0.0013	0.0018
C	0.0005	0.0009	0.0014	0.0021
D	0.0005	0.0010	0.0013	0.0018
E	0.0006	0.0009	0.0013	0.0017
F	0.0005	0.0008	0.0012	0.0016

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X5_P10**	**X2_P10**	**X5_P10**
A to Z ↓	0.0191	0.0233	7.7385	4.4388
A to Z ↑	0.0467	0.0434	19.1660	8.6233
B to Z ↓	0.0211	0.0258	7.7765	4.4518
B to Z ↑	0.0431	0.0412	19.2360	8.5783
C to Z ↓	0.0179	0.0211	7.8078	4.4113
C to Z ↑	0.0405	0.0383	19.2476	8.6382
D to Z ↓	0.0196	0.0232	7.8611	4.4297
D to Z ↑	0.0370	0.0364	19.2420	8.6106
E to Z ↓	0.0138	0.0164	7.8330	4.3531
E to Z ↑	0.0308	0.0303	19.2222	8.5871
F to Z ↓	0.0147	0.0175	7.9017	4.3751
F to Z ↑	0.0262	0.0268	19.1872	8.6056
	X7_P10	**X9_P10**	**X7_P10**	**X9_P10**
A to Z ↓	0.0231	0.0235	3.0642	2.3288
A to Z ↑	0.0425	0.0435	5.6814	4.2812
B to Z ↓	0.0244	0.0245	3.0739	2.3366
B to Z ↑	0.0390	0.0394	5.7702	4.3287
C to Z ↓	0.0209	0.0217	3.0755	2.3116
C to Z ↑	0.0378	0.0395	5.7593	4.3295
D to Z ↓	0.0223	0.0219	3.0905	2.3220
D to Z ↑	0.0340	0.0344	5.7253	4.3060
E to Z ↓	0.0155	0.0157	3.0699	2.3091
E to Z ↑	0.0285	0.0285	5.7101	4.3078
F to Z ↓	0.0163	0.0156	3.0931	2.3302
F to Z ↑	0.0249	0.0242	5.7457	4.3060

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P10	5.745e-06	1.000e-20
X5_P10	1.156e-05	1.000e-20
X7_P10	1.657e-05	1.000e-20
X9_P10	2.175e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

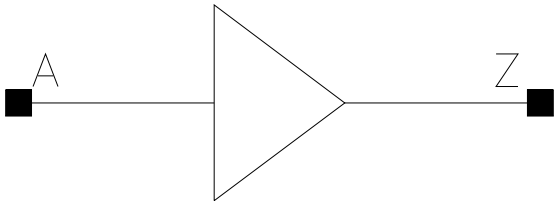
Pin Cycle (vdd)	X2_P10	X5_P10	X7_P10	X9_P10
A (output stable)	1.945e-05	3.647e-05	6.663e-05	9.287e-05
B (output stable)	2.196e-05	4.790e-05	9.286e-05	1.521e-04
C (output stable)	2.787e-05	5.697e-05	8.611e-05	1.232e-04
D (output stable)	3.253e-05	6.615e-05	1.195e-04	1.739e-04
E (output stable)	4.233e-05	9.585e-05	1.502e-04	2.115e-04
F (output stable)	5.036e-05	1.046e-04	1.779e-04	2.652e-04

A to Z	1.531e-03	3.130e-03	4.596e-03	6.271e-03
B to Z	1.413e-03	2.979e-03	4.158e-03	5.630e-03
C to Z	1.153e-03	2.427e-03	3.533e-03	4.817e-03
D to Z	1.046e-03	2.279e-03	3.144e-03	4.250e-03
E to Z	7.308e-04	1.698e-03	2.336e-03	3.102e-03
F to Z	6.330e-04	1.513e-03	1.982e-03	2.538e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X2_P10	X5_P10	X7_P10	X9_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.544	0.4352
X5_P10	0.800	0.544	0.4352
X9_P10	0.800	0.680	0.5440
X11_P10	1.600	0.408	0.6528
X13_P10	0.800	0.680	0.5440
X19_P10	0.800	0.952	0.7616
X23_P10	1.600	0.544	0.8704
X24_P10	0.800	1.088	0.8704
X29_P10	0.800	1.224	0.9792
X34_P10	1.600	0.680	1.0880
X38_P10	0.800	1.632	1.3056
X46_P10	1.600	0.952	1.5232
X57_P10	0.800	2.312	1.8496
X68_P10	1.600	1.224	1.9584
X91_P10	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P10	X5_P10	X9_P10	X11_P10
A	0.0005	0.0005	0.0005	0.0008
	X13_P10	X19_P10	X23_P10	X24_P10
A	0.0007	0.0009	0.0011	0.0011
	X29_P10	X34_P10	X38_P10	X46_P10
A	0.0013	0.0014	0.0019	0.0019
	X57_P10	X68_P10	X91_P10	
A	0.0025	0.0026	0.0035	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X5_P10**	**X2_P10**	**X5_P10**
A to Z ↓	0.0321	0.0328	8.5854	4.4479
A to Z ↑	0.0254	0.0249	13.8359	7.0987
	X9_P10	**X11_P10**	**X9_P10**	**X11_P10**
A to Z ↓	0.0393	0.0362	2.2853	1.6672
A to Z ↑	0.0293	0.0261	3.5404	3.3402
	X13_P10	**X19_P10**	**X13_P10**	**X19_P10**
A to Z ↓	0.0338	0.0342	1.5592	1.1039
A to Z ↑	0.0266	0.0253	2.4305	1.7151
	X23_P10	**X24_P10**	**X23_P10**	**X24_P10**
A to Z ↓	0.0345	0.0334	0.8084	0.8960
A to Z ↑	0.0246	0.0258	1.6767	1.3737
	X29_P10	**X34_P10**	**X29_P10**	**X34_P10**
A to Z ↓	0.0318	0.0337	0.7440	0.5547
A to Z ↑	0.0249	0.0248	1.1497	1.1391
	X38_P10	**X46_P10**	**X38_P10**	**X46_P10**
A to Z ↓	0.0312	0.0331	0.5626	0.4175
A to Z ↑	0.0247	0.0241	0.8524	0.8569
	X57_P10	**X68_P10**	**X57_P10**	**X68_P10**
A to Z ↓	0.0326	0.0324	0.3782	0.2833
A to Z ↑	0.0257	0.0239	0.5709	0.5727
	X91_P10		**X91_P10**	
A to Z ↓	0.0343		0.2183	
A to Z ↑	0.0251		0.4309	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P10	3.027e-06	1.000e-20
X5_P10	4.925e-06	1.000e-20
X9_P10	8.072e-06	1.000e-20
X11_P10	1.069e-05	1.000e-20
X13_P10	1.226e-05	1.000e-20
X19_P10	1.606e-05	1.000e-20
X23_P10	2.061e-05	1.000e-20
X24_P10	2.004e-05	1.000e-20
X29_P10	2.430e-05	1.000e-20
X34_P10	2.943e-05	1.000e-20
X38_P10	3.287e-05	1.000e-20
X46_P10	3.781e-05	1.000e-20
X57_P10	4.714e-05	1.000e-20
X68_P10	5.573e-05	1.000e-20
X91_P10	7.159e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P10	X5_P10	X9_P10	X11_P10
A to Z	8.493e-04	1.099e-03	1.756e-03	2.125e-03
	X13_P10	X19_P10	X23_P10	X24_P10
A to Z	2.513e-03	3.388e-03	3.826e-03	4.227e-03
	X29_P10	X34_P10	X38_P10	X46_P10

A to Z	4.883e-03	5.760e-03	6.732e-03	7.394e-03
	X57_P10	X68_P10	X91_P10	
A to Z	9.925e-03	1.076e-02	1.464e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

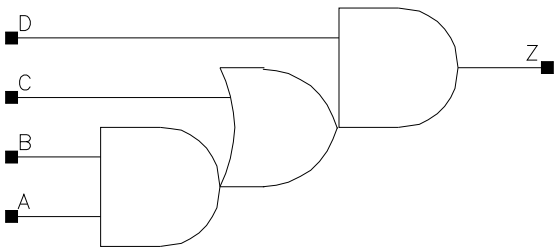
Pin Cycle (vdds)	X2_P10	X5_P10	X9_P10	X11_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P10	X19_P10	X23_P10	X24_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P10	X34_P10	X38_P10	X46_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P10	X68_P10	X91_P10	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.952	0.7616
X10_P10	0.800	1.632	1.3056
X14_P10	0.800	1.768	1.4144
X19_P10	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0006	0.0012	0.0012	0.0012
B	0.0006	0.0011	0.0011	0.0011
C	0.0006	0.0014	0.0014	0.0013
D	0.0009	0.0012	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0432	0.0394	4.5491	2.1518
A to Z ↑	0.0400	0.0361	7.2513	3.4493
B to Z ↓	0.0405	0.0363	4.5360	2.1455
B to Z ↑	0.0408	0.0363	7.2457	3.4481
C to Z ↓	0.0364	0.0325	4.5299	2.1424
C to Z ↑	0.0298	0.0262	7.1882	3.4117

D to Z ↓	0.0355	0.0301	4.4943	2.1272
D to Z ↑	0.0350	0.0292	7.1987	3.4168
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0435	0.0470	1.4929	1.1243
A to Z ↑	0.0398	0.0430	2.3132	1.7374
B to Z ↓	0.0406	0.0443	1.4916	1.1236
B to Z ↑	0.0402	0.0434	2.3150	1.7388
C to Z ↓	0.0365	0.0401	1.4865	1.1187
C to Z ↑	0.0292	0.0317	2.2861	1.7157
D to Z ↓	0.0327	0.0348	1.4687	1.1021
D to Z ↑	0.0320	0.0343	2.2909	1.7191

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	7.594e-06	1.000e-20
X10_P10	1.505e-05	1.000e-20
X14_P10	1.798e-05	1.000e-20
X19_P10	2.093e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	3.303e-05	6.285e-05	6.408e-05	6.431e-05
B (output stable)	4.600e-05	8.599e-05	8.763e-05	8.751e-05
C (output stable)	1.476e-04	2.395e-04	2.400e-04	2.399e-04
D (output stable)	5.120e-05	7.698e-05	7.785e-05	7.814e-05
A to Z	1.847e-03	3.338e-03	4.228e-03	5.084e-03
B to Z	1.741e-03	3.079e-03	3.965e-03	4.816e-03
C to Z	1.463e-03	2.515e-03	3.342e-03	4.140e-03
D to Z	1.886e-03	3.252e-03	4.058e-03	4.800e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

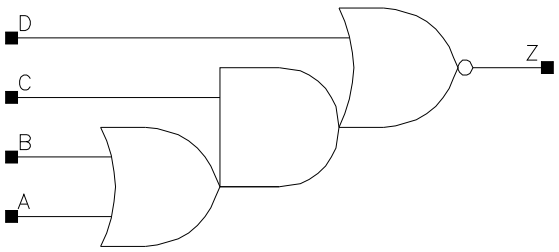
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X6_P10	0.800	1.496	1.1968
X9_P10	0.800	1.768	1.4144
X12_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X9_P10	X12_P10
A	0.0005	0.0010	0.0016	0.0020
B	0.0005	0.0010	0.0015	0.0020
C	0.0005	0.0010	0.0014	0.0019
D	0.0007	0.0009	0.0014	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0185	0.0170	7.5695	3.8588
A to Z ↑	0.0380	0.0371	18.7620	9.7365
B to Z ↓	0.0177	0.0168	7.3983	3.8793
B to Z ↑	0.0374	0.0354	18.7697	9.7456
C to Z ↓	0.0165	0.0154	6.9714	3.5990
C to Z ↑	0.0242	0.0228	12.9232	6.6284

D to Z ↓	0.0103	0.0083	4.3505	2.2156
D to Z ↑	0.0221	0.0185	13.7381	7.0609
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0171	0.0174	2.6585	2.0475
A to Z ↑	0.0345	0.0364	6.3376	4.8490
B to Z ↓	0.0164	0.0167	2.6734	2.0435
B to Z ↑	0.0341	0.0347	6.3435	4.8528
C to Z ↓	0.0156	0.0156	2.4903	1.9041
C to Z ↑	0.0220	0.0222	4.3400	3.2906
D to Z ↓	0.0084	0.0083	1.5426	1.1786
D to Z ↑	0.0174	0.0171	4.6156	3.5089

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	4.798e-06	1.000e-20
X6_P10	9.176e-06	1.000e-20
X9_P10	1.255e-05	1.000e-20
X12_P10	1.668e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	9.836e-06	2.431e-05	2.951e-05	5.053e-05
B (output stable)	1.001e-05	2.346e-05	3.119e-05	5.325e-05
C (output stable)	3.880e-05	8.591e-05	1.160e-04	1.575e-04
D (output stable)	1.208e-04	2.932e-04	4.145e-04	5.915e-04
A to Z	1.226e-03	2.325e-03	3.225e-03	4.502e-03
B to Z	1.074e-03	1.928e-03	2.784e-03	3.745e-03
C to Z	8.686e-04	1.575e-03	2.259e-03	3.073e-03
D to Z	5.784e-04	9.424e-04	1.306e-03	1.710e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

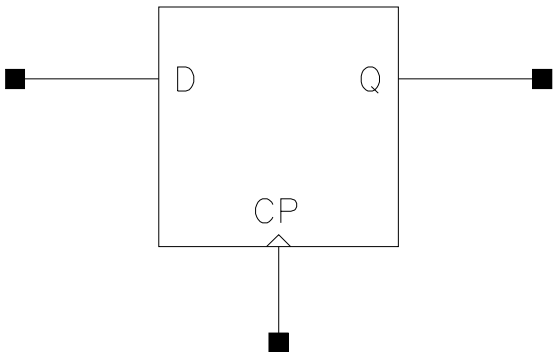
Pin Cycle (vdds)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	1.600	1.496	2.3936
X19_P10	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P10	X19_P10
CP	0.0008	0.0008
D	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P10	X19_P10	X10_P10	X19_P10
CP to Q ↓	0.0653	0.0887	2.2466	1.2218
CP to Q ↑	0.0760	0.0871	3.4232	1.7548

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P10	X19_P10
CP ↓	min_pulse_width to CP	0.0664	0.0664
CP ↑	min_pulse_width to CP	0.0547	0.0784
D ↓	hold_rising to CP	0.0124	0.0124
D ↑	hold_rising to CP	0.0049	0.0049
D ↓	setup_rising to CP	0.0343	0.0343
D ↑	setup_rising to CP	0.0222	0.0222

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P10	2.343e-05	1.000e-20
X19_P10	2.921e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

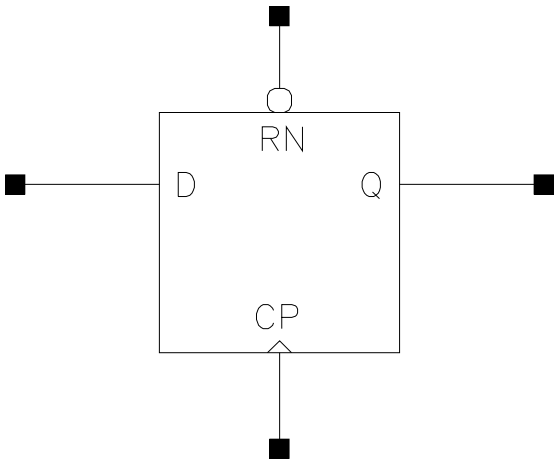
Pin Cycle	X10_P10	X19_P10
Clock 100Mhz Data 0Mhz	5.957e-03	5.962e-03
Clock 100Mhz Data 25Mhz	7.175e-03	8.500e-03
Clock 100Mhz Data 50Mhz	8.394e-03	1.104e-02
Clock = 0 Data 100Mhz	2.373e-03	2.373e-03
Clock = 1 Data 100Mhz	1.389e-05	1.397e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	1.600	1.768	2.8288
X19_P10	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P10	X19_P10
CP	0.0008	0.0008
D	0.0006	0.0006
RN	0.0008	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P10	X19_P10	X10_P10	X19_P10
CP to Q ↓	0.0714	0.0924	2.2834	1.2085
CP to Q ↑	0.0794	0.0902	3.4151	1.7422
RN to Q ↓	0.0740	0.0961	2.2459	1.1675

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P10	X19_P10
CP ↓	min_pulse_width to CP	0.0664	0.0664
CP ↑	min_pulse_width to CP	0.0580	0.0784
D ↓	hold_rising to CP	0.0118	0.0118
D ↑	hold_rising to CP	0.0053	0.0053
D ↓	setup_rising to CP	0.0321	0.0321
D ↑	setup_rising to CP	0.0249	0.0249
RN ↓	min_pulse_width to RN	0.0876	0.1121
RN ↑	recovery_rising to CP	0.0157	0.0157
RN ↑	removal_rising to CP	-0.0055	-0.0055

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P10	2.619e-05	1.000e-20
X19_P10	3.280e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

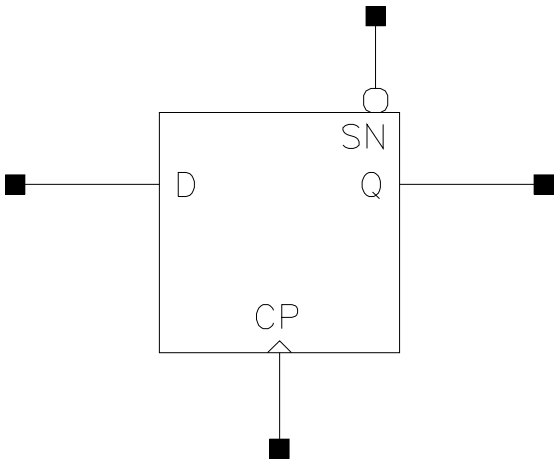
Pin Cycle	X10_P10	X19_P10
Clock 100Mhz Data 0Mhz	6.022e-03	6.024e-03
Clock 100Mhz Data 25Mhz	7.358e-03	8.683e-03
Clock 100Mhz Data 50Mhz	8.695e-03	1.134e-02
Clock = 0 Data 100Mhz	2.387e-03	2.387e-03
Clock = 1 Data 100Mhz	1.400e-05	1.411e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	1.600	1.768	2.8288
X19_P10	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P10	X19_P10
CP	0.0008	0.0008
D	0.0006	0.0006
SN	0.0010	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P10	X19_P10	X10_P10	X19_P10
CP to Q ↓	0.0673	0.0902	2.2633	1.2006
CP to Q ↑	0.0787	0.0905	3.4112	1.7452
SN to Q ↑	0.0473	0.0538	3.3522	1.6974

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P10	X19_P10
CP ↓	min_pulse_width to CP	0.0712	0.0712
CP ↑	min_pulse_width to CP	0.0546	0.0784
D ↓	hold_rising to CP	0.0124	0.0124
D ↑	hold_rising to CP	0.0049	0.0049
D ↓	setup_rising to CP	0.0343	0.0343
D ↑	setup_rising to CP	0.0196	0.0196
SN ↓	min_pulse_width to SN	0.0518	0.0544
SN ↑	recovery_rising to CP	0.0058	0.0054
SN ↑	removal_rising to CP	0.0410	0.0410

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P10	2.726e-05	1.000e-20
X19_P10	3.390e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

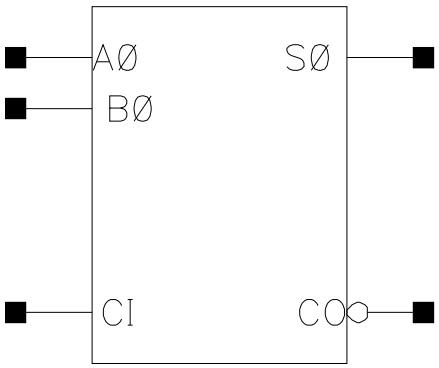
Pin Cycle	X10_P10	X19_P10
Clock 100Mhz Data 0Mhz	5.911e-03	5.913e-03
Clock 100Mhz Data 25Mhz	7.184e-03	8.562e-03
Clock 100Mhz Data 50Mhz	8.458e-03	1.121e-02
Clock = 0 Data 100Mhz	2.288e-03	2.289e-03
Clock = 1 Data 100Mhz	1.399e-05	1.409e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_-P10	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_-P10	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_-P10	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_-P10	1.600	2.720	4.3520
C8T28SOIDV_LLS1_-FA1X4_P10	1.600	2.040	3.2640
C8T28SOIDV_LLS1_-FA1X9_P10	1.600	3.128	5.0048
C8T28SOIDV_LLS1_-FA1X18_P10	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P10	C8T28SOIDV_LL_-FA1X9_P10	C8T28SOIDV_LL_-FA1X14_P10	C8T28SOIDV_LL_-FA1X19_P10
A0	0.0022	0.0023	0.0036	0.0038
B0	0.0018	0.0019	0.0033	0.0035
CI	0.0014	0.0014	0.0024	0.0027
	C8T28SOIDV_LLS1_-FA1X4_P10	C8T28SOIDV_LLS1_-FA1X9_P10	C8T28SOIDV_LLS1_-FA1X18_P10	
A0	0.0021	0.0028	0.0029	
B0	0.0020	0.0032	0.0035	
CI	0.0015	0.0022	0.0026	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P10	**C8T28SOIDV_LL_-FA1X9_P10**	**C8T28SOIDV_LL_-FA1X5_P10**	**C8T28SOIDV_LL_-FA1X9_P10**
A0 to CO ↓	0.0571	0.0607	4.6411	2.3915
A0 to CO ↑	0.0423	0.0447	6.7788	3.4581
A0 to S0 ↓	0.0622	0.0674	4.5810	2.3595
A0 to S0 ↑	0.0643	0.0688	6.7635	3.3984
B0 to CO ↓	0.0570	0.0607	4.6620	2.4011
B0 to CO ↑	0.0436	0.0459	6.7799	3.4602
B0 to S0 ↓	0.0625	0.0680	4.5804	2.3600
B0 to S0 ↑	0.0648	0.0697	6.7657	3.4004
CI to CO ↓	0.0534	0.0566	4.6594	2.3999
CI to CO ↑	0.0424	0.0444	6.7755	3.4546
CI to S0 ↓	0.0619	0.0673	4.5826	2.3595
CI to S0 ↑	0.0641	0.0687	6.7640	3.3997
	C8T28SOIDV_LL_-FA1X14_P10	**C8T28SOIDV_LL_-FA1X19_P10**	**C8T28SOIDV_LL_-FA1X14_P10**	**C8T28SOIDV_LL_-FA1X19_P10**
A0 to CO ↓	0.0579	0.0635	1.5463	1.1800
A0 to CO ↑	0.0428	0.0442	2.3545	1.7617
A0 to S0 ↓	0.0713	0.0717	1.5400	1.1460
A0 to S0 ↑	0.0732	0.0752	2.2925	1.7119
B0 to CO ↓	0.0567	0.0622	1.5515	1.1836
B0 to CO ↑	0.0432	0.0445	2.3535	1.7611
B0 to S0 ↓	0.0715	0.0719	1.5401	1.1463
B0 to S0 ↑	0.0733	0.0753	2.2938	1.7126
CI to CO ↓	0.0532	0.0585	1.5485	1.1813
CI to CO ↑	0.0418	0.0433	2.3531	1.7612
CI to S0 ↓	0.0704	0.0709	1.5398	1.1464
CI to S0 ↑	0.0718	0.0740	2.2934	1.7125
	C8T28SOIDV_-LLS1_FA1X4_P10	**C8T28SOIDV_-LLS1_FA1X9_P10**	**C8T28SOIDV_-LLS1_FA1X4_P10**	**C8T28SOIDV_-LLS1_FA1X9_P10**
A0 to CO ↓	0.0374	0.0346	8.9867	2.9036
A0 to CO ↑	0.0330	0.0317	6.8031	3.4514
A0 to S0 ↓	0.0824	0.0902	4.9125	1.7467
A0 to S0 ↑	0.0774	0.0768	7.1860	3.3854
B0 to CO ↓	0.0355	0.0354	8.9751	2.9054
B0 to CO ↑	0.0288	0.0301	6.7868	3.4487
B0 to S0 ↓	0.0839	0.0939	4.9102	1.7463
B0 to S0 ↑	0.0791	0.0806	7.1776	3.3857
CI to CO ↓	0.0360	0.0491	8.9787	2.9280
CI to CO ↑	0.0315	0.0296	6.8064	3.4710

CI to S0 ↓	0.0458	0.0546	4.9138	1.7481
CI to S0 ↑	0.0407	0.0410	7.1851	3.3848
	C8T28SOIDV_-LLS1_FA1X18_P10		**C8T28SOIDV_-LLS1_FA1X18_P10**	
A0 to CO ↓	0.0439		1.5094	
A0 to CO ↑	0.0331		1.6958	
A0 to S0 ↓	0.0953		0.9036	
A0 to S0 ↑	0.0772		1.6958	
B0 to CO ↓	0.0453		1.5108	
B0 to CO ↑	0.0316		1.6941	
B0 to S0 ↓	0.0973		0.9036	
B0 to S0 ↑	0.0793		1.6963	
CI to CO ↓	0.0616		1.5253	
CI to CO ↑	0.0345		1.6987	
CI to S0 ↓	0.0562		0.9036	
CI to S0 ↑	0.0375		1.6951	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P10	1.794e-05	1.000e-20
C8T28SOIDV_LL_FA1X9_P10	2.514e-05	1.000e-20
C8T28SOIDV_LL_FA1X14_P10	3.754e-05	1.000e-20
C8T28SOIDV_LL_FA1X19_P10	4.674e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P10	3.886e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P10	5.888e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P10	8.873e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P10	C8T28SOIDV_LL_-FA1X9_P10	C8T28SOIDV_LL_-FA1X14_P10	C8T28SOIDV_LL_-FA1X19_P10
A0 to CO	2.040e-03	2.828e-03	4.695e-03	5.681e-03
A0 to S0	2.087e-03	2.770e-03	4.791e-03	5.799e-03
B0 to CO	2.059e-03	2.865e-03	4.721e-03	5.737e-03
B0 to S0	2.059e-03	2.762e-03	4.760e-03	5.768e-03
CI to CO	2.056e-03	2.836e-03	4.746e-03	5.803e-03
CI to S0	2.048e-03	2.747e-03	4.733e-03	5.736e-03
	C8T28SOIDV_LLS1_-FA1X4_P10	C8T28SOIDV_LLS1_-FA1X9_P10	C8T28SOIDV_LLS1_-FA1X18_P10	
A0 to CO	3.165e-03	4.840e-03	7.685e-03	
A0 to S0	4.291e-03	6.265e-03	9.603e-03	
B0 to CO	3.362e-03	4.926e-03	7.743e-03	
B0 to S0	4.633e-03	6.449e-03	9.759e-03	
CI to CO	2.255e-03	3.989e-03	6.691e-03	
CI to S0	2.544e-03	4.436e-03	7.250e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P10	C8T28SOIDV_LL_-FA1X9_P10	C8T28SOIDV_LL_-FA1X14_P10	C8T28SOIDV_LL_-FA1X19_P10
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P10	C8T28SOIDV_LLS1_-FA1X9_P10	C8T28SOIDV_LLS1_-FA1X18_P10	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P10	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P10	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P10	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P10	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P10	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P10	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P10	C8T28SOI_LL_-HA1X9_P10	C8T28SOI_LLS1_-HA1X5_P10	C8T28SOIDV_LL_-HA1X14_P10
A0	0.0007	0.0010	0.0012	0.0014
B0	0.0007	0.0011	0.0012	0.0013
	C8T28SOIDV_LL_-HA1X19_P10	C8T28SOIDV_LLS1_-HA1X11_P10		
A0	0.0018	0.0018		
B0	0.0016	0.0018		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P10	**C8T28SOI_LL_-HA1X9_P10**	**C8T28SOI_LL_-HA1X5_P10**	**C8T28SOI_LL_-HA1X9_P10**
A0 to CO ↓	0.0444	0.0371	4.5916	2.2498
A0 to CO ↑	0.0416	0.0352	7.2261	3.4654
A0 to S0 ↓	0.0589	0.0519	4.4103	2.2284
A0 to S0 ↑	0.0543	0.0484	7.0533	3.4467
B0 to CO ↓	0.0434	0.0363	4.5996	2.2515
B0 to CO ↑	0.0438	0.0378	7.2261	3.4664
B0 to S0 ↓	0.0602	0.0524	4.4094	2.2304
B0 to S0 ↑	0.0538	0.0478	7.0557	3.4479
	C8T28SOI_LLS1_-HA1X5_P10	**C8T28SOIDV_LL_-HA1X14_P10**	**C8T28SOI_LLS1_-HA1X5_P10**	**C8T28SOIDV_LL_-HA1X14_P10**
A0 to CO ↓	0.0355	0.0385	4.4921	1.5207
A0 to CO ↑	0.0331	0.0351	7.1364	2.3195
A0 to S0 ↓	0.0507	0.0581	4.4821	1.5248
A0 to S0 ↑	0.0558	0.0536	7.1803	2.2947
B0 to CO ↓	0.0338	0.0359	4.4952	1.5141
B0 to CO ↑	0.0346	0.0356	7.1364	2.3197
B0 to S0 ↓	0.0526	0.0567	4.4814	1.5264
B0 to S0 ↑	0.0554	0.0514	7.1801	2.2948
	C8T28SOIDV_LL_-HA1X19_P10	**C8T28SOIDV_-LLS1_HA1X11_P10**	**C8T28SOIDV_LL_-HA1X19_P10**	**C8T28SOIDV_-LLS1_HA1X11_P10**
A0 to CO ↓	0.0352	0.0337	1.1107	1.5745
A0 to CO ↑	0.0331	0.0347	1.7492	3.4118
A0 to S0 ↓	0.0526	0.0440	1.1028	1.6013
A0 to S0 ↑	0.0490	0.0458	1.7219	3.4351
B0 to CO ↓	0.0329	0.0321	1.1065	1.5717
B0 to CO ↑	0.0338	0.0368	1.7493	3.4123
B0 to S0 ↓	0.0520	0.0459	1.1028	1.5992
B0 to S0 ↑	0.0471	0.0457	1.7219	3.4349

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_HA1X5_P10	1.039e-05	1.000e-20
C8T28SOI_LL_HA1X9_P10	2.224e-05	1.000e-20
C8T28SOI_LLS1_HA1X5_P10	1.275e-05	1.000e-20
C8T28SOIDV_LL_HA1X14_P10	3.159e-05	1.000e-20
C8T28SOIDV_LL_HA1X19_P10	4.381e-05	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P10	3.081e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

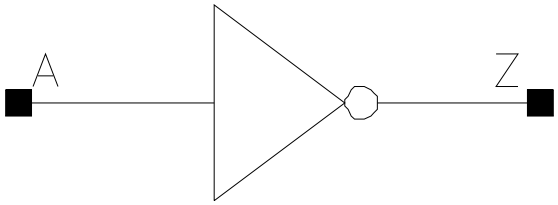
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P10	C8T28SOI_LL_-HA1X9_P10	C8T28SOI_LLS1_-HA1X5_P10	C8T28SOIDV_LL_-HA1X14_P10
A0 to CO	1.545e-03	2.477e-03	1.858e-03	4.016e-03
A0 to S0	1.392e-03	2.375e-03	1.640e-03	4.037e-03
B0 to CO	1.564e-03	2.579e-03	1.890e-03	4.016e-03
B0 to S0	1.370e-03	2.323e-03	1.599e-03	3.908e-03
	C8T28SOIDV_LL_-HA1X19_P10	C8T28SOIDV_LLS1_-HA1X11_P10		
A0 to CO	4.804e-03	3.531e-03		
A0 to S0	4.830e-03	3.185e-03		

B0 to CO	4.801e-03	3.243e-03		
B0 to S0	4.690e-03	3.270e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P10	C8T28SOI_LL_-HA1X9_P10	C8T28SOI_LLS1_-HA1X5_P10	C8T28SOIDV_LL_-HA1X14_P10
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P10	C8T28SOIDV_LLS1_-HA1X11_P10		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P10	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P10	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P10	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P10	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P10	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P10	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P10	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P10	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P10	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P10	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P10	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P10	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P10	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P10	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P10	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P10	C8T28SOI_LL_IVX3_-P10	C8T28SOI_LL_IVX5_-P10	C8T28SOI_LL_-IVX10_P10

A	0.0004	0.0004	0.0005	0.0010
	C8T28SOI_LL_-IVX14_P10	C8T28SOI_LL_-IVX19_P10	C8T28SOI_LL_-IVX29_P10	C8T28SOI_LL_-IVX34_P10
A	0.0015	0.0019	0.0028	0.0032
	C8T28SOI_LL_-IVX38_P10	C8T28SOIDV_LL_-IVX11_P10	C8T28SOIDV_LL_-IVX23_P10	C8T28SOIDV_LL_-IVX34_P10
A	0.0037	0.0011	0.0021	0.0030
	C8T28SOIDV_LL_-IVX46_P10	C8T28SOIDV_LL_-IVX68_P10	C8T28SOIDV_LL_-IVX91_P10	
A	0.0040	0.0061	0.0084	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P10	**C8T28SOI_LL_-IVX3_P10**	**C8T28SOI_LL_-IVX2_P10**	**C8T28SOI_LL_-IVX3_P10**
A to Z ↓	0.0097	0.0092	8.7390	6.6724
A to Z ↑	0.0166	0.0150	14.0265	10.4784
	C8T28SOI_LL_-IVX5_P10	**C8T28SOI_LL_-IVX10_P10**	**C8T28SOI_LL_-IVX5_P10**	**C8T28SOI_LL_-IVX10_P10**
A to Z ↓	0.0083	0.0066	4.5237	2.1643
A to Z ↑	0.0132	0.0109	7.2238	3.4348
	C8T28SOI_LL_-IVX14_P10	**C8T28SOI_LL_-IVX19_P10**	**C8T28SOI_LL_-IVX14_P10**	**C8T28SOI_LL_-IVX19_P10**
A to Z ↓	0.0068	0.0072	1.4969	1.1408
A to Z ↑	0.0110	0.0113	2.3049	1.7580
	C8T28SOI_LL_-IVX29_P10	**C8T28SOI_LL_-IVX34_P10**	**C8T28SOI_LL_-IVX29_P10**	**C8T28SOI_LL_-IVX34_P10**
A to Z ↓	0.0071	0.0067	0.7657	0.6538
A to Z ↑	0.0109	0.0105	1.1662	0.9969
	C8T28SOI_LL_-IVX38_P10	**C8T28SOIDV_LL_-IVX11_P10**	**C8T28SOI_LL_-IVX38_P10**	**C8T28SOIDV_LL_-IVX11_P10**
A to Z ↓	0.0069	0.0066	0.5781	1.6848
A to Z ↑	0.0107	0.0127	0.8808	3.4959
	C8T28SOIDV_LL_-IVX23_P10	**C8T28SOIDV_LL_-IVX34_P10**	**C8T28SOIDV_LL_-IVX23_P10**	**C8T28SOIDV_LL_-IVX34_P10**
A to Z ↓	0.0055	0.0060	0.8207	0.5619
A to Z ↑	0.0112	0.0114	1.7038	1.1402
	C8T28SOIDV_LL_-IVX46_P10	**C8T28SOIDV_LL_-IVX68_P10**	**C8T28SOIDV_LL_-IVX46_P10**	**C8T28SOIDV_LL_-IVX68_P10**
A to Z ↓	0.0057	0.0057	0.4238	0.2881
A to Z ↑	0.0108	0.0108	0.8556	0.5732
	C8T28SOIDV_LL_-IVX91_P10		**C8T28SOIDV_LL_-IVX91_P10**	
A to Z ↓	0.0062		0.2220	
A to Z ↑	0.0111		0.4341	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_IVX2_P10	1.603e-06	1.000e-20
C8T28SOI_LL_IVX3_P10	2.201e-06	1.000e-20
C8T28SOI_LL_IVX5_P10	3.333e-06	1.000e-20
C8T28SOI_LL_IVX10_P10	6.907e-06	1.000e-20

C8T28SOI_LL_IVX14_P10	9.828e-06	1.000e-20
C8T28SOI_LL_IVX19_P10	1.268e-05	1.000e-20
C8T28SOI_LL_IVX29_P10	1.838e-05	1.000e-20
C8T28SOI_LL_IVX34_P10	2.123e-05	1.000e-20
C8T28SOI_LL_IVX38_P10	2.409e-05	1.000e-20
C8T28SOIDV_LL_IVX11_P10	8.123e-06	1.000e-20
C8T28SOIDV_LL_IVX23_P10	1.610e-05	1.000e-20
C8T28SOIDV_LL_IVX34_P10	2.297e-05	1.000e-20
C8T28SOIDV_LL_IVX46_P10	2.965e-05	1.000e-20
C8T28SOIDV_LL_IVX68_P10	4.298e-05	1.000e-20
C8T28SOIDV_LL_IVX91_P10	5.633e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P10	C8T28SOI_LL_IVX3_-P10	C8T28SOI_LL_IVX5_-P10	C8T28SOI_LL_-IVX10_P10
A to Z	2.538e-04	3.047e-04	3.747e-04	6.461e-04
	C8T28SOI_LL_-IVX14_P10	C8T28SOI_LL_-IVX19_P10	C8T28SOI_LL_-IVX29_P10	C8T28SOI_LL_-IVX34_P10
A to Z	1.004e-03	1.384e-03	1.986e-03	2.196e-03
	C8T28SOI_LL_-IVX38_P10	C8T28SOIDV_LL_-IVX11_P10	C8T28SOIDV_LL_-IVX23_P10	C8T28SOIDV_LL_-IVX34_P10
A to Z	2.573e-03	8.051e-04	1.398e-03	2.171e-03
	C8T28SOIDV_LL_-IVX46_P10	C8T28SOIDV_LL_-IVX68_P10	C8T28SOIDV_LL_-IVX91_P10	
A to Z	2.652e-03	3.966e-03	5.297e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

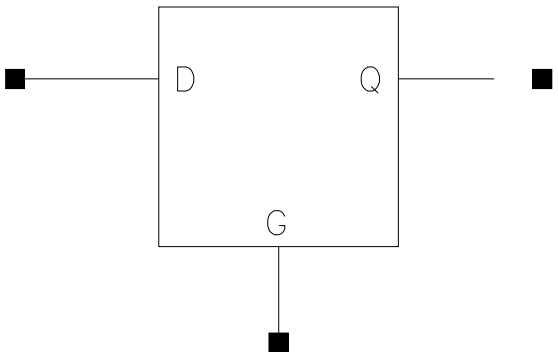
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P10	C8T28SOI_LL_IVX3_-P10	C8T28SOI_LL_IVX5_-P10	C8T28SOI_LL_-IVX10_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P10	C8T28SOI_LL_-IVX19_P10	C8T28SOI_LL_-IVX29_P10	C8T28SOI_LL_-IVX34_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P10	C8T28SOIDV_LL_-IVX11_P10	C8T28SOIDV_LL_-IVX23_P10	C8T28SOIDV_LL_-IVX34_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P10	C8T28SOIDV_LL_-IVX68_P10	C8T28SOIDV_LL_-IVX91_P10	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.360	1.0880
X9_P10	1.600	0.952	1.5232
X19_P10	1.600	1.224	1.9584
X28_P10	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10	X28_P10
D	0.0004	0.0006	0.0009	0.0015
G	0.0008	0.0008	0.0017	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D to Q ↓	0.0655	0.0612	4.6905	2.3288
D to Q ↑	0.0362	0.0429	6.9608	3.4167
G to Q ↓	0.0716	0.0651	4.6832	2.3263

G to Q ↑	0.0351	0.0395	6.9649	3.4223
	X19_P10	**X28_P10**	**X19_P10**	**X28_P10**
D to Q ↓	0.0495	0.0524	1.1175	0.7525
D to Q ↑	0.0360	0.0364	1.7163	1.1508
G to Q ↓	0.0562	0.0509	1.1163	0.7520
G to Q ↑	0.0332	0.0334	1.7191	1.1499

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P10	X9_P10	X19_P10	X28_P10
D ↓	hold_falling to G	-0.0192	-0.0165	-0.0040	-0.0088
D ↑	hold_falling to G	-0.0003	-0.0052	0.0003	-0.0030
D ↓	setup_falling to G	0.0585	0.0564	0.0414	0.0431
D ↑	setup_falling to G	0.0383	0.0448	0.0399	0.0399
G ↑	min_pulse_width to G	0.0565	0.0517	0.0456	0.0443

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	8.920e-06	1.000e-20
X9_P10	1.405e-05	1.000e-20
X19_P10	2.387e-05	1.000e-20
X28_P10	3.213e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	6.877e-06	1.956e-05	2.219e-05	6.229e-05
G (output stable)	6.142e-04	7.266e-04	1.200e-03	1.117e-03
D to Q	2.313e-03	3.661e-03	5.436e-03	7.980e-03
G to Q	2.165e-03	3.410e-03	4.978e-03	6.842e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

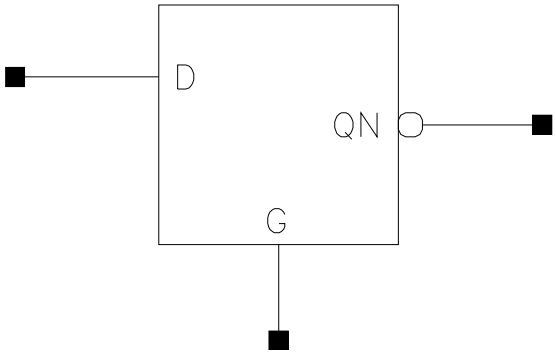
Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P10
D	0.0004
G	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P10	X10_P10
D to QN ↓	0.0575	2.1568
D to QN ↑	0.0774	3.4005
G to QN ↓	0.0561	2.1559
G to QN ↑	0.0826	3.3974

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X10_P10
D ↓	hold_falling to G	-0.0289
D ↑	hold_falling to G	-0.0105
D ↓	setup_falling to G	0.0537
D ↑	setup_falling to G	0.0383
G ↑	min_pulse_width to G	0.0517

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X10_P10	1.310e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X10_P10
D (output stable)	6.778e-06
G (output stable)	6.486e-04
D to QN	3.083e-03
G to QN	2.883e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

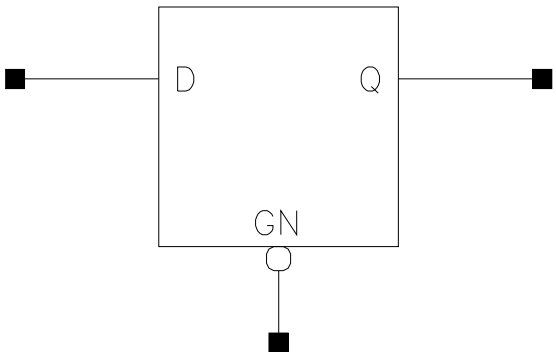
Pin Cycle (vdds)	X10_P10
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.360	1.0880
X9_P10	1.600	0.952	1.5232
X19_P10	1.600	1.224	1.9584
X28_P10	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10	X28_P10
D	0.0004	0.0006	0.0009	0.0013
GN	0.0008	0.0009	0.0013	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D to Q ↓	0.0661	0.0601	4.7006	2.3354
D to Q ↑	0.0365	0.0425	6.9512	3.4244
GN to Q ↓	0.0586	0.0561	4.7003	2.3346

GN to Q ↑	0.0643	0.0605	6.9531	3.4168
	X19_P10	**X28_P10**	**X19_P10**	**X28_P10**
D to Q ↓	0.0501	0.0502	1.1153	0.7511
D to Q ↑	0.0379	0.0373	1.7102	1.1423
GN to Q ↓	0.0440	0.0423	1.1173	0.7512
GN to Q ↑	0.0532	0.0530	1.7064	1.1406

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P10	X9_P10	X19_P10	X28_P10
D ↓	hold_rising to GN	-0.0211	-0.0198	-0.0117	-0.0123
D ↑	hold_rising to GN	0.0026	-0.0022	0.0036	0.0032
D ↓	setup_rising to GN	0.0714	0.0618	0.0569	0.0548
D ↑	setup_rising to GN	0.0320	0.0394	0.0368	0.0313
GN ↓	min_pulse_width to GN	0.0723	0.0681	0.0594	0.0563

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	8.415e-06	1.000e-20
X9_P10	1.364e-05	1.000e-20
X19_P10	2.400e-05	1.000e-20
X28_P10	3.150e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	6.764e-06	1.120e-05	2.187e-05	5.245e-05
GN (output stable)	6.154e-04	7.178e-04	1.029e-03	1.121e-03
D to Q	2.313e-03	3.667e-03	5.615e-03	7.820e-03
GN to Q	3.486e-03	4.945e-03	7.219e-03	9.269e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

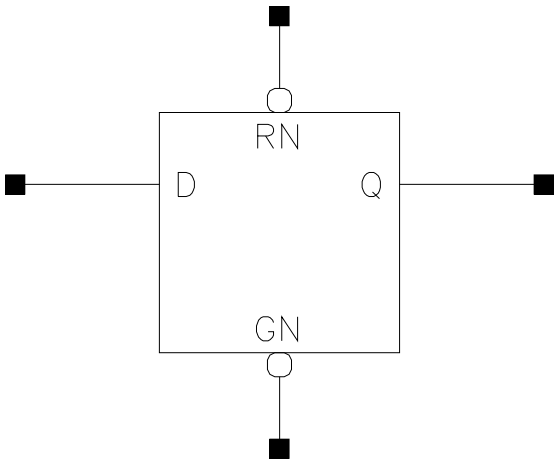
Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.632	1.3056
X9_P10	1.600	1.224	1.9584
X19_P10	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10
D	0.0004	0.0006	0.0011
GN	0.0010	0.0010	0.0014
RN	0.0004	0.0005	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D to Q ↓	0.0675	0.0635	4.6132	2.2833

D to Q ↑	0.0606	0.0668	7.2294	3.5457
GN to Q ↓	0.0615	0.0581	4.6092	2.2837
GN to Q ↑	0.0846	0.0797	7.2279	3.5569
RN to Q ↓	0.0535	0.0681	4.4253	2.2864
RN to Q ↑	0.0670	0.0719	7.2316	3.5470
	X19_P10		**X19_P10**	
D to Q ↓	0.0524		1.1245	
D to Q ↑	0.0711		1.7914	
GN to Q ↓	0.0468		1.1246	
GN to Q ↑	0.0754		1.7967	
RN to Q ↓	0.0879		1.2157	
RN to Q ↑	0.0772		1.7935	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P10	X9_P10	X19_P10
D ↓	hold_rising to GN	-0.0211	-0.0220	-0.0149
D ↑	hold_rising to GN	-0.0169	-0.0212	-0.0289
D ↓	setup_rising to GN	0.0764	0.0663	0.0570
D ↑	setup_rising to GN	0.0611	0.0654	0.0783
GN ↓	min_pulse_width to GN	0.0804	0.0808	0.0810
RN ↓	min_pulse_width to RN	0.0637	0.0779	0.0974
RN ↑	recovery_rising to GN	0.0688	0.0758	0.0881
RN ↑	removal_rising to GN	-0.0412	-0.0515	-0.0586

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	8.168e-06	1.000e-20
X9_P10	1.268e-05	1.000e-20
X19_P10	2.165e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10
D (output stable)	4.779e-05	4.294e-05	6.316e-05
GN (output stable)	6.892e-04	7.068e-04	8.821e-04
RN (output stable)	2.400e-05	3.240e-05	4.271e-05
D to Q	2.903e-03	4.123e-03	6.297e-03
GN to Q	4.169e-03	5.345e-03	7.731e-03
RN to Q	2.217e-03	3.170e-03	5.062e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

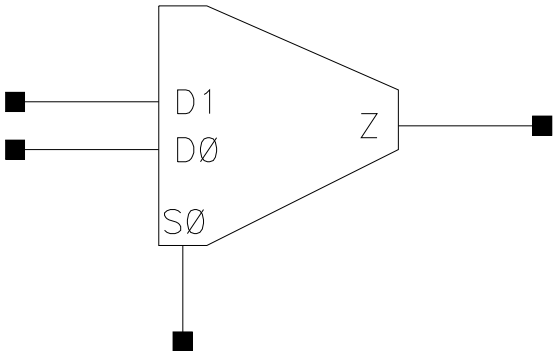
Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.360	1.0880
X9_P10	0.800	1.496	1.1968
X14_P10	0.800	2.176	1.7408
X19_P10	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P10	X9_P10	X14_P10	X19_P10
D0	0.0005	0.0007	0.0009	0.0012
D1	0.0005	0.0007	0.0009	0.0012
S0	0.0009	0.0009	0.0012	0.0015

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D0 to Z ↓	0.0480	0.0442	4.6261	2.3379
D0 to Z ↑	0.0380	0.0363	7.1590	3.6152
D1 to Z ↓	0.0484	0.0430	4.6221	2.3339
D1 to Z ↑	0.0372	0.0341	7.1710	3.6081
S0 to Z ↓	0.0455	0.0386	4.6133	2.3298
S0 to Z ↑	0.0432	0.0385	7.1617	3.6110

	X14_P10	X19_P10	X14_P10	X19_P10
D0 to Z ↓	0.0482	0.0418	1.6136	1.1629
D0 to Z ↑	0.0388	0.0352	2.4394	1.7710
D1 to Z ↓	0.0489	0.0431	1.6121	1.1622
D1 to Z ↑	0.0367	0.0338	2.4379	1.7712
S0 to Z ↓	0.0461	0.0418	1.6083	1.1608
S0 to Z ↑	0.0453	0.0404	2.4390	1.7694

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	1.032e-05	1.000e-20
X9_P10	1.703e-05	1.000e-20
X14_P10	2.287e-05	1.000e-20
X19_P10	3.337e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X9_P10	X14_P10	X19_P10
D0 (output stable)	4.111e-04	7.725e-04	8.611e-04	1.051e-03
D1 (output stable)	3.897e-04	6.419e-04	9.055e-04	1.132e-03
S0 (output stable)	6.504e-04	5.811e-04	9.478e-04	1.111e-03
D0 to Z	1.712e-03	2.657e-03	4.234e-03	5.121e-03
D1 to Z	1.662e-03	2.481e-03	4.109e-03	5.072e-03
S0 to Z	2.095e-03	2.600e-03	4.659e-03	5.569e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

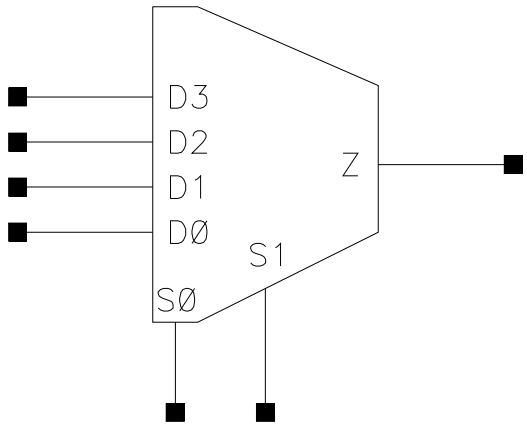
Pin Cycle (vdds)	X5_P10	X9_P10	X14_P10	X19_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.600	1.496	2.3936
X9_P10	1.600	1.768	2.8288
X13_P10	1.600	2.312	3.6992
X18_P10	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P10	X9_P10	X13_P10	X18_P10
D0	0.0004	0.0006	0.0009	0.0009
D1	0.0004	0.0005	0.0009	0.0009
D2	0.0004	0.0006	0.0009	0.0009
D3	0.0004	0.0005	0.0009	0.0009
S0	0.0012	0.0016	0.0021	0.0021
S1	0.0007	0.0008	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X9_P10	X4_P10	X9_P10
D0 to Z ↓	0.1067	0.0869	5.1040	2.4961
D0 to Z ↑	0.0657	0.0581	7.3980	3.6546
D1 to Z ↓	0.1051	0.0864	5.0925	2.4977
D1 to Z ↑	0.0658	0.0578	7.3836	3.6526
D2 to Z ↓	0.0982	0.0876	5.0365	2.5035
D2 to Z ↑	0.0633	0.0576	7.3472	3.6507
D3 to Z ↓	0.0996	0.0865	5.0531	2.5032
D3 to Z ↑	0.0643	0.0575	7.3431	3.6471
S0 to Z ↓	0.1119	0.0972	5.0713	2.4989
S0 to Z ↑	0.0786	0.0736	7.3908	3.6581
S1 to Z ↓	0.0708	0.0650	5.0659	2.4993
S1 to Z ↑	0.0598	0.0561	7.3721	3.6514
	X13_P10	X18_P10	X13_P10	X18_P10
D0 to Z ↓	0.0824	0.0895	1.7299	1.2940
D0 to Z ↑	0.0523	0.0565	2.4411	1.8464
D1 to Z ↓	0.0831	0.0902	1.7320	1.2955
D1 to Z ↑	0.0537	0.0579	2.4415	1.8452
D2 to Z ↓	0.0768	0.0834	1.7098	1.2784
D2 to Z ↑	0.0518	0.0560	2.4332	1.8418
D3 to Z ↓	0.0767	0.0832	1.7103	1.2791
D3 to Z ↑	0.0522	0.0564	2.4314	1.8403
S0 to Z ↓	0.0894	0.0963	1.7197	1.2865
S0 to Z ↑	0.0668	0.0710	2.4400	1.8461
S1 to Z ↓	0.0607	0.0676	1.7201	1.2868
S1 to Z ↑	0.0506	0.0548	2.4370	1.8438

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	9.942e-06	1.000e-20
X9_P10	1.578e-05	1.000e-20
X13_P10	2.616e-05	1.000e-20
X18_P10	2.945e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X9_P10	X13_P10	X18_P10
D0 (output stable)	2.730e-05	2.914e-05	6.875e-05	6.794e-05
D1 (output stable)	3.781e-05	4.293e-05	5.774e-05	5.717e-05
D2 (output stable)	3.871e-05	4.416e-05	6.390e-05	6.360e-05
D3 (output stable)	2.843e-05	4.213e-05	5.475e-05	5.458e-05
S0 (output stable)	8.311e-04	1.025e-03	1.663e-03	1.664e-03
S1 (output stable)	8.447e-04	9.731e-04	1.544e-03	1.544e-03
D0 to Z	2.215e-03	3.218e-03	5.178e-03	6.295e-03
D1 to Z	2.187e-03	3.205e-03	5.243e-03	6.363e-03
D2 to Z	2.077e-03	3.206e-03	4.977e-03	6.069e-03
D3 to Z	2.103e-03	3.205e-03	4.999e-03	6.086e-03
S0 to Z	3.126e-03	4.431e-03	7.051e-03	8.164e-03
S1 to Z	2.345e-03	3.398e-03	5.411e-03	6.501e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

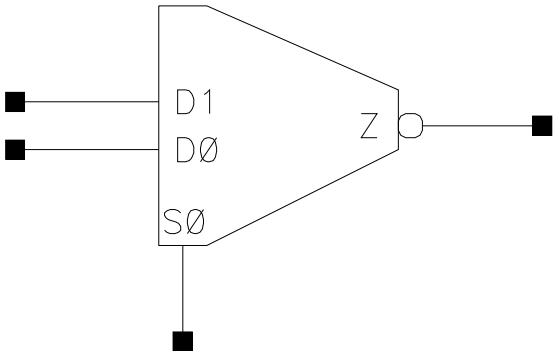
Pin Cycle (vdds)	X4_P10	X9_P10	X13_P10	X18_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P10	0.800	0.952	0.7616
X2_P10	0.800	0.952	0.7616
X6_P10	0.800	1.904	1.5232
X9_P10	0.800	2.448	1.9584
X12_P10	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P10	X2_P10	X6_P10	X9_P10
D0	0.0003	0.0005	0.0010	0.0015
D1	0.0003	0.0005	0.0010	0.0015
S0	0.0009	0.0013	0.0018	0.0026
	X12_P10			
D0	0.0020			
D1	0.0020			
S0	0.0029			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P10	X2_P10	X1_P10	X2_P10
D0 to Z ↓	0.0163	0.0155	13.4246	8.8657

D0 to Z ↑	0.0327	0.0248	30.7757	15.9586
D1 to Z ↓	0.0155	0.0144	13.2389	8.7439
D1 to Z ↑	0.0332	0.0259	30.8111	16.1184
S0 to Z ↓	0.0302	0.0204	13.2617	8.8024
S0 to Z ↑	0.0346	0.0218	30.6621	16.0156
	X6_P10	**X9_P10**	**X6_P10**	**X9_P10**
D0 to Z ↓	0.0173	0.0160	3.9069	2.6350
D0 to Z ↑	0.0262	0.0248	6.5269	4.5395
D1 to Z ↓	0.0166	0.0159	3.8522	2.6469
D1 to Z ↑	0.0279	0.0257	6.7256	4.4189
S0 to Z ↓	0.0239	0.0204	3.8705	2.6363
S0 to Z ↑	0.0250	0.0220	6.6137	4.4790
	X12_P10		**X12_P10**	
D0 to Z ↓	0.0166		2.0128	
D0 to Z ↑	0.0250		3.4183	
D1 to Z ↓	0.0158		2.0059	
D1 to Z ↑	0.0255		3.3254	
S0 to Z ↓	0.0221		2.0053	
S0 to Z ↑	0.0232		3.3688	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X1_P10	3.758e-06	1.000e-20
X2_P10	7.165e-06	1.000e-20
X6_P10	1.424e-05	1.000e-20
X9_P10	2.205e-05	1.000e-20
X12_P10	2.667e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X1_P10	X2_P10	X6_P10	X9_P10
D0 (output stable)	6.661e-06	1.564e-05	4.965e-05	7.098e-05
D1 (output stable)	6.418e-06	1.666e-05	5.325e-05	7.622e-05
S0 (output stable)	6.409e-04	6.913e-04	1.250e-03	1.880e-03
D0 to Z	5.475e-04	7.135e-04	1.902e-03	2.562e-03
D1 to Z	5.446e-04	7.094e-04	1.938e-03	2.627e-03
S0 to Z	1.121e-03	1.182e-03	2.562e-03	3.549e-03
	X12_P10			
D0 (output stable)	9.321e-05			
D1 (output stable)	9.574e-05			
S0 (output stable)	2.189e-03			
D0 to Z	3.472e-03			
D1 to Z	3.455e-03			
S0 to Z	4.469e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X1_P10	X2_P10	X6_P10	X9_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

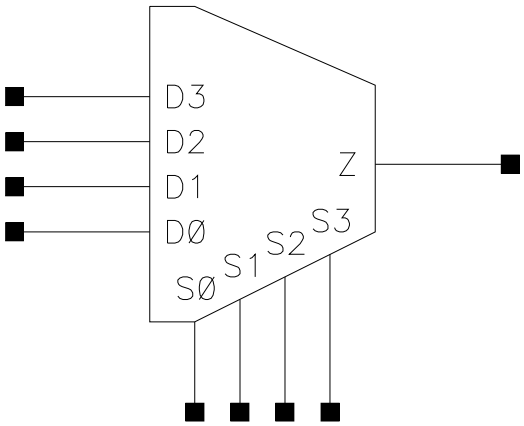
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P10			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.600	0.952	1.5232
X15_P10	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
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0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P10	X15_P10
D0	0.0005	0.0013
D1	0.0005	0.0011
D2	0.0005	0.0013
D3	0.0005	0.0011
S0	0.0005	0.0012
S1	0.0005	0.0013
S2	0.0005	0.0012
S3	0.0006	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X15_P10	X4_P10	X15_P10
D0 to Z ↓	0.0535	0.0567	7.6157	2.0026
D0 to Z ↑	0.0448	0.0421	6.7676	1.7079
D1 to Z ↓	0.0484	0.0502	7.6141	2.0015
D1 to Z ↑	0.0388	0.0368	6.7309	1.6988
D2 to Z ↓	0.0521	0.0547	7.6308	2.0053
D2 to Z ↑	0.0435	0.0398	6.7919	1.7153
D3 to Z ↓	0.0465	0.0485	7.6212	2.0035
D3 to Z ↑	0.0374	0.0349	6.7567	1.7076
S0 to Z ↓	0.0512	0.0518	7.6136	2.0008
S0 to Z ↑	0.0471	0.0421	6.7694	1.7075
S1 to Z ↓	0.0457	0.0462	7.6106	1.9996
S1 to Z ↑	0.0406	0.0371	6.7324	1.6981
S2 to Z ↓	0.0505	0.0504	7.6276	2.0028
S2 to Z ↑	0.0459	0.0402	6.7896	1.7163
S3 to Z ↓	0.0455	0.0445	7.6167	2.0003
S3 to Z ↑	0.0401	0.0351	6.7570	1.7063

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	1.189e-05	1.000e-20
X15_P10	3.511e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X15_P10
D0 (output stable)	3.072e-04	8.652e-04
D1 (output stable)	2.480e-04	6.924e-04
D2 (output stable)	3.053e-04	8.502e-04
D3 (output stable)	2.474e-04	6.818e-04
S0 (output stable)	2.927e-04	8.285e-04
S1 (output stable)	2.369e-04	6.825e-04
S2 (output stable)	2.973e-04	8.273e-04
S3 (output stable)	2.404e-04	6.783e-04
D0 to Z	2.338e-03	6.640e-03
D1 to Z	1.979e-03	5.648e-03
D2 to Z	2.141e-03	5.892e-03
D3 to Z	1.787e-03	4.927e-03
S0 to Z	2.253e-03	6.173e-03
S1 to Z	1.903e-03	5.254e-03
S2 to Z	2.076e-03	5.482e-03
S3 to Z	1.731e-03	4.512e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

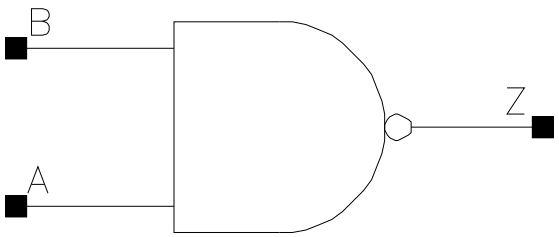
Pin Cycle (vdds)	X4_P10	X15_P10
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P10	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P10	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P10	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P10	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P10	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P10	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P10	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P10	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P10	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P10	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P10	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P10	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P10	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P10	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P10	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P10	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P10	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P10	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P10	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P10	C8T28SOI_LL_-NAND2X4_P10	C8T28SOI_LL_-NAND2X8_P10	C8T28SOI_LL_-NAND2X12_P10
A	0.0003	0.0005	0.0010	0.0015
B	0.0003	0.0005	0.0009	0.0014
	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X24_P10	C8T28SOI_-LLBR0P8_-NAND2X4_P10
A	0.0019	0.0024	0.0007	0.0006
B	0.0018	0.0022	0.0006	0.0005
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	C8T28SOI_-LLBR0P8_-NAND2X12_P10	C8T28SOI_-LLBR0P8_-NAND2X16_P10	C8T28SOI_LLS_-NAND2X8_P10
A	0.0010	0.0015	0.0020	0.0010
B	0.0009	0.0013	0.0017	0.0009
	C8T28SOI_LLS_-NAND2X15_P10	C8T28SOI_LLS_-NAND2X23_P10	C8T28SOI_LLS_-NAND2X31_P10	C8T28SOIDV_LL_-NAND2X9_P10
A	0.0020	0.0030	0.0039	0.0011
B	0.0018	0.0027	0.0036	0.0011
	C8T28SOIDV_LL_-NAND2X18_P10	C8T28SOIDV_LL_-NAND2X27_P10	C8T28SOIDV_LL_-NAND2X36_P10	
A	0.0021	0.0031	0.0042	
B	0.0020	0.0029	0.0039	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-NAND2X2_P10	**C8T28SOI_LL_-NAND2X4_P10**	**C8T28SOI_LL_-NAND2X2_P10**	**C8T28SOI_LL_-NAND2X4_P10**
A to Z ↓	0.0125	0.0108	14.5832	7.7272
A to Z ↑	0.0190	0.0157	13.9534	7.1842
B to Z ↓	0.0144	0.0118	14.6681	7.7781
B to Z ↑	0.0179	0.0139	14.0073	7.2671
	C8T28SOI_LL_-NAND2X8_P10	**C8T28SOI_LL_-NAND2X12_P10**	**C8T28SOI_LL_-NAND2X8_P10**	**C8T28SOI_LL_-NAND2X12_P10**
A to Z ↓	0.0122	0.0116	3.8717	2.6435
A to Z ↑	0.0159	0.0155	3.4256	2.3244
B to Z ↓	0.0108	0.0113	3.9017	2.6640
B to Z ↑	0.0124	0.0127	3.4458	2.3475

	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10
A to Z ↓	0.0120	0.0117	2.0018	1.6154
A to Z ↑	0.0155	0.0155	1.7487	1.4114
B to Z ↓	0.0108	0.0114	2.0194	1.6286
B to Z ↑	0.0122	0.0126	1.7652	1.4257
	C8T28SOI_LL_-NAND2X24_P10	**C8T28SOI_-LLBR0P8_-NAND2X4_P10**	**C8T28SOI_LL_-NAND2X24_P10**	**C8T28SOI_-LLBR0P8_-NAND2X4_P10**
A to Z ↓	0.0455	0.0092	0.8981	5.3823
A to Z ↑	0.0459	0.0200	1.3944	9.2150
B to Z ↓	0.0467	0.0095	0.8980	5.4430
B to Z ↑	0.0439	0.0170	1.3935	9.2336
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	**C8T28SOI_-LLBR0P8_-NAND2X12_P10**	**C8T28SOI_-LLBR0P8_-NAND2X8_P10**	**C8T28SOI_-LLBR0P8_-NAND2X12_P10**
A to Z ↓	0.0102	0.0101	2.9194	1.9925
A to Z ↑	0.0201	0.0201	4.6286	3.1228
B to Z ↓	0.0081	0.0090	2.9583	2.0179
B to Z ↑	0.0148	0.0155	4.6573	3.1404
	C8T28SOI_-LLBR0P8_-NAND2X16_P10	**C8T28SOI_LLS_-NAND2X8_P10**	**C8T28SOI_-LLBR0P8_-NAND2X16_P10**	**C8T28SOI_LLS_-NAND2X8_P10**
A to Z ↓	0.0098	0.0122	1.5180	3.8623
A to Z ↑	0.0193	0.0160	2.3377	3.4574
B to Z ↓	0.0079	0.0108	1.5384	3.8923
B to Z ↑	0.0141	0.0125	2.3583	3.4896
	C8T28SOI_LLS_-NAND2X15_P10	**C8T28SOI_LLS_-NAND2X23_P10**	**C8T28SOI_LLS_-NAND2X15_P10**	**C8T28SOI_LLS_-NAND2X23_P10**
A to Z ↓	0.0121	0.0121	1.9989	1.3471
A to Z ↑	0.0156	0.0155	1.7278	1.1524
B to Z ↓	0.0109	0.0111	2.0157	1.3588
B to Z ↑	0.0123	0.0123	1.7387	1.1605
	C8T28SOI_LLS_-NAND2X31_P10	**C8T28SOIDV_LL_-NAND2X9_P10**	**C8T28SOI_LLS_-NAND2X31_P10**	**C8T28SOIDV_LL_-NAND2X9_P10**
A to Z ↓	0.0120	0.0101	1.0188	2.9277
A to Z ↑	0.0154	0.0164	0.8666	3.3687
B to Z ↓	0.0113	0.0105	1.0272	2.9558
B to Z ↑	0.0124	0.0141	0.8725	3.4169
	C8T28SOIDV_LL_-NAND2X18_P10	**C8T28SOIDV_LL_-NAND2X27_P10**	**C8T28SOIDV_LL_-NAND2X18_P10**	**C8T28SOIDV_LL_-NAND2X27_P10**
A to Z ↓	0.0112	0.0111	1.4789	1.0070
A to Z ↑	0.0169	0.0169	1.6930	1.1382
B to Z ↓	0.0096	0.0105	1.4941	1.0159
B to Z ↑	0.0130	0.0137	1.7032	1.1447
	C8T28SOIDV_LL_-NAND2X36_P10		**C8T28SOIDV_LL_-NAND2X36_P10**	
A to Z ↓	0.0113		0.7585	
A to Z ↑	0.0168		0.8533	
B to Z ↓	0.0098		0.7664	
B to Z ↑	0.0129		0.8586	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P10	1.648e-06	1.000e-20
C8T28SOI_LL_NAND2X4_P10	3.509e-06	1.000e-20
C8T28SOI_LL_NAND2X8_P10	6.918e-06	1.000e-20
C8T28SOI_LL_NAND2X12_P10	9.951e-06	1.000e-20
C8T28SOI_LL_NAND2X15_P10	1.299e-05	1.000e-20
C8T28SOI_LL_NAND2X19_P10	1.604e-05	1.000e-20
C8T28SOI_LL_NAND2X24_P10	2.439e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P10	3.888e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P10	6.952e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_-P10	9.906e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_-P10	1.287e-05	1.000e-20
C8T28SOI_LLS_NAND2X8_P10	6.918e-06	1.000e-20
C8T28SOI_LLS_NAND2X15_P10	1.299e-05	1.000e-20
C8T28SOI_LLS_NAND2X23_P10	1.908e-05	1.000e-20
C8T28SOI_LLS_NAND2X31_P10	2.518e-05	1.000e-20
C8T28SOIDV_LL_NAND2X9_P10	8.563e-06	1.000e-20
C8T28SOIDV_LL_NAND2X18_P10	1.620e-05	1.000e-20
C8T28SOIDV_LL_NAND2X27_P10	2.338e-05	1.000e-20
C8T28SOIDV_LL_NAND2X36_P10	3.058e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P10	C8T28SOI_LL_-NAND2X4_P10	C8T28SOI_LL_-NAND2X8_P10	C8T28SOI_LL_-NAND2X12_P10
A (output stable)	4.563e-06	9.102e-06	4.429e-05	5.547e-05
B (output stable)	9.937e-06	1.882e-05	1.401e-04	1.363e-04
A to Z	3.396e-04	5.107e-04	1.154e-03	1.638e-03
B to Z	2.951e-04	4.176e-04	7.795e-04	1.214e-03
	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X24_P10	C8T28SOI_-LLBR0P8_-NAND2X4_P10
A (output stable)	8.334e-05	9.127e-05	1.103e-05	1.313e-05
B (output stable)	2.411e-04	2.216e-04	2.159e-05	2.636e-05
A to Z	2.218e-03	2.713e-03	5.446e-03	5.883e-04
B to Z	1.535e-03	1.997e-03	5.348e-03	4.488e-04
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	C8T28SOI_-LLBR0P8_-NAND2X12_P10	C8T28SOI_-LLBR0P8_-NAND2X16_P10	C8T28SOI_LLS_-NAND2X8_P10
A (output stable)	5.346e-05	6.387e-05	1.005e-04	4.511e-05
B (output stable)	1.635e-04	1.611e-04	2.776e-04	1.486e-04
A to Z	1.219e-03	1.803e-03	2.273e-03	1.161e-03
B to Z	7.336e-04	1.213e-03	1.380e-03	7.874e-04
	C8T28SOI_LLS_-NAND2X15_P10	C8T28SOI_LLS_-NAND2X23_P10	C8T28SOI_LLS_-NAND2X31_P10	C8T28SOIDV_LL_-NAND2X9_P10
A (output stable)	8.600e-05	1.256e-04	1.592e-04	2.363e-05
B (output stable)	2.461e-04	3.392e-04	4.158e-04	4.898e-05
A to Z	2.245e-03	3.336e-03	4.412e-03	1.215e-03
B to Z	1.557e-03	2.356e-03	3.155e-03	9.611e-04
	C8T28SOIDV_LL_-NAND2X18_P10	C8T28SOIDV_LL_-NAND2X27_P10	C8T28SOIDV_LL_-NAND2X36_P10	
A (output stable)	9.488e-05	1.163e-04	1.948e-04	

B (output stable)	3.269e-04	2.658e-04	6.315e-04	
A to Z	2.579e-03	3.812e-03	5.085e-03	
B to Z	1.718e-03	2.820e-03	3.417e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

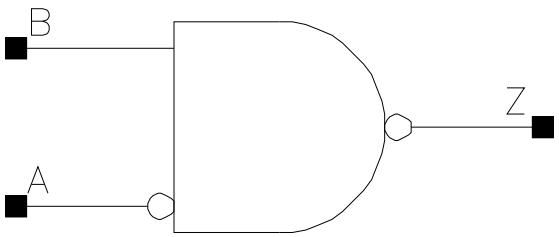
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P10	C8T28SOI_LL_-NAND2X4_P10	C8T28SOI_LL_-NAND2X8_P10	C8T28SOI_LL_-NAND2X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X24_P10	C8T28SOI_-LLBR0P8_-NAND2X4_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	C8T28SOI_-LLBR0P8_-NAND2X12_P10	C8T28SOI_-LLBR0P8_-NAND2X16_P10	C8T28SOI_LLS_-NAND2X8_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P10	C8T28SOI_LLS_-NAND2X23_P10	C8T28SOI_LLS_-NAND2X31_P10	C8T28SOIDV_LL_-NAND2X9_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P10	C8T28SOIDV_LL_-NAND2X27_P10	C8T28SOIDV_LL_-NAND2X36_P10	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.544	0.4352
X4_P10	0.800	0.680	0.5440
X9_P10	1.600	0.544	0.8704
X13_P10	1.600	0.816	1.3056
X17_P10	1.600	0.816	1.3056
X23_P10	0.800	2.312	1.8496
X27_P10	1.600	1.088	1.7408
X31_P10	0.800	2.992	2.3936
X36_P10	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P10	X4_P10	X9_P10	X13_P10
A	0.0005	0.0005	0.0009	0.0009
B	0.0003	0.0005	0.0010	0.0016
	X17_P10	X23_P10	X27_P10	X31_P10
A	0.0008	0.0018	0.0014	0.0024
B	0.0019	0.0027	0.0029	0.0035
	X36_P10			
A	0.0014			
B	0.0039			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X4_P10**	**X2_P10**	**X4_P10**
A to Z ↓	0.0337	0.0346	14.6730	7.7999
A to Z ↑	0.0263	0.0264	13.7844	7.0552
B to Z ↓	0.0148	0.0119	14.8760	7.9139
B to Z ↑	0.0180	0.0139	14.0116	7.2634
	X9_P10	**X13_P10**	**X9_P10**	**X13_P10**
A to Z ↓	0.0336	0.0409	2.9904	1.9149
A to Z ↑	0.0253	0.0305	3.3423	2.2614
B to Z ↓	0.0107	0.0106	3.0420	1.9454
B to Z ↑	0.0141	0.0145	3.4294	2.3470
	X17_P10	**X23_P10**	**X17_P10**	**X23_P10**
A to Z ↓	0.0443	0.0322	1.5002	1.3386
A to Z ↑	0.0315	0.0256	1.7139	1.1544
B to Z ↓	0.0102	0.0109	1.5189	1.3606
B to Z ↑	0.0137	0.0122	1.7829	1.1837
	X27_P10	**X31_P10**	**X27_P10**	**X31_P10**
A to Z ↓	0.0375	0.0318	1.0048	1.0106
A to Z ↑	0.0281	0.0252	1.1314	0.8486
B to Z ↓	0.0100	0.0111	1.0216	1.0276
B to Z ↑	0.0131	0.0123	1.1489	0.8897
	X36_P10		**X36_P10**	
A to Z ↓	0.0433		0.7611	
A to Z ↑	0.0319		0.8492	
B to Z ↓	0.0098		0.7710	
B to Z ↑	0.0128		0.8633	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P10	2.947e-06	1.000e-20
X4_P10	5.004e-06	1.000e-20
X9_P10	1.233e-05	1.000e-20
X13_P10	1.506e-05	1.000e-20
X17_P10	1.929e-05	1.000e-20
X23_P10	2.867e-05	1.000e-20
X27_P10	3.060e-05	1.000e-20
X31_P10	3.762e-05	1.000e-20
X36_P10	3.793e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P10	X4_P10	X9_P10	X13_P10
A (output stable)	5.130e-04	6.538e-04	1.258e-03	1.842e-03
B (output stable)	1.004e-05	1.911e-05	5.122e-05	1.431e-04
A to Z	8.742e-04	1.193e-03	2.568e-03	4.067e-03
B to Z	2.978e-04	4.148e-04	9.748e-04	1.485e-03
	X17_P10	X23_P10	X27_P10	X31_P10
A (output stable)	2.070e-03	3.201e-03	3.240e-03	4.184e-03
B (output stable)	1.709e-04	2.945e-04	2.674e-04	3.865e-04
A to Z	4.830e-03	6.783e-03	7.126e-03	8.962e-03
B to Z	1.822e-03	2.348e-03	2.642e-03	3.116e-03
	X36_P10			
A (output stable)	4.263e-03			

B (output stable)	4.434e-04			
A to Z	9.486e-03			
B to Z	3.377e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

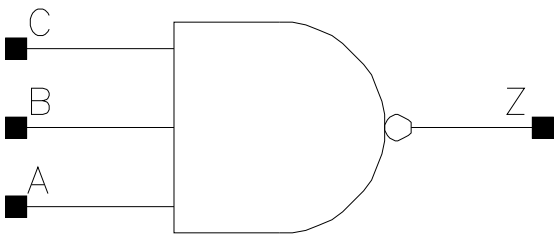
Pin Cycle (vdds)	X2_P10	X4_P10	X9_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P10	X23_P10	X27_P10	X31_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P10	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P10	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P10	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P10	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P10	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P10	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P10	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P10	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P10	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P10	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P10	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P10	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P10	C8T28SOI_LL_-NAND3X7_P10	C8T28SOI_LL_-NAND3X10_P10	C8T28SOI_LL_-NAND3X14_P10
A	0.0005	0.0010	0.0015	0.0019
B	0.0005	0.0010	0.0014	0.0018
C	0.0005	0.0009	0.0013	0.0018
	C8T28SOI_LL_-NAND3X20_P10	C8T28SOI_LL_-NAND3X27_P10	C8T28SOI_-LLBR0P6_-NAND3X3_P10	C8T28SOI_-LLBR0P6_-NAND3X7_P10
A	0.0029	0.0039	0.0006	0.0010
B	0.0028	0.0037	0.0005	0.0010
C	0.0026	0.0035	0.0005	0.0009
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	C8T28SOI_-LLBR0P6_-NAND3X14_P10	C8T28SOI_-LLBR0P6_-NAND3X20_P10	C8T28SOI_-LLBR0P6_-NAND3X27_P10
A	0.0015	0.0020	0.0029	0.0040
B	0.0014	0.0018	0.0027	0.0036
C	0.0013	0.0018	0.0026	0.0034

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND3X3_P10	**C8T28SOI_LL_-NAND3X7_P10**	**C8T28SOI_LL_-NAND3X3_P10**	**C8T28SOI_LL_-NAND3X7_P10**
A to Z ↓	0.0165	0.0187	11.3342	5.6049
A to Z ↑	0.0195	0.0201	7.2253	3.5197
B to Z ↓	0.0169	0.0179	11.3548	5.6193
B to Z ↑	0.0180	0.0184	7.2470	3.5245
C to Z ↓	0.0173	0.0160	11.3914	5.6339
C to Z ↑	0.0164	0.0153	7.3046	3.4461
	C8T28SOI_LL_-NAND3X10_P10	**C8T28SOI_LL_-NAND3X14_P10**	**C8T28SOI_LL_-NAND3X10_P10**	**C8T28SOI_LL_-NAND3X14_P10**
A to Z ↓	0.0177	0.0182	3.8677	2.9100
A to Z ↑	0.0190	0.0193	2.2909	1.7711
B to Z ↓	0.0176	0.0174	3.8778	2.9175
B to Z ↑	0.0174	0.0175	2.3439	1.7707
C to Z ↓	0.0160	0.0158	3.8891	2.9262
C to Z ↑	0.0148	0.0147	2.3564	1.7598
	C8T28SOI_LL_-NAND3X20_P10	**C8T28SOI_LL_-NAND3X27_P10**	**C8T28SOI_LL_-NAND3X20_P10**	**C8T28SOI_LL_-NAND3X27_P10**
A to Z ↓	0.0177	0.0178	1.9764	1.4995
A to Z ↑	0.0187	0.0187	1.1523	0.8679
B to Z ↓	0.0175	0.0175	1.9817	1.5036
B to Z ↑	0.0171	0.0170	1.1524	0.8668
C to Z ↓	0.0157	0.0159	1.9883	1.5086
C to Z ↑	0.0143	0.0143	1.1766	0.8853
	C8T28SOI_-LLBR0P6_-NAND3X3_P10	**C8T28SOI_-LLBR0P6_-NAND3X7_P10**	**C8T28SOI_-LLBR0P6_-NAND3X3_P10**	**C8T28SOI_-LLBR0P6_-NAND3X7_P10**
A to Z ↓	0.0122	0.0150	7.0094	3.8274
A to Z ↑	0.0274	0.0296	10.9935	5.5727
B to Z ↓	0.0119	0.0138	7.0549	3.8455
B to Z ↑	0.0240	0.0256	10.9709	5.5789

C to Z ↓	0.0114	0.0110	7.1137	3.8747
C to Z ↑	0.0202	0.0197	11.0381	5.5428
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	**C8T28SOI_-LLBR0P6_-NAND3X14_P10**	**C8T28SOI_-LLBR0P6_-NAND3X10_P10**	**C8T28SOI_-LLBR0P6_-NAND3X14_P10**
A to Z ↓	0.0137	0.0146	2.5775	1.9483
A to Z ↑	0.0278	0.0285	3.7165	2.8099
B to Z ↓	0.0126	0.0129	2.5927	1.9598
B to Z ↑	0.0237	0.0242	3.7276	2.8140
C to Z ↓	0.0106	0.0102	2.6146	1.9770
C to Z ↑	0.0186	0.0182	3.7506	2.8122
	C8T28SOI_-LLBR0P6_-NAND3X20_P10	**C8T28SOI_-LLBR0P6_-NAND3X27_P10**	**C8T28SOI_-LLBR0P6_-NAND3X20_P10**	**C8T28SOI_-LLBR0P6_-NAND3X27_P10**
A to Z ↓	0.0139	0.0139	1.3179	1.0062
A to Z ↑	0.0278	0.0277	1.8708	1.4093
B to Z ↓	0.0127	0.0127	1.3256	1.0118
B to Z ↑	0.0238	0.0236	1.8747	1.4100
C to Z ↓	0.0101	0.0102	1.3374	1.0208
C to Z ↑	0.0178	0.0178	1.8858	1.4180

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P10	2.806e-06	1.000e-20
C8T28SOI_LL_NAND3X7_P10	5.868e-06	1.000e-20
C8T28SOI_LL_NAND3X10_P10	8.033e-06	1.000e-20
C8T28SOI_LL_NAND3X14_P10	1.088e-05	1.000e-20
C8T28SOI_LL_NAND3X20_P10	1.590e-05	1.000e-20
C8T28SOI_LL_NAND3X27_P10	2.091e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P10	3.255e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P10	6.332e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_-P10	8.394e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_-P10	1.149e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_-P10	1.665e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_-P10	2.179e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P10	C8T28SOI_LL_-NAND3X7_P10	C8T28SOI_LL_-NAND3X10_P10	C8T28SOI_LL_-NAND3X14_P10
A (output stable)	1.076e-05	4.473e-05	5.737e-05	8.436e-05
B (output stable)	1.412e-05	7.798e-05	1.028e-04	1.443e-04
C (output stable)	3.935e-05	2.272e-04	2.735e-04	4.149e-04
A to Z	7.671e-04	1.768e-03	2.432e-03	3.319e-03
B to Z	6.646e-04	1.447e-03	1.989e-03	2.691e-03
C to Z	5.697e-04	1.107e-03	1.548e-03	2.072e-03
	C8T28SOI_LL_-NAND3X20_P10	C8T28SOI_LL_-NAND3X27_P10	C8T28SOI_-LLBR0P6_-NAND3X3_P10	C8T28SOI_-LLBR0P6_-NAND3X7_P10

A (output stable)	1.142e-04	1.534e-04	1.748e-05	6.028e-05
B (output stable)	2.051e-04	2.735e-04	2.196e-05	9.472e-05
C (output stable)	6.132e-04	7.883e-04	6.465e-05	2.976e-04
A to Z	4.797e-03	6.370e-03	8.444e-04	1.966e-03
B to Z	3.929e-03	5.203e-03	6.760e-04	1.502e-03
C to Z	2.947e-03	3.934e-03	5.042e-04	9.971e-04
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	C8T28SOI_-LLBR0P6_-NAND3X14_P10	C8T28SOI_-LLBR0P6_-NAND3X20_P10	C8T28SOI_-LLBR0P6_-NAND3X27_P10
A (output stable)	7.642e-05	1.244e-04	1.592e-04	2.158e-04
B (output stable)	1.249e-04	2.010e-04	2.680e-04	3.554e-04
C (output stable)	3.623e-04	5.690e-04	8.106e-04	1.045e-03
A to Z	2.640e-03	3.694e-03	5.286e-03	6.990e-03
B to Z	1.955e-03	2.712e-03	3.906e-03	5.136e-03
C to Z	1.324e-03	1.731e-03	2.477e-03	3.289e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

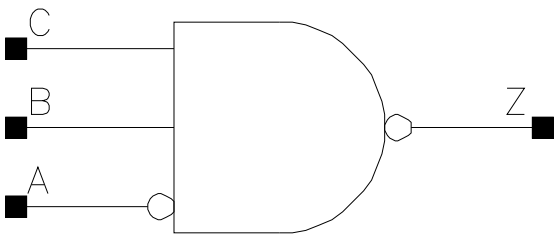
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P10	C8T28SOI_LL_-NAND3X7_P10	C8T28SOI_LL_-NAND3X10_P10	C8T28SOI_LL_-NAND3X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P10	C8T28SOI_LL_-NAND3X27_P10	C8T28SOI_-LLBR0P6_-NAND3X3_P10	C8T28SOI_-LLBR0P6_-NAND3X7_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	C8T28SOI_-LLBR0P6_-NAND3X14_P10	C8T28SOI_-LLBR0P6_-NAND3X20_P10	C8T28SOI_-LLBR0P6_-NAND3X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X7_P10	0.800	1.360	1.0880
X10_P10	0.800	1.632	1.3056
X14_P10	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X10_P10	X14_P10
A	0.0006	0.0009	0.0007	0.0007
B	0.0005	0.0010	0.0014	0.0019
C	0.0005	0.0009	0.0013	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0422	0.0404	11.3624	5.6449
A to Z ↑	0.0301	0.0299	7.0553	3.3979
B to Z ↓	0.0164	0.0176	11.4322	5.6740
B to Z ↑	0.0175	0.0177	7.2544	3.4541
C to Z ↓	0.0167	0.0154	11.4681	5.6911
C to Z ↑	0.0158	0.0145	7.3136	3.4516
	X10_P10	**X14_P10**	**X10_P10**	**X14_P10**
A to Z ↓	0.0445	0.0482	3.8630	2.9274

A to Z ↑	0.0331	0.0361	2.3094	1.7306
B to Z ↓	0.0175	0.0170	3.8790	2.9382
B to Z ↑	0.0173	0.0170	2.3464	1.7566
C to Z ↓	0.0159	0.0153	3.8912	2.9476
C to Z ↑	0.0147	0.0140	2.3612	1.7616

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	4.142e-06	1.000e-20
X7_P10	9.103e-06	1.000e-20
X10_P10	1.130e-05	1.000e-20
X14_P10	1.417e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	6.692e-04	1.225e-03	1.563e-03	1.916e-03
B (output stable)	1.473e-05	6.292e-05	1.085e-04	1.312e-04
C (output stable)	3.998e-05	2.349e-04	2.903e-04	4.003e-04
A to Z	1.428e-03	3.030e-03	4.222e-03	5.396e-03
B to Z	6.276e-04	1.377e-03	1.983e-03	2.576e-03
C to Z	5.307e-04	1.021e-03	1.530e-03	1.935e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

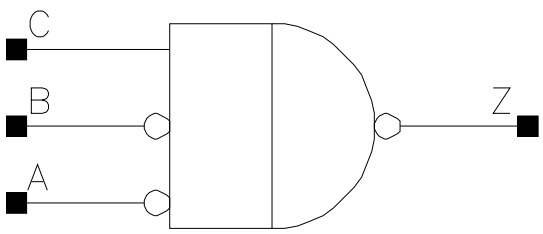
Pin Cycle (vdds)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	0.816	0.6528
X8_P10	0.800	1.088	0.8704
X12_P10	0.800	1.632	1.3056
X15_P10	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X12_P10	X15_P10
A	0.0006	0.0006	0.0012	0.0011
B	0.0007	0.0006	0.0012	0.0011
C	0.0005	0.0009	0.0013	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0373	0.0461	7.2874	3.8663
A to Z ↑	0.0251	0.0289	6.7519	3.3711
B to Z ↓	0.0376	0.0463	7.2926	3.8687
B to Z ↑	0.0237	0.0276	6.7385	3.3681
C to Z ↓	0.0121	0.0110	7.3780	3.8971
C to Z ↑	0.0142	0.0126	6.7827	3.4691
	X12_P10	**X15_P10**	**X12_P10**	**X15_P10**
A to Z ↓	0.0417	0.0459	2.6292	2.0034
A to Z ↑	0.0265	0.0313	2.2522	1.6962
B to Z ↓	0.0390	0.0436	2.6270	2.0016

B to Z ↑	0.0242	0.0289	2.2473	1.6933
C to Z ↓	0.0119	0.0109	2.6582	2.0227
C to Z ↑	0.0133	0.0121	2.3458	1.7357

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	6.910e-06	1.000e-20
X8_P10	9.369e-06	1.000e-20
X12_P10	1.482e-05	1.000e-20
X15_P10	1.654e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	3.606e-04	4.922e-04	8.270e-04	9.502e-04
B (output stable)	3.209e-04	4.515e-04	7.116e-04	8.417e-04
C (output stable)	2.107e-05	1.418e-04	1.392e-04	2.284e-04
A to Z	1.662e-03	2.747e-03	4.310e-03	5.224e-03
B to Z	1.520e-03	2.603e-03	3.801e-03	4.744e-03
C to Z	4.697e-04	8.059e-04	1.316e-03	1.564e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

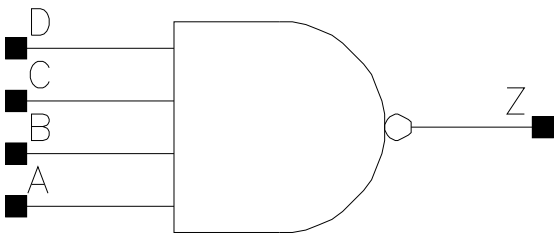
Pin Cycle (vdds)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.224	0.9792
X10_P10	0.800	1.360	1.0880
X14_P10	0.800	1.904	1.5232
X18_P10	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X18_P10
A	0.0004	0.0004	0.0005	0.0006
B	0.0005	0.0005	0.0005	0.0008
C	0.0004	0.0004	0.0005	0.0006
D	0.0004	0.0004	0.0005	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0639	0.0588	4.3362	2.1873
A to Z ↑	0.0503	0.0511	6.7945	3.4305
B to Z ↓	0.0663	0.0614	4.3318	2.1851
B to Z ↑	0.0491	0.0506	6.7949	3.4286
C to Z ↓	0.0663	0.0602	4.3321	2.1878
C to Z ↑	0.0527	0.0543	6.7823	3.4306

D to Z ↓	0.0693	0.0630	4.3366	2.1874
D to Z ↑	0.0525	0.0541	6.7923	3.4263
	X14_P10	**X18_P10**	**X14_P10**	**X18_P10**
A to Z ↓	0.0628	0.0580	1.5039	1.2215
A to Z ↑	0.0504	0.0492	2.3397	1.8539
B to Z ↓	0.0653	0.0601	1.5044	1.2215
B to Z ↑	0.0491	0.0484	2.3380	1.8547
C to Z ↓	0.0601	0.0531	1.5024	1.2200
C to Z ↑	0.0512	0.0484	2.3333	1.8512
D to Z ↓	0.0626	0.0549	1.5014	1.2209
D to Z ↑	0.0506	0.0469	2.3326	1.8519

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	7.581e-06	1.000e-20
X10_P10	1.190e-05	1.000e-20
X14_P10	1.690e-05	1.000e-20
X18_P10	2.185e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	2.611e-04	3.182e-04	4.685e-04	5.153e-04
B (output stable)	2.458e-04	3.019e-04	4.454e-04	4.897e-04
C (output stable)	2.831e-04	3.157e-04	4.863e-04	4.821e-04
D (output stable)	2.675e-04	2.996e-04	4.601e-04	4.491e-04
A to Z	2.018e-03	2.877e-03	4.457e-03	5.194e-03
B to Z	1.974e-03	2.831e-03	4.388e-03	5.125e-03
C to Z	2.139e-03	2.939e-03	4.227e-03	4.805e-03
D to Z	2.108e-03	2.899e-03	4.164e-03	4.720e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

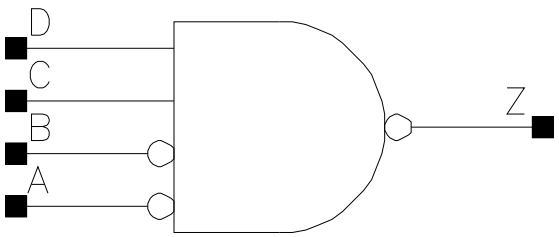
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.952	0.7616
X7_P10	0.800	1.360	1.0880
X10_P10	0.800	2.040	1.6320
X14_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P10	X7_P10	X10_P10	X14_P10
A	0.0007	0.0007	0.0012	0.0011
B	0.0007	0.0006	0.0012	0.0011
C	0.0006	0.0010	0.0014	0.0018
D	0.0005	0.0009	0.0013	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X7_P10	X3_P10	X7_P10
A to Z ↓	0.0432	0.0506	10.7567	5.6522
A to Z ↑	0.0276	0.0314	6.7908	3.4077
B to Z ↓	0.0427	0.0505	10.7592	5.6536
B to Z ↑	0.0259	0.0297	6.7886	3.4077
C to Z ↓	0.0169	0.0174	10.8311	5.6706
C to Z ↑	0.0181	0.0176	6.9369	3.4580

D to Z ↓	0.0165	0.0153	10.8488	5.6867
D to Z ↑	0.0159	0.0144	6.9194	3.4525
	X10_P10	**X14_P10**	**X10_P10**	**X14_P10**
A to Z ↓	0.0473	0.0518	3.8577	2.9355
A to Z ↑	0.0288	0.0360	2.2946	1.7059
B to Z ↓	0.0446	0.0500	3.8582	2.9359
B to Z ↑	0.0266	0.0339	2.2891	1.7036
C to Z ↓	0.0174	0.0170	3.8723	2.9436
C to Z ↑	0.0173	0.0170	2.3477	1.7587
D to Z ↓	0.0158	0.0153	3.8840	2.9526
D to Z ↑	0.0146	0.0141	2.3610	1.7636

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	6.039e-06	1.000e-20
X7_P10	7.903e-06	1.000e-20
X10_P10	1.295e-05	1.000e-20
X14_P10	1.390e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	4.434e-04	6.037e-04	1.065e-03	1.248e-03
B (output stable)	3.903e-04	5.500e-04	8.992e-04	1.101e-03
C (output stable)	3.433e-05	7.158e-05	1.120e-04	1.493e-04
D (output stable)	9.534e-05	2.679e-04	3.256e-04	4.646e-04
A to Z	1.951e-03	3.196e-03	5.016e-03	6.351e-03
B to Z	1.812e-03	3.059e-03	4.527e-03	5.905e-03
C to Z	6.777e-04	1.366e-03	1.960e-03	2.573e-03
D to Z	5.786e-04	1.011e-03	1.515e-03	1.949e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

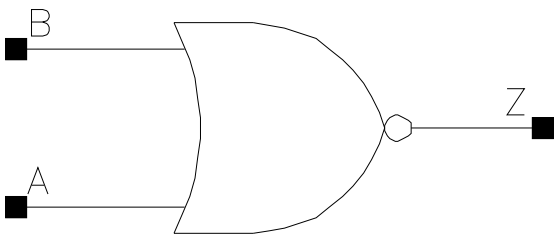
Pin Cycle (vdds)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.408	0.3264
X4_P10	0.800	0.408	0.3264
X8_P10	0.800	0.680	0.5440
X9_P10	1.600	0.408	0.6528
X12_P10	0.800	0.952	0.7616
X16_P10	0.800	1.224	0.9792
X19_P10	1.600	0.680	1.0880
X20_P10	0.800	1.496	1.1968
X23_P10	0.800	1.496	1.1968
X24_P10	0.800	1.768	1.4144
X27_P10	0.800	1.632	1.3056
X29_P10	1.600	0.952	1.5232
X31_P10	0.800	2.312	1.8496
X34_P10	0.800	2.040	1.6320
X38_P10	0.800	2.176	1.7408
X39_P10	1.600	1.224	1.9584
X46_P10	1.600	1.224	1.9584
X57_P10	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P10	X4_P10	X8_P10	X9_P10
A	0.0004	0.0005	0.0010	0.0011
B	0.0003	0.0005	0.0009	0.0010
	X12_P10	X16_P10	X19_P10	X20_P10

A	0.0015	0.0020	0.0022	0.0025
B	0.0013	0.0018	0.0020	0.0022
	X23_P10	X24_P10	X27_P10	X29_P10
A	0.0007	0.0029	0.0007	0.0032
B	0.0006	0.0027	0.0006	0.0030
	X31_P10	X34_P10	X38_P10	X39_P10
A	0.0039	0.0007	0.0007	0.0043
B	0.0036	0.0006	0.0006	0.0039
	X46_P10	X57_P10		
A	0.0007	0.0007		
B	0.0008	0.0008		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X4_P10**	**X2_P10**	**X4_P10**
A to Z ↓	0.0118	0.0111	8.7398	4.5606
A to Z ↑	0.0225	0.0198	26.6506	13.9829
B to Z ↓	0.0108	0.0097	8.7842	4.5932
B to Z ↑	0.0228	0.0194	26.7232	14.0206
	X8_P10	**X9_P10**	**X8_P10**	**X9_P10**
A to Z ↓	0.0103	0.0094	2.1966	1.6987
A to Z ↑	0.0191	0.0182	6.5266	6.3165
B to Z ↓	0.0075	0.0080	2.2001	1.7479
B to Z ↑	0.0150	0.0178	6.5507	6.3334
	X12_P10	**X16_P10**	**X12_P10**	**X16_P10**
A to Z ↓	0.0105	0.0105	1.5013	1.1206
A to Z ↑	0.0184	0.0189	4.3050	3.2720
B to Z ↓	0.0081	0.0079	1.5130	1.1301
B to Z ↑	0.0155	0.0151	4.3239	3.2880
	X19_P10	**X20_P10**	**X19_P10**	**X20_P10**
A to Z ↓	0.0100	0.0107	0.8537	0.9161
A to Z ↑	0.0208	0.0186	3.2085	2.6046
B to Z ↓	0.0081	0.0082	0.8597	0.9239
B to Z ↑	0.0176	0.0155	3.2167	2.6161
	X23_P10	**X24_P10**	**X23_P10**	**X24_P10**
A to Z ↓	0.0410	0.0105	0.9436	0.7603
A to Z ↑	0.0572	0.0186	1.4217	2.1894
B to Z ↓	0.0389	0.0079	0.9444	0.7673
B to Z ↑	0.0565	0.0151	1.4216	2.1995
	X27_P10	**X29_P10**	**X27_P10**	**X29_P10**
A to Z ↓	0.0430	0.0097	0.7887	0.5675
A to Z ↑	0.0590	0.0195	1.1870	2.1513
B to Z ↓	0.0409	0.0077	0.7877	0.5714
B to Z ↑	0.0584	0.0171	1.1867	2.1569
	X31_P10	**X34_P10**	**X31_P10**	**X34_P10**
A to Z ↓	0.0106	0.0448	0.5680	0.6435
A to Z ↑	0.0187	0.0669	1.6419	0.9727
B to Z ↓	0.0081	0.0428	0.5736	0.6430
B to Z ↑	0.0153	0.0666	1.6498	0.9732
	X38_P10	**X39_P10**	**X38_P10**	**X39_P10**
A to Z ↓	0.0457	0.0099	0.5618	0.4319
A to Z ↑	0.0674	0.0200	0.8537	1.6138

B to Z ↓	0.0437	0.0078	0.5615	0.4360
B to Z ↑	0.0669	0.0168	0.8538	1.6182
	X46_P10	**X57_P10**	**X46_P10**	**X57_P10**
A to Z ↓	0.0528	0.0574	0.4207	0.3440
A to Z ↑	0.0703	0.0736	0.8465	0.6809
B to Z ↓	0.0513	0.0558	0.4204	0.3440
B to Z ↑	0.0710	0.0743	0.8458	0.6811

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P10	1.584e-06	1.000e-20
X4_P10	3.378e-06	1.000e-20
X8_P10	6.919e-06	1.000e-20
X9_P10	8.355e-06	1.000e-20
X12_P10	9.991e-06	1.000e-20
X16_P10	1.307e-05	1.000e-20
X19_P10	1.589e-05	1.000e-20
X20_P10	1.616e-05	1.000e-20
X23_P10	2.374e-05	1.000e-20
X24_P10	1.924e-05	1.000e-20
X27_P10	2.666e-05	1.000e-20
X29_P10	2.302e-05	1.000e-20
X31_P10	2.541e-05	1.000e-20
X34_P10	3.431e-05	1.000e-20
X38_P10	3.729e-05	1.000e-20
X39_P10	3.017e-05	1.000e-20
X46_P10	3.941e-05	1.000e-20
X57_P10	4.594e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P10	X4_P10	X8_P10	X9_P10
A (output stable)	8.517e-06	1.533e-05	6.168e-05	3.352e-05
B (output stable)	1.409e-05	2.599e-05	1.351e-04	5.986e-05
A to Z	3.582e-04	5.922e-04	1.192e-03	1.203e-03
B to Z	2.893e-04	4.585e-04	7.069e-04	9.333e-04
	X12_P10	X16_P10	X19_P10	X20_P10
A (output stable)	8.768e-05	1.218e-04	1.302e-04	1.434e-04
B (output stable)	1.771e-04	2.535e-04	2.951e-04	2.766e-04
A to Z	1.748e-03	2.367e-03	2.726e-03	2.931e-03
B to Z	1.139e-03	1.461e-03	1.866e-03	1.904e-03
	X23_P10	X24_P10	X27_P10	X29_P10
A (output stable)	1.680e-05	1.789e-04	1.692e-05	1.665e-04
B (output stable)	2.892e-05	3.579e-04	2.912e-05	3.459e-04
A to Z	5.416e-03	3.489e-03	6.072e-03	3.773e-03
B to Z	5.276e-03	2.188e-03	5.932e-03	2.627e-03
	X31_P10	X34_P10	X38_P10	X39_P10
A (output stable)	2.405e-04	1.775e-05	1.786e-05	2.536e-04
B (output stable)	4.799e-04	3.097e-05	3.107e-05	5.340e-04
A to Z	4.661e-03	8.169e-03	8.775e-03	5.170e-03
B to Z	2.956e-03	8.010e-03	8.613e-03	3.484e-03
	X46_P10	X57_P10		

A (output stable)	1.819e-05	1.834e-05		
B (output stable)	3.197e-05	3.225e-05		
A to Z	9.769e-03	1.195e-02		
B to Z	9.644e-03	1.182e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

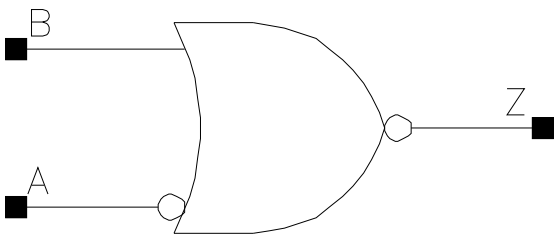
Pin Cycle (vdds)	X2_P10	X4_P10	X8_P10	X9_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P10	X16_P10	X19_P10	X20_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P10	X24_P10	X27_P10	X29_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P10	X34_P10	X38_P10	X39_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P10	X57_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.544	0.4352
X3_P10	0.800	0.544	0.4352
X4_P10	0.800	0.544	0.4352
X10_P10	1.600	0.544	0.8704
X14_P10	1.600	0.816	1.3056
X19_P10	1.600	0.816	1.3056
X29_P10	1.600	1.088	1.7408
X39_P10	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P10	X3_P10	X4_P10	X10_P10
A	0.0005	0.0005	0.0005	0.0009
B	0.0003	0.0004	0.0004	0.0010
	X14_P10	X19_P10	X29_P10	X39_P10
A	0.0009	0.0009	0.0014	0.0014
B	0.0016	0.0019	0.0030	0.0038

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	X3_P10	X2_P10	X3_P10
A to Z ↓	0.0324	0.0326	8.6091	6.3553
A to Z ↑	0.0307	0.0304	26.5428	22.2576
B to Z ↓	0.0104	0.0093	8.8555	6.5358

B to Z ↑	0.0217	0.0205	26.7079	22.3741
	X4_P10	**X10_P10**	**X4_P10**	**X10_P10**
A to Z ↓	0.0335	0.0325	4.8084	1.6664
A to Z ↑	0.0299	0.0287	15.8478	6.2528
B to Z ↓	0.0088	0.0081	4.9410	1.6712
B to Z ↑	0.0182	0.0182	15.9336	6.2883
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0396	0.0420	1.0757	0.8325
A to Z ↑	0.0329	0.0336	4.2902	3.1383
B to Z ↓	0.0075	0.0072	1.1572	0.8988
B to Z ↑	0.0171	0.0157	4.3186	3.1587
	X29_P10	**X39_P10**	**X29_P10**	**X39_P10**
A to Z ↓	0.0361	0.0419	0.5601	0.4220
A to Z ↑	0.0320	0.0341	2.1500	1.5900
B to Z ↓	0.0076	0.0071	0.5728	0.4471
B to Z ↑	0.0169	0.0154	2.1629	1.5997

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P10	2.942e-06	1.000e-20
X3_P10	3.472e-06	1.000e-20
X4_P10	4.466e-06	1.000e-20
X10_P10	1.243e-05	1.000e-20
X14_P10	1.480e-05	1.000e-20
X19_P10	1.972e-05	1.000e-20
X29_P10	3.030e-05	1.000e-20
X39_P10	3.779e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P10	X3_P10	X4_P10	X10_P10
A (output stable)	5.143e-04	5.608e-04	6.296e-04	1.284e-03
B (output stable)	1.441e-05	1.697e-05	2.360e-05	6.264e-05
A to Z	8.884e-04	9.827e-04	1.148e-03	2.628e-03
B to Z	2.700e-04	3.027e-04	3.628e-04	9.791e-04
	X14_P10	X19_P10	X29_P10	X39_P10
A (output stable)	1.926e-03	2.171e-03	3.279e-03	4.302e-03
B (output stable)	9.327e-05	1.254e-04	3.532e-04	2.378e-04
A to Z	3.847e-03	4.612e-03	7.335e-03	9.169e-03
B to Z	1.287e-03	1.568e-03	2.591e-03	3.081e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X2_P10	X3_P10	X4_P10	X10_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P10	X19_P10	X29_P10	X39_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

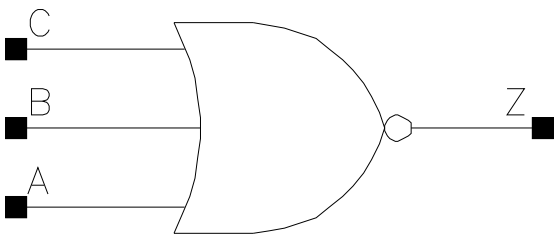
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.544	0.4352
X7_P10	0.800	0.952	0.7616
X11_P10	0.800	1.360	1.0880
X14_P10	0.800	1.768	1.4144
X21_P10	0.800	2.584	2.0672
X29_P10	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X11_P10	X14_P10
A	0.0005	0.0009	0.0015	0.0020
B	0.0005	0.0011	0.0014	0.0021
C	0.0005	0.0008	0.0013	0.0018
	X21_P10	X29_P10		
A	0.0031	0.0041		
B	0.0031	0.0041		
C	0.0026	0.0035		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0124	0.0124	4.6234	2.4194
A to Z ↑	0.0266	0.0275	19.4771	9.9441

B to Z ↓	0.0118	0.0117	4.6468	2.3405
B to Z ↑	0.0251	0.0273	19.4990	9.9542
C to Z ↓	0.0104	0.0088	4.6994	2.3581
C to Z ↑	0.0231	0.0191	19.5394	9.9633
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0124	0.0124	1.5132	1.1587
A to Z ↑	0.0280	0.0272	6.4853	4.7580
B to Z ↓	0.0118	0.0117	1.5302	1.1292
B to Z ↑	0.0253	0.0265	6.4906	4.7629
C to Z ↓	0.0095	0.0090	1.5207	1.1443
C to Z ↑	0.0209	0.0195	6.4983	4.7697
	X21_P10	**X29_P10**	**X21_P10**	**X29_P10**
A to Z ↓	0.0123	0.0124	0.7724	0.5801
A to Z ↑	0.0269	0.0270	3.1883	2.3959
B to Z ↓	0.0117	0.0118	0.7602	0.5744
B to Z ↑	0.0261	0.0261	3.1909	2.3980
C to Z ↓	0.0092	0.0093	0.7721	0.5833
C to Z ↑	0.0195	0.0197	3.1957	2.4020

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	2.776e-06	1.000e-20
X7_P10	5.335e-06	1.000e-20
X11_P10	8.160e-06	1.000e-20
X14_P10	1.098e-05	1.000e-20
X21_P10	1.618e-05	1.000e-20
X29_P10	2.144e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	1.837e-05	4.297e-05	8.083e-05	8.956e-05
B (output stable)	1.193e-05	3.832e-05	4.961e-05	7.549e-05
C (output stable)	3.692e-05	1.196e-04	1.478e-04	2.443e-04
A to Z	7.775e-04	1.586e-03	2.507e-03	3.270e-03
B to Z	6.355e-04	1.344e-03	1.922e-03	2.746e-03
C to Z	4.934e-04	8.050e-04	1.383e-03	1.713e-03
	X21_P10	X29_P10		
A (output stable)	1.323e-04	1.750e-04		
B (output stable)	1.116e-04	1.493e-04		
C (output stable)	3.545e-04	4.759e-04		
A to Z	4.838e-03	6.453e-03		
B to Z	4.026e-03	5.373e-03		
C to Z	2.566e-03	3.438e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

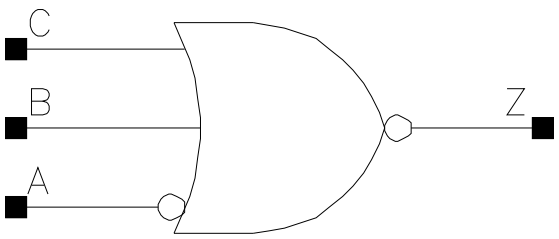
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P10	X29_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X7_P10	0.800	1.360	1.0880
X11_P10	0.800	1.632	1.3056
X14_P10	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X11_P10	X14_P10
A	0.0007	0.0007	0.0009	0.0013
B	0.0005	0.0010	0.0014	0.0019
C	0.0005	0.0009	0.0013	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0361	0.0318	4.5278	2.1183
A to Z ↑	0.0400	0.0395	19.5277	9.4631
B to Z ↓	0.0118	0.0117	4.6701	2.2075
B to Z ↑	0.0249	0.0267	19.5860	9.4898
C to Z ↓	0.0104	0.0092	4.7104	2.2186
C to Z ↑	0.0230	0.0201	19.6294	9.4963
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0389	0.0306	1.4943	1.1049

A to Z ↑	0.0436	0.0384	6.4910	4.8100
B to Z ↓	0.0118	0.0115	1.5314	1.1395
B to Z ↑	0.0251	0.0254	6.5093	4.8248
C to Z ↓	0.0093	0.0090	1.5231	1.1490
C to Z ↑	0.0205	0.0195	6.5154	4.8306

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	4.236e-06	1.000e-20
X7_P10	9.584e-06	1.000e-20
X11_P10	1.134e-05	1.000e-20
X14_P10	1.726e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	6.836e-04	1.169e-03	1.591e-03	2.138e-03
B (output stable)	1.446e-05	5.380e-05	6.556e-05	1.043e-04
C (output stable)	4.063e-05	1.520e-04	1.736e-04	2.718e-04
A to Z	1.497e-03	3.110e-03	4.251e-03	5.826e-03
B to Z	6.288e-04	1.397e-03	1.917e-03	2.607e-03
C to Z	4.877e-04	9.051e-04	1.345e-03	1.706e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

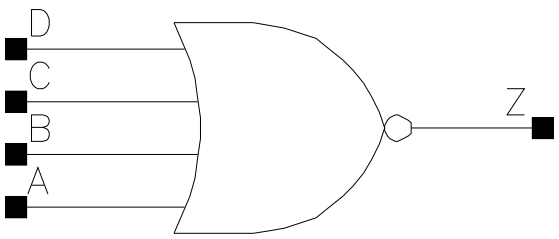
Pin Cycle (vdds)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.224	0.9792
X10_P10	0.800	1.632	1.3056
X14_P10	0.800	1.904	1.5232
X18_P10	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X18_P10
A	0.0005	0.0004	0.0005	0.0006
B	0.0005	0.0006	0.0006	0.0007
C	0.0005	0.0004	0.0005	0.0006
D	0.0005	0.0004	0.0005	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0408	0.0460	4.5013	2.1472
A to Z ↑	0.0666	0.0746	7.1566	3.4331
B to Z ↓	0.0399	0.0465	4.5018	2.1473
B to Z ↑	0.0670	0.0776	7.1475	3.4338
C to Z ↓	0.0420	0.0471	4.5000	2.1437
C to Z ↑	0.0712	0.0812	7.1586	3.4330

D to Z ↓	0.0419	0.0456	4.4938	2.1450
D to Z ↑	0.0729	0.0810	7.1497	3.4348
	X14_P10	**X18_P10**	**X14_P10**	**X18_P10**
A to Z ↓	0.0439	0.0458	1.4785	1.1762
A to Z ↑	0.0673	0.0652	2.3461	1.7857
B to Z ↓	0.0435	0.0443	1.4764	1.1749
B to Z ↑	0.0688	0.0653	2.3463	1.7851
C to Z ↓	0.0427	0.0455	1.4725	1.1704
C to Z ↑	0.0675	0.0662	2.3455	1.7824
D to Z ↓	0.0415	0.0437	1.4718	1.1718
D to Z ↑	0.0680	0.0661	2.3442	1.7850

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	8.015e-06	1.000e-20
X10_P10	1.181e-05	1.000e-20
X14_P10	1.759e-05	1.000e-20
X18_P10	2.288e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	2.819e-04	3.710e-04	4.588e-04	5.725e-04
B (output stable)	2.554e-04	3.539e-04	4.282e-04	5.217e-04
C (output stable)	3.018e-04	3.589e-04	4.693e-04	5.954e-04
D (output stable)	2.796e-04	3.324e-04	4.317e-04	5.417e-04
A to Z	1.998e-03	3.157e-03	4.430e-03	5.640e-03
B to Z	1.925e-03	3.098e-03	4.338e-03	5.517e-03
C to Z	2.077e-03	3.103e-03	4.151e-03	5.304e-03
D to Z	2.027e-03	3.034e-03	4.059e-03	5.167e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

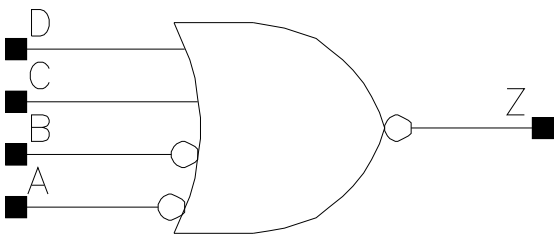
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	1.224	0.9792
X7_P10	0.800	1.496	1.1968
X11_P10	0.800	2.040	1.6320
X14_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P10	X7_P10	X11_P10	X14_P10
A	0.0007	0.0007	0.0013	0.0012
B	0.0007	0.0007	0.0012	0.0013
C	0.0005	0.0010	0.0014	0.0019
D	0.0005	0.0009	0.0013	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X7_P10	X4_P10	X7_P10
A to Z ↓	0.0355	0.0370	4.1892	2.1608
A to Z ↑	0.0498	0.0485	18.6711	9.5552
B to Z ↓	0.0328	0.0343	4.1844	2.1577
B to Z ↑	0.0497	0.0485	18.6808	9.5605
C to Z ↓	0.0121	0.0117	4.2726	2.2263
C to Z ↑	0.0263	0.0264	18.7103	9.5815

D to Z ↓	0.0107	0.0092	4.2932	2.2228
D to Z ↑	0.0242	0.0202	18.7253	9.5923
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0332	0.0366	1.4742	1.1114
A to Z ↑	0.0445	0.0486	6.4368	4.8013
B to Z ↓	0.0301	0.0341	1.4715	1.1097
B to Z ↑	0.0442	0.0492	6.4372	4.8013
C to Z ↓	0.0117	0.0118	1.5308	1.1420
C to Z ↑	0.0250	0.0257	6.4504	4.8104
D to Z ↓	0.0094	0.0091	1.5235	1.1401
D to Z ↑	0.0206	0.0199	6.4586	4.8164

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	6.229e-06	1.000e-20
X7_P10	8.181e-06	1.000e-20
X11_P10	1.316e-05	1.000e-20
X14_P10	1.512e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X7_P10	X11_P10	X14_P10
A (output stable)	5.636e-04	6.541e-04	1.046e-03	1.263e-03
B (output stable)	5.199e-04	6.108e-04	9.387e-04	1.181e-03
C (output stable)	4.295e-05	4.885e-05	7.354e-05	1.095e-04
D (output stable)	7.364e-05	1.477e-04	1.914e-04	2.994e-04
A to Z	2.474e-03	3.373e-03	5.115e-03	6.700e-03
B to Z	2.283e-03	3.183e-03	4.725e-03	6.358e-03
C to Z	7.147e-04	1.371e-03	1.925e-03	2.653e-03
D to Z	5.747e-04	8.995e-04	1.357e-03	1.758e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

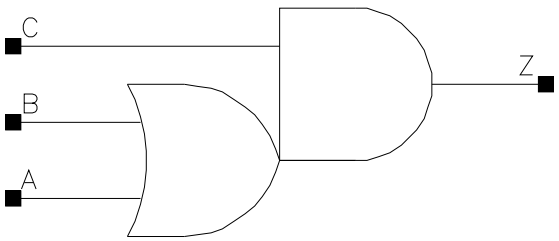
Pin Cycle (vdds)	X4_P10	X7_P10	X11_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.680	0.5440
X10_P10	0.800	0.952	0.7616
X19_P10	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0005	0.0006	0.0011
B	0.0006	0.0006	0.0013
C	0.0007	0.0008	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0353	0.0400	4.3141	2.1597
A to Z ↑	0.0286	0.0335	7.8865	3.4352
B to Z ↓	0.0356	0.0403	4.3192	2.1599
B to Z ↑	0.0266	0.0310	7.8747	3.4268
C to Z ↓	0.0318	0.0342	4.2718	2.1245
C to Z ↑	0.0276	0.0314	7.8772	3.4316
	X19_P10		**X19_P10**	
A to Z ↓	0.0413		1.1223	
A to Z ↑	0.0347		1.7464	

B to Z ↓	0.0417		1.1221	
B to Z ↑	0.0321		1.7440	
C to Z ↓	0.0341		1.1011	
C to Z ↑	0.0315		1.7421	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	6.735e-06	1.000e-20
X10_P10	1.123e-05	1.000e-20
X19_P10	2.108e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	3.604e-05	3.681e-05	7.867e-05
B (output stable)	4.130e-05	4.397e-05	8.703e-05
C (output stable)	2.934e-05	3.067e-05	5.945e-05
A to Z	1.354e-03	2.218e-03	4.488e-03
B to Z	1.234e-03	2.070e-03	4.204e-03
C to Z	1.499e-03	2.315e-03	4.576e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

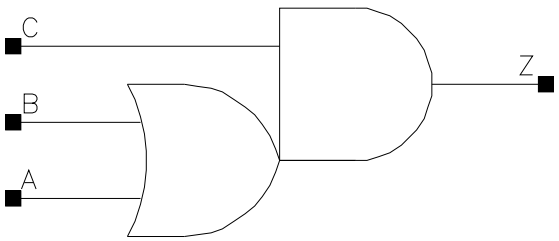
Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	1.360	1.0880
X14_P10	0.800	1.496	1.1968
X19_P10	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0006	0.0012	0.0012	0.0012
B	0.0006	0.0011	0.0011	0.0011
C	0.0006	0.0012	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0437	0.0360	4.2266	2.1357
A to Z ↑	0.0299	0.0272	6.8168	3.3602
B to Z ↓	0.0438	0.0356	4.2311	2.1389
B to Z ↑	0.0279	0.0251	6.8130	3.3615
C to Z ↓	0.0292	0.0237	4.1414	2.1056
C to Z ↑	0.0274	0.0241	6.8142	3.3593
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0403	0.0439	1.4844	1.1231

A to Z ↑	0.0300	0.0322	2.2725	1.7088
B to Z ↓	0.0400	0.0439	1.4857	1.1238
B to Z ↑	0.0280	0.0304	2.2672	1.7057
C to Z ↓	0.0268	0.0293	1.4535	1.0971
C to Z ↑	0.0272	0.0296	2.2679	1.7025

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	7.617e-06	1.000e-20
X10_P10	1.528e-05	1.000e-20
X14_P10	1.824e-05	1.000e-20
X19_P10	2.116e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.103e-05	2.347e-05	2.353e-05	2.343e-05
B (output stable)	1.391e-05	3.277e-05	3.269e-05	3.289e-05
C (output stable)	1.136e-04	2.279e-04	2.282e-04	2.289e-04
A to Z	1.744e-03	3.031e-03	3.909e-03	4.736e-03
B to Z	1.607e-03	2.704e-03	3.581e-03	4.418e-03
C to Z	1.401e-03	2.323e-03	3.149e-03	3.894e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

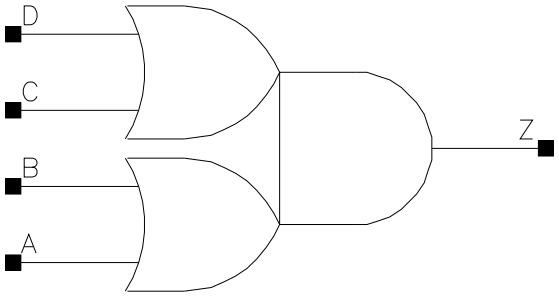
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.952	0.7616
X10_P10	0.800	1.088	0.8704
X14_P10	0.800	1.904	1.5232
X19_P10	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0004	0.0006	0.0011	0.0011
B	0.0004	0.0006	0.0011	0.0011
C	0.0004	0.0006	0.0012	0.0012
D	0.0004	0.0006	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0627	0.0489	4.3903	2.1844
A to Z ↑	0.0419	0.0352	6.8576	3.4242
B to Z ↓	0.0630	0.0491	4.3933	2.1846

B to Z ↑	0.0403	0.0333	6.8522	3.4196
C to Z ↓	0.0535	0.0433	4.3494	2.1703
C to Z ↑	0.0403	0.0348	6.8542	3.4221
D to Z ↓	0.0535	0.0431	4.3484	2.1714
D to Z ↑	0.0381	0.0325	6.8469	3.4188
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0463	0.0490	1.5058	1.1340
A to Z ↑	0.0332	0.0346	2.2772	1.7113
B to Z ↓	0.0445	0.0472	1.5063	1.1342
B to Z ↑	0.0305	0.0319	2.2719	1.7085
C to Z ↓	0.0394	0.0424	1.4959	1.1269
C to Z ↑	0.0319	0.0335	2.2751	1.7124
D to Z ↓	0.0371	0.0402	1.4967	1.1268
D to Z ↑	0.0288	0.0305	2.2707	1.7067

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	5.876e-06	1.000e-20
X10_P10	1.230e-05	1.000e-20
X14_P10	2.040e-05	1.000e-20
X19_P10	2.323e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.095e-05	1.695e-05	5.105e-05	5.083e-05
B (output stable)	1.367e-05	2.342e-05	9.775e-05	9.746e-05
C (output stable)	3.872e-05	4.246e-05	1.021e-04	1.018e-04
D (output stable)	4.262e-05	4.972e-05	1.467e-04	1.464e-04
A to Z	1.755e-03	2.711e-03	4.591e-03	5.270e-03
B to Z	1.677e-03	2.552e-03	4.131e-03	4.812e-03
C to Z	1.516e-03	2.397e-03	3.941e-03	4.615e-03
D to Z	1.441e-03	2.250e-03	3.468e-03	4.147e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

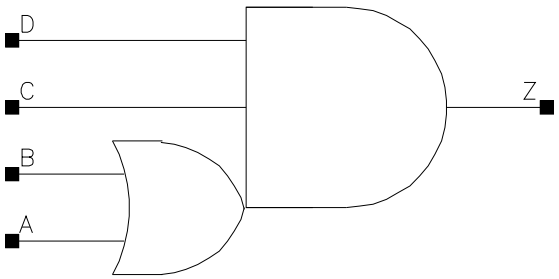
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	0.816	0.6528
X10_P10	0.800	1.088	0.8704
X14_P10	0.800	1.904	1.5232
X19_P10	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P10	X10_P10	X14_P10	X19_P10
A	0.0004	0.0008	0.0009	0.0011
B	0.0004	0.0006	0.0009	0.0011
C	0.0005	0.0006	0.0010	0.0012
D	0.0004	0.0006	0.0010	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X10_P10	X4_P10	X10_P10
A to Z ↓	0.0529	0.0499	4.8078	2.2216
A to Z ↑	0.0469	0.0478	7.2967	3.4827
B to Z ↓	0.0542	0.0462	4.8095	2.2213
B to Z ↑	0.0452	0.0415	7.2772	3.4730
C to Z ↓	0.0432	0.0378	4.6711	2.1766

C to Z ↑	0.0455	0.0427	7.2807	3.4718
D to Z ↓	0.0425	0.0366	4.6718	2.1749
D to Z ↑	0.0470	0.0438	7.2781	3.4717
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0490	0.0463	1.5082	1.1247
A to Z ↑	0.0456	0.0458	2.3220	1.7400
B to Z ↓	0.0468	0.0443	1.5095	1.1250
B to Z ↑	0.0415	0.0417	2.3135	1.7326
C to Z ↓	0.0394	0.0374	1.4780	1.1039
C to Z ↑	0.0429	0.0426	2.3129	1.7311
D to Z ↓	0.0374	0.0357	1.4740	1.1014
D to Z ↑	0.0428	0.0426	2.3126	1.7337

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	4.659e-06	1.000e-20
X10_P10	1.009e-05	1.000e-20
X14_P10	1.511e-05	1.000e-20
X19_P10	1.991e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X10_P10	X14_P10	X19_P10
A (output stable)	4.910e-05	7.344e-05	1.153e-04	1.252e-04
B (output stable)	4.673e-05	7.545e-05	1.248e-04	1.381e-04
C (output stable)	9.035e-06	1.812e-05	4.664e-05	5.213e-05
D (output stable)	1.629e-05	2.760e-05	1.085e-04	1.149e-04
A to Z	1.478e-03	2.680e-03	4.089e-03	5.074e-03
B to Z	1.416e-03	2.392e-03	3.709e-03	4.600e-03
C to Z	1.607e-03	2.720e-03	4.338e-03	5.315e-03
D to Z	1.544e-03	2.609e-03	4.041e-03	4.983e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

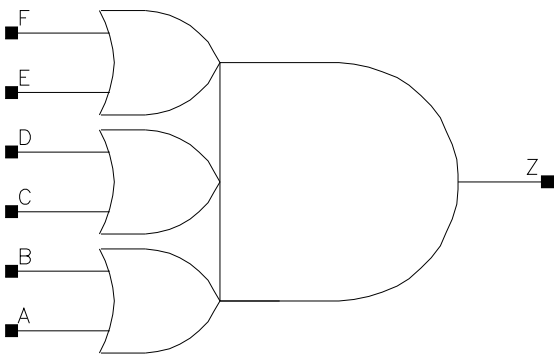
Pin Cycle (vdds)	X4_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	1.360	1.0880
X9_P10	0.800	1.496	1.1968
X19_P10	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P10	X9_P10	X19_P10
A	0.0004	0.0006	0.0010
B	0.0006	0.0008	0.0011
C	0.0004	0.0006	0.0010
D	0.0004	0.0005	0.0011
E	0.0004	0.0006	0.0010
F	0.0004	0.0006	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X9_P10	X4_P10	X9_P10
A to Z ↓	0.0745	0.0598	4.9001	2.4070
A to Z ↑	0.0559	0.0510	7.4803	3.6562
B to Z ↓	0.0769	0.0617	4.9010	2.4081
B to Z ↑	0.0556	0.0495	7.4814	3.6522
C to Z ↓	0.0684	0.0544	4.8653	2.3923
C to Z ↑	0.0557	0.0494	7.4896	3.6555
D to Z ↓	0.0684	0.0545	4.8653	2.3924
D to Z ↑	0.0530	0.0466	7.4802	3.6496
E to Z ↓	0.0584	0.0481	4.8079	2.3760
E to Z ↑	0.0505	0.0464	7.4798	3.6508
F to Z ↓	0.0595	0.0489	4.8119	2.3760
F to Z ↑	0.0488	0.0443	7.4721	3.6470
	X19_P10		X19_P10	
A to Z ↓	0.0578		1.1506	
A to Z ↑	0.0484		1.7387	
B to Z ↓	0.0587		1.1504	
B to Z ↑	0.0456		1.7336	
C to Z ↓	0.0533		1.1429	
C to Z ↑	0.0478		1.7384	
D to Z ↓	0.0540		1.1434	
D to Z ↑	0.0452		1.7332	
E to Z ↓	0.0469		1.1350	
E to Z ↑	0.0450		1.7358	
F to Z ↓	0.0477		1.1354	
F to Z ↑	0.0424		1.7322	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	5.792e-06	1.000e-20
X9_P10	1.200e-05	1.000e-20
X19_P10	2.386e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X9_P10	X19_P10
A (output stable)	1.001e-05	1.659e-05	2.999e-05
B (output stable)	1.497e-05	2.303e-05	3.883e-05
C (output stable)	2.105e-05	2.740e-05	5.333e-05
D (output stable)	2.441e-05	3.168e-05	6.295e-05
E (output stable)	7.086e-05	8.473e-05	1.582e-04
F (output stable)	6.924e-05	8.910e-05	1.643e-04
A to Z	2.093e-03	3.269e-03	6.333e-03
B to Z	2.042e-03	3.153e-03	6.056e-03
C to Z	1.895e-03	2.975e-03	5.813e-03
D to Z	1.814e-03	2.820e-03	5.527e-03
E to Z	1.632e-03	2.653e-03	5.186e-03
F to Z	1.570e-03	2.524e-03	4.928e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

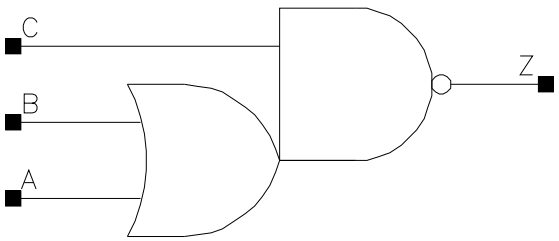
Pin Cycle (vdds)	X4_P10	X9_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.544	0.4352
X10_P10	0.800	1.360	1.0880
X20_P10	0.800	2.720	2.1760
X26_P10	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P10	X10_P10	X20_P10	X26_P10
A	0.0004	0.0014	0.0027	0.0037
B	0.0004	0.0013	0.0025	0.0034
C	0.0005	0.0015	0.0029	0.0040

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X10_P10**	**X3_P10**	**X10_P10**
A to Z ↓	0.0142	0.0155	8.6519	2.6778
A to Z ↑	0.0198	0.0203	15.9471	4.3505
B to Z ↓	0.0121	0.0126	8.5279	2.6984
B to Z ↑	0.0193	0.0176	15.9899	4.3697
C to Z ↓	0.0137	0.0142	7.8790	2.4627
C to Z ↑	0.0190	0.0176	8.5324	2.3488
	X20_P10	**X26_P10**	**X20_P10**	**X26_P10**
A to Z ↓	0.0162	0.0163	1.3647	1.0320

A to Z ↑	0.0210	0.0209	2.2142	1.6645
B to Z ↓	0.0131	0.0133	1.3746	1.0430
B to Z ↑	0.0185	0.0185	2.2229	1.6712
C to Z ↓	0.0150	0.0150	1.2553	0.9510
C to Z ↑	0.0181	0.0181	1.1602	0.8715

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	3.575e-06	1.000e-20
X10_P10	1.215e-05	1.000e-20
X20_P10	2.404e-05	1.000e-20
X26_P10	3.160e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X10_P10	X20_P10	X26_P10
A (output stable)	3.059e-05	1.197e-04	2.461e-04	3.166e-04
B (output stable)	3.655e-05	1.460e-04	3.113e-04	3.950e-04
C (output stable)	2.677e-05	9.451e-05	1.995e-04	2.627e-04
A to Z	5.116e-04	1.973e-03	4.094e-03	5.438e-03
B to Z	3.981e-04	1.348e-03	2.906e-03	3.882e-03
C to Z	6.438e-04	2.232e-03	4.702e-03	6.205e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

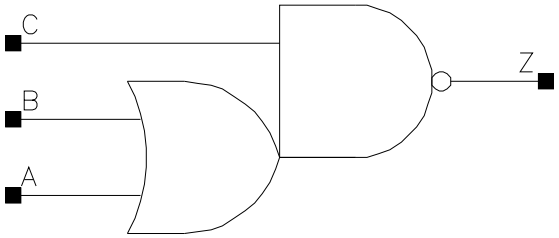
Pin Cycle (vdds)	X3_P10	X10_P10	X20_P10	X26_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X7_P10	0.800	0.952	0.7616
X10_P10	0.800	1.360	1.0880
X13_P10	0.800	1.904	1.5232
X26_P10	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X10_P10	X13_P10
A	0.0005	0.0010	0.0016	0.0020
B	0.0005	0.0010	0.0014	0.0018
C	0.0007	0.0009	0.0013	0.0018
	X26_P10			
A	0.0040			
B	0.0036			
C	0.0036			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X7_P10	X3_P10	X7_P10
A to Z ↓	0.0175	0.0156	7.4999	3.9018
A to Z ↑	0.0267	0.0234	12.6635	6.4565
B to Z ↓	0.0155	0.0133	7.5147	3.8159

B to Z ↑	0.0264	0.0228	12.6943	6.4782
C to Z ↓	0.0146	0.0123	7.0447	3.6050
C to Z ↑	0.0164	0.0137	6.9442	3.5841
	X10_P10	**X13_P10**	**X10_P10**	**X13_P10**
A to Z ↓	0.0152	0.0160	2.6324	1.9999
A to Z ↑	0.0226	0.0249	4.2776	3.2661
B to Z ↓	0.0130	0.0132	2.6253	2.0014
B to Z ↑	0.0220	0.0221	4.2903	3.2780
C to Z ↓	0.0120	0.0121	2.4616	1.8661
C to Z ↑	0.0130	0.0130	2.3697	1.7902
	X26_P10		**X26_P10**	
A to Z ↓	0.0159		1.0284	
A to Z ↑	0.0244		1.6432	
B to Z ↓	0.0129		1.0255	
B to Z ↑	0.0216		1.6501	
C to Z ↓	0.0122		0.9590	
C to Z ↑	0.0127		0.9013	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	4.789e-06	1.000e-20
X7_P10	8.494e-06	1.000e-20
X10_P10	1.238e-05	1.000e-20
X13_P10	1.667e-05	1.000e-20
X26_P10	3.192e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X7_P10	X10_P10	X13_P10
A (output stable)	1.303e-05	2.364e-05	3.491e-05	6.541e-05
B (output stable)	1.588e-05	3.119e-05	4.593e-05	1.035e-04
C (output stable)	1.166e-04	2.269e-04	2.991e-04	4.368e-04
A to Z	1.012e-03	1.618e-03	2.340e-03	3.440e-03
B to Z	8.468e-04	1.301e-03	1.849e-03	2.504e-03
C to Z	6.211e-04	1.004e-03	1.408e-03	1.971e-03
	X26_P10			
A (output stable)	1.255e-04			
B (output stable)	1.921e-04			
C (output stable)	8.039e-04			
A to Z	6.645e-03			
B to Z	4.773e-03			
C to Z	3.781e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P10	X7_P10	X10_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

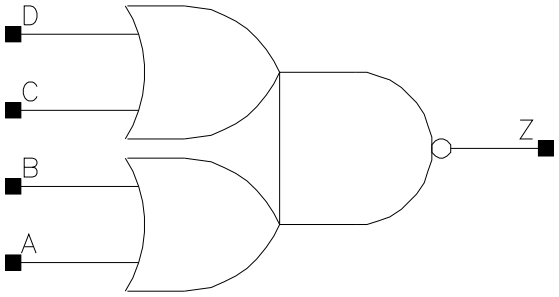
	X26_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X6_P10	0.800	1.360	1.0880
X8_P10	0.800	1.768	1.4144
X11_P10	0.800	2.448	1.9584
X24_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X8_P10	X11_P10
A	0.0005	0.0010	0.0015	0.0019
B	0.0005	0.0009	0.0013	0.0017
C	0.0005	0.0009	0.0014	0.0018
D	0.0004	0.0008	0.0012	0.0016
	X24_P10			
A	0.0041			
B	0.0037			
C	0.0038			
D	0.0035			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X6_P10**	**X3_P10**	**X6_P10**
A to Z ↓	0.0164	0.0191	7.0406	3.8477
A to Z ↑	0.0294	0.0292	15.8296	6.8160
B to Z ↓	0.0149	0.0165	6.9997	3.8540
B to Z ↑	0.0291	0.0264	15.8495	6.8343
C to Z ↓	0.0137	0.0166	7.1260	3.8614
C to Z ↑	0.0205	0.0221	15.8650	6.8390
D to Z ↓	0.0119	0.0132	7.0924	3.8908
D to Z ↑	0.0199	0.0181	15.8965	6.8661
	X8_P10	**X11_P10**	**X8_P10**	**X11_P10**
A to Z ↓	0.0183	0.0185	2.6259	1.9856
A to Z ↑	0.0273	0.0276	4.5597	3.4200
B to Z ↓	0.0160	0.0158	2.6430	1.9871
B to Z ↑	0.0253	0.0252	4.5749	3.4318
C to Z ↓	0.0162	0.0166	2.6456	2.0005
C to Z ↑	0.0205	0.0213	4.5526	3.4379
D to Z ↓	0.0135	0.0134	2.6801	2.0072
D to Z ↑	0.0179	0.0179	4.5768	3.4552
	X24_P10		**X24_P10**	
A to Z ↓	0.0185		0.9618	
A to Z ↑	0.0275		1.6468	
B to Z ↓	0.0158		0.9562	
B to Z ↑	0.0254		1.6519	
C to Z ↓	0.0169		0.9697	
C to Z ↑	0.0211		1.6477	
D to Z ↓	0.0136		0.9673	
D to Z ↑	0.0181		1.6562	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	4.580e-06	1.000e-20
X6_P10	1.002e-05	1.000e-20
X8_P10	1.423e-05	1.000e-20
X11_P10	1.923e-05	1.000e-20
X24_P10	3.864e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X6_P10	X8_P10	X11_P10
A (output stable)	1.495e-05	5.270e-05	6.711e-05	9.418e-05
B (output stable)	2.016e-05	9.811e-05	1.155e-04	1.746e-04
C (output stable)	3.989e-05	1.038e-04	1.323e-04	1.815e-04
D (output stable)	4.782e-05	1.491e-04	1.814e-04	2.599e-04
A to Z	9.267e-04	2.192e-03	3.013e-03	4.077e-03
B to Z	7.902e-04	1.715e-03	2.361e-03	3.180e-03
C to Z	5.794e-04	1.552e-03	2.116e-03	2.953e-03
D to Z	4.667e-04	1.074e-03	1.520e-03	2.078e-03
	X24_P10			
A (output stable)	1.938e-04			
B (output stable)	3.391e-04			
C (output stable)	3.480e-04			
D (output stable)	4.877e-04			

A to Z	8.389e-03			
B to Z	6.567e-03			
C to Z	6.077e-03			
D to Z	4.336e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

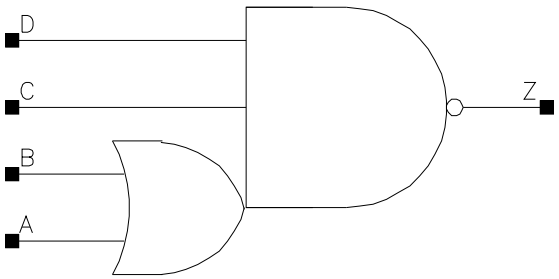
Pin Cycle (vdds)	X3_P10	X6_P10	X8_P10	X11_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X6_P10	0.800	1.360	1.0880
X12_P10	0.800	2.448	1.9584
X18_P10	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X12_P10	X18_P10
A	0.0007	0.0009	0.0018	0.0027
B	0.0005	0.0009	0.0017	0.0025
C	0.0005	0.0010	0.0019	0.0030
D	0.0005	0.0010	0.0019	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0257	0.0212	10.7369	5.6857
A to Z ↑	0.0294	0.0238	13.0012	6.5284
B to Z ↓	0.0191	0.0170	10.6979	5.7016
B to Z ↑	0.0243	0.0208	13.0036	6.5519
C to Z ↓	0.0214	0.0213	10.1045	5.3729

C to Z ↑	0.0226	0.0216	6.7528	3.4569
D to Z ↓	0.0229	0.0207	10.1292	5.3857
D to Z ↑	0.0219	0.0198	6.8837	3.4621
	X12_P10	**X18_P10**	**X12_P10**	**X18_P10**
A to Z ↓	0.0215	0.0217	2.9455	1.9884
A to Z ↑	0.0235	0.0234	3.2727	2.1907
B to Z ↓	0.0172	0.0175	2.9563	1.9976
B to Z ↑	0.0204	0.0206	3.2868	2.2004
C to Z ↓	0.0210	0.0212	2.7834	1.8802
C to Z ↑	0.0211	0.0210	1.7545	1.1595
D to Z ↓	0.0207	0.0207	2.7908	1.8849
D to Z ↑	0.0193	0.0193	1.7500	1.1687

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	3.903e-06	1.000e-20
X6_P10	7.275e-06	1.000e-20
X12_P10	1.366e-05	1.000e-20
X18_P10	2.006e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X6_P10	X12_P10	X18_P10
A (output stable)	7.136e-05	1.454e-04	2.722e-04	3.797e-04
B (output stable)	7.406e-05	1.575e-04	2.828e-04	4.016e-04
C (output stable)	1.592e-05	5.022e-05	9.289e-05	1.481e-04
D (output stable)	2.664e-05	1.083e-04	1.882e-04	2.937e-04
A to Z	1.044e-03	1.631e-03	3.201e-03	4.767e-03
B to Z	7.525e-04	1.178e-03	2.278e-03	3.439e-03
C to Z	1.176e-03	2.167e-03	4.111e-03	6.160e-03
D to Z	1.081e-03	1.817e-03	3.469e-03	5.146e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

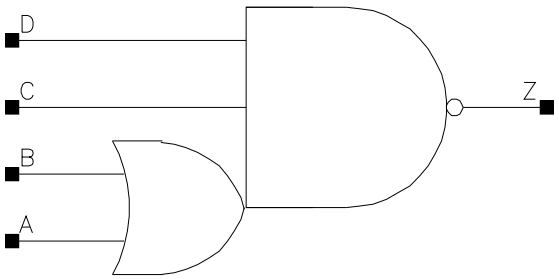
Pin Cycle (vdds)	X3_P10	X6_P10	X12_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X6_P10	0.800	1.360	1.0880
X9_P10	0.800	1.768	1.4144
X12_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X9_P10	X12_P10
A	0.0005	0.0010	0.0016	0.0020
B	0.0005	0.0009	0.0014	0.0021
C	0.0005	0.0009	0.0014	0.0019
D	0.0005	0.0009	0.0013	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0217	0.0224	11.5916	5.6435
A to Z ↑	0.0281	0.0298	13.3150	6.5205
B to Z ↓	0.0190	0.0188	11.4448	5.6630
B to Z ↑	0.0278	0.0275	13.3448	6.5411
C to Z ↓	0.0170	0.0181	10.9396	5.3682

C to Z ↑	0.0176	0.0178	7.2499	3.5515
D to Z ↓	0.0174	0.0168	10.9776	5.3878
D to Z ↑	0.0159	0.0151	7.3105	3.5676
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0226	0.0226	3.8721	2.9322
A to Z ↑	0.0290	0.0295	4.3192	3.3288
B to Z ↓	0.0192	0.0191	3.8768	2.9373
B to Z ↑	0.0270	0.0278	4.3313	3.3412
C to Z ↓	0.0179	0.0182	3.6771	2.7844
C to Z ↑	0.0173	0.0174	2.3516	1.7786
D to Z ↓	0.0171	0.0168	3.6907	2.7951
D to Z ↑	0.0148	0.0146	2.3650	1.7925

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	3.493e-06	1.000e-20
X6_P10	7.374e-06	1.000e-20
X9_P10	1.027e-05	1.000e-20
X12_P10	1.383e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	9.467e-06	2.136e-05	3.436e-05	4.348e-05
B (output stable)	1.022e-05	3.099e-05	4.423e-05	5.977e-05
C (output stable)	2.812e-05	6.499e-05	9.848e-05	1.260e-04
D (output stable)	5.487e-05	2.088e-04	2.311e-04	3.779e-04
A to Z	1.037e-03	2.275e-03	3.315e-03	4.439e-03
B to Z	8.743e-04	1.791e-03	2.603e-03	3.477e-03
C to Z	6.776e-04	1.523e-03	2.158e-03	2.943e-03
D to Z	5.793e-04	1.206e-03	1.749e-03	2.307e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

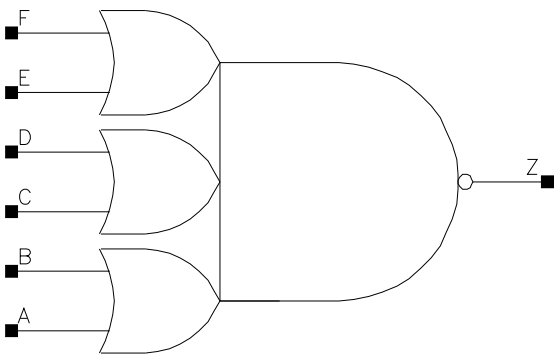
Pin Cycle (vdds)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.224	0.9792
X3_P10	0.800	1.224	0.9792
X5_P10	0.800	2.040	1.6320
X8_P10	0.800	2.720	2.1760
X10_P10	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P10	X3_P10	X5_P10	X8_P10
A	0.0004	0.0005	0.0010	0.0016
B	0.0004	0.0005	0.0009	0.0014
C	0.0004	0.0005	0.0010	0.0015
D	0.0005	0.0005	0.0009	0.0013

E	0.0004	0.0005	0.0009	0.0014
F	0.0004	0.0004	0.0009	0.0013
	X10_P10			
A	0.0021			
B	0.0019			
C	0.0019			
D	0.0018			
E	0.0018			
F	0.0017			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X3_P10**	**X2_P10**	**X3_P10**
A to Z ↓	0.0284	0.0271	12.7592	9.7642
A to Z ↑	0.0406	0.0350	18.3286	12.5759
B to Z ↓	0.0266	0.0252	12.7822	9.8063
B to Z ↑	0.0411	0.0356	18.3554	12.5955
C to Z ↓	0.0274	0.0266	12.8075	9.7879
C to Z ↑	0.0354	0.0313	18.3305	12.7127
D to Z ↓	0.0264	0.0239	12.8851	9.8696
D to Z ↑	0.0371	0.0310	18.3841	12.7274
E to Z ↓	0.0234	0.0227	12.8442	9.8132
E to Z ↑	0.0279	0.0247	18.3332	12.7292
F to Z ↓	0.0218	0.0204	12.8985	9.8919
F to Z ↑	0.0285	0.0245	18.3845	12.7609
	X5_P10	**X8_P10**	**X5_P10**	**X8_P10**
A to Z ↓	0.0285	0.0281	5.1446	3.5068
A to Z ↑	0.0363	0.0351	6.5291	4.3313
B to Z ↓	0.0252	0.0250	5.1629	3.5093
B to Z ↑	0.0340	0.0337	6.5428	4.3407
C to Z ↓	0.0259	0.0266	5.1658	3.5240
C to Z ↑	0.0306	0.0302	6.5702	4.4005
D to Z ↓	0.0227	0.0233	5.1761	3.5222
D to Z ↑	0.0287	0.0293	6.5883	4.4095
E to Z ↓	0.0237	0.0235	5.1878	3.5353
E to Z ↑	0.0250	0.0241	6.5753	4.4093
F to Z ↓	0.0200	0.0201	5.2022	3.5229
F to Z ↑	0.0223	0.0226	6.5973	4.4258
	X10_P10		**X10_P10**	
A to Z ↓	0.0286		2.6531	
A to Z ↑	0.0356		3.2804	
B to Z ↓	0.0253		2.6567	
B to Z ↑	0.0337		3.2881	
C to Z ↓	0.0262		2.6608	
C to Z ↑	0.0303		3.3230	
D to Z ↓	0.0230		2.6653	
D to Z ↑	0.0287		3.3321	
E to Z ↓	0.0238		2.6680	
E to Z ↑	0.0245		3.3169	
F to Z ↓	0.0205		2.6786	
F to Z ↑	0.0225		3.3300	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P10	4.239e-06	1.000e-20
X3_P10	6.412e-06	1.000e-20
X5_P10	1.212e-05	1.000e-20
X8_P10	1.716e-05	1.000e-20
X10_P10	2.287e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P10	X3_P10	X5_P10	X8_P10
A (output stable)	1.295e-05	1.634e-05	4.752e-05	6.448e-05
B (output stable)	1.608e-05	2.127e-05	7.735e-05	9.694e-05
C (output stable)	2.393e-05	2.922e-05	7.346e-05	9.836e-05
D (output stable)	2.750e-05	3.321e-05	1.038e-04	1.262e-04
E (output stable)	7.558e-05	9.268e-05	1.635e-04	2.465e-04
F (output stable)	8.025e-05	9.973e-05	1.936e-04	2.772e-04
A to Z	1.300e-03	1.583e-03	3.217e-03	4.616e-03
B to Z	1.192e-03	1.432e-03	2.730e-03	3.942e-03
C to Z	1.070e-03	1.322e-03	2.546e-03	3.725e-03
D to Z	9.827e-04	1.162e-03	2.129e-03	3.175e-03
E to Z	8.042e-04	9.973e-04	2.027e-03	2.860e-03
F to Z	7.135e-04	8.583e-04	1.601e-03	2.336e-03
	X10_P10			
A (output stable)	9.156e-05			
B (output stable)	1.447e-04			
C (output stable)	1.360e-04			
D (output stable)	1.919e-04			
E (output stable)	3.135e-04			
F (output stable)	3.632e-04			
A to Z	6.251e-03			
B to Z	5.302e-03			
C to Z	4.980e-03			
D to Z	4.179e-03			
E to Z	3.917e-03			
F to Z	3.154e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X2_P10	X3_P10	X5_P10	X8_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P10			

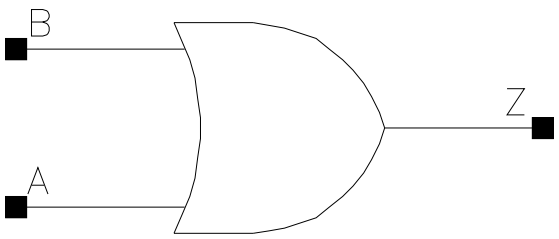
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.544	0.4352
X9_P10	0.800	0.680	0.5440
X19_P10	0.800	1.360	1.0880
X29_P10	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10	X29_P10
A	0.0005	0.0006	0.0011	0.0011
B	0.0004	0.0006	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X9_P10**	**X5_P10**	**X9_P10**
A to Z ↓	0.0467	0.0399	4.5975	2.3124
A to Z ↑	0.0276	0.0284	7.1014	3.5674
B to Z ↓	0.0463	0.0392	4.5937	2.3123
B to Z ↑	0.0265	0.0266	7.1103	3.5688
	X19_P10	**X29_P10**	**X19_P10**	**X29_P10**
A to Z ↓	0.0401	0.0477	1.1061	0.7573
A to Z ↑	0.0279	0.0319	1.6973	1.1392
B to Z ↓	0.0376	0.0454	1.1064	0.7585
B to Z ↑	0.0254	0.0295	1.6968	1.1381

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	4.924e-06	1.000e-20
X9_P10	9.322e-06	1.000e-20
X19_P10	1.903e-05	1.000e-20
X29_P10	2.448e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10	X29_P10
A (output stable)	9.003e-06	1.709e-05	6.454e-05	6.468e-05
B (output stable)	1.666e-05	2.894e-05	1.464e-04	1.468e-04
A to Z	1.270e-03	2.014e-03	4.232e-03	5.978e-03
B to Z	1.191e-03	1.870e-03	3.742e-03	5.491e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

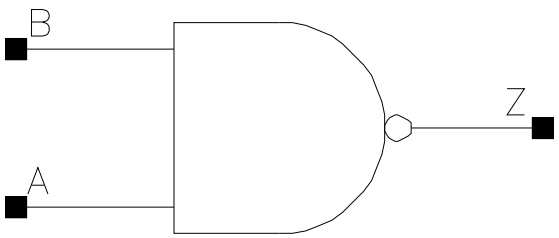
Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10	X29_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X9_P10	0.800	0.952	0.7616
X14_P10	0.800	1.088	0.8704
X18_P10	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P10	X9_P10	X14_P10	X18_P10
A	0.0007	0.0006	0.0006	0.0006
B	0.0006	0.0007	0.0007	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X9_P10**	**X5_P10**	**X9_P10**
A to Z ↓	0.0361	0.0419	4.1309	2.2682
A to Z ↑	0.0385	0.0425	6.7905	3.5737
B to Z ↓	0.0372	0.0438	4.1266	2.2687
B to Z ↑	0.0364	0.0411	6.7951	3.5687
	X14_P10	**X18_P10**	**X14_P10**	**X18_P10**
A to Z ↓	0.0465	0.0492	1.5630	1.1869
A to Z ↑	0.0456	0.0467	2.3724	1.8211
B to Z ↓	0.0485	0.0509	1.5645	1.1868
B to Z ↑	0.0443	0.0453	2.3739	1.8206

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	1.087e-05	1.000e-20
X9_P10	1.322e-05	1.000e-20
X14_P10	1.601e-05	1.000e-20
X18_P10	1.745e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X9_P10	X14_P10	X18_P10
A (output stable)	1.012e-05	9.454e-06	9.572e-06	1.000e-05
B (output stable)	2.153e-05	1.955e-05	1.963e-05	1.857e-05
A to Z	2.284e-03	2.943e-03	3.794e-03	4.215e-03
B to Z	2.185e-03	2.858e-03	3.709e-03	4.130e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

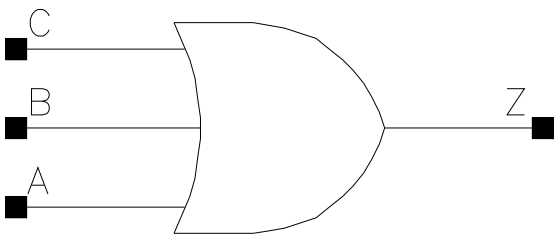
Pin Cycle (vdds)	X5_P10	X9_P10	X14_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.680	0.5440
X10_P10	0.800	0.952	0.7616
X14_P10	0.800	1.496	1.1968
X19_P10	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0004	0.0007	0.0010	0.0017
B	0.0004	0.0006	0.0012	0.0016
C	0.0005	0.0006	0.0011	0.0017

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0632	0.0548	4.7729	2.2591
A to Z ↑	0.0320	0.0275	7.1367	3.3858
B to Z ↓	0.0615	0.0533	4.7730	2.2582
B to Z ↑	0.0315	0.0264	7.1286	3.3810
C to Z ↓	0.0607	0.0512	4.7768	2.2620
C to Z ↑	0.0304	0.0248	7.1293	3.3782
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0508	0.0489	1.5073	1.1469

A to Z ↑	0.0253	0.0250	2.2971	1.7526
B to Z ↓	0.0509	0.0467	1.5078	1.1479
B to Z ↑	0.0242	0.0242	2.2950	1.7483
C to Z ↓	0.0441	0.0428	1.5057	1.1483
C to Z ↑	0.0220	0.0221	2.2906	1.7473

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	4.582e-06	1.000e-20
X10_P10	9.295e-06	1.000e-20
X14_P10	1.552e-05	1.000e-20
X19_P10	2.091e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.104e-05	2.083e-05	4.296e-05	8.128e-05
B (output stable)	5.839e-06	1.414e-05	3.979e-05	4.975e-05
C (output stable)	1.861e-05	4.076e-05	1.322e-04	1.451e-04
A to Z	1.515e-03	2.466e-03	4.051e-03	5.743e-03
B to Z	1.426e-03	2.311e-03	3.804e-03	5.159e-03
C to Z	1.352e-03	2.161e-03	3.288e-03	4.597e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

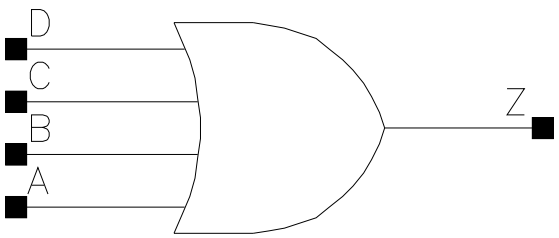
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	1.224	0.9792
X8_P10	0.800	1.496	1.1968
X12_P10	0.800	2.176	1.7408
X15_P10	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X12_P10	X15_P10
A	0.0004	0.0006	0.0011	0.0012
B	0.0004	0.0006	0.0009	0.0012
C	0.0004	0.0006	0.0010	0.0012
D	0.0004	0.0007	0.0010	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
A to Z ↓	0.0482	0.0449	7.3648	3.8703
A to Z ↑	0.0286	0.0287	6.6666	3.4921
B to Z ↓	0.0492	0.0454	7.3602	3.8733
B to Z ↑	0.0276	0.0274	6.6617	3.4935
C to Z ↓	0.0517	0.0438	7.3811	3.8674
C to Z ↑	0.0296	0.0278	6.7909	3.5049

D to Z ↓	0.0532	0.0447	7.3789	3.8683
D to Z ↑	0.0289	0.0267	6.7956	3.5031
	X12_P10	**X15_P10**	**X12_P10**	**X15_P10**
A to Z ↓	0.0461	0.0458	2.6691	2.0013
A to Z ↑	0.0294	0.0276	2.2657	1.7271
B to Z ↓	0.0446	0.0435	2.6688	2.0010
B to Z ↑	0.0278	0.0255	2.2646	1.7237
C to Z ↓	0.0447	0.0434	2.6643	1.9972
C to Z ↑	0.0280	0.0260	2.2605	1.7337
D to Z ↓	0.0432	0.0415	2.6646	1.9979
D to Z ↑	0.0263	0.0241	2.2596	1.7304

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	5.702e-06	1.000e-20
X8_P10	1.176e-05	1.000e-20
X12_P10	1.489e-05	1.000e-20
X15_P10	2.184e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	3.303e-04	5.830e-04	9.063e-04	1.232e-03
B (output stable)	3.063e-04	5.309e-04	8.004e-04	1.072e-03
C (output stable)	3.241e-04	5.534e-04	8.202e-04	1.116e-03
D (output stable)	3.011e-04	5.017e-04	7.125e-04	9.767e-04
A to Z	1.389e-03	2.758e-03	3.938e-03	5.198e-03
B to Z	1.325e-03	2.625e-03	3.637e-03	4.711e-03
C to Z	1.412e-03	2.432e-03	3.497e-03	4.397e-03
D to Z	1.354e-03	2.304e-03	3.196e-03	3.976e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

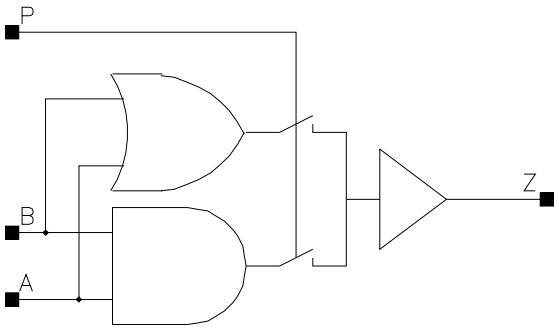
Pin Cycle (vdds)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.952	0.7616
X10_P10	1.600	0.816	1.3056
X14_P10	1.600	1.224	1.9584
X19_P10	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0009	0.0010	0.0020	0.0020
B	0.0008	0.0011	0.0021	0.0021
P	0.0004	0.0006	0.0012	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0579	0.0513	4.6864	2.1723
A to Z ↑	0.0319	0.0367	7.1493	3.4114
B to Z ↓	0.0573	0.0521	4.7053	2.1806
B to Z ↑	0.0332	0.0384	7.1552	3.4152
P to Z ↓	0.0513	0.0485	4.6999	2.1816
P to Z ↑	0.0315	0.0370	7.1478	3.4150
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**

A to Z ↓	0.0470	0.0502	1.4884	1.0998
A to Z ↑	0.0348	0.0366	2.3215	1.7346
B to Z ↓	0.0441	0.0478	1.4999	1.1080
B to Z ↑	0.0342	0.0366	2.3224	1.7371
P to Z ↓	0.0421	0.0461	1.5049	1.1101
P to Z ↑	0.0340	0.0365	2.3215	1.7350

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	5.999e-06	1.000e-20
X10_P10	1.328e-05	1.000e-20
X14_P10	2.156e-05	1.000e-20
X19_P10	2.491e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	2.330e-05	3.453e-05	1.024e-04	9.651e-05
B (output stable)	3.149e-05	5.333e-05	2.190e-04	2.096e-04
P (output stable)	8.746e-05	1.528e-04	2.813e-04	2.671e-04
A to Z	1.539e-03	2.879e-03	4.647e-03	5.488e-03
B to Z	1.492e-03	2.839e-03	4.324e-03	5.195e-03
P to Z	1.328e-03	2.620e-03	4.145e-03	5.046e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

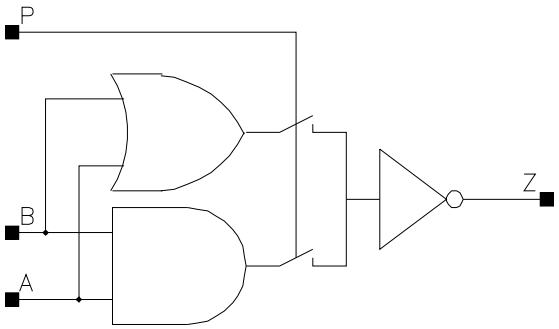
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.600	0.544	0.8704
X10_P10	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P10	X10_P10
A	0.0010	0.0019
B	0.0009	0.0017
P	0.0006	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0186	0.0175	7.3828	3.8425
A to Z ↑	0.0298	0.0277	12.6943	6.4149
B to Z ↓	0.0195	0.0167	7.3236	3.8560
B to Z ↑	0.0295	0.0244	12.6690	6.4731
P to Z ↓	0.0192	0.0154	7.4712	3.8837
P to Z ↑	0.0272	0.0213	12.7567	6.4459

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	6.112e-06	1.000e-20
X10_P10	1.130e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10
A (output stable)	3.320e-05	1.026e-04
B (output stable)	4.828e-05	2.115e-04
P (output stable)	1.311e-04	3.013e-04
A to Z	1.151e-03	2.047e-03
B to Z	1.077e-03	1.681e-03
P to Z	8.959e-04	1.440e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

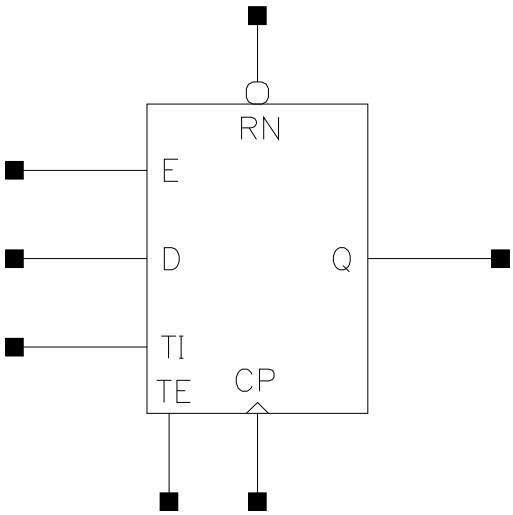
Pin Cycle (vdds)	X5_P10	X10_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.600	2.992	4.7872
X10_P10	1.600	3.128	5.0048
X19_P10	1.600	3.264	5.2224
X23_P10	1.600	3.264	5.2224
X29_P10	1.600	3.536	5.6576
X34_P10	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10	X23_P10
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0011	0.0011	0.0011	0.0011

RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P10	X34_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0011	0.0011		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
CP to Q ↓	0.0720	0.1179	4.2805	2.1247
CP to Q ↑	0.1006	0.1604	6.7588	3.4053
RN to Q ↓	0.0615	0.1151	4.3008	2.1261
	X19_P10	**X23_P10**	**X19_P10**	**X23_P10**
CP to Q ↓	0.1279	0.1288	1.0916	0.8155
CP to Q ↑	0.1663	0.1642	1.7138	1.6868
RN to Q ↓	0.1173	0.1186	1.0875	0.8123
	X29_P10	**X34_P10**	**X29_P10**	**X34_P10**
CP to Q ↓	0.1081	0.1073	0.7142	0.5593
CP to Q ↑	0.1325	0.1337	1.1370	1.1342
RN to Q ↓	0.0999	0.0989	0.7146	0.5595

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P10	X10_P10	X19_P10	X23_P10
CP ↓	min_pulse_width to CP	0.0968	0.0968	0.0961	0.0961
CP ↑	min_pulse_width to CP	0.0623	0.0624	0.0624	0.0624
D ↓	hold_rising to CP	-0.0654	-0.0680	-0.0680	-0.0680
D ↑	hold_rising to CP	-0.0240	-0.0267	-0.0267	-0.0267
D ↓	setup_rising to CP	0.1150	0.1155	0.1123	0.1123
D ↑	setup_rising to CP	0.0568	0.0542	0.0542	0.0542
E ↓	hold_rising to CP	-0.0626	-0.0653	-0.0653	-0.0653
E ↑	hold_rising to CP	-0.0267	-0.0267	-0.0267	-0.0267
E ↓	setup_rising to CP	0.1588	0.1588	0.1588	0.1588
E ↑	setup_rising to CP	0.1150	0.1150	0.1150	0.1150
RN ↓	min_pulse_width to RN	0.0806	0.0762	0.0784	0.0806
RN ↑	recovery_rising to CP	-0.0018	-0.0038	-0.0038	-0.0038
RN ↑	removal_rising to CP	0.0167	0.0167	0.0167	0.0167
TE ↓	hold_rising to CP	-0.0387	-0.0387	-0.0387	-0.0387

TE ↑	hold_rising to CP	-0.0191	-0.0191	-0.0191	-0.0191
TE ↓	setup_rising to CP	0.0900	0.0900	0.0905	0.0905
TE ↑	setup_rising to CP	0.1203	0.1177	0.1177	0.1177
TI ↓	hold_rising to CP	-0.0684	-0.0681	-0.0681	-0.0684
TI ↑	hold_rising to CP	-0.0162	-0.0205	-0.0205	-0.0205
TI ↓	setup_rising to CP	0.1140	0.1127	0.1127	0.1127
TI ↑	setup_rising to CP	0.0466	0.0469	0.0469	0.0466
		X29_P10	X34_P10		
CP ↓	min_pulse_width to CP	0.0968	0.0968		
CP ↑	min_pulse_width to CP	0.0623	0.0623		
D ↓	hold_rising to CP	-0.0680	-0.0680		
D ↑	hold_rising to CP	-0.0240	-0.0240		
D ↓	setup_rising to CP	0.1150	0.1150		
D ↑	setup_rising to CP	0.0542	0.0542		
E ↓	hold_rising to CP	-0.0626	-0.0626		
E ↑	hold_rising to CP	-0.0267	-0.0267		
E ↓	setup_rising to CP	0.1588	0.1588		
E ↑	setup_rising to CP	0.1150	0.1150		
RN ↓	min_pulse_width to RN	0.0828	0.0828		
RN ↑	recovery_rising to CP	-0.0044	-0.0044		
RN ↑	removal_rising to CP	0.0167	0.0167		
TE ↓	hold_rising to CP	-0.0354	-0.0354		
TE ↑	hold_rising to CP	-0.0191	-0.0191		
TE ↓	setup_rising to CP	0.0932	0.0900		
TE ↑	setup_rising to CP	0.1203	0.1203		
TI ↓	hold_rising to CP	-0.0684	-0.0684		
TI ↑	hold_rising to CP	-0.0169	-0.0169		
TI ↓	setup_rising to CP	0.1186	0.1186		
TI ↑	setup_rising to CP	0.0466	0.0466		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	2.425e-05	1.000e-20
X10_P10	2.960e-05	1.000e-20
X19_P10	3.849e-05	1.000e-20
X23_P10	4.042e-05	1.000e-20

X29_P10	4.951e-05	1.000e-20
X34_P10	5.246e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

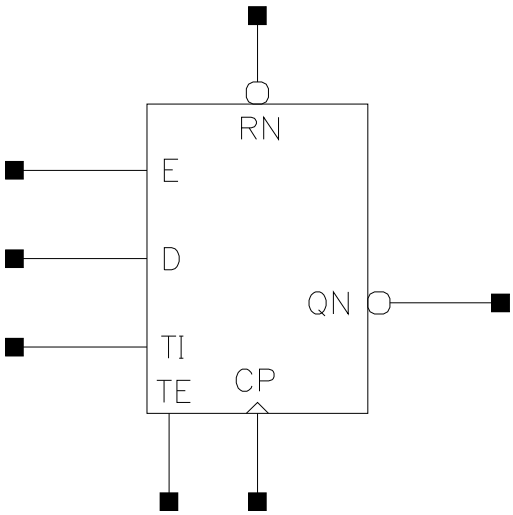
Pin Cycle	X5_P10	X10_P10	X19_P10	X23_P10
Clock 100Mhz Data 0Mhz	6.182e-03	6.175e-03	6.181e-03	6.183e-03
Clock 100Mhz Data 25Mhz	6.389e-03	6.738e-03	7.301e-03	7.352e-03
Clock 100Mhz Data 50Mhz	6.596e-03	7.300e-03	8.420e-03	8.521e-03
Clock = 0 Data 100Mhz	3.582e-03	3.580e-03	3.580e-03	3.580e-03
Clock = 1 Data 100Mhz	1.473e-03	1.473e-03	1.473e-03	1.473e-03
	X29_P10	X34_P10		
Clock 100Mhz Data 0Mhz	6.183e-03	6.184e-03		
Clock 100Mhz Data 25Mhz	7.874e-03	8.036e-03		
Clock 100Mhz Data 50Mhz	9.564e-03	9.888e-03		
Clock = 0 Data 100Mhz	3.580e-03	3.580e-03		
Clock = 1 Data 100Mhz	1.473e-03	1.473e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.600	2.992	4.7872
X10_P10	1.600	3.128	5.0048
X19_P10	1.600	3.264	5.2224
X23_P10	1.600	3.264	5.2224
X29_P10	1.600	3.536	5.6576
X34_P10	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10	X23_P10
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0011	0.0012	0.0012	0.0012

RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P10	X34_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0012	0.0011		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
CP to QN ↓	0.1415	0.1209	4.3068	2.1223
CP to QN ↑	0.0984	0.0912	6.7479	3.4030
RN to QN ↑	0.0953	0.0828	6.7475	3.4016
	X19_P10	**X23_P10**	**X19_P10**	**X23_P10**
CP to QN ↓	0.1267	0.1278	1.0831	0.8150
CP to QN ↑	0.0994	0.0968	1.7134	1.6871
RN to QN ↑	0.0915	0.0885	1.7160	1.6880
	X29_P10	**X34_P10**	**X29_P10**	**X34_P10**
CP to QN ↓	0.1756	0.1718	0.7141	0.5531
CP to QN ↑	0.1321	0.1304	1.1380	1.1348
RN to QN ↑	0.1285	0.1277	1.1375	1.1342

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X5_P10	X10_P10	X19_P10	X23_P10
CP ↓	min_pulse_width to CP	0.0968	0.0968	0.0968	0.0968
CP ↑	min_pulse_width to CP	0.0624	0.0623	0.0623	0.0623
D ↓	hold_rising to CP	-0.0680	-0.0680	-0.0680	-0.0680
D ↑	hold_rising to CP	-0.0267	-0.0240	-0.0240	-0.0240
D ↓	setup_rising to CP	0.1150	0.1150	0.1150	0.1150
D ↑	setup_rising to CP	0.0542	0.0542	0.0542	0.0542
E ↓	hold_rising to CP	-0.0626	-0.0626	-0.0626	-0.0626
E ↑	hold_rising to CP	-0.0267	-0.0267	-0.0267	-0.0267
E ↓	setup_rising to CP	0.1588	0.1588	0.1588	0.1588
E ↑	setup_rising to CP	0.1150	0.1150	0.1150	0.1150
RN ↓	min_pulse_width to RN	0.0762	0.0806	0.0876	0.0876
RN ↑	recovery_rising to CP	-0.0038	-0.0018	-0.0044	-0.0044
RN ↑	removal_rising to CP	0.0167	0.0167	0.0167	0.0167
TE ↓	hold_rising to CP	-0.0387	-0.0387	-0.0354	-0.0354

TE ↑	hold_rising to CP	-0.0191	-0.0191	-0.0191	-0.0191
TE ↓	setup_rising to CP	0.0900	0.0900	0.0932	0.0932
TE ↑	setup_rising to CP	0.1203	0.1203	0.1199	0.1199
TI ↓	hold_rising to CP	-0.0684	-0.0684	-0.0684	-0.0684
TI ↑	hold_rising to CP	-0.0205	-0.0169	-0.0169	-0.0169
TI ↓	setup_rising to CP	0.1140	0.1183	0.1183	0.1183
TI ↑	setup_rising to CP	0.0466	0.0466	0.0466	0.0466
		X29_P10	X34_P10		
CP ↓	min_pulse_width to CP	0.0961	0.0961		
CP ↑	min_pulse_width to CP	0.0624	0.0624		
D ↓	hold_rising to CP	-0.0680	-0.0680		
D ↑	hold_rising to CP	-0.0267	-0.0267		
D ↓	setup_rising to CP	0.1123	0.1123		
D ↑	setup_rising to CP	0.0542	0.0542		
E ↓	hold_rising to CP	-0.0653	-0.0653		
E ↑	hold_rising to CP	-0.0267	-0.0267		
E ↓	setup_rising to CP	0.1588	0.1588		
E ↑	setup_rising to CP	0.1154	0.1150		
RN ↓	min_pulse_width to RN	0.0762	0.0762		
RN ↑	recovery_rising to CP	-0.0071	-0.0071		
RN ↑	removal_rising to CP	0.0167	0.0167		
TE ↓	hold_rising to CP	-0.0387	-0.0387		
TE ↑	hold_rising to CP	-0.0191	-0.0191		
TE ↓	setup_rising to CP	0.0905	0.0905		
TE ↑	setup_rising to CP	0.1177	0.1177		
TI ↓	hold_rising to CP	-0.0681	-0.0681		
TI ↑	hold_rising to CP	-0.0205	-0.0205		
TI ↓	setup_rising to CP	0.1127	0.1127		
TI ↑	setup_rising to CP	0.0469	0.0469		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	2.461e-05	1.000e-20
X10_P10	2.957e-05	1.000e-20
X19_P10	3.896e-05	1.000e-20
X23_P10	4.204e-05	1.000e-20

X29_P10	4.947e-05	1.000e-20
X34_P10	5.416e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

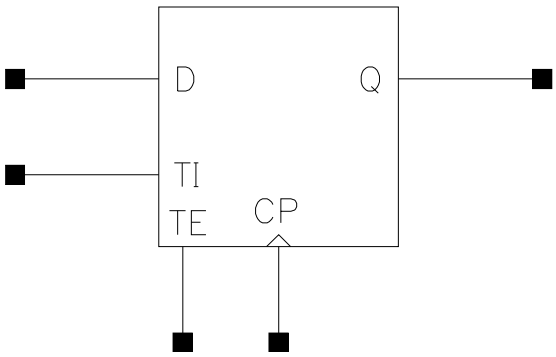
Pin Cycle	X5_P10	X10_P10	X19_P10	X23_P10
Clock 100Mhz Data 0Mhz	6.180e-03	6.186e-03	6.186e-03	6.187e-03
Clock 100Mhz Data 25Mhz	6.433e-03	6.716e-03	7.291e-03	7.330e-03
Clock 100Mhz Data 50Mhz	6.686e-03	7.246e-03	8.395e-03	8.474e-03
Clock = 0 Data 100Mhz	3.581e-03	3.580e-03	3.580e-03	3.581e-03
Clock = 1 Data 100Mhz	1.473e-03	1.473e-03	1.473e-03	1.473e-03
	X29_P10	X34_P10		
Clock 100Mhz Data 0Mhz	6.188e-03	6.187e-03		
Clock 100Mhz Data 25Mhz	7.928e-03	8.059e-03		
Clock 100Mhz Data 50Mhz	9.669e-03	9.932e-03		
Clock = 0 Data 100Mhz	3.580e-03	3.580e-03		
Clock = 1 Data 100Mhz	1.473e-03	1.473e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P10	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P10	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P10	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P10	C8T28SOI_LLHF_-SDFPQX3_P10	C8T28SOIDV_LL_-SDFPQX5_P10	C8T28SOIDV_LL_-SDFPQX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P10	C8T28SOIDV_LL_-SDFPQX23_P10	C8T28SOIDV_LL_-SDFPQX29_P10	
CP	0.0005	0.0005	0.0005	
D	0.0005	0.0005	0.0005	
TE	0.0009	0.0009	0.0009	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P10	**C8T28SOI_LLHF_-SDFPQX3_P10**	**C8T28SOI_LL_-SDFPQX5_P10**	**C8T28SOI_LLHF_-SDFPQX3_P10**
CP to Q ↓	0.0773	0.0658	4.5345	7.0812
CP to Q ↑	0.0721	0.0853	6.8183	10.4710
	C8T28SOIDV_LL_-SDFPQX5_P10	**C8T28SOIDV_LL_-SDFPQX10_P10**	**C8T28SOIDV_LL_-SDFPQX5_P10**	**C8T28SOIDV_LL_-SDFPQX10_P10**
CP to Q ↓	0.0673	0.0951	4.2750	2.0623
CP to Q ↑	0.0855	0.1249	6.7448	3.3700
	C8T28SOIDV_LL_-SDFPQX19_P10	**C8T28SOIDV_LL_-SDFPQX23_P10**	**C8T28SOIDV_LL_-SDFPQX19_P10**	**C8T28SOIDV_LL_-SDFPQX23_P10**
CP to Q ↓	0.1039	0.1070	1.0735	0.8103
CP to Q ↑	0.1327	0.1356	1.7045	1.6881
	C8T28SOIDV_LL_-SDFPQX29_P10		**C8T28SOIDV_LL_-SDFPQX29_P10**	
CP to Q ↓	0.1014		0.7214	
CP to Q ↑	0.1251		1.1291	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P10	C8T28SOI_-LLHF_-SDFPQX3_P10	C8T28SOIDV_-LL_SDFPQX5_-P10	C8T28SOIDV_-LL_SDFPQX10_-P10
CP ↓	min_pulse_width to CP	0.1317	0.1270	0.1138	0.1138
CP ↑	min_pulse_width to CP	0.0627	0.0500	0.0544	0.0531
D ↓	hold_rising to CP	-0.0631	-0.1283	-0.0175	-0.0197
D ↑	hold_rising to CP	-0.0185	-0.0164	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1074	0.1852	0.0742	0.0716
D ↑	setup_rising to CP	0.0466	0.0515	0.0320	0.0320
TE ↓	hold_rising to CP	-0.0403	-0.0453	-0.0126	-0.0121
TE ↑	hold_rising to CP	-0.0196	-0.0137	-0.0196	-0.0196
TE ↓	setup_rising to CP	0.1052	0.1516	0.0663	0.0663
TE ↑	setup_rising to CP	0.1350	0.1812	0.1345	0.1345

TI ↓	hold_rising to CP	-0.0879	-0.1260	-0.0746	-0.0746
TI ↑	hold_rising to CP	-0.0162	-0.0154	-0.0202	-0.0218
TI ↓	setup_rising to CP	0.1322	0.1704	0.1286	0.1286
TI ↑	setup_rising to CP	0.0466	0.0410	0.0459	0.0466
		C8T28SOIDV_-LL_SDFPQX19_-P10	C8T28SOIDV_-LL_SDFPQX23_-P10	C8T28SOIDV_-LL_SDFPQX29_-P10	
CP ↓	min_pulse_width to CP	0.1138	0.1121	0.1138	
CP ↑	min_pulse_width to CP	0.0531	0.0531	0.0531	
D ↓	hold_rising to CP	-0.0197	-0.0197	-0.0192	
D ↑	hold_rising to CP	-0.0071	-0.0071	-0.0071	
D ↓	setup_rising to CP	0.0716	0.0716	0.0737	
D ↑	setup_rising to CP	0.0320	0.0320	0.0320	
TE ↓	hold_rising to CP	-0.0121	-0.0121	-0.0121	
TE ↑	hold_rising to CP	-0.0196	-0.0196	-0.0196	
TE ↓	setup_rising to CP	0.0663	0.0663	0.0685	
TE ↑	setup_rising to CP	0.1345	0.1345	0.1372	
TI ↓	hold_rising to CP	-0.0746	-0.0746	-0.0802	
TI ↑	hold_rising to CP	-0.0218	-0.0202	-0.0202	
TI ↓	setup_rising to CP	0.1286	0.1286	0.1345	
TI ↑	setup_rising to CP	0.0466	0.0466	0.0466	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P10	2.030e-05	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P10	1.827e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P10	1.905e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P10	2.602e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P10	3.199e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P10	3.464e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P10	4.124e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P10	C8T28SOI_LLHF_-SDFPQX3_P10	C8T28SOIDV_LL_-SDFPQX5_P10	C8T28SOIDV_LL_-SDFPQX10_P10
Clock 100Mhz Data 0Mhz	5.883e-03	5.666e-03	5.431e-03	5.309e-03
Clock 100Mhz Data 25Mhz	5.656e-03	5.452e-03	5.312e-03	5.561e-03
Clock 100Mhz Data 50Mhz	5.429e-03	5.238e-03	5.194e-03	5.813e-03

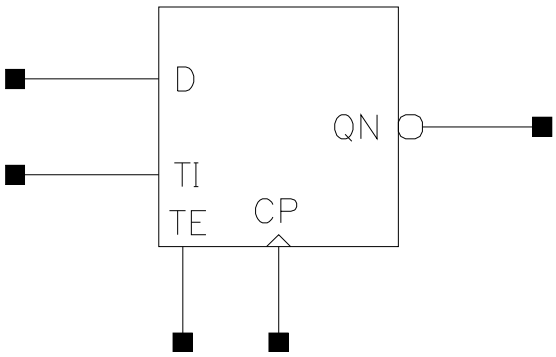
Clock = 0 Data 100Mhz	2.830e-03	2.945e-03	2.787e-03	2.706e-03
Clock = 1 Data 100Mhz	2.338e-05	3.808e-04	2.625e-04	2.035e-04
	C8T28SOIDV_LL_-SDFPQX19_P10	C8T28SOIDV_LL_-SDFPQX23_P10	C8T28SOIDV_LL_-SDFPQX29_P10	
Clock 100Mhz Data 0Mhz	5.239e-03	5.193e-03	5.160e-03	
Clock 100Mhz Data 25Mhz	5.959e-03	5.975e-03	6.369e-03	
Clock 100Mhz Data 50Mhz	6.679e-03	6.758e-03	7.578e-03	
Clock = 0 Data 100Mhz	2.656e-03	2.622e-03	2.601e-03	
Clock = 1 Data 100Mhz	1.680e-04	1.444e-04	1.276e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P10	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P10	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P10	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P10	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P10	C8T28SOI_LLHF_-SDFPQNX3_P10	C8T28SOIDV_LL_-SDFPQNX5_P10	C8T28SOIDV_LL_-SDFPQNX10_P10

CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P10	C8T28SOIDV_LL_-SDFPQNX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P10	**C8T28SOI_LLHF_-SDFPQNX3_P10**	**C8T28SOI_LL_-SDFPQNX5_P10**	**C8T28SOI_LLHF_-SDFPQNX3_P10**
CP to QN ↓	0.0964	0.1043	4.3431	6.6508
CP to QN ↑	0.0846	0.0807	7.3922	10.2288
	C8T28SOIDV_LL_-SDFPQNX5_P10	**C8T28SOIDV_LL_-SDFPQNX10_P10**	**C8T28SOIDV_LL_-SDFPQNX5_P10**	**C8T28SOIDV_LL_-SDFPQNX10_P10**
CP to QN ↓	0.1072	0.0998	4.1720	2.0829
CP to QN ↑	0.0768	0.0831	6.6707	3.3715
	C8T28SOIDV_LL_-SDFPQNX19_P10	**C8T28SOIDV_LL_-SDFPQNX29_P10**	**C8T28SOIDV_LL_-SDFPQNX19_P10**	**C8T28SOIDV_LL_-SDFPQNX29_P10**
CP to QN ↓	0.1134	0.1310	1.0834	0.7188
CP to QN ↑	0.0992	0.1108	1.7231	1.1328

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P10	C8T28SOI_-LLHF_-SDFPQNX3_P10	C8T28SOIDV_-LL_SDFPQNX5_-P10	C8T28SOIDV_-LL_-SDFPQNX10_-P10
CP ↓	min_pulse_width to CP	0.1317	0.1247	0.1138	0.1138
CP ↑	min_pulse_width to CP	0.0499	0.0454	0.0531	0.0531
D ↓	hold_rising to CP	-0.0631	-0.1283	-0.0197	-0.0201
D ↑	hold_rising to CP	-0.0185	-0.0164	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1074	0.1829	0.0737	0.0737
D ↑	setup_rising to CP	0.0466	0.0515	0.0314	0.0320
TE ↓	hold_rising to CP	-0.0399	-0.0447	-0.0126	-0.0126
TE ↑	hold_rising to CP	-0.0195	-0.0137	-0.0147	-0.0196
TE ↓	setup_rising to CP	0.1052	0.1463	0.0689	0.0689
TE ↑	setup_rising to CP	0.1350	0.1763	0.1345	0.1345
TI ↓	hold_rising to CP	-0.0879	-0.1260	-0.0743	-0.0746
TI ↑	hold_rising to CP	-0.0162	-0.0154	-0.0169	-0.0202
TI ↓	setup_rising to CP	0.1322	0.1704	0.1286	0.1286

TI ↑	setup_rising to CP	0.0466	0.0453	0.0453	0.0466
		C8T28SOIDV_-LL_-SDFPQNX19_-P10	C8T28SOIDV_-LL_-SDFPQNX29_-P10		
CP ↓	min_pulse_width to CP	0.1138	0.1121		
CP ↑	min_pulse_width to CP	0.0624	0.0531		
D ↓	hold_rising to CP	-0.0197	-0.0197		
D ↑	hold_rising to CP	-0.0071	-0.0071		
D ↓	setup_rising to CP	0.0742	0.0742		
D ↑	setup_rising to CP	0.0320	0.0320		
TE ↓	hold_rising to CP	-0.0126	-0.0121		
TE ↑	hold_rising to CP	-0.0196	-0.0196		
TE ↓	setup_rising to CP	0.0663	0.0663		
TE ↑	setup_rising to CP	0.1345	0.1345		
TI ↓	hold_rising to CP	-0.0746	-0.0746		
TI ↑	hold_rising to CP	-0.0202	-0.0202		
TI ↓	setup_rising to CP	0.1286	0.1286		
TI ↑	setup_rising to CP	0.0466	0.0466		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P10	2.010e-05	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P10	1.858e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P10	1.920e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P10	2.542e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P10	3.203e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P10	4.742e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P10	C8T28SOI_LLHF_-SDFPQNX3_P10	C8T28SOIDV_LL_-SDFPQNX5_P10	C8T28SOIDV_LL_-SDFPQNX10_P10
Clock 100Mhz Data 0Mhz	5.883e-03	5.728e-03	5.479e-03	5.344e-03
Clock 100Mhz Data 25Mhz	5.623e-03	5.522e-03	5.296e-03	5.535e-03
Clock 100Mhz Data 50Mhz	5.363e-03	5.316e-03	5.113e-03	5.725e-03
Clock = 0 Data 100Mhz	2.830e-03	2.953e-03	2.795e-03	2.713e-03
Clock = 1 Data 100Mhz	2.351e-05	3.825e-04	2.637e-04	2.043e-04

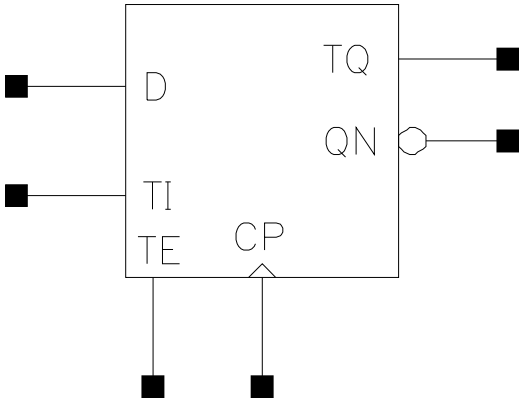
	C8T28SOIDV_LL_-SDFPQNX19_P10	C8T28SOIDV_LL_-SDFPQNX29_P10		
Clock 100Mhz Data 0Mhz	5.266e-03	5.213e-03		
Clock 100Mhz Data 25Mhz	6.065e-03	6.794e-03		
Clock 100Mhz Data 50Mhz	6.863e-03	8.376e-03		
Clock = 0 Data 100Mhz	2.661e-03	2.628e-03		
Clock = 1 Data 100Mhz	1.687e-04	1.450e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P10	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P10	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P10	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P10	C8T28SOI_LLHF_-SDFPQNTX3_P10	C8T28SOIDV_LL_-SDFPQNTX5_P10	C8T28SOIDV_LL_-SDFPQNTX10_P10
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P10	C8T28SOIDV_LL_-SDFPQNTX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNTX5_P10	**C8T28SOI_LLHF_-SDFPQNTX3_P10**	**C8T28SOI_LL_-SDFPQNTX5_P10**	**C8T28SOI_LLHF_-SDFPQNTX3_P10**
CP to QN ↓	0.1089	0.1142	4.4928	6.7865
CP to QN ↑	0.1088	0.1004	7.4066	10.2477
CP to TQ ↓	0.0893	0.0694	12.2844	7.9497
CP to TQ ↑	0.0916	0.0843	35.1468	18.8048
	C8T28SOIDV_LL_-SDFPQNTX5_P10	**C8T28SOIDV_LL_-SDFPQNTX10_P10**	**C8T28SOIDV_LL_-SDFPQNTX5_P10**	**C8T28SOIDV_LL_-SDFPQNTX10_P10**
CP to QN ↓	0.1153	0.1112	4.1235	2.1055
CP to QN ↑	0.0907	0.0910	6.6766	3.3754
CP to TQ ↓	0.0629	0.0659	7.9229	8.2645
CP to TQ ↑	0.0856	0.0879	14.7522	15.3841
	C8T28SOIDV_LL_-SDFPQNTX19_P10	**C8T28SOIDV_LL_-SDFPQNTX29_P10**	**C8T28SOIDV_LL_-SDFPQNTX19_P10**	**C8T28SOIDV_LL_-SDFPQNTX29_P10**
CP to QN ↓	0.1146	0.1341	1.0800	0.7221
CP to QN ↑	0.0990	0.1178	1.7121	1.1309
CP to TQ ↓	0.0687	0.0664	8.0972	8.3246
CP to TQ ↑	0.0908	0.0917	15.7655	20.3643

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_-P10	C8T28SOI_-LLHF_-SDFPQNTX3_-P10	C8T28SOIDV_-LL_-SDFPQNTX5_-P10	C8T28SOIDV_-LL_-SDFPQNTX10_-P10
CP ↓	min_pulse_width to CP	0.1317	0.1264	0.1138	0.1138
CP ↑	min_pulse_width to CP	0.0688	0.0594	0.0530	0.0577
D ↓	hold_rising to CP	-0.0631	-0.1288	-0.0197	-0.0175
D ↑	hold_rising to CP	-0.0218	-0.0159	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1074	0.1803	0.0737	0.0742

D ↑	setup_rising to CP	0.0488	0.0515	0.0314	0.0320
TE ↓	hold_rising to CP	-0.0431	-0.0447	-0.0121	-0.0126
TE ↑	hold_rising to CP	-0.0196	-0.0165	-0.0147	-0.0196
TE ↓	setup_rising to CP	0.1052	0.1463	0.0685	0.0663
TE ↑	setup_rising to CP	0.1350	0.1763	0.1378	0.1345
TI ↓	hold_rising to CP	-0.0886	-0.1260	-0.0746	-0.0746
TI ↑	hold_rising to CP	-0.0162	-0.0154	-0.0154	-0.0202
TI ↓	setup_rising to CP	0.1322	0.1688	0.1286	0.1286
TI ↑	setup_rising to CP	0.0466	0.0453	0.0453	0.0459
		C8T28SOIDV_-LL_-SDFPQNTX19_-P10	C8T28SOIDV_-LL_-SDFPQNTX29_-P10		
CP ↓	min_pulse_width to CP	0.1138	0.1138		
CP ↑	min_pulse_width to CP	0.0624	0.0544		
D ↓	hold_rising to CP	-0.0175	-0.0197		
D ↑	hold_rising to CP	-0.0071	-0.0071		
D ↓	setup_rising to CP	0.0737	0.0737		
D ↑	setup_rising to CP	0.0320	0.0320		
TE ↓	hold_rising to CP	-0.0126	-0.0126		
TE ↑	hold_rising to CP	-0.0196	-0.0196		
TE ↓	setup_rising to CP	0.0689	0.0663		
TE ↑	setup_rising to CP	0.1345	0.1345		
TI ↓	hold_rising to CP	-0.0746	-0.0746		
TI ↑	hold_rising to CP	-0.0202	-0.0202		
TI ↓	setup_rising to CP	0.1286	0.1286		
TI ↑	setup_rising to CP	0.0466	0.0459		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P10	2.022e-05	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P10	1.988e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P10	2.056e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P10	2.430e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P10	3.182e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P10	4.818e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

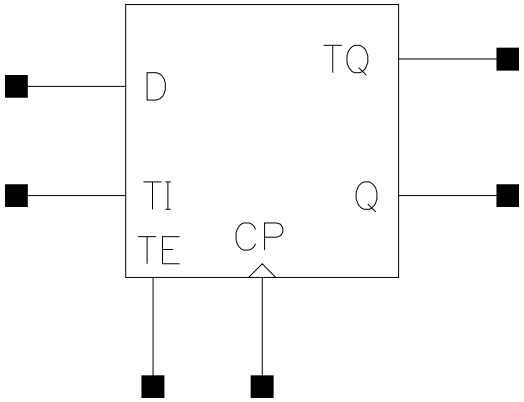
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P10	C8T28SOI_LLHF_-SDFPQNTX3_P10	C8T28SOIDV_LL_-SDFPQNTX5_P10	C8T28SOIDV_LL_-SDFPQNTX10_P10
Clock 100Mhz Data 0Mhz	5.885e-03	5.729e-03	5.476e-03	5.343e-03
Clock 100Mhz Data 25Mhz	5.852e-03	5.695e-03	5.463e-03	5.531e-03
Clock 100Mhz Data 50Mhz	5.820e-03	5.662e-03	5.451e-03	5.720e-03
Clock = 0 Data 100Mhz	2.833e-03	2.955e-03	2.799e-03	2.716e-03
Clock = 1 Data 100Mhz	2.359e-05	3.853e-04	2.656e-04	2.057e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P10	C8T28SOIDV_LL_-SDFPQNTX29_P10		
Clock 100Mhz Data 0Mhz	5.263e-03	5.207e-03		
Clock 100Mhz Data 25Mhz	5.978e-03	6.936e-03		
Clock 100Mhz Data 50Mhz	6.692e-03	8.664e-03		
Clock = 0 Data 100Mhz	2.666e-03	2.633e-03		
Clock = 1 Data 100Mhz	1.698e-04	1.459e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P10	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P10	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P10	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P10	C8T28SOI_LLHF_-SDFPQTX3_P10	C8T28SOIDV_LL_-SDFPQTX5_P10	C8T28SOIDV_LL_-SDFPQTX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P10	C8T28SOIDV_LL_-SDFPQTX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQTX5_P10	**C8T28SOI_LLHF_-SDFPQTX3_P10**	**C8T28SOI_LL_-SDFPQTX5_P10**	**C8T28SOI_LLHF_-SDFPQTX3_P10**
CP to Q ↓	0.0915	0.0843	4.7901	7.3316
CP to Q ↑	0.0783	0.0852	6.8645	10.5825
CP to TQ ↓	0.1098	0.0827	13.3709	8.1549
CP to TQ ↑	0.1012	0.0909	35.5360	19.0207
	C8T28SOIDV_LL_-SDFPQTX5_P10	**C8T28SOIDV_LL_-SDFPQTX10_P10**	**C8T28SOIDV_LL_-SDFPQTX5_P10**	**C8T28SOIDV_LL_-SDFPQTX10_P10**
CP to Q ↓	0.0733	0.0977	4.3818	2.0746
CP to Q ↑	0.0884	0.1271	6.8193	3.3749
CP to TQ ↓	0.0728	0.1009	8.1317	8.3478
CP to TQ ↑	0.0916	0.1326	16.1866	16.0268
	C8T28SOIDV_LL_-SDFPQTX19_P10	**C8T28SOIDV_LL_-SDFPQTX29_P10**	**C8T28SOIDV_LL_-SDFPQTX19_P10**	**C8T28SOIDV_LL_-SDFPQTX29_P10**
CP to Q ↓	0.1060	0.1158	1.0763	0.7025
CP to Q ↑	0.1334	0.1312	1.7101	1.1274
CP to TQ ↓	0.1111	0.0706	8.4132	8.5808
CP to TQ ↑	0.1417	0.0938	16.0705	20.3536

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P10	C8T28SOI_-LLHF_-SDFPQTX3_P10	C8T28SOIDV_-LL_SDFPQTX5_-P10	C8T28SOIDV_-LL_-SDFPQTX10_-P10
CP ↓	min_pulse_width to CP	0.1323	0.1247	0.1138	0.1138
CP ↑	min_pulse_width to CP	0.0783	0.0641	0.0589	0.0531
D ↓	hold_rising to CP	-0.0631	-0.1283	-0.0175	-0.0197
D ↑	hold_rising to CP	-0.0185	-0.0164	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1074	0.1830	0.0742	0.0716

D ↑	setup_rising to CP	0.0466	0.0515	0.0320	0.0320
TE ↓	hold_rising to CP	-0.0403	-0.0447	-0.0126	-0.0121
TE ↑	hold_rising to CP	-0.0196	-0.0137	-0.0196	-0.0196
TE ↓	setup_rising to CP	0.1052	0.1463	0.0663	0.0663
TE ↑	setup_rising to CP	0.1350	0.1763	0.1345	0.1345
TI ↓	hold_rising to CP	-0.0886	-0.1260	-0.0746	-0.0746
TI ↑	hold_rising to CP	-0.0162	-0.0154	-0.0202	-0.0218
TI ↓	setup_rising to CP	0.1322	0.1688	0.1286	0.1286
TI ↑	setup_rising to CP	0.0466	0.0453	0.0459	0.0466
		C8T28SOIDV_-LL_-SDFPQTX19_-P10	C8T28SOIDV_-LL_-SDFPQTX29_-P10		
CP ↓	min_pulse_width to CP	0.1121	0.1138		
CP ↑	min_pulse_width to CP	0.0531	0.0624		
D ↓	hold_rising to CP	-0.0197	-0.0197		
D ↑	hold_rising to CP	-0.0071	-0.0071		
D ↓	setup_rising to CP	0.0716	0.0737		
D ↑	setup_rising to CP	0.0320	0.0320		
TE ↓	hold_rising to CP	-0.0121	-0.0126		
TE ↑	hold_rising to CP	-0.0196	-0.0196		
TE ↓	setup_rising to CP	0.0663	0.0685		
TE ↑	setup_rising to CP	0.1345	0.1378		
TI ↓	hold_rising to CP	-0.0746	-0.0746		
TI ↑	hold_rising to CP	-0.0218	-0.0202		
TI ↓	setup_rising to CP	0.1286	0.1286		
TI ↑	setup_rising to CP	0.0466	0.0466		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P10	2.053e-05	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P10	1.987e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P10	2.046e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P10	2.733e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P10	3.386e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P10	4.385e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

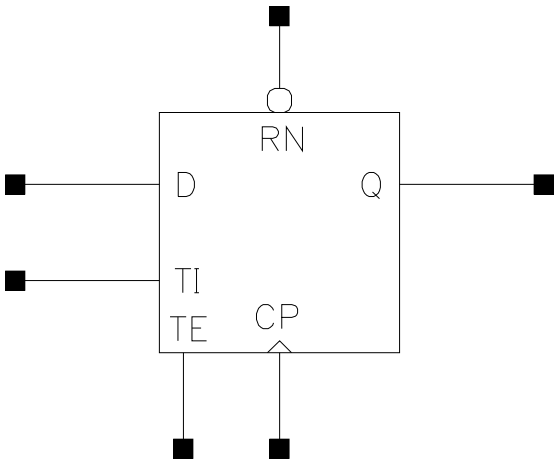
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P10	C8T28SOI_LLHF_-SDFPQTX3_P10	C8T28SOIDV_LL_-SDFPQTX5_P10	C8T28SOIDV_LL_-SDFPQTX10_P10
Clock 100Mhz Data 0Mhz	5.887e-03	5.735e-03	5.477e-03	5.344e-03
Clock 100Mhz Data 25Mhz	5.867e-03	5.693e-03	5.476e-03	5.711e-03
Clock 100Mhz Data 50Mhz	5.848e-03	5.651e-03	5.476e-03	6.077e-03
Clock = 0 Data 100Mhz	2.833e-03	2.957e-03	2.795e-03	2.712e-03
Clock = 1 Data 100Mhz	2.333e-05	3.832e-04	2.642e-04	2.047e-04
	C8T28SOIDV_LL_-SDFPQTX19_P10	C8T28SOIDV_LL_-SDFPQTX29_P10		
Clock 100Mhz Data 0Mhz	5.266e-03	5.218e-03		
Clock 100Mhz Data 25Mhz	6.121e-03	6.605e-03		
Clock 100Mhz Data 50Mhz	6.977e-03	7.992e-03		
Clock = 0 Data 100Mhz	2.660e-03	2.629e-03		
Clock = 1 Data 100Mhz	1.690e-04	1.453e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P10	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P10	C8T28SOI_LLHF_-SDFPRQX3_P10	C8T28SOIDV_LL_-SDFPRQX5_P10	C8T28SOIDV_LL_-SDFPRQX10_P10
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0010	0.0010	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P10	C8T28SOIDV_LL_-SDFPRQX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P10	**C8T28SOI_LLHF_-SDFPRQX3_P10**	**C8T28SOI_LL_-SDFPRQX5_P10**	**C8T28SOI_LLHF_-SDFPRQX3_P10**
CP to Q ↓	0.0892	0.0805	4.5810	7.1392
CP to Q ↑	0.0752	0.0850	6.8214	10.3932
RN to Q ↓	0.0789	0.0772	4.2173	6.6876
	C8T28SOIDV_LL_-SDFPRQX5_P10	**C8T28SOIDV_LL_-SDFPRQX10_P10**	**C8T28SOIDV_LL_-SDFPRQX5_P10**	**C8T28SOIDV_LL_-SDFPRQX10_P10**
CP to Q ↓	0.0680	0.0976	4.2619	2.0869
CP to Q ↑	0.0893	0.1300	6.7427	3.3762
RN to Q ↓	0.0640	0.1000	4.2384	2.0874
	C8T28SOIDV_LL_-SDFPRQX19_P10	**C8T28SOIDV_LL_-SDFPRQX29_P10**	**C8T28SOIDV_LL_-SDFPRQX19_P10**	**C8T28SOIDV_LL_-SDFPRQX29_P10**
CP to Q ↓	0.1046	0.1062	1.0751	0.7328
CP to Q ↑	0.1364	0.1419	1.7232	1.1668
RN to Q ↓	0.1074	0.1090	1.0749	0.7321

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P10	C8T28SOI_-LLHF_-SDFPRQX3_P10	C8T28SOIDV_-LL_SDFPRQX5_-P10	C8T28SOIDV_-LL_-SDFPRQX10_-P10
CP ↓	min_pulse_width to CP	0.1330	0.1230	0.1179	0.1186
CP ↑	min_pulse_width to CP	0.0687	0.0594	0.0530	0.0531
D ↓	hold_rising to CP	-0.0631	-0.1261	-0.0143	-0.0197
D ↑	hold_rising to CP	-0.0218	-0.0218	-0.0071	-0.0066
D ↓	setup_rising to CP	0.1132	0.1777	0.0737	0.0737
D ↑	setup_rising to CP	0.0515	0.0564	0.0368	0.0368
RN ↓	min_pulse_width to RN	0.0833	0.0833	0.0730	0.0708
RN ↑	recovery_rising to CP	0.0076	0.0027	0.0027	0.0031

RN ↑	removal_rising to CP	0.0095	0.0095	0.0086	0.0086
TE ↓	hold_rising to CP	-0.0457	-0.0506	-0.0121	-0.0121
TE ↑	hold_rising to CP	-0.0195	-0.0191	-0.0191	-0.0218
TE ↓	setup_rising to CP	0.1079	0.1467	0.0685	0.0685
TE ↑	setup_rising to CP	0.1345	0.1763	0.1350	0.1350
TI ↓	hold_rising to CP	-0.0886	-0.1209	-0.0753	-0.0746
TI ↑	hold_rising to CP	-0.0202	-0.0147	-0.0218	-0.0215
TI ↓	setup_rising to CP	0.1322	0.1655	0.1286	0.1286
TI ↑	setup_rising to CP	0.0515	0.0450	0.0515	0.0515
		C8T28SOIDV_-LL_-SDFPRQX19_-P10	C8T28SOIDV_-LL_-SDFPRQX29_-P10		
CP ↓	min_pulse_width to CP	0.1162	0.1169		
CP ↑	min_pulse_width to CP	0.0531	0.0531		
D ↓	hold_rising to CP	-0.0197	-0.0197		
D ↑	hold_rising to CP	-0.0066	-0.0066		
D ↓	setup_rising to CP	0.0737	0.0737		
D ↑	setup_rising to CP	0.0368	0.0368		
RN ↓	min_pulse_width to RN	0.0686	0.0708		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0086	0.0086		
TE ↓	hold_rising to CP	-0.0147	-0.0143		
TE ↑	hold_rising to CP	-0.0218	-0.0218		
TE ↓	setup_rising to CP	0.0685	0.0717		
TE ↑	setup_rising to CP	0.1350	0.1350		
TI ↓	hold_rising to CP	-0.0746	-0.0746		
TI ↑	hold_rising to CP	-0.0215	-0.0215		
TI ↓	setup_rising to CP	0.1286	0.1286		
TI ↑	setup_rising to CP	0.0515	0.0515		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P10	2.139e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P10	1.987e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P10	2.020e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P10	2.662e-05	1.000e-20

C8T28SOIDV_LL_SDFPRQX19_P10	3.309e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P10	4.175e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

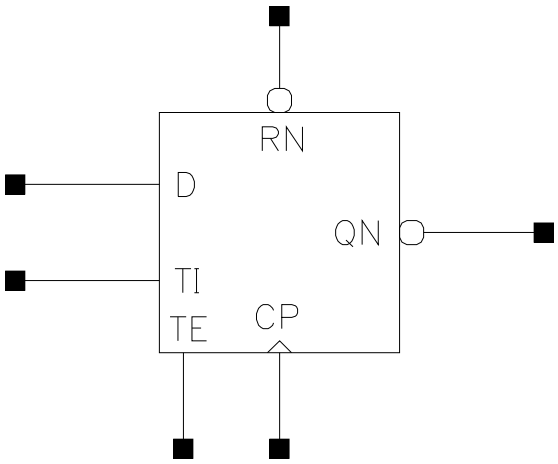
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P10	C8T28SOI_LLHF_-SDFPRQX3_P10	C8T28SOIDV_LL_-SDFPRQX5_P10	C8T28SOIDV_LL_-SDFPRQX10_P10
Clock 100Mhz Data 0Mhz	6.121e-03	5.906e-03	5.632e-03	5.495e-03
Clock 100Mhz Data 25Mhz	5.881e-03	5.705e-03	5.454e-03	5.729e-03
Clock 100Mhz Data 50Mhz	5.641e-03	5.505e-03	5.275e-03	5.964e-03
Clock = 0 Data 100Mhz	2.719e-03	2.868e-03	2.762e-03	2.710e-03
Clock = 1 Data 100Mhz	2.332e-05	3.852e-04	2.651e-04	2.050e-04
	C8T28SOIDV_LL_-SDFPRQX19_P10	C8T28SOIDV_LL_-SDFPRQX29_P10		
Clock 100Mhz Data 0Mhz	5.413e-03	5.359e-03		
Clock 100Mhz Data 25Mhz	6.107e-03	6.658e-03		
Clock 100Mhz Data 50Mhz	6.800e-03	7.958e-03		
Clock = 0 Data 100Mhz	2.678e-03	2.659e-03		
Clock = 1 Data 100Mhz	1.691e-04	1.451e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P10	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P10	C8T28SOI_LLHF_-SDFPRQNX3_P10	C8T28SOIDV_LL_-SDFPRQNX5_P10	C8T28SOIDV_LL_-SDFPRQNX10_P10
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0010	0.0010	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P10	C8T28SOIDV_LL_-SDFPRQNX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0007	0.0007		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNX5_P10	**C8T28SOI_LLHF_-SDFPRQNX3_P10**	**C8T28SOI_LL_-SDFPRQNX5_P10**	**C8T28SOI_LLHF_-SDFPRQNX3_P10**
CP to QN ↓	0.1018	0.1089	4.4701	6.6698
CP to QN ↑	0.0945	0.0886	7.0491	10.2405
RN to QN ↑	0.0926	0.0909	7.0320	10.2234
	C8T28SOIDV_LL_-SDFPRQNX5_P10	**C8T28SOIDV_LL_-SDFPRQNX10_P10**	**C8T28SOIDV_LL_-SDFPRQNX5_P10**	**C8T28SOIDV_LL_-SDFPRQNX10_P10**
CP to QN ↓	0.1162	0.1041	4.1095	2.0922
CP to QN ↑	0.0858	0.0840	6.6628	3.3769
RN to QN ↑	0.0870	0.0805	6.6536	3.3805
	C8T28SOIDV_LL_-SDFPRQNX19_P10	**C8T28SOIDV_LL_-SDFPRQNX29_P10**	**C8T28SOIDV_LL_-SDFPRQNX19_P10**	**C8T28SOIDV_LL_-SDFPRQNX29_P10**
CP to QN ↓	0.1162	0.1239	1.1016	0.7379
CP to QN ↑	0.0932	0.1051	1.7296	1.1609
RN to QN ↑	0.0867	0.1011	1.7258	1.1604

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P10	C8T28SOI_-LLHF_-SDFPRQNX3_-P10	C8T28SOIDV_-LL_-SDFPRQNX5_-P10	C8T28SOIDV_-LL_-SDFPRQNX10_-P10
CP ↓	min_pulse_width to CP	0.1330	0.1247	0.1186	0.1186
CP ↑	min_pulse_width to CP	0.0544	0.0500	0.0531	0.0530
D ↓	hold_rising to CP	-0.0631	-0.1235	-0.0175	-0.0143
D ↑	hold_rising to CP	-0.0218	-0.0218	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1106	0.1777	0.0737	0.0737
D ↑	setup_rising to CP	0.0515	0.0564	0.0368	0.0368
RN ↓	min_pulse_width to RN	0.0833	0.0833	0.0708	0.0779
RN ↑	recovery_rising to CP	0.0076	0.0027	0.0031	0.0027

RN ↑	removal_rising to CP	0.0095	0.0096	0.0086	0.0090
TE ↓	hold_rising to CP	-0.0457	-0.0506	-0.0121	-0.0121
TE ↑	hold_rising to CP	-0.0196	-0.0191	-0.0196	-0.0191
TE ↓	setup_rising to CP	0.1079	0.1467	0.0685	0.0717
TE ↑	setup_rising to CP	0.1345	0.1763	0.1350	0.1350
TI ↓	hold_rising to CP	-0.0886	-0.1211	-0.0746	-0.0753
TI ↑	hold_rising to CP	-0.0202	-0.0147	-0.0218	-0.0218
TI ↓	setup_rising to CP	0.1322	0.1655	0.1286	0.1286
TI ↑	setup_rising to CP	0.0515	0.0443	0.0515	0.0515
		C8T28SOIDV_-LL_-SDFPRQNX19_-P10	C8T28SOIDV_-LL_-SDFPRQNX29_-P10		
CP ↓	min_pulse_width to CP	0.1185	0.1185		
CP ↑	min_pulse_width to CP	0.0578	0.0684		
D ↓	hold_rising to CP	-0.0143	-0.0143		
D ↑	hold_rising to CP	-0.0071	-0.0071		
D ↓	setup_rising to CP	0.0737	0.0737		
D ↑	setup_rising to CP	0.0368	0.0368		
RN ↓	min_pulse_width to RN	0.0801	0.0947		
RN ↑	recovery_rising to CP	0.0010	0.0005		
RN ↑	removal_rising to CP	0.0118	0.0118		
TE ↓	hold_rising to CP	-0.0094	-0.0094		
TE ↑	hold_rising to CP	-0.0196	-0.0196		
TE ↓	setup_rising to CP	0.0717	0.0717		
TE ↑	setup_rising to CP	0.1350	0.1350		
TI ↓	hold_rising to CP	-0.0697	-0.0697		
TI ↑	hold_rising to CP	-0.0218	-0.0218		
TI ↓	setup_rising to CP	0.1286	0.1286		
TI ↑	setup_rising to CP	0.0515	0.0515		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P10	2.153e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P10	2.039e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P10	2.057e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P10	2.672e-05	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P10	3.212e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P10	4.121e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

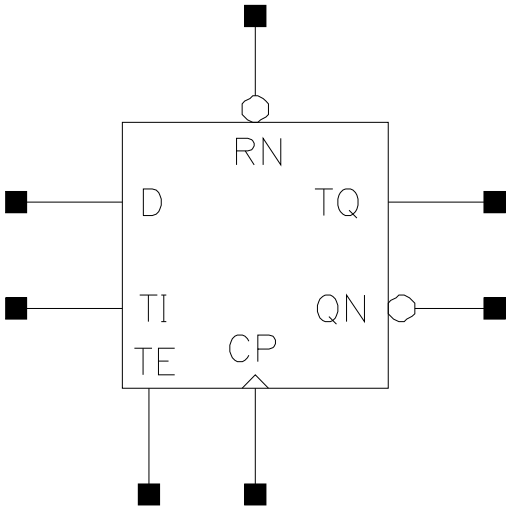
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P10	C8T28SOI_LLHF_-SDFPRQNX3_P10	C8T28SOIDV_LL_-SDFPRQNX5_P10	C8T28SOIDV_LL_-SDFPRQNX10_P10
Clock 100Mhz Data 0Mhz	6.115e-03	5.888e-03	5.622e-03	5.488e-03
Clock 100Mhz Data 25Mhz	5.834e-03	5.677e-03	5.481e-03	5.704e-03
Clock 100Mhz Data 50Mhz	5.553e-03	5.465e-03	5.339e-03	5.921e-03
Clock = 0 Data 100Mhz	2.715e-03	2.864e-03	2.762e-03	2.709e-03
Clock = 1 Data 100Mhz	2.335e-05	3.846e-04	2.647e-04	2.047e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P10	C8T28SOIDV_LL_-SDFPRQNX29_P10		
Clock 100Mhz Data 0Mhz	5.450e-03	5.445e-03		
Clock 100Mhz Data 25Mhz	6.139e-03	6.819e-03		
Clock 100Mhz Data 50Mhz	6.829e-03	8.192e-03		
Clock = 0 Data 100Mhz	2.676e-03	2.655e-03		
Clock = 1 Data 100Mhz	1.688e-04	1.449e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P10	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P10	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P10	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P10	C8T28SOI_LLHF_-SDFPRQNTX3_P10	C8T28SOIDV_LL_-SDFPRQNTX5_P10	C8T28SOIDV_LL_-SDFPRQNTX10_P10
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0007	0.0008	0.0009
TE	0.0010	0.0010	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P10	C8T28SOIDV_LL_-SDFPRQNTX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0007	0.0007		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNTX5_P10	**C8T28SOI_LLHF_-SDFPRQNTX3_P10**	**C8T28SOI_LL_-SDFPRQNTX5_P10**	**C8T28SOI_LLHF_-SDFPRQNTX3_P10**
CP to QN ↓	0.1128	0.1187	4.3596	6.7569
CP to QN ↑	0.1189	0.1088	7.4057	10.2392
CP to TQ ↓	0.1003	0.0777	12.8900	8.0104
CP to TQ ↑	0.0934	0.0886	35.1490	18.8435
RN to QN ↑	0.1020	0.0986	7.4072	10.2820
RN to TQ ↓	0.0872	0.0763	12.4854	7.6592
	C8T28SOIDV_LL_-SDFPRQNTX5_P10	**C8T28SOIDV_LL_-SDFPRQNTX10_P10**	**C8T28SOIDV_LL_-SDFPRQNTX5_P10**	**C8T28SOIDV_LL_-SDFPRQNTX10_P10**
CP to QN ↓	0.1224	0.1299	4.1644	2.1701
CP to QN ↑	0.0941	0.0993	6.6585	3.3756
CP to TQ ↓	0.0645	0.0655	7.9399	8.0129
CP to TQ ↑	0.0906	0.0906	14.7592	14.7651
RN to QN ↑	0.0903	0.0963	6.6625	3.3706
RN to TQ ↓	0.0586	0.0602	7.9653	8.0414
	C8T28SOIDV_LL_-SDFPRQNTX19_P10	**C8T28SOIDV_LL_-SDFPRQNTX29_P10**	**C8T28SOIDV_LL_-SDFPRQNTX19_P10**	**C8T28SOIDV_LL_-SDFPRQNTX29_P10**
CP to QN ↓	0.1218	0.1235	1.0873	0.7378
CP to QN ↑	0.1014	0.1135	1.7041	1.1519
CP to TQ ↓	0.0709	0.0864	8.0813	9.2080
CP to TQ ↑	0.0968	0.1076	14.7920	16.9867
RN to QN ↑	0.0949	0.1082	1.7022	1.1502
RN to TQ ↓	0.0627	0.0794	8.0738	9.0829

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P10	C8T28SOI_-LLHF_-SDFPRQNTX3_-P10	C8T28SOIDV_-LL_-SDFPRQNTX5_-P10	C8T28SOIDV_-LL_SDF-PRQNTX10_P10
CP ↓	min_pulse_width to CP	0.1330	0.1230	0.1186	0.1186
CP ↑	min_pulse_width to CP	0.0735	0.0641	0.0577	0.0578
D ↓	hold_rising to CP	-0.0637	-0.1235	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0218	-0.0218	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1074	0.1777	0.0737	0.0733
D ↑	setup_rising to CP	0.0515	0.0564	0.0368	0.0368
RN ↓	min_pulse_width to RN	0.0876	0.0854	0.0806	0.0828
RN ↑	recovery_rising to CP	0.0076	0.0027	0.0031	0.0027
RN ↑	removal_rising to CP	0.0095	0.0096	0.0086	0.0096
TE ↓	hold_rising to CP	-0.0457	-0.0506	-0.0121	-0.0121
TE ↑	hold_rising to CP	-0.0196	-0.0191	-0.0196	-0.0191
TE ↓	setup_rising to CP	0.1052	0.1467	0.0685	0.0717
TE ↑	setup_rising to CP	0.1345	0.1763	0.1345	0.1350
TI ↓	hold_rising to CP	-0.0843	-0.1211	-0.0753	-0.0753
TI ↑	hold_rising to CP	-0.0202	-0.0147	-0.0218	-0.0218
TI ↓	setup_rising to CP	0.1322	0.1655	0.1286	0.1286
TI ↑	setup_rising to CP	0.0515	0.0459	0.0515	0.0515
		C8T28SOIDV_-LL_SDF-PRQNTX19_P10	C8T28SOIDV_-LL_SDF-PRQNTX29_P10		
CP ↓	min_pulse_width to CP	0.1185	0.1185		
CP ↑	min_pulse_width to CP	0.0624	0.0731		
D ↓	hold_rising to CP	-0.0143	-0.0143		
D ↑	hold_rising to CP	-0.0071	-0.0071		
D ↓	setup_rising to CP	0.0733	0.0733		
D ↑	setup_rising to CP	0.0368	0.0368		
RN ↓	min_pulse_width to RN	0.0876	0.1045		
RN ↑	recovery_rising to CP	0.0031	0.0031		
RN ↑	removal_rising to CP	0.0118	0.0118		
TE ↓	hold_rising to CP	-0.0094	-0.0094		
TE ↑	hold_rising to CP	-0.0196	-0.0196		

TE ↓	setup_rising to CP	0.0717	0.0717		
TE ↑	setup_rising to CP	0.1350	0.1350		
TI ↓	hold_rising to CP	-0.0697	-0.0697		
TI ↑	hold_rising to CP	-0.0218	-0.0218		
TI ↓	setup_rising to CP	0.1286	0.1286		
TI ↑	setup_rising to CP	0.0515	0.0515		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P10	2.160e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P10	2.136e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P10	2.182e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_P10	2.475e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_P10	3.230e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_P10	4.224e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

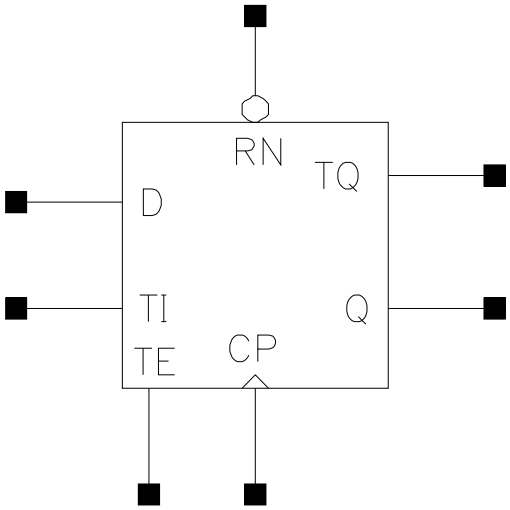
Pin Cycle	C8T28SOI_LL_SDFPRQNTX5_P10	C8T28SOI_LLHF_SDFPRQNTX3_P10	C8T28SOIDV_LL_SDFPRQNTX5_P10	C8T28SOIDV_LL_SDFPRQNTX10_P10
Clock 100Mhz Data 0Mhz	6.124e-03	5.895e-03	5.636e-03	5.499e-03
Clock 100Mhz Data 25Mhz	6.049e-03	5.851e-03	5.630e-03	5.730e-03
Clock 100Mhz Data 50Mhz	5.973e-03	5.808e-03	5.624e-03	5.962e-03
Clock = 0 Data 100Mhz	2.702e-03	2.862e-03	2.762e-03	2.710e-03
Clock = 1 Data 100Mhz	2.320e-05	3.868e-04	2.662e-04	2.059e-04
	C8T28SOIDV_LL_SDFPRQNTX19_P10	C8T28SOIDV_LL_SDFPRQNTX29_P10		
Clock 100Mhz Data 0Mhz	5.461e-03	5.428e-03		
Clock 100Mhz Data 25Mhz	6.146e-03	6.926e-03		
Clock 100Mhz Data 50Mhz	6.831e-03	8.424e-03		
Clock = 0 Data 100Mhz	2.678e-03	2.658e-03		
Clock = 1 Data 100Mhz	1.697e-04	1.457e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P10	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P10	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P10	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P10	C8T28SOI_LLHF_-SDFPRQTX3_P10	C8T28SOIDV_LL_-SDFPRQTX5_P10	C8T28SOIDV_LL_-SDFPRQTX10_P10
CP	0.0007	0.0006	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0008	0.0007	0.0008	0.0008
TE	0.0010	0.0010	0.0008	0.0008
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P10	C8T28SOIDV_LL_-SDFPRQTX29_P10		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0008		
TE	0.0008	0.0008		
TI	0.0003	0.0003		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQTX5_P10	**C8T28SOI_LLHF_-SDFPRQTX3_P10**	**C8T28SOI_LL_-SDFPRQTX5_P10**	**C8T28SOI_LLHF_-SDFPRQTX3_P10**
CP to Q ↓	0.1044	0.0899	4.8724	7.3762
CP to Q ↑	0.0809	0.0886	6.8718	10.5906
CP to TQ ↓	0.1232	0.0878	13.4866	8.2005
CP to TQ ↑	0.1039	0.0940	35.2025	19.0302
RN to Q ↓	0.0835	0.0811	4.4251	6.8583
RN to TQ ↓	0.0961	0.0808	12.9694	7.7799
	C8T28SOIDV_LL_-SDFPRQTX5_P10	**C8T28SOIDV_LL_-SDFPRQTX10_P10**	**C8T28SOIDV_LL_-SDFPRQTX5_P10**	**C8T28SOIDV_LL_-SDFPRQTX10_P10**
CP to Q ↓	0.0739	0.0993	4.3881	2.1154
CP to Q ↑	0.0923	0.1312	6.7884	3.3753
CP to TQ ↓	0.0748	0.1031	8.1136	7.9254
CP to TQ ↑	0.0962	0.1369	14.9182	14.8086
RN to Q ↓	0.0708	0.1029	4.3428	2.1150
RN to TQ ↓	0.0716	0.1068	8.0683	7.9243
	C8T28SOIDV_LL_-SDFPRQTX19_P10	**C8T28SOIDV_LL_-SDFPRQTX29_P10**	**C8T28SOIDV_LL_-SDFPRQTX19_P10**	**C8T28SOIDV_LL_-SDFPRQTX29_P10**
CP to Q ↓	0.1114	0.1070	1.1118	0.7441
CP to Q ↑	0.1400	0.1421	1.7125	1.1582
CP to TQ ↓	0.1170	0.1104	8.0058	7.8736
CP to TQ ↑	0.1482	0.1495	14.8124	15.2865
RN to Q ↓	0.1135	0.1099	1.1121	0.7433
RN to TQ ↓	0.1191	0.1133	8.0070	7.8739

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_-P10	C8T28SOI_-LLHF_-SDFPRQTX3_-P10	C8T28SOIDV_-LL_-SDFPRQTX5_-P10	C8T28SOIDV_-LL_-SDFPRQTX10_-P10
CP ↓	min_pulse_width to CP	0.1330	0.1247	0.1186	0.1162
CP ↑	min_pulse_width to CP	0.0877	0.0689	0.0577	0.0531
D ↓	hold_rising to CP	-0.0637	-0.1235	-0.0143	-0.0197
D ↑	hold_rising to CP	-0.0218	-0.0218	-0.0071	-0.0066
D ↓	setup_rising to CP	0.1074	0.1777	0.0737	0.0737
D ↑	setup_rising to CP	0.0515	0.0564	0.0368	0.0368
RN ↓	min_pulse_width to RN	0.0898	0.0854	0.0828	0.0686
RN ↑	recovery_rising to CP	0.0076	0.0059	0.0027	0.0005
RN ↑	removal_rising to CP	0.0095	0.0069	0.0086	0.0086
TE ↓	hold_rising to CP	-0.0457	-0.0506	-0.0121	-0.0121
TE ↑	hold_rising to CP	-0.0195	-0.0191	-0.0191	-0.0218
TE ↓	setup_rising to CP	0.1079	0.1467	0.0717	0.0685
TE ↑	setup_rising to CP	0.1345	0.1763	0.1350	0.1350
TI ↓	hold_rising to CP	-0.0828	-0.1211	-0.0753	-0.0746
TI ↑	hold_rising to CP	-0.0202	-0.0147	-0.0218	-0.0215
TI ↓	setup_rising to CP	0.1322	0.1655	0.1286	0.1286
TI ↑	setup_rising to CP	0.0515	0.0459	0.0515	0.0515
		C8T28SOIDV_-LL_-SDFPRQTX19_-P10	C8T28SOIDV_-LL_-SDFPRQTX29_-P10		
CP ↓	min_pulse_width to CP	0.1145	0.1162		
CP ↑	min_pulse_width to CP	0.0531	0.0531		
D ↓	hold_rising to CP	-0.0197	-0.0197		
D ↑	hold_rising to CP	-0.0066	-0.0066		
D ↓	setup_rising to CP	0.0742	0.0737		
D ↑	setup_rising to CP	0.0368	0.0368		
RN ↓	min_pulse_width to RN	0.0708	0.0708		
RN ↑	recovery_rising to CP	0.0005	0.0005		
RN ↑	removal_rising to CP	0.0086	0.0086		
TE ↓	hold_rising to CP	-0.0147	-0.0143		
TE ↑	hold_rising to CP	-0.0218	-0.0218		

TE ↓	setup_rising to CP	0.0685	0.0717		
TE ↑	setup_rising to CP	0.1350	0.1350		
TI ↓	hold_rising to CP	-0.0746	-0.0746		
TI ↑	hold_rising to CP	-0.0215	-0.0215		
TI ↓	setup_rising to CP	0.1286	0.1286		
TI ↑	setup_rising to CP	0.0515	0.0515		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P10	2.162e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P10	2.094e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P10	2.147e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P10	2.800e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P10	3.391e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P10	4.312e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

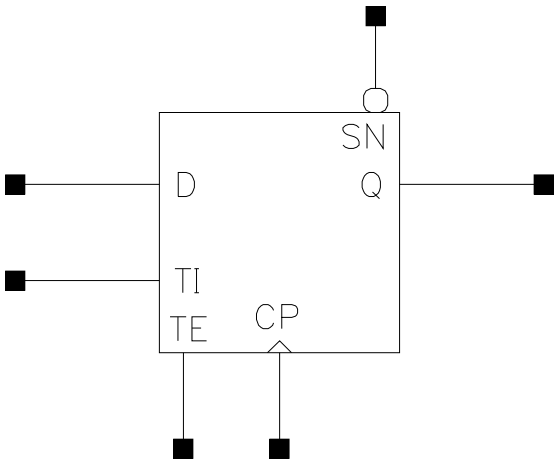
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P10	C8T28SOI_LLHF_-SDFPRQTX3_P10	C8T28SOIDV_LL_-SDFPRQTX5_P10	C8T28SOIDV_LL_-SDFPRQTX10_P10
Clock 100Mhz Data 0Mhz	6.128e-03	5.900e-03	5.630e-03	5.495e-03
Clock 100Mhz Data 25Mhz	6.090e-03	5.843e-03	5.587e-03	5.886e-03
Clock 100Mhz Data 50Mhz	6.053e-03	5.787e-03	5.544e-03	6.278e-03
Clock = 0 Data 100Mhz	2.708e-03	2.866e-03	2.762e-03	2.710e-03
Clock = 1 Data 100Mhz	2.331e-05	3.871e-04	2.664e-04	2.060e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P10	C8T28SOIDV_LL_-SDFPRQTX29_P10		
Clock 100Mhz Data 0Mhz	5.413e-03	5.360e-03		
Clock 100Mhz Data 25Mhz	6.269e-03	6.743e-03		
Clock 100Mhz Data 50Mhz	7.124e-03	8.126e-03		
Clock = 0 Data 100Mhz	2.679e-03	2.659e-03		
Clock = 1 Data 100Mhz	1.699e-04	1.458e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P10	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P10	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P10	C8T28SOI_LLHF_-SDFPSQX3_P10	C8T28SOIDV_LL_-SDFPSQX5_P10	C8T28SOIDV_LL_-SDFPSQX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0013	0.0013	0.0009	0.0010
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQX14_P10	C8T28SOIDV_LL_-SDFPSQX19_P10	C8T28SOIDV_LL_-SDFPSQX29_P10	
CP	0.0005	0.0005	0.0005	
D	0.0003	0.0003	0.0003	
SN	0.0010	0.0010	0.0010	
TE	0.0009	0.0009	0.0009	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P10	**C8T28SOI_LLHF_-SDFPSQX3_P10**	**C8T28SOI_LL_-SDFPSQX5_P10**	**C8T28SOI_LLHF_-SDFPSQX3_P10**
CP to Q ↓	0.0929	0.0818	4.7094	7.2685
CP to Q ↑	0.0776	0.0871	6.8677	10.4312
SN to Q ↑	0.0640	0.0580	6.7842	10.3162
	C8T28SOIDV_LL_-SDFPSQX5_P10	**C8T28SOIDV_LL_-SDFPSQX10_P10**	**C8T28SOIDV_LL_-SDFPSQX5_P10**	**C8T28SOIDV_LL_-SDFPSQX10_P10**
CP to Q ↓	0.0670	0.0992	4.2636	2.0504
CP to Q ↑	0.0850	0.1398	6.7317	3.3671
SN to Q ↑	0.0578	0.1094	6.7184	3.3678
	C8T28SOIDV_LL_-SDFPSQX14_P10	**C8T28SOIDV_LL_-SDFPSQX19_P10**	**C8T28SOIDV_LL_-SDFPSQX14_P10**	**C8T28SOIDV_LL_-SDFPSQX19_P10**
CP to Q ↓	0.0997	0.1062	1.3865	1.0599
CP to Q ↑	0.1395	0.1445	2.2539	1.6971
SN to Q ↑	0.1086	0.1136	2.2530	1.6981
	C8T28SOIDV_LL_-SDFPSQX29_P10		**C8T28SOIDV_LL_-SDFPSQX29_P10**	
CP to Q ↓	0.1053		0.7182	
CP to Q ↑	0.1517		1.1289	
SN to Q ↑	0.1209		1.1279	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P10	C8T28SOI_-LLHF_-SDFPSQX3_P10	C8T28SOIDV_-LL_SDFPSQX5_-P10	C8T28SOIDV_-LL_-SDFPSQX10_-P10
CP ↓	min_pulse_width to CP	0.1424	0.1419	0.1233	0.1234
CP ↑	min_pulse_width to CP	0.0783	0.0642	0.0530	0.0532
D ↓	hold_rising to CP	-0.0680	-0.1359	-0.0241	-0.0338
D ↑	hold_rising to CP	-0.0165	-0.0164	-0.0061	-0.0061
D ↓	setup_rising to CP	0.1203	0.1972	0.0888	0.0879
D ↑	setup_rising to CP	0.0466	0.0515	0.0368	0.0368

SN ↓	min_pulse_width to SN	0.0620	0.0522	0.0522	0.0549
SN ↑	recovery_rising to CP	0.0106	0.0102	0.0009	-0.0017
SN ↑	removal_rising to CP	0.0309	0.0407	0.0455	0.0449
TE ↓	hold_rising to CP	-0.0403	-0.0453	-0.0224	-0.0289
TE ↑	hold_rising to CP	-0.0142	-0.0137	-0.0066	-0.0147
TE ↓	setup_rising to CP	0.1176	0.1609	0.0835	0.0858
TE ↑	setup_rising to CP	0.1475	0.1936	0.1345	0.1296
TI ↓	hold_rising to CP	-0.0928	-0.1306	-0.0740	-0.0697
TI ↑	hold_rising to CP	-0.0169	-0.0141	-0.0049	-0.0169
TI ↓	setup_rising to CP	0.1420	0.1850	0.1331	0.1225
TI ↑	setup_rising to CP	0.0466	0.0453	0.0355	0.0453
		C8T28SOIDV_-LL_-SDFPSQX14_-P10	C8T28SOIDV_-LL_-SDFPSQX19_-P10	C8T28SOIDV_-LL_-SDFPSQX29_-P10	
CP ↓	min_pulse_width to CP	0.1210	0.1210	0.1210	
CP ↑	min_pulse_width to CP	0.0532	0.0532	0.0532	
D ↓	hold_rising to CP	-0.0338	-0.0338	-0.0338	
D ↑	hold_rising to CP	-0.0061	-0.0061	-0.0094	
D ↓	setup_rising to CP	0.0879	0.0879	0.0879	
D ↑	setup_rising to CP	0.0368	0.0368	0.0368	
SN ↓	min_pulse_width to SN	0.0522	0.0522	0.0549	
SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	
SN ↑	removal_rising to CP	0.0449	0.0449	0.0450	
TE ↓	hold_rising to CP	-0.0289	-0.0289	-0.0289	
TE ↑	hold_rising to CP	-0.0147	-0.0147	-0.0147	
TE ↓	setup_rising to CP	0.0858	0.0858	0.0858	
TE ↑	setup_rising to CP	0.1296	0.1296	0.1296	
TI ↓	hold_rising to CP	-0.0681	-0.0697	-0.0697	
TI ↑	hold_rising to CP	-0.0169	-0.0169	-0.0169	
TI ↓	setup_rising to CP	0.1225	0.1225	0.1225	
TI ↑	setup_rising to CP	0.0453	0.0453	0.0453	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds

C8T28SOI_LL_SDFPSQX5_P10	2.188e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQX3_P10	2.058e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P10	2.086e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P10	2.787e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P10	3.132e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P10	3.542e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P10	4.340e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

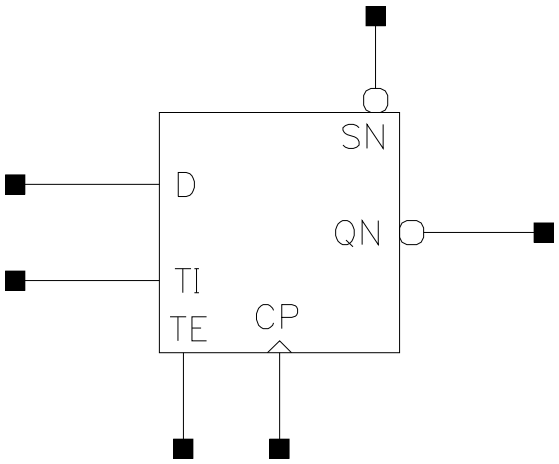
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P10	C8T28SOI_LLHF_-SDFPSQX3_P10	C8T28SOIDV_LL_-SDFPSQX5_P10	C8T28SOIDV_LL_-SDFPSQX10_P10
Clock 100Mhz Data 0Mhz	6.025e-03	5.740e-03	5.494e-03	5.372e-03
Clock 100Mhz Data 25Mhz	5.915e-03	5.618e-03	5.329e-03	5.698e-03
Clock 100Mhz Data 50Mhz	5.805e-03	5.496e-03	5.163e-03	6.024e-03
Clock = 0 Data 100Mhz	2.797e-03	2.947e-03	2.864e-03	2.843e-03
Clock = 1 Data 100Mhz	2.330e-05	3.826e-04	2.635e-04	2.041e-04
	C8T28SOIDV_LL_-SDFPSQX14_P10	C8T28SOIDV_LL_-SDFPSQX19_P10	C8T28SOIDV_LL_-SDFPSQX29_P10	
Clock 100Mhz Data 0Mhz	5.300e-03	5.251e-03	5.216e-03	
Clock 100Mhz Data 25Mhz	5.817e-03	6.107e-03	6.483e-03	
Clock 100Mhz Data 50Mhz	6.335e-03	6.962e-03	7.749e-03	
Clock = 0 Data 100Mhz	2.830e-03	2.822e-03	2.816e-03	
Clock = 1 Data 100Mhz	1.685e-04	1.448e-04	1.279e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P10	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P10	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P10	C8T28SOI_LLHF_-SDFPSQNX3_P10	C8T28SOIDV_LL_-SDFPSQNX5_P10	C8T28SOIDV_LL_-SDFPSQNX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0012	0.0012	0.0010	0.0010
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNX14_P10	C8T28SOIDV_LL_-SDFPSQNX19_P10	C8T28SOIDV_LL_-SDFPSQNX23_P10	C8T28SOIDV_LL_-SDFPSQNX29_P10
CP	0.0005	0.0005	0.0005	0.0005
D	0.0003	0.0003	0.0003	0.0003
SN	0.0010	0.0010	0.0010	0.0009
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNX5_P10	**C8T28SOI_LLHF_-SDFPSQNX3_P10**	**C8T28SOI_LL_-SDFPSQNX5_P10**	**C8T28SOI_LLHF_-SDFPSQNX3_P10**
CP to QN ↓	0.1076	0.1092	4.5673	6.6358
CP to QN ↑	0.1011	0.0929	7.1186	10.2324
SN to QN ↓	0.0955	0.0810	4.5712	6.6287
	C8T28SOIDV_LL_-SDFPSQNX5_P10	**C8T28SOIDV_LL_-SDFPSQNX10_P10**	**C8T28SOIDV_LL_-SDFPSQNX5_P10**	**C8T28SOIDV_LL_-SDFPSQNX10_P10**
CP to QN ↓	0.1156	0.1072	4.1006	2.0266
CP to QN ↑	0.0900	0.0917	6.6747	3.3431
SN to QN ↓	0.0873	0.0768	4.0967	2.0250
	C8T28SOIDV_LL_-SDFPSQNX14_P10	**C8T28SOIDV_LL_-SDFPSQNX19_P10**	**C8T28SOIDV_LL_-SDFPSQNX14_P10**	**C8T28SOIDV_LL_-SDFPSQNX19_P10**
CP to QN ↓	0.1114	0.1143	1.3896	1.0581
CP to QN ↑	0.0943	0.0973	2.2450	1.6891
SN to QN ↓	0.0789	0.0829	1.3863	1.0586
	C8T28SOIDV_LL_-SDFPSQNX23_P10	**C8T28SOIDV_LL_-SDFPSQNX29_P10**	**C8T28SOIDV_LL_-SDFPSQNX23_P10**	**C8T28SOIDV_LL_-SDFPSQNX29_P10**
CP to QN ↓	0.1159	0.1111	0.8204	0.7114
CP to QN ↑	0.0969	0.0989	1.6806	1.1284
SN to QN ↓	0.0853	0.0847	0.8193	0.7113

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P10	C8T28SOI_-LLHF_-SDFPSQNX3_-P10	C8T28SOIDV_-LL_-SDFPSQNX5_-P10	C8T28SOIDV_-LL_-SDFPSQNX10_-P10
CP ↓	min_pulse_width to CP	0.1424	0.1413	0.1233	0.1281
CP ↑	min_pulse_width to CP	0.0592	0.0547	0.0531	0.0576
D ↓	hold_rising to CP	-0.0680	-0.1359	-0.0241	-0.0241
D ↑	hold_rising to CP	-0.0165	-0.0164	-0.0061	-0.0061
D ↓	setup_rising to CP	0.1171	0.1972	0.0888	0.0888

D ↑	setup_rising to CP	0.0466	0.0515	0.0368	0.0368
SN ↓	min_pulse_width to SN	0.0593	0.0496	0.0522	0.0522
SN ↑	recovery_rising to CP	0.0106	0.0102	-0.0017	0.0005
SN ↑	removal_rising to CP	0.0309	0.0407	0.0455	0.0508
TE ↓	hold_rising to CP	-0.0403	-0.0453	-0.0219	-0.0224
TE ↑	hold_rising to CP	-0.0142	-0.0137	-0.0066	-0.0066
TE ↓	setup_rising to CP	0.1176	0.1609	0.0835	0.0835
TE ↑	setup_rising to CP	0.1475	0.1936	0.1345	0.1345
TI ↓	hold_rising to CP	-0.0928	-0.1299	-0.0740	-0.0697
TI ↑	hold_rising to CP	-0.0169	-0.0157	-0.0049	-0.0049
TI ↓	setup_rising to CP	0.1420	0.1850	0.1331	0.1331
TI ↑	setup_rising to CP	0.0466	0.0453	0.0355	0.0355
		C8T28SOIDV_-LL_-SDFPSQNX14_-P10	C8T28SOIDV_-LL_-SDFPSQNX19_-P10	C8T28SOIDV_-LL_-SDFPSQNX23_-P10	C8T28SOIDV_-LL_-SDFPSQNX29_-P10
CP ↓	min_pulse_width to CP	0.1281	0.1281	0.1281	0.1234
CP ↑	min_pulse_width to CP	0.0589	0.0624	0.0624	0.0637
D ↓	hold_rising to CP	-0.0241	-0.0241	-0.0241	-0.0241
D ↑	hold_rising to CP	-0.0061	-0.0061	-0.0061	-0.0061
D ↓	setup_rising to CP	0.0888	0.0888	0.0888	0.0883
D ↑	setup_rising to CP	0.0368	0.0368	0.0368	0.0368
SN ↓	min_pulse_width to SN	0.0549	0.0549	0.0571	0.0598
SN ↑	recovery_rising to CP	0.0009	0.0005	0.0009	0.0005
SN ↑	removal_rising to CP	0.0508	0.0508	0.0508	0.0455
TE ↓	hold_rising to CP	-0.0224	-0.0224	-0.0224	-0.0224
TE ↑	hold_rising to CP	-0.0066	-0.0066	-0.0066	-0.0039
TE ↓	setup_rising to CP	0.0835	0.0835	0.0835	0.0835
TE ↑	setup_rising to CP	0.1345	0.1345	0.1345	0.1345
TI ↓	hold_rising to CP	-0.0697	-0.0697	-0.0697	-0.0697
TI ↑	hold_rising to CP	-0.0049	-0.0049	-0.0049	-0.0049
TI ↓	setup_rising to CP	0.1331	0.1331	0.1331	0.1329
TI ↑	setup_rising to CP	0.0355	0.0355	0.0355	0.0355

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P10	2.141e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P10	2.020e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P10	2.080e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P10	2.822e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P10	3.075e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P10	3.464e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P10	3.676e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P10	4.361e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

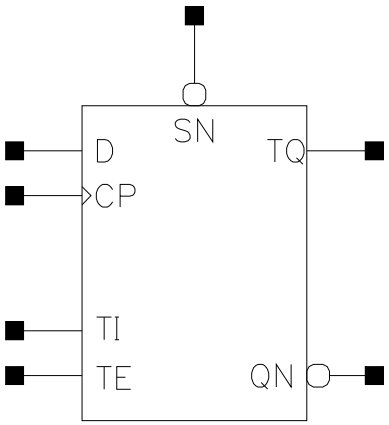
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P10	C8T28SOI_LLHF_-SDFPSQNX3_P10	C8T28SOIDV_LL_-SDFPSQNX5_P10	C8T28SOIDV_LL_-SDFPSQNX10_P10
Clock 100Mhz Data 0Mhz	6.013e-03	5.733e-03	5.487e-03	5.423e-03
Clock 100Mhz Data 25Mhz	5.840e-03	5.585e-03	5.417e-03	5.772e-03
Clock 100Mhz Data 50Mhz	5.667e-03	5.436e-03	5.348e-03	6.122e-03
Clock = 0 Data 100Mhz	2.796e-03	2.947e-03	2.864e-03	2.821e-03
Clock = 1 Data 100Mhz	2.333e-05	3.826e-04	2.635e-04	2.039e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P10	C8T28SOIDV_LL_-SDFPSQNX19_P10	C8T28SOIDV_LL_-SDFPSQNX23_P10	C8T28SOIDV_LL_-SDFPSQNX29_P10
Clock 100Mhz Data 0Mhz	5.383e-03	5.357e-03	5.339e-03	5.300e-03
Clock 100Mhz Data 25Mhz	5.923e-03	6.093e-03	6.170e-03	6.563e-03
Clock 100Mhz Data 50Mhz	6.462e-03	6.829e-03	7.001e-03	7.825e-03
Clock = 0 Data 100Mhz	2.795e-03	2.778e-03	2.766e-03	2.758e-03
Clock = 1 Data 100Mhz	1.682e-04	1.444e-04	1.275e-04	1.147e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P10	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P10	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P10	C8T28SOI_LLHF_-SDFPSQNTX3_P10	C8T28SOIDV_LL_-SDFPSQNTX5_P10	C8T28SOIDV_LL_-SDFPSQNTX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0013	0.0013	0.0009	0.0009
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNTX19_P10	C8T28SOIDV_LL_-SDFPSQNTX23_P10	C8T28SOIDV_LL_-SDFPSQNTX29_P10	
CP	0.0005	0.0005	0.0005	
D	0.0003	0.0003	0.0003	
SN	0.0009	0.0009	0.0009	
TE	0.0009	0.0009	0.0009	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P10	**C8T28SOI_LLHF_-SDFPSQNTX3_P10**	**C8T28SOI_LL_-SDFPSQNTX5_P10**	**C8T28SOI_LLHF_-SDFPSQNTX3_P10**
CP to QN ↓	0.1176	0.1175	4.6326	6.7184
CP to QN ↑	0.1184	0.1107	7.0625	10.2616
CP to TQ ↓	0.0979	0.0786	12.7133	8.0762
CP to TQ ↑	0.0964	0.0907	35.1342	18.8587
SN to QN ↓	0.1015	0.0867	4.6363	6.7272
SN to TQ ↑	0.0813	0.0612	35.0857	18.7958
	C8T28SOIDV_LL_-SDFPSQNTX5_P10	**C8T28SOIDV_LL_-SDFPSQNTX10_P10**	**C8T28SOIDV_LL_-SDFPSQNTX5_P10**	**C8T28SOIDV_LL_-SDFPSQNTX10_P10**
CP to QN ↓	0.1156	0.1073	4.1610	2.0164
CP to QN ↑	0.0929	0.0984	6.6773	3.3530
CP to TQ ↓	0.0650	0.0757	8.0021	8.1219
CP to TQ ↑	0.0870	0.0915	16.0496	16.1282
SN to QN ↓	0.0862	0.0798	4.1650	2.0166
SN to TQ ↑	0.0574	0.0640	16.0247	16.0605
	C8T28SOIDV_LL_-SDFPSQNTX19_P10	**C8T28SOIDV_LL_-SDFPSQNTX23_P10**	**C8T28SOIDV_LL_-SDFPSQNTX19_P10**	**C8T28SOIDV_LL_-SDFPSQNTX23_P10**
CP to QN ↓	0.1140	0.1170	1.0506	0.8183
CP to QN ↑	0.1046	0.1037	1.6909	1.6798
CP to TQ ↓	0.0754	0.0767	8.1206	8.1810
CP to TQ ↑	0.0914	0.0924	16.1329	16.1476
SN to QN ↓	0.0864	0.0893	1.0504	0.8169
SN to TQ ↑	0.0639	0.0650	16.0673	16.0808
	C8T28SOIDV_LL_-SDFPSQNTX29_P10		**C8T28SOIDV_LL_-SDFPSQNTX29_P10**	
CP to QN ↓	0.1156		0.7127	
CP to QN ↑	0.1065		1.1268	

CP to TQ ↓	0.0802		8.3379	
CP to TQ ↑	0.0987		18.7501	
SN to QN ↓	0.0880		0.7125	
SN to TQ ↑	0.0712		18.6563	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P10	C8T28SOI_-LLHF_-SDFPSQNTX3_-P10	C8T28SOIDV_-LL_-SDFPSQNTX5_-P10	C8T28SOIDV_-LL_SDFP-SQNTX10_P10
CP ↓	min_pulse_width to CP	0.1441	0.1419	0.1233	0.1233
CP ↑	min_pulse_width to CP	0.0735	0.0642	0.0577	0.0624
D ↓	hold_rising to CP	-0.0680	-0.1359	-0.0241	-0.0241
D ↑	hold_rising to CP	-0.0169	-0.0164	-0.0061	-0.0061
D ↓	setup_rising to CP	0.1220	0.1972	0.0888	0.0883
D ↑	setup_rising to CP	0.0466	0.0515	0.0368	0.0368
SN ↓	min_pulse_width to SN	0.0642	0.0544	0.0549	0.0549
SN ↑	recovery_rising to CP	0.0134	0.0102	0.0009	0.0005
SN ↑	removal_rising to CP	0.0309	0.0407	0.0450	0.0455
TE ↓	hold_rising to CP	-0.0408	-0.0453	-0.0224	-0.0224
TE ↑	hold_rising to CP	-0.0142	-0.0137	-0.0066	-0.0039
TE ↓	setup_rising to CP	0.1204	0.1609	0.0835	0.0835
TE ↑	setup_rising to CP	0.1492	0.1936	0.1345	0.1378
TI ↓	hold_rising to CP	-0.0925	-0.1306	-0.0740	-0.0697
TI ↑	hold_rising to CP	-0.0153	-0.0157	-0.0049	-0.0049
TI ↓	setup_rising to CP	0.1469	0.1850	0.1331	0.1329
TI ↑	setup_rising to CP	0.0466	0.0453	0.0355	0.0355
		C8T28SOIDV_-LL_SDFP-SQNTX19_P10	C8T28SOIDV_-LL_SDFP-SQNTX23_P10	C8T28SOIDV_-LL_SDFP-SQNTX29_P10	
CP ↓	min_pulse_width to CP	0.1233	0.1233	0.1234	
CP ↑	min_pulse_width to CP	0.0672	0.0672	0.0684	
D ↓	hold_rising to CP	-0.0241	-0.0241	-0.0241	
D ↑	hold_rising to CP	-0.0061	-0.0061	-0.0066	
D ↓	setup_rising to CP	0.0883	0.0883	0.0888	
D ↑	setup_rising to CP	0.0368	0.0368	0.0368	
SN ↓	min_pulse_width to SN	0.0571	0.0571	0.0598	

SN ↑	recovery_rising to CP	0.0005	0.0005	0.0005	
SN ↑	removal_rising to CP	0.0455	0.0455	0.0455	
TE ↓	hold_rising to CP	-0.0224	-0.0224	-0.0224	
TE ↑	hold_rising to CP	-0.0039	-0.0039	-0.0039	
TE ↓	setup_rising to CP	0.0835	0.0835	0.0835	
TE ↑	setup_rising to CP	0.1378	0.1378	0.1378	
TI ↓	hold_rising to CP	-0.0697	-0.0697	-0.0697	
TI ↑	hold_rising to CP	-0.0049	-0.0049	-0.0049	
TI ↓	setup_rising to CP	0.1329	0.1329	0.1329	
TI ↑	setup_rising to CP	0.0355	0.0355	0.0355	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P10	2.150e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P10	2.182e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P10	2.263e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_-P10	2.990e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_-P10	3.651e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_-P10	3.887e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_-P10	4.513e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P10	C8T28SOI_LLHF_-SDFPSQNTX3_P10	C8T28SOIDV_LL_-SDFPSQNTX5_P10	C8T28SOIDV_LL_-SDFPSQNTX10_P10
Clock 100Mhz Data 0Mhz	5.819e-03	5.636e-03	5.426e-03	5.321e-03
Clock 100Mhz Data 25Mhz	5.879e-03	5.689e-03	5.449e-03	5.807e-03
Clock 100Mhz Data 50Mhz	5.939e-03	5.742e-03	5.473e-03	6.293e-03
Clock = 0 Data 100Mhz	2.792e-03	2.945e-03	2.862e-03	2.822e-03
Clock = 1 Data 100Mhz	2.331e-05	3.833e-04	2.639e-04	2.043e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P10	C8T28SOIDV_LL_-SDFPSQNTX23_P10	C8T28SOIDV_LL_-SDFPSQNTX29_P10	
Clock 100Mhz Data 0Mhz	5.258e-03	5.216e-03	5.186e-03	
Clock 100Mhz Data 25Mhz	6.134e-03	6.219e-03	6.621e-03	
Clock 100Mhz Data 50Mhz	7.009e-03	7.223e-03	8.056e-03	

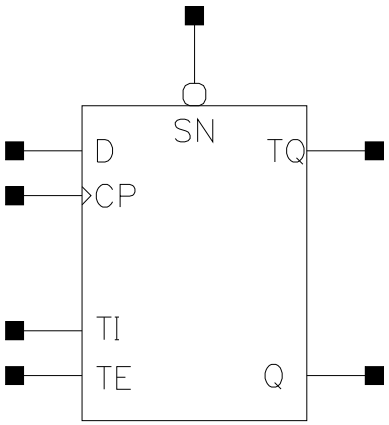
Clock = 0 Data 100Mhz	2.797e-03	2.781e-03	2.770e-03	
Clock = 1 Data 100Mhz	1.685e-04	1.447e-04	1.277e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P10	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P10	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P10	C8T28SOI_LLHF_-SDFPSQTX3_P10	C8T28SOIDV_LL_-SDFPSQTX5_P10	C8T28SOIDV_LL_-SDFPSQTX10_P10
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0004	0.0003	0.0003
SN	0.0013	0.0013	0.0009	0.0010
TE	0.0010	0.0010	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQTX19_P10	C8T28SOIDV_LL_-SDFPSQTX29_P10		
CP	0.0005	0.0005		
D	0.0003	0.0003		
SN	0.0010	0.0010		
TE	0.0009	0.0009		
TI	0.0004	0.0004		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQTX5_P10	**C8T28SOI_LLHF_-SDFPSQTX3_P10**	**C8T28SOI_LL_-SDFPSQTX5_P10**	**C8T28SOI_LLHF_-SDFPSQTX3_P10**
CP to Q ↓	0.1003	0.0909	4.9180	7.4765
CP to Q ↑	0.0820	0.0906	6.8695	10.6090
CP to TQ ↓	0.1194	0.0886	13.3723	8.2745
CP to TQ ↑	0.1058	0.0960	35.1566	19.0459
SN to Q ↑	0.0669	0.0606	6.7835	10.4870
SN to TQ ↑	0.0877	0.0651	35.0452	18.9514
	C8T28SOIDV_LL_-SDFPSQTX5_P10	**C8T28SOIDV_LL_-SDFPSQTX10_P10**	**C8T28SOIDV_LL_-SDFPSQTX5_P10**	**C8T28SOIDV_LL_-SDFPSQTX10_P10**
CP to Q ↓	0.0752	0.0978	4.3846	2.1034
CP to Q ↑	0.0883	0.1381	6.8080	3.3831
CP to TQ ↓	0.0763	0.1009	8.1188	8.2875
CP to TQ ↑	0.0919	0.1440	16.1802	16.0100
SN to Q ↑	0.0607	0.1071	6.7857	3.3848
SN to TQ ↑	0.0643	0.1130	16.1184	16.0034
	C8T28SOIDV_LL_-SDFPSQTX19_P10	**C8T28SOIDV_LL_-SDFPSQTX29_P10**	**C8T28SOIDV_LL_-SDFPSQTX19_P10**	**C8T28SOIDV_LL_-SDFPSQTX29_P10**
CP to Q ↓	0.1067	0.1197	1.0879	0.7020
CP to Q ↑	0.1456	0.1584	1.7262	1.1454
CP to TQ ↓	0.1076	0.0668	6.9829	7.2577
CP to TQ ↑	0.1529	0.0963	18.6159	18.7211
SN to Q ↑	0.1146	0.1273	1.7261	1.1458
SN to TQ ↑	0.1219	0.0657	18.6137	18.7057

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_-P10	C8T28SOI_-LLHF_-SDFPSQTX3_-P10	C8T28SOIDV_-LL_-SDFPSQTX5_-P10	C8T28SOIDV_-LL_-SDFPSQTX10_-P10
CP ↓	min_pulse_width to CP	0.1440	0.1419	0.1233	0.1258
CP ↑	min_pulse_width to CP	0.0878	0.0689	0.0589	0.0532
D ↓	hold_rising to CP	-0.0680	-0.1359	-0.0241	-0.0338
D ↑	hold_rising to CP	-0.0169	-0.0164	-0.0061	-0.0094
D ↓	setup_rising to CP	0.1220	0.1998	0.0883	0.0937
D ↑	setup_rising to CP	0.0466	0.0515	0.0368	0.0368
SN ↓	min_pulse_width to SN	0.0669	0.0544	0.0549	0.0522
SN ↑	recovery_rising to CP	0.0134	0.0134	0.0005	-0.0017
SN ↑	removal_rising to CP	0.0309	0.0407	0.0450	0.0449
TE ↓	hold_rising to CP	-0.0408	-0.0453	-0.0224	-0.0289
TE ↑	hold_rising to CP	-0.0142	-0.0137	-0.0066	-0.0142
TE ↓	setup_rising to CP	0.1199	0.1609	0.0835	0.0858
TE ↑	setup_rising to CP	0.1492	0.1931	0.1345	0.1329
TI ↓	hold_rising to CP	-0.0925	-0.1309	-0.0740	-0.0697
TI ↑	hold_rising to CP	-0.0153	-0.0141	-0.0049	-0.0169
TI ↓	setup_rising to CP	0.1469	0.1850	0.1329	0.1240
TI ↑	setup_rising to CP	0.0466	0.0453	0.0355	0.0466
		C8T28SOIDV_-LL_-SDFPSQTX19_-P10	C8T28SOIDV_-LL_-SDFPSQTX29_-P10		
CP ↓	min_pulse_width to CP	0.1210	0.1227		
CP ↑	min_pulse_width to CP	0.0532	0.0592		
D ↓	hold_rising to CP	-0.0338	-0.0344		
D ↑	hold_rising to CP	-0.0094	-0.0061		
D ↓	setup_rising to CP	0.0879	0.0879		
D ↑	setup_rising to CP	0.0368	0.0368		
SN ↓	min_pulse_width to SN	0.0522	0.0647		
SN ↑	recovery_rising to CP	-0.0017	-0.0017		
SN ↑	removal_rising to CP	0.0449	0.0482		
TE ↓	hold_rising to CP	-0.0289	-0.0290		
TE ↑	hold_rising to CP	-0.0147	-0.0147		

TE ↓	setup_rising to CP	0.0858	0.0858		
TE ↑	setup_rising to CP	0.1296	0.1296		
TI ↓	hold_rising to CP	-0.0697	-0.0691		
TI ↑	hold_rising to CP	-0.0169	-0.0169		
TI ↓	setup_rising to CP	0.1225	0.1225		
TI ↑	setup_rising to CP	0.0453	0.0450		

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P10	2.192e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P10	2.215e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P10	2.285e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P10	2.933e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P10	3.603e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P10	4.618e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

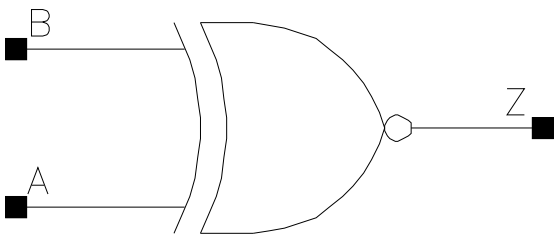
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P10	C8T28SOI_LLHF_-SDFPSQTX3_P10	C8T28SOIDV_LL_-SDFPSQTX5_P10	C8T28SOIDV_LL_-SDFPSQTX10_P10
Clock 100Mhz Data 0Mhz	5.826e-03	5.643e-03	5.432e-03	5.326e-03
Clock 100Mhz Data 25Mhz	5.899e-03	5.694e-03	5.450e-03	5.755e-03
Clock 100Mhz Data 50Mhz	5.972e-03	5.745e-03	5.469e-03	6.185e-03
Clock = 0 Data 100Mhz	2.792e-03	2.945e-03	2.862e-03	2.850e-03
Clock = 1 Data 100Mhz	2.332e-05	3.832e-04	2.639e-04	2.045e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P10	C8T28SOIDV_LL_-SDFPSQTX29_P10		
Clock 100Mhz Data 0Mhz	5.262e-03	5.221e-03		
Clock 100Mhz Data 25Mhz	6.178e-03	6.665e-03		
Clock 100Mhz Data 50Mhz	7.095e-03	8.110e-03		
Clock = 0 Data 100Mhz	2.836e-03	2.827e-03		
Clock = 1 Data 100Mhz	1.689e-04	1.451e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.600	0.544	0.8704
X5_P10	0.800	1.496	1.1968
X8_P10	1.600	1.088	1.7408
X9_P10	0.800	1.632	1.3056
X11_P10	1.600	1.360	2.1760
X14_P10	0.800	2.312	1.8496
X15_P10	1.600	1.904	3.0464
X19_P10	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P10	X5_P10	X8_P10	X9_P10
A	0.0010	0.0005	0.0016	0.0006
B	0.0009	0.0009	0.0013	0.0012
	X11_P10	X14_P10	X15_P10	X19_P10
A	0.0024	0.0009	0.0028	0.0011
B	0.0022	0.0015	0.0026	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X5_P10	X4_P10	X5_P10
A to Z ↓	0.0220	0.0660	5.8768	4.4383
A to Z ↑	0.0254	0.0587	9.5964	7.2423
B to Z ↓	0.0210	0.0484	5.8727	4.4237
B to Z ↑	0.0261	0.0444	9.6062	7.2364

	X8_P10	X9_P10	X8_P10	X9_P10
A to Z ↓	0.0262	0.0604	3.0729	2.2810
A to Z ↑	0.0309	0.0548	5.0288	3.6822
B to Z ↓	0.0252	0.0454	3.0709	2.2766
B to Z ↑	0.0303	0.0425	5.0354	3.6829
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0242	0.0574	2.1448	1.5422
A to Z ↑	0.0279	0.0509	3.2981	2.3474
B to Z ↓	0.0223	0.0423	2.1426	1.5365
B to Z ↑	0.0268	0.0396	3.3046	2.3453
	X15_P10	**X19_P10**	**X15_P10**	**X19_P10**
A to Z ↓	0.0267	0.0526	1.6191	1.1473
A to Z ↑	0.0310	0.0481	2.5030	1.7506
B to Z ↓	0.0247	0.0398	1.6166	1.1456
B to Z ↑	0.0298	0.0380	2.5062	1.7506

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	1.030e-05	1.000e-20
X5_P10	1.176e-05	1.000e-20
X8_P10	1.651e-05	1.000e-20
X9_P10	1.886e-05	1.000e-20
X11_P10	2.477e-05	1.000e-20
X14_P10	2.836e-05	1.000e-20
X15_P10	3.150e-05	1.000e-20
X19_P10	3.901e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X5_P10	X8_P10	X9_P10
A to Z	1.278e-03	2.745e-03	2.542e-03	3.810e-03
B to Z	1.257e-03	2.179e-03	2.497e-03	3.029e-03
	X11_P10	X14_P10	X15_P10	X19_P10
A to Z	3.563e-03	5.992e-03	4.868e-03	7.231e-03
B to Z	3.425e-03	4.660e-03	4.707e-03	5.751e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

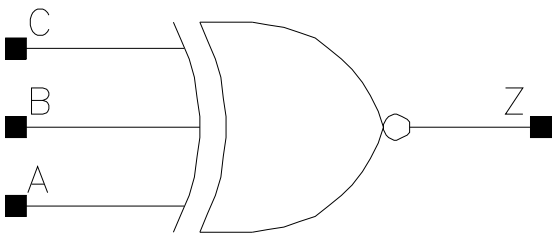
Pin Cycle (vdds)	X4_P10	X5_P10	X8_P10	X9_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P10	X14_P10	X15_P10	X19_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P10	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P10	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P10	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P10	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P10	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P10	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P10	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P10	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P10	C8T28SOIDV_LL_-XNOR3X4_P10	C8T28SOIDV_LL_-XNOR3X9_P10	C8T28SOIDV_LL_-XNOR3X13_P10
A	0.0015	0.0015	0.0019	0.0025
B	0.0014	0.0014	0.0018	0.0024
C	0.0006	0.0006	0.0006	0.0006
	C8T28SOIDV_LLS_-XNOR3X1_P10	C8T28SOIDV_LLS_-XNOR3X2_P10	C8T28SOIDV_LLS_-XNOR3X5_P10	C8T28SOIDV_LLS_-XNOR3X7_P10

A	0.0014	0.0016	0.0035	0.0053
B	0.0015	0.0017	0.0032	0.0051
C	0.0010	0.0012	0.0023	0.0034

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XNOR3X2_P10	**C8T28SOIDV_LL_-XNOR3X4_P10**	**C8T28SOIDV_LL_-XNOR3X2_P10**	**C8T28SOIDV_LL_-XNOR3X4_P10**
A to Z ↓	0.0683	0.0727	9.3219	4.8449
A to Z ↑	0.0650	0.0660	13.6168	7.3440
B to Z ↓	0.0689	0.0735	9.3240	4.8447
B to Z ↑	0.0658	0.0669	13.6168	7.3495
C to Z ↓	0.0921	0.0981	9.3202	4.8438
C to Z ↑	0.0890	0.0913	13.6168	7.3481
	C8T28SOIDV_LL_-XNOR3X9_P10	**C8T28SOIDV_LL_-XNOR3X13_P10**	**C8T28SOIDV_LL_-XNOR3X9_P10**	**C8T28SOIDV_LL_-XNOR3X13_P10**
A to Z ↓	0.0612	0.0704	2.4282	1.6568
A to Z ↑	0.0638	0.0721	3.5845	2.4687
B to Z ↓	0.0622	0.0713	2.4277	1.6565
B to Z ↑	0.0651	0.0736	3.5855	2.4698
C to Z ↓	0.0888	0.1068	2.4273	1.6570
C to Z ↑	0.0914	0.1093	3.5854	2.4680
	C8T28SOIDV_LLS_-XNOR3X1_P10	**C8T28SOIDV_LLS_-XNOR3X2_P10**	**C8T28SOIDV_LLS_-XNOR3X1_P10**	**C8T28SOIDV_LLS_-XNOR3X2_P10**
A to Z ↓	0.0405	0.0455	17.3323	9.2405
A to Z ↑	0.0425	0.0415	29.1216	14.9014
B to Z ↓	0.0415	0.0468	17.3385	9.2409
B to Z ↑	0.0434	0.0427	29.0957	14.8933
C to Z ↓	0.0399	0.0439	17.3312	9.2517
C to Z ↑	0.0424	0.0407	29.0524	14.8870
	C8T28SOIDV_LLS_-XNOR3X5_P10	**C8T28SOIDV_LLS_-XNOR3X7_P10**	**C8T28SOIDV_LLS_-XNOR3X5_P10**	**C8T28SOIDV_LLS_-XNOR3X7_P10**
A to Z ↓	0.0455	0.0384	4.3567	3.0167
A to Z ↑	0.0436	0.0375	7.2646	4.8539
B to Z ↓	0.0447	0.0372	4.3615	3.0227
B to Z ↑	0.0430	0.0369	7.2592	4.8510
C to Z ↓	0.0424	0.0355	4.3548	3.0222
C to Z ↑	0.0408	0.0347	7.2480	4.8481

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P10	7.946e-06	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P10	9.446e-06	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P10	1.648e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P10	2.339e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P10	5.262e-06	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P10	8.911e-06	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P10	2.151e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P10	3.218e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P10	C8T28SOIDV_LL_-XNOR3X4_P10	C8T28SOIDV_LL_-XNOR3X9_P10	C8T28SOIDV_LL_-XNOR3X13_P10
A to Z	1.707e-03	2.027e-03	3.010e-03	5.010e-03
B to Z	1.693e-03	2.014e-03	3.030e-03	5.042e-03
C to Z	2.695e-03	3.060e-03	4.329e-03	7.046e-03
	C8T28SOIDV_LLS_-XNOR3X1_P10	C8T28SOIDV_LLS_-XNOR3X2_P10	C8T28SOIDV_LLS_-XNOR3X5_P10	C8T28SOIDV_LLS_-XNOR3X7_P10
A to Z	1.012e-03	1.484e-03	3.278e-03	4.484e-03
B to Z	1.008e-03	1.509e-03	3.318e-03	4.425e-03
C to Z	9.833e-04	1.487e-03	3.240e-03	4.322e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

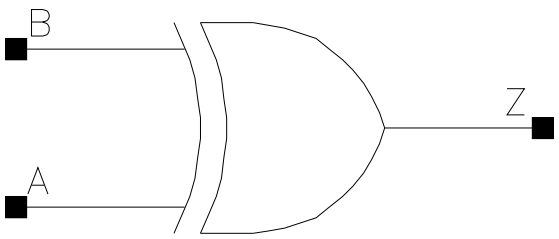
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P10	C8T28SOIDV_LL_-XNOR3X4_P10	C8T28SOIDV_LL_-XNOR3X9_P10	C8T28SOIDV_LL_-XNOR3X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P10	C8T28SOIDV_LLS_-XNOR3X2_P10	C8T28SOIDV_LLS_-XNOR3X5_P10	C8T28SOIDV_LLS_-XNOR3X7_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.360	1.0880
X4_P10	1.600	0.544	0.8704
X5_P10	0.800	1.360	1.0880
X8_P10	1.600	1.088	1.7408
X9_P10	0.800	1.496	1.1968
X12_P10	1.600	1.360	2.1760
X13_P10	0.800	2.176	1.7408
X15_P10	1.600	1.904	3.0464
X17_P10	0.800	2.312	1.8496
X18_P10	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P10	X4_P10	X5_P10	X8_P10
A	0.0005	0.0010	0.0006	0.0016
B	0.0010	0.0009	0.0011	0.0015
	X9_P10	X12_P10	X13_P10	X15_P10
A	0.0006	0.0025	0.0011	0.0029
B	0.0014	0.0019	0.0021	0.0024
	X17_P10	X18_P10		
A	0.0011	0.0015		
B	0.0021	0.0019		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X4_P10**	**X2_P10**	**X4_P10**
A to Z ↓	0.0563	0.0232	8.8487	4.4695
A to Z ↑	0.0535	0.0272	13.9805	12.6100
B to Z ↓	0.0425	0.0234	8.7819	4.4956
B to Z ↑	0.0440	0.0256	13.9837	12.5964
	X5_P10	**X8_P10**	**X5_P10**	**X8_P10**
A to Z ↓	0.0520	0.0303	4.5521	2.3964
A to Z ↑	0.0469	0.0325	7.0764	6.5294
B to Z ↓	0.0390	0.0310	4.5351	2.4116
B to Z ↑	0.0382	0.0311	7.0697	6.5212
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0503	0.0271	2.3982	1.6166
A to Z ↑	0.0467	0.0290	3.6489	4.3677
B to Z ↓	0.0379	0.0257	2.3912	1.6274
B to Z ↑	0.0373	0.0266	3.6498	4.3621
	X13_P10	**X15_P10**	**X13_P10**	**X15_P10**
A to Z ↓	0.0463	0.0294	1.6296	1.2474
A to Z ↑	0.0431	0.0334	2.5265	3.8679
B to Z ↓	0.0320	0.0277	1.6251	1.2565
B to Z ↑	0.0305	0.0308	2.5217	3.8620
	X17_P10	**X18_P10**	**X17_P10**	**X18_P10**
A to Z ↓	0.0489	0.0539	1.2374	1.2455
A to Z ↑	0.0449	0.0483	1.8940	1.8491
B to Z ↓	0.0347	0.0411	1.2343	1.2451
B to Z ↑	0.0325	0.0375	1.8916	1.8479

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X2_P10	9.100e-06	1.000e-20
X4_P10	1.053e-05	1.000e-20
X5_P10	1.408e-05	1.000e-20
X8_P10	1.707e-05	1.000e-20
X9_P10	2.225e-05	1.000e-20
X12_P10	2.571e-05	1.000e-20
X13_P10	3.573e-05	1.000e-20
X15_P10	3.129e-05	1.000e-20
X17_P10	3.842e-05	1.000e-20
X18_P10	3.839e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X2_P10	X4_P10	X5_P10	X8_P10
A to Z	2.008e-03	1.308e-03	2.538e-03	2.609e-03
B to Z	1.755e-03	1.259e-03	2.167e-03	2.595e-03
	X9_P10	X12_P10	X13_P10	X15_P10
A to Z	3.627e-03	3.657e-03	5.908e-03	4.786e-03
B to Z	3.152e-03	3.477e-03	3.827e-03	4.590e-03
	X17_P10	X18_P10		
A to Z	6.641e-03	7.341e-03		
B to Z	4.538e-03	5.569e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

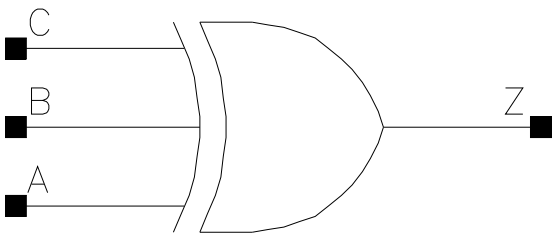
Pin Cycle (vdds)	X2_P10	X4_P10	X5_P10	X8_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P10	X12_P10	X13_P10	X15_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P10	X18_P10		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P10	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P10	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P10	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P10	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P10	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P10	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P10	C8T28SOIDV_LL_-XOR3X4_P10	C8T28SOIDV_LL_-XOR3X9_P10	C8T28SOIDV_LL_-XOR3X13_P10
A	0.0015	0.0014	0.0017	0.0025
B	0.0015	0.0015	0.0018	0.0024
C	0.0009	0.0009	0.0013	0.0020
	C8T28SOIDV_LLS_-XOR3X1_P10	C8T28SOIDV_LLS_-XOR3X2_P10	C8T28SOIDV_LLS_-XOR3X5_P10	C8T28SOIDV_LLS_-XOR3X7_P10

A	0.0015	0.0017	0.0028	0.0043
B	0.0016	0.0016	0.0027	0.0044
C	0.0005	0.0005	0.0005	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P10	**C8T28SOIDV_LL_-XOR3X4_P10**	**C8T28SOIDV_LL_-XOR3X2_P10**	**C8T28SOIDV_LL_-XOR3X4_P10**
A to Z ↓	0.0664	0.0731	9.3743	4.8595
A to Z ↑	0.0635	0.0681	13.9996	7.3400
B to Z ↓	0.0667	0.0742	9.3736	4.8591
B to Z ↑	0.0641	0.0696	14.0111	7.3446
C to Z ↓	0.0659	0.0730	9.3705	4.8609
C to Z ↑	0.0627	0.0676	14.0054	7.3462
	C8T28SOIDV_LL_-XOR3X9_P10	**C8T28SOIDV_LL_-XOR3X13_P10**	**C8T28SOIDV_LL_-XOR3X9_P10**	**C8T28SOIDV_LL_-XOR3X13_P10**
A to Z ↓	0.0649	0.0725	2.4123	1.6040
A to Z ↑	0.0657	0.0737	3.5967	2.4195
B to Z ↓	0.0662	0.0733	2.4129	1.6038
B to Z ↑	0.0673	0.0751	3.5998	2.4222
C to Z ↓	0.0644	0.0725	2.4124	1.6046
C to Z ↑	0.0646	0.0743	3.5976	2.4210
	C8T28SOIDV_LLS_-XOR3X1_P10	**C8T28SOIDV_LLS_-XOR3X2_P10**	**C8T28SOIDV_LLS_-XOR3X1_P10**	**C8T28SOIDV_LLS_-XOR3X2_P10**
A to Z ↓	0.0426	0.0473	12.0716	9.4489
A to Z ↑	0.0427	0.0415	20.7313	14.2097
B to Z ↓	0.0437	0.0481	12.0973	9.4511
B to Z ↑	0.0438	0.0422	20.7311	14.1990
C to Z ↓	0.0675	0.0731	12.1016	9.4364
C to Z ↑	0.0689	0.0682	20.7351	14.1720
	C8T28SOIDV_LLS_-XOR3X5_P10	**C8T28SOIDV_LLS_-XOR3X7_P10**	**C8T28SOIDV_LLS_-XOR3X5_P10**	**C8T28SOIDV_LLS_-XOR3X7_P10**
A to Z ↓	0.0636	0.0539	4.8374	3.3506
A to Z ↑	0.0523	0.0448	7.3253	4.9287
B to Z ↓	0.0602	0.0531	4.8486	3.3545
B to Z ↑	0.0510	0.0448	7.3248	4.9284
C to Z ↓	0.1017	0.0841	4.8645	3.3541
C to Z ↑	0.0928	0.0756	7.3175	4.9196

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P10	6.471e-06	1.000e-20
C8T28SOIDV_LL_XOR3X4_P10	8.122e-06	1.000e-20
C8T28SOIDV_LL_XOR3X9_P10	1.464e-05	1.000e-20
C8T28SOIDV_LL_XOR3X13_P10	2.190e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P10	9.015e-06	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P10	1.058e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P10	1.835e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P10	2.734e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P10	C8T28SOIDV_LL_-XOR3X4_P10	C8T28SOIDV_LL_-XOR3X9_P10	C8T28SOIDV_LL_-XOR3X13_P10
A to Z	1.621e-03	2.023e-03	3.039e-03	5.325e-03
B to Z	1.602e-03	2.022e-03	3.062e-03	5.346e-03
C to Z	1.577e-03	1.989e-03	3.039e-03	5.347e-03
	C8T28SOIDV_LLS_-XOR3X1_P10	C8T28SOIDV_LLS_-XOR3X2_P10	C8T28SOIDV_LLS_-XOR3X5_P10	C8T28SOIDV_LLS_-XOR3X7_P10
A to Z	1.242e-03	1.522e-03	3.061e-03	4.243e-03
B to Z	1.245e-03	1.545e-03	3.108e-03	4.307e-03
C to Z	2.382e-03	2.751e-03	5.120e-03	7.123e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P10	C8T28SOIDV_LL_-XOR3X4_P10	C8T28SOIDV_LL_-XOR3X9_P10	C8T28SOIDV_LL_-XOR3X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P10	C8T28SOIDV_LLS_-XOR3X2_P10	C8T28SOIDV_LLS_-XOR3X5_P10	C8T28SOIDV_LLS_-XOR3X7_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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