C28SOI_SC_12_COREPBP10_LR Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 10 nm

Overview

- C28SOI_SC_12_COREPBP10_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

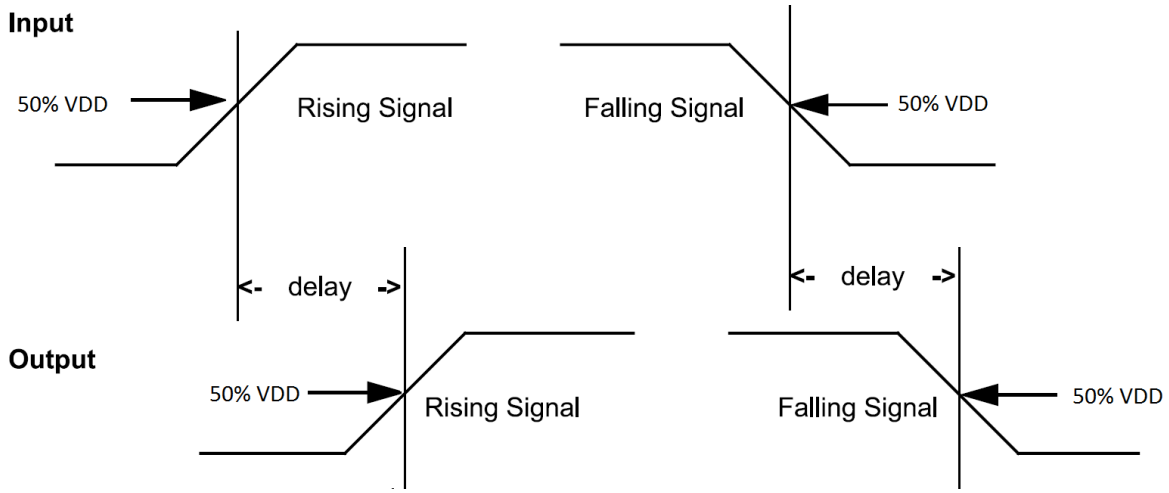


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

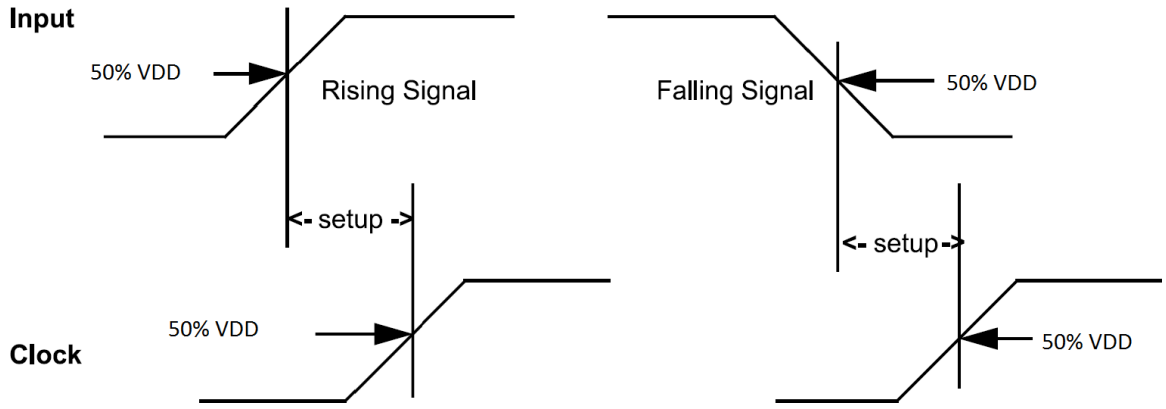


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

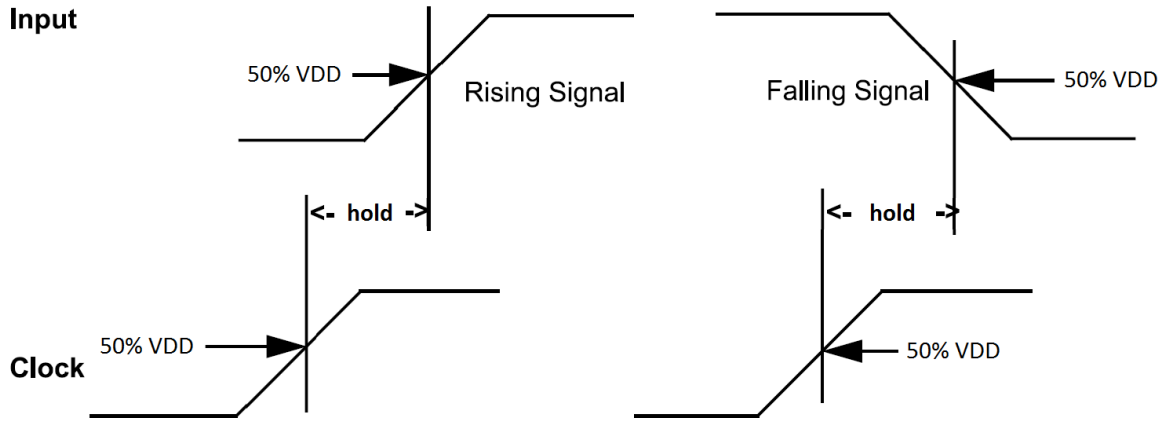


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

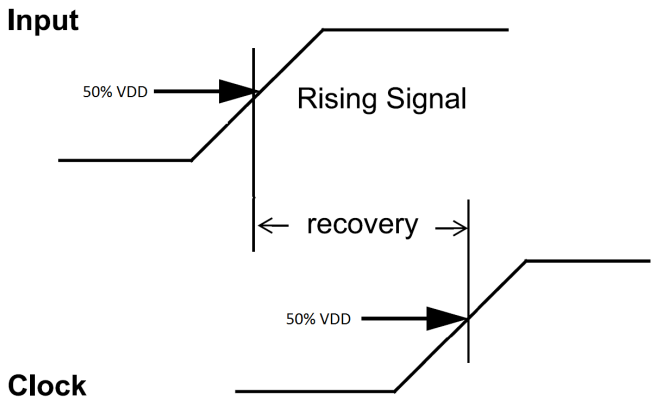


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

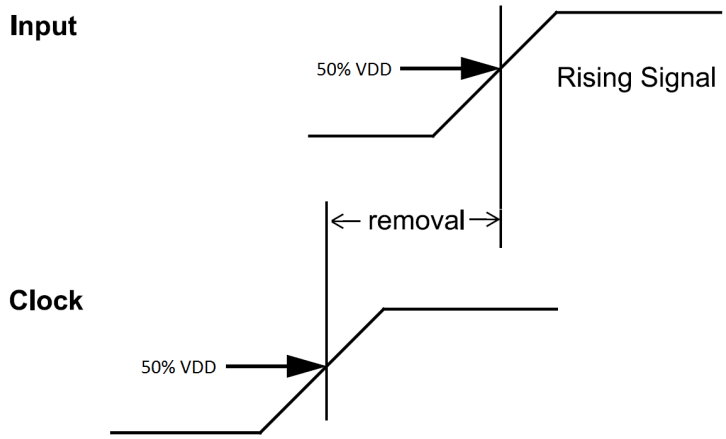


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

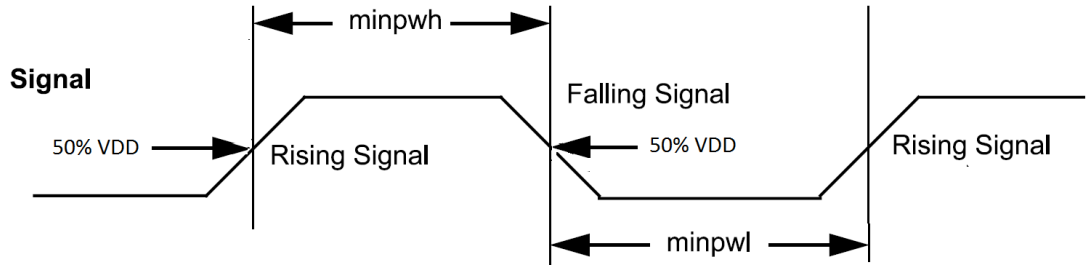


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

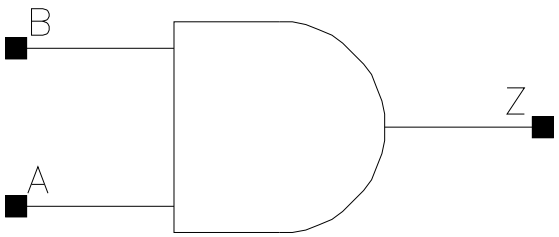
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X25_P10	1.200	1.088	1.3056
X33_P10	1.200	1.360	1.6320
X42_P10	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0008	0.0011	0.0017	0.0021
B	0.0007	0.0011	0.0016	0.0021
	X42_P10			
A	0.0021			
B	0.0021			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0412	0.0346	2.0125	1.0206
A to Z ↑	0.0311	0.0289	3.8653	1.8699
B to Z ↓	0.0393	0.0328	2.0103	1.0207
B to Z ↑	0.0324	0.0298	3.8624	1.8731
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0354	0.0343	0.6781	0.5031

A to Z ↑	0.0285	0.0291	1.2361	0.9329
B to Z ↓	0.0337	0.0318	0.6783	0.5028
B to Z ↑	0.0295	0.0293	1.2364	0.9334
	X42_P10		**X42_P10**	
A to Z ↓	0.0368		0.4102	
A to Z ↑	0.0314		0.7469	
B to Z ↓	0.0343		0.4093	
B to Z ↑	0.0318		0.7469	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	8.692e-08	1.772e-12
X16_P10	1.629e-07	2.024e-12
X25_P10	2.468e-07	2.776e-12
X33_P10	3.340e-07	3.282e-12
X42_P10	3.800e-07	3.535e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	1.092e-05	1.950e-05	3.089e-05	5.516e-05
B (output stable)	4.195e-05	7.746e-05	1.214e-04	3.964e-04
A to Z	2.372e-03	3.863e-03	5.932e-03	7.740e-03
B to Z	2.222e-03	3.593e-03	5.511e-03	6.942e-03
	X42_P10			
A (output stable)	5.417e-05			
B (output stable)	4.003e-04			
A to Z	9.226e-03			
B to Z	8.421e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

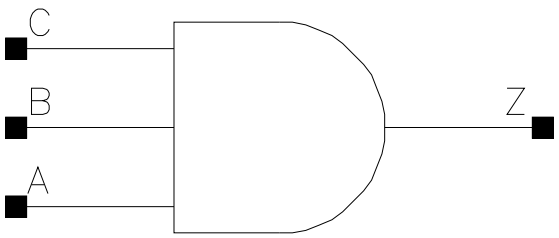
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	6.310e-08	-9.000e-10	-8.100e-09	-2.500e-08
B (output stable)	4.840e-08	-1.080e-08	-6.710e-08	-1.099e-07
A to Z	-2.174e-07	-4.609e-07	-5.168e-07	-5.740e-08
B to Z	-1.759e-07	-1.042e-07	-1.748e-07	-4.694e-07
	X42_P10			
A (output stable)	-2.420e-08			
B (output stable)	-8.380e-08			
A to Z	-9.455e-07			
B to Z	-7.663e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X25_P10	1.200	1.360	1.6320
X33_P10	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0007	0.0011	0.0018	0.0022
B	0.0006	0.0011	0.0016	0.0020
C	0.0007	0.0011	0.0015	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0444	0.0376	2.0362	0.9948
A to Z ↑	0.0401	0.0368	3.8879	1.8523
B to Z ↓	0.0430	0.0361	2.0365	0.9938
B to Z ↑	0.0404	0.0373	3.8886	1.8530
C to Z ↓	0.0412	0.0343	2.0344	0.9939
C to Z ↑	0.0413	0.0373	3.8932	1.8521
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0378	0.0362	0.6868	0.5121

A to Z ↑	0.0365	0.0351	1.2656	0.9485
B to Z ↓	0.0364	0.0347	0.6858	0.5121
B to Z ↑	0.0371	0.0357	1.2645	0.9481
C to Z ↓	0.0346	0.0330	0.6851	0.5119
C to Z ↑	0.0373	0.0359	1.2653	0.9485

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	9.204e-08	2.024e-12
X17_P10	1.808e-07	2.276e-12
X25_P10	2.667e-07	3.284e-12
X33_P10	3.556e-07	3.537e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	4.853e-06	8.665e-06	1.064e-05	1.424e-05
B (output stable)	2.533e-05	4.821e-05	7.048e-05	9.396e-05
C (output stable)	1.639e-05	3.063e-05	4.576e-05	6.138e-05
A to Z	2.608e-03	4.452e-03	6.526e-03	8.355e-03
B to Z	2.463e-03	4.207e-03	6.149e-03	7.847e-03
C to Z	2.340e-03	3.932e-03	5.745e-03	7.306e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

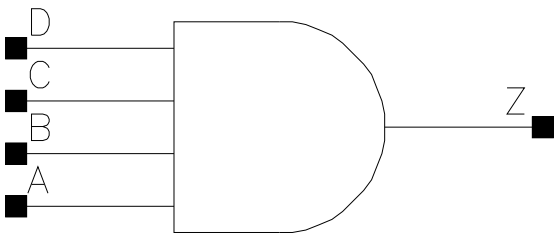
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	5.894e-08	4.317e-09	-1.543e-08	-7.597e-08
B (output stable)	5.662e-08	3.243e-09	-2.343e-08	-8.663e-08
C (output stable)	5.183e-08	-1.000e-08	-5.820e-08	-1.039e-07
A to Z	-1.822e-07	-3.180e-08	-5.592e-07	-9.977e-07
B to Z	-1.919e-07	-4.006e-07	-5.280e-08	-3.387e-07
C to Z	-1.009e-07	-3.560e-07	-5.937e-07	-5.303e-07

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X6_P10	1.200	1.088	1.3056
X20_P10	1.200	2.312	2.7744
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P10	X6_P10	X20_P10	X27_P10
A	0.0006	0.0008	0.0018	0.0021
B	0.0005	0.0008	0.0018	0.0021
C	0.0005	0.0008	0.0018	0.0021
D	0.0005	0.0008	0.0018	0.0021

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X6_P10	X4_P10	X6_P10
A to Z ↓	0.0471	0.0399	3.7672	2.4524
A to Z ↑	0.0444	0.0343	14.6705	7.8725
B to Z ↓	0.0457	0.0376	3.7703	2.4516
B to Z ↑	0.0459	0.0350	14.6758	7.8753
C to Z ↓	0.0485	0.0424	3.7433	2.4741
C to Z ↑	0.0428	0.0328	14.6878	7.8896

D to Z ↓	0.0472	0.0396	3.7414	2.4716
D to Z ↑	0.0451	0.0337	14.6987	7.8951
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0385	0.0364	0.7195	0.5094
A to Z ↑	0.0349	0.0389	2.6244	1.9908
B to Z ↓	0.0354	0.0340	0.7187	0.5089
B to Z ↑	0.0348	0.0391	2.6251	1.9909
C to Z ↓	0.0379	0.0353	0.7271	0.5123
C to Z ↑	0.0305	0.0327	2.6261	1.9920
D to Z ↓	0.0346	0.0328	0.7255	0.5126
D to Z ↑	0.0304	0.0330	2.6282	1.9929

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	9.139e-08	2.780e-12
X6_P10	1.596e-07	2.780e-12
X20_P10	4.742e-07	5.050e-12
X27_P10	5.880e-07	5.555e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	4.507e-04	6.884e-04	2.022e-03	2.540e-03
B (output stable)	4.128e-04	6.033e-04	1.687e-03	2.182e-03
C (output stable)	4.227e-04	6.813e-04	1.719e-03	2.122e-03
D (output stable)	3.896e-04	5.973e-04	1.435e-03	1.761e-03
A to Z	1.791e-03	2.741e-03	8.106e-03	1.053e-02
B to Z	1.698e-03	2.551e-03	7.350e-03	9.762e-03
C to Z	1.731e-03	2.723e-03	6.831e-03	8.457e-03
D to Z	1.641e-03	2.521e-03	6.059e-03	7.652e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

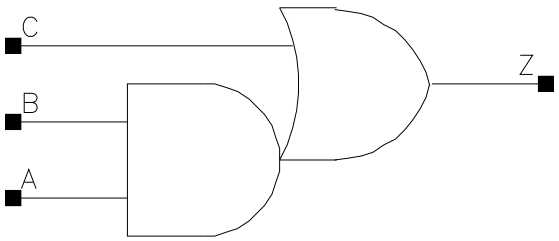
Pin Cycle (vdds)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	-5.348e-06	-9.674e-06	-3.216e-05	-5.673e-05
B (output stable)	-4.571e-06	-7.132e-06	-2.331e-05	-4.176e-05
C (output stable)	5.589e-06	1.019e-05	3.583e-05	6.383e-05
D (output stable)	7.353e-08	1.714e-07	-1.246e-06	-1.456e-06
A to Z	-2.041e-06	-3.860e-06	-1.281e-05	-1.969e-05
B to Z	-1.972e-06	-3.719e-06	-1.169e-05	-2.029e-05
C to Z	-2.000e-07	-4.349e-07	-4.097e-07	-5.105e-07
D to Z	-1.918e-07	-1.227e-07	-1.231e-06	-1.011e-06

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0010	0.0021
B	0.0007	0.0011	0.0019
C	0.0007	0.0011	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0540	0.0485	2.0830	1.0190
A to Z ↑	0.0321	0.0287	3.7563	1.8387
B to Z ↓	0.0501	0.0450	2.0771	1.0174
B to Z ↑	0.0337	0.0304	3.7558	1.8404
C to Z ↓	0.0537	0.0486	2.0706	1.0149
C to Z ↑	0.0288	0.0271	3.7357	1.8317
	X33_P10		**X33_P10**	
A to Z ↓	0.0482		0.5183	
A to Z ↑	0.0291		0.9273	

B to Z ↓	0.0447		0.5181	
B to Z ↑	0.0301		0.9274	
C to Z ↓	0.0482		0.5162	
C to Z ↑	0.0265		0.9227	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.031e-07	2.024e-12
X17_P10	1.920e-07	2.276e-12
X33_P10	3.848e-07	3.787e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	4.897e-06	8.268e-06	2.012e-05
B (output stable)	2.436e-05	3.754e-05	1.297e-04
C (output stable)	2.134e-04	2.680e-04	5.845e-04
A to Z	2.386e-03	4.028e-03	7.894e-03
B to Z	2.245e-03	3.763e-03	7.240e-03
C to Z	2.683e-03	4.568e-03	8.905e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

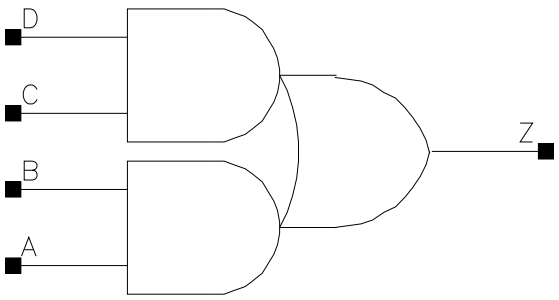
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	2.096e-06	4.399e-06	5.895e-06
B (output stable)	1.532e-05	2.517e-05	4.782e-05
C (output stable)	-4.283e-05	-5.098e-05	-9.773e-05
A to Z	-3.290e-07	-3.962e-07	-1.901e-07
B to Z	-2.060e-07	-4.208e-07	-1.158e-06
C to Z	-1.002e-05	-1.643e-05	-3.040e-05

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0010	0.0020
B	0.0007	0.0010	0.0018
C	0.0006	0.0009	0.0020
D	0.0007	0.0010	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0621	0.0547	2.0061	1.0104
A to Z ↑	0.0395	0.0360	3.6984	1.8380
B to Z ↓	0.0580	0.0513	2.0010	1.0084
B to Z ↑	0.0406	0.0375	3.6978	1.8387

C to Z ↓	0.0553	0.0495	1.9996	1.0081
C to Z ↑	0.0346	0.0316	3.6918	1.8346
D to Z ↓	0.0528	0.0470	1.9956	1.0061
D to Z ↑	0.0367	0.0332	3.6924	1.8346
	X33_P10		**X33_P10**	
A to Z ↓	0.0518		0.5182	
A to Z ↑	0.0328		0.9311	
B to Z ↓	0.0492		0.5182	
B to Z ↑	0.0346		0.9305	
C to Z ↓	0.0469		0.5171	
C to Z ↑	0.0294		0.9286	
D to Z ↓	0.0442		0.5169	
D to Z ↑	0.0307		0.9285	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.238e-07	2.527e-12
X17_P10	2.318e-07	2.780e-12
X33_P10	4.453e-07	4.292e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.668e-05	4.629e-05	5.474e-05
B (output stable)	4.645e-05	6.027e-05	6.058e-05
C (output stable)	6.459e-06	1.239e-05	2.205e-05
D (output stable)	2.578e-05	4.824e-05	9.724e-05
A to Z	3.157e-03	5.243e-03	9.673e-03
B to Z	2.935e-03	4.924e-03	9.162e-03
C to Z	2.646e-03	4.426e-03	8.031e-03
D to Z	2.520e-03	4.174e-03	7.486e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

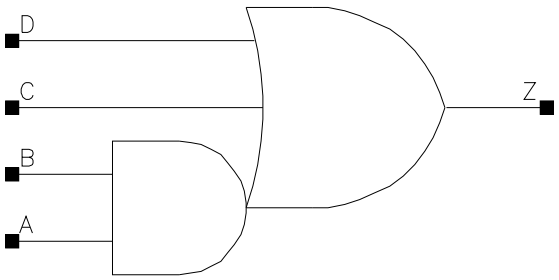
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	2.220e-07	-1.430e-06	-3.697e-06
B (output stable)	-9.913e-07	-1.432e-06	-3.257e-06
C (output stable)	8.062e-08	1.104e-07	2.048e-07
D (output stable)	8.164e-07	1.448e-06	2.142e-06
A to Z	-3.972e-06	-8.428e-06	-1.806e-05
B to Z	-6.715e-06	-1.247e-05	-2.915e-05
C to Z	-2.275e-07	-2.228e-07	-3.805e-07
D to Z	-1.214e-07	-3.899e-07	-8.824e-07

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	0.952	1.1424
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0010	0.0018
B	0.0007	0.0010	0.0019
C	0.0007	0.0010	0.0019
D	0.0006	0.0010	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0718	0.0623	2.2063	1.0871
A to Z ↑	0.0343	0.0309	3.7381	1.9072
B to Z ↓	0.0684	0.0579	2.2008	1.0850
B to Z ↑	0.0361	0.0320	3.7401	1.9078
C to Z ↓	0.0768	0.0671	2.1964	1.0830
C to Z ↑	0.0309	0.0286	3.7199	1.8981

D to Z ↓	0.0753	0.0665	2.1974	1.0834
D to Z ↑	0.0306	0.0285	3.7163	1.8974
	X33_P10		**X33_P10**	
A to Z ↓	0.0629		0.5440	
A to Z ↑	0.0307		0.9289	
B to Z ↓	0.0564		0.5418	
B to Z ↑	0.0313		0.9284	
C to Z ↓	0.0678		0.5415	
C to Z ↑	0.0279		0.9246	
D to Z ↓	0.0660		0.5416	
D to Z ↑	0.0272		0.9233	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.128e-07	2.275e-12
X17_P10	2.100e-07	2.528e-12
X33_P10	4.274e-07	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.255e-06	3.557e-06	1.440e-05
B (output stable)	7.637e-06	1.392e-05	6.412e-05
C (output stable)	1.343e-04	2.517e-04	6.756e-04
D (output stable)	4.153e-06	6.695e-06	1.571e-05
A to Z	2.584e-03	4.227e-03	8.383e-03
B to Z	2.463e-03	3.956e-03	7.583e-03
C to Z	3.041e-03	5.056e-03	1.013e-02
D to Z	2.847e-03	4.726e-03	9.245e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

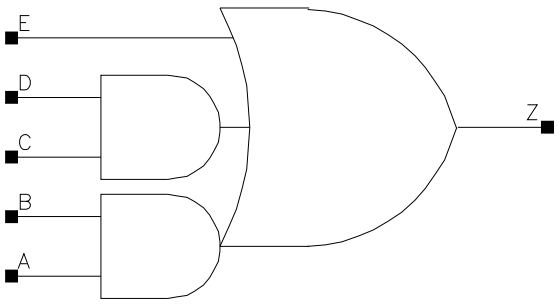
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	1.508e-06	2.276e-06	4.475e-06
B (output stable)	6.500e-06	1.089e-05	2.170e-05
C (output stable)	-2.481e-05	-4.605e-05	-1.183e-04
D (output stable)	4.496e-06	9.670e-06	3.118e-05
A to Z	-9.630e-08	-5.422e-07	-1.633e-06
B to Z	-2.822e-07	-6.350e-07	-1.253e-06
C to Z	-9.269e-06	-1.656e-05	-3.579e-05
D to Z	-6.458e-06	-1.129e-05	-1.987e-05

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.088	1.3056
X17_P10	1.200	1.224	1.4688
X33_P10	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0010	0.0020
B	0.0007	0.0010	0.0018
C	0.0008	0.0012	0.0019
D	0.0007	0.0010	0.0019
E	0.0006	0.0010	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0888	0.0766	2.1058	1.0523
A to Z ↑	0.0411	0.0357	3.6671	1.8478

B to Z ↓	0.0855	0.0728	2.1006	1.0508
B to Z ↑	0.0437	0.0377	3.6661	1.8480
C to Z ↓	0.0743	0.0650	2.0931	1.0479
C to Z ↑	0.0361	0.0311	3.6405	1.8388
D to Z ↓	0.0692	0.0592	2.0858	1.0436
D to Z ↑	0.0379	0.0325	3.6411	1.8398
E to Z ↓	0.0780	0.0673	2.0819	1.0430
E to Z ↑	0.0322	0.0284	3.6181	1.8286
	X33_P10		**X33_P10**	
A to Z ↓	0.0746		0.5436	
A to Z ↑	0.0363		0.9333	
B to Z ↓	0.0702		0.5428	
B to Z ↑	0.0381		0.9335	
C to Z ↓	0.0624		0.5413	
C to Z ↑	0.0310		0.9277	
D to Z ↓	0.0571		0.5397	
D to Z ↑	0.0322		0.9282	
E to Z ↓	0.0653		0.5391	
E to Z ↑	0.0282		0.9220	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.388e-07	2.779e-12
X17_P10	2.558e-07	3.033e-12
X33_P10	4.894e-07	5.049e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.248e-05	3.004e-05	6.402e-05
B (output stable)	6.289e-05	9.268e-05	2.087e-04
C (output stable)	1.064e-05	1.257e-05	3.378e-05
D (output stable)	6.790e-06	1.283e-05	3.096e-05
E (output stable)	9.744e-05	1.309e-04	3.104e-04
A to Z	3.585e-03	5.713e-03	1.111e-02
B to Z	3.491e-03	5.471e-03	1.049e-02
C to Z	2.781e-03	4.436e-03	8.504e-03
D to Z	2.637e-03	4.141e-03	7.845e-03
E to Z	3.107e-03	4.935e-03	9.461e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-1.427e-06	-4.070e-06	-8.407e-06
B (output stable)	-1.050e-05	-1.627e-05	-3.352e-05
C (output stable)	6.208e-06	1.021e-05	2.186e-05
D (output stable)	6.583e-07	1.313e-06	6.388e-07
E (output stable)	-2.935e-06	-5.070e-06	-1.746e-05
A to Z	-1.021e-05	-1.611e-05	-3.271e-05
B to Z	-1.282e-05	-2.066e-05	-4.474e-05
C to Z	-2.721e-07	-3.794e-07	-1.050e-06
D to Z	-3.319e-07	-4.534e-07	-1.005e-06

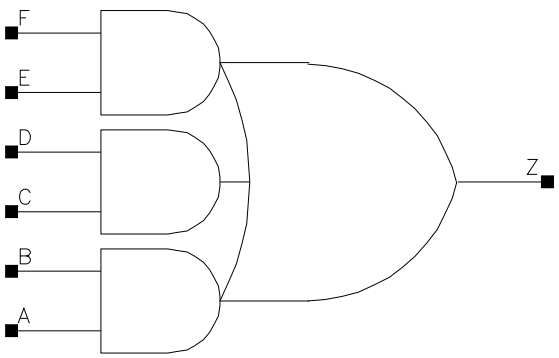
E to Z	-6.573e-06	-1.084e-05	-2.237e-05

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.360	1.6320
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
A	0.0006	0.0007	0.0009	0.0020

B	0.0007	0.0008	0.0013	0.0018
C	0.0006	0.0007	0.0009	0.0019
D	0.0006	0.0007	0.0009	0.0018
E	0.0007	0.0008	0.0010	0.0020
F	0.0007	0.0008	0.0010	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
A to Z ↓	0.0881	0.0835	3.9573	2.0891
A to Z ↑	0.0432	0.0416	7.3094	3.7363
B to Z ↓	0.0813	0.0775	3.9419	2.0804
B to Z ↑	0.0441	0.0429	7.3049	3.7350
C to Z ↓	0.0806	0.0769	3.9450	2.0842
C to Z ↑	0.0398	0.0383	7.2681	3.7171
D to Z ↓	0.0768	0.0733	3.9352	2.0779
D to Z ↑	0.0420	0.0406	7.2642	3.7156
E to Z ↓	0.0664	0.0646	3.9245	2.0742
E to Z ↑	0.0348	0.0336	7.2357	3.7018
F to Z ↓	0.0618	0.0603	3.9133	2.0674
F to Z ↑	0.0363	0.0352	7.2391	3.7031
	X17_P10	X33_P10	X17_P10	X33_P10
A to Z ↓	0.0806	0.0768	1.0542	0.5413
A to Z ↑	0.0386	0.0386	1.8530	0.9364
B to Z ↓	0.0759	0.0726	1.0492	0.5407
B to Z ↑	0.0406	0.0404	1.8532	0.9362
C to Z ↓	0.0750	0.0720	1.0520	0.5407
C to Z ↑	0.0357	0.0365	1.8440	0.9316
D to Z ↓	0.0710	0.0681	1.0484	0.5400
D to Z ↑	0.0378	0.0381	1.8440	0.9318
E to Z ↓	0.0628	0.0631	1.0462	0.5386
E to Z ↑	0.0312	0.0324	1.8384	0.9297
F to Z ↓	0.0587	0.0583	1.0430	0.5373
F to Z ↑	0.0328	0.0340	1.8384	0.9294

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	1.333e-07	3.283e-12
X8_P10	1.832e-07	3.286e-12
X17_P10	2.901e-07	3.538e-12
X33_P10	5.461e-07	5.554e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	5.674e-05	6.968e-05	8.705e-05	1.743e-04
B (output stable)	2.032e-04	2.460e-04	3.126e-04	5.896e-04
C (output stable)	2.622e-05	3.287e-05	4.665e-05	8.007e-05
D (output stable)	3.726e-05	4.697e-05	5.947e-05	1.201e-04
E (output stable)	2.644e-05	2.854e-05	3.253e-05	4.456e-05
F (output stable)	2.505e-05	2.848e-05	3.745e-05	7.796e-05

A to Z	3.353e-03	4.326e-03	6.376e-03	1.202e-02
B to Z	3.108e-03	4.039e-03	6.004e-03	1.135e-02
C to Z	2.854e-03	3.729e-03	5.577e-03	1.054e-02
D to Z	2.725e-03	3.566e-03	5.311e-03	9.907e-03
E to Z	2.278e-03	3.082e-03	4.610e-03	9.008e-03
F to Z	2.137e-03	2.901e-03	4.343e-03	8.395e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

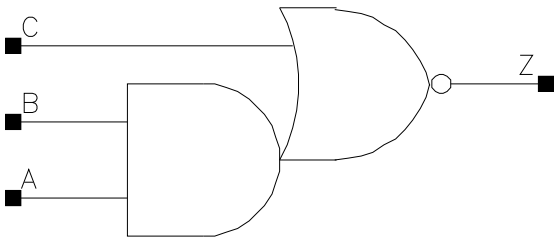
Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	-6.296e-06	-8.002e-06	-1.144e-05	-2.266e-05
B (output stable)	-2.447e-05	-3.043e-05	-4.348e-05	-8.293e-05
C (output stable)	-2.812e-06	-3.414e-06	-4.504e-06	-4.692e-06
D (output stable)	-1.114e-06	-1.359e-06	-1.522e-06	5.356e-06
E (output stable)	1.562e-05	1.932e-05	2.718e-05	4.409e-05
F (output stable)	1.085e-05	1.340e-05	1.898e-05	3.565e-05
A to Z	-1.232e-05	-1.526e-05	-2.137e-05	-3.784e-05
B to Z	-1.232e-05	-1.521e-05	-2.118e-05	-3.991e-05
C to Z	-8.740e-06	-1.068e-05	-1.495e-05	-2.220e-05
D to Z	-7.531e-06	-9.248e-06	-1.241e-05	-1.755e-05
E to Z	-2.008e-07	-4.432e-07	-6.335e-07	-1.226e-06
F to Z	-3.065e-07	-3.769e-07	-5.807e-07	-1.165e-06

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008
X44_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X33_P10	X44_P10
A	0.0008	0.0024	0.0048	0.0064
B	0.0008	0.0022	0.0044	0.0060
C	0.0009	0.0026	0.0050	0.0065

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0131	0.0136	3.6803	1.2552
A to Z ↑	0.0252	0.0256	8.0237	2.6732
B to Z ↓	0.0126	0.0128	3.7222	1.2745
B to Z ↑	0.0209	0.0206	7.9263	2.6809
C to Z ↓	0.0129	0.0131	2.0550	0.7088
C to Z ↑	0.0269	0.0268	7.3410	2.4687
	X33_P10	**X44_P10**	**X33_P10**	**X44_P10**
A to Z ↓	0.0139	0.0138	0.6384	0.4843

A to Z ↑	0.0256	0.0256	1.3377	1.0139
B to Z ↓	0.0127	0.0126	0.6487	0.4921
B to Z ↑	0.0204	0.0203	1.3394	1.0127
C to Z ↓	0.0144	0.0146	0.4218	0.3288
C to Z ↑	0.0270	0.0270	1.2329	0.9332

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P10	1.007e-07	1.772e-12
X17_P10	2.955e-07	3.286e-12
X33_P10	5.626e-07	5.551e-12
X44_P10	7.427e-07	7.065e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	8.390e-06	3.017e-05	6.418e-05	8.600e-05
B (output stable)	3.940e-05	1.802e-04	3.953e-04	5.105e-04
C (output stable)	2.666e-04	8.089e-04	1.689e-03	2.268e-03
A to Z	1.087e-03	3.428e-03	6.882e-03	9.128e-03
B to Z	8.197e-04	2.338e-03	4.675e-03	6.151e-03
C to Z	1.602e-03	4.754e-03	9.604e-03	1.272e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

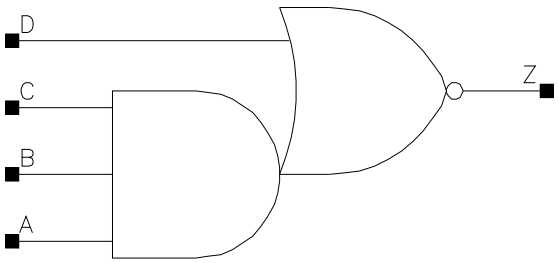
Pin Cycle (vdds)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	3.191e-06	9.605e-06	1.911e-05	2.538e-05
B (output stable)	2.275e-05	5.261e-05	1.069e-04	1.370e-04
C (output stable)	-4.741e-05	-1.153e-04	-2.345e-04	-3.038e-04
A to Z	-1.180e-08	-2.560e-07	-3.780e-07	-5.500e-08
B to Z	1.229e-07	3.700e-07	-2.604e-06	-2.175e-06
C to Z	-1.433e-05	-3.851e-05	-7.644e-05	-1.003e-04

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X29_P10	1.200	3.536	4.2432
X38_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X29_P10	X38_P10
A	0.0009	0.0049	0.0063
B	0.0008	0.0047	0.0061
C	0.0008	0.0044	0.0058
D	0.0009	0.0050	0.0062

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X29_P10	X5_P10	X29_P10
A to Z ↓	0.0183	0.0196	5.3343	0.9268
A to Z ↑	0.0317	0.0318	8.0174	1.3254
B to Z ↓	0.0183	0.0189	5.3490	0.9303
B to Z ↑	0.0284	0.0282	8.0123	1.3343
C to Z ↓	0.0174	0.0172	5.3785	0.9368
C to Z ↑	0.0244	0.0235	7.9343	1.3466
D to Z ↓	0.0151	0.0168	2.0994	0.4247

D to Z ↑	0.0304	0.0306	6.8507	1.1455
	X38_P10		**X38_P10**	
A to Z ↓	0.0190		0.7162	
A to Z ↑	0.0308		0.9986	
B to Z ↓	0.0185		0.7195	
B to Z ↑	0.0273		1.0079	
C to Z ↓	0.0166		0.7248	
C to Z ↑	0.0225		1.0206	
D to Z ↓	0.0173		0.3522	
D to Z ↑	0.0298		0.8645	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P10	1.181e-07	2.027e-12
X29_P10	6.691e-07	7.317e-12
X38_P10	8.686e-07	9.333e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P10	X29_P10	X38_P10
A (output stable)	8.162e-06	7.502e-05	9.442e-05
B (output stable)	1.961e-05	1.279e-04	1.680e-04
C (output stable)	3.622e-05	4.090e-04	5.345e-04
D (output stable)	5.300e-04	3.762e-03	4.899e-03
A to Z	1.681e-03	1.060e-02	1.314e-02
B to Z	1.427e-03	8.547e-03	1.063e-02
C to Z	1.156e-03	6.333e-03	7.620e-03
D to Z	2.105e-03	1.272e-02	1.612e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

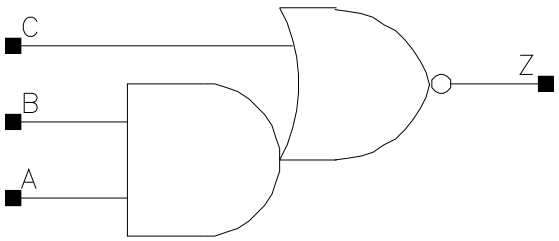
Pin Cycle (vdds)	X5_P10	X29_P10	X38_P10
A (output stable)	1.125e-05	7.743e-05	1.010e-04
B (output stable)	1.458e-06	9.766e-06	1.426e-05
C (output stable)	1.167e-06	5.796e-06	7.117e-06
D (output stable)	-7.399e-05	-5.509e-04	-7.179e-04
A to Z	7.700e-08	-1.990e-07	-2.640e-07
B to Z	1.690e-07	-3.413e-06	-4.749e-06
C to Z	-2.040e-07	-4.000e-09	-1.110e-07
D to Z	-1.158e-05	-8.315e-05	-1.104e-04

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X11_P10	1.200	1.088	1.3056
X16_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X11_P10	X16_P10	X23_P10
A	0.0009	0.0018	0.0026	0.0035
B	0.0009	0.0017	0.0025	0.0032
C	0.0009	0.0016	0.0023	0.0032
	X46_P10			
A	0.0066			
B	0.0063			
C	0.0063			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X11_P10	X6_P10	X11_P10
A to Z ↓	0.0148	0.0160	3.5511	1.8084
A to Z ↑	0.0291	0.0305	8.0087	3.9059
B to Z ↓	0.0153	0.0156	3.5880	1.8301

B to Z ↑	0.0258	0.0264	7.9172	3.9211
C to Z ↓	0.0096	0.0099	2.1170	1.2465
C to Z ↑	0.0207	0.0202	7.3040	3.5925
	X16_P10	**X23_P10**	**X16_P10**	**X23_P10**
A to Z ↓	0.0154	0.0157	1.2536	0.9423
A to Z ↑	0.0288	0.0293	2.6259	1.9870
B to Z ↓	0.0155	0.0154	1.2699	0.9538
B to Z ↑	0.0247	0.0251	2.6284	1.9977
C to Z ↓	0.0101	0.0091	0.8702	0.5467
C to Z ↑	0.0197	0.0199	2.4129	1.8290
	X46_P10		**X46_P10**	
A to Z ↓	0.0153		0.4850	
A to Z ↑	0.0285		1.0272	
B to Z ↓	0.0150		0.4911	
B to Z ↑	0.0242		1.0260	
C to Z ↓	0.0092		0.2809	
C to Z ↑	0.0196		0.9442	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P10	1.063e-07	1.772e-12
X11_P10	2.098e-07	2.779e-12
X16_P10	2.990e-07	3.284e-12
X23_P10	4.233e-07	4.292e-12
X46_P10	8.296e-07	7.315e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	2.636e-05	6.354e-05	8.940e-05	1.216e-04
B (output stable)	1.738e-04	4.765e-04	5.498e-04	7.652e-04
C (output stable)	3.962e-05	1.051e-04	1.279e-04	2.159e-04
A to Z	1.646e-03	3.644e-03	4.920e-03	6.743e-03
B to Z	1.377e-03	2.889e-03	3.856e-03	5.235e-03
C to Z	7.793e-04	1.574e-03	2.178e-03	2.967e-03
	X46_P10			
A (output stable)	2.328e-04			
B (output stable)	1.357e-03			
C (output stable)	3.127e-04			
A to Z	1.244e-02			
B to Z	9.608e-03			
C to Z	5.397e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	-2.598e-06	-6.329e-06	-6.822e-06	-8.101e-06
B (output stable)	-2.887e-05	-7.480e-05	-6.728e-05	-9.420e-05
C (output stable)	5.843e-05	1.526e-04	1.353e-04	1.886e-04
A to Z	-8.539e-06	-1.899e-05	-1.761e-05	-2.462e-05
B to Z	-7.681e-06	-1.893e-05	-1.887e-05	-2.343e-05
C to Z	3.083e-07	2.166e-07	5.117e-07	-1.232e-07

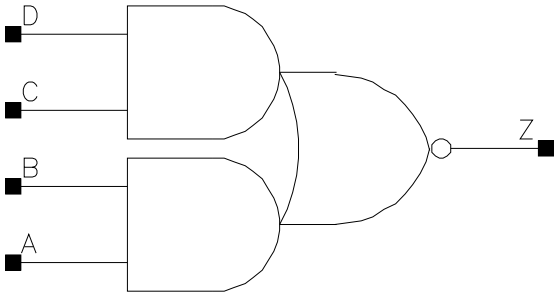
	X46_P10			
A (output stable)	-1.782e-05			
B (output stable)	-1.723e-04			
C (output stable)	3.474e-04			
A to Z	-4.968e-05			
B to Z	-5.148e-05			
C to Z	-8.987e-07			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P10	X10_P10	X16_P10	X21_P10
A	0.0007	0.0018	0.0026	0.0034
B	0.0007	0.0016	0.0024	0.0032
C	0.0007	0.0017	0.0024	0.0032
D	0.0007	0.0015	0.0023	0.0030
	X42_P10			
A	0.0068			
B	0.0064			
C	0.0064			
D	0.0060			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X10_P10**	**X4_P10**	**X10_P10**
A to Z ↓	0.0165	0.0161	4.4203	1.7389
A to Z ↑	0.0361	0.0313	10.9806	3.6113
B to Z ↓	0.0172	0.0171	4.4672	1.7592
B to Z ↑	0.0326	0.0287	10.9577	3.6908
C to Z ↓	0.0134	0.0127	4.5222	1.7461
C to Z ↑	0.0286	0.0252	10.8594	3.5916
D to Z ↓	0.0133	0.0126	4.5839	1.7746
D to Z ↑	0.0246	0.0217	10.8331	3.6412
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0175	0.0174	1.2616	0.9472
A to Z ↑	0.0326	0.0324	2.4319	1.8760
B to Z ↓	0.0179	0.0174	1.2754	0.9579
B to Z ↑	0.0289	0.0285	2.4326	1.8786
C to Z ↓	0.0136	0.0139	1.2588	0.9455
C to Z ↑	0.0258	0.0263	2.4055	1.8530
D to Z ↓	0.0129	0.0125	1.2796	0.9625
D to Z ↑	0.0214	0.0216	2.4119	1.8586
	X42_P10		**X42_P10**	
A to Z ↓	0.0182		0.4929	
A to Z ↑	0.0329		0.9401	
B to Z ↓	0.0180		0.4982	
B to Z ↑	0.0288		0.9373	
C to Z ↓	0.0144		0.4860	
C to Z ↑	0.0266		0.9312	
D to Z ↓	0.0132		0.4940	
D to Z ↑	0.0219		0.9297	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	9.981e-08	2.024e-12
X10_P10	2.630e-07	3.283e-12
X16_P10	3.806e-07	4.039e-12
X21_P10	5.110e-07	5.297e-12
X42_P10	1.008e-06	8.765e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	1.919e-05	4.928e-05	9.423e-05	1.300e-04
B (output stable)	2.299e-05	6.320e-05	1.311e-04	1.880e-04
C (output stable)	9.195e-06	2.370e-05	5.894e-05	8.827e-05
D (output stable)	3.616e-05	9.218e-05	2.551e-04	3.940e-04
A to Z	1.692e-03	4.079e-03	6.492e-03	8.379e-03
B to Z	1.479e-03	3.569e-03	5.469e-03	6.972e-03
C to Z	9.853e-04	2.400e-03	3.761e-03	5.080e-03
D to Z	7.721e-04	1.860e-03	2.674e-03	3.551e-03
	X42_P10			
A (output stable)	2.471e-04			
B (output stable)	3.520e-04			
C (output stable)	1.653e-04			
D (output stable)	7.146e-04			

A to Z	1.665e-02			
B to Z	1.393e-02			
C to Z	9.984e-03			
D to Z	7.057e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

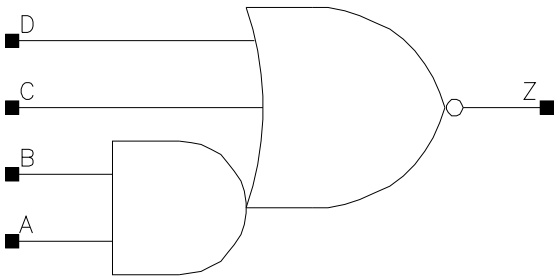
Pin Cycle (vdds)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	-1.486e-06	-3.369e-06	-5.068e-06	-5.969e-06
B (output stable)	-1.189e-06	-3.230e-06	-5.116e-06	-7.496e-06
C (output stable)	1.354e-07	2.074e-07	3.192e-07	3.037e-06
D (output stable)	7.484e-07	2.302e-06	3.454e-06	3.339e-06
A to Z	-9.111e-06	-1.980e-05	-2.776e-05	-3.421e-05
B to Z	-1.395e-05	-2.953e-05	-4.530e-05	-5.628e-05
C to Z	-1.403e-07	-4.835e-07	-4.527e-07	-2.097e-07
D to Z	4.597e-08	-1.960e-07	-2.993e-07	-1.098e-06
	X42_P10			
A (output stable)	-1.049e-05			
B (output stable)	-1.384e-05			
C (output stable)	4.636e-06			
D (output stable)	8.306e-06			
A to Z	-6.229e-05			
B to Z	-1.074e-04			
C to Z	-7.347e-07			
D to Z	-2.380e-06			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X35_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P10	X35_P10
A	0.0008	0.0062
B	0.0008	0.0057
C	0.0009	0.0061
D	0.0009	0.0056

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X35_P10	X5_P10	X35_P10
A to Z ↓	0.0147	0.0154	3.7209	0.5496
A to Z ↑	0.0328	0.0312	12.1964	1.5509
B to Z ↓	0.0147	0.0148	3.7732	0.5589
B to Z ↑	0.0275	0.0251	12.1276	1.5505
C to Z ↓	0.0152	0.0188	2.1981	0.4223
C to Z ↑	0.0388	0.0380	11.5327	1.4674
D to Z ↓	0.0147	0.0175	2.2161	0.4213

D to Z ↑	0.0376	0.0357	11.5418	1.4696

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P10	1.201e-07	2.027e-12
X35_P10	7.760e-07	9.331e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P10	X35_P10
A (output stable)	3.702e-06	4.568e-05
B (output stable)	1.378e-05	1.677e-04
C (output stable)	2.435e-04	2.400e-03
D (output stable)	5.837e-06	8.574e-05
A to Z	1.333e-03	9.722e-03
B to Z	1.067e-03	7.081e-03
C to Z	2.174e-03	1.684e-02
D to Z	1.828e-03	1.329e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

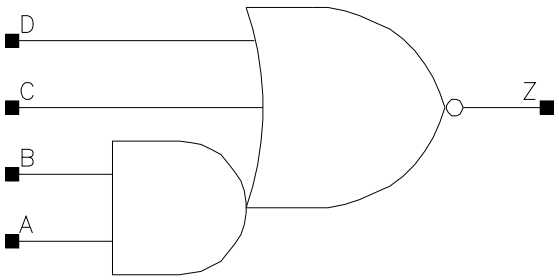
Pin Cycle (vdds)	X5_P10	X35_P10
A (output stable)	2.674e-06	2.167e-05
B (output stable)	1.050e-05	6.413e-05
C (output stable)	-4.414e-05	-3.377e-04
D (output stable)	9.280e-06	7.796e-05
A to Z	-2.683e-07	-1.898e-06
B to Z	-2.954e-07	-9.390e-07
C to Z	-1.506e-05	-9.921e-05
D to Z	-1.072e-05	-6.480e-05

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X17_P10	1.200	2.448	2.9376
X34_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P10	X17_P10	X34_P10
A	0.0008	0.0034	0.0068
B	0.0008	0.0032	0.0065
C	0.0007	0.0029	0.0058
D	0.0007	0.0027	0.0053

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X17_P10	X4_P10	X17_P10
A to Z ↓	0.0168	0.0181	4.0332	1.0712
A to Z ↑	0.0389	0.0408	12.2483	3.0148
B to Z ↓	0.0180	0.0184	4.0749	1.0818
B to Z ↑	0.0347	0.0354	12.1507	3.0177
C to Z ↓	0.0159	0.0156	3.5042	0.8552
C to Z ↑	0.0297	0.0312	11.4977	2.8453

D to Z ↓	0.0135	0.0124	3.5857	0.8605
D to Z ↑	0.0255	0.0236	11.5486	2.8586
	X34_P10		**X34_P10**	
A to Z ↓	0.0179		0.5498	
A to Z ↑	0.0402		1.5319	
B to Z ↓	0.0185		0.5552	
B to Z ↑	0.0349		1.5269	
C to Z ↓	0.0158		0.4525	
C to Z ↑	0.0305		1.4440	
D to Z ↓	0.0125		0.4573	
D to Z ↑	0.0232		1.4499	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	1.072e-07	2.024e-12
X17_P10	4.277e-07	5.306e-12
X34_P10	8.278e-07	9.339e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P10	X17_P10	X34_P10
A (output stable)	2.728e-05	1.206e-04	2.446e-04
B (output stable)	8.465e-05	3.983e-04	7.736e-04
C (output stable)	8.724e-05	6.101e-04	1.157e-03
D (output stable)	1.673e-06	7.148e-05	1.230e-04
A to Z	2.070e-03	8.951e-03	1.733e-02
B to Z	1.838e-03	7.592e-03	1.475e-02
C to Z	1.256e-03	5.414e-03	1.032e-02
D to Z	8.532e-04	3.149e-03	5.972e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

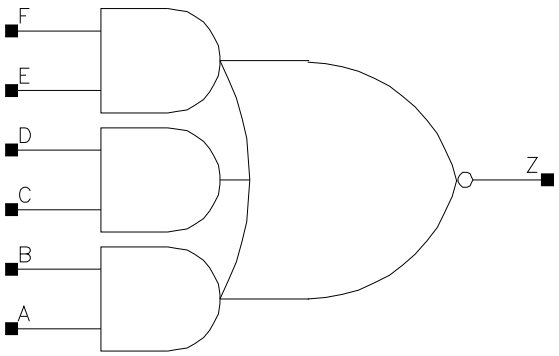
Pin Cycle (vdds)	X4_P10	X17_P10	X34_P10
A (output stable)	-3.995e-06	-1.136e-05	-2.309e-05
B (output stable)	-1.531e-05	-4.714e-05	-9.352e-05
C (output stable)	-1.267e-06	-6.118e-05	-9.836e-05
D (output stable)	1.015e-05	6.860e-05	1.209e-04
A to Z	-1.180e-05	-4.305e-05	-8.532e-05
B to Z	-1.404e-05	-5.433e-05	-1.014e-04
C to Z	-4.739e-06	-2.670e-05	-4.862e-05
D to Z	-4.477e-07	-5.493e-07	-1.145e-06

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X8_P10	1.200	2.176	2.6112
X13_P10	1.200	2.720	3.2640
X17_P10	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P10	X8_P10	X13_P10	X17_P10
A	0.0009	0.0017	0.0026	0.0034

B	0.0008	0.0016	0.0024	0.0031
C	0.0008	0.0016	0.0024	0.0032
D	0.0008	0.0015	0.0023	0.0030
E	0.0010	0.0016	0.0023	0.0030
F	0.0008	0.0015	0.0022	0.0028

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0189	0.0224	3.5773	2.0741
A to Z ↑	0.0536	0.0528	11.7412	5.4298
B to Z ↓	0.0206	0.0231	3.6090	2.0885
B to Z ↑	0.0493	0.0478	11.7309	5.4402
C to Z ↓	0.0178	0.0207	3.5411	2.0860
C to Z ↑	0.0477	0.0479	11.7715	5.4373
D to Z ↓	0.0190	0.0215	3.5840	2.1060
D to Z ↑	0.0433	0.0430	11.7215	5.4348
E to Z ↓	0.0141	0.0165	3.4722	2.0839
E to Z ↑	0.0357	0.0357	11.6222	5.3804
F to Z ↓	0.0144	0.0163	3.5325	2.1165
F to Z ↑	0.0310	0.0305	11.6926	5.3898
	X13_P10	**X17_P10**	**X13_P10**	**X17_P10**
A to Z ↓	0.0216	0.0217	1.4141	1.0790
A to Z ↑	0.0494	0.0495	3.5912	2.7410
B to Z ↓	0.0228	0.0224	1.4233	1.0865
B to Z ↑	0.0450	0.0445	3.6011	2.7413
C to Z ↓	0.0201	0.0200	1.4239	1.0666
C to Z ↑	0.0445	0.0448	3.6007	2.7516
D to Z ↓	0.0211	0.0203	1.4371	1.0770
D to Z ↑	0.0402	0.0397	3.6064	2.7475
E to Z ↓	0.0161	0.0161	1.4172	1.0670
E to Z ↑	0.0339	0.0339	3.5684	2.7168
F to Z ↓	0.0159	0.0152	1.4379	1.0837
F to Z ↑	0.0290	0.0286	3.5755	2.7280

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	1.844e-07	2.782e-12
X8_P10	3.534e-07	4.798e-12
X13_P10	5.086e-07	5.806e-12
X17_P10	6.794e-07	7.570e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

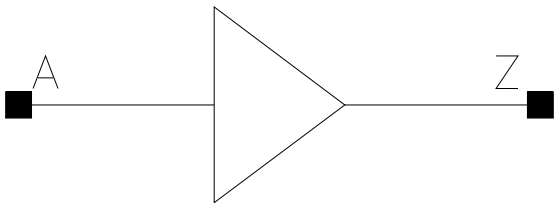
Pin Cycle (vdd)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	8.169e-05	1.871e-04	2.626e-04	3.459e-04
B (output stable)	3.074e-04	6.861e-04	8.934e-04	1.183e-03
C (output stable)	4.262e-05	1.004e-04	1.299e-04	1.763e-04
D (output stable)	5.796e-05	1.549e-04	1.827e-04	2.731e-04
E (output stable)	2.146e-05	6.174e-05	8.300e-05	1.108e-04
F (output stable)	3.046e-05	1.040e-04	1.276e-04	2.064e-04

A to Z	3.265e-03	6.881e-03	9.516e-03	1.255e-02
B to Z	3.004e-03	6.168e-03	8.592e-03	1.116e-02
C to Z	2.483e-03	5.413e-03	7.293e-03	9.646e-03
D to Z	2.204e-03	4.714e-03	6.380e-03	8.235e-03
E to Z	1.538e-03	3.498e-03	4.724e-03	6.233e-03
F to Z	1.280e-03	2.821e-03	3.795e-03	4.851e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	-1.274e-05	-2.864e-05	-3.198e-05	-4.238e-05
B (output stable)	-5.283e-05	-1.093e-04	-1.184e-04	-1.608e-04
C (output stable)	-4.675e-06	-1.163e-05	-1.008e-05	-1.314e-05
D (output stable)	1.839e-06	-2.928e-06	-8.061e-07	-3.707e-06
E (output stable)	2.778e-05	6.505e-05	6.761e-05	9.410e-05
F (output stable)	2.313e-05	4.891e-05	5.267e-05	7.098e-05
A to Z	-2.449e-05	-5.074e-05	-5.367e-05	-7.079e-05
B to Z	-2.690e-05	-5.251e-05	-5.701e-05	-7.645e-05
C to Z	-1.675e-05	-3.558e-05	-3.676e-05	-5.263e-05
D to Z	-1.208e-05	-2.891e-05	-2.914e-05	-4.078e-05
E to Z	-6.909e-07	-1.763e-06	-1.982e-06	-2.227e-06
F to Z	-2.453e-07	-1.263e-06	-1.361e-06	-1.678e-06

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.408	0.4896
X6_P10	1.200	0.408	0.4896
X8_P10	1.200	0.408	0.4896
X13_P10	1.200	0.544	0.6528
X16_P10	1.200	0.544	0.6528
X21_P10	1.200	0.680	0.8160
X25_P10	1.200	0.680	0.8160
X29_P10	1.200	0.952	1.1424
X33_P10	1.200	0.952	1.1424
X42_P10	1.200	1.088	1.3056
X50_P10	1.200	1.224	1.4688
X58_P10	1.200	1.496	1.7952
X67_P10	1.200	1.632	1.9584
X75_P10	1.200	1.768	2.1216
X84_P10	1.200	1.904	2.2848
X100_P10	1.200	2.312	2.7744
X134_P10	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0008	0.0008	0.0008	0.0008
	X16_P10	X21_P10	X25_P10	X29_P10
A	0.0008	0.0011	0.0011	0.0016
	X33_P10	X42_P10	X50_P10	X58_P10
A	0.0015	0.0017	0.0021	0.0031

	X67_P10	X75_P10	X84_P10	X100_P10
A	0.0031	0.0030	0.0030	0.0040
	X134_P10			
A	0.0050			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0332	0.0334	3.6533	2.6719
A to Z ↑	0.0244	0.0242	7.1832	5.2621
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0347	0.0390	1.9838	1.2843
A to Z ↑	0.0250	0.0278	3.7539	2.4504
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0419	0.0353	1.0252	0.7905
A to Z ↑	0.0294	0.0255	1.8798	1.4736
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0370	0.0354	0.6815	0.5754
A to Z ↑	0.0266	0.0249	1.2367	1.0522
	X33_P10	**X42_P10**	**X33_P10**	**X42_P10**
A to Z ↓	0.0367	0.0359	0.5100	0.4143
A to Z ↑	0.0257	0.0259	0.9237	0.7432
	X50_P10	**X58_P10**	**X50_P10**	**X58_P10**
A to Z ↓	0.0351	0.0326	0.3443	0.2973
A to Z ↑	0.0252	0.0237	0.6172	0.5307
	X67_P10	**X75_P10**	**X67_P10**	**X75_P10**
A to Z ↓	0.0344	0.0359	0.2608	0.2361
A to Z ↑	0.0249	0.0260	0.4644	0.4161
	X84_P10	**X100_P10**	**X84_P10**	**X100_P10**
A to Z ↓	0.0375	0.0355	0.2138	0.1799
A to Z ↑	0.0270	0.0258	0.3753	0.3143
	X134_P10		**X134_P10**	
A to Z ↓	0.0367		0.1402	
A to Z ↑	0.0269		0.2402	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	5.541e-08	1.519e-12
X6_P10	6.547e-08	1.520e-12
X8_P10	7.816e-08	1.518e-12
X13_P10	1.038e-07	1.771e-12
X16_P10	1.237e-07	1.771e-12
X21_P10	1.697e-07	2.024e-12
X25_P10	1.890e-07	2.025e-12
X29_P10	2.284e-07	2.527e-12
X33_P10	2.465e-07	2.527e-12
X42_P10	3.038e-07	2.778e-12
X50_P10	3.641e-07	3.031e-12
X58_P10	4.517e-07	3.534e-12
X67_P10	4.956e-07	3.786e-12
X75_P10	5.394e-07	4.035e-12

X84_P10	5.832e-07	4.294e-12
X100_P10	7.147e-07	5.055e-12
X134_P10	9.339e-07	6.299e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	1.644e-03	1.828e-03	2.152e-03	2.821e-03
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	3.356e-03	4.579e-03	5.113e-03	5.714e-03
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	6.237e-03	7.895e-03	9.144e-03	1.107e-02
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	1.246e-02	1.382e-02	1.510e-02	1.833e-02
	X134_P10			
A to Z	2.423e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

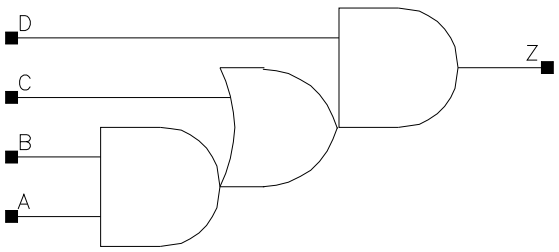
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	-3.847e-07	-5.316e-07	-3.960e-08	-3.216e-07
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	-2.013e-07	-7.188e-07	-7.795e-07	-6.466e-07
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	-3.050e-07	-2.680e-07	-9.523e-07	-1.687e-06
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	-1.039e-06	-1.690e-06	-1.632e-06	-2.112e-06
	X134_P10			
A to Z	-1.866e-06			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.632	1.9584
X25_P10	1.200	1.768	2.1216
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0010	0.0021	0.0021	0.0020
B	0.0010	0.0019	0.0019	0.0018
C	0.0011	0.0024	0.0023	0.0023
D	0.0015	0.0020	0.0020	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0474	0.0451	2.0326	1.0112
A to Z ↑	0.0373	0.0353	3.7898	1.8445
B to Z ↓	0.0440	0.0412	2.0269	1.0093
B to Z ↑	0.0374	0.0346	3.7882	1.8448
C to Z ↓	0.0395	0.0366	2.0236	1.0069
C to Z ↑	0.0286	0.0261	3.7640	1.8317

D to Z ↓	0.0370	0.0330	1.9983	0.9964
D to Z ↑	0.0329	0.0289	3.7661	1.8328
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0493	0.0520	0.6898	0.5214
A to Z ↑	0.0385	0.0402	1.2491	0.9377
B to Z ↓	0.0455	0.0491	0.6891	0.5212
B to Z ↑	0.0379	0.0404	1.2486	0.9377
C to Z ↓	0.0408	0.0443	0.6865	0.5185
C to Z ↑	0.0288	0.0308	1.2385	0.9288
D to Z ↓	0.0356	0.0373	0.6765	0.5085
D to Z ↑	0.0315	0.0329	1.2396	0.9299

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.650e-07	2.528e-12
X17_P10	3.220e-07	3.789e-12
X25_P10	3.675e-07	4.040e-12
X33_P10	4.129e-07	4.292e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	3.001e-05	7.158e-05	7.031e-05	6.884e-05
B (output stable)	7.183e-05	1.164e-04	1.168e-04	1.211e-04
C (output stable)	3.024e-04	5.062e-04	5.136e-04	4.833e-04
D (output stable)	6.339e-05	7.487e-05	6.872e-05	7.381e-05
A to Z	3.649e-03	6.650e-03	8.147e-03	9.210e-03
B to Z	3.372e-03	5.927e-03	7.427e-03	8.618e-03
C to Z	2.783e-03	4.707e-03	6.214e-03	7.396e-03
D to Z	3.731e-03	6.339e-03	7.850e-03	8.954e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

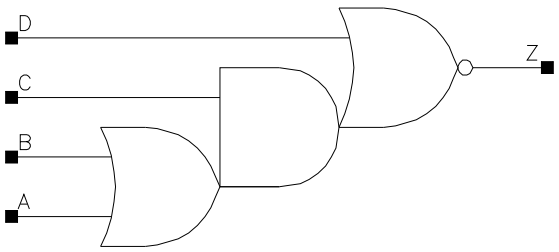
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	-2.508e-06	-4.942e-06	-4.971e-06	-4.822e-06
B (output stable)	-3.350e-06	-5.366e-06	-5.327e-06	-5.322e-06
C (output stable)	-3.368e-06	-6.201e-06	-6.300e-06	-5.606e-06
D (output stable)	3.431e-06	4.992e-06	5.022e-06	3.942e-06
A to Z	-8.806e-06	-1.543e-05	-1.570e-05	-1.567e-05
B to Z	-8.975e-06	-1.584e-05	-1.582e-05	-1.637e-05
C to Z	-3.139e-07	-7.077e-07	-8.349e-07	-1.099e-06
D to Z	-2.514e-06	-4.324e-06	-4.372e-06	-4.444e-06

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.952	1.1424
X11_P10	1.200	1.496	1.7952
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X16_P10	X21_P10
A	0.0009	0.0017	0.0026	0.0034
B	0.0009	0.0016	0.0026	0.0034
C	0.0009	0.0016	0.0025	0.0033
D	0.0011	0.0017	0.0024	0.0032

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0176	0.0170	3.4943	1.8469
A to Z ↑	0.0462	0.0432	11.9952	6.2202
B to Z ↓	0.0171	0.0168	3.4005	1.8113
B to Z ↑	0.0439	0.0415	12.0154	6.2244
C to Z ↓	0.0160	0.0154	3.2222	1.7058
C to Z ↑	0.0288	0.0268	7.8536	4.0266

D to Z ↓	0.0106	0.0092	2.0327	1.0316
D to Z ↑	0.0249	0.0218	8.4633	4.3493
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0169	0.0173	1.2510	0.9630
A to Z ↑	0.0405	0.0423	4.0095	3.0880
B to Z ↓	0.0164	0.0168	1.2568	0.9637
B to Z ↑	0.0396	0.0408	4.0120	3.0872
C to Z ↓	0.0156	0.0156	1.1765	0.9009
C to Z ↑	0.0261	0.0265	2.6624	1.9973
D to Z ↓	0.0093	0.0093	0.7242	0.5533
D to Z ↑	0.0206	0.0206	2.8541	2.1576

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P10	1.458e-07	2.528e-12
X11_P10	2.823e-07	3.537e-12
X16_P10	4.005e-07	4.039e-12
X21_P10	5.385e-07	5.301e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	3.408e-05	6.460e-05	8.672e-05	1.345e-04
B (output stable)	5.963e-05	1.274e-04	1.765e-04	2.488e-04
C (output stable)	2.682e-04	5.239e-04	7.212e-04	1.025e-03
D (output stable)	3.289e-05	6.689e-05	7.657e-05	1.428e-04
A to Z	2.632e-03	4.606e-03	6.443e-03	9.011e-03
B to Z	2.156e-03	3.800e-03	5.458e-03	7.456e-03
C to Z	1.777e-03	3.028e-03	4.348e-03	6.014e-03
D to Z	9.907e-04	1.621e-03	2.175e-03	2.903e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

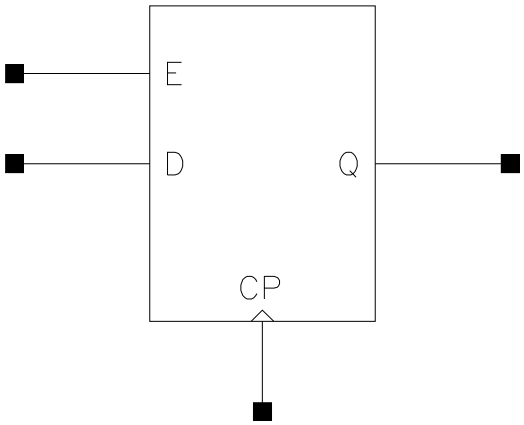
Pin Cycle (vdds)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	-5.711e-06	-8.632e-06	-1.216e-05	-1.850e-05
B (output stable)	-4.250e-06	-1.149e-05	-9.248e-06	-1.566e-05
C (output stable)	-3.277e-05	-6.023e-05	-8.088e-05	-1.222e-04
D (output stable)	4.186e-05	8.931e-05	1.069e-04	1.662e-04
A to Z	-1.323e-05	-2.308e-05	-3.261e-05	-4.845e-05
B to Z	-9.225e-06	-2.066e-05	-2.638e-05	-3.645e-05
C to Z	-1.031e-05	-1.929e-05	-2.459e-05	-3.730e-05
D to Z	-1.870e-07	1.012e-07	5.400e-09	-1.442e-07

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.128	3.7536
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0012	0.0012	0.0012

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0523	0.0607	2.0412	1.0625
CP to Q ↑	0.0613	0.0651	3.8102	1.9043
	X33_P10		**X33_P10**	
CP to Q ↓	0.0873		0.5190	
CP to Q ↑	0.1046		0.9451	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0759	0.0759	0.0759
CP ↑	min_pulse_width to CP	0.0405	0.0502	0.0368
D ↓	hold_rising to CP	-0.0330	-0.0330	-0.0361
D ↑	hold_rising to CP	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.0825	0.0825	0.0825
D ↑	setup_rising to CP	0.0386	0.0386	0.0386
E ↓	hold_rising to CP	-0.0285	-0.0285	-0.0285
E ↑	hold_rising to CP	-0.0087	-0.0087	-0.0087
E ↓	setup_rising to CP	0.0724	0.0724	0.0724
E ↑	setup_rising to CP	0.0882	0.0882	0.0882

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	3.934e-07	6.308e-12
X17_P10	4.393e-07	6.561e-12
X33_P10	5.839e-07	7.569e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

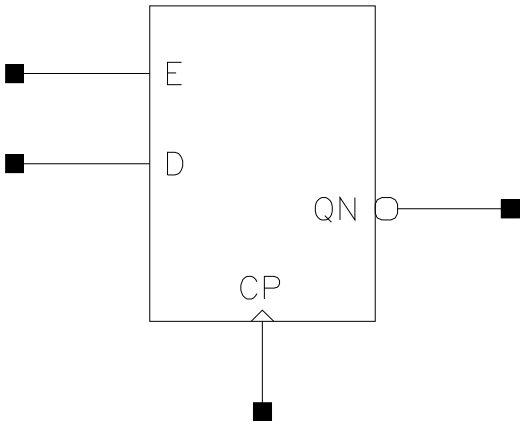
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.960e-03	3.960e-03	3.964e-03
Clock 100Mhz Data 25Mhz	8.445e-03	9.014e-03	1.173e-02
Clock 100Mhz Data 50Mhz	1.293e-02	1.407e-02	1.949e-02
Clock = 0 Data 100Mhz	5.053e-03	5.054e-03	5.054e-03
Clock = 1 Data 100Mhz	1.401e-03	1.401e-03	1.401e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.264	3.9168
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0012	0.0012	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0868	0.0810	2.0887	0.9964
CP to QN ↑	0.0678	0.0707	3.8502	1.8488
	X33_P10		**X33_P10**	
CP to QN ↓	0.0863		0.5206	
CP to QN ↑	0.0784		0.9476	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0759	0.0759	0.0759
CP ↑	min_pulse_width to CP	0.0357	0.0405	0.0453
D ↓	hold_rising to CP	-0.0361	-0.0330	-0.0330
D ↑	hold_rising to CP	-0.0086	-0.0090	-0.0090
D ↓	setup_rising to CP	0.0825	0.0825	0.0825
D ↑	setup_rising to CP	0.0386	0.0386	0.0386
E ↓	hold_rising to CP	-0.0285	-0.0285	-0.0285
E ↑	hold_rising to CP	-0.0087	-0.0087	-0.0087
E ↓	setup_rising to CP	0.0724	0.0724	0.0724
E ↑	setup_rising to CP	0.0882	0.0882	0.0882

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	3.908e-07	6.308e-12
X17_P10	4.610e-07	6.813e-12
X33_P10	5.734e-07	7.569e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

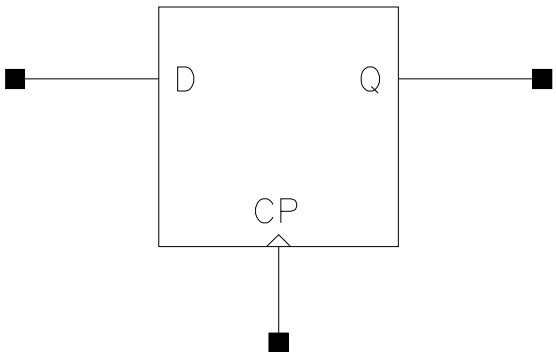
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.960e-03	3.960e-03	3.961e-03
Clock 100Mhz Data 25Mhz	8.524e-03	9.693e-03	1.149e-02
Clock 100Mhz Data 50Mhz	1.309e-02	1.543e-02	1.901e-02
Clock = 0 Data 100Mhz	5.083e-03	5.084e-03	5.085e-03
Clock = 1 Data 100Mhz	1.401e-03	1.401e-03	1.401e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.176	2.6112
X17_P10	1.200	2.448	2.9376
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0543	0.0603	2.0348	1.0540
CP to Q ↑	0.0619	0.0683	3.6854	1.8728
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to Q ↓	0.0768	0.0801	0.6362	0.5790
CP to Q ↑	0.0768	0.0779	1.0550	0.9605

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0662	0.0699	0.0699	0.0699
CP ↑	min_pulse_width to CP	0.0405	0.0491	0.0636	0.0684
D ↓	hold_rising to CP	0.0033	-0.0022	-0.0022	-0.0022
D ↑	hold_rising to CP	0.0078	0.0078	0.0078	0.0078
D ↓	setup_rising to CP	0.0465	0.0465	0.0465	0.0465
D ↑	setup_rising to CP	0.0219	0.0219	0.0219	0.0219

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	3.081e-07	4.796e-12
X17_P10	3.576e-07	5.301e-12
X30_P10	4.311e-07	5.806e-12
X33_P10	4.461e-07	5.806e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

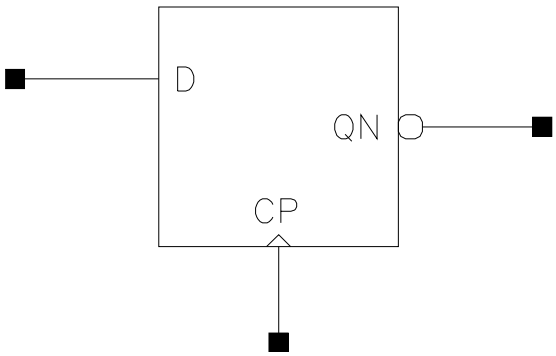
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.151e-03	4.174e-03	4.183e-03	4.187e-03
Clock 100Mhz Data 25Mhz	7.493e-03	8.436e-03	9.639e-03	9.897e-03
Clock 100Mhz Data 50Mhz	1.084e-02	1.270e-02	1.510e-02	1.561e-02
Clock = 0 Data 100Mhz	3.457e-03	3.569e-03	3.603e-03	3.621e-03
Clock = 1 Data 100Mhz	4.045e-05	4.050e-05	4.044e-05	4.045e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0523	0.0631	2.1049	1.0941
CP to QN ↑	0.0550	0.0582	3.6774	1.8698
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to QN ↓	0.0866	0.0864	0.5735	0.5192
CP to QN ↑	0.0721	0.0841	1.0212	0.9465

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0576	0.0576	0.0699	0.0662
CP ↑	min_pulse_width to CP	0.0405	0.0491	0.0405	0.0502
D ↓	hold_rising to CP	0.0075	0.0100	-0.0022	0.0033
D ↑	hold_rising to CP	0.0078	0.0103	0.0078	0.0078
D ↓	setup_rising to CP	0.0319	0.0319	0.0465	0.0465
D ↑	setup_rising to CP	0.0244	0.0219	0.0219	0.0219

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	2.786e-07	4.292e-12
X17_P10	3.251e-07	4.545e-12
X30_P10	4.607e-07	5.804e-12
X33_P10	4.898e-07	6.056e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

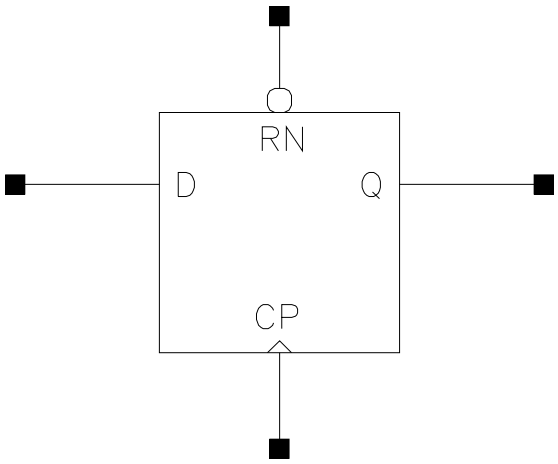
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.011e-03	4.012e-03	4.084e-03	4.114e-03
Clock 100Mhz Data 25Mhz	7.091e-03	7.709e-03	1.008e-02	1.048e-02
Clock 100Mhz Data 50Mhz	1.017e-02	1.141e-02	1.607e-02	1.685e-02
Clock = 0 Data 100Mhz	3.014e-03	3.015e-03	3.238e-03	3.297e-03
Clock = 1 Data 100Mhz	4.010e-05	4.003e-05	4.030e-05	4.039e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0010
D	0.0007	0.0007
RN	0.0010	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0625	0.0795	1.0642	0.6485
CP to Q ↑	0.0703	0.0786	1.8781	1.0599
RN to Q ↓	0.0987	0.1310	1.1521	0.7089

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0747	0.0747
CP ↑	min_pulse_width to CP	0.0502	0.0684
D ↓	hold_rising to CP	-0.0022	-0.0022
D ↑	hold_rising to CP	0.0056	0.0056
D ↓	setup_rising to CP	0.0514	0.0514
D ↑	setup_rising to CP	0.0268	0.0268
RN ↓	min_pulse_width to RN	0.1262	0.1626
RN ↑	recovery_rising to CP	0.0272	0.0272
RN ↑	removal_rising to CP	-0.0127	-0.0096

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P10	4.154e-07	6.560e-12
X30_P10	4.902e-07	7.065e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

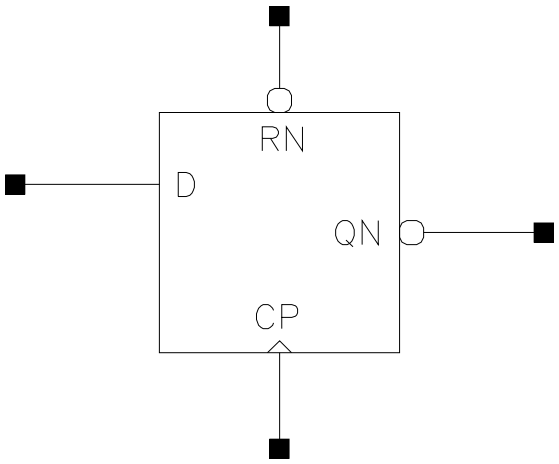
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	4.479e-03	4.484e-03
Clock 100Mhz Data 25Mhz	9.017e-03	1.023e-02
Clock 100Mhz Data 50Mhz	1.355e-02	1.597e-02
Clock = 0 Data 100Mhz	4.233e-03	4.236e-03
Clock = 1 Data 100Mhz	4.135e-05	4.144e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0010
D	0.0007	0.0007
RN	0.0010	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.0828	0.0897	0.9868	0.5748
CP to QN ↑	0.0707	0.0758	1.8388	1.0247
RN to QN ↑	0.1049	0.1114	1.8428	1.0285

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0747	0.0747
CP ↑	min_pulse_width to CP	0.0416	0.0416
D ↓	hold_rising to CP	-0.0019	-0.0019
D ↑	hold_rising to CP	0.0056	0.0056
D ↓	setup_rising to CP	0.0514	0.0514
D ↑	setup_rising to CP	0.0268	0.0268
RN ↓	min_pulse_width to RN	0.1013	0.1062
RN ↑	recovery_rising to CP	0.0241	0.0241
RN ↑	removal_rising to CP	-0.0096	-0.0096

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P10	4.421e-07	6.561e-12
X30_P10	5.134e-07	7.065e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

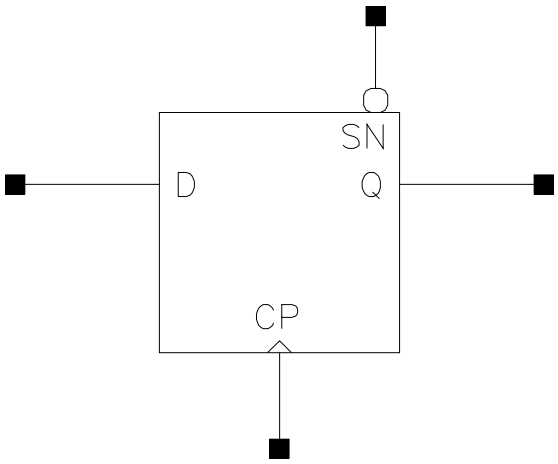
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	4.500e-03	4.499e-03
Clock 100Mhz Data 25Mhz	9.664e-03	1.088e-02
Clock 100Mhz Data 50Mhz	1.483e-02	1.725e-02
Clock = 0 Data 100Mhz	4.294e-03	4.278e-03
Clock = 1 Data 100Mhz	5.493e-05	5.503e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0631	0.0797	1.0667	0.6436
CP to Q ↑	0.0698	0.0778	1.8794	1.0590
SN to Q ↑	0.0718	0.0817	1.8856	1.0626

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0796	0.0796
CP ↑	min_pulse_width to CP	0.0502	0.0684
D ↓	hold_rising to CP	-0.0019	-0.0022
D ↑	hold_rising to CP	0.0078	0.0078
D ↓	setup_rising to CP	0.0563	0.0563
D ↑	setup_rising to CP	0.0219	0.0219
SN ↓	min_pulse_width to SN	0.0691	0.0793
SN ↑	recovery_rising to CP	0.0124	0.0124
SN ↑	removal_rising to CP	0.0339	0.0339

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P10	4.230e-07	6.561e-12
X30_P10	4.942e-07	7.074e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

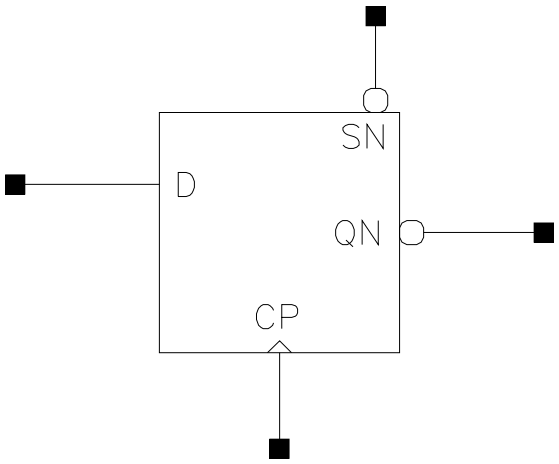
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	4.528e-03	4.519e-03
Clock 100Mhz Data 25Mhz	9.084e-03	1.023e-02
Clock 100Mhz Data 50Mhz	1.364e-02	1.595e-02
Clock = 0 Data 100Mhz	4.222e-03	4.221e-03
Clock = 1 Data 100Mhz	4.006e-05	4.004e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.0822	0.0891	0.9896	0.5770
CP to QN ↑	0.0711	0.0760	1.8353	1.0236
SN to QN ↓	0.0840	0.0912	0.9893	0.5770

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0796	0.0796
CP ↑	min_pulse_width to CP	0.0416	0.0416
D ↓	hold_rising to CP	-0.0019	-0.0019
D ↑	hold_rising to CP	0.0078	0.0078
D ↓	setup_rising to CP	0.0563	0.0563
D ↑	setup_rising to CP	0.0219	0.0219
SN ↓	min_pulse_width to SN	0.0637	0.0637
SN ↑	recovery_rising to CP	0.0124	0.0124
SN ↑	removal_rising to CP	0.0339	0.0339

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P10	4.551e-07	6.561e-12
X30_P10	5.296e-07	7.065e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

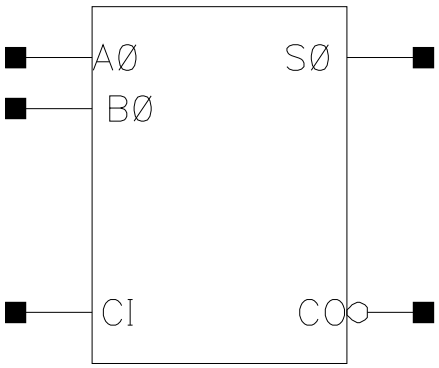
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	4.543e-03	4.543e-03
Clock 100Mhz Data 25Mhz	9.687e-03	1.091e-02
Clock 100Mhz Data 50Mhz	1.483e-02	1.727e-02
Clock = 0 Data 100Mhz	4.221e-03	4.221e-03
Clock = 1 Data 100Mhz	4.067e-05	4.074e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_-P10	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_-P10	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_-P10	1.200	3.672	4.4064
C12T28SOI_LRS1_-FA1X33_P10	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10
A0	0.0033	0.0068	0.0030	0.0058
B0	0.0030	0.0065	0.0032	0.0056
CI	0.0023	0.0051	0.0022	0.0040

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10
A0 to CO ↓	0.0626	0.0680	2.1180	0.5651
A0 to CO ↑	0.0399	0.0412	3.7968	0.9781
A0 to S0 ↓	0.0614	0.0773	2.0813	0.5498
A0 to S0 ↑	0.0627	0.0758	3.7594	0.9608
B0 to CO ↓	0.0610	0.0676	2.1291	0.5692
B0 to CO ↑	0.0410	0.0427	3.7994	0.9736
B0 to S0 ↓	0.0615	0.0781	2.0791	0.5492
B0 to S0 ↑	0.0623	0.0762	3.7620	0.9611
CI to CO ↓	0.0582	0.0649	2.1383	0.5694
CI to CO ↑	0.0406	0.0416	3.7984	0.9784
CI to S0 ↓	0.0606	0.0773	2.0787	0.5491
CI to S0 ↑	0.0617	0.0760	3.7581	0.9607
	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10
A0 to CO ↓	0.0399	0.0491	4.1563	0.7229
A0 to CO ↑	0.0306	0.0350	3.8534	0.9644
A0 to S0 ↓	0.0807	0.0984	2.2449	0.5741
A0 to S0 ↑	0.0722	0.0781	3.9189	0.9818
B0 to CO ↓	0.0403	0.0498	4.1571	0.7243
B0 to CO ↑	0.0289	0.0340	3.8509	0.9646
B0 to S0 ↓	0.0809	0.1004	2.2436	0.5735
B0 to S0 ↑	0.0725	0.0802	3.9205	0.9819
CI to CO ↓	0.0386	0.0655	4.1486	0.7355
CI to CO ↑	0.0319	0.0380	3.9521	0.9718
CI to S0 ↓	0.0469	0.0606	2.2475	0.5751
CI to S0 ↑	0.0387	0.0390	3.9178	0.9819

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_FA1X8_P10	4.322e-07	4.796e-12
C12T28SOI_LR_FA1X33_P10	1.038e-06	9.835e-12
C12T28SOI_LRS1_FA1X8_P10	5.827e-07	7.567e-12
C12T28SOI_LRS1_FA1X33_P10	1.449e-06	1.563e-11

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10
A0 to CO	3.883e-03	1.036e-02	5.840e-03	1.416e-02
A0 to S0	3.890e-03	1.071e-02	7.836e-03	1.758e-02
B0 to CO	3.807e-03	1.029e-02	5.891e-03	1.439e-02
B0 to S0	3.665e-03	1.034e-02	7.924e-03	1.788e-02
CI to CO	3.753e-03	1.021e-02	4.125e-03	1.246e-02
CI to S0	3.620e-03	1.030e-02	4.657e-03	1.340e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P10	C12T28SOI_LR_-FA1X33_P10	C12T28SOI_LRS1_-FA1X8_P10	C12T28SOI_LRS1_-FA1X33_P10
A0 to CO	-2.780e-05	-5.442e-05	3.392e-06	8.100e-06
A0 to S0	-2.137e-05	-4.189e-05	6.042e-06	1.246e-05
B0 to CO	-1.188e-05	-2.251e-05	-9.856e-06	-2.016e-05
B0 to S0	4.940e-07	-4.007e-07	-1.348e-05	-2.727e-05
CI to CO	1.148e-05	2.162e-05	-1.376e-06	-1.693e-06
CI to S0	1.884e-06	1.546e-06	-1.447e-06	7.886e-07

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X33_P10	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X33_P10
A0	0.0012	0.0034
B0	0.0010	0.0029

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
A0 to CO ↓	0.0445	0.0408	2.0752	0.5155
A0 to CO ↑	0.0378	0.0339	3.7588	0.9669
A0 to S0 ↓	0.0570	0.0538	2.0315	0.5161
A0 to S0 ↑	0.0525	0.0567	3.7171	0.9543
B0 to CO ↓	0.0433	0.0381	2.0756	0.5114
B0 to CO ↑	0.0398	0.0349	3.7593	0.9669
B0 to S0 ↓	0.0580	0.0525	2.0324	0.5164
B0 to S0 ↑	0.0519	0.0544	3.7169	0.9543

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.898e-07	3.032e-12
X33_P10	6.780e-07	6.304e-12

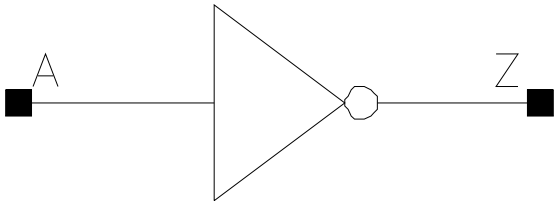
Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X33_P10
A0 to CO	2.971e-03	9.550e-03
A0 to S0	2.693e-03	8.988e-03
B0 to CO	2.946e-03	9.199e-03
B0 to S0	2.606e-03	8.399e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X8_P10	X33_P10
A0 to CO	-8.199e-06	-5.008e-05
A0 to S0	-5.281e-06	-3.091e-05
B0 to CO	6.286e-06	3.935e-05
B0 to S0	3.091e-06	1.922e-05

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.272	0.3264
X6_P10	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X13_P10	1.200	0.408	0.4896
X17_P10	1.200	0.408	0.4896
X21_P10	1.200	0.544	0.6528
X25_P10	1.200	0.544	0.6528
X29_P10	1.200	0.680	0.8160
X33_P10	1.200	0.680	0.8160
X50_P10	1.200	0.952	1.1424
X58_P10	1.200	1.088	1.3056
X67_P10	1.200	1.224	1.4688
X75_P10	1.200	1.360	1.6320
X84_P10	1.200	1.496	1.7952
X100_P10	1.200	1.768	2.1216
X134_P10	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0006	0.0007	0.0009	0.0013
	X17_P10	X21_P10	X25_P10	X29_P10
A	0.0017	0.0022	0.0025	0.0029
	X33_P10	X50_P10	X58_P10	X67_P10
A	0.0033	0.0049	0.0057	0.0066
	X75_P10	X84_P10	X100_P10	X134_P10

A	0.0075	0.0084	0.0104	0.0144

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0101	0.0095	3.8298	2.9612
A to Z ↑	0.0178	0.0166	7.3290	5.5156
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0085	0.0075	2.0218	1.3110
A to Z ↑	0.0152	0.0140	3.8026	2.5087
	X17_P10	**X21_P10**	**X17_P10**	**X21_P10**
A to Z ↓	0.0073	0.0079	1.0066	0.8112
A to Z ↑	0.0134	0.0142	1.8719	1.5077
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0078	0.0074	0.6924	0.5882
A to Z ↑	0.0138	0.0133	1.2592	1.0765
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0072	0.0075	0.5210	0.3526
A to Z ↑	0.0129	0.0130	0.9435	0.6317
	X58_P10	**X67_P10**	**X58_P10**	**X67_P10**
A to Z ↓	0.0078	0.0076	0.3062	0.2691
A to Z ↑	0.0134	0.0131	0.5444	0.4768
	X75_P10	**X84_P10**	**X75_P10**	**X84_P10**
A to Z ↓	0.0080	0.0082	0.2432	0.2198
A to Z ↑	0.0135	0.0136	0.4270	0.3862
	X100_P10	**X134_P10**	**X100_P10**	**X134_P10**
A to Z ↓	0.0089	0.0095	0.1872	0.1462
A to Z ↑	0.0142	0.0147	0.3251	0.2498

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	2.865e-08	1.268e-12
X6_P10	3.564e-08	1.268e-12
X8_P10	5.047e-08	1.267e-12
X13_P10	7.818e-08	1.519e-12
X17_P10	9.997e-08	1.519e-12
X21_P10	1.242e-07	1.770e-12
X25_P10	1.446e-07	1.770e-12
X29_P10	1.693e-07	2.016e-12
X33_P10	1.885e-07	2.025e-12
X50_P10	2.760e-07	2.528e-12
X58_P10	3.198e-07	2.780e-12
X67_P10	3.637e-07	3.029e-12
X75_P10	4.075e-07	3.283e-12
X84_P10	4.513e-07	3.535e-12
X100_P10	5.390e-07	4.036e-12
X134_P10	7.143e-07	5.045e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10

A to Z	4.136e-04	4.827e-04	5.800e-04	7.420e-04
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	9.065e-04	1.315e-03	1.479e-03	1.570e-03
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	1.663e-03	2.494e-03	3.181e-03	3.345e-03
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	3.858e-03	4.158e-03	5.023e-03	6.702e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

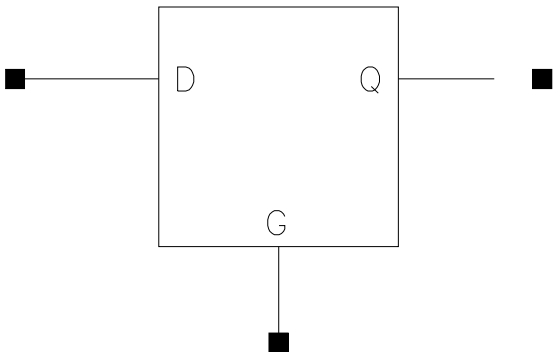
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	-3.030e-08	2.052e-07	2.309e-07	4.204e-07
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	5.082e-07	1.132e-06	1.136e-06	9.019e-07
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	4.832e-06	3.050e-07	1.600e-06	-9.000e-07
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	7.566e-06	-1.947e-06	3.572e-06	3.963e-06

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X23_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P10	X23_P10
D	0.0006	0.0014
G	0.0012	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X23_P10	X8_P10	X23_P10
D to Q ↓	0.0703	0.0559	2.1635	1.0013
D to Q ↑	0.0398	0.0403	3.7047	0.9807
G to Q ↓	0.0714	0.0551	2.1598	1.0004
G to Q ↑	0.0389	0.0366	3.7087	0.9812

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P10	X23_P10
D ↓	hold_falling to G	-0.0264	-0.0135
D ↑	hold_falling to G	-0.0048	-0.0047
D ↓	setup_falling to G	0.0678	0.0514
D ↑	setup_falling to G	0.0422	0.0471
G ↑	min_pulse_width to G	0.0589	0.0523

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.626e-07	3.032e-12
X23_P10	3.059e-07	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X23_P10
D (output stable)	1.748e-05	7.458e-05
G (output stable)	9.526e-04	1.840e-03
D to Q	4.447e-03	8.691e-03
G to Q	4.045e-03	7.577e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

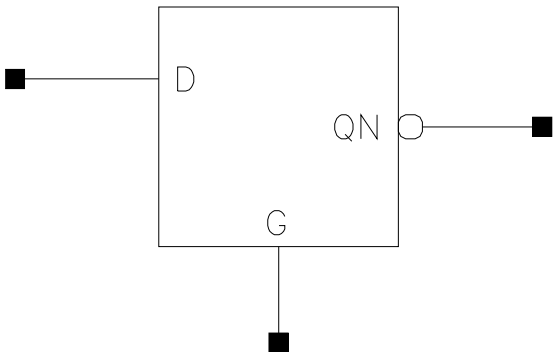
Pin Cycle (vdds)	X8_P10	X23_P10
D (output stable)	-2.066e-06	-7.034e-06
G (output stable)	1.855e-08	4.647e-07
D to Q	-4.142e-06	-8.804e-06
G to Q	3.184e-05	2.189e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P10
D	0.0006
G	0.0014

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P10	X17_P10
D to QN ↓	0.0541	0.9933
D to QN ↑	0.0761	1.8241
G to QN ↓	0.0524	0.9935
G to QN ↑	0.0745	1.8261

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P10
D ↓	hold_falling to G	-0.0315
D ↑	hold_falling to G	-0.0076
D ↓	setup_falling to G	0.0585
D ↑	setup_falling to G	0.0352
G ↑	min_pulse_width to G	0.0453

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P10	2.296e-07	3.284e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X17_P10
D (output stable)	3.695e-05
G (output stable)	1.036e-03
D to QN	5.802e-03
G to QN	5.226e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

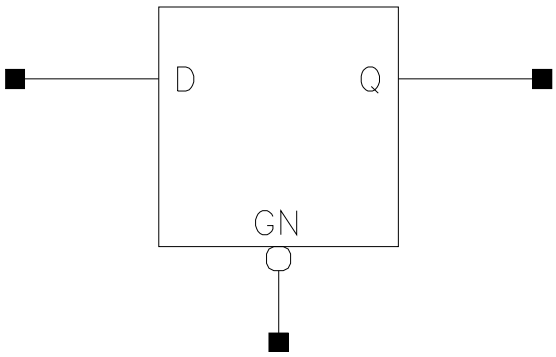
Pin Cycle (vdds)	X17_P10
D (output stable)	-8.618e-06
G (output stable)	1.348e-06
D to QN	-4.094e-06
G to QN	6.514e-05

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
D	0.0006	0.0008	0.0018
GN	0.0012	0.0015	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D to Q ↓	0.0709	0.0615	2.1725	1.0582
D to Q ↑	0.0408	0.0379	3.7117	1.8996
GN to Q ↓	0.0629	0.0539	2.1737	1.0593
GN to Q ↑	0.0623	0.0592	3.7036	1.8990

	X33_P10		X33_P10	
D to Q ↓	0.0593		0.5398	
D to Q ↑	0.0329		0.9542	
GN to Q ↓	0.0507		0.5404	
GN to Q ↑	0.0469		0.9529	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X33_P10
D ↓	hold_rising to GN	-0.0309	-0.0238	-0.0238
D ↑	hold_rising to GN	-0.0016	0.0007	0.0029
D ↓	setup_rising to GN	0.0783	0.0686	0.0658
D ↑	setup_rising to GN	0.0390	0.0338	0.0285
GN ↓	min_pulse_width to GN	0.0826	0.0731	0.0684

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.635e-07	3.033e-12
X17_P10	2.376e-07	3.537e-12
X33_P10	3.920e-07	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
D (output stable)	2.112e-05	3.734e-05	8.548e-05
GN (output stable)	9.507e-04	1.298e-03	1.498e-03
D to Q	4.451e-03	6.192e-03	1.007e-02
GN to Q	6.396e-03	8.635e-03	1.261e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

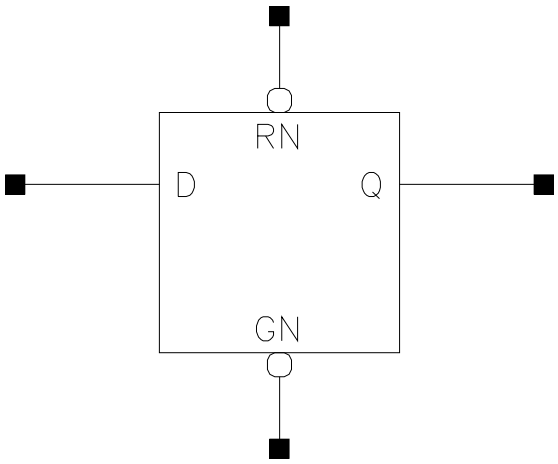
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
D (output stable)	-2.009e-06	-3.513e-06	-7.217e-06
GN (output stable)	1.705e-08	-1.884e-07	2.933e-07
D to Q	-3.846e-06	-5.851e-06	-9.065e-06
GN to Q	-4.624e-05	-2.618e-05	-3.333e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.496	1.7952
X33_P10	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X33_P10
D	0.0006	0.0014
GN	0.0013	0.0024
RN	0.0006	0.0007

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
D to Q ↓	0.0665	0.0598	2.0956	0.5440
D to Q ↑	0.0520	0.0643	3.7734	0.9814

GN to Q ↓	0.0595	0.0545	2.0972	0.5440
GN to Q ↑	0.0698	0.0701	3.7699	0.9810
RN to Q ↓	0.0499	0.0895	2.0063	0.6039
RN to Q ↑	0.0550	0.0693	3.7689	0.9811

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P10	X33_P10
D ↓	hold_rising to GN	-0.0287	-0.0186
D ↑	hold_rising to GN	-0.0118	-0.0264
D ↓	setup_rising to GN	0.0707	0.0637
D ↑	setup_rising to GN	0.0487	0.0682
GN ↓	min_pulse_width to GN	0.0741	0.0732
RN ↓	min_pulse_width to RN	0.0605	0.1089
RN ↑	recovery_rising to GN	0.0536	0.0752
RN ↑	removal_rising to GN	-0.0339	-0.0508

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.810e-07	3.537e-12
X33_P10	3.879e-07	5.302e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X33_P10
D (output stable)	8.975e-05	1.485e-04
GN (output stable)	1.105e-03	1.643e-03
RN (output stable)	1.936e-05	3.737e-05
D to Q	4.424e-03	1.069e-02
GN to Q	6.509e-03	1.377e-02
RN to Q	3.569e-03	7.958e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

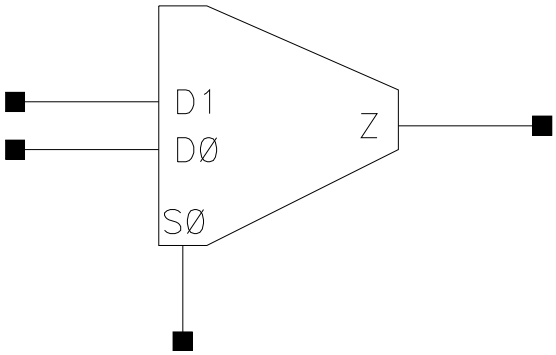
Pin Cycle (vdds)	X8_P10	X33_P10
D (output stable)	-6.203e-06	-1.764e-05
GN (output stable)	2.093e-06	7.141e-06
RN (output stable)	2.274e-06	2.621e-06
D to Q	-1.474e-05	-2.059e-05
GN to Q	-5.883e-05	-2.177e-06
RN to Q	3.647e-06	-3.102e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
D0	0.0008	0.0011	0.0015	0.0020
D1	0.0008	0.0011	0.0015	0.0020
S0	0.0014	0.0015	0.0017	0.0025

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D0 to Z ↓	0.0528	0.0470	2.0753	1.0184
D0 to Z ↑	0.0381	0.0347	3.8008	1.8583
D1 to Z ↓	0.0507	0.0467	2.0703	1.0171
D1 to Z ↑	0.0349	0.0327	3.7905	1.8547
S0 to Z ↓	0.0448	0.0429	2.0673	1.0156
S0 to Z ↑	0.0409	0.0407	3.7939	1.8578

	X25_P10	X33_P10	X25_P10	X33_P10
D0 to Z ↓	0.0503	0.0454	0.7059	0.5286
D0 to Z ↑	0.0382	0.0348	1.2507	0.9359
D1 to Z ↓	0.0540	0.0473	0.7087	0.5293
D1 to Z ↑	0.0361	0.0331	1.2481	0.9357
S0 to Z ↓	0.0493	0.0449	0.7059	0.5282
S0 to Z ↑	0.0457	0.0415	1.2498	0.9361

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.626e-07	3.031e-12
X17_P10	2.677e-07	3.283e-12
X25_P10	3.803e-07	5.030e-12
X33_P10	5.166e-07	5.298e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	8.426e-04	1.192e-03	1.271e-03	1.676e-03
D1 (output stable)	6.700e-04	1.083e-03	1.445e-03	1.773e-03
S0 (output stable)	1.159e-03	1.320e-03	1.728e-03	2.097e-03
D0 to Z	3.095e-03	4.899e-03	7.618e-03	9.486e-03
D1 to Z	2.840e-03	4.752e-03	7.664e-03	9.305e-03
S0 to Z	3.546e-03	5.259e-03	8.561e-03	1.039e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

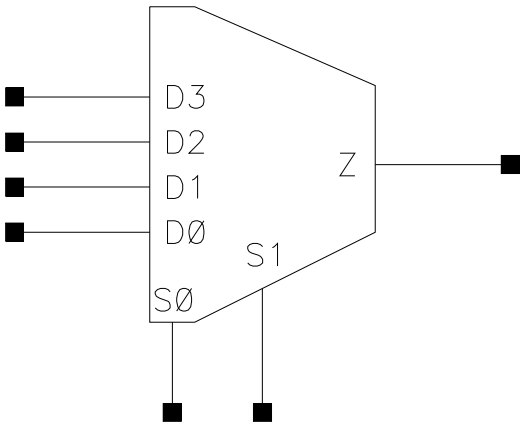
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	8.970e-08	-2.355e-08	3.800e-07	5.535e-07
D1 (output stable)	-1.838e-07	1.806e-07	8.315e-08	1.000e-07
S0 (output stable)	-1.481e-07	-1.359e-07	-2.723e-07	1.963e-07
D0 to Z	-1.549e-07	-6.035e-07	1.144e-07	-4.715e-07
D1 to Z	-2.852e-07	5.385e-08	-5.360e-07	9.100e-08
S0 to Z	-2.448e-07	-3.362e-07	-1.708e-07	-4.519e-07

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.312	2.7744
X31_P10	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P10	X31_P10
D0	0.0006	0.0015
D1	0.0006	0.0015
D2	0.0006	0.0015
D3	0.0006	0.0015
S0	0.0020	0.0039
S1	0.0012	0.0025

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X31_P10	X8_P10	X31_P10

D0 to Z ↓	0.0945	0.0958	2.2043	0.6140
D0 to Z ↑	0.0528	0.0544	3.8156	1.0269
D1 to Z ↓	0.0938	0.0959	2.2018	0.6139
D1 to Z ↑	0.0531	0.0541	3.8156	1.0270
D2 to Z ↓	0.1009	0.0903	2.2167	0.6077
D2 to Z ↑	0.0552	0.0502	3.8245	1.0205
D3 to Z ↓	0.1005	0.0895	2.2159	0.6068
D3 to Z ↑	0.0545	0.0519	3.8224	1.0239
S0 to Z ↓	0.1016	0.1013	2.2055	0.6098
S0 to Z ↑	0.0672	0.0701	3.8222	1.0253
S1 to Z ↓	0.0690	0.0676	2.2084	0.6105
S1 to Z ↑	0.0508	0.0511	3.8131	1.0230

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	2.532e-07	5.048e-12
X31_P10	7.336e-07	9.333e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X31_P10
D0 (output stable)	4.752e-05	2.003e-04
D1 (output stable)	4.696e-05	2.083e-04
D2 (output stable)	5.247e-05	1.614e-04
D3 (output stable)	4.296e-05	1.876e-04
S0 (output stable)	1.880e-03	4.478e-03
S1 (output stable)	1.104e-03	2.254e-03
D0 to Z	3.246e-03	1.068e-02
D1 to Z	3.241e-03	1.075e-02
D2 to Z	3.470e-03	1.005e-02
D3 to Z	3.455e-03	1.002e-02
S0 to Z	5.288e-03	1.518e-02
S1 to Z	3.460e-03	9.446e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

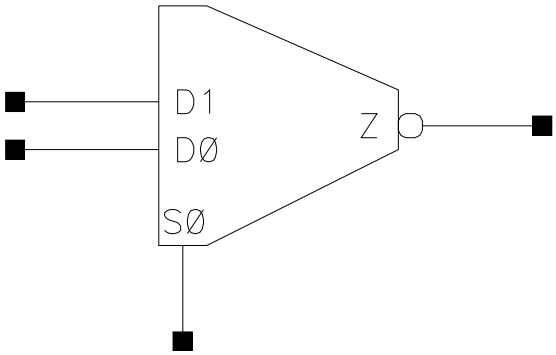
Pin Cycle (vdds)	X8_P10	X31_P10
D0 (output stable)	-4.935e-06	-2.055e-05
D1 (output stable)	-5.222e-06	-2.271e-05
D2 (output stable)	-8.132e-06	-2.513e-05
D3 (output stable)	-5.563e-06	-2.049e-05
S0 (output stable)	-3.133e-05	-1.076e-04
S1 (output stable)	1.881e-05	7.030e-05
D0 to Z	-5.381e-06	-2.140e-05
D1 to Z	-6.033e-06	-2.321e-05
D2 to Z	-5.880e-06	-1.897e-05
D3 to Z	-5.930e-06	-1.778e-05
S0 to Z	-2.523e-05	-8.427e-05
S1 to Z	1.642e-05	7.164e-05

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.816	0.9792
X5_P10	1.200	0.952	1.1424
X10_P10	1.200	1.768	2.1216
X16_P10	1.200	2.448	2.9376
X21_P10	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P10	X5_P10	X10_P10	X16_P10
D0	0.0006	0.0008	0.0017	0.0026
D1	0.0005	0.0009	0.0017	0.0026
S0	0.0012	0.0020	0.0027	0.0041
	X21_P10			
D0	0.0035			
D1	0.0034			
S0	0.0047			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X5_P10	X3_P10	X5_P10
D0 to Z ↓	0.0169	0.0167	6.7144	4.1461

D0 to Z ↑	0.0325	0.0295	17.0127	8.6650
D1 to Z ↓	0.0165	0.0159	6.6472	3.9275
D1 to Z ↑	0.0337	0.0308	17.0268	8.9730
S0 to Z ↓	0.0265	0.0220	6.6643	4.0249
S0 to Z ↑	0.0295	0.0243	16.9950	8.8114
	X10_P10	**X16_P10**	**X10_P10**	**X16_P10**
D0 to Z ↓	0.0185	0.0173	1.9479	1.2740
D0 to Z ↑	0.0317	0.0304	4.0325	2.6570
D1 to Z ↓	0.0167	0.0165	1.8797	1.2436
D1 to Z ↑	0.0321	0.0313	4.0913	2.6791
S0 to Z ↓	0.0265	0.0232	1.9094	1.2570
S0 to Z ↑	0.0284	0.0247	4.0617	2.6655
	X21_P10		**X21_P10**	
D0 to Z ↓	0.0172		0.9737	
D0 to Z ↑	0.0298		2.0125	
D1 to Z ↓	0.0165		0.9438	
D1 to Z ↑	0.0313		2.0013	
S0 to Z ↓	0.0243		0.9570	
S0 to Z ↑	0.0254		2.0042	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P10	8.796e-08	2.276e-12
X5_P10	1.563e-07	2.529e-12
X10_P10	2.873e-07	4.041e-12
X16_P10	4.523e-07	5.301e-12
X21_P10	5.686e-07	6.564e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	2.233e-05	4.926e-05	1.842e-04	2.494e-04
D1 (output stable)	3.963e-05	1.981e-04	2.226e-04	3.409e-04
S0 (output stable)	9.661e-04	1.349e-03	2.413e-03	3.665e-03
D0 to Z	9.782e-04	1.618e-03	4.000e-03	5.615e-03
D1 to Z	9.746e-04	1.599e-03	3.813e-03	5.544e-03
S0 to Z	1.659e-03	2.280e-03	4.851e-03	6.652e-03
	X21_P10			
D0 (output stable)	3.331e-04			
D1 (output stable)	4.804e-04			
S0 (output stable)	4.134e-03			
D0 to Z	7.208e-03			
D1 to Z	7.313e-03			
S0 to Z	8.196e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	-2.304e-06	-4.276e-06	-9.086e-06	-1.914e-05
D1 (output stable)	-9.679e-06	-4.449e-05	-3.999e-05	-6.372e-05
S0 (output stable)	5.634e-06	3.343e-05	2.311e-05	3.332e-05
D0 to Z	-2.046e-06	-3.499e-06	-7.458e-06	-1.694e-05

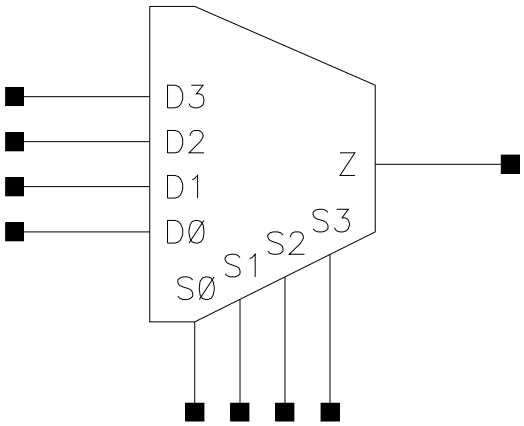
D1 to Z	-2.098e-06	-6.682e-06	-7.711e-06	-1.398e-05
S0 to Z	5.424e-06	1.002e-05	2.069e-05	5.037e-05
	X21_P10			
D0 (output stable)	-2.401e-05			
D1 (output stable)	-1.050e-04			
S0 (output stable)	6.025e-05			
D0 to Z	-1.880e-05			
D1 to Z	-2.193e-05			
S0 to Z	5.723e-05			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	1.768	2.1216
X27_P10	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P10	X27_P10
D0	0.0007	0.0020
D1	0.0007	0.0021
D2	0.0007	0.0020
D3	0.0007	0.0021
S0	0.0007	0.0019
S1	0.0007	0.0019
S2	0.0007	0.0019
S3	0.0007	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	X27_P10	X7_P10	X27_P10
D0 to Z ↓	0.0697	0.0589	3.4486	0.9506
D0 to Z ↑	0.0442	0.0375	3.7240	0.9292
D1 to Z ↓	0.0632	0.0535	3.4463	0.9508
D1 to Z ↑	0.0406	0.0338	3.7135	0.9261
D2 to Z ↓	0.0701	0.0562	3.4644	0.9537
D2 to Z ↑	0.0433	0.0352	3.7415	0.9331
D3 to Z ↓	0.0636	0.0509	3.4559	0.9522
D3 to Z ↑	0.0398	0.0315	3.7324	0.9305
S0 to Z ↓	0.0673	0.0557	3.4480	0.9502
S0 to Z ↑	0.0466	0.0390	3.7237	0.9288
S1 to Z ↓	0.0612	0.0501	3.4442	0.9499
S1 to Z ↑	0.0427	0.0348	3.7144	0.9262
S2 to Z ↓	0.0676	0.0530	3.4659	0.9524
S2 to Z ↑	0.0457	0.0366	3.7383	0.9335
S3 to Z ↓	0.0616	0.0476	3.4602	0.9516
S3 to Z ↑	0.0419	0.0326	3.7333	0.9308

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X7_P10	2.193e-07	4.040e-12
X27_P10	7.948e-07	7.569e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X7_P10	X27_P10
D0 (output stable)	5.368e-04	1.698e-03
D1 (output stable)	4.208e-04	1.271e-03
D2 (output stable)	5.325e-04	1.666e-03
D3 (output stable)	3.915e-04	1.177e-03
S0 (output stable)	5.520e-04	1.686e-03
S1 (output stable)	4.124e-04	1.228e-03
S2 (output stable)	4.936e-04	1.462e-03
S3 (output stable)	3.652e-04	1.044e-03
D0 to Z	4.047e-03	1.252e-02
D1 to Z	3.557e-03	1.077e-02
D2 to Z	3.878e-03	1.079e-02
D3 to Z	3.388e-03	9.058e-03
S0 to Z	3.938e-03	1.187e-02
S1 to Z	3.439e-03	1.010e-02
S2 to Z	3.764e-03	1.010e-02
S3 to Z	3.270e-03	8.414e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

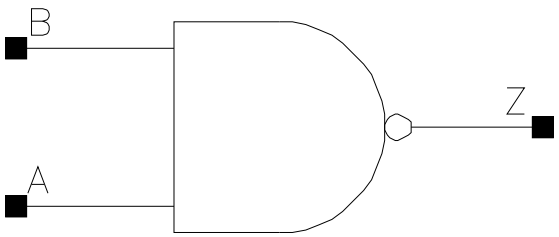
Pin Cycle (vdds)	X7_P10	X27_P10
D0 (output stable)	-3.930e-06	-1.263e-05
D1 (output stable)	2.182e-07	6.638e-07
D2 (output stable)	-9.796e-06	-2.970e-05
D3 (output stable)	7.286e-06	2.116e-05
S0 (output stable)	-9.090e-06	-2.594e-05
S1 (output stable)	6.645e-06	1.835e-05
S2 (output stable)	-6.093e-06	-1.772e-05
S3 (output stable)	2.091e-06	5.985e-06
D0 to Z	-7.784e-06	-2.213e-05
D1 to Z	-1.512e-07	-4.252e-07
D2 to Z	-7.985e-06	-2.399e-05
D3 to Z	4.741e-08	-6.036e-07
S0 to Z	-8.577e-06	-2.553e-05
S1 to Z	-2.592e-07	-7.501e-07
S2 to Z	-7.830e-06	-2.354e-05
S3 to Z	-8.177e-08	-3.908e-07

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P10	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P10	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P10	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P10	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P10	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P10	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P10	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P10	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P10	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P10	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P10	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P10	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P10	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P10	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P10	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P10	C12T28SOI_LR_-NAND2X5_P10	C12T28SOI_LR_-NAND2X7_P10	C12T28SOI_LR_-NAND2X10_P10
A	0.0006	0.0007	0.0009	0.0014
B	0.0006	0.0007	0.0008	0.0013
	C12T28SOI_LR_-NAND2X13_P10	C12T28SOI_LR_-NAND2X17_P10	C12T28SOI_LR_-NAND2X20_P10	C12T28SOI_LR_-NAND2X24_P10
A	0.0017	0.0022	0.0025	0.0030
B	0.0016	0.0021	0.0024	0.0028
	C12T28SOI_LR_-NAND2X27_P10	C12T28SOI_LR_-NAND2X42_P10	C12T28SOI_LR_-NAND2X47_P10	C12T28SOI_LR_-NAND2X50_P10
A	0.0033	0.0011	0.0011	0.0011
B	0.0031	0.0011	0.0011	0.0011
	C12T28SOI_LR_-NAND2X58_P10	C12T28SOI_LR_-NAND2X67_P10	C12T28SOI_-LRBR0D8_-NAND2X7_P10	C12T28SOI_-LRBR0D8_-NAND2X14_P10
A	0.0011	0.0011	0.0008	0.0017
B	0.0011	0.0011	0.0008	0.0016
	C12T28SOI_LRS_-NAND2X40_P10	C12T28SOI_LRS_-NAND2X54_P10		
A	0.0050	0.0067		
B	0.0047	0.0062		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P10	**C12T28SOI_LR_-NAND2X5_P10**	**C12T28SOI_LR_-NAND2X3_P10**	**C12T28SOI_LR_-NAND2X5_P10**
A to Z ↓	0.0132	0.0120	6.5262	4.1927
A to Z ↑	0.0208	0.0191	7.3305	4.6771
B to Z ↓	0.0137	0.0119	6.6149	4.2475
B to Z ↑	0.0190	0.0169	7.3808	4.7090
	C12T28SOI_LR_-NAND2X7_P10	**C12T28SOI_LR_-NAND2X10_P10**	**C12T28SOI_LR_-NAND2X7_P10**	**C12T28SOI_LR_-NAND2X10_P10**
A to Z ↓	0.0118	0.0137	3.5209	2.3456
A to Z ↑	0.0186	0.0199	3.7777	2.4784
B to Z ↓	0.0117	0.0119	3.5581	2.3827
B to Z ↑	0.0163	0.0164	3.8108	2.4965
	C12T28SOI_LR_-NAND2X13_P10	**C12T28SOI_LR_-NAND2X17_P10**	**C12T28SOI_LR_-NAND2X13_P10**	**C12T28SOI_LR_-NAND2X17_P10**
A to Z ↓	0.0131	0.0131	1.8062	1.4353

A to Z ↑	0.0189	0.0192	1.8545	1.4969
B to Z ↓	0.0112	0.0118	1.8336	1.4564
B to Z ↑	0.0154	0.0161	1.8723	1.5078
	C12T28SOI_LR_-NAND2X20_P10	**C12T28SOI_LR_-NAND2X24_P10**	**C12T28SOI_LR_-NAND2X20_P10**	**C12T28SOI_LR_-NAND2X24_P10**
A to Z ↓	0.0129	0.0134	1.2375	1.0553
A to Z ↑	0.0187	0.0191	1.2488	1.0669
B to Z ↓	0.0117	0.0115	1.2558	1.0702
B to Z ↑	0.0157	0.0155	1.2599	1.0752
	C12T28SOI_LR_-NAND2X27_P10	**C12T28SOI_LR_-NAND2X42_P10**	**C12T28SOI_LR_-NAND2X27_P10**	**C12T28SOI_LR_-NAND2X42_P10**
A to Z ↓	0.0131	0.0448	0.9419	0.4171
A to Z ↑	0.0186	0.0482	0.9362	0.7418
B to Z ↓	0.0113	0.0458	0.9540	0.4174
B to Z ↑	0.0151	0.0465	0.9437	0.7413
	C12T28SOI_LR_-NAND2X47_P10	**C12T28SOI_LR_-NAND2X50_P10**	**C12T28SOI_LR_-NAND2X47_P10**	**C12T28SOI_LR_-NAND2X50_P10**
A to Z ↓	0.0463	0.0467	0.3713	0.3482
A to Z ↑	0.0491	0.0494	0.6456	0.6192
B to Z ↓	0.0473	0.0477	0.3712	0.3486
B to Z ↑	0.0472	0.0476	0.6459	0.6189
	C12T28SOI_LR_-NAND2X58_P10	**C12T28SOI_LR_-NAND2X67_P10**	**C12T28SOI_LR_-NAND2X58_P10**	**C12T28SOI_LR_-NAND2X67_P10**
A to Z ↓	0.0491	0.0506	0.3030	0.2667
A to Z ↑	0.0510	0.0519	0.5325	0.4683
B to Z ↓	0.0501	0.0517	0.3029	0.2666
B to Z ↑	0.0493	0.0502	0.5332	0.4686
	C12T28SOI_-LRBR0D8_-NAND2X7_P10	**C12T28SOI_-LRBR0D8_-NAND2X14_P10**	**C12T28SOI_-LRBR0D8_-NAND2X7_P10**	**C12T28SOI_-LRBR0D8_-NAND2X14_P10**
A to Z ↓	0.0104	0.0117	2.6421	1.4001
A to Z ↑	0.0219	0.0223	5.0386	2.4576
B to Z ↓	0.0097	0.0090	2.6913	1.4311
B to Z ↑	0.0184	0.0168	5.2008	2.5096
	C12T28SOI_LRS_-NAND2X40_P10	**C12T28SOI_LRS_-NAND2X54_P10**	**C12T28SOI_LRS_-NAND2X40_P10**	**C12T28SOI_LRS_-NAND2X54_P10**
A to Z ↓	0.0130	0.0130	0.6391	0.4835
A to Z ↑	0.0185	0.0185	0.6273	0.4729
B to Z ↓	0.0114	0.0114	0.6475	0.4906
B to Z ↑	0.0151	0.0151	0.6328	0.4777

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P10	3.978e-08	1.520e-12
C12T28SOI_LR_NAND2X5_P10	5.983e-08	1.520e-12
C12T28SOI_LR_NAND2X7_P10	7.108e-08	1.520e-12
C12T28SOI_LR_NAND2X10_P10	1.076e-07	2.024e-12
C12T28SOI_LR_NAND2X13_P10	1.393e-07	2.024e-12
C12T28SOI_LR_NAND2X17_P10	1.745e-07	2.528e-12
C12T28SOI_LR_NAND2X20_P10	2.048e-07	2.529e-12
C12T28SOI_LR_NAND2X24_P10	2.411e-07	3.033e-12
C12T28SOI_LR_NAND2X27_P10	2.703e-07	3.033e-12

C12T28SOI_LR_NAND2X42_P10	3.783e-07	3.268e-12
C12T28SOI_LR_NAND2X47_P10	4.105e-07	3.530e-12
C12T28SOI_LR_NAND2X50_P10	4.200e-07	3.530e-12
C12T28SOI_LR_NAND2X58_P10	4.617e-07	3.782e-12
C12T28SOI_LR_NAND2X67_P10	5.034e-07	4.052e-12
C12T28SOI_LRBR0D8_NAND2X7_-P10	7.866e-08	2.774e-12
C12T28SOI_LRBR0D8_NAND2X14_-P10	1.529e-07	3.305e-12
C12T28SOI_LRS_NAND2X40_P10	4.015e-07	4.041e-12
C12T28SOI_LRS_NAND2X54_P10	5.327e-07	5.047e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P10	C12T28SOI_LR_-NAND2X5_P10	C12T28SOI_LR_-NAND2X7_P10	C12T28SOI_LR_-NAND2X10_P10
A (output stable)	1.065e-05	1.638e-05	1.940e-05	4.513e-05
B (output stable)	3.817e-05	5.962e-05	7.226e-05	3.335e-04
A to Z	6.427e-04	8.379e-04	9.879e-04	1.785e-03
B to Z	5.071e-04	6.202e-04	7.246e-04	1.125e-03
	C12T28SOI_LR_-NAND2X13_P10	C12T28SOI_LR_-NAND2X17_P10	C12T28SOI_LR_-NAND2X20_P10	C12T28SOI_LR_-NAND2X24_P10
A (output stable)	5.416e-05	7.602e-05	8.447e-05	1.062e-04
B (output stable)	3.852e-04	3.943e-04	4.380e-04	6.544e-04
A to Z	2.123e-03	2.728e-03	3.082e-03	3.802e-03
B to Z	1.297e-03	1.799e-03	2.020e-03	2.354e-03
	C12T28SOI_LR_-NAND2X27_P10	C12T28SOI_LR_-NAND2X42_P10	C12T28SOI_LR_-NAND2X47_P10	C12T28SOI_LR_-NAND2X50_P10
A (output stable)	1.133e-04	2.069e-05	2.072e-05	2.076e-05
B (output stable)	6.950e-04	7.865e-05	7.908e-05	7.877e-05
A to Z	4.094e-03	1.108e-02	1.191e-02	1.222e-02
B to Z	2.506e-03	1.081e-02	1.164e-02	1.195e-02
	C12T28SOI_LR_-NAND2X58_P10	C12T28SOI_LR_-NAND2X67_P10	C12T28SOI_-LRBR0D8_-NAND2X7_P10	C12T28SOI_-LRBR0D8_-NAND2X14_P10
A (output stable)	2.089e-05	2.089e-05	2.460e-05	6.691e-05
B (output stable)	7.888e-05	7.936e-05	9.560e-05	4.856e-04
A to Z	1.383e-02	1.495e-02	1.041e-03	2.258e-03
B to Z	1.355e-02	1.467e-02	6.831e-04	1.187e-03
	C12T28SOI_LRS_-NAND2X40_P10	C12T28SOI_LRS_-NAND2X54_P10		
A (output stable)	1.672e-04	2.200e-04		
B (output stable)	9.675e-04	1.244e-03		
A to Z	6.059e-03	7.933e-03		
B to Z	3.748e-03	4.950e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P10	C12T28SOI_LR_-NAND2X5_P10	C12T28SOI_LR_-NAND2X7_P10	C12T28SOI_LR_-NAND2X10_P10
A (output stable)	5.630e-08	1.500e-08	-5.500e-09	4.866e-07
B (output stable)	2.940e-08	-1.440e-08	-3.500e-08	-2.429e-06
A to Z	-6.210e-08	-1.096e-07	2.447e-07	5.580e-07

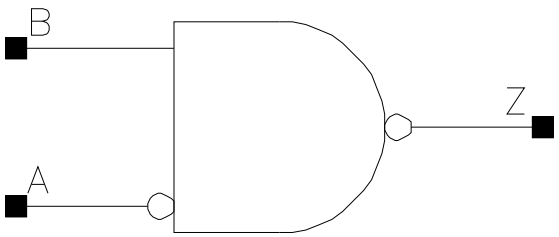
B to Z	1.107e-07	1.453e-07	1.193e-07	-2.263e-07
	C12T28SOI_LR_-NAND2X13_P10	C12T28SOI_LR_-NAND2X17_P10	C12T28SOI_LR_-NAND2X20_P10	C12T28SOI_LR_-NAND2X24_P10
A (output stable)	4.118e-07	3.168e-07	-2.060e-07	7.024e-07
B (output stable)	-2.429e-06	-2.252e-06	-2.303e-07	-4.565e-06
A to Z	-5.887e-07	6.970e-07	4.720e-07	1.040e-06
B to Z	-2.469e-07	-5.550e-07	3.890e-07	4.550e-07
	C12T28SOI_LR_-NAND2X27_P10	C12T28SOI_LR_-NAND2X42_P10	C12T28SOI_LR_-NAND2X47_P10	C12T28SOI_LR_-NAND2X50_P10
A (output stable)	5.692e-07	-1.870e-09	-1.120e-09	-1.180e-09
B (output stable)	-4.212e-06	-3.170e-08	-3.020e-08	-3.080e-08
A to Z	1.263e-06	-4.780e-07	-7.500e-07	-3.400e-07
B to Z	3.830e-07	-3.220e-07	-3.500e-07	-7.990e-07
	C12T28SOI_LR_-NAND2X58_P10	C12T28SOI_LR_-NAND2X67_P10	C12T28SOI_-LRBR0D8_-NAND2X7_P10	C12T28SOI_-LRBR0D8_-NAND2X14_P10
A (output stable)	-3.100e-10	7.000e-11	2.689e-08	1.897e-06
B (output stable)	-3.060e-08	-3.050e-08	5.700e-09	-9.379e-06
A to Z	-8.530e-07	-2.290e-07	1.651e-07	3.394e-07
B to Z	-8.020e-07	-3.620e-07	3.788e-07	6.413e-07
	C12T28SOI_LRS_-NAND2X40_P10	C12T28SOI_LRS_-NAND2X54_P10		
A (output stable)	6.396e-07	9.354e-07		
B (output stable)	-5.489e-06	-7.616e-06		
A to Z	1.691e-06	2.002e-06		
B to Z	7.280e-07	9.980e-07		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X7_P10	1.200	0.544	0.6528
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X40_P10	1.200	2.312	2.7744
X54_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P10	X7_P10	X13_P10	X27_P10
A	0.0008	0.0008	0.0011	0.0021
B	0.0006	0.0008	0.0015	0.0031
	X40_P10	X54_P10		
A	0.0031	0.0040		
B	0.0046	0.0062		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0355	0.0376	6.5052	3.5119
A to Z ↑	0.0263	0.0272	7.1680	3.7417
B to Z ↓	0.0140	0.0117	6.6808	3.5877
B to Z ↑	0.0191	0.0163	7.3826	3.8448
	X13_P10	**X27_P10**	**X13_P10**	**X27_P10**

A to Z ↓	0.0349	0.0340	1.8941	0.9418
A to Z ↑	0.0257	0.0251	1.9223	0.9302
B to Z ↓	0.0109	0.0110	1.9400	0.9668
B to Z ↑	0.0152	0.0149	1.9170	0.9453
	X40_P10	**X54_P10**	**X40_P10**	**X54_P10**
A to Z ↓	0.0347	0.0345	0.6305	0.4792
A to Z ↑	0.0258	0.0256	0.6200	0.4680
B to Z ↓	0.0111	0.0112	0.6460	0.4904
B to Z ↑	0.0149	0.0150	0.6352	0.4799

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P10	6.547e-08	1.772e-12
X7_P10	9.718e-08	1.772e-12
X13_P10	1.877e-07	2.529e-12
X27_P10	3.679e-07	3.788e-12
X40_P10	5.430e-07	5.049e-12
X54_P10	7.180e-07	6.309e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	1.049e-03	1.354e-03	2.228e-03	4.293e-03
B (output stable)	3.892e-05	7.248e-05	3.643e-04	6.382e-04
A to Z	1.795e-03	2.485e-03	4.503e-03	8.784e-03
B to Z	5.168e-04	7.192e-04	1.255e-03	2.497e-03
	X40_P10	X54_P10		
A (output stable)	6.685e-03	8.675e-03		
B (output stable)	9.369e-04	1.223e-03		
A to Z	1.340e-02	1.759e-02		
B to Z	3.678e-03	4.897e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

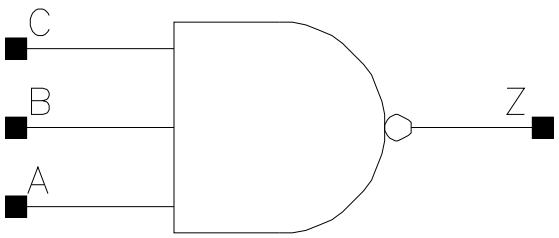
Pin Cycle (vdds)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	-1.759e-07	-1.960e-07	-3.486e-07	2.312e-06
B (output stable)	2.750e-08	-3.810e-08	-1.126e-07	-2.869e-06
A to Z	5.152e-08	-2.373e-07	-4.013e-07	-5.260e-07
B to Z	1.358e-07	4.297e-07	-2.711e-07	-6.570e-07
	X40_P10	X54_P10		
A (output stable)	3.545e-06	6.019e-06		
B (output stable)	-4.448e-06	-6.932e-06		
A to Z	-7.900e-08	-5.390e-07		
B to Z	2.800e-08	-1.690e-06		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P10	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P10	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P10	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P10	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P10	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P10	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P10	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P10	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P10	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P10	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P10	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P10	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P10	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P10	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P10	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P10	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A	0.0007	0.0009	0.0014	0.0017
B	0.0007	0.0009	0.0013	0.0016
C	0.0007	0.0008	0.0013	0.0016
	C12T28SOI_LR_-NAND3X15_P10	C12T28SOI_LR_-NAND3X18_P10	C12T28SOI_LR_-NAND3X21_P10	C12T28SOI_LR_-NAND3X24_P10
A	0.0022	0.0025	0.0030	0.0034
B	0.0021	0.0024	0.0029	0.0032
C	0.0020	0.0023	0.0028	0.0031
	C12T28SOI_LR_-NAND3X35_P10	C12T28SOI_LR_-NAND3X47_P10	C12T28SOI_-LRBR0P6_-NAND3X6_P10	C12T28SOI_-LRBR0P6_-NAND3X12_P10
A	0.0050	0.0067	0.0009	0.0017
B	0.0048	0.0064	0.0009	0.0016
C	0.0046	0.0062	0.0008	0.0015
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	C12T28SOI_-LRBR0P6_-NAND3X24_P10	C12T28SOI_-LRBR0P6_-NAND3X35_P10	C12T28SOI_-LRBR0P6_-NAND3X47_P10
A	0.0025	0.0033	0.0050	0.0066
B	0.0024	0.0032	0.0047	0.0063
C	0.0022	0.0030	0.0044	0.0060
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10			
A	0.0026			
B	0.0025			
C	0.0023			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10
A to Z ↓	0.0198	0.0181	6.9293	4.9476
A to Z ↑	0.0256	0.0235	5.3248	3.6676
B to Z ↓	0.0208	0.0186	6.9482	4.9629
B to Z ↑	0.0245	0.0221	5.3391	3.6775
C to Z ↓	0.0182	0.0163	6.9903	4.9934
C to Z ↑	0.0213	0.0192	5.3478	3.7046

	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A to Z ↓	0.0201	0.0189	3.3768	2.6263
A to Z ↑	0.0246	0.0232	2.4956	1.8762
B to Z ↓	0.0190	0.0180	3.3877	2.6349
B to Z ↑	0.0225	0.0212	2.5001	1.8797
C to Z ↓	0.0165	0.0156	3.4095	2.6521
C to Z ↑	0.0192	0.0180	2.4939	1.8665
	C12T28SOI_LR_-NAND3X15_P10	**C12T28SOI_LR_-NAND3X18_P10**	**C12T28SOI_LR_-NAND3X15_P10**	**C12T28SOI_LR_-NAND3X18_P10**
A to Z ↓	0.0184	0.0178	2.1210	1.8231
A to Z ↑	0.0229	0.0221	1.4955	1.2468
B to Z ↓	0.0181	0.0176	2.1294	1.8297
B to Z ↑	0.0209	0.0202	1.4997	1.2496
C to Z ↓	0.0160	0.0152	2.1428	1.8417
C to Z ↑	0.0180	0.0171	1.5123	1.2601
	C12T28SOI_LR_-NAND3X21_P10	**C12T28SOI_LR_-NAND3X24_P10**	**C12T28SOI_LR_-NAND3X21_P10**	**C12T28SOI_LR_-NAND3X24_P10**
A to Z ↓	0.0189	0.0185	1.5425	1.3786
A to Z ↑	0.0230	0.0226	1.0731	0.9430
B to Z ↓	0.0181	0.0179	1.5478	1.3817
B to Z ↑	0.0210	0.0206	1.0750	0.9448
C to Z ↓	0.0158	0.0155	1.5577	1.3910
C to Z ↑	0.0179	0.0175	1.0770	0.9461
	C12T28SOI_LR_-NAND3X35_P10	**C12T28SOI_LR_-NAND3X47_P10**	**C12T28SOI_LR_-NAND3X35_P10**	**C12T28SOI_LR_-NAND3X47_P10**
A to Z ↓	0.0178	0.0180	0.9408	0.7168
A to Z ↑	0.0220	0.0222	0.6312	0.4769
B to Z ↓	0.0175	0.0177	0.9450	0.7194
B to Z ↑	0.0200	0.0201	0.6316	0.4760
C to Z ↓	0.0152	0.0154	0.9514	0.7244
C to Z ↑	0.0170	0.0170	0.6359	0.4787
	C12T28SOI_-LRBR0P6_-NAND3X6_P10	**C12T28SOI_-LRBR0P6_-NAND3X12_P10**	**C12T28SOI_-LRBR0P6_-NAND3X6_P10**	**C12T28SOI_-LRBR0P6_-NAND3X12_P10**
A to Z ↓	0.0150	0.0157	3.3453	1.7707
A to Z ↑	0.0314	0.0313	5.8021	2.9613
B to Z ↓	0.0150	0.0143	3.3698	1.7836
B to Z ↑	0.0285	0.0271	5.8173	2.9671
C to Z ↓	0.0119	0.0109	3.4103	1.8087
C to Z ↑	0.0225	0.0205	5.8586	2.9739
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	**C12T28SOI_-LRBR0P6_-NAND3X24_P10**	**C12T28SOI_-LRBR0P6_-NAND3X18_P10**	**C12T28SOI_-LRBR0P6_-NAND3X24_P10**
A to Z ↓	0.0148	0.0153	1.2297	0.9279
A to Z ↑	0.0298	0.0304	1.9686	1.4869
B to Z ↓	0.0140	0.0140	1.2400	0.9360
B to Z ↑	0.0258	0.0262	1.9741	1.4902
C to Z ↓	0.0111	0.0109	1.2545	0.9476
C to Z ↑	0.0200	0.0199	1.9887	1.4922
	C12T28SOI_-LRBR0P6_-NAND3X35_P10	**C12T28SOI_-LRBR0P6_-NAND3X47_P10**	**C12T28SOI_-LRBR0P6_-NAND3X35_P10**	**C12T28SOI_-LRBR0P6_-NAND3X47_P10**

A to Z ↓	0.0149	0.0150	0.6360	0.4859
A to Z ↑	0.0302	0.0301	1.0214	0.7726
B to Z ↓	0.0139	0.0139	0.6410	0.4894
B to Z ↑	0.0259	0.0258	1.0227	0.7731
C to Z ↓	0.0107	0.0110	0.6495	0.4966
C to Z ↑	0.0194	0.0197	1.0339	0.7765
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P10**	
A to Z ↓	0.0155		1.1863	
A to Z ↑	0.0299		1.8561	
B to Z ↓	0.0139		1.1949	
B to Z ↑	0.0257		1.8598	
C to Z ↓	0.0103		1.2120	
C to Z ↑	0.0191		1.8480	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P10	6.318e-08	2.024e-12
C12T28SOI_LR_NAND3X6_P10	8.762e-08	2.024e-12
C12T28SOI_LR_NAND3X9_P10	1.299e-07	2.780e-12
C12T28SOI_LR_NAND3X12_P10	1.688e-07	2.780e-12
C12T28SOI_LR_NAND3X15_P10	2.071e-07	3.300e-12
C12T28SOI_LR_NAND3X18_P10	2.446e-07	3.284e-12
C12T28SOI_LR_NAND3X21_P10	2.917e-07	4.293e-12
C12T28SOI_LR_NAND3X24_P10	3.284e-07	4.293e-12
C12T28SOI_LR_NAND3X35_P10	4.896e-07	5.805e-12
C12T28SOI_LR_NAND3X47_P10	6.490e-07	7.318e-12
C12T28SOI_LRBR0P6_NAND3X6_-P10	9.722e-08	3.444e-12
C12T28SOI_LRBR0P6_NAND3X12_-P10	1.879e-07	4.260e-12
C12T28SOI_LRBR0P6_NAND3X18_-P10	2.708e-07	4.803e-12
C12T28SOI_LRBR0P6_NAND3X24_-P10	3.667e-07	5.892e-12
C12T28SOI_LRBR0P6_NAND3X35_-P10	5.484e-07	7.524e-12
C12T28SOI_LRBR0P6_NAND3X47_-P10	7.275e-07	9.154e-12
C12T28SOIDV_LRBR0P6_-NAND3X18_P10	2.923e-07	3.963e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A (output stable)	1.204e-05	1.708e-05	2.135e-05	2.894e-05
B (output stable)	4.920e-05	6.515e-05	1.115e-04	1.355e-04
C (output stable)	6.837e-05	7.796e-05	1.153e-04	1.303e-04
A to Z	1.480e-03	1.800e-03	2.969e-03	3.494e-03
B to Z	1.319e-03	1.556e-03	2.374e-03	2.793e-03
C to Z	9.898e-04	1.158e-03	1.700e-03	1.983e-03

	C12T28SOI_LR_-NAND3X15_P10	C12T28SOI_LR_-NAND3X18_P10	C12T28SOI_LR_-NAND3X21_P10	C12T28SOI_LR_-NAND3X24_P10
A (output stable)	2.984e-05	3.026e-05	4.835e-05	5.388e-05
B (output stable)	1.675e-04	1.847e-04	2.301e-04	2.524e-04
C (output stable)	1.336e-04	1.529e-04	2.128e-04	2.252e-04
A to Z	4.219e-03	4.667e-03	6.000e-03	6.545e-03
B to Z	3.380e-03	3.711e-03	4.786e-03	5.217e-03
C to Z	2.466e-03	2.603e-03	3.405e-03	3.679e-03
	C12T28SOI_LR_-NAND3X35_P10	C12T28SOI_LR_-NAND3X47_P10	C12T28SOI_-LRBR0P6_-NAND3X6_P10	C12T28SOI_-LRBR0P6_-NAND3X12_P10
A (output stable)	5.939e-05	8.131e-05	2.237e-05	3.864e-05
B (output stable)	3.463e-04	4.425e-04	9.446e-05	1.973e-04
C (output stable)	3.265e-04	4.131e-04	1.027e-04	1.844e-04
A to Z	9.198e-03	1.219e-02	1.952e-03	3.839e-03
B to Z	7.306e-03	9.736e-03	1.588e-03	2.819e-03
C to Z	5.022e-03	6.766e-03	1.004e-03	1.606e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	C12T28SOI_-LRBR0P6_-NAND3X24_P10	C12T28SOI_-LRBR0P6_-NAND3X35_P10	C12T28SOI_-LRBR0P6_-NAND3X47_P10
A (output stable)	4.118e-05	7.208e-05	7.631e-05	1.125e-04
B (output stable)	2.658e-04	3.670e-04	5.034e-04	6.871e-04
C (output stable)	1.975e-04	3.228e-04	4.760e-04	5.799e-04
A to Z	5.171e-03	7.166e-03	1.031e-02	1.343e-02
B to Z	3.787e-03	5.250e-03	7.493e-03	9.759e-03
C to Z	2.263e-03	2.989e-03	4.078e-03	5.428e-03
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10			
A (output stable)	4.865e-05			
B (output stable)	3.037e-04			
C (output stable)	2.679e-04			
A to Z	5.581e-03			
B to Z	4.062e-03			
C to Z	2.209e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P10	C12T28SOI_LR_-NAND3X6_P10	C12T28SOI_LR_-NAND3X9_P10	C12T28SOI_LR_-NAND3X12_P10
A (output stable)	4.550e-08	2.600e-08	8.695e-07	-4.897e-08
B (output stable)	3.274e-08	-1.585e-08	1.147e-06	-8.260e-08
C (output stable)	1.283e-08	-9.700e-09	-1.043e-06	-1.132e-07
A to Z	-6.980e-07	-8.610e-07	6.940e-07	5.240e-07
B to Z	-4.710e-07	-6.120e-07	-4.210e-07	7.800e-07
C to Z	1.920e-07	2.000e-07	1.890e-07	-8.760e-07
	C12T28SOI_LR_-NAND3X15_P10	C12T28SOI_LR_-NAND3X18_P10	C12T28SOI_LR_-NAND3X21_P10	C12T28SOI_LR_-NAND3X24_P10
A (output stable)	7.288e-07	6.542e-07	3.205e-06	1.277e-06
B (output stable)	7.785e-07	6.992e-07	1.002e-06	1.563e-06
C (output stable)	-9.777e-07	-9.767e-07	-1.998e-06	-1.865e-06
A to Z	6.680e-07	1.153e-06	2.474e-06	1.259e-06
B to Z	-8.900e-08	1.284e-06	-5.000e-09	1.776e-06

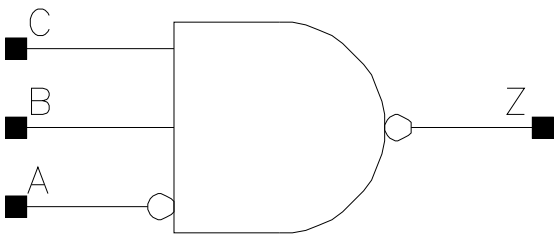
C to Z	-9.410e-07	1.410e-07	4.610e-07	5.620e-07
	C12T28SOI_LR_-NAND3X35_P10	C12T28SOI_LR_-NAND3X47_P10	C12T28SOI_-LRBR0P6_-NAND3X6_P10	C12T28SOI_-LRBR0P6_-NAND3X12_P10
A (output stable)	1.895e-06	2.264e-06	1.654e-06	5.696e-06
B (output stable)	2.261e-06	2.649e-06	2.269e-06	1.109e-06
C (output stable)	-2.818e-06	-3.487e-06	-2.028e-06	-2.507e-06
A to Z	1.927e-06	-7.022e-06	8.160e-07	1.188e-06
B to Z	2.431e-06	2.982e-06	-2.880e-07	-1.030e-06
C to Z	1.454e-06	-1.224e-06	1.079e-07	3.690e-07
	C12T28SOI_-LRBR0P6_-NAND3X18_P10	C12T28SOI_-LRBR0P6_-NAND3X24_P10	C12T28SOI_-LRBR0P6_-NAND3X35_P10	C12T28SOI_-LRBR0P6_-NAND3X47_P10
A (output stable)	-1.151e-07	6.691e-06	2.943e-06	9.588e-07
B (output stable)	-1.023e-07	1.662e-06	3.549e-06	9.664e-07
C (output stable)	-1.071e-07	-3.350e-06	-3.522e-06	-1.508e-06
A to Z	1.210e-07	1.223e-06	1.073e-06	4.650e-07
B to Z	-7.100e-07	5.100e-07	3.820e-07	1.190e-06
C to Z	-2.130e-07	1.148e-06	1.025e-06	-1.082e-06
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P10			
A (output stable)	-3.140e-08			
B (output stable)	-1.178e-07			
C (output stable)	-1.204e-07			
A to Z	6.400e-08			
B to Z	2.140e-07			
C to Z	5.500e-08			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.816	0.9792
X12_P10	1.200	1.224	1.4688
X18_P10	1.200	1.496	1.7952
X24_P10	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0008	0.0012	0.0011	0.0020
B	0.0008	0.0016	0.0024	0.0032
C	0.0008	0.0016	0.0023	0.0031

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X12_P10**	**X6_P10**	**X12_P10**
A to Z ↓	0.0419	0.0401	4.9695	2.6536
A to Z ↑	0.0294	0.0282	3.6363	1.8223
B to Z ↓	0.0166	0.0172	5.0068	2.6733
B to Z ↑	0.0204	0.0201	3.6892	1.8554
C to Z ↓	0.0159	0.0146	5.0383	2.6926
C to Z ↑	0.0183	0.0169	3.7132	1.8719
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0456	0.0390	1.8258	1.3810

A to Z ↑	0.0321	0.0269	1.2287	0.9201
B to Z ↓	0.0176	0.0172	1.8372	1.3913
B to Z ↑	0.0202	0.0199	1.2501	0.9397
C to Z ↓	0.0153	0.0146	1.8478	1.4010
C to Z ↑	0.0173	0.0167	1.2602	0.9473

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P10	1.103e-07	2.276e-12
X12_P10	2.171e-07	3.032e-12
X18_P10	2.904e-07	3.536e-12
X24_P10	4.302e-07	5.048e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	1.296e-03	2.272e-03	3.119e-03	4.195e-03
B (output stable)	2.686e-05	8.744e-05	1.435e-04	2.095e-04
C (output stable)	4.387e-05	1.812e-04	2.138e-04	3.553e-04
A to Z	3.029e-03	5.862e-03	8.462e-03	1.120e-02
B to Z	1.297e-03	2.507e-03	3.743e-03	4.844e-03
C to Z	1.023e-03	1.688e-03	2.630e-03	3.245e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

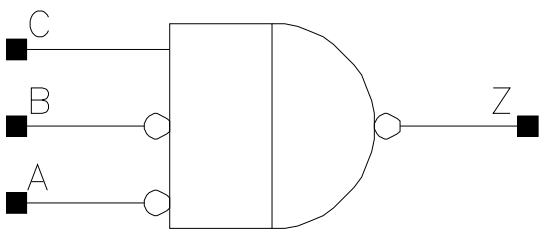
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	-2.220e-07	9.700e-09	-1.249e-07	2.482e-06
B (output stable)	-5.597e-09	1.003e-06	-1.990e-07	-9.773e-08
C (output stable)	-3.433e-08	-1.100e-06	-2.164e-07	-1.932e-06
A to Z	-2.183e-07	5.080e-07	-3.900e-08	5.970e-07
B to Z	5.400e-07	-1.280e-07	1.094e-06	1.610e-06
C to Z	1.590e-07	1.660e-07	2.620e-07	-2.346e-06

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	0.816	0.9792
X13_P10	1.200	1.088	1.3056
X20_P10	1.200	1.632	1.9584
X27_P10	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P10	X13_P10	X20_P10	X27_P10
A	0.0010	0.0010	0.0020	0.0018
B	0.0011	0.0011	0.0021	0.0019
C	0.0008	0.0016	0.0023	0.0031

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	**X13_P10**	**X7_P10**	**X13_P10**
A to Z ↓	0.0422	0.0511	3.3690	1.8046
A to Z ↑	0.0249	0.0282	3.6078	1.8131
B to Z ↓	0.0413	0.0506	3.3705	1.8093
B to Z ↑	0.0236	0.0270	3.6045	1.8115
C to Z ↓	0.0116	0.0108	3.4420	1.8355
C to Z ↑	0.0162	0.0150	3.7003	1.8685
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0465	0.0511	1.2311	0.9392
A to Z ↑	0.0264	0.0312	1.2230	0.9177
B to Z ↓	0.0433	0.0490	1.2334	0.9393

B to Z ↑	0.0245	0.0298	1.2213	0.9171
C to Z ↓	0.0120	0.0116	1.2554	0.9540
C to Z ↑	0.0161	0.0156	1.2592	0.9466

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X7_P10	1.385e-07	2.276e-12
X13_P10	1.932e-07	2.780e-12
X20_P10	3.180e-07	3.790e-12
X27_P10	3.513e-07	4.293e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	7.569e-04	1.051e-03	1.732e-03	2.057e-03
B (output stable)	5.913e-04	8.478e-04	1.228e-03	1.590e-03
C (output stable)	3.672e-05	1.462e-04	1.602e-04	1.907e-04
A to Z	3.322e-03	5.384e-03	8.628e-03	1.066e-02
B to Z	2.941e-03	5.019e-03	7.464e-03	9.690e-03
C to Z	7.432e-04	1.241e-03	2.173e-03	2.802e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

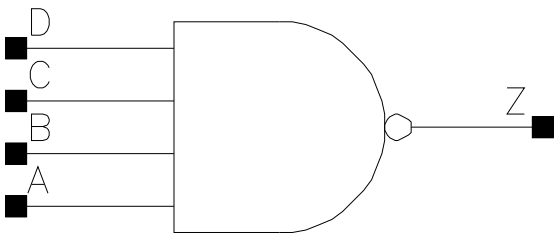
Pin Cycle (vdds)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	-4.410e-06	-4.579e-06	-1.443e-05	-1.388e-05
B (output stable)	9.693e-08	-2.533e-09	7.130e-08	7.147e-08
C (output stable)	-1.797e-08	-1.017e-07	-1.665e-07	-2.967e-07
A to Z	-4.329e-06	-4.927e-06	-1.534e-05	-1.515e-05
B to Z	-1.018e-07	-4.548e-07	-1.910e-07	-3.600e-07
C to Z	1.380e-07	3.938e-07	4.980e-07	5.760e-07

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0007	0.0006	0.0008	0.0010
B	0.0007	0.0007	0.0009	0.0011
C	0.0007	0.0007	0.0009	0.0011
D	0.0007	0.0007	0.0009	0.0011

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0635	0.0627	2.0297	1.0149
A to Z ↑	0.0498	0.0538	3.6777	1.8277
B to Z ↓	0.0648	0.0649	2.0324	1.0140
B to Z ↑	0.0480	0.0530	3.6811	1.8281
C to Z ↓	0.0634	0.0610	2.0301	1.0148
C to Z ↑	0.0512	0.0559	3.6745	1.8249

D to Z ↓	0.0650	0.0623	2.0324	1.0149
D to Z ↑	0.0500	0.0539	3.6792	1.8286
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0653	0.0601	0.7022	0.5248
A to Z ↑	0.0520	0.0506	1.2333	0.9244
B to Z ↓	0.0666	0.0611	0.7025	0.5247
B to Z ↑	0.0506	0.0490	1.2322	0.9242
C to Z ↓	0.0594	0.0549	0.7025	0.5253
C to Z ↑	0.0527	0.0511	1.2313	0.9226
D to Z ↓	0.0609	0.0563	0.7024	0.5253
D to Z ↑	0.0508	0.0493	1.2318	0.9235

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.695e-07	3.033e-12
X17_P10	2.383e-07	3.536e-12
X25_P10	3.651e-07	4.292e-12
X33_P10	4.414e-07	4.545e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	5.391e-04	6.883e-04	1.019e-03	1.199e-03
B (output stable)	4.834e-04	6.358e-04	9.220e-04	1.066e-03
C (output stable)	5.290e-04	6.461e-04	9.768e-04	1.108e-03
D (output stable)	4.782e-04	5.805e-04	8.284e-04	9.315e-04
A to Z	3.901e-03	5.883e-03	9.103e-03	1.102e-02
B to Z	3.762e-03	5.762e-03	8.900e-03	1.075e-02
C to Z	3.995e-03	5.778e-03	8.491e-03	1.025e-02
D to Z	3.866e-03	5.629e-03	8.282e-03	9.984e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

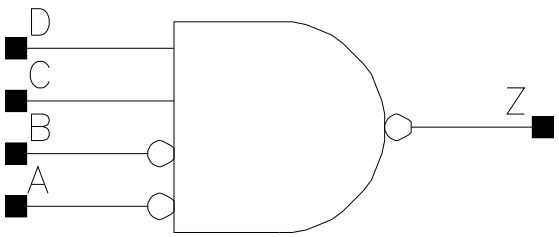
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	-5.017e-06	-9.635e-06	-2.546e-05	-3.126e-05
B (output stable)	-4.359e-06	-7.146e-06	-1.996e-05	-2.306e-05
C (output stable)	5.050e-06	1.026e-05	2.697e-05	3.307e-05
D (output stable)	4.829e-08	8.533e-08	1.245e-07	1.838e-07
A to Z	-2.044e-06	-3.786e-06	-8.932e-06	-1.109e-05
B to Z	-2.077e-06	-3.751e-06	-8.981e-06	-1.134e-05
C to Z	-2.045e-07	-2.440e-07	-6.630e-07	-7.080e-07
D to Z	-7.010e-08	-2.034e-07	-2.810e-07	-4.320e-07

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X12_P10	1.200	1.496	1.7952
X18_P10	1.200	2.040	2.4480
X24_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0010	0.0011	0.0020	0.0018
B	0.0011	0.0014	0.0021	0.0019
C	0.0008	0.0016	0.0024	0.0032
D	0.0008	0.0016	0.0023	0.0032

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X12_P10	X6_P10	X12_P10
A to Z ↓	0.0442	0.0587	5.1329	2.6647
A to Z ↑	0.0265	0.0316	3.6053	1.8149
B to Z ↓	0.0426	0.0574	5.1336	2.6637
B to Z ↑	0.0244	0.0302	3.6032	1.8137
C to Z ↓	0.0167	0.0173	5.1664	2.6721
C to Z ↑	0.0206	0.0202	3.9147	1.8550

D to Z ↓	0.0157	0.0145	5.1964	2.6906
D to Z ↑	0.0183	0.0168	3.9401	1.8715
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0505	0.0567	1.8204	1.3855
A to Z ↑	0.0280	0.0353	1.2238	0.9192
B to Z ↓	0.0475	0.0545	1.8218	1.3852
B to Z ↑	0.0262	0.0337	1.2226	0.9182
C to Z ↓	0.0171	0.0177	1.8304	1.3897
C to Z ↑	0.0199	0.0203	1.2553	0.9383
D to Z ↓	0.0151	0.0154	1.8423	1.3991
D to Z ↑	0.0171	0.0171	1.2842	0.9470

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P10	1.414e-07	2.528e-12
X12_P10	2.158e-07	3.538e-12
X18_P10	3.492e-07	4.545e-12
X24_P10	3.868e-07	5.302e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	8.473e-04	1.409e-03	2.105e-03	2.569e-03
B (output stable)	6.579e-04	1.178e-03	1.599e-03	2.124e-03
C (output stable)	4.949e-05	1.206e-04	1.891e-04	2.579e-04
D (output stable)	3.415e-05	1.313e-04	1.456e-04	2.208e-04
A to Z	3.575e-03	6.747e-03	9.888e-03	1.305e-02
B to Z	3.199e-03	6.254e-03	8.814e-03	1.208e-02
C to Z	1.261e-03	2.520e-03	3.606e-03	5.080e-03
D to Z	9.778e-04	1.677e-03	2.588e-03	3.525e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

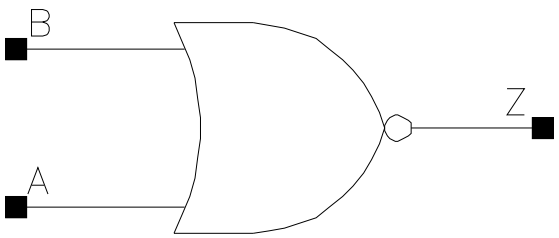
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	-4.290e-06	-8.607e-06	-1.413e-05	-1.377e-05
B (output stable)	1.556e-07	4.895e-07	4.826e-07	9.931e-07
C (output stable)	-5.290e-09	6.227e-07	3.955e-07	1.076e-06
D (output stable)	-1.523e-08	-1.045e-06	-1.084e-06	-2.267e-06
A to Z	-3.503e-06	-8.503e-06	-1.277e-05	-1.241e-05
B to Z	2.128e-07	-6.400e-08	-5.000e-08	1.270e-07
C to Z	5.260e-07	1.043e-06	1.346e-06	2.276e-06
D to Z	1.170e-07	2.440e-07	1.200e-07	1.380e-07

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.408	0.4896
X5_P10	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X10_P10	1.200	0.680	0.8160
X14_P10	1.200	0.680	0.8160
X17_P10	1.200	0.952	1.1424
X21_P10	1.200	0.952	1.1424
X24_P10	1.200	1.224	1.4688
X27_P10	1.200	1.224	1.4688
X34_P10	1.200	1.496	1.7952
X40_P10	1.200	1.360	1.6320
X41_P10	1.200	1.768	2.1216
X49_P10	1.200	1.496	1.7952
X53_P10	1.200	1.904	2.2848
X55_P10	1.200	2.312	2.7744
X57_P10	1.200	1.904	2.2848
X65_P10	1.200	2.040	2.4480
X84_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P10	X5_P10	X7_P10	X10_P10
A	0.0006	0.0007	0.0009	0.0014
B	0.0006	0.0007	0.0009	0.0013
	X14_P10	X17_P10	X21_P10	X24_P10

A	0.0018	0.0022	0.0026	0.0030
B	0.0016	0.0020	0.0024	0.0029
	X27_P10	X34_P10	X40_P10	X41_P10
A	0.0034	0.0043	0.0010	0.0052
B	0.0032	0.0039	0.0011	0.0048
	X49_P10	X53_P10	X55_P10	X57_P10
A	0.0010	0.0010	0.0069	0.0010
B	0.0011	0.0009	0.0063	0.0009
	X65_P10	X84_P10		
A	0.0010	0.0012		
B	0.0010	0.0010		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X5_P10**	**X3_P10**	**X5_P10**
A to Z ↓	0.0122	0.0114	3.8296	2.7850
A to Z ↑	0.0251	0.0234	15.3284	11.1547
B to Z ↓	0.0109	0.0099	3.9267	2.8100
B to Z ↑	0.0237	0.0215	15.4106	11.1974
	X7_P10	**X10_P10**	**X7_P10**	**X10_P10**
A to Z ↓	0.0111	0.0116	2.0507	1.3318
A to Z ↑	0.0223	0.0248	7.8786	5.2544
B to Z ↓	0.0095	0.0089	2.0774	1.3479
B to Z ↑	0.0201	0.0190	7.9129	5.2836
	X14_P10	**X17_P10**	**X14_P10**	**X17_P10**
A to Z ↓	0.0113	0.0115	1.0150	0.8156
A to Z ↑	0.0236	0.0237	3.8978	3.1469
B to Z ↓	0.0086	0.0093	1.0281	0.8244
B to Z ↑	0.0180	0.0193	3.9206	3.1618
	X21_P10	**X24_P10**	**X21_P10**	**X24_P10**
A to Z ↓	0.0114	0.0113	0.6962	0.5935
A to Z ↑	0.0231	0.0234	2.6198	2.2828
B to Z ↓	0.0093	0.0089	0.7041	0.6006
B to Z ↑	0.0189	0.0186	2.6346	2.2949
	X27_P10	**X34_P10**	**X27_P10**	**X34_P10**
A to Z ↓	0.0111	0.0116	0.5269	0.4262
A to Z ↑	0.0226	0.0231	2.0086	1.5997
B to Z ↓	0.0087	0.0092	0.5338	0.4313
B to Z ↑	0.0179	0.0188	2.0205	1.6083
	X40_P10	**X41_P10**	**X40_P10**	**X41_P10**
A to Z ↓	0.0399	0.0113	0.4262	0.3550
A to Z ↑	0.0614	0.0227	0.7585	1.3255
B to Z ↓	0.0385	0.0088	0.4262	0.3598
B to Z ↑	0.0609	0.0178	0.7585	1.3329
	X49_P10	**X53_P10**	**X49_P10**	**X53_P10**
A to Z ↓	0.0420	0.0428	0.3547	0.3247
A to Z ↑	0.0635	0.0722	0.6302	0.5822
B to Z ↓	0.0407	0.0415	0.3545	0.3244
B to Z ↑	0.0632	0.0712	0.6298	0.5827
	X55_P10	**X57_P10**	**X55_P10**	**X57_P10**
A to Z ↓	0.0114	0.0432	0.2685	0.3051
A to Z ↑	0.0227	0.0724	0.9986	0.5415

B to Z ↓	0.0089	0.0418	0.2727	0.3052
B to Z ↑	0.0179	0.0714	1.0043	0.5421
	X65_P10	**X84_P10**	**X65_P10**	**X84_P10**
A to Z ↓	0.0445	0.0466	0.2682	0.2139
A to Z ↑	0.0734	0.0740	0.4746	0.3763
B to Z ↓	0.0431	0.0452	0.2680	0.2138
B to Z ↑	0.0725	0.0733	0.4746	0.3761

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P10	4.312e-08	1.520e-12
X5_P10	5.709e-08	1.520e-12
X7_P10	7.605e-08	1.520e-12
X10_P10	1.157e-07	2.022e-12
X14_P10	1.490e-07	2.022e-12
X17_P10	1.873e-07	2.527e-12
X21_P10	2.190e-07	2.526e-12
X24_P10	2.581e-07	3.029e-12
X27_P10	2.891e-07	3.029e-12
X34_P10	3.592e-07	3.533e-12
X40_P10	3.848e-07	3.285e-12
X41_P10	4.293e-07	4.037e-12
X49_P10	4.296e-07	3.536e-12
X53_P10	5.072e-07	4.289e-12
X55_P10	5.695e-07	5.044e-12
X57_P10	5.263e-07	4.289e-12
X65_P10	5.711e-07	4.543e-12
X84_P10	6.765e-07	5.050e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	2.527e-05	3.461e-05	4.838e-05	1.030e-04
B (output stable)	1.173e-06	2.208e-06	4.197e-06	3.349e-05
A to Z	6.821e-04	8.245e-04	1.080e-03	1.915e-03
B to Z	4.810e-04	5.505e-04	6.896e-04	9.540e-04
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	1.302e-04	1.671e-04	1.934e-04	2.235e-04
B (output stable)	4.526e-05	4.621e-05	4.638e-05	5.345e-05
A to Z	2.353e-03	2.969e-03	3.398e-03	4.018e-03
B to Z	1.169e-03	1.660e-03	1.880e-03	2.128e-03
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	2.436e-04	3.243e-04	4.907e-05	3.879e-04
B (output stable)	5.903e-05	6.205e-05	4.397e-06	9.866e-05
A to Z	4.289e-03	5.583e-03	1.087e-02	6.543e-03
B to Z	2.235e-03	3.101e-03	1.051e-02	3.341e-03
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	4.921e-05	5.066e-05	5.247e-04	5.064e-05
B (output stable)	4.377e-06	4.588e-06	1.198e-04	4.589e-06
A to Z	1.217e-02	1.502e-02	8.650e-03	1.544e-02
B to Z	1.181e-02	1.463e-02	4.437e-03	1.504e-02
	X65_P10	X84_P10		

A (output stable)	5.074e-05	5.113e-05		
B (output stable)	4.690e-06	5.362e-06		
A to Z	1.660e-02	1.944e-02		
B to Z	1.621e-02	1.897e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

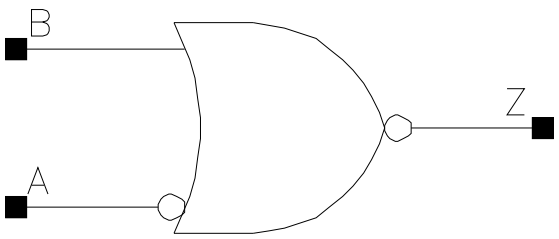
Pin Cycle (vdds)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	-2.389e-06	-3.180e-06	-4.395e-06	-1.190e-05
B (output stable)	3.239e-06	7.290e-06	1.395e-05	4.551e-05
A to Z	-2.594e-06	-3.474e-06	-4.884e-06	-1.509e-05
B to Z	-1.422e-07	1.118e-07	2.757e-07	6.600e-08
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	-1.500e-05	-1.207e-05	-1.338e-05	-2.222e-05
B (output stable)	6.862e-05	4.401e-05	4.945e-05	8.169e-05
A to Z	-1.844e-05	-1.455e-05	-1.590e-05	-2.546e-05
B to Z	7.220e-08	-2.081e-07	2.610e-07	-3.730e-07
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	-2.175e-05	-2.251e-05	-4.380e-06	-3.204e-05
B (output stable)	8.342e-05	8.309e-05	1.380e-05	1.217e-04
A to Z	-2.444e-05	-2.567e-05	-5.537e-06	-3.570e-05
B to Z	2.601e-07	3.250e-07	-5.380e-07	2.130e-07
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	-4.379e-06	-4.400e-06	-4.070e-05	-4.400e-06
B (output stable)	1.369e-05	1.535e-05	1.501e-04	1.535e-05
A to Z	-5.393e-06	-5.630e-06	-4.474e-05	-5.849e-06
B to Z	-8.870e-07	-7.720e-07	2.900e-08	-7.680e-07
	X65_P10	X84_P10		
A (output stable)	-4.399e-06	-4.543e-06		
B (output stable)	1.535e-05	1.577e-05		
A to Z	-5.425e-06	-5.804e-06		
B to Z	-5.110e-07	-1.003e-06		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X7_P10	1.200	0.680	0.8160
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X41_P10	1.200	2.312	2.7744
X55_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X7_P10	X13_P10
A	0.0008	0.0008	0.0008	0.0011
B	0.0006	0.0009	0.0008	0.0016
	X27_P10	X41_P10	X55_P10	
A	0.0021	0.0031	0.0040	
B	0.0032	0.0047	0.0064	

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0336	0.0368	3.6799	2.4202
A to Z ↑	0.0309	0.0307	15.2131	7.8366
B to Z ↓	0.0112	0.0107	3.8980	2.5847
B to Z ↑	0.0240	0.0201	15.3838	7.9329

	X7_P10	X13_P10	X7_P10	X13_P10
A to Z ↓	0.0372	0.0338	1.9287	1.0529
A to Z ↑	0.0333	0.0315	7.7591	4.1074
B to Z ↓	0.0098	0.0090	1.9864	1.0805
B to Z ↑	0.0212	0.0193	7.8220	4.1497
	X27_P10	**X41_P10**	**X27_P10**	**X41_P10**
A to Z ↓	0.0329	0.0333	0.5045	0.3420
A to Z ↑	0.0303	0.0302	1.9697	1.3210
B to Z ↓	0.0089	0.0088	0.5358	0.3620
B to Z ↑	0.0186	0.0180	1.9903	1.3348
	X55_P10		**X55_P10**	
A to Z ↓	0.0329		0.2589	
A to Z ↑	0.0300		0.9962	
B to Z ↓	0.0089		0.2743	
B to Z ↑	0.0181		1.0066	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P10	6.859e-08	1.772e-12
X6_P10	9.332e-08	1.770e-12
X7_P10	1.085e-07	2.022e-12
X13_P10	1.972e-07	2.527e-12
X27_P10	3.875e-07	3.789e-12
X41_P10	5.717e-07	5.049e-12
X55_P10	7.557e-07	6.308e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	1.024e-03	1.298e-03	1.367e-03	2.176e-03
B (output stable)	2.639e-07	3.500e-07	4.212e-07	7.772e-07
A to Z	1.793e-03	2.479e-03	2.875e-03	4.808e-03
B to Z	4.953e-04	6.871e-04	8.179e-04	1.297e-03
	X27_P10	X41_P10	X55_P10	
A (output stable)	4.269e-03	6.456e-03	8.431e-03	
B (output stable)	1.447e-06	2.312e-06	2.808e-06	
A to Z	9.545e-03	1.393e-02	1.838e-02	
B to Z	2.483e-03	3.473e-03	4.629e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

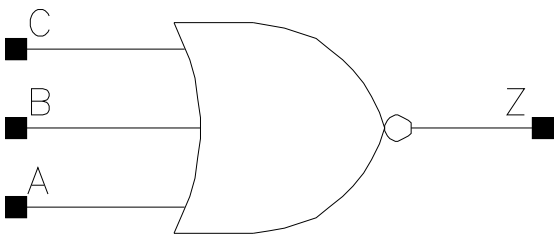
Pin Cycle (vdds)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	-2.309e-06	-4.161e-06	-8.190e-06	-1.336e-05
B (output stable)	1.531e-07	1.780e-07	2.606e-07	3.593e-07
A to Z	-2.635e-06	-4.764e-06	-1.029e-05	-1.754e-05
B to Z	1.960e-08	2.715e-07	1.719e-07	-2.616e-07
	X27_P10	X41_P10	X55_P10	
A (output stable)	-2.332e-05	-2.865e-05	-3.791e-05	
B (output stable)	4.230e-07	6.850e-07	6.570e-07	
A to Z	-3.032e-05	-3.789e-05	-4.908e-05	
B to Z	2.090e-07	2.300e-07	2.810e-07	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X9_P10	1.200	0.952	1.1424
X13_P10	1.200	0.952	1.1424
X16_P10	1.200	1.360	1.6320
X19_P10	1.200	1.496	1.7952
X22_P10	1.200	1.768	2.1216
X25_P10	1.200	1.904	2.2848
X37_P10	1.200	2.584	3.1008
X49_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P10	X6_P10	X9_P10	X13_P10
A	0.0007	0.0009	0.0013	0.0016
B	0.0007	0.0008	0.0015	0.0018
C	0.0007	0.0009	0.0013	0.0016
	X16_P10	X19_P10	X22_P10	X25_P10
A	0.0022	0.0026	0.0030	0.0034
B	0.0023	0.0029	0.0032	0.0040
C	0.0020	0.0023	0.0028	0.0031
	X37_P10	X49_P10		
A	0.0051	0.0068		
B	0.0052	0.0070		

C	0.0045	0.0063		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0136	0.0130	2.8265	2.0835
A to Z ↑	0.0348	0.0323	17.0494	12.0583
B to Z ↓	0.0130	0.0123	2.8297	2.0853
B to Z ↑	0.0330	0.0304	17.0889	12.0552
C to Z ↓	0.0116	0.0107	2.8554	2.1099
C to Z ↑	0.0290	0.0259	17.1034	12.0906
	X9_P10	**X13_P10**	**X9_P10**	**X13_P10**
A to Z ↓	0.0133	0.0131	1.3787	1.0625
A to Z ↑	0.0348	0.0330	7.9968	5.9640
B to Z ↓	0.0127	0.0121	1.3399	1.0152
B to Z ↑	0.0347	0.0321	8.0131	5.9704
C to Z ↓	0.0102	0.0097	1.3521	1.0334
C to Z ↑	0.0241	0.0225	8.0217	5.9861
	X16_P10	**X19_P10**	**X16_P10**	**X19_P10**
A to Z ↓	0.0133	0.0130	0.8230	0.6960
A to Z ↑	0.0338	0.0333	4.8223	3.9913
B to Z ↓	0.0129	0.0125	0.8245	0.6798
B to Z ↑	0.0329	0.0332	4.8200	3.9931
C to Z ↓	0.0105	0.0102	0.8295	0.7100
C to Z ↑	0.0251	0.0237	4.8335	4.0049
	X22_P10	**X25_P10**	**X22_P10**	**X25_P10**
A to Z ↓	0.0131	0.0130	0.6068	0.5313
A to Z ↑	0.0332	0.0331	3.4384	2.9991
B to Z ↓	0.0124	0.0123	0.5954	0.5099
B to Z ↑	0.0323	0.0330	3.4417	3.0020
C to Z ↓	0.0098	0.0097	0.6021	0.5316
C to Z ↑	0.0230	0.0224	3.4518	3.0108
	X37_P10	**X49_P10**	**X37_P10**	**X49_P10**
A to Z ↓	0.0130	0.0132	0.3653	0.2773
A to Z ↑	0.0323	0.0325	2.0096	1.5121
B to Z ↓	0.0123	0.0125	0.3608	0.2742
B to Z ↑	0.0311	0.0312	2.0104	1.5138
C to Z ↓	0.0101	0.0103	0.3660	0.2779
C to Z ↑	0.0224	0.0230	2.0168	1.5184

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	7.107e-08	1.771e-12
X6_P10	9.470e-08	1.772e-12
X9_P10	1.462e-07	2.527e-12
X13_P10	1.884e-07	2.530e-12
X16_P10	2.378e-07	3.283e-12
X19_P10	2.852e-07	3.535e-12
X22_P10	3.296e-07	4.061e-12
X25_P10	3.769e-07	4.325e-12
X37_P10	5.456e-07	5.555e-12

X49_P10	7.254e-07	7.075e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	1.501e-04	2.123e-04	4.240e-04	5.422e-04
B (output stable)	1.419e-05	1.924e-05	1.699e-04	1.867e-04
C (output stable)	2.337e-06	3.036e-06	2.446e-05	2.549e-05
A to Z	1.274e-03	1.617e-03	2.692e-03	3.329e-03
B to Z	1.021e-03	1.265e-03	2.246e-03	2.680e-03
C to Z	7.446e-04	8.683e-04	1.222e-03	1.448e-03
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	6.246e-04	7.874e-04	9.236e-04	1.091e-03
B (output stable)	1.736e-04	2.482e-04	3.001e-04	3.778e-04
C (output stable)	2.579e-05	3.119e-05	4.005e-05	4.419e-05
A to Z	4.284e-03	5.065e-03	5.836e-03	6.679e-03
B to Z	3.480e-03	4.175e-03	4.718e-03	5.491e-03
C to Z	2.138e-03	2.364e-03	2.604e-03	2.858e-03
	X37_P10	X49_P10		
A (output stable)	1.533e-03	2.012e-03		
B (output stable)	4.389e-04	5.347e-04		
C (output stable)	6.523e-05	7.994e-05		
A to Z	9.635e-03	1.288e-02		
B to Z	7.648e-03	1.020e-02		
C to Z	4.174e-03	5.735e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

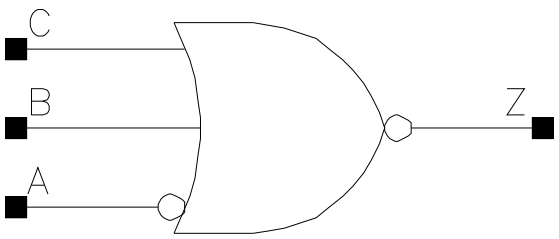
Pin Cycle (vdds)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	-2.391e-05	-3.366e-05	-6.991e-05	-8.996e-05
B (output stable)	6.638e-06	9.293e-06	-2.096e-06	-3.727e-07
C (output stable)	1.054e-05	1.462e-05	5.222e-05	6.379e-05
A to Z	-6.619e-06	-9.304e-06	-2.097e-05	-2.616e-05
B to Z	-3.107e-06	-4.780e-06	-1.731e-05	-1.970e-05
C to Z	-1.970e-07	-2.997e-07	-2.128e-07	-4.775e-07
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	-8.738e-05	-1.156e-04	-1.395e-04	-1.693e-04
B (output stable)	1.684e-05	2.446e-05	1.481e-05	2.647e-05
C (output stable)	4.706e-05	6.643e-05	8.655e-05	1.050e-04
A to Z	-2.473e-05	-3.229e-05	-4.139e-05	-4.944e-05
B to Z	-1.450e-05	-2.178e-05	-2.785e-05	-3.563e-05
C to Z	-5.822e-07	-2.680e-07	-4.638e-07	-5.349e-07
	X37_P10	X49_P10		
A (output stable)	-2.292e-04	-2.844e-04		
B (output stable)	3.293e-05	5.544e-05		
C (output stable)	1.325e-04	1.504e-04		
A to Z	-6.617e-05	-8.300e-05		
B to Z	-4.568e-05	-5.149e-05		
C to Z	-1.260e-07	-5.020e-07		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.680	0.8160
X13_P10	1.200	1.224	1.4688
X19_P10	1.200	1.496	1.7952
X25_P10	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0008	0.0011	0.0011	0.0021
B	0.0009	0.0018	0.0025	0.0035
C	0.0009	0.0016	0.0023	0.0031

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X13_P10**	**X6_P10**	**X13_P10**
A to Z ↓	0.0371	0.0353	2.0142	1.1318
A to Z ↑	0.0414	0.0407	12.1982	5.9583
B to Z ↓	0.0125	0.0121	2.0960	1.0214
B to Z ↑	0.0307	0.0318	12.2033	5.9704
C to Z ↓	0.0108	0.0096	2.1127	1.0347
C to Z ↑	0.0264	0.0223	12.2376	5.9865
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0402	0.0351	0.6859	0.5206

A to Z ↑	0.0436	0.0402	4.0046	3.0042
B to Z ↓	0.0126	0.0123	0.7115	0.5305
B to Z ↑	0.0311	0.0310	4.0179	3.0114
C to Z ↓	0.0102	0.0098	0.7110	0.5350
C to Z ↑	0.0238	0.0226	4.0267	3.0204

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P10	1.207e-07	2.025e-12
X13_P10	2.407e-07	3.033e-12
X19_P10	3.255e-07	3.548e-12
X25_P10	4.704e-07	4.799e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	1.543e-03	2.898e-03	3.897e-03	5.634e-03
B (output stable)	2.016e-06	3.461e-05	3.643e-05	5.778e-05
C (output stable)	1.196e-06	3.055e-05	1.906e-05	4.047e-05
A to Z	3.071e-03	6.010e-03	8.349e-03	1.153e-02
B to Z	1.276e-03	2.661e-03	3.866e-03	5.103e-03
C to Z	8.891e-04	1.420e-03	2.349e-03	2.863e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

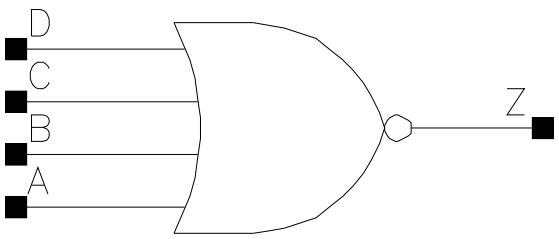
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	-4.401e-05	-1.180e-04	-1.458e-04	-2.159e-04
B (output stable)	1.566e-05	3.574e-05	5.782e-05	7.588e-05
C (output stable)	8.325e-06	3.574e-05	3.262e-05	5.638e-05
A to Z	-7.398e-06	-1.955e-05	-2.414e-05	-3.552e-05
B to Z	-3.800e-06	-1.206e-05	-1.359e-05	-2.092e-05
C to Z	1.474e-07	-2.639e-07	-1.740e-07	-5.797e-07

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	1.904	2.2848
X32_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X32_P10
A	0.0007	0.0007	0.0008	0.0009
B	0.0007	0.0007	0.0009	0.0012
C	0.0006	0.0006	0.0008	0.0010
D	0.0007	0.0006	0.0008	0.0009

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0420	0.0413	1.9739	0.9722
A to Z ↑	0.0669	0.0719	3.7438	1.8464
B to Z ↓	0.0406	0.0403	1.9754	0.9712
B to Z ↑	0.0659	0.0713	3.7468	1.8478
C to Z ↓	0.0412	0.0412	1.9746	0.9702
C to Z ↑	0.0676	0.0738	3.7410	1.8475

D to Z ↓	0.0407	0.0407	1.9737	0.9706
D to Z ↑	0.0673	0.0738	3.7412	1.8468
	X25_P10	**X32_P10**	**X25_P10**	**X32_P10**
A to Z ↓	0.0424	0.0446	0.6788	0.5337
A to Z ↑	0.0710	0.0689	1.2638	0.9587
B to Z ↓	0.0414	0.0435	0.6789	0.5341
B to Z ↑	0.0707	0.0683	1.2651	0.9592
C to Z ↓	0.0406	0.0432	0.6765	0.5326
C to Z ↑	0.0701	0.0689	1.2649	0.9579
D to Z ↓	0.0394	0.0413	0.6765	0.5318
D to Z ↑	0.0695	0.0680	1.2648	0.9590

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.645e-07	3.032e-12
X17_P10	2.409e-07	3.285e-12
X25_P10	3.532e-07	4.292e-12
X32_P10	4.292e-07	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	5.449e-04	6.715e-04	9.224e-04	1.176e-03
B (output stable)	4.470e-04	5.786e-04	8.111e-04	1.019e-03
C (output stable)	5.295e-04	6.343e-04	9.391e-04	1.206e-03
D (output stable)	4.144e-04	5.257e-04	7.763e-04	9.863e-04
A to Z	3.769e-03	5.647e-03	8.628e-03	1.081e-02
B to Z	3.562e-03	5.460e-03	8.347e-03	1.048e-02
C to Z	3.817e-03	5.622e-03	8.091e-03	1.015e-02
D to Z	3.605e-03	5.431e-03	7.824e-03	9.786e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

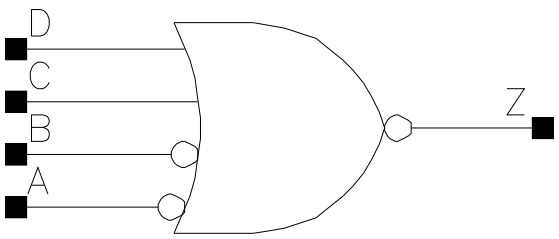
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	-2.283e-06	-2.183e-06	-3.092e-06	-4.097e-06
B (output stable)	-2.464e-08	4.789e-08	-2.486e-09	1.237e-08
C (output stable)	-6.679e-06	-6.531e-06	-9.603e-06	-1.262e-05
D (output stable)	3.625e-06	3.427e-06	5.099e-06	6.610e-06
A to Z	-2.511e-06	-2.561e-06	-3.607e-06	-4.861e-06
B to Z	-2.423e-07	-2.348e-07	-3.180e-07	-2.234e-07
C to Z	-2.528e-06	-2.332e-06	-3.936e-06	-4.828e-06
D to Z	-2.350e-07	-6.990e-08	-6.468e-07	-4.752e-07

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X13_P10	1.200	1.496	1.7952
X19_P10	1.200	2.040	2.4480
X25_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0011	0.0011	0.0020	0.0020
B	0.0011	0.0015	0.0021	0.0021
C	0.0009	0.0017	0.0025	0.0033
D	0.0008	0.0016	0.0023	0.0031

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X13_P10	X6_P10	X13_P10
A to Z ↓	0.0323	0.0396	1.9656	0.9821
A to Z ↑	0.0414	0.0500	11.7280	6.0458
B to Z ↓	0.0302	0.0382	1.9646	0.9815
B to Z ↑	0.0415	0.0507	11.7417	6.0416
C to Z ↓	0.0130	0.0121	2.1365	1.0195
C to Z ↑	0.0310	0.0316	11.7682	6.0581

D to Z ↓	0.0110	0.0097	2.1397	1.0317
D to Z ↑	0.0261	0.0228	11.7980	6.0728
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0351	0.0383	0.6754	0.5095
A to Z ↑	0.0457	0.0492	4.0069	3.0321
B to Z ↓	0.0324	0.0361	0.6747	0.5091
B to Z ↑	0.0451	0.0492	4.0089	3.0252
C to Z ↓	0.0127	0.0124	0.7116	0.5333
C to Z ↑	0.0310	0.0308	4.0166	3.0352
D to Z ↓	0.0102	0.0098	0.7114	0.5342
D to Z ↑	0.0238	0.0223	4.0277	3.0400

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P10	1.610e-07	2.529e-12
X13_P10	2.605e-07	3.537e-12
X19_P10	4.117e-07	4.547e-12
X25_P10	5.007e-07	5.304e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	9.179e-04	1.688e-03	2.493e-03	3.124e-03
B (output stable)	7.875e-04	1.480e-03	2.084e-03	2.716e-03
C (output stable)	2.812e-06	3.394e-05	4.962e-05	7.182e-05
D (output stable)	2.457e-06	2.467e-05	2.111e-05	4.835e-05
A to Z	3.661e-03	6.878e-03	1.028e-02	1.321e-02
B to Z	3.404e-03	6.548e-03	9.531e-03	1.258e-02
C to Z	1.332e-03	2.618e-03	3.848e-03	5.010e-03
D to Z	9.210e-04	1.445e-03	2.347e-03	2.781e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

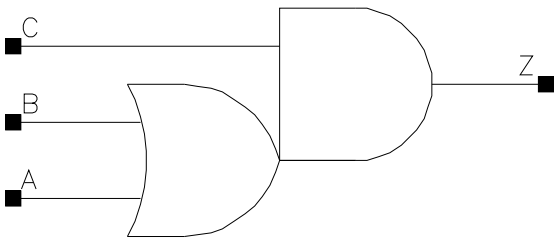
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	-2.394e-05	-5.849e-05	-7.643e-05	-1.088e-04
B (output stable)	-1.952e-05	-4.845e-05	-6.159e-05	-8.814e-05
C (output stable)	1.883e-05	3.045e-05	5.155e-05	6.551e-05
D (output stable)	8.083e-06	2.998e-05	2.985e-05	4.890e-05
A to Z	-8.546e-06	-2.546e-05	-2.936e-05	-4.478e-05
B to Z	-1.108e-05	-3.291e-05	-3.785e-05	-5.785e-05
C to Z	-3.403e-06	-1.217e-05	-1.382e-05	-2.049e-05
D to Z	-2.834e-07	-2.860e-07	-1.820e-07	-5.700e-07

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0010	0.0010	0.0019
B	0.0011	0.0011	0.0021
C	0.0011	0.0011	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0385	0.0446	2.0409	1.0214
A to Z ↑	0.0285	0.0316	3.7702	1.8516
B to Z ↓	0.0375	0.0441	2.0440	1.0214
B to Z ↑	0.0261	0.0295	3.7665	1.8501
C to Z ↓	0.0324	0.0357	2.0136	0.9993
C to Z ↑	0.0274	0.0299	3.7626	1.8492
	X33_P10		**X33_P10**	
A to Z ↓	0.0463		0.5208	
A to Z ↑	0.0339		0.9303	

B to Z ↓	0.0457		0.5210	
B to Z ↑	0.0312		0.9285	
C to Z ↓	0.0366		0.5083	
C to Z ↑	0.0312		0.9283	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.373e-07	2.024e-12
X17_P10	1.866e-07	2.275e-12
X33_P10	3.748e-07	3.787e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.170e-04	1.169e-04	2.436e-04
B (output stable)	1.607e-05	1.580e-05	2.934e-05
C (output stable)	5.382e-05	5.734e-05	1.033e-04
A to Z	2.769e-03	3.937e-03	8.190e-03
B to Z	2.393e-03	3.563e-03	7.460e-03
C to Z	3.023e-03	4.177e-03	8.642e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

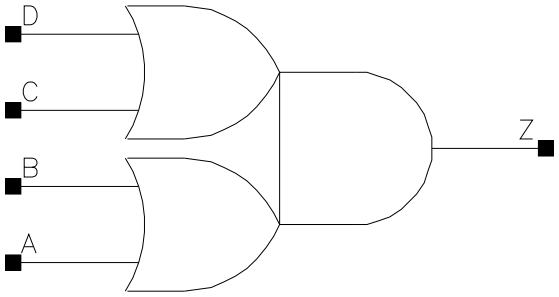
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-3.462e-06	-3.626e-06	-7.220e-06
B (output stable)	-1.642e-06	-1.696e-06	-3.424e-06
C (output stable)	2.062e-06	2.396e-06	4.181e-06
A to Z	-4.105e-06	-4.118e-06	-8.442e-06
B to Z	-5.003e-07	-4.890e-07	-1.222e-06
C to Z	-1.936e-06	-1.802e-06	-3.593e-06

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0010	0.0019
B	0.0007	0.0010	0.0019
C	0.0007	0.0010	0.0020
D	0.0007	0.0010	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0636	0.0544	2.0049	1.0170
A to Z ↑	0.0386	0.0340	3.6900	1.8442
B to Z ↓	0.0637	0.0541	2.0048	1.0179
B to Z ↑	0.0374	0.0325	3.6883	1.8439

C to Z ↓	0.0558	0.0484	1.9926	1.0143
C to Z ↑	0.0375	0.0340	3.6876	1.8446
D to Z ↓	0.0547	0.0473	1.9949	1.0148
D to Z ↑	0.0355	0.0315	3.6863	1.8414
	X33_P10		**X33_P10**	
A to Z ↓	0.0547		0.5253	
A to Z ↑	0.0338		0.9277	
B to Z ↓	0.0523		0.5257	
B to Z ↑	0.0317		0.9261	
C to Z ↓	0.0478		0.5228	
C to Z ↑	0.0330		0.9267	
D to Z ↓	0.0448		0.5237	
D to Z ↑	0.0305		0.9257	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.244e-07	2.527e-12
X17_P10	2.326e-07	2.778e-12
X33_P10	4.534e-07	4.545e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.093e-05	4.017e-05	1.017e-04
B (output stable)	1.663e-05	2.370e-05	4.416e-05
C (output stable)	4.500e-05	8.962e-05	2.958e-04
D (output stable)	7.523e-05	9.411e-05	2.331e-04
A to Z	3.171e-03	5.074e-03	9.990e-03
B to Z	2.992e-03	4.706e-03	8.961e-03
C to Z	2.759e-03	4.476e-03	8.712e-03
D to Z	2.556e-03	4.086e-03	7.640e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

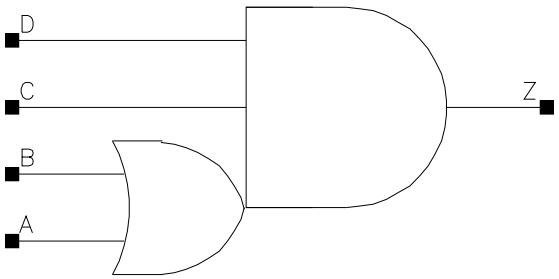
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-1.807e-06	-3.570e-06	-1.118e-05
B (output stable)	1.692e-07	-1.075e-06	-2.090e-06
C (output stable)	-7.685e-06	-1.474e-05	-5.057e-05
D (output stable)	3.712e-06	8.416e-06	3.133e-05
A to Z	-2.722e-06	-5.848e-06	-1.809e-05
B to Z	-5.460e-07	-2.097e-06	-5.956e-06
C to Z	-2.980e-06	-5.901e-06	-1.848e-05
D to Z	-8.867e-07	-1.828e-06	-6.252e-06

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	1.088	1.3056
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0007	0.0010	0.0016	0.0020
B	0.0006	0.0010	0.0017	0.0020
C	0.0007	0.0010	0.0017	0.0020
D	0.0007	0.0011	0.0017	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0544	0.0506	2.1049	1.0263
A to Z ↑	0.0452	0.0414	3.8103	1.8458
B to Z ↓	0.0541	0.0485	2.1061	1.0266
B to Z ↑	0.0431	0.0378	3.8154	1.8443
C to Z ↓	0.0426	0.0392	2.0397	0.9999

C to Z ↑	0.0434	0.0391	3.8091	1.8432
D to Z ↓	0.0414	0.0379	2.0397	0.9990
D to Z ↑	0.0446	0.0402	3.8082	1.8449
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0530	0.0511	0.7008	0.5243
A to Z ↑	0.0427	0.0432	1.2550	0.9402
B to Z ↓	0.0509	0.0490	0.7005	0.5249
B to Z ↑	0.0397	0.0399	1.2534	0.9388
C to Z ↓	0.0415	0.0399	0.6821	0.5105
C to Z ↑	0.0408	0.0406	1.2529	0.9385
D to Z ↓	0.0395	0.0382	0.6804	0.5096
D to Z ↑	0.0408	0.0409	1.2521	0.9383

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.043e-07	2.276e-12
X17_P10	2.005e-07	2.781e-12
X25_P10	3.181e-07	4.291e-12
X33_P10	4.031e-07	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	5.321e-05	1.089e-04	2.011e-04	2.312e-04
B (output stable)	3.967e-05	9.498e-05	1.496e-04	1.765e-04
C (output stable)	9.463e-06	1.561e-05	5.324e-05	6.309e-05
D (output stable)	1.955e-05	4.549e-05	1.214e-04	1.274e-04
A to Z	2.637e-03	4.562e-03	7.455e-03	9.156e-03
B to Z	2.457e-03	4.068e-03	6.707e-03	8.191e-03
C to Z	2.908e-03	4.943e-03	8.268e-03	9.965e-03
D to Z	2.775e-03	4.701e-03	7.667e-03	9.328e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

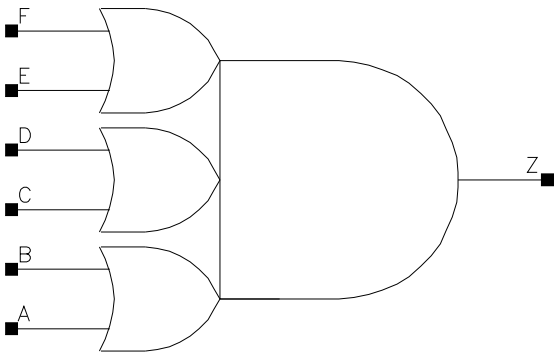
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	-1.659e-06	-4.716e-06	-5.484e-06	-6.732e-06
B (output stable)	-1.641e-06	-5.039e-06	-6.111e-06	-7.176e-06
C (output stable)	5.964e-07	6.041e-07	8.012e-07	-4.802e-08
D (output stable)	7.494e-07	7.278e-07	1.348e-06	-1.754e-08
A to Z	-2.340e-06	-7.793e-06	-9.789e-06	-1.235e-05
B to Z	-1.847e-07	-6.296e-07	-3.868e-07	-7.310e-07
C to Z	-9.949e-07	-2.390e-06	-3.133e-06	-4.196e-06
D to Z	-7.672e-07	-2.433e-06	-3.995e-06	-4.820e-06

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0010	0.0017
B	0.0007	0.0010	0.0019
C	0.0007	0.0010	0.0017
D	0.0007	0.0010	0.0019
E	0.0007	0.0010	0.0018
F	0.0007	0.0010	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0723	0.0617	2.1618	1.0484
A to Z ↑	0.0497	0.0447	3.7839	1.8613
B to Z ↓	0.0719	0.0616	2.1624	1.0489
B to Z ↑	0.0482	0.0433	3.7851	1.8614
C to Z ↓	0.0663	0.0582	2.1489	1.0467
C to Z ↑	0.0498	0.0443	3.7866	1.8611
D to Z ↓	0.0663	0.0578	2.1490	1.0473
D to Z ↑	0.0479	0.0424	3.7839	1.8611
E to Z ↓	0.0575	0.0512	2.1339	1.0423
E to Z ↑	0.0461	0.0419	3.7852	1.8598
F to Z ↓	0.0576	0.0504	2.1355	1.0429
F to Z ↑	0.0441	0.0396	3.7824	1.8593
	X33_P10		X33_P10	
A to Z ↓	0.0622		0.5379	
A to Z ↑	0.0459		0.9399	
B to Z ↓	0.0622		0.5380	
B to Z ↑	0.0432		0.9381	
C to Z ↓	0.0573		0.5347	
C to Z ↑	0.0453		0.9397	
D to Z ↓	0.0571		0.5351	
D to Z ↑	0.0428		0.9378	
E to Z ↓	0.0506		0.5324	
E to Z ↑	0.0430		0.9388	
F to Z ↓	0.0502		0.5326	
F to Z ↑	0.0402		0.9373	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.512e-07	3.031e-12
X17_P10	2.775e-07	3.285e-12
X33_P10	5.343e-07	5.554e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.795e-05	3.910e-05	6.292e-05
B (output stable)	6.906e-06	1.451e-05	2.227e-05
C (output stable)	3.323e-05	5.873e-05	1.167e-04
D (output stable)	3.375e-05	5.630e-05	1.180e-04
E (output stable)	2.932e-05	5.463e-05	1.013e-04
F (output stable)	1.070e-04	1.583e-04	3.054e-04
A to Z	3.637e-03	5.913e-03	1.148e-02
B to Z	3.446e-03	5.566e-03	1.084e-02
C to Z	3.309e-03	5.436e-03	1.049e-02
D to Z	3.129e-03	5.076e-03	9.822e-03
E to Z	2.878e-03	4.791e-03	9.262e-03
F to Z	2.705e-03	4.423e-03	8.580e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

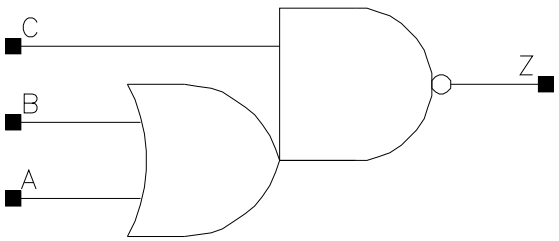
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	-1.369e-06	-3.121e-06	-4.497e-06
B (output stable)	-5.118e-07	-1.388e-06	-2.145e-06
C (output stable)	-3.564e-06	-7.462e-06	-1.411e-05
D (output stable)	1.107e-06	1.778e-06	2.903e-06
E (output stable)	-3.996e-06	-7.478e-06	-1.442e-05
F (output stable)	4.406e-08	1.386e-06	1.097e-06
A to Z	-3.252e-06	-6.683e-06	-1.185e-05
B to Z	-1.364e-06	-3.212e-06	-5.667e-06
C to Z	-3.377e-06	-7.621e-06	-1.384e-05
D to Z	-1.459e-06	-3.368e-06	-6.390e-06
E to Z	-3.935e-06	-7.539e-06	-1.457e-05
F to Z	-1.681e-06	-3.186e-06	-6.076e-06

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X34_P10	1.200	2.720	3.2640
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X34_P10	X46_P10
A	0.0008	0.0024	0.0050	0.0065
B	0.0008	0.0022	0.0045	0.0060
C	0.0009	0.0025	0.0052	0.0067

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0153	0.0156	3.8740	1.2705
A to Z ↑	0.0235	0.0245	7.8675	2.6632
B to Z ↓	0.0127	0.0129	3.8005	1.2819
B to Z ↑	0.0213	0.0210	7.9135	2.6790
C to Z ↓	0.0150	0.0151	3.5023	1.1613
C to Z ↑	0.0211	0.0208	3.7858	1.2560
	X34_P10	**X46_P10**	**X34_P10**	**X46_P10**
A to Z ↓	0.0165	0.0164	0.6481	0.4951

A to Z ↑	0.0256	0.0253	1.3270	1.0180
B to Z ↓	0.0134	0.0134	0.6574	0.5039
B to Z ↑	0.0217	0.0217	1.3359	1.0241
C to Z ↓	0.0156	0.0155	0.5950	0.4555
C to Z ↑	0.0213	0.0211	0.6272	0.4794

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P10	9.202e-08	1.771e-12
X17_P10	2.712e-07	3.284e-12
X34_P10	5.422e-07	5.807e-12
X46_P10	7.179e-07	7.318e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	1.072e-04	3.558e-04	7.326e-04	8.806e-04
B (output stable)	1.892e-05	5.206e-05	1.096e-04	1.466e-04
C (output stable)	4.370e-05	1.514e-04	3.250e-04	3.789e-04
A to Z	1.202e-03	3.794e-03	8.191e-03	1.051e-02
B to Z	8.187e-04	2.398e-03	5.191e-03	6.731e-03
C to Z	1.430e-03	4.328e-03	9.161e-03	1.174e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

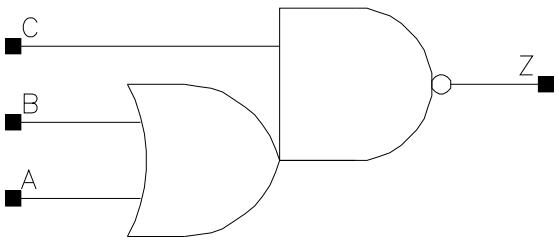
Pin Cycle (vdds)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	-2.906e-06	-9.982e-06	-2.437e-05	-2.750e-05
B (output stable)	-1.592e-06	-5.137e-06	-1.264e-05	-1.518e-05
C (output stable)	2.980e-08	3.985e-06	1.049e-05	4.735e-06
A to Z	-3.473e-06	-9.945e-06	-2.650e-05	-3.284e-05
B to Z	1.973e-07	4.870e-07	-5.260e-07	-3.603e-06
C to Z	-1.520e-06	-6.034e-06	-1.547e-05	-1.605e-05

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.544	0.6528
X11_P10	1.200	0.952	1.1424
X17_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X17_P10	X23_P10
A	0.0008	0.0017	0.0026	0.0035
B	0.0008	0.0017	0.0024	0.0032
C	0.0008	0.0016	0.0024	0.0032
	X46_P10			
A	0.0070			
B	0.0064			
C	0.0065			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0162	0.0165	3.9128	1.8254
A to Z ↑	0.0285	0.0288	8.2657	3.9014
B to Z ↓	0.0143	0.0145	3.8456	1.7727

B to Z ↑	0.0269	0.0273	8.2984	3.9160
C to Z ↓	0.0127	0.0127	3.6528	1.6971
C to Z ↑	0.0165	0.0164	4.0541	1.9062
	X17_P10	**X23_P10**	**X17_P10**	**X23_P10**
A to Z ↓	0.0159	0.0167	1.2713	0.9390
A to Z ↑	0.0273	0.0299	2.5897	1.9696
B to Z ↓	0.0138	0.0145	1.2675	0.9374
B to Z ↑	0.0254	0.0266	2.5966	1.9775
C to Z ↓	0.0122	0.0126	1.1961	0.8819
C to Z ↑	0.0154	0.0160	1.2672	0.9639
	X46_P10		**X46_P10**	
A to Z ↓	0.0166		0.4913	
A to Z ↑	0.0293		0.9937	
B to Z ↓	0.0142		0.4857	
B to Z ↑	0.0261		0.9981	
C to Z ↓	0.0127		0.4594	
C to Z ↑	0.0156		0.4870	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P10	1.024e-07	1.770e-12
X11_P10	2.118e-07	2.527e-12
X17_P10	3.138e-07	3.283e-12
X23_P10	4.239e-07	4.296e-12
X46_P10	8.312e-07	7.316e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	3.321e-05	7.331e-05	1.087e-04	1.880e-04
B (output stable)	1.246e-05	2.930e-05	4.371e-05	7.808e-05
C (output stable)	2.705e-04	6.303e-04	7.511e-04	1.181e-03
A to Z	1.576e-03	3.398e-03	4.632e-03	7.064e-03
B to Z	1.189e-03	2.601e-03	3.372e-03	4.969e-03
C to Z	8.197e-04	1.784e-03	2.367e-03	3.539e-03
	X46_P10			
A (output stable)	3.546e-04			
B (output stable)	1.496e-04			
C (output stable)	2.210e-03			
A to Z	1.362e-02			
B to Z	9.466e-03			
C to Z	6.756e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	-2.783e-06	-4.989e-06	-9.165e-06	-1.298e-05
B (output stable)	-1.515e-06	-3.161e-06	-5.044e-06	-8.449e-06
C (output stable)	-1.100e-09	-2.815e-06	-2.048e-07	-6.078e-06
A to Z	-4.125e-06	-1.053e-05	-1.402e-05	-2.351e-05
B to Z	-8.276e-07	-3.202e-06	-3.444e-06	-5.292e-06
C to Z	-1.084e-06	-2.635e-06	-4.022e-06	-8.414e-06

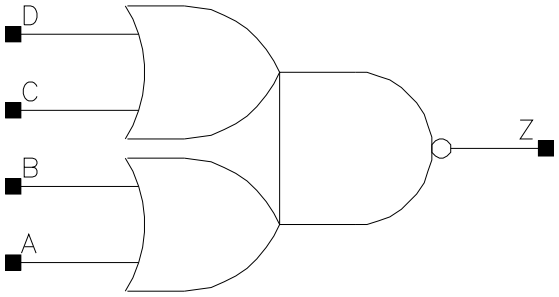
	X46_P10			
A (output stable)	-2.310e-05			
B (output stable)	-1.510e-05			
C (output stable)	-1.159e-05			
A to Z	-4.167e-05			
B to Z	-9.816e-06			
C to Z	-1.245e-05			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0009	0.0017	0.0025	0.0035
B	0.0009	0.0016	0.0023	0.0032
C	0.0008	0.0016	0.0024	0.0034
D	0.0008	0.0015	0.0022	0.0030
	X42_P10			
A	0.0069			
B	0.0063			
C	0.0066			
D	0.0061			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0177	0.0186	3.5838	1.7850
A to Z ↑	0.0326	0.0328	8.6806	3.9864
B to Z ↓	0.0160	0.0165	3.5009	1.7876
B to Z ↑	0.0307	0.0293	8.7005	4.0022
C to Z ↓	0.0157	0.0167	3.6500	1.8039
C to Z ↑	0.0246	0.0262	8.5065	3.9977
D to Z ↓	0.0133	0.0137	3.5579	1.8162
D to Z ↑	0.0222	0.0212	8.5501	4.0267
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0180	0.0183	1.2259	0.8827
A to Z ↑	0.0310	0.0321	2.6806	1.9766
B to Z ↓	0.0162	0.0161	1.2296	0.8803
B to Z ↑	0.0284	0.0289	2.6922	1.9825
C to Z ↓	0.0163	0.0164	1.2404	0.8925
C to Z ↑	0.0245	0.0252	2.6907	1.9781
D to Z ↓	0.0135	0.0135	1.2568	0.8965
D to Z ↑	0.0206	0.0208	2.7098	1.9923
	X42_P10		**X42_P10**	
A to Z ↓	0.0185		0.4644	
A to Z ↑	0.0320		1.0040	
B to Z ↓	0.0163		0.4584	
B to Z ↑	0.0289		1.0080	
C to Z ↓	0.0169		0.4705	
C to Z ↑	0.0252		1.0000	
D to Z ↓	0.0138		0.4669	
D to Z ↑	0.0208		1.0073	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P10	1.275e-07	2.024e-12
X10_P10	2.566e-07	3.284e-12
X15_P10	3.713e-07	4.041e-12
X21_P10	5.188e-07	5.302e-12
X42_P10	1.024e-06	9.337e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	3.647e-05	1.002e-04	1.426e-04	2.026e-04
B (output stable)	1.667e-05	3.972e-05	4.699e-05	6.712e-05
C (output stable)	8.496e-05	3.110e-04	3.629e-04	5.661e-04
D (output stable)	8.314e-05	2.122e-04	2.671e-04	3.809e-04
A to Z	1.918e-03	4.361e-03	5.946e-03	8.452e-03
B to Z	1.547e-03	3.270e-03	4.500e-03	6.386e-03
C to Z	1.310e-03	3.130e-03	4.177e-03	5.950e-03
D to Z	9.491e-04	2.002e-03	2.732e-03	3.832e-03
	X42_P10			
A (output stable)	3.919e-04			
B (output stable)	1.346e-04			
C (output stable)	1.099e-03			
D (output stable)	7.518e-04			

A to Z	1.664e-02			
B to Z	1.249e-02			
C to Z	1.173e-02			
D to Z	7.569e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

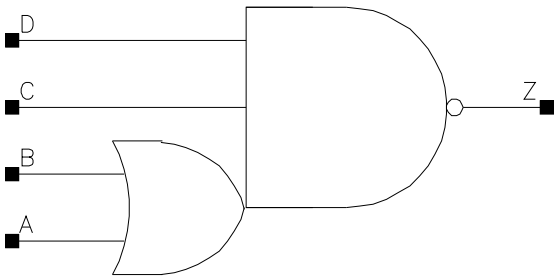
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	-3.206e-06	-1.092e-05	-1.056e-05	-1.892e-05
B (output stable)	-4.300e-07	-1.858e-06	-1.830e-06	-3.361e-06
C (output stable)	-1.376e-05	-5.406e-05	-4.453e-05	-8.725e-05
D (output stable)	7.295e-06	3.328e-05	2.517e-05	5.154e-05
A to Z	-5.377e-06	-1.813e-05	-1.531e-05	-2.727e-05
B to Z	-1.280e-06	-5.525e-06	-6.271e-06	-8.337e-06
C to Z	-4.894e-06	-1.856e-05	-1.589e-05	-2.900e-05
D to Z	-1.383e-06	-5.200e-06	-5.265e-06	-1.005e-05
	X42_P10			
A (output stable)	-3.344e-05			
B (output stable)	-6.213e-06			
C (output stable)	-1.518e-04			
D (output stable)	8.902e-05			
A to Z	-5.359e-05			
B to Z	-2.253e-05			
C to Z	-5.139e-05			
D to Z	-1.629e-05			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X21_P10	1.200	2.448	2.9376
X31_P10	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X21_P10	X31_P10
A	0.0009	0.0016	0.0032	0.0048
B	0.0010	0.0015	0.0029	0.0043
C	0.0008	0.0017	0.0034	0.0051
D	0.0009	0.0016	0.0032	0.0048

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0212	0.0204	5.0079	2.6825
A to Z ↑	0.0301	0.0281	7.8610	3.9564
B to Z ↓	0.0189	0.0167	5.0512	2.6938
B to Z ↑	0.0282	0.0242	7.9169	3.9803
C to Z ↓	0.0201	0.0207	4.7226	2.5260

C to Z ↑	0.0250	0.0245	3.6835	1.8534
D to Z ↓	0.0210	0.0202	4.7397	2.5375
D to Z ↑	0.0238	0.0225	3.7295	1.8575
	X21_P10	**X31_P10**	**X21_P10**	**X31_P10**
A to Z ↓	0.0205	0.0207	1.4029	0.9530
A to Z ↑	0.0273	0.0272	1.9761	1.3263
B to Z ↓	0.0166	0.0166	1.4103	0.9613
B to Z ↑	0.0233	0.0232	1.9889	1.3351
C to Z ↓	0.0204	0.0206	1.3230	0.8999
C to Z ↑	0.0239	0.0239	0.9393	0.6333
D to Z ↓	0.0201	0.0203	1.3277	0.9034
D to Z ↑	0.0220	0.0220	0.9410	0.6329

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P10	1.057e-07	2.276e-12
X10_P10	2.068e-07	3.284e-12
X21_P10	4.041e-07	5.303e-12
X31_P10	6.016e-07	7.318e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	1.065e-04	2.434e-04	4.625e-04	6.828e-04
B (output stable)	9.279e-05	1.858e-04	3.470e-04	5.175e-04
C (output stable)	1.878e-05	4.763e-05	8.029e-05	1.085e-04
D (output stable)	4.541e-05	1.296e-04	2.336e-04	3.384e-04
A to Z	1.875e-03	3.253e-03	6.170e-03	9.150e-03
B to Z	1.365e-03	2.182e-03	4.059e-03	6.002e-03
C to Z	2.229e-03	4.239e-03	8.010e-03	1.188e-02
D to Z	1.996e-03	3.536e-03	6.673e-03	9.904e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

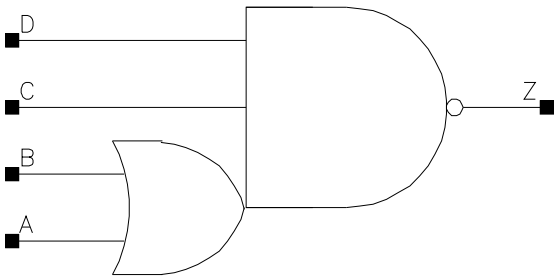
Pin Cycle (vdds)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	-4.624e-06	-8.073e-06	-1.444e-05	-2.041e-05
B (output stable)	-5.767e-06	-8.763e-06	-1.506e-05	-2.122e-05
C (output stable)	6.192e-07	1.003e-06	2.112e-06	2.694e-06
D (output stable)	7.498e-07	1.668e-06	3.296e-06	4.101e-06
A to Z	-7.634e-06	-1.144e-05	-1.917e-05	-2.581e-05
B to Z	2.640e-08	-1.540e-07	9.000e-07	6.200e-07
C to Z	-3.347e-06	-3.162e-06	-5.124e-06	-7.269e-06
D to Z	-2.950e-06	-4.602e-06	-7.916e-06	-1.174e-05

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0009	0.0018	0.0026	0.0035
B	0.0009	0.0016	0.0024	0.0033
C	0.0008	0.0016	0.0025	0.0033
D	0.0008	0.0016	0.0024	0.0031

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0208	0.0223	5.1123	2.6685
A to Z ↑	0.0328	0.0353	7.6506	3.8941
B to Z ↓	0.0185	0.0195	5.0235	2.6670
B to Z ↑	0.0316	0.0325	7.6740	3.9055
C to Z ↓	0.0169	0.0188	4.8165	2.5349

C to Z ↑	0.0203	0.0213	3.7478	1.8954
D to Z ↓	0.0164	0.0170	4.8532	2.5538
D to Z ↑	0.0181	0.0182	3.7742	1.9110
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0220	0.0222	1.8407	1.3882
A to Z ↑	0.0340	0.0347	2.6207	1.9854
B to Z ↓	0.0195	0.0194	1.8326	1.3840
B to Z ↑	0.0319	0.0324	2.6291	1.9907
C to Z ↓	0.0185	0.0187	1.7446	1.3160
C to Z ↑	0.0205	0.0208	1.2619	0.9508
D to Z ↓	0.0168	0.0171	1.7579	1.3256
D to Z ↑	0.0176	0.0179	1.2719	0.9586

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P10	1.256e-07	2.276e-12
X10_P10	2.512e-07	3.285e-12
X15_P10	3.647e-07	4.040e-12
X21_P10	4.963e-07	5.554e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	2.172e-05	5.665e-05	7.748e-05	1.102e-04
B (output stable)	2.883e-05	9.898e-05	1.186e-04	1.811e-04
C (output stable)	6.743e-05	1.248e-04	1.955e-04	2.488e-04
D (output stable)	1.648e-04	5.042e-04	6.233e-04	9.125e-04
A to Z	2.185e-03	4.760e-03	6.735e-03	9.217e-03
B to Z	1.773e-03	3.706e-03	5.248e-03	7.172e-03
C to Z	1.371e-03	3.111e-03	4.312e-03	5.958e-03
D to Z	1.092e-03	2.319e-03	3.251e-03	4.449e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

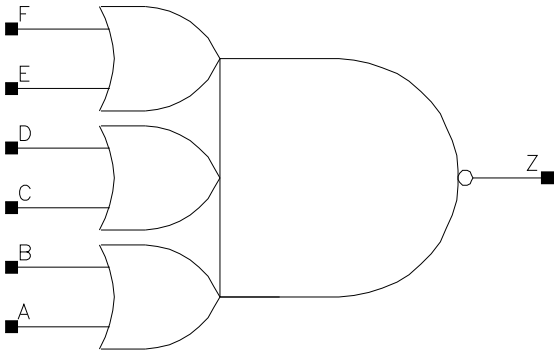
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	-2.537e-06	-7.042e-06	-6.310e-06	-1.234e-05
B (output stable)	-2.481e-06	-7.679e-06	-7.303e-06	-1.349e-05
C (output stable)	-2.180e-10	2.146e-06	1.048e-06	3.827e-06
D (output stable)	-2.320e-09	-2.292e-06	-2.728e-06	-4.297e-06
A to Z	-3.697e-06	-1.154e-05	-1.007e-05	-1.832e-05
B to Z	-2.173e-06	-8.000e-08	-3.046e-06	-1.540e-07
C to Z	-8.570e-07	-3.797e-06	-2.528e-06	-4.866e-06
D to Z	-9.010e-07	-3.948e-06	-2.978e-06	-6.717e-06

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	1.088	1.3056
X9_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X9_P10
A	0.0007	0.0018
B	0.0007	0.0016
C	0.0007	0.0017
D	0.0007	0.0016
E	0.0007	0.0017
F	0.0007	0.0015

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X9_P10	X3_P10	X9_P10
A to Z ↓	0.0258	0.0269	5.8738	2.4228
A to Z ↑	0.0429	0.0409	10.7465	3.9099
B to Z ↓	0.0244	0.0243	5.9090	2.4225
B to Z ↑	0.0427	0.0382	10.7693	3.9202
C to Z ↓	0.0249	0.0255	5.9120	2.4324
C to Z ↑	0.0373	0.0356	10.7632	3.8997
D to Z ↓	0.0230	0.0227	5.9478	2.4352
D to Z ↑	0.0368	0.0326	10.7974	3.9146
E to Z ↓	0.0212	0.0222	5.9537	2.4361
E to Z ↑	0.0294	0.0287	10.7954	3.9043
F to Z ↓	0.0193	0.0188	5.9958	2.4407
F to Z ↑	0.0284	0.0246	10.8559	3.9274

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P10	1.424e-07	2.780e-12
X9_P10	3.639e-07	4.545e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P10	X9_P10
A (output stable)	2.418e-05	8.703e-05
B (output stable)	8.960e-06	3.314e-05
C (output stable)	4.291e-05	1.876e-04
D (output stable)	4.948e-05	1.647e-04
E (output stable)	3.839e-05	1.661e-04
F (output stable)	1.452e-04	3.476e-04
A to Z	2.536e-03	6.590e-03
B to Z	2.271e-03	5.517e-03
C to Z	2.068e-03	5.378e-03
D to Z	1.803e-03	4.357e-03
E to Z	1.493e-03	4.068e-03
F to Z	1.232e-03	2.995e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

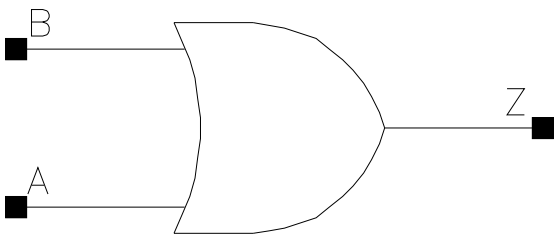
Pin Cycle (vdds)	X3_P10	X9_P10
A (output stable)	-2.042e-06	-9.193e-06
B (output stable)	-8.043e-07	-4.195e-06
C (output stable)	-5.183e-06	-2.658e-05
D (output stable)	1.567e-06	1.044e-05
E (output stable)	-5.426e-06	-2.651e-05
F (output stable)	3.327e-07	5.648e-06
A to Z	-4.323e-06	-1.904e-05
B to Z	-1.943e-06	-8.591e-06
C to Z	-4.986e-06	-2.150e-05
D to Z	-2.152e-06	-8.535e-06
E to Z	-5.115e-06	-2.359e-05
F to Z	-2.003e-06	-9.746e-06

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X33_P10	1.200	1.360	1.6320
X50_P10	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P10	X16_P10	X33_P10	X50_P10
A	0.0008	0.0010	0.0019	0.0019
B	0.0007	0.0010	0.0019	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0500	0.0445	2.0575	1.0374
A to Z ↑	0.0271	0.0278	3.7265	1.8767
B to Z ↓	0.0486	0.0433	2.0580	1.0384
B to Z ↑	0.0258	0.0261	3.7275	1.8760
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0459	0.0536	0.5142	0.3561
A to Z ↑	0.0277	0.0276	0.9153	0.6183
B to Z ↓	0.0430	0.0512	0.5152	0.3564
B to Z ↑	0.0256	0.0261	0.9145	0.6177

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	9.031e-08	1.771e-12
X16_P10	1.531e-07	2.023e-12
X33_P10	3.110e-07	3.282e-12
X50_P10	4.143e-07	3.787e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	2.653e-05	5.112e-05	1.189e-04	1.127e-04
B (output stable)	1.592e-06	4.052e-06	6.260e-05	5.402e-05
A to Z	2.444e-03	3.855e-03	8.113e-03	1.069e-02
B to Z	2.227e-03	3.467e-03	7.020e-03	9.660e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

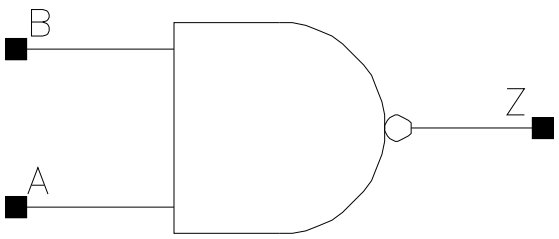
Pin Cycle (vdds)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	-2.442e-06	-4.390e-06	-1.372e-05	-1.376e-05
B (output stable)	4.057e-06	1.502e-05	6.366e-05	6.213e-05
A to Z	-2.769e-06	-5.233e-06	-1.854e-05	-1.879e-05
B to Z	-3.892e-07	-3.262e-07	-7.158e-07	-1.180e-06

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X16_P10	1.200	0.952	1.1424
X24_P10	1.200	1.088	1.3056
X32_P10	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P10	X16_P10	X24_P10	X32_P10
A	0.0010	0.0010	0.0010	0.0010
B	0.0011	0.0011	0.0011	0.0011

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0370	0.0386	1.9786	1.0314
A to Z ↑	0.0418	0.0429	3.7641	1.9218
B to Z ↓	0.0380	0.0397	1.9780	1.0322
B to Z ↑	0.0400	0.0405	3.7580	1.9193
	X24_P10	**X32_P10**	**X24_P10**	**X32_P10**
A to Z ↓	0.0430	0.0434	0.7015	0.5273
A to Z ↑	0.0458	0.0471	1.2830	0.9579
B to Z ↓	0.0441	0.0448	0.7012	0.5271
B to Z ↑	0.0433	0.0454	1.2822	0.9577

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.688e-07	2.277e-12
X16_P10	2.118e-07	2.530e-12
X24_P10	2.532e-07	2.778e-12
X32_P10	3.282e-07	3.032e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	1.961e-05	1.973e-05	1.983e-05	1.986e-05
B (output stable)	7.069e-05	7.097e-05	7.107e-05	7.215e-05
A to Z	4.785e-03	5.512e-03	6.971e-03	9.221e-03
B to Z	4.534e-03	5.275e-03	6.744e-03	8.974e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

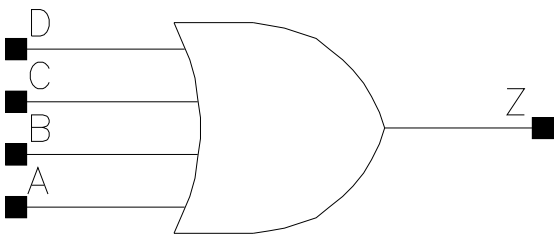
Pin Cycle (vdds)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	-7.500e-10	3.110e-09	2.920e-09	9.290e-09
B (output stable)	-3.770e-08	-3.780e-08	-3.740e-08	-3.560e-08
A to Z	-4.324e-07	-3.864e-07	-6.662e-07	-2.522e-07
B to Z	-1.640e-07	-1.157e-07	-7.030e-07	-3.338e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P10	1.200	2.176	2.6112
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P10	X27_P10
A	0.0017	0.0020
B	0.0016	0.0020
C	0.0017	0.0020
D	0.0016	0.0021

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P10	X27_P10	X20_P10	X27_P10
A to Z ↓	0.0501	0.0524	1.2536	0.9384
A to Z ↑	0.0288	0.0280	1.2264	0.9137
B to Z ↓	0.0478	0.0495	1.2530	0.9367
B to Z ↑	0.0274	0.0262	1.2251	0.9131
C to Z ↓	0.0484	0.0507	1.2522	0.9383
C to Z ↑	0.0275	0.0273	1.2287	0.9171
D to Z ↓	0.0462	0.0482	1.2544	0.9380
D to Z ↑	0.0261	0.0257	1.2272	0.9168

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X20_P10	3.789e-07	4.796e-12
X27_P10	5.252e-07	5.553e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X20_P10	X27_P10
A (output stable)	1.847e-03	2.544e-03
B (output stable)	1.504e-03	2.060e-03
C (output stable)	1.773e-03	2.543e-03
D (output stable)	1.302e-03	1.897e-03
A to Z	7.741e-03	1.091e-02
B to Z	6.977e-03	9.794e-03
C to Z	6.713e-03	9.328e-03
D to Z	5.957e-03	8.322e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

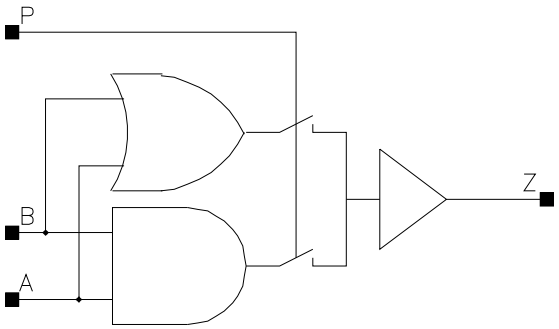
Pin Cycle (vdds)	X20_P10	X27_P10
A (output stable)	-6.612e-06	-1.328e-05
B (output stable)	-1.236e-07	6.190e-07
C (output stable)	-2.270e-05	-4.907e-05
D (output stable)	1.282e-05	2.833e-05
A to Z	-7.673e-06	-1.556e-05
B to Z	-5.640e-07	-8.490e-07
C to Z	-7.257e-06	-1.517e-05
D to Z	-5.600e-08	-3.690e-07

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X16_P10	1.200	1.224	1.4688
X25_P10	1.200	2.040	2.4480
X33_P10	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0013	0.0018	0.0032	0.0032
B	0.0012	0.0018	0.0036	0.0036
P	0.0007	0.0010	0.0019	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0602	0.0550	2.1021	1.0282
A to Z ↑	0.0362	0.0337	3.7735	1.8862
B to Z ↓	0.0592	0.0542	2.1183	1.0372
B to Z ↑	0.0374	0.0349	3.7755	1.8898
P to Z ↓	0.0536	0.0497	2.1226	1.0399
P to Z ↑	0.0362	0.0340	3.7755	1.8871
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**

A to Z ↓	0.0525	0.0559	0.6998	0.5312
A to Z ↑	0.0336	0.0351	1.2683	0.9507
B to Z ↓	0.0516	0.0546	0.7046	0.5344
B to Z ↑	0.0350	0.0363	1.2711	0.9514
P to Z ↓	0.0479	0.0511	0.7074	0.5359
P to Z ↑	0.0334	0.0349	1.2689	0.9496

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	1.368e-07	2.528e-12
X16_P10	2.551e-07	3.032e-12
X25_P10	4.500e-07	4.544e-12
X33_P10	4.971e-07	4.795e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	4.136e-05	8.175e-05	1.609e-04	1.628e-04
B (output stable)	1.661e-04	3.005e-04	5.338e-04	5.414e-04
P (output stable)	1.200e-04	2.007e-04	3.499e-04	3.586e-04
A to Z	2.821e-03	4.746e-03	8.235e-03	9.333e-03
B to Z	2.721e-03	4.574e-03	7.855e-03	8.974e-03
P to Z	2.432e-03	4.155e-03	7.224e-03	8.326e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

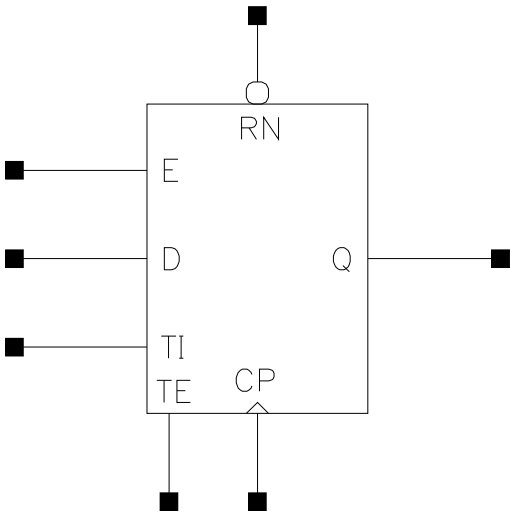
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	-2.337e-06	-5.795e-06	-1.005e-05	-1.019e-05
B (output stable)	-2.364e-05	-3.988e-05	-4.541e-05	-4.641e-05
P (output stable)	1.280e-05	3.249e-05	4.140e-05	4.269e-05
A to Z	-4.723e-06	-8.312e-06	-1.051e-05	-1.035e-05
B to Z	-3.744e-06	-6.564e-06	-8.506e-06	-8.155e-06
P to Z	-1.284e-06	-2.664e-06	-6.007e-06	-5.839e-06

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.488	5.3856
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
E	0.0009	0.0011	0.0011	0.0011
RN	0.0008	0.0007	0.0007	0.0008
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to Q ↓	0.1110	0.0558	4.7043	2.0569
CP to Q ↑	0.0823	0.0695	7.6734	3.7378
RN to Q ↓	0.0900	0.0750	3.8897	2.1999
	X17_P10	X33_P10	X17_P10	X33_P10
CP to Q ↓	0.0934	0.0981	0.9904	0.5228
CP to Q ↑	0.1139	0.1190	1.8358	0.9349
RN to Q ↓	0.1255	0.1300	0.9881	0.5221

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1702	0.1117	0.1117	0.1117
CP ↑	min_pulse_width to CP	0.1013	0.0453	0.0405	0.0405
D ↓	hold_rising to CP	-0.1817	-0.0943	-0.0943	-0.0943
D ↑	hold_rising to CP	-0.0818	-0.0316	-0.0312	-0.0312
D ↓	setup_rising to CP	0.2455	0.1535	0.1560	0.1535
D ↑	setup_rising to CP	0.1215	0.0682	0.0682	0.0686
E ↓	hold_rising to CP	-0.0987	-0.0987	-0.1039	-0.1039
E ↑	hold_rising to CP	-0.0796	-0.0316	-0.0316	-0.0316
E ↓	setup_rising to CP	0.2043	0.2075	0.2075	0.2075
E ↑	setup_rising to CP	0.2348	0.1559	0.1590	0.1615
RN ↓	min_pulse_width to RN	0.0942	0.1018	0.0898	0.0920
RN ↑	recovery_rising to CP	0.0266	0.0297	0.0297	0.0297
RN ↑	removal_rising to CP	-0.0197	-0.0126	-0.0152	-0.0152
TE ↓	hold_rising to CP	-0.0765	-0.0627	-0.0623	-0.0623
TE ↑	hold_rising to CP	-0.0556	-0.0360	-0.0357	-0.0357
TE ↓	setup_rising to CP	0.1658	0.1215	0.1219	0.1215
TE ↑	setup_rising to CP	0.2903	0.2054	0.2050	0.2050
TI ↓	hold_rising to CP	-0.2209	-0.1262	-0.1257	-0.1257
TI ↑	hold_rising to CP	-0.0658	-0.0339	-0.0379	-0.0379
TI ↓	setup_rising to CP	0.2905	0.1902	0.1902	0.1902
TI ↑	setup_rising to CP	0.1020	0.0734	0.0734	0.0734

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	4.501e-07	9.677e-12
X8_P10	4.692e-07	9.081e-12
X17_P10	5.467e-07	9.585e-12
X33_P10	6.509e-07	1.009e-11

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

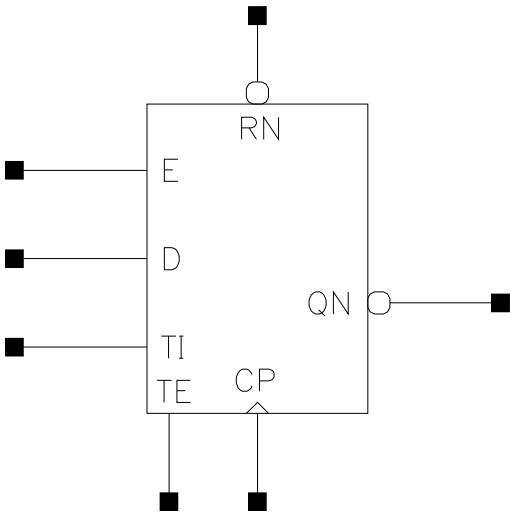
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.489e-03	4.526e-03	4.536e-03	4.541e-03
Clock 100Mhz Data 25Mhz	7.249e-03	7.442e-03	8.182e-03	8.965e-03
Clock 100Mhz Data 50Mhz	1.001e-02	1.036e-02	1.183e-02	1.339e-02
Clock = 0 Data 100Mhz	6.241e-03	6.155e-03	6.128e-03	6.115e-03
Clock = 1 Data 100Mhz	2.489e-03	2.513e-03	2.523e-03	2.527e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.624	5.5488
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
E	0.0009	0.0011	0.0011	0.0011
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to QN ↓	0.1025	0.0954	3.7793	1.9744
CP to QN ↑	0.1209	0.0719	7.5337	3.6352
RN to QN ↑	0.1072	0.1061	7.5116	3.6329
	X17_P10	X33_P10	X17_P10	X33_P10
CP to QN ↓	0.0902	0.0951	0.9914	0.5233
CP to QN ↑	0.0768	0.0832	1.8335	0.9369
RN to QN ↑	0.1057	0.1158	1.8410	0.9386

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1678	0.1117	0.1117	0.1117
CP ↑	min_pulse_width to CP	0.0733	0.0368	0.0453	0.0502
D ↓	hold_rising to CP	-0.1817	-0.0943	-0.0943	-0.0943
D ↑	hold_rising to CP	-0.0818	-0.0312	-0.0316	-0.0316
D ↓	setup_rising to CP	0.2511	0.1535	0.1535	0.1560
D ↑	setup_rising to CP	0.1215	0.0682	0.0682	0.0682
E ↓	hold_rising to CP	-0.1017	-0.1039	-0.0987	-0.0987
E ↑	hold_rising to CP	-0.0796	-0.0316	-0.0316	-0.0316
E ↓	setup_rising to CP	0.2092	0.2075	0.2075	0.2075
E ↑	setup_rising to CP	0.2344	0.1590	0.1590	0.1590
RN ↓	min_pulse_width to RN	0.0942	0.0925	0.1040	0.1111
RN ↑	recovery_rising to CP	0.0266	0.0296	0.0297	0.0297
RN ↑	removal_rising to CP	-0.0197	-0.0148	-0.0126	-0.0126
TE ↓	hold_rising to CP	-0.0765	-0.0623	-0.0630	-0.0605
TE ↑	hold_rising to CP	-0.0552	-0.0357	-0.0360	-0.0360
TE ↓	setup_rising to CP	0.1658	0.1215	0.1215	0.1219
TE ↑	setup_rising to CP	0.2903	0.2050	0.2050	0.2050
TI ↓	hold_rising to CP	-0.2250	-0.1262	-0.1262	-0.1206
TI ↑	hold_rising to CP	-0.0658	-0.0379	-0.0339	-0.0339
TI ↓	setup_rising to CP	0.2905	0.1902	0.1902	0.1902
TI ↑	setup_rising to CP	0.1005	0.0734	0.0775	0.0775

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	4.506e-07	9.677e-12
X8_P10	4.676e-07	9.332e-12
X17_P10	5.459e-07	9.585e-12
X33_P10	6.442e-07	1.009e-11

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

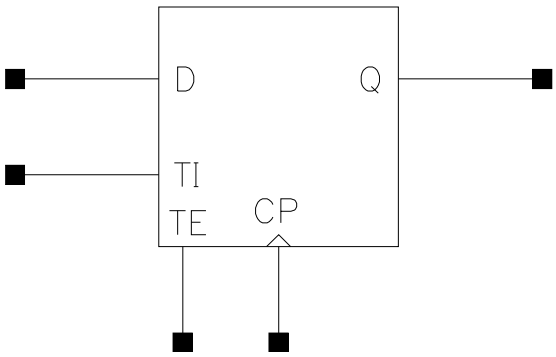
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.463e-03	4.499e-03	4.506e-03	4.510e-03
Clock 100Mhz Data 25Mhz	7.244e-03	7.481e-03	8.099e-03	8.862e-03
Clock 100Mhz Data 50Mhz	1.003e-02	1.046e-02	1.169e-02	1.321e-02
Clock = 0 Data 100Mhz	6.246e-03	6.159e-03	6.131e-03	6.117e-03
Clock = 1 Data 100Mhz	2.489e-03	2.511e-03	2.520e-03	2.524e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.400	4.0800
X8_P10	1.200	3.128	3.7536
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0898	0.0518	4.4007	2.0509
CP to Q ↑	0.0738	0.0632	7.7198	3.6910
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0764	0.0840	0.9693	0.5133
CP to Q ↑	0.1119	0.1181	1.8299	0.9330

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1455	0.1480	0.1480	0.1480
CP ↑	min_pulse_width to CP	0.0684	0.0405	0.0357	0.0358
D ↓	hold_rising to CP	-0.1085	-0.0508	-0.0508	-0.0508
D ↑	hold_rising to CP	-0.0357	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1577	0.1050	0.1050	0.1050
D ↑	setup_rising to CP	0.0654	0.0338	0.0338	0.0338
TE ↓	hold_rising to CP	-0.0596	-0.0397	-0.0428	-0.0428
TE ↑	hold_rising to CP	-0.0454	-0.0286	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1337	0.1020	0.1020	0.1020
TE ↑	setup_rising to CP	0.2539	0.2055	0.2055	0.2055
TI ↓	hold_rising to CP	-0.2114	-0.1325	-0.1319	-0.1319
TI ↑	hold_rising to CP	-0.0511	-0.0290	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.2661	0.2014	0.1973	0.1973
TI ↑	setup_rising to CP	0.0864	0.0601	0.0601	0.0601

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	3.480e-07	7.064e-12
X8_P10	3.679e-07	6.560e-12
X17_P10	4.686e-07	7.317e-12
X33_P10	5.571e-07	7.821e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

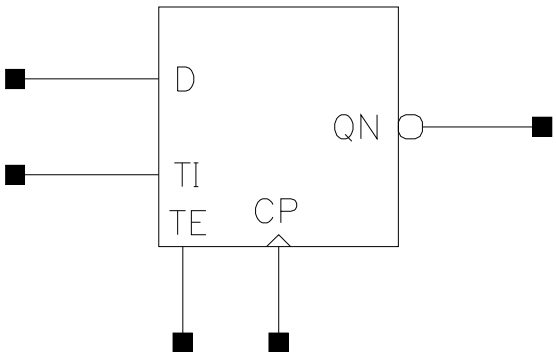
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.001e-03	4.012e-03	4.013e-03	4.012e-03
Clock 100Mhz Data 25Mhz	5.957e-03	6.075e-03	6.771e-03	7.414e-03
Clock 100Mhz Data 50Mhz	7.914e-03	8.137e-03	9.530e-03	1.082e-02
Clock = 0 Data 100Mhz	4.985e-03	4.741e-03	4.659e-03	4.619e-03
Clock = 1 Data 100Mhz	1.409e-03	7.464e-04	5.257e-04	4.154e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.536	4.2432
X8_P10	1.200	3.264	3.9168
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0964	0.1027	4.3244	2.0531
CP to QN ↑	0.0968	0.0658	7.6820	3.6426
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0768	0.0852	0.9705	0.5142
CP to QN ↑	0.0670	0.0737	1.8269	0.9323

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1437	0.1480	0.1480	0.1480
CP ↑	min_pulse_width to CP	0.0539	0.0357	0.0405	0.0405
D ↓	hold_rising to CP	-0.1085	-0.0533	-0.0508	-0.0508
D ↑	hold_rising to CP	-0.0357	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1577	0.1050	0.1050	0.1050
D ↑	setup_rising to CP	0.0654	0.0338	0.0338	0.0338
TE ↓	hold_rising to CP	-0.0596	-0.0428	-0.0397	-0.0397
TE ↑	hold_rising to CP	-0.0454	-0.0286	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1312	0.1020	0.1020	0.1020
TE ↑	setup_rising to CP	0.2539	0.2055	0.2055	0.2055
TI ↓	hold_rising to CP	-0.2114	-0.1319	-0.1325	-0.1325
TI ↑	hold_rising to CP	-0.0511	-0.0290	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.2607	0.2014	0.2014	0.1973
TI ↑	setup_rising to CP	0.0858	0.0601	0.0601	0.0601

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	3.497e-07	7.316e-12
X8_P10	3.690e-07	6.812e-12
X17_P10	4.679e-07	7.316e-12
X33_P10	5.564e-07	7.820e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

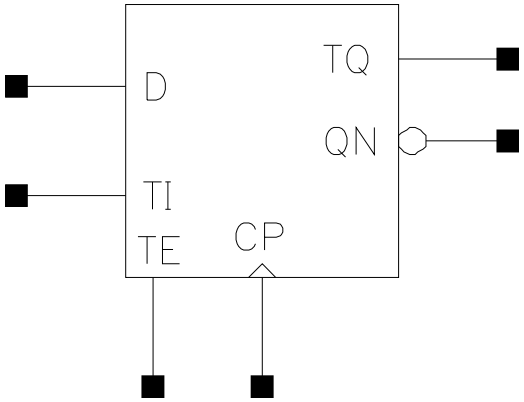
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.968e-03	3.989e-03	3.994e-03	3.997e-03
Clock 100Mhz Data 25Mhz	5.989e-03	6.151e-03	6.716e-03	7.377e-03
Clock 100Mhz Data 50Mhz	8.011e-03	8.314e-03	9.439e-03	1.076e-02
Clock = 0 Data 100Mhz	5.030e-03	4.782e-03	4.699e-03	4.658e-03
Clock = 1 Data 100Mhz	1.414e-03	7.569e-04	5.378e-04	4.283e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.536	4.2432
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0013	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1066	0.0906	3.9049	1.9851
CP to QN ↑	0.1189	0.0701	7.5712	3.6698
CP to TQ ↓	0.0837	0.0478	5.5096	3.7716
CP to TQ ↑	0.0759	0.0630	14.7065	10.3715
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0852	0.0916	0.9959	0.5268
CP to QN ↑	0.0721	0.0770	1.8564	0.9534
CP to TQ ↓	0.0499	0.0523	4.9978	5.0151
CP to TQ ↑	0.0641	0.0657	13.5467	14.3335

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1455	0.1480	0.1480	0.1480
CP ↑	min_pulse_width to CP	0.0722	0.0405	0.0405	0.0416
D ↓	hold_rising to CP	-0.1085	-0.0508	-0.0508	-0.0508
D ↑	hold_rising to CP	-0.0357	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1580	0.1050	0.1050	0.1050
D ↑	setup_rising to CP	0.0654	0.0338	0.0338	0.0338
TE ↓	hold_rising to CP	-0.0596	-0.0397	-0.0397	-0.0397
TE ↑	hold_rising to CP	-0.0454	-0.0286	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1312	0.0995	0.0995	0.0995
TE ↑	setup_rising to CP	0.2539	0.2055	0.2055	0.2055
TI ↓	hold_rising to CP	-0.2119	-0.1325	-0.1325	-0.1325
TI ↑	hold_rising to CP	-0.0511	-0.0290	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.2607	0.1958	0.1958	0.1958
TI ↑	setup_rising to CP	0.0864	0.0601	0.0601	0.0601

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	3.743e-07	7.834e-12
X8_P10	4.043e-07	7.316e-12
X17_P10	4.563e-07	7.569e-12
X33_P10	5.591e-07	8.072e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10

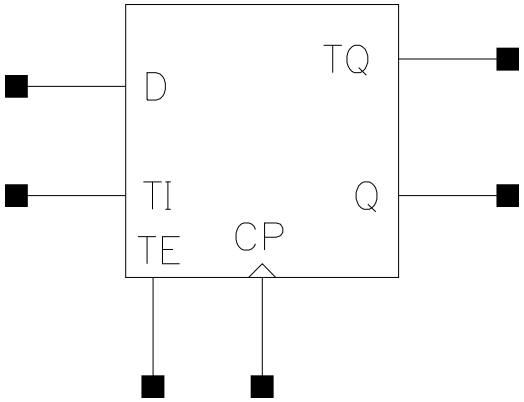
Clock 100Mhz Data 0Mhz	4.073e-03	4.045e-03	4.035e-03	4.031e-03
Clock 100Mhz Data 25Mhz	6.284e-03	6.468e-03	6.746e-03	7.453e-03
Clock 100Mhz Data 50Mhz	8.495e-03	8.890e-03	9.456e-03	1.088e-02
Clock = 0 Data 100Mhz	5.001e-03	4.755e-03	4.673e-03	4.633e-03
Clock = 1 Data 100Mhz	1.422e-03	7.262e-04	4.944e-04	3.786e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.400	4.0800
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1176	0.0582	4.7264	2.0538
CP to Q ↑	0.0842	0.0669	7.8209	3.7128
CP to TQ ↓	0.1153	0.0617	4.6906	5.1313
CP to TQ ↑	0.0864	0.0737	10.4129	14.5278
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0786	0.0862	1.0000	0.5253
CP to Q ↑	0.1141	0.1200	1.8678	0.9379
CP to TQ ↓	0.0821	0.0916	4.8773	4.9697
CP to TQ ↑	0.1208	0.1288	14.0578	14.2133

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1455	0.1480	0.1480	0.1480
CP ↑	min_pulse_width to CP	0.1013	0.0442	0.0358	0.0358
D ↓	hold_rising to CP	-0.1085	-0.0508	-0.0508	-0.0508
D ↑	hold_rising to CP	-0.0357	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1580	0.1050	0.1050	0.1050
D ↑	setup_rising to CP	0.0654	0.0338	0.0338	0.0338
TE ↓	hold_rising to CP	-0.0596	-0.0397	-0.0428	-0.0428
TE ↑	hold_rising to CP	-0.0454	-0.0286	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1312	0.0995	0.1020	0.1020
TE ↑	setup_rising to CP	0.2539	0.2055	0.2055	0.2055
TI ↓	hold_rising to CP	-0.2119	-0.1325	-0.1319	-0.1319
TI ↑	hold_rising to CP	-0.0511	-0.0290	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.2607	0.1958	0.1973	0.2014
TI ↑	setup_rising to CP	0.0864	0.0601	0.0601	0.0601

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	3.753e-07	7.568e-12
X8_P10	3.884e-07	7.064e-12
X17_P10	4.870e-07	7.569e-12
X33_P10	5.750e-07	8.072e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

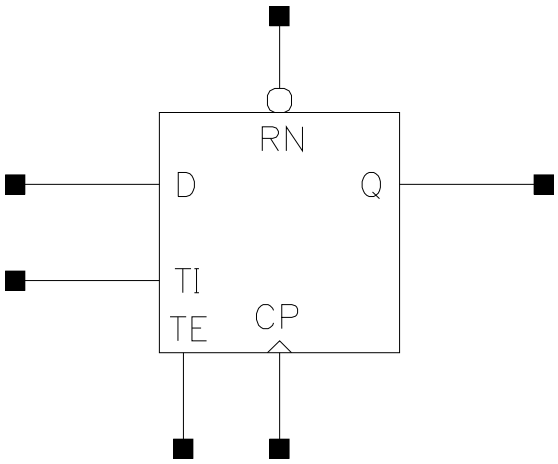
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	3.982e-03	3.996e-03	4.002e-03	4.002e-03
Clock 100Mhz Data 25Mhz	6.225e-03	6.283e-03	6.975e-03	7.633e-03
Clock 100Mhz Data 50Mhz	8.468e-03	8.569e-03	9.948e-03	1.126e-02
Clock = 0 Data 100Mhz	4.979e-03	4.737e-03	4.658e-03	4.619e-03
Clock = 1 Data 100Mhz	1.401e-03	7.163e-04	4.881e-04	3.741e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.672	4.4064
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
RN	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1086	0.0556	4.8012	2.0631
CP to Q ↑	0.0812	0.0681	7.7163	3.7326
RN to Q ↓	0.0887	0.0756	3.9594	2.1813
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0804	0.0884	0.9820	0.5213
CP to Q ↑	0.1004	0.1061	1.8279	0.9327
RN to Q ↓	0.1131	0.1211	0.9784	0.5206

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1625	0.1547	0.1571	0.1571
CP ↑	min_pulse_width to CP	0.0916	0.0405	0.0368	0.0368
D ↓	hold_rising to CP	-0.0987	-0.0410	-0.0410	-0.0410
D ↑	hold_rising to CP	-0.0405	-0.0090	-0.0121	-0.0121
D ↓	setup_rising to CP	0.1577	0.1024	0.1020	0.1020
D ↑	setup_rising to CP	0.0756	0.0436	0.0491	0.0491
RN ↓	min_pulse_width to RN	0.0916	0.0969	0.0925	0.0925
RN ↑	recovery_rising to CP	0.0296	0.0297	0.0297	0.0297
RN ↑	removal_rising to CP	-0.0197	-0.0148	-0.0151	-0.0151
TE ↓	hold_rising to CP	-0.0645	-0.0361	-0.0361	-0.0361
TE ↑	hold_rising to CP	-0.0525	-0.0334	-0.0334	-0.0334
TE ↓	setup_rising to CP	0.1368	0.1002	0.1002	0.1002
TE ↑	setup_rising to CP	0.2570	0.2006	0.2006	0.2006
TI ↓	hold_rising to CP	-0.1972	-0.1124	-0.1178	-0.1178
TI ↑	hold_rising to CP	-0.0609	-0.0352	-0.0352	-0.0352
TI ↓	setup_rising to CP	0.2661	0.1909	0.1924	0.1924
TI ↑	setup_rising to CP	0.0969	0.0752	0.0747	0.0747

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	4.064e-07	8.072e-12
X8_P10	4.226e-07	7.569e-12
X17_P10	5.172e-07	8.324e-12
X33_P10	6.075e-07	8.827e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.491e-03	4.530e-03	4.564e-03	4.581e-03

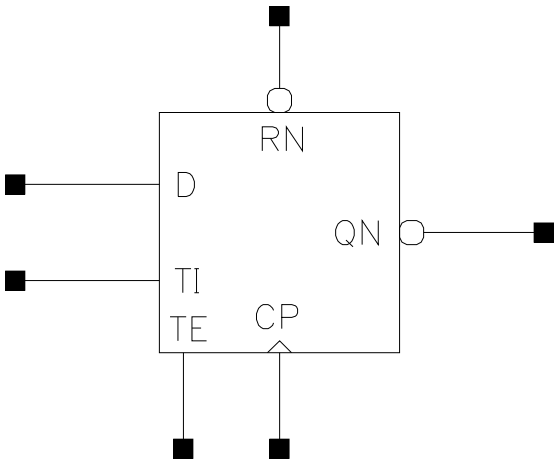
Clock 100Mhz Data 25Mhz	6.700e-03	6.738e-03	7.594e-03	8.282e-03
Clock 100Mhz Data 50Mhz	8.908e-03	8.946e-03	1.062e-02	1.198e-02
Clock = 0 Data 100Mhz	5.177e-03	4.840e-03	4.727e-03	4.670e-03
Clock = 1 Data 100Mhz	1.435e-03	7.983e-04	5.851e-04	4.786e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	3.944	4.7328
X33_P10	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
RN	0.0008	0.0008	0.0009	0.0009
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0923	0.0849	3.6679	1.9165
CP to QN ↑	0.1111	0.0652	7.5256	3.6213
RN to QN ↑	0.0999	0.1001	7.5023	3.6104
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0836	0.0919	0.9822	0.5207
CP to QN ↑	0.0740	0.0810	1.8432	0.9450
RN to QN ↑	0.1039	0.1133	1.8461	0.9459

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1625	0.1547	0.1547	0.1547
CP ↑	min_pulse_width to CP	0.0684	0.0368	0.0453	0.0453
D ↓	hold_rising to CP	-0.1018	-0.0410	-0.0413	-0.0382
D ↑	hold_rising to CP	-0.0405	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1577	0.1027	0.1020	0.1020
D ↑	setup_rising to CP	0.0756	0.0436	0.0466	0.0466
RN ↓	min_pulse_width to RN	0.0916	0.0898	0.1013	0.1084
RN ↑	recovery_rising to CP	0.0296	0.0290	0.0293	0.0293
RN ↑	removal_rising to CP	-0.0197	-0.0145	-0.0148	-0.0148
TE ↓	hold_rising to CP	-0.0645	-0.0361	-0.0361	-0.0361
TE ↑	hold_rising to CP	-0.0525	-0.0334	-0.0334	-0.0334
TE ↓	setup_rising to CP	0.1368	0.1002	0.1002	0.1002
TE ↑	setup_rising to CP	0.2570	0.1981	0.2006	0.2006
TI ↓	hold_rising to CP	-0.1967	-0.1139	-0.1124	-0.1124
TI ↑	hold_rising to CP	-0.0609	-0.0352	-0.0352	-0.0352
TI ↓	setup_rising to CP	0.2661	0.1915	0.1909	0.1909
TI ↑	setup_rising to CP	0.0969	0.0752	0.0752	0.0752

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	4.086e-07	8.167e-12
X8_P10	4.209e-07	7.820e-12
X17_P10	5.118e-07	8.072e-12
X33_P10	5.965e-07	8.576e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.406e-03	4.370e-03	4.357e-03	4.350e-03

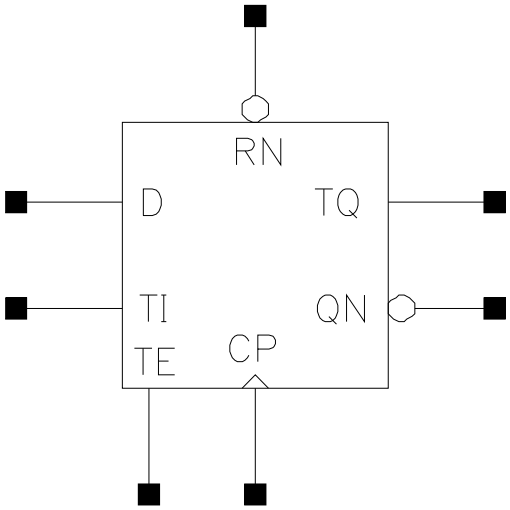
Clock 100Mhz Data 25Mhz	6.624e-03	6.680e-03	7.303e-03	7.931e-03
Clock 100Mhz Data 50Mhz	8.843e-03	8.989e-03	1.025e-02	1.151e-02
Clock = 0 Data 100Mhz	5.196e-03	4.862e-03	4.755e-03	4.702e-03
Clock = 1 Data 100Mhz	1.437e-03	7.599e-04	5.344e-04	4.218e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

RN	0.0011	0.0007	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1030	0.0881	3.6730	2.0162
CP to QN ↑	0.1465	0.0740	6.6997	3.7662
CP to TQ ↓	0.1047	0.0509	5.0108	3.9159
CP to TQ ↑	0.0842	0.0688	11.7651	10.8814
RN to QN ↑	0.0990	0.0989	6.7806	3.7573
RN to TQ ↓	0.0690	0.0677	4.3722	4.1557
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0908	0.0975	1.0048	0.5340
CP to QN ↑	0.0749	0.0787	1.8847	0.9479
CP to TQ ↓	0.0531	0.0553	4.8845	4.7841
CP to TQ ↑	0.0688	0.0705	10.1982	10.3490
RN to QN ↑	0.1020	0.1082	1.8818	0.9462
RN to TQ ↓	0.0725	0.0760	5.1236	5.0456

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1625	0.1547	0.1552	0.1552
CP ↑	min_pulse_width to CP	0.0975	0.0405	0.0405	0.0454
D ↓	hold_rising to CP	-0.0987	-0.0410	-0.0410	-0.0382
D ↑	hold_rising to CP	-0.0405	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1577	0.1024	0.1020	0.1020
D ↑	setup_rising to CP	0.0756	0.0436	0.0491	0.0491
RN ↓	min_pulse_width to RN	0.0964	0.0964	0.0991	0.1040
RN ↑	recovery_rising to CP	0.0296	0.0293	0.0297	0.0297
RN ↑	removal_rising to CP	-0.0218	-0.0148	-0.0148	-0.0148
TE ↓	hold_rising to CP	-0.0645	-0.0361	-0.0361	-0.0361
TE ↑	hold_rising to CP	-0.0525	-0.0334	-0.0334	-0.0334
TE ↓	setup_rising to CP	0.1368	0.1002	0.1002	0.1002
TE ↑	setup_rising to CP	0.2570	0.1981	0.2006	0.2006
TI ↓	hold_rising to CP	-0.1972	-0.1124	-0.1124	-0.1124
TI ↑	hold_rising to CP	-0.0609	-0.0352	-0.0352	-0.0352
TI ↓	setup_rising to CP	0.2661	0.1915	0.1909	0.1909
TI ↑	setup_rising to CP	0.0969	0.0752	0.0747	0.0747

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	4.310e-07	8.325e-12
X8_P10	4.433e-07	7.820e-12
X17_P10	4.990e-07	8.323e-12
X33_P10	5.997e-07	8.828e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

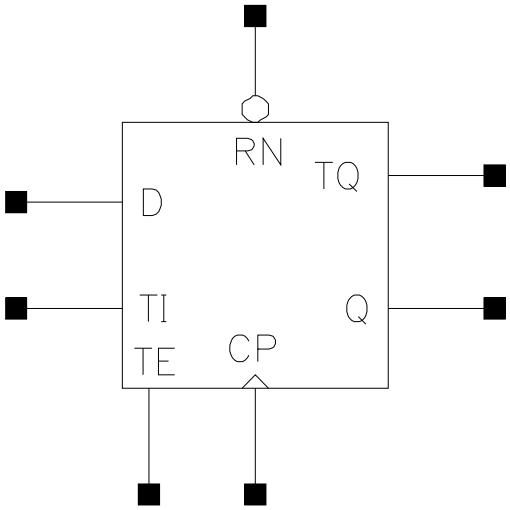
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.421e-03	4.411e-03	4.430e-03	4.440e-03
Clock 100Mhz Data 25Mhz	6.835e-03	6.881e-03	7.225e-03	7.967e-03
Clock 100Mhz Data 50Mhz	9.249e-03	9.351e-03	1.002e-02	1.149e-02
Clock = 0 Data 100Mhz	5.165e-03	4.833e-03	4.718e-03	4.661e-03
Clock = 1 Data 100Mhz	1.435e-03	7.690e-04	5.470e-04	4.361e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

RN	0.0008	0.0009	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1227	0.0605	5.1281	2.1307
CP to Q ↑	0.0866	0.0709	8.0095	3.8683
CP to TQ ↓	0.1201	0.0622	6.3045	5.2023
CP to TQ ↑	0.0898	0.0749	15.9704	14.4805
RN to Q ↓	0.0920	0.0855	4.1814	2.2655
RN to TQ ↓	0.0911	0.0877	5.3054	5.4500
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0836	0.0911	0.9979	0.5303
CP to Q ↑	0.1017	0.1069	1.8355	0.9366
CP to TQ ↓	0.0872	0.0976	4.9124	4.9973
CP to TQ ↑	0.1082	0.1166	14.2204	14.2924
RN to Q ↓	0.1163	0.1238	0.9952	0.5288
RN to TQ ↓	0.1199	0.1303	4.9093	4.9944

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1625	0.1547	0.1547	0.1547
CP ↑	min_pulse_width to CP	0.1072	0.0453	0.0368	0.0368
D ↓	hold_rising to CP	-0.0987	-0.0382	-0.0410	-0.0410
D ↑	hold_rising to CP	-0.0405	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1584	0.1027	0.1024	0.1024
D ↑	setup_rising to CP	0.0756	0.0466	0.0436	0.0436
RN ↓	min_pulse_width to RN	0.0964	0.1067	0.0898	0.0898
RN ↑	recovery_rising to CP	0.0297	0.0290	0.0297	0.0297
RN ↑	removal_rising to CP	-0.0197	-0.0145	-0.0148	-0.0148
TE ↓	hold_rising to CP	-0.0676	-0.0361	-0.0361	-0.0361
TE ↑	hold_rising to CP	-0.0556	-0.0334	-0.0334	-0.0334
TE ↓	setup_rising to CP	0.1312	0.1002	0.1002	0.1002
TE ↑	setup_rising to CP	0.2539	0.1981	0.2006	0.2006
TI ↓	hold_rising to CP	-0.1972	-0.1129	-0.1139	-0.1178
TI ↑	hold_rising to CP	-0.0609	-0.0352	-0.0352	-0.0352
TI ↓	setup_rising to CP	0.2607	0.1909	0.1909	0.1909
TI ↑	setup_rising to CP	0.0969	0.0752	0.0752	0.0754

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	4.257e-07	8.324e-12
X8_P10	4.402e-07	7.820e-12
X17_P10	5.329e-07	8.324e-12
X33_P10	6.232e-07	8.828e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

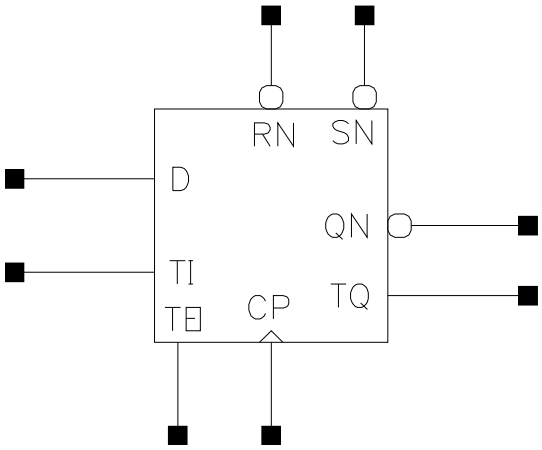
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.472e-03	4.511e-03	4.524e-03	4.530e-03
Clock 100Mhz Data 25Mhz	6.814e-03	6.870e-03	7.758e-03	8.418e-03
Clock 100Mhz Data 50Mhz	9.156e-03	9.229e-03	1.099e-02	1.231e-02
Clock = 0 Data 100Mhz	5.166e-03	4.834e-03	4.723e-03	4.668e-03
Clock = 1 Data 100Mhz	1.435e-03	7.306e-04	4.957e-04	3.783e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.352	5.2224
X17_P10	1.200	4.488	5.3856
X33_P10	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0008	0.0008	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0971	0.1034	1.9571	1.0148
CP to QN ↑	0.0779	0.0814	3.6377	1.8396
CP to TQ ↓	0.0597	0.0596	6.1794	6.1761
CP to TQ ↑	0.0799	0.0799	18.8471	18.8620
RN to QN ↓	0.1062	0.1127	1.9556	1.0155
RN to QN ↑	0.1112	0.1164	3.6411	1.8425
RN to TQ ↓	0.0855	0.0853	6.7274	6.7200
RN to TQ ↑	0.0896	0.0896	18.8171	18.8251
SN to QN ↓	0.1143	0.1217	1.9667	1.0182
SN to TQ ↑	0.0950	0.0948	19.0204	19.0291
	X33_P10		**X33_P10**	
CP to QN ↓	0.1191		0.5482	
CP to QN ↑	0.0900		0.9427	
CP to TQ ↓	0.0597		6.1993	
CP to TQ ↑	0.0802		18.8959	
RN to QN ↓	0.1281		0.5485	
RN to QN ↑	0.1281		0.9441	
RN to TQ ↓	0.0853		6.7558	
RN to TQ ↑	0.0899		18.8722	
SN to QN ↓	0.1390		0.5489	
SN to TQ ↑	0.0952		19.1118	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1601	0.1601	0.1620
CP ↑	min_pulse_width to CP	0.0453	0.0453	0.0502
D ↓	hold_rising to CP	-0.0410	-0.0413	-0.0410
D ↑	hold_rising to CP	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1072	0.1072	0.1072
D ↑	setup_rising to CP	0.0488	0.0488	0.0488
RN ↓	min_pulse_width to RN	0.1062	0.1089	0.1160
RN ↑	non_seq_hold_rising to SN	-0.0381	-0.0381	-0.0381
RN ↑	non_seq_setup_rising to SN	0.0907	0.0907	0.0907
RN ↑	recovery_rising to CP	0.0442	0.0442	0.0442
RN ↑	removal_rising to CP	-0.0246	-0.0246	-0.0246
SN ↓	min_pulse_width to SN	0.0859	0.0886	0.0913
SN ↑	recovery_rising to CP	0.0177	0.0177	0.0177
SN ↑	removal_rising to CP	0.0384	0.0384	0.0384

TE ↓	hold_rising to CP	-0.0361	-0.0361	-0.0361
TE ↑	hold_rising to CP	-0.0334	-0.0334	-0.0334
TE ↓	setup_rising to CP	0.1051	0.1051	0.1051
TE ↑	setup_rising to CP	0.2055	0.2055	0.2055
TI ↓	hold_rising to CP	-0.1124	-0.1124	-0.1124
TI ↑	hold_rising to CP	-0.0352	-0.0352	-0.0352
TI ↓	setup_rising to CP	0.1958	0.1958	0.1958
TI ↑	setup_rising to CP	0.0803	0.0803	0.0803

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	5.036e-07	8.856e-12
X17_P10	5.507e-07	9.108e-12
X33_P10	6.375e-07	9.615e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

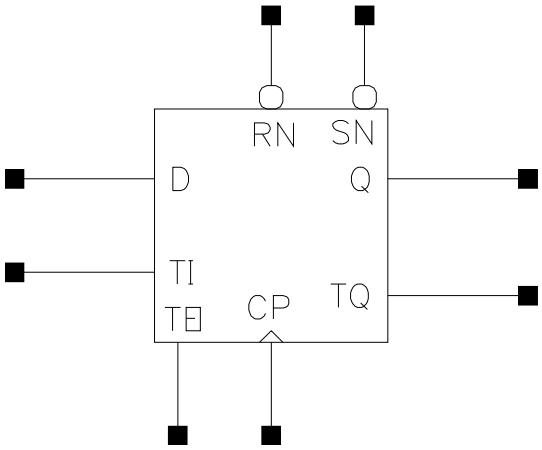
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.630e-03	4.630e-03	4.631e-03
Clock 100Mhz Data 25Mhz	7.181e-03	7.476e-03	8.194e-03
Clock 100Mhz Data 50Mhz	9.733e-03	1.032e-02	1.176e-02
Clock = 0 Data 100Mhz	4.734e-03	4.732e-03	4.732e-03
Clock = 1 Data 100Mhz	1.628e-04	1.629e-04	1.626e-04

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.216	5.0592
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0662	0.0743	2.0667	1.0833
CP to Q ↑	0.0774	0.0811	3.7233	1.8953
CP to TQ ↓	0.0696	0.0807	6.2858	6.3697
CP to TQ ↑	0.0858	0.0943	18.3767	18.4942
RN to Q ↓	0.0974	0.1120	2.3989	1.2655
RN to Q ↑	0.0684	0.0760	3.8566	1.9743
RN to TQ ↓	0.1023	0.1211	6.9034	7.0916
RN to TQ ↑	0.0819	0.0973	18.5348	18.6754
SN to Q ↑	0.0940	0.1014	3.8565	1.9735
SN to TQ ↑	0.1075	0.1227	18.5385	18.6788
	X33_P10		**X33_P10**	
CP to Q ↓	0.0942		0.5942	
CP to Q ↑	0.0914		0.9841	
CP to TQ ↓	0.1005		6.6315	
CP to TQ ↑	0.1100		18.6989	
RN to Q ↓	0.1473		0.7091	
RN to Q ↑	0.0958		1.0380	
RN to TQ ↓	0.1545		7.5729	
RN to TQ ↑	0.1266		18.9330	
SN to Q ↑	0.1210		1.0384	
SN to TQ ↑	0.1517		18.9397	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1601	0.1601	0.1620
CP ↑	min_pulse_width to CP	0.0502	0.0587	0.0829
D ↓	hold_rising to CP	-0.0382	-0.0382	-0.0386
D ↑	hold_rising to CP	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1075	0.1075	0.1075
D ↑	setup_rising to CP	0.0488	0.0488	0.0488
RN ↓	min_pulse_width to RN	0.1138	0.1355	0.1746
RN ↑	non_seq_hold_rising to SN	-0.0431	-0.0502	-0.0676
RN ↑	non_seq_setup_rising to SN	0.0859	0.0859	0.1065
RN ↑	recovery_rising to CP	0.0394	0.0394	0.0394
RN ↑	removal_rising to CP	-0.0193	-0.0193	-0.0193
SN ↓	min_pulse_width to SN	0.0913	0.0989	0.1260
SN ↑	recovery_rising to CP	0.0177	0.0177	0.0177
SN ↑	removal_rising to CP	0.0384	0.0384	0.0384

TE ↓	hold_rising to CP	-0.0361	-0.0364	-0.0364
TE ↑	hold_rising to CP	-0.0334	-0.0334	-0.0334
TE ↓	setup_rising to CP	0.1051	0.1051	0.1051
TE ↑	setup_rising to CP	0.2055	0.2055	0.2055
TI ↓	hold_rising to CP	-0.1129	-0.1129	-0.1129
TI ↑	hold_rising to CP	-0.0352	-0.0352	-0.0352
TI ↓	setup_rising to CP	0.1958	0.1958	0.1958
TI ↑	setup_rising to CP	0.0803	0.0803	0.0803

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P10	4.984e-07	8.595e-12
X17_P10	5.468e-07	8.846e-12
X33_P10	6.371e-07	9.351e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

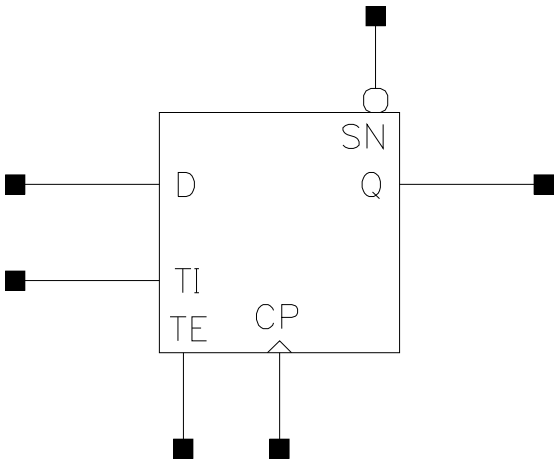
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.603e-03	4.604e-03	4.604e-03
Clock 100Mhz Data 25Mhz	7.020e-03	7.326e-03	8.059e-03
Clock 100Mhz Data 50Mhz	9.437e-03	1.005e-02	1.151e-02
Clock = 0 Data 100Mhz	4.704e-03	4.704e-03	4.703e-03
Clock = 1 Data 100Mhz	1.139e-04	1.139e-04	1.139e-04

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0005	0.0005	0.0005
SN	0.0015	0.0015	0.0014	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P10			

CP	0.0010			
D	0.0005			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to Q ↓	0.1092	0.0580	4.8303	2.0496
CP to Q ↑	0.0848	0.0714	7.7790	3.7056
SN to Q ↑	0.0659	0.0744	7.6014	3.7140
	X17_P10	X25_P10	X17_P10	X25_P10
CP to Q ↓	0.0801	0.0843	0.9829	0.6853
CP to Q ↑	0.1013	0.1044	1.8295	1.2421
SN to Q ↑	0.1042	0.1073	1.8285	1.2422
	X33_P10		X33_P10	
CP to Q ↓	0.0876		0.5226	
CP to Q ↑	0.1063		0.9335	
SN to Q ↑	0.1092		0.9339	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.1649	0.1606	0.1625	0.1606
CP ↑	min_pulse_width to CP	0.0927	0.0443	0.0357	0.0357
D ↓	hold_rising to CP	-0.1018	-0.0431	-0.0462	-0.0431
D ↑	hold_rising to CP	-0.0379	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1633	0.1069	0.1069	0.1069
D ↑	setup_rising to CP	0.0703	0.0390	0.0390	0.0390
SN ↓	min_pulse_width to SN	0.0588	0.0686	0.0686	0.0686
SN ↑	recovery_rising to CP	0.0177	0.0177	0.0177	0.0177
SN ↑	removal_rising to CP	0.0286	0.0363	0.0363	0.0363
TE ↓	hold_rising to CP	-0.0645	-0.0413	-0.0410	-0.0410
TE ↑	hold_rising to CP	-0.0503	-0.0286	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1361	0.1051	0.1051	0.1051
TE ↑	setup_rising to CP	0.2592	0.2048	0.2048	0.2048
TI ↓	hold_rising to CP	-0.1972	-0.1188	-0.1227	-0.1227
TI ↑	hold_rising to CP	-0.0560	-0.0303	-0.0303	-0.0303
TI ↓	setup_rising to CP	0.2661	0.2014	0.2014	0.2014
TI ↑	setup_rising to CP	0.0920	0.0650	0.0650	0.0650
		X33_P10			

CP ↓	min_pulse_width to CP	0.1606			
CP ↑	min_pulse_width to CP	0.0357			
D ↓	hold_rising to CP	-0.0462			
D ↑	hold_rising to CP	-0.0090			
D ↓	setup_rising to CP	0.1069			
D ↑	setup_rising to CP	0.0390			
SN ↓	min_pulse_width to SN	0.0686			
SN ↑	recovery_rising to CP	0.0177			
SN ↑	removal_rising to CP	0.0363			
TE ↓	hold_rising to CP	-0.0410			
TE ↑	hold_rising to CP	-0.0286			
TE ↓	setup_rising to CP	0.1051			
TE ↑	setup_rising to CP	0.2048			
TI ↓	hold_rising to CP	-0.1227			
TI ↑	hold_rising to CP	-0.0303			
TI ↓	setup_rising to CP	0.2014			
TI ↑	setup_rising to CP	0.0650			

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	4.162e-07	8.072e-12
X8_P10	4.365e-07	7.820e-12
X17_P10	5.290e-07	8.325e-12
X25_P10	5.714e-07	8.577e-12
X33_P10	6.137e-07	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	4.342e-03	4.370e-03	4.380e-03	4.384e-03
Clock 100Mhz Data 25Mhz	6.540e-03	6.664e-03	7.456e-03	7.823e-03
Clock 100Mhz Data 50Mhz	8.739e-03	8.958e-03	1.053e-02	1.126e-02
Clock = 0 Data 100Mhz	5.051e-03	4.805e-03	4.724e-03	4.683e-03
Clock = 1 Data 100Mhz	1.436e-03	7.624e-04	5.379e-04	4.257e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	4.387e-03			

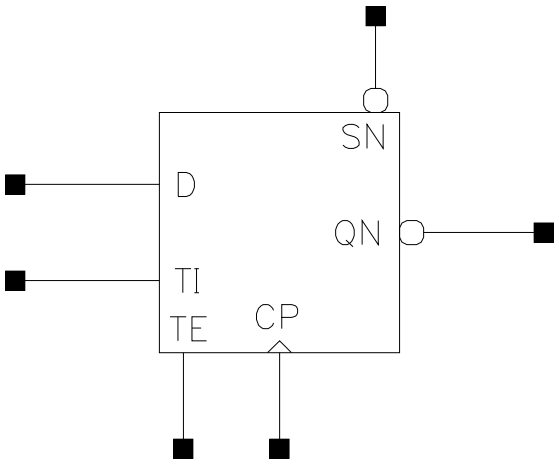
Clock 100Mhz Data 25Mhz	8.093e-03			
Clock 100Mhz Data 50Mhz	1.180e-02			
Clock = 0 Data 100Mhz	4.659e-03			
Clock = 1 Data 100Mhz	3.584e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0005	0.0005	0.0005
SN	0.0015	0.0014	0.0015	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P10			

CP	0.0010			
D	0.0005			
SN	0.0015			
TE	0.0010			
TI	0.0004			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0963	0.0859	3.6734	1.9177
CP to QN ↑	0.1123	0.0652	7.5253	3.6366
SN to QN ↓	0.0791	0.0885	3.6576	1.9164
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
CP to QN ↓	0.0892	0.0942	0.9870	0.6876
CP to QN ↑	0.0788	0.0832	1.8305	1.2431
SN to QN ↓	0.0934	0.0986	0.9863	0.6868
	X33_P10		**X33_P10**	
CP to QN ↓	0.0981		0.5246	
CP to QN ↑	0.0859		0.9336	
SN to QN ↓	0.1024		0.5242	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.1649	0.1625	0.1606	0.1625
CP ↑	min_pulse_width to CP	0.0684	0.0357	0.0454	0.0491
D ↓	hold_rising to CP	-0.1043	-0.0428	-0.0431	-0.0435
D ↑	hold_rising to CP	-0.0379	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1633	0.1069	0.1069	0.1069
D ↑	setup_rising to CP	0.0703	0.0390	0.0390	0.0390
SN ↓	min_pulse_width to SN	0.0588	0.0659	0.0735	0.0735
SN ↑	recovery_rising to CP	0.0177	0.0177	0.0177	0.0177
SN ↑	removal_rising to CP	0.0286	0.0363	0.0363	0.0363
TE ↓	hold_rising to CP	-0.0645	-0.0410	-0.0413	-0.0413
TE ↑	hold_rising to CP	-0.0503	-0.0286	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1361	0.1051	0.1051	0.1051
TE ↑	setup_rising to CP	0.2592	0.2048	0.2048	0.2048
TI ↓	hold_rising to CP	-0.1967	-0.1227	-0.1173	-0.1173
TI ↑	hold_rising to CP	-0.0560	-0.0303	-0.0303	-0.0303
TI ↓	setup_rising to CP	0.2661	0.2014	0.2014	0.2014
TI ↑	setup_rising to CP	0.0920	0.0650	0.0650	0.0650
		X33_P10			

CP ↓	min_pulse_width to CP	0.1606			
CP ↑	min_pulse_width to CP	0.0502			
D ↓	hold_rising to CP	-0.0435			
D ↑	hold_rising to CP	-0.0090			
D ↓	setup_rising to CP	0.1069			
D ↑	setup_rising to CP	0.0390			
SN ↓	min_pulse_width to SN	0.0762			
SN ↑	recovery_rising to CP	0.0177			
SN ↑	removal_rising to CP	0.0363			
TE ↓	hold_rising to CP	-0.0413			
TE ↑	hold_rising to CP	-0.0286			
TE ↓	setup_rising to CP	0.1051			
TE ↑	setup_rising to CP	0.2048			
TI ↓	hold_rising to CP	-0.1173			
TI ↑	hold_rising to CP	-0.0303			
TI ↓	setup_rising to CP	0.2014			
TI ↑	setup_rising to CP	0.0650			

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	4.169e-07	8.072e-12
X8_P10	4.371e-07	7.821e-12
X17_P10	5.307e-07	8.325e-12
X25_P10	5.758e-07	8.576e-12
X33_P10	6.210e-07	8.828e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	4.327e-03	4.361e-03	4.369e-03	4.372e-03
Clock 100Mhz Data 25Mhz	6.502e-03	6.659e-03	7.407e-03	7.773e-03
Clock 100Mhz Data 50Mhz	8.678e-03	8.957e-03	1.044e-02	1.117e-02
Clock = 0 Data 100Mhz	5.050e-03	4.810e-03	4.727e-03	4.686e-03
Clock = 1 Data 100Mhz	1.437e-03	7.667e-04	5.434e-04	4.318e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	4.375e-03			

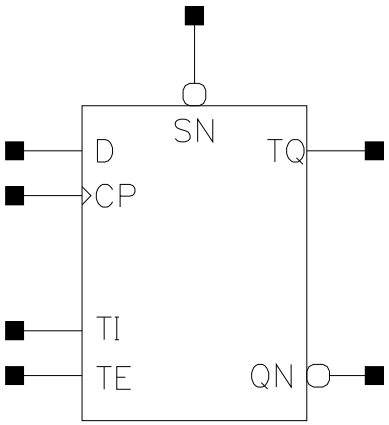
Clock 100Mhz Data 25Mhz	8.045e-03			
Clock 100Mhz Data 50Mhz	1.172e-02			
Clock = 0 Data 100Mhz	4.661e-03			
Clock = 1 Data 100Mhz	3.648e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.216	5.0592
X8_P10	1.200	4.080	4.8960
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0005	0.0005	0.0005

SN	0.0016	0.0016	0.0016	0.0016
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1107	0.0901	3.6578	1.9233
CP to QN ↑	0.1480	0.0746	7.3860	3.7086
CP to TQ ↓	0.1063	0.0520	5.6963	4.5403
CP to TQ ↑	0.0848	0.0677	10.3886	10.1414
SN to QN ↓	0.0750	0.0713	3.6572	1.9272
SN to TQ ↑	0.0525	0.0543	10.2297	10.1710
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0895	0.0985	1.0106	0.5177
CP to QN ↑	0.0854	0.0931	1.8418	0.9386
CP to TQ ↓	0.0652	0.0651	4.7702	4.7725
CP to TQ ↑	0.0757	0.0757	10.2062	10.2345
SN to QN ↓	0.0781	0.0869	1.0115	0.5168
SN to TQ ↑	0.0637	0.0637	10.2034	10.2399

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1667	0.1625	0.1625	0.1625
CP ↑	min_pulse_width to CP	0.0975	0.0405	0.0502	0.0550
D ↓	hold_rising to CP	-0.1018	-0.0431	-0.0435	-0.0435
D ↑	hold_rising to CP	-0.0379	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1633	0.1069	0.1069	0.1069
D ↑	setup_rising to CP	0.0703	0.0390	0.0390	0.0390
SN ↓	min_pulse_width to SN	0.0540	0.0562	0.0588	0.0615
SN ↑	recovery_rising to CP	0.0177	0.0146	0.0146	0.0146
SN ↑	removal_rising to CP	0.0286	0.0363	0.0363	0.0363
TE ↓	hold_rising to CP	-0.0645	-0.0410	-0.0413	-0.0413
TE ↑	hold_rising to CP	-0.0503	-0.0286	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1361	0.1051	0.1051	0.1051
TE ↑	setup_rising to CP	0.2592	0.2048	0.2048	0.2048
TI ↓	hold_rising to CP	-0.1972	-0.1229	-0.1173	-0.1173
TI ↑	hold_rising to CP	-0.0560	-0.0303	-0.0303	-0.0303
TI ↓	setup_rising to CP	0.2661	0.2014	0.2014	0.2014
TI ↑	setup_rising to CP	0.0920	0.0650	0.0650	0.0650

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	4.438e-07	8.576e-12
X8_P10	4.640e-07	8.325e-12
X17_P10	5.576e-07	8.829e-12
X33_P10	6.479e-07	9.333e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

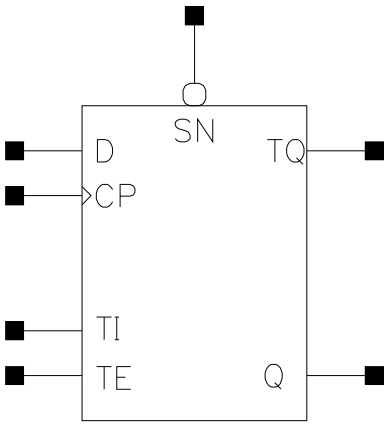
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.338e-03	4.434e-03	4.466e-03	4.483e-03
Clock 100Mhz Data 25Mhz	6.796e-03	6.954e-03	7.626e-03	8.276e-03
Clock 100Mhz Data 50Mhz	9.254e-03	9.474e-03	1.078e-02	1.207e-02
Clock = 0 Data 100Mhz	5.053e-03	4.805e-03	4.722e-03	4.681e-03
Clock = 1 Data 100Mhz	1.434e-03	7.348e-04	5.019e-04	3.855e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.944	4.7328
X17_P10	1.200	4.216	5.0592
X33_P10	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0005	0.0005	0.0005

SN	0.0016	0.0014	0.0014	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1258	0.0624	4.9951	2.1020
CP to Q ↑	0.0903	0.0738	7.8264	3.7552
CP to TQ ↓	0.1260	0.0663	7.1252	5.2149
CP to TQ ↑	0.0893	0.0817	10.4545	14.5889
SN to Q ↑	0.0557	0.0774	7.6279	3.7593
SN to TQ ↑	0.0548	0.0864	10.2529	14.5735
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0822	0.0896	1.0140	0.5324
CP to Q ↑	0.1029	0.1078	1.8378	0.9374
CP to TQ ↓	0.0859	0.0961	4.9107	4.9855
CP to TQ ↑	0.1094	0.1174	14.2321	14.3015
SN to Q ↑	0.1057	0.1106	1.8365	0.9375
SN to TQ ↑	0.1123	0.1202	14.2304	14.3018

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1625	0.1601	0.1625	0.1606
CP ↑	min_pulse_width to CP	0.1072	0.0454	0.0357	0.0358
D ↓	hold_rising to CP	-0.1018	-0.0435	-0.0462	-0.0462
D ↑	hold_rising to CP	-0.0409	-0.0090	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1633	0.1069	0.1069	0.1069
D ↑	setup_rising to CP	0.0703	0.0390	0.0390	0.0390
SN ↓	min_pulse_width to SN	0.0513	0.0762	0.0686	0.0686
SN ↑	recovery_rising to CP	0.0180	0.0177	0.0177	0.0177
SN ↑	removal_rising to CP	0.0286	0.0363	0.0363	0.0363
TE ↓	hold_rising to CP	-0.0645	-0.0413	-0.0410	-0.0410
TE ↑	hold_rising to CP	-0.0503	-0.0286	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1365	0.1051	0.1051	0.1051
TE ↑	setup_rising to CP	0.2567	0.2048	0.2048	0.2048
TI ↓	hold_rising to CP	-0.1972	-0.1173	-0.1227	-0.1227
TI ↑	hold_rising to CP	-0.0560	-0.0303	-0.0303	-0.0303
TI ↓	setup_rising to CP	0.2661	0.2014	0.2014	0.2014
TI ↑	setup_rising to CP	0.0920	0.0650	0.0650	0.0650

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	4.359e-07	8.324e-12
X8_P10	4.541e-07	8.073e-12
X17_P10	5.459e-07	8.577e-12
X33_P10	6.305e-07	9.081e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

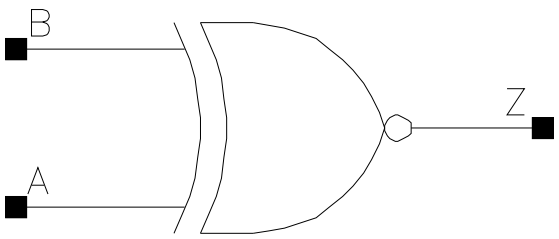
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	4.333e-03	4.438e-03	4.472e-03	4.489e-03
Clock 100Mhz Data 25Mhz	6.687e-03	6.889e-03	7.742e-03	8.413e-03
Clock 100Mhz Data 50Mhz	9.041e-03	9.340e-03	1.101e-02	1.234e-02
Clock = 0 Data 100Mhz	5.051e-03	4.797e-03	4.714e-03	4.671e-03
Clock = 1 Data 100Mhz	1.437e-03	7.363e-04	5.028e-04	3.862e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P10	X8_P10	X17_P10	X25_P10
A	0.0017	0.0007	0.0010	0.0015
B	0.0015	0.0015	0.0019	0.0025
	X33_P10			
A	0.0017			
B	0.0029			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X8_P10**	**X6_P10**	**X8_P10**
A to Z ↓	0.0266	0.0629	3.6410	2.0896
A to Z ↑	0.0292	0.0530	6.0511	3.8319
B to Z ↓	0.0251	0.0439	3.6360	2.0789
B to Z ↑	0.0287	0.0396	6.0645	3.8207
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
A to Z ↓	0.0598	0.0601	1.0344	0.7147
A to Z ↑	0.0487	0.0497	1.8768	1.2488

B to Z ↓	0.0456	0.0448	1.0322	0.7135
B to Z ↑	0.0393	0.0387	1.8745	1.2458
	X33_P10		**X33_P10**	
A to Z ↓	0.0567		0.5361	
A to Z ↑	0.0479		0.9379	
B to Z ↓	0.0430		0.5356	
B to Z ↑	0.0382		0.9369	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P10	1.683e-07	2.529e-12
X8_P10	1.726e-07	3.282e-12
X17_P10	2.649e-07	3.534e-12
X25_P10	4.280e-07	5.046e-12
X33_P10	5.400e-07	5.299e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	2.761e-03	4.910e-03	6.803e-03	1.107e-02
B to Z	2.532e-03	3.358e-03	5.032e-03	8.039e-03
	X33_P10			
A to Z	1.338e-02			
B to Z	1.000e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

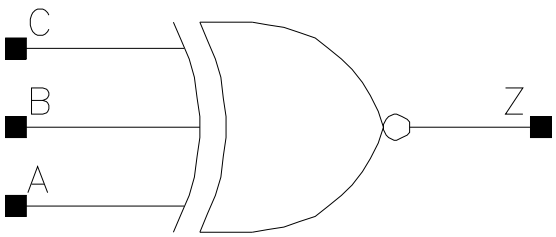
Pin Cycle (vdds)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	-1.724e-05	-2.582e-07	-7.773e-08	-5.818e-07
B to Z	1.180e-05	3.810e-08	-1.739e-07	-1.790e-07
	X33_P10			
A to Z	-6.676e-07			
B to Z	-5.588e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	2.176	2.6112
X16_P10	1.200	2.720	3.2640
X25_P10	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X16_P10	X25_P10
A	0.0029	0.0024	0.0030	0.0044
B	0.0032	0.0022	0.0030	0.0040
C	0.0020	0.0007	0.0007	0.0008

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0435	0.0741	4.3694	2.2372
A to Z ↑	0.0416	0.0657	8.9223	3.7928
B to Z ↓	0.0442	0.0737	4.3664	2.2359
B to Z ↑	0.0415	0.0655	8.9117	3.7940
C to Z ↓	0.0429	0.0955	4.3667	2.2345
C to Z ↑	0.0398	0.0859	8.8781	3.7949
	X16_P10	**X25_P10**	**X16_P10**	**X25_P10**
A to Z ↓	0.0739	0.0737	1.1484	0.7356
A to Z ↑	0.0709	0.0704	1.9888	1.2532
B to Z ↓	0.0737	0.0743	1.1477	0.7345

B to Z ↑	0.0708	0.0716	1.9889	1.2533
C to Z ↓	0.1001	0.1060	1.1468	0.7344
C to Z ↑	0.0955	0.1018	1.9880	1.2533

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	2.973e-07	4.545e-12
X8_P10	2.751e-07	4.811e-12
X16_P10	4.108e-07	5.802e-12
X25_P10	5.971e-07	8.073e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	3.082e-03	3.913e-03	6.248e-03	9.340e-03
B to Z	2.824e-03	3.807e-03	6.084e-03	9.154e-03
C to Z	2.728e-03	5.906e-03	8.680e-03	1.302e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

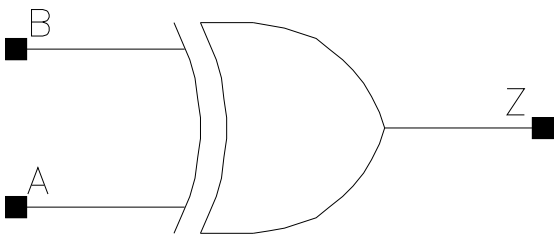
Pin Cycle (vdds)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	-4.445e-05	-1.486e-05	-2.464e-05	-3.748e-05
B to Z	-2.247e-06	-9.936e-06	-8.015e-06	-9.825e-06
C to Z	1.069e-05	4.880e-06	2.502e-06	8.103e-07

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.224	1.4688
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.224	1.4688
X16_P10	1.200	1.360	1.6320
X25_P10	1.200	2.176	2.6112
X31_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X16_P10
A	0.0008	0.0016	0.0010	0.0011
B	0.0013	0.0015	0.0015	0.0017
	X25_P10	X31_P10		
A	0.0015	0.0019		
B	0.0026	0.0034		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0562	0.0286	3.7410	2.7897
A to Z ↑	0.0499	0.0297	7.3229	7.9005
B to Z ↓	0.0401	0.0281	3.7296	2.8110
B to Z ↑	0.0390	0.0280	7.3216	7.9059
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0506	0.0526	2.0364	1.0575

A to Z ↑	0.0433	0.0454	3.7318	1.8805
B to Z ↓	0.0392	0.0406	2.0311	1.0558
B to Z ↑	0.0358	0.0376	3.7314	1.8804
	X25_P10	**X31_P10**	**X25_P10**	**X31_P10**
A to Z ↓	0.0562	0.0525	0.7087	0.5687
A to Z ↑	0.0484	0.0458	1.2464	1.0057
B to Z ↓	0.0432	0.0403	0.7081	0.5689
B to Z ↑	0.0375	0.0358	1.2468	1.0051

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	1.461e-07	3.032e-12
X6_P10	1.683e-07	2.529e-12
X8_P10	2.067e-07	3.032e-12
X16_P10	2.833e-07	3.284e-12
X25_P10	4.213e-07	4.792e-12
X31_P10	5.328e-07	5.047e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	3.790e-03	2.740e-03	4.510e-03	6.359e-03
B to Z	2.865e-03	2.448e-03	3.649e-03	5.207e-03
	X25_P10	X31_P10		
A to Z	9.924e-03	1.211e-02		
B to Z	6.861e-03	8.296e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

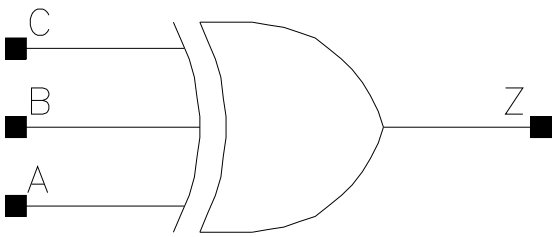
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	-2.060e-07	-2.465e-05	-3.988e-07	-4.888e-07
B to Z	-3.262e-07	7.311e-06	8.150e-08	3.201e-07
	X25_P10	X31_P10		
A to Z	-6.364e-07	-8.810e-07		
B to Z	-2.235e-07	1.690e-08		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X24_P10	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X24_P10
A	0.0024	0.0024	0.0030	0.0054
B	0.0025	0.0022	0.0028	0.0045
C	0.0008	0.0017	0.0023	0.0035

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0442	0.0740	4.6033	2.2367
A to Z ↑	0.0418	0.0655	9.7432	3.7914
B to Z ↓	0.0443	0.0737	4.6017	2.2343
B to Z ↑	0.0418	0.0654	9.7299	3.7922
C to Z ↓	0.0727	0.0716	4.5793	2.2338
C to Z ↑	0.0706	0.0629	9.7142	3.7901
	X17_P10	**X24_P10**	**X17_P10**	**X24_P10**
A to Z ↓	0.0674	0.0783	1.0653	0.7709
A to Z ↑	0.0649	0.0582	1.8478	1.2563
B to Z ↓	0.0671	0.0781	1.0643	0.7697

B to Z ↑	0.0647	0.0579	1.8491	1.2571
C to Z ↓	0.0660	0.0753	1.0639	0.7690
C to Z ↑	0.0633	0.0568	1.8481	1.2567

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P10	3.130e-07	4.544e-12
X8_P10	2.467e-07	4.292e-12
X17_P10	3.891e-07	4.541e-12
X24_P10	6.584e-07	7.820e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	2.780e-03	3.942e-03	6.053e-03	1.028e-02
B to Z	2.674e-03	3.788e-03	5.791e-03	9.873e-03
C to Z	5.584e-03	3.649e-03	5.721e-03	9.509e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	-2.440e-05	-1.882e-05	-3.404e-05	-6.276e-05
B to Z	-1.221e-05	-4.119e-06	-4.237e-06	-2.367e-05
C to Z	4.436e-06	3.223e-06	8.084e-06	2.907e-05

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