C28SOI_SC_12_COREPBP16_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 16 nm

Overview

- C28SOI_SC_12_COREPBP16_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

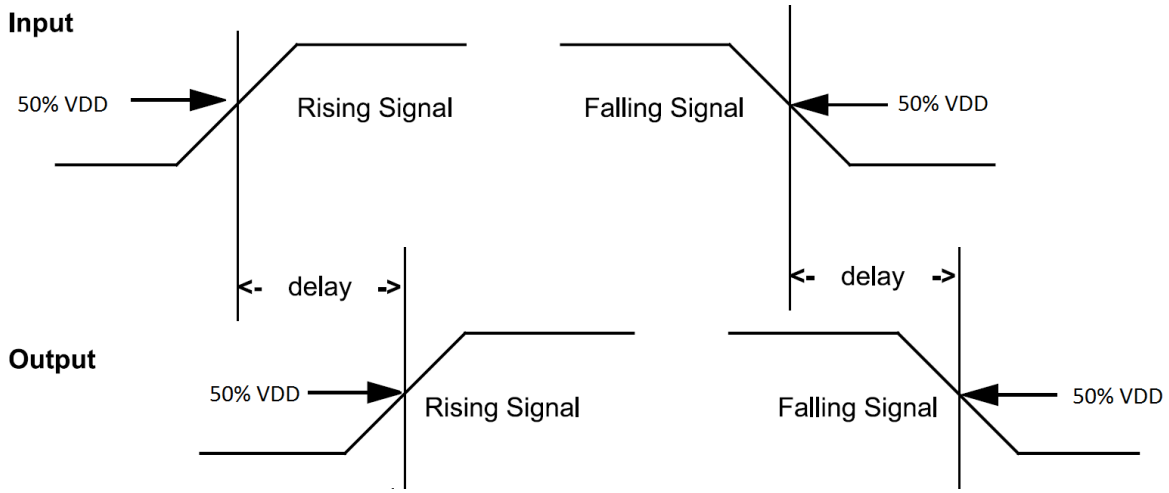


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

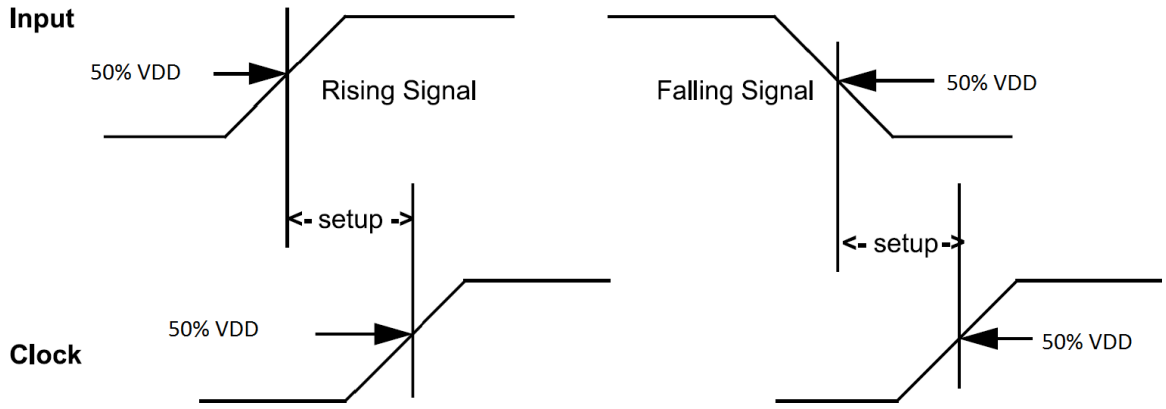


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

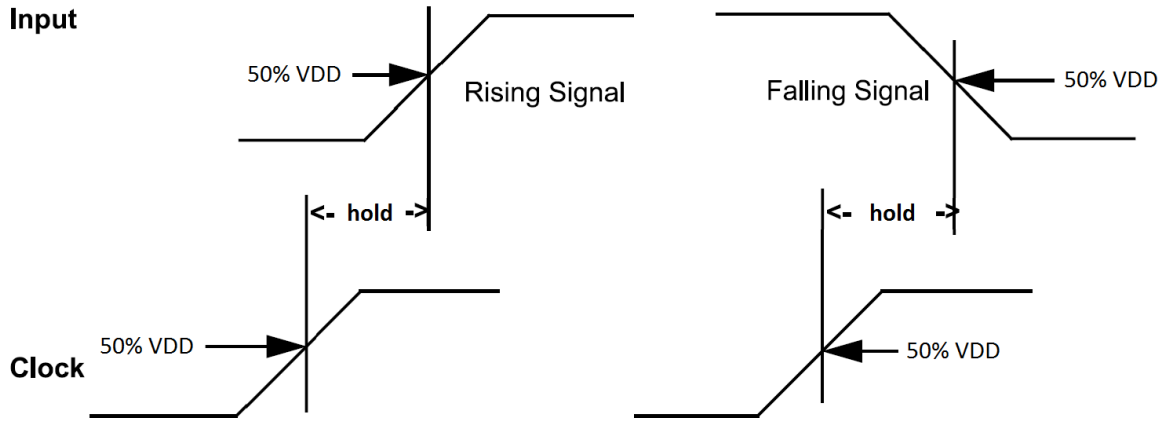


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

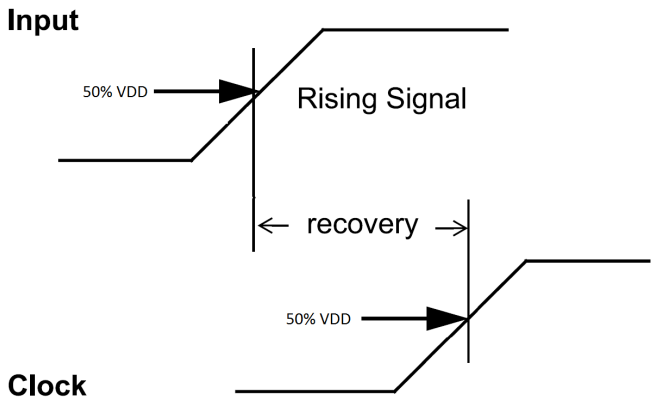


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

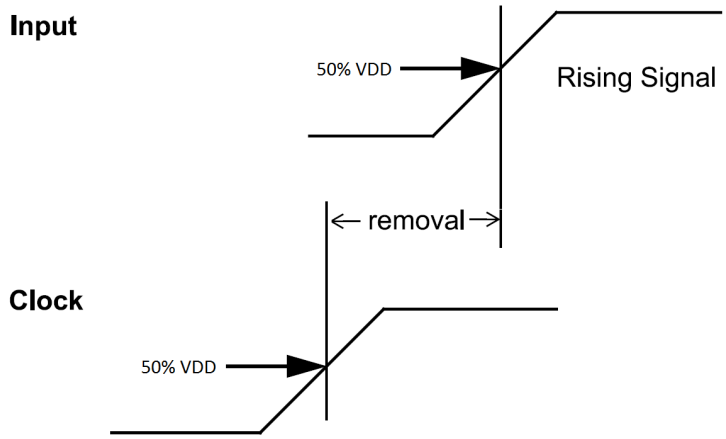


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

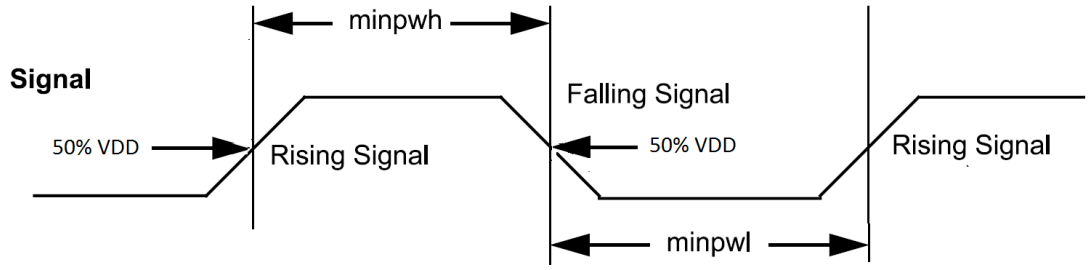


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

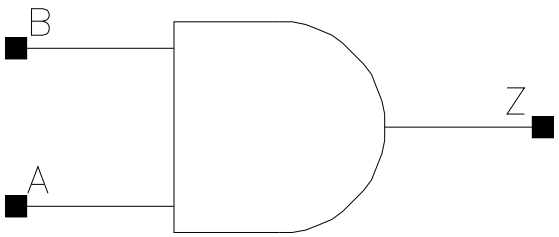
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X25_P16	1.200	1.088	1.3056
X33_P16	1.200	1.360	1.6320
X42_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0009	0.0014	0.0021	0.0026
B	0.0008	0.0013	0.0020	0.0026
	X42_P16			
A	0.0026			
B	0.0026			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0285	0.0239	1.7925	0.9089
A to Z ↑	0.0221	0.0214	2.7651	1.3451
B to Z ↓	0.0269	0.0223	1.7902	0.9077
B to Z ↑	0.0241	0.0232	2.7646	1.3455
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0247	0.0239	0.6004	0.4475

A to Z ↑	0.0210	0.0218	0.8872	0.6703
B to Z ↓	0.0232	0.0216	0.6009	0.4469
B to Z ↑	0.0227	0.0229	0.8880	0.6698
	X42_P16		**X42_P16**	
A to Z ↓	0.0261		0.3633	
A to Z ↑	0.0240		0.5368	
B to Z ↓	0.0239		0.3625	
B to Z ↑	0.0254		0.5366	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	1.671e-05	1.000e-20
X16_P16	3.510e-05	1.000e-20
X25_P16	5.195e-05	1.000e-20
X33_P16	7.145e-05	1.000e-20
X42_P16	8.327e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	1.238e-05	2.360e-05	3.737e-05	9.393e-05
B (output stable)	3.068e-05	5.397e-05	8.446e-05	3.897e-04
A to Z	3.820e-03	6.593e-03	1.019e-02	1.348e-02
B to Z	3.626e-03	6.260e-03	9.669e-03	1.243e-02
	X42_P16			
A (output stable)	9.505e-05			
B (output stable)	3.865e-04			
A to Z	1.648e-02			
B to Z	1.542e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

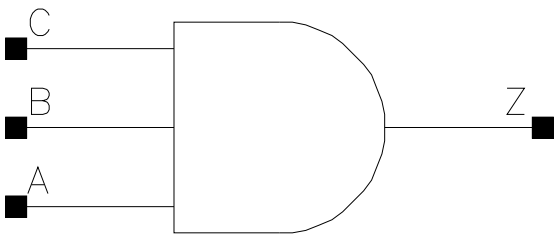
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X25_P16	1.200	1.360	1.6320
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0009	0.0014	0.0022	0.0027
B	0.0008	0.0013	0.0020	0.0025
C	0.0008	0.0013	0.0019	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0309	0.0263	1.8105	0.8853
A to Z ↑	0.0282	0.0272	2.7891	1.3331
B to Z ↓	0.0297	0.0249	1.8100	0.8841
B to Z ↑	0.0293	0.0282	2.7867	1.3320
C to Z ↓	0.0281	0.0233	1.8067	0.8830
C to Z ↑	0.0307	0.0292	2.7861	1.3334
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0264	0.0253	0.6072	0.4536

A to Z ↑	0.0266	0.0260	0.9086	0.6815
B to Z ↓	0.0252	0.0239	0.6059	0.4530
B to Z ↑	0.0277	0.0271	0.9094	0.6813
C to Z ↓	0.0235	0.0224	0.6058	0.4521
C to Z ↑	0.0288	0.0282	0.9091	0.6807

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	1.671e-05	1.000e-20
X17_P16	3.593e-05	1.000e-20
X25_P16	5.179e-05	1.000e-20
X33_P16	7.067e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	1.673e-05	3.373e-05	4.480e-05	6.132e-05
B (output stable)	3.913e-05	8.047e-05	1.128e-04	1.549e-04
C (output stable)	9.125e-05	1.788e-04	2.645e-04	3.656e-04
A to Z	4.259e-03	7.679e-03	1.125e-02	1.462e-02
B to Z	4.058e-03	7.315e-03	1.069e-02	1.387e-02
C to Z	3.873e-03	6.956e-03	1.014e-02	1.313e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

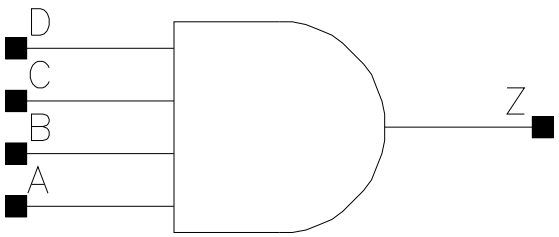
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X6_P16	1.200	1.088	1.3056
X20_P16	1.200	2.312	2.7744
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P16	X6_P16	X20_P16	X27_P16
A	0.0006	0.0010	0.0023	0.0026
B	0.0006	0.0009	0.0023	0.0026
C	0.0006	0.0010	0.0022	0.0026
D	0.0006	0.0009	0.0023	0.0026

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X6_P16	X4_P16	X6_P16
A to Z ↓	0.0314	0.0282	3.3158	2.1877
A to Z ↑	0.0280	0.0225	8.4842	4.6562
B to Z ↓	0.0302	0.0261	3.3152	2.1874
B to Z ↑	0.0301	0.0241	8.4852	4.6565
C to Z ↓	0.0321	0.0297	3.2886	2.1978
C to Z ↑	0.0281	0.0224	8.4883	4.6628

D to Z ↓	0.0308	0.0273	3.2854	2.1952
D to Z ↑	0.0307	0.0239	8.4917	4.6621
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0278	0.0257	0.6403	0.4528
A to Z ↑	0.0240	0.0271	1.5591	1.1856
B to Z ↓	0.0251	0.0234	0.6389	0.4524
B to Z ↑	0.0250	0.0283	1.5594	1.1853
C to Z ↓	0.0270	0.0247	0.6437	0.4542
C to Z ↑	0.0216	0.0240	1.5578	1.1833
D to Z ↓	0.0241	0.0226	0.6424	0.4536
D to Z ↑	0.0224	0.0253	1.5574	1.1827

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	9.103e-06	1.000e-20
X6_P16	2.086e-05	1.000e-20
X20_P16	6.339e-05	1.000e-20
X27_P16	8.242e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	6.443e-04	1.037e-03	3.066e-03	3.749e-03
B (output stable)	5.971e-04	9.418e-04	2.808e-03	3.476e-03
C (output stable)	5.941e-04	1.001e-03	2.594e-03	3.189e-03
D (output stable)	5.527e-04	9.015e-04	2.312e-03	2.913e-03
A to Z	2.629e-03	4.152e-03	1.272e-02	1.639e-02
B to Z	2.503e-03	3.903e-03	1.169e-02	1.535e-02
C to Z	2.567e-03	4.148e-03	1.098e-02	1.387e-02
D to Z	2.441e-03	3.877e-03	9.939e-03	1.286e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

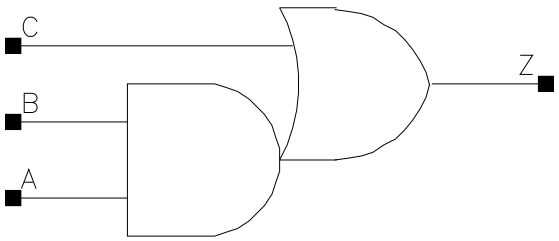
Pin Cycle (vdds)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0008	0.0012	0.0026
B	0.0008	0.0013	0.0025
C	0.0009	0.0014	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0352	0.0322	1.8391	0.8997
A to Z ↑	0.0230	0.0214	2.6989	1.3217
B to Z ↓	0.0323	0.0294	1.8314	0.8969
B to Z ↑	0.0251	0.0235	2.6948	1.3215
C to Z ↓	0.0332	0.0304	1.8318	0.8966
C to Z ↑	0.0222	0.0214	2.6768	1.3132
	X33_P16		**X33_P16**	
A to Z ↓	0.0323		0.4569	
A to Z ↑	0.0219		0.6663	

B to Z ↓	0.0298		0.4563	
B to Z ↑	0.0236		0.6656	
C to Z ↓	0.0307		0.4555	
C to Z ↑	0.0212		0.6624	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	1.599e-05	1.000e-20
X17_P16	3.336e-05	1.000e-20
X33_P16	6.652e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	4.304e-05	7.979e-05	1.844e-04
B (output stable)	4.986e-05	9.435e-05	2.394e-04
C (output stable)	5.978e-05	1.008e-04	2.323e-04
A to Z	4.012e-03	7.241e-03	1.449e-02
B to Z	3.790e-03	6.824e-03	1.356e-02
C to Z	4.285e-03	7.687e-03	1.542e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

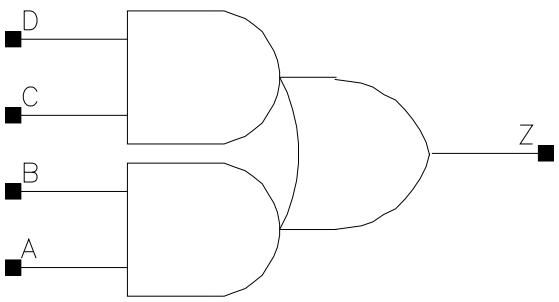
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0008	0.0013	0.0025
B	0.0009	0.0013	0.0024
C	0.0008	0.0012	0.0025
D	0.0008	0.0013	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0390	0.0346	1.7802	0.8966
A to Z ↑	0.0300	0.0281	2.6631	1.3251
B to Z ↓	0.0359	0.0318	1.7710	0.8930
B to Z ↑	0.0317	0.0301	2.6616	1.3242

C to Z ↓	0.0362	0.0327	1.7723	0.8931
C to Z ↑	0.0250	0.0235	2.6531	1.3191
D to Z ↓	0.0342	0.0307	1.7676	0.8911
D to Z ↑	0.0274	0.0256	2.6514	1.3186
	X33_P16		**X33_P16**	
A to Z ↓	0.0333		0.4576	
A to Z ↑	0.0259		0.6690	
B to Z ↓	0.0312		0.4572	
B to Z ↑	0.0282		0.6689	
C to Z ↓	0.0315		0.4565	
C to Z ↑	0.0220		0.6664	
D to Z ↓	0.0295		0.4559	
D to Z ↑	0.0240		0.6666	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	1.952e-05	1.000e-20
X17_P16	4.049e-05	1.000e-20
X33_P16	7.823e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	3.405e-05	4.883e-05	7.073e-05
B (output stable)	1.680e-04	2.050e-04	1.048e-04
C (output stable)	4.821e-05	8.098e-05	1.902e-04
D (output stable)	5.691e-05	9.931e-05	2.341e-04
A to Z	5.209e-03	9.014e-03	1.698e-02
B to Z	4.812e-03	8.414e-03	1.616e-02
C to Z	4.481e-03	7.816e-03	1.462e-02
D to Z	4.280e-03	7.441e-03	1.387e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

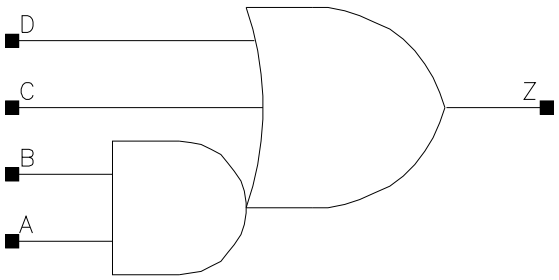
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	0.952	1.1424
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0008	0.0012	0.0024
B	0.0008	0.0012	0.0024
C	0.0009	0.0013	0.0025
D	0.0008	0.0013	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0449	0.0402	1.9139	0.9466
A to Z ↑	0.0247	0.0232	2.6887	1.3683
B to Z ↓	0.0426	0.0374	1.9074	0.9440
B to Z ↑	0.0270	0.0250	2.6895	1.3685
C to Z ↓	0.0450	0.0400	1.9068	0.9441
C to Z ↑	0.0240	0.0228	2.6698	1.3592

D to Z ↓	0.0451	0.0404	1.9084	0.9445
D to Z ↑	0.0236	0.0226	2.6689	1.3599
	X33_P16		**X33_P16**	
A to Z ↓	0.0412		0.4746	
A to Z ↑	0.0234		0.6669	
B to Z ↓	0.0369		0.4718	
B to Z ↑	0.0247		0.6672	
C to Z ↓	0.0417		0.4726	
C to Z ↑	0.0227		0.6638	
D to Z ↓	0.0409		0.4728	
D to Z ↑	0.0218		0.6625	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	1.394e-05	1.000e-20
X17_P16	2.920e-05	1.000e-20
X33_P16	5.897e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	4.191e-05	9.178e-05	2.102e-04
B (output stable)	4.340e-05	9.258e-05	2.539e-04
C (output stable)	3.241e-05	5.980e-05	1.744e-04
D (output stable)	3.744e-05	7.563e-05	2.832e-04
A to Z	4.513e-03	7.930e-03	1.604e-02
B to Z	4.309e-03	7.511e-03	1.479e-02
C to Z	5.027e-03	8.800e-03	1.810e-02
D to Z	4.767e-03	8.351e-03	1.680e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

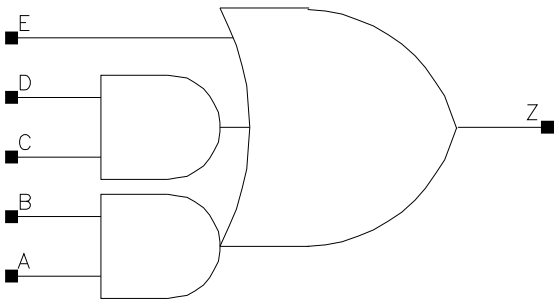
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.088	1.3056
X17_P16	1.200	1.224	1.4688
X33_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0008	0.0012	0.0025
B	0.0008	0.0012	0.0023
C	0.0009	0.0014	0.0025
D	0.0008	0.0012	0.0024
E	0.0008	0.0013	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0533	0.0468	1.8333	0.9237
A to Z ↑	0.0318	0.0284	2.6430	1.3306

B to Z ↓	0.0510	0.0442	1.8260	0.9214
B to Z ↑	0.0347	0.0309	2.6437	1.3297
C to Z ↓	0.0468	0.0424	1.8246	0.9202
C to Z ↑	0.0263	0.0234	2.6212	1.3220
D to Z ↓	0.0433	0.0386	1.8148	0.9155
D to Z ↑	0.0285	0.0253	2.6199	1.3217
E to Z ↓	0.0470	0.0414	1.8164	0.9170
E to Z ↑	0.0251	0.0225	2.5998	1.3126
	X33_P16		**X33_P16**	
A to Z ↓	0.0461		0.4745	
A to Z ↑	0.0295		0.6722	
B to Z ↓	0.0430		0.4734	
B to Z ↑	0.0317		0.6718	
C to Z ↓	0.0409		0.4724	
C to Z ↑	0.0236		0.6668	
D to Z ↓	0.0376		0.4705	
D to Z ↑	0.0255		0.6666	
E to Z ↓	0.0405		0.4711	
E to Z ↑	0.0227		0.6620	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	1.746e-05	1.000e-20
X17_P16	3.591e-05	1.000e-20
X33_P16	6.841e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.009e-05	3.209e-05	7.418e-05
B (output stable)	2.679e-05	3.838e-05	1.016e-04
C (output stable)	6.157e-05	1.042e-04	2.503e-04
D (output stable)	7.077e-05	1.244e-04	2.837e-04
E (output stable)	1.301e-04	1.793e-04	4.170e-04
A to Z	6.103e-03	1.024e-02	2.019e-02
B to Z	5.889e-03	9.799e-03	1.912e-02
C to Z	4.904e-03	8.404e-03	1.624e-02
D to Z	4.659e-03	7.923e-03	1.523e-02
E to Z	5.221e-03	8.800e-03	1.710e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

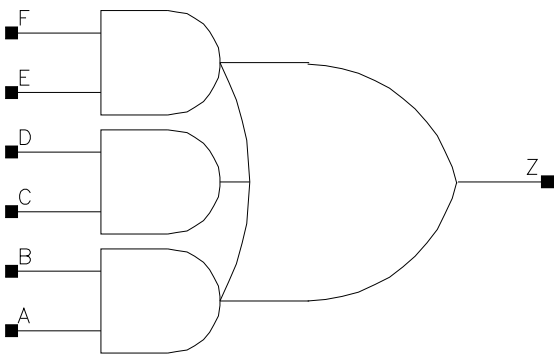
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.360	1.6320
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
A	0.0008	0.0009	0.0012	0.0025

B	0.0008	0.0010	0.0016	0.0023
C	0.0008	0.0009	0.0012	0.0024
D	0.0008	0.0009	0.0012	0.0023
E	0.0008	0.0010	0.0012	0.0025
F	0.0008	0.0009	0.0013	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0526	0.0509	3.4578	1.8366
A to Z ↑	0.0333	0.0328	5.0903	2.6922
B to Z ↓	0.0480	0.0468	3.4313	1.8244
B to Z ↑	0.0347	0.0346	5.0870	2.6906
C to Z ↓	0.0479	0.0469	3.4443	1.8312
C to Z ↑	0.0297	0.0293	5.0542	2.6729
D to Z ↓	0.0453	0.0444	3.4309	1.8241
D to Z ↑	0.0323	0.0319	5.0527	2.6727
E to Z ↓	0.0412	0.0413	3.4268	1.8225
E to Z ↑	0.0245	0.0244	5.0275	2.6605
F to Z ↓	0.0382	0.0384	3.4129	1.8147
F to Z ↑	0.0266	0.0265	5.0258	2.6602
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
A to Z ↓	0.0496	0.0482	0.9272	0.4733
A to Z ↑	0.0314	0.0317	1.3348	0.6747
B to Z ↓	0.0465	0.0454	0.9208	0.4723
B to Z ↑	0.0339	0.0340	1.3351	0.6744
C to Z ↓	0.0466	0.0450	0.9247	0.4729
C to Z ↑	0.0282	0.0290	1.3280	0.6710
D to Z ↓	0.0436	0.0425	0.9204	0.4717
D to Z ↑	0.0307	0.0313	1.3275	0.6708
E to Z ↓	0.0411	0.0417	0.9200	0.4713
E to Z ↑	0.0236	0.0249	1.3222	0.6687
F to Z ↓	0.0382	0.0385	0.9162	0.4693
F to Z ↑	0.0257	0.0271	1.3220	0.6687

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	1.464e-05	1.000e-20
X8_P16	2.415e-05	1.000e-20
X17_P16	4.264e-05	1.000e-20
X33_P16	8.061e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	3.726e-05	4.357e-05	5.543e-05	1.042e-04
B (output stable)	1.286e-04	1.408e-04	1.409e-04	1.557e-04
C (output stable)	4.365e-05	5.426e-05	6.849e-05	1.574e-04
D (output stable)	5.118e-05	6.422e-05	8.118e-05	2.188e-04
E (output stable)	9.778e-05	1.269e-04	1.798e-04	3.047e-04
F (output stable)	1.030e-04	1.321e-04	1.930e-04	3.510e-04

A to Z	5.125e-03	7.100e-03	1.131e-02	2.177e-02
B to Z	4.693e-03	6.584e-03	1.061e-02	2.070e-02
C to Z	4.353e-03	6.160e-03	1.004e-02	1.933e-02
D to Z	4.139e-03	5.882e-03	9.592e-03	1.838e-02
E to Z	3.554e-03	5.222e-03	8.638e-03	1.713e-02
F to Z	3.343e-03	4.942e-03	8.202e-03	1.617e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

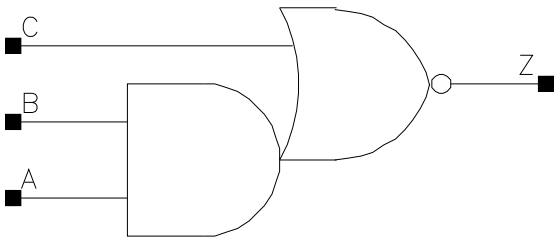
Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008
X44_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X33_P16	X44_P16
A	0.0010	0.0030	0.0061	0.0082
B	0.0010	0.0028	0.0057	0.0075
C	0.0011	0.0033	0.0063	0.0084

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0083	0.0086	3.0891	1.0444
A to Z ↑	0.0158	0.0162	4.7598	1.5951
B to Z ↓	0.0090	0.0093	3.1235	1.0594
B to Z ↑	0.0125	0.0124	4.6991	1.5975
C to Z ↓	0.0095	0.0097	1.8481	0.6315
C to Z ↑	0.0149	0.0150	4.3432	1.4674
	X33_P16	**X44_P16**	**X33_P16**	**X44_P16**
A to Z ↓	0.0088	0.0088	0.5318	0.4037

A to Z ↑	0.0162	0.0162	0.7983	0.6061
B to Z ↓	0.0093	0.0092	0.5395	0.4097
B to Z ↑	0.0124	0.0123	0.7981	0.6038
C to Z ↓	0.0113	0.0115	0.3756	0.2917
C to Z ↑	0.0152	0.0150	0.7333	0.5556

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P16	1.441e-05	1.000e-20
X17_P16	4.225e-05	1.000e-20
X33_P16	8.165e-05	1.000e-20
X44_P16	1.079e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	8.149e-05	2.477e-04	5.383e-04	7.072e-04
B (output stable)	9.279e-05	3.350e-04	7.366e-04	9.684e-04
C (output stable)	9.999e-05	3.091e-04	6.718e-04	8.774e-04
A to Z	1.892e-03	5.922e-03	1.188e-02	1.570e-02
B to Z	1.559e-03	4.596e-03	9.182e-03	1.214e-02
C to Z	2.537e-03	7.637e-03	1.528e-02	2.010e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

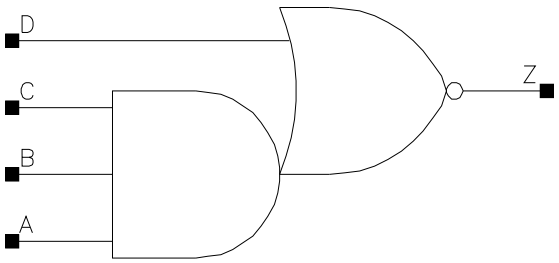
Pin Cycle (vdds)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X29_P16	1.200	3.536	4.2432
X38_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X29_P16	X38_P16
A	0.0011	0.0062	0.0081
B	0.0010	0.0059	0.0078
C	0.0010	0.0056	0.0075
D	0.0011	0.0064	0.0079

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X29_P16	X5_P16	X29_P16
A to Z ↓	0.0125	0.0134	4.3277	0.7491
A to Z ↑	0.0203	0.0203	4.7634	0.7908
B to Z ↓	0.0130	0.0132	4.3412	0.7527
B to Z ↑	0.0178	0.0177	4.7668	0.7968
C to Z ↓	0.0133	0.0132	4.3634	0.7570
C to Z ↑	0.0147	0.0142	4.7091	0.8037
D to Z ↓	0.0116	0.0135	1.8839	0.3780

D to Z ↑	0.0177	0.0179	4.0585	0.6810
	X38_P16		**X38_P16**	
A to Z ↓	0.0132		0.5788	
A to Z ↑	0.0199		0.5964	
B to Z ↓	0.0132		0.5818	
B to Z ↑	0.0173		0.6023	
C to Z ↓	0.0131		0.5852	
C to Z ↑	0.0140		0.6097	
D to Z ↓	0.0144		0.3133	
D to Z ↑	0.0176		0.5144	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.452e-05	1.000e-20
X29_P16	8.196e-05	1.000e-20
X38_P16	1.068e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X29_P16	X38_P16
A (output stable)	4.443e-05	3.527e-04	4.525e-04
B (output stable)	6.385e-05	5.488e-04	7.053e-04
C (output stable)	1.057e-04	1.037e-03	1.332e-03
D (output stable)	1.269e-04	9.349e-04	1.220e-03
A to Z	2.595e-03	1.622e-02	2.085e-02
B to Z	2.235e-03	1.333e-02	1.721e-02
C to Z	1.896e-03	1.063e-02	1.366e-02
D to Z	3.204e-03	1.941e-02	2.505e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

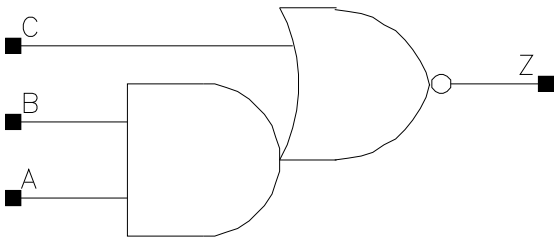
Pin Cycle (vdds)	X5_P16	X29_P16	X38_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X11_P16	1.200	1.088	1.3056
X16_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X11_P16	X16_P16	X23_P16
A	0.0011	0.0023	0.0033	0.0044
B	0.0011	0.0021	0.0031	0.0041
C	0.0011	0.0020	0.0029	0.0041
	X46_P16			
A	0.0086			
B	0.0081			
C	0.0082			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X11_P16	X6_P16	X11_P16
A to Z ↓	0.0106	0.0115	2.9835	1.5160
A to Z ↑	0.0165	0.0176	4.7472	2.3226
B to Z ↓	0.0119	0.0122	3.0151	1.5324

B to Z ↑	0.0138	0.0141	4.6938	2.3331
C to Z ↓	0.0061	0.0068	1.9022	1.1196
C to Z ↑	0.0128	0.0124	4.3992	2.1706
	X16_P16	**X23_P16**	**X16_P16**	**X23_P16**
A to Z ↓	0.0109	0.0112	1.0427	0.7851
A to Z ↑	0.0164	0.0167	1.5636	1.1850
B to Z ↓	0.0121	0.0120	1.0555	0.7941
B to Z ↑	0.0129	0.0131	1.5656	1.1915
C to Z ↓	0.0068	0.0058	0.7751	0.4875
C to Z ↑	0.0118	0.0125	1.4603	1.1066
	X46_P16		**X46_P16**	
A to Z ↓	0.0109		0.4027	
A to Z ↑	0.0161		0.6156	
B to Z ↓	0.0117		0.4077	
B to Z ↑	0.0125		0.6148	
C to Z ↓	0.0062		0.2490	
C to Z ↑	0.0127		0.5732	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P16	1.454e-05	1.000e-20
X11_P16	2.927e-05	1.000e-20
X16_P16	4.162e-05	1.000e-20
X23_P16	5.796e-05	1.000e-20
X46_P16	1.132e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	2.596e-05	7.484e-05	9.570e-05	1.375e-04
B (output stable)	3.768e-05	1.671e-04	1.687e-04	2.752e-04
C (output stable)	3.405e-04	8.667e-04	1.012e-03	1.386e-03
A to Z	2.551e-03	5.513e-03	7.658e-03	1.038e-02
B to Z	2.181e-03	4.525e-03	6.233e-03	8.393e-03
C to Z	1.646e-03	3.312e-03	4.618e-03	6.548e-03
	X46_P16			
A (output stable)	2.461e-04			
B (output stable)	4.640e-04			
C (output stable)	2.264e-03			
A to Z	1.953e-02			
B to Z	1.579e-02			
C to Z	1.261e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

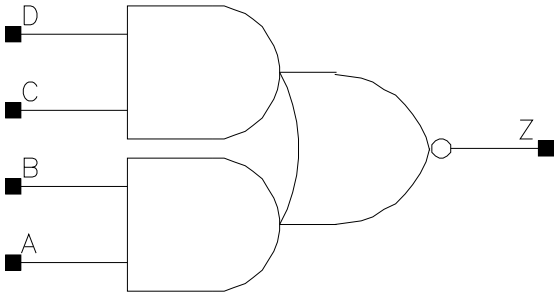
	X46_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P16	X10_P16	X16_P16	X21_P16
A	0.0009	0.0023	0.0033	0.0043
B	0.0009	0.0020	0.0031	0.0041
C	0.0008	0.0022	0.0031	0.0042
D	0.0009	0.0019	0.0029	0.0038
	X42_P16			
A	0.0087			
B	0.0081			
C	0.0082			
D	0.0077			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X10_P16**	**X4_P16**	**X10_P16**
A to Z ↓	0.0120	0.0121	3.6854	1.4592
A to Z ↑	0.0220	0.0185	6.4160	2.1419
B to Z ↓	0.0136	0.0138	3.7272	1.4762
B to Z ↑	0.0192	0.0163	6.4065	2.1968
C to Z ↓	0.0084	0.0081	3.7736	1.4695
C to Z ↑	0.0184	0.0160	6.4644	2.1722
D to Z ↓	0.0093	0.0092	3.8274	1.4920
D to Z ↑	0.0153	0.0133	6.4529	2.2066
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0132	0.0132	1.0470	0.7877
A to Z ↑	0.0194	0.0194	1.4432	1.1170
B to Z ↓	0.0147	0.0144	1.0579	0.7960
B to Z ↑	0.0163	0.0163	1.4456	1.1203
C to Z ↓	0.0088	0.0091	1.0481	0.7898
C to Z ↑	0.0166	0.0171	1.4566	1.1252
D to Z ↓	0.0098	0.0095	1.0628	0.8008
D to Z ↑	0.0133	0.0135	1.4603	1.1287
	X42_P16		**X42_P16**	
A to Z ↓	0.0140		0.4086	
A to Z ↑	0.0198		0.5596	
B to Z ↓	0.0149		0.4128	
B to Z ↑	0.0164		0.5583	
C to Z ↓	0.0097		0.4057	
C to Z ↑	0.0173		0.5650	
D to Z ↓	0.0103		0.4113	
D to Z ↑	0.0139		0.5640	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	1.155e-05	1.000e-20
X10_P16	3.574e-05	1.000e-20
X16_P16	5.098e-05	1.000e-20
X21_P16	6.843e-05	1.000e-20
X42_P16	1.344e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	2.850e-05	6.714e-05	1.321e-04	1.832e-04
B (output stable)	4.317e-05	1.068e-04	2.832e-04	4.587e-04
C (output stable)	7.659e-05	1.882e-04	3.217e-04	4.164e-04
D (output stable)	9.340e-05	2.339e-04	4.767e-04	6.887e-04
A to Z	2.519e-03	6.296e-03	9.782e-03	1.286e-02
B to Z	2.197e-03	5.502e-03	8.316e-03	1.090e-02
C to Z	1.628e-03	4.206e-03	6.495e-03	8.763e-03
D to Z	1.350e-03	3.496e-03	5.163e-03	6.920e-03
	X42_P16			
A (output stable)	3.457e-04			
B (output stable)	7.684e-04			
C (output stable)	8.087e-04			
D (output stable)	1.251e-03			

A to Z	2.543e-02			
B to Z	2.162e-02			
C to Z	1.728e-02			
D to Z	1.379e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

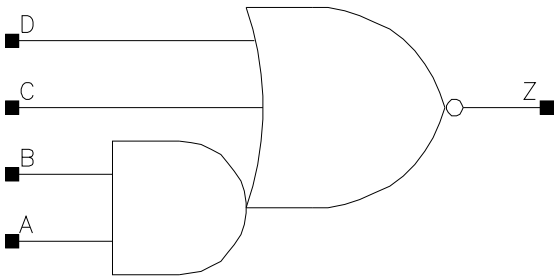
Pin Cycle (vdds)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X35_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P16	X35_P16
A	0.0010	0.0078
B	0.0010	0.0072
C	0.0011	0.0076
D	0.0011	0.0071

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X35_P16	X5_P16	X35_P16
A to Z ↓	0.0098	0.0102	3.1178	0.4589
A to Z ↑	0.0207	0.0194	6.7278	0.8652
B to Z ↓	0.0108	0.0110	3.1581	0.4657
B to Z ↑	0.0168	0.0151	6.6830	0.8655
C to Z ↓	0.0117	0.0158	1.9671	0.3751
C to Z ↑	0.0215	0.0211	6.3355	0.8159
D to Z ↓	0.0111	0.0144	1.9797	0.3749

D to Z ↑	0.0212	0.0198	6.3486	0.8191

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.292e-05	1.000e-20
X35_P16	9.315e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X35_P16
A (output stable)	8.755e-05	7.341e-04
B (output stable)	9.151e-05	8.207e-04
C (output stable)	5.781e-05	6.467e-04
D (output stable)	7.297e-05	8.708e-04
A to Z	2.158e-03	1.568e-02
B to Z	1.803e-03	1.243e-02
C to Z	3.265e-03	2.512e-02
D to Z	2.785e-03	2.018e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

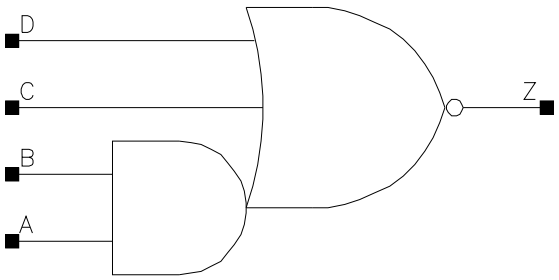
Pin Cycle (vdds)	X5_P16	X35_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X17_P16	1.200	2.448	2.9376
X34_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P16	X17_P16	X34_P16
A	0.0011	0.0043	0.0087
B	0.0010	0.0041	0.0082
C	0.0009	0.0037	0.0071
D	0.0009	0.0034	0.0067

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X17_P16	X4_P16	X17_P16
A to Z ↓	0.0126	0.0138	3.3707	0.8873
A to Z ↑	0.0219	0.0231	6.7766	1.6732
B to Z ↓	0.0143	0.0150	3.4067	0.8962
B to Z ↑	0.0187	0.0190	6.7172	1.6783
C to Z ↓	0.0121	0.0122	3.0726	0.7500
C to Z ↑	0.0157	0.0166	6.4200	1.5942

D to Z ↓	0.0097	0.0088	3.1571	0.7559
D to Z ↑	0.0149	0.0140	6.4435	1.5991
	X34_P16		**X34_P16**	
A to Z ↓	0.0136		0.4543	
A to Z ↑	0.0227		0.8538	
B to Z ↓	0.0150		0.4591	
B to Z ↑	0.0186		0.8519	
C to Z ↓	0.0126		0.4005	
C to Z ↑	0.0161		0.8115	
D to Z ↓	0.0093		0.4047	
D to Z ↑	0.0137		0.8144	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	1.195e-05	1.000e-20
X17_P16	4.791e-05	1.000e-20
X34_P16	9.374e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X17_P16	X34_P16
A (output stable)	2.612e-05	1.255e-04	2.503e-04
B (output stable)	2.977e-05	1.930e-04	3.549e-04
C (output stable)	8.809e-05	4.525e-04	8.773e-04
D (output stable)	1.762e-04	1.083e-03	2.036e-03
A to Z	3.054e-03	1.312e-02	2.545e-02
B to Z	2.695e-03	1.114e-02	2.167e-02
C to Z	1.959e-03	8.443e-03	1.611e-02
D to Z	1.516e-03	5.929e-03	1.129e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

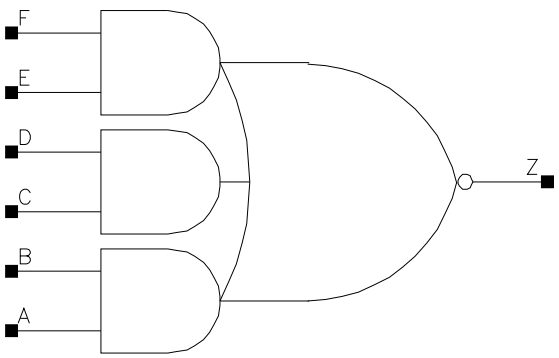
Pin Cycle (vdds)	X4_P16	X17_P16	X34_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X8_P16	1.200	2.176	2.6112
X13_P16	1.200	2.720	3.2640
X17_P16	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P16	X8_P16	X13_P16	X17_P16
A	0.0011	0.0021	0.0033	0.0043

B	0.0010	0.0020	0.0030	0.0040
C	0.0010	0.0021	0.0031	0.0040
D	0.0010	0.0019	0.0029	0.0037
E	0.0012	0.0020	0.0029	0.0038
F	0.0010	0.0018	0.0027	0.0036

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0153	0.0187	2.9929	1.7232
A to Z ↑	0.0324	0.0318	6.4909	3.0186
B to Z ↓	0.0175	0.0203	3.0220	1.7352
B to Z ↑	0.0290	0.0283	6.4927	3.0294
C to Z ↓	0.0136	0.0164	2.9678	1.7357
C to Z ↑	0.0283	0.0285	6.5350	3.0352
D to Z ↓	0.0154	0.0181	3.0054	1.7528
D to Z ↑	0.0249	0.0248	6.5095	3.0389
E to Z ↓	0.0097	0.0118	2.9405	1.7416
E to Z ↑	0.0232	0.0229	6.5046	3.0322
F to Z ↓	0.0108	0.0127	2.9920	1.7670
F to Z ↑	0.0198	0.0190	6.5582	3.0394
	X13_P16	**X17_P16**	**X13_P16**	**X17_P16**
A to Z ↓	0.0179	0.0181	1.1698	0.8912
A to Z ↑	0.0295	0.0296	1.9926	1.5281
B to Z ↓	0.0199	0.0197	1.1779	0.8974
B to Z ↑	0.0264	0.0260	2.0022	1.5304
C to Z ↓	0.0157	0.0157	1.1751	0.8831
C to Z ↑	0.0262	0.0265	2.0071	1.5408
D to Z ↓	0.0175	0.0171	1.1860	0.8915
D to Z ↑	0.0229	0.0228	2.0124	1.5395
E to Z ↓	0.0112	0.0111	1.1736	0.8865
E to Z ↑	0.0214	0.0215	2.0095	1.5358
F to Z ↓	0.0123	0.0118	1.1901	0.8984
F to Z ↑	0.0179	0.0178	2.0155	1.5440

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	2.006e-05	1.000e-20
X8_P16	4.130e-05	1.000e-20
X13_P16	5.907e-05	1.000e-20
X17_P16	7.884e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

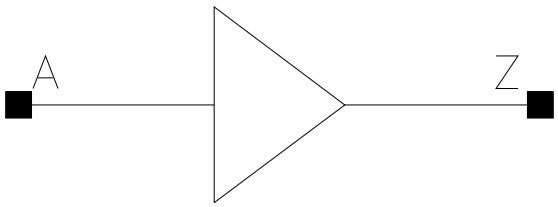
Pin Cycle (vdd)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	4.784e-05	1.136e-04	1.588e-04	2.130e-04
B (output stable)	5.780e-05	2.231e-04	2.394e-04	3.944e-04
C (output stable)	8.324e-05	1.789e-04	2.392e-04	3.159e-04
D (output stable)	9.505e-05	3.000e-04	3.263e-04	4.977e-04
E (output stable)	1.476e-04	3.579e-04	4.878e-04	6.603e-04
F (output stable)	1.691e-04	4.694e-04	5.803e-04	8.407e-04

A to Z	4.733e-03	9.951e-03	1.392e-02	1.839e-02
B to Z	4.308e-03	8.954e-03	1.258e-02	1.640e-02
C to Z	3.590e-03	7.786e-03	1.063e-02	1.414e-02
D to Z	3.206e-03	6.853e-03	9.387e-03	1.233e-02
E to Z	2.497e-03	5.452e-03	7.412e-03	9.829e-03
F to Z	2.141e-03	4.544e-03	6.210e-03	8.124e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.408	0.4896
X6_P16	1.200	0.408	0.4896
X8_P16	1.200	0.408	0.4896
X13_P16	1.200	0.544	0.6528
X16_P16	1.200	0.544	0.6528
X21_P16	1.200	0.680	0.8160
X25_P16	1.200	0.680	0.8160
X29_P16	1.200	0.952	1.1424
X33_P16	1.200	0.952	1.1424
X42_P16	1.200	1.088	1.3056
X50_P16	1.200	1.224	1.4688
X58_P16	1.200	1.496	1.7952
X67_P16	1.200	1.632	1.9584
X75_P16	1.200	1.768	2.1216
X84_P16	1.200	1.904	2.2848
X100_P16	1.200	2.312	2.7744
X134_P16	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0010	0.0010	0.0010	0.0010
	X16_P16	X21_P16	X25_P16	X29_P16
A	0.0010	0.0014	0.0014	0.0019
	X33_P16	X42_P16	X50_P16	X58_P16
A	0.0019	0.0022	0.0026	0.0039

	X67_P16	X75_P16	X84_P16	X100_P16
A	0.0038	0.0038	0.0038	0.0050
	X134_P16			
A	0.0063			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0218	0.0222	3.2390	2.3821
A to Z ↑	0.0174	0.0176	4.9704	3.7104
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0235	0.0270	1.7742	1.1406
A to Z ↑	0.0185	0.0212	2.6825	1.7379
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0296	0.0247	0.9109	0.7018
A to Z ↑	0.0229	0.0200	1.3463	1.0494
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0260	0.0247	0.6023	0.5076
A to Z ↑	0.0208	0.0190	0.8847	0.7507
	X33_P16	**X42_P16**	**X33_P16**	**X42_P16**
A to Z ↓	0.0259	0.0254	0.4510	0.3656
A to Z ↑	0.0198	0.0203	0.6620	0.5326
	X50_P16	**X58_P16**	**X50_P16**	**X58_P16**
A to Z ↓	0.0250	0.0231	0.3036	0.2620
A to Z ↑	0.0200	0.0188	0.4425	0.3801
	X67_P16	**X75_P16**	**X67_P16**	**X75_P16**
A to Z ↓	0.0243	0.0258	0.2301	0.2075
A to Z ↑	0.0197	0.0208	0.3332	0.2980
	X84_P16	**X100_P16**	**X84_P16**	**X100_P16**
A to Z ↓	0.0271	0.0251	0.1876	0.1576
A to Z ↑	0.0219	0.0204	0.2694	0.2255
	X134_P16		**X134_P16**	
A to Z ↓	0.0267		0.1226	
A to Z ↑	0.0219		0.1728	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	9.659e-06	1.000e-20
X6_P16	1.215e-05	1.000e-20
X8_P16	1.573e-05	1.000e-20
X13_P16	2.010e-05	1.000e-20
X16_P16	2.598e-05	1.000e-20
X21_P16	3.608e-05	1.000e-20
X25_P16	4.181e-05	1.000e-20
X29_P16	4.711e-05	1.000e-20
X33_P16	5.261e-05	1.000e-20
X42_P16	6.648e-05	1.000e-20
X50_P16	8.072e-05	1.000e-20
X58_P16	1.002e-04	1.000e-20
X67_P16	1.099e-04	1.000e-20
X75_P16	1.197e-04	1.000e-20

X84_P16	1.294e-04	1.000e-20
X100_P16	1.586e-04	1.000e-20
X134_P16	2.073e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	2.519e-03	2.876e-03	3.475e-03	4.847e-03
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	6.036e-03	7.908e-03	9.029e-03	1.027e-02
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	1.143e-02	1.430e-02	1.702e-02	2.035e-02
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	2.296e-02	2.587e-02	2.892e-02	3.376e-02
	X134_P16			
A to Z	4.771e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

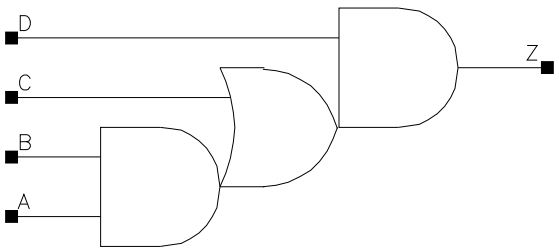
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P16			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.632	1.9584
X25_P16	1.200	1.768	2.1216
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0012	0.0026	0.0026	0.0026
B	0.0013	0.0024	0.0024	0.0023
C	0.0013	0.0028	0.0028	0.0028
D	0.0018	0.0025	0.0025	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0292	0.0277	1.8125	0.8972
A to Z ↑	0.0284	0.0271	2.7284	1.3297
B to Z ↓	0.0265	0.0248	1.8056	0.8955
B to Z ↑	0.0293	0.0275	2.7271	1.3280
C to Z ↓	0.0255	0.0239	1.8026	0.8937
C to Z ↑	0.0213	0.0197	2.7013	1.3157

D to Z ↓	0.0258	0.0230	1.7874	0.8863
D to Z ↑	0.0240	0.0212	2.7071	1.3188
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0308	0.0331	0.6091	0.4589
A to Z ↑	0.0301	0.0322	0.8995	0.6762
B to Z ↓	0.0280	0.0308	0.6083	0.4580
B to Z ↑	0.0306	0.0332	0.8989	0.6758
C to Z ↓	0.0271	0.0298	0.6060	0.4565
C to Z ↑	0.0223	0.0244	0.8893	0.6673
D to Z ↓	0.0251	0.0269	0.5997	0.4501
D to Z ↑	0.0235	0.0253	0.8913	0.6692

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	2.690e-05	1.000e-20
X17_P16	5.307e-05	1.000e-20
X25_P16	6.436e-05	1.000e-20
X33_P16	7.566e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	1.076e-04	2.211e-04	2.237e-04	2.011e-04
B (output stable)	1.492e-04	3.172e-04	3.200e-04	2.777e-04
C (output stable)	4.180e-04	7.076e-04	7.121e-04	6.843e-04
D (output stable)	1.145e-04	1.719e-04	1.741e-04	1.722e-04
A to Z	5.679e-03	1.061e-02	1.369e-02	1.674e-02
B to Z	5.259e-03	9.606e-03	1.267e-02	1.584e-02
C to Z	4.540e-03	8.155e-03	1.098e-02	1.383e-02
D to Z	5.744e-03	1.034e-02	1.305e-02	1.567e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

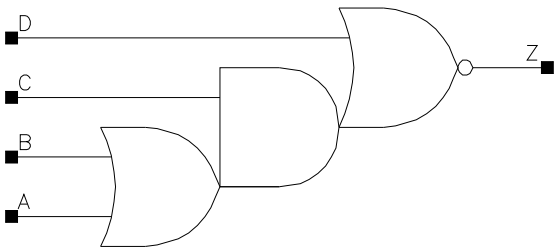
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.952	1.1424
X11_P16	1.200	1.496	1.7952
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X16_P16	X21_P16
A	0.0012	0.0022	0.0033	0.0044
B	0.0011	0.0021	0.0033	0.0042
C	0.0011	0.0021	0.0031	0.0042
D	0.0014	0.0021	0.0031	0.0042

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0132	0.0126	2.9527	1.5488
A to Z ↑	0.0264	0.0247	6.6486	3.4822
B to Z ↓	0.0124	0.0121	2.8793	1.5189
B to Z ↑	0.0251	0.0240	6.6601	3.4879
C to Z ↓	0.0125	0.0121	2.7425	1.4389
C to Z ↑	0.0160	0.0147	4.6740	2.4045

D to Z ↓	0.0068	0.0057	1.8453	0.9325
D to Z ↑	0.0155	0.0139	4.9543	2.5575
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0125	0.0129	1.0388	0.8009
A to Z ↑	0.0228	0.0242	2.2241	1.7226
B to Z ↓	0.0116	0.0120	1.0449	0.8020
B to Z ↑	0.0225	0.0232	2.2278	1.7259
C to Z ↓	0.0121	0.0123	0.9836	0.7543
C to Z ↑	0.0140	0.0142	1.5890	1.1923
D to Z ↓	0.0057	0.0058	0.6473	0.4931
D to Z ↑	0.0129	0.0128	1.6742	1.2679

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.682e-05	1.000e-20
X11_P16	3.235e-05	1.000e-20
X16_P16	4.587e-05	1.000e-20
X21_P16	6.124e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	3.083e-05	5.641e-05	7.447e-05	1.201e-04
B (output stable)	3.946e-05	6.525e-05	8.218e-05	1.486e-04
C (output stable)	1.007e-04	2.040e-04	2.758e-04	3.873e-04
D (output stable)	4.268e-04	8.985e-04	1.293e-03	1.794e-03
A to Z	3.818e-03	6.823e-03	9.614e-03	1.338e-02
B to Z	3.122e-03	5.650e-03	8.160e-03	1.098e-02
C to Z	2.705e-03	4.812e-03	6.891e-03	9.398e-03
D to Z	1.889e-03	3.381e-03	4.721e-03	6.270e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

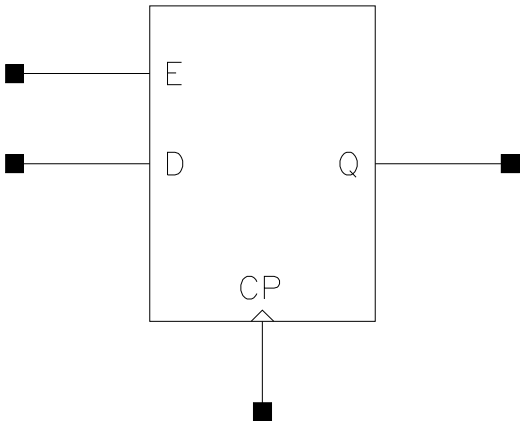
Pin Cycle (vdds)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.128	3.7536
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011
D	0.0008	0.0008	0.0008
E	0.0010	0.0014	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0363	0.0423	1.7973	0.9264
CP to Q ↑	0.0457	0.0496	2.7339	1.3692
	X33_P16		**X33_P16**	
CP to Q ↓	0.0647		0.4571	
CP to Q ↑	0.0793		0.6766	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0444	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0284	0.0365	0.0271
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120
D ↑	hold_rising to CP	0.0010	0.0010	-0.0017
D ↓	setup_rising to CP	0.0441	0.0441	0.0441
D ↑	setup_rising to CP	0.0298	0.0298	0.0298
E ↓	hold_rising to CP	-0.0067	-0.0067	-0.0067
E ↑	hold_rising to CP	-0.0017	-0.0017	-0.0017
E ↓	setup_rising to CP	0.0479	0.0479	0.0479
E ↑	setup_rising to CP	0.0493	0.0493	0.0493

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	6.001e-05	1.000e-20
X17_P16	7.013e-05	1.000e-20
X33_P16	1.024e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

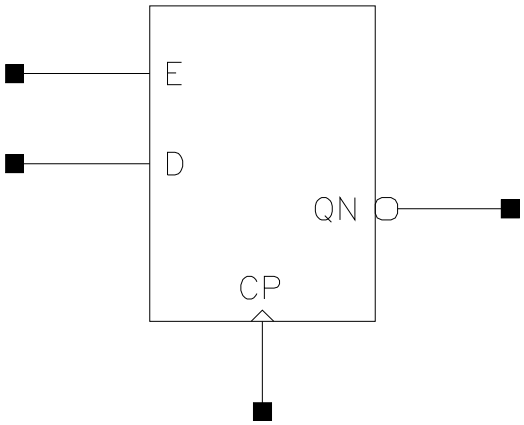
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.148e-02	1.148e-02	1.149e-02
Clock 100Mhz Data 25Mhz	1.526e-02	1.685e-02	2.082e-02
Clock 100Mhz Data 50Mhz	1.904e-02	2.222e-02	3.014e-02
Clock = 0 Data 100Mhz	7.537e-03	7.537e-03	7.537e-03
Clock = 1 Data 100Mhz	2.048e-03	2.048e-03	2.048e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.264	3.9168
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0011	0.0011	0.0011
D	0.0008	0.0008	0.0008
E	0.0010	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.0638	0.0608	1.8487	0.8843
CP to QN ↑	0.0488	0.0500	2.7623	1.3269
	X33_P16		**X33_P16**	
CP to QN ↓	0.0660		0.4587	
CP to QN ↑	0.0559		0.6782	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0444	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0271	0.0271	0.0318
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0049	-0.0017	0.0010
D ↓	setup_rising to CP	0.0441	0.0441	0.0441
D ↑	setup_rising to CP	0.0298	0.0298	0.0298
E ↓	hold_rising to CP	-0.0067	-0.0067	-0.0067
E ↑	hold_rising to CP	-0.0017	-0.0017	-0.0017
E ↓	setup_rising to CP	0.0479	0.0479	0.0479
E ↑	setup_rising to CP	0.0493	0.0493	0.0493

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	5.950e-05	1.000e-20
X17_P16	7.652e-05	1.000e-20
X33_P16	9.997e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

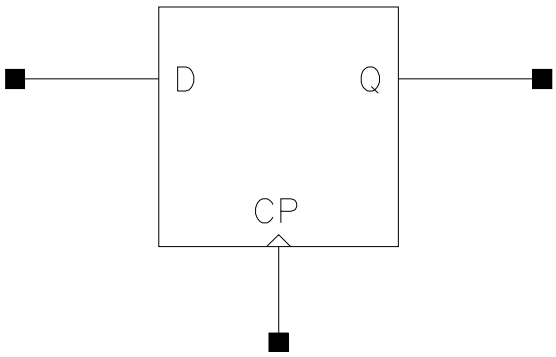
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.147e-02	1.147e-02	1.148e-02
Clock 100Mhz Data 25Mhz	1.528e-02	1.716e-02	2.074e-02
Clock 100Mhz Data 50Mhz	1.908e-02	2.285e-02	3.000e-02
Clock = 0 Data 100Mhz	7.537e-03	7.536e-03	7.536e-03
Clock = 1 Data 100Mhz	2.048e-03	2.048e-03	2.048e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.176	2.6112
X17_P16	1.200	2.448	2.9376
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0012	0.0012	0.0012	0.0012
D	0.0009	0.0009	0.0009	0.0009

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0380	0.0425	1.7884	0.9169
CP to Q ↑	0.0458	0.0516	2.6500	1.3445
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to Q ↓	0.0544	0.0567	0.5406	0.4917
CP to Q ↑	0.0594	0.0609	0.7556	0.6899

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0431	0.0431	0.0431	0.0431
CP ↑	min_pulse_width to CP	0.0284	0.0331	0.0424	0.0458
D ↓	hold_rising to CP	0.0129	0.0129	0.0129	0.0129
D ↑	hold_rising to CP	0.0129	0.0129	0.0129	0.0129
D ↓	setup_rising to CP	0.0224	0.0246	0.0246	0.0246
D ↑	setup_rising to CP	0.0146	0.0146	0.0146	0.0146

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	4.675e-05	1.000e-20
X17_P16	5.791e-05	1.000e-20
X30_P16	7.353e-05	1.000e-20
X33_P16	7.758e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

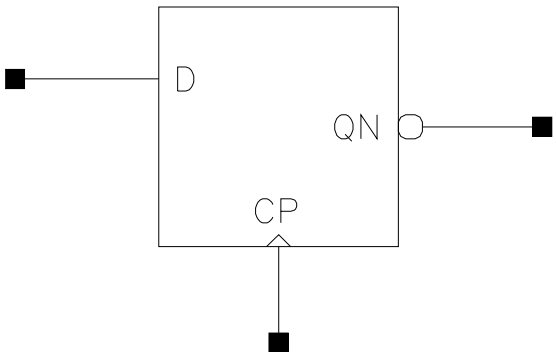
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.193e-02	1.200e-02	1.202e-02	1.203e-02
Clock 100Mhz Data 25Mhz	1.393e-02	1.593e-02	1.967e-02	2.060e-02
Clock 100Mhz Data 50Mhz	1.593e-02	1.986e-02	2.731e-02	2.917e-02
Clock = 0 Data 100Mhz	5.073e-03	5.215e-03	5.258e-03	5.280e-03
Clock = 1 Data 100Mhz	2.393e-05	2.397e-05	2.409e-05	2.414e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0012	0.0012	0.0012	0.0012
D	0.0009	0.0009	0.0009	0.0009

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.0372	0.0436	1.8429	0.9474
CP to QN ↑	0.0387	0.0418	2.6468	1.3458
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to QN ↓	0.0652	0.0657	0.5039	0.4577
CP to QN ↑	0.0520	0.0595	0.7295	0.6766

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0383	0.0417	0.0431	0.0431
CP ↑	min_pulse_width to CP	0.0270	0.0318	0.0283	0.0330
D ↓	hold_rising to CP	0.0146	0.0146	0.0129	0.0129
D ↑	hold_rising to CP	0.0119	0.0119	0.0129	0.0129
D ↓	setup_rising to CP	0.0175	0.0175	0.0246	0.0218
D ↑	setup_rising to CP	0.0146	0.0146	0.0146	0.0146

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	4.366e-05	1.000e-20
X17_P16	5.389e-05	1.000e-20
X30_P16	8.175e-05	1.000e-20
X33_P16	8.689e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

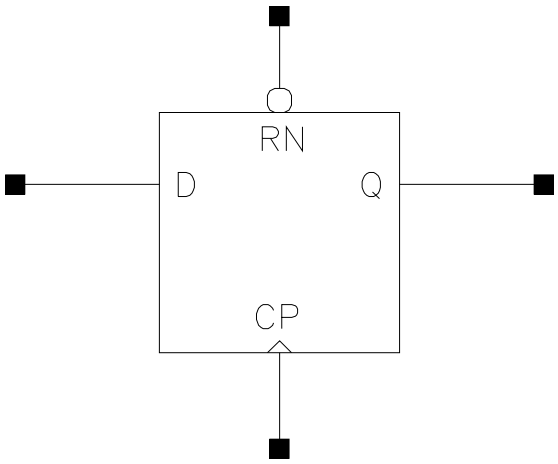
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.159e-02	1.160e-02	1.175e-02	1.181e-02
Clock 100Mhz Data 25Mhz	1.337e-02	1.504e-02	1.831e-02	1.937e-02
Clock 100Mhz Data 50Mhz	1.515e-02	1.848e-02	2.486e-02	2.694e-02
Clock = 0 Data 100Mhz	4.417e-03	4.417e-03	4.728e-03	4.815e-03
Clock = 1 Data 100Mhz	2.360e-05	2.366e-05	2.388e-05	2.400e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0012	0.0012
D	0.0009	0.0009
RN	0.0011	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0442	0.0561	0.9251	0.5489
CP to Q ↑	0.0530	0.0606	1.3490	0.7587
RN to Q ↓	0.0572	0.0648	0.9018	0.5305

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0365	0.0458
D ↓	hold_rising to CP	0.0129	0.0129
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0272	0.0272
D ↑	setup_rising to CP	0.0174	0.0174
RN ↓	min_pulse_width to RN	0.0854	0.1099
RN ↑	recovery_rising to CP	0.0125	0.0151
RN ↑	removal_rising to CP	-0.0028	-0.0028

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P16	6.533e-05	1.000e-20
X30_P16	8.290e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

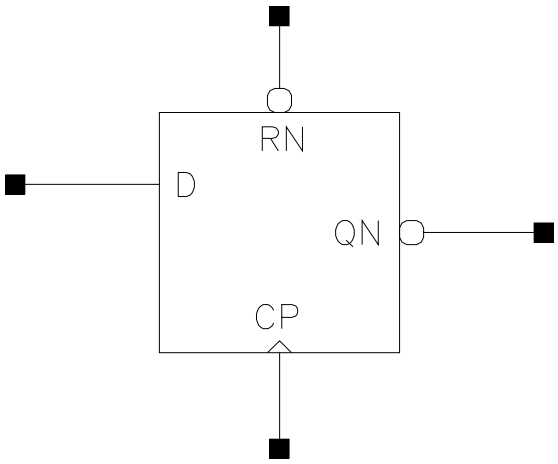
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	1.266e-02	1.266e-02
Clock 100Mhz Data 25Mhz	1.683e-02	2.052e-02
Clock 100Mhz Data 50Mhz	2.099e-02	2.838e-02
Clock = 0 Data 100Mhz	6.061e-03	6.065e-03
Clock = 1 Data 100Mhz	2.427e-05	2.441e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0012	0.0012
D	0.0009	0.0009
RN	0.0011	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.0616	0.0672	0.8775	0.5052
CP to QN ↑	0.0498	0.0542	1.3174	0.7321
RN to QN ↑	0.0652	0.0692	1.3152	0.7319

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0270	0.0318
D ↓	hold_rising to CP	0.0097	0.0097
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0272	0.0272
D ↑	setup_rising to CP	0.0174	0.0174
RN ↓	min_pulse_width to RN	0.0686	0.0708
RN ↑	recovery_rising to CP	0.0125	0.0125
RN ↑	removal_rising to CP	-0.0028	-0.0028

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P16	7.061e-05	1.000e-20
X30_P16	8.408e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

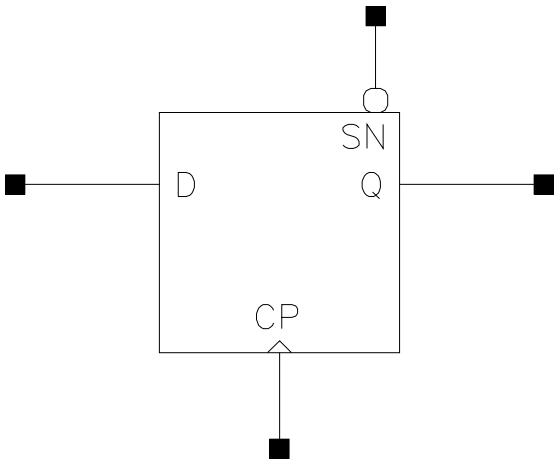
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	1.266e-02	1.266e-02
Clock 100Mhz Data 25Mhz	1.710e-02	1.949e-02
Clock 100Mhz Data 50Mhz	2.155e-02	2.632e-02
Clock = 0 Data 100Mhz	6.134e-03	6.115e-03
Clock = 1 Data 100Mhz	2.427e-05	2.436e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0012	0.0012
D	0.0009	0.0009
SN	0.0016	0.0016

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0440	0.0566	0.9255	0.5458
CP to Q ↑	0.0525	0.0605	1.3492	0.7580
SN to Q ↑	0.0413	0.0462	1.3332	0.7439

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0491	0.0491
CP ↑	min_pulse_width to CP	0.0365	0.0458
D ↓	hold_rising to CP	0.0097	0.0097
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0295	0.0295
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0527	0.0625
SN ↑	recovery_rising to CP	0.0032	0.0032
SN ↑	removal_rising to CP	0.0237	0.0237

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P16	6.204e-05	1.000e-20
X30_P16	7.556e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

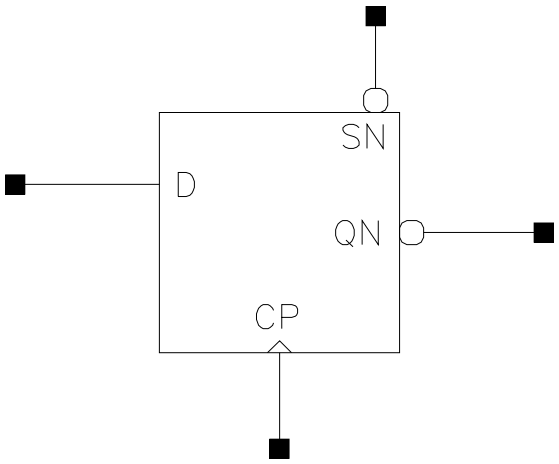
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	1.277e-02	1.275e-02
Clock 100Mhz Data 25Mhz	1.692e-02	2.061e-02
Clock 100Mhz Data 50Mhz	2.107e-02	2.848e-02
Clock = 0 Data 100Mhz	5.977e-03	5.976e-03
Clock = 1 Data 100Mhz	2.430e-05	2.441e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0012	0.0012
D	0.0009	0.0009
SN	0.0016	0.0016

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.0610	0.0667	0.8803	0.5059
CP to QN ↑	0.0497	0.0541	1.3152	0.7311
SN to QN ↓	0.0508	0.0562	0.8796	0.5058

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0491	0.0491
CP ↑	min_pulse_width to CP	0.0270	0.0318
D ↓	hold_rising to CP	0.0097	0.0097
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0295	0.0295
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0403	0.0430
SN ↑	recovery_rising to CP	0.0032	0.0032
SN ↑	removal_rising to CP	0.0237	0.0237

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P16	7.343e-05	1.000e-20
X30_P16	9.085e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

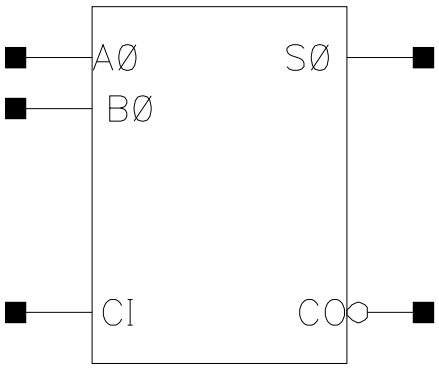
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	1.277e-02	1.276e-02
Clock 100Mhz Data 25Mhz	1.715e-02	1.955e-02
Clock 100Mhz Data 50Mhz	2.154e-02	2.634e-02
Clock = 0 Data 100Mhz	5.977e-03	5.979e-03
Clock = 1 Data 100Mhz	2.439e-05	2.449e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_P16	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_P16	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_P16	1.200	3.672	4.4064
C12T28SOI_LLS1_FA1X33_P16	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_FA1X8_P16	C12T28SOI_LL_FA1X33_P16	C12T28SOI_LLS1_FA1X8_P16	C12T28SOI_LLS1_FA1X33_P16
A0	0.0041	0.0084	0.0036	0.0069
B0	0.0037	0.0080	0.0038	0.0068
CI	0.0027	0.0061	0.0027	0.0048

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16
A0 to CO ↓	0.0391	0.0435	1.8685	0.4873
A0 to CO ↑	0.0304	0.0326	2.7352	0.7014
A0 to S0 ↓	0.0417	0.0534	1.8399	0.4754
A0 to S0 ↑	0.0429	0.0535	2.7015	0.6903
B0 to CO ↓	0.0391	0.0443	1.8744	0.4897
B0 to CO ↑	0.0317	0.0343	2.7372	0.6995
B0 to S0 ↓	0.0424	0.0546	1.8409	0.4754
B0 to S0 ↑	0.0435	0.0546	2.7023	0.6906
CI to CO ↓	0.0385	0.0442	1.8743	0.4883
CI to CO ↑	0.0316	0.0338	2.7345	0.7013
CI to S0 ↓	0.0421	0.0543	1.8408	0.4756
CI to S0 ↑	0.0437	0.0552	2.7015	0.6905
	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16
A0 to CO ↓	0.0255	0.0321	3.4667	0.5967
A0 to CO ↑	0.0233	0.0273	2.7657	0.6851
A0 to S0 ↓	0.0547	0.0689	1.9883	0.4966
A0 to S0 ↑	0.0504	0.0552	2.8047	0.7015
B0 to CO ↓	0.0268	0.0338	3.4678	0.5976
B0 to CO ↑	0.0213	0.0258	2.7625	0.6853
B0 to S0 ↓	0.0553	0.0709	1.9885	0.4967
B0 to S0 ↑	0.0509	0.0571	2.8054	0.7016
CI to CO ↓	0.0271	0.0496	3.4616	0.6044
CI to CO ↑	0.0230	0.0292	2.8334	0.6909
CI to S0 ↓	0.0317	0.0424	1.9889	0.4972
CI to S0 ↑	0.0272	0.0279	2.8054	0.7019

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_FA1X8_P16	5.953e-05	1.000e-20
C12T28SOI_LL_FA1X33_P16	1.576e-04	1.000e-20
C12T28SOI_LLS1_FA1X8_P16	1.238e-04	1.000e-20
C12T28SOI_LLS1_FA1X33_P16	2.603e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16
A0 to CO	6.004e-03	1.849e-02	8.731e-03	2.300e-02
A0 to S0	6.010e-03	1.904e-02	1.169e-02	2.837e-02
B0 to CO	6.098e-03	1.892e-02	8.835e-03	2.335e-02
B0 to S0	5.959e-03	1.903e-02	1.194e-02	2.904e-02
CI to CO	6.222e-03	1.923e-02	6.298e-03	2.139e-02
CI to S0	5.931e-03	1.897e-02	7.187e-03	2.285e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X33_P16	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X33_P16
A0	0.0014	0.0042
B0	0.0012	0.0035

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
A0 to CO ↓	0.0313	0.0292	1.8417	0.4566
A0 to CO ↑	0.0278	0.0260	2.7088	0.6957
A0 to S0 ↓	0.0394	0.0382	1.8050	0.4561
A0 to S0 ↑	0.0382	0.0444	2.6733	0.6860
B0 to CO ↓	0.0302	0.0267	1.8424	0.4534
B0 to CO ↑	0.0304	0.0277	2.7080	0.6957
B0 to S0 ↓	0.0414	0.0389	1.8036	0.4557
B0 to S0 ↑	0.0375	0.0425	2.6732	0.6861

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	3.590e-05	1.000e-20
X33_P16	1.475e-04	1.000e-20

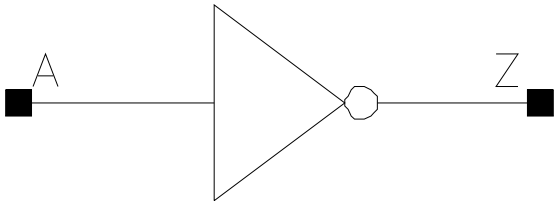
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X33_P16
A0 to CO	4.643e-03	1.593e-02
A0 to S0	4.329e-03	1.574e-02
B0 to CO	4.723e-03	1.630e-02
B0 to S0	4.261e-03	1.530e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X8_P16	X33_P16
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.272	0.3264
X6_P16	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X13_P16	1.200	0.408	0.4896
X17_P16	1.200	0.408	0.4896
X21_P16	1.200	0.544	0.6528
X25_P16	1.200	0.544	0.6528
X29_P16	1.200	0.680	0.8160
X33_P16	1.200	0.680	0.8160
X50_P16	1.200	0.952	1.1424
X58_P16	1.200	1.088	1.3056
X67_P16	1.200	1.224	1.4688
X75_P16	1.200	1.360	1.6320
X84_P16	1.200	1.496	1.7952
X100_P16	1.200	1.768	2.1216
X134_P16	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0007	0.0008	0.0011	0.0017
	X17_P16	X21_P16	X25_P16	X29_P16
A	0.0021	0.0028	0.0032	0.0038
	X33_P16	X50_P16	X58_P16	X67_P16
A	0.0042	0.0063	0.0074	0.0085
	X75_P16	X84_P16	X100_P16	X134_P16

A	0.0097	0.0110	0.0135	0.0187

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0059	0.0057	3.4203	2.6423
A to Z ↑	0.0105	0.0098	5.0976	3.9016
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0052	0.0043	1.8253	1.1751
A to Z ↑	0.0089	0.0082	2.7320	1.7830
	X17_P16	**X21_P16**	**X17_P16**	**X21_P16**
A to Z ↓	0.0044	0.0048	0.9038	0.7261
A to Z ↑	0.0078	0.0082	1.3451	1.0770
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0048	0.0045	0.6181	0.5234
A to Z ↑	0.0079	0.0077	0.9043	0.7702
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0046	0.0048	0.4644	0.3134
A to Z ↑	0.0075	0.0076	0.6777	0.4537
	X58_P16	**X67_P16**	**X58_P16**	**X67_P16**
A to Z ↓	0.0049	0.0050	0.2717	0.2384
A to Z ↑	0.0077	0.0077	0.3910	0.3426
	X75_P16	**X84_P16**	**X75_P16**	**X84_P16**
A to Z ↓	0.0055	0.0058	0.2151	0.1946
A to Z ↑	0.0081	0.0083	0.3068	0.2774
	X100_P16	**X134_P16**	**X100_P16**	**X134_P16**
A to Z ↓	0.0067	0.0076	0.1656	0.1288
A to Z ↑	0.0092	0.0101	0.2338	0.1797

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	5.009e-06	1.000e-20
X6_P16	6.928e-06	1.000e-20
X8_P16	1.079e-05	1.000e-20
X13_P16	1.553e-05	1.000e-20
X17_P16	2.184e-05	1.000e-20
X21_P16	2.575e-05	1.000e-20
X25_P16	3.173e-05	1.000e-20
X29_P16	3.588e-05	1.000e-20
X33_P16	4.146e-05	1.000e-20
X50_P16	6.091e-05	1.000e-20
X58_P16	7.064e-05	1.000e-20
X67_P16	8.038e-05	1.000e-20
X75_P16	9.012e-05	1.000e-20
X84_P16	9.985e-05	1.000e-20
X100_P16	1.193e-04	1.000e-20
X134_P16	1.583e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16

A to Z	8.846e-04	1.117e-03	1.513e-03	2.198e-03
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	2.861e-03	3.715e-03	4.328e-03	4.923e-03
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	5.522e-03	8.266e-03	9.680e-03	1.099e-02
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	1.256e-02	1.404e-02	1.747e-02	2.439e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

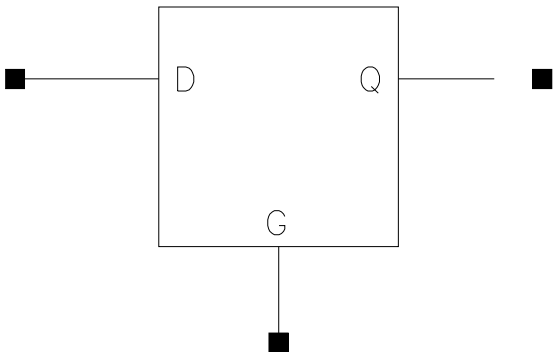
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X23_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P16	X23_P16
D	0.0007	0.0017
G	0.0015	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X23_P16	X8_P16	X23_P16
D to Q ↓	0.0444	0.0358	1.8604	0.8655
D to Q ↑	0.0300	0.0301	2.6633	0.7103
G to Q ↓	0.0472	0.0387	1.8564	0.8653
G to Q ↑	0.0294	0.0265	2.6666	0.7104

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P16	X23_P16
D ↓	hold_falling to G	-0.0072	-0.0001
D ↑	hold_falling to G	0.0019	0.0019
D ↓	setup_falling to G	0.0409	0.0296
D ↑	setup_falling to G	0.0329	0.0376
G ↑	min_pulse_width to G	0.0411	0.0397

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	2.608e-05	1.000e-20
X23_P16	6.297e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X23_P16
D (output stable)	1.678e-05	7.101e-05
G (output stable)	1.518e-03	3.028e-03
D to Q	7.680e-03	1.530e-02
G to Q	7.174e-03	1.385e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

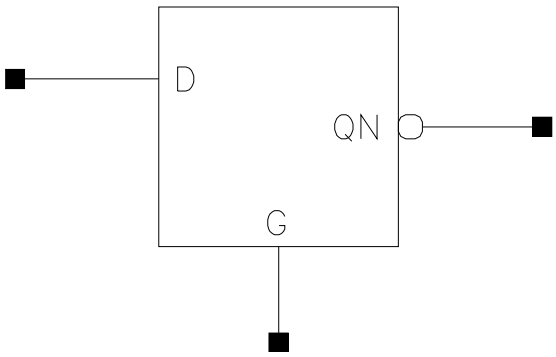
Pin Cycle (vdds)	X8_P16	X23_P16
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P16
D	0.0007
G	0.0017

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P16	X17_P16
D to QN ↓	0.0405	0.8825
D to QN ↑	0.0499	1.3087
G to QN ↓	0.0393	0.8822
G to QN ↑	0.0512	1.3087

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X17_P16
D ↓	hold_falling to G	-0.0120
D ↑	hold_falling to G	-0.0039
D ↓	setup_falling to G	0.0370
D ↑	setup_falling to G	0.0286
G ↑	min_pulse_width to G	0.0330

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P16	4.131e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X17_P16
D (output stable)	1.716e-05
G (output stable)	1.819e-03
D to QN	9.404e-03
G to QN	8.846e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

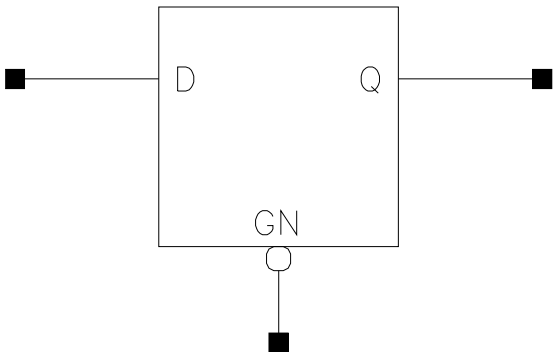
Pin Cycle (vdds)	X17_P16
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
D	0.0007	0.0010	0.0023
GN	0.0014	0.0017	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D to Q ↓	0.0449	0.0393	1.8653	0.9209
D to Q ↑	0.0305	0.0295	2.6675	1.3661
GN to Q ↓	0.0410	0.0353	1.8668	0.9222
GN to Q ↑	0.0446	0.0429	2.6667	1.3646

	X33_P16		X33_P16	
D to Q ↓	0.0384		0.4707	
D to Q ↑	0.0254		0.6856	
GN to Q ↓	0.0332		0.4712	
GN to Q ↑	0.0339		0.6844	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P16	X17_P16	X33_P16
D ↓	hold_rising to GN	-0.0101	-0.0025	-0.0025
D ↑	hold_rising to GN	0.0058	0.0058	0.0073
D ↓	setup_rising to GN	0.0498	0.0450	0.0429
D ↑	setup_rising to GN	0.0294	0.0297	0.0249
GN ↓	min_pulse_width to GN	0.0554	0.0479	0.0438

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	2.611e-05	1.000e-20
X17_P16	4.238e-05	1.000e-20
X33_P16	7.340e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
D (output stable)	1.656e-05	2.741e-05	7.442e-05
GN (output stable)	1.507e-03	2.034e-03	2.729e-03
D to Q	7.723e-03	1.127e-02	1.844e-02
GN to Q	1.054e-02	1.474e-02	2.232e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

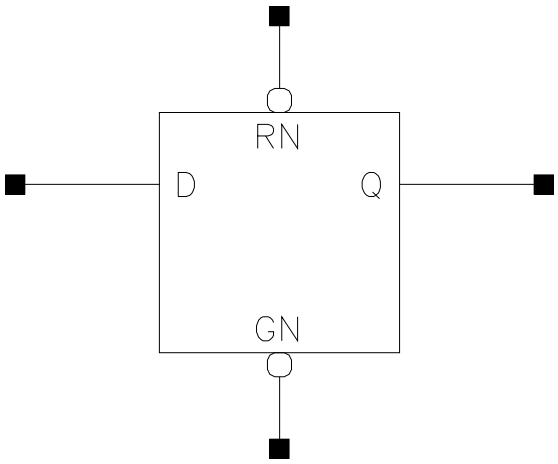
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.496	1.7952
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X33_P16
D	0.0007	0.0018
GN	0.0015	0.0028
RN	0.0007	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
D to Q ↓	0.0419	0.0386	1.8269	0.4724
D to Q ↑	0.0398	0.0531	2.7238	0.7069

GN to Q ↓	0.0386	0.0353	1.8276	0.4729
GN to Q ↑	0.0511	0.0548	2.7209	0.7075
RN to Q ↓	0.0355	0.0627	1.7432	0.4795
RN to Q ↑	0.0414	0.0582	2.7229	0.7079

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P16	X33_P16
D ↓	hold_rising to GN	-0.0078	-0.0030
D ↑	hold_rising to GN	-0.0045	-0.0196
D ↓	setup_rising to GN	0.0446	0.0398
D ↑	setup_rising to GN	0.0390	0.0588
GN ↓	min_pulse_width to GN	0.0510	0.0577
RN ↓	min_pulse_width to RN	0.0425	0.0784
RN ↑	recovery_rising to GN	0.0417	0.0628
RN ↑	removal_rising to GN	-0.0244	-0.0408

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	2.963e-05	1.000e-20
X33_P16	7.564e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X33_P16
D (output stable)	1.072e-04	2.108e-04
GN (output stable)	1.753e-03	2.801e-03
RN (output stable)	4.940e-05	9.600e-05
D to Q	7.881e-03	2.216e-02
GN to Q	1.092e-02	2.672e-02
RN to Q	5.962e-03	1.820e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

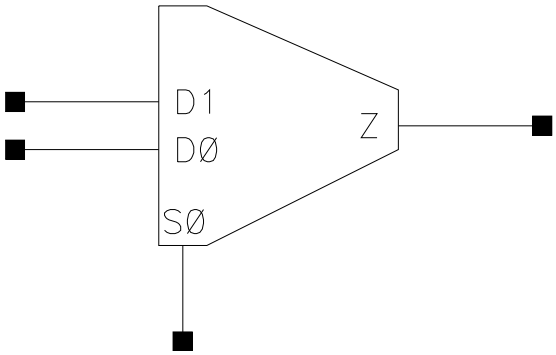
Pin Cycle (vdds)	X8_P16	X33_P16
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
D0	0.0009	0.0014	0.0018	0.0025
D1	0.0009	0.0014	0.0018	0.0025
S0	0.0016	0.0018	0.0021	0.0031

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D0 to Z ↓	0.0343	0.0312	1.8393	0.9008
D0 to Z ↑	0.0279	0.0261	2.7315	1.3350
D1 to Z ↓	0.0327	0.0306	1.8370	0.8991
D1 to Z ↑	0.0256	0.0247	2.7265	1.3338
S0 to Z ↓	0.0296	0.0293	1.8313	0.8977
S0 to Z ↑	0.0284	0.0291	2.7271	1.3333

	X25_P16	X33_P16	X25_P16	X33_P16
D0 to Z ↓	0.0335	0.0302	0.6186	0.4636
D0 to Z ↑	0.0278	0.0260	0.8977	0.6722
D1 to Z ↓	0.0356	0.0313	0.6217	0.4649
D1 to Z ↑	0.0270	0.0252	0.8962	0.6719
S0 to Z ↓	0.0332	0.0306	0.6187	0.4632
S0 to Z ↑	0.0322	0.0297	0.8968	0.6720

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	3.019e-05	1.000e-20
X17_P16	5.664e-05	1.000e-20
X25_P16	7.505e-05	1.000e-20
X33_P16	1.114e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	1.349e-03	2.138e-03	2.486e-03	3.538e-03
D1 (output stable)	1.179e-03	2.049e-03	2.663e-03	3.629e-03
S0 (output stable)	1.740e-03	1.992e-03	2.580e-03	3.282e-03
D0 to Z	5.057e-03	8.688e-03	1.354e-02	1.716e-02
D1 to Z	4.734e-03	8.464e-03	1.368e-02	1.710e-02
S0 to Z	5.743e-03	9.159e-03	1.488e-02	1.840e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

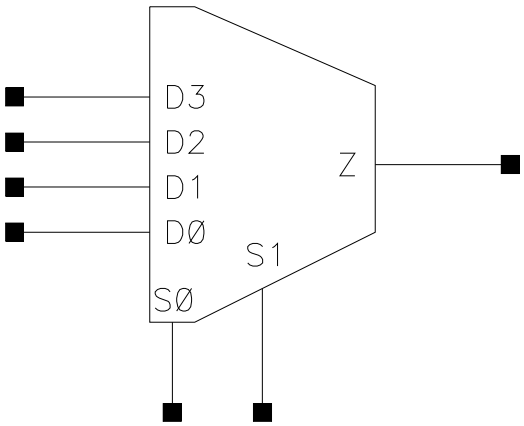
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.312	2.7744
X31_P16	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P16	X31_P16
D0	0.0007	0.0019
D1	0.0007	0.0019
D2	0.0007	0.0019
D3	0.0007	0.0019
S0	0.0024	0.0049
S1	0.0014	0.0029

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X31_P16	X8_P16	X31_P16

D0 to Z ↓	0.0570	0.0596	1.9220	0.5309
D0 to Z ↑	0.0403	0.0441	2.7528	0.7402
D1 to Z ↓	0.0565	0.0596	1.9199	0.5311
D1 to Z ↑	0.0405	0.0440	2.7522	0.7402
D2 to Z ↓	0.0608	0.0565	1.9305	0.5262
D2 to Z ↑	0.0426	0.0406	2.7588	0.7354
D3 to Z ↓	0.0606	0.0559	1.9301	0.5251
D3 to Z ↑	0.0421	0.0423	2.7593	0.7384
S0 to Z ↓	0.0635	0.0666	1.9226	0.5277
S0 to Z ↑	0.0498	0.0548	2.7564	0.7391
S1 to Z ↓	0.0460	0.0471	1.9250	0.5278
S1 to Z ↑	0.0391	0.0426	2.7548	0.7383

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	3.145e-05	1.000e-20
X31_P16	9.779e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X31_P16
D0 (output stable)	2.722e-05	1.621e-04
D1 (output stable)	2.727e-05	1.502e-04
D2 (output stable)	3.194e-05	1.547e-04
D3 (output stable)	3.138e-05	1.654e-04
S0 (output stable)	2.565e-03	5.960e-03
S1 (output stable)	2.107e-03	4.661e-03
D0 to Z	5.807e-03	2.085e-02
D1 to Z	5.788e-03	2.093e-02
D2 to Z	6.173e-03	1.963e-02
D3 to Z	6.154e-03	1.972e-02
S0 to Z	8.707e-03	2.709e-02
S1 to Z	6.893e-03	2.143e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

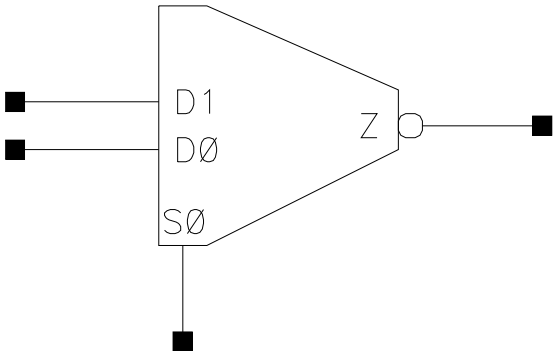
Pin Cycle (vdds)	X8_P16	X31_P16
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.816	0.9792
X5_P16	1.200	0.952	1.1424
X10_P16	1.200	1.768	2.1216
X16_P16	1.200	2.448	2.9376
X21_P16	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P16	X5_P16	X10_P16	X16_P16
D0	0.0007	0.0011	0.0022	0.0033
D1	0.0007	0.0011	0.0021	0.0033
S0	0.0014	0.0024	0.0032	0.0049
	X21_P16			
D0	0.0044			
D1	0.0043			
S0	0.0056			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X5_P16**	**X3_P16**	**X5_P16**
D0 to Z ↓	0.0111	0.0115	5.4629	3.4638

D0 to Z ↑	0.0186	0.0167	9.7636	5.1258
D1 to Z ↓	0.0109	0.0111	5.4304	3.2848
D1 to Z ↑	0.0193	0.0175	9.7733	5.3315
S0 to Z ↓	0.0178	0.0153	5.4352	3.3726
S0 to Z ↑	0.0190	0.0162	9.7420	5.2177
	X10_P16	**X16_P16**	**X10_P16**	**X16_P16**
D0 to Z ↓	0.0131	0.0121	1.6364	1.0681
D0 to Z ↑	0.0182	0.0173	2.3998	1.5840
D1 to Z ↓	0.0118	0.0115	1.5804	1.0401
D1 to Z ↑	0.0183	0.0178	2.4432	1.6013
S0 to Z ↓	0.0189	0.0163	1.6049	1.0531
S0 to Z ↑	0.0195	0.0168	2.4165	1.5898
	X21_P16		**X21_P16**	
D0 to Z ↓	0.0120		0.8163	
D0 to Z ↑	0.0169		1.2009	
D1 to Z ↓	0.0115		0.7894	
D1 to Z ↑	0.0178		1.1956	
S0 to Z ↓	0.0173		0.8018	
S0 to Z ↑	0.0174		1.1952	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	1.137e-05	1.000e-20
X5_P16	2.557e-05	1.000e-20
X10_P16	4.611e-05	1.000e-20
X16_P16	7.397e-05	1.000e-20
X21_P16	9.118e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	1.662e-05	3.712e-05	1.092e-04	1.703e-04
D1 (output stable)	1.654e-05	3.929e-05	9.288e-05	1.615e-04
S0 (output stable)	1.519e-03	2.403e-03	3.854e-03	6.346e-03
D0 to Z	1.436e-03	2.429e-03	5.885e-03	8.395e-03
D1 to Z	1.437e-03	2.410e-03	5.640e-03	8.292e-03
S0 to Z	2.596e-03	4.077e-03	7.976e-03	1.185e-02
	X21_P16			
D0 (output stable)	2.196e-04			
D1 (output stable)	2.187e-04			
S0 (output stable)	7.017e-03			
D0 to Z	1.089e-02			
D1 to Z	1.098e-02			
S0 to Z	1.441e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

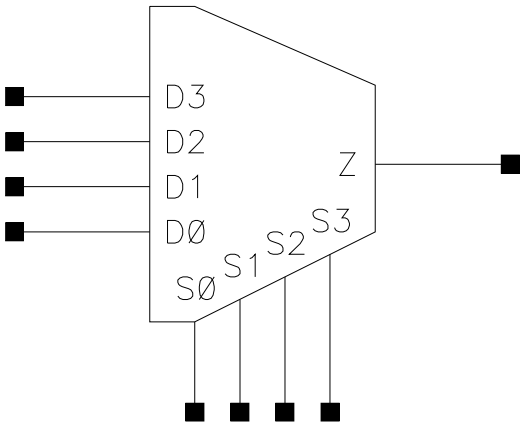
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P16			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	1.768	2.1216
X27_P16	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P16	X27_P16
D0	0.0008	0.0026
D1	0.0008	0.0026
D2	0.0008	0.0026
D3	0.0008	0.0026
S0	0.0008	0.0024
S1	0.0009	0.0025
S2	0.0008	0.0025
S3	0.0009	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	X27_P16	X7_P16	X27_P16
D0 to Z ↓	0.0439	0.0376	2.8866	0.7877
D0 to Z ↑	0.0334	0.0295	2.6860	0.6702
D1 to Z ↓	0.0411	0.0356	2.8827	0.7870
D1 to Z ↑	0.0294	0.0254	2.6732	0.6672
D2 to Z ↓	0.0449	0.0367	2.8941	0.7876
D2 to Z ↑	0.0325	0.0275	2.6962	0.6731
D3 to Z ↓	0.0422	0.0348	2.8879	0.7863
D3 to Z ↑	0.0286	0.0235	2.6864	0.6697
S0 to Z ↓	0.0420	0.0352	2.8852	0.7873
S0 to Z ↑	0.0363	0.0316	2.6841	0.6699
S1 to Z ↓	0.0395	0.0332	2.8816	0.7866
S1 to Z ↑	0.0320	0.0271	2.6752	0.6671
S2 to Z ↓	0.0429	0.0342	2.8917	0.7871
S2 to Z ↑	0.0353	0.0296	2.6953	0.6727
S3 to Z ↓	0.0406	0.0321	2.8862	0.7857
S3 to Z ↑	0.0311	0.0252	2.6844	0.6696

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X7_P16	2.915e-05	1.000e-20
X27_P16	1.197e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X7_P16	X27_P16
D0 (output stable)	7.547e-04	2.450e-03
D1 (output stable)	6.508e-04	2.079e-03
D2 (output stable)	6.880e-04	2.235e-03
D3 (output stable)	5.845e-04	1.866e-03
S0 (output stable)	7.268e-04	2.319e-03
S1 (output stable)	6.217e-04	1.964e-03
S2 (output stable)	6.597e-04	2.104e-03
S3 (output stable)	5.550e-04	1.754e-03
D0 to Z	6.095e-03	1.959e-02
D1 to Z	5.401e-03	1.716e-02
D2 to Z	5.867e-03	1.751e-02
D3 to Z	5.185e-03	1.510e-02
S0 to Z	5.905e-03	1.863e-02
S1 to Z	5.217e-03	1.625e-02
S2 to Z	5.673e-03	1.650e-02
S3 to Z	4.999e-03	1.418e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

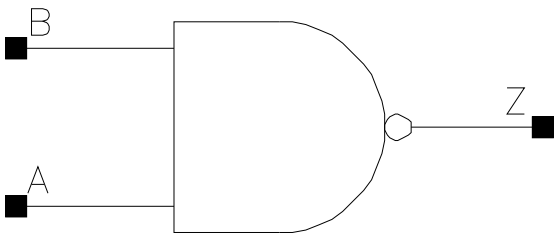
Pin Cycle (vdds)	X7_P16	X27_P16
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P16	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P16	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P16	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P16	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P16	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P16	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P16	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P16	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P16	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P16	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P16	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P16	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P16	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P16	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P16	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P16	C12T28SOI_LL_-NAND2X5_P16	C12T28SOI_LL_-NAND2X7_P16	C12T28SOI_LL_-NAND2X10_P16
A	0.0007	0.0009	0.0011	0.0017
B	0.0007	0.0009	0.0011	0.0016
	C12T28SOI_LL_-NAND2X13_P16	C12T28SOI_LL_-NAND2X17_P16	C12T28SOI_LL_-NAND2X20_P16	C12T28SOI_LL_-NAND2X24_P16
A	0.0022	0.0028	0.0032	0.0039
B	0.0020	0.0026	0.0030	0.0036
	C12T28SOI_LL_-NAND2X27_P16	C12T28SOI_LL_-NAND2X42_P16	C12T28SOI_LL_-NAND2X47_P16	C12T28SOI_LL_-NAND2X50_P16
A	0.0043	0.0013	0.0013	0.0013
B	0.0040	0.0014	0.0014	0.0014
	C12T28SOI_LL_-NAND2X58_P16	C12T28SOI_LL_-NAND2X67_P16	C12T28SOI_-LLBR0D8_-NAND2X7_P16	C12T28SOI_-LLBR0D8_-NAND2X14_P16
A	0.0013	0.0013	0.0011	0.0022
B	0.0014	0.0014	0.0011	0.0020
	C12T28SOI_LLS_-NAND2X40_P16	C12T28SOI_LLS_-NAND2X54_P16		
A	0.0065	0.0087		
B	0.0060	0.0080		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P16	**C12T28SOI_LL_-NAND2X5_P16**	**C12T28SOI_LL_-NAND2X3_P16**	**C12T28SOI_LL_-NAND2X5_P16**
A to Z ↓	0.0081	0.0075	5.3592	3.5214
A to Z ↑	0.0130	0.0120	5.1158	3.3458
B to Z ↓	0.0095	0.0086	5.4361	3.5671
B to Z ↑	0.0113	0.0098	5.1599	3.3744
	C12T28SOI_LL_-NAND2X7_P16	**C12T28SOI_LL_-NAND2X10_P16**	**C12T28SOI_LL_-NAND2X7_P16**	**C12T28SOI_LL_-NAND2X10_P16**
A to Z ↓	0.0076	0.0085	2.9649	1.9511
A to Z ↑	0.0115	0.0124	2.7213	1.7704
B to Z ↓	0.0086	0.0085	2.9986	1.9749
B to Z ↑	0.0094	0.0094	2.7483	1.7863
	C12T28SOI_LL_-NAND2X13_P16	**C12T28SOI_LL_-NAND2X17_P16**	**C12T28SOI_LL_-NAND2X13_P16**	**C12T28SOI_LL_-NAND2X17_P16**
A to Z ↓	0.0083	0.0081	1.5140	1.1986

A to Z ↑	0.0118	0.0118	1.3393	1.0736
B to Z ↓	0.0083	0.0087	1.5319	1.2122
B to Z ↑	0.0087	0.0093	1.3527	1.0817
	C12T28SOI_LL_-NAND2X20_P16	**C12T28SOI_LL_-NAND2X24_P16**	**C12T28SOI_LL_-NAND2X20_P16**	**C12T28SOI_LL_-NAND2X24_P16**
A to Z ↓	0.0080	0.0082	1.0338	0.8755
A to Z ↑	0.0115	0.0117	0.9016	0.7677
B to Z ↓	0.0088	0.0084	1.0459	0.8856
B to Z ↑	0.0089	0.0087	0.9096	0.7732
	C12T28SOI_LL_-NAND2X27_P16	**C12T28SOI_LL_-NAND2X42_P16**	**C12T28SOI_LL_-NAND2X27_P16**	**C12T28SOI_LL_-NAND2X42_P16**
A to Z ↓	0.0081	0.0348	0.7841	0.3679
A to Z ↑	0.0115	0.0356	0.6763	0.5317
B to Z ↓	0.0084	0.0365	0.7931	0.3681
B to Z ↑	0.0085	0.0338	0.6816	0.5318
	C12T28SOI_LL_-NAND2X47_P16	**C12T28SOI_LL_-NAND2X50_P16**	**C12T28SOI_LL_-NAND2X47_P16**	**C12T28SOI_LL_-NAND2X50_P16**
A to Z ↓	0.0359	0.0364	0.3268	0.3072
A to Z ↑	0.0362	0.0367	0.4625	0.4441
B to Z ↓	0.0377	0.0382	0.3266	0.3070
B to Z ↑	0.0346	0.0350	0.4623	0.4440
	C12T28SOI_LL_-NAND2X58_P16	**C12T28SOI_LL_-NAND2X67_P16**	**C12T28SOI_LL_-NAND2X58_P16**	**C12T28SOI_LL_-NAND2X67_P16**
A to Z ↓	0.0383	0.0399	0.2663	0.2343
A to Z ↑	0.0381	0.0392	0.3822	0.3357
B to Z ↓	0.0401	0.0416	0.2663	0.2342
B to Z ↑	0.0364	0.0375	0.3824	0.3356
	C12T28SOI_-LLBR0D8_-NAND2X7_P16	**C12T28SOI_-LLBR0D8_-NAND2X14_P16**	**C12T28SOI_-LLBR0D8_-NAND2X7_P16**	**C12T28SOI_-LLBR0D8_-NAND2X14_P16**
A to Z ↓	0.0054	0.0063	2.2582	1.1882
A to Z ↑	0.0149	0.0151	3.5595	1.7418
B to Z ↓	0.0058	0.0055	2.2992	1.2106
B to Z ↑	0.0118	0.0107	3.6738	1.7762
	C12T28SOI_LLS_-NAND2X40_P16	**C12T28SOI_LLS_-NAND2X54_P16**	**C12T28SOI_LLS_-NAND2X40_P16**	**C12T28SOI_LLS_-NAND2X54_P16**
A to Z ↓	0.0081	0.0082	0.5309	0.4017
A to Z ↑	0.0114	0.0114	0.4530	0.3409
B to Z ↓	0.0085	0.0087	0.5371	0.4064
B to Z ↑	0.0084	0.0086	0.4568	0.3444

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P16	5.329e-06	1.000e-20
C12T28SOI_LL_NAND2X5_P16	9.140e-06	1.000e-20
C12T28SOI_LL_NAND2X7_P16	1.149e-05	1.000e-20
C12T28SOI_LL_NAND2X10_P16	1.608e-05	1.000e-20
C12T28SOI_LL_NAND2X13_P16	2.259e-05	1.000e-20
C12T28SOI_LL_NAND2X17_P16	2.688e-05	1.000e-20
C12T28SOI_LL_NAND2X20_P16	3.306e-05	1.000e-20
C12T28SOI_LL_NAND2X24_P16	3.767e-05	1.000e-20
C12T28SOI_LL_NAND2X27_P16	4.354e-05	1.000e-20

C12T28SOI_LL_NAND2X42_P16	7.559e-05	1.000e-20
C12T28SOI_LL_NAND2X47_P16	8.129e-05	1.000e-20
C12T28SOI_LL_NAND2X50_P16	8.324e-05	1.000e-20
C12T28SOI_LL_NAND2X58_P16	9.089e-05	1.000e-20
C12T28SOI_LL_NAND2X67_P16	9.854e-05	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_-P16	1.081e-05	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_-P16	2.086e-05	1.000e-20
C12T28SOI_LLS_NAND2X40_P16	6.451e-05	1.000e-20
C12T28SOI_LLS_NAND2X54_P16	8.548e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND2X3_P16	C12T28SOI_LL_-NAND2X5_P16	C12T28SOI_LL_-NAND2X7_P16	C12T28SOI_LL_-NAND2X10_P16
A (output stable)	1.264e-05	1.865e-05	2.227e-05	7.761e-05
B (output stable)	2.766e-05	4.252e-05	5.189e-05	3.324e-04
A to Z	1.128e-03	1.594e-03	1.911e-03	3.159e-03
B to Z	9.480e-04	1.312e-03	1.575e-03	2.382e-03
	C12T28SOI_LL_-NAND2X13_P16	C12T28SOI_LL_-NAND2X17_P16	C12T28SOI_LL_-NAND2X20_P16	C12T28SOI_LL_-NAND2X24_P16
A (output stable)	9.323e-05	1.094e-04	1.212e-04	1.687e-04
B (output stable)	3.723e-04	3.308e-04	3.559e-04	6.211e-04
A to Z	3.980e-03	4.979e-03	5.779e-03	6.920e-03
B to Z	3.031e-03	3.910e-03	4.552e-03	5.289e-03
	C12T28SOI_LL_-NAND2X27_P16	C12T28SOI_LL_-NAND2X42_P16	C12T28SOI_LL_-NAND2X47_P16	C12T28SOI_LL_-NAND2X50_P16
A (output stable)	1.800e-04	2.579e-05	2.603e-05	2.598e-05
B (output stable)	6.655e-04	5.455e-05	5.476e-05	5.467e-05
A to Z	7.702e-03	1.807e-02	1.978e-02	2.064e-02
B to Z	5.899e-03	1.773e-02	1.945e-02	2.030e-02
	C12T28SOI_LL_-NAND2X58_P16	C12T28SOI_LL_-NAND2X67_P16	C12T28SOI_-LLBR0D8_-NAND2X7_P16	C12T28SOI_-LLBR0D8_-NAND2X14_P16
A (output stable)	2.611e-05	2.615e-05	2.906e-05	1.139e-04
B (output stable)	5.486e-05	5.502e-05	6.795e-05	4.523e-04
A to Z	2.378e-02	2.674e-02	1.948e-03	4.072e-03
B to Z	2.344e-02	2.641e-02	1.487e-03	2.800e-03
	C12T28SOI_LLS_-NAND2X40_P16	C12T28SOI_LLS_-NAND2X54_P16		
A (output stable)	2.582e-04	3.364e-04		
B (output stable)	8.789e-04	1.105e-03		
A to Z	1.141e-02	1.513e-02		
B to Z	8.799e-03	1.171e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND2X3_P16	C12T28SOI_LL_-NAND2X5_P16	C12T28SOI_LL_-NAND2X7_P16	C12T28SOI_LL_-NAND2X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

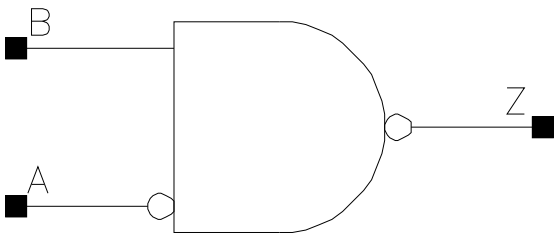
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X13_P16	C12T28SOI_LL_-NAND2X17_P16	C12T28SOI_LL_-NAND2X20_P16	C12T28SOI_LL_-NAND2X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P16	C12T28SOI_LL_-NAND2X42_P16	C12T28SOI_LL_-NAND2X47_P16	C12T28SOI_LL_-NAND2X50_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P16	C12T28SOI_LL_-NAND2X67_P16	C12T28SOI_-LLBR0D8_-NAND2X7_P16	C12T28SOI_-LLBR0D8_-NAND2X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P16	C12T28SOI_LLS_-NAND2X54_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X7_P16	1.200	0.544	0.6528
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X40_P16	1.200	2.312	2.7744
X54_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P16	X7_P16	X13_P16	X27_P16
A	0.0010	0.0010	0.0014	0.0026
B	0.0007	0.0010	0.0020	0.0040
	X40_P16	X54_P16		
A	0.0039	0.0051		
B	0.0059	0.0080		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0236	0.0256	5.3137	2.9435
A to Z ↑	0.0192	0.0205	4.9613	2.6784
B to Z ↓	0.0097	0.0086	5.4780	3.0153
B to Z ↑	0.0113	0.0094	5.1621	2.7700
	X13_P16	**X27_P16**	**X13_P16**	**X27_P16**

A to Z ↓	0.0242	0.0236	1.5862	0.7855
A to Z ↑	0.0200	0.0195	1.3760	0.6668
B to Z ↓	0.0083	0.0083	1.6264	0.8059
B to Z ↑	0.0086	0.0083	1.3846	0.6831
	X40_P16	**X54_P16**	**X40_P16**	**X54_P16**
A to Z ↓	0.0239	0.0239	0.5239	0.3971
A to Z ↑	0.0200	0.0199	0.4443	0.3352
B to Z ↓	0.0083	0.0084	0.5371	0.4070
B to Z ↑	0.0083	0.0083	0.4582	0.3458

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	9.809e-06	1.000e-20
X7_P16	1.602e-05	1.000e-20
X13_P16	3.325e-05	1.000e-20
X27_P16	6.500e-05	1.000e-20
X40_P16	9.574e-05	1.000e-20
X54_P16	1.265e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	1.676e-03	2.118e-03	3.599e-03	7.052e-03
B (output stable)	2.819e-05	5.203e-05	3.207e-04	5.407e-04
A to Z	2.720e-03	3.829e-03	7.092e-03	1.402e-02
B to Z	9.503e-04	1.560e-03	2.952e-03	5.912e-03
	X40_P16	X54_P16		
A (output stable)	1.078e-02	1.420e-02		
B (output stable)	7.714e-04	1.026e-03		
A to Z	2.113e-02	2.788e-02		
B to Z	8.702e-03	1.149e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

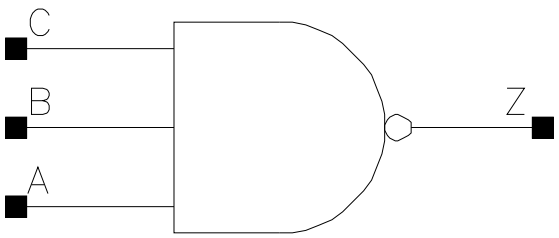
Pin Cycle (vdds)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P16	X54_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P16	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P16	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P16	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P16	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P16	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P16	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P16	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P16	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P16	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P16	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P16	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P16	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P16	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P16	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P16	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A	0.0009	0.0011	0.0018	0.0022
B	0.0009	0.0011	0.0017	0.0021
C	0.0008	0.0010	0.0016	0.0020
	C12T28SOI_LL_-NAND3X15_P16	C12T28SOI_LL_-NAND3X18_P16	C12T28SOI_LL_-NAND3X21_P16	C12T28SOI_LL_-NAND3X24_P16
A	0.0028	0.0032	0.0039	0.0043
B	0.0027	0.0031	0.0037	0.0041
C	0.0026	0.0029	0.0035	0.0039
	C12T28SOI_LL_-NAND3X35_P16	C12T28SOI_LL_-NAND3X47_P16	C12T28SOI_-LLBR0P6_-NAND3X6_P16	C12T28SOI_-LLBR0P6_-NAND3X12_P16
A	0.0065	0.0087	0.0011	0.0022
B	0.0062	0.0083	0.0011	0.0021
C	0.0059	0.0080	0.0010	0.0020
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	C12T28SOI_-LLBR0P6_-NAND3X24_P16	C12T28SOI_-LLBR0P6_-NAND3X35_P16	C12T28SOI_-LLBR0P6_-NAND3X47_P16
A	0.0032	0.0043	0.0064	0.0086
B	0.0030	0.0041	0.0061	0.0081
C	0.0028	0.0038	0.0057	0.0076
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16			
A	0.0033			
B	0.0032			
C	0.0029			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16
A to Z ↓	0.0135	0.0125	5.5879	4.0562
A to Z ↑	0.0167	0.0152	3.7935	2.6530
B to Z ↓	0.0147	0.0132	5.6113	4.0723
B to Z ↑	0.0157	0.0140	3.8040	2.6595
C to Z ↓	0.0138	0.0127	5.6366	4.0899
C to Z ↑	0.0130	0.0114	3.8113	2.6802

	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A to Z ↓	0.0136	0.0129	2.7270	2.1433
A to Z ↑	0.0159	0.0148	1.7835	1.3561
B to Z ↓	0.0132	0.0126	2.7373	2.1514
B to Z ↑	0.0142	0.0132	1.7870	1.3587
C to Z ↓	0.0127	0.0122	2.7490	2.1607
C to Z ↑	0.0114	0.0104	1.7842	1.3509
	C12T28SOI_LL_-NAND3X15_P16	**C12T28SOI_LL_-NAND3X18_P16**	**C12T28SOI_LL_-NAND3X15_P16**	**C12T28SOI_LL_-NAND3X18_P16**
A to Z ↓	0.0122	0.0120	1.7121	1.4750
A to Z ↑	0.0145	0.0141	1.0755	0.9013
B to Z ↓	0.0125	0.0123	1.7197	1.4809
B to Z ↑	0.0129	0.0125	1.0787	0.9037
C to Z ↓	0.0122	0.0120	1.7278	1.4873
C to Z ↑	0.0104	0.0099	1.0871	0.9110
	C12T28SOI_LL_-NAND3X21_P16	**C12T28SOI_LL_-NAND3X24_P16**	**C12T28SOI_LL_-NAND3X21_P16**	**C12T28SOI_LL_-NAND3X24_P16**
A to Z ↓	0.0127	0.0125	1.2426	1.1172
A to Z ↑	0.0146	0.0143	0.7728	0.6818
B to Z ↓	0.0125	0.0124	1.2477	1.1216
B to Z ↑	0.0130	0.0127	0.7744	0.6830
C to Z ↓	0.0123	0.0122	1.2531	1.1265
C to Z ↑	0.0104	0.0100	0.7762	0.6843
	C12T28SOI_LL_-NAND3X35_P16	**C12T28SOI_LL_-NAND3X47_P16**	**C12T28SOI_LL_-NAND3X35_P16**	**C12T28SOI_LL_-NAND3X47_P16**
A to Z ↓	0.0120	0.0123	0.7603	0.5785
A to Z ↑	0.0140	0.0142	0.4564	0.3447
B to Z ↓	0.0123	0.0124	0.7636	0.5808
B to Z ↑	0.0123	0.0124	0.4567	0.3442
C to Z ↓	0.0121	0.0121	0.7673	0.5837
C to Z ↑	0.0097	0.0096	0.4600	0.3462
	C12T28SOI_-LLBR0P6_-NAND3X6_P16	**C12T28SOI_-LLBR0P6_-NAND3X12_P16**	**C12T28SOI_-LLBR0P6_-NAND3X6_P16**	**C12T28SOI_-LLBR0P6_-NAND3X12_P16**
A to Z ↓	0.0092	0.0098	2.7748	1.4691
A to Z ↑	0.0226	0.0224	4.0627	2.0732
B to Z ↓	0.0094	0.0088	2.7994	1.4826
B to Z ↑	0.0199	0.0189	4.0775	2.0781
C to Z ↓	0.0078	0.0070	2.8334	1.5016
C to Z ↑	0.0150	0.0136	4.1052	2.0866
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	**C12T28SOI_-LLBR0P6_-NAND3X24_P16**	**C12T28SOI_-LLBR0P6_-NAND3X18_P16**	**C12T28SOI_-LLBR0P6_-NAND3X24_P16**
A to Z ↓	0.0090	0.0095	1.0138	0.7686
A to Z ↑	0.0213	0.0216	1.3789	1.0415
B to Z ↓	0.0084	0.0085	1.0234	0.7759
B to Z ↑	0.0178	0.0182	1.3838	1.0441
C to Z ↓	0.0071	0.0070	1.0352	0.7855
C to Z ↑	0.0130	0.0131	1.3953	1.0468
	C12T28SOI_-LLBR0P6_-NAND3X35_P16	**C12T28SOI_-LLBR0P6_-NAND3X47_P16**	**C12T28SOI_-LLBR0P6_-NAND3X35_P16**	**C12T28SOI_-LLBR0P6_-NAND3X47_P16**

A to Z ↓	0.0090	0.0093	0.5254	0.4014
A to Z ↑	0.0217	0.0217	0.7150	0.5403
B to Z ↓	0.0085	0.0086	0.5308	0.4054
B to Z ↑	0.0181	0.0181	0.7161	0.5408
C to Z ↓	0.0070	0.0074	0.5374	0.4100
C to Z ↑	0.0130	0.0133	0.7248	0.5433
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P16**	
A to Z ↓	0.0100		1.0035	
A to Z ↑	0.0217		1.3308	
B to Z ↓	0.0088		1.0121	
B to Z ↑	0.0182		1.3342	
C to Z ↓	0.0071		1.0240	
C to Z ↑	0.0130		1.3262	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P16	6.736e-06	1.000e-20
C12T28SOI_LL_NAND3X6_P16	1.027e-05	1.000e-20
C12T28SOI_LL_NAND3X9_P16	1.393e-05	1.000e-20
C12T28SOI_LL_NAND3X12_P16	1.935e-05	1.000e-20
C12T28SOI_LL_NAND3X15_P16	2.242e-05	1.000e-20
C12T28SOI_LL_NAND3X18_P16	2.745e-05	1.000e-20
C12T28SOI_LL_NAND3X21_P16	3.213e-05	1.000e-20
C12T28SOI_LL_NAND3X24_P16	3.700e-05	1.000e-20
C12T28SOI_LL_NAND3X35_P16	5.470e-05	1.000e-20
C12T28SOI_LL_NAND3X47_P16	7.232e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_-P16	9.929e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P16	1.828e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P16	2.521e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P16	3.425e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P16	5.027e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P16	6.617e-05	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P16	3.030e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A (output stable)	2.751e-05	3.718e-05	9.030e-05	1.067e-04
B (output stable)	7.355e-05	9.415e-05	2.381e-04	2.763e-04
C (output stable)	3.169e-04	3.797e-04	6.180e-04	7.107e-04
A to Z	2.250e-03	2.863e-03	4.539e-03	5.516e-03
B to Z	1.992e-03	2.494e-03	3.722e-03	4.543e-03
C to Z	1.605e-03	2.024e-03	2.968e-03	3.634e-03

	C12T28SOI_LL_-NAND3X15_P16	C12T28SOI_LL_-NAND3X18_P16	C12T28SOI_LL_-NAND3X21_P16	C12T28SOI_LL_-NAND3X24_P16
A (output stable)	1.170e-04	1.329e-04	1.823e-04	1.999e-04
B (output stable)	3.066e-04	3.512e-04	4.715e-04	5.168e-04
C (output stable)	7.544e-04	8.648e-04	1.183e-03	1.276e-03
A to Z	6.652e-03	7.651e-03	9.438e-03	1.043e-02
B to Z	5.473e-03	6.276e-03	7.763e-03	8.560e-03
C to Z	4.440e-03	5.067e-03	6.224e-03	6.860e-03
	C12T28SOI_LL_-NAND3X35_P16	C12T28SOI_LL_-NAND3X47_P16	C12T28SOI_-LLBR0P6_-NAND3X6_P16	C12T28SOI_-LLBR0P6_-NAND3X12_P16
A (output stable)	2.653e-04	3.515e-04	5.235e-05	1.501e-04
B (output stable)	7.001e-04	9.276e-04	1.341e-04	3.997e-04
C (output stable)	1.832e-03	2.367e-03	5.080e-04	1.014e-03
A to Z	1.516e-02	2.007e-02	3.104e-03	6.089e-03
B to Z	1.243e-02	1.645e-02	2.534e-03	4.606e-03
C to Z	9.851e-03	1.309e-02	1.795e-03	3.129e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	C12T28SOI_-LLBR0P6_-NAND3X24_P16	C12T28SOI_-LLBR0P6_-NAND3X35_P16	C12T28SOI_-LLBR0P6_-NAND3X47_P16
A (output stable)	1.835e-04	2.798e-04	3.724e-04	4.865e-04
B (output stable)	4.984e-04	7.426e-04	1.009e-03	1.299e-03
C (output stable)	1.198e-03	1.844e-03	2.694e-03	3.442e-03
A to Z	8.381e-03	1.147e-02	1.674e-02	2.200e-02
B to Z	6.306e-03	8.641e-03	1.255e-02	1.663e-02
C to Z	4.421e-03	5.916e-03	8.466e-03	1.132e-02
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16			
A (output stable)	2.183e-04			
B (output stable)	5.907e-04			
C (output stable)	1.465e-03			
A to Z	9.089e-03			
B to Z	6.881e-03			
C to Z	4.688e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P16	C12T28SOI_LL_-NAND3X18_P16	C12T28SOI_LL_-NAND3X21_P16	C12T28SOI_LL_-NAND3X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

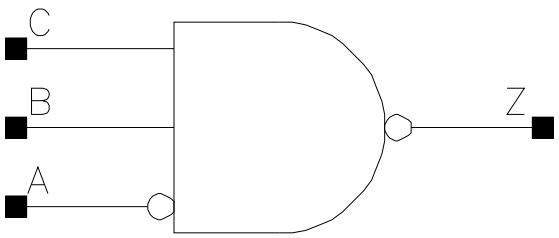
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P16	C12T28SOI_LL_-NAND3X47_P16	C12T28SOI_-LLBR0P6_-NAND3X6_P16	C12T28SOI_-LLBR0P6_-NAND3X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	C12T28SOI_-LLBR0P6_-NAND3X24_P16	C12T28SOI_-LLBR0P6_-NAND3X35_P16	C12T28SOI_-LLBR0P6_-NAND3X47_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.816	0.9792
X12_P16	1.200	1.224	1.4688
X18_P16	1.200	1.496	1.7952
X24_P16	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0010	0.0014	0.0014	0.0025
B	0.0011	0.0021	0.0031	0.0041
C	0.0010	0.0020	0.0029	0.0039

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X12_P16**	**X6_P16**	**X12_P16**
A to Z ↓	0.0291	0.0284	4.0390	2.1558
A to Z ↑	0.0221	0.0221	2.6069	1.3092
B to Z ↓	0.0117	0.0121	4.0735	2.1754
B to Z ↑	0.0125	0.0126	2.6686	1.3430
C to Z ↓	0.0121	0.0114	4.0973	2.1848
C to Z ↑	0.0106	0.0096	2.6875	1.3542
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0328	0.0277	1.4730	1.1172

A to Z ↑	0.0257	0.0211	0.8814	0.6605
B to Z ↓	0.0123	0.0119	1.4838	1.1268
B to Z ↑	0.0124	0.0122	0.9041	0.6799
C to Z ↓	0.0121	0.0115	1.4901	1.1318
C to Z ↑	0.0101	0.0093	0.9111	0.6858

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P16	1.436e-05	1.000e-20
X12_P16	3.000e-05	1.000e-20
X18_P16	3.789e-05	1.000e-20
X24_P16	5.892e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	2.088e-03	3.814e-03	5.044e-03	7.256e-03
B (output stable)	7.534e-05	2.269e-04	3.766e-04	5.192e-04
C (output stable)	1.734e-04	7.112e-04	8.688e-04	1.318e-03
A to Z	4.526e-03	8.952e-03	1.279e-02	1.726e-02
B to Z	2.166e-03	4.280e-03	6.289e-03	8.151e-03
C to Z	1.835e-03	3.328e-03	5.078e-03	6.355e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

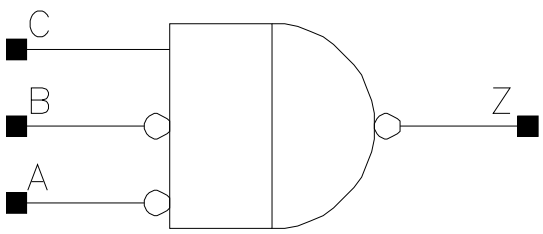
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	0.816	0.9792
X13_P16	1.200	1.088	1.3056
X20_P16	1.200	1.632	1.9584
X27_P16	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P16	X13_P16	X20_P16	X27_P16
A	0.0013	0.0013	0.0025	0.0023
B	0.0014	0.0013	0.0026	0.0024
C	0.0011	0.0021	0.0030	0.0040

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	**X13_P16**	**X7_P16**	**X13_P16**
A to Z ↓	0.0257	0.0320	2.8383	1.5069
A to Z ↑	0.0192	0.0225	2.5872	1.3028
B to Z ↓	0.0269	0.0334	2.8393	1.5068
B to Z ↑	0.0177	0.0211	2.5838	1.3001
C to Z ↓	0.0085	0.0081	2.9017	1.5339
C to Z ↑	0.0094	0.0085	2.6723	1.3506
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0291	0.0321	1.0255	0.7802
A to Z ↑	0.0209	0.0253	0.8780	0.6595
B to Z ↓	0.0287	0.0323	1.0249	0.7802

B to Z ↑	0.0187	0.0235	0.8755	0.6585
C to Z ↓	0.0090	0.0086	1.0458	0.7948
C to Z ↑	0.0091	0.0087	0.9092	0.6835

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X7_P16	2.106e-05	1.000e-20
X13_P16	2.840e-05	1.000e-20
X20_P16	4.681e-05	1.000e-20
X27_P16	5.234e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	1.149e-03	1.536e-03	2.611e-03	3.022e-03
B (output stable)	1.032e-03	1.417e-03	2.352e-03	2.800e-03
C (output stable)	5.524e-05	3.943e-04	3.305e-04	4.483e-04
A to Z	5.130e-03	8.461e-03	1.326e-02	1.664e-02
B to Z	4.701e-03	8.036e-03	1.191e-02	1.542e-02
C to Z	1.626e-03	2.994e-03	4.696e-03	6.183e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

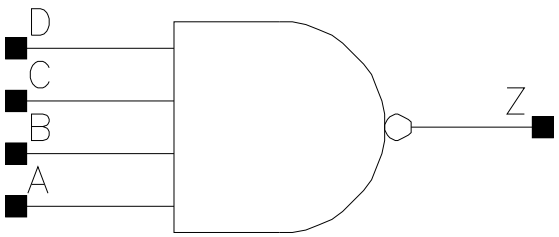
Pin Cycle (vdds)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0008	0.0008	0.0010	0.0012
B	0.0009	0.0009	0.0011	0.0014
C	0.0008	0.0009	0.0011	0.0013
D	0.0008	0.0009	0.0011	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0419	0.0422	1.7899	0.8952
A to Z ↑	0.0356	0.0390	2.6392	1.3112
B to Z ↓	0.0437	0.0447	1.7900	0.8953
B to Z ↑	0.0338	0.0380	2.6419	1.3110
C to Z ↓	0.0422	0.0421	1.7900	0.8955
C to Z ↑	0.0360	0.0402	2.6372	1.3097

D to Z ↓	0.0443	0.0440	1.7899	0.8956
D to Z ↑	0.0347	0.0383	2.6384	1.3090
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0452	0.0423	0.6165	0.4612
A to Z ↑	0.0380	0.0378	0.8840	0.6631
B to Z ↓	0.0473	0.0442	0.6164	0.4613
B to Z ↑	0.0366	0.0363	0.8828	0.6628
C to Z ↓	0.0423	0.0394	0.6162	0.4608
C to Z ↑	0.0381	0.0376	0.8824	0.6612
D to Z ↓	0.0443	0.0413	0.6162	0.4609
D to Z ↑	0.0363	0.0359	0.8821	0.6611

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	2.218e-05	1.000e-20
X17_P16	3.449e-05	1.000e-20
X25_P16	4.980e-05	1.000e-20
X33_P16	6.812e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	8.201e-04	1.012e-03	1.488e-03	1.790e-03
B (output stable)	7.506e-04	9.464e-04	1.389e-03	1.666e-03
C (output stable)	7.924e-04	9.365e-04	1.422e-03	1.639e-03
D (output stable)	7.196e-04	8.612e-04	1.311e-03	1.502e-03
A to Z	6.054e-03	9.478e-03	1.460e-02	1.825e-02
B to Z	5.867e-03	9.298e-03	1.432e-02	1.790e-02
C to Z	6.118e-03	9.256e-03	1.373e-02	1.699e-02
D to Z	5.939e-03	9.061e-03	1.344e-02	1.664e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

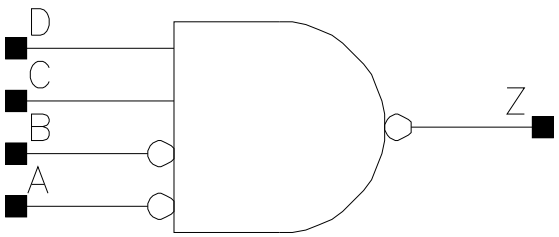
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X12_P16	1.200	1.496	1.7952
X18_P16	1.200	2.040	2.4480
X24_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0013	0.0014	0.0025	0.0023
B	0.0013	0.0017	0.0026	0.0024
C	0.0010	0.0021	0.0030	0.0042
D	0.0010	0.0020	0.0029	0.0040

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X12_P16	X6_P16	X12_P16
A to Z ↓	0.0276	0.0374	4.1600	2.1602
A to Z ↑	0.0205	0.0253	2.5888	1.3049
B to Z ↓	0.0283	0.0381	4.1603	2.1604
B to Z ↑	0.0183	0.0236	2.5856	1.3043
C to Z ↓	0.0117	0.0120	4.1938	2.1741
C to Z ↑	0.0127	0.0125	2.8246	1.3426

D to Z ↓	0.0121	0.0114	4.2156	2.1834
D to Z ↑	0.0106	0.0096	2.8439	1.3539
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0325	0.0362	1.4707	1.1186
A to Z ↑	0.0224	0.0287	0.8787	0.6602
B to Z ↓	0.0322	0.0360	1.4709	1.1184
B to Z ↑	0.0202	0.0265	0.8767	0.6594
C to Z ↓	0.0121	0.0124	1.4806	1.1249
C to Z ↑	0.0123	0.0125	0.9073	0.6783
D to Z ↓	0.0119	0.0120	1.4875	1.1299
D to Z ↑	0.0099	0.0097	0.9259	0.6847

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P16	1.841e-05	1.000e-20
X12_P16	2.575e-05	1.000e-20
X18_P16	4.246e-05	1.000e-20
X24_P16	4.621e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	1.333e-03	2.135e-03	3.311e-03	3.903e-03
B (output stable)	1.178e-03	1.954e-03	2.921e-03	3.519e-03
C (output stable)	9.622e-05	2.637e-04	4.026e-04	5.693e-04
D (output stable)	2.136e-04	7.910e-04	9.660e-04	1.503e-03
A to Z	5.400e-03	1.009e-02	1.501e-02	1.953e-02
B to Z	4.998e-03	9.494e-03	1.374e-02	1.821e-02
C to Z	2.100e-03	4.261e-03	6.179e-03	8.502e-03
D to Z	1.772e-03	3.318e-03	5.012e-03	6.721e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

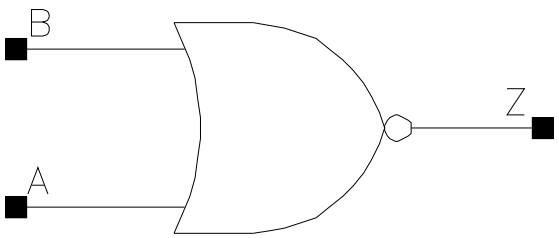
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.408	0.4896
X5_P16	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X10_P16	1.200	0.680	0.8160
X14_P16	1.200	0.680	0.8160
X17_P16	1.200	0.952	1.1424
X21_P16	1.200	0.952	1.1424
X24_P16	1.200	1.224	1.4688
X27_P16	1.200	1.224	1.4688
X34_P16	1.200	1.496	1.7952
X40_P16	1.200	1.360	1.6320
X41_P16	1.200	1.768	2.1216
X49_P16	1.200	1.496	1.7952
X53_P16	1.200	1.904	2.2848
X55_P16	1.200	2.312	2.7744
X57_P16	1.200	1.904	2.2848
X65_P16	1.200	2.040	2.4480
X84_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P16	X5_P16	X7_P16	X10_P16
A	0.0007	0.0008	0.0011	0.0018
B	0.0007	0.0008	0.0011	0.0016
	X14_P16	X17_P16	X21_P16	X24_P16

A	0.0022	0.0029	0.0033	0.0039
B	0.0020	0.0026	0.0030	0.0036
	X27_P16	X34_P16	X40_P16	X41_P16
A	0.0043	0.0054	0.0012	0.0067
B	0.0040	0.0050	0.0014	0.0061
	X49_P16	X53_P16	X55_P16	X57_P16
A	0.0013	0.0013	0.0088	0.0013
B	0.0014	0.0012	0.0081	0.0012
	X65_P16	X84_P16		
A	0.0013	0.0014		
B	0.0012	0.0013		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X5_P16**	**X3_P16**	**X5_P16**
A to Z ↓	0.0080	0.0076	3.4299	2.5019
A to Z ↑	0.0136	0.0126	8.8537	6.5323
B to Z ↓	0.0064	0.0059	3.5123	2.5266
B to Z ↑	0.0144	0.0132	8.9075	6.5631
	X7_P16	**X10_P16**	**X7_P16**	**X10_P16**
A to Z ↓	0.0076	0.0078	1.8504	1.1934
A to Z ↑	0.0118	0.0132	4.6543	3.0973
B to Z ↓	0.0057	0.0051	1.8755	1.2078
B to Z ↑	0.0123	0.0116	4.6814	3.1110
	X14_P16	**X17_P16**	**X14_P16**	**X17_P16**
A to Z ↓	0.0078	0.0078	0.9126	0.7311
A to Z ↑	0.0123	0.0125	2.3128	1.8612
B to Z ↓	0.0050	0.0057	0.9242	0.7391
B to Z ↑	0.0110	0.0119	2.3248	1.8705
	X21_P16	**X24_P16**	**X21_P16**	**X24_P16**
A to Z ↓	0.0079	0.0077	0.6222	0.5291
A to Z ↑	0.0120	0.0122	1.5562	1.3556
B to Z ↓	0.0057	0.0052	0.6290	0.5357
B to Z ↑	0.0116	0.0114	1.5639	1.3626
	X27_P16	**X34_P16**	**X27_P16**	**X34_P16**
A to Z ↓	0.0077	0.0080	0.4705	0.3796
A to Z ↑	0.0118	0.0120	1.1966	0.9524
B to Z ↓	0.0052	0.0056	0.4766	0.3841
B to Z ↑	0.0111	0.0115	1.2029	0.9569
	X40_P16	**X41_P16**	**X40_P16**	**X41_P16**
A to Z ↓	0.0317	0.0079	0.3764	0.3162
A to Z ↑	0.0406	0.0118	0.5429	0.7883
B to Z ↓	0.0302	0.0054	0.3761	0.3202
B to Z ↑	0.0422	0.0111	0.5428	0.7925
	X49_P16	**X53_P16**	**X49_P16**	**X53_P16**
A to Z ↓	0.0334	0.0347	0.3126	0.2859
A to Z ↑	0.0422	0.0479	0.4518	0.4163
B to Z ↓	0.0318	0.0332	0.3126	0.2860
B to Z ↑	0.0437	0.0493	0.4515	0.4163
	X55_P16	**X57_P16**	**X55_P16**	**X57_P16**
A to Z ↓	0.0080	0.0350	0.2389	0.2690
A to Z ↑	0.0119	0.0481	0.5944	0.3884

B to Z ↓	0.0055	0.0335	0.2423	0.2693
B to Z ↑	0.0111	0.0495	0.5974	0.3885
	X65_P16	**X84_P16**	**X65_P16**	**X84_P16**
A to Z ↓	0.0360	0.0379	0.2362	0.1876
A to Z ↑	0.0490	0.0500	0.3399	0.2698
B to Z ↓	0.0345	0.0363	0.2362	0.1877
B to Z ↑	0.0503	0.0513	0.3401	0.2699

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	5.445e-06	1.000e-20
X5_P16	8.014e-06	1.000e-20
X7_P16	1.197e-05	1.000e-20
X10_P16	1.676e-05	1.000e-20
X14_P16	2.373e-05	1.000e-20
X17_P16	2.817e-05	1.000e-20
X21_P16	3.484e-05	1.000e-20
X24_P16	3.960e-05	1.000e-20
X27_P16	4.596e-05	1.000e-20
X34_P16	5.708e-05	1.000e-20
X40_P16	8.607e-05	1.000e-20
X41_P16	6.821e-05	1.000e-20
X49_P16	9.779e-05	1.000e-20
X53_P16	1.121e-04	1.000e-20
X55_P16	9.045e-05	1.000e-20
X57_P16	1.192e-04	1.000e-20
X65_P16	1.310e-04	1.000e-20
X84_P16	1.565e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	2.154e-05	2.884e-05	3.901e-05	1.222e-04
B (output stable)	4.067e-05	5.376e-05	7.496e-05	3.321e-04
A to Z	1.123e-03	1.423e-03	1.923e-03	3.165e-03
B to Z	9.038e-04	1.131e-03	1.509e-03	2.172e-03
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	1.424e-04	1.687e-04	1.901e-04	2.324e-04
B (output stable)	4.036e-04	4.118e-04	4.524e-04	5.921e-04
A to Z	4.019e-03	5.047e-03	5.877e-03	6.877e-03
B to Z	2.809e-03	3.704e-03	4.322e-03	4.931e-03
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	2.526e-04	3.022e-04	3.968e-05	3.922e-04
B (output stable)	6.392e-04	6.517e-04	7.504e-05	9.519e-04
A to Z	7.673e-03	9.642e-03	1.771e-02	1.155e-02
B to Z	5.507e-03	7.102e-03	1.732e-02	8.241e-03
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	3.998e-05	4.045e-05	5.152e-04	4.024e-05
B (output stable)	7.519e-05	7.925e-05	1.241e-03	7.904e-05
A to Z	2.041e-02	2.477e-02	1.533e-02	2.567e-02
B to Z	2.002e-02	2.434e-02	1.096e-02	2.524e-02
	X65_P16	X84_P16		

A (output stable)	4.106e-05	4.297e-05		
B (output stable)	7.975e-05	8.115e-05		
A to Z	2.816e-02	3.420e-02		
B to Z	2.772e-02	3.369e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

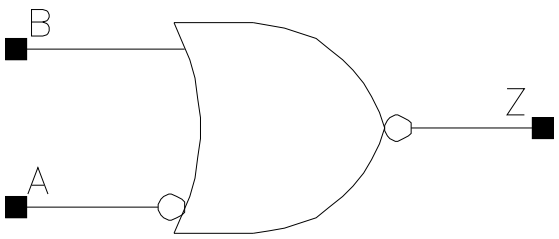
Pin Cycle (vdds)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P16	X84_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X7_P16	1.200	0.680	0.8160
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X41_P16	1.200	2.312	2.7744
X55_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X7_P16	X13_P16
A	0.0010	0.0010	0.0010	0.0014
B	0.0007	0.0011	0.0011	0.0020
	X27_P16	X41_P16	X55_P16	
A	0.0026	0.0039	0.0050	
B	0.0041	0.0061	0.0081	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0226	0.0256	3.2606	2.1624
A to Z ↑	0.0210	0.0214	8.7606	4.6204
B to Z ↓	0.0067	0.0071	3.4861	2.3139
B to Z ↑	0.0145	0.0119	8.8873	4.6964

	X7_P16	X13_P16	X7_P16	X13_P16
A to Z ↓	0.0259	0.0237	1.7298	0.9391
A to Z ↑	0.0236	0.0228	4.5837	2.4418
B to Z ↓	0.0061	0.0054	1.7988	0.9714
B to Z ↑	0.0134	0.0121	4.6357	2.4732
	X27_P16	**X41_P16**	**X27_P16**	**X41_P16**
A to Z ↓	0.0230	0.0234	0.4484	0.3033
A to Z ↑	0.0219	0.0222	1.1668	0.7834
B to Z ↓	0.0053	0.0054	0.4793	0.3225
B to Z ↑	0.0114	0.0113	1.1828	0.7936
	X55_P16		**X55_P16**	
A to Z ↓	0.0231		0.2295	
A to Z ↑	0.0219		0.5913	
B to Z ↓	0.0054		0.2441	
B to Z ↑	0.0112		0.5990	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	9.947e-06	1.000e-20
X6_P16	1.591e-05	1.000e-20
X7_P16	1.777e-05	1.000e-20
X13_P16	3.407e-05	1.000e-20
X27_P16	6.736e-05	1.000e-20
X41_P16	9.937e-05	1.000e-20
X55_P16	1.314e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	1.659e-03	2.058e-03	2.190e-03	3.647e-03
B (output stable)	4.077e-05	7.473e-05	1.987e-04	3.517e-04
A to Z	2.731e-03	3.773e-03	4.341e-03	7.401e-03
B to Z	9.119e-04	1.443e-03	1.715e-03	2.912e-03
	X27_P16	X41_P16	X55_P16	
A (output stable)	7.251e-03	1.094e-02	1.439e-02	
B (output stable)	6.824e-04	9.689e-04	1.268e-03	
A to Z	1.481e-02	2.208e-02	2.918e-02	
B to Z	5.756e-03	8.458e-03	1.114e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

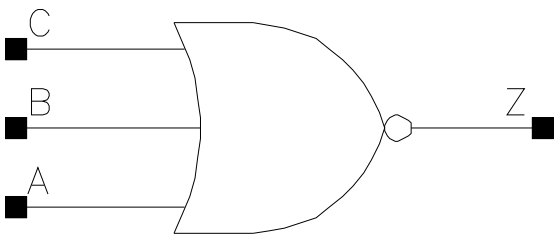
Pin Cycle (vdds)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P16	X41_P16	X55_P16	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X9_P16	1.200	0.952	1.1424
X13_P16	1.200	0.952	1.1424
X16_P16	1.200	1.360	1.6320
X19_P16	1.200	1.496	1.7952
X22_P16	1.200	1.768	2.1216
X25_P16	1.200	1.904	2.2848
X37_P16	1.200	2.584	3.1008
X49_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P16	X6_P16	X9_P16	X13_P16
A	0.0009	0.0011	0.0017	0.0021
B	0.0008	0.0011	0.0019	0.0022
C	0.0008	0.0011	0.0016	0.0020
	X16_P16	X19_P16	X22_P16	X25_P16
A	0.0028	0.0033	0.0038	0.0043
B	0.0028	0.0036	0.0040	0.0048
C	0.0025	0.0029	0.0036	0.0039
	X37_P16	X49_P16		
A	0.0064	0.0087		
B	0.0066	0.0088		

C	0.0058	0.0080		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0095	0.0093	2.5345	1.8757
A to Z ↑	0.0186	0.0170	9.3207	6.6376
B to Z ↓	0.0088	0.0084	2.5396	1.8768
B to Z ↑	0.0179	0.0162	9.3347	6.6478
C to Z ↓	0.0072	0.0066	2.5638	1.8991
C to Z ↑	0.0177	0.0158	9.3521	6.6598
	X9_P16	**X13_P16**	**X9_P16**	**X13_P16**
A to Z ↓	0.0095	0.0095	1.2273	0.9463
A to Z ↑	0.0187	0.0175	4.3999	3.3028
B to Z ↓	0.0086	0.0084	1.1997	0.9115
B to Z ↑	0.0185	0.0169	4.4097	3.3100
C to Z ↓	0.0061	0.0059	1.2134	0.9285
C to Z ↑	0.0149	0.0141	4.4095	3.3103
	X16_P16	**X19_P16**	**X16_P16**	**X19_P16**
A to Z ↓	0.0094	0.0093	0.7357	0.6233
A to Z ↑	0.0179	0.0176	2.6645	2.2130
B to Z ↓	0.0088	0.0087	0.7374	0.6112
B to Z ↑	0.0174	0.0175	2.6690	2.2172
C to Z ↓	0.0064	0.0063	0.7430	0.6346
C to Z ↑	0.0155	0.0147	2.6715	2.2190
	X22_P16	**X25_P16**	**X22_P16**	**X25_P16**
A to Z ↓	0.0094	0.0094	0.5389	0.4740
A to Z ↑	0.0177	0.0176	1.9046	1.6634
B to Z ↓	0.0086	0.0085	0.5305	0.4582
B to Z ↑	0.0171	0.0175	1.9088	1.6668
C to Z ↓	0.0060	0.0060	0.5372	0.4752
C to Z ↑	0.0145	0.0141	1.9100	1.6676
	X37_P16	**X49_P16**	**X37_P16**	**X49_P16**
A to Z ↓	0.0094	0.0095	0.3257	0.2464
A to Z ↑	0.0170	0.0170	1.1156	0.8405
B to Z ↓	0.0086	0.0087	0.3226	0.2442
B to Z ↑	0.0163	0.0163	1.1178	0.8422
C to Z ↓	0.0064	0.0066	0.3268	0.2475
C to Z ↑	0.0142	0.0144	1.1184	0.8429

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	7.005e-06	1.000e-20
X6_P16	1.053e-05	1.000e-20
X9_P16	1.482e-05	1.000e-20
X13_P16	2.115e-05	1.000e-20
X16_P16	2.508e-05	1.000e-20
X19_P16	3.189e-05	1.000e-20
X22_P16	3.539e-05	1.000e-20
X25_P16	4.212e-05	1.000e-20
X37_P16	6.164e-05	1.000e-20

X49_P16	8.194e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	3.512e-05	4.803e-05	8.739e-05	1.139e-04
B (output stable)	2.392e-05	4.038e-05	7.670e-05	1.068e-04
C (output stable)	8.650e-05	1.325e-04	3.070e-04	4.092e-04
A to Z	1.911e-03	2.486e-03	4.105e-03	5.165e-03
B to Z	1.584e-03	2.033e-03	3.439e-03	4.267e-03
C to Z	1.290e-03	1.620e-03	2.376e-03	3.006e-03
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	1.373e-04	1.650e-04	1.968e-04	2.267e-04
B (output stable)	1.165e-04	1.565e-04	1.752e-04	2.149e-04
C (output stable)	4.324e-04	5.732e-04	6.676e-04	8.091e-04
A to Z	6.539e-03	7.777e-03	9.043e-03	1.034e-02
B to Z	5.402e-03	6.492e-03	7.459e-03	8.644e-03
C to Z	4.045e-03	4.650e-03	5.356e-03	5.979e-03
	X37_P16	X49_P16		
A (output stable)	3.293e-04	4.349e-04		
B (output stable)	3.045e-04	4.006e-04		
C (output stable)	1.119e-03	1.469e-03		
A to Z	1.500e-02	1.997e-02		
B to Z	1.228e-02	1.632e-02		
C to Z	8.806e-03	1.180e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

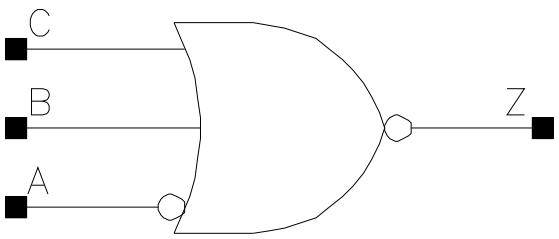
Pin Cycle (vdds)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P16	X49_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.680	0.8160
X13_P16	1.200	1.224	1.4688
X19_P16	1.200	1.496	1.7952
X25_P16	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0010	0.0014	0.0014	0.0026
B	0.0011	0.0022	0.0032	0.0043
C	0.0011	0.0020	0.0029	0.0039

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X13_P16**	**X6_P16**	**X13_P16**
A to Z ↓	0.0258	0.0253	1.7980	0.9948
A to Z ↑	0.0278	0.0279	6.6992	3.2959
B to Z ↓	0.0085	0.0084	1.8833	0.9163
B to Z ↑	0.0165	0.0169	6.7318	3.3098
C to Z ↓	0.0068	0.0059	1.8995	0.9292
C to Z ↑	0.0161	0.0141	6.7439	3.3107
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0289	0.0251	0.6075	0.4608

A to Z ↑	0.0307	0.0279	2.2212	1.6656
B to Z ↓	0.0087	0.0085	0.6345	0.4739
B to Z ↑	0.0164	0.0164	2.2330	1.6738
C to Z ↓	0.0062	0.0060	0.6357	0.4780
C to Z ↑	0.0148	0.0141	2.2349	1.6755

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P16	1.521e-05	1.000e-20
X13_P16	3.257e-05	1.000e-20
X19_P16	4.184e-05	1.000e-20
X25_P16	6.335e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	2.129e-03	3.899e-03	5.020e-03	7.649e-03
B (output stable)	4.549e-05	1.224e-04	1.685e-04	2.343e-04
C (output stable)	1.376e-04	4.525e-04	5.492e-04	8.125e-04
A to Z	4.594e-03	9.189e-03	1.261e-02	1.781e-02
B to Z	2.040e-03	4.276e-03	6.145e-03	8.229e-03
C to Z	1.636e-03	3.005e-03	4.617e-03	5.910e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

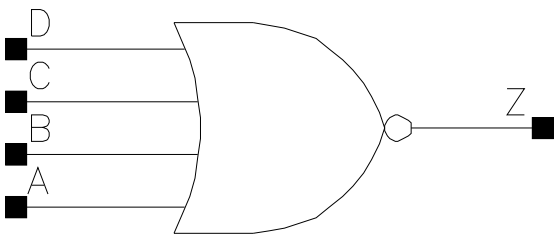
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	1.904	2.2848
X32_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X32_P16
A	0.0008	0.0009	0.0009	0.0012
B	0.0009	0.0008	0.0011	0.0014
C	0.0008	0.0008	0.0010	0.0012
D	0.0008	0.0008	0.0010	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0314	0.0317	1.7674	0.8678
A to Z ↑	0.0428	0.0466	2.6913	1.3275
B to Z ↓	0.0297	0.0305	1.7654	0.8679
B to Z ↑	0.0439	0.0480	2.6910	1.3273
C to Z ↓	0.0305	0.0315	1.7633	0.8660
C to Z ↑	0.0436	0.0480	2.6903	1.3271

D to Z ↓	0.0295	0.0307	1.7628	0.8656
D to Z ↑	0.0450	0.0498	2.6908	1.3257
	X25_P16	**X32_P16**	**X25_P16**	**X32_P16**
A to Z ↓	0.0330	0.0351	0.6022	0.4725
A to Z ↑	0.0465	0.0450	0.9077	0.6874
B to Z ↓	0.0318	0.0338	0.6014	0.4727
B to Z ↑	0.0481	0.0462	0.9076	0.6871
C to Z ↓	0.0320	0.0347	0.5995	0.4707
C to Z ↑	0.0466	0.0458	0.9065	0.6869
D to Z ↓	0.0306	0.0326	0.5995	0.4710
D to Z ↑	0.0480	0.0469	0.9061	0.6869

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	2.674e-05	1.000e-20
X17_P16	4.367e-05	1.000e-20
X25_P16	6.634e-05	1.000e-20
X32_P16	8.644e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	8.161e-04	1.007e-03	1.414e-03	1.773e-03
B (output stable)	7.292e-04	9.194e-04	1.298e-03	1.608e-03
C (output stable)	7.508e-04	8.909e-04	1.376e-03	1.747e-03
D (output stable)	6.642e-04	8.084e-04	1.251e-03	1.581e-03
A to Z	5.715e-03	9.027e-03	1.380e-02	1.731e-02
B to Z	5.486e-03	8.817e-03	1.348e-02	1.694e-02
C to Z	5.705e-03	8.914e-03	1.304e-02	1.652e-02
D to Z	5.467e-03	8.702e-03	1.274e-02	1.609e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

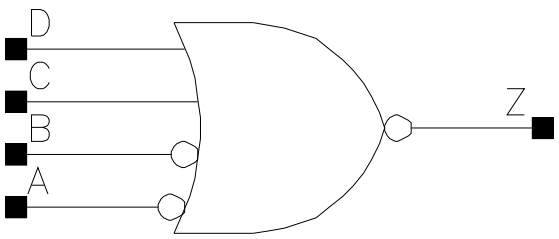
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X13_P16	1.200	1.496	1.7952
X19_P16	1.200	2.040	2.4480
X25_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0013	0.0014	0.0026	0.0025
B	0.0013	0.0018	0.0026	0.0026
C	0.0011	0.0021	0.0031	0.0042
D	0.0010	0.0020	0.0030	0.0039

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X13_P16	X6_P16	X13_P16
A to Z ↓	0.0226	0.0285	1.7485	0.8787
A to Z ↑	0.0272	0.0343	6.4605	3.3540
B to Z ↓	0.0206	0.0269	1.7471	0.8779
B to Z ↑	0.0284	0.0360	6.4622	3.3549
C to Z ↓	0.0090	0.0085	1.9105	0.9168
C to Z ↑	0.0165	0.0171	6.4968	3.3700

D to Z ↓	0.0069	0.0059	1.9177	0.9269
D to Z ↑	0.0159	0.0144	6.5032	3.3705
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0251	0.0277	0.6007	0.4523
A to Z ↑	0.0309	0.0338	2.2215	1.6802
B to Z ↓	0.0226	0.0256	0.5998	0.4521
B to Z ↑	0.0318	0.0351	2.2216	1.6802
C to Z ↓	0.0088	0.0087	0.6342	0.4751
C to Z ↑	0.0164	0.0165	2.2317	1.6866
D to Z ↓	0.0062	0.0061	0.6360	0.4775
D to Z ↑	0.0148	0.0142	2.2332	1.6872

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P16	2.061e-05	1.000e-20
X13_P16	3.034e-05	1.000e-20
X19_P16	4.955e-05	1.000e-20
X25_P16	5.829e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	1.323e-03	2.101e-03	3.279e-03	3.924e-03
B (output stable)	1.194e-03	1.980e-03	3.018e-03	3.690e-03
C (output stable)	4.934e-05	1.417e-04	2.016e-04	2.825e-04
D (output stable)	1.655e-04	4.648e-04	6.111e-04	9.084e-04
A to Z	5.592e-03	1.029e-02	1.548e-02	1.993e-02
B to Z	5.267e-03	9.784e-03	1.447e-02	1.896e-02
C to Z	2.108e-03	4.253e-03	6.127e-03	8.184e-03
D to Z	1.692e-03	3.045e-03	4.624e-03	5.923e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

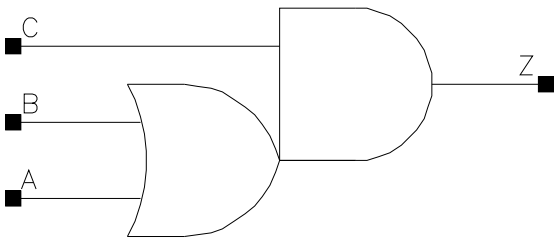
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0012	0.0013	0.0024
B	0.0013	0.0014	0.0027
C	0.0013	0.0014	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0231	0.0275	1.8157	0.9042
A to Z ↑	0.0220	0.0251	2.7054	1.3302
B to Z ↓	0.0240	0.0288	1.8167	0.9040
B to Z ↑	0.0195	0.0228	2.7001	1.3290
C to Z ↓	0.0224	0.0252	1.7954	0.8901
C to Z ↑	0.0199	0.0225	2.7005	1.3284
	X33_P16		**X33_P16**	
A to Z ↓	0.0288		0.4588	
A to Z ↑	0.0271		0.6689	

B to Z ↓	0.0300		0.4587	
B to Z ↑	0.0244		0.6674	
C to Z ↓	0.0259		0.4507	
C to Z ↑	0.0236		0.6675	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	2.498e-05	1.000e-20
X17_P16	3.695e-05	1.000e-20
X33_P16	7.360e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.076e-04	1.094e-04	2.237e-04
B (output stable)	1.262e-04	1.281e-04	2.459e-04
C (output stable)	7.026e-05	7.272e-05	1.362e-04
A to Z	4.435e-03	7.007e-03	1.477e-02
B to Z	3.982e-03	6.520e-03	1.381e-02
C to Z	4.816e-03	7.151e-03	1.491e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

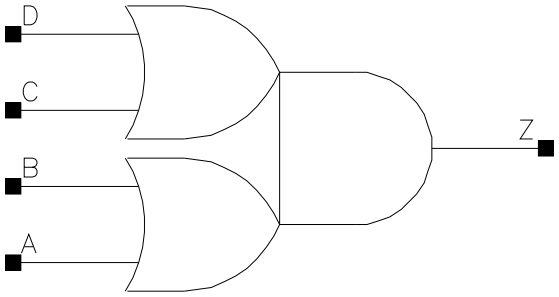
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0008	0.0012	0.0025
B	0.0009	0.0013	0.0025
C	0.0008	0.0013	0.0025
D	0.0008	0.0013	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0397	0.0345	1.7708	0.8988
A to Z ↑	0.0289	0.0263	2.6538	1.3274
B to Z ↓	0.0415	0.0360	1.7714	0.8986
B to Z ↑	0.0274	0.0245	2.6499	1.3246

C to Z ↓	0.0342	0.0300	1.7563	0.8938
C to Z ↑	0.0287	0.0270	2.6477	1.3259
D to Z ↓	0.0353	0.0311	1.7567	0.8936
D to Z ↑	0.0266	0.0244	2.6461	1.3237
	X33_P16		**X33_P16**	
A to Z ↓	0.0354		0.4615	
A to Z ↑	0.0267		0.6671	
B to Z ↓	0.0357		0.4618	
B to Z ↑	0.0244		0.6660	
C to Z ↓	0.0304		0.4588	
C to Z ↑	0.0269		0.6665	
D to Z ↓	0.0303		0.4589	
D to Z ↑	0.0242		0.6650	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	1.891e-05	1.000e-20
X17_P16	3.947e-05	1.000e-20
X33_P16	7.632e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.429e-05	3.910e-05	1.173e-04
B (output stable)	3.425e-05	5.927e-05	2.911e-04
C (output stable)	9.381e-05	1.157e-04	2.653e-04
D (output stable)	1.043e-04	1.361e-04	4.399e-04
A to Z	5.255e-03	8.844e-03	1.761e-02
B to Z	4.998e-03	8.337e-03	1.627e-02
C to Z	4.577e-03	7.861e-03	1.562e-02
D to Z	4.326e-03	7.372e-03	1.427e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

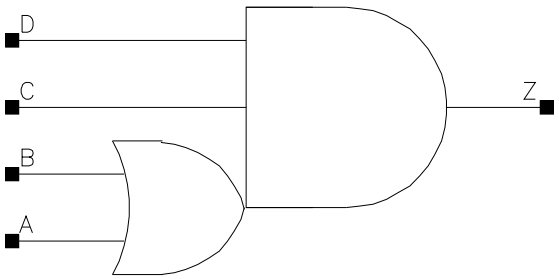
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	1.088	1.3056
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0008	0.0013	0.0021	0.0025
B	0.0008	0.0013	0.0021	0.0026
C	0.0009	0.0013	0.0022	0.0025
D	0.0008	0.0013	0.0021	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0332	0.0321	1.8514	0.9052
A to Z ↑	0.0344	0.0338	2.7459	1.3345
B to Z ↓	0.0346	0.0326	1.8515	0.9054
B to Z ↑	0.0323	0.0306	2.7434	1.3311
C to Z ↓	0.0299	0.0285	1.8128	0.8889

C to Z ↑	0.0310	0.0302	2.7398	1.3309
D to Z ↓	0.0288	0.0273	1.8109	0.8874
D to Z ↑	0.0326	0.0316	2.7413	1.3310
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0331	0.0320	0.6147	0.4604
A to Z ↑	0.0340	0.0350	0.9042	0.6777
B to Z ↓	0.0333	0.0323	0.6154	0.4607
B to Z ↑	0.0308	0.0316	0.9008	0.6754
C to Z ↓	0.0296	0.0285	0.6044	0.4524
C to Z ↑	0.0306	0.0309	0.9015	0.6757
D to Z ↓	0.0279	0.0270	0.6032	0.4512
D to Z ↑	0.0311	0.0317	0.9022	0.6760

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	1.789e-05	1.000e-20
X17_P16	3.790e-05	1.000e-20
X25_P16	5.712e-05	1.000e-20
X33_P16	7.540e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	1.089e-04	2.068e-04	3.456e-04	3.745e-04
B (output stable)	1.119e-04	2.271e-04	3.829e-04	4.164e-04
C (output stable)	2.017e-05	4.163e-05	1.023e-04	1.129e-04
D (output stable)	4.852e-05	9.607e-05	3.122e-04	3.315e-04
A to Z	4.460e-03	8.356e-03	1.313e-02	1.666e-02
B to Z	4.212e-03	7.724e-03	1.206e-02	1.531e-02
C to Z	4.704e-03	8.698e-03	1.398e-02	1.733e-02
D to Z	4.505e-03	8.323e-03	1.306e-02	1.638e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

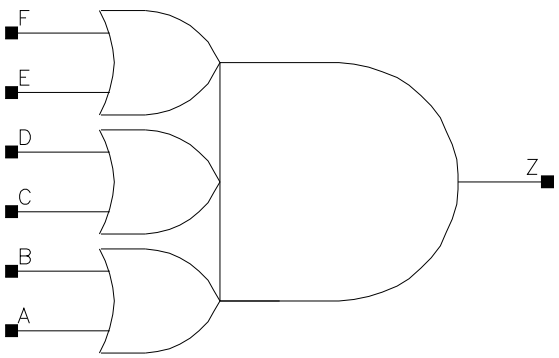
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0009	0.0012	0.0022
B	0.0008	0.0012	0.0024
C	0.0008	0.0012	0.0022
D	0.0008	0.0012	0.0024
E	0.0008	0.0012	0.0022
F	0.0008	0.0012	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0456	0.0403	1.8923	0.9205
A to Z ↑	0.0368	0.0352	2.7310	1.3444
B to Z ↓	0.0473	0.0420	1.8917	0.9207
B to Z ↑	0.0351	0.0336	2.7314	1.3442
C to Z ↓	0.0416	0.0380	1.8795	0.9184
C to Z ↑	0.0374	0.0352	2.7327	1.3444
D to Z ↓	0.0433	0.0394	1.8794	0.9185
D to Z ↑	0.0354	0.0332	2.7291	1.3435
E to Z ↓	0.0359	0.0331	1.8642	0.9128
E to Z ↑	0.0356	0.0342	2.7288	1.3427
F to Z ↓	0.0377	0.0344	1.8645	0.9130
F to Z ↑	0.0335	0.0320	2.7254	1.3408
	X33_P16		X33_P16	
A to Z ↓	0.0409		0.4698	
A to Z ↑	0.0363		0.6782	
B to Z ↓	0.0427		0.4699	
B to Z ↑	0.0335		0.6763	
C to Z ↓	0.0373		0.4668	
C to Z ↑	0.0362		0.6779	
D to Z ↓	0.0389		0.4668	
D to Z ↑	0.0336		0.6759	
E to Z ↓	0.0326		0.4640	
E to Z ↑	0.0352		0.6768	
F to Z ↓	0.0341		0.4641	
F to Z ↑	0.0324		0.6750	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	2.071e-05	1.000e-20
X17_P16	4.383e-05	1.000e-20
X33_P16	8.406e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.248e-05	3.877e-05	7.397e-05
B (output stable)	2.937e-05	5.621e-05	1.021e-04
C (output stable)	4.865e-05	7.762e-05	1.591e-04
D (output stable)	5.735e-05	9.288e-05	1.873e-04
E (output stable)	1.741e-04	2.519e-04	4.831e-04
F (output stable)	1.771e-04	2.614e-04	5.081e-04
A to Z	6.090e-03	1.060e-02	2.100e-02
B to Z	5.816e-03	1.011e-02	1.997e-02
C to Z	5.552e-03	9.817e-03	1.926e-02
D to Z	5.290e-03	9.320e-03	1.825e-02
E to Z	4.896e-03	8.823e-03	1.733e-02
F to Z	4.657e-03	8.348e-03	1.638e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

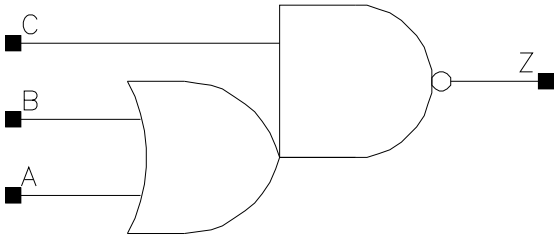
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X34_P16	1.200	2.720	3.2640
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X34_P16	X46_P16
A	0.0010	0.0031	0.0063	0.0082
B	0.0010	0.0028	0.0057	0.0076
C	0.0011	0.0033	0.0067	0.0087

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0117	0.0122	3.2476	1.0588
A to Z ↑	0.0124	0.0132	4.6604	1.5865
B to Z ↓	0.0091	0.0094	3.1966	1.0653
B to Z ↑	0.0127	0.0127	4.6874	1.5963
C to Z ↓	0.0101	0.0102	2.9505	0.9693
C to Z ↑	0.0135	0.0135	2.7346	0.9069
	X34_P16	**X46_P16**	**X34_P16**	**X46_P16**
A to Z ↓	0.0127	0.0127	0.5389	0.4109

A to Z ↑	0.0137	0.0134	0.7910	0.6079
B to Z ↓	0.0098	0.0098	0.5468	0.4185
B to Z ↑	0.0130	0.0130	0.7957	0.6116
C to Z ↓	0.0106	0.0105	0.4958	0.3785
C to Z ↑	0.0137	0.0136	0.4534	0.3459

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P16	1.415e-05	1.000e-20
X17_P16	4.179e-05	1.000e-20
X34_P16	8.320e-05	1.000e-20
X46_P16	1.100e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	9.063e-05	3.201e-04	6.846e-04	8.348e-04
B (output stable)	1.096e-04	3.870e-04	9.008e-04	1.049e-03
C (output stable)	6.324e-05	2.112e-04	4.365e-04	5.501e-04
A to Z	1.976e-03	6.275e-03	1.295e-02	1.674e-02
B to Z	1.555e-03	4.681e-03	9.583e-03	1.252e-02
C to Z	2.419e-03	7.440e-03	1.526e-02	1.982e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

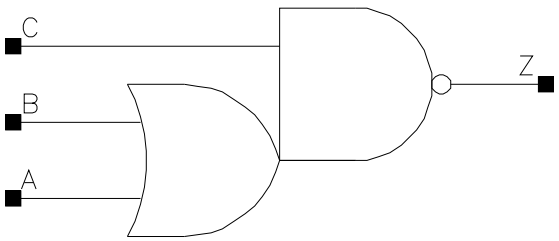
Pin Cycle (vdds)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.544	0.6528
X11_P16	1.200	0.952	1.1424
X17_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X17_P16	X23_P16
A	0.0011	0.0021	0.0033	0.0045
B	0.0010	0.0022	0.0031	0.0041
C	0.0010	0.0021	0.0030	0.0041
	X46_P16			
A	0.0089			
B	0.0081			
C	0.0084			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0114	0.0115	3.2778	1.5273
A to Z ↑	0.0164	0.0164	4.8968	2.3180
B to Z ↓	0.0092	0.0091	3.2296	1.4916

B to Z ↑	0.0170	0.0170	4.9199	2.3290
C to Z ↓	0.0095	0.0095	3.0741	1.4268
C to Z ↑	0.0098	0.0097	2.9258	1.3761
	X17_P16	**X23_P16**	**X17_P16**	**X23_P16**
A to Z ↓	0.0111	0.0117	1.0597	0.7845
A to Z ↑	0.0156	0.0171	1.5363	1.1724
B to Z ↓	0.0087	0.0091	1.0581	0.7859
B to Z ↑	0.0160	0.0167	1.5439	1.1780
C to Z ↓	0.0093	0.0095	1.0006	0.7399
C to Z ↑	0.0090	0.0093	0.9153	0.6957
	X46_P16		**X46_P16**	
A to Z ↓	0.0116		0.4082	
A to Z ↑	0.0167		0.5929	
B to Z ↓	0.0089		0.4051	
B to Z ↑	0.0164		0.5959	
C to Z ↓	0.0096		0.3835	
C to Z ↑	0.0090		0.3514	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.379e-05	1.000e-20
X11_P16	2.905e-05	1.000e-20
X17_P16	4.289e-05	1.000e-20
X23_P16	5.767e-05	1.000e-20
X46_P16	1.125e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	2.529e-05	5.644e-05	8.144e-05	1.499e-04
B (output stable)	3.473e-05	7.941e-05	1.132e-04	2.939e-04
C (output stable)	2.624e-04	6.411e-04	7.380e-04	1.223e-03
A to Z	2.435e-03	5.185e-03	7.337e-03	1.070e-02
B to Z	1.992e-03	4.281e-03	5.905e-03	8.244e-03
C to Z	1.669e-03	3.627e-03	5.086e-03	7.186e-03
	X46_P16			
A (output stable)	2.831e-04			
B (output stable)	5.342e-04			
C (output stable)	2.166e-03			
A to Z	2.071e-02			
B to Z	1.587e-02			
C to Z	1.386e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

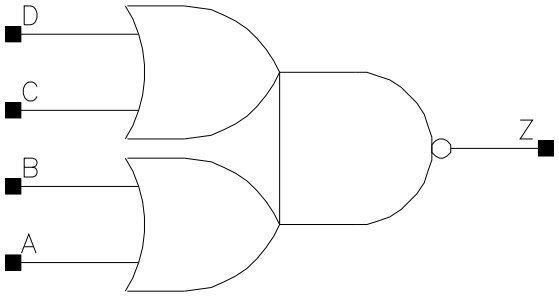
	X46_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0011	0.0022	0.0032	0.0044
B	0.0011	0.0020	0.0029	0.0040
C	0.0010	0.0021	0.0031	0.0043
D	0.0010	0.0019	0.0028	0.0039
	X42_P16			
A	0.0090			
B	0.0081			
C	0.0084			
D	0.0078			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0127	0.0138	3.0072	1.4944
A to Z ↑	0.0195	0.0196	5.1560	2.3718
B to Z ↓	0.0107	0.0113	2.9501	1.5010
B to Z ↑	0.0201	0.0191	5.1702	2.3819
C to Z ↓	0.0120	0.0132	3.0765	1.5172
C to Z ↑	0.0134	0.0143	5.0439	2.3830
D to Z ↓	0.0096	0.0101	3.0017	1.5283
D to Z ↑	0.0137	0.0130	5.0685	2.3978
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0132	0.0134	1.0202	0.7353
A to Z ↑	0.0185	0.0191	1.5958	1.1763
B to Z ↓	0.0110	0.0109	1.0253	0.7359
B to Z ↑	0.0184	0.0189	1.6039	1.1814
C to Z ↓	0.0129	0.0129	1.0381	0.7473
C to Z ↑	0.0134	0.0137	1.6043	1.1801
D to Z ↓	0.0101	0.0100	1.0486	0.7510
D to Z ↑	0.0127	0.0129	1.6158	1.1875
	X42_P16		**X42_P16**	
A to Z ↓	0.0137		0.3848	
A to Z ↑	0.0192		0.5994	
B to Z ↓	0.0111		0.3814	
B to Z ↑	0.0190		0.6020	
C to Z ↓	0.0136		0.3923	
C to Z ↑	0.0139		0.5972	
D to Z ↓	0.0105		0.3895	
D to Z ↑	0.0131		0.6014	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.679e-05	1.000e-20
X10_P16	3.560e-05	1.000e-20
X15_P16	5.164e-05	1.000e-20
X21_P16	7.101e-05	1.000e-20
X42_P16	1.398e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	3.484e-05	1.140e-04	1.471e-04	2.128e-04
B (output stable)	5.508e-05	2.832e-04	2.946e-04	4.637e-04
C (output stable)	9.240e-05	2.501e-04	3.143e-04	4.524e-04
D (output stable)	1.163e-04	4.202e-04	4.595e-04	6.955e-04
A to Z	2.901e-03	6.471e-03	9.066e-03	1.271e-02
B to Z	2.470e-03	5.202e-03	7.301e-03	1.027e-02
C to Z	2.097e-03	4.857e-03	6.762e-03	9.436e-03
D to Z	1.706e-03	3.628e-03	5.124e-03	7.146e-03
	X42_P16			
A (output stable)	4.206e-04			
B (output stable)	8.817e-04			
C (output stable)	8.835e-04			
D (output stable)	1.374e-03			

A to Z	2.519e-02			
B to Z	2.030e-02			
C to Z	1.879e-02			
D to Z	1.425e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

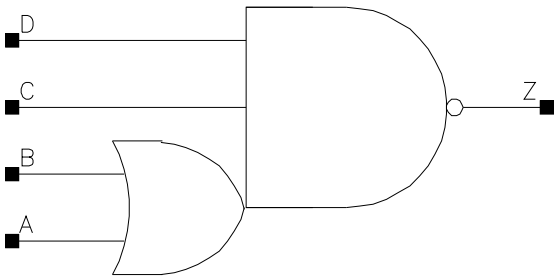
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X21_P16	1.200	2.448	2.9376
X31_P16	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X21_P16	X31_P16
A	0.0011	0.0020	0.0041	0.0061
B	0.0012	0.0019	0.0036	0.0055
C	0.0011	0.0022	0.0044	0.0066
D	0.0011	0.0021	0.0041	0.0062

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0169	0.0164	4.0783	2.1778
A to Z ↑	0.0168	0.0155	4.6682	2.3541
B to Z ↓	0.0142	0.0127	4.1421	2.1911
B to Z ↑	0.0170	0.0145	4.7062	2.3691
C to Z ↓	0.0143	0.0148	3.8504	2.0507

C to Z ↑	0.0166	0.0163	2.6688	1.3437
D to Z ↓	0.0154	0.0147	3.8718	2.0613
D to Z ↑	0.0155	0.0144	2.7003	1.3473
	X21_P16	**X31_P16**	**X21_P16**	**X31_P16**
A to Z ↓	0.0166	0.0169	1.1329	0.7686
A to Z ↑	0.0151	0.0151	1.1758	0.7898
B to Z ↓	0.0129	0.0131	1.1411	0.7767
B to Z ↑	0.0142	0.0142	1.1838	0.7953
C to Z ↓	0.0147	0.0147	1.0684	0.7256
C to Z ↑	0.0159	0.0159	0.6800	0.4583
D to Z ↓	0.0149	0.0150	1.0732	0.7290
D to Z ↑	0.0142	0.0143	0.6811	0.4581

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.282e-05	1.000e-20
X10_P16	2.469e-05	1.000e-20
X21_P16	4.763e-05	1.000e-20
X31_P16	7.059e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	1.985e-04	4.261e-04	7.934e-04	1.159e-03
B (output stable)	2.130e-04	4.608e-04	8.504e-04	1.251e-03
C (output stable)	3.880e-05	1.155e-04	2.208e-04	3.244e-04
D (output stable)	8.914e-05	3.387e-04	6.087e-04	8.875e-04
A to Z	2.741e-03	4.909e-03	9.549e-03	1.421e-02
B to Z	2.129e-03	3.658e-03	7.084e-03	1.060e-02
C to Z	3.403e-03	6.588e-03	1.269e-02	1.885e-02
D to Z	3.037e-03	5.546e-03	1.073e-02	1.598e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

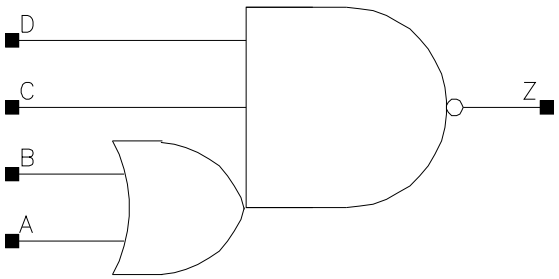
Pin Cycle (vdds)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0011	0.0023	0.0034	0.0045
B	0.0011	0.0021	0.0030	0.0041
C	0.0011	0.0021	0.0032	0.0042
D	0.0010	0.0020	0.0030	0.0040

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0151	0.0164	4.1519	2.1658
A to Z ↑	0.0192	0.0210	4.5368	2.3127
B to Z ↓	0.0126	0.0133	4.0884	2.1717
B to Z ↑	0.0200	0.0206	4.5541	2.3230
C to Z ↓	0.0121	0.0136	3.9291	2.0681

C to Z ↑	0.0126	0.0134	2.7118	1.3720
D to Z ↓	0.0127	0.0134	3.9577	2.0795
D to Z ↑	0.0106	0.0108	2.7364	1.3845
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0160	0.0162	1.4868	1.1223
A to Z ↑	0.0201	0.0206	1.5591	1.1817
B to Z ↓	0.0132	0.0131	1.4832	1.1224
B to Z ↑	0.0201	0.0205	1.5666	1.1868
C to Z ↓	0.0132	0.0135	1.4151	1.0689
C to Z ↑	0.0128	0.0130	0.9153	0.6877
D to Z ↓	0.0132	0.0137	1.4238	1.0748
D to Z ↑	0.0103	0.0106	0.9236	0.6940

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.299e-05	1.000e-20
X10_P16	2.563e-05	1.000e-20
X15_P16	3.678e-05	1.000e-20
X21_P16	4.984e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	2.305e-05	5.144e-05	7.673e-05	9.844e-05
B (output stable)	2.616e-05	9.086e-05	1.107e-04	1.582e-04
C (output stable)	8.271e-05	1.827e-04	2.854e-04	3.641e-04
D (output stable)	1.803e-04	6.121e-04	7.180e-04	1.084e-03
A to Z	3.240e-03	6.977e-03	9.949e-03	1.356e-02
B to Z	2.728e-03	5.615e-03	8.022e-03	1.092e-02
C to Z	2.295e-03	4.994e-03	7.028e-03	9.670e-03
D to Z	1.956e-03	4.098e-03	5.817e-03	7.952e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

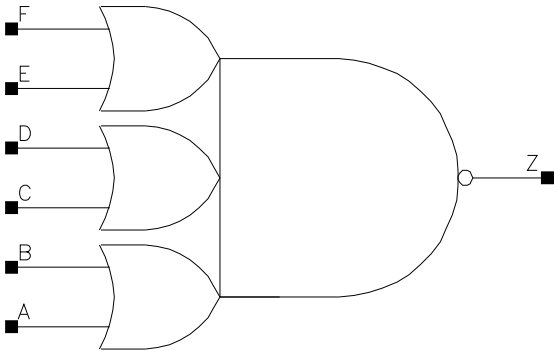
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	1.088	1.3056
X9_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X9_P16
A	0.0009	0.0023
B	0.0009	0.0021
C	0.0009	0.0022
D	0.0008	0.0020
E	0.0009	0.0021
F	0.0008	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X9_P16	X3_P16	X9_P16
A to Z ↓	0.0194	0.0210	4.7424	1.9666
A to Z ↑	0.0267	0.0258	6.3124	2.3278
B to Z ↓	0.0176	0.0181	4.7869	1.9728
B to Z ↑	0.0283	0.0257	6.3319	2.3346
C to Z ↓	0.0188	0.0200	4.7864	1.9789
C to Z ↑	0.0227	0.0218	6.3336	2.3248
D to Z ↓	0.0167	0.0170	4.8344	1.9878
D to Z ↑	0.0240	0.0215	6.3602	2.3338
E to Z ↓	0.0167	0.0182	4.8355	1.9888
E to Z ↑	0.0169	0.0163	6.3664	2.3325
F to Z ↓	0.0147	0.0149	4.8888	1.9970
F to Z ↑	0.0179	0.0154	6.4087	2.3464

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	1.507e-05	1.000e-20
X9_P16	4.290e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X9_P16
A (output stable)	3.055e-05	1.089e-04
B (output stable)	3.999e-05	2.183e-04
C (output stable)	6.860e-05	2.013e-04
D (output stable)	7.714e-05	3.131e-04
E (output stable)	2.236e-04	5.505e-04
F (output stable)	2.352e-04	6.527e-04
A to Z	3.651e-03	9.590e-03
B to Z	3.293e-03	8.220e-03
C to Z	2.961e-03	7.785e-03
D to Z	2.624e-03	6.551e-03
E to Z	2.210e-03	6.043e-03
F to Z	1.905e-03	4.812e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

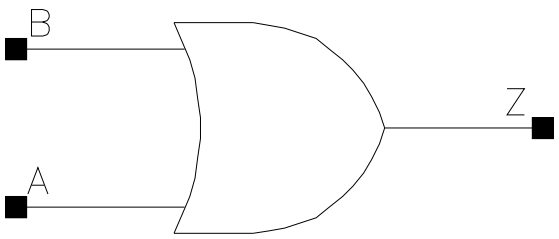
Pin Cycle (vdds)	X3_P16	X9_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X33_P16	1.200	1.360	1.6320
X50_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P16	X16_P16	X33_P16	X50_P16
A	0.0010	0.0012	0.0024	0.0025
B	0.0008	0.0012	0.0024	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0305	0.0276	1.8220	0.9187
A to Z ↑	0.0205	0.0222	2.6710	1.3444
B to Z ↓	0.0315	0.0286	1.8198	0.9182
B to Z ↑	0.0192	0.0205	2.6675	1.3450
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0286	0.0341	0.4544	0.3116
A to Z ↑	0.0223	0.0222	0.6567	0.4431
B to Z ↓	0.0285	0.0344	0.4544	0.3115
B to Z ↑	0.0201	0.0204	0.6554	0.4427

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	1.438e-05	1.000e-20
X16_P16	2.777e-05	1.000e-20
X33_P16	5.627e-05	1.000e-20
X50_P16	7.310e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	2.230e-05	4.055e-05	1.427e-04	1.329e-04
B (output stable)	4.437e-05	7.812e-05	4.172e-04	3.880e-04
A to Z	3.957e-03	6.779e-03	1.418e-02	1.999e-02
B to Z	3.723e-03	6.350e-03	1.290e-02	1.877e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

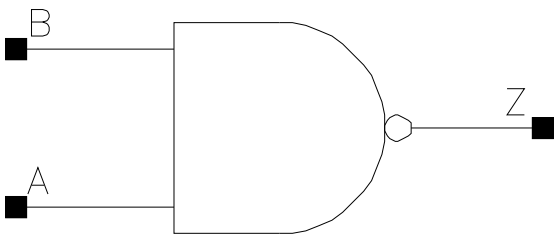
Pin Cycle (vdds)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X16_P16	1.200	0.952	1.1424
X24_P16	1.200	1.088	1.3056
X32_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P16	X16_P16	X24_P16	X32_P16
A	0.0013	0.0013	0.0013	0.0012
B	0.0014	0.0014	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0274	0.0292	1.7731	0.9214
A to Z ↑	0.0296	0.0310	2.6953	1.3745
B to Z ↓	0.0289	0.0309	1.7719	0.9208
B to Z ↑	0.0278	0.0287	2.6915	1.3745
	X24_P16	**X32_P16**	**X24_P16**	**X32_P16**
A to Z ↓	0.0327	0.0335	0.6219	0.4661
A to Z ↑	0.0335	0.0345	0.9175	0.6858
B to Z ↓	0.0344	0.0355	0.6219	0.4660
B to Z ↑	0.0311	0.0328	0.9179	0.6854

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	3.253e-05	1.000e-20
X16_P16	4.066e-05	1.000e-20
X24_P16	4.837e-05	1.000e-20
X32_P16	6.561e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	2.272e-05	2.281e-05	2.288e-05	2.511e-05
B (output stable)	5.073e-05	5.112e-05	5.123e-05	4.975e-05
A to Z	7.199e-03	8.758e-03	1.131e-02	1.495e-02
B to Z	6.863e-03	8.434e-03	1.100e-02	1.463e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

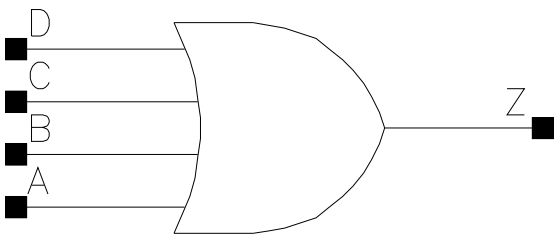
Pin Cycle (vdds)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P16	1.200	2.176	2.6112
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P16	X27_P16
A	0.0021	0.0025
B	0.0020	0.0025
C	0.0021	0.0026
D	0.0020	0.0026

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P16	X27_P16	X20_P16	X27_P16
A to Z ↓	0.0311	0.0329	1.0383	0.7761
A to Z ↑	0.0228	0.0222	0.8804	0.6570
B to Z ↓	0.0314	0.0327	1.0379	0.7763
B to Z ↑	0.0211	0.0202	0.8797	0.6555
C to Z ↓	0.0306	0.0325	1.0365	0.7746
C to Z ↑	0.0217	0.0216	0.8817	0.6585
D to Z ↓	0.0308	0.0326	1.0359	0.7743
D to Z ↑	0.0199	0.0198	0.8805	0.6576

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X20_P16	4.865e-05	1.000e-20
X27_P16	6.990e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X20_P16	X27_P16
A (output stable)	2.832e-03	3.921e-03
B (output stable)	2.533e-03	3.509e-03
C (output stable)	2.489e-03	3.578e-03
D (output stable)	2.181e-03	3.226e-03
A to Z	1.217e-02	1.701e-02
B to Z	1.128e-02	1.567e-02
C to Z	1.087e-02	1.514e-02
D to Z	9.978e-03	1.395e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

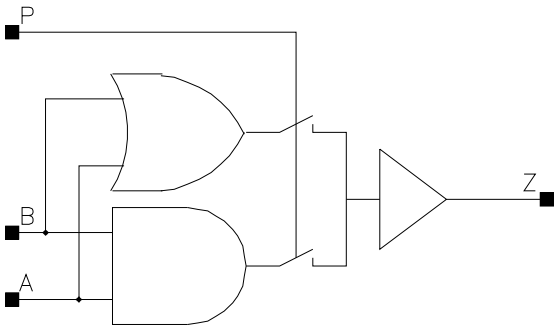
Pin Cycle (vdds)	X20_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X16_P16	1.200	1.224	1.4688
X25_P16	1.200	2.040	2.4480
X33_P16	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0015	0.0023	0.0041	0.0042
B	0.0015	0.0023	0.0046	0.0046
P	0.0008	0.0012	0.0024	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0372	0.0343	1.8527	0.9070
A to Z ↑	0.0267	0.0259	2.7139	1.3567
B to Z ↓	0.0377	0.0349	1.8615	0.9124
B to Z ↑	0.0280	0.0271	2.7146	1.3594
P to Z ↓	0.0353	0.0331	1.8583	0.9109
P to Z ↑	0.0274	0.0267	2.7107	1.3570
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**

A to Z ↓	0.0327	0.0356	0.6158	0.4661
A to Z ↑	0.0254	0.0274	0.9123	0.6838
B to Z ↓	0.0331	0.0357	0.6191	0.4682
B to Z ↑	0.0270	0.0287	0.9136	0.6845
P to Z ↓	0.0320	0.0348	0.6186	0.4674
P to Z ↑	0.0261	0.0280	0.9110	0.6824

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	1.857e-05	1.000e-20
X16_P16	3.922e-05	1.000e-20
X25_P16	6.640e-05	1.000e-20
X33_P16	7.643e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	4.699e-05	7.632e-05	1.688e-04	1.678e-04
B (output stable)	6.577e-05	1.177e-04	3.335e-04	3.332e-04
P (output stable)	2.199e-04	3.840e-04	5.891e-04	6.030e-04
A to Z	4.586e-03	8.147e-03	1.364e-02	1.665e-02
B to Z	4.477e-03	8.010e-03	1.315e-02	1.620e-02
P to Z	4.182e-03	7.573e-03	1.262e-02	1.562e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

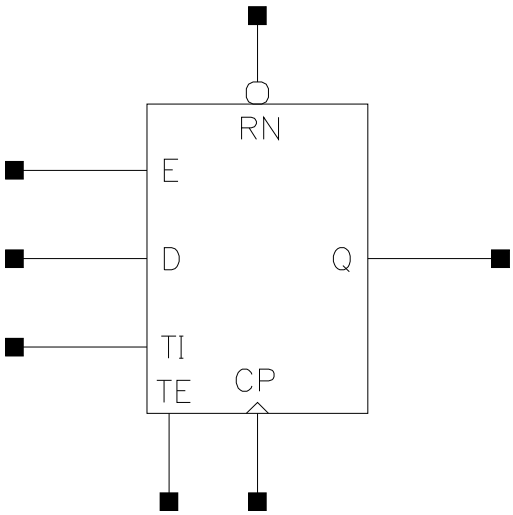
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.488	5.3856
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0011	0.0011	0.0011
D	0.0009	0.0008	0.0008	0.0008
E	0.0011	0.0013	0.0013	0.0013
RN	0.0010	0.0009	0.0009	0.0010
TE	0.0011	0.0011	0.0011	0.0011

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to Q ↓	0.0679	0.0388	3.8290	1.8058
CP to Q ↑	0.0592	0.0513	5.3087	2.6869
RN to Q ↓	0.0496	0.0578	3.4653	1.7609
	X17_P16	X33_P16	X17_P16	X33_P16
CP to Q ↓	0.0671	0.0718	0.8811	0.4604
CP to Q ↑	0.0825	0.0875	1.3148	0.6696
RN to Q ↓	0.0792	0.0847	0.8810	0.4606

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0874	0.0598	0.0598	0.0598
CP ↑	min_pulse_width to CP	0.0611	0.0318	0.0271	0.0270
D ↓	hold_rising to CP	-0.0891	-0.0440	-0.0440	-0.0440
D ↑	hold_rising to CP	-0.0576	-0.0190	-0.0190	-0.0190
D ↓	setup_rising to CP	0.1269	0.0777	0.0777	0.0836
D ↑	setup_rising to CP	0.0904	0.0467	0.0467	0.0467
E ↓	hold_rising to CP	-0.0621	-0.0679	-0.0675	-0.0675
E ↑	hold_rising to CP	-0.0555	-0.0197	-0.0197	-0.0197
E ↓	setup_rising to CP	0.1096	0.1068	0.1094	0.1094
E ↑	setup_rising to CP	0.1204	0.0830	0.0830	0.0830
RN ↓	min_pulse_width to RN	0.0637	0.0713	0.0588	0.0615
RN ↑	recovery_rising to CP	0.0151	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0104	-0.0056	-0.0056	-0.0056
TE ↓	hold_rising to CP	-0.0452	-0.0230	-0.0230	-0.0262
TE ↑	hold_rising to CP	-0.0360	-0.0240	-0.0234	-0.0234
TE ↓	setup_rising to CP	0.0798	0.0700	0.0700	0.0700
TE ↑	setup_rising to CP	0.1492	0.1079	0.1079	0.1079
TI ↓	hold_rising to CP	-0.1113	-0.0565	-0.0563	-0.0606
TI ↑	hold_rising to CP	-0.0462	-0.0238	-0.0238	-0.0238
TI ↓	setup_rising to CP	0.1517	0.0961	0.0961	0.0961
TI ↑	setup_rising to CP	0.0759	0.0537	0.0537	0.0537

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	5.519e-05	1.000e-20
X8_P16	6.281e-05	1.000e-20
X17_P16	8.019e-05	1.000e-20
X33_P16	1.057e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

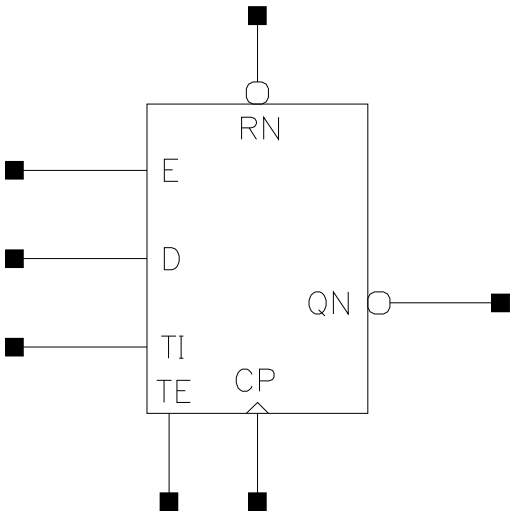
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.264e-02	1.273e-02	1.275e-02	1.277e-02
Clock 100Mhz Data 25Mhz	1.386e-02	1.395e-02	1.501e-02	1.657e-02
Clock 100Mhz Data 50Mhz	1.508e-02	1.517e-02	1.727e-02	2.038e-02
Clock = 0 Data 100Mhz	1.008e-02	9.542e-03	9.366e-03	9.279e-03
Clock = 1 Data 100Mhz	3.329e-03	3.441e-03	3.481e-03	3.501e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.624	5.5488
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0011	0.0011	0.0011
D	0.0009	0.0008	0.0008	0.0008
E	0.0011	0.0013	0.0013	0.0013
RN	0.0010	0.0010	0.0010	0.0010
TE	0.0011	0.0011	0.0011	0.0011

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to QN ↓	0.0725	0.0691	3.3018	1.7481
CP to QN ↑	0.0752	0.0511	5.1865	2.6099
RN to QN ↑	0.0607	0.0644	5.1761	2.6140
	X17_P16	X33_P16	X17_P16	X33_P16
CP to QN ↓	0.0672	0.0720	0.8817	0.4605
CP to QN ↑	0.0537	0.0593	1.3152	0.6708
RN to QN ↑	0.0715	0.0757	1.3132	0.6688

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0874	0.0598	0.0598	0.0598
CP ↑	min_pulse_width to CP	0.0458	0.0271	0.0317	0.0330
D ↓	hold_rising to CP	-0.0923	-0.0440	-0.0440	-0.0440
D ↑	hold_rising to CP	-0.0576	-0.0190	-0.0190	-0.0190
D ↓	setup_rising to CP	0.1259	0.0777	0.0836	0.0836
D ↑	setup_rising to CP	0.0904	0.0467	0.0467	0.0488
E ↓	hold_rising to CP	-0.0621	-0.0675	-0.0679	-0.0679
E ↑	hold_rising to CP	-0.0555	-0.0197	-0.0197	-0.0197
E ↓	setup_rising to CP	0.1117	0.1068	0.1094	0.1094
E ↑	setup_rising to CP	0.1200	0.0830	0.0830	0.0830
RN ↓	min_pulse_width to RN	0.0588	0.0593	0.0708	0.0757
RN ↑	recovery_rising to CP	0.0151	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0104	-0.0055	-0.0056	-0.0056
TE ↓	hold_rising to CP	-0.0409	-0.0230	-0.0230	-0.0230
TE ↑	hold_rising to CP	-0.0360	-0.0234	-0.0240	-0.0240
TE ↓	setup_rising to CP	0.0798	0.0700	0.0700	0.0700
TE ↑	setup_rising to CP	0.1492	0.1079	0.1074	0.1074
TI ↓	hold_rising to CP	-0.1113	-0.0563	-0.0563	-0.0565
TI ↑	hold_rising to CP	-0.0462	-0.0238	-0.0238	-0.0238
TI ↓	setup_rising to CP	0.1517	0.0961	0.0961	0.0961
TI ↑	setup_rising to CP	0.0759	0.0537	0.0537	0.0537

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	5.507e-05	1.000e-20
X8_P16	6.071e-05	1.000e-20
X17_P16	7.668e-05	1.000e-20
X33_P16	9.797e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

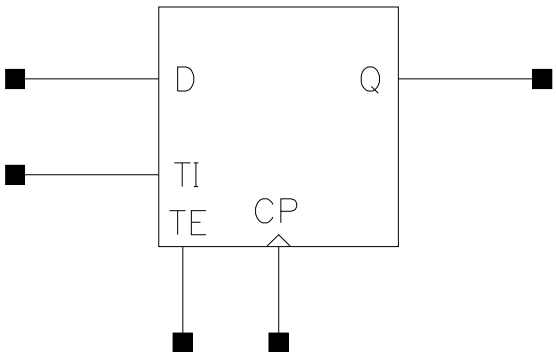
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.263e-02	1.273e-02	1.274e-02	1.275e-02
Clock 100Mhz Data 25Mhz	1.366e-02	1.398e-02	1.499e-02	1.656e-02
Clock 100Mhz Data 50Mhz	1.468e-02	1.524e-02	1.724e-02	2.036e-02
Clock = 0 Data 100Mhz	1.009e-02	9.553e-03	9.372e-03	9.283e-03
Clock = 1 Data 100Mhz	3.325e-03	3.444e-03	3.483e-03	3.504e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.400	4.0800
X8_P16	1.200	3.128	3.7536
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0011	0.0011	0.0011
D	0.0011	0.0009	0.0009	0.0009
TE	0.0010	0.0013	0.0013	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0562	0.0362	3.6258	1.8061
CP to Q ↑	0.0533	0.0470	5.3274	2.6518
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0559	0.0622	0.8673	0.4538
CP to Q ↑	0.0807	0.0862	1.3133	0.6691

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0786	0.0842	0.0842	0.0842
CP ↑	min_pulse_width to CP	0.0458	0.0270	0.0271	0.0271
D ↓	hold_rising to CP	-0.0555	-0.0196	-0.0196	-0.0196
D ↑	hold_rising to CP	-0.0208	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0879	0.0559	0.0559	0.0559
D ↑	setup_rising to CP	0.0514	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0386	-0.0147	-0.0147	-0.0147
TE ↑	hold_rising to CP	-0.0283	-0.0137	-0.0169	-0.0169
TE ↓	setup_rising to CP	0.0733	0.0540	0.0540	0.0540
TE ↑	setup_rising to CP	0.1346	0.1128	0.1128	0.1128
TI ↓	hold_rising to CP	-0.1080	-0.0668	-0.0668	-0.0668
TI ↑	hold_rising to CP	-0.0321	-0.0146	-0.0162	-0.0162
TI ↓	setup_rising to CP	0.1420	0.1078	0.1078	0.1078
TI ↑	setup_rising to CP	0.0610	0.0453	0.0453	0.0453

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	4.442e-05	1.000e-20
X8_P16	5.200e-05	1.000e-20
X17_P16	7.414e-05	1.000e-20
X33_P16	9.377e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

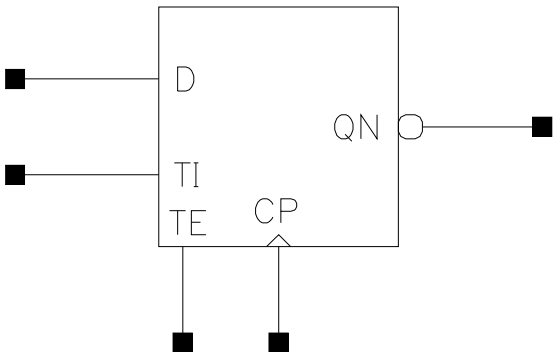
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.156e-02	1.171e-02	1.176e-02	1.178e-02
Clock 100Mhz Data 25Mhz	1.178e-02	1.192e-02	1.305e-02	1.440e-02
Clock 100Mhz Data 50Mhz	1.201e-02	1.213e-02	1.434e-02	1.702e-02
Clock = 0 Data 100Mhz	7.939e-03	7.370e-03	7.181e-03	7.086e-03
Clock = 1 Data 100Mhz	1.880e-03	9.634e-04	6.580e-04	5.053e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.536	4.2432
X8_P16	1.200	3.264	3.9168
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0011	0.0011	0.0011
D	0.0011	0.0009	0.0009	0.0009
TE	0.0010	0.0013	0.0013	0.0013
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0677	0.0728	3.7538	1.7959
CP to QN ↑	0.0603	0.0473	5.2806	2.6151
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0581	0.0651	0.8679	0.4544
CP to QN ↑	0.0476	0.0533	1.3126	0.6687

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0786	0.0842	0.0842	0.0842
CP ↑	min_pulse_width to CP	0.0330	0.0271	0.0270	0.0283
D ↓	hold_rising to CP	-0.0555	-0.0196	-0.0196	-0.0196
D ↑	hold_rising to CP	-0.0208	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0879	0.0559	0.0559	0.0559
D ↑	setup_rising to CP	0.0514	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0386	-0.0147	-0.0147	-0.0147
TE ↑	hold_rising to CP	-0.0283	-0.0169	-0.0137	-0.0137
TE ↓	setup_rising to CP	0.0707	0.0540	0.0540	0.0540
TE ↑	setup_rising to CP	0.1350	0.1128	0.1128	0.1128
TI ↓	hold_rising to CP	-0.1064	-0.0668	-0.0668	-0.0668
TI ↑	hold_rising to CP	-0.0321	-0.0146	-0.0146	-0.0146
TI ↓	setup_rising to CP	0.1420	0.1078	0.1078	0.1078
TI ↑	setup_rising to CP	0.0602	0.0453	0.0453	0.0453

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	4.476e-05	1.000e-20
X8_P16	5.219e-05	1.000e-20
X17_P16	7.384e-05	1.000e-20
X33_P16	9.348e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

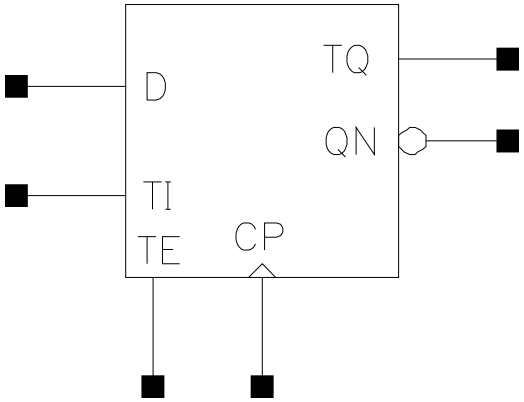
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.146e-02	1.166e-02	1.172e-02	1.176e-02
Clock 100Mhz Data 25Mhz	1.165e-02	1.205e-02	1.296e-02	1.436e-02
Clock 100Mhz Data 50Mhz	1.185e-02	1.245e-02	1.420e-02	1.696e-02
Clock = 0 Data 100Mhz	7.980e-03	7.389e-03	7.192e-03	7.094e-03
Clock = 1 Data 100Mhz	1.869e-03	9.580e-04	6.544e-04	5.026e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.536	4.2432
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0015	0.0012	0.0012	0.0012
D	0.0011	0.0009	0.0009	0.0009
TE	0.0010	0.0013	0.0012	0.0012

TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0756	0.0672	3.4231	1.7603
CP to QN ↑	0.0736	0.0495	5.1903	2.6251
CP to TQ ↓	0.0506	0.0326	4.6047	3.2527
CP to TQ ↑	0.0545	0.0466	9.4226	6.9021
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0643	0.0705	0.8856	0.4643
CP to QN ↑	0.0517	0.0562	1.3283	0.6816
CP to TQ ↓	0.0337	0.0350	4.2628	4.2763
CP to TQ ↑	0.0472	0.0487	8.7042	9.1457

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0786	0.0842	0.0842	0.0842
CP ↑	min_pulse_width to CP	0.0424	0.0270	0.0270	0.0317
D ↓	hold_rising to CP	-0.0523	-0.0196	-0.0196	-0.0196
D ↑	hold_rising to CP	-0.0208	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0852	0.0564	0.0564	0.0564
D ↑	setup_rising to CP	0.0514	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0386	-0.0147	-0.0147	-0.0147
TE ↑	hold_rising to CP	-0.0283	-0.0137	-0.0137	-0.0137
TE ↓	setup_rising to CP	0.0675	0.0540	0.0538	0.0538
TE ↑	setup_rising to CP	0.1350	0.1128	0.1128	0.1128
TI ↓	hold_rising to CP	-0.1064	-0.0670	-0.0670	-0.0670
TI ↑	hold_rising to CP	-0.0321	-0.0146	-0.0146	-0.0146
TI ↓	setup_rising to CP	0.1420	0.1078	0.1078	0.1078
TI ↑	setup_rising to CP	0.0609	0.0450	0.0450	0.0450

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	4.749e-05	1.000e-20
X8_P16	5.775e-05	1.000e-20
X17_P16	7.016e-05	1.000e-20
X33_P16	9.299e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16

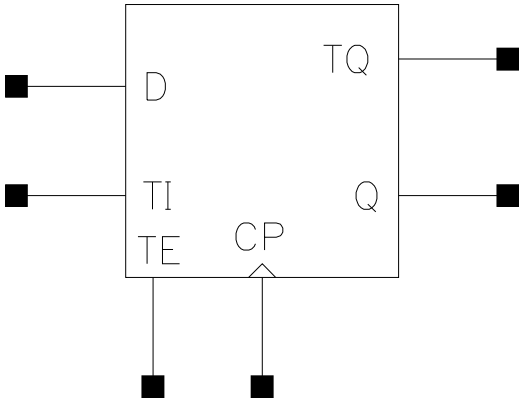
Clock 100Mhz Data 0Mhz	1.170e-02	1.179e-02	1.181e-02	1.183e-02
Clock 100Mhz Data 25Mhz	1.218e-02	1.249e-02	1.307e-02	1.468e-02
Clock 100Mhz Data 50Mhz	1.266e-02	1.319e-02	1.433e-02	1.752e-02
Clock = 0 Data 100Mhz	7.970e-03	7.394e-03	7.205e-03	7.112e-03
Clock = 1 Data 100Mhz	1.881e-03	9.640e-04	6.584e-04	5.056e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.400	4.0800
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0011	0.0011	0.0011
D	0.0011	0.0009	0.0009	0.0009

TE	0.0010	0.0012	0.0013	0.0013
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0745	0.0405	3.8073	1.7981
CP to Q ↑	0.0616	0.0501	5.3882	2.6724
CP to TQ ↓	0.0700	0.0404	3.8125	4.3645
CP to TQ ↑	0.0630	0.0544	6.9324	9.2725
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0575	0.0638	0.8909	0.4620
CP to Q ↑	0.0823	0.0876	1.3399	0.6723
CP to TQ ↓	0.0590	0.0656	4.2138	4.2920
CP to TQ ↑	0.0868	0.0941	9.0130	9.1037

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0786	0.0842	0.0842	0.0842
CP ↑	min_pulse_width to CP	0.0646	0.0317	0.0271	0.0271
D ↓	hold_rising to CP	-0.0555	-0.0196	-0.0196	-0.0196
D ↑	hold_rising to CP	-0.0208	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0879	0.0564	0.0559	0.0559
D ↑	setup_rising to CP	0.0514	0.0239	0.0239	0.0239
TE ↓	hold_rising to CP	-0.0386	-0.0147	-0.0147	-0.0147
TE ↑	hold_rising to CP	-0.0283	-0.0137	-0.0169	-0.0169
TE ↓	setup_rising to CP	0.0707	0.0540	0.0540	0.0540
TE ↑	setup_rising to CP	0.1346	0.1128	0.1128	0.1128
TI ↓	hold_rising to CP	-0.1064	-0.0670	-0.0668	-0.0668
TI ↑	hold_rising to CP	-0.0321	-0.0146	-0.0162	-0.0162
TI ↓	setup_rising to CP	0.1420	0.1078	0.1078	0.1078
TI ↑	setup_rising to CP	0.0610	0.0453	0.0453	0.0453

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	4.847e-05	1.000e-20
X8_P16	5.475e-05	1.000e-20
X17_P16	7.648e-05	1.000e-20
X33_P16	9.602e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

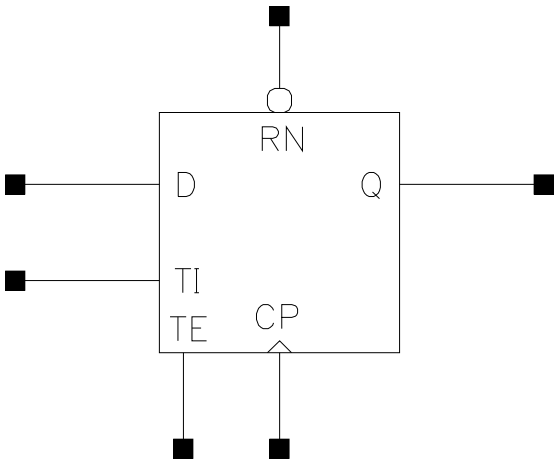
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.152e-02	1.169e-02	1.174e-02	1.177e-02
Clock 100Mhz Data 25Mhz	1.251e-02	1.231e-02	1.334e-02	1.480e-02
Clock 100Mhz Data 50Mhz	1.350e-02	1.292e-02	1.494e-02	1.783e-02
Clock = 0 Data 100Mhz	7.923e-03	7.358e-03	7.173e-03	7.081e-03
Clock = 1 Data 100Mhz	1.866e-03	9.565e-04	6.534e-04	5.019e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.672	4.4064
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0011	0.0011	0.0011
D	0.0011	0.0009	0.0009	0.0009
RN	0.0010	0.0009	0.0009	0.0009
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0673	0.0388	3.8736	1.8100
CP to Q ↑	0.0587	0.0504	5.3312	2.6827
RN to Q ↓	0.0493	0.0579	3.4783	1.7660
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0583	0.0650	0.8749	0.4597
CP to Q ↑	0.0743	0.0793	1.3098	0.6683
RN to Q ↓	0.0709	0.0775	0.8753	0.4595

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0874	0.0842	0.0858	0.0858
CP ↑	min_pulse_width to CP	0.0565	0.0318	0.0271	0.0271
D ↓	hold_rising to CP	-0.0474	-0.0094	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0257	-0.0049	-0.0040	-0.0040
D ↓	setup_rising to CP	0.0852	0.0542	0.0542	0.0542
D ↑	setup_rising to CP	0.0563	0.0347	0.0347	0.0347
RN ↓	min_pulse_width to RN	0.0588	0.0686	0.0593	0.0593
RN ↑	recovery_rising to CP	0.0146	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0099	-0.0056	-0.0056	-0.0056
TE ↓	hold_rising to CP	-0.0337	-0.0072	-0.0072	-0.0098
TE ↑	hold_rising to CP	-0.0360	-0.0244	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.0733	0.0527	0.0527	0.0527
TE ↑	setup_rising to CP	0.1318	0.1057	0.1057	0.1057
TI ↓	hold_rising to CP	-0.1025	-0.0521	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0410	-0.0251	-0.0251	-0.0251
TI ↓	setup_rising to CP	0.1369	0.1016	0.1016	0.1016
TI ↑	setup_rising to CP	0.0710	0.0551	0.0551	0.0551

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	5.059e-05	1.000e-20
X8_P16	5.685e-05	1.000e-20
X17_P16	7.791e-05	1.000e-20
X33_P16	1.001e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.264e-02	1.276e-02	1.285e-02	1.290e-02

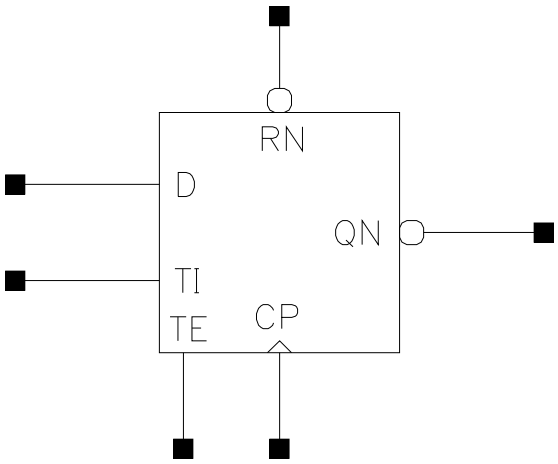
Clock 100Mhz Data 25Mhz	1.305e-02	1.295e-02	1.413e-02	1.555e-02
Clock 100Mhz Data 50Mhz	1.346e-02	1.313e-02	1.540e-02	1.819e-02
Clock = 0 Data 100Mhz	7.921e-03	7.234e-03	7.007e-03	6.893e-03
Clock = 1 Data 100Mhz	1.911e-03	9.802e-04	6.702e-04	5.153e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	3.944	4.7328
X33_P16	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0011	0.0011	0.0011
D	0.0011	0.0009	0.0009	0.0009
RN	0.0010	0.0010	0.0010	0.0010
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0657	0.0623	3.2570	1.7132
CP to QN ↑	0.0688	0.0462	5.1801	2.5960
RN to QN ↑	0.0551	0.0594	5.1678	2.6012
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0626	0.0697	0.8755	0.4589
CP to QN ↑	0.0518	0.0580	1.3207	0.6758
RN to QN ↑	0.0701	0.0756	1.3202	0.6755

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0858	0.0842	0.0842	0.0842
CP ↑	min_pulse_width to CP	0.0424	0.0271	0.0317	0.0317
D ↓	hold_rising to CP	-0.0474	-0.0094	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0257	-0.0049	-0.0049	-0.0049
D ↓	setup_rising to CP	0.0852	0.0542	0.0542	0.0542
D ↑	setup_rising to CP	0.0563	0.0347	0.0347	0.0347
RN ↓	min_pulse_width to RN	0.0588	0.0593	0.0708	0.0735
RN ↑	recovery_rising to CP	0.0151	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0099	-0.0078	-0.0055	-0.0055
TE ↓	hold_rising to CP	-0.0332	-0.0072	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0360	-0.0244	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.0733	0.0527	0.0528	0.0527
TE ↑	setup_rising to CP	0.1318	0.1057	0.1057	0.1057
TI ↓	hold_rising to CP	-0.1025	-0.0521	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0410	-0.0251	-0.0251	-0.0251
TI ↓	setup_rising to CP	0.1369	0.1016	0.1016	0.1016
TI ↑	setup_rising to CP	0.0710	0.0551	0.0551	0.0551

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	5.091e-05	1.000e-20
X8_P16	5.475e-05	1.000e-20
X17_P16	7.530e-05	1.000e-20
X33_P16	9.205e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.255e-02	1.271e-02	1.276e-02	1.279e-02

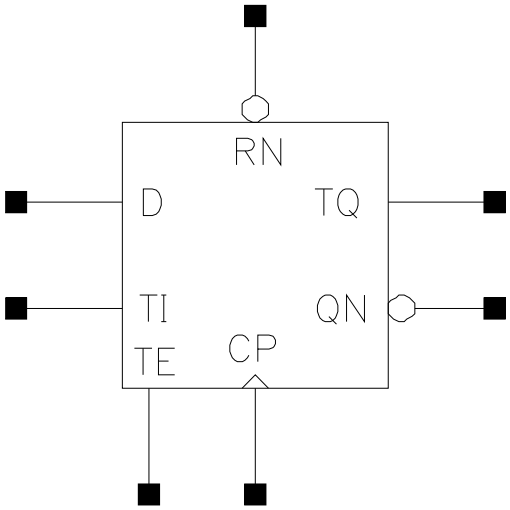
Clock 100Mhz Data 25Mhz	1.271e-02	1.287e-02	1.400e-02	1.541e-02
Clock 100Mhz Data 50Mhz	1.286e-02	1.303e-02	1.523e-02	1.803e-02
Clock = 0 Data 100Mhz	7.911e-03	7.226e-03	7.005e-03	6.895e-03
Clock = 1 Data 100Mhz	1.908e-03	9.788e-04	6.693e-04	5.146e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0011	0.0011	0.0011
D	0.0011	0.0009	0.0009	0.0009

RN	0.0012	0.0009	0.0010	0.0010
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0736	0.0650	3.2591	1.8023
CP to QN ↑	0.0894	0.0518	4.6582	2.6935
CP to TQ ↓	0.0625	0.0346	4.0990	3.4023
CP to TQ ↑	0.0602	0.0503	7.7065	7.1925
RN to QN ↑	0.0642	0.0678	4.7249	2.6843
RN to TQ ↓	0.0475	0.0556	3.6500	3.3301
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0680	0.0742	0.8932	0.4694
CP to QN ↑	0.0533	0.0568	1.3441	0.6773
CP to TQ ↓	0.0360	0.0373	4.1738	4.0816
CP to TQ ↑	0.0503	0.0516	6.7880	6.8757
RN to QN ↑	0.0717	0.0743	1.3450	0.6780
RN to TQ ↓	0.0566	0.0572	4.0973	3.9961

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0857	0.0842	0.0858	0.0858
CP ↑	min_pulse_width to CP	0.0599	0.0277	0.0283	0.0318
D ↓	hold_rising to CP	-0.0474	-0.0094	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0257	-0.0049	-0.0049	-0.0049
D ↓	setup_rising to CP	0.0852	0.0542	0.0542	0.0542
D ↑	setup_rising to CP	0.0563	0.0347	0.0347	0.0347
RN ↓	min_pulse_width to RN	0.0637	0.0637	0.0686	0.0735
RN ↑	recovery_rising to CP	0.0200	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0119	-0.0050	-0.0055	-0.0055
TE ↓	hold_rising to CP	-0.0337	-0.0072	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0360	-0.0244	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.0733	0.0527	0.0527	0.0527
TE ↑	setup_rising to CP	0.1318	0.1057	0.1057	0.1057
TI ↓	hold_rising to CP	-0.1025	-0.0521	-0.0521	-0.0524
TI ↑	hold_rising to CP	-0.0410	-0.0251	-0.0251	-0.0251
TI ↓	setup_rising to CP	0.1369	0.1016	0.1016	0.1016
TI ↑	setup_rising to CP	0.0710	0.0551	0.0551	0.0551

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	5.613e-05	1.000e-20
X8_P16	5.805e-05	1.000e-20
X17_P16	7.003e-05	1.000e-20
X33_P16	9.038e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

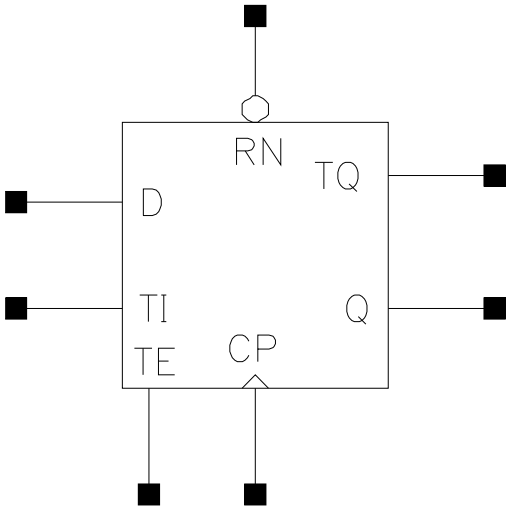
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.255e-02	1.270e-02	1.281e-02	1.286e-02
Clock 100Mhz Data 25Mhz	1.320e-02	1.314e-02	1.389e-02	1.551e-02
Clock 100Mhz Data 50Mhz	1.385e-02	1.358e-02	1.497e-02	1.816e-02
Clock = 0 Data 100Mhz	7.907e-03	7.226e-03	6.996e-03	6.881e-03
Clock = 1 Data 100Mhz	1.908e-03	9.792e-04	6.695e-04	5.146e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0011	0.0011	0.0011
D	0.0011	0.0009	0.0009	0.0009

RN	0.0011	0.0010	0.0009	0.0009
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0767	0.0422	4.0614	1.8557
CP to Q ↑	0.0631	0.0529	5.5144	2.7776
CP to TQ ↓	0.0709	0.0410	5.0353	4.4036
CP to TQ ↑	0.0654	0.0555	10.0876	9.2404
RN to Q ↓	0.0539	0.0605	3.6178	1.8045
RN to TQ ↓	0.0505	0.0597	4.5400	4.3028
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0603	0.0672	0.8860	0.4651
CP to Q ↑	0.0750	0.0803	1.3165	0.6708
CP to TQ ↓	0.0619	0.0696	4.2316	4.3156
CP to TQ ↑	0.0793	0.0872	9.1130	9.1533
RN to Q ↓	0.0725	0.0795	0.8854	0.4652
RN to TQ ↓	0.0740	0.0819	4.2336	4.3127

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0857	0.0842	0.0842	0.0842
CP ↑	min_pulse_width to CP	0.0693	0.0317	0.0271	0.0271
D ↓	hold_rising to CP	-0.0474	-0.0094	-0.0094	-0.0094
D ↑	hold_rising to CP	-0.0257	-0.0049	-0.0049	-0.0049
D ↓	setup_rising to CP	0.0852	0.0542	0.0542	0.0542
D ↑	setup_rising to CP	0.0563	0.0347	0.0347	0.0347
RN ↓	min_pulse_width to RN	0.0664	0.0735	0.0566	0.0566
RN ↑	recovery_rising to CP	0.0151	0.0151	0.0151	0.0151
RN ↑	removal_rising to CP	-0.0104	-0.0046	-0.0055	-0.0055
TE ↓	hold_rising to CP	-0.0337	-0.0040	-0.0072	-0.0072
TE ↑	hold_rising to CP	-0.0360	-0.0244	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.0733	0.0527	0.0527	0.0527
TE ↑	setup_rising to CP	0.1318	0.1057	0.1057	0.1057
TI ↓	hold_rising to CP	-0.1025	-0.0524	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0410	-0.0251	-0.0251	-0.0251
TI ↓	setup_rising to CP	0.1369	0.1016	0.1016	0.1016
TI ↑	setup_rising to CP	0.0710	0.0551	0.0551	0.0551

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	5.300e-05	1.000e-20
X8_P16	5.926e-05	1.000e-20
X17_P16	7.968e-05	1.000e-20
X33_P16	1.019e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

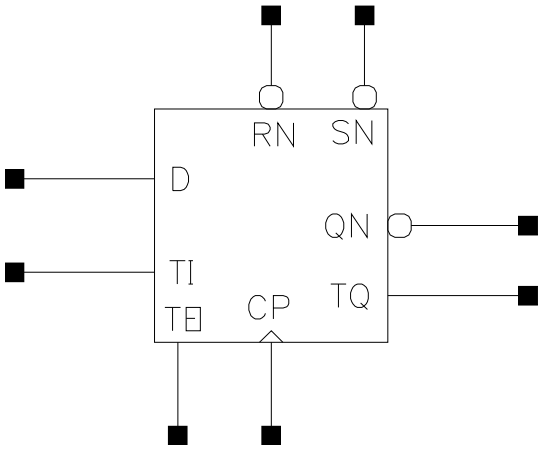
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.262e-02	1.275e-02	1.279e-02	1.281e-02
Clock 100Mhz Data 25Mhz	1.346e-02	1.324e-02	1.434e-02	1.582e-02
Clock 100Mhz Data 50Mhz	1.430e-02	1.374e-02	1.588e-02	1.884e-02
Clock = 0 Data 100Mhz	7.917e-03	7.232e-03	7.005e-03	6.891e-03
Clock = 1 Data 100Mhz	1.911e-03	9.804e-04	6.704e-04	5.155e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.352	5.2224
X17_P16	1.200	4.488	5.3856
X33_P16	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0012	0.0012
D	0.0007	0.0007	0.0007
RN	0.0011	0.0011	0.0011

SN	0.0015	0.0015	0.0015
TE	0.0013	0.0013	0.0013
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
CP to QN ↓	0.0716	0.0772	1.7437	0.8964
CP to QN ↑	0.0523	0.0556	2.6104	1.3210
CP to TQ ↓	0.0392	0.0391	5.2481	5.2554
CP to TQ ↑	0.0581	0.0580	11.7103	11.7194
RN to QN ↓	0.0645	0.0710	1.7512	0.8986
RN to QN ↑	0.0605	0.0634	2.6090	1.3203
RN to TQ ↓	0.0486	0.0486	5.1809	5.1782
RN to TQ ↑	0.0496	0.0494	11.8407	11.8460
SN to QN ↓	0.0693	0.0748	1.7442	0.8982
SN to TQ ↑	0.0562	0.0562	11.6972	11.7006
	X33_P16		X33_P16	
CP to QN ↓	0.0900		0.4751	
CP to QN ↑	0.0632		0.6756	
CP to TQ ↓	0.0392		5.2600	
CP to TQ ↑	0.0582		11.7399	
RN to QN ↓	0.0852		0.4744	
RN to QN ↑	0.0704		0.6758	
RN to TQ ↓	0.0487		5.1928	
RN to TQ ↑	0.0495		11.8904	
SN to QN ↓	0.0875		0.4755	
SN to TQ ↑	0.0564		11.7289	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0906	0.0913	0.0913
CP ↑	min_pulse_width to CP	0.0317	0.0317	0.0330
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120
D ↑	hold_rising to CP	-0.0049	-0.0049	-0.0049
D ↓	setup_rising to CP	0.0591	0.0591	0.0591
D ↑	setup_rising to CP	0.0347	0.0347	0.0347
RN ↓	min_pulse_width to RN	0.0686	0.0735	0.0784
RN ↑	non_seq_hold_rising to SN	-0.0265	-0.0265	-0.0265
RN ↑	non_seq_setup_rising to SN	0.0622	0.0622	0.0622
RN ↑	recovery_rising to CP	0.0248	0.0248	0.0248
RN ↑	removal_rising to CP	-0.0152	-0.0152	-0.0152
SN ↓	min_pulse_width to SN	0.0598	0.0598	0.0652
SN ↑	recovery_rising to CP	0.0022	0.0022	0.0022
SN ↑	removal_rising to CP	0.0285	0.0285	0.0285

TE ↓	hold_rising to CP	-0.0098	-0.0098	-0.0098
TE ↑	hold_rising to CP	-0.0244	-0.0244	-0.0244
TE ↓	setup_rising to CP	0.0586	0.0586	0.0586
TE ↑	setup_rising to CP	0.1102	0.1102	0.1102
TI ↓	hold_rising to CP	-0.0537	-0.0537	-0.0537
TI ↑	hold_rising to CP	-0.0251	-0.0251	-0.0251
TI ↓	setup_rising to CP	0.1065	0.1065	0.1065
TI ↑	setup_rising to CP	0.0551	0.0551	0.0551

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	6.523e-05	1.000e-20
X17_P16	7.495e-05	1.000e-20
X33_P16	9.295e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

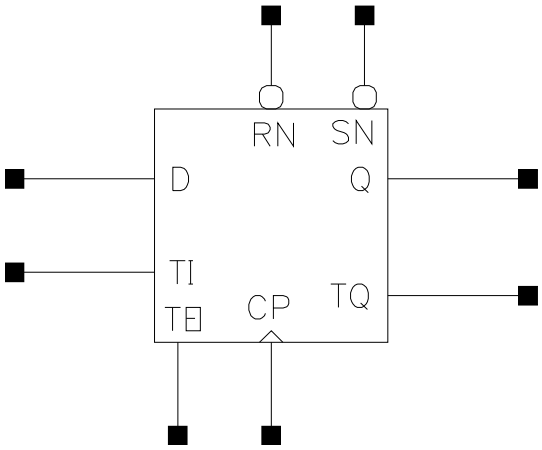
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.346e-02	1.346e-02	1.346e-02
Clock 100Mhz Data 25Mhz	1.370e-02	1.439e-02	1.633e-02
Clock 100Mhz Data 50Mhz	1.395e-02	1.533e-02	1.921e-02
Clock = 0 Data 100Mhz	6.726e-03	6.724e-03	6.725e-03
Clock = 1 Data 100Mhz	5.051e-05	5.059e-05	5.067e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.216	5.0592
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0012	0.0012
D	0.0007	0.0007	0.0007
RN	0.0011	0.0011	0.0011

SN	0.0015	0.0015	0.0015
TE	0.0013	0.0013	0.0013
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0453	0.0516	1.8058	0.9357
CP to Q ↑	0.0577	0.0621	2.6849	1.3645
CP to TQ ↓	0.0448	0.0507	5.3380	5.4231
CP to TQ ↑	0.0630	0.0703	11.3715	11.4570
RN to Q ↓	0.0523	0.0561	1.7535	0.9048
RN to Q ↑	0.0601	0.0630	2.6645	1.3522
RN to TQ ↓	0.0521	0.0558	5.2389	5.2896
RN to TQ ↑	0.0647	0.0700	11.3197	11.3914
SN to Q ↑	0.0554	0.0587	2.6708	1.3547
SN to TQ ↑	0.0599	0.0655	11.3372	11.4091
	X33_P16		**X33_P16**	
CP to Q ↓	0.0668		0.5012	
CP to Q ↑	0.0728		0.7075	
CP to TQ ↓	0.0616		5.6413	
CP to TQ ↑	0.0840		11.6041	
RN to Q ↓	0.0659		0.4796	
RN to Q ↑	0.0709		0.6984	
RN to TQ ↓	0.0625		5.4377	
RN to TQ ↑	0.0797		11.5190	
SN to Q ↑	0.0670		0.6983	
SN to TQ ↑	0.0757		11.5396	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0913	0.0913	0.0913
CP ↑	min_pulse_width to CP	0.0365	0.0412	0.0552
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0094
D ↑	hold_rising to CP	-0.0049	-0.0049	-0.0049
D ↓	setup_rising to CP	0.0591	0.0591	0.0591
D ↑	setup_rising to CP	0.0347	0.0347	0.0347
RN ↓	min_pulse_width to RN	0.0833	0.0979	0.1245
RN ↑	non_seq_hold_rising to SN	-0.0286	-0.0383	-0.0480
RN ↑	non_seq_setup_rising to SN	0.0572	0.0623	0.0846
RN ↑	recovery_rising to CP	0.0200	0.0200	0.0200
RN ↑	removal_rising to CP	-0.0103	-0.0103	-0.0103
SN ↓	min_pulse_width to SN	0.0647	0.0771	0.1016
SN ↑	recovery_rising to CP	0.0048	0.0081	0.0081
SN ↑	removal_rising to CP	0.0285	0.0285	0.0285

TE ↓	hold_rising to CP	-0.0098	-0.0098	-0.0072
TE ↑	hold_rising to CP	-0.0244	-0.0244	-0.0218
TE ↓	setup_rising to CP	0.0586	0.0586	0.0586
TE ↑	setup_rising to CP	0.1102	0.1102	0.1102
TI ↓	hold_rising to CP	-0.0521	-0.0521	-0.0521
TI ↑	hold_rising to CP	-0.0253	-0.0253	-0.0253
TI ↓	setup_rising to CP	0.1065	0.1065	0.1065
TI ↑	setup_rising to CP	0.0551	0.0551	0.0551

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P16	6.601e-05	1.000e-20
X17_P16	7.716e-05	1.000e-20
X33_P16	9.847e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

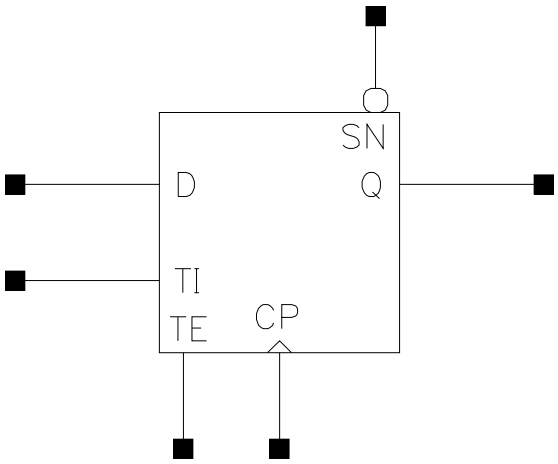
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.344e-02	1.344e-02	1.344e-02
Clock 100Mhz Data 25Mhz	1.371e-02	1.471e-02	1.748e-02
Clock 100Mhz Data 50Mhz	1.398e-02	1.598e-02	2.153e-02
Clock = 0 Data 100Mhz	6.725e-03	6.725e-03	6.725e-03
Clock = 1 Data 100Mhz	5.046e-05	5.051e-05	5.058e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0012	0.0012	0.0012	0.0012
D	0.0010	0.0005	0.0005	0.0005
SN	0.0017	0.0017	0.0017	0.0017
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005
	X33_P16			

CP	0.0012			
D	0.0005			
SN	0.0017			
TE	0.0012			
TI	0.0005			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0672	0.0398	3.8800	1.7948
CP to Q ↑	0.0610	0.0528	5.3621	2.6701
SN to Q ↑	0.0399	0.0426	5.2152	2.6431
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to Q ↓	0.0573	0.0610	0.8755	0.6058
CP to Q ↑	0.0747	0.0776	1.3104	0.8886
SN to Q ↑	0.0652	0.0681	1.3091	0.8888
	X33_P16		**X33_P16**	
CP to Q ↓	0.0638		0.4600	
CP to Q ↑	0.0796		0.6688	
SN to Q ↑	0.0702		0.6690	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.0904	0.0929	0.0929	0.0929
CP ↑	min_pulse_width to CP	0.0565	0.0283	0.0271	0.0271
D ↓	hold_rising to CP	-0.0533	-0.0143	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0266	-0.0023	-0.0023	-0.0023
D ↓	setup_rising to CP	0.0873	0.0587	0.0587	0.0587
D ↑	setup_rising to CP	0.0563	0.0298	0.0298	0.0298
SN ↓	min_pulse_width to SN	0.0403	0.0500	0.0452	0.0452
SN ↑	recovery_rising to CP	0.0081	0.0048	0.0022	0.0022
SN ↑	removal_rising to CP	0.0211	0.0287	0.0287	0.0287
TE ↓	hold_rising to CP	-0.0360	-0.0098	-0.0088	-0.0088
TE ↑	hold_rising to CP	-0.0332	-0.0196	-0.0196	-0.0196
TE ↓	setup_rising to CP	0.0733	0.0591	0.0591	0.0591
TE ↑	setup_rising to CP	0.1346	0.1123	0.1123	0.1123
TI ↓	hold_rising to CP	-0.1015	-0.0586	-0.0579	-0.0579
TI ↑	hold_rising to CP	-0.0370	-0.0202	-0.0202	-0.0202
TI ↓	setup_rising to CP	0.1420	0.1114	0.1114	0.1114
TI ↑	setup_rising to CP	0.0667	0.0502	0.0502	0.0502
		X33_P16			

CP ↓	min_pulse_width to CP	0.0929			
CP ↑	min_pulse_width to CP	0.0271			
D ↓	hold_rising to CP	-0.0143			
D ↑	hold_rising to CP	-0.0023			
D ↓	setup_rising to CP	0.0587			
D ↑	setup_rising to CP	0.0298			
SN ↓	min_pulse_width to SN	0.0452			
SN ↑	recovery_rising to CP	0.0028			
SN ↑	removal_rising to CP	0.0287			
TE ↓	hold_rising to CP	-0.0088			
TE ↑	hold_rising to CP	-0.0196			
TE ↓	setup_rising to CP	0.0591			
TE ↑	setup_rising to CP	0.1123			
TI ↓	hold_rising to CP	-0.0579			
TI ↑	hold_rising to CP	-0.0202			
TI ↓	setup_rising to CP	0.1114			
TI ↑	setup_rising to CP	0.0502			

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	4.952e-05	1.000e-20
X8_P16	5.671e-05	1.000e-20
X17_P16	7.717e-05	1.000e-20
X25_P16	8.558e-05	1.000e-20
X33_P16	9.392e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	1.233e-02	1.266e-02	1.277e-02	1.282e-02
Clock 100Mhz Data 25Mhz	1.279e-02	1.296e-02	1.404e-02	1.476e-02
Clock 100Mhz Data 50Mhz	1.324e-02	1.327e-02	1.531e-02	1.671e-02
Clock = 0 Data 100Mhz	7.548e-03	7.072e-03	6.915e-03	6.836e-03
Clock = 1 Data 100Mhz	1.910e-03	9.800e-04	6.700e-04	5.151e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	1.285e-02			

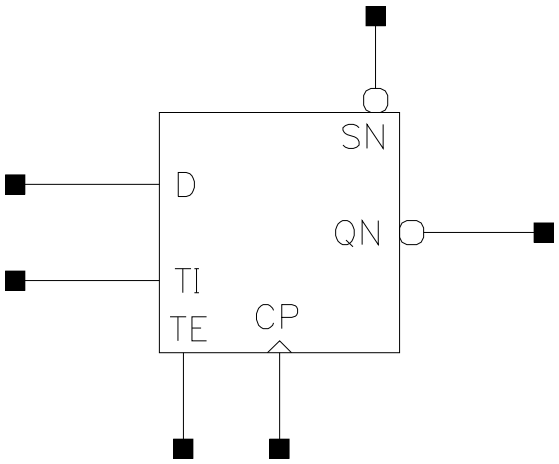
Clock 100Mhz Data 25Mhz	1.544e-02			
Clock 100Mhz Data 50Mhz	1.803e-02			
Clock = 0 Data 100Mhz	6.789e-03			
Clock = 1 Data 100Mhz	4.221e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0012	0.0012	0.0012	0.0012
D	0.0010	0.0005	0.0005	0.0005
SN	0.0017	0.0017	0.0017	0.0017
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005
	X33_P16			

CP	0.0012			
D	0.0005			
SN	0.0017			
TE	0.0012			
TI	0.0005			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0682	0.0629	3.2540	1.7135
CP to QN ↑	0.0687	0.0457	5.1705	2.6057
SN to QN ↓	0.0489	0.0534	3.2478	1.7159
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to QN ↓	0.0664	0.0707	0.8783	0.6072
CP to QN ↑	0.0540	0.0578	1.3117	0.8896
SN to QN ↓	0.0550	0.0591	0.8772	0.6064
	X33_P16		**X33_P16**	
CP to QN ↓	0.0743		0.4611	
CP to QN ↑	0.0606		0.6695	
SN to QN ↓	0.0624		0.4600	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.0904	0.0929	0.0929	0.0929
CP ↑	min_pulse_width to CP	0.0424	0.0271	0.0318	0.0318
D ↓	hold_rising to CP	-0.0533	-0.0143	-0.0147	-0.0147
D ↑	hold_rising to CP	-0.0266	-0.0023	-0.0023	-0.0023
D ↓	setup_rising to CP	0.0873	0.0587	0.0587	0.0587
D ↑	setup_rising to CP	0.0563	0.0298	0.0298	0.0298
SN ↓	min_pulse_width to SN	0.0403	0.0425	0.0500	0.0500
SN ↑	recovery_rising to CP	0.0059	0.0022	0.0048	0.0048
SN ↑	removal_rising to CP	0.0211	0.0287	0.0287	0.0287
TE ↓	hold_rising to CP	-0.0360	-0.0088	-0.0098	-0.0098
TE ↑	hold_rising to CP	-0.0332	-0.0196	-0.0196	-0.0196
TE ↓	setup_rising to CP	0.0733	0.0591	0.0591	0.0591
TE ↑	setup_rising to CP	0.1346	0.1123	0.1123	0.1155
TI ↓	hold_rising to CP	-0.1015	-0.0579	-0.0586	-0.0586
TI ↑	hold_rising to CP	-0.0370	-0.0202	-0.0202	-0.0202
TI ↓	setup_rising to CP	0.1420	0.1114	0.1114	0.1114
TI ↑	setup_rising to CP	0.0667	0.0502	0.0502	0.0502
		X33_P16			

CP ↓	min_pulse_width to CP	0.0929			
CP ↑	min_pulse_width to CP	0.0318			
D ↓	hold_rising to CP	-0.0147			
D ↑	hold_rising to CP	-0.0023			
D ↓	setup_rising to CP	0.0587			
D ↑	setup_rising to CP	0.0298			
SN ↓	min_pulse_width to SN	0.0500			
SN ↑	recovery_rising to CP	0.0048			
SN ↑	removal_rising to CP	0.0287			
TE ↓	hold_rising to CP	-0.0098			
TE ↑	hold_rising to CP	-0.0196			
TE ↓	setup_rising to CP	0.0591			
TE ↑	setup_rising to CP	0.1155			
TI ↓	hold_rising to CP	-0.0586			
TI ↑	hold_rising to CP	-0.0202			
TI ↓	setup_rising to CP	0.1114			
TI ↑	setup_rising to CP	0.0502			

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	4.974e-05	1.000e-20
X8_P16	5.868e-05	1.000e-20
X17_P16	7.955e-05	1.000e-20
X25_P16	9.061e-05	1.000e-20
X33_P16	1.017e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	1.233e-02	1.267e-02	1.278e-02	1.283e-02
Clock 100Mhz Data 25Mhz	1.246e-02	1.281e-02	1.418e-02	1.493e-02
Clock 100Mhz Data 50Mhz	1.258e-02	1.295e-02	1.557e-02	1.702e-02
Clock = 0 Data 100Mhz	7.548e-03	7.077e-03	6.917e-03	6.838e-03
Clock = 1 Data 100Mhz	1.910e-03	9.799e-04	6.700e-04	5.150e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	1.286e-02			

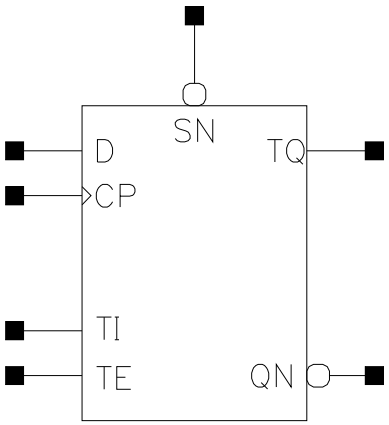
Clock 100Mhz Data 25Mhz	1.569e-02			
Clock 100Mhz Data 50Mhz	1.851e-02			
Clock = 0 Data 100Mhz	6.790e-03			
Clock = 1 Data 100Mhz	4.221e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.216	5.0592
X8_P16	1.200	4.080	4.8960
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0012	0.0012	0.0012
D	0.0010	0.0005	0.0005	0.0005

SN	0.0018	0.0019	0.0018	0.0018
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.0784	0.0661	3.2540	1.7221
CP to QN ↑	0.0887	0.0517	5.0959	2.6500
CP to TQ ↓	0.0639	0.0348	4.5847	3.9128
CP to TQ ↑	0.0604	0.0492	6.9207	6.7422
SN to QN ↓	0.0529	0.0555	3.2484	1.7214
SN to TQ ↑	0.0368	0.0383	6.8017	6.7526
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0669	0.0747	0.9012	0.4563
CP to QN ↑	0.0585	0.0652	1.3194	0.6725
CP to TQ ↓	0.0430	0.0429	4.0677	4.0708
CP to TQ ↑	0.0557	0.0557	6.8240	6.8376
SN to QN ↓	0.0579	0.0653	0.9001	0.4553
SN to TQ ↑	0.0466	0.0465	6.7964	6.8129

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0904	0.0929	0.0929	0.0929
CP ↑	min_pulse_width to CP	0.0599	0.0271	0.0330	0.0365
D ↓	hold_rising to CP	-0.0533	-0.0143	-0.0147	-0.0147
D ↑	hold_rising to CP	-0.0266	-0.0023	0.0009	0.0009
D ↓	setup_rising to CP	0.0873	0.0587	0.0587	0.0587
D ↑	setup_rising to CP	0.0563	0.0298	0.0298	0.0298
SN ↓	min_pulse_width to SN	0.0376	0.0403	0.0430	0.0430
SN ↑	recovery_rising to CP	0.0059	0.0028	0.0028	0.0028
SN ↑	removal_rising to CP	0.0211	0.0287	0.0287	0.0287
TE ↓	hold_rising to CP	-0.0360	-0.0088	-0.0098	-0.0098
TE ↑	hold_rising to CP	-0.0332	-0.0196	-0.0196	-0.0196
TE ↓	setup_rising to CP	0.0733	0.0591	0.0591	0.0591
TE ↑	setup_rising to CP	0.1346	0.1123	0.1155	0.1155
TI ↓	hold_rising to CP	-0.1015	-0.0579	-0.0579	-0.0586
TI ↑	hold_rising to CP	-0.0370	-0.0202	-0.0202	-0.0202
TI ↓	setup_rising to CP	0.1420	0.1114	0.1114	0.1114
TI ↑	setup_rising to CP	0.0667	0.0502	0.0502	0.0502

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	5.590e-05	1.000e-20
X8_P16	6.473e-05	1.000e-20
X17_P16	8.559e-05	1.000e-20
X33_P16	1.078e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

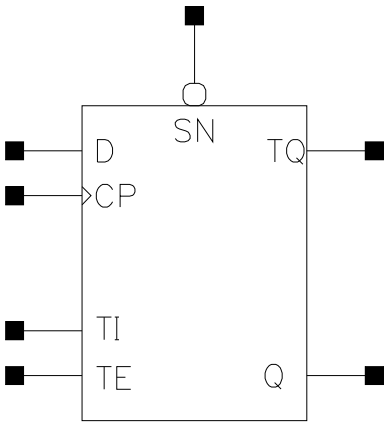
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.235e-02	1.267e-02	1.278e-02	1.284e-02
Clock 100Mhz Data 25Mhz	1.310e-02	1.320e-02	1.453e-02	1.600e-02
Clock 100Mhz Data 50Mhz	1.385e-02	1.372e-02	1.628e-02	1.915e-02
Clock = 0 Data 100Mhz	7.561e-03	7.086e-03	6.928e-03	6.848e-03
Clock = 1 Data 100Mhz	1.910e-03	9.801e-04	6.701e-04	5.151e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.944	4.7328
X17_P16	1.200	4.216	5.0592
X33_P16	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0012	0.0012	0.0012	0.0012
D	0.0010	0.0005	0.0005	0.0005

SN	0.0018	0.0017	0.0017	0.0017
TE	0.0010	0.0012	0.0012	0.0012
TI	0.0007	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0777	0.0431	3.9759	1.8295
CP to Q ↑	0.0654	0.0552	5.3946	2.7030
CP to TQ ↓	0.0772	0.0428	5.6697	4.4229
CP to TQ ↑	0.0642	0.0601	6.9742	9.3266
SN to Q ↑	0.0400	0.0442	5.2449	2.6723
SN to TQ ↑	0.0390	0.0480	6.8201	9.2771
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0588	0.0654	0.8977	0.4673
CP to Q ↑	0.0760	0.0809	1.3171	0.6721
CP to TQ ↓	0.0604	0.0678	4.2308	4.3063
CP to TQ ↑	0.0804	0.0880	9.1184	9.1702
SN to Q ↑	0.0665	0.0714	1.3172	0.6722
SN to TQ ↑	0.0709	0.0785	9.1183	9.1696

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0904	0.0929	0.0929	0.0929
CP ↑	min_pulse_width to CP	0.0693	0.0318	0.0271	0.0271
D ↓	hold_rising to CP	-0.0533	-0.0147	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0266	-0.0023	-0.0023	-0.0023
D ↓	setup_rising to CP	0.0873	0.0587	0.0587	0.0587
D ↑	setup_rising to CP	0.0563	0.0298	0.0298	0.0298
SN ↓	min_pulse_width to SN	0.0376	0.0549	0.0452	0.0452
SN ↑	recovery_rising to CP	0.0059	0.0048	0.0022	0.0028
SN ↑	removal_rising to CP	0.0211	0.0287	0.0287	0.0287
TE ↓	hold_rising to CP	-0.0360	-0.0098	-0.0088	-0.0088
TE ↑	hold_rising to CP	-0.0332	-0.0196	-0.0196	-0.0196
TE ↓	setup_rising to CP	0.0733	0.0591	0.0591	0.0591
TE ↑	setup_rising to CP	0.1367	0.1123	0.1123	0.1123
TI ↓	hold_rising to CP	-0.1015	-0.0586	-0.0579	-0.0579
TI ↑	hold_rising to CP	-0.0370	-0.0202	-0.0202	-0.0202
TI ↓	setup_rising to CP	0.1420	0.1114	0.1114	0.1114
TI ↑	setup_rising to CP	0.0667	0.0502	0.0502	0.0502

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	5.457e-05	1.000e-20
X8_P16	5.940e-05	1.000e-20
X17_P16	7.956e-05	1.000e-20
X33_P16	9.626e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

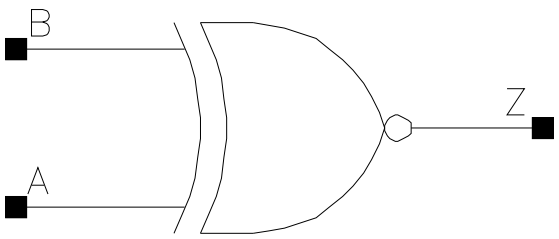
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	1.233e-02	1.266e-02	1.277e-02	1.282e-02
Clock 100Mhz Data 25Mhz	1.332e-02	1.332e-02	1.435e-02	1.584e-02
Clock 100Mhz Data 50Mhz	1.430e-02	1.399e-02	1.592e-02	1.886e-02
Clock = 0 Data 100Mhz	7.563e-03	7.081e-03	6.921e-03	6.840e-03
Clock = 1 Data 100Mhz	1.910e-03	9.801e-04	6.702e-04	5.153e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P16	X8_P16	X17_P16	X25_P16
A	0.0021	0.0008	0.0012	0.0018
B	0.0019	0.0017	0.0022	0.0031
	X33_P16			
A	0.0021			
B	0.0036			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X8_P16**	**X6_P16**	**X8_P16**
A to Z ↓	0.0189	0.0416	3.0562	1.8535
A to Z ↑	0.0191	0.0383	3.8387	2.7534
B to Z ↓	0.0175	0.0284	3.0526	1.8390
B to Z ↑	0.0200	0.0274	3.8482	2.7443
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
A to Z ↓	0.0403	0.0408	0.9111	0.6260
A to Z ↑	0.0359	0.0361	1.3504	0.8978

B to Z ↓	0.0297	0.0288	0.9079	0.6239
B to Z ↑	0.0279	0.0270	1.3477	0.8957
	X33_P16		**X33_P16**	
A to Z ↓	0.0392		0.4695	
A to Z ↑	0.0355		0.6747	
B to Z ↓	0.0279		0.4680	
B to Z ↑	0.0269		0.6734	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X6_P16	3.054e-05	1.000e-20
X8_P16	3.498e-05	1.000e-20
X17_P16	5.907e-05	1.000e-20
X25_P16	9.217e-05	1.000e-20
X33_P16	1.265e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	4.068e-03	7.661e-03	1.164e-02	1.850e-02
B to Z	3.942e-03	5.570e-03	9.260e-03	1.437e-02
	X33_P16			
A to Z	2.301e-02			
B to Z	1.840e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

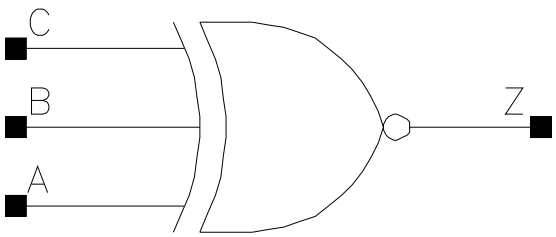
Pin Cycle (vdds)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P16			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	2.176	2.6112
X16_P16	1.200	2.720	3.2640
X25_P16	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X16_P16	X25_P16
A	0.0036	0.0029	0.0037	0.0054
B	0.0038	0.0027	0.0036	0.0049
C	0.0025	0.0009	0.0008	0.0009

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0289	0.0480	3.5841	1.9490
A to Z ↑	0.0273	0.0444	5.2066	2.7268
B to Z ↓	0.0300	0.0485	3.5849	1.9501
B to Z ↑	0.0278	0.0450	5.2054	2.7273
C to Z ↓	0.0297	0.0655	3.5925	1.9497
C to Z ↑	0.0271	0.0616	5.2109	2.7254
	X16_P16	**X25_P16**	**X16_P16**	**X25_P16**
A to Z ↓	0.0490	0.0493	1.0014	0.6396
A to Z ↑	0.0485	0.0485	1.4282	0.9007
B to Z ↓	0.0497	0.0505	1.0015	0.6397

B to Z ↑	0.0492	0.0499	1.4294	0.9011
C to Z ↓	0.0705	0.0755	1.0014	0.6396
C to Z ↑	0.0694	0.0744	1.4285	0.9007

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	3.313e-05	1.000e-20
X8_P16	3.374e-05	1.000e-20
X16_P16	5.619e-05	1.000e-20
X25_P16	8.174e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	4.282e-03	6.138e-03	1.040e-02	1.588e-02
B to Z	4.356e-03	6.101e-03	1.043e-02	1.599e-02
C to Z	4.301e-03	9.142e-03	1.414e-02	2.141e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

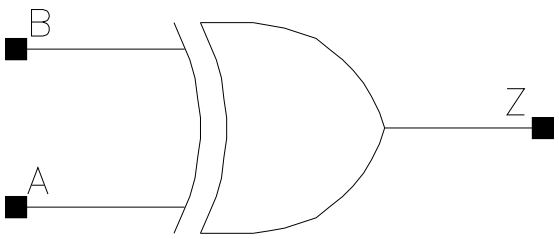
Pin Cycle (vdds)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.224	1.4688
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.224	1.4688
X16_P16	1.200	1.360	1.6320
X25_P16	1.200	2.176	2.6112
X31_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X16_P16
A	0.0009	0.0020	0.0012	0.0014
B	0.0015	0.0018	0.0018	0.0020
	X25_P16	X31_P16		
A	0.0018	0.0024		
B	0.0031	0.0041		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0370	0.0180	3.3142	2.3941
A to Z ↑	0.0356	0.0203	5.0748	4.6737
B to Z ↓	0.0264	0.0190	3.2939	2.4116
B to Z ↑	0.0268	0.0187	5.0715	4.6727
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0342	0.0364	1.8181	0.9389

A to Z ↑	0.0316	0.0339	2.6833	1.3536
B to Z ↓	0.0260	0.0276	1.8108	0.9363
B to Z ↑	0.0251	0.0271	2.6820	1.3527
	X25_P16	**X31_P16**	**X25_P16**	**X31_P16**
A to Z ↓	0.0382	0.0364	0.6220	0.4977
A to Z ↑	0.0353	0.0339	0.8958	0.7216
B to Z ↓	0.0282	0.0267	0.6210	0.4972
B to Z ↑	0.0267	0.0257	0.8958	0.7219

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	2.839e-05	1.000e-20
X6_P16	2.904e-05	1.000e-20
X8_P16	4.445e-05	1.000e-20
X16_P16	6.721e-05	1.000e-20
X25_P16	9.102e-05	1.000e-20
X31_P16	1.248e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	5.650e-03	4.064e-03	7.208e-03	1.102e-02
B to Z	4.467e-03	3.870e-03	6.044e-03	9.347e-03
	X25_P16	X31_P16		
A to Z	1.730e-02	2.138e-02		
B to Z	1.330e-02	1.648e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

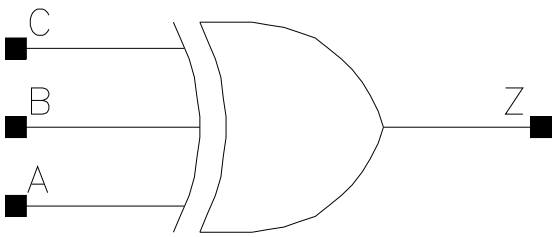
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P16	X31_P16		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X24_P16	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X24_P16
A	0.0031	0.0029	0.0037	0.0065
B	0.0031	0.0027	0.0034	0.0054
C	0.0009	0.0019	0.0027	0.0042

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0291	0.0480	3.7760	1.9488
A to Z ↑	0.0275	0.0443	5.6969	2.7245
B to Z ↓	0.0297	0.0485	3.7787	1.9494
B to Z ↑	0.0280	0.0450	5.6945	2.7249
C to Z ↓	0.0523	0.0477	3.7615	1.9496
C to Z ↑	0.0507	0.0441	5.6745	2.7240
	X17_P16	**X24_P16**	**X17_P16**	**X24_P16**
A to Z ↓	0.0451	0.0529	0.9333	0.6709
A to Z ↑	0.0449	0.0406	1.3292	0.9031
B to Z ↓	0.0456	0.0534	0.9336	0.6710

B to Z ↑	0.0455	0.0410	1.3293	0.9035
C to Z ↓	0.0453	0.0523	0.9340	0.6710
C to Z ↑	0.0452	0.0409	1.3292	0.9036

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	3.604e-05	1.000e-20
X8_P16	2.883e-05	1.000e-20
X17_P16	5.358e-05	1.000e-20
X24_P16	8.455e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	4.053e-03	6.136e-03	1.008e-02	1.692e-02
B to Z	4.112e-03	6.100e-03	1.009e-02	1.690e-02
C to Z	8.172e-03	6.019e-03	1.009e-02	1.681e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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