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C28SOI_SC_12_CLK_LL Databook

12 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

Overview

- C28SOI_SC_12_CLK_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 328 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

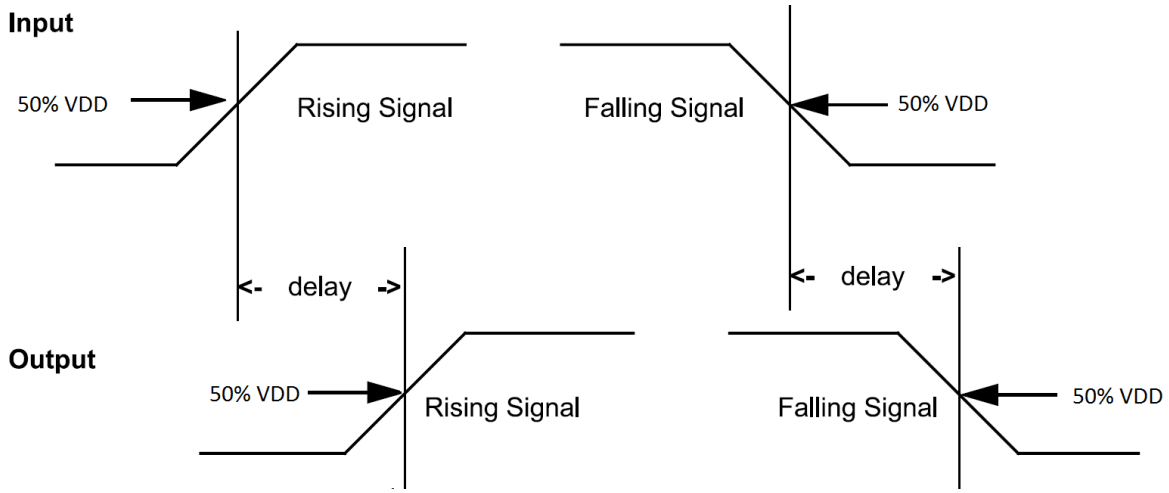


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

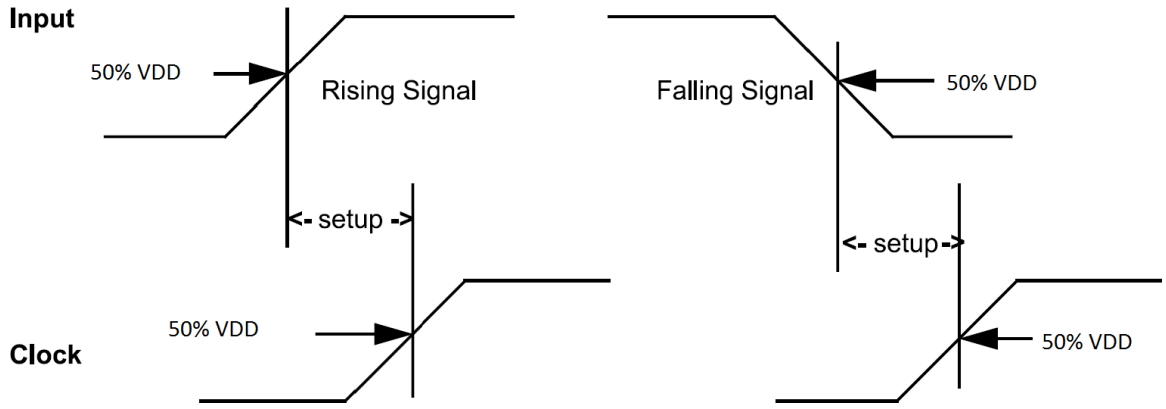


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

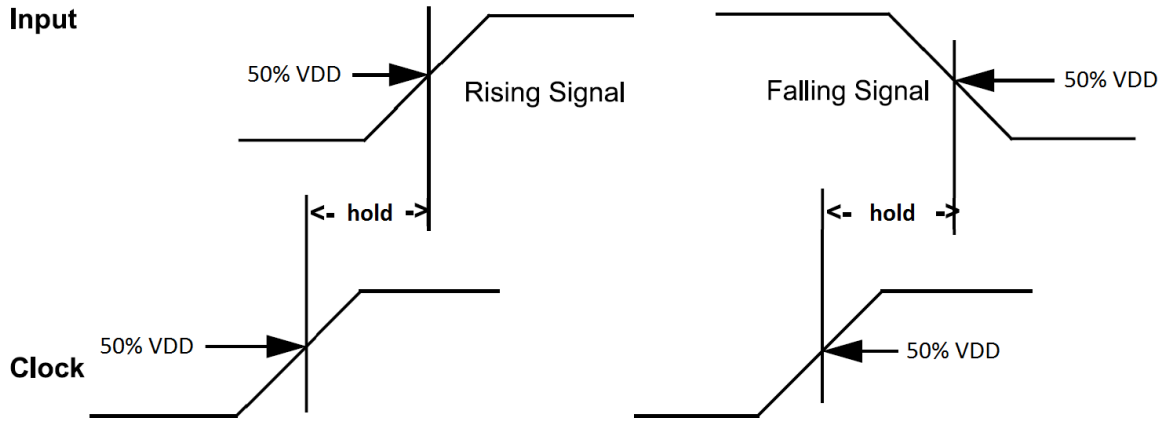


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

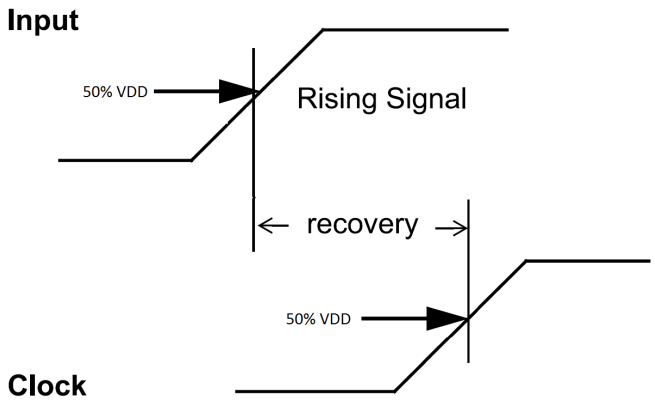


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

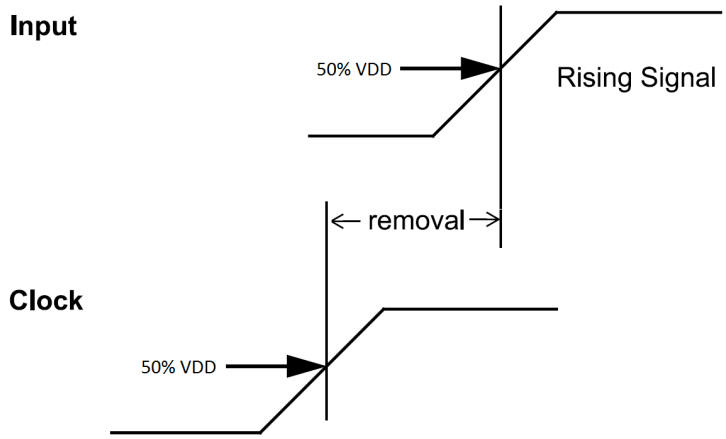


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

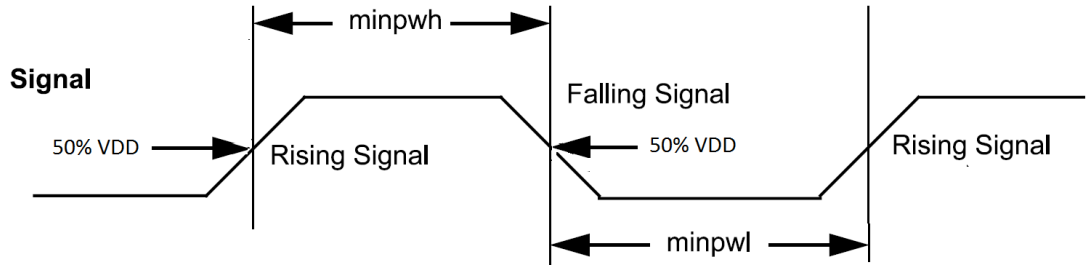


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

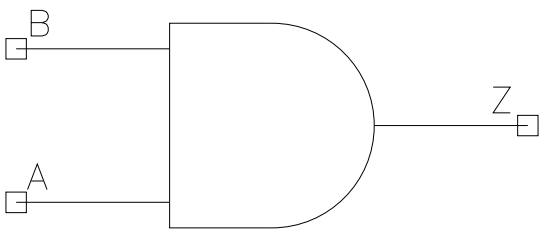
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

CNAND2

Cell Description

2 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.680	0.8160
X15_P4	1.200	0.680	0.8160
X15_P10	1.200	0.680	0.8160
X15_P16	1.200	0.680	0.8160
X20_P0	1.200	0.816	0.9792
X20_P4	1.200	0.816	0.9792
X20_P10	1.200	0.816	0.9792
X20_P16	1.200	0.816	0.9792
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0010	0.0010	0.0011	0.0012
B	0.0009	0.0010	0.0010	0.0011
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0010	0.0010	0.0011	0.0012
B	0.0009	0.0009	0.0010	0.0011
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0016	0.0017	0.0018	0.0020
B	0.0016	0.0017	0.0018	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0174	0.0197	0.8472	0.9086
A to Z ↑	0.0148	0.0163	0.8622	0.9829
B to Z ↓	0.0164	0.0187	0.8476	0.9077
B to Z ↑	0.0163	0.0179	0.8615	0.9814
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0240	0.0277	0.9949	1.0724
A to Z ↑	0.0193	0.0220	1.1652	1.3305
B to Z ↓	0.0226	0.0262	0.9950	1.0726
B to Z ↑	0.0211	0.0239	1.1640	1.3299
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0193	0.0226	0.6226	0.6677
A to Z ↑	0.0168	0.0191	0.6359	0.7266
B to Z ↓	0.0184	0.0216	0.6217	0.6676
B to Z ↑	0.0184	0.0209	0.6348	0.7259
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0274	0.0316	0.7319	0.7891
A to Z ↑	0.0226	0.0258	0.8600	0.9828
B to Z ↓	0.0262	0.0303	0.7308	0.7888
B to Z ↑	0.0246	0.0279	0.8602	0.9831
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0192	0.0222	0.3575	0.3833
A to Z ↑	0.0143	0.0163	0.4386	0.4987
B to Z ↓	0.0175	0.0202	0.3567	0.3819
B to Z ↑	0.0156	0.0176	0.4372	0.4978
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0266	0.0310	0.4195	0.4522
A to Z ↑	0.0194	0.0226	0.5883	0.6711
B to Z ↓	0.0242	0.0281	0.4180	0.4511
B to Z ↑	0.0207	0.0237	0.5879	0.6712

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X15_P0	1.539e-03	1.000e-20
X15_P4	3.885e-04	1.000e-20
X15_P10	8.463e-05	1.000e-20
X15_P16	3.179e-05	1.000e-20
X20_P0	1.957e-03	1.000e-20
X20_P4	4.892e-04	1.000e-20
X20_P10	1.057e-04	1.000e-20
X20_P16	3.953e-05	1.000e-20
X33_P0	2.906e-03	1.000e-20
X33_P4	7.427e-04	1.000e-20
X33_P10	1.648e-04	1.000e-20
X33_P16	6.295e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	2.836e-05	2.455e-05	2.182e-05	1.957e-05
B (output stable)	4.354e-05	4.586e-05	4.587e-05	4.481e-05
A to Z	7.949e-03	6.872e-03	6.414e-03	6.250e-03

B to Z	7.812e-03	6.697e-03	6.179e-03	5.980e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.682e-05	2.473e-05	2.235e-05	1.990e-05
B (output stable)	5.000e-05	4.668e-05	4.592e-05	4.462e-05
A to Z	1.055e-02	9.478e-03	8.875e-03	8.635e-03
B to Z	1.046e-02	9.336e-03	8.668e-03	8.378e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.118e-04	9.536e-05	8.463e-05	8.140e-05
B (output stable)	2.982e-04	2.897e-04	2.894e-04	3.482e-04
A to Z	1.641e-02	1.451e-02	1.349e-02	1.340e-02
B to Z	1.577e-02	1.378e-02	1.262e-02	1.239e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

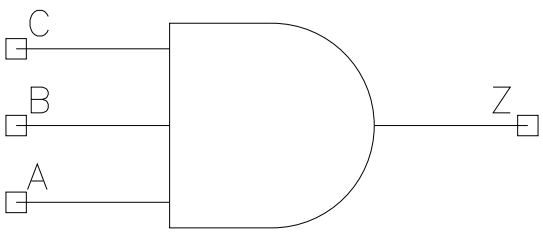
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAND3

Cell Description

3 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X25_P0	1.200	1.360	1.6320
X25_P4	1.200	1.360	1.6320
X25_P10	1.200	1.360	1.6320
X25_P16	1.200	1.360	1.6320
X33_P0	1.200	1.768	2.1216
X33_P4	1.200	1.768	2.1216
X33_P10	1.200	1.768	2.1216
X33_P16	1.200	1.768	2.1216

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0009	0.0010	0.0010	0.0011
B	0.0009	0.0009	0.0010	0.0010
C	0.0009	0.0009	0.0010	0.0011
	X25_P0	X25_P4	X25_P10	X25_P16
A	0.0018	0.0020	0.0021	0.0023
B	0.0017	0.0017	0.0019	0.0021
C	0.0016	0.0017	0.0019	0.0020
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0021	0.0023	0.0025	0.0026
B	0.0020	0.0021	0.0023	0.0025

C	0.0020	0.0021	0.0023	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0225	0.0261	0.6962	0.7465
A to Z ↑	0.0206	0.0233	0.6243	0.7113
B to Z ↓	0.0218	0.0252	0.6964	0.7470
B to Z ↑	0.0222	0.0248	0.6241	0.7113
C to Z ↓	0.0209	0.0241	0.6959	0.7465
C to Z ↑	0.0233	0.0260	0.6227	0.7106
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
A to Z ↓	0.0315	0.0368	0.8183	0.8831
A to Z ↑	0.0278	0.0324	0.8419	0.9628
B to Z ↓	0.0304	0.0355	0.8183	0.8821
B to Z ↑	0.0290	0.0333	0.8425	0.9632
C to Z ↓	0.0291	0.0339	0.8169	0.8815
C to Z ↑	0.0302	0.0345	0.8412	0.9619
	X25_P0	**X25_P4**	**X25_P0**	**X25_P4**
A to Z ↓	0.0164	0.0192	0.4809	0.5153
A to Z ↑	0.0161	0.0181	0.5956	0.6745
B to Z ↓	0.0155	0.0182	0.4807	0.5144
B to Z ↑	0.0177	0.0195	0.5956	0.6754
C to Z ↓	0.0145	0.0170	0.4807	0.5139
C to Z ↑	0.0188	0.0207	0.5951	0.6742
	X25_P10	**X25_P16**	**X25_P10**	**X25_P16**
A to Z ↓	0.0232	0.0270	0.5633	0.6064
A to Z ↑	0.0215	0.0248	0.7956	0.9064
B to Z ↓	0.0221	0.0256	0.5623	0.6059
B to Z ↑	0.0228	0.0259	0.7953	0.9062
C to Z ↓	0.0205	0.0237	0.5619	0.6051
C to Z ↑	0.0239	0.0270	0.7953	0.9061
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0175	0.0206	0.3450	0.3706
A to Z ↑	0.0183	0.0206	0.3089	0.3498
B to Z ↓	0.0166	0.0197	0.3450	0.3698
B to Z ↑	0.0199	0.0221	0.3088	0.3496
C to Z ↓	0.0158	0.0187	0.3452	0.3697
C to Z ↑	0.0212	0.0235	0.3082	0.3491
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0250	0.0292	0.4059	0.4368
A to Z ↑	0.0243	0.0280	0.4122	0.4697
B to Z ↓	0.0239	0.0278	0.4057	0.4371
B to Z ↑	0.0256	0.0291	0.4122	0.4700
C to Z ↓	0.0227	0.0264	0.4055	0.4367
C to Z ↑	0.0270	0.0304	0.4120	0.4697

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P0	2.220e-03	1.000e-20
X17_P4	5.501e-04	1.000e-20

X17_P10	1.166e-04	1.000e-20
X17_P16	4.287e-05	1.000e-20
X25_P0	2.503e-03	1.000e-20
X25_P4	6.328e-04	1.000e-20
X25_P10	1.382e-04	1.000e-20
X25_P16	5.247e-05	1.000e-20
X33_P0	4.694e-03	1.000e-20
X33_P4	1.183e-03	1.000e-20
X33_P10	2.541e-04	1.000e-20
X33_P16	9.390e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	3.333e-05	3.073e-05	2.823e-05	2.746e-05
B (output stable)	4.606e-05	4.239e-05	4.231e-05	6.612e-05
C (output stable)	8.833e-05	9.247e-05	1.069e-04	1.458e-04
A to Z	1.183e-02	1.051e-02	9.854e-03	9.721e-03
B to Z	1.166e-02	1.030e-02	9.598e-03	9.417e-03
C to Z	1.154e-02	1.012e-02	9.342e-03	9.109e-03
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	6.227e-05	5.536e-05	5.113e-05	4.978e-05
B (output stable)	9.000e-05	8.218e-05	8.066e-05	1.251e-04
C (output stable)	1.795e-04	1.887e-04	2.183e-04	2.949e-04
A to Z	1.387e-02	1.228e-02	1.146e-02	1.135e-02
B to Z	1.338e-02	1.178e-02	1.091e-02	1.072e-02
C to Z	1.299e-02	1.134e-02	1.037e-02	1.010e-02
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	7.849e-05	6.770e-05	6.315e-05	6.182e-05
B (output stable)	1.133e-04	1.006e-04	9.997e-05	1.550e-04
C (output stable)	2.356e-04	2.346e-04	2.725e-04	3.658e-04
A to Z	2.278e-02	2.032e-02	1.885e-02	1.858e-02
B to Z	2.224e-02	1.975e-02	1.819e-02	1.783e-02
C to Z	2.185e-02	1.926e-02	1.759e-02	1.710e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

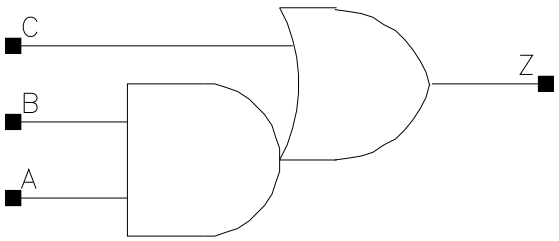
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	1.632	1.9584
X33_P4	1.200	1.632	1.9584
X33_P10	1.200	1.632	1.9584
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0019	0.0021	0.0022	0.0024
B	0.0017	0.0018	0.0020	0.0021
C	0.0017	0.0018	0.0019	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0188	0.0217	0.3592	0.3851
A to Z ↑	0.0184	0.0205	0.4386	0.4980
B to Z ↓	0.0179	0.0207	0.3590	0.3846
B to Z ↑	0.0202	0.0224	0.4382	0.4975
C to Z ↓	0.0173	0.0203	0.3586	0.3845
C to Z ↑	0.0211	0.0235	0.4351	0.4951
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0261	0.0303	0.4222	0.4556

A to Z ↑	0.0239	0.0273	0.5880	0.6706
B to Z ↓	0.0247	0.0286	0.4216	0.4550
B to Z ↑	0.0259	0.0293	0.5871	0.6704
C to Z ↓	0.0250	0.0294	0.4214	0.4549
C to Z ↑	0.0272	0.0306	0.5850	0.6675

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X33_P0	2.558e-03	1.000e-20
X33_P4	6.808e-04	1.000e-20
X33_P10	1.583e-04	1.000e-20
X33_P16	6.234e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.985e-04	2.037e-04	1.957e-04	1.788e-04
B (output stable)	2.400e-04	2.480e-04	2.425e-04	2.313e-04
C (output stable)	3.162e-04	2.574e-04	2.358e-04	2.337e-04
A to Z	1.783e-02	1.569e-02	1.445e-02	1.411e-02
B to Z	1.748e-02	1.527e-02	1.394e-02	1.352e-02
C to Z	1.871e-02	1.664e-02	1.558e-02	1.539e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

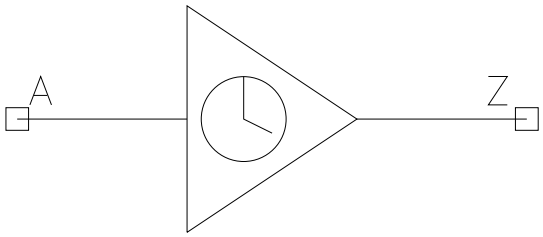
Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNBF

Cell Description

Buffer with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X4_P4	1.200	0.408	0.4896
X4_P10	1.200	0.408	0.4896
X4_P16	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X15_P0	1.200	0.544	0.6528
X15_P4	1.200	0.544	0.6528
X15_P10	1.200	0.544	0.6528
X15_P16	1.200	0.544	0.6528
X22_P0	1.200	0.680	0.8160
X22_P4	1.200	0.680	0.8160
X22_P10	1.200	0.680	0.8160
X22_P16	1.200	0.680	0.8160
X30_P0	1.200	0.952	1.1424
X30_P4	1.200	0.952	1.1424
X30_P10	1.200	0.952	1.1424
X30_P16	1.200	0.952	1.1424
X38_P0	1.200	1.088	1.3056
X38_P4	1.200	1.088	1.3056
X38_P10	1.200	1.088	1.3056
X38_P16	1.200	1.088	1.3056
X44_P0	1.200	1.224	1.4688
X44_P4	1.200	1.224	1.4688
X44_P10	1.200	1.224	1.4688
X44_P16	1.200	1.224	1.4688
X52_P0	1.200	1.496	1.7952
X52_P4	1.200	1.496	1.7952
X52_P10	1.200	1.496	1.7952
X52_P16	1.200	1.496	1.7952
X59_P0	1.200	1.632	1.9584

X59_P4	1.200	1.632	1.9584
X59_P10	1.200	1.632	1.9584
X59_P16	1.200	1.632	1.9584
X70_P0	1.200	1.768	2.1216
X70_P4	1.200	1.768	2.1216
X70_P10	1.200	1.768	2.1216
X70_P16	1.200	1.768	2.1216
X94_P0	1.200	2.312	2.7744
X94_P4	1.200	2.312	2.7744
X94_P10	1.200	2.312	2.7744
X94_P16	1.200	2.312	2.7744
X133_P0	1.200	3.264	3.9168
X133_P4	1.200	3.264	3.9168
X133_P10	1.200	3.264	3.9168
X133_P16	1.200	3.264	3.9168

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X4_P4	X4_P10	X4_P16
A	0.0007	0.0007	0.0008	0.0008
	X7_P0	X7_P4	X7_P10	X7_P16
A	0.0007	0.0007	0.0008	0.0008
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0009	0.0010	0.0011	0.0011
	X22_P0	X22_P4	X22_P10	X22_P16
A	0.0011	0.0012	0.0013	0.0013
	X30_P0	X30_P4	X30_P10	X30_P16
A	0.0016	0.0016	0.0018	0.0019
	X38_P0	X38_P4	X38_P10	X38_P16
A	0.0018	0.0020	0.0021	0.0023
	X44_P0	X44_P4	X44_P10	X44_P16
A	0.0019	0.0020	0.0022	0.0024
	X52_P0	X52_P4	X52_P10	X52_P16
A	0.0025	0.0027	0.0029	0.0032
	X59_P0	X59_P4	X59_P10	X59_P16
A	0.0029	0.0030	0.0032	0.0036
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0030	0.0031	0.0034	0.0037
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0039	0.0041	0.0045	0.0049
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0058	0.0062	0.0067	0.0073

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X4_P4	X4_P0	X4_P4
A to Z ↓	0.0163	0.0186	3.0133	3.2224

A to Z ↑	0.0125	0.0143	3.0872	3.5143
	X4_P10	**X4_P16**	**X4_P10**	**X4_P16**
A to Z ↓	0.0220	0.0251	3.5171	3.7820
A to Z ↑	0.0169	0.0192	4.1553	4.7558
	X7_P0	**X7_P4**	**X7_P0**	**X7_P4**
A to Z ↓	0.0165	0.0189	1.6527	1.7684
A to Z ↑	0.0125	0.0143	1.8367	2.0969
	X7_P10	**X7_P16**	**X7_P10**	**X7_P16**
A to Z ↓	0.0224	0.0258	1.9347	2.0814
A to Z ↑	0.0169	0.0194	2.4795	2.8324
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0158	0.0182	0.8617	0.9230
A to Z ↑	0.0140	0.0157	0.8530	0.9758
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0218	0.0253	1.0101	1.0884
A to Z ↑	0.0183	0.0209	1.1564	1.3214
	X22_P0	**X22_P4**	**X22_P0**	**X22_P4**
A to Z ↓	0.0159	0.0185	0.5872	0.6297
A to Z ↑	0.0150	0.0169	0.5745	0.6572
	X22_P10	**X22_P16**	**X22_P10**	**X22_P16**
A to Z ↓	0.0224	0.0260	0.6899	0.7433
A to Z ↑	0.0198	0.0224	0.7787	0.8886
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**
A to Z ↓	0.0152	0.0177	0.4115	0.4409
A to Z ↑	0.0132	0.0150	0.4311	0.4918
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
A to Z ↓	0.0210	0.0245	0.4834	0.5214
A to Z ↑	0.0173	0.0198	0.5819	0.6646
	X38_P0	**X38_P4**	**X38_P0**	**X38_P4**
A to Z ↓	0.0152	0.0176	0.3310	0.3551
A to Z ↑	0.0137	0.0155	0.3467	0.3952
	X38_P10	**X38_P16**	**X38_P10**	**X38_P16**
A to Z ↓	0.0211	0.0245	0.3893	0.4197
A to Z ↑	0.0180	0.0204	0.4673	0.5330
	X44_P0	**X44_P4**	**X44_P0**	**X44_P4**
A to Z ↓	0.0156	0.0180	0.2854	0.3063
A to Z ↑	0.0141	0.0159	0.3042	0.3468
	X44_P10	**X44_P16**	**X44_P10**	**X44_P16**
A to Z ↓	0.0217	0.0252	0.3355	0.3620
A to Z ↑	0.0186	0.0211	0.4104	0.4684
	X52_P0	**X52_P4**	**X52_P0**	**X52_P4**
A to Z ↓	0.0152	0.0176	0.2463	0.2642
A to Z ↑	0.0149	0.0167	0.2554	0.2901
	X52_P10	**X52_P16**	**X52_P10**	**X52_P16**
A to Z ↓	0.0212	0.0246	0.2895	0.3121
A to Z ↑	0.0195	0.0220	0.3431	0.3909
	X59_P0	**X59_P4**	**X59_P0**	**X59_P4**
A to Z ↓	0.0153	0.0177	0.2156	0.2312
A to Z ↑	0.0140	0.0158	0.2253	0.2567
	X59_P10	**X59_P16**	**X59_P10**	**X59_P16**
A to Z ↓	0.0211	0.0246	0.2534	0.2732
A to Z ↑	0.0183	0.0209	0.3034	0.3467

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0164	0.0187	0.1796	0.1927
A to Z ↑	0.0147	0.0164	0.1957	0.2226
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0225	0.0260	0.2113	0.2279
A to Z ↑	0.0192	0.0217	0.2630	0.2999
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0163	0.0186	0.1367	0.1467
A to Z ↑	0.0147	0.0164	0.1489	0.1695
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0222	0.0256	0.1610	0.1740
A to Z ↑	0.0191	0.0215	0.2000	0.2282
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0168	0.0191	0.1006	0.1086
A to Z ↑	0.0153	0.0171	0.1087	0.1238
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0227	0.0261	0.1195	0.1293
A to Z ↑	0.0199	0.0224	0.1462	0.1663

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	3.235e-04	1.000e-20
X4_P4	8.311e-05	1.000e-20
X4_P10	1.973e-05	1.000e-20
X4_P16	8.041e-06	1.000e-20
X7_P0	5.905e-04	1.000e-20
X7_P4	1.530e-04	1.000e-20
X7_P10	3.520e-05	1.000e-20
X7_P16	1.383e-05	1.000e-20
X15_P0	1.226e-03	1.000e-20
X15_P4	3.148e-04	1.000e-20
X15_P10	7.035e-05	1.000e-20
X15_P16	2.686e-05	1.000e-20
X22_P0	1.835e-03	1.000e-20
X22_P4	4.695e-04	1.000e-20
X22_P10	1.037e-04	1.000e-20
X22_P16	3.918e-05	1.000e-20
X30_P0	2.351e-03	1.000e-20
X30_P4	6.063e-04	1.000e-20
X30_P10	1.360e-04	1.000e-20
X30_P16	5.203e-05	1.000e-20
X38_P0	2.996e-03	1.000e-20
X38_P4	7.728e-04	1.000e-20
X38_P10	1.726e-04	1.000e-20
X38_P16	6.566e-05	1.000e-20
X44_P0	3.423e-03	1.000e-20
X44_P4	8.746e-04	1.000e-20
X44_P10	1.937e-04	1.000e-20
X44_P16	7.343e-05	1.000e-20
X52_P0	4.040e-03	1.000e-20
X52_P4	1.042e-03	1.000e-20
X52_P10	2.327e-04	1.000e-20

X52_P16	8.851e-05	1.000e-20
X59_P0	4.744e-03	1.000e-20
X59_P4	1.215e-03	1.000e-20
X59_P10	2.692e-04	1.000e-20
X59_P16	1.019e-04	1.000e-20
X70_P0	5.293e-03	1.000e-20
X70_P4	1.371e-03	1.000e-20
X70_P10	3.068e-04	1.000e-20
X70_P16	1.168e-04	1.000e-20
X94_P0	7.026e-03	1.000e-20
X94_P4	1.819e-03	1.000e-20
X94_P10	4.071e-04	1.000e-20
X94_P16	1.549e-04	1.000e-20
X133_P0	9.962e-03	1.000e-20
X133_P4	2.589e-03	1.000e-20
X133_P10	5.813e-04	1.000e-20
X133_P16	2.215e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	2.898e-03	2.547e-03	2.353e-03	2.300e-03
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	4.033e-03	3.529e-03	3.246e-03	3.188e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	7.302e-03	6.350e-03	5.821e-03	5.690e-03
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	1.080e-02	9.455e-03	8.677e-03	8.512e-03
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	1.430e-02	1.245e-02	1.115e-02	1.099e-02
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	1.798e-02	1.565e-02	1.422e-02	1.384e-02
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	2.045e-02	1.782e-02	1.607e-02	1.571e-02
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	2.490e-02	2.161e-02	1.980e-02	1.924e-02
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	2.803e-02	2.444e-02	2.204e-02	2.167e-02
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	3.321e-02	2.882e-02	2.633e-02	2.563e-02
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	4.451e-02	3.848e-02	3.505e-02	3.403e-02
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	6.844e-02	6.073e-02	5.538e-02	5.343e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

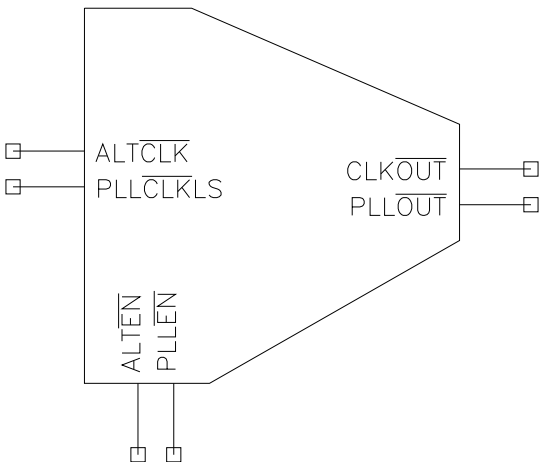
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNGFMUX21

Cell Description

2:1 Glitch-free MUX for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	2.400	2.856	6.8544
X15_P4	2.400	2.856	6.8544
X15_P10	2.400	2.856	6.8544
X15_P16	2.400	2.856	6.8544
X30_P0	2.400	3.944	9.4656
X30_P4	2.400	3.944	9.4656
X30_P10	2.400	3.944	9.4656
X30_P16	2.400	3.944	9.4656

Truth Table

PLL_CLK_LS	ALT_CLK	IPLL_EN_LD	IALT_EN_LD	CLK_OUT
0	-	-	0	0
0	0	-	-	0
-	0	0	-	0
PLL_CLK_LS	1	-	1	1
1	ALT_CLK	1	-	1
1	1	0	0	0

PLL_CLK_LS	PLL_OUT
PLL_CLK_LS	PLL_CLK_LS
1	1

PLL_EN	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

PLL_EN	0	-	PLL_EN
-	-	IPLL_EN_LD	IPLL_EN_LD
-	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

ALT_EN	ALT_CLK	IALT_EN_LD	IALT_EN_LD
ALT_EN	0	-	ALT_EN
-	-	IALT_EN_LD	IALT_EN_LD
-	ALT_CLK	IALT_EN_LD	IALT_EN_LD

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK	0.0025	0.0027	0.0029	0.0031
ALT_EN	0.0006	0.0006	0.0007	0.0007
PLL_CLK_LS	0.0035	0.0035	0.0039	0.0040
PLL_EN	0.0006	0.0006	0.0006	0.0007
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK	0.0039	0.0042	0.0045	0.0048
ALT_EN	0.0006	0.0006	0.0007	0.0007
PLL_CLK_LS	0.0053	0.0056	0.0060	0.0066
PLL_EN	0.0006	0.0006	0.0006	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
ALT_CLK to CLK_OUT ↓	0.0214	0.0243	0.8254	0.8898
ALT_CLK to CLK_OUT ↑	0.0149	0.0173	0.9989	1.1410
PLL_CLK_LS to CLK_OUT ↓	0.0196	0.0222	0.8279	0.8926
PLL_CLK_LS to CLK_OUT ↑	0.0154	0.0176	0.9982	1.1415
PLL_CLK_LS to PLL_OUT ↓	0.0160	0.0185	0.8191	0.8766
PLL_CLK_LS to PLL_OUT ↑	0.0142	0.0160	0.8571	0.9789
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
ALT_CLK to CLK_OUT ↓	0.0290	0.0335	0.9837	1.0694
ALT_CLK to CLK_OUT ↑	0.0212	0.0249	1.3530	1.5463
PLL_CLK_LS to CLK_OUT ↓	0.0262	0.0300	0.9864	1.0716
PLL_CLK_LS to CLK_OUT ↑	0.0210	0.0241	1.3548	1.5485
PLL_CLK_LS to PLL_OUT ↓	0.0222	0.0258	0.9607	1.0346
PLL_CLK_LS to PLL_OUT ↑	0.0188	0.0213	1.1595	1.3247
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**

ALT_CLK to CLK_OUT ↓	0.0206	0.0236	0.4273	0.4603
ALT_CLK to CLK_OUT ↑	0.0152	0.0176	0.4508	0.5145
PLL_CLK_LS to CLK_OUT ↓	0.0194	0.0219	0.4312	0.4641
PLL_CLK_LS to CLK_OUT ↑	0.0165	0.0186	0.4525	0.5171
PLL_CLK_LS to PLL_OUT ↓	0.0137	0.0160	0.4146	0.4441
PLL_CLK_LS to PLL_OUT ↑	0.0125	0.0141	0.4317	0.4924
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
ALT_CLK to CLK_OUT ↓	0.0282	0.0323	0.5082	0.5518
ALT_CLK to CLK_OUT ↑	0.0215	0.0249	0.6087	0.6943
PLL_CLK_LS to CLK_OUT ↓	0.0258	0.0294	0.5121	0.5556
PLL_CLK_LS to CLK_OUT ↑	0.0219	0.0249	0.6113	0.6976
PLL_CLK_LS to PLL_OUT ↓	0.0193	0.0223	0.4862	0.5237
PLL_CLK_LS to PLL_OUT ↑	0.0166	0.0188	0.5826	0.6649

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0372	0.0418	0.0462	0.0542
ALT_EN ↓	hold_rising to ALT_CLK	-0.0052	-0.0105	-0.0149	-0.0198
ALT_EN ↑	hold_rising to ALT_CLK	0.0079	0.0025	0.0009	-0.0049
ALT_EN ↓	setup_rising to ALT_CLK	0.0303	0.0352	0.0429	0.0499
ALT_EN ↑	setup_rising to ALT_CLK	0.0194	0.0222	0.0239	0.0288
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0373	0.0418	0.0462	0.0508
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0052	-0.0101	-0.0149	-0.0230
PLL_EN ↑	hold_rising to PLL_CLK_LS	0.0079	0.0058	0.0009	-0.0049
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0303	0.0352	0.0397	0.0499
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0194	0.0222	0.0239	0.0288
		X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0373	0.0418	0.0462	0.0507
ALT_EN ↓	hold_rising to ALT_CLK	-0.0052	-0.0078	-0.0149	-0.0198

ALT_EN ↑	hold_rising to ALT_CLK	0.0079	0.0025	0.0009	-0.0049
ALT_EN ↓	setup_rising to ALT_CLK	0.0303	0.0352	0.0397	0.0499
ALT_EN ↑	setup_rising to ALT_CLK	0.0194	0.0243	0.0292	0.0337
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0373	0.0418	0.0463	0.0508
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0052	-0.0101	-0.0149	-0.0257
PLL_EN ↑	hold_rising to PLL_CLK_LS	0.0084	0.0025	0.0009	-0.0049
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0335	0.0352	0.0429	0.0499
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0194	0.0243	0.0298	0.0342

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X15_P0	5.583e-03	1.000e-20
X15_P4	1.451e-03	1.000e-20
X15_P10	3.370e-04	1.000e-20
X15_P16	1.352e-04	1.000e-20
X30_P0	9.919e-03	1.000e-20
X30_P4	2.566e-03	1.000e-20
X30_P10	5.860e-04	1.000e-20
X30_P16	2.312e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	5.844e-03	5.571e-03	5.369e-03	5.412e-03
ALT_EN (output stable)	4.146e-03	3.835e-03	3.699e-03	3.752e-03
PLL_CLK_LS (output stable)	7.322e-02	2.438e-02	1.368e-02	1.186e-02
PLL_EN (output stable)	4.211e-03	3.904e-03	3.790e-03	3.835e-03
ALT_CLK to CLK_OUT	1.313e-02	1.213e-02	1.175e-02	1.189e-02
PLL_CLK_LS to CLK_OUT	9.424e-03	8.055e-03	7.549e-03	7.466e-03
PLL_CLK_LS to PLL_OUT	1.019e-01	2.896e-02	1.309e-02	1.018e-02
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	7.587e-03	7.027e-03	6.839e-03	6.917e-03
ALT_EN (output stable)	4.414e-03	4.133e-03	4.047e-03	4.111e-03
PLL_CLK_LS (output stable)	1.473e-01	5.035e-02	2.185e-02	1.871e-02

PLL_EN (output stable)	4.596e-03	4.350e-03	4.324e-03	4.424e-03
ALT_CLK to CLK_OUT	2.307e-02	2.150e-02	2.103e-02	2.111e-02
PLL_CLK_LS to CLK_OUT	1.803e-02	1.599e-02	1.355e-02	1.334e-02
PLL_CLK_LS to PLL_OUT	2.109e-01	6.620e-02	2.321e-02	1.795e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

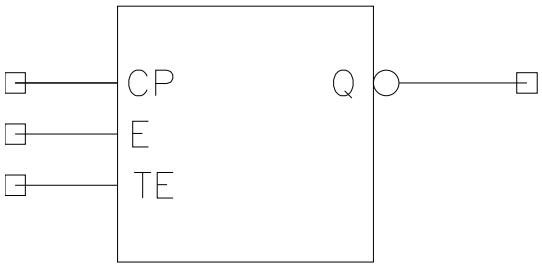
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_CLK to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to PLL_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_CLK to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to PLL_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNHLS

Cell Description

Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LLP_-CNHLSX7_P0	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX7_P4	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX7_P10	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX7_P16	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX15_P0	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX15_P4	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX15_P10	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX15_P16	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX22_P0	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX22_P4	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX22_P10	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX22_P16	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX29_P0	1.200	2.448	2.9376
C12T28SOI_LLP_-CNHLSX29_P4	1.200	2.448	2.9376
C12T28SOI_LLP_-CNHLSX29_P10	1.200	2.448	2.9376
C12T28SOI_LLP_-CNHLSX29_P16	1.200	2.448	2.9376

C12T28SOI_LLP_-CNHLSX36_P0	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX36_P4	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX36_P10	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX36_P16	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX51_P0	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX51_P4	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX51_P10	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX51_P16	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX58_P0	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX58_P4	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX58_P10	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX58_P16	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX71_P0	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX71_P4	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX71_P10	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX71_P16	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX93_P0	1.200	4.896	5.8752
C12T28SOI_LLP_-CNHLSX93_P4	1.200	4.896	5.8752
C12T28SOI_LLP_-CNHLSX93_P10	1.200	4.896	5.8752
C12T28SOI_LLP_-CNHLSX93_P16	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX29_P0	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX29_P4	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX29_P10	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX29_P16	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX36_P0	1.200	3.128	3.7536
C12T28SOI_LLPHP_-CNHLSX36_P4	1.200	3.128	3.7536

C12T28SOI_LLPHP_-CNHLSX36_P10	1.200	3.128	3.7536
C12T28SOI_LLPHP_-CNHLSX36_P16	1.200	3.128	3.7536
C12T28SOI_LLPHP_-CNHLSX44_P0	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX44_P4	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX44_P10	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX44_P16	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX51_P0	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX51_P4	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX51_P10	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX51_P16	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX58_P0	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX58_P4	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX58_P10	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX58_P16	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX71_P0	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX71_P4	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX71_P10	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX71_P16	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX86_P0	1.200	5.304	6.3648
C12T28SOI_LLPHP_-CNHLSX86_P4	1.200	5.304	6.3648
C12T28SOI_LLPHP_-CNHLSX86_P10	1.200	5.304	6.3648
C12T28SOI_LLPHP_-CNHLSX86_P16	1.200	5.304	6.3648

Truth Table

CP	E	TE	OLDIE	Q
0	-	-	-	0
1	-	-	OLDIE	OLDIE

OLDIE	OLDIE
OLDIE	OLDIE

Pin Capacitance

Pin	C12T28SOI_LLP_-CNHLSX7_P0	C12T28SOI_LLP_-CNHLSX7_P4	C12T28SOI_LLP_-CNHLSX7_P10	C12T28SOI_LLP_-CNHLSX7_P16
CP	0.0022	0.0023	0.0024	0.0025
E	0.0005	0.0006	0.0006	0.0007
TE	0.0010	0.0011	0.0012	0.0013
	C12T28SOI_LLP_-CNHLSX15_P0	C12T28SOI_LLP_-CNHLSX15_P4	C12T28SOI_LLP_-CNHLSX15_P10	C12T28SOI_LLP_-CNHLSX15_P16
CP	0.0028	0.0029	0.0031	0.0033
E	0.0005	0.0006	0.0006	0.0007
TE	0.0010	0.0011	0.0012	0.0012
	C12T28SOI_LLP_-CNHLSX22_P0	C12T28SOI_LLP_-CNHLSX22_P4	C12T28SOI_LLP_-CNHLSX22_P10	C12T28SOI_LLP_-CNHLSX22_P16
CP	0.0030	0.0031	0.0033	0.0035
E	0.0005	0.0006	0.0006	0.0007
TE	0.0010	0.0011	0.0012	0.0012
	C12T28SOI_LLP_-CNHLSX29_P0	C12T28SOI_LLP_-CNHLSX29_P4	C12T28SOI_LLP_-CNHLSX29_P10	C12T28SOI_LLP_-CNHLSX29_P16
CP	0.0032	0.0033	0.0036	0.0038
E	0.0005	0.0006	0.0006	0.0007
TE	0.0010	0.0011	0.0012	0.0012
	C12T28SOI_LLP_-CNHLSX36_P0	C12T28SOI_LLP_-CNHLSX36_P4	C12T28SOI_LLP_-CNHLSX36_P10	C12T28SOI_LLP_-CNHLSX36_P16
CP	0.0036	0.0037	0.0039	0.0042
E	0.0005	0.0006	0.0006	0.0007
TE	0.0010	0.0011	0.0012	0.0012
	C12T28SOI_LLP_-CNHLSX51_P0	C12T28SOI_LLP_-CNHLSX51_P4	C12T28SOI_LLP_-CNHLSX51_P10	C12T28SOI_LLP_-CNHLSX51_P16
CP	0.0042	0.0043	0.0046	0.0050
E	0.0005	0.0006	0.0006	0.0007
TE	0.0010	0.0011	0.0012	0.0012
	C12T28SOI_LLP_-CNHLSX58_P0	C12T28SOI_LLP_-CNHLSX58_P4	C12T28SOI_LLP_-CNHLSX58_P10	C12T28SOI_LLP_-CNHLSX58_P16
CP	0.0057	0.0059	0.0064	0.0068
E	0.0005	0.0006	0.0006	0.0006
TE	0.0010	0.0011	0.0011	0.0012
	C12T28SOI_LLP_-CNHLSX71_P0	C12T28SOI_LLP_-CNHLSX71_P4	C12T28SOI_LLP_-CNHLSX71_P10	C12T28SOI_LLP_-CNHLSX71_P16
CP	0.0065	0.0069	0.0074	0.0079
E	0.0005	0.0006	0.0006	0.0006
TE	0.0010	0.0011	0.0011	0.0012
	C12T28SOI_LLP_-CNHLSX93_P0	C12T28SOI_LLP_-CNHLSX93_P4	C12T28SOI_LLP_-CNHLSX93_P10	C12T28SOI_LLP_-CNHLSX93_P16
CP	0.0077	0.0081	0.0088	0.0094
E	0.0005	0.0006	0.0006	0.0007
TE	0.0010	0.0011	0.0012	0.0012
	C12T28SOI_LLPHP_-CNHLSX29_P0	C12T28SOI_LLPHP_-CNHLSX29_P4	C12T28SOI_LLPHP_-CNHLSX29_P10	C12T28SOI_LLPHP_-CNHLSX29_P16
CP	0.0026	0.0027	0.0029	0.0031
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_LLPHP_-CNHLSX36_P0	C12T28SOI_LLPHP_-CNHLSX36_P4	C12T28SOI_LLPHP_-CNHLSX36_P10	C12T28SOI_LLPHP_-CNHLSX36_P16

CP	0.0029	0.0031	0.0033	0.0035
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_LLPHP_-CNHLSX44_P0	C12T28SOI_LLPHP_-CNHLSX44_P4	C12T28SOI_LLPHP_-CNHLSX44_P10	C12T28SOI_LLPHP_-CNHLSX44_P16
CP	0.0034	0.0036	0.0038	0.0041
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_LLPHP_-CNHLSX51_P0	C12T28SOI_LLPHP_-CNHLSX51_P4	C12T28SOI_LLPHP_-CNHLSX51_P10	C12T28SOI_LLPHP_-CNHLSX51_P16
CP	0.0034	0.0036	0.0039	0.0041
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_LLPHP_-CNHLSX58_P0	C12T28SOI_LLPHP_-CNHLSX58_P4	C12T28SOI_LLPHP_-CNHLSX58_P10	C12T28SOI_LLPHP_-CNHLSX58_P16
CP	0.0046	0.0049	0.0053	0.0056
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_LLPHP_-CNHLSX71_P0	C12T28SOI_LLPHP_-CNHLSX71_P4	C12T28SOI_LLPHP_-CNHLSX71_P10	C12T28SOI_LLPHP_-CNHLSX71_P16
CP	0.0057	0.0060	0.0064	0.0069
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_LLPHP_-CNHLSX86_P0	C12T28SOI_LLPHP_-CNHLSX86_P4	C12T28SOI_LLPHP_-CNHLSX86_P10	C12T28SOI_LLPHP_-CNHLSX86_P16
CP	0.0068	0.0072	0.0078	0.0083
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LLP_-CNHLSX7_P0	**C12T28SOI_LLP_-CNHLSX7_P4**	**C12T28SOI_LLP_-CNHLSX7_P0**	**C12T28SOI_LLP_-CNHLSX7_P4**
CP to Q ↓	0.0200	0.0229	1.6982	1.8220
CP to Q ↑	0.0146	0.0166	1.7172	1.9616
	C12T28SOI_LLP_-CNHLSX7_P10	**C12T28SOI_LLP_-CNHLSX7_P16**	**C12T28SOI_LLP_-CNHLSX7_P10**	**C12T28SOI_LLP_-CNHLSX7_P16**
CP to Q ↓	0.0273	0.0315	1.9955	2.1527
CP to Q ↑	0.0197	0.0225	2.3266	2.6564
	C12T28SOI_LLP_-CNHLSX15_P0	**C12T28SOI_LLP_-CNHLSX15_P4**	**C12T28SOI_LLP_-CNHLSX15_P0**	**C12T28SOI_LLP_-CNHLSX15_P4**
CP to Q ↓	0.0169	0.0193	0.8570	0.9189
CP to Q ↑	0.0144	0.0163	0.8669	0.9886
	C12T28SOI_LLP_-CNHLSX15_P10	**C12T28SOI_LLP_-CNHLSX15_P16**	**C12T28SOI_LLP_-CNHLSX15_P10**	**C12T28SOI_LLP_-CNHLSX15_P16**
CP to Q ↓	0.0231	0.0265	1.0070	1.0848
CP to Q ↑	0.0192	0.0217	1.1702	1.3355
	C12T28SOI_LLP_-CNHLSX22_P0	**C12T28SOI_LLP_-CNHLSX22_P4**	**C12T28SOI_LLP_-CNHLSX22_P0**	**C12T28SOI_LLP_-CNHLSX22_P4**
CP to Q ↓	0.0169	0.0194	0.5928	0.6355
CP to Q ↑	0.0156	0.0175	0.5830	0.6653
	C12T28SOI_LLP_-CNHLSX22_P10	**C12T28SOI_LLP_-CNHLSX22_P16**	**C12T28SOI_LLP_-CNHLSX22_P10**	**C12T28SOI_LLP_-CNHLSX22_P16**

CP to Q ↓	0.0233	0.0271	0.6965	0.7500
CP to Q ↑	0.0204	0.0234	0.7878	0.8999
	C12T28SOI_LLP_-CNHLSX29_P0	**C12T28SOI_LLP_-CNHLSX29_P4**	**C12T28SOI_LLP_-CNHLSX29_P0**	**C12T28SOI_LLP_-CNHLSX29_P4**
CP to Q ↓	0.0167	0.0192	0.4440	0.4757
CP to Q ↑	0.0155	0.0175	0.4371	0.4993
	C12T28SOI_LLP_-CNHLSX29_P10	**C12T28SOI_LLP_-CNHLSX29_P16**	**C12T28SOI_LLP_-CNHLSX29_P10**	**C12T28SOI_LLP_-CNHLSX29_P16**
CP to Q ↓	0.0228	0.0266	0.5216	0.5621
CP to Q ↑	0.0203	0.0233	0.5909	0.6743
	C12T28SOI_LLP_-CNHLSX36_P0	**C12T28SOI_LLP_-CNHLSX36_P4**	**C12T28SOI_LLP_-CNHLSX36_P0**	**C12T28SOI_LLP_-CNHLSX36_P4**
CP to Q ↓	0.0165	0.0189	0.3549	0.3807
CP to Q ↑	0.0155	0.0174	0.3509	0.4003
	C12T28SOI_LLP_-CNHLSX36_P10	**C12T28SOI_LLP_-CNHLSX36_P16**	**C12T28SOI_LLP_-CNHLSX36_P10**	**C12T28SOI_LLP_-CNHLSX36_P16**
CP to Q ↓	0.0227	0.0264	0.4170	0.4495
CP to Q ↑	0.0204	0.0234	0.4737	0.5405
	C12T28SOI_LLP_-CNHLSX51_P0	**C12T28SOI_LLP_-CNHLSX51_P4**	**C12T28SOI_LLP_-CNHLSX51_P0**	**C12T28SOI_LLP_-CNHLSX51_P4**
CP to Q ↓	0.0186	0.0213	0.2576	0.2767
CP to Q ↑	0.0161	0.0182	0.2528	0.2879
	C12T28SOI_LLP_-CNHLSX51_P10	**C12T28SOI_LLP_-CNHLSX51_P16**	**C12T28SOI_LLP_-CNHLSX51_P10**	**C12T28SOI_LLP_-CNHLSX51_P16**
CP to Q ↓	0.0255	0.0295	0.3032	0.3270
CP to Q ↑	0.0213	0.0242	0.3405	0.3886
	C12T28SOI_LLP_-CNHLSX58_P0	**C12T28SOI_LLP_-CNHLSX58_P4**	**C12T28SOI_LLP_-CNHLSX58_P0**	**C12T28SOI_LLP_-CNHLSX58_P4**
CP to Q ↓	0.0162	0.0186	0.2279	0.2441
CP to Q ↑	0.0140	0.0158	0.2218	0.2528
	C12T28SOI_LLP_-CNHLSX58_P10	**C12T28SOI_LLP_-CNHLSX58_P16**	**C12T28SOI_LLP_-CNHLSX58_P10**	**C12T28SOI_LLP_-CNHLSX58_P16**
CP to Q ↓	0.0220	0.0255	0.2670	0.2878
CP to Q ↑	0.0184	0.0209	0.2989	0.3411
	C12T28SOI_LLP_-CNHLSX71_P0	**C12T28SOI_LLP_-CNHLSX71_P4**	**C12T28SOI_LLP_-CNHLSX71_P0**	**C12T28SOI_LLP_-CNHLSX71_P4**
CP to Q ↓	0.0157	0.0182	0.1883	0.2017
CP to Q ↑	0.0145	0.0163	0.1811	0.2063
	C12T28SOI_LLP_-CNHLSX71_P10	**C12T28SOI_LLP_-CNHLSX71_P16**	**C12T28SOI_LLP_-CNHLSX71_P10**	**C12T28SOI_LLP_-CNHLSX71_P16**
CP to Q ↓	0.0217	0.0249	0.2211	0.2382
CP to Q ↑	0.0190	0.0214	0.2436	0.2780
	C12T28SOI_LLP_-CNHLSX93_P0	**C12T28SOI_LLP_-CNHLSX93_P4**	**C12T28SOI_LLP_-CNHLSX93_P0**	**C12T28SOI_LLP_-CNHLSX93_P4**
CP to Q ↓	0.0169	0.0192	0.1484	0.1592
CP to Q ↑	0.0159	0.0175	0.1437	0.1636
	C12T28SOI_LLP_-CNHLSX93_P10	**C12T28SOI_LLP_-CNHLSX93_P16**	**C12T28SOI_LLP_-CNHLSX93_P10**	**C12T28SOI_LLP_-CNHLSX93_P16**
CP to Q ↓	0.0230	0.0264	0.1746	0.1884
CP to Q ↑	0.0205	0.0232	0.1929	0.2198
	C12T28SOI_-LLPHP_-CNHLSX29_P0	**C12T28SOI_-LLPHP_-CNHLSX29_P4**	**C12T28SOI_-LLPHP_-CNHLSX29_P0**	**C12T28SOI_-LLPHP_-CNHLSX29_P4**

CP to Q ↓	0.0159	0.0183	0.4514	0.4837
CP to Q ↑	0.0149	0.0167	0.4483	0.5087
	C12T28SOI_-LLPHP_-CNHLSX29_P10	**C12T28SOI_-LLPHP_-CNHLSX29_P16**	**C12T28SOI_-LLPHP_-CNHLSX29_P10**	**C12T28SOI_-LLPHP_-CNHLSX29_P16**
CP to Q ↓	0.0218	0.0253	0.5292	0.5700
CP to Q ↑	0.0195	0.0222	0.5980	0.6812
	C12T28SOI_-LLPHP_-CNHLSX36_P0	**C12T28SOI_-LLPHP_-CNHLSX36_P4**	**C12T28SOI_-LLPHP_-CNHLSX36_P0**	**C12T28SOI_-LLPHP_-CNHLSX36_P4**
CP to Q ↓	0.0156	0.0180	0.3608	0.3862
CP to Q ↑	0.0149	0.0167	0.3609	0.4094
	C12T28SOI_-LLPHP_-CNHLSX36_P10	**C12T28SOI_-LLPHP_-CNHLSX36_P16**	**C12T28SOI_-LLPHP_-CNHLSX36_P10**	**C12T28SOI_-LLPHP_-CNHLSX36_P16**
CP to Q ↓	0.0216	0.0251	0.4224	0.4547
CP to Q ↑	0.0196	0.0223	0.4816	0.5485
	C12T28SOI_-LLPHP_-CNHLSX44_P0	**C12T28SOI_-LLPHP_-CNHLSX44_P4**	**C12T28SOI_-LLPHP_-CNHLSX44_P0**	**C12T28SOI_-LLPHP_-CNHLSX44_P4**
CP to Q ↓	0.0162	0.0185	0.3017	0.3229
CP to Q ↑	0.0144	0.0161	0.3023	0.3424
	C12T28SOI_-LLPHP_-CNHLSX44_P10	**C12T28SOI_-LLPHP_-CNHLSX44_P16**	**C12T28SOI_-LLPHP_-CNHLSX44_P10**	**C12T28SOI_-LLPHP_-CNHLSX44_P16**
CP to Q ↓	0.0221	0.0254	0.3531	0.3799
CP to Q ↑	0.0188	0.0212	0.4018	0.4573
	C12T28SOI_-LLPHP_-CNHLSX51_P0	**C12T28SOI_-LLPHP_-CNHLSX51_P4**	**C12T28SOI_-LLPHP_-CNHLSX51_P0**	**C12T28SOI_-LLPHP_-CNHLSX51_P4**
CP to Q ↓	0.0174	0.0199	0.2607	0.2792
CP to Q ↑	0.0156	0.0174	0.2607	0.2953
	C12T28SOI_-LLPHP_-CNHLSX51_P10	**C12T28SOI_-LLPHP_-CNHLSX51_P16**	**C12T28SOI_-LLPHP_-CNHLSX51_P10**	**C12T28SOI_-LLPHP_-CNHLSX51_P16**
CP to Q ↓	0.0237	0.0275	0.3055	0.3291
CP to Q ↑	0.0201	0.0230	0.3465	0.3946
	C12T28SOI_-LLPHP_-CNHLSX58_P0	**C12T28SOI_-LLPHP_-CNHLSX58_P4**	**C12T28SOI_-LLPHP_-CNHLSX58_P0**	**C12T28SOI_-LLPHP_-CNHLSX58_P4**
CP to Q ↓	0.0150	0.0172	0.2282	0.2442
CP to Q ↑	0.0133	0.0149	0.2299	0.2600
	C12T28SOI_-LLPHP_-CNHLSX58_P10	**C12T28SOI_-LLPHP_-CNHLSX58_P16**	**C12T28SOI_-LLPHP_-CNHLSX58_P10**	**C12T28SOI_-LLPHP_-CNHLSX58_P16**
CP to Q ↓	0.0205	0.0239	0.2669	0.2873
CP to Q ↑	0.0173	0.0199	0.3048	0.3469
	C12T28SOI_-LLPHP_-CNHLSX71_P0	**C12T28SOI_-LLPHP_-CNHLSX71_P4**	**C12T28SOI_-LLPHP_-CNHLSX71_P0**	**C12T28SOI_-LLPHP_-CNHLSX71_P4**
CP to Q ↓	0.0149	0.0172	0.1896	0.2029
CP to Q ↑	0.0141	0.0158	0.1872	0.2117

	C12T28SOI_-LLPHP_-CNHLSX71_P10	C12T28SOI_-LLPHP_-CNHLSX71_P16	C12T28SOI_-LLPHP_-CNHLSX71_P10	C12T28SOI_-LLPHP_-CNHLSX71_P16
CP to Q ↓	0.0204	0.0238	0.2219	0.2388
CP to Q ↑	0.0182	0.0207	0.2484	0.2824
	C12T28SOI_-LLPHP_-CNHLSX86_P0	**C12T28SOI_-LLPHP_-CNHLSX86_P4**	**C12T28SOI_-LLPHP_-CNHLSX86_P0**	**C12T28SOI_-LLPHP_-CNHLSX86_P4**
CP to Q ↓	0.0145	0.0168	0.1602	0.1714
CP to Q ↑	0.0141	0.0158	0.1587	0.1789
	C12T28SOI_-LLPHP_-CNHLSX86_P10	**C12T28SOI_-LLPHP_-CNHLSX86_P16**	**C12T28SOI_-LLPHP_-CNHLSX86_P10**	**C12T28SOI_-LLPHP_-CNHLSX86_P16**
CP to Q ↓	0.0200	0.0232	0.1874	0.2018
CP to Q ↑	0.0183	0.0207	0.2098	0.2383

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C12T28SOI_-LLP_CNHLSX7_-P0	C12T28SOI_-LLP_CNHLSX7_-P4	C12T28SOI_-LLP_CNHLSX7_-P10	C12T28SOI_-LLP_CNHLSX7_-P16
CP ↓	min_pulse_width to CP	0.0195	0.0234	0.0255	0.0300
E ↓	hold_rising to CP	0.0014	-0.0007	-0.0061	-0.0078
E ↑	hold_rising to CP	0.0128	0.0106	0.0107	0.0058
E ↓	setup_rising to CP	0.0235	0.0252	0.0306	0.0355
E ↑	setup_rising to CP	0.0146	0.0141	0.0190	0.0249
TE ↓	hold_rising to CP	0.0010	0.0019	-0.0030	-0.0084
TE ↑	hold_rising to CP	0.0107	0.0107	0.0058	0.0032
TE ↓	setup_rising to CP	0.0236	0.0231	0.0279	0.0328
TE ↑	setup_rising to CP	0.0141	0.0194	0.0216	0.0265
		C12T28SOI_-LLP_-CNHLSX15_P0	C12T28SOI_-LLP_-CNHLSX15_P4	C12T28SOI_-LLP_-CNHLSX15_P10	C12T28SOI_-LLP_-CNHLSX15_P16
CP ↓	min_pulse_width to CP	0.0197	0.0211	0.0255	0.0301
E ↓	hold_rising to CP	0.0014	-0.0007	-0.0061	-0.0110
E ↑	hold_rising to CP	0.0128	0.0106	0.0085	0.0058
E ↓	setup_rising to CP	0.0261	0.0252	0.0301	0.0355
E ↑	setup_rising to CP	0.0146	0.0174	0.0191	0.0245
TE ↓	hold_rising to CP	0.0010	0.0019	-0.0030	-0.0084
TE ↑	hold_rising to CP	0.0107	0.0107	0.0058	0.0032
TE ↓	setup_rising to CP	0.0236	0.0257	0.0306	0.0355
TE ↑	setup_rising to CP	0.0142	0.0195	0.0216	0.0265

		C12T28SOI_-LLP_-CNHLSX22_P0	C12T28SOI_-LLP_-CNHLSX22_P4	C12T28SOI_-LLP_-CNHLSX22_P10	C12T28SOI_-LLP_-CNHLSX22_P16
CP ↓	min_pulse_width to CP	0.0213	0.0258	0.0296	0.0341
E ↓	hold_rising to CP	-0.0007	-0.0035	-0.0052	-0.0127
E ↑	hold_rising to CP	0.0106	0.0107	0.0058	0.0058
E ↓	setup_rising to CP	0.0256	0.0310	0.0359	0.0408
E ↑	setup_rising to CP	0.0142	0.0195	0.0249	0.0266
TE ↓	hold_rising to CP	0.0019	-0.0039	-0.0088	-0.0105
TE ↑	hold_rising to CP	0.0107	0.0058	0.0058	0.0036
TE ↓	setup_rising to CP	0.0230	0.0285	0.0334	0.0382
TE ↑	setup_rising to CP	0.0168	0.0190	0.0244	0.0293
		C12T28SOI_-LLP_-CNHLSX29_P0	C12T28SOI_-LLP_-CNHLSX29_P4	C12T28SOI_-LLP_-CNHLSX29_P10	C12T28SOI_-LLP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0219	0.0257	0.0296	0.0324
E ↓	hold_rising to CP	-0.0003	-0.0061	-0.0110	-0.0127
E ↑	hold_rising to CP	0.0106	0.0107	0.0058	0.0058
E ↓	setup_rising to CP	0.0251	0.0310	0.0355	0.0404
E ↑	setup_rising to CP	0.0142	0.0195	0.0249	0.0266
TE ↓	hold_rising to CP	0.0019	-0.0035	-0.0084	-0.0133
TE ↑	hold_rising to CP	0.0107	0.0058	0.0058	0.0036
TE ↓	setup_rising to CP	0.0289	0.0279	0.0328	0.0403
TE ↑	setup_rising to CP	0.0168	0.0190	0.0239	0.0293
		C12T28SOI_-LLP_-CNHLSX36_P0	C12T28SOI_-LLP_-CNHLSX36_P4	C12T28SOI_-LLP_-CNHLSX36_P10	C12T28SOI_-LLP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0219	0.0258	0.0296	0.0324
E ↓	hold_rising to CP	-0.0003	-0.0061	-0.0110	-0.0127
E ↑	hold_rising to CP	0.0106	0.0107	0.0058	0.0058
E ↓	setup_rising to CP	0.0251	0.0310	0.0355	0.0403
E ↑	setup_rising to CP	0.0142	0.0195	0.0249	0.0266
TE ↓	hold_rising to CP	0.0019	-0.0030	-0.0084	-0.0133
TE ↑	hold_rising to CP	0.0107	0.0058	0.0058	0.0036
TE ↓	setup_rising to CP	0.0289	0.0279	0.0328	0.0403
TE ↑	setup_rising to CP	0.0168	0.0190	0.0244	0.0293

		C12T28SOI_-LLP_-CNHLSX51_P0	C12T28SOI_-LLP_-CNHLSX51_P4	C12T28SOI_-LLP_-CNHLSX51_P10	C12T28SOI_-LLP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0220	0.0258	0.0296	0.0323
E ↓	hold_rising to CP	-0.0013	-0.0035	-0.0052	-0.0101
E ↑	hold_rising to CP	0.0106	0.0107	0.0058	0.0058
E ↓	setup_rising to CP	0.0256	0.0310	0.0359	0.0376
E ↑	setup_rising to CP	0.0142	0.0195	0.0249	0.0266
TE ↓	hold_rising to CP	0.0019	-0.0039	-0.0088	-0.0137
TE ↑	hold_rising to CP	0.0107	0.0107	0.0058	0.0036
TE ↓	setup_rising to CP	0.0231	0.0285	0.0334	0.0382
TE ↑	setup_rising to CP	0.0174	0.0190	0.0244	0.0293
		C12T28SOI_-LLP_-CNHLSX58_P0	C12T28SOI_-LLP_-CNHLSX58_P4	C12T28SOI_-LLP_-CNHLSX58_P10	C12T28SOI_-LLP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0218	0.0257	0.0302	0.0347
E ↓	hold_rising to CP	-0.0035	-0.0052	-0.0106	-0.0155
E ↑	hold_rising to CP	0.0106	0.0107	0.0058	0.0032
E ↓	setup_rising to CP	0.0310	0.0300	0.0376	0.0425
E ↑	setup_rising to CP	0.0168	0.0191	0.0239	0.0293
TE ↓	hold_rising to CP	-0.0039	-0.0056	-0.0105	-0.0154
TE ↑	hold_rising to CP	0.0107	0.0058	0.0058	0.0036
TE ↓	setup_rising to CP	0.0285	0.0338	0.0387	0.0431
TE ↑	setup_rising to CP	0.0195	0.0190	0.0239	0.0314
		C12T28SOI_-LLP_-CNHLSX71_P0	C12T28SOI_-LLP_-CNHLSX71_P4	C12T28SOI_-LLP_-CNHLSX71_P10	C12T28SOI_-LLP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0220	0.0257	0.0303	0.0348
E ↓	hold_rising to CP	-0.0061	-0.0052	-0.0101	-0.0181
E ↑	hold_rising to CP	0.0106	0.0107	0.0058	0.0032
E ↓	setup_rising to CP	0.0310	0.0301	0.0376	0.0425
E ↑	setup_rising to CP	0.0169	0.0191	0.0239	0.0293
TE ↓	hold_rising to CP	-0.0039	-0.0056	-0.0105	-0.0186
TE ↑	hold_rising to CP	0.0107	0.0058	0.0058	0.0036
TE ↓	setup_rising to CP	0.0285	0.0338	0.0383	0.0431
TE ↑	setup_rising to CP	0.0195	0.0190	0.0265	0.0314

		C12T28SOI_-LLP_-CNHLSX93_P0	C12T28SOI_-LLP_-CNHLSX93_P4	C12T28SOI_-LLP_-CNHLSX93_P10	C12T28SOI_-LLP_-CNHLSX93_P16
CP ↓	min_pulse_width to CP	0.0219	0.0264	0.0310	0.0372
E ↓	hold_rising to CP	-0.0061	-0.0110	-0.0127	-0.0176
E ↑	hold_rising to CP	0.0106	0.0107	0.0058	0.0032
E ↓	setup_rising to CP	0.0310	0.0359	0.0408	0.0457
E ↑	setup_rising to CP	0.0169	0.0191	0.0239	0.0314
TE ↓	hold_rising to CP	-0.0035	-0.0088	-0.0137	-0.0181
TE ↑	hold_rising to CP	0.0107	0.0058	0.0058	0.0036
TE ↓	setup_rising to CP	0.0279	0.0334	0.0382	0.0457
TE ↑	setup_rising to CP	0.0190	0.0249	0.0297	0.0342
		C12T28SOI_-LLPHP_-CNHLSX29_P0	C12T28SOI_-LLPHP_-CNHLSX29_P4	C12T28SOI_-LLPHP_-CNHLSX29_P10	C12T28SOI_-LLPHP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0240	0.0286	0.0355	0.0418
E ↓	hold_rising to CP	0.0075	0.0080	0.0085	0.0026
E ↑	hold_rising to CP	0.0274	0.0274	0.0269	0.0302
E ↓	setup_rising to CP	0.0214	0.0272	0.0262	0.0316
E ↑	setup_rising to CP	0.0071	0.0125	0.0174	0.0191
TE ↓	hold_rising to CP	0.0102	0.0107	0.0081	0.0053
TE ↑	hold_rising to CP	0.0248	0.0249	0.0244	0.0244
TE ↓	setup_rising to CP	0.0193	0.0247	0.0296	0.0322
TE ↑	setup_rising to CP	0.0129	0.0151	0.0200	0.0249
		C12T28SOI_-LLPHP_-CNHLSX36_P0	C12T28SOI_-LLPHP_-CNHLSX36_P4	C12T28SOI_-LLPHP_-CNHLSX36_P10	C12T28SOI_-LLPHP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0240	0.0286	0.0355	0.0418
E ↓	hold_rising to CP	0.0075	0.0080	0.0085	0.0026
E ↑	hold_rising to CP	0.0274	0.0274	0.0269	0.0302
E ↓	setup_rising to CP	0.0214	0.0272	0.0262	0.0316
E ↑	setup_rising to CP	0.0071	0.0125	0.0174	0.0191
TE ↓	hold_rising to CP	0.0102	0.0107	0.0048	0.0053
TE ↑	hold_rising to CP	0.0248	0.0249	0.0244	0.0244
TE ↓	setup_rising to CP	0.0215	0.0247	0.0296	0.0316
TE ↑	setup_rising to CP	0.0130	0.0125	0.0200	0.0217

		C12T28SOI_-LLPHP_-CNHLSX44_P0	C12T28SOI_-LLPHP_-CNHLSX44_P4	C12T28SOI_-LLPHP_-CNHLSX44_P10	C12T28SOI_-LLPHP_-CNHLSX44_P16
CP ↓	min_pulse_width to CP	0.0239	0.0286	0.0372	0.0442
E ↓	hold_rising to CP	0.0075	0.0085	0.0059	0.0031
E ↑	hold_rising to CP	0.0274	0.0274	0.0269	0.0302
E ↓	setup_rising to CP	0.0214	0.0268	0.0321	0.0337
E ↑	setup_rising to CP	0.0071	0.0125	0.0174	0.0223
TE ↓	hold_rising to CP	0.0107	0.0107	0.0048	0.0053
TE ↑	hold_rising to CP	0.0248	0.0249	0.0244	0.0244
TE ↓	setup_rising to CP	0.0247	0.0247	0.0296	0.0344
TE ↑	setup_rising to CP	0.0130	0.0151	0.0200	0.0249
		C12T28SOI_-LLPHP_-CNHLSX51_P0	C12T28SOI_-LLPHP_-CNHLSX51_P4	C12T28SOI_-LLPHP_-CNHLSX51_P10	C12T28SOI_-LLPHP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0256	0.0285	0.0371	0.0442
E ↓	hold_rising to CP	0.0075	0.0085	0.0059	0.0031
E ↑	hold_rising to CP	0.0274	0.0274	0.0269	0.0302
E ↓	setup_rising to CP	0.0214	0.0272	0.0289	0.0316
E ↑	setup_rising to CP	0.0103	0.0125	0.0174	0.0223
TE ↓	hold_rising to CP	0.0107	0.0107	0.0048	0.0053
TE ↑	hold_rising to CP	0.0248	0.0249	0.0244	0.0244
TE ↓	setup_rising to CP	0.0215	0.0247	0.0296	0.0316
TE ↑	setup_rising to CP	0.0130	0.0151	0.0200	0.0249
		C12T28SOI_-LLPHP_-CNHLSX58_P0	C12T28SOI_-LLPHP_-CNHLSX58_P4	C12T28SOI_-LLPHP_-CNHLSX58_P10	C12T28SOI_-LLPHP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0257	0.0303	0.0372	0.0448
E ↓	hold_rising to CP	0.0085	0.0085	0.0026	0.0031
E ↑	hold_rising to CP	0.0274	0.0274	0.0269	0.0302
E ↓	setup_rising to CP	0.0268	0.0262	0.0311	0.0365
E ↑	setup_rising to CP	0.0103	0.0125	0.0174	0.0249
TE ↓	hold_rising to CP	0.0107	0.0081	0.0053	0.0032
TE ↑	hold_rising to CP	0.0248	0.0249	0.0244	0.0244
TE ↓	setup_rising to CP	0.0241	0.0296	0.0312	0.0365
TE ↑	setup_rising to CP	0.0130	0.0146	0.0200	0.0249

		C12T28SOI_-LLPHP_-CNHLSX71_P0	C12T28SOI_-LLPHP_-CNHLSX71_P4	C12T28SOI_-LLPHP_-CNHLSX71_P10	C12T28SOI_-LLPHP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0288	0.0334	0.0403	0.0466
E ↓	hold_rising to CP	0.0085	0.0026	0.0031	-0.0023
E ↑	hold_rising to CP	0.0248	0.0248	0.0243	0.0243
E ↓	setup_rising to CP	0.0262	0.0317	0.0365	0.0414
E ↑	setup_rising to CP	0.0130	0.0146	0.0195	0.0249
TE ↓	hold_rising to CP	0.0081	0.0053	0.0032	0.0004
TE ↑	hold_rising to CP	0.0221	0.0253	0.0248	0.0244
TE ↓	setup_rising to CP	0.0263	0.0296	0.0344	0.0393
TE ↑	setup_rising to CP	0.0125	0.0142	0.0191	0.0266
		C12T28SOI_-LLPHP_-CNHLSX86_P0	C12T28SOI_-LLPHP_-CNHLSX86_P4	C12T28SOI_-LLPHP_-CNHLSX86_P10	C12T28SOI_-LLPHP_-CNHLSX86_P16
CP ↓	min_pulse_width to CP	0.0271	0.0310	0.0403	0.0489
E ↓	hold_rising to CP	0.0085	0.0085	0.0031	0.0010
E ↑	hold_rising to CP	0.0274	0.0248	0.0243	0.0302
E ↓	setup_rising to CP	0.0262	0.0321	0.0370	0.0418
E ↑	setup_rising to CP	0.0129	0.0146	0.0195	0.0239
TE ↓	hold_rising to CP	0.0081	0.0048	0.0032	0.0004
TE ↑	hold_rising to CP	0.0253	0.0253	0.0244	0.0244
TE ↓	setup_rising to CP	0.0268	0.0296	0.0344	0.0393
TE ↑	setup_rising to CP	0.0125	0.0174	0.0191	0.0266

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LLP_CNHLSX7_P0	2.058e-03	1.000e-20
C12T28SOI_LLP_CNHLSX7_P4	5.318e-04	1.000e-20
C12T28SOI_LLP_CNHLSX7_P10	1.218e-04	1.000e-20
C12T28SOI_LLP_CNHLSX7_P16	4.793e-05	1.000e-20
C12T28SOI_LLP_CNHLSX15_P0	2.902e-03	1.000e-20
C12T28SOI_LLP_CNHLSX15_P4	7.467e-04	1.000e-20
C12T28SOI_LLP_CNHLSX15_P10	1.686e-04	1.000e-20
C12T28SOI_LLP_CNHLSX15_P16	6.542e-05	1.000e-20
C12T28SOI_LLP_CNHLSX22_P0	3.667e-03	1.000e-20
C12T28SOI_LLP_CNHLSX22_P4	9.358e-04	1.000e-20
C12T28SOI_LLP_CNHLSX22_P10	2.079e-04	1.000e-20
C12T28SOI_LLP_CNHLSX22_P16	7.958e-05	1.000e-20
C12T28SOI_LLP_CNHLSX29_P0	4.138e-03	1.000e-20
C12T28SOI_LLP_CNHLSX29_P4	1.054e-03	1.000e-20
C12T28SOI_LLP_CNHLSX29_P10	2.345e-04	1.000e-20
C12T28SOI_LLP_CNHLSX29_P16	8.994e-05	1.000e-20

C12T28SOI_LLP_CNHLSX36_P0	4.754e-03	1.000e-20
C12T28SOI_LLP_CNHLSX36_P4	1.209e-03	1.000e-20
C12T28SOI_LLP_CNHLSX36_P10	2.682e-04	1.000e-20
C12T28SOI_LLP_CNHLSX36_P16	1.027e-04	1.000e-20
C12T28SOI_LLP_CNHLSX51_P0	5.930e-03	1.000e-20
C12T28SOI_LLP_CNHLSX51_P4	1.516e-03	1.000e-20
C12T28SOI_LLP_CNHLSX51_P10	3.377e-04	1.000e-20
C12T28SOI_LLP_CNHLSX51_P16	1.294e-04	1.000e-20
C12T28SOI_LLP_CNHLSX58_P0	7.151e-03	1.000e-20
C12T28SOI_LLP_CNHLSX58_P4	1.828e-03	1.000e-20
C12T28SOI_LLP_CNHLSX58_P10	4.071e-04	1.000e-20
C12T28SOI_LLP_CNHLSX58_P16	1.562e-04	1.000e-20
C12T28SOI_LLP_CNHLSX71_P0	8.478e-03	1.000e-20
C12T28SOI_LLP_CNHLSX71_P4	2.168e-03	1.000e-20
C12T28SOI_LLP_CNHLSX71_P10	4.824e-04	1.000e-20
C12T28SOI_LLP_CNHLSX71_P16	1.848e-04	1.000e-20
C12T28SOI_LLP_CNHLSX93_P0	1.043e-02	1.000e-20
C12T28SOI_LLP_CNHLSX93_P4	2.667e-03	1.000e-20
C12T28SOI_LLP_CNHLSX93_P10	5.928e-04	1.000e-20
C12T28SOI_LLP_CNHLSX93_P16	2.266e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P0	4.638e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P4	1.184e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P10	2.652e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P16	1.023e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P0	5.243e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P4	1.336e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P10	2.986e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P16	1.150e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P0	5.961e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P4	1.529e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P10	3.426e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P16	1.320e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P0	6.502e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P4	1.665e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P10	3.718e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P16	1.427e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P0	7.632e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P4	1.953e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P10	4.364e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P16	1.679e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P0	9.045e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P4	2.306e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P10	5.133e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P16	1.969e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P0	1.038e-02	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P4	2.659e-03	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P10	5.932e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P16	2.276e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LLP_-CNHLSX7_P0	C12T28SOI_LLP_-CNHLSX7_P4	C12T28SOI_LLP_-CNHLSX7_P10	C12T28SOI_LLP_-CNHLSX7_P16

CP (output stable)	4.041e-03	3.713e-03	3.591e-03	3.624e-03
E (output stable)	2.326e-03	2.054e-03	1.877e-03	1.816e-03
TE (output stable)	2.481e-03	2.197e-03	2.036e-03	2.000e-03
CP to Q	6.610e-03	5.788e-03	5.299e-03	5.168e-03
	C12T28SOI_LLP_-CNHLSX15_P0	C12T28SOI_LLP_-CNHLSX15_P4	C12T28SOI_LLP_-CNHLSX15_P10	C12T28SOI_LLP_-CNHLSX15_P16
CP (output stable)	4.538e-03	4.221e-03	4.142e-03	4.206e-03
E (output stable)	2.361e-03	2.096e-03	1.928e-03	1.877e-03
TE (output stable)	2.517e-03	2.239e-03	2.088e-03	2.061e-03
CP to Q	1.002e-02	8.702e-03	8.003e-03	7.749e-03
	C12T28SOI_LLP_-CNHLSX22_P0	C12T28SOI_LLP_-CNHLSX22_P4	C12T28SOI_LLP_-CNHLSX22_P10	C12T28SOI_LLP_-CNHLSX22_P16
CP (output stable)	4.958e-03	4.654e-03	4.593e-03	4.684e-03
E (output stable)	2.485e-03	2.218e-03	2.053e-03	2.005e-03
TE (output stable)	2.639e-03	2.362e-03	2.212e-03	2.188e-03
CP to Q	1.308e-02	1.142e-02	1.044e-02	1.022e-02
	C12T28SOI_LLP_-CNHLSX29_P0	C12T28SOI_LLP_-CNHLSX29_P4	C12T28SOI_LLP_-CNHLSX29_P10	C12T28SOI_LLP_-CNHLSX29_P16
CP (output stable)	5.139e-03	4.853e-03	4.814e-03	4.950e-03
E (output stable)	2.511e-03	2.247e-03	2.080e-03	2.030e-03
TE (output stable)	2.664e-03	2.388e-03	2.239e-03	2.214e-03
CP to Q	1.612e-02	1.411e-02	1.279e-02	1.257e-02
	C12T28SOI_LLP_-CNHLSX36_P0	C12T28SOI_LLP_-CNHLSX36_P4	C12T28SOI_LLP_-CNHLSX36_P10	C12T28SOI_LLP_-CNHLSX36_P16
CP (output stable)	5.456e-03	5.153e-03	5.152e-03	5.294e-03
E (output stable)	2.523e-03	2.255e-03	2.090e-03	2.043e-03
TE (output stable)	2.678e-03	2.398e-03	2.249e-03	2.226e-03
CP to Q	1.890e-02	1.645e-02	1.510e-02	1.481e-02
	C12T28SOI_LLP_-CNHLSX51_P0	C12T28SOI_LLP_-CNHLSX51_P4	C12T28SOI_LLP_-CNHLSX51_P10	C12T28SOI_LLP_-CNHLSX51_P16
CP (output stable)	5.884e-03	5.632e-03	5.682e-03	5.901e-03
E (output stable)	2.513e-03	2.258e-03	2.109e-03	2.072e-03
TE (output stable)	2.667e-03	2.401e-03	2.268e-03	2.256e-03
CP to Q	2.576e-02	2.263e-02	2.080e-02	2.033e-02
	C12T28SOI_LLP_-CNHLSX58_P0	C12T28SOI_LLP_-CNHLSX58_P4	C12T28SOI_LLP_-CNHLSX58_P10	C12T28SOI_LLP_-CNHLSX58_P16
CP (output stable)	7.359e-03	7.140e-03	7.236e-03	7.542e-03
E (output stable)	2.689e-03	2.443e-03	2.301e-03	2.274e-03
TE (output stable)	2.841e-03	2.584e-03	2.458e-03	2.456e-03
CP to Q	2.973e-02	2.584e-02	2.340e-02	2.272e-02
	C12T28SOI_LLP_-CNHLSX71_P0	C12T28SOI_LLP_-CNHLSX71_P4	C12T28SOI_LLP_-CNHLSX71_P10	C12T28SOI_LLP_-CNHLSX71_P16
CP (output stable)	8.173e-03	7.997e-03	8.196e-03	8.558e-03
E (output stable)	2.758e-03	2.514e-03	2.381e-03	2.362e-03
TE (output stable)	2.910e-03	2.655e-03	2.538e-03	2.544e-03
CP to Q	3.663e-02	3.196e-02	2.920e-02	2.818e-02
	C12T28SOI_LLP_-CNHLSX93_P0	C12T28SOI_LLP_-CNHLSX93_P4	C12T28SOI_LLP_-CNHLSX93_P10	C12T28SOI_LLP_-CNHLSX93_P16
CP (output stable)	9.139e-03	8.985e-03	9.338e-03	9.798e-03
E (output stable)	2.901e-03	2.668e-03	2.548e-03	2.543e-03
TE (output stable)	3.054e-03	2.811e-03	2.707e-03	2.728e-03
CP to Q	4.859e-02	4.198e-02	3.846e-02	3.746e-02

	C12T28SOI_LLPHP_-CNHLSX29_P0	C12T28SOI_LLPHP_-CNHLSX29_P4	C12T28SOI_LLPHP_-CNHLSX29_P10	C12T28SOI_LLPHP_-CNHLSX29_P16
CP (output stable)	6.786e-03	6.599e-03	6.656e-03	6.874e-03
E (output stable)	2.477e-03	2.183e-03	1.993e-03	1.932e-03
TE (output stable)	2.643e-03	2.334e-03	2.157e-03	2.119e-03
CP to Q	1.845e-02	1.642e-02	1.529e-02	1.514e-02
	C12T28SOI_LLPHP_-CNHLSX36_P0	C12T28SOI_LLPHP_-CNHLSX36_P4	C12T28SOI_LLPHP_-CNHLSX36_P10	C12T28SOI_LLPHP_-CNHLSX36_P16
CP (output stable)	7.061e-03	6.879e-03	6.961e-03	7.208e-03
E (output stable)	2.484e-03	2.194e-03	2.007e-03	1.948e-03
TE (output stable)	2.651e-03	2.346e-03	2.171e-03	2.135e-03
CP to Q	2.120e-02	1.886e-02	1.757e-02	1.737e-02
	C12T28SOI_LLPHP_-CNHLSX44_P0	C12T28SOI_LLPHP_-CNHLSX44_P4	C12T28SOI_LLPHP_-CNHLSX44_P10	C12T28SOI_LLPHP_-CNHLSX44_P16
CP (output stable)	7.528e-03	7.366e-03	7.500e-03	7.751e-03
E (output stable)	2.539e-03	2.253e-03	2.076e-03	2.023e-03
TE (output stable)	2.707e-03	2.405e-03	2.240e-03	2.210e-03
CP to Q	2.486e-02	2.187e-02	2.032e-02	1.984e-02
	C12T28SOI_LLPHP_-CNHLSX51_P0	C12T28SOI_LLPHP_-CNHLSX51_P4	C12T28SOI_LLPHP_-CNHLSX51_P10	C12T28SOI_LLPHP_-CNHLSX51_P16
CP (output stable)	7.566e-03	7.357e-03	7.492e-03	7.782e-03
E (output stable)	2.538e-03	2.256e-03	2.076e-03	2.023e-03
TE (output stable)	2.705e-03	2.407e-03	2.240e-03	2.210e-03
CP to Q	2.787e-02	2.464e-02	2.263e-02	2.236e-02
	C12T28SOI_LLPHP_-CNHLSX58_P0	C12T28SOI_LLPHP_-CNHLSX58_P4	C12T28SOI_LLPHP_-CNHLSX58_P10	C12T28SOI_LLPHP_-CNHLSX58_P16
CP (output stable)	8.651e-03	8.509e-03	8.748e-03	9.115e-03
E (output stable)	2.626e-03	2.345e-03	2.176e-03	2.133e-03
TE (output stable)	2.794e-03	2.498e-03	2.340e-03	2.320e-03
CP to Q	3.092e-02	2.698e-02	2.464e-02	2.437e-02
	C12T28SOI_LLPHP_-CNHLSX71_P0	C12T28SOI_LLPHP_-CNHLSX71_P4	C12T28SOI_LLPHP_-CNHLSX71_P10	C12T28SOI_LLPHP_-CNHLSX71_P16
CP (output stable)	9.577e-03	9.475e-03	9.762e-03	1.024e-02
E (output stable)	2.759e-03	2.491e-03	2.327e-03	2.289e-03
TE (output stable)	2.927e-03	2.643e-03	2.490e-03	2.477e-03
CP to Q	3.738e-02	3.298e-02	2.992e-02	2.945e-02
	C12T28SOI_LLPHP_-CNHLSX86_P0	C12T28SOI_LLPHP_-CNHLSX86_P4	C12T28SOI_LLPHP_-CNHLSX86_P10	C12T28SOI_LLPHP_-CNHLSX86_P16
CP (output stable)	1.031e-02	1.024e-02	1.061e-02	1.117e-02
E (output stable)	2.801e-03	2.536e-03	2.390e-03	2.368e-03
TE (output stable)	2.966e-03	2.687e-03	2.555e-03	2.555e-03
CP to Q	4.354e-02	3.813e-02	3.477e-02	3.407e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C12T28SOI_LLP_-CNHLSX7_P0	C12T28SOI_LLP_-CNHLSX7_P4	C12T28SOI_LLP_-CNHLSX7_P10	C12T28SOI_LLP_-CNHLSX7_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX15_P0	C12T28SOI_LLP_-CNHLSX15_P4	C12T28SOI_LLP_-CNHLSX15_P10	C12T28SOI_LLP_-CNHLSX15_P16

CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX22_P0	C12T28SOI_LLP_-CNHLSX22_P4	C12T28SOI_LLP_-CNHLSX22_P10	C12T28SOI_LLP_-CNHLSX22_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX29_P0	C12T28SOI_LLP_-CNHLSX29_P4	C12T28SOI_LLP_-CNHLSX29_P10	C12T28SOI_LLP_-CNHLSX29_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX36_P0	C12T28SOI_LLP_-CNHLSX36_P4	C12T28SOI_LLP_-CNHLSX36_P10	C12T28SOI_LLP_-CNHLSX36_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX51_P0	C12T28SOI_LLP_-CNHLSX51_P4	C12T28SOI_LLP_-CNHLSX51_P10	C12T28SOI_LLP_-CNHLSX51_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX58_P0	C12T28SOI_LLP_-CNHLSX58_P4	C12T28SOI_LLP_-CNHLSX58_P10	C12T28SOI_LLP_-CNHLSX58_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX71_P0	C12T28SOI_LLP_-CNHLSX71_P4	C12T28SOI_LLP_-CNHLSX71_P10	C12T28SOI_LLP_-CNHLSX71_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX93_P0	C12T28SOI_LLP_-CNHLSX93_P4	C12T28SOI_LLP_-CNHLSX93_P10	C12T28SOI_LLP_-CNHLSX93_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX29_P0	C12T28SOI_LLPHP_-CNHLSX29_P4	C12T28SOI_LLPHP_-CNHLSX29_P10	C12T28SOI_LLPHP_-CNHLSX29_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

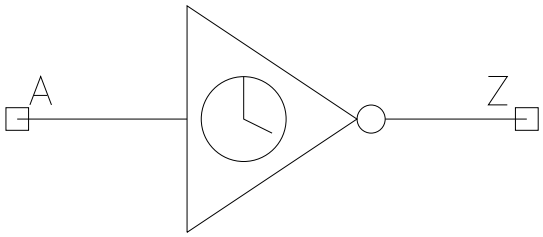
	C12T28SOI_LLPHP_-CNHLSX36_P0	C12T28SOI_LLPHP_-CNHLSX36_P4	C12T28SOI_LLPHP_-CNHLSX36_P10	C12T28SOI_LLPHP_-CNHLSX36_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX44_P0	C12T28SOI_LLPHP_-CNHLSX44_P4	C12T28SOI_LLPHP_-CNHLSX44_P10	C12T28SOI_LLPHP_-CNHLSX44_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX51_P0	C12T28SOI_LLPHP_-CNHLSX51_P4	C12T28SOI_LLPHP_-CNHLSX51_P10	C12T28SOI_LLPHP_-CNHLSX51_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX58_P0	C12T28SOI_LLPHP_-CNHLSX58_P4	C12T28SOI_LLPHP_-CNHLSX58_P10	C12T28SOI_LLPHP_-CNHLSX58_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX71_P0	C12T28SOI_LLPHP_-CNHLSX71_P4	C12T28SOI_LLPHP_-CNHLSX71_P10	C12T28SOI_LLPHP_-CNHLSX71_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX86_P0	C12T28SOI_LLPHP_-CNHLSX86_P4	C12T28SOI_LLPHP_-CNHLSX86_P10	C12T28SOI_LLPHP_-CNHLSX86_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNIV

Cell Description

Inverter with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.272	0.3264
X5_P4	1.200	0.272	0.3264
X5_P10	1.200	0.272	0.3264
X5_P16	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X16_P0	1.200	0.408	0.4896
X16_P4	1.200	0.408	0.4896
X16_P10	1.200	0.408	0.4896
X16_P16	1.200	0.408	0.4896
X23_P0	1.200	0.544	0.6528
X23_P4	1.200	0.544	0.6528
X23_P10	1.200	0.544	0.6528
X23_P16	1.200	0.544	0.6528
X31_P0	1.200	0.680	0.8160
X31_P4	1.200	0.680	0.8160
X31_P10	1.200	0.680	0.8160
X31_P16	1.200	0.680	0.8160
X39_P0	1.200	0.816	0.9792
X39_P4	1.200	0.816	0.9792
X39_P10	1.200	0.816	0.9792
X39_P16	1.200	0.816	0.9792
X47_P0	1.200	0.952	1.1424
X47_P4	1.200	0.952	1.1424
X47_P10	1.200	0.952	1.1424
X47_P16	1.200	0.952	1.1424
X55_P0	1.200	1.088	1.3056
X55_P4	1.200	1.088	1.3056
X55_P10	1.200	1.088	1.3056
X55_P16	1.200	1.088	1.3056
X61_P0	1.200	1.224	1.4688

X61_P4	1.200	1.224	1.4688
X61_P10	1.200	1.224	1.4688
X61_P16	1.200	1.224	1.4688
X70_P0	1.200	1.360	1.6320
X70_P4	1.200	1.360	1.6320
X70_P10	1.200	1.360	1.6320
X70_P16	1.200	1.360	1.6320
X94_P0	1.200	1.768	2.1216
X94_P4	1.200	1.768	2.1216
X94_P10	1.200	1.768	2.1216
X94_P16	1.200	1.768	2.1216
X133_P0	1.200	2.448	2.9376
X133_P4	1.200	2.448	2.9376
X133_P10	1.200	2.448	2.9376
X133_P16	1.200	2.448	2.9376

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X5_P0	X5_P4	X5_P10	X5_P16
A	0.0006	0.0007	0.0007	0.0007
	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0009	0.0010	0.0010	0.0011
	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0017	0.0018	0.0019	0.0021
	X23_P0	X23_P4	X23_P10	X23_P16
A	0.0026	0.0027	0.0029	0.0031
	X31_P0	X31_P4	X31_P10	X31_P16
A	0.0035	0.0036	0.0038	0.0041
	X39_P0	X39_P4	X39_P10	X39_P16
A	0.0044	0.0045	0.0048	0.0051
	X47_P0	X47_P4	X47_P10	X47_P16
A	0.0053	0.0055	0.0059	0.0062
	X55_P0	X55_P4	X55_P10	X55_P16
A	0.0061	0.0064	0.0068	0.0071
	X61_P0	X61_P4	X61_P10	X61_P16
A	0.0068	0.0070	0.0075	0.0080
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0081	0.0084	0.0089	0.0094
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0111	0.0116	0.0124	0.0130
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0161	0.0169	0.0183	0.0191

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X5_P4	X5_P0	X5_P4
A to Z ↓	0.0034	0.0041	2.5386	2.7118

A to Z ↑	0.0074	0.0083	3.1779	3.6016
	X5_P10	**X5_P16**	**X5_P10**	**X5_P16**
A to Z ↓	0.0051	0.0059	2.9474	3.1537
A to Z ↑	0.0096	0.0106	4.2441	4.8437
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0039	0.0044	1.6275	1.7393
A to Z ↑	0.0053	0.0063	1.7540	2.0014
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0052	0.0058	1.8929	2.0289
A to Z ↑	0.0075	0.0085	2.3574	2.6854
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0032	0.0036	0.8014	0.8569
A to Z ↑	0.0047	0.0055	0.8784	1.0011
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0043	0.0049	0.9323	0.9991
A to Z ↑	0.0066	0.0075	1.1775	1.3403
	X23_P0	**X23_P4**	**X23_P0**	**X23_P4**
A to Z ↓	0.0036	0.0041	0.5689	0.6084
A to Z ↑	0.0046	0.0055	0.5990	0.6805
	X23_P10	**X23_P16**	**X23_P10**	**X23_P16**
A to Z ↓	0.0048	0.0054	0.6621	0.7097
A to Z ↑	0.0066	0.0075	0.8001	0.9087
	X31_P0	**X31_P4**	**X31_P0**	**X31_P4**
A to Z ↓	0.0034	0.0038	0.4120	0.4407
A to Z ↑	0.0046	0.0054	0.4477	0.5094
	X31_P10	**X31_P16**	**X31_P10**	**X31_P16**
A to Z ↓	0.0044	0.0050	0.4797	0.5143
A to Z ↑	0.0063	0.0073	0.5986	0.6805
	X39_P0	**X39_P4**	**X39_P0**	**X39_P4**
A to Z ↓	0.0037	0.0042	0.3330	0.3560
A to Z ↑	0.0048	0.0056	0.3610	0.4104
	X39_P10	**X39_P16**	**X39_P10**	**X39_P16**
A to Z ↓	0.0049	0.0056	0.3875	0.4156
A to Z ↑	0.0067	0.0077	0.4823	0.5475
	X47_P0	**X47_P4**	**X47_P0**	**X47_P4**
A to Z ↓	0.0037	0.0042	0.2767	0.2957
A to Z ↑	0.0048	0.0057	0.3009	0.3417
	X47_P10	**X47_P16**	**X47_P10**	**X47_P16**
A to Z ↓	0.0048	0.0055	0.3222	0.3455
A to Z ↑	0.0066	0.0076	0.4016	0.4555
	X55_P0	**X55_P4**	**X55_P0**	**X55_P4**
A to Z ↓	0.0041	0.0045	0.2385	0.2550
A to Z ↑	0.0050	0.0059	0.2582	0.2936
	X55_P10	**X55_P16**	**X55_P10**	**X55_P16**
A to Z ↓	0.0052	0.0058	0.2780	0.2981
A to Z ↑	0.0070	0.0079	0.3449	0.3917
	X61_P0	**X61_P4**	**X61_P0**	**X61_P4**
A to Z ↓	0.0042	0.0047	0.2141	0.2289
A to Z ↑	0.0053	0.0061	0.2334	0.2653
	X61_P10	**X61_P16**	**X61_P10**	**X61_P16**
A to Z ↓	0.0054	0.0061	0.2495	0.2676
A to Z ↑	0.0072	0.0081	0.3118	0.3541

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0047	0.0051	0.1880	0.2012
A to Z ↑	0.0056	0.0064	0.2039	0.2310
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0059	0.0065	0.2190	0.2349
A to Z ↑	0.0075	0.0085	0.2709	0.3074
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0061	0.0065	0.1442	0.1544
A to Z ↑	0.0069	0.0076	0.1555	0.1763
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0073	0.0080	0.1683	0.1803
A to Z ↑	0.0088	0.0098	0.2067	0.2339
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0080	0.0083	0.1064	0.1140
A to Z ↑	0.0085	0.0092	0.1131	0.1281
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0093	0.0102	0.1244	0.1334
A to Z ↑	0.0107	0.0119	0.1498	0.1695

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	2.104e-04	1.000e-20
X5_P4	5.500e-05	1.000e-20
X5_P10	1.313e-05	1.000e-20
X5_P16	5.338e-06	1.000e-20
X8_P0	4.709e-04	1.000e-20
X8_P4	1.224e-04	1.000e-20
X8_P10	2.767e-05	1.000e-20
X8_P16	1.064e-05	1.000e-20
X16_P0	9.473e-04	1.000e-20
X16_P4	2.463e-04	1.000e-20
X16_P10	5.555e-05	1.000e-20
X16_P16	2.130e-05	1.000e-20
X23_P0	1.360e-03	1.000e-20
X23_P4	3.531e-04	1.000e-20
X23_P10	7.939e-05	1.000e-20
X23_P16	3.035e-05	1.000e-20
X31_P0	1.851e-03	1.000e-20
X31_P4	4.783e-04	1.000e-20
X31_P10	1.069e-04	1.000e-20
X31_P16	4.072e-05	1.000e-20
X39_P0	2.278e-03	1.000e-20
X39_P4	5.895e-04	1.000e-20
X39_P10	1.318e-04	1.000e-20
X39_P16	5.021e-05	1.000e-20
X47_P0	2.658e-03	1.000e-20
X47_P4	6.915e-04	1.000e-20
X47_P10	1.555e-04	1.000e-20
X47_P16	5.939e-05	1.000e-20
X55_P0	3.168e-03	1.000e-20
X55_P4	8.187e-04	1.000e-20
X55_P10	1.827e-04	1.000e-20

X55_P16	6.944e-05	1.000e-20
X61_P0	3.525e-03	1.000e-20
X61_P4	9.042e-04	1.000e-20
X61_P10	2.007e-04	1.000e-20
X61_P16	7.614e-05	1.000e-20
X70_P0	3.954e-03	1.000e-20
X70_P4	1.028e-03	1.000e-20
X70_P10	2.307e-04	1.000e-20
X70_P16	8.798e-05	1.000e-20
X94_P0	5.251e-03	1.000e-20
X94_P4	1.364e-03	1.000e-20
X94_P10	3.059e-04	1.000e-20
X94_P16	1.166e-04	1.000e-20
X133_P0	7.774e-03	1.000e-20
X133_P4	1.997e-03	1.000e-20
X133_P10	4.420e-04	1.000e-20
X133_P16	1.670e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	1.881e-03	1.422e-03	1.094e-03	9.362e-04
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	3.163e-03	2.368e-03	1.762e-03	1.479e-03
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	6.263e-03	4.627e-03	3.378e-03	2.751e-03
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	9.080e-03	6.771e-03	5.000e-03	4.111e-03
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	1.222e-02	8.996e-03	6.525e-03	5.338e-03
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	1.517e-02	1.127e-02	8.275e-03	6.821e-03
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	1.811e-02	1.351e-02	9.842e-03	8.114e-03
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	2.129e-02	1.587e-02	1.167e-02	9.566e-03
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	2.372e-02	1.762e-02	1.293e-02	1.060e-02
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	2.752e-02	2.054e-02	1.514e-02	1.248e-02
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	3.835e-02	2.860e-02	2.125e-02	1.760e-02
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	5.903e-02	4.438e-02	3.373e-02	2.838e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

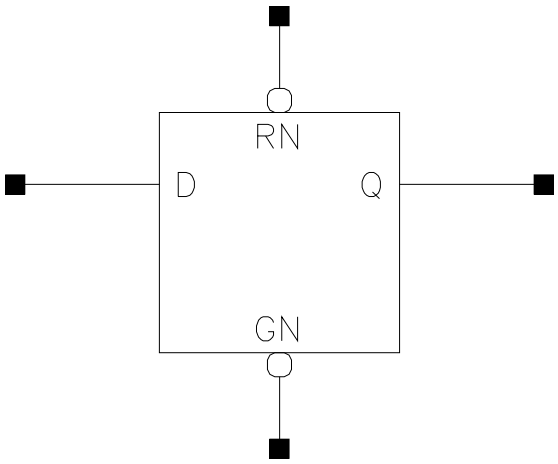
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNLDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
D	0.0013	0.0014	0.0015	0.0015
GN	0.0023	0.0024	0.0025	0.0027
RN	0.0007	0.0007	0.0007	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	X33_P4	X33_P0	X33_P4

D to Q ↓	0.0287	0.0333	0.3738	0.4032
D to Q ↑	0.0333	0.0374	0.4565	0.5208
GN to Q ↓	0.0264	0.0308	0.3742	0.4036
GN to Q ↑	0.0352	0.0399	0.4564	0.5208
RN to Q ↓	0.0377	0.0439	0.3687	0.3979
RN to Q ↑	0.0370	0.0418	0.4569	0.5209
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D to Q ↓	0.0404	0.0475	0.4450	0.4829
D to Q ↑	0.0441	0.0509	0.6171	0.7055
GN to Q ↓	0.0371	0.0432	0.4453	0.4835
GN to Q ↑	0.0473	0.0546	0.6175	0.7061
RN to Q ↓	0.0531	0.0622	0.4401	0.4787
RN to Q ↑	0.0492	0.0564	0.6174	0.7057

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X33_P0	X33_P4	X33_P10	X33_P16
D ↓	hold_rising to GN	0.0041	0.0019	-0.0025	-0.0095
D ↑	hold_rising to GN	0.0010	-0.0043	-0.0088	-0.0137
D ↓	setup_rising to GN	0.0336	0.0385	0.0450	0.0495
D ↑	setup_rising to GN	0.0394	0.0410	0.0486	0.0557
GN ↓	min_pulse_width to GN	0.0366	0.0408	0.0498	0.0576
RN ↓	min_pulse_width to RN	0.0474	0.0544	0.0664	0.0784
RN ↑	recovery_rising to GN	0.0411	0.0460	0.0530	0.0611
RN ↑	removal_rising to GN	-0.0245	-0.0261	-0.0310	-0.0418

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X33_P0	3.336e-03	1.000e-20
X33_P4	8.543e-04	1.000e-20
X33_P10	1.913e-04	1.000e-20
X33_P16	7.384e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	1.220e-04	1.057e-04	1.653e-04	2.059e-04
GN (output stable)	4.014e-03	3.330e-03	2.950e-03	2.798e-03
RN (output stable)	1.283e-04	1.097e-04	1.025e-04	9.582e-05
D to Q	2.835e-02	2.519e-02	2.322e-02	2.267e-02
GN to Q	3.336e-02	2.999e-02	2.786e-02	2.730e-02
RN to Q	2.101e-02	1.921e-02	1.812e-02	1.788e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

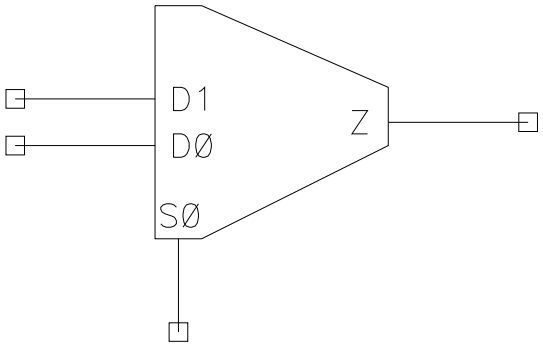
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX21

Cell Description

2:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320
X17_P4	1.200	1.360	1.6320
X17_P10	1.200	1.360	1.6320
X17_P16	1.200	1.360	1.6320
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0011	0.0012	0.0013	0.0014
D1	0.0011	0.0012	0.0013	0.0014
S0	0.0015	0.0016	0.0017	0.0018
	X33_P0	X33_P4	X33_P10	X33_P16
D0	0.0020	0.0022	0.0024	0.0025
D1	0.0020	0.0021	0.0023	0.0025
S0	0.0026	0.0027	0.0028	0.0031

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X17_P4	X17_P0	X17_P4

D0 to Z ↓	0.0198	0.0226	0.7098	0.7605
D0 to Z ↑	0.0174	0.0195	0.8692	0.9906
D1 to Z ↓	0.0194	0.0222	0.7088	0.7593
D1 to Z ↑	0.0166	0.0186	0.8688	0.9885
S0 to Z ↓	0.0191	0.0216	0.7076	0.7578
S0 to Z ↑	0.0189	0.0215	0.8693	0.9889
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0270	0.0312	0.8343	0.9009
D0 to Z ↑	0.0229	0.0261	1.1705	1.3351
D1 to Z ↓	0.0265	0.0307	0.8336	0.9005
D1 to Z ↑	0.0217	0.0248	1.1693	1.3334
S0 to Z ↓	0.0256	0.0293	0.8312	0.8978
S0 to Z ↑	0.0254	0.0292	1.1691	1.3336
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
D0 to Z ↓	0.0191	0.0220	0.3650	0.3913
D0 to Z ↑	0.0173	0.0195	0.4390	0.4990
D1 to Z ↓	0.0198	0.0227	0.3659	0.3922
D1 to Z ↑	0.0170	0.0190	0.4389	0.4989
S0 to Z ↓	0.0201	0.0228	0.3648	0.3908
S0 to Z ↑	0.0190	0.0218	0.4388	0.4992
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D0 to Z ↓	0.0264	0.0303	0.4296	0.4636
D0 to Z ↑	0.0229	0.0260	0.5900	0.6722
D1 to Z ↓	0.0271	0.0313	0.4307	0.4650
D1 to Z ↑	0.0222	0.0252	0.5902	0.6719
S0 to Z ↓	0.0269	0.0306	0.4291	0.4633
S0 to Z ↑	0.0259	0.0297	0.5896	0.6722

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P0	2.445e-03	1.000e-20
X17_P4	6.377e-04	1.000e-20
X17_P10	1.457e-04	1.000e-20
X17_P16	5.663e-05	1.000e-20
X33_P0	4.815e-03	1.000e-20
X33_P4	1.258e-03	1.000e-20
X33_P10	2.867e-04	1.000e-20
X33_P16	1.112e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	3.684e-03	2.944e-03	2.390e-03	2.126e-03
D1 (output stable)	3.698e-03	2.920e-03	2.339e-03	2.060e-03
S0 (output stable)	2.592e-03	2.257e-03	2.055e-03	1.997e-03
D0 to Z	1.082e-02	9.541e-03	8.840e-03	8.687e-03
D1 to Z	1.065e-02	9.348e-03	8.647e-03	8.487e-03
S0 to Z	1.131e-02	1.002e-02	9.324e-03	9.177e-03
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	6.811e-03	5.267e-03	4.101e-03	3.538e-03
D1 (output stable)	6.805e-03	5.326e-03	4.174e-03	3.628e-03
S0 (output stable)	4.328e-03	3.749e-03	3.386e-03	3.284e-03

D0 to Z	2.127e-02	1.886e-02	1.764e-02	1.717e-02
D1 to Z	2.120e-02	1.880e-02	1.749e-02	1.710e-02
S0 to Z	2.235e-02	2.001e-02	1.881e-02	1.841e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

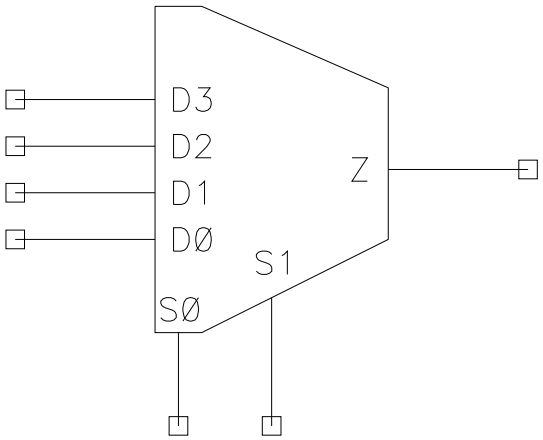
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX41

Cell Description

4:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	2.400	2.176	5.2224
X17_P4	2.400	2.176	5.2224
X17_P10	2.400	2.176	5.2224
X17_P16	2.400	2.176	5.2224
X27_P0	2.400	2.312	5.5488
X27_P4	2.400	2.312	5.5488
X27_P10	2.400	2.312	5.5488
X27_P16	2.400	2.312	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0017	0.0018	0.0020	0.0021
D1	0.0016	0.0017	0.0019	0.0020
D2	0.0017	0.0018	0.0020	0.0021
D3	0.0017	0.0018	0.0019	0.0021
S0	0.0041	0.0044	0.0048	0.0052
S1	0.0023	0.0024	0.0026	0.0028

	X27_P0	X27_P4	X27_P10	X27_P16
D0	0.0016	0.0017	0.0018	0.0019
D1	0.0015	0.0016	0.0017	0.0018
D2	0.0015	0.0016	0.0017	0.0018
D3	0.0015	0.0016	0.0017	0.0018
S0	0.0037	0.0039	0.0042	0.0045
S1	0.0020	0.0021	0.0023	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
D0 to Z ↓	0.0283	0.0329	0.7397	0.7939
D0 to Z ↑	0.0250	0.0283	0.8893	1.0107
D1 to Z ↓	0.0279	0.0325	0.7390	0.7933
D1 to Z ↑	0.0247	0.0280	0.8886	1.0097
D2 to Z ↓	0.0282	0.0330	0.7394	0.7936
D2 to Z ↑	0.0244	0.0277	0.8872	1.0085
D3 to Z ↓	0.0279	0.0327	0.7391	0.7934
D3 to Z ↑	0.0242	0.0275	0.8872	1.0083
S0 to Z ↓	0.0342	0.0400	0.7379	0.7916
S0 to Z ↑	0.0318	0.0367	0.8894	1.0104
S1 to Z ↓	0.0249	0.0284	0.7397	0.7924
S1 to Z ↑	0.0253	0.0285	0.8880	1.0093
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0397	0.0467	0.8704	0.9415
D0 to Z ↑	0.0332	0.0383	1.1926	1.3596
D1 to Z ↓	0.0392	0.0461	0.8706	0.9415
D1 to Z ↑	0.0328	0.0378	1.1917	1.3600
D2 to Z ↓	0.0402	0.0474	0.8706	0.9411
D2 to Z ↑	0.0327	0.0376	1.1910	1.3596
D3 to Z ↓	0.0398	0.0469	0.8703	0.9414
D3 to Z ↑	0.0324	0.0373	1.1903	1.3586
S0 to Z ↓	0.0487	0.0573	0.8684	0.9392
S0 to Z ↑	0.0441	0.0514	1.1930	1.3605
S1 to Z ↓	0.0333	0.0384	0.8691	0.9403
S1 to Z ↑	0.0334	0.0383	1.1920	1.3595
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0316	0.0368	0.4667	0.5023
D0 to Z ↑	0.0320	0.0360	0.5992	0.6807
D1 to Z ↓	0.0287	0.0334	0.4619	0.4965
D1 to Z ↑	0.0310	0.0349	0.5993	0.6796
D2 to Z ↓	0.0323	0.0380	0.4671	0.5033
D2 to Z ↑	0.0313	0.0353	0.5986	0.6800
D3 to Z ↓	0.0320	0.0376	0.4671	0.5032
D3 to Z ↑	0.0309	0.0349	0.5984	0.6799
S0 to Z ↓	0.0379	0.0443	0.4643	0.4997
S0 to Z ↑	0.0372	0.0429	0.6002	0.6811
S1 to Z ↓	0.0259	0.0299	0.4662	0.5012
S1 to Z ↑	0.0352	0.0394	0.5992	0.6804
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.0449	0.0526	0.5541	0.6014
D0 to Z ↑	0.0426	0.0487	0.8038	0.9163

D1 to Z ↓	0.0407	0.0476	0.5469	0.5922
D1 to Z ↑	0.0414	0.0475	0.8033	0.9162
D2 to Z ↓	0.0468	0.0547	0.5554	0.6028
D2 to Z ↑	0.0419	0.0479	0.8038	0.9167
D3 to Z ↓	0.0463	0.0542	0.5552	0.6026
D3 to Z ↑	0.0414	0.0473	0.8030	0.9161
S0 to Z ↓	0.0541	0.0632	0.5511	0.5978
S0 to Z ↑	0.0517	0.0600	0.8044	0.9174
S1 to Z ↓	0.0361	0.0417	0.5526	0.5994
S1 to Z ↑	0.0464	0.0530	0.8035	0.9161

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P0	3.218e-03	1.000e-20
X17_P4	8.585e-04	1.000e-20
X17_P10	2.042e-04	1.000e-20
X17_P16	8.410e-05	1.000e-20
X27_P0	3.371e-03	1.000e-20
X27_P4	8.944e-04	1.000e-20
X27_P10	2.114e-04	1.000e-20
X27_P16	8.631e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	1.784e-04	1.701e-04	1.605e-04	1.690e-04
D1 (output stable)	1.380e-04	1.281e-04	1.194e-04	1.187e-04
D2 (output stable)	1.832e-04	1.734e-04	1.632e-04	1.691e-04
D3 (output stable)	1.820e-04	1.710e-04	1.619e-04	1.717e-04
S0 (output stable)	6.047e-03	5.769e-03	5.797e-03	6.024e-03
S1 (output stable)	5.680e-03	5.254e-03	5.098e-03	5.127e-03
D0 to Z	1.485e-02	1.373e-02	1.321e-02	1.335e-02
D1 to Z	1.481e-02	1.370e-02	1.318e-02	1.333e-02
D2 to Z	1.502e-02	1.395e-02	1.353e-02	1.369e-02
D3 to Z	1.488e-02	1.380e-02	1.338e-02	1.353e-02
S0 to Z	2.091e-02	1.997e-02	1.986e-02	2.040e-02
S1 to Z	1.758e-02	1.613e-02	1.531e-02	1.511e-02
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	1.770e-04	1.634e-04	1.523e-04	1.481e-04
D1 (output stable)	1.388e-04	1.286e-04	1.193e-04	1.198e-04
D2 (output stable)	1.776e-04	1.618e-04	1.494e-04	1.432e-04
D3 (output stable)	1.737e-04	1.596e-04	1.487e-04	1.535e-04
S0 (output stable)	5.745e-03	5.419e-03	5.386e-03	5.555e-03
S1 (output stable)	4.808e-03	4.527e-03	4.476e-03	4.487e-03
D0 to Z	2.097e-02	1.892e-02	1.793e-02	1.767e-02
D1 to Z	2.031e-02	1.834e-02	1.741e-02	1.720e-02
D2 to Z	2.103e-02	1.907e-02	1.815e-02	1.787e-02
D3 to Z	2.085e-02	1.890e-02	1.798e-02	1.770e-02
S0 to Z	2.630e-02	2.448e-02	2.385e-02	2.393e-02
S1 to Z	2.275e-02	2.058e-02	1.944e-02	1.889e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

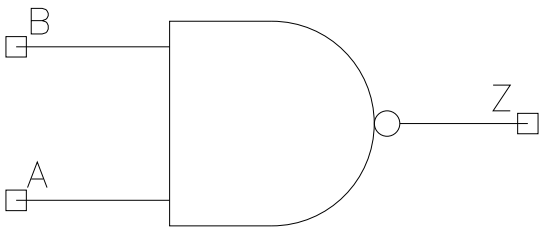
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2

Cell Description

2 input NAND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X33_P0	1.200	1.224	1.4688
X33_P4	1.200	1.224	1.4688
X33_P10	1.200	1.224	1.4688
X33_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0022	0.0023	0.0025	0.0026
B	0.0021	0.0022	0.0023	0.0024
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0008	0.0009	0.0010	0.0010
B	0.0008	0.0009	0.0009	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0039	0.0046	0.9148	0.9836
A to Z ↑	0.0087	0.0100	0.8998	1.0284
B to Z ↓	0.0049	0.0054	0.9288	1.0000
B to Z ↑	0.0063	0.0074	0.9094	1.0379
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0057	0.0067	1.0822	1.1708
A to Z ↑	0.0118	0.0134	1.2112	1.3779
B to Z ↓	0.0062	0.0069	1.1007	1.1908
B to Z ↑	0.0087	0.0099	1.2224	1.3902
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0219	0.0249	0.3604	0.3858
A to Z ↑	0.0250	0.0288	0.4368	0.4963
B to Z ↓	0.0236	0.0267	0.3600	0.3855
B to Z ↑	0.0241	0.0278	0.4366	0.4967
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0304	0.0354	0.4221	0.4547
A to Z ↑	0.0353	0.0411	0.5866	0.6684
B to Z ↓	0.0322	0.0373	0.4220	0.4546
B to Z ↑	0.0340	0.0396	0.5860	0.6684

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X15_P0	9.570e-04	1.000e-20
X15_P4	2.545e-04	1.000e-20
X15_P10	6.014e-05	1.000e-20
X15_P16	2.445e-05	1.000e-20
X33_P0	2.643e-03	1.000e-20
X33_P4	6.950e-04	1.000e-20
X33_P10	1.601e-04	1.000e-20
X33_P16	6.241e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.382e-04	1.212e-04	1.085e-04	1.064e-04
B (output stable)	2.874e-04	3.022e-04	3.099e-04	3.249e-04
A to Z	7.443e-03	5.955e-03	4.918e-03	4.493e-03
B to Z	6.582e-03	5.044e-03	3.899e-03	3.352e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	2.818e-05	2.155e-05	1.916e-05	1.722e-05
B (output stable)	3.500e-05	3.818e-05	3.797e-05	3.740e-05
A to Z	1.594e-02	1.474e-02	1.459e-02	1.479e-02
B to Z	1.582e-02	1.459e-02	1.439e-02	1.455e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

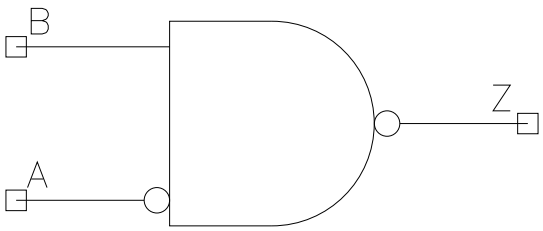
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2A

Cell Description

2 input NAND with A input inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0009	0.0009	0.0010	0.0011
B	0.0010	0.0011	0.0012	0.0012
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0013	0.0014	0.0015	0.0016
B	0.0009	0.0010	0.0011	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0169	0.0194	0.7007	0.7507
A to Z ↑	0.0171	0.0191	0.8666	0.9857
B to Z ↓	0.0205	0.0231	0.6987	0.7494
B to Z ↑	0.0201	0.0229	0.8654	0.9858
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**

A to Z ↓	0.0239	0.0278	0.8234	0.8896
A to Z ↑	0.0225	0.0252	1.1674	1.3307
B to Z ↓	0.0280	0.0323	0.8228	0.8877
B to Z ↑	0.0275	0.0315	1.1657	1.3288
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0184	0.0214	0.4181	0.4492
A to Z ↑	0.0195	0.0218	0.5615	0.6383
B to Z ↓	0.0218	0.0248	0.4171	0.4480
B to Z ↑	0.0223	0.0256	0.5603	0.6369
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0262	0.0309	0.4930	0.5330
A to Z ↑	0.0253	0.0288	0.7540	0.8614
B to Z ↓	0.0296	0.0344	0.4919	0.5318
B to Z ↑	0.0307	0.0357	0.7520	0.8589

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X17_P0	1.557e-03	1.000e-20
X17_P4	4.163e-04	1.000e-20
X17_P10	9.776e-05	1.000e-20
X17_P16	3.867e-05	1.000e-20
X27_P0	2.012e-03	1.000e-20
X27_P4	5.362e-04	1.000e-20
X27_P10	1.270e-04	1.000e-20
X27_P16	5.079e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	6.645e-05	4.744e-05	4.171e-05	3.999e-05
B (output stable)	3.542e-03	2.842e-03	2.342e-03	2.121e-03
A to Z	8.947e-03	7.808e-03	7.315e-03	7.117e-03
B to Z	1.074e-02	9.628e-03	9.218e-03	9.063e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.739e-04	1.444e-04	1.355e-04	1.343e-04
B (output stable)	3.541e-03	2.937e-03	2.475e-03	2.369e-03
A to Z	1.457e-02	1.289e-02	1.201e-02	1.191e-02
B to Z	1.517e-02	1.388e-02	1.332e-02	1.341e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

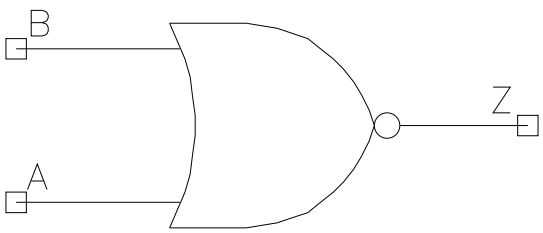
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2

Cell Description

2 input NOR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	0.952	1.1424
X14_P4	1.200	0.952	1.1424
X14_P10	1.200	0.952	1.1424
X14_P16	1.200	0.952	1.1424
X33_P0	1.200	1.496	1.7952
X33_P4	1.200	1.496	1.7952
X33_P10	1.200	1.496	1.7952
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0024	0.0025	0.0027	0.0029
B	0.0022	0.0023	0.0025	0.0026
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0010	0.0010	0.0011	0.0012
B	0.0010	0.0010	0.0011	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0072	0.0081	0.8107	0.8656
A to Z ↑	0.0058	0.0069	1.1198	1.2508
B to Z ↓	0.0047	0.0054	0.8222	0.8777
B to Z ↑	0.0066	0.0075	1.1320	1.2644
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**

A to Z ↓	0.0093	0.0104	0.9428	1.0094
A to Z ↑	0.0087	0.0104	1.4400	1.6174
B to Z ↓	0.0064	0.0072	0.9555	1.0235
B to Z ↑	0.0086	0.0097	1.4560	1.6342
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0261	0.0297	0.3555	0.3805
A to Z ↑	0.0211	0.0247	0.4355	0.4950
B to Z ↓	0.0245	0.0279	0.3556	0.3803
B to Z ↑	0.0227	0.0262	0.4347	0.4953
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0350	0.0410	0.4167	0.4493
A to Z ↑	0.0299	0.0357	0.5842	0.6658
B to Z ↓	0.0330	0.0389	0.4165	0.4492
B to Z ↑	0.0311	0.0368	0.5839	0.6655

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X14_P0	1.337e-03	1.000e-20
X14_P4	3.501e-04	1.000e-20
X14_P10	7.940e-05	1.000e-20
X14_P16	3.069e-05	1.000e-20
X33_P0	3.406e-03	1.000e-20
X33_P4	8.869e-04	1.000e-20
X33_P10	2.015e-04	1.000e-20
X33_P16	7.797e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	2.339e-04	1.907e-04	1.728e-04	1.711e-04
B (output stable)	3.864e-04	4.282e-04	4.100e-04	4.113e-04
A to Z	7.927e-03	6.414e-03	5.378e-03	4.990e-03
B to Z	6.745e-03	5.210e-03	4.023e-03	3.457e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	6.500e-05	4.745e-05	4.300e-05	4.077e-05
B (output stable)	7.364e-05	8.336e-05	8.368e-05	8.050e-05
A to Z	1.768e-02	1.645e-02	1.586e-02	1.630e-02
B to Z	1.743e-02	1.617e-02	1.549e-02	1.589e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

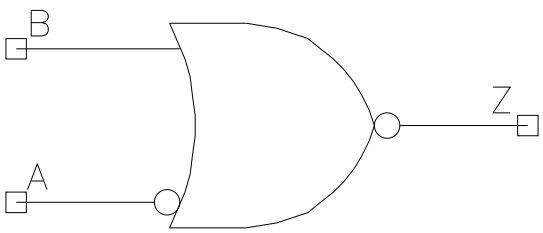
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2A

Cell Description

2 input NOR with A input Inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	1.224	1.4688
X15_P4	1.200	1.224	1.4688
X15_P10	1.200	1.224	1.4688
X15_P16	1.200	1.224	1.4688
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0014	0.0014	0.0015	0.0016
B	0.0009	0.0010	0.0011	0.0012
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0016	0.0017	0.0019	0.0020
B	0.0010	0.0011	0.0011	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0198	0.0226	0.8698	0.9307
A to Z ↑	0.0125	0.0144	0.8700	0.9907
B to Z ↓	0.0200	0.0227	0.8656	0.9263
B to Z ↑	0.0184	0.0211	0.8667	0.9891
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0270	0.0312	1.0196	1.0993
A to Z ↑	0.0174	0.0201	1.1721	1.3376
B to Z ↓	0.0272	0.0315	1.0150	1.0932
B to Z ↑	0.0254	0.0294	1.1696	1.3356
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0165	0.0191	0.4875	0.5228
A to Z ↑	0.0150	0.0167	0.4646	0.5286
B to Z ↓	0.0203	0.0232	0.4877	0.5217
B to Z ↑	0.0206	0.0236	0.4640	0.5279
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0232	0.0268	0.5715	0.6158
A to Z ↑	0.0198	0.0225	0.6242	0.7105
B to Z ↓	0.0280	0.0323	0.5715	0.6153
B to Z ↑	0.0286	0.0328	0.6231	0.7103

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X15_P0	2.080e-03	1.000e-20
X15_P4	5.286e-04	1.000e-20
X15_P10	1.164e-04	1.000e-20
X15_P16	4.415e-05	1.000e-20
X27_P0	3.430e-03	1.000e-20
X27_P4	8.644e-04	1.000e-20
X27_P10	1.884e-04	1.000e-20
X27_P16	7.083e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	9.182e-05	7.795e-05	6.989e-05	6.648e-05
B (output stable)	3.660e-03	2.997e-03	2.540e-03	2.410e-03
A to Z	8.726e-03	7.743e-03	7.241e-03	7.163e-03
B to Z	1.021e-02	9.288e-03	8.862e-03	8.863e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.350e-04	1.130e-04	1.022e-04	9.888e-05
B (output stable)	3.976e-03	3.302e-03	2.907e-03	2.833e-03
A to Z	1.480e-02	1.300e-02	1.219e-02	1.192e-02
B to Z	1.558e-02	1.430e-02	1.398e-02	1.393e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

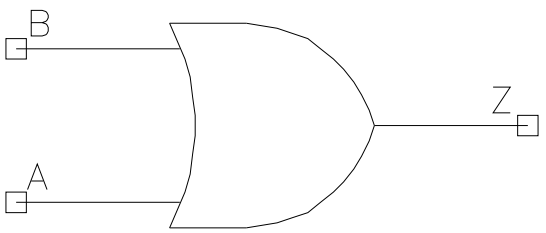
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR2

Cell Description

2 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X20_P0	1.200	1.360	1.6320
X20_P4	1.200	1.360	1.6320
X20_P10	1.200	1.360	1.6320
X20_P16	1.200	1.360	1.6320
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320
X37_P0	1.200	1.632	1.9584
X37_P4	1.200	1.632	1.9584
X37_P10	1.200	1.632	1.9584
X37_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0017	0.0018	0.0020	0.0021
B	0.0016	0.0017	0.0018	0.0020
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0026	0.0027	0.0030	0.0032
B	0.0027	0.0028	0.0031	0.0033
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0018	0.0019	0.0021	0.0022

B	0.0018	0.0019	0.0021	0.0022
	X37_P0	X37_P4	X37_P10	X37_P16
A	0.0026	0.0027	0.0030	0.0032
B	0.0026	0.0028	0.0031	0.0033

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0138	0.0159	0.7910	0.8474
A to Z ↑	0.0125	0.0143	0.9032	1.0299
B to Z ↓	0.0146	0.0166	0.7901	0.8475
B to Z ↑	0.0110	0.0126	0.9021	1.0303
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0191	0.0224	0.9271	0.9996
A to Z ↑	0.0169	0.0192	1.2215	1.3955
B to Z ↓	0.0194	0.0222	0.9274	0.9998
B to Z ↑	0.0149	0.0170	1.2201	1.3939
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0125	0.0146	0.6194	0.6629
A to Z ↑	0.0134	0.0152	0.6295	0.7170
B to Z ↓	0.0135	0.0154	0.6188	0.6630
B to Z ↑	0.0115	0.0130	0.6276	0.7163
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0177	0.0209	0.7246	0.7802
A to Z ↑	0.0177	0.0202	0.8472	0.9666
B to Z ↓	0.0181	0.0208	0.7251	0.7802
B to Z ↑	0.0153	0.0174	0.8458	0.9644
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0170	0.0196	0.3583	0.3839
A to Z ↑	0.0162	0.0182	0.4264	0.4864
B to Z ↓	0.0179	0.0204	0.3580	0.3838
B to Z ↑	0.0143	0.0162	0.4261	0.4852
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0240	0.0282	0.4209	0.4544
A to Z ↑	0.0214	0.0242	0.5764	0.6583
B to Z ↓	0.0243	0.0279	0.4210	0.4540
B to Z ↑	0.0191	0.0216	0.5754	0.6563
	X37_P0	**X37_P4**	**X37_P0**	**X37_P4**
A to Z ↓	0.0153	0.0178	0.3459	0.3706
A to Z ↑	0.0156	0.0176	0.3497	0.3982
B to Z ↓	0.0164	0.0189	0.3452	0.3705
B to Z ↑	0.0138	0.0157	0.3489	0.3975
	X37_P10	**X37_P16**	**X37_P10**	**X37_P16**
A to Z ↓	0.0217	0.0253	0.4064	0.4378
A to Z ↑	0.0206	0.0231	0.4700	0.5356
B to Z ↓	0.0224	0.0256	0.4059	0.4379
B to Z ↑	0.0183	0.0205	0.4692	0.5352

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X15_P0	1.276e-03	1.000e-20

X15_P4	3.401e-04	1.000e-20
X15_P10	8.020e-05	1.000e-20
X15_P16	3.204e-05	1.000e-20
X20_P0	2.189e-03	1.000e-20
X20_P4	5.806e-04	1.000e-20
X20_P10	1.346e-04	1.000e-20
X20_P16	5.283e-05	1.000e-20
X33_P0	2.104e-03	1.000e-20
X33_P4	5.734e-04	1.000e-20
X33_P10	1.377e-04	1.000e-20
X33_P16	5.534e-05	1.000e-20
X37_P0	2.812e-03	1.000e-20
X37_P4	7.515e-04	1.000e-20
X37_P10	1.758e-04	1.000e-20
X37_P16	6.926e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.343e-04	1.099e-04	1.013e-04	1.017e-04
B (output stable)	2.322e-04	2.545e-04	2.559e-04	2.506e-04
A to Z	9.319e-03	8.046e-03	7.368e-03	7.240e-03
B to Z	8.596e-03	7.315e-03	6.538e-03	6.279e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.475e-04	1.960e-04	1.785e-04	1.749e-04
B (output stable)	3.894e-04	4.306e-04	4.110e-04	3.965e-04
A to Z	1.424e-02	1.234e-02	1.127e-02	1.114e-02
B to Z	1.300e-02	1.106e-02	9.848e-03	9.498e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.834e-04	1.481e-04	1.384e-04	1.379e-04
B (output stable)	3.756e-04	4.059e-04	4.092e-04	4.015e-04
A to Z	1.756e-02	1.541e-02	1.433e-02	1.410e-02
B to Z	1.656e-02	1.440e-02	1.319e-02	1.279e-02
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	2.472e-04	1.964e-04	1.804e-04	1.775e-04
B (output stable)	3.899e-04	4.348e-04	4.168e-04	3.980e-04
A to Z	2.076e-02	1.826e-02	1.693e-02	1.654e-02
B to Z	1.945e-02	1.697e-02	1.546e-02	1.488e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

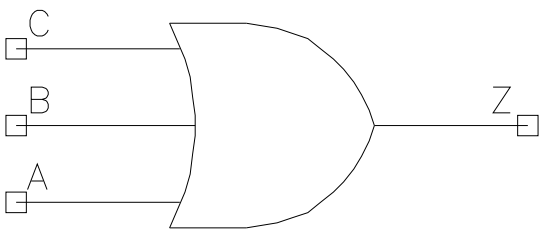
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR3

Cell Description

3 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	1.360	1.6320
X14_P4	1.200	1.360	1.6320
X14_P10	1.200	1.360	1.6320
X14_P16	1.200	1.360	1.6320
X20_P0	1.200	1.632	1.9584
X20_P4	1.200	1.632	1.9584
X20_P10	1.200	1.632	1.9584
X20_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0010	0.0010	0.0011	0.0012
B	0.0009	0.0010	0.0011	0.0012
C	0.0009	0.0010	0.0011	0.0012
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0009	0.0010	0.0011	0.0012
B	0.0009	0.0010	0.0011	0.0012
C	0.0009	0.0010	0.0011	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	X14_P4	X14_P0	X14_P4
A to Z ↓	0.0286	0.0327	0.8674	0.9290
A to Z ↑	0.0248	0.0284	0.9113	1.0397

B to Z ↓	0.0275	0.0317	0.8674	0.9295
B to Z ↑	0.0266	0.0304	0.9121	1.0406
C to Z ↓	0.0268	0.0306	0.8667	0.9293
C to Z ↑	0.0229	0.0261	0.9124	1.0381
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0394	0.0461	1.0169	1.0971
A to Z ↑	0.0340	0.0395	1.2275	1.4006
B to Z ↓	0.0386	0.0456	1.0175	1.0974
B to Z ↑	0.0361	0.0418	1.2272	1.4013
C to Z ↓	0.0368	0.0430	1.0166	1.0966
C to Z ↑	0.0311	0.0361	1.2266	1.4002
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0286	0.0329	0.6388	0.6833
A to Z ↑	0.0265	0.0306	0.6460	0.7339
B to Z ↓	0.0274	0.0318	0.6388	0.6835
B to Z ↑	0.0280	0.0322	0.6461	0.7344
C to Z ↓	0.0258	0.0298	0.6389	0.6841
C to Z ↑	0.0254	0.0291	0.6453	0.7338
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0396	0.0462	0.7478	0.8065
A to Z ↑	0.0371	0.0434	0.8657	0.9855
B to Z ↓	0.0388	0.0457	0.7481	0.8061
B to Z ↑	0.0389	0.0453	0.8653	0.9862
C to Z ↓	0.0360	0.0421	0.7483	0.8062
C to Z ↑	0.0349	0.0407	0.8642	0.9855

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X14_P0	1.890e-03	1.000e-20
X14_P4	5.010e-04	1.000e-20
X14_P10	1.179e-04	1.000e-20
X14_P16	4.709e-05	1.000e-20
X20_P0	2.193e-03	1.000e-20
X20_P4	5.863e-04	1.000e-20
X20_P10	1.389e-04	1.000e-20
X20_P16	5.556e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	1.112e-03	9.737e-04	8.861e-04	8.611e-04
B (output stable)	1.206e-03	1.057e-03	9.851e-04	9.816e-04
C (output stable)	3.194e-03	2.621e-03	2.224e-03	2.072e-03
A to Z	1.105e-02	1.036e-02	1.012e-02	1.031e-02
B to Z	1.134e-02	1.067e-02	1.048e-02	1.073e-02
C to Z	1.108e-02	1.026e-02	9.914e-03	1.004e-02
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	1.099e-03	9.531e-04	8.614e-04	8.335e-04
B (output stable)	1.189e-03	1.034e-03	9.556e-04	9.460e-04
C (output stable)	3.093e-03	2.509e-03	2.100e-03	1.936e-03
A to Z	1.323e-02	1.253e-02	1.234e-02	1.256e-02
B to Z	1.353e-02	1.283e-02	1.269e-02	1.296e-02

C to Z	1.317e-02	1.235e-02	1.206e-02	1.222e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

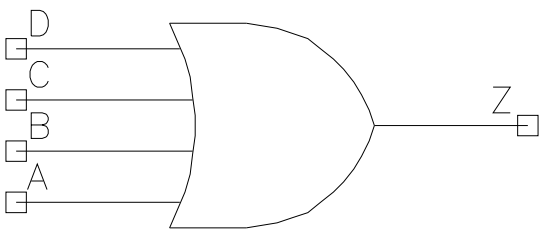
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR4

Cell Description

4 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X20_P4	1.200	2.176	2.6112
X20_P10	1.200	2.176	2.6112
X20_P16	1.200	2.176	2.6112
X27_P0	1.200	2.312	2.7744
X27_P4	1.200	2.312	2.7744
X27_P10	1.200	2.312	2.7744
X27_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0014	0.0014	0.0016	0.0017
B	0.0015	0.0016	0.0017	0.0018
C	0.0014	0.0015	0.0016	0.0017
D	0.0015	0.0016	0.0018	0.0019
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0014	0.0015	0.0016	0.0016
B	0.0015	0.0016	0.0017	0.0018
C	0.0014	0.0015	0.0016	0.0017
D	0.0016	0.0017	0.0018	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0182	0.0212	0.5994	0.6463
A to Z ↑	0.0214	0.0243	0.7443	0.8491
B to Z ↓	0.0178	0.0208	0.5991	0.6462
B to Z ↑	0.0201	0.0227	0.7427	0.8485
C to Z ↓	0.0177	0.0204	0.5963	0.6431
C to Z ↑	0.0207	0.0232	0.7357	0.8417
D to Z ↓	0.0177	0.0204	0.5958	0.6429
D to Z ↑	0.0194	0.0216	0.7356	0.8416
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0256	0.0302	0.7145	0.7769
A to Z ↑	0.0284	0.0329	1.0037	1.1469
B to Z ↓	0.0247	0.0289	0.7144	0.7770
B to Z ↑	0.0263	0.0303	1.0032	1.1460
C to Z ↓	0.0248	0.0285	0.7115	0.7732
C to Z ↑	0.0271	0.0304	0.9978	1.1410
D to Z ↓	0.0244	0.0277	0.7113	0.7729
D to Z ↑	0.0251	0.0280	0.9968	1.1386
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0201	0.0234	0.4936	0.5323
A to Z ↑	0.0229	0.0260	0.5562	0.6355
B to Z ↓	0.0199	0.0230	0.4933	0.5322
B to Z ↑	0.0217	0.0245	0.5562	0.6354
C to Z ↓	0.0189	0.0217	0.4908	0.5293
C to Z ↑	0.0212	0.0238	0.5512	0.6296
D to Z ↓	0.0190	0.0217	0.4905	0.5288
D to Z ↑	0.0195	0.0218	0.5507	0.6296
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0283	0.0331	0.5888	0.6410
A to Z ↑	0.0306	0.0350	0.7514	0.8589
B to Z ↓	0.0277	0.0321	0.5890	0.6411
B to Z ↑	0.0287	0.0327	0.7514	0.8585
C to Z ↓	0.0263	0.0306	0.5856	0.6369
C to Z ↑	0.0279	0.0317	0.7470	0.8550
D to Z ↓	0.0259	0.0300	0.5853	0.6367
D to Z ↑	0.0254	0.0288	0.7456	0.8531

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X20_P0	1.817e-03	1.000e-20
X20_P4	4.940e-04	1.000e-20
X20_P10	1.207e-04	1.000e-20
X20_P16	5.007e-05	1.000e-20
X27_P0	1.956e-03	1.000e-20
X27_P4	5.331e-04	1.000e-20
X27_P10	1.310e-04	1.000e-20
X27_P16	5.468e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.755e-03	2.614e-03	2.600e-03	2.739e-03

B (output stable)	2.638e-03	2.461e-03	2.368e-03	2.442e-03
C (output stable)	2.697e-03	2.487e-03	2.424e-03	2.478e-03
D (output stable)	2.559e-03	2.315e-03	2.174e-03	2.169e-03
A to Z	1.408e-02	1.312e-02	1.274e-02	1.310e-02
B to Z	1.371e-02	1.263e-02	1.209e-02	1.232e-02
C to Z	1.389e-02	1.253e-02	1.192e-02	1.168e-02
D to Z	1.347e-02	1.200e-02	1.123e-02	1.088e-02
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	3.069e-03	2.971e-03	3.038e-03	3.188e-03
B (output stable)	2.946e-03	2.808e-03	2.802e-03	2.893e-03
C (output stable)	2.830e-03	2.624e-03	2.580e-03	2.648e-03
D (output stable)	2.708e-03	2.465e-03	2.339e-03	2.338e-03
A to Z	1.751e-02	1.620e-02	1.566e-02	1.591e-02
B to Z	1.708e-02	1.566e-02	1.497e-02	1.511e-02
C to Z	1.614e-02	1.452e-02	1.370e-02	1.369e-02
D to Z	1.571e-02	1.397e-02	1.302e-02	1.289e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

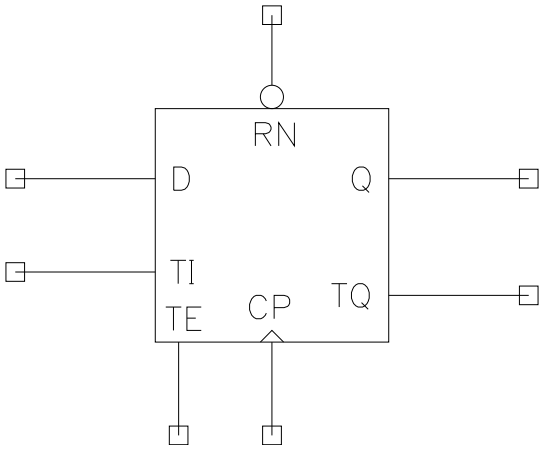
Pin Cycle (vdds)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNSDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.080	4.8960
X15_P4	1.200	4.080	4.8960
X15_P10	1.200	4.080	4.8960
X15_P16	1.200	4.080	4.8960

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0008	0.0009	0.0010	0.0010
D	0.0007	0.0007	0.0008	0.0008
RN	0.0009	0.0009	0.0010	0.0010

TE	0.0010	0.0011	0.0012	0.0012
TI	0.0003	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	X15_P4	X15_P0	X15_P4
CP to Q ↓	0.0445	0.0508	0.8770	0.9383
CP to Q ↑	0.0470	0.0535	0.8531	0.9720
CP to TQ ↓	0.0451	0.0516	4.0510	4.3129
CP to TQ ↑	0.0503	0.0573	7.3990	8.3454
RN to Q ↓	0.0464	0.0538	0.8761	0.9377
RN to TQ ↓	0.0469	0.0545	4.0519	4.3140
	X15_P10	X15_P16	X15_P10	X15_P16
CP to Q ↓	0.0608	0.0704	1.0264	1.1032
CP to Q ↑	0.0638	0.0737	1.1508	1.3135
CP to TQ ↓	0.0618	0.0717	4.6793	4.9980
CP to TQ ↑	0.0683	0.0790	9.8157	11.2193
RN to Q ↓	0.0651	0.0762	1.0262	1.1039
RN to TQ ↓	0.0661	0.0775	4.6794	4.9961

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.0369	0.0461	0.0562	0.0696
CP ↑	min_pulse_width to CP	0.0265	0.0299	0.0345	0.0390
D ↓	hold_rising to CP	0.0048	0.0052	0.0003	-0.0050
D ↑	hold_rising to CP	0.0005	-0.0049	-0.0098	-0.0094
D ↓	setup_rising to CP	0.0251	0.0300	0.0344	0.0445
D ↑	setup_rising to CP	0.0272	0.0298	0.0346	0.0395
RN ↓	min_pulse_width to RN	0.0376	0.0447	0.0518	0.0588
RN ↑	recovery_rising to CP	0.0054	0.0081	0.0103	0.0151
RN ↑	removal_rising to CP	0.0024	-0.0008	-0.0030	-0.0030
TE ↓	hold_rising to CP	0.0096	0.0074	0.0025	-0.0024
TE ↑	hold_rising to CP	-0.0071	-0.0125	-0.0174	-0.0222
TE ↓	setup_rising to CP	0.0386	0.0435	0.0511	0.0586
TE ↑	setup_rising to CP	0.0445	0.0569	0.0715	0.0884
TI ↓	hold_rising to CP	-0.0169	-0.0215	-0.0329	-0.0439
TI ↑	hold_rising to CP	-0.0079	-0.0085	-0.0147	-0.0202
TI ↓	setup_rising to CP	0.0465	0.0562	0.0724	0.0870
TI ↑	setup_rising to CP	0.0335	0.0391	0.0453	0.0492

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X15_P0	3.347e-03	1.000e-20
X15_P4	8.667e-04	1.000e-20
X15_P10	2.014e-04	1.000e-20
X15_P16	8.082e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

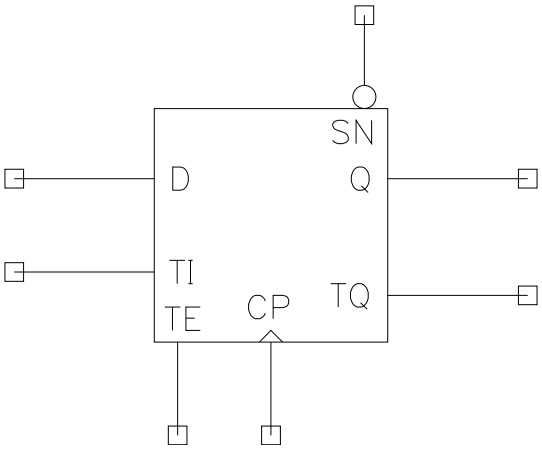
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	1.494e-02	1.441e-02	1.409e-02	1.396e-02
Clock 100Mhz Data 25Mhz	1.551e-02	1.496e-02	1.473e-02	1.476e-02
Clock 100Mhz Data 50Mhz	1.608e-02	1.551e-02	1.537e-02	1.555e-02
Clock = 0 Data 100Mhz	6.252e-03	6.178e-03	6.183e-03	6.238e-03
Clock = 1 Data 100Mhz	6.091e-05	5.665e-05	5.373e-05	5.190e-05

CNSDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.216	5.0592
X15_P4	1.200	4.216	5.0592
X15_P10	1.200	4.216	5.0592
X15_P16	1.200	4.216	5.0592

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0008	0.0009	0.0010	0.0010
D	0.0004	0.0005	0.0005	0.0005
SN	0.0016	0.0016	0.0018	0.0019

TE	0.0010	0.0011	0.0012	0.0013
TI	0.0004	0.0004	0.0005	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	X15_P4	X15_P0	X15_P4
CP to Q ↓	0.0447	0.0509	0.8777	0.9394
CP to Q ↑	0.0472	0.0538	0.8522	0.9735
CP to TQ ↓	0.0452	0.0517	4.0598	4.3220
CP to TQ ↑	0.0506	0.0577	7.3993	8.3517
SN to Q ↑	0.0381	0.0438	0.8520	0.9719
SN to TQ ↑	0.0415	0.0477	7.3983	8.3485
	X15_P10	X15_P16	X15_P10	X15_P16
CP to Q ↓	0.0607	0.0703	1.0256	1.1042
CP to Q ↑	0.0641	0.0741	1.1512	1.3129
CP to TQ ↓	0.0618	0.0717	4.6893	5.0066
CP to TQ ↑	0.0688	0.0796	9.8186	11.2245
SN to Q ↑	0.0528	0.0615	1.1512	1.3131
SN to TQ ↑	0.0575	0.0670	9.8149	11.2200

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.0417	0.0510	0.0626	0.0784
CP ↑	min_pulse_width to CP	0.0264	0.0311	0.0344	0.0390
D ↓	hold_rising to CP	0.0052	-0.0001	-0.0050	-0.0104
D ↑	hold_rising to CP	0.0026	0.0005	-0.0049	-0.0098
D ↓	setup_rising to CP	0.0300	0.0348	0.0419	0.0490
D ↑	setup_rising to CP	0.0244	0.0239	0.0288	0.0346
SN ↓	min_pulse_width to SN	0.0305	0.0327	0.0376	0.0425
SN ↑	recovery_rising to CP	-0.0043	-0.0017	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0184	0.0237	0.0260	0.0281
TE ↓	hold_rising to CP	0.0070	0.0021	-0.0028	-0.0050
TE ↑	hold_rising to CP	-0.0044	-0.0072	-0.0120	-0.0169
TE ↓	setup_rising to CP	0.0365	0.0414	0.0489	0.0528
TE ↑	setup_rising to CP	0.0515	0.0645	0.0813	0.0982
TI ↓	hold_rising to CP	-0.0215	-0.0315	-0.0426	-0.0524
TI ↑	hold_rising to CP	-0.0021	-0.0079	-0.0141	-0.0147
TI ↓	setup_rising to CP	0.0565	0.0619	0.0806	0.0968
TI ↑	setup_rising to CP	0.0286	0.0335	0.0404	0.0453

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X15_P0	3.138e-03	1.000e-20
X15_P4	8.212e-04	1.000e-20
X15_P10	1.939e-04	1.000e-20
X15_P16	7.886e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

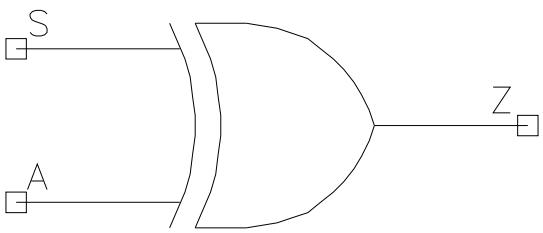
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	1.505e-02	1.452e-02	1.420e-02	1.407e-02
Clock 100Mhz Data 25Mhz	1.567e-02	1.512e-02	1.489e-02	1.491e-02
Clock 100Mhz Data 50Mhz	1.629e-02	1.572e-02	1.557e-02	1.575e-02
Clock = 0 Data 100Mhz	6.373e-03	6.281e-03	6.274e-03	6.318e-03
Clock = 1 Data 100Mhz	6.500e-05	5.869e-05	5.501e-05	5.284e-05

CNXOR2

Cell Description

2 input Exclusive OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X16_P0	1.200	1.360	1.6320
X16_P4	1.200	1.360	1.6320
X16_P10	1.200	1.360	1.6320
X16_P16	1.200	1.360	1.6320
X27_P0	1.200	2.040	2.4480
X27_P4	1.200	2.040	2.4480
X27_P10	1.200	2.040	2.4480
X27_P16	1.200	2.040	2.4480

Truth Table

A	S	Z
1	S	!S
0	S	S

Pin Capacitance

Pin	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0012	0.0012	0.0013	0.0014
S	0.0016	0.0017	0.0019	0.0020
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0017	0.0018	0.0020	0.0021
S	0.0023	0.0024	0.0026	0.0027

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0228	0.0262	0.7397	0.7924
A to Z ↑	0.0222	0.0251	0.8759	0.9997
S to Z ↓	0.0179	0.0204	0.7374	0.7901
S to Z ↑	0.0175	0.0200	0.8749	0.9988
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0312	0.0364	0.8684	0.9389

A to Z ↑	0.0295	0.0339	1.1840	1.3536
S to Z ↓	0.0239	0.0276	0.8658	0.9363
S to Z ↑	0.0235	0.0271	1.1821	1.3527
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0238	0.0272	0.4878	0.5229
A to Z ↑	0.0239	0.0271	0.4703	0.5352
S to Z ↓	0.0197	0.0224	0.4872	0.5224
S to Z ↑	0.0197	0.0224	0.4700	0.5353
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0326	0.0376	0.5738	0.6195
A to Z ↑	0.0322	0.0367	0.6326	0.7216
S to Z ↓	0.0266	0.0305	0.5733	0.6194
S to Z ↑	0.0264	0.0302	0.6322	0.7218

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X16_P0	2.993e-03	1.000e-20
X16_P4	7.741e-04	1.000e-20
X16_P10	1.749e-04	1.000e-20
X16_P16	6.721e-05	1.000e-20
X27_P0	4.932e-03	1.000e-20
X27_P4	1.258e-03	1.000e-20
X27_P10	2.786e-04	1.000e-20
X27_P16	1.052e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	1.307e-02	1.183e-02	1.104e-02	1.102e-02
S to Z	1.205e-02	1.053e-02	9.508e-03	9.347e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	2.385e-02	2.146e-02	2.015e-02	1.977e-02
S to Z	1.955e-02	1.716e-02	1.570e-02	1.526e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

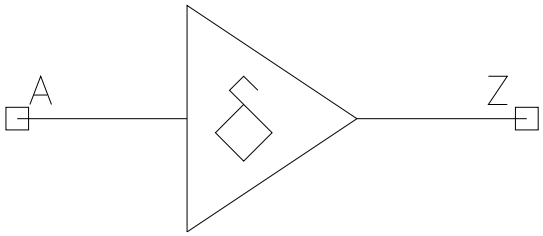
Pin Cycle (vdds)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DLYHF

Cell Description

Delay cell for Hold Time Fixing

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-DLYHFM4X7_P0	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X7_P4	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X7_P10	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X7_P16	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X15_P0	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM4X15_P4	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM4X15_P10	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM4X15_P16	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM8X7_P0	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X7_P4	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X7_P10	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X7_P16	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X15_P0	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X15_P4	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X15_P10	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X15_P16	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X54_P0	1.200	4.216	5.0592

C12T28SOI_LL_-DLYHFM8X54_P4	1.200	4.216	5.0592
C12T28SOI_LL_-DLYHFM8X54_P10	1.200	4.216	5.0592
C12T28SOI_LL_-DLYHFM8X54_P16	1.200	4.216	5.0592

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C12T28SOI_LL_-DLYHFM4X7_P0	C12T28SOI_LL_-DLYHFM4X7_P4	C12T28SOI_LL_-DLYHFM4X7_P10	C12T28SOI_LL_-DLYHFM4X7_P16
A	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LL_-DLYHFM4X15_P0	C12T28SOI_LL_-DLYHFM4X15_P4	C12T28SOI_LL_-DLYHFM4X15_P10	C12T28SOI_LL_-DLYHFM4X15_P16
A	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LL_-DLYHFM8X7_P0	C12T28SOI_LL_-DLYHFM8X7_P4	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A	0.0008	0.0009	0.0009	0.0009
	C12T28SOI_LL_-DLYHFM8X15_P0	C12T28SOI_LL_-DLYHFM8X15_P4	C12T28SOI_LL_-DLYHFM8X15_P10	C12T28SOI_LL_-DLYHFM8X15_P16
A	0.0008	0.0008	0.0009	0.0009
	C12T28SOI_LL_-DLYHFM8X54_P0	C12T28SOI_LL_-DLYHFM8X54_P4	C12T28SOI_LL_-DLYHFM8X54_P10	C12T28SOI_LL_-DLYHFM8X54_P16
A	0.0008	0.0008	0.0009	0.0009

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-DLYHFM4X7_P0	**C12T28SOI_LL_-DLYHFM4X7_P4**	**C12T28SOI_LL_-DLYHFM4X7_P0**	**C12T28SOI_LL_-DLYHFM4X7_P4**
A to Z ↓	0.0580	0.0667	1.6758	1.8042
A to Z ↑	0.0566	0.0652	1.9973	2.2801
	C12T28SOI_LL_-DLYHFM4X7_P10	**C12T28SOI_LL_-DLYHFM4X7_P16**	**C12T28SOI_LL_-DLYHFM4X7_P10**	**C12T28SOI_LL_-DLYHFM4X7_P16**
A to Z ↓	0.0806	0.0944	1.9846	2.1493
A to Z ↑	0.0788	0.0924	2.6957	3.0826
	C12T28SOI_LL_-DLYHFM4X15_P0	**C12T28SOI_LL_-DLYHFM4X15_P4**	**C12T28SOI_LL_-DLYHFM4X15_P0**	**C12T28SOI_LL_-DLYHFM4X15_P4**
A to Z ↓	0.0634	0.0731	0.8069	0.8698
A to Z ↑	0.0634	0.0732	0.9233	1.0555
	C12T28SOI_LL_-DLYHFM4X15_P10	**C12T28SOI_LL_-DLYHFM4X15_P16**	**C12T28SOI_LL_-DLYHFM4X15_P10**	**C12T28SOI_LL_-DLYHFM4X15_P16**
A to Z ↓	0.0887	0.1045	0.9629	1.0474
A to Z ↑	0.0887	0.1042	1.2511	1.4305
	C12T28SOI_LL_-DLYHFM8X7_P0	**C12T28SOI_LL_-DLYHFM8X7_P4**	**C12T28SOI_LL_-DLYHFM8X7_P0**	**C12T28SOI_LL_-DLYHFM8X7_P4**
A to Z ↓	0.1009	0.1166	1.6785	1.8071
A to Z ↑	0.0950	0.1098	1.8536	2.1155

	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A to Z ↓	0.1414	0.1663	1.9919	2.1612
A to Z ↑	0.1333	0.1567	2.5024	2.8566
	C12T28SOI_LL_-DLYHFM8X15_P0	**C12T28SOI_LL_-DLYHFM8X15_P4**	**C12T28SOI_LL_-DLYHFM8X15_P0**	**C12T28SOI_LL_-DLYHFM8X15_P4**
A to Z ↓	0.1055	0.1221	0.8045	0.8697
A to Z ↑	0.1019	0.1179	0.9251	1.0571
	C12T28SOI_LL_-DLYHFM8X15_P10	**C12T28SOI_LL_-DLYHFM8X15_P16**	**C12T28SOI_LL_-DLYHFM8X15_P10**	**C12T28SOI_LL_-DLYHFM8X15_P16**
A to Z ↓	0.1487	0.1754	0.9627	1.0495
A to Z ↑	0.1433	0.1686	1.2529	1.4337
	C12T28SOI_LL_-DLYHFM8X54_P0	**C12T28SOI_LL_-DLYHFM8X54_P4**	**C12T28SOI_LL_-DLYHFM8X54_P0**	**C12T28SOI_LL_-DLYHFM8X54_P4**
A to Z ↓	0.1426	0.1658	0.2180	0.2340
A to Z ↑	0.1292	0.1508	0.2678	0.3039
	C12T28SOI_LL_-DLYHFM8X54_P10	**C12T28SOI_LL_-DLYHFM8X54_P16**	**C12T28SOI_LL_-DLYHFM8X54_P10**	**C12T28SOI_LL_-DLYHFM8X54_P16**
A to Z ↓	0.2022	0.2399	0.2566	0.2771
A to Z ↑	0.1849	0.2203	0.3582	0.4085

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C12T28SOI_LL_DLYHFM4X7_P0	4.488e-04	1.000e-20
C12T28SOI_LL_DLYHFM4X7_P4	1.203e-04	1.000e-20
C12T28SOI_LL_DLYHFM4X7_P10	2.966e-05	1.000e-20
C12T28SOI_LL_DLYHFM4X7_P16	1.284e-05	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P0	9.441e-04	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P4	2.481e-04	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P10	5.816e-05	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P16	2.369e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P0	5.005e-04	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P4	1.365e-04	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P10	3.469e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P16	1.560e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P0	9.678e-04	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P4	2.565e-04	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P10	6.147e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P16	2.583e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P0	3.507e-03	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P4	9.445e-04	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P10	2.288e-04	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P16	9.582e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C12T28SOI_LL_-DLYHFM4X7_P0	C12T28SOI_LL_-DLYHFM4X7_P4	C12T28SOI_LL_-DLYHFM4X7_P10	C12T28SOI_LL_-DLYHFM4X7_P16
A to Z	6.892e-03	6.692e-03	6.720e-03	6.907e-03
	C12T28SOI_LL_-DLYHFM4X15_P0	C12T28SOI_LL_-DLYHFM4X15_P4	C12T28SOI_LL_-DLYHFM4X15_P10	C12T28SOI_LL_-DLYHFM4X15_P16
A to Z	1.227e-02	1.147e-02	1.111e-02	1.118e-02

	C12T28SOI_LL_-DLYHFM8X7_P0	C12T28SOI_LL_-DLYHFM8X7_P4	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A to Z	1.037e-02	1.022e-02	1.038e-02	1.072e-02
	C12T28SOI_LL_-DLYHFM8X15_P0	C12T28SOI_LL_-DLYHFM8X15_P4	C12T28SOI_LL_-DLYHFM8X15_P10	C12T28SOI_LL_-DLYHFM8X15_P16
A to Z	1.570e-02	1.498e-02	1.475e-02	1.496e-02
	C12T28SOI_LL_-DLYHFM8X54_P0	C12T28SOI_LL_-DLYHFM8X54_P4	C12T28SOI_LL_-DLYHFM8X54_P10	C12T28SOI_LL_-DLYHFM8X54_P16
A to Z	4.620e-02	4.510e-02	4.534e-02	4.710e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

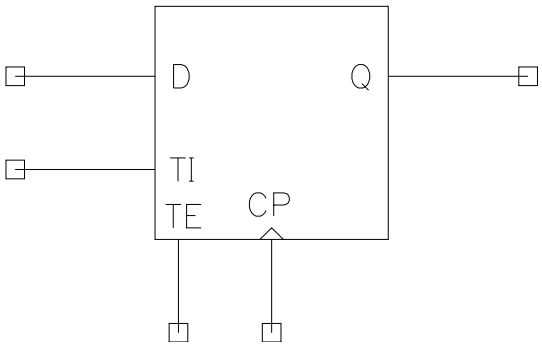
Pin Cycle (vdds)	C12T28SOI_LL_-DLYHFM4X7_P0	C12T28SOI_LL_-DLYHFM4X7_P4	C12T28SOI_LL_-DLYHFM4X7_P10	C12T28SOI_LL_-DLYHFM4X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM4X15_P0	C12T28SOI_LL_-DLYHFM4X15_P4	C12T28SOI_LL_-DLYHFM4X15_P10	C12T28SOI_LL_-DLYHFM4X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM8X7_P0	C12T28SOI_LL_-DLYHFM8X7_P4	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM8X15_P0	C12T28SOI_LL_-DLYHFM8X15_P4	C12T28SOI_LL_-DLYHFM8X15_P10	C12T28SOI_LL_-DLYHFM8X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM8X54_P0	C12T28SOI_LL_-DLYHFM8X54_P4	C12T28SOI_LL_-DLYHFM8X54_P10	C12T28SOI_LL_-DLYHFM8X54_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFSYNCPQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.400	8.1600
X8_P4	2.400	3.400	8.1600
X8_P10	2.400	3.400	8.1600
X8_P16	2.400	3.400	8.1600

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0009	0.0010	0.0011	0.0011
D	0.0007	0.0007	0.0008	0.0008
TE	0.0011	0.0011	0.0012	0.0013
TI	0.0003	0.0003	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X8_P4	X8_P0	X8_P4
CP to Q ↓	0.0713	0.0826	1.3732	1.4729
CP to Q ↑	0.0888	0.1015	1.7048	1.9495

	X8_P10	X8_P16	X8_P10	X8_P16
CP to Q ↓	0.1006	0.1182	1.6146	1.7410
CP to Q ↑	0.1224	0.1436	2.3077	2.6414

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.0913	0.1141	0.1440	0.1729
CP ↑	min_pulse_width to CP	0.0471	0.0552	0.0644	0.0738
D ↓	hold_rising to CP	-0.0137	-0.0245	-0.0343	-0.0440
D ↑	hold_rising to CP	-0.0067	-0.0121	-0.0169	-0.0244
D ↓	setup_rising to CP	0.0493	0.0613	0.0786	0.0932
D ↑	setup_rising to CP	0.0341	0.0369	0.0444	0.0493
TE ↓	hold_rising to CP	-0.0125	-0.0196	-0.0294	-0.0392
TE ↑	hold_rising to CP	-0.0316	-0.0364	-0.0434	-0.0537
TE ↓	setup_rising to CP	0.0515	0.0587	0.0738	0.0886
TE ↑	setup_rising to CP	0.0960	0.1204	0.1519	0.1812
TI ↓	hold_rising to CP	-0.0608	-0.0752	-0.0963	-0.1208
TI ↑	hold_rising to CP	-0.0336	-0.0400	-0.0454	-0.0557
TI ↓	setup_rising to CP	0.0955	0.1163	0.1455	0.1764
TI ↑	setup_rising to CP	0.0592	0.0639	0.0759	0.0856

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	3.987e-03	1.000e-20
X8_P4	1.050e-03	1.000e-20
X8_P10	2.506e-04	1.000e-20
X8_P16	1.036e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

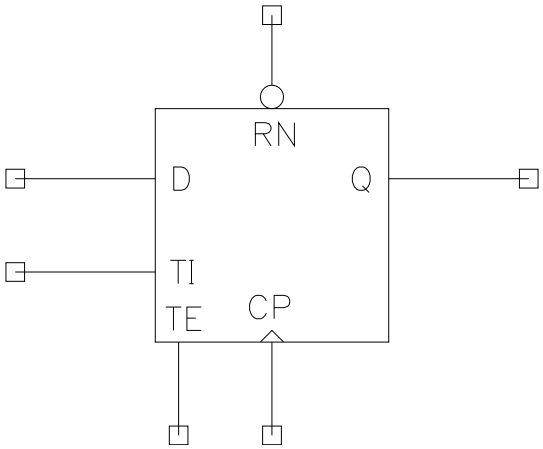
Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	2.625e-02	2.625e-02	2.661e-02	2.718e-02
Clock 100Mhz Data 25Mhz	2.884e-02	2.835e-02	2.850e-02	2.900e-02
Clock 100Mhz Data 50Mhz	3.143e-02	3.046e-02	3.039e-02	3.083e-02
Clock = 0 Data 100Mhz	1.765e-02	1.698e-02	1.651e-02	1.628e-02
Clock = 1 Data 100Mhz	5.250e-05	4.818e-05	4.458e-05	4.248e-05

SDFSYNCPRQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0009	0.0010	0.0011	0.0011
D	0.0007	0.0008	0.0008	0.0009
RN	0.0020	0.0021	0.0023	0.0025
TE	0.0011	0.0011	0.0012	0.0013
TI	0.0003	0.0003	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
CP to Q ↓	0.0779	0.0903	1.3761	1.4779
CP to Q ↑	0.0893	0.1023	1.6931	1.9387
RN to Q ↓	0.0884	0.1021	1.3774	1.4788
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
CP to Q ↓	0.1095	0.1287	1.6204	1.7481
CP to Q ↑	0.1235	0.1449	2.3001	2.6300
RN to Q ↓	0.1242	0.1469	1.6214	1.7521

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.0889	0.1101	0.1406	0.1699
CP ↑	min_pulse_width to CP	0.0470	0.0551	0.0643	0.0736
D ↓	hold_rising to CP	-0.0147	-0.0192	-0.0294	-0.0392
D ↑	hold_rising to CP	-0.0093	-0.0121	-0.0196	-0.0244
D ↓	setup_rising to CP	0.0493	0.0591	0.0737	0.0883
D ↑	setup_rising to CP	0.0373	0.0390	0.0444	0.0488
RN ↓	min_pulse_width to RN	0.0708	0.0828	0.1001	0.1147
RN ↑	recovery_rising to CP	0.0080	0.0081	0.0103	0.0103
RN ↑	removal_rising to CP	-0.0030	-0.0030	-0.0056	-0.0055
TE ↓	hold_rising to CP	-0.0098	-0.0174	-0.0272	-0.0343
TE ↑	hold_rising to CP	-0.0337	-0.0391	-0.0462	-0.0586
TE ↓	setup_rising to CP	0.0506	0.0560	0.0743	0.0835
TE ↑	setup_rising to CP	0.0911	0.1155	0.1470	0.1763
TI ↓	hold_rising to CP	-0.0559	-0.0719	-0.0955	-0.1172
TI ↑	hold_rising to CP	-0.0344	-0.0397	-0.0495	-0.0608
TI ↓	setup_rising to CP	0.0906	0.1114	0.1449	0.1699
TI ↑	setup_rising to CP	0.0632	0.0697	0.0752	0.0872

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	4.160e-03	1.000e-20
X8_P4	1.092e-03	1.000e-20
X8_P10	2.620e-04	1.000e-20
X8_P16	1.100e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	2.719e-02	2.721e-02	2.762e-02	2.823e-02

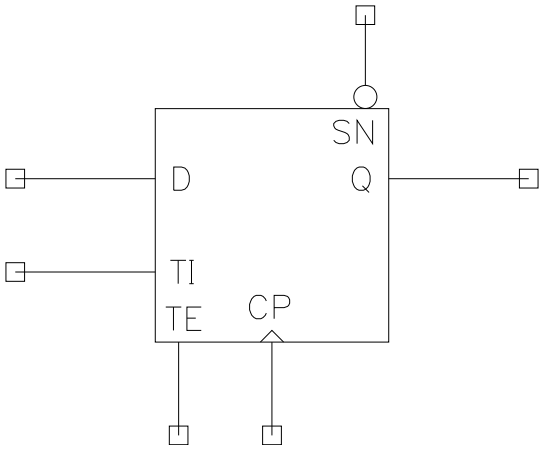
Clock 100Mhz Data 25Mhz	2.946e-02	2.904e-02	2.925e-02	2.983e-02
Clock 100Mhz Data 50Mhz	3.174e-02	3.087e-02	3.089e-02	3.142e-02
Clock = 0 Data 100Mhz	1.678e-02	1.622e-02	1.585e-02	1.570e-02
Clock = 1 Data 100Mhz	4.841e-05	4.434e-05	4.210e-05	4.070e-05

SDFSYNCPSQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0009	0.0010	0.0011	0.0011
D	0.0005	0.0005	0.0005	0.0006
SN	0.0019	0.0020	0.0022	0.0023
TE	0.0011	0.0011	0.0012	0.0013
TI	0.0004	0.0004	0.0004	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
CP to Q ↓	0.0614	0.0709	1.5728	1.7181
CP to Q ↑	0.0779	0.0890	1.8163	2.0817
SN to Q ↑	0.0728	0.0842	1.7450	2.0032
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
CP to Q ↓	0.0853	0.0992	1.9305	2.1309
CP to Q ↑	0.1073	0.1258	2.4770	2.8364
SN to Q ↑	0.1024	0.1207	2.3825	2.7291

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.0865	0.1053	0.1346	0.1635
CP ↑	min_pulse_width to CP	0.0518	0.0565	0.0692	0.0785
D ↓	hold_rising to CP	-0.0098	-0.0143	-0.0218	-0.0316
D ↑	hold_rising to CP	-0.0088	-0.0147	-0.0195	-0.0244
D ↓	setup_rising to CP	0.0445	0.0542	0.0688	0.0840
D ↑	setup_rising to CP	0.0337	0.0395	0.0440	0.0515
SN ↓	min_pulse_width to SN	0.0913	0.1011	0.1206	0.1401
SN ↑	recovery_rising to CP	-0.0088	-0.0088	-0.0066	-0.0066
SN ↑	removal_rising to CP	0.0332	0.0350	0.0426	0.0449
TE ↓	hold_rising to CP	-0.0076	-0.0125	-0.0196	-0.0241
TE ↑	hold_rising to CP	-0.0332	-0.0381	-0.0488	-0.0586
TE ↓	setup_rising to CP	0.0511	0.0560	0.0657	0.0808
TE ↑	setup_rising to CP	0.0889	0.1106	0.1399	0.1714
TI ↓	hold_rising to CP	-0.0510	-0.0655	-0.0863	-0.1074
TI ↑	hold_rising to CP	-0.0341	-0.0406	-0.0508	-0.0621
TI ↓	setup_rising to CP	0.0855	0.1065	0.1373	0.1666
TI ↑	setup_rising to CP	0.0648	0.0710	0.0808	0.0918

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	3.530e-03	1.000e-20
X8_P4	9.545e-04	1.000e-20
X8_P10	2.375e-04	1.000e-20
X8_P16	1.023e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	2.682e-02	2.684e-02	2.724e-02	2.785e-02

Clock 100Mhz Data 25Mhz	2.942e-02	2.882e-02	2.887e-02	2.936e-02
Clock 100Mhz Data 50Mhz	3.201e-02	3.080e-02	3.051e-02	3.087e-02
Clock = 0 Data 100Mhz	1.640e-02	1.590e-02	1.558e-02	1.547e-02
Clock = 1 Data 100Mhz	6.500e-05	5.952e-05	5.598e-05	5.377e-05

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