C28SOI_SC_12_CORE_LL

User Manual

12 track Standard Cell Library comprising commonly used booleans and sequential cells

Overview

Features

- The C28SOI_SC_12_CORE_LL Standard Cell library contains 383 cells.

Application

- Design needs in CMOS28FDSOI platform IPs.

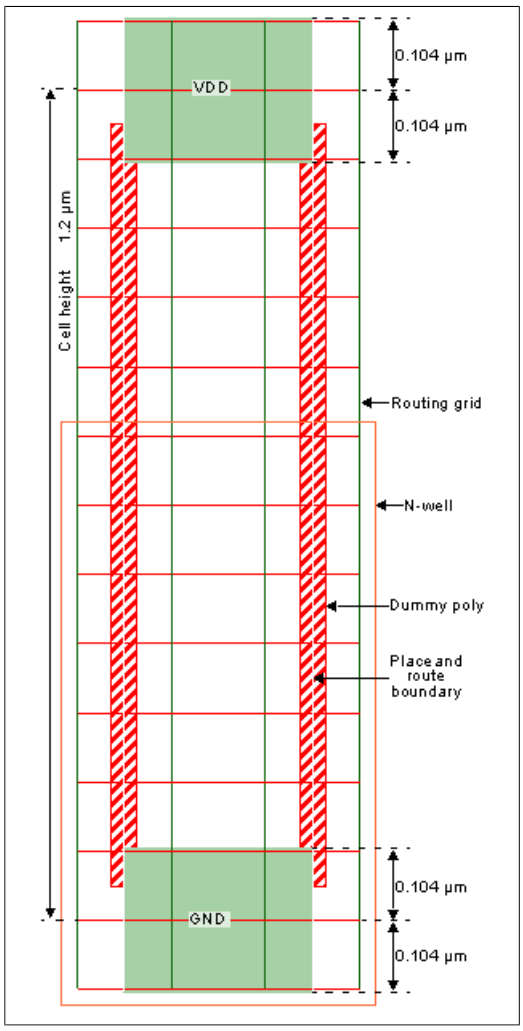
Library Architecture

This section illustrates the architecture used for C28SOI_SC_12_CORE_LL Standard Cell library.

Following table shows the Physical Specifications for this library.

Physical Specifications	
Parameter	**Measurement**
Drawn Gate Length (um)	0.030
Layout Grid (um)	0.001
Vertical Pin Grid (um)	0.1
Horizontal Pin Grid (um)	0.136
Cell Power and Ground Rail Width (um)	0.208

Figure 1: Cell Architecture



1. Quick References

	Please refer to the Naming Convention Document available in Design Package for more details regarding cell names.

	Please refer to the Standard Cells Reference Manual available in Design Package for more details on library specific information.

2. Functional Specification

2.1. Cell Info

2.1.1. LL(LP Low Vt)

2.1.1.1. Poly Bias With 0nm

Table 2: Cell List

Cell Type	Drive Strength	Cell Description
C12T28SOI_LL_SDFPRSQNT	X17, X33, X8	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ
C12T28SOI_LL_MX41	X27, X7	4:1 non-inverting Multiplexer with individual selects
C12T28SOI_LL_SDFPQN	X17, X33, X8	Positive edge triggered Scan D flip-flop; having inverted output QN only
C12T28SOI_LL_NOR2A	X13, X27, X3, X41, X55, X6, X7	2 input NOR with A input inverted
C12T28SOI_LL_AO12	X17, X33, X8	2 input AND into 2 input OR
C12T28SOI_LL_NAND2A	X13, X27, X3, X40, X54, X7	2 input NAND with A input inverted
C12T28SOI_LL_SDFPQT	X17, X33, X8	Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LL_SDFPSQN	X17, X25, X33, X8	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only
C12T28SOIDV_LLBR0P6_NAND3	X18	Beta ratio optimization 0.6, 3 input NAND,Vdd rail at the bottom of the cell
C12T28SOI_LL_SDFPSQNT	X17, X33, X8	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ
C12T28SOI_LL_OA222	X17, X33, X8	Triple 2 input OR into 3 input AND
C12T28SOI_LL_DFPSQN	X17, X30	Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only
C12T28SOI_LL_NOR3A	X13, X19, X25, X6	3 input NOR with A input inverted
C12T28SOI_LL_SDFPQNT	X17, X33, X8	Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ
C12T28SOI_LLHF_SDFPSQN	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only
C12T28SOI_LL_MUXI21	X10, X16, X21, X3, X5	2:1 inverting Multiplexer with coded selects
C12T28SOI_LL_SDFPHRQ	X17, X33, X8	Positive edge triggered Scan D flip-flop; with active high data enable and active low

Cell Type	Drive Strength	Cell Description
		asynchronous Reset; having non-inverted output Q only
C12T28SOI_LL_AO112	X17, X33, X8	2 input AND into 3 input OR
C12T28SOI_LLHF_SDFPRQNT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ
C12T28SOI_LL_NAND3A	X12, X18, X24, X6	3 input NAND with A input inverted
C12T28SOI_LL_LDLQ	X17, X33, X8	Active Low transparent Latch; having non-inverted output Q only
C12T28SOI_LLHF_SDFPSQNT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ
C12T28SOI_LL_NAND4AB	X12, X18, X24, X6	4 input NAND with A and B inputs inverted
C12T28SOI_LL_SDFPRQ	X17, X33, X8	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LL_OAI222	X3, X9	Triple 2 input OR into 3 input NAND
C12T28SOI_LL_NAND3AB	X13, X20, X27, X7	3 input NAND with A and B inputs inverted
C12T28SOI_LLHF_SDFPSQT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LL_LDLRQ	X33, X8	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LL_AOI13	X29, X38, X5	3 input AND into 2 input NOR
C12T28SOI_LL_OR2	X16, X33, X50, X8	2 input OR
C12T28SOI_LL_OR4	X20, X27	4 input OR
C12T28SOI_LL_AOI12	X17, X33, X44, X6	2 input AND into 2 input NOR
C12T28SOI_LL_OA22	X17, X33, X8	Double 2 input OR into 2 input AND
C12T28SOI_LL_AO222	X17, X33, X4, X8	Triple 2 input AND into 3 input OR
C12T28SOI_LLHF_SDFPRQT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LL_CBI4I6	X11, X16, X21, X5	4 input multi stage compound Boolean with inverting last stage
C12T28SOI_LL_SDFPRQN	X17, X33, X8	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only
C12T28SOI_LL_SDFPSQT	X17, X33, X8	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LL_OAI211	X10, X15, X21, X5	2 input OR into 3 input NAND

Cell Type	Drive Strength	Cell Description
C12T28SOI_LL_SDFPRSQT	X17, X33, X8	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LLBR0P6_NAND3	X12, X18, X24, X35, X47, X6	Beta ratio optimization 0.6, 3 input NAND
C12T28SOI_LL_MUX41	X31, X8	4:1 non-inverting Multiplexer with coded selects
C12T28SOI_LL_AO22	X17, X33, X8	Double 2 input AND into 2 input OR
C12T28SOI_LL_DFPHQN	X17, X33, X8	Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only
C12T28SOI_LL_AOI22	X10, X16, X21, X42, X4	Double 2 input AND into 2 input NOR
C12T28SOI_LL_OA12	X17, X33, X8	2 input OR into 2 input AND
C12T28SOI_LLHF_SDFPHRQN	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only
C12T28SOI_LL_AOI21	X11, X16, X23, X46, X6	2 input AND into 2 input NOR
C12T28SOI_LL_LDHQN	X17	Active High transparent Latch; having inverted output QN only
C12T28SOI_LL_SDFPHRQN	X17, X33, X8	Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only
C12T28SOI_LL_SDFPQ	X17, X33, X8	Positive edge triggered Scan D flip-flop; having non-inverted output Q only
C12T28SOI_LLBR0D8_NAND2	X14, X7	2 input NAND
C12T28SOI_LL_NOR2	X10, X14, X17, X21, X24, X27, X3, X40, X49, X53, X57, X5, X65, X7, X84	2 input NOR
C12T28SOI_LL_NOR3	X13, X16, X19, X22, X25, X37, X49, X4, X6, X9	3 input NOR
C12T28SOI_LLHF_SDFPQT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LL_NOR4	X17, X25, X32, X8	4 input NOR
C12T28SOI_LL_DFPHQ	X17, X33, X8	Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only
C12T28SOI_LLHF_SDFPQN	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having inverted output QN only
C12T28SOI_LL_BF	X100, X134, X13, X16, X21, X25, X29, X33, X42, X4, X50, X58, X67, X6, X75, X84, X8	Buffer
C12T28SOI_LLS_NOR2	X34, X41, X55	Design optimized for speed, 2 input NOR

Cell Type	Drive Strength	Cell Description
C12T28SOI_LL_SDFPRQT	X17, X33, X8	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LL_HA1	X33, X8	Half-adder having 1 bit input operand
C12T28SOI_LL_XNOR3	X16, X25, X8	3 input Exclusive NOR
C12T28SOI_LL_DFPQ	X17, X30, X33, X8	Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only
C12T28SOI_LL_XNOR2	X17, X25, X33, X8	2 input Exclusive NOR
C12T28SOI_LL_DFPRQN	X17, X30	Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only
C12T28SOI_LLHF_SDFPRQN	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only
C12T28SOI_LL_AND2	X16, X25, X33, X42, X8	2 input AND
C12T28SOI_LL_AND3	X17, X25, X33, X8	3 input AND
C12T28SOI_LL_AND4	X20, X27, X4, X6	4 input AND
C12T28SOI_LL_DFPQN	X17, X30, X33, X8	Positive edge triggered Non-scan D flip-flop; having inverted output QN only
C12T28SOI_LL_OAI22	X10, X15, X21, X42, X5	Double 2 input OR into 2 input NAND
C12T28SOI_LLHF_SDFPRQ	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LL_AO212	X17, X33, X8	Double 2 input AND into 3 input OR
C12T28SOI_LL_MUX21	X17, X25, X33, X8	2:1 non-inverting Multiplexer with coded selects
C12T28SOI_LL_AOI222	X13, X17, X4, X8	Triple 2 input AND into 3 input NOR
C12T28SOI_LL_IV	X100, X134, X13, X17, X21, X25, X29, X33, X4, X50, X58, X67, X6, X75, X84, X8	Inverter
C12T28SOI_LL_FA1	X33, X8	Full-adder having 1 bit input operand
C12T28SOI_LL_XOR2	X16, X25, X31, X4, X8	2 input Exclusive OR
C12T28SOI_LL_XOR3	X17, X24, X8	3 input Exclusive OR
C12T28SOI_LL_LDHQ	X23, X8	Active High transparent Latch; having non-inverted output Q only
C12T28SOI_LLHF_SDFPSQ	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only
C12T28SOI_LL_DFPRQ	X17, X30	Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LL_OAI12	X17, X34, X46, X6	2 input OR into 2 input NAND
C12T28SOI_LLS_NAND2	X40, X54	Design optimized for speed, 2 input NAND

Cell Type	Drive Strength	Cell Description
C12T28SOI_LL_AOI211	X17, X34, X4	2 input AND into 3 input NOR
C12T28SOI_LL_OAI21	X11, X17, X23, X46, X5	2 input OR into 2 input NAND
C12T28SOI_LLHF_SDFPQ	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having non-inverted output Q only
C12T28SOI_LL_PAO2	X16, X25, X33, X8	2 bit programmable AND/OR logic
C12T28SOI_LL_SDFPSQ	X17, X25, X33, X8	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only
C12T28SOI_LL_NOR4AB	X13, X19, X25, X6	4 input NOR with A and B inputs inverted
C12T28SOI_LL_NAND3	X12, X15, X18, X21, X24, X35, X47, X4, X6, X9	3 input NAND
C12T28SOI_LL_SDFPRQNT	X17, X33, X8	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ
C12T28SOI_LLS_XOR2	X6	Design optimized for speed, 2 input Exclusive OR
C12T28SOI_LL_NAND2	X10, X13, X17, X20, X24, X27, X3, X42, X47, X50, X58, X5, X67, X7	2 input NAND
C12T28SOI_LLS_XOR3	X4	Design optimized for speed, 3 input Exclusive OR
C12T28SOI_LL_AOI112	X35, X5	2 input AND into 3 input NOR
C12T28SOI_LL_NAND4	X17, X25, X33, X8	4 input NAND
C12T28SOI_LLHF_SDFPHRQ	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LL_CB4I1	X17, X25, X33, X8	4 input multi stage compound Boolean with non-inverting last stage
C12T28SOI_LL_OAI112	X10, X21, X31, X5	2 input OR into 3 input NAND
C12T28SOI_LL_OR2AB	X16, X24, X32, X8	2 input OR with A and B inputs inverted
C12T28SOI_LLS1_FA1	X33, X8	Design optimized for speed, Full-adder having 1 bit input operand
C12T28SOI_LL_DFPSQ	X17, X30	Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only
C12T28SOI_LL_OA112	X17, X25, X33, X8	2 input OR into 3 input AND
C12T28SOI_LLHF_SDFPQNT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ
C12T28SOI_LLS_XNOR2	X6	Design optimized for speed, 2 input Exclusive NOR
C12T28SOI_LLS_XNOR3	X4	Design optimized for speed, 3 input Exclusive NOR

3. Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com