Merging GDS

CMOS and derivative PDK

life.augmented

3 Solutions to merge GDS

	license	Gzip support	Multi CPU	Check multiple cell	Memory usage	Disk usage	# GDS to merge
fgdsout	free	yes	no	no	<1Gb	2x input GDSs size	2
Calibredrv interactive	Caldesignrev	yes	no	yes	2x input GDS size	2x input GDSs size	2
Calibredrv file merge	caldesignrev	yes	no	yes	<1Gb	2x input GDSs size	No limit

fgdsOut command

Usage: fgdsOut [-gdsdir <path>] -scale <float> -I1gds <file>
-I1topcell <string> -I2gds <file> -I2topcell <string> -outgds <path>
-outtopcell <string> [-help|-h|-u|-U] [-gui] [-version]
where:

-gdsdir	Gds directory. Default is '.'.
-scale	Scale. Default is '1000.0'.
-I1gds	Gds Path of Input file I1.
-I1topcell	Top Cell Name for I1 File.
-I2gds	Gds Path of Input file I2.
-I2topcell	Top Cell Name for I2 File.
-outgds	Gds Path of Output file.
-outtopcell	Top Cell Name for Output File.
-help|-h|-u|-U	Display the script usage.
-gui	Graphical user interface.
-version	Display the script version.

Example: command line


```
>> fgdsOut  -gdsdir "." - scale 1000.0
-I1gds chip_withoutTiles.gds.gz -I1topcell_withoutTiles
-I2gds chip_with_Tiles_BE.gds.gz -I2topcell_Tiles
-outgds Final.gds -outtopcell TOP
```

Example: merge time

Input files

- Chip no tiles: 6.8GB (40.4GB unzipped)
- Tiles BE: 2.5GB (13.8GB unzipped)
- IDAS 30Mb/s

Min required disk space: 2x(40.4 + 13.8) ~110GB

Merge time

- Unzip time: 39mn
- Merging time: 30mn
- Total time: 70mn

Calibredrv Layout filemerge

Uses less than 1GB RAM in all cases…

But needs disk space

Input files are unzipped in a temporary directory

- Use -tmp option to specify it
- or use MGC_CWB_TMP_DIR environment variable

Make sure temp dir space > total unzipped files size :

To know unzipped GDS size (bytes):

> “gunzip -c file_name.gds.gz | wc -c”

Temp files are automatically removed after merge

Example: command line

2 ways to invoke layout file merge :

```
>>calibredrv -a layout filemerge
-in chip_withoutTiles.gds.gz
-in chip_with_Tiles_BE.gds.gz
-in chip_with_Tiles_FE.gds
-out chip_withTiles.gds.gz
-createtop TOP
-force_rename
-tmp ./TMP
```

```
>> calibredrv
// Calibre DESIGNrev
v2012.3_31.26...
// ...
// DESIGNrev authorized.
% layout filemerge
-in chip_withoutTiles.gds.gz
-in chip_with_Tiles_BE.gds.gz
...
```

layout filemerge features

- Handles GDSII, OASIS, .gz files
- Special modes to address common issues
  - Create top cell
  - Detect different cells with same name and apply selected mode
  - Include / exclude specific layers

  …

Full information in
Calibre® DESIGNrev Reference Manual,
Ch. 6 Batch Commands for Layout Manipulation,
Layout Object, layout filemerge (calbr_drv_ref.pdf).

Example: merge time

Input files

- Chip no tiles: 6.8GB (40.4GB unzipped)
- Tiles BE: 2.5GB (13.8GB unzipped)
- Tiles FE: 27MB (not zipped)
- IDAS 30Mb/s

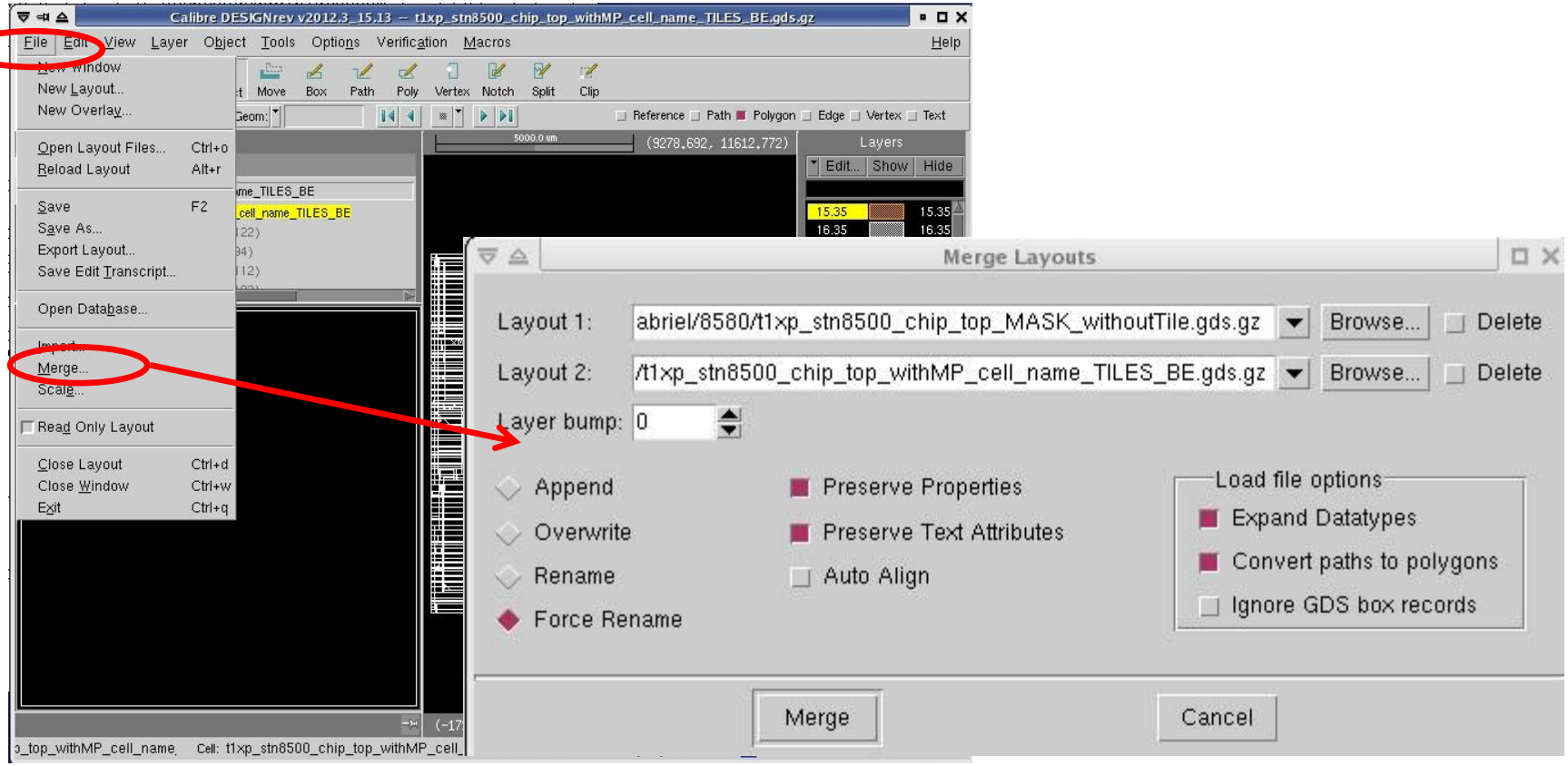
Min required disk space: 2x(40.4 + 13.8) ~110GB

Merge time

- Unzip time: 39mn
- Merging time: 52mn
- Total time: 91mn

Calibredrv interactive

Open both GDS to merge in calibredrv
-> File -> Merge
-> File -> save as…



Example: merge time

Input files

- Chip no tiles: 6.8GB (40.4GB unzipped)
- Tiles BE: 2.5GB (13.8GB unzipped)
- Tiles FE: 27MB (not zipped)
- IDAS 85Mb/s

Min required disk space: 2x(40.4 + 13.8) ~110GB

Merge time

- Unzip time: 18mn
- Merging time: 30mn
- Total time: 48mn

Important factor for performance

Instantaneous Disk Access Speed (IDAS)

Approximate loading time:

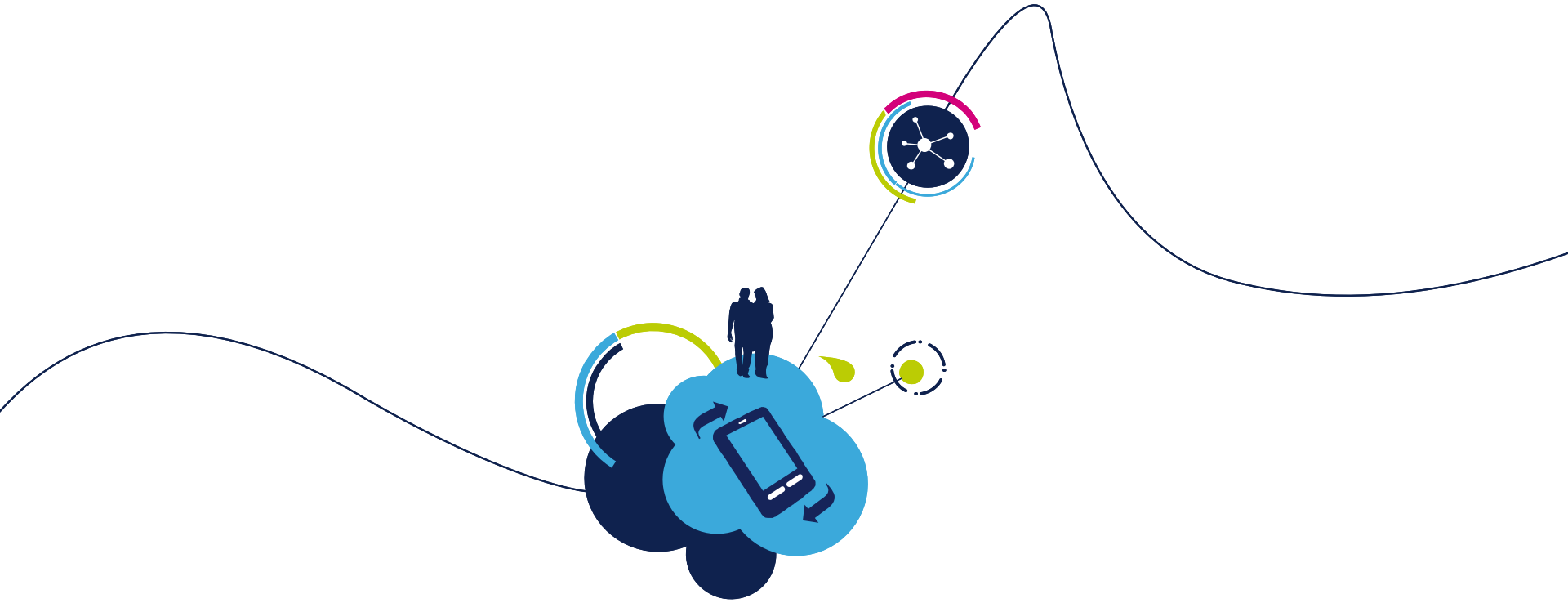
GDS size in MB IDAS 60 ≃ min loading time in minutes

E.g.: GDS size = 40 GB

IDAS = 80 MB/s

minimum loading time:

40,000MB 80 MB/s 60 ≃ 8 mn



Thank You