Innovus Menu Reference

Product Version 19.17
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Contents

About This Manual

The Cadence® Innovus™ Implementation System family of products provides an integrated solution for an RTL-to-GDSII design flow. This manual provides information specific to the forms and commands available in the graphical user interface of Innovus Implementation System (Innovus).

This document applies to the Innovus user interface. See the Innovus Stylus Common UI Menu Reference document for the Innovus Stylus user interface.

Audience

This manual is written for experienced designers of digital integrated circuits. Such designers must be familiar with design planning, placement and routing, block implementation, chip assembly, and design verification. Designers must also have a solid understanding of UNIX and Tcl/Tk programming.

How This Manual Is Organized

The chapters in this manual are organized to correspond to the menus in the Innovus graphical user interface (GUI). Each chapter contains one of more of the following sections. A particular section is omitted from a chapter if there is no significant information related to the topic.

Form Overview	Introduces the features available through the various menu selections and provides an illustration of the forms and screens used to set options and run the features.
Forms and Options	Lists and describes the fields and options on each screen.
Related Topics	Provides links to related tasks and concepts in the *Innovus User Guide*.
Related Commands	Lists the text commands that correspond to the GUI forms for this feature.

Conventions Used in This Manual

This section describes the typographic and syntax conventions used in this manual.

`text`	Indicates text that you must type exactly as shown. For example: `set_message -severity info`
`text`	Indicates information for which you must substitute a name or value. In the following example, you must substitute the name of a specific file for *`file_name`*: `report_area -out_file` *file_name*
text	Indicates the following: • Text found in the graphical user interface (GUI), including form names, button labels, and field names • Terms that are new to the manual, are the subject of discussion, or need special emphasis • Titles of manuals
`[ ]`	Indicates optional arguments. In the following example, you can specify none, one, or both of the bracketed arguments: `command [-arg1] [arg2` *`value`*`]`
`[ | ]`	Indicates an optional choice from a mutually exclusive list. In the following example, you can specify any of the arguments or none of the arguments, but you cannot specify more than one: `command [arg1 | arg2 | arg3 | arg4]`
`{ | }`	Indicates a required choice from a mutually exclusive list. In the following example, you must specify one, and only one, of the arguments: `command {arg1 | arg2 | arg3}`

`{[ ] [ ]}`	Indicates a required choice of one or more items in a list. In the following example, you must choose one argument from the list, but you can choose more than one: `command {[arg1] [arg2] [arg3]}`
{ }	Indicates curly braces that must be entered with the command syntax. In the following example, you must type the curly braces: `command arg1` **{**`x y`**}**
`...`	Indicates that you can repeat the previous argument.
. . .	Indicates an omission in an example of computer output or input.
Command - Subcommand	Indicates a command sequence, which shows the order in which you choose commands and subcommands from the GUI menu. In the following example, you choose *Power* from the menu, then *Power Planning* from the submenu, and then *Add Ring* from the displayed list: *Power - Power Planning - Add Ring* This sequence opens the *Add Rings* form.

Related Documents

For more information about the Innovus family of products, see the following documents. You can access these and other Cadence documents with the Cadence Help documentation system.

Innovus Product Documentation

- What's New in Innovus
  Provides information about new and changed features in this release of the Innovus family of products.
- Innovus User Guide
  Describes how to install and configure the Innovus software, and provides strategies for implementing digital integrated circuits.

- Innovus Text Command Reference
  Describes the Innovus text commands, including syntax and examples.
- Innovus Database Access Command Reference
  Lists all the Innovus database access commands and provides a brief description of syntax and usage.
- Innovus Foundation Flows User Guide
  Describes how to use the scripts that represent the recommended implementation flows for digital timing closure with the Innovus software.
- Mixed Signal Interoperability Guide
  Describes the digital mixed-signal flow.
- README file
  Contains installation, compatibility, and other prerequisite information, including a list of Cadence Change Requests (CCRs) that were resolved in this release. You can read this file online at downloads.cadence.com.

Innovus Stylus Common UI Product Documentation

- Innovus Stylus Common UI Migration Guide
  Provides information on migrating from legacy to the Stylus Common UI version of the Innovus software.
- What's New in Innovus Stylus Common UI
  Provides information about new and changed features in this release of the Innovus family of products.
- Innovus Stylus Common UI User Guide
  Describes how to install and configure the Innovus Stylus Common UI software, and provides strategies for implementing digital integrated circuits.
- Innovus Stylus Common UI Text Reference Manual
  Describes the Innovus Stylus Common UI text commands, including syntax and examples.
- Innovus Stylus Common UI Menu Reference
  Provides information specific to the forms and commands available from the Innovus Stylus Common UI graphical user interface.
- Stylus Common UI Database Object Information
  Provides information about Stylus Common UI database objects.
- Innovus Stylus Common UI Mixed Signal (MS) Interoperability Guide
  Describes the digital mixed-signal flow using Innovus Stylus Common UI.

For a complete list of documents provided with this release, see the Cadence Help documentation system.

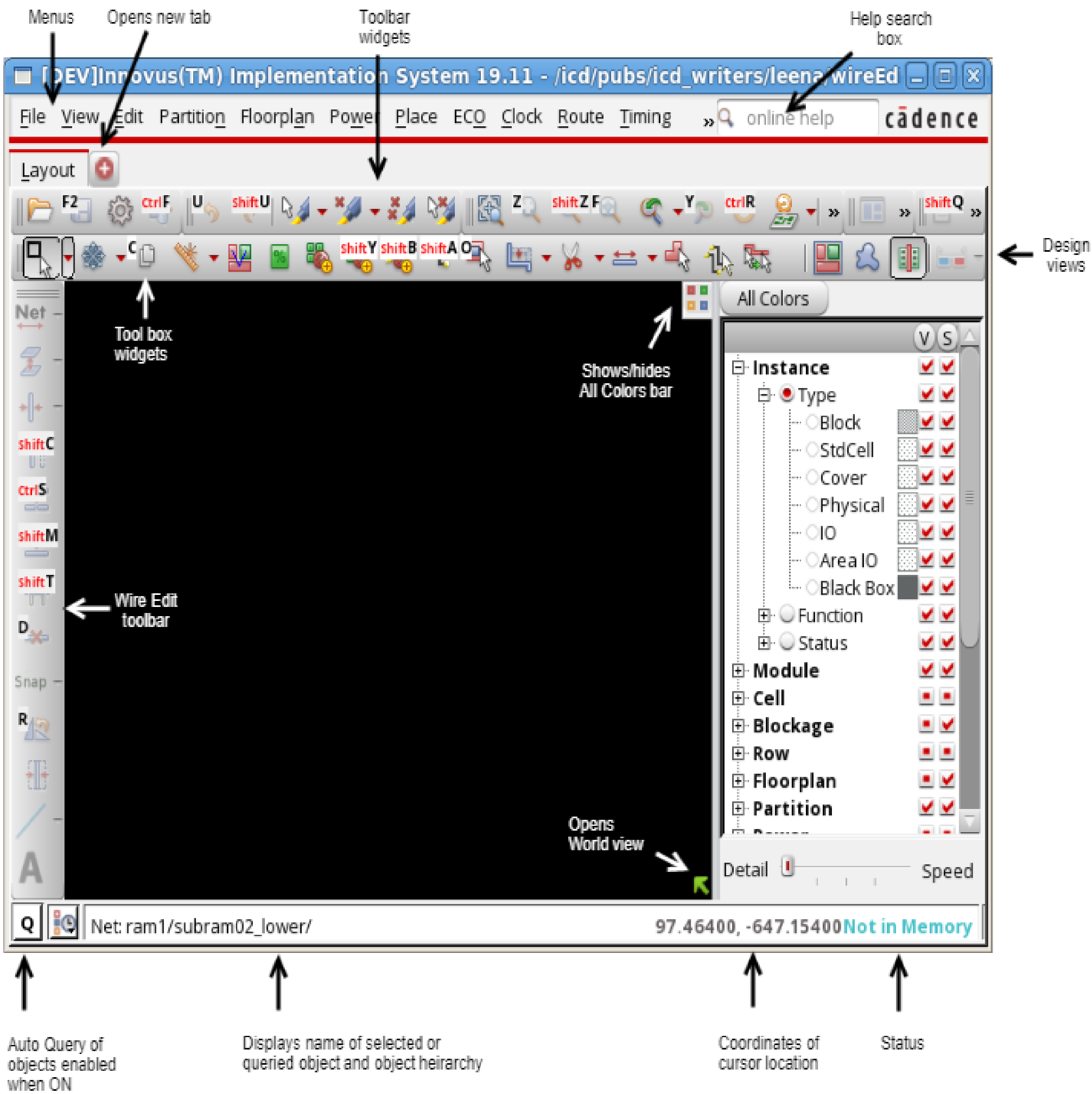
1

The Main Window

- Auto Query
- Select Bar
- Docking Tool and Toolbar Widgets
- Tear-off Menus and Submenus
- Mouse Operation
- Keyboard Shortcuts
- Selecting a Large Number of Objects
- Viewing the Documentation Library through the Help Menu
- Accessing the Documentation Library Quickly through the Help Search Box
- Displaying Innovus Version Number, and Patent- and Copyright-Information
- Customizing the User Interface
- Closing or Hiding the GUI

Main Window Components

The components in the Innovus™ Implementation System main window are identified in the following figure, and described in the sections that follow.



In the display area, the *Layout* tab is open by default. This tab displays the design layout. You can click the + sign next to the *Layout* tab title to open any of the following in a new tab:

- *Layout*
- Debug *Timing*

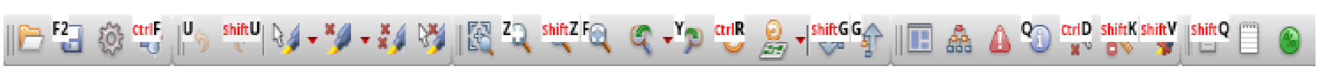
- *Timing Path Analyzer*
- *Clock Tree Debugger*
- *Design Browser*
- *Layout Viewer*
- *Violation Browser*
- *Schematic*

Toolbar Widgets

The following row of widgets, located below the menus and above the design display area, includes shortcuts for some commonly used Innovus commands. Similar icons are clubbed together into logical groups.

You can show/hide, dock, and move around the icon groups, as desired. To access the toggle feature of toolbars, right-click anywhere on the toolbar and select/deselect an icon group to show/hide that group.

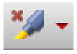
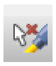
Note: Press the `Alt` key to view the shortcut keys (bindkeys) of various toolbar widgets, where applicable.

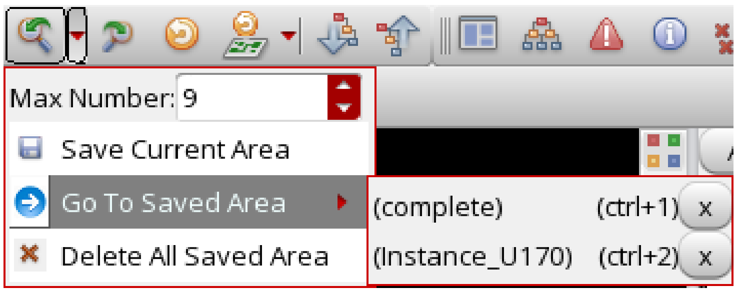


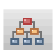
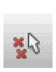
The following table describes the widgets that are located in the Toolbar Widget area:

Widget	Description
File Widgets	
	*Import Design*--Opens the Design Import form.
	*Save Design*--Opens the Save Design form. The equivalent bindkey is `F2`.
	*Set Preference*--Opens the Preferences form.

	*Find/Select Object*--Opens the Find/Select Object form. The equivalent bindkey is `Ctrl+F`.
Edit Widgets	
	*Undo*--Click this widget to undo the previous action. You can only undo a single action. You can undo any wire editor action, any power planning action, and the following floorplanning actions: • Align Object • Shift Object • Space Object • Flip/Rotate Object • Snap Floorplan The default equivalent bindkey is `U`. The equivalent text command is `undo`.
	*Redo*--Click this widget to restore the design to the same state as before you clicked the undo button. You can only redo a single undo action. You can redo any wire editor action, any power planning action, and the following floorplanning actions: • Align Object • Shift Object • Space Object • Flip/Rotate Object • Snap Floorplan • Resize Floorplan The equivalent bindkey is `SHIFT+U`. The equivalent text command is `redo`.
	*Highlight Selected*--Highlights the objects selected in the GUI with the current highlight set, as displayed in the *Edit Highlight Color* widget. Use the drop-down menu to select a new highlight set.

	*Clear Highlight*--Clears the highlight from those objects that are highlighted with the current highlight set, as displayed in the *Edit Highlight Color* widget. You can choose the type of highlight to be deleted from the drop-down menu.
	*Clear All Highlight*--Clears all highlights from the GUI.
	*Clear Selected*--Clears highlight from the selected object in the GUI.
View Widgets	
	*Zoom Selected*--Select one or more design objects, then click this widget to zoom into the area that contains the selected objects. The equivalent text command is `zoomSelected`. You can use the *Margin* option in the drop-down menu of the *Zoom Selected* widget to specify how close to the selected object the tool zooms in.  The zoom margin is the minimum spacing between the bounding box of the selected object(s) and the layout view.
	*Zoom In*--Click this widget to display a smaller area of the design in greater detail. Each click zooms in one level. The equivalent bindkey is `z`. The equivalent text command is `zoomIn`.
	*Zoom Out*--Click this widget to display a larger area of the design in less detail. Each click zooms out one level. The equivalent bindkey is `Shift+Z`. The equivalent text command is `zoomOut`.
	*Fit*--Click this widget to display the entire placed design within the design display area. The equivalent bindkey is `F`.

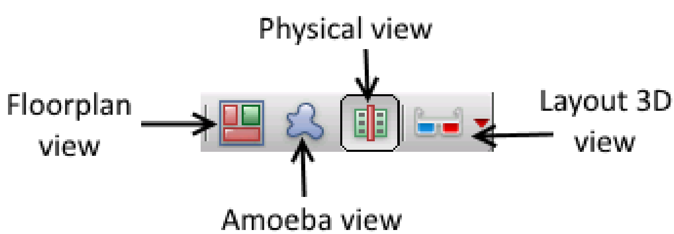
	*Previous*--Click this widget to switch the display from the current to the previous view. The previous view could be a previously saved area or previously accessed zoom level. The equivalent bindkey is W. Pressing the bindkey repeatedly cycles through all the previous views. Use the *Max Number* field in the drop-down menu of this widget to specify the maximum number of views (areas plus zoom levels) that can be saved. You can also use the drop-down menu to save the current area of the design visible in the main window, access previously saved areas, and delete all saved areas.  The bindkey shortcut for saving the current area is `Ctrl+P`. To quickly switch to a previously saved area, use the `Ctrl+`*<number>* bindkey. For example, suppose you have saved four different locations/zoom levels in the design display area. You can go to the first area you saved by pressing `Ctrl+1`, the second saved area by pressing `Ctrl+2`, and so on. If you want the *Previous* widget to cycle through only the saved areas and disregard zoom levels, select the *Only Save User Specified View* check box on the *Display* page of the Preferences form. For more details about this option, see the View Menu chapter. By default, the maximum number of views that can be saved is *9*. You can decrease this value, if required.
	*Next*--Click this widget to switch the display from the current to the next location in the *Go To Saved Area* list or the next zoom level in the zoom sequence saved in the design memory. The equivalent bindkey is `Y`. When you press the bindkey or click this widget repeatedly, the tool cycles through all saved views (saved areas and zoom levels). If you want the *Next* widget to cycle through only the saved areas and disregard zoom levels, select the *Only Save User Specified View* check box on the *Display* page of the Preferences form. For more details about this option, see the View Menu chapter.

	*Redraw*--Click this widget to update the display with new colors or stipple patterns that you selected from the More Colors form. The equivalent bindkey is `Ctrl+R`.
	*Regenerate Layout Snapshot*--Use this widget to take a snapshot of the layout and redraw it based on the specified resolution. You can specify the resolution in the drop-down menu of the widget. For this feature to work, you must select the *Enable Layout Snapshot* check box in the drop-down menu.
	*Ungroup*--Click this widget to display the submodules for a selected module guide. Each time you click this widget, you move further down the hierarchy. The equivalent bindkey is `Shift+G`.
	*Group*--Click this widget to display the next module up for a selected module guide. Each time you click this widget, you move further up the hierarchy. The equivalent bindkey is `g`.
Tools Widgets	
	*Floorplan Toolbox*--Provides access to the features commonly used during floorplanning. For more information, see Floorplan Toolbox in the Floorplan Menu chapter.
	*Design Browser*--Opens the Design Browser form. For more information, see Design Browser in the Tools Menu chapter.
	*Violation Browser*--Opens the Violation Browser form. For more information, see Violation Browser in the Tools Menu chapter.
	*Attribute Editor*--Opens the Attribute Editor form. The equivalent default bindkey is `q`. For more information, see Attribute Editor in the Edit Menu chapter.
	*Deselect All*--Deselects all objects in the design display area.The equivalent bindkey is `Ctrl+D`.
	*Clear All Rulers*--Clears all rulers from the display area. The equivalent bindkey is Shift+`K`. **Note:** To remove a single ruler, place the mouse cursor over the ruler and press `Ctrl+w` or `Delete`.

	*Clear Violations*--Clears all the violation markers in your design. The equivalent bindkey is `Shift+V`.
Report Widgets	
	*Summary Report*--Opens the Summary Report form. The equivalent bindkey is `Shift+Q`.
	*Report Select Obj*--Returns information on the selected object. For more information, see Selected Object in the File Menu chapter.
	*Query Design Density*--Click this widget to output the module density. For more information, see the Effective Utilization Display section in the "Floorplanning the Design" chapter of the *Innovus User Guide*.

Design Views

The Innovus main window includes different design views that you can switch to during a session: the *Floorplan* view, the *Amoeba* view, the *Physical* view, and the *Layout 3D* view.



Selecting a design view also changes the display of the available tool widgets. For a descriptions of all the widgets, see Tool Widgets.

Floorplan View

The *Floorplan* view displays the hierarchical module and block guides, connection flight lines, and floorplan objects, including block placement, and power and ground nets.

Use the `Shift+G` keys or click the *Ungroup* widget to display the submodules for a selected module guide. Each time you use the `Shift+G` keys, you move further down the hierarchy. Use the `G` key or click the *Group* widget to move up the hierarchy.

Amoeba View

The *Amoeba* view displays the outline of the modules and submodules after placement, showing physical locality of the module.

Use the `Shift+G` keys or click the *Ungroup* widget to display the submodules for a selected module guide. Each time you use the `Shift+G` keys, you move further down the hierarchy. Use the `G` key or click the *Group* widget to move up the hierarchy.

Physical View

The *Physical* view displays the detailed placements of the module's blocks, standard cells, nets, and interconnects. You can move standard cells, blocks, and power and ground objects in the *Physical* and *Floorplan* views.

Viewing Floorplan Objects in Physical View

You can view the floorplan objects even in the physical view. To enable this feature:

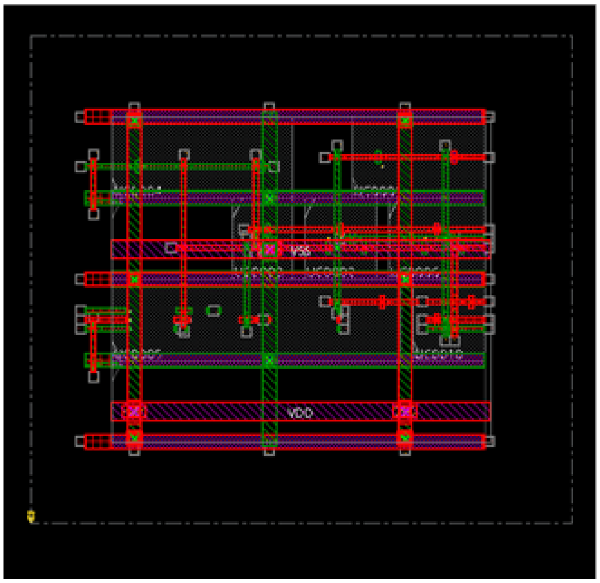
1. Select *View - Set Preference*.
2. Select the Display page in the Preferences form.
3. Select the option *Show Floorplan Object in Physical View*.

You can use this feature together with color groups to create a custom view. For example, you can create a color group that has a custom setting for block colors and use this color group while viewing floorplan objects in the physical view.

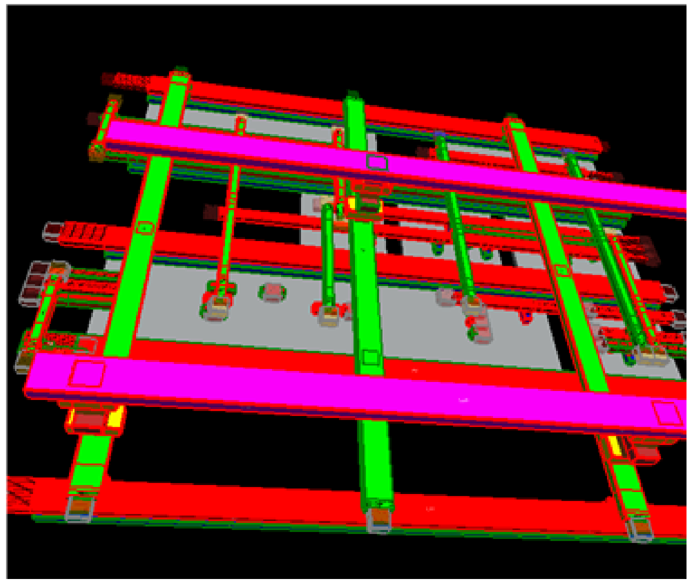
Layout 3D View

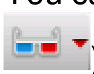
The *Layout 3D* view provides you a three-dimensional view of objects. Modern designs have more than 15 layers, and include complicated routing shapes, such as via stacks, shielding nets, and via pillars. In such cases, a 3D view makes it easier for you to visualize and browse the layout.

2D view of layout



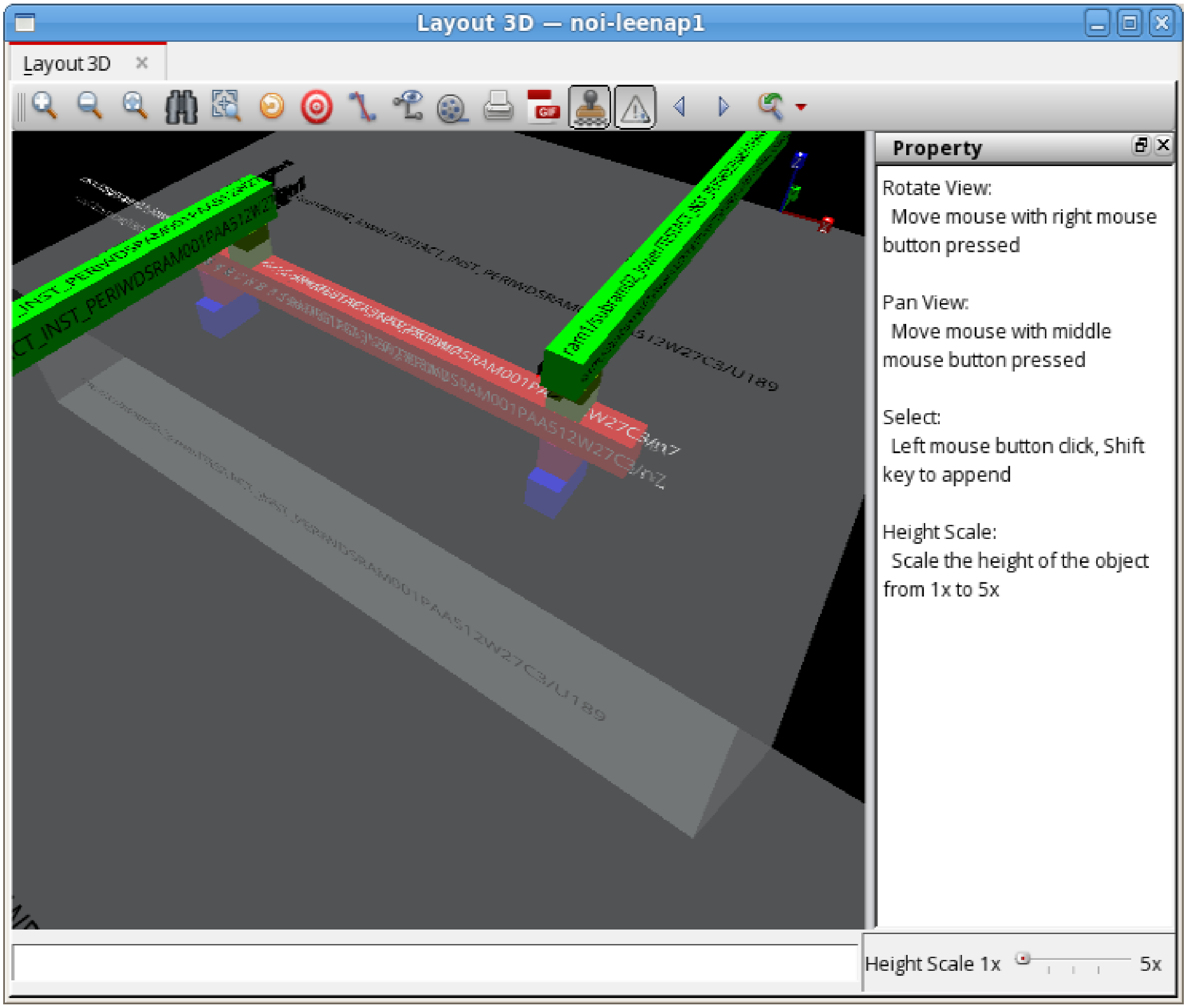
3D view of layout



You can choose one of the following options from the drop-down menu of the *Layout 3D* widget ():

- *Current view*: Generates a bird's eye view of all objects that are currently visible in the design display area of the main window.
- *Base On selected*: Generates a 3D view around the objects that are currently selected in the main window.
- *Select Area By Mouse*: Generates a 3D view of the area you select in the main window by drawing a box.
- *Box*: Generates a 3D view of the area enclosed by the box coordinates you specify.

Layout 3D Window



Note: The Layout 3D view is currently supported only for design areas containing less than 20,000 objects. When you select one of the *Layout 3D* options, the tool checks whether this criterion is met before launching the 3D view.

For more information on the Layout 3D view, see Using the Layout 3D View.

Tool Box Widgets

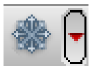
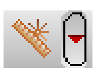
The Innovus main window includes several types of tool box widgets, which are located on the left side of the design view icons. Selecting a design view displays the tool box widgets that are available for that operation.

Note: Press the `Alt` key to view the shortcut keys (bindkeys) of various tool widgets, where applicable.

The main window also contains *toolbar* widgets across the top of the window. For more information about these widgets, see Toolbar Widgets.

The following table describes the tool box widgets for all aspects of design editing:

Widget	Description
	*Select by Box/Line*--Click this widget, then click a floorplan object to select it. To select multiple objects, use the *Shift* key or click and drag the mouse. Use the drop-down menu of this widget to choose between selecting by drawing a line or box. Turn on the *Only Select Highlighted* option in the drop-down menu to select only the highlighted objects during box selection. That is, if this option is turned on and you draw a box on the main window to select objects, the non-highlighted objects are not selected even if they fall within the selection box. Select the *Double Clicks for Box/Line Selection* check box in the drop-down menu to zoom in and out of the design easily while making the selection.That is, you can zoom in to the required part of the design and double-click to initiate the selection (by line or box), zoom out (or fit the design) to view a larger portion of the design in the main window, and then zoom in to a different area of the design to complete the selection. This option is useful when you need to make an area selection in a large design.

	*Move/Resize/Reshape*--Click this widget, then click a floorplan object or I/O pad and click on a new location. Use the *Shift* key to select multiple objects to move. Move the mouse to the side or corner of a floorplan object and click and hold to resize and reshape. You can also move or resize rectilinear edges with this tool. Use the drop-down of the *Move* widget to enable or disable movement without restrictions. By default, you can move the selected object without any restriction. If you want to move objects only in orthogonal direction, choose *Orthogonal* from the drop-down menu. In the *Orthogonal* mode, the *Move* widget icon changes to .
	*Copy*--Select the object to be copied and then click the *Copy* widget or press the bindkey `c`. The icon changes to a black circle when you hover over the selected object. Click and drag the object copy. A black and white image of the object moves along with the cursor to guide you. Click to paste the object at the new location. You can set the direction and orientation of the object copy by clicking the widget and then pressing the `F3` key to display the Copy form. For more information, see Copy in the Edit Menu chapter.
	*Create Ruler*--Click this widget, then left-click in the design display area and drag the mouse to add a ruler (in micrometers), and left-click again to end the ruler. To move the ruler, left-click and drag it to a new location. Left-click the ruler again to keep it in the new location. To remove all rulers, press `K` (`Shift-k`). To remove a single ruler, select the *Create Ruler* widget and then place the cursor on the ruler. The ruler color changes indicating that it is selected. Click to move the ruler or press `Ctrl-w` or `Delete` to remove the ruler. You can set the direction in which rulers can be drawn by clicking the widget, then pressing the `F3` key to display the Create Ruler Preferences form. You can also snap rulers to floorplan objects. The ruler can snap to any type of edge, including 45-degree edges. Use the *Color Setting* option in the form to change the color of the ruler. This is useful if you need to draw multiple rulers in an area and want to use different colors for them. For more information, see Create Ruler Preferences in the Tools Menu chapter. Many of these actions are also available in the drop-down menu of the *Create Ruler* widget.

Floorplan Widgets

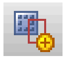
The following table describes tool box widgets for editing the floorplan. For more information on floorplanning, see the "Floorplanning the Design" chapter in the *Innovus User Guide*.

Widget	Description
	*Query Area Density*--Click this widget, then drag the mouse across an area in the design. The placement density utilization for that area is written to the Innovus console.
	*Cut Rectilinear*--Click this widget, then left-click and drag the mouse over a module or partition to create a rectilinear area.
	*Create Size Blockage*--Click this widget, then left-click and drag the mouse over an area in the design to create a size blockage.
	*Create Placement Blockage*--Click this widget, then drag the mouse over an area in the design to draw a placement blockage. You can specify the type of placement object to add, by clicking the widget, then pressing the `F3` key to display the Set Placement Blockage Options form. You can choose between hard, partial, or soft blockages.
	*Create Routing Blockage*--Click this widget, then drag the mouse to create a routing blockage on a specified metal layer. To change or specify more than one layer, double-click the routing blockage to open the Attribute Editor.

Partition Widgets

The following table describes tool widgets for editing the partition. For more information on partitioning, see the "Partitioning the Design" chapter in the *Innovus User Guide*.

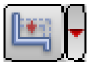
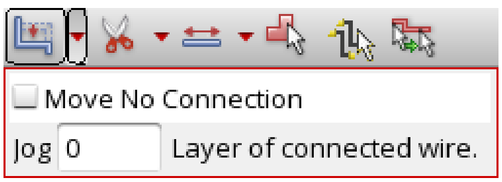
Widget	Description
	*Create Physical Feedthrough*--Click this widget, then drag the mouse over both sides of a partition to insert physical feedthroughs.
	*Create Pin Blockage*--Click this widget, then drag the mouse over a partition to block the area from creating pins on specific metal layers. To change or specify more than one layer, double-click the partition pin blockage to open the Attribute Editor.

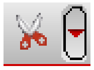
	*Create Pin Guide*--Click this widget, then drag the mouse over an area that overlaps a partition fence or top cell to create a port for a net or bus.

Wire Editing Widgets

The following table describes tool widgets for wire editing. For more information on editing wires, see the "Editing Wires" chapter in the *Innovus User Guide*.

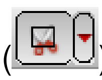
Widget	Description
	*Edit Wire*--When you click this widget, the cursor changes to a pencil when moved into the design area. You can add power or signal wires. Click at a start point and move the cursor. A second click makes a turn. To end the route, double-click the left mouse button. Click the *Select* widget or press the `a` keyboard shortcut to return to *select* mode. *Equivalent keyboard shortcut:* `A`
	*Add Via*--When you click this widget, the cursor changes to a set of concentric squares when moved into the design area. Press the `F3` key to open the Edit Via form. Click the *Select* widget or press the `a` keyboard shortcut to return to *select* mode. *Equivalent keyboard shortcut:* `o`

	*Move Wire*-- When you click this widget, the cursor changes to a circle when moved over the selected wire in the design area. Use the mouse or the arrow keys to move the wire. You can move horizontal wires vertically and vertical wires horizontally. Click the *Select* widget or press the `a` keyboard shortcut to return to *Select* mode. The display area auto pans 20-25% at a time during wire editing. For example, if you are moving a wire to the right of the area currently visible in the main window, the display area automatically pans to the right as you move the wire. When moving a wire, new jog segments are created. You can use the *Jog ____ Layer of connected wire* option in the drop-down menu to specify the number of layers by which the new jog wire segments should be moved up or down.  *Equivalent keyboard shortcut:* `m`

<table>
<tr>
<td></td>
<td>

Cut Wire--Use this widget to cut wires and bus guides on the visible layers. There are two operating modes:

- *Cut Wire by Line* (default): When you click this widget, the cursor changes to scissors in the design display area. Move the cursor to draw a draw a line indicating where to cut a wire. The cut must go all the way through the wire. You can cut special wires horizontally and vertically. The results retain the same direction as the original wire. You can also cut rectangles. Signal wires maintain a one-half wire width extension after being cut. Power wires do not maintain an extension.
- *Cut Wire by Box*: Select the *Cut by Box* option from the drop-down menu to switch to the *Cut Wire by Box* mode.

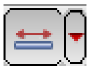
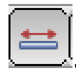
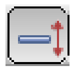
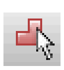
  A square appears on the *Cut Wire* widget () to indicate that you are now in the *Cut Wire by Box* mode. In this mode, you can cut a wire or bus guide by drawing a cut-box to indicate the places from which the wire should be cut. This mode makes it possible to cut off a wire in a single step. Only the wires that are perpendicular to the cut-box edge are cut. In addition, the cut-box edge must pass across the wire, bus guide, or rectangle completely.

You can also use the drop-down menu of the widget to choose between cutting all visible wires or selected wires overlapping with the cut line or box.

Click the *Select* widget or press the `a` keyboard shortcut to return to *select* mode.

Equivalent keyboard shortcut: `x`

</td>
</tr>
</table>

	*Stretch Wire*--Use this widget to stretch a wire. The widget can be used to stretch regular as well as special wires. The *Stretch Wire* widget has two operating modes, which you can select from its drop-down menu: • *Stretch Wire Length* (default): By default, the *Stretch Wire Length* option is selected, as indicated by the widget icon . This option is used to stretch wires in the preferred direction. • *Stretch Wire Width*: If you want to change a wire's width instead of length, choose the *Stretch Wire Width* option. When this option is selected, the widget icon changes to  and you can stretch the wires in the non-preferred direction. In addition to the two stretch modes, the drop-down menu offers the following options: • *Stretch No Connection* - Select this option if you want to stretch the wire without auto via/wire creation and DRC checking. • *Keep Center Line* - Select this option if you want to stretch or shrink the wire or physical pin without changing the center line. This option is enabled only if you have selected the *Stretch No Connection* option on the menu. After wire stretch is complete, click the *Select* widget or press the `a` keyboard shortcut to return to the *Select* mode. *Equivalent keyboard shortcut for Stretch Wire:* `s`
	*Add Polygon*--When you click this widget, the cursor changes to a pencil when moved into the design area. Click in the main window at the start point of the polygon and move the cursor. Click once for each turn. Backspace to cancel the last point in the wire. Double-click to commit the wire. Click the *Select* widget or press the `a` keyboard shortcut to return to *select* mode. *No equivalent keyboard shortcut.*

Bus Guide Widgets

The following table describes tool widget for bus guide editing. For more information on bus planning, see the "Bus Planning" chapter in the *Innovus User Guide*.

Widget	Description
	*Edit Bus Guide*--Click this widget to create a new bus guide, associated with an existing net group.

Flip Chip Widgets

The following table describes tool widget for flip chip editing. For more information on floorplanning, see the "Flip Chip Methodologies" chapter in the *Innovus User Guide*.

Widget	Description
	*Point To Point Route*--Click this widget first and then click on two points-I/O Pad Pin and Bump (or Wire)-to enable the point-to-point router route between these two points. **Note:** To use the *Point To Point Route* icon, you only need to specify the route width, not wider than the I/O pad pin. The router automatically picks up the net name.

Status Bar Hints for Tool Box Widgets

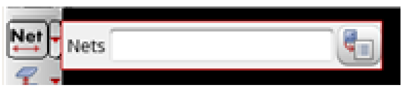
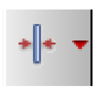
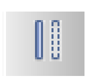
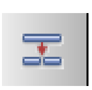
Some of the Tool box widgets provide hint or guidance when you enter the interactive toolbar or icon mode. The hint guides you on the next mouse action to be taken while navigating through the selected mode.

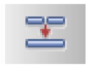
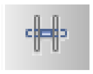
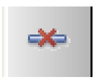
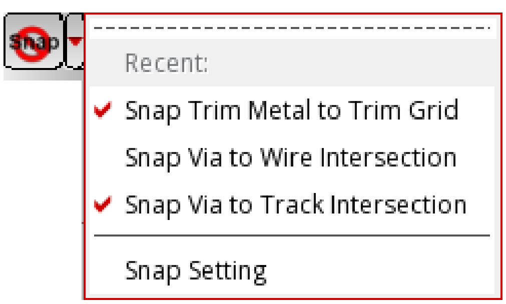
For example, when a user enters the **Create Ruler** mode, the status bar first displays the message Click at the first point of the ruler. After the first mouse click, the status bar message changes to Click the next point of the ruler. This message is repeated until the user exits the **Create Ruler** mode.

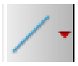
Wire Edit Toolbar

The Wire Edit toolbar is pinned to the left of the main window. It contains the following widgets:

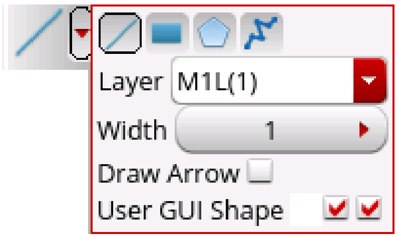
Widget	Description

	*Change Net of Selected Wires* – Use the drop-down menu of the *Change Net of Selected Wires* widget to change the net of a selected wire. To change the net of a selected wire: 1. Click the drop-down next to the Net icon. 2. Type the new net name in the *Nets* text box. Alternatively, click the *Get Selected* button to add the net name of the selected wire automatically to the text box. 3. Press the `Enter` key to implement the net change.  Note that if multiple wires are selected, clicking the *Get Selected* button will add the net name of the last selected wire to the *Nets* text box.
	*Change Layer of Selected Wires* – Use the drop-down menu of the *Change Layer of Selected Wires* widget to change the layer of the selected wire. You can choose the required layer from the horizontal or vertical layer submenus.
	*Change Width of Selected Wires* – Use the drop-down menu of the *Change Width of Selected Wires* widget to change the width of the selected wire. You can specify the required width for horizontal and vertical wires in the submenu.
	*Duplicate Selected Wires* – Duplicates the selected wires on the layer specified in the *Layer* section of *Creation* page in the *Edit Route* form. Press the `Shift` key and click to select multiple wires. The duplicated wires are in the same location as the original. The duplicated wires are selected and the original wires are deselected, allowing you to move the duplicated wires without disturbing the original wires. Equivalent keyboard shortcut: `Shift + C`
	*Split Selected Wires* – Splits selected wires into segments. Wire splits occur at the intersections of wires on the same net. If you delete a section of the split wire so that the remaining wire is only partially connected to another wire, the remaining wire is automatically repaired so it extends to the appropriate edge of the wire to which it connects. Equivalent keyboard shortcut: `Ctrl + S`

	*Merge Selected Wires* – Select wires and click this widget to join all wires of the same width, layer, and net that are collinear with and electrically connected to a selected wire. Does not merge signal wires that contain branches. Equivalent keyboard shortcut: `Shift + M`
	*Trim Selected Wires* – Removes any portion of the selected wire that extends beyond another wire or pin of the same net. Trims the selected wire back to the intersection with the other wire or pin. Equivalent keyboard shortcut: `Shift+T`
	*Delete Wires* – Opens the Select/Delete Routes form. Refer to the "*Select/Delete/Deselect Routes*" section in the Edit Menu chapter of the *Menu Reference* for a detailed description of this form. You can also delete patch wires with this widget. Equivalent keyboard shortcut: `D`
	*Disable Snap* – Click this widget to disable all snap options for wires and vias. Once clicked, the icon for this widget changes to  to indicate that snap is currently disabled. You can use the drop-down menu of the widget to open the Snap Setting form and customize snap settings. Refer to the "*Snap*" section in the Edit Menu chapter of the *Menu Reference* for a detailed description of this form. The recently made snap adjustments are also listed under *Recent* in the drop-down menu. This enables you to quickly toggle between snap settings: 
	*Rotate Selected Wires* - Click this widget to open the Flip/Rotate Selected Objects form and specify the settings for rotating the selected wire.

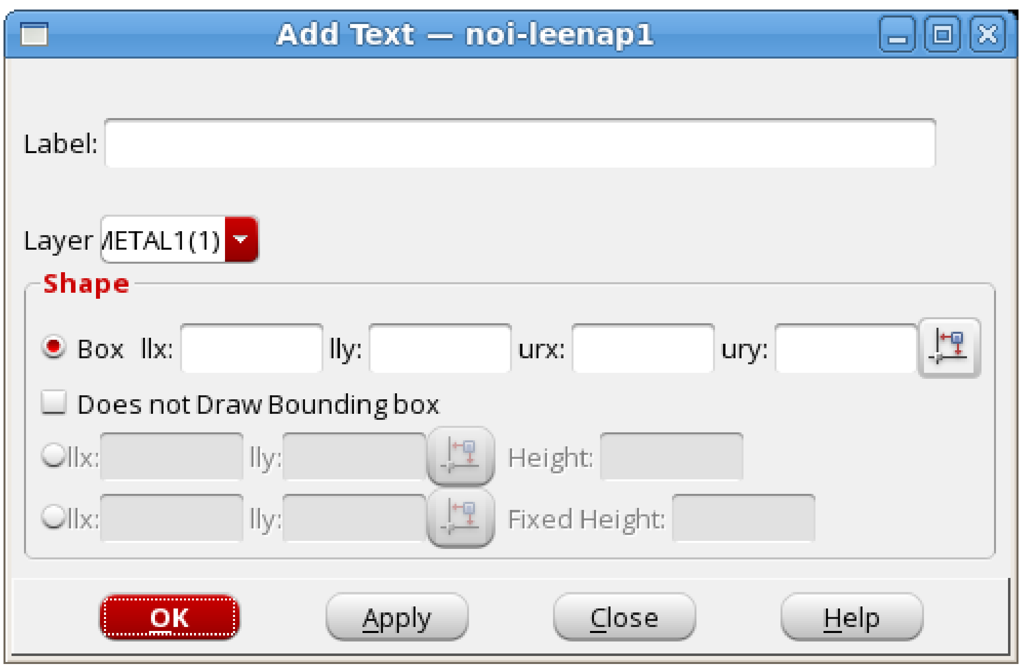


Draw Shapes - Click this widget to add shapes to a specific layer in the layout. The shapes you add through this widget annotate comment shapes and do not show up in a DEF output. You can use the drop-down menu to customize the shape you are adding.

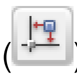


The options in the drop-down menu map to the parameters of the `add_gui_shape` command. Check the *Text Command Reference* for more details.

Add Text - Click this widget to open the Add Text form and specify the settings for adding text labels (annotations) to the specified custom layer. The text added through this form annotates comment text and does not show up in a DEF output.



Add Text Form - Fields and Options

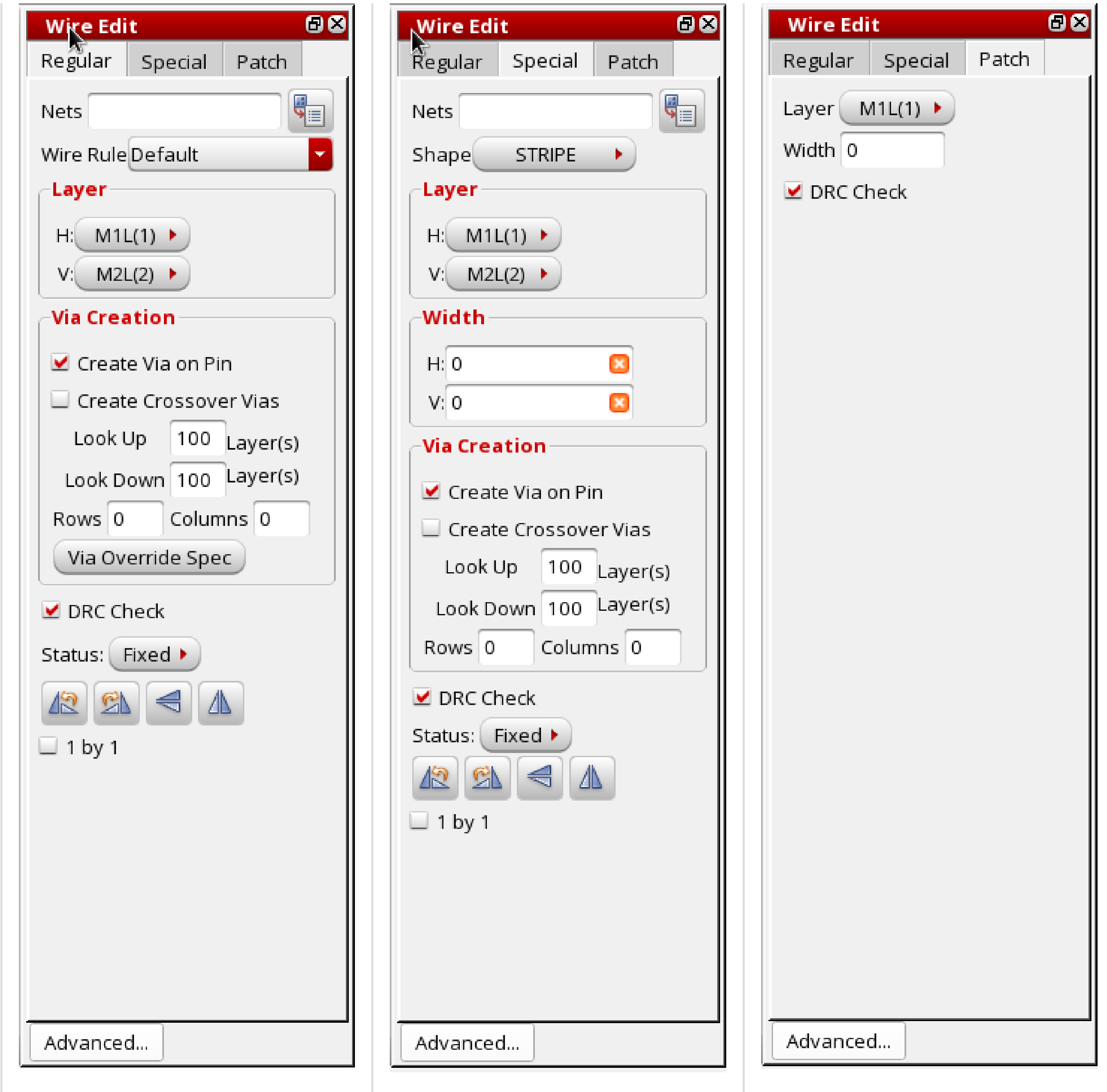
Label	Specifies the text to be displayed. The text can include spaces.
Layer	Specifies the GUI layer name to use or create for the text. If the specified layer does not exist, it will be automatically created.
Box	Specifies the coordinates of the box in which text will be added. The coordinate values are specified in microns in the corresponding coordinate fields. The text is center justified in the box. You can use this option to control the text orientation and size. Click the *Specify area to add text* () button to draw a box in the design area and fetch its coordinates.
Does not Draw Bounding box	Specifies that the bounding box should not be drawn around the text displayed at the specified box coordinates.
llx lly and *Height*	Use this combination to add text of specified height at the specified coordinates. You can specify the height of the text in microns in the *Height* field, which becomes available when you click the corresponding *llx* option button. Specify the origin coordinates of the text in the *llx* and *lly* fields. Alternatively, you can click the *Get Starting Coordinate* () button to select the starting point in the design area and fetch its coordinates.
llx lly and *Fixed Height*	Use this combination to add text of specified height at the specified coordinates. You can specify the height of the text in pixels in the *Fixed Height* field, which becomes available when you click the corresponding *llx* option button. Specify the ending coordinates of the text in the *llx* and *lly* fields. Alternatively, you can click the *Get Ending Coordinate* () button to select the ending point in the design area and fetch its coordinates.

`add_gui_text` is the equivalent text command.

Wire Edit Panel

You can use the Wire Edit panel to customize the settings for adding or editing a wire quickly, without opening the Edit Route form. To open the Wire Edit panel, click the *Edit Wire* () widget on the tool box. You can switch between options for adding or editing a regular, special, or patch wire by using the tabs at the top of the panel.

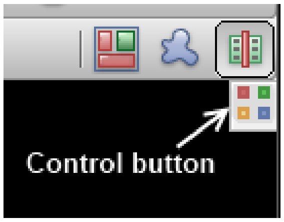
Regular	*Special*	*Patch*



The panel provides all the commonly used options for adding or editing wires. For details on these options, refer to the Edit Route form description in the Edit Menu chapter. You can click the Advanced button at the bottom of the panel to open the Edit Route form.

Control Panel

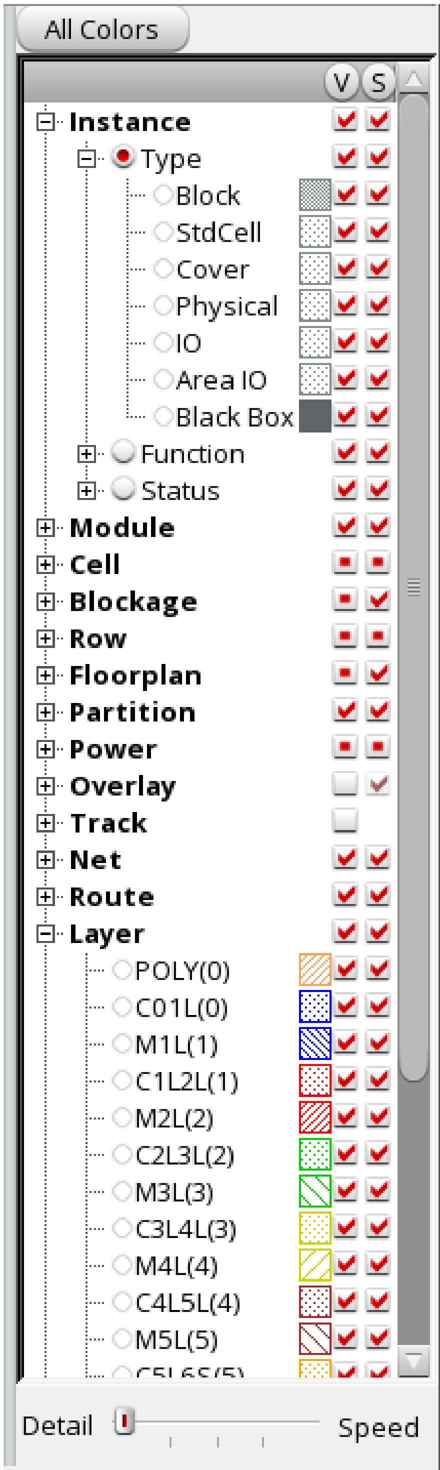
To customize display settings for objects in the design display area, click the *Control* button at the upper right of the display area, just below the toolbars. This displays the control panel.



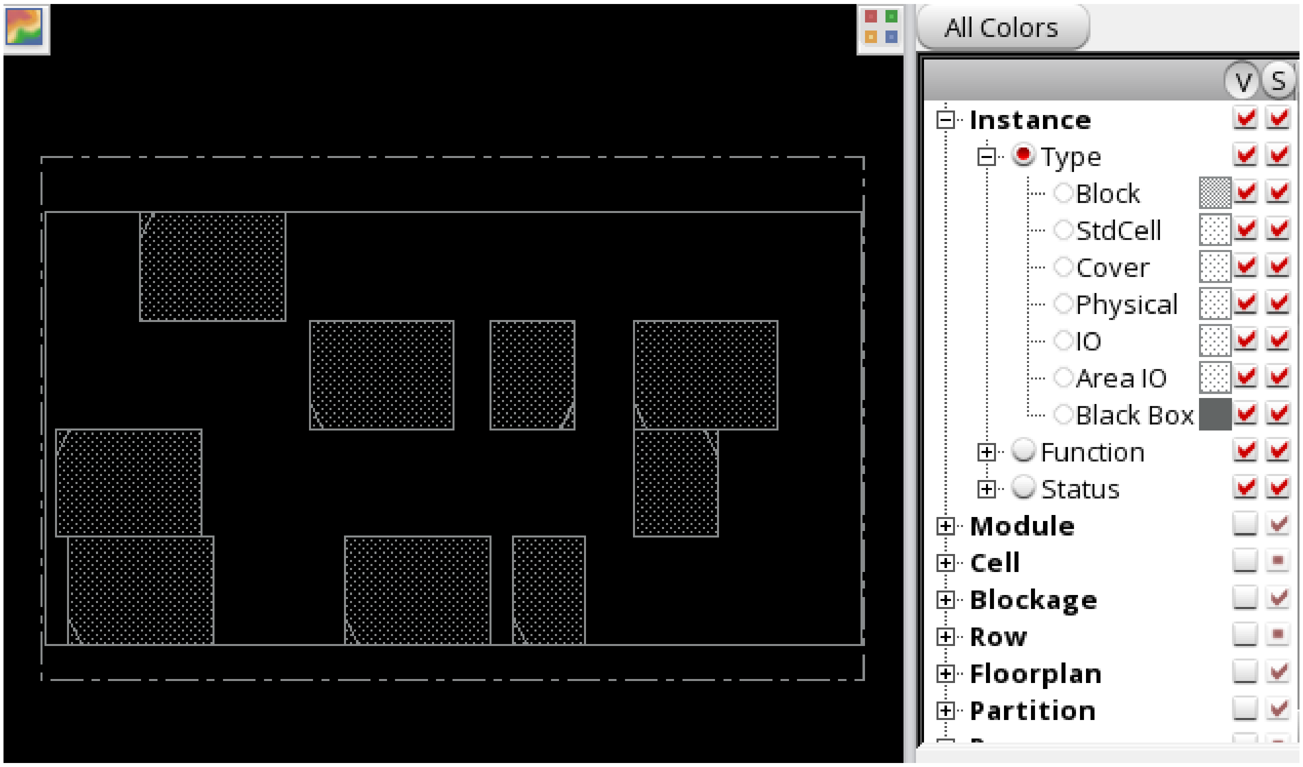
The control panel has color, visibility, and selectability settings for objects in the design display area. Each object type can have a color button that displays the current color used to identify the object in the design display area, a visibility (*V*) check box for displaying the object in the design display area, and a selectability (*S*) check box for controlling selection of that object type in the design display area.

By default, the control panel displays related objects in groups. This way you can view the color, visibility, and selectability controls for related objects together. You can use the Customize Tab form to add or delete groups, and to add objects in each group. The Customize Tab form is available from all pages of the Color Preferences form. For more information, see Customize Tab.

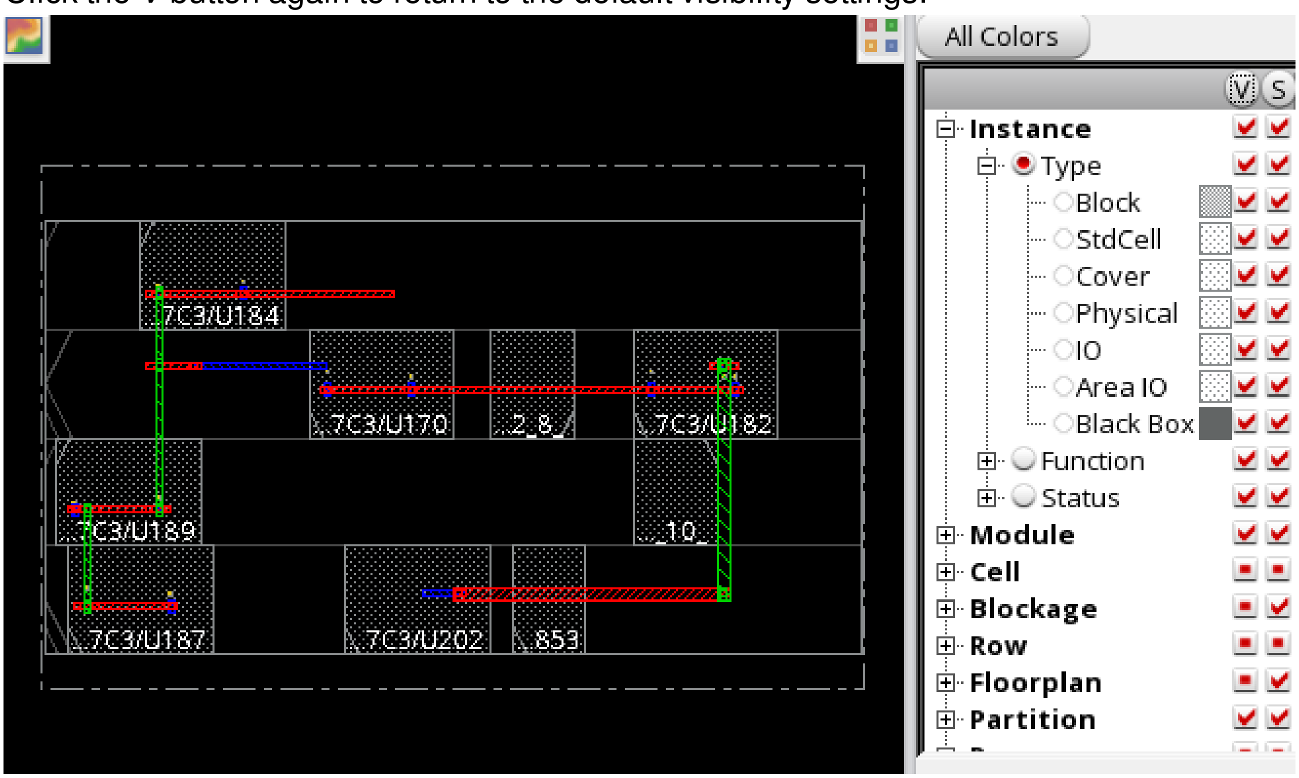
Note: You can right-click on an individual layer to toggle the visibility/selectability of all objects on the layer.



- You can use the *V* and *S* buttons at the top of the control panel to turn on or off the visibility and selectability of all objects with one click. For example, click the *V* button to turn off visibility of all objects. You can now turn on visibility of a specific object type, such as *Instance*:



Click the *V* button again to return to the default visibility settings:



- If you select the visibility check box for an object type, the object type displays in the design display area in the specified color. If you clear the check box, the object type does not display in the design display area. If the visibility check box is cleared for an object type, the corresponding selectability check box is grayed out. Similarly, if you clear the visibility check for an object group, the selectability check boxes for all objects in that group are grayed out.

- If you select the selectability check box for an object type, the object type can be selected in the design display area when you use the *Selection* icon. If you clear the check box, the object type cannot be selected.

  Note: Some object types, such as *Special Nets* under *Nets*, do not have a selectability check box.

You can use the *Detail - Speed* slider at the bottom of the bar to control the display/hide level for instances and nets. In the *Speed* mode, the software ignores the display for net and instances until you zoom in the layout window view to a suitable level. In the *Detail* mode, the software displays net and instances at the default zoom level.

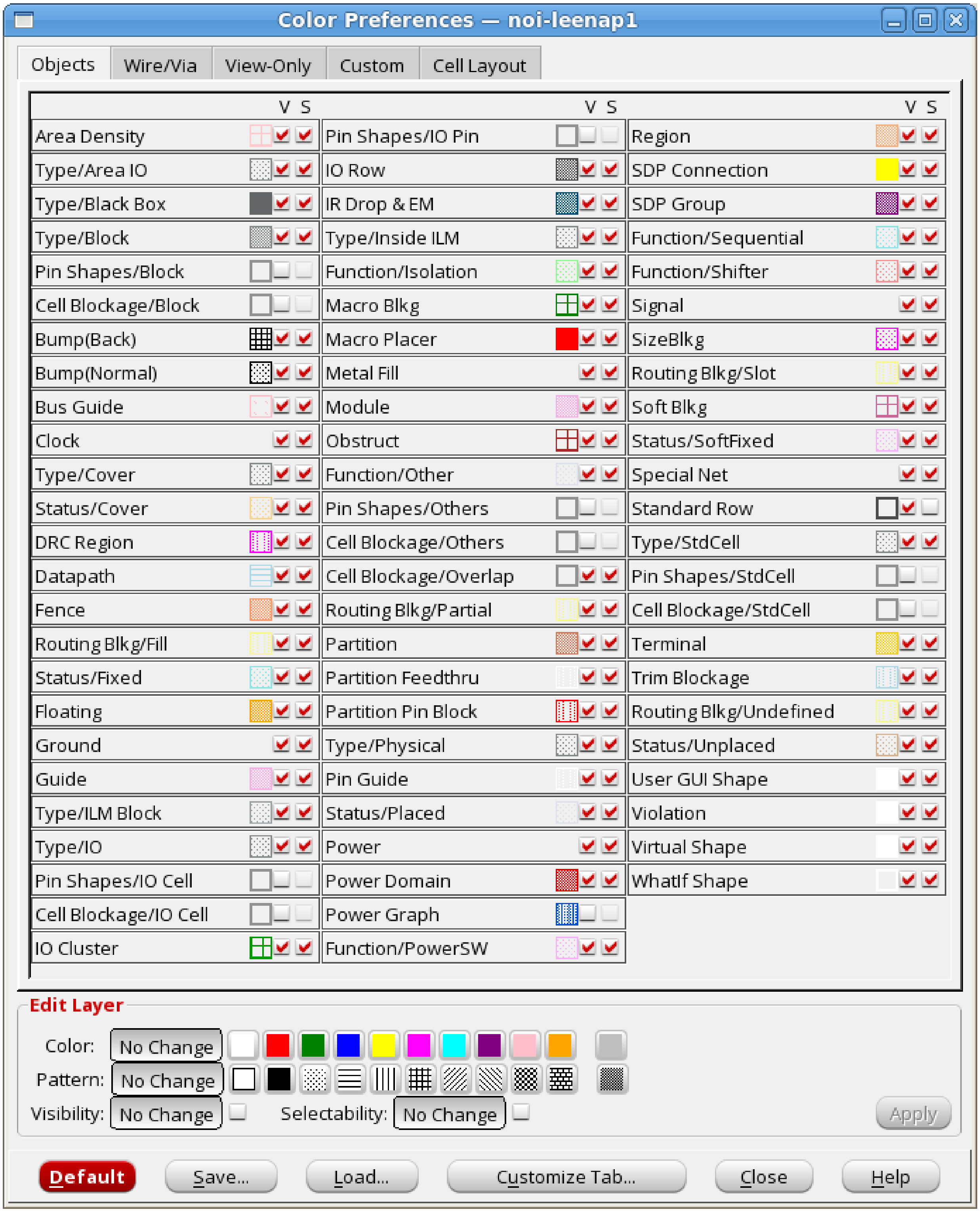
Color Preferences

To set advanced color options, click the *All Colors* button on the control panel to open the Color Preferences form, which has five pages:

- Objects
- Wire/Via
- View-Only
- Custom
- Cell Layout

The visibility settings between the pages and the main window are synchronized. That is, as soon you change any setting on any page, the corresponding changes are applied in the main window. For example, if you change the visibility setting of blackboxes, the changes are immediately applied to any blackboxes in the main window.

Objects Page



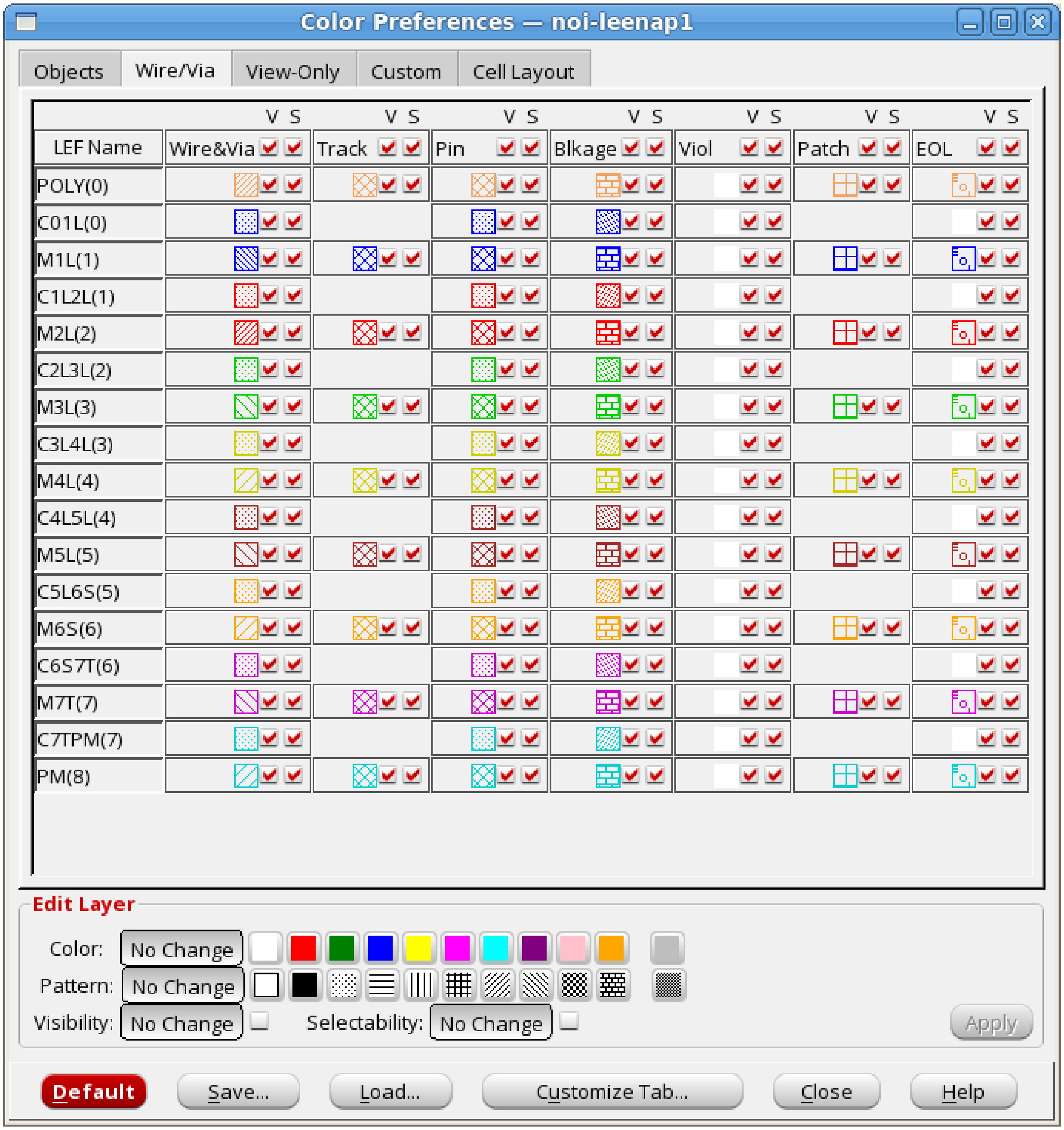
The Objects page includes the visibility and selectability controls for objects that can be viewed and selected. Each object type has the following features:

- A color button that displays the current color and stipple pattern used to identify the object in the design display area. Click the color button to change the color for that object type.
- A check box indicating whether the object type is visible in the design display area.
- A check box for making the object type selectable.
  Note: If an object type does not have a *Selectability* check box, it cannot be selected.

> When you move the cursor over an object layer name, the equivalent database object name is displayed.

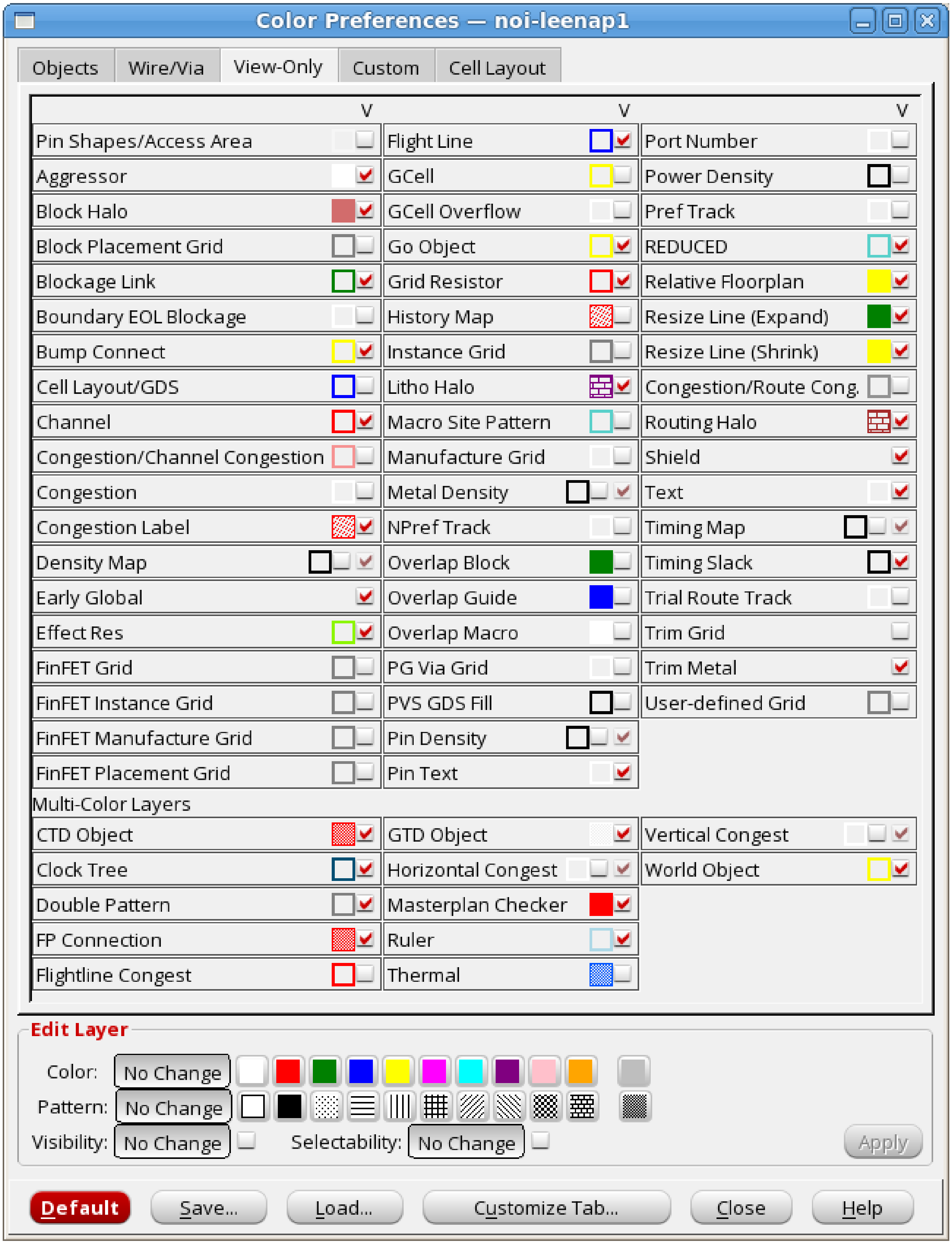
Wire/Via Page

The Wire/Via page includes the visibility and selectability controls for layer-based objects: Wires and vias, Tracks, Pins, Blockages, Violations, Patch wires, and EOL blockages. You can set global display controls for all objects on the same layer. You can also set controls for individual objects on specific layers.



View-Only Page

The View-Only page includes the visibility controls for objects that can be viewed but not selected in the Innovus main window.

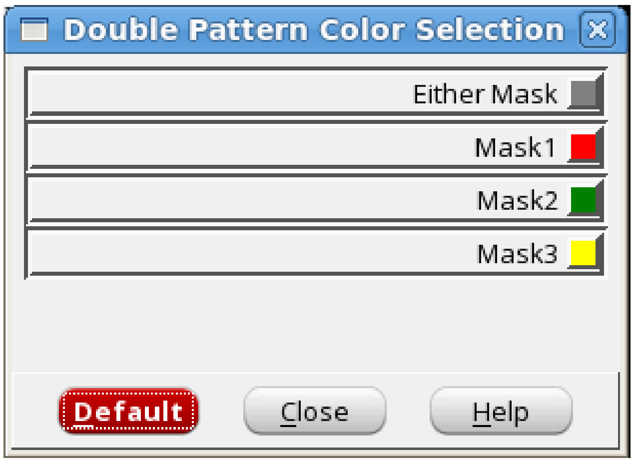

Color Preferences — noi-leenap1
Objects
Wire/Via
View-Only
Custom
Cell Layout
V
V
V
Pin Shapes/Access Area
Aggressor
Block Halo
Block Placement Grid
Blockage Link
Boundary EOL Blockage
Bump Connect
Cell Layout/GDS
Channel
Congestion/Channel Congestion
Congestion
Congestion Label
Density Map
Early Global
Effect Res
FinFET Grid
FinFET Instance Grid
FinFET Manufacture Grid
FinFET Placement Grid
Flight Line
GCell
GCell Overflow
Go Object
Grid Resistor
History Map
Instance Grid
Litho Halo
Macro Site Pattern
Manufacture Grid
Metal Density
NPref Track
Overlap Block
Overlap Guide
Overlap Macro
PG Via Grid
PVS GDS Fill
Pin Density
Pin Text
Port Number
Power Density
Pref Track
REDUCED
Relative Floorplan
Resize Line (Expand)
Resize Line (Shrink)
Congestion/Route Cong.
Routing Halo
Shield
Text
Timing Map
Timing Slack
Trial Route Track
Trim Grid
Trim Metal
User-defined Grid
Multi-Color Layers
CTD Object
Clock Tree
Double Pattern
FP Connection
Flightline Congest
GTD Object
Horizontal Congest
Masterplan Checker
Ruler
Thermal
Vertical Congest
World Object
Edit Layer
Color:
No Change
Pattern:
No Change
Visibility:
No Change
Selectability:
No Change
Apply
Default
Save...
Load...
Customize Tab...
Close
Help

Double Pattern Color Selection

Use the Double Pattern Color Selection form to configure the Double Pattern Technology (DPT) colors.

To open the Double Pattern Color Selection form:

1. Click the *All Colors* button in the main window to open the Color Preferences form.
2. Open the *View-Only* page.
3. Click on the color indicator box for the Double Pattern object.



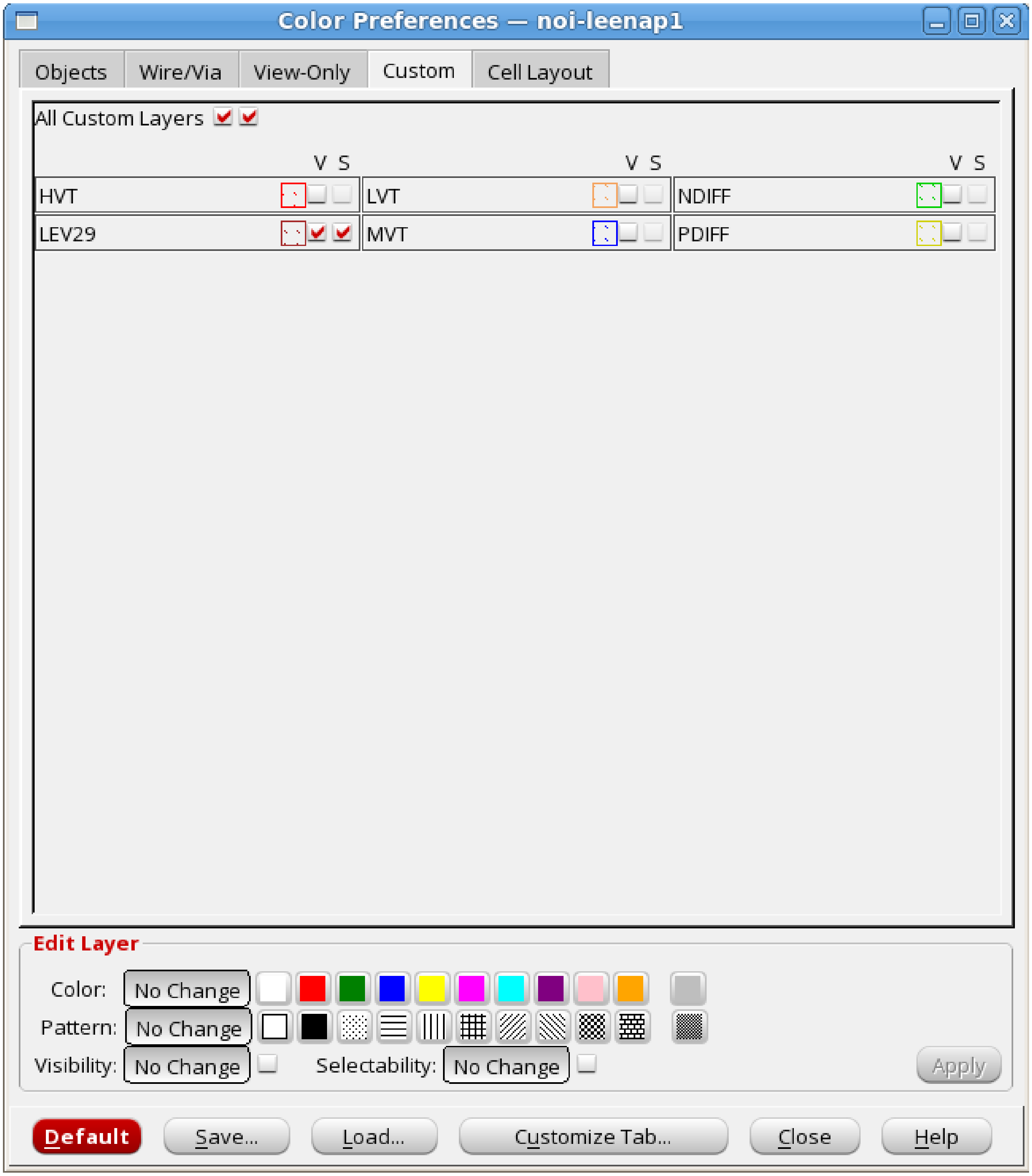
Click the color indicator next to any of the options to select a different color in the Select Color form.

Custom Page

The Custom page contains custom objects. These objects are either imported through the GDS file or created using the Custom Object Editor, accessible through *Edit - Custom Object Editor* menu.

In designs having a large number of custom layers, turning off layers one by one can be difficult when you want to focus on a specific layer in the design. In such cases, you can first use the *All Custom Layers* option to disable all layers. Then, you can select the *Visibility* and *Selectability* toggles of only the specific layer on which you want to focus.

To select a group of objects that are to have the same color and fill pattern, `Shift`-click the first and last objects in the group, click the new color and the new fill pattern, then click *Close.*

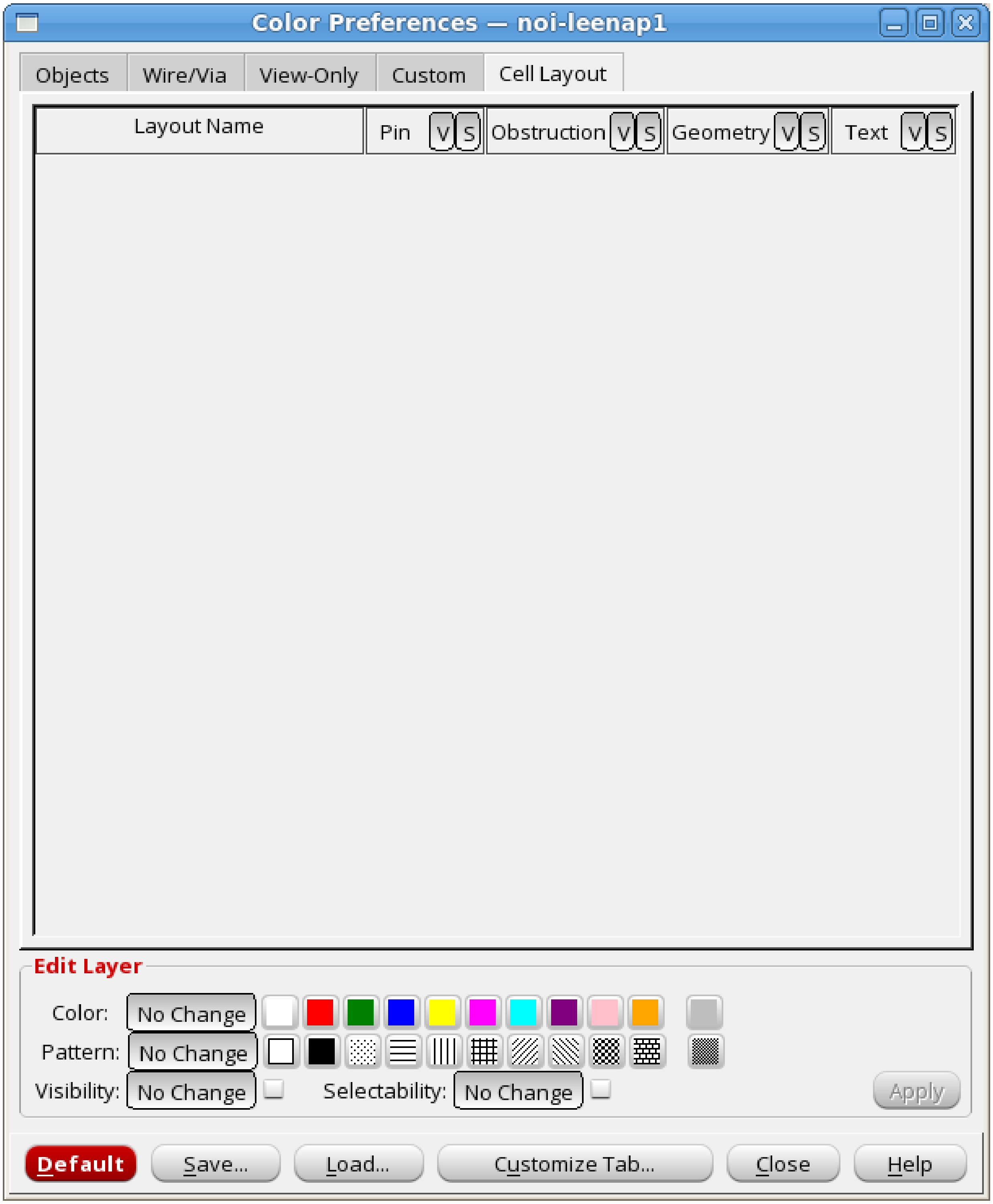

Color Preferences — noi-leenap1
Objects
Wire/Via
View-Only
Custom
Cell Layout
All Custom Layers
V S
HVT
LEV29
LVT
MVT
NDIFF
PDIFF
Edit Layer
Color:
No Change
Pattern:
No Change
Visibility:
No Change
Selectability:
No Change
Apply
Default
Save...
Load...
Customize Tab...
Close
Help

Cell Layout Page

Use the Cell Layout page to set the color settings for the OpenAccess cell layout in designs that support an OpenAccess database.

To enable the OpenAccess layout view, enable the visibility of the *Cell Layout* option in the *Cells* category on the control panel bar in the main window or in the *View-Only* page in the Color preferences form.

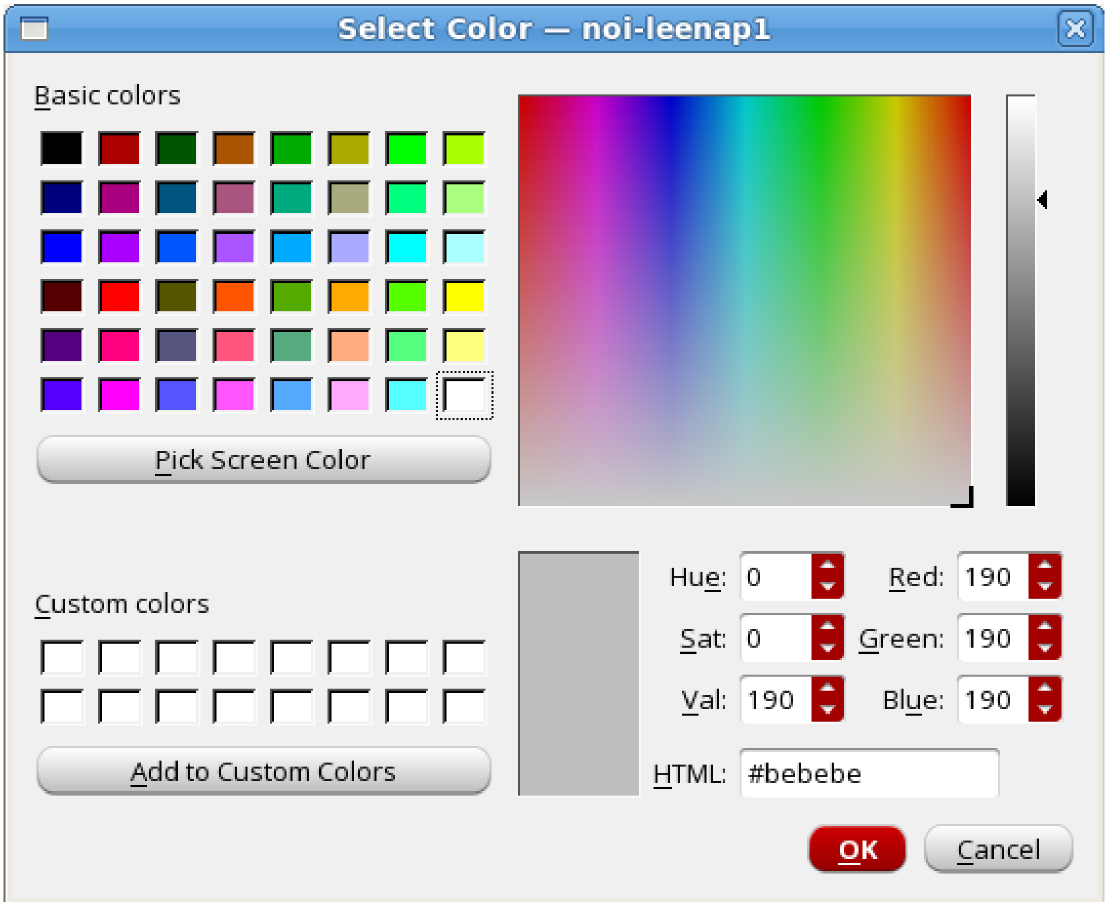
To select the cells whose layout should be displayed, use the Cell Layout Preference form, which can be accessed from the *Design* page of the Preferences form.


Color Preferences — noi-leenap1
Objects
Wire/Via
View-Only
Custom
Cell Layout
Layout Name
Pin V S
Obstruction V S
Geometry V S
Text V S
Edit Layer
Color:
No Change
Pattern:
No Change
Visibility:
No Change
Selectability:
No Change
Apply
Default
Save...
Load...
Customize Tab...
Close
Help

Select Color

Use the Select color form to customize the display color of an object

- Click the color indicator of the object type to open the Select color form.

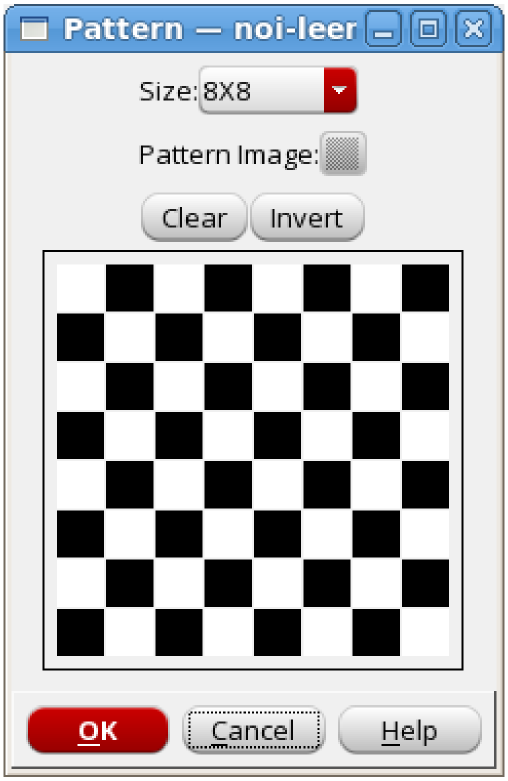


ⓘ If you use the text fields, you must press the `Return` key after your text entry.

Customizing Layer Color Patterns

You can customize the color patterns for the layers by clicking the Custom pattern icon in the Edit Layer group. The Custom pattern icon is the rightmost icon in the Pattern field.

- Click the Custom icon to display the Pattern form.

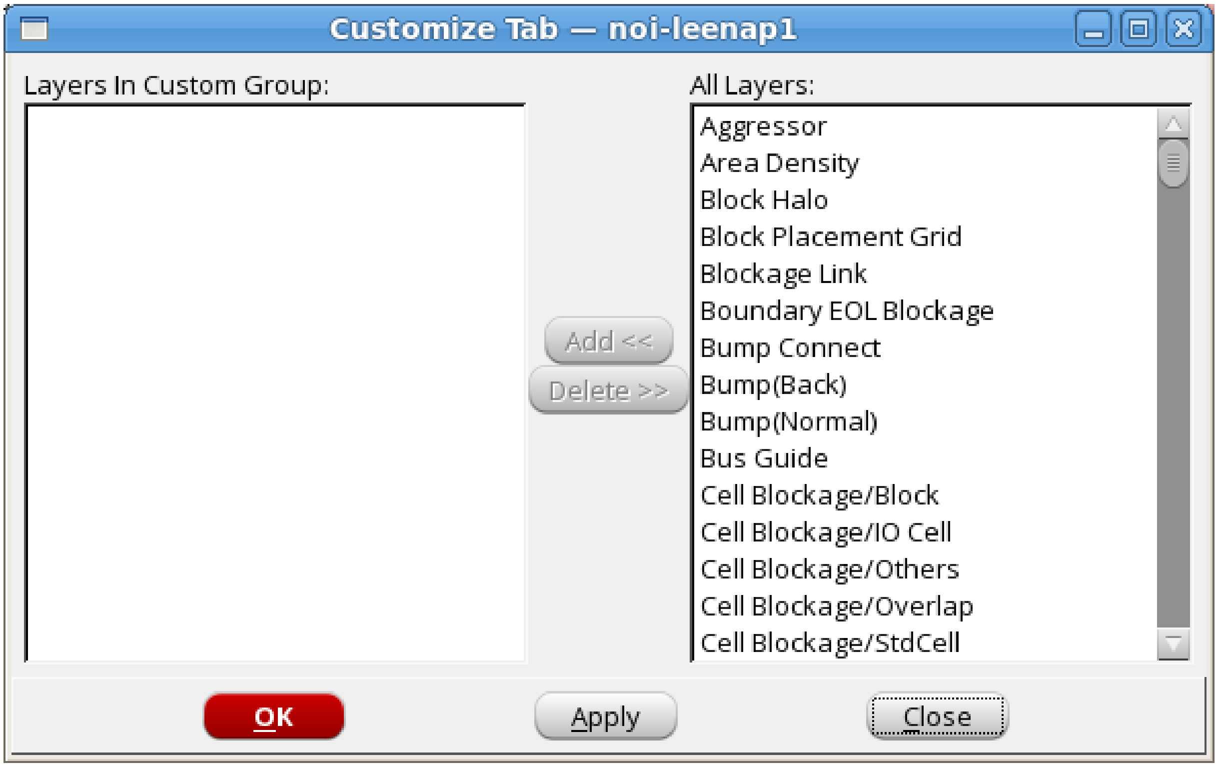


- To clear the pattern, click the *Clear* button.
- To invert the pattern, click the *Invert* button.
- To customize the pattern, do the following:
  - To change a square to black color, click on the square with the left mouse button.
  - To change a square to white color, click on the square with the right mouse button.

Customize Tab

You can use the Customize Tab form, accessible by clicking the *Customize Tab* button in any page on the Color Preferences form, to customize or add custom groups to the Control Panel on the main window.

- On any page of the Color Preferences form, click the *Customize Tab* button.



Customize Tab Form - Fields and Options

All Layers	Displays a list of all objects that you can add to a group.
Add <<	Adds the object currently selected in the *All Layers* list to the *Layers in Custom Group* list.
Layers in Custom Group	Lists the objects that are in the custom group you are creating.
Delete >>	Removes the object currently selected in the *Layers in Custom Group* list.

After you click *OK* or *Apply*, the new group is added to the *Control Panel* on the right of the main window.

Applying Preferences in the Color Preferences Form

After making changes to the Color Preferences form, you can perform the following actions:

- To apply the changes in visibility, selectability, color, and stipple pattern to objects in the design display area, click *Close*.

- To save a color preference file, click *Save*. For more information, see Save Color Preference.
- To load a preference file, click *Load*.

Save Color Preference

Use the Save Color Preference form to save a color preference file. A preference file is a Tcl file that contains color preference information and preference information from the Preferences form (*View - Set Preference*). The recommended filename and extension name is `gui.color.tcl`.

In the Color Preference form, click *Save*.

Save Color Preferences Form--Fields and Options

Save to Home Directory	Saves the color preferences file in your home directory.
Save to Current Directory	Saves the color preferences file in the current working directory.
Save to a File	Saves the color preferences file in the specified location.
Include Customize Tab Setting	
	Along with the color preference information, also saves the settings specified through the *Customize Tab* form.

Multicolor Layers

During a design session, some object types do not have a single color, but each object has a color that shows a level of severity and magnitude. Examples of such object types are:

- *Horizontal Congest*
- *Vertical Congest*
- *IR Drop or EM*
- *Clock Tree*

To see the level indicator colors, double-click the color button for the object type. This opens a color preferences form for that object type.

Metal Layers and Other Layered Components

Click the *Wire/Via* tab to see the metal layers available in the design. The vias are also shown, with *V01* representing the via between the masterslice layer and the first metal layer, *VIA12* representing the via between the first and second metal layers, and so on.

You can set preferences for other layered components in addition to wires and vias. For each metal layer, you can set the color, stipple pattern, visibility, and selectability for pins, tracks, blockages, and violations.

Using the Layout 3D View

Innovus supports the Layout 3D view from the 18.10 release. The following sections describe the requirements, benefits, and usage model of the Layout 3D view.

Supported Environment for Layout 3D View

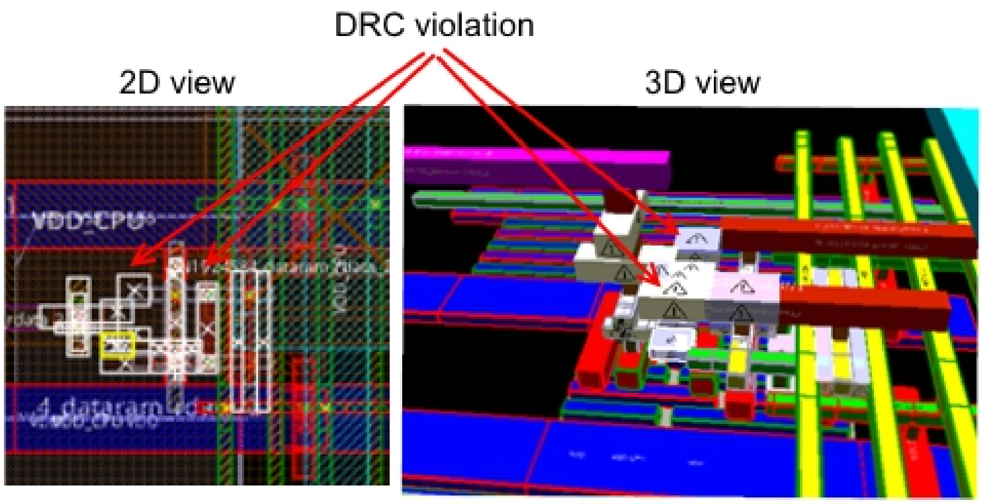
The following requirements must be met for the Layout 3D view to work correctly:

- Open Graphics Library (OpenGL) 1.2 or higher
- One of the following clients: VNC, NX, or EOD. Layout 3D works best with VNC currently.
- Design area to be viewed in 3D must have less than 20000 objects

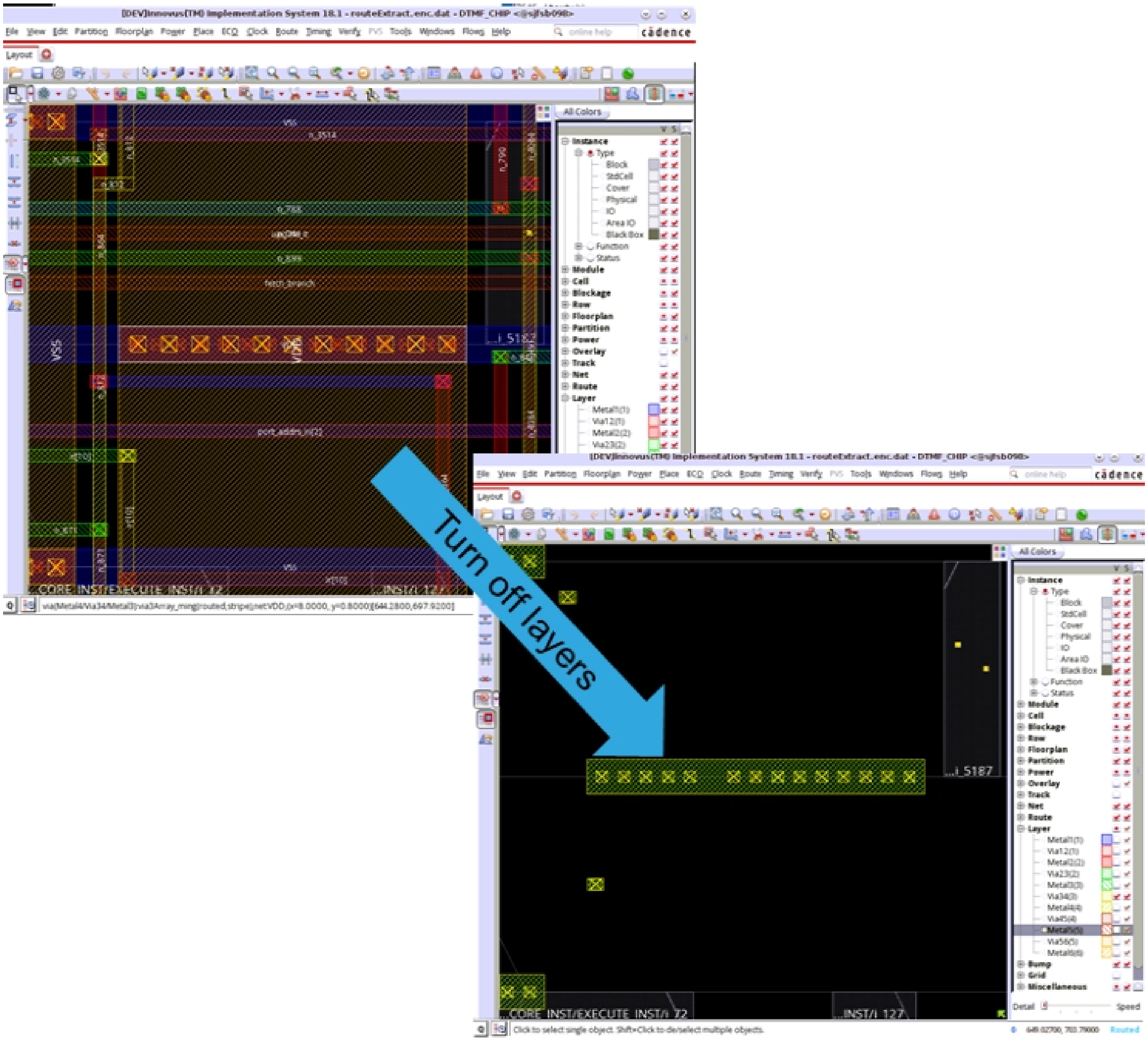
Advantages of the Layout 3D View

The Layout 3D view offers several advantages over a 2D view:

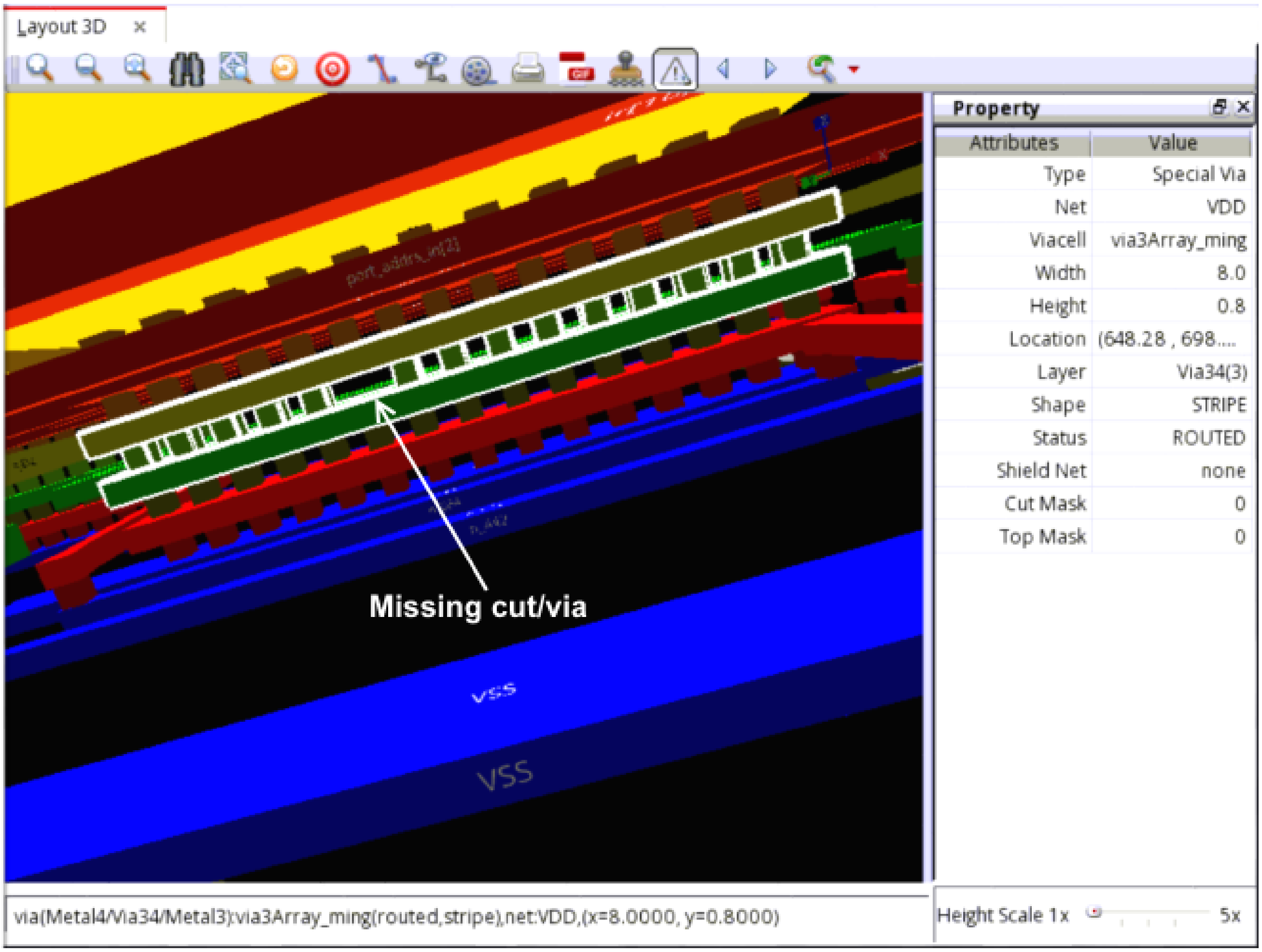
- **Better representation of multi-layer DRC violations**: If your design has several, multi-layer DRC violations in a small area, the 2D view displays these violations as overlapping DRC markers at the same spot. In contrast, a 3D view helps you see the DRC violations much more clearly by displaying each DRC violation as a blinking cuboid.



- **Easier identification of a missing via or cut in the PG structure**: In the 2D view, you may be able to spot a missing via or cut only when you turn off other layers.

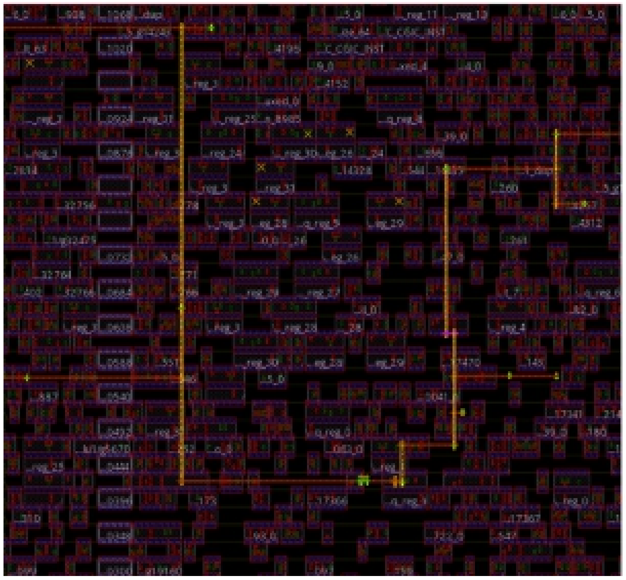


In the Layout 3D view, you can spot a missing via or cut much more easily:

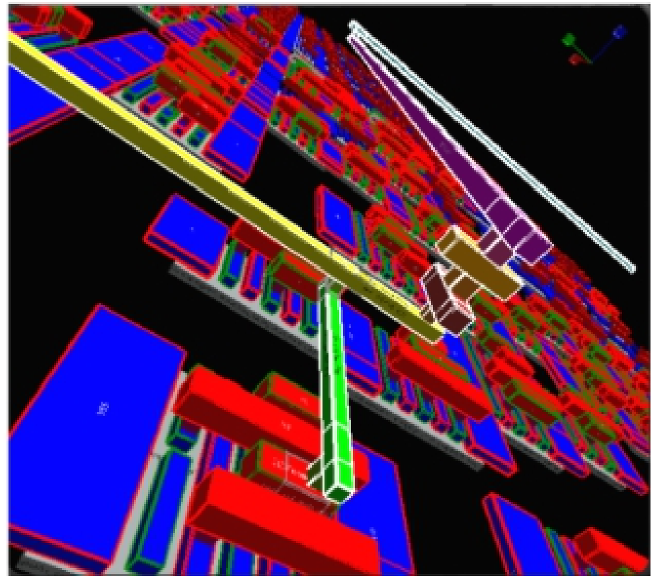


- **Better representation of single net routing**: In the Layout 3D view, the net is represented as a waterfall, making it easier for you to study the routing.

2D view

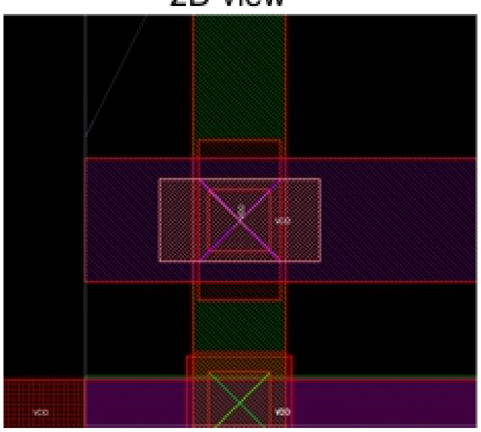


3D view

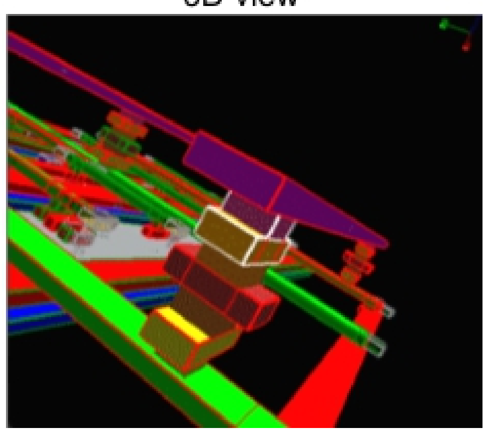


- **Better representation of complex routing shapes**: Complex routing shapes, such as stacked vias, via pillars, and shielding nets, are represented better in 3D space as shown below:
  Stacked via

2D view

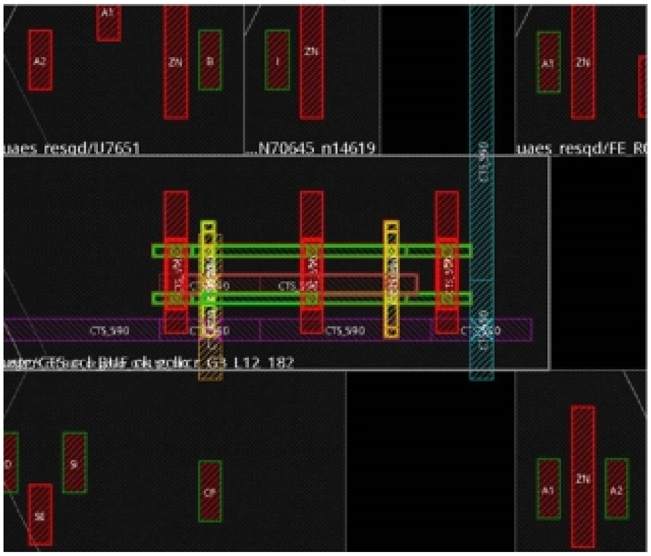


3D view

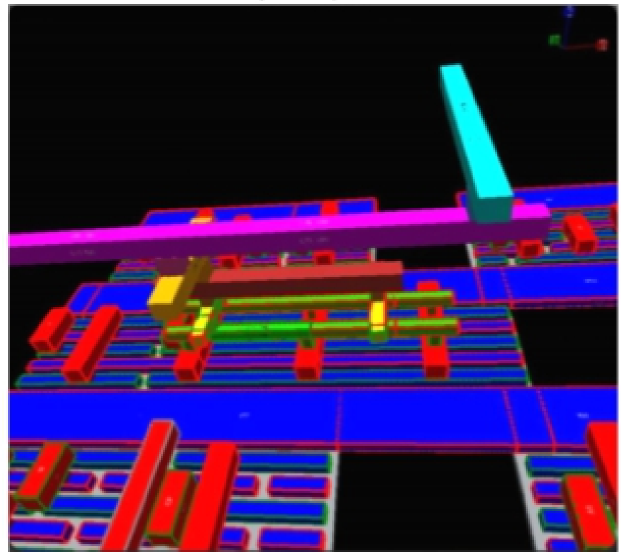


Via pillar

2D view

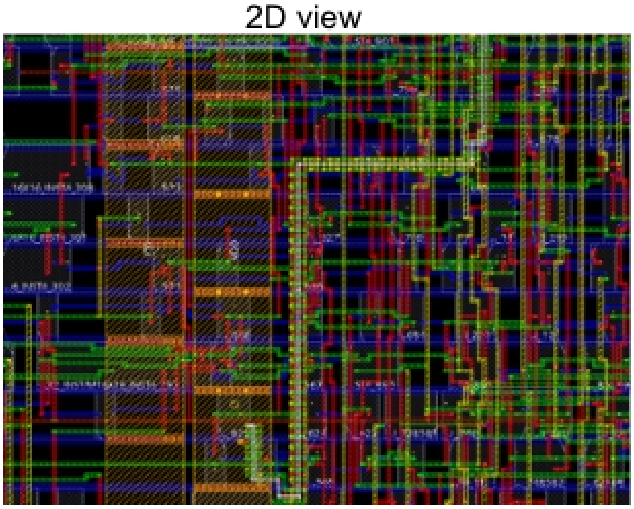


3D view

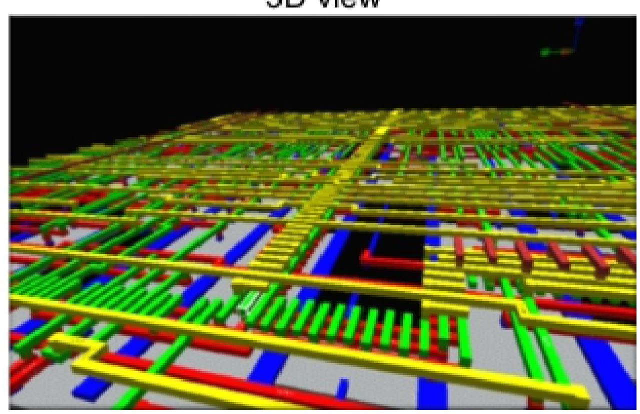


Shielding net

2D view

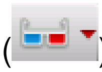


3D view



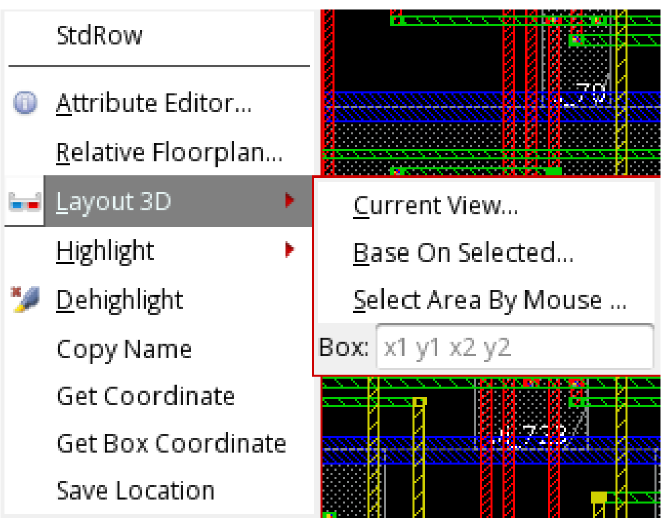
- **Support for cross-probing with 3D GDSII viewers**: Open-source 3D GDSII viewers cannot be used for cross-probing with the 2D layout. These open-source viewers are supported in the Layout 3D view.

Opening the Layout 3D View

You can launch the 3D view of the layout by using the *Layout 3D* widget () on the *Design View* toolbar. You can select one of the following options from the drop-down menu of the *Layout 3D* widget:

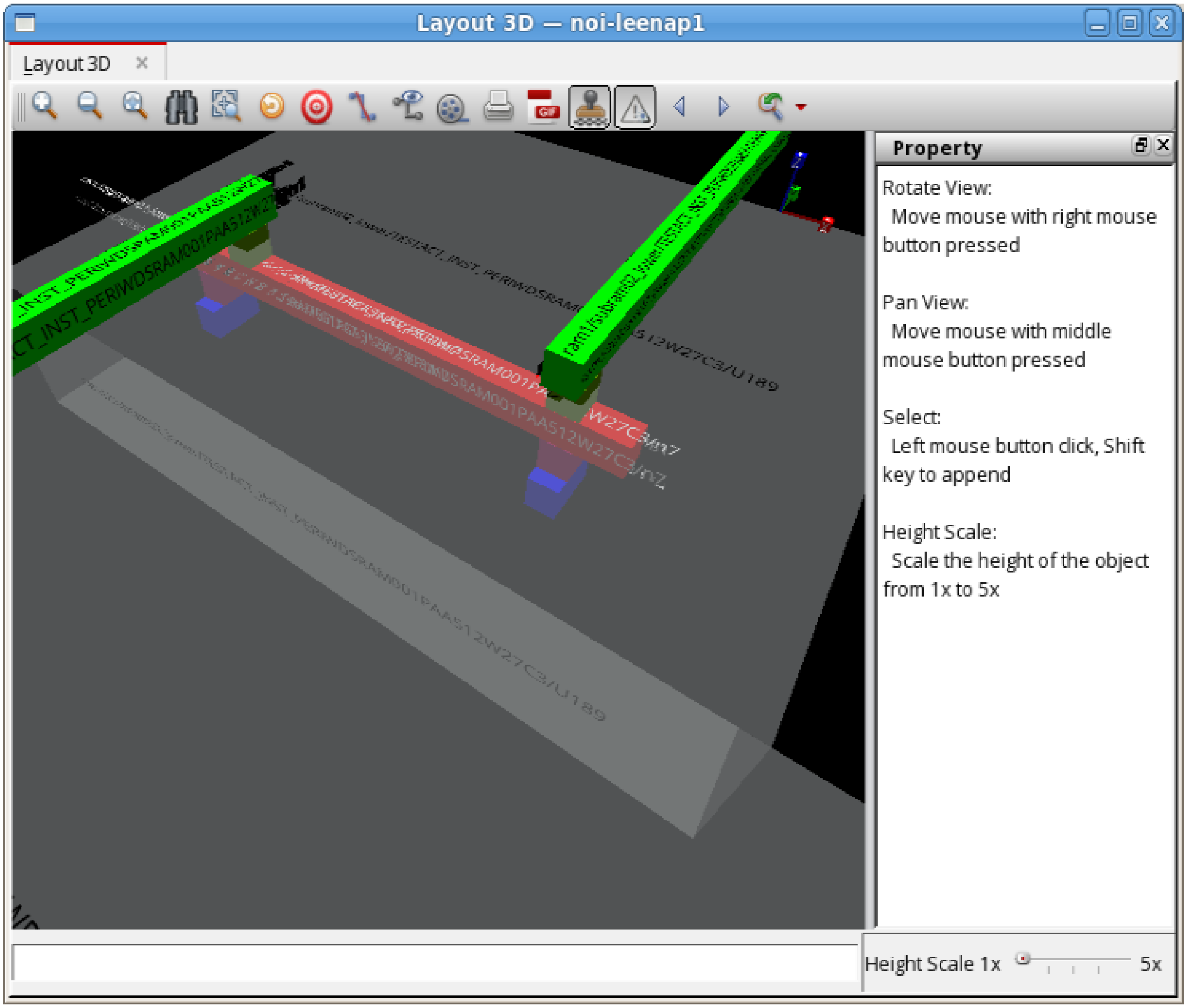
- *Current View*: Generates a bird's eye view of all objects that are currently visible in the design display area of the main window.
- *Base On Selected*: Generates a 3D view around the objects that are currently selected in the main window.
- *Select Area By Mouse*: Generates a 3D view of the area you select in the main window by drawing a box.
- *Box*: Generates a 3D view of the area enclosed by the box coordinates you specify.

Alternatively, you can launch the 3D view of the required area by right-clicking the layout in the main window, clicking *Layout 3D* in the context menu, and then selecting one of the options from the submenu.



This opens the 3D view of the specified area in the Layout 3D window:

Layout 3D Window



Note: The Layout 3D view is currently supported only for design areas containing less than 20,000 objects. When you select one of the *Layout 3D* options, the tool checks whether this criterion is met before launching the 3D view.

The Layout 3D window supports cross-probing with the main window. They share the same layer control, status bar, selection set, property panel and query information.

Supported Objects

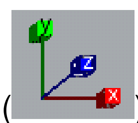
The following objects are currently supported in the Layout 3D view:

- Blockages

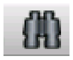
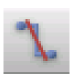
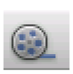
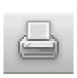
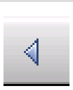
- Bumps
- Cell pin shapes
- Instances
- Object mask/color
- Routing track
- Violation markers
- Wires and vias

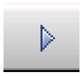
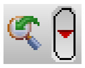
Layout 3D Window - Components and Options

The Layout window has the following components:

- *3D Display Area* - This is the area where the 3D view is displayed. Click to select an object. You can press the `F12` key to dim the background so that the selected object can be seen clearly.
- *Coordinate Axis* () - The *Coordinate Axis* is displayed at the top-right corner of the *3D Display Area*. It acts as a reference to the absolute coordinate's system. Click on the boxes at the end of an axis line to align the camera with the view along that axis.
- Property window - Displays the attributes of the object currently selected in the display area. If no object is selected, this window displays tips for using the mouse to adjust the view.
- *Height Scale* - Adjusts the layer height. The range is 1x to 5x.
- *Status Bar* - Displays the name of the selected object or hints for the next action.
- *Toolbar* - Displays various widgets that can be used to customize the view in the *3D Display Area*. The following table describes the widgets on the toolbar:

Widget	**Description**
	*Zoom In* – Click this widget to display a smaller area of the design in greater detail. The equivalent bindkey is `z`.
	*Zoom Out* – Click this widget to display a larger area of the design in less detail. The equivalent bindkey is `Shift+Z`.

	*Zoom to Full Window* – Fits the screen to the original bird's eye view of the area. The equivalent bindkey is `f`.
	*Zoom Layout View* – Zooms to make the 2D view port same as the 3D view's fit screen view port. The equivalent bindkey is `Shift+F`.
	*Zoom Selected* -- Zooms on to the selected object based on its size, and also focuses the camera on its position. The equivalent bindkey is `o`.
	*Reload View* – Reloads the 3D view based on the original view box. Use this widget to reload the 3D view after you delete objects in the 2D view in the main window. The equivalent bindkey is `Ctrl+R`.
	*Target On Selected* – Centers the selected object and focuses the camera on its position. You can rotate the view around the selected object. If any other operation is applied, the camera will keep the previous target point until the next *Target On Selected* or *Zoom Selected* operation. The equivalent bindkey is `t`.
	*Hide Selected* – Hides the selected object. The equivalent bindkey is `h`.
	*Show All, Dehide All* – Shows all hidden objects. The equivalent bindkey is `Shift+H`.
	*Auto Revolving for Demo* – Automatically rotates the view around the selected objects. Click the widget again to stop.
	*Snap Shot* – Saves the 3D view as a `.png` file. You can change the name of the snapshot and the directory in which it is saved in the Save 3D Snap Shot form that opens when you click this icon.
	*Record Demo as GIF* – Records the 3D view animation as an animated `.gif` file. You can change the name of the file and the directory in which it is saved in the Save 3D Demo GIF form that opens when you click this icon. Click the widget again to stop recording.
	*Enable Stipple Display* – Displays the digital stipple of wires and vias. This widget is turned on by default.
	*Enable Violation Blink* – Makes the violation markers blink.
	*Previous Vista* – Change to the previous saved vista. The equivalent bindkey is `p`.

	*Next Vista* – Change to the next saved vista. The equivalent bindkey is `n`.
	*Save Current Vista* – Saves the current 3D view in vista history. The equivalent bindkey is `s`. You can later navigate the vista history by using the *Previous Vista* and *Next Vista* widgets. Alternatively, you can use the drop-down menu of this widget to access previously saved vistas and delete all saved vistas.

In addition to the widgets, you can use various mouse actions to control the view in the *3D Display Area* of the Layout 3D window. See the following table for details:

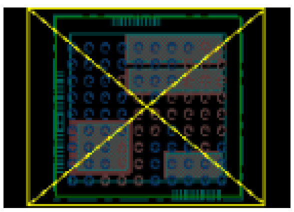
Operation	**Mouse Action**
Selection	Click to select a single object in the display area. Keep the `Shift` key pressed while clicking to add multiple objects to the selection.
Rotating the view	Keep the right mouse button pressed and move the mouse to rotate the view. In addition, you can press the: • `r` key to rotate the view along the X axis. • `y` key to rotate the view along the Y axis. • `p` key to rotate the view along the Z axis.
Focusing the camera while rotating the view	While rotating the view with the right mouse button pressed, press the: • `Ctrl+x` keys to align the camera view along the X axis. • `Ctrl+y` keys to align the camera view along the Y axis. • `Ctrl+z` keys to align the camera view along the Z axis.
Panning the view	Keep the middle mouse button pressed and move the mouse to rotate the view.
Zooming in and out	To zoom in or out, move the scroll wheel of the mouse forward or backward.

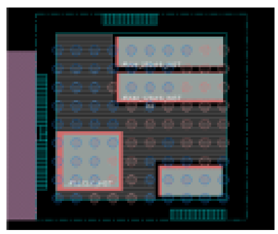
World View

The main window includes a dynamic World View widget, which identifies the location of the current view in the design display area, relative to the entire design. The chip area is replicated in miniature in the design window, and the satellite view is identified by a crossbox. When you display an entire chip in the design display area, the satellite crossbox encompasses the chip area miniature.

The World View widget is auto-hidden by default. Place the cursor over the arrow at the bottom right of the display area to see the World View. You can also pin the World View to the display area by clicking it.

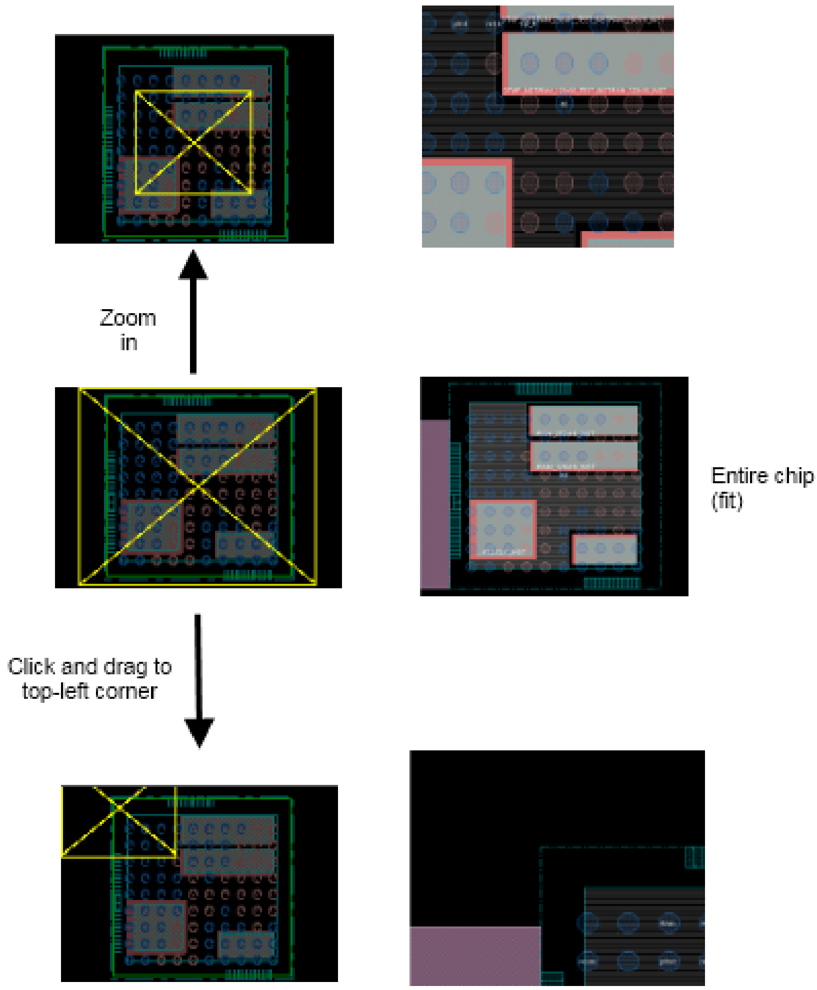
Satellite crossbox
(entire chip)





Design display area
(entire chip)

- When you zoom and pan through the chip in the design display area, the satellite crossbox identifies where you are relative to the entire chip.
- To move to an area in the design display area, click and drag the satellite crossbox.



- To select a new area in the design display area, click and drag the satellite crossbox.
- To resize an area in the satellite window, click with the `Shift` key and drag a corner of the crossbox.
- To define a chip area in the satellite window, right-click and drag on an area.

Attribute Viewers

Attribute Viewers display the basic properties of objects. The Innovus software provide two Attribute Viewers:

- Context Pop-up Attribute Viewer
  The context pop-up attribute viewer displays the basic properties of an object in a pop-up

window right next to the location of the object.

- Property Window
  The Property window displays the basic properties of an object in a fixed window at the bottom right side of the main display area.

You can select either of these Attribute Viewers depending according to your preference. By default, the context pop-up attribute Viewer is enabled.

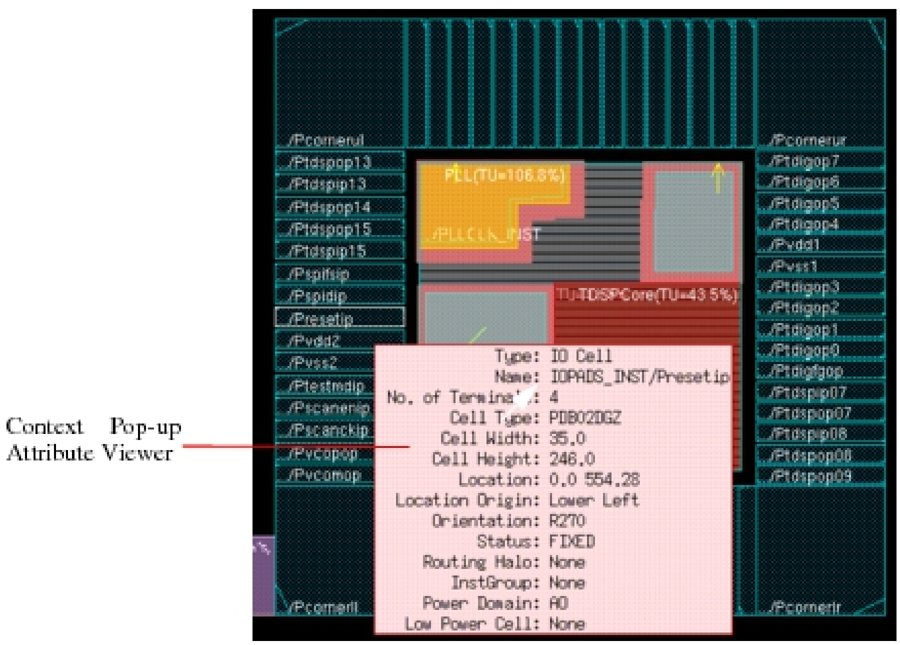
These Attribute Viewers are described in the subsequent sections.

Note: The Attribute Viewers display the basic properties of objects. To view all the properties of an object, open the Attribute Editor by double-clicking the object or by clicking the right mouse button and selecting Attribute Editor from the context menu.

Context Pop-up Attribute Viewer

The context pop-up attribute viewer appears when you hold the cursor over an object. It displays the basic properties of the object.

You can view properties of overlapping objects--use the `n` key to view the next object and the `p` key to view the previous object.



You can turn off the context pop-up attribute viewer by deselecting the Show Attributes Popup checkbox in the Display page of the Preferences GUI, accessible by selecting *View - Set*

Preference from the menu. By default, the Show Attributes Popup checkbox is selected.

Note: If you select the Property Window, the context pop-up attribute viewer is turned off.

Note: For this feature to work, the Auto Query mode (bindkey `Q`) should be enabled.

Property Window

The Property window displays an object's type, name, and attributes. When turned on, the Property window is displayed to the left of the main window. The contents of the Property window change depending on the object selected in the design.

The Property window is off by default. To turn the Property window on, select *View - Set Preference - Windows - Property*. You can show or hide the property window by clicking the icon on its right.

Click on an object in the main display window to retrieve data. You can click the Auto Query button (the *Q* icon located at the bottom of the design display area) to automatically retrieve the data when placing the cursor over the object.

Note: The Property window displays the basic properties of objects. To view all the properties of an object, open the Attribute Editor by double-clicking the object or by clicking the right mouse button and selecting Attribute Editor.

Context Menu

The right-click context menu, which is also referred as the shortcut menu, can be used to access frequently used commands quickly. The context menu commands change depending on the object selected or the cursor location in the main window. Some tasks that can be performed using the context menu are covered below.

Invoking GCD from the Main Window

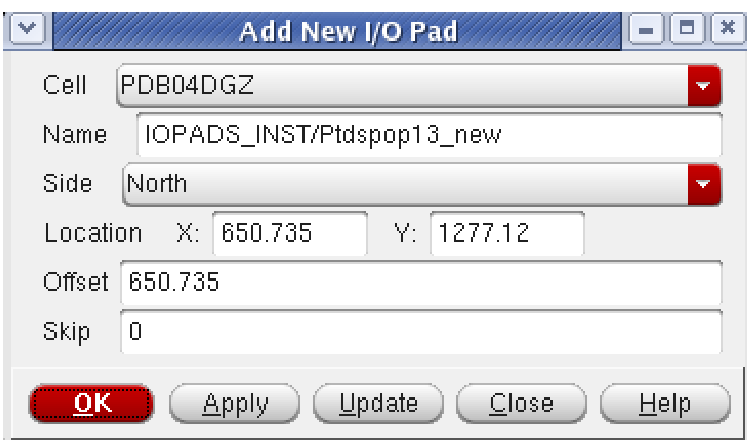
You can easily invoke GCD from the main window by using the context menu.

- Right-click on an instance that is in a clock tree and choose *Invoke GCD* from the context menu.

Adding a New I/O Pad

You can easily pop up the Add New I/O Pad form from the main window by using the context menu.

- Right-click on an I/O Cell and choose the *Add I/O Pad* option.



Add New I/O Pad Fields and Options

Cell	Specifies one or more cells. Adds one I/O for each cell that was specified.
Name	Specifies the instance name prefix for the new I/O. This must match with the number of cells that are specified.
Side	Specifies the side on which the new I/O instance is added.
Location	Adds the new I/O instance at the location specified by lower-left x and lower-left y coordinates.
Offset	Specifies the offsets.
Skip	Skips the number of cells specified, before adding the first I/O instance.

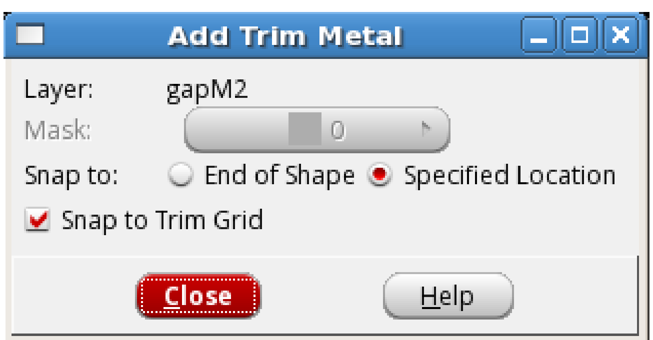
Related Text Commands

`addIoInstance`

Adding Trim Metal

You can add trim metal to a wire easily from the main window.

- Right-click the required wire and select the *Add Trim Metal* option from the context menu.
- Select the required options from the Add Trim Metal form.



Add Trim Metal Fields and Options

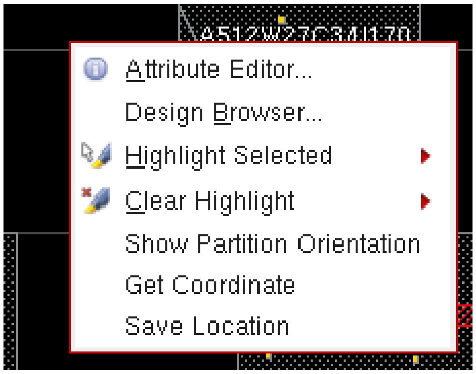
Layer	Displays the layer in which trim metal is being added.
Mask	Specifies the mask value for the trim metal. However, if `USEMETALMASK` is already defined for the trim layer in the tech LEF, you cannot define the mask value here.
Snap to	Specifies the snap options for trim metal. Choose one of the following: • *End of Shape*: Snaps the trim metal to the closest end of the selected shape. • *Specified Location*: Specifies the proximate location of the trim metal. After selecting this option, you can click on the GUI to specify the location. The tool may adjust automatically to the closest location that is best for the trim metal. You can also additionally select the *Snap to Trim Grid* check box, if you want to snap the added trim metal to the nearest trim grid. If you want to add the trim metal centered around a specific location instead of a trim grid, deselect the *Snap to Trim Grid* option.

Related Text Commands

`editAddTrimMetal`

Getting the Coordinates of the Cursor

You can copy the coordinates of the cursor location by using the *Get Coordinate* command from the right-click context menu.



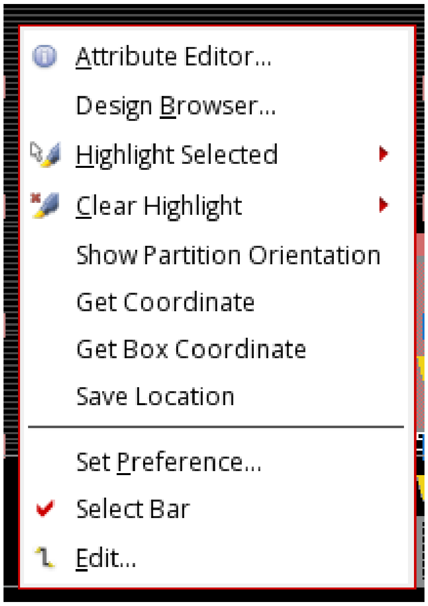
When you select *Get Coordinate*, the cursor coordinates are copied to the clipboard and can be pasted directly at the command prompt.

```
innovus 3> Copied coordinate of cursor {96.053 -642.648} to clipboard.

innovus 3> {96.053 -642.648}
```

Use this feature to specify the value for `-loc` or `-pt` for a command easily.

Getting the Box Coordinates

You can copy the coordinates of the box drawn with the cursor by using the *Get Box Coordinate* command from the right-click context menu.



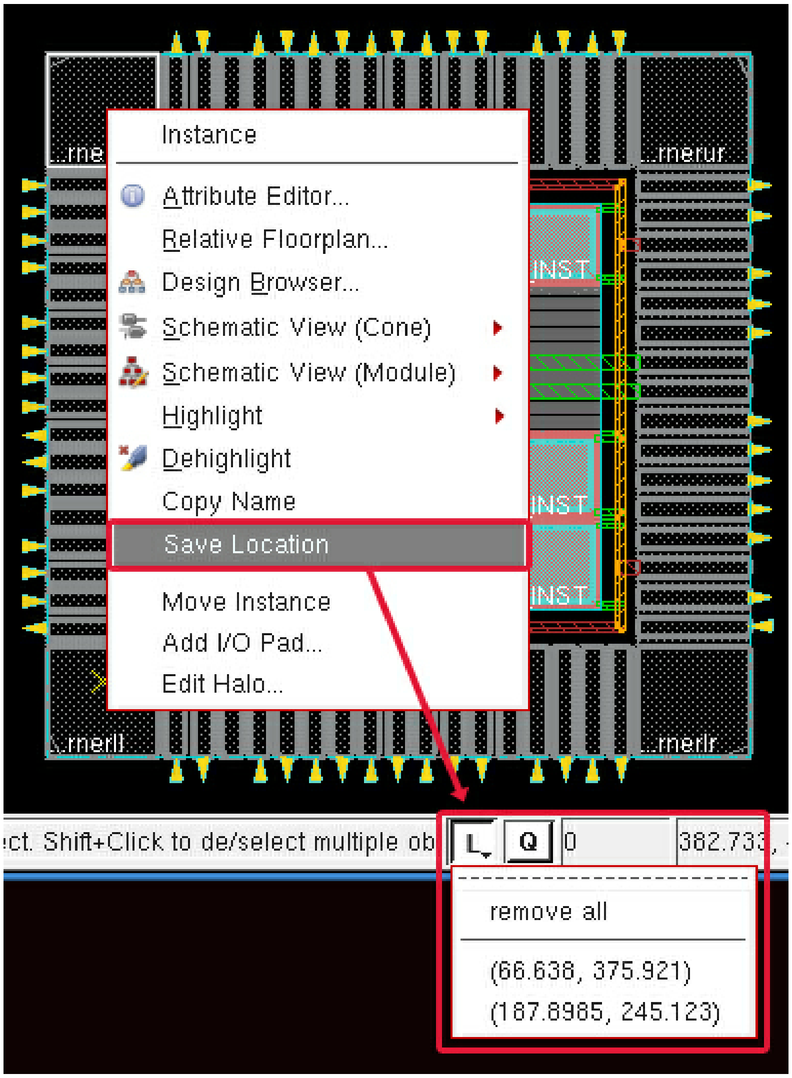
After selecting *Get Box Coordinate*, drag the cursor to draw a box enclosing the required area in the main window. When you complete drawing the box, the box coordinate are copied to the clipboard and the command window.

```
innovus 4> Copied Box of cursor {959.9645 425.9715 1148.23 242.84} to clipboard.
```

Use this feature to specify the value for `-box` for a command easily.

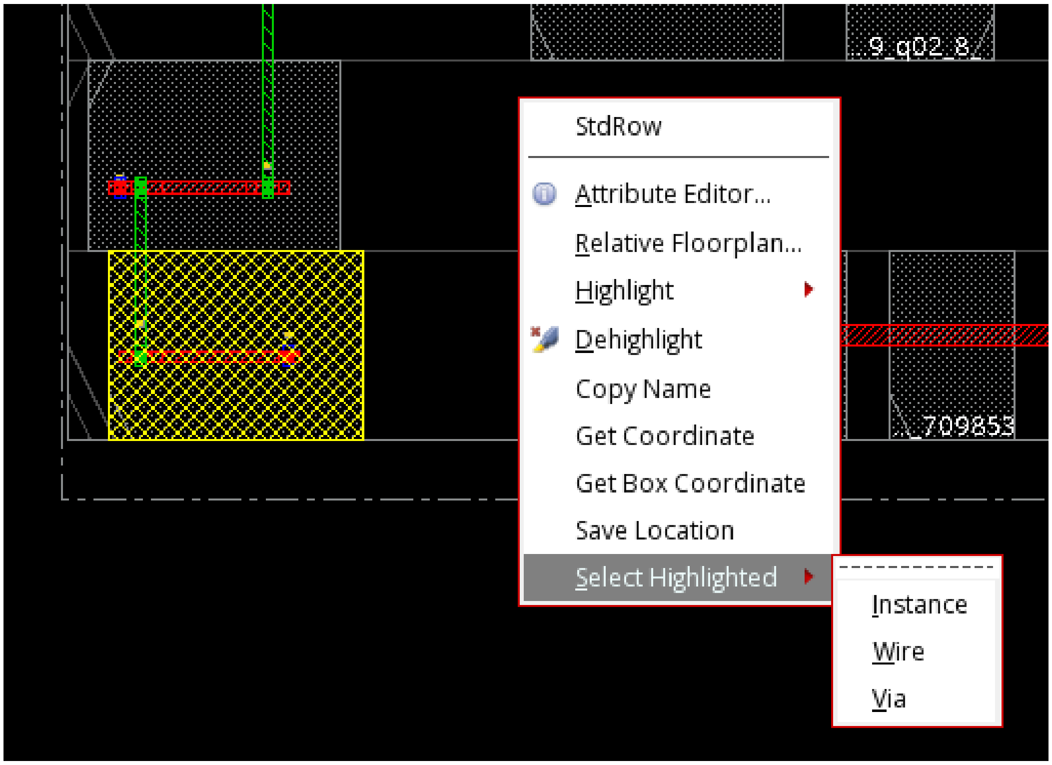
Saving the Coordinates of a Location

You can record the coordinates of a location by using the *Save Location* submenu in the right-click context menu. The saved coordinates can be accessed by clicking the *Location* (L) button located at the bottom of the design display area.



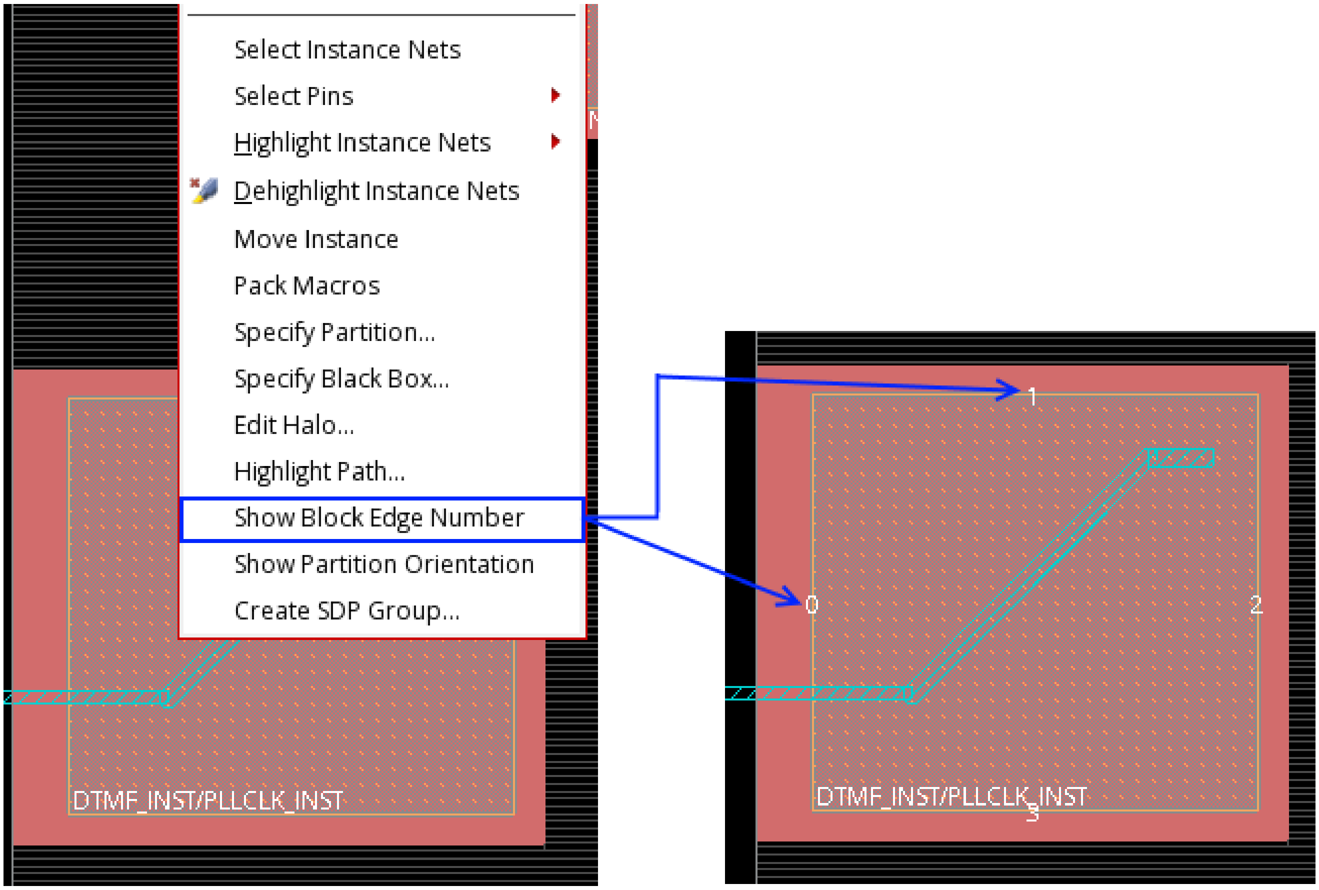
Selecting Highlighted Objects

You can select highlighted objects by using the *Select Highlighted* option in the right-click context menu. If you have objects highlighted in the main window, choose the required type from the *Select Highlighted* submenu to select highlighted objects of that type.



Displaying Edge Numbers of Blocks

During relative floorplanning, you may need to specify the edge number for the reference or target object. If a block is rotated or flipped, determining the edge number may not always be easy. You can click the *Show Block Edge Number* item in the context menu of a block to display the edge numbers in the layout window.



Auto Query

The main window includes an Auto Query (Q) button located at the bottom of the design display area that enables and disables the auto query. When you enable auto query, text information displays for any object that is under the cursor. You can use auto query for blockages, hand-drawn or inside cell instances, instance pins, special route wires and vias, and cell instances. When you use the `loadViolationReport` command to load a file with violation markers generated by external tools, auto query displays the rule names for the markers.

If there are overlapping objects under the cursor, text information displays for the object that is on top. Use the `n` key to get information on the next object, and the `p` key to get information on the previous object. You can also use the F8 binding key to copy auto query text from the message bar in the Innovus main window to the Innovus console. The text is displayed in the Innovus console with the prefix `Message`.

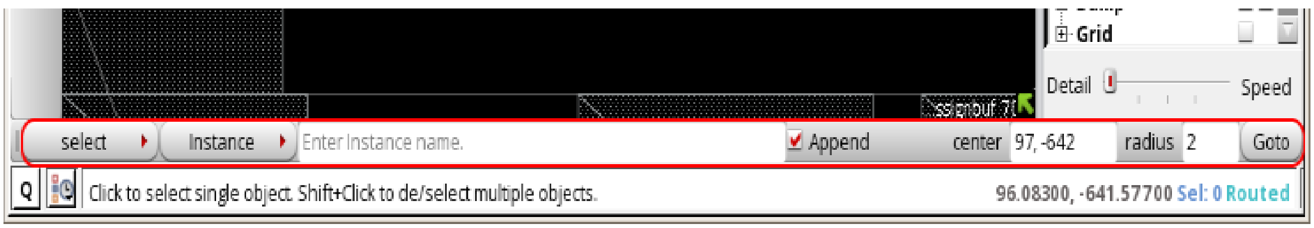
Select Bar

You can use the *Select Bar* on the display window to select or deselect objects. This bar is turned off by default. To turn it on, choose *Windows* -> *Toolbars* -> *Layout* -> *Select Bar* from the main menu. Alternatively, you can turn it on by right-clicking any tool bar and choosing *Select Bar* from the context menu. The *Select Bar* appears at the bottom of the main window. You can then re-position the bar as required by using the docking handles.

Choose the first drop-down on the bar (*select*) to specify whether you want to select or deselect objects.

Use the second drop-down on the bar to specify the type of object you want to select or deselect – *IO Pin*, *Cell*, *Group*, *Instance*, *Module*, *Net, Pin*.

In the text field, you can specify the name of the object to be selected or deselected.



You can also use the Select Bar to zoom in to a required point on the screen. To do so, enter the coordinates of the required point in the *center* text box. Specify the radius of the zoom area in microns in the *radius* text box. When you click the *Goto* button, the display area is centered at the point you entered in the *center* text box and has the radius you specified in the *radius* text box.

Docking Tool and Toolbar Widgets

You can dock tool and toolbar widgets to the side, top, or bottom of the display area:

- Click on the dock/undock handle (). For ease-of-recognition, the mouse cursor changes to a `move' icon when you place it over the dock handle of tool or toolbar widgets.
- Drag to the desired location.

Tear-off Menus and Submenus

You can tear off any menu or submenu and place it anywhere in the design area. To tear off a menu or submenu, click on the dotted line that appears at the top of the menu or submenu, and drag the menu to where you want it displayed in the design area. The menu remains on the screen as a window when you release the mouse button.

Mouse Operation

You can use the mouse buttons to perform various command shortcuts.

- Left-click the mouse to perform the action of the active mode.
  - The *Select* mode is active by default. Each of the three design views allows certain objects to be selected:
    - Floorplan view: Modules, blocks, and floorplan objects.
    - Amoeba view: Modules and blocks
    - Physical view: Blocks, instances, and nets

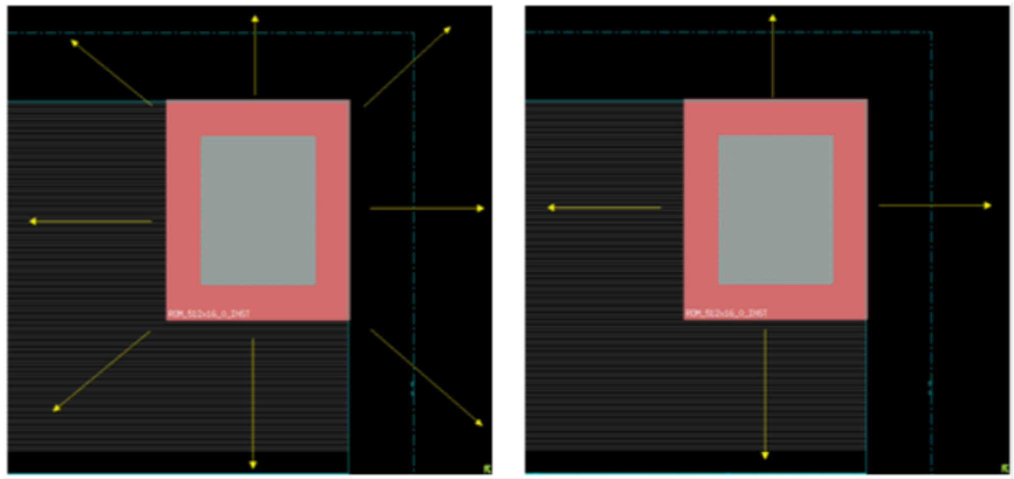
    In the *Select* mode, use the `Shift` key for multiple object selections.

    You can also left-click and drag the mouse over a specific area in the main window to select the objects within that area. Press the `Ctrl + M` toggle key combination to switch to the line selection mode. In the line selection mode, draw a line across the objects you want to select. All the objects that the line crosses are selected. You can press `Ctrl + M` again to return to the window selection mode.

    Use the space bar to change the highlighting focus on an object.

    Double-click an object to view or change object attributes.
  - In the *Move* mode:
    - Left-click and drag an object to move it in any direction by default.
    - Press the `Shift` key and then click and drag an object if you want to move it only in either vertical or horizontal direction (orthogonal movement).

Move mode



Click and drag an object in any direction by default.

Equivalent to the *Move Restrictions: No Restrictions* option on the *Edit* tab of the Preferences form.

Press the *Shift* key and then click and drag an object to restrict movement to orthogonal (vertical or horizontal direction only).

Equivalent to the *Move Restrictions: Orthogonal* option on the *Edit* tab of the Preferences form.

- Right-click and drag the mouse to specify an area that you want to see in greater detail. When you release the mouse button, the display zooms in to the selected area.
- Click the middle button of your mouse to pan the viewable window to the center point. This is equivalent to using the `panCenter` command.
- Move the scroll wheel of your mouse to pan and zoom the design:
    - To zoom in or out, simply move the wheel forward or backward.
    - To pan up or down, press `Shift` and move the wheel forward or backward.
    - To pan left or right, press `Ctrl` and move the wheel forward or backward.

Keyboard Shortcuts

Innovus provides keyboard shortcuts, called binding keys, to access commands in the design display area. For information on creating or modifying bindkeys, see Binding Key in the View Menu chapter.

Selecting a Large Number of Objects

While working with the GUI, you may sometimes attempt to select a wide area accidentally. Selection of a large number of objects can take a long time and may slow down the tool. To prevent this, Innovus pops up a warning message if you attempt to select more than 10,000 objects in the design. If you made the selection accidentally, click *No* to cancel the selection.

Viewing the Documentation Library through the Help Menu

You can access the complete library of Innovus documentation through the *Help* menu. The *Help - Documentation Library* link opens the Cadence Help viewer with all the books in the Innovus documentation suite.

You can also view the individual books through their respective links from the *Help* menu. For example, to view the *Text Command Reference*, select *Help - Text Command Reference*.

Accessing the Documentation Library Quickly through the Help Search Box

The help search box next to the menu bar in Innovus enables you to search the help library directly from the main window. To search for information, simply type a relevant keyword in the help search box and press `Enter`. The Cadence Help window pops up, listing related documents based on the keyword you entered.

Innovus records your search history and displays keywords that you have previously searched in the help drop-down list. This makes it easy for you to repeat a search.

Displaying Innovus Version Number, and Patent- and Copyright-Information

The *Help - About* menu brings up the About: Innovus RTL-to-GDSII System dialog box. This dialog box displays the version number as well as patent- and copyright-related information.

Customizing the User Interface

Innovus provides a GUI development kit comprising five APIs that let you customize the menus, toolbars, status bar, main window, and other interface elements. Using the GUI development kit, you can:

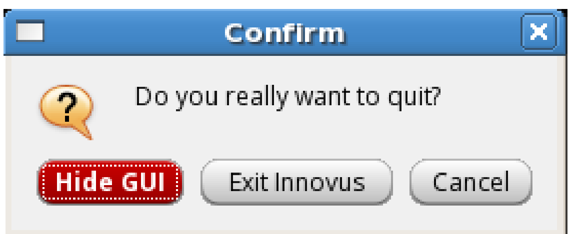
- Add a new menu, submenu, menu item, toolbar, toolbutton or other interface element using the `uiAdd` command.
- Delete a specific menu, toolbar, or menu item using the `uiDelete` command.
- Change the properties of a menu, menu item, toolbar, toolbutton, or the main window using the `uiSet` command.
- Query an existing property of a specific menu, toolbar, or other interface element using the `uiGet` command.
- Find an existing widget by specifying one or more of its properties using the `uiFind` command.

For more information, read the following:

- The "GUI Commands" chapter of the *Text Command Reference*.
- The "Customizing the User Interface" chapter of the *Innovus User Guide*.

Closing or Hiding the GUI

Use the *Close* button at the top-right corner of the main window to hide or close the GUI.



Choose the *Hide GUI* button in the confirmation box to hide the GUI. To quit the tool, click *Exit Innovus*.

2

File Menu

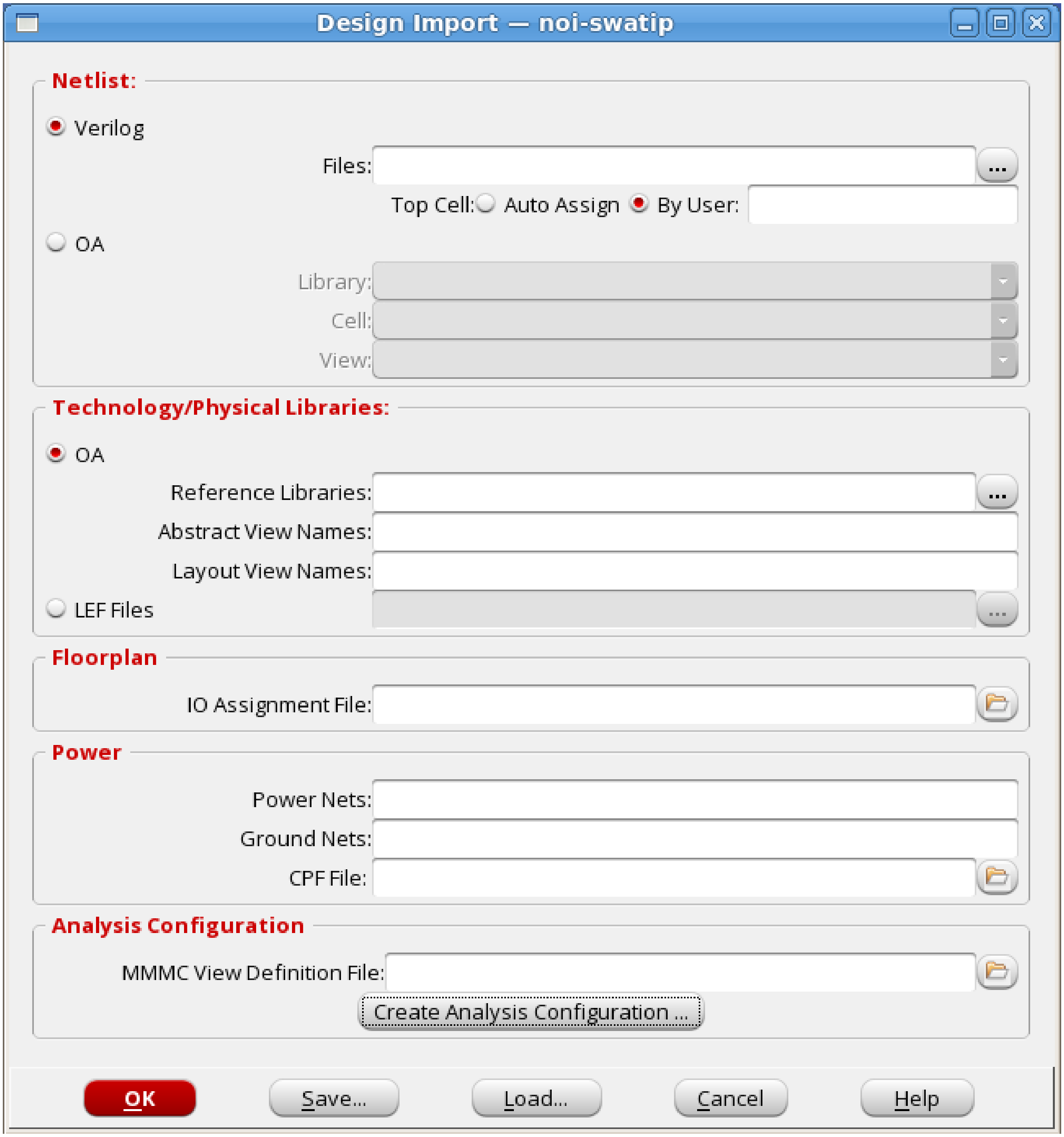
- Import Design
  - MMMC Browser
  - MMMC Configuration
  - Add Library Set
  - Add RC Corner
  - Add OP Cond
  - Add Power Domain
  - Add Constraint Mode
  - Add Analysis View
  - Add Setup Analysis View
  - Add Hold Analysis View
  - MMMC Preferences
  - Add Object
  - Edit Library Set
  - Edit OP Cond
  - Edit RC Corner
  - Edit Constraint Mode
  - Edit Delay Corner
  - Edit Power Domain
  - Edit Analysis View
- Restore Design
  - OA Page

Import Design

The Design Import form enables you to set up the design for import into the Innovus Implementation System (Innovus) software. Use this form to import a full chip design; a partial design, such as a module; or a partitioned design.

Note: The options on the Design Import form correspond to variables in the globals file.

- Choose *File - Import Design*.



Design Import - Fields and Options

Note: The browse (...) button next to the text fields opens a form from which you can load selected files. The form that opens depends on the type of file you are loading.

Verilog		
	Files	Specifies the gate-level Verilog netlist files to import. Innovus automatically checks whether the netlist is unique, and displays a message accordingly. If specifying multiple names in the text field, use spaces to separate the names. You can use wildcards (*.`extension`) or directory names to specify multiple files. You can specify compressed files (`.gz` extension).
	Auto Assign	Extracts the design's top cell name from the netlist, provided the netlist contains only one design. *Default:* Off
	By User	Specifies the name of the design's top cell when a netlist contains more than one design (more than one top design name). The top cell name specified is the design the software imports and processes. *Default:* On
OA		
	Library	Specifies the location of the Open Access database to import. It contains the cell and the view to be loaded. The Open Access library name should be specified in the `cds.lib` file. The Import Design form contains *Verilog* and *OA* radio button that changes the form from the current LEF based style (default) to the Open Access-based style.
	Cell	Specifies the design cell from the library that is to be loaded.
	View	Specifies the view name of the cell that is to be loaded.
Technology/Physical Libraries		Specifies the technology and physical libraries being used depending on the flow - *OA* or *LEF*.

	OA	This is the default option. With this option, you need to specify the following: • *Technology Libraries*: Specifies the list of OpenAccess libraries. These library names are defined in the cds.lib file. All the abstract views in the specified libraries are loaded. You can use this option to specify the library that is used to load the OpenAccess technology data. If not specified, the first library specified in the *OA Reference Libraries* list will be used. • *OA Reference Libraries*: Specifies the list of one or more Open Access libraries. These library names are defined in the cds.lib file. • You must specify the technology library first, then specify the standard cell and block reference libraries in any order. In the case where an OpenAccess database is loaded, the technology information will be read from the library specified as OpenAccess library. **Note:** The browse (...) button next to this field opens a form from which you can select technology libraries, instead of typing the names of these libraries. • *OA Abstract View Names*: Specifies a list of one or more views to be processed as abstract (LEF MACRO equivalent) views. • *OA Layout View Names*: Specifies a list of one or more views to be processed as cell layout views. For more information, see the Cell Layout Page in the "Main Window" chapter of the *Innovus Menu Reference*.

	LEF Files	Specifies the list of one or more LEF files to import. Choose this option if you want to use the LEF flow. You must specify the technology LEF file first, then specify the standard cell LEF and block LEF in any order. The LEF file provides technology information, such as metal layer and via layer information and via generation rules, which is used in the Add Rings and Add Stripes forms. The router also uses the technology information contained in the LEF file. If a cell is defined multiple times, Innovus reads the geometry information only from the first definition. For subsequent definitions, Innovus reads the antenna information only. If the LEF file contains all the physical information for the design, no other files are required for the Technology Information/Physical Libraries panel. **Note:** Use either an all-LEF flow or an all-OpenAccess flow. Do not mix these two.
Floorplan		
	IO Assignment File	Specifies the I/O files to import. The I/O assignment file assigns an I/O pad for a chip design, or a pin for a block design. The I/O assignment file can be in line order sequence for the I/O pad instance names, or can be rule based. If I/O pads are placed from loading a floorplan file, you do not need to specify an assignment file. For information on creating an I/O assignment file, see "Generating the I/O Assignment File," in the Data Preparation chapter of the *Innovus User Guide*.
Power		

	Power Nets	Specifies the names of the power nets. You can enter multiple names by separating the net names with a space, for example: `vdd vdd_lp vdd_lp_s` Use the power net names specified here when creating the power strips in the floorplan.
	Ground Nets	Specifies the names of the ground nets. You can enter multiple names by separating the net names with a space, for example: `vss Avss` Use the ground net names specified here when creating the ground strips in the floorplan.
	CPF File	Specifies the Common Power Format (CPF) file
Analysis Configuration		
	MMMC View Definition File	Specifies a Tcl command script that contains the analysis view configurations for multi-mode multi-corner (MMMC) timing analysis and optimization. The file contains a list of Tcl commands that create library sets, constraint modes, RC corners, delay corners, and analysis views. Processing the file does not automatically place the software in MMMC mode. If the file also contains a `set_analysis_view` command, then the software is placed in MMMC analysis mode after the file is processed. If you do not have an MMMC view definition file, you can click the *Create Analysis Configuration* button to generate a new definition file with MMMC Browser.
	Create Analysis Configuration	Opens the MMMC Browser. The browser displays the multi-mode multi-corner (MMMC) configuration, and allows you to create and edit the various objects and analysis views necessary for multi-mode multi-corner analysis.

Related Text Commands

- `loadLefFile`
- `loadIoFile`

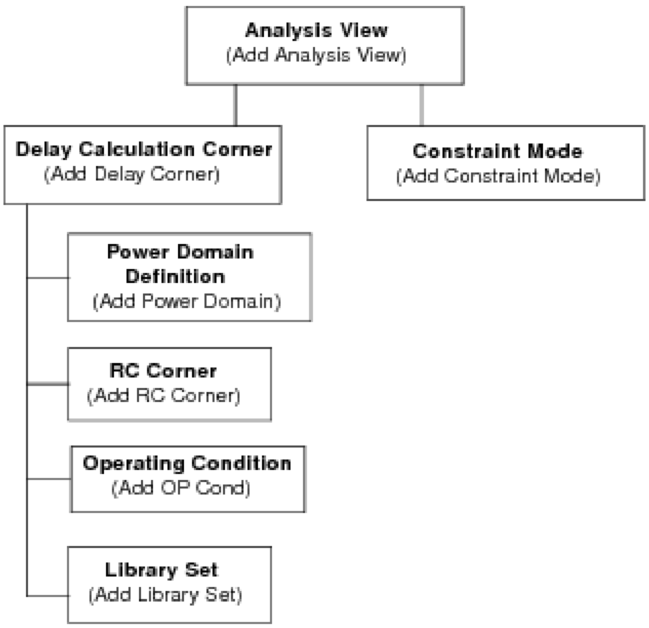
Related Topics

- For information on preparing the design for import, see "Data Preparation" in the *Innovus User Guide*.
- For information on importing designs, see "Importing and Exporting Designs" in the *Innovus User Guide.*

MMMC Browser

Use the MMMC Browser to create hierarchically a new MMMC configuration for the design. The view configurations that you create are stored as Tcl commands in a view definition file that can then be loaded into the design. Each top-level set of information is called an analysis view, which is composed of a delay calculation corner and a constraint mode. The active analysis views defined in the software represent the different design variations that will be analyzed.

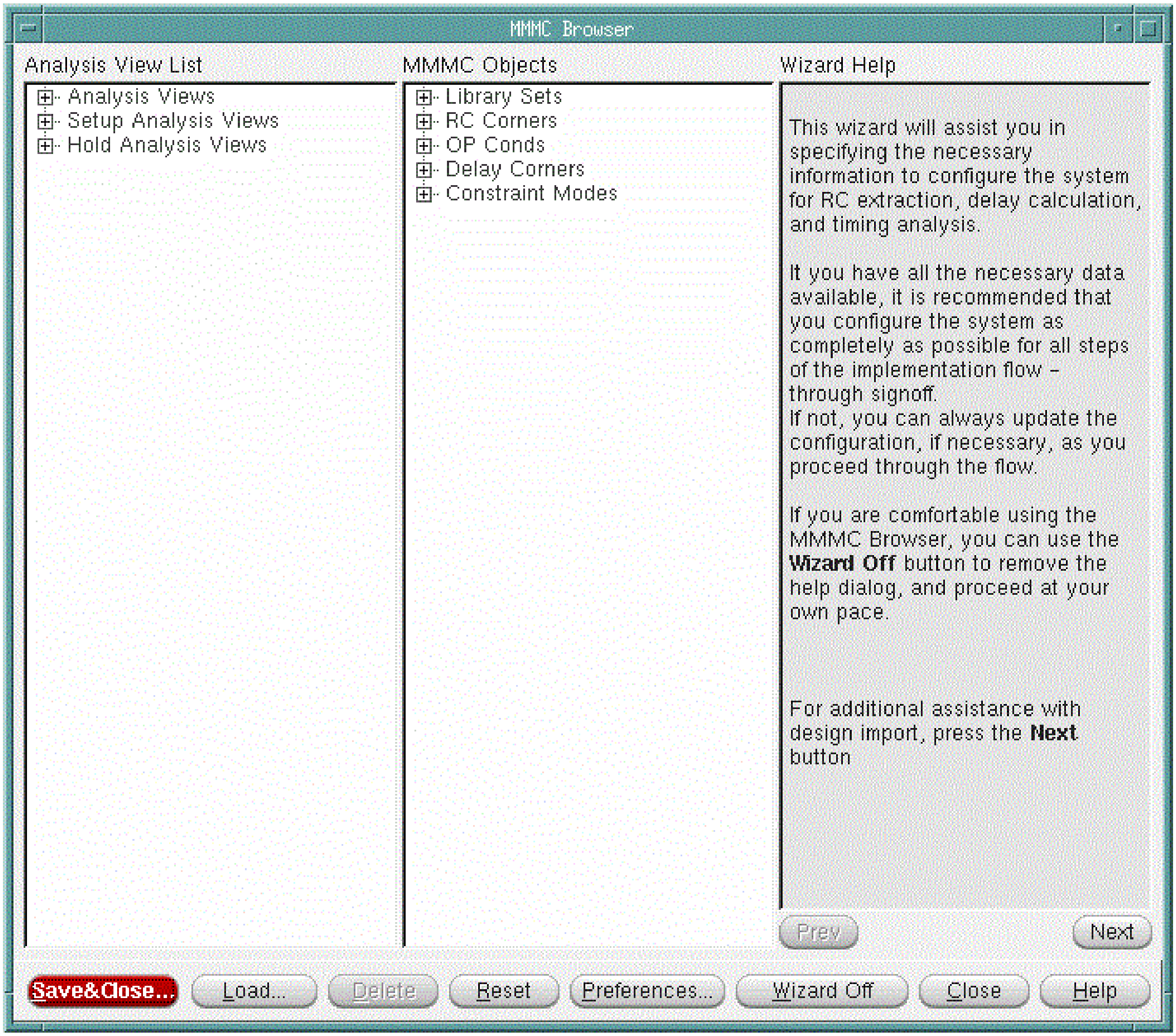
Figure 2-1 Hierarchical Analysis View Configuration



To access MMMC Browser:

→ Choose *File - Import Design* and click the *Create Analysis Configuration* button on the *Basic* page.

Note: You can also access MMMC Browser from the *Timing* menu to add new objects and control analysis views to the existing MMMC configuration that is in memory for the design.



By default, the MMMC browser opens in *Wizard On* mode. In this mode, the *Wizard Help* pane and guides you through the process of configuring the MMMC environment and informs you about pertinent design considerations at each step. If you are comfortable using the MMMC Browser on your own, click the *Wizard Off* button to remove the *Wizard Help* pane and proceed at your own pace.

For more information on configuring MMMC and generating a MMMC view definition file, see MMMC Configuration.

MMMC Configuration

The MMMC environment is configured and assembled hierarchically. You must specify the lower-level information first, so that it can be referenced later on in the process.

The recommended configuration order is:

1. Specifying timing related library information (Add Library Set)
2. Specifying RC extraction corners (Add RC Corner)
3. Specifying operating conditions (Add OP Cond)
4. Specifying delay corners (Add Delay Corner and Add Power Domain)
5. Specifying constraint modes (Add Constraint Mode)
6. Creating analysis views (Add Analysis View)
7. Selecting views for Setup (Add Setup Analysis View) and Hold analysis (Add Hold Analysis View)

The *Wizard Help* pane in MMMC Browser takes you through each of these required steps in the order shown above. When you have finished configuring the analysis environment, click the *Save&Close* button to save your configuration in a file and return to the main Design Import form. When the Design Import form is executed, the system will load the MMMC configuration for the active Setup and Hold views that you have specified.

You can change how the configuration is displayed in MMMC Browser by using the MMMC Preferences form.

Additionally, you can access the following editing forms from the MMMC Browser by double-clicking on a specific object name.

- Edit Library Set
- Edit OP Cond
- Edit RC Corner
- Edit Constraint Mode
- Edit Delay Corner
- Edit Power Domain
- Edit Analysis View

Add Library Set

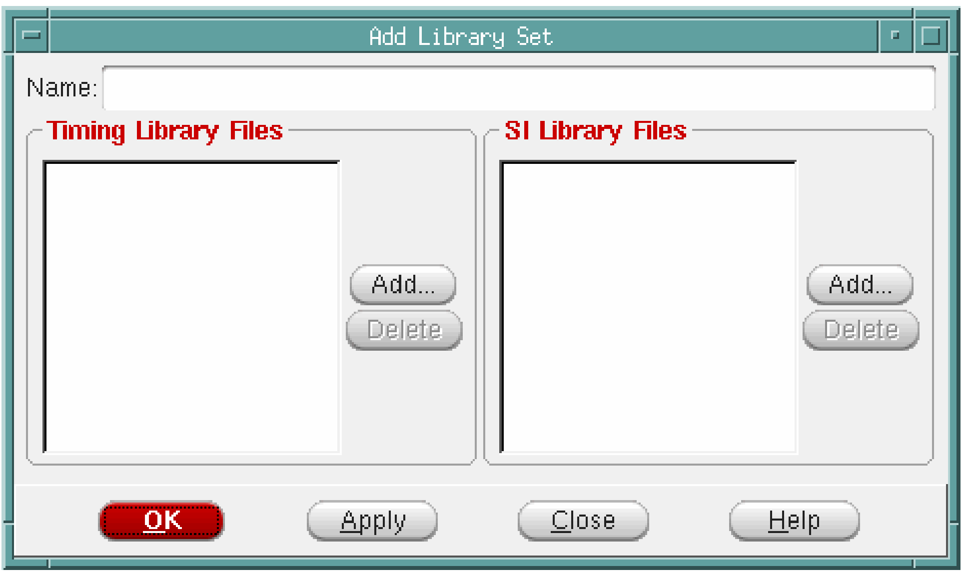
Use the Add Library Set form to associate a list of timing and signal integrity (cdB) libraries with a library set name. Library sets allow a group of library files to be treated as a single entity so that higher-level descriptions (delay calculation corners) can simply refer to the library configuration by name. The same library set can be referenced multiple times by different delay calculation corners.

Note: The order in which you define timing libraries is important. The software considers the first library you specify in the list as the master library, with each successive library having a lower priority.

- Choose *File - Import Design*, click the *Create Analysis Configuration* button, and then double-click *Library Sets* on the *MMMC Objects* pane of MMMC Browser.

or

- Choose *Timing - Configure MMMC*, and double click on *Library Sets*.



Fields and Options

Name	Specifies the name for the library set being created. This name is used to associate the library list with a specific delay calculation corner.
Timing Library Files	Specifies the timing libraries to include in the library set.
SI Library Files	Specifies cdB libraries and/or user-defined noise (UDN) models to include in the library set.

Related Text Commands

- `create_library_set`
- `get_library_set`
- `all_library_sets`

Related Topics

- Creating Library Sets

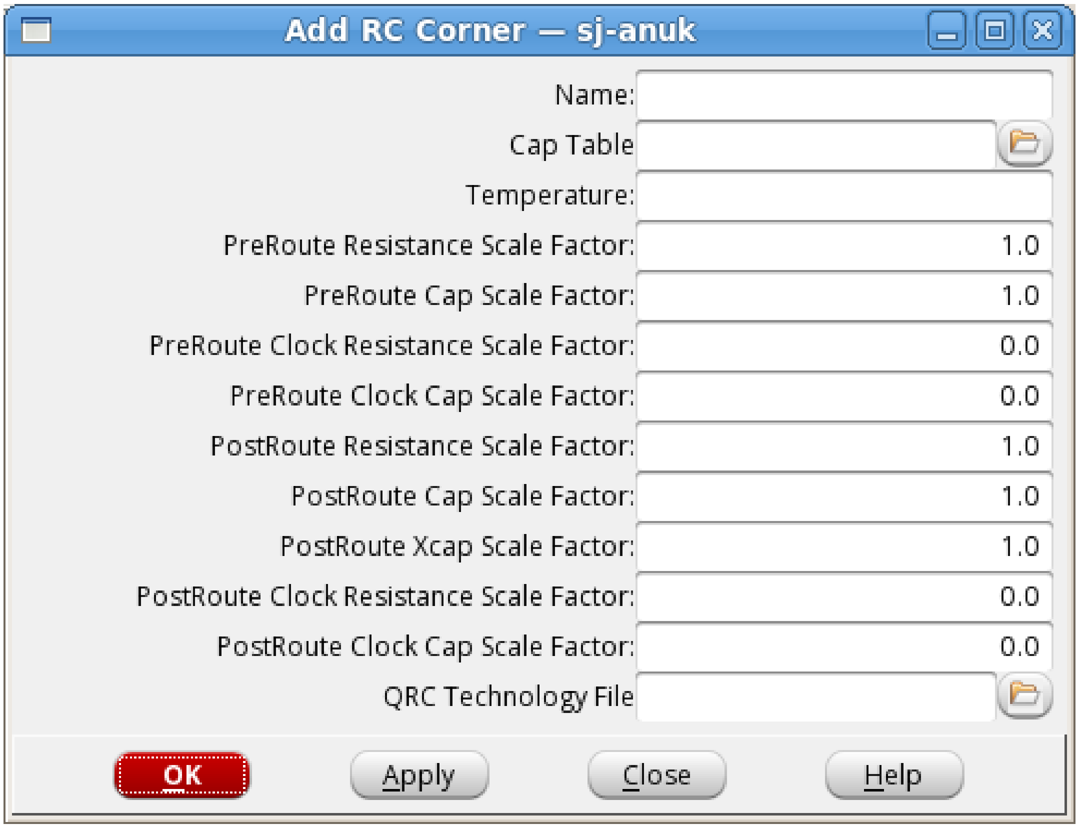
Add RC Corner

Use the Add RC Corner form to create a named RC corner object that can be referenced later when creating a delay calculation corner object. An RC corner object provides the software with all of the information necessary to properly extract, annotate, and use the RCs for delay calculation.

→ Choose *File - Import Design*, click the *Create Analysis Configuration* button, and then double-click *RC Corners* on the *MMMC Objects* pane of MMMC Browser.

or

→ Choose *Timing - Configure MMMC*, and double click on *RC Corners*.



Fields and Options

Name	Specifies the name for the RC corner object being created. You can choose any name for an RC corner object, but it is recommended that you use a name that can be easily recognized as referring to a specific RC corner (for example, rc-min, rc-max, c-min, c-max, and so on).
Cap Table	Specifies the capacitance table to be used by the PreRoute and PostRoute `-effortLevel low` extraction engines when using this RC corner.
Temperature	Specifies the Operating temperature, in units of Celsius, to be used to derate extracted resistance values. **Note:** The software does not require that the temperature specified by the PVT operating condition at the delay calculation corner level be the same as the RC nominal or user-specified temperature value. If you do not specify a temperature, the extracted resistance will not be derated.

PreRoute Resistance Scale Factor	
	Specifies the resistance scale factor for RC extraction of signal nets in the PreRoute mode. *Default:* `1.0`
PreRoute Cap Scale Factor	
	Specifies the capacitance scale factor for RC extraction of signal nets in the PreRoute mode. *Default:* `1.0`
PreRoute Clock Resistance Scale Factor	
	Specifies the scale factor for resistance of clock nets in the PreRoute mode. *Default:* `0` If you do not specify the clock resistance scale factor value for PreRoute extraction explicitly, the software uses the scale factor value specified in the `PostRoute Resistance Scale Factor` field. When used, the value specified in this field overrides the value specified in the `PostRoute Resistance Scale Factor` field for clock nets. **Note:** Clock net extraction in the PreRoute stage uses the same engine as PostRoute extraction for increased accuracy. Therefore, a separate scale factor for clock nets is appropriate.
PreRoute Clock Cap Scale Factor	
	Specifies the scale factor for capacitance of clock nets in PreRoute mode. *Default:* `0` If you do not specify the clock capacitance scale factor value for PreRoute extraction explicitly, the software uses the scale factor value specified in the `PostRoute Cap Scale Factor` field. When used, the value specified in this field overrides the value specified in the `PostRoute Cap Scale Factor` field for clock nets. **Note:** Clock net extraction in the PreRoute stage uses the same engine as PostRoute extraction for increased accuracy. Therefore, a separate scale factor for clock nets is appropriate.

PostRoute Resistance Scale Factor	
	Specifies the resistance scale factor for RC extraction of signal nets in the PostRoute mode. **Note:** This parameter supports the use of duplets or triplets for engine dependent scaling. See `create_rc_corner` for more information on setting scale factors. *Default:* `1.0`
PostRoute Cap Scale Factor	
	Specifies the capacitance scale factor for RC extraction of signal nets in the PostRoute mode. **Note:** This parameter supports the use of duplets or triplets for engine dependent scaling. See `create_rc_corner` for more information on setting scale factors. *Default:* `1.0`
PostRoute XCap Scale Factor	
	Specifies the cross-coupling capacitance scale factor for RC extraction in the PostRoute mode. **Note:** This parameter supports the use of duplets or triplets for engine dependent scaling. See `create_rc_corner` for more information on setting scale factors. *Default:* `1.0`
PostRoute Clock Resistance Scale Factor	

	Specifies the scale factor for resistance of clock nets in the PostRoute mode for the extractor with `effortLevel low`. *Default:* `0` If you do not specify the clock resistance scale factor value for postRoute extraction explicitly, or change the value back to the symbolic value of 0, the postRoute extractor with `effortLevel low` uses the scale factor value specified in the `PostRoute Resistance Scale Factor` field. **Note:** The other postRoute extractors do not support the use for different scaling factors for clock nets.
PostRoute Clock Cap Scale Factor	
	Specifies the scale factor for capacitance of clock nets in PostRoute mode for the extractor with effortLevel `low`. *Default:* `0` If you do not specify the clock capacitance scale factor value for postRoute extraction explicitly, or change the value back to the symbolic value of 0, the postRoute extractor with effortLevel `low` uses the scale factor value specified in the `PostRoute Cap Scale Factor` field. **Note:** The other postRoute extractors do not support the use for different scaling factors for clock nets.
QRC Technology File	Specifies the name of the Quantus QRC Technology file used by TQuantus, IQuantus, or sign-off QRC extraction. For most technologies, you can get the Quantus QRC Technology file from your foundry. For technologies that are not available through the technology vendors, you use the same ASCII-format interconnect technology (ICT) input file that is used to generate the captable. TechGen, the utility used to create the Quantus QRC Technology file, is provided with the Innovus software and does not require any additional license. For more information on running TechGen, see *EXT TechGen Reference Manual*. For more information on creating the ICT files, see Appendix A "Creating the ICT File", in the *Innovus User Guide*.

Related Text Commands

- `create_rc_corner`
- `get_rc_corner`
- `all_rc_corners`

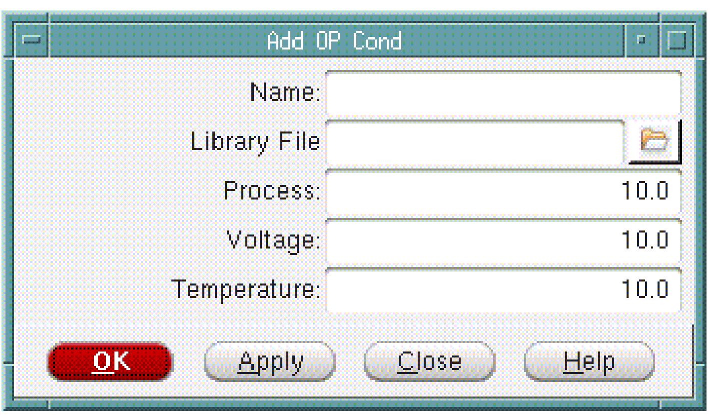
Related Topics

- *Creating RC Corner Objects* section of the *Importing and Exporting Designs* chapter of the Innovus User Guide.

Add OP Cond

Use the Add OP Cond form to create a set of virtual operating conditions in the specified library without actually modifying the library. These virtual operating conditions can then be referenced by a delay calculation corner as if they actually existed in the library.
→ Choose *File - Import Design*, click the *Create Analysis Configuration* button, and then double-click *OP Conds* on the *MMMC Objects* pane of MMMC Browser.

or
→ Choose *Timing - Configure MMMC*, and double click on *OP Conds*.



Fields and Options

Name	Specifies the name for the operating condition being created.
Library File	Specifies the library for which to create the virtual operating conditions.
Process	Specifies the process value for the operating condition.
Voltage	Specifies the voltage value for the operating condition.
Temperature	Specifies the temperature value for the operating condition.

Related Text Commands

- `create_op_cond`
- `get_op_cond`
- `all_op_conds`

Related Topics

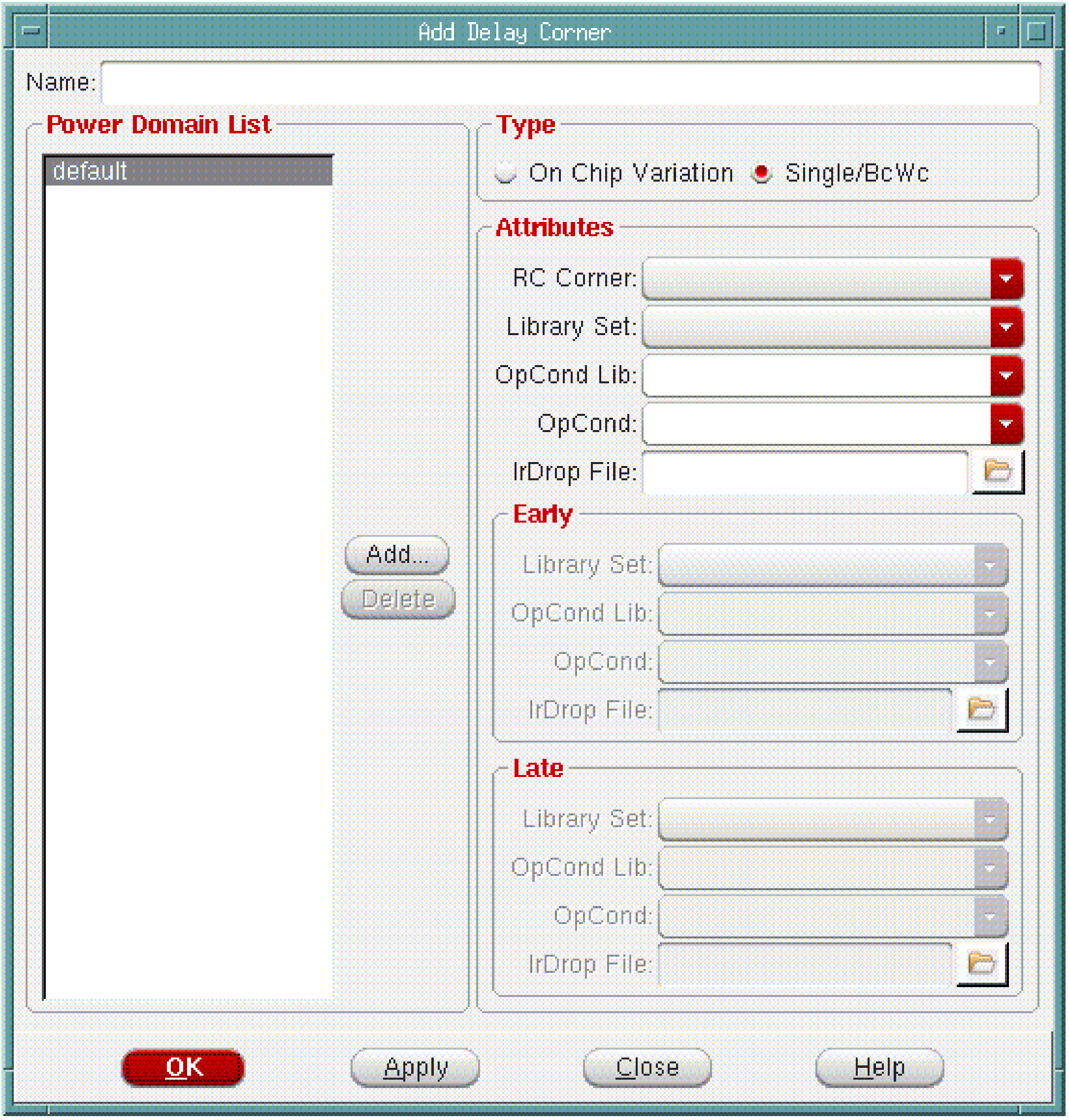
- *Creating Virtual Operating Conditions* section of the *Importing and Exporting Designs* chapter of the Innovus User Guide

Use the Add Delay Corner form to create a named delay calculation corner object that can be referenced later when creating an analysis view. A delay calculation corner provides all of the information necessary to control delay calculation for a specific view. Each corner contains information on the libraries to use, the operating conditions with which the libraries should be accessed, and the RC extraction parameters to use for calculating parasitic data. Delay corner objects can be shared by multiple top-level analysis views.

Note: A single delay calculation corner object specifies the delay calculation rules for the entire design. If a design includes power domains, the delay calculation corner can contain domain-specific subsections that specify the required operating condition information, and any necessary timing library rebinding for the power domain. Use the Add Power Domain form to add a power domain definition to a delay calculation corner.
→ Choose *File - Import Design*, click the *Create Analysis Configuration* button, and then double-click *Delay Corners* on the *MMMC Objects* pane of MMMC Browser.

or

→ Choose *Timing - Configure MMMC*, and double click on *Delay Corners*.



Fields and Options

Name	Specifies the name for the delay calculation corner object being created.

Type	Specifies the type of analysis for which you are configuring the multi-mode multi-corner environment. When running Single or Best-Case Worst-Case (BcWc) timing analysis, a delay calculation corner generally contains one library set and one RC corner object. When running on-chip-variation timing analysis, a delay calculation corner can contain early and late library sets and RC corners. **Note:** If you use a delay calculation corner containing early and late attributes when the software is in BC-WC mode, the software uses the early information for analysis of hold views, and the late information for the analysis of setup views.
RC Corner	Specifies the RC corner object to associate with this delay calculation corner object.
Library Set	Specifies the library set to associate with this delay calculation corner object.
OpCond Lib	Specifies the internal library name for the library in which the operating condition is defined. This is *not* the library file name. If you do not specify a library name,the software searches the library set for the specified operating condition (`-opcond`), starting with the master library.
OpCond	Specifies the operating condition to use for setup and hold analysis. If you do not specify an operating condition, each library in the library set uses its own default operating condition.
IrDrop File	Specifies the IR drop files to apply when calculating early arrival times at a single delay corner.
Early Library Set	Specifies the library set to associate with this delay calculation corner object for calculating early arrival times at a single delay corner.
Early OpCond Lib	Specifies the internal library name for the library in which the early operating condition is defined. This is *not* the library file name. If you do not specify a library name, the software searches the early library set for the specified operating condition (*Early OpCond*), starting with the master library.

Early OpCond	Specifies the operating condition to use for calculating early arrival times at a single delay corner. If you do not specify an operating condition, each library in the early library set uses its own default operating condition.
Early IrDrop File	Specifies the IR drop files to apply when calculating early arrival times at a single delay corner.
Late Library Set	Specifies the library set to associate with this delay calculation corner object for calculating late arrival times at a single delay corner.
Late OpCond Lib	Specifies the internal library name for the library in which the late operating condition is defined. This is *not* the library file name. If you do not specify a library name, the software searches the late library set for the specified operating condition (*Late OpCond*), starting with the master library.
Late OpCond	Specifies the operating condition to use for calculating late arrival times at a single delay calculation corner. If you do not specify an operating condition, each library in the late library set uses its own default operating condition.
Late IrDrop File	Specifies the IR drop files to apply when calculating late arrival times at a single delay corner.
Power Domain List	Displays a list of the delay calculation corner's power domain definitions. To add a power domain definition to the delay corner, click the *Add* button to open the Add Power Domain form. To delete a power domain definition from the delay corner, choose the power domain in the list and click the *Delete* button.

Related Text Commands

- `create_delay_corner`
- `get_delay_corner`
- `all_delay_corners`

- `update_delay_corner`

Related Topics

Importing and Exporting the Design chapter of *Innovus User Guide*:

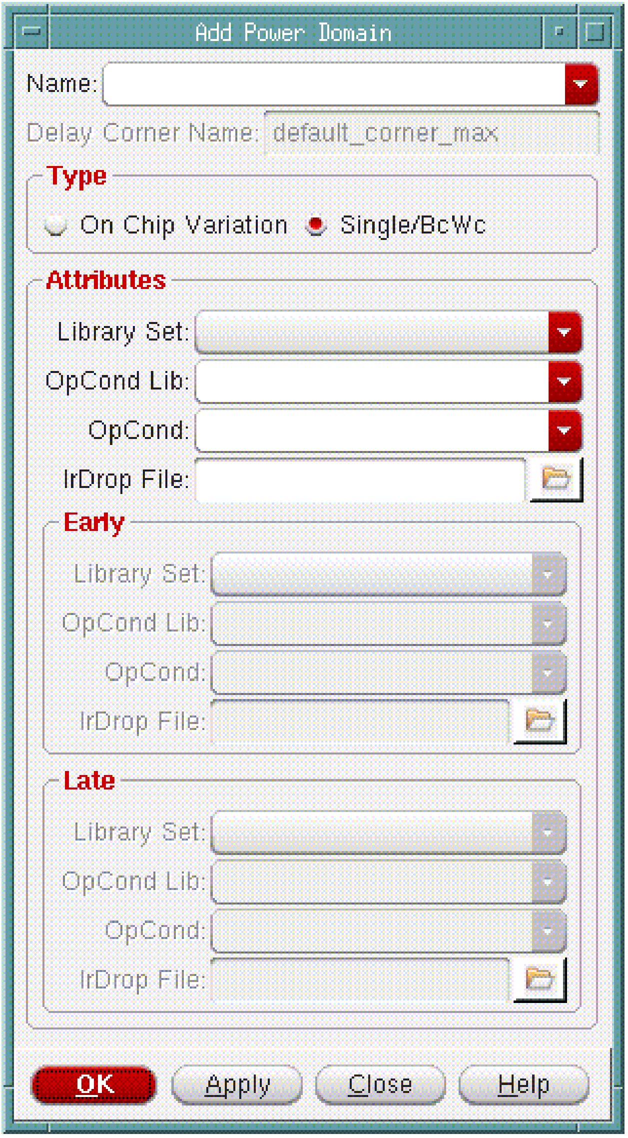
- Creating Delay Calculation Corner Objects
- Adding a Power Domain Definition to a Delay Calculation Corner

Add Power Domain

Use the Add Power Domain form to add a power domain definition to the specified delay calculation corner. Instances contained within an MSMV power domain often require a different library or operating condition that used for the default power domain. Power domain definitions within a delay calculation corner object can be used to assign specific libraries and PVT settings per power domain.

Note: Use separate delay calculation corners to define Best-Case Worst-Case differences. Use the *Early* and *Late* options within a single delay calculation corner to control on-chip-variation.
→ Choose *File - Import Design*, click the *Create Analysis Configuration* button, double-click *Delay Corners*, and then click the *Add* button next to the *Power Domain List*.

or
→ Choose *Timing - Configure MMMC*, double click on *Delay Corners*, and click the *Add* button next to the *Power Domain List*.



Fields and Options

Name	Specifies the name of the power domain to add to the delay calculation corner.
Delay Corner Name	Displays the name of the delay calculation corner to which the power domain definition is being added.

Type	Specifies the type of analysis for which you are configuring the multi-mode multi-corner environment. When running Single or Best-Case Worst-Case (BcWc) timing analysis, a power domain generally contains one library set and operating condition. When running on-chip-variation timing analysis, a power domain can contain early and late library sets and operating conditions.
Library Set	Specifies the library set to associate with the power domain. All of the cells and macros in the power domain get their timing and power information from these libraries.
OpCond Lib	Specifies the internal library name for the library in which the operating condition is defined. This is *not* the library file name. If you do not specify a library name, the software searches the library set for the specified operating condition (*OpCond*), starting with the master library.
OpCond	Specifies the operating condition to use for the power domain. If you do not specify an operating condition, each library in the library set uses its own default operating condition.
IrDrop File	Specifies the IR drop files to apply to both early and late delay calculation for this power domain object.
Early Library Set	Specifies the library set to associate with the power domain for calculating early arrival times for this power domain.
Early OpCond Lib	Specifies the internal library name for the library in which the early operating condition is defined. This is *not* the library file name. If you do not specify a library name, the software searches the early library set for the specified operating condition (*Early OpCond*), starting with the master library.
Early OpCond	Specifies the operating condition to use for calculating early arrival times for this power domain. *Default:* If you do not specify an operating condition, each library in the early library set uses its own default operating condition.
Early IrDrop File	Specifies the IR drop files to apply when calculating early arrival times at a single power domain.

Late Library Set	Specifies the library set to associate with this delay corner object for calculating late arrival times for this power domain.
Late OpCond Lib	Specifies the internal library name for the library in which the late operating condition is defined. This is *not* the library file name. If you do not specify a library name, the software searches the late library set for the specified operating condition (*Late OpCond*), starting with the master library.
Late OpCond	Specifies the operating condition to use for calculating late arrival times for this power domain. *Default:* If you do not specify an operating condition, each library in the late library set uses its own default operating condition.
Late IR Drop File	Specifies the IR drop files to apply when calculating late arrival times at a single power domain.

Related Text Commands

- `update_delay_corner`

Related Topics

Importing and Exporting the Design chapter of *Innovus User Guide*:

- Adding A Power Domain Definition To A Delay Calculation Corner

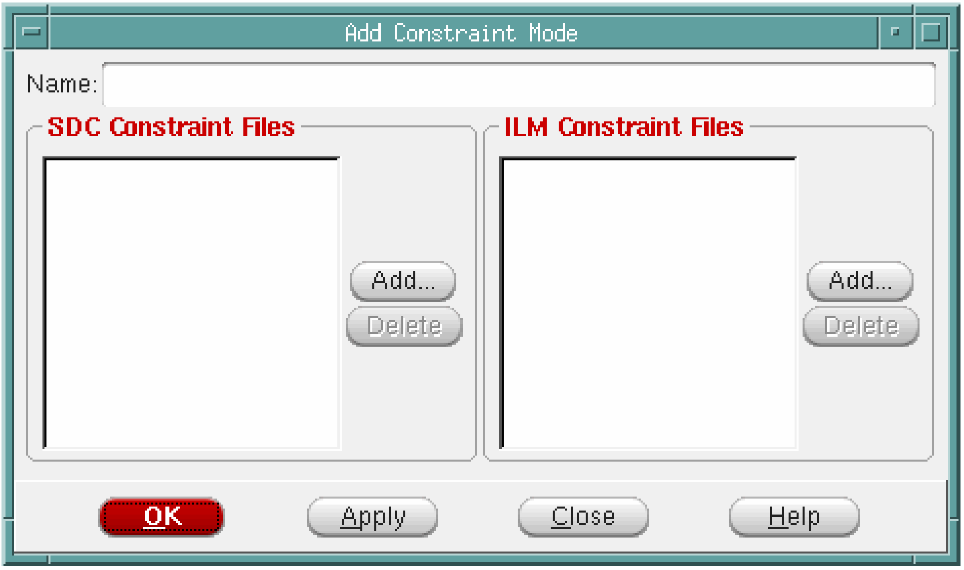
Add Constraint Mode

Use the Add Constraint Mode form to associate a list of SDC constraint files with a specified constraint mode name. This constraint mode name can be referred to later when creating analysis views. A constraint mode defines one of possibly many different functional, test behaviors, or Dynamic Voltage and Frequency Scaling (DVFS) modes of a design. SDC files can be shared by many different constraint modes, and the same constraint mode can be associated with multiple analysis views.

→ Choose *File - Import Design*, click the *Create Analysis Configuration* button, and then double-click *Constraint Modes* on the *MMMC Objects* pane of MMMC Browser.

or

→ Choose *Timing - Configure MMMC*, and double click on *Constraint Modes*.



Fields and Options

Name	Specifies the name of the mode to be created.
SDC Constraint Files	Specifies a list of SDC files to be included in the mode.
ILM Constraint Files	Specifies a list of ILM constraint files to be included in the mode.

Related Text Commands

- `create_constraint_mode`
- `get_constraint_mode`
- `all_constraint_modes`

Related Topics

Following sections in the *Importing and Exporting Designs* chapter of the Innovus User Guide.

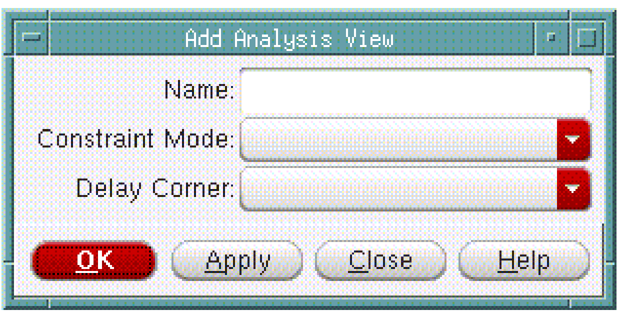
- *Creating Constraint Mode Objects*
- *Constraint the Setup for Multi-Mode and Multi-Mode Multi-Corner Analysis*

Add Analysis View

Use the Add Analysis View form to create an analysis view object that associates a delay calculation corner with a constraint mode. An analysis view object provides all of the information necessary to control a given multi-mode multi-corner analysis.

After creating analysis view objects, use the Add Hold Analysis View and Add Setup Analysis View forms to specify which views to use for setup and hold optimization or timing analysis.
→ Choose *File - Import Design*, click the *Create Analysis Configuration* button, and then double-click *Analysis Views* on the *MMMC Objects* pane of MMMC Browser.

or
→ Choose *Timing - Configure MMMC*, and double click on *Analysis Views*.



Fields and Options

Name	Specifies the name of the analysis view being defined.
Constraint Mode	Specifies the name of the constraint mode to associate with this analysis view. A constraint mode groups a set of constraints to be used with any given analysis. To create a constraint mode, use the Add Constraint Mode form.
Delay Corner	Specifies the name of the delay calculation corner object to associate with this analysis view. A delay calculation corner object contains all of the information needed to control delay calculation for a specific analysis view. To create a delay calculation corner, use the Add Delay Corner form.

Related Text Commands

- `create_analysis_view`
- `get_analysis_view`
- `all_analysis_views`

Related Topics

- Creating Analysis Views

Add Setup Analysis View

Use the Add Setup Analysis View form to define which views to use for setup analysis and optimization. These "active" views represent the different design variations that will be analyzed. Active views can be changed throughout the flow to utilize different subsets of views. Innovus applications can handle the views concurrently, sequentially, or in a distributed manner, depending on their individual capabilities. Libraries and data are loaded into the system, as required to support the selected set of active views. You must define at least one setup and one hold analysis view in a multi-mode multi-corner configuration.

The order in which you specify setup views is important. By default, the first view defined is the default setup view. Certain Innovus applications that do not support multi-mode multi-corner can only process the data defined for a single view. These applications use the information defined for the default view.

Note: Use the `set_default_view` command, if you want to change the default analysis view. Using the `set_default_view` command does not affect software performance because it only uses views that are already active in the design. If you use the Add Setup Analysis View form to change the default views, the existing timing, delay calculation, and RC data is reset.
→ Choose *File - Import Design*, click the *Create Analysis Configuration* button, and then double-click *Setup Analysis Views* on the *MMMC Objects* pane of MMMC Browser.

or
→ Choose *Timing - Configure MMMC*, and double click on *Setup Analysis Views*.

Fields and Options

Analysis View	Specifies the active view for setup analysis. Use the Add Setup Analysis View form multiple times to specify more than one setup analysis view.

Related Text Commands

- `set_analysis_view`
- `all_setup_analysis_views`

Related Topics

- Setting Active Analysis Views
- Guidelines For Setting Active Analysis Views
- Changing the Default Active Analysis View

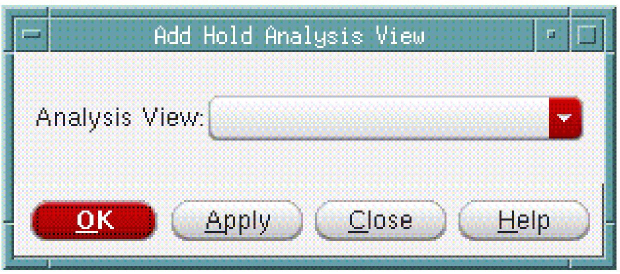
Add Hold Analysis View

Use the Add Hold Analysis View form to define the analysis views to use for hold analysis and optimization. These "active" views represent the different design variations that will be analyzed. Active views can be changed throughout the flow to utilize different subsets of views. Innovus applications can handle the views concurrently, sequentially, or in a distributed manner, depending on their individual capabilities. Libraries and data are loaded into the system, as required to support the selected set of active views. You must define at least one setup and one hold analysis view in a multi-mode multi-corner configuration.

The order in which you specify hold views is important. By default, the first view defined is the default hold view. Certain Innovus applications that do not support multi-mode multi-corner can only process the data defined for a single view. These applications use the information defined for the default view.

Note: Use the `set_default_view` command, if you want to change the default analysis view. Using the `set_default_view` command does not affect software performance because it only uses views that are already active in the design. If you use the Add Hold Analysis View form to change the default views, the existing timing, delay calculation, and RC data is reset.
→ Choose *File - Import Design*, click the *Create Analysis Configuration* button, and then double-click *Hold Analysis Views* on the *MMMC Objects* pane of MMMC Browser.

or
→ Choose *Timing - Configure MMMC*, and double click on *Hold Analysis Views*.



Fields and Options

Analysis View	Specifies the active view for hold analysis. Use the Add Hold Analysis View form multiple times to specify more than one active hold analysis view.

Related Text Commands

- `set_analysis_view`
- `all_hold_analysis_views`

Related Topics

- Setting Active Analysis Views
- Guidelines For Setting Active Analysis Views
- Changing the Default Active Analysis View

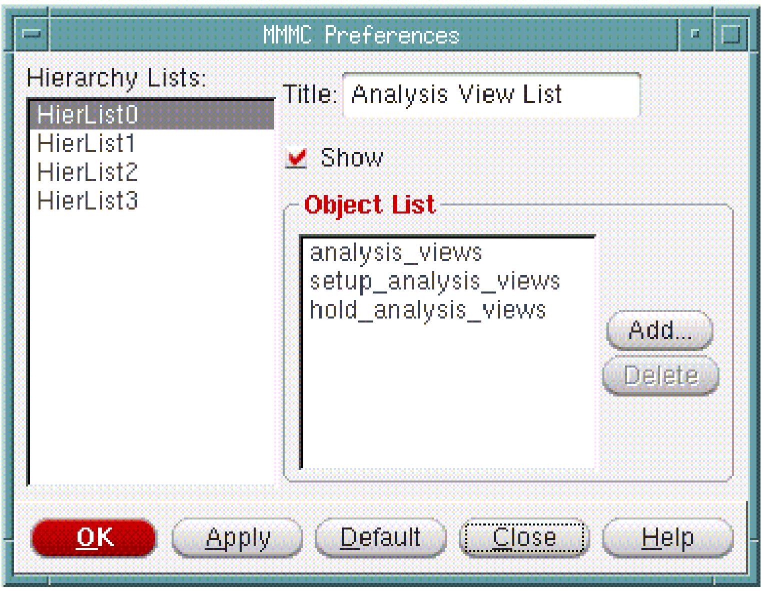
MMMC Preferences

Use the Preferences form to change how the MMMC Browser displays configuration information. By default, the MMMC Browser displays configuration information in two columns. You can change the number of columns displayed, rename the titles of the columns, change which objects are displayed in the columns, and rearrange the order in which the objects are listed.

→ Choose *File - Import Design*, click the *Create Analysis Configuration* button, and then click the *Preferences* button at the bottom of the MMMC Browser.

or

→ Choose *Timing - Configure MMMC*, and click the *Preferences* button.



Fields and Options

Hierarchy Lists	Lists the four columns that can be displayed, from left to right, in the MMC Browser. When you select a column name in the *Hierarchy Lists* window, the form fields reflect the current settings for that column.
Title	Specifies the name of the selected column.
Show	Enables the display of the selected column in the Browser.
Object List	Lists the objects that are displayed in the selected column. To add an object to the column, click the *Add* button and choose an object from the drop down list on the Add Object form. To delete an object from the column, select the object and click the *Delete* button. **Note:** You can rearrange the order of the objects in the list. Click and hold the left mouse button on the name of an object, and drag it to a different position in the list.

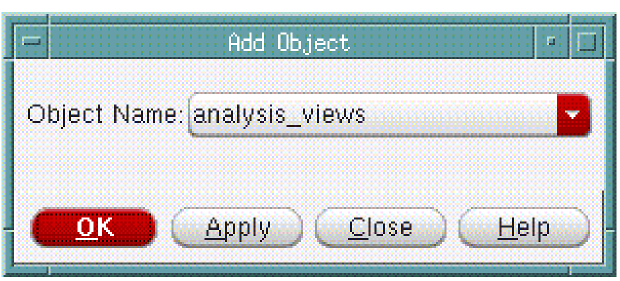
Related Text Commands

There is no equivalent text command for this function. You only can change how the Browser displays the configuration using the MMMC Preferences form.

Add Object

Use the Add Object form to add an object to the list of objects you want displayed for a specific column on the MMMC Browser.

→ Click the *Add* button on the Preferences form.



Fields and Options

Object Name	Specifies the object to add to the list.

Related Text Commands

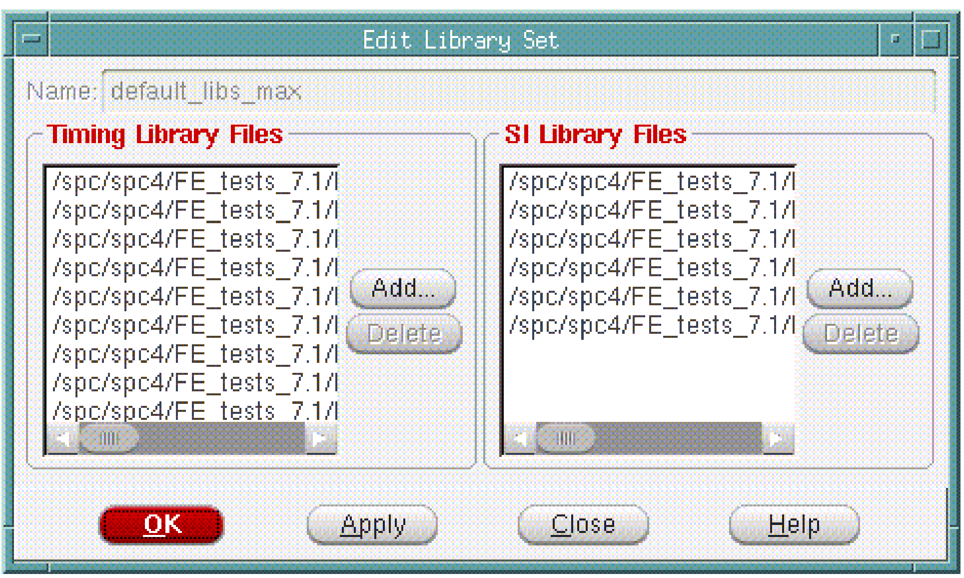
There is no equivalent text command for this function. You only can add an object using the Add Object form.

Edit Library Set

Use the Edit Library Set form to add or delete library files from an existing library set.

> You can edit a library set using the Edit Library Set form before multi-mode multi-corner view definitions are loaded into the design, or after. However, after the software is in multi-mode multi-corner analysis mode, any change to an existing analysis view results in the timing, delay calculation, and RC data being reset for all analysis views.

→ In MMMC browser, double-click the name of the library set you want to edit.



Fields and Options

Name	Specifies the name of the library set being edited.
Timing Library Files	Displays the timing libraries that are included in the library set. Use the *Add* button to add libraries to the list. Use the *Delete* button to delete libraries from the list.
SI Library Files	Displays the cdB libraries that are included in the library set. Use the *Add* button to add libraries to the list. Use the *Delete* button to delete libraries from the list.

Related Text Commands

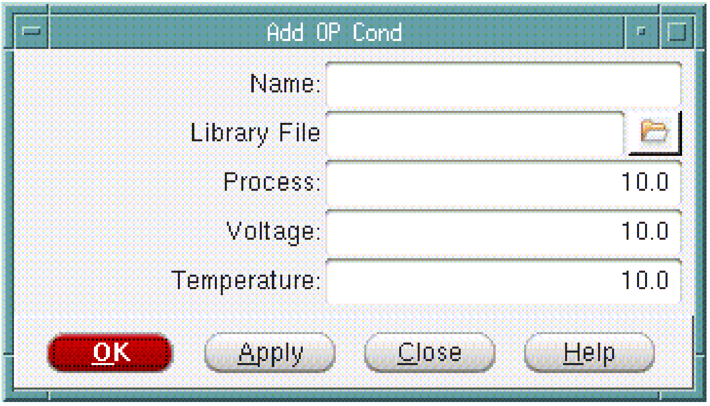
- `update_library_set`

Edit OP Cond

Use the Edit OP Cond form to add, delete, or change attributes for an existing operating condition.

> ⓘ You can edit an operating condition using the Edit Op Cond form before multi-mode multi-corner view definitions are loaded into the design, or after. However, after the software is in multi-mode multi-corner analysis mode, any change to an existing analysis view results in the timing, delay calculation, and RC data being reset for all analysis views.

→ In MMMC browser, double-click the name of the operating condition you want to edit.



Fields and Options

Name	Specifies the name of the operating condition being edited.
Library File	Specifies the library with which to associate the virtual operating conditions.
Process	Specifies the process value for the operating condition.
Voltage	Specifies the voltage value for the operating condition.
Temperature	Specifies the temperature value for the operating condition.

Related Text Commands

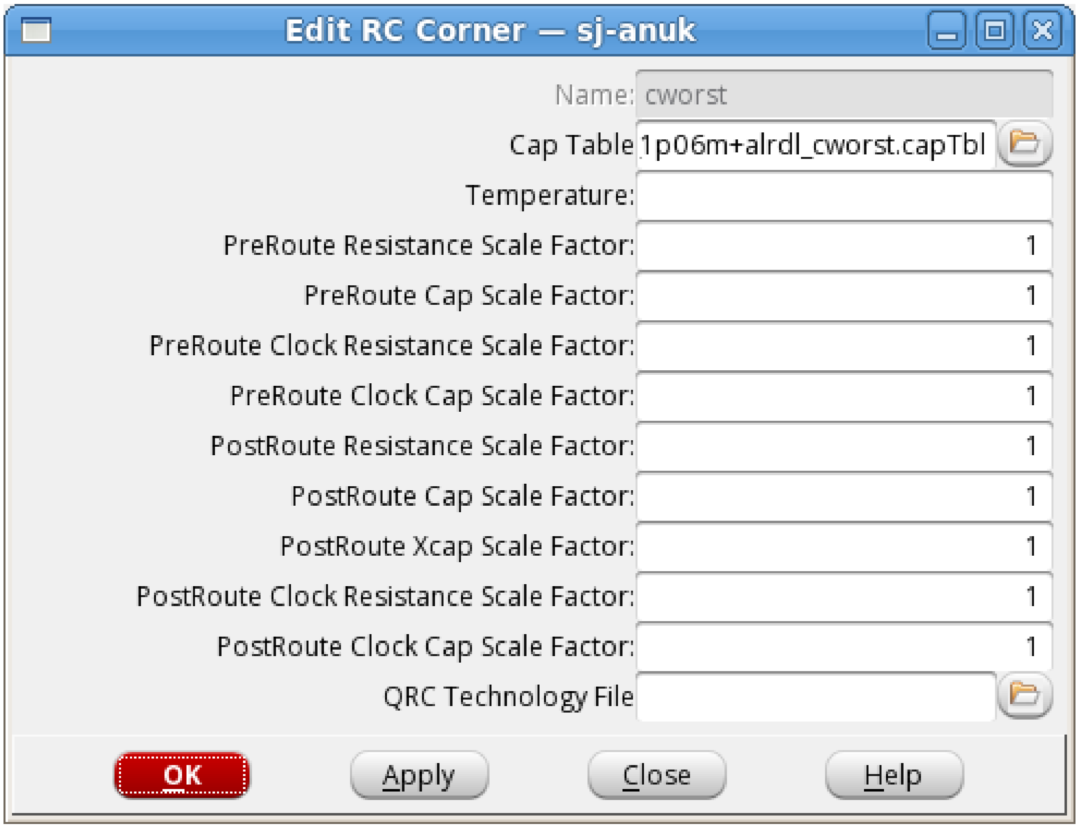
There is no equivalent text command for this function. You only can edit an operating condition using the Edit OP Cond form.

Edit RC Corner

Use the Edit RC Corner form to add, delete, or change attributes for an existing RC corner object.

> ⓘ You can edit an RC corner object using the Edit RC Corner form before multi-mode multi-corner view definitions are loaded into the design, or after. However, after the software is in multi-mode multi-corner analysis mode, any change to an existing analysis view results in the timing, delay calculation, and RC data being reset for all analysis views.

→ In MMMC browser, double-click double click the name of the RC corner object you want to edit.



Fields and Options

Name	Specifies the name for the RC corner object being edited.
Cap Table	Specifies the capacitance table to be used by the PreRoute and PostRoute `-effortLevel low` extraction engines when using this RC corner.
Temperature	Specifies the Operating temperature, in units of Celsius, to be used to derate extracted resistance values. **Note:** The software does not require that the temperature specified by the PVT operating condition at the delay calculation corner level be the same as the RC nominal or user-specified temperature value. If you do not specify a temperature, the extracted resistance will not be derated.

PreRoute Resistance Scale Factor	Specifies the resistance scale factor for RC extraction of signal nets in the PreRoute mode.
PreRoute Cap Scale Factor	Specifies the capacitance scale factor for RC extraction of signal nets in the PreRoute mode.
PreRoute Clock Resistance Scale Factor	Specifies the scale factor for resistance of clock nets in the PreRoute mode.
PreRoute Clock Cap Scale Factor	Specifies the scale factor for capacitance of clock nets in PreRoute mode.
PostRoute Resistance Scale Factor	Specifies the resistance scale factor for RC extraction of signal nets in the PostRoute mode.
PostRoute Cap Scale Factor	Specifies the capacitance scale factor for RC extraction of signal nets in the PostRoute mode.
PostRoute XCap Scale Factor	Specifies the cross-coupling capacitance scale factor for RC extraction in the PostRoute mode.
PostRoute Clock Resistance Scale Factor	Specifies the scale factor for resistance of clock nets in the PostRoute mode for the extractor with `effortLevel low`.
PostRoute Clock Cap Scale Factor	Specifies the scale factor for capacitance of clock nets in PostRoute mode for the extractor with `effortLevel low`.

QRC Technology File	Specifies the name of the Quantus QRC Technology file used by TQuantus, IQuantus, or sign-off QRC extraction. For most technologies, you can get the Quantus QRC Technology file from your foundry. For technologies that are not available through the technology vendors, you use the same ASCII-format interconnect technology (ICT) input file that is used to generate the captable. TechGen, the utility used to create the Quantus QRC Technology file, is provided with the Innovus software and does not require any additional license. For more information on running TechGen, see *EXT Techgen Reference Manual*. For more information on creating the ICT files, see Appendix A "Creating the ICT File", in the *Innovus User Guide*.

Related Text Commands

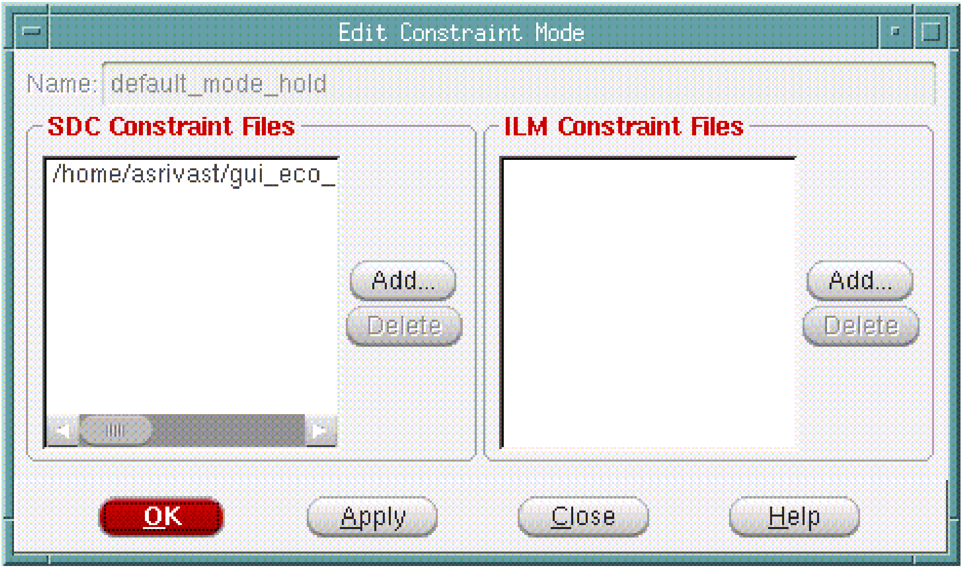
- `update_rc_corner`

Edit Constraint Mode

Use the Edit Constraint Mode form to add or delete SDC constraint files from an existing constraint mode object.

> ⓘ You can edit a constraint mode object using the Edit Constraint Mode form before multi-mode multi-corner view definitions are loaded into the design, or after. However, after the software is in multi-mode multi-corner analysis mode, any change to an existing analysis view results in the timing, delay calculation, and RC data being reset for all analysis views.

→ In MMMC browser, double-click the name of the constraint mode object you want to edit.



Fields and Options

Name	Displays the name of the constraint mode object being edited.
SDC Constraint Files	Displays the SDC constraint files that are associated with the constraint mode object. Use the *Add* button to add SDC files to the list. Use the *Delete* button to delete SDC files from the list.
ILM Constraint Files	Displays the SDC constraint files for the ILM flow that are associated with the constraint mose object. Use the *Add* button to add SDC files to the list. Use the *Delete* button to delete SDC files from the list.

Related Text Commands

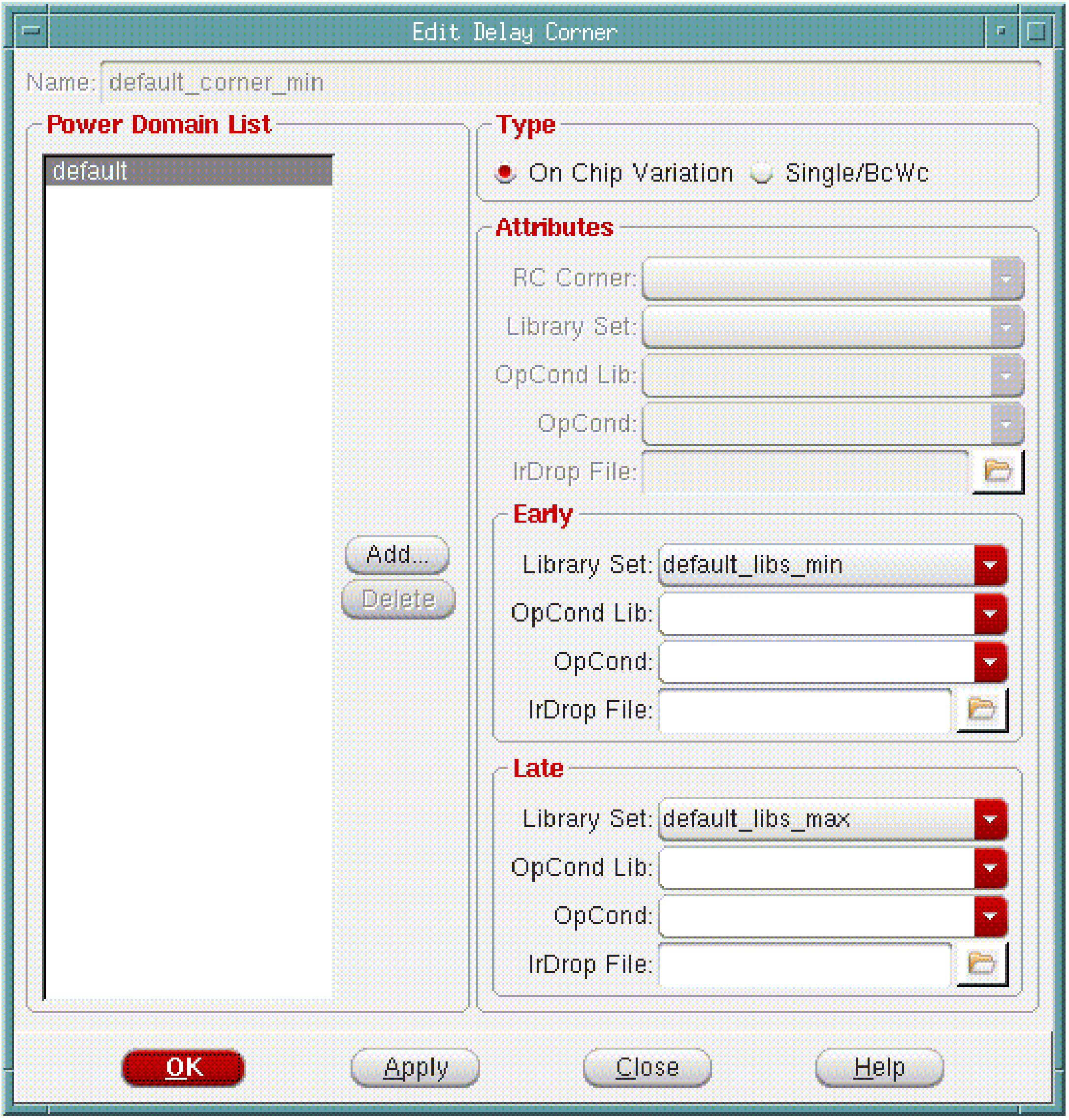
- `update_constraint_mode`

Edit Delay Corner

Use the Edit Delay Corner form to add, delete, or change attributes for an existing delay calculation corner object.

ⓘ You can edit a delay calculation corner object using the Edit Delay Corner form before multi-mode multi-corner view definitions are loaded into the design, or after. However, after the software is in multi-mode multi-corner analysis mode, any change to an existing analysis view results in the timing, delay calculation, and RC data being reset for all analysis views.

→ In MMMC browser, double-click the name of the delay calculation corner you want to edit.



Fields and Options

Name	Displays the name for the delay calculation corner object being edited.
Type	Specifies the type of analysis for which you are configuring the multi-mode multi-corner environment. When running Single or Best-Case Worst-Case (BcWc) timing analysis, a delay calculation corner generally contains one library set and one RC corner object. When running on-chip-variation timing analysis, a delay calculation corner can contain early and late library sets and RC corners. **Note:** If you use a delay calculation corner containing early and late attributes when the software is in BC-WC mode, the software uses the early information for analysis of hold views, and the late information for the analysis of setup views.
RC Corner	Specifies an RC corner object to associate with this delay calculation corner object.
Library Set	Specifies a library set to associate with this delay calculation corner object.
OpCond Lib	Specifies the internal library name for the library in which the operating condition is defined. This is *not* the library file name.
OpCond	Specifies an operating condition to use for setup and hold analysis.
IrDrop File	Specifies the IR drop files to apply to both early and late delay calculation for this delay corner object.
Early Library Set	Specifies a library set to associate with this delay calculation corner object for calculating early arrival times at a single delay calculation corner.
Early OpCond Lib	Specifies the internal library name for the library in which the early operating condition is defined. This is *not* the library file name.
Early OpCond	Specifies an operating condition to use for calculating early arrival times at a single delay calculation corner.
Early IrDrop File	Specifies the IR drop files to apply when calculating early arrival times at a single delay corner.

Late Library Set	Specifies a library set to associate with this delay calculation corner object for calculating late arrival times at a single delay calculation corner.
Late OpCond Lib	Specifies the internal library name for the library in which the late operating condition is defined. This is *not* the library file name.
Late OpCond	Specifies an operating condition to use for calculating late arrival times at a single delay calculation corner.
Late IrDrop File	Specifies the IR drop files to apply when calculating late arrival times at a single delay corner.
Power Domain List	Displays a list the delay calculation corner's power domain definitions. To add a power domain definition to the delay calculation corner, click the *Add* button to open the Add Power Domain form. To delete a power domain definition from the delay calculation corner, choose the power domain in the list and click the *Delete* button.

Related Text Commands

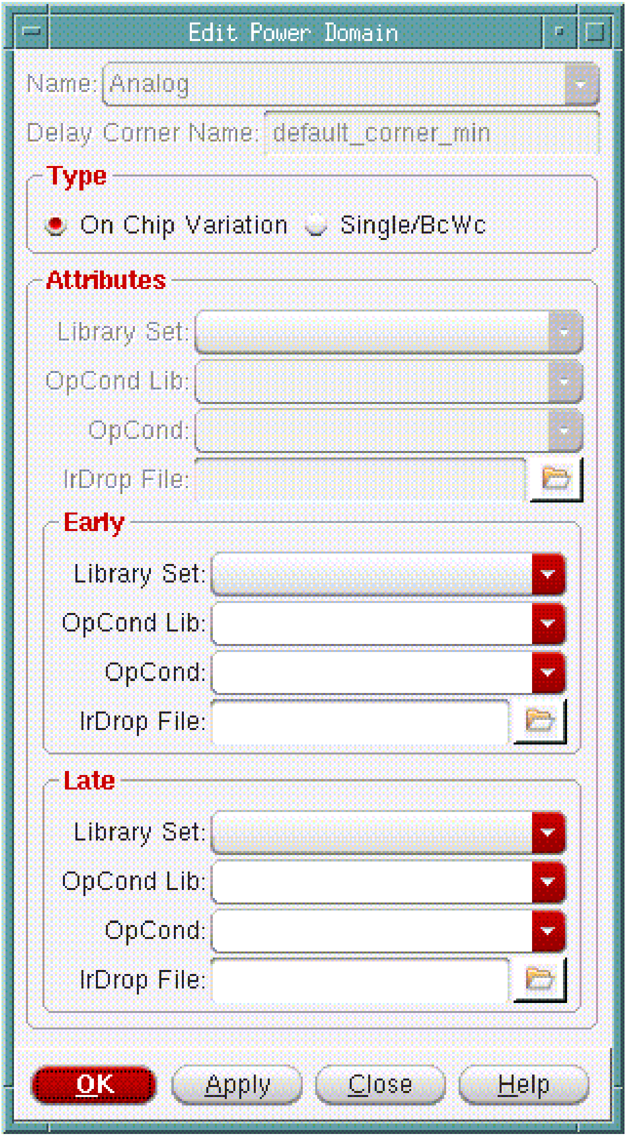
- `update_delay_corner`

Edit Power Domain

Use the Edit Power Domain form to add, delete, or change attributes for an existing power domain definition.

> ⓘ You can edit a power domain using the Edit Power Domain form before multi-mode multi-corner view definitions are loaded into the design, or after. However, after the software is in multi-mode multi-corner analysis mode, any change to an existing analysis view results in the timing, delay calculation, and RC data being reset for all analysis views.

→ In MMMC browser, click the + next to *Delay Corners* to list the available delay corners, click the + next to the delay corner to which the power domain definition belongs, and double click on the name of the power domain definition.



Fields and Options

Name	Displays the name of the power domain being edited.
Delay Corner Name	Displays the delay calculation corner to which to the power domain definition belongs.

Type	Specifies the type of analysis for which you are configuring the multi-mode multi-corner environment. When running Single or Best-Case Worst-Case (BcWc) timing analysis, a power domain generally contains one library set and operating condition. When running on-chip-variation timing analysis, a power domain can contain early and late library sets and operating conditions.
Attribute Library Set	Specifies a library set to associate with the power domain. All of the cells and macros in the power domain get their timing and power information from these libraries.
Attribute OpCond Lib	Specifies the internal library name for the library in which the operating condition is defined. This is *not* the library file name.
Attribute OpCond	Specifies an operating condition to use for the power domain.
Attribute IrDrop File	Specifies the IR drop files to apply to both early and late delay calculation for this power domain object.
Early Library Set	Specifies a library set to associate with the power domain for calculating early arrival times at a single delay corner.
Early OpCond Lib	Specifies the internal library name for the library in which the early operating condition is defined. This is *not* the library file name.
Early OpCond	Specifies an operating condition to use for calculating early arrival times at a single delay corner.
Early IrDrop File	Specifies the IR drop files to apply when calculating early arrival times at a single power domain.
Late Library Set	Specifies a library set to associate with this delay corner object for calculating late arrival times at a single delay corner.

Late OpCond Lib	Specifies the internal library name for the library in which the late operating condition is defined. This is *not* the library file name.
Late OpCond	Specifies an operating condition to use for calculating late arrival times at a single delay corner.
Late IrDrop File	Specifies the IR drop files to apply when calculating late arrival times at a single power domain.

Related Text Commands

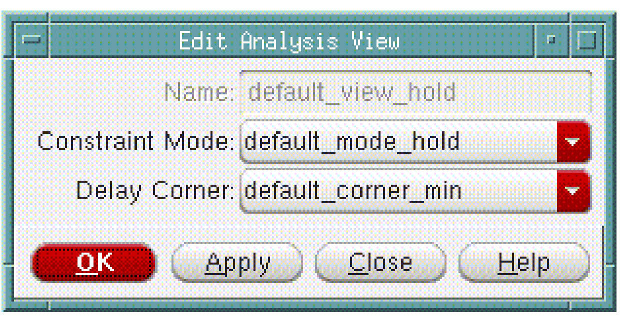
- `update_delay_corner`

Edit Analysis View

Use the Edit Analysis View form to add or delete constraint mode and delay corner objects from an existing anaylsis view.

> You can edit an analysis view using the Edit Analysis view form before multi-mode multi-corner view definitions are loaded into the design, or after. However, after the software is in multi-mode multi-corner analysis mode, any change to an existing analysis view results in the timing, delay calculation, and RC data being reset for all analysis views.

→ In MMMC browser, double-click the name of the analysis view you want to edit.



Fields and Options

Name	Displays the name of the analysis view being edited.
Constraint Mode	Specifies the name of the constraint mode to associate with this analysis view.
Delay Corner	Specifies the name of the delay corner to associate with this analysis view.

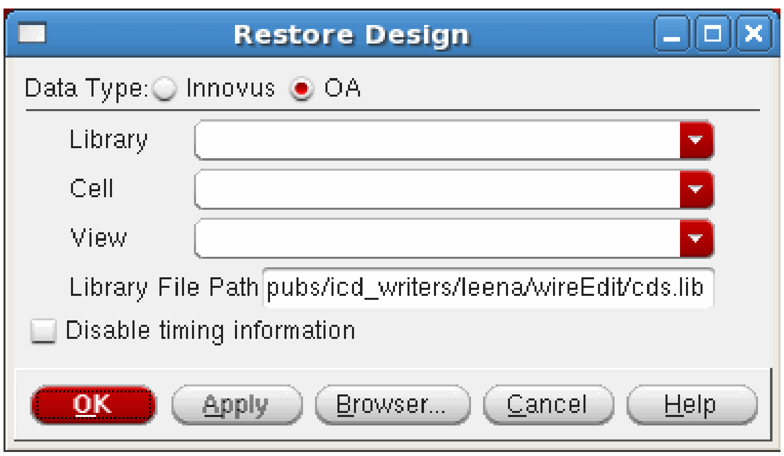
Related Text Commands

- `update_analysis_view`

Restore Design

Use the Restore Design form to load saved data from a previous design session and using the OpenAccess database format.

- Choose *File - Restore Design*.



The Restore Design form has two pages:

- OA Page
- Innovus Page

OA Page

The OA page within the Restore Design form is used to restore all design information from the previous design session, using the OpenAccess database format.

Restore Design - OA Fields and Options

Library	Specifies the location of the OpenAccess database to be restored. It contains the cell and the view to be restored. The OpenAccess library name should be specified in the `cds.lib` file. The Import Design form contains *Verilog* and *OA* radio button that changes the form from the current LEF based style (default) and includes the OpenAccess-based style.
Cell	Specifies the design cell from the library that is to be restored.
View	Specifies the view name of the cell that is to be restored. The values in this field are set by the *Save OA Design* form when you saved the design in the previous session. *Default:* The layout view.
Library File Path	Specifies the full path to the library definitions file (`cds.lib`).
Disable timing information	Disables reading of timing libraries and constraints during the restore design process.
Browser button	Opens the Library Browser form, which enables you to browse available libraries, cells, views.

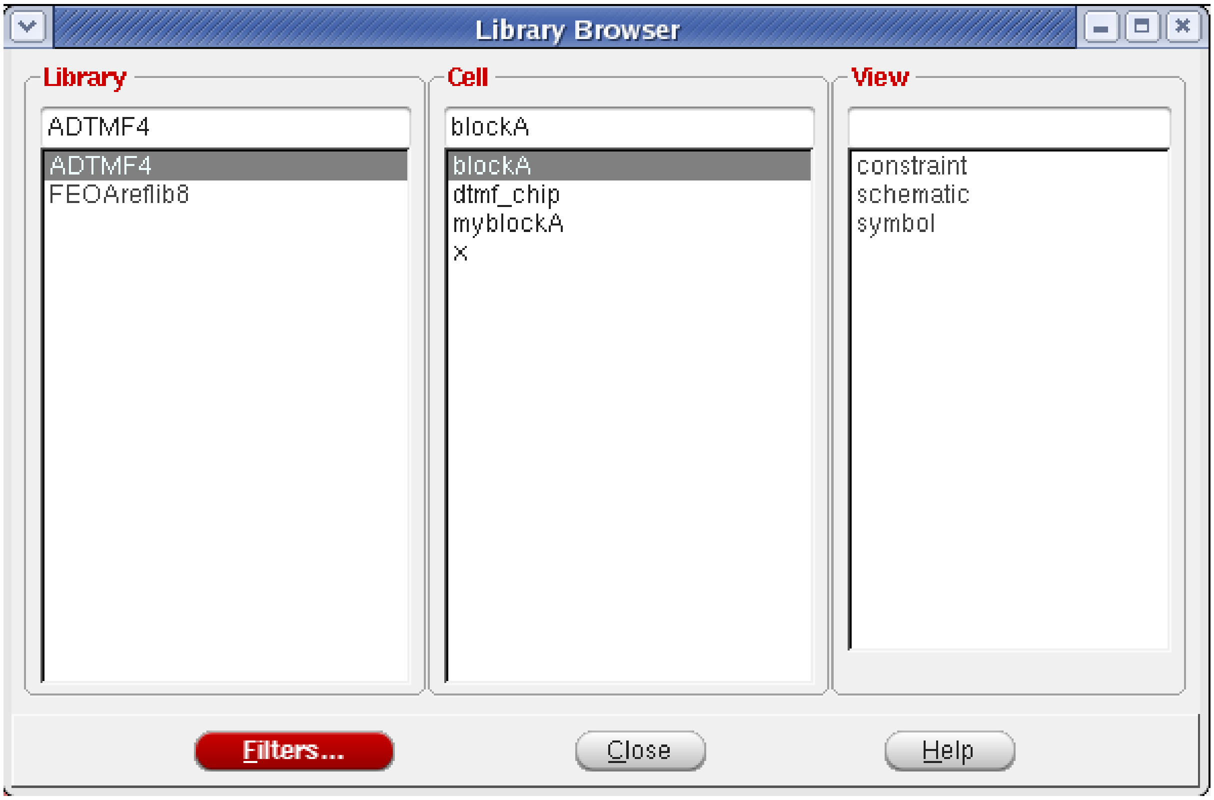
Related Text Commands

- `restoreDesign`

Library Browser

Use Library Browser to browse available library, cell, views, when restoring an OpenAccess design. To open the form:

1. Choose *File - Restore Design.*
2. On the default OA page of the Restore Design form, click the *Browser* button.

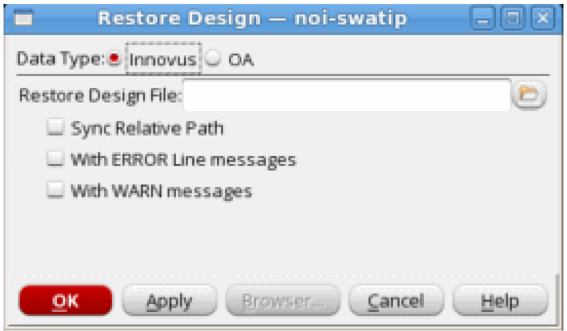


Library Browser - Fields and Options

Library	Lists the available libraries.
Cell	Lists the available cells for the selected library.
View	Lists the available views for the selected cell.

Innovus Page

Use the *Restore Design* form to load saved data from a previous design session.



Restore Design - Innovus Fields and Options

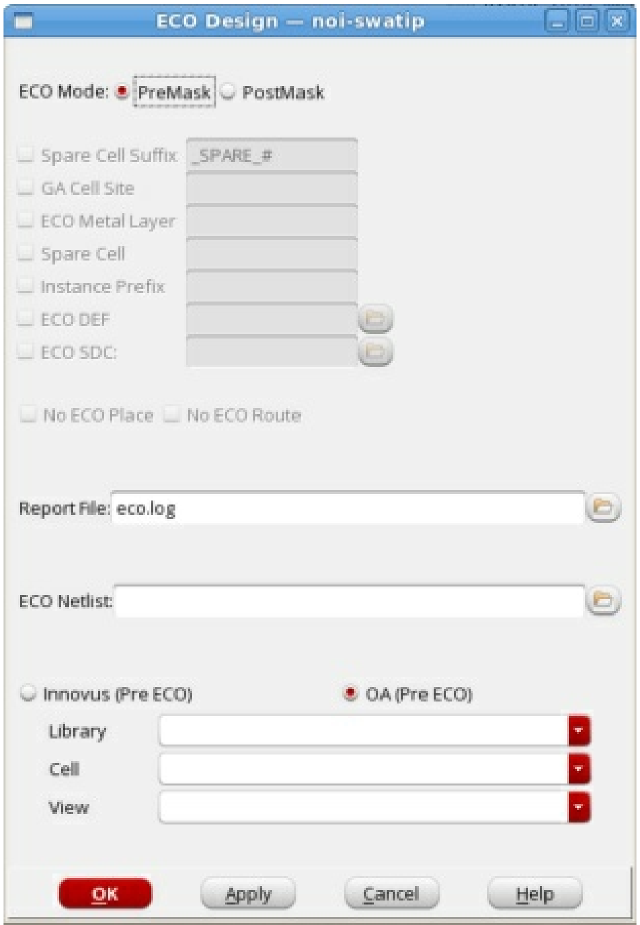
Restore Design File	
	Specifies the design file to restore.
Sync Relative Path	Synchronizes all relative paths in the configuration file to the current working directory. *Default:* Off
With ERROR Line messages	
	Displays information messages while restoring the design. *Default:* Off
With WARN messages	Displays any warning messages while restoring the design. *Default:* Off

Related Text Commands

- `restoreDesign`

ECO Design

Use the ECO Design form to select options related to making ECO changes to the design.
→ Choose *File - ECO Design*.



ECO Design Fields and Options

PreMask	Indicates that the ECO changes are being made to a pre-mask design. *Default:* On
PostMask	Specifies the options that are available during the post-mask ECO process. *Default:* Off
Spare Cell Suffix	Specifies the suffix to be appended to spare cell names. *Default:* `_SPARE_#`
GA Cell Site	Specifies the location of the gate array cells. *Default:* Off

ECO Metal Layer	Specifies the layers to be modified during the ECO process. *Default:* Off
Spare Cell	Specifies the name of the spare cell to be modified during the ECO process. *Default:* Off
Instance Prefix	Specifies the filler cell instance prefix.
ECO DEF	Specifies the DEF file you want the software to load automatically when performing ECO.
ECO SDC	Specifies the name of the new sdc file. *Default:* Off
No ECO Place	Prevents placement and routing during the ECO process.
No ECO Route	Prevents routing during the ECO process. *Default:* Off
ReportFile	Specifies a report file. Default: `eco.log`
Eco Netlist	Specifies the name of the new netlist with the design changes to be implemented.
OA (Pre ECO)	Takes an OpenAccess database as input. *Default:* On
Library	Specifies the OpenAccess library name.
Cell	Specifies the OpenAccess cell name of the top cell to import.
View	Specifies the OpenAccess view name to import.
Innovus (Pre ECO)	Takes an Innovus database as input. *Default:* Off
Top Cell	Specifies the name of the top cell.

Pre Eco Design	Specifies the name of the design to be modified.

Related Text Command

- `ecoDesign`
- `ecoOaDesign`

Save Design

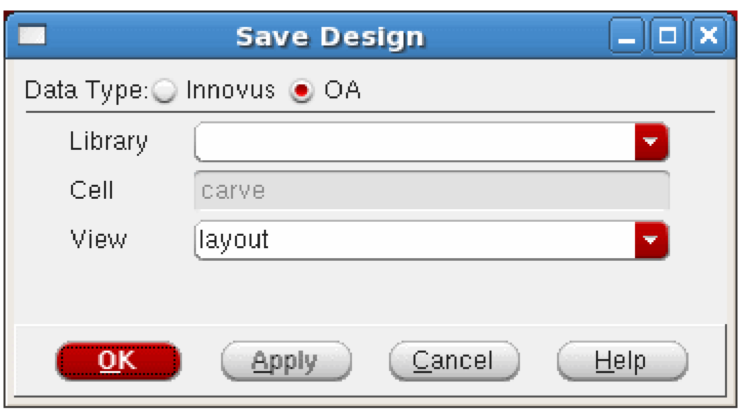
The Save Design form enables you to save design files from the Innovus session and to save all design information using the OpenAccess database format.

The Save Design form contains the following two pages:

- Save Design - OA
- Save Design - Innovus

Save Design - OA

Use the OA page in the Save Design form to save all information from the current design session, using the OA database format.
→ Choose *File - Save Design. The OA* page opens by default.



Save Design - OA Fields and Options

Library	Specifies the target OpenAccess library name. **Note:** *File - Save Design - OA* can create libraries and their entries in the `cds.lib` file but it is recommended that you create libraries using `createLib` before the database is saved. This allows you to define the technology structure to be used for the library (the *Attach to an existing technology library*, *Copy from an existing technology library*, and *Reference existing technology libraries* parameters can be used with the `createLib` command).
Cell	Specifies the top cell that is to be saved. **Note:** This field is read-only.
View	Specifies the view to save.
Note: The *OA Reference Libraries* and *OA Abstract View Names* fields from the *File - Import Design* form are used when saving the design for the first time. If the design is loaded using *File - Restore Design - OA,* then the reference libraries and abstract names specified in the design are used. **Note:** While saving a lib/cell/view to a different cellview, the overwrite is not allowed by default. So, you will be prompted to overwrite.	

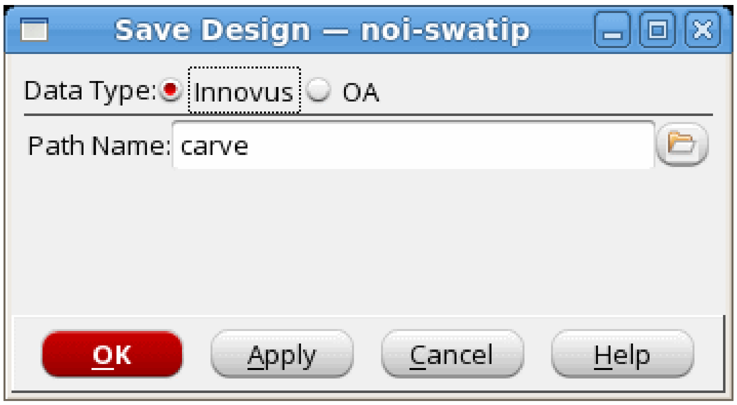
Related Text Commands

For information on the following command, see "Import Commands" in the *Innovus Text Command Reference*.

- `saveDesign`

Save Design - Innovus

Use the Innovus page of the Save Design form to save design files in a user-specified directory at anytime in a design session. Only files that exist during the save are copied to the directory.
→ Choose *File - Save Design* and click the *Innovus* option button.



Save Design - Innovus Fields and Options

File Name *Path Name*	Enter the name of the file to which you want to save the design. Click the button next to the field to choose the directory where you can save your file.

Related Text Commands

For information on the following command, see "General Commands" in the *Innovus Text Command Reference*.

- saveDesign

Related Topics

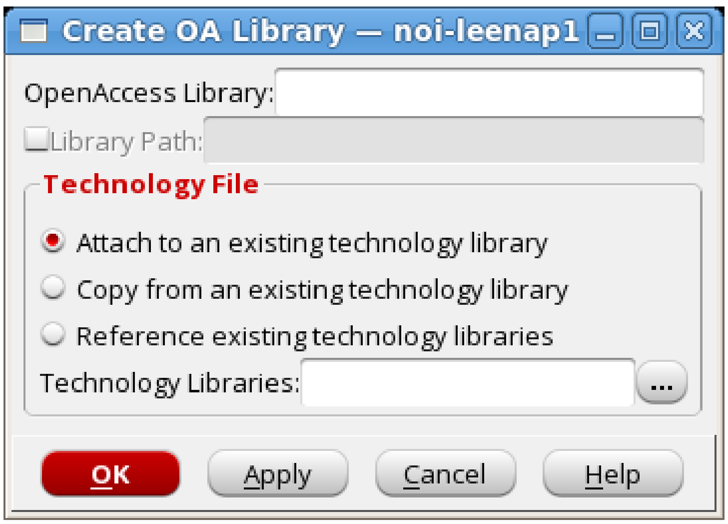
For information on the following topic, see "Importing and Exporting Designs" in the *Innovus User Guide*.

- Saving Designs

Create OA Library

The Create OA Library form lets you copy or attach a technology database to a library.

- Choose *File* - *Create OA Library*



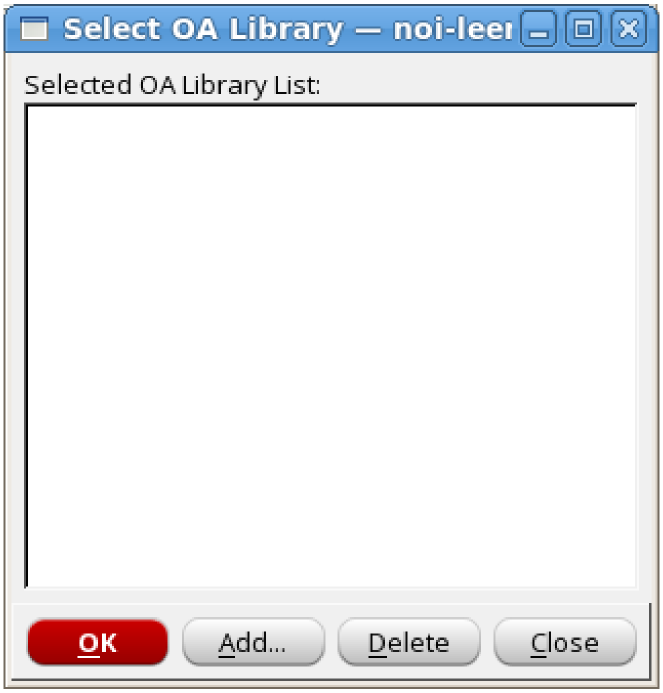
Create OA Library Fields and Options

OpenAccess Library	Specifies the name of the library to be created.
Library Path	Specifies the name of a directory in which to save the library. The path you specify must include the directory that will become the library itself. *Default*: Library name specified in the *OpenAccess Library* field will be created in the current working directory.
Attach to an existing technology library	Attaches the technology database specified by the technology library to the library when this option is selected. **Note:** If this option is selected, the technology library is referred in read-only mode.
Copy from an existing technology library	Copies the technology database specified by technology library name to the library specified. You can specify only one technology library when this option is selected.
Reference existing technology libraries	Creates a local technology database in the design library that can be modified incrementally. You can specify one or more technology libraries when this option is selected.
Technology Libraries	Specifies the library containing the technology data to be used for attaching/copying/referencing the technology database. You cannot use this field if you choose to create the technology database from memory. **Note:** The browse (...) button next to this field opens a form from which you can select technology libraries, instead of typing the names of these libraries.

Select OA Library

The *Select OA Library* form lets you select an OpenAccess library.

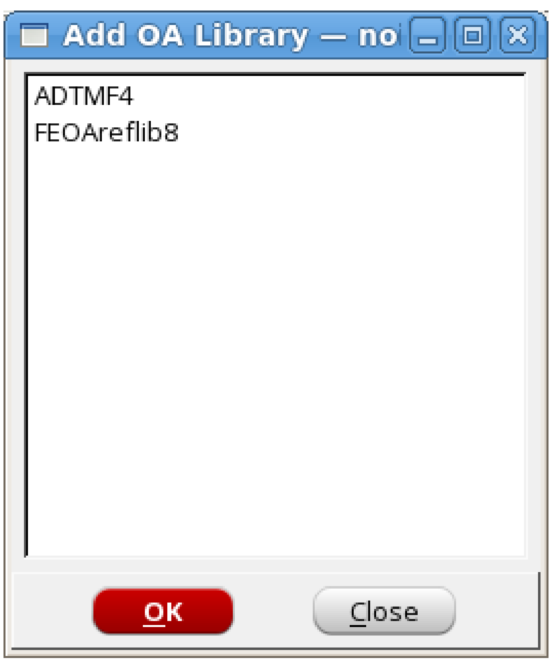
- Select the *...* button next to the *Technology Libraries* field.



Add OA Library

The *Add OA Library* form lets you add an OpenAccess library.

- Select the *Add* button on the *Select OA Library* form.



Load

The *File* menu's *Load* forms enable you to restore individual design files during a design session. The following options are available:

- Load - Partition
- Load - Floorplan
- Load - I/O File
- Load - Place
- Load - DEF
- Load - PDEF
- Load - SPEF
- Load - SDF
- Load - OA Cellview

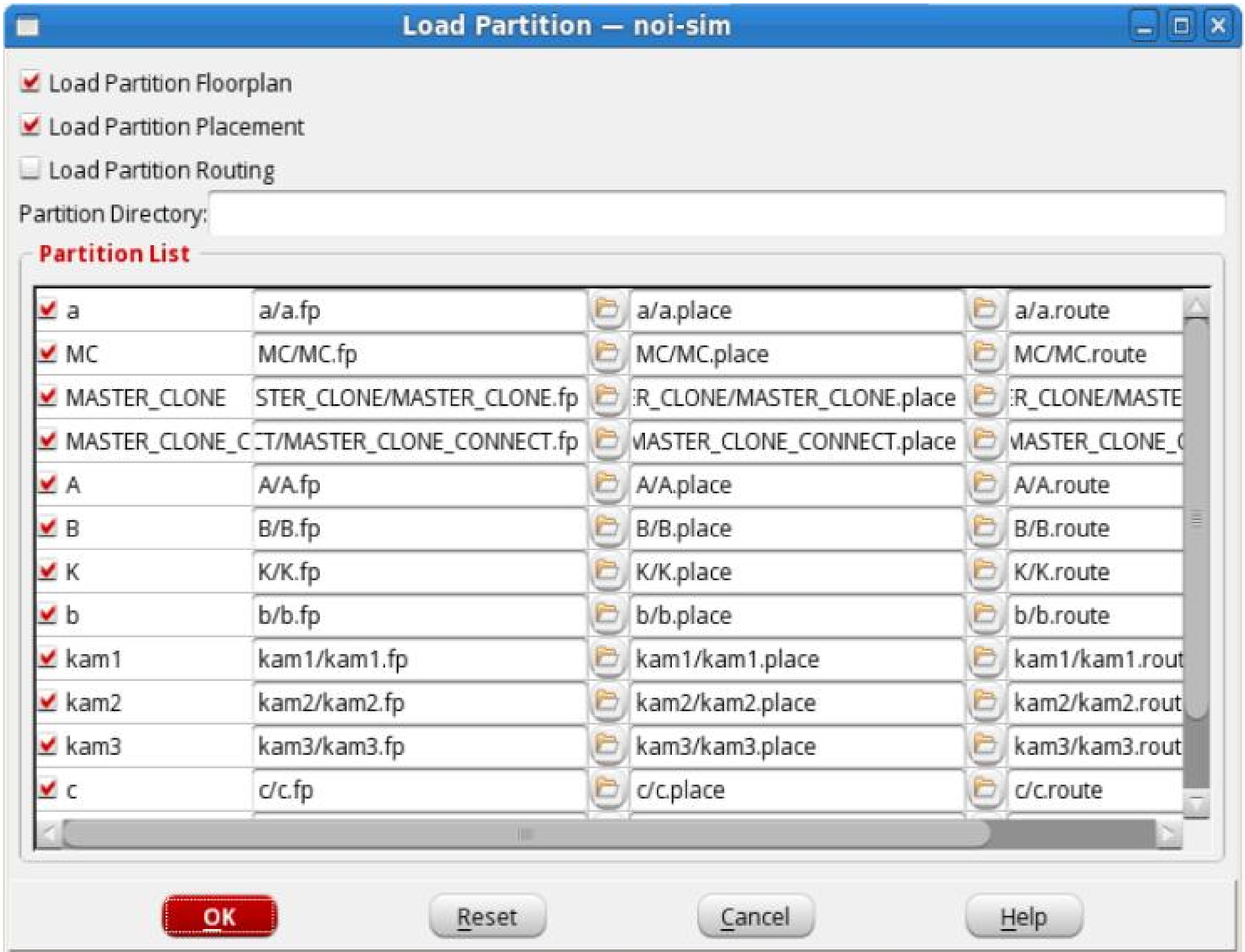
Related Topics

For more information on loading individual design files, see the following topic in the Importing and Exporting Designs chapter in the *Innovus User Guide*.

- Loading and Saving Design Data

Load - Partition

Use the Load Partition form to load partition floorplan, placement, and routing files. Loading the partition data to the top level prepares the partition for timing budget refinement flow and top-level timing analysis.
→ Choose *File - Load - Partition.*


Load Partition — noi-sim
Load Partition Floorplan
Load Partition Placement
Load Partition Routing
Partition Directory:
Partition List
a
a/a.fp
a/a.place
a/a.route
MC
MC/MC.fp
MC/MC.place
MC/MC.route
MASTER_CLONE
STER_CLONE/MASTER_CLONE.fp
R_CLONE/MASTER_CLONE.place
R_CLONE/MASTE
MASTER_CLONE_C
T/MASTER_CLONE_CONNECT.fp
MASTER_CLONE_CONNECT.place
MASTER_CLONE_
A
A/A.fp
A/A.place
A/A.route
B
B/B.fp
B/B.place
B/B.route
K
K/K.fp
K/K.place
K/K.route
b
b/b.fp
b/b.place
b/b.route
kam1
kam1/kam1.fp
kam1/kam1.place
kam1/kam1.rout
kam2
kam2/kam2.fp
kam2/kam2.place
kam2/kam2.rout
kam3
kam3/kam3.fp
kam3/kam3.place
kam3/kam3.rout
c
c/c.fp
c/c.place
c/c.route
OK
Reset
Cancel
Help

Load Partition Fields and Options

Load Partition Floorplan	
	Allows you to load a partition floorplan file.
Load Partition Placement	
	Allows you to load a partition placement file.
Load Partition Routing	
	Allows you to load a partition routing file.
Partition Directory	Directory name where the partition data was saved.
Partition List	Allows you to browse and select a floorplan, placement, or routing file for each module partition. **Note:** All the partitioned modules are displayed as hard blocks.

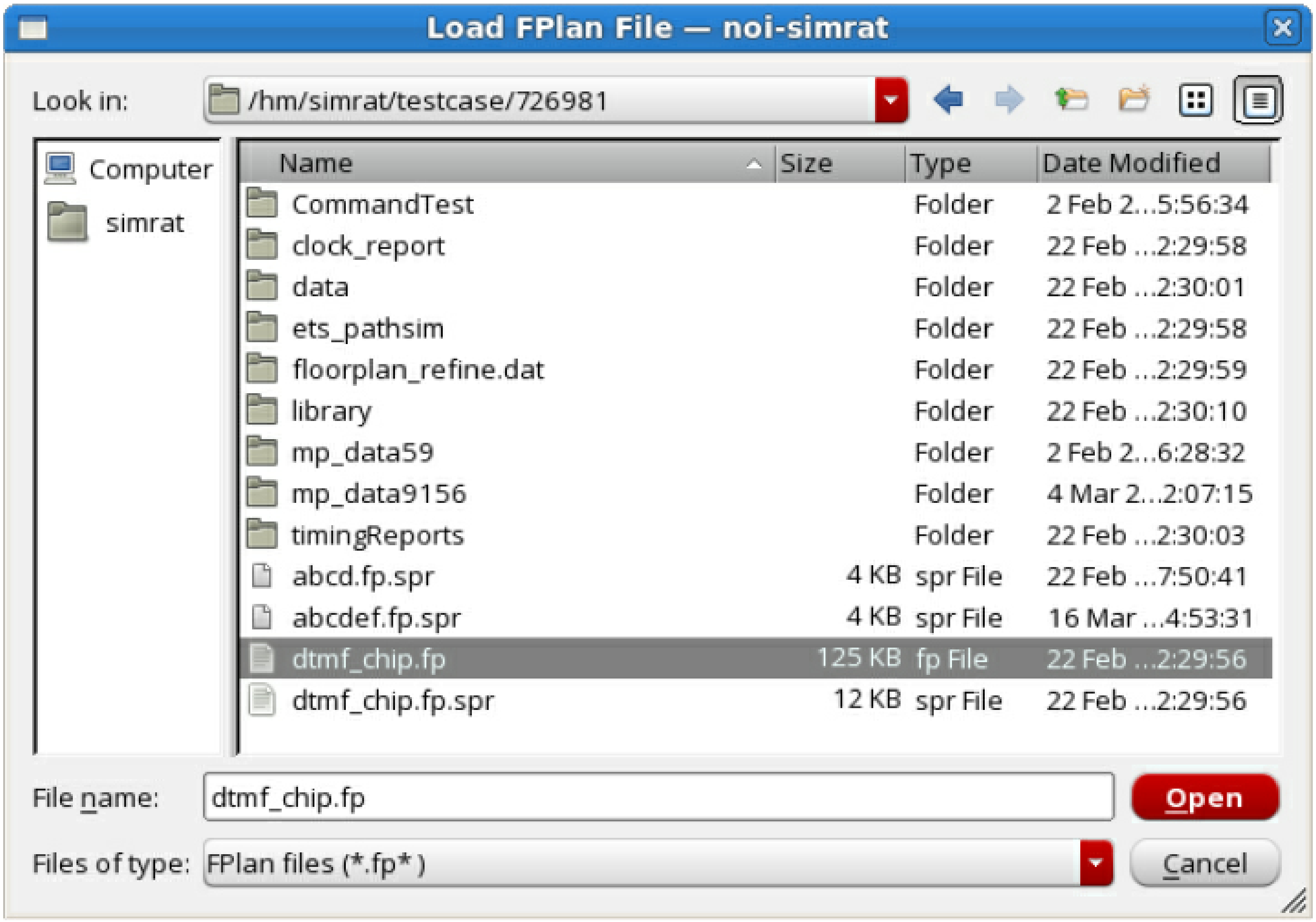
Related Text Commands

The following text command provides equivalent or additional functionality:

- `loadFPlan`
- `setTopCell`

Load - Floorplan

Use the Load FPlan File form to load floorplan data for a design session.
→ Choose *File - Load - Floorplan.*



Load FPlan File Fields and Options

Look in	Displays the name and contents of a directory where you can load your file. Click on the Look in pull-down to choose a different directory.
File name	Enter the name of the file containing the floor plan data you want to load.
Files of type	Specifies a file display filter. The default is `.fp`.

Related Text Commands

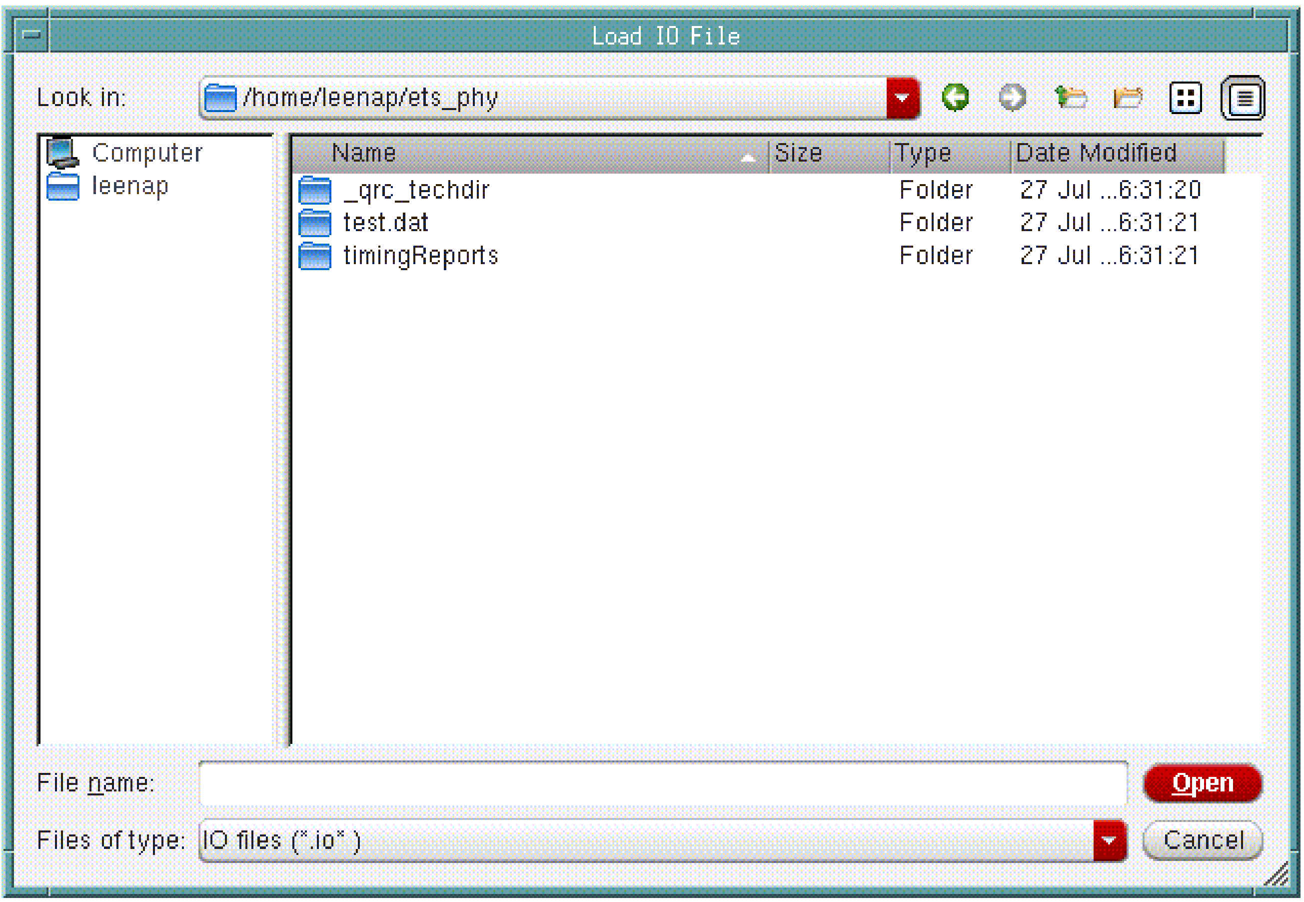
The following text command provides equivalent or additional functionality:

- `loadFPlan`

Load - I/O File

Use the Load IO File form to load an I/O assignment file.

→ Choose *File - Load - I/O File*.



Load I/O File Fields and Options

Look in	Displays the name and contents of a directory where you can load your file. Click on the Look in pull-down to choose a different directory.
File name	Enter the name of the file containing the I/O file you want to load.
Files of type	Specifies a file display filter. The default is `.io`.

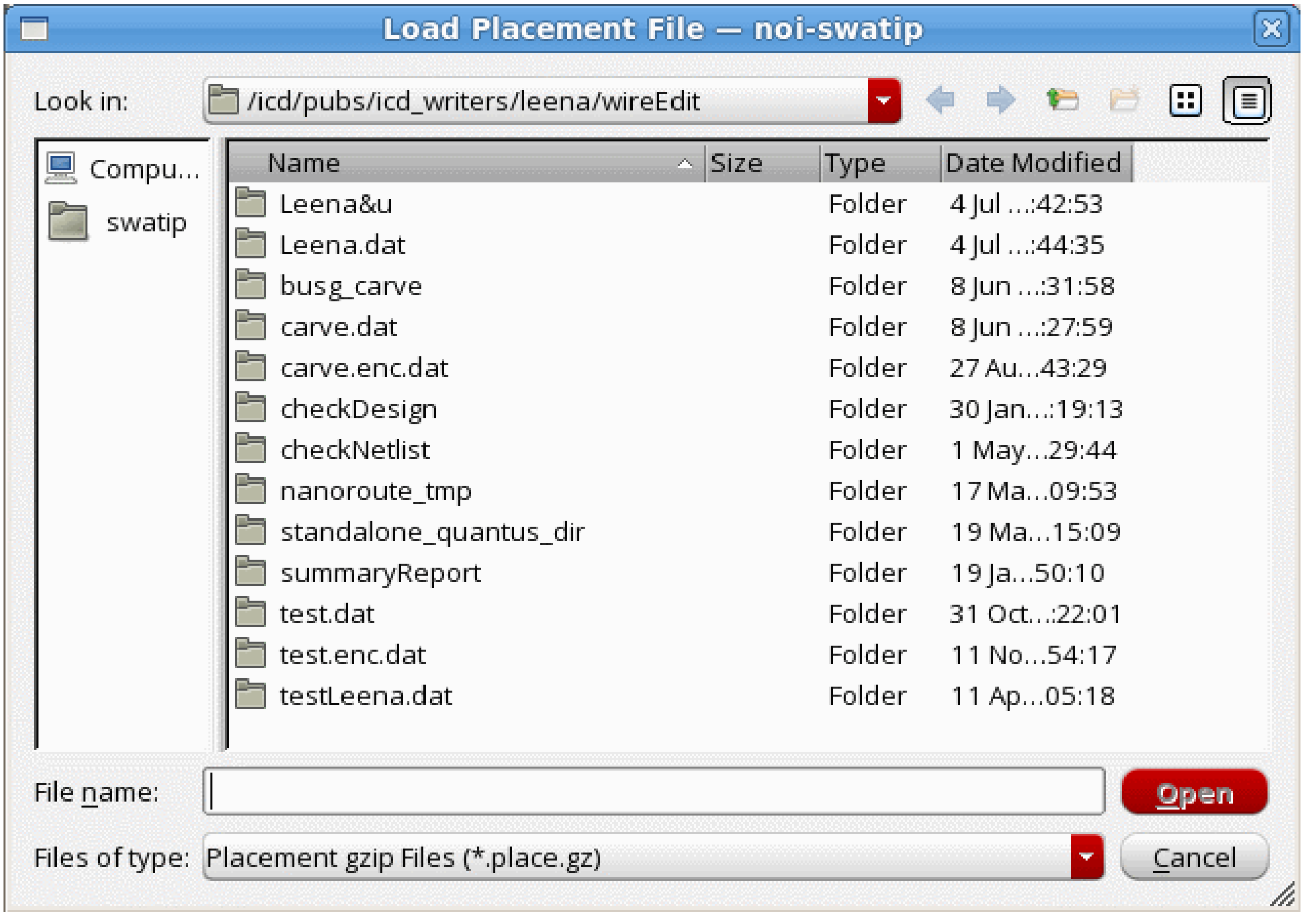
Related Text Commands

The following text command provides equivalent or additional functionality:

- `loadIoFile`

Load - Place

Use the Load Placement File form to restore placement data from a previous design session. You can restore the data from a file that was previously saved in Innovus.
→ Choose *File - Load - Place.*



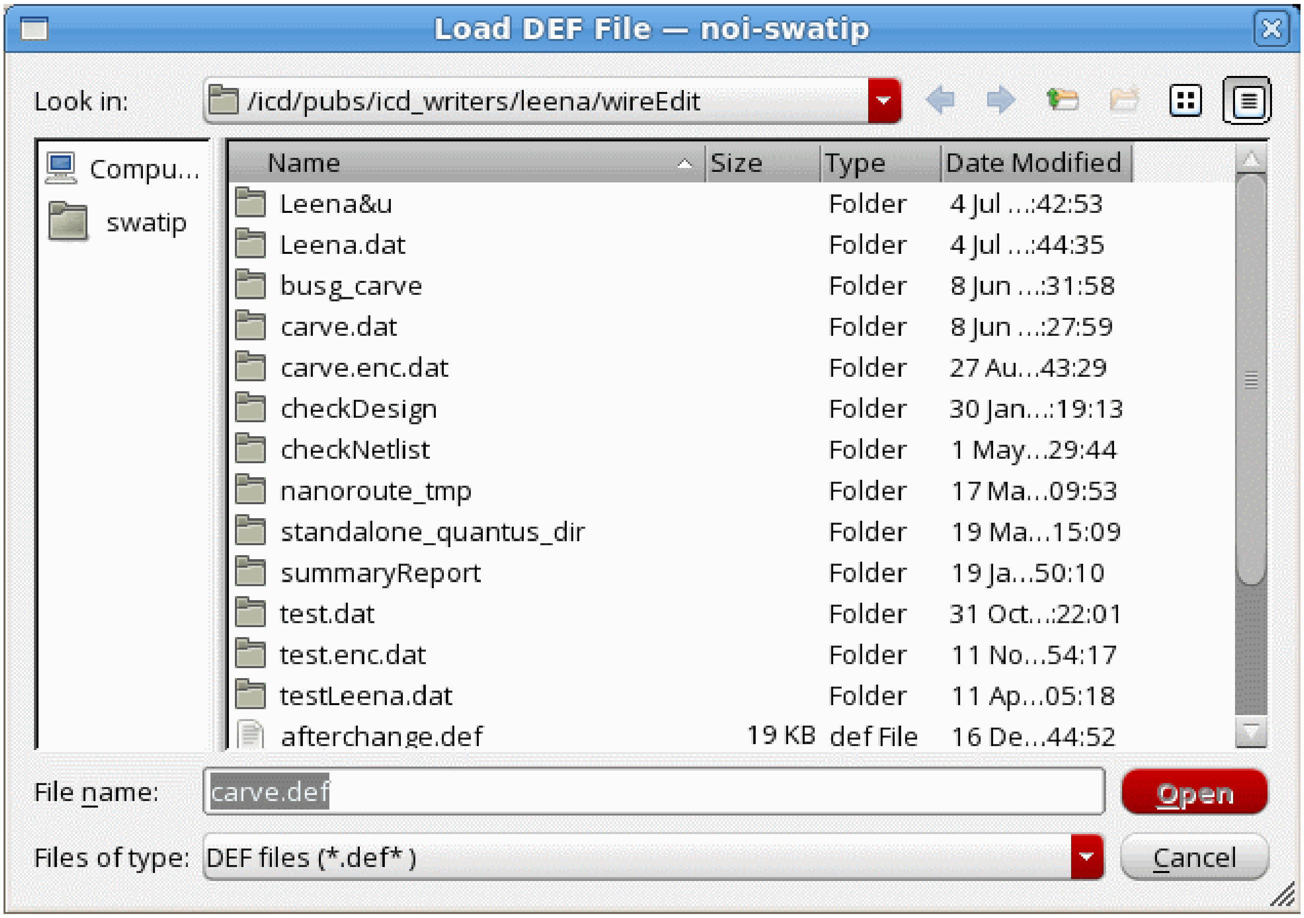
Load Placement Fields and Options

Look in	Displays the name and contents of a directory where you can load your file. Click on the Look in pull-down to choose a different directory.
File name	Enter the name of the file containing the placement data you want to load.
Files of type	Specifies a file display filter. The default is `.place`.

Load - DEF

Use the Load DEF File form to load a Design Exchange Format (DEF) file.

→ Choose *File - Load - DEF*.



Load DEF File Fields and Options

Look in	Displays the name and contents of a directory where you can load your file. Click on the Look in pull-down to choose a different directory.
File name	Enter the name of the file containing the DEF file you want to load.
Files of type	Specifies a file display filter. The default is `.def`.

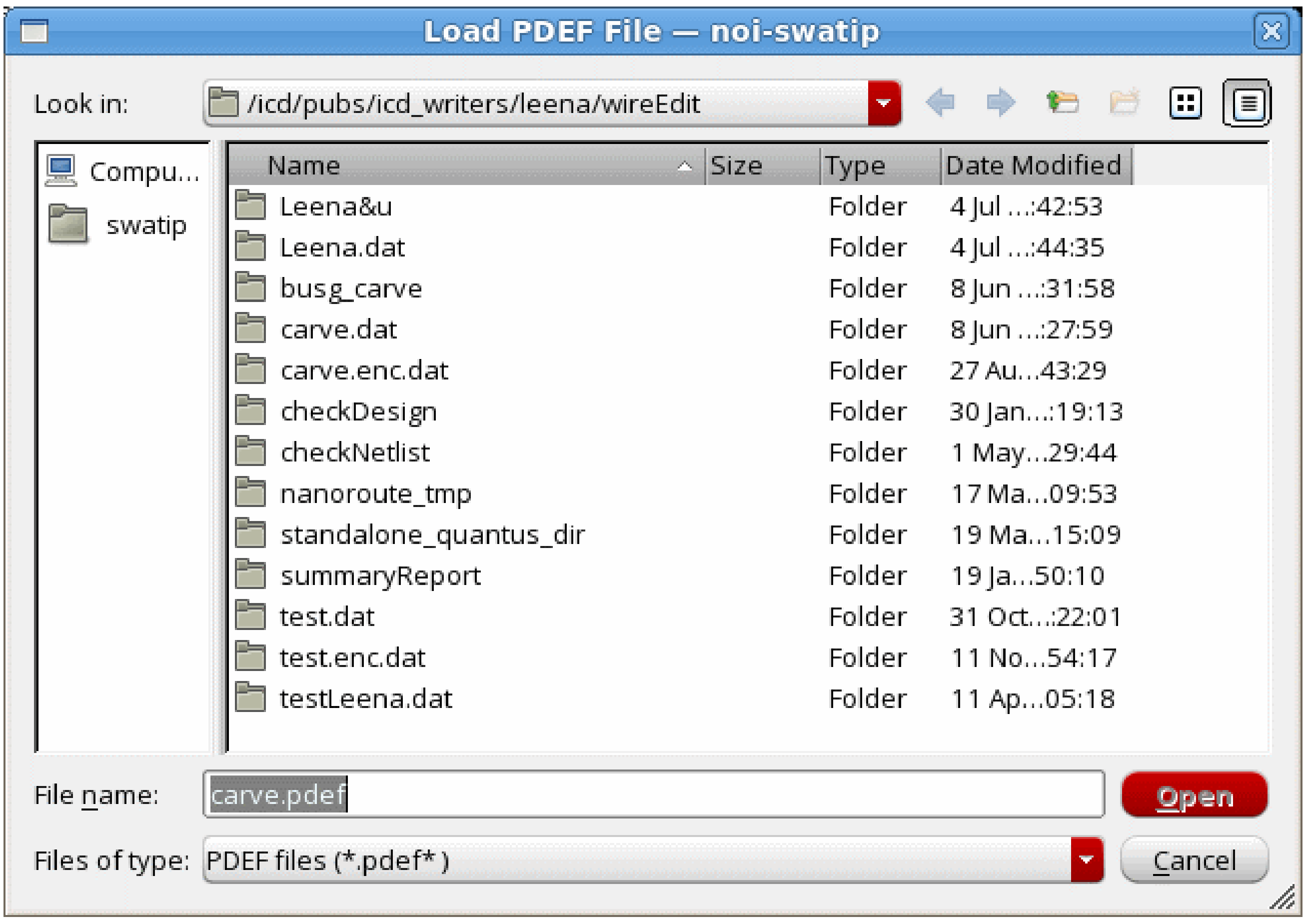
Related Text Commands

For information on the following command, see "Import Commands" in the *Innovus Text Command Reference*.

- `defIn`

Load - PDEF

Use the Load PDEF File form to load a Physical Design Exchange Format (PDEF) file.
→ Choose *File - Load - PDEF*.



Load PDEF File Fields and Options

Look in	Displays the name and contents of a directory where you can load your file. Click on the Look in pull-down to choose a different directory.
File name	Enter the name of the file containing the PDEF file you want to load.
Files of type	Specifies a file display filter. The default is `.pdef`.

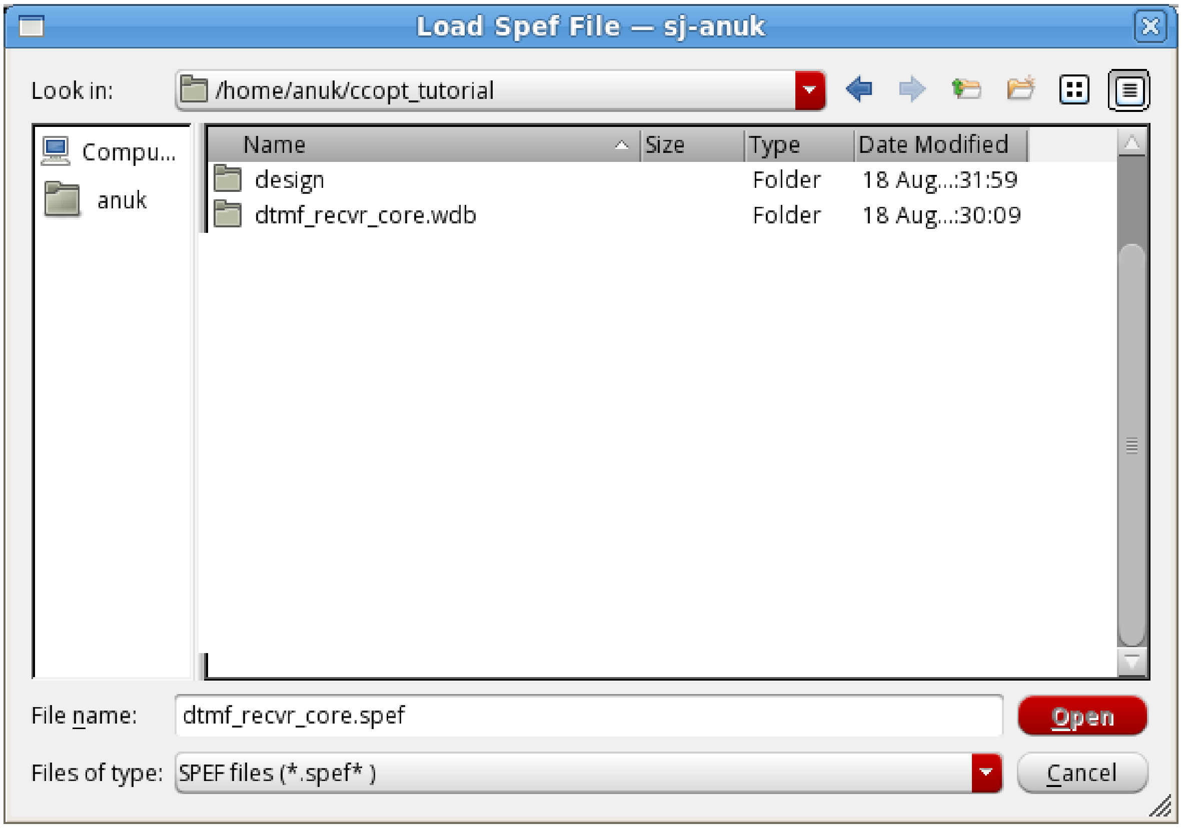
Load - SPEF

Use the Load SPEF form to load a SPEF file.
→ Choose *File - Load - SPEF.*

Load SPEF Fields and Options

SPEF File	Specify the name of the SPEF file you want to load.
RC Corner	Specify the name of the corresponding RC Corner.

→ When you Browse to specify the SPEF file, the following form opens:



Load SPEF File Fields and Options

Look in	Displays the name and contents of a directory where you can load your file. Click on the Look in pull-down to choose a different directory.
File name	Enter the name of the file containing the SPEF file you want to load.
Files of type	Specifies a file display filter. The default is `.spef`.

Related Text Commands

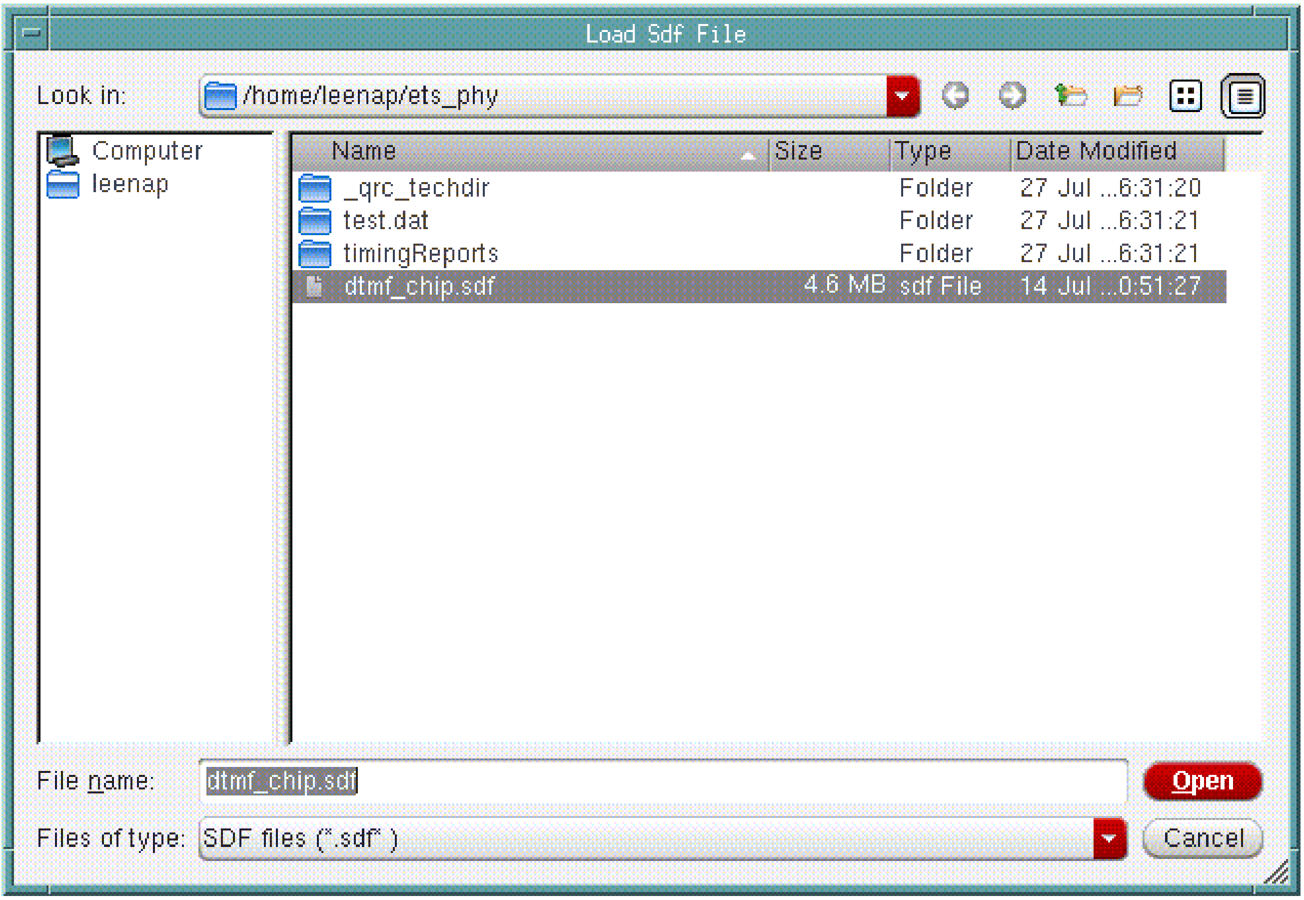
For information on the following command, see "RC Extraction Commands" in the *Innovus Text Command Reference*.

- `spefIn`

Load - SDF

Use the Load SDF form to load an SDF file.

→ Choose *File - Load - SDF.*



Load SDF File Fields and Options

Look in	Displays the name and contents of a directory where you can load your file. Click on the Look in pull-down to choose a different directory.
File name	Enter the name of the file containing the SDF file you want to load.
Files of type	Specifies a file display filter. The default is `.sdf`.

Related Text Commands

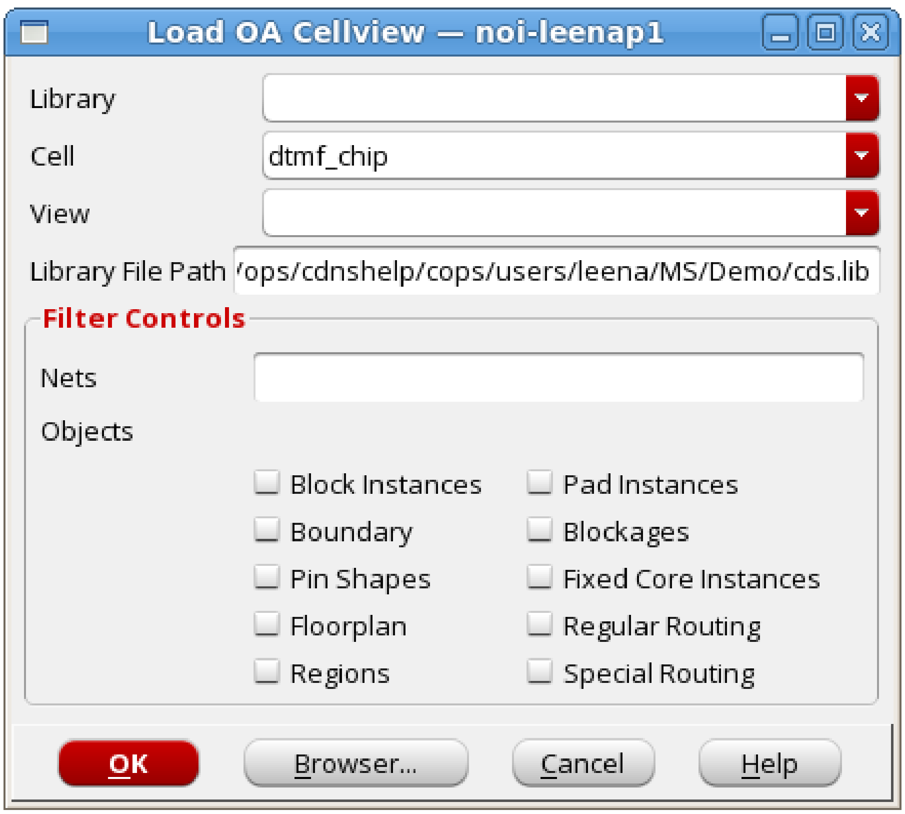
For information on the following command, see "Timing Commands" in the *Innovus Text Command Reference*.

- read_sdf

Load - OA Cellview

Use the Load OA Database form to load floorplan, placement, and routing information in the OpenAccess format.

- Choose *File - Load - OA Cellview*.



Load OA Database Fields and Options

Library	Specifies the name of the OpenAccess library where the design has been saved.	
Cell	Specifies the name of the top cell.	
View	Specifies the name of the cell view to load.	
Library File Path	Specifies the path of the library file.	
Filter Controls	Allows you to load some data selectively, while not loading others. When this section is used, error checking for database consistency (nets, instances, terminals, etc.) is disabled. While similar to Virtuoso Load Physical View (LPV), the *Filter Controls* section is only a subset and not intended to be a complete replacement. Use the *Filter Controls* section to read floorplanning information from a cellview whose connectivity does not match the current Innovus in-memory connectivity. The section provides the following options.	
	Nets	Specifies the list of nets whose routing (routing and special) and constraints have to be read in. Shielding wiring/vias are also read in if they are used to shield any of the specified nets.

	Objects	Specifies the object types that should be read in. If you do not select any objects, all information is read from the OpenAccess cellview. The available object types are: • *Block Instances* - Indicates that any CLASS BLOCK instances should be updated. Physical-only block instances may be added to the database if the placement status is fixed or cover. • *Pad Instances* - Indicates that any CLASS PAD instances should be updated. Physical-only pad instances may be added to the database if the placement status is fixed or cover. • *Boundary* - Indicates that the design boundary information, including rows and tracks, should be updated. • *Blockages* - Indicates that blockages should be processed. If a blockage is attached to an instance that does not exist in the in-memory database, then it is ignored. • *Pin Shapes* - Indicates that pin shapes should be read. • *Fixed Core Instances* - Indicates that any CLASS CORE instances that have placement status fixed or cover should be updated. Physical-only core instances may be added to the database if the placement status is fixed or cover. • *Floorplan* - Is equivalent to selecting all of the following: *Block Instances, Blockages,* Boundary, *Fixed Core Instances, Pad Instances*, *Pin Shapes, Regions*, and *Special Routing.* • *Regular Routing* - Indicates that nets should be processed and regular routing (and associated shield net wiring) and net constraints updated. • *Regions* - Indicates regions should be updated. • *Special Routing* - Indicates that nets should be processed and special routing (except shield nets wiring) should be read.

Related Text Commands

`oaIn`

Save

The *File* menu's *Save* forms enable you to save individual design files during a design session. You can also save a detailed RC extraction file, but you cannot save a normal extraction file. You can save the design information at any time while working in a design session. You can then use this saved data to restore a design session.

The following options are available:

- Save - Partition
- Save - Floorplan
- Save - IO File
- Save - Place
- Save - Netlist
- Save - Testcase
- Save - DEF
- Save - PDEF
- Save - Timing Budget
- Save - GDS/OASIS

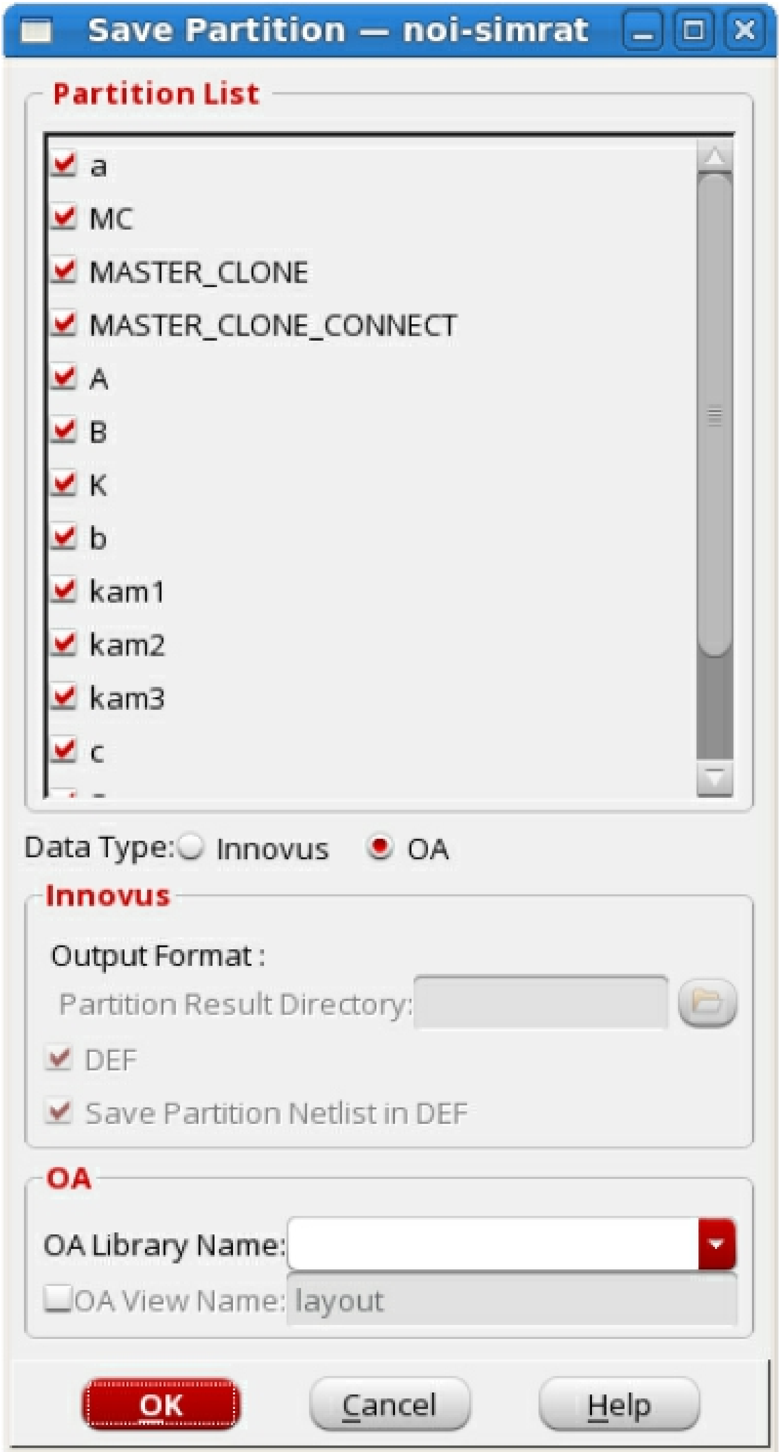
Related Topics

For more information on saving individual design files, see the following topic in the Importing and Exporting Designs chapter in the *Innovus User Guide*.

- Loading and Saving Design Data

Save - Partition

Use the Save Partition form to save the partition design files to separate partition directories.
→ Choose *File - Save - Partition*.


Save Partition — noi-simrat
Partition List
a
MC
MASTER_CLONE
MASTER_CLONE_CONNECT
A
B
K
b
kam1
kam2
kam3
c
Data Type:
Innovus
OA
Innovus
Output Format :
Partition Result Directory:
DEF
Save Partition Netlist in DEF
OA
OA Library Name:
OA View Name:
layout
OK
Cancel
Help

Save Partition Fields and Options

Partition List	Displays an entry for each module partition and one entry for the top-level partition. All the partitioned modules are displayed as hard blocks.
Data Type	Specifies the format in which the data should be saved: • *Innovus*: Specifies that the data should be saved in the native format of the Innovus software. • *OA*: Specifies that the data should be saved in the OpenAccess database format. *Default*: *OA*
Output Format	Specifies the output format. The files saved are used for specific back-end third-party tools. **Note:** The Verilog® netlist, configuration file, floorplan file, and cdump files are also saved.
Partition Result Directory	Specifies a directory name to save the resulting partition file. If a name is not entered, the top-level and partition directories are created in the work directory.
DEF	Writes out the DEF format files for the design.
Save Partition Netlist in DEF	Saves the partitioned netlist file for each partition in DEF. A top-level netlist file is also saved. The netlist is always saved in Verilog format for the top level and for each of the partitions.
OA Library Name	Specifies an OpenAccess database library directory where the top-level design and the block-level design for all the partitions will be saved.
OA View Name	Specifies the OpenAccess database view name for the top and the partition views. *Default:* The default value of this field is `layout`.

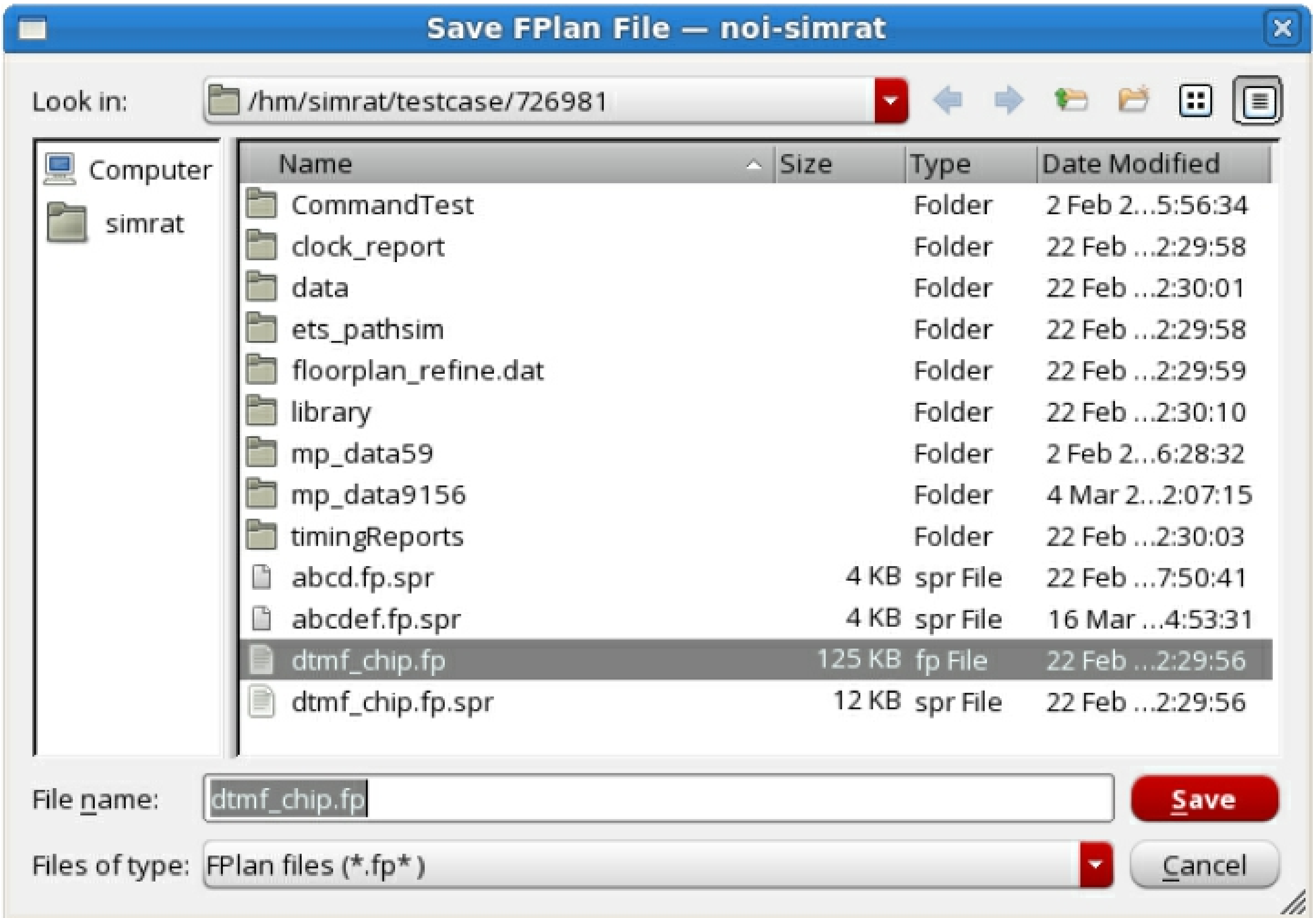
Related Text Commands

The following text command provides equivalent or additional functionality:

- savePartition

Save - Floorplan

Use the *Save FPlan File* form to save floorplan data at any time during a design session.
→ Choose *File - Save - Floorplan*.



Save FPlan File Fields and Options

Look in	Displays the name and contents of a directory where you can save your file. Click on the Look in pull-down to choose a different directory.
File name	Enter the name of the file to which you want to save the floor plan data.
Files of type	Specifies a file display filter. The default is `.fp`.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `saveFPlan`

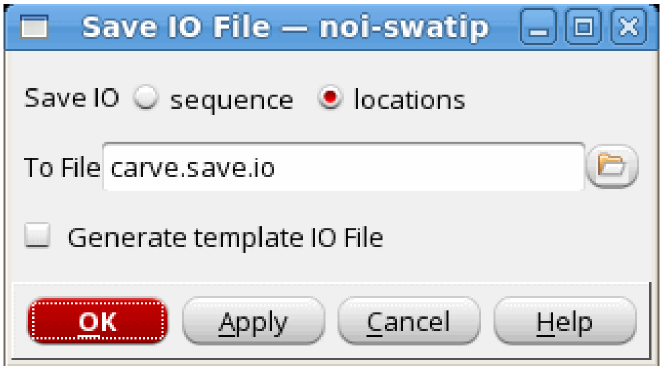
Save - IO File

Use the Save IO File form to save the design's I/O pad and pin information to a file. This file can be edited to customize the placement of pads and pins.

You can save the I/O information any time after floorplanning is complete. The results can be reloaded for future designs.

> By default, the I/O information is saved to a version: 3 file, for the current release version of Innovus. For the release versions 6.2 and below, you must save the I/O information to a version: 2 file, by specifying the *-v2* parameter in the `saveIoFile` command.

Note: This form can be used after loading I/O pad and pin placement data using DEF or TDF.
→ Choose *File* - *Save* - *I/O File*.



Save IO File Fields and Options

Save IO	Choose an I/O file type.
sequence	Creates a file that contains the pad and pin names in sequence for all sides of the die area. This file can be edited to customize I/O rule based commands and be read in during design import.
locations	Creates a file that contains the pad and pin names and their placement locations.
To File	Specify a name for the I/O file. The recommended filename extension is `.io`. The file format is ASCII.
Generate template IO File	Creates a template file with the extension `.io.tdf`

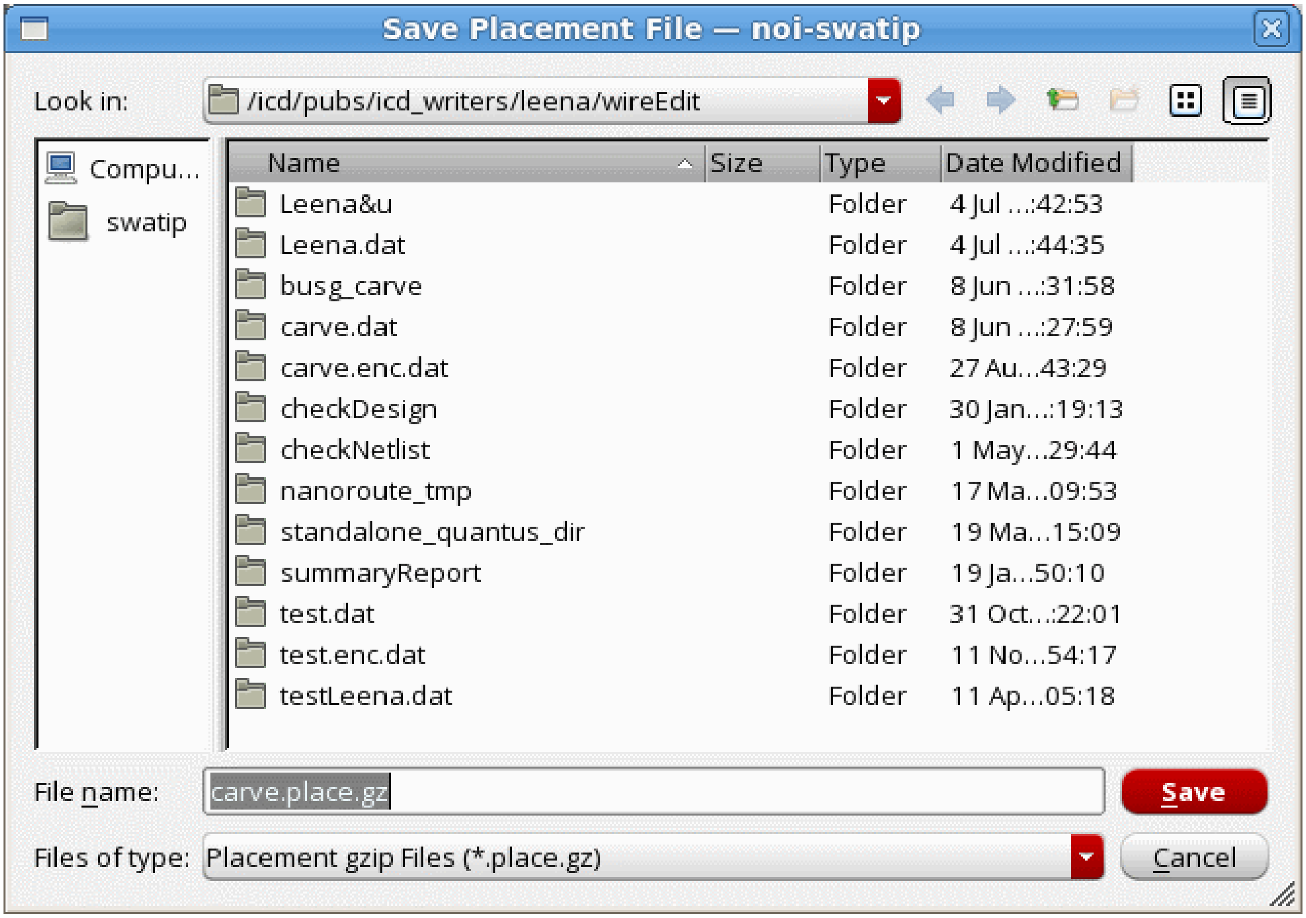
Related Text Commands

The following text command provides equivalent or additional functionality:

- `saveIoFile`

Save - Place

Use the Save Placement File form to write placement information to a file in Innovus placement data format. To save the placement data in DEF, PDEF, or TDF format, see Save".
→ Choose *File - Save - Place*.

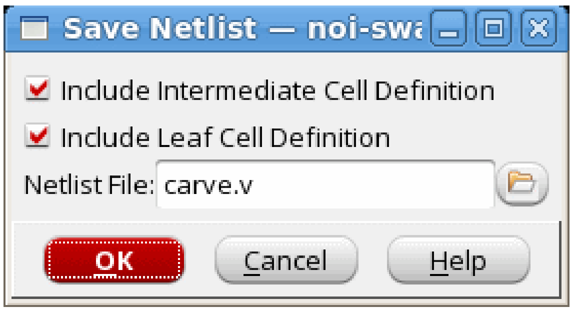


Save Placement File Fields and Options

Look in	Displays the name and contents of a directory where you can save your file. Click on the Look in pull-down to choose a different directory.
File name	Enter the name of the file to which you want to save the placement data.
Files of type	Specifies a file display filter. *Default:* `.place`

Save - Netlist

Use the Save Netlist form to write a netlist file of the design in Innovus. The netlist is in hierarchical Verilog format only if the original netlist loaded was hierarchical. The netlist is saved after running placement with timing driven option, clock tree synthesis, scan group reorder, or IPO. You must save the netlist if you performed timing-driven placement, scan optimization, clock tree synthesis (CTS), or in-place optimization (IPO) during the design session.
→ Choose *File - Save - Netlist.*



Save Netlist Fields and Options

Include Intermediate Cell Definition	Includes all the intermediate cell definitions in the netlist file. You must choose this to generate the design's complete netlist. Do not choose this option if you want to generate only leaf cell definitions.
Include Leaf Cell Definition	Includes all leaf cell definitions to the netlist file. Leaf cell definitions are needed when pin orders are implied in the netlist.
Netlist File	Specify a name for the netlist file.

Related Text Commands

For information on the following command, see "General Commands" in the *Innovus Text Command Reference*.

- `saveNetlist`

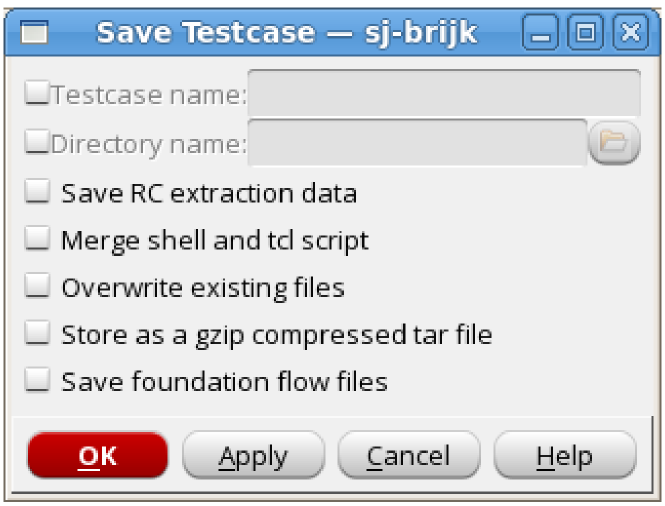
Save - Testcase

Use the Save Testcase form to save test case information to a file. Saves your design as a standalone testcase that includes both the design and the library files. All database references to files in the generated testcase are self-contained, such that the database can be loaded into Innovus on a different network.

You can use this command after loading a design.

Note: Exit Innovus after using the command. This is to avoid a possibility where saveDesign may create a configuration file with a timing constraints file pointing to the testcase directory. Given that the testcase directory is considered temporary, and may be gzipped or even deleted, a pointer to its data is not desirable. Exiting Innovus and re-loading a previously saved database will avoid this possibility.

Choose *File* - *Save* - *Testcase*.



Save Testcase Fields and Options

Testcase Name	The name of the testcase.
Directory Name	Name of the directory where you want to save the testcase.
Save RC Extraction Data	Chck if you want to save RC extraction data.
Merge shell and tcl script	Check to merge shell and tcl script.
Overwrite existing files	Check to overwrite existing files.
Store as a gzip compressed tar file	Check to store the testcase as a compressed tar file.
Save foundation flow files	Check to save foundation flow files

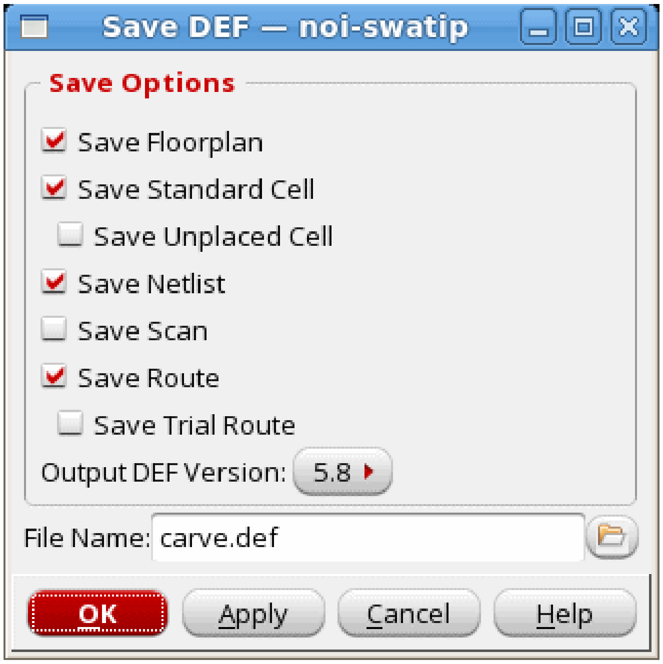
Related Text Commands

For information on the following command, see "General Commands" in the *Innovus System Text Command Reference*.

- `saveTestcase`

Save - DEF

Use the Save DEF form to save DEF information to a file. The DEF file can contain floorplan, placement, scan, or route data. Each data type is saved into a single DEF file.
→ Choose *File* - *Save* - *DEF*.


Save DEF — noi-swatip
Save Options
Save Floorplan
Save Standard Cell
Save Unplaced Cell
Save Netlist
Save Scan
Save Route
Save Trial Route
Output DEF Version: 5.8
File Name: carve.def
OK
Apply
Cancel
Help

Save DEF Fields and Options

Save Floorplan	Saves DEF rows, tracks, die area, gcell grids, corebox, block placement, special nets, and I/Os.
Save Standard Cell	Saves standard cell placements.
Save Unplaced Cell	Saves unplaced standard cell information. This option is available only if *Save Standard Cell* is selected.
Save Netlist	Saves netlist connectivity information.
Save Scan	Saves scan cell information.
Save Route	Saves `NET`s wiring. Trial routes are ignored unless Trial Route is selected.
Save Trial Route	Saves trial route data.
Output DEF Version	Specifies the DEF file version. The available options are 5.8, 5.7, and 5.6. The default value is `5.8`.
File Name	Specify a name for the DEF file.

Note: Fields are available based on the status of the design. For example, if the design is placed, the *Save Route* field is unavailable.

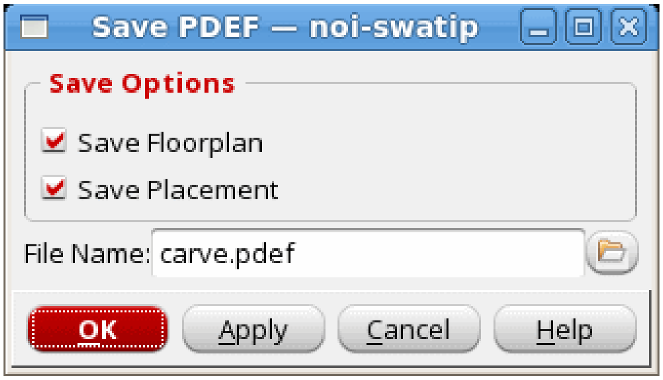
Related Text Commands

For information on the following command, see "Import Commands" in the *Innovus Text Command Reference*.

- `defOut`

Save - PDEF

Use the Save PDEF form to save floorplan information to a file.
→ Choose *File* - *Save* - *PDEF*.

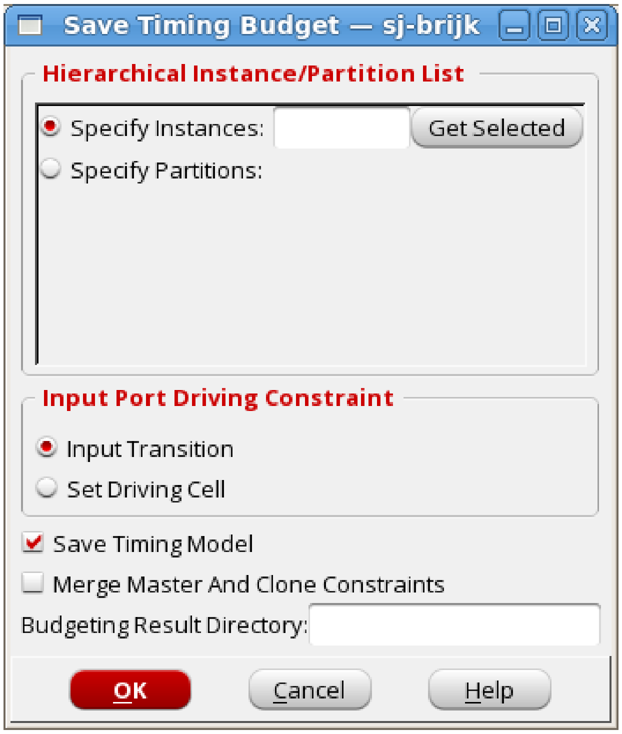


Save PDEF Fields and Options

Save Floorplan	Specifies that only floorplan information be written into the output PDEF file. If you do not specify this option, both floorplanning and placement information appear in the output PDEF file.
Save Placement	Saves placement information to the output PDEF file.
File Name	Specify a name for the PDEF file.

Save - Timing Budget

Use the Save Timing Budget form to save time budget files of specified hierarchical instances to a specified directory.
→ Choose *File* - *Save* - *Timing Budget*.


Save Timing Budget — sj-brijk
Hierarchical Instance/Partition List
Specify Instances:
Get Selected
Specify Partitions:
Input Port Driving Constraint
Input Transition
Set Driving Cell
Save Timing Model
Merge Master And Clone Constraints
Budgeting Result Directory:
OK
Cancel
Help

Save Timing Budget Fields and Options

Specify Instances	Saves the budget files for instances.
Specify Partitions	Saves the budget files for partitions.
Input Transition	Writes out input transition time in the budgeting output files using the `set_input_transition` constraint.
Set Driving Cell	Writes out the boundary drive information using the `set_driving_cell` constraint.
Save Timing Model	Saves the timing model.
Merge Master and Clone Constraints	Saves the timing budgets for the masters/clones based on the worst-case timing data per pin. When used with the *Specify Instances*, this option saves the budget based on the worst-case data for the specified instances in the master/clone set. When used with *Specify Partitions*, this option saves the budget based on the worst-case data for all the partitions in the master/clone set.
Budgeting Result Directory	Specifies the directory name that contains the derived timing budget files. The files are derived in a subdirectory *`dirName`*`/`*`cellTypeName`*`/`*`cellTypeName`*`.constr.pt`. If you do not specify this option, the timing budget files are derived in the current directory.

Related Text Commands

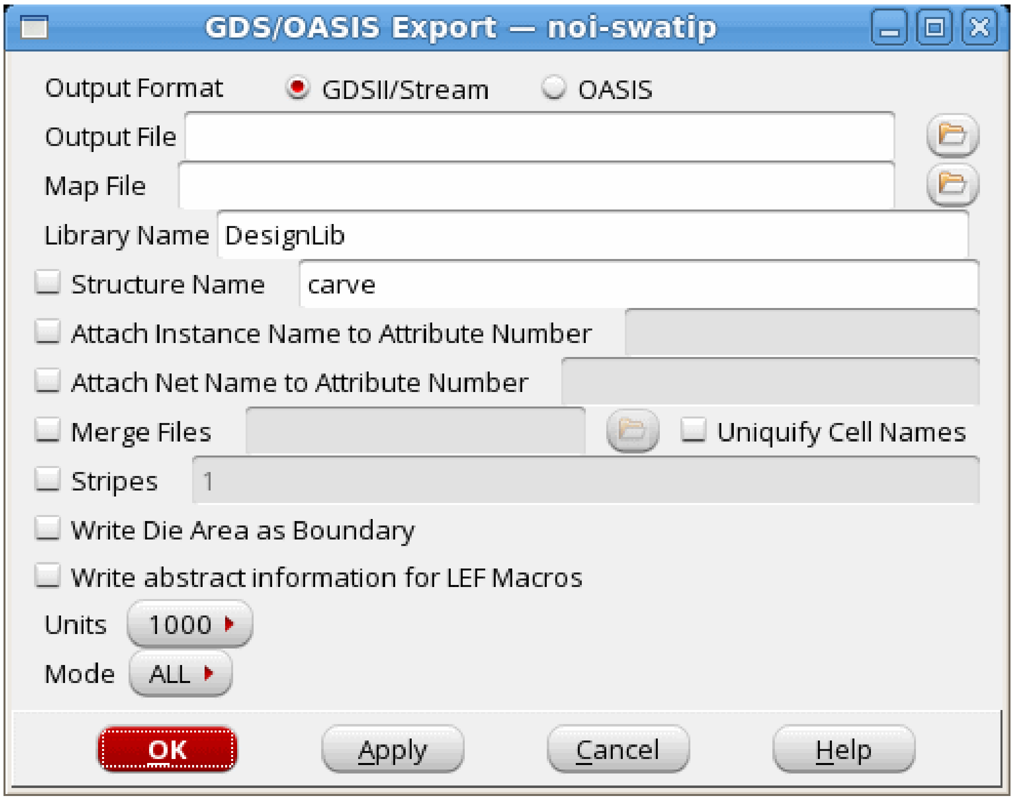
For information on the following command, see "Timing Budgeting Commands" in the *Text Command Reference* document.

`saveTimingBudget`

Save - GDS/OASIS

Use the GDS/OASIS Export form to create a GDSII/Stream or OASIS file version of the current database.

→ Choose *File - Save - GDS/OASIS*.



GDS/OASIS Export Fields and Options

Output Format	Specifies the file format in which to save the database. *Default*: GDSII/Stream	
	GDSII/Stream	Saves the database as a GDSII Stream file.
	OASIS	Saves the database as an OASIS file.
Output File	Specifies the GDSII Stream output file. Use the file folder icon to find the directory and file you want. **Note:** Add the `.gz` extension to the filename to enable compression (for example, `GDS_file.gds.gz`).	

Map File	Specifies the file used for layer mapping between the Innovus software and GDSII Stream format. Use the file folder icon to find the file you want. If a file is not specified, the software creates a map file with the name `streamOut.map`. For more information, see the "About the GDSII Stream or OASIS Map File" section in the Importing and Exporting Designs chapter of the *Innovus User Guide*.
Library Name	Specifies the library that you want to create in GDSII /Stream format. The default name is `DesignLib`.
Structure Name	Specifies the structure name that contains all geometries and instances. The default is the current design's top cell name.
Attach Instance Name to Attribute Number	
	Specifies the instance name value added to the attribute on SREF of the specified attribute number.
Attach Net Name to Attribute Number	
	Specifies the attribute number for paths and via SREF. The Innovus software adds the net name values to this attribute.
Merge Files	Specifies a single file or list of files to merge with the database. All files must be Stream GDSII files. Compressed files are acceptable. If a merge file contains extra cells that are not used in the design, the Innovus software merges only the cells used in the design. The software automatically creates blackboxes when merging and writing macro files.

Uniquify Cell Names	Creates unique cell names if there are name collisions when the Innovus software merges files. When a cell name is repeated, the software renames the cell *`cellName_filename`*, where *`filename`* is the name of the merge file in which the cell name appears. The Innovus software changes the name of references to that cell in the merge file. The software changes the reference name if the referenced cell is defined in the same file, regardless of whether the cell is defined before or after the reference. If a reference in a merge file refers to a cell definition in a different merge file, then the reference is not changed in the OASIS output file. **Note:** You must select *Merge Stream Files* to enable this option. *Default:* Off (The Innovus software ignores duplicate cell names.)
Stripes	Specifies the number of stripes that divide the design. For example, setting *Stripes* to `2` divides the design into two equal windows and creates three files. Setting *Stripes* to `3` divides the design into three equal windows and creates four files. The default is `1`. **Note:** All polygons and shapes whose lower-left corner is in the current window are output with that stripe. If the *Stripes* value is greater than `1`, the naming conventions are as follows: • `GDS_file.gds` Contains top structure, SREFs for top structures of other stripes, and via definitions • `GDS_file.gds.1` Contains stripe number 1, `structureName.1` • `GDS_file.gds.2` Contains stripe number 2, `structureName.2`
Write Die Area as Boundary	
	Forces the Innovus software to output die areas as boundaries. If not specified, the software outputs die areas as bounding boxes.
Write abstract information for LEF Macros	

	Outputs LEF abstract information, such as LEF pin geometries and obstructions for macros. Optionally, you can select *Write abstract information for LEF Macros* when you want to create a GDSII Stream output that contains the LEF macro structures as well as the design data. This option can be used for debugging the LEF macro definitions against verification DRC rules. The output contains macro pins and obstructions. **Note:** `LEFPIN` and `LEFOBS` apply only when *Write abstract information for LEF Macros* is enabled. Additionally, if you select *Write abstract information for LEF Macros* and `LEFPIN` and `LEFOBS` are not specified in the map file for the layers in the LEF `MACRO`s, the GDSII structures for those `MACRO`s will be empty.	
Units	Selects the resolution for values in the GDSII Stream file. Choose one of the values provided in the cyclic field. The default unit value is the value that is specified in the LEF technology file.	
Mode	Identifies the layers to write.	
	ALL	Specifies all layer information in the map file: • All instances • All via instances • All generated via cells
	FILLONLY	Specifies only fill layers in the map file: • No instances • Only fill via instances • Only generated fill via cells
	NOFILL	Specifies only non-fill layers in the map file: • All instances • Only non-fill via instances • Only non-fill generated via cell
	NOINSTANCES	Writes wiring (including vias) only; does not write out COMPONENT instances.

Related Text Commands

For information on the following command, see "Import Commands" in the *Innovus Text Command Reference*.

- `streamOut`

Related Topics

For information on the following topics, see "Importing and Exporting Designs" in the *Innovus User Guide*.

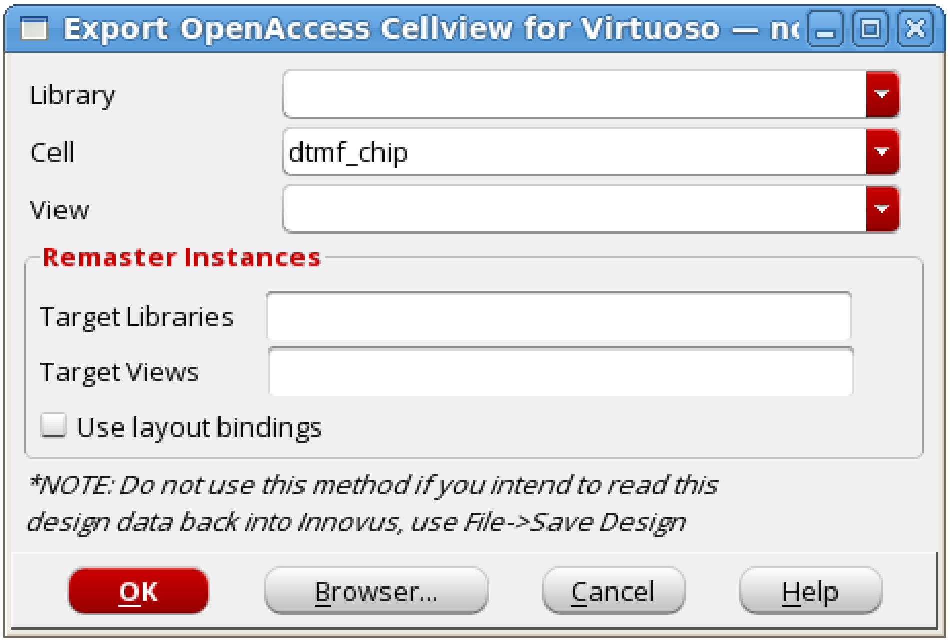
- Merging GDSII Files
- GDS Map File Format

Save - OA Cellview

Use the Export OpenAccess Cellview for Virtuoso form to save floorplan, placement, and routing data in the OpenAccess format. To access this form:

- Choose *File - Save - OA Cellview*.

Use the Export OpenAccess Cellview for Virtuoso form only if you intend to to take the OpenAccess implementation of the block to Virtuoso. If you need to read the design data in Innovus, use *File - Save Design* instead.



Export OpenAccess Cellview for Virtuoso Fields and Options

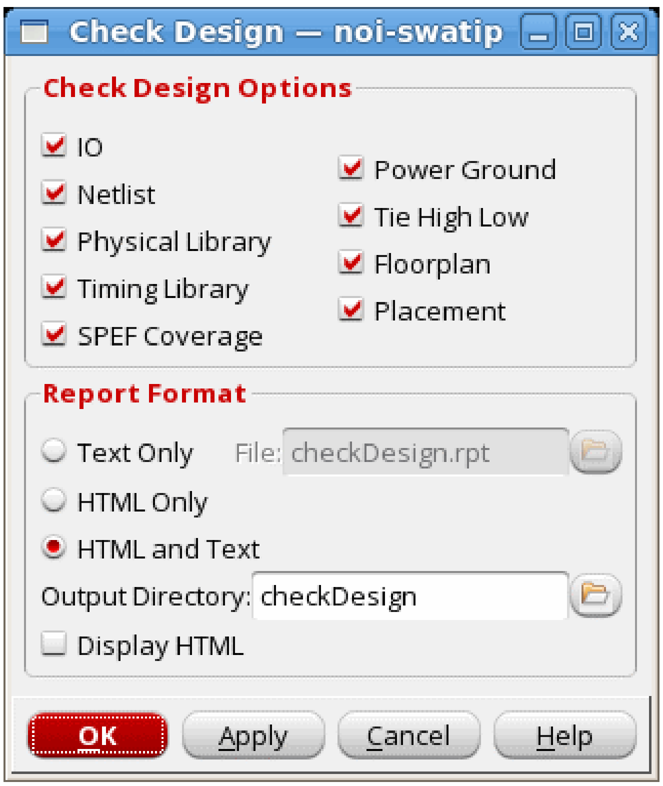
Library	Specifies the target OpenAccess library name.
Cell	Specifies the target cell name.
View	Specifies the target view name.
Target Libraries	Specifies the names of the external libraries that will contain the leaf cell masters, LEF abstract, and technology file. This field accepts only library names, not paths. The mapping between the external library name and its path is defined in the cds.lib file. Innovus references technology information only from the first library in the list of libraries.
Target Views	Specifies a list of view names to be searched during leaf cell instance binding.
Use layout bindings	Overrides the reference libraries and leaf-view-name-specified binding, and utilizes the cell layout viewing binding stored on the library cell master for each leaf cell (stored in the library cell's layout library and layout view attributes).

Check Design

Use the Check Design form to check for missing or inconsistent library and design data at any stage of the design. Cadence recommends that you check libraries and data as follows:

- Perform I/O checking at any time. I/O problems might not impede any tool, but they might add to design problems.
- Perform netlist checking at any time after the design has been loaded.
- Perform physical library checking before floorplanning.
- Perform power/ground checking before routing and extraction, and verifying geometry and connectivity.
- Perform timing library checking before any timing-related operation (for example, timing driven placement or routing, timing optimization, clock-tree synthesis, and static timing analysis)
- Perform tie-high and tie-low checking before routing and extraction.

→ Choose *File - Check Design*.



Check Design Fields and Options

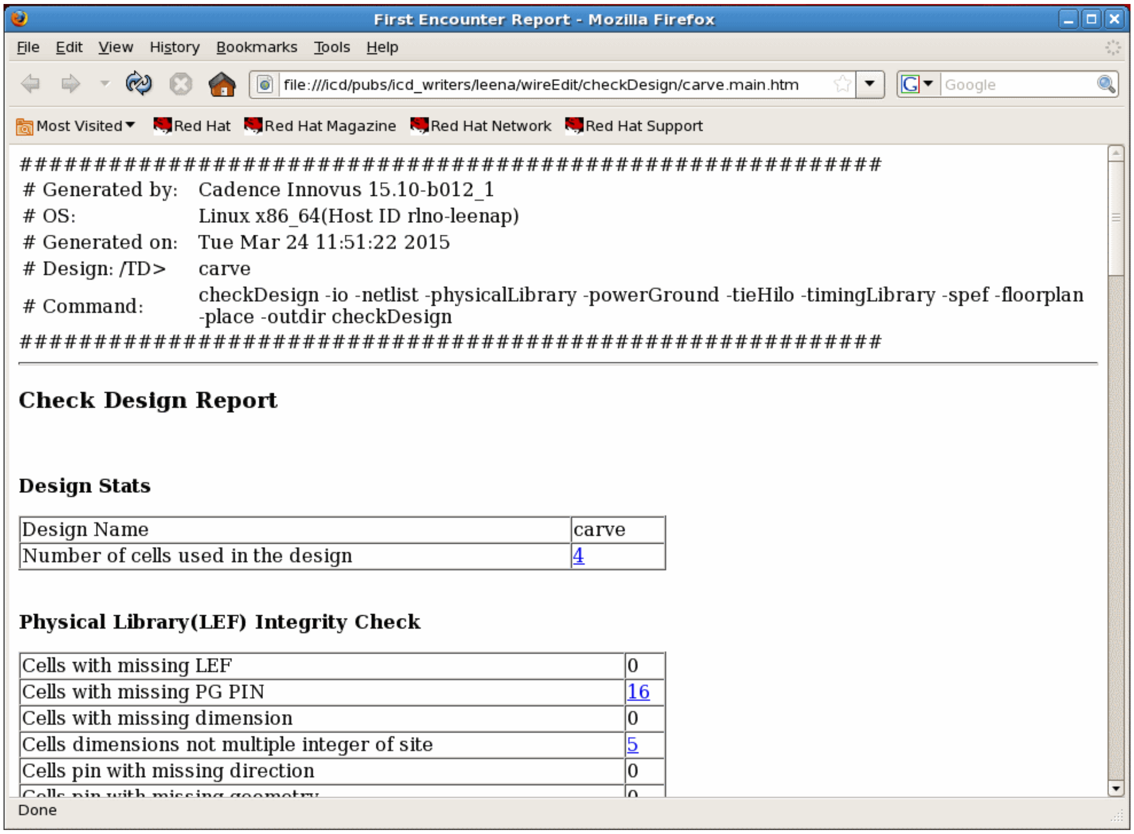
IO	Checks I/O pads, issues warning messages, and reports the following information: • Unplaced I/O cells • Floating pins that belongs to I/O pads (warning) • I/O pins connected to non-I/O instances (directly connected to core cells) • Unplaced I/O pins • Floating I/O pins *Default:* On
Netlist	Checks the netlist, issues error or warning messages, and reports the following information: • Output pins tied to power/ground nets (for example, `BUFX1 U1 (.A(net1),.Y1(1'b0))`) • Input pins floating (warning) • Multiple driver nets (warning) *Default:* On
Physical Library	Checks the physical libraries and reports whether all cells have LEF views. Issues error messages for the following conditions: • Cells not defined in LEF • Cells with missing dimensions • Pins with missing direction • Cells and pins with missing geometry • Cell dimensions are not an integer multiple of the core site dimensions *Default:* On
Timing Library	Checks whether the cells used in the design have been defined in the timing library. This option does not check for the presence of timing arcs. All physical cells are excluded from this check. *Default:* On

Floorplan	Checks the floorplan, issues error or warning messages, and reports the following information: • Off-grid horizontal and vertical tracks • Instances not snapped to row site • Unplaced I/O pins • Off Grid Power/Ground Pre-routes • Instances not on the manufacturing grid • Preroutes not on the manufacturing grid (error) • Regular preroutes not on tracks *Default:* On
Power Ground	Checks power and ground connections, issues warning messages, and reports the following information: • Power terminals connected to ground net • Ground terminals connected to power net • Floating power and ground terminals • Power and ground terminals connected to non-power and ground nets. *Default:* On
Tie High Low	Reports unconnected tie-high or tie-low terminals, and issues a warning message. *Default:* On
Placement	Checks placement, issues error or warning messages, and reports the following information: • Number of placed and unplaced instances • Number of overlapping instances • Number of placement blockage violations • Placement density *Default:* On

SPEF Coverage	Reports the following SPEF information: • SPEF coverage • Number of nets in the design that are not in SPEF • List of nets
Text Only	Generates a text version of the report. *Default:* Off
File	Writes the report information to the specified file. *Default:* `checkDesign.rpt`
HTML Only	Generates an HTML version of the report. Some sections of the report include links to more detailed HTML reports. For an example of an HTML report, see HTML Check Design Report. *Default:* Off
HTML and Text	Generates both an HTML version and a text version of the report. *Default:* On
Output Directory	Saves the HTML version of the report to the specified directory. If you select the *HTML and Text* option, the software saves both the HTML and text versions of the report to the specified directory. *Default:* `checkDesign`
Display HTML	Opens a browser and displays the HTML version of the report. *Default:* Off

HTML Check Design Report

The following is an example of an HTML report generated by the Check Design form.



##

# Generated by:	Cadence Innovus 15.10-b012_1
# OS:	Linux x86_64(Host ID rlno-leenap)
# Generated on:	Tue Mar 24 11:51:22 2015
# Design: /TD>	carve
# Command:	checkDesign -io -netlist -physicalLibrary -powerGround -tieHilo -timingLibrary -spef -floorplan -place -outdir checkDesign

##

Check Design Report

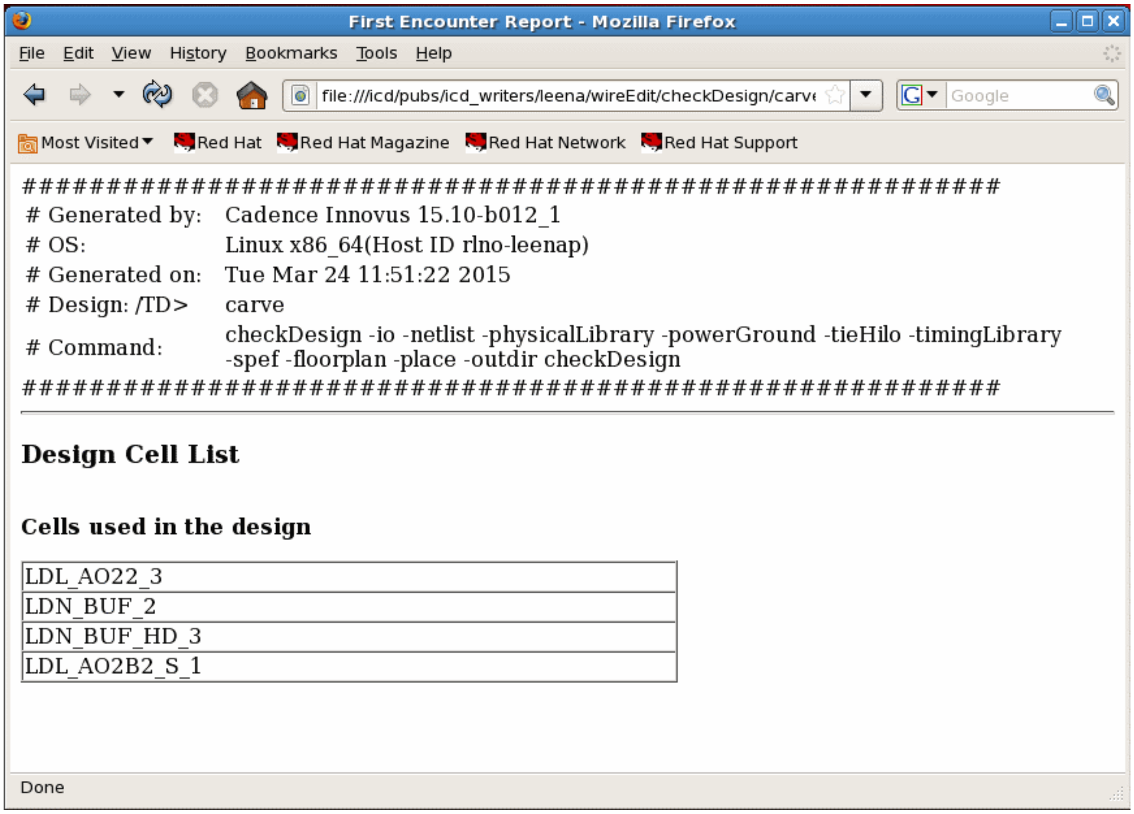
Design Stats

Design Name	carve
Number of cells used in the design	4

Physical Library(LEF) Integrity Check

Cells with missing LEF	0
Cells with missing PG PIN	16
Cells with missing dimension	0
Cells dimensions not multiple integer of site	5
Cells pin with missing direction	0
Cells pin with missing geometry	0

Some sections of the report include links to more detailed HTML reports. For example, if you click on the *Design Stats* link on the main page of the HTML report, the software displays a list of the cells used in the design.



Related Text Commands

For information on the following command, see "Import and Export Commands" in the *Innovus Text Command Reference*.

- `checkDesign`

Report

The Report menu provides access to the following forms that allow you to generate reports that contain statistics for the entire design, calculate the gate count, and create a list of design statistics:

- Summary Report
- Selected Object
- Gate Count Report
- Netlist Statistics

Summary Report

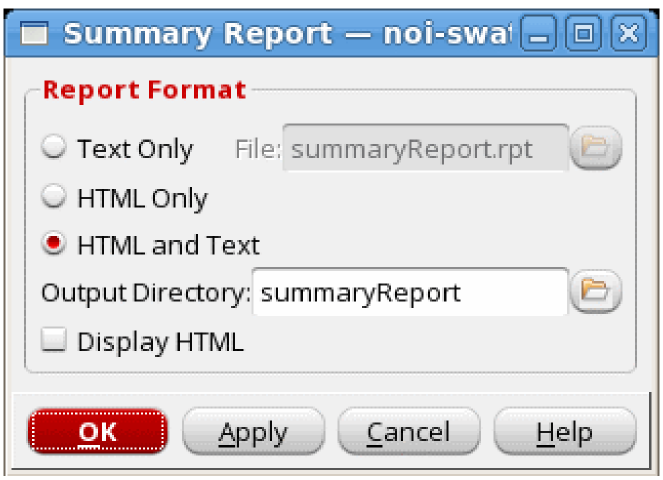
Use the Summary Report form to create a report that contains statistics for the entire design, or a selected object in the design.

A report on the entire design includes statistics for the following categories:

- General Design Information
- General Library Information
- Netlist Information
- Timing Information
- Floorplan/Placement Information

The information contained in a report on a selected object varies depending on the object you select. You can select a module, an instance, or a net.

1. Select an object in the design display area. (If you want to display information about the entire design, skip Step 1.)
2. Choose *File - Report - Summary* or click the *Summary Report* widget on the toolbar.

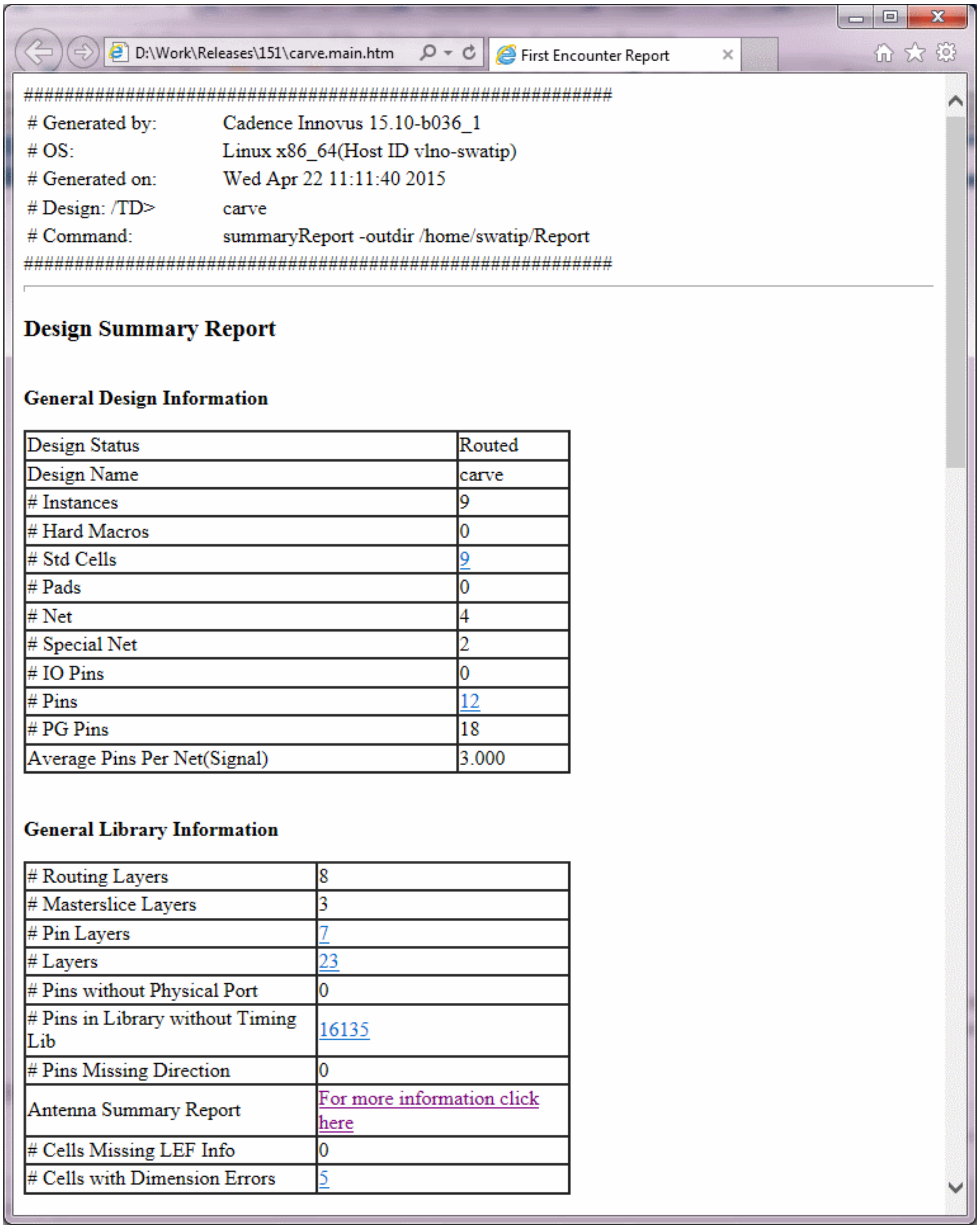


Summary Report Fields and Options

Text Only	Generates a text version of the summary report. *Default:* Off	
	File	Writes the report information to the specified file. *Default:* `summaryReport.rpt`
HTML Only	Generates an HTML version of the summary report. Some statistics in the sections include links to more detailed HTML reports. For example, if you click on the *# Layers* link under *General Library Information* section of the HTML report, the software displays a detailed HTML report on the layers in the design. For an example of an HTML report, see HTML Summary Report *Default:* Off	
HTML and Text	Generates both a text version and an HTML version of the summary report. *Default:* On	
Output Directory	Saves the HTML version of the report to the specified directory. If you select the *HTML and Text* option, the software saves both the HTML and text versions of the report to the specified directory. *Default:* `summaryReport`	
Display HTML	Opens a browser and displays the HTML version of the report. *Default:* Off	

HTML Summary Report

The following is an example of an HTML summary report for an entire design.



D:\Work\Releases\151\carve.main.htm

First Encounter Report

###

# Generated by:	Cadence Innovus 15.10-b036_1
# OS:	Linux x86_64(Host ID vlno-swatip)
# Generated on:	Wed Apr 22 11:11:40 2015
# Design: /TD>	carve
# Command:	summaryReport -outdir /home/swatip/Report

###

Design Summary Report

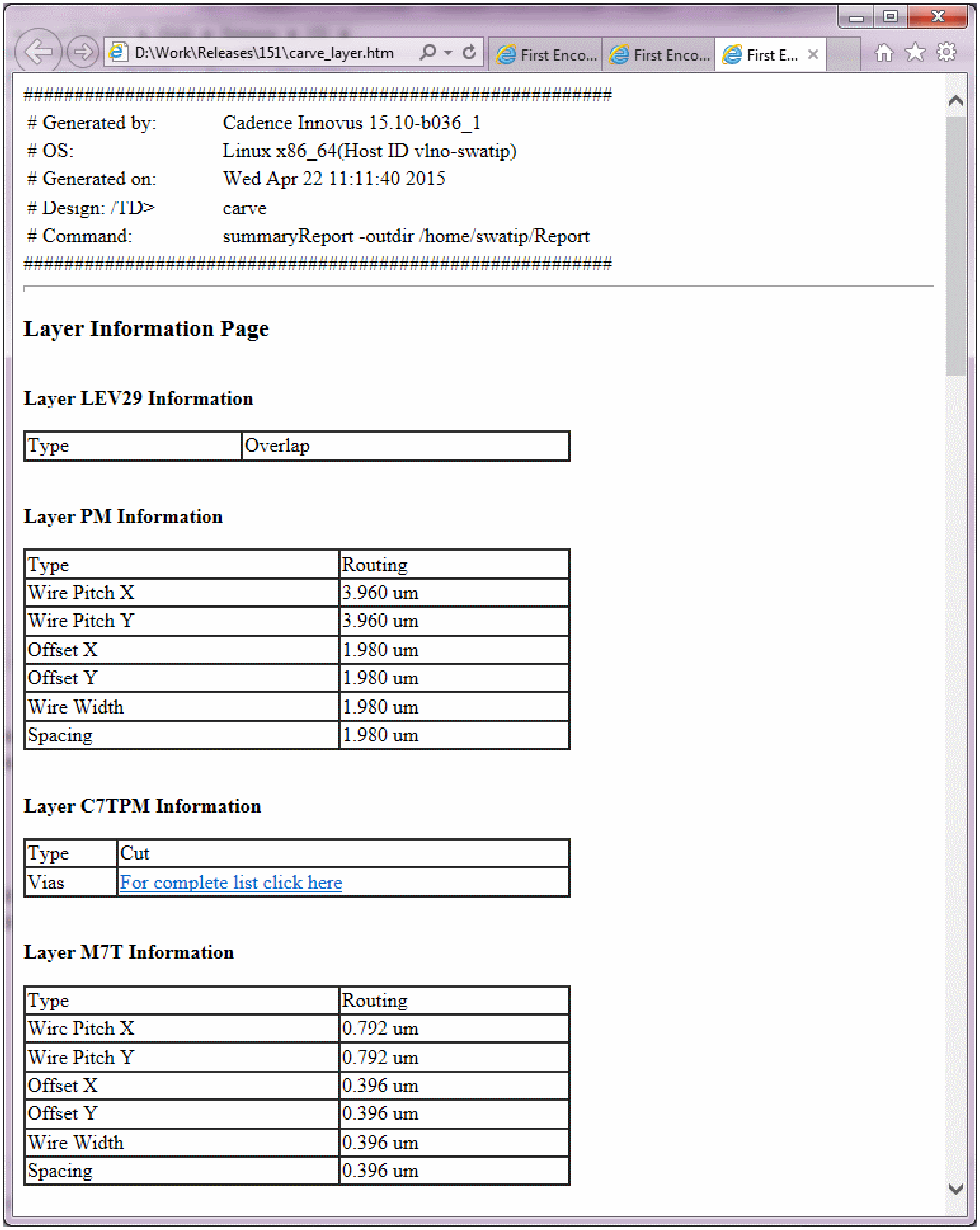
General Design Information

Design Status	Routed
Design Name	carve
# Instances	9
# Hard Macros	0
# Std Cells	9
# Pads	0
# Net	4
# Special Net	2
# IO Pins	0
# Pins	12
# PG Pins	18
Average Pins Per Net(Signal)	3.000

General Library Information

# Routing Layers	8
# Masterslice Layers	3
# Pin Layers	7
# Layers	23
# Pins without Physical Port	0
# Pins in Library without Timing Lib	16135
# Pins Missing Direction	0
Antenna Summary Report	For more information click here
# Cells Missing LEF Info	0
# Cells with Dimension Errors	5

Some statistics in the sections include links to more detailed HTML reports. For example, if you click on the *# Layers* link under the *General Library Information* section of the HTML report, the software displays a detailed HTML report on the layers in the design.



###

# Generated by:	Cadence Innovus 15.10-b036_1
# OS:	Linux x86_64(Host ID vlno-swatip)
# Generated on:	Wed Apr 22 11:11:40 2015
# Design: /TD>	carve
# Command:	summaryReport -outdir /home/swatip/Report

###

Layer Information Page

Layer LEV29 Information

Type	Overlap

Layer PM Information

Type	Routing
Wire Pitch X	3.960 um
Wire Pitch Y	3.960 um
Offset X	1.980 um
Offset Y	1.980 um
Wire Width	1.980 um
Spacing	1.980 um

Layer C7TPM Information

Type	Cut
Vias	For complete list click here

Layer M7T Information

Type	Routing
Wire Pitch X	0.792 um
Wire Pitch Y	0.792 um
Offset X	0.396 um
Offset Y	0.396 um
Wire Width	0.396 um
Spacing	0.396 um

Related Text Commands

For information on the following command, see "General Commands" in the *Innovus Text Command Reference*.

- summaryReport

Selected Object

Use the File - Report - Selected Object menu item to report the properties of selected objects in the main console window.

To view the properties, select the object(s) in the design display area and:

- Choose *File - Report - Selected Object*.

or

- Click the Report Select Obj  tool widget.

The properties are displayed in the main console window.

Related Text Command

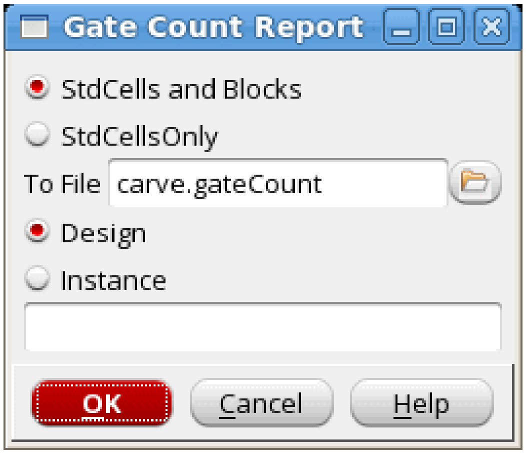
The following text command provides equivalent or additional functionality:

- reportSelect

For more information, see "Floorplan Commands" in the *Innovus Text Command Reference.*

Gate Count Report

Use the Gate Count Report form to calculate the gate count based upon standard cells and blocks, or standard cells only. You can calculate gate counts for the entire design or for a specific instance.
→ Choose *File - Report - Gate Count*.



Gate Count Report Fields and Options

Std Cells and Blocks	Sets the gate count calculation for standard cells and blocks.
Std Cells Only	Sets the gate count calculation for standard cells only.
To File	Specifies the filename to which to output the report. The default file extension is `.gateCount`. Use this file extension so the report will display in the Innovus console.
Design	Calculates gate counts for the entire design.
Instance	Calculates gate counts for a specified instance. If you select this option, you must specify an instance name in the text field.

Related Text Commands

For information on the following command, see "General Commands" in the *Innovus Text Command Reference*.

- `reportGateCount`

Netlist Statistics

Use the *Netlist Statistics* menu command to create a list of design statistics, such as number of cells, nets, pins, and instances. A summary of the netlist is printed to the Innovus console and a log file and saved in the run directory.
→ To print a list of design statistics, choose *File - Report - Netlist Statistics*.

Exit

Use the *Exit* menu command to end an Innovus session.

No ECO Place

3

View Menu

- Zoom
  - In
  - Out
  - Selected
  - Previous
  - Next
- Pan
  - Up
  - Down
  - Left
  - Right
- Fit
- Redraw
- Set Preference
  - Preferences - Design
  - Preferences - Display
  - Preferences - Edit
  - Preferences - Floorplan
  - Preferences - Selection
  - Preferences - Windows
  - Preferences - Flightline
  - Preferences - Text

    - Save Preference
    - Load Preference File
- All Colors
- Set Flightline Congest Color
- Go To
- Find/Select Object
    - Mode Settings
- Deselect All
- Highlight Selected
- Clear Highlight
- Edit Highlight Color
- Dim Background

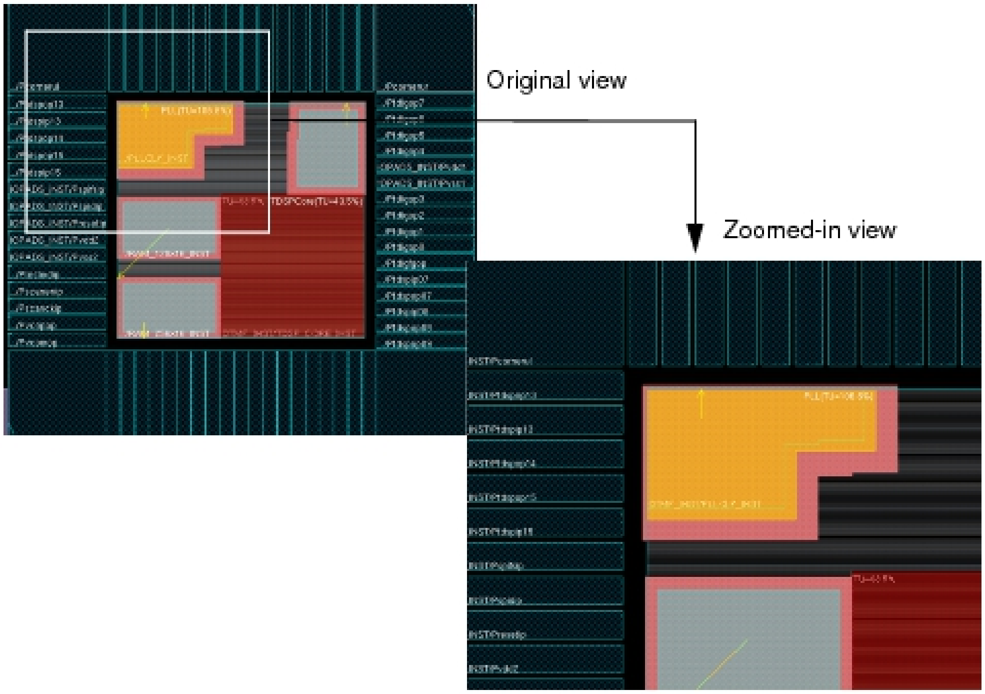
Zoom

The *View -> Zoom* submenu comprises the following items: *In*, *Out*, *Selected*, *Previous*, and *Next*.

In

Use the *Zoom - In* menu command to zoom into a portion of the design and view it in greater detail. Each click zooms in two levels. The equivalent bindkey is `z`.

You can also use the scroll wheel of your mouse to zoom into a portion of the design. Each forward scroll of the scroll wheel zooms in one level.



Related Text Command

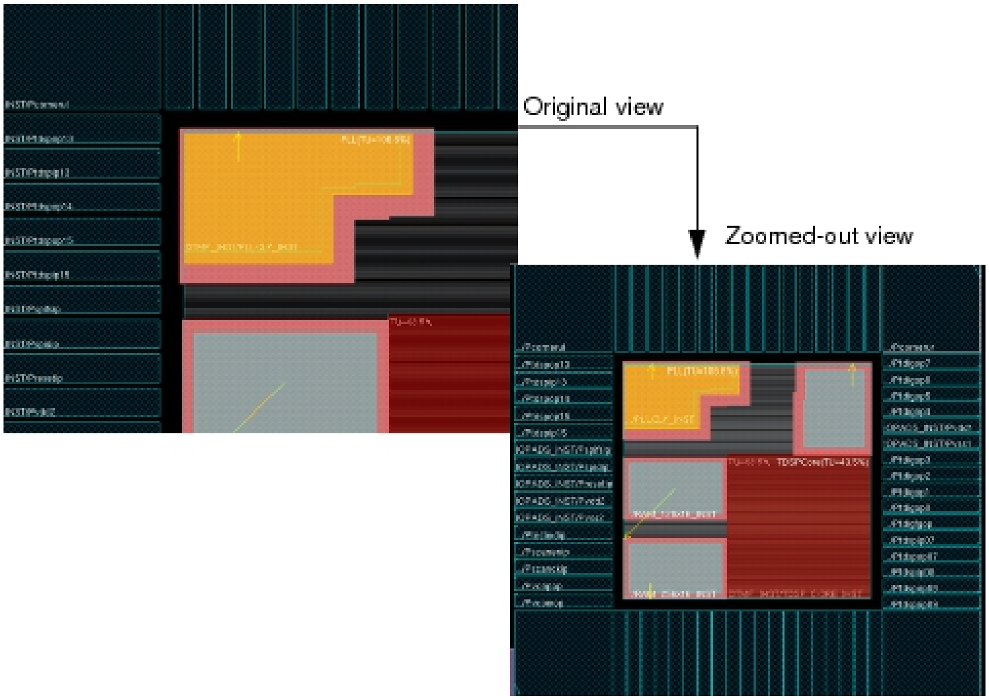
The following text command provides equivalent or additional functionality:

- `zoomIn`

Out

Use the *Zoom - Out* menu command to display a larger area of the design in less detail. Each click zooms out two levels. The equivalent bindkey is `Shift+Z`.

You can also use the scroll wheel of your mouse to zoom out of a detailed view of the design. Each backward scroll of the scroll wheel zooms in one level.



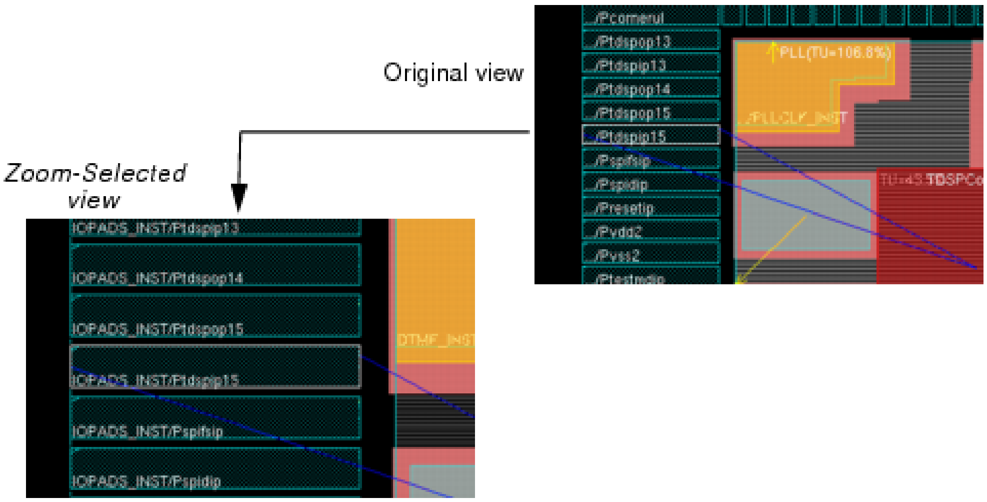
Related Text Command

The following text command provides equivalent or additional functionality:

- `zoomOut`

Selected

Select a design object and then use the *Zoom - Selected* menu command to zoom into the area that contains the selected object.



Related Text Command

The following text command provides equivalent or additional functionality:

- `zoomSelected`

Previous

Use the *Zoom - Previous* menu command to toggle the display between the previous location/zoom level and the current location/zoom level. The equivalent bindkey is `W`.

Next

Use the *Zoom - Next* menu command to to display the next view window, which could be the next location in the *Go To Saved Area* list of the *Previous* widget or the next zoom level of the zoom sequence saved in the design memory. This command provides the same function as the *Next* widget () on the toolbar. The equivalent bindkey is `Y`. When you press the `Y` bindkey repeatedly, the tool cycles through all saved views (saved areas and zoom levels).

If you want the *Next* command to cycle through only the saved areas and disregard zoom levels, select the new *Only Save User Specified View* check box on the *Display* page of the Preferences form.

Pan

The *View -> Pan* submenu comprises the following items: *Up*, *Down*, *Left*, and *Right*.

Up

Pans up the viewable window in pages. The size of each page is equal to the size of the current viewable window. The equivalent bindkey is the Up arrow key.

You can also use the scroll wheel of your mouse to pan up the viewable window. Press `Shift` and move the scroll wheel forward to pan upwards.

Down

Pans down the viewable window in pages. The size of each page is equal to the size of the current viewable window. The equivalent bindkey is the Down arrow key.

You can also use the scroll wheel of your mouse to pan down the viewable window. Press `Shift` and move the scroll wheel backward to pan downwards.

Left

Pans the viewable window to the left in pages. The size of each page is equal to the size of the current viewable window. The equivalent bindkey is the Left arrow key.

You can also use the scroll wheel of your mouse to pan the viewable window to the left. Press `Ctrl` and move the scroll wheel forward to pan to the left.

Right

Pans the viewable window to the right in pages. The size of each page is equal to the size of the current viewable window. The equivalent bindkey is the Right arrow key.

You can also use the scroll wheel of your mouse to pan the viewable window to the right. Press `Ctrl` and move the scroll wheel backward to pan to the right.

Fit

Use the *Fit* menu command to fit the entire design within the design display area. The equivalent bindkey is `F`.

Related Text Command

The following text command provides equivalent or additional functionality:

- `fit`

Redraw

Use the *Redraw* menu command to refresh the display in the viewable window. The equivalent keyboard shortcut is `Ctrl+R`.

Related Text Command

The following text command provides equivalent or additional functionality:

- `redraw`

Set Preference

Use the *Set Preference* command in the *View* menu to access the Preferences form. This form allows you to set the design settings for the Innovus Implementation System (Innovus) session.

You can save custom preference settings to a file (see Save Preference), load a previously saved file (see Load Preference File), or load default settings. The default settings are saved in the enc.pref.tcl file; custom settings can be saved with a different filename.

The Preferences form also allows you to create, edit, apply, and save design keyboard shortcut commands (see Binding Key).

The Preferences form contains the following pages:

- Preferences - Design
- Preferences - Display

- Preferences - Edit
- Preferences - Floorplan
- Preferences - Selection
- Preferences - Windows
- Preferences - Flightline
- Preferences - Text

Preferences - Design

Use the *Design* page of the Preferences form to set hierarchy levels in the netlist and DEF files, specify bus delimiters for PDEF files, denote output of command logs, and create binding key shortcuts. The default settings are saved in the enc.pref.tcl file; custom settings can be saved with a different filename.

- Choose *View - Set Preference* and click on the *Design* tab.

Preferences - Design Fields and Options

Design Name	Specifies the name of the design for which to set the preferences.
Design Hierarchical Character	
	Denotes the character being used as the hierarchy delimiter in a netlist. If the netlist uses another character, enter it in the text box and import the design. *Default:* /

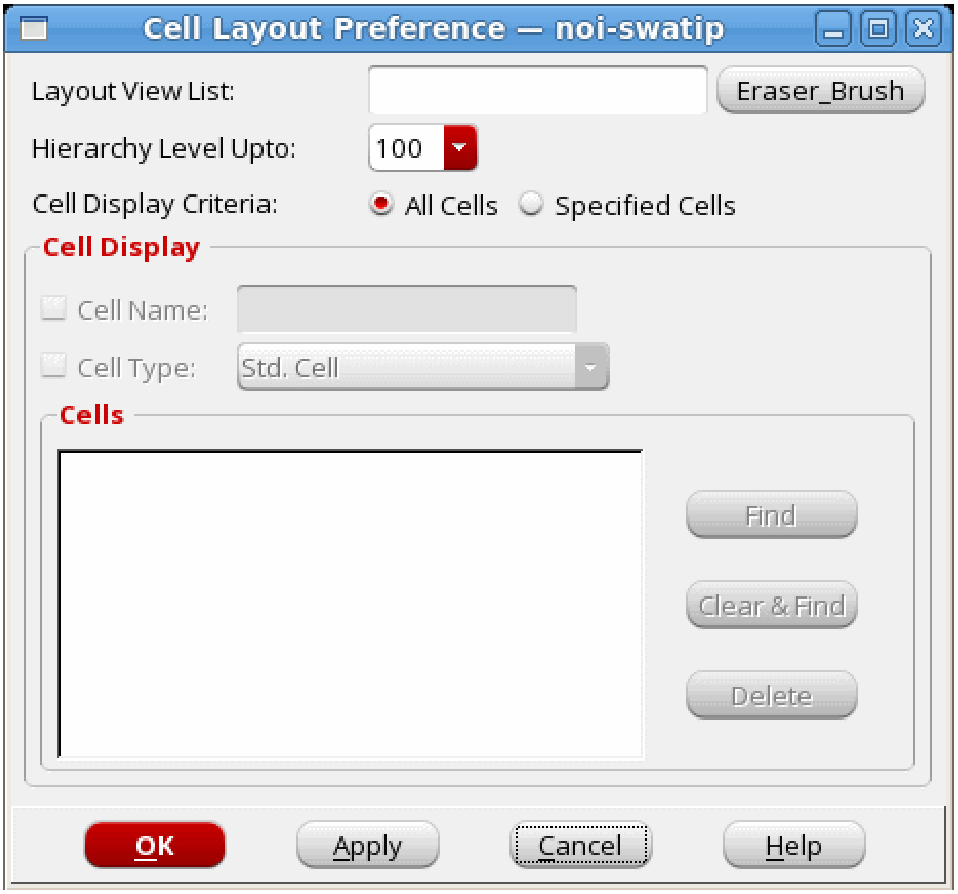
DEF Hierarchical Character	Denotes the character being used as the hierarchy delimiter in a DEF file. If the DEF file uses another character, enter it in the text box and load the DEF file. When writing a DEF file, the software uses the same character. *Default:* /	
PDEF Bus Delimiter	Denotes the character being used as the hierarchy delimiter in a PDEF file. If the PDEF file uses another character, enter it in the text box and load the PDEF file. When writing a PDEF file, the software uses the same character. *Default:* []	
Write Conformal/LEC dofile When Design is Saved		
	When saving a netlist, this option saves a dofile (a set of commands contained in a specified file) for the Conformal® Equivalence Checking capabilities. *Default:* Off	
Command Log Mode	Specifies where the command log is written. *Default: Command and Log*	
	Command Only	Writes to the command file only.
	Command and Log	Writes to the command file and log files.
	Command, Log, and Screen	Writes to the command file, log files, and screen.
	Note: When writing to log file and screen, the commands are preceded with <CMD>.	
Log Type-In Command	Logs whatever is manually entered (typed), to the command file. In the case of source commands, only the source command is logged, and not the commands in the sourced file. *Default:* Off	
Invoke viewLog at Start Up		
	Displays log viewer at startup. If you select this check box and click Save in the Preferences form, setPreference logviewer 1 is written to the user specified preference file. *Default:* Off	

Enable Rectilinear Design	
	Enables you to set a rectilinear object or cut a rectilinear area in a design with IO cells.
Cell Layout Preference	
	Opens the Cell Layout Preference form, which you can use to select the OpenAccess cells whose layout should be displayed. For more information, see Cell Layout Preference.
Binding Key	Opens the Binding Key form, which you use to edit or add binding keys. For more information, see Binding Key.

Cell Layout Preference

Use the Cell Layout Preference form to select the OpenAccess cells whose layout should be displayed.

- In the *Design* Page of the Preferences form (*View - Set Preference*), click the *Cell Layout Preference* button.


Cell Layout Preference — noi-swatip
Layout View List:
Eraser_Brush
Hierarchy Level Upto:
100
Cell Display Criteria:
All Cells
Specified Cells
Cell Display
Cell Name:
Cell Type:
Std. Cell
Cells
Find
Clear & Find
Delete
OK
Apply
Cancel
Help

Cell Layout Preference Form - Fields and Options

Layout View List	Displays the name of the layout view.
Eraser_Brush	Removes cell layout data from memory.
Hierarchy Level Upto	Specifies how many hierarchy levels should be displayed. The available options are: 0, 1,2, 3, 4, 5, and 100. *Default:* 100
Cell Display Criteria	
	All Cells: Displays the layout for all the cells.
	Specified Cells: Displays the layout for the specified cells. To specify the cells, us the *Cell Name* or the *Cell Type* field.
Cell Name	Specify the name of the cell(s) whose layout should be displayed. You can use wildcard (*) for the cell name.
Cell Type	Specify the type of cell(s) whose layout should be displayed. The available options are: Std. Cell, Block, Black Box, Partition, and IO. *Default:* Std. Cell.
Find	Displays the cells in the *Cells* display list.
Clear and Find	Clears the previous result and displays the cells in the *Cells* display list.
Delete	Removes the cells from the *Cells* display list. **Note:** The cells are not actually deleted; they are only removed from the *Cells* display list. When you click OK or Apply, the layout for only those cells that are in the Cells display list is shown.

Related Text Commands

For information on the following commands, see "General Commands" in the *Innovus Text Command Reference*.

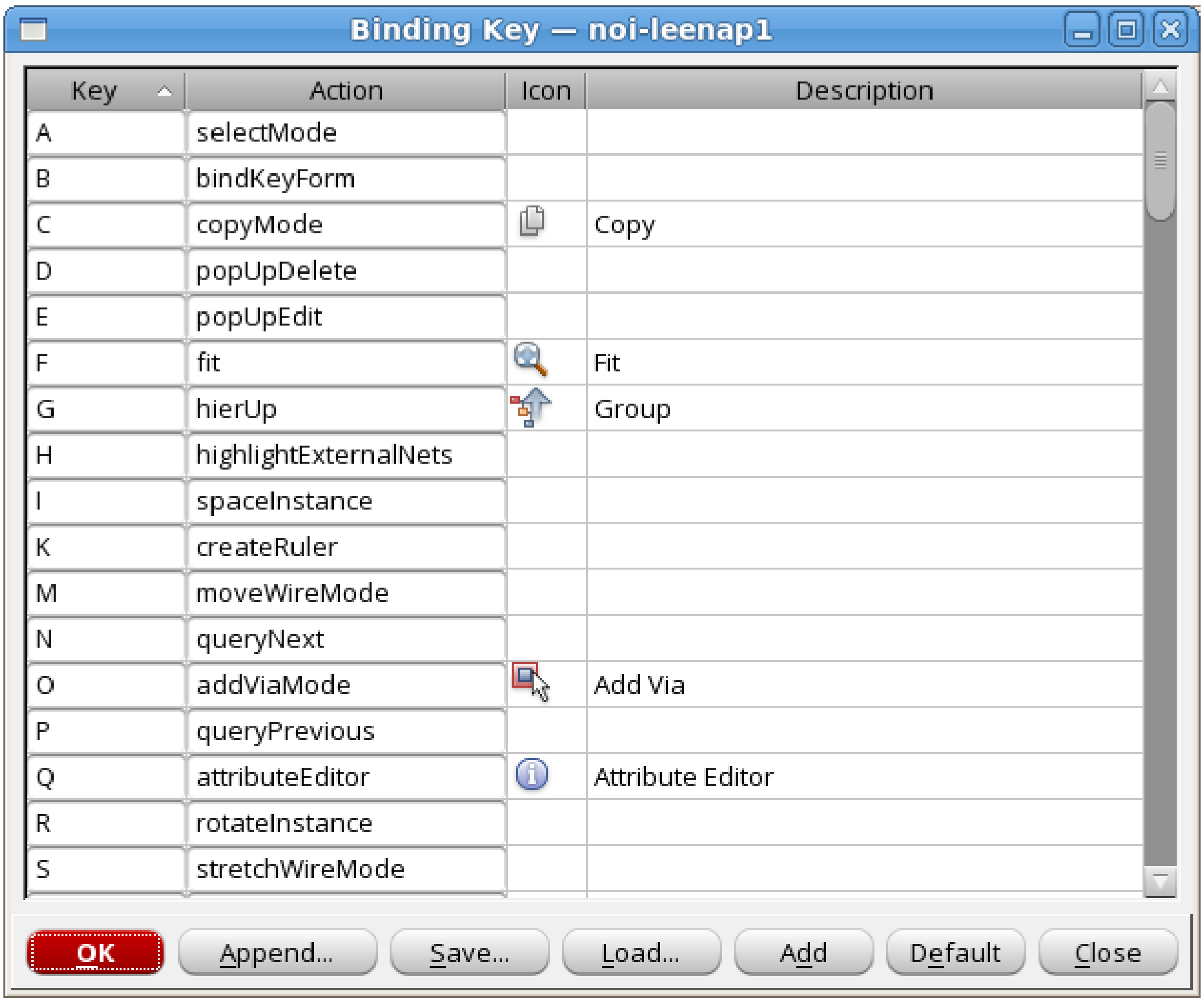
- `setLayerPreference`

- setPreference

Binding Key

Use the Binding Key form to load, save, create, or define keyboard shortcut commands. You can sort either column by selecting the *Key* or *Action* label at the top of the form.

- Choose *View - Set Preference* to open the *Design* page of the Preferences form and click the *Binding Key* button, or click the `B` key in the Innovus main window.



Binding Key Fields and Options

OK	Applies your changes to the design session and closes the window
Append	Opens the Append Binding Key to File form to appends the specified binding key to the selected Tcl file. **Note:** If a binding key is appended with conflicting Tcl file information, the last information read in the file takes precedence and is used.
Save	Opens the Append Binding Key to File form to save your changes to a Tcl file.
Load	Opens the Append Binding Key to File form to load binding key functionality from an existing Tcl file.
Add	Adds an new line to the end of the Binding Key table, where you can specify the key and the action. To create a new binding key shortcut: 1. Click the *Add* button in the Binding Key form. 2. Type the new key in the *Key* column. 3. Start typing the corresponding action for the new bindkey in the *Action* column. As you type, a drop-down list opens to suggest possible actions beginning with the letters you are typing. Enter a suitable action. 4. Click *OK.*
Close	Closes the window without applying any changes.

Related Text Commands

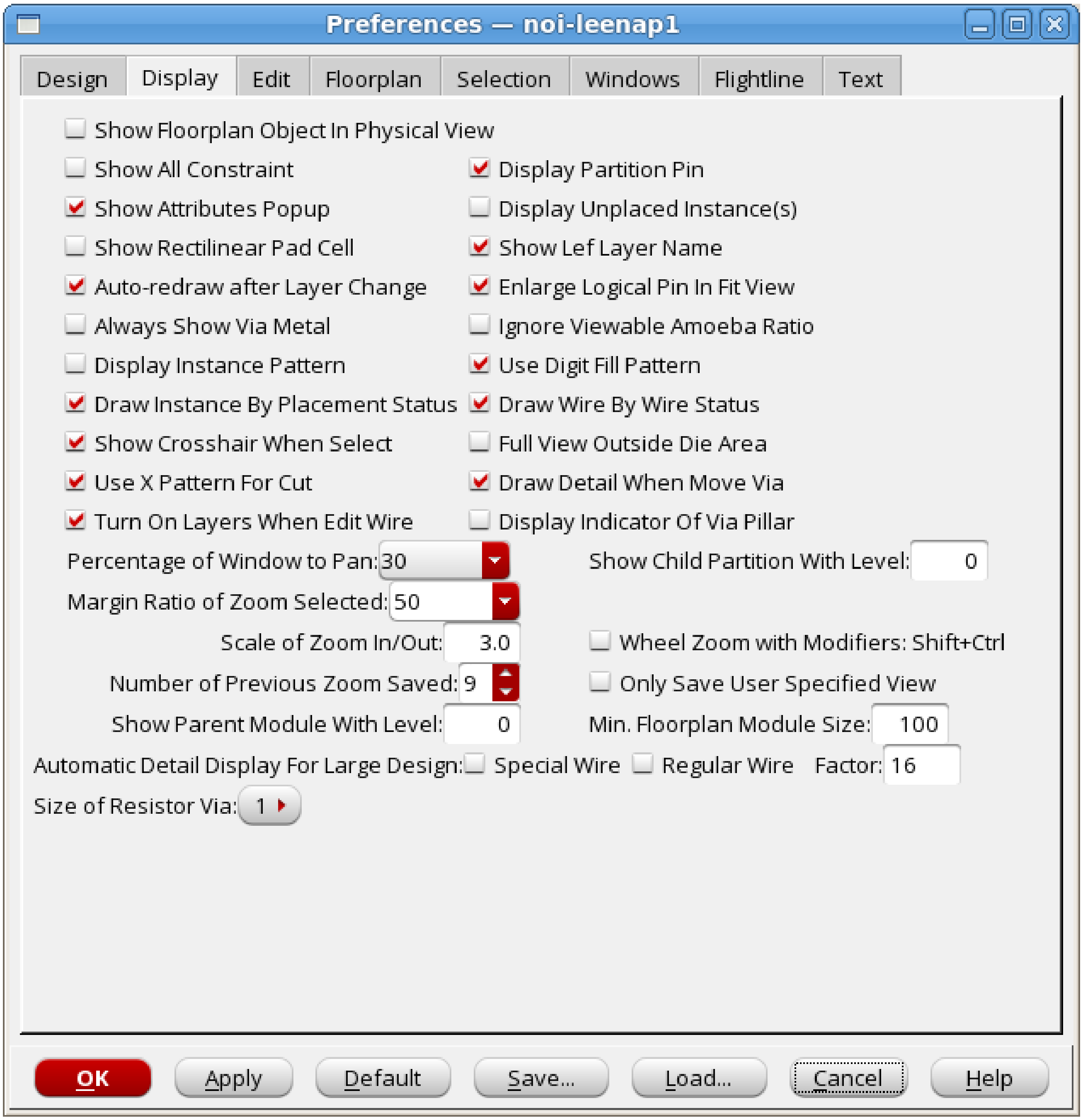
For information on the following commands, see "General Commands" in the *Innovus Text Command Reference*.

- `bindKey`

Preferences - Display

Use the *Display* page of the *Preferences* form to set viewing preferences for standard cells, wires, route congestion ranges, modules, and objects. The default settings are saved in the enc.pref.tcl file; custom settings can be saved with a different file name.

- Choose *View - Set Preference* and click the *Display* tab.

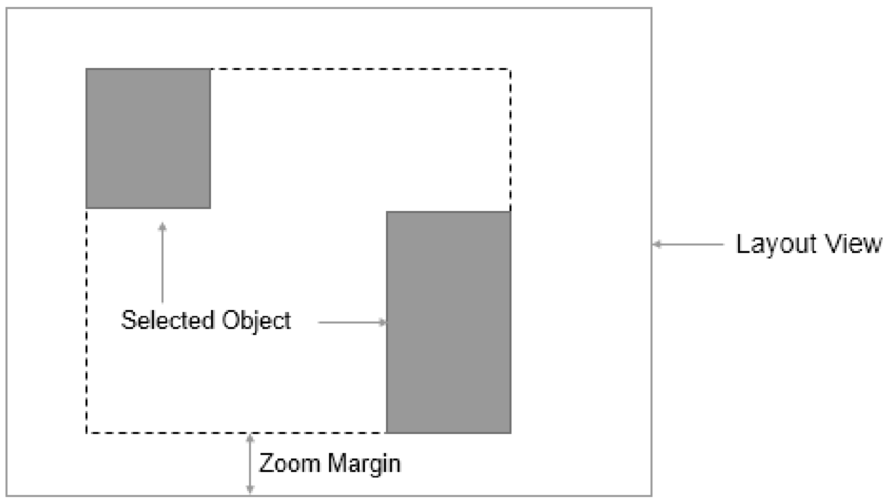


Preferences - Display Fields and Options

Show Floorplan Object in Physical View	Enables the display and querying of floorplan objects in the physical view. You can use this feature together with color groups to create a custom view. For example, you can create a color group that has a custom setting for block colors and use this color group while viewing floorplan objects in the physical view. For information on using color groups, see "Creating and Editing Color Groups" in the File Menu chapter of this document. *Default*: Off
Show All Constraint	Displays all constraints, such as fences, guides, regions, and softguides, regardless of the current hierarchy. When this option is selected, you can see the child guides of each fence as you shape the fence. *Default:* Off
Display Partition Pin	Displays partition pins. *Default:* On
Show Attributes Popup	Specifies that the Context Pop-up Attribute Viewer, which is displayed when you place the mouse cursor over an object, should be displayed. *Default:* On
Display Unplaced Instance(s)	Displays unplaced cells in the Physical view. *Default:* Off
Show Rectilinear Pad Cell	Displays bounding box if the pad cell has rectilinear shape. *Default:* Off
Show Lef Layer Name	Specifies that the layer name as specified in the LEF file should be displayed in the color bar. *Default:* On
Auto-redraw after Layer Change	
	Enables or disables auto-redraw when layers are changed. *Default:* On

Enlarge Logical Pin In Fit View	Displays larger symbols for logical pins in Fit view. Select this option to check the pin distribution in a block design. *Default:* On
Always Show Via Metal	Keeps the additional metal of a via visible even if you turn off the via cut layer. With the *Always Show Via Metal* option selected: • If you turn off the metal layer and keep via on, only the cut via is visible in the main window. • If you turn off the via and keep metal layer on, the top/bottom layer of the via is visible. This option makes it easy for you to view the top/bottom layer of the via by turning off the via. If this option is selected, you can select the via metal and view its attributes in Attribute Editor. *Default:* Off
Ignore Viewable Amoeba Ratio	Displays all modules in the *Amoeba View* when selected, irrespective of their display size. By default, if the display size of a module is smaller than 1/3rd the area of the current module or 1/20th of the fplan box, it is not displayed in the *Amoeba View*. *Default:* Off
Display Instance Pattern	Marks overlapping instances with X in the display area. This makes it easier to identify overlapping instances as compared to the default fill pattern. *Default:* Off
Use Digit Fill Pattern	Displays layer ID digit of the metal layer as part of the pattern for wires. This makes it easy to identify the metal layer of a wire in the design display area. *Default:* On
Draw Instance By Placement Status	Controls thickness of instance borders on the basis of their placement status. Select the new *Draw Instance by Placement Status* option if you want fixed instances to be marked with a thick border. *Default:* On

Draw Wire By Wire Status	Draws the different pattern based on the wire status. Select the *Draw Wire By Wire Status to* enable or disable the thick border which is drawn around the wire and via when it has the fixed status. *Default:* On
Show Crosshair When Select	Displays a crosshair when a small object is selected in the main window. This makes it easier to distinguish the selected object from other objects in the main window. *Default:* On
Full View Outside Die Area	Displays full view outside die area. *Default:* Off
Use X Pattern For Cut	Draws via cuts with an X pattern, instead of the stipple pattern. This makes vias more clearly visible even when you zoom out of a design. *Default:* On
Draw Detail When Move Via	Shows the actual shape of the via while moving it. This makes it easier to align the vertical and/or horizontal segments of the via with wires or pins. If you turn off this option, the via detail is not visible during the move operation. For example, while moving a via with a cross shape, the tool displays a box encompassing the via below the cursor during the drag operation. *Default:* On
Turn On Layers When Edit Wire	Turns on the visibility of the related layers automatically when a wire is being drawn. If you do not want layer visibility to be turned on automatically while drawing a wire, deselect this option. *Default:* On
Display Indicator Of Via Pillar	Displays a dashed-line bounding box around all the shapes in the via of a via pillar. The bounding box has the same color as the cut layer to which the via pillar belongs and becomes visible when you zoom in to the via. *Default:* Off
Percentage of Window to Pan	Specifies the percentage of display area that will be panned when you pan the display using the right or the left arrow keys. *Default*: `30`

Show Child Partition With Level	Displays child partitions from the specified level. *Default:* `0`
Margin Ratio of Zoom Selected	Specifies the zoom margin ratio as an integral value. The zoom margin is the minimum spacing between the bounding box of the selected object(s) and the layout view.  The minimum value is `0` and the maximum value is `99`. *Default:* `50`
Scale of Zoom In/Out	Specifies the scale for the zoom in and zoom out feature. You can use a decimal number for the scale. *Default:* 3.0
Wheel Zoom with Modifiers: Shift+Ctrl	Enables use of scroll wheel to zoom in and out, when used along with the `Shift` and `Ctrl` keys. *Default:* Off
Number of Previous Zoom Saved	Specifies the number of zoom views that are saved. You can then view the previous zoom views by clicking the Zoom Previous icon or the bindkey `w`. For example, if you set the number to 4, you can view four previous zoom views by clicking the Zoom Previous icon or the bindkey `w`. *Default*: 9

<table>
<tr><td>Only Save User Specified View</td><td colspan="2">Controls whether the Previous and Next widgets display both the views explicitly saved by the user and zoom levels. By default, this option is turned off so that when the user clicks the Previous or Next widget repeatedly, the tool cycles through all saved views (saved areas and zoom levels). However, if you turn on this option, the Previous and Next widgets only cycle through the saved areas in the Go To Saved Area submenu in the context menu of the Previous widget.

For more details on how the Previous and Next widgets work, see the The Main Window chapter.

Default: Off</td></tr>
<tr><td>Min. Floorplan Module Size</td><td colspan="2">Filters out modules from the display in the Floorplan view that have an area less than the specified value. For example, a value of 100 displays all the modules that contain 100 or more instances. You can also add a small sized module to the Floorplan view by using the <code>addModuleToFPlan</code> text command.

Note: If modules or submodules contain at least one block, they are always displayed, regardless of the specified value.

Default: 100</td></tr>
<tr><td>Show Parent Module With Level</td><td colspan="2">Displays regions in hierarchy from the specified level.

Default: 0</td></tr>
<tr><td>Automatic Detail Display for Large Design</td><td colspan="2">Controls the performance of redraw in large designs. If you select Special Wire and/or Regular Wire, the tool only draws these wires when you zoom in to the specified level (Factor). By default, the wires are drawn in full view (no zoom) itself.</td></tr>
<tr><td></td><td>Special Wire</td><td>Draws special wires only when you zoom in to the specified level.

Default: Off</td></tr>
<tr><td></td><td>Regular Wire</td><td>Draws regular wires only when you zoom in to the specified level.

Default: Off</td></tr>
<tr><td></td><td>Factor</td><td>Specifies the zoom level at which wires will be drawn in large designs.

Default: 16</td></tr>
</table>

Size of Resistor Via	Controls the resistor via size displayed in GUI. The default resistor size is `1`. This field is useful for debugging purpose when viewing and analyzing vias only.

Related Text Commands

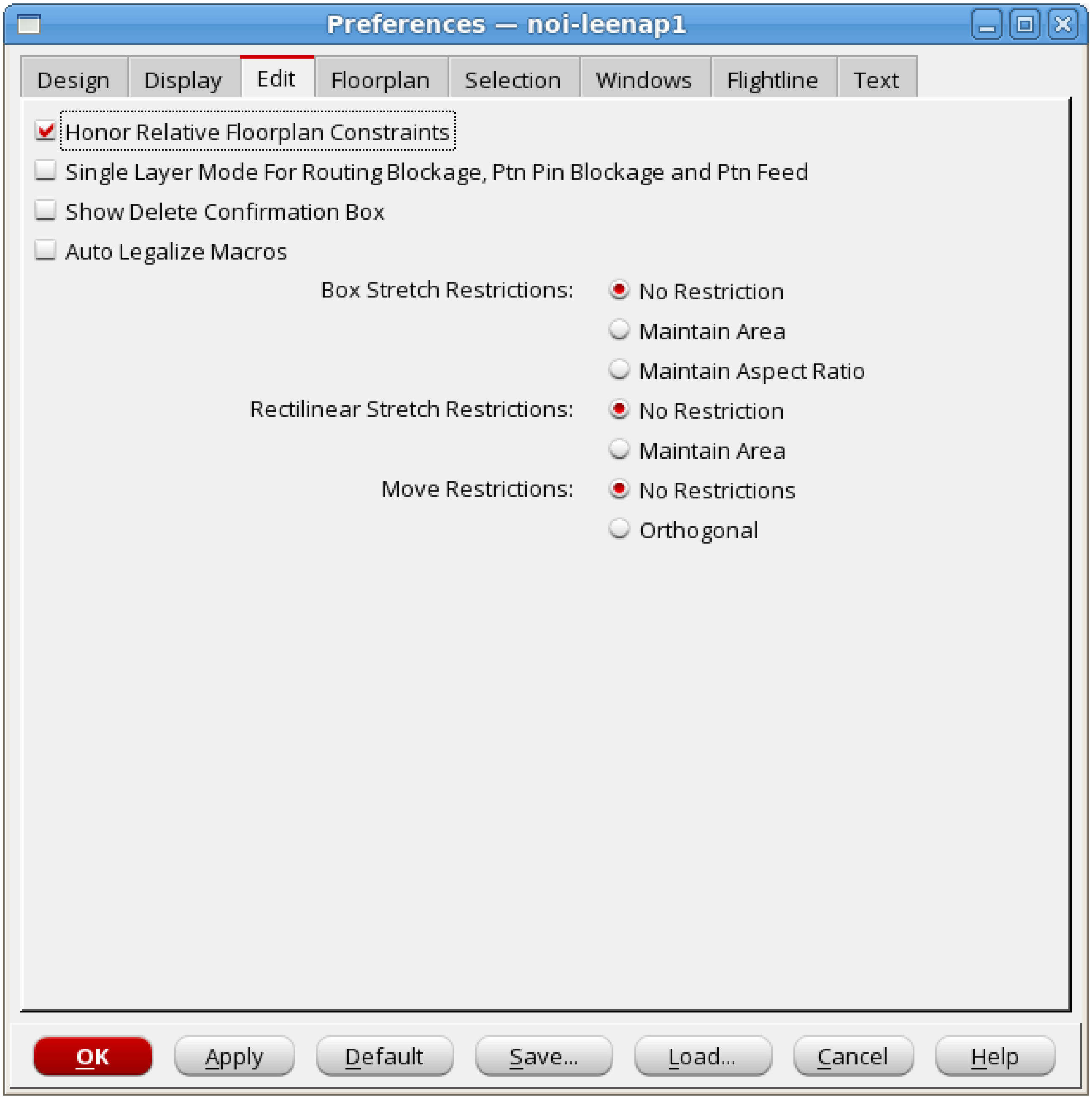
For information on the following commands, see "General Commands" in the *Innovus Text Command Reference*.

- `setLayerPreference`
- `setPreference`

Preferences - Edit

Use the *Edit* page of the *Preferences* form to set interactive editing preferences.

- Choose *View - Set Preference* and click the *Edit* tab.



Preferences - Edit Fields and Options

Honor Relative Floorplan Constraints	Determines whether interactive commands take into account the existing relative floorplan constraints. For example, if you have two blocks called blockA and blockB, and blockA is relative to the right side of blockB: • If *Honor Relative Floorplan Constraints* is enabled, when you move blockB, blockA also moves in such a way that it still stays on the right side of blockB. You cannot move blockA to another location because it must stay on the right side of blockB. • If *Honor Relative Floorplan Constraints* is disabled, when you move blockB, blockA does not move with it, and can be freely moved to another location. *Default:* On	
Single Layer Mode For Routing Blockage, Ptn Pin Blockage and Ptn Feed	Supports single routing blockage movement. If you select this option, you can move the selected routing blockage without affecting other routing blockages in the same location. *Default:* Off	
Show Delete Confirmation Box	Displays a dialog box that prompts for confirmation whenever you delete an object. *Default:* Off	
Auto Legalize Macros	Determines if the macros will be legalized automatically after they are moved. • If *Auto Legalize Macros* is enabled, you can legalize the macros automatically after moving them. • If *Auto Legalize Macros* is disabled, you cannot legalize the macros automatically after moving them. *Default:* Off	
Box Stretch Restrictions		
	No Restriction	No restrictions when resizing an object. *Default:* On

	Maintain Area	Maintains the area of an object when resizing. This is applicable for edge stretching as well as for corner resizing. *Default:* Off
	Maintain Aspect Ratio	
		Maintains the aspect ratio of an object when resizing. *Default:* Off
Rectilinear Stretch Restrictions		
	No Restriction	No restrictions when resizing a rectilinear object. *Default:* On
	Maintain Area	Maintains the area of a rectilinear object when resizing. *Default:* Off
Move Restrictions		
	No Restriction	No restrictions when moving an object. *Default:* On
	Orthogonal	Restricts the object moves to straight vertical and horizontal directions. *Default:* Off

Preferences - Floorplan

Use the *Floorplan* page of the Preferences form to set object behavior, including movement capabilities for guides regions, fences, snap macros, or blackboxes. The default settings are saved in the enc.pref.tcl file; custom settings can be saved with a different filename.

- Choose *View - Set Preference* and click the *Floorplan* tab.

Preferences - Floorplan Fields and Options

Snap	Sets the rules for snapping floorplan objects to the grid.

	Fence/Region/Guide to	Specifies the snapping of floorplan guides, regions, and fences.You can choose the grid on which the snap rule is set by selecting one of the following options: • *Manufacture Grid* • *Instance Grid* • *User-define Grid* • *Placement Grid* • *LayerTrack Grid* • *FinFET Manufacture Grid* • *FinFET Instance Grid* • *FinFET Placement Grid* *Default: Instance Grid*
	Macro/BlackBox to	Specifies the snapping of macros and blackboxes. You can choose the grid on which the snap rule is set by selecting one of the following options: • *Manufacture Grid* • *Instance Grid* • *User-define Grid* • *Placement Grid* • *LayerTrack Grid* • *FinFET Manufacture Grid* • *FinFET Instance Grid* • *FinFET Placement Grid* *Default: Manufacture Grid*

	Placement Blockage to	Specifies the snapping of placement blockages. You can choose the grid on which the snap rule is set by selecting one of the following options: • *Manufacture Grid* • *Instance Grid* • *User-define Grid* *Default: Instance Grid*
	IO Pad to	Specifies the snapping of IO pads. You can choose the grid on which the snap rule is set by selecting one of the following options: • *Manufacture Grid* • *Instance Grid* • *User-define Grid* • *Placement Grid* • *LayerTrack Grid* • *FinFET Manufacture Grid* • *FinFET Instance Grid* • *FinFET Placement Grid* *Default: Manufacture Grid*

	Die to	Sets the rules for snapping the die. You can choose the grid on which the snap rule is set by selecting one of the following options: • *Manufacture Grid* • *Instance Grid* • *User-define Grid* • *Placement Grid* • *LayerTrack Grid* • *FinFET Manufacture Grid* • *FinFET Instance Grid* • *FinFET Placement Grid* *Default: Placement Grid*
	Core to	Sets the rules for snapping the core. You can choose the grid on which the snap rule is set by selecting one of the following options: • *Manufacture Grid* • *Instance Grid* • *User-define Grid* • *Placement Grid* • *LayerTrack Grid* • *FinFET Manufacture Grid* • *FinFET Instance Grid* • *FinFET Placement Grid* *Default: Placement Grid*
Snap All Corners to Grid	Snaps all corners to the grid.	

User-defined Grid	Snaps I/O cells to a user-defined grid. You can change the default snapping to a grid defined in the *X* and *Y* location fields. The *X* and *Y* fields are for the horizontal and vertical spacing between the user-defined snap grids. The *X* and *Y Offset* fields are for the distance values from the lower left corner of the design or die to the first x y grid, respectively. By default, the *X* and *Y Offset* values are 0.0 microns. However, if you choose *User-defined Grid*, but do not provide the *X* and *Y* spacing values, you will get the error message: *User-defined grid should be greater than 0 for both X and Y direction*. Specify the *Unit* by selecting *Micron* or *Track*. The user-defined grid is honored by the interactive move and stretch features in the *Snap Floorplan* menu command, and by the *Relative Floorplan* menu commands.	
Clones snapping to same master row orientation	Allows you to keep clone to be on different row orientation than the master.	
Descendant Macros Move with Their Ancestor Modules for Constraints		
	Guide	Allows you to move guide objects with their descendant standard cells when floorplanning.
	Region	Allows you to move region objects with their descendant blocks when floorplanning.
	Fence (default)	Allows you to move fence objects with their descendant blocks when floorplanning. **Note:** If you move descendant blocks with a fence, blocks outside the fence boundary also move, but unplaced blocks will not move.
Descendant Std Cell Move with Their Ancestor Modules for Constraints		
	Guide	Allows you to move guide objects with their descendant standard cells when floorplanning.
	Region	Allows you to move region objects with their descendant standard cells when floorplanning.

	Fence	Allows you to move objects with their descendant standard cells when floorplanning. **Note:** If you move descendant standard cells with a fence, standard cells outside the fence boundary also move, do unplaced cells do not move.
	Move Preplaced Cell Only	Allows you to move only preplaced descendant cells with their group, region, and fence when floorplanning. **Note:** When this option is not selected, all descendant cells, preplaced or not, move with the guide, region, and fence.

Related Text Commands

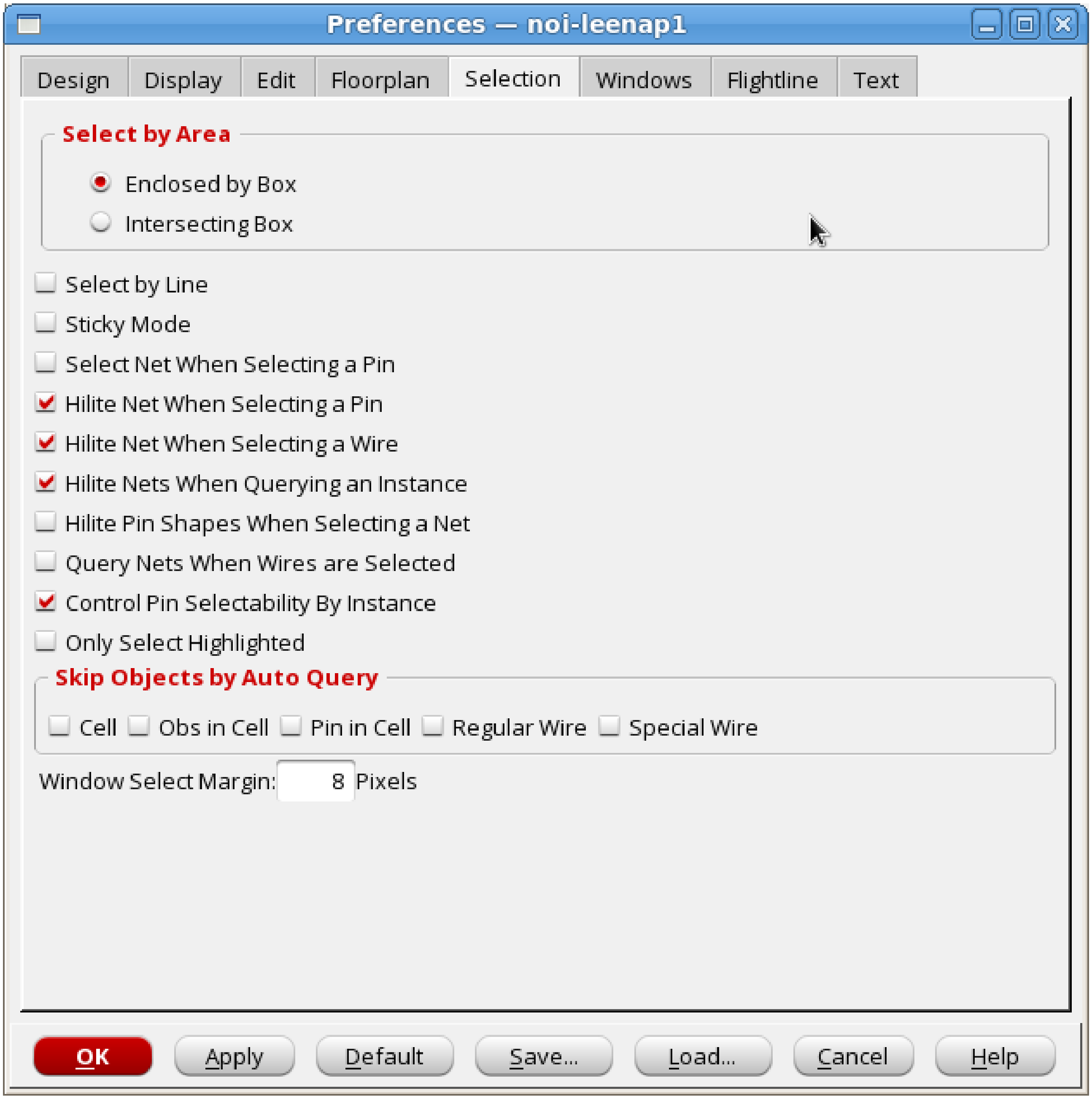
For information on the following commands, see "Floorplan Commands" in the *Innovus Text Command Reference*.

- `snapFPlan`

Preferences - Selection

Use the *Selection* page of the Preferences form to select and display objects and determine their behavior within a selected area. The default settings are saved in the enc.pref.tcl file; custom settings can be saved with a different filename.

- Choose *View - Set Preference* and click the *Selection* tab.



Preferences - Selection Fields and Options

Select by Area

<table>
<tr><td></td><td>Enclosed by BoxEnclosed by Box</td><td>Selects objects that are fully enclosed inside the specified area. Use the left mouse button to draw and define an area or bounding box. Any objects fully enclosed inside the drawing area are selected.
Default: On</td></tr>
<tr><td></td><td>Intersecting Box</td><td>Selects objects that are fully enclosed or intersected within the specified area. Use the left mouse button to draw and define an area or bounding box. Any objects enclosed inside or intersected with the area bounding box are selected. This mode should be used to select wire or row.
Default: Off</td></tr>
<tr><td>Select by Line</td><td colspan="2">Specifies that objects can be selected by drawing a line that crosses the objects.

When you select this option and then choose the Select widget from the main menu, you can draw a line across several objects in the GUI; all the objects that the line crosses are selected.

Alternatively, you can use the <code>Ctrl + M</code> key combination to toggle between window and line selection modes quickly:
The default selection mode is window.
Press the <code>Ctrl + M</code> key combination to switch to the line selection mode.
After making line selections, press the <code>Ctrl + M</code> key combination again to switch back to the window selection mode.
Default: Off</td></tr>
<tr><td>Sticky Mode</td><td colspan="2">Reverse the object selection behavior. When you select the Sticky Mode option, the selection behavior changes as follows:
Single click: adds current object to selection.
CTRL+single click: selects new object (and clears previous selection).
This feature is useful when, for example, you want to select multiple objects without having to press the CTRL key while clicking.</td></tr>
<tr><td colspan="3">Select Net When Selecting a Pin</td></tr>
<tr><td></td><td colspan="2">Selects a net through a pin selection. If this option is set when you select a pin, the corresponding net is selected.
Default: Off</td></tr>
</table>

Hilite Net When Selecting a Pin	
	Highlights a net through a pin selection. If this option is set when you select a pin, the corresponding net is highlighted. *Default:* On
Hilite Net When Selecting a Wire	
	Highlights a net through a wire selection. If this option is set when you select a wire, the corresponding net is highlighted. You can turn this option off to hide the center line of the net when selecting a wire. *Default:* On
Hilite Nets When Querying an Instance	
	Highlights nets that are connected to an instance when this instance is queried. For example, if you query a selected instance and this option is set, all nets that connect to this instance pin are also highlighted. *Default*: On
Hilite Pin Shapes When Selecting a Net	
	Highlights connected cell term shapes when you select a net. *Default*: Off
Query Nets When Wires are Selected	
	Queries all nets that connect to the selected wires. *Default:* Off
Control Pin Selectability by Instance	
	Controls the selection of pins in an instance. You can select only partial pins in an instance by using the *Select by Line* method when this option is on. *Default*: On
Only Select Highlighted	
	Selects only the highlighted objects during box selection. If this option is turned on and you draw a box on the main window to select objects, non-highlighted objects are not selected even if they fall within the selection box. *Default:* Off

Skip Objects by Auto Query	
	Skips querying of specified objects. You can choose to skip Auto Query of: • *Cell* • *Obs in Cell* • *Pin in Cell* • *Regular Wire* • *Special Wire*
Window Select Margin	Specifies the number of pixels for the window margin. *Default:* 8

Related Text Commands

For information on the following commands, see "General Commands" in the *Innovus Text Command Reference*.

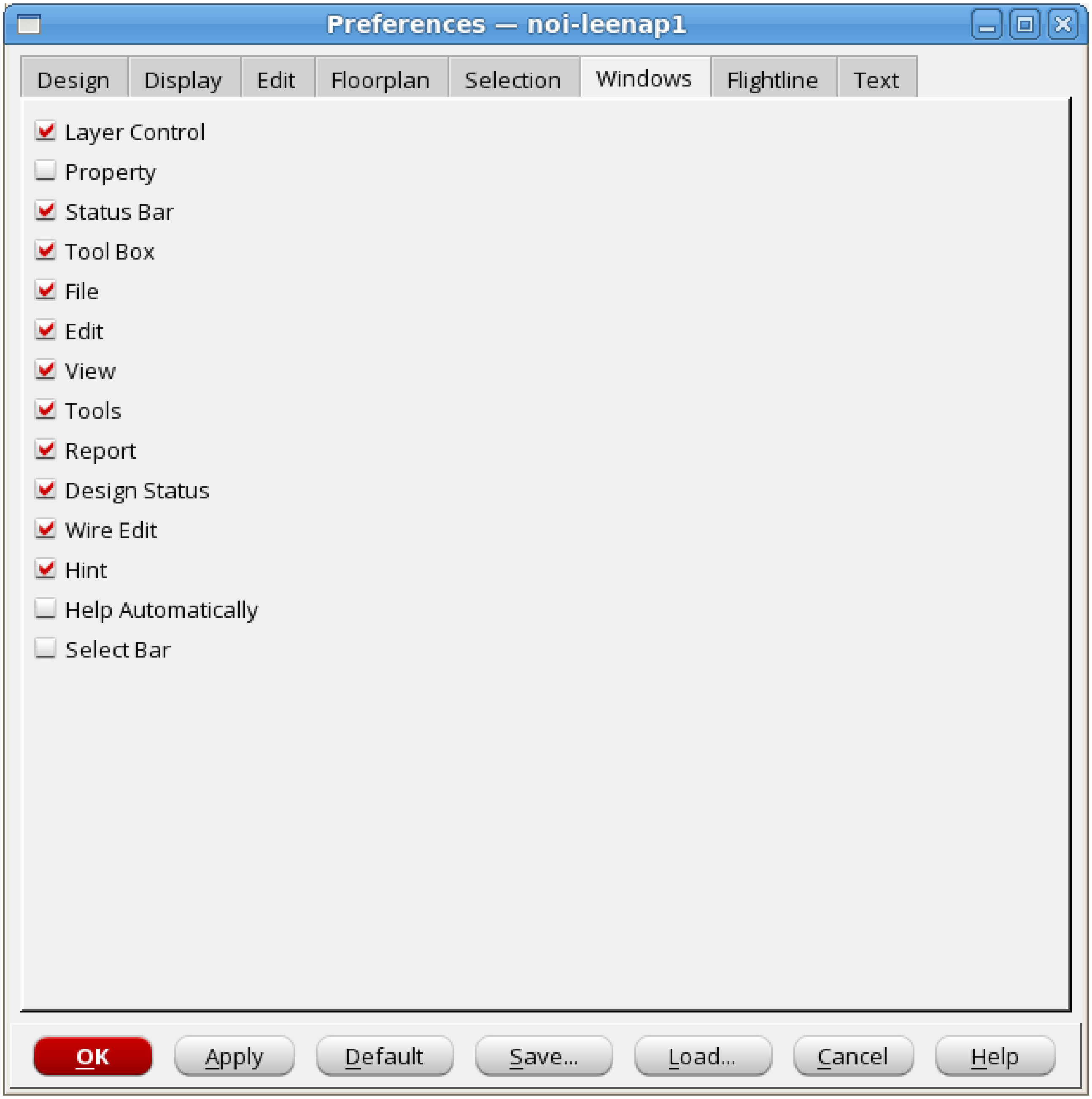
- `setLayerPreference`
- `setPreference`

Preferences - Windows

Use the *Windows* page of the Preferences form to show or hide Innovus main display windows. When you click the *OK* or the *Apply* button, the Windows settings are saved in the.enc file in your home directory. When you launch a new session, the settings in the .enc file are loaded automatically. The Windows settings are also saved in the .enc file when you click the Save button and save the other settings for Design, Display, Floorplan, and Selection in the .enc.pref.tcl or some other file.

Note: This page shows the same windows that are selected or deselected in the *Show/Hide* menu.

- Choose *View - Set Preference* and click the *Windows* tab.



Preferences - Windows Fields and Options

Layer Control	Controls the visibility, selectability, and color display of various attributes at the top right side of the main window. *Default:* On

Property	Controls the Attribute Viewer panel that appears when you place the cursor over an object. See "Context Pop-up Attribute Viewer" in the The Main Window chapter for more information. *Default:* Off
Status Bar	Controls the message bar display below of the main design display area, which shows object identifier or coordinate information. *Default:* On
Tool Box	Controls the tool widget display above the design display area. See Tool Widgets for more information. *Default:* On
File	Controls the display of widgets related to the File menu in the Toolbar Widget area above the design display area. See Toolbar Widgets for more information. *Default:* On
Edit	Controls the display of widgets related to the Edit menu in the Toolbar Widget area above the design display area. See Toolbar Widgets for more information. *Default:* On
View	Controls the display of widgets related to the View menu in the Toolbar Widget area above the design display area. See Toolbar Widgets for more information. *Default:* On
Tools	Controls the display of widgets related to the Tools menu in the Toolbar Widget area above the design display area. See Toolbar Widgets for more information. *Default:* On
Report	Controls the display of widgets related to the File - Report submenu in the Toolbar Widget area above the design display area. See Toolbar Widgets for more information. *Default:* On
Design Status	Controls the display of Design Status widget in the Toolbar Widget area above the design display area. See Toolbar Widgets for more information. *Default:* On
Wire Edit	Controls the display of the Wire Edit widgets.

Hint	Activates the help system. *Default:* On
Help Automatically	Activates the help system. *Default:* Off
Select Bar	Controls the display of the window to select or deselect objects. *Default:* Off

Related Text Commands

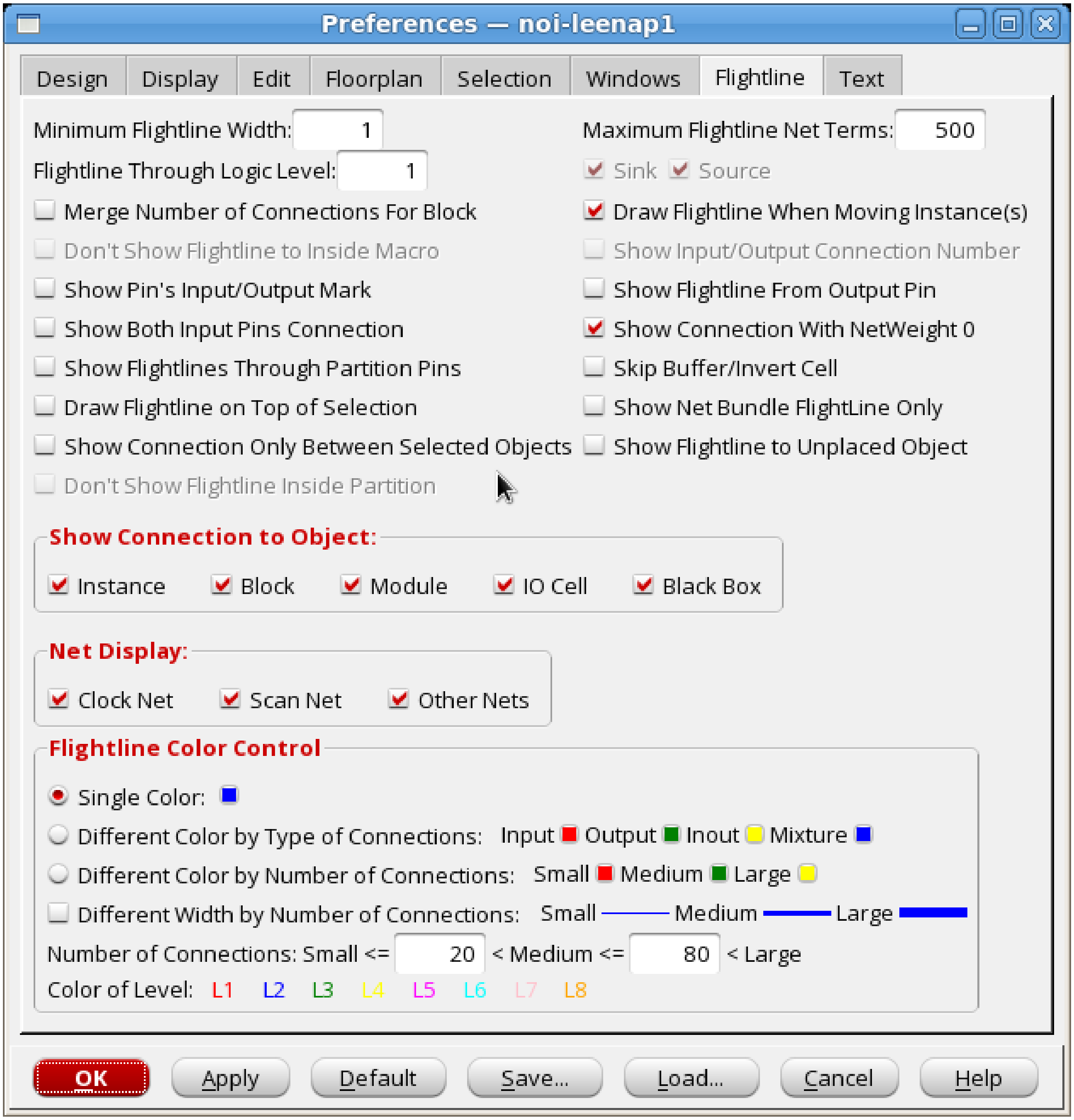
For information on the following commands, see "General Commands" in the *Innovus Text Command Reference*.

- `setWindowPreference`

Preferences - Flightline

Use the *Flightline* page of the Preferences form to set options for displaying net connections in the design.

- Choose *View - Set Preference* and click the *Flightline* tab.



Preferences - Flightline Fields and Options

Minimum Flightline Width	Sets the minimum connection threshold in order for flightlines to be displayed in the Floorplan view. For example, a threshold value of 5 displays flight lines that have 5 or more connections between modules and blocks. *Default:* 1 (Displays all flight lines)
Maximum Flightline Net Terms	Sets the maximum connection threshold in order for flightlines to be displayed in the Floorplan view. For example, a value of 500 displays the flight lines for nets that have 500 terminals or less. *Default:* 500
Flightline Through Logic Level	Displays flightlines up to the specified logic level for the selected instance. For example, if you select *2* in the drop-down and then select a std cell in the main window, the tool will draw flightlines to all instances connected to the selected std cell till up to 2 logic levels. If you select a value higher than 1 from the drop-down, the *Sink* and *Source* check boxes are enabled: • *Sink* - Traces flightlines from the output pins of the selected instance. • *Source* - Traces flightlines from the input pins of the selected instance. *Default:* 1
Merge Number of Connections For Block	Displays the number of net connections from a selected block. *Default:* Off
Draw Flightline When Moving Instance(s)	Displays net connections for instances when you move them. *Default:* On
Don't Show Flightline to Inside Macro	Disables the display of the flightlines to macros that are embedded inside a module. *Default:* Off

Show Input/Output Connection Number	Displays the total number net connections, the number of input connections, and the number of output connections for a selected block. For example, if there are 23 total connections for the selected block and they are all output connections, the main window displays the following numbers: 23/0/23. **Note:** The software does not include I/Os in the number of output connections. Therefore, if the software displays a number such as: 10/5/4, this indicates that one of the output connections is an I/O. *Default:* Off
Show Pin's Input/Output Mark	Displays a symbol that distinguishes whether the pin is an input or an output pin on the block. The software displays an "o" for output pins, and an "x" for input pins. *Default:* Off
Show Flightline From Output Pin	Displays flightlines from the output pin, instead of using the center of gravity representation style. *Default:* Off
Show Both Input Pins Connection	Displays net connections between inputs pins of two blocks or modules. *Default:* Off
Show Connection With Netweight 0	Displays flightlines for nets that have a weight of 0. *Default:* On
Show Flightlines Through Partition Pins	Displays net and connection flightlines to partition pins for the selected partition module. If this check box is not selected, the software displays net connections to instances inside partition blocks, but does not display the connection to the partition pins. This option can be useful for checking pin assignment results, especially for the un-committed partition pins. *Default:* Off

Skip Buffer/Invert Cell	Ignores buffer or inverter cells and displays the flightline connection from macro to the first sequential cell. *Default:* Off
Draw Flightline on Top of Selection	Changes the drawing order so that the flightlines are always drawn last and are shown on top of highlighted objects. Select this option if standard cell highlights are significantly reducing flightline visibility. *Default:* Off
Show Net Bundle FlightLine Only	Displays only the flightlines based on net bundles. *Default:* Off
Show Connection Only Between Selected Objects	Displays net connections between only the selected objects. *Default:* Off
Show Flightline to Unplaced Object	Controls the display of flightlines to unplaced objects, including unplaced physical pins and unassigned partition pins. Keep this option unchecked if you want to focus on analyzing pin connections for placed objects. Flightlines to unplaced objects may seem as "noise" while analyzing pin connections for placed objects. *Default*: Off
Don't show Flightline Inside Partition	Controls the display of flightlines inside partitions. By default, the software displays flightlines inside partitions. Keep this option unchecked if want to focus on checking the alignment of the top-level connections. Flightlines inside partitions may seem as "noise" while analyzing top-level connections. *Default*: Off
Show Connection to Object	Shows connections to the following objects if their corresponding check box is selected.

	Instance	Shows flightlines to instances, if selected. *Default*: On
	Block	Shows flightlines to blocks, if selected. *Default*: On
	Module	Shows flightlines to modules, if selected. *Default*: On
	IO Cell	Shows flightlines to IO cells, if selected. *Default*: On
	Black Box	Shows flightlines to black box, if selected. *Default*: On
Net Display	Shows connections for the following nets if the corresponding check box is selected.	
	Clock Net	Displays clock net connections. Deselect this check box to hide clock net connections to improve flightline visibility. *Default:* On
	Scan Net	Displays flightlines for scan chains. You can deselect this check box to turn off the scan chain flightlines. *Default:* On
	Other Nets	Displays flightlines for other nets. *Default:* On
Flightline Color Control	Provides options for controlling color and width of flightlines	

	Single Color	Uses a single color for all flightlines. *Default:* On *Default Color:* Blue
	Different Color by Type of Connections	Displays the input, output, and inout net connections using different colors. *Default:* Off *Default Connection Color*s: • *Input* - Red • *Output* - Green • *Inout* - Yellow • *Mixture* - Blue
	Different Color by Number of Connections	Displays small, medium, and large number of net connections using different colors. *Default:* Off *Default Connection Color*s: • *Small* - Red • *Medium* - Green • *Large* - Yellow
	Different Width by Number of Connections	Displays small, medium, and large number of net connections using lines of different widths. *Default:* Off *Default Widths*: • *Small* - Thin line • *Medium* - Medium line • *Large* - Thick line

	Number of Connections	Specifies the thresholds for determining whether number of connections is small, medium, or large. By default, connections lower than 20 is considered *Small,* connections equal to or between 20 and 80 is considered *Medium,* and connections greater than 80 is considered *Large.* *Default Low Threshold*: 20 *Default High Threshold:* 80
	Color of Level	Specifies the colors for L1 to L8 levels of flightlines.

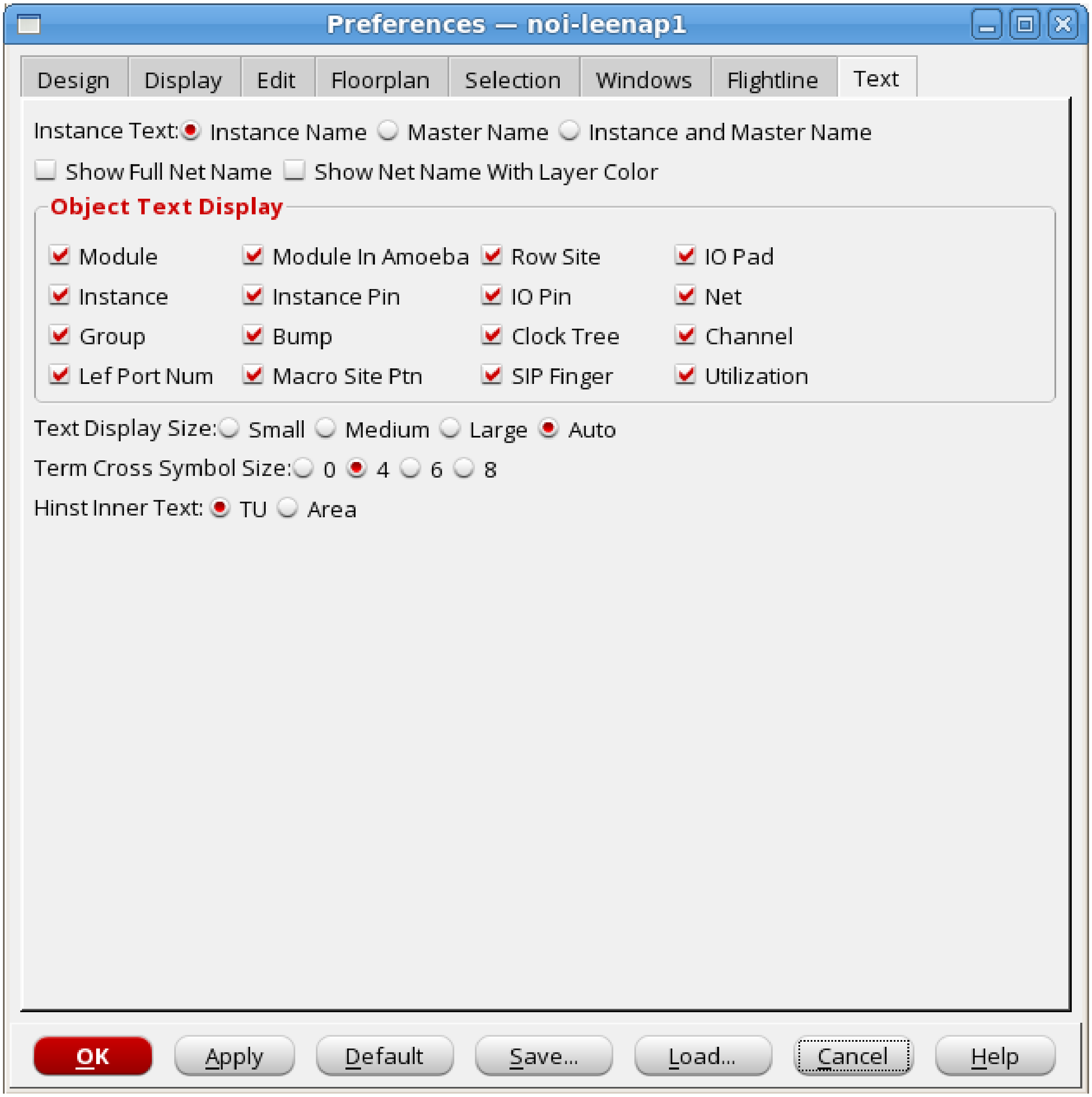
Preferences - Text

Use the *Text* page of the Preferences form to customize the way text is displayed on the main window. The *Text* tab in the Preferences form enables you to do the following:

- Choose whether you want to view instance name or master name as instance text
- Select/de-select the objects for which you want to view text labels
- Choose text display size
- Choose term cross symbol size

To open the *Text* page:

- Choose *View - Set Preference* and click the *Text* tab.



Preferences - Text Fields and Options

Instance Text	Specifies what will be displayed as instance text.

	Instance Name	Specifies that instance name will be displayed as instance text. *Default*: On
	Master Name	Specifies that master cell name will be displayed as instance text. *Default*: Off
	Instance and Master Name	Specifies that both instance and master cell name will be displayed as instance text. *Default*: Off
Show Full Net Name	Displays complete net names in the design area.	
Show Net Name With Layer Color		
	Displays net name with layer color.	
Object Text Display	Specifies the objects for which you want to view text labels.	
	Module	Specifies that module labels will be displayed. *Default*: On
	Module in Amoeba	Specifies that module labels will be displayed in Amoeba view. *Default*: On
	Row Site	Specifies that row site labels will be displayed. *Default*: On
	IO Pad	Specifies that IO pad labels will be displayed. *Default*: On
	Instance	Specifies that instance labels will be displayed. *Default*: On

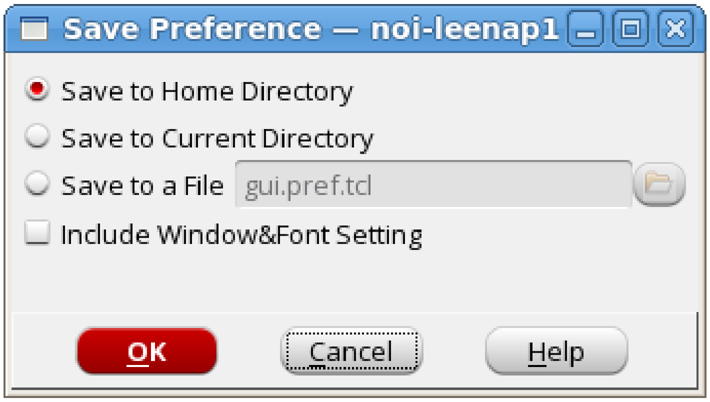
	Instance Pin	Specifies that instance pin labels will be displayed. *Default*: On
	IO Pin	Specifies that IO pin labels will be displayed. *Default*: On
	Net	Specifies that net names will be displayed. *Default*: On
	Group	Specifies that group labels will be displayed. *Default*: On
	Bump	Specifies that bump labels will be displayed. *Default*: On
	Clock Tree	Specifies that clock tree labels will be displayed. *Default*: On
	Channel	Specifies that channel labels will be displayed. *Default*: On
	Lef Port Num	Specifies that LEF port number labels will be displayed. *Default*: On
	Macro Site Ptn	Specifies that macro site partition labels will be displayed. *Default*: On
	SIP Finger	Specifies that System-in-Package finger labels will be displayed. *Default*: On
	Utilization	Specifies that target utilization will be displayed. *Default*: On

Text Display Size	Specifies the text display size. Choose one of the following options: • *Small* • *Medium* • *Large* • *Auto* *Default*: *Small*
Term Cross Symbol Size	Specifies the term cross symbol size. Choose one of the following options: • *0* • *4* • *6* • *8* If you set *0* as the value for the *Term Cross Symbol Size* option, the input and output pin symbols (*X* and *O* symbols) are not displayed in the main window. *Default*: *4*
Hinst Inner Text	Specifies whether to display target utilization (TU) or area on partition fence. Choose one of the following options: • *TU* • *Area* *Default: TU*

Save Preference

Use the Save Preference form to save custom preference design settings to a file. By default, settings are saved in the enc.pref.tcl file; however, custom settings can be saved to a different file.

- Choose *View - Set Preference* to open the Preferences form and click the *Save* button.



Fields and Options

Save to Home Directory	Saves the preference file in the user's home directory. *Default:* On
Save to Current Directory	Saves the preference file in the current working directoy. *Default:* Off
Save to a File	Specifies the name of a file in which to save the preference settings. *Default:* gui.pref.tcl
Include Window & Font Setting	Saves the window and text font settings. *Default:* Off

Related Text Commands

- `setPreference`

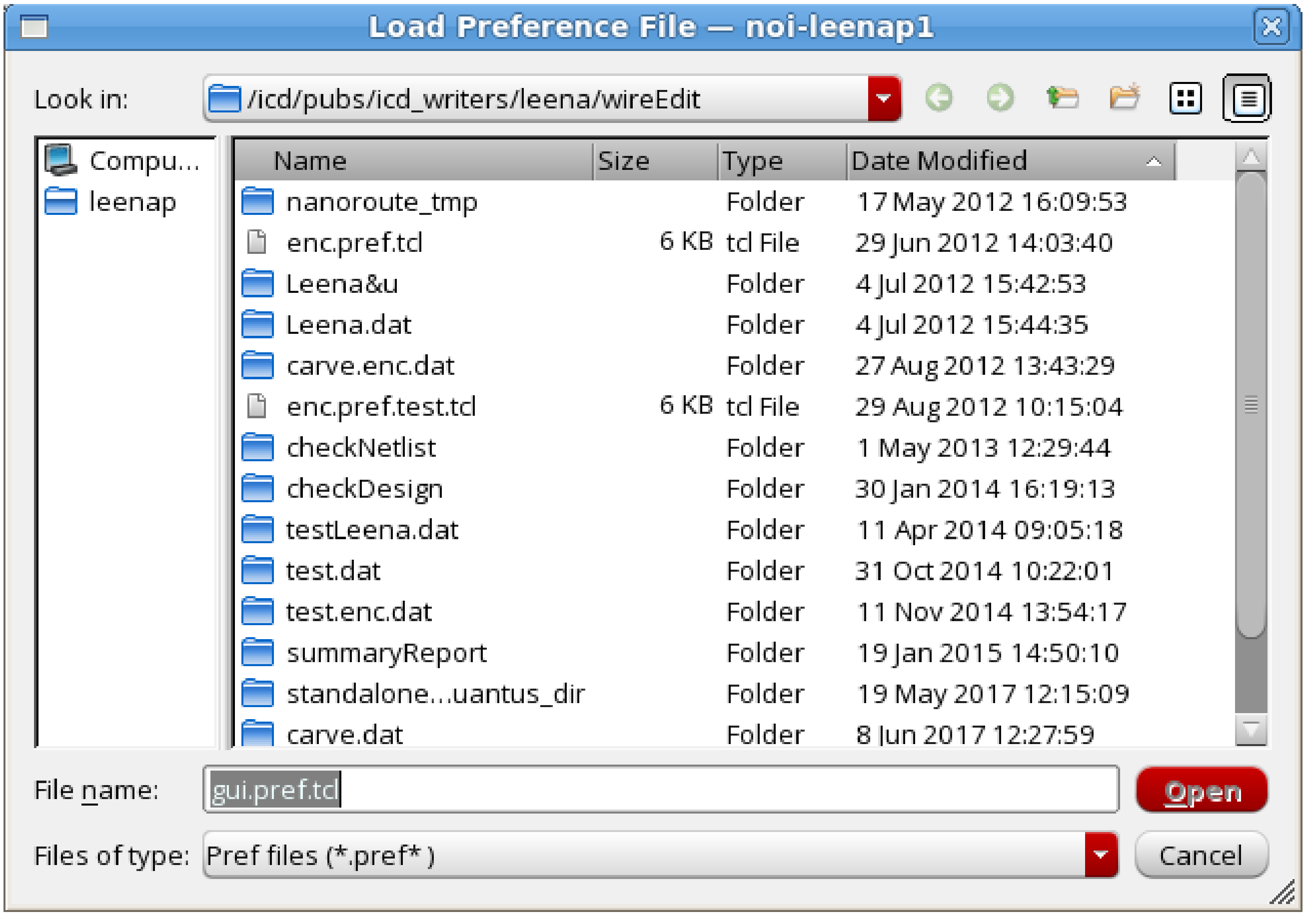
For information on the following topics, see Getting Started in the *Innovus User Guide*:

- Setting Preferences
- Initialization Files

Load Preference File

Use the Load Preference File form to load a previously saved file. By default, settings are saved in the enc.pref.tcl file; however, custom settings can be saved to a different file.

- Choose *View - Set Preference* to open the Preferences form and click the *Load* button.



All Colors

Use the *All Colors* menu item in the *View* menu to set advanced color options. This item opens the Color Preferences form, which has five pages:

- Objects Page
  - Front Bumps Color Selection
  - Back Bumps Color Selection
  - Bus Guide Color Selection

   - Power Domain Color Selection
- Wire/Via Page
- View-Only Page
- Custom Page
- Cell Layout Page

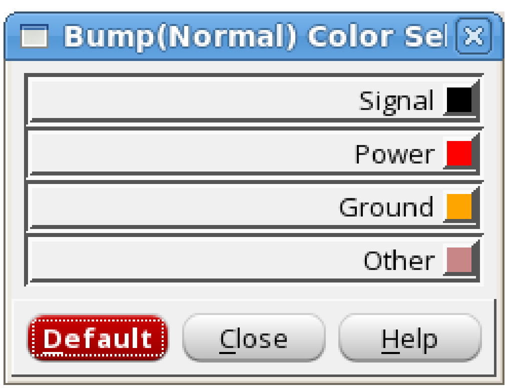
Note: The Color Preferences form can also be accessed from the main window by clicking the All Colors button in the Layer Control sub-window.

For more information on the Color Preferences form and its sub-forms, please read the Color Preferences section in the "Main Window" chapter of the *Innovus Menu Reference*.

Front Bumps Color Selection

Use the Bump(Normal) Color Selection form to change the color of front bumps in the design. Front bumps are bumps on the top metal layer.

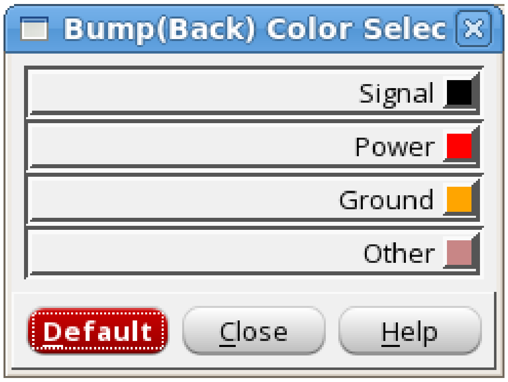
1. Open the Color Preferences form. Choose *View* > *All Colors* from the menu or click the *All Colors* button on the Layer Control bar.
2. The *Objects* page is open by default. Click the *Bump(Normal) Color* box next to the *Bump(Normal)* object type. This displays the Bump(Normal) Color Selection form.
3. Click the color box for a bump type to display the Select Color form. Choose a new color for the bump type.



Back Bumps Color Selection

Use the Bump(Back) Color Selection form to change the color of back bumps in the design. Back bumps are bumps on the back side metal layer.

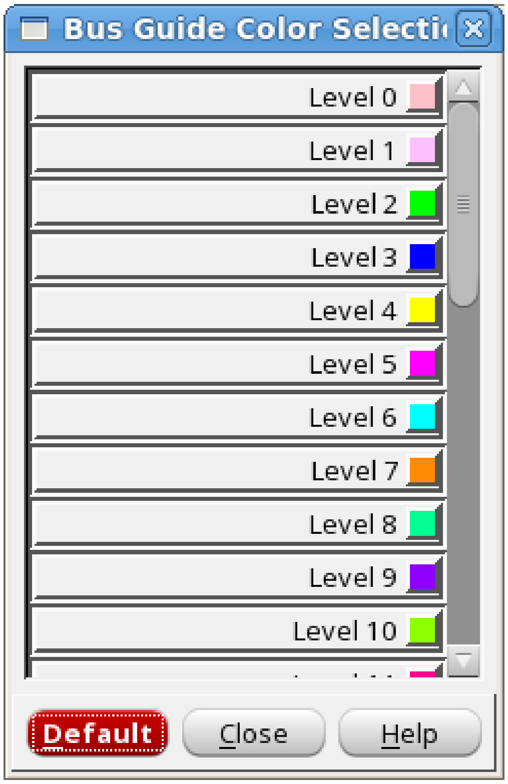
1. Open the Color Preferences form. Choose *View > All Colors* from the menu or click the *All Colors* button on the Layer Control bar.
2. The *Objects* page is open by default. Click the *Bump(Back) Color* box next to the *Bump(Back)* object type. This displays the Bump(Back) Color Selection form.
3. Click the color box for a bump type to display the Select Color form. Choose a new color for the bump type.



Bus Guide Color Selection

Use the *Bus Guide Color Selection* form to specify multiple colors for bus guide objects.

- Click the *Color Preferences > Objects > Bus Guide* object type to display the *Bus Guide Color Selection* form.

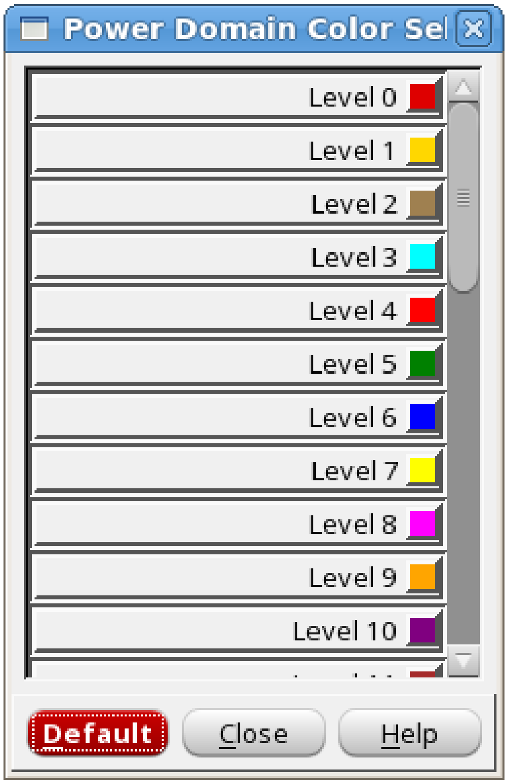


For more information, see "Customizing the Bus Guide Display" in the Bus Planning chapter of the *Innovus User Guide*.

Power Domain Color Selection

Use the *Power Domain Color Selection* form to change the color of power domains in the design. This form contains a list of all power domains.

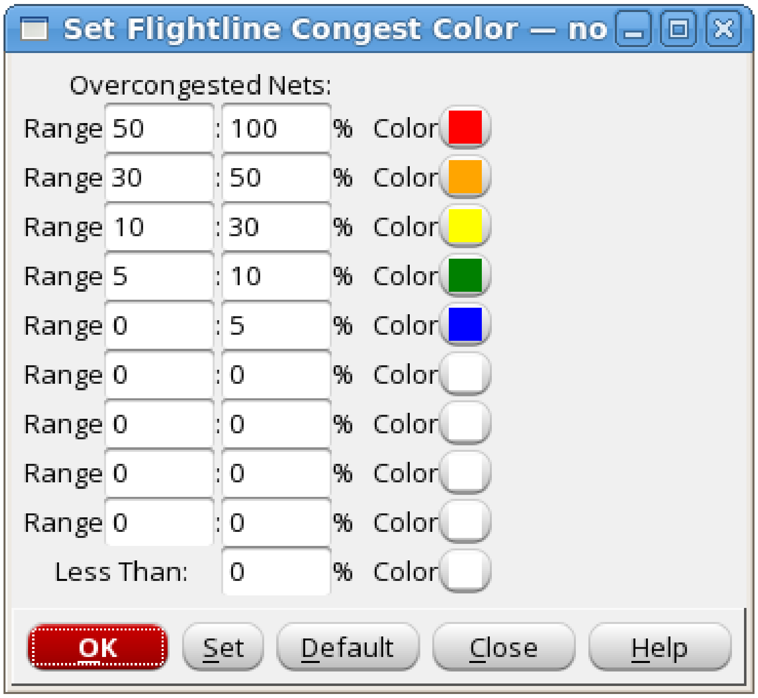
1. Click the *Color Preferences -- Objects -- Power Domain* object type to display the *Power Domain Color Selection* form.
2. Click on a power domain color to change the color.



Set Flightline Congest Color

Use the Set Flightline Congest Color form to configure flightline colors based on their congestion percentage.

- Choose *View - Set Flightline Congest Color*.



The color-coded flightlines make it easy for you to determine at a glance whether the nets from a module guide are causing congestion. You can also determine the approximate percentage of congestion from the color. By default, the flightlines are color-coded as follows:

% Overcongested Nets	Color
50-100%	Red
30-50%	Orange
10-30%	Yellow
5-10%	Green
0-5%	Blue

Set Flightline Congest Color Fields and Options

Overcongested Nets	Displays the overcongestion range and the corresponding color that is used for color-coding flightlines in the Floorplan view of the design. Click on a Color square to display the Select Color form, which enables you to choose a new color for a specific range. You can also define a new percentage congestion range by using the Range text boxes.
OK	Applies the selected colors to flightlines according to the congestion percentage and closes the form.
Set	Applies the selected colors to flightlines according to the congestion percentage without closing the form.
Default	Loads the software's default color table into the form.
Close	Closes the Set Flightline Congest Color form.

Note: To view color-coded flightlines, select the *Fightline Congest* visibility check box on the View-Only page of the Color Preferences form.

Go To

Use the Goto form to go to a specific point in the main window display. To open the Goto form:

- Select *View - Go To*.

Goto Fields and Options

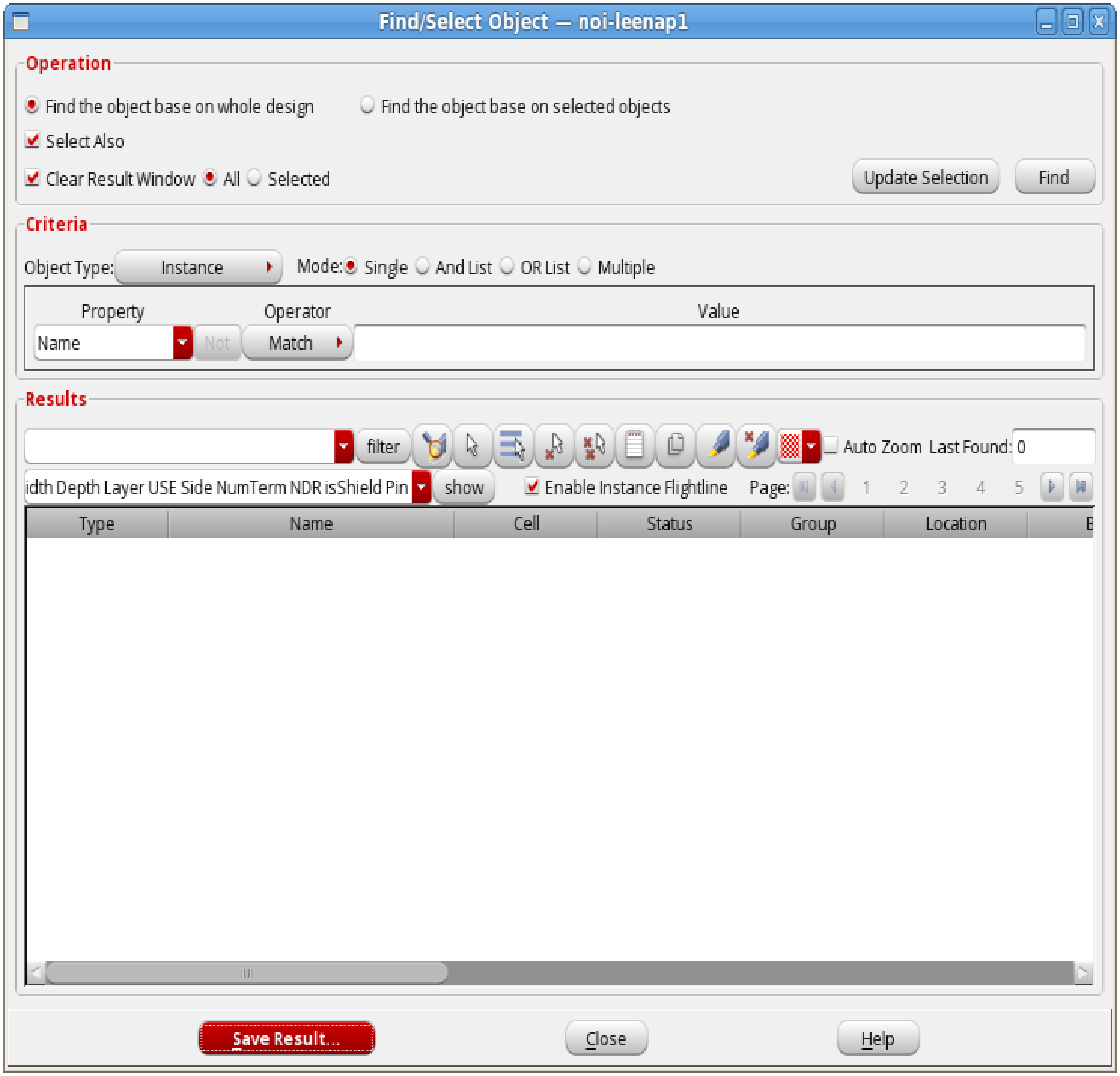
Micron units	Specifies the coordinates in micron or db units.
db units	
Add	Adds the specified coordinates to the list box below.
Goto	Zooms in to the selected location in the main window display and places a marker on the location. Click this button after selecting a coordinate from the list.
Remove	Removes the selected coordinate from the list and the corresponding marker from the main window display.
Clear All	Clears the list and removes all *Goto* markers from the main window display.
Load	Loads the coordinates from a file.
Save	Saves the coordinates in the list to a file.
Close	Closes the Goto form.

Find/Select Object

Use the Find/Select Object form to find and select specific object types in the design display area.

Note: The Select operations are recorded in the command file and the log file with the `selectObjByProp` command.

- Choose *View - Find/Select Object*.
  Or
- Press `Ctrl+F`.



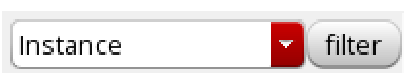
Find/Select Object Fields and Options

Operation

Find the object base on whole design	Searches for objects that match the specified criteria in the entire design and reports them in the *Results* section. This is the default operation if no objects are selected in the design display area when you open the Find/Select Object form.
Select Also	Selects the objects matching the criteria in the design display area. *Default:* This check box is turned on by default if the *Find the object base on whole design* option is selected.
Find the object base on selected objects	Searches for the required object within the selected object list, instead of the entire design. This is the default operation if you have selected objects in the design display area before opening the Find/Select Object form.
Update Selection	Dynamically updates the Objects table at the bottom of the form when you change the selection in the GUI.
Clear Result Window	Clears objects previously listed in the *Results* list, then finds the objects that meet the specified criteria and reports them in the Results list. *Default:* The objects previously listed are retained in the results window along with the results of the current search. Additionally, you can choose one of the following clear options: • *All* - Clears all objects previously listed in the *Results* list (default). • *Selected* - Clears selected entries from the *Results* list.
Find button	Finds all objects that meet the specified criteria and reports them in the *Results* window.
Criteria	

Object Type	Specifies the type of object to find. Choose from: *Instance*, *Pin, Net, Module, Instance Group*, *Bump, Wire,* or *Via*. The Pin object type pin can be used for I/O pins, partition pins, and instance pins. Names of instance pins and/or partition pins should be specified with the full path name. For example, `pin A` of instance `DTMF_CHIP/alu` should be specified as: `DTMF_CHIP/alu/A` You can use the *Net* option to find/display bus names. This option can also be used to find nets with non-default width or space.
Mode	Specifies the type of find/select operation. Select one of the following: • *Single*: Performs a simple search for a Property/Value combination. • *And List*: Performs a find/select operation that matches an AND list of two or more multiple Property/Value combinations. • *OR List*: Performs a find/select operation that matches an OR list of two or more multiple Property/Value combinations. • *Multiple*: Performs a find/select operation that matches multiple lists of Property/Value combinations; these lists can be a combination of AND lists and OR lists. For more information, see Mode Settings.

Property	Displays the available properties for the object that you selected in the Object Type field. You can use the pre-defined property Connection to find/select objects by connectivity. The Connection property supports connectivity search for the following objects: • Instance • Pin • Net • Module • Selected objects
NOT	Inverses the value of the operator in the Operator field. For example, If the value in the Operator field is <, clicking the NOT button effectively changes the value to NOT <
Operator	Specifies the relationship between the property and its value. This field is dynamically populated based on the specified object type.
Value	Specifies the value of the property. This field is dynamically populated based on the specified object type. In some cases, you may have to manually specify a value, for example, the name of a cell.
Add button	Adds the search criteria based on the values of Property, Operator, and Value fields. The search criteria are displayed in the form. This button is not available if you select the *Single* mode.
Delete button	Deletes the currently selected search criteria. This button is not available in the *Single* mode.
Update button	Updates the currently selected search criteria based on the values of Property, Operator, and Value fields. This button is not available in the *Single* mode.

Add List button	Adds a blank list to the search criteria. This button is available only in the *Multiple* mode. • If the And button is selected, an AND list is added • If the OR button is selected, an OR list is added. You can then add search criteria to the list by specifying values in the Property, Operator, and Value fields, selecting the list in the search criteria, and clicking the *Add* button. You can create a NOT AND list or a NOT OR list by selecting the *Not* button before you click the *Add List* button.
And	Specifies that the list added through the *Add List* button is an AND list. This button is available only in the *Multiple* mode.
OR	Specifies that the list added through the Add List button is an OR list. This button is available only in the *Multiple* mode.
Not	Creates a NOT AND list or a NOT OR List when the Add List button is clicked.
Results	
filter button and drop-down list 	Filters the results based on the option specified in the associated drop-down list.
Zoom in Highlight 	Zooms in the highlighted object(s). You can highlight object(s) by selecting them in the results window and clicking the *Highlight* button.
Select 	When you click *Select*, the objects selected in the Results window are selected in the design display area.
Select All 	When you click *Select All*, all the objects in the Results window are selected in the design display area.

Deselect	When you click *Deselect*, the objects selected in the Results window are deselected in the design display area.
Deselect All	When you click *Deselect All*, all the objects in the Results window are deselected in the design display area.
Select All Result of Current Page	Selects all items displayed in the current page of the Results window.
Select All Result of All Page	Selects all items displayed on all pages of the Results window.
Highlight	When you click *Highlight*, the objects selected in the Results window are highlighted in the design display area.
Dehighlight	When you click *Dehighlight*, the objects selected in the Results window are dehighlighted in the design display area.
Highlight Color	Specifies color for highlighting objects in the design display area.
Auto Zoom	Automatically zooms in to the selected object in the design display area as you browse through the search results in the Find/Select Object form. *Auto Zoom* is off by default.
Last Found	Specifies the number of objects found in the search.
show button and combo box Type Name Status Location NDR show	Displays only the object property columns specified in the combo box drop-down list. Use this button and combo box to add or remove object property columns from the Objects table. By default, all applicable columns are displayed in the Objects table. Deselect the check box for a column name in the drop-down list of the combo box and then click *show* to remove the corresponding column from the Objects table.

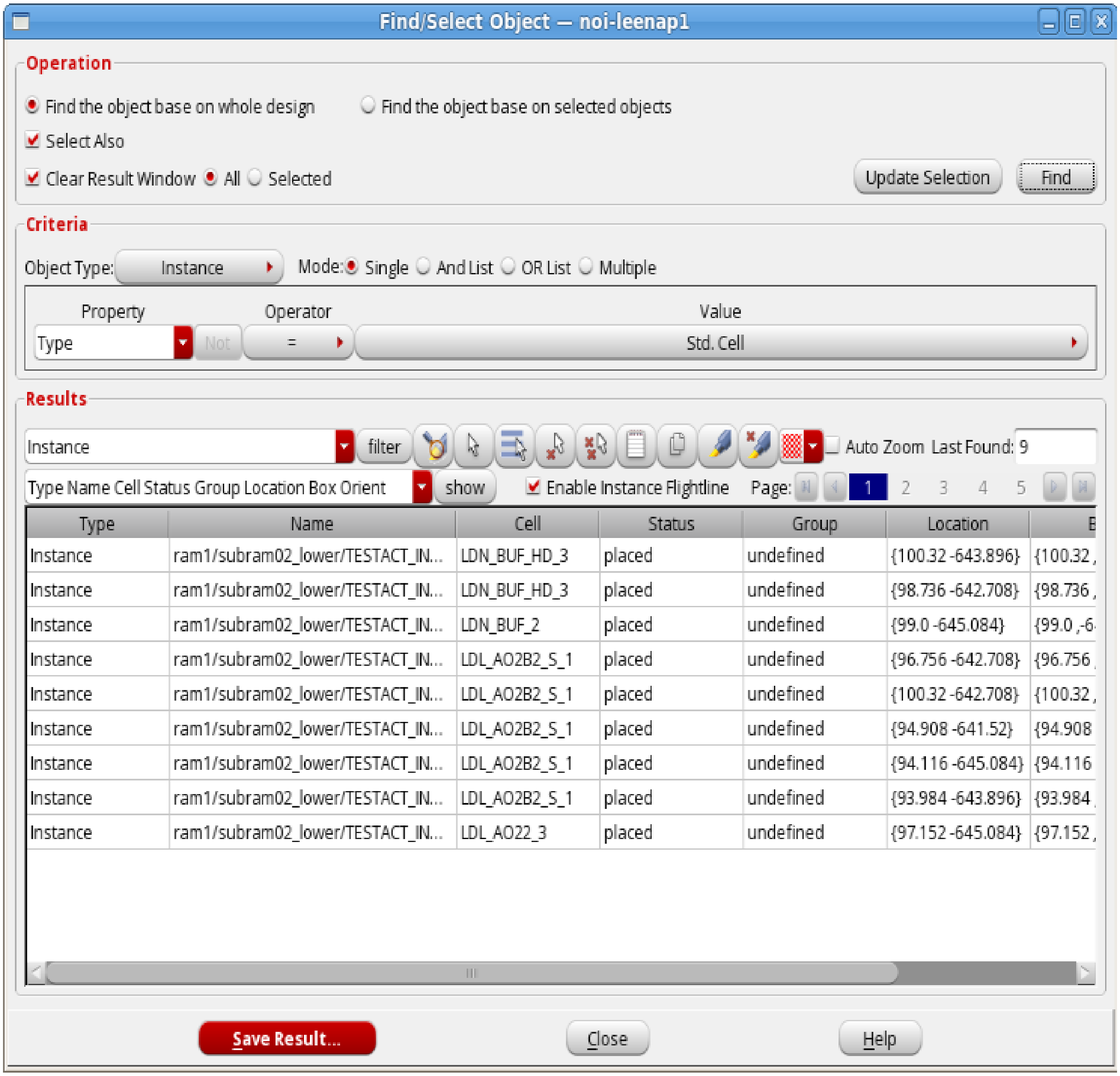
Mode Settings

The Mode field in the Find/Select Object form provides the following options:

- Single
- And List
- OR List
- Multiple

Single

Performs a simple search for a Property/Value combination. The following example illustrates the search for all instances of the type Standard Cell.



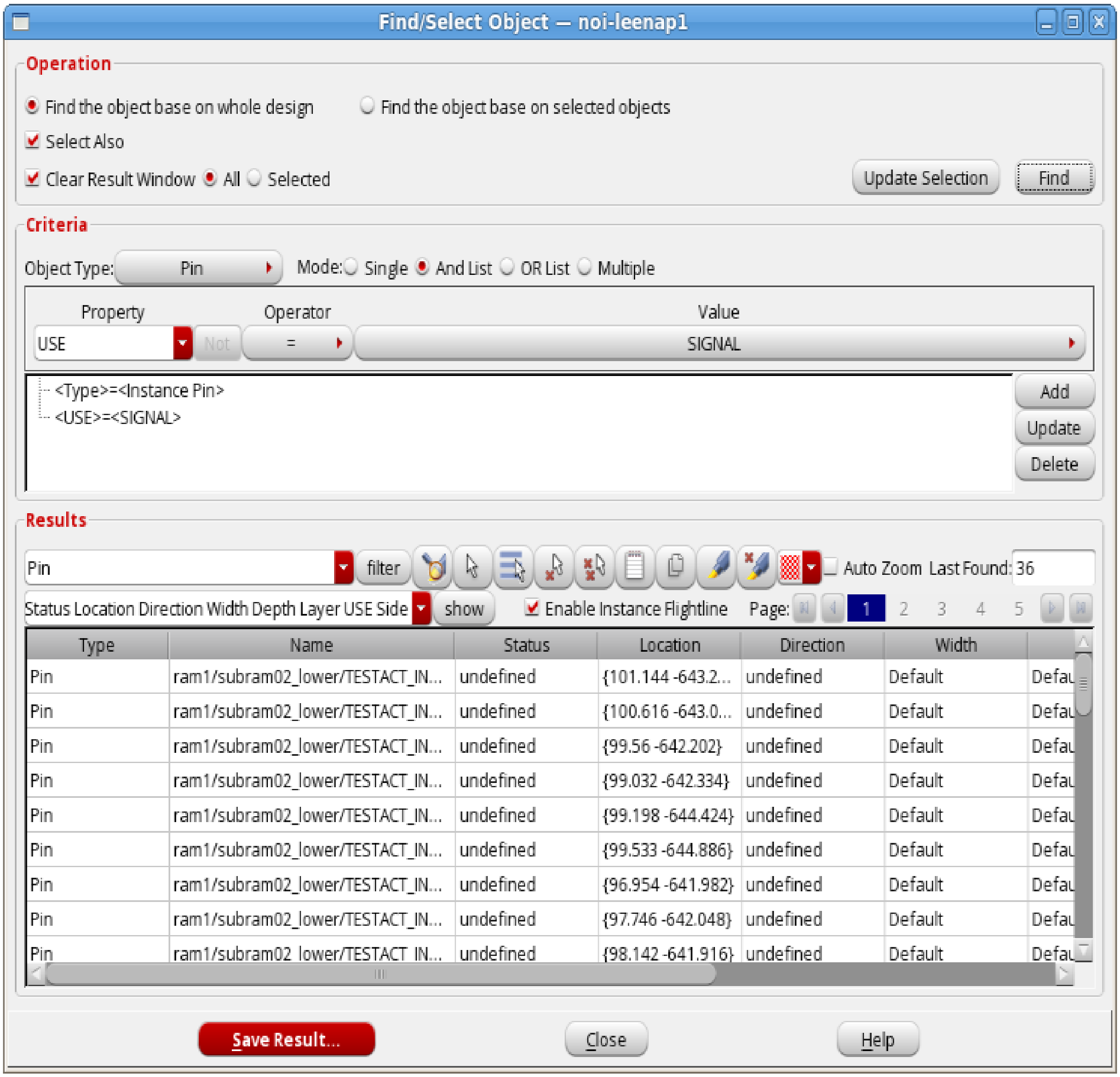
The select operation logged in this case by the `selectObjByProp` command would be:

```
selectObjByProp Instance {<Type>=<Std. Cell>}
```

And List

Performs a find/select operation that matches an AND list of two or more Property/Value combinations. The following example illustrates the search for all pins that match *all* of the following criteria:

- Type is Instance Pin
- USE is SIGNAL

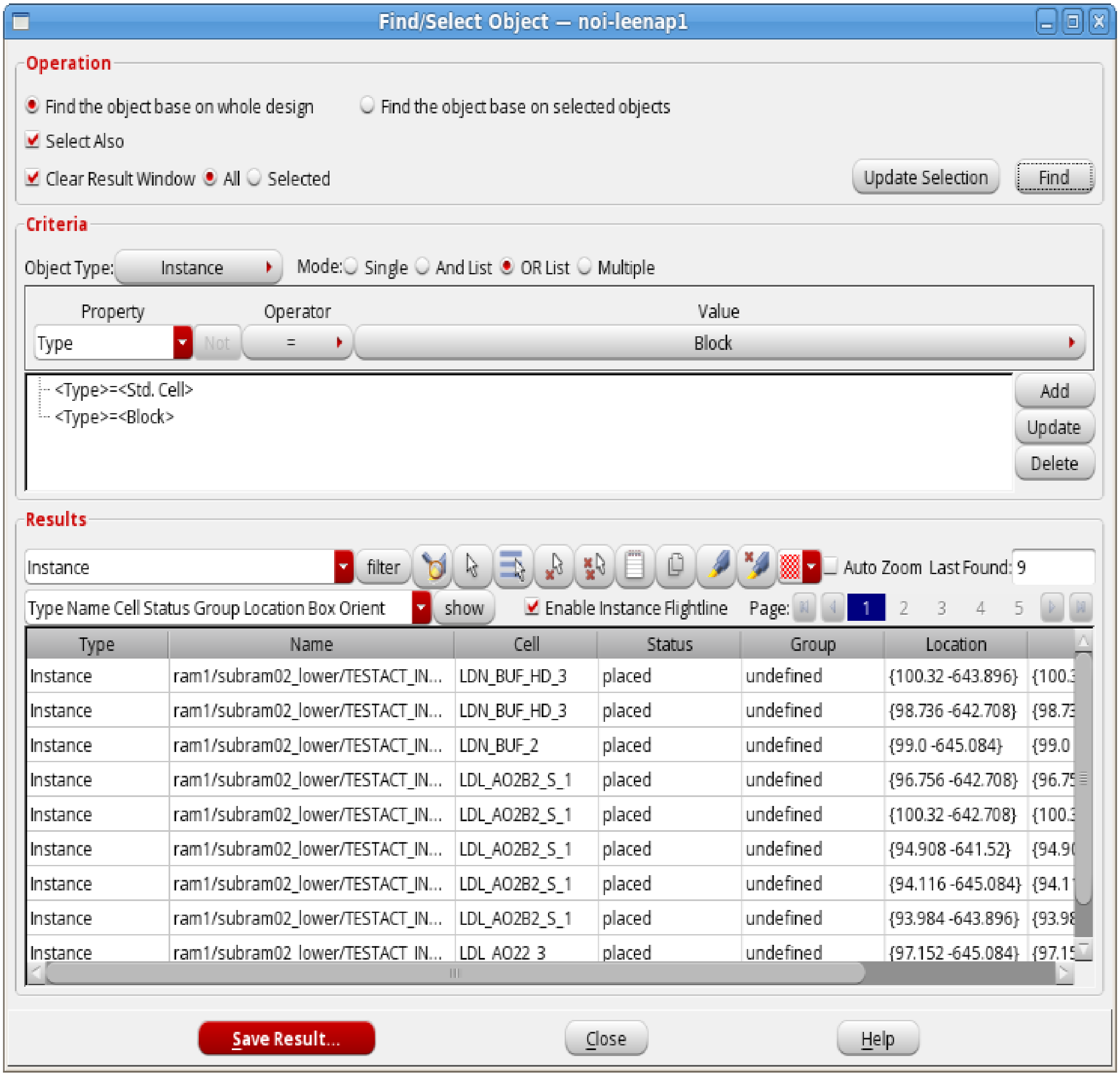


The select operation logged in this case by the `selectObjByProp` command would be:

```
selectObjByProp Pin {And(<Type>=<Instance Pin>,<USE>=<SIGNAL>)}
```

OR List

Performs a find/select operation that matches an OR list of two or more Property/Value combinations. The following example illustrates the search for all instances whose type is Block or Standard Cell.

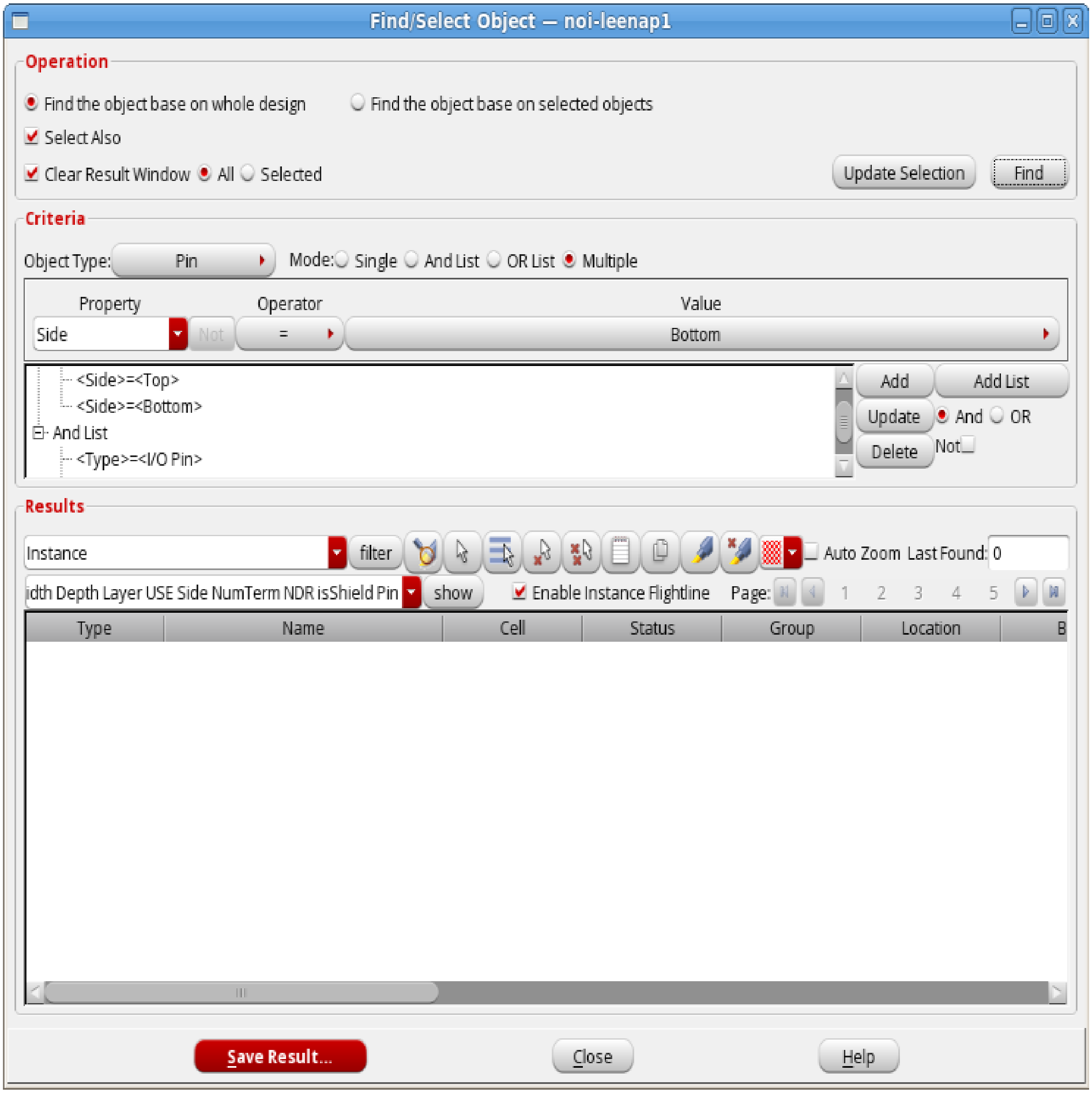


The select operation logged in this case by the `selectObjByProp` command would be:

```
selectObjByProp Instance {OR(<Type>=<Block>,<Type>=<Std. Cell>)}
```

Multiple

Performs a find/select operation that matches multiple lists of Property/Value combinations; these lists can be a combination of AND lists and OR lists. The following example illustrates the find/select operation for all I/O pins that have a status of *Placed* and are on either the *Top* or *Bottom* side.



The select operation logged in this case by the `selectObjByProp` command would be:

```
selectObjByProp Pin {OR(<Side>=<Top>,<Side>=<Bottom>),And(<Type>=<I/O Pin>,<Status>=
<Placed>)}
```

Related Text Commands

The following text command provides equivalent or additional functionality:

- `selectGroup`
- `selectInstByCellName`
- `selectInstOnNet`
- `selectIOPin`
- `selectObjByProp`

For more information, see "Floorplan Commands" in the *Text Command Reference.*

Deselect All

Use the *Deselect All* menu command to deselect all selected nets.

- Choose *View - Deselect All*.

Highlight Selected

Use the *Highlight Selected* menu command to highlight the object or object set you have selected in the design display area. You can select object sets using the Find/Select Object form.

1. Select an object or object set.
2. Click *View - Highlight Selected* and select one of the following options:
   - Select *Original* to color the selected object in original color. This option is useful if you want to check a specific net or instance more closely with the background dimmed. An object highlighted in original color will stand out in the dimmed background.
   - Select the desired highlight set. The default number of highlight colors is 64.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `highlight`
- `deselectGroup`
- `deselectInstByCellName`
- `deselectInstOnNet`
- `deselectIOPin`
- `selectGroup`
- `selectInstByCellName`
- `selectInstOnNet`
- `selectIOPin`

Clear Highlight

Use the *Clear Highlight* submenu to clear highlights.

- Choose *View* - *Clear Highlight* and select one of the following options:
  - *Clear Original* - Clears all original highlights.
  - *Clear All*--Clears all highlights from the design display area.
  - *Clear Selected*--Clears highlight from the object selected in the design display area.
  - *Clear Set #<n>*--Clears the highlight set you choose. For example, if you select *Clear Set #2*, highlight is cleared from all objects that were highlighted with Highlight Set #2.

Note: The clear highlight options are also available from the context menu, which you can open by right-clicking an object in the design display area.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `deselectGroup`

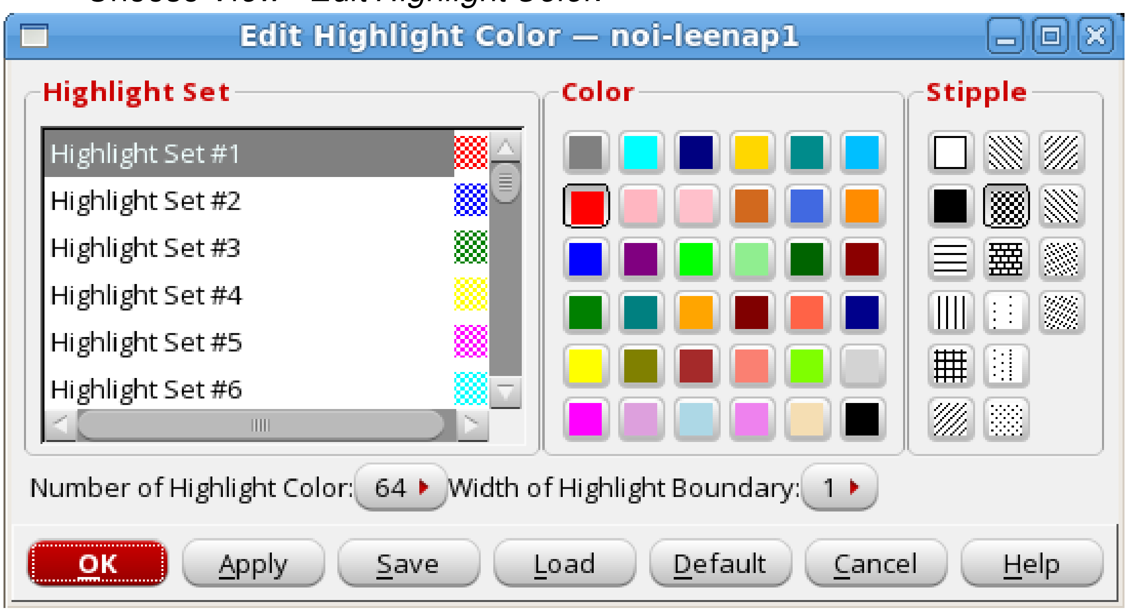
- `deselectInstByCellName`
- `deselectInstOnNet`
- `deselectIOPin`
- `selectGroup`
- `selectInstByCellName`
- `selectInstOnNet`
- `selectIOPin`

For more information, see "Floorplan Commands" in the *Text Command Reference.*

Edit Highlight Color

Use the Edit Highlight Color form to further customize the highlight color and pattern of selected object sets in the design display area.

- Choose *View - Edit Highlight Color*.



Edit Highlight Color Fields and Options

Highlight Set	Lists the available highlight sets. To customize a highlight set: • Select the set. • Choose the appropriate highlight color and pattern from the *Color* and *Stipple* area, respectively. • Click *Apply*.
Color	Specifies the highlight color for the selected highlight set.
Stipple	Specifies the highlight pattern for the selected set.
Number of Highlight Color	Specifies the number of highlight colors available. You can set the value as 64, 128, or 256. *Default*: 64
Width of Highlight Boundary	Specifies the width of highlight boundary. You can set the number as 1, 2, 3, 4, or 5. *Default*: 1
Save	Saves the highlight settings. The default filename is enc.hilite.tcl.
Load	Loads highlight settings previously saved in a file.
Default	Reverts to the default settings for all highlight sets.

Related Text Commands

- `highlight`

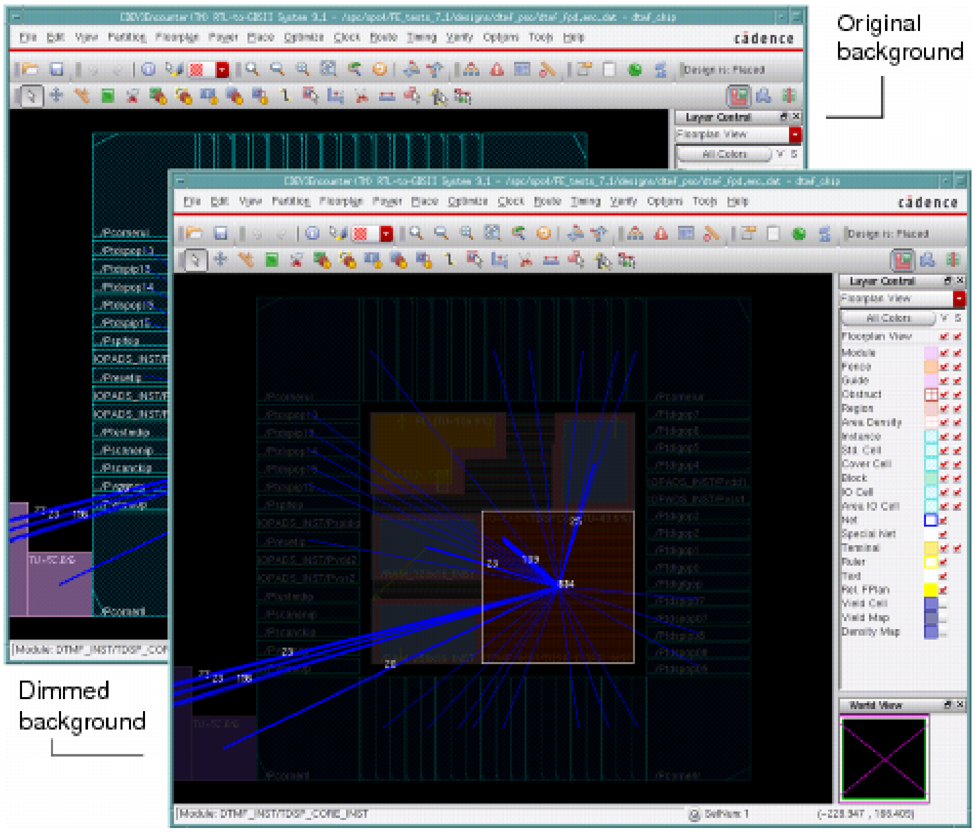
Dim Background

Use the *View - Dim Background* menu command to dim the background of the Innovus display. This enhancement helps you view selected and highlighted objects more clearly. This is especially useful when you are debugging.

To enable the dim mode:

- Select the View - Dim Background menu command.

The equivalent bindkey is `F12`. The `F12` key is used as a three-way toggle; so if you want to quit dim mode, press the `F12` key again twice.



Related Text Commands

- gui_dim_foreground

4

Edit Menu

- Snap
- Stretch
- Add Via
- Replace Via
- Add Polygon

- Create Non Default Rule

Undo

Use the *Edit-Undo* menu command to undo the previous action. You can only undo a single action. You can undo specific wire editor actions, any power planning action, bump creation and deletion, and the following floorplanning actions:

- Align Object
- Shift Object
- Space Object
- Flip/Rotate Object
- Snap Floorplan

The equivalent bindkey is `u`.

Related Text Command

The following text command provides equivalent or additional functionality:

- `undo`

Redo

Use the *Edit-Redo* menu command to restore the design to the same state as before you clicked the *Undo* button. You can only redo a single undo action. You can redo specific wire editor actions, any power planning action, bump creation and deletion, and the following floorplanning actions:

- Align Object

- Shift Object
- Space Object
- Flip/Rotate Object
- Snap Floorplan
- Resize Floorplan

The equivalent bindkey is `Shift+U`.

Related Text Command

The following text command provides equivalent or additional functionality:

- `redo`

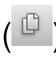
Copy

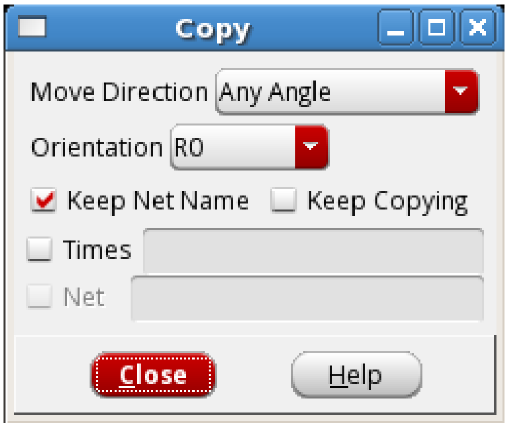
Use the Copy form to copy and paste the following objects:

- Physical cells
- Regular, special, and patch wires
- Vias
- Routing blockages:
  - Layer routing blockages
  - Cut routing blockages
  - Trim routing blockages
  - DRC regions
  - Partial routing blockages
- Placement blockages:
  - Hard placement blockages
  - Partial placement blockages

- Soft placement blockages
- Macro only placement blockages

To access the Copy form:

- Select the *Edit - Copy* menu command.
  Or
- Click the *Copy* widget () on the toolbar.



Copy Fields and Options

Move Direction	Specifies the direction in which you can move the object copy. Choose one of the following options from the drop-down list: • *Any Angle* (default) • *Diagonal* • *Orthogonal* • *Horizontal* • *Vertical*
Orientation	Specifies the orientation of object copy after pasting. Use this option to rotate the selected wire or via during copy/paste.
Keep Net Name	Specifies that the net name from the original object should be retained for its copies. *Default*: On **Note** - If a copied via touches an existing wire at the location where it is pasted and the *Keep Net Name* check box is not selected and no net is specified in the *Net* field, the copied via will inherit the net name of the existing wire at the paste location.
Keep Copying	Allows repetitive copy of the same selected object. *Default*: Off
Times	Specifies the number of times the object is to be copied. *Default* : Off
Net	Specifies the net name that should be assigned to the object copy. Choose the required net from the associated drop-down. *Default* : Off

Related Topics

- `editCopy`
- `copyObject`

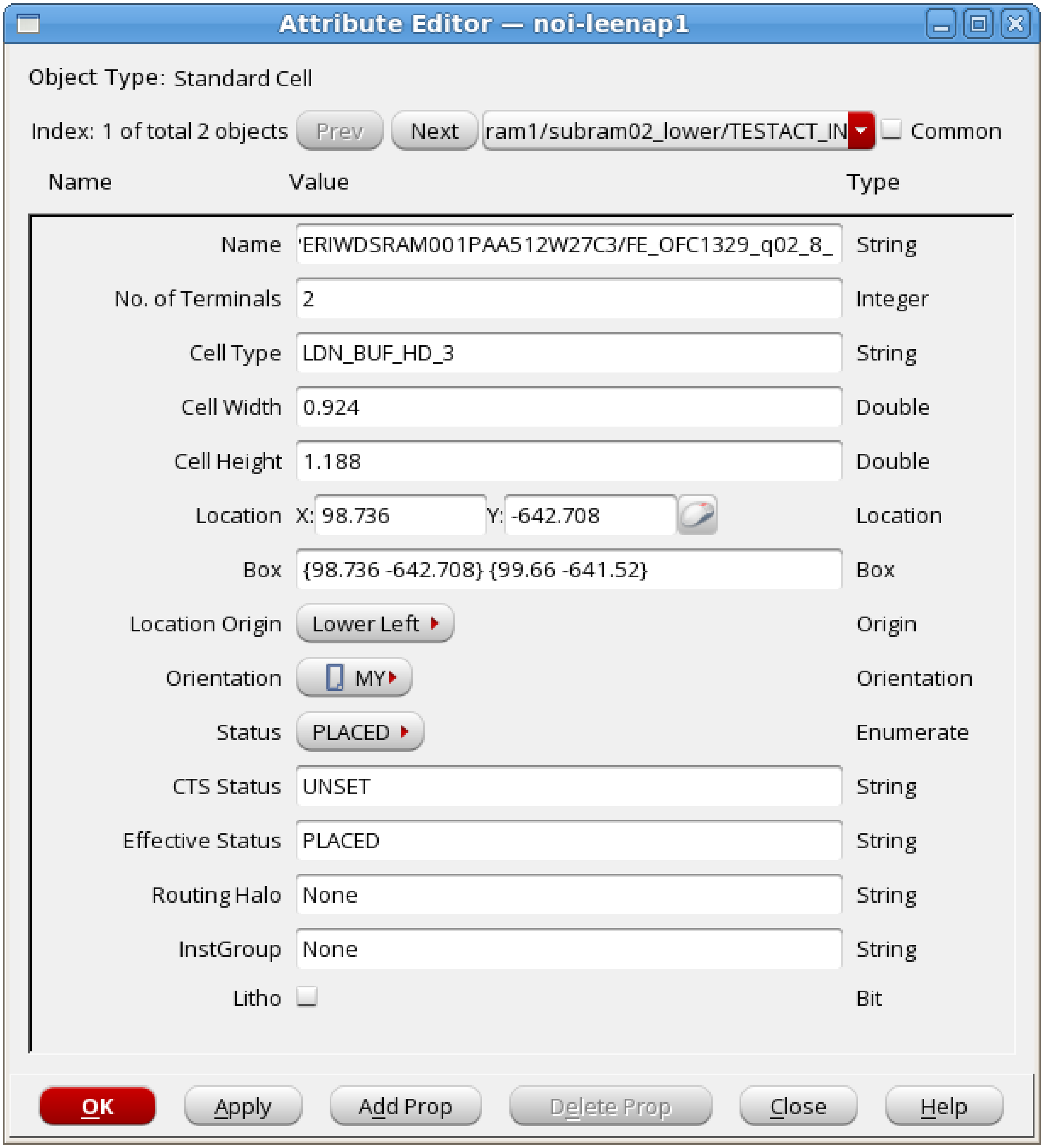
- `pasteObject`
- *Copying Wires* section in the Editing Wires chapter of the *User Guide*

Attribute Editor

Use the Attribute Editor to display an object's type, name, and attributes. The Attribute Editor displays different attributes, depending on the objects selected in the main window.

Note: For Special Route objects, you can select layer, shape, and status from the pull-down menu in the Attribute Editor.

Note: For Bump Cell objects, you can select the placement status from the pull-down menu.



There are several ways to open the Attribute Editor.

To open the Attribute Editor from the menu bar, do the following:

- Click on an object and then select *Edit-Attribute Editor* widget.

To open the Attribute Editor from the design display window, do the following:

- For a single object, double-left click on an object, or left click on the object to highlight it and click the *Attribute Editor* widget. When you change the selection by clicking on another object, the Attribute Editor is automatically updated to display the attributes of the newly selected object.
- For multiple objects, left click on the objects to highlight and click the *Attribute Editor* widget.

To open the Attribute Editor from the Violation Browser:

1. Click the *Attribute Editor* button in the Violation Browser.
2. Double-click a violation in the Violation Browser.

To open the Attribute Editor from the Design Browser, do the following:

1. Choose *Tools* - *Design Browser*, or left click the *Design Browser* widget on the toolbar.
2. In the Design Browser, highlight or left click on an object or a set of objects.
3. Click the *Attribute Editor* from the Design Browser tool widgets.

Attribute Editor Fields and Options

Object Type	Specifies the type of object currently selected.
Index	Indicates the object's number in the sequence, such as `1 of total 34 objects`, if you have selected more than one object before opening Attribute Editor. Use the drop-down menu to view attributes of a specific object from the list of selected objects. **Note:** This field is available only when multiple objects are selected in the main window.
Next and *Prev*	Click *Next* to display the attributes of the next object in the sequence or *Prev* to view the previous object. **Note:** These buttons are available only when multiple objects are selected in the main window.

Common	Enables you to make the same change to a common attribute of multiple objects. When you select the *Common* check box, only changeable attributes are active and other fields are grayed out (non-editable). **Note:** This check box is available only when multiple objects are selected in the main window. *Default*: Unchecked
AS IS	If the selected objects have different values for a changeable field (eg. *Module Width*), the field has an *AS IS* check box to its right. Deselect the *AS IS* check box if you want to apply a change in the associated field to all selected objects. **Note:** This check box is available only when multiple objects are selected in the main window and the *Common* check box is selected in Attribute Editor. *Default*: Checked
OK	Applies your changes to the selected objects and closes the window.
Apply	Applies your changes to the selected object. If multiple objects are selected, applies the change to the object whose attributes are currently displayed in Attribute Editor. **Note:** This button is available either when only a single object is selected in the main window or when multiple objects are selected but the *Common* check box is not selected.
Apply All	Applies changes to all the selected multiple objects. **Note:** When selecting objects of different types, only the objects with the same attribute selections are affected. **Note:** This button is available only when multiple objects are selected in the main window and the *Common* check box is selected in Attribute Editor.
Add Prop	Allows you to add a property name and value. If the new property is DEF-supported, it is written out to a DEF file.
Delete Prop	Allows you to delete a property name and value.
Close	Closes the Attribute Editor window.

DB Browser

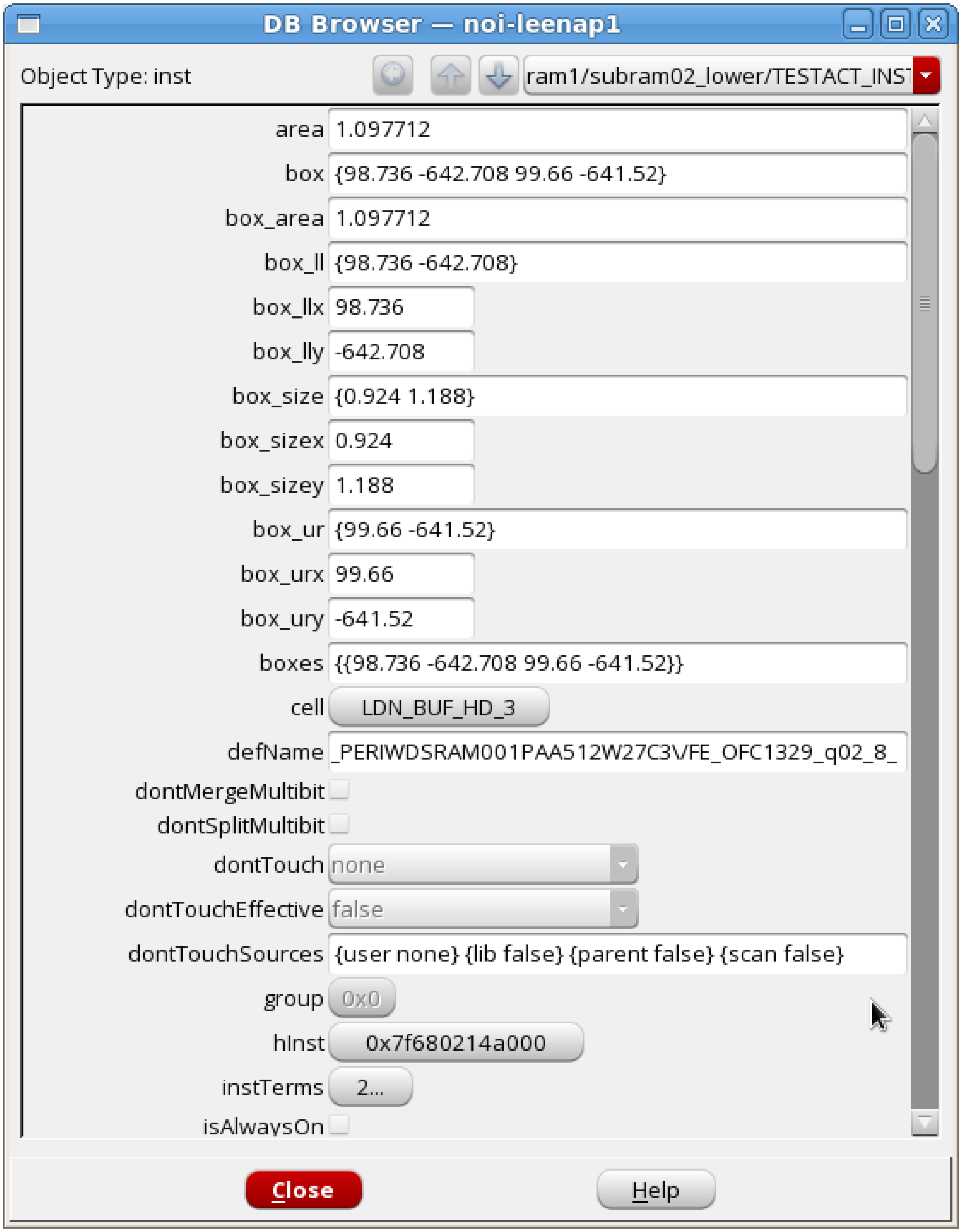
You can use the database browser (DB Browser) to retrieve the selected object's attributes. This browser is the GUI equivalent to the `dbGet .selected.??` command. The DB Browser displays different attributes, depending on the objects selected in the main window.

To launch the database browser:

1. Select one or more objects in the main window.
2. Press the bindkey `v`.

Or

- Select *Edit - DB Browser*.


DB Browser — noi-leenap1
Object Type: inst
ram1/subram02_lower/TESTACT_INST
area 1.097712
box {98.736 -642.708 99.66 -641.52}
box_area 1.097712
box_ll {98.736 -642.708}
box_llx 98.736
box_lly -642.708
box_size {0.924 1.188}
box_sizex 0.924
box_sizey 1.188
box_ur {99.66 -641.52}
box_urx 99.66
box_ury -641.52
boxes {{98.736 -642.708 99.66 -641.52}}
cell LDN_BUF_HD_3
defName _PERIWDSRAM001PAA512W27C3VFE_OFC1329_q02_8_
dontMergeMultibit
dontSplitMultibit
dontTouch none
dontTouchEffective false
dontTouchSources {user none} {lib false} {parent false} {scan false}
group 0x0
hInst 0x7f680214a000
instTerms 2...
isAlwaysOn
Close
Help

DB Browser Fields and Options

Object Type	Specifies the type of object currently selected.
	Click the *Show next object in list* button to display the attributes of the next object in the sequence. or *Prev* to view the previous object. **Note:** This button is available only when multiple objects are selected in the main window.
	Click the *Show last object in list* button to display the attributes of the previous object in the sequence. **Note:** These buttons are available only when multiple objects are selected in the main window.
	Click the *Back to previous object* button to return to the first object in the list. For example, if you select two instances `i1` and `i2`. Use the *Show next object in list* button to move from `i1` to `i2` as the active instance, then decend to the `i2`'s cell. Now if you select *Back to previous object* button, you return to `i1`.
Close	Closes the DB Browser.

Related Topics

- `dbGet`

Move/Resize/Reshape

Use the *Edit - Move/Resize/Reshape* menu command to move, resize, or reshape an object.

- ## Moving Objects

  Click the *Move/Resize/Reshape* menu command, then click a floorplan object or I/O pad and click on a new location. Use the *Shift* key to select multiple objects to move.

- ## Resizing and Reshaping Objects

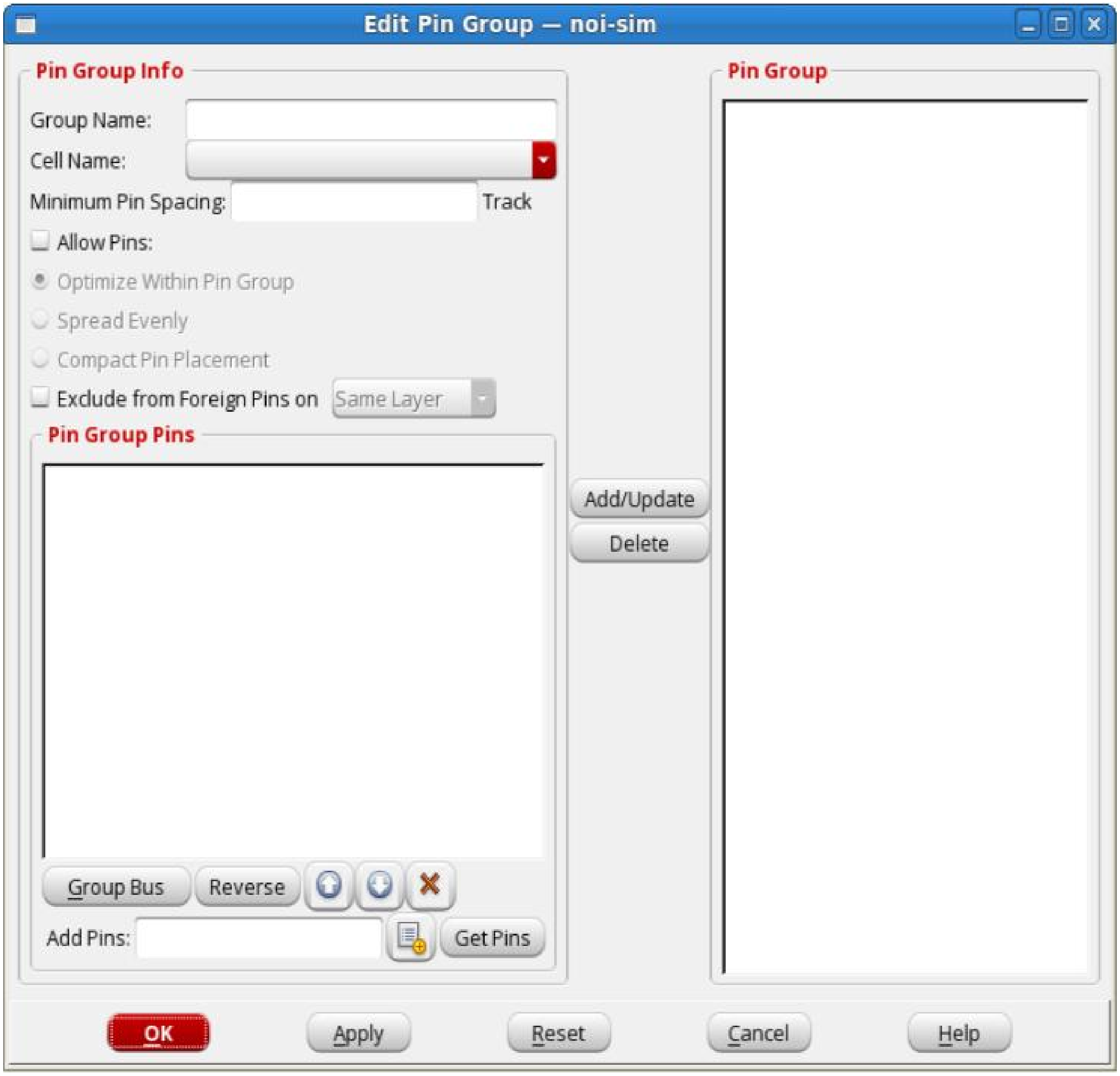
Move the mouse to the side or corner of a floorplan object and click and hold to resize and reshape. You can also move or resize rectilinear edges with the *Move/Resize/Reshape* menu command.

Edit Pin Group

Use the Edit Pin Group form to create a new pin group, add or delete pins to an existing pin group, delete all or specific pin groups, list all pins of the specified partition or block-level design, and change pin orders within a pin group.

You can use this form in conjunction with the Pin Editor.

- Choose *Edit* - *Edit Pin Group*.



Edit Pin Group Fields and Options

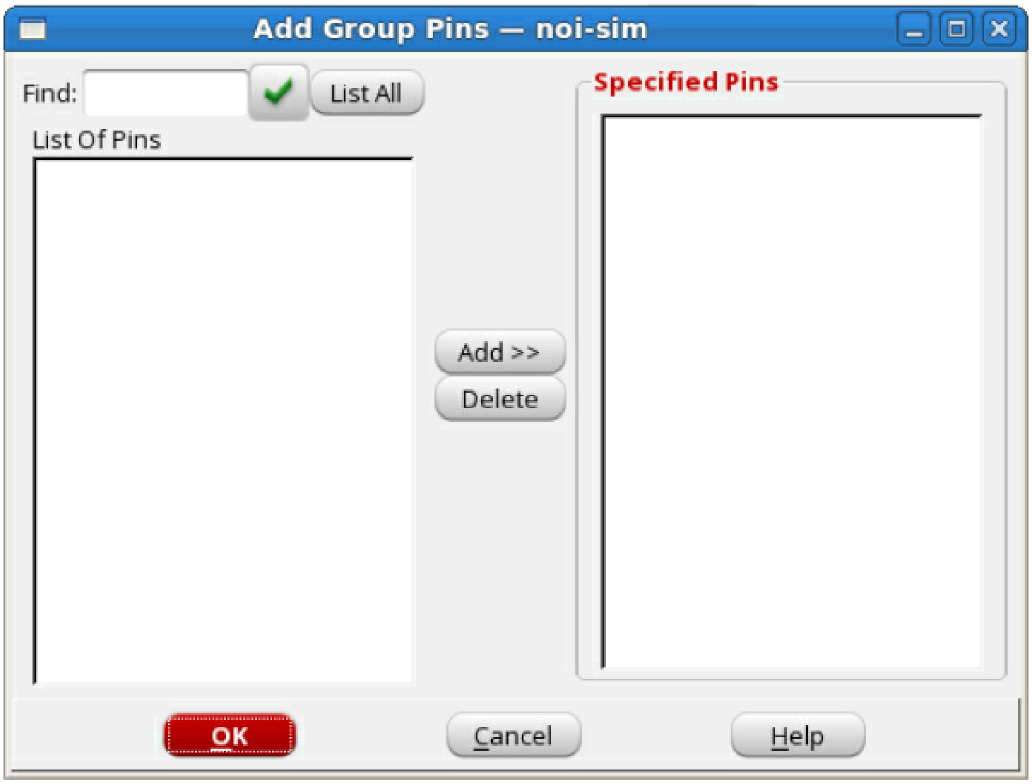
Group Name	Specify an existing or new pin group name in the field, specify a partition in the *Cell Name* field, and click the *Add/Update* button to add it to the *Pin Group* list.
Cell Name	Specify the partition name to associate with the pin group.
Minimum Pin Spacing	Specify the minimum spacing between the members of the net group.

Allow Pins	Use this option to enable options for grouping pins
Optimize Within Pin Group	Specifies that pins in the group are reordered to optimize wire length. If this option is not selected, the pin order is exactly as specified in the pin group.
Spread Evenly	Specifies that pins in the group must be distributed evenly.
Compact Pin Placement	Specifies that pins in the specified pin group are assigned tightly together.
Exclude from Foreign Pins on	Specifies that pins in the group must exclude foreign pins on *All Layers* or the *Same Layer*.
Pin Group Pins	Lists the pin names in the pin group. To add a pin to the list, use the *Add Pins* field. To delete pins, highlight them in the list and click the X button.
Group/Expand Bus	The Group Bus option specifies that all bus bits should be displayed as one bus in the *Pin Group Pins* list. The Expand Bus option specifies that all bus bits should be displayed individually in the *Pin Group Pins* list. Consider a bus named `A` that contains the bits `A1`, `A2`, `A3`, and `A4`. The *Group Bus* option displays them as one bus, bus `A`, in the Pin Group Pins list. The *Expand Bus* option displays them as individual bus bits `A1`, `A2`, `A3`, and `A4`, in the *Pin Group Pins* list.
Reverse	Reverses the order in which the pins are listed in the *Pin Group Pins* list.
Add Pins	Specify the name of the pin(s) and click the check button to include it in the *Pin Group Pins* list. You can use the wildcard (*) character to select a set. To select from a list of the available nets, click the Get Pins button.
Pin Group List	Displays all pin groups. Highlighting a group adds the name to the left side of the form where you can display and edit the group. To delete pin groups, highlight them in the list and click the Delete button.

Add Group Pins

Use the Add Group Pins form to add nets from a list of available pins.

- In the Edit Pin Group form, click the *Get Pins* button.



Add Group Pin Fields and Options

Find	Type the name of pin to find. You can specify wildcard (*) with pin names. To start the search, click the check icon next to the Find field or press Enter.
List All	Lists all available pins.
List of Pins	Displays the available pins.
Add	Adds the pins selected in the List of Pins window to the Specified Pins window. The pins listed in the Specified Pins window are added to the Edit Pin Group form when you click OK.
Delete	Deletes the pins selected in Specified Pins window.

Related Text Commands

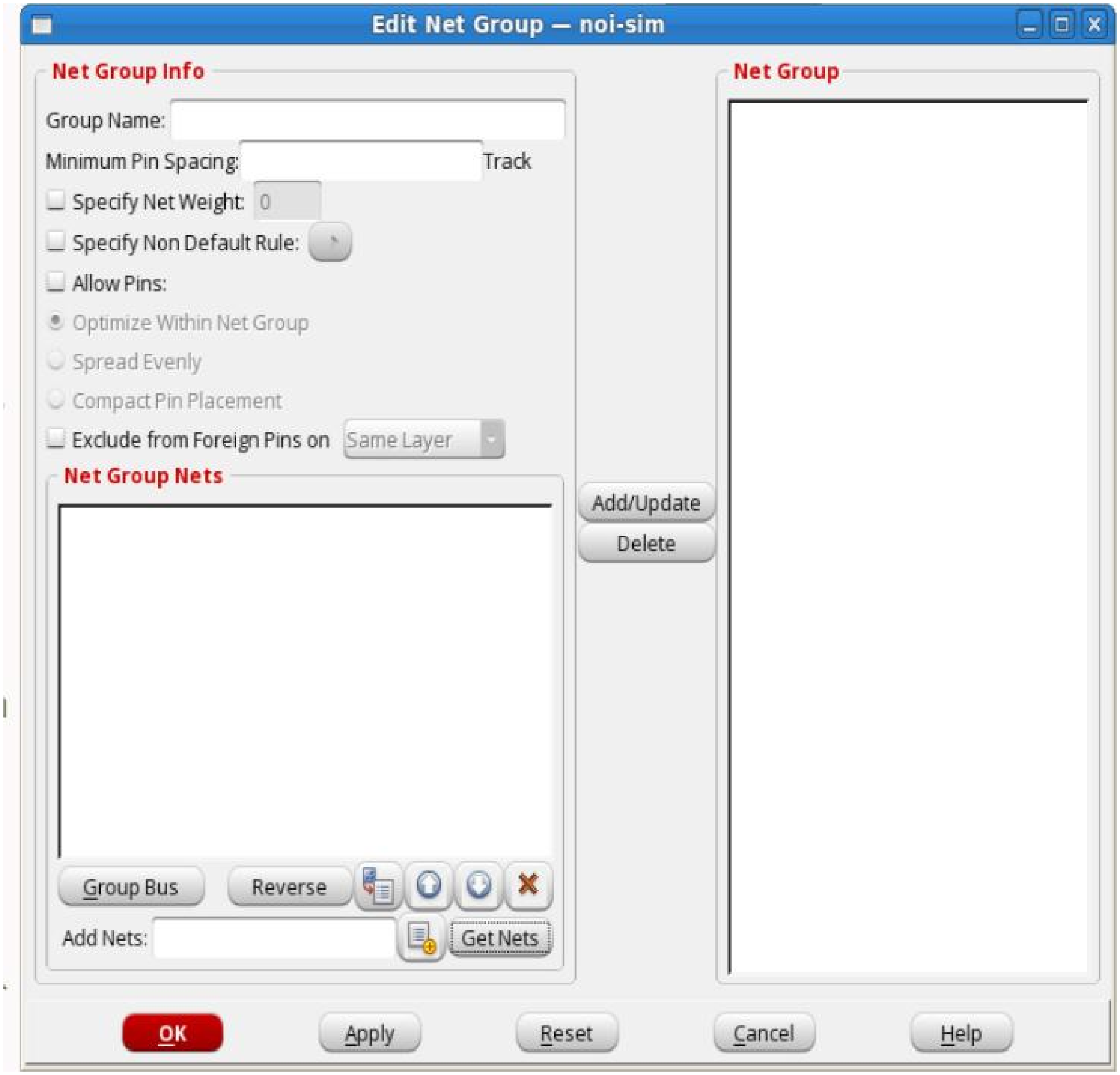
The following text commands provide equivalent or additional functionality:

- `addPinToPinGroup`
- `createPinGroup`
- `deletePinGroup`

Edit Net Group

Use the Edit Net Group form to create a new net group, add or delete nets to an existing net group, delete all or specific net groups, select nets based on a list of all the nets that connect to a specified partition or block-level design, and change net orders within a net group.

- Choose *Edit - Edit Net Group*.



Edit Net Group Fields and Options

Group Name	Specify an existing or new net group name in the field and click the Add/Update button to add it to the Net Group list.
Minimum Pin Spacing	Specify the minimum spacing between the members of the net group.

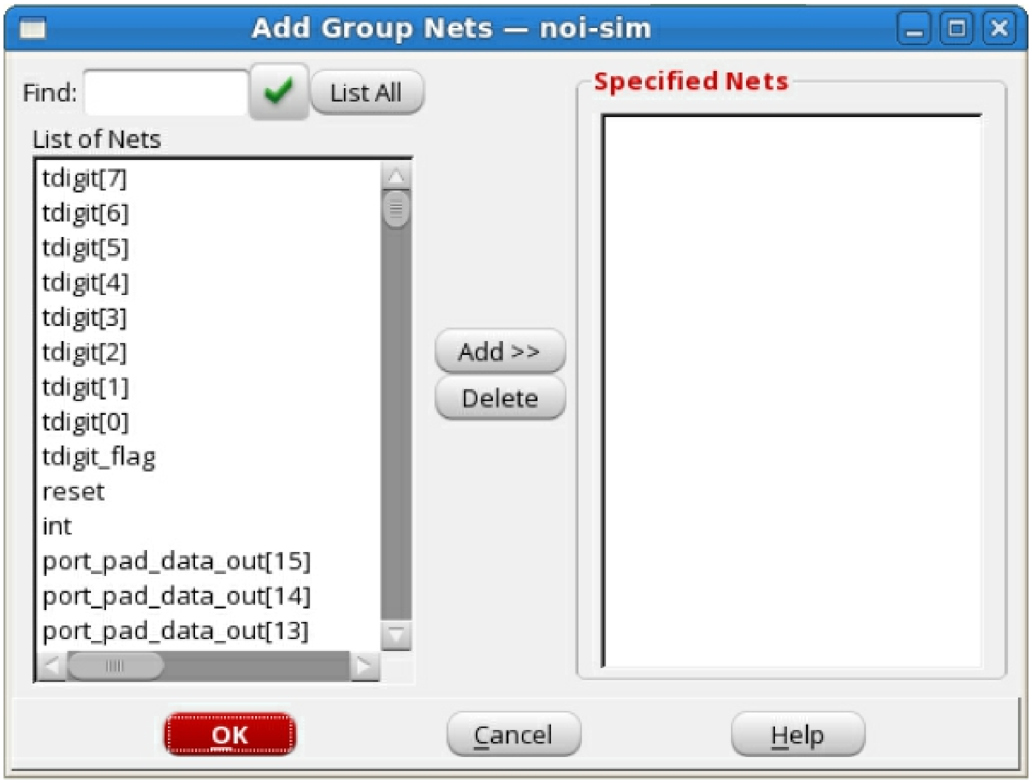
Specify Net Weight	Specifies the weighting priorities of the net, with values ranging between 512 (highest) through 1(lowest) or 0 (don't care). Cadence recommends using a value between 1 and 10. *Default*: The default value is 0.
Specify Non Default Rule	Specifies that the selected non-default rule should be applied to the nets. The drop-down menu next to the option lists the available non-default rules. For information on creating a non-default rule, see Add Polygon.
Allow Pins	Use this option to enable options for grouping pins
Optimize Within Net Group	Use this option to specify that pins in the group should be reordered to optimize wire length. *Default*: Off. The pin order is exactly as specified in the pin group.
Spread Evenly	Specifies that pins in the group must be distributed evenly.
Compact Pin Placement	Specifies that pins in the specified net group are assigned tightly together.
Exclude from Foreign Pins on	Specifies that pins in the group must exclude foreign pins on *All Layers* or the *Same Layer*.
Net Group Nets	Lists the net names in the net group. To add a net to the list, use the *Add Nets* field. To delete nets, highlight them in the list and click the X button.
Group/Expand Bus	The Group Bus option specifies that all bus bits should be displayed as one bus in the *Net Group Nets* list. The Expand Bus option specifies that all bus bits should be displayed individually in the *Net Group Nets* list. Consider a bus named `A` that contains the bits `A1`, `A2`, `A3`, and `A4`. The *Group Bus* option displays them as one bus, bus `A`, in the *Net Group Nets* list. The *Expand Bus* option displays them as individual bus bits `A1`, `A2`, `A3`, and `A4`, in the *Net Group Nets* list.
Reverse	Reverses the order in which the pins are listed in the *Net Group Pins* list.

Get Selected Nets 	Specifies that the nets selected in the main window should be displayed in the *Net Group Nets* list.
Move Up 	Moves up by one position the net currently selected in the *Net Group Nets* list.
Move Down 	Moves down by one position the net currently selected in the *Net Group Nets* list.
Delete 	Specifies that the net currently selected in the *Net Group Nets* list should be removed from the list. **Note:** The net is not actually deleted; it is only removed from the *Net Group Nets* list.
Add Nets 	Specify the name of the net(s) and click the *Add Nets* icon to include it in the *Net Group Nets* list. You can use the wildcard (*) character to select a set. To select from a list of the available nets, click the *Get Nets* button. For more information, see Add Group Nets.
Net Group	Displays all net groups. Highlighting a group adds the name to the left side of the form where you can display and edit the group. To delete net groups, highlight them in the list and click the *Delete* button.

Add Group Nets

Use the Add Group Nets form to add nets from a list of available nets.

- In the Edit Net Group form, click the *Get Nets* button.



Add Group Net Fields and Options

Find	Type the name of net to find. You can specify wildcard (*) with net names. To start the search, click the check icon next to the Find field or press Enter.
List All	Lists all available nets.
List of Nets	Displays the available nets.
Add	Adds the nets selected in the List of Nets window to the Specified Nets window. The nets listed in the Specified Nets window are added to the Edit Net Group form when you click OK.
Delete	Deletes the nets selected in Specified Nets window.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `createNetGroup`
- `addNetToNetGroup`

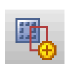
Edit Pin Guide

Use the Edit Pin Guide menu command to create or edit a pin guide object using the *Edit Pin Guide* form. The pin guide restricts the pins associated with the pin guide within the specified area.

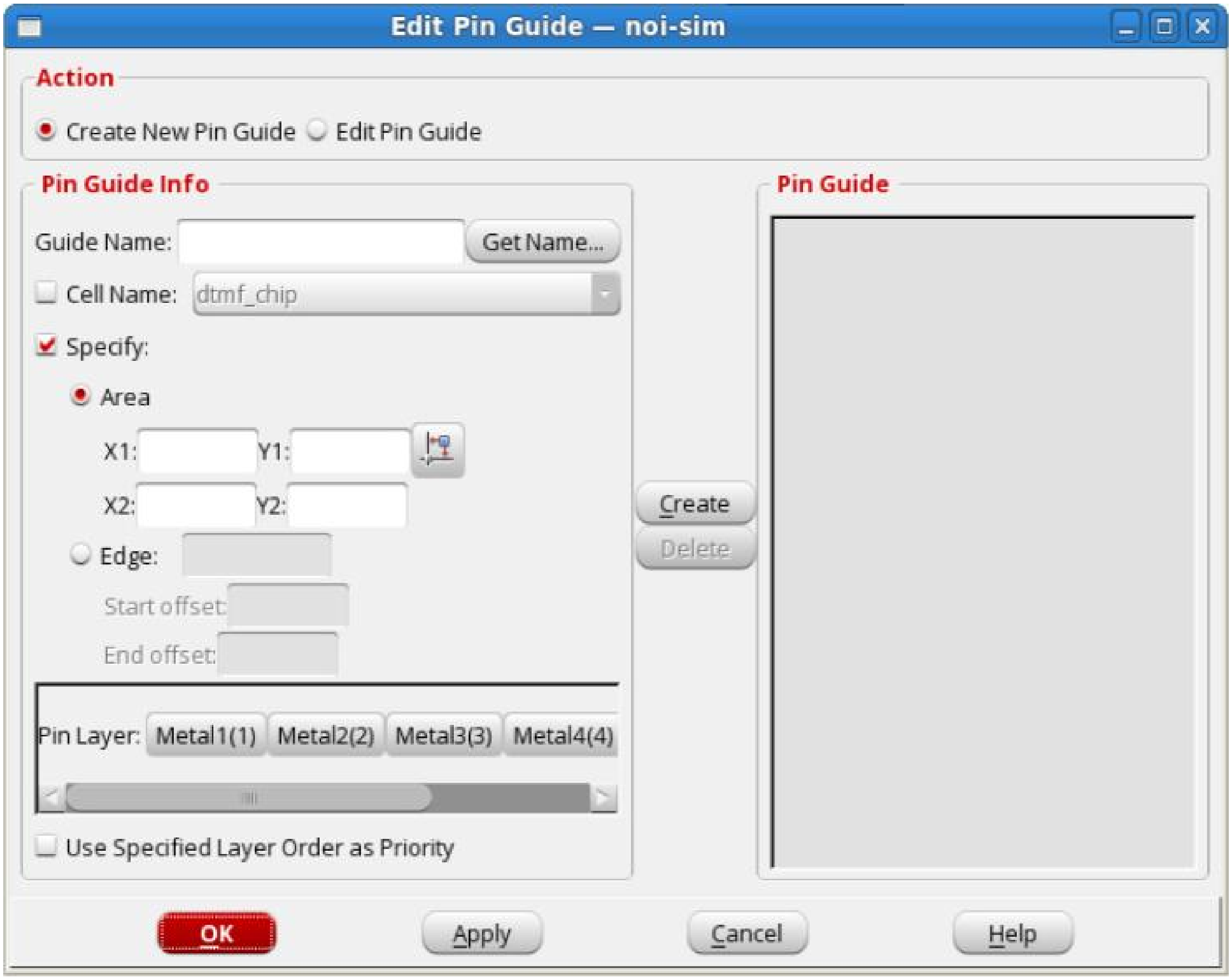
To open the *Edit Pin Guide* form:

- Choose Edit - Edit Pin Guide.

Or

- Click the *Create Pin Guide*  icon in the toolbox and then press the `F3` key.

Specify pin guide preferences in this form and then drag the mouse over an area that overlaps a partition fence or top cell to create a port for a net or bus.


Edit Pin Guide — noi-sim
Action
Create New Pin Guide
Edit Pin Guide
Pin Guide Info
Guide Name:
Get Name...
Cell Name:
dtmf_chip
Specify:
Area
X1:
Y1:
X2:
Y2:
Edge:
Start offset:
End offset:
Pin Layer:
Metal1(1)
Metal2(2)
Metal3(3)
Metal4(4)
Use Specified Layer Order as Priority
Create
Delete
Pin Guide
OK
Apply
Cancel
Help

Edit Pin Guide Options - Fields and Options

Create New Pin Guide	Enables options to create a new pin guide.
Edit Pin Guide	Enables options to edit an existing pin guide.
Guide Name	Specifies the name of the partition pin guide object.
Get Name	Displays the *Get Name* form using which you can select the object type and the corresponding name of the object.
Cell Name	Specifies the name of the cell. This parameter is not required if you are using the command for a top-level module.
Specify	Specifies the mode for defining the physical location of pin guide. The physical location constraint can be specified either *By Area* or *By Edge*.
Area	*X1, Y1, X2*, and *Y2* specify the coordinates of the pin guide area.
Draw	Draws the pin guide area.
Edge	Specifies the integer value where edge numbering starts from lower-left corner of a partition clock-wise. Edge `0` is the edge that has the smallest y value.
Start offset	Specifies the distance, in microns, from the starting corner of the edge.
End offset	Specifies the distance, in microns, from the ending corner of the edge.
Pin Layer	Specifies the metal layer(s) for the pin guide. *Default*: If you do not specify the layer number, pin guides are created only on the preferred layers.
Use Specified Layer Order as Priority	Assign pins based on layer order that the user specified for optimized pin/net group.

Related Text Command

The following text command provides equivalent or additional functionality:

- `createPinGuide`

Related Topics

For more information, see the Partitioning the Design chapter in the *Innovus User Guide*.

Bus Guide

The Edit - Bus Guide menu provides the following options:

- Edit
- Color
- Clear Color

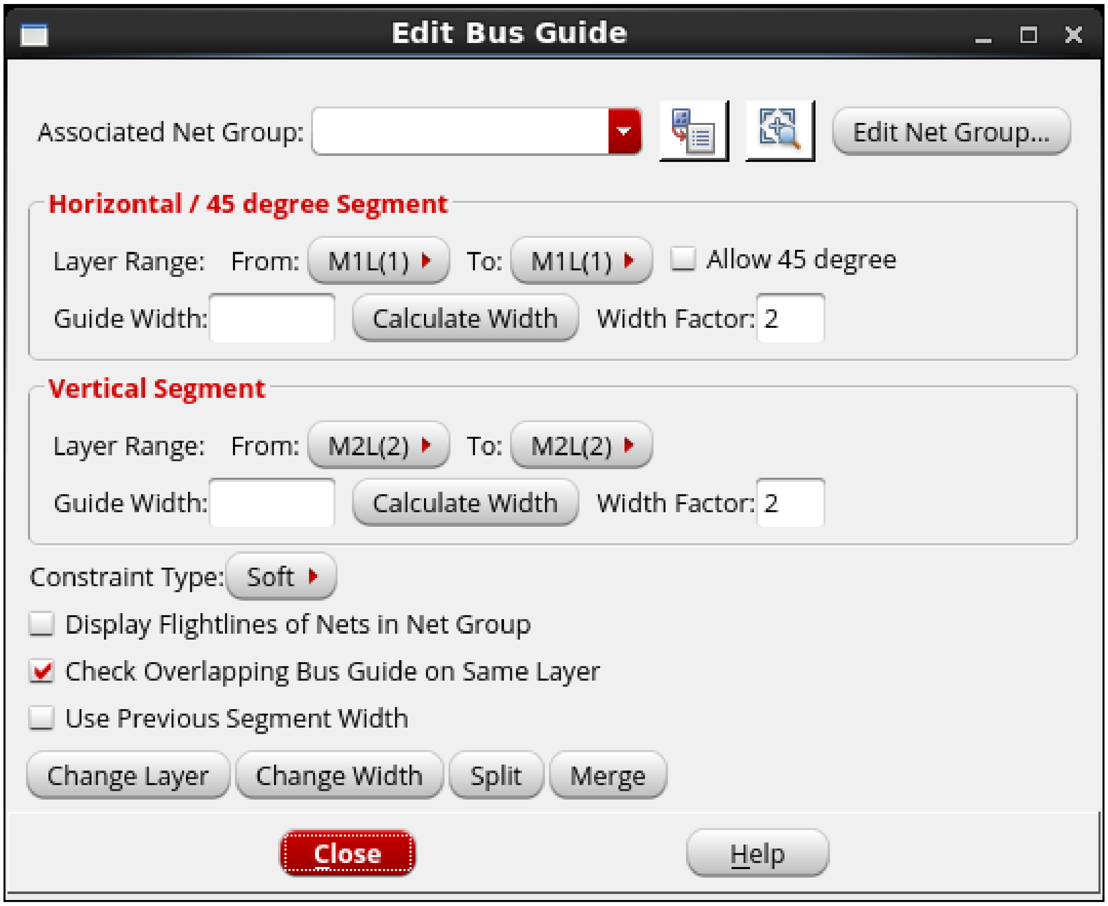
Edit

Use the Edit Bus Guide form to create a new bus guide, associated with an existing net group.

- Choose *Edit - Bus Guide - Edit*.

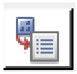
or

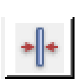
- Click the *Edit Bus Guide*  icon on the tool bar and press the `F3` key.

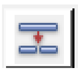
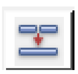


Edit Bus Guide Fields and Options

Associated Net Group	Specifies the net group name of the bus guide you are creating. This is an editable drop-down list, which lists all net groups by default. You can either select the required net group from the list or type the name of the net group in the box. As you start typing the name of the net group, the drop-down list changes to show only the net group names that match the pattern. **Note:** Innovus displays a warning message if the net group you specify is already assigned to an existing bus guide.

Get Selected button 	Gets the name of the net group associated with the bus guide segment selected in the main window. This button is useful for cross-probing. Select a bus guide segment in the main window and then click the *Get Selected* button. The drop-down list jumps to the net group of the selected bus guide segment. **Note:** If multiple bus guides are selected, *Get Selected* does not work.
Zoom Selected button 	Zooms to the bus guide of the net group selected in the *Associated Net Group* drop-down list. This button is useful for cross-probing. Select a net group from the *Associated Net Group* drop-down list and then click the *Zoom Selected* button. On the floorplan, the view window will zoom to fit the bus guide of the net group. **Note:** If the selected net group does not have a bus guide drawn on the floorplan, *Zoom Selected* does not work.
Edit Net Group	Launches the Edit Net Group form.
Layer Range	Specifies the layer constraint for horizontal, 45-degree, and vertical bus guide segments. To specify a single layer constraint specify the same value in the \`From' and \`To' fields.
Allow 45 degree	Allows the creation of 45-degree bus guide segments. 45-degree bus guides are required for flip chip routing.
Guide Width	Specifies the bus guide width, in microns, of the current editing bus guide segment. You can specify different widths for horizontal/45-degree and vertical segments. If you don't specify the width value, the bus guide editor uses the automatically calculated width value.
Calculate Width	Automatically calculates the default bus width of the specified net group, based on the number of nets in the net group, number of nets per micron across layers in the preferred routing direction, and the width factor.
Width Factor	Specifies a width factor value that is used to calculate the default guide width; The default value of the width factor is the spacing value of the associated net group.

Constraint Type	Specifies the constraint type of the bus guide: • *Hard* - After running Early Global Route (eGR), NanoRoute (NR), or NanoRoute High Frequency Router (NRHF), the route obeys the path of the bus guide. • *Soft* - After running eGR, NR, or NRHF, the bus guide only guides the route path. The tool can route the net out of the bus guide.
Display Flightlines of Nets in Net Group	Displays flightlines of nets when you create the bus guide.
Check Overlapping Bus Guide On Same Layer	Enables the overlapping check for bus guides that are on the same layer.
Use Previous Segment Width	Uses the width of the previous bus guide segment for the new segment you are adding.
Change Layer of Selected Guide Segments button 	Changes the layer of the selected bus guide segment.
Change Width of Selected Guide Segments button 	Changes the width of the selected bus guide segment.

Split Selected Bus Guides button 	Splits the selected bus guide. The equivalent bindkey combination is `Ctrl+S`.
Merge Selected Bus Guides button 	Merges the selected bus guides. The equivalent bindkey combination is `Shift+M`.

Related Text Commands

- createBusGuide

For more information, see "Bus Plan Commands" chapter in the *Text Command Reference*.

Related Topics

- Using the Edit Bus Guide GUI in the Bus Planning chapter of the *Innovus User Guide*.

Color

Use the *Color* item on the *Edit -- Bus Guide* menu to highlight bus guides with multiple preset colors.

- Choose *Edit -- Bus Guide -- Color.*

The order of highlighting colors repeat for the next set of bus guides.

Note: This menu command does not have an associated GUI form.

To specify multiple colors for bus guide objects, or, to change the preset colors, use the *Bus Guide Color Selection* form. For more information, see Bus Guide Color Selection in the View Menu chapter.

Related Topics

- "Highlighting and Dehighlighting the Bus Guide" in the Bus Planning chapter of the *Innovus User Guide*.

Related Text Commands

- `setBusGuideMultiColors`
- `resetBusGuideMultiColors`

Clear Color

Use the *Clear Color* item on the *Edit -- Bus Guide* menu to clear the highlighted bus guide colors.

- Choose *Edit -- Bus Guide -- Clear Color.*

Note: This menu command does not have an associated GUI form.

Related Topics

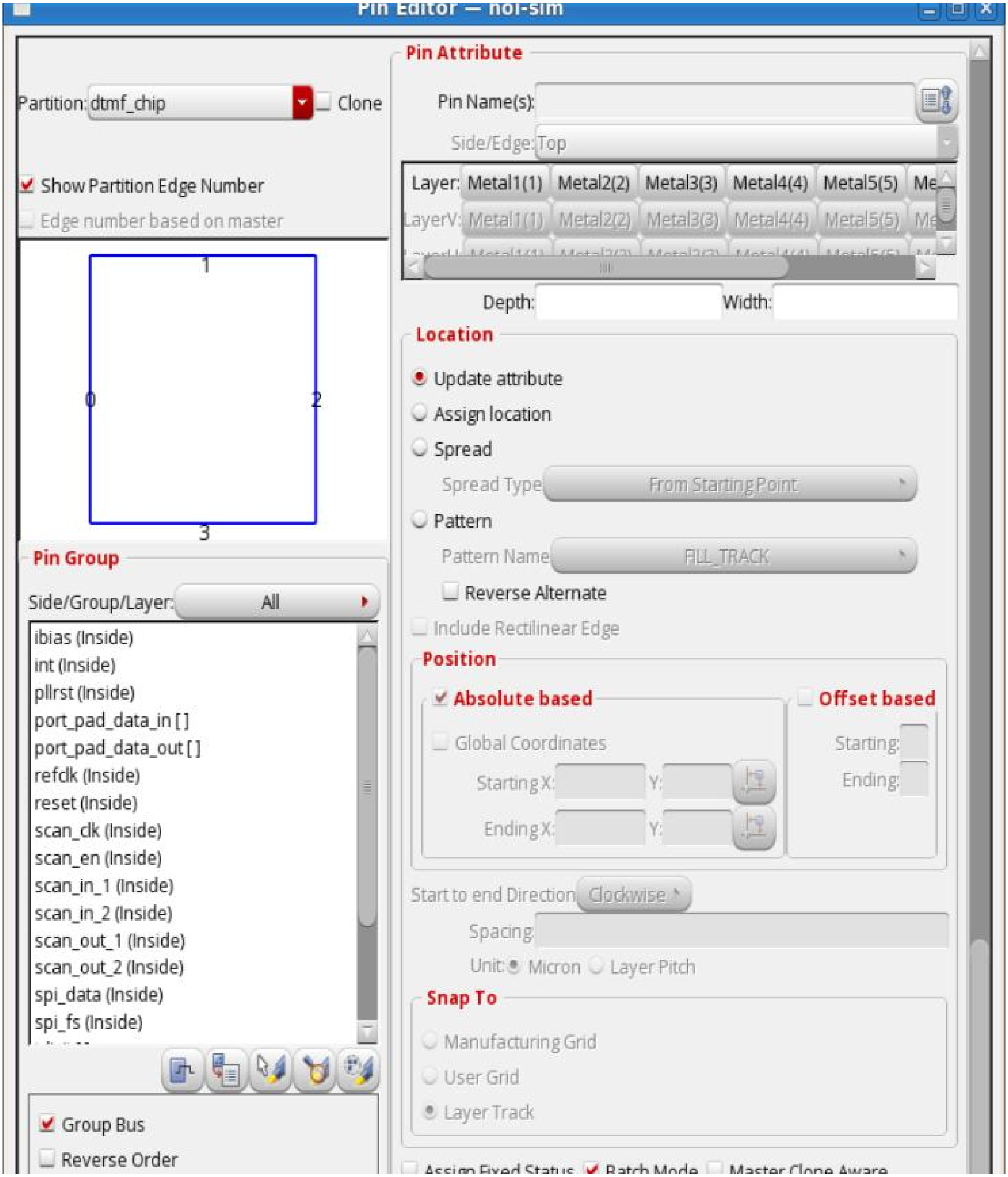
- "Highlighting and Dehighlighting the Bus Guide" in the Bus Planning chapter of the *Innovus User Guide*.

Related Text Commands

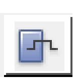
- `setBusGuideMultiColors`
- `resetBusGuideMultiColors`

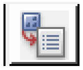
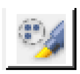
Pin Editor

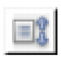
Use the Pin Editor to display and edit pin and pin groups.
→Choose *Edit - Pin Editor*.


Pin Editor — noi-sim
Pin Attribute
Partition: dtmf_chip
Clone
Pin Name(s):
Side/Edge: Top
Show Partition Edge Number
Edge number based on master
Layer: Metal1(1) Metal2(2) Metal3(3) Metal4(4) Metal5(5)
LayerV: Metal1(1) Metal2(2) Metal3(3) Metal4(4) Metal5(5)
Depth:
Width:
Location
Update attribute
Assign location
Spread
Spread Type
From Starting Point
Pattern
Pattern Name
FILL_TRACK
Reverse Alternate
Include Rectilinear Edge
Pin Group
Side/Group/Layer:
All
ibias (Inside)
int (Inside)
pllrst (Inside)
port_pad_data_in [ ]
port_pad_data_out [ ]
refclk (Inside)
reset (Inside)
scan_clk (Inside)
scan_en (Inside)
scan_in_1 (Inside)
scan_in_2 (Inside)
scan_out_1 (Inside)
scan_out_2 (Inside)
spi_data (Inside)
spi_fs (Inside)
Position
Absolute based
Offset based
Global Coordinates
Starting X:
Y:
Ending X:
Y:
Starting:
Ending:
Start to end Direction
Clockwise
Spacing
Unit: Micron Layer Pitch
Snap To
Manufacturing Grid
User Grid
Layer Track
Group Bus
Reverse Order
Assign Fixed Status
Batch Mode
Master Clone Aware

Pin Editor Fields and Options

Partition	Specifies the partition name to display the pin group for all the pins in a partition, and the cell name (module name) of the currently specified partition. Pins are grouped alphabetically if they are unassigned.
Clone	If selected, you can work on master as well as clone partitions.
Show Partition Edge Number	Displays the partition boundary shape in a window along with the edge numbers for the partition . The edge numbering starts from lower-left corner of a partition clock-wise. Edge 0 is the edge that has the smallest y value.
Edge number based on master	Specifies that the clone's edge number, spreadDirection, and offset based on its master.
Side/Group/Layer	Displays pins by side, group, or layer. For the pin group list, you can select a side or group criteria of *Top*, *Bottom*, *Left*, *Right*, *Inside*, *Unassigned*, *All*, or Other. *Inside*: The group of pins that are assigned but not on boundary. *Other*: The pins that you bring in from the artwork window by clicking the Get Selected Pin icon.
Pin Group	The *Pin Group* panel provides the following widgets and options:
	*Timing Budget Info.*--Displays timing budgeting justification information for the highlighted pins, if timing information is available.

	*Get Selected Pin*--In the *Pin Group* panel, lists pins that you have selected in the design display area.
	*Select Highlighted in Display*--In the design display area, selects the pins that you have highlighted in the *Pin Group* panel.
	*Zoom in Highlighted in Display*--In the design display area, zooms in on the pins that you have highlighted in the *Pin Group* panel.
	*Group Highlighted*--Creates a temporary subgroup list of the original pin group.
Group Bus	Groups bus bits with their respective pins for ease in reordering the pin list.
Reverse Order	Reverses the pin ordering in the pin list.
Sort by	Sorts according to one of the following options: *Name*: Sorts in alphabetical order. *Location*: Sorts left to right, and bottom to top.
Find Pins	Searches for pins by name. You can use the asterisk (*) as a wildcard character for this field. Click the *Update* icon, or press `Return` to start the search.
Update 	Updates the list of pins after the Find operation.
Append Pin(s) to Pin Name List	

	Allows you to add multiple pins to the *Pin Name(s)* list. You can select multiple pins in the Pin Group list by clicking SHIFT + pin name (contiguous selection) or CTRL + pin name (non-contiguous selection). These pins are added to the pin name list. If the Append Pin(s) to Pin Name List option is selected, any new pins that you select from the Pin Group will be appended to the pin name list. If this option is off, any new pins that you select from the Pin Group will replace the previous list of pins.
Pin Name(s)	Displays the pin or pin group names as selected from the pin group list. Click the widget to the right of the field.  This opens the Pin Editing List form. For more information, see Reorder Pin List.
Side/Edge	Displays the side. For rectilinear partitions, also displays the edges. Use the pull-down menu to assign a side or an edge. You can select *Top*, *Bottom*, *Left*, *Right*, *Inside*, or *Unassigned* for side, or the edge number for a particular edge.
Layer	Displays the layer names. Select the layers on which the pins will be assigned. Click the *Prioritize* button to display the *Layer Priority* form using which you can set the priority of the in input layer.
LayerV	Select the preferred vertical layer on which the pins will be assigned Click the *Prioritize* button to display the *Layer Priority* form using which you can set the priority of the in input layer.
LayerH	Select the preferred horizontal layer on which the pins will be assigned. Click the *Prioritize* button to display the *Layer Priority* form using which you can set the priority of the in input layer.
Depth	Displays the depth of the edited pin in microns. *Default*: If no value is specified, the minimum area depth is taken by default as the pin depth.
Width	Displays the width of the edited pin in microns.

Update attribute	Updates the attributes of the pin.	
Assign location	Preassigns a pin at the specified location.	
Spread	Defines how to position pins along a block's edge. Use the pull down menu to choose one of the following options:	
	From Starting Point	Uses the coordinates of the first pin in the *Pin Name* list as the starting point (anchor) for spreading a group of pins.
	From Center	Spreads pins beginning at the starting x and y coordinates of the center of the block's edge or side.
	Along Entire Edge	If you had selected an Edge in the Side/Edge option, the pins are spread evenly along the entire specified edge, using the limits of the edge as the starting and ending points. If you had selected a side in the Side/Edge option, the pins are spread evenly along all the edges belonging to the specified side. The pins are spread from left to right and from top to bottom. The Pin Editor determines the appropriate spacing.
	Between Points	Spreads pins evenly along the block edge between points you specify with *Starting X/Y* and *Ending X/Y*. The ending coordinates become the coordinates of the last pin in the pin group. The Pin Editor determines the appropriate spacing. For rectilinear partitions, if the start and/or end points are not on the specified side, the start and/or end points are snapped to the nearest correct location on the specified side.

Pattern	Specifies the multi-layer-spread-pattern must be followed by the set of selected pins. Use the pull down menu to choose one of the following options: • FILL_TRACK • FILL_LAYER • FILL_OPTIMISED • FILL_DIAGONAL • FILL_SINUSOIDAL • FILL_CHECKERBOARD	
Reverse Alternate	Specifies that the reverse of the multi-layer-spread-pattern must be followed by the set of selected pins.	
Include Rectilinear Edge	Specifies that all the edges coming in the solution space should be included.	
Absolute based	Specifies actual start/end coordinates.	
	Global Coordinates	Specifies that all the locations are global.
	Starting X/Y	Specifies the x and y starting location. Use the mouse widget to get the coordinates from the design display area.
	Ending X/Y	Specifies the x and y ending location. Use the mouse widget to get the coordinates from the design display area.
Offset based	Specifies start/end offsets for editing pins instead of providing actual start/end coordinates. It supports an offset from a vertex/corner which is derived based on the specified edge information and spread direction.	
	Starting	Sets the offset from the start of edge (in microns) to be considered as start point for placing the pin.
	Ending	Sets the offset from the end of edge (in microns) to be considered as end point for placing the pin.

Start to end Direction	Specifies the direction in which the pins are spread. Use the pull down menu to choose the direction. Select clockwise option to set the pins in the clockwise direction and the counterclockwiseoption to set the pins in the counter clockwise direction. *Default:* The pins are set in the clockwise direction by default.	
Spacing	Displays the center-to-center spacing between pins for multi-pin editing. A spacing of 1 track means pins should be placed on every track with no empty tracks between them. The spacing is either in micrometers or by layer track, as specified by *Unit*. *Positive* spacing values spread pins to the right along a horizontal block edge, or up along a vertical block edge. *Negative* spacing values spread pins to the left along a horizontal block edge, or down along a vertical block edge.	
Unit	Specifies the units used for pin spacing: micrometers or layer tracks.	
Snap To	Indicates the grid or layer to which the pins should snap:	
	Manufacturing Grid	Specifies that the pins should snap to the manufacturing grid.
	User Grid	Specifies that the pins should snap to a user-defined grid.
	Layer Track	Specifies that pins should snap to the layer tracks.
Assign Fixed Status	If selected, sets pin status to *fixed*. *Default*: The pin status is set to placed.	
Batch Mode	If selected, enables pin-editing in batch mode.	
Master Clone Aware	If selected, it enables master-clone context awareness for feasibility checking.	
Fix Overlapping	If selected, automatically moves the pin to the closest acceptable position. When deselected, allows a pin to be placed in the selected position, overriding overlap rules. **Note:** This option applies only to *Snap To Layer Track*.	

Honor Partition and/or Pin-Level Constraints	
	If selected, the user-defined partition-level and/or pin-level constraints will be followed. The following constraints are honored when this option is selected: pin spacing, pin size, pin-to-corner distance, and partition-allowed pin layers. If not selected, the user-defined constraints are not applied to the affected pins. in this case, the pins are assigned exactly as per the attributes you specify in the Pin Editor form.
USE	Specifies one of the following +USE properties: • SIGNAL • CLOCK • ANALOG
	*Reset Pin Info*--Resets the pin editing entries to their original values.
Align	Opens the Pin Alignment form.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `editPin`

Related Topics

For information on the following topics, see Floorplanning the Design in the *Innovus User Guide*.

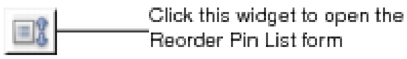
- Using the Pin-Spreading Feature
- Using a Pin as the Starting Point for Spreading Pins
- Using the Center of a Block Edge as the Starting Point for Spreading Pins
- Spacing Pins Evenly Using Explicit Starting and Ending Points

Reorder Pin List

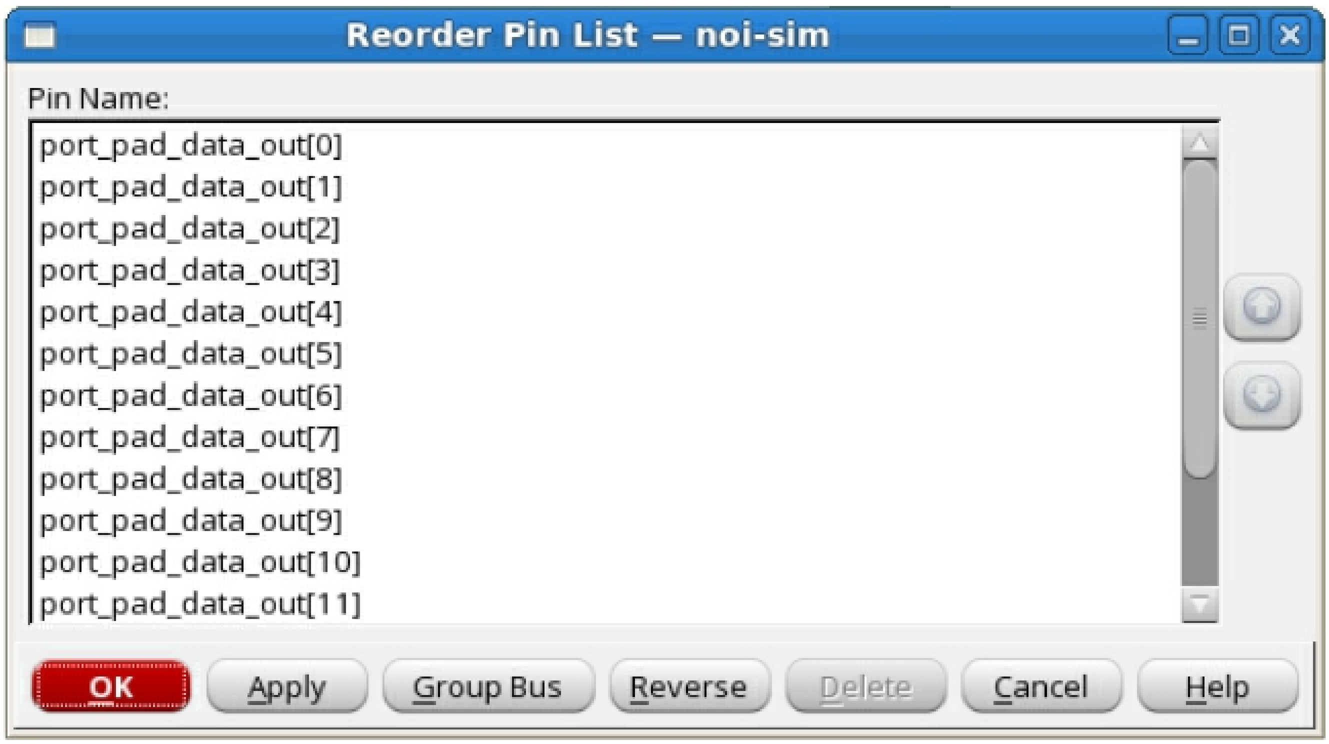
Use the Reorder Pin List form to display and manage your pin editing session.

Complete the following steps:

1. Choose *Edit - Pin Editor*.
2. Click on a pin or group of pins from the *Pin Group* panel.
3. Click the widget to the right of the *Pin Name(s)* text field.



The Reorder Pin List form appears.



Reorder Pin List Fields and Options

Pin Names	Highlight a pin and use the up or down arrow keys at the right side of the Reorder Pin List form to move the pin to a different place in the pin list. You can also select a pin and drag-and-drop it to the new location. **Note:** You can select multiple pins.
Group Bus / Expand Bus	*Group Bus*: Groups bus pins. *Expand Bus*: Ungroups bus pins.
Group PG Pin/Expand PG Pin	
	Group PG Pin: Groups power and ground pins. *Expand PG Pin*: Ungroups power and ground pins.
Reverse	Reverses the order of the selected pins.
Delete	Deletes selected pins from the list.

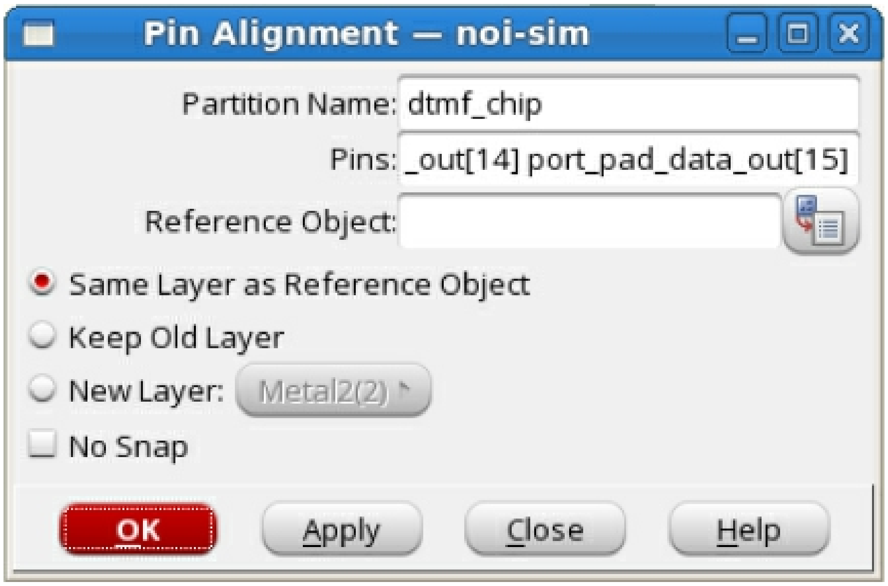
Pin Alignment

Use the Pin Alignment form to align pins between blocks on their facing edges. By default, this command snaps pins to the routing grid.

Note: Specified pins will not be aligned if they do not have the reference connections on the reference block, or if the reference pins are not assigned prior to running this command.

Complete the following steps:

1. Choose *Edit - Pin Editor.*
2. Click the *Align* button at the bottom of the Pin Editor.



Pin Alignment Fields and Options

Partition Name	Specifies the name of the partition for which you want to align pins.
Pins	Specifies the pin(s) to be aligned between the facing edges of the target block and reference block. This field contains the same value(s) as *Pin Name(s)*. When you select a pin group in the Pin Editor, those pins appear in the *Pins* field of this form.
Reference Block	Specifies the instance name of the reference block to which the specified pins will be aligned.
New Layer	Specifies whether to keep the current pin layer or specify a new pin layer. *Default*: If you do not specify this option, the new pin layer will be the same as the referenced layer to reduce wire routing.
No Snap	Prevents pins from being snapped to the routing grid.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `pinAlignment`
- `createNetGroup`
- `addNetToNetGroup`

Wire

The Edit - Wire menu provides the following options:

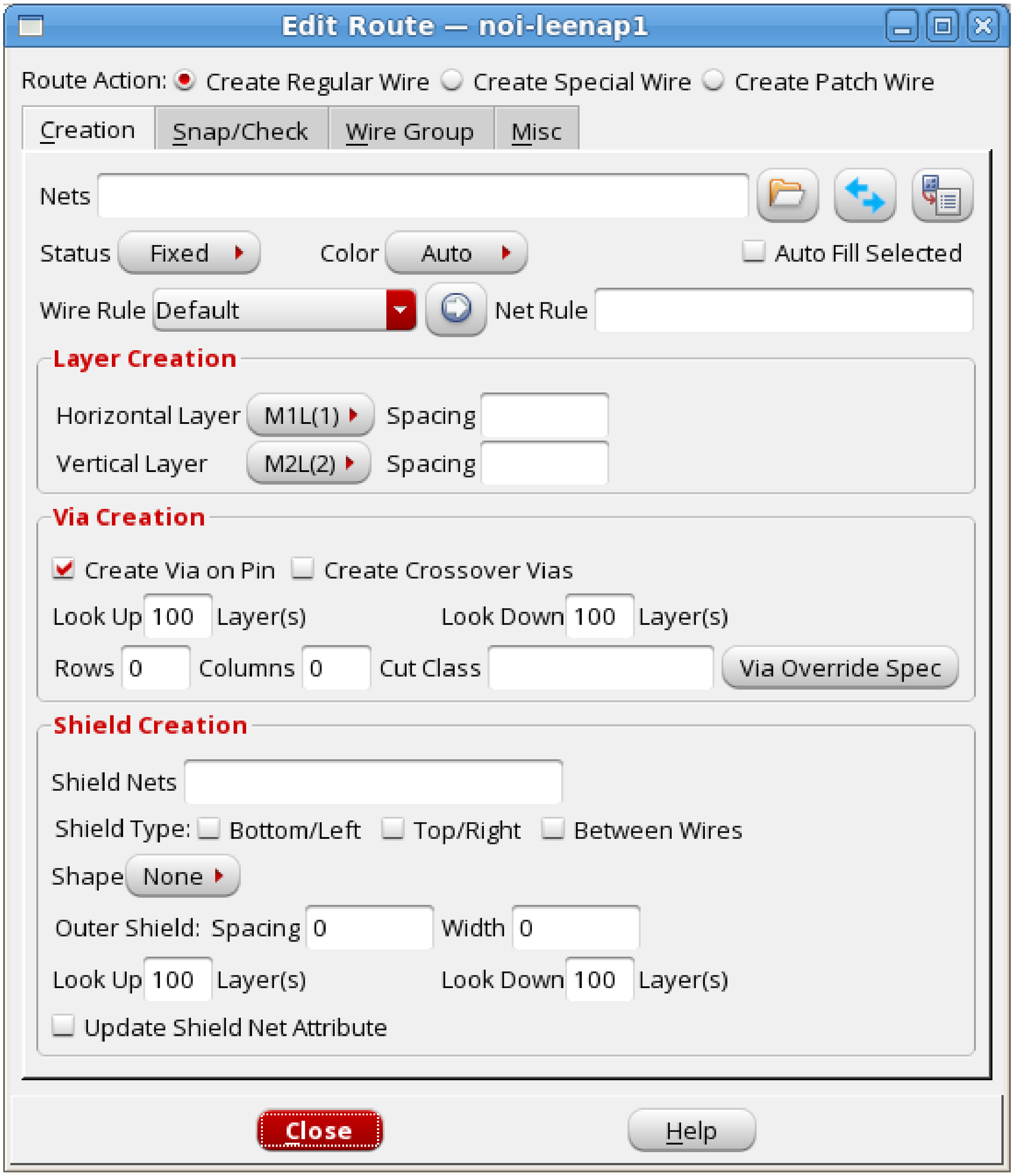
- Edit
- Move
- Cut
- Stretch
- Add Via
- Add Polygon

Edit

Use the Wire Editor or Edit Route form to edit wires and vias. The information you specify on the form applies only to wires and vias that you add or change with the wire editor--it does not affect wires or vias added by the NanoRoute router, power route, or other routing commands.

Use one of the following methods to open the Edit Route form:

- Choose *Edit - Wire - Edit*.
  Or
- Press the `e` bindkey to access the Edit Route form quickly



The Wire Editor or the Edit Route form provides the following route actions:

- *Create Regular Wire* - Provides options for creating a regular wire. This is the default route action.
- *Create Special Wire* - Provides options for creating a special wire.
- *Create Patch Wire* - Provides options for creating a patch wire.

The Edit Route form contains the following dynamic pages:

- *Creation*
- *Snap/Check*
- *Wire Group*
- *Misc*

On all pages, the content changes dynamically depending on the route action you have chosen (regular, special, or patch). The *Creation* and *Snap/Check* pages are available for all route actions. The remaining pages are not available for the *Create Patch Wire* route action.

Edit Route - Creation

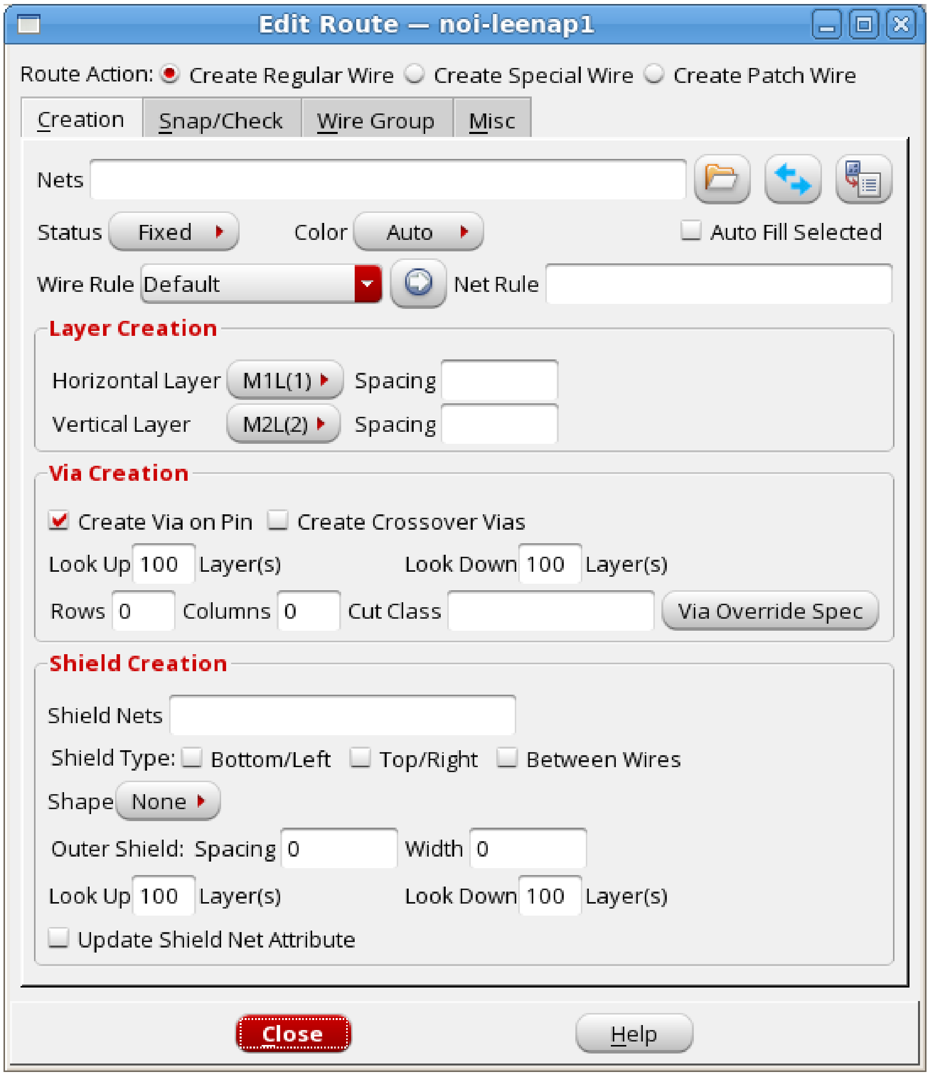
Use the *Creation* page of the Edit Route form to specify the options for creating a wire on a regular or special net or to create a patch wire. To open the *Creation* page:

1. Select the appropriate *Route Action* on the Edit Route form depending on whether you are creating a regular, special, or patch wire.
2. Click the *Creation* tab. This tab is open by default.

Note: The contents of the *Creation* page varies depending on the *Route Action* you have chosen.

Edit Route - Creation Fields and Options

Route Action: Create Regular Wire



Wire Creation	Provides the following options for wire creation:
Nets	Specifies the nets to edit. By default, the Edit Route form displays the name of the previously edited net in the *Nets* field. This is convenient if you want to continue drawing wires on the same net. However, if you want to edit another net, click the new delete button ( ) in the *Nets* field to delete the net name easily and then specify the required net name(s). For example, you can specify the net names VDD1 VSS1 VDD2 VSS2. The order of the net names determines the drawing arrangement of the wires.

- For horizontally drawn wires, the first net name entered is drawn as the top-most wire, followed by the next net name, and so on. The last-entered net name is drawn as the bottom-most wire.
- For vertically drawn wires, the first net name entered is drawn as the left-most wire, followed by the next net name, and so on. The last-entered net name is drawn as the right-most wire.

Use the following format to specify a bus:

`netName[x:y]`

For example, to draw eight wires for a bus, specify the following:

`netName[7:0]`

This is equivalent to specifying `netName[7], netName[6], ... netName[0]`. Specifying `netName[0:7]` reverses the order.

> When auto query is enabled, you can use the `Shift + S` keyboard shortcut to populate the *Nets* field with the net name of the selected wire. For more information, see *Auto Query*.

The following buttons and check box are associated with this field:

-  (Load) - Loads a file that contains a list of net names. In the file, each net name must be on a separate line. For more information, see **Open (For Net Names)** form below.
-  (Reverse) - Reverses the order of the names displayed in the *Nets* field. For example, if the *Nets* field contains the net names VDD1 VSS1 VDD2 VSS2 and you click *Reverse,* the order of the net names changes to VSS2 VDD2 VSS1 VDD1.
-  (*Copy From Selected*) - Copies the name of the selected net or the net for the selected wire, via, instance pin, or IO pin in the main window. Use this button to fill the Nets field easily with the name of the net for the selected object. If the *Auto Fill Selected* check box is selected, the tool automatically inputs the net name of the selected pin/net when you pop up the Edit Route form.

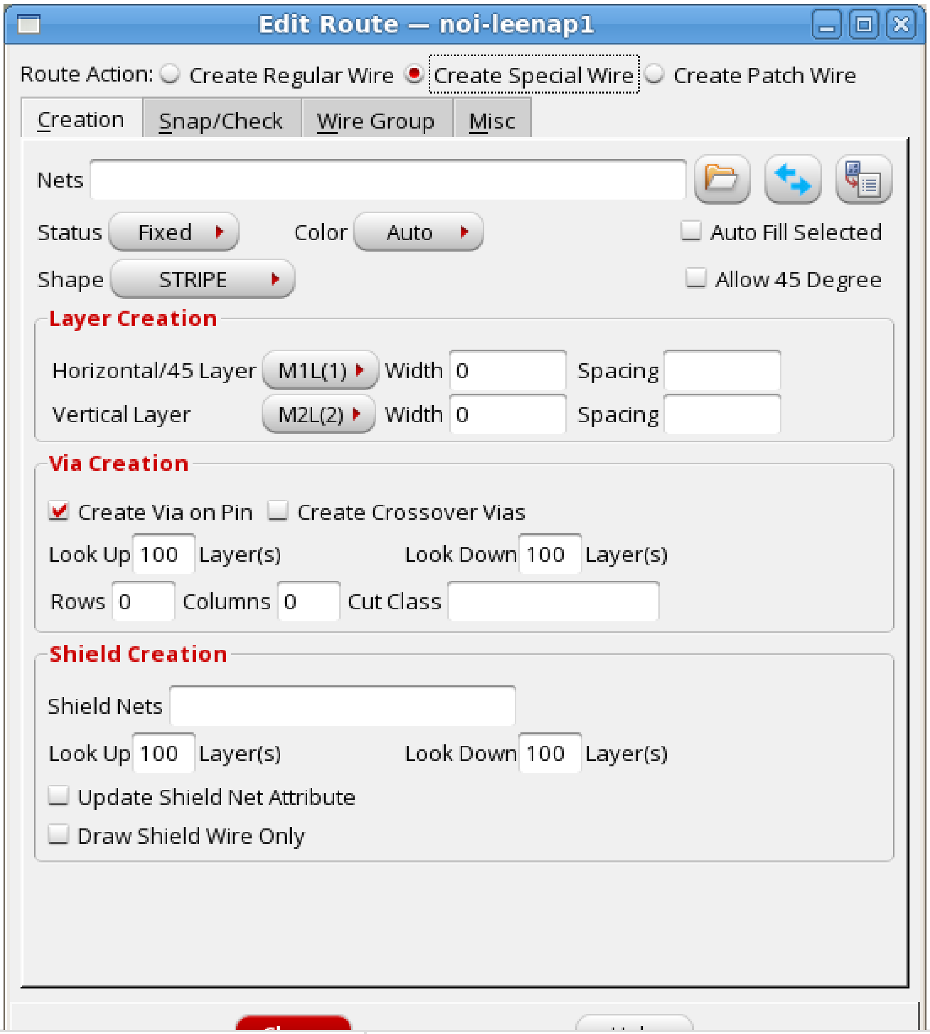
		• *Auto Fill Selected* - When turned on, the *Nets*, *Status*, *Horizontal Layer*, and *Vertical Layer* fields are dynamically updated whenever you change your selection in the GUI. However, if you select wires belonging to multiple nets in the main window, the tool ignores the *Auto Fill Selected* option and retains the name of the previously edited net. Default: Off
	Status	Specifies the status associated with the wire you draw. Default: *Fixed*
	Color	Specifies how to assign mask color on the double patterning technology (DPT) layer of the wire segment to be created. Select one of the following: • *Auto*: Mask color is assigned automatically. • *Mask1*: Assigns *Mask1* color to the added wire segment. • *Mask2*: Assigns *Mask2* color to the added wire segment. • *Mask3*: Assigns *Mask3* color to the added wire segment. Default: *Auto*
	Wire Rule	Specifies the non-default rule (NDR) assigned to the wires to be created. The added wire segments use the width and extension defined in LEF file for that rule. By default, the *Wire Rule* drop-down list shows all the NDRs in LEF. If the specified net(s) already has an NDR attached, that rule will be displayed selected in the *Wire Rule* field. Otherwise, *Wire Rule* field displays the *Default* rule. If you select a different NDR from the *Wire Rule* drop-down list on this form, the selected NDR is applied to the wire segments created during the session and does not impact the rule assigned on the net(s). The  (*Apply Wire Rule to Net Rule*) button updates the net rule with the user-specified wire rule.
	Net Rule	Specifies the non-default rule (NDR) from LEF for the nets specified in the *Nets* field. This field is read-only and is grayed out.

	Horizontal Layer	Specifies the layer for horizontal wires. *Default*: `M1` The *Spacing* text box next to *Horizontal Layer* can be used to specify the distance between horizontal wires. For regular wires with *Default* rule, you can change the spacing to be a larger value than the default. For regular wires with an NDR rule, the *Spacing* value is taken from the NDR. *Default*: `""`
	Vertical Layer	Specifies the layer for vertical wires. *Default*: `M2` The *Spacing* text box next to *Vertical Layer* can be used to specify the distance between vertical wires. For regular wires with *Default* rule, you can change the spacing to be a larger value than the default. For regular wires with an NDR rule, the *Spacing* value is taken from the NDR. *Default*: `""`
Via Creation		Provides the following options for creating vias:
	Create Via on Pin	Creates vias at pins. You might need to deselect this option for bump pins that are not square-shaped. *Default*: On
	Create Crossover Vias	Creates a via when you draw a wire that crosses a wire or pin of the same net that is on a different layer. Vias are not created if the minimum or maximum layer constraints prevent the creation of a via. If you deselect this option, the tool does not create vias at crossovers. For example, if you draw a wire from left to right, the tool begins creating a via at the left edge of the vertical target. This via is removed as soon as the drawing wire moves past the right edge of the vertical target. **Note:** If you draw a wire between two pins, the tool creates vias on the pins as needed, regardless of whether this option is selected or deselected. *Default*: Off

	Look Up ___ Layer(s)	Specifies the number of layers above the current layer that an added wire connects to using a via. Default: 100 (all metal layers)
	Look Down ___ Layer(s)	Specifies the number of layers below the current layer that an added wire connects to using a via. Default: 100 (all metal layers)
	Rows	Specifies the number of rows in a via cut. *Default:* `0`
	Columns	Specifies the number of columns in a via cut. *Default*: `0`
	Cut Class	Specifies the cut class name of the vias. *Default:* `""`
	Via Override Spec	Opens the Via Override Spec form in which you can enter the specs for overriding the default via selection. Use the Via Override Spec form if you do not want Wire Editor to select vias automatically. For more information, see Via Override Spec form below. Specifying overrides in this form is equivalent to using the `setEditMode -via_override_spec {`*`specification`*`}` option.

<table>
<tr><td colspan="2">Shield Creation</td><td>Provides the following options for creating shields:</td></tr>
<tr><td></td><td>Shield Nets</td><td>Specifies the nets for the shield wires, usually power or ground names. Separate multiple net names with spaces.</td></tr>
<tr><td></td><td>Shield Type</td><td>Specifies the side to which a minimum width shield wire should be added:
Bottom/Left - Specifies that minimum width shield wires should be added at the bottom side of horizontal routes or the left side of vertical routes. The spacing of the added shield wire is determined by the design rules in the technology file.
Top/Right - Adds a minimum-width shield wire at the top side of horizontal routes or the right side of vertical routes. The spacing of the shield wire is determined by the design rules in the technology file.
Between Wires - Adds minimum-width shield wires centered between two adjacent wires.
Note: If you do not want to specify the side to which the minimum width shield wire should be added, leave the check boxes unselected.</td></tr>
<tr><td></td><td>Shape</td><td>Specifies the shape associated with the shield wire you draw. Use all upper-case letters for the shape.
Default: None</td></tr>
<tr><td></td><td>Outer Shield</td><td>Specifies the spacing and width for outer shield wires. The following options are associated with this field:
Spacing - Specifies the spacing, in microns, to the outer shield wires.
Default: <code>0</code> (minimum spacing on the layer)
Width- Specifies the width, in microns, of the outer shield wires. Entering a value in this field is optional.
Default: <code>0</code> (minimum wire width on the layer)</td></tr>
</table>

	Look up ___ layer(s)	Specifies the number of layers above the current layer that an added shield wire connects to using a via. Default*:* 100 (all metal layers)
	Look down ___ layer(s)	Specifies the number of layers below the current layer that an added shield wire connects to using a via. Default*:* 100 (all metal layers)
	Update Shield Net Attribute	Specifies whether the shield net attribute on a signal net should be automatically updated. Select this check box if you want Nanoroute to recognize the net as a shield net and not remove it during routing. Default: Off
Route Action: Create Special Wire		



Wire Creation		Provides the following options for wire creation:
	Nets	Specifies the nets to edit. See description of *Nets* for regular wires (*Route Action: Create Regular Wire*) for more details.
	Status	Specifies the status associated with the wire you draw. Default: *Fixed*
	Color	Specifies how to assign mask color on the DPT layer of the wire segment to be created. See description of *Color* for regular wires (*Route Action: Create Regular Wire*) for more details.

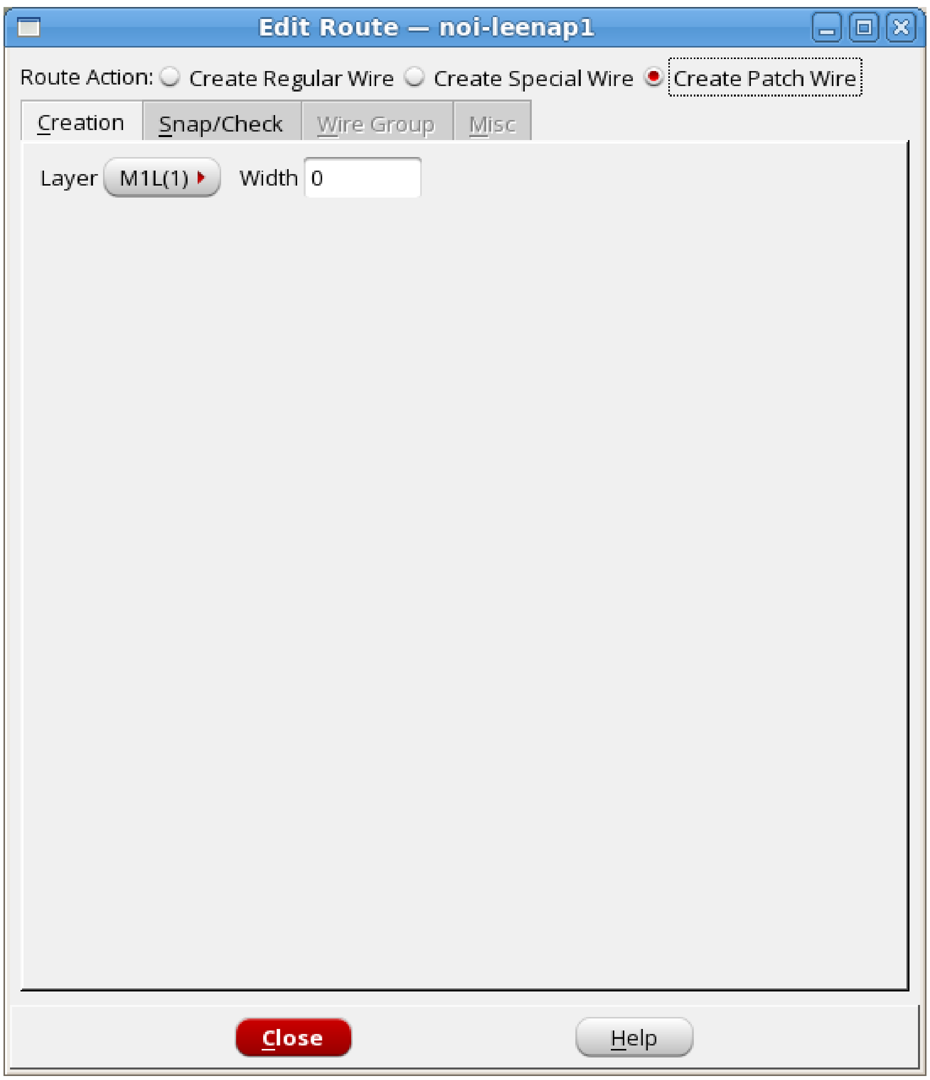
	Shape	Select one of the following shapes for each wire created in the Add Wire mode: • *None* • *RING* • *STRIPE* • *FOLLOWPIN* • *IOWIRE* • *COREWIRE* • *BLOCKWIRE* • *FILLWIRE* • *FILLWIREOPC* • *PADRING* • *BLOCKRING* • *DRCFILL* *Default:* None
	Allow 45 Degree	Lets you draw a 45-degree wire using the mouse. The wire direction is determined by the mouse position. This option has the following limitations: • It can be used for special nets and bus guides. • You can draw only one net at a time. • It is limited to on-line design rule checking. *Default*: Off

	Horizontal/45 Layer	Specifies the layer for horizontal or 45-degree wires. *Default*: `M1` The following options are associated with this field: • *Width* - Specifies the width for horizontal or 45-degree wires. *Default:* `0` • *Spacing* - Specifies the distance between horizontal/45-degree wires. *Default*: ""
	Vertical Layer	Specifies the layer for vertical wires. *Default*: `M2` The following options are associated with this field: • *Width* - Specifies the width for vertical wires. *Default:* `0` • *Spacing* - Specifies the distance between vertical wires. *Default*: ""
Via Creation		Provides the following options for creating vias:
	Create Via on Pin	Creates vias at pins. You might need to deselect this option for bump pins that are not square-shaped. *Default*: On
	Create Crossover Vias	Creates a via when you draw a wire that crosses a wire or pin of the same net that is on a different layer. See description of *Create Crossover Vias* for regular wires (*Route Action: Create Regular Wire*) for more details. *Default*: Off
	Look Up ___ Layer(s)	Specifies the number of layers above the current layer that an added wire connects to using a via. Default: 100 (all metal layers)

	Look Down ___ Layer(s)	Specifies the number of layers below the current layer that an added wire connects to using a via. Default: 100 (all metal layers)
	Rows	Specifies the number of rows in a via cut. *Default:* 0
	Columns	Specifies the number of columns in a via cut. *Default*: 0
	Cut Class	Specifies the cut class name of the vias. *Default:* ""
Shield Creation		Provides the following options for creating shields:
	Shield Nets	Specifies the nets for the shield wires, usually power or ground names. Separate multiple net names with spaces.
	Look up ___ layer(s)	Specifies the number of layers above the current layer that an added shield wire connects to using a via. Default*:* 100 (all metal layers)
	Look down ___ layer(s)	Specifies the number of layers below the current layer that an added shield wire connects to using a via. Default*:* 100 (all metal layers)
	Update Shield Net Attribute	Specifies whether the shield net attribute on a signal net should be automatically updated. Select this check box if you want NanoRoute to recognize the net as a shield net and not remove it during routing. Default: Off

	Draw Shield Wire Only	Specifies whether the wire being created is a shield wire. When this check box is selected, the wire editor creates a wire with the net name in *Shield Nets*. The newly created wire/via has its status set to *Shield* and its shield signal net set to the net name specified in *Nets*. Note that you can specify only one net in *Nets* when drawing a shield wire. The new shield wire/via also has its shape set to *None*. The shield wire defaults to the minimum width and spacing, unless explicitly set to other values. Note that NanoRoute supports only minimum width and minimum spacing. Default: Off

Route Action: Create Patch Wire



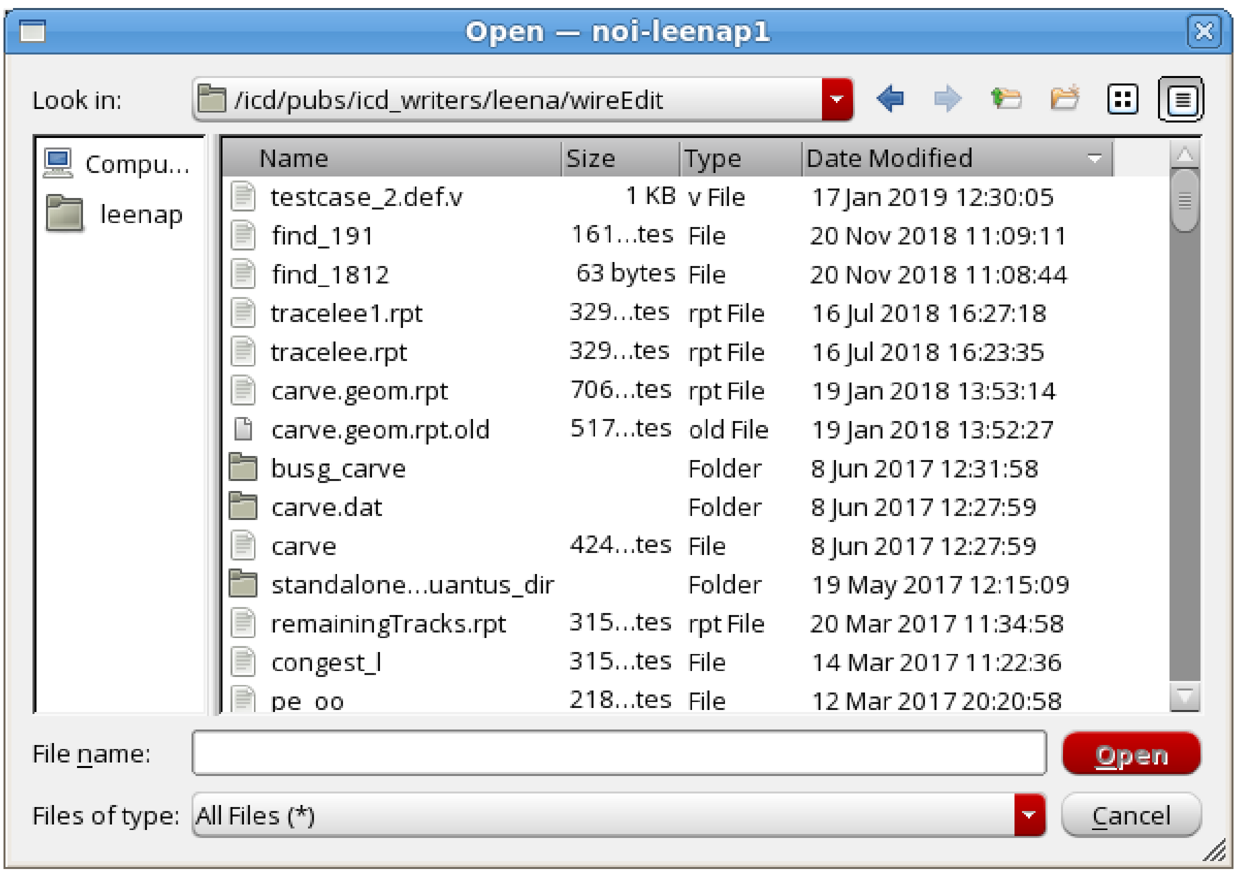
Layer	Specifies the layer for creating a patch wire.
Width	Specifies the width for the patch wire.

Open (For Net Names)

Use the Open form to load a net name file in the *Nets* field of the *Edit Route - Creation* page. The net name file can contain only one net name per line. Net names for a bus must be listed as individual net names. The following example shows the contents of a file with a list of net names:

```
VDD1

VSS1

VDD2

VSS2
```

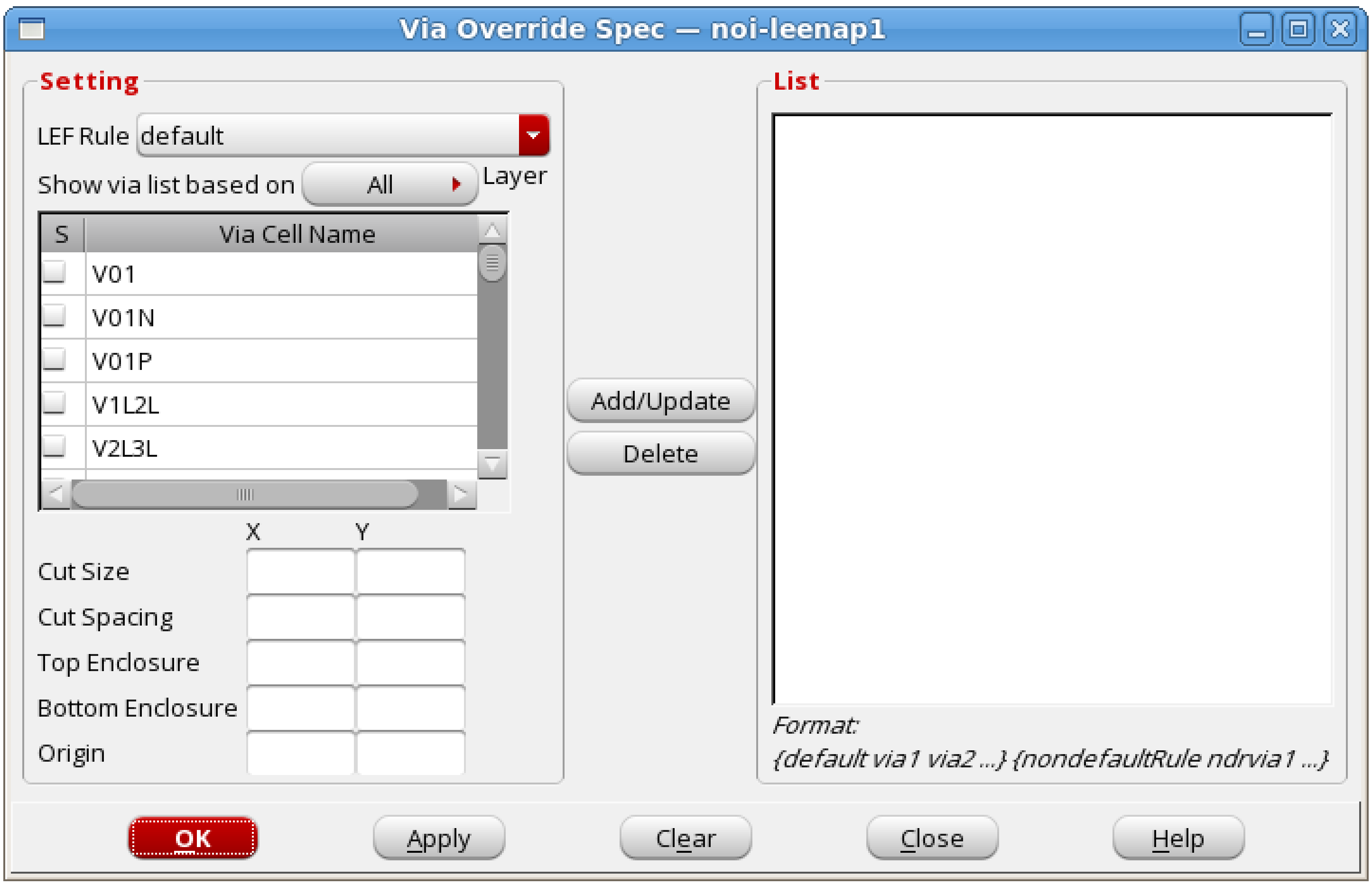
To access this form, choose *Edit - Wire - Edit* from the menu bar and then click the *Load* button on the *Creation* page of the Edit Route form.



Via Override Spec

Use the Via Override Spec form if you do not want Wire Editor to select vias automatically for regular wires.

1. Choose *Edit* - *Wire* - *Edit* from the menu bar.
2. Click the *Creation* tab of the Edit Route form.
3. Click the *Via Override Spec* button on the *Creation* page.



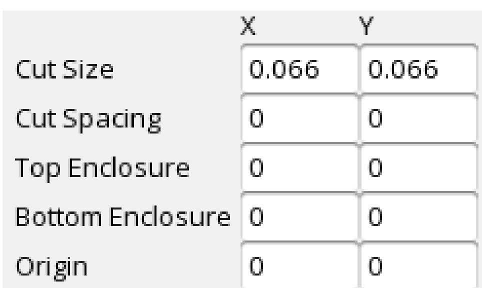
Via Override Spec - Fields and Options

LEF Rule	Lists the default rule and NDRs.

<table>
<tr>
<td>Show via list based on ______ layer</td>
<td>Lists the via layers based on the rule specified in LEF Rule. Select the via layer for which you want to view the via cell list.</td>
</tr>
<tr>
<td>Via List</td>
<td>Lists the vias for the specified layer(s). The list has two columns:

S column - Displays a checkbox for each via cell name in the via list. If you want to add a via to the override list, choose the corresponding check box from this column.
Via Cell Name column - Lists the via cells for the specified via layers.
</td>
</tr>
<tr>
<td>Via Information Box</td>
<td>Displays the following information for the via selected in the via list:

Cut Size
Cut Spacing
Top Enclosure
Bottom Enclosure
Origin

The via information displayed is read-only.


Note - Via information is displayed if only one via is selected. If multiple vias are selected (or no via is selected) in the via list, the via information box remains blank.</td>
</tr>
</table>

List	Displays the existing via override spec. Override values have the following format:
	`{default` *`via1 via2`* `...} {`*`nondefaultrule ndrvia1 ndrvia2 ...`*`}`
	For example, the following override spec specifies via selections for the *default* rule:
	`{default via12 via23 via45} {SP spvia12}`
	As specified, Wire Editor makes via selections for layers as follows:
	• For the *Default* rule:
	   ◦ via12 for layer V12
	   ◦ via23 for layer V23
	   ◦ via45 for layer V45
	• For the non-default rule SP:
	   ◦ spvia12 for layer V12
	Note: Wire Editor automatically selects the best vias for the layers that are not specified in Via Override Spec.

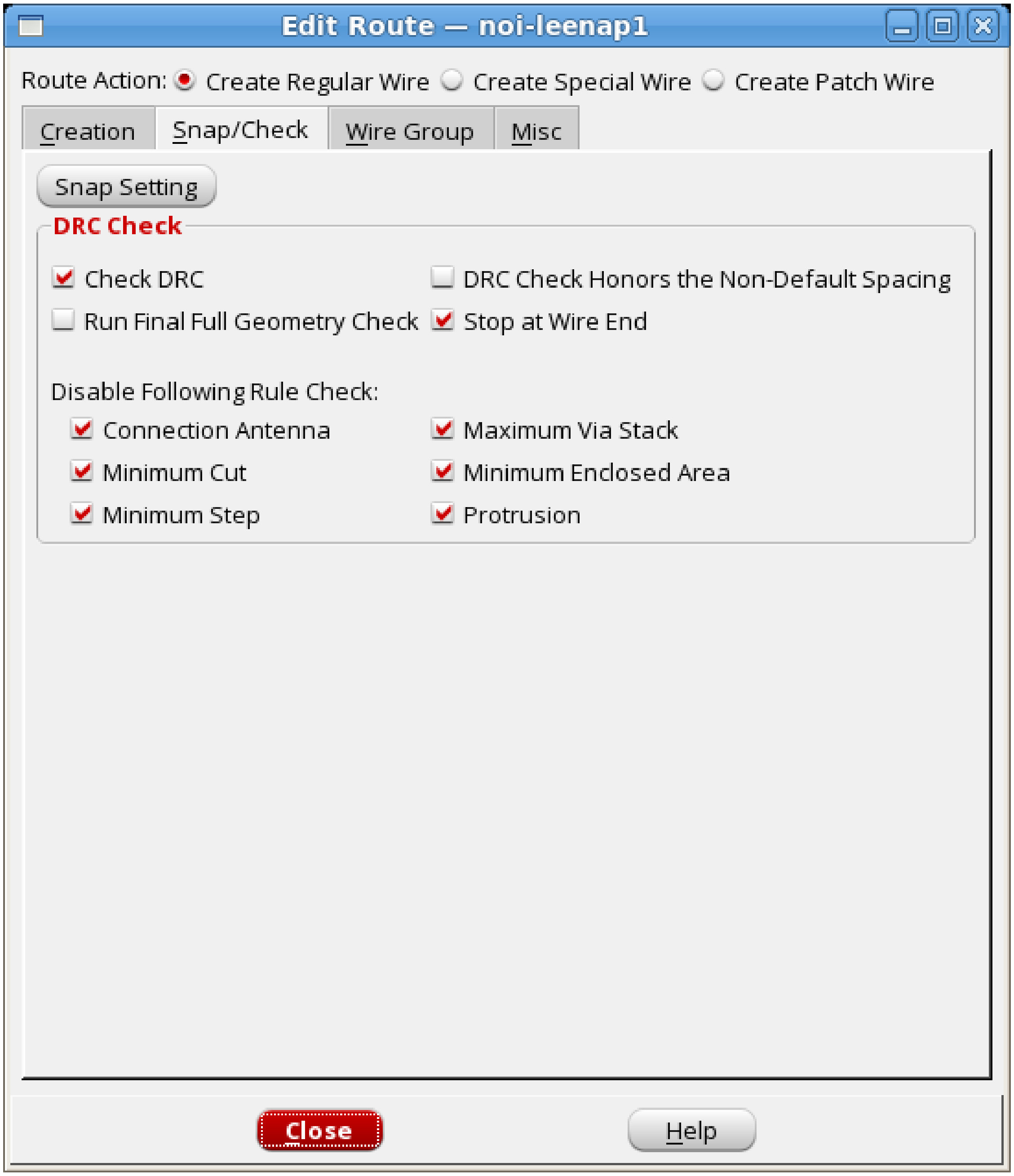
Add/Update button	Adds a via override value or appends to an existing one: • If you want to add a via cell to a new override spec, select its check box in the *S* column and then click the *Add/Update* button. • If you want to add a via cell to an existing via override spec, select the existing spec from the *List*, select the via cell you want to add, and then click the *Add/Update* button. Click *OK* or *Apply* after you have completed the override spec list.
Delete button	Deletes the selected via override spec from the *List*.

Edit Route - Snap/Check

Use the *Snap/Check* page of the Edit Route form to specify snap settings and DRC options for creating a regular, special, or patch wire. To open the *Snap/Check* page:

1. Select the appropriate *Route Action* on the Edit Route form depending on whether you are creating a regular, special, or a patch wire.
2. Click the *Snap/Check* tab.

Note: The content of the *Snap/Check* page remains the same, irrespective of the type of wire you are creating.



Edit Route - Snap/Check Fields and Options

Snap Setting button	Opens the *Snap Setting* form, where you can customize the way wires, vias, and trims are snapped. You can also access this form by choosing *Edit - Wire - Snap* from the menu bar or by clicking the drop-down arrow next to the *Snap* button () on the Wire Edit toolbar and selecting *Snap Setting* from the drop-down menu. For details on the options available for snapping, see the *Snap Setting* section in this chapter.	
DRC Check	Provides the following options for performing DRC checks during wire creation:	
	Check DRC	Specifies whether design rule checking (DRC) should be performed during wire editing. If a check does not pass, a DRC marker appears on the screen. *Default*: On
	DRC Check Honors the Non-Default Spacing	Specifies whether non-default spacing defined in the non-default rule (NDR) of the editing net should be used for spacing check during wire editing. ***Notes*** • By default, the Wire Editor DRC check honors the default/minimum spacing. • If the net or via has an NDR with the `HARDSPACING` keyword, the Wire Editor DRC check honors the non-default spacing even if *DRC Check Honors the Non-Default Spacing* is not selected. • If *DRC Check Honors the Non-Default Spacing* is selected, all subsequent wire editing commands honor the non-default spacing during the geometry check on the net/via if the NDR is defined. *Default*: Off
	Run Final Full Geometry Check	Specifies whether to do final check with verify. When selected, Wire Editor calls the Full Geometry Checker (FGC) engine for the final DRC check on the bounding box of the changed area after commits. This ensures that the final wire editing result is DRC clean as per FGC. Select this option if you are using advanced rules, such as 20nm and 14nm. *Default*: Off

	Stop at Wire End	Checks DRC rules and stops moving or stretching wires before causing a violation: • If selected, the software stops moving or stretching the wire at the closest location available before a violation occurs. In this case, you cannot move a wire to the desired destination if that wire passes through a location where a DRC violation occurs. • If this check box is deselected, the software ignores DRC rules when moving or stretching wires. That is, you can move or stretch a wire to the desired location even if it results in a DRC violation. *Default*: On
	Disable Following Rule Check	Specifies which violation types should be ignored during wire editing. You can specify the following options: • *Connection Antenna* - Does not check the connection antenna for DRC violations. *Default*: On • *Maximum Via Stack* - Does not check maximum via stack DRC violations during wire editing. *Default*: On • *Minimum Cut* - Does not check for minimum cut DRC during wire editing. *Default*: On • *Minimum Enclosed Area* - Does not perform minimum enclosed area DRC during wire editing. *Default*: On • *Minimum Step* - Does not perform minimum step DRC during wire editing. *Default*: On • *Protrusion* - Does not perform protrusion DRC during wire editing. *Default*: On **Note**: If you do not want any violation to be ignored, deselect all the options.

Edit Route - Wire Group

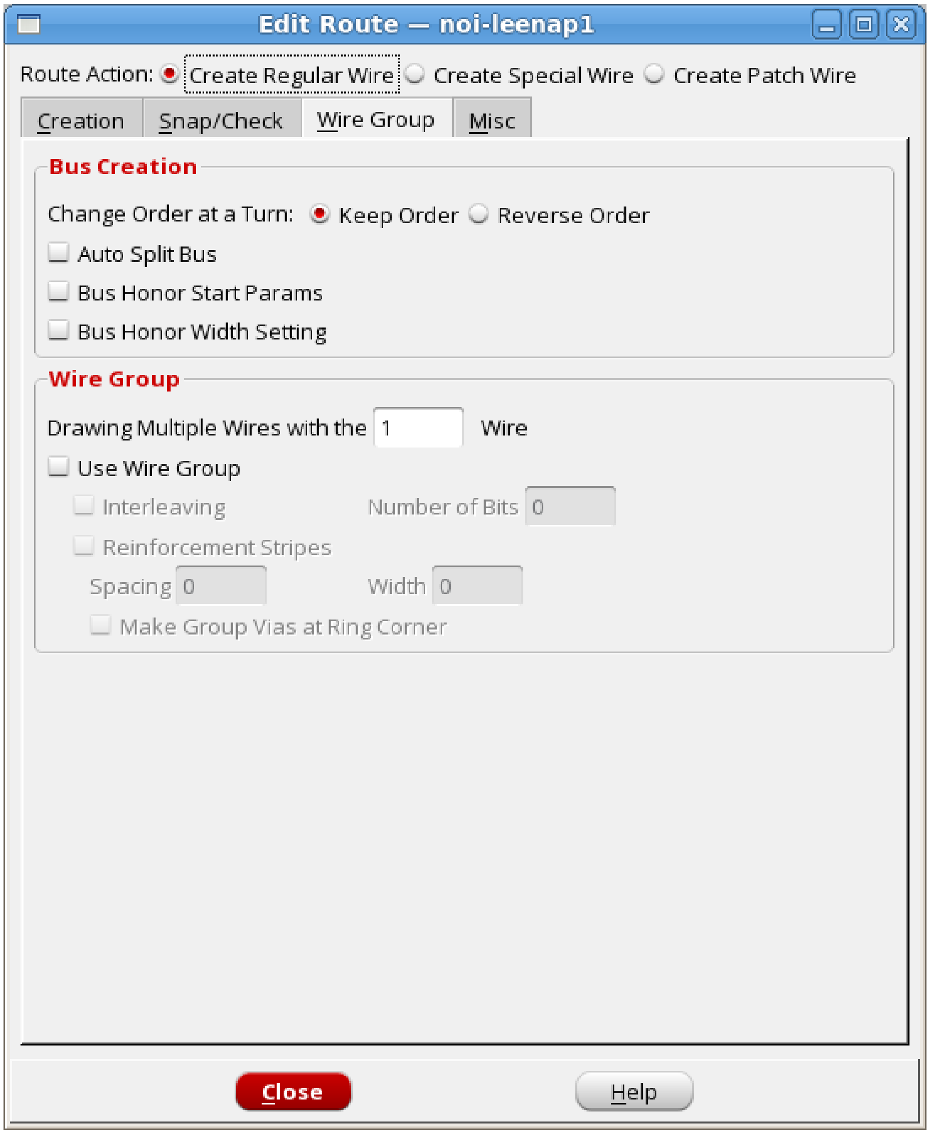
Use the *Wire Group* page of the Edit Route form to group multiple wires from the same net and specify bus creation options. Use wire groups to decrease resistance and provide stronger connections. To open the *Wire Group* page:

1. Select the appropriate *Route Action* on the Edit Route form depending on whether you are creating a regular wire or a special wire.
2. Click the *Wire Group* tab.

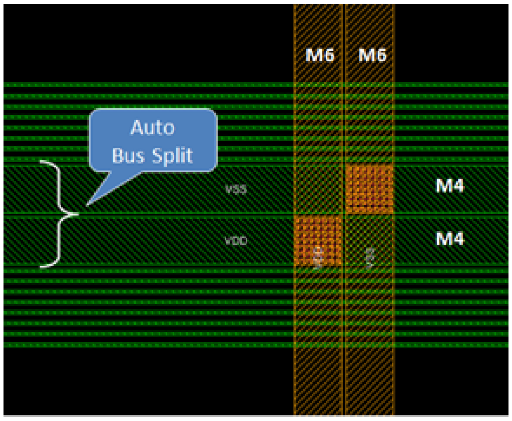
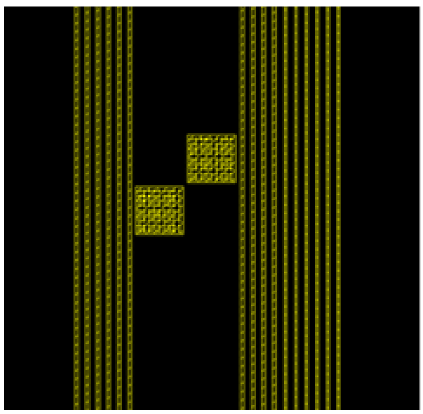
Note: The content of the *Wire Group* page varies depending on the *Route Action* you have chosen. This page is not available (grayed out) for the *Create Patch Wire* route action.

Edit Route - Wire Group Fields and Options

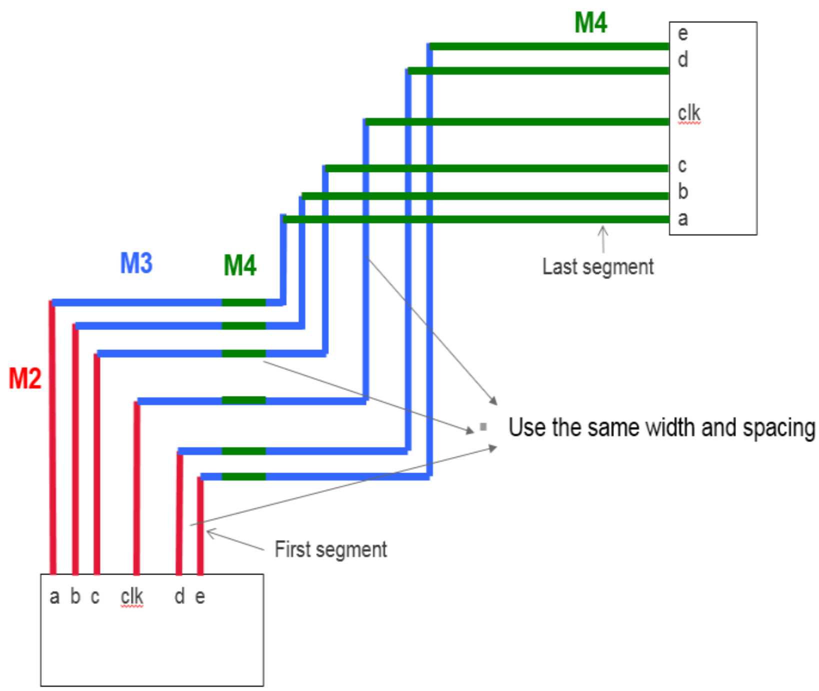
Route Action: Create Regular Wire



Bus Creation	Provides the following options for bus creation:
Change Order at a Turn	Specifies whether the order of the wires reverses or stays the same when the wire makes a 90-degree turn. *Default: Keep Order*

	Auto Split Bus	Specifies whether or not Wire Editor should split buses automatically around power structures to avoid DRC violations.  Auto bus split around power trunk  Auto bus split around power vias By default, there is no detour around via array and anchor wires of the bus being drawn always snap to the routing tracks. *Default*: Off

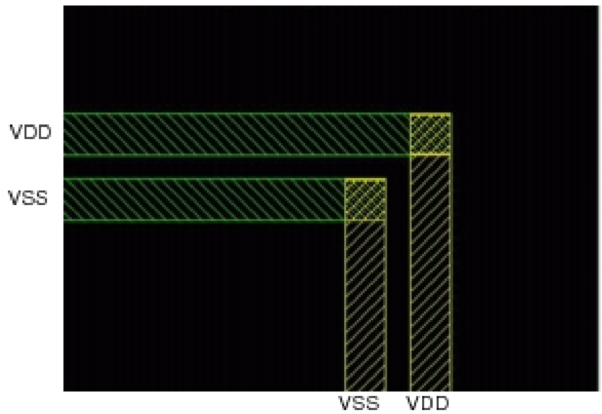
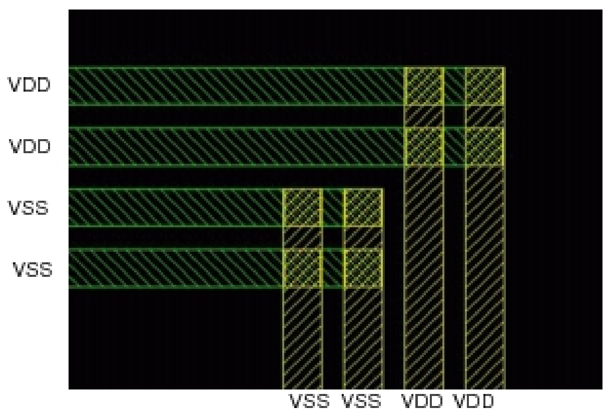
<table>
<tr><td></td><td>Bus Honor Start Params</td><td>
Specifies that the wire width and spacing of the start points (pins) should be honored when drawing routes for a bus. The following diagram depicts how the width and spacing of the bus is maintained through turns for the the 2nd to N-1 wire segment, if you select the Bus Honor Start Params check box:

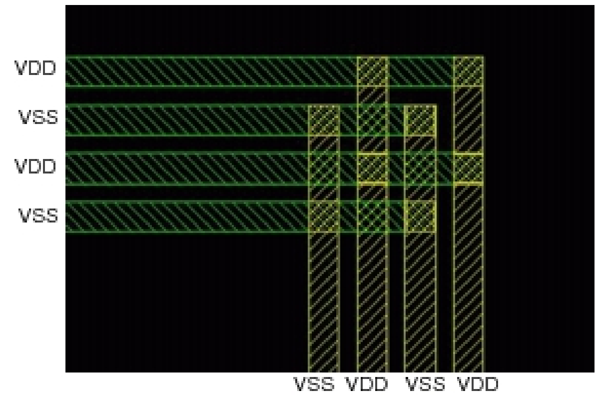


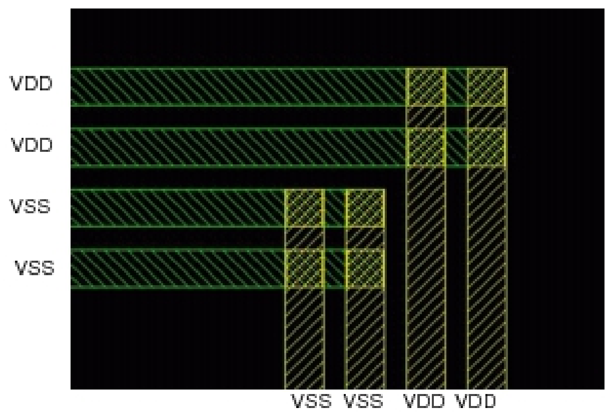
Default: Off
</td></tr>
<tr><td></td><td>Bus Honor Width Setting</td><td>
Specifies whether or not the tool should adjust the wire width when snapping bus wires to pin. By default, if the Snap Bus to Pin check box is selected in the Snap Setting form, the tool adjusts the wire width to be the same as the macro or IO pin width. If you do not want the wire width to be adjusted to match the pin width, select the Bus Honor Width Setting check box. In this case, the tool uses the width values defined on the Creation page when snapping the bus to pin.

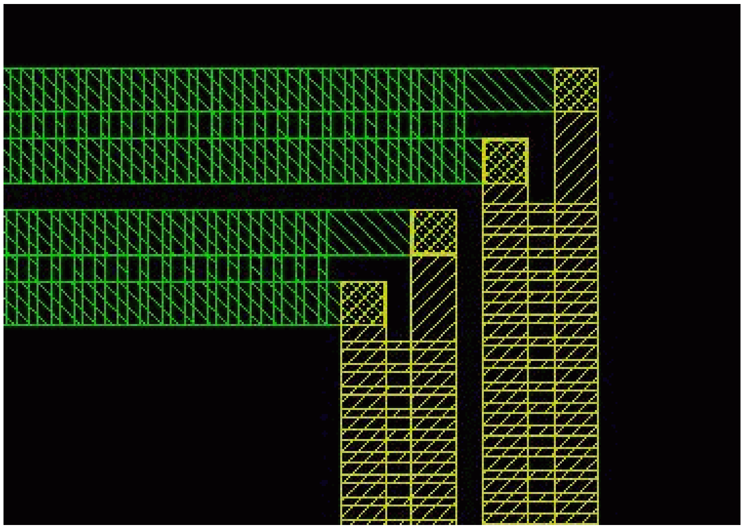
Default: Off (Pin width is used with Snap Bus to Pin)
</td></tr>
<tr><td colspan="2">Wire Group</td><td>Provides the following options for forming wire groups:</td></tr>
</table>

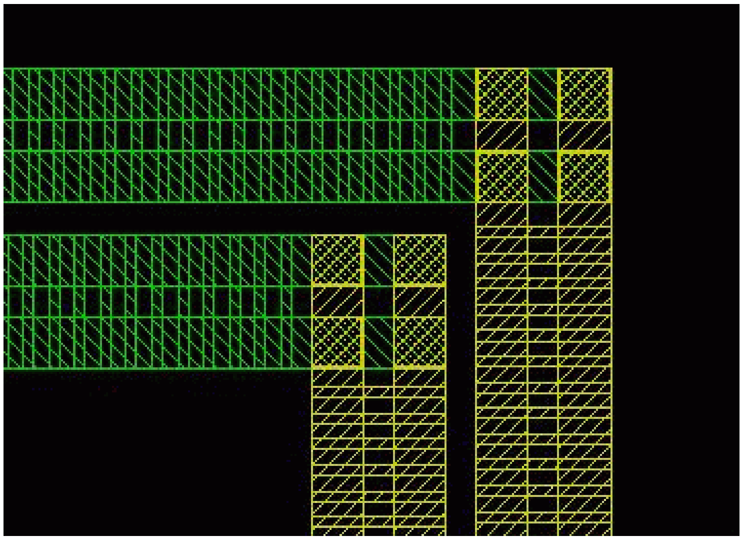
	Drawing Multiple Wires with the _____ wire	Specifies which of the nets specified in the *Nets* field on the *Creation* page corresponds to the mouse pointer location when adding an array of wires. For horizontal wires, a value of `1` indicates the bottom-most net. For vertical wires, a value of `1` indicates the leftmost net. The *`value`* is an integer of the same or lower value as the number of nets. For example, if you specify five nets, you can specify `1`, `2`, `3`, `4`, or `5` as the value for this parameter. This net is also used as the reference net when changing direction. All other nets around this net are lengthened or shortened accordingly. *Default:* `1`

	Use Wire Group	Groups multiple wires from the same net. *Default:* Off **Note:** You must select *Use Wire Group* and specify 2 or more for *Number of Bits* to enable wire groups. The following figure shows power and ground wires that do not form a wire group.  The following figure shows power and ground wires that form a wire group. 

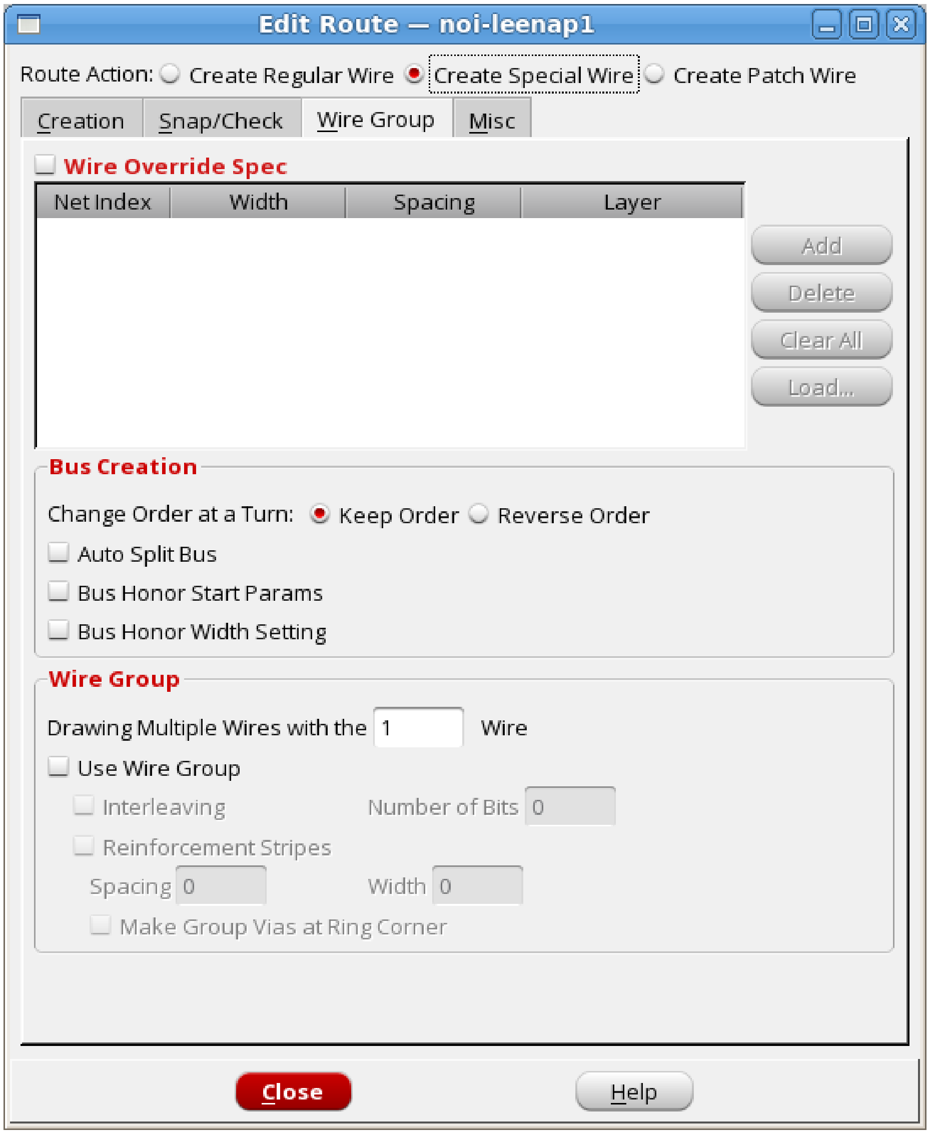
	Interleaving	Alternates the specified wires in the wire group. For example, if you specify VDD and VSS on the *Nets* page and select this option, the software alternates the power and ground wires in the wire group. *Default:* Off When *Interleaving* is specified, the Innovus software draws a wire group like the following:  **Note:** Do not select both *Interleaving* and *Reinforcement Stripes*--doing so creates shorts in the wire groups.

	Number of Bits	Specifies the number of times to replicate a wire in the wire group. For example, if you specify VSS and VDD on the *Nets* page, and specify 2 for this option, the software creates a wire group with two power wires and two ground wires. *Default:* 0 (disabled) **Note**: The value of this option must be greater than `1` to enable wire groups. When *Number of bits* is specified as 2, the software draws a wire group like the following: 

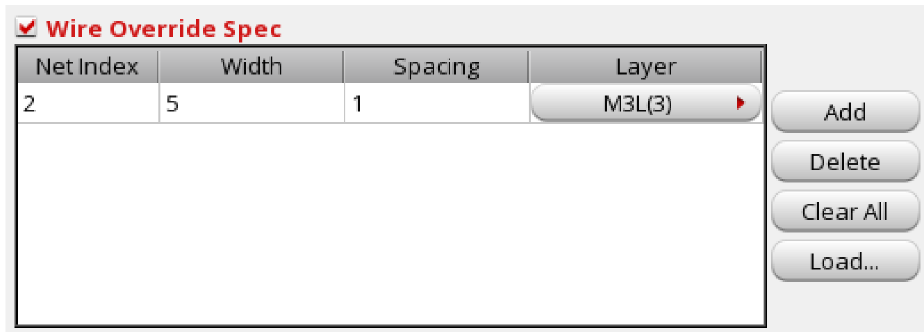
	Reinforcement Stripes	Creates slots in the wire group by creating wires that connect the wires in the wire group, but are orthogonal to them. Slots help to reduce resistance in power networks. *Default:* Off When *Reinforcement Stripes* is selected, the software draws a wire group like the following:  **Note:** Do not select both *Reinforcement Stripes* and *Interleaving*--doing so creates shorts in the wire groups.	
		Spacing	Specifies the spacing for the reinforcement stripes. *Default:* 0
		Width	Specifies the width of the reinforcement stripes. *Default:* 0

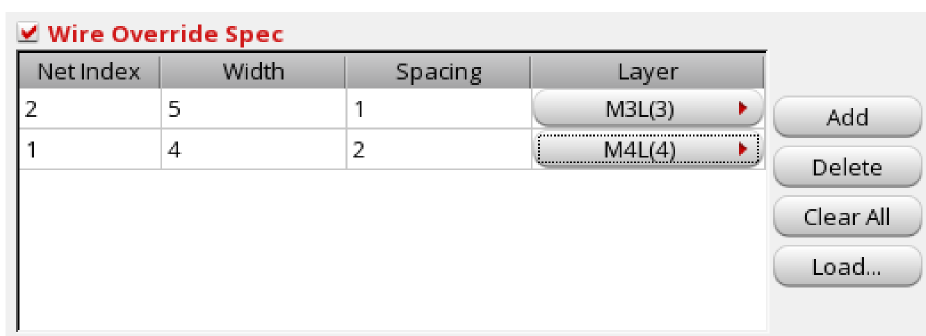
		Make Group Vias at Ring Corner	Specifies that the wire group uses group vias. Group vias are connected vias in a wire group. Using group vias ensures that the contact is maintained if one of the vias in the wire group produces a void. *Default:* Off In the following figure, the wire group has group vias:  **Note:** The figures in the rows explaining *Interleaving* and *Reinforcement Stripes* show wire groups that do not have group vias.

Route Action: Create Special Wire



Wire Override Spec	Specifies whether or not to use the override specification. Select this check box to enable the buttons and wire override specification table in this section. *Default*: Off

<table>
<tr>
<td></td>
<td>Add</td>
<td>
Adds a blank row to the wire override specification table. Specify desired values for Net Index, Width, Spacing, and Layer in the new row to complete the wire override specification and implement the related wire edit command.
For example, consider the wire override specification below:


This specification implements the following command:
<code>setEditMode -wire_override_spec {{2 5 1 M3L}}</code>
Note: You need not specify values for each cell in a wire override specification row. If you leave a specific cell in the row blank, that particular value is not overriden. For example, if you do not select any value from the Layer drop-down list, the tool does not override the layer setting.
You can add multiple wire override specification rows as follows:


This is equivalent to implementing the following command:
<code>setEditMode -wire_override_spec {{2 5 1 M3L} {1 4 2 M4L}}</code>
</td>
</tr>
</table>

	Delete	Deletes a row from the wire override specification table. To delete a row: 1. Click in any cell in the row to be deleted. The row gets selected. 2. Click the *Delete* button. **Note**: You cannot select multiple rows at the same time.
	Clear All	Clears all override specifications from the wire override specification table.
	Load	Loads the wire override specifications from a file.
Bus Creation		Provides options for bus creation. See description of the *Bus Creation* section for regular wires (*Route Action: Create Regular Wire*) for details.
Wire Group		Provides options for forming wire groups. See description of the *Wire Group* section for regular wires (*Route Action: Create Regular Wire*) for details.

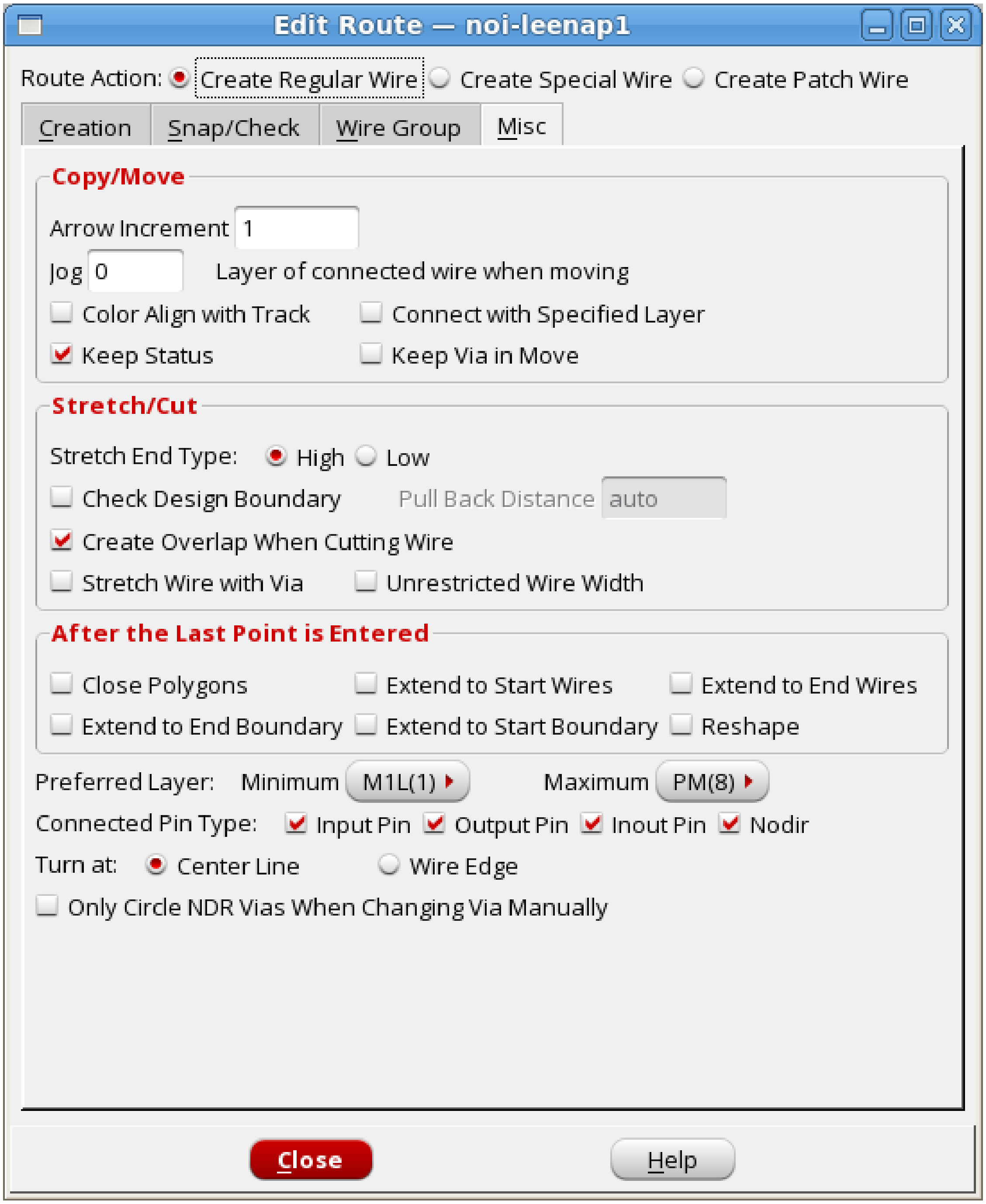
Edit Route - Misc

Use the *Misc* page of the Edit Route form to specify the shape and behavior of wires that are added or modified. To open the *Misc* page:

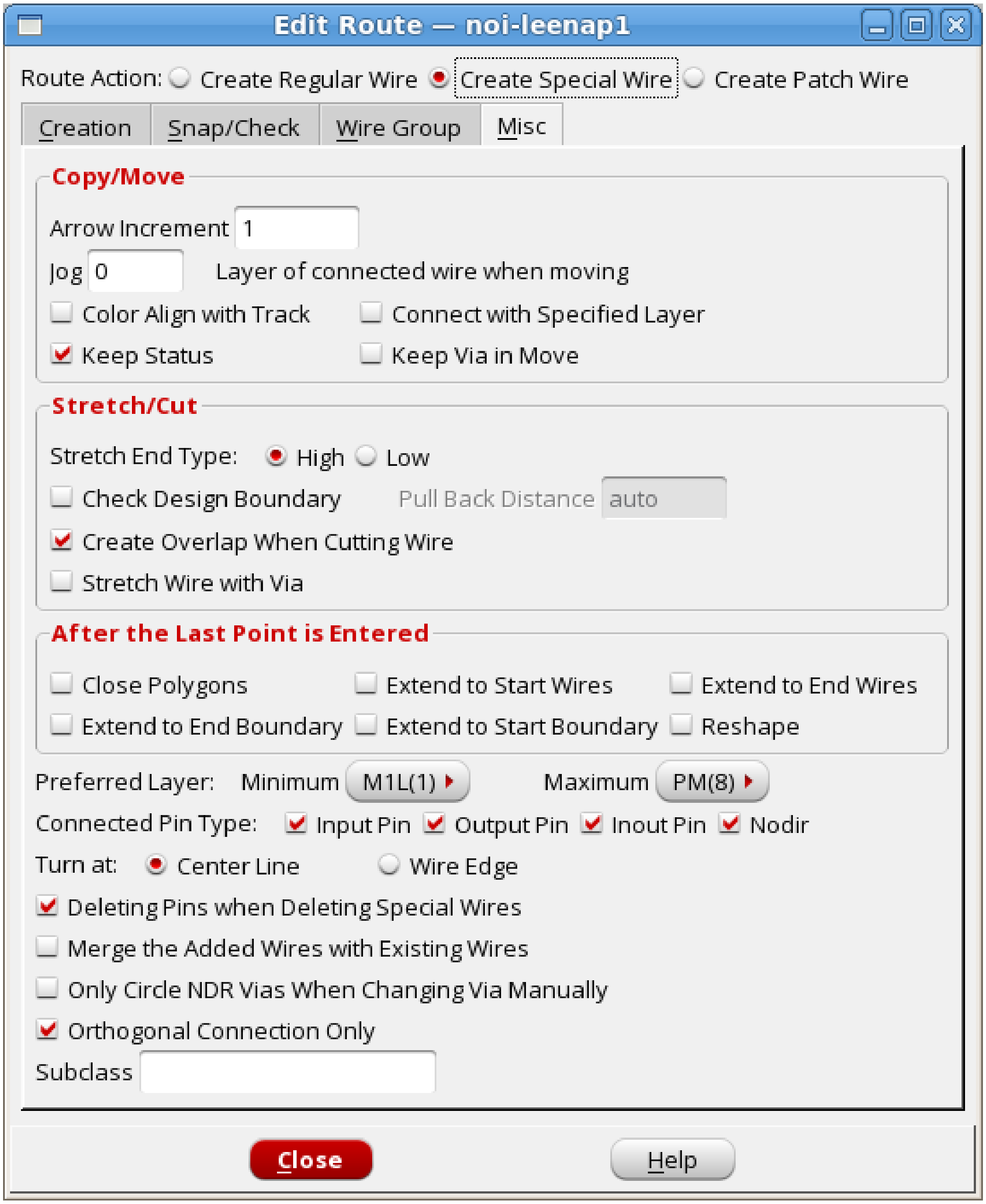
1. Select the appropriate *Route Action* on the Edit Route form to indicate whether you are creating a regular wire or a special wire.
2. Click the *Misc* tab.

Note: The contents of the *Misc* page varies depending on the *Route Action* that you have chosen. This page is not available (grayed out) for the *Create Patch Wire* route action.

Create Regular Wire - Misc



Create Special Wire - Misc



Edit Route - Misc Fields and Options

Note: Unless indicated otherwise, the fields defined below are available for **both** regular and special wires.

Copy/Move	Provides the following settings for copying or moving regular and special wires:	
	Arrow Increment	Specifies the step increments, in microns, to move wires with the arrow keys. *Default:* 1.0 The wire moves the specified increment distance in the direction of the arrow. Wire movement is subject to snap constraints.
	Jog ____ Layer of connected wire when moving	Specifies the number of layers by which the new jog wire segments created on moving a wire should be moved up or down. Note that the *Jog ____ Layer of connected wire when moving* option will have no impact if you have selected the *Connect with Specified Layer* check box. *Default*: 0
	Color Align with Track	Specifies whether the wire color is to be changed to match the track color during a move or copy operation. If you select the *Color Align with Track* check box and move or copy a wire to snap it to a track, the track color is automatically assigned to the wire. Note that if the wire does not snap to a track or if the wire covers more than one track, this option will not have any effect. This checkbox is turned off by default. This means when you move or copy a wire, the wire color is retained by default. *Default*: Off

	Connect with Specified Layer	Specifies whether or not the layer of connecting wires should be changed as per the Horizontal Layer or Vertical Layer setting when moving wires. If you select this check box, the move operation honors the Horizontal Layer and Vertical Layer settings while jogging metal layers. For instance, suppose you cut a vertical wire on `M4` such that the wire is divided into three wire segments. Now, if you select the wire segment in the middle and move it in the horizontal direction, the tool automatically creates new connecting wires on the layer defined by Horizontal Layer and drops vias correctly. *Default*
	Keep Status	Specifies whether or not object status should be changed during editing. This check box is selected by default, which means the wire status is not changed after editing. If this check box is deselected, the wire status is changed to `FIXED` automatically after a move or stretch operation. *Default*: On
	Keep Via in Move	Controls whether or not the original via is retained in a wire move or stretch. If this check box is selected, the tool keeps the via unchanged if there is no DRC violation as a result of the move or stretch. However, the tool can change the via if a DRC violation occurs. Do not select this check box if you do not want the original via to be retained when a wire is moved or stretched. *Default*: Off
Stretch/Cut	Provides the following settings for stretching or cutting regular and special wires:	
	Stretch End Type	Specifies the direction in which to stretch or reduce wires. Select one of the following options: • *High* - Stretches or reduces wires from the top for vertical wires or from the right for horizontal wires. • *Low* - Stretches or reduces wires from the bottom for vertical wires or from the left for horizontal wires. *Default*: *High*

	Check Design Boundary	Specifies that wires and vias are to be made inside the design boundary. If *Check Design Boundary* is selected, you cannot manually stretch a wire into the area defined by *Pull Back Distance*. **Note:** 45-degree wires do not follow this rule. *Default*: Off
	Pull Back Distance	Specifies the value for forbidden distance. If the *Check Design Boundary* is selected, the tool takes into account the *Pull Back Distance* setting during wire edit operations: • If the *Pull Back Distance* value is positive, the tool marks the corresponding area inside the boundary as an extra keep-out area. • If the *Pull Back Distance* value is `0`, the tool does not allow you to manually stretch a wire beyond the die boundary. If you try to stretch the wire edge beyond the boundary, the tool stops the wire edge at the boundary and prints a warning. If the edge of a wire is already beyond the boundary and you attempt to stretch it further, the wire remains in the current location and the tool does not allow further stretching. • If you stretch multiple wires with *Pull Back Distance* set to *auto*, the tool uses the largest spacing value of each layer as the pull back distance for related wire. **Note:** 45-degree wires do not follow this rule *Default*: *auto*, which means the tool uses the largest min spacing of the layer as the forbidden distance.
	Create Overlap When Cutting Wire	Creates overlaps while cutting wires. *Default*: On

	Stretch Wire with Via	Enables wires with intersects to be stretched easily. If this option is selected, you can select the via and the edge of metals and then stretch the wires and via together in a single step. *Default*: Off
	Unrestricted Wire Width	**For Regular Wires Only** Specifies whether the widening of a regular wire is unrestricted. By default, when you are changing the width of a wire, it snaps to the closest non-default route (NDR) available. If you select the *Unrestricted Wire Width* check box, a wire can be stretched to any width without any restrictions. *Default*: Off
After the Last Point is Entered	Specifies the behavior of the wires when the route is completed (that is, after the last point is set). Select any of the following options:	
	Close Polygons	Closes a route structure toward itself. For the closing to complete, the ending route segments must be drawn toward (but do not need to touch) the starting route segments. *Default*: Off
	Extend to Start Wires	After completing a route, the start of the route segment extends and connects to wires on the same net. If there is no such wire to extend to, the start point is not changed. *Default*: Off
	Extend to End Wires	After completing a route, the end of the route segment extends and connects to wires on the same net. If there is no such wire to extend to, then the end point is not changed. *Default*: Off
	Extend to End Boundary	Requires selection of *Extend to End Wires*. After completing a route, the end of the segment always extends to the cell boundary. If the segment is extended to the boundary and crosses wires on the same net, the tool makes a via connection to the wires. In addition, the tool creates pins at the boundary. *Default*: Off

	Extend to Start Boundary	Requires selection of Extend to Start Wires. After completing a route, the start of the segment always extends to the cell boundary. If the segment is extended to the boundary and crosses the wires on the same net, the tool makes a via connection to the wires. In addition, the tool creates pins at the boundary. *Default*: Off
	Reshape	Automatically trims redundant wires when new wires are added. *Default*: Off
Other settings	Provides options for miscellaneous settings, such as layer and connection pin type:	
	Preferred Layer	Specifies the layer range for added or moved wires and vias. Choose a layer from each of the following drop-down lists: • *Minimum* - Specifies the bottom-most layer on which to create or move wires and vias. • *Maximum* - Specifies the topmost layer on which to create or move wires and vias.
	Connected Pin Type	Specifies the type of pin on which a via should be generated. You can specify the following pin types: • *Input Pin* - Generates a via on an input pin. • *Output Pin* - Generates a via on an output pin. • *Inout Pin* - Generates a via on an inout pin. • *Nodir* - Generates a via on a pin for which no direction is specified. *Default*: On for all pin types

	Turn at	Specifies the start location of the new wire segment when a wire is turned. You can specify one of the following values: • *Center Line* - When you turn a wire, the center line of the new wire segment aligns to the end of the old wire segment. • *Wire Edge* - When you turn a wire, the long edge of the new wire segment aligns to the end of the old wire segment. *Default*: *Center Line*
	Delete Pins when Deleting Special Wires	**For Special Wires Only** Removes pins when deleting special wires. To keep pins, deselect this check box. *Default*: On
	Merge the Added Wires with Existing Wires	**For Special Wires Only** Specifies whether or not a wire being added should be merged automatically with any existing wire at that point. *Default*: Off
	Only Circle NDR Vias When Changing Via Manually	Specifies that when the *Shift + N* bindkey is used, the Wire Editor should circle through NDR vias only. *Default*: Off
	Orthogonal Connection Only	**For Special Wires Only** Does not consider wires and pins that are in the same direction as a target for connection when creating vias. For example, if you extend a wire to the left, any horizontal wire it meets is not considered a target. However, a vertical wire is considered a target. *Default*: On
	Subclass	**For Special Wires Only** Specifies the subclass name.

Related Topics

For more information on wire editing, see the Editing Wires chapter in the *Innovus User Guide*.

Related Text Commands

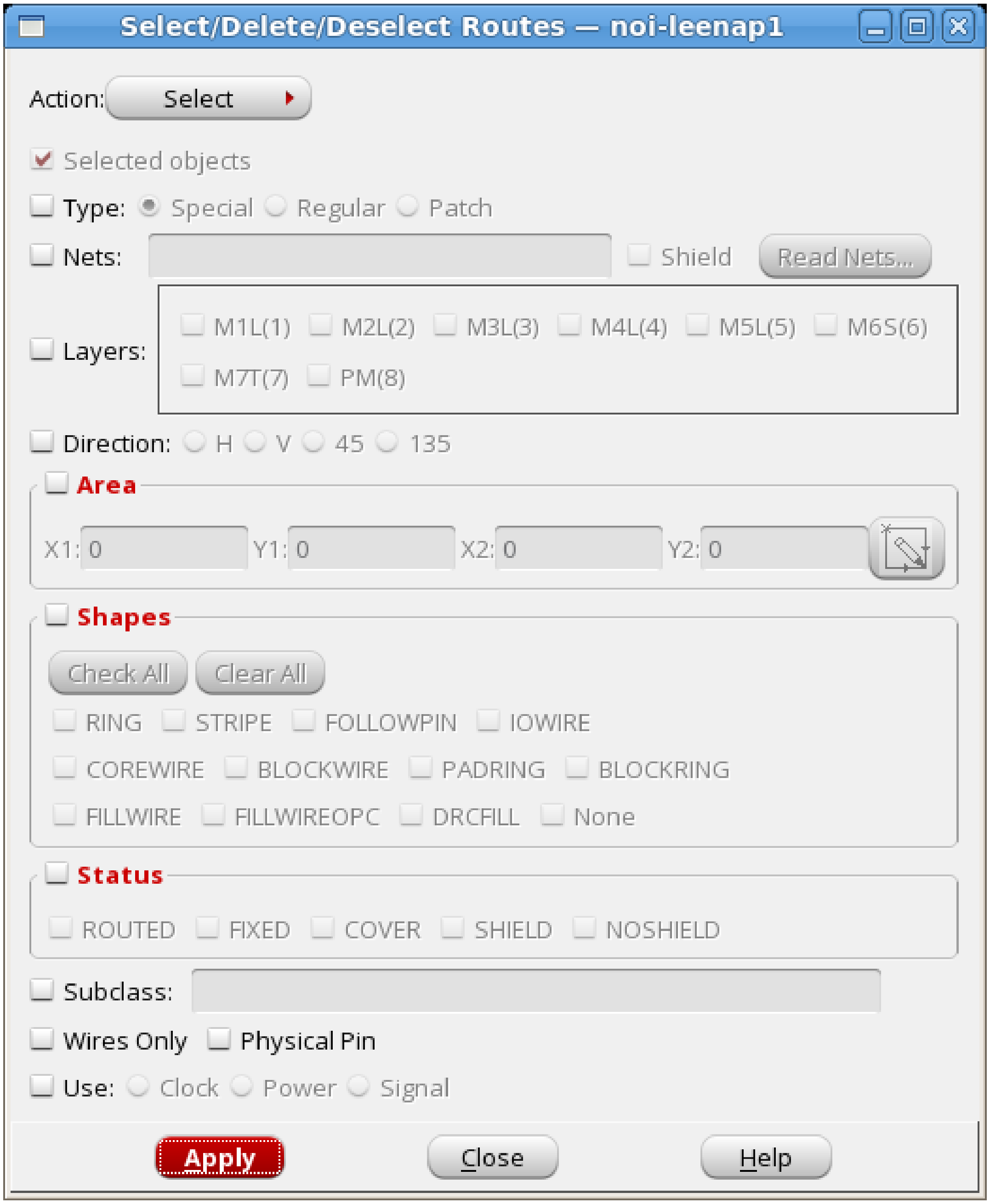
For information on the following commands, see "Wire Edit Commands" in the *Text Command Reference*.

- `editAddRoute`
- `setEditMode`

Select/Delete/Deselect Routes

Use the Select/Delete/Deselect Routes form to select, delete, or deselect wires. Use one of the following methods to open the Select/Delete/Deselect Routes form:

- Click the *Delete Wires* widget on the Wire Edit toolbar.
- Use the `D` keyboard shortcut.



Select/Delete/Deselect Routes Fields and Options

Action	Specifies whether to select, deselect, or delete wires when you click the *Apply* button. Select one of the following options from the pulldown menu:

	Select	Selects wires with attributes selected with other options on this form when you click the *Apply* button. This is the default.
	Deselect	Deselects wires with attributes selected with other option on this form when you click the *Apply* button.
	Delete	Deletes wires with attributes selected with other options on this form when you click the *Apply* button.
Selected Objects	Specifies whether to delete only selected objects. This option is available only for the *Delete* action. For *Select and Deselect*, this check box is grayed out. *Default* (for *Delete* action): *On*	
Type	• If selected, you must specify the type of wire to be selected, deselected, or deleted. • If deselected, all three wire types can be selected, deselected, or deleted. This is the default. *Default*: Off Select one of the following:	
	Special	Selects or deletes only special (power or ground) wires.
	Signal	Selects or deletes only regular (signal) wires.
	Patch	Selects or deletes only patch wires.
Nets	If selected, wires are selected, deselected, or deleted from only the nets specified in the text entry field. You can use wildcard values in this field. For example, if you specify `V*`, wires can be selected, deselected, or deleted from nets `VDD` and `VSS`. If deselected, objects can be selected, deselected, or deleted from any net. When auto query is enabled, you can use the `Shift + S` keyboard shortcut to populate this field with the net names of the selected objects. *Default*: Off	
Shield	Selects, deselects, or deletes the shield wire associated with the specified net.	

Read Nets	Loads an ASCII file that contains a list of net names. In the file, each net name must be on a separate line. The following example shows the contents of a net name file:
	`DTMF_INST/TDSP_CORE_INST/EXECUTE_INST/FE41_scan_enI`
	`DTMF_INST/FE47_scan_enI`
	`DTMF_INST/TDSP_CORE_INST/EXECUTE_INST/FE40_scan_enI`
	`DTMF_INST/FE46_scan_enI`
	`DTMF_INST/TDSP_CORE_INST/EXECUTE_INST/FE39_scan_enI`
	`DTMF_INST/FE45_scan_enI`
	`DTMF_INST/FE54_scan_enI`
	`DTMF_INST/TDSP_CORE_INST/FE38_scan_enI`
	`...`	

Layers	Selects, deselects, or deletes wires from the specified layers only. By default, wires are selected, deselected, or deleted from all layers. *Default*: Off	
Direction	Selects, deselects, or deletes wires with the specified orientation only, when selected. *Default*: Off	
	H	Specifies that only horizontal wires can be selected, deselected, or deleted.
	V	Specifies that only vertical wires can be selected, deselected, or deleted.
	45	Specifies that only 45-degree wires can be selected, deselected, or deleted.
	135	Specifies that only 135-degree wires can be selected, deselected, or deleted.
Area	Specifies the area in which to perform the action. Use the area button or specify the coordinates in the text boxes. *Default*: Off	

Shapes	Enables you to specify the shapes to select, deselect, or delete. If not selected, you can select, deselect, or delete all shapes. For shape definitions, see "`SHAPE`" in the *DEF Syntax* chapter of the LEF/DEF Language Reference. *Default: IOWIRE*	
	Check All	Makes all shapes on the list available to select, deselect, or delete.
	Clear All	Makes all shapes on the list unavailable to select, deselect, or delete.
Status	Enables you to specify the status of the object to select, deselect, or delete. Select one or more of the following: *ROUTED*, *FIXED*, *COVER*, *SHIELD*, *NOSHIELD*. **Note:** If you select *Type Special* and *Status NOSHIELD* or *Type Signal* and *Status SHIELD*, the software generates an error message. *Default*: Off	
Subclass	Enables you to select, deselect, or delete rings, stripes, or other wires belonging to a specific subclass. Select the check box and specify the required subclass name in the adjacent text box. *Default*: Off	
Wires Only	Deletes all the special wires in the net, leaving the vias untouched. *Default*: Off	
Physical Pin	Specifies that physical pins are to be deleted. You can use filter options, such as *Nets, Layers*, *Area,* and *Selected Objects,* along with *Physical Pin* to delete specific physical pins. **Note**: This option is available only for the *Delete* action. For *Select and Deselect*, this check box is grayed out. *Default* (for *Delete* action): Off	

Use	Indicates that wires will be deleted/selected/deselected on the basis of the specified use: `CLOCK`: Specifies that only wires for clock nets will be deleted. `POWER`: Specifies that only wires for power nets will be deleted. `SIGNAL`: Specifies that only wires for general signal nets will be deleted. *Default*: Off

Related Topics

For more information on wire editing, see the Editing Wires chapter in the *Innovus User Guide*.

Related Text Commands

For information on the following commands, see "Wire Edit Commands" in the *Text Command Reference*.

- `editDelete`
- `editDeselect`
- `editSelect`

Move

To move a wire segment:

- Choose *Edit - Wire - Move*.

Click the wire segment to be moved. Move the mouse pointer to see possible directions in which you can move the segment. You can move horizontal wires vertically and vertical wires horizontally. Click again at the new position where you want to place the wire segment.

Related Topics

For more information, see the "Moving Wires" section of the Editing Wires chapter in the *Innovus User Guide*.

Cut

Click this option to change the cursor to scissors when moved into the design display area. Move the cursor to draw a draw a line indicating where to cut a wire. The cut must go all the way through the wire.

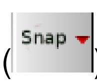
- Choose *Edit - Wire - Cut*.

Related Topics

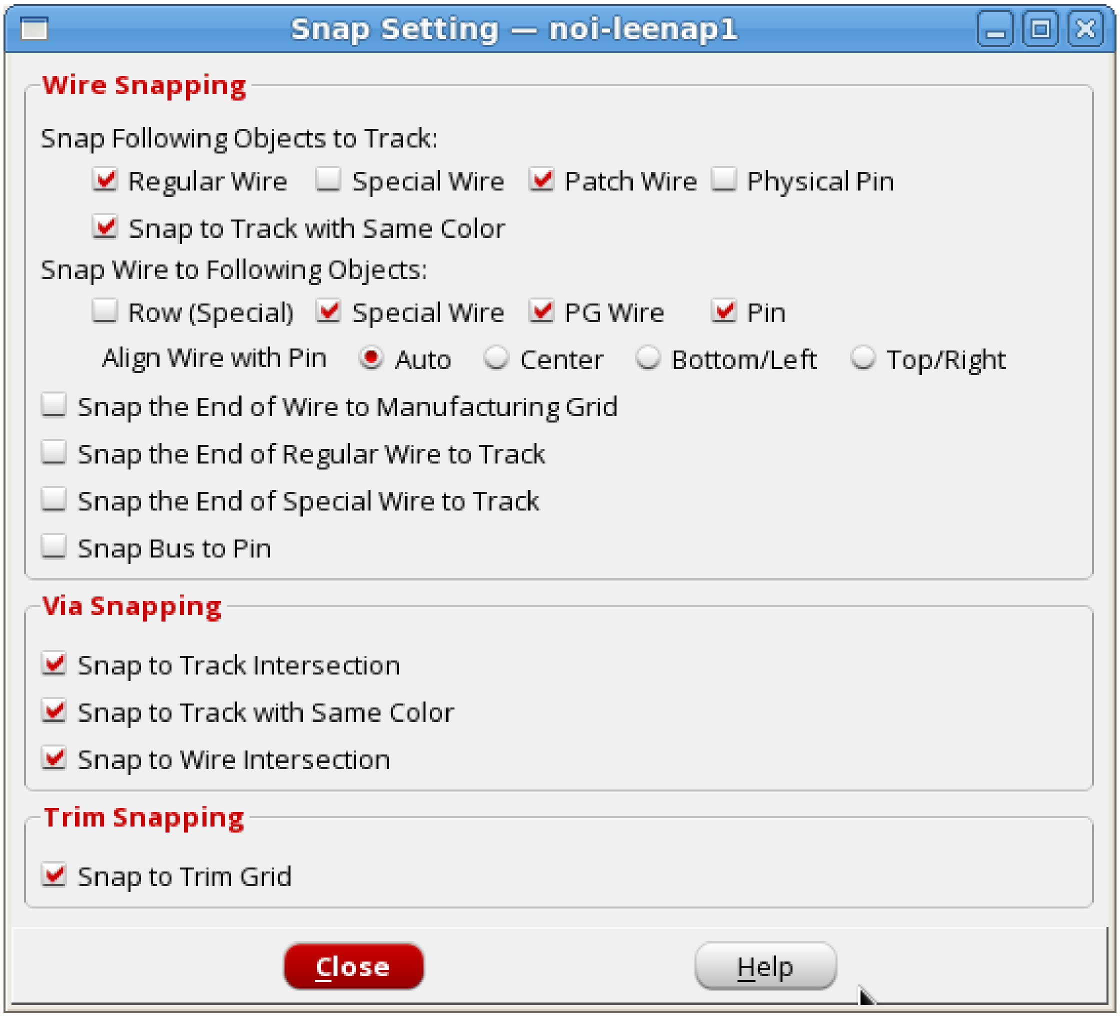
For more information, see the "Cutting Wires" section of the Editing Wires chapter in the *Innovus User Guide*.

Snap

Click this option to open the Snap Setting form where you can customize the way wires and vias are snapped. Use one of the following methods to access the Snap Setting form:

- Choose *Edit - Wire - Snap*.
- Click the drop-down arrow next to the *Snap* button (

) on the Wire Edit toolbar and select *Snap Setting* from the drop-down menu.
- Choose *Edit - Wire - Edit* to open the Edit Route form, open the *Snap/Check* page of the form, and then click the *Snap Setting* button.



Snap Setting Fields and Options

Wire Snapping

Snap Following Objects to Track	Snaps the wires being added or moved to the closest routing track in the preferred direction for the layer automatically. You can select the following options: • *Regular Wire* - Snaps the signal wires being added or moved to the closest routing track in the preferred direction for the layer automatically. This option also controls whether to cut signal wires on the routing track. *Default*: Selected • *Special Wire* - Snaps the special wires being added or moved to the closest routing track in the preferred direction for the layer automatically. This option also controls whether to cut special wires on the routing track. *Default*: Deselected • *Patch Wire* - Snaps patch wires automatically to the closest routing track for the layer as the wires are drawn, copied, or moved. *Default*: Selected • *Physical Pin* - Snaps a physical pin being moved to the closest routing track in the preferred direction for the layer automatically. *Default*: Selected • *Snap to Track with Same Color* - Snaps wires to a track with the same color automatically. *Default*: Selected **Notes** • If you do not want to snap any object to track, deselect all the options in this section. • See *Snap Wire to Following Objects > Pin* for a description of the software's behavior when both *Snap Following Objects to Track > Regular* (or *Special*) and *Snap Wire to Following Objects > Pin* are specified.
Snap Wire to Following Objects	Snaps the wires being added or moved to the specified object. You can select the following objects: • *Row (Special)* - Snaps the wires being added or moved to the nearest standard cell row. Use this option to create followpins. This option supports both horizontal and vertical rows. *Default*: Deselected • *Special Wire* - Automatically extends a special wire for maximum via

	coverage when crossing over a same-net wire on an adjacent layer.
	Default: Selected
	
	• *PG Wire* - Snaps new wires whose start point is within a "snap region" to the closest end of a power or ground wire on the same net. The snap region is one-half the width of the target wire.
	  ◦ The snap region for orthogonal wires forms a square with the width of the power or ground wire.
	  ◦ The snap region for wires at 45-degree angles to the power or ground wire forms a square from the point where the wire will connect. Each side of the square is the width of the power or ground wire.
	  ◦ The snap region for wires that are parallel to power or ground wires is the full power or ground wire.
	Default: Selected
	
	• *Pin* - Snaps the wires being added or moved to a pin automatically. If you double-click at a pin, it snaps the wire to the pin. To ensure the wire is snapped to the center of the pin, specify *Snap Following Objects to Track > Regular* (or *Special*) and select *Center* for *Align Wire with Pin*.
	Default: Selected
	
	When you select both *Snap Following Objects to Track > Regular* (or *Special*) and *Snap Wire to Following Objects > Pin*, the software has the following behavior:
	  ◦ If the wire will fall partially outside the pin when snapped to a track, it snaps to the pin.
	  ◦ If the wire will fall inside the pin when snapped to a track, it snaps to both the pin and a track.
	  ◦ If there is no track on the pin, the wire snaps to the pin.
	
	Note: If you do not want to snap wires to any object, deselect all the options in this section.

Align Wire with Pin	Specifies how to align with a pin when ending a route. Select one of the following: • *Auto* - The software determines alignment automatically. • *Center* - Snaps wires to the center of the pin. • *Low* - Snaps wires to the bottom of vertical pins or to the left side of horizontal pins. • *High* - Snaps wires to the top of vertical pins or to the right side of horizontal pins. **Note**: To ensure proper alignment, do not snap any object to track. That is, deselect all the options in the *Snap Following Objects to Track* section. *Default: Auto*
Snap the End of Wire to Manufacturing Grid	Snaps the end of an off-grid wire being drawn to the manufacturing grid. *Default*: Deselected
Snap the End of Regular Wire to Track	Snaps the end of regular wires to track. For a long multi-pin net, you might want to draw the trunk wire first and then draw the branch wires along the trunk wire. The start/end points of the trunk wire are usually not on pins. So if the trunk wire start/end points do not snap to the track, it will leave an off-grid wire segment. To prevent this, snap the end of regular wires to track by selecting the *Snap the End of Regular Wire to Track* check box. The start/end points of the regular wire will snap to the closest orthogonal layer preferred track. *Default*: Deselected
Snap the End of Special Wire to Track	Snaps the end of special routes to track. For a long multi-pin net, you might want to draw the trunk wire first and then draw the branch wires along the trunk wire. The start/end points of the trunk wire are usually not on pins. So if the trunk wire start/end points do not snap to the track, it will leave an off-grid wire segment. To prevent this, snap the end of special routes to track by selecting the *Snap the End of Special Wire to Track* check box. The start/end points of the special route will snap to the closest orthogonal layer preferred track. *Default*: Deselected

Snap Bus to Pin	Specifies whether or not to change wire width, spacing, and order according to the connected pin. This option supports macro to IO pin snapping as well as IO pin to IO pin snapping. For details on how this setting works and its limitations, see the description for the `setEditMode -snap_bus_to_pin` option in the *Innovus Text Command Reference.* *Default*: Deselected
Via Snapping	
Snap to Track Intersection	Controls whether to snap vias to the intersection of wires on the same net or to the manufacturing grid: • When *Snap to Track Intersection* is selected, the tool snaps the via to the center of the intersection of wires on the same net. • When *Snap to Track Intersection* is deselected, the tool keeps the via in the location where it is added or moved, snapping only to the manufacturing grid. *Default:* Selected
Snap to Track with Same Color	Specifies whether or not to snap the via automatically to a track with the same color. *Default:* Selected
Snap to Wire Intersection	Specifies whether to snap vias to the intersection of wires. *Default:* Selected
Trim Snapping	

Snap to Trim Grid	Specifies whether or not the trim metal should snap to the closest trim grid during trim-metal editing. If you deselect this check box, the trim metal is drawn centered on the location specified while adding trim metal.  **Note**: This option does not affect wire move operations. *Default:* Selected

Stretch

Click this option to stretch or shrink wires.

- Choose *Edit - Wire - Stretch*.

This opens the Edit Route form.

Related Topics

For more information, see the "Stretching Wires" section of the Editing Wires chapter in the *Innovus User Guide*.

Add Via

Use the Edit Via form to add and modify vias. Use one of the following methods to place the software in add via mode:

- Choose *Edit - Wire - Add Via*.
- Click the *Add Via* widget on the Tools list and then press the `F3` key.

- Use the o keyboard shortcut and then press the F3 key.

The Edit Via form has two versions, depending on which via creation option you select:

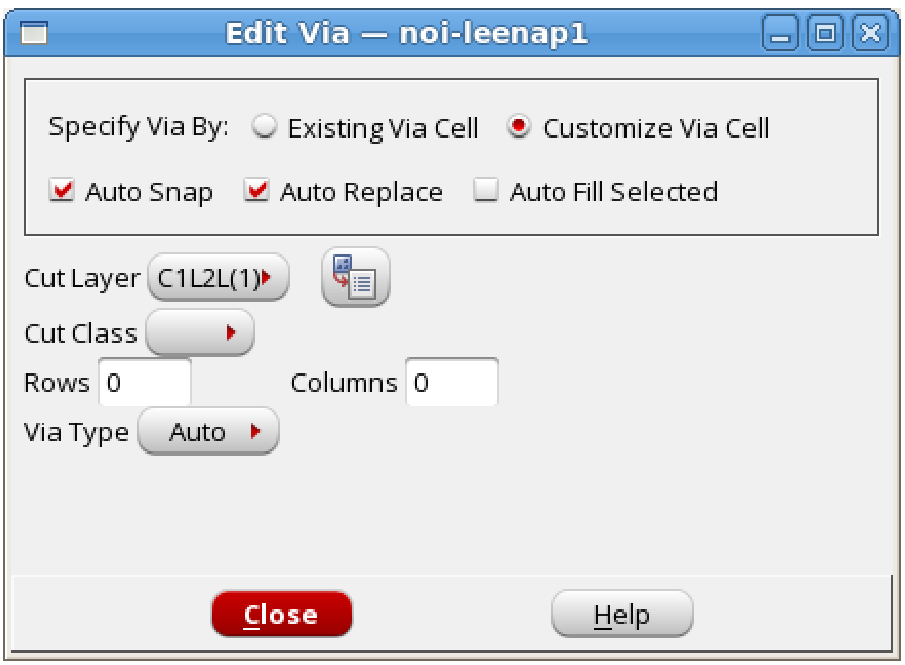
- Existing Via Cell
- Customize Via Cell

Note: You can replace a via by using the Replace Via form.

Edit Via - Customize Via Cell

Use the Edit Via - Customize Via Cell form to add or modify vias based on the cut class.

- Click the *Add Via* widget and then press the F3 key and then select *Customize Via Cell* in the *Specify Via By* section.
  Or
- Choose *Edit - Wire - Add Via* and then select *Customize Via Cell* in the *Specify Via By* section.



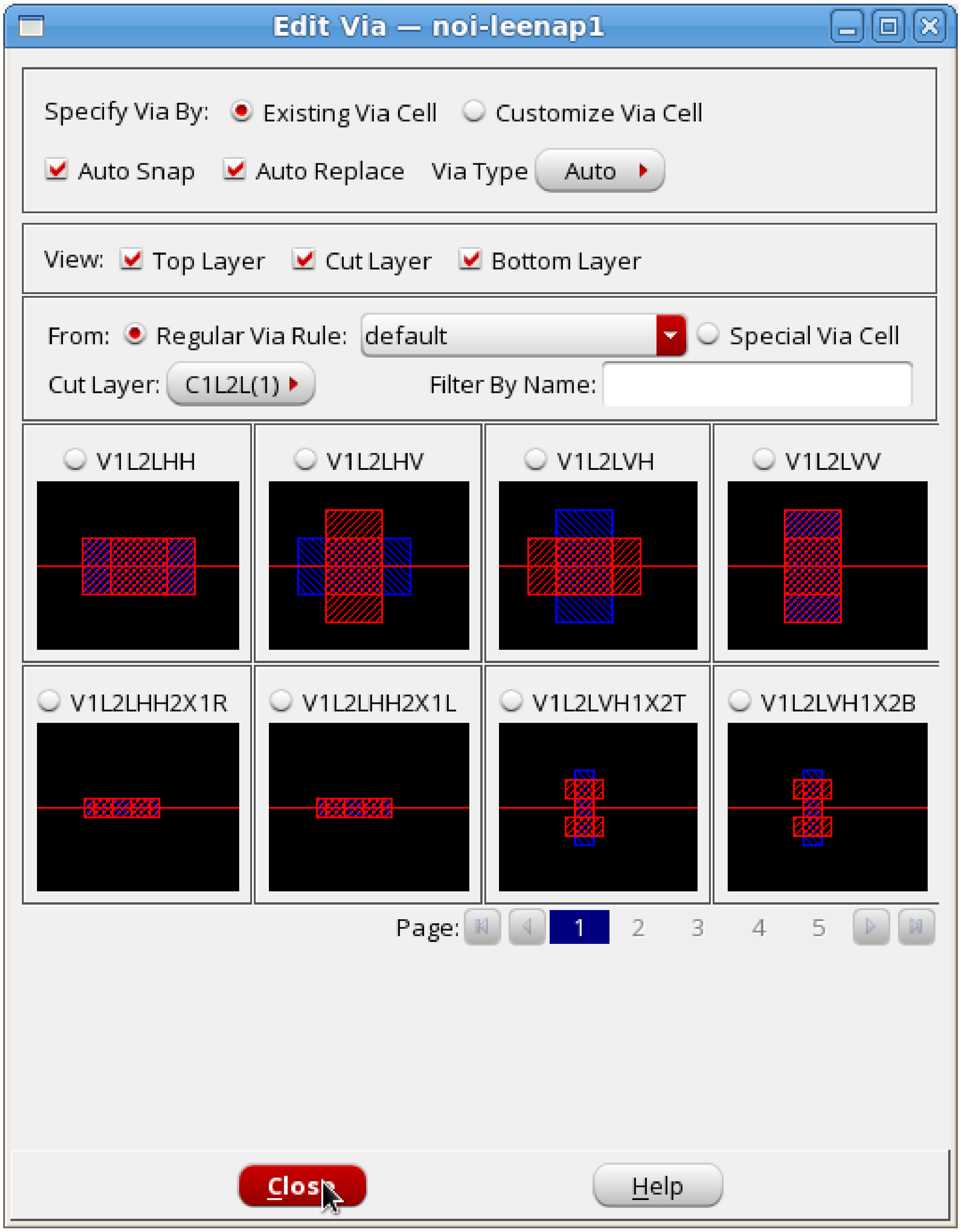
Edit Via - Customize Via Cell Fields and Options

Auto Snap	Snaps vias to the center of the intersection of wires on the same net. This is the default. If deselected, the via stays in the location where it is added or moved, snapping only to the manufacturing grid.
Auto Replace	Determines whether existing vias are replaced with new ones in case of overlap. By default, existing vias are replaced with the new ones in case of any overlap. If you deselect this check box, existing vias are retained even if there is some overlap with the new vias being added.
Auto Fill Selected	When turned on, the *Cut Layer* field is dynamically updated whenever you change your selection in the GUI. Default: Off
Cut Layer	Specifies the layer for the via. Choose a cut layer name from the drop-down menu. Alternatively, click the *Copy From Selected* button to select the layer of the selected via.
Cut Class	Specifies the cut class name of the vias.
Rows	Specifies the number of horizontal cuts for the via.
Cols	Specifies the number of vertical cuts for the via.
Via Type	Specifies the type of the via to be created, *Regular* or *Special*. *Default*: *Auto*

Edit Via - Existing Via Cell

Use the Edit Via - Existing Via Cell form to add or modify a via such that it has the same geometry as a specific cell. The specific cell could be based on a regular via rule or could be a special via cell.

- Click the *Add Via* widget and then press the `F3` key and then select *Existing Via Cell* in the *Specify Via By* section.
  Or
- Choose *Edit - Wire - Add Via* and then select *Existing Via Cell* in the *Specify Via By* section.



Edit Via - Existing Via Cell Fields and Options

Auto Snap	Snaps vias to the center of the intersection of wires on the same net. This is the default. If deselected, the via stays in the location where it is added or moved and snaps to the manufacturing grid.

Auto Replace	Determines whether existing vias are replaced with new ones in case of overlap. By default, existing vias are replaced with the new ones in case of any overlap. If you deselect this check box, existing vias are retained even if there is some overalp with the new vias being added.	
Via Type	Specifies the type of the via to be created, *Regular* or *Special*. *Default*: *Auto*	
View	Provides the following options	
	Top Layer	Specifies whether to display top layer of the via. *Default*: On
	Cut Layer	Specifies whether to display cut layer of the via. *Default*: On
	Bottom Layer	Specifies whether to display bottom layer of the via. *Default*: On
From		
	Regular Via Rule	Specifies the rule for the selected regular via. You can choose a different rule, including a non-default rule (NDR), from this drop-down list.
	Special Via Cell	Specifies special via cells for selection and display.
Cut Layer	Specifies the layer for the via cut. Choose a cut layer name from pull-down menu. Depending on the cut layer chosen, the list of via cells displayed as thumbnails in the *Viacell Thumbnails Area* changes.	
Filter By Name	Specifies the text string for matching via names to narrow down the viacell list.	
Viacell Thumbnails Area	Displays thumbnails of all the viacells that match the filtering criteria.	

Related Topics

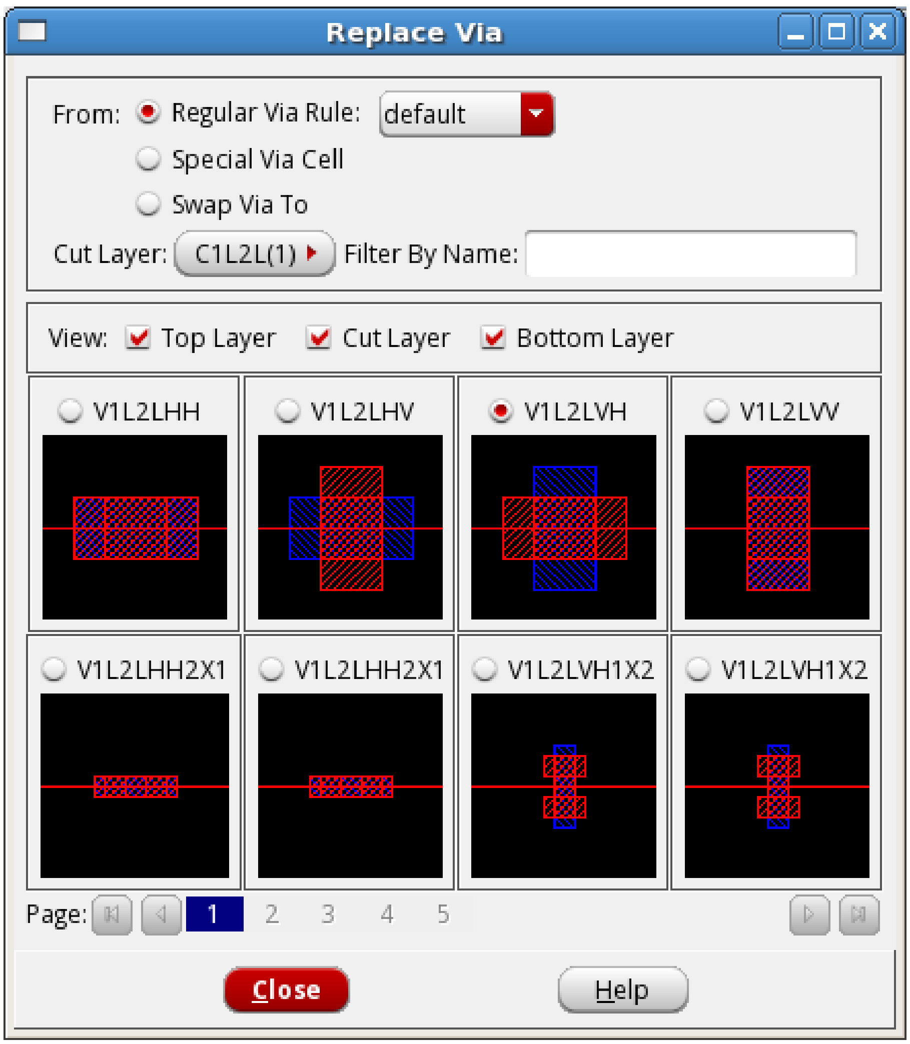
For information on the following topics, see Editing Wires in the *Innovus User Guide*.

- Adding Vias

Replace Via

You can replace a selected via with another one. To replace a via:

1. Select the via to change.
2. Press the `F4` key. This brings up the Replace Via form.



3. Use appropriate filtering options as per your requirements to update the list of via cell

thumbnails.

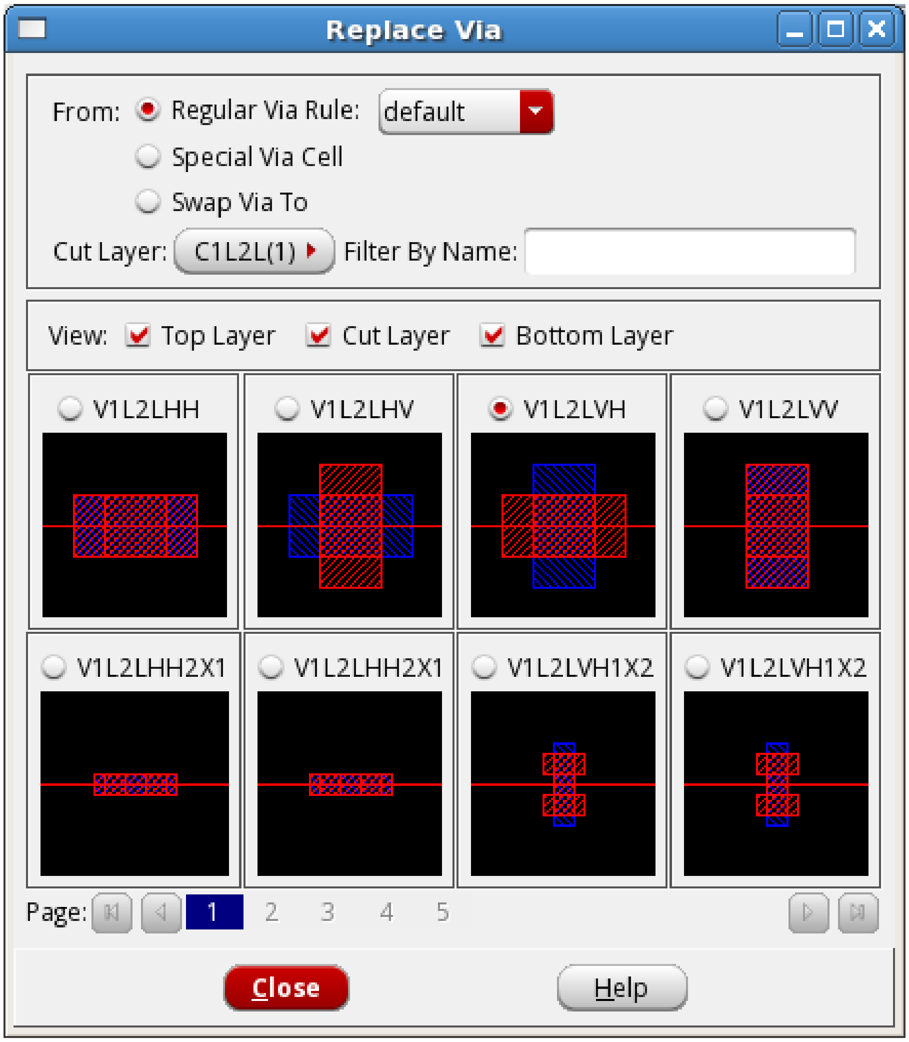
4. Select the via with which you want to replace the current via by clicking the corresponding via name in the *Viacells Thumbnail Area.*
5. Click Close.

The *From* section in the Replace Via form provides three options for specifying the vias to be replaced:

- *Regular Via Rule*
- *Special Via Cell*
- *Swap Via To*

Regular Via Rule

Specifies the rule for the selected regular via. You can choose a different rule, including a non-default rule (NDR), from this drop-down list.

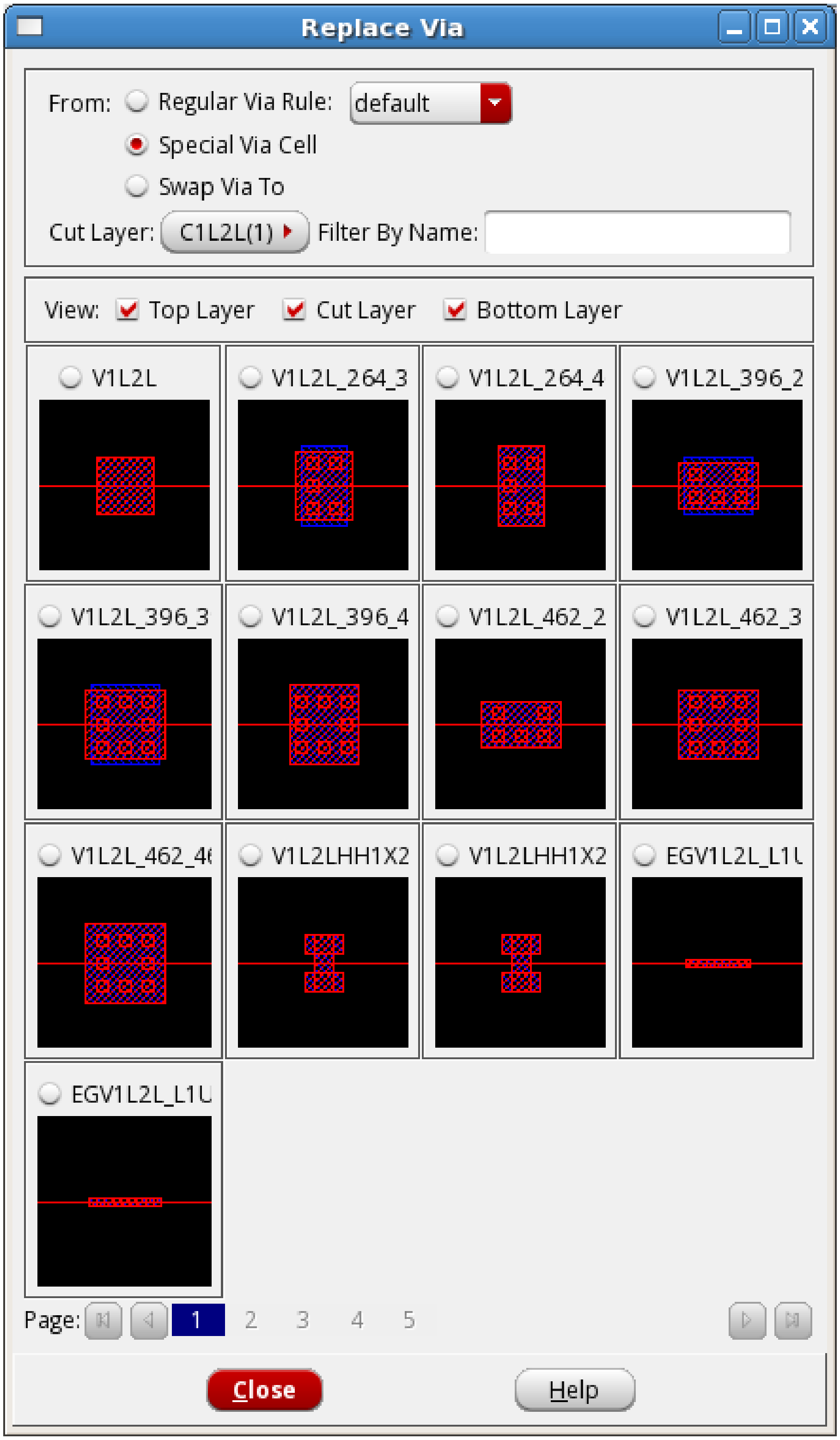


Cut Layer	Specifies the layer for the via cut. Choose a cut layer name from pull-down menu. Depending on the cut layer chosen, the list of via cells displayed as thumbnails in the *Viacell Thumbnails Area* changes.	
Filter By Name	Specifies the text string for matching via names to narrow down the viacell list.	
View	Provides the following options	
	Top Layer	Specifies whether to display top layer of the via. *Default*: On
	Cut Layer	Specifies whether to display cut layer of the via. *Default*: On

	Bottom Layer	Specifies whether to display bottom layer of the via. *Default*: On
Viacell Thumbnails Area	Displays thumbnails of all the via cells that match the filtering criteria, including the specified rule. The name of each viacell is displayed on top of the via thumbnail.The via you selected before opening the Replace Via form appears preselected in the *Viacell Thumbnails Area*. You can choose another via from the thumbnail list to replace the current via by clicking the corresponding via name.	

Special Via Cell

Specifies special via cells for selection and display.



The fields and options in this tab are the same as on the *Regular Via Rule* tab.

Swap Via To

Specifies cut pattern for the replacement via.

Rows	Specifies the number of rows in the replacement via. *Default*: 1
Columns	Specifies the number of columns in the replacement via. *Default* : 1

Add Polygon

Select this option to change the cursor to a pencil when on the design area. You can use this pencil at the start point of the polygon and move the cursor in the main window. Click once for each turn. Backspace to cancel the last point in the wire and double-click to commit the wire.

- Choose *Edit - Wire - Add Polygon*.

Add Polygon - Fields and Options

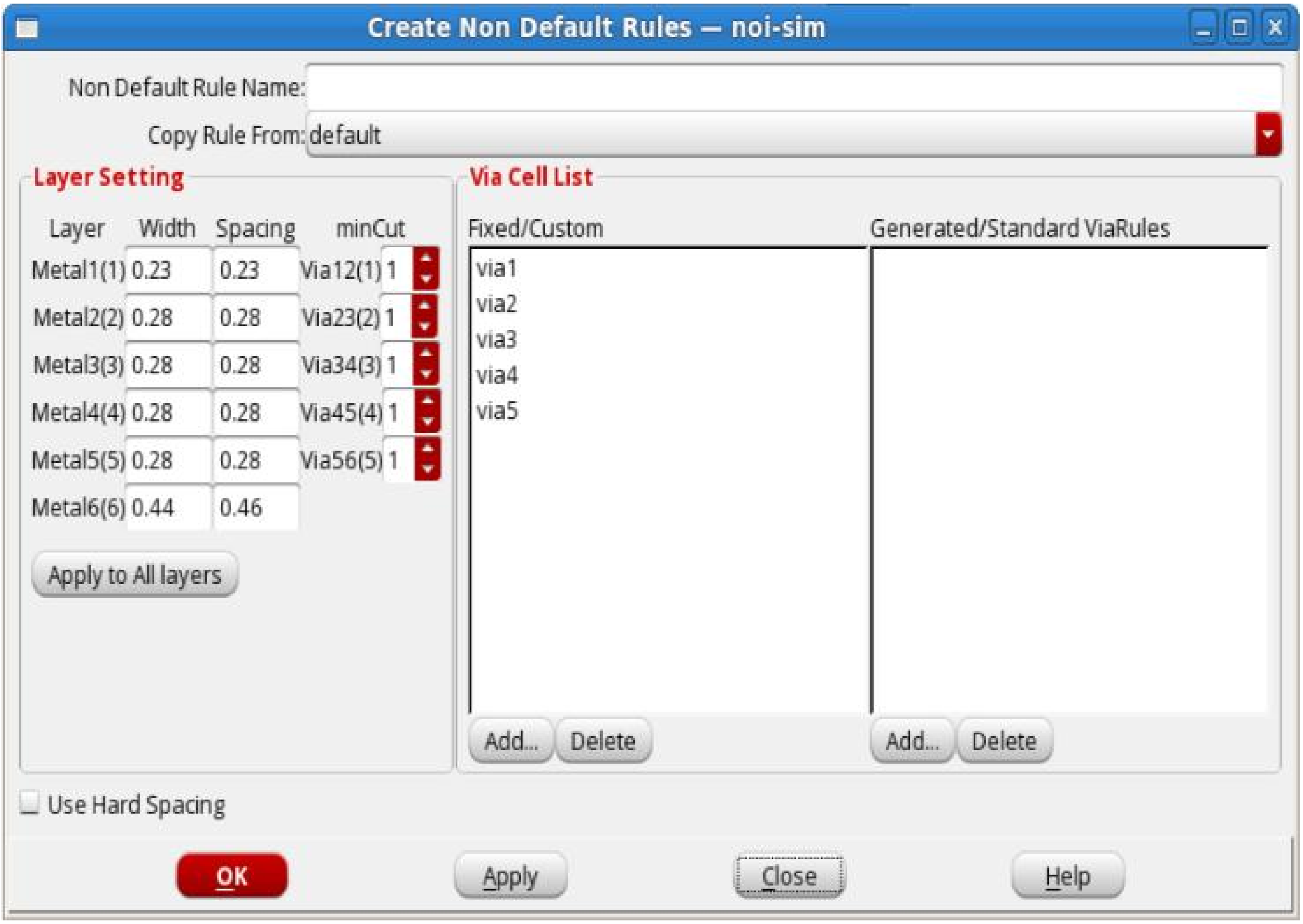
Polygon Net	Specifies the polygon net.
Polygon Layer	Selects the metal layer for the polygon net.

Create Non Default Rule

Use the Create Non Default Rules form to define non-default rules for objects.

Note: You cannot create non-default rules for diagonal width, wire extension, via rule and minimum cuts.

- Choose *Edit - Create Non Default Rule.*



Note: You cannot specify a non-default rule for creating a new via.

Fields and Options

Non Default Rule Name	Specifies the name of the non default rule.
Copy Rule From	Specifies the default rule that is copied from an existing LEF technology.
Layer	Displays the names of the metal layers.

Width	Specifies the width, in microns, of each metal layer.	
Spacing	Specifies the spacing, in microns, between two metal layers.	
minCut	Specifies the min cut limit for via layers.	
Apply to All Layers	Applies the settings specified for the first layer to all other layers.	
Via Cell List	Displays the list of the via cells from the current editing rule.	
	Fixed/Custom	Specifies the via cells that have the `DEFAULT` keyword against the via names. These via cells are mainly used by signal routes. Click the *Add* button below this text box to open the Add Via Cell form to select the via cells to be added. Use the *Delete* button below the *Fixed/Custom* text box to delete the selected via cell from the text box.
	Generated/Standard Via Rules	Specifies the VIA cells that do not have the `DEFAULT` keyword against the via names. The tool usually generates its own via based on these rules. Examples of these kinds of vias are non-default vias and power vias. Click the *Add* button below this text box to open the Add Via Rule form to select the via rules to be added. Use the *Delete* button below the *Generated/Standard Via Rules* text box to delete the selected via rule from the text box.
Use Hard Spacing	Specifies hard spacing between the metal layers. When this option is selected, the routor honors NDR spacing even if the design is congested. Typically, the spacing rules for NDR are considered soft, meaning that the router honors the spacing only if the design is not congested. If the design is congested, the router does not honor soft spacing rules	

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `add_ndr`
- `exportNdr`

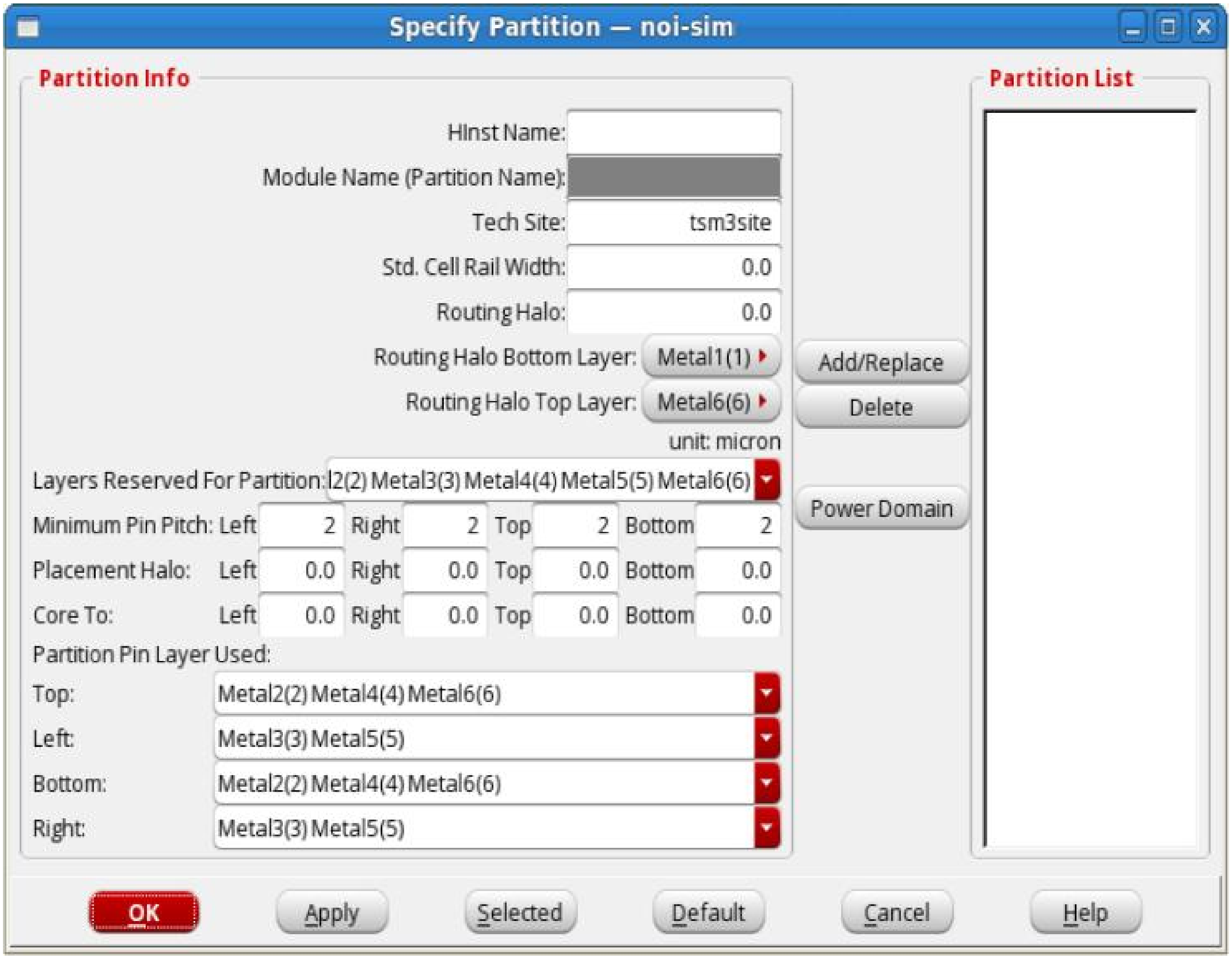
5

Partition Menu

Specify Partition

Use the Specify Partition form to designate partitions. Before specifying a module or sub-module as a partition, you must move the module into the core area.

- Choose Partition - Specify Partition



Specify Partition Fields and Options

HInst Name	Specifies the instance name of a module that is to become a partition. A module must correspond to a single module, regardless of its level in the netlist hierarchy. **Important:** A partition cannot have another partition as its ancestor or descendant.
Module Name (Partition Name)	
	The name of the hierarchical instance module is taken as the name of the partition.

Tech Site	Specifies the technology site name. The partition will have the same site as the top-level design. If the specified hierarchical instance is also a power domain, then the corresponding power domain row structure is displayed.
Std. Cell Rail Width	Specifies the standard cell power rail width, in micrometers. If partition pins are not allowed above power or ground rail width, enter the dimension of the power rail width. If a value of 0.0 is entered (the default), the width from the Technology file will be used. If partition pins are not allowed above power and ground rails, select Disallow pins above power/ground rails in the Partition form.
Routing Halo	Specifies routing spacing, in micrometers, around the sides of the partition. Routing on the specific routing layers in this area will be considered as high cost. The router can, however, perform routing perpendicular to the pins. You can specify a positive or a negative value for the routing halo. A positive value means that the halo will be outside the partition. A negative value means that the halo will be applicable during block implementation, inside of the partition. The same value is used for all sides of the partition. **Note:** For instance blocks- Edit Halo blackboxes, hard macros or block-level designs-specify the routing halo through the *Edit Halo* form or through the `addRoutingHalo` command. Also, for bottom-up hierarchical flow, specify routing halo for a block at the top-level design or at the block-level design through the *Edit Halo* form or through the `addRoutingHalo` command.
Routing Halo Bottom Layer	Specifies the bottom partition layer for which routing halo will be created. *Default*: By default, the bottom layer reserved for the partition is used
Routing Halo Top Layer	Specifies the top partition layer for which routing halo will be created. *Default*: By default, the top layer reserved for the partition is used.

Layers Reserved for Partition	Specifies the selected metal layers that are used for routing in the partition and generating partition pins. Any unselected metal layers, usually the top-most metal layers, are allowed to route over the partition. When saving the partition, the LEF generated for this partition will have routing blockages on their layers so that the top-level router is aware of which metal layers are being used in the partition
Minimum Pin Pitch	Specifies the pin pitch dimension for the *Left*, *Right*, *Top*,and *Bottom* partition sides. The default is 2, which places one pin for every two metal tracks. The actual pin pitch depends on the pin's metal layer. **Note:** The Partition Pin Guide floorplan object will supersede this entry and use the Min. Space entry in the object's Attribute Editor.
Placement Halo	Specifies extra spacing, in micrometers (around the left, bottom, right and top sides respectively) of the partition that should not be used for placement. The placement program will not place standard cells in the area for partition placement. This spacing is called placement halo. At the top-level design, this information is saved as part of the partition section in a floorplan file. This information is also saved in a partition floorplan file when saving partitions. By default, the value is 0 for all the sides. If the hierarchical instance was earlier defined as a power domain, then this field corresponds to the minimum gap parameter of the power domain.
Core to Left *Core to Right* *Core to Top* *Core to Bottom*	Specifies the space, in micrometers, between the module boundary and core design area of the partition module. The partition pins will be located at the partition instance boundary and the core area. The placement program will not place standard cells in this area for partition placement. If the specified hierarchical instance is also a power domain, then these fields will have the same value as the power domain.

Partition Pin Layer Used	Specifies the metal layers from the defaults. The default metal layers correspond to the sides of the partition, where the vertical metal layers (for example, *Metal*2(2) , *Metal*4(3), and so on) are for the Top and Bottom sides, and horizontal metal layers (for example, *Metal*3(3) , *Metal*5(5) , and so on) are for the Left and Right sides of the partition. Deselecting all metal layers for a side of a partition prevents pins from being created for the entire side of that partition. These deselected layers overwrite the *Partition Pin Layer* selection, used when clicking Add/ Replace . **Note:** The initially displayed pin layers are the layers that are specified in the LEF or technology file.
Add/Replace	Updates the partition constraint information and adds it to the Partition List .
Delete	Removes highlighted entries in the Partition List .
Power Domain	Opens the Power Domain form to designate a power domain as a partition. If the specified hierarchical instance is also a power domain, the corresponding power domain information will be available. See Power Domain for more information.
Partition List	Lists the specified partitions. To change the order of the partitions in the list, click the left mouse button on the partition name and drag it to its new area.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `definePartition`

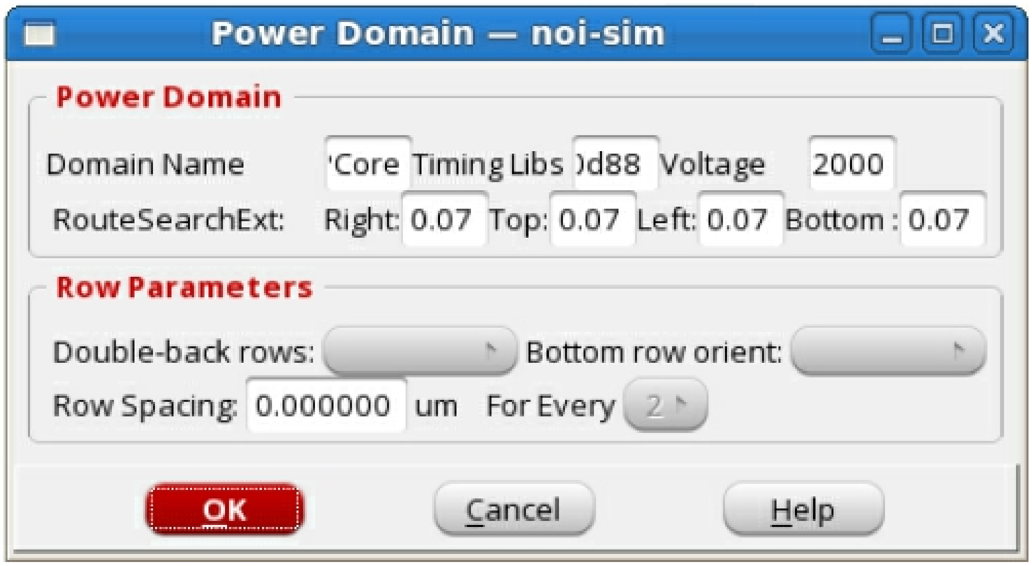
Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Power Domain

Use the Power Domain form to designate a power domain as a partition.

Clicking the *Power Domain* button in the Specify Partition form opens the Power Domain form.



Power Domain Fields and Options

Domain Name	Specifies the name of the partition to become a power domain.
Timing Libs	Specifies the name of one or more timing libraries to associate with the power domain. To choose a timing library, use the Specify Timing Libraries form. For information about using this form, see Power Menu .
Voltage	Specifies the voltage information for the power domain. **Note:** You cannot enter a value in this field. This field is populated with values obtained when you use the *Specify Timing Libraries* form. For more information, see Power Menu.
RouteSearchExt	(Optional) Specifies a distance, in microns, that limits the search for legal targets by the power planning and routing software beyond the power domain boundary. This prevents unwanted connections to targets of the same net that are not associated with the power domain.
Double-back rows	Allows the selection of standard cell row pair orientations. The orientation selections for the row pair are bottom-to-bottom or top-to-bottom. The default is bottom-to-bottom orientation.
Bottom row orient	Specifies the orientation of the bottom row in the core area. The default is an `R0` orientation, or you can choose the `MX` orientation (mirrored through the x axis).
Row Spacing for Every # rows	
	Specifies the standard row spacing, in micrometers. This must be a positive value. By default, this value is zero. In the *For Every Row* pull-down menu, specify *1* for every row, or *2* for every other row.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `modifyPowerDomainAttr`

Related Topics

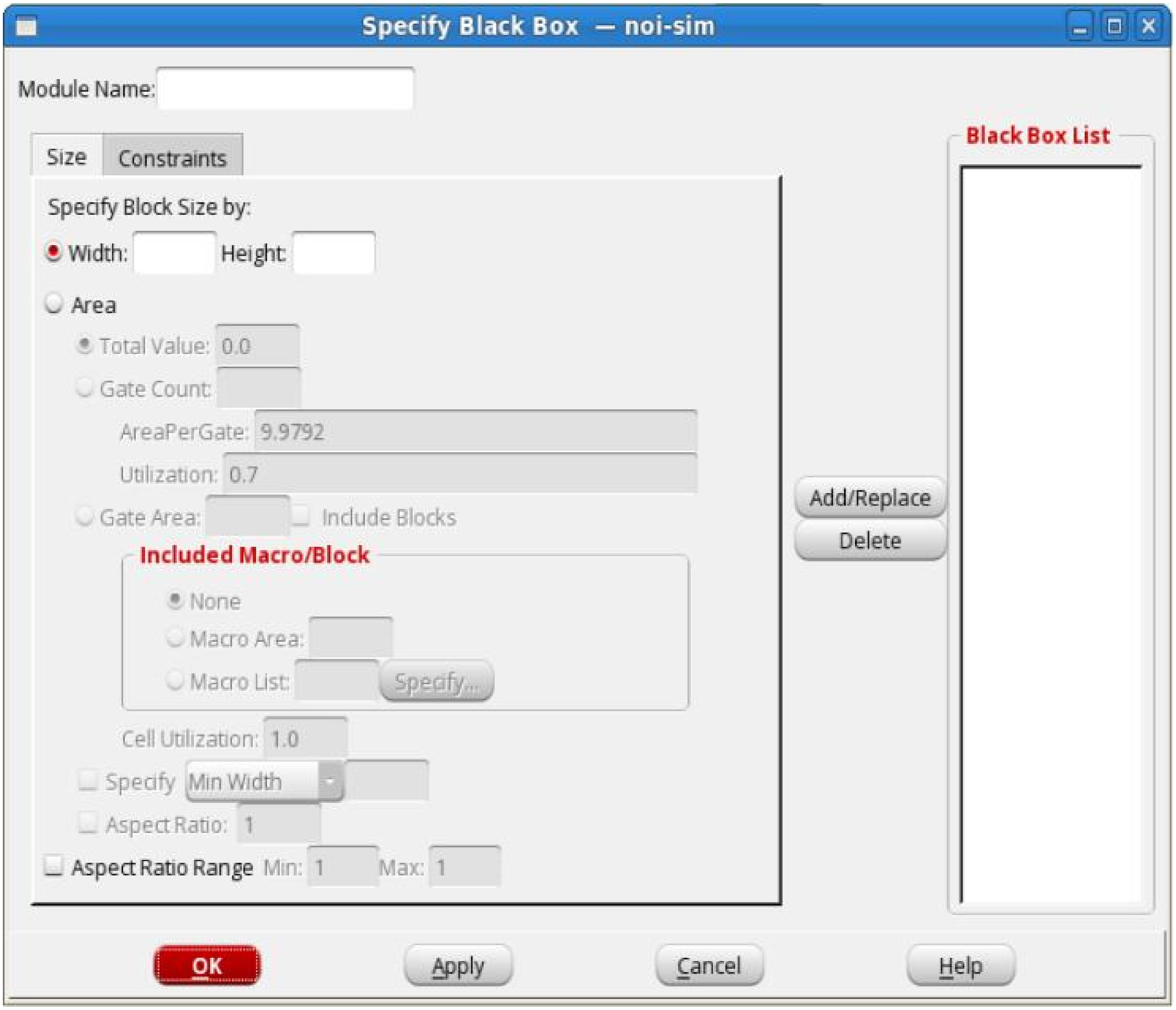
For information on the following topics, see "Low Power Design" in the *Innovus User Guide* .

- Multiple Supply Voltage Flat Flow
- Creating a Rectilinear Power Domain

Specify Black Box

Use the Specify Black Box form to specify which modules will be regarded as blackboxes.

- Choose *Partition* - *Specify Black Box.*



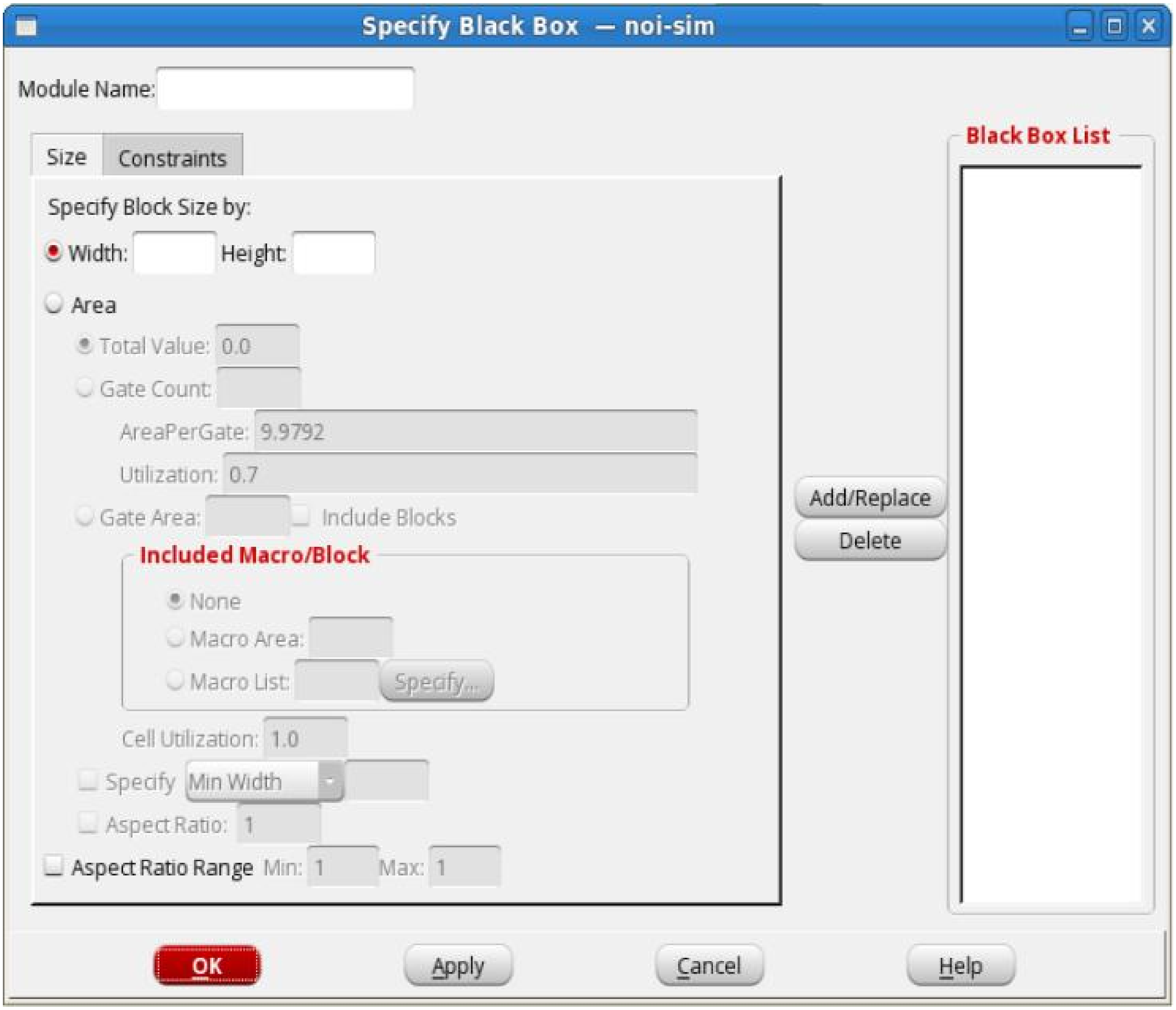
The *Specify Black Box* form contains the following pages:

- Specify Black Box
- Constraints

Size

Use the *Size* page to specify the area, macros to include, and target utilization for the blackbox.

- Choose *Partition - Specify Black Box* and then click the *Size* tab.



Size Fields and Options

Module Name	Specifies a module name or leaf cell name that is defined in the netlist to be treated as a blackbox. For the modules that are not empty, the content information of this module is not expanded in the data structure to reduce the used memory.

Width, Height	Specifies fixed width and height of a specified module, in micrometers.	
Area	Specifies that the blackbox will be sized by area.	
Total Value	Specifies area value in square micrometers. If you specify the block size area, the default created block aspect ratio is 1.	
Gate Count	Specifies a gate count value. The total cell area is equal to the specified gate count multiplied by the specified area per gate. This field has no default value.	
AreaPerGate	Specifies an area per gate value in square micrometers. The default value is three times (3x) the area of the standard cell site.	
Utilization	Specifies the cell utilization. This value derives the area that is reserved for routing. The final block size is equal to the total cell area plus the routing area. The default value is 0.7 (70 percent).	
Gate Area	Specifies the gate area.	
Include Blocks	Specifies that the gate area includes the macro area. If the *Include Blocks* option is not selected, the final gate area for the blackbox is derived by adding the area of the hard macro(s) to the gate area specified in the *Gate Area* field. If the *Include Blocks* option is selected, the specified gate area also includes the area of the specified hard macro(s). *Default:* Off.	
Included Macro/Block		
	None	Specifies that no macros or blocks are included.
	Macro Area	
		Specifies the total area of the macro(s) in square microns. This value is added to the total gate area.

<table>
<tr><td></td><td colspan="2">Macro List</td></tr>
<tr><td></td><td></td><td>Specifies the hard macro(s) to include in the blackbox. Enter the name of the macro followed by the number of times the macro will be instantiated in the blackbox. You can specify more than one blackbox. For example, to specify the macro <code>RAM_128x16A</code> two times and the macro <code>pllclk</code> one time, enter the following in the Macro List field:

<code>RAM_128x16A 2 pllclk 1</code>

You can also select the macros from a list of available macros. For this, click the Specify... button and enter the details in the Specify Macros form that appears. For more information, see Specify Macros .</td></tr>
<tr><td>Cell Utilization</td><td colspan="2">Specifies the cell utilization. This value is used to derive the area of the blackbox, which is calculated using the following formula:

<code>Blackbox area = (standard cell area / cell utilization) + macro area</code>

Default : The default value of cell utilization is 1 (100%).</td></tr>
<tr><td>Specify</td><td colspan="2">Specify the value for the Min Width, Min Height, Fixed Width , Fixed Height of the module.</td></tr>
<tr><td>Aspect Ratio</td><td colspan="2">Specifies the aspect ratio value of its width divided by its height (x/y). This value combined with the specified related area information determines the necessary width and height of a blackbox.</td></tr>
<tr><td>Aspect Ratio Range</td><td colspan="2">Specifies the Min and Max values for the aspect ratio range. This value combined with the specified related area information enables the blackbox to be reshaped while maintaining the current area.</td></tr>
<tr><td>Add/Replace</td><td colspan="2">Adds the new specified module as a blackbox with its block size information to the Black Box List . If you modify the block size of a given module that is already specified as a blackbox, click the Add/ Replace button to update the block size information.</td></tr>
<tr><td>Delete</td><td colspan="2">Deletes a selected blackbox in the Black Box List and its specified constraints.

Note: You cannot delete a blackbox if it is a cell that has no physical macro definition.</td></tr>
</table>

Black Box List	Lists all the blackbox modules, if available. You can highlight a module entry field name to populate the *Module Name* and block size information. For a blackbox that already has pin assignment, if you change its size, the Innovus software will change the blackbox size and un-assign all the pins.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `specifyBlackBox`
- `unspecifyBlackBox`

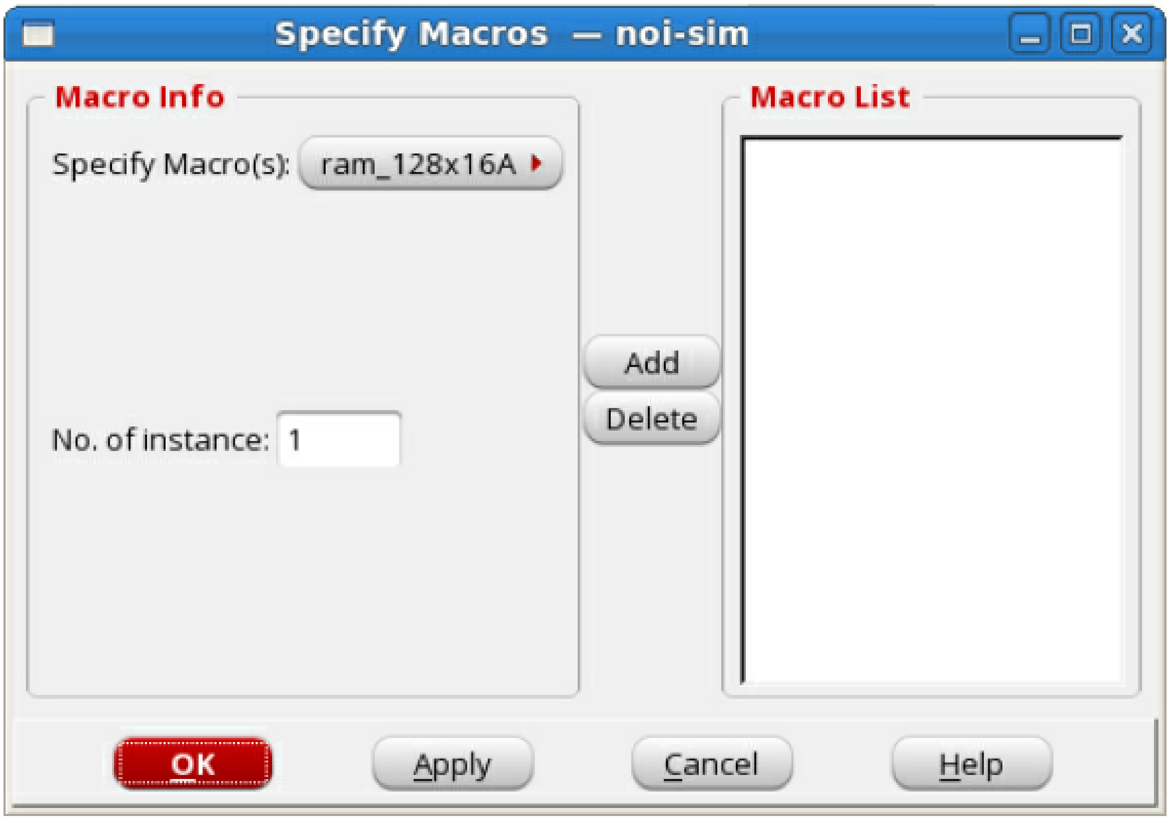
Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Specify Macros

Use the Specify Macros form to select the hard macro(s) whose area(s) will be included while calculating the total gate area of the blackbox.

- Choose *Partition - Specify Black Box* , and then click the *Specify...* button, which is located next to the *Macro List* option.



Specify Macros Fields and Options

Specify Macro(s)	Displays the macros from a list of the available macros. To specify a macro whose area should be included while calculating the total area of the blackbox, select the macro and click the *Add* button.
No. of Instances	Specifies the number of times the macro is referenced. Thus, by specifying a value for count, you avoid repeating the macro names for macros that are referenced multiple times. *Default* : The default value is `1`.
Add	Adds the macro selected in the *Specify Macro* field to the *Macro List* field.
Delete	To remove a macro from the *Macro List* field, select the macro in the *Macro List* field and click the `Delete` button.
Macro List	Displays the list of macro(s) whose area(s) will be included while calculating the total gate area of the blackbox.

Related Text Commands

The following text command provides equivalent or additional functionality:

Related Text Commands

The following text command provides equivalent or additional functionality:

- `create_blackbox`
- `InnovusMR_unspecifyBlackBox`

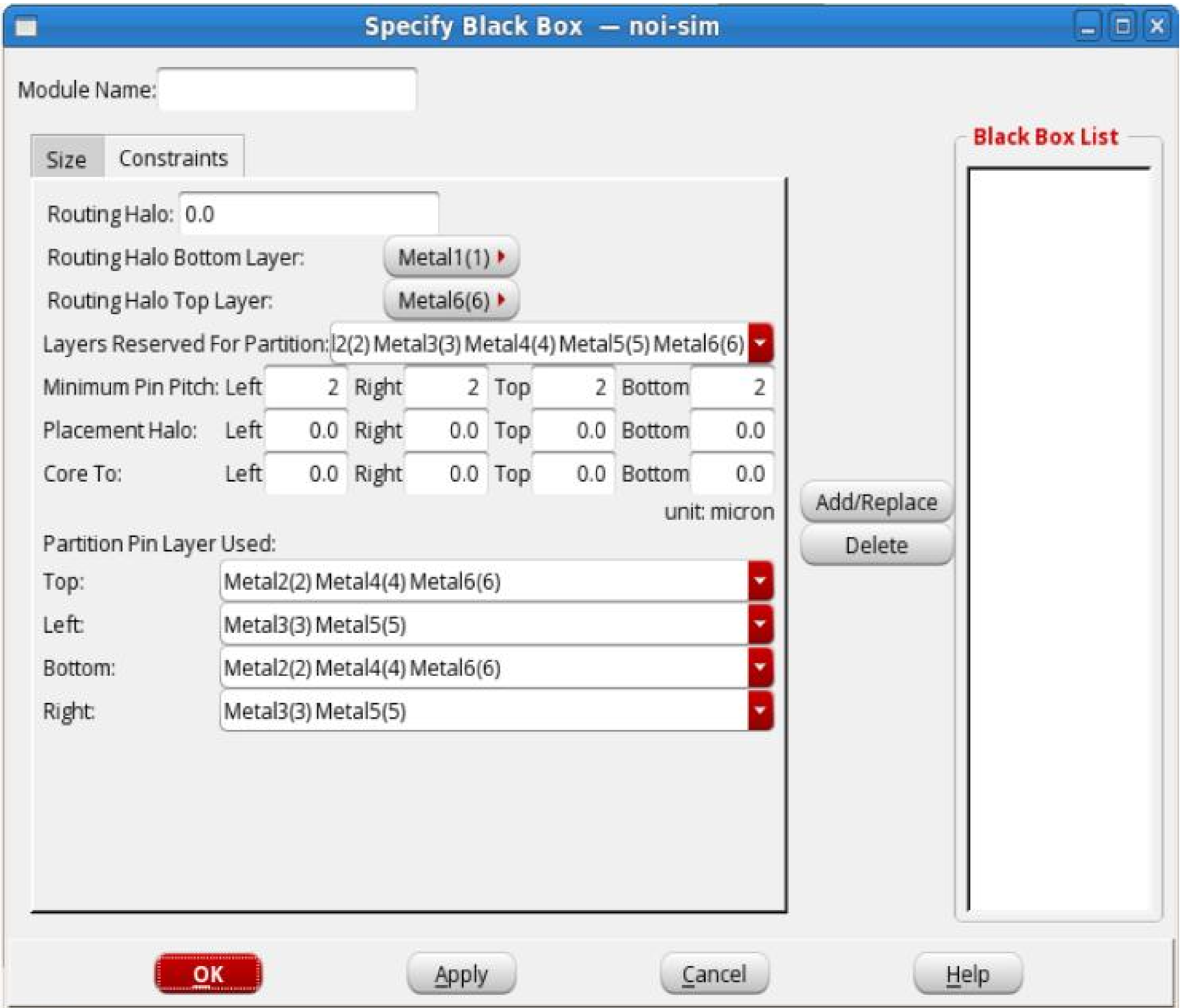
Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Constraints

Use the *Constraints* page to specify blackbox constraints such as reserved routing layers, pin layer, and pin spacing.

- Choose *Partition - Specify Black Box* and then click the *Constraints* tab.



Constraints Fields and Options

Module Name	Specifies a module name or leaf cell name that is defined in the netlist to be treated as a blackbox. For the modules that are not empty, the content information of this module is not expanded in the data structure to reduce the used memory.

Routing Halo	Specifies routing spacing, in micrometers, around the sides of the blackbox.
Routing Halo Bottom Layer	Specifies the bottom partition layer for which routing halo will be created. *Default* : By default, the bottom layer reserved for the partition is used
Routing Halo Top Layer	Specifies the top partition layer for which routing halo will be created. *Default:* By default, the top layer reserved for the partition is used.
Layers Reserved For Partition	
	Specifies the selected metal layers that are used for routing in the partition and generating partition pins. Any unselected metal layers, usually the top-most metal layers, are allowed to route over the partition. A normal six-metal layer selection process is *Metal1(1), Metal2(2), Metal3(3), Metal4(4),* and *Metal5(5)* selected, and *Metal6(6)* unselected. When saving the partition, the LEF generated for this partition will have routing blockages on their layers so that the top-level router is aware of which metal layers are being used in the partition.
Minimum Pin Pitch	Specifies the pin pitch dimension for the *Left, Right, Top,* and *Bottom* blackbox sides. The default is 2, which places one pin for every two metal tracks. The actual pin pitch depends on the pin's metal layer.
Placement Halo	Specifies extra spacing, in micrometers (around the *Left* , *Right* , *Top,* and *Bottom* sides respectively) of the blackbox that should not be used for placement. By default, the value is 0 for all the sides.
Core to Left *Core to Right* *Core to Top* *Core to Bottom*	Specifies the space, in micrometers, between the module boundary and core design area of the module on the left, right, top, and bottom sides respectively. The partition pins will be located at the partition instance boundary and the core area.
Partition Pin Layer Used	

	Specifies the metal layers to use for the blackbox. The metal layers correspond to the sides of the partition, where the vertical metal layers (for example, *Metal2, Metal4* , and so on) are for the *Top* and *Bottom* sides, and horizontal metal layers (for example, *Metal3* , *Metal5* , and so on) are for the *Left* and *Right* sides of the blackbox. Deselecting all metal layers for a side of a blackbox prevents pins from being created for the entire side of that blackbox. These deselected layers overwrite the Partition Pin Layer selection, used when clicking *Add/ Replace* . **Note:** The initially displayed pin layers are the layers that are specified in the LEF or technology file.
Add/Replace	Adds the new specified module as a blackbox with its block size information to the *Black Box List* . If you modify the block size of a given module that is already specified as a blackbox, click the *Add/ Replace* button to update the block size information.
Delete	Deletes a selected blackbox in the *Black Box List* and its specified constraints. **Note:** You cannot delete a blackbox if it is an empty module in the netlist, or a cell that has no physical macro definition.
Black Box List	Lists all the blackbox modules, if available. You can highlight a module entry field name to populate the *Module Name* and block size information. For a blackbox that already has pin assignment, if you change its size, the Innovus software will change the blackbox size and un-assign all the pins.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `create_blackbox`
- `InnovusMR_unspecifyBlackBox`

Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Clone Place

Use the *Clone Place* menu command to place all clone instances with relative location and relative orientation according to the master partition instances. It adjusts the instance orientation based on the clone orientation. This is used after running `place_design`.

- Choose *Partition* - *Clone Place* .

Related Text Commands

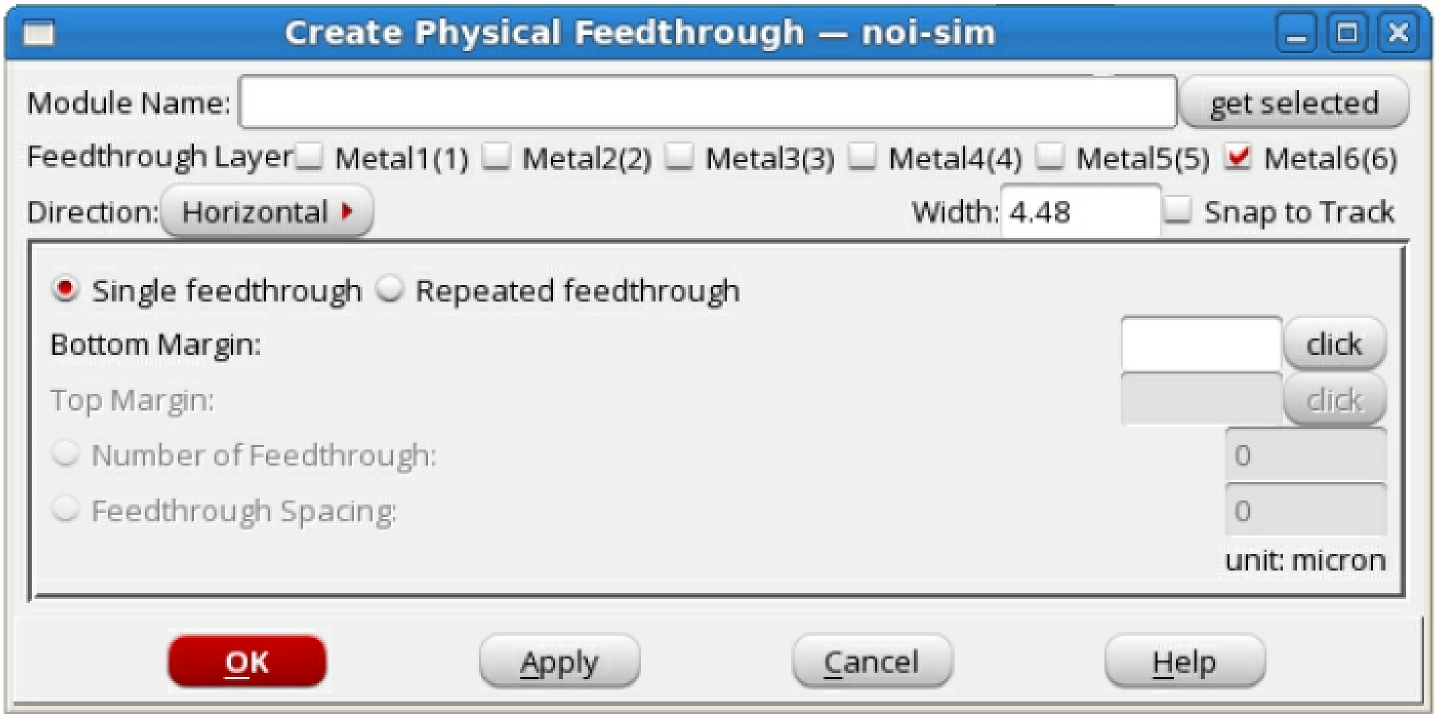
The following text command provides equivalent or additional functionality:

- `clonePlace`

Create Physical Feedthrough

Use the Create Physical Feedthrough form to specify a feedthrough or several feedthroughs on a partition. You can insert feedthroughs in partitions to satisfy timing requirements or accommodate physical constraints. Use this form after specifying the partition(s), but before running the Partition program.

- Choose *Partition* - *Create Physical Feedthrough*


Create Physical Feedthrough — noi-sim
Module Name:
get selected
Feedthrough Layer
Metal1(1)
Metal2(2)
Metal3(3)
Metal4(4)
Metal5(5)
Metal6(6)
Direction:
Horizontal
Width:
4.48
Snap to Track
Single feedthrough
Repeated feedthrough
Bottom Margin:
click
Top Margin:
click
Number of Feedthrough:
0
Feedthrough Spacing:
0
unit: micron
OK
Apply
Cancel
Help

Create Physical Feedthrough Fields and Options

Module Name	Type the module name in the field or highlight the module in the design display area and click *get selected* .
Feedthrough Layer	Specifies the metal layer(s) that can be routed over the feedthrough area. The default is metal layer 8 (*Metal*8), the top-most metal layer.
Direction	Specifies either a *Horizontal* or *Vertical* direction.
Width	Specifies the width of the feedthrough, in micrometers.
Snap to Track	Snaps the feedthrough to a routing track.
Single feedthrough	Creates one feedthrough.
Repeated feedthrough	Creates repeated feedthroughs.
Bottom Margin	With the *Direction: Horizontal* option selected, this specifies the bottom margin for a single feedthrough or repeated feedthroughs.
Top Margin	With the *Direction: Horizontal* option selected, this specifies the top margin for repeated feedthroughs.
Left Margin	With the *Direction: Vertical* option selected, this specifies the left margin for a single feedthrough or repeated feedthroughs.
Right Margin	With the *Direction: Vertical* option selected, this specifies the right margin for repeated feedthroughs.
Number of Feedthrough	Specifies the number of feedthroughs when selecting Repeated feedthrough.
Feedthrough Spacing	Specifies the spacing, in micrometers, between the feedthroughs when selecting Repeated feedthrough.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `createPtnFeedthrough`
- `deleteAllPtnFeedthroughs`

Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Show Wire Crossing

Use the Show Wire Crossing form to display all the nets that have cross-partition routing. The nets that have wire crossing are highlighted in the artwork window. You can use this feature to help you decide whether a net should be a feedthrough net or not.

The Show Wire Crossing form consists of the following two pages:

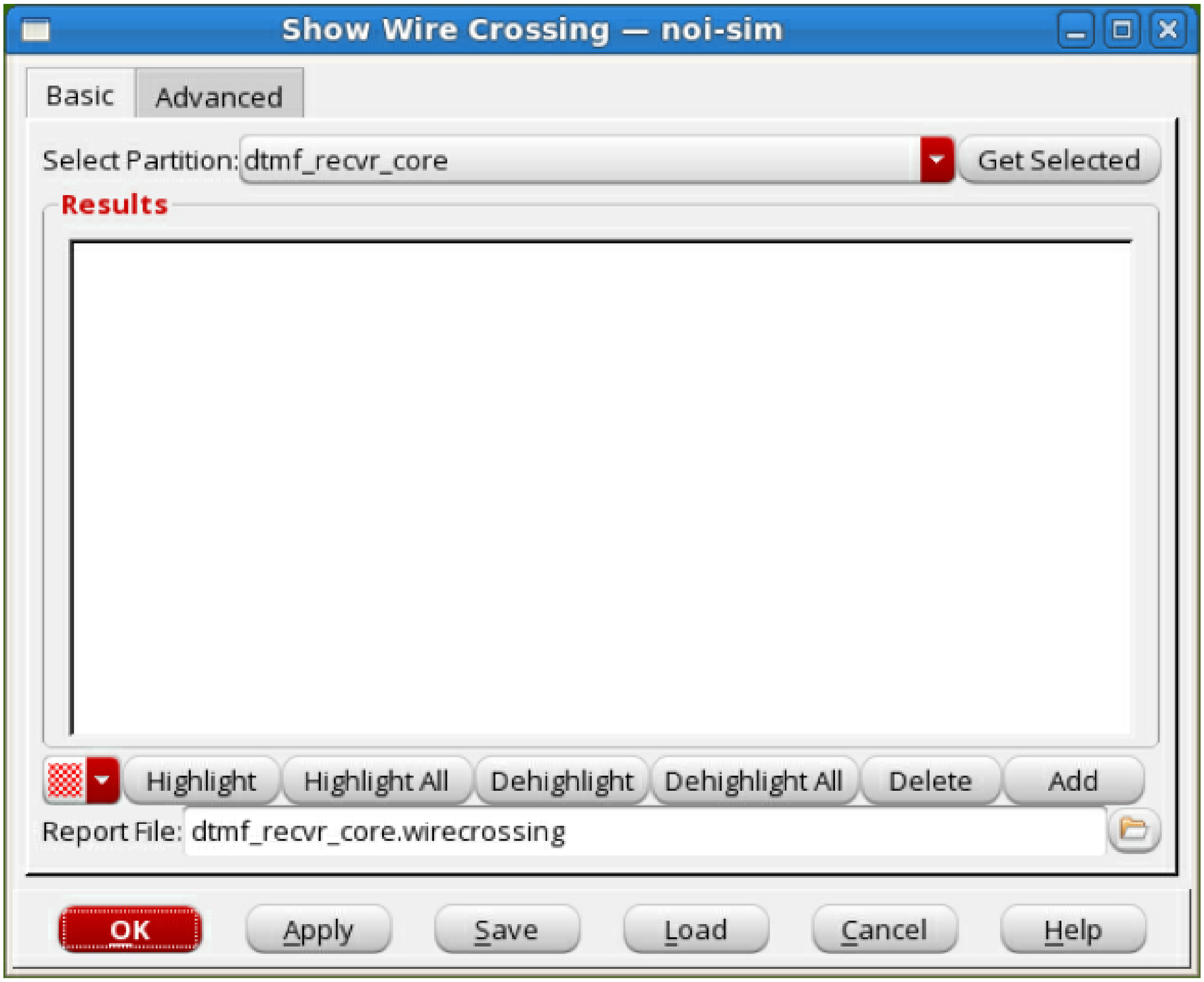
- Show Wire Crossing - Basic
- Show Wire Crossing - Advanced

Show Wire Crossing - Basic

Use the Show Wire Crossing - Basic form to display all the nets that have cross-partition routing. The nets that have wire crossing are highlighted in the artwork window.

You can save the list of nets that have wire crossing in a file, and later use this file as an input file while inserting feedthrough buffers. You can thus use this feature to help you decide which nets should be used as feedthrough nets.

- Choose *Partition - Show Wire Crossing,* and then click on the *Basic* tab.


Show Wire Crossing — noi-sim
Basic
Advanced
Select Partition: dtmf_recvr_core
Get Selected
Results
Highlight
Highlight All
Dehighlight
Dehighlight All
Delete
Add
Report File: dtmf_recvr_core.wirecrossing
OK
Apply
Save
Load
Cancel
Help

Show Wire Crossing - Basic Fields and Options

Select Partition	Displays a list of partitions in the design. Select the partition for which you want to display the nets that cross the partition.
Get Selected	Gets the names of the currently selected partition in the artwork. By default, the current-level design name is displayed.
Results	Displays the nets for the selected partitions. The nets displayed are considered part of the current editing list of nets, which will be saved in the file specified in the *Report File* field.
Highlight	Displays nets that have wire crossing over the specified partition. If the specified partition is a design, the *Results* window displays those nets that have wire crossing over all the partitions in this design.
Highlight All	When you click *Highlight All* , all nets in the Results window are highlighted in the design display area.
Dehighlight	When you click *Highlight* , the nets selected in the Results window are dehighlighted in the design display area.
Dehighlight All	When you click *Highlight All* , all nets in the Results window are dehighlighted in the design display area.
Delete	Deletes the net selected in the Results Window from the Results Window. The deleted net will not be saved in the file specified in the *Report File* field.
Add	Displays the Add Net Names form, which you can use to add nets to the current editing list displayed in the Results Window. The added nets will be saved in the file specified in the *Report File* field. For more information, see Add Net Names .
Report File	Specifies the file in which the current editing list displayed in the Results Window is saved. You can later use this file as an input file while inserting partition feedthrough buffers. You can thus choose which nets should be feedthrough nets.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `showPtnWireX`

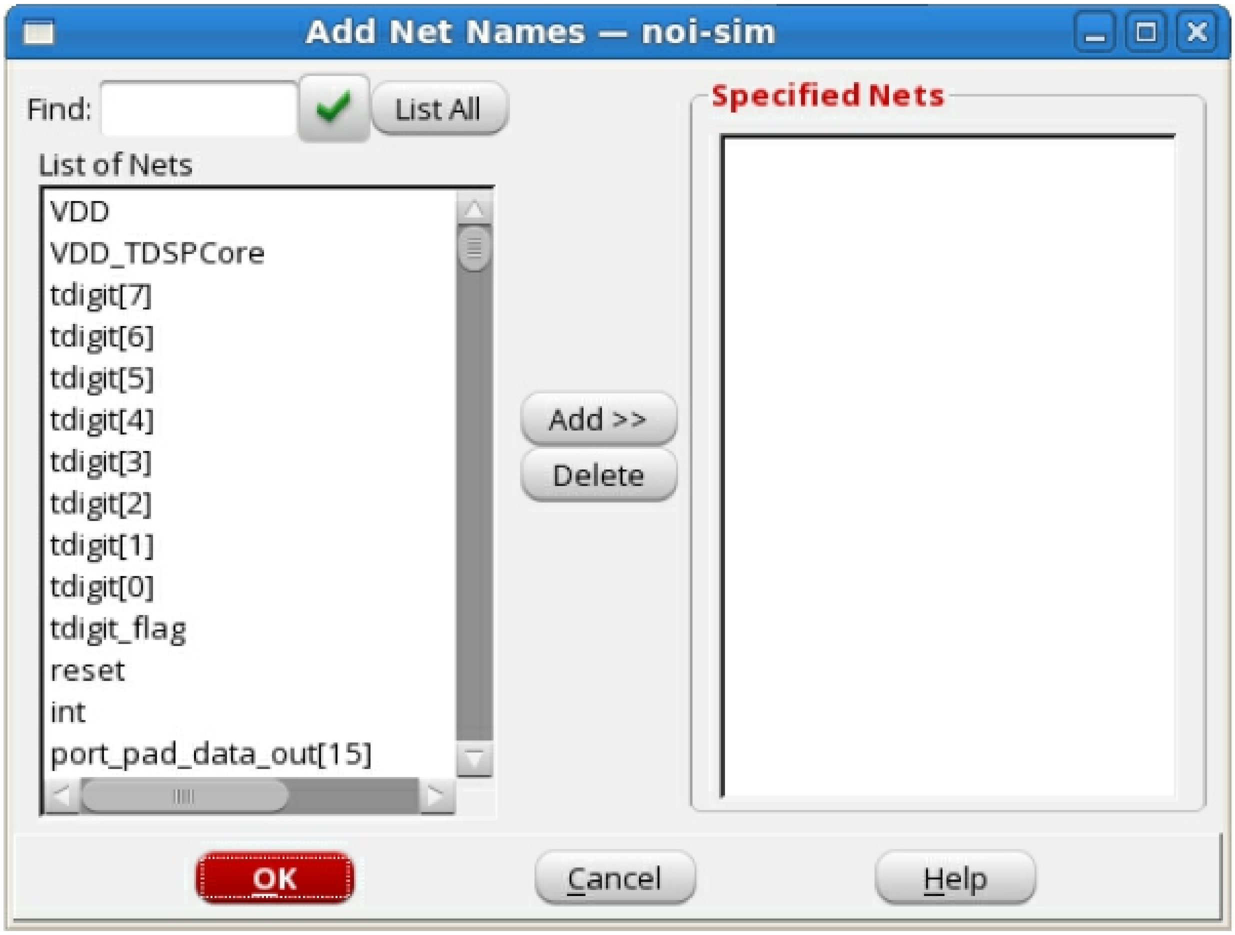
Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Add Net Names

Use the Add Net Names form to add nets to the current editing list displayed in the Results Window of the *Show Wire Crossing - Basic* form. The added nets will be saved in the file specified in the *Report File* field of the *Show Wire Closing - Basic* form

- Choose *Partition - Show Wire Crossing,* and in the *Basic* tab, click *Add*



Add Net Names - Fields and Options

Find	Type the name of the net that you want to include in the list of specified nets and click the button next to the field. The selected net is displayed in the *List of Nets* field. You can also specify wildcards(*). The names are case-sensitive.
List All	Displays all the nets in the design for the selected partitions.
Specified Nets	Displays the list of the nets that will be added to the Results window of the *Show Wire Crossing - Basic* form when you click *OK* or *Apply* .
Add	Add the selected net in the *List of Nets* field to the list displayed in *Specified Nets* .
Delete	Removes the net selected in *Specified Nets* .

Related Text Commands

The following text command provides equivalent or additional functionality:

- `showPtnWireX`

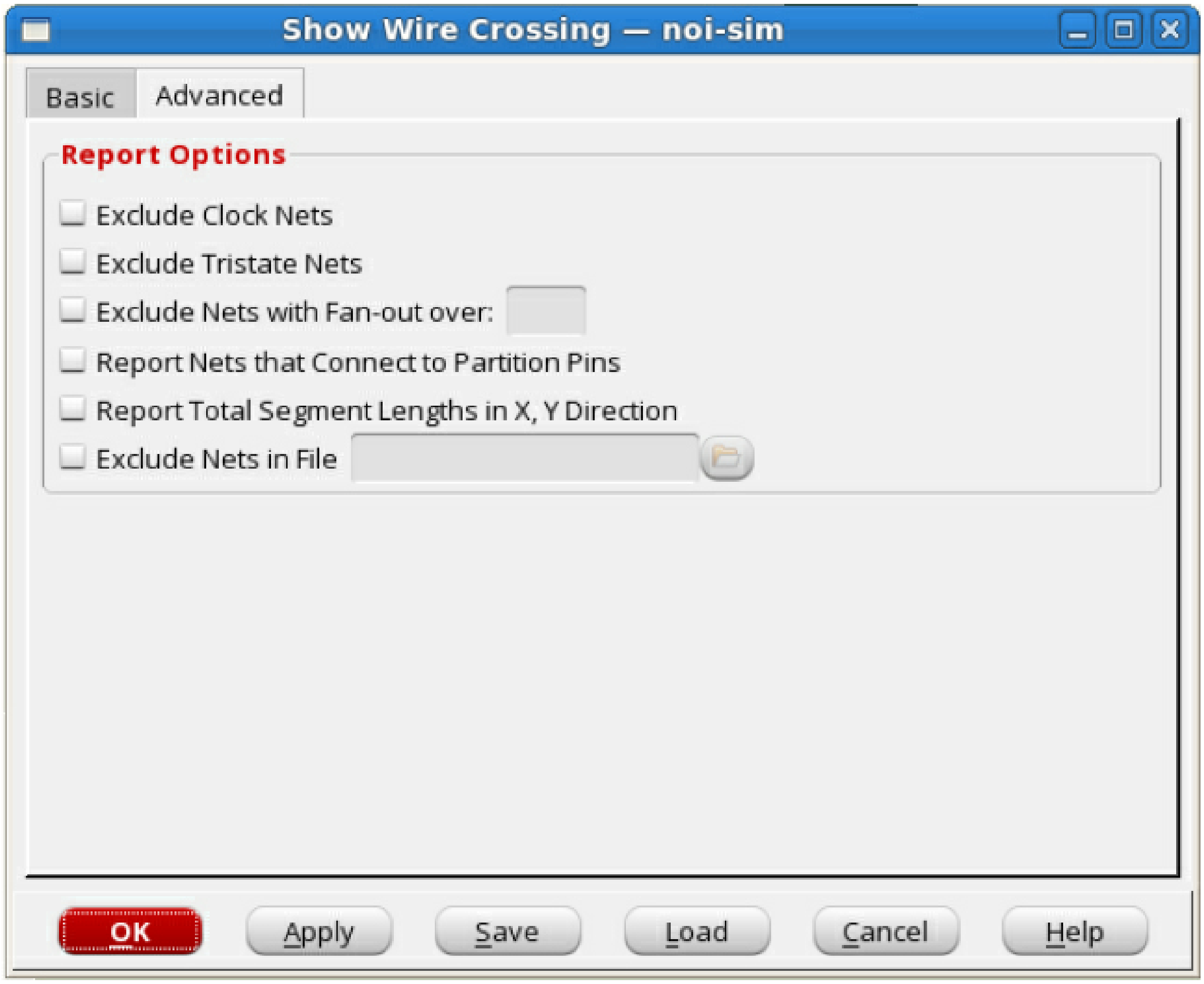
Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Show Wire Crossing - Advanced

Use the Show Wire Crossing - Advanced form to customize the list of nets that will be highlighted. For example, you can specify whether clock nets should be highlighted.

- Choose *Partition - Show Wire Crossing,* and then click on the *Advanced* tab.


Show Wire Crossing — noi-sim
Basic
Advanced
Report Options
Exclude Clock Nets
Exclude Tristate Nets
Exclude Nets with Fan-out over:
Report Nets that Connect to Partition Pins
Report Total Segment Lengths in X, Y Direction
Exclude Nets in File
OK
Apply
Save
Load
Cancel
Help

Show Wire Crossing - Advanced Fields and Options

Exclude Clock Nets	Specifies that clock nets should not be displayed in the Results window and highlighted. Default *Off*
Exclude Tristate Nets	Specifies that tristate nets should not be displayed in the Results window and highlighted. Default *Off*
Exclude Nets with fan-out over	Specifies that nets that have a fan-out value greater than the specified value should not be displayed in the Results window and highlighted. Default *Off*
Report Nets also Connect to Partition Pins	Specifies that nets that connect to partition pins should be reported and highlighted. Default *Off*
Report Total Segment Lengths in the X, Y Direction	Specifies that the segment length in the X, Y direction should also be displayed in the artwork window.
Exclude Nets in File	Specifies that the nets in the specified file should not be included in the Results window and highlighted.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `showPtnWireX`

Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Feedthrough Ports

⚠ The *Browse/Plan Partition Feedthroughs* form provides enhanced GUI support for Feedthrough Insertion and Debugging. This form is a limited-access feature in this release. It is enabled by a variable specified using the `setLimitedAccessFeature` command. To use this feature, contact your Cadence representative to explain your usage requirements, and make sure this feature meets your needs before deploying it widely.

Partition feedthrough insertion manages partitioned designs that have nets that need to be pushed down to become a component of each partition design. That is, each feedthrough buffer must be added to the partitioned design, which changes the partition's netlist. You can use the *Feedthrough Ports* menu to inserts feedthrough buffers into the partitions to change the partition netlists, and avoid routing nets over partition areas. Additionally, you can use this menu for the following:

- Change both the top-level and partition-level netlists.
- Specify a file that contains net names for which to insert feedthrough buffers.
- Save feedthrough insertion buffer topology tree information in a file.
- Apply filters on nets.

The *Feedthrough Ports* menu command opens the *Browse/Plan Partition Feedthroughs* form, which contains the following pages:

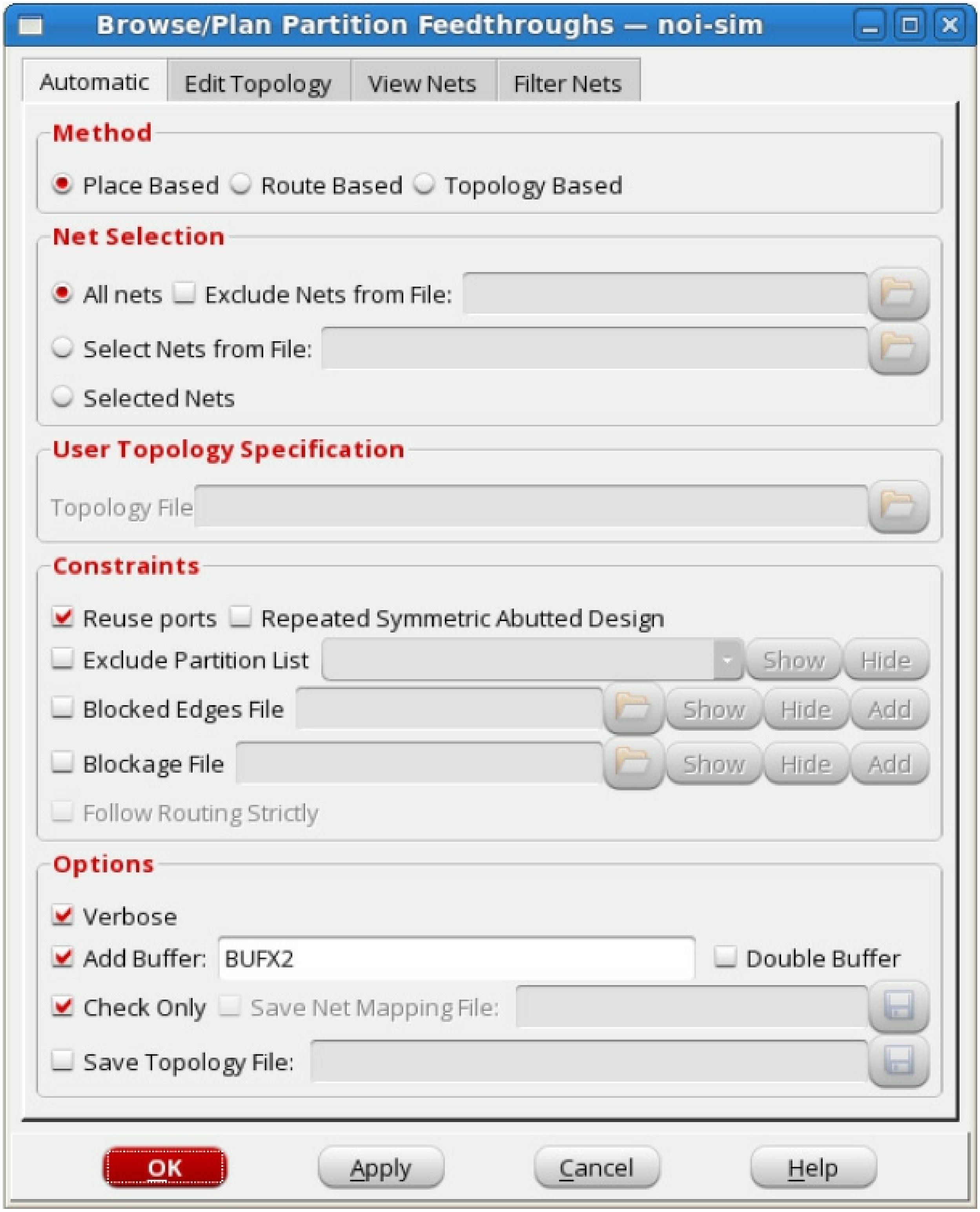
- Browse/Plan Partition Feedthroughs - Automatic
- Browse/Plan Partition Feedthroughs - Edit Topology
- Browse/Plan Partition Feedthroughs - View Nets
- Browse/Plan Partition Feedthroughs - Filter Nets

Browse/Plan Partition Feedthroughs - Automatic

Use the *Automatic* page of the *Browse/Plan Partition Feedthroughs* form to insert feedthrough buffers into the partitions to avoid routing a net over a block area. This automatically runs ECO placement and changes the original netlist.

- Choose *Partition - Feedthrough Ports* and then click *Automatic.*

Note: This page displays by default when you choose *Partition - Feedthrough Ports.*



Browse/Plan Partition Feedthroughs - Automatic Fields and

Options

Method	Specifies the method to use for defining feedthrough insertion. *Default: Place Based*	
	Place Based	Click to derive the feedthrough topology based on the placement and shape of the elements of the design irrespective of the routing.
	Route Based	Click to derive the feedthrough topology based on the routing results.
	Topology Based	Click to derive the feedthrough topology based on the topology defined in the file.
Net Selection	Specifies options for selecting nets for feedthough insertion. *Default: All nets*	
	All nets	Click to use all the nets in the design for feedthough insertion.
	Exclude Nets from File	Select to specify a file that contains net names to be excluded from feedthrough insertion.
	Select Nets from File	Click to specify the file that contains net names to be considered for feedthrough insertion.
	Selected Nets	Click to use the nets that are currently selected in the GUI for feedthough insertion.
Topology File	Specify the file that has the topology tree information. This information is used to create feedthrough buffers for the netlist.	
Constraints	Specifies the different constrains on finding path.	
	Reuse Ports	Select to reuse inserted buffers and ports across multiple instantiation of a module (master and clone) within one run. This option is enabled by default. Cadence recommends you to use this option to reduce the number of feedthrough buffers and ports in master and clone designs.

	Repeated Symmetric Abutted Design	Select to use for floorplans which have master and clone arranged in a symmetric fashion with a symmetrical data flow. If the design has nested partitions, it will delete all the partitions which are parents. It perform its operation and restores the parent partitions once finished. **Note:** This option is relevant to master clone designs.
	Exclude Partition List	Select and specify the feedthrough buffers should not be added to the specified partitions.
	Blocked Edges File	Select and specify the file that contains the names of the partitions followed by the edge numbers for the partition which are considered as blocked for the purpose of inserting partition feedthroughs. The following is the example of the blocked Edges file: *A 0 1* *B 3*
	Blockage File	Select and specify the file that contains the coordinates of line segments that are considered as blockages for placement based feedthrough insertion. **Note:** The blockages must be defined as lines that do not overlap with partitions or macros. These blockage lines are supported only with automatic feedthrough insertion or placement based feedthrough insertion. The following is the format of the blockage file: *`x1 y1 x2 y2`* *`x1 y1 x2 y2`* `...` *`xn yn xm ym`* The blockage lines are specified as coordinates of a box, however, the boxes should be of zero width or height.
	Follow Routing Strictly	Select to derive the feedthrough topology based on the routing results.
Options	Specifies options for feedthrough insertion. *Default: Verbose*	

	Verbose	Select to include the net-specific information in the logs. *Default:* Only the summary information is included in the logs.
	Add Buffer	Select to specify the name of the feedthrough buffer cell type.
	Double Buffer	Select to add docuble buffers - one close to the feedthrough input pin, and the other close to the feedthrough output pin.
	Check Only	Select to check how inserting feedthrough buffers will affect the design. With this option, the feedthrough buffers and ports are *not* inserted, they are only checked. **Note:** You can use this option along with the *Save Topology File* option. This will save the feedthrough topology information.
	Save Net Mapping File	Select and specify the name of the net mapping file. This generates a file that maps the original net name to the new net name created for the feedthrough buffers.
	Save Topology File	Select and specify the name of the topology file that will have the feedthrough buffer topology tree information from an existing floorplan. **Note**: It only saves topo version 1.0 file.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `insertPtnFeedthrough`

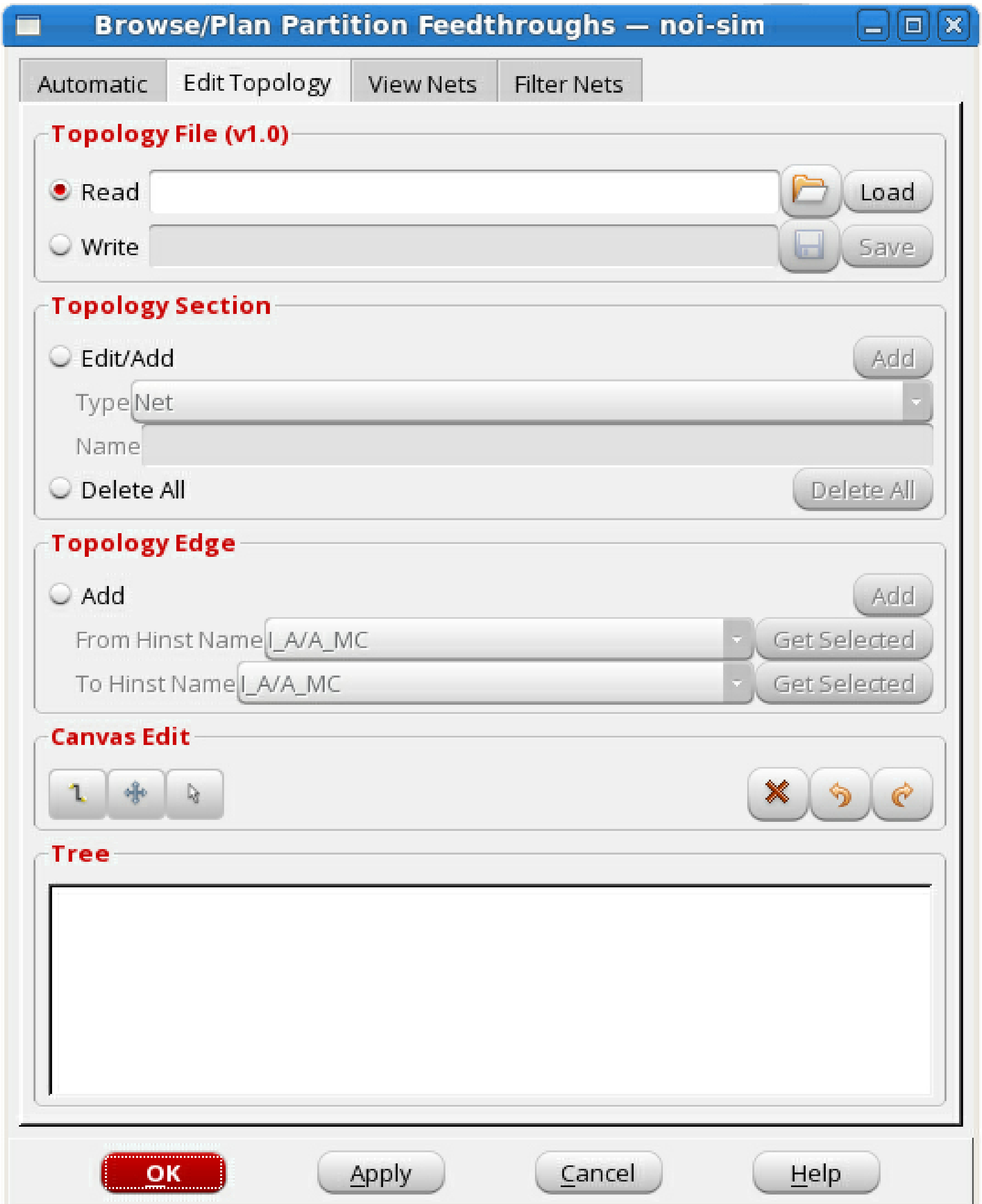
Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Browse/Plan Partition Feedthroughs - Edit Topology

Use the *Edit Topology* page of the *Browse/Plan Partition Feedthroughs* form to make changes to the file that has the topology tree information. You can use this page to interactively edit the topology tree structure in the canvas within the Innovus GUI.

- Choose *Partition* - *Feedthrough Ports* and then click *Edit Topology*.



Browse/Plan Partition Feedthroughs - Edit Topology Fields and

Options

<table>
<tr><td>Read</td><td colspan="2">Specify the name of the file that has the topology information. After specifying the name of the file, you must click the Load button to load the file. Alternatively, you can click the file browse button to specify the name of the topology file in the Open Feedthrough Topology File form.

Note: You can only edit version 1.0 of the topology file.

Note: If feedthrough was run using the Automatic Page of Browse/Plan Partition Feedthroughs form, the topology file name is automatically populated.

Note: After loading the topology file, you must click the Load button to populate the Tree area with the topology information.</td></tr>
<tr><td>Write</td><td colspan="2">Specify the name of the file in which to save the topology information. After specifying the name of the file, you must click the Save button to save the file. Alternatively, you can click the file save button to specify the name of the topology file in the Save Feedthrough Topology File form.</td></tr>
<tr><td>Edit/Add</td><td colspan="2">Click to add a new entry in the Tree area.</td></tr>
<tr><td></td><td>Type</td><td>Select the type of entry. You can select between: Net, NetGroup or Bus.</td></tr>
<tr><td></td><td>Name</td><td>Enter the name of the entry. This name displays in the Tree area.

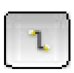
Note: After specifying the name of the entry, you must click Add to add the entry to the Tree area . The new entry then displays in topology tree displayed in the Tree area.</td></tr>
<tr><td>Delete All</td><td colspan="2">Click to delete all entries from the topology tree.

Note: Click the Delete All button to delete all entries from the topology tree displayed in the Tree area.</td></tr>
<tr><td>Add</td><td colspan="2">Click to add new nodes in the topology. The new node is added to the bottom of the topology.

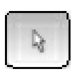
Note: Click the Add button after specifying the start and end of the partition to create a node for the object in the specified hierarchy.</td></tr>
<tr><td></td><td>From Hinst Name</td><td>Specify the start hierarchical instance name.</td></tr>
</table>

<table>
<tr><td></td><td>To Hinst Name</td><td>Specify the end hierarchical instance name.</td></tr>
<tr><td>Canvas Edit</td><td colspan="2">Enables you to interactively edit the topology tree structure in the canvas within the Innovus GUI.

Note: The nodes and direction arrows of the feedthrough path follow a color-coded representation in the GUI for easy identification. These nodes can be dragged and dropped in the GUI canvas to make changes to the feedthrough topology.

<table>
<tr><td></td><td>Represents the source node in the feedthrough path. There is only one source for a feedthrough path.</td></tr>
<tr><td></td><td>Represents the sink node in the feedthrough path. There can be multiple sink nodes in a feedthrough path.</td></tr>
<tr><td></td><td>Represents the partition selected for feedthrough that has no endpoint from original net.</td></tr>
<tr><td></td><td>Represents the current selected partition node where feedthrough is intended.</td></tr>
<tr><td></td><td>Directional arrows that point towards the path already selected for the feedthrough</td></tr>
<tr><td></td><td>Directional arrows that point towards the path being selected for the feedthrough</td></tr>
</table>
</td></tr>
<tr><td></td><td></td><td>Click to a create a node in the GUI canvas on the partition where the net source is. This node is highlighted in Blue color on the Innovus GUI canvas.

Note:
This node is also added and selected in the Tree area of the form. The partition of the selected node also gets selected in the Innovus GUI canvas.
When the cursor is moved, the node changes the color from blue to white. This signifies that the node is selected. Directional arrows showing all the possible endpoints of the net also appear. These arrows follow the cursor. For a feedthrough path to be complete, the created path should include all these endpoints.</td></tr>
</table>

		Click to move the selected node of the feedthrough path in the GUI canvas. Directional arrows follow the cursor movement. **Notes** • You can click on any new partition to move the node to that partition or click on another node to move it to a different partition. • The root the topology tree cannot be dragged. • The topology tree structure is updated in the *Tree* area only after you drop the node being moved. • Nodes are always placed at the center of the partition even if you drag and drop a node to any other point in the partition fence area. Directional arrow links are automatically updated to point to/from the new location of the node.
		Click to disable the interactive editing mode.
	Delete selected node/section in Topology Tree	Click to delete the node selected in the *Tree* area from the topology tree structure. **Note:** The selected node and the all its sub-nodes are deleted.
	Undo	Click to undo the last operation. The nodes in the *Tree* area of the form are accordingly updated along with the selected partition in the Innovus GUI canvas. This is a sequential operation.
	Redo	Click to redo the last undo operation. The nodes in the *Tree* area of the form are accordingly updated along with the selected partition in the Innovus GUI canvas. This is a sequential operation.
Tree	Displays the topology tree structure. Each node represents a hierarchical instance. You can use this area to select nodes and then make changes to the topology.	

Related Text Commands

The following text command provides equivalent or additional functionality:

- `insertPtnFeedthrough`

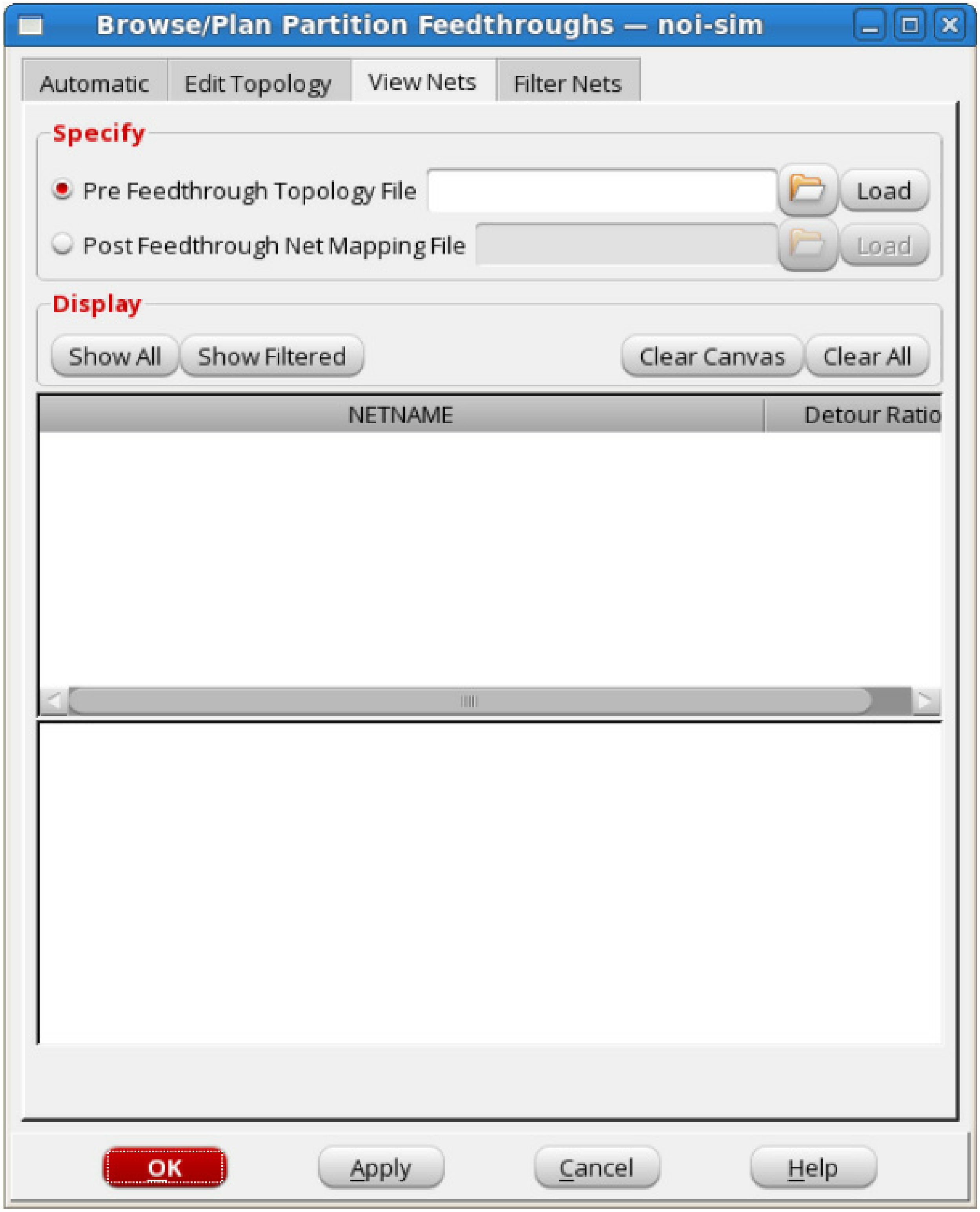
Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Browse/Plan Partition Feedthroughs - View Nets

Use the *View Nets* page of the *Browse/Plan Partition Feedthroughs* form to highlight all nets for which feedthrough buffers were inserted or were considered. The highlighted feedthrough path consists of the nets, the terms, and the instances.

- Choose *Partition* - *Feedthrough Ports* and then click *View Nets*.



Browse/Plan Partition Feedthroughs - View Nets Fields and

Options

Load	Loads the pre-feedthrough topology file or post-feedthrough net mapping file for analysis.	
	Pre Feedthrough Topology File	Click and specify the name of the file that has the topology information. After specifying the pre-feedthrough topology file, you must click the *Load* button to populate the *Display* area with the net names and the detour ratios. Alternatively, you can click the file browse button to specify the name of the topology file in the *Topology File* form. **Note**: If feedthrough was run using the *Automatic* Page of *Browse/Plan Partition Feedthroughs* form without mapping file, the topology file name is automatically populated. **Note**: To analyze the path before inserting feedthroughs, Cadence recommends you to use the topology file.
	Post Feedthrough Net Mapping File	Click and specify the name of the net mapping file. After specifying the net mapping file, you must click the *Load* button to populate the *Display* area with the net names and the detour ratios. Alternatively, you can click the file browse button to specify the name of the net mapping file in the *Mapping File* form. **Note**: If feedthrough was run using the *Automatic* Page of *Browse/Plan Partition Feedthroughs* form with mapping file, the net mapping file name is automatically populated. **Note**: To analyze the path after inserting feedthroughs, Cadence recommends you to use the mapping file.
Display	Controls the display of nets.	
	Show All	Click to display the details of all nets and shows path markers in the Innovus window.
	Show Filtered	Click to display the details of filtered nets and shows their path markers in the Innovus window.
	Clear All	Click to clear all the net entries in the list and also clears the details table. It clears the path markers from the Innovus window and removes all selections.

	Clear Canvas	Click to remove all path markers from the Innovus window and removes all selections. However, it retains the net details.
NETNAME	Displays the net names. You can select a net to display its details and analyze its topology. A corresponding path is also drawn in the GUI. **Tip**: You can press the `shift` key and add more nets for analysis. **Tip**: You can click the header to sort the net names in ascending or descending alphabetical order.	
Detour Ratio	Displays the feedthrough path detour ratio of the nets. **Tip**: You can click the header to sort the nets in ascending or descending order of their detour ratio.	

Related Text Commands

The following text command provides equivalent or additional functionality:

- `insertPtnFeedthrough`

Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Browse/Plan Partition Feedthroughs - Filter Nets

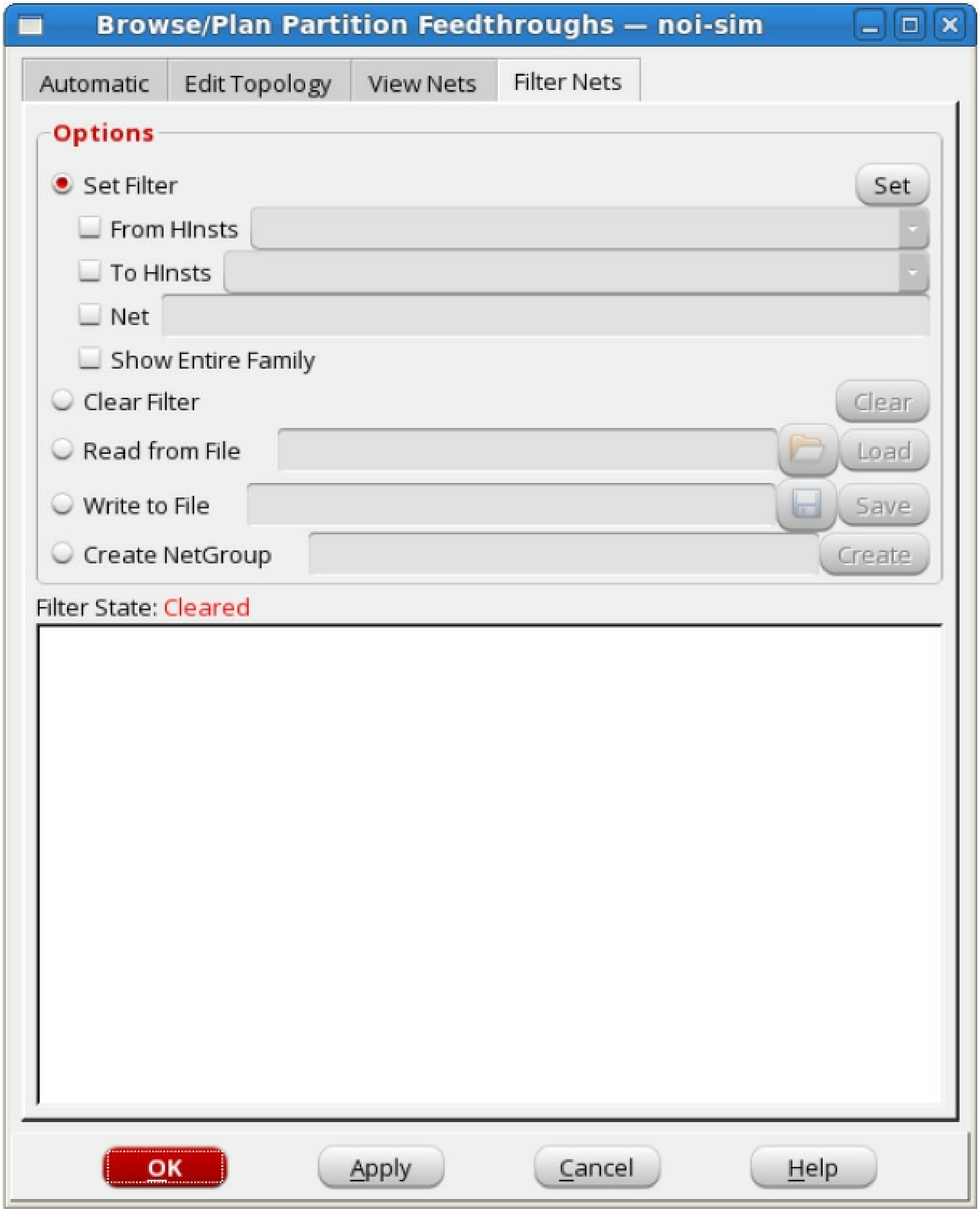
Use the *Filter Nets* page of the *Browse/Plan Partition Feedthroughs* form for applying filters on nets in order to choose target nets. You can use this page to:

- Filter nets and save them in a file for the purpose of automatic feedthrough insertion in

Automatic page.

- Filter nets and create netgroups for the purpose of topology based feedthrough insertion in Edit Topology page.
- Filter nets to view selected nets only in the View Nets page.

Choose *Partition - Feedthrough Ports* and then click *Filter Nets*.



Browse/Plan Partition Feedthroughs - Filter Nets Fields and

Options

Set Filter	Select the mode to use for filtering nets.	
	Set	Click to set the filters based on the options specified below. **Note:** Click the *Set* button after specifying the different filter criterions to display the filtered nets in the display area. **Note:** If multiple filter options are chosen then the filtered nets must match all the specified conditions. For example if *From Hinsts* is chosen as A and *To Hinsts* is chosen as D and *Net* name is specified as n*, then only those nets that meet all three conditions will be selected.
	From HInsts	Select and choose the hierarchical instances from the list to select the nets whose "source" is within these hierarchical insances.
	To HInsts	Select and choose the hierarchical instances from the list to select the nets whose "sink" is within these hierarchical insances.
	Net	Select and specify the name of the net to display the nets with the specified name. **Note:** You can use wildecards in the net name.
	Show Entire Family	Select to include all the master and clone related nets. This lists the entire chain of connected nets in designs with master and clone partitions.
Clear Filter	Click to clear the applied filters. **Note:** Click the *Clear* button to clear the filters and remove the net names from the display area. **Note**: Clearing the applied filters does not impact the *View Nets* page.	
Read from File	Click and specify the name of the file from which the nets are loaded. After specifying the *Read from File* name, you must click the *Load* button to load the file. Alternatively, you can click the file browse button to specify the name of the filter file in the *Load Filter File* form.	

Write to File	Click and specify the name of the file in which filtered nets are to be saved. After specifying the *Write to File* name, you must click the *Save* button to save the file. Alternatively, you can click the file save button to specify the name of the filter file in the *Save Filter File* form. **Note:** The saved file can then be used in the *Automatic* tab to select or exclude these nets.
Create Net Group	Click and specify the name of the net group to create with the filtered nets. This NetGroup name is used in the *Topology* Section of the *Edit Topology* tab if the *Type* chosen is NetGroup. After specifying the *NetGroup* name, you must click the *Create* button to create the net group.
Filter State	Displays the status of the filter. • Clear: If the *Filter State* is cleared, then pressing the *Show Filtered* button on the *View Nets* tab has no effect. • Applied: If the *Filter State* is applied, then the list below contains the names of the filtered nets filtered. Pressing the *Show Filtered* button on the *View Nets* tab will display only the nets listed below.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `insertPtnFeedthrough`

Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Assign Pin

Use the Assign Pin menu command to assign partition pins. You can assign pins for a partition without having to commit the partition.

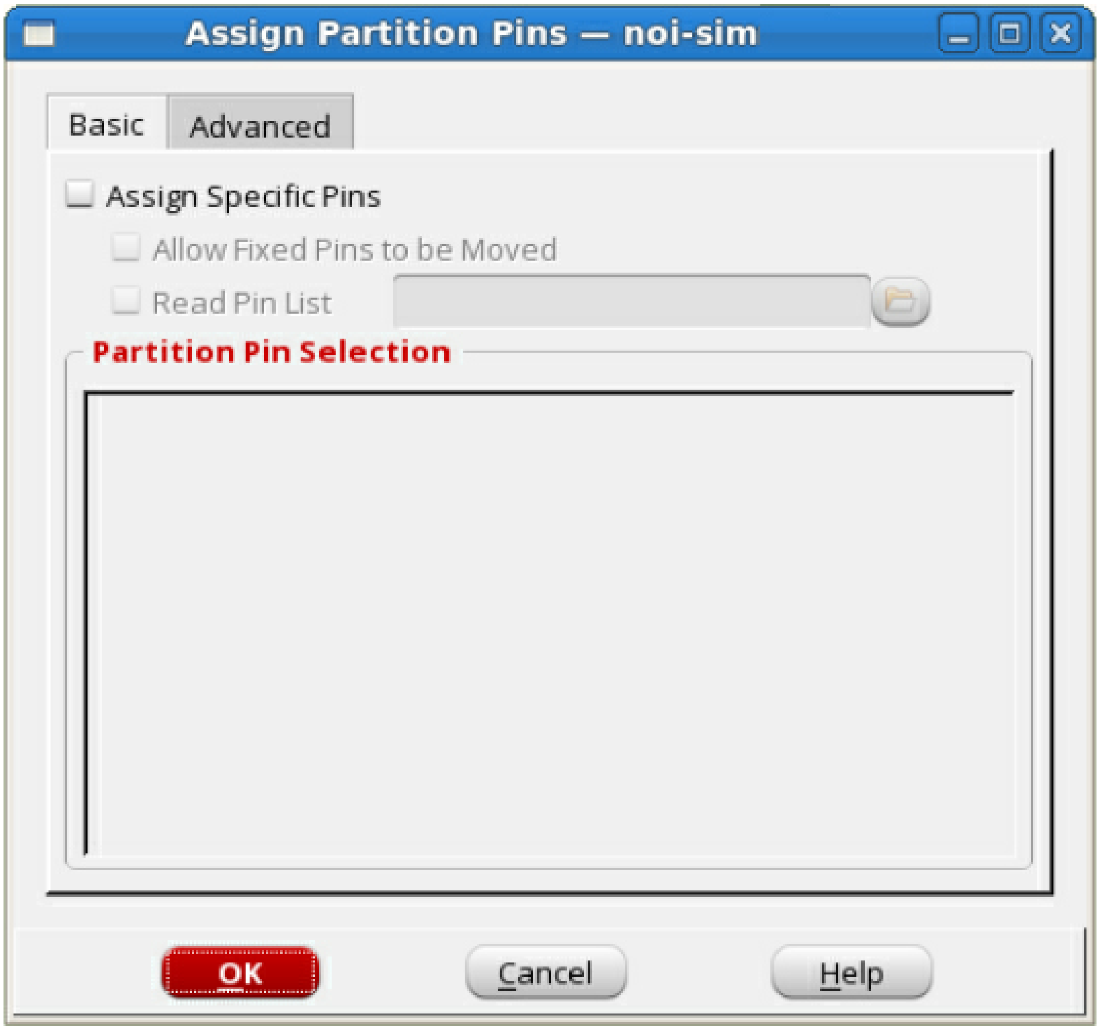
The Assign Pin menu command opens the Assign Partition Pins form, which consists of the following two pages:

- Assign Partition Pins - Basic
- Assign Partition Pins - Advanced

Assign Partition Pins - Basic

Use the Assign Partition Pins - Basic form to create pins for the partitions.
Note: You should route the design before assigning partition pins.

- Choose *Partition - AssignPin* , and click the *Basic* tab.


Assign Partition Pins — noi-sim
Basic
Advanced
Assign Specific Pins
Allow Fixed Pins to be Moved
Read Pin List
Partition Pin Selection
OK
Cancel
Help

Assign Partition Pins - Basic Fields and Options

Assign Specific Pins	Specifies that only the specified pins should be assigned. If you do not select this check box, all pins for all partitions are assigned.	
	Allow fixed Pins to be Moved	
		If you select this checkbox, the specified pins with a *Fixed* status can also be moved. **Note:** Pins that are not specified but have a *Fixed* status are *not* moved. *Default* : The specified pins with a *Fixed* status are *not* moved.
	Read Pin List	Specifies the file that contains the list of pins to be assigned to the respective partitions.
	Partition Pin selection	
		If you select the *Assign Specific Pins* checkbox, specify the pins to assign for each partition, in the corresponding *Pins* field next to the name of the partition.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `assignPtnPin`

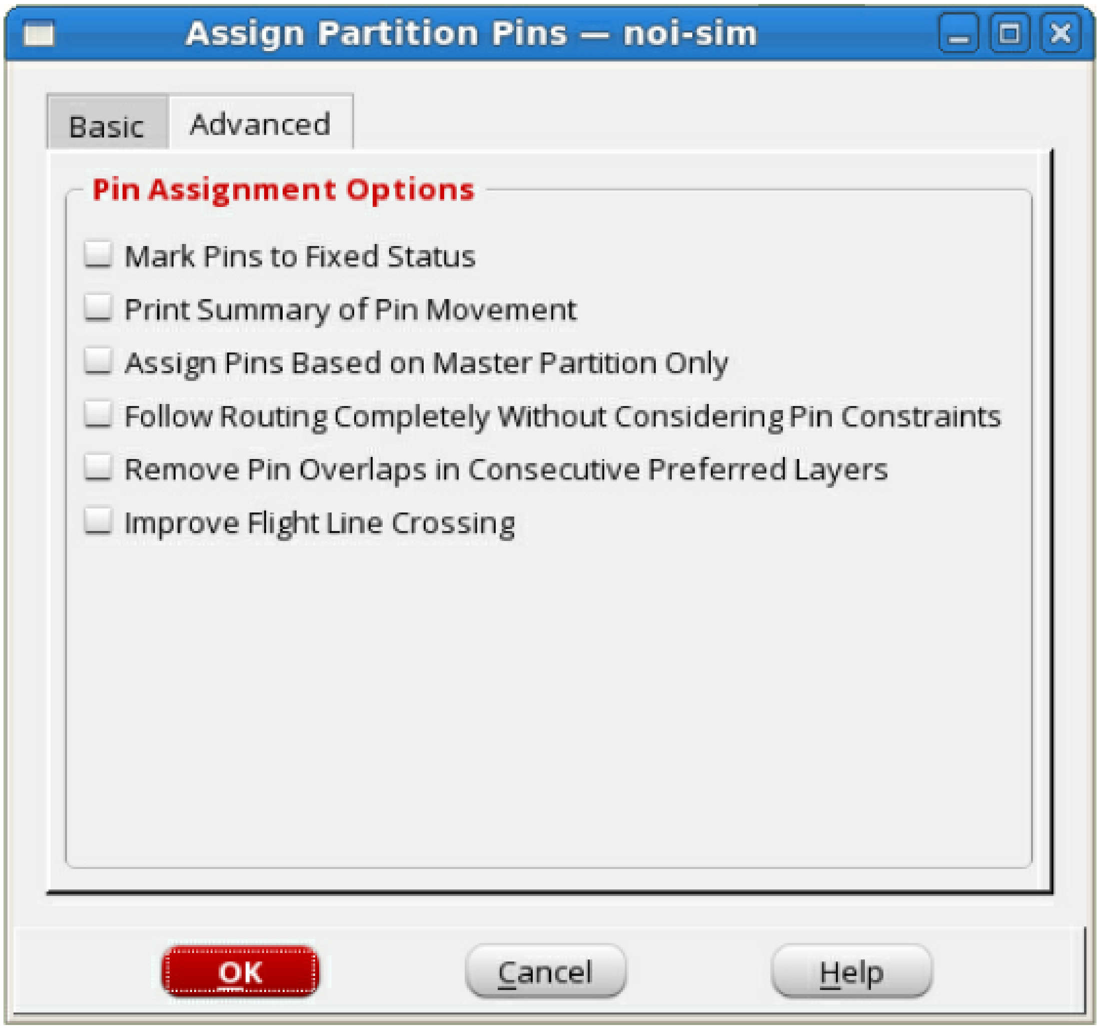
Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Assign Partition Pins - Advanced

Use the Advanced Partition Pins - Advanced form to customize the pin assignment options. For example, you can specify that the status of the assigned pins should be changed to *Fixed* .

- Choose *Partition* - *AssignPin* and click the *Advanced* tab



Assign Partition Pins - Advanced Fields and Options

Mark Pins to Fixed Status

	Specifies that all pins will have a Fixed status.
Print Summary of Pin Movement	
	Prints a summary report of the deviation (in micrometers) of the final pin locations from the point of intersection of the net and the partition edge. For details of the report, see the description of the `assignPtnPin` command in the *Innovus Text Command Reference* .
Assign Pins Based on Master Partition Only	
	Specifies that for designs that have partition clones, the command should consider only the partition master and use the master assignment for all the clones.
Follow Routing Completely Without Considering Pin Constraints	
	Specifies that the pin assignment completely follows the routing results generated by Early Global Route, without taking into consideration any pin constraints. The option can be useful when, for example, you want to compare pin locations based purely on Early Global Route results with pin locations that honor the specified pin constraints.
Remove Pin Overlaps in Consecutive Preferred Layers	
	Specifies the following: • There are no pins above or below any pin, across layers. That is, if a pin on a layer has co-ordinates x and y, there are no pins on co-ordinates x and y on any other layer. This applies to all pins on all layers. • If the value of the pin pitch is 1 (instead of the default value of 2 or any other value), adjacent pins are not placed on the same layer.
Improve Flight Line Crossing	

	Reduces flightline crossing during pin alignment. The partition and the blackbox pins are rearranged to be aligned with external connections: • Guided pins are reordered within the pin guide box. • Pins are rearranged at (or close to) their original locations. • Pin ordering is performed independently for each partition edge. The locations of fixed pins, aligned pins or multi-location pins is not changed. Master-clone pins are not reordered.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `assignPtnPin`

Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Check Pin Assignment

Use the *Check Pin Assignment* menu command to check whether pin assignment results are valid. A report is output to the Innovus console window. For each partition, it reports whether it has passed the pin checking. If it does not pass, the report indicates the number of pins that are unassigned. This is useful when working with the Pin Editor.

- Choose *Partition - Check Pin Assignment* .

Related Text Commands

The following text command provides equivalent or additional functionality:

- `checkPinAssignment`

Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Derive Timing Budget

The Derive Timing Budget form enables you to generate timing budgets.

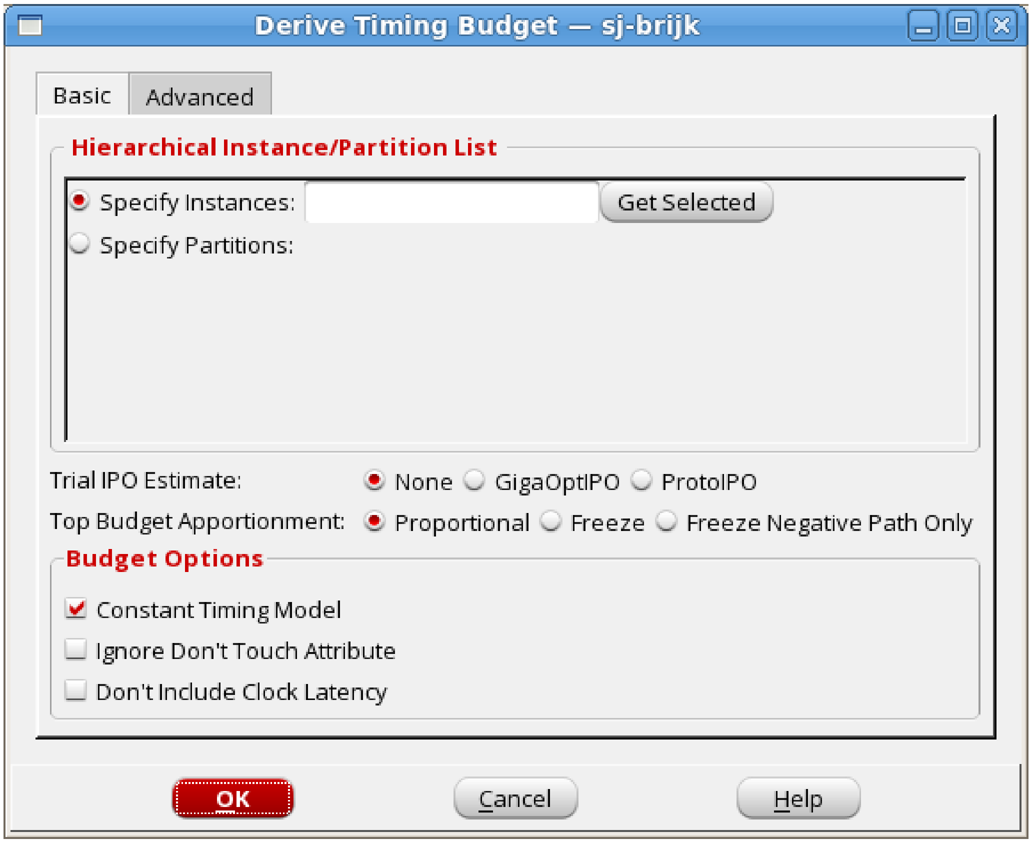
The Derive Timing Budget form has the following pages:

- DeriveTimingBudgetBasic
- DeriveTimingBudgetAdvanced

Derive Timing Budget - Basic

Use the *Basic* page of the Derive Timing Budget form to select partition pins and set budgeting options.

- Choose *Partition - Derive Timing Budget*. The *Basic* tab is selected by default.



Derive Timing Budget - Basic Fields and Options

Hierarchical Instance Solution	
Specify Instances	Performs budgeting for the hierarchical instance(s). This instance could be a black box. You can derive timing budgets for black boxes and other instances in the same run. If you select *Merge Master and Clone* from the Derive Timing Budget - Advanced page, the software worst-case budgets based on worst-case data per-pin for specified instances in a master/clone set. If you specify instances from more than one master/clone set, the tool derives separate worst-case timing budgets for the specified instances in each set.
Specify Partitions	Performs budgeting for the specified partition(s). If you select Merge Master and Clone from the Derive Timing Budget - Advanced page, the software obtains worst-case budgets based on worst-case data per-pin for all partitions in the master/clone set containing the partition.

Trial IPO Estimate	Inserts trial IPO fixes when generating the timing budget files. These parameters are used only for trial IPO operation, and the Innovus software does not make actual changes in the design.
Trial IPO	Runs trial IPO operations on all the top-level nets and the section of the path that is within the partition.
Full	Runs trial IPO operations on all the nets in the design.
None	Does not run trial IPO operations.
Top Budget Apportionment	
Proportional	Proportions the timing budget for the top-level and the partitions.
Freeze	Fixes the top-level timing budget, and proportions the remaining timing budget only for the partitions.
Freeze Negative Path Only	Fixes the top-level timing budget, and proportions the remaining timing budget only for the partitions when the slack is negative.
Budget Options	
Setup And Hold	Derives budgeting for both setup and hold analysis modes. **Note:** If you do not select this budget option, the software derives budgets for setup mode only.
Constant Timing Model	Creates load-dependent timing models.
Ignore Don't Touch Attribute	Handles don't touch objects as fixed.
Don't Include Clock Latency	Does not include the clock latency in the `set_input_delay` and `set_output_delay` constraints. **Note:** The clock latency is always included if the design has propagated clock(s) irrespective of this option.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `deriveTimingBudget`

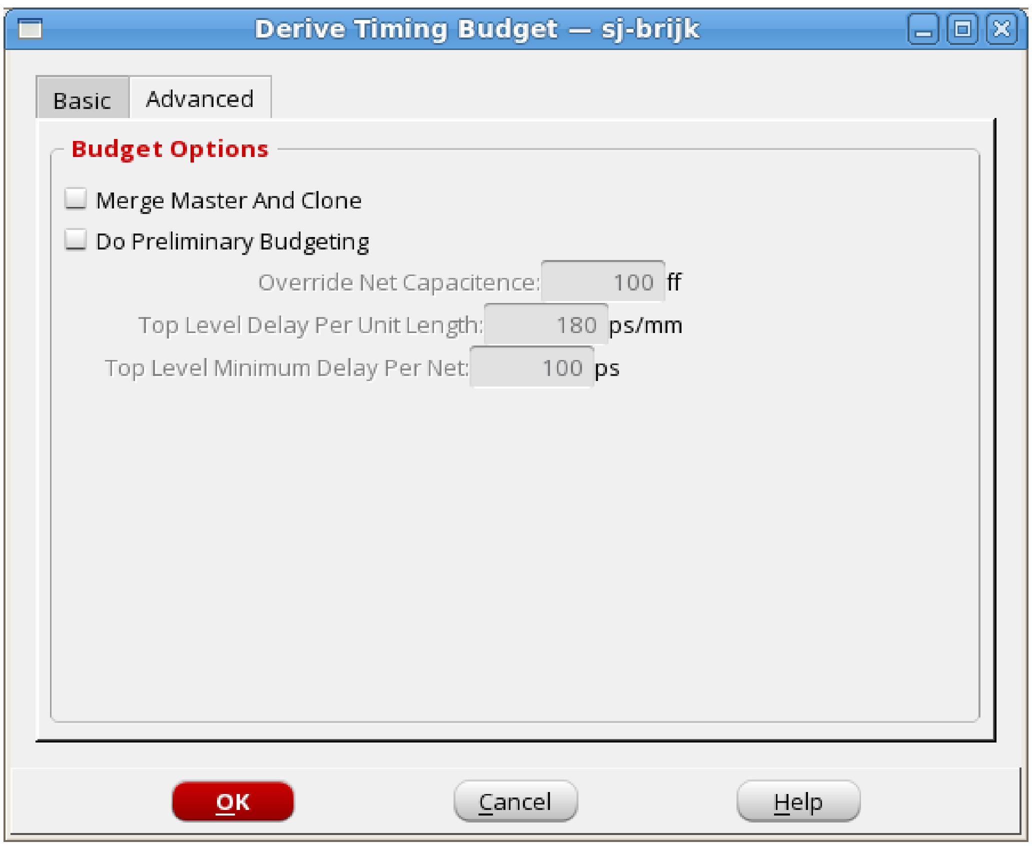
Related Topic

For more information, see the "Timing Budgeting" chapter in the *Innovus User Guide* .

Derive Timing Budget - Advanced

Use the *Advanced* page of the Derive Timing Budget form to specify pin assignment options.

- Choose *Partition* -- *Derive Timing Budget* and click the *Advanced* tab.



Derive Timing Budget - Advanced Fields and Options

Merge Master and Clone	Derives a timing budget for hierarchical partitions based on the worst-case data per-pin on the master/clone set containing the partitions. The timing data for the partitions in the master/clone set will be identical, reflecting the worst case among the corresponding pins on the master/clones. You can use this option with the *Specify Instances* or *Specify Partitions* options on the Derive Timing Budget - Basic page. When used with instances, this option derives worst-case budgets for specified instances in a master/clone set. For example, in a master/clone set that includes `instA`, `instB`, and `instC`, if `pin1` has the worst case data on `instA` among pins on `instA`, `instB`, and `instC`, then the software uses the data from `instA/pin1` for `instB/pin1 and instC/pin1`. Similarly, if `pin2` has the worst case data among `instA`, `instB`, and `instC`, then the software uses the data from `instA/pin2` for `instB/pin2` and `instC/pin2`. When used with partitions, this parameter derives worst-case budgets for all partitions in the master/clone set that contains the specified partition.
Do Preliminary Budgeting	Derives timing budgets in the early stages of the design to get a preliminary estimate of the budgets. When you use this parameter the software uses the net delays and net loads that you specify using the `setThresholdBudgetThreshold` command. The software does not perform calculations to derive the values for net delay and net load, and does not use trial IPO operations for calculating budgets. The software distributes the positive slack equally between source block, destination block, and top-level. For negative slack, the *Freeze Negative Path Only* option on the Derive Timing Budget - Basic form.
Override Net Capacitance	Specifies the lump capacitance value.
Top Level Delay Per Unit Length	Specifies the top-level estimated delay per mm length.
Top Level Minimum Delay Per Net	Specifies the top-level minimum delay per net value.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `deriveTimingBudget`

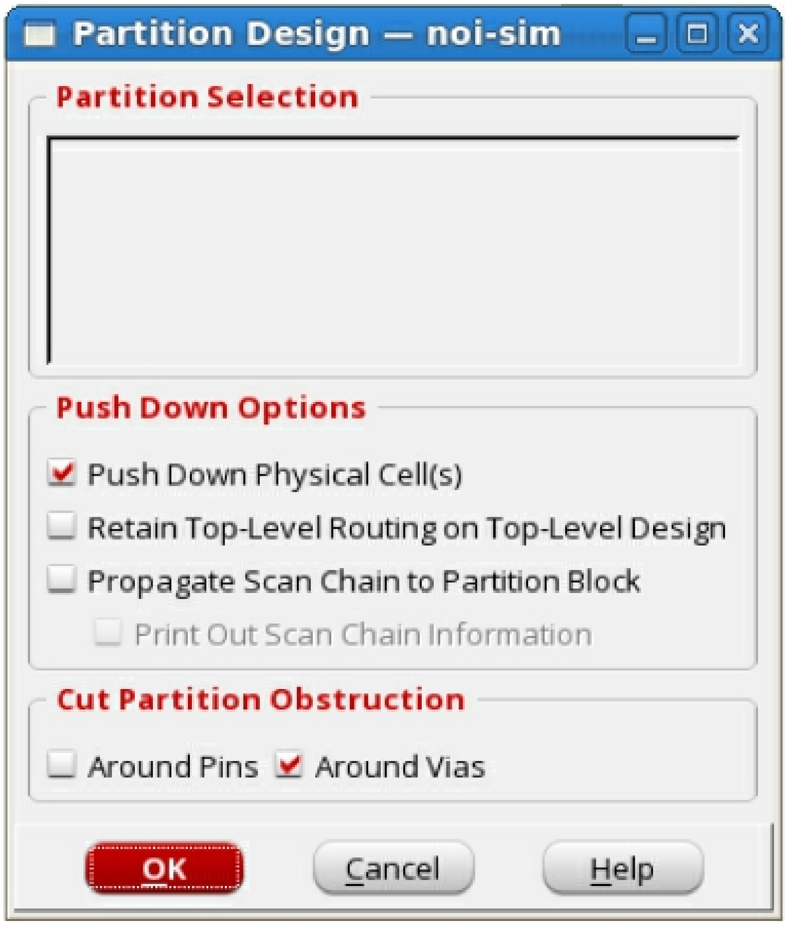
Related Topic

For more information, see the "Timing Budgeting" chapter in the *Innovus User Guide*.

Commit Partition

Use the Commit Partition form to push down the physical cells to the partition-level design(s).

- Choose *Partition* -- *Commit Partition*



Partition Design - Fields and Options

Partition Selection	Specifies the modules to convert to a partition.
Push Down Physical Cells	
	Specifies that physical only (filler) cells are pushed down into the partition; they are not retained at the top level.
Retain Top Level Routing Stay on Top-Level Design	
	Specifies that stripes that are not on a layer reserved by the partition are retained at the top level and are also copied into the partition Default: *Off*
Propagate Scan Chain to Partition Block	

	Specifies that scan chains should be propagated to the partition blocks. Default: *Off*
Print Out Scan Chain Information	
	Displays detailed information about the scan chain on the screen and also prints it in the log file. Default: *Off*
Around Pins	
	Specifies that there are no cuts in the obstructions around pins. You can use this parameter when you want to ensure that the top-level routing can connect the pins without using the space between the pins and the corresponding cover blockages. Default: *On*
Around Vias	
	Specifies that there are no cuts in the obstructions around vias. You can use this parameter when you want to ensure that the top-level routing can connect the vias without using the space between the vias and the corresponding cover blockages. Default: *On*

Related Text Commands

The following text command provides equivalent or additional functionality:

- `partition`
- `savePartition`

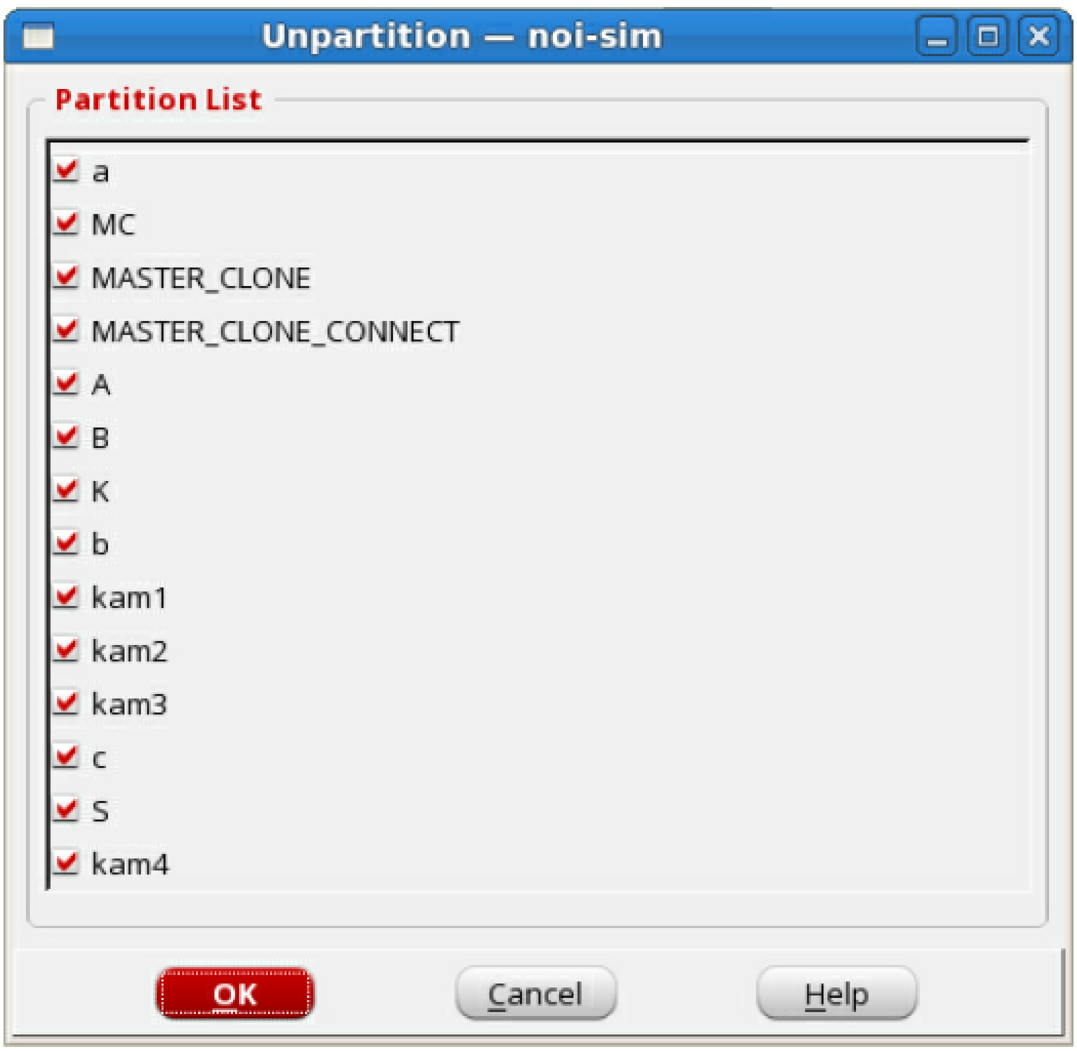
Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Flatten Partition

Use the Flatten Partition command to convert selected partitions in a design back to soft modules. This command opens the Unpartition form. You can use this in sequence with the Partition program to fine tune partition size and shape for top-level routing or block-level implementation.

- Choose *Partition - Flatten Partition*



Unpartition Fields and Options

Partition List	Specifies the partition(s) to convert back to soft modules. By default, all are selected

Related Text Commands

The following text command provides equivalent or additional functionality:

- `flattenPartition`

Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Assemble Design

Use the Assemble Design form to bring back specified block data to the top-level design for chip assembly.

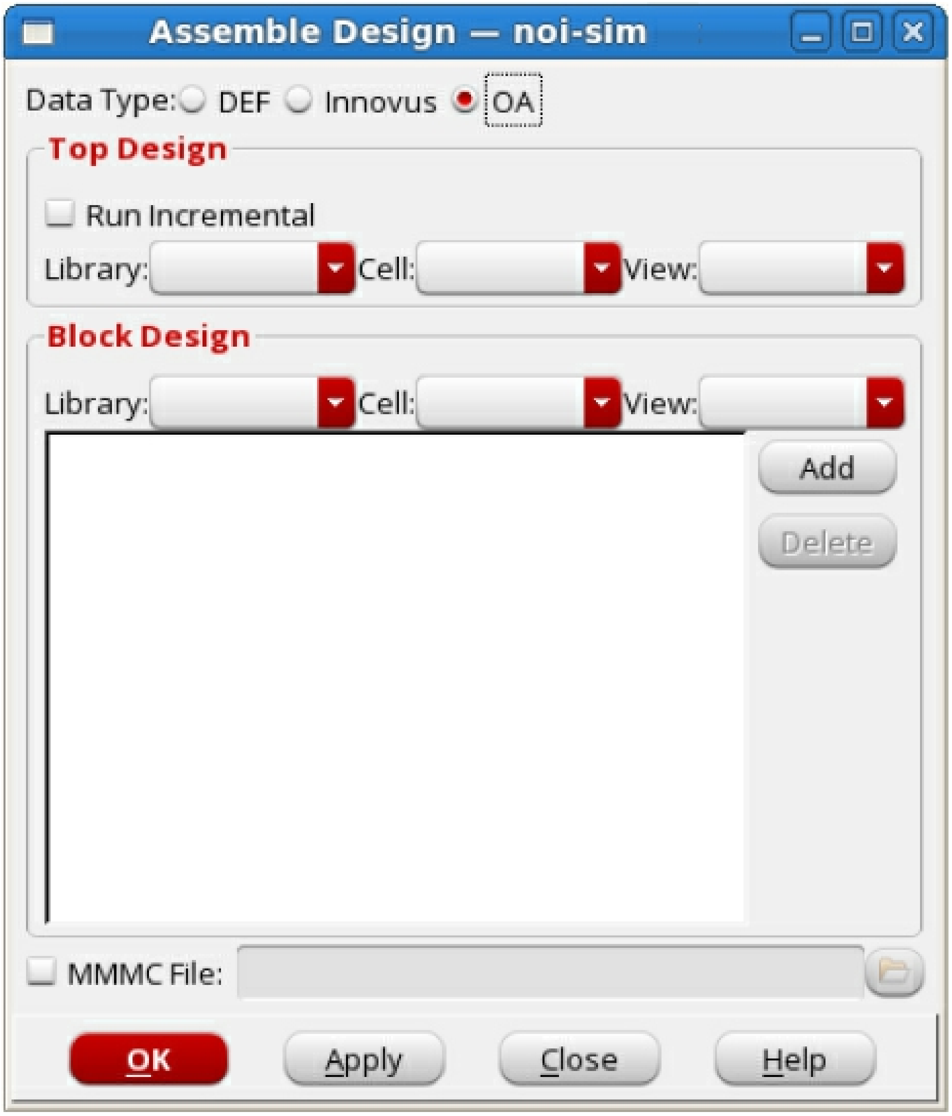
The Assemble Design form consists of the following tabs:

- Assemble Design - OA
- Assemble Design - Innovus
- Assemble Design - DEF

Assemble Design - OA

Use the Assemble Design-OA form when you want to assemble an OpenAccess database design.

- Choose *Partition* - *Assemble Design. The* OA tab is open by default.



Assemble Design-OA Fields and Options

Top Design	*Run Incremental*	Enables partitions to be brought back in one session, thus, avoiding the need to run multiple sessions for bringing back all the data of a design.
	Library	Specifies the top-level library name of the OpenAccess database design.
	Cell	Specifies the top-level cell name of the OpenAccess database design.
	View	Specifies the top-level view name of the OpenAccess database design.
Block Design	Specifies the path to the block-level design. You can use the Add button to specify additional block-level designs.	
	Library	Specifies the block-level library name of the OpenAccess database design.
	Cell	Specifies the block-level cell name of the OpenAccess database design.
	View	Specifies the block-level view name of the OpenAccess database design.
Add	Adds the block design data to the list of block-level designs that will be assembled.	
Bring Back Rows	Specifies that row information should be brought back from the block-level design.	

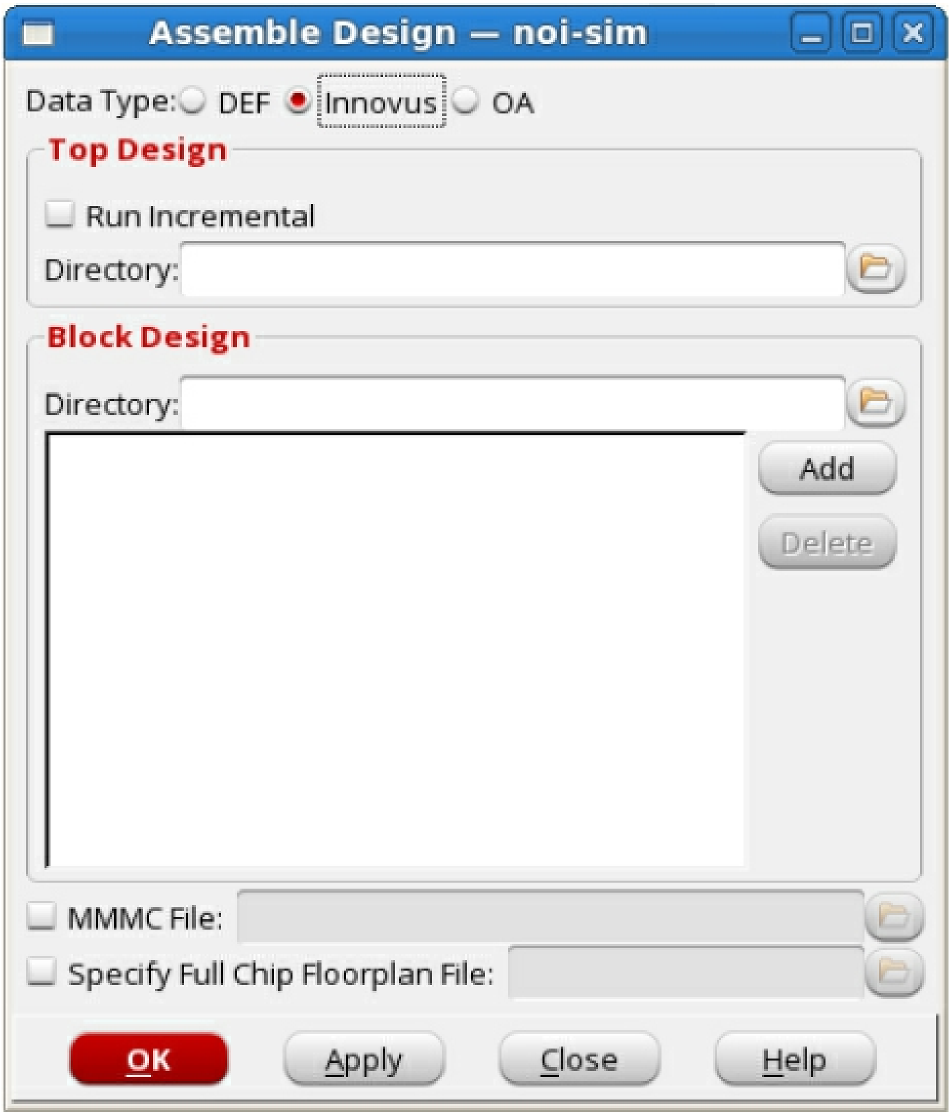
Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Assemble Design - Innovus

Use the Assemble Design - Innovus form when you want the place-and-route data to be used while assembling the design.

- Choose *Partition - Assemble Design* and click the Innovus tab.



Assemble Design - Innovus Fields and Options

Top Design	*Run Incremental*	Enables partitions to be brought back in one session, thus, avoiding the need to run multiple sessions for bringing back all the data of a design.
	Directory	Specifies the path to the top-level design created by `saveDesign`. This design directory should contain the top-level configuration file, floorplan file, Verilog netlist, and placement and routing data.
Block Design	*Directory*	Specifies the path to the block-level design(s). This directory should be generated by the `saveDesign` command. After you specify the directory, click the Add button to add the block to the list of block-level designs that will be assembled. Repeat this for each block-level design.
Add	Adds the block design data, or the set of DEF file name and Verilog netlist name, to the list of block-level designs that will be assembled.	
Specify Full Chip Floorplan File	Specifies the chip-level floorplan file. By default, the command reads in the floorplan file from the provided top-level design. Use this option for the top-down hierarchical flow.	
Bring Back Rows	Specifies that row information should be brought back from the block-level design.	

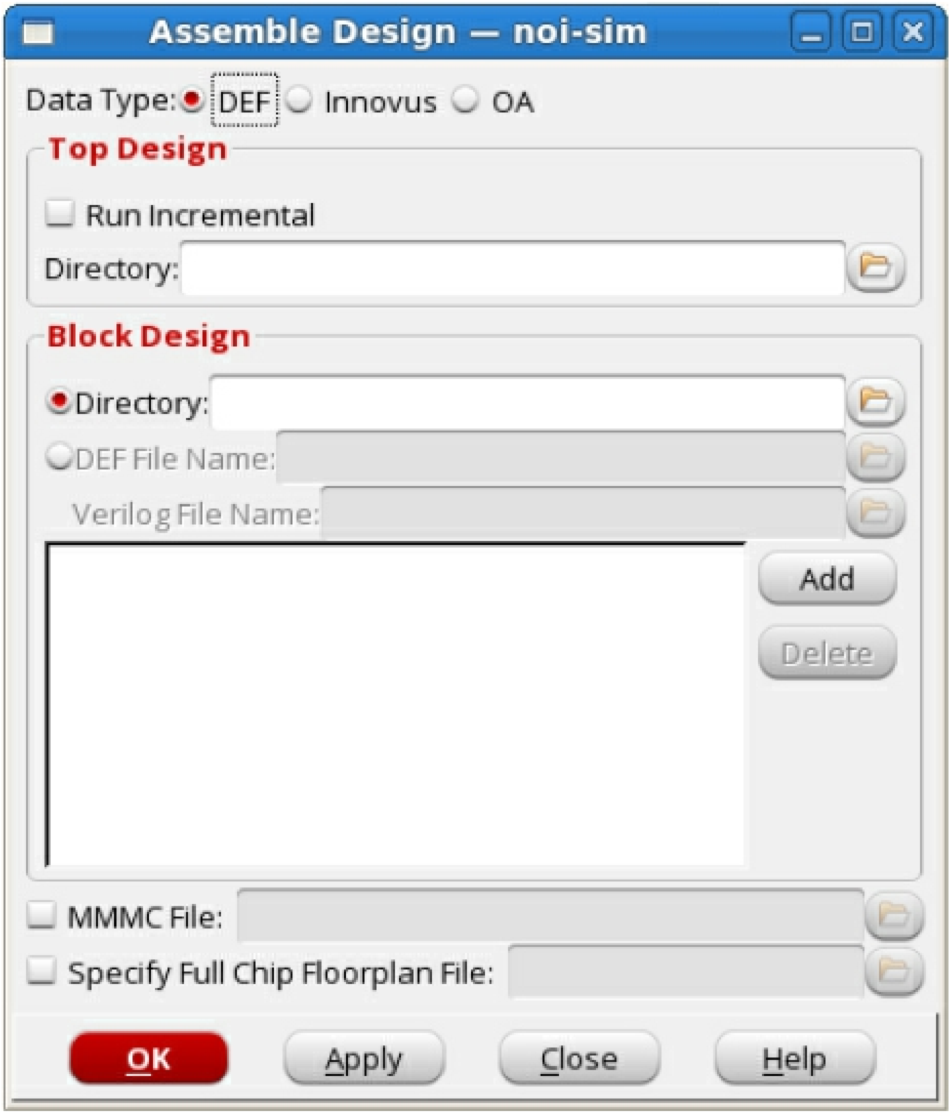
Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see Partitioning the Design in the *User Guide*.

Assemble Design - DEF

Use the Assemble Design - DEF form when you want the DEF data to be used while assembling the design.

- Choose *Partition* - *Assemble Design* and click the DEF tab.



Assemble Design-DEF Fields and Options

Top Design	*Run Incremental*	Enables partitions to be brought back in one session, thus, avoiding the need to run multiple sessions for bringing back all the data of a design.
	Directory	Specifies the path to the top-level design created by `saveDesign -def`. This design directory should contain the configuration file, top-level floorplan, Verilog netlist, and DEF files.
Block Design	*Directory*	Specifies the path to the block-level design(s). This directory should be generated by the `saveDesign -def` command. After you specify the directory, click the Add button to add the block to the list of block-level designs that will be assembled. Repeat this for each block-level design.
	DEF File Name Verilog File Name	Specifies the DEF file name and the Verilog name. Use this option if the Verilog netlist name and/or the DEF file name is different from the cell or module name. You must provide the full path (absolute or relative) with the file names. After you specify a set of DEF file name and Verilog Netlist name, click the Add button to add the files to the list of block-level designs that will be assembled. Repeat this for each block-level design.
Add	Adds the block design data, or the set of DEF file name and Verilog netlist name, to the list of block-level designs that will be assembled.	
Specify Full Chip Floorplan File	Specifies the chip-level floorplan file. By default, the command reads in the floorplan file from the provided top-level design. Use this option for the top-down hierarchical flow.	
Bring Back Rows	Specifies that row information should be brought back from the block-level design.	

Related Topics

- For information on Partition commands, see Partition Commands in the *Text Command Reference*.
- For information on Partitioning the Design, see *Partitioning the Design* in the *User Guide*.

Change Partition View

Use the *Change Partition View* menu command to toggle the design display area view between the selected partition and the top-level design.

Note: This menu command does not have an associated GUI form.

Tip: This command is only for viewing and examining into the partition. Real work that is to be done in a partition must be done in the created partition directories, which were created when saving the partitions.

- Highlight a partition in the design display area and choose *Partition* - *Change Partition View* .

Related Text Commands

There are no related text commands. This feature is available only through the *Partition* menu.

6

Floorplan Menu

- Macro Timing Slack Analysis
- Edit Floorplan
    - Cut Rectilinear
    - Create Size Blockage
    - Create Placement Blockage
    - Create Routing Blockage
    - Create Pin Blockage
    - Align
    - Shift
    - Space
    - Flip/Rotate
    - Edit Halo
    - Edit Routing Blockage
    - Color Module
    - Legalize Floorplan
    - Set Instance Placement Status
- Snap Floorplan
- Check Floorplan
- Clear Floorplan
- Instance Group
- Generate Regrouped Netlist
    - Group Pin(s) Move
    - Swap Two Selected I/O Cells
- Generate Floorplan
    - Prototype Design
    - Initialize Fast Timing Analysis
    - Fast Slack Analysis/Display

  - Generate Fence
  - Place Macros

Specify Floorplan

Use the *Specify Floorplan* form to view or change your floorplan specifications after importing the design. Use this form to specify the dimensions by size; or by die, I/O, or core coordinates. When you use the *Specify Floorplan* form (or specify the floorplan through the `floorPlan` command), the floorplan is resized automatically - relatively floorplan constraints are automatically derived on the fly for blocks, fixed standard cells, fixed pre-routes, and blockages.

The floorplan is linearly adjusted as follows:

- Spacing among blocks is evenly adjusted.
- The size of the modules and black boxes is evenly adjusted.
- The fixed pre-routes and I/Os are automatically adjusted.

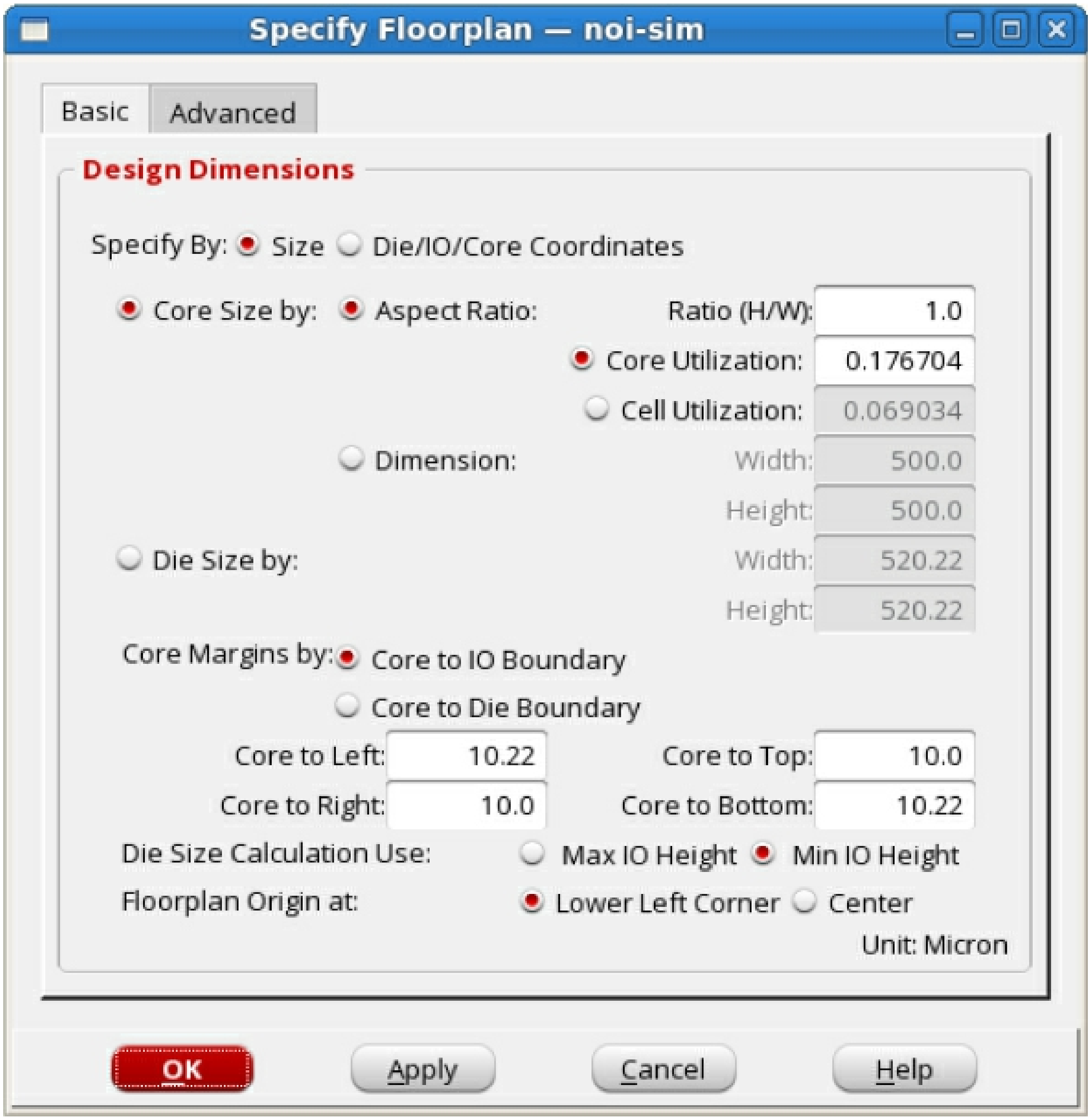
The Specify Floorplan Plan consists of the following two pages:

- Specify Floorplan - Basic
- Specify Floorplan - Advanced

Specify Floorplan - Basic

Use the *Specify Floorplan - Basic* form to specify the design dimensions.

- Choose *Floorplan* - *Specify Floorplan*, and then click the *Basic* tab.



Specify Floorplan - Fields and Options

Size	Specifies that the design dimensions are specified by size. If you select this option, specify the details in *Core Size* or *Die Size* fields.
Die/IO/Core Coordinates	Specifies that the design dimensions are specified by die, I/O, or core coordinates. Specify the Die/IO/Core lower left (ll) and upper right (ur) coordinates in the fields that are displayed if you select this option.

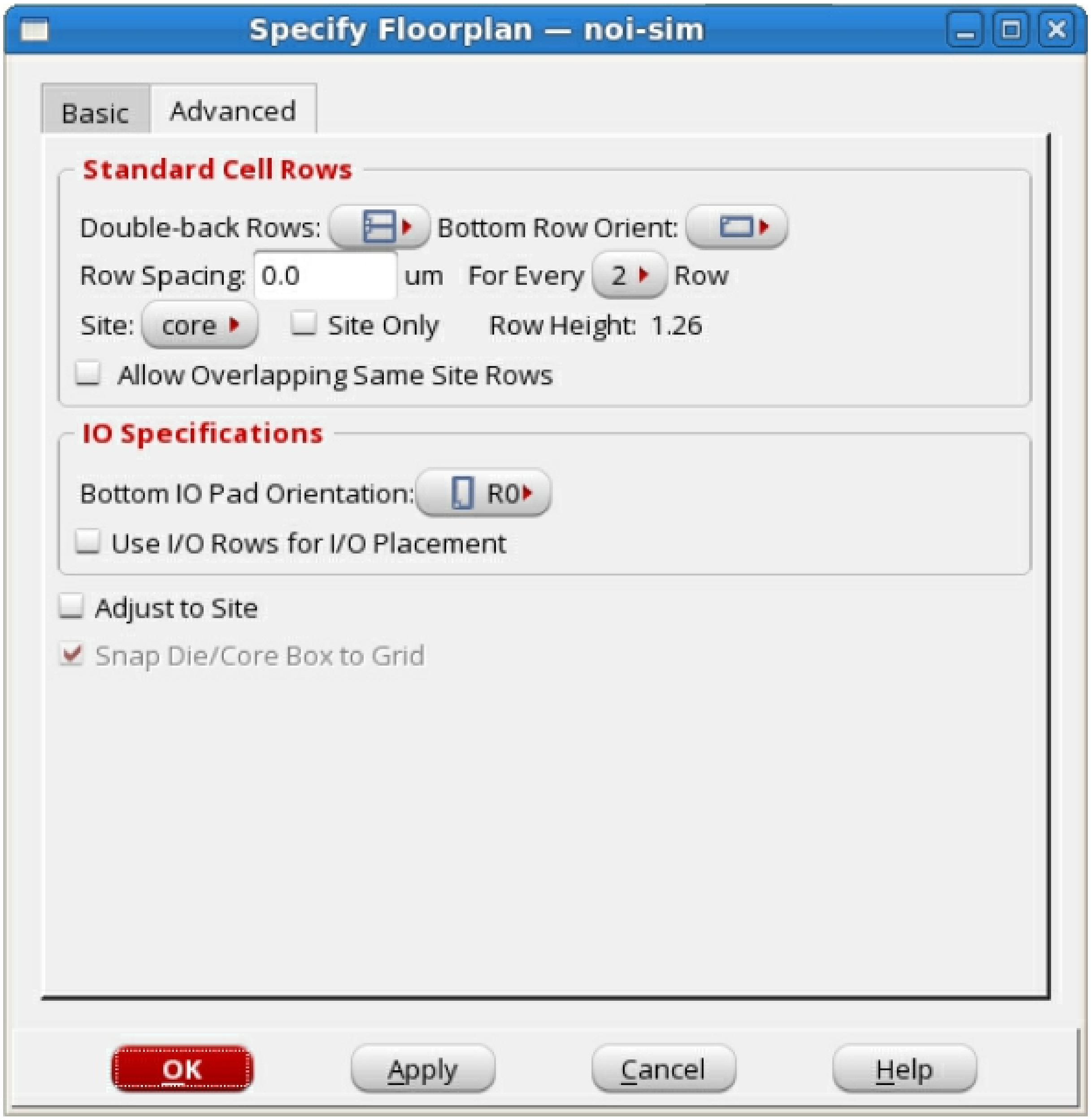
Core Size by	Specifies the core size dimension definition. *Aspect Ratio* defines the chip's core dimensions as the ratio of the height divided by the width. If a value of 1.0 is used, a square chip is defined. A value of 2.0 will define a rectangular chip with height dimension that is twice the width dimension. Choose one of the following ways of determining core and module sizes: *Core Utilization* determines the core and module sizes by total standard cells and macros density. *Cell Utilization* determines the core and module sizes by standard cell density. *Dimension* specifies the core's *Width* and *Height* values, in micrometers. For more information on total density versus standard cell density calculation, see Calculating Density in the *Innovus User Guide*.
Die Size by: Width and Height	
	Specifies the design's die size, in micrometers.
Core Margins by	Specifies the core margin dimension definition. Choose one of the following: *Core to IO Boundary* uses the spacing, in micrometers, between the core edge and the I/O box, which is the margin between the outside edge of the core box and the inside edge of the I/O box. The margin values and the height of the I/O pad instances determines the die size. You can specify the margins on all four sides: *Core to Left*, *Core to Bottom*, *Core to Right*, and *Core to Top*. *Core to Die Boundary* uses the spacing, in micrometers, between the core edge and the die edge, which is the margin between the outside edge of the core box and the inside edge of the die (head) box. This sets the die size once the core size is calculated. You can specify the margins on all four sides: *Core to Left*, *Core to Bottom*, *Core to Right*, and *Core to Top*.
Die Size Calculation Use	Specifies the die size and I/O box calculation when using *Core Margins by*. The height of the I/O pad instance determines the final die size calculation. Choose one of the following: *Max I/O Height* uses the tallest height I/O pad instance dimension to calculate the die size. *Min I/O Height* uses the shortest I/O pad instance dimension to calculate the die size.

Floorplan Origin at	Specifies the floorplan's origin. Choose one of the following: *Lower Left Corner* when loading a design that has its origin at the lower left. All files saved or output will reference the origin selection. *Center* when loading a design that has its origin at the center of the core.

Specify Floorplan - Advanced

Use the *Specify Floorplan - Advanced* form to specify the standard cell rows and bottom I/O pad orientation.

- Choose *Floorplan - Specify Floorplan* and then click the *Advanced* tab.



Specify Floorplan - Advanced Fields and Options

Row Direction	Specifies whether the rows are horizontal or vertical. **Note:** Support for vertical rows is a beta feature. Usage and support of this beta feature are subject to prior agreement with Cadence. Contact your Cadence representative if you have any questions.

Double-back Rows	Allows the selection of standard cell row pair orientations. The orientation selections for the row pair are bottom-to-bottom or top-to-bottom. The default is bottom-to-bottom orientation.
Bottom Row Orient (*Bottom/Left Row Orient*, if vertical row support is enabled)	Specifies the orientation of the bottom/left row in the core area. The default is an `R0` orientation, or you can choose the `MX` orientation (mirrored through the x axis) for horizontal rows or MY orientation for vertical rows. **Note:** Support for vertical rows is a beta feature. Usage and support of this beta feature are subject to prior agreement with Cadence. Contact your Cadence representative if you have any questions.
Row Spacing for Every # rows	
	Specifies the standard row spacing, in micrometers. This must be a positive value. By default, this value is zero. In the *For Every Row* pull-down menu, specify *1* for every row, or *2* for every other row.
Site	Specifies a core row site. The tech site names listed in the pull-down menu come from the *LEF Files* field of the Design Import form.
Site Only	Creates rows only for the specified *Site*.
Row Height	Specifies the standard cell row height, in micrometers. During design import, the standard cell row height is automatically determined.
Allow Overlapping Same Site Rows	
	If selected, specifies that same-site rows can overlap with one another. If deselected, specifies that same-site rows cannot overlap with one another. Single height rows must not overlap. Only double- or multiple-height rows can overlap. The overlap must be in sections that are multiple of single height--any other overlap section size will result in the rows being ignored.

Bottom IO Pad Orientation	Specifies an orientation of *R0* (default), *R90*, *R180*, and *R270*. If the bottom I/O pad orientation is changed, the other three sides will also change. The west side is rotated 90 degrees counterclockwise from the bottom I/O pad orientation; the north side is rotated 180 degrees counterclockwise from the bottom I/O pad orientation; and the east side is rotated 270 degrees counterclockwise from the bottom I/O pad orientation. The default orientation of the bottom I/O pad instance is *R0*; however, during design import, the software approximates the I/O pad orientation.
Use I/O Rows for I/O Placement	
	Enables I/O row based pad placement.
Adjust to Site	Adjusts the width of the die area such that it is an integer multiple of the width of the IO site or core site.
Snap Die/Core Box to Grid	
	Specifies that the core box (or die box) boundary will be snapped to the nearest metal pitch if the specified die/core box size is not an integer multiple of the smallest metal pitch. **Note:** This check box is disabled when you specify the floorplan dimensions by *Size* on the *Floorplan - Specify Floorplan - Basic* form and select the *Core Size by* and *Aspect Ratio* options.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `floorPlan`
- `setBottomIoPadOrient`
- `setFlipping`
- `setFPlanRowSpacingAndType`

Related Topics

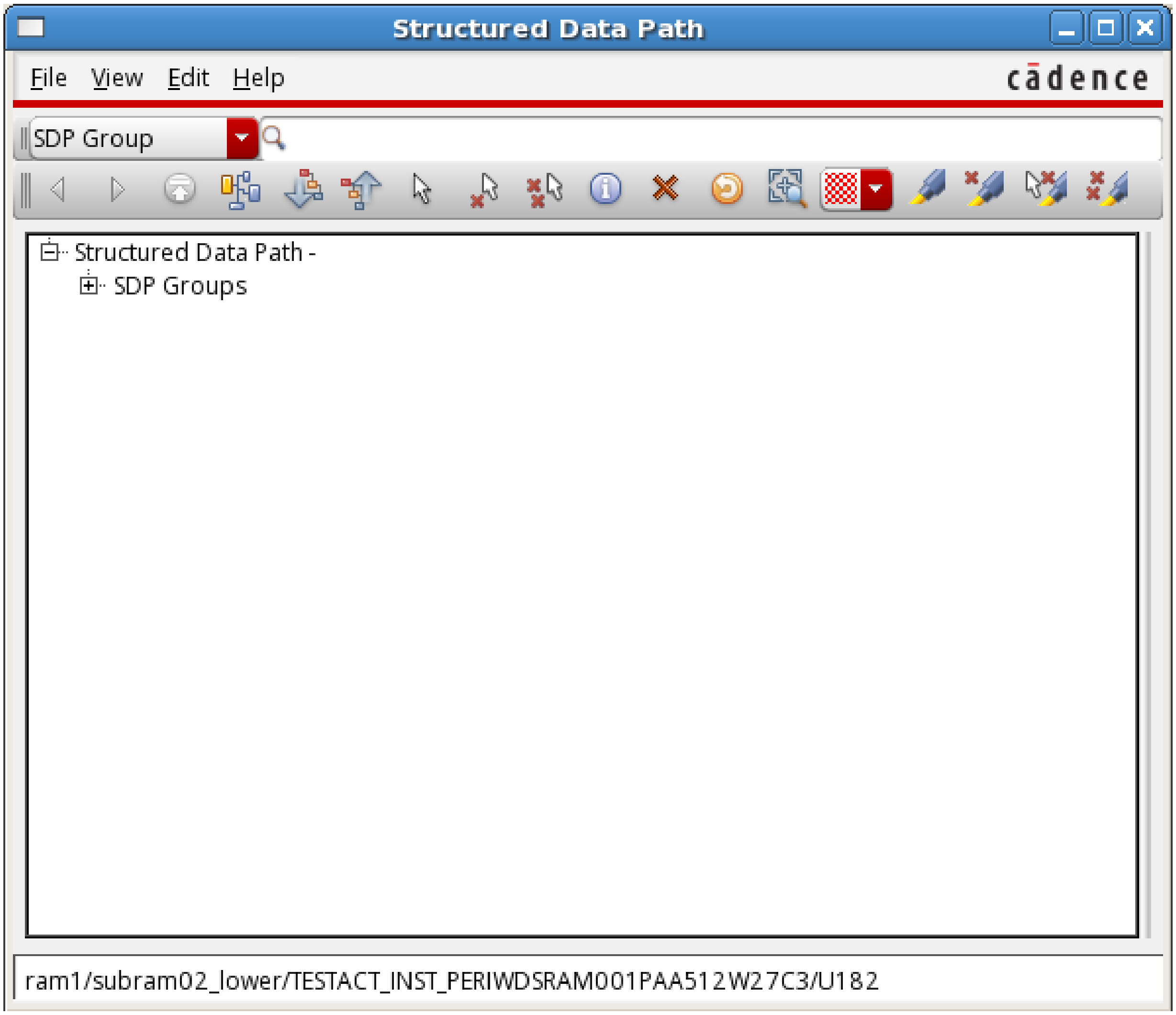
- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Structured Data Path

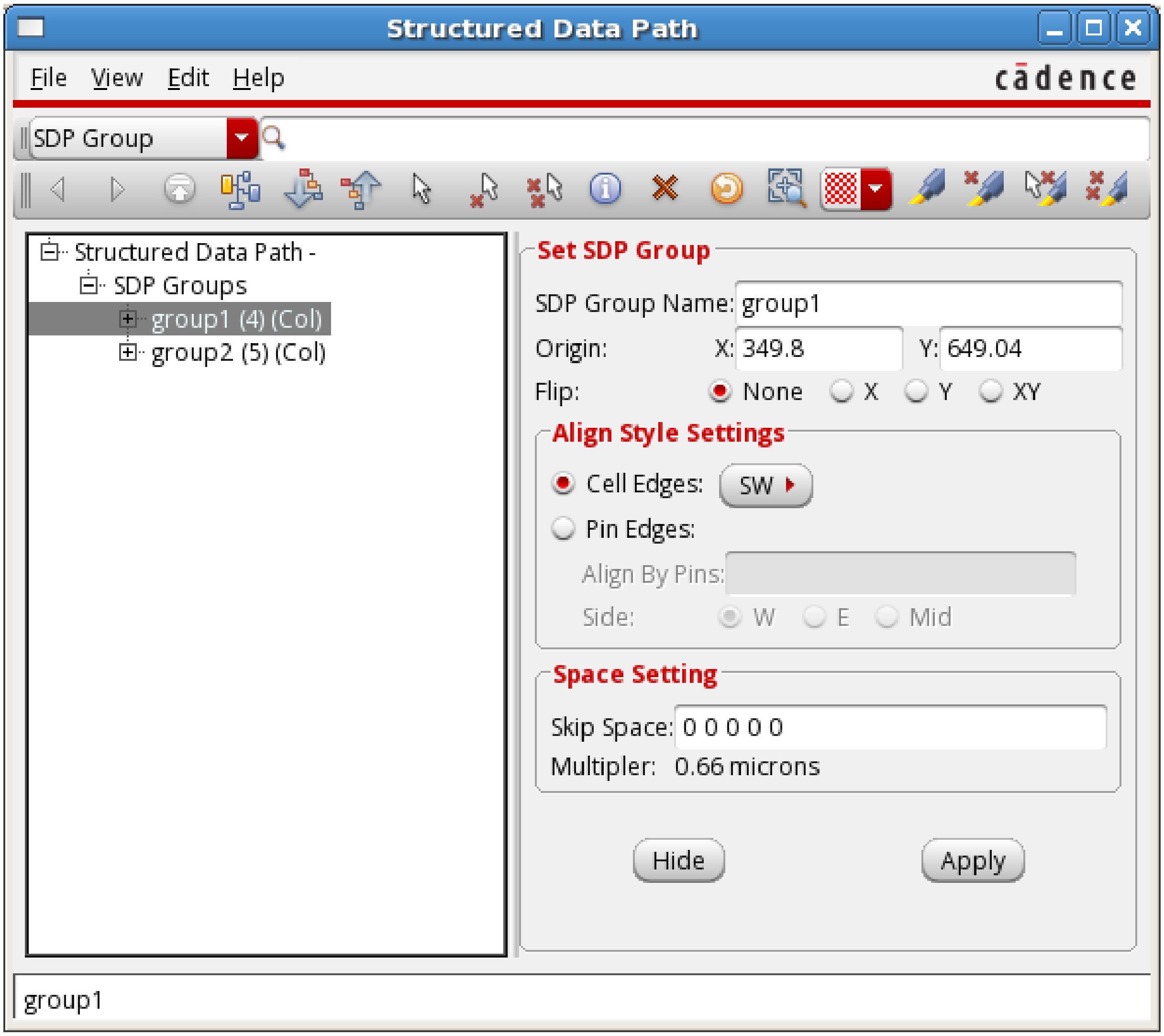
Use the *Structured Data Path* form or SDP browser to manipulate SDP groups and/or their elements easily.

In the SDP browser, you can also directly drag and drop an SDP group or instance to a new location using the middle mouse button.

- Choose *Floorplan - Structured Data Path*.



If you expand the *SDP Groups* node and select any SDP group, the settings for that group are displayed on the right pane of the SDP browser:



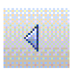
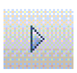
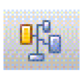
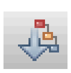
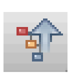
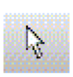
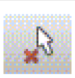
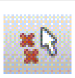
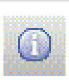
Structured Data Path Fields and Options

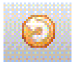
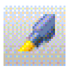
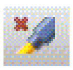
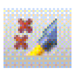
File	The *File* menu provides the following options:	
	Load	Displays the Load SDP File form which you can use to load the SDP file in relative placement language format.
	Save As	Displays the Save Relative Placement File form which you can use to save the SDP file in relative placement language format.
	Create Template File	Creates a sample SDP file.

	Quit	Closes the SDP browser.
View	The *View* menu provides the following options:	
	Refresh	Redraws the SDP browser display.
	Zoom Selected	Zooms into the object you have selected in the SDP browser in the design display area.
	Show Connectivity	Opens the Show SDP Connectivity form, which is used to display connectivity for the selected SDP group.
	Clear Connectivity	Clears all connectivity information.
	Get Selected	Expands and browses the SDP group for the selected instance.
Edi*t*	The *Edit* menu provides the following options:	
	Flip X	Flips the selected SDP group(s) or instance(s) on the X axis. The cells inside the SDP are also flipped.
	Flip Y	Flips the selected SDP group(s) or instance(s) on the Y axis. The cells inside the SDP are also flipped.
	Edit Attribute	*Attribute Editor*--Opens the Attribute Editor form. For more information, see Attribute Editor in the Edit Menu chapter.
	Delete Selected SDP Group	Deletes the selected SDP group and updates relative placement in the design display area.
	Insert Space before/after SDP Group	Opens the Insert Space before/after SDP Group form, which is used to insert space before or after the selected SDP group(s). The relative placement in the design display area is updated.
	Create SDP Group for Selected Instance	Opens the Create SDP Group for Selected Instances form, which can be used to create an SDP group from the instance(s) that are currently selected in the design display area.

Structured Data Path Tool Widgets

You can use the widgets in the SDP browser to navigate through displays, make selections, and perform actions.

Widget	Description
	Allows you to search for specified SDP objects: • *SDP Group*--Searches for specified SDP group. • *SDP Instance*--Searches for specified SDP instance. You can use wildcards to specify object names in the text input box. When you enter text in the text input box, the Clear button () is displayed next to the text input box. Use this button to clear any existing text in the input box.
	*Previous*--Displays viewable data in a reverse direction.
	*Next*--Displays viewable data in a forward direction.
	*Top*--Returns to the top node.
	*Show Connectivity*--Opens the Show SDP Connectivity form, which is used to display connectivity for the selected SDP group.
	*Expand All Group* --Click this widget to expand all SDP groups.
	*Collapse All Group*--Click this widget to collapse all the SDP groups.
	*Select Instances*--Selects instances related to the selected group in the design display area.
	*Deselect Instances*--Deselects instances related to the selected group in the design display area.
	*Deselect All*--Deselects all instances in the design display area.
	*Attribute Editor*--Opens the Attribute Editor form for the selected group.
	*Delete Selected SDP Group*--Deletes the selected SDP group.

	*Refresh*--Refreshes the SDP browser display.
	*Zoom Selected*--Select one or more groups, then click this widget to zoom into the design display area that contains the selected group.
	*Edit Highlight Color*--Allows you to select a highlight color from the available choices in the drop-down menu.
	*Highlight*--Highlights instances related to the selected group in the design display area.
	*Dehighlight*--Dehighlights instances related to the selected group in the design display area.
	*Dehighlight Selected*--Dehighlights the selected object.
	*Dehighlight All*--Dehighlights all objects in the design display area.

Related Topics

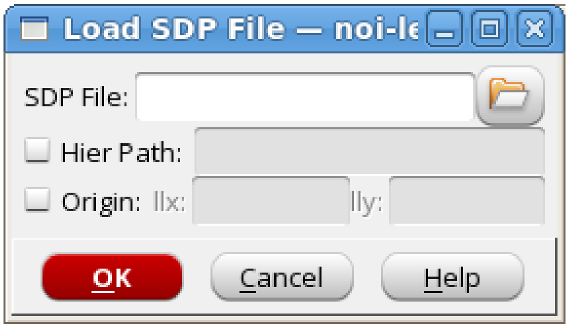
- For information on SDP commands, see Structured Data Path Commands in the *Text Command Reference*.
- For information on the SDP flow, see *Using Structured Data Paths* in the *User Guide*.

Load SDP File

Use the Load SDP File form to read a relative placement file (in .sdp format) containing SDP definitions and place all SDP elements defined in the input file. If the SDP(s) do not have origin information, they are placed outside the die area on the right hand side. The Load SDP File form makes it easy for you to define SDPs in the Innovus environment.

To access the Load SDP File form:

1. Choose *Floorplan - Structured Data Path*.
2. In the SDP browser, choose *File - Load.*



Load SDP File Fields and Options

SDP File	Specifies the name of the input file containing SDP definitions.
Hier Path	Specifies the hierarchical path name of the SDP elements specified in the SDP file. This path name is appended to all SDP instances defined in the file.
Origin	Defines the SDP location by specifying the SDP block origin. The origin information is applied to all SDPs specified in the SDP file.

Related Text Commands

- `readSdpFile`

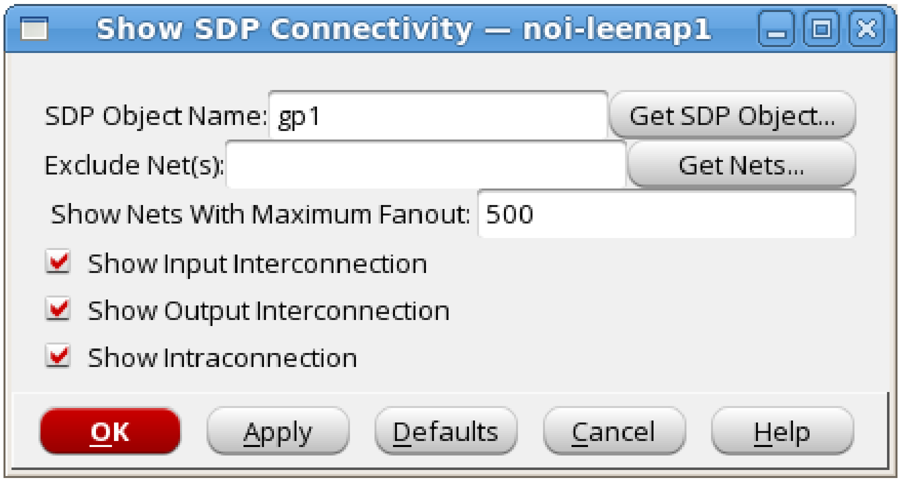
Show SDP Connectivity

Use the Show SDP Connectivity form to display connection information or flightlines for the selected SDP group. You can change the color of SDP connections or flightlines using the SDP Connection Color Selection form.

To access the Show SDP Connectivity form:

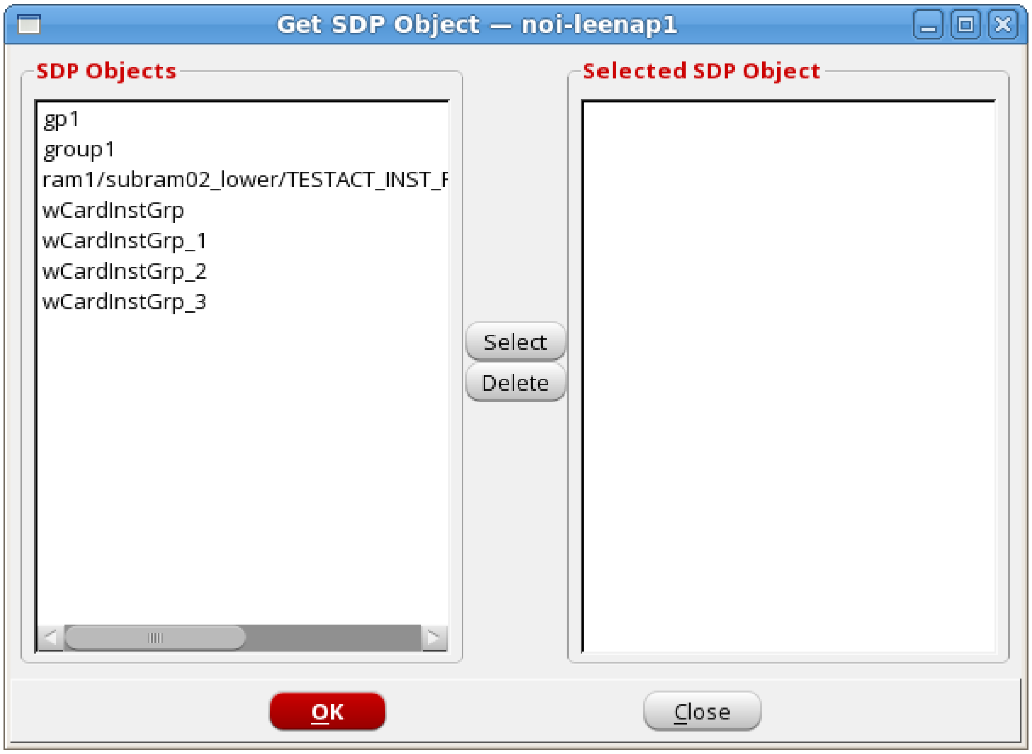
1. Choose *Floorplan - Structured Data Path*.
2. In the SDP browser, select an SDP group and:
    - Choose *View - Show Connectivity.*
      OR

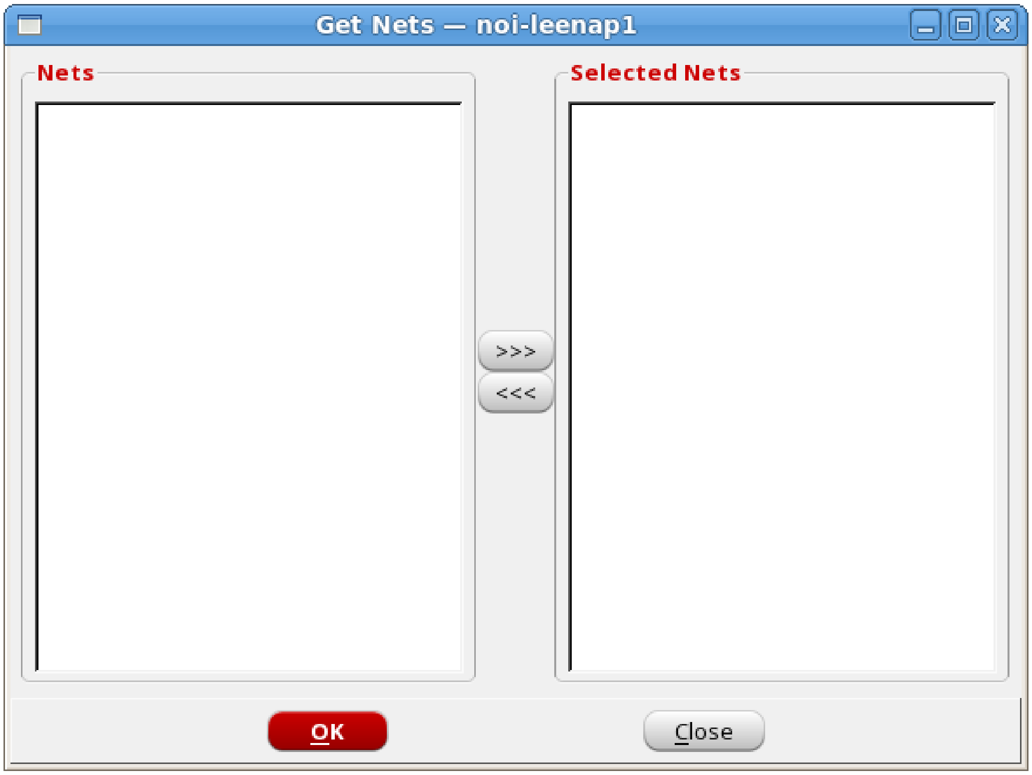
- Click the *Show Connectivity* widget on the SDP browser toolbar.



Show SDP Connectivity Fields and Options

SDP Object Name	Specifies the name of the SDP group or object for which you want to display connection information.

Get SDP Object	Opens the Get SDP Object form in which you can select the SDP object for which you want to display connection information: 
Exclude Net(s)	Excludes display of flightlines of specified nets. Use this option to exclude nets with many fanouts. Flightlines of such nets may crisscross all over the design display area making it difficult for you to view flightlines of other nets.

Get Nets	Opens the Get Nets form in which you can select the nets you want to exclude: 
Show Nets With Maximum Fanout	Specifies the maximum fanout limit. By using this option, you can restrict display to flightlines of only those nets that have fewer fanouts than the number specified. This is a good way of excluding nets with large fanouts, such as clock nets and reset nets.
Show Input Interconnection	Specifies whether or not you want to show input interconnections.
Show Output Interconnection	Specifies whether or not you want to show output interconnections.
Show Intraconnection	Specifies whether or not you want to show intraconnections.

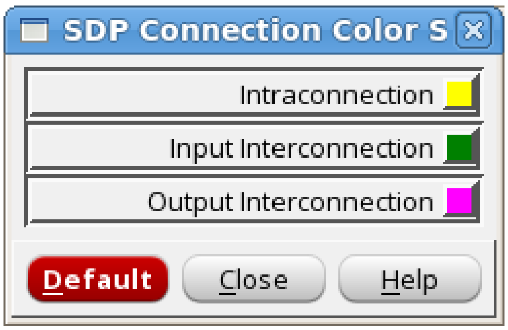
SDP Connection Color Selection

Use the SDP Connection Color Selection form to configure the colors of intraconnections and input and output interconnections.

To open the SDP Connection Color Selection form:

1. Click the *All Colors* button in the main window to open the Color Preferences form.
2. Open the *Objects* page.
3. Click on the color indicator box for the *SDP Connection* object.

Note: If you do not want to display SDP flightlines, turn them off by deselecting the Visibility (*V*) check box for *SDP Connection* object on the *View-Only* page.



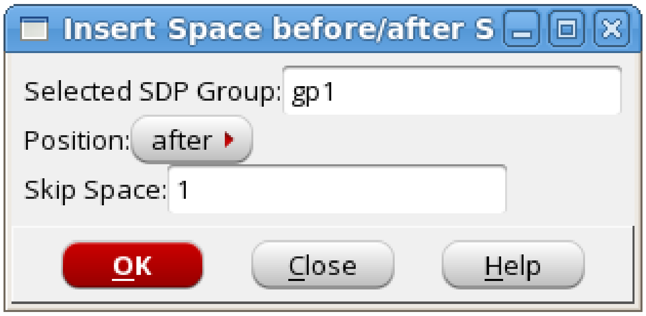
SDP Connection Color Selection Fields and Options

Intraconnection	Specifies the color of intraconnections. Click the color indicator next to Intraconnections to select a different color in the Select Color form.
Input Interconnection	Specifies the color of input interconnections. Click the color indicator to select a different color.
Output Interconnection	Specifies the color of output interconnections. Click the color indicator to select a different color.

Insert Space before/after SDP Group

Use the Insert Space before/after SDP Group form to insert space before or after the selected SDP group. The relative placement in the design display area is updated.

1. Choose *Floorplan - Structured Data Path*.
2. In the SDP browser, select an SDP group and choose Edi*t - Insert Space before/after SDP Group.*



Insert Space before/after SDP Group Fields and Options

Selected SDP Group	Specifies the SDP group before/after which you want to insert space or empty rows
Position	Specifies whether you want to insert space before or after selected SDP group.
Skip Space	Indicates the number of spaces or empty rows to be inserted. *Default*: 1

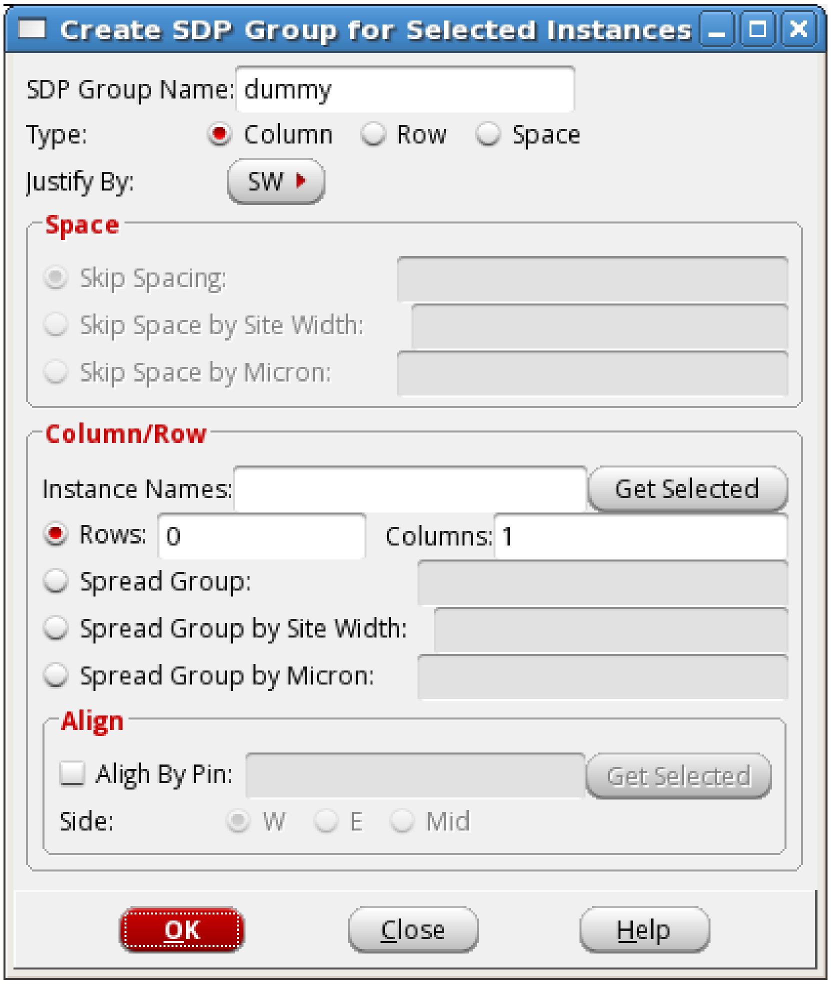
Related Text Commands

- `addSdpObject`

Create SDP Group for Selected Instances

Use the Create SDP Group for Selected Instances form to create an SDP group from the instance(s) that are currently selected in the design display area.

1. Select an instance in the design display area and choose *Floorplan - Structured Data Path*.
2. In the SDP browser, choose Edi*t - Create SDP Group for Selected Instances*.



Create SDP Group for Selected Instances Fields and Options

SDP Group Name	Specifies the name of the new SDP group you are creating. *Default*: `dummy`
Type	Indicates whether the new group is a row, column, or an empty (skipped) space. *Default*: *Column*
Justify By	Specifies the anchor point that will be used to align the SDP group you are creating. *Default*: *SW*

Skip Spacing	Specifies a space value to be skipped. Use the *Skip Spacing* option with the *Type - Space* option to add row/column spaces. By default, if *Skip Spacing* is defined in a column, its value represents the number of skipped rows. If *Skip Spacing* is defined in a row, its value is for column skipping and represents the number of M2 tracks (pitch of first vertical layer). Skip space value can also be specified as number of widths of a specified row site by using the *Skip Space by Site Width* option. However, row site width should be specified only for an SDP row, and not for an SDP column. Alternatively, you can specify the *Skip Space by Micron* option to specify the distance to be skipped in microns (`um`).
Skip Space by Site Width	Specifies the number of row/column space to be skipped and the name of the tech site. Uses the width of the specified site as the skip unit in the horizontal direction. **Note**: This option cannot be used with either *Skip Spacing* or *Skip Space by Micron*.
Skip Space by Micron	Specifies the space value to be skipped in microns (`um`). If the specified distance value is not equal to the exact number of first vertical metal pitches or number of rows, the tool rounds off the value. **Note**: This option cannot be used with either *Skip Spacing* or *Skip Space by Site Width*.
Instance Names	Specifies one or more instance names. Use this option if you want to create the SDP group from the specified instances.
Rows	Indicates the number of rows to be created. *Default*: 0
Columns	Indicates the number of columns to be created. *Default*: 1 **Note:** If you specify both *Rows* and *Columns*, use the *Type* option to specify the parent structure type (*Row* or *Column*). If you do not specify type, the default parent structure will be column.
Spread Group	Inserts space between group of instances. If *Spread Group* is specified in a column, spacing will be the number of added rows. If *Spread Group* is specified in a row, spacing will be the number of placement grids added between the columns in that row.

Spread Group by Site Width	Specifies the number of row/column space to be inserted and the name of the tech site. Uses the width of the specified site as the spread unit in the horizontal direction. **Note**: This option cannot be used with either *Spread Group* or *Spread Group by Micron*.
Spread Group by Micron	Specifies the space to be inserted between groups of instances in microns (`um`). **Note**: This option cannot be used with either *Spread Group* or *Spread Group by Site Width*.
Align by Pin	Specifies the pin names by which you want to align SDPs. **Note:** You can specify this option only for a column SDP group.
Side	Indicates the pin edge to be used for alignment. *Default*: *W*

Related Text Commands

- `createSdpGroup`

Automatic Floorplan

The Automatic Floorplan menu provides the following forms and menu commands for running the features of the Automatic Floorplan Synthesis:

- Plan Design
- Refine Macro Placement
- Finish Floorplan
- Check Floorplan Space Rule

Plan Design

The Plan Design form enables you to set the Automatic Floorplan Synthesis global parameters, and run the Automatic Floorplan Synthesis feature to generate quick, initial floorplans.

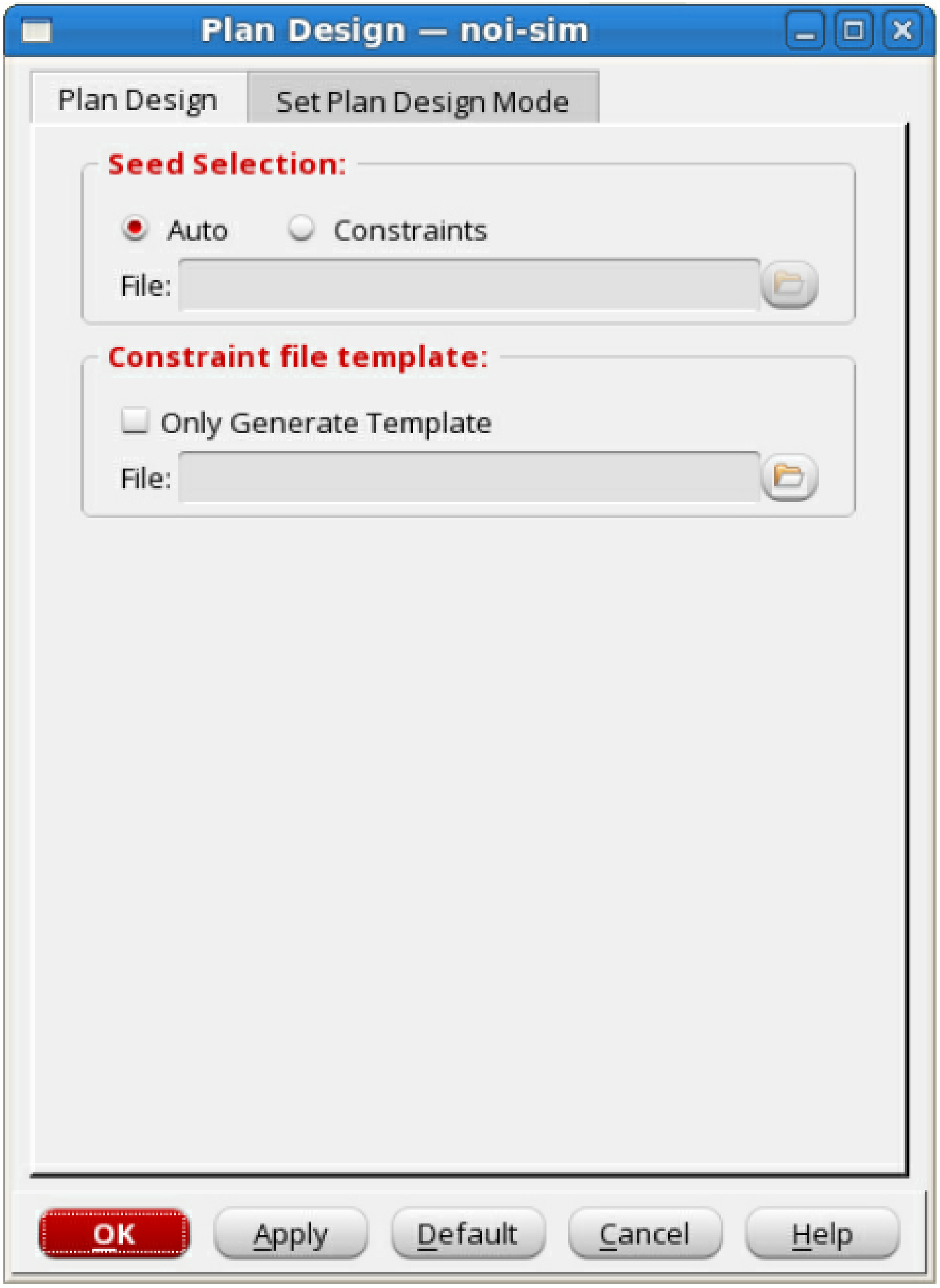
The Plan Design form includes the following pages:

- Plan Design - Plan Design
- Plan Design - Set Plan Design Mode

Plan Design - Plan Design

Use the P*lan Design* page to generate a quick, initial floorplan that can be used as a starting point for making the final floorplan. Use Automatic Floorplan Synthesis to create multiple floorplans. You can then test the floorplans to find the one that gives you the best placement and routing results. When you click *OK*, Automatic Floorplan Synthesis performs the following internal functions in order:

- Selects the floorplan objects (called seeds) to be placed.
- Places the seeds.
- Refines the seeds.
- Places the macros.
- Choose *Floorplan - Automatic Floorplan - Plan Design*.


Plan Design — noi-sim
Plan Design
Set Plan Design Mode
Seed Selection:
Auto
Constraints
File:
Constraint file template:
Only Generate Template
File:
OK
Apply
Default
Cancel
Help

planDesign - Fields and Options

Auto	Performs automatic seed selection. Automatic Floorplan Synthesis selects seeds using the following methods in the specified order: • Chooses modules that fit an internally calculated size range • Chooses large hard macros as seeds • Groups small modules or single standard cells to fit an internally calculated size range *Default:* On
Constraints	Uses the constraints set in the specified Automatic Floorplan Synthesis constraint file for fence creation, macro placement and module guide generation. A constraint file is a text file that can contain a list of seeds for Automatic Floorplan Synthesis to use when generating fences and module guides, and basic relative, spacing and orientation constraints to follow during macro placement. *Default:* Off
File	Specifies the name a constraint file.
Only Generate Template	Generates a template of the Automatic Floorplan Synthesis constraint file in the current working directory. When specified, the software creates the file only; it does *not* generate a floorplan (that is, it does not run `planDesign`).
File	Specifies the name of the constraint file template. If you do not specify a name, the software creates a file named constr.tmp.

Related Text Commands

- `planDesign`
- `setPlanDesignMode`

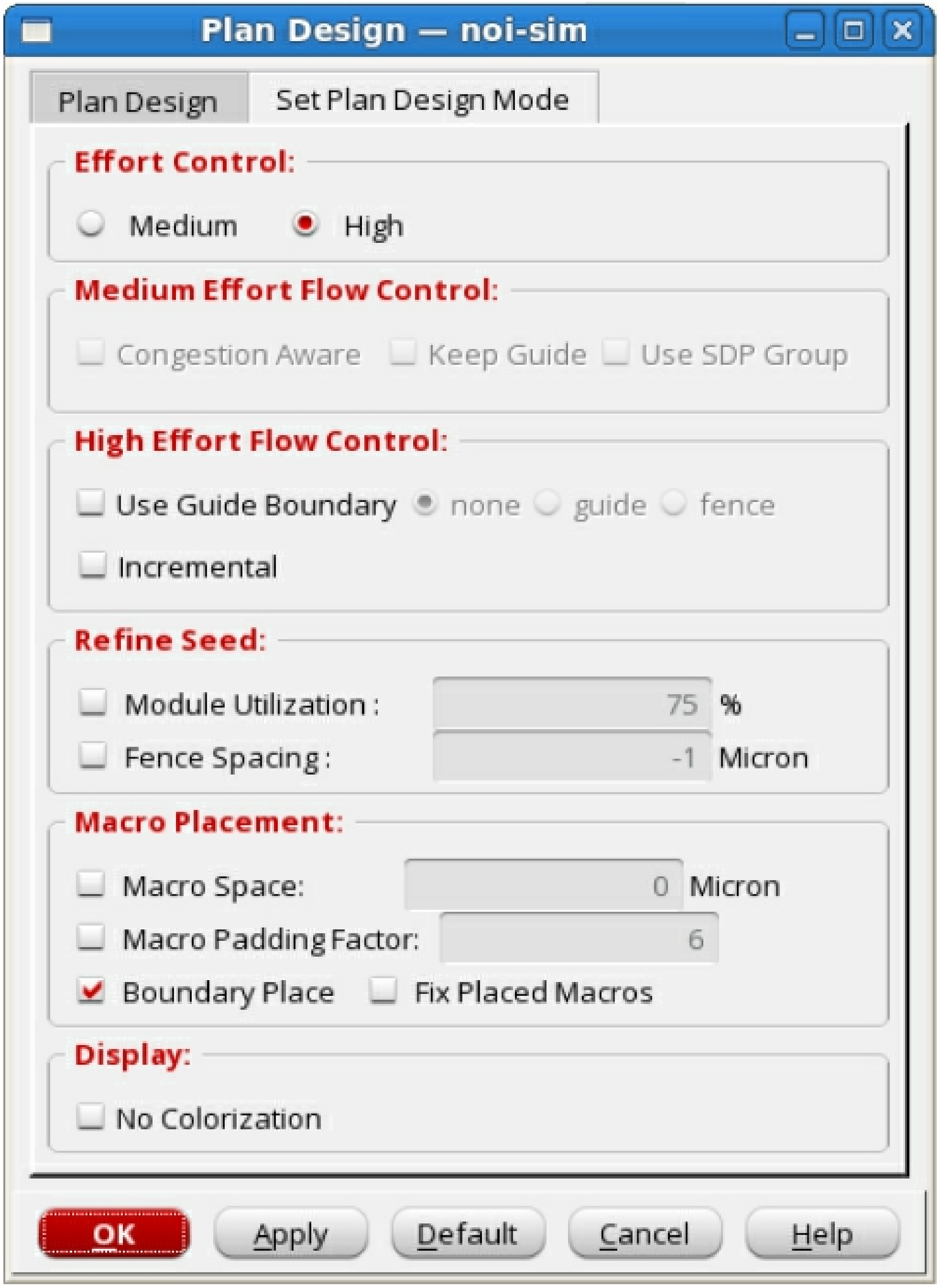
Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.
- For information on Data Preparation, see *Data Preparation* in the *User Guide*.

Plan Design - Set Plan Design Mode

Use the S*et Plan Design Mode* page of the Plan Design form to set the Automatic Floorplan Synthesis global parameters. Parameters specified with the S*et Plan Design Mode* page are then used whenever you run the Automatic Floorplan Synthesis feature to create an initial floorplan.

- Choose *Floorplan - Automatic Floorplan - Plan Design*, and click the S*et Plan Design Mode* tab.



Plan Design - Set Plan Design Mode Fields and Options

Effort Control	Specifies the effort level to use for Plan Design. By setting effort level to *High*, Plan Design performs concurrent macro and standard placement to help get better macro location. Default: Medium
Congestion Aware	Estimates the congestion for the floorplan after macro placement. If congestion is greater than 0.5 percent in either the X or Y direction, Automatic Floorplan Synthesis attempts to resolve it by refining the macro placement (such as changing the spacing, orientation, or grouping). Automatic Floorplan Synthesis does not touch user-preplaced macros during this refinement. After re-estimating the congestion, if the congestion improved, Automatic Floorplan Synthesis keeps the new floorplan. If congestion did not improve, Automatic Floorplan Synthesis restores the previous floorplan. *Default:* Off
Keep Guide	Retains the Automatic Floorplan Synthesis-generated module guides after the floorplan has been created. *Default:* Off
Use SDP Group	Specifies support for placing structured data path objects during `planDesign`. With this option selected, Plan Design places SDP instance groups and their elements.
Use Guide Boundary	Places the macros that belong to a guide constraint inside the guide boundary during Plan Design. • *none*: Ignores guide constraint in Plan Design • *guide*: Honors guide constraint in Plan Design • *fence*: Treats guide constraint as fence in Plan Design
Incremental	Performs incremental macro placement. **Note:** When this field is selected, high effort `planDesign` supports incremental macro placement that honors existing fences and guides.

Module Utilization	Specifies the target utilization for generated floorplan guides. You can use this field to decrease congestion between fences during hierarchical floorplanning. *Default:* 75% In the fence generation flow with utilization set in set Plan Design Mode, the regular fence without any macro honors global utilization value. For fence with macro, the automatic fence generator uses lower utilization for fence (bigger in area), to make macro placement easier to legalize, and tries to get the utilization closer to global utilization. Any fence specific utilization setting in the constraint file overrides the global utilization setting for that fence.
Fence Spacing	Specifies the spacing between adjacent fences, in microns.
Macro Space	Specifies the spacing between adjacent hard macros, in microns.
Macro Padding Factor	Specifies the number of routing layers to be used in congestion estimation. you can specify a value between 0 and 128. *Default:* 0 When this option is set to a value greater than 0, the macro halos will be automatically estimated based on number of pins on each side of a macro together with the given number of routing layers. The smaller the given `macroPaddingFactor` is, the bigger the estimated macro halos will be. For example, the estimated macro halo with `macroPaddingFactor` 4 will be half width of that with `macroPaddingFactor` 2. By default 0, the auto halo estimation is turned off.
Boundary Place	Places macros along the core boundary for chip and block designs. Macros are placed along the fence boundary for hierarchical floorplans. Preplaced hard macro boundaries are also used, if possible. **Note:** Selecting this option can disable the *Max Distance To Guide* option. Seed locations might also be ignored.

Fix Placed Macros	Marks all placed macros as FIXED after running Automatic Floorplan Synthesis. Marking the macros as FIXED prevents them from accidentally being moved when the design is placed. *Default:* Off
No Colorization	Does not color the module guides and macros in the resulting floorplan. *Default:* off
Default	Uses the default automatic seed selection method for seed selection. By default, Automatic Floorplan Synthesis selects seeds using the following methods in order: • Chooses modules that fit an internally calculated size range • Chooses large hard macros as seeds • Groups small modules or single standard cells to fit an internally calculated size range *Default:* On

Related Text Commands

- `planDesign`
- `setPlanDesignMode`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Refine Macro Placement

Use the Refine Macro Placement form to adjust the placement of macros in the floorplan. You can adjust specific macro packs, or all of the macros in a specific area of the design.

- Choose *Floorplan - Automatic Floorplan - Refine Macro Placement*.

Refine Macro Placement - Fields and Options

Permute Pack	Adjusts the placement of a selected pack of macros to reduce empty area between them. A pack is a set of macros from the same seed that have similar sizes and aspect ratios and have been grouped together. **Note:** You must select the macro pack in the main window before using this option. You can select one macro to select the entire pack.	
Window Refine	Adjusts the placement of any macros within a specified area (*Target Window*) to reduce empty area between them.	
Target Window	Creates a box in the design window. Automatic Floorplan Synthesis adjusts any macros within the specified area to reduce empty area between them.	
	Point 1 X/Y	Specifies the coordinates of one corner of the box. This corner can be the lower-left, upper-left, lower-right, or upper-right corner of the box.
	Point 2 X/Y	Specifies the opposite corner of the box.
	Draw	Enables you to physically draw the box in the design window. The coordinates for where you start drawing the box populate the text fields for *Point 1*. The coordinates for where you finish drawing the box populate the text fields for *Point 2*.
Include Selected Macro	Moves the selected macros to the *Target Window* area, and adjusts their position along with any macros already within the area. **Note:** You must select one or more macros in the main window before using this option.	

Related Text Commands

- `refineMacro`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Finish Floorplan

Use the *Finish Floorplan* form to perform advanced placement-related refinements to a floorplan, to produce a more polished floorplan.

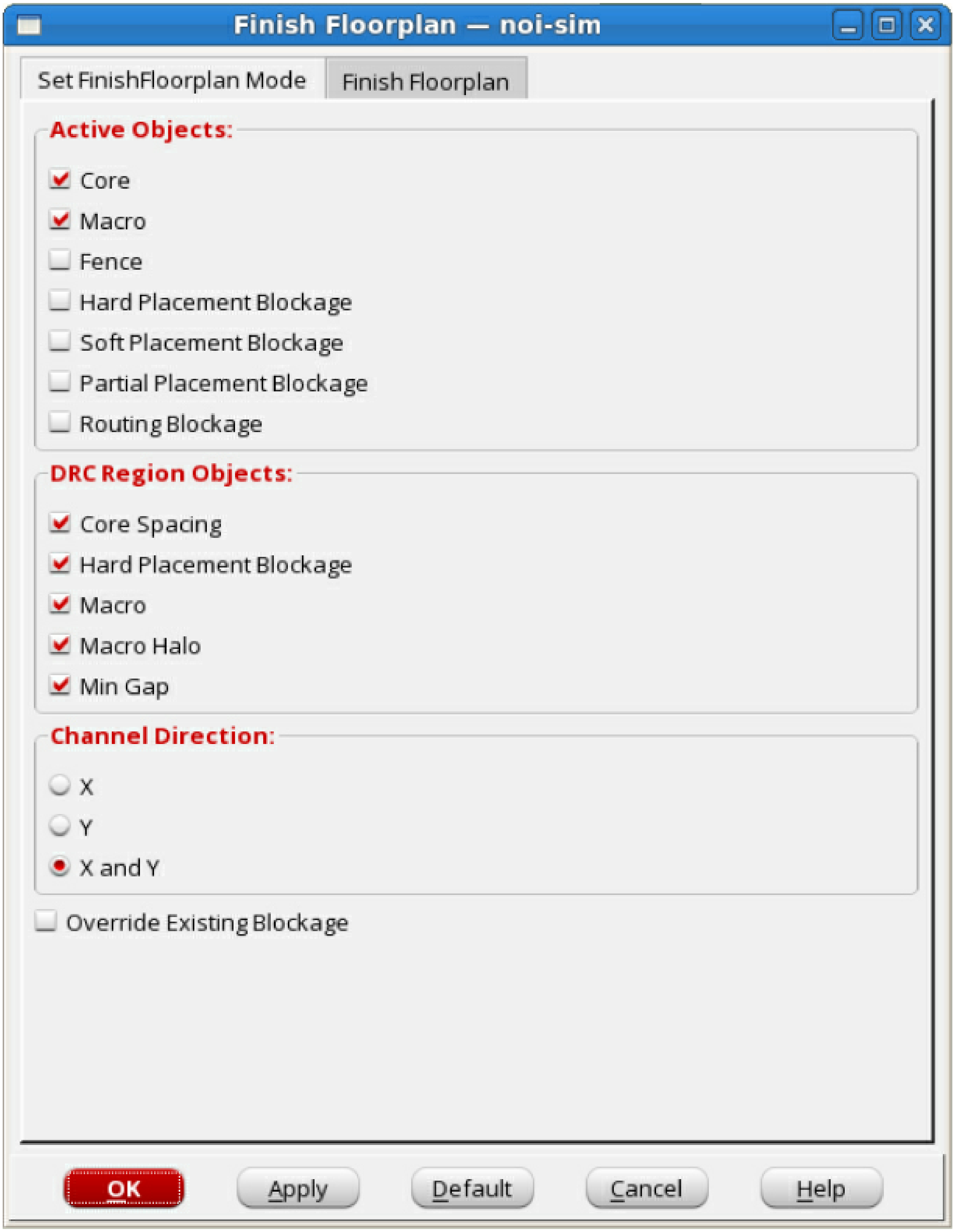
The *Finish Floorplan* form consists of the following two pages:

- Finish Floorplan - Set FinishFloorplan Mode
- Finish Floorplan - Finish Floorplan

Finish Floorplan - Set FinishFloorplan Mode

Use the *Finish Floorplan - Set FinishFloorplan Mode* form to set the active objects and specify the channel direction for the Finish Floorplan feature. The fields and options specified with this form are used whenever you run the Finish Floorplan capability to perform advanced placement-related refinements to a floorplan.

- Choose *Floorplan - Automatic Floorplan - Finish Floorplan*, and then click the S*et FinishFloorplan Mode* tab.


Finish Floorplan — noi-sim
Set FinishFloorplan Mode
Finish Floorplan
Active Objects:
Core
Macro
Fence
Hard Placement Blockage
Soft Placement Blockage
Partial Placement Blockage
Routing Blockage
DRC Region Objects:
Core Spacing
Hard Placement Blockage
Macro
Macro Halo
Min Gap
Channel Direction:
X
Y
X and Y
Override Existing Blockage
OK
Apply
Default
Cancel
Help

Finish Floorplan - Set FinishFloorplan Mode Fields and Options

Active Objects	Specifies that the boundaries of the selected active objects should be looked at while deciding where to add blockages. Non-active objects are treated like they don't exist by the Finish Floorplan capability. You can choose the active objects by selecting the following: • *Core* • *Macro* • *Fence* • *Hard Placement Blockage* • *Soft Placement Blockage* • *Partial Placement Blockage* • *Routing Blockage* *Default*: *Core* and *Macro*
DRC Region Objects	Specifies the DRC region object list. The boundaries of the specified DRC region objects are looked at while deciding where to add blockages. The DRC region objects can be: • *Core Spacing* • *Hard Placement Blockage* • *Macro* • *Macro Halo* • *Min Gap* *Default: Core Spacing, Hard Placement Blockage, Macro, Macro Halo,* and *Min Gap*

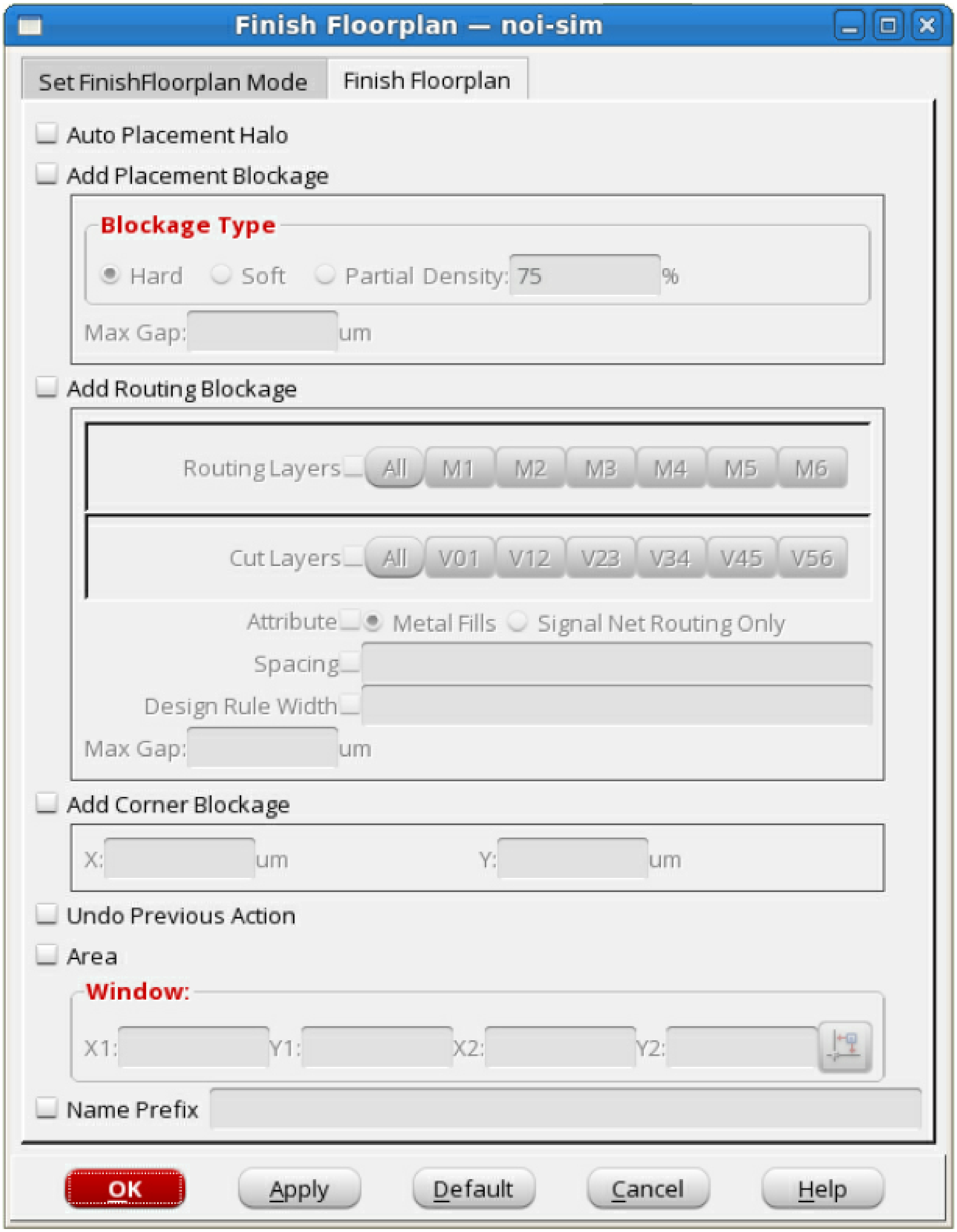
Channel Direction	Specifies the direction in which the blockage is added. You can choose the direction by selecting one of the following options: • *X*: Fills the channel whose height is less than width. • *Y*: Fills the channel whose width is less than height. • *X and Y*: Fills every channel whose smallest size (in X or Y direction) is within Max Gap range. *Default*: *X and Y*
Override Existing Blockage	Overrides old blockages that overlap with the new blockages.

Finish Floorplan - Finish Floorplan

Use the *Finish Floorplan - Finish Floorplan* form to to perform advanced placement-related refinements to a floorplan, to produce a more polished floorplan.

The Finish Floorplan form can be used on any floorplan, including third-party generated floorplans.

- Choose *Floorplan - Automatic Floorplan - Finish Floorplan*, and then click the *Finish Floorplan* tab.


Finish Floorplan — noi-sim
Set FinishFloorplan Mode
Finish Floorplan
Auto Placement Halo
Add Placement Blockage
Blockage Type
Hard
Soft
Partial Density:
75
%
Max Gap:
um
Add Routing Blockage
Routing Layers
All
M1
M2
M3
M4
M5
M6
Cut Layers
All
V01
V12
V23
V34
V45
V56
Attribute
Metal Fills
Signal Net Routing Only
Spacing
Design Rule Width
Max Gap:
um
Add Corner Blockage
X:
um
Y:
um
Undo Previous Action
Area
Window:
X1:
Y1:
X2:
Y2:
Name Prefix
OK
Apply
Default
Cancel
Help

Finish Floorplan - Finish Floorplan Fields and Options

Auto Placement Halo	Automatically add halos around every macro in design. For each macro edge, the halo thickness is proportional to pin density on that edge.	
Add Placement Blockage		
	Adds placement blockages around macros to reduce potential congestion after placement.	
	Blockage Type	
		Specifies the blockage type. For Blockage Type, you can select from Soft, Hard, or Partial.
	Max Gap	
		Adds placement blockage of the specified width, in microns.
	Override Macro Halo	
		Replaces the existing halo with new one. By default, the additional halo is added to the existing one.
Add Routing Blockage		
	Adds routing blockage upto a specified size.	
	Routing Layers	Specifies the layer ID of the route blockage.
	Cut Layers	Specifies the cut layer ID on which the routing blockage is to be applied.
	Attribute	*Metal Fill*: Specifies that the routing blockage is to be applied on metalfills. *Signal Net Routing Only*: Specifies that the routing blockage is to be applied on a signal net routing and not on power or ground net routing
	Spacing	Specifies the minimum spacing between layers within the routing blockage. The value is a real number greater than or equal to 0.

	Design Rule Width	Specifies the effective width of the routing blockage. The value is a real number greater than 0.
	Max Gap	Adds routing blockage of the specified width, in microns.
Add Corner Blockage		
	Adds a hard placement blockage around the corner.	
	X	Specifies the width of the hard placement blockage around the corner.
	Y	Specifies the height of the hard placement blockage around the corner.
Undo Previous Action		
	Reverses the previous run of `finishFloorplan`.	
Area	Specifies the lower left x coordinate, lower left y coordinate, upper right x coordinate, and upper right y coordinate respectively of the blockage area.	
Name Prefix	Specifies the name prefix for the added blockage to avoid naming conflict with the existing one.	

Related Text Commands

- `finishFloorplan`
- `setFinishFPlanMode`

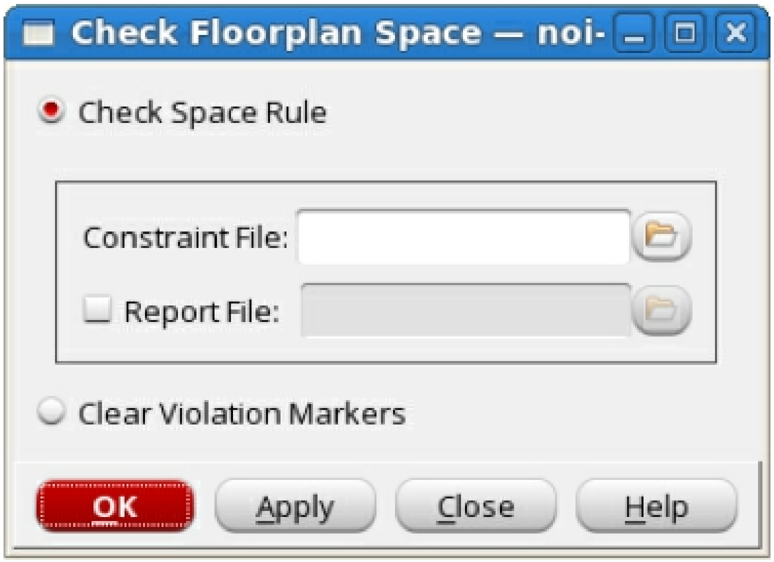
Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Check Floorplan Space Rule

Use the *Check Floorplan Space* form to check the floorplan for spacing rule violations. A marker is displayed at each violation spot.

- Choose *Floorplan - Automatic Floorplan - Check Floorplan Space Rule*



Check Floorplan Space - Fields and Options

Check Space Rule	Reads spacing rules for the constraints file and checks the current floorplan. *Default:* On	
	Constraint File	Specifies the file that contains the spacing rules.
	Report File	Writes the spacing rule violation information to the specified file.
Clear Violation Markers	Clears all space violation markers. *Default:* Off	

Related Text Commands

- `checkFPlanSpace`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Resize Floorplan

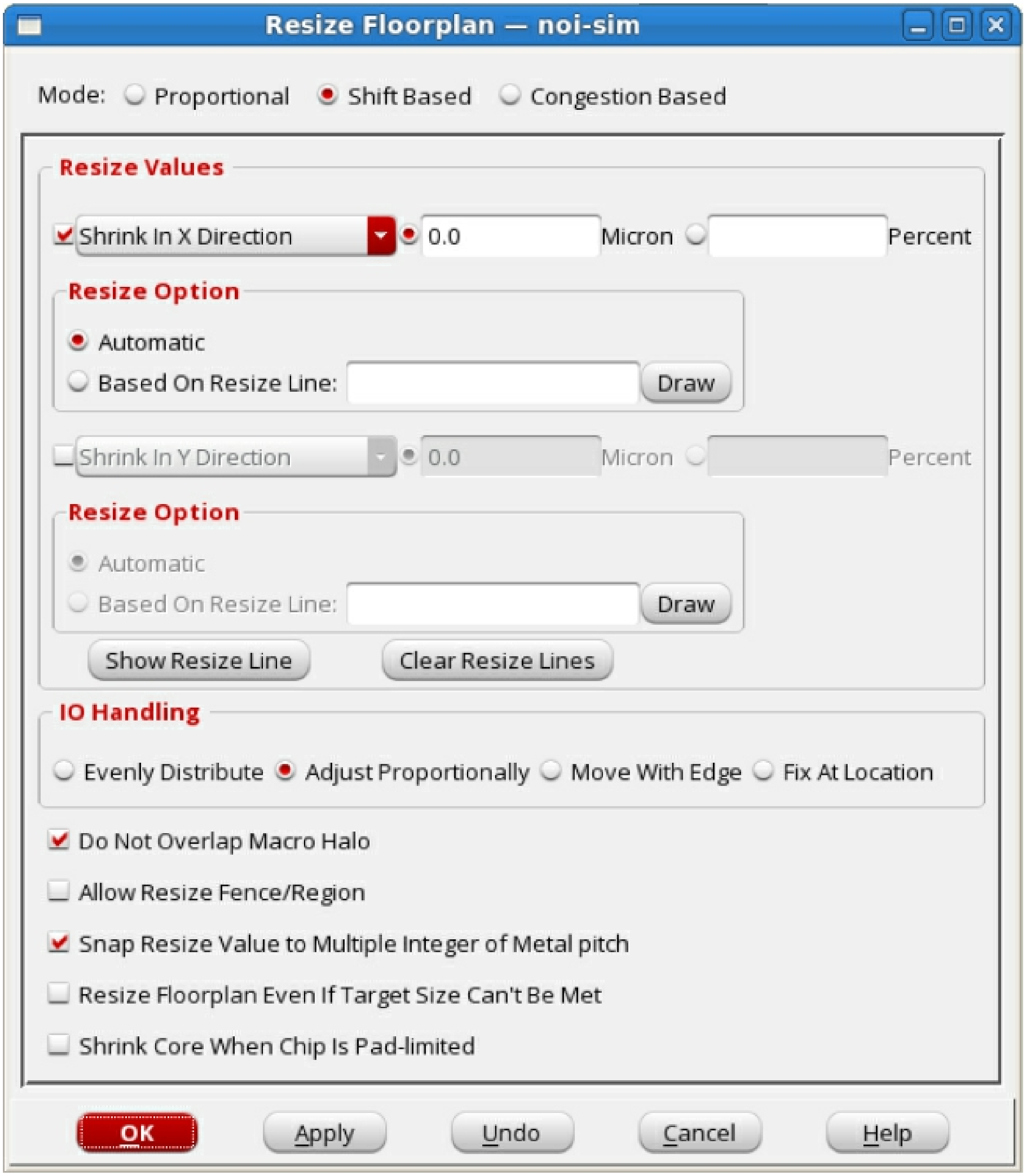
Use this form to resize the floorplan while maintaining the relative locations of the existing floorplan. You can resize the space among floorplan objects in the three ways:

- Proportional Spacing
  Distributes the space among floorplan objects proportionally. It can shrink or expand the space in both, X and/or Y directions. However, you cannot adjust pre-routed wires using proportional spacing.
- Shift Based Spacing
  Shifts floorplan objects at the right/upper(x/y resize) side of resize line and keeps the location of the rest of floorplan objects.
- Congestion Based Spacing
  Resizes and shifts the floorplan objects by estimating the congestion for the floorplan and automatically deciding where to draw a resize line to avoid the congested area.

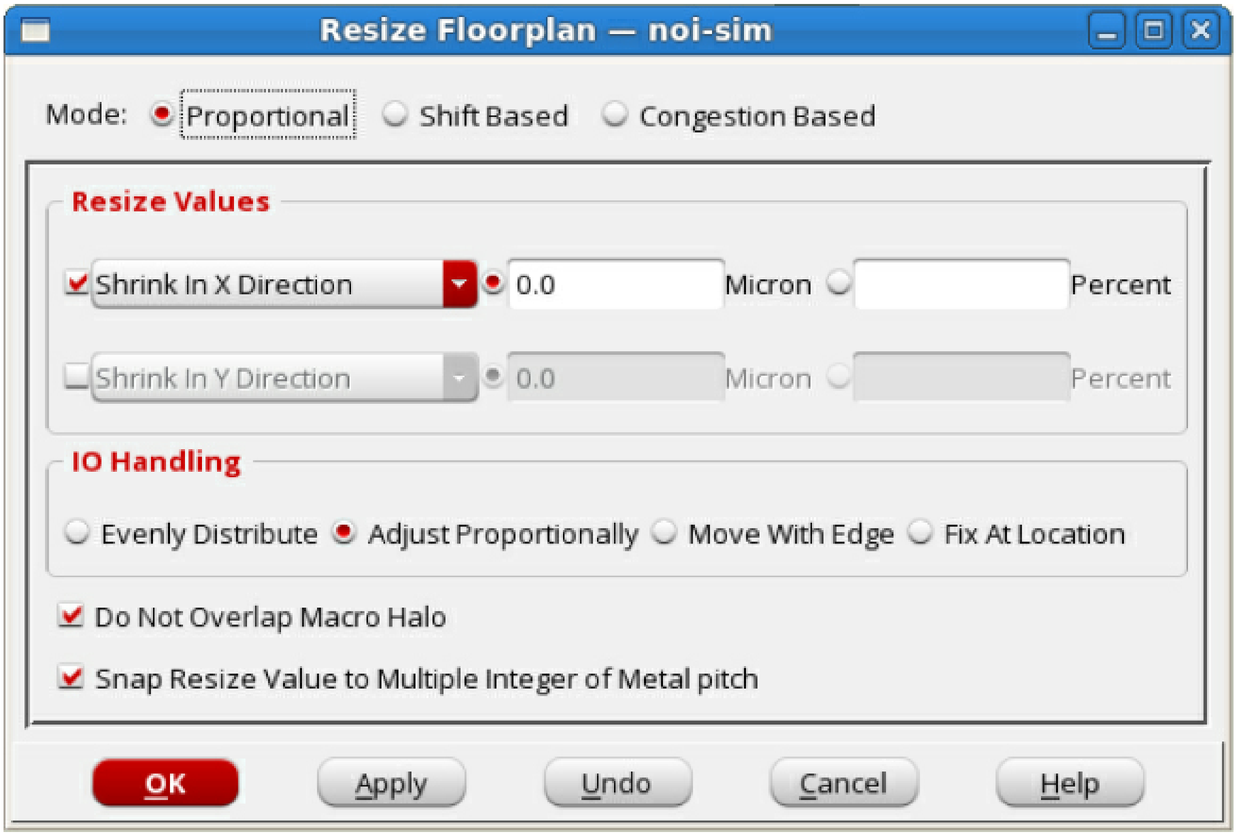
The resize values can be snapped to the multiple integer of the metal layer pitch. You can adjust the space between the I/Os proportionally, by selecting *Adjust Proportionally* in the Resize Floorplan form. Resize floorplan treats the overlapping I/O pads as single entities that can be moved together when resizing the floorplan.

Resize floorplan preserves any offset that exists between the I/O pads and the design boundary.

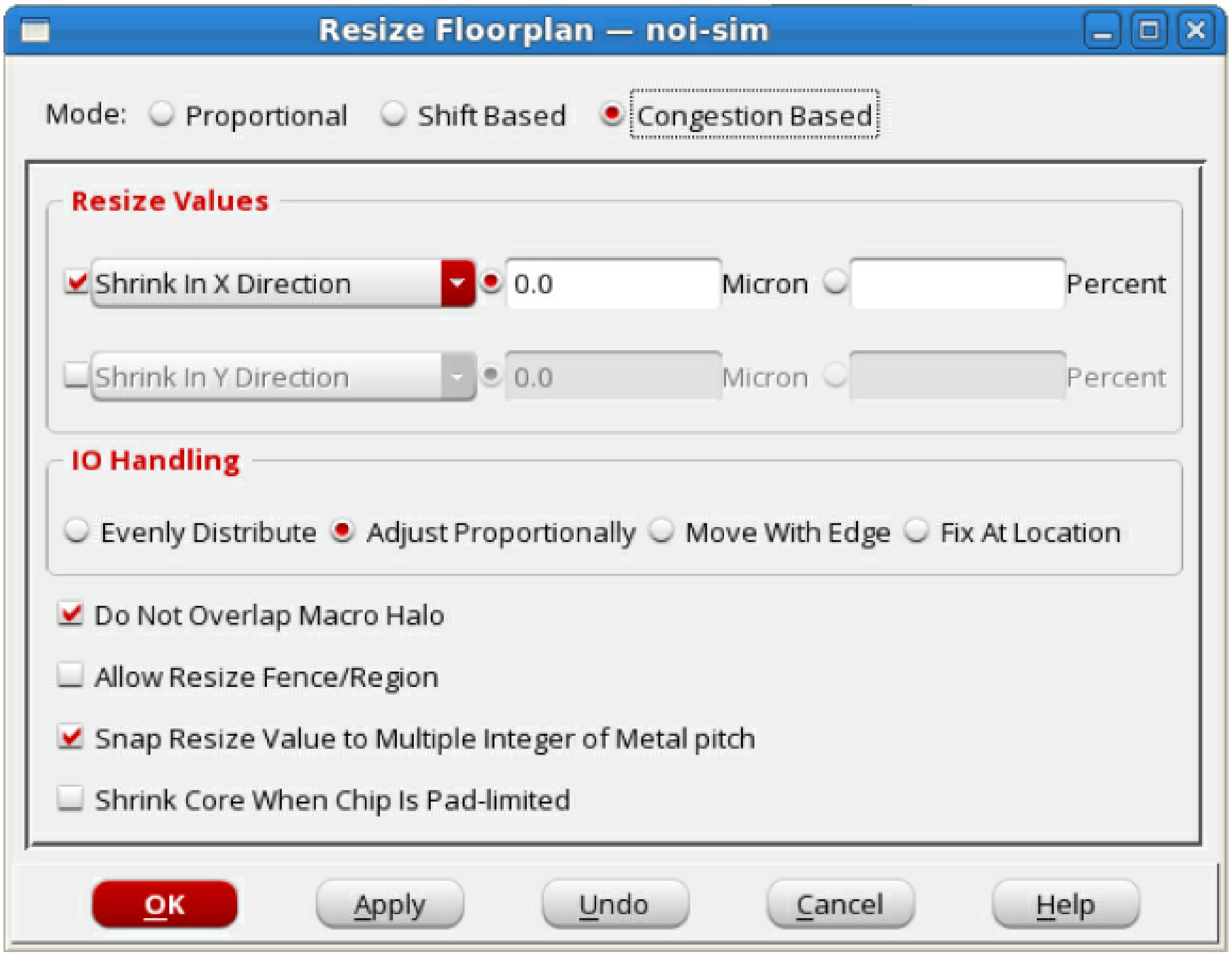
Choose *Floorplan - Resize Floorplan*. By default, the *Shift Based* mode is selected.



To select the Proportional mode, click the *Proportional* option.



To select the congestion-based mode, click the *Congestion Based* option.



Resize Floorplan - Fields and Options

Mode	Select one of the following options:	
	Proportional	Resizes the space among floorplan objects proportionally
	Shift Based	Shifts floorplan objects at the right/upper(x/y resize) side of resize line and keeps the location of the rest of floorplan objects.
	Congestion Based	Resizes and shifts the floorplan objects by estimating the congestion for the floorplan and automatically deciding where to draw a resize line to avoid the congested area.
Resize Values		

	Specifies the resize direction and the resize value in microns or percentage. In the dropdown box on the top, you can select one of the four resize directions: • *Shrink in X Direction* • *Expand in X Direction* • *Shrink in Y Direction* • *Expand in Y Direction* If you select resize in one direction from the dropdown menu on the top, the other direction is available in the dropdown menu on the bottom. For example, if you select *Shrink in X Direction* or *Expand in X Direction* in the dropdown box on the top, the following options are available in the dropdown menu on the bottom: • *Shrink in Y Direction* • *Expand in Y Direction* The floorplan will be resized first in the direction specified in the top dropdown menu, and then in the direction specified in the bottom dropdown menu. The resize value specifies how much the floorplan will be resized in the x and/or y directions. The value can be specified in *Micron* or *Percent* fields.	
Resize Option		
	Specifies whether the floorplan will be resized automatically or based on the specified resize lines.	
	Automatic	Specifies that the floorplan will be resized automatically. If you select this option, the resize lines are derived automatically based on the current floorplan and the specified resize values.

	Based On Resize Line	Specifies that the floorplan will be resized based on resize lines. Resize lines control the areas of floorplan that will be expanded or shrunk. You can specify coordinates for resize lines, or you can use the *Draw* button to draw resize lines in the floorplan area. You can specify resize lines using (x1 y1) (x2 y2)...(xn yn) coordinates. Each resize line can have multiple segments (for example, horizontal, vertical, and again horizontal) but it can only be applied to one direction. If you want to shrink or expand the floorplan in both directions, specify resize lines for each direction.
	Draw	Click the *Draw* button to draw resize lines in the floorplan area. To resize the floorplan in the x direction, draw vertical lines. To resize the floorplan in the y direction, draw horizontal lines. To complete a line, press the ESC key. You can draw multiple lines by dragging and clicking the left mouse button.
Show Resize Line		
	Displays the current resize line. If you update the values of the coordinates in the *Based on Resize Lines* field, you can click the *Show Resize Lines* button to update the display of the resize lines in the GUI.	
Clear Resize Line		
	Clears the current resize line. **Note:** The resize lines are automatically cleared when the floorplan is resized.	
IO Handling		
	Specifies how I/Os are handled during floorplan resize.	
	Evenly Distribute	Distributes I/Os evenly.

	Adjust Proportionally	Resizes the space among I/Os proportionally. **Note:** The overlapping I/Os are also spaced proportionally when you choose this option. By default, the overlapping I/Os are spaced proportionally. However, the relative placement order of the I/Os and the side constraints remain unchanged.
	Move With Edge	Moves pins on the moved edge orthogonally to edge direction so pins stay on edge after movement. The pins on other edges are not touched.
	Fix at Location	Fixes I/Os at current location.
Do Not Overlap Macro Halo		
	Honors placement halo and preserves the space between macros held by halo after the floorplan resize. With this option on, if the original placement halo does not overlap with other macros or placement halo, after resize floorplan, it will not overlap with other macros or placement halo.	
Allow Resize Fence Region		
	Enables resized lines to go through fences and regions in floorplan. With this option fences, regions, and guides are automatically resized inside the floorplan while maintaining their minimum size after the shrink.	
Snap Resize Value to Multiple Integer of Metal Pitch		
	Snaps resize values (shrink/expand) of the floorplan to a multiple integer of the metal layer pitch. For example, if the horizontal metal pitch is 1.568 microns and you want to shrink the floorplan by 8 microns in y direction, the actual shrink value is 7.84 microns, the nearest multiple integer of the metal pitch. The x direction resize value snaps to the first vertical layer pitch and the y direction resize value snaps to the first horizontal layer pitch.	
Resize Floorplan Even if Target Size Cannot be Met		
	Resizes the floorplan even if the target size can not be met. However, the floorplan is resized as near as possible to the specified size.	

Shrink Core When Chip Is Pad-Limited	
	Shrinks the core when the chip is pad-limited.

Related Text Commands

- `setResizeFPlanMode`
- `setResizeLine`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Relative Floorplan

You can capture and define the placement relationship of floorplan objects independently from the actual coordinates in a floorplan. You can also resize a module or blackbox based on other floorplan objects. You can also:

- Automatically generate constraints.
- Edit and save the constraints for floorplan objects.
- Place macros in an array

The Relative Floorplan menu contains the following submenus:

- Edit Constraint
- Define Array Constraints
- Save Constraint

Edit Constraint

The Edit Constraint menu command opens the Relative Floorplan form, which contains the following pages:

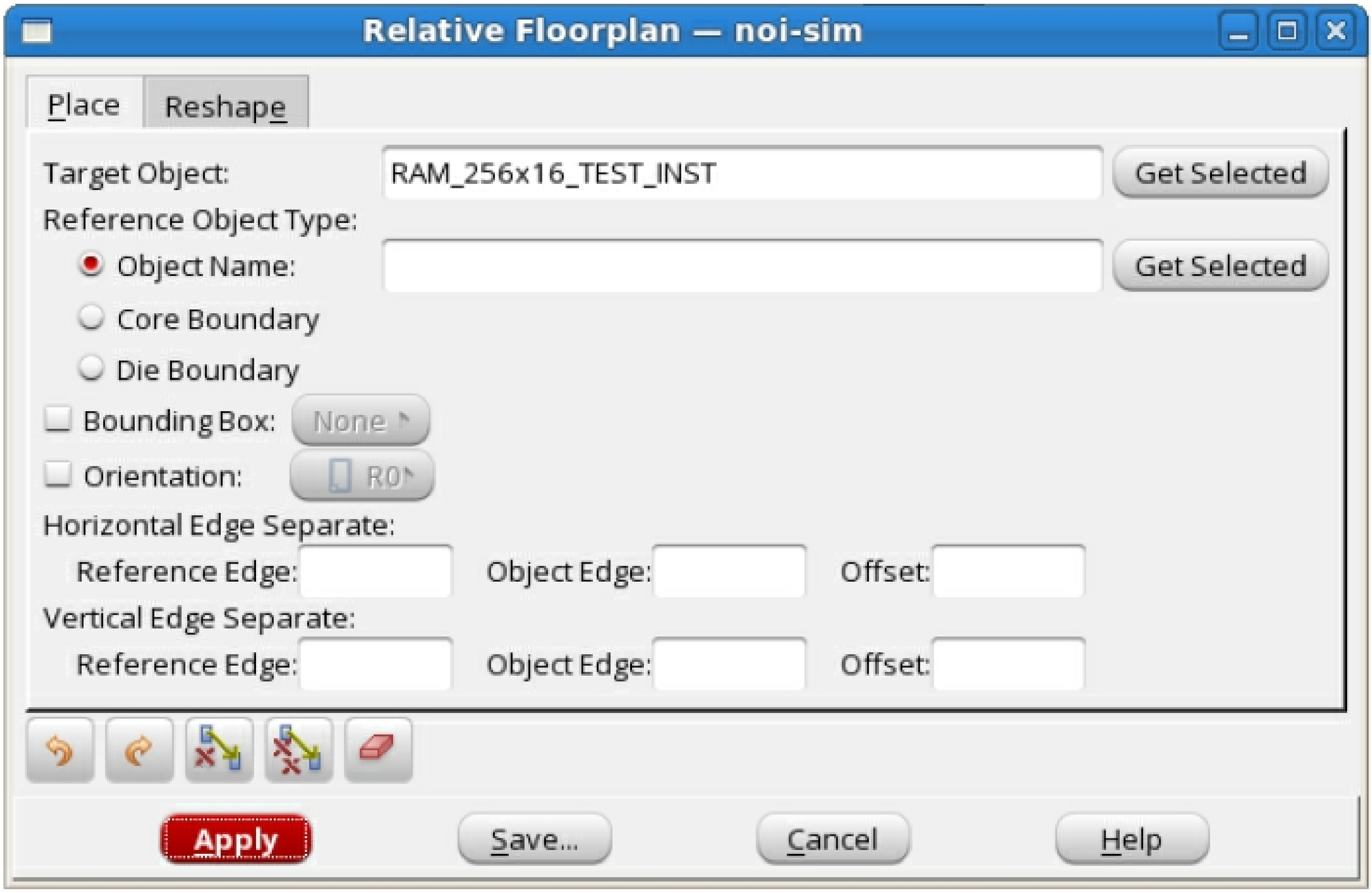
- Relative Floorplan - Place
- Relative Floorplan - Reshape

Tip: You can access the *Relative Floorplan* form from a context menu (that appears when you click the middle mouse button) of any object that has relative floorplan constraints.

Relative Floorplan - Place

Use the *Place* page of the Relative Floorplan form to place specific instances relative to other floorplan objects.

- Choose *Floorplan* - *Relative Floorplan* - *Edit Constraint* and then click *Place*.



Relative Floorplan - Place Fields and Options

Target Object	Specifies the target object to place. It can be hInst, inst, group, power_domain, pin_guide, blockages, or port.	
Reference Object Type	Specifies the type of the reference object.	
	Object Name	Specifies the name of the placed instance. You can retrieve the name of the instance currently selected in the design display area by clicking *get selected*.
	Core Boundary	Specified that the object is placed with respect to the core boundary.

	Die Boundary	Specified that the object is placed with respect to the die boundary.
Bounding Box	Specifies whether to use a bounding box instead of the rectilinear shape of target or reference object. You can choose none, target, reference, or both.	
Orientation	Specifies the orientation of the target object. The orientation can be: R0 R90 R180 R270 MX MY MX90 MY90. For a definition of the orientation symbols, see the Orientation Key table in the "Floorplanning the Design" chapter of the *Innovus User Guide*.	
Horizontal Edge Separate	Specifies the vertical spacing between the horizontal edge of the target and reference objects.	
	Reference Edge	Specifies the reference object edge.
	Object Edge	Specifies the target object edge.
	Offset	Specifies the offset value from the reference object in the specified dimension.
Vertical Edge Separate	Specifies the horizontal spacing between the vertical edge of the target and reference objects.	
	Reference Edge	Specifies the reference object edge.
	Object Edge	Specifies the target object edge.
	Offset	Specifies the offset value from the reference object in the specified dimension.
Undo	Click to reverse the previous action	
Redo	Click to restore the design to the same state as before you clicked the *Undo*	

Delete Target Object	Click to delete the target object.
Delete all	Click to delete all relative floorplan constraints.
Clear Input	Click to clear any existing text in the input box.

Tip: To save all the Relative Floorplan commands that were executed during a session, click *Save*. This saves a script that can be used later for updating or adjusting an existing floorplan based on the new blocks' size and position.

Tip: To modify multiple relative constraints associated with the object, click *Next*. This loads the next relative constraint for editing.

Related Text Commands

- `delete_relative_floorplan`
- `create_relative_floorplan`

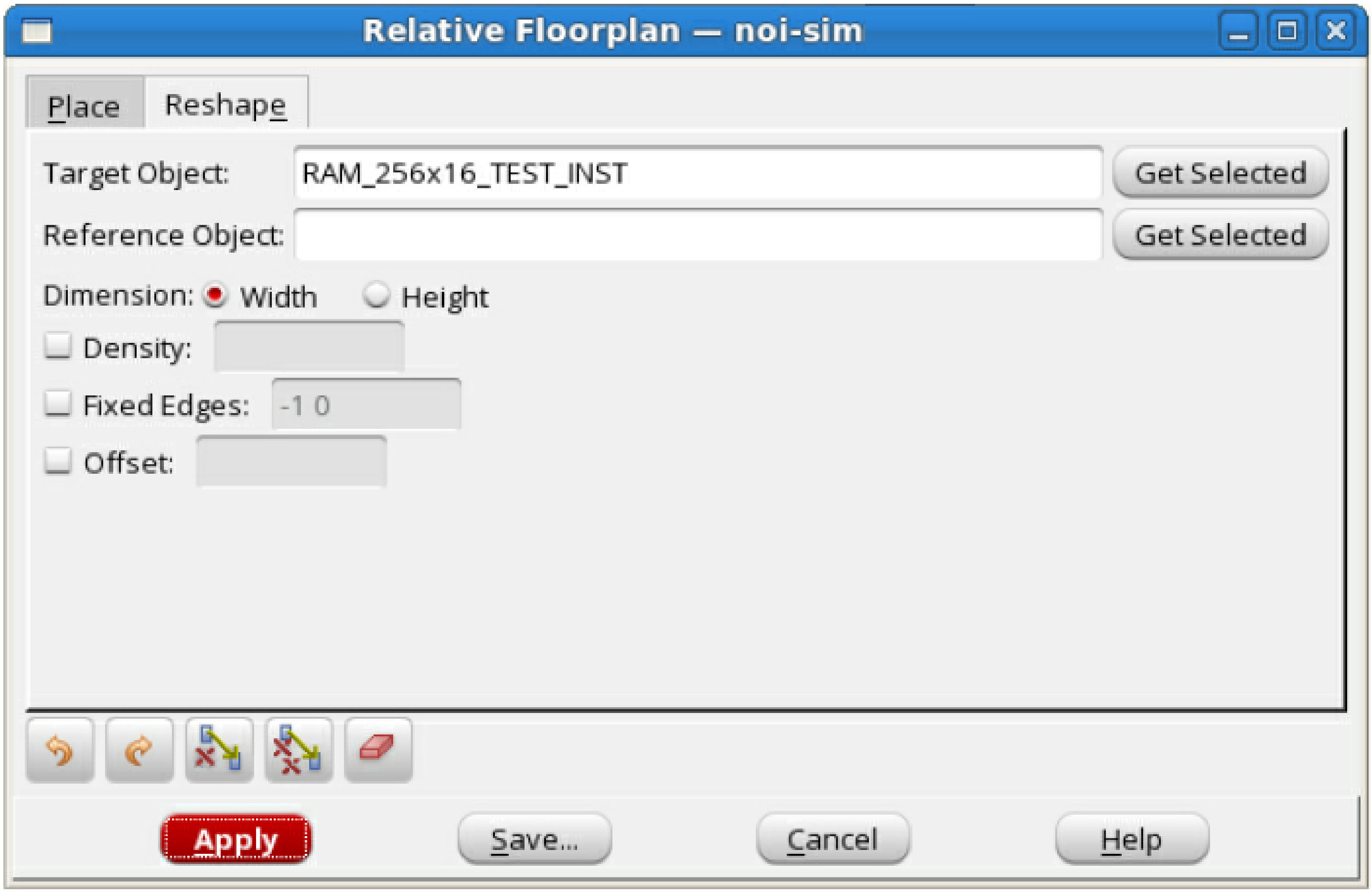
Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Relative Floorplan - Reshape

Use the *Reshape* page of the Relative Floorplan form to reshape specific instances.

- Choose *Floorplan - Relative Floorplan - Edit Constraint* and then click *Reshape*.


Relative Floorplan — noi-sim
Place
Reshape
Target Object:
RAM_256x16_TEST_INST
Get Selected
Reference Object:
Get Selected
Dimension:
Width
Height
Density:
Fixed Edges:
-1 0
Offset:
Apply
Save...
Cancel
Help

Relative Floorplan - Reshape Fields and Options

Target Object	Specifies the target object to reshape. It can be hInst,group, power_domain, pin_guide, or blockages. You can retrieve the instance currently selected in the design display area by clicking *get selected*.
Reference Object	Specifies the reference object for reshaping. You can retrieve the name of the instance currently selected in the design display area by clicking *get selected*.
Width	Specifies the width of the referenced object as the reference dimension.
Height	Specifies the height of the referenced object as the reference dimension.
Density	Specifies the target utilization (TU). By default, reshaping the object will keep the current TU.
Fixed Edges	Specifies that the reshape object will be stretched while fixing two perpendicular edges. *Default*: `-1 0`
Offset	Specifies the offset value from the reference object in the specified dimension.

Tip: To save all the Relative Floorplan commands that were executed during a session, click *Save*. This saves a script that can be used later for updating or adjusting an existing floorplan based on the new blocks' size and position.

Related Text Commands

- `delete_relative_floorplan`
- `create_relative_floorplan`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.

- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Define Array Constraint

Use the *Define Array Constraints* form to easily place macros in a matrix. You can use the Define Array Constraints form to place macros in a matrix aligned to a region, guide, or boundary.

- Select the macros that you want to display in an array. Choose *Floorplan* - *Relative Floorplan* and click *Define Array Constraint.*

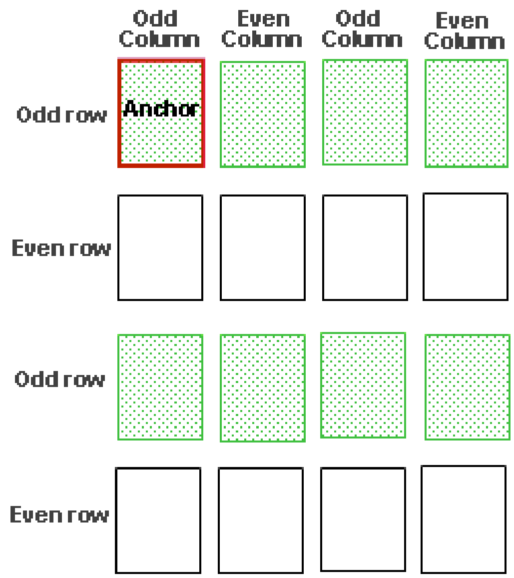
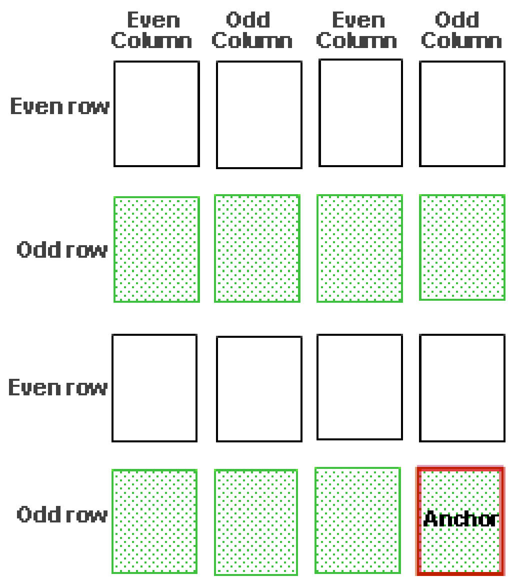
Define Array Constraint Fields and Options

Instance List	Displays the macros that will be placed in the array. The topmost macro in the list is considered as the reference object.
Up	Moves the selected macro up in the Instance List.

Down	Moves the selected macro down in the Instance List.
Swap	Swaps two selected macros.
Reverse	Reverses the order of the macros in the Instance List.
Sort	Sorts the macros, by name, in the Instance List
Clear Constraints	Clears the array constraints, specified for macros, from the Instance List.
Load Selected	If any macros are selected in the main GUI window, includes them in the Instance List **Note:** Any macros that are not selected in the main GUI window are removed from the Instance List.
Add Selected	If any macros are selected in the main GUI window, adds them to the Instance List. Other macros in the Instance List are also retained.
Delete	Removes the selected macros from the Instance List. **Note:** Removes those macros that are selected in the Instance List. This does not remove the macros selected in the main GUI window.
DeleteAll	Removes all macros from the Instance List
Undo	Undo the last operation performed on the Instance List.
Highlight	Specifies that the macros selected in the Instance List should be highlighted in the main GUI window.
Array Mode	Select one of the modes for the array:

	• *Vertical:* Specifies that the macros should be placed in a column. • *Horizontal*: Specifies that the macros should be placed in a row. • *Matrix*: Specifies that the macros should be placed in a matrix. • *row*: For the *Matrix* option, specifies the number of rows in the matrix • *col*: For the *Matrix* option, specifies the number of columns in the matrix • *Align XY*: For the *Matrix* option, specifies that the objects should be aligned to the maximum height and width. • *Horizontal:* For the *Matrix* option, specifies that the macros should be placed in a horizontal direction first and then in the vertical directions. That is, the macros will be placed row-wise. • *Vertical:* For the *Matrix* option, specifies that the macros should be placed in a vertical direction first and then in the horizontal direction. That is, the macros will be placed column-wise.
Anchor Point	Choose one of the following as the anchor point. This is the corner in which the anchor object (the first macro in the Instance List) will be placed, relative to the other macros. • *Top Left:* The anchor object is placed at the top left corner relative to the other macros. • *Top Right:* The anchor object is placed at the top right corner relative to the other macros. • *Bottom Left:* The anchor object is placed at the bottom left corner relative to the other macros. • *Bottom Right:* The anchor object is placed at the bottom right corner relative to the other macros.

Flip Control (From Anchor Object)	Specify the flip options for the rows as follows:
	• *Row*: Specify one of the following for the horizontal rows:
	  ◦ *No Flipping*: Specifies that the rows should not be flipped
	  ◦ *Flip Even Ones*: Specifies that even numbered rows should be flipped.
	  ◦ *Flip Odd Ones*: Specifies that odd numbered rows should be flipped.
	  ◦ *Flip All*: Specifies that all rows should be flipped.
	• *Column*: Specify one of the following for the vertical rows:
	  ◦ *No Flipping*: Specifies that the rows should not be flipped
	  ◦ *Flip Even Ones*: Specifies that even numbered rows should be flipped.
	  ◦ *Flip Odd Ones*: Specifies that odd numbered rows should be flipped.
	  ◦ *Flip All*: Specifies that all rows should be flipped.
	The way even/odd columns are flipped depends on the location of the anchor object. This is illustrated as follows:
	Here is the scenario with the anchor object at the top left

	 Anchor Point: Top Left Here is the scenario with the anchor object at the bottom right.  Anchor Point: Bottom Right
Rotate R90	If selected, the macros are rotated right by 90 degrees.

Anchor Object Alignment	Has the following fields

	• *Align*: The name of the anchor object is displayed in this field.
	• *To*: Specify one of the following:
	  ◦ *Current Location*: Specifies that the anchor object stays at the current location.
	  ◦ *Guide*: Specifies that the anchor object is aligned to the parent module of the macro.
	  ◦ *Core*: Specifies that the anchor object is aligned to the core boundary.
	  ◦ *Boundary*: Specifies that the anchor object is aligned to the design boundary.

Spacing	Provide the details of the spacing as follows: • *Row*: Provide the spacing between rows. • *Column*: Provide the spacing between columns. • *Unit*: Select whether the unit for spacing is microns or tracks.
Output TCL file	Provide options for the file in which the details of array constraints are stored. Specify the following: • *Name*: Name of the file. • *Append*: Specifies that the corresponding relative constraints will be appended to the specified output file. • *Auto Increment:* Specifies that the file name is incremented automatically, starting from 0, every time the changes are applied.

Related Text Commands

- `delete_relative_floorplan`
- `create_relative_floorplan`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Save Constraint

Use the Save Constraint menu command to save the floorplan constraints.

- Choose *Floorplan - Relative Floorplan - Save Constraint* and specify a file in which to save floorplan constraints.

Row

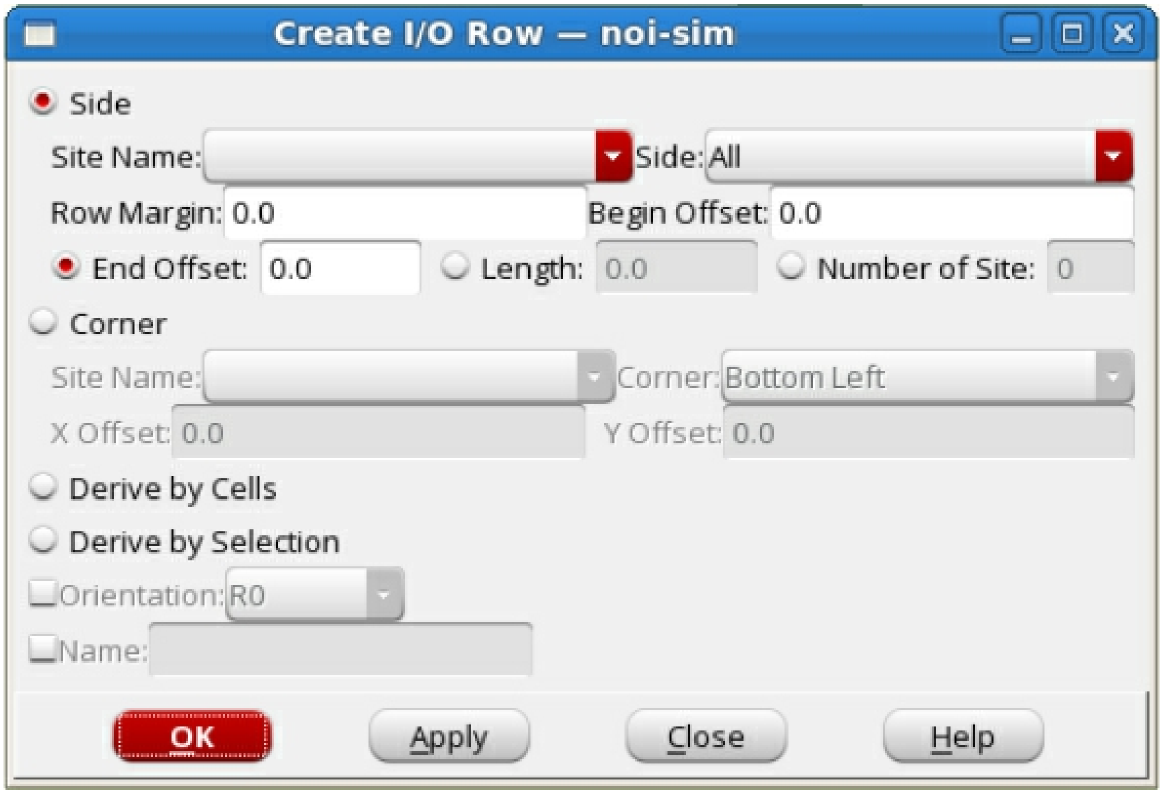
The *Row* menu provides the following forms for creating and editing I/O rows and core rows:

- Create I/O Row
- Edit I/O Ring
- Create Core Row
- Cut Core Row
- Stretch Core Row

Create I/O Row

Use the *Create I/O Row* form to create I/O rows.

- Choose *Floorplan - Row - Create I/O Row*.



Create I/O Row Fields and Options

Side	Specifies the side on which the row is to be created. If you do not specify the side, by default, one row is created on all sides (South, East, North, and West).
Site Name	Specifies the name of the site defined in the LEF library.
Row Margin	Specifies the distance, in µmeters, from the row edge to the die edge. The row edge is \`top' for a North side row, \`bottom' for a South side row, \`left' for a West side row, and \`right' for an East side row.
Begin Offset	Specifies the starting location of the I/O row from the die edge. For a horizontal row, this value is the lower `X` value. For a vertical row, this value is the lower `Y` value. *Default*: `0`, starting from the die edge.

End Offset	Specifies the end location of the I/O row from the die edge. For a horizontal row, this value is the higher `X` value. For a vertical row, this value is the higher `Y` value. *Default*: `0`, ending from the die edge.
Length	Specifies the length of the row, in µmeters, starting from the die edge or the *Begin Offset* value.
Number of Site	Specifies the number of sites to define the length of the row. **Note:** You can either specify End Offset or Length or Number of Site.
Corner	Specifies the location of the corner cell: • *Bottom Left* • *Bottom Right* • *Top Right* • *Top Left*
X Offset	Specifies the distance, in µmeters, from the left or right edge of the corner row to the die edge.
Y Offset	Specifies the distance, in µmeters, from the top or bottom edge of the corner row to the die edge.
Derive by Cells	Specifies to create I/O row for all I/O cells in the design
Derive by Selection	Specifies to creates I/O row only for selected I/O cells. When you specify this option, some I/O rows may overlap depending on the I/O cell distribution.
Name	Specifies the name of the I/O row to be created.

Orientation	Specifies the orientation of the created row. If you do not specify this parameter, the default orientation for each side starting from the row on the south side is `R0`, rotate to `R90` for the next side, and so on... as follows: • `R0` - South West • `R90` - South East • `R180` - North East • `R270` - North West The default order of orientation is South, East, North, and West.

Related Text Commands

- `createIoRow`

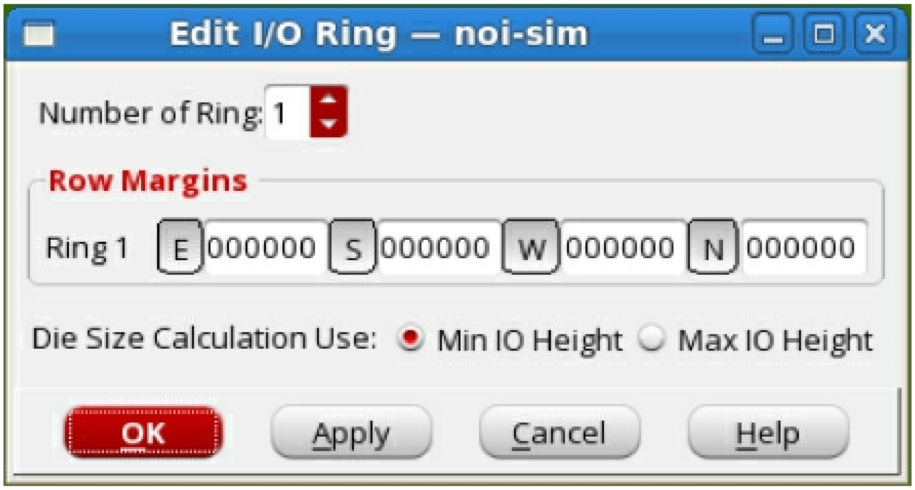
Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Edit I/O Ring

Use the Edit I/O Ring form to specify I/O pad rings and row margins. You can use this form to create symmetric or asymmetric I/O rows.

- Choose *Floorplan - Row - Edit I/O Ring*.



Edit IO Row Fields and Options

Number of Rings	Specifies the number of I/O rings needed for the placement.
Row Margins	Specifies the distance between the die boundary edge to the I/O row edge, in microns, where `E` is the East side, `S` is the South side, `W` is the West side, and `N` is the North side.
Die Size Calculation Use	Select either the minimum or maximum height that will be used to calculate the design size.

Related Text Commands

- `placePadIO`
- `saveIoFile`
- `setIoRowMargin`

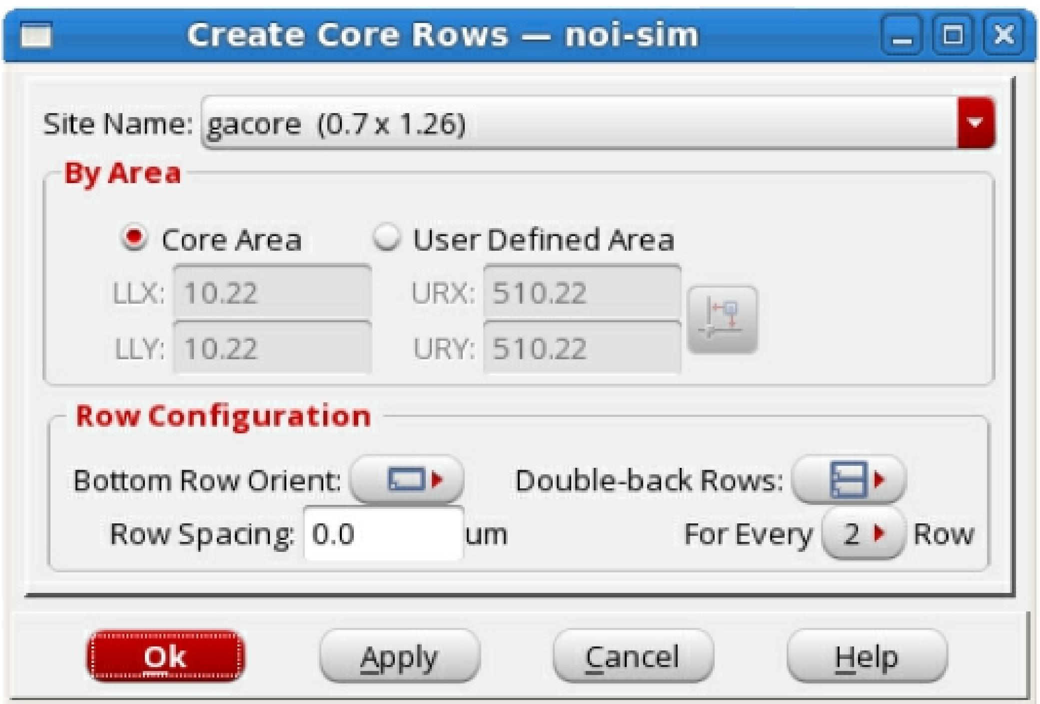
Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Create Core Row

Use the *Create Core Rows* form to create rows for the specified site, both inside and outside the core area, but within the die.

- Choose *Floorplan - Row - Create Core Row*



Create Core Rows Fields and Options

Site Name	Specifies the name of the site for which rows will be created.
Core Area	Specifies the lower-left and upper-right x and y coordinates within the core area of site for which rows will be created. The coordinates of the core area core area are selected by default.
User Defined Area	If selected, you can click the *Draw Box* button to physically draw a box in the design window corresponding to the coordinates of the area in which rows will be created.
Bottom Row Orient	Specifies whether the first row is not flipped (default) or flipped.
Double-back Rows	Specifies whether rows are created back-to-back or not.
Row Spacing For Every # Rows	
	Specifies the standard row spacing, in micrometers. This must be a positive value. By default, this value is zero. In the *For Every Row* pull-down menu, specify *1* for every row, or *2* for every other row.

Related Text Commands

- `createRow`
- `cutRow`
- `deleteRow`
- `stretchRows`

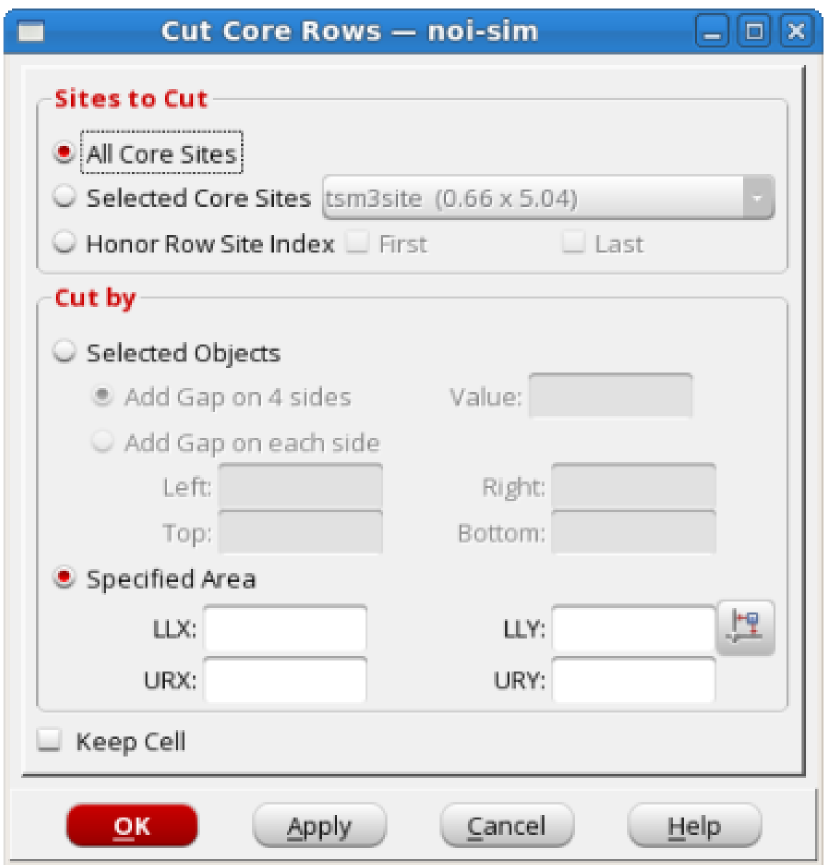
Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Cut Core Row

Use the *Cut Core Rows* form to cut site rows that intersect with the specified area or selected object(s).

- Choose *Floorplan - Row - Cut Core Row*.



Cut Core Rows Fields and Options

All Core Sites	Specifies that rows will be cut for all core sites.
Selected Core Sites	Specifies the core site for which rows will be cut.
Honor Row Site Index	Specifies that in a mixed row design, the row site index in honored in the specified area for which rows will be created. • *First*: Select to honor the first row site index. • *Last*: Select to honor the last row site index.
Selected Objects	Specifies that rows that intersect with the selected objects will be cut.
Add Gap on 4 Sides	Specifies the additional space to be provided on the left, right, top, and bottom sides of the selected objects. The same value will be used for all sides.
Add Gap on each side	Specifies the additional space to be provided on the top, bottom, left, and right sides respectively of the selected objects.
Specified Area	Specifies the lower-left and upper-right x and y coordinates within the core area of site for which rows will be created. The coordinates of the core area core area are selected by default.
Draw Box	You can click the *Draw Box* button to physically draw a box in the design window corresponding to the coordinates of the area for which rows will be cut.
Keep Cell	Specifies that all cells that are placed inside the cut row area will not be unplaced. *Default*: By default, all cells inside the target area will be unplaced.

Related Text Commands

- `createRow`

- `cutRow`
- `deleteRow`
- `stretchRows`

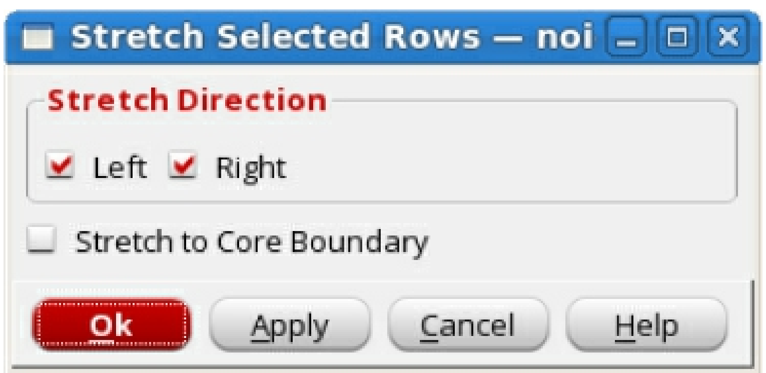
Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Stretch Core Row

Use the *Stretch Selected Rows* form to stretch selected rows.

- Choose *Floorplan - Row - Stretch Core Row*



Stretch Selected Rows Fields and Options

Left	Specifies that the left edge of all selected rows should be aligned to the left-most edge among all selected tows
Right	Specifies that the right edge of all selected rows should be aligned to the right-most edge among all selected rows
Stretch to Core Boundary	Specifies that row edges should be aligned to the core boundary.

Related Text Commands

- `createRow`
- `cutRow`
- `deleteRow`
- `stretchRows`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

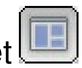
Floorplan Toolbox

The Floorplan Toolbox provides for easy access to the commonly used features during floorplanning. You can use the Floorplan toolbox to:

- Use display-related commands such as zoom, fit, and pan.
- Access the floorplanning interactive commands such as shift, align, space, rotate, and flip objects.
- Perform other functions such as swap selected objects, display/calculate effective query

utilization, and so on.

Note: You can use the Floorplan Toolbox to perform floorplan operations on objects that are outside the core box.

- Choose *Floorplan* - *Floorplan Toolbox*
- Click on the *Floorplan Toolbox* widget  in the main window.

Note: The Floorplan Toolbox is dockable and detachable. You can detach the *Toolbox* and move it around to make more space in the main window. Alternatively, you can dock the *Toolbox* back to the main window.

Toolbox Fields and Options

Shift	Displays options for shifting the floorplan objects.	
	Shift Up	Click to shift the object up.

	Shift Left	Click to shift the object towards the left side
	Shift Down	Click to shift the object down
	Shift Right	Click to shift the object towards the right side
	To Core Box	Select to shift the object towards the core box.
	To Die Box	Select to shift the object towards the die box.
	1 by 1	Select to shift all selected objects by 1 micrometer.
	Shift	Specify the shift distance value, in micrometers.
Space	Displays options for maintaining the space between floorplan objects.	
	Space From Top	Click to fix the top most object and shift all other objects vertically to the down side of the fixed object, maintaining the specified *Space*.
	Space From Center	Click maintain the center point of the selected object. It calculates the mid-point between the left most edge and right most edge of the selected objects and then spaces the blocks at the specified distance and centers them around this mid-point so that the left most edge and right most edge are at an equal distance from the mid-point.
	Space From Bottom	Click to fix the bottom most object and shift all other objects vertically to the up side of the fixed object, maintaining the specified *Space*.
	Space From Left	Click to fix the left most object and shift all other objects horizontally to the right side of the fixed object, maintaining the specified *Space*.
	Space From Middle	Click maintain the center point of the selected object. It calculates the mid-point between the top most edge and bottom most edge of the selected objects and then spaces the blocks at the specified distance and centers them around this mid-point so that the top most edge and bottom most edge are at an equal distance from the mid-point.

	Space From Right	Click to fix the right most object and shift all other objects horizontally to the left side of the fixed object, maintaining the specified *Space*.
	Space TB Dist.	Click for an even vertical distribution of the objects.
	Space LR Dist.	Click for an even horizontal distribution. of the objects.
	Space	Specify the spacing value, in micrometers.
	Honor Halo	Select to honor placement halo. The selected objects are spaced by a given value measured from the edge of the halo and not from the edge of the object.
Align	Displays options for aligning the floorplan objects.	
	Align Top	Click for horizontal top alignment of the selected object.
	Align Bottom	Click for horizontal bottom alignment of the selected object.
	Align Left	Click for vertical left alignment of the selected object.
	Align Right	Click for vertical right alignment of the selected object.
	Align Ver. Center	Click for vertical middle alignment of the selected object.
	Align Hor. Center	Click for horizontal middle alignment of the selected object.
	1st Selected	Select to make the first selected object as the reference object. The reference object highlighted in the design display area.
	Mixed Type	Select to consider all the selected objects together while aligning them.
	Align Top Left	Click to align the selected macros to the upper left corner.
	Align Top Right	Click to align the selected macros to the upper right corner

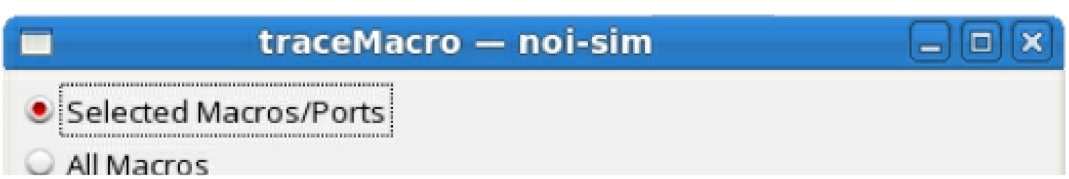
	Align Bottom Left	Click to align the selected macros to the lower left corner
	Align Bottom Right	Click to align the selected macros to the lower right corner
	X Space	Specify the spacing value between all macros when they are aligned in the X-direction. *Default*: 0 *Minimum*: 0 *Maximum*: 1000
	Y Space	Specify the spacing value between all macros when they are aligned in the Y-direction. *Default*: 0 *Minimum*: 0 *Maximum*: 1000
	Honor Halo	Select to place macros by the given value measured from the edge of the halo and not from the edge of the macro. Default is false
	Flipping Macro I/Os to Center	Click to flip the macro I/Os to the center.
	Abut Macro on Non I/O side	Click to abut macros on non I/O sides.
	Refine Macro Place	Click to legalizes the macros based on constraints such as halo and blockages, forbidden spacing, min-space, etc. **Note:** This is a limited-access feature in this release. To use this feature, contact your Cadence representative to explain your usage requirements, and make sure this feature meets your needs before deploying it widely.
	Pack Macros	**Note**: This is a beta feature.

Flip/Rotate	Displays options for flipping and rotating floorplan objects.	
	Rotate 90	Click to rotate the select object by 90 degrees.
	Rotate -90	Click to rotate the select object by -90 degrees.
	Flip X	Click to flip the selected object through X axis.
	Flip Y	Click to flip the selected object through Y axis.
	1 By1	Select to flip or rotate all the selected objects.
	Keep Relative	Select to rotate and update the relative objects automatically when the anchor objects are rotated.
Miscellaneous	Displays miscellaneous floorplan.	
	Swap Instances	Click to switches the locations of two instances.
	Define Array Constraints	Click to open the *Define Array Constraints* form.
	Preferences	Click to open the *Floorplan* page of the *Preference* form.
	Set Placement Status	Click to open the *Set Placement Status* form.

Trace Macro

Use the traceMacro form to trace the connections of specified macros, selected macros, or specified ports. You can also trace the macros based on netlist and timing.

- Choose *Floorplan - Trace Macro*.




All Ports
Macro Names:
Get Selected
Port Names:
Get Selected
Trace
Level: 1
Trace Mode:
Netlist Based
Timing Based
Output File:
Advanced...
Run
Clear All
Save All
Load...
Display
Direction: all
Highlight Traced Macro
Display Line To Ports
Through Registers
Display All Registers
Min Connection: 1
Lines
Insts
ALL
L1
L2
L3
L4
L5
L6
L7
L8
Display
Clear
Report
Output File: dtmf_recvr_core.tmcrpt
Report
Close
Bindkey...
Slack Display...
Help

Trace Macro Fields and Options

Selected Macros/Ports	Traces the selected macros or ports.	
All Macros	Traces all macros.	
All Ports	Traces all ports.	
Macro Names	Specifies the names of the macros to be traced. Alternately, click *Get Selected* to get the name of the selected macro.	
Port Name	Specifies the names of the ports to be traced. Alternately, click *Get Selected* to get the name of the selected port.	
Level	Specifies the trace level. *Maximum Level*: 10 *Minimum Level*: 1 *Default*: 1	
Trace Mode	Specifies the trace mode to use:	
	Netlist Based	Specifies that connection of the macro will be traced based on the netlist.
	Timing Based	Specifies that connection of the macro will be traced based on the timing graph.
Output File	Specifies the name of the file in which the trace macro results will be saved. *Default*: `<top_module_name>.tmcdb`	
Advanced	Click to display the *Trace Mode - Advanced* form that enables you to get the required values for the selected trace mode.	
	Register Input Pin Name	Specifies the register input pin name.
	Register Output Pin Name	Specifies the register output pin name.

	Macro Pin Name Patterns	Specifies the macro pin name patterns.
	Max Fanin/Fanout	Specifies the maximum fanin/fanout number for a pin. While tracing the connectivity, a pin will be ignored if its fanin/fanout number is larger than the specified number.
Run	Traces the macro/port connections.	
Clear All	Clears the traces.	
Save All	Saves the selected the trace macro settings.	
Load	Displays the *Load Trace File* form that enabkes you to loads saved trace macro results from a file.	
Direction	Specify the pin direction of objects to be displayed. The direction can be all, in, or out.	
Highlight Traced Macro	Specifies that the traced macro will be highlighted.	
Display Line to Ports	Displays paths from/to primary ports.	
Through Registers	Displays flightlines going through registers.	
Display All Registers	Displays all registers found during the analysis.	
Min Connection	Specify the trace minimum connection. *Default*: 1	
Lines	Controls the visibility of the trace line.	
Insts	Controls the visibility of the instances on the trace line	
Display	Display the connections of specified macros, selected macros, or specified ports.	
Clear	Clears display trace macros	

Output File	Specifies the name of the file in which the trace macro results will be saved. *Default*: <top_module_name>.tmcdb
Report	Reports the connections of specified macros, selected macros, or specified ports.
Close	Closes the form without applying any changes.
Bind Key	Displays the *TraceMacro Bind Key* form that enables you use to edit or add binding keys for the Trace Macro capability. For more information, see Binding Key.
Slack Display	Displays the *Macro Slack Timing Analysis* form

Related Text Commands

- `trace_obj_connectivity`

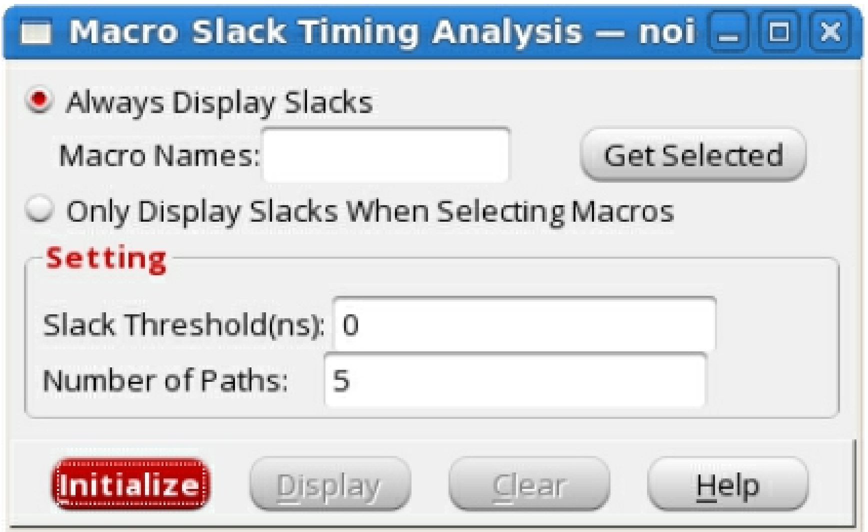
Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Macro Timing Slack Analysis

Use the *Macro Slack Timing Analysis* form to display the timing slack for macros.

- Choose *Floorplan - Macro Timing Slack Analysis*.



Macro Slack Timing Analysis Fields and Options

Always Display Slacks	Displays the timing slack for all macros.
Macro Names	Specifies the macros for which the timing slack is displayed.
Get Selected	Displays the timing slack of selected macros.
Only Displays Slacks When Selecting Macros	Displays the slack only when the macros are selected.
Slack Threshold (ns)	Specifies the threshold value. Only the patch with slack equal to or less than the specified threshold are checked.
Number of Paths	Specifies the number of paths to display for each macro.

Edit Floorplan

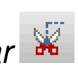
The *Edit Floorplan* submenu provides access to the following features:

- Cut Rectilinear
- Create Size Blockage

- Create Placement Blockage
- Create Routing Blockage
- Create Pin Blockage
- Align
- Shift
- Space
- Flip/Rotate
- Edit Halo
- Edit Routing Blockage
- Color Module
- Legalize Floorplan
- Set Instance Placement Status

Cut Rectilinear

Select Floorplan - Edit Floorplan - Cut Rectilinear and drag the mouse over a module or partition to create a rectilinear area.

You can also create a rectilinear area with the *Cut Rectilinear*  icon in the toolbox.

Create Size Blockage

Select *Floorplan - Edit Floorplan - Create Size Blockage* and drag the mouse over an area in the design to create a size blockage.

You can also create size blockages with the *Create Size Blockage*  icon in the toolbox.

Related Text Commands

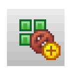
- addSizeBlockage

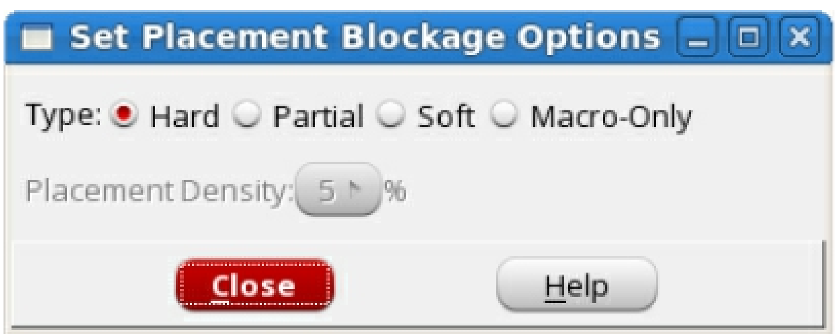
Create Placement Blockage

Use the *Create Placement Blockage* menu command to create all types of placement blockages--*Hard*, *Partial*, *Soft,* and *Macro Only* using the *Set Placement Blockage Options* form.

Specify blockage preferences in this form and then drag-and-drop the cursor in the design area to create the placement blockage.

To open the *Set Placement Blockage Options* form:

- Choose *Floorplan - Edit Floorplan - Create Placement Blockage*.
    - Or
- Click the *Create Placement Blockage*  icon in the toolbox and then press the `F3` key.



Set Placement Blockage Options - Fields and Options

Type	Specifies the placement blockage types. You can select one of the following: • *Hard* - The area cannot be used to place blocks or cells. This is the default. • *Partial* - Sets a percentage of the area that is available for placement. Use the *Placement Density* pull-down menu to select a percentage. • *Soft* - The area cannot be used to place blocks or cells during standard cell placement, but can be used during in-place optimization, clock tree synthesis, or ECO placement or placement legalization. Use the *Placement Density* pull-down menu to select a percentage for soft placement. • *Macro-Only* - Enables `planDesign` to keep macros out of the placement blockage; however, it enables standard cells to be placed inside the box as if no blockage is present. Macro-Only blockage is represented as "0" percent partial blockage in floorplan file, DEF file, and in Innovus DB.
Placement Density	Select a percentage density for partial or soft placement blockages. For example, a partial placement percentage of 75 percent means that up to 75 percent of placement density is allowed in the area.

Related Text Commands

- `createPlaceBlockage`

Related Topics

- Attribute Editor in the "Edit Menu" chapter of the *Innovus Menu Reference*
- Guiding Placement With Blockages in "Placing the Design" chapter in the *Innovus User Guide*.

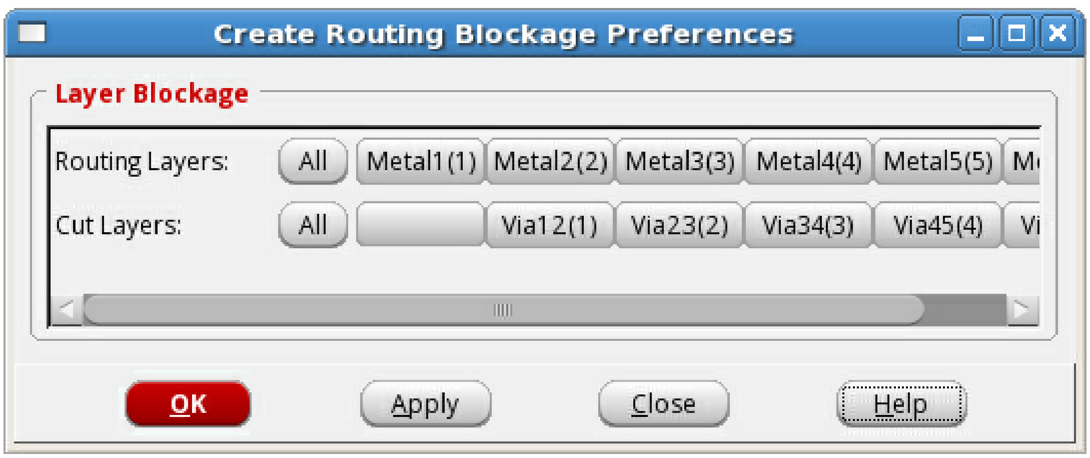
Create Routing Blockage

The Create Routing Blockage menu command can be used to create a routing blockage object that can be moved even outside the core area. The object area prevents routing of specified metal layers, signal routes, and hierarchical instances in the specified area. You can use the *Create Routing Blockage Preferences* form to specify blockage preferences and then drag the mouse to create a routing blockage on a specified metal layer.

To open the *Create Routing Blockage Preferences* form:

- Choose *Floorplan - Edit Floorplan - Create Routing Blockage* and then press the `F3` key.
    - Or
- Click the *Create Routing Blockage*  icon in the toolbox and then press the `F3` key.

Note: To change or specify more than one layer, double-click the routing blockage to open the Attribute Editor.



Create Routing Blockage Preferences - Fields and Options

Routing Layers	Select the layer, list of layers, or all layers on which the routing blockage is to be applied.
Cut Layers	Select the cut layer, list of cut layers, or all cut layers on which the routing blockage is to be applied.

Related Text Commands

- createRouteBlk

Create Pin Blockage

Select *Floorplan - Edit Floorplan - Create Pin Blockage* and drag the mouse over a partition to block the area from creating pins on specific metal layers.

You can also create pin blockages with the *Create Pin Blockage*  icon in the toolbox.

Note: To change or specify more than one layer, double-click the pin blockage to open the Attribute Editor.

Related Text Commands

- createPinBlkg

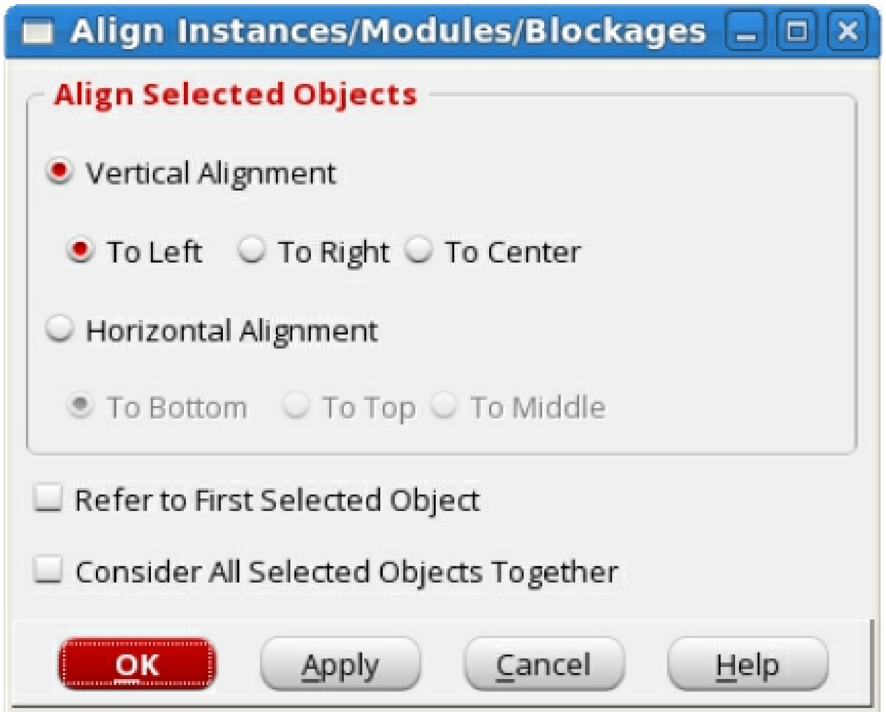
Related Topics

- Setting Pin Constraints in "Partitioning the Design" chapter in the *Innovus User Guide*.

Align

The *Align* menu item is used to access the *Align Instances/Modules/Blockages* form that enables you to align objects vertically or horizontally.

- Highlight object(s) in the design display area and choose *Floorplan - Edit Floorplan - Align*.



Alternatively, you can click the middle mouse button to bring up a context sensitive pop-up menu to select the *Align* commands.

Note: To undo the previous action, use the *Undo* widget or `U` bindkey. To restore the design to the same state as before the undo, use the *Redo* widget or `R` bindkey.

Align Instances/Modules/Blockages Fields and Options

Vertical Alignment	Specifies the selected vertical object alignment. Choose either *To Left*, *To Right*, or *To Center*.
Horizontal Alignment	Specifies the selected horizontal object alignment. Choose either *To Bottom*, *To Top*, or *To Middle*.
Refer to First Selected Object	
	Specifies a reference object highlighted in the design display area. If you specify this option, the first selected object is the reference object.
Consider All Selected Objects Together	
	Considers all the selected objects together while aligning them.

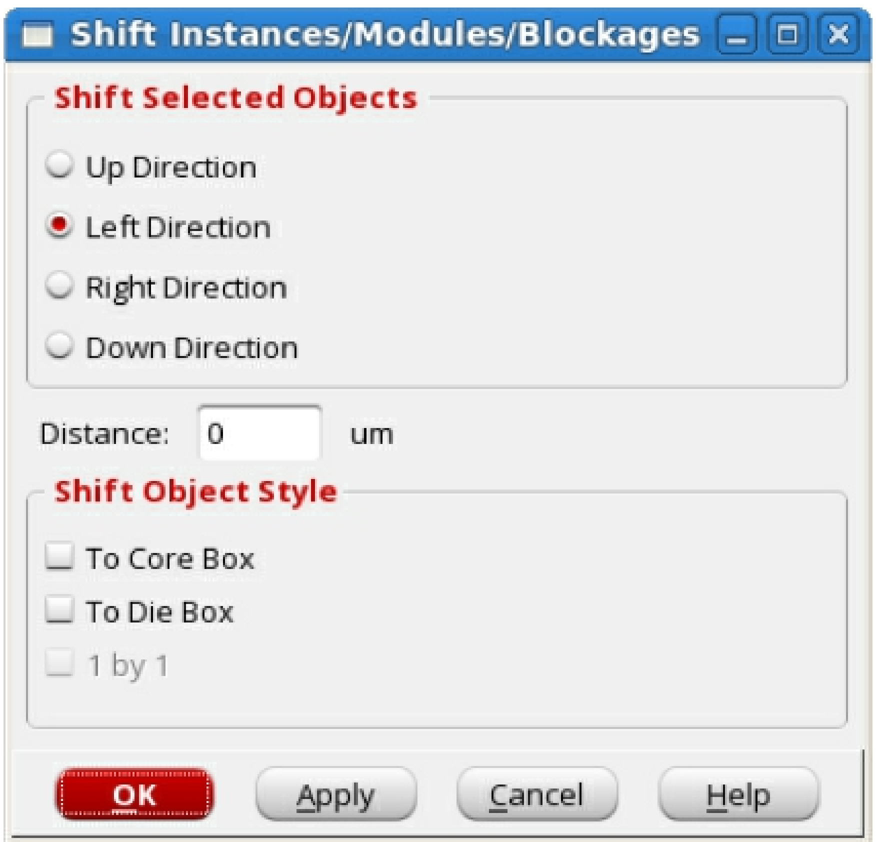
Related Text Commands

- `alignObject`

Shift

The *Shift* menu item is used to access the *Shift Instances/Modules/Blockages* form that enables you to shift objects vertically or horizontally by a specified distance value.

- Highlight object(s) in the design display area and choose *Floorplan - Edit Floorplan - Shift*.



Note: To undo the previous action, use the *Undo* widget or `U` bindkey. To restore the design to the same state as before the undo, use the *Redo* widget or `R` bindkey.

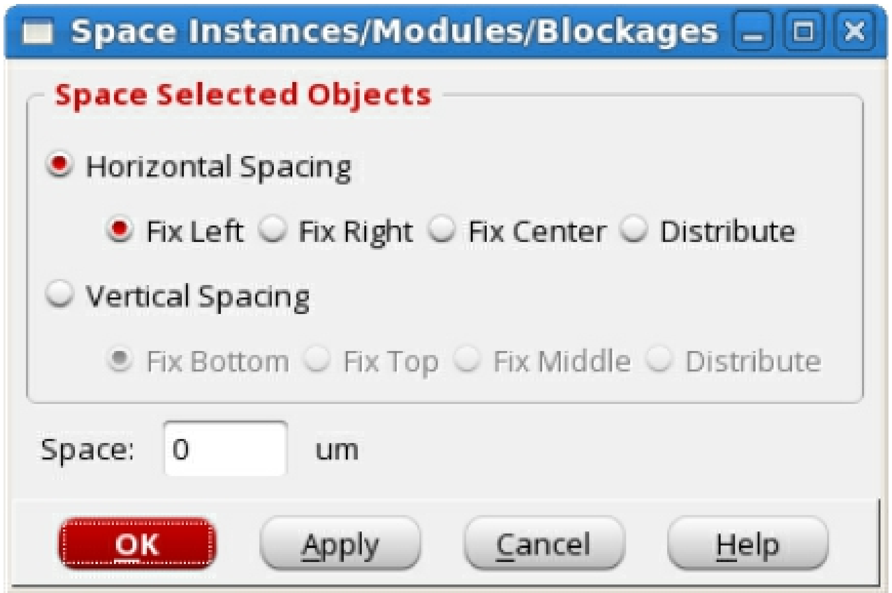
Shift Instances/Modules Fields and Options

Up Direction	Shifts the selected object(s) upward.
Left Direction	Shifts the selected object(s) to the left.
Right Direction	Shifts the selected object(s) to the right.
Down Direction	Shifts the selected object(s) downward.
Distance	Specifies the distance value, in micrometers.
To Border	Shifts the object(s) towards the border
Shift 1 by 1	Shifts each of the selected object one by one.

Space

The *Space* menu item is used to access the *Space Instances/Modules/Blockages* form that enables you to space objects horizontally or vertically by a specified distance value. You can also evenly distribute the spacing horizontally or vertically between three or more objects.

- Highlight object(s) in the design display area and choose *Floorplan* - *Edit Floorplan* - *Space*.



Note: To undo the previous action, use the *Undo* widget or `U` bindkey. To restore the design to the same state as before the undo, use the *Redo* widget or `R` bindkey.

Space Instances/Modules/Blockages Fields and Options

Horizontal Spacing	Specifies the selected horizontal object spacing. Choose either *Fix Left*, *Fix Right*, *Fix Center*, or *Distribute*.
Vertical Spacing	Specifies the selected vertical object spacing. Choose either *Fix Bottom*, *Fix Top*, *Fix Middle*, or *Distribute*.
Space	Specifies the spacing value, in micrometers.

Related Text Commands

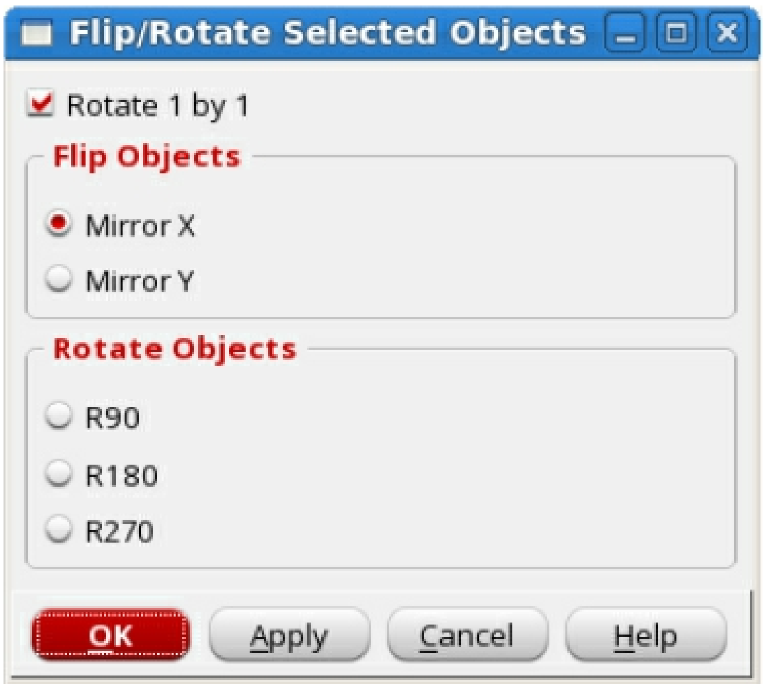
- `spaceObject`

Flip/Rotate

The *Flip/Rotate* menu item is used to access the *Flip/Rotate Selected Objects* form that enables you to flip or rotate selected objects, including wires and vias. If a wire or via is selected when the Flip/Rotate form is used, the tool internally calls the `editRotate` command. If you try to rotate an instance and wire/via at the same time, the tool gives a warning.

To flip or rotate object(s):

- Select the object(s) in the design display area and choose *Floorplan* - *Edit Floorplan* - *Flip/Rotate*.



Alternatively, right-click the mouse to bring up the context menu and use the Flip (*Flip Horizontal* and *Flip Vertically*) and Rotate (*Rotate Left 90* and *Rotate Right 90*) commands. Another alternative is to open the Attribute Editor form by double-clicking on the block, and selecting the new orientation (default orientation is R0).

Notes: To undo the previous action, use the *Undo* widget or `U` bindkey. To restore the design to the same state as before the undo, use the *Redo* widget or `R` bindkey.

Flip/Rotate Selected Objects Fields and Options

Rotate 1 by 1	Rotates each of the selected objects one by one.
Mirror X	Flips the selected object(s) through the x axis.
Mirror Y	Flips the selected object(s) through the y axis.
R90	Rotates the selected object(s) 90 degrees.
R180	Rotates the selected object(s) 180 degrees.
R270	Rotates the selected object(s) 270 degrees.

You can flip a hierarchical object on the x-axis or the y-axis, as follows:
Select the hierarchical object and click the middle mouse button. From the context menu that appears, select Flip Horizontal or Flip Vertically to flip the hierarchical object on the x-axis or the y-axis respectively.

All the placed or fixed objects inside the hierarchical objects are also flipped.

Related Text Commands

- `flipOrRotateObject`

Edit Halo

Use the Edit Halo form to add a routing halo or a placement halo to prevent the routing and/or placement of blocks and standard cells in order to reduce congestion around a block. These halos can be specified for hard macros, blackboxes, or committed partitions. When you add a halo to a block, it becomes part of the block's properties. If you move the block, the halo moves with it.

For the bottom-up hierarchical flow, use this form to specify routing halo for a block at the top-level design or at the block-level design.

Note: For top-down hierarchical flow, specify routing halo for a partition through the Specify Partition form.
Highlight block(s) in the design display area and choose *Floorplan* - *Edit Floorplan* - *Edit Halo*.

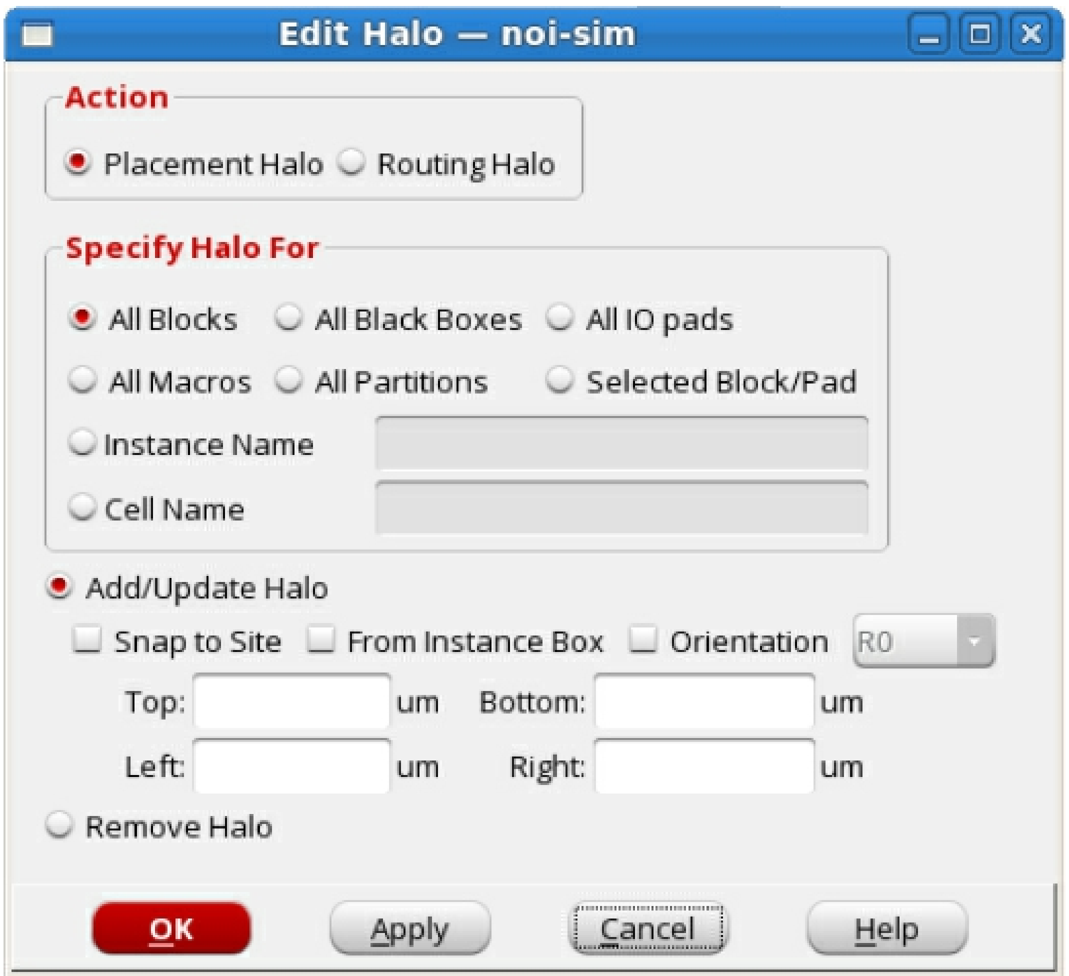
The Edit Halo form includes two pages:

- Edit Halo - Placement Halo
- Edit Halo - Routing Halo

Placement Halo

Use the *Placement Halo* page to add placement halos to a block. You can also use this form to delete placement halos.

Choose *Floorplan - Edit Floorplan - Edit Halo.*



Edit Halo - Placement Halo Fields and Options

All Blocks	Specifies that the halo will be created for all blocks.	
All Black Boxes	Specifies that the halo will be created for all black boxes.	
All IO Pads	Specifies that the halo will be created for all IO pads.	
All Macros	Specifies that the halo will be created for all macros.	
All Partitions	Specifies that the halo will be created for all partitions.	
Selected Block/Pad	Specifies that the halo will be created for the selected blocks.	
Instance Name	Specifies the block where the halo is to be added. You can use wildcards (* or ?) for specifying instance names.	
Cell Name	Specifies halo values for all instances of a cell.	
Add/Update Halo	(Default) Adds or overwrites a placement halo. Define the halo using the following fields:	
	Snap to Site	Snaps the halo box to a site.
	From Instance Box	Creates a block halo, based on the instance boundary, even when there is an overlap layer defined in the block cell or macro definition.
	Orientation	Specifies the orientation value of the instances to which the block halo values are applied. The orientation value can be R0, R90, R180, R270, MX, MX90, MY, or MY90.
	Top	Specifies the distance, in micrometers, from the top edge of the block to the end of the halo area.
	Bottom	Specifies the distance, in micrometers, from the bottom edge of the block to the end of the halo area.
	Left	Specifies the distance, in micrometers, from the left edge of the block to the end of the halo area.
	Right	Specifies the distance, in micrometers, from the right edge of the block to the end of the halo area.

Remove Halo	Removes the placement halo.

Related Text Commands

- `addHaloToBlock`
- `deleteHaloFromBlock`

Routing Halo

Use the *Routing Halo* page to add routing halo for blackboxes, hard macros, or block-level designs. You can also use this form to delete routing halos. A routing halo significantly reduces the possibility of long wire routing within the specified area, thus helping reduce signal integrity violations at the top- and/or block-level designs. A routing halo is honored only by the signal router.

Choose *Floorplan - Edit Floorplan - Edit Halo - Routing Halo.*


Edit Halo — noi-sim
Action
Placement Halo
Routing Halo
Specify Halo For
All Blocks
Selected Blocks
Selected Instances
Design Halo
Block Names
Instance Names
Cell Name
Litho Halo
Add/Update Halo
Halo Value:
um
Bottom Layer:
M1(1)
Top Layer:
AP(7)
Remove Halo
OK
Apply
Cancel
Help

Edit Halo - Routing Halo Fields and Options

All Blocks	Specifies that the routing halo should be added to all blocks in the design.	
Selected Blocks	Specifies that the routing halo will be created for selected blocks.	
Selected Instances	Specifies that the routing halo will be created for selected instances.	
Design Halo	Specifies that the routing halo should be added at the block-level design.	
Block Names	Specifies that the routing halo should be added to the specified blocks. A block name must be an instance name and not a cell master name. The specified blocks should be separated by a space.	
Instance Names	Specifies that the routing halo should be added to the specified instance. This parameter can be useful for adding halo for I/O cells.	
Cell Name	Specifies that the routing halo should be added to the specified cell.	
Litho Halo	Adds a litho halo to the instances on each routing layer with `LEF LITHOMACROHALO` defined.	
Add/Update Halo	(Default) Adds or overwrites a routing halo. Define the halo using the following fields:	
	Halo Value	Specifies the routing halo value in microns.
	Bottom Layer	Specifies the bottom layer for the routing halo.
	Top Layer	Specifies the top layer for the routing halo.
Remove Halo	Removes the routing halo.	

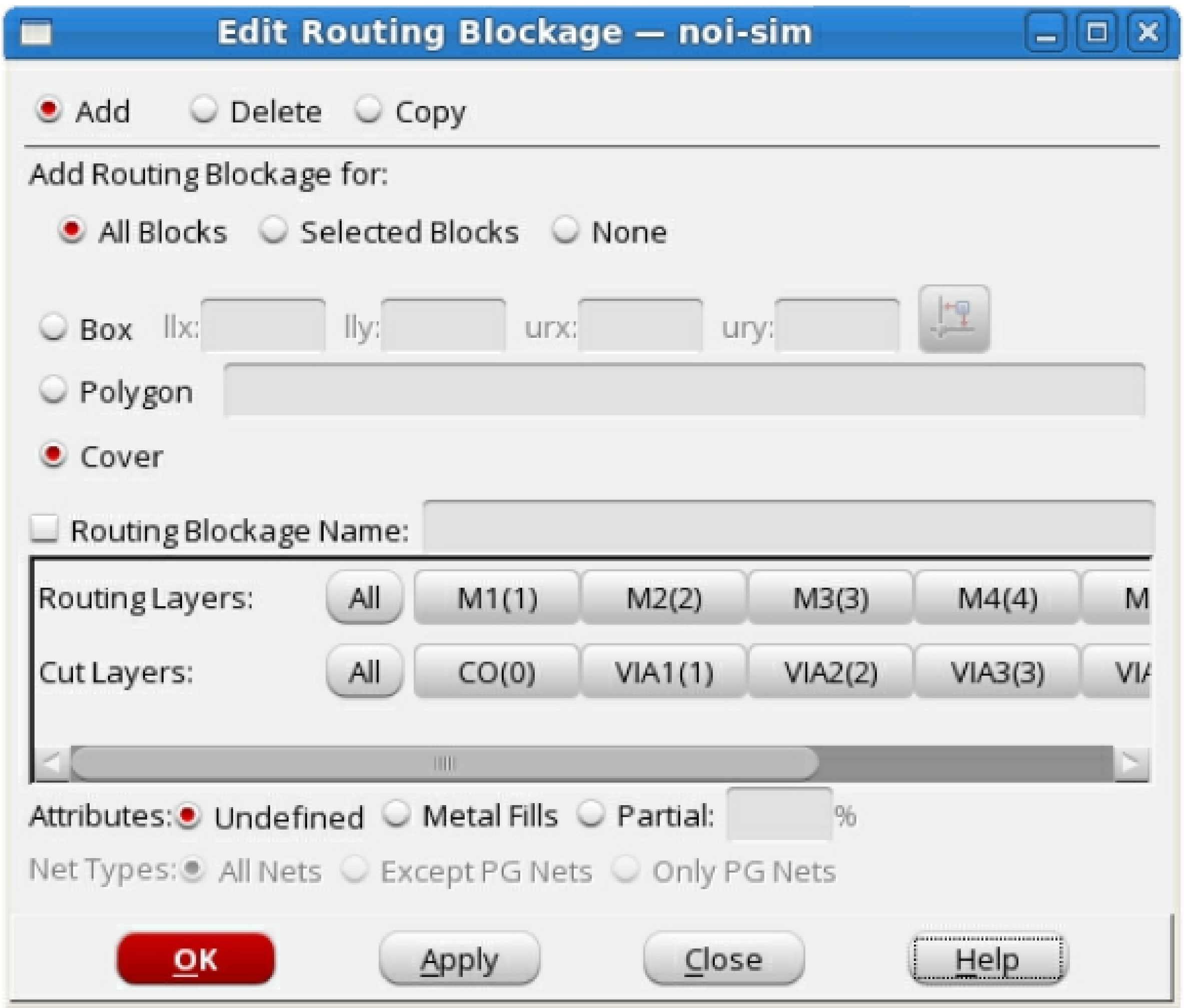
Related Text Commands

- `addRoutingHalo`
- `deleteRoutingHalo`

Edit Routing Blockage

Use the *Edit Routing Blockage* form for creating, editing, deleting, and copying routing blockages.

- Choose *Floorplan - Edit Floorplan - Edit Routing Blockage*.



The *Edit Routing Blockage* form has three pages:

- Add Page
- Delete Page
- Copy Page

Add Page

Use the *Edit Routing Blockage* form to create a routing blockage object that can be moved even outside the core area. The object area prevents routing of specified metal layers, signal routes, and hierarchical instances in this area.

Edit Routing Blockage - Add Fields and Options

All Blocks	Adds routing blockages for all blocks.
Selected Blocks	Adds routing blockages for selected blocks.
None	Adds routing blockages that are not associated with any places macro.
Box	Specifies the coordinates of the blockage, in microns, for the lower left (*llx*) and upper right (*urx*) boundaries in the x-direction, and the lower left (*lly*) and upper right (*ury*) boundaries in the y-direction.
Polygon	Specifies the polygon vertices of the blockage, in microns. **Note:** You must specify the vertices in the x1 y1 x2 y2 . . . format.
Cover	Specifies that a routing blockage of the same size as the selected block instance(s) will be created on top of the instance. **Note:** You must select a block instance while using this option.
Routing Blockage Name	
	Specifies the name of the route blockage.

Routing/ Cut Layers	*Routing Layers* specify the layer, list of layers, or all layers on which the routing blockage is to be applied. **Note:** The values specified with this parameter will override any default blockage layers specified with the `setRouteBlkDefaultLayer` command. *Default*: If you do not specify this parameter, the Innovus software will check if any default blockage layers have been specified with the `setRouteBlkDefaultLayer` command. If yes, the layers specified with the `setRouteBlkDefaultLayer` command will be used. If no, the default is wire3 if the number of layers is greater than 3, or wire2 if the number of layers is less than or equal to 3. *Cut Layers* specify the cut layer, list of cut layers, or all cut layers on which the routing blockage is to be applied. To specify cut layer between *Metal*1 and *Metal*2, select *V12*. Similarly, if you want to create blockage on cut layer between *Metal*2 and *Metal*3, select *V23.*
Trim Layers	Specifies the trim metal layer, list of trim metal layers, or all trim metal layers on which the routing blockage is to be applied.
Region Layers	Specifies the DRC region layers on which the routing blockage is to be applied.
Undefined	Specified that the routing blockage is to be applied on undefined nets.
Metal Fills	Specifies that the routing blockage is to be applied on metal fills.
Partial	Specifies that the routing blockage should be partial. A partial routing blockage has a density attribute that defines how many percent of routing tracks are available for each layers. For example, a density of 75% means 75% of routing tracks are available and 25% are blocked. 0% is equivalent to full routing blockage. If there is any overlap of two partial routing blockages with different density attributes, the lower density will be used in the overlapping regions.
All Nets	Specifies that the routing blockage is to be applied on all nets.
Except PG Nets	Specifies that the routing blockage is to be applied on a signal net routing and not on power or ground net routing. **Note:** Blocking the signal net routing helps in avoiding cross talk or coupling caused by signal route.

Only PG Nets	Specifies that the routing blockage is to be applied only on power and ground nets.

Related Text Command

- createRouteBlk

Delete Page

The Delete page within the *Edit Routing Blockage* form is used to delete routing blockage objects.

Edit Routing Blockage - Delete Fields and Options

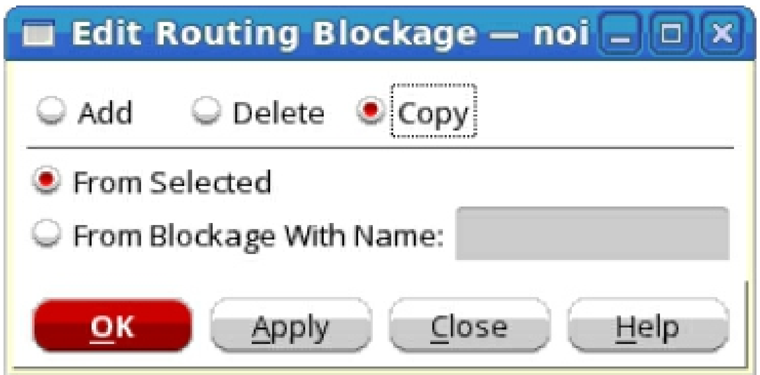
All Routing Blockages	Removes all route blockage objects in the floorplan.
Selected Routing Blockages	
	Removes the selected routing blockages.
Routing Blockages Linked To All Blocks	
	Removes routing blockages linked to all blocks.
Routing Blockages Linked To Selected Blocks	
	Removes routing blockages linked to selected blocks.
By Box	Removes the bounding box of blockage area. The coordinates of the bounding box (*llx lly urx ury*) are specified in microns.
By Routing Name Blockage	
	Removes the specified routing blockage.
Routing Layers	Specifies the layer, list of layers, or all layers on which the routing blockage is to be deleted. *Default*: If you do not specify this parameter, it deletes the routing blockage object on all layers.
Cut Layers	Specifies the cut layer, list of cut layers, or all cut layers on which the routing blockage is to be deleted. *Default:* If you do not specify this parameter, it deletes the routing blockage object on all cut layers.
Trim Layers	Specifies the trim metal layer, list of trim layers, or all trim metal layers on which the routing blockage is to be deleted. *Default:* If you do not specify this parameter, it deletes the routing blockage object on all trim metal layers.
Region Layers	Specifies the DRC region layers on which the routing blockage is to be deleted.

Related Text Command

- `deleteRouteBlk`

Copy Page

The Copy page within the *Edit Routing Blockage* form is used to copy routing blockages.



Edit Routing Blockage - Copy Fields and Options

From Selected	Creates a copy from the selected routing blockage.
From Blockage With Name	
	Creates a copy from the specified routing blockage.

Alternatively, you can select a routing blockage and then select *Copy* from the context menu.

Note: The copy of the routing blockage is automatically pasted, partially overlapping the original blockage.

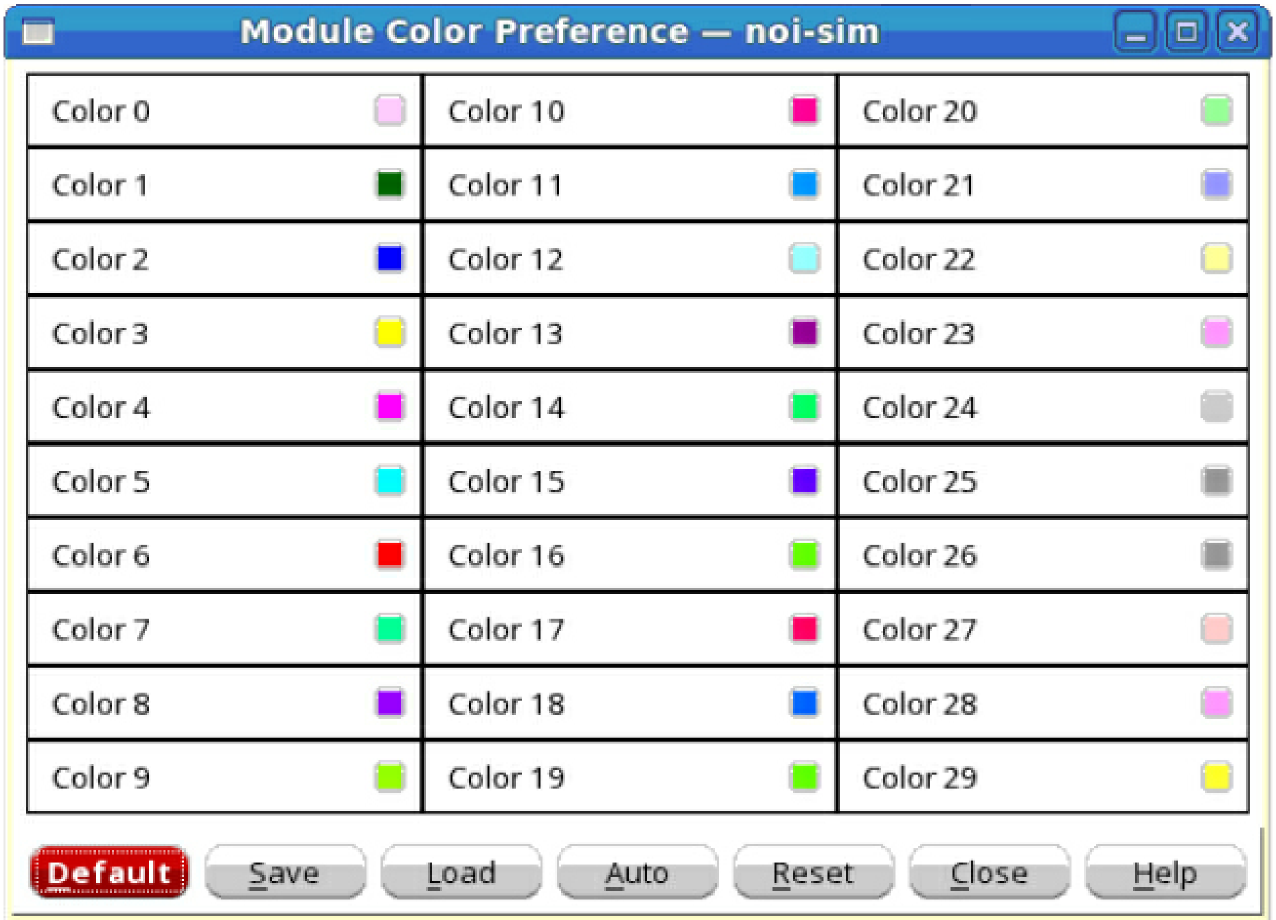
Related Text Command

- `createRouteBlk`

Color Module

Use the Module Color Preference form to create a color table to use for coloring modules.

- Choose *Floorplan - Edit Floorplan - Color Module*.



Module Color Preferences - Fields and Options

Close	Closes the Module color preference form.
Use Default	Loads the software's default color table into the form.
Save	Saves the color table.
Load	Loads a previously saved color table.
Auto	Applies colors from the color table to modules (starting from the lowest index color to the highest index color, depending on the number of modules in the design).
Reset	Resets the module colors to the software's default color values.

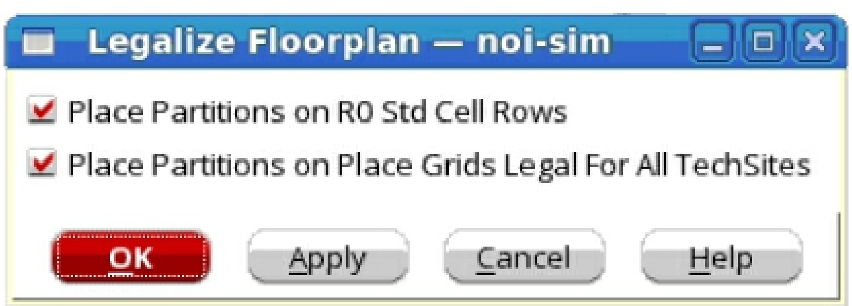
Legalize Floorplan

Use the Legalize Floorplan form for cases where you might have to legalize partition locations according to standard cell row orientations or specific constraints of your design. For each partition, the software checks if it overlaps with any row cutting areas. If it does, the software finds the closest location where the partition has no overlap with any row cutting area.

If the horizontal distance between the new location and old location is less than or equal to the width of the partition, and the vertical distance between the new location and old location is less than or equal to the height of the partition, the software moves the partition to a new location.

Note: If no legalization rules are specified, the Innovus software does not check any legal rules.

- Choose *Floorplan - Edit Floorplan - Legalize Floorplan*.



Legalize Floorplan Fields and Options

Place Partitions on R0 Std Cell Rows	
	Specifies that all partitions snap to the closest `R0` row on the grid. For this rule, the Innovus software assumes that standard cell rows start with an `R0` orientation and continue in an `R0`-to-`MX` pattern.
Place Partitions on Place Grids Legal For All TechSites	
	Specifies that partitions be placed on grids so that they are legal for all design constraints.

Related Text Command

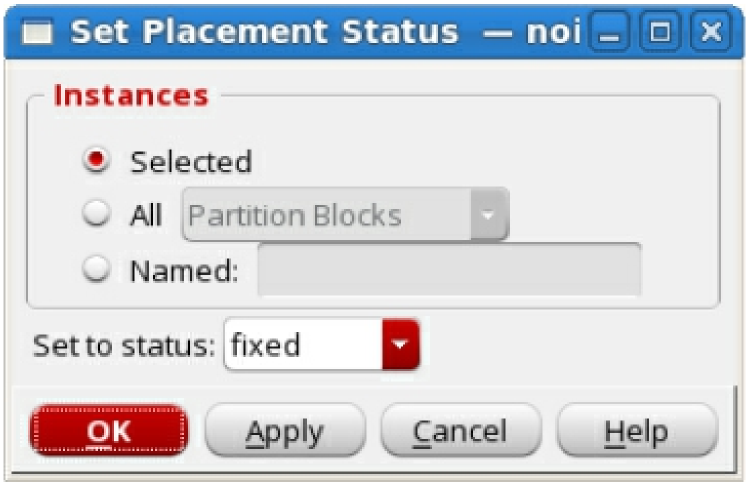
- `legalizePin`

Set Instance Placement Status

Use the Set Placement Status form to change placement status for all instances or selected instances.

Note: This cannot be used to change the placement status of standard cells.

- Choose *Floorplan - Edit Floorplan - Set Instance Placement Status*.


Set Placement Status — noi
Instances
Selected
All
Partition Blocks
Named:
Set to status:
fixed
OK
Apply
Cancel
Help

Set Placement Status - Fields and Options

Selected	Specifies all instances selected (highlighted) in the design display area.
All	Specifies the type of instance to enclose macros. Use the pull-down menu to choose *Hard Macros*, *Partition Blocks*, or *Black Boxes*.
Named	Specifies a particular instance. You can use a wildcard character (*) in this field.
Set to status	Use the pull-down menu to specify a *cover*, *fixed*, *softFixed*, *placed*, or *unplaced* placement status for the specified instances. • *cover*: Specifies the change in placement status to a *cover* status. The cover component has a location, but cannot be moved by automatic tools or interactive commands. • *fixed*: Specifies the change in placement status to a *fixed* status. The fixed component has a location and cannot be moved by automatic tools, but can be moved using interactive commands. • *softFixed*: Specifies the change in placement status to a *softFixed* status. The softFixed placement status means that instances cannot be moved by global placement and can only be moved by the legalization step of detail placement. Instances with this status can also be upsized by optimization. • *placed*: Specifies the change in placement status to a *placed* status. The placed component has a location, and can be moved using automatic tools and interactive commands. • *unplaced*: Specifies the change in placement status to be an *unplaced* status. The unplaced component does not have a location.

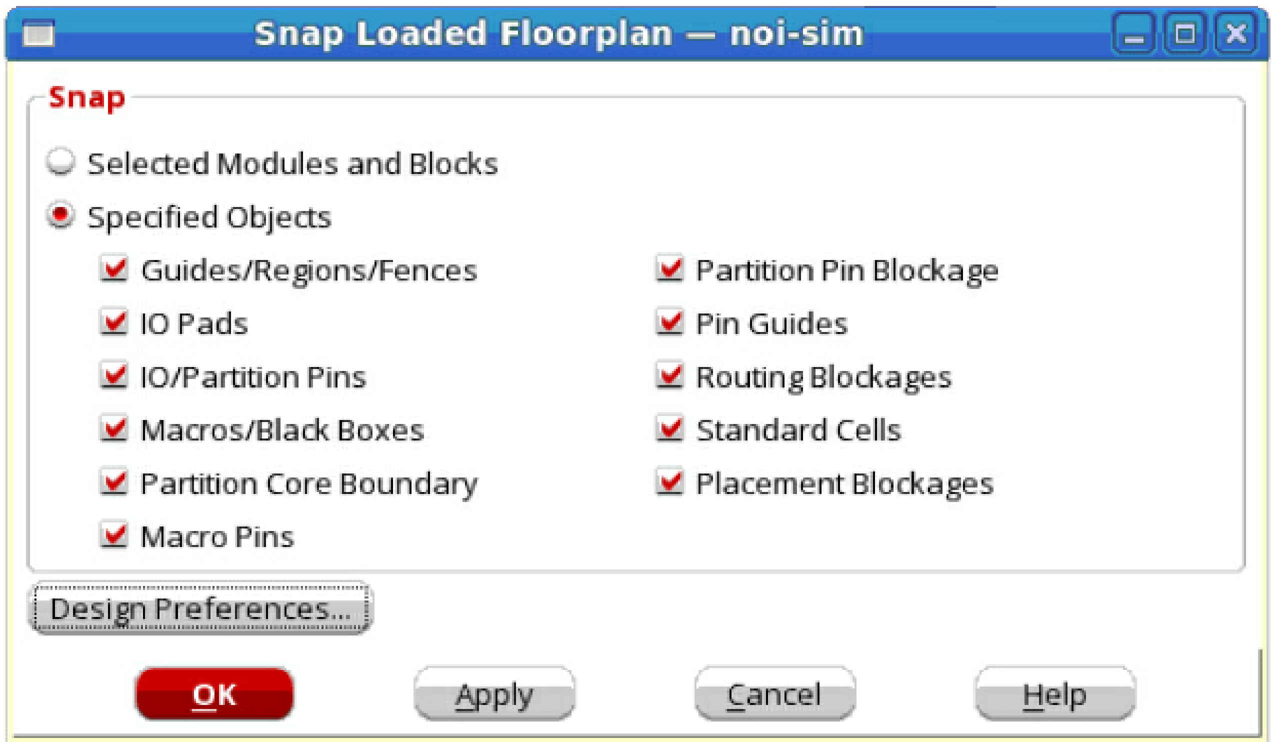
Related Text Command

- `setInstancePlacementStatus`

Snap Floorplan

Use the Snap Loaded Floorplan form to snap objects to the grid. You can define the snap grid in the Preferences form.

- Choose *Floorplan - Snap Floorplan*.



Alternatively, you can click the middle mouse button to bring up a context sensitive pop-up menu to select the *Snap* command.

Note: To undo the previous action, use the *Undo* widget or `U` bindkey. To restore the design to the same state as before the undo, use the *Redo* widget or `R` bindkey.

Snap Loaded Floorplan Fields and Options

Selected Modules and Blocks	Specifies snapping floorplan modules and blocks that are selected in the design display area.
Specified Objects	Specifies snapping one or more of the following floorplan objects
Guides/Regions/Fences	Specifies snapping floorplan guides, regions, and fences.
IO Pads	Specifies snapping floorplan I/O pads.
IO Pins/Partition Pins	Specifies snapping floorplan I/O pins and partition pins.
Macros/Blackboxes	Specifies snapping floorplan macros (hard blocks).
Partition Core Boundary	Specifies snapping floorplan partition core boundary. **Note:** This will snap to core-grid. However, if the partition is a power-domain, this will snap to placement grid.
Macro Pins	Specifies snapping floorplan macro pins.
Partition Pin Blockage	Specifies snapping floorplan partition pin blockage.
Pin Guides	Specifies snapping floorplan pin guides. **Note:** This will snap to mfg. grid and not to tracks.
Routing Blockages	Specifies snapping floorplan routing blockages.
Standard Cells	Specifies snapping floorplan standard cells.
Placement Blockages	Specifies snapping floorplan placement blockages.
Design Preferences...	Brings up the Preferences - Floorplan GUI.

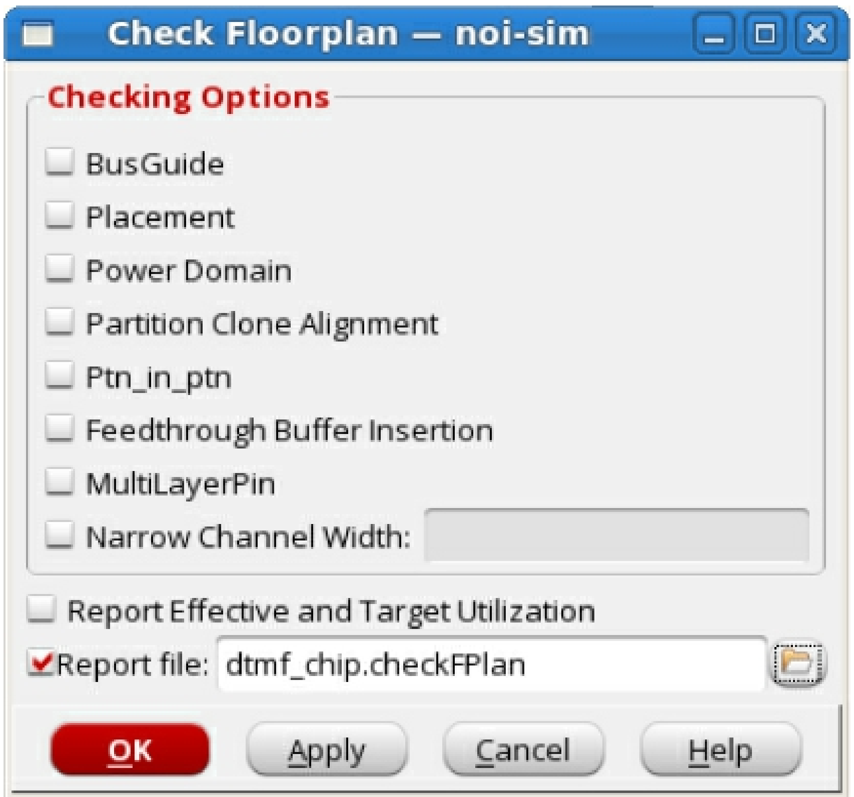
Related Text Command

- `snapFPlan`
- `snapFPlanIO`

Check Floorplan

Use the Check Floorplan form to identify problems before a design is passed to downstream tools. You can check the routing grid, placement, pins, power domains, partition clone alignment, and feedthrough buffer insertion.

- Choose *Floorplan - Check Floorplan*.



Check Floorplan Fields and Options

BusGuide	Checks incorrect overlapping and connectivity.
Placement	Checks the placement.
Power Domains	Checks the power domains.
Partition Clone Alignment	Checks that partition clones are aligned with their master on the power mesh. This checks that the master and clones partitions are inside a core boundary, and ensures that the partition fence instances sizes match the master instance.
Ptn_in_ptn	Checks if child partitions reside inside parent partitions. When nested partition (fences, regions, or guides) are detected in floorplan, following legality checks are performed: • Inner partition module should be completely enclosed by outer partition module • Inner partition module should be logically the child of the outer partition module
Feedthrough Buffer Insertion	Checks feedthrough buffer insertion.
MultiLayerPin	Checks multi layer pins.
Narrow Channel Width	Reports narrow channels whose width, in microns, is smaller than the specified value.
Report Effective and Target Utilization	
	Reports effective utilization (EU) and target utilization (TU) for the entire design, fences, and regions (partitions, power domains, and regular fences).
Report File	Outputs detailed information for the specified checks. The default filename is `hdr_top.checkFPlan`.

Related Text Command

- `checkFPlan`

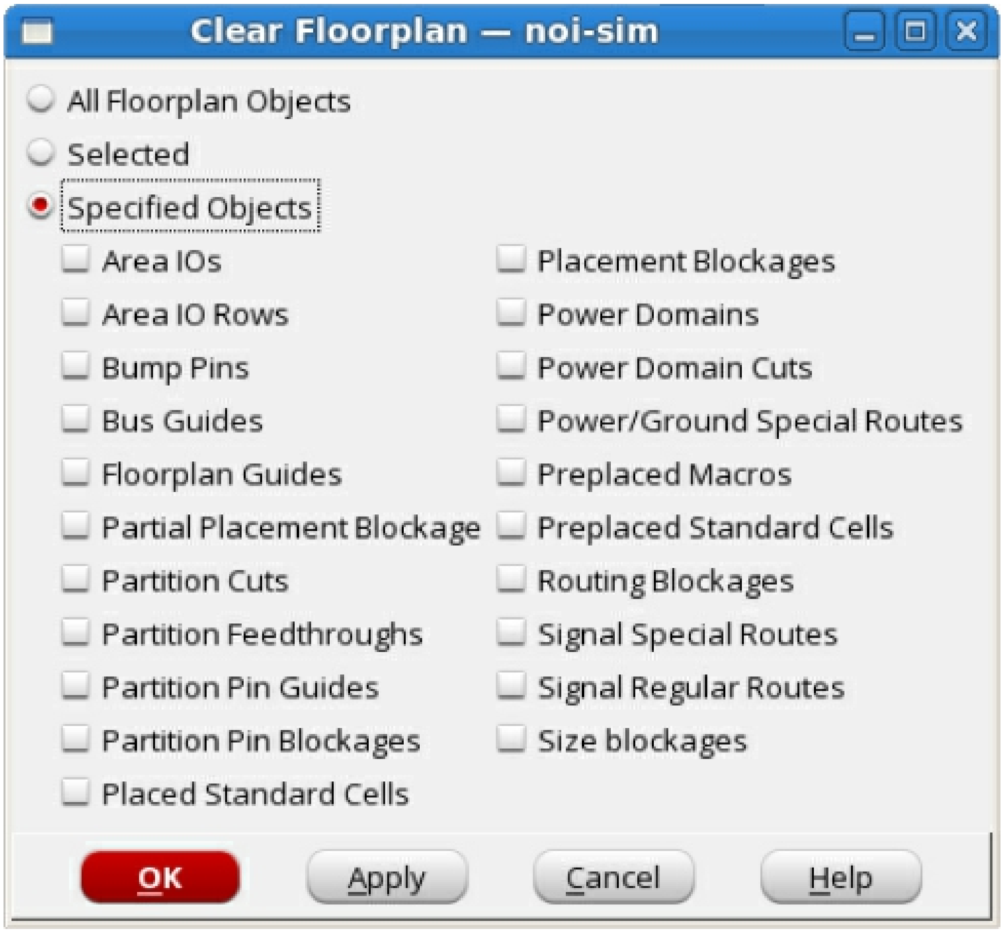
Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Clear Floorplan

Use the Clear Floorplan form to remove the design's floorplan constraints. You can clear these constraints at any time. If any floorplan constraints are changed, you must run, or rerun, the placement program.

- Choose *Floorplan - Clear Floorplan*.



Clear Floorplan Fields and Options

All Floorplan Objects	Clears all floorplan objects, including instance groups.	
Selected	Clears all floorplan objects currently selected in the design window.	
Specify Objects	Clears all the specified objects. You can specify one or more of the following objects.	
	Area IO	Removes area I/O cells.
	Area IO Rows	Removes all area I/O rows.
	Bump Pins	Removes all bump pins.

	Bus Guide	Removes all bus guides.
	Floorplan Guides	Removes all module constraints. The modules will be unplaced outside the core area.
	Partial Placement Blockages	Removes all partial placement blockages (area density screens)
	Partition Cuts	Removes all partition cuts for partition modules.
	Partition Feedthroughs	Removes all partition feedthrough guides for the partition modules.
	Partition Pin Guides	Removes all partition pin guides for partition modules.
	Partition Pin Blockages	Removes all partition pin blockages for partition modules.
	Placed Standard Cells	Unplaces all standard cells that have a fixed placement status.
	Placement Blockage	Removes all placement blockages.
	Power Domains	Removes all power domain objects.
	Power Domain Cuts	Removes all power domain cuts.
	Power/Ground Special Routes	Removes all power and ground special wires.
	Preplaced Macros	Unplaces all preplaced macros.
	Preplaced Standard Cells	Unplaces all preplaced standard cells.
	Routing Blockages	Removes all routing blockages.
	Signal Special Routes	Removes all signal special routes.

	Signal Regular Routes	Removes all signal regular routes.

Related Text Commands

- `deleteAllDensityAreas`
- `deleteAllFPObjects`
- `deletePlaceBlockage`
- `deleteAllPowerPreroutes`
- `deleteAllSignalPreroutes`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Instance Group

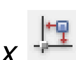
Use the Group Instances form to improve your design hierarchy, apply and test different hierarchical schemes prior to regrouping the netlist, and determine the initial size and shape of the floorplan object.

By default, all instance groups are output to the netlist as logic modules when saving the regrouped netlist. The new group can be viewed or displayed by using the pull-down menu from *Floorplan - Instance Group*, or by using the Design Browser and selecting *Group*.

- Click on and highlight the module or submodule guides that you want in the group and choose *Floorplan - Instance Group - Create New Group*.


Group Instances — noi-sim
Group Name:
new_group
Specify Box
Guide
Fence
Region
Floating Fence
llx
0.0
lly
0.0
urx
0.0
ury
0.0
Specify Placement Density
70
%
Aspect Ratio
1
Create as Physical Hierarchy
Remove Old Constraint
OK
Cancel
Help

Group Instances Fields and Options

Group Name	Specifies the name of the new group.
Specify Box	Allows you to select a module constraint type: • *Guide:* Creates a group of guides. • *Fence:* Creates a group of fences. • *Region:* Creates a group of regions. • *Floating Fence:* Creates a group of floating fence/region. This constraint allows the entire region/fence to move as a cluster across the core area.
llx lly urx ury	Specifies the coordinates of the bounding box, in microns, for the lower left (*llx*) and upper right (*urx*) boundaries in the x-direction, and the lower left (*lly*) and upper right (*ury*) boundaries in the y-direction. You can type in the fields, or click *Get Box*  icon and use the left mouse button to drag over an area in the design display area to get the boundary coordinates.
Specify Placement Density %	Specifies a placement density value. The default is 70%.
Aspect Ratio	Specifies an aspect ratio value. This is the ratio of the floorplan object's width divided by the height.
Create as Physical Hierarchy	Specifies that the created group is a physical hierarchy. If you deselect this option, the created group is not saved back to the netlist. To change this option after creating the instance group, use the Object Attribute form.
Remove Old Constraint	Specifies that the existing constraints are removed when creating the instance group.

Related Text Commands

- `addInstToInstGroup`
- `createInstGroup`
- `deleteAllInstGroups`
- `deleteInstFromInstGroup`
- `deleteInstGroup`

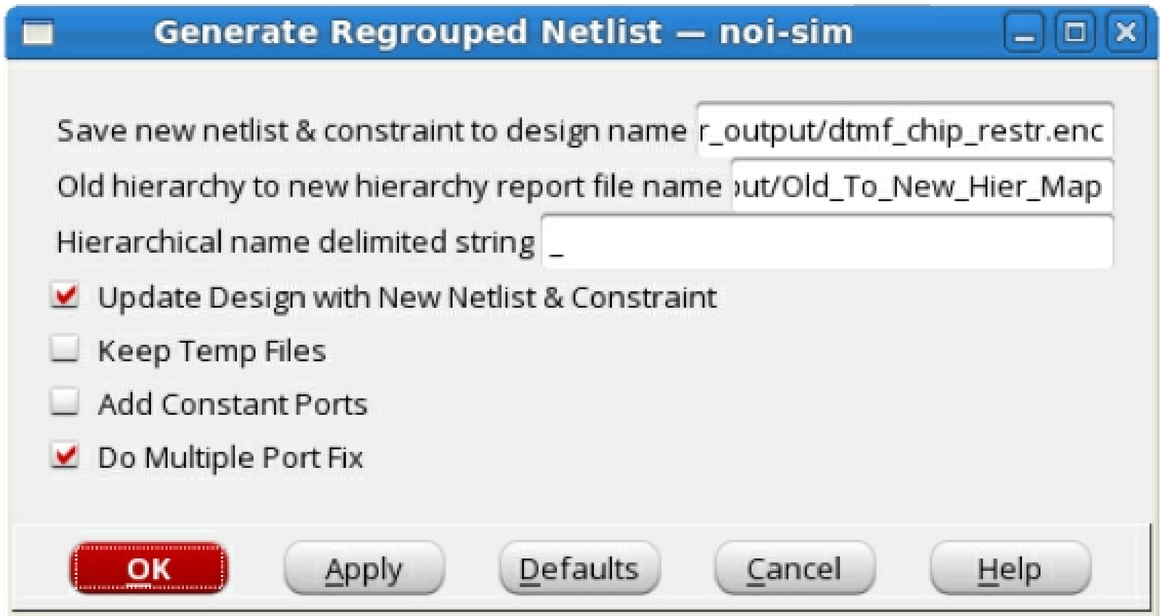
Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Generate Regrouped Netlist

Use the Generate Regrouped Netlist form to save instance groups back to the netlist.

- Choose *Floorplan - Generate Regrouped Netlist*.



Generate Regrouped Netlist - Fields and Options

Save new netlist & constraint to design name	
	Specifies the new directory prefix where the data will be stored. The default name is`top_module_restruct.enc`.
Old hierarchy to new hierarchy report file name	
	Specifies a report file that provides the mapping between the old and new logical hierarchy. This enables you to provide the report file directory and file name.
Hierarchical name delimited string	

<table>
<tr><td></td><td>Generates the hierarchical name for moved instances after restructuring. For example, if you have an original hierarchy of <code>/a/b/c</code> and want to place module <code>c</code> into a new module called <code>r</code>, using the following delimiters will enable you to retain the original hierarchy name after restructuring:

<code>delimiter: _ (underscore)</code>
<code>original hierarchy: /a/b/c</code>
<code>new hierarchy: /r/a_b_c</code>

<code>delimiter: / (slash)</code>
<code>original hierarchy: /a/b/c</code>
<code>new hierarchy: /r/a\/b\/c</code>

<code>delimiter: "" (no name delimiter)</code>
<code>original hierarchy: /a/b/c</code>
<code>new hierarchy: /r/c</code></td></tr>
<tr><td colspan="2">Update Design with New Netlist _Constraint</td></tr>
<tr><td></td><td>Updates the design netlist and constraints.</td></tr>
<tr><td>Keep Temp Files</td><td>Keeps temporary files.</td></tr>
<tr><td colspan="2">Add Constant Ports</td></tr>
<tr><td></td><td>Adds constant ports and avoids additional assign nets for restructured instances. The software creates a constant port to propagate the tie-high and tie-low ports through the new hierarchy. A new netlist is assigned to the port with an assignment of 1.</td></tr>
<tr><td colspan="2">Do Multiple Port Fix</td></tr>
<tr><td></td><td>Specifies that no nets will be split.</td></tr>
</table>

Related Text Command

- `runRcNetlistRestruct`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Group Pin(s) Move

Use the Group Pin(s) Move form to change the pin layer, the pin size, pin status, and resolve pin overlap.

Complete the following steps in the design display area:

1. Click the *Move/Resize/Reshape* widget.
2. Select (left-click) the pin in the design display area.
   For a group of pins, press the `Shift` key to highlight each pin.
3. Left click on the pin(s) and move them to the new location.

Related Text Command

- `moveGroupPins`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Swap Two Selected I/O Cells

You can swap the locations of two selected I/O cells. Select the two I/O cells whose locations you want to swap and right-click the mouse. From the context menu that appears, select *Swap Instances*.

Related Text Command

- `swapPins`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Generate Floorplan

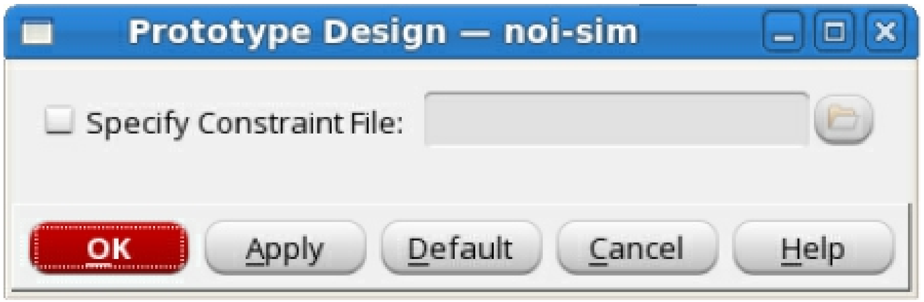
The Generate Floorplan menu provides the following forms and menu commands to guide you through major steps of the design planning stage of the prototyping flow.

- Prototype Design
- Initialize Fast Timing Analysis
- Fast Slack Analysis Display
- Generate Fence
- Place Macros

Prototype Design

Use the Prototype Design form to generate an initial floorplan for a design with FlexModels that can be used as a starting point for making the final floorplan.

- Choose *Floorplan - Generate Floorplan - Prototype Design*



Prototype Design - Fields and Options

Specify Constraint File	Specifies the constraint file name. *Default:* unchecked

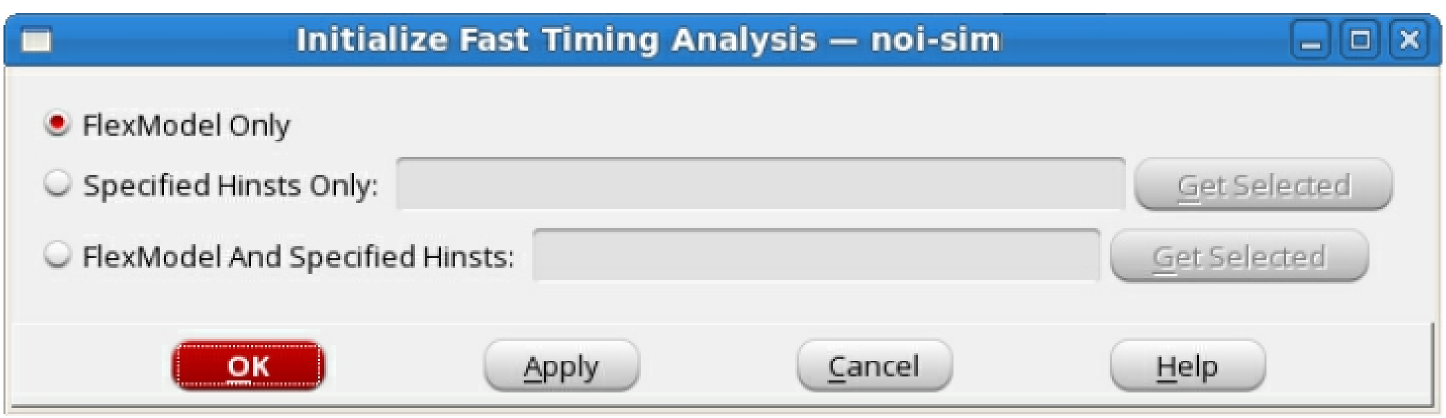
Related Text Command

- proto_design

Initialize Fast Timing Analysis

Initialize Fast Timing Analysis calculates the initial timing between FlexModels and/or specific modules based on Manhattan distance using psPM timing value for net delay.

- Choose *Floorplan - Generate Floorplan - Initialize Fast Timing Analysis*



The Initialize Fast Timing Analysis form is displayed.

- Choose one of three usage models based on your design

- Click *OK*

Once initialization is done, slack is automatically updated if the location of a model is changed.

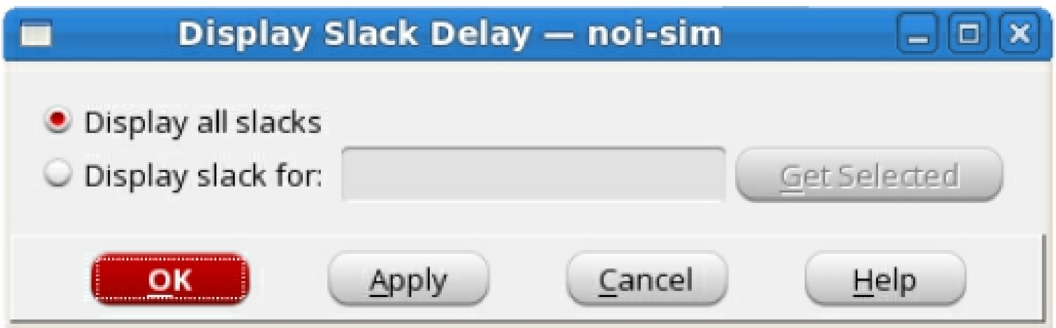
The *Slack Preference* Form is displayed (for detailed field descriptions, see Slack Preference form in the next section).

Note: The psPM model should be available before invoking fast slack timing analysis.

Fast Slack Analysis/Display

Use the Fast Slack Analysis/Display form for analyzing and displaying slack information of FlexModels and/or specified modules in the artwork window.

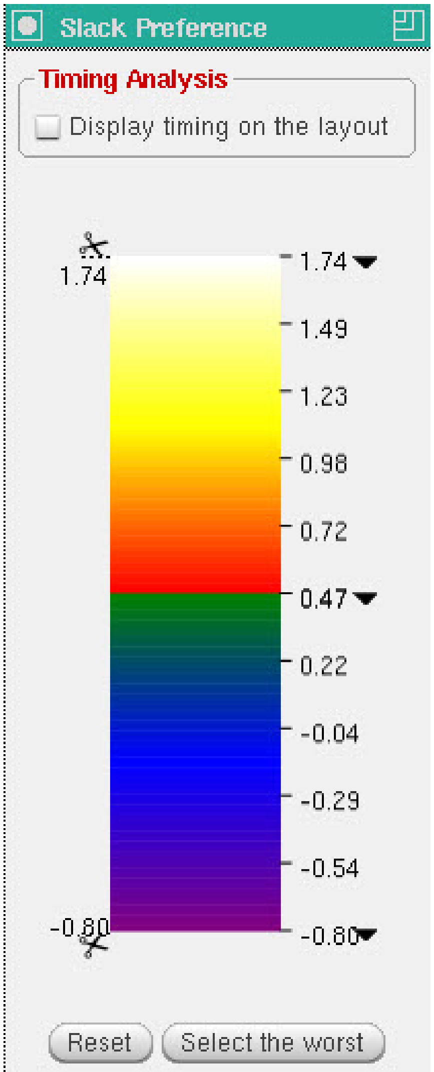
Choose *Floorplan - Generate Floorplan - Fast Slack Analysis/Display*



Display Slack Delay - Fields and Options

Display all slacks	Displays the slack for all models.
Display slack for:	Displays the slack for selected model.
Get Selected	Displays the name of a selected model. Clicking the *Get Selected* button without first selecting a model results in error.

On clicking the *Apply* button, the Slack Preference Form is displayed.


Slack Preference
Timing Analysis
Display timing on the layout
1.74
1.74
1.49
1.23
0.98
0.72
0.47
0.22
-0.04
-0.29
-0.54
-0.80
-0.80
Reset
Select the worst

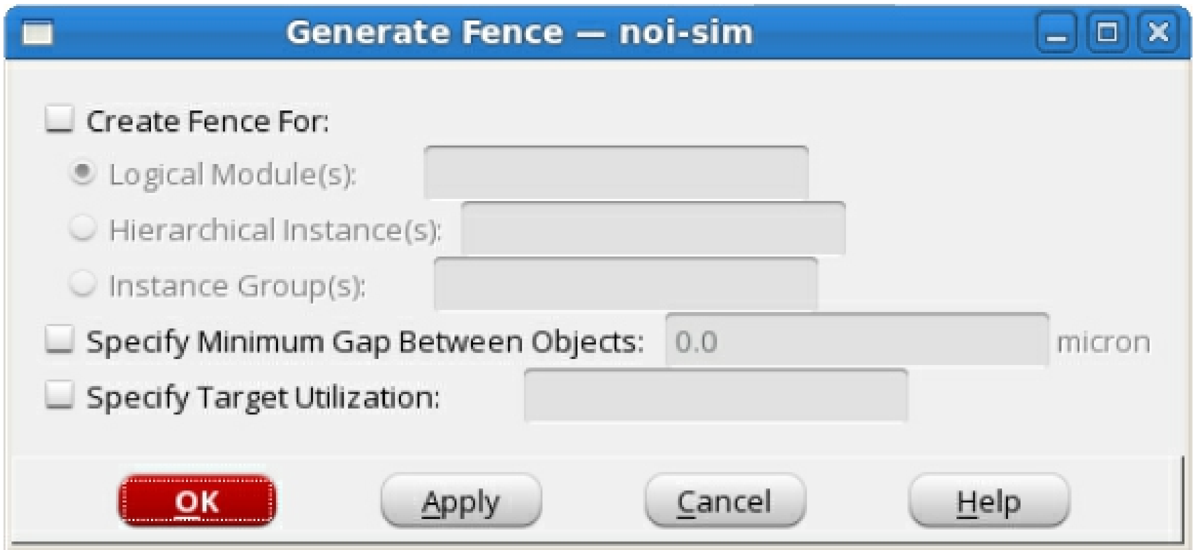
Slack Preference - Fields and Options

Display timing on the layout	When checked, displays the timing at the center of line. *Default:* unchecked
	Edit the Max/Min value of range.
	You can use the scissors to edit the range for timing slack. The scissor at the top of the color range indicates the maximum value of the slack and the scissor at the bottom of the color range indicates the minimum value of the slack. When you move the scissors along the color scale, the slack that is out of the range, specified by the two scissors, is hidden.
Select the worst	Selects the line for which slack is worst.
Reset	Resets the settings.

Generate Fence

Use the Generate Fence form to automatically draw partition fences that enclose all their children FlexModel guides and/or macros.

- Choose *Floorplan* - *Generate Floorplan* - *Generate Fence*



Generate Fence - Fields and Options

Logical Modules(s):	Specifies list of partition modules to draw fences. This option should be used for master/clone partitions.
Hierarchical Instance(s):	Specifies the list of hierarchical instance names to draw fences. This option can be used if you only want to create a fence for a specific master or clone. **Note:** It can not be used for both master and clones. You can use wildcards.
Instance Group(s):	Specifies list of instance group names to draw fences. You can use wildcards.
Specify Minimum Gap Between Objects:	Specifies the minimum-size gap between flexmode/block (in microns). *Default:* unchecked
Specify Target Utilization:	Specifies the target utilization value. *Default:* unchecked

Related Text Command

- `generate_fence`

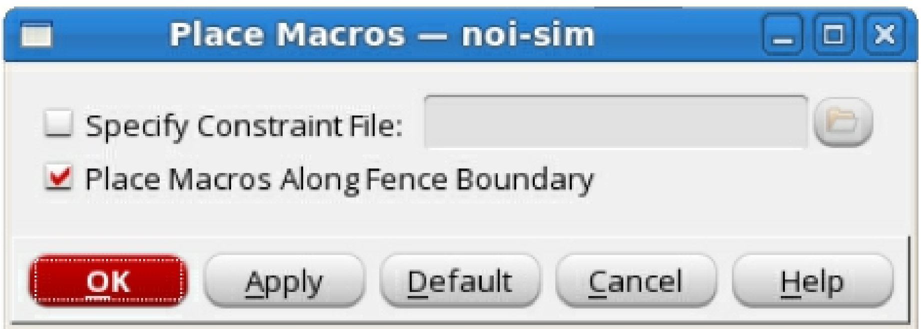
Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

Place Macros

Use the Places Macros form to place macros along the core boundary for chip and block designs.

- Choose *Floorplan - Generate Floorplan - Place Macros*



Place Macros - Fields and Options

Specify Constraint File:	Uses the constraints set in the specified Automatic Floorplan Synthesis constraint file for fence creation, macro placement and module guide generation. A constraint file is a text file that can contain a list of seeds for Automatic Floorplan Synthesis to use when generating fences and module guides, and basic relative, spacing and orientation constraints to follow during macro placement. (For more information, see Automatic Floorplan Synthesis Constraint File Format.) *Default:* unchecked
Place Macros Along Fence Boundary:	Places macros along the core boundary for chip and block designs. Macros are placed along the fence boundary for hierarchical floorplans. It avoids fence edges blocked by "macro only" blockage. Preplaced hard macro boundaries are also used, if possible. **Note:** Specifying this parameter can disable the `-maxDistToGuide` parameter. Seed locations might also be ignored. *Default:* unchecked

Related Text Commands

- `planDesign`
- `setPlanDesignMode`

Related Topics

- For information on Floorplan commands, see Floorplan Commands in the *Text Command Reference*.
- For information on the Floorplan flow, see *Floorplanning the Design* in the *User Guide*.

7

Power Menu

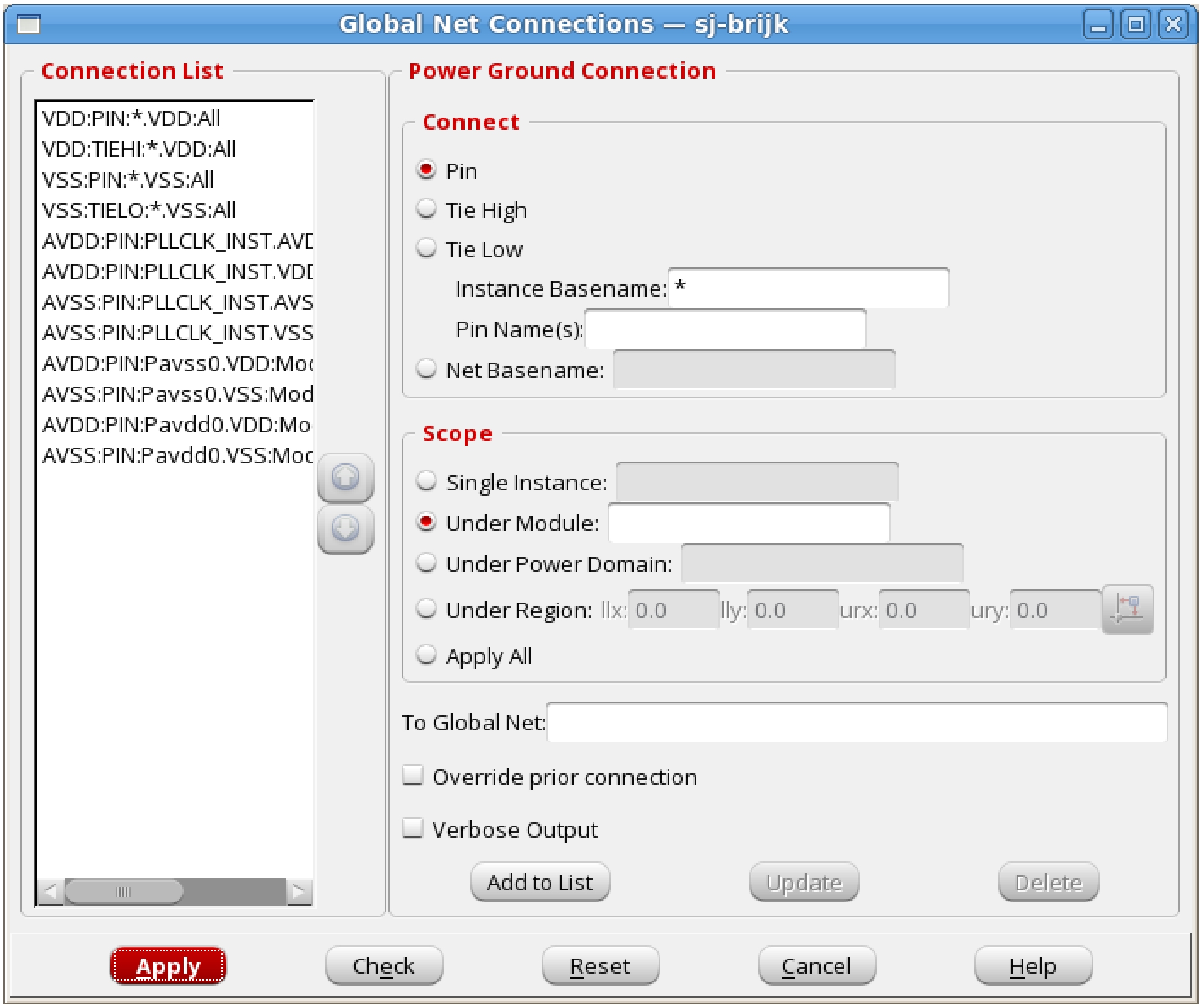
- Highlight Power Domains
- Highlight MSV Objects - Power Domain
- Highlight MSV Objects - Signal Net/HLS Cell
- Highlight MSV Objects - Highlight Set
- Color
- Report Power Domain
- Verify Power Domain
- Power Planning
- Add Rings
- Add Rings - Basic
- Add Rings - Advanced
- Add Rings - Via Generation
- Net Selection
- Add Stripes
- Add Stripes - Basic
- Add Stripes - Advanced
- Add Stripes - Via Generation
- Create P/G Pin
- Pg Cut/Repair
- Edit Power Vias
- Edit Power Vias - Basic
- Edit Power Vias - Advanced
- Power Analysis
- Set Power Analysis Mode
- Set Power Analysis Mode - Basic
- Set Power Analysis Mode - Advanced
- Run Power Analysis

Connect Global Nets

The Global Net Connections form assigns pins or nets to a global net such as a power or ground. In addition, tie-high and tie-low pins are assigned to global nets.

Note: This form can be used for incremental updating.

→ Choose *Power - Connect Global Nets*.



Global Net Connections Fields and Options

Connection List	The list of connection information. When you select an item on the list, the *Power Ground Connection* panel of the form is populated with the corresponding information.
Power Ground Connection	

	Helps assign pins or nets to a global net such as a power or ground.	
Connect	Controls which objects are connected to the global net. Select one of the following options:	
	Pins	Select this option, then use the text entry field to specify the pin name to be connected. These are the power and ground port names in the standard cells, block cells, and I/O pad cells.
	Tie High	Connects the tie-high pins to a global power and ground net.
	Tie Low	Connects the tie-low pins to a global power and ground net.
	Instance Basename	Specifies the leaf instance basenames whose pins are to be connected to the global net. You can use a wildcard (*) as an entry. By default, all pins are connected.
	Pin Name(s)	Specifies the pins to connect to the global net.
	Net Basename	Select this option, then use the text entry field to specify the local net names. This connects local power and ground nets to the global power and ground nets. These net names must be initially specified during design import.
Scope	Provides a greater degree of control for specifying objects to connect to the global net. Select one of the following:	
	Single Instance	Makes a connection only to the specified instance.
	Under Module	Select this option, then use the text entry field to specify the module (or hierarchical instance) name from which the pins or local nets connect. Only the pins or local nets of the instances under the specified module are connected.
	Under Power Domain	
		Applies the global net connection to the instances within the specified power domain.

	Under Region	Select this option, then specify the coordinates for a region within the design display area that encompasses the pins or local nets to be connected. Clicking on the mouse icon and moving the cursor to the design display area enables you to use the mouse to specify the region coordinates.
	Apply All	Specifies that the pins or local nets connect from the top module in the hierarchy.
To Global Net	The power and ground net to which to connect a group of standard cells. Standard cells are connected to the net that you specify in the text entry field.	
Override prior connection		
	If selected, disconnects pins and local nets that are already connected to a global net before reconnecting them to the global net specified in this form. If deselected, only new pins and local nets are connected to the specified global net. This is the default.	
Verbose Output	If selected, connection statistics and warning messages are displayed in the console. If deselected, some warning messages are suppressed. This is the default.	
Add to List	Adds the new connection information to the *Connection List* at the left side of the form	
Update	Applies new values to the selected connection in the *Connection List*.	
Delete	Removes the selected connection from the *Connection List*.	
Apply	The pins and instances or local nets specified in the *Connection List* are connected to the specified global net.	
Check	Displays a list of instances for which power and ground pins are not connected to special nets.	
Reset	Removes power and ground connectivity from the global net.	

Related Text Commands

For information on the `globalNetConnect` command, see the "Power Planning Commands" chapter in the *Text Command Reference* document.

Related Topics

For more information, see the "Global Net Connections" section on the Power Planning and Routing page of *Innovus User Guide*.

Multiple Supply Voltage

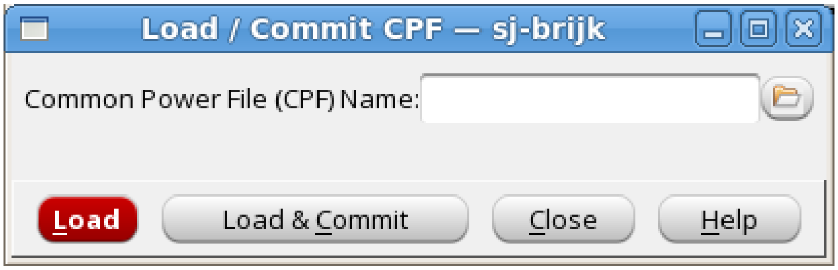
The Multiple Supply Voltage submenu contains the following items:

- Load/Commit CPF
  Opens the Load/Commit CPF form.
- Cut Power Domain by Overlaps
  Opens the Cut Power Domain by Overlaps form.
- Shifter/Isolation Cells
  Opens the Report Shifter/Isolation Cells form.
- Add Power Switch
  Opens the Add Power Switch forms.
- Flexible Chaining Options
  Opens the Chain/Unchain Power Switch Enable form.
- Delete Power Switch
  Opens the Delete Power Switches form.
- Verify Power Domain
  Opens the Verify Power Domain form.
- Report Power Domain
  Opens the Report Power Domain form.
- Highlight Power Domains.
  Opens the Highlight Power Domains forms.

Load/Commit CPF

Use the Load/Commit CPF form to load a Common Power Format (CPF) form into the design, or commit a CPF file that you have already loaded.

→ To open the Load/Commit CPF form, choose *Power - Multiple Supply Voltage - Load/Commit CPF.*



Load/Commit CPF Fields and Options

Commit	Executes the commands provided in the loaded CPF file, such as `create_power_domain`, `create_power_ground_connection`, and `create_*_logic`. As a result, running this command does the following: • Creates power domains • Creates logical power/ground net connections • Inserts shifter cells and isolation cells • Replaces regular registers with state-retention (SRPG) registers After running this command, you can then place and floorplan the power domains.
Common Power File (CPF) Name	
	Specifies the name of the CPF file to load or commit.
Load	Reads the CPF file and performs lint, parsing, and semantics checking. If the power/ground connections are incomplete, then the command automatically generates a power net specification template in CPF. You can then examine the template and update it to fully specify the power/ground connections.

Load & Commit	Reads the CPF file, as in *Load*, and runs the commands provided in the CPF file. Among many operations, this option does the following: • Creates power domains • Creates logical power/ground net connections • Inserts shifter cells and isolation cells • Replaces registers with state-retention (SRPG) registers

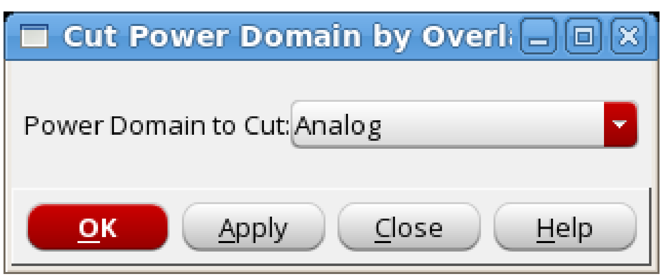
Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `read_power_intent`
- `commit_power_intent`

Cut Power Domain by Overlaps

Use the Cut Power Domain by Overlaps form to specify the power domain you want to cut to include another power domain you have created.
→ To open the Cut Power Domain by Overlaps form, choose *Power - Multiple Supply Voltage - Cut Power Domain by Overlaps*.



Cut Power Domain by Overlaps Fields and Options

Power Domain to Cut	Specifies the power domain to cut to include the nested power domain you have created.

Related Text Commands

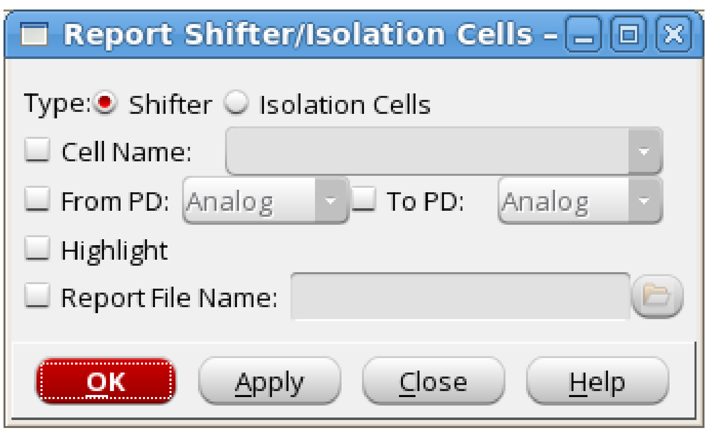
For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

`cutPowerDomainByOverlaps`

Report Shifter/Isolation Cells

Use the Report Shifter/Isolation Cells form to report or show isolation cells and instances, or level shifters.

→ To open the Report Shifter/Isolation Cells form, choose *Power - Multiple Supply Voltage - Shifter/Isolation Cells - Report/Highlight*.



Report Shifter/Isolation Cells Fields and Options

Shifter	Reports shifters.
Isolation Cells	Reports isolation cells.
Cell Name	Reports shifters or isolation cells with the specified cell name.

From PD	Reports shifters or isolation cells between power domain pairs.
To PD	Reports shifters or isolation cells in the receiving power domain.
Highlight	Highlights placed level shifters or isolation cells.
Report File Name	Specifies the name of the report file you want to generate.

Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `reportIsolation`
- `reportShifter`

Add Power Switch

The Power Switch Insertion form has the following pages:

- Power Switch Ring
- Power Switch Column

Power Switch Insertion - Ring

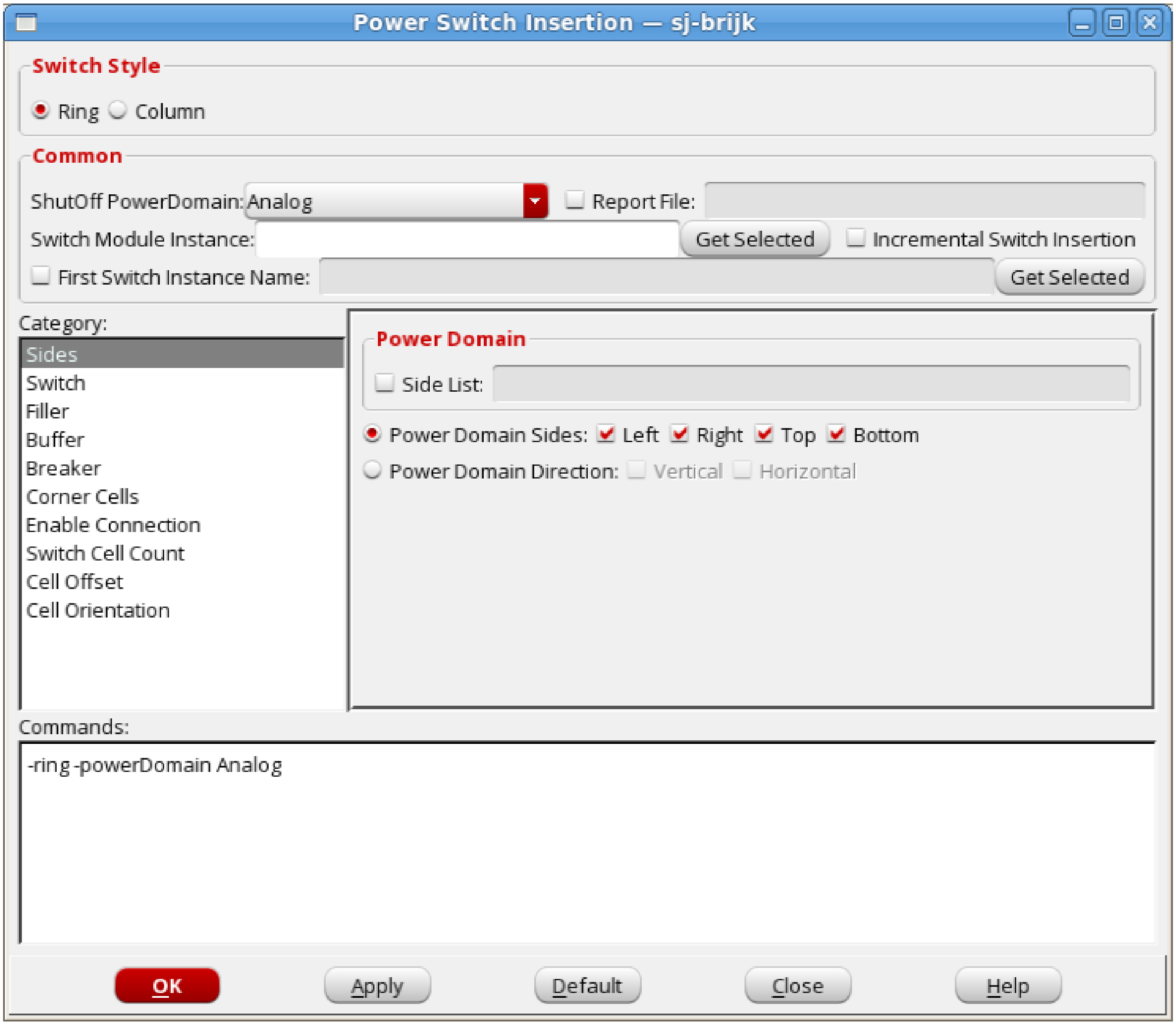
The *Ring* button controls the following pages:

- PSO Ring Sides
- PSO Ring Switch
- PSO Ring Filler
- PSO Ring Buffer
- PSO Ring Breaker
- PSO Ring Corner Cells

- PSO Ring Enable Connection
- PSO Ring Switch Cell Count
- PSO Ring Cell Offset
- PSO Ring Cell Orientation

Power Switch Insertion - Ring - Sides

Use the Power Switch Insertion - Ring form to add a ring of switches around a power domain. The *Sides* option specifies the sides of the power domain on which the switches are placed.
→ To open the Power Switch Insertion - Ring - Sides form, choose *Power* - *Multiple Supply Voltage* - *Add Power Switch*, click on the *Ring* button, and select the *Sides* option from the *Category* panel.



Power Switch Insertion - Ring - Sides Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.

Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Side List	Specifies the sides of a power domain where switches can and cannot be placed. In the list, 1 indicates that the side can contain ring switches, and 0 indicates that the side cannot contain ring switches. The list must contain either 0 or 1 for each side of the shape. The first member of the list indicates the first side relative to Corner 0, which is the lower left corner of the ring. If *Start Placing Cells in Counter-Clockwise Direction* is specified on the *Switch Cell Count* form, the first side is counterclockwise from Corner 0.
Power Domain Sides	Specifies the sides on which switches are placed.
Left	Inserts switches on the left side of the power domain.
Right	Inserts switches on the right side of the power domain.
Top	Inserts switches on the top side of the power domain.
Bottom	Inserts switches on the bottom side of the power domain.
Power Domain Direction	Inserts switches on multiple sides of the same direction. These options are useful for rectilinear power domains.

Vertical	Inserts switches on all vertical sides of the power domain.
Horizontal	Inserts switches on all horizontal sides of the power domain.

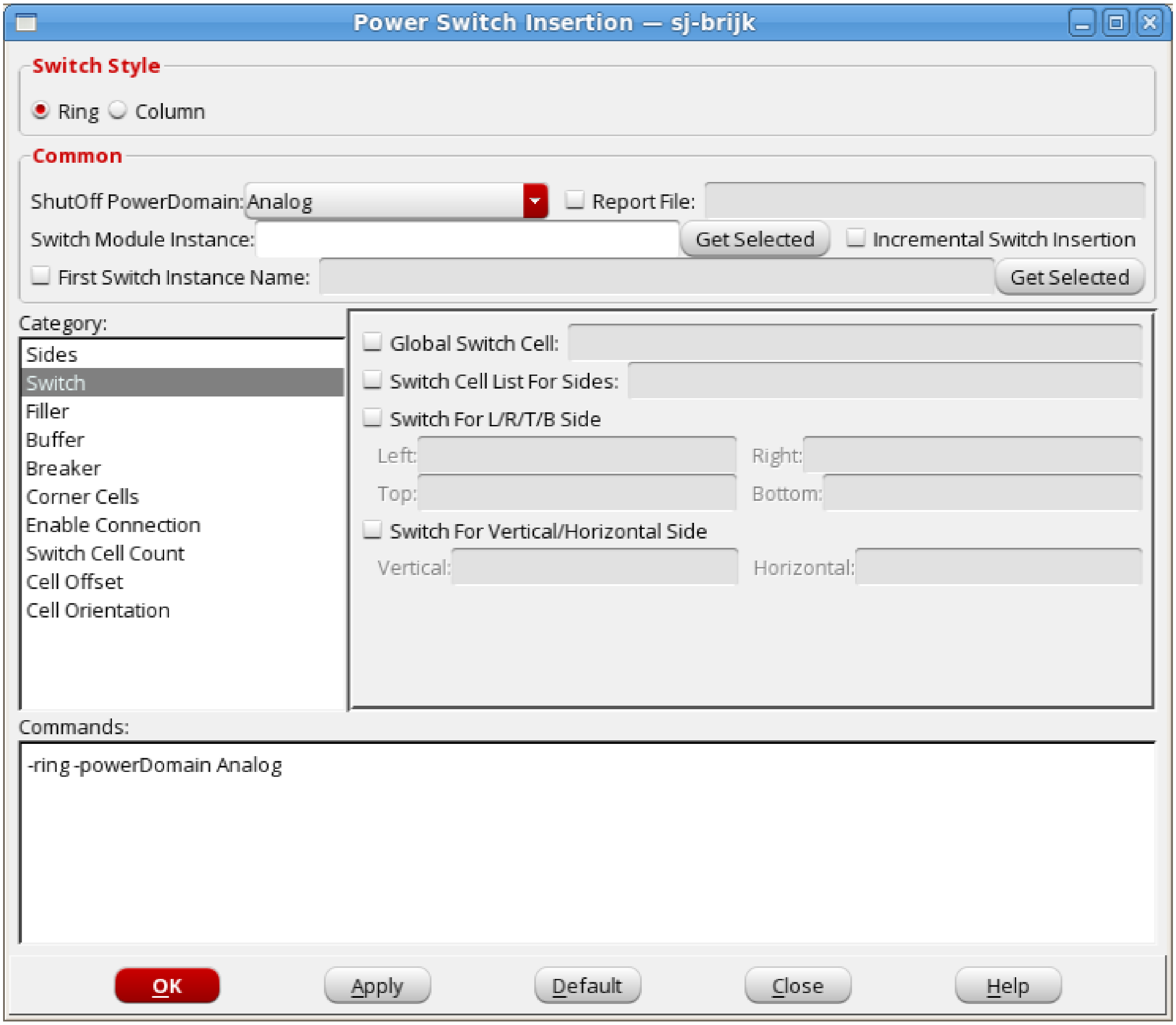
Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion - Ring - Switch

Use the Power Switch Insertion - Ring form to add a ring of switches around a power domain. The *Switch* option specifies switch placement.
→ To open the Power Switch Insertion - Ring form, choose *Power* - *Multiple Supply Voltage* - *Add Power Switch*, click the *Ring* button, then click on *Switch* in the *Category* pane.



Power Switch Insertion - Ring - Switch Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.

Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Global Switch Cell	Specifies the cell name of the switch cell to insert in the power switch ring surrounding the specified power domain.
Switch Cell List for Sides	The number of cells must match the number of sides in the power domain. The software checks that the number of cells you specify is the number you specified with `optPowerSwitch -specifySideList`, and issues an error message if it finds a discrepancy.
Switch Cell List for L/R/T/B Side	
	Lists switch cells for specific sides. You can choose different cells for each side.
Left	Specifies a switch cell for the left side of the power switch ring.
Right	Specifies a switch cell for the right side of the power switch ring.
Top	Specifies a switch cell for the top side of the power switch ring.
Bottom	Specifies a switch cell for the bottom side of the power switch ring.
Switch for Vertical/Horizontal Side	

	Lists switch cells for all horizontal or all vertical sides. You can choose different cells for each side.
Vertical	Specifies a switch cell for the vertical sides of the power switch ring.
Horizontal	Specifies a switch cell for the horizontal sides of the power switch ring.

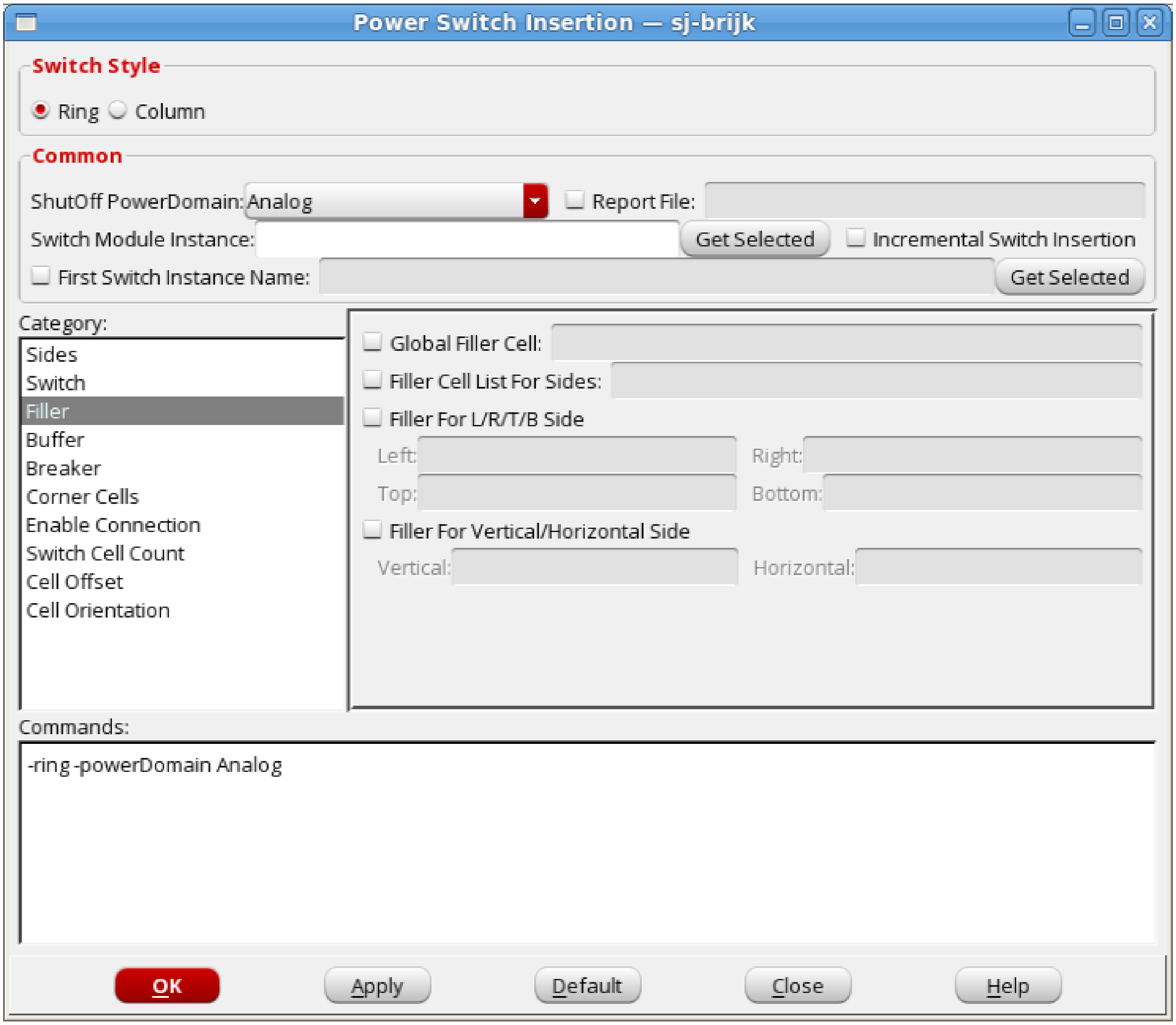
Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion - Ring - Filler

Use the Power Switch Insertion - Ring form to add a ring of switches around a power domain. The *Filler* option specifies filler cell placement.
→ To open the Power Switch Insertion - Ring form, choose *Power* - *Multiple Supply Voltage* - *Add Power Switch*, click the *Ring* button, then click on *Filler* in the *Category* pane.



Power Switch Insertion - Ring - Filler Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.

Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Global Filler Cell	Specifies the cell name of the filler cell to insert in the power switch ring surrounding the specified power domain.
Filler Cell List for Sides	Specifies the filler cell to use for all sides.
Filler Cell List for L/R/T/B Side	
	Lists filler cells for specific sides. You can choose different cells for each side.
Left	Specifies a filler cell for the left side of the power switch ring.
Right	Specifies a filler cell for the right side of the power switch ring.
Top	Specifies a filler cell for the top side of the power switch ring.
Bottom	Specifies a filler cell for the bottom side of the power switch ring.
Filler for Vertical/Horizontal Side	
	Lists filler cells for all horizontal or all vertical sides. You can choose different cells for each side.

Vertical	Specifies a filler cell for the vertical sides of the power switch ring.
Horizontal	Specifies a filler cell for the horizontal sides of the power switch ring.

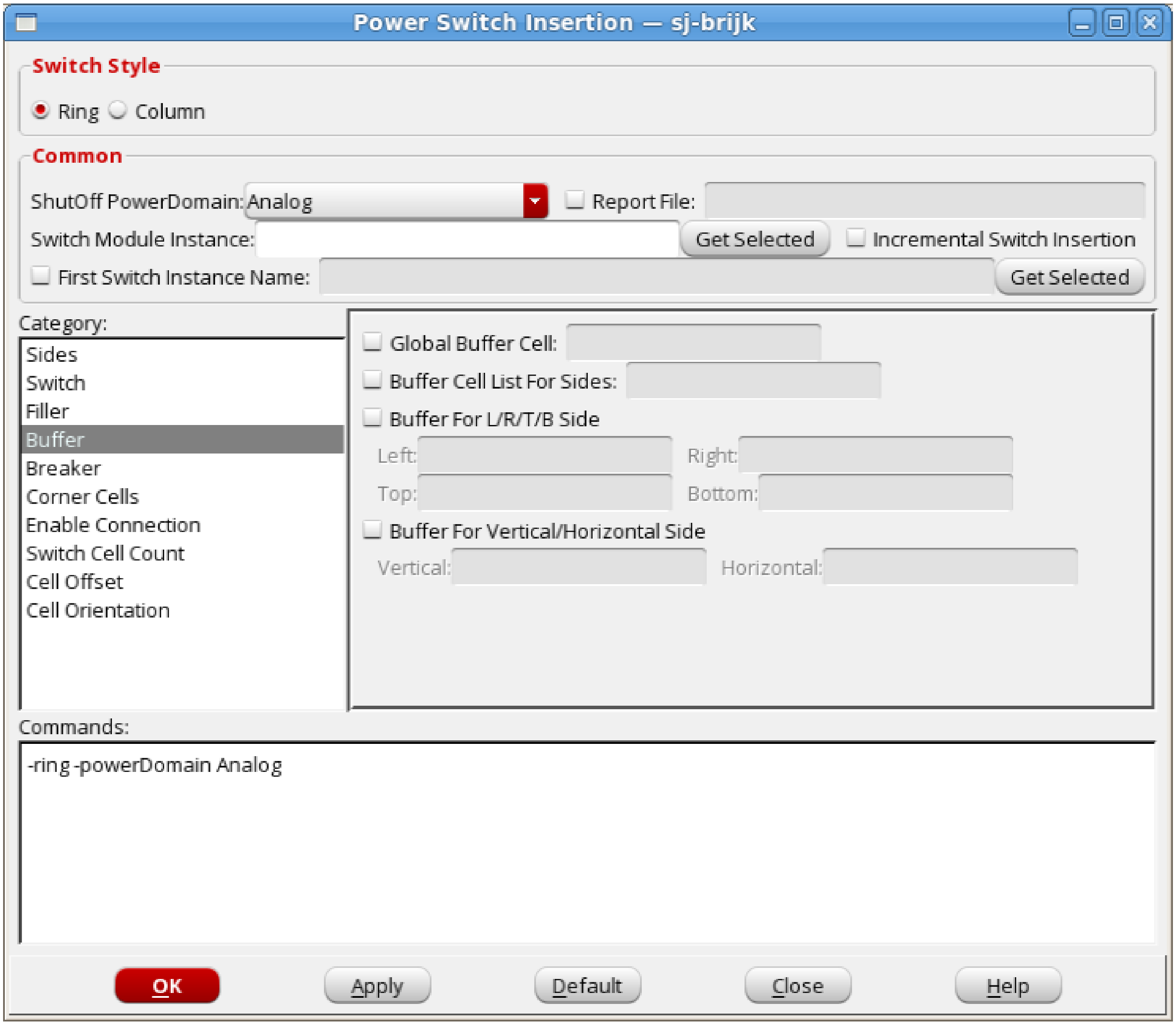
Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion - Ring - Buffer

Use the Power Switch Insertion - Ring form to add a ring of switches around a power domain. The *Buffer* option specifies buffer cell placement.
→ To open the Power Switch Insertion - Ring form, choose *Power* - *Multiple Supply Voltage* - *Add Power Switch*, click the *Ring* button, then click on *Buffer* in the *Category* pane.



Power Switch Insertion - Ring - Buffer Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.

Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Global Buffer Cell	Specifies the cell name of the buffer cell to insert in the power switch ring surrounding the specified power domain.
Buffer Cell List for Sides	Specifies the buffer switch cell to use for all sides.
Buffer Cell List for L/R/T/B Side	
	Lists buffer cells for specific sides. You can choose different cells for each side.
Left	Specifies a buffer cell for the left side of the power switch ring.
Right	Specifies a buffer cell for the right side of the power switch ring.
Top	Specifies a buffer cell for the top side of the power switch ring.
Bottom	Specifies a buffer cell for the bottom side of the power switch ring.
Buffer for Vertical/Horizontal Side	
	Lists buffer cells for all horizontal or all vertical sides. You can choose different cells for each side.

Vertical	Specifies a buffer cell for the vertical sides of the power switch ring.
Horizontal	Specifies a buffer cell for the horizontal sides of the power switch ring.

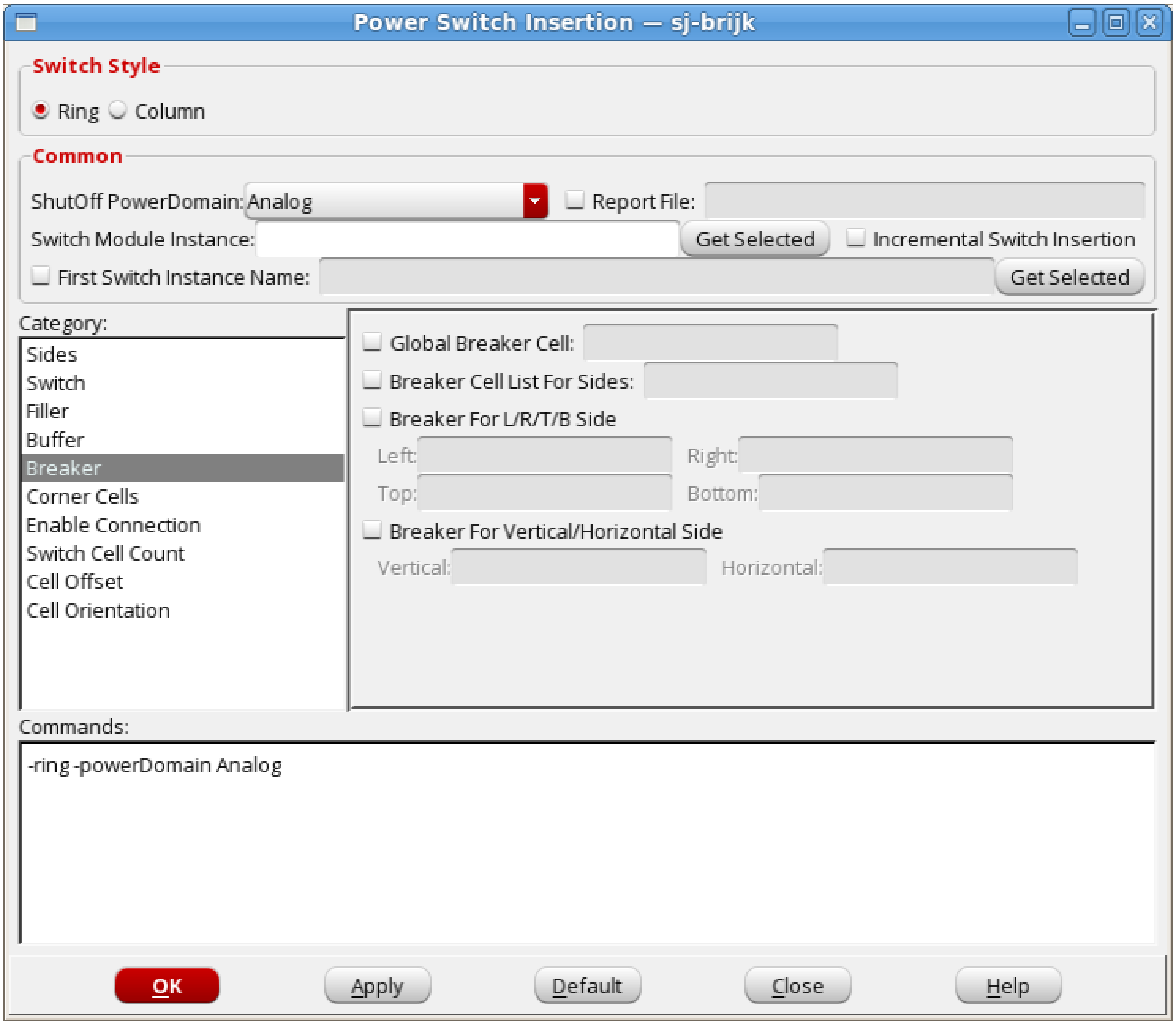
Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion - Ring - Breaker

Use the Power Switch Insertion - Ring form to add a ring of switches around a power domain. The *Breaker* option specifies breaker cell placement.
→ To open the Power Switch Insertion - Ring form, choose *Power* - *Multiple Supply Voltage* - *Add Power Switch*, click the *Ring* button, then click on *Breaker* in the *Category* pane.



Power Switch Insertion - Ring - Breaker Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.

Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Global Breaker Cell	Specifies the cell name of the breaker cell to insert in the power switch ring surrounding the specified power domain.
Breaker Cell List for Sides	Specifies the breaker cell to use for all sides.
Breaker Cell List for L/R/T/B Side	
	Lists cells for specific sides. You can choose different cells for each side.
Left	Specifies a breaker cell for the left side of the power switch ring.
Right	Specifies a breaker cell for the right side of the power switch ring.
Top	Specifies a breaker cell for the top side of the power switch ring.
Bottom	Specifies a breaker cell for the bottom side of the power switch ring.
Breaker for Vertical/Horizontal Side	
	Lists breaker cells for all horizontal or all vertical sides. You can choose different cells for each side.
Vertical	Specifies a breaker cell for the vertical sides of the power switch ring.

Horizontal	Specifies a breaker cell for the horizontal sides of the power switch ring.

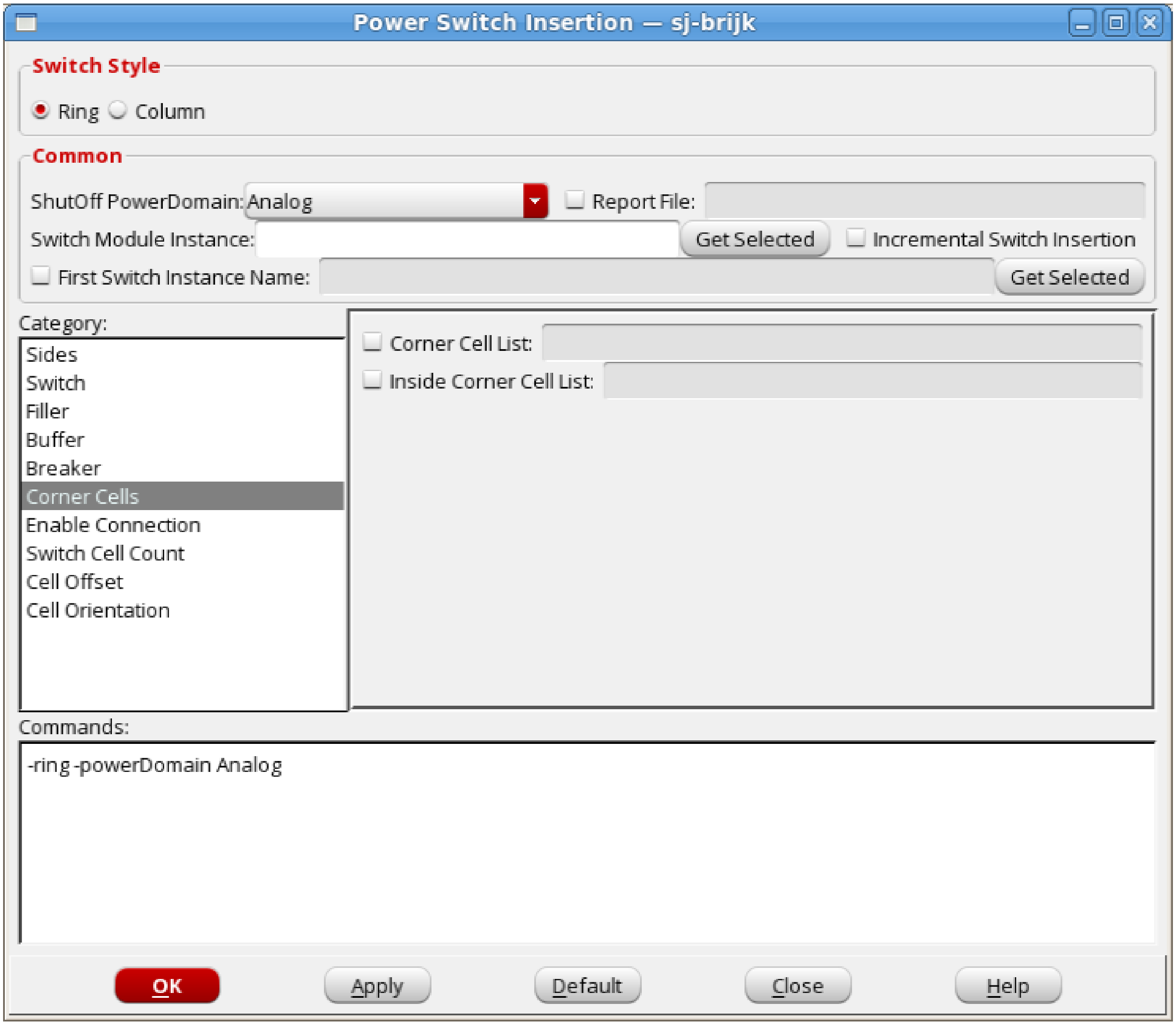
Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion - Ring - Corner Cells

Use the Power Switch Insertion - Ring form to add a ring of switches around a power domain. The *Corner Cells* option specifies which corner cells to use.
→ To open the Power Switch Insertion - Ring form, choose *Power* - *Multiple Supply Voltage* - *Add Power Switch*, click the *Ring* button, then click on *Corner Cells* in the *Category* pane.



Power Switch Insertion - Ring - Corner Cells Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.

Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
Corner Cell List	Specifies the list of available corner cells that can be used by the tool to fill the corners of the ring. If you specify only one corner cell, that same cell is used on all four corners with the appropriate orientation.
Inside Corner Cell List	Specifies a list of cells for the tool to choose for the inside corners of the ring. You do not need to list a specific cell for a specific corner. The tool selects from the list you provide.

Related Text Commands

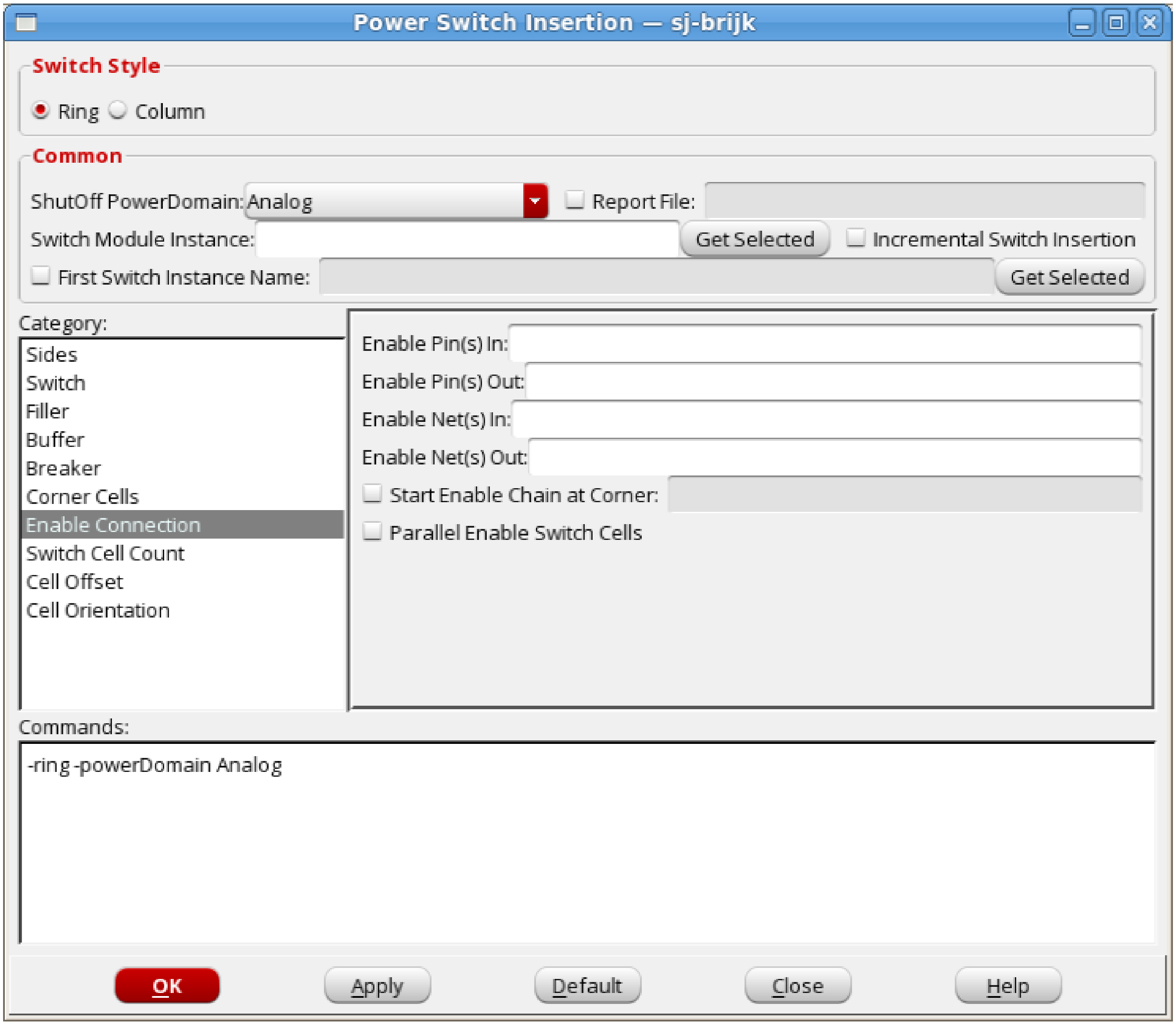
For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion - Ring - Enable Connection

Use the Power Switch Insertion - Ring form to add a ring of switches around a power domain. The *Enable Connection* option specifies the enable pins and nets to use, and the enable connection style.

→ To open the Power Switch Insertion - Ring form, choose *Power - Multiple Supply Voltage - Add Power Switch*, click the *Ring* button, then click on *Enable Connection* in the *Category* pane.



Power Switch Insertion - Ring - Enable Connection Fields and Options

Switch Style	Specifies how the switches are arranged.

Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Enable Pin(s) In	Specifies the list of enable input pins of the buffers inside the switch cell. The order in which you specify these pins is important because nets are assigned to pins sequentially. The software ties the Enable Pin Out of the first switch cell to the Enable Pin In of the next switch cell in the same ring: All the enable pin of the switch cells in the same column are daisy-chained together. For the first switch of the ring, the Enable Pin In is tied to Enable Net In.
Enable Pin(s) Out	Specifies the list of enable output pin(s) of the buffer(s) inside the switch cell. The order in which you specify these pins is important because nets are assigned to pins sequentially. The software ties the Enable Pin Out of the first switch cell to the Enable Pin In of the next switch cell in the same column: all the enable pin of the switch cells in the same column are daisy-chained together. For the last switch of the column, the Enable Pin Out is tied to Enable Net Out.

Enable Net(s) In	Specifies the list of input nets that the software attaches to the enable input pins. The order in which you specify these nets is important because nets are assigned to pins sequentially.
Enable Net(s) Out	Specifies the enable output nets that the software attaches to the enable output pins. The order in which you specify these nets is important because nets are assigned to pins sequentially. For the last switch of the ring, the Enable Pin Out is tied to the Enable Pin Out.
Start Enable Chain at Corner	
	Specifies the corner where the switch ring insertion begins. The software inserts switches starting from the specified corner and continuing in a clockwise direction (unless *Start Placing Cells in the Counter-Clockwise Direction* is specified on the *Switch Cell Count* form) until it completes the full ring.
Parallel Enable Switch Cells	
	Connects a power switch's input pin in parallel style rather than daisy-chaining. You do not have to specify *Enable Pin(s) Out* or *Enable Net(s) Out*.

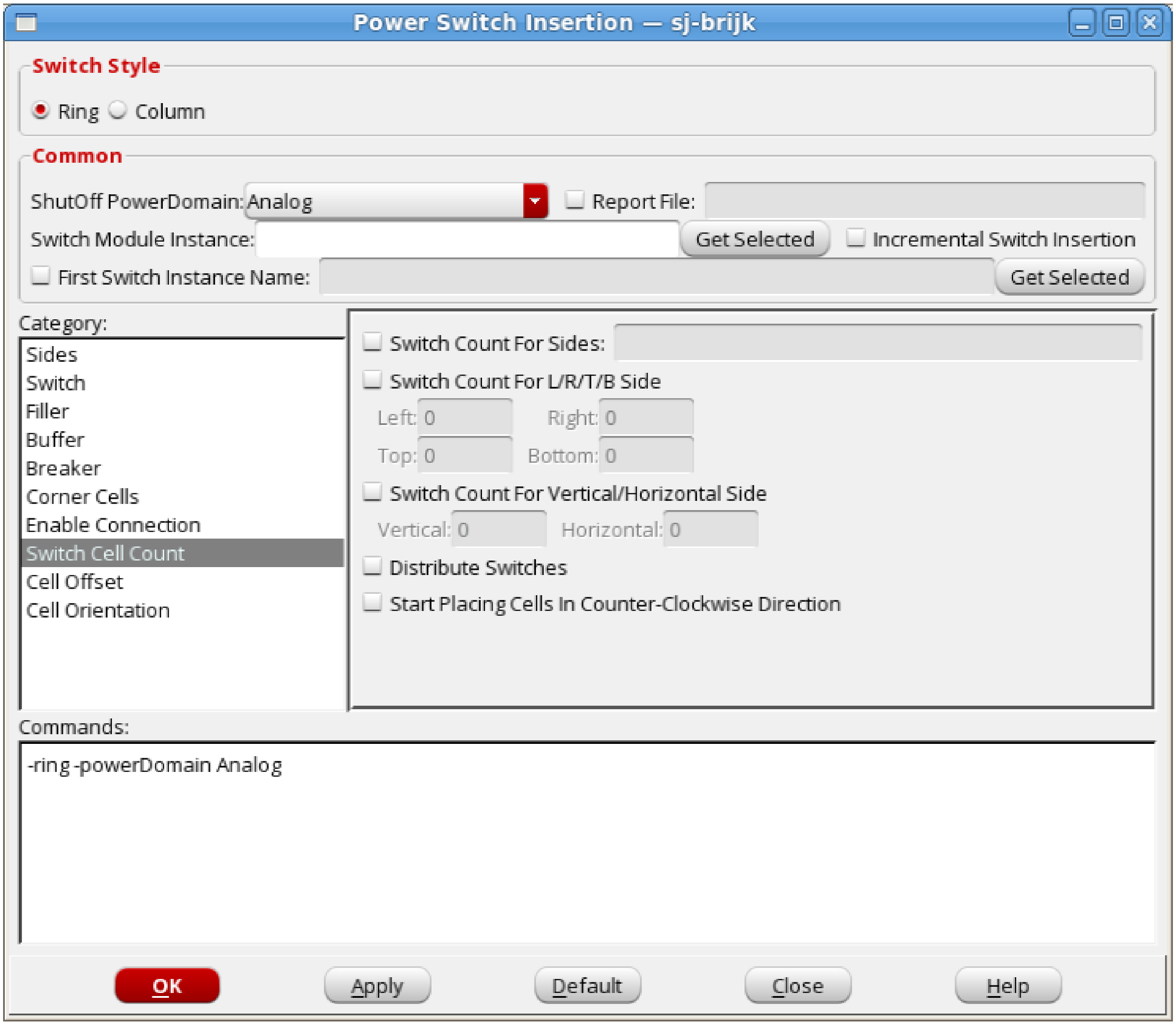
Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion - Ring - Switch Cell Count

Use the Power Switch Insertion - Ring form to add a ring of switches around a power domain. The *Switch Cell Count* option specifies the number of switches to use.
→ To open the Power Switch Insertion - Ring form, choose *Power* - *Multiple Supply Voltage* - *Add Power Switch*, click the *Ring* button, then click on *Switch Cell Count* in the *Category* pane.



Power Switch Insertion - Ring - Switch Cell Count Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.

Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Switch Cell Count for Sides	
	Lists the number of switches to insert on each side. Each value in the list corresponds to a side specified with *Side List* in on the *Sides* form.
Switch Cell Count for L/R/T/B Side	
	Specifies the cell count for each side. **Note:** This parameter applies to power switch ring creation only. Three scenarios can occur: • If the spaces available match the number specified, the software fills these spaces with switches. • If the number exceeds the spaces available, the software issues an error message. If the number is less than the spaces available, the tool inserts the switches, then inserts filler cells to fill the space.
Left	Specifies the number of switches to insert on the left side of the power domain.

Right	Specifies the number of switches to insert on the right side of the power domain.
Top	Specifies the number of switches to insert on the Top side of the power domain.
Bottom	Specifies the number of switches to insert on the bottom side of the power domain.
Switch Count for Vertical/Horizontal Side	
	Specifies the cell count for each horizontal and/or vertical side. **Note:** This parameter applies to power switch ring creation only. Three scenarios can occur: • If the spaces available match the number specified, the software fills these spaces with switches. • If the number exceeds the spaces available, the software issues an error message. If the number is less than the spaces available, the tool inserts the switches, then inserts filler cells to fill the space.
Vertical	Specifies the number of switches to insert on all vertical side(s) of the power domain.
Horizontal	Specifies the number of switches to insert on all horizontal side(s) of the power domain.
Distribute Switches	Distributes switches of different types as evenly as possible on a ring side. For example, if there are 40 available slots, and there are 20 switches and 20 fillers, the software will alternate switches and fillers in the available slots.
Start Placing Switches in the Counter-Clockwise Direction	
	Places the cell pattern in a counter-clockwise direction in a switch ring. Switch placement begins at the lower left corner of the ring.

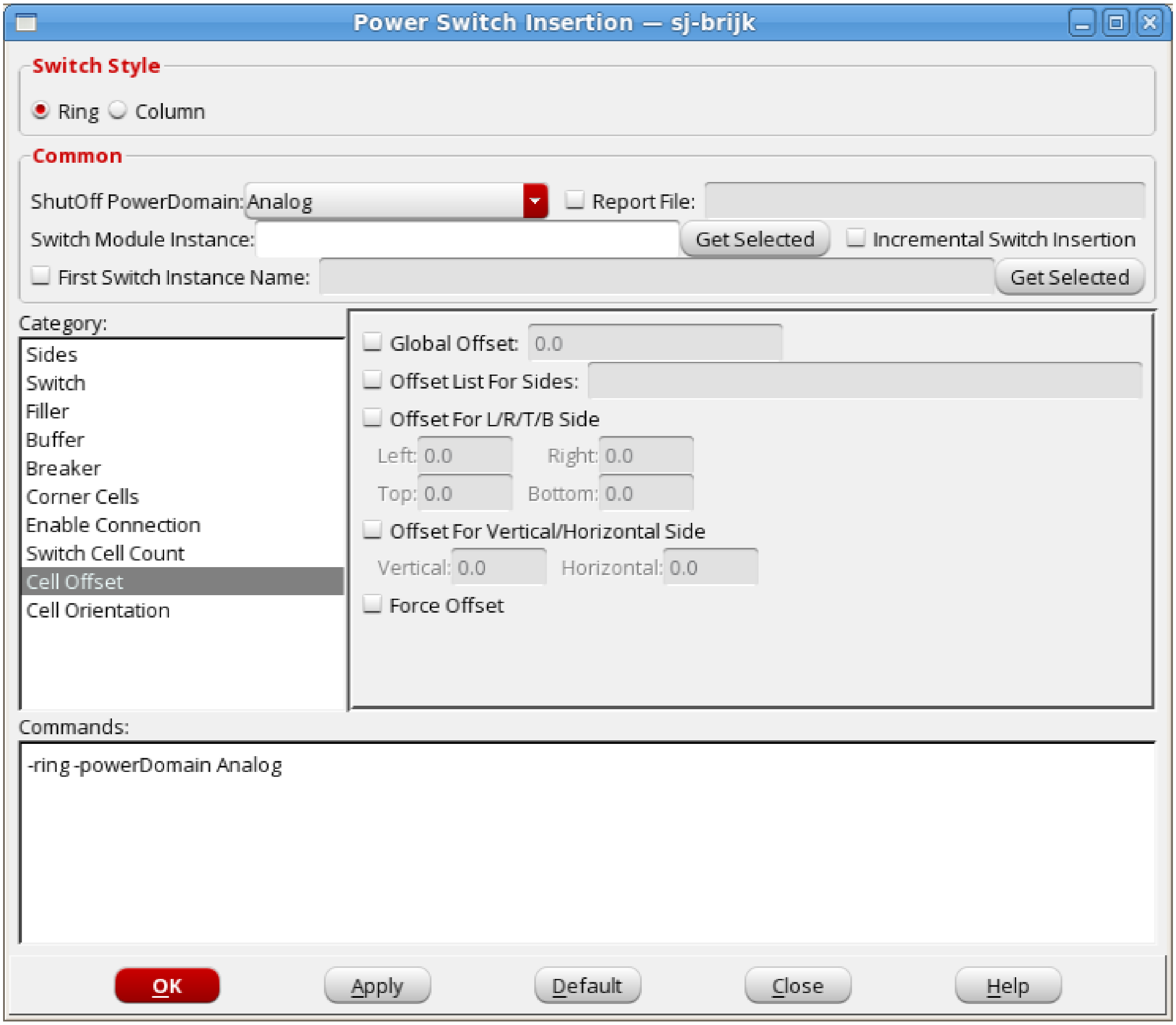
Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion - Ring - Cell Offset

Use the Power Switch Insertion - Ring form to add a ring of switches around a power domain. The *Cell Offset* option specifies the offsets to use.
→ To open the Power Switch Insertion - Ring form, choose *Power* - *Multiple Supply Voltage* - *Add Power Switch*, click the *Ring* button, then click on *Cell Offset* in the *Category* pane.



Power Switch Insertion - Ring - Cell Offset Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.

Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Global Offset	Offsets all sides of the power switch ring the specified distance from the power domain. Specify the offset in µm. **Note:** If you do not specify a global offset, or offset for any sides, the tool places switches with `0` offset.

Offset List For Sides	Lists the offset values representing the distance between the power domain fence boundary and each side of the power switch ring. Each value in the list corresponds to a side specified with the *Side List* on the *Sides* form. **Note:** When you create a power domain, a `minGap` exists for this power domain, and the switches are inserted within this `minGap`. However, if the specified `minGap` is less than the switch dimension, then the tool automatically adds filler cells and assigns a new `minGap` for this power domain. **Important:** You *must* specify a valid cell name for each side, even if no cells can be specified for a side. The tools checks that the number of cells you specify is the same number you specified with the *Side List* on the *Sides* form, and issues an error message if it finds a discrepancy.
Offset For L/R/T/B Sides	
	Specifies the distance between the power domain boundary and the nearest switch cell on the specified side(s).
Left	Specifies the distance between the left power domain boundary and the nearest switch cell.
Right	Specifies the distance between the right power domain boundary and the nearest switch cell. T
Top	Specifies the distance between the top power domain boundary and the nearest switch cell.
Bottom	Specifies the distance between the bottom power domain boundary and the nearest switch cell.
Offset For Vertical/Horizontal Side	
	Specifies the distance between the power domain boundary and the nearest switch cell on the specified horizontal and vertical sides.

Vertical	Offsets the switch ring from the vertical edges of the power domain. Specify the offset in µm.
Horizontal	Offsets the switch ring from the horizontal edges of the power domain. Specify the offset in µm.
Force Offset	Forces the software to place ring switches at the exact offset you specify for all sides. Sides with unspecified offsets are forces to 0.0 µ. When you specify any other offset without specifying *Force Offset*, the tool places switches at the smallest distance that is greater than or equal to the specified offset for each side, in order to maintain a contiguous ring.

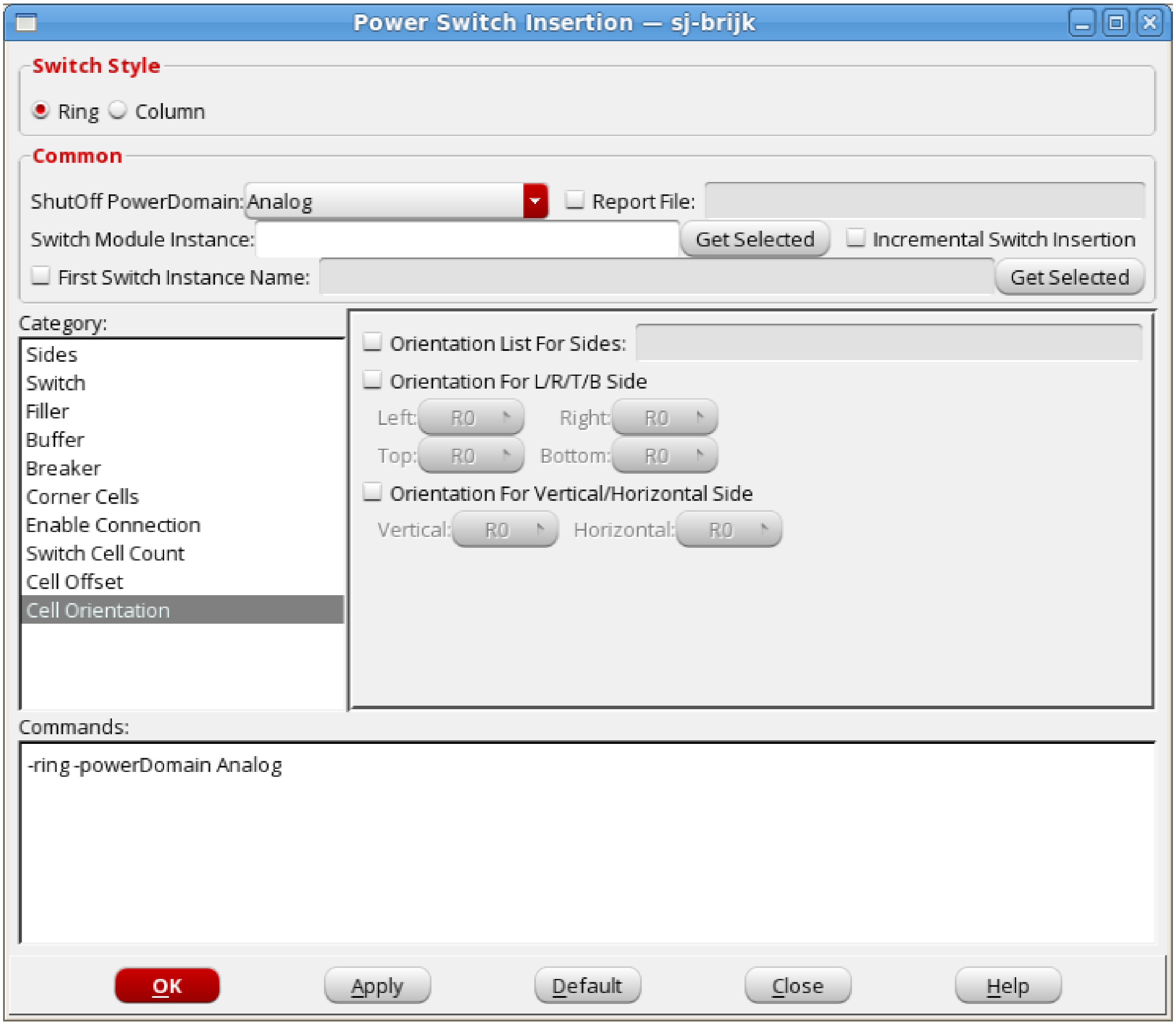
Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion - Ring - Cell Orientation

Use the Power Switch Insertion - Ring form to add a ring of switches around a power domain. The *Cell Orientation* option specifies the orientation for ring sides.
→ To open the Power Switch Insertion - Ring form, choose *Power* - *Multiple Supply Voltage* - *Add Power Switch*, click the *Ring* button, then click on *Cell Orientation* in the *Category* pane.



Power Switch Insertion - Ring - Cell Orientation Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.

Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Orientation List For Sides	
	Lists the orientations for cells for each side of the power switch ring. Each orientation in the list corresponds to a side specified, so you must have already specified sides. Use the following notation for orientation: `R0|R90|R180|R270|MX|MY|MX90|MY90`
Orientation for L/R/T/B Side	
	Specifies the orientation for specific sides.
Left	Specifies the cell orientation for the left side of the power switch ring.
Right	Specifies the cell orientation for the right side of the power switch ring.
Top	Specifies the cell orientation for the top side of the power switch ring.
Bottom	Specifies the cell orientation for the bottom side of the power switch ring.
Orientation for Vertical/Horizontal Side	
	Specifies the cell orientation for vertical and horizontal sides.

Vertical	Specifies the cell orientation for vertical sides.
Horizontal	Specifies the cell orientation for horizontal sides.

Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

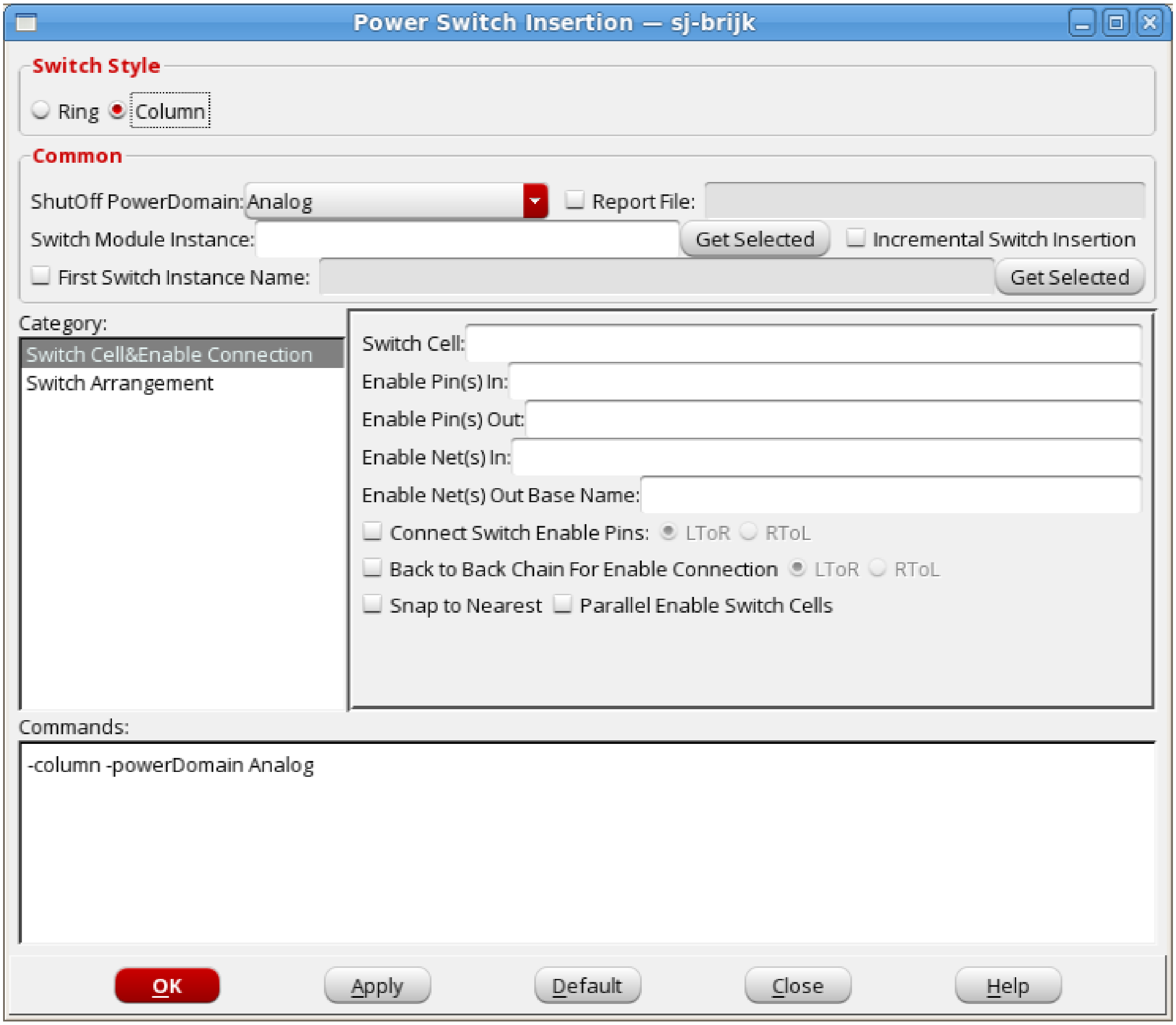
Power Switch Insertion - Column

The *Column* button controls the following pages:

- PSOColumnSwitchArrangement

Power Switch Insertion - Column - Switch Cell and Enable Connection

Use the Power Switch Insertion - Column form to add a ring of switches around a power domain. The *Switch Cell and Enable Connection* option specifies which switch an enable usage.
→ To open the Power Switch Insertion - Column form, choose *Power - Multiple Supply Voltage - Add Power Switch*, click the *Column* button. The *Switch Cell and Enable Connection* option in the *Category* pane is selected by default.



Power Switch Insertion - Column - Switch Cell and Enable Connections Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.

Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Switch Cell	Specifies the cell name of the switch to insert in the specified power domain.
Enable Pin(s) In	Specifies the list of enable input pins of the buffers inside the switch cell. The order in which you specify these pins is important because nets are assigned to pins sequentially. The software ties the Enable Pin Out of the first switch cell to the Enable Pin In of the next switch cell in the same column: All the enable pin of the switch cells in the same column are daisy-chained together. For the last switch of the column, the Enable Pin Out is tied to Enable Net Out.
Enable Pin(s) Out	Specifies the list of enable output pin(s) of the buffer(s) inside the switch cell. The order in which you specify these pins is important because nets are assigned to pins sequentially. The software ties the Enable Pin Out of the first switch cell to the Enable Pin In of the next switch cell in the same column: all the enable pin of the switch cells in the same column are daisy-chained together. For the last switch of the column, the Enable Pin Out is tied to Enable Net Out.
Enable Net(s) In:	Specifies the list of input nets that the software attaches to the enable input pins. The order in which you specify these pins is important because nets are assigned to pins sequentially.

Enable Net Out Base Name	
	Specifies the base name for the Enable Out Nets.
Connect Switch Enable Pins	
	Connects the first switch of the first column to the enable net specified. The software connects the first switch in the remaining columns to the output enable net of the first switch in the previous column. For more information, see the `-connectBottomSwitchEnablePins` option of the `addPowerSwitch` command in the "Low Power Commands" chapter of *Text Command Reference*.
L To R	Connects switches left-to-right.
R To L	Connects switches right-to-left.
Back to Back Chain for Enable Connection	
	Connect the Enable Net Out at the top of a column to the Enable Net In at the top of the next column, and connects the Enable Net In at the bottom of a column to the Enable Net In at the bottom of the next column. By default, the Enable Net In is connected to the bottom of each column, and the Enable Net Out exits from the top of each column, in parallel.
Snap to Nearest	Snaps the cell placement to the nearest legal location. This parameter can be used when a hard macro blocks part of a column. The switches that would overlap the hard macro blockage are placed at legal locations nearest to the expected original location.
Parallel Enable Switch Cells	
	Connects a power switch's input pin in parallel style rather than daisy-chaining. You do not have to specify *Enable Pin(s) Out* or *Enable Net(s) Out*.

Related Text Commands

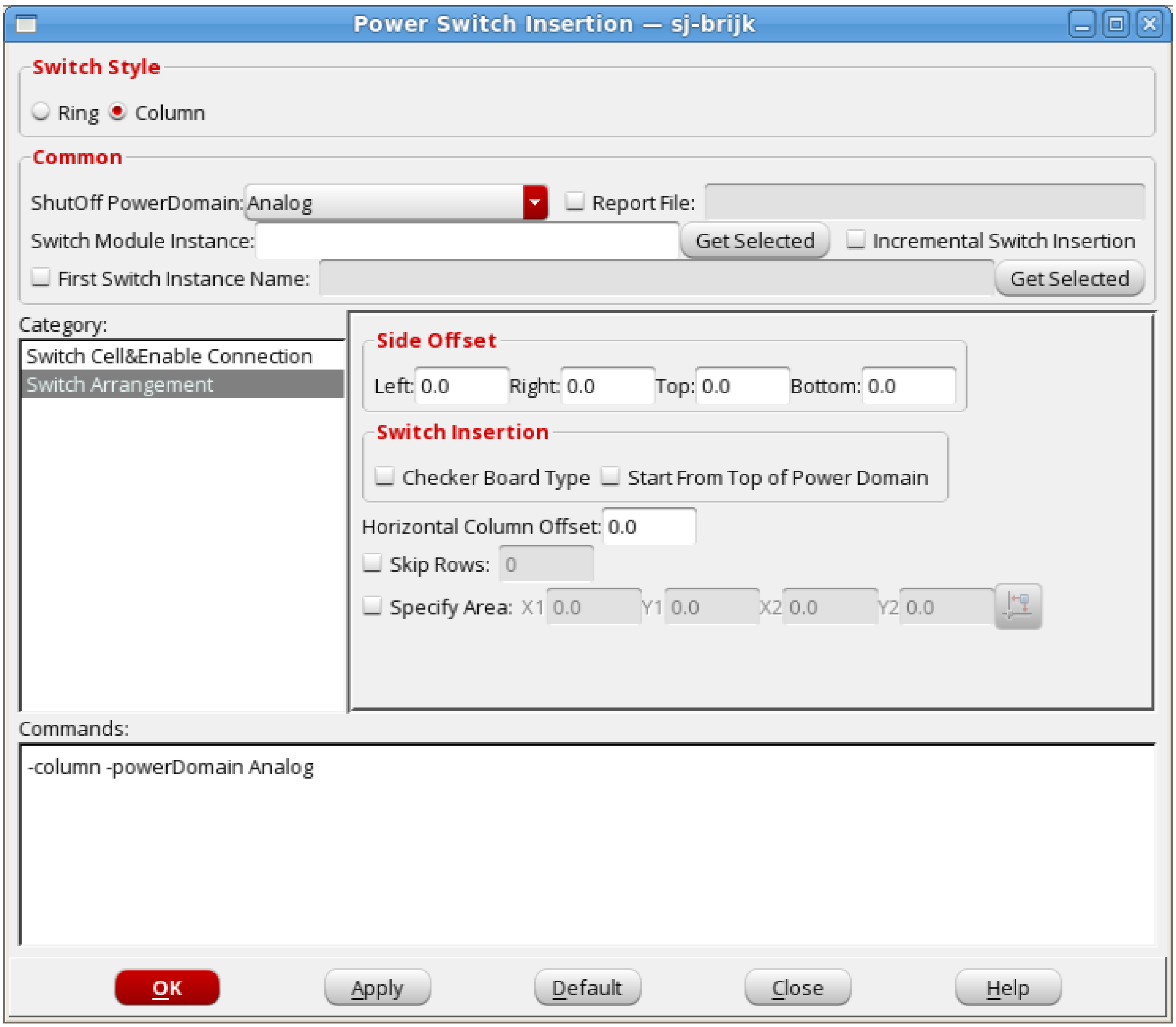
For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion - Column - Switch Arrangement

Use the Power Switch Insertion - Column form to add a switch columns for a power domain. The *Switch Arrangement* option specifies how switches are arranged.

→ To open the Power Switch Insertion - Column form, choose *Power* - *Multiple Supply Voltage* - *Add Power Switch*, click the *Column* button, then click on *Switch Arrangement* in the *Category* pane.



Power Switch Insertion - Column - Switch Arrangement Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Side Offset	Specifies the distance between the power domain boundaries and the nearest switch cell.
Left	Specifies the distance between the left power domain boundary and the nearest switch cell.
Right	Specifies the distance between the right power domain boundary and the nearest switch cell.
Top	Specifies the distance between the top power domain boundary and the nearest switch cell.

Bottom	Specifies the distance between the bottom power domain boundary and the nearest switch cell.
Checker Board Type	Arranges switch cells in a checkerboard pattern within a power domain.
Start From Top of Power Domain	Adds switches from the top down rather than from the bottom up.
Horizontal Column Offset	Specifies the distance between switch columns in µm. This parameter is required.
Skip Rows	Specifies the number of rows to skip when placing a switch in a column. For example, `2` skips two rows before placing the next switch in a column.
Specify Area	Defines an area within a power domain where the tool can insert power switches. *x1 y1* is the lower left coordinate of the area. *x2 y2* is the upper right corner of the area. You can specify left, right, top, and/or bottom offsets to offset the switches from the boundaries of the area.

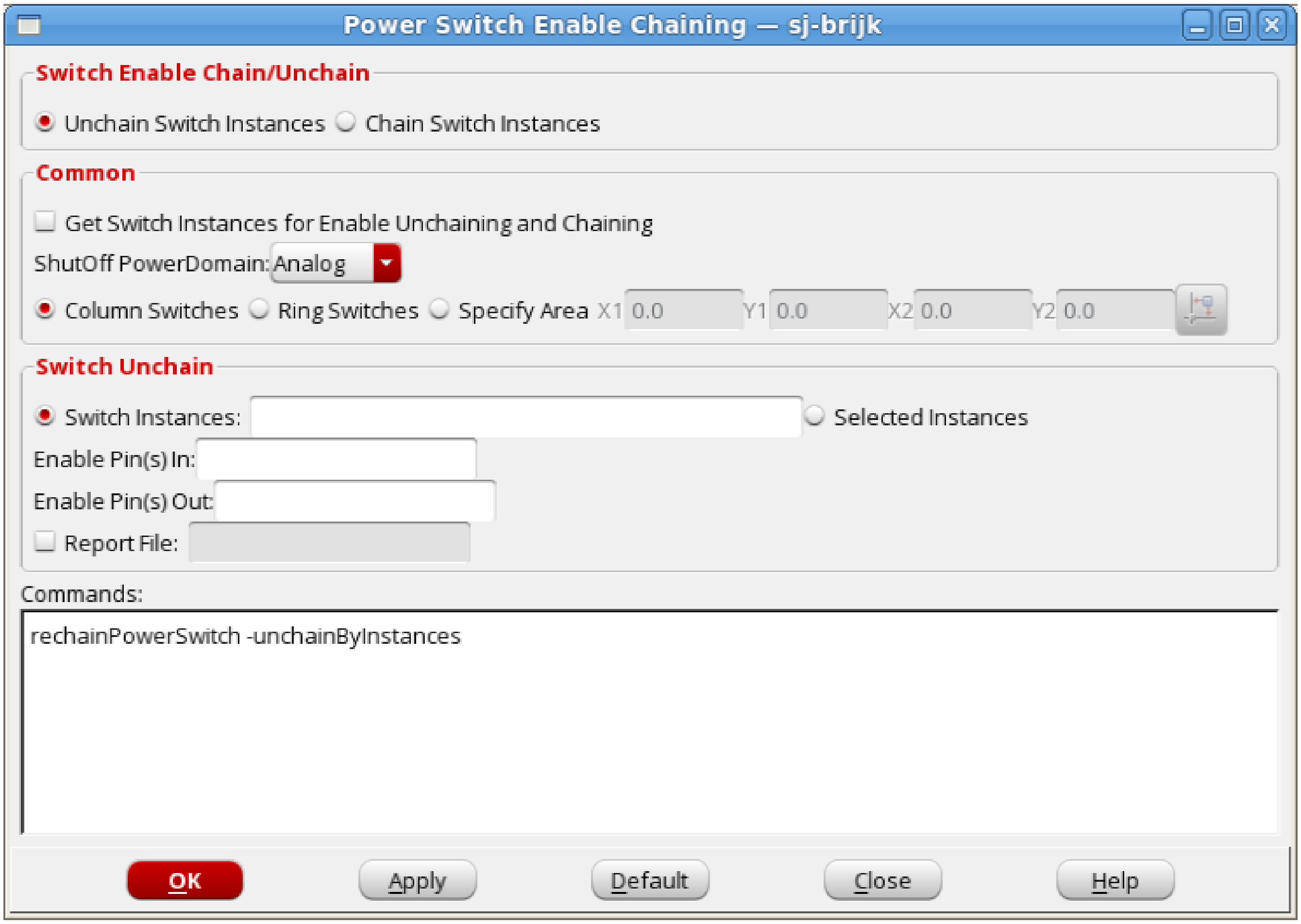
Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

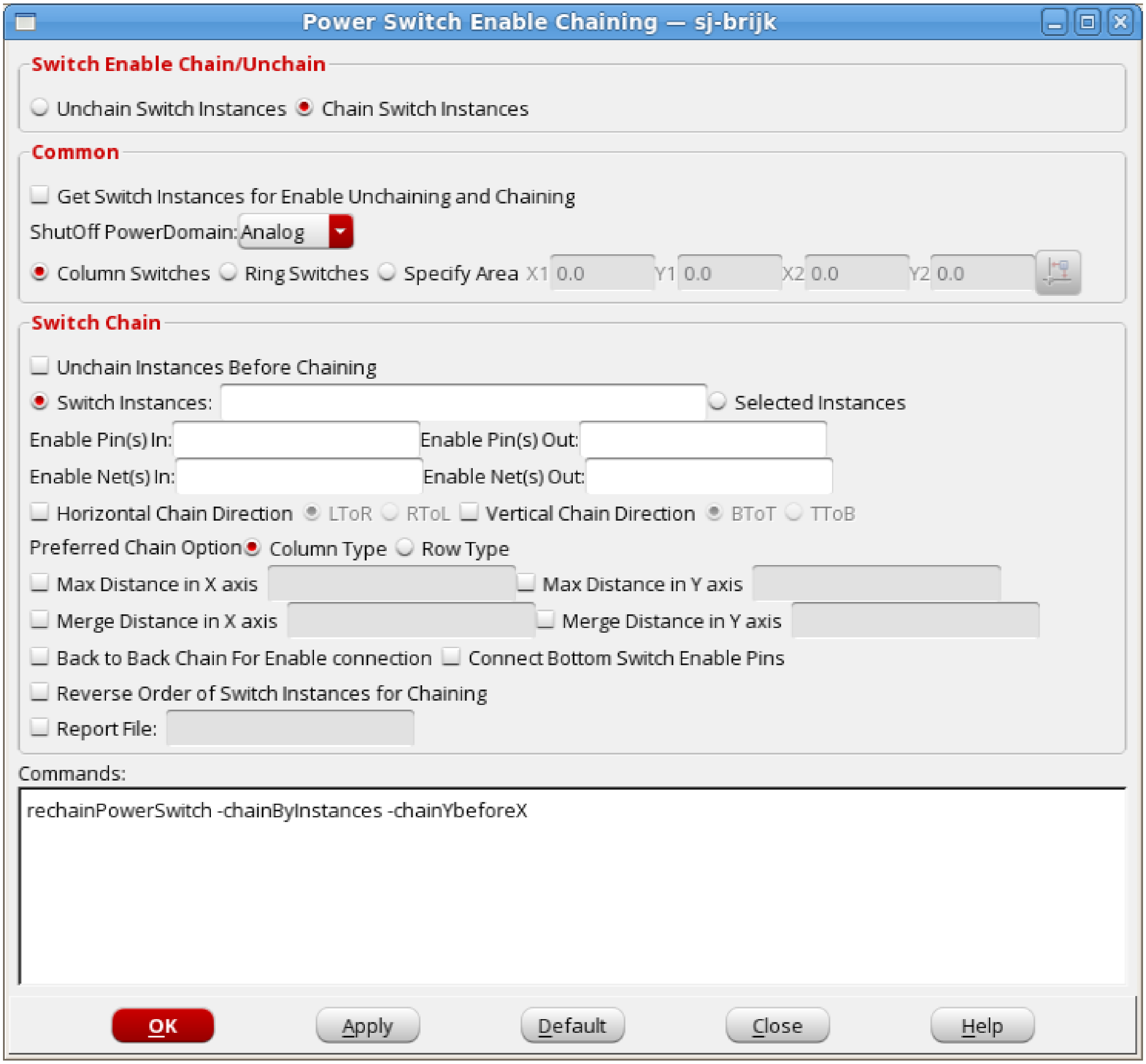
- `addPowerSwitch`

Chain/Unchain Power Switch Enable

Use the Chain/Unchain Power Switch Enabled form for adding flexible chaining options.
→ To open the Power Switch Enabled form, choose *Power* - *Multiple Supply Voltage* - *Chain/Unchain Power Switch Enable* - *Unchain Switch Instances*.



→ To open the Power Switch Enabled form for Chain Switch Instances click the relevant radio button, choose *Power - Multiple Supply Voltage - Chain/Unchain Power Switch Enable - Chain Switch Instances*.



Chain/Unchain Power Switch Enable - Fields and Options

Switch Enable Chain/Unchain	
Unchain Switch Instances	
	Select to unchain switch instances.

Chain Switch Instances	Select to chain switch instances.
Common	
Get Switch Options to Enable Unchaining and Chaining	
	Select to get switch options to enable chaining and unchaining.
ShutOff Power Domain	Select Power domains to switch off.
Column Switches	Select to choose column switches.
Ring Switches	Select to choose ring switches.
Specify Area	Specify are in the fields.
Switch Unchain	
Switch Instances	Select to switch instances.
Selected Instances	Select to choose selected instances.
Enable Pin(s) In	Enter to enable in pin(s).
Enable Pin(s) Out	Enter to enable out pin(s).
Report File	Select to choose the report file.
Commands	Enter commands in this field.
Switch Chain	
Unchain Instances Before Chaining	
	Select to unchain instances before chaining them.
Switch Instances	Select and enter instances to switch.
Enables Pin(s) In/Out	Enter In and Out Pins.
Enables Net(s) In/Out	Enter In and Out Nets.

Horizontal Chain Direction	
	Click to select the horizontal chain direction Left to Right or Right to Left.
Vertical Chain Direction	
	Click to select the vertical chain direction Bottom to Top or Top to Bottom.
Preferred Chain Option	
	Select preferred option: column or ring
Max Distance	Select and enter maximum distance in X or Y axis.
Merge Distance	Select and enter merge distance in X or Y axis.
Back to Back Chain for Enable Connection	
	Select for back to back chains
Connect Bottom Switch Enable Pins	
	Select for bottom switch pins
Reverse Order of Switch Instances for Chaining	
	Select to reverse order of instances
Report File	Select to generate report file
Commands	Enter commands in this field.

Related Text Commands

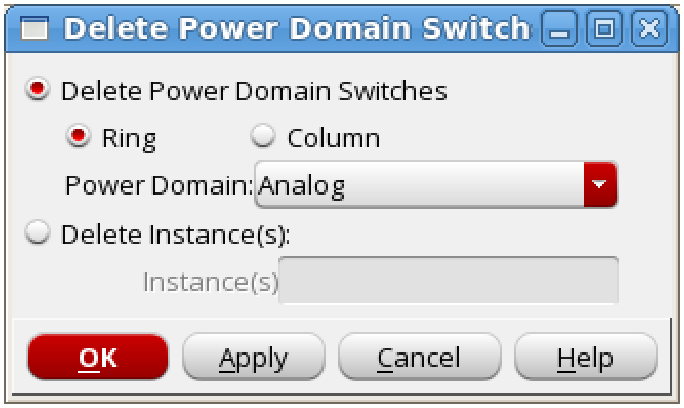
For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- `addPowerSwitch`

Delete Power Switches

Use the Delete Power Switches form to remove power switches from multiple power domain designs.

→ To open the Delete Power Switches form, choose *Power - Multiple Supply Voltage - Delete Power Switch*.



Delete Power Switches Fields and Options

Delete Power Domain Switches	
	Removes switches from rings or columns.
Ring	Removes all switches and filler cells that were inserted by the *Power Switch Insertion* (`addPowerSwitch`) command, from the switch ring for the specified power domain.
Column	Removes all switches and filler cells that were inserted by the *Power Switch Insertion* (`addPowerSwitch`) command, from the switch columns for the specified power domain.
Power Domain	Specifies the power domain.
Delete Instances	Specifies the power switch cell instances to delete.

Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

- deletePowerSwitch

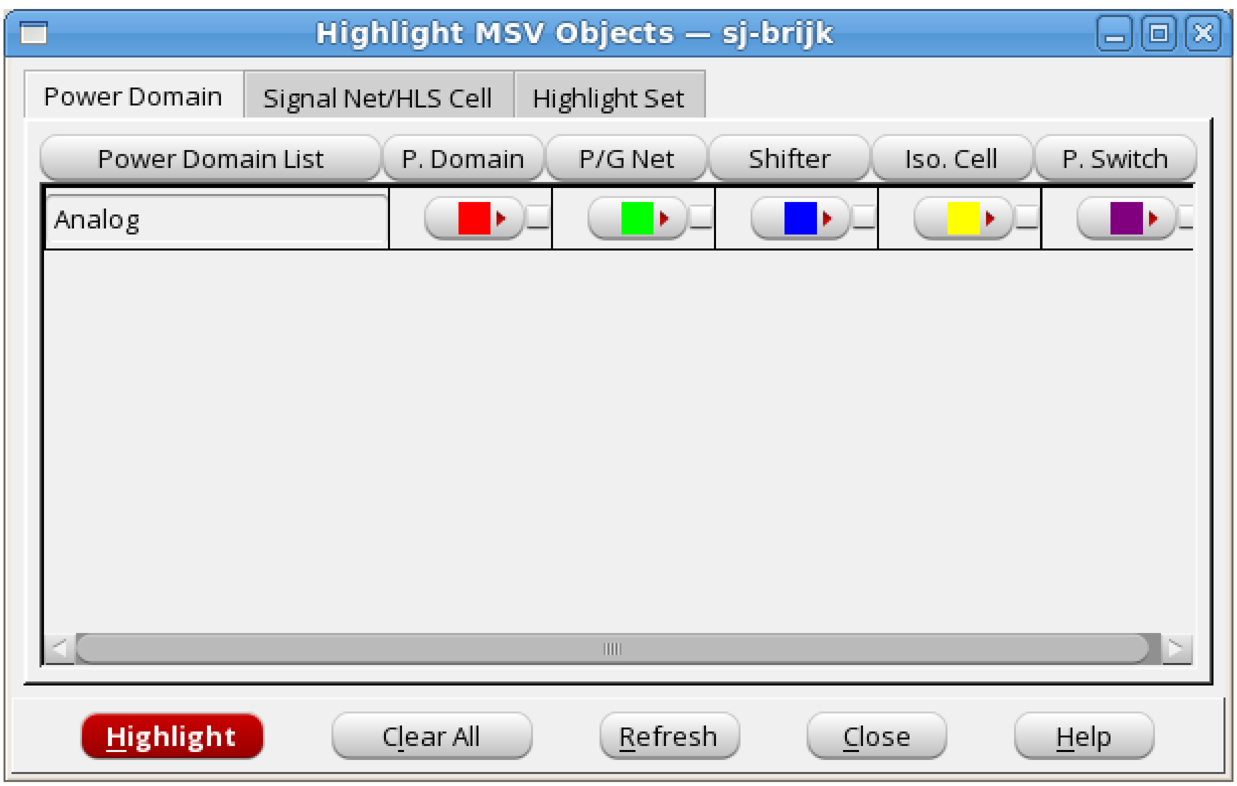
Highlight Power Domains

The Highlight Power Domains submenu opens the Highlight MSV objects form.

Highlight MSV Objects - Power Domain

Use the Highlight MSV Objects - Power Domain form to highlight power domains, and power/ground nets, level shifters, isolation cells, and power switches in power domains.

→ To open the Highlight MSV Objects -Power Domain form, choose *Power - Multiple Supply Voltage - Highlight Power Domain* and click on the Power Domain tab.



Highlight MSV Objects - Power Domain Fields and Options

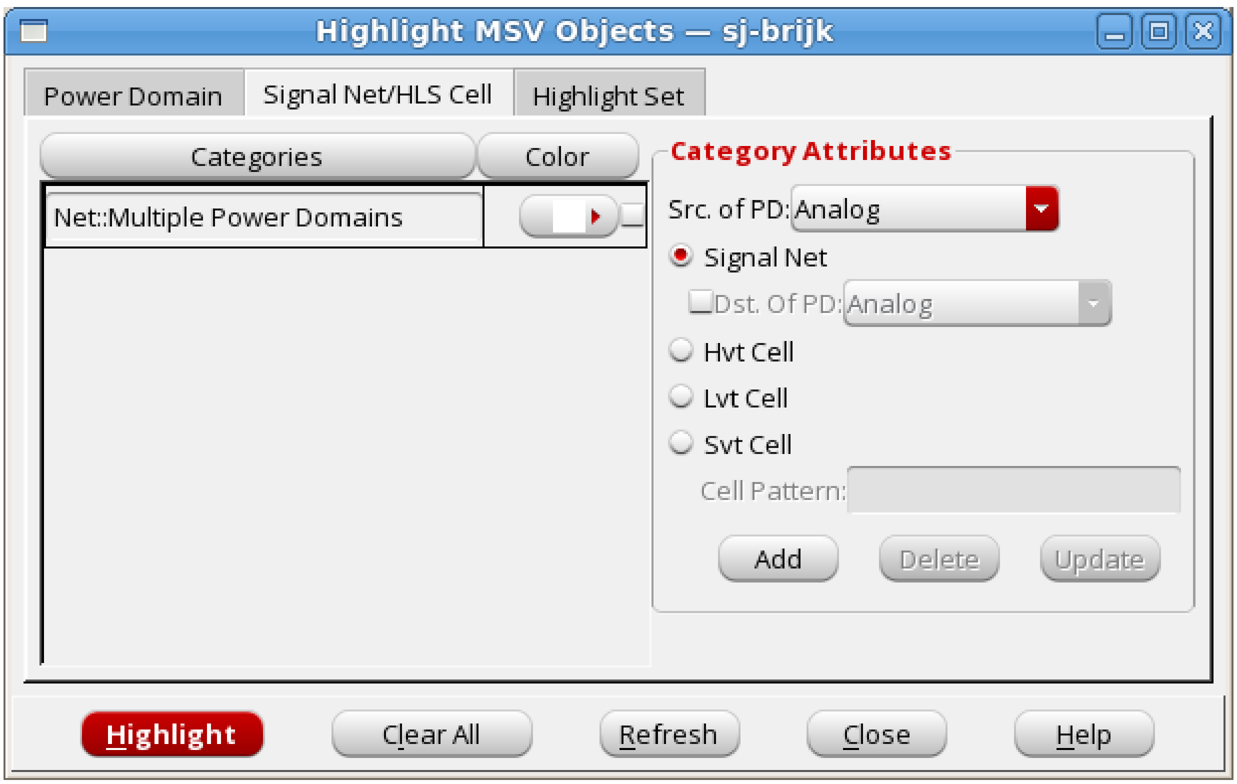
Power Domain List	Lists the power domains in your design. The software populates this list automatically.
P. Domain	Lets you select the color (highlight set) to use when highlighting a power domain. Click the checkbox and *Highlight* to highlight a power domain. For more information about highlight sets, see "Highlight MSV Objects - Highlight Set".
P/G Net	Lets you select the color (highlight set) to use when highlighting power/ground nets in a power domain. Click the checkbox and *Highlight* to highlight the power/ground nets. For more information about highlight sets, see "Highlight MSV Objects - Highlight Set".
Shifter	Lets you select the color (highlight set) to use when highlighting level shifters in a power domain. Click the checkbox and *Highlight* to highlight the level shifters. For more information about highlight sets, see "Highlight MSV Objects - Highlight Set".
Iso. Cell	Lets you select the color (highlight set) to use when highlighting isolation cells in a power domain. Click the check box and *Highlight* to highlight the isolation cells. For more information about highlight sets, see "Highlight MSV Objects - Highlight Set".
P. Switch	Lets you select the color (highlight set) to use when highlighting power switches in a power domain. Click the checkbox and *Highlight* to highlight the power switches. For more information about highlight sets, see "Highlight MSV Objects - Highlight Set".
Highlight	Highlights the selected object settings (power domains, power/ground nets, level shifters, isolation cells, and/or power switches) from the Highlight MSV Objects - Power Domain page and categories from the Highlight MSV Objects - Signal Net/HLS Cell page. Settings on the Highlight MSV Objects - Highlight Set page determine the highlight colors.
Clear All	Clears all highlights as determined from the current settings on the Highlight MSV Objects - Power Domain and Highlight MSV Objects - Signal Net/HLS Cell pages.

Refresh	Adds or deletes power domains from the Highlight MSV Objects - Power Domain if you have added or deleted power domains since the last time you highlighted objects. This option also removes categories on the Highlight MSV Objects - Signal Net/HLS Cell page if you have deleted power domains.

Highlight MSV Objects - Signal Net/HLS Cell

Use the Highlight MSV Objects - Signal/HLS form to specify the signal nets or cells you want to highlight.

→ To open the Highlight MSV Objects - Signal Net/HLS Cell form, choose *Power - Multiple Supply Voltage -Highlight Power Domain* and click on the Signal Net/HLS tab.



Highlight MSV Objects - Signal Net/HLS Cell Fields and Options

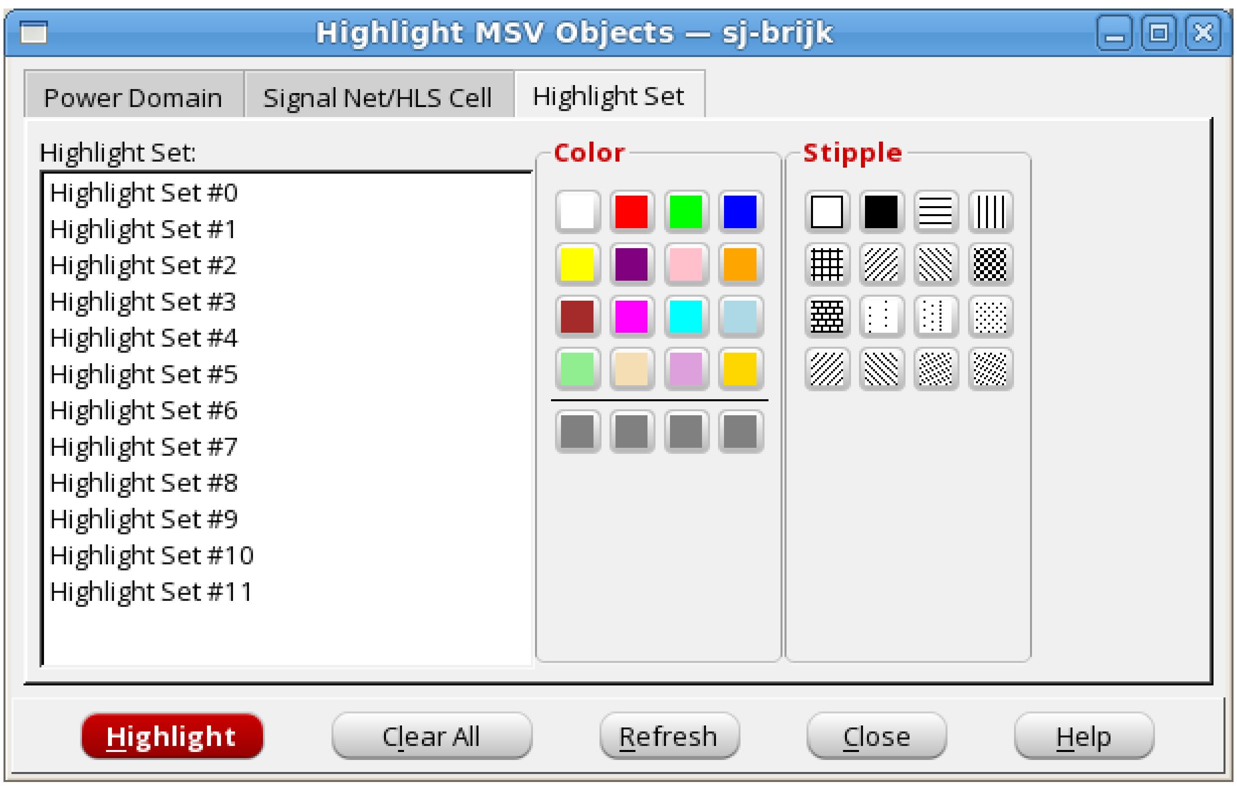
Categories	Specifies the categories created when you make selections from *Category Attributes* and click *Add*.

Color	Specifies the color for the category. The colors available are determined by the highlight sets. For more information, see "Highlight MSV Objects - Highlight Set".
Src. of PD.	Specifies the power domain containing the Hvt, Lvt, or Svt cells, or the power domain from where the signal nets originate.
Signal Net	Creates a signal net category. You must specify the *Src. of PD* to indicate where the signal nets originate. Optionally, you can specify the *Dst. Of PD* to specify the signal nets that originate in *Src. of PD* and are connected to the *Dst. Of PD*.
Dst. of PD	Specifies the destination power domain for the signal nets.
Hvt Cell	Creates a category for high voltage threshold (Hvt) cells. You must specify a *Src. of PD* to indicate the power domain that contains the Hvt cells and a *Cell Pattern* to specify the cell names.
Lvt Cell	Creates a category for low voltage threshold (Lvt) cells. You must specify a *Src. of PD* to indicate the power domain that contains the Lvt cells and a *Cell Pattern* to specify the cell names.
Svt Cell	Creates a category for standard voltage threshold (Svt) cells. You must specify a *Src. of PD* to indicate the power domain that contains the Svt cells, and a *Cell Pattern* to specify the cell names.
Cell Pattern	Specifies the cell names. You can use a prefix or suffix, plus a wildcard, for example `MyCells*` indicates all cells with prefix `MyCells`. You must specify a *Cell Pattern* if you select *Hvt Cell*, *Lvt Cell*, or *Svt Cell*.
Add	Adds a category to the *Categories* list based on the selections you have made in *Category Attributes*.
Highlight	Highlights the selected objects (power domains, power/ground nets, level shifters, isolation cells, and/or power switches) from the Highlight MSV Objects - Power Domain settings and categories from the Highlight MSV Objects - Signal Net/HLS Cell page. Settings on the Highlight MSV Objects - Highlight Set page determine the highlight colors.
Clear All	Clears all highlights as determined from the current settings on the Highlight MSV Objects - Power Domain and Highlight MSV Objects - Signal Net/HLS Cell pages.

Refresh	Adds or deletes power domains from the Highlight MSV Objects - Power Domain if you have added or deleted power domains since the last time you highlighted objects. This option also removes categories on the Highlight MSV Objects - Signal Net/HLS Cell page if you have deleted power domains.
Highlight	Highlights the selected object settings (power domains, power/ground nets, level shifters, isolation cells, and/or power switches) from the Highlight MSV Objects - Power Domain page and categories from the Highlight MSV Objects - Signal Net/HLS Cell page. Settings on the Highlight MSV Objects - Highlight Set page determine the highlight colors.
Update	Enables you to changes the source or destination power domains for a selected category.

Highlight MSV Objects - Highlight Set

Use the Highlight MSV Objects - Highlight Set form to specify the highlight colors for highlight sets.
→ To open the Highlight MSV Objects - Highlight Set form, choose *Power - Multiple Supply Voltage -Highlight Power Domain* and click on the Highlight Set tab.

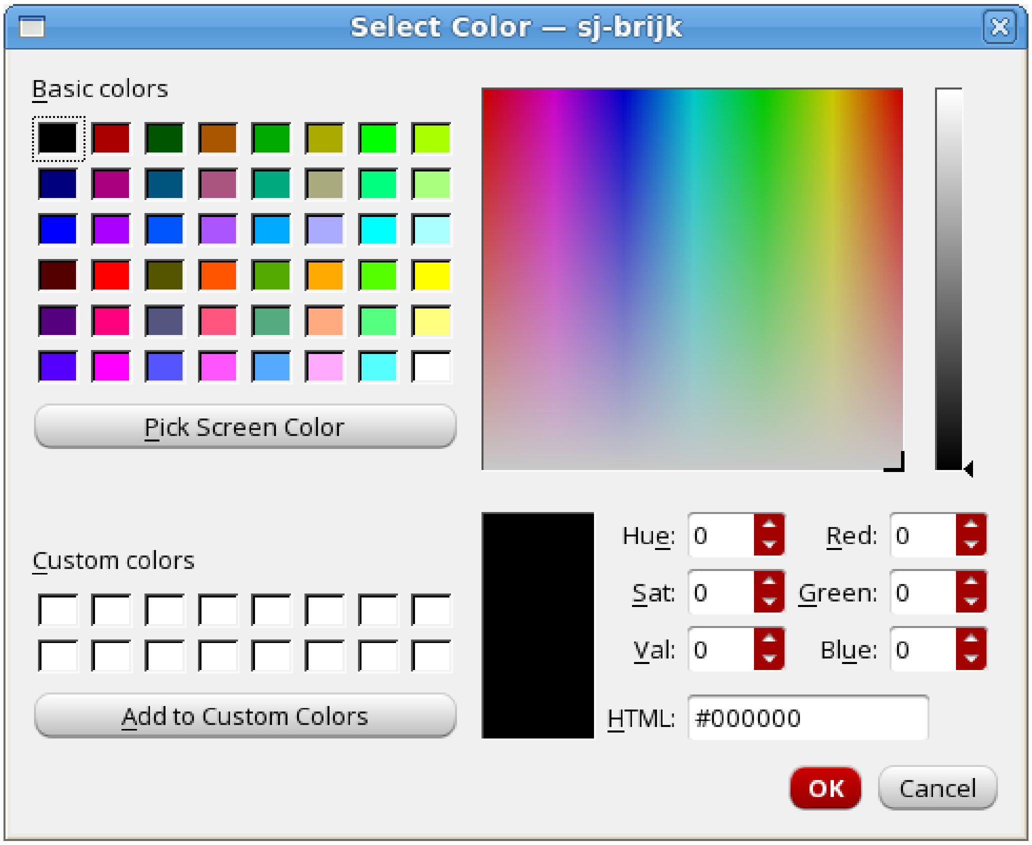


Highlight MSV Objects - Highlight Set Fields and Options

Highlight Set	Lists the 12 highlight sets. A highlight set is the combination of a color and stipple pattern. The highlight sets you define appear as choices for highlight colors for the various MSV objects on the Power Domain and Signal Net/HLS Cell forms. If you click on a highlight set, the current Color and Stipple settings are shown.
Color	Displays the colors you can select for the highlight set. The four gray boxes at the bottom of the color palette enable you to define custom colors. If you double-click on one of the gray boxes, the Color form opens. For more information, see "Color".
Stipple	Displays the stipple patterns you can select for the highlight set.
Highlight	Highlights the selected object settings (power domains, power/ground nets, level shifters, isolation cells, and/or power switches) from the Highlight MSV Objects - Power Domain page and categories from the Highlight MSV Objects - Signal Net/HLS Cell page. Settings on the Highlight MSV Objects - Highlight Set page determine the highlight colors.
Clear All	Clears all highlights as determined from the current settings on the Highlight MSV Objects - Power Domain and Highlight MSV Objects - Signal Net/HLS Cell pages.
Refresh	Adds or deletes power domains from the Highlight MSV Objects - Power Domain if you have added or deleted power domains since the last time you highlighted objects. This option also removes categories on the Highlight MSV Objects - Signal Net/HLS Cell page if you have deleted power domains.

Color

Use the Color form to create a custom color for the *Color* palette on the Highlight MSV Objects - Highlight Set form.
→ To open the Color form, choose *Power - Multiple Supply Voltage -Highlight Power Domain*, click on the Highlight Set tab, then double-click one of the gray boxes in the *Color* palette.



Color Fields and Options

Red	Lets you use a slider to select the red color value. The read-only box next to the slider displays the red color value.
Green	Lets you use a slider to select the green color value. The read-only box next to the slider displays the green color value.
Blue	Lets you use a slider to select the green color value. The read-only box next to the slider displays the blue color value.
Selection	Displays the RGB color determined by the *Red*, *Green*, and *Blue* settings. This is a read-only field. The color is displayed in the area below.

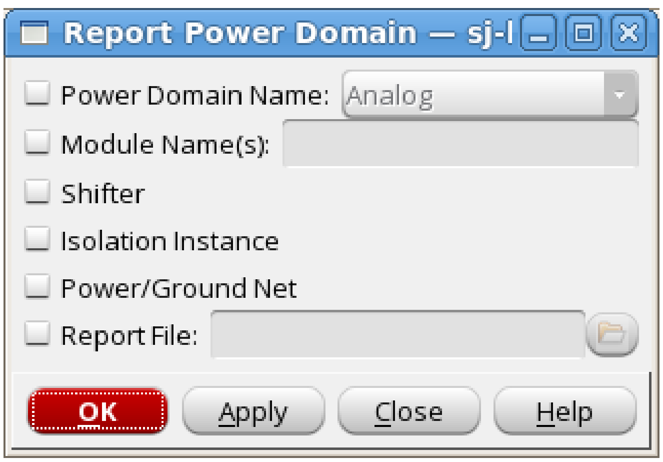
Report Power Domain

Use the Report Power Domain form to reports information about power domains.
→ To open the Report Power Domain form, choose *Power - Multiple Supply Voltage - Report Power Domain*.

The report includes the following attributes:

- Power domain name
- Power domain bounding box
- Timing library
- Mingap
- RS extension
- Row type
- Row spacing

The command also reports whether the power domain is always on.



Report Power Domain Fields and Options

Power Domain Name	Specifies the power domain whose attributes you want to report. *Default:* If you do not specify the power domain, this command report data about all power domains.

Module Name(s)	Checks whether the specified instances or hierarchical instances are in the power domain.
Shifter	Reports all shifters in the power domain.
Isolation Instance	Reports all isolation cells in the power domain.
Power/Ground Net	Reports all the power/ground nets in the power domain.
Report File	Specifies the file in which you want to write the data.

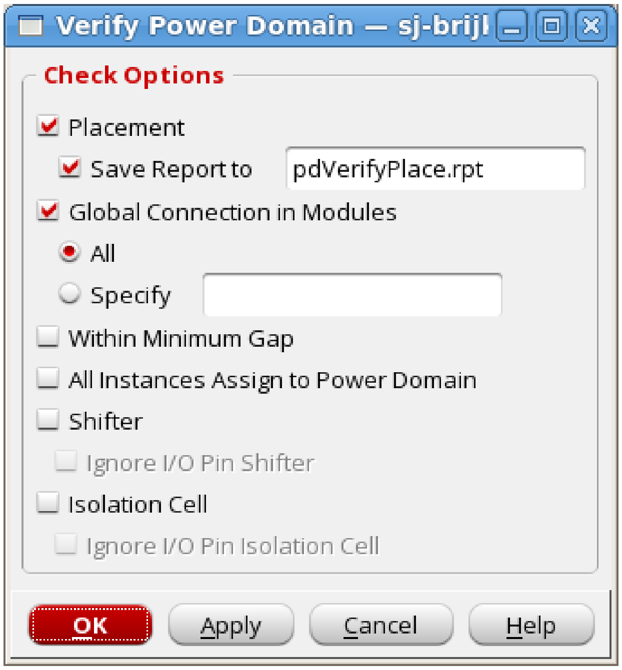
Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

`reportPowerDomain`

Verify Power Domain

Use the Verify Power Domain form to verify that members of a power domain are placed correctly and that their power and ground pins are connected to the power domain's power and ground nets.
→ To open the Verify Power Domain form, choose *Power - Multiple Supply Voltage - Verify Power Domain*.



Verify Power Domain Fields and Options

Placement	Verifies that only those cells assigned to a power domain are placed within the boundary of the power domain and reports any placement violations.	
Save Report to	Specifies a name and location for the report generated when you select *Placement*.	
Global Connection in Modules		
	Verifies that power and ground pins of instances within the power domain are connected to the power and ground nets of that power domain. In addition, this verifies that the tie-high and tie-low connections of a cell are connected to the same power and ground nets of the power domain to which the cell belongs.	
	All	All modules are verified.
	Specify	Specified modules are verified.
Within Minimum Gap	Verifies that the power domain ring is within the distance specified by the minimum gap specified when creating power domains.	

All Instances Assigned to Power Domain	
	Verifies that all instances are in the power domain.
Shifter	Verifies that shifters are added to all nets crossing power domains.
Ignore I/O Pin Shifter	Ignores I/O pin nets when verifying shifters.
Isolation Cell	Verifies that isolation cells are added for all nets that need isolation cells.
Ignore I/O Pin Isolation Cell	
	Ignores I/O pin nets when verifying isolation cells.

Related Text Commands

For information on the following text commands, see "Low Power Commands" in the *Text Command Reference*.

`verifyPowerDomain`

Power Planning

The Power Planning submenu contains the following items:

- Add Rings
  Opens the Add Rings form.
- Add Stripes
  Opens the Add Stripes form.
- Edit Power Via
  Opens the Edit Power Vias form.
- Create P/G Pin

Opens the Create P/G Pin form.

Add Rings

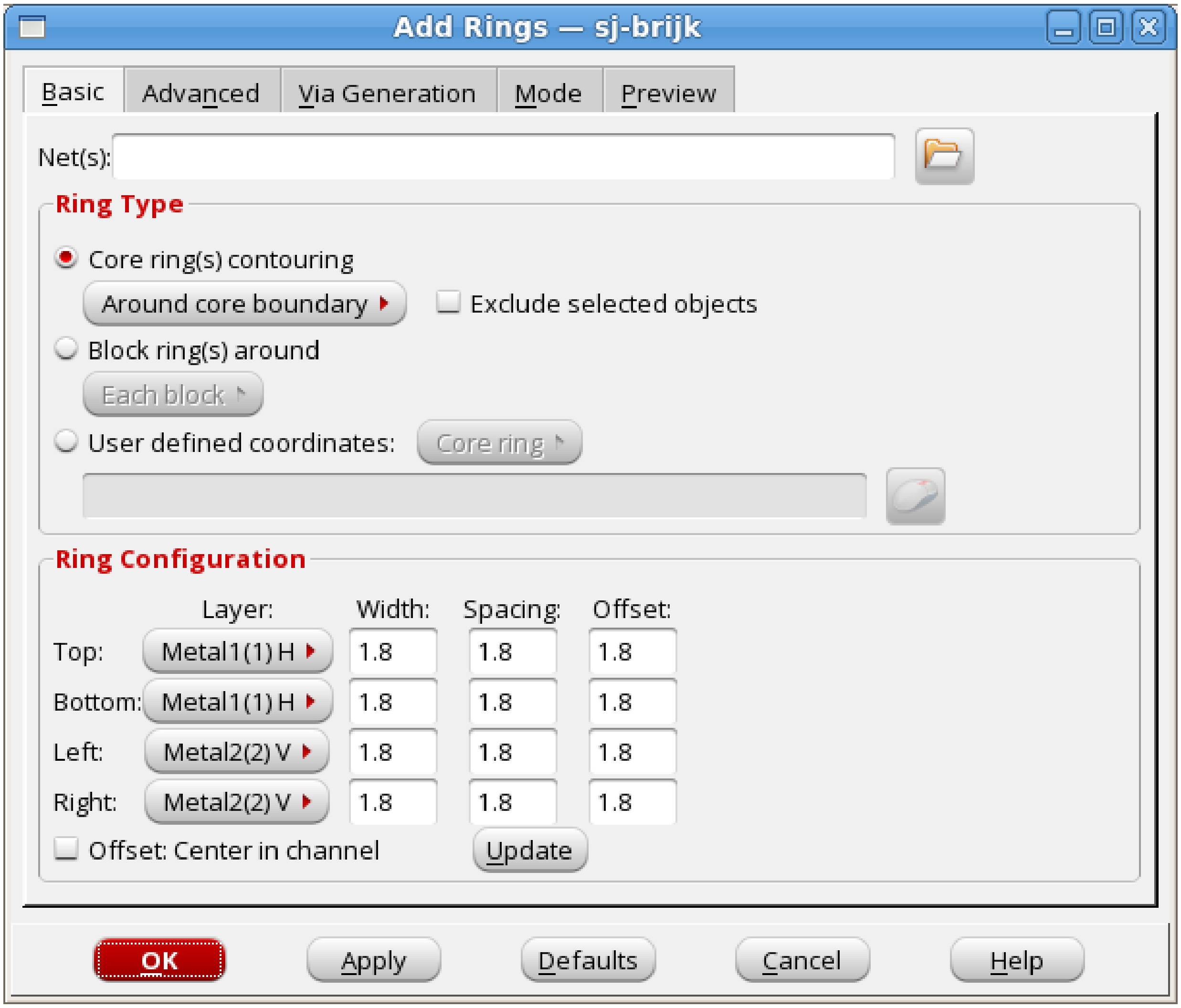
Use the Add Rings form to create power rings for specified nets around the core boundary or selected power domains, blocks, and groups of core rows. Add Ring has been enhanced to generate rings without checking for full DRC. This option can be used if user wants to create a quick power planning prototype. The Add Ring engine would try to honor user-defined parameters as much as possible. The Add Rings form contains the following three pages:

- Add Rings Basic
- Add Rings Advanced
- Add Rings Via Gen

You can access the Net Selection form from the Add Rings form.

Add Rings - Basic

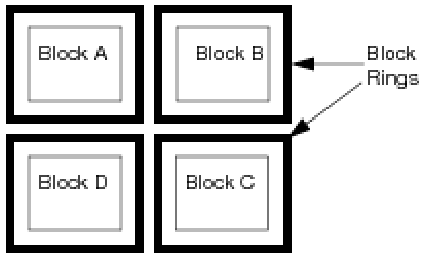
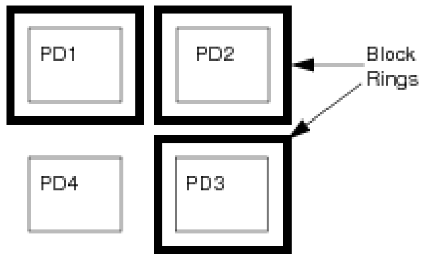
The *Basic* page of the Add Rings form lets you specify the net names for the power rings to be created, as well as the type of rings and their configuration.
→ To open the *Basic* page of the Add Rings form, choose *Power - Power Planning - Add Ring*, then click the *Basic* tab.

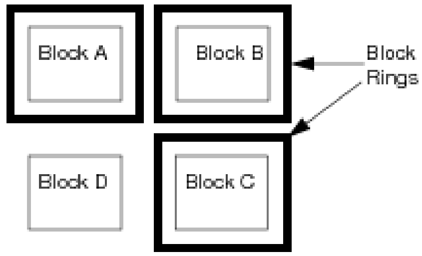
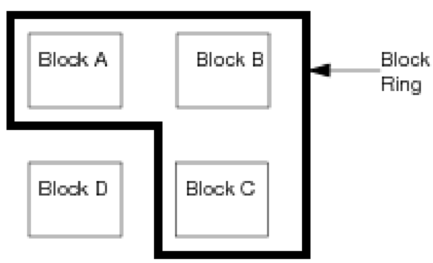


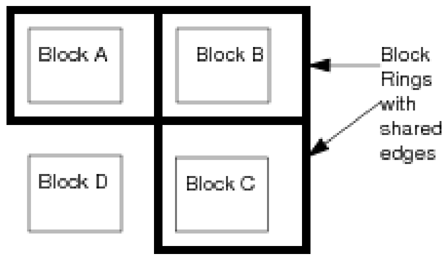
Add Rings - Basic Fields and Options

Net(s)	The net names for power rings to be created. With this option users can selectively choose the nets to be routed by Add Ring from the available special nets.
Ring Type	

Specifies the type of ring to be created. You can specify only one type at a time. For example, if you need both core rings and block rings, create core rings first, then select this form again to create block rings. Select one of the following options:		
Core Ring(s) contouring		
	Creates core rings that follow either the contour of the core boundary or contour around the I/O boundary. Select one of the following options:	
	Around core boundary	
		Creates core rings that contour around blocks or rows in the core area of the design, including cores that are rectilinear. This is the default. Use the options in the Ring Configuration panel to either center the ring in the channel between the core boundary and the I/O area, or offset each side of the ring by a specific distance from the core boundary.
	Along I/O boundary	
		Creates core rings that contour the I/O area. Use the options in the Ring Configuration panel to either center the ring in the channel between the core boundary and the I/O area, or offset each side of the ring by a specific distance from the I/O boundary.
	Exclude selected objects	
		If selected, creates a ring that contours the core boundary while contouring around the selected objects so that they are outside of the ring. If deselected, all objects in the core area are enclosed within the core ring. This is the default.
Block ring(s) around		
	Creates block rings that follow the contour of the specified objects. Choose one of the following options:	

	Each Block	Creates a separate ring around each block in the design. Rings are created as shown in the following illustration. 
	Each Reef	Creates a separate ring around each reef in the design. Reefs are used in flipchip designs.
	Selected power domain/fences/reefs	
		Creates a separate ring around each power domain selected in the design display area, around the fence that surrounds a soft block, or around a reef of bumps. If both a power domain and a fence are selected, the power domain takes precedence. For example, if you select PD1, PD2, and PD3, rings are created as shown in the following illustration. 
	Each selected block and/or group of core rows	

		Creates a separate ring around each block and each group of core rows that is selected in the design display area. For example, if you select Block A, Block B, and Block C, block rings are created as shown in the following illustration. 
	Cluster of selected blocks and/or groups of core rows	
		Treats all the blocks and groups of core rows selected in the design display area as a single cluster and creates a ring around the cluster. For example, if you select Block A, Block B, and Block C, a ring is created as shown in the following illustration. 
	With shared ring edges	

		Treats all the blocks and groups of core rows selected in the design display area as a single cluster and creates rings with shared ring edges around the cluster. To enable this option, you must first select *Cluster of selected blocks/groups of core rows*. For example, if you select Block A, Block B, and Block C, block rings with shared edges are created as shown in the following illustration. 
User defined coordinates		
	Creates a ring that has the same number of corners as the number of x and y coordinates that you specify. You must specify the coordinates in a linear sequence. For example, you cannot specify the coordinates in a sequence such as bottom left, top right, bottom right, top left. For more information, see the "Creating a Ring with User Defined Coordinates" section of the Power Planning and Routing chapter of Innovus User Guide.	
Mouse Click	Click this button, then move the cursor to the design display area. Click the points to define the corners of the ring. A temporary image shows the location of the ring wires that will be created. When you press the *Esc* key, the *User Specified Coordinates* text entry field is automatically populated with the coordinates of the area you selected.	
Core ring	The ring has the shape `RING`. This is the default.	
Block ring	The ring has the shape `BLOCKRING`.	
Ring Configuration	The configuration of the rings to be created. Specify options to meet the requirements of your design.	
Layer	Use the pull-down menus to select the layer to use for each side of the ring(s) being created.	

Width	Use the text entry fields to specify the width, in microns, of the ring segments for each side ring(s).	
Spacing	Use the text entry fields to specify the edge-to-edge spacing, in microns, between rings for each side of the ring.	
Update	Click this button to automatically update the values in the *Spacing* fields. If spacing values in the *Spacing* fields are less than the values from the LEF file for a particular width, the values in the *Spacing* fields are increased to prevent minimum spacing violations.	
Offset	Controls how core rings are offset from the core area. Select one of the following options:	
	Center in channel	
		Specifies that the core ring is centered in the channel between the I/O area and the core area. This option is not available for block rings.
	Specify	Select this option, then use the text entry boxes to specify the distance, in microns, between the edge of the inner ring and the boundary of the referenced object (blocks, rows, power domains, I/O area or core area) for each side of the ring. If you specify a negative number, the ring is created inside of, rather than surrounding, the referenced object. **Note:** For core rings, you can choose between this option and the *Center in channel* option. For block rings, you must specify offset values.

Related Text Commands

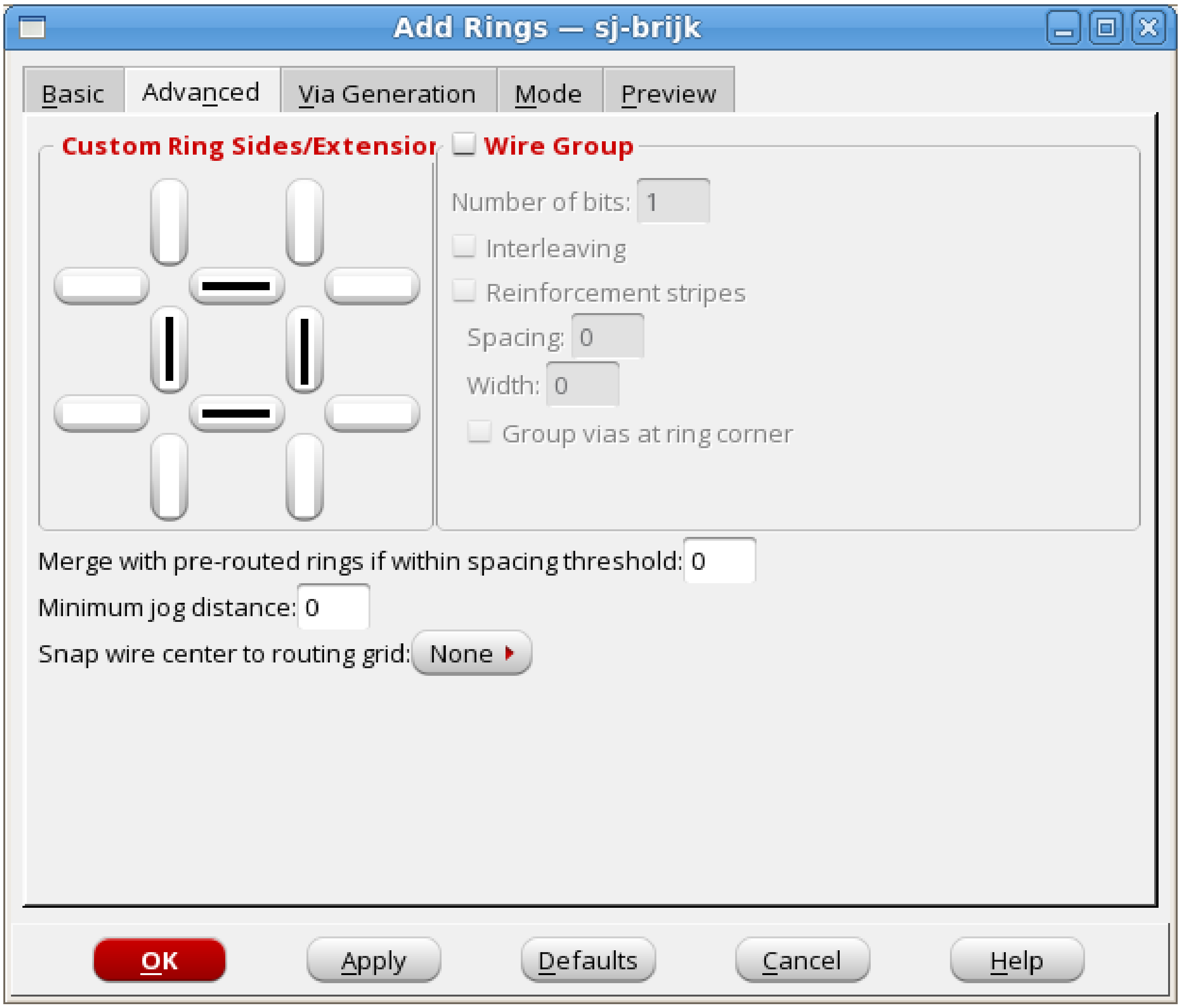
For information on the following command, see "Power Planning Commands" in the Text Command Reference.

`addRing`

Add Rings - Advanced

The Advanced page of the Add Rings form lets you limit which sides of a ring are to be created and which sides are to be extended to connect to existing power structures. This page also provides options for you to customize rings to meet your design needs.

→ To open the Advanced page of the Add Rings form, choose *Power - Power Planning - Add Rings*, then click the *Advanced* tab.



Add Rings - Advanced Fields and Options

Set Custom Ring Sides and Extension

	(Optional) Allows you to create rings in any configuration. Click a ring edge bar to select or deselect one or more edges to indicate where rings segments are to be created. Click an extension bar to select or deselect one or more of the eight strips (above, below, or to the sides of the ring edges) to indicate the direction in which you want to extend the ring. The ring is extended in those areas until encountering a legal target. By default, all edges are selected and all extensions are deselected.	
Create rectangular ring(s) only		
	If selected, the software does not create rectilinear rings. If deselected, the software can create either rectangular or rectilinear rings. This is the default.	
Merge with pre-routed rings if within spacing threshold		
	(Optional) The minimum spacing, in microns, allowed between ring segments before they can be merged. If spacing is less that this value, rings are merged.	
Minimum jog distance	(Optional) The minimum jog distance, in microns, allowed (to follow the contour of the object that the ring surrounds) before the jog is straightened. If the ring would need to jog a distance equal to or less than this value in order to follow the contour of the object, the ring will not jog.	
Snap wire center to routing grid		
	Control the snapping of the center of the sides of the rings to the routing grid. Choose one of the following:	
	None	Does not snap the wires. This is the default.
	Grid	Snaps the centers of the wires to the routing grid of the same layer as the wire.
	Half_Grid	Snaps the centers of the wires to the half-routing grid. The half-routing grid is a virtual grid with the tracks at the center of every two adjacent tracks of the routing grid.
	Either	Snaps the centers of the wires to the closer of the routing grid or half grid track.

Related Text Commands

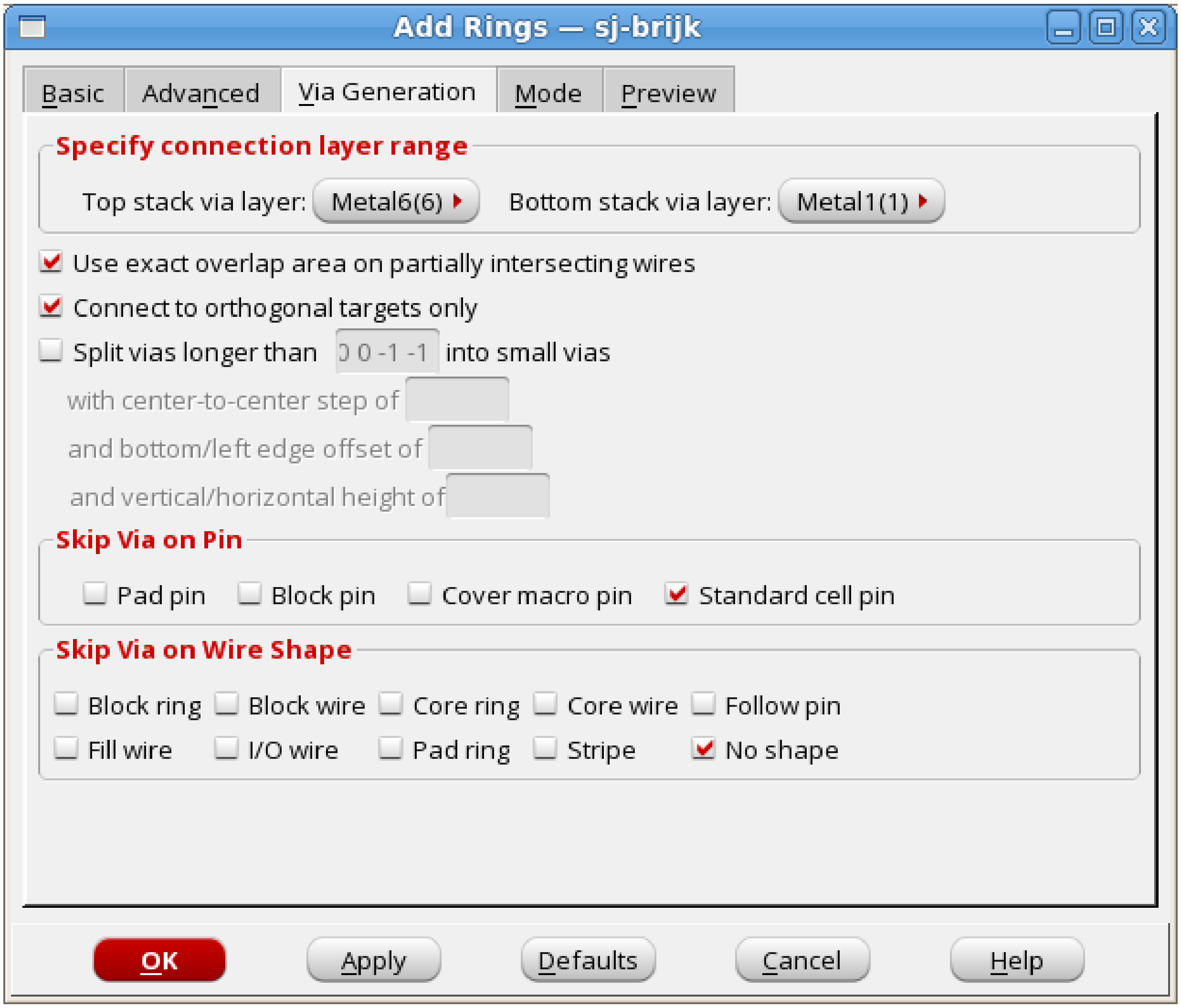
For information on the following command, see "Power Planning Commands" in the Text Command Reference.

`addRing`

Add Rings - Via Generation

The Via Generation page of the Add Rings form lets you specify how vias connect to the power rings.

→ To open the Via Generation page of the Add Rings form, choose *Power* - *Power Planning* - *Add Rings*, then click the *Via Generation* tab.



Add Rings - Via Generation Fields and Options

Top stack via layer	The highest metal layer to which stacked vias can connect. This limits the generation of vias to targets in the specified range.
Bottom stack via layer	The lowest metal layer to which stacked vias can connect. This limits the generation of vias to targets in the specified range.
Use exact overlap area on partially intersecting wires	

	If selected, the software can generate partial vias of the exact size of the overlap area. If deselected, the software always generates full-size vias.
Connect to orthogonal wires only	
	Creates vias *only* for orthogonal wires and pin intersections. *Default*: On
Split vias longer than X into smaller vias with center-to-center step of Y and bottom/left edge offset of Z	
	Splits vias that are longer than the specified length into smaller vias that have the specified center-to-center step and bottom/left edge offset (all values in micrometers). *Default*: Off
Skip Via on Pin	Select the types of pins for which via connections are permitted. Deselect the types of wires or pins to which via connections are not to be made: ◦ *Pad pin* ◦ *Block pin* ◦ *Cover macro pin* ◦ *Standard cell pin (Default selected)*

Skip Via on Wire Shape	Select the types of wires for which via connections are permitted. Deselect the types of wires or pins to which via connections are not to be made: ◦ *Pad pin* ◦ *Block pin* ◦ *Core ring* ◦ *Core wire* ◦ *Follow pin* ◦ *Fill wire* ◦ *I/O wire* ◦ *Pad ring* ◦ *Stripe* ◦ *No shape (Default selected)*

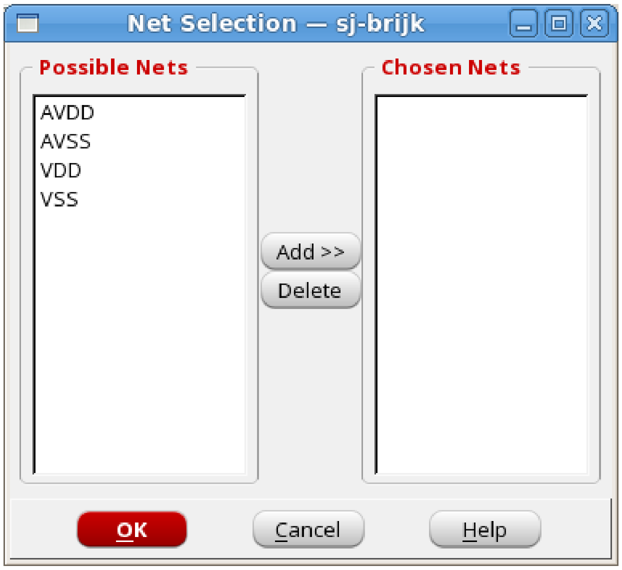
Related Text Commands

For information on the following command, see "Power Planning Commands" in the Text Command Reference.

`addRing`

Net Selection

Use the Net Selection form to select the net.
→ To open the Net Selection form, choose *Power - Power Planning - Add Rings* (*Basic* tab), then click the *browser* button at the top of the form.



Net Selection Fields and Options

Possible Nets	The list of nets available.
Chosen Nets	The list of nets added or list after nets are deleted.

Add Stripes

Use the Add Stripes form to create power stripes within the specified range. If block rings are encountered, the stripes connect to the block rings. If an obstruction is encountered, the stripe connects to the last stripe on the same net; otherwise the stripe stops at the core row boundary.

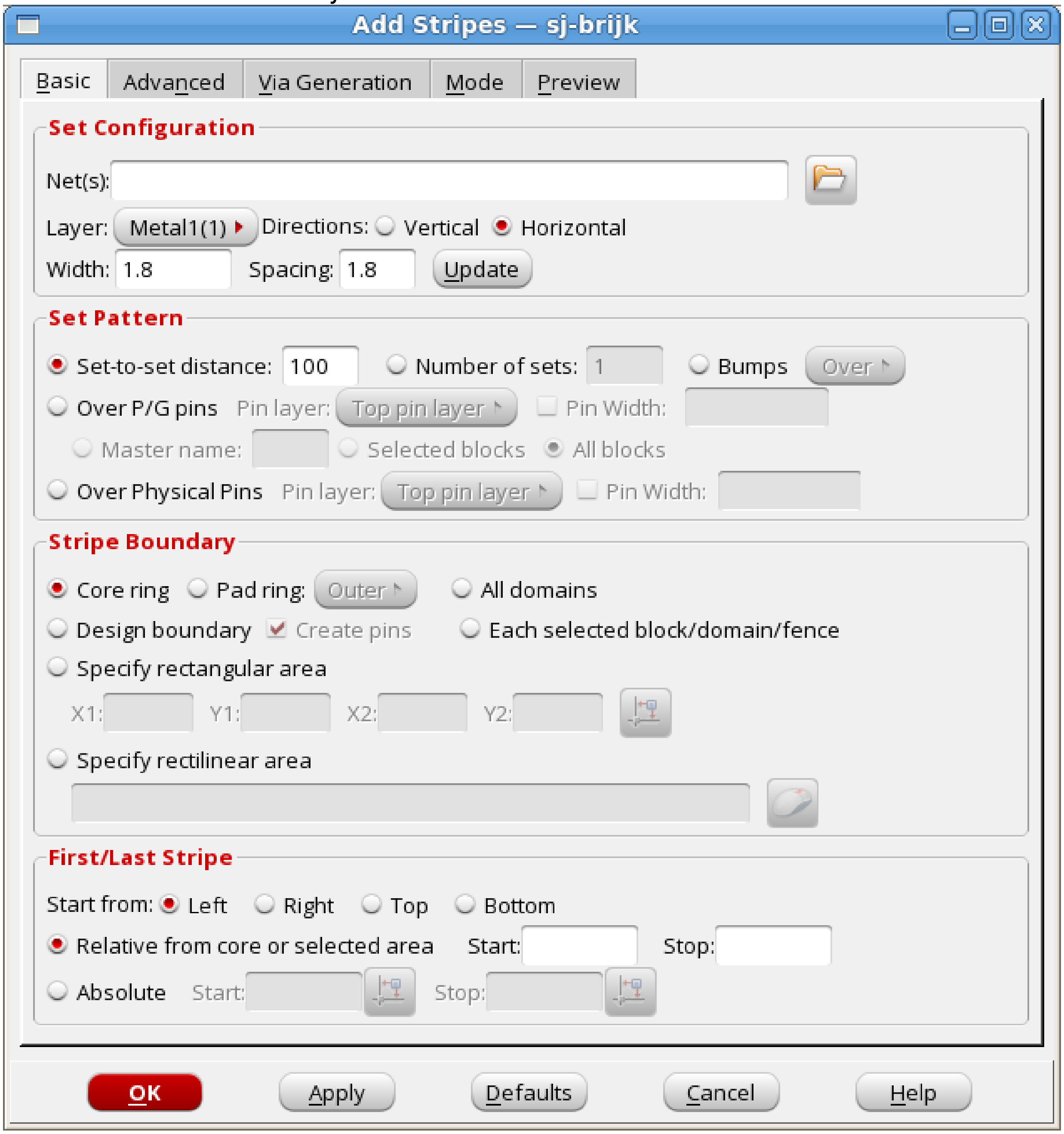
The Add Stripes form contains the following three pages:

- Add Stripes - Basic
- Add Stripes - Advanced
- Add Stripes - Via Generation

Add Stripes - Basic

Use the *Basic* page of the Add Stripes form to specify the nets, layers, direction, and other configuration options for power stripes that you add to the design.

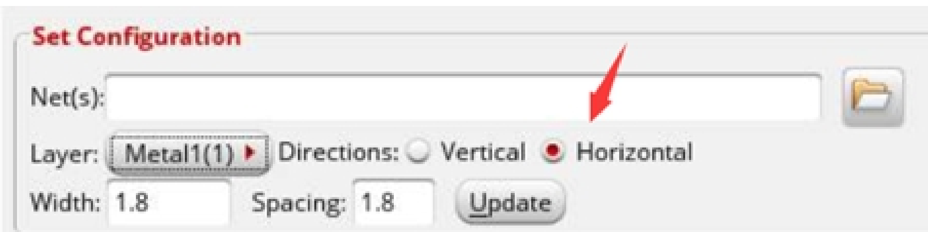
→ To open the *Basic* page of the Add Stripes form, choose *Power - Power Planning - Add Stripes*, the *Basic* tab is selected by default.



Note: On updating the layer settings through the LEF Definition file, the layer direction will automatically be updated on the Add Stripes form. For example, in the LEF Definition file, if you specify:

```
LAYER Metal1
TYPE ROUTING ;
WIDTH 0.230 ;
SPACING 0.230 ;
SPACING 0.6 RANGE 10.0 100000.0 ;
PITCH 0.560 ;
DIRECTION HORIZONTAL ;
```

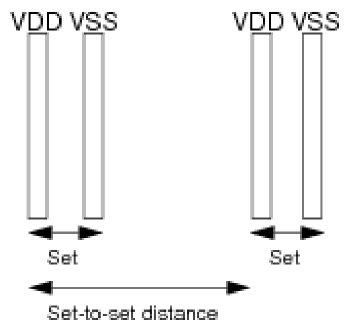
The direction will automatically be set to *Horizontal* under the *Set Configuration* section of the Add Stripes form.



Add Stripes - Basic Fields and Options

Set Configuration	The configuration of the stripe set to be created. Specify options to meet the needs of your design. With this option users can selectively choose the nets to be routed by Add Stripe from the available special nets.
Net(s)	The net name(s) for which stripes must be created. The number of net names determines the number of stripes within each set of stripes. The first net in the name list is created first and corresponds to the left or bottom stripe of the set. Separate multiple net names with a space. **Note:** This field is ignored if you specify *All domains* in the *Stripe Boundary* panel.
Layer	The layer to use to create stripes. By default, the software uses the first vertical routing layer or the second horizontal routing layer in the technology file to populate the form. **Note:** When you select a layer, the *Direction* buttons below *Layer* indicate the preferred direction of the layer you have selected.

Direction	The stripe orientation. You can specify only one direction at a time. If you need both vertical and horizontal stripes, create stripes in one direction first, then select this form again to create stripes in the other direction. Choose one of the following options:	
	Vertical	Creates vertical stripes with the attributes specified by the selected options. This is the default.
	Horizontal	Creates horizontal stripes with the attributes specified by the selected options.
Width	The width, in microns, of the stripes. You can specify a different width for each net within a set. If the number of widths specified does not match the number of net names, the last specified width is used for the unmatched nets.	
Spacing	The edge-to-edge spacing, in microns, between stripes in each set. You can specify different spacing rules between each pair of stripes. For *N* number of stripes in a set, *N* – 1 number of spacing rules must be to specified. If fewer values are specified, the last specified spacing is used for the unmatched stripe pairs.	
Update	(Optional) Automatically updates the values in the *Spacing* fields. If spacing values in the *Spacing* fields are less than the values from the LEF file for a particular width, the values in the *Spacing* fields are increased to prevent minimum spacing violations.	
Set Pattern	Controls the spacing between stripes. Choose one of the following options:	
	Set-to-set-distance	

		The distance (pitch), in microns, from the edge of the first stripe of the set to the same edge of the first stripe of the next set. The number of sets is derived from the stripe range and pitch. The value entered must be a positive number, in microns. The following diagram shows the locations from which this distance is measured for a set that contains two stripes. 
	Number of sets	The number of stripe sets to be created. The set-to-set distance is derived from the stripe range and number of sets you specify in this field.
	Bumps	Determines the generation of stripes in relation to bumps. • *Over* indicates that stripes should be generated over bumps. • *Between* indicates that stripes should be generated between bumps. *Default*: *Over*

<table>
<tr><td></td><td>Over P/G pins</td><td>Generates stripes over power/ground pins in a standard cell or block.
Pin layer indicates the layer on which the stripe is generated.
Default: Top pin layer of the standard cell or block
Master Name indicates instances of the standard cell (or block) master over which the stripes should be generated. This is the default setting.
Selected blocks allows you to use the Innovus main window display to select instances for which to generate stripes.
All blocks specifies that stripes should be generated over all blocks.
Max pin width indicates that only pins less than or equal to this maximum pin width setting will be considered when generating stripes over pins. This is available only when Over P/G pins is enabled.
Default: off</td></tr>
<tr><td>Stripe Boundary</td><td colspan="2">Controls the region over which stripes are to be created. Select one of the following options:</td></tr>
<tr><td></td><td>Core ring</td><td>Stripes are created within the area enclosed by the core ring.</td></tr>
<tr><td></td><td>Pad ring</td><td>Stripes are created within the area enclosed by the pad ring. If you select this option, you must also select one of the following options to indicate stripe behavior for multiple pad rings of the same net:
Inner indicates that stripes stop at the pad ring closest to the core area.
Outer indicates that stripes stop at the pad ring closest to the design boundary.</td></tr>
<tr><td></td><td colspan="2">Design Boundary</td></tr>
</table>

		Stripes are created within the design boundary.
	Create pins	**Note:** If selected, create I/O pins for each stripe. Any overlap with existing I/O pins at the design boundary are flagged as warnings after stripes are created. This is the default. If deselected, pins are not created.
	Each selected block/domain/fence	
		Stripes are created only for the selected block or power domain, or for a fence surrounding a soft block. For power domains, these stripes start and stop at the power ring that surrounds the selected power domain boundary. For fences, these stripes start and stop at the fence. If both a power domain and a fence are selected, the power domain takes precedence. If deselected, stripes are created in the manner that you specify with the other options on this form, treating the power domain boundary as a block. This is the default.
	All Domains	Stripes are created over all power domains for each power and ground net within each power domain. Stripes start and stop at each power domain boundary or rings around the domain, and ignore any values that you specify in the Net(s) field.
	Specify rectangular area	
		Stripes are created within the exact rectangular area indicated by the coordinates.
	Specify rectilinear area	
		Stripes are created within the exact rectilinear area indicated by the coordinates.
First / Last Stripe	Controls the location of the first and last stripe. Select one of the following options:	

	Start from	For vertical stripes: • *left* indicates that stripes should be generated from left to right, taking the left offset into account. • *right* indicates that stripes should be generated from right to left, taking the right offset into account. *Default*: *left* For horizontal stripes: • *bottom* indicates that stripes should be generated from bottom to top, taking the bottom offset into account. • *top* indicates that stripes should be generated from top to bottom, taking the top offset into account. *Default*: *bottom*
	Relative from core or specified area	
		The distance, in microns, of the start point of the stripes from the stripe boundary. If the boundary is the core ring, pad ring, or design area, the first and last stripe start at the core area. This is the default. For vertical stripes, enter the distance from the left/right side of the boundary for the first stripe. For horizontal stripes, enter the distance from the top/bottom of the boundary for the first stripe.
	Absolute locations	
		The exact x and y coordinates where the first and last stripes must be created. For vertical stripes, enter the distance from the left/right side of the boundary for the first stripe. For horizontal stripes, enter the distance from the top/bottom of the boundary for the first stripe.

Related Text Commands

For information on the following command, see "Power Planning Commands" in the Text Command Reference.

`addStripe`

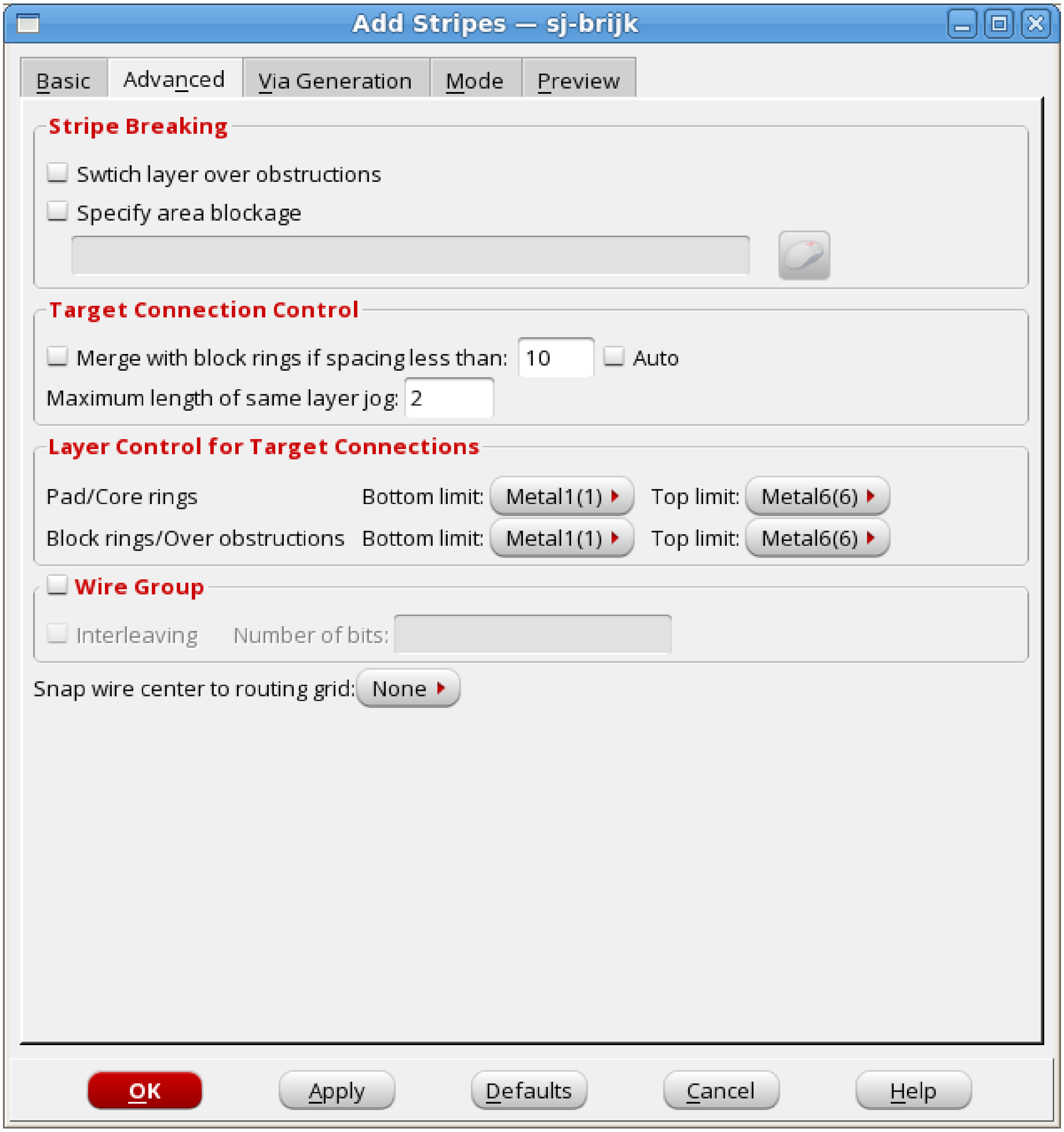
Related Topics

For more information, see the "Adding Stripes to Power Domains" section of the Power Planning and Routing chapter of Innovus User Guide.

Add Stripes - Advanced

Use the Advanced page of the Add Stripes form to limit the area in which stripes can be created as well as specify the behavior of stripes when they are near rings, obstructions, rows, or design boundaries.

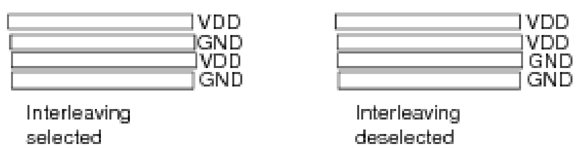
→ Choose *Power - Power Planning - Add Stripes*, then click the *Advanced* tab.



Add Stripes - Advanced Fields and Options

Switch layer over obstructions

	If selected, stripes switch layers, are routed over obstructions, and then continue on the original layer. *Default*: Off
Specify area blockage	
	Specifies a rectilinear area blockage that restricts the addition of any stripes to this region. Select this option, then specify the blockage coordinates. Clicking on the MouseClick icon and moving the cursor to the design display area enables you to use the mouse to specify the blockage coordinates. *Default*: Off
Merge with rings if spacing less than	
	If selected, you can specify the threshold, in microns, for merging stripes. If the threshold spacing between the stripe and ring is smaller than the value specified, the stripe jogs to connect to the nearby ring. The default value of this field is the same as the value in the *Spacing* field on the *Basic* page of this form. If deselected, stripes do not merge with block rings.
Maximum length of same layer jog	
	The maximum length, in user units, that a stripe can jog on the same layer before switching to an adjacent layer. For example, if you specify a value of `2` user units, and an obstruction causes a stripe on layer `4` to jog for `3` user units, the jog will occur on layer `3` or `5`. However, if an obstruction causes the stripe to jog for only `1` user unit, the jog occurs on layer `4`.
Layer Control for Target Connections	
	Controls the layers that stripes can switch to when encountering rings. Choose a top and bottom layer for each of the following types of rings:

	Pad/Core rings	Stripes that encounter a pad or core ring can only switch to layers within the range you select. By default, both the Top Limit and Bottom Limit are set to two layers above and below the stripe layer.
	Block rings / Over obstructions	Stripes that encounter a block ring can only switch to layers within the range you select. By default, both the Top Limit and Bottom Limit are set to two layers above and below the stripe layer
Wire group	If selected, permits the use of wire groups for buses, based on a property set in the DEF. If deselected, wire groups are not used. This is the default. **Note:** For stripes to connect to rings using wire groups, you must select *Use wire group* in both the Add Rings and Add Stripes forms.	
Interleaving	The style of the wire groups. The following illustration shows the difference in how wires are created:  	
Snap wire center to routing grid		
	Controls how wires snap to the grid. Select one of the following options from the pulldown menu:	
	None	Does not snap the wires. This is the default.\
	Grid	Snaps the centers of the wires to the routing grid of the same layer as the wire.
	Half_Grid	Snaps the centers of the wires to the half-routing grid. The half-routing grid is a virtual grid with the tracks at the center of every two adjacent tracks of the routing grid.
	Either	Snaps the centers of the wires to the closer of the routing grid or half grid track.

Related Text Commands

For information on the following command, see "Power Planning Commands" in the Text Command Reference.

`addStripe`

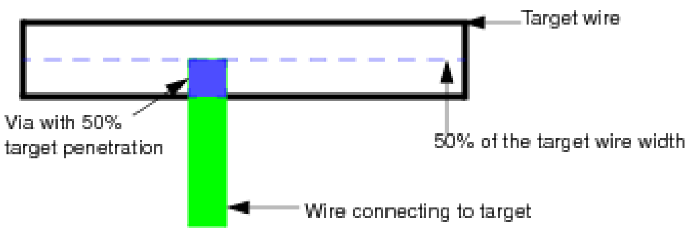
Add Stripes - Via Generation

Use the Via Generation page of the Add Stripes form to specify how vias connect to the power stripes.
→ To open the Via Generation page of the Add Stripes form, choose *Power - Power Planning - Add Stripes*, then click the *Via Generation* tab.

Add Stripes - Via Generation Fields and Options

Split vias longer than X into smaller vias and bottom/left edge offset of Z with center-to-center step of Y

	Splits vias that are longer than the specified length into smaller vias that have the specified center-to-center stFor vertical stripes, enter the distance from the left/right side of the boundary for the first stripe.ep and bottom/left edge offset (all values in micrometers). *Default*: Off
If same layer target exists, connect to	
Same layer target only	Prevents the creation of vias to connect to other layers when a target exists on the same layer. This only applies when targets of multiple layers of the same net are stacked on top of one another. If a target does not exist on the same layer, vias are generated to connect to targets on other layers.
Targets on all layers	Allows the creation of vias to connect to other layers when a target exists on the same layer.
Make via connection to	Select the types of wires or pins for which via connections are permitted. Deselect the types of wires or pins to which via connections are not to be made. By default, vias can connect to each of the following types of wire or pin: ◦ *Pad ring/pin* ◦ *Core ring* ◦ *Stripe* ◦ *Block ring* ◦ *Block pin* ◦ *Cover macro pin*
Crossover Width	The maximum width of a crossover via, specified as a percentage of a full-size via.
Crossover Height	The maximum height of a crossover via, specified as a percentage of a full-size via.

Target penetration (%)	Specifies a smaller size for vias connecting to targets of a particular wire or pin type. By default, if a wire or pin is a target to which a via can be connected, the via is a full-sized. If you want the via to be smaller, you can specify a value in this field for each wire type. Only a single dimension of the via will be scaled. For example, if you specify a value of 50, the via will be full-sized in one dimension (the width of the wire that crosses the ring), but only half the width in the other dimension (the width of the target wire). 
Skip Via on Wire Shape	
	Select the types of wire shapes for which via connections need to be skipped: • *Block ring* • *Block wire* • *Core ring* • *Core wire* • *Follow pin* • *Fill wire* • *I/O wire* • *Pad ring* • *Stripe* • *No shape*

Related Text Commands

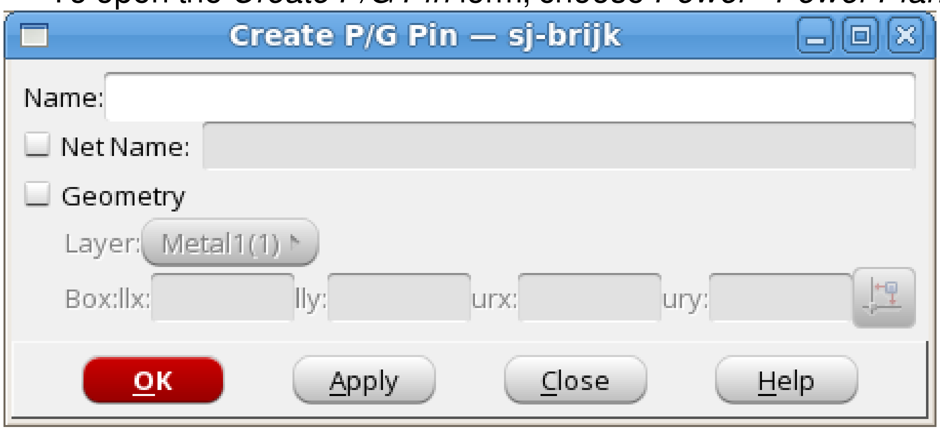
For information on the following command, see "Power Planning Commands" in the Text Command Reference.

addStripe

Create P/G Pin

Use the *Create P/G Pin* form to create a power/ground pin as per the specified coordinates of the physical shape.

→ To open the *Create P/G Pin* form, choose *Power - Power Planning - Create Power/Ground Pin*.



Create P/G Pin Fields and Options

Name	Specifies the name of the power/ground pin.
Net Name	Specifies the name of the net to which the power/ground pin will be attached.
Geometry	Specifies the geometry of the physical pin: the layer on which to create it, and the location.
Layer	Specifies the layer on which the power/ground pin will be created. The layer id should be a numerical number, ranging from `1` to `7`.

Box	Specifies the location of the P/G pin. Specify the coordinates or select them in the artwork window.	
	llx	Specifies the lower-left x coordinate of the power/ground pin.
	lly	Specifies the lower-left y coordinate of the power/ground pin.
	urx	Specifies the upper-right x coordinate of the power/ground pin.
	ury	Specifies the upper-right y coordinate of the power/ground pin.

Related Text Commands

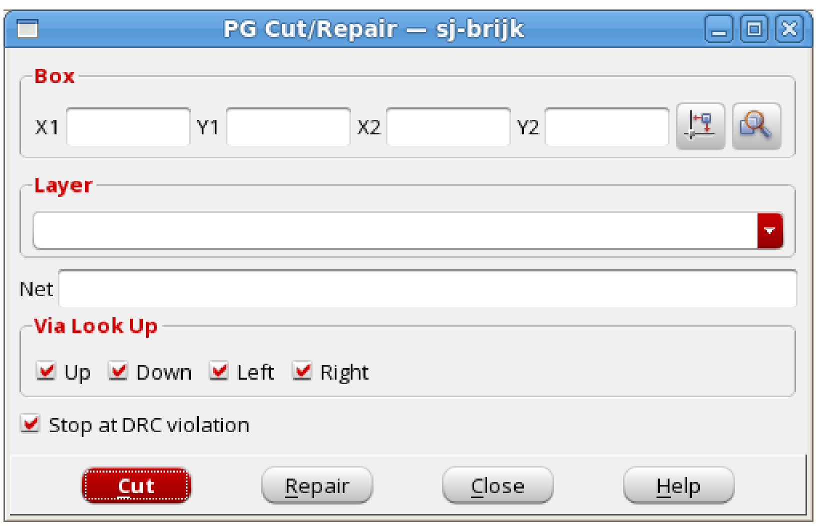
For information on the following command, see "Floorplan Commands" in the *Text Command Reference* document.

`createPGPin`

Pg Cut/Repair

Use the *PG Cut/Repair* form to cut/repair power strips for specified nets.

→ To open the *PG Cut/Repair* form, choose *Power - Power Planning - PG Cut/Repair*.



PG Cut/Repair Fields and Options

Box	Specifies the area for PG Cut/Repair. • Click the *Draw* button and your mouse to create a rectangular area in the design. The software displays the coordinates in the *X1*, *Y1*, *X2* and *Y2* fields. • Manually enter the coordinates in the *X1*, *Y1*, *X2* and *Y2* fields. • Click the *View Area* button to retrieve the coordinates of the current viewing area in the Innovus design display window.
Layer	Specifies the layers for PG Cut/Repair. Automatically populates the layers that overlap or touch the box.
Net	Specifies the nets for PG Cut/Repair. Automatically populates the nets that overlap or touch the box.
Via Look Up	Defines the via that are used in the repaired area. Catches the via based on the selection. *Default:* Select all. **Example** If only the *Up* check box is selected, during PG repair, Innovus catches the first via up to the repaired area.PG repair, Innovus catches the first via up to the repaired area. Only then this via is used for the PG repair.
Stop at DRC violation	Specifies if creation of wires or vias having DRC violations should be allowed. Select this option to disable creation of such wires and vias. *Default:* On.

Edit Power Vias

Use the Edit Power Vias form to add, modify, and delete power vias.

The Edit Power Vias form contains the following two pages:

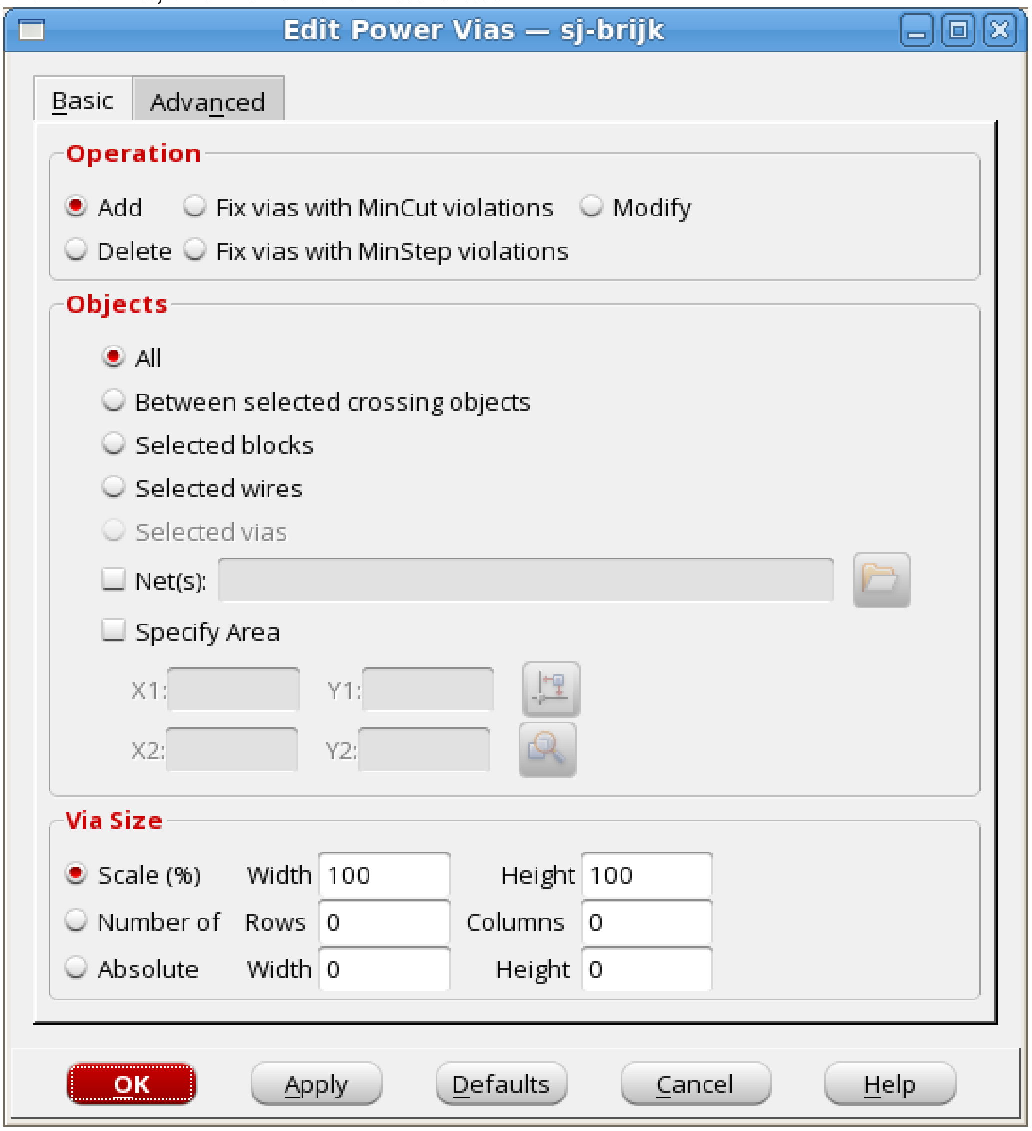
- Edit Power Vias - Basic
- Edit Power Vias - Advanced

Edit Power Vias - Basic

Use the *Basic* page of the Edit Power Vias form to add power vias to the design or to perform one of the following actions on existing power vias:

- Modify
- Delete
- Convert virtual vias created by the Automatic Power Planning (APP) software to real vias
- Fix vias that are not in compliance with the LEF `MINIMUMCUT` rule

→ To open the *Basic* page of the Edit Power Vias form, choose *Power -- Power Planning -- Edit Power Via*, then click the *Basic* tab.



Edit Power Vias - Basic Fields and Options

Operation	The action that will be performed by the software. Select one of the following actions:	
	Modify	Changes the size of existing vias.
	Add	Generates new vias.
	Delete	Removes existing vias.
	Fix vias with MinCut Violations	
		Updates existing vias that violate the LEF `MINIMUMCUT` rule. Note: When this option is selected the below options Selected Blocks and Via Size are greyed out.
	Fix vias with MinStep violations	
		Updates existing vias that violate the LEF `MINIMUMSTEP` rule.
Objects	The vias that will be affected by the selected operation. Select one of the following options:	
	All	Adds, modifies, or deletes all power vias in the design.
	Between selected crossing objects	
		Adds, modifies, or deletes power vias between the selected objects and wires crossing those objects.
	Selected blocks	
		Adds, modifies, or deletes power vias between the selected blocks.
	Selected wires	
		Adds, modifies, or deletes power vias between the selected wires crossing blocks.
	Selected Vias	

		Modifies or deletes the selected vias. This radio button is enabled only when the *Operation* is selected as *Modify* or *Delete*.
Net(s):	Enables you to select the nets for editing vias.	
Specify Area	You can either manually enter the coordinates for the area or use the mouse to automatically populate the coordinate fields for adding, modifying, or deleting power vias.	
Via Size	The size of the via to be added or the size to which an existing via is to be modified to. **Note:** This section is only available if you select *Add* or *Modify* in the *Operation* panel. Select one of the following options:	
	Scale (%)	The percentage values by which to scale the via dimensions. Use the text entry fields to specify values for both width and height.
	Number of Rows X Columns Y	The number of cuts per row and per column.
	Absolute Width X Height Y	The width and height of the added or modified vias.

Related Text Commands

For information on the following command, see "Power Planning Commands" in the *Text Command Reference* document.

`editPowerVia`

Related Topics

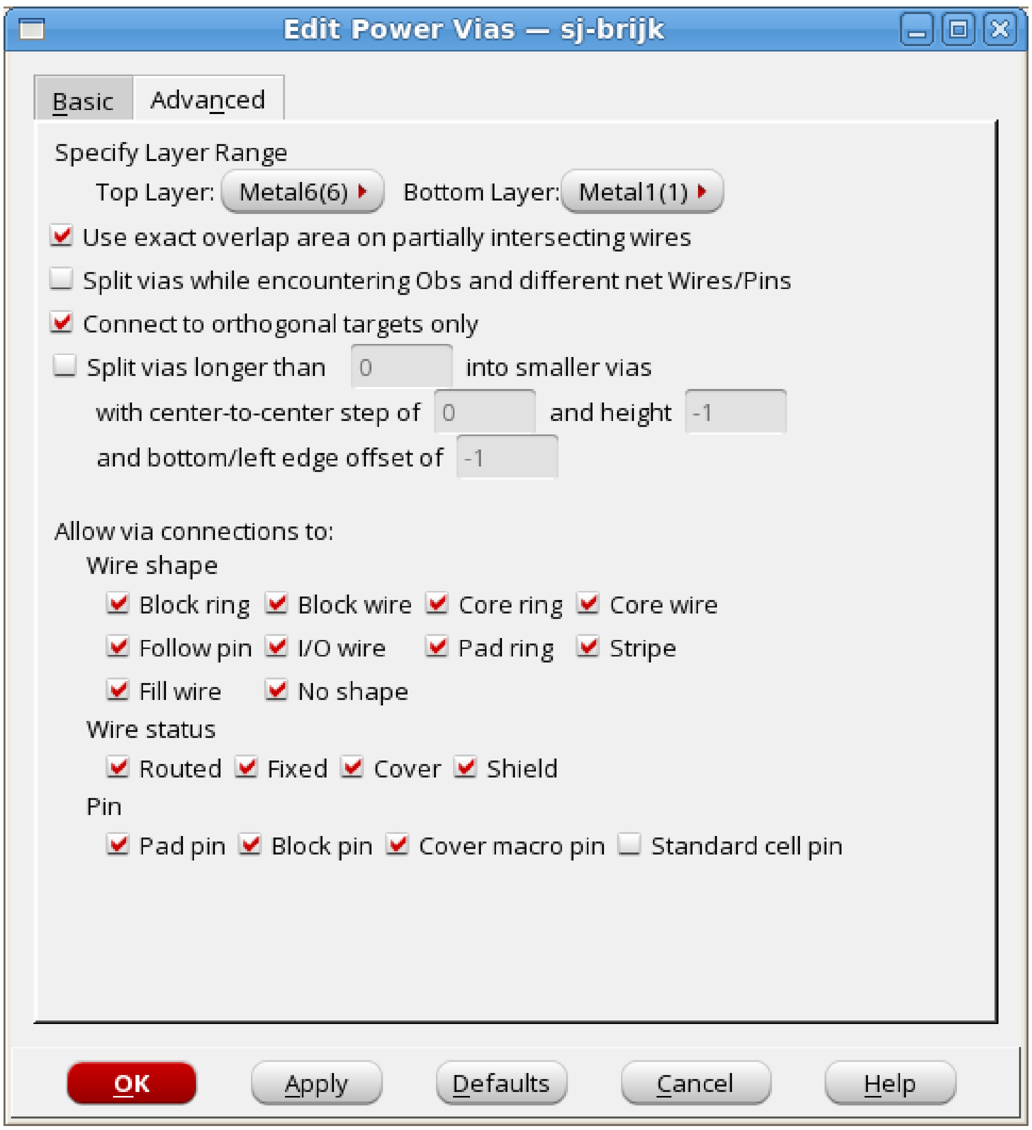
For more information, see the the following sections of the Power Planning and Routing chapter of Innovus User Guide:

- Fixing LEF MINIMUMCUT Violations

- Fixing LEF Minimum Spacing Violations

Edit Power Vias - Advanced

Use the Advanced page of the Edit Power Vias form to specify a range of layers on which vias can be created, as well as the types of wires to which vias can connect.
→ To open the Advanced page of the Edit Power Vias form, choose *Power -- Power Planning -- Edit Power Via*, then click the *Advanced* tab.



Edit Power Vias - Advanced Fields and Options

Top layer	The highest metal layer to which vias can connect. This limits the generation of vias to targets in the specified range.
Bottom layer	The lowest metal layer to which vias can connect. This limits the generation of vias to targets in the specified range.
Use exact overlap area on partially intersecting wires	
	If selected, the software can generate partial vias of the exact size of the overlap area. If deselected, the software always generates full-size vias.
Split vias while encountering Obs and different Wires/Pins	
	If selected, two or more partial vias can be created at the crossover between a stripe and any target (pin or wire) if an obstruction (macro obstruction; wire or pin on a different net) prevents the creation of a full-size via. This may be useful, for example, if several metal obstructions partially obstruct the area where a full-size via would normally be placed. This option permits the creation of partial vias that would not violate the process rules, in the open areas. If deselected, one via of the maximum size will be created. *Default*: Off
Connect to orthogonal wires only	
	Creates vias *only* for orthogonal wires and pin intersections. *Default*: On
Split vias longer than W into smaller vias with center-to-center step of X and height Y and bottom/left edge offset of Z	
	Splits vias that are longer than the specified length into smaller vias that have the specified center-to-center step and bottom/left edge offset (all values in micrometers). *Default*: Off

Allow via connections to	Select the types of wires or pins for which via connections are permitted. Deselect those to which via connections are not to be made. By default, vias can connect to each of the following. Wire Shape ◦ *Block ring* ◦ *Block wire* ◦ *Core ring* ◦ *Core wire* ◦ *Follow pin* ◦ *I/O wire* ◦ *Pad ring* ◦ *Stripe* ◦ *Fill wire* Wire Status: ◦ *Routed* ◦ *Fixed* ◦ *Cover* ◦ *Shield* Pin ◦ *Pad pin* ◦ *Block pin* ◦ *Cover Macro pin*

Related Text Commands

For information on the following command, see "Power Planning Commands" in the *Text Command Reference* document.

`editPowerVia`

Power Analysis

The Power Analysis sub-menu contains the following items:

- Set Power Analysis Mode
  Opens the Set Power Analysis Mode form
- Run Power Analysis
  Opens the Run Power Analysis form

Set Power Analysis Mode

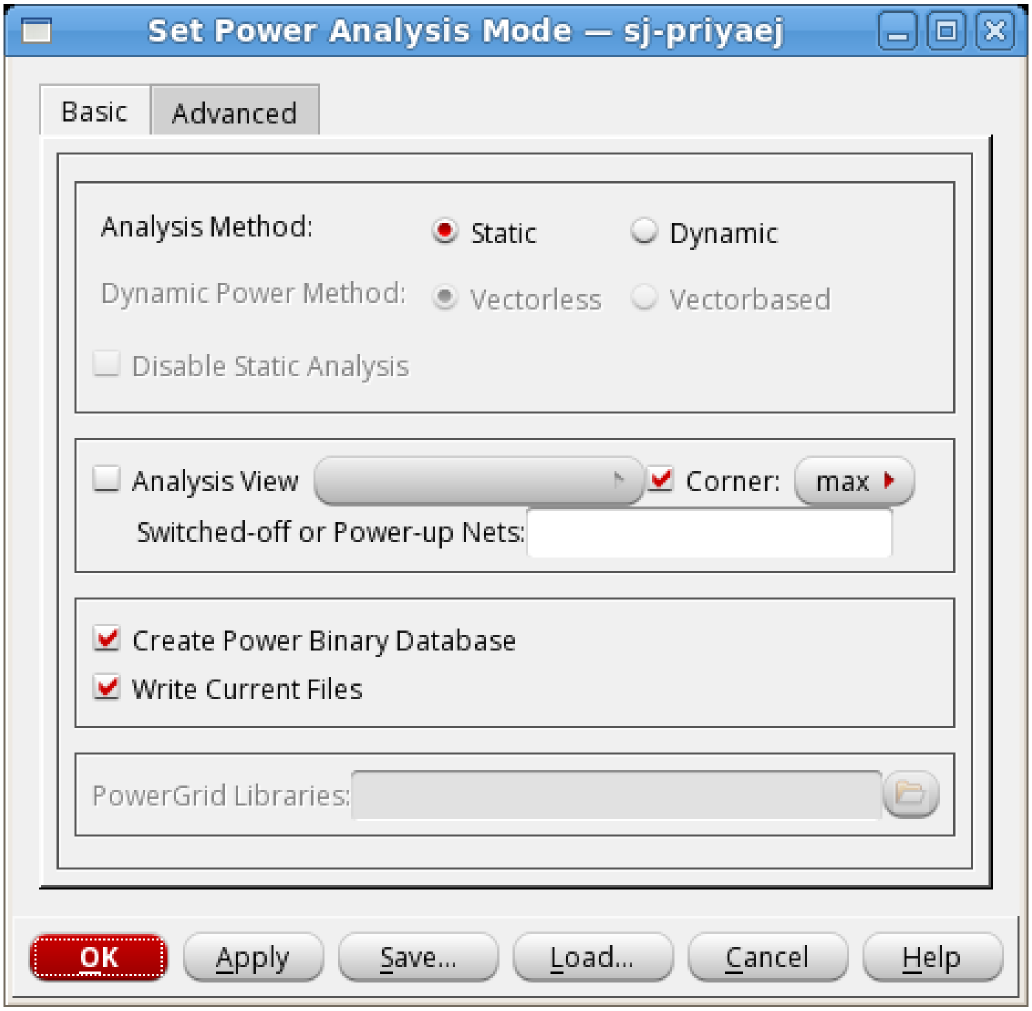
The Set Power Analysis Mode form contains the following pages:

- Set Power Analysis Mode - Basic
- Set Power Analysis Mode - Advanced

Set Power Analysis Mode - Basic

Specifies whether static or dynamic power analysis should be run and some additional settings.

→ To open the Basic page of the Set Power Analysis Mode form, choose *Power* -- *Power Analysis* -- *Setup*.

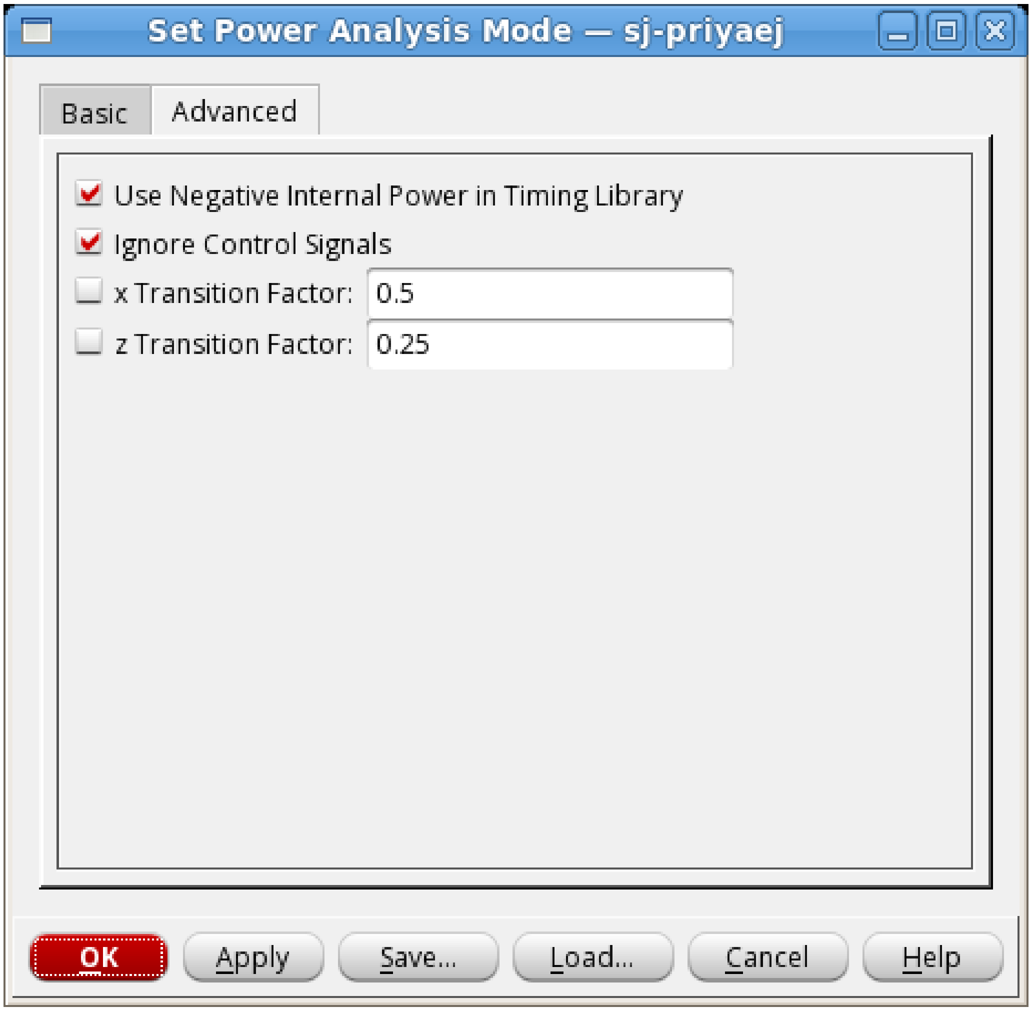


Fields and Options

Analysis Method	Specifies either static or dynamic power analysis
Dynamic Power Method	If dynamic power analysis is set this specifies if the method of analysis is vectorless or vector based.

Disable Static Analysis	When selected in the dynamic vector-based or dynamic vectorless flows, the command performs only dynamic analysis and turns-off static power calculation. *Default*: Not selected for *Static* analysis method, selected for *Dynamic* analysis method
Analysis View	Specifies the Analysis view.
Corner	Specifies the corner via a pulldown list. The choices are `min`, or `max`. *Default*: `max`
Switch off Power Nets	Specifies if power nets should be switched off
Create Power Binary Database	Specifies that a binary power database should be created. This can be used for viewing the power data graphically.
Write Current Files	Specifies the tool to generate the current data files, one current data file per net. *Default*: `true`.
PowerGrid Libraries	Specifies the name of the Cadence power cell libraries (.cl)

Set Power Analysis Mode - Advanced



Fields and Options

Use Negative Internal Power in Timing Library	Specifies that the tool will keep negative internal energy numbers from the `.lib` internal power table. When not set, negative power is treated as 0. *Default*: `true`
Ignore Control Signals	If set specifies that control signals will be ignored when propagating activity. *Default*: `true`
X Transition Factor	When using VCD one can specify how transitions to and from X are counted. These transitions are defined as shown in the table below. Transitions to and from the X state will be treated as full transitions multiplied by the specified factor. *Default*: `0.5`
Z Transition Factor	When using VCD one can specify how transitions to and from Z are counted. These transitions are defined as shown in the table below. Transitions to and from the Z state will be treated as full transitions multiplied by the specified factor. *Default*: `0.25`

Transitions from/to X and Z Values

Transition	Definition	Default
to/from X	[0 or 1 or Z] <-> X	0.5
to/from Z	[0 or 1] <-> Z	0.25

Related Text Commands

- `set_power_analysis_mode`

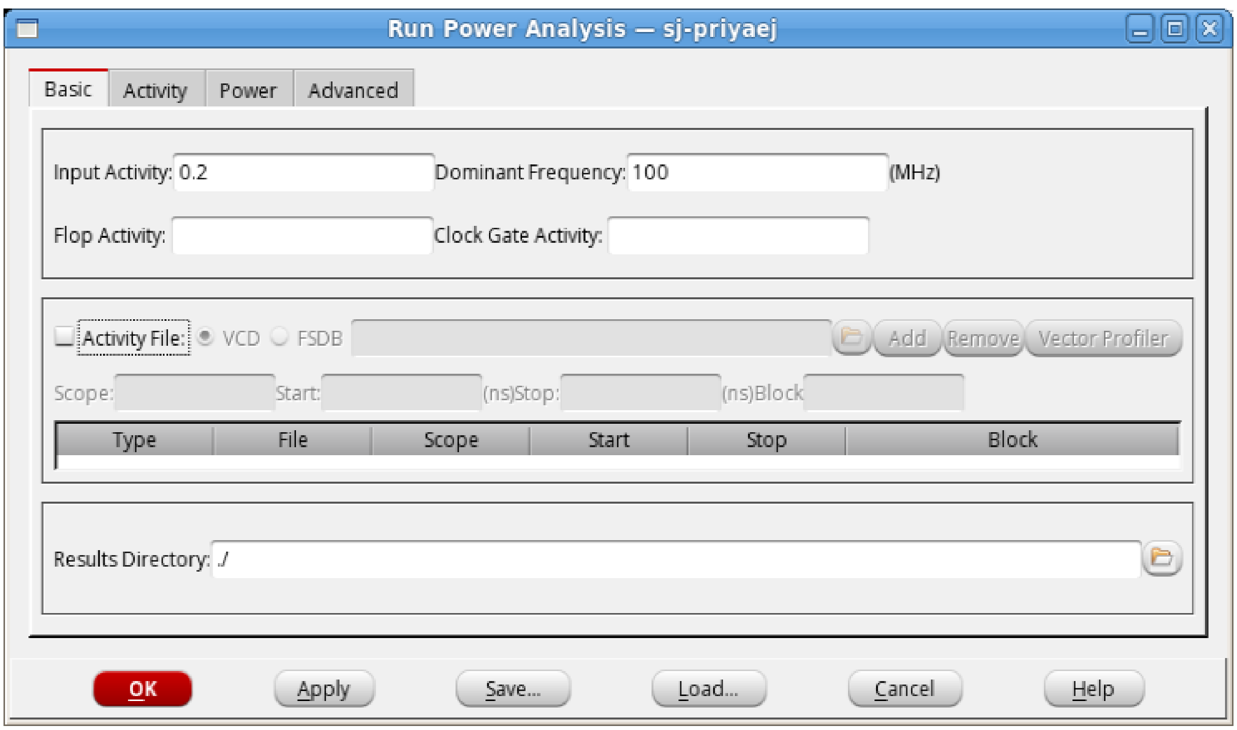
Run Power Analysis

The Run Power Analysis form has five pages:

- Run Power Analysis - Basic
- Run Power Analysis - Activity
- Run Power Analysis - Power
- Run Power Analysis - Advanced

Run Power Analysis - Basic

Runs the power analysis with the provided parameters.



Fields and Options

Input Activity	Specifies the average number of times as a (Specified as a fraction) that a primary input switches in a clock cycle. It can be any number between 0 and 1. *Default*: 0.2
Dominant Frequency	Specifies the dominant frequency of the design.
Flop Activity	Specifies the activity of outputs of sequential logic. There is no default.
Clock Gate Activity	Specifies the average number of times that a clock-gating cell switches in a clock cycle at the output of the pin. Enter any positive number. There is no default. **Note:** The value that you specify in GUI will overwrite the value in `set_default_switching_activity -clock_gates_output` parameter.
Activity File	If selected, activates the fields for entering VCD/FSDB information. A VCD/FSDB file must be specified.
Vector Profiler	When clicked, displays the Run Vector Profile window.
Scope	Specifies the scope of the VCD file.
Start	Specifies the start time in nanoseconds (ns) of the VCD file that will be used for power analysis.
Stop	Specifies the stop time in nanoseconds (ns) of the VCD file that will be used for power analysis.
Block	Specifies the block name.
Results Directory	Specifies the directory where the power analysis output will be placed.

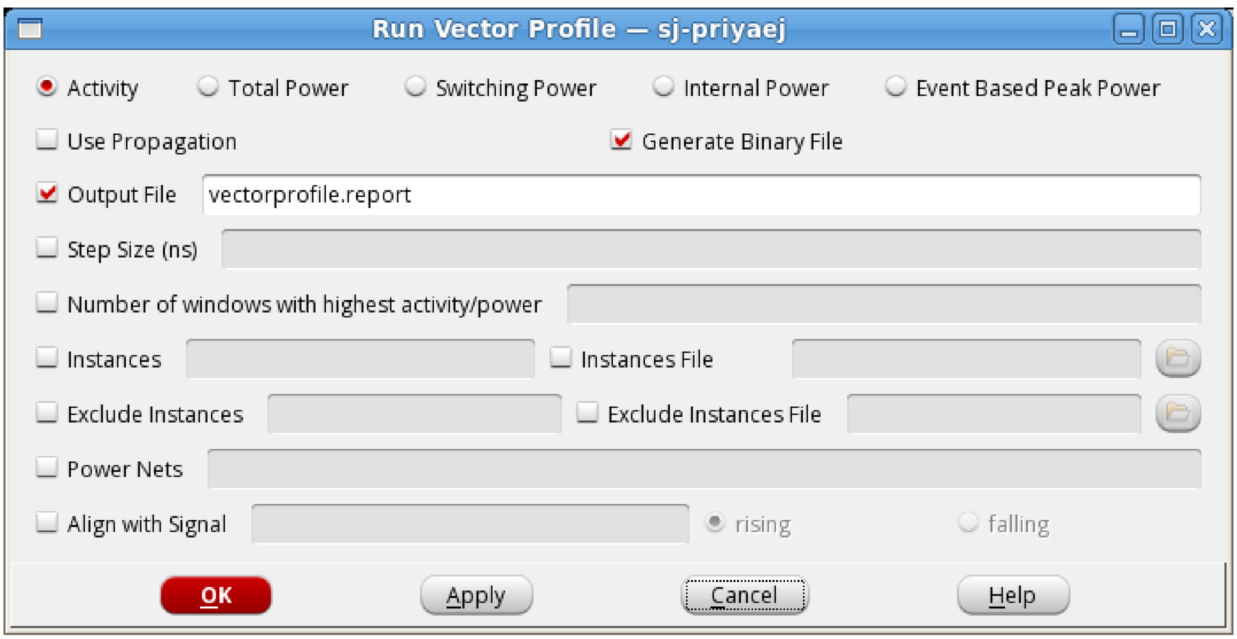
Related Text Commands

For information on the following command, see "Power Calculation Commands and Attributes" in the *Text Command Reference*:

- `report_power`

Run Vector Profile

Use this form to create Vector profile report for the specified VCD file.
→ Choose *Power & Rail* - *Run Power Analysis* - *Basic* tab, and then click the *Vector Profiler* button.



Run Vector Profile Fields and Options

Activity	Enables activity profiling. Reports the number of toggles for every window.
Total Power	Enables total power profiling. Reports total power in milliWatts (mW).

Switching Power	Enables switching power profiling. Reports switching power in milliWatts (mW).
Internal Power	Enables internal power profiling. Reports internal power in milliWatts (mW).
Use Propagation	Enables propagation when partial VCD is provided.
Event Based Peak Power	Specifies to enable event-based vector profiling. This method computes power profile of every event on each net. The event-based peak power profiling enables you to accurately capture vectors that could produce peak power using very small resolution (1ps) and with better performance than average power profiling which uses larger resolution to compute average toggle density.
Output File	Writes out the Vector profiling report into the file that you specify. By default, the report is written out into `vcdprofile.report` file.
Step Size (ns)	Specifies the step size, in nanoseconds (ns). Activity / Power profiling is carried out for every step size that you specify.
Number of windows with highest activity/power	Provides `n` top windows with maximum activity or power. *Default*: 3
Instances	Enables profiling of the instances that you specify.

Instances File	Enables profiling of the instances from the instance file that you specify.
	For example, instances in an instance file can be specified as follows:
	-- 	
	`inst_1`
	`inst_2`
	`inst_3`
	`.`
	`.`
	`.`
	`inst_n`
	-- 	

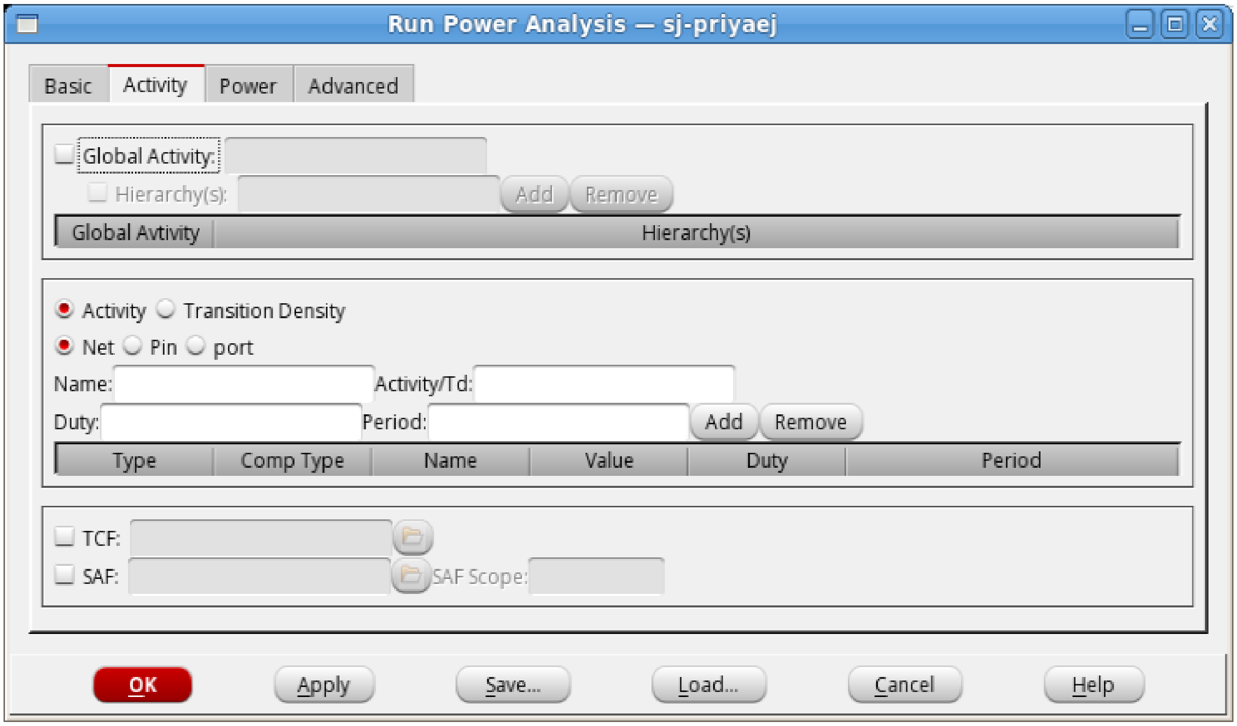
Exclude Instances	Disables counting of toggles or calculating power for the specified instances while reporting activity or calculating power for the entire design.
Exclude Instances File	Disables counting of toggles or calculating power for the specified instances file while reporting activity or calculating power for the entire design.
Power Nets	Enables power profiling for the specified power net(s).
Align with Signal	Starts profiling at the first rise or fall of the signal. Select *rising* to start profiling at the first rising edge. Select *falling* to start profiling at the first falling edge.

Related Text Commands

For information on the following command, see "Power Calculation Commands and Attributes" in the *Text Command Reference*:

- `report_vector_profile`

Run Power Analysis - Activity



Global Activity	Specifies the average number of times that all unset nodes switch in a clock cycle. If not specified the fastest domain frequency will be used unless one turns off clock domains. There is no default.
Hierarchy(s)	A hierarchical name that the *Global Activity* is being assigned to. If not provided the whole design is assumed. Selecting the *Add* button adds hierarchical activity information to a list. The *Remove* button removes a selected item in the list. To highlight multiple items, click them while pressing either the *Shift* or *Control* key.
Activity *Transition Density*	Specifies whether *Activity* or *Transition Density* numbers will be used when supplying *Net*, *Pin*, or *Port* activities.
Net *Port* *Pin*	Specifies that the activity numbers are for a *Net*, *Pin*, or *Port*.

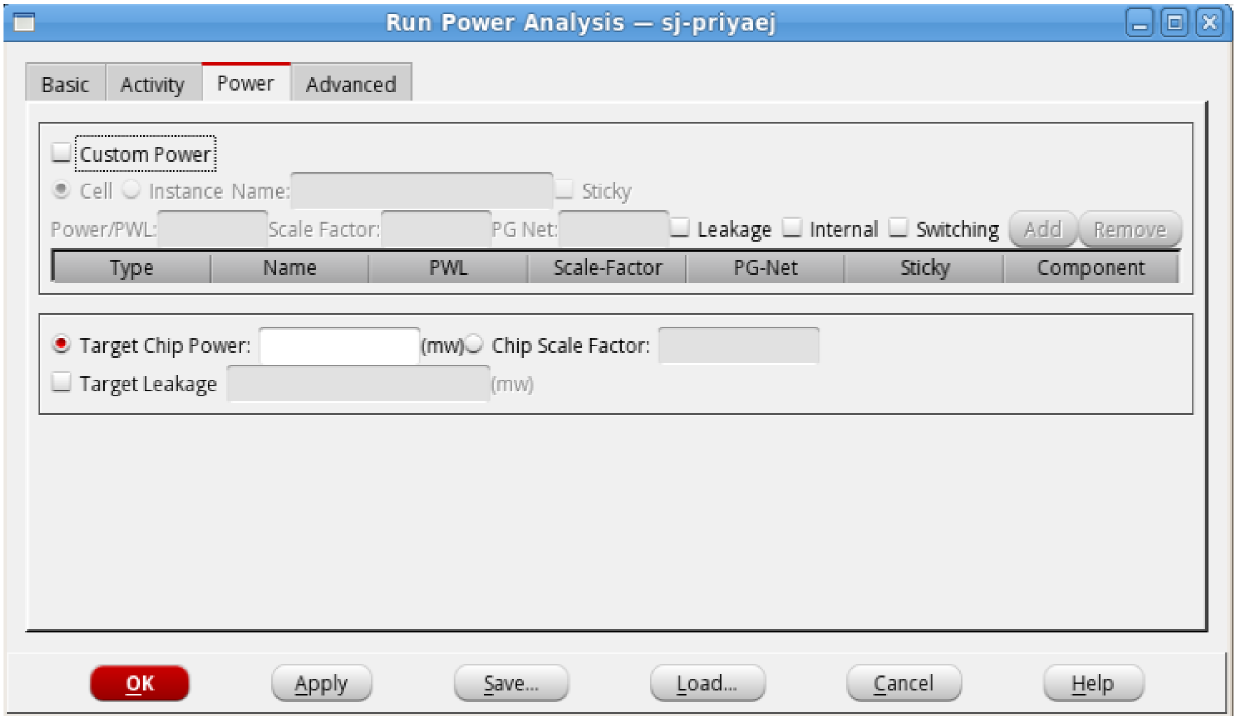
Name	Name of the Net, Pin, or Port.
Activity/Td	The *Activity* or *Transition Density* value based on which of these two was selected.
Duty *Period*	Duty cycle and Period for the named Net, Pin, or Port. Duty is the fraction of time that a net, pin, or port has a value of 1.0 A duty cycle of 0.25 has a value of one 25% of the time. By selecting *Add* adds the supplied information to the list. Selecting *Remove* deletes selected items on the list. To highlight multiple items, click them while pressing either the *Shift* or *Control* key.
Period	Period for the named Net, Pin, or Port.
TCF	TCF file.
SAF	SAF file
SAF Scope	Scope of SAF file if *SAF* is selected.

Related Text Commands

For information on the following command, see "Power Calculation Commands and Attributes" in the *Text Command Reference*:

- `set_default_switching_activity`

Run Power Analysis - Power



Fields and Options

Custom Power	When selected it activates the *Power/PWL* and *PG Net* fields for adding Cells
Cell	Specifies that the *Custom Power* information is for a cell.
Instance	Specifies that the *Custom Power* information is for an Instance.
Name	The name of the cell or instance. Must be provided.
Sticky	Applies the simulation-based PWL waveform as is to the specified cell/instance.

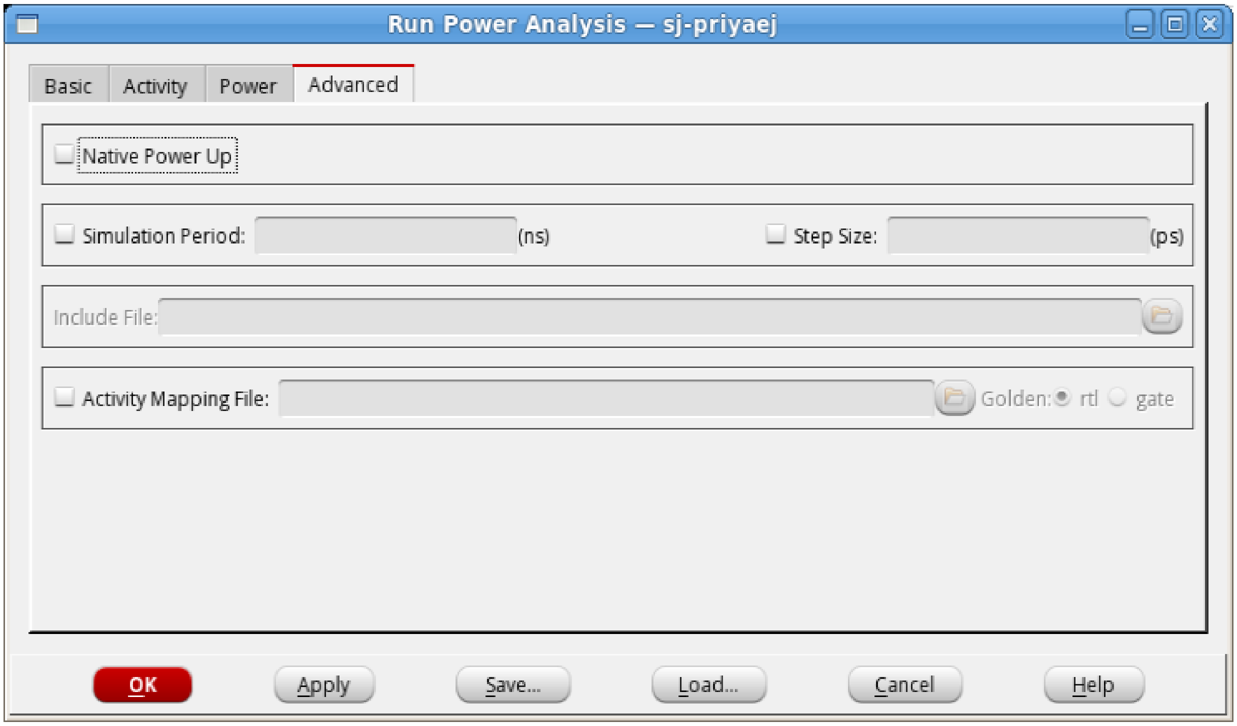
Power/PWL	After selecting *Custom Power, Cell* or *Instance*, the *Power/PWL* and *PG Net* fields can be entered. By selecting the *Add* button this information is added to the list. The *Remove* button deletes any selected items that were previously added to the list. To highlight multiple items, click them while pressing either the *Shift* or *Control* key.
Scale Factor	Specifies to scale the power value by the specified scale factor. You can use this option to specify the scale factor for specific cells and instances.
PG Net	Specifies the name of the power rail.
Leakage	Specifies the target leakage power of the design, cell, or instance. To specify leakage power for cells and instances, you can use the *Leakage* option in conjunction with the `Cell` or *Instance* option.
Internal	Specifies the target internal power of the design, cell, or instance. To specify internal power for cells and instances, you can use the *Internal* option in conjunction with the `Cell` or *Instance* option.
Switching	Specifies the target switching power of the design, cell, or instance. To specify switching power for cells and instances, you can use the *Switching* option in conjunction with the `Cell` or *Instance* option.
Target Chip Power	Specifies the power for the entire design or rail, in milliwatts (mW).
Chip Scale Factor	Scales the power value by the specified scale factor.
Target Leakage	Sets the total target leakage power of the entire design in milliwatts (mW).

Related Text Commands

For information on the following command, see "Power Calculation Commands and Attributes" in the *Text Command Reference*:

- `set_power`

Run Power Analysis - Advanced



Fields and Options

Native Power Up	Specifies to enable the native power up flow.
Simulation Period	The simulation period that dynamic rail analysis will be performed.
Step Size	Specifies the transient time step size or resolution.
Include File	Adds Design and ChipPwr PowerMeter objects. See *VoltageStorm PowerMeter Manual* from ANLS release for details in creating this include file.

Activity Mapping File	Specifies the rtl2gate mapping file which contains instance name mapping between RTL netlist and GATE level netlist. RTL level VCD or TCF are obtained from simulation on RTL Verilog netlist. Power analysis uses this instance name mapping to annotate the output nets of this instance from the pin based RTL, VCD, or TCF. By default, this option is always selected when either VCD/TCF is specified.
Golden • *rtl* • *gate*	Specifies whether *rtl* or *gate* is *Golden*. The one not specified as golden will be considered as Revised. Currently the Conformal MatchPoint file does not specify this. *Default*: *rtl*

Rail Analysis

The Rail Analysis contains the following items:

- PowerGrid Library
    - Set PG Library Mode form
    - Generate PG Library form
- Rail Analysis
    - Set Rail Analysis Mode form
    - Run Rail Analysis form
- Create Hierarchical View
    - Create Hierarchical View form

PowerGrid Library

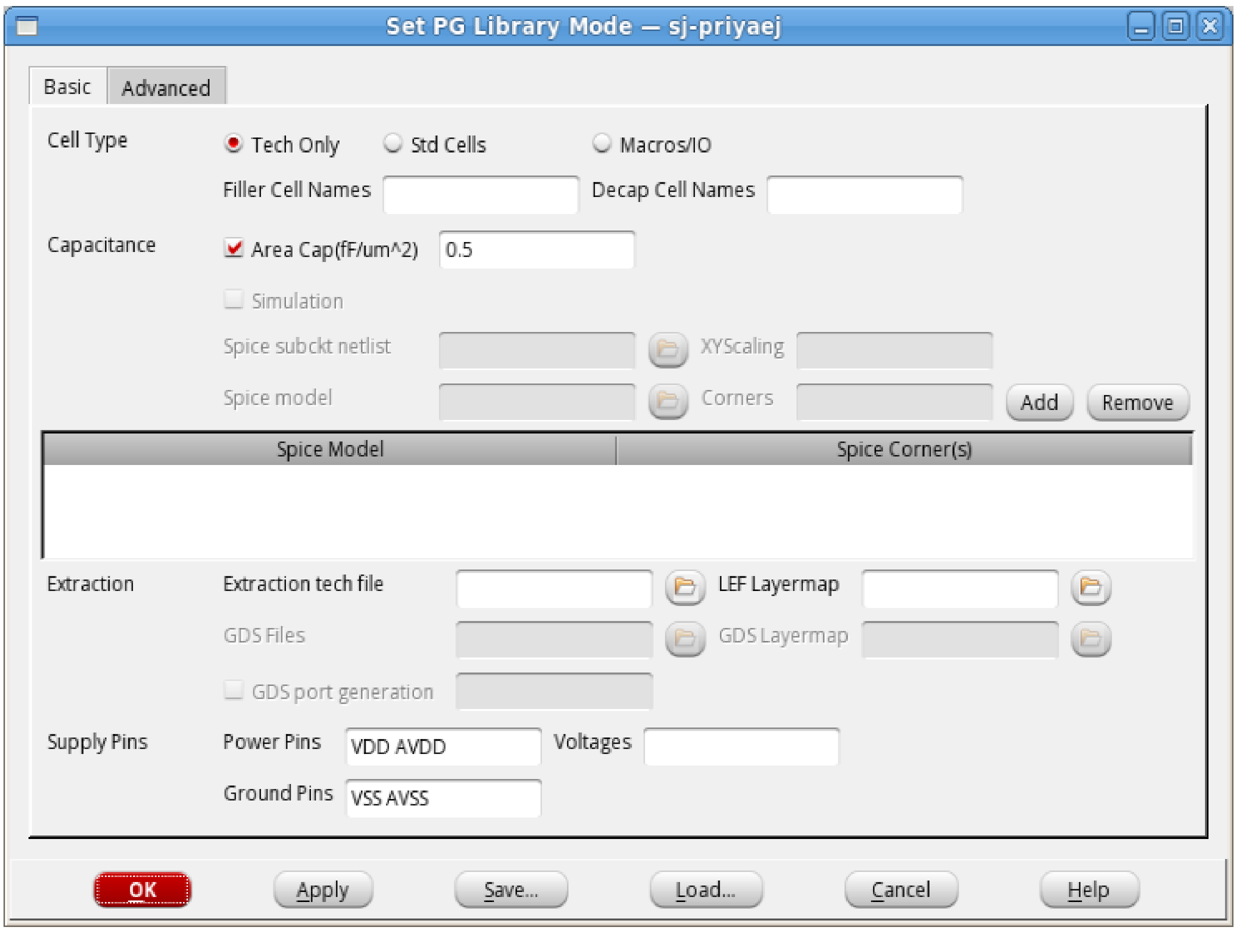
Power Grid Library contains the following items:

- Set PG Library Mode - Basic

- Set PG Library Mode - Advanced
- Generate PG Library

Set PG Library Mode - Basic

Specifies what kind of power-grid library will be created. This form is used to define the type of input and configuration for generating power-grid libraries.



Fields and Options

Cell Type	Specifies the cell type used for library creation. The choices are *Tech Only*, *Std Cells*, *Macros/IOs.* The default is *Tech Only*. • *Tech Only* Creates a technology Library that contains the tech file, area capacitance specification, decap/filler/powergate cells, and Tech view for all the cells. A technology library is a requirement for running rail analysis. • *Std Cells* Generates a power-grid library for all the standard cells using the Spice netlist. The stdcells power-grid library does not contain the tech file. Power-grid is connected at the LEF pin, and all the capacitance are derived from simulation. The power-grid library contains three kind of power-grid views (PGVs), Early/IR/EM, and the views are selected based on the accuracy mode of rail analysis. • *Macros/IOs* Generates a power-grid library for memory, I/Os and macros using the Spice and GDS netlist. GDS is mandatory for the cell type macros. The `macros` power-grid library does not contain the tech file. Power-grid is connected down to contact/specified via, and all the capacitance are derived from simulation. The power-grid library contains three kind of PGVs, Early/IR/EM, and the views are selected based on the accuracy mode of rail analysis.
Filler Cell Names	Lists the names of the filler cells that have no GDS data. Wildcards (*) can be used. These cells can be swapped out for decaps during decap optimization.
Decap Cell Names	Specifies the names of cells that have explicit decoupling capacitance for use in decap optimization. These cells are nearly equivalent to filler cells, except that there is typically an active device between the power and ground nets to provide extra decoupling capacitance. Power-grid view library generation uses this list of cells to ensure that a capacitance value is associated with each cell. If no capacitance is associated with a cell, a warning message will be issued. Wildcards (*) can be used.
Capacitance	

Area Cap (fF/um^2)	Specifies the default amount of area based decoupling capacitance in a cell. This option is enabled for the cell type: *Tech Only*.
Simulation	Specifies that the capacitance is derived from netlist simulation. This option is enabled for the cell types: *Std Cells* and *Macros/IOs*.
Spice subckt netlist	Specifies the names of the SPICE netlist files containing the subcircuits corresponding to the cells being processed during power-grid library generation. These subcircuit netlists will be used to calculate pin capacitances using Voltus library simulator.
XYScaling	Specifies the current region scale factor for the Netlist-based flow. The current region scale factor is the factor by which the netlist coordinates are scaled before finding the closest node to attach the tap currents.
Spice Model	Specifies the names of the SPICE model files used by the SPICE netlist file.
Corners	Specifies a list of SPICE corners. This field is optional. If you specify SPICE corner(s), the number of corner items should be equal to the number of SPICE model files specified in the *Spice Model* field.
Extraction	
Extraction Tech File	Specifies the name of the technology file that will be used for extraction.
LEF Layermap	Specifies a file that provides the mapping of layers between the LEF and technology file.
GDS Files	Specifies the names of the GDSII files used during power-grid library generation.
GDS Layermap	Specifies a file that provides the mapping of layers between the LEF and GDS files.
GDS Port Generation	Identifies the layer name that library generation uses to compute the placement bounding box for GDSII cells that are placed by the DEF file.
Supply Pins	
Power Pins	Specifies the names of the nets considered power nets for all cells for which the power nets are not specified.
Voltages	Specifies the voltages for the power pins.

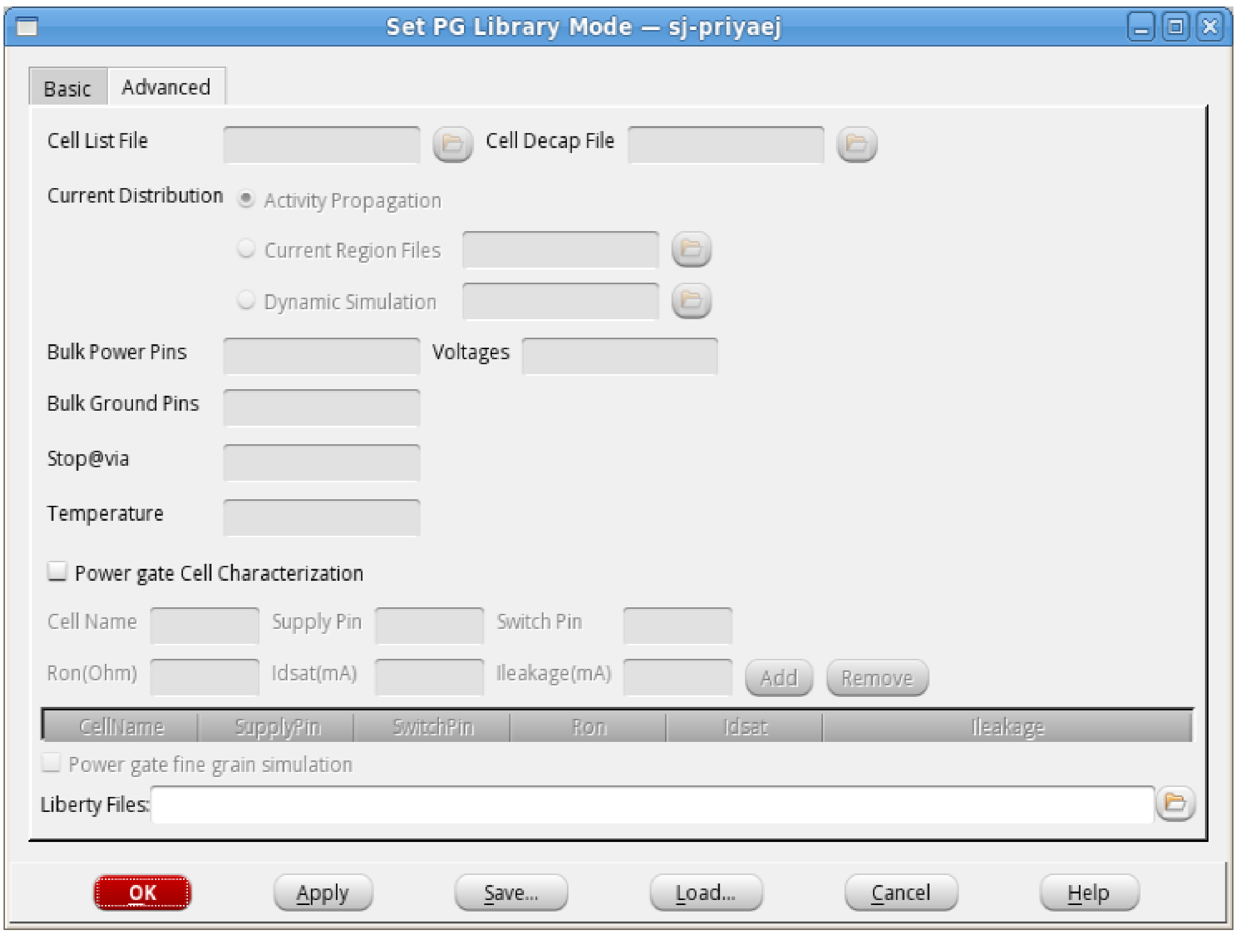
Ground Pins	Specifies the names of the nets considered power nets for all cells for which the power nets are not specified.

Related Text Commands

See `set_pg_library_mode` and `set_advanced_pg_library_mode` command in the Text Command Reference.

Set PG Library Mode - Advanced

Specifies the advanced power-grid library generation features.



Fields and Options

Cell List File	Specifies a file containing a list of cells that will be processed. The *Cell List File* field is required when celltype *Macros/IOs* is selected. The program spawns the library generation job in serial mode for each macro in the cell list file. A separate library for each macro is generated. This facilitates debugging when library generation of any macro fails. It also helps in improving the overall performance.
Cell Decap File	Specifies the name of a file containing a list of cells and the decoupling capacitance value for each.
Current Distribution	Specifies the method of current distribution inside the cell. • **Activity Propagation** uses Voltus library simulator to determine the propagation activity to distribute the current. • **Current Region Files** specifies the amount of current to distribute within a cell region. • **Dynamic simulation** uses a trigger file to run detailed analysis to determine current distribution.
Bulk Power Pins	Specifies the names of nets that connect transistor bulk terminals to the power net. This information is used to prevent any current from being assigned to these nets. If a net is connected to any transistor terminals other than a bulk terminal, you must specify that net in the *Power Pins* field.
Voltages	Specifies the voltages for the bulk power pins.
Bulk Power Pins	Specifies the names of nets that connect transistor bulk terminals to the ground net. This information is used to prevent any current from being assigned to these nets. If a net is connected to any transistor terminals other than a bulk terminal, you must specify that net in the *Ground Pins* field.
Stop@via	Stops the extraction of the power-grid network inside a cell at the specified via layer.
Temperature	Specifies the temperature in degree celcius used in library characterization for thermal aware EM/IR analysis.

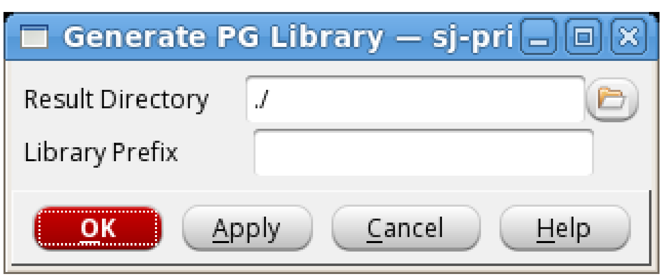
Power Gate Cell Characterization	Specifies the information that power-grid library generation needs to create a port power gate view. Specifies the cell name, the unswitched power pin, the switched power pin, the on resistance in ohms, the saturation current in milliamps, and the leakage current in milliamps. If *Ron*, *Idsat*, or *Ileakage*,values are specified, they will be used to override the data extracted by Thunder.
Cell Name	Specifies the power gate cell name.
Supply Pin	Specifies the power gate supply pin (unswitched power pin).
Switch Pin	Specifies the power gate switched power pin.
Ron (ohms)	Specifies the power gate on resistance.
Idsat (mA)	Specifies the power gate saturation current.
Ileakage (mA)	Specifies the power gate leakage current.
Power gate fine grain simulation	Specifies to enable finegrain powergate simulation.

Related Text Commands

See `set_pg_library_mode` and `set_advanced_pg_library_mode` command in the Text Command Reference.

Generate PG Library

Generates the output for power-grid library generation.



Fields and Options

Result Directory	Generates the output for power-grid library generation in the specified directory.
Library Prefix	Specifies a prefix for the power-grid library. When this option is specified, the default PGV for each cell type is as follows: • techonly - `prefix_techonly.cl (default: techonly.cl)` • stdcells - `prefix_stdcells.cl (default: stdcells.cl)` • macros - `prefix_cellname.cl (default: macros_cellname.cl)`

Related Text Commands

See `generate_pg_library` command in the Text Command Reference.

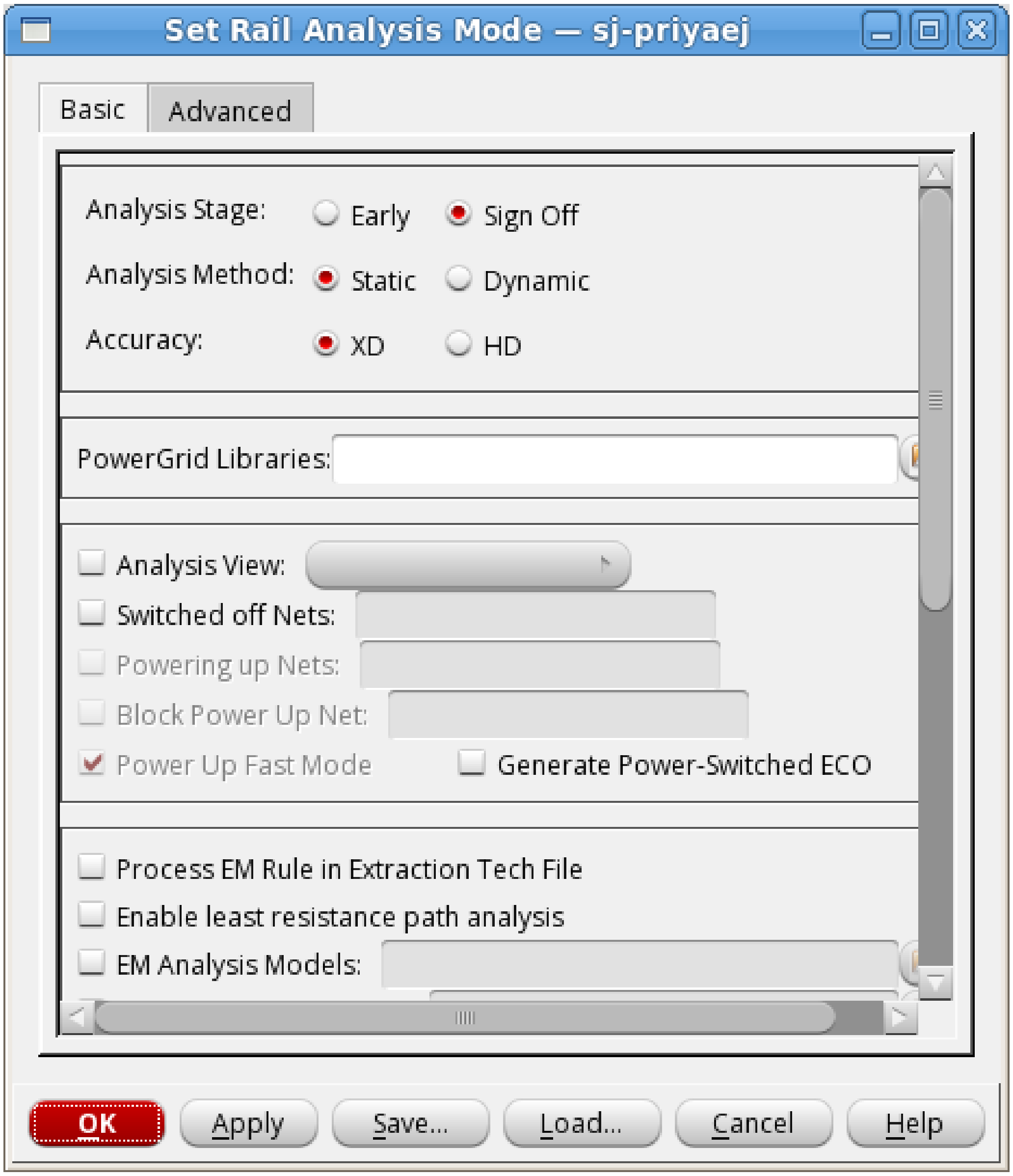
Set Rail Analysis Mode

The Set Rail Analysis Mode form includes the following:

- Set Rail Analysis Mode - Basic
- Power Grid Library Directories
- Set Rail Analysis Mode - Advanced
- Create Current Region

Set Rail Analysis Mode - Basic

Sets whether static or dynamic rail analysis should be performed along with some related parameters.



Fields and Options

Analysis Stage	Specifies whether early rail analysis (*Early*) or signoff (*Sign Off*) rail analysis will be done. If you select *Early*, the *XD* mode is selected by default and *HD* mode is disabled. *Default*: `Sign Off`

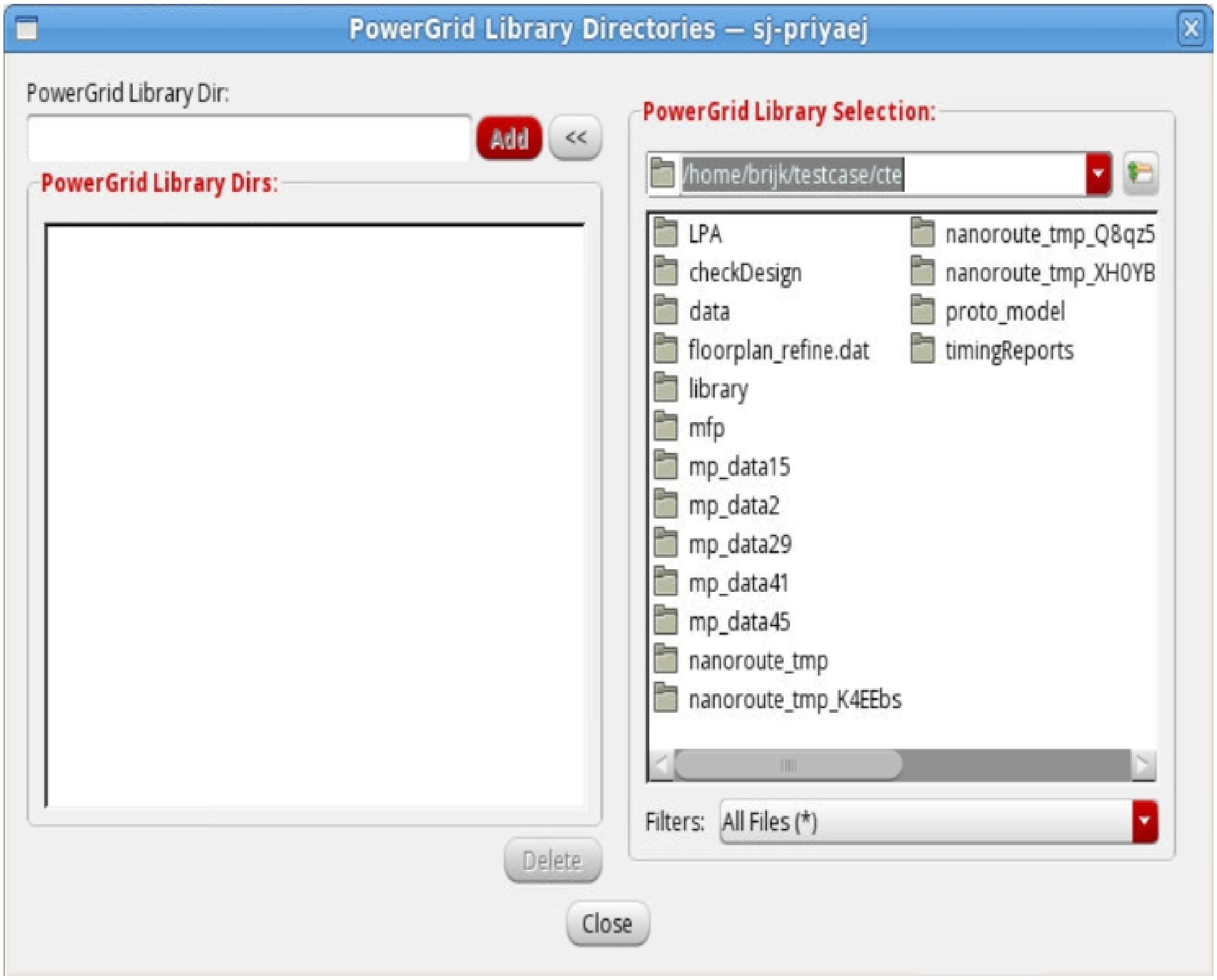
Analysis Method	Specifies whether static or dynamic analysis will be done. *Default*: static
Accuracy	Specifies the accuracy mode of analysis. • `XD (accelerated definition)` – use for early implementation stage IR/EM analysis • `HD (high definition)` – use for final verification stage IR/EM analysis *Default*: `XD`
PowerGrid Libraries	Specifies the name of the power-grid view library directories. If you select the folder icon, the Set Rail Analysis form appears, which will be used to select and add the appropriate files.
MMMC View	Specifies the Mult-Mode Multi-Corner (MMMC) view.
CPF mode	Specifies Common Power Format (CPF) mode.
Switched off Power Nets	Specifies a list of nets to exclude from analysis.
Powering up Nets	Specifies a list of powering up nets.
Block Power Up Net	Specifies a net for block power-up analysis.
Generate Power-Switched ECO	Specifies that a power switch eco file should be created. *Default*: false
Process EM Rule in Extraction Tech File	Processes the EM rules defined in the extraction technology file. When *Process EM Rule in Extraction Tech File* is specified with *Extraction Tech File*, the extraction technology file will be processed. If *Process EM Rule in Extraction Tech File* is specified without *Extraction Tech File*, the .cl model will be processed.

Enable Least Resistance Path Analysis	Enables least resistance path analysis for all the instances in the design.
EM Analysis Models	Specifies the name of a file that includes the electromigration (em) models.
ICT-EM Analysis Models	Specifies the ICT-EM file which only contains the EM rules and excludes the RC extraction data in ICT. The software will use the EM rules in the specified ICT-EM file to calculate EM limits for power net EM analysis even if there are embedded EM rules in the Quantus QRC tech file.
Default Package	Specifies the default resistance, inductance and capacitance values of the package to be used for RLC model.
Source Search Distance	Specifies the search distance in microns(u) for adding voltage sources at power pin locations. *Default*: 50um
Extraction Tech File	Specifies the extraction technology file to be used for top-level power-grid extraction. If you do not specify this field, the software will use the extraction technology file stored inside the power-grid view library.
Thermal Map	Specifies to process the thermal map file generated for QRC to calculate resistance based on uniform temperature. *Default*: Not selected.
Generate Movies	Used to specify that dynamic movies will be created. For dynamic only. *Default*: true
Save Voltage Waveforms Files	
	Saves voltage waveform files in the state directory of analyzed net(s) to feed to SPICE critical path analysis and Substrate Noise Analysis. *Default*: Not selected. This option is disabled in the *Static* mode.

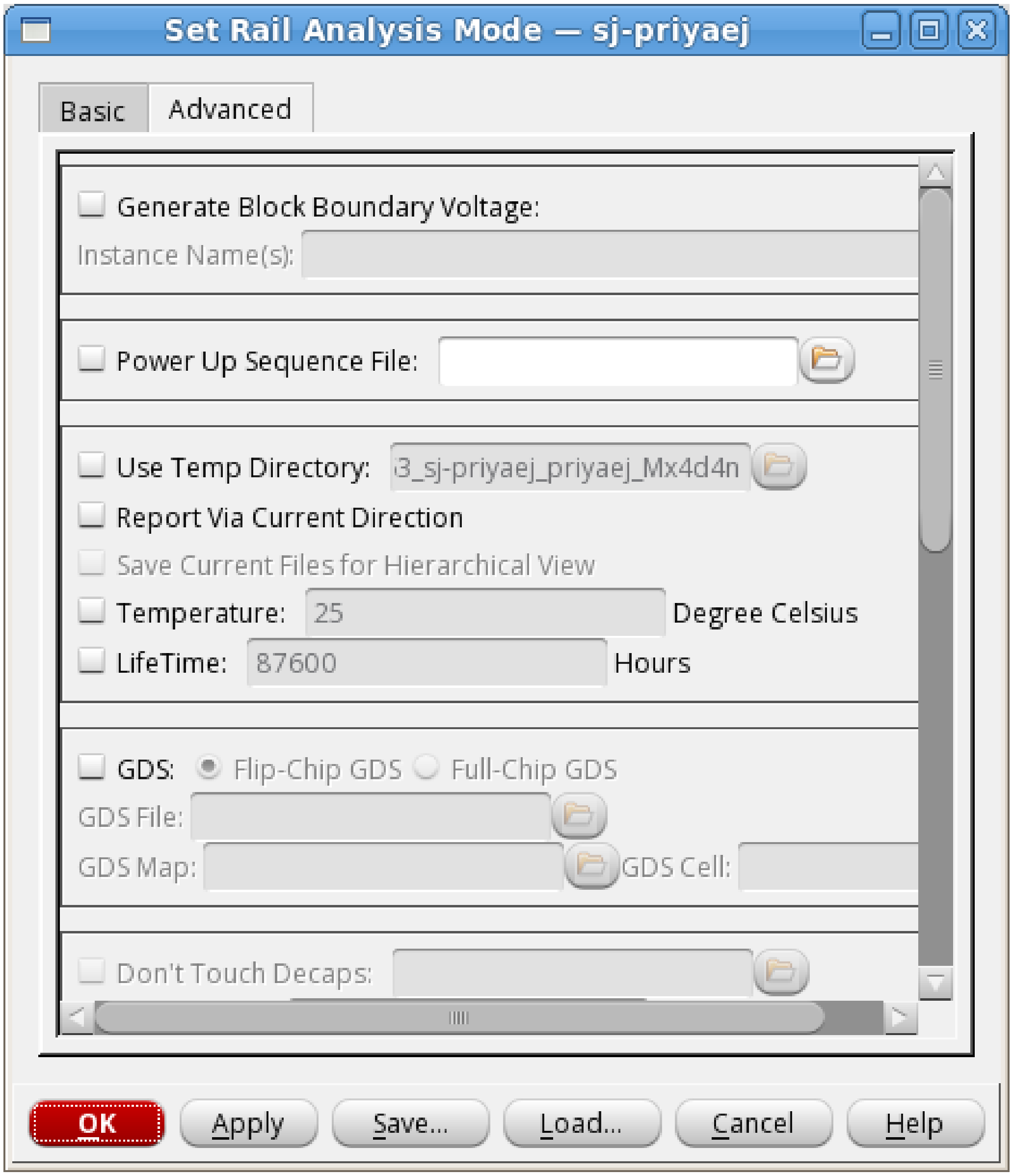
Decap Optimization Method	Specifies the decap optimization method to use. For dynamic only. Choices are *Placement-Aware* and *Timing-Aware*, *Area based*, and *Removal*. *Default*: *Area based*.
Decap Removal Method	Choices are *Conservative* and *Aggressive*. Used with *Removal* option of *Decap Optimization Method*. *Default*: *Aggressive*
Maximum Leakage Current	Specifies the maximum leakage current in A, for placement-aware and timing-aware decap optimization methods.
Generate Decap ECO	Specifies that a decap eco file should be created.
Generate reduced die model:N-port	
	Creates n_port_freq_domain as well as n_port_time_domain die-models simultaneously.

Power Grid Library Directories

A form such as the one shown below appears when the folder icon is selected from a menu. Selecting the folder icon on this form will toggle the Selection part of the form. To add items, select a file, and then select the *Add* button. To add multiple items from the selection list, select the first item, then move the cursor to the last item and hold down the shift key while selecting the last item. The *Delete* button can be used for deleting items. Similarly the shift key can be used for deleting multiple items.



Set Rail Analysis Mode - Advanced



Fields and Options

Generate Block Boundary Voltage	Generated the voltages on the block pins. This data can be used for doing rail analysis at the next level up in hierarchy.

Instance Name(s)	The name of the instance that the block boundary voltages will be generated for.
Use Temp Directory	Specifies a directory to use for temporary files.
Report Via Current Direction	Determines that the current direction of vias will be reported. *Default*: false
Save Current Files for Hierarchical View	Determines whether Voltus automatically saves current files. *Default*: false
Temperature	Specifies the temperature in degree celcius during rail analysis. The default temperature is 25 degree celsius.
Lifetime	Specifies the lifetime value in hours. *Default*: 87,600 hours
GDS	Specifies that a GDS file will be used.
Flip-Chip GDS	Specifies that the gds data is for flipchip.
Full-Chip GDS	Specifies that the gds data is for full chip.
GDS File	Specifies the name of the gds file.
GDS Map	Specifies the name of the gds map file.
GDS Cell	Specifies the name of the gds top cell.
Don't Touch Decaps	Specifies the decaps that will not be removed. For dynamic only and used if option: -decap_opt_method removal is set.
Decap Cells	Specifies the decap cells that will be used during decap optimization. This option is used when the decap cells are not tagged in the power-grid library. For dynamic only.

Filler Cells	Specifies the filler cells that will be used during *Placement- Aware* or *Timing-Aware* decap optimization. This option is used when the filler cells are not tagged in the power-grid library. For dynamic only.
Decap ECO	Specifies the name of the decap ECO file for domain based analysis that will be created after decap analysis is performed. This file is generated in `decap_opt/addcap.cmd` in the state directory. For dynamic only.
Specify Current Region	Specifies a file that includes a list of regions and the amount of current to be distributed within them for the power-grid. This field will be enabled only if you select *Early* analysis stage in the *Set Rail Analysis Mode - Basic* tab. If you select this checkbox, the *Create* button is enabled that lets you create current regions for Static and Dynamic analysis. Click *Create* to view the Create Current Region form. Default units in file are `mA`. You can also specify rectilinear current regions in the file.
Power Gate File	Specifies the name of the power gate (power switch) file that will be used to perform power gate steady-state analysis. This field will be enabled only if you select *Early* analysis stage in the *Set Rail Analysis Mode - Basic* tab.
Layer Mapping File	Specifies the layer map file to generate a port view. If a layer map file is not provided, it would be automatically inferred by the tool. This field will be enabled only if you select *Early* analysis stage in the *Set Rail Analysis Mode - Basic* tab.
Skip Layer (Pair)s for Virtual Via Insertion	Specifies to skip via insertion between stripes and non-stripes, on the specified LEF layer pairs. This field will be enabled only if you select *Early* analysis stage in the *Set Rail Analysis Mode - Basic* tab.

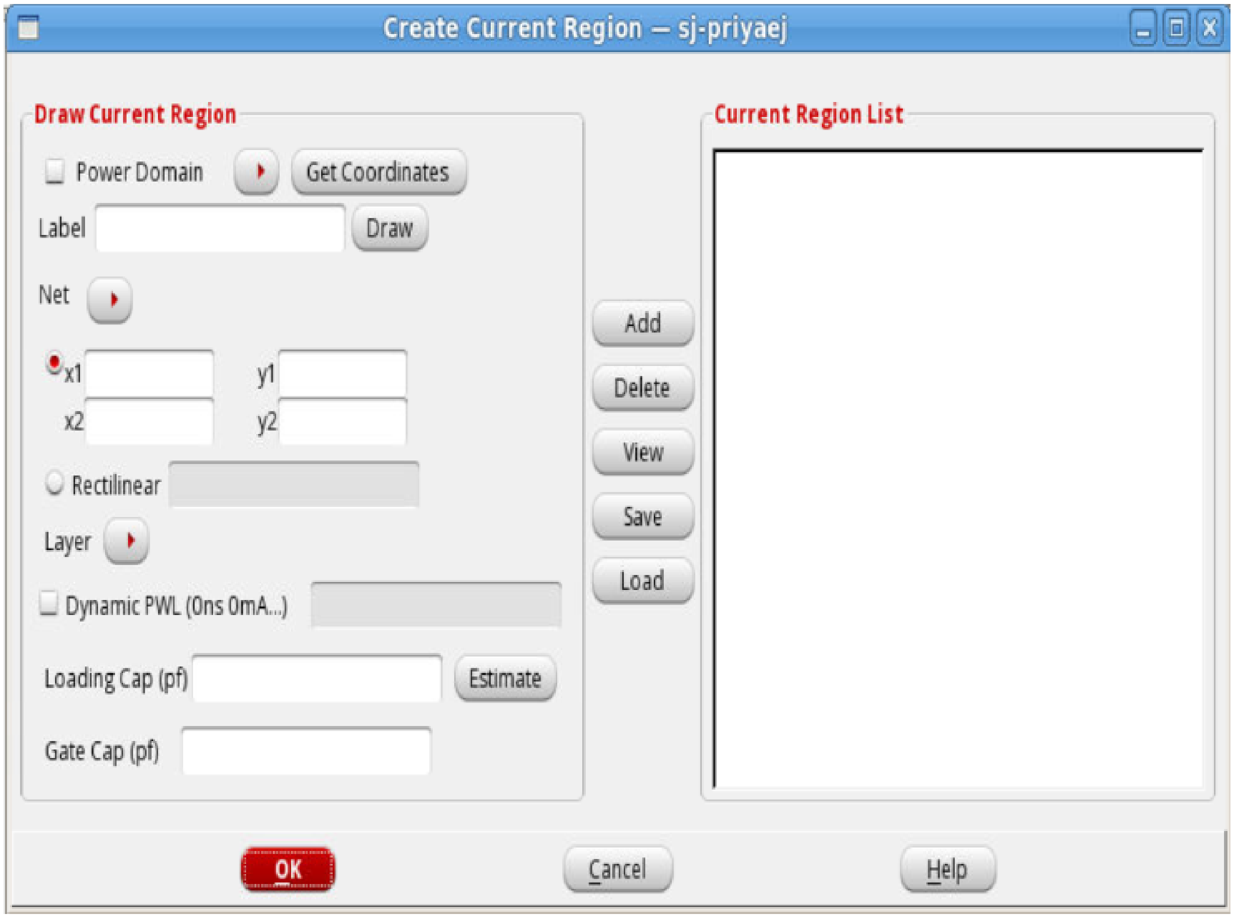
Skip Virtual Via Insertion for Shape Type	Specifies to skip a given via type. By default, ERA generates all virtual via layer types. ***whatif*** - vias are virtual vias that have connectivity to user-defined what if shapes. ***def*** - vias are virtual vias between two metal shapes defined in DEF. ***all*** - will skip all virtual via generation.
Current Distribution Layer for Unplaced Instances	Specifies the layer name for distributing unplaced current in the early rail analysis mode. This field will be enabled only if you select *Early* analysis stage in the *Set Rail Analysis Mode - Basic* tab.
Enable Current Distribution for	Controls the behavior of era current distribution. `set_power_data area` based power, or `current_region_file` need to be specified for ERA current distribution to work. Placed instanced without uti or ascii based power can also be considered for era current distribution. • ***Unplaced***: Enable current distribution only for unplaced instances. If set_power_data area based power is specified, -era_current_distribution_layer will be required. • ***Placed***: Enable current distribution for placed instances without any power specified. • ***All***: Both unplaced and placed instances without power specified; will have ERA current. • ***None***: Disable ERA current distribution. This field will be enabled only if you select *Early* analysis stage in the *Set Rail Analysis Mode - Basic* tab.
Virtual Followpin Insertion	Generates virtual followpins. The `extended` followpins will create followpins that extend from one stripe to another. The `standard` followpins may extend to previous stripe but does not reach the next stripe. This field will be enabled only if you select *Early* analysis stage in the *Set Rail Analysis Mode - Basic* tab.

Current Distribution Factor for Placed Macros	When you use *Distribute Current for Placed Instance* or *Generate Current Region File for Unplaced Area*, the ratio of power allocated to each macro/block is calculated based on its total area. This field controls the current distribution factors for the placed instances, hence power allocated for area-based power calculation. For example, if you specify 0.5, the software will assume all placed instances to be 50% of its actual size and distribute current accordingly. This field will be enabled only if you select *Early* analysis stage in the *Set Rail Analysis Mode - Basic* tab.
Ignore Shorts	Specifies to perform sign-off mode extraction while ignoring shorts, extract each net per geometry defined in LEF/DEF and honor manufacturing effects. This option allows you to ignore shorts and continue sign-off mode extraction.
Enable Manufacturing Effects	Specifies to honor manufacturing effects during static or dynamic analysis.

Related Text Commands

See `set_rail_analysis_mode` command in the *Text Command Reference*.

Create Current Region



Fields and Options

Draw Current Region	Specifies the coordinates of the region, the layer, and the static current. The *Add* button can be selected to add the region to the *Current Region List*. The *Delete* button will delete a selected item on the list. *Label* specifies a name for the region. If not specified, Innovus will provide a name (region1, region2...) *Net* specifies the power/ground net name for domain-based analysis. This option allows you to specify current region values for a specific net. *x1*, *y1*, *x2*, and *y2* specifies a rectangular region that the current will be distributed within. *Rectilinear* specifies the rectilinear current region that the current will be distributed within. **Note:** In the static mode, ERA splits the rectilinear region into several rectangular regions and distributes current to the rectangular regions based on the area. In the dynamic mode, you can specify rectilinear regions interactively in the layout canvas by selecting the *Draw* button. You can select a rectlinear region by clicking each vertex of the rectlinear in sequence (clockwise or counter-clockwise), and then pressing the *ESC* key on the keyboard. This will quit the point selection mode, and the selected points appear in the *Rectlinear* field. Current in rectangular region = Area of the rectangle / Area of the rectilinear *Layer* specifies the metal layer that the current sink will be placed on. If you select *Draw*, then select a box in main window, the coordinate of this box will be automatically populated in the x1 y1 x2 y2. If you select *View* after selecting an item in the list, the selected region will be displayed in the main window.
Dynamic PWL (0ns 0mA...)	Specifies the dynamic PWL for regions without any placed instance, in time (in ns) and current (in mA) format. For example, 0ns 0mA 0.5ns 1mA 1ns 2mA 3ns 1mA 4ns 0. This option is displayed only if you select the analysis method *Dynamic*.
Loading Cap (pf)	Specifies loading capacitance in pf (picoFarads) waveform for the current region(s). This option is displayed only if you select the analysis method *Dynamic*.
Estimate	Estimates Gate Capacitance (C1) and Loading Capacitance (C2) values for the specified current regions. These estimated values of C1 and C2 are used along with the PWL current waveform for the regions to perform dynamic rail analysis. This option is displayed only if you select the analysis method *Dynamic*.

Gate Cap (pf)	Specifies gate capacitance in pf (picoFarads) waveform for the current region(s). This option is displayed only if you select the analysis method *Dynamic*.
Current Region List	Displays the current region list. This is created by specifying the *Draw Current Regions* information and selecting *Add*. Selecting an item on the list and then *Delete* will delete the selected item.

Related Text Commands

See `set_rail_analysis_mode` command in the *Text Command Reference*.

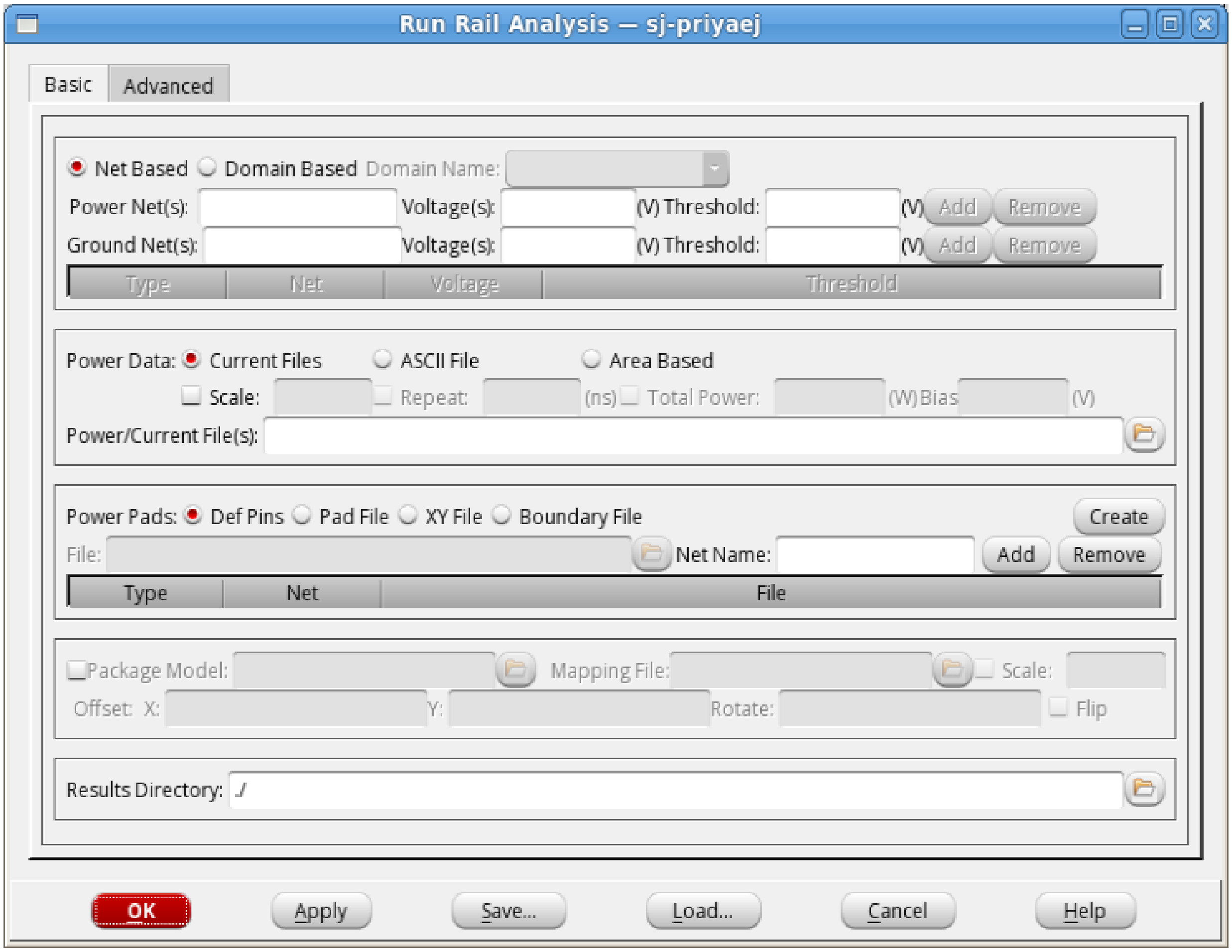
Run Rail Analysis

The Run Rail Analysis form has two pages:

- Run Rail Analysis - Basic
- Edit Pad Location
- Run Rail Analysis - Advanced

Run Rail Analysis - Basic

Runs rail analysis using the provided parameters.



Fields and Options

Net Based	Set if net based analysis is being run.
Domain Based	Set if domain based analysis is being run.
Domain Name	Name of the power domain that rail analysis will be performed on. Only used for domain based analysis.
Power Net(s)	Name of the power nets that the rail analysis will be performed on.
Voltages	The voltage of the power net.

V Threshold	The voltage threshold of the power net
Ground Net(s)	Name of the ground nets that rail analysis will be performed on.
Voltage(s)	The voltage of the ground net.
V Threshold	The voltage threshold of the ground net.
Add	Click the *Add* button to add details of a specific net to the power/ground nets table for domain-based analysis.
Remove	Click the *Remove* button to remove details of a specific net from the power/ground nets table for domain-based analysis.
Power Data	The power data will be supplied by Current Files, an ASCII file or will be area based.
Scale	Specifies a scale factor to apply to the current data. You can use this parameter to scale currents to a more optimistic or pessimistic power-consumption estimate. This parameter is only for `-format current` and `-format ascii`.
Repeat	Repeats the dynamic current waveform for the specified time. You must ensure that the stop time for dynamic analysis is also specified and it matches the repeat duration. This option is only available for current format files during dynamic analysis. The repeat option can be used when multiple current files have different simulation periods or when IR drop analysis needs to be run for longer duration. *Default units*: `ns`.
Total Power	Specifies the power per area in watts. Only required for option `-format area`.
Bias	The value of the bias voltage. This parameter is only for `-format ascii` and `-format area`.
Power File(s)	Specifies the name of the power data files. The file is optional if `-format area` is specified.

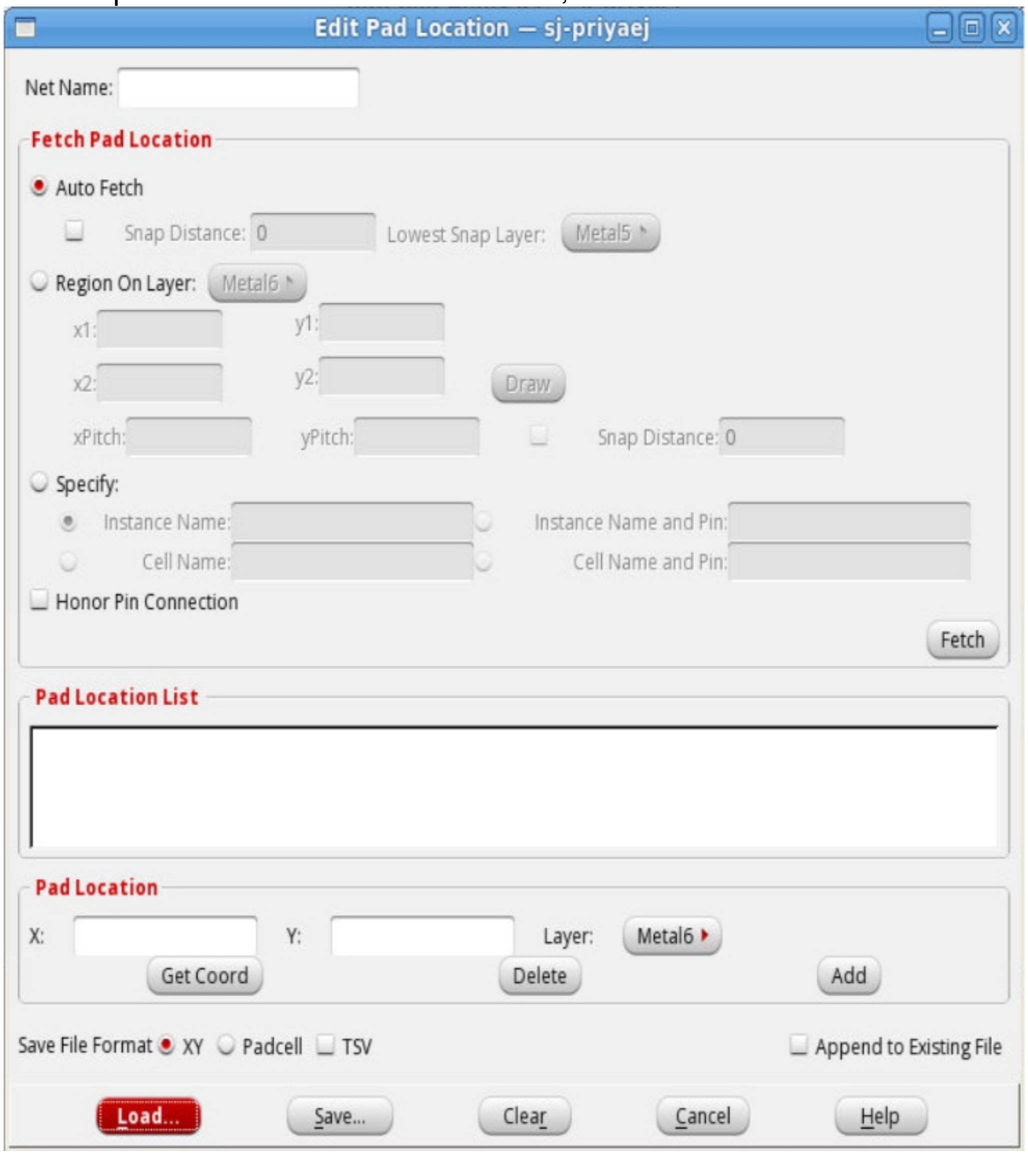
Power Pads	*XY*File specifies that voltage sources will be specified by x y coordinates. *Def Pins* specifies that voltage sources will be determined by power pins. *Pad File* specifies that voltage sources will be determined by pad cells given in the file. *Boundary File*specifies that voltage source locations will be specified by information in the boundary file. *Default: Def Pins*
File	The name of the power file.
Net Name	The name of the power net. The *Add* button adds the net to the list. The *Remove* button removes the net from the list. To highlight multiple items, click them while pressing either the *Shift* or *Control* key.
Package Model	Specifies a file containing a SPICE subcircuit describing the package model. This file is generated by Allegro Package SI (also known as APE3D from Cadence) or other package-modeling products.
Mapping File	Specifies the name of the package terminal mapping file, which contains the mapping of the terminals of the SPICE subcircuit in the package model file (Specified by the *Package Model* field above) to the locations at the grid or top-level pins.
Offset X *Offset Y*	Specifies the lower left and upper right points coordinate of the die.
Rotate	Specifies the rotation angle of the die. The possible values are: 0/45/90/135/180/225/270/315. Rotation is always in the counter clockwise direction from the original point.
Flip	Specifies to flip the die along the Y axis.
Results Directory	The directory where the rail analysis output will be saved.

Edit Pad Location

Use the Edit Pad Location form to create or edit power pad location files (one for each power net) to mark points on the power structures as voltage source reference points. Power pad location files identify the voltage source reference points, such as VCC, VDD, and VSS. You can use these files during all stages of power analysis.

Note: Pad location displays are updated immediately after clicking *Auto Fetch*, *Delete*, or *Add*. The IR drops leading from the pad locations are displayed after running power analysis.

→ To open the Edit Pad Location form, click the *Create* button in *the Run Rail Analysis* form



Fields and Options

Net Name	The power net or ground net name of the pad cells. This field is required only when the file format is `Padcell`. **Note:** You can only edit the pad location file for one net at a time.
Fetch Pad Location	
Auto Fetch	Specifies to fetch all voltage sources. If you select this option, you must specify the net name.
Snap Distance	Specifies the distance of snapping distance constraint from IO/pad pins. The default value is 0. When selected , the software performs autofetch with snapping.
Lowest Snap Layer	Specifies the lowest layer used to fetch a DC source. Use a value such as 1 or 2. The default value is 5.
Region	
	Specifies a rectangular region that the current will be distributed within. A grid is created by using the *xPitch* and *yPitch* within the specified region. The current will be specified at each of the intersecting pitch lines. *Layer*specifies the metal layer that the current sink will be placed on. If you click *Draw*, and then select a box in the main window, the coordinate of this box will be automatically populated in the x1 y1 x2 y2. For region-based auto fetch, if the voltage source points that were fetched according to the start point and the specified region pitch (xPitch/yPitch) are not on the stripe, these points will be ignored during analysis. You can use the *Snap Distance* option to snap the voltage sources to a stripe within +/- snap distance/2. If no such stripe is found, this point will not be saved into the pad location file. As a result, the voltage sources are generated only on the stripes and these points will be saved to the pad location file.
Specify	Specifies an instance/cell and their pins to autofetch DC sources.
Instance Name	Specifies the instances from which voltage sources are determined.

Instance Name and Pin	Specifies the instances and their pins from which voltage sources are determined.
Cell Name	Specifies the cells from which voltage sources are determined.
Cell Name and Pin	Specifies the cells and their pins from which voltage sources are determined.
Honor Pin Wire Connection	Honors pin wire connection when fetching voltage source location from a power pad. When you select this option, only pins with wire connection are output as voltage sources.
Fetch	Automatically populates the *Pad Location List* with the pad locations based on properties defined in the LEF file. There are three ways to get the dc sources: • fetch all voltage sources - specifying *Net Name* and *Auto Fetch* • fetch the voltage sources within the specified region of the specified layer controlled by the specified xPitch/yPitch • fetch voltage source for the specified cell/cell pin/instance/instance pin **Note:** You may need to reissue the globalNetConnect command for *Auto Fetch* to function properly if the power pads were not defined in the database at the time that the globalNetConnect command was first issued.
Pad Location List	The list of coordinates for pad cells. To populate this field manually, click the *Add* button. To populate this field automatically, click the *Auto Fetch* button.
Pad Location	The X and Y coordinates of a pad cell.
Layer	The layer that contains the pad cell.
Get coord	Populates the X and Y coordinates in the *Pad Location* field. Click this button, then click a location in the design display area.
Delete	Removes one or more pad location items from the *Pad Location List*. Highlight the item be removed, then click this button. To highlight multiple items, click them while pressing either the Shift or Control key.
Add	Adds the X and Y coordinates of a pad cell to the *Pad Location List*.

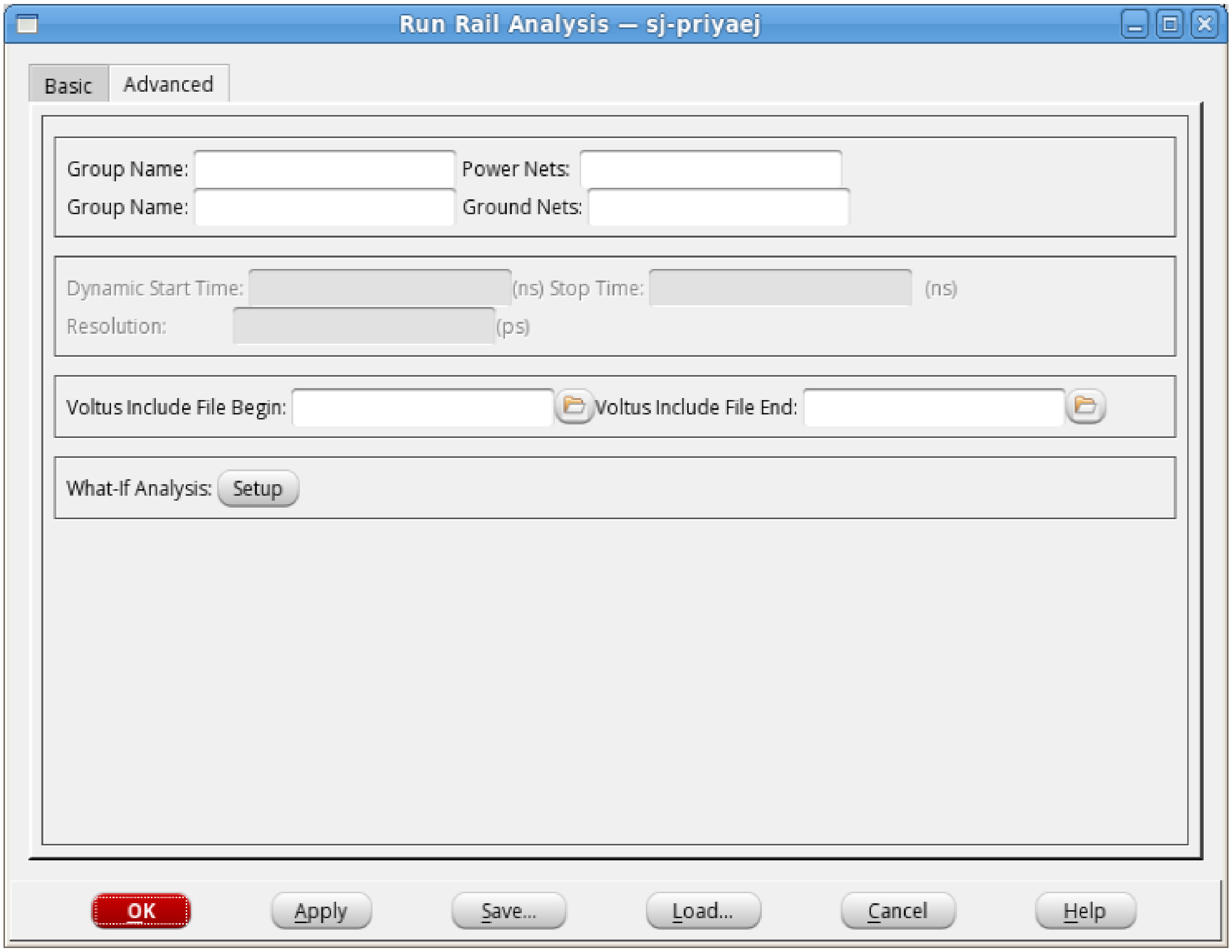
Save File Format	The format of the saved Pad Location File. The choices are *XY file* (xy coordinates) *, Padcell file* (VoltageStorm), and *TSV*. You can create and save the voltage sources location file with a unique name for the voltage sources (both VDD and VSS).
Load	Opens the Load Pad Location File form. Select a file from this list, then click *Open* to display the pad locations in the *Pad Location List*.
Save	Opens the Save Pad Location File form. Specify a location for the pad location file, then click *OK*. This saves the pad location file, clears the *Pad Location List*, and closes the Save Pad Location form.
Clear	Clears the *Pad Location List*. Once the *Pad Location List* is cleared, you can begin creating a pad location file for a new net. **Note:** Cadence recommends that you use the *Clear* button after you save the pad location file before you use *Auto Fetch* again.

Related Text Commands

For information on the following command, see "Rail Analysis Commands" in the Text Command Reference.

- `create_power_pads`

Run Rail Analysis - Advanced



Fields and Options

Group Name	Specifies the name for a group of power or ground nets.
Power Nets *Ground Nets*	Replace power domain by group.
Start Time	Specifies the start time in nanoseconds (`ns`) for dynamic analysis.

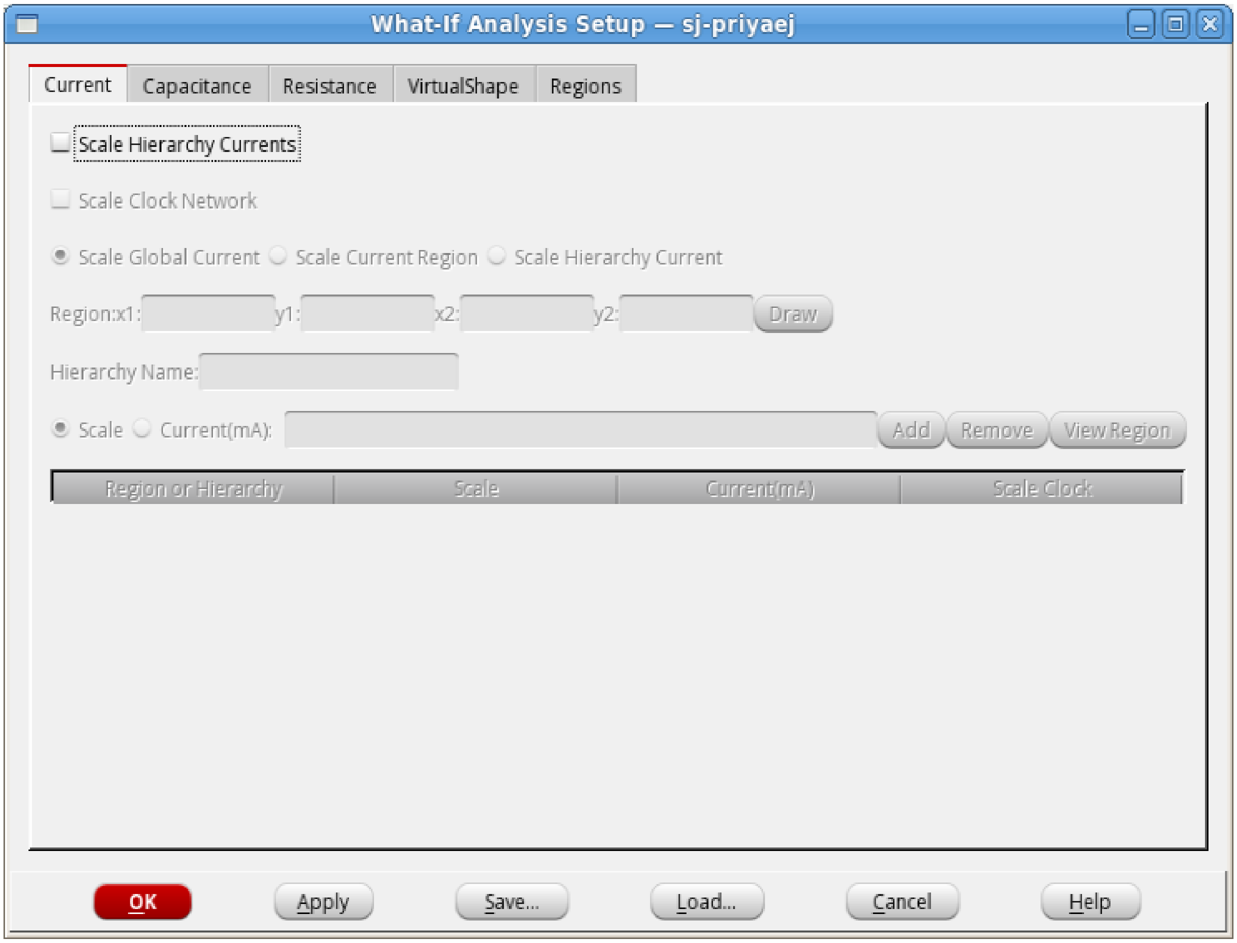
Stop Time	Specifies the stop time in nanoseconds (`ns`) for dynamic analysis.
Resolution	Specifies the transient time step size or resolution in picoseconds (`ps`).
Voltus Include File Begin	This field provides the ability to provide a file that includes `vstorm2` commands that will be run prior to the `analyze` command. This can be used for those VoltageStorm commands that do not have a Voltus GUI equivalent.
Voltus Include File End	This field provides the ability to provide a file that includes `vstorm2` commands that will be run after the `analyze` command. This can be used for those VoltageStorm commands that do not have a Voltus GUI equivalent.
What-If Analysis • *Setup*	Clicking the *Setup* button displays the GUI for • What-If Analysis Setup - Current • What-If Analysis Setup - Capacitance • What-If Analysis Setup - Resistance • What-If Analysis Setup - Virtual Shape and • What-If Analysis Setup - Regions.

Related Text Commands

See `set_pg_nets`, `set_rail_analysis_domain`, `set_power_data`, `set_power_pads`, `set_net_group`, `set_package`, `analyze_rail`, `set_advanced_rail_options` commands in the Text Command Reference.

What-If Analysis Setup - Current

Use this form to scale current to do what-if analysis for a hierarchical partition and assess its effect on IR drop.
→ Choose *Power > Rail Analysis > Run Rail Analysis > Advanced* form, click on the *What-If Analysis - Setup* button.



Fields and Options

Scale Hierarchy Currents	Specifies to scale hierarchical currents for all instances within the given hierarchy.
Scale Clock Network	Specifies to scale instances that belong to the clock network and scale currents for the rest of the instances within the given hierarchy to the specified value. You cannot specify this option with `-region` *`x1 y1 x2 y2`* or `-global` options. *Default*: Not selected
Scale Global Current	Specifies current scaling to be applied to the entire design.

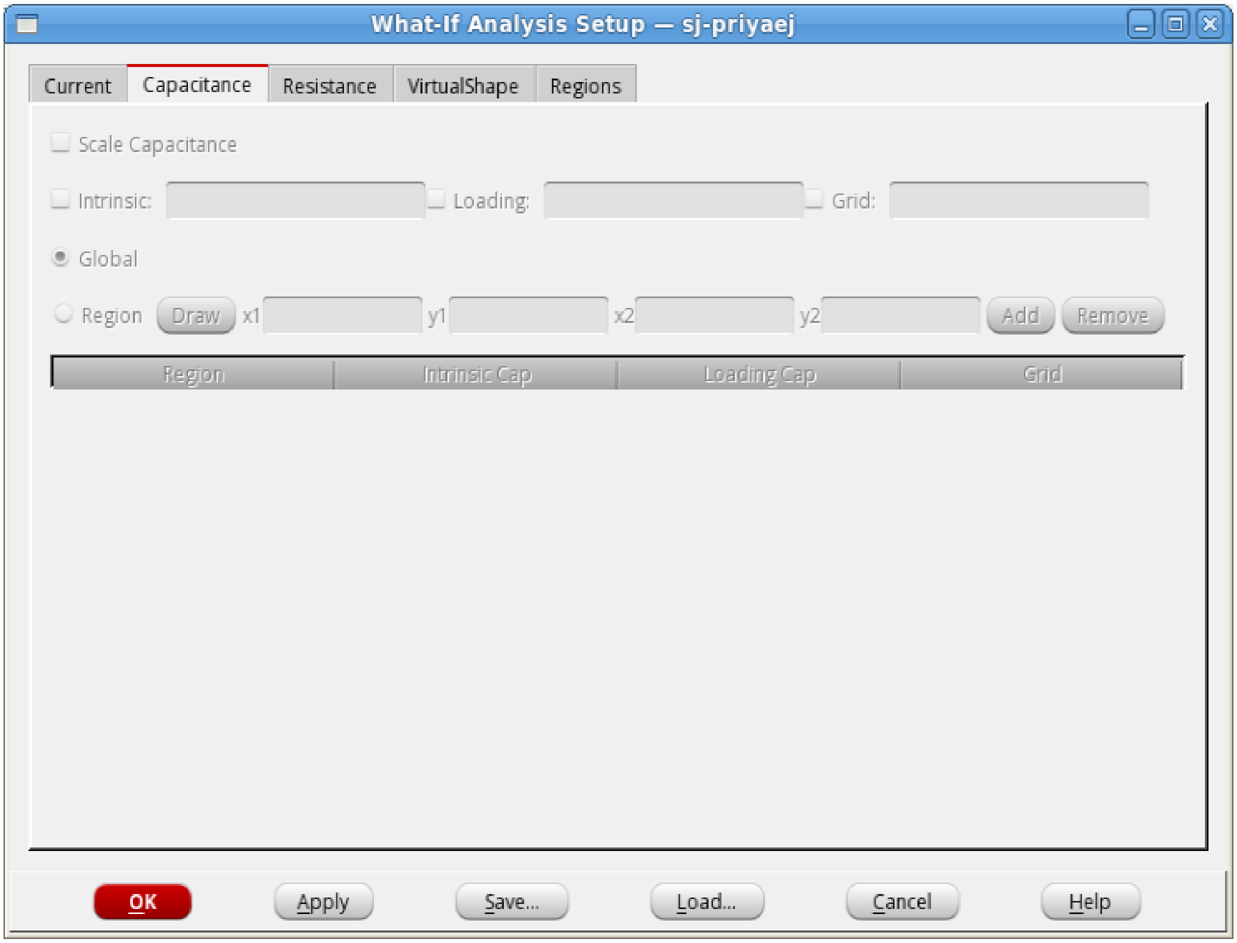
Scale Current Region	Specifies current scaling to be applied to the specified current region in the design.
Scale Hierarchy Current	Specifies current scaling to be applied to the specified hierarchical block.
Region	Specifies a region where current scaling is to be applied. The default unit of `x` and `y` coordinates is in microns (um).
Hierarchy Name	Specifies the name of the hierarchical block. For example, `-hierarchy top/blockA`. To specify global scaling for the design use "`/`". For example, `-hierarchy /` This is a required option.
Scale	Specifies any value greater than `0`. For example, a value of `0.5` will scale the resistance in half. This is a required option.
Current (mA)	Specifies current value in milliAmperes. This is used as target peak current for the given hierarchy and is then scaled appropriately. You cannot specify this option with `-region` *`x1 y1 x2 y2`* or `-global` options.

Related topics

See `scale_what_if_current` command in the Rail Analysis Commands chapter in the *Text Command Reference*.

What-If Analysis Setup - Capacitance

Use this form to scale the intrinsic cell capacitance value to determine how much additional capacitance can be added in a region to reduce dynamic IR drop.
→ Choose *Power > Rail Analysis > Run Rail Analysis > Advanced* form, click on the *What-If Analysis - Setup* button > *Capacitance* tab.



Fields and Options

Scale Capacitance	Specifies to scale capacitance.
Intrinsic	Scales instance internal gate capacitance to the specified scale factor. The default scale value is 1.
Loading	Scales loading capacitance of the instance to the specified scale factor. The default scale value is 1.
Grid	Scales power-grid capacitance of the design to the specified scale factor. The default scale value is 1.
Global	Scales the specified capacitances for the entire design.

Region • *Draw*	Scales the specified capacitances in the region. The default unit of `x1 y1 x2 y2` is in database units.

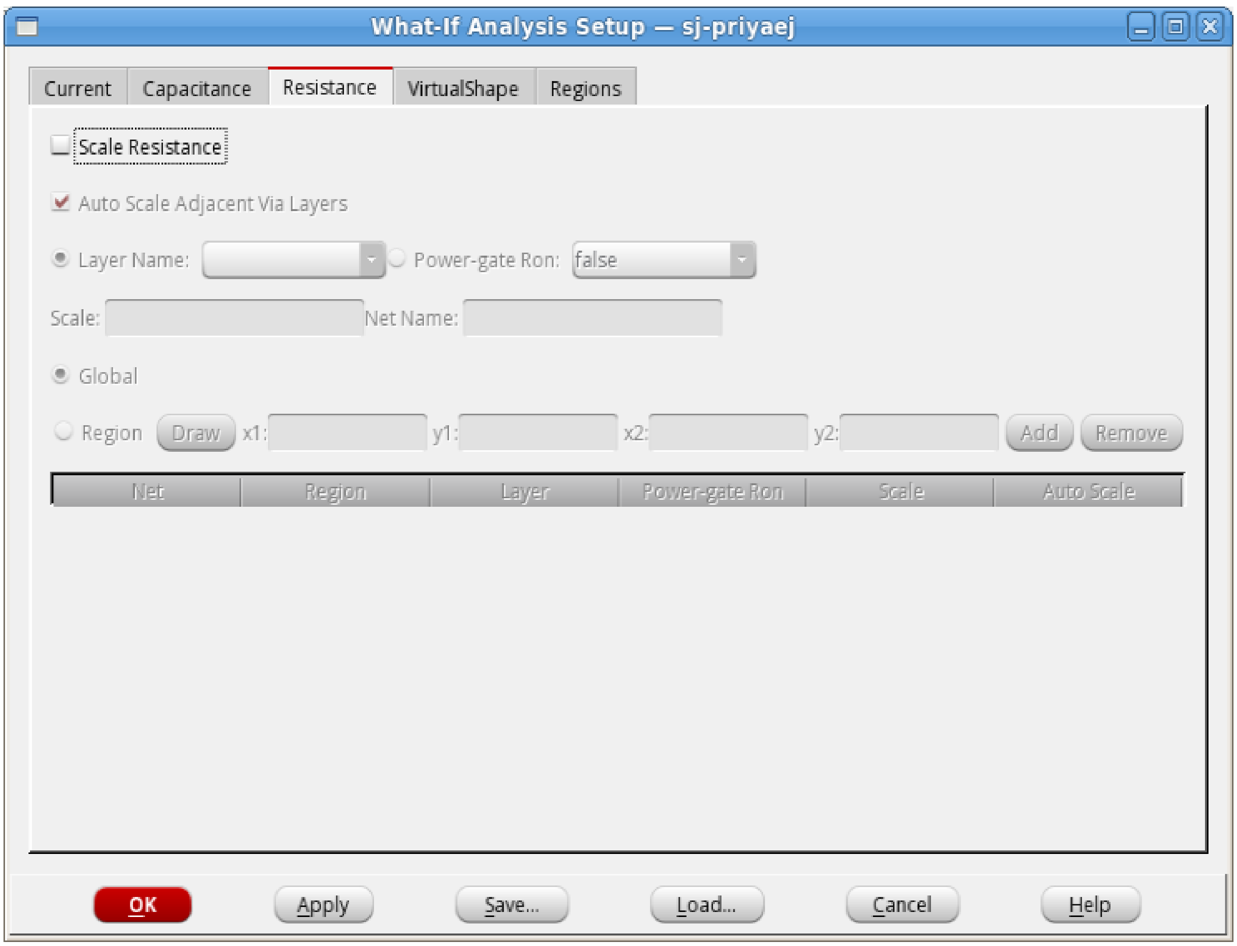
Related topics

See `scale_what_if_capacitance` command in the Rail Analysis Commands chapter in the Innovus *Text Command Reference*.

What-If Analysis Setup - Resistance

Use this form to scale resistance globally or in a region to determine how much resistance can be modified in a region to reduce the entire IR drop.

→ Choose *Power* > *Rail Analysis* > *Run Rail Analysis* > *Advanced* form, click on the *What-If Analysis - Setup* button > *Resistance* tab.



Fields and Options

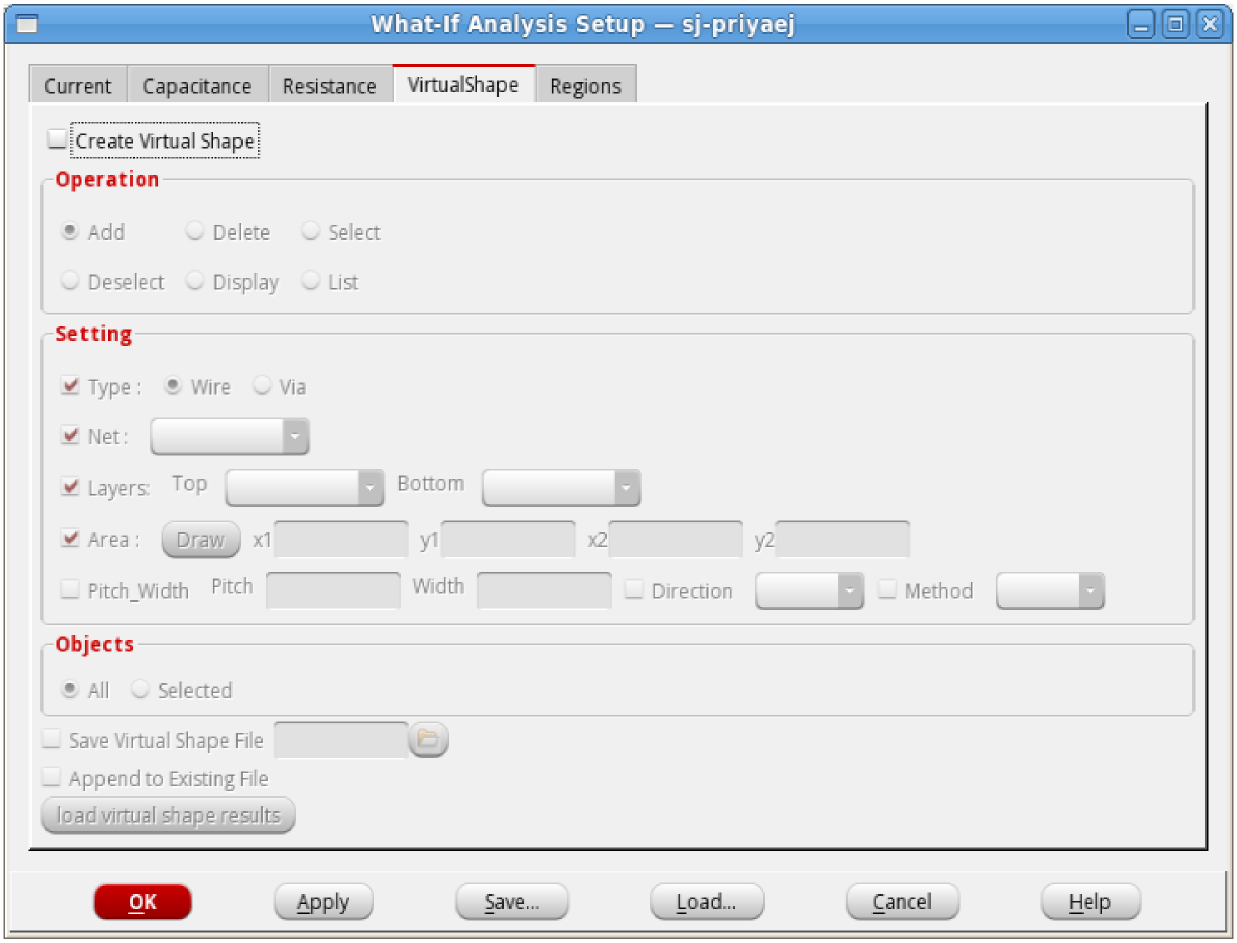
Scale Resistance	Specifies to scale resistance.
Auto Scale Adjacent Via Layers	Specifies to use auto via scaling for what-if resistance analysis.
Scale	Specifies any value greater than 0. For example, a value of 0.5 will scale the resistance in half. This is a required option.
Layer Name	Specifies the layer name (LEF layer or technology layer) on which the scaling is performed. Multiple commands can be issued to scale resistance on multiple layers. This is a required option.
Net Name	Scales resistance of the specified net in the domain which is being analyzed. This is a required option.
Global	Scales the resistance to the specified value for the entire design for a given layer.
Region • *Draw*	Scales the resistance in the specified region. The default unit of `x1 y1 x2 y2` is in database units.

Related topics

See `scale_what_if_resistance` command in the Rail Analysis Commands chapter in the Innovus *Text Command Reference*.

What-If Analysis Setup - Virtual Shape

Use this form to add, select, deselect, delete, list, and display the what if wires/vias to a design.
→ Choose *Power & Rail > Run Rail Analysis > Advanced* form, click on the *What-If Analysis - Setup* button > *Virtual Shape* tab.



Fields and Options

Create Virtual Shape	Creates virtual shapes (wires/vias) to a design.

Operation	• *Add* - Specifies to add what-if wires/vias. • *Delete* - Specifies to delete all or selected what-if shapes by constraint *Net/Layers/Type*. You can use this field in conjunction with the *Objects* field. • *Select* - Specifies to select all what-if shapes by constraint *Net/Layers/Type*. Use this field in conjunction with *Area* to select what-if shapes overlapping with the specified area. • *Deselect* - Specifies to deselect all what-if shapes by constraint *Net/Layers/Type*. Use this parameter in conjunction with *Area* to deselect what-if shapes overlapping with the specified area. • *Display* - Invokes the GUI to show what-if shapes and zooms to the selected shapes. • *List* - Specifies to list all or selected what-if shapes by constraint *Net/Layers/Type*. You can use this field in conjunction with the *Objects* field.
Type	Specifies what kind of shape is to be created.
Net	Specifies the name of the net for which what-if wires/vias is to be created.
Layers	Specifies the LEF layer name for wires, or layer pair for via to be added.
Area	Specifies the rectangular region in which the what if wires/vias are to be generated.
Pitch Width	Specifies the width of what-if wires and the distance between the centre line of two adjacent what-if wires (pitch) to be drawn in the specified *Area* in the preferred direction of the specified layer. The direction of created wires can also be controlled using the *Direction* field. If this field is not provided, a single rectangular shape of size {llx,lly,urx,ury} is created.
Direction	Controls the direction of the wires added with the *Pitch Width* field.
Method	Specifies the method used to add vias: • `Auto`: When area and layer pair are specified, the tool automatically adds vias on all intersecting points on the specified layer pairs in the given area. • `Exact`: When an area and layer pair are specified, the tool adds a via of exact size of the specified area between the specified layer pair.

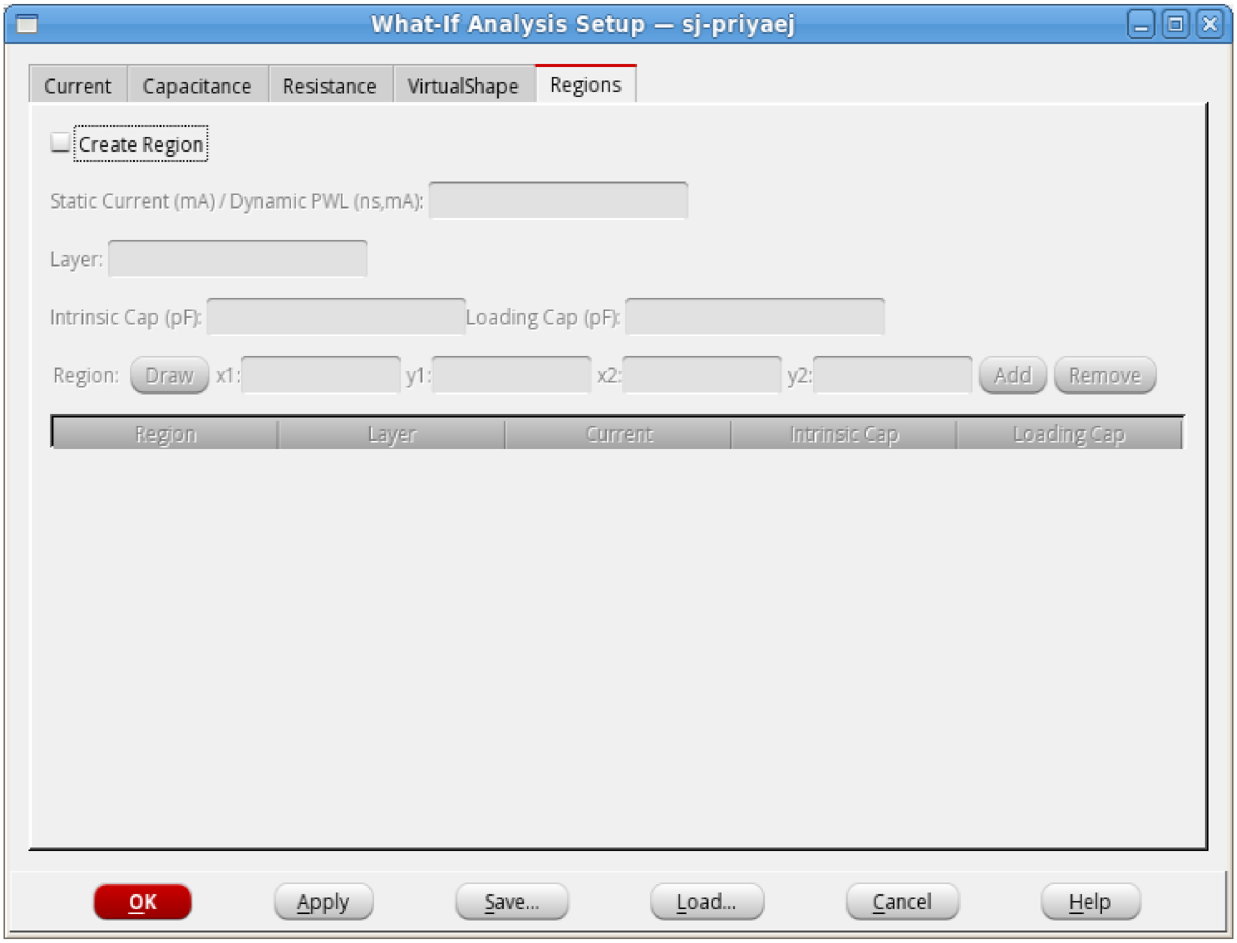
Objects	Specify *Objects* in conjunction with the *Delete* or *List* fields to delete or list the selected what-if shapes. You can also delete or list all what-if shapes. The default value is *All*.
Save Virtual Shape File	Specifies to save all the in-memory what-if wires/vias to the specified file.
Append to Existing File	Specifies to append all what-if wires/vias to the existing file specified with the *Save Virtual Shape File* field.
Load Virtual Shape Results	Loads the saved files of all vias/wires from the *What-If Analysis Setup* form and results are displayed in the design layout.

Related topics

See `create_what_if_shape` command in the *Rail Analysis Commands* chapter in the *Text Command Reference.*

What-If Analysis Setup - Regions

Use this form to specify static or dynamic current regions on global power-grids over the placed macro to accurately capture high and low current consuming regions during rail analysis.
→ Choose *Power* > *Rail Analysis* > *Run Rail Analysis* > *Advanced* form, click on the *What-If Analysis - Setup* button > *Regions* tab.



Fields and Options

Create Region	Creates current regions on global power-grids.
Static Current / Dynamic PWL	*Static Current*: Specifies a single current value in mAmp. *Dynamic PWL*: Specifies a PWL current waveform in time (in ns) and current (in mA) format. For example, 0ns 0mA 0.5ns 1mA 1ns 2mA 3ns 1mA 4ns 0.
Layer	Specifies a layer name on which the scaling will be performed. This is a required option.

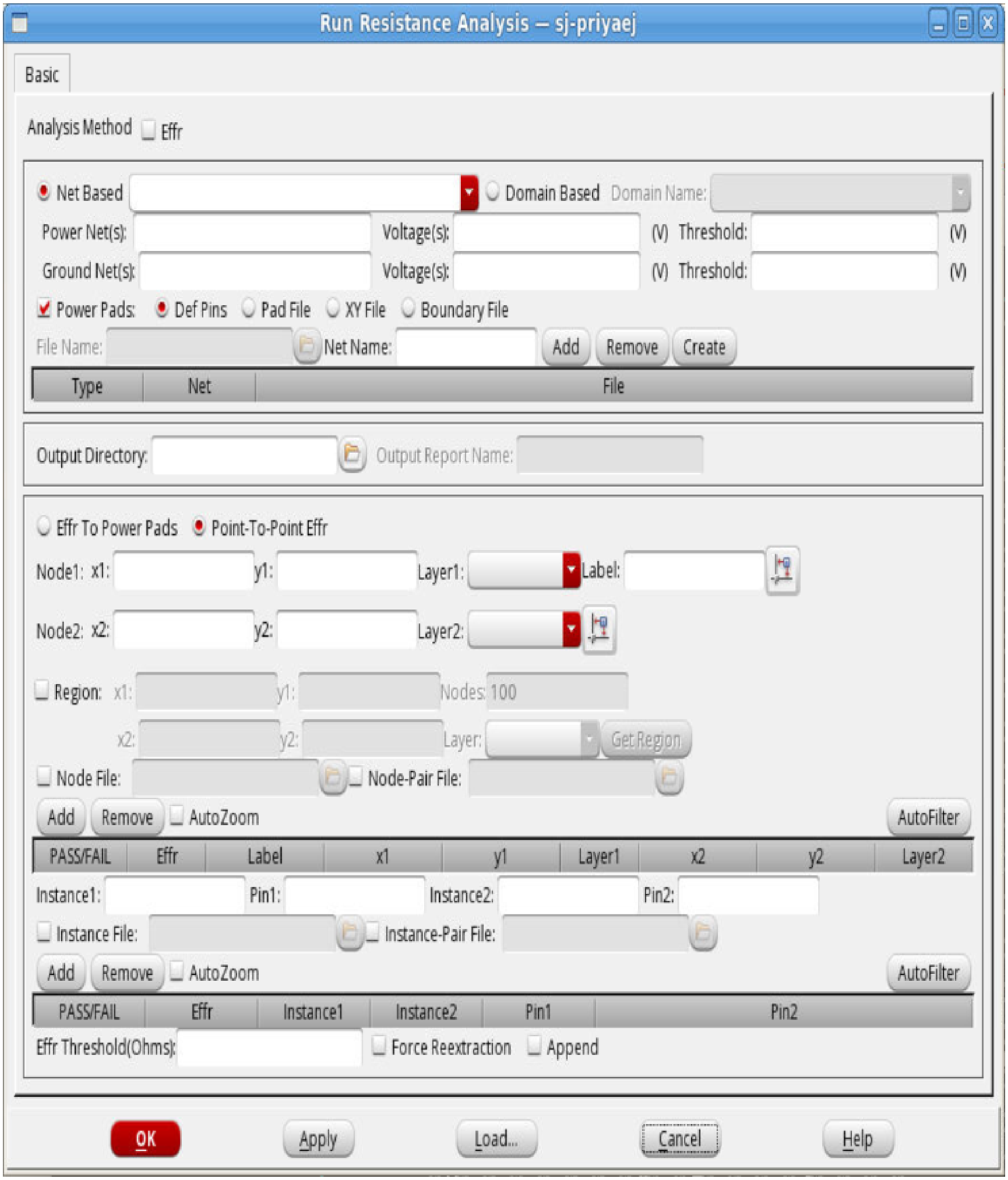
Intrinsic Cap	Specifies the cell intrinsic capacitance in pico farads (pf). This is required option when set in the dynamic mode (`set_rail_analysis_mode -method dynamic`). This option is disabled in static mode.
Loading Cap	Specifies the cell loading capacitance in pico farads (pf). This is required option when set in the dynamic mode (`set_rail_analysis_mode -method dynamic`). This option is disabled in static mode.
Region • *Draw*	Specifies the region on the layer across which the specified current and capacitance (in dynamic mode) is distributed by the rail analysis engine. This is a required option.

Related topics

See `create_current_region` command in the Rail Analysis Commands chapter in the Innovus *Text Command Reference*.

Run Resistance Analysis - Basic

Performs effective resistance calculation for all instances in a design. Effective resistance computes effective resistance between two nodes on the power-grid, or from a node to all the voltage sources in the design, or from an instance to all the voltage sources in the design.



Fields and Options

Analysis Method	Specifies the resistance analysis method as *Effr*.
Net Name	Specifies the net name that is to be analyzed.
Domain Name	Specifies the domain name that is to be analyzed.
Set PG Nets or Domain	• *Net Based* - is equivalent to the `set_pg_nets` command. • *Domain Based* - is equivalent to the `set_rail_analysis_domain` command. If you have used Tcl command in your scripts, you do not have to use these GUI fields to set PG nets or rail analysis power domain.
Power Net(s)	Specifies names of the power nets for which resistance analysis will be performed.
Voltage(s)	The voltage of the power net.
Threshold	The voltage threshold of the power net
Ground Net(s)	Specifies names of the ground nets for which resistance analysis will be performed.
Voltage(s)	The voltage of the ground net.
Threshold	The voltage threshold of the ground net
Power Pads	• *Def Pins* - specifies that voltage sources will be determined by power pins. • *Pad File* - specifies that voltage sources will be determined by pad cells given in the file. • *XY File* - specifies that voltage sources will be specified by x y coordinates. • *Boundary File* - specifies that voltage source locations will be specified by information in the boundary file. *Default: Def Pins*
File Name	The name of the power file containing the locations of the power rail voltage sources (VDD, VSS). You can automatically generate this file by clicking the *Create* button. The Edit Pad Location form appears.

Net Name	The name of the power net. The *Add* button adds the net to the list. The *Remove* button removes the net from the list.
Output Directory	Specifies the name of the directory in which the output report file is saved.
Output Report Name	Specifies the name of the output report file that contains the report header and the sorted list for resistance values.
Effr To Power Pads	Specifies to check effective resistance of a node to the voltage sources or power pads. This option is enabled only when *Power Pads* is selected. When this option is selected, *Node2* and *Instance2* options are disabled.
Point-To-Point Effr	Specifies to check effective resistance between two nodes on the power-grid. When this option is selected, *Node2* and *Instance2* options are enabled.
Node1	Specifies the list of user-defined nodes for effective resistance calculation between the specified user-defined node and all voltage sources, or between two nodes on the power-grid. This option is enabled for both *Effr To Power Pads* and *Point-To-Point Effr*. You can add a list of nodes based on the region on a given layer. • *x1* and *y1* are the coordinates of the node. • *Layer1* is the generic metal routing layer name on which the node is located. • *Label* is any name chosen by you to identify node entries in the list. This is optional but helps during debugging. • Get
Node2	Specifies the second node for effective resistance calculation between two nodes on the power-grid. This option is enabled only for *Point-To-Point Effr*. • *x2* and *y2* are the coordinates of the second node. • *Layer2* is the generic metal routing layer name on which the second node is located. • Get

Region	Analyzes resistance in the specified region. You can draw a box on a specific layer, and specify the number of nodes to be selected (maximum limit of 100 nodes). This field allows you to compute effective resistance on a given layer across the chip and determine how the resistance is changing for the design from top to bottom layer. You can assign a name for the region. • *x1*, *y1*, *x2*, and *y2* are the coordinates of the box. • *Nodes* are the number of nodes to be selected • *Layer* is the generic metal routing layer name on which the nodes are located. • Get Region
Node File	Specifies the name of the node list file. This file contains the list of user-defined nodes in the same format as mentioned for the `-node_list` parameter of the `analyze_resistance` command. The file allows you to specify a large number of nodes.
Node-Pair File	Specifies the name of the node pair list file. This file contains the node pair list in the same format as mentioned for the `-node_pair_list` parameter of the `analyze_resistance` command. The file allows you to specify a large number of node pairs.
Instance1	Specifies the list of instances for which effective resistance is to be calculated. This option is enabled for both *Effr To Power Pads* and *Point-To-Point Effr*.
Pin1	Optionally, you can specify instance pin name. By default, the tool will use the instance pin associated with the net being analyzed. Pin name can be used in special cases when two different pins of an instance are connected to the same net.
Instance2	Specifies the second instance to enable effective resistance calculation between two instances in the design. This option is enabled only for *Point-To-Point Effr*.
Pin2	Specifies the pin name for the second instance.
Instance File	Specifies the name of the instance list file. This file contains the list of instances in the same format as mentioned for the `-instance_list` parameter of the `analyze_resistance` command. The file allows you to specify a large number of instances.

Instance-Pair File	Specifies the name of the instance pair list file. This file contains the instance pair list in the same format as mentioned for the `-instance_pair_list` parameter of the `analyze_resistance` command. The file allows you to specify a large number of instance pairs.
Effr Threshold (Ohms)	Specifies the minimum allowed effective resistance to display node/node-pair/instance/instance-pair that have a resistance value above this threshold value.
Force Re-extraction	Specifies to force a re-extract of resistances.
Append	When you select *Append* and click the *Load* button, the content of the effective resistance analysis result file is appended to the previous list in the node/instance list box. If *Append* is not selected, the previous list is cleared.
Add	Adds the specified node/node-pair/instance/instance-pair to the list box.
Remove	Removes the selected node/node-pair/instance/instance-pair to the list box.
Auto Zoom	Specifies to automatically zoom in to the selected node/instance in the list box.
AutoFilter	Specifies to show the nodes or instances with eight color filter. When you specify *Effr Threshold (Ohms)* and click *AutoFilter*, the layout displays the nodes or instances with eight color filter. When you change the threshold value, you will get different plots on the layout.

Package

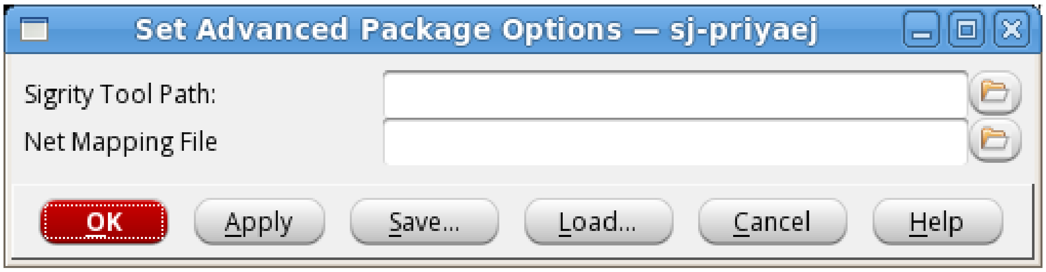
The Package menu consists of:

- Set Advanced Package Option
- Extract Package
- Analyze Package
- Package Plots

Set Advanced Package Options

Use the *Set Advanced Package Options* form to specify the path to the bin folder of package extraction and analysis tools.

- Select *Power - Package - Set Advanced Package Options*.



Fields and Options

Sigrity Tool Path	Specifies the full path to the bin folder of the package extraction and analysis tools (XtractIM and PowerDC).
Net Mapping File	Specifies the name of the two column mapping file that contains the mapping between the net names of package with the net names of die.

Related Text Commands

The following text command provides equivalent or additional functionality:

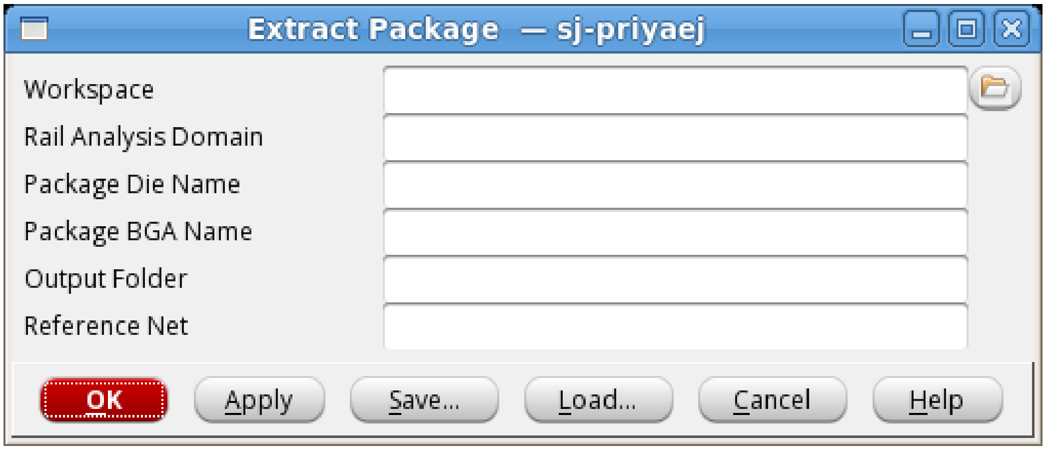
- set_advanced_package_options

For more information, see "Package Analysis" in the *Voltus User Guide.*

Extract Package

Specifies to start package model extraction.

- *Select Power - Package - Extract Package*.



Fields and Descriptions

Workspace	Specify the workspace name (package model database) of the package extraction tool (XtractIM). The file name extension is `.ximx`.
Rail Analysis Domain	Specifies the domain name.
Package Die Name	Defines the die circuit name. When specified, the software automatically creates a mapping between the die name in the package extraction tool and the die name in the software.
Package BGA Name	Defines the ball grid array (BGA) circuit name. It is the PCB component in the package model, which eventually connects to the PCB model.
Output Folder	Specifies the output/result directory. By default, the package model will be created in the workspace. However, if you specify an output directory, then a copy of the result will be made in the new directory
Reference Net	Specifies the ground net that is selected as reference net for pin-based model generation.

Related Text Commands

The following text command provides equivalent or additional functionality:

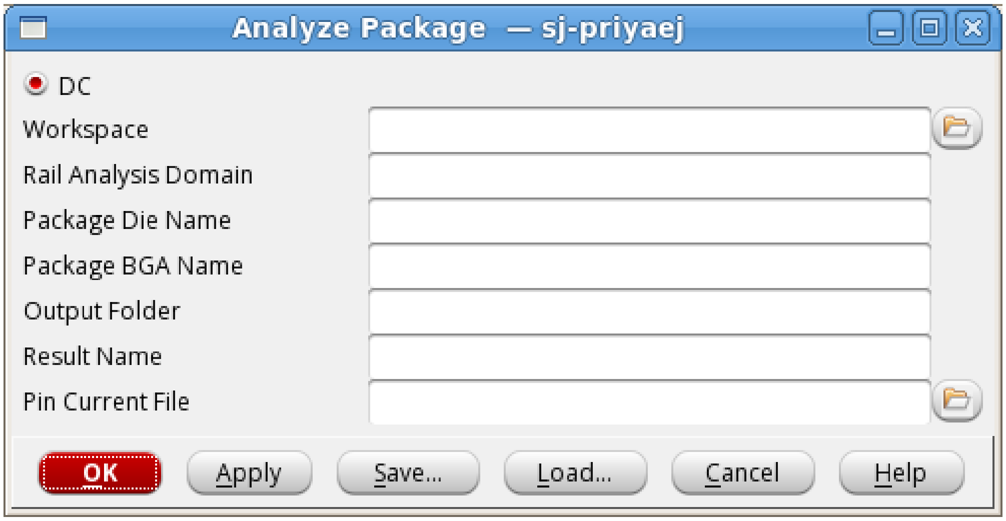
- extract_package

For more information, see "Package Analysis" in the *Voltus User Guide.*

Analyze Package

Specifies how the package analysis will be performed, and to run package analysis.

- *Select Power - Package - Analyze Package*.



Fields and Descriptions

Workspace	Specify the workspace name for package analysis (powerDC). The file name extension is `.pdcx`.
Rail Analysis Domain	Specifies the domain name.
Package Die Name	Defines the die circuit name. When specified, the software automatically creates a mapping between the die name in the package analysis tool and the die name in the software.
Package BGA Name	Defines the ball grid array (BGA) circuit name.
Output Folder	Specifies the package analysis results directory. By default, the package model results will be created in the workspace.
Result Name	Specifies the name of the .xml result file.

Pin Current File	Specifies the name of the generated pin current file from rail analysis that contains the package pin names and the current values. It is automatically generated after the package model is created, and IR drop analysis is performed using the package model.

Related Text Commands

The following text command provides equivalent or additional functionality:

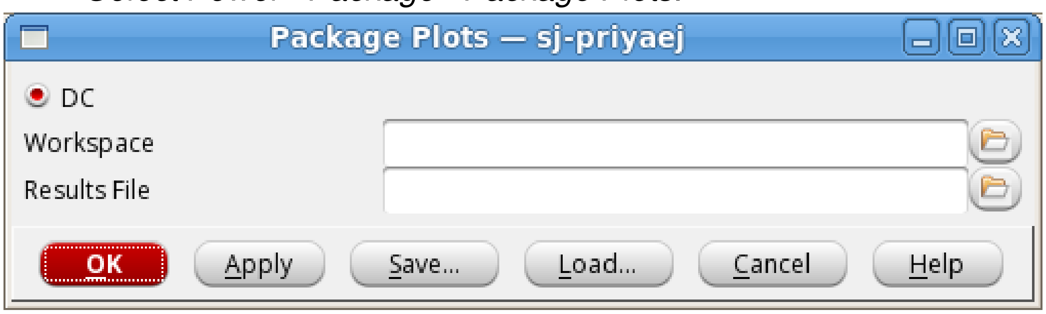
- `analyze_package`

For more information, see "Package Analysis" in the *Voltus User Guide.*

Package Plots

Allows you to view the package IR drop analysis results in the PowerDC GUI which will be invoked from within the software.

- *Select Power - Package - Package Plots*.



Fields and Descriptions

Workspace	Specifies the workspace name for package analysis (powerDC).
Results File	Specifies the name of the .xml result file.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `view_package_results`

For more information, see "Package Analysis" in the *Voltus User Guide.*

Sigrity

You can access the following Sigrity tools from within Innovus using the *Power - Package* -> *Sigrity* menu:

- *XtractIM*
- *PowerDC*

These are additional options that allow you to access the package extraction (*XtractIM*) and analysis (*PowerDC*) tools to have more control over package modeling and to easily make modifications (if needed), and then proceed with extraction or package analysis.

For details on Sigrity tools, refer to product documentation for Sigrity.

Report

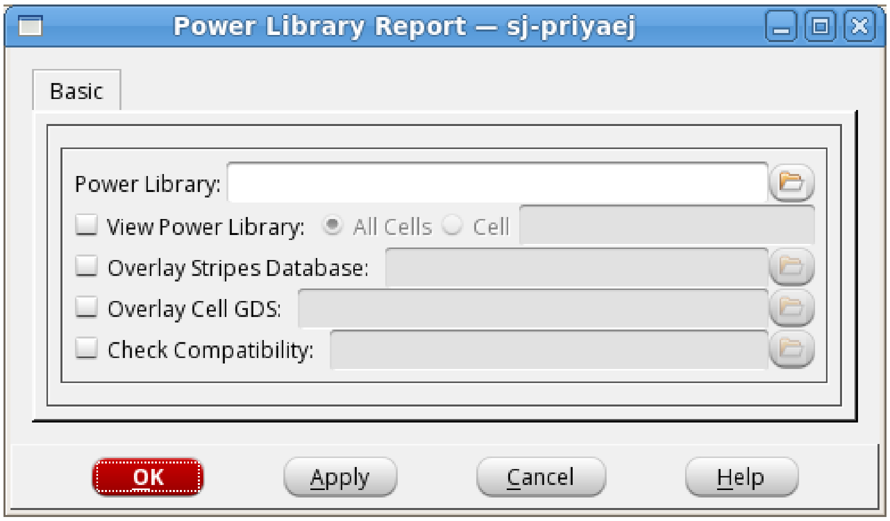
The Report submenu contains the following items:

- PowerGrid Library Report
  Opens the Power Library Report form
- Power Report has the following pages
  - Power Report - Report Power
  - Power Report - Format
- Power Histograms
  Opens the Power Histograms form
- Power and Rail Plots
  Opens the Power and Rail Plots form
- Dynamic Movies
  Opens the Dynamic Movies form

- Dynamic Waveforms
  Opens the Dynamic Waveforms form

Power Library Report

Reports contents of the already generated power library and physical view of the library power-grid network.



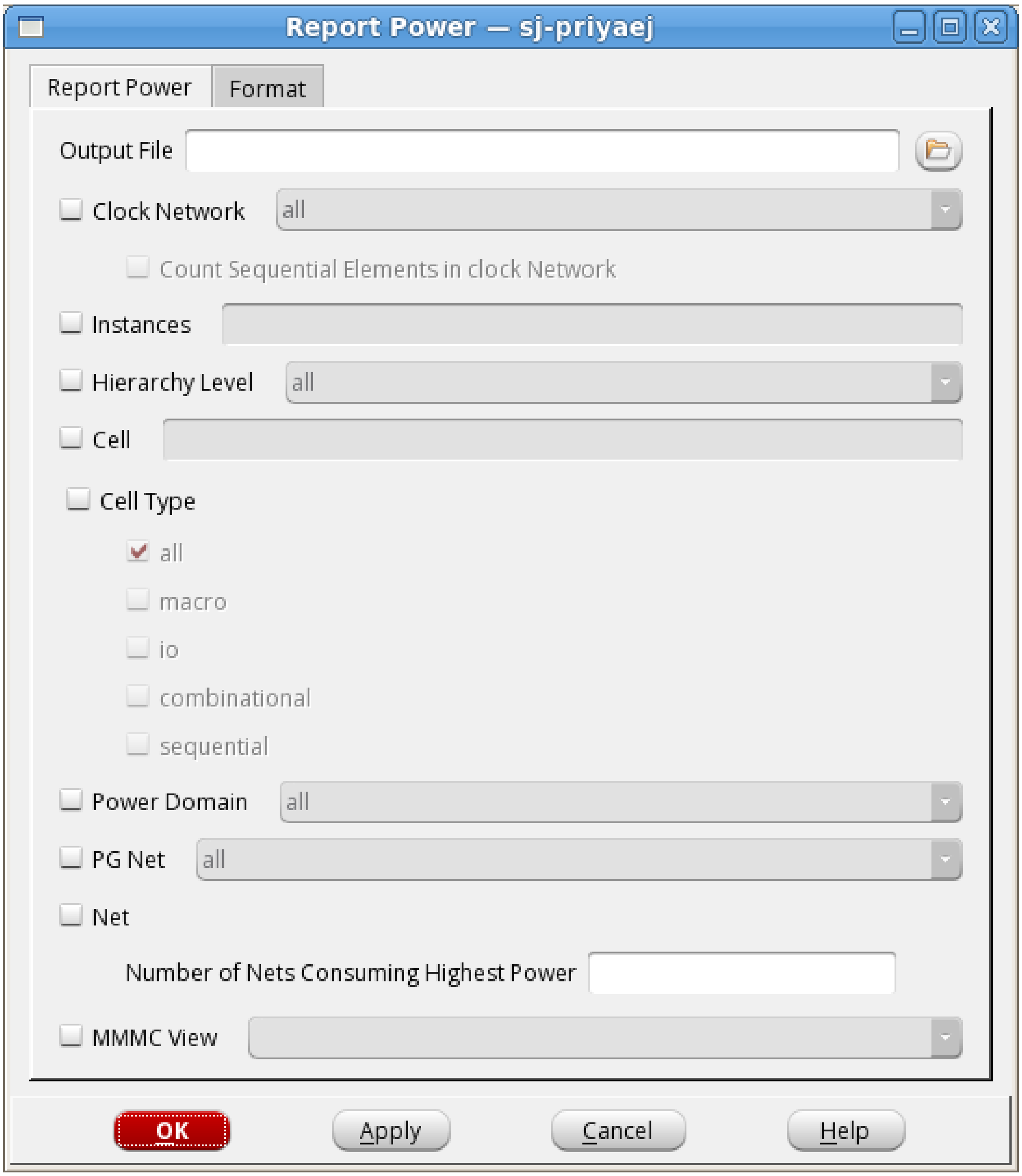
Fields and Options

Power Library	Specifies the power-grid library to generate the power library report.
View Power Library	Specifies the following options to view the power library: • *All Cells* • *Cells*
Overlay Stripes Database	Specifies the stripes database to be overlaid during the psviewer session.
Overlay Cell GDS	Specifies the cell gds design file to be overlaid, during the psviewer session.
Check Compatibility	Checks the compatibility between the specified cell libraries.

Power Report

Provides the ability to provide reports of power information in various ways.

Power Report - Report Power

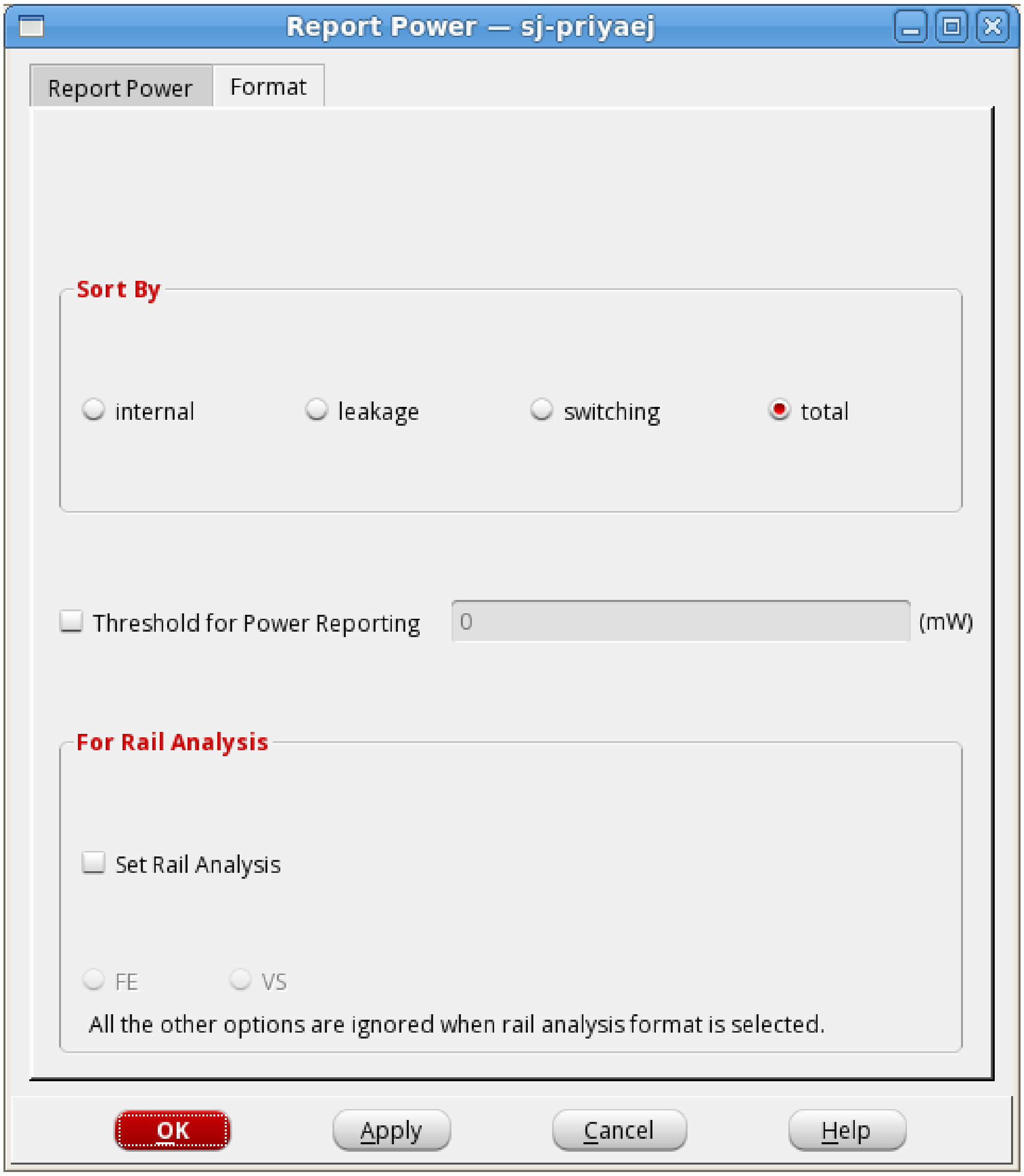


Fields and Options

Output File	Specifies the name of the report file in which power analysis output information is written. You can include the directory name. **Note:** If you do not specify this parameter, the software directs the power report to the command line, as well as the log file, and no power report is written to a separate file.
Clock Network	Reports the power consumption of the clock network, including the power for generated clocks.Specify a list to report the power consumed by specific clocks.Specify `all` to report all clock networks.*Default*: `all`
Count Sequential Elements in clock Network	If selected, report will include the leaf flip-flop power in the clock network power report.*Default*: The leaf flip-flop power will not be included in the clock network power report.
Instances	Specifies a list of instances to include in the power report. The power report provides the amount of power consumed by a specified list of hierarchical or leaf-level instances. This field accepts wildcards (*) for leaf-level instances only.
Hierarchy Level	Specifies the hierarchy level that is included in the power report. You can specify the *`Hierarchy_level`* as a number that corresponds to a specific hierarchy level in the design. A *`Hierarchy_level`* of 0 specifies the top level.*Default*: all
Cell	Specifies the cells to include in the power report. Accepts wildcards (*)
Cell Type	Specifies the cell type to included in the power report. The choices are `all` or any combination of macro, io, combinational, or sequential.*Default*: `all`
Power Domain	Specifies all power domains or a list of power domains to be included in report.
PG Net	Specifies `all` power nets or those of a particular hierarchy level to be included in power report.

Net	Reports the net switching power, as well as the load capacitance, toggle rate, and switching values for each net in the design.
Number of Nets Consuming Highest Power	Reports the number of nets with the highest net switching power. **Note:** You must use this parameter in conjunction with the *Net* parameter.
MMMC View	Specifies the view that was created using the multi-mode multi-corner (MMMC) `create_analysis_view` command. Power analysis is performed for the specified view.Default: Uses current view in Innovus PS.

Power Report - Format

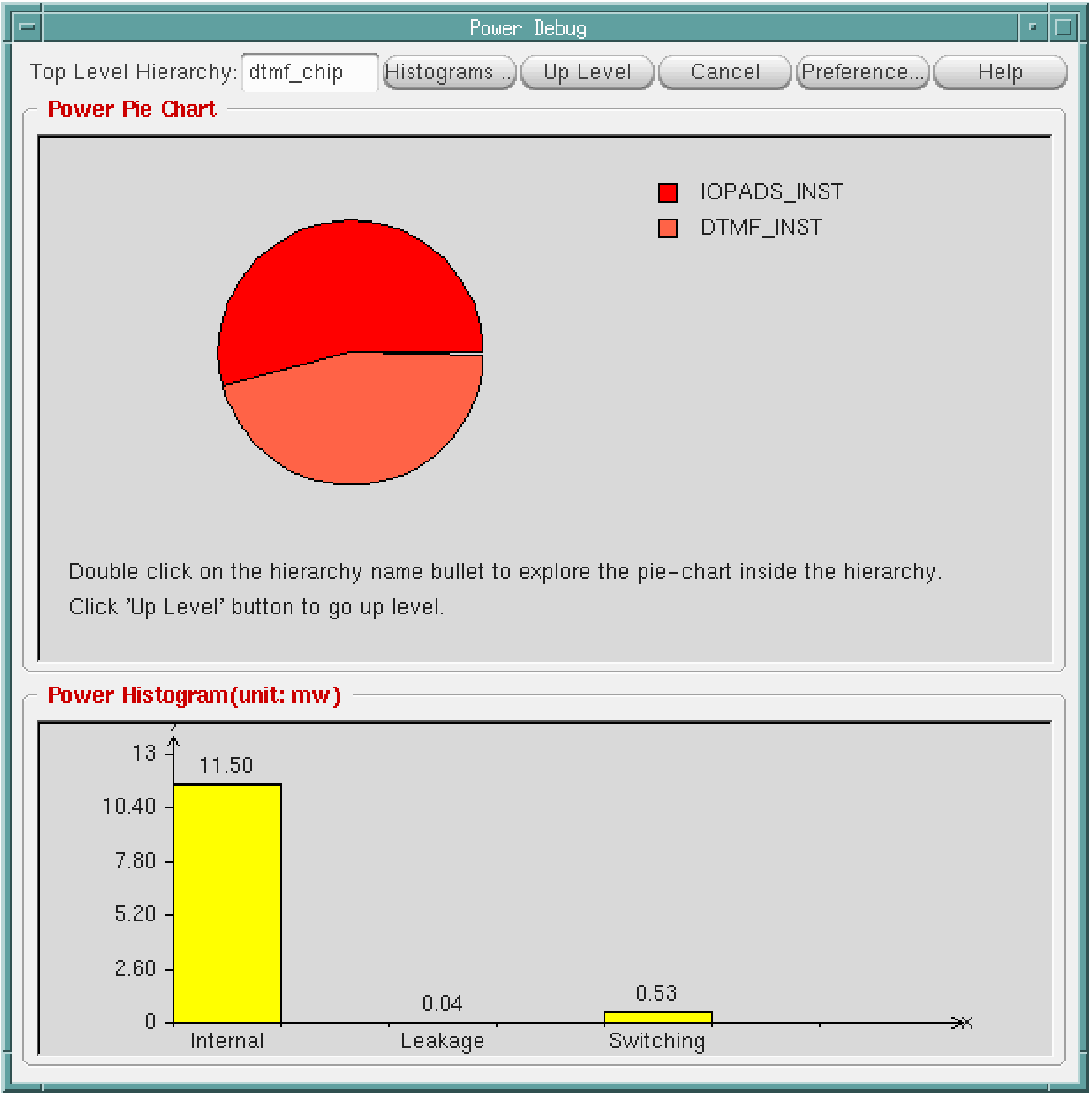


Fields and Options

Sort By: • *internal* • *leakage* • *switching* • *total*	Sorts power report based on the power (internal / leakage / swtiching / total) option that you select.
Threshold for Power Reporting	
	Specifies the threshold value for power reporting.
For Rail Analysis	• *Set Rail Analysis: Specifies to report power in rail analysis format.* • *FE:* • *VS:*

Power Histograms

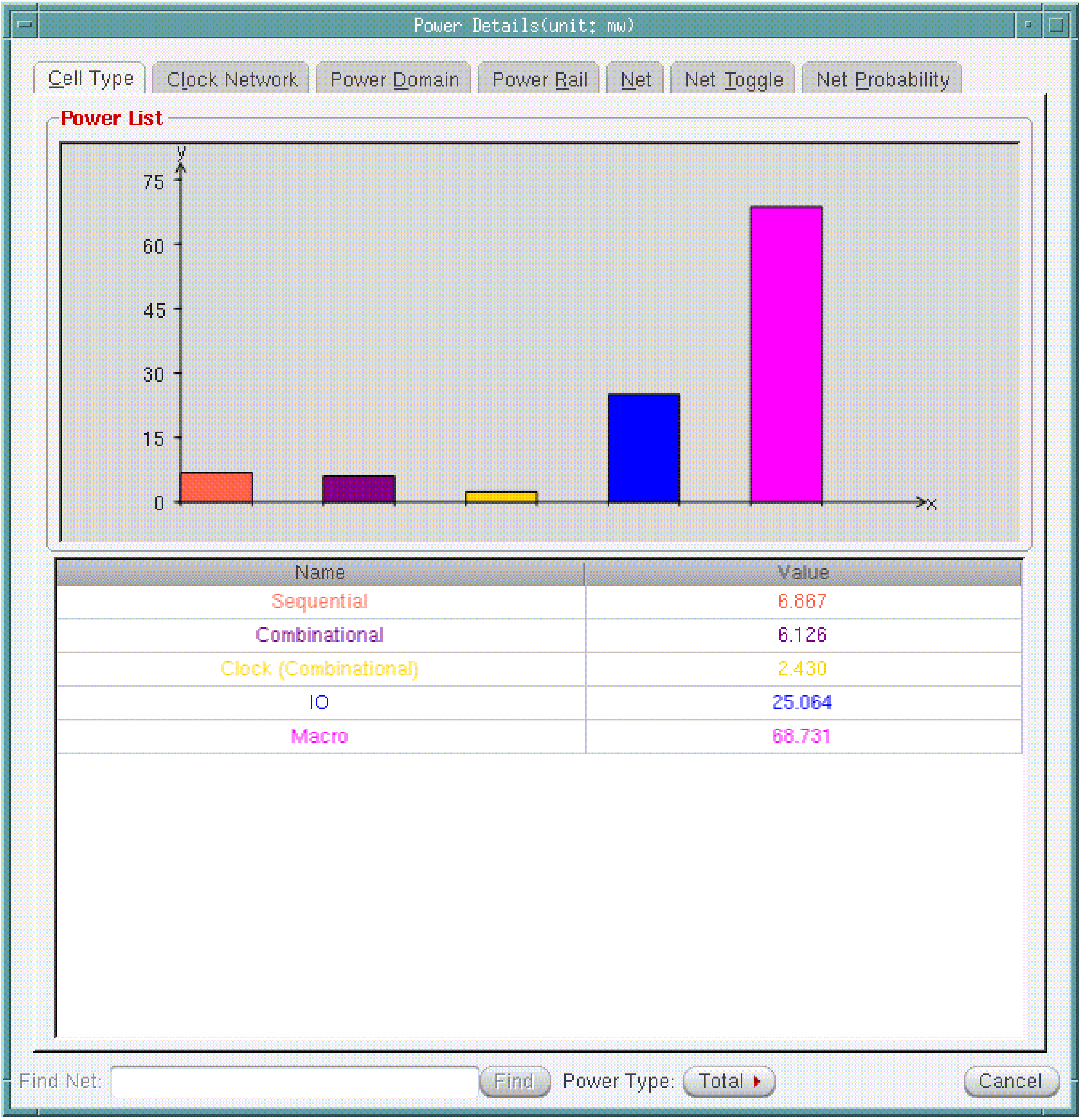
The Power Debug form displays power histograms in various ways.
→ To open the Power Debug form, choose *Power - Power Histograms*.
→ To display information from one level down in the hierarchy, double-click on a listed instance.
→ To display information from one level higher in the hierarchy, select *Up Level.*



Power Histograms - Power Details

The Power Details form displays histograms by cell type, clock domain, power domain, power rail, net, net toggle, or net probability.

→ To open the Power Details form, click on the *Histograms* button on the Power Debug form.


Power Details(unit: mw)
Cell Type
Clock Network
Power Domain
Power Rail
Net
Net Toggle
Net Probability
Power List
y
75
60
45
30
15
0
x
Name
Value
Sequential
6.867
Combinational
6.126
Clock (Combinational)
2.430
IO
25.064
Macro
68.731
Find Net:
Find
Power Type:
Total
Cancel

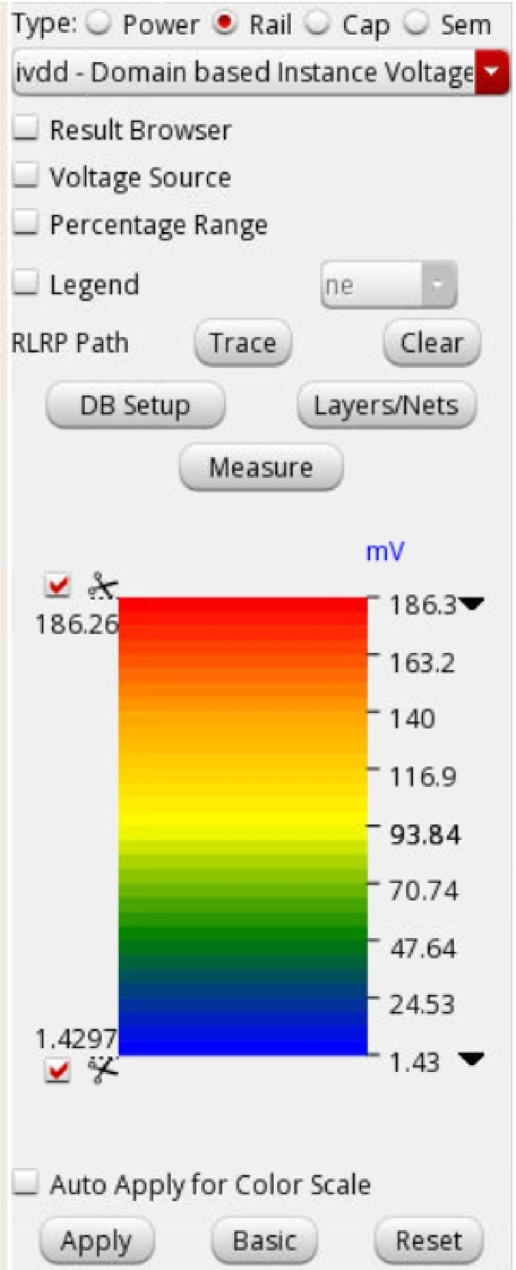
Power Histograms - Power Debug Preference

The Power Debug Preference form is used to specify Y-max/Y-min/Y-step for each of the power debug histogram, such as *Cell Type*, *Clock Network*, and so on. You can also save and load these setting for all the histograms as a `.tcl` file. The default file name is `pdg.pref.tcl`.

→ To open the Power Debug Preference form, click on the *Preference* button on the Power Debug form or right-click on any of the power debug histograms in the Power Details form.

Power and Rail Plots

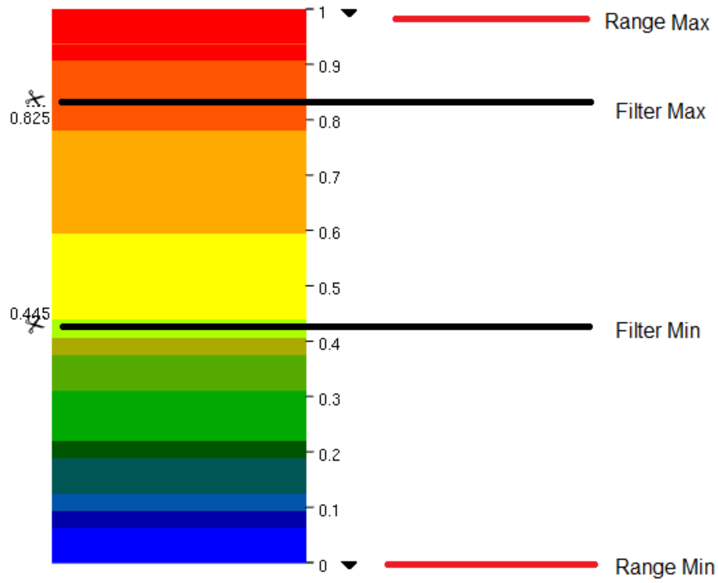
The Power & Rail Plots form is the main console window for displaying the power and rail analysis results. The data can be loaded into GUI using the *Power & Rail Setup* form accessed by clicking the *DB Setup* button. The displayed nets and layers selection can be changed using the *Power & Rail Layers/Nets* form accessed by clicking the *Layers/Nets* button. The rest of the display can be configured on the main window.



Fields and Options

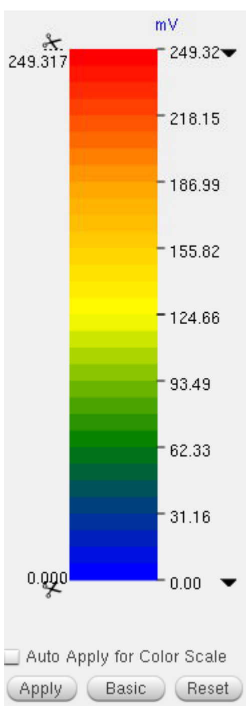
Type	• *Power* - Plots the power analysis plot type. • *Rail* - Plots the rail analysis plot type. • *Cap* - Plots the capacitance plot type. • *Sem* - Plots the signal electromigration (EM) plot type. You can select a power, rail, capacitance, or signal EM plot type from the drop-down list. For a description of the various plot types, see the `set_power_rail_display` command.
Result Browser	Displays the Results Browser form.
Voltage Source	Displays voltage sources (power pads) using white pixels in the layout canvas.
Percentage Range	Displays color gradients for the following plots by percentage: • IR Drop • IVDD • IVDN By default, the Voltus GUI displays color gradients by the voltage value, and these gradients are applied to all rails/instances with varying voltage levels (rails/instances with max voltage value will be red and with min voltage value will be blue). When this option is selected, the GUI displays color gradients by percentage of voltages. The percentage value is based on the nominal voltage value of each rail/instance. When the *Percentage Range* option is selected, the GUI displays high percentage voltages in red and low percentage voltages in blue. This option allows you to be more intuitive when analyzing these plots.

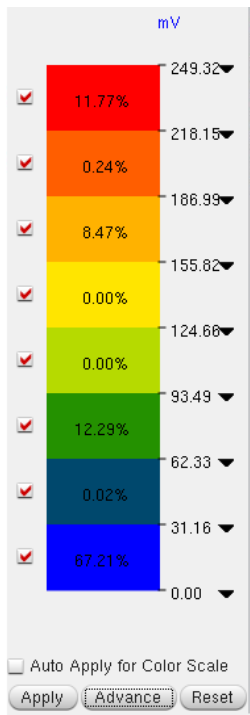
RLRP Path	You can select an object (instance or resistor) and click the *Trace* button to highlight the least effective resistance path from the object to the nearest voltage source, and to open the *Resistance Path* form. The rail analysis must include RLRP analysis (`set_rail_analysis_mode -enable_rlrp_analysis true`) in order to have the required data for this functionality. You can click the *Clear* button to clear the path. The *Result Browser* will list each instance's total resistance, and the *Resistance Path* form will list the break down of each resistance in the rlrp path. You can select a resistor in this form, single click to select/zoom, and double click to query. **Note:** If the *Resistance Path* form is closed, you can open it again by first selecting the object that you want to trace, and then clicking the *Trace* button.
Legend	Displays the filter color and range details. When you select a location (`ne nw se sw`) , this opens the legend at the specified location on the design layout. You can clear the checkbox to close the legend. **Note**: Legend is useful when dumping the screen capture to save the color range information.
DB Setup	Opens the Power & Rail Setup form that allows you to load power/rail/signal EM analysis results into GUI.
Layer/Nets	Opens the Power & Rail Layers/Nets form that allows you to control the visibility of the layers, the opacity of the rail analysis or design database, the visibility of power/ground nets, and visibility of the signal EM layers.
Measure	Provides the ability to measure tap current and capacitance of the specified region. The use model is as follows: 1. Click the *Measure* button. 2. Select a region in the main window. 3. Look for the results in the console window.

<table>
<tr>
<td>Range</td>
<td>When a plot type is selected, the filter values automatically get filled in.


Range Min and Max - Click the icon to specify the minimum and maximum value to report. When the filter is at the default (max/min) position, any values greater than “Range Max” will take on the range max color, and vice-versa for “Range Min”.
Filter Min and Max - Click the icon to specify the minimum and maximum value to include in the report/display. Use the scissor icon to further filter out the data within the range specified. This is used to obtain statistic of filter range. “Filter Max” will hide any data point greater than the filtered value, and vice-versa for “Filter Min”.

</td>
</tr>
<tr>
<td>Auto Apply for Color Scale</td>
<td>Allows you to to automatically redraw the layout after modifying the range values. If you do not select this checkbox, you can click the Apply button to manually redraw the layout.</td>
</tr>
</table>

<table>
<tr>
<td>Basic/Advanced</td>
<td>
The Basic/Advanced toggle button allows you to alternate between the color gradient (Basic) and color range (Advanced) mode when it is clicked. By default, the Basic button and the color gradient based filter are displayed. When you click the Basic button, the button text changes to Advanced, and the form shows the color range based filter. The color gradient based filter allows you to modify the minimum and maximum values, and the color range based filter allows you to modify 8 equal filters between the minimum and maximum values.
Basic (Color Gradient) Advanced (Color Range)




Selecting Apply will accept the changes, and Reset will set it to default values.
</td>
</tr>
</table>

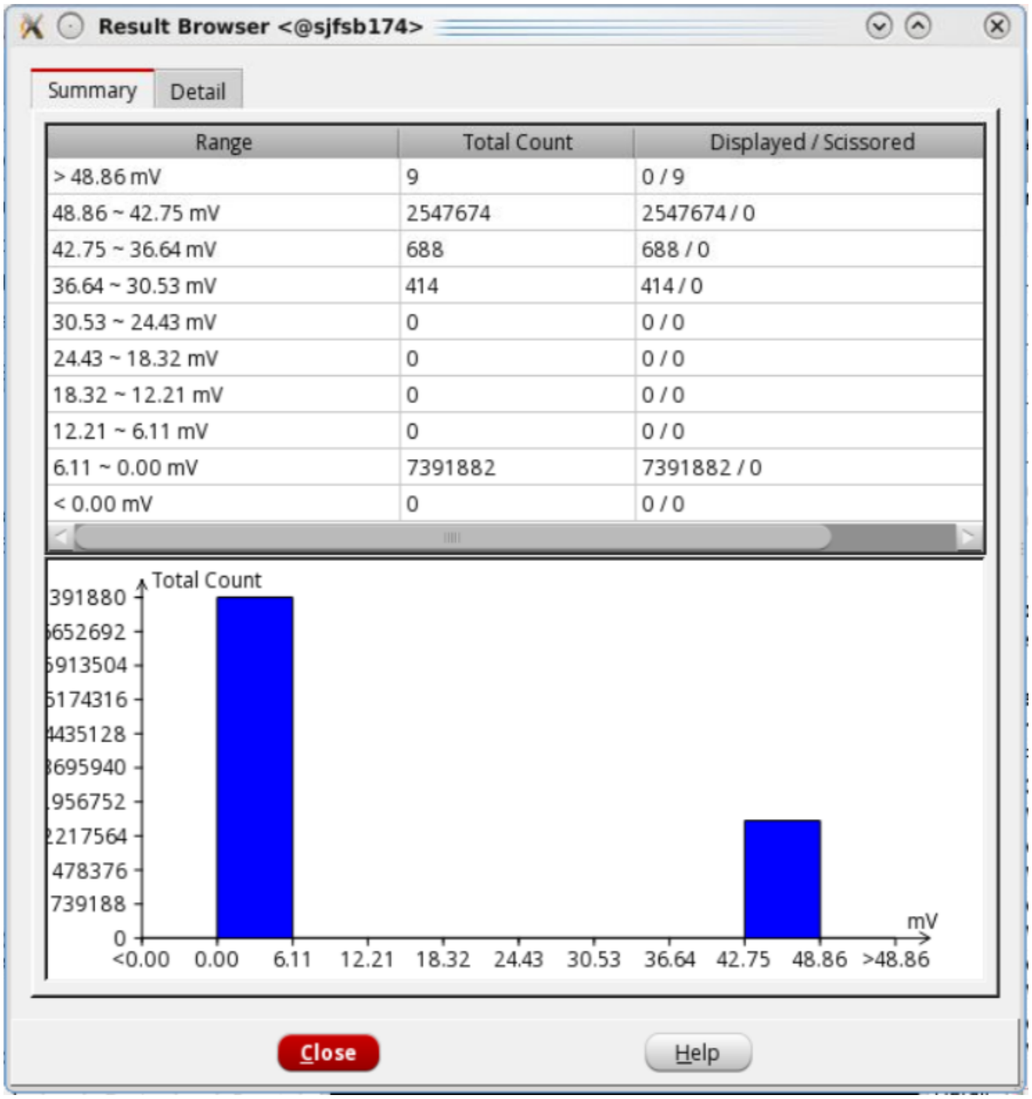
Related Text Commands

See `report_power_rail_results` and `set_power_rail_display` commands in *Text Command Reference.*

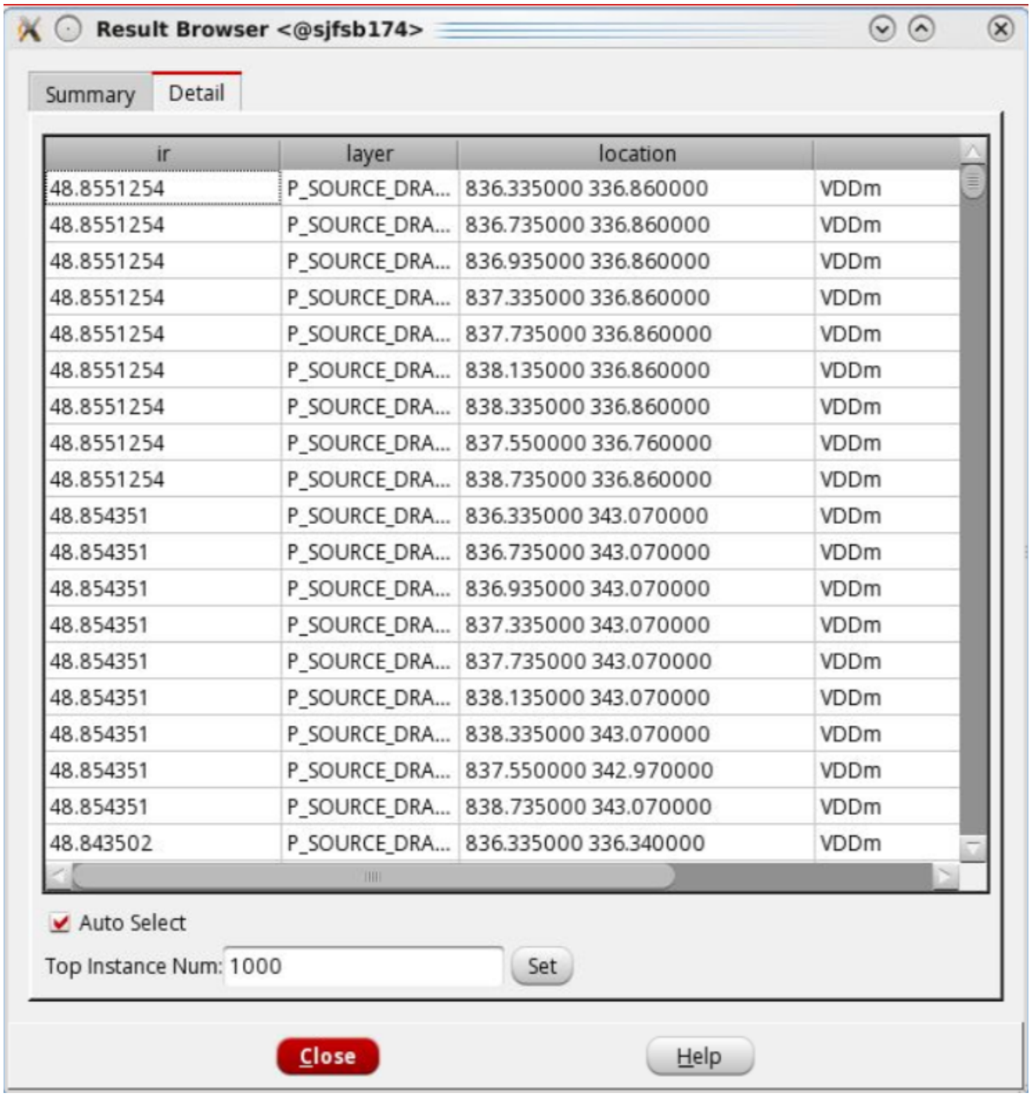
Result Browser

The Result Browser form has the following two tabs:

- *Summary* - provides summary information about the plot displayed. The data points are divided into buckets based on the range specified, and the summary information provides the statistic of each bucket. The tab also displays the rail analysis results in the histogram form.



- *Detail* - provides details of the individual data points of the plot displayed. By default, the first 1000 data points are displayed.



Power and Rail Plots - DB Setup

Loads power/rail analysis results into GUI.

Fields and Options

Power Database	Specifies the power database file. This file was created by using the `-create_binary_db` option of the `set_power_analysis_mode` command.
Rail Database	Specifies the rail analysis directory. You can load all the domain results by selecting the automatically generated analysis directory under the output directory (`<domain>_<temp>_<dynamic/avg>_#`), or load individual nets by going one level further and selecting the net directory.

SEM Database	Specifies the database file generated by the `verify_AC_limit -report_db` command. This file contains the information required for loading and displaying signal EM data in GUI.
Effective Res	Specifies the result file from effective resistance analysis (only instance-based result is supported). When the rail analysis plot type `effr` is selected and a result file is specified, the layout shows effective resistance analysis result for each instance. **Note**: This field supports display of both net and domain based result file.
Inst Heat	Specifies the name of the instance-based delta temperature file from self-heating analysis. This is the device instance temperature.
Tile Heat	Specifies the name of the tile-based delta temperature file of self-heating analysis. This is the worst instance temperature among all wire segments in a tile. This is also layer-based. The FEOL or cell layer is used to show the device instance temperature.
Detailed Heat	Specifies the name of the detailed wire-based delta temperature file from self-heating analysis.
Custom Value Instance Files	Specifies the name of the custom value instance file (CVIF) that can be used to display a user-specified instance voltage file in GUI. After specifying the CVIF file, you can select the *cvil Rail* plot in the *Power & Rail Plots* form for displaying the EIV map.

<table>
<tr>
<td>Selective Loading</td>
<td>

Nets - Specifies whether all nets or selected nets are to be loaded into the GUI.

All - loads all the nets in the domain-based state directory to the GUI. This option is selected by default.
Partial - Loads only the specified nets in the domain-based state directory to the GUI. To specify nets:

Select Partial and click the Select button.
The Selective Nets form appears.
Select the required power and ground nets, and click OK.

IV Window - Loads the instance voltage data for the selected EIV window. By default, the instance voltage results for both the timing and switching windows, and the entire rail simulation are loaded.
IV Method Type - Loads the instance voltage data for the specified EIV computing method. By default, the instance voltage results for all the four methods are loaded.

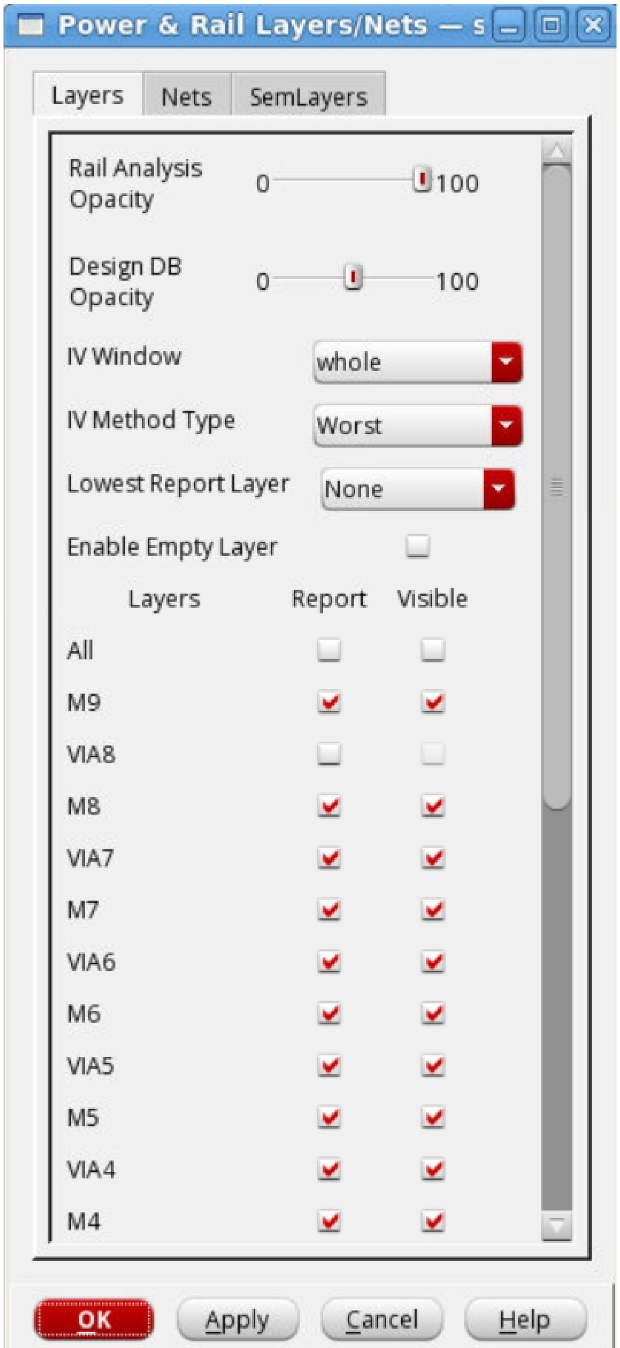
</td>
</tr>
</table>

Related Text Commands

See `read_power_rail_results` command in *Text Command Reference.*

Power and Rail Plots - Layers

Provides the ability to set the visibility of the layers and the opacity of the rail analysis or design database. This makes it easier to view when overlaying the rail analysis and the design database.



Fields and Options

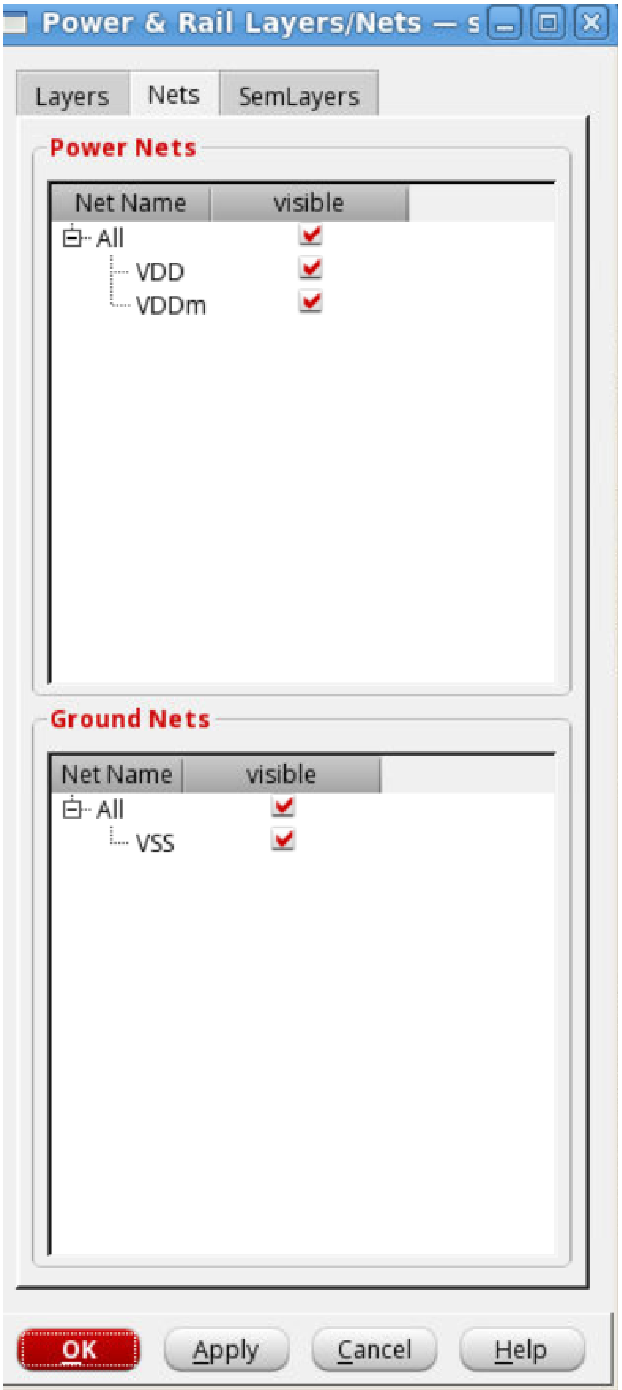
Rail Analysis Opacity	Sets the opacity of the rail analysis output. These will be the resistor/node database load from rail analysis.
Design DB Opacity	Sets the opacity of the design database. These will be the shapes coming from DEF (main control panel).
IV Window	Controls the window where effective instance voltage (EIV) is evaluated. EIV is obtained by processing the voltage waveforms and finding the worse-case effective voltage between the power and ground pins during a specific window. There are two possible options to evaluate EIV: • *timing/switching* – both switching activity (current is non-leakage) and timing window • *whole* – entire rail simulation not filtered to a specific window
IV Method	Allows different methods of computing effective instance voltage during rail analysis. Using this option, you can write out the *Best*, *Worst*, or *Average* effective instance voltage between power and ground nets. The *WorstAvg* method computes the average instance voltage during each evaluation window defined by the *IV Window* field, and reports the worst average instance voltage out of all the windows. If *IV Method* is *WorstAvg* and *IV Window* is *whole*, then this method will report average voltage across all time steps in simulation. *Default* : `Worst`
Layers	You can enable or disable the reporting and visibility of the displayed layers.
Report	Specifies to select the user-defined layers to be used for processing.
Visible	Specifies which layers should be made visible when plotting.

Related Text Commands

See `set_power_rail_layers_nets` command in *Text Command Reference.*

Power and Rail Plots - Nets

Controls the visibility of power/ground nets.



Fields and Options

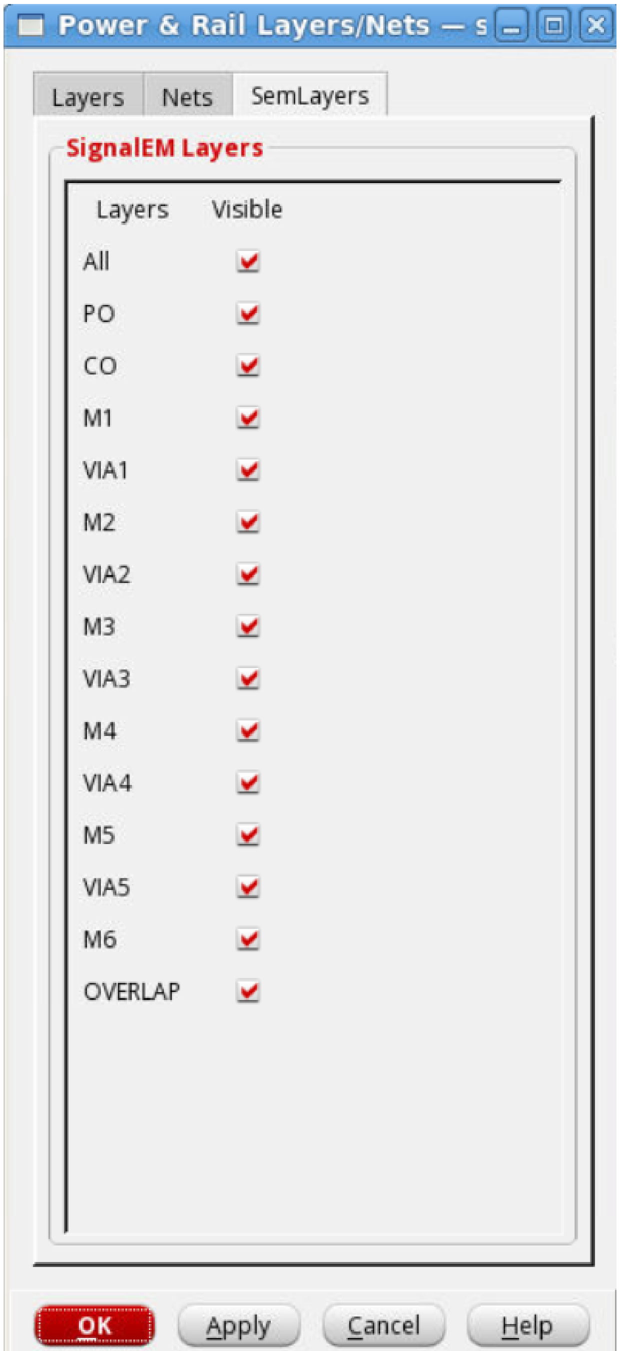
Power Nets	Displays the selected power nets.
Ground Nets	Displays the selected ground nets.

Related Text Commands

See `set_power_rail_layers_nets` command in *Text Command Reference.*

Power and Rail Plots - Sem Layers

Controls the visibility of the signal EM layers.



Fields and Options

Layers	You can enable or disable the visibility of the displayed signal EM layers.

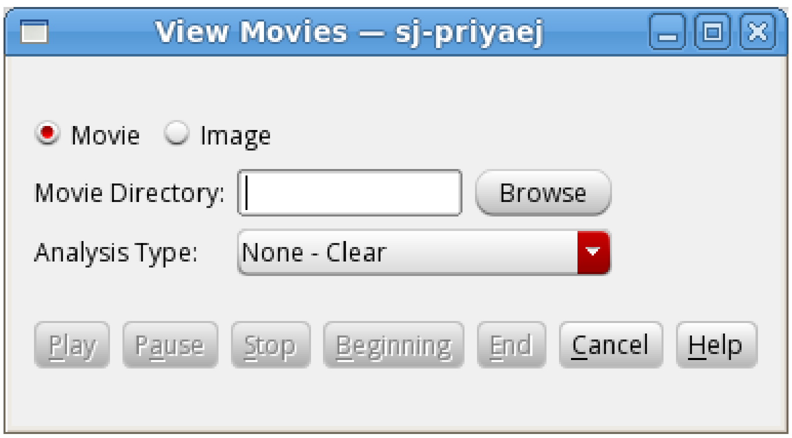
Visible	Specifies which layers should be made visible when plotting.

Related Text Commands

See `set_power_rail_layers_nets` command in *Text Command Reference.*

Dynamic Movies

Provides the ability to view dynamic movies.



Fields and Options

Movie Directory	Specifies the directory that includes the movie files.
Analysis Type	Specifies the analysis type that will be viewed.
Movie	Specifies that a movie will be viewed.
Image	Specifies that an image or plot will be viewed.
Play	Plays the movie.

Pause	Pauses the movie.
Stop	Stops the movie.
Beginning	Goes to the beginning of the movie.
End	Goes to the end of the movie.
Cancel	Cancels the movie.

Dynamic Waveforms

Provides the ability to display dynamic waveforms. This functionality requires a Simvision license.

Fields and Options

Power (Current) Waveforms	Specifies Current waveforms will be displayed.

IRdrop (Voltage) Waveforms	Specifies Voltage waveforms will be displayed.
Profiling Histograms	Specifies to profile Power Histograms.
Power Database	Specifies the power database.
Waveform Files	Specifies the waveforms that will be viewed. Current or Voltage files can be loaded or removed using the *Add* and *Remove* buttons respectively. To highlight multiple items, click them while pressing either the *Shift* or *Control* key.
Filter - Pattern	The items on the list can be filtered. This is done by entering a value in the *Pattern* field and selecting either *Net* or *Instance*.
Net	Specifies that the nets will be filtered by the text in the *Pattern* field
Instance	Specifies that the instances will be filtered by the text in the *Pattern* field
Select From GUI	This button can be used to plot a waveform for an instance that is selected in the window.
Clear	The Pattern field can be emptied by selecting the `Clear` button.
Plot	To view a current or voltage waveform, select an item on the list, and select the *Plot* button. This will result in Simvision being run and a Simvision window appearing with the selected current waveform displayed.
Cancel	Closes the View Waveforms form.

8

Place Menu

Specify

The *Place* menu's Specify forms enable you to specify and assign spare cells, scan cells, JTAG cells, and placement blockage for power and ground stripes. You must assign these objects before running placement.

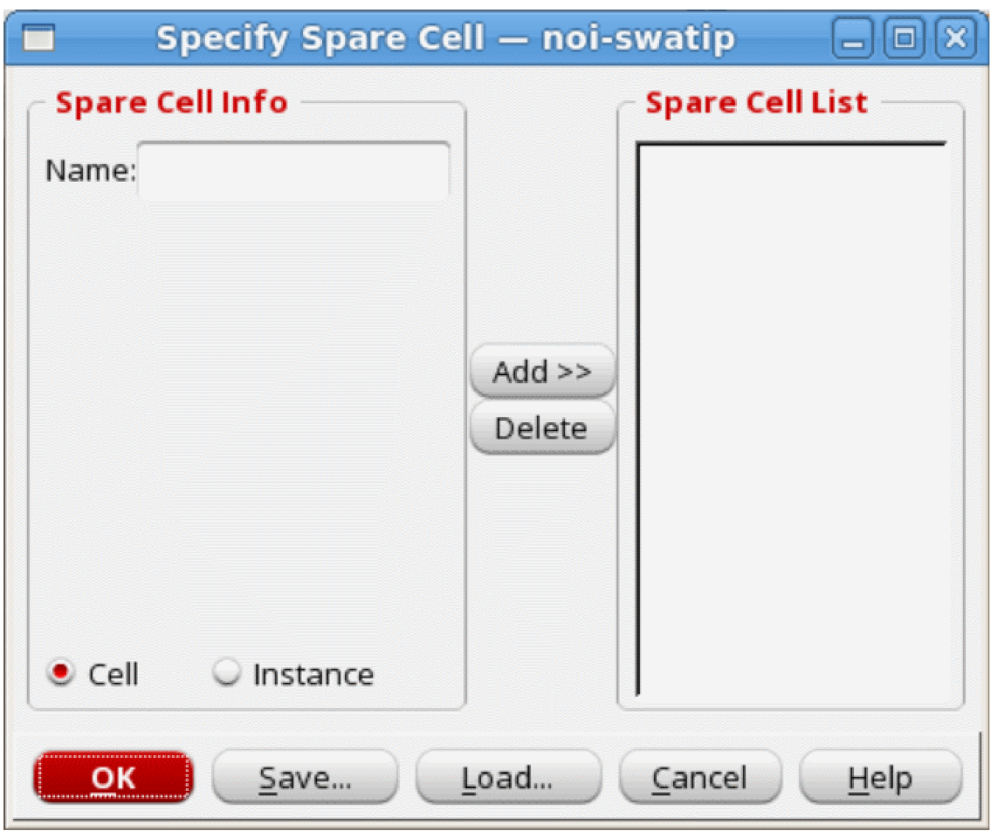
The *Specify* submenu provides access to the following features:

- Spare Cell
- Cell Padding
- Jtag Cell
- Placement Blockage

Spare Cell

Use the Specify Spare Cell form to assign cell types or modules that are designated as spare cells in the design.

Note: The module that contains the spare gates should be guided during the floorplanning session to localize the spare gate cell placements.
→ Choose *Place* - *Specify* - *Spare Cell*.



Specify Spare Cell Fields and Options

Name	Specifies the library cell of instance to designate as a spare cell.
Cell	Specifies that *Name* is a library cell. Use this option for for leaf cells (standard cells) only--it cannot be used for spare modules.
Instance	Specifies that *Name* is an instance of a library cell.
Add >>	Adds *Name* to the *Spare Cell List*.
Delete	Removes *Name* from the *Spare Cell List*.

Related Text Commands

- `specifySpareGate`

- For cases where several spare cells are specified, it is faster to use the `specifySpareGate` command than the *Specify Spare Cell* form.
- For cases where several spare cells are specified, it is faster to use the `specifySpareGate` command than the *Specify Spare Cell* form.

Related Topics

For information on the following topic, see the following section in the Placing the Design chapter of the *Innovus User Guide*.

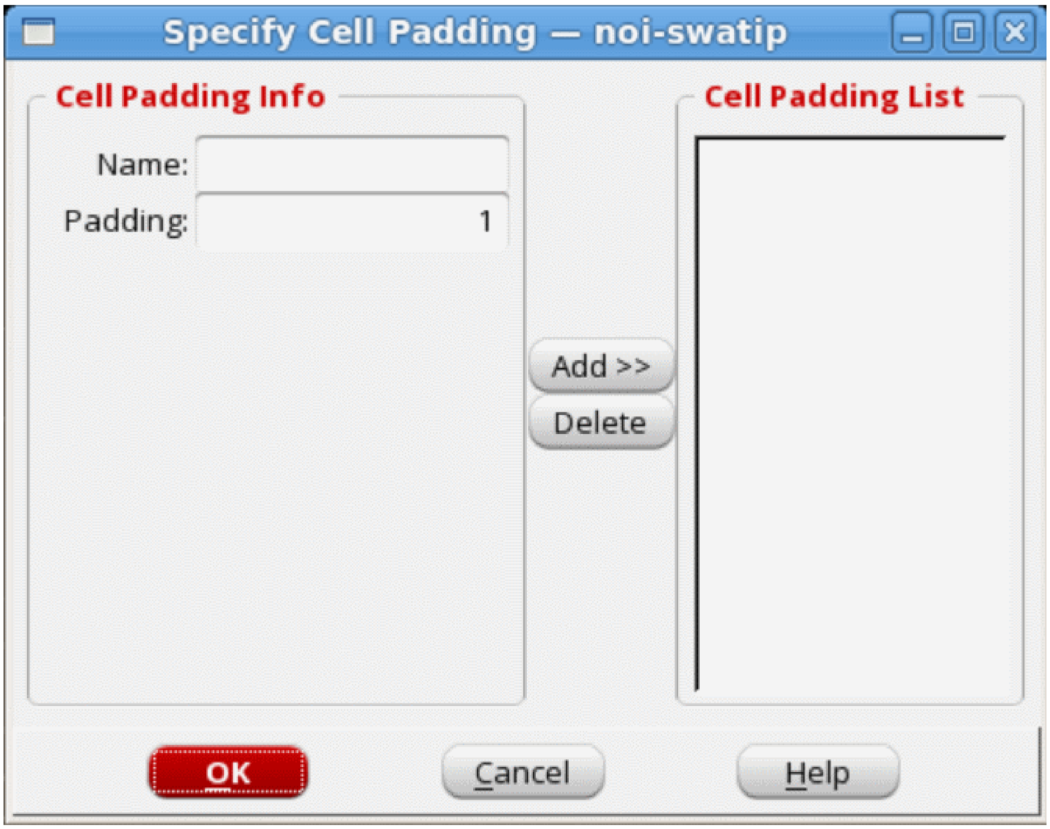
- Specifying Spare Cells

Cell Padding

Use the Specify Cell Padding form to assign cell types, such as clock flip-flops, with a small placement clearance so that a buffer can be inserted during clock tree synthesis. When the cell is placed, this clearance is on the right side of the cell. Cell padding is retained during optimization and CTS. If there are any congestion problems, delete the cell padding.

Use the `deleteAllCellPad` command to remove the padding.
→ Choose *Place* - *Specify* - *Cell Padding*.

Note: You can also save or load the spare cell information to or from the floorplan file.



Specify Cell Padding Fields and Options

Name	Specifies the cell to which to add or delete padding.
Padding	Specifies the numerical value of the padding dimension. The value is multiplied by the *metal2* pitch value to determine the padding dimension. The *metal2* pitch value is read from the technology file. *Default:* one *metal2* pitch.
Add >>	Adds the pad assignment to the *Cell Padding List*.
Delete	Removes the pad assignment from the *Cell Padding List*.

Related Text Commands

- `specifyCellPad`

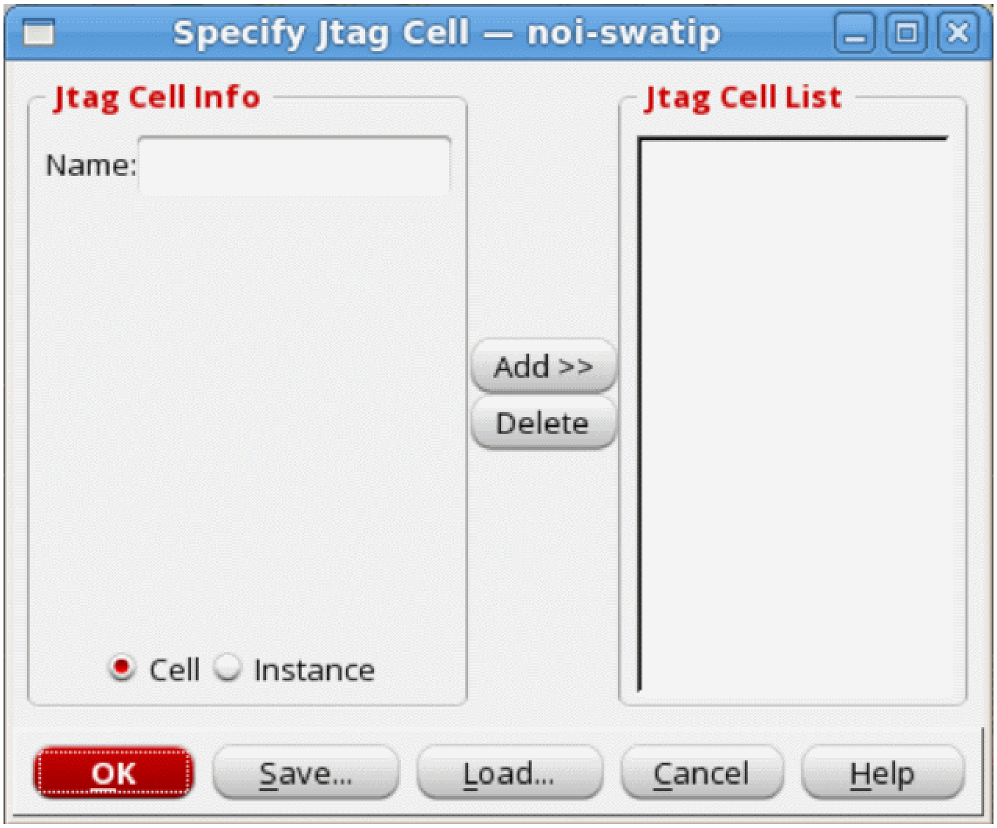
Related Topics

For information on the following topic, see the following section in the Placing the Design chapter of the *Innovus User Guide*.

- Specifying Cell Padding

Jtag Cell

Use the Specify Jtag Cell form to specify the modules that contain the JTAG logic. You can also use this form to save and load your specification data.
→ Choose *Place - Specify - Jtag Cell*.



Specify Jtag Cells Fields and Options

Name	Specifies a cell or instance. If you select *Instance*, you can use the asterisk wildcard (`*`) character.
Cell	Marks all instances of the specified cell type as JTAG instances.
Instance	Marks an instance as a JTAG instance. You can use a wildcard (`*`) character for this parameter.
Add >>	Adds *Name* to the *Jtag Cell List*.
Delete	Removes *Name* from the *Jtag Cell List*.

Related Text Commands

- `specifyJtag`

Related Topics

For information on the following topic, see the following section in the Placing the Design chapter of the *Innovus User Guide*.

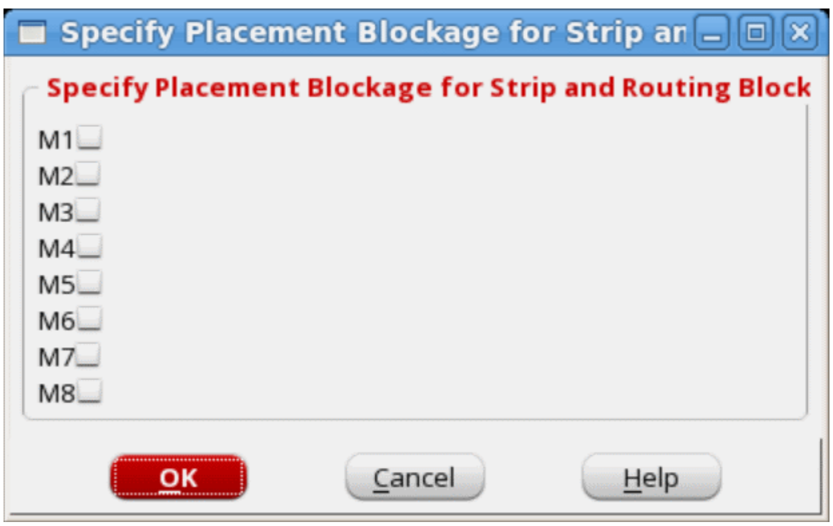
- Running JTAG Placement

Placement Blockage

Use the Specify Placement Blockage for Strip and Routing Blockage form to treat routing blockage objects and wires with the DEF attribute `+ SHAPE STRIPE` on the specified layers as placement blockages so that placement commands do not place cells under them.

Note: Preplaced instances are not moved by the placement commands, even if they violate the specified blockage.

Note: Filler cells are still added under preroute wires.
→ Choose *Place* - *Specify* - *Placement Blockage*.



Note: For fine but dense power lines, deselect the metal layers in the form. Cells will be positioned underneath the power stripes, and will not block the interconnection.

Specify Placement Blockage for Strip and Routing Blockage Fields and Options

M1 M2 M3 M4 M5 M6 M7 M8	Specify the metal layer numbers.

Related Text Commands

- `setPlaceMode -place_detail_preroute_as_obs`

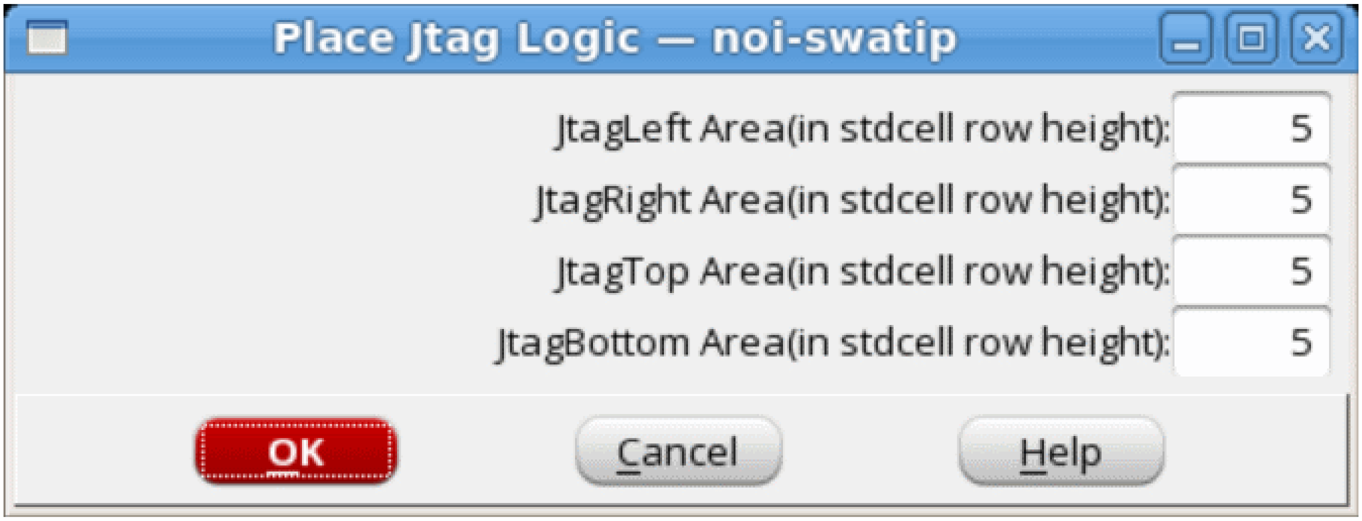
Related Topics

For information on the following topic, see the following section in the Placing the Design chapter of the *Innovus User Guide*.

- Guiding Placement With Blockages

Place Jtag

Use the Place Jtag Logic form to place JTAG instances close to their I/O pads.
→ Choose *Place* - *Place Jtag*.



Place Jtag Logic Fields and Options

Jtag Left Area	Specifies the standard cell row height for the left side of the JTAG placement area. *Default:* 5 (approximately five times the standard cell height. This creates a temporary placement blockage layer during JTAG placement, and is removed thereafter.
Jtag Right Area	Specifies the standard cell row height for the right side of the JTAG placement area. *Default:* `5` (approximately five times the standard cell height. This creates a temporary placement blockage layer during JTAG placement, and is removed thereafter.
Jtag Top Area	Specifies the standard cell row height for the top of the JTAG placement area. *Default:* `5` (Places the JTAG instance within five standard cell rows at the top of the chip.)
Jtag Bottom Area	Specifies the standard cell row height for the bottom of the JTAG placement area. *Default:* `5` (Places the JTAG instance within five standard cell rows at the bottom of the chip.)

Related Text Commands

- `placeJtag`
- `traceJtag`

Related Topics

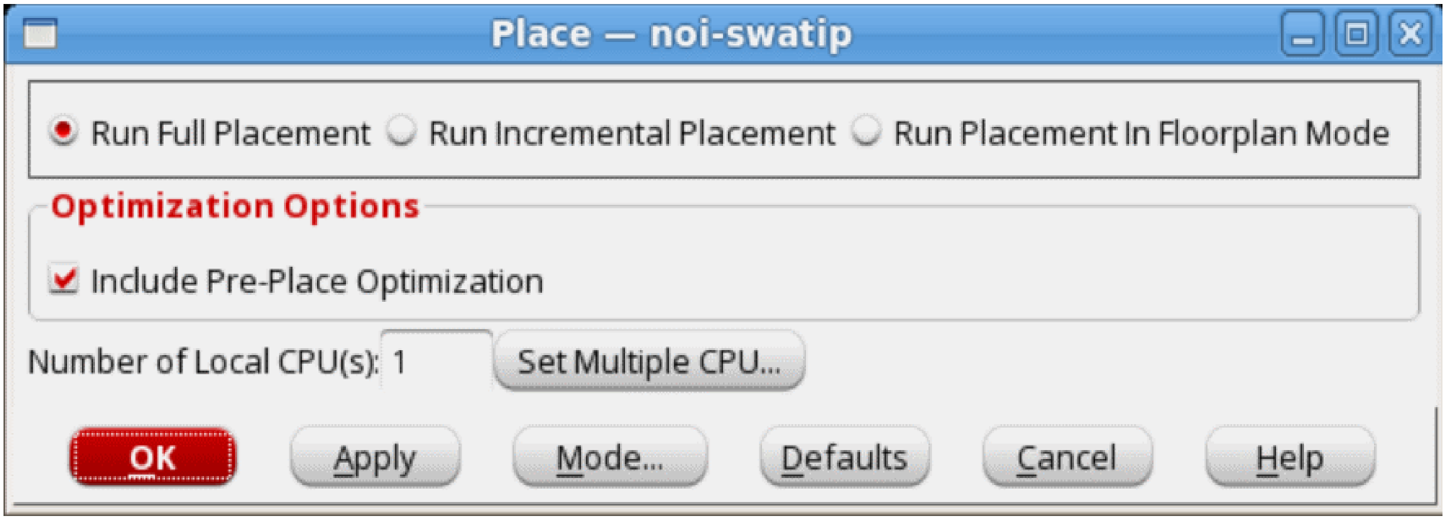
For information on the following topic, see the following section in the Placing the Design chapter of the *Innovus User Guide*.

- Running JTAG Placement

Place Standard Cell

Use the *Place* form to place standard cells in the design based on the global settings for placement, RC extraction, timing analysis, and early global routing. The placement commands consider the modules that were placed (guided) during floorplanning, and take into account the design's hierarchy and connectivity.

→ Choose *Place - Place Standard Cell*.



Place Fields and Options

Run Full Placement	Runs placement in timing-driven mode, based on the global settings for placement, RC extraction, timing analysis, and early global routing. It also relieves the congestion, and reorders the scan cells. *Default:* On
Run Incremental Placement	Reruns placement in timing-driven mode while honoring current placement. *Default:* Off
Run Placement in Floorplan Mode	Runs a quick placement to gauge the feasibility of the netlist, but might not place components in legal locations. This mode assumes non-timing-driven placement. *Default:* Off **Note:** In this mode the *Include In-Place Optimization* option is disabled.
Optimization Options	
Include Pre-Place Optimization	Simplifies the netlist, for example, by deleting buffer trees, before running placement. *Default:* On
Number of Local CPUs	Displays the number of threads to use for multiple-CPU processing. **Note:** This is a non-editable field. To edit this field, select *Set Multiple CPU*.
Set Multiple CPU	Opens the Multiple CPU Processing form. For more information, see Tools Menu - Set Multiple CPU Usage.
Mode	Helps you in selecting different modes for placement of standard cells. For more information, see Tools Menu - Mode Setup - Placement.
Defaults	Sets the default values.

Related Text Command

- `place_design`

Related Topics

For information on the following topics, see "Placing the Design" in the *Innovus User Guide*.

- Placing Standard Cells

Place Spare Cell

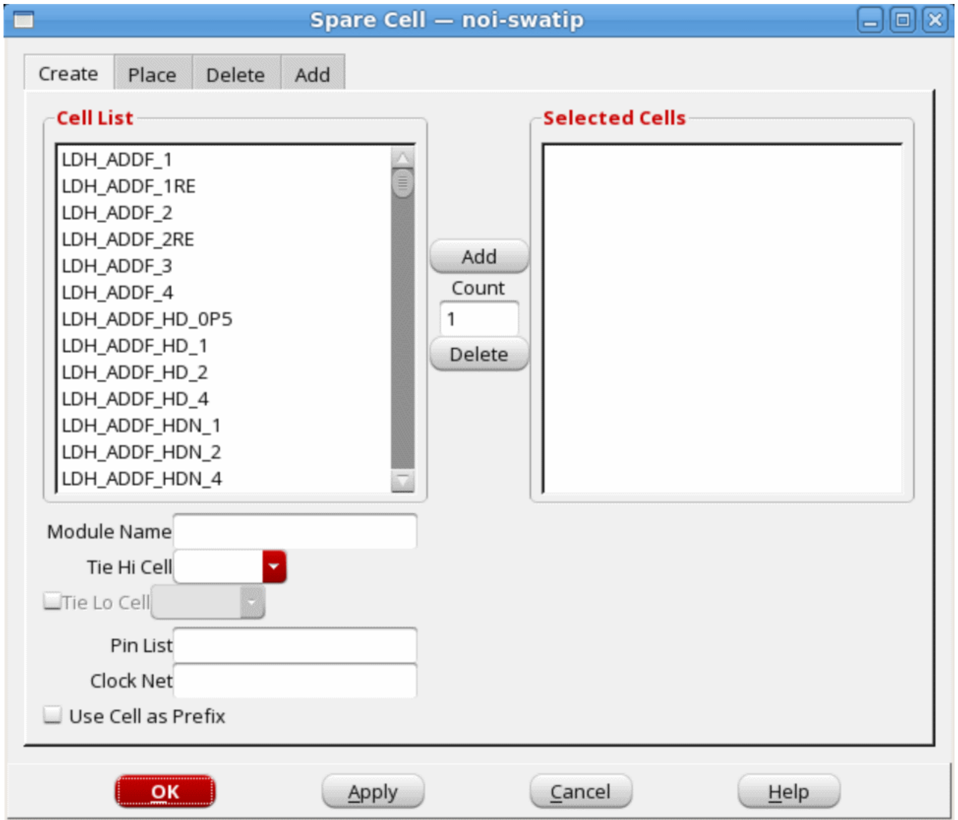
Use the Spare Cell form to place a group of designated instances together as a spare module, with a constraint in the floorplan file, and distributed across the design by the number of rows and columns. The use of modules helps to ensure that the designated spare instances stay together, and makes it easy to place multiple copies of the group in the design. This can be done after placement.

The Spare Cell form contains the following pages:

- Spare Cell - Create
- Spare Cell - Place
- Spare Cell - Delete
- Spare Cell - Add

Spare Cell - Create

Use the *Create* page of the Spare Cell form to specify the cells to add to a module and to name the module.
→ Choose *Place* - *Spare*, then click the *Create* tab.


Spare Cell — noi-swatip
Create
Place
Delete
Add
Cell List
LDH_ADDF_1
LDH_ADDF_1RE
LDH_ADDF_2
LDH_ADDF_2RE
LDH_ADDF_3
LDH_ADDF_4
LDH_ADDF_HD_0P5
LDH_ADDF_HD_1
LDH_ADDF_HD_2
LDH_ADDF_HD_4
LDH_ADDF_HDN_1
LDH_ADDF_HDN_2
LDH_ADDF_HDN_4
Add
Count
1
Delete
Selected Cells
Module Name
Tie Hi Cell
Tie Lo Cell
Pin List
Clock Net
Use Cell as Prefix
OK
Apply
Cancel
Help

Spare Cell - Create Fields and Options

Cell List	Displays a list of spare cells that can be added to the module.
Selected Cells	Displays the list of spare cells that are selected to add to the module.
Add	Adds highlighted cells in the *Cell List* to the *Selected Cells* box.
Count	Displays the number of cells in the *Selected Cells* box.
Delete	Removes highlighted cells from the *Selected Cells* box.
Module name	Specifies a name for the spare module.
Tie Hi Cell	Specifies a tie-high cell to add to the spare module.
Tie Lo Cell	Specifies a tie-low cell to add to the spare module.
Pin List	Specifies pins to connect to a cell specified in the *Tie Lo Cell* field. If you do not specify a tie-low cell in the *Tie Lo Cell* field, any pins you list in this field are tied to `1'b0`.
Clock Net	Specifies a clock net to connect to the clock pins of the instances in the spare module.
Use Cell as Prefix	Adds the master cell name as a prefix to the name of gates that are instantiated inside the module. The software adds `spr_gate_`*n* as a prefix by default; when you select this option, it prepends the master cell name to the default prefix.

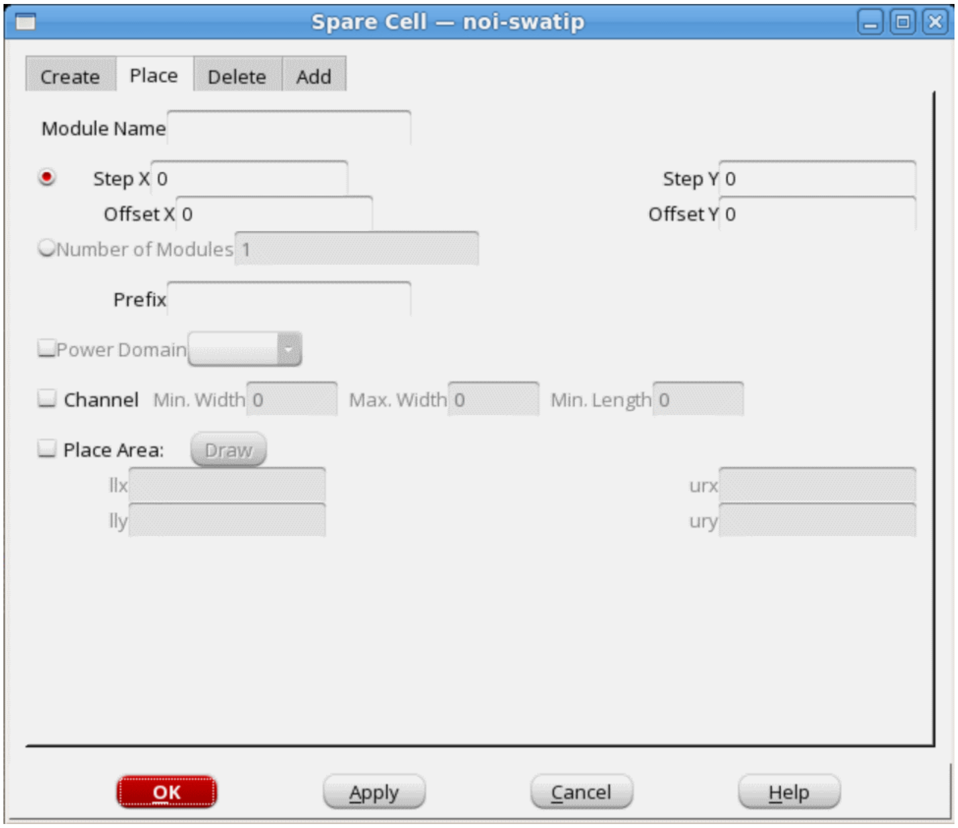
Related Text Commands

- `createSpareModule`

Spare Cell - Place

Use the *Place* page of the Spare Cell form to instantiate the created spare module and place copies of the spare module across the design. You can place spare modules before or after placement. To place them after placement, the software runs ECO placement.

→ Choose *Place* - *Spare*, then click the *Place* tab.



Spare Cell - Place Fields and Options

Module Name	Specifies the name of the spare module. This module must have been created using *Spare Cell - Create*.
Step X	Specifies the distance, in microns, between the instantiated spare modules along the x axis. The distance must be greater than the spare module bounding box.
Step Y	Specifies the distance, in microns, between the instantiated spare modules along the y axis. The distance must be greater than the spare module bounding box.

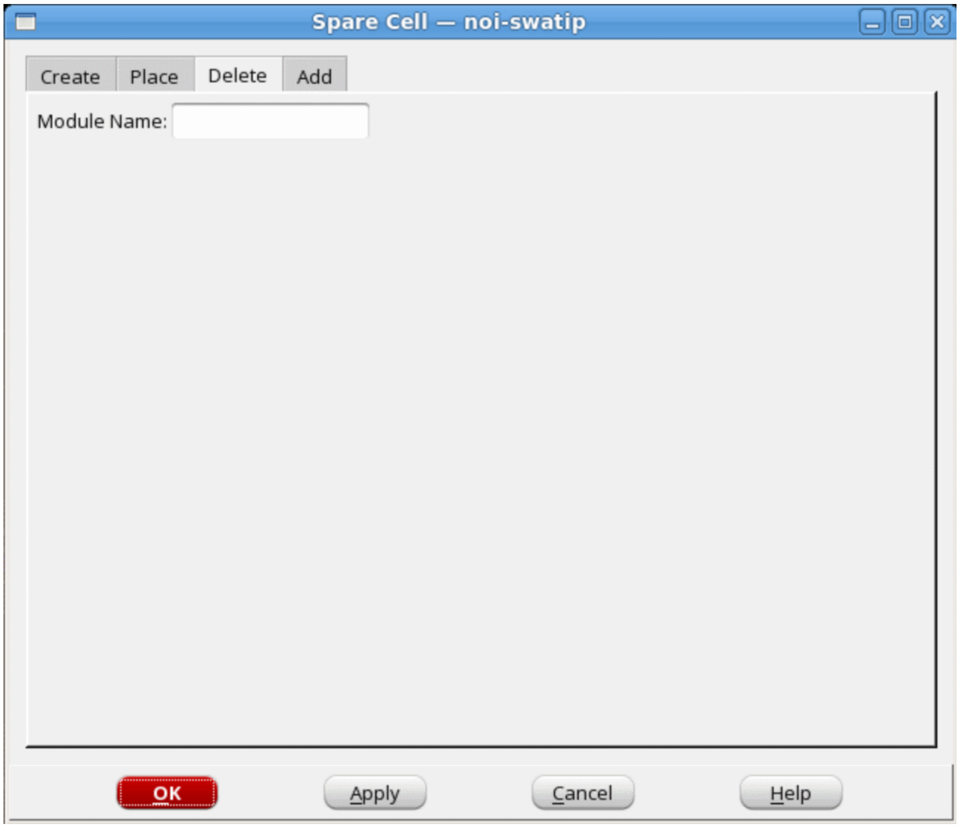
Offset X	Specifies the offset along the x axis, in microns, from the left core boundary.	
Offset Y	Specifies the offset along the y axis, in microns, from the left core boundary.	
Number of Module	Specifies the number of spare modules to add. *Default:* `1`	
Prefix	Specifies a prefix to add to the automatically generated prefix for spare modules. The software already uses the prefix `spr_` *`n`* for spare modules. If you specify `spareMod`, the instances of this module are named `spareMod_spr_1`, `spareMod_spr_2`, `spareMod_spr_3`, and so on.	
Power Domain	Specifies the power domain in which to place the spare modules.	
Channel	Places the spare modules in the channels between placement blockages	
	Min Width	Specifies the minimum channel width, in microns. The *Min Width* should be greater than the width of the largest-space cell provided.
	Max Width	Specifies the maximum channel width, in microns. The *Max Width* determines whether the placeable area between two macro blocks is considered a channel.
	Min Length	Specifies the minimum channel length, in microns. The *Min Length* must be greater than the specified *Max Width*.
Place Area	Specifies an area in the design where the spare modules are placed. Select the *Draw* button, click in the design display area, and draw a box to retrieve the x and y coordinates, or type the corners of the box in the *llx*, *urx*, *lly*, and *ury* text entry boxes.	

Related Text Commands

- `placeSpareModule`

Spare Cell - Delete

Use the *Delete* page of the Spare Cell form to delete the spare module from the netlist.
→ Choose *Place* - *Spare*, then click the *Delete* tab.



Spare Cell - Delete Fields and Options

Module Name	Specifies the name of the spare module.

Related Text Commands

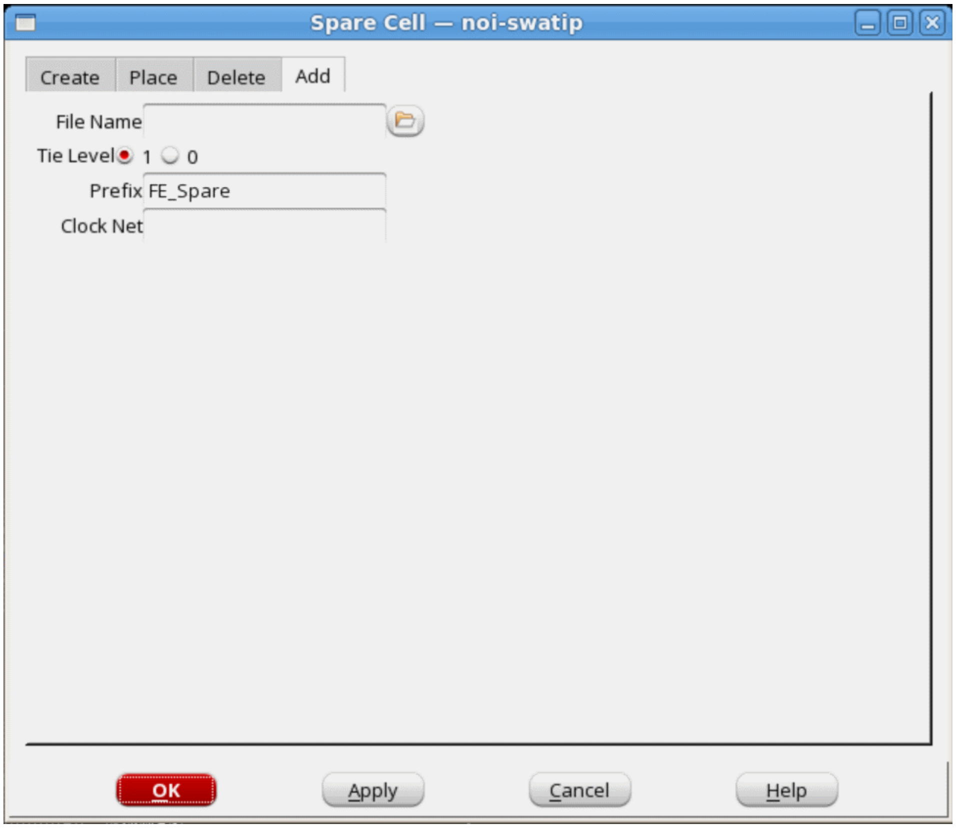
- `deleteSpareModule`

Spare Cell - Add

Use the *Add* page of the Spare Cell form to add spare cells to the netlist without including them in spare modules.

- If you use this page before placement, the `place_design` command distributes and places the added instances without including them in spare modules. It adds the instances to the top level of the design by default.
- If you use this page after placement, the software places the added instances without creating spare modules or disturbing the existing placement. The distribution of the cells is dependent upon the number of instantiations of each cell type.

→ Choose Choose *Place* - *Spare*, then click the *Add* tab.



Spare Cell - Add Fields and Options

File Name	Specifies a text file that lists the spare cells, and the number of each, to add to the netlist.
Tie Level	Specifies the logical net to which the cells are connected. *Default:* `1`
Prefix	Specifies a prefix for the names of the newly added cells. *Default:* `FE_spare`
Cock Net	Specifies the clock net that is tied to the clock pins.

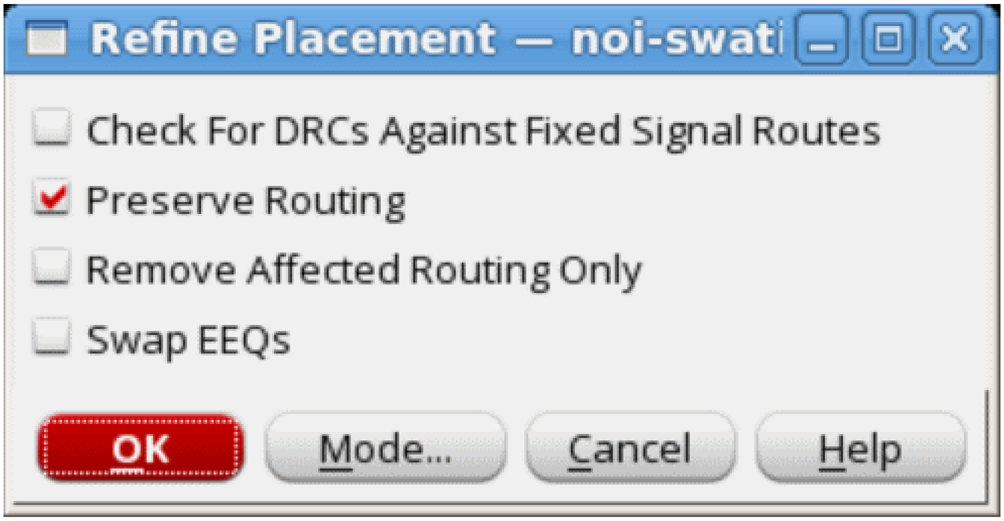
Related Commands

- `addSpareInstance`

Refine Placement

Use the *Refine Placement* form to correct flawed cell locations and report corrections or instance overlap problems.

You do not need a fully placed design in order to refine placement.
→ Choose *Place - Refine Placement*.



Refine Placement Fields and Options

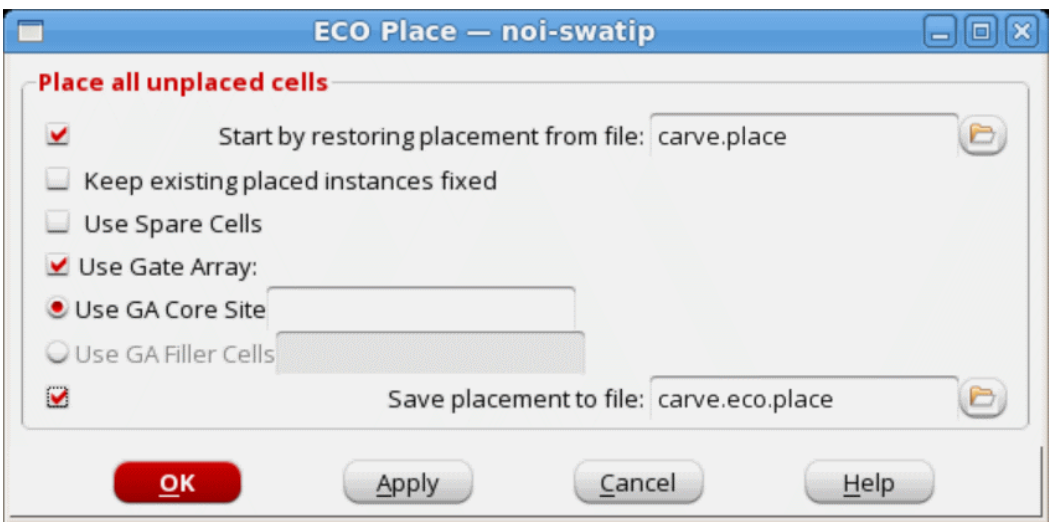
Check For DRCs Against Fixed Signal Routes	
	Considers pre-routed `FIXED` signal wires and avoids creating DRC violations between `FIXED` signal wires and instance pins. When this option is not selected, the software ignores `FIXED` signal wires. *Default:* Off **Note:** Running placement with this option selected might result in longer run time.
Preserve Routing	Preserves all routed wires. *Default:* Off. Refine Placement removes all wires.
Remove Affected Routing Only	
	Removes wires connected to moved cells. *Default:* Off. Refine Placement removes all wires, whether connected cells were moved or not.
Swap EEQs	Specifies whether master cells can be replaced by EEQ cells during detailed placement to improve routability. After detailed placement, the software reports the number of replacements. EEQ cells are defined in the LEF file. *Default:* Off

Related Text Commands

- refinePlace

ECO Placement

Use the ECO Place form to run netlist ECO (Engineering Change Order) placement. You can set global options for incremental placement of standard cells. In a pre-mask flow, this command moves the unplaced standard cells into the core area. In a post-mask flow , the software can map the unplaced cells to the available spare cells. Use this form for minor design changes. The ECO for logic changes should not exceed 20 percent from the previous imported design.
→ Choose *Place* - *ECO Placement*.



ECO Place Fields and Options

Start by restoring placement from file:	Restores an existing placement file before placing ECOs. This placement file is saved from the previous netlist that was imported and placed in the Innovus Implementation System (Innovus) software. Running ECO Placement will change this design as per the new imported netlist. The placement file format must be from the Innovus software.
Keep existing placed instances fixed	Specifies that instances with the PLACED status are not moved.
Use Spare Cells	Maps unplaced cells to spare cells during placement. First, checks whether all unplaced cells match spare cells. Next, chooses a spare cell and changes the connections from the unplaced cell to the selected spare cell. Finally, deletes the unplaced cell. You can use this parameter only for post-mask ECO. This option observes the power domain when selecting the spare cell and maps an unplaced cell to the spare cell in the power domain, based on the instance name of the cell. For example, if module A/B is defined for power domain PD2, this option will map an unplaced cell A/B/inst1 to a spare cell in module A/B.
Use GA Core Cells	Specifies a list of Gate Array (GA) cells. The tool matches the GACoreSite to available spare cells. The tool chooses a spare cell and changes the connections from the unplaced cell to the selected spare cell. You can use this parameter only for post-mask ECO.
Use GA Filler Cells	Specifies a list of Gate Array (GA) filler cells that the tool can replace with GA cells during post-mask ECO. You can only use this parameter in a post-mask ECO flow. The new logic instances adding during a post-mask flow must already be present in the netlist.
Save Placement to file	Specifies the filename to save the placement results.

Related Text Commands

- `ecoPlace`

Related Topics

For information on the following topic, see "ECO Placement" in the *Innovus User Guide*.

- Running ECO Placement

Physical Cell

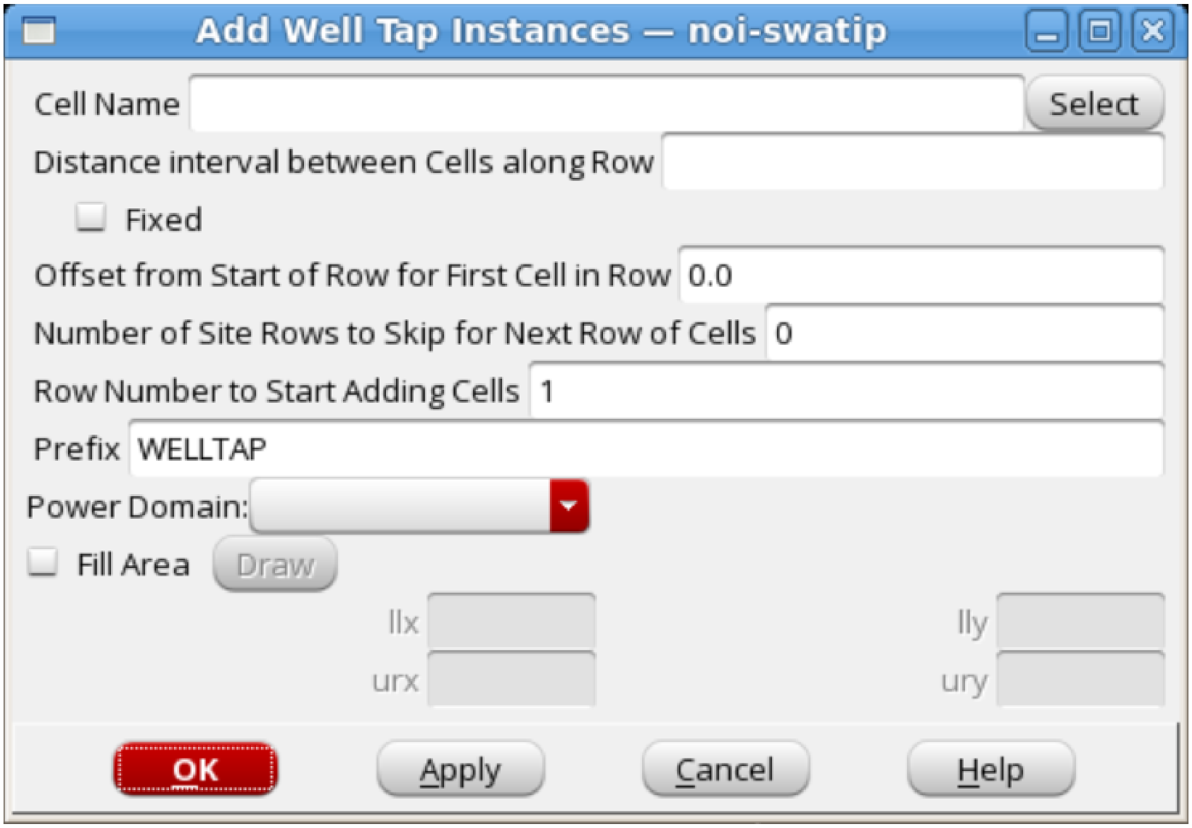
The *Place* menu's Physical Cell submenu enables you to add or delete filler, well tap, end cap, and I/O filler cells.

The *Physical Cell* submenu provides access to the following items:

- Add Well Tap Instances
- Add End Cap
- Add Filler
- Delete Filler
- Add I/O Filler
- Delete I/O Filler
- Check Filler

Add Well Tap Instances

Use the Add Well Tap Instances form to place physical-only well-tap cells.
→ Choose *Place - Physical Cell - Add Well Tap*.



Add Well Tap Instances Fields and Options

Cell Name	Specifies the name of the cell in the technology library of class type `CORE` to use as a well-tap. You can type the cell name, or click *Select* to open a list of cells where you can click a cell name and click *OK* to add the cell name to the field.
Distance interval between Cells along Row	Specifies the distance, in microns, between two consecutive well-tap cells on a row. If well-tap cells cannot be placed at this gap due to placement blockage, the software will search for a legal location: first towards the previous well-tap, and then away from the specified location.
Fixed	Ensures that the specified gap is always maintained. The software does not search for a legal location if it cannot place well-tap cells at the specified *Max. Gap*. Instead, it goes on to place well-tap cells at the next position.

Offset from Start of Row for First Cell in Row	Specifies the offset, in microns, of the first well-tap cell from the start of the site row. *Default:* `0` (The first cell on beginning of row is the starting point.)
Number of Site Rows to Skip for Next Row of Cells	Specifies the row number from bottom (or left) on which the well-taps have to be placed. *Default:* `1` (Specifies that the first row from the bottom is the starting point.)
Prefix	Specifies the prefix for the placed instances. The generated name for the instance uses this prefix as `prefix_` *`uniqueString`* . *Default:* `WELLTAP` ⓘ Do not include an underscore at the end of the prefix.
Power Domain	Select the specific power domain for Well Taps insertion. If no power domain is specified, Well Taps will be inserted in all power domains by default.
Fill Area	Specifies the coordinates of the bounding box, in microns, for the lower left (*llx*) and upper right (*urx*) boundaries in the x-direction, and the lower left (*lly*) and upper right (*ury*) boundaries in the y-direction. You can type in the fields, or click *Draw* and use the left mouse button to drag over an area in the design display area to get the boundary coordinates. **Note:** If the area is not defined properly, well-tap instances are not added.

Related Text Commands

- `addWellTap`

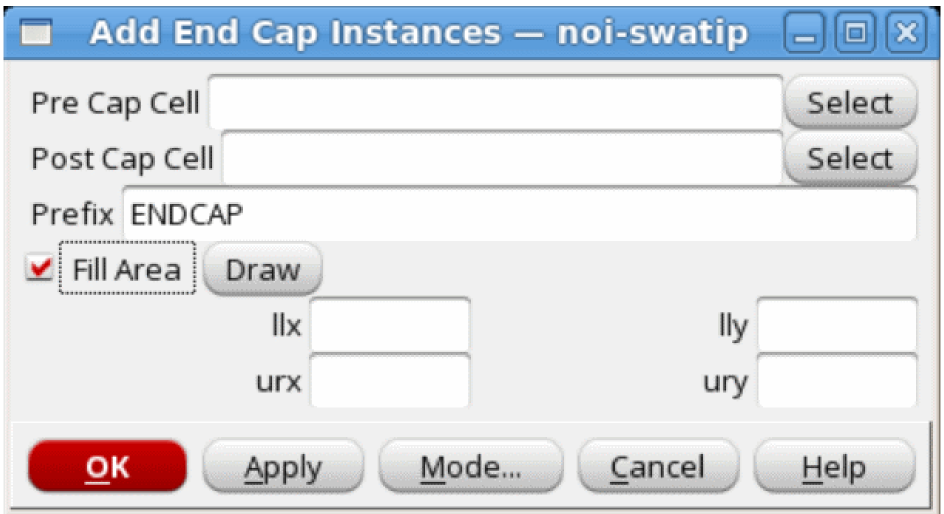
Related Topics

For information on the following topic, see "Placing the Design" in the *Innovus User Guide*.

- Adding Well-Tap Cells

Add End Cap

Use the Add End Cap Instances form to place physical-only end-cap cells at the ends of the site rows.
→ Choose *Place - Physical Cell - Add End Cap*.



Add End Cap Instances Fields and Options

Pre Cap Cell	Specifies the name of the cell in the technology library to use to cap the beginning of each site row. You can type the cell name, or click *Select* to open a list of cells where you can click a cell name and click *OK* to add the cell name to the field.
Post Cap Cell	Specifies the name of the cell in the technology library to use to cap the end of each site row. You can type the cell name, or click *Select* to open a list of cells where you can click a cell name and click *OK* to add the cell name to the field.
Prefix	Specifies the prefix for the placed instances. The generated name for the instance uses this prefix as `prefix_` *`uniqueString`* . The default is `ENDCAP`. ⓘ Do not include an underscore at the end of the prefix name.
Fill Area	Specifies the coordinates of the bounding box, in microns, for the lower left (*llx*) and upper right (*urx*) boundaries in the x-direction, and the lower left (*lly*) and upper right (*ury*) boundaries in the y-direction. You can type in the fields, or click *Draw* and use the left mouse button to drag over an area in the design display area to get the boundary coordinates. **Note:** If the area is not defined properly, end cap instances will not be added.

Related Text Commands

- `addEndCap`

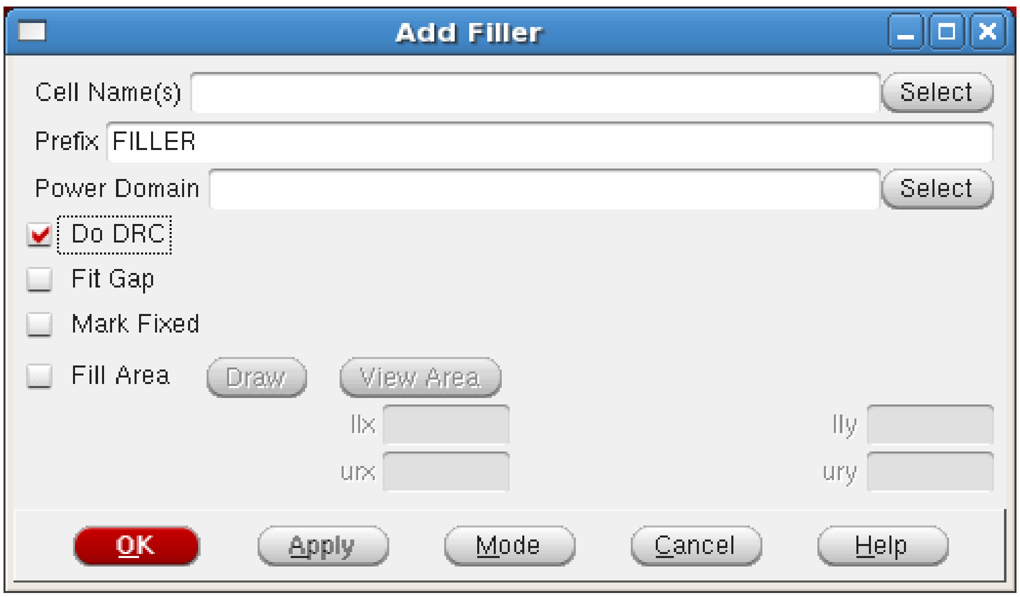
Add Filler

Use the Add Filler form to insert filler cell instances between the gaps of standard cell instances. If the design is routed, the software does DRC checks of the filler cells added to the wires in the design. It does not check adjacent cells. This process ensures that adding filler cells is fast enough to be used many times in the design flow.

To resolve adjacent cell DRC violations created by the insertion of filler cells, run Verify Geometry to mark these violations. Then, use Add Filler with *No DRC* turned off to add more filler cells to replace filler cells that cause violations.

Note: This command resolves only filler-related violations--it cannot resolve net-based violations. To repair net-based violations, reroute the net with violations.

Add Filler recognizes up to five implant layers and attempts to honor implant layer width and spacing rules within each implant layer. If it does not find the correct filler cell to add to an implant layer, it tries to add "no-implant" filler cells. If it cannot add the "no-implant" cells, it inserts a filler cell that is large enough that it does not violate the minimum width rule of the relevant implant layer.
→ Choose *Place - Physical Cell - Add Filler*.



Add Filler Fields and Options

Cell Name(s)	Specifies the cell name(s) of the filler cell instance. Click *Select* to open a browser to highlight a cell, or cells, from the *Selectable Cells List*. Clicking *Add* includes the cell name(s) to the *Cells List* and *Cell Name(s)* field. Highlighting a cell or cells in the *Cells List* and clicking *Delete* removes the cell name(s) from both areas.
Prefix	Specifies the prefix for the added filler cell instances. *Default:* `FILLER`
Power Domain	Specifies the power domain in which the fillers are to be inserted. If this parameter is not specified, and a list of filler cells is specified with *Cell Name(s)*, the software tries to add fillers to all power domains. Click *Select* to open a browser to highlight a cell, or cells, from the *Selectable Power Domain List*. Clicking *Add* includes the cell name(s) in the *Cells List* and *Cell Name(s)* field. Highlighting a cell or cells in the *Cells List* and clicking *Delete* removes the cell name(s) from both areas.
Do DRC	Controls postroute DRC violation checking against existing net routing, without considering adjacent cell DRC violations. This parameter does not disable regular placement checks. *Default:* On
Fit Gap	Fills a gap between cells by adding a combination of cells, instead of by adding the single largest cell that fits, if doing so avoids leaving an unfilled single-width gap.
Mark Fixed	Marks added fillers as `FIXED`. *Default:* Off
Fill Area	Specifies an area to fill. Specify values for the lower left (*llx*) and upper right (*urx*) boundaries in the x-direction, and the lower left (*lly*) and upper right (*ury*) boundaries in the y-direction. Use *Draw* to click and drag a window around the area in the design display area. This will automatically update the values for the boundaries. **Note:** If the area is not defined properly, no filler cells are added.

Related Text Commands

- addFiller

Related Topics

For information on the following topic, see "Placing the Design" in the *Innovus User Guide*.

- Adding Filler Cells

Delete Filler

Use the Delete Instances form to remove physical cell instances, filler cells, end-cap cells, and well-tap cells from standard cell rows.

→ Choose *Place - Physical Cell - Delete Filler*.

Delete Instances Fields and Options

Cell Name	Specifies the cell name, or list of cells, to remove. Separate cell names with spaces. Type the cell name, or click *Select* to open the a list of cells where you can click a cell name and click *Add* to add the cell name(s) to the field.
Prefix	Specifies the prefix of the filler cell instances to remove. This command adds an underscore at the end of the provided prefix while checking it against the instance names.
Fill Area	Specifies the coordinates of the bounding box, in microns, for the lower left (*llx*) and upper right (*urx*) boundaries in the x-direction, and the lower left (*lly*) and upper right (*ury*) boundaries in the y-direction. By default, the core box that encloses all core rows is used. Type in the fields, or click *Draw* and use the left mouse button to drag over an area in the design display area to get the boundary coordinates.

Related Text Commands

- `deleteFiller`

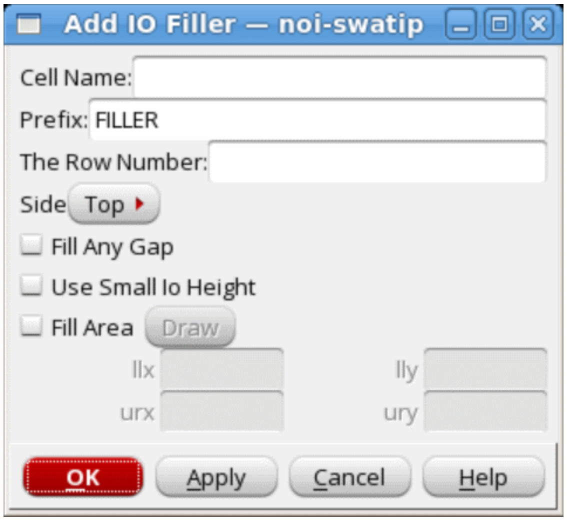
Related Topics

For information on the following topic, see "Placing the Design" in the *Innovus User Guide*.

- Adding Filler Cells

Add I/O Filler

Use the Add IO Filler form to add I/O instances to the I/O box netlist.
→ Choose *Place - Physical Cell - Add I/O Filler*.


Add IO Filler — noi-swatip
Cell Name:
Prefix: FILLER
The Row Number:
Side Top
Fill Any Gap
Use Small Io Height
Fill Area
Draw
llx
lly
urx
ury
OK
Apply
Cancel
Help

Add IO Filler Fields and Options

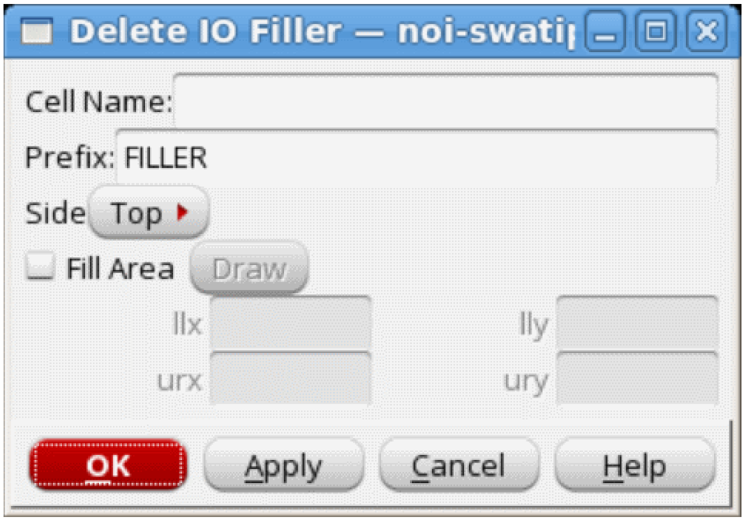
Cell Name	Specifies the name of the I/O filler cell to add.
Prefix	Specifies the prefix name to be appended for the added I/O filler instance.
The Row Number	Specifies the row number of the I/O pads (in multiple ring I/O pads) to insert the fillers.
Side	Specifies the side as the Top, Bottom, Left, or Right side of the I/O box. *Default:* By default, the top side is used.
Fill Any Gap	If selected, forces the I/O filler instance into a gap even though the gap (clearance) is not large enough.
Use Small IO Height	Specifies that the filler cell should be inserted between I/O pads only when the smallest I/O pad has the same height as the height of the filler cell. For example, consider that there are I/O pads A, B, C, D, and E. Out of these, A, B, and E are the same height, and C and D have a height double that of A, B, and E. Assume that you want to insert an I/O filler cell F, which has the same height as A, B, and E. If you do *not* specify this option, the cell F will be inserted between A and B, B and C, C and D, and D and E. If you specify this option, the cell F will be inserted between A and B, B and C, and D and E. However, the cell will not be inserted between C and D, because both C and D have a height different from F.
Fill Area	Specifies the lower-left and upper-right x and y coordinates of the range where I/O filler cells are added. The values are in micrometers.
Draw	You can click the *Draw Box* button to physically draw a box in the design window corresponding to the coordinates of the range where I/O filler cells will be added.

Related Text Commands

- `addIoFiller`

Delete I/O Filler

Use the Delete IO Filler form to delete I/O filler cell instances from the design.
→ Choose *Place - Physical Cell - Delete I/O Filler*.



Delete IO Filler Fields and Options

Cell Name	Specifies the name of the I/O filler cell to delete.
Prefix	Specifies the prefix name of the I/O filler instance to be removed.
Side	Specifies the side as the Top, Bottom, Left, or Right side of the I/O box where the I/O filler cells will be removed. *Default:* By default, the top side is used.
Fill Area	Specifies the lower-left and upper-right x and y coordinates of the range where I/O filler cells are to be deleted. The values are in micrometers.
Draw	You can click the *Draw Box* button to physically draw a box in the design window corresponding to the coordinates of the range where I/O filler cells will be deleted.

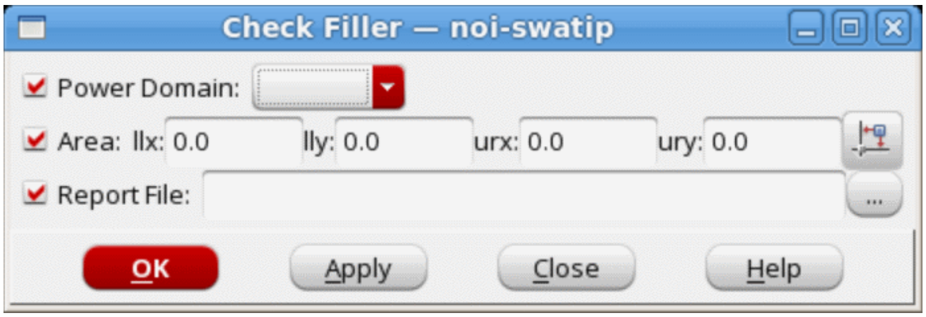
Related Text Commands

- `deleteIoFiller`

Check Filler

Use the Check Filler form to check for locations that are missing filler cells after adding the cells with the `addFiller` command. If any gaps are found, the software reports the number of sites that are missing filler cells in the log file. To generate a report, use the *Report File* option.

→ Choose *Place - Physical Cell - Check Filler*.



Check Filler Fields and Options

Power Domain	Checks only the specified power domain. *Default:* Checks all power domains.
Area	Limits the area to check to the specified area. *Default:* Checks the entire core area.
Report File	Generates a report that lists the locations that are missing filler cells. Specify a name for the report in the text-entry box. *Default:* The software reports the number of unoccupied sites in the log file.

Related Text Commands

- `checkFiller`

Related Topics

For information on the following topic, see "Placing the Design" in the *Innovus User Guide*.

- Adding Filler Cells

Tie Hi/Lo Cell

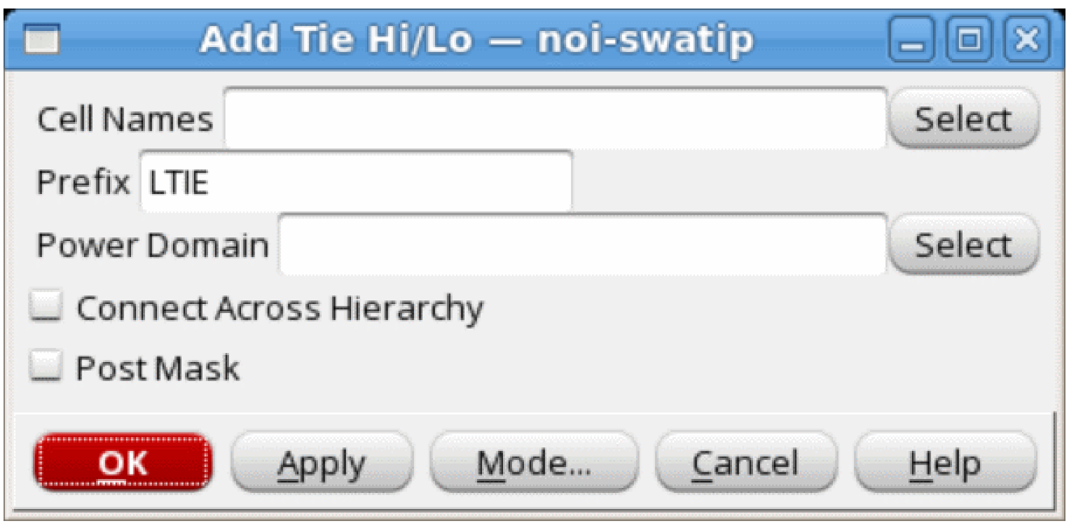
Use the Place menu's Tie Hi/Lo Cell submenu to add or delete tie high or tie low cells from the design and connect tie-off pins of netlist instances to tie-off pins of added instances.

The *Tie Hi/Lo Cell* submenu provides access to the following features:

- Add
- Delete

Add

Use the Add Tie Hi/Lo form to add instances of specified tie-off cells to the logical hierarchy of the design and connect the tie-off pins of netlist instances to the tie-off pins of the added instances. Thus, these instances provide the connectivity between the tie-high and tie-low pins of the netlist instances to power and ground.
→ Choose *Place - Tie Hi/Lo Cell - Add*.



Add Tie Hi/Lo Fields and Options

Cell Names	Specifies the names of the tie-off cell instances. You can specify a maximum of two tie cells, when one cell is a tie-high driver, and the other a tie-low driver. Click *Select* to open a browser to highlight a cell, or cells, from the *Selectable Cells List*. Clicking *OK* adds the cell name(s) to this field.
Prefix	Specifies the prefix for the added tie-off cell instances. *Default:* `LTIE`
PowerDomain	Specifies the power domain in which the tie-cells are inserted. This identifies the area where to place the tie-cells and connect to the correct power and ground nets. Click *Select* to open a browser to highlight a power domain from the *Selectable Power Domain*. Clicking *OK* adds the power domain name to this field.
Connect Across Hierarchy	Allows the added tie cells to connect to tie pins across hierarchical boundaries if other constraints, such as maximum fanout and maximum distance, allow it. The port connections are logged to a file named `tiehilo.rpt`. *Default:* Off
Post Mask	Instructs the software to reuse existing tie cells to tie off a newly created spare instance in the design instead of adding or deleting cells. Searches for input pins with the `tieHi` or `tieLo` property and attempts to them off to tie high or tie low cells.

Related Text Commands

- `addTieHiLo`
- `deleteTieHiLo`
- `getTieHiLoMode`
- `setTieHiLoMode`

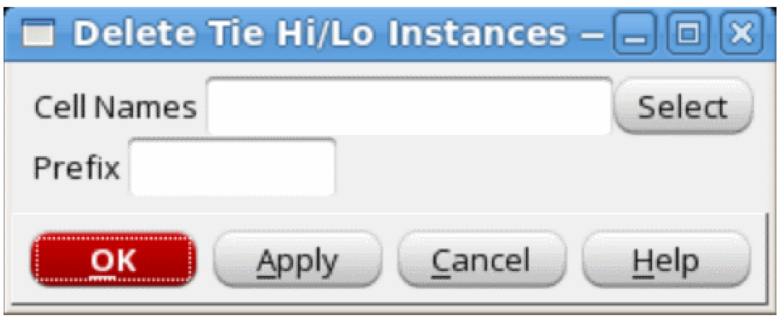
Related Topics

For information on the following topic, see "Placing the Design" in the *Innovus User Guide*.

- Adding Logical Tie-Off Cells

Delete

Use the Delete Tie Hi/Lo Instances form to remove logical tie-off cell instances from the netlist and reconnect the tie input pins.
→ Choose *Place - Tie Hi/Lo Cell - Delete*.



Delete Tie Hi/Lo Instances Fields and Options

Cell Names	Specifies the names of the tie-off cell instances to delete. Click *Select* to open a browser to highlight a cell, or cells, from the *Selectable Cells List*. Clicking *OK* adds the cell name(s) to this field.
Prefix	Specifies the prefix of the instances to delete.

Related Text Commands

- `addTieHiLo`
- `deleteTieHiLo`
- `getTieHiLoMode`
- `setTieHiLoMode`

Related Topics

For information on the following topic, see "Placing the Design" in the *Innovus User Guide*.

- Adding Logical Tie-Off Cells

Scan Chain

Use the *Place* menu's Scan Chain submenu to reorder or delete scan cells.

Note: From this release, only one window with button Display/Clear and syntax 2 and 5 or 2 to 5 will take effect on the scan chain form.

The *Scan Chain* submenu provides access to the following features:

- Delete
- Reorder

Delete

Use the Delete Scan Groups form to unassign scan cell groups.

Note: Scan groups are sometimes called scan partitions.
→ Choose *Place - Scan Chain - Delete*.

Delete Scan Groups Fields and Options

All Scan Group(s)	Unassigns all scan groups.
Selected Scan Group	Unassigns a particular scan group.

Related Text Commands

- deleteScanChain

Related Topics

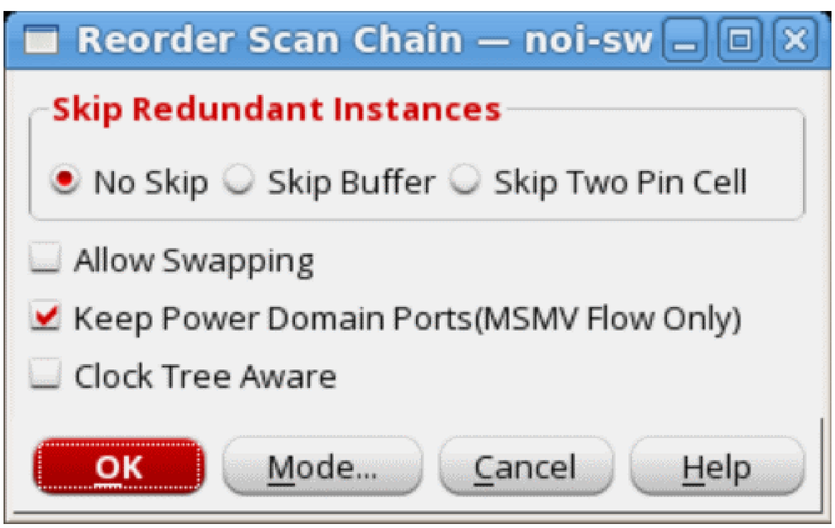
For information on the following topic, see "Placing the Design" in the *Innovus User Guide*.

- Scan Cell Functionality

Reorder

Use the Reorder Scan Chain form to reorder the scan edge order for scan groups. Reordering the groups eases connection constraints on the scan instances without constraining the placement of the scan instances.

Note: Scan groups are sometimes called scan partitions.
→ Choose *Place - Scan Chain - Reorder*.



Reorder Scan Chain Fields and Options

Skip Redundant Instances	Specifies the way that scan reordering handles buffers and inverters in the scan chain. *Default: No Skip* Select one of the following options:
No Skip	Does not remove buffers or inverters after scan chain reordering.
Skip Buffer	Skips the buffers in the scan chain. If a buffer or inverter is not connected elsewhere in the design, the software removes the buffer.
Skip Two Pin Cell	Skips buffers and inverters in the scan chain. If a buffer or inverter is not connected elsewhere in the design, the software removes the buffer or inverter.
Allow Swapping	Allows the software to swap scan elements between scan chains within the same partition. *Default:* Swapping is not allowed.
Clock Tree Aware	Specifies whether scan reordering is clock tree aware. • When selected, scan reordering is clock tree aware, and is clock tree driven. • When not selected, scan reordering is not clock tree aware, and is wirelength driven. *Default:* Not selected (The software is not clock tree aware.)

Related Text Commands

- `scanReorder`

Related Topics

For information on the following topic, see "Placing the Design" in the *Innovus User Guide*.

- Reordering Scan Chains

Check Placement

Use the Check Placement form to check `FIXED` and `PLACED` cells and blocks for violations, add violation markers to the design display area, and generate a violation report. Use the Violation Browser to see the violation markers.

Rules as to what constitutes a placement violation are different for `FIXED` and `PLACED` cells. For example, `FIXED` cells in obstruction areas are not considered to be violations, but `PLACED` cells are considered to be violations.

Note: The utilization value reported by `checkPlace` and the density value reported by `timeDesign` might differ because `checkPlace` considers padding when calculating utilization but `timeDesign` does not consider padding when calculating density.

You can delete padding by running the `deleteAllCellPad` command before running `checkPlace`.

The command checks for the following violations:

- Region and fence violations (Instances placed outside their region or fence)
- Out of core area violations (Instances placed partly or wholly outside the core area)
- Not placed on placement grid (Instances not on the placement grid, or blocks not on the manufacturing grid)
- Row orientation violations (Instances whose orientation is illegal for their row; may short power to ground)
- Tech site violations (Instances placed on tech sites not matching their cells and instances that do not have rows for their tech sites)
- Overlapping with other instance (Placed instances that overlap with other instances)
- Pin access violations (Instances with at least one signal pin that does not have routing access due to pre-wires)
- Orientation violations (Instances whose orientation is not legal based on its cell symmetry rules)
- Routing/placement blockage violations in the core area (Instances placed in an obstruction created by pre-wires or routing blockage)
  The command does not check fixed blocks.
- Placement blockage violations in the core area (for example, placed instances in an obstruction created by prerouted wires or a routing blockage, placed instances that overlap a placement blockage area).

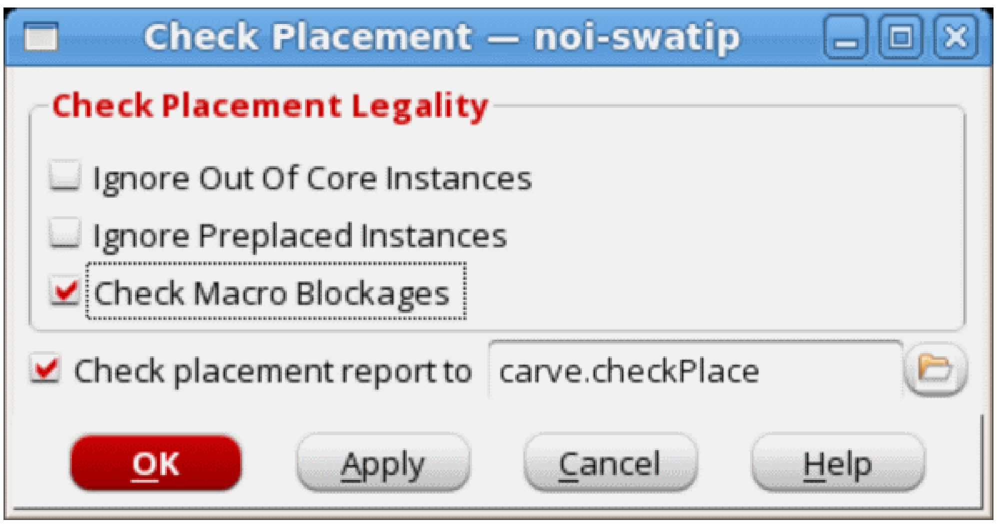
Note: The command does not check fixed instances overlapping placement or routing blockages by default.

- Site orientation violations (Instances whose orientation does not match the tech site orientation)
- Not of fence violations (Instances placed inside a fence to which it does not belong)
- Instance padding violations if `setPlaceMode` `-place_detail_honor_inst_pad` is set to `true`.

In addition to checking for violations, the command reports the following:

- Number of placed instances in the design
- Number of unplaced macros in the design
- Placement density, in terms of used sites over available sites

→ Choose *Place - Check Placement*.



Check Placement Fields and Options

Ignore Out of Core Instances	Disables the reporting on instances that are in the area in between the core design boundary area and chip design (head box) area. The instances preplaced in this in between area are assumed to be correct. This also includes I/O pad instances that are outside the core design area. *Default:* Off
Ignore Preplaced Instances	Disables reporting on instances that are preplaced within the design (head box) area. This includes placement of instances from loading DEF or TDF placement files. *Default:* Off
Check Macro Blockage	Checks for overlap between hard macro and macro-only blockage and reports macro blockage violation. By default, macro-only blockage is ignored for both hard macro and standard cell. With this setting, it is treated as a placement obstruction for macros.
Check placement report to	Specifies the filename for the check placement report.

Related Text Commands

- `checkPlace`

Display

Use the *Place* menu's *Display* forms and commands to display spare cells and scan cells and remove them from the design display area.

The *Display* submenu provides access to the following features:

- Display Spare Cell
- Clear Spare Cell Display
- Display Scan Chain
- Get Scan Chain
- Display Density Map

- Display Pin Density Map
- Display Edge Constraints
- Display Cell Padding

Display Spare Cell

Use the Display Spare Cell command to display the results of placing the spare instances.
→ Choose *Place* - *Display* - *Display Spare Cell*.

There is no GUI form for this command.

Related Text Commands

- `displaySpareCell`

Clear Spare Cell Display

Use the Clear Spare Cell Display command to remove the displayed spare instances.
→ Choose *Place* - *Display* - *Clear Spare Cell Display*.

There is no GUI form for this command.

Related Text Commands

- `clearSpareCellDisplay`

Display Scan Chain

Use the Display Scan Connections form to display scan cell connections.

1. Set the design display to Physical view.
2. Choose *Place* - *Display* - *Display Scan Chain*.

Display Scan Connections Fields and Options

All Scan Group(s)	Displays scan connections of all scan groups. **Note:** Scan groups are sometimes called scan partitions.
Selected Scan Group	Displays scan connections of the specified scan group.
Select	Displays the *Get ScanChain* form. For more information, see Get Scan Chain .

Related Text Commands

- `displayScanChain`

Get Scan Chain

Use the *Get ScanChain* form to view the available scan chains and select one or multiple chain connections to display in GUI.

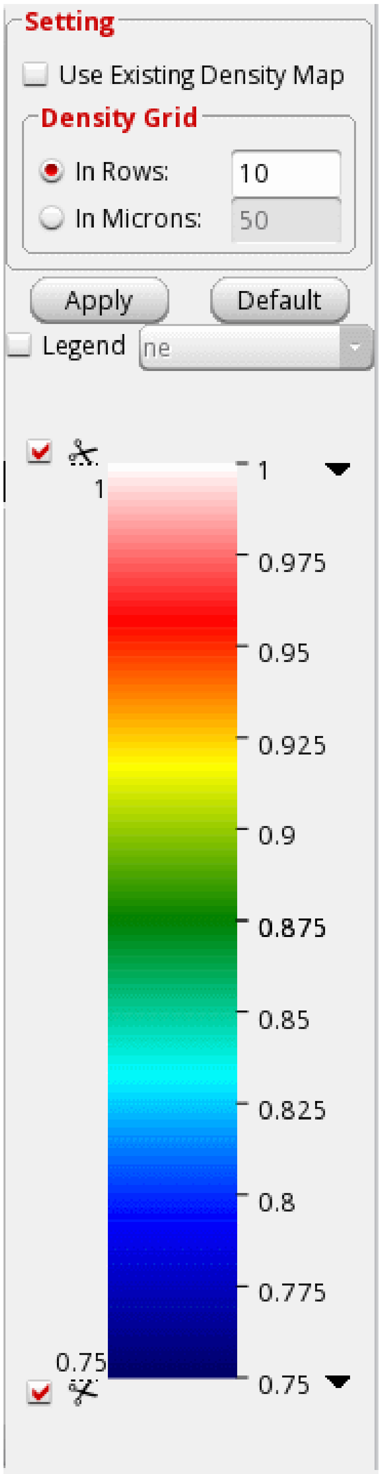
- In the *Display Scan Connections* form, click the *Select* button to display the *Get ScanChain* form.

Get ScanChain Fields and Options

List of ScanChains	Lists all available scan chains.
Selected ScanChains	Lists the scan chains you selected from the available scan chain list. The selected scan chains are displayed in GUI.
Add	Adds the scan chain(s) from *List of ScanChains* to *Specified ScanChains*.
Delete	Deletes the selected scan chain from *Specified ScanChains*.

Display Density Map

Use the Display Density Map form to set options for displaying placement density.
→ Choose *Place - Display - Display Density Map*.
Note: When you click OK, the display of the density is automatically set to on.


Setting
Use Existing Density Map
Density Grid
In Rows:
10
In Microns:
50
Apply
Default
Legend
ne
1
1
0.975
0.95
0.925
0.9
0.875
0.85
0.825
0.8
0.775
0.75
0.75

Display Density Map Fields and Options

Use Existing Density Map	Redraws the screen when you click *Apply*, without recalculating the density. Select this option if you change the threshold or the step size, but haven't made any changes to placement. *Default:* Off
Density Grid	Specifies the basis for the map grid. Each bin in the map is a square. *Default: In Rows*
In Rows	Specifies that the dimensions of the bins are based on the height of a standard cell row. For example, if you specify 12, the dimensions of each bin represent 12 times the standard row height. If you specify a value less than `1`, the software uses `1`. *Default:* 10
In Microns	Specifies that the dimensions of the bins are based on microns. For example, if you specify `45`, the dimensions of each bin represent 45 microns. *Default:* 50
Legend	Displays legends in the density map on the layout. You can change the location of legend by using the drop-down menu next to *Legend*. Here, *ne* means north east, nw means north west and so on. *Default*: ne

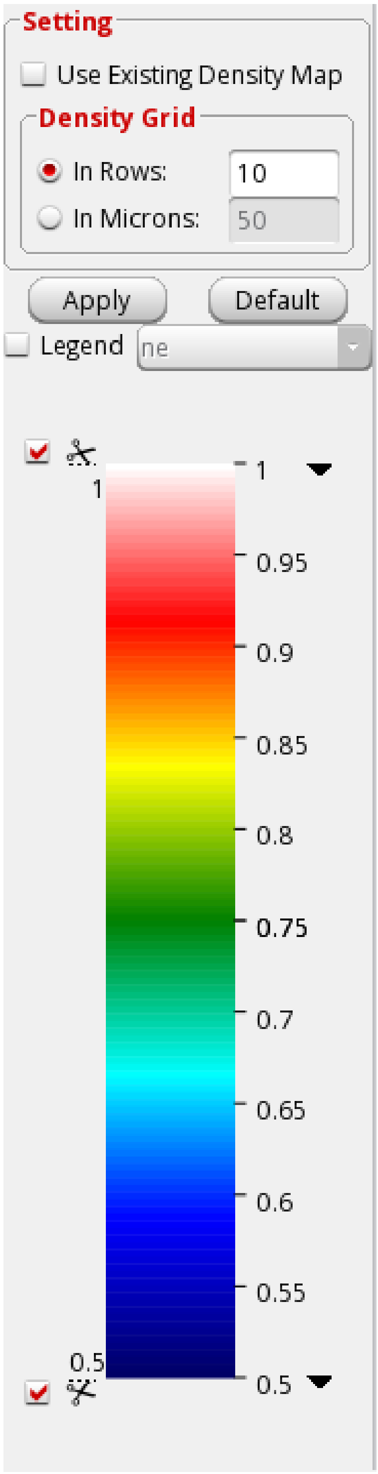
Related Text Commands

- `getDensityMapMode`
- `reportDensityMap`
- `setDensityMapMode`

Display Pin Density Map

Use the Display Density Pin Map form to set options for displaying placement pin density.

→ Choose *Place - Display - Display Pin Density Map*.


Setting
Use Existing Density Map
Density Grid
In Rows:
10
In Microns:
50
Apply
Default
Legend
ne
1
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.5

Display Pin Density Map Fields and Options

Use Existing Density Map	Redraws the screen when you click *Apply*, without recalculating the density. Select this option if you change the threshold or the step size, but haven't made any changes to placement. *Default:* Off
Density Grid	Specifies the basis for the map grid. Each bin in the map is a square. *Default: In Rows*
In Rows	Specifies that the dimensions of the bins are based on the height of a standard cell row. For example, if you specify 12, the dimensions of each bin represent 12 times the standard row height. If you specify a value less than 1, the software uses 1. *Default:* 10 *Minimum: 1* *Maximum: 100*
In Microns	Specifies that the dimensions of the bins are based on microns. For example, if you specify 45, the dimensions of each bin represent 45 microns. *Default:* 50 *Minimum: 0* *Maximum: 1000*
Legend	Displays legends in the density map on the layout. You can change the location of legend by using the drop-down menu next to *Legend*. Here, *ne* means north east, nw means north west and so on. *Default*: ne

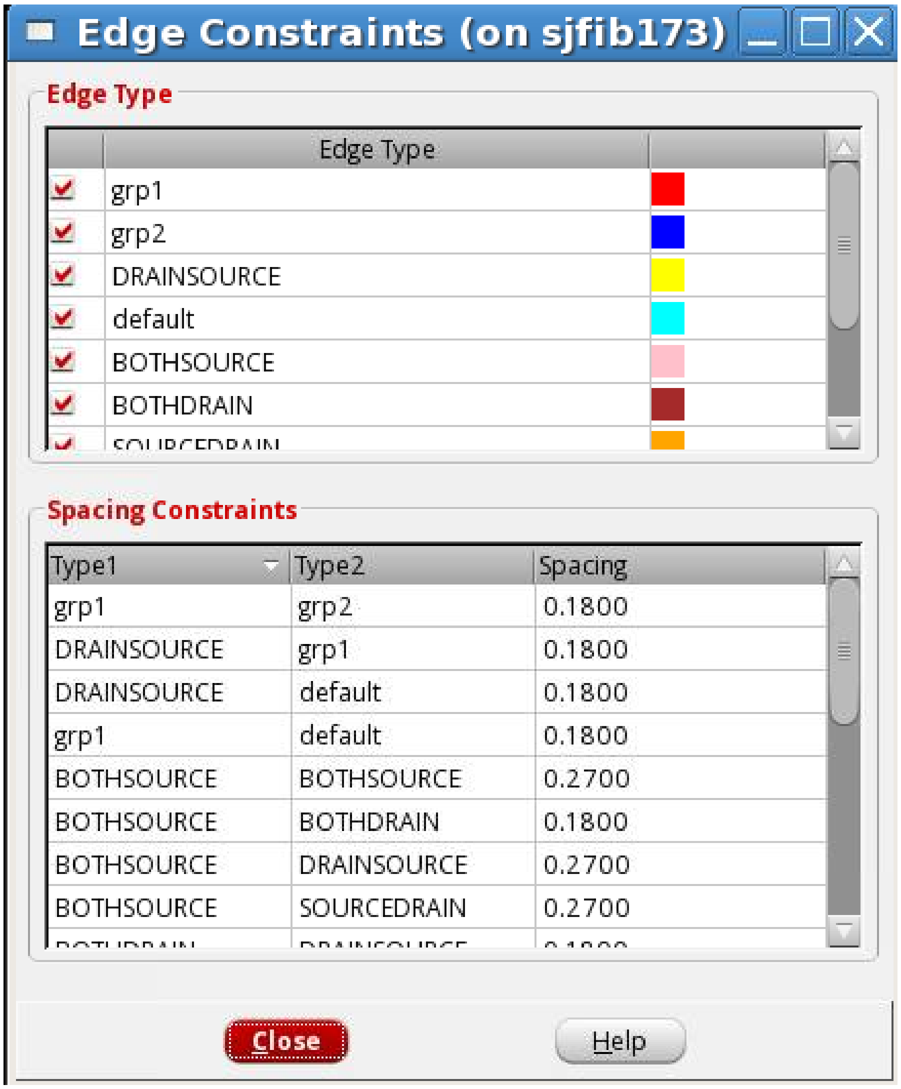
Related Text Commands

- `reportPinDensityMap`
- `getPinDensityMapMode`
- `reportPinDensityMap_`
- `setPinDensityMapMode`

Display Edge Constraints

Use the *Edge Constraints* form to select the groups to be displayed on the GUI and the color of each group.

→ Choose *Place* - *Display* - *Display Edge Constraints*.



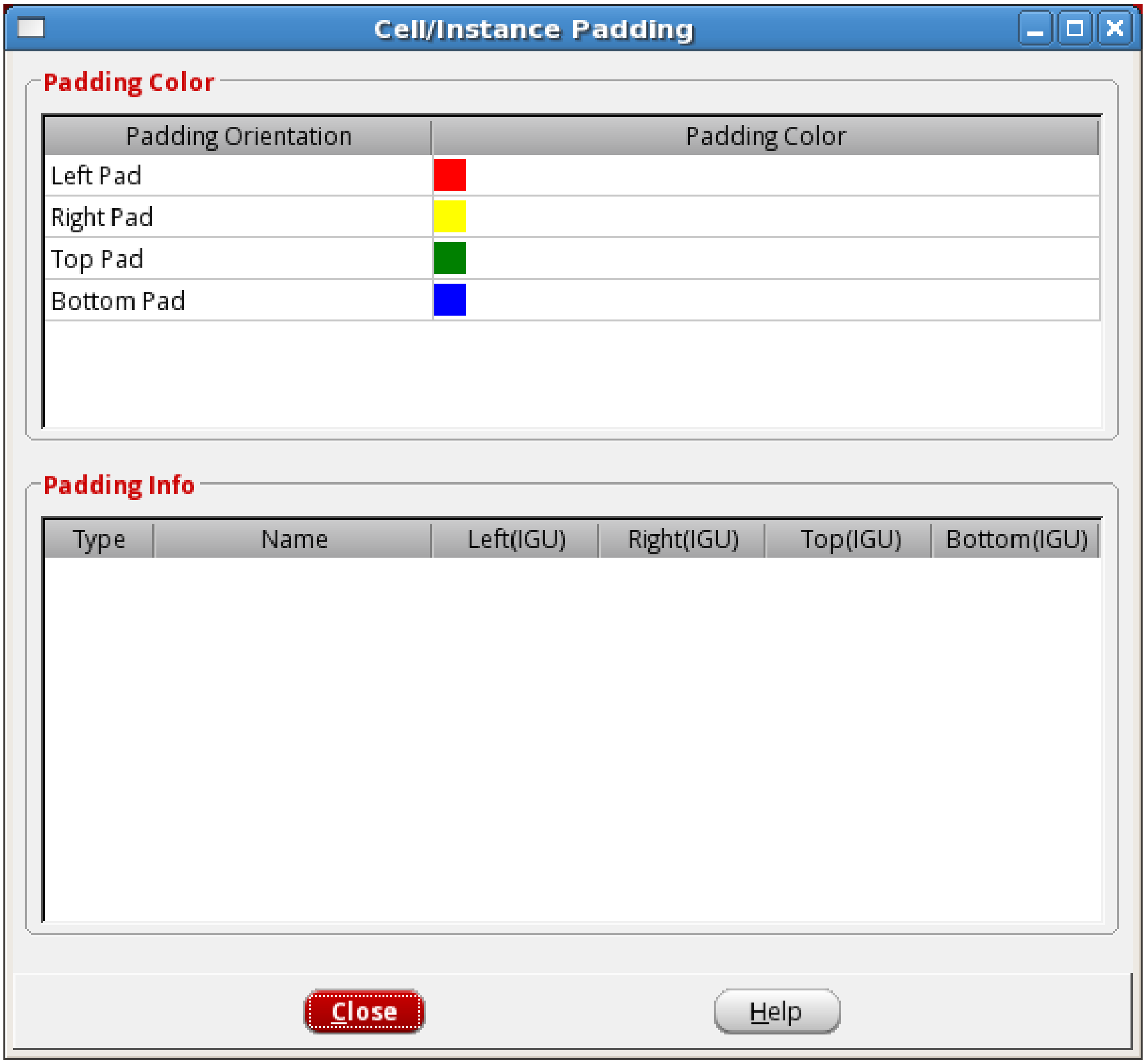
Edge Constraints Fields and Options

Edge Type	Allows you to select the group to be displayed on the GUI. You can use the color button next to a group name to open the Select Color form and change the color for a group.
Spacing Constraint	Displays the spacing constraints for Edge Type, *Type1* and *Type2*.
Close	Closes the *Edge Constraints* form.

Display Cell Padding

Use the *Cell/Instance Padding* form to display cell and instance padding in the GUI and select the color as per the pad orientation.

→ Choose *Place* - *Display* - *Display Cell Padding*.



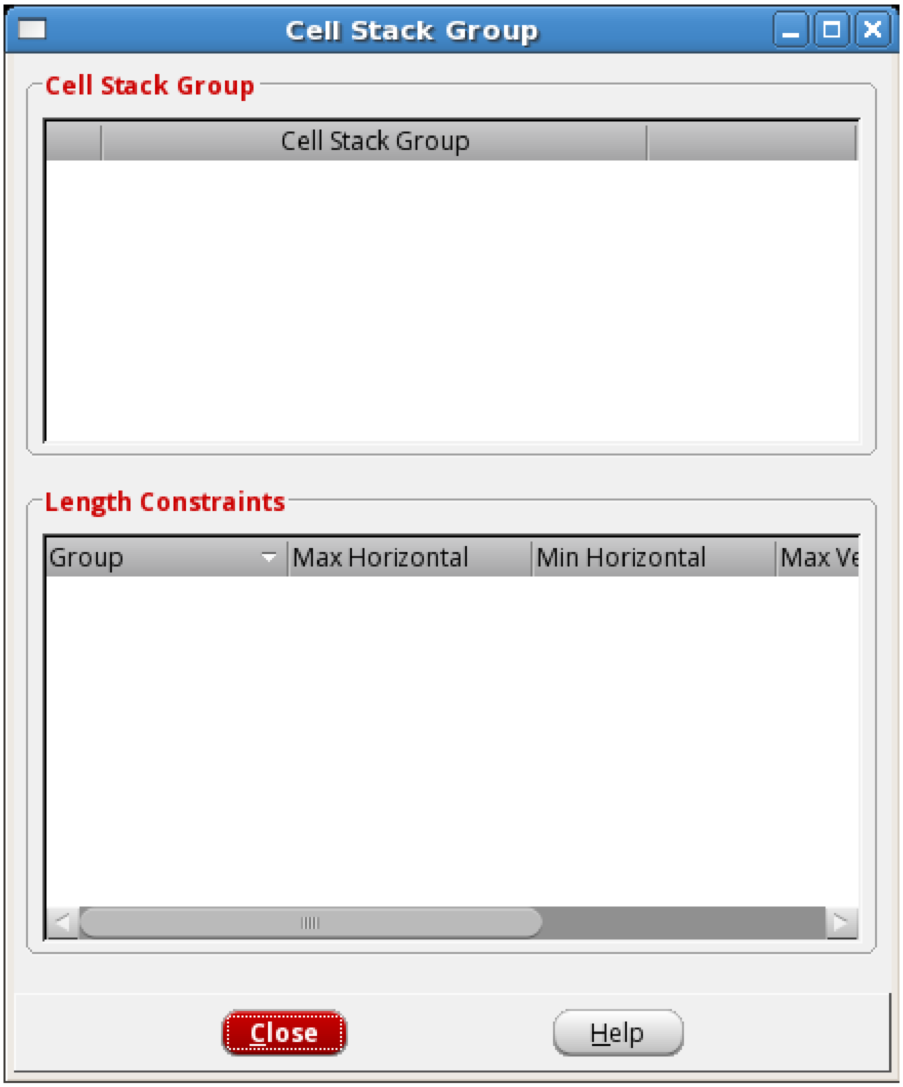
Cell Padding Fields and Options

Padding Color	Allows you to select the color of the padding orientation to be displayed on the GUI. You can use the Padding Color button next to a padding orientation to open the Select Color form and change the color.
Padding Info	Displays the padding information.

Display Cell Stack Group

Use the *Cell Stack Group* form to display cell stack group in the GUI and select the color as per the group.

→ Choose *Place* - *Display* - *Display Cell Stack Group*



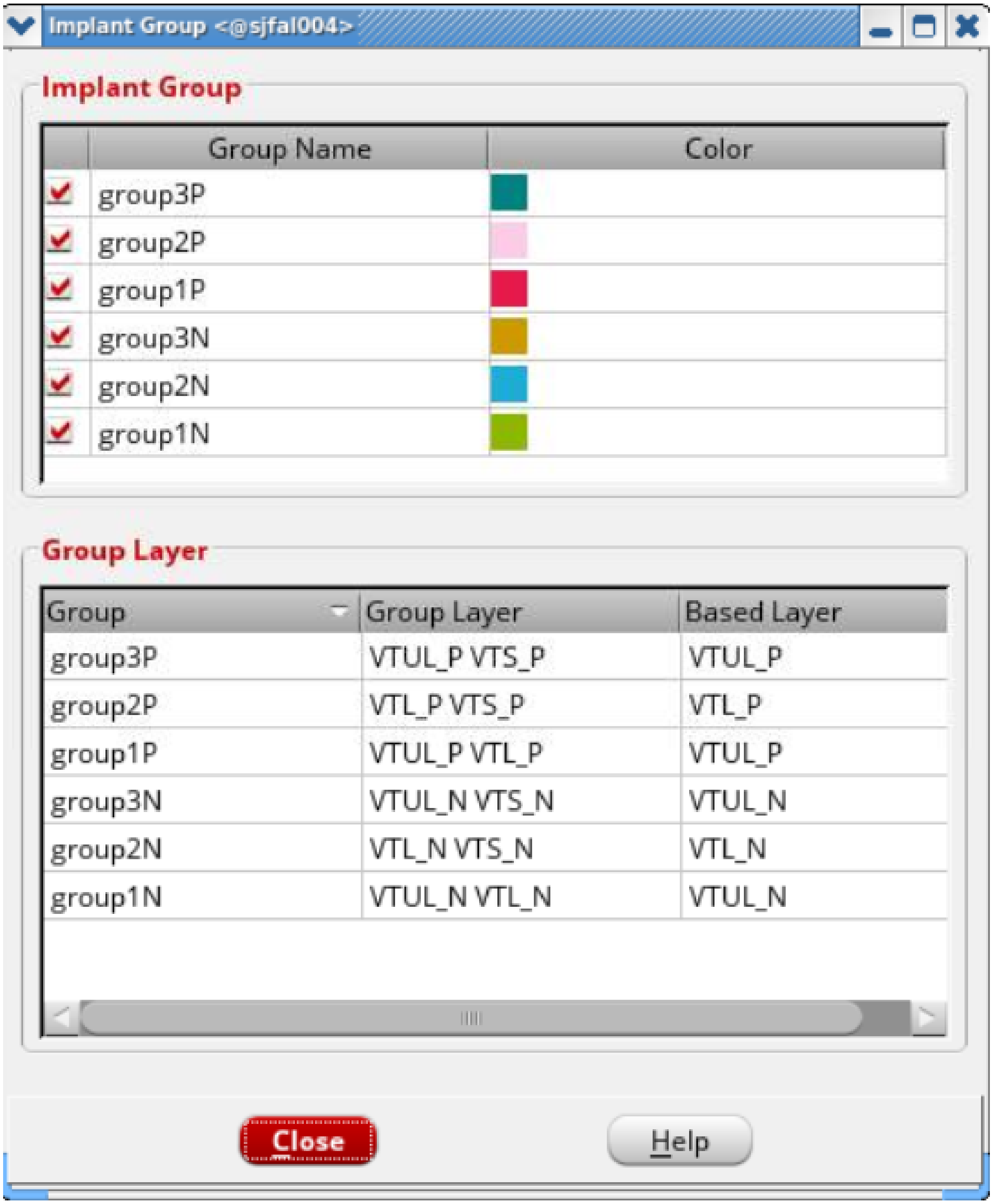
Cell Stack Group Fields and Options

Cell Stack Group	Allows you to select the color of the cell stack group to be displayed on the GUI.
Length Constraints	Displays the Length constraints of cell stack groups.

Display Implant Group

Use the *Cell Stack Group* form to display implant group in the GUI and select the color as per the group. display the cell blockage according to the layer and its VT group

→ Choose *Place* - *Display* - *Display Implant Group*



Display Implant Group Fields and Options

Implant Group	Displays the group name and edit group color.
Group Layer	Displays group, group layer, and based layer.

Query Density

Use the *Place* menu's *Query Density* forms and commands to display cell and pin density in a design.

The *Query Density* submenu provides access to the following features:

- Query Place Density
- Query Pin Density

Query Place Density

Use this option to output the module density.
→ Choose Place - Query Place Density.

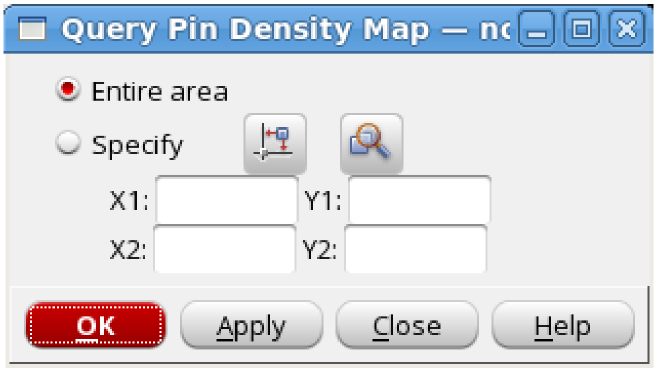
Following is a sample of the output that gets generated on selecting this option:

```
Average module density = 0.424.

Density for the design = 0.424.

 = stdcell_area 694 (2309 um^2) / alloc_area 1638 (5449 um^2).

Pin Density = 0.099.

 = total # of pins 69 / total Instance area 694.
```

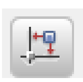
Query Pin Density

Use this option to report the pin density for a specified area in the design.

→ Choose Place - Query Density - Query Pin Density.



Display Query Pin Density Fields and Options

Entire area	Outputs standard cell density in the design.
Specify	Reports the pin density for a specified area in the design.
	User can draw and get the coordinate from GUI directly.
	This View Area button gets the coordinate based on the view area.

Related Text Commands

queryPinDensity

9

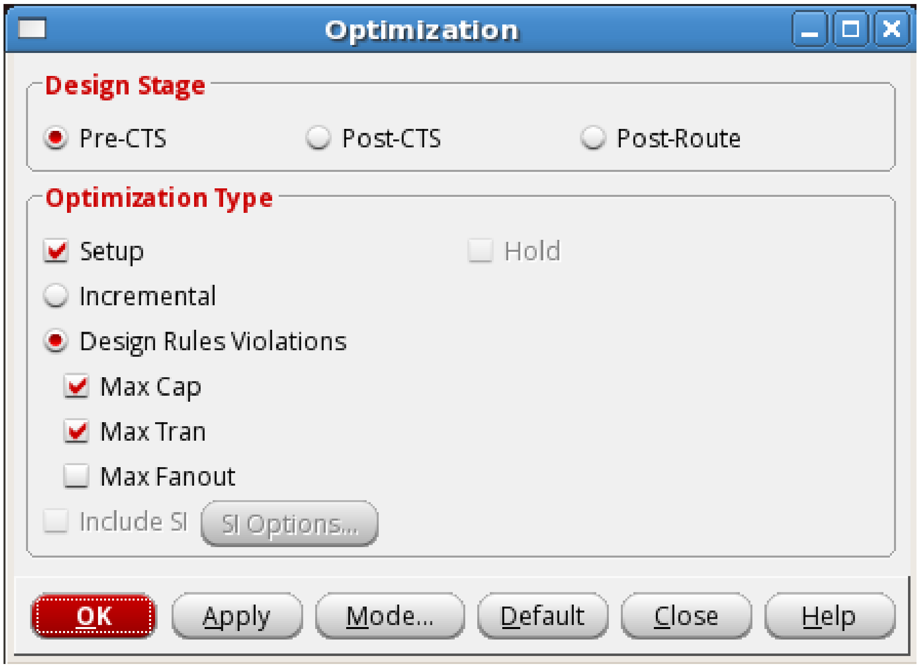
ECO Menu

Optimize Design

Use the *Optimization* form to make the following improvements to your design:

- Reduce path delays
- Improve transition times
- Correct capacitance violations

→*Choose ECO - Optimize Design*.



Optimization Fields and Options

Design Stage Pre-CTS	Performs timing optimization on placed design before the clock tree is built. By default, repairs DRVs and setup violations for all path groups. If the worst negative slack found during the first optimization pass does not occur on a register-to-register path, the software performs an additional optimization for the register-to-register critical paths. *Default:* Selected
Post-CTS	Performs timing optimization after the clock tree is built. By default, repairs DRVs and setup violations for all path groups. If the worst negative slack found during the first optimization pass does not occur on a register-to-register path, the software performs an additional optimization for the register-to-register critical paths. In this mode, if you are running *Useful Skew* and you have already detail routed the clock, the Innovus software performs ECO routing using the NanoRoute® router. *Default:* Deselected

Post-Route	Performs timing optimization on routed designs. By default, repairs DRVs and setup violations for all path groups. If the worst negative slack found during the first optimization pass does not occur on a register-to-register path, the software performs an additional optimization for the register-to-register critical paths. In this mode, the software performs ECO routing using the NanoRoute router. *Default:* Deselected
Optimization Type	
Setup	Corrects setup time violations. *Default:* Selected in all modes.
Hold	Corrects hold time violations. *Default:* Deselected. Available in *Post-CTS* and *Post-Route* modes.
Incremental	Performs incremental optimization on all path groups. *Default:* Deselected
Design Rules Violations	
	Specifies the type of design rule violations to correct. *Default:* Selected. Unavailable if *Incremental* is selected, or if *Pre-CTS* mode and *Low* effort (on the *Mode Setup - Optimization* form) are selected.
Max Cap	Corrects maximum capacitance violations in the design based on the threshold specified in the SDC constraints file or in the timing libraries. *Default:* Selected. Available only if *Design Rule Violations* is selected.
Max Tran	Corrects maximum transition violations in the design based on the threshold specified in the SDC constraints file or in the timing libraries. *Default:* Selected. Available only if *Design Rule Violations* is selected.

Max Fanout	Corrects maximum fanout-load violations. In the library, each cell output pin might have a `maxfanout` constraint defined, and each input pin might have a `fanout_load` defined. The Innovus software checks `maxfanout` against the total `fanout_load` that the output pin drives in the netlist. A violation exists if the total fanout load exceeds the `maxfanout`. You can override these limits by specifying new limits in the SDC file. If `maxfanout` or `fanout_load` are not defined in the library, the Innovus software does not perform maximum fanout repair. *Default:* Deselected. Available only if *Design Rule Violations* is selected.
Include SI	Corrects signal integrity violations for designs routed in signal integrity prevention mode. *Default:* Deselected. This option is available in *Post-Route* mode only.
SI Options	Opens the Fix Crosstalk form, enabling you to select options for repairing noise-on-delay and glitch noise violations. This option is available only in *Post-Route* mode, and only if you select *Include SI*.

Related Text Commands

For information on the following commands, see "Timing Optimization Commands" in the *Innovus Text Command Reference*.

- `optDesign`
- `setAnalysisMode`
- `setOptMode`
- `setSIMode`
- `setUsefulSkewMode`

Related Topics

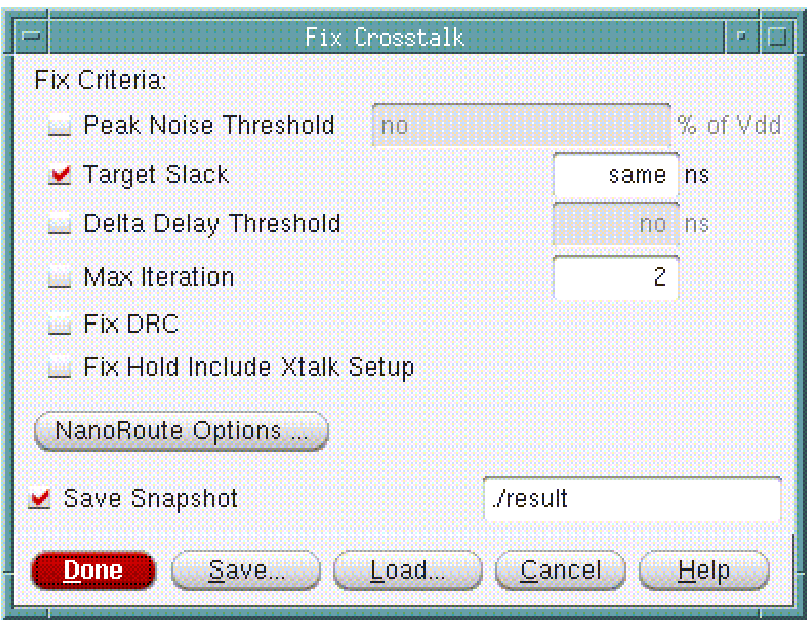
For information on the following topics, see "Optimizing Timing" in the *Innovus User Guide*.

- Performing Pre-CTS Optimization
- Performing Post-CTS Optimization
- Performing Postroute Optimization
- Useful Skew

Fix Crosstalk

→ Choose *ECO - Optimize Design*. Then, select the *Post-Route* option in the *Design Stage* section. Next, select the *Include SI* option under the *Optimization Type* section and click *SI Options*.

Use the Fix Crosstalk form to repair noise-on-delay and glitch noise violations. Innovus can repair noise violations using driver resizing, buffer insertion, downsizing rip-up aggressors, or soft spacing routing.



Fix Crosstalk Fields and Options

Related Text Commands

- setSIMode

For more information, see "Signal Integrity Commands" in the *Innovus Text Command Reference*.

Related Topics

For more information, see the "Analyzing and Repairing Crosstalk" chapter in the *Innovus User Guide*.

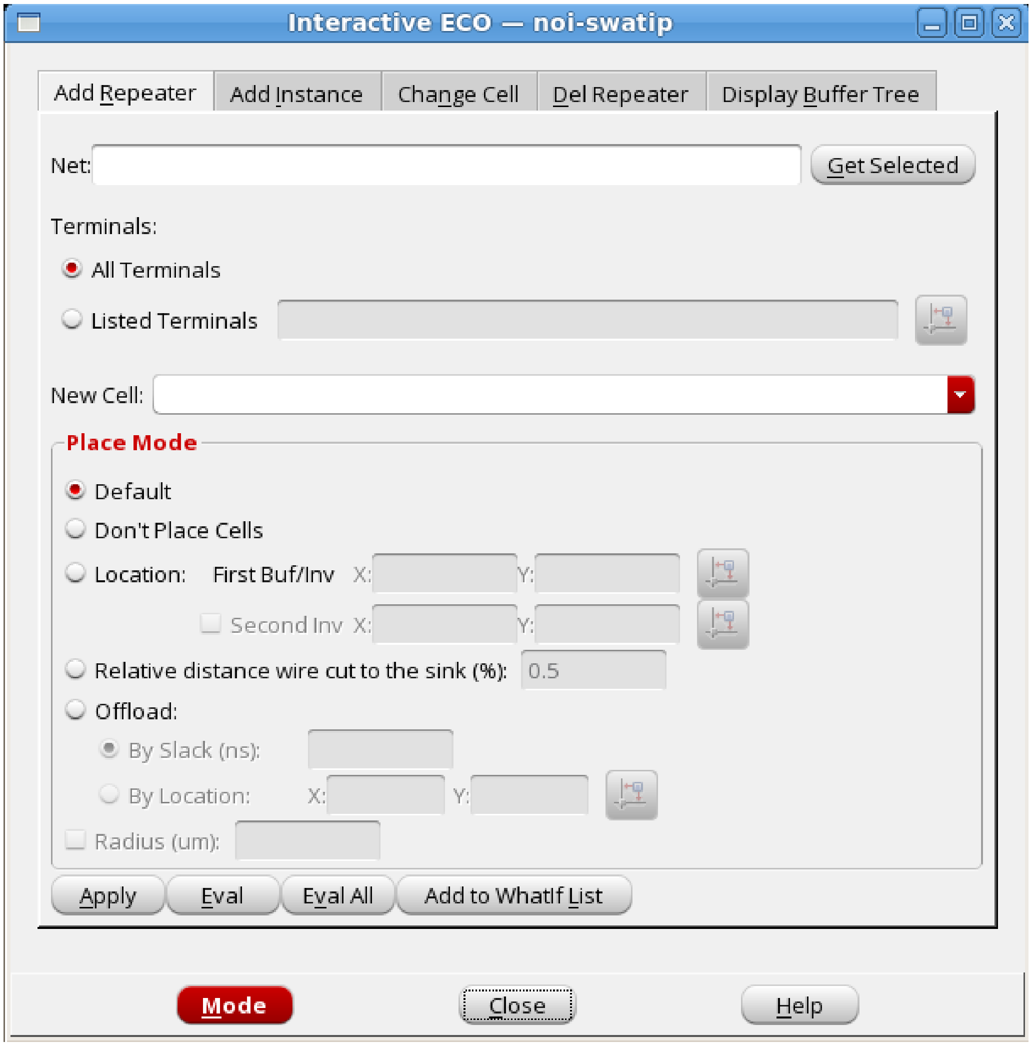
Interactive ECO

The Interactive ECO feature enables you to perform manual incremental updates to the design to repair timing or transition time violations. The *Interactive ECO* form contains the following five pages:

- Interactive ECO - Add Repeater
- Interactive ECO - Add Instance
- Interactive ECO - Change Cell
- Interactive ECO - Delete Repeater
- Interactive ECO - Display Buffer Trees

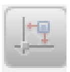
Interactive ECO - Add Repeater

Use the *Add Repeater* page of the Interactive ECO form to add buffers or a pair of inverters.
→ Choose *ECO - Interactive ECO* and click on the *Add Repeater* tab.



Interactive ECO - Add Repeater Fields and Options

Net	Type the net name, or click on a displayed net in the design display window and click *Get Selected*.
Get Selected	Displays the name of a selected net. If you click on the *Get Selected* button on this form without first selecting a net, the software issues an error message.
Terminals	Provides two methods for specifying the buffer connection

All Terminals	Connects the added buffer to drive all the receivers. Use this to reduce the delay and output transition time of a weak driver driving a large capacitive load.
Listed Terminals	Connects the added buffer to drive the listed receivers, and provides full flexibility for building an arbitrary buffer connection.
	The draw terminal button allows you to draw an area covering the terminals to which you want to add the buffer.
New Cell	Enter the cell type name of the buffer cell to add, or click on the arrow to right of the field and select a buffer from the list
Place Mode	The following options specify various aspects for ECO placement.
Default	The software automatically determines a location and places the new cell.
Don't Place Cells	Specifies that the inserted cells should not be placed.
Location	Specifies where the buffer should be inserted. • *First Buf/Inv X Y:* Specifies the X and Y locations for the buffer or first inverter. You can use the automatically assigned location, enter the location, or click on an area in the design display window and click *get coord.* If the cell is a buffer and location is specified, the newly created buffer is placed at the specified location. If the cell is an inverter and only one location is specified, both inverters will be placed at the same location. • *Second Inv X Y: Specifies the X and Y locations for the second inverter.You can use the automatically assigned location, enter the location, or click on an area in the design display window and click get coord.*

Offload	Specifies the manner of buffer insertion for slack or load reduction. • By Slack (ns): Inserts a buffer to offload the paths with less than the specified slack threshold from the driver of a net with multiple cells. This option ignores the `term` option, if it is provided. • By Location: Inserts a buffer at a the specified location on a net to reduce the load on the net driver. The tool determines the buffer direction by tracing backward on the net to find the buffer driving the wire segment at the new buffer location. The driven segment is connected to the input terminal of the new buffer. • *get coord:* Retrieves and displays the X and Y coordinates for a specified location in the design window
Relative Distance wire cut to the sink (%):	
	Specifies the location of the buffer based on its distance from the sink or the driver pin. The value is a number between 0 and 1. A low value (0.1) places the buffer near the sink; a high value (0.9) places the buffer near the driver.
Offload (ns):	Offloads all paths with less than the specified slack threshold (in nanoseconds) from the driver of a net with multiple cells. This option ignores the `term` option, if it is provided.
By Location (x y)	Specifies the x and y coordinates for the location of the buffer or inverter pair to insert. If no location is specified, the tool will automatically determine a location. If the cell is a buffer and location is specified, the newly created buffer is placed at the specified location. If the cell is an inverter pair and only one location is specified, both inverters will be placed at the same location.
Radius (um):	Specifies the radius in which the added instances are free to move. If no legal location can be found in the specified radius, the cells would be placed at the specified location resulting in an overlap with other cells. In that case, you should perform legalization.
Eval	Evaluates the effect on timing if you add *New Cell*. These values are reported but not applied, so you can experiment with different cell types. **Note:** This option is active only if the design is routed.

Eval All	Evaluates the effect on timing for all the cell types available for *New Cell*. The timing report shows the effects of all the cell types, enabling you to select the best cell for your design. **Note:** This option is active only if the design is routed.
Add to WhatIf List	Calculates the timing change introduced. Result is presented in Timing Debug control panel under Path Category.
Apply	Applies your selections.
Mode	Helps you select different modes to control the behavior of ECO commands.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `ecoAddRepeater`
- `attachIOBuffer`

For more information, see "Interactive ECO Commands" in the *Innovus Text Command Reference*.

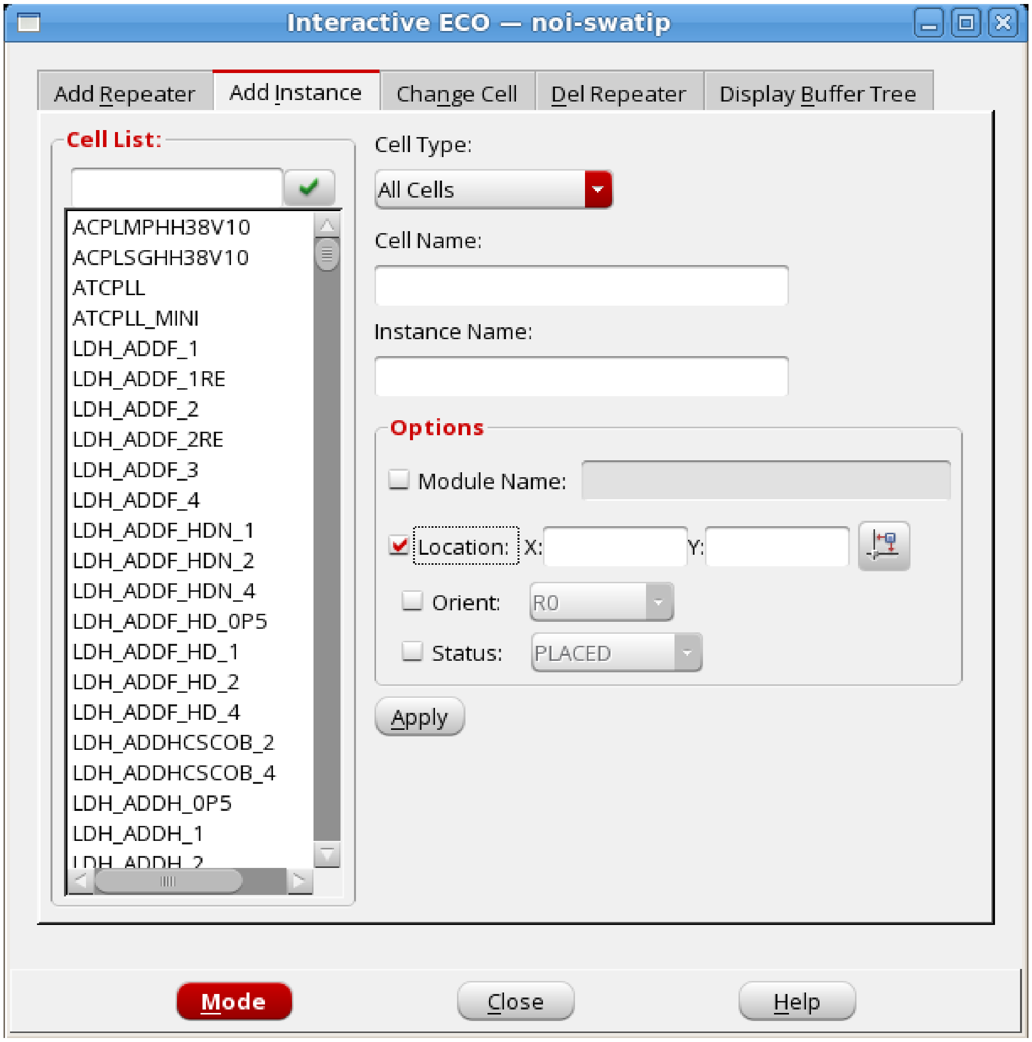
Related Topics

For information on the following topic, see "ECO" in the *Innovus User Guide*.

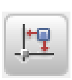
- Adding Buffers

Interactive ECO - Add Instance

Use the *Add Instance* page of the Interactive ECO form to add instances.
→ Choose *ECO - Interactive ECO* and click on the *Add Instance* tab.


Interactive ECO — noi-swatip
Add Repeater
Add Instance
Change Cell
Del Repeater
Display Buffer Tree
Cell List:
ACPLMPHH38V10
ACPLSGHH38V10
ATCPLL
ATCPLL_MINI
LDH_ADDF_1
LDH_ADDF_1RE
LDH_ADDF_2
LDH_ADDF_2RE
LDH_ADDF_3
LDH_ADDF_4
LDH_ADDF_HDN_1
LDH_ADDF_HDN_2
LDH_ADDF_HDN_4
LDH_ADDF_HD_0P5
LDH_ADDF_HD_1
LDH_ADDF_HD_2
LDH_ADDF_HD_4
LDH_ADDHCSCOB_2
LDH_ADDHCSCOB_4
LDH_ADDH_0P5
LDH_ADDH_1
Cell Type:
All Cells
Cell Name:
Instance Name:
Options
Module Name:
Location: X: Y:
Orient: R0
Status: PLACED
Apply
Mode
Close
Help

Interactive ECO - Add Instance Fields and Options

Cell List	Lists all the cells. To search for a cell, enter the cell name in the text box and click the tick button.
Cell Type	Allows you to select the following options: • All Cells • Standard Cell • Physical Cell • IO Cell • TIE Cell • Macro Cell
Cell Name	Enter a cell name.
Instance Name	Allows you to enter an instance name.
Options	
Module Name	Enter a module name.
Location	Specify X and Y coordinates for the instance.
	The get coordinate button retrieves and displays the X and Y coordinates for a specified location in the design window.
Orient	Specify the orientation of the instance.
Status	Specifies that the status of the instance - placed, fixed, or covered.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `addInst`

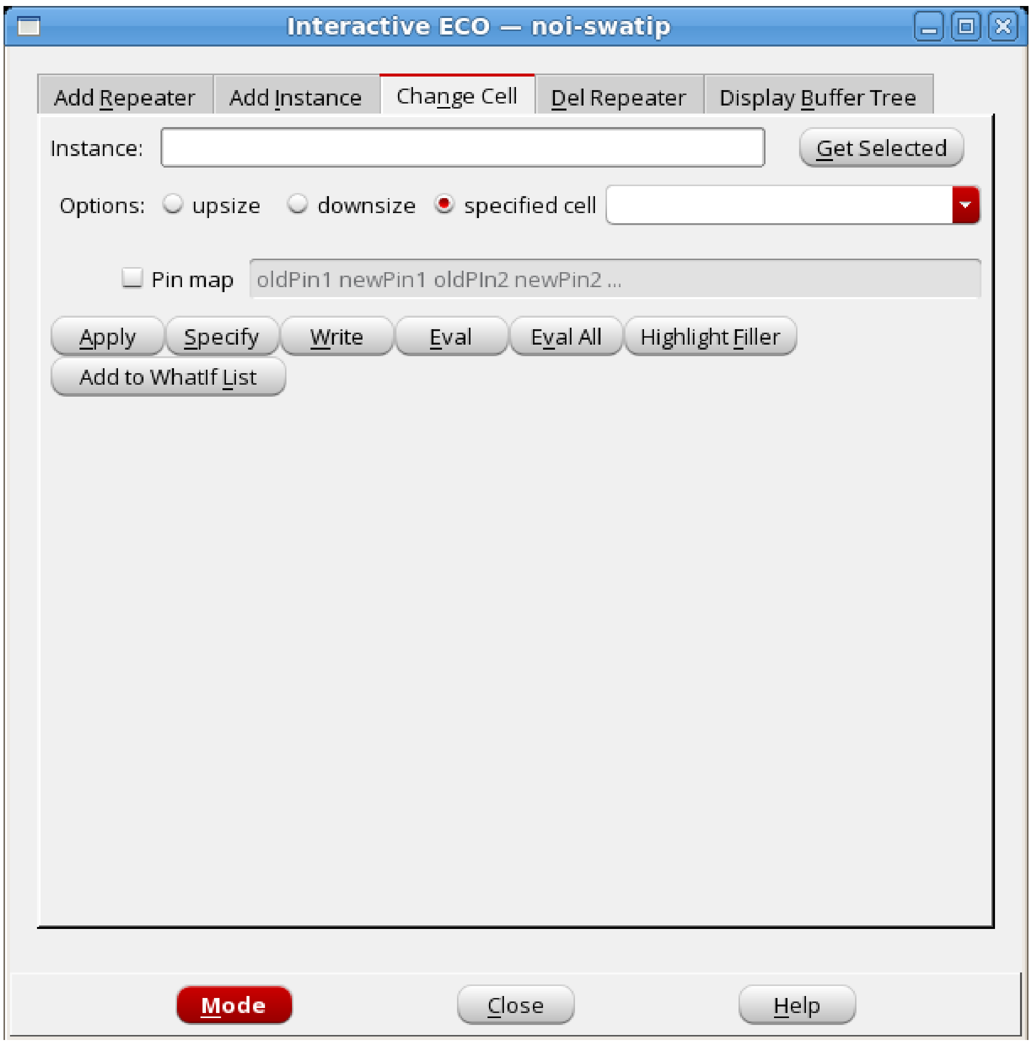
For more information, see "Interactive ECO Commands" in the *Innovus Text Command Reference*.

Interactive ECO - Change Cell

Use the *Change Cell* page of the Interactive ECO form to upsize or downsize an instance. This drives a large load to improve the driver delay and the transition time at the receivers. This can also downsize an instance on the noncritical path to reduce the loading of its driver on the critical path.

Note: You can also open the *Change Cell* page from the right-click menu in Main window.

→ Choose *ECO - Interactive ECO* and click on the *Change Cell* tab.



Interactive ECO - Change Cell Fields and Options

Instance	Enter the hierarchical instance name to be changed.
Get Selected	Displays the name of a selected instance. If you click on the *Get Selected* button on this form without first selecting an instance, the software issues an error message.
Options:	Select from the following options
upsize	Upsizing an instance that drives a large load can improve the driver delay and the transition time at the receivers.
downsize	Downsizing an instance on the noncritical path can reduce the loading of its driver on the critical path.
specified cell	Enter the name of the placement cell, or use the pull-down menu to select a cell.
Pin map	Specifies the pin mapping for the new cell based on the old cell.
Eval	Evaluates the effect on timing if you upsize or downsize a cell, or change to a different cell. These values are reported but not applied. **Note:** The option is active only if the design is placed.
Eval All	Evaluates the effect on timing for all the options available. **Note:** The option is active only if the design is placed.
Highlight Filler	Highlights the filler cell.
Add to WhatIf List	Calculates the timing change introduced. Result is presented in Timing Debug control panel under Path Category.
Apply	Applies your selections.
Specify	Specifies the instance.
Write	Saves the ECO file.
Mode	Helps you select different modes to control the behavior of ECO commands.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `ecoChangeCell`

For more information, see "Interactive ECO Commands" in the *Innovus Text Command Reference*.

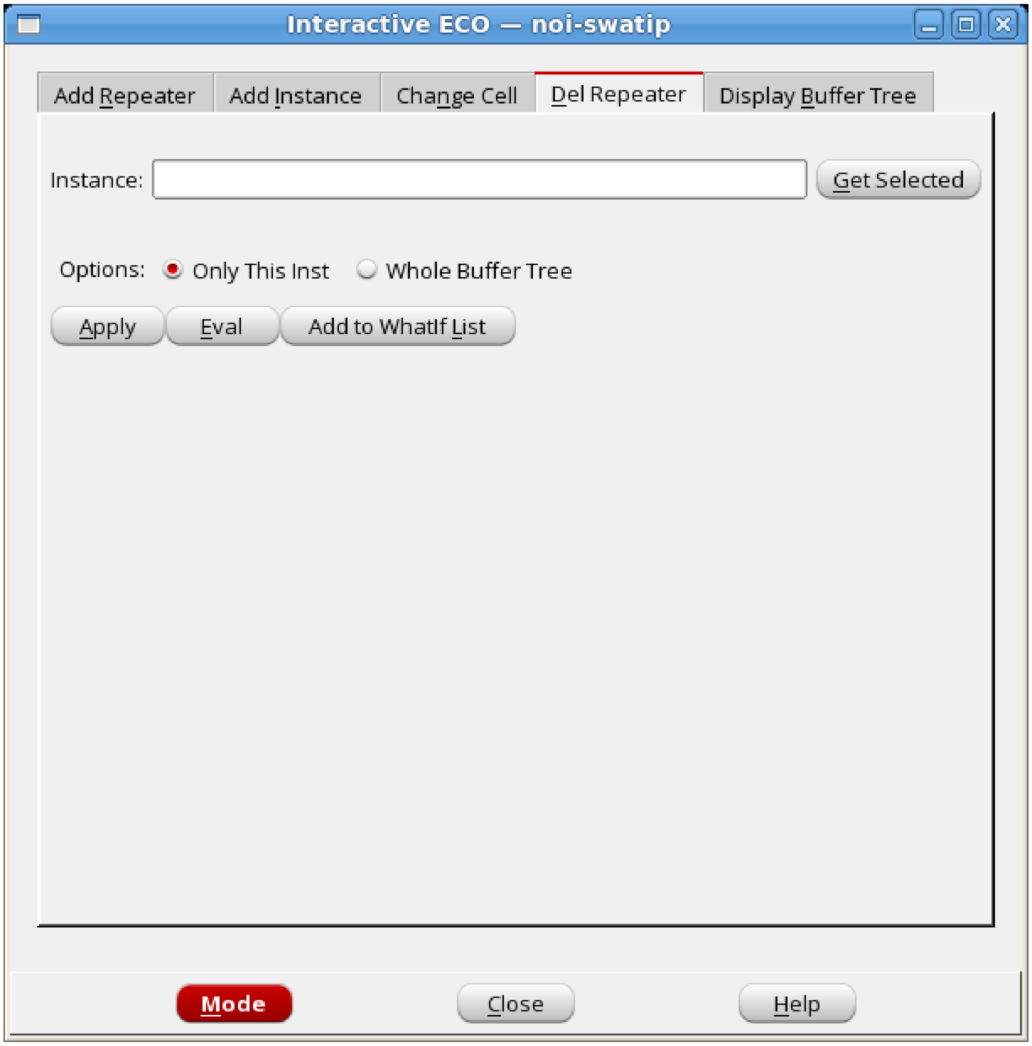
Related Topics

For information on the following topic, see "ECO" in the *Innovus User Guide*.

- Changing the Cell

Interactive ECO - Delete Repeater

Use the *Del Repeater* page of the Interactive ECO form to delete redundant buffers that cause extra delay. Buffers are typically over-added by synthesis tools based on wireload models.
→ Choose *ECO - Interactive ECO* and click on the *Del Repeater* tab.


Interactive ECO — noi-swatip
Add Repeater
Add Instance
Change Cell
Del Repeater
Display Buffer Tree
Instance:
Get Selected
Options:
Only This Inst
Whole Buffer Tree
Apply
Eval
Add to WhatIf List
Mode
Close
Help

Interactive ECO - Del Repeater Fields and Options

Instance	Enter the name of the buffer instance to be removed.
Get Selected	Displays the name of a selected instance. If you click on the *Get Selected* button on this form without first selecting an instance, the software issues an error message.
Only This Inst	(Default) Deletes only the selected instance.
Whole Buffer Tree	Automatically traverses the buffer tree associated with the instance, and removes the buffers in the same buffer tree.
Eval	Evaluates the effect on timing if you delete the specified instances or the buffer tree. These values are reported but not applied until you click *Apply*. **Note:** This option is active only if the design is routed.
Add to WhatIf List	Calculates the timing change introduced. Result is presented in Timing Debug control panel under Path Category.
Apply	Applies your selections.
Mode	Helps you select different modes to control the behavior of ECO commands.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `ecoDeleteRepeater`

For more information, see "Interactive ECO Commands" in the *Innovus Text Command Reference*.

Related Topics

For information on the following topic, see "ECO" in the *Innovus User Guide*.

- Deleting Buffers

Interactive ECO - Display Buffer Trees

Use the *Display Buffer Tree* page from the Interactive ECO form to inspect the routing topology of the buffer tree. If the buffer tree requires correction, it can be rebuilt or modified through the other three pages in the Interactive ECO form.

→ Choose *ECO - Interactive ECO* and click on the *Display Buffer Trees* tab.

Interactive ECO - Display Buffer Tree Fields and Options

Net	Enter the name of the net to be selected.
Get Selected	Displays the name of a selected net. If you click on the *Get Selected* button on this form without first selecting a net, the software issues an error message.
Apply	Applies your selections.
Mode	Helps you select different modes to control the behavior of ECO commands.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `displayBufTree`

For more information, see "Interactive ECO Commands" in the *Innovus Text Command Reference*.

Related Topics

For information on the following topic, see "ECO" in the *Innovus User Guide*.

- Displaying Buffer Trees

10

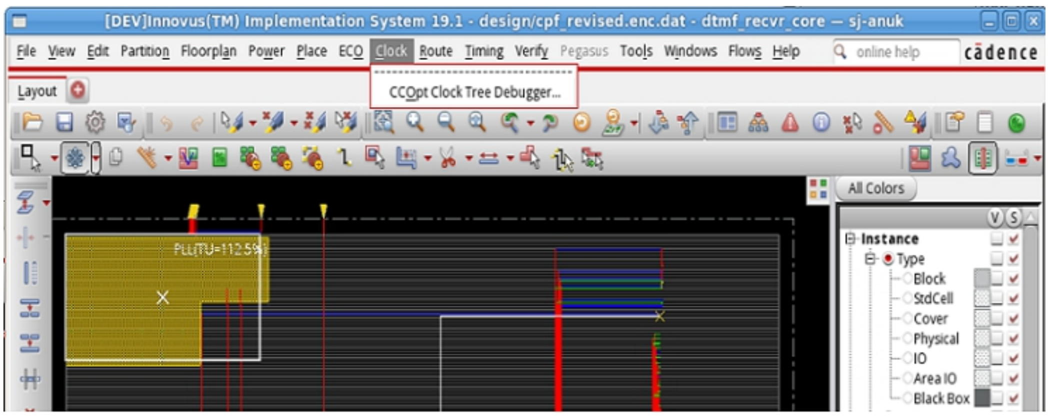
Clock Menu

- Context Menu of the Clock Path Analyzer

CCOpt Clock Tree Debugger

The *CCOpt Clock Tree Debugger* provides clock tree debugging facilities that will help you understand the quality of the CCOpt results better.

→Choose *Clock – CCOpt Clock Tree Debugger*



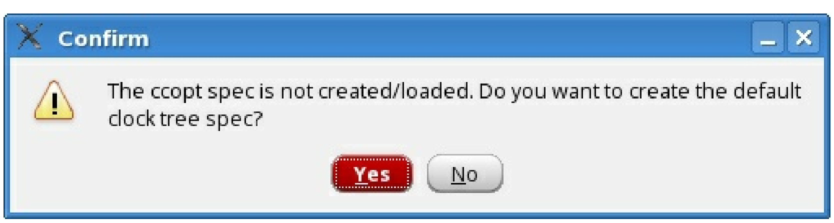
The tool provides the following three basic views for clock tree visualization:

1. **Clock Tree Debugger**: Displays a top-down tree view of the CCOpt clock trees
2. **Clock Path Browser**: Displays the clock path data in a table and provides the option for bringing up a clock path analyzer either from its context menu or by double-clicking on a row in the table
3. **Clock Path Analyzer**: Provides a view to examine a single clock path

The three views are detailed in subsequent sections.

Note: The *CCOpt Clock Tree Debugger* opens only after the CCOpt clock tree specification file has been created using the `create_ccopt_clock_tree_spec` command.

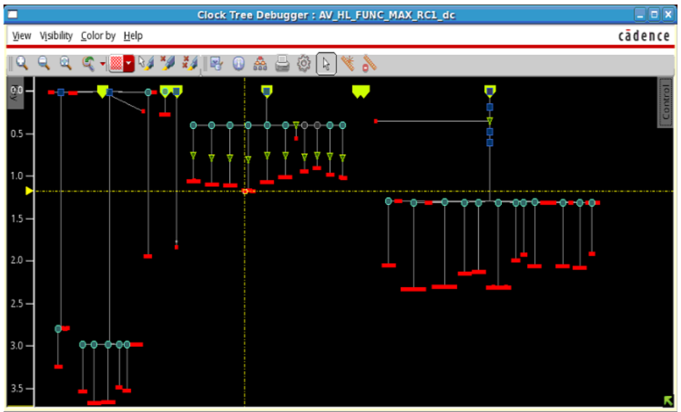
However, if you click on the *CCOpt Clock tree Debugger* menu before creating the clock tree specification file, the *Confirm* pop-up window opens to give a warning message that the CCOpt clock tree specification is not created or loaded. The pop-up gives you an option to create a default clock tree specification file.



The *Clock Tree Debugger* tool displays a top-down tree view of the CCOpt clock trees with the vertical axis representing delays. It has the following features:

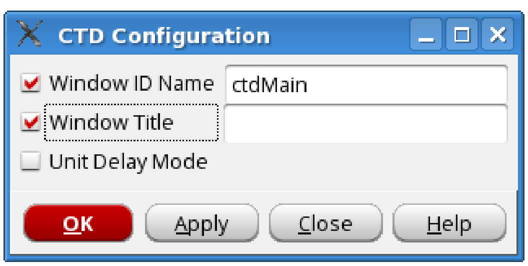
- The tool display shows a schematic-like representation of the CCOpt clock trees. You can control the level of details and the elements that you want to view.

- The results shown in the tool are based on the CCOpt clock tree specification file.
- The units on the vertical scale of the display represent time, so that distance between two elements indicates delays that you can measure.
- A comprehensive search mechanism lets you find instances, paths, and reconvergent clocks easily.
- The tool displays several clocks at the same time.
- The tool can display reconvergent and crossover clocks.



Clock Tree Debugger - CTD Configuration

The CTD Configuration form is used to specify the CTD window you want to open and also enable the unit delay mode. When you click *CCOpt Clock Tree Debugger*, the CTD Configuration form opens.



Options	Descriptions
Window ID Name	Opens a CTD window with a user-specified window ID. The default window ID is `ctdMain`.
Window Title	Specifies the title to be given to the specified window. This option is used either if a unique ID has not been specified for a window or if you want to change the existing window ID.
Unit Delay Mode	Opens the CTD in unit delay mode. For more information about this mode, see the Unit delay option description in the Clock Tree Debugger - Visibility Menu section.

Commands to Invoke, Name, and Close CTD Windows

In addition to opening the CCOpt CTD from the *Clock* menu, you can use the following commands to invoke, name, and close CTD windows.

When you open multiple CTD windows, they all have the same IDs. This can be confusing if you are either running multiple software sessions or switching between multiple CTD windows. These commands are useful in identifying the different windows and opening and closing specific windows.

- `ctd_win`: Opens a CTD window with the user-defined window ID and title. Use the `-unit_delay` parameter of this command to open the CTD in unit delay mode.
- `close_ctd_win`: Closes open CTD windows
- `get_ctd_win_id`: Retrieves the IDs of the CTD windows

Note: If you run any of the following commands, the CCOpt CTD will close.

- `delete_ccopt_clock_tree_spec`
- `delete_ccopt_clock_trees`
- `delete_ccopt_clock_tree_source_group`
- `delete_ccopt_skew_groups`
- `reset_ccopt_config`

Clock Tree Debugger - Main Window Features

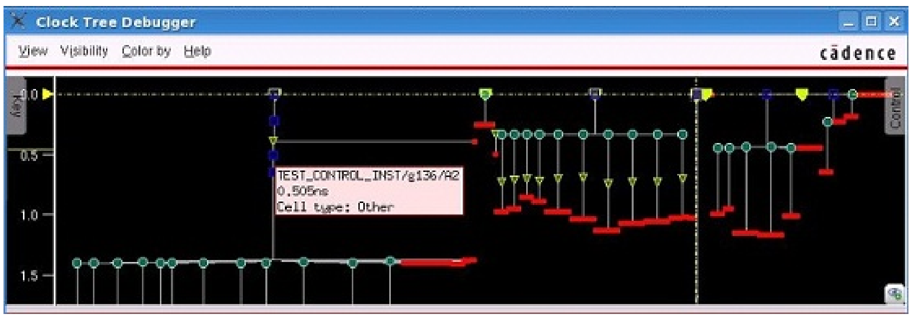
The following options are available in the main window of the *Clock Tree Debugger*:

Options	Descriptions
Ruler	Displays time units (in nanoseconds) that measure the delay between elements.
Browser	A text-based browser that shows information about the different analysis views.
Display area	Displays the clock tree views.
World viewer	
	It is a rectangular area at the right-bottom corner of the *Clock Tree Debugger* canvas that shows you a satellite view, or the world view, of the clock trees. The canvas of the world viewer is demarcated by a white bounding box. You can right-click on any region in the world viewer to navigate to that region with the current zoom level. Click the button again to hide the world viewer. The button is highlighted using a red textbox, as shown in the image below. You can increase or decrease the size of the world viewer from the Set Preference form. Click the *Preference* submenu in the *View* menu to open this form. Click *Small*, *Middle*, or *Large* to change the size of the world viewer window. For details, see "Set Preferences for CTD GUI Configuration" section.
The Context Pop-up Attribute Viewer	

When you position the pointer over an object for a particular time, an attribute pop-up window will appear. The context pop-up attribute viewer displays the basic properties of an object in a pop-up window right next to the location of the object.

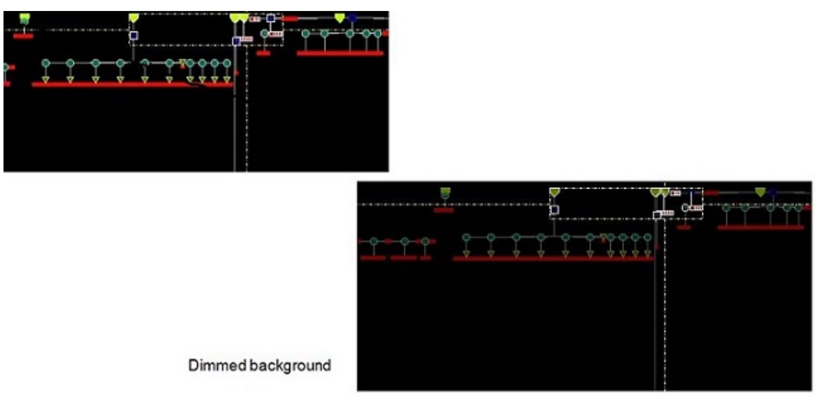
It shows the following information about the object, if available:

- Name
- Insertion delay
- Skew groups
- Clock trees
- If the visualization is being colored by some attribute (for example, skew), then the value of that attribute will be shown



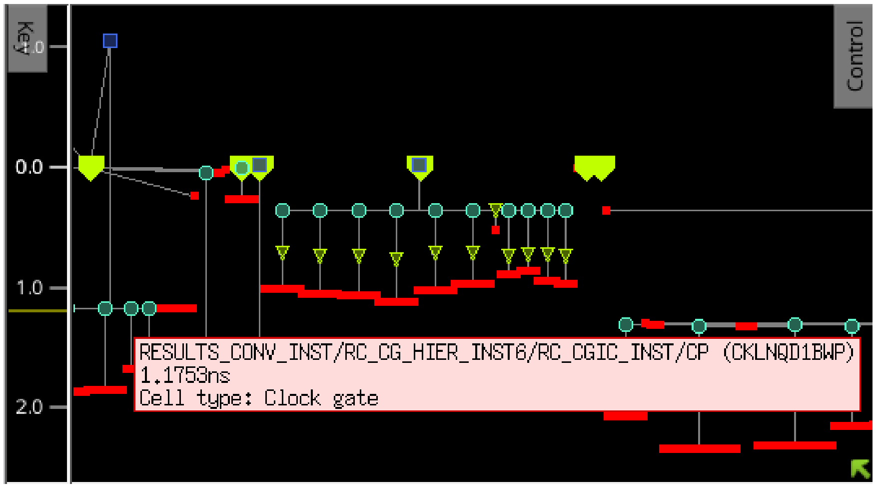
Dim Background of Clock Tree Debugger Display

In addition to the above features, the clock tree debugger allows you to dim the background of the display area. This allows you to view selected and highlighted objects more clearly. This is useful when you are debugging clock trees. To dim the display, press F12. The F12 key is used as a three-way toggle. So, to quit the dim mode, press the F12 key again twice. This is shown in the image below.



Clock Tree Debugger - Tooltips

The tooltips are provided to let you view relevant information about any object by hovering the pointer over that object in the display area. This is shown in the image below.



Clock Tree Debugger - Menu Bar

The *Clock Tree Debugger* has the following menus:

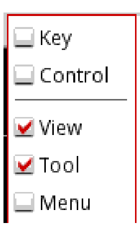
- View Menu
- Visibility Menu
- Color by Menu

You can tear off any menu or submenu and place it anywhere in the layout window. To tear off a menu or submenu, click on the dotted line that appears at the top of the menu or submenu, and drag the menu to where you want it displayed in the design area. The menu remains on the screen as a window when you release the mouse button.

Toolbar Widgets

The following row of widgets, located below the menus and above the display area, includes shortcuts for some commonly used commands, forms, and menus in CTD.

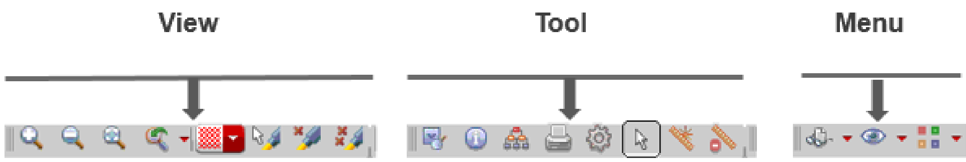
Right-click on the toolbar to enable or disable all or a particular group of widgets. The following options are available:

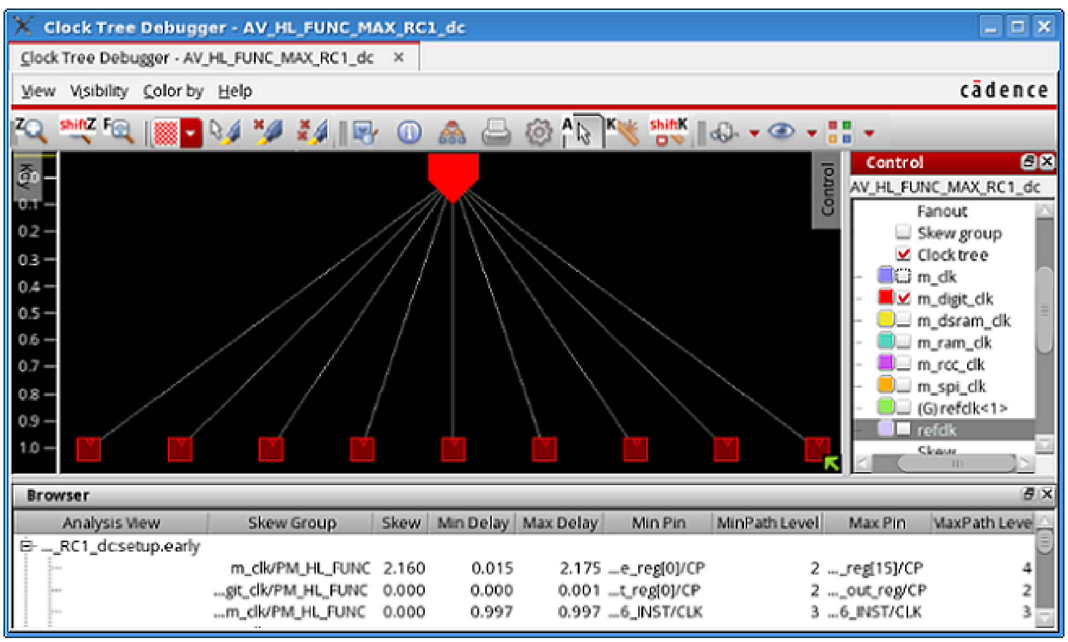


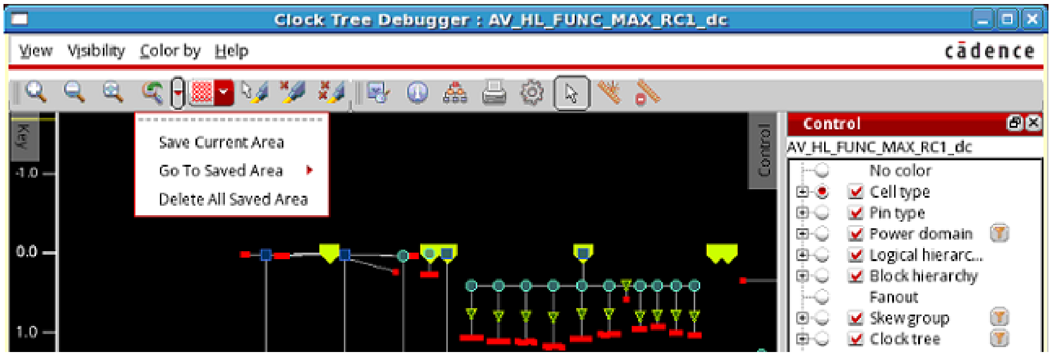
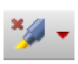
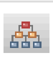
- The options, *Key* and *Control* allow you to toggle the visibility of the Key Panel and Control Panel, respectively.
- The *View* widgets provide options to customize the clock tree display.
- The *Tool* widgets open up forms in CTD.

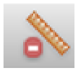
- The *Menu* widgets display all the submenus of the CTD main menus.

The widgets enabled by the *View*, *Tool*, and *Menu* options are detailed below.



Widget	Description
	*Zoom In*--Click this widget to zoom into a smaller area of the clock tree to view it in greater detail. Each click zooms in one level. The equivalent bindkey is `z`.
	*Zoom Out*--Click this widget to zoom out of the clock tree. Each click zooms out one level. The equivalent bindkey is `Shift+Z`.
	*Fit*--Click this widget to fit the clock tree within the display area. You can also select one clock tree or specific clock trees in the control panel. In this case when you click the widget, only the selected trees will be fit in the display area. This is shown below. The equivalent bindkey is `f`. 

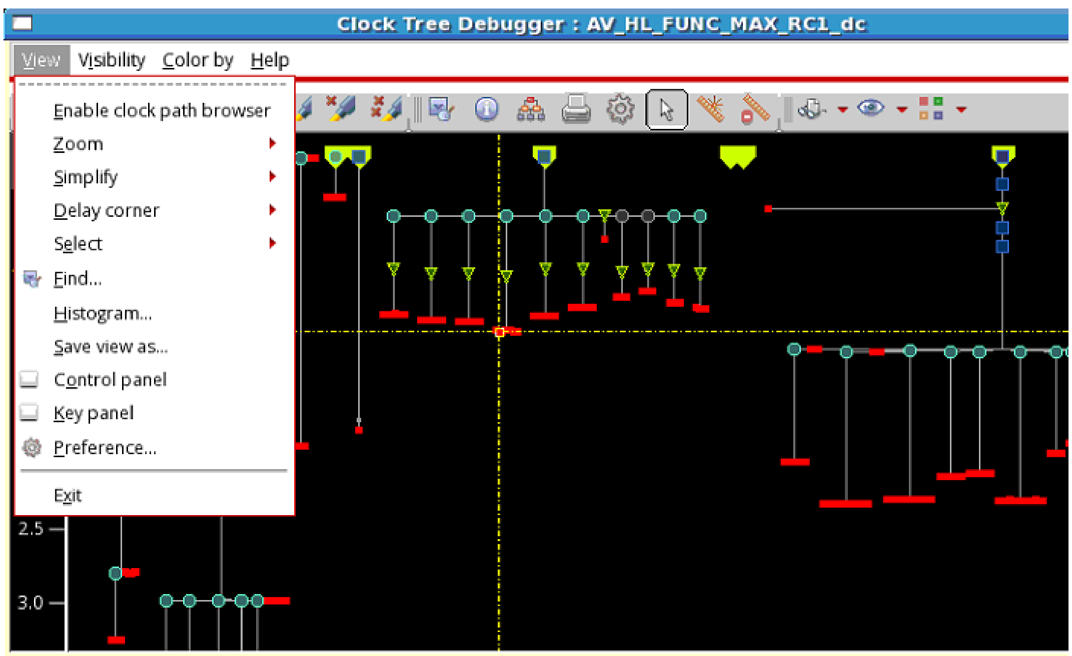
	*Zoom Previous*–Allows you to save a current display and view previously-saved displays. When you click this widget, a drop-down menu is available.  In this menu: • Click *Save Current Area* to save the current display. • Click *Go To Saved Area* to view a previously-saved display. You can save multiple displays. They are numbered 1,2,3...and so on. You can select the display you want to view again. • Click *Delete All Saved Area* to delete all previously-saved displays.
	*Edit Highlight Color*–Allows you to select a highlight color from the available choices in the drop-down menu.
	*Highlight Selected*--Highlights the objects selected in the GUI with the current highlight set, as displayed in the *Edit Highlight Color* widget. Use the drop-down menu to select a new highlight set.
	*Clear Highlight*--Clears the highlight from those objects that are highlighted with the current highlight set, as displayed in the *Edit Highlight Color* widget.
	*Clear All Highlight*--Clears all highlights from the GUI.
	*Find*--Opens the Find/Select Object form.
	*Attribute Editor*--Opens the Attribute Editor for the selected object.
	*Design Browser*--Opens the Design Browser form.
	*Print*–Opens the Dump View form.
	Opens the Set Preference form.

	*Select* - Enables the select arrow. The equivalent bindkey is A.
	*Create Rulers* - Click this widget, then left-click in the display area and drag the mouse to add a ruler (in micrometers), and left-click again to end the ruler. The equivalent bindkey is k.
	*Clear All Rulers*--Clears all rulers from the display area. The equivalent bindkey is Shift+`K`.
	*View*–Provides all the options of the View menu of the CTD in a drop-down menu.
	*Visibility*–Provides all the options of the Visibility menu of the CTD in a drop-down menu.
	*Color by*–Provides all the options of the Color by menu of the CTD in a drop-down menu.

Clock Tree Debugger - View Menu

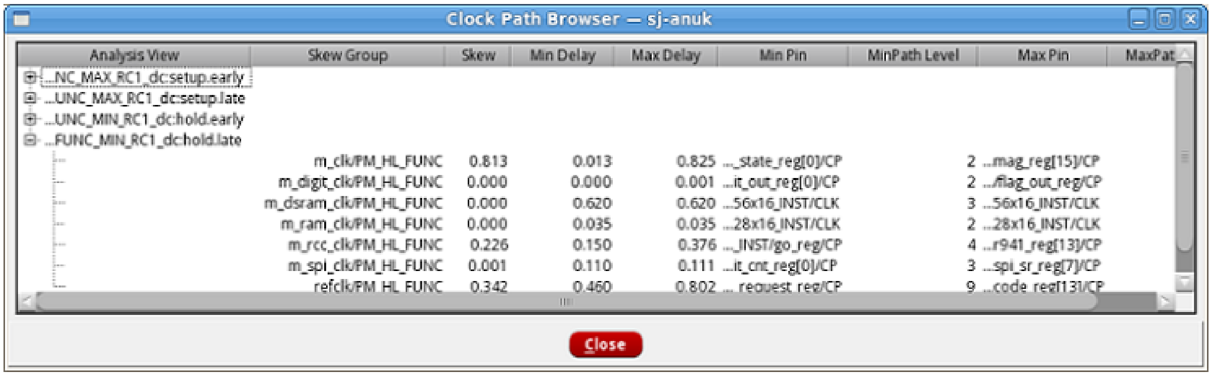
Use the *View* Menu to customize the clock tree display.

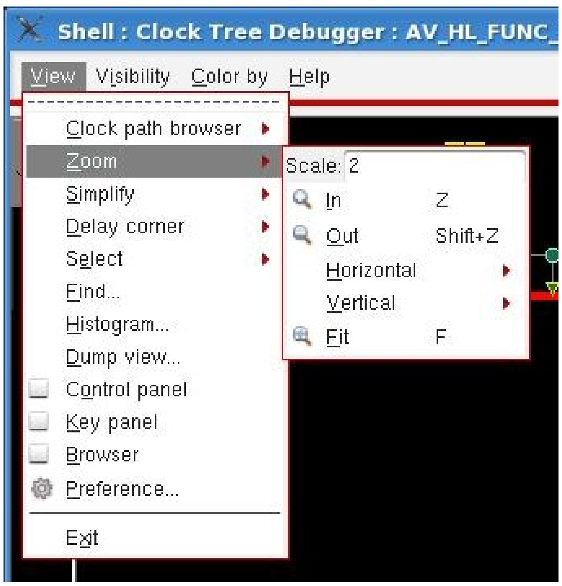
→Choose *Clock Tree Debugger* – *View*.

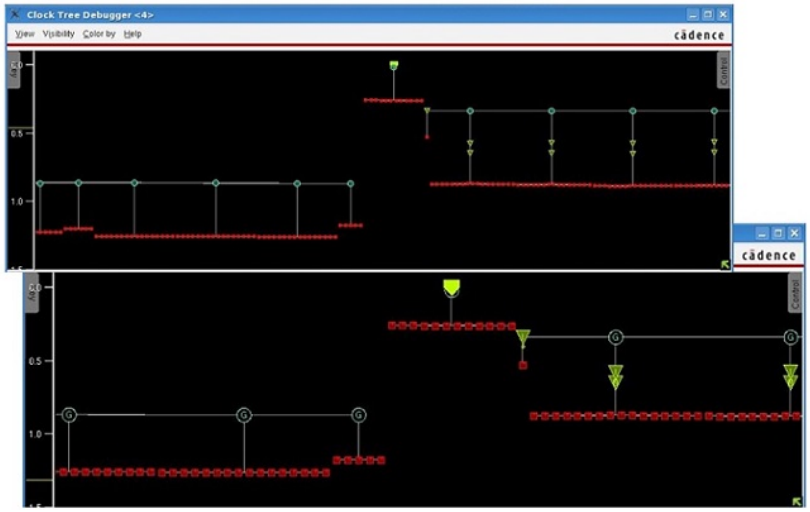
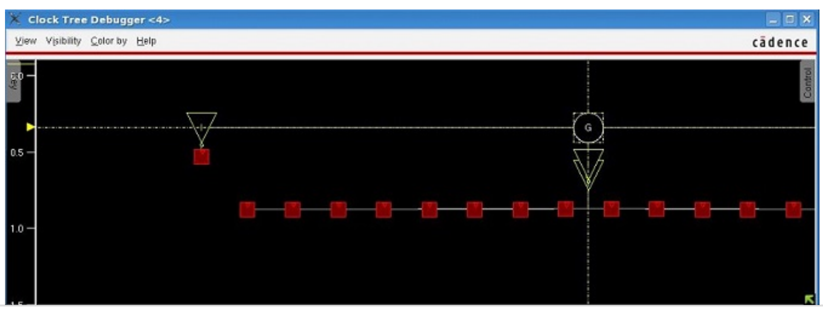


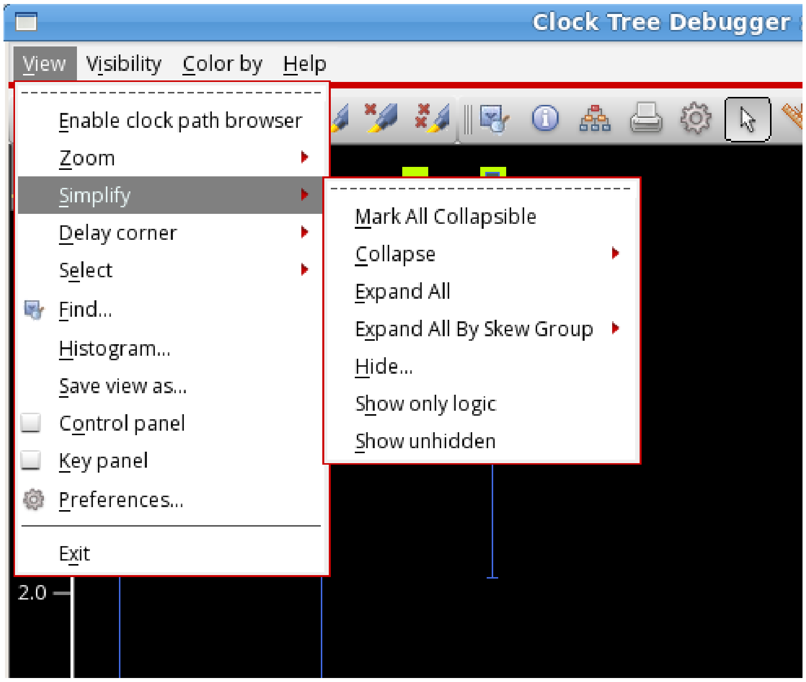
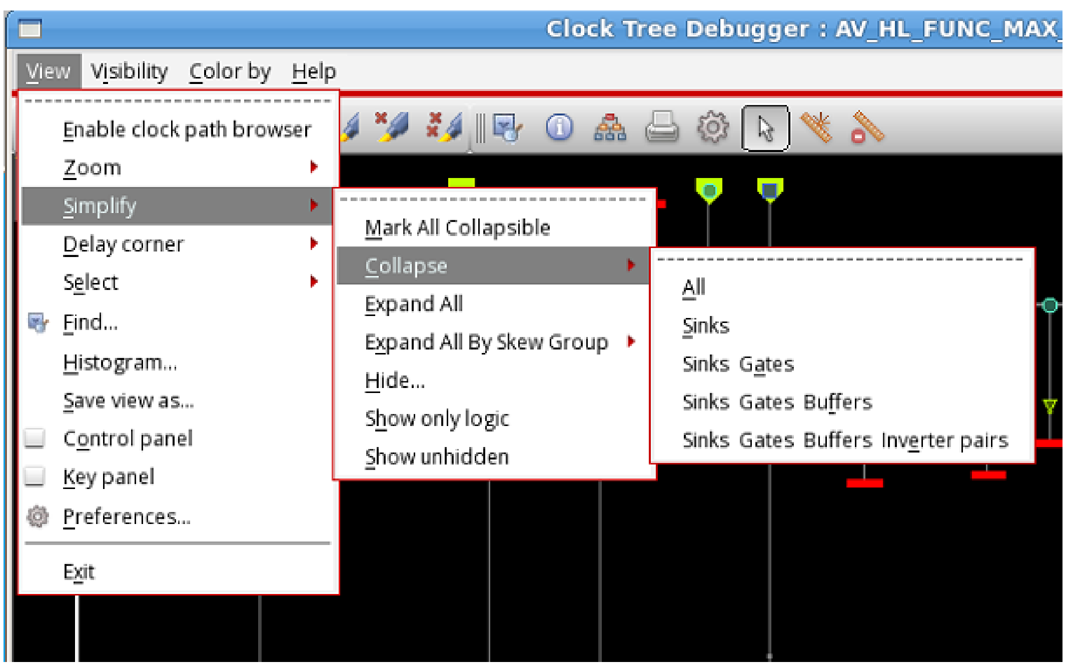
Options	Descriptions

<table>
<tr><td>Enable clock path browser</td><td colspan="2">Opens the clock path browser. The clock path browser opens in a separate window. For more information, see Clock Path Browser.

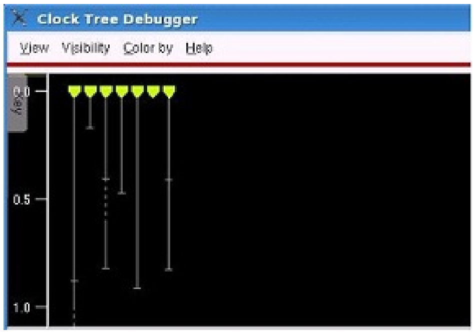

</td></tr>
<tr><td>Zoom</td><td colspan="2">Allows you to zoom in and out of the clock tree view.


</td></tr>
<tr><td></td><td>Scale</td><td>Allows you to specify the scale of zoom in or zoom out of the clock tree view.</td></tr>
<tr><td></td><td>In</td><td>Zooms into the clock tree view.</td></tr>
<tr><td></td><td>Out</td><td>Zooms out of the clock tree view.</td></tr>
</table>

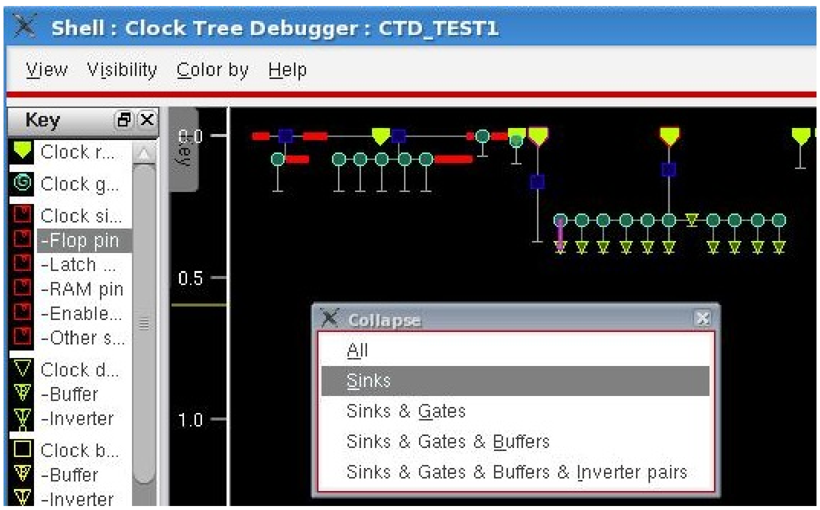
	Horizontal	Zooms in or out of the clock tree view horizontally. In this submenu, you can select *In* or *Out*. You can also use the keys, "x" and "shift x" to zoom in and out of the display horizontally or along the x-axis. By default, the display will zoom with respect to its center point as shown in the image below.  To zoom into specific objects, select the object and keeping the left mouse button pressed, press "x". This is shown in the image below. 
	Vertical	Zooms in and out of the clock tree view vertically. In this submenu, you can select *In* or *Out*. You can also use the keys, "y" and "shift y" to zoom in and out of the display vertically or along the y-axis. By default, the display will zoom with respect to its center point.
	Fit	Zooms in or out to fit the *Clock Tree Debugger* window.

Simplify	Manages the complexity of the clock tree visualization.  	
	Mark All Collapsible	Marks all nodes as collapsible. This includes all nodes that may have been marked uncollapsible using the "Mark Uncollapsible" option available in the context menu of the CTD.
	Collapse	Provides options to collapse subtrees that consist of clock gates and flops in their fanout. There are different options available for collapsing subtrees in the drop-down menu of this option. These options are shown in the image below. 

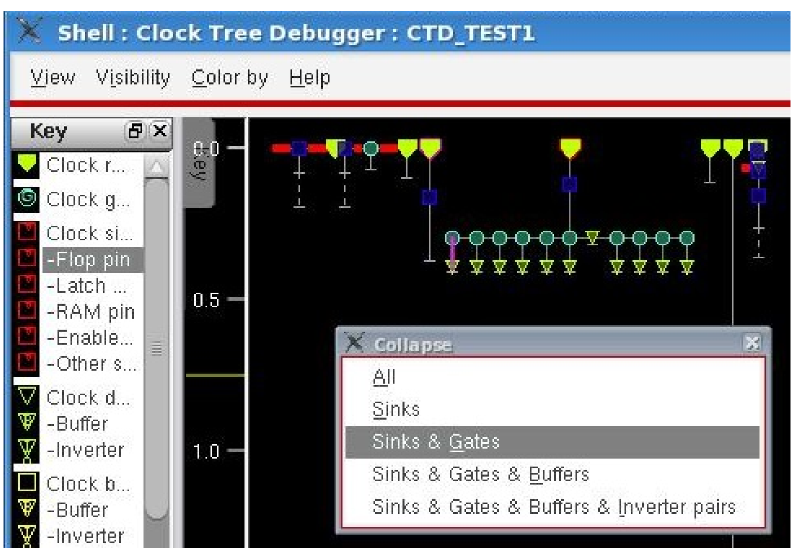
All - Collapses everything up to the top-level clock tree roots, so that the visualization shows only a set of clock trees represented by vertical summary bars.



Sinks - collapses subtrees with sinks.



Sinks & Gates - collapses subtrees with clusters of gates directly driving sinks.



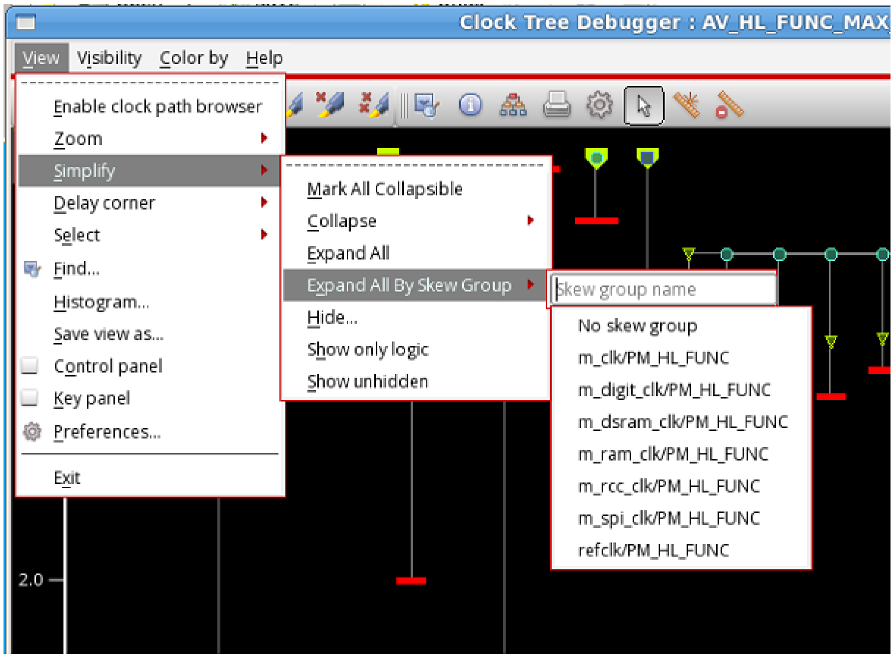
Sinks & Gates & Buffers - collapses subtrees with clusters of gates driving sinks connected by buffers

		Sinks & Gates & Buffers & Inverter pairs - collapses subtrees with clusters of gates driving sinks connected by buffers or inverters where the edge is not changed ⚠ You can also double-click to collapse the subtrees of any node of the clock tree.
	Expand All	Expands everything so that no subtree is collapsed. ⚠ You can also double-click to expand the subtrees of any node of the clock tree.

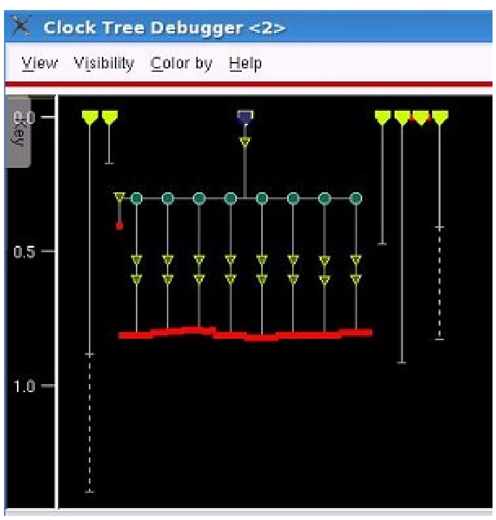
Expand All By Skew Group

Expands all subtrees that pass through the selected skew group, choosing parents of reconvergent nodes that are in the skew group.

You can specify a skew group as shown below.

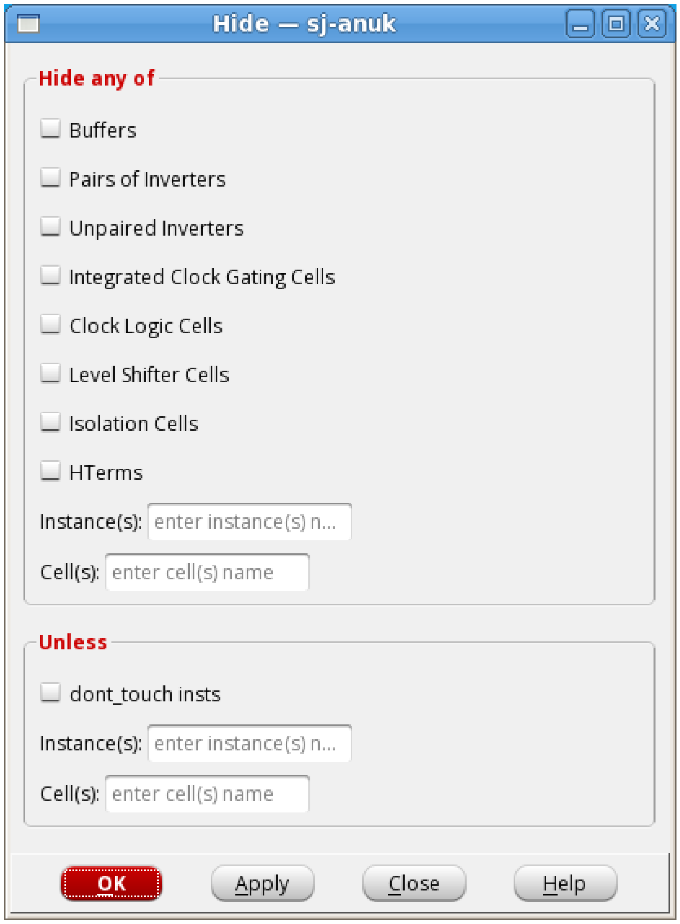


The image below shows the expanded subtrees for the skew group specified in the image above.



Hide

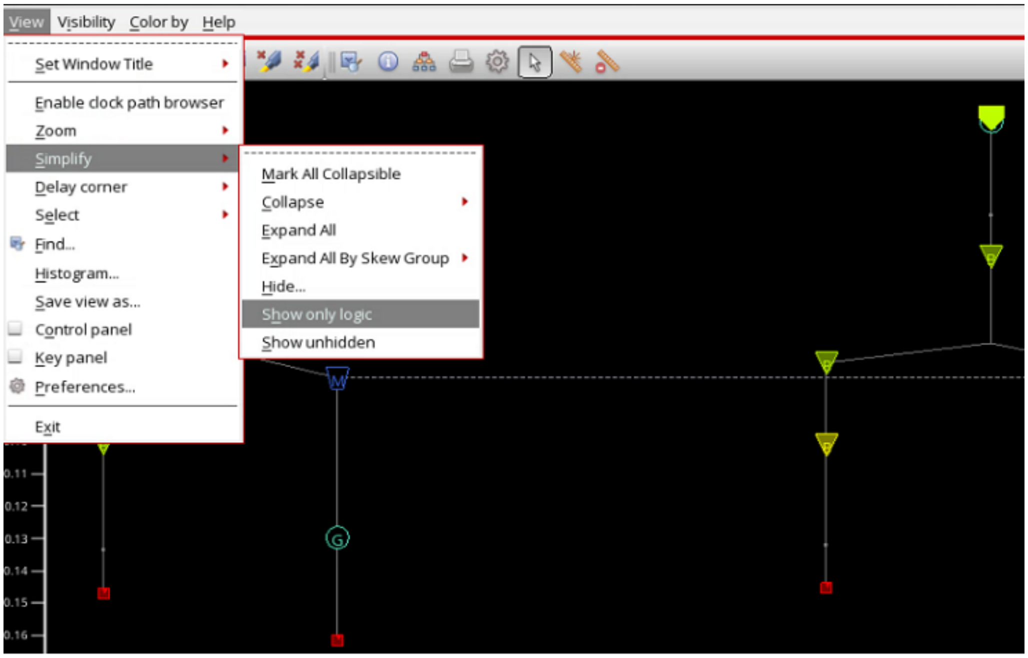
Hides specified instances and cells from view in the Clock Tree Viewer. The hidden objects are shown as small icons in the visualization. When you click this option, the form below opens.



Options	Descriptions
Buffers	Hides all buffers of the clock tree.
Pairs of Inverters	Hides all pairs of inverters of the clock tree.
Unpaired Inverters	Hides all unpaired inverters of the clock tree.
Integrated Clock Gating Cells	Hides all integrated clock gating cells of the clock tree.
Clock Logic Cells	Hides all clock logic cells of the clock tree.
Level Shifter Cells	Hides all level shifter cells of the clock tree.

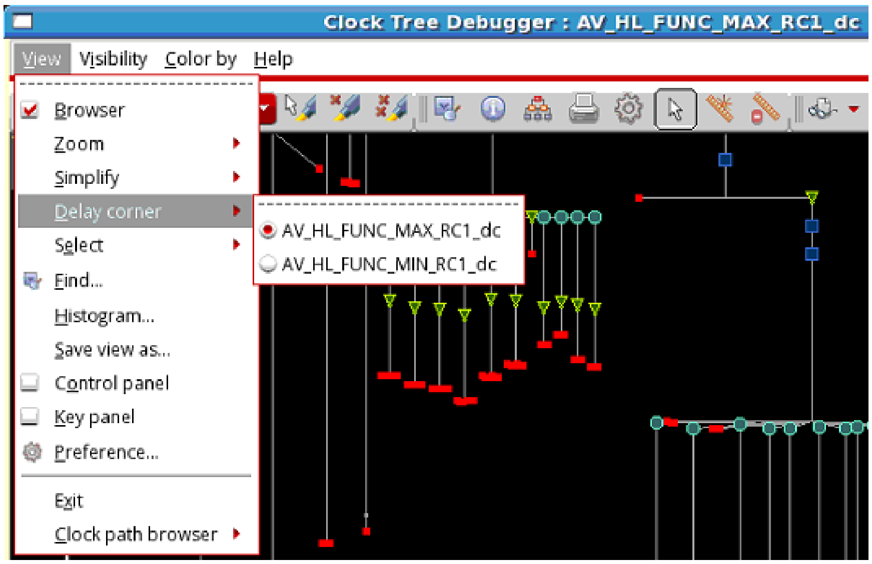
Isolation Cells	Hides all isolation cells of the clock tree.
HTerms	Hides all the preserved ports. The preserved ports are visible only in the Unit Delay mode. Use this option to hide the port bits. **Note**: The name of this option in Stylus menu is *HPins*.
Instance(s)	Names of instances to be hidden. You can provide multiple instance names separated by a space.
Cell(s)	Names of cells to be hidden. You can provide multiple cell names separated by a space.
dont_touch insts	Specifies that any clock tree objects that have the dont_touch constraint in the SDC and are specified, should not be hidden. You can specify the following: • *Instance(s) - You can provide multiple instance names separated by a space.* • *Cell(s) - You can provide multiple cell names separated by a space.*

All options are unselected by default. For details, see the "Abstraction Function in CTD" section.

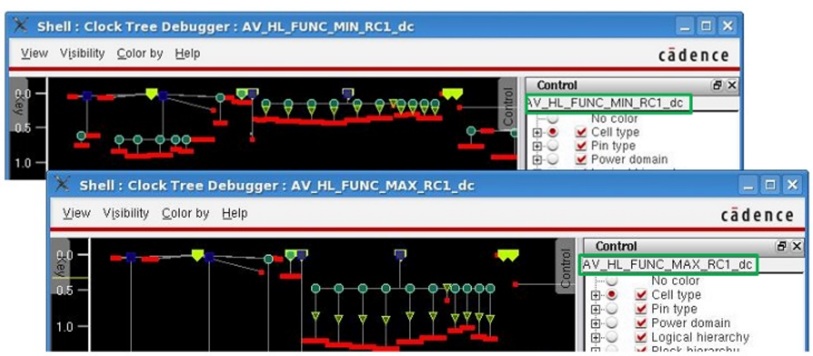
	Show only logic	Hides all the buffers, inverters, clock gates, and collapses subtrees consisting entirely of sinks, buffers, inverters or clock gates in a single step. Only logic cells are displayed. 
	Show unhidden	Expands all the hidden instances and cells in the Clock Tree Viewer.

<table>
<tr>
<td>Delay corner</td>
<td colspan="2">
Selects the delay half-corner you want to use to produce the visualization. This delay corner is mainly used to calculate timing for delays, as shown on the y axis, but also determines the set of available clock trees and available skew groups.

Note: When you select a delay corner, the name of the delay corner appears in the title bar of the CTD. This is shown below.

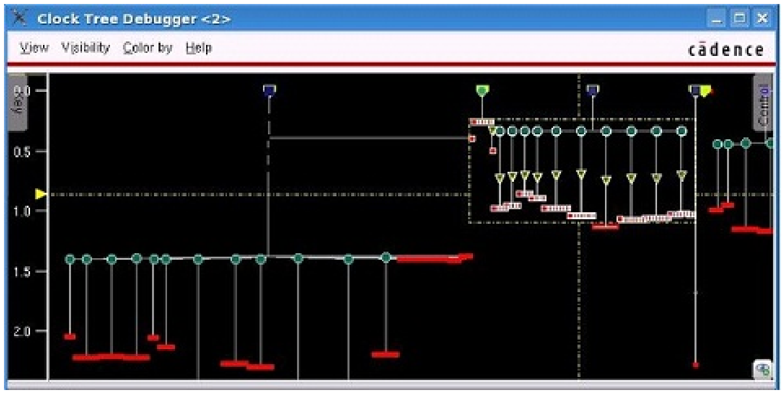


You can also switch the delay corner by using the bindkeys. Use the “d” key to switch to the next delay corner and use "D" or "shift + d" to display the default delay corner. The name of the current delay corner, which is displayed both in the information bar on the top of the Control Panel and in the title bar of the CTD, will be updated every time the delay corner is switched using the bindkey. This is shown in the image below.

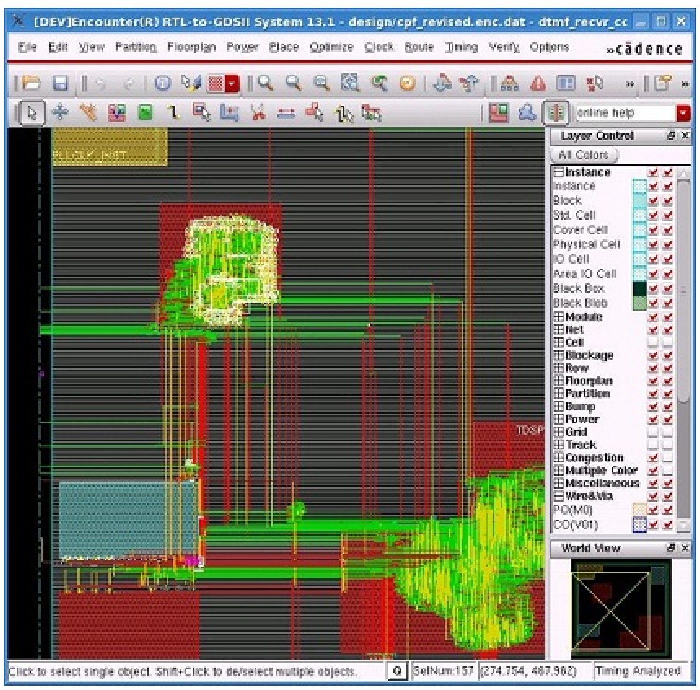


</td>
</tr>
<tr>
<td>Select</td>
<td colspan="2">Selects the specified object.</td>
</tr>
<tr>
<td></td>
<td>Select minimum</td>
<td>Selects the object with the minimum value for the current coloring.</td>
</tr>
</table>

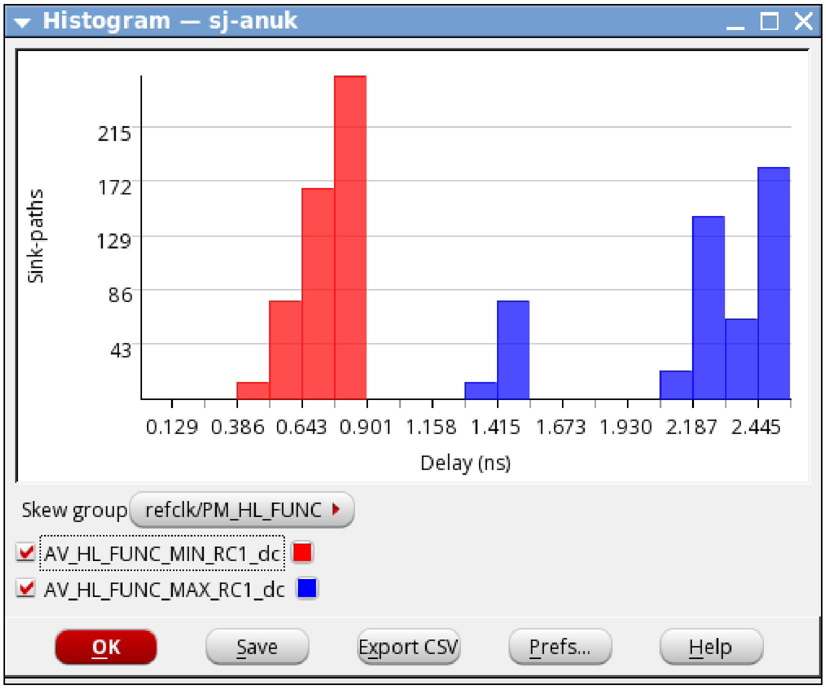
<table>
<tr><td></td><td>Select maximum</td><td>Selects the object with the maximum value for the current coloring.</td></tr>
<tr><td></td><td>Enable crossprobing</td><td>
Allows you to turn on/off cross-probing - locating objects in the layout window when the corresponding object is selected in the Clock Tree Debugger, and vice versa.

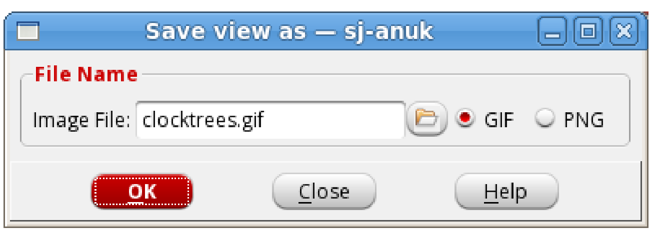


The layout view of the above selection is shown below:

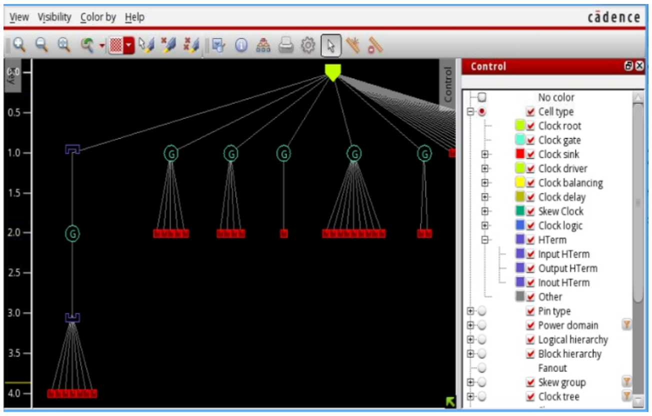


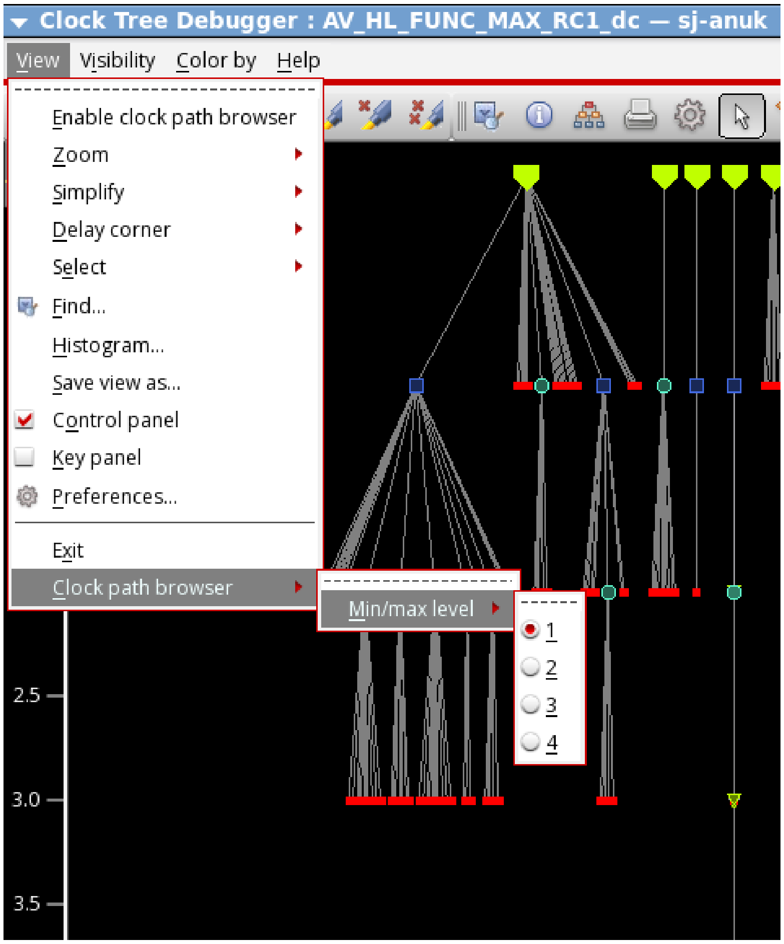
For an example of cross-probing of a clock root, see the "Cross-probing of Clock Root" section.
</td></tr>
<tr><td></td><td>Enable zoom selected</td><td>Allows you to turn-off zoom selected while cross probing. By default, this option is enabled.</td></tr>
</table>

<table>
<tr><td>Find...</td><td>Finds and selects specific object types in the design display area. For more information about the various fields and options in this form, see Find/Select Object in the Edit Menu chapter.</td></tr>
<tr><td>Histogram</td><td>Displays histogram of number of sink paths versus clock insertion delay for skew groups.


For details, see the "Clock Tree Debugger Histogram" section.</td></tr>
<tr><td>Save view as...</td><td>Saves the current snapshot of the clock tree viewer into a file. When you click this option, the Save view as form opens.


<table>
<tr><th>Option</th><th>Description</th></tr>
<tr><td>Image File</td><td>Specifies the name of the file where you want to dump the display image.
Default: <code>dump.gif</code></td></tr>
<tr><td>GIF</td><td>Specifies that the format of the image should be GIF.</td></tr>
<tr><td>PNG</td><td>Specifies that the format of the image should be PNG.</td></tr>
</table>
</td></tr>
</table>

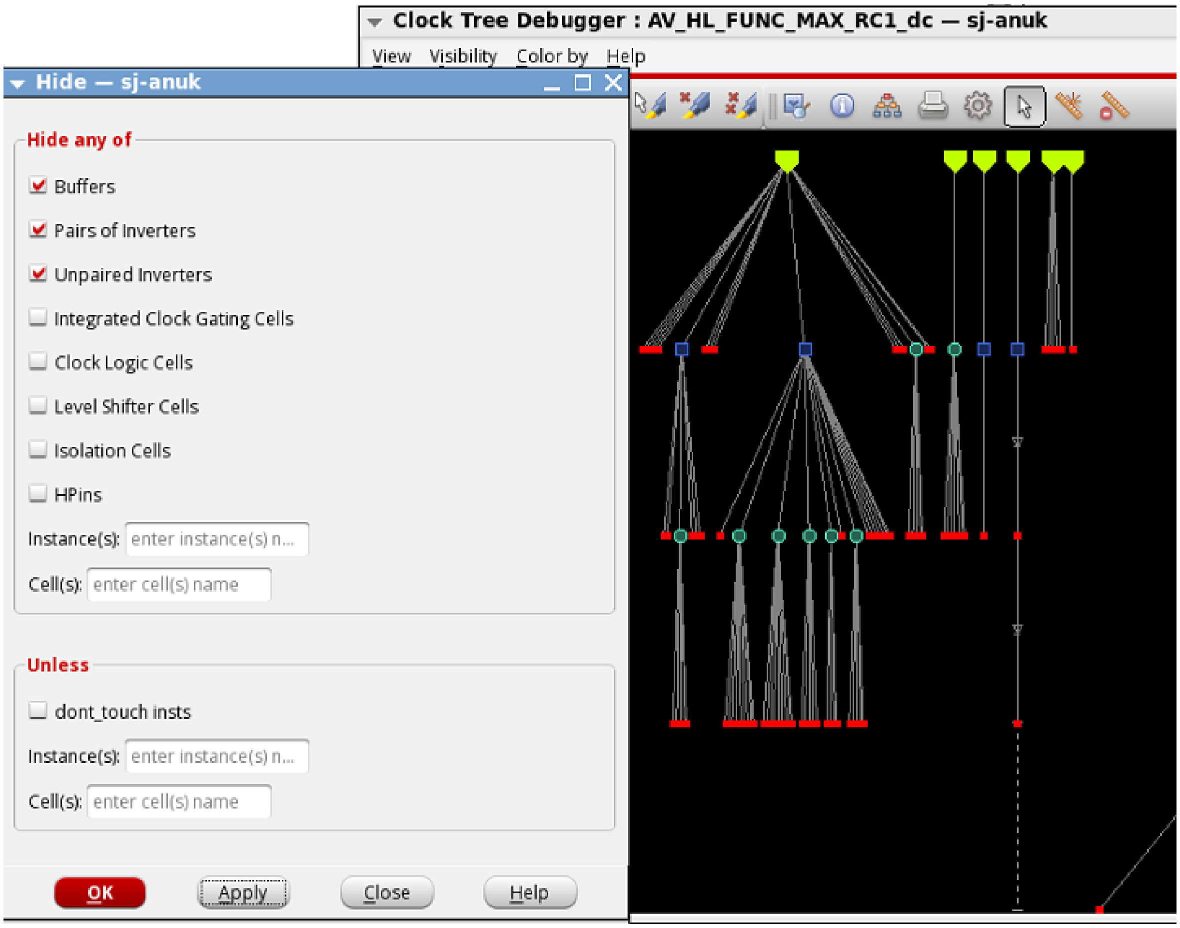
Control panel	Controls the visibility of the control panel in the *Clock Tree Debugger* window. When checked, you can drag and view the control panel on the right side of the *Clock Tree Debugger* main window and the *key panel* on the left side of the main window, as shown below. The *Control panel* shows the current selections for *No color, Cell type, Pin Type, Power domain, Logical hierarchy, Block hierarchy, Fanout, Skew group, Clock tree, Skew, Transition time, Max trans violations, Net length, Net length violations, Total net cap, Max cap violations, Setup slack, Hold slack, Window outage, Signal edge, Net type, Route type, Constraints,* and *Timing windows*.  For details, see the "Control Panel" section.
Key panel	When enumeration or subset coloring is in effect, a window showing a key is available in the Clock Tree Debugger. The key contains a list of enumeration categories or subsets and their corresponding colors. For details, see the "Key Panel" section.
Preference	Opens the Set Preference form. In this form, you can specify the GUI configuration settings for clock tree viewer, histogram, and world viewer. For details, see "Set Preferences for CTD GUI Configuration" section below.
Exit	Allows you to exit the *Clock Tree Debugger* tool.
Clock path browser	Specifies the min/max setting of the Browser window. *Min/max level:* Specifies the number of min/max levels for the skew groups in the Browser. You can choose 1, 2, 3, or 4 to view the first, second,third, or fourth level of min/max paths for skew groups.



By default, 1 is selected. When you choose an option in the above submenu, the Clock Path Browser is updated to show the specified number of min/max paths. An example is provided below.

The Hide Function in CTD

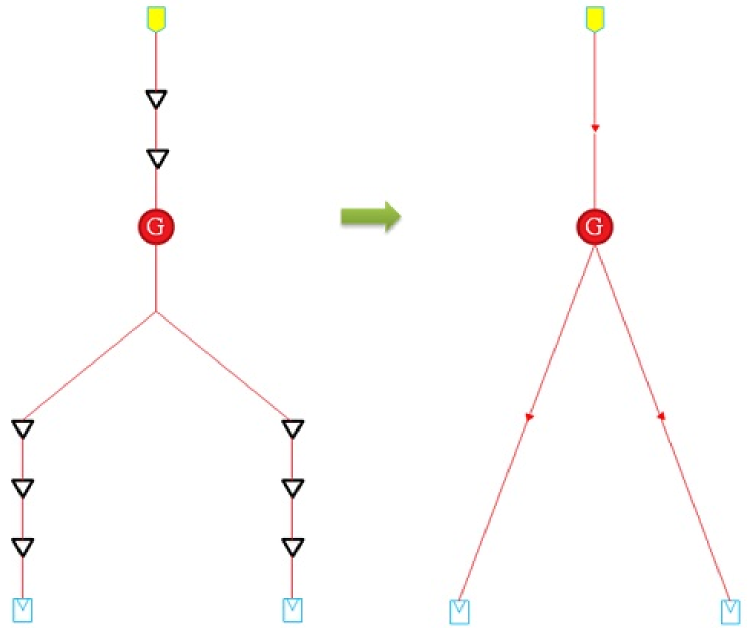
To hide instances or cells from view in the Clock Tree Viewer, you can select the *Hide* option in the *Simplify* submenu in the *View* Menu. In the Hide form, you can specify the buffers, inverters, the instances, and cells that you want to hide.



Hiding Buffers and Inverters

The figure below illustrates the behavior of only hiding buffers and inverters of clock trees. When you specify only the Buffers or Pairs of Inverters options or Unpaired Inverters in the Hide form, then all cascaded logic will be turned into one small icon, which will be a small red triangle. This is shown in the figure below.

After hiding, the hidden part of clock tree will no longer care about the delays, and the hidden structure will show the simplified clock tree logic structure. The structure will turn into a simplified structure in which the basic element is a path from one “non-hidden” point to another “non-hidden” point or to a sink pin. This path contains a start point, an end point, a small icon that stands for the hidden clock tree logic, and a flight line that connects the start point and end point, and feeds through the small icon. A “non-hidden” point is the clock tree object which is not included in user-specified list.

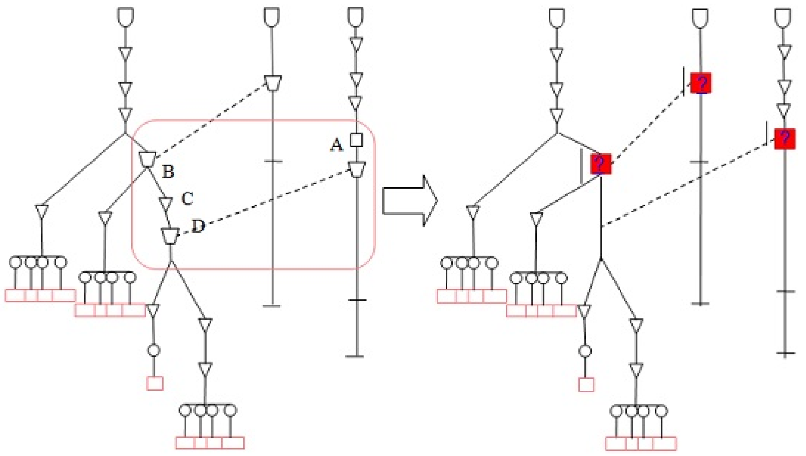


Hiding Clock Logic Cells

Clock logic cells, such as clock gate cells, can be specified for hiding. If the cells, which are connected directly, contain any clock logic (excluding buffers and inverters), then they are collapsed as large red square icons in the Clock Tree Viewer. The red square has a question mark "?" in the center, which indicates that the content is unknown or complex. This size of the red square icon is larger than the symbol shape of the normal clock objects. This square icon is placed at the earliest point at which it is encountered in each clock tree.

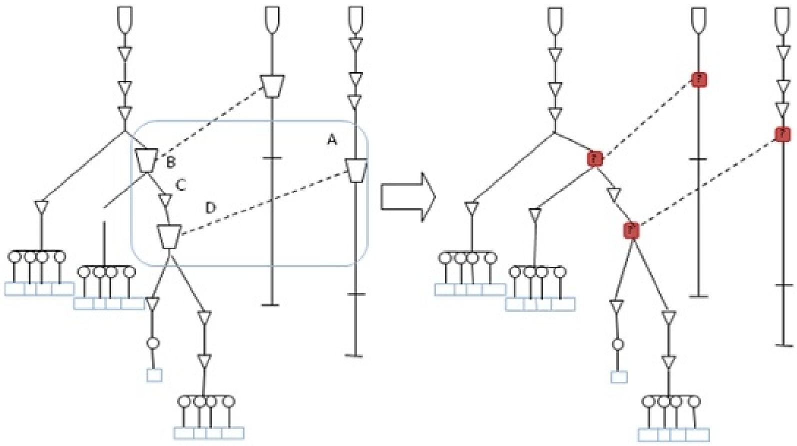
In the sample scenario 1 shown below, the points A, B, C, and D are user-specified points. The points B, C, and D are on the same clock tree so the square icon is placed only on point B, which is encountered first. The vertical line below the hidden logic is used to show the total delay across the logic, and connect offshoots in and out at the appropriate time offsets.

Sample Scenario 1

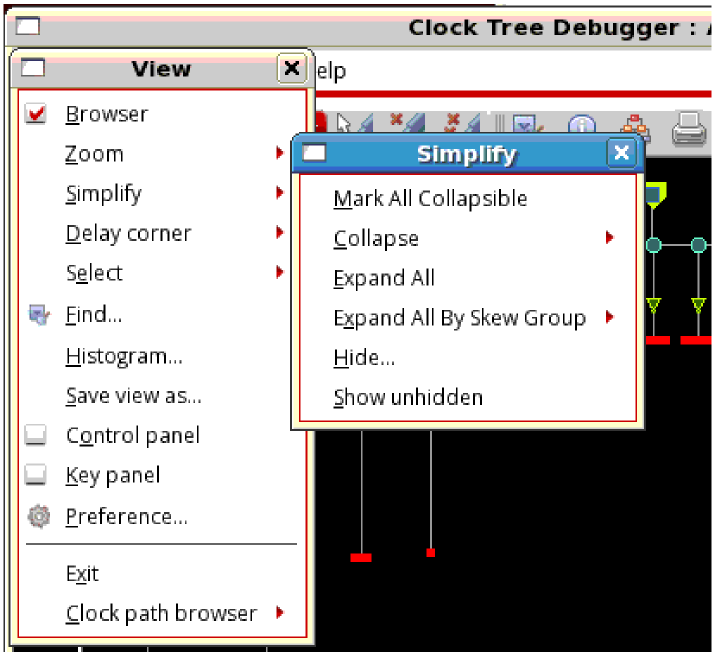


Now consider another scenario in which point C is not specified by the user for hiding. In this case, the hide will be as shown below. The red square icon will be placed on both points B and D.

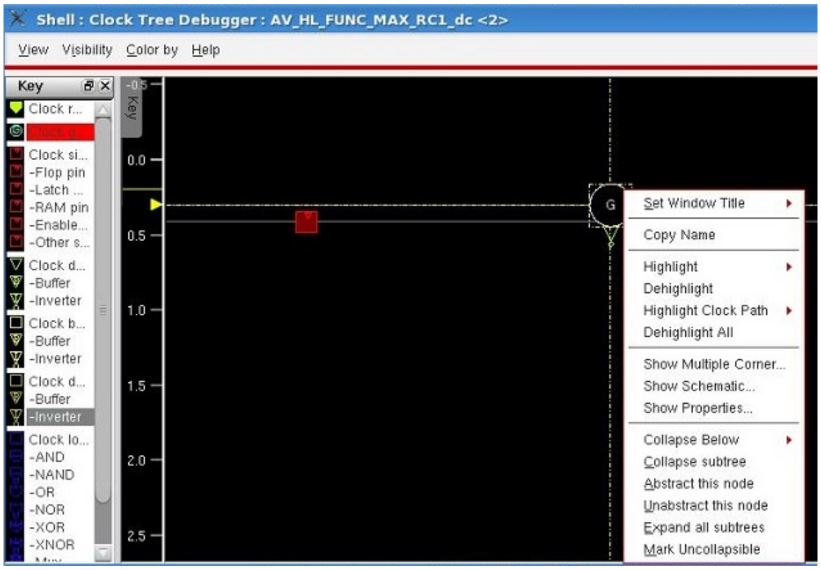
Sample Scenario 2



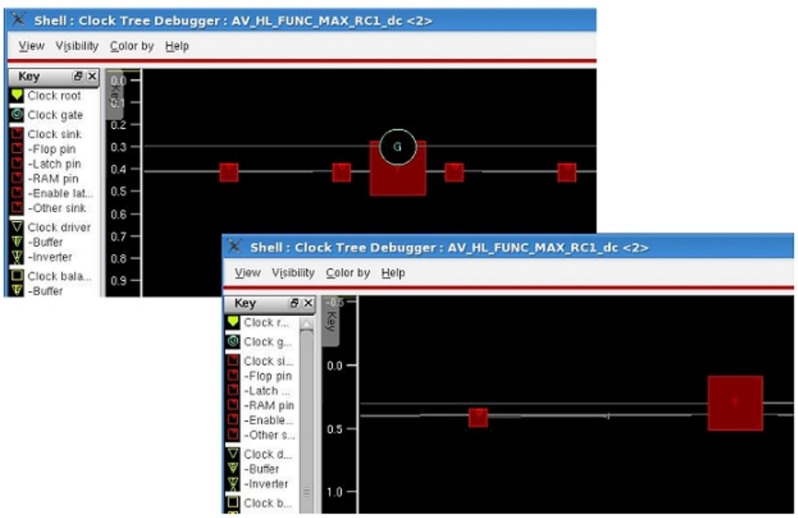
To view the hidden objects again, select the *Show unhidden* option in the *Simplify* submenu of the View menu.



The hide function also allows you to hide and unhide selected nodes by clicking options, *Abstract this node* and *Unabstract this node*, provided in the content menu of the Clock Tree Viewer.



Below is a screenshot showing the hiding of a selected clock gate.

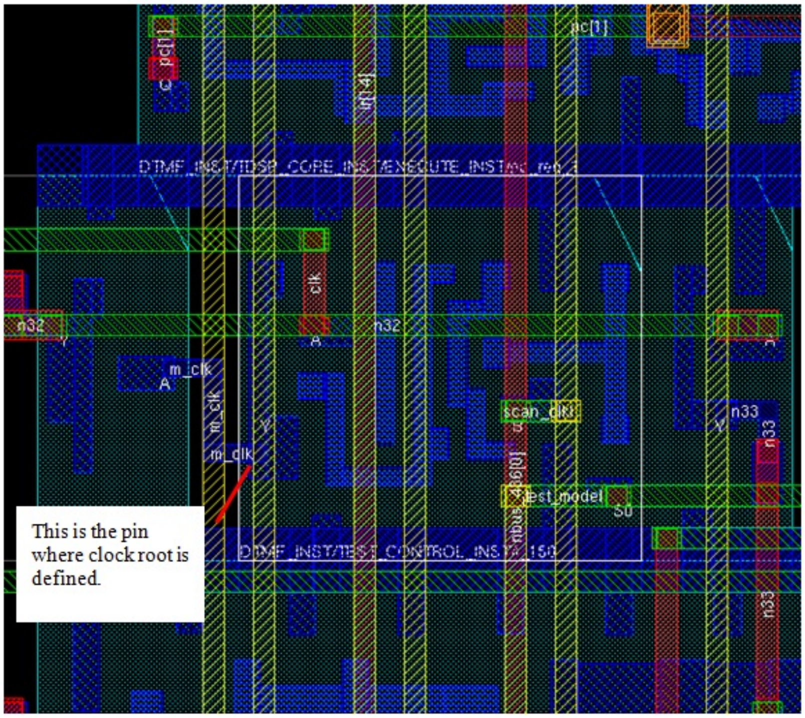


Cross-probing of Clock Root

To cross-probe a clock root, select the clock root symbol in the display area of the CTD. Then select the *View* menu and check the *Enable crossprobing* option in the *Select* submenu. The layout window will zoom into the object in which that clock root is defined. The object of clock root could be a cell pin, an I/O port, or an I/O pad. If the clock root is a cell pin, layout window will zoom in the area of that pin and select that cell. This is shown in the figure below.

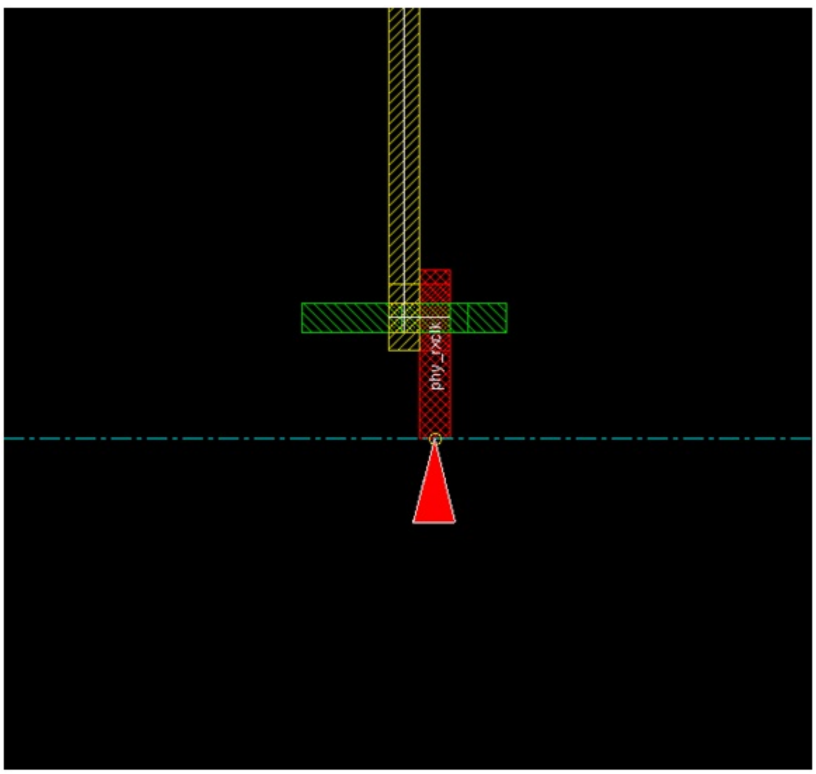
Note: Alternatively, you can select the clock root pin, port, or pad - depending on where the clock root is defined - in the layout window and the clock root will be selected in the CTD.

Clock Root in Cell Pin



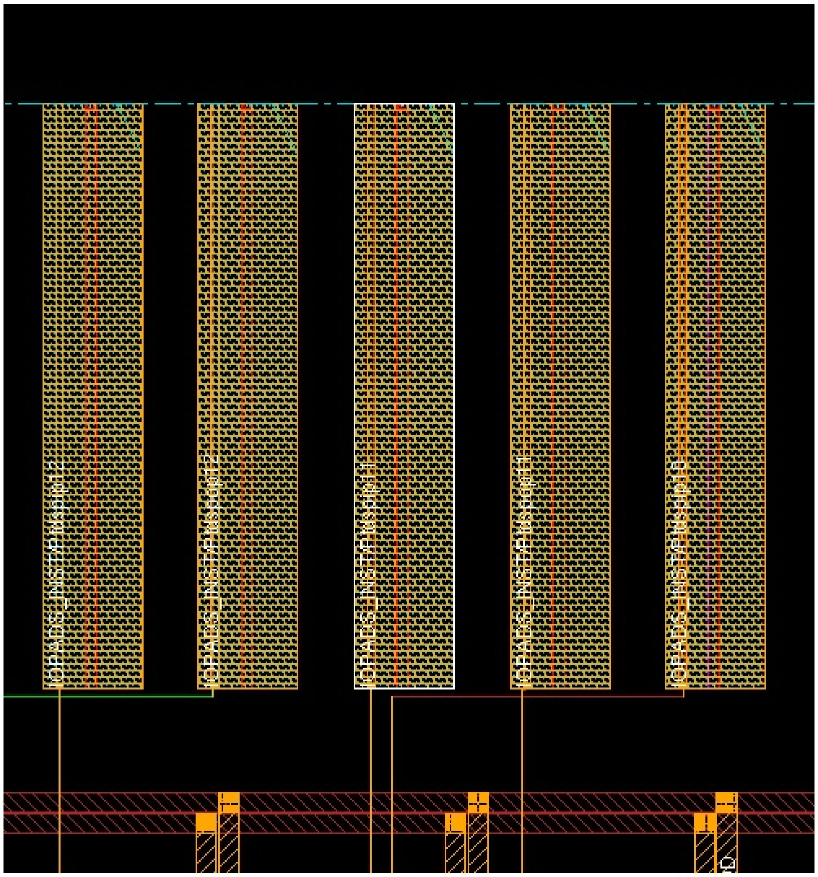
If the clock root is defined in an I/O port, the layout window will zoom to the area where the port is and select that port.

Clock Root in I/O Port



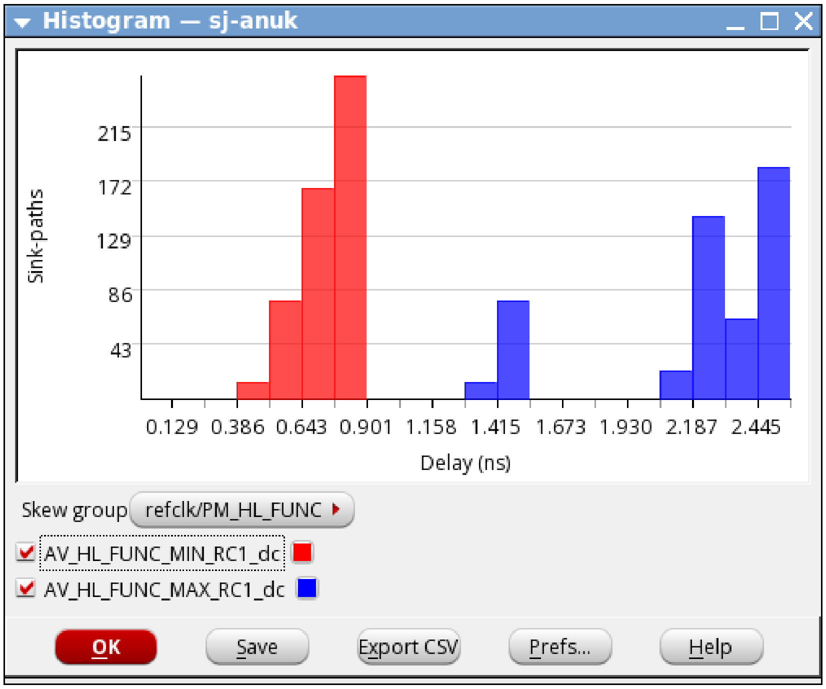
If the clock root is defined in an I/O pad, the layout window will zoom to the area where the pad is and select that pad.

Clock Root in I/O Pad



Clock Tree Debugger Histogram

Displays histogram of number of sink paths versus clock insertion delay. In the *View* menu, choose *Histogram*. The form shown below opens. The vertical axis of the histogram shows the number of sink paths that have the delay shown (in nanooseconds) on the horizontal axis of the histogram. You can view histogram for multiple corners at once in different colours. You can also Export the data displayed in the histogram in a CSV format.

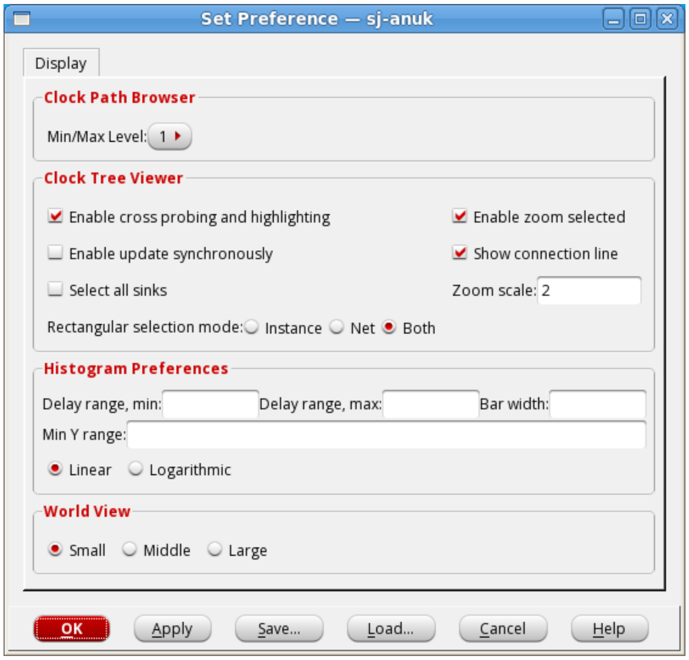


Options	Descriptions
Skew group	Specifies the skew group to be displayed in the histogram. You can select different skew groups from the dropdown list. You can also select the delay corners for which to display the graph. The graphs for different delay corners is diplayed in different colors.
Export CSV	Exports the underlying data in a CSV format.
Prefs...	Opens the Set Preference form. In this form, you can select preferences for the histogram.
Save	Saves the histogram information to a file.

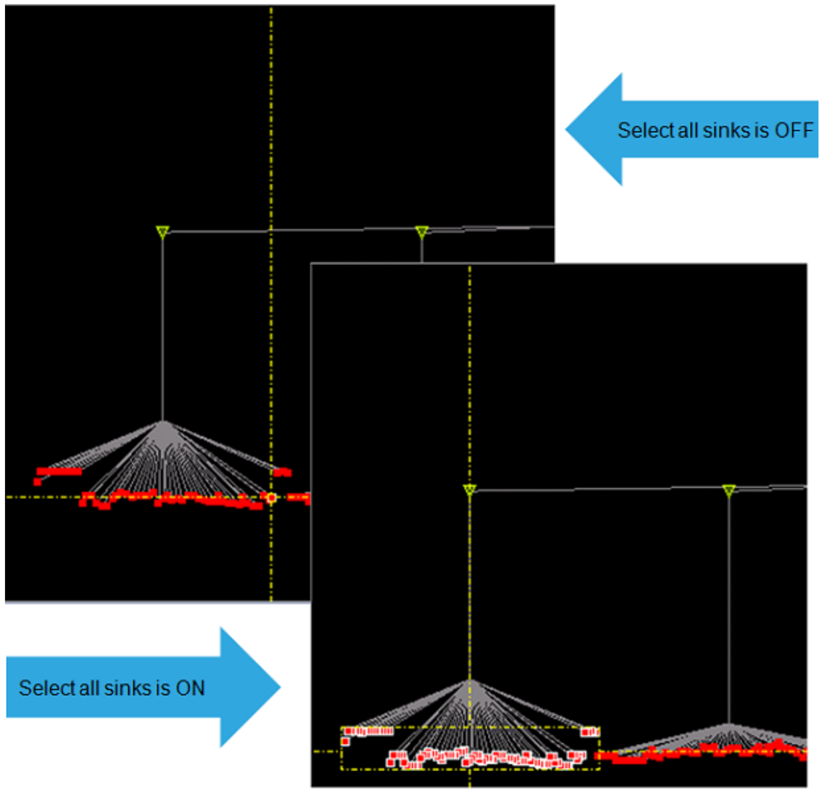
You can also click the *Preference* submenu in the *View* menu of the CTD to open this form. For details, see "Set Preferences for CTD GUI Configuration" section below.

Set Preferences for CTD GUI Configuration

Displays settings for Clock Path Browser, Clock Tree Viewer, Histogram, and World Viewer. In the *View* menu, choose *Preference*. The following form opens:



Options	**Descriptions**	
Clock Path Browser	*Min/Max Level*	Specifies the number of min/max levels for the skew groups in the Browser. You can choose 1, 2, 3, or 4 to view the first, second, third, or fourth level of min/max paths for skew groups. By default, 1 is selected. When you choose an option in the above submenu, the Clock Path Browser is updated to show the specified number of min/max paths.
Clock Tree Viewer	Displays the settings for the clock tree viewer.	
	Enable cross probing and highlighting	Allows you to turn on/off cross-probing and highlighting - locating objects in the layout window when the corresponding object is selected in the CTD, and vice versa. By default, cross probing is enabled.
	Enable update synchronously	When enabled, if you manually ECO the clock nets or nodes, the clock tree graph in Clock Tree Viewer will be updated accordingly.

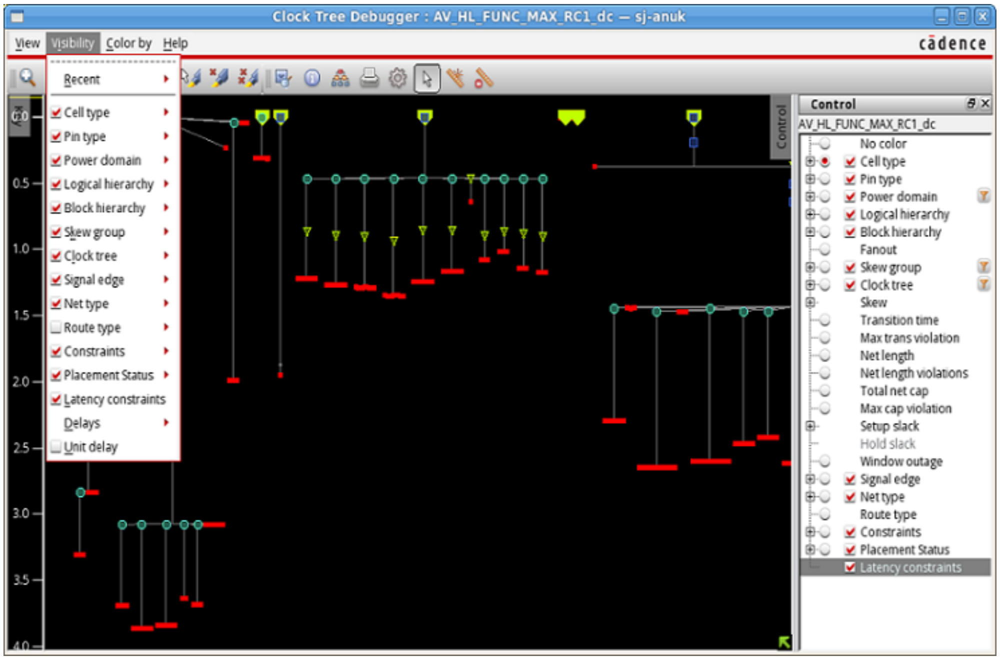
	Select all sinks	Allows you to select clock sinks. When this option is disabled, you can select a single sink. When this option is enabled and if you select one sink under a node (maybe a buffer or a gate), the CTD will select all sinks under that node. This is shown in below image. 
	Enable zoom selected	If you select any clock net or node in the CTD and check this option, it will make the layout window automatically zoom in to that selected object.
	Show connection line	Toggles the display of flight lines in the Clock Tree Viewer. By default, the option is turned ON.
	Zoom scale	Specifies the scale of zoom into the clock tree view. By default, the zoom scale value is 2.
	Rectangular selection mode	Specifies the object that is to be selected in a rectangular selection. You can specify any one of the following: *Instance*: Specifies that instances should be selected *Net*: Specifies that nets should be selected *Both*: Specifies that both instances and nets should be selected. This option is ON by default.

Histogram Preferences	Displays the settings for the histogram.	
	Delay Range, min	The minimum value of the delay range to be displayed for the X-axis.
	Delay Range, max	The maximum value of the delay range to be displayed for the X-axis.
	Bar width	Sets the width of each bar displayed in the histogram. For example, if the range is from 0 to 1000ps, and you want 10 bars, you can specify a width of 100ps to accomodate all 10 bars in the histogram. A smaller width lets you display more bars.
	Min Y Range	Specifies the minimum range for the Y-axis. The histogram automatically scales the vertical axis to accommodate the tallest bar that it is showing. However, you can specify this to make sure that it is at least a certain height to make it easier to compare with other histograms. This is similar to setting a Y range, but if you set a value smaller than the tallest bar, it will be ignored because it does not make sense to chop the bar that it has to display. For example, if you set a value of 1000, but the tallest bar is 487, then the tallest bar will be a little less than half the height of the histogram. If you do not specify one, then that bar will be the whole height of the histogram. So, if you are comparing histograms between different runs, it is easier to view them if they are all showing the same ranges.
	Linear/Logarithmic	Select *Linear* or *Logarithmic* for the type of histogram you want to view.
World View	Displays the settings for the size of the world viewer.	
	Small	Select for a small world viewer window.
	Middle	Select for a medium world viewer window.
	Large	Select for a large world viewer window.

Clock Tree Debugger - Visibility Menu

Use the *Visibility* menu to control the visibility of items in the clock tree view.

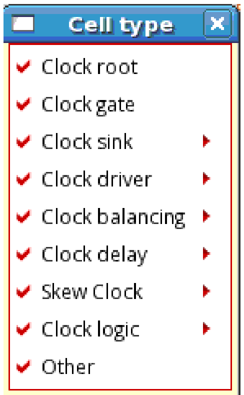
→Choose *Clock – CCOpt Clock Tree Debugger – Visibility.*



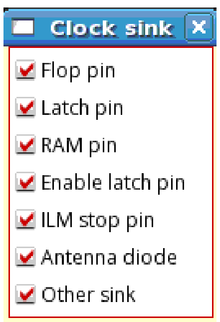
In the *Visibility* menu, for items with both a check box and a submenu, checking the box also checks all items in the submenu and its descendants, and unchecking it unchecks those items. If none of the descendants are checked, the box is also shown as unchecked. In addition, double-clicking a check box selects that check box and unselects all of its peers underneath the same top-level menu item. For example, double-clicking the check box for a single skew group will select that skew group, and unselect all other skew groups, while leaving other menus such as *Cell type* unchanged.

Options	Descriptions
Recent	Allows you to view the the five most recently used items from the *Visibility* menu. Select or deselect the check boxes against each option in the drop-down menu depending on what you want to view. You can choose to view or not view the Cell type, Cell type/Clock root, Cell type/Clock gate, Cell type/clock sink, and Cell type/clock sink/Flop pin, and so on. These are full copies of the original items, and can be checked and unchecked in the same way. The items are also still present in their usual locations.

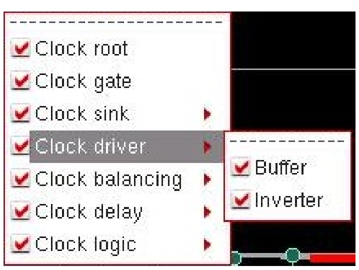
<table>
<tr>
<td>Cell type</td>
<td>
Specifies the visibility of various elements of visualization. Select or deselect the check boxes against each option in the drop-down menu depending on what you want to view. You can choose to view or not view the Clock root, Clock gate, Clock sink, Clock driver, Clock balancing, Clock delay, Clock logic and Other.



For Clock sink, you can choose to view one or more of the following:

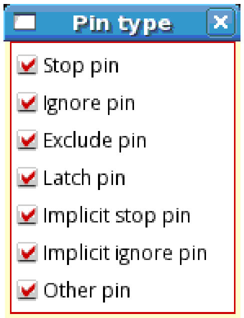
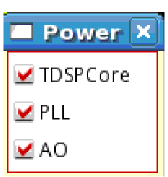


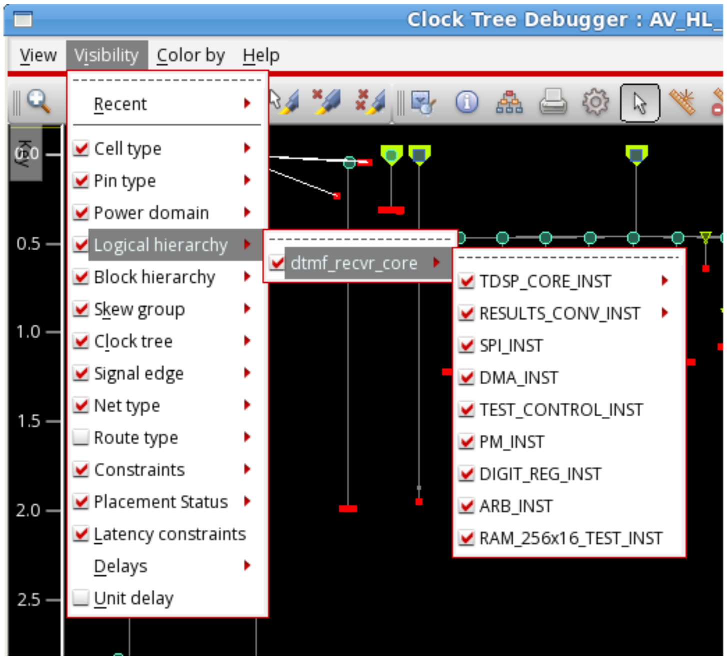
For Clock driver, Clock balancing, and Clock delay you can choose to turn on or off the display of buffers and paired inverters.



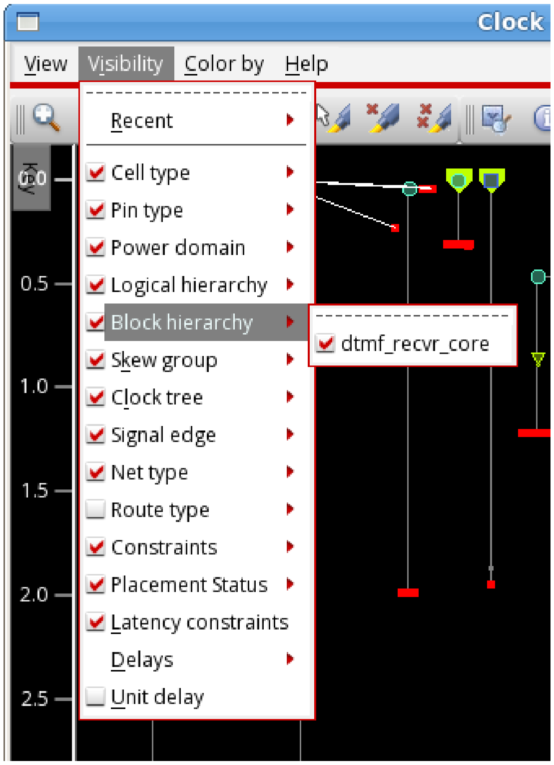
For Clock logic, you can select or deselect any of the following:

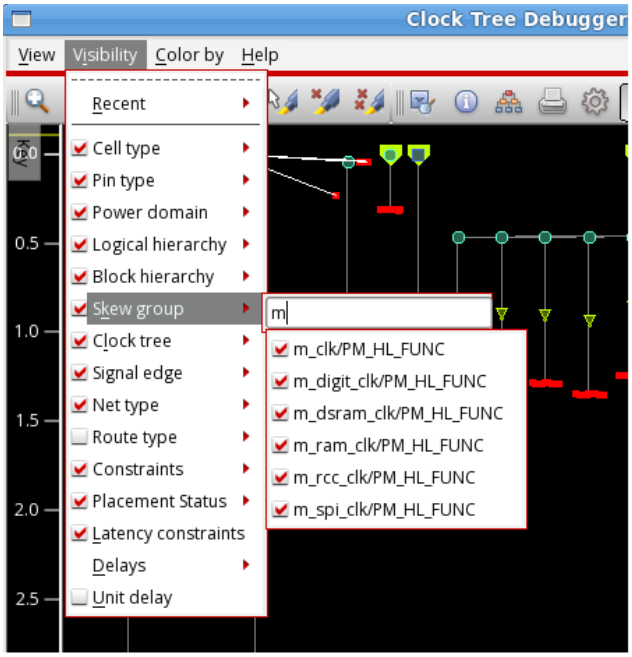
</td>
</tr>
</table>

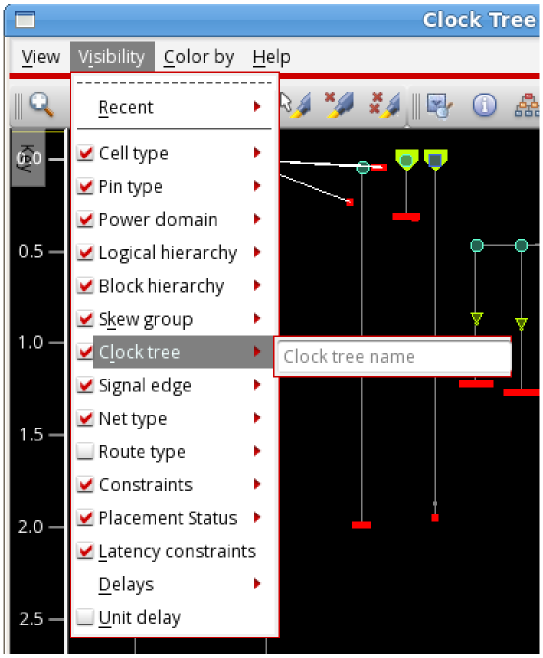
Pin type	Specifies the visibility of different types of pins. Select or deselect the check boxes against each option in the drop-down menu depending on what you want to view. You can choose to view *Stop pin*, *Ignore pin*, *Exclude pin*, *Latch pin*, *Implicit stop pin, Implicit ignore pin*, and *Other pin*. By default, all options are selected.  An implicit stop pin is created on a pin where there is no combinational arc across the cell, but where the pin is marked as being a clock pin in the liberty data or it is listed as having a trigger or a check arc. These pins behave the same as explicit or user-defined stop pins and will be delay balanced against the other sinks in the appropriate skew groups. An implicit ignore pin is created at a cell where there is no combinational arc across the cell, and there is no trigger or check arc present. These pins will not be delay balanced, but will have clock tree design rule violations (DRVs) enforced on the path to them. Each option has a default color. Stop pin – red Ignore pin – green Exclude pin – blue Latch pin – yellow Implicit stop pin – pink Implicit ignore pin – green Other pin – gray When this option is selected, all other objects in the clock tree are displayed as gray.
Power domain	The coloring or visibility of the marker indicates the power domain to which the cell corresponding to the marker belongs. 

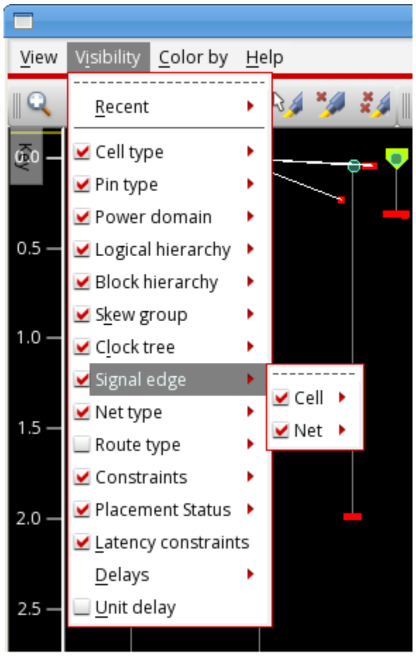
Logical hierarchy	The coloring or visibility of the marker indicates the Verilog module containing the cell corresponding to the marker. 

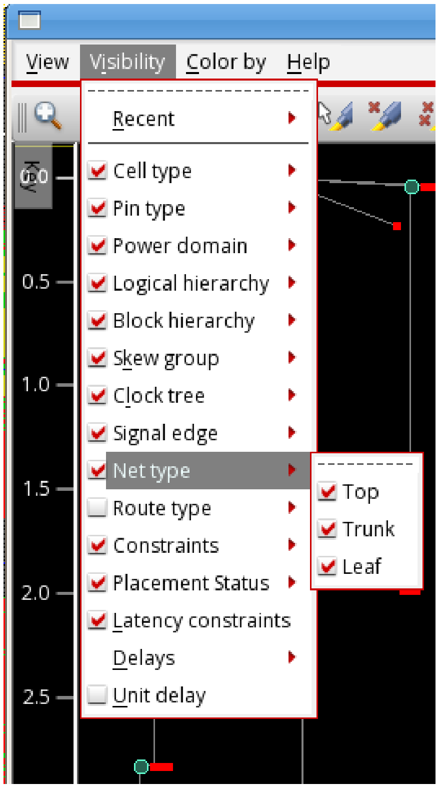
Block hierarchy	The coloring or visibility of the marker indicates modules that represent ILM and other sub-blocks.

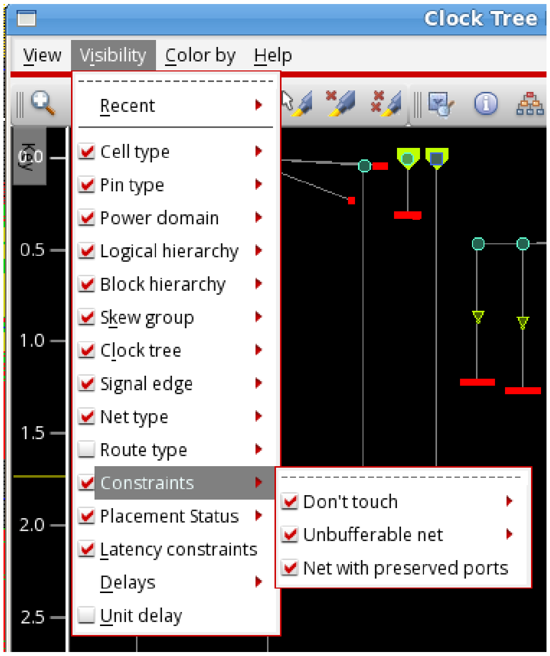


Skew group	Selectively shows, hides, and highlights the specified skew groups in your clock tree view. The list of skew groups is presented as a filtered hierarchy. Type the first few letters of the skew group in the search field and you can see the options that match the letters below in the drop-down menu. Select the skew group you want to view.  If you do not type any letters in the search field, you will get a list of all skew groups in the drop-down menu. Type "No" in the search field to view the *No skew group* option. This option lets you view nets and buffers that do not belong to any skew group. **Note**: Markers may be in more than one skew group at one time.

Clock tree	Selectively shows, hides, and highlights individual clock trees - including generated clocks - in your design. You can select the clock tree from the dropdown list.  **Note**: Markers may be in more than one clock tree at one time.

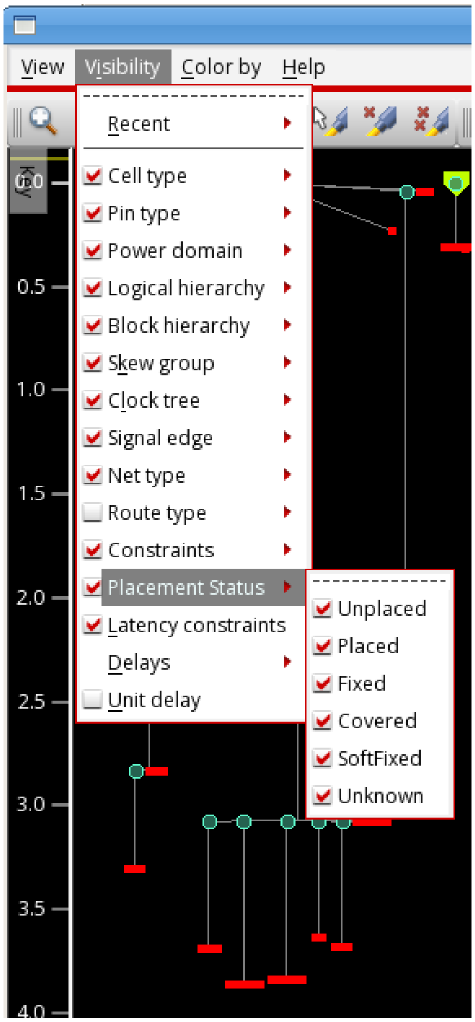
Signal edge	There are two options to view edge coloring, for *Net* and for *Cell*. *Net* subgroup: When edge coloring is enabled, you can view the connectors of the net that are colored to represent the *Rise* or *Fall* edge.  Cell subgroup: When selected, turns on the visibility of the instances that determine which edge is drawn on the output net connector. • *Cell:* this subgroup shows the instances that determine the edge that is drawn on the output net connector. • *Root:* the root cells always force a rise edge • *Non-unate:* the non-unate cells, such as XOR gates, don't deterministically set the output net edge, so it will be represented as rising • *Simple:* the simple cells do not change the edge • *Invert:* the inverting cells have toggled the edge that was input You can remove the clutter of cell subgroup coloring by changing the color or visibility of the Cell sub-item.

Net type	When enabled, visualization shows all the net types; Top, Trunk, and Leaf. Use this option to view a specific net type. 
Route type	When enabled, visualization shows all the route types.
Constraints	Shows the don't touch, unbufferable clock nets, and nets with preserved ports in the Clock Tree Viewer. By default, all options are selected.

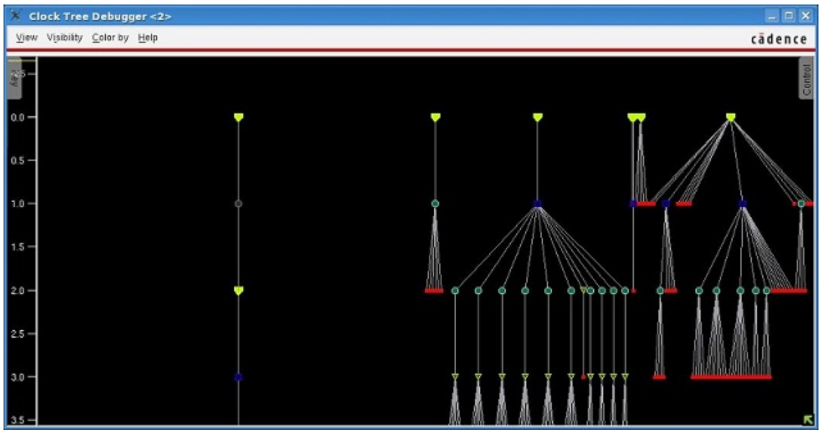


A clock net may be unbufferable or Don't touch for a number of reasons. When you select these options, a list of possible reasons for why the net is unbufferable or don't touch are provided. This is shown below. You can choose to view clock nets based on these. By default, all sub options or reasons are selected.

Placement Status	When selected, highlights instances that are *Unplaced*, *Placed*, *Fixed*, *Covered*, *SoftFixed*, and *Unknown*. This option is also available in the *Control* panel.


View
Visibility
Color by
Help
Recent
Cell type
Pin type
Power domain
Logical hierarchy
Block hierarchy
Skew group
Clock tree
Signal edge
Net type
Route type
Constraints
Placement Status
Latency constraints
Delays
Unit delay
Unplaced
Placed
Fixed
Covered
SoftFixed
Unknown
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0

Latency Constraints	When enabled, visualization shows the target delays that the CCOpt algorithm is aiming for as a range. For a user, these target delays are useful only after running the `ccopt_design` command. This option is also available in the *Control* panel. When this option is selected, hovering the pointer anywhere over the timing window will show the timing window information in the tooltip.
Delays	Specifies the delays that you want to view in the clock tree view. Select or deselect the check boxes against each option in the drop-down menu depending on what you want to view. You can choose to view or not view the Gate delay, Wire delay, Virtual delay, Pin insertion delay, or Gate level delay. • **Gate delay** is the delay within the gate between the clock pin and the output pin. It is shown as a vertical line below the marker. • **Wire delay** is the delay on the wire, between the output pin and the pins it drives. This is shown as diagonal lines from the bottom of the gate delay, or the marker, if the gate delay is not shown, to the markers for each of the fanout. • **Virtual delay** is the delay that CCOpt has scheduled but not yet implemented. It will be present if a trial run has been performed. It is shown as a double vertical line. • **Pin insertion delay** is the additional user-specified delay. It is shown as a dotted line. **Note**: If a component of the delay is unchecked, it is not used to calculate the y-axis coordinates. So markers below that type of delay will appear higher. Markers are shown at the arrival time for the clock signal at the clock pin.

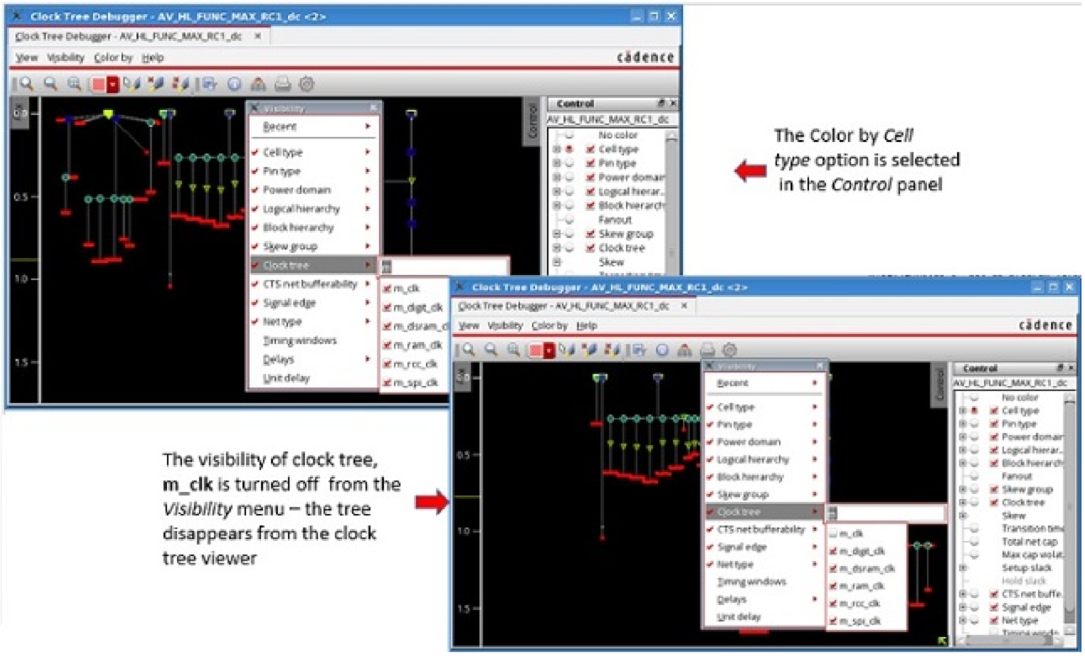
<table>
<tr>
<td>Unit delay</td>
<td>
Unit delay is the delay between the input to the gate and the output.
The unit delay lets you view the depth of clock tree objects easily. This is useful when you have large designs with deep gate-level trees. When debugging clock trees, you can use this view to check how the clock trees are balanced by looking at the depth of the clock trees. When this option is selected, the ruler by the side of the Key panel is updated to display the number of units. All nodes of a tree are aligned by its level. The level starts from 0 and increases by one unit for each level. This is shown in the image below.
Note: When this option is selected, the Timing windows and Delays options are disabled.


Note: You can also open the CTD directly in the unit delay mode by using the <code>-unit_delay</code> parameter of the <code>ctd_win</code> command. This can be done even for unplaced designs without running CTS. For details, see the <code>ctd_win</code> command documentation in the Innovus Text Command Reference.
</td>
</tr>
</table>

Clock Tree Debugger - Color by Menu

Use the *Visibility* menu to control the coloring of the various elements in the Clock Tree Viewer. Colorings are mutually exclusive – selecting one deselects all others. The items for enumerations also have a submenu to allow the color used for individual categories to be customized.

Additionally, the visibility options in the CTD are independent of the coloring options. You can choose to color an item, say Cell type, from the Color by menu or the Control panel, while at the same time hide the skew groups by unchecking the Skew group option in the Visibility menu or by unchecking the option just before the items of interest in the Control panel. An example is shown in the below image.



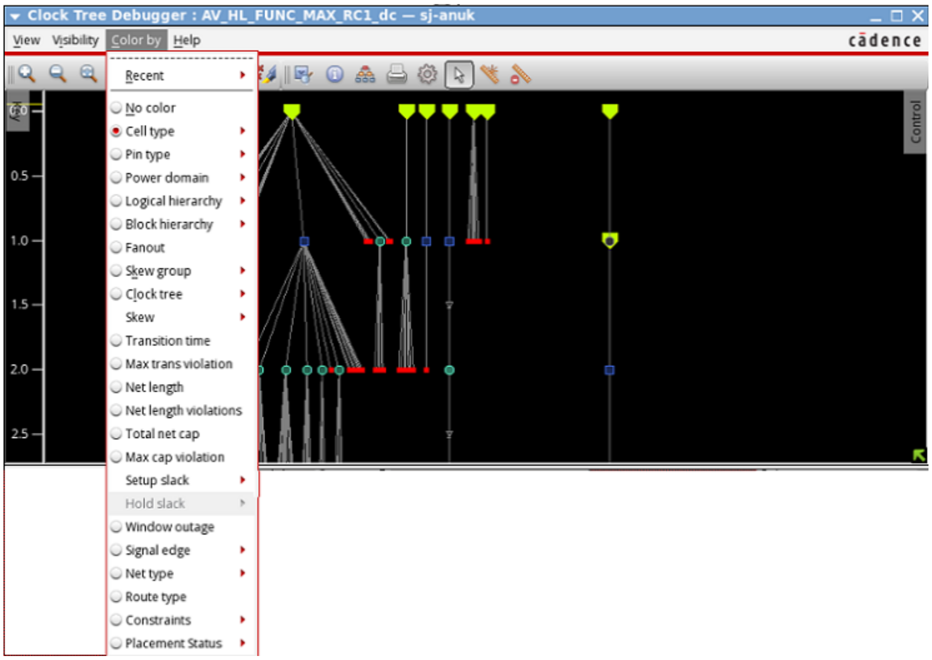
Types of Colorings

Three types of colorings are supported:

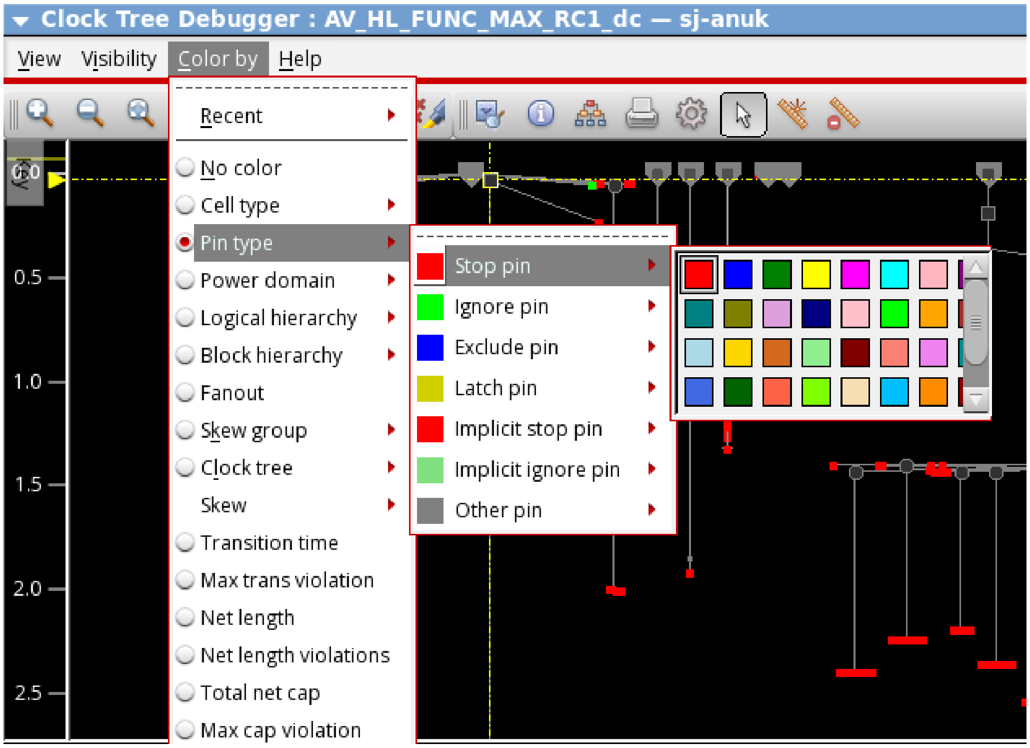
- **Enumerations**, which partition the objects in the visualization into a number of non-overlapping categories. For example, *Cell type* categorizes cells into various types. Each category in an enumeration, for example *Clock gate* within *Cell type*, has a distinct color.
- **Continuous color scales**, which color each applicable element according to the value of some numerical value. For example, *Transition time*.
- **Collections of subsets of objects** in the design, which color objects within the subset in a single color. For example, a skew group is one subset.

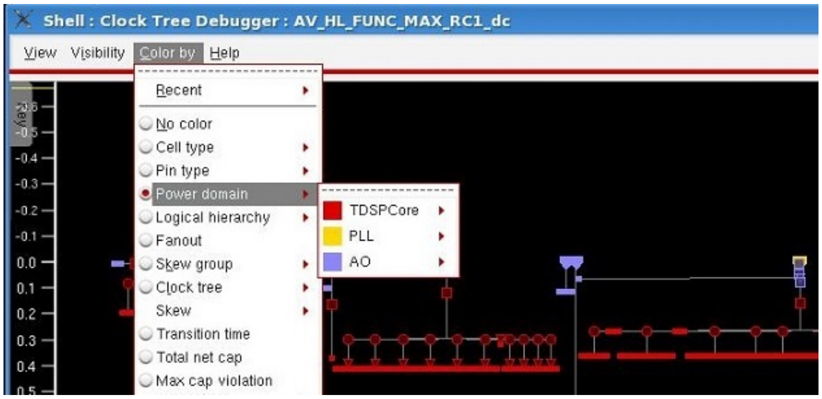
Color by Menu Options

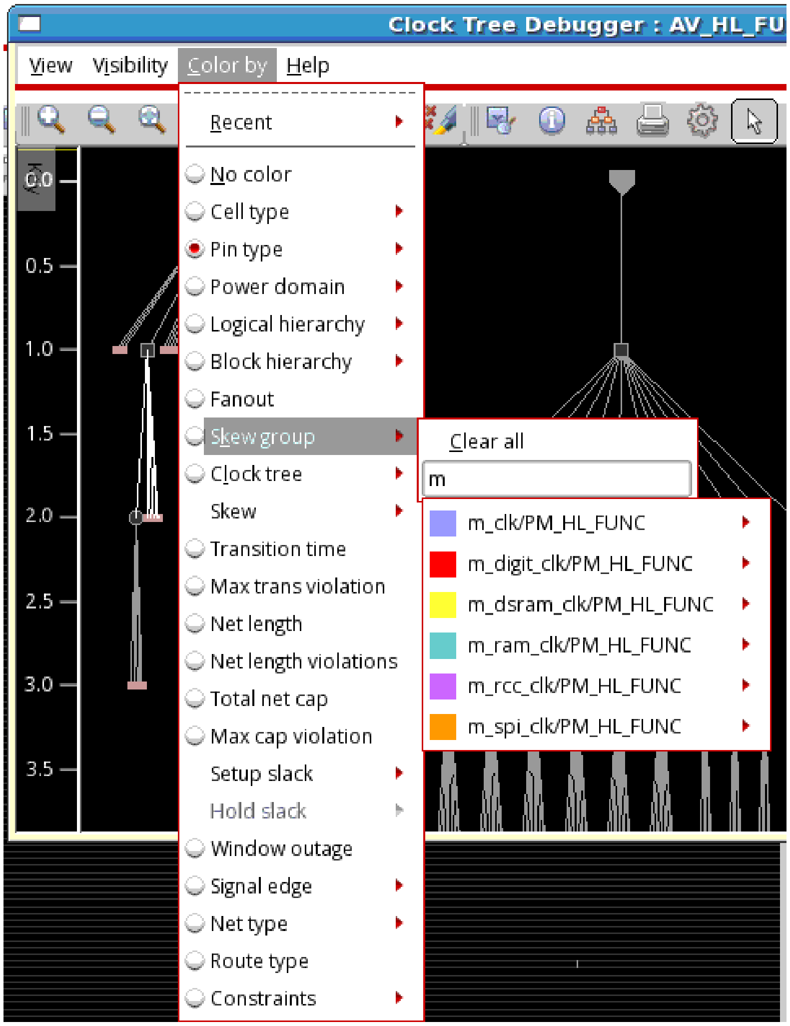
Choose *Clock – CCOpt Clock Tree Debugger – Color by.*



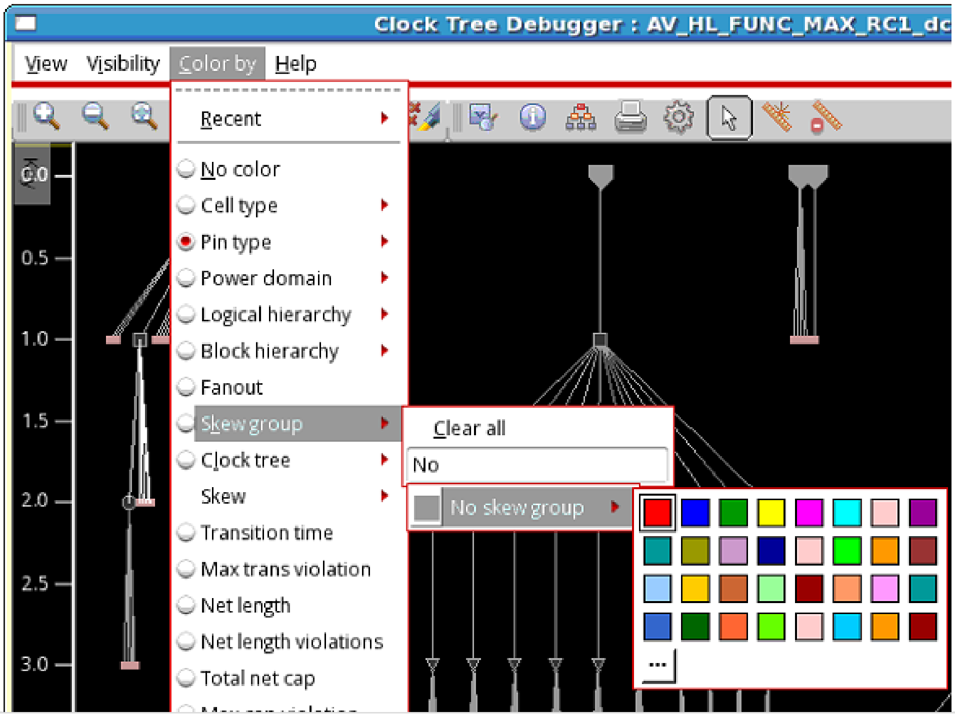
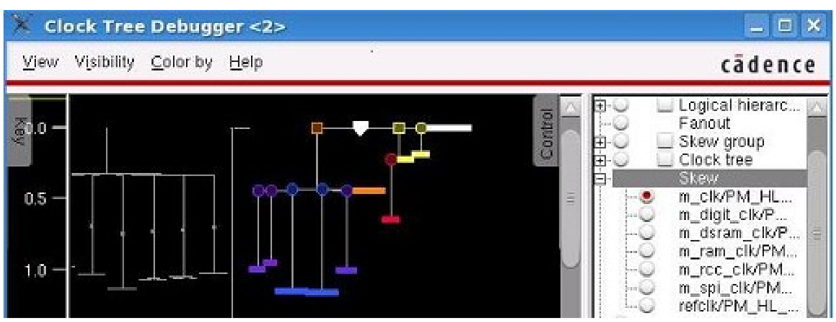
Options	Descriptions
Recent	Shows a list of the five most recently used items from the *Color by* menu. Select the radio button for each option to view the most recently done coloring for that option.
No color	Removes all colors from the display.
Cell type	Specifies the colors for different cell types. You can choose colors based on your preference form the color options available in the color picker.

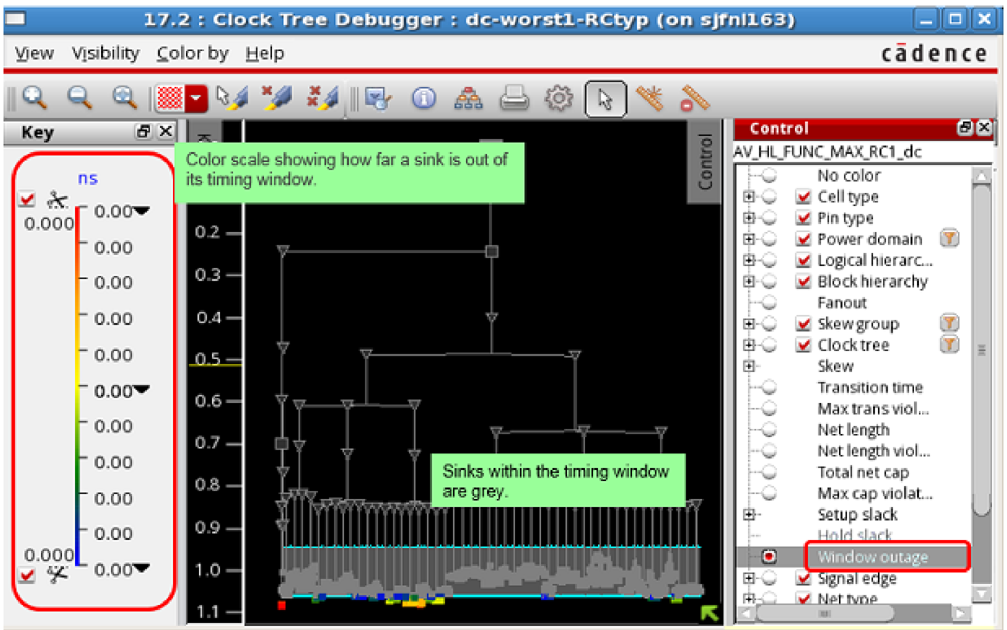
Pin type	Specifies the colors for different pin types. If this option is selected, the rest of clock tree objects are displayed as gray, and the CTS pins, such as ignore pins and stop pins are shown in the colors defined in the control panel. You can choose colors based on your preference form the color options available in the color picker. 

Power Domain	Specifies the colors for different power domains of the clock tree. You can choose colors based on your preference form the color options available in the color picker. 
Logical hierarchy	Specifies the colors for the different hierarchy levels in the clock tree view.
Fanout	Colors each cell based on its fanout, which is the number of cells it drives.
Skew group	Specifies the colors for the different skew groups in the clock tree view. The list of skew groups is presented as a filtered hierarchy. You can select the skew group from the drop-down list.



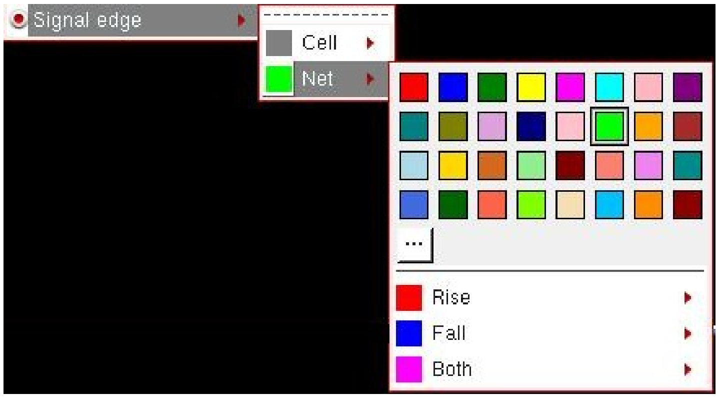
If you do not type any letters in the search field, you will get a list of all skew groups in the drop-down menu. Type "No" in the search field to view the *No skew group* option. This option lets you specify a color for nets and buffers that do not belong to any skew group. You can choose colors based on your preference form the color options available in the color picker.

	
Clock tree	Specifies the color for the clock tree. You can *Clear all* to clear the color selections for all clock trees. You can select the clock tree from the dropdown list.
Skew	Shows the skew group specified in the drop-down menu. The list of skew groups is presented as a filtered hierarchy. Select the radio button for each skew group to view it in the clock tree view. When you select the radio button to view the colors for the specific skew group using this option, the *Skew group* option is deselected. 
Transition time	Shows the transition time in the clock tree view using color.
Max trans violation	Colors each node in the clock tree based on the maximum transition violation. **Note:** The options - *Transition time*, *Total net cap*, and *Max trans violation* - are mutually exclusive.
Net length	Shows the net length in the clock tree view using color.
Net length violations	Shows the net length violations using color.

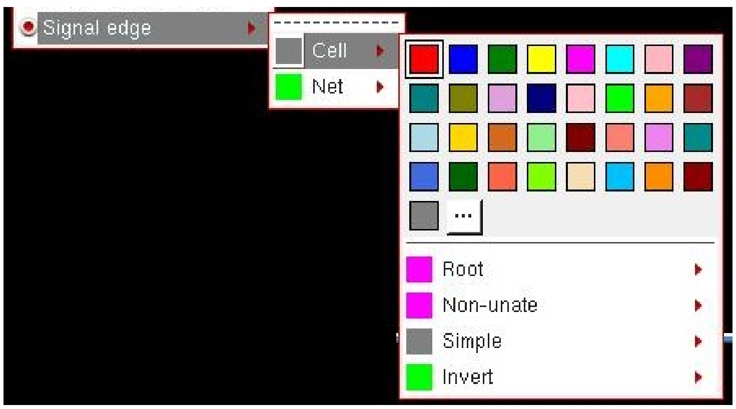
Total net cap	Shows the total net capacitance in the clock tree view using color.
Max cap violation	Colors each node in the clock tree based on the maximum capacitance violation.
Setup slack	Colors nodes by setup slack, as measured by the Common Timing Engine or the CTE.
Hold slack	Colors nodes by hold slack, as measured by the CTE.
Window outage	This is a colour scale that shows how far a sink is out of its timing window. A sink within its timing window is grey. 

<table>
<tr>
<td>Signal edge</td>
<td>

When selected, the connectors representing the net are colored to represent the Rise or Fall edge or Both. You can change the color from the color picker provided against each option.



The Cell subgroup specifies the colors of instances that determine the edge that is drawn on the output net connector.

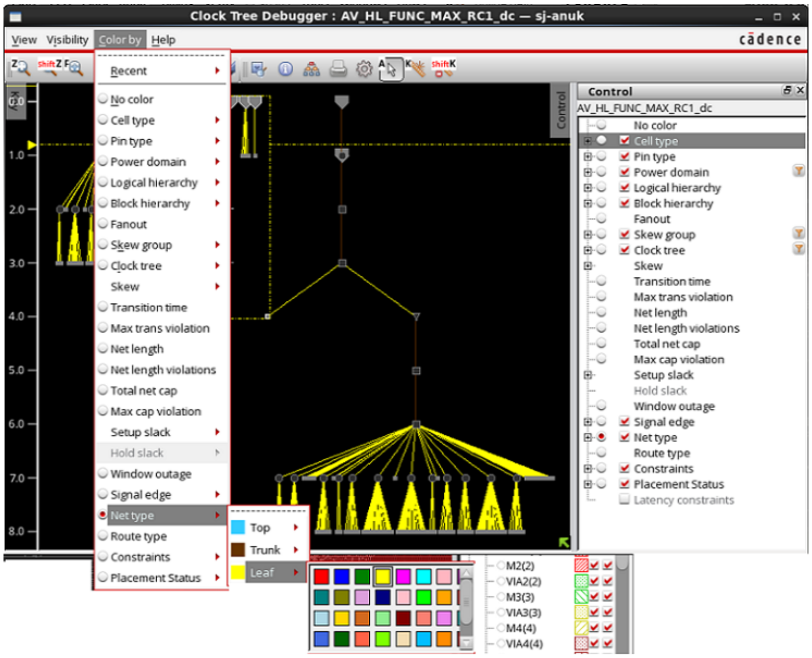


- *Root:* specifies the color of root cells that always force a rise edge
- *Non-unate:* specifies the color for the non-unate cells, such as XOR gates
- *Simple:* specifies the color for the simple cells
- *Invert:* specifies the color for the inverting cells, which are cells that have toggled the edge that was input

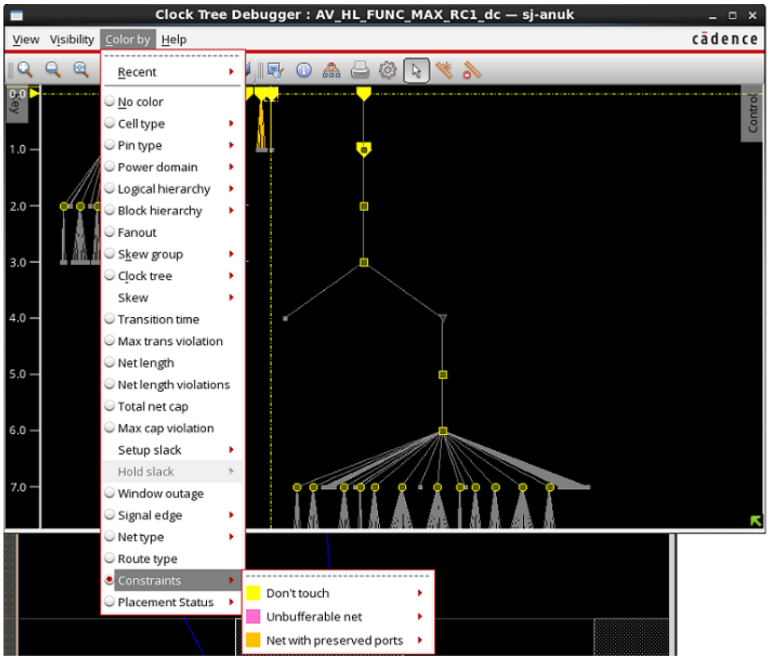
If the visibility of any of the above options is turned off, the specified coloring will only be visible once the option visibility is enabled from the *Visibility* menu.

</td>
</tr>
</table>

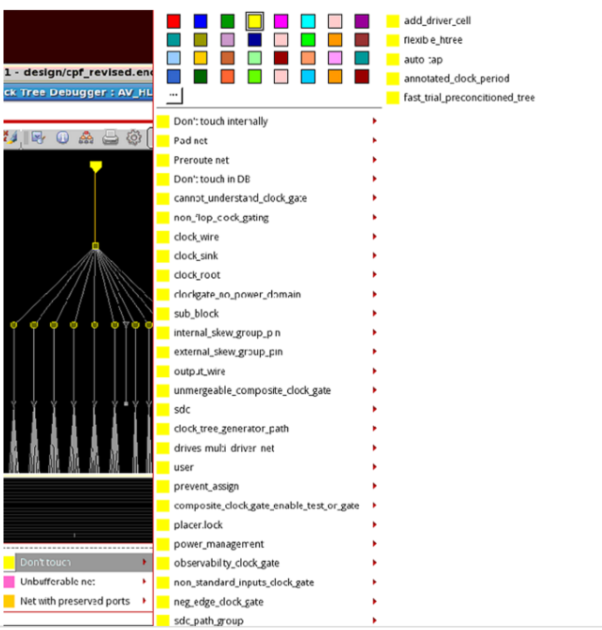
<table>
<tr><td>Net type</td><td>Specifies the color for net types. Use this option to specify colors for Top, Trunk, and Leaf net types.

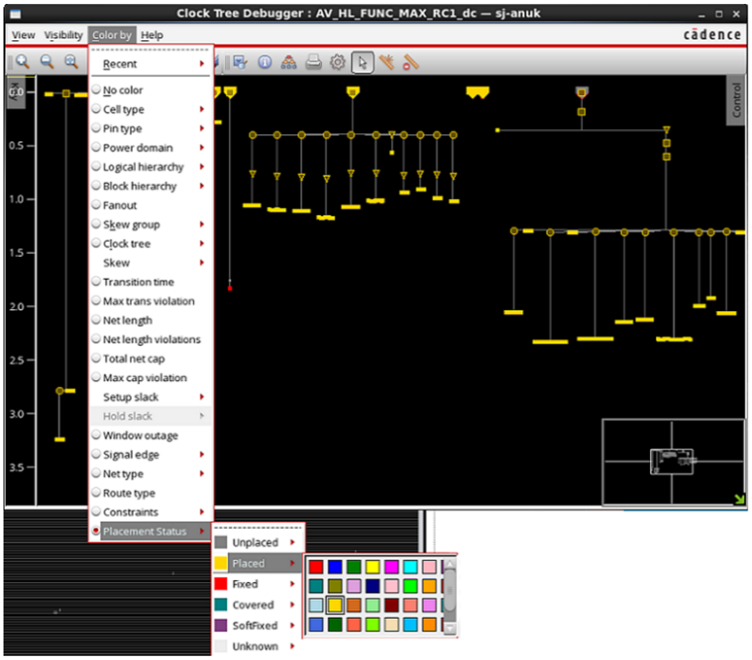


</td></tr>
<tr><td>Constraints</td><td>Specifies the color of don't touch nets, unbufferable nets, and nets with preserved ports. By default, the don't touch nets are colored red while the unbufferable nets are colored pink and the nets with preserved ports are colored yellow. You can change the highlight color from the color options available in the color picker as per your preference .For example, in the image below, the don't touch nets are highlighted in yellow.</td></tr>
</table>



For the don't touch and unbufferable clock nets, you can choose to highlight nets based on the reasons why they are don't touch or unbufferable. The list of reasons is provided in the drop-down menu of these options. This is shown below. You can change of the color of the reasons from the color picker provided against each reason. By default, a clock net may be don't touch or unbufferable for a number of reasons, but it is colored with the first applicable reason. However, if the visibility of that reason is disabled, then it will be colored with the next applicable reason.



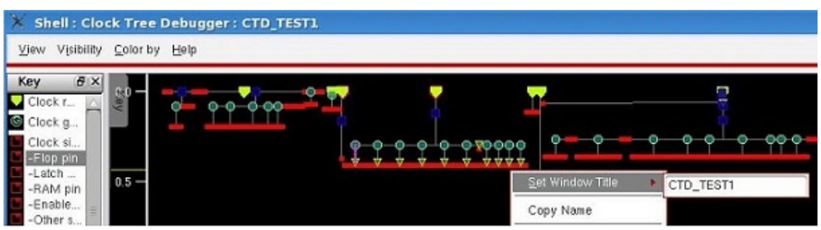
Placement Status	When selected, uses different colorings to highlight instances that are *Unplaced*, *Placed*, *Fixed*, *Covered*, *SoftFixed*, and *Unknown*. 

Context Menu of Clock Tree Debugger

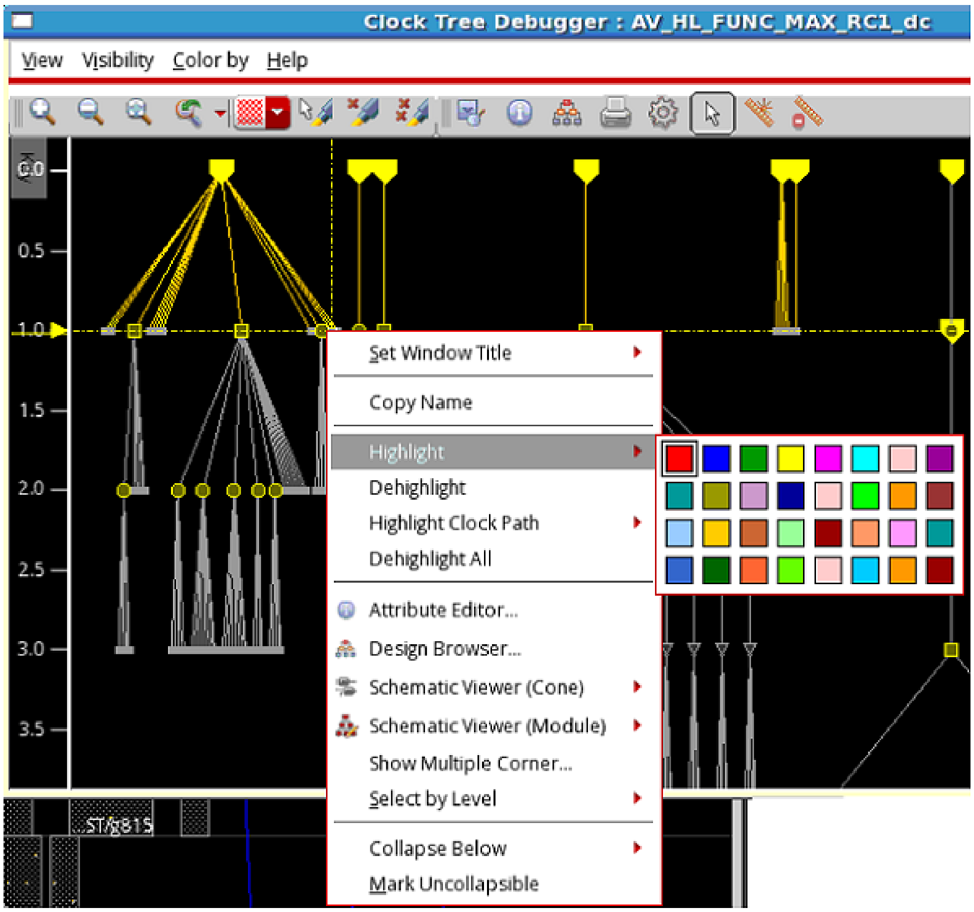
The context menu of the *Clock Tree Debugger* provides the following functionalities, which you can access when you right-click any marker or line in the clock tree view.

1. Set Window Title
2. Copy Name
3. Highlight
4. Dehighlight
5. Highlight Clock Path
6. Dehighlight All
7. Attribute Editor
8. Design Browser

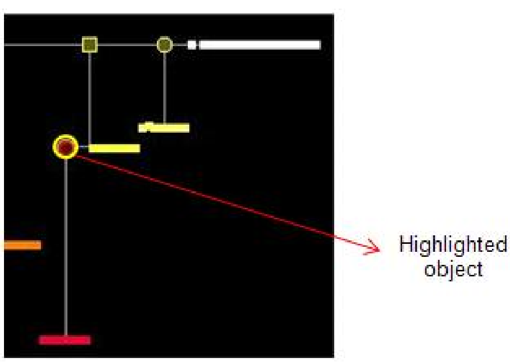
9. Schematic Viewer (Cone)
10. Schematic Viewer (Module)
11. Show Multiple Corner
12. select
13. Collapse Below
14. Collapse subtree
15. Abstract this node
16. Unabstract this node
17. Expand all subtrees
18. Expand all sinks
19. Select transitive sink fanout
20. Select subtree
21. Mark Uncollapsible

Options	Descriptions
Set Window Title	Specifies the window title for the CTD session. After you type the title and press enter, the new title appears in the top bar of the CTD.  You can also use the following commands to retrieve and set the title of the CTD windows: • `get_ctd_win_titlegui_ctd_get_window_id` • `set_ctd_win_title`
Copy Name	Copies the name of the selected object to the clipboard.

<table>
<tr>
<td>Highlight</td>
<td>Highlights the selected markers or lines. The highlighting functionality is different from the coloring options described above. When showing highlights in the skew clock tree, the coloring is shown as a halo, rendered behind the highlighted objects but in front of non-highlighted objects. The halo is created by rendering the highlighted objects with a thick stroke, for example five pixels, to give a two-pixel border, and then rendering them again using a normal stroke. This allows highlighting to be viewed concurrently with other colorings. If multiple highlights cover the same objects, the colors in question will be blended for the objects where the highlights overlap. You can change the highlight color from the color options available in the color picker as per your preference.



The image below shows the highlighted object. A yellow border is seen around the highlighted object.

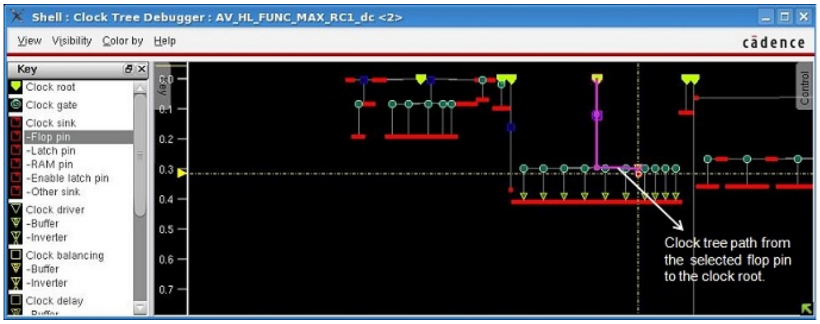


</td>
</tr>
<tr>
<td>Dehighlight</td>
<td>Dehighlights the selected highlighted object.</td>
</tr>
</table>

Highlight Clock Path

Highlights the complete clock tree path from the selected clock tree object, which may be a flip flop, a clock gate, a clock buffer or an inverter, to the clock root in the Clock Tree Viewer. In addition, if cross-probing is enabled, then the physical layout window of the software will also either highlight or show flight lines for that full clock tree path. If there are wires, the layout will highlight the path, otherwise, it will show only flight lines.

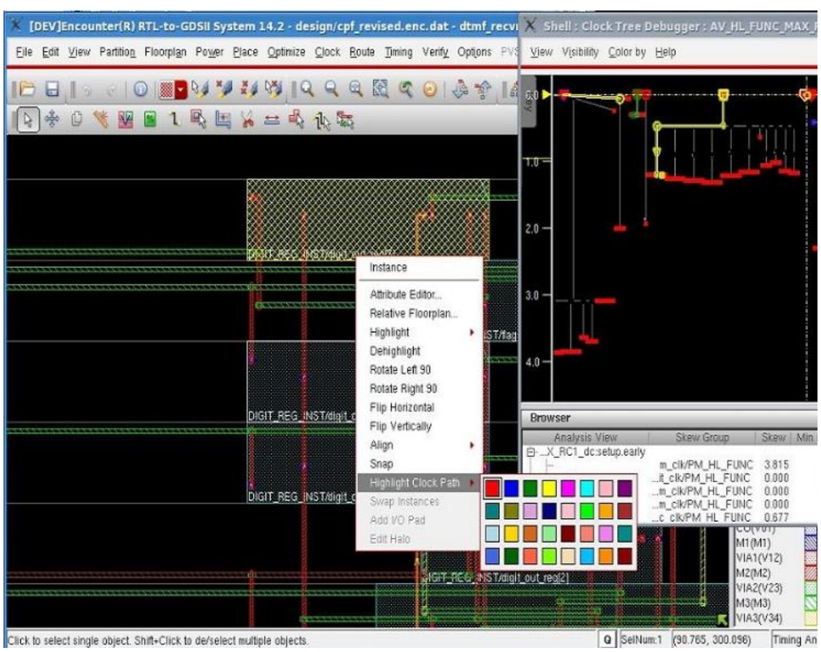
You can change the highlight color from the color options available in the color picker as per your preference. The image below shows the clock tree path from the selected flop pin to the clock root. The path is highlighted in pink.

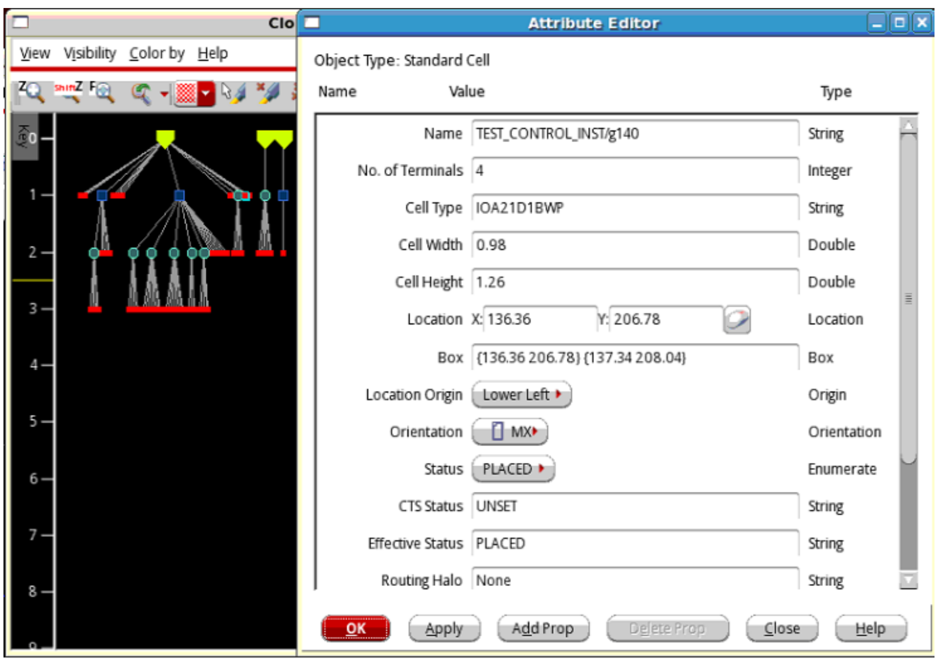


This option only shows up in the context menu when you right-click any clock tree object. It does not show up when you right-click either a clock net or a blank area of the Clock Tree Viewer. For details, see the "Highlight Clock Tree Path" section.

You can also highlight the clock tree paths in the following ways:

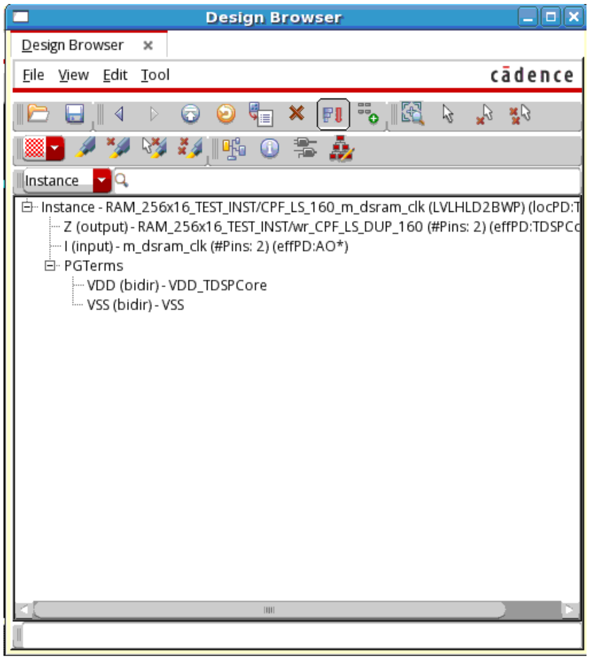
- Use the `ctd_trace` command to highlight clock tree paths in the specified color.
- Use the *Highlight Clock Path* option from the context menu in the layout window. You can select an instance in the layout window. Right-click to view the context menu. In this menu, select *Highlight Clock Path* and select the color in which you want to highlight the clock path from the color picker. This will highlight the clock path from the clock root to that instance if it is in the clock tree. This is shown below.



<table>
<tr><td></td><td></td></tr>
<tr><td>Dehighlight All</td><td>Removes the highlights from all markers or lines.</td></tr>
<tr><td>Attribute Editor</td><td>Shows the properties of the selected object in the Attribute Editor.


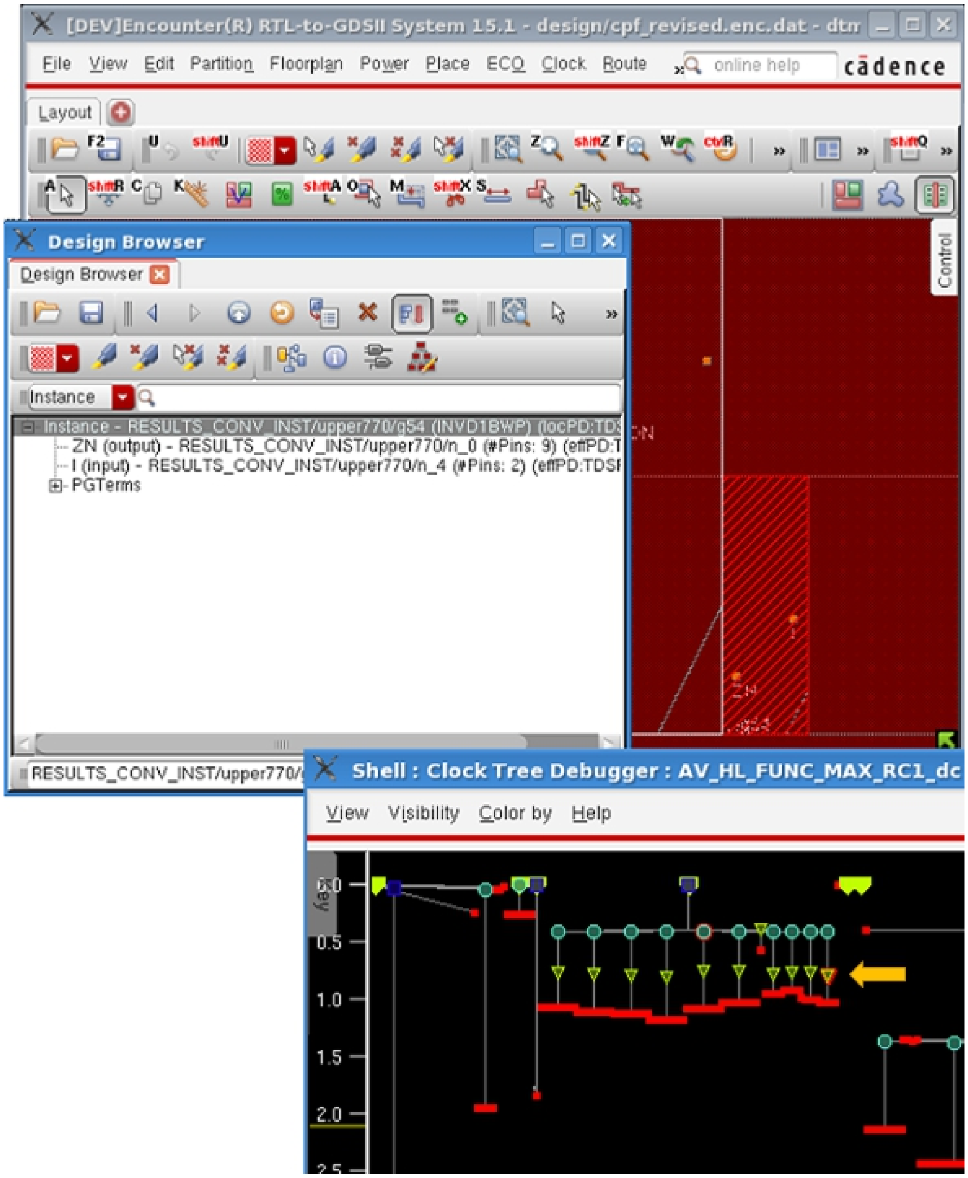
For more information, see the Attribute Editor section in the Edit Menu chapter.</td></tr>
<tr><td>Design Browser</td><td>Use the Design Browser to highlight specific modules, instances, or nets in the design display area. Select an object in the CTD and click on Design Browser in the context menu. The Design Browser window shown below opens.</td></tr>
</table>

Design Browser Window



You can use the widgets in the Design Browser to open forms, to navigate through displays, and perform actions. For details of the Design Browser and the available tool widgets, see the "Design Browser " section in the Tools Menu chapter.

The image below shows the details of an object selected in the CTD, in the Design Browser. The object is highlighted in the display area.


[DEV]Encounter(R) RTL-to-GDSII System 15.1 - design/cpf_revised.enc.dat - dtm
File View Edit Partition Floorplan Power Place ECO Clock Route
online help
cādence
Layout
Design Browser
Design Browser
Instance
Instance - RESULTS_CONV_INST/upper770/g54 (INVD1BWP) (locPD:TD
ZN (output) - RESULTS_CONV_INST/upper770/n_0 (#Pins: 9) (effPD:T
I (input) - RESULTS_CONV_INST/upper770/n_4 (#Pins: 2) (effPD:TDSI
PGTerms
RESULTS_CONV_INST/upper770/
Control
Shell : Clock Tree Debugger : AV_HL_FUNC_MAX_RC1_dc
View Visibility Color by Help
0.5
1.0
1.5
2.0

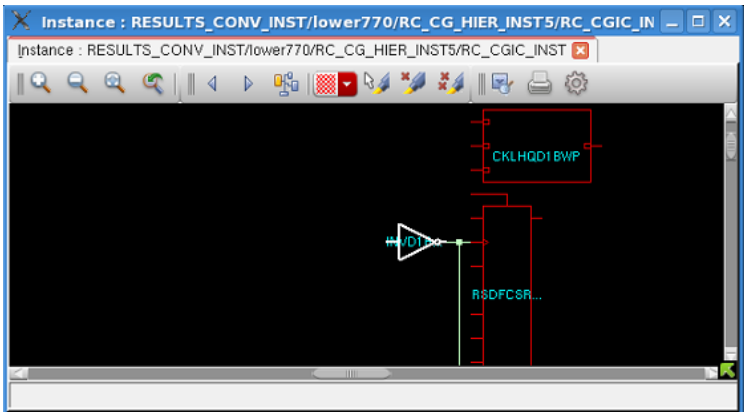
Schematic

Viewer (Cone)

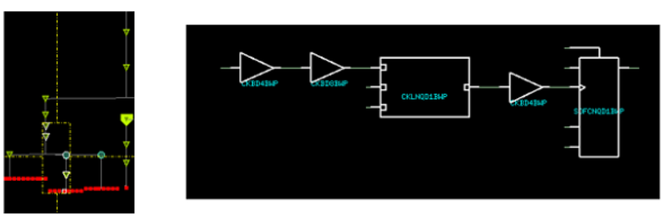
Shows instance-based schematic of the selected objects in the *Schematic Viewer*. You can choose from the following submenus:

- *In Main*....: opens the schematic view of the objects within the main window of the Schematic Viewer. For this, select multiple objects in the CTD GUI and then select *Schematic Viewer (Cone) > In Main*.
- *In New*...opens the schematic view of the selected objects in a new Schematic Viewer window even if a window is already open.
- *Append*: appends the schematic view of the selected objects in an existing open Schematic Viewer window of another object.

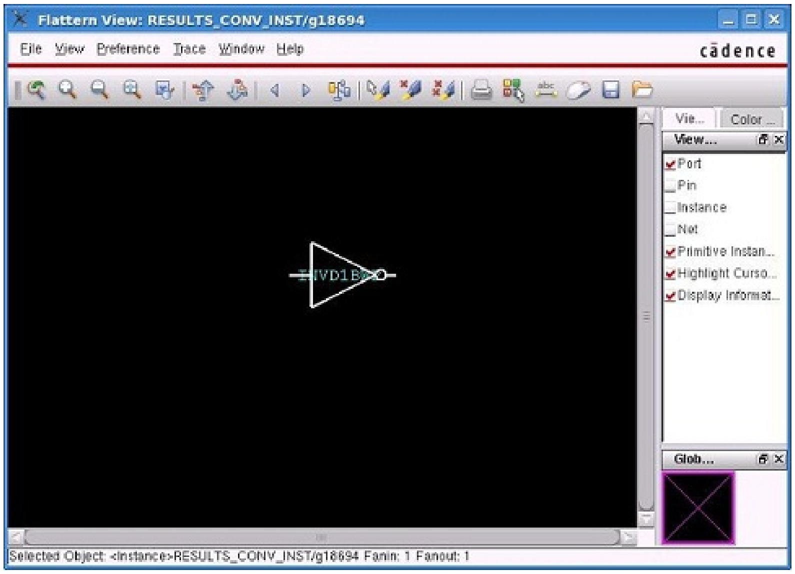
Schematic Viewer - In Main



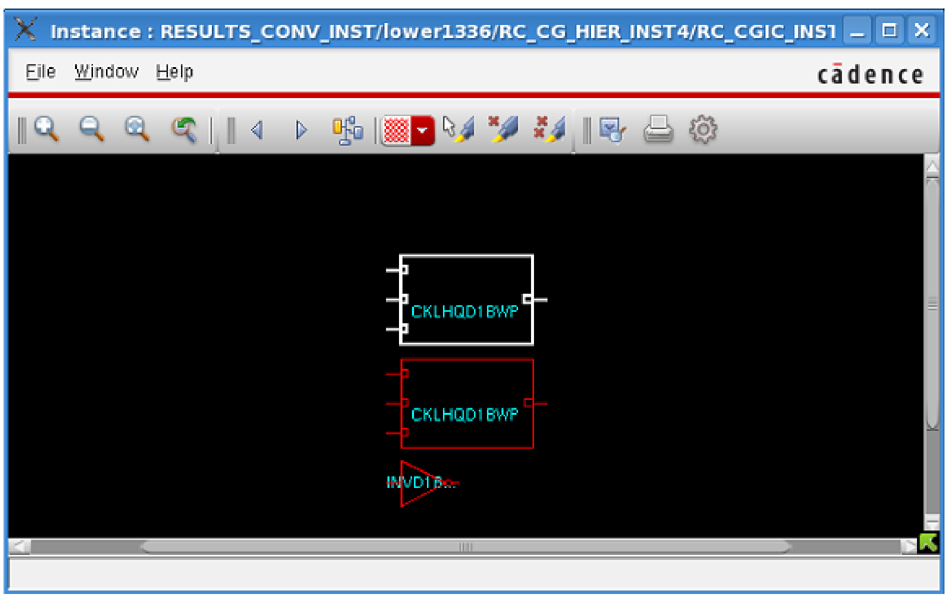
Viewing Multiple Objects in the Same Schematic Viewer - In Main



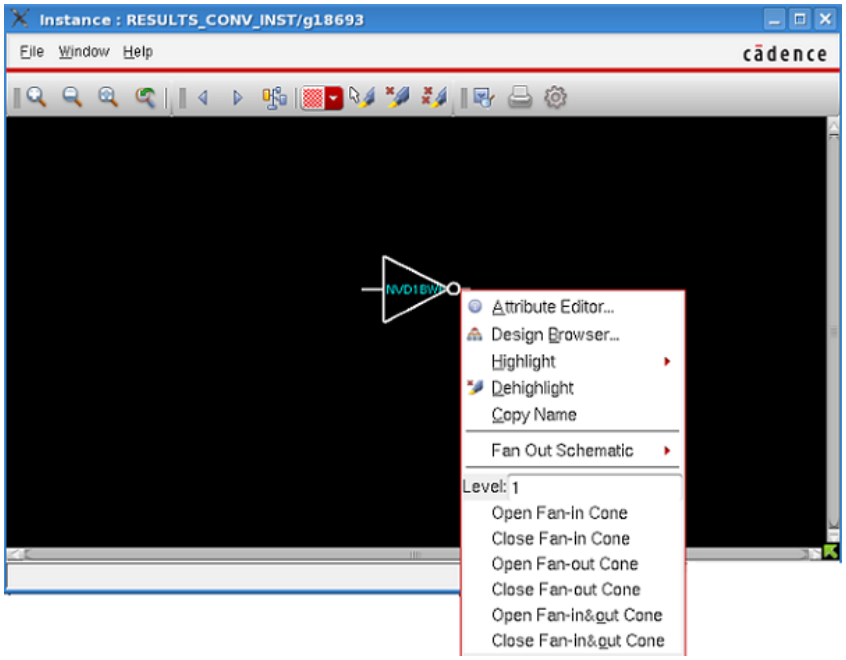
Schematic Viewer - In New



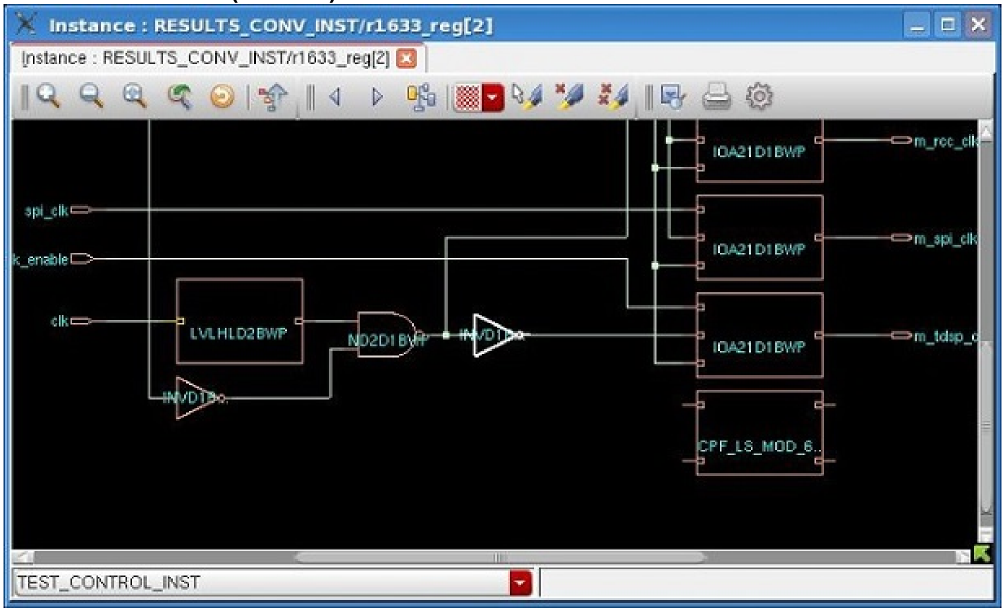
Schematic Viewer - Append

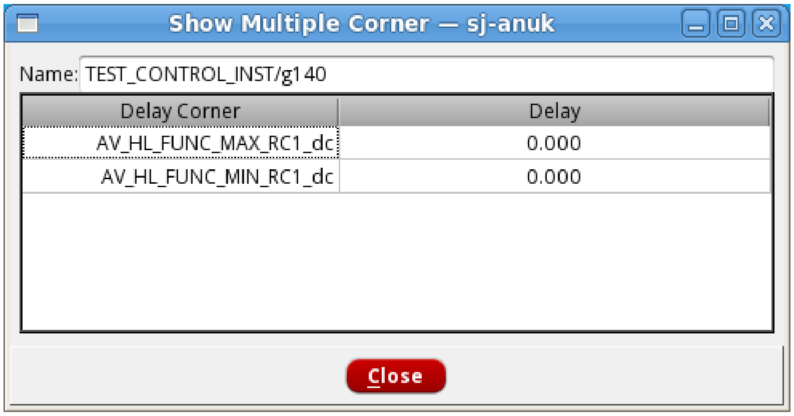


For any instance open in the Schematic Viewer window, you can customize the view using the options available in the context menu.



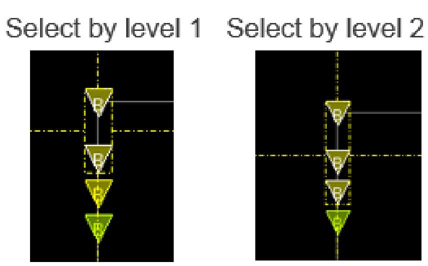
For more information about the options available in the Schematic Viewer and detailed descriptions of the different components of the viewer, see the "Schematic Viewer" section in the Tools Menu chapter.

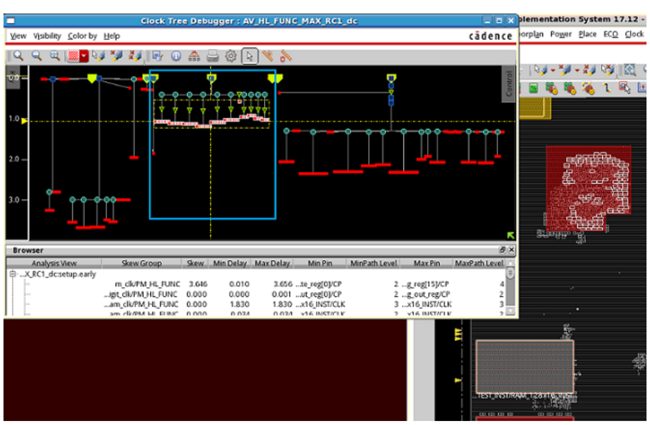
Schematic Viewer (Module)	Shows hierarchical-based schematic of the selected objects in the *Schematic Viewer*. You can choose from the following submenus: • *In Main*....: opens the schematic view of the objects within the main window of the Schematic Viewer. • *In New*...opens the schematic view of the selected objects in a new Schematic Viewer window even if a window is already open. **Schematic Viewer (Module) - In Main** 

<table>
<tr>
<td>Show Multiple Corner...</td>
<td>
Shows the delay values for multiple corners for the selected object in the Show Multiple Corner form. The form lists the name of the object and the delay values for all the corners. This lets you view delays for different corners at the same time.


</td>
</tr>
<tr>
<td>Select by Level</td>
<td>
Provides options for selction. THe following options are available:

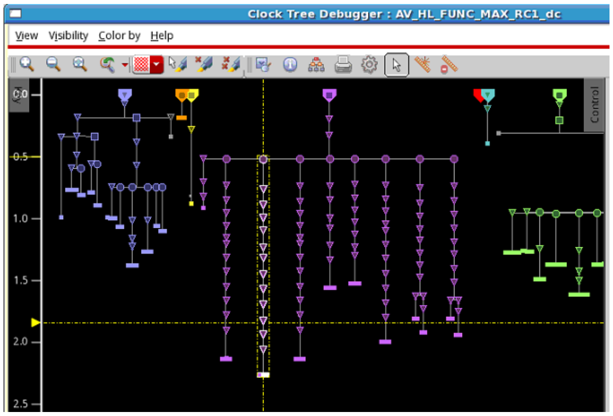
Select by Level
Select transitive sink fanout
Select subtree

The Select by Level option lets you select clock trees from one depth level up to another depth level. The default level is 1. This is shown below.


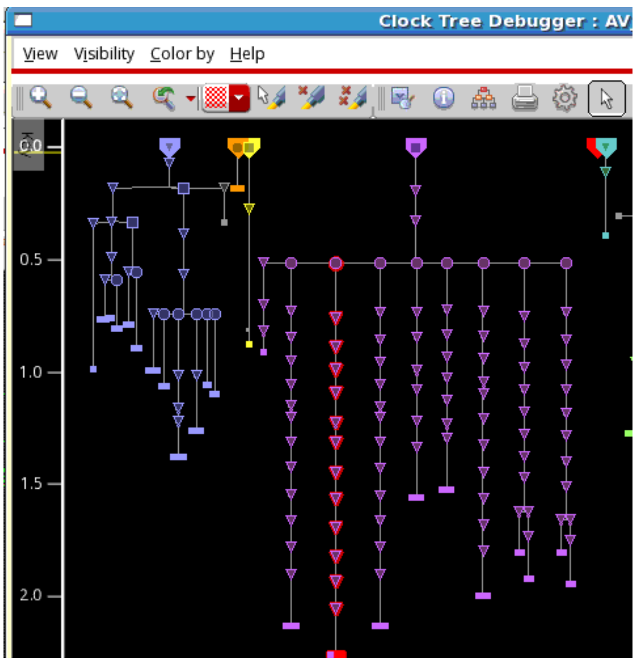
The Select transitive sink fanout option is available when you right-click objects other than sinks. It selects the transitive sink fanouts for the selected object.


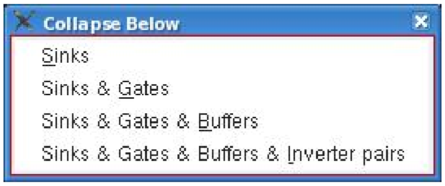
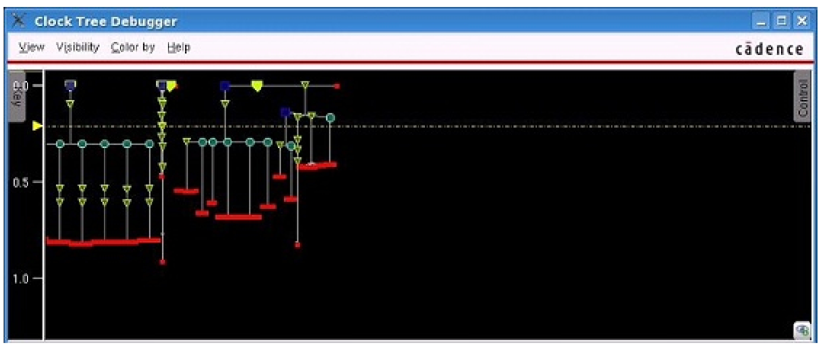
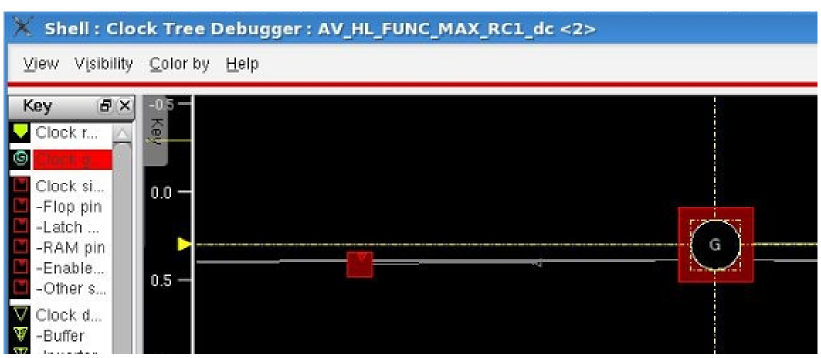
</td>
</tr>
</table>

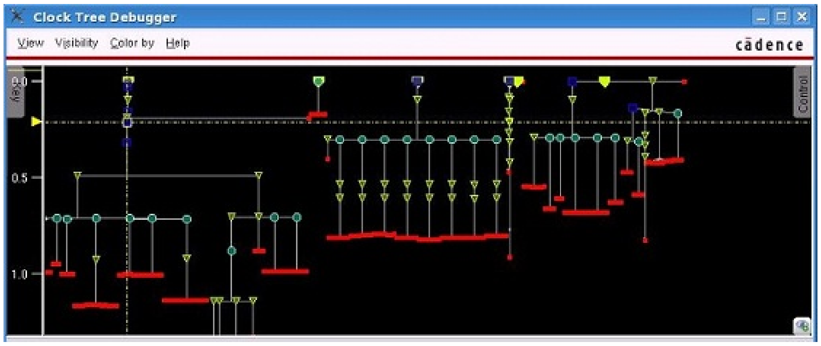
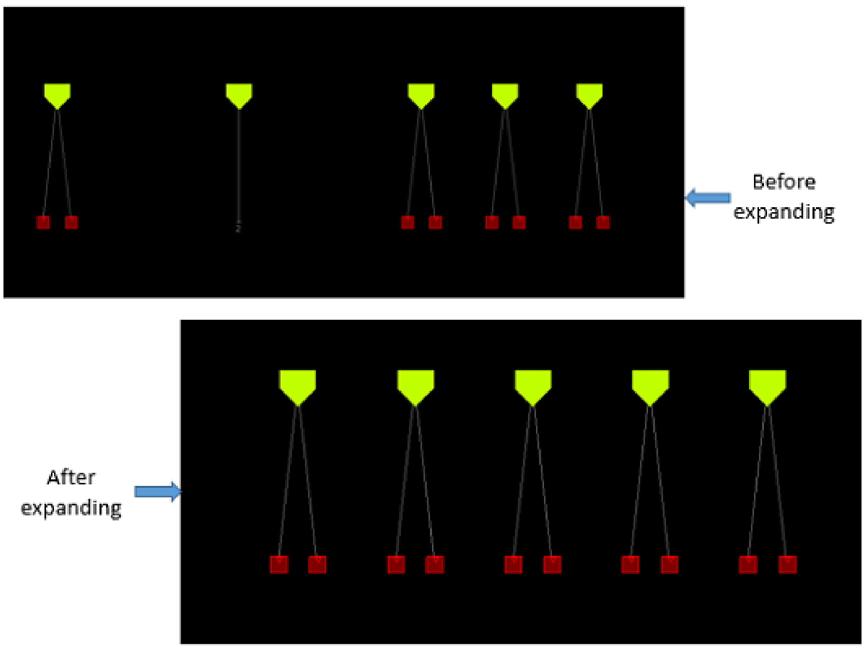
The *Select subtree* option selects everything under the selected node.



To highlight the whole subtree, you can select it with this option, then use the existing *Highlight* option in the menu to select a color to highlight your selection. In the image below, all the nodes of the selected subtree are highlighted in red color.



Collapse Below	Provides options to collapse subtrees with clock gates and flops. Similar options are available in the *View* menu - *Simplify* submenu - *Collapse* option.  *Sinks* - collapses subtrees with clusters of sinks *Sinks & Gates* - collapses subtrees with clusters of gates directly driving sinks *Sinks & Gates & Buffers* - collapses subtrees with clusters of gates driving sinks connected by buffers *Sinks & Gates & Buffers & Inverter pairs* - collapses subtrees with clusters of gates driving sinks connected by buffers or inverters where the edge is not changed
Collapse subtree	Collapses the subtree.  ⓘ You can also double-click to expand or collapse subtrees of any node of the clock tree.
Abstract this node	Abstracts the selected node.  This option only appears in the context menu if you select buffers, inverters, or clock gates. It does not appear if you select clock root.
Unabstract this node	Unabstracts the selected node.

Expand all subtrees	Expands all the collapsed subtrees. 
Expand all sinks	Expands all the collapsed sinks. This is shown in the image below. 
Mark Uncollapsible	Marks the selected nodes as uncollapsible. If you mark a node as uncollapsible, then when the parent node is collapsed, all the subnodes below that node will not be collapsed.

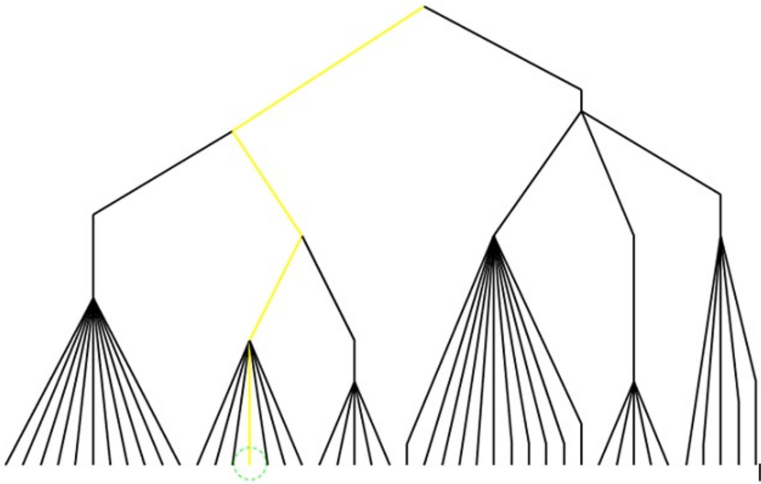
Highlight Clock Tree Path

The *Highlight Clock Path* option in the context menu of the Clock Tree Viewer highlights the complete clock tree path from the selected clock tree object to the clock root in the Clock Tree Viewer. When you select this option, the CTD traces back to find the path from the clock root to the selected node and then highlights the path in the Clock Tree Viewer. Two scenarios are detailed below.

- Use the `ctd_trace` command to highlight clock tree paths in the specified color.

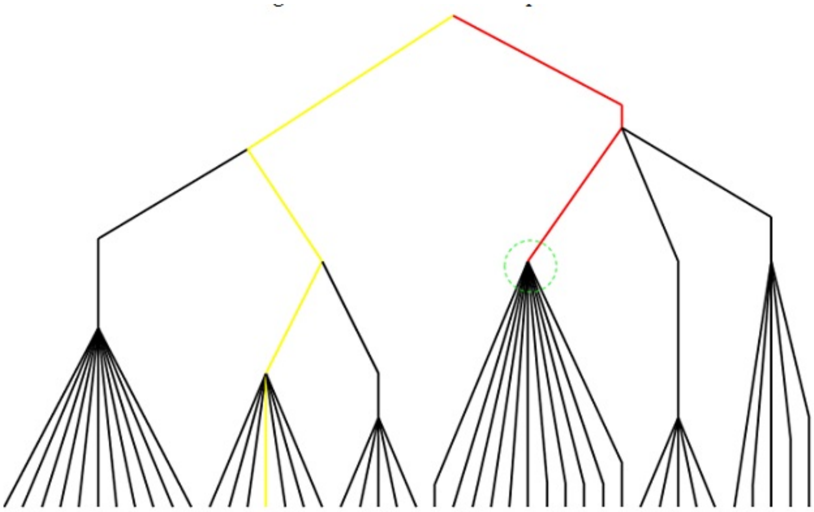
Scenario 1: When you select a pin

In this case, the path from the clock root to the sink will be highlighted. This is shown in the image below.

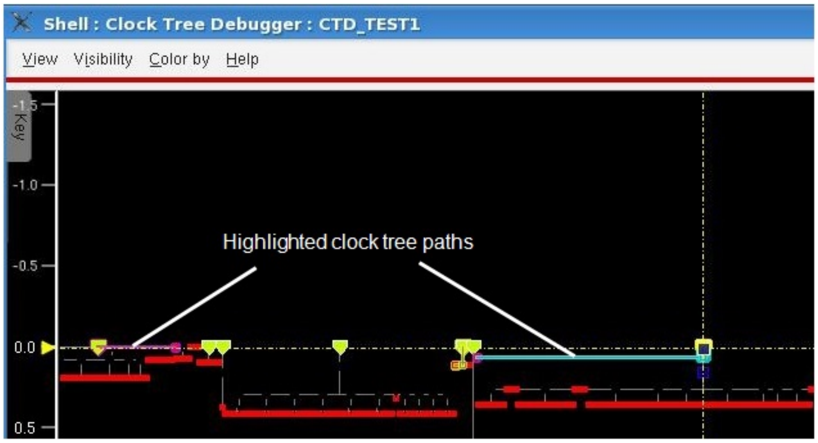


Scenario 2: When you select an intermediate node

In this case, the path from the clock root to the intermediate node (buffer, inverter, or clock gate) will be highlighted. This is shown in the image below.



The highlighted path for a selected object remains highlighted even when you select another object and trace its path. So, you can view multiple paths at a time. In the image below, two paths are highlighted, one from a clock gate and the other from a flop pin.



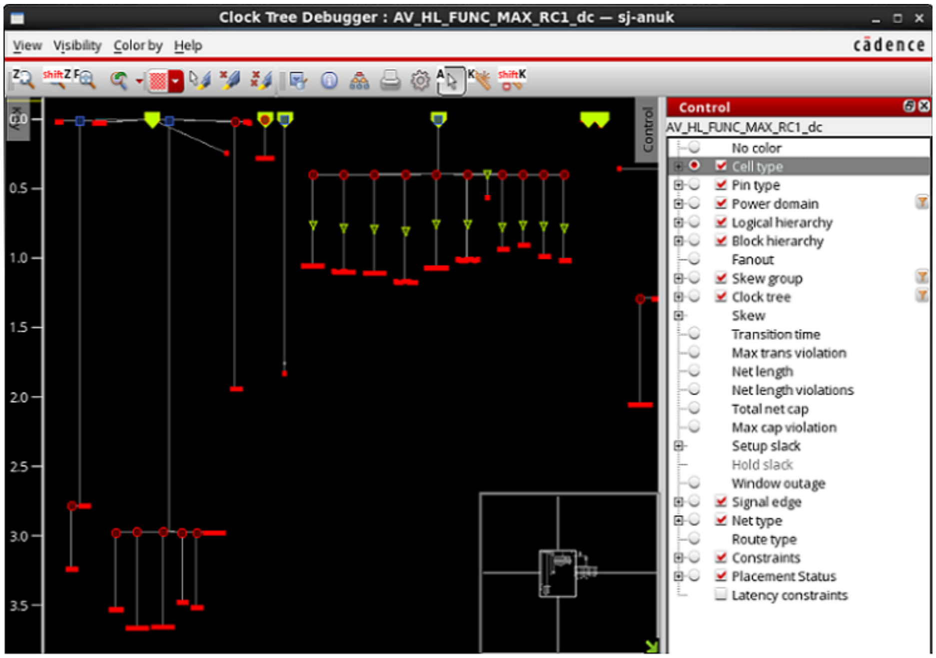
To erase all clock tree path highlights and flight lines from the Clock Tree Viewer and the physical layout window respectively, click the *Dehighlight All* option in the context menu.

Control Panel

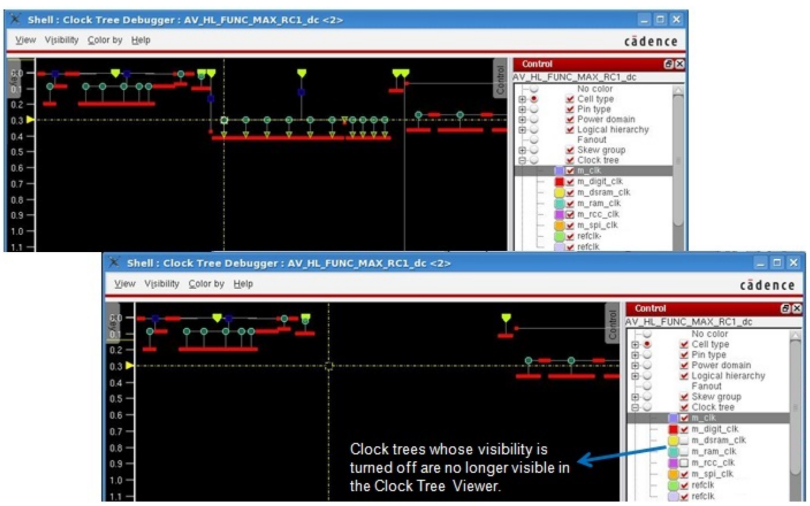
Use this window to specify controls in the *Visibility* and *Color by* menus. The Control panel contains a tree view including the items in the two menus, arranged in the same hierarchy. Similarly named items in the two menus are merged. For example, the Cell type item has both a radio button - from the *Color By* menu - and a submenu - from the *Visibility* menu. In the case of the *Skew group* submenu, individual items have a check box for both visibility and color.

The Control panel has an advantage over the individual menus. For example, if a user is required to set the color and visibility of multiple objects at the same time, the menu system requires navigating through the Visibility menu hierarchy and the color hierarchy separately while the Control panel shows both these controls at the same time. Additionally, the panel can keep the current state so that when revisiting the panel, the user immediately goes to the same place.

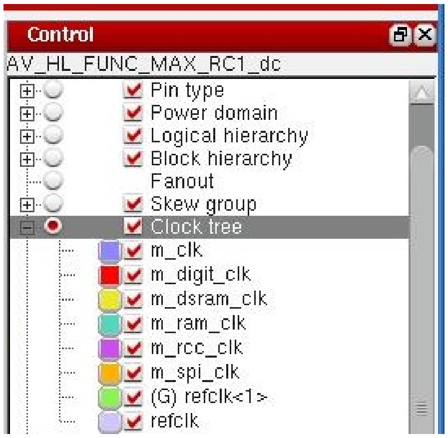
Choose – *View* – *Control panel*.



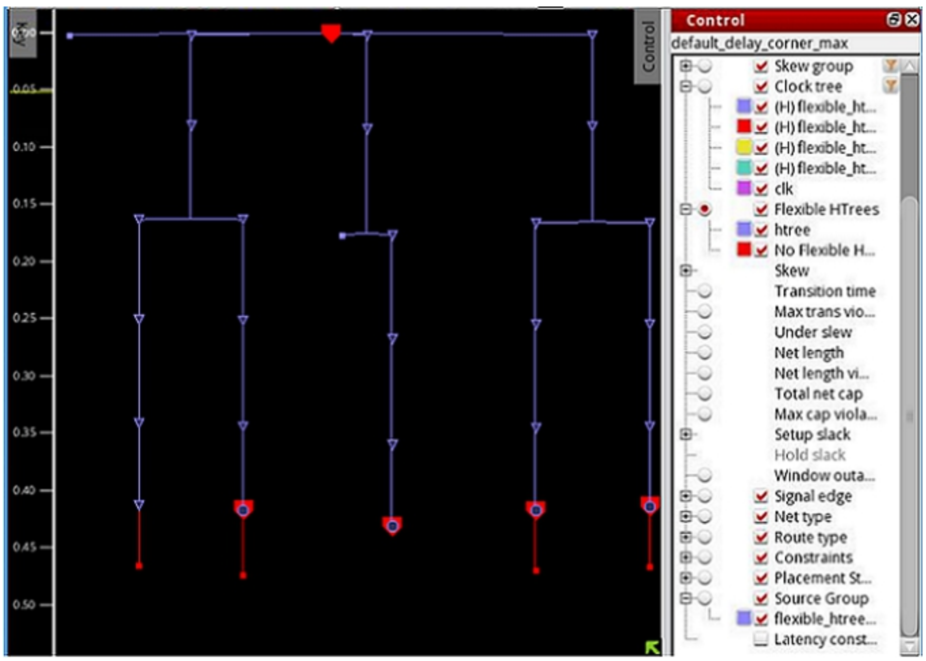
The Control panel allows you to turn off the visibility of clock trees in the Clock Tree Viewer. For example, when you turn off the visibility of some trees in the control panel, the trees will no longer be shown in the Clock Tree Viewer. This is useful if you have many clock trees and the display window is very tight. You can choose to turn off the display of some trees using the Control panel. This can be seen in the image below.



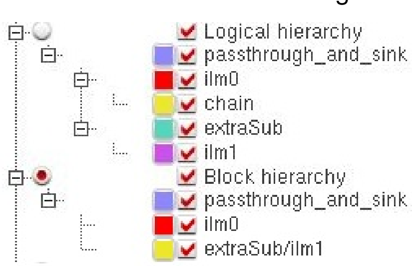
The Control panel lets you identify generated clock trees easily. In the Control panel, a mark, (G), appears before the names of all generated clock trees. This helps users to identify the generated clock trees easily and saves them time when debugging clock trees. The image below shows a generated clock marked by (G) in the Control panel.



The Control panel lets you identify flexible H-trees when the design has flexible H-trees. In the Control panel, a mark, (H), appears before the names of all flexible H-trees. A new coloring is added to show things in flexible H-trees in different colors. This helps users to identify the H-trees trees easily and saves them time when debugging flexible H-trees. A source group coloring is added so that everything in the same clock tree source group can be colored together. The source group appears only when the design has source groups. The image below shows flexible H-trees marked by (H) in the Control panel.



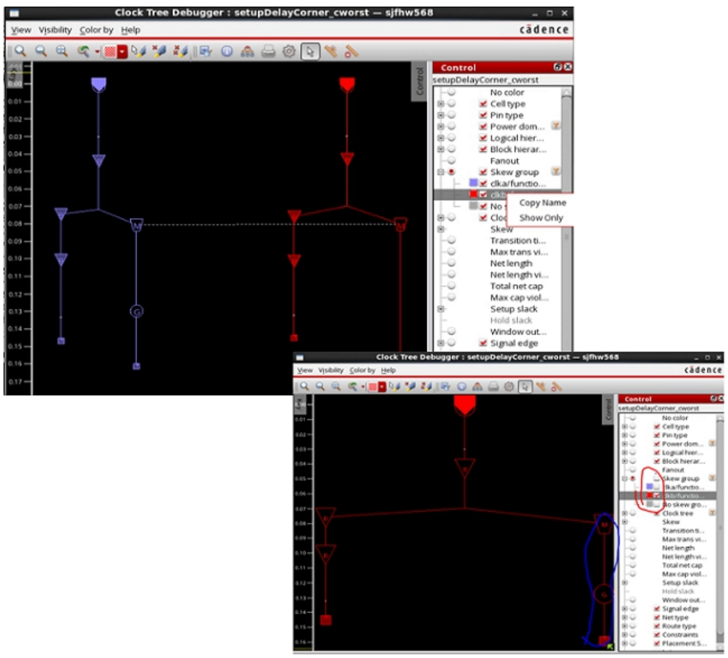
Note: The Logical hierarchy option in the Control panel shows the level hierarchy as a tree of modules or level names that can be toggled. The level hierarchy displays only those level names that are used by the elements in the CCOpt clock tree. This is shown in the image below.



The Block hierarchy option is used to color modules that represent ILM and other sub-blocks. For example, in the image above, you can see that there are four modules in the logical hierarchy but only two of these are ILM blocks, `ilm0` and `ilm1`. The Block hierarchy option lists both these blocks. Also, in order to distinguish names, the hierarchical name of the `ilm1` block (`extraSub`) is preserved in the listing.

Support to View the Cells and Sinks of Selected Skew Group in the Display Area

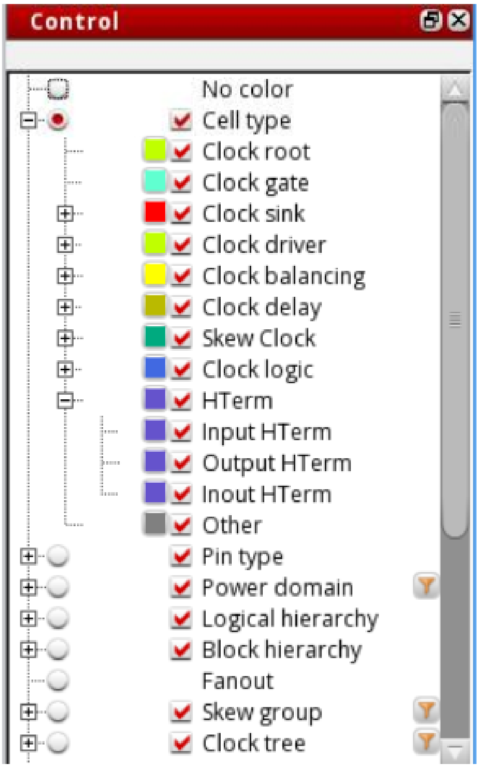
A dropdown menu, *Show Only* is added to the Skew group options in the *Control Panel* window. Right-click a skew group and select *Show Only*. The selected skew group is displayed in the display area of the CTD and all the clock convergence points are expanded. In the image below, the skew group with red color is selected and the convergence points for this skew groups are expanded in the display area.



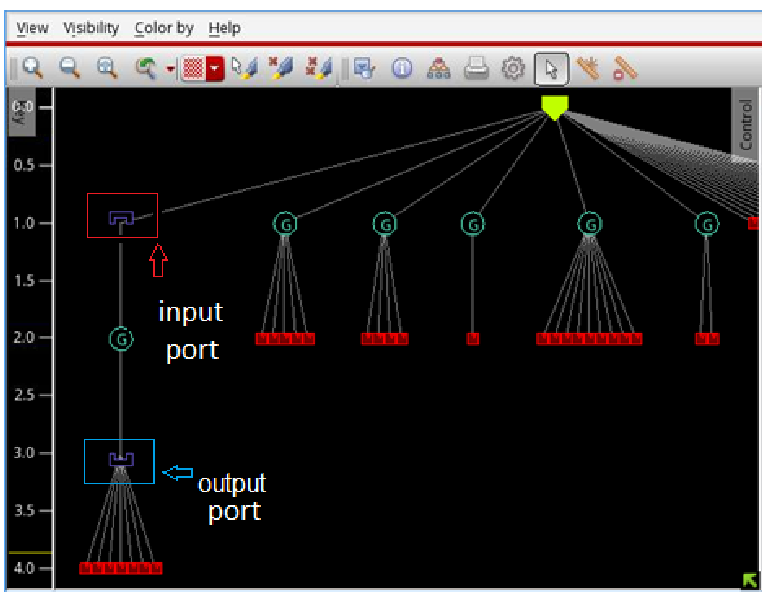
Options to View Preserved Ports in the Control Window

The following options are provided in the Control window for viewing preserved ports:

- *HTerm*
- *InputHTerm*
- *OutputHTerm*



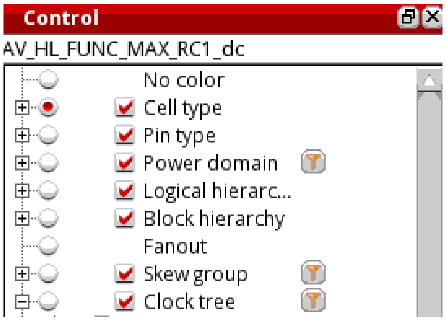
The above options are visible in the Contol panel only when using the Unit Delay mode. The input and output port bit markers show gates with preserved input and output ports. For example, in the image below, the new input and output port bit markers show that the gate on the left is in a module with a preserved input port before it and a preserved output port after it.



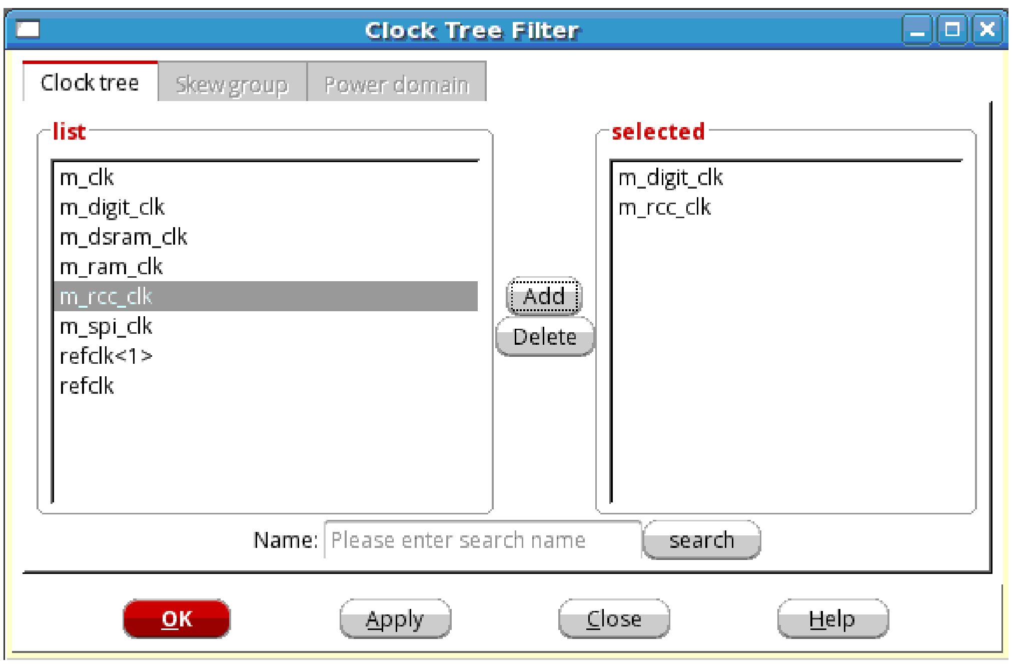
To hide the port markers, use the *View* < *Simplify* < *Hide* option.

Filter Options in the Control Window

In the Control panel, filter options are provided for power domains, skew groups, and clock trees. These are available by clicking the filter icons provided next to these items in the Control panel. These options let you view specific clock trees/power domains/skew groups in the display area while filtering out the rest. You can also search for specific clock trees/power domains/skew groups by name to filter from the display.



When any of the three filter icons is clicked, the Clock Tree Filter form opens.



The form has three tabs. Depending upon which filter icon is clicked, the corresponding tab is enabled. The rest are disabled. You can select the clock trees/power domains/skew groups to filter from the display.

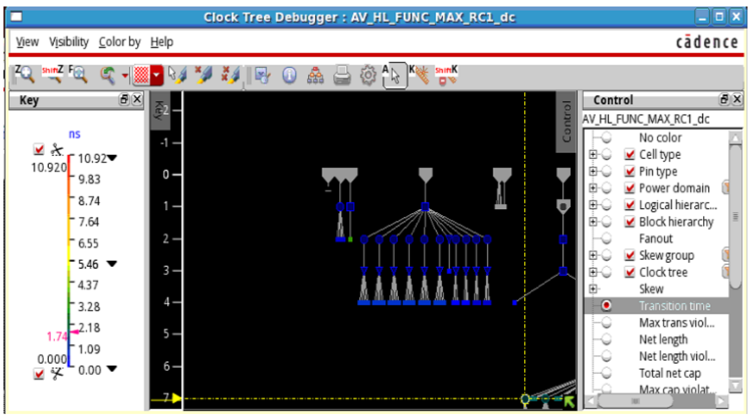
Options	Descriptions
list	Lists all the clock trees/power domains/skew groups.
selected	Lists all the clock trees/power domains/skew groups that are selected and added from the list box.
Add	Adds the clock tree/power domain/skew group selected in the list box to the selected box.

Delete	Deletes the clock tree/power domain/skew group in the selected box.
Name	Specifies the name of the clock tree/power domain/skew group to be searched.
search	Searches the specified clock tree/power domain/skew group.

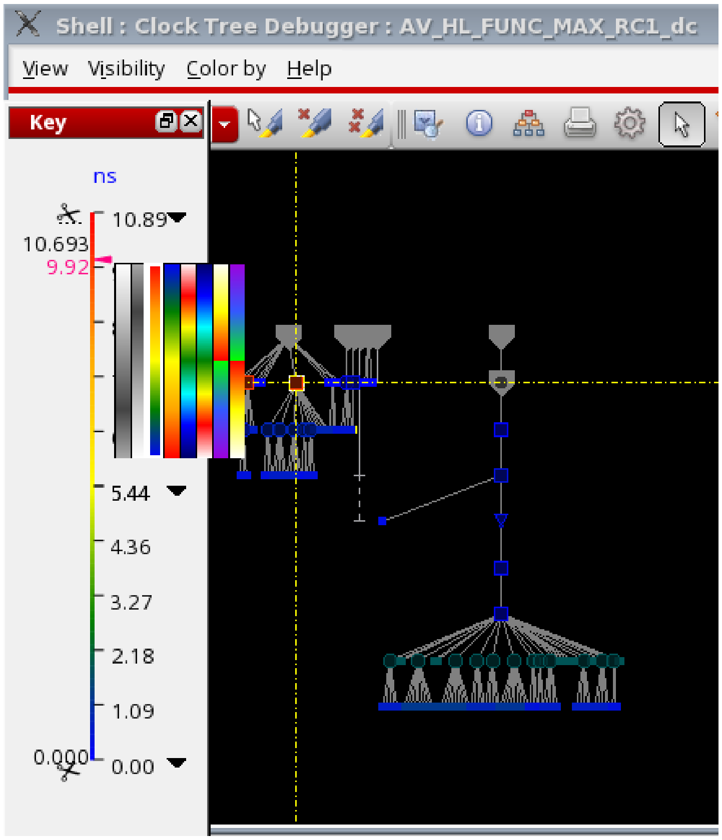
Key Panel

When enumeration or subset coloring is in effect, a window showing a key is available in the *Clock Tree Debugger* tool. The key contains a list of enumeration categories or subsets and their corresponding colors. If the window is visible, the contents change to reflect the currently selected coloring. Many enumeration categories are named after objects in the database, for example, skew groups, and may therefore be long. In these cases, the names are truncated, to avoid introducing a horizontal scroll bar to the window.

Choose – *View – Key panel*.



The window has a minimum width but you can drag it to make it wider. When a continuous color scale is in effect, a vertical scale is shown on the right side of the visualization. This shows the color scale in use, and provides controls to adjust the bounds of the scale, and limit objects based on value (the scissors). You can right-click the scale to select a different coloring - grayscale, rainbow, or heat map. This is shown in the image below.

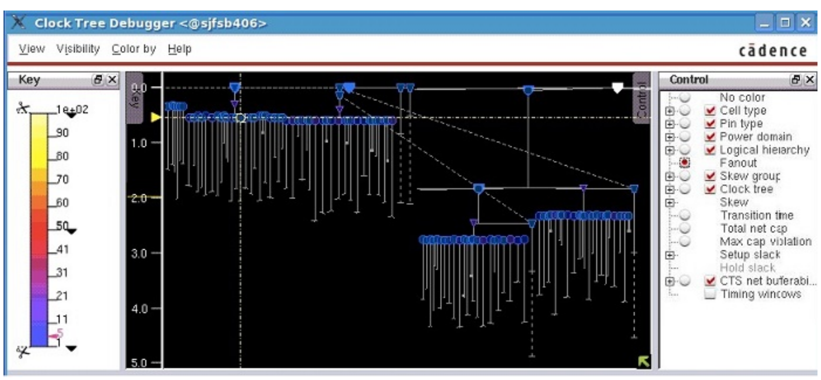


Unlike the enumeration key, which includes labels with arbitrary text, the color scale key is fixed and has a small width. This is the minimum width of the window. A check box is added to the *View* menu when a color scale is present to allow you to show or hide the scale.

Note: Enumeration is shown one at a time. Therefore, the key and scale panels are mutually exclusive. A single window may be used for both panels.

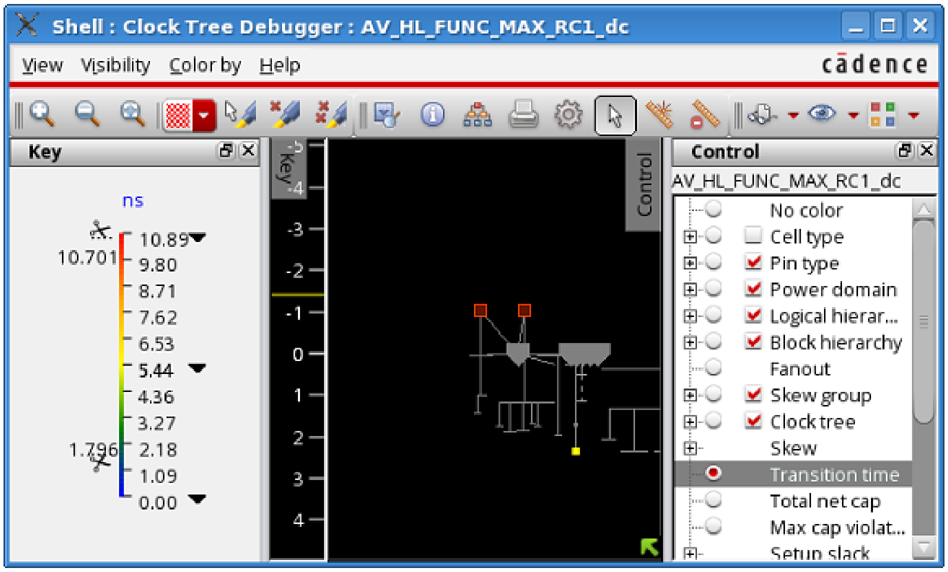
When you are coloring by a color scale, the values for selected objects are indicated on the scale shown in the Key panel in red color. However, the number of distinct values shown in the Key panel is limited when a large number of objects are selected. This helps avoid clutter and excessive redraw time.

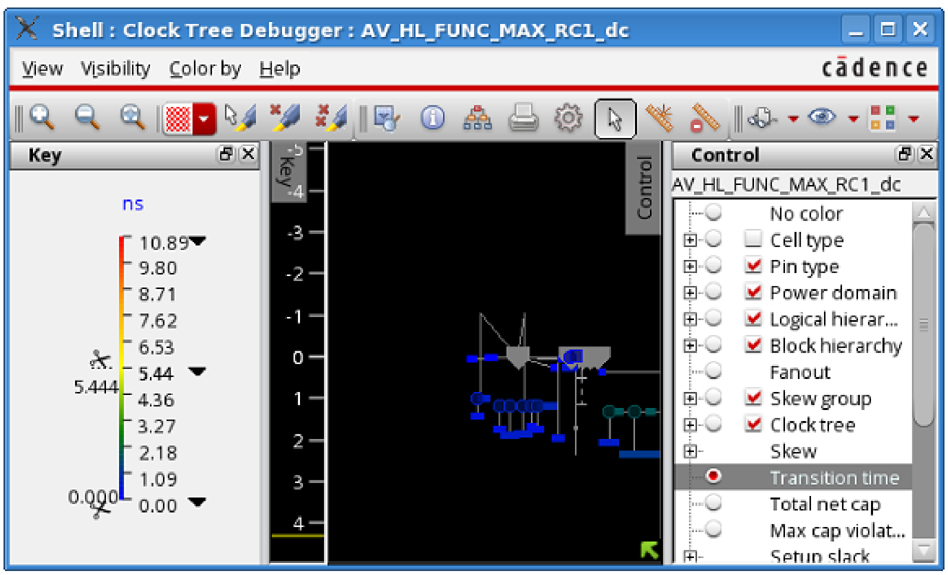
In the image below, you can see that the fanout of the selected object is 5.



You can use the scissors to redraw on the CTD display. The scissor at the top of the color range indicates the maximum value of the attribute and the scissor at the bottom of the color range indicates the minimum value of the attribute. When you move the scissors along the color scale, the clock objects that have attribute values out of the range specified by the two scissors will be hidden. You can see this in the two images below.

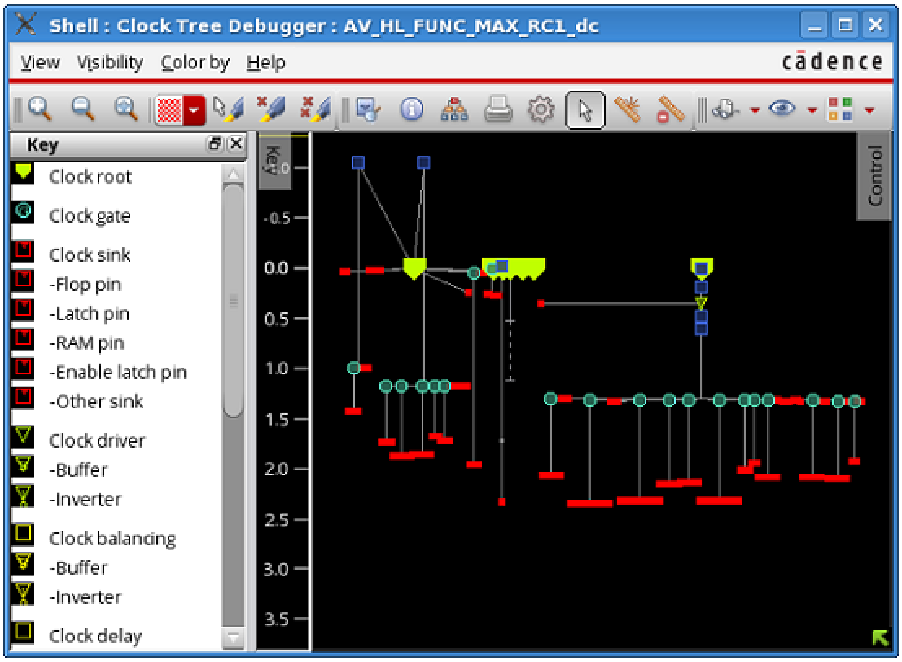
Note: The CTD display area is updated as you drag the scissors up or down.

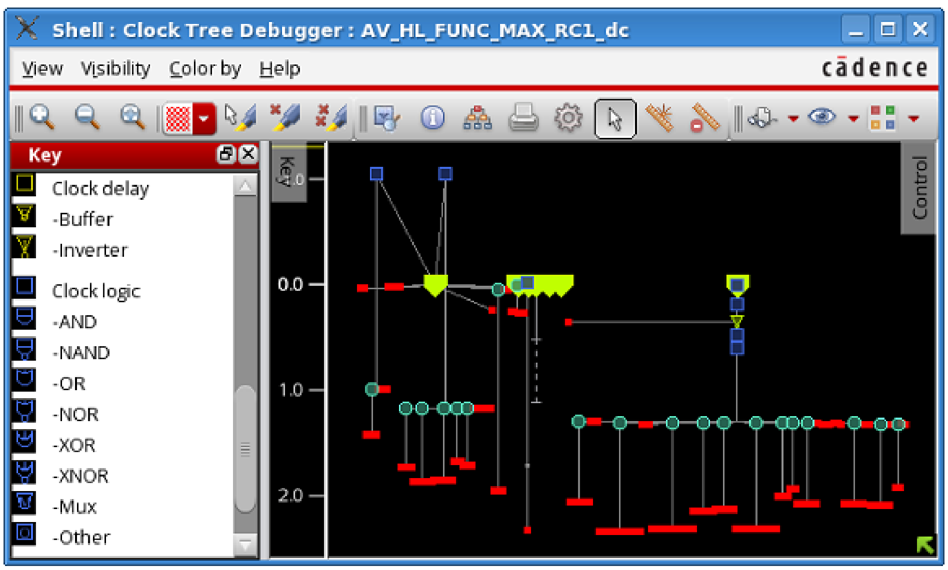




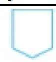
Key Panel for Cell Type Option

For enumeration of *Cell Type* options, the key panel shows a set of symbols with colors and graphic shapes. This is shown in the images below.





Symbols for each type of clock tree object in the *Cell Type* catalog are shown below.

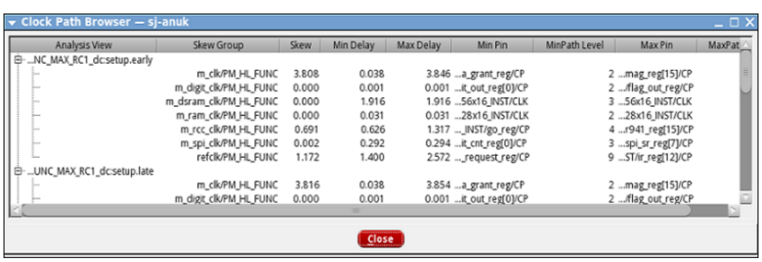
Object	Symbol
Clock root	
Clock gate	
Buffer	
Inverted	
Sink	
AND	
NAND	
OR	
NOR	
XOR	
XNOR	
Mux	
Others clock logic	

Clock Path Browser

The *Clock Path Browser* window consists of the following:

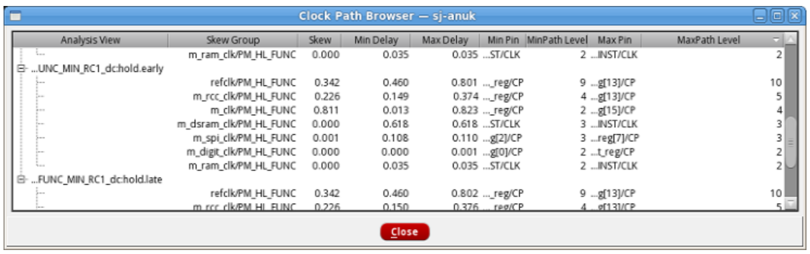
- A menu bar
- A table of path pairs

Choose - *View* - *Clock path browser*. When you open the CTD main window, the browser does not not open by default. To view the browser in the *Clock Tree Debugger* main window, select *Enable clock browser* in the *View* menu. The browser opens as a new window. You can choose to view first, second, or third level of min/max paths for skew groups. For details of above options, see the Clock Tree Debugger - View Menu section. You can also update these settings for the Clock Path Browser in the Set Preferences form. For details, see the "Set Preferences for CTD GUI Configuration" section.
To close the browser, click the Close button at the bottom of the browser window.



The *Browser* shows a table of path pairs with one row per minimum (min) or maximum (max) path in a particular skew group for a particular analysis view. Each row provides the following information in the various columns listed below:

- Analysis View
- Skew Group
- Skew
- Min Delay
- Max Delay
- Min Pin
- MinPath Level
- Max Pin
- MaxPath Level

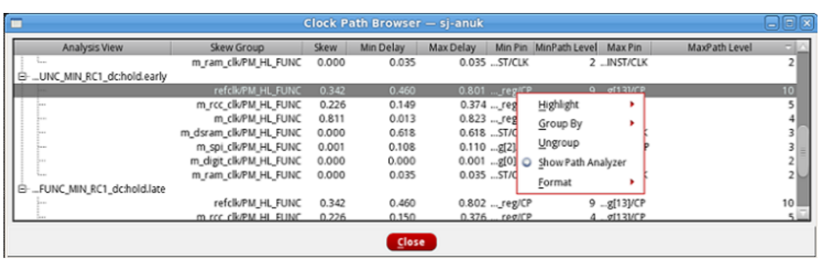


Cells in the table that correspond to objects such as the skew group, analysis view, and min or max pins have the context menu applicable to that object, allowing the full set of operations such as coloring by a skew group in the clock tree view.

Context Menu of the Clock Path Browser

Browser
provides the following functionalities, which you can access when you right-click any marker or line in the clock tree view:

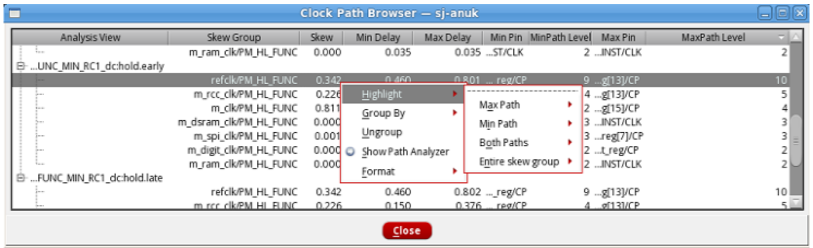
1. Highlight
2. Group By
3. Ungroup
4. Show Path Analyzer
5. Format



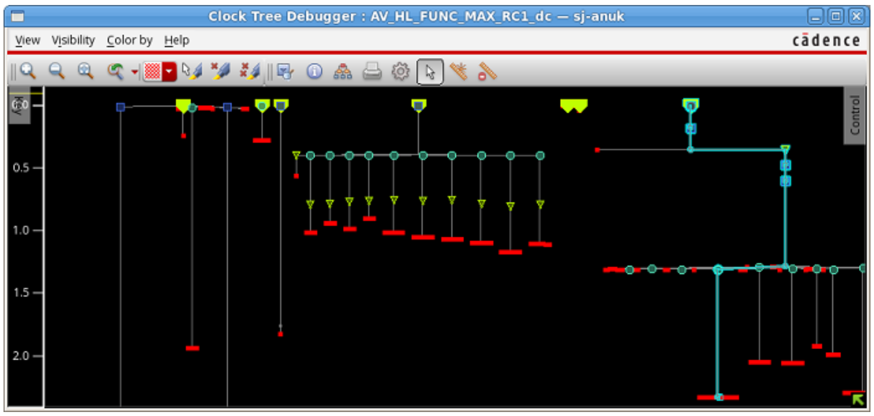
Options	Descriptions

Highlight

Highlights the selected item in the specified color. You can highlight the *Max Path*, *Min Path*, *Both Paths*, and *Entire skew group*. Each of these items has a submenu containing a color picker, as in the *Color by* menu.



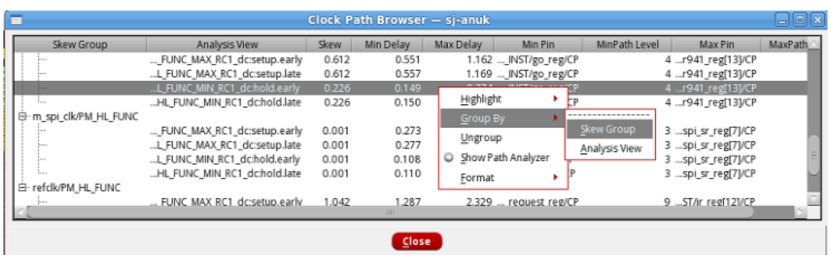
The image below shows the *Max Path* highlighted in blue for the selected item.



Group By

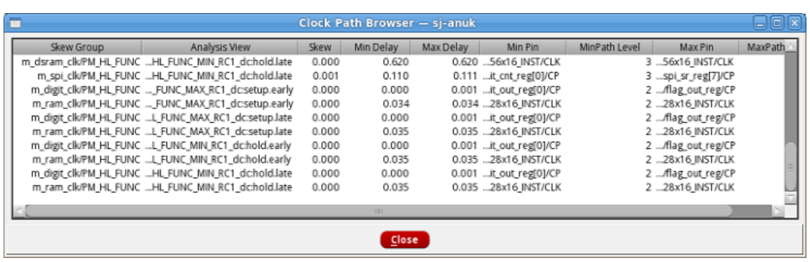
You can group the information displayed in the browser by *Skew Group* or *Analysis View*. When *Skew Group* is selected, the skew group information is displayed in column #1. When *Analysis View* is selected, the analysis view information is displayed in column #1.

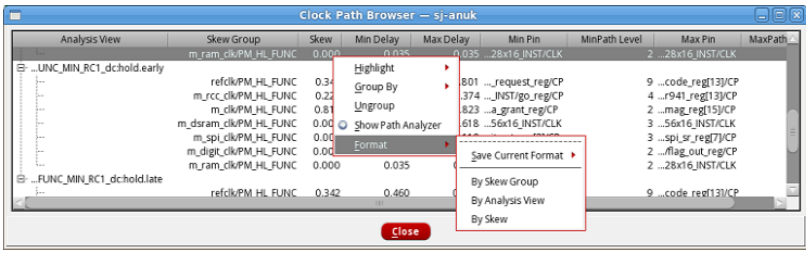
The image below shows the information grouped by the skew group.



Ungroup

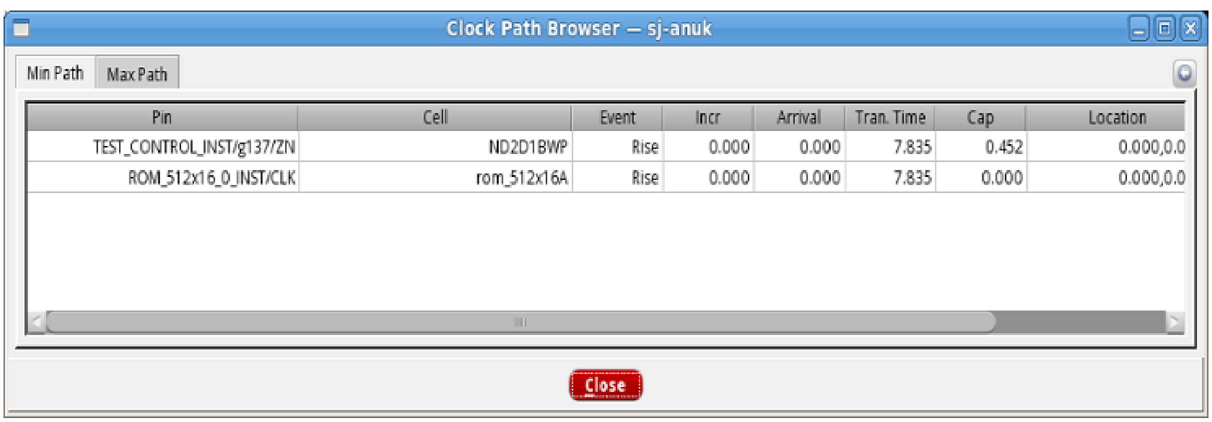
You can ungroup to view all the skew information, which includes both the skew group and analysis view information.



Show Path Analyzer	When you select this option in the context menu, the *Clock Path Analyzer* replaces the *Clock Path Browser* in its window. It provides a tabbed view containing tables for the *min* and m*ax paths*. To go back to the *Clock Path Browser*, click the *Back* button provided in the top-right corner of the window. For more information about the information displayed in the analyzer, see the "Clock Path Analyzer" section below.
Format	Allows you to format the information in the Browser *By Skew Group*, *By Analysis View*, and *By Skew*. When *By Skew Group* is selected, the skew group information is displayed in column #1. When *By Analysis View* is selected, the analysis view information is displayed in column #1.You can also save the current format by selecting *Save Current Format* and specifying the name of the format. 

Clock Path Analyzer

Double-click any row in the *Clock Path Browser* to view the *Clock Path Analyzer*. The *Clock Path Analyzer* replaces the *Clock Path Browser* in its window. You can also select the *Show Path Analyzer* option in the context menu of the *Clock Path Browser* to view the *Clock Path Analyzer*. Click the back arrow to return to the *Clock Path Browser* window.



Each row in the table of the *Clock Path Analyzer* represents a stage in the path in question. The following columns are shown:

- *Pin* – displays the name of the instance pin to which this row applies
- *Cell* – displays the library cell for the instance
- *Event* – states whether the row relates to a rise or fall event
- *Incr* – displays the delay between this row and the previous one

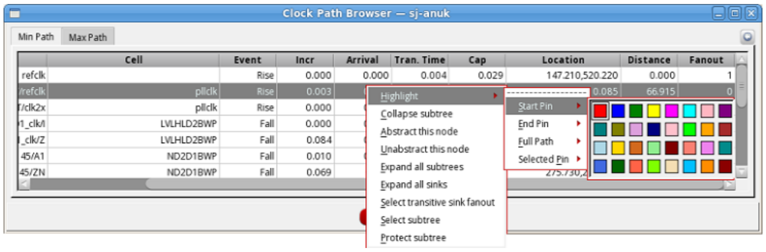
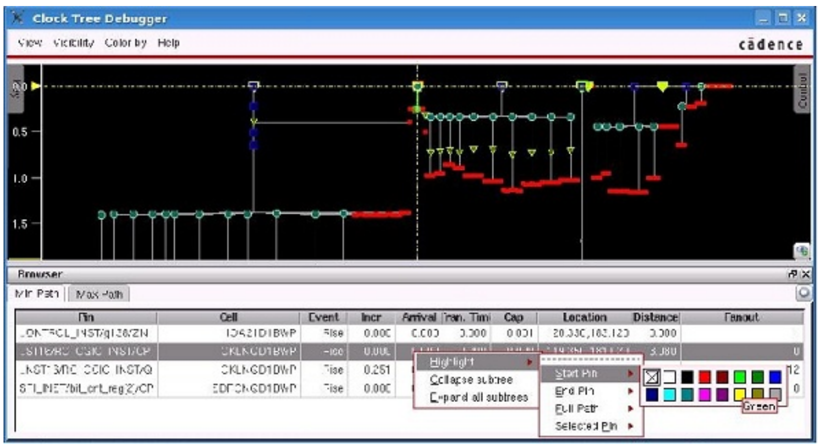
- *Arrival* – displays the total arrival time of the clock signal at this pin
- *Tran. time* – displays the transition time at this pin
- *Cap* – displays the capacitance at the pin (only for output pins)
- *Location* – displays the location of the pin
- *Distance* – displays the Manhattan distance from the last pin to this one
- *Fanout* – displays the fanout driven by this pin (only for output pins)

Context Menu of the Clock Path Analyzer

Right-click anywhere in the *Clock Path Analyzer* window to view the context menu. The following options are available in this menu:

1. Highlight
2. Collapse subtree
3. Abstract this node
4. Unabstract this node
5. Expand all subtrees
6. Select transitive sink fanout
7. Select subtree
8. Protect subtree

Options	Descriptions

Highlight	You can choose to highlight the *Start Pin*, *End Pin*, *Full Path* and *Selected Pin* in the color of your choice. Each of these items has a submenu containing a color picker, as in the *Color By* menu.  The image below shows the *Start Pin* of the selected object highlighted in green. 
Collapse subtree	Collapses the subtree.
Abstract this node	Abstracts the selected node.
Unabstract this node	Unabstracts the selected node.
Expand all subtrees	Expands all the collapsed subtrees.
Select transitive sink fanout	This option is available in the context menu when you right-click objects other than sinks. It selects the transitive sink fanouts for the selected object.
Select subtree	Selects everything under the selected node.
Protect subtree	Protects the subtree from collapsing.

11

Route Menu

Generate Routing Guide

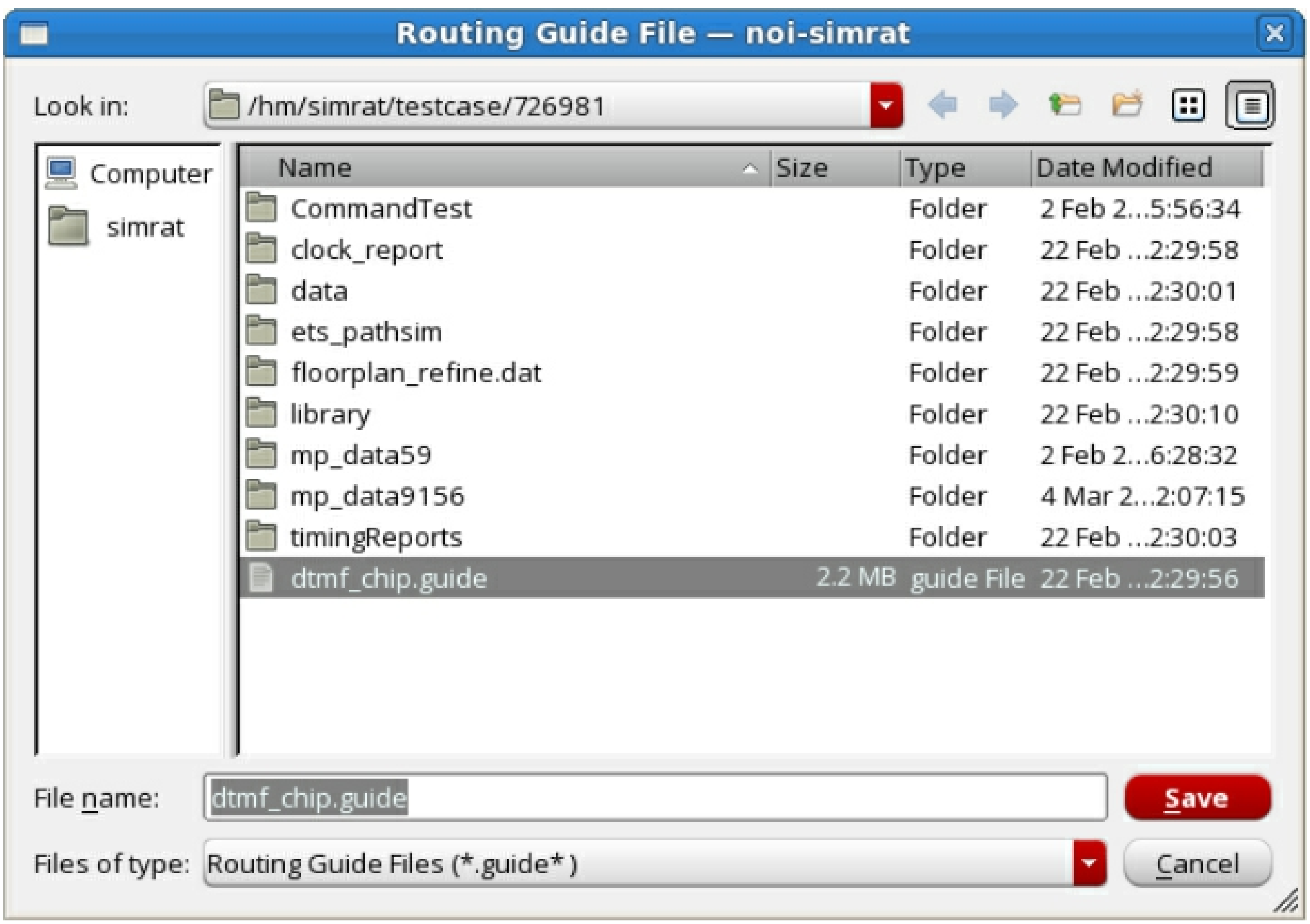
Routing guide files help control the routing topology by creating regions in which Early Global Route can create wires.

Routing guide files contain the following wire information: the coordinates of the wire ends, whether it is a horizontal or vertical wire, the width of the wire, and the layer number. The following example shows a section of a routing guide file:

```
routeGuideNet clk
wire 32.89 50 32.89 45.715 V 0.5 L 3
wire 32.89 45.715 32.89 10.045 V 0.5 L 5
wire 32.89 45.715 43.47 45.715 H 0.5 L 4
wire 32.89 10.045 7.13 10.045 H 0.5 L 4
wire 7.13 10.045 7.13 35.465 V 0.5 L 3
endRouteGuideNet
```

Note: Early Global Route honors completely routed nets with wires marked `FIXED` or `COVER`

- Choose *Route - Generate Routing Guide*.



Routing Guide File Fields and Options

File name	Specifies a name for the routing guide file.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `earlyGlobalRoute`

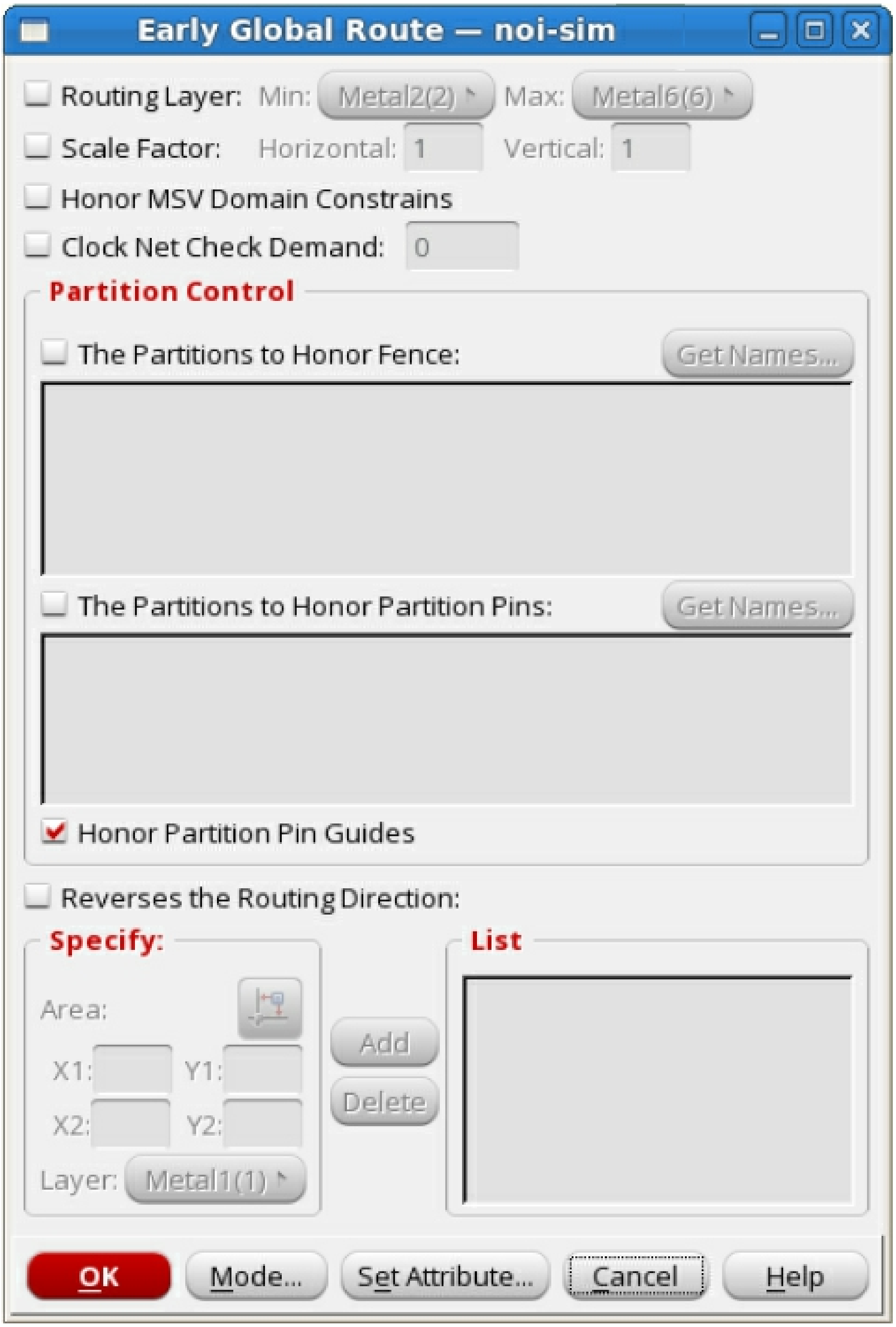
Early Global Route

Use the Early Global Route form to perform quick global routing for estimating routing-related congestion and parasitic (resistance and capacitance) values. You can use Early Global Route results to estimate and view routing congestion, and to estimate parasitic values for optimization and timing analysis. When used during prototyping, Early Global Route creates actual wires, so that you can get a good representation of RC and coupling for timing optimization at an early stage in the flow. Early Global Route also produces a congestion map that you can view to get an early feedback on whether the design is routable.

Note: The Early Global Router does not guarantee DRC-clean routing results. In congestion estimation, Early Global Route is used to calculate the track utilization by routing wires. Using the Early Global Router is correct if there is any overlap between Early Global Route wires and pre-routed wires as you should focus on the congestion value. If the congestion is different from NanoRoute DRC result or routing pattern, then the Early Global Router displays an alert.

Note: Do not perform signal integrity analysis on a design that has been routed using Early Global Route, because the routes are only used to estimate parasitic values for timing analysis. Route designs with NanoRoute, if you want to perform signal integrity analysis.

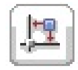
- Choose *Route* - *Early Global Route*



Early Global Route Fields and Options

Routing Layer	Select to specify the routing layer limits.	
	Min	Limits routing to layers at and above the specified layer. However, layers below the specified layer can still be used for routing if necessary, such as for short connections to pins. *Default:* Bottom-most layer
	Max	Limits routing to layers at and below the specified layer. All metal layers above the specified metal number are not routed. *Default:* Top-most layer
Scale Factor	Select to specify the scale factor values.	
	Horizontal	Scale the horizontal track supply by the specified value. *Default* : `1`
	Vertical	Scales the vertical track supply by the specified value *Default*: `1`
Honor MSV Domain Constrains	Honors MSV domain constraints. Select this option to enable Early Global Route to honor power domain settings. By default, Early Global Route ignores the power domain settings and routes as flat design. When enabled, Early Global Route honors power domain settings and routes wires inside preferred power domain as much as possible.	
Clock Net Check Demand	Select to specify the special width for clock wires. *Default*: `0`	

The Partitions to Honor Fence	Select to honor partition fences with a single-entry constraint and also honor fixed pins. Under the single-entry constraint once a hierarchical route enters a partition fence it does not cross the boundary again. The *Partitions to Honor Fence* option routes a net belonging to more than one partition so that the routing does not violate partition boundaries, in addition to routing intra-partition and global nets using the specifications of the partitions. For example, if a net belongs to partitions `P1` and `P3`, but not `P2`, the net is routed without going over the `P2` partition boundary. Click *Get Name* to display the *Get Partitions* form that enables you to specify the list of partitions. **Notes:** • Supports designs with up to 180 partitions. • Early Global Route supports nested partitions. *Default* : ""
The Partitions to Honor Partition Pins	Select to honor partition fences with single-entry constraint and pre-assigned pins (pins marked `FIXED`) and assigned pins (pins marked `PLACED`). Click *Get Name* to display the *Get Partitions* form that enables you to specify the list of partitions. *Default*: ""
Honor Partition Pin Guides	Select to honor partition pin guides. It uses the pin guide statements in the floorplan file to guide the routing through partition pin points. **Note**: Fixed pins and pin guides are only honored when this option is enabled.
Reverses the Routing Direction	Reverses the routing direction in the given area on the specified layer-range. It specifies an *Area* in which Early Global Route routes wires in the non-preferred direction. **Note:** You can define the reverse direction routing area by “`(x1 y1 x2 y2)`” and routing layer by “`Metal2:Metal2`” . The Early Global Router only supports a single layer with this option. Consequently, “`Metal2:Metal3`” is not supported. The `-reverseDirection` parameter only has impact on the congestion value calculation. By routing on reverse direction, you can reduce the routing capacity on the specified layer and add extract resource on the above and below layers. Innovus does not display the routing wires in reverse direction routing region.

	Area	Specify the reverse direction routing area coordinates in the *X1*, *Y1*, *X2*, *Y2 boxes.* Alternatively, click the  button to draw a rectangle to specify area. It automatically populates the *X1*, *Y1*, *X2*, and *Y2* boxes with the coordinates of the rectangle you draw on the main window.
	Layer	Specify the routing layer. **Note:** The Early Global Router only supports a single layer with this option. Consequently, `"Metal2:Metal3"` is not supported.
	Add	Click to add a selected area to the reverse routing direction list.
	Delete	Click to delete a selected area from the reverse routing direction list.
Mode	Opens the the *Mode Setup - EarlyGlobalRoute* form.	
Set Attribute	Click to display the *Route Attributes* form.	

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `earlyGlobalRoute`
- `setRouteMode`

Related Topics

- For information on Route commands, see Route Commands in the *Text Command Reference*.
- For information on Early Global Route, see *Using Early Global Route for Congestion and Timing Analysis* in the *User Guide*.

Special Route

Use the Special Route menu to access the SRoute form. This form enables you to route pins to nearby rings and stripes.

The SRoute form contains the following three pages:

- SRoute - Basic
- SRoute - Advanced
- SRoute - Via Generation

SRoute - Basic

Use the *Basic* page on the SRoute form to limit connections to specific nets or routes.

SRoute - Basic Page

Use the *Basic* page of the SRoute form to limit connections to specific nets or routes.

- To open the Basic page of the SRoute form, choose *Route* - *Special Route*, then click the *Basic* tab.

SRoute - Basic Fields and Options

Nets	The nets that must be connected in the core rows, or on the blocks, pads, or stripes. Both ground and power are specified by default. With this option users can selectively choose the nets to be routed by sroute from the available special nets.

SRoute	The types of routing that the Sroute tool can perform. Sroute performs all routing types (except secondary power pin) by default. Select or deselect any of the following options:
Block Pins	Connects the power and ground pins of the blocks to rings and stripes. With this option you can extend the ring pins corners of a block to the closest target.
Pad Pins	Connects the power and ground pins of the power pads into the core power ring. **Note:** The physical port must be identified with the `CLASS CORE` statement in the LEF file so that SRoute can recognize the proper pad pins to be routed to the core.
Pad Rings	Creates pad rings. If you do not specify any layers, a pad ring is created on each layer that contains pad pins.
Follow Pins	Connects the power and ground pins of the standard cells along the core rows. The end connections are based on the options you set using the Advanced tab of this form. By default, the end connections are at the first ring or stripe outside the row.
Floating Stripes	Connects to the floating stripes.
Secondary Power Pins	Connects secondary power pins on the specified nets to the closest segment of the ring around the power domain. You must specify one or more nets in the *Net(s)* field directly below this option
Top Layer	The top-most metal layers that the tool can use when routing power structures. Power structures on higher layers are not connected.
Bottom Layer	The bottom-most metal layers that the tool can use when routing power structures. Power structures on lower layers are not connected.

Allow Jogging	Specifies that jogs are allowed during routing to avoid DRC violations. • If both this option and Allow Layer Change are selected, the route uses both layer changes and jogging to avoid DRC violations. • If this option is selected and Allow Layer Change is deselected, then, if the route must jog to avoid a DRC violation, the jog occurs on the same layer whenever possible. This can result in routing in the non-preferred direction. • If this option is deselected and *Allow Layer Change* is selected, only straight connections are made between targets and that jogs are not allowed during routing. Routing can change to another layer to avoid DRC violations. • If both this option and *Allow Layer Change* are deselected, only straight connections to targets on the same layer are allowed.
Allow Layer Change	Allows connections to targets on different layers. See *Allow Jogging* for more information.
Area	If selected, you can either enter coordinates in the *X1*, *X2*, *Y1*, and *Y2* fields, or click the *Draw* button to interactively select an area in the design display window. Metal fill is created only in the specified area. If deselected, the tool performs routing for the entire design area. This is the default. **Note:** Selecting the *Area* option always preserves existing connections. If you select this option, the *Delete Existing Routes* option is disabled.
Connect to Target Inside the Area Only	If selected, connections from all sources within the specified area can connect only to targets that are also inside that area. If deselected, the tool makes connections from all sources within the specified area to targets both inside and outside the specified area.
Delete Existing Routes	If selected, removes existing connections when you click *Apply* or *OK*. If deselected, existing connections are left untouched each time you use the SRoute form. **Note:** This option is disabled if you select the *Area* option.

Generate progress messages	If selected, allows you to see all messages displayed while power routing takes place. Specify an integer value in the associated text entry field to set the interval at which progress messages are generated. If you specify `1`, SRoute generates every progress message; if you specify `2`, SRoute generates every other progress message, and so on. If deselected or if you specify a value of `0`, routing messages do not display in the Innovus console. This is the default.
Mode Setup	Opens the Mode Setup form that contains additional commands to provide more control over the special route property. For more information about mode options, see `setSrouteMode` in the *Text Command Reference* document.
Power Domain Selection	Determines which power domains are connected. Select one of the following options:
All	Connects the power and ground pins of all power domains. This is the default.
Selected	Connects only to the power domains that you select interactively. Place the cursor on a block, and then click to select it.
Named	Connects only to power domains that you specify in the text field.

Related Text Commands

For information on the following command, see "Power Route Commands" in the *Text Command Reference* document.

`setSrouteMode`

SRoute - Basic - Mode Setup

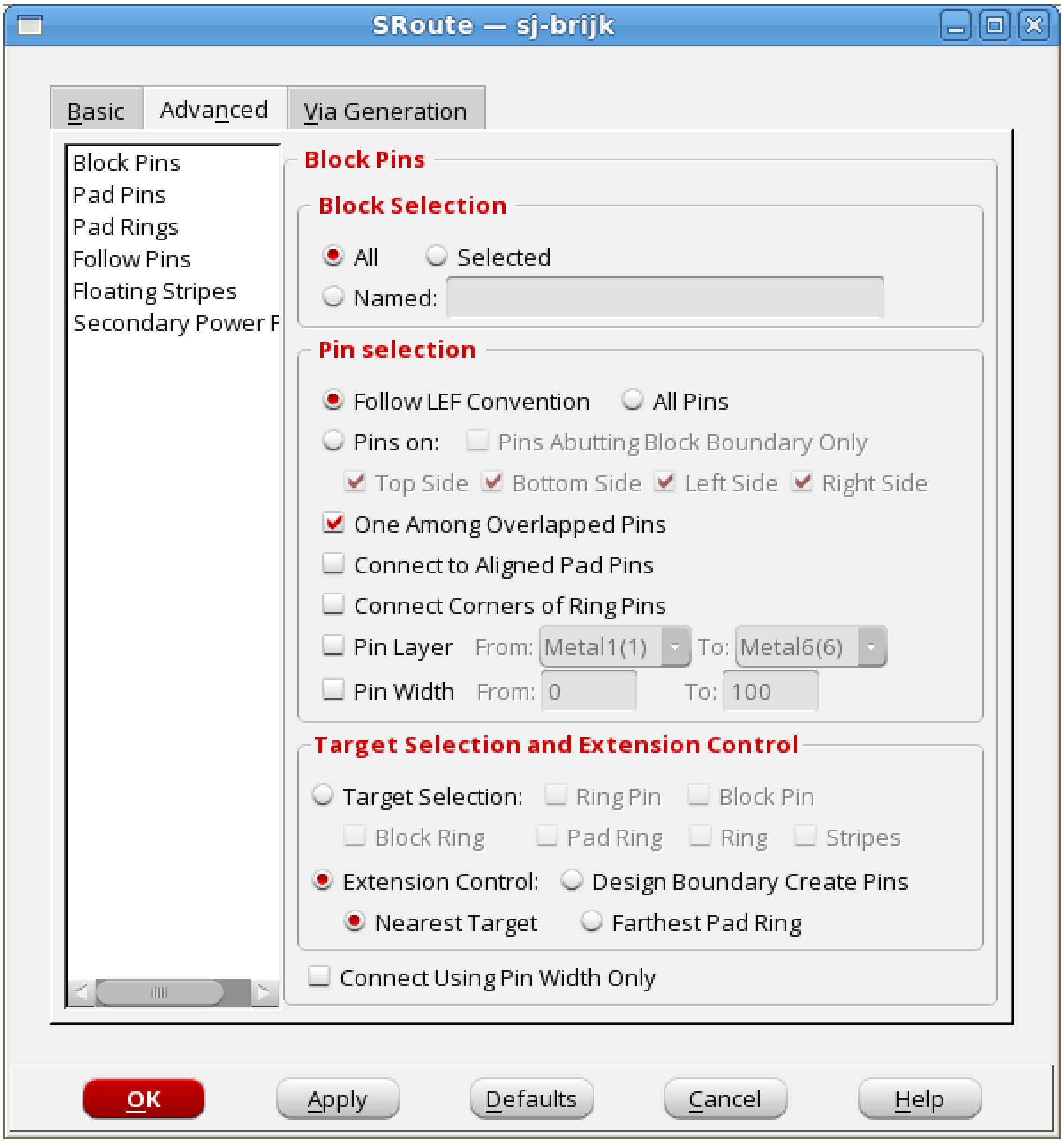
Use the *Basic* page of the SRoute form to setup the route modes.

- To open the Basic page of the SRoute form, choose *Route* - *Special Route*, then click the *Mode Setup* button.

The form is displayed as below. You get the following pages on the form:

- Routing (displayed by default)
- Block Pins
- Pad Pins
- Pad Rings
- Follow Pins
- Secondary Power Pins

On clicking the above-mentioned page names on the form, you will get different fields on each page to setup Special Route. See field descriptions in the table below for more information.



SRoute - Mode Setup Fields and Options

Routing	
Allow Wrong Way Route	Allow wrong way routing.

Via Only Connect to Closest Ring Layer	Specifies that a via should connect only to the closest ring layer when multiple rings overlap. *Default:* If you do not specify this parameter, vias connect to all overlapping rings.
Extend Nearest Target	Extends the nearest target so that it can be connected. The option is of type: bool. *Default*: false
Layer Cost of Preferred Direction	Specifies layer cost of preferred direction. The option is of type: string. *Default*: ""
Layer Cost of Non-Preferred Direction	Specifies layer cost of non-preferred direction.
Target Number	Specify number of target to connect. The option type is: int. *Default:* 0. Minimum and maximum are 0 and 20, respectively.
Target Search Distance	Specifies target search distance. The option type is: float. *Default*: 0
Jog Threshold Ratio	Defines the distance ratio between a jogging target and a straight target.
Connect Vias to	Specifies which shapes vias can connect to. *Default:* If this parameter is not specified, vias can connect to all shapes.
Block Pins	
Connect Ring Pins at Corners	Specifies whether to extend the ring pins at corners. *Default:* False

Connect Using Pin Width	Specifies that the block wire used for a connection is to have the same width as the pin from which it connects. *Default:* False
Pad Pins	
Minimum Via Size	Permits the software to reduce the size of vias at pad pins when changing layers, if there is not enough room for a standard size via. *Default:* If you do not specify this parameter, the software uses a value of 20, which permits vias that are 20% of the standard via size.
Split Wide Pad Pins with Width of	Splits the width and spacing for wide pad pins.
Pad Rings	
Use Lef Convention	If selected, pad rings are routed based on the specified information in the LEF file. If deselected, the tool chooses the pad pin connection style (ABUTMENT or FEEDTHRU) when routing pad rings, disregarding based on the specified information in the LEF file. *Default:* This option is selected by default.
Take signal Pins as PG Pins	Specifies signal pins as PG pins in pad ring creation. The option type is: bool. *Default*: False
Follow Pins	
Join Follow Pins with Gaps Smaller Than	Joins follow pin rail gaps smaller than this variable, bigger gaps will remain open. The option is of type: float. *Default:* 0.
Connect Core Pins with Length at least	Connects core pins of specified length. The option is of type: float. *Default:* 0.

Connect Core Pins with Same Length as Instance	Connects core pins whose length equals or is greater than the length of instance. *Default:* False.
Reference Macro	Uses specified macros as references for followpin creation. The option is of type: string. *Default*: ""
Treat Endcap Macro as Core Macro	Specifies to treat Endcap macro as core macro. The option type is: bool. *Default*: false
Secondary Power Pins	
Break Secondary Pin Rail with Gaps Bigger Than	Specifies variable value for gaps bigger than this value cause level shifter rail to break. The option type is: float.
Width of Secondary Pin Rail	Specifies width of followpin rail. The option type is: float.
Use NanoRoute to Connect Cell/Pin	Lists the cell/pin information NOT extracted from CPF.

Related Text Commands

For information on the following command, see "Power Route Commands" in the *Text Command Reference* document.

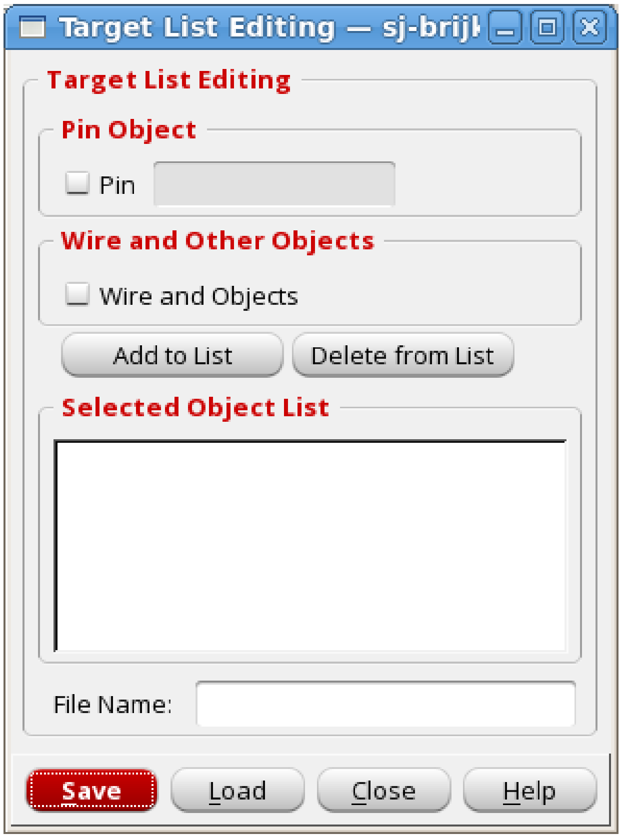
`sroute`

SRoute - Basic - Target List Editing

Use the *Basic* page of the SRoute form to set the target lists.

- To open the Basic page of the SRoute form, choose *Route - Special Route - Basic*, then click the *Target Editing Options* button.

Note: You may have to click the Pin, Wire and Objects options to display the full form.



SRoute - Target List Editing Fields and Options

Pin	The name of the Pin. Check the box and enter the name of the Pin and where it is located: *Instance* or *Macro* or *Selected*.
Add Object as Target	Select radio button to add object as target
Remove from Target	Select radio button to remove object as target
Wire and Objects	The name of the Wire and other objects. Check the box and enter the name of the Wire and other objects.
Location	Enter the location. You can click Draw to select the precise location.
Shape	Enter the shape, select from options.
Layer	Select the layer and layer number
Add to List	Select radio button to add to list
Delete from List	Select radio button to delete from list
Selected Object List	The list will display the object
File Name	Enter the file name

Related Text Commands

For information on the following command, see "Power Route Commands" in the *Text Command Reference* document.

`sroute`

SRoute - Advanced

Use the *Advanced* page on the SRoute form to set additional options for creating pad rings and routing block pins, pad pins, and standard cell pins.

- To open the Advanced page of the SRoute form, choose *Route - SRoute*, then click the

- To open the Advanced page of the SRoute form, choose Route - SRoute, then click the *Advanced* tab.

The *Advanced* page on the SRoute form contains the following pages:

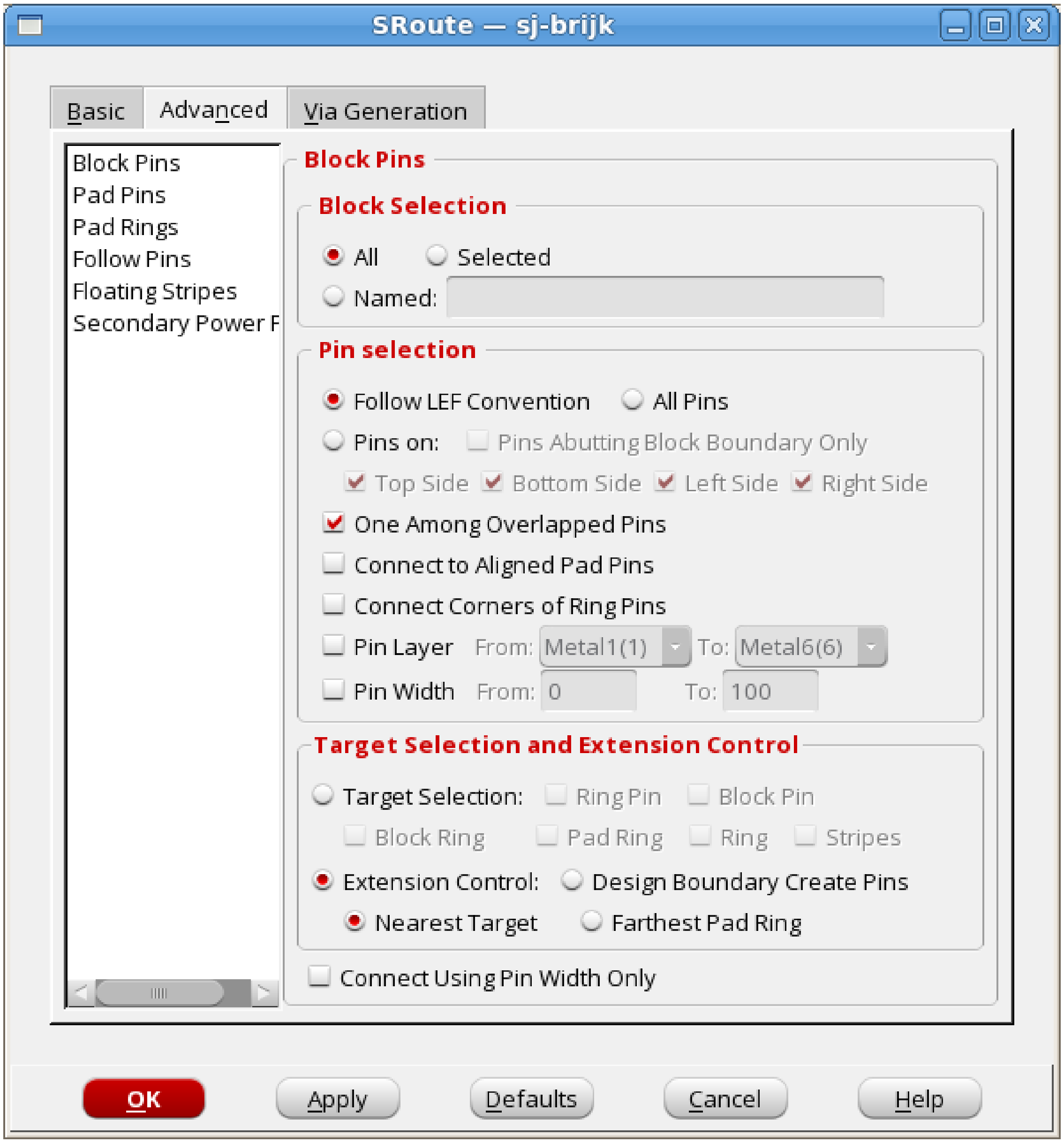
- SRoute - Advanced - Block Pins
- SRoute - Advanced - Pad Pins
- SRoute - Advanced - Pad Rings
- SRoute - Advanced - Follow Pins
- SRoute - Advanced - Secondary Power Pins

SRoute - Advanced - Block Pins

Use the Block Pins page of the SRoute form to specify options for how block pins are to be connected.

- To open the Block Pins page of the SRoute forms, choose *Route* - *Special Route* and click the *Advanced* tab

The *Block Pins* page is displayed by default.



SRoute - Advanced - Block Pins Fields and Options

Block Selection	The blocks for which pins are to be connected. Select one of the following options:
All	Connects the power and ground pins of all blocks. This is the default.
Selected	Connects only to the blocks that you select interactively. Place the cursor on a block, and then click to select it.

Named	Connects only to blocks that you specify in the text field.
Pin Selection	The block pins that are to be connected. Select one of the following options:
Follow LEF convention	Pins are connected exactly as specified in the LEF file. For example, if the LEF file has multiple ports with one geometry connecting to each port, then one port per pin is connected.
All Pins	All pins on all ports are connected, regardless of how pins are specified in the LEF file.
Pins on	Only boundary pins are connected. If you select this option, you can also deselect one or more of the following options to prevent the connection of boundary pins at the deselected location: *Top Side* *Bottom Side* *Left Side* *Right Side* Pins abutting block boundary only
One Among Overlapped Pins	If selected, specifies that all pins (including those that overlap) should be routed. If deselected, if multiple pins overlap either fully or partially, only one will be routed. **Note:** This parameter is effective *only* if *Pin Selection - All Pins* is selected.
Connect to aligned pad pins	If selected, specifies that a pad pin can be considered a connection target for a block pin if the pad pin is aligned with the block pin. *Default:* If you do not specify this option, pad pins are never considered a target for block pin connection.
Connect Corners of Ring Pins	Select to connected corners of ring pins.
Pin Layer	If selected, limits the layers on which block pins can be routed to the layer numbers you select in the *From* and the *To* drop-down menus. If deselected, the tool routes block pins on all layers. This is the default behavior.

Pin Width	If selected, limits the size of block pins that can be routed to a range that you specify. Specify the minimum pin width in the *From* text entry field and a maximum pin width in the *To* text entry field. If deselected, the tool routes block pins of all widths. This is the default behavior.
Target Selection	The target to which block pins are connected during routing. Select one of the following options: • *Block Ring* • *Ring* • *Pad* • *Stripes* • *Ring Pin* • *Block Pin*
Extension Control	Extends the block pin to targets of specified type. Multiple target types are allowed. The block pin will be open if no specified target is found: • *Nearest Target:* Extends the block pin to the nearest legal target. • *Design Boundary Create Pins:* Extends the block pin to the design boundary and creates a new power pin along the design boundary. Any overlaps with existing I/O pins at the design boundary are flagged as violations after the extension. • *Fathest Pad Ring*: Extends the block pin to the last pad ring that already exists on top of the I/O pad cells.
Connect using pin width only	If selected, specifies that the block wire used for a connection is to have the same width as the pin from which it connects. If you do not specify this option, the block wire width is either the width of the target or the width of the pin, whichever is smaller. This is the default.

Related Text Commands

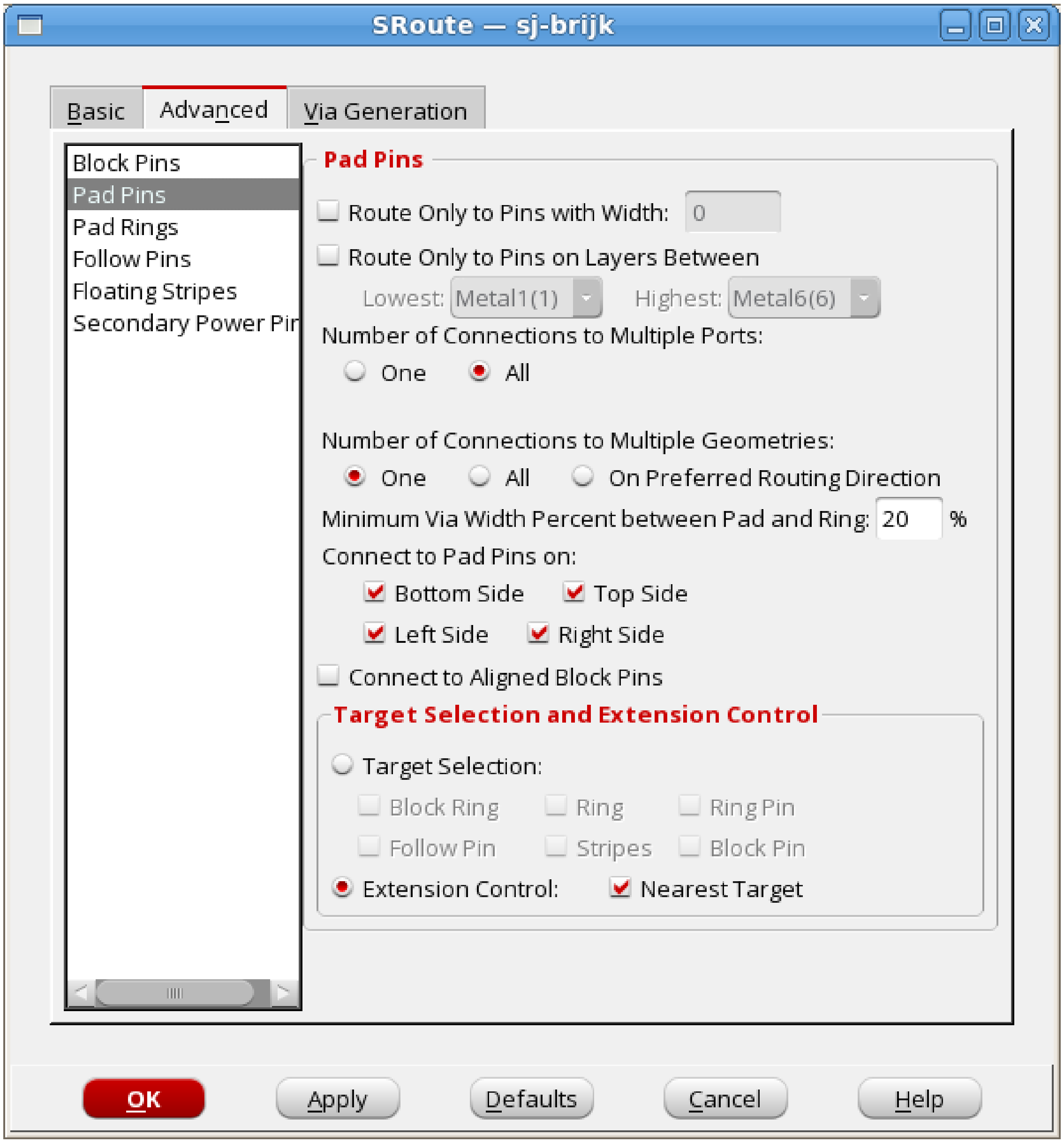
For information on the following command, see "Power Route Commands" in the *Text Command Reference* document.

`sroute`

SRoute - Advanced - Pad Pins

Use the Pad Pins page of the SRoute form to specify options for how pad pins are to be connected.

- To open the Pad Pins page of the SRoute form, choose *Route* - *Special Route* , click the *Advanced* tab, then choose *Pad Pins* from the display list.



SRoute - Advanced - Pad Pins Fields and Options

Route Only to Pins with Width	If selected, connects only pins with the width you specify in the text entry field. If deselected or if no width is specified, the tool automatically determines the width of the power pins to use. This is the default. It is generally not necessary to specify the width value.

Route Only to Pins on Layers between	If selected, you can use the drop-down menus to select the lowest and highest layers permitted for a pin connection. If deselected, the tool routes pins to all layers. This is the default.
Number of connections to multiple ports	Controls the connection behavior for pins that have multiple ports defined in the LEF file. Select one of the following options:
One	Connects only a single port of a block pin if multiple ports are defined in the LEF file. This is the default.
All	Connects all ports defined in the LEF file.
Number of connections to multiple geometries	Controls the connection behavior for pins that have multiple geometries defined in the LEF file for each port. Select one of the following options:
One	Connects to only one geometry per port. This is the default.
All	Connects to all geometries defined for the port, in both the preferred and nonpreferred routing directions.
On the preferred routing direction	Connects to all geometries defined for the port that are on the preferred routing direction.
Minimum via width percent between pad and ring	(Optional) Controls the size of vias that connect the pad and the ring. Specify this value as a percentage of pad width. The default value is `20`, which prevents the generation of vias that are smaller than 20 percent of the width of the pad.
Connect to Pad Pins on	Specifies which edges pad pins can connect to. You can prevent connections to pad pins from a particular edge by deselecting it. By default, you can connect pad pins along all edges.
Connect to Aligned Block Pins	If selected, a block pin can be considered a connection target for a pad pin if the block pin is aligned with the pad pin. If deselected, block pins are never considered a target for pad pin connection. This is the default.

Related Text Commands

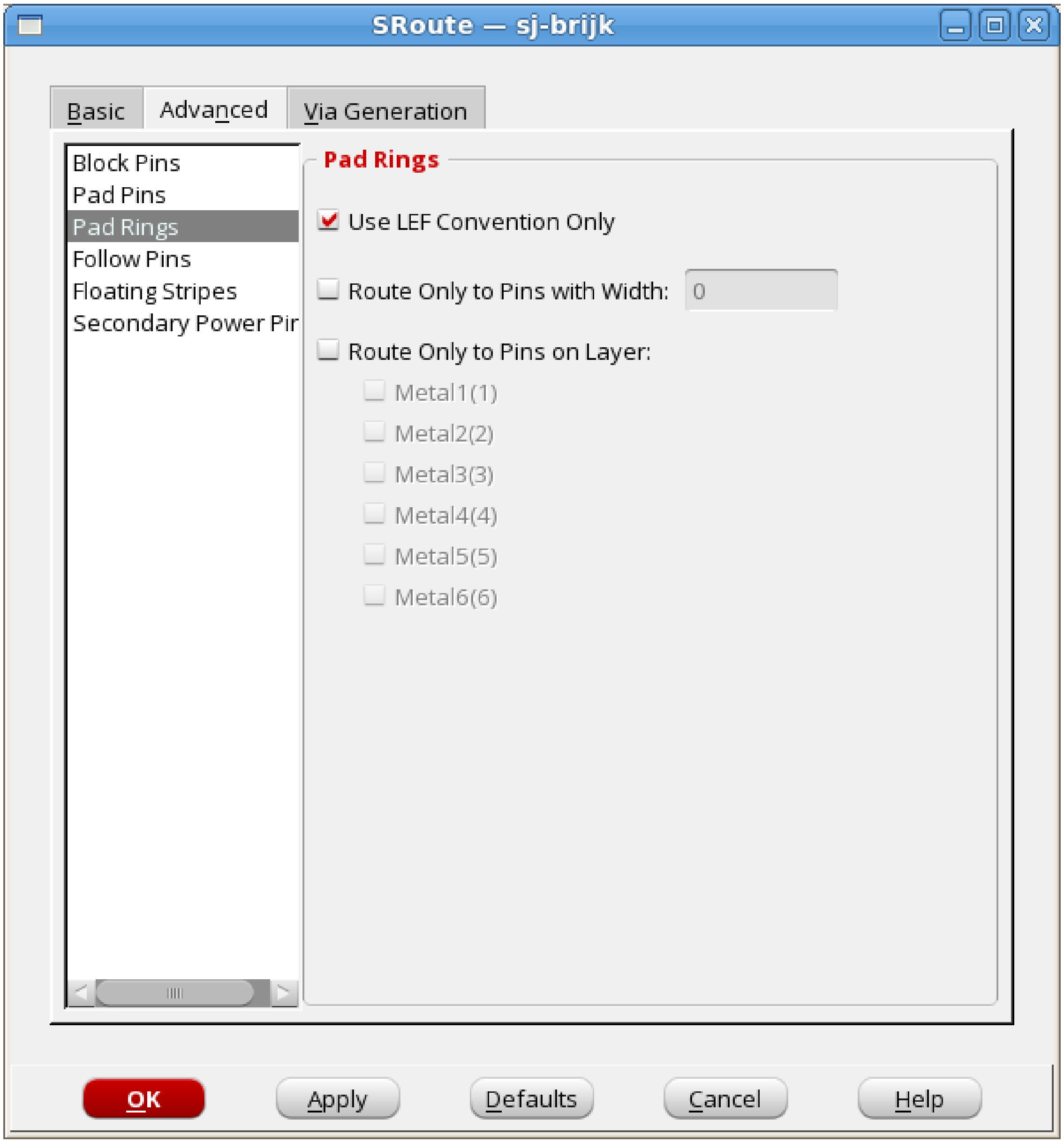
For information on the following command, see "Power Route Commands" in the *Text Command Reference* document.

sroute

SRoute - Advanced - Pad Rings

Use the Pad Rings page of the SRoute form to set limits on the pins that are connected to the pad ring.

- To open the Pad Rings page of the SRoute form, choose *Route* - *Special Route* , click the *Advanced* tab, then choose *Pad Rings* from the display list.


SRoute — sj-brijk
Basic
Advanced
Via Generation
Block Pins
Pad Pins
Pad Rings
Follow Pins
Floating Stripes
Secondary Power Pir
Pad Rings
Use LEF Convention Only
Route Only to Pins with Width:
0
Route Only to Pins on Layer:
Metal1(1)
Metal2(2)
Metal3(3)
Metal4(4)
Metal5(5)
Metal6(6)
OK
Apply
Defaults
Cancel
Help

SRoute - Advanced - Pad Rings Fields and Options

Use LEF Convention Only	If selected, pad rings are routed based on what is specified in the LEF file. This is the default. If deselected, the tool chooses the pad pin connection style (`ABUTMENT` or `FEEDTHRU`) when routing pad rings, disregarding what is specified in the LEF file.
Route Only to Pins with Width	If selected, the tool connects only pins with the width you specify in the text entry field. If deselected or if no width is specified, the tool automatically determines the width of the power pins to use. This is the default. It is generally not necessary to specify the width value.
Route Only to Pins on Layer	If selected, pins are connected only on the layers you select from the list. If deselected, pins on all layers are connected. This is the default.

Related Text Commands

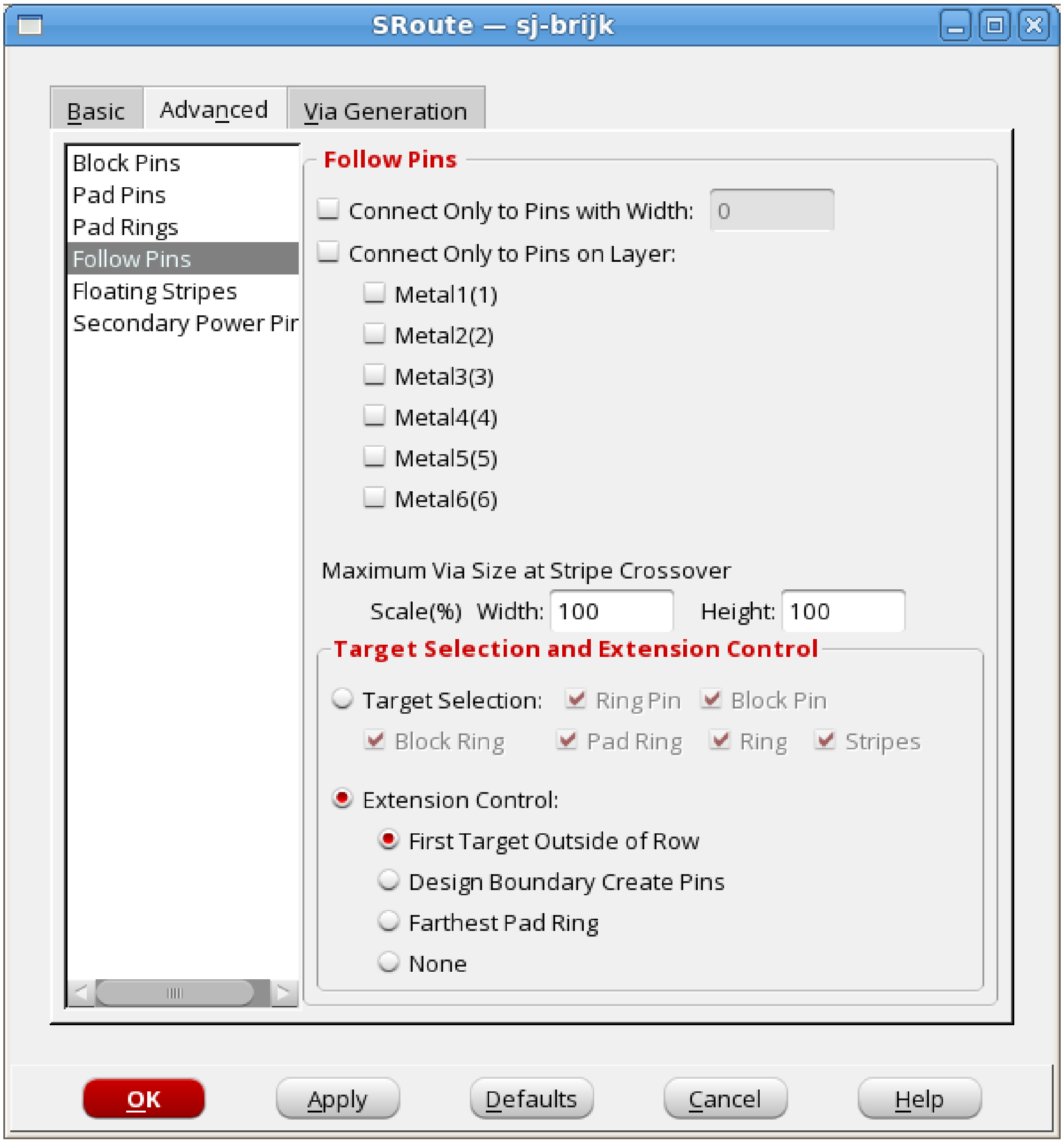
For information on the following command, see "Power Route Commands" in the *Text Command Reference* document.

`sroute`

SRoute - Advanced - Follow Pins

Use the Follow Pins page of the SRoute form to specify connectivity options for standard cell pins.

- To open the Standard Cell Pins page of the SRoute form, choose *Route - Special Route* , click the *Advanced* tab, then choose *Follow Pins* from the display list.


SRoute — sj-brijk
Basic
Advanced
Via Generation
Block Pins
Pad Pins
Pad Rings
Follow Pins
Floating Stripes
Secondary Power Pir
Follow Pins
Connect Only to Pins with Width:
0
Connect Only to Pins on Layer:
Metal1(1)
Metal2(2)
Metal3(3)
Metal4(4)
Metal5(5)
Metal6(6)
Maximum Via Size at Stripe Crossover
Scale(%) Width: 100
Height: 100
Target Selection and Extension Control
Target Selection:
Ring Pin
Block Pin
Block Ring
Pad Ring
Ring
Stripes
Extension Control:
First Target Outside of Row
Design Boundary Create Pins
Farthest Pad Ring
None
OK
Apply
Defaults
Cancel
Help

SRoute - Advanced - Follow Pins Fields and Options

Connect only to pins with width	If selected, connects only pins with the width you specify in the text entry field. If deselected or if no width is specified, the tool automatically determines the width of the power pins to use. This is the default. It is generally not necessary to specify the width value.
Connect only to pins on layer	If selected, you can select one or more layers on which the tool can connect pins. If deselected, all layers are used. This is the default.
Maximum via size at stripe crossover	(Optional) Specify a *Width* and *Height* value as percentages of the width and height of the via at the top of the stack to limit the maximum size of stacked vias. Smaller vias leave room for more routing tracks on layers between the vias. The default value is `100`.
Extension Control	
First Target Outside of Row	Extends the stripe or standard cell pin to the first ring or stripe beyond the end of the row. This is the default.
Design Boundary Create Pins	Extends the stripe or standard cell pin to the design boundary and creates new power pins along the design boundary. Any overlaps with existing I/O pins at the design boundary are flagged as violations after wire extension.
Farthest pad ring	Extends the stripe or standard cell pin to the farthest pad ring that already exists on top of the I/O pad cells.
None	Unconnected stripes and standard cell pins are not extended. Standard cell pins are extended to the location specified by the *Secondary Target* option.

Related Text Commands

For information on the following command, see "Power Route Commands" in the *Text Command Reference* document.

`sroute`

SRoute - Advanced - Floating Stripes

Use the Secondary Power Pins page of the SRoute form to specify the secondary power pins.

- To open the Secondary Power Pins page of the SRoute form, choose *Route* - *Special Route* , click the *Advanced* tab, then choose *Floating Stripes Pins* from the display list.

SRoute - Advanced - Floating Stripes Fields and Options

Target Selection	At least one specified target or ALL targets should be chosen.

Related Text Commands

For information on the following command, see "Power Route Commands" in the *Text Command Reference* document.

`sroute`

SRoute - Advanced - Secondary Power Pins

Use the Secondary Power Pins page of the SRoute form to specify the secondary power pins.

- To open the Secondary Power Pins page of the SRoute form, choose *Route* - *Special Route* , click the *Advanced* tab, then choose *Secondary Power Pins* from the display list.


SRoute — sj-brijk
Basic
Advanced
Via Generation
Block Pins
Pad Pins
Pad Rings
Follow Pins
Floating Stripes
Secondary Power Pir
Secondary Power Pins
Net(s):
Stripe Layer:
Metal6(6)
Width:
0
Pitch:
0
Secondary Pin Rail Layer
Metal6(6)
OK
Apply
Defaults
Cancel
Help

SRoute - Advanced - Secondary Power Pins Fields and Options

Net(s)	Specifies the nets belonging to the secondary pins you want to connect.
Stripe Layer	Defines the stripe layer on which secondary power pins should be connected. *Default*: If you turn this option off, the software uses the preferred layer.
Secondary Pin Rail Layer	Specifies the layer on which you want to connect the secondary pins.
Secondary Pin Alignment Check	Checks the alignment of secondary pins, and if they aligned, creates rails to connect them. The tool connects unaligned secondary pins individually.

Related Text Commands

For information on the following command, see "Power Route Commands" in the *Text Command Reference* document.

`setViaGenMode`

SRoute - Via Generation

Use the Via Generation page of the SRoute form to limit the connections that vias generated by SRoute are allowed to make.

To open the Via Generation page of the SRoute form, choose *Route* - *Special Route* , then click the *Via Generation* tab.

> ⓘ The following information applies to users who modify the existing set of valid target objects on the *Target List Editing page* (SRoute form, *Advanced* tab) and then open the *Via Generation* tab to make further changes to that set of objects: When you open the *Via Generation* tab of the SRoute form to make modifications on that tab, the via generation modifications you make apply *only* to the set of objects that you have modified on the *Target List Editing* page.

SRoute - Via Generation Fields and Options

Specify Layer Ranges
Crossover Connection

	The range of layers in which vias are created to connect wires that cross over the route. Vias are not created to connect wires outside this range. Select a layer from each of the following pulldown menus:	
	Top Stack Via Layer	
		The highest layer in which vias can be stacked. The default is the top-most metal layer.
	Bottom Stack Via Layer	
		The lowest layer in which vias can be stacked. The default is the bottom-most metal layer.
Target Connection		
	The range of layers in which vias are created to connect wires that reach the route. Vias are not created to connect wires outside this range. Select a layer from each of the following pulldown menus:	
	Top Stack Via Layer	
		The highest layer in which vias can be stacked. The default is the top-most metal layer.
	Bottom Stack Via Layer	
		The lowest layer in which vias can be stacked. The default is the bottom-most metal layer.
Check Standard Cell Geometry		
	If selected, checks the standard cell geometries in the design for any spacing violations between the power rail to power stripe vias and cell blockages to repair any DRC violations. When detected, Innovus repairs these violations by trimming the via arrays as needed. This check box is off by default.	
Split vias longer than X into smaller vias with center-to-center step of Y and bottom/left edge offset of Z		

	Splits vias that are longer than the specified length into smaller vias that have the specified center-to-center step and bottom/left edge offset (all values in micrometers). *Default*: Off
Make via connections to	
	Controls the wire shapes for which the software can generate vias. Select or deselect any of the following shapes: • *Pad ring/pin* • *Core ring* • *Block pin* • *Stripe* • *Block ring* • *Cover macro pin* • *No shape* By default, vias can be generated on all wire shapes.

Related Text Commands

For information on the following command, see "Power Route Commands" in the *Text Command Reference* document.

`sroute`

NanoRoute

Use the NanoRoute™ forms to specify the following:

- Net attributes
- Most commonly used run-time options
- Routing type (global, detailed, or both)
- Congestion map style and options

The *NanoRoute* submenu contains the following items:

- Specify Attribute
  Opens the *Route Attributes* form.
- Route
  Opens the *NanoRoute* form.
- Analyze Congestion
  Opens the *Analyze Congestion* form.

Specify Attribute

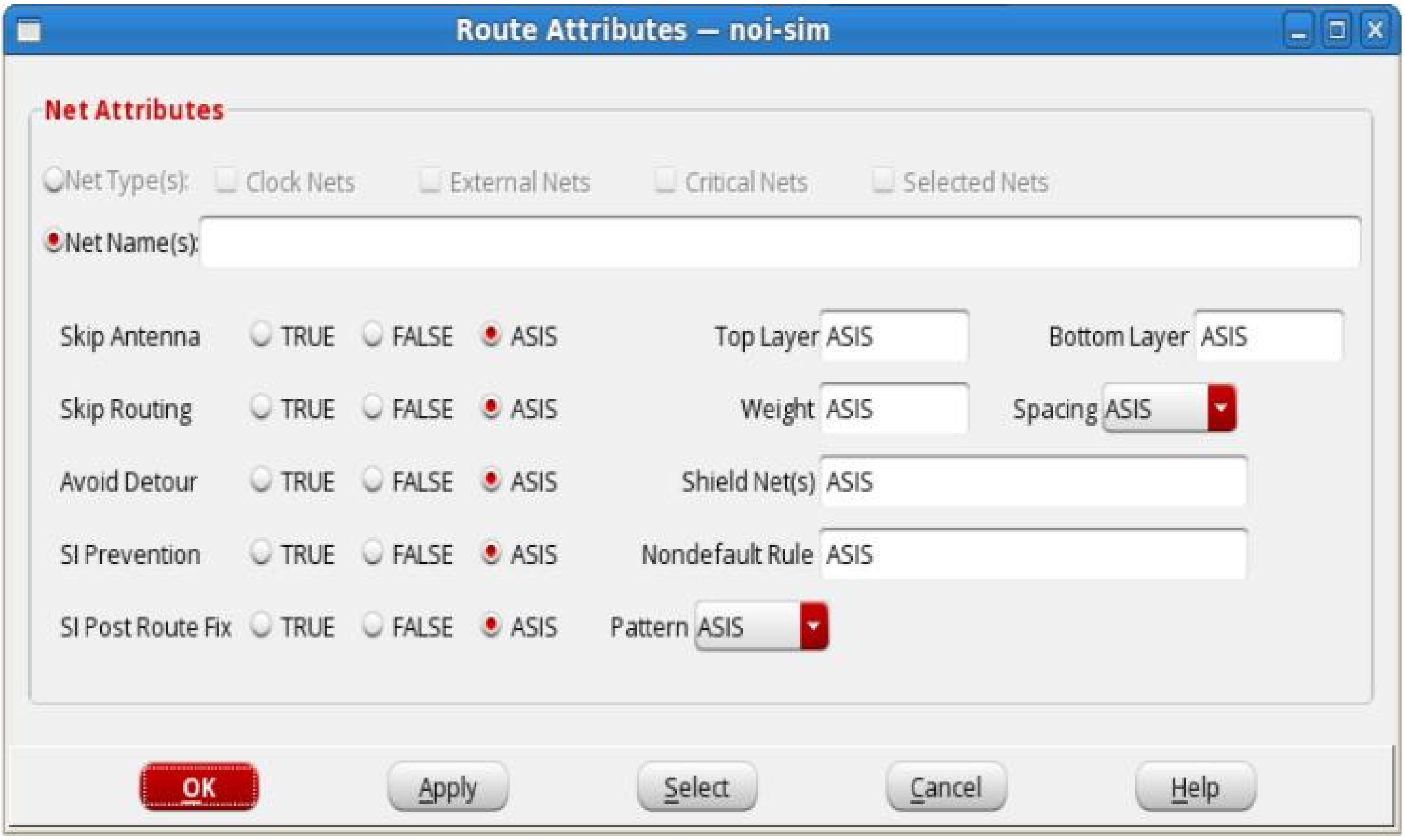
Use the *Specify Attribute* menu item to access the *Route Attributes* form.

Route Attributes

Using the *Route Attributes* form, you can specify net attributes to use when you route your design. Specifying net attributes is optional.

Attaching the attributes allows the router to route the nets following specific requirements. Attributes are persistent; that is, throughout the routing process, from global routing to optimization, the router honors the attributes. The attributes are saved with the Innovus database. If you save the database and exit, the attributes remain attached to the nets when you re-import the database. Attributes are not saved with the DEF file.

- Do one of the following:
  - Choose *Route - NanoRoute - Specify Attribute* on the menu.
  - Choose *Route - NanoRoute - Route* on the menu, and click the *Attribute* button on the *NanoRoute* form.
  - Choose *Route - Early Global Route* on the menu, and click the *Set Attribute* button on the *Early Global Route* form.



Route Attributes Fields and Options

Note: When *ASIS* is selected for a net attribute, the router does not change the current value of the attribute in the database. To see the current value of an attribute, use the `getAttribute` text command.

Net Type(s)	Specifies the net type(s). Select one or more of the following types:	
	Clock Nets	Specifies all clock nets.
	External Nets	Specifies all nets with external pins.
	Critical Nets	Specifies all timing-critical nets. If you select *Critical Nets*, you must have already run timing analysis to determine the nets that are timing critical.

	Selected Nets	Sets attributes for selected nets only.
Net Name(s)	Specifies nets. You can only specify one net name. To select more than one net, you can use the asterisk (`*`) and question mark (`?`) wildcards in this field. • If you select a *Net Type*, sets attributes for nets of that type only. • If you click *Select* at the bottom of the form, selects the nets in the design display area of the Innovus main window.	
Skip Antenna	Prevents the router from repairing process antenna violations on specified nets. This attribute is useful on nets that will have antenna violations repaired at the next level of hierarchy.	
Skip Routing	Prevents the router from routing or rerouting unrouted or partially routed nets. When you specify this option for a net, the router treats the net as if you had marked it `+ FIXED` in the DEF file and it becomes an obstruction for other nets. If the net is partially routed, the router does not complete the routing. **Note:** The value you specify with this attribute also applies to Early Global Route and the `earlyGlobalRoute` command.	
Avoid Detour	Routes critical nets as short as possible. When you set this attribute, the router does not allow a net to go beyond the minimum bounding box of all of its pins. ***Do not unnecessarily specify TRUE for this attribute because it adds congestion to the design.***	
SI Prevention	Prevents signal integrity violations by setting attributes for specified nets to avoid detours, add net weight, and add extra spacing. **Note:** You can specify the *SI Prevention* attribute for a net, even if you do not run signal integrity-driven routing.	

	Select *True* to set the following attributes for clock nets: • *Avoid Detour True* • *Weight* `10` • *Extra Spacing* `1`
	Select *True* to set the following attributes for nets with external pins: • *Avoid Detour True* • *Weight* `5` • *Extra Spacing* `1`
	Select *True* to set the following attributes for timing-critical nets: • *Avoid Detour True* • *Weight* `5` • *Extra Spacing* `1`
SI Post Route Fix	Repairs crosstalk violations after routing. If you are using a third-party tool for noise analysis, use this attribute to specify nets to target during for postroute crosstalk repair, in combination with the *Post Route SI* option on the NanoRoute form.
Top Layer	Specifies the highest layer for routing specified nets. NanoRoute might still use a layer above the specified layer if necessary to complete the routing. Use this attribute to improve timing by restricting the routing layers available for critical nets, while simultaneously routing other nets on all routing layers. *Range:* `0-15` **Note:** This is a soft limit. To set a hard limit, use *Top Layer* on the NanoRoute form.

Bottom Layer	Specifies the lowest routing layer. This attribute is a soft limit; that is, NanoRoute might use a layer below the specified layer if necessary to complete routing. To set a hard limit, use *Bottom Layer* on the NanoRoute form. *Range:* `0-15` **Note:** If the top routing layer is equal to or greater than 4 and no bottom preferred routing layer is specified for clock nets, the router automatically sets the bottom preferred routing layer for clock nets to 3, to prevent the clock nets from blocking other nets.
Weight	Specifies a relative weight for routing nets within a switch box. NanoRoute routes nets with the highest weight first, then the next highest weight, and so on. *Default:* `2` **Note:** A switch box is a collection of global routing cells used during detailed routing. When you specify a net weight and route a net, NanoRoute does not route the entire net according to the weight. It routes the nets in each switch box with the highest weight first, then the next highest weight, and so on.
Spacing	Gives one or more additional pitch spacing to specified nets. NanoRoute bases the spacing on the default spacing rule defined in the LEF file plus the extra pitch defined by this attribute. For example, specify `1` to give a net 1 extra pitch spacing, compared to other nets. This parameter creates a soft rule and, if the design is congested, might not give the extra space to the net. Use this attribute to space specific nets, such as clock nets, farther apart if they are very sensitive to coupling capacitance. *Range:* `0-3`
Shield Net(s)	Specifies a special net to use as a shield for a critical or high-speed net. Typically, you route shielded nets before routing other nets. You can specify one or two shield nets, however, you cannot control which side is used by the special net that is routed on the same layer as the signal routing. The shield terminates near the pin. Shielding information is saved in the DEF file.

Nondefault Rule	Identifies the nondefault routing rule to use with the specified net. Use this attribute for critical nets, such as clock nets, that might need to have wider wires or wider spacing than other nets. The router treats nondefault rule spacing as a soft attribute; that is, when routing resources are available, it honors the nondefault rule. If the area is too congested, and resources are not available, the router might not honor nondefault spacing rules. You can override this behavior by specifying `setNanoRouteMode -routeStrictlyHonorNonDefaultRuleroute_design_strict_honor_route_rule true` You define nondefault routing rules in the `NONDEFAULTRULE` statement of the LEF file.	
Pattern	Specifies the routing pattern. Select one of the following:	
	ASIS	Retains the current setting.
	steiner	Routes all pins with a single steiner tree.
	trunk	Routes pins to the nearest special net of the same name. Creates multiple steiner trees and connects them to the trunk.
Select	Selects nets in the design display area of the Innovus main window.	

Related Text Commands

- `getAttribute`
- `setAttribute`

Related Topics

- For information on Route commands, see Route Commands in the *Text Command Reference*.
- For information on the NanoRoute Router, see *Using the NanoRoute Router* in the *User Guide*.

Route

Use the *Route* menu item in the *NanoRoute* submenu to open the NanoRoute form.

- Choose *Route - NanoRoute - Route*.

NanoRoute

Use the NanoRoute form to specify the most commonly used NanoRoute run-time options, and to run global and detailed routing.

NanoRoute Fields and Options

Global Route	Plans the global interconnect and detailed routing for the design using the NanoRoute router, and produces a congestion map. During global routing, the router breaks the design into rectangles called global routing cells (gcells). It connects the regular nets defined in the `NETS` section of the DEF file by assigning them to gcells. The goals of global routing are to distribute and minimize congestion and to minimize the number of gcells that have more nets assigned than routing resources available.	
Detail Route	Uses the NanoRoute router to perform detailed routing on the entire design, on an area of the design specified, or on selected nets. During detailed routing, the router follows the global routing plan and lays down actual wires that connect the pins to their corresponding nets. The primary goal of detailed routing is to complete the interconnect without creating shorts or spacing violations. **Note:** If you have not already run detailed routing on the entire design, you cannot run detailed routing on a specified area. For more information, see Area Route.	
	End Iteration	Specifies the last pass in a detailed routing step or the beginning of postroute optimization. **Note:** Setting *End Iteration* to a value higher than 20 generally does not improve results.
Post Route Optimization		
	Replaces single-cut vias with multiple-cut vias or fat single-cut vias after postroute optimization.	
	Optimize Via	Optimizes vias after routing.
	Exercise caution with the use of this option, as the router might create violations during postroute via optimization. It runs a search and repair step after optimization if violations occur.	
	Optimize Wire	Optimizes wires after routing.

Concurrent Routing Features		
Fix Antenna	Repairs process antenna violations during postroute optimization. NanoRoute repairs process antenna violations if it can do so without creating design rule violations. The router might need to make several passes before repairing all antenna violations. By default, this option is selected.	
Insert Diodes	Inserts and places antenna diode cells during postroute optimization if there are available placement locations for the cells. By default, NanoRoute repairs antenna violations by changing layers (also called antenna stapling or layer hopping), but it can also repair antenna violations by inserting diodes as close as possible to input gates to discharge current. By default, this option is not selected.	
	Diode Cell Name	
		Routes antenna diode cells with the specified name during postroute optimization. The antenna diode cells must have the same LEF `SITE` definition as the standard cells. If you select *Insert Diodes* and do not enter a cell name, NanoRoute searches the LEF file and inserts the first `MACRO` with `CLASS CORE ANTENNACELL` it finds with the appropriate `SITE` definition.
Timing Driven	Minimizes timing violations by analyzing the timing slack for each path, the drive strengths of each cell in the library, and the maximum capacitance and maximum transition limits. During timing-driven routing, NanoRoute routes multi-pin nets to the most critical sink first, performs wire optimization by reducing resistance and coupling, and continually adjusts detouring. By default, this option is not selected.	
	Effort	Specifies how aggressively the router works to meet timing constraints. A higher value increases the effort toward meeting timing constraints and decreases the effort toward relieving congestion. *Range: 0 - 10* *Default:* Dynamic default setting

<table>
<tr><td>S.M.A.R.T.</td><td colspan="2">Abbreviation for Signal integrity, Manufacturing Awareness, Routability, and Timing.

During SMART routing, the router runs both timing-driven and signal integrity-driven routing concurrently. It uses the Innovus software's extraction, delay calculation, and timing engines during detailed routing to make intelligent trade-offs between routability, timing, and crosstalk minimization.</td></tr>
<tr><td>SI Driven</td><td colspan="2">Prevents or reduces crosstalk. Works in conjunction with timing-driven routing. By default, this option is not selected.
When Timing Driven is selected, uses SMART routing to identify victim nets and minimize crosstalk by wire spacing, layer hopping, net ordering, and minimizing the use of long parallel wires.
When Timing Driven is not selected, uses an older signal integrity engine to identify victim nets and minimize crosstalk by preventing or reducing the use of long parallel wires.</td></tr>
<tr><td>Post Route SI</td><td colspan="2">After routing and signal integrity analysis, uses information from a file that contains a list of victim nets to change the routing topology, including layer assignments, spacing, and location, to prevent coupling to other nets. Specify the file with Use SI Victim File. Postroute signal integrity repair requires both global and detailed routing. By default, this option is not selected.

Note: This option applies to nets with the SI Post Route Fix attribute set to True.</td></tr>
<tr><td></td><td>SI Victim File</td><td>Specifies a file from a crosstalk analysis tool, such as the CeltIC™ crosstalk analyzer for cell-based designs, that contains a list of nets with crosstalk problems.</td></tr>
<tr><td>Litho Driven</td><td colspan="2">Avoids lithography problems during routing by avoiding certain routing patterns that might lead to the creation of lithography hotspots.

Default: Off</td></tr>
<tr><td>Routing Control</td><td colspan="2"></td></tr>
</table>

Selected Nets Only	Specifies whether NanoRoute routes all nets at once or routes selected nets only. To route critical nets as short as possible, select the critical nets and select this option. By default, this option is not selected. When this option is selected, NanoRoute does the following: • Removes incomplete nets unless they are marked `+ FIXED` or have a `-skip_routing` net attribute. • Routes the remaining selected nets.
Bottom Layer	Specifies the lowest layer the router uses for global and detailed routing. If the design has pins below the layer specified by this parameter, and if the tracks for the in-between layers are aligned to allow stacked vias to be dropped directly on top of the pins, the router uses stacked vias. However, if the tracks are not aligned, the router adds a short piece of wire before dropping a via to go to the next layer. *Default: 1* **Note:** To set a soft limit, use the *Bottom Layer* attribute.
Top Layer	Specifies the highest layer NanoRoute uses for global and detailed routing. This option sets a hard limit, that is, NanoRoute does not route nets above the specified layer. The default value is the number of the highest routing layer specified in the LEF `LAYER` (Routing) statement. For example, setting the value to `4` means no wires will be routed on any layer above *metal4*: The global and detailed routers will use *metal1*, *metal2*, *metal3*, and *metal4*. **Note:** To set a soft limit, use the *Top Layer* attribute.
ECO Route	Specifies engineering change order (ECO) mode. During ECO mode, NanoRoute completes partial routes with added logic, while maintaining the existing wire segments as much as possible. **Note:** Select *ECO Route* only if you are running both global and detailed routing.
Area Route	Repairs violations in a local area after global and detailed routing. If you move any cells after routing, you must rerun global and detailed routing before running *Area Route*. By default, this option is not selected. **Note:** If you select *Area Route* and the design is not already routed, *Area Route* will route the entire design and issue a warning in the log file.

	Area	Specifies the area to route.
	Select Area and Route	Lets you select the routing area when you click and drag the mouse in the design display area of the Innovus main window.
Job Control		
Auto Stop	Controls whether NanoRoute continues routing if there are many violations. In highly congested designs, NanoRoute stops if the number of violations is too high. If you deselect this option, NanoRoute continues routing until there is no improvement. By default, this option is selected.	
Number of Thread(s) For Multiple Threaded		
	Displays the maximum number of threads for multi-threaded routing. This is a view-only field.	
Number of Thread(s) For Superthreaded		
	Displays the maximum number of threads for Superthreading. This is a view-only field.	
Number of Host(s) for Superthreaded		
	Displays the maximum number of hosts for Superthreading. This is a view-only field.	
Set Multiple CPU …	Opens the Multiple CPU Processing form. Use this form to configure multi-threading and Superthreading.	
Attribute	Opens the NanoRoute/Attributes form.	
Mode	Opens the NanoRoute page of the *Mode Setup* form.	
Save	Lets you save the router's option settings, so you can load them later. Opens the Save As form. For information, see File Menu.	
Load	Loads a previously saved file with NanoRoute option settings. Opens the Open form. For information, see File Menu.	

Related Text Commands

- `add_tracks`
- `detailRoute`
- `globalDetailRoute`
- `globalRoute`
- `setNanoRouteMode`

Related Topics

- For information on Route commands, see Route Commands in the *Text Command Reference*.
- For information on the NanoRoute Router, see *Using the NanoRoute Router* in the *User Guide*.

Analyze Congestion

Use the *Analyze Congestion* menu item in the *NanoRoute* submenu to open the *Congestion Map* form. Use the *Congestion Map* form to display congestion in the design after running Early Global Route or running global routing with the NanoRoute router. You can change the way congestion is displayed by selecting options on the form.

The *Congestion Map* form displayed depends on the type of routing that was performed.

- If you ran Early Global Route, or have a Early Global Routed design saved in the database, the software displays the Early Global Route version of the form.
- If you ran NanoRoute, or have a global-routed design saved in the database, the software displays the NanoRoute version of the form.

The *Congestion Map* form has two pages:

- Congestion Map - EarlyGlobalRoute
- Congestion Map - NanoRoute/WRoute

Note: The *Congestion Map* form is dockable and detachable. You can move the form to make more space in the main window. Alternatively, you can dock the from back to the main window.

The Load and Save buttons on each page of the form provide access to the following forms:

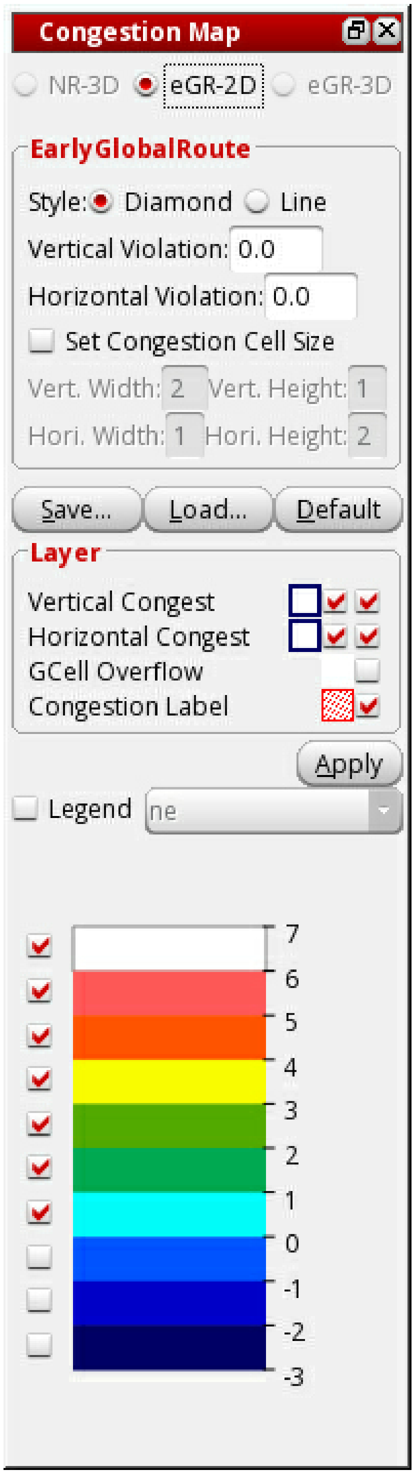
- Load: Load Preference File
- Save: Save Preference

Congestion Map - EarlyGlobalRoute

Use the *Congestion Map - EarlyGlobalRoute* form after running Early Global Route to see a graphical representation of routing congestion in the design. You can display congestion information using the default Early Global Route map style or the map style used by the global router.

Note: To change the display, you must click *OK* to close the form.

- Choose *Route - NanoRoute - Analyze Congestion*.



Congestion Map (EarlyGlobalRoute) Fields and Options

<table>
<tr><td>NR-3D</td><td colspan="2">Displays the Nanoroute congestion in 3D layout.
Note: GUI will draw 3D map first. If there is no 3D map, then it draws the 2D map. When 2D and 3D maps co-exist, the 2D option is not shown.</td></tr>
<tr><td>eGR-2D</td><td colspan="2">Displays the Early Global Route congestion in 2D layout.</td></tr>
<tr><td>eGR-3D</td><td colspan="2">Displays the Early Global Route congestion in 3D layout.</td></tr>
<tr><td>Style</td><td colspan="2">Specifies the display style.
Default: Diamond</td></tr>
<tr><td></td><td>Diamond</td><td>Displays routing congestion using the default Early Global Route map style. If you select diamond, you can choose whether to display horizontal congestion, vertical congestion, or both. Overflow Setting values do not apply.</td></tr>
<tr><td></td><td>Line</td><td>Displays routing congestion using the global router map style. If you select line, you can choose whether to display horizontal congestion, vertical congestion, or both. You can also specify different Overflow Setting values.</td></tr>
<tr><td colspan="3">Vertical Violation / Horizontal Violation</td></tr>
<tr><td></td><td colspan="2">Set the range for vertical and horizontal route congestion display. The default value of <code>0.0</code> displays vertical and horizontal route-demand congestion values close to or greater than the vertical and horizontal route-resource value.
Vertical and horizontal violation values are the numbers in the diamond-shaped congestion symbols. Changing the value to a high value, such as <code>20.0</code>, can be used to display severe congestion symbols where the route-demand exceeds the route-resource by 20 or greater. Changing the value to a negative value, such as <code>-5.0</code>, will display several more congestion symbols where the route-demand is less than the route-resource by 5 or greater.
Default: <code>0.0</code></td></tr>
<tr><td>Set Congestion Cell Size</td><td colspan="2">Select to specify the congestion cell size.</td></tr>
</table>

	Vert. Width	Specify the vertical width of the congestion cell.
	Vert. Height	Specify the vertical height of the congestion cell.
	Hori. Width	Specify the horizontal width of the congestion cell.
	Hori. Height	Specify the horizontal height of the congestion cell.
Legend	Displays legends in the congestion map on the layout. You can change the location of legend by using the drop-down menu next to *Legend*. In the listed location options, *ne* means north east, *nw* means north west and so on. *Default*: ne	
Layer		
Vertical Congest		
	Displays vertical congestion. Corresponds to the *VCongest* visibility toggle in the main Innovus window. **Note**: Vertical lines display vertical routing congestion.	
Horizontal Congest		
	Displays horizontal congestion. Corresponds to the *HCongest* visibility toggle in the main Innovus window. **Note**: Horizontal lines display horizontal routing congestion.	
GCell Overflow	Displays different levels of congestion in the map by assigning specified colors to specified overflow values. Overflow is the number of tracks required for routing minus the number of tracks that are available in a particular gcell. A negative number indicates that there are more tracks available than required. A positive number indicates that more tracks are required than available.	
Congestion Label	Displays the congestion label color and visibility.	

Apply	Click to apply the settings.
Legend	Displays legends in the congestion map on the layout. You can change the location of legend by using the drop-down menu next to *Legend*. In the listed location options, *ne* means north east, *nw* means north west and so on. *Default*: ne

Related Topics

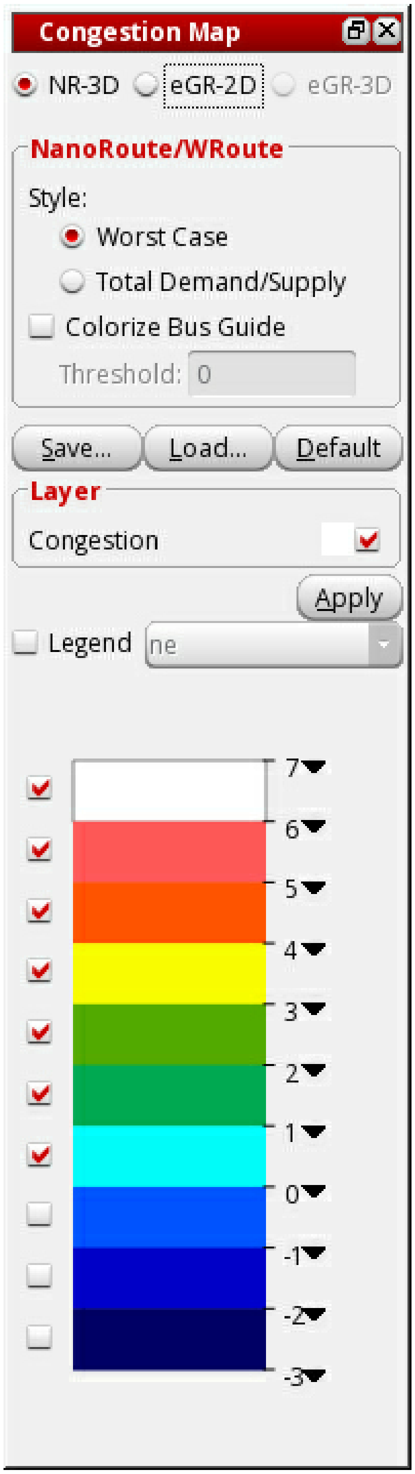
- For information on Route commands, see Route Commands in the *Text Command Reference*.
- For information on the NanoRoute Router, see *Using the NanoRoute Router* in the *User Guide*.

Congestion Map - NanoRoute/WRoute

Use the *Congestion Map - NanoRoute/WRoute* form after running global routing to customize the congestion map. You can select options to display congestion on all visible layers or on the most-congested visible layer only.

Note: To change the display, you must click *Apply* to close the form.

- Choose *Route - NanoRoute - Analyze Congestion*.



Congestion Map (NanoRoute/WRoute) Fields and Options

NR-3D	Displays the Nanoroute congestion in 3D layout. **Note**: GUI will draw 3D map first. If there is no 3D map, then it draws the 2D map. When 2D and 3D maps co-exist, the 2D option is not shown.	
eGR-3D	Displays the Early Global Route congestion in 3D layout.	
eGR-2D	Displays the Early Global Route congestion in 2D layout.	
Style	Specifies the display style. *Default: Worst case*	
	Worst case	Bases the map on visible layer with the worst congestion.
	Total Demand/Supply	Bases the map on the total demand (tracks required to complete global routing) and supply (total tracks available for global routing) on all visible layers.
Colorize Bus Guide	Select to colorize bus guides and specify the *Threshold* value.	
Congestion	Turns congestion on or off. Corresponds to the *Congestion* visibility toggle in the main Innovus window.	
Apply	Click to apply the settings.	
Legend	Displays legends in the congestion map on the layout. You can change the location of legend by using the drop-down menu next to *Legend*. In the listed location options, *ne* means north east, *nw* means north west and so on. *Default*: ne	

Related Topics

- For information on Route commands, see Route Commands in the *Text Command Reference*.
- For information on the NanoRoute Router, see *Using the NanoRoute Router* in the *User Guide*.

Metal Fill

Use the metal fill forms to create or trim metal fill automatically, based on the constraints specified in the LEF file or the values you specify on the forms.

The *Metal Fill* submenu contains the following items:

- *Setup*
  Opens the Setup Metal Fill Options form.
- *Add*
  Opens the Add Metal Fill form.
- *Trim*
  Opens the Trim Metal Fill form.
- *Delete*

  Opens the Delete Metal Fill form.

Setup

Use the *Setup* command in the Metal Fill submenu to access the Setup Metal Fill Options form, which enables you to set options for adding or trimming metal fill.

Setup Metal Fill Options

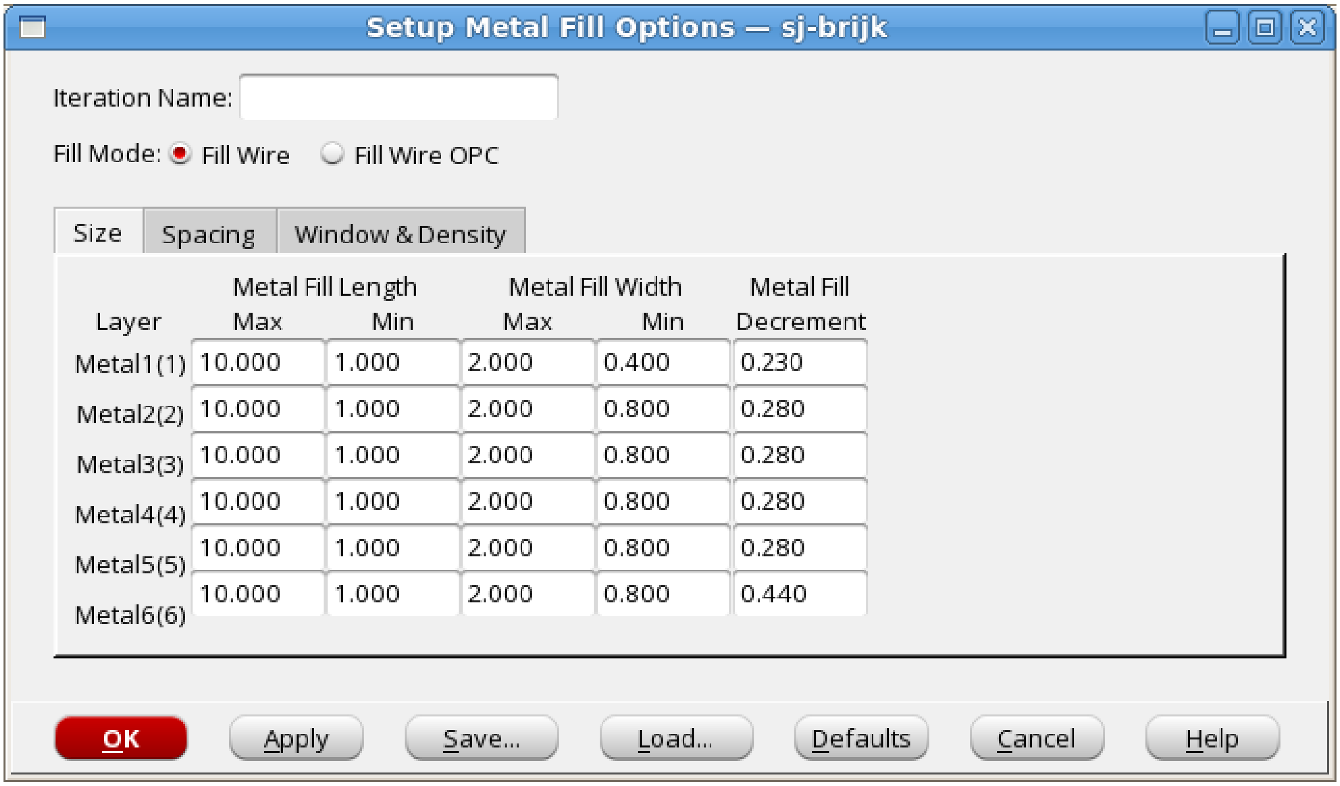
The Setup Metal Fill Options form contains the following pages:

- Setup Metal Fill Options - Size
- Setup Metal Fill Options - Spacing
- Setup Metal Fill Options - Window & Density

Setup Metal Fill Options - Size

Use the *Size & Spacing* page of the Setup Metal Fill Options form to specify the size of metal fill segments.

- Choose *Route* - *Metal Fill* - *Setup*, then click the *Size* tab if it is not already open.



Setup Metal Fill Options - Size and Spacing Fields and Options

Note: For each of the following options, you can specify different values for each layer.

<table>
<tr><td>Iteration Name</td><td colspan="2">Specifies a name for a set of values for metal fill options that the software stores and uses when it adds metal fill.

Window size and step must be the same for all iterations of a specific layer.</td></tr>
<tr><td>Fill Mode</td><td colspan="2">Specifies whether the metal fill will go through the optical proximity correction (OPC) process.
Default: Fill Wire</td></tr>
<tr><td></td><td>Fill Wire</td><td>Specifies metal fill that will not go through the OPC process.</td></tr>
</table>

<table>
<tr><td></td><td>Fill Wire OPC</td><td>Specifies metal fill that will go through the OPC process. This fill can be smaller than non-OPC metal fill and is governed by the same design rules as regular wires, instead of the rules that govern non-OPC metal fill.
OPC metal fill that is floating (unconnected) is included in the Fills statement of DEF 5.7.
OPC metal fill that is tied off (connected) is included in the Special Wiring statement of DEF 5.7.
For more information, see the DEF Syntax chapter in the LEF/DEF Language Reference.
The GDSII map file identifies the following object names for OPC and non-OPC metal fill: FILL, FILLOPC, VIA, VIAFILL.

For more information, see "GDSII Map File Format" in the Importing and Exporting Designs chapter of the Innovus User Guide.</td></tr>
<tr><td>Metal Fill Length Max</td><td colspan="2">Specifies the maximum length (in microns) of each metal fill segment.
Default: <code>10.0</code>

Note: Use this field only if you select the Rectangular shape option on the Add Metal Fill form.</td></tr>
<tr><td>Metal Fill Length Min</td><td colspan="2">Specifies the minimum length (in microns) of each metal fill segment.
Default: <code>1.0</code>

Note: Use this field only if you select the Rectangular shape option on the Add Metal Fill form.</td></tr>
<tr><td>Metal Fill Width Max</td><td colspan="2">Specifies the maximum width (in microns) of each metal fill segment.
Default: <code>2.0</code></td></tr>
<tr><td>Metal Fill Width Min</td><td colspan="2">Specifies the minimum width (in microns) of each metal fill segment.
Default: <code>0.4</code> on thin layers (less than 0.24 microns); <code>0.8</code> on thick layers</td></tr>
</table>

Metal Fill Decrement	Specifies the number of microns used to decrease the size of each successively smaller segment of metal fill until the *Metal Fill Width Min* size is reached. Use this field to control the number of different sizes of metal fill in the design. The software uses the maximum metal fill size specified unless it is impossible to fit a piece of metal fill into a particular area. The software then attempts to use successively smaller pieces of metal fill until the *Metal Fill Width Min* value is reached. For example, if the *Metal Fill Width Max* value is `8`, the *Metal Fill Width Min* value is `4`, and the *Decrement* value is `2`, then metal fill with widths of `8`, `6`, and `4` are used. However, to give the software more flexibility, you can change the *Metal Fill Decrement* value to a smaller value. If the *Metal Fill Decrement* value is `1`, metal fill with widths of `8`, `7`, `6`, `5`, and `4` can all be used. *Default:* `WIDTH` value specified in the `Layer` (Routing) statement of the LEF file **Note:** Use this field only if you select the *Square* shape option on the Add Metal Fill form.

Related Topics

- Specifying Metal Fill Parameters
- Specifying the Active Spacing Value

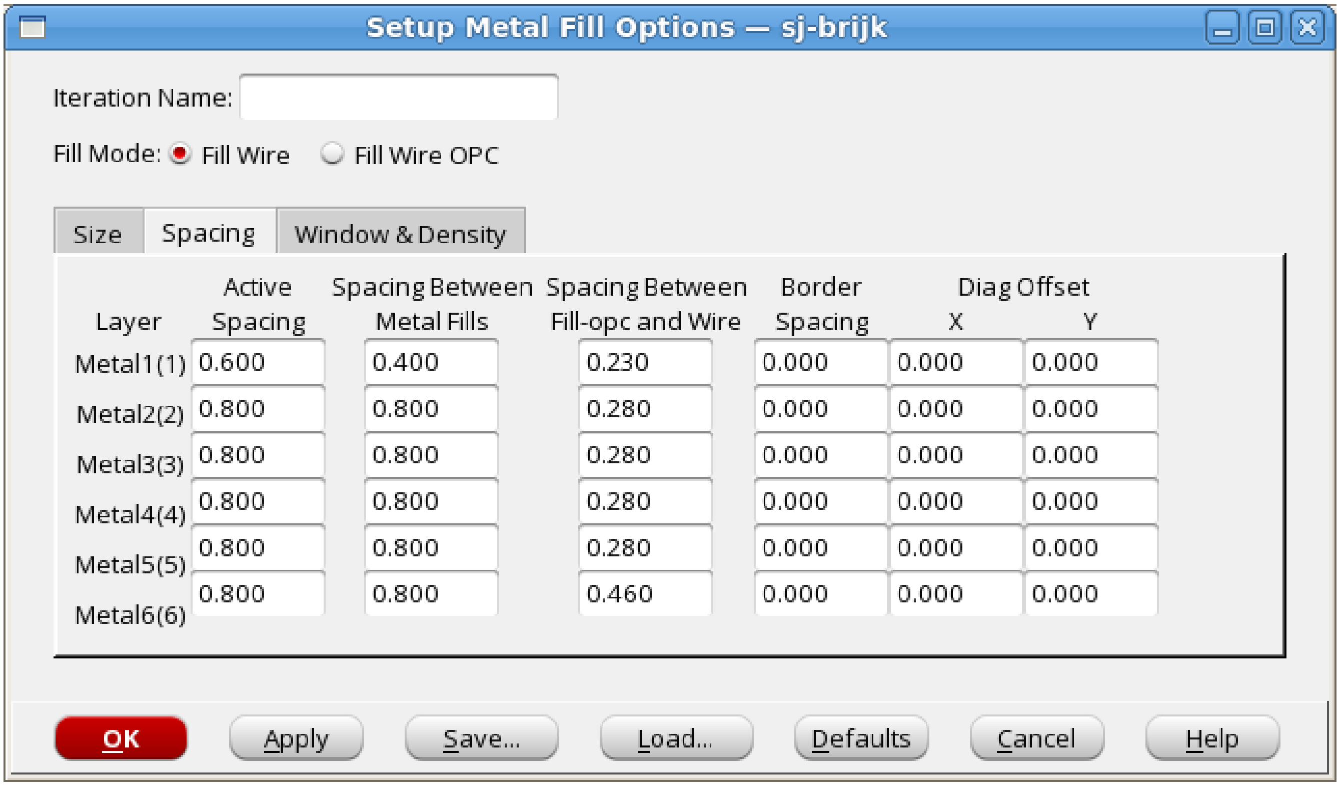
Related Text Commands

`setMetalFill`

Setup Metal Fill Options - Spacing

Use the *Spacing* page of the Setup Metal Fill Options form to specify the spacing requirements of metal fill segments.

- Choose *Route* - *Metal Fill* - *Setup*, then click the *Spacing* tab.



Setup Metal Fill Options - Spacing Fields and Options

Note: For each of the following options, you can specify different values for each layer.

Iteration Name		
	Specifies a name for a set of values for metal fill options that the software stores and uses when it adds metal fill. Window size and step must be the same for all iterations of a specific layer.	
Fill Mode	Specifies whether the metal fill will go through the optical proximity correction (OPC) process. *Default: Fill Wire*	
	Fill Wire	Specifies metal fill that will not go through the OPC process.

<table>
<tr><td></td><td>Fill Wire OPC</td><td>Specifies metal fill that will go through the OPC process. This fill can be smaller than non-OPC metal fill and is governed by the same design rules as regular wires, instead of the rules that govern non-OPC metal fill.
OPC metal fill that is floating (unconnected) is included in the Fills statement of DEF 5.7.
OPC metal fill that is tied off (connected) is included in the Special Wiring statement of DEF 5.7.

For more information, see the DEF Syntax chapter in the LEF/DEF Language Reference.
The GDSII map file identifies the following object names for OPC and non-OPC metal fill: <code>FILL</code>, <code>FILLOPC</code>, <code>VIA</code>, <code>VIAFILL</code>.

For more information, "GDSII Map File Format" in the Importing and Exporting Designs chapter of the Innovus User Guide.</td></tr>
<tr><td>Active Spacing</td><td colspan="2">Specifies the minimum distance (in microns) between a metal fill segment and any object in the design other than another metal fill segment.
Default: <code>FILLACTIVESPACING</code> value specified in the <code>LAYER</code> (Routing) statement of the LEF file. If not defined, <code>0.6</code> on thin layers (less than 0.24 microns); <code>0.8</code> on thick layers</td></tr>
<tr><td colspan="3">Spacing Between Metal Fills</td></tr>
<tr><td></td><td colspan="2">Specifies the minimum distance (in microns) between one metal fill segment and another metal fill segment.
Default: <code>0.4</code> on thin layers (less than 0.24 microns); <code>0.8</code> on thick layers</td></tr>
<tr><td colspan="3">Spacing Between Fill - opc and Wire</td></tr>
<tr><td></td><td colspan="2">Specifies the minimum distance in microns between the OPC metal fill shapes (FILLWIREOPC) and main patterns. This option is equivalent to <code>setMetalFill -opcActiveSpacing</code>.

Default: <code>0.6</code> on thin layers (less than 0.24 microns); <code>0.8</code> on thick layers</td></tr>
</table>

Border Spacing	Specifies the space in microns along the design border that needs to be kept free of metal fill. This option is equivalent to `setMetalFill -borderSpacing`. This option is useful if you want open space next to the place and route border. If you have set border spacing, the `addMetalFill` and `verifyMetalDensity` commands consider the density in the specified border space area as `0`. *Default:* `0.0`	
Diag Offset	Specifies the *X* and *Y* offsets for staggering metal fill. This option is equivalent to `setMetalFill -diagOffset`. *Default:* `0.0`	
	X	Specifies the horizontal offset.
	Y	Specifies the vertical offset.

Related Topics

- Specifying Metal Fill Parameters
- Specifying the Active Spacing Value

Related Text Commands

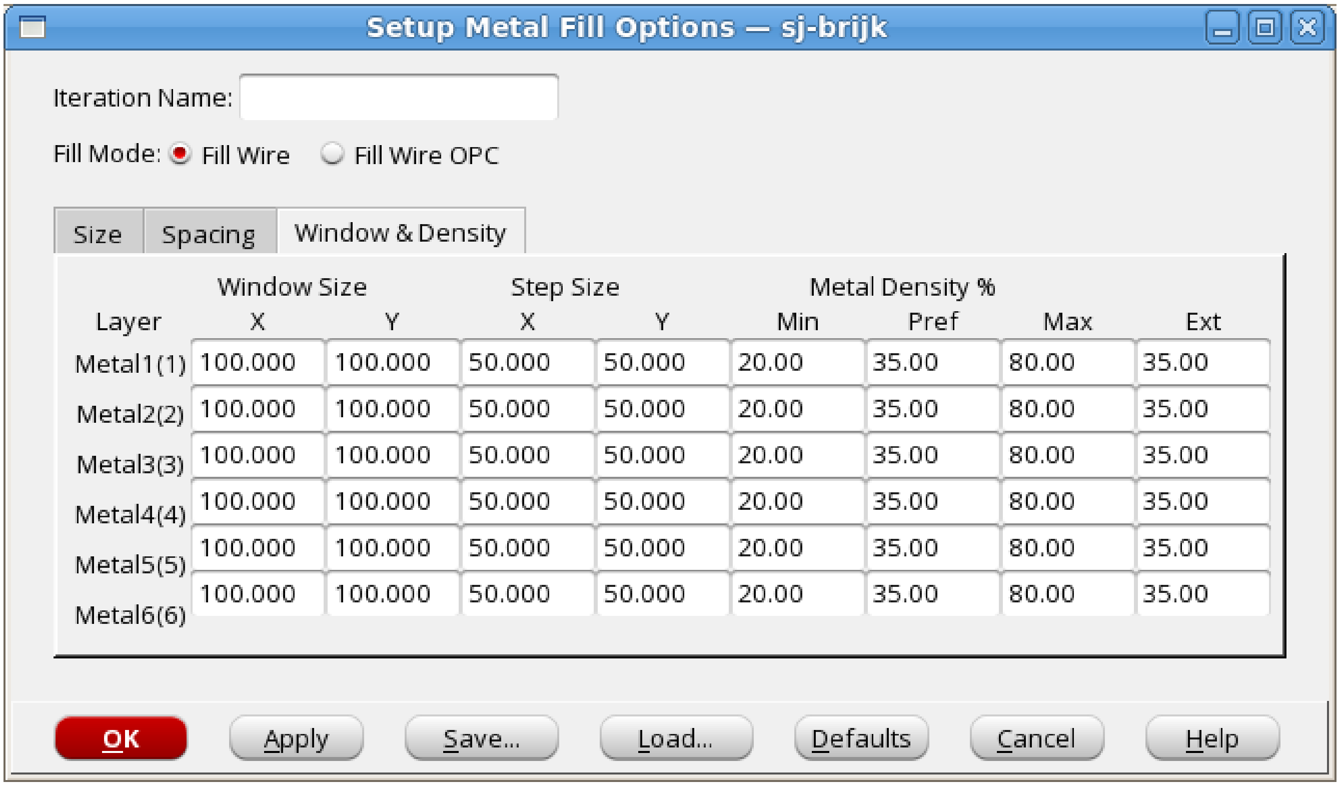
`setMetalFill`

Setup Metal Fill Options - Window and Density

Use the *Window & Density* page of the Setup Metal Fill Options form to specify the density for the metal fill, as well as the areas in which density is checked before metal fill is added. The software examines the metal density in each window and automatically inserts metal fill to achieve preferred density.

Note: If the metal density in a window exceeds the maximum metal density allowed in the LEF file, the software issues an error message.

- Choose *Route - Metal Fill - Setup*, then click the *Window & Density* tab.



Setup Metal Fill Options- Window and Density Fields and Options

Note: You can specify different values for the options for each layer.

Iteration Name	Specifies a name for a set of values for metal fill parameters that the software stores and uses later, when it adds metal fill. Window size and step must be the same for all iterations of a specific layer.
Fill Mode	Specifies the type of metal fill to add. Select one of the following types:
	Fill Wire Specifies metal fill that has not gone through the OPC process.

	Fill Wire OPC Specifies metal fill that has gone through the OPC process.
Window Size X	specifies the x dimension (width in microns) of the area used by the software to examine the metal density. The command assesses the metal density in each window, moving the window iteratively through the design. *Default:* `DENSITYCHECKWINDOW` value in the `LAYER` (Routing) statement of the LEF file. If not defined, `100.000`.
Window Size Y	Specifies the y dimension (height in microns) of the area this command uses to examine the metal density. The command assesses the metal density in each window, moving the window iteratively through the design. *Default:* `DENSITYCHECKWINDOW` value in the `LAYER` (Routing) statement of the LEF file. If not defined, `100.000`.
Step Size X	Specifies the x distance (width in microns) the window moves for each iteration of metal density analysis. The recommended value is half the value of the Window Size. *Default:* `DENSITYCHECKSTEP` in the LEF file. If not defined, `50.000`.
Step Size Y	Specifies the y distance (height in microns) the window moves for each iteration of metal density analysis. The recommended value is half the value of the Window Size. *Default:* `DENSITYCHECKSTEP` in the LEF file. If not defined, `50.000`.
Metal Density % Min	Specifies the minimum metal density allowed in the design. Changing this value overrides the value defined in the LEF file. The software checks for a conflict between the value you specify and the default density range defined in the LEF file. *Default:* `MINIMUMDENSITY` value of the `LAYER` (Routing) statement of the LEF file. If not defined, `20.000`.

Metal Density % Pref	Specifies a percentage value for the preferred metal density for the layer. When the metal density in a window is less than the minimum metal fill density value, adds metal fill to achieve a density slightly above the preferred density if possible. In addition, metal fill uses the preferred density value in the estimation of `MACRO` density for layers that have most of the `MACRO` covered by `OBS` shapes and for DEF `BLOCKAGES` without both `+ FILLS` and `+ PUSHDOWN`. Metal fill uses the following scheme for the treatment of DEF blockages with `+ FILLS` or `+ PUSHDOWN`: • DEF `BLOCKAGES` with `+ PUSHDOWN` = 100 percent density (the same as real metal segments) • DEF `BLOCKAGES` with `+ FILLS` = 0 percent density Cadence recommends modelling LEF `MACRO`s by using the `DENSITY` statement, with density windows that are smaller than the metal fill windows. For example, if the metal fill windows are 100 x 100, use 25 x 25 or smaller values for the density rectangles. *Default:* `35.00`
Metal Density % Max	Specifies the maximum metal density allowed in the design. Changing this value overrides the value defined in the LEF file. This command checks whether the value you specify conflicts with the default density range defined in the LEF file. *Default:* `MAXIMUMDENSITY` value of the `LAYER` (Routing) statement of the LEF file. If not defined, `80.000`.
Metal Density % Ext	Specifies the external metal density percentage for a layer when `addMetalFill`'s windows lie partially outside of the die area. For each layer, a different external density value can be specified.

Related Topics

- Specifying Metal Fill Parameters
- Specifying the Active Spacing Value

Related Text Commands

`setMetalFill`

Add

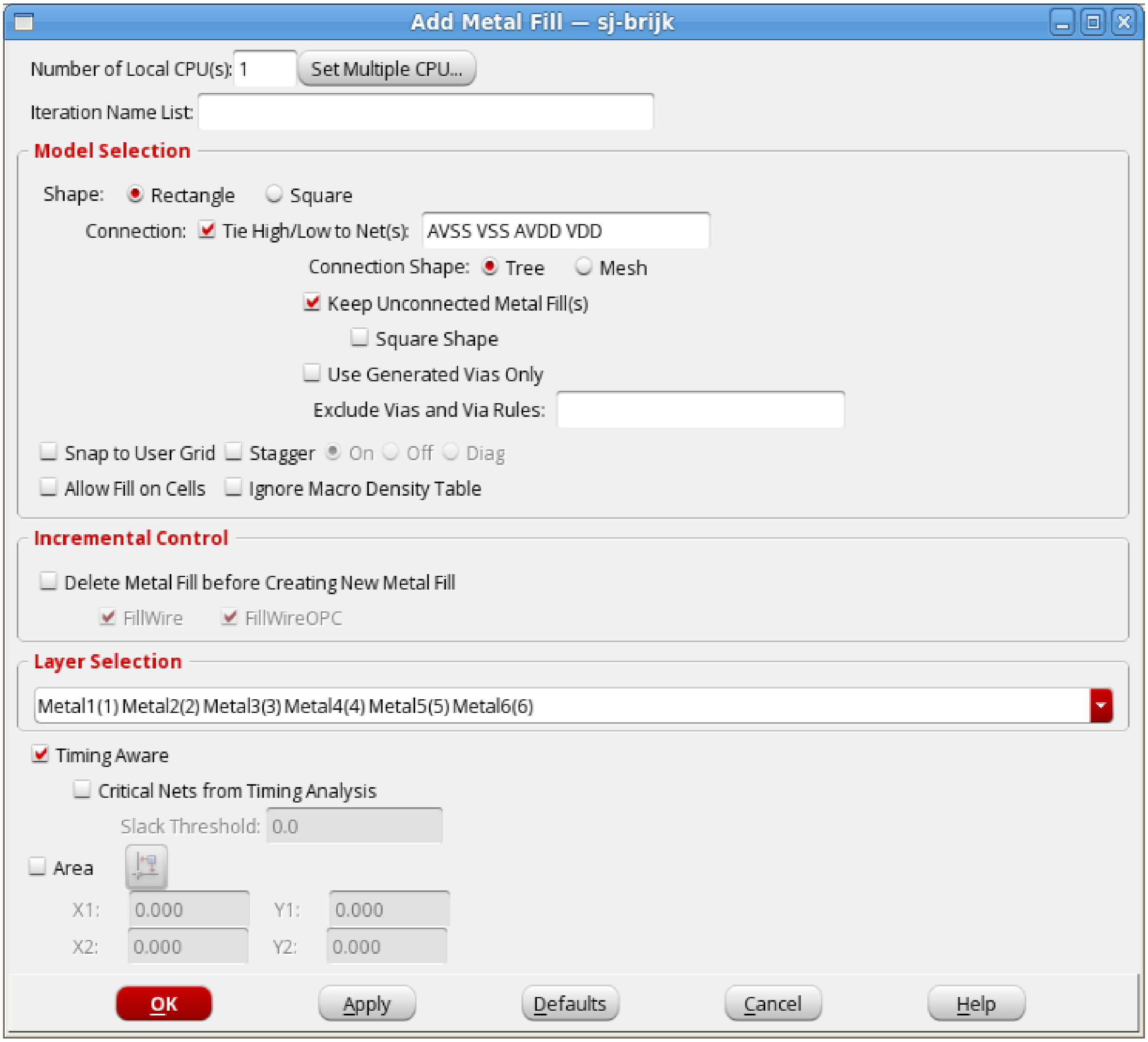
Use the *Add* command in the *Metal Fill* submenu to open the Add Metal Fill form.

Add Metal Fill

Use the Add Metal Fill form to specify how to perform the following operations:

  - Connect new metal fill
  - Specify whether to remove or retain existing metal fill
  - Select the layers on which to add metal fill
  - Specify an area within the design into which to add metal fill

- Choose *Route* - *Metal Fill* - *Add*.



Add Metal Fill Fields and Options

Number of Local CPU(s)	
	Displays the number of local CPUs used for multi-threading. This is a non-editable field. To change setting for multi-threading, click the *Set Multiple CPU* button.

Set Multiple CPU	Opens the Multiple CPU Processing form, where you can view or change settings for multi-threading and distributed processing.	
Iteration Name List	Specifies a list of iterations (specify the names on the Setup Metal Fill form) for adding metal fill. Processes the iterations in the order listed, and stops when the preferred density is reached in any iteration. When you add metal fill in iteration mode, it runs several times with just one invocation of `addMetalFill`, and uses the ending density from an iteration as the starting density of the next iteration. For that one invocation, the window size and step for a specific layer must be the same for all iterations.	
Shape	Specifies the shape of the metal fill. Select one of the following options:	
	Rectangle	Creates both rectangular and square metal fill. If you select this option, you can specify maximum and minimum width and height values on the Setup Metal Fill Options - Size page.
	Square	Creates only square metal fill. If you select this option, you can specify maximum and minimum width values, as well as a decrement value on the Setup Metal Fill Options - Size page.
Tie High/Low to Net(s):	Connects metal fill to the nets specified in the text entry field. List the nets in a priority order, because the software always attempts to connect metal fill segments to the first net in the list. Metal fill segments connect to other nets in the list if a connection to the first net in the list is not possible. *Default:* By default, this option is selected and the text entry field is automatically populated with the net names specified on the Design Import form. If deselected, metal fill is left floating.	
Connection Shape	Specifies whether metal fill is connected in a *Tree* or *Mesh* shape. *Default: Tree*	
	Tree	Connects metal fill shapes using the minimum number of via cuts. When *Tree* is selected, metal fill shapes do not carry current.

	Mesh	Connects metal fill shapes to the power mesh, allowing it to carry current as part of the power and ground structure. Uses the maximum number of cuts in vias at every intersection. Increasing the number of cuts helps to reduce IR drop.
Keep Unconnected Metal Fill(s):		
	Allows the creation of metal fill that is not connected to the nets specified by the *Tie High//low to Net(s)* option. If deselected, the software does not create unconnected metal fill segments. **Note:** This option is enabled when you select *Tie High/Low to N et(s)*.	
Square Shape	Adds unconnected metal fill that has a square shape. If deselected, the software can create both rectangular and square unconnected metal fill segments. This is the default. **Note:** This option is available only if you select *Tie High/Low to Net(s)* and *Keep Unconnected Metal Fill(s)*.	
Use Generated Vias Only	Specifies that only generated vias are used for metal fill connections. *Default:* Off	
Snap to User Grid	Snaps edges of metal fill shapes and centers of cuts to a user-defined snap grid. This option is equivalent to `addMetalFill -snap`.	
Stagger	Specifies the pattern for adding metal fill. This option is equivalent to `addMetalFill -stagger { on | off | diag}`. *Default*: Unchecked Select one of the following options:	
	On	Adds metal fill shapes in a staggered pattern in the preferred routing direction and in an aligned pattern in the non-preferred direction. This is the default option if *Stagger* is selected.
	Off	Adds metal fill shapes that line up in both the preferred and non-preferred routing directions, so that metal fill is not staggered.
	Diag	Adds metal fill shapes in a staggered pattern in both the preferred and non-preferred directions.

Allow Fill on Cells	Allows the software to add metal fill into `CLASS BLOCK` and `CLASS PAD` macro cells. Before adding the metal fill, make sure that the cells are at preferred density, because adding metal fill shapes inside the cells might lead to timing problems inside the cells. The software can always add metal fill to `CLASS CORE SPACER` cells, but can add it to `CLASS BLOCK` and `CLASS PAD` cells only when this option is specified. *Default:* Off
Ignore Macro Density Table	Ignores the MACRO DENSITY table in the LEF file and instead uses the default macro density calculation method. This option is equivalent to `addMetalFill -ignoreLEFDensity`. *Default:* Off
Delete Metal Fill before Creating New Metal Fill	
	Removes existing metal fill from a layer before creating more metal fill on that layer. *Default:* Off
Layer Selection	Specifies the metal layers for adding metal fill. Click *Deselect All Layers* to deselect all layers quickly. Click *All Layers* to select all layers quickly.
Timing Aware	Considers the impact of metal fill on timing. Minimizes cross-coupling while meeting preferred density targets when adding metal fill. Assigns costs to adding metal fill near power or ground nets (0 cost), signal nets (moderate cost), and clock nets (high cost) and minimizes costs when adding metal fill. If metal fill is added, the software adjusts the costs as a function of the slack (the worst slack has the highest cost).
Critical Nets from Timing Analysis	
	Uses the Innovus common timing engine (CTE) for static timing analysis. Further divides signal nets into non-critical nets (small cost) and critical nets (moderate cost).

	Slack Threshold	Specifies a slack threshold for timing-critical nets during timing-driven routing with CTE. Specify a small positive value, such as 100 nanoseconds, to give yourself a margin of safety. *Default:* `0.0`
Area	Restricts metal fill to the specified portion of the design. You can enter coordinates in the *X1*, *X2*, *Y1*, and *Y2* fields or click the *Draw* button and drag the mouse in the design area to populate the coordinate fields automatically. *Default:* Entire design area	

Related Topics

- Specifying Metal Fill Parameters

Related Text Commands

- `addMetalFill`
- `editDelete`

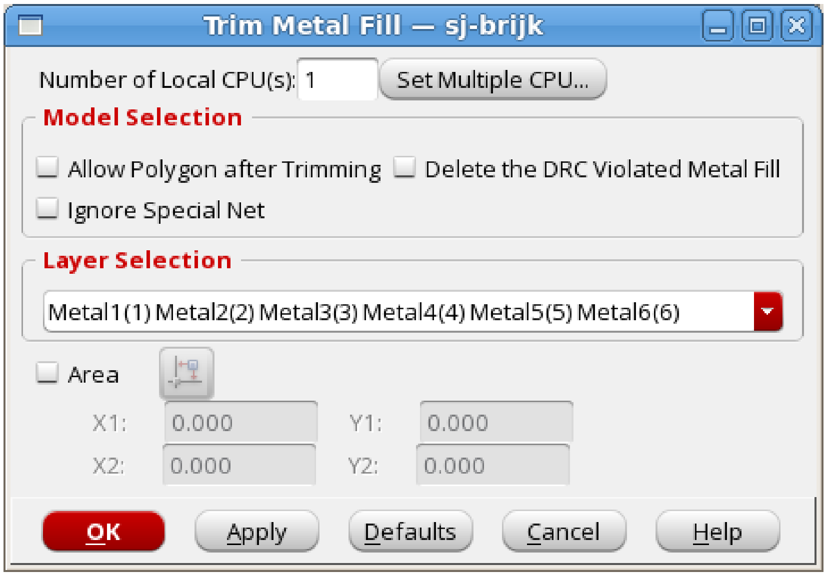
Trim

Use the *Trim* item on the *Metal Fill* submenu to open the Trim Metal Fill form.

Trim Metal Fill

Use the Trim Metal Fill form to trim metal and via fill that causes DRC violations.

- Choose *Route - Metal Fill - Trim*.



Trim Metal Fill Fields and Options

Number of Local CPU(s)	Displays the number of local CPUs used for multi-threading. This is a non-editable field. To change setting for multi-threading, click the *Set Multiple CPU* button.
Set Multiple CPU	Opens the Multiple CPU Processing form, where you can view or change settings for multi-threading and distributed processing.
Allow Polygon after Trimming	Allows rectilinear shapes after trimming metal fill (FILLWIRE and FILLWIREOPC shapes).
Delete the DRC Violated Metal Fill	

<table>
<tr><td></td><td colspan="2">Deletes metal fill shapes that cause DRC violations or shorts, instead of trimming sections of the shapes. If metal fill is trimmed using this option, the remaining shapes are still rectangles. If using this option causes metal density to drop below the target density, add metal fill again.

Always specify this option in the following two cases:
• If the design has minimum step rules, specify this option to avoid creating minimum step violations.
• If you ran <code>addMetalFillsnap1 -snap</code>, specify this option to delete entire shapes instead of trimming sections of the shapes. Otherwise, the trimmed shapes will not be on-grid.</td></tr>
<tr><td>Ignore Special Net</td><td colspan="2">Ignores special nets while checking for DRC violations.</td></tr>
<tr><td>Layer Selection</td><td colspan="2">Specifies the metal layers in which metal fill needs to be trimmed. By default, metal fill is trimmed for all metal layers. You can deselect the check boxes for the layers on which you do not want to trim metal fill.

Note: This option is recommended for use with only floating metal fill. If you try to perform layer-specific trimming on tied-off fill shapes, Innovus returns a warning message that some of the shapes may become isolated from the Power/Ground network.</td></tr>
<tr><td></td><td>All Layers</td><td>Specifies that metal fill needs to be trimmed on all layers. Use this button to select all metal layer check boxes quickly.</td></tr>
<tr><td></td><td>Deselect All Layers</td><td>Deselects all layer check boxes quickly.

As all layers are selected by default. Click this button to deselect all layers quickly and then select the specific layers you want.</td></tr>
<tr><td>Area</td><td colspan="2">Specifies a set of coordinates within which metal fill needs to be trimmed. By limiting the area in which metal fill is trimmed, you can speed up the trimming process.

Note: This option is recommended for use with only floating metal fill. If you try to perform area-specific trimming on tied-off fill shapes, Innovus returns a warning message that some of the shapes may become isolated from the Power/Ground network.</td></tr>
</table>

	Draw	Populates the *X1*, *Y1*, *X2*, and *Y2* boxes with the coordinates of the rectangle you draw on the main window.

Related Topics

- *Trimming Metal Fill* in the Optimizing Metal Density chapter of the *Innovus User Guide*

Related Text Commands

`trimMetalFill`

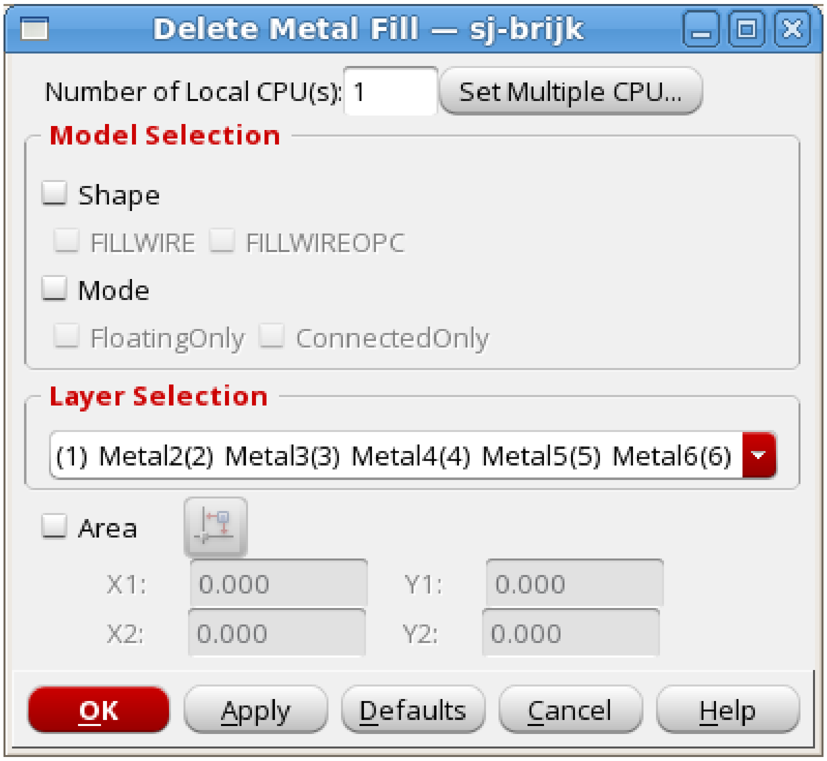
Delete

Use the *Delete* item on the *Metal Fill* submenu to open the Delete Metal Fill form.

Delete Metal Fill

Use the Delete Metal Fill form to remove metal and via fill in order to start over with the metal fill process.

- Choose *Route - Metal Fill - Delete*.



Delete Metal Fill Fields and Options

Number of Local CPU(s)	Displays the number of local CPUs used for multi-threading. This is a non-editable field. To change setting for multi-threading, click the *Set Multiple CPU* button.	
Set Multiple CPU	Opens the Multiple CPU Processing form, where you can view or change settings for multi-threading and distributed processing.	
Shape	Specifies whether the software removes FILLWIRE or FILLWIREOPC shapes or both kinds of shapes. If *Shape* is selected, both FILLWIRE AND FILLWIREOPC shapes are deleted by default.	
	FILLWIRE	Removes FILLWIRE shapes.
	FILLWIREOPC	Removes FILLWIREOPC shapes.

Mode	Specifies whether the software removes only connected fill, only floating fill, or all fill. if *Mode* is selected, both connected and floating fill are removed by default.	
	FloatingOnly	Removes floating fill.
	ConnectedOnly	Removes connected fill.
Layer Selection	Specifies the metal layers in which metal fill needs to be removed. By default, metal and via fill is removed from all metal layers. You can deselect the check boxes for the layers from which you do not want to remove metal fill.	
	All Layers	Specifies that metal fill needs to be removed from all layers. Use this button to select all metal layer check boxes quickly.
	Deselect All Layers	Deselects all layer check boxes quickly. As all layers are selected by default. Click this button to deselect all layers quickly and then select the specific layers you want.
Area	Specifies a set of coordinates within which metal and via fill needs to be removed. If you do not specify this option, metal fill is removed from the entire design area by default	
	Draw	Populates the *X1*, *Y1*, *X2*, and *Y2* boxes with the coordinates of the rectangle you draw on the main window.

Related Topics

Trimming Metal Fill

Related Text Commands

`deleteMetalFill`

Via Fill

Use the Via Fill forms to create via fill, based on the values you specify on the forms.

The Innovus software inserts vias into a placed and routed design to help achieve cut density within the range required by a specific manufacturing process. Unlike adding metal fill, when the software considers only the layer on which the fill is added, adding via fill requires that the software consider the metal layers above and below the cut layer.

The vias can be floating or connected to power or ground wiring.

Add via fill in the following areas immediately before adding metal fill:

- Where metal fill shapes would intersect with power or ground nets on consecutive layers if no via fill was added.
- Where metal fill shapes on consecutive layers would intersect if no via fill was added.

> To reduce the need for via fill, insert multiple-cut vias with the NanoRoute® router. For information, see `setNanoRouteMode`.

The *Via Fill* submenu contains the following items:

- Setup
  Opens the Setup Via Fill Options form.
- Add
  Opens the Add Via Fill form.

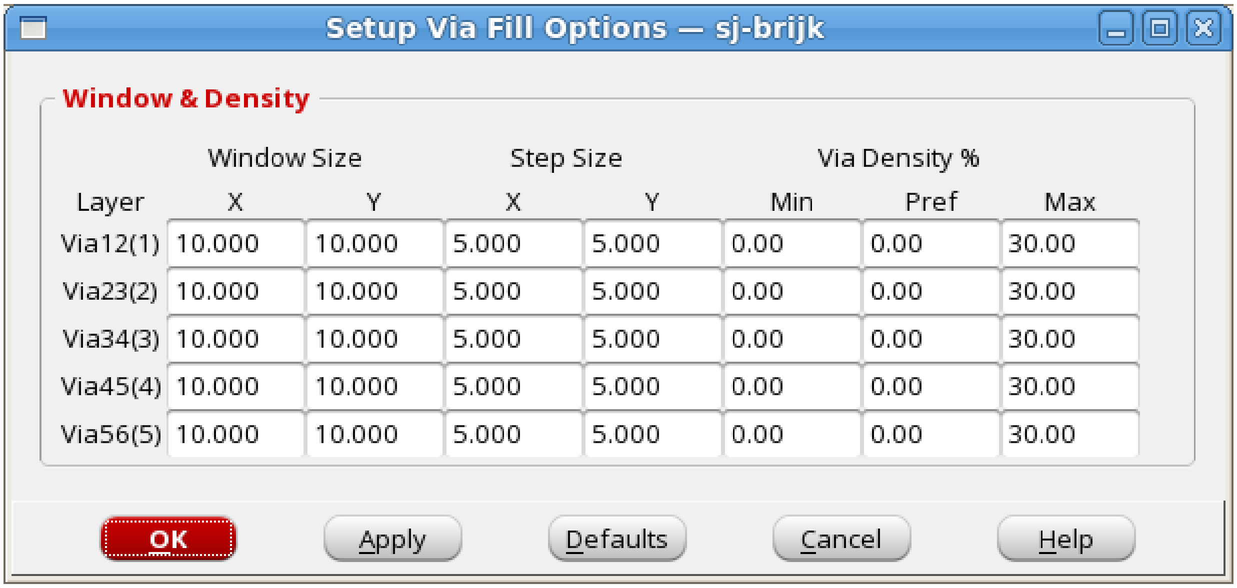
Setup

Use the *Setup* command in the *Via Fill* submenu to access the Setup Via Fill Options form.

Setup Via Fill Options

Setup Metal Fill form to set options for adding or trimming via fill.

- Choose *Route - Via Fill - Setup*.



Setup Via Fill Fields and Options

Note: The software uses the width and spacing values on the Setup Via Fill Options form.

Window Size	Specifies the x and y dimensions in microns of the area `setViaFill` uses to examine the cut density. The software assesses the cut density in each window, moving the window iteratively through the design. *Default:* 10 microns in each dimension	
Step Size	Specifies the x and y step distance in microns the window moves for each iteration of cut density analysis. *Default:* 5 microns in each dimension	
Via Density %	*Min*	Specifies a percentage value for the minimum cut density allowed in the design. *Default:* area of two cuts divided by 100 square microns

	Pref	Specifies a percentage value for the preferred cut density for the layer. When the cut density in a window is less than the minimum cut density value, this parameter adds via fill to achieve a density as close as possible to the preferred value. To disable the preferred density feature, specify `0`. *Default:* area of two cuts in the cut layer
	Max	Specifies a percentage value for the maximum cut density allowed. *Default:* `30%`
Layer	Specifies the cut layer to which the parameters of the `setViaFill` command apply. Specifies the cut layer to which the parameters of the `setViaFill` command apply.	

Related Text Commands

`setViaFill`

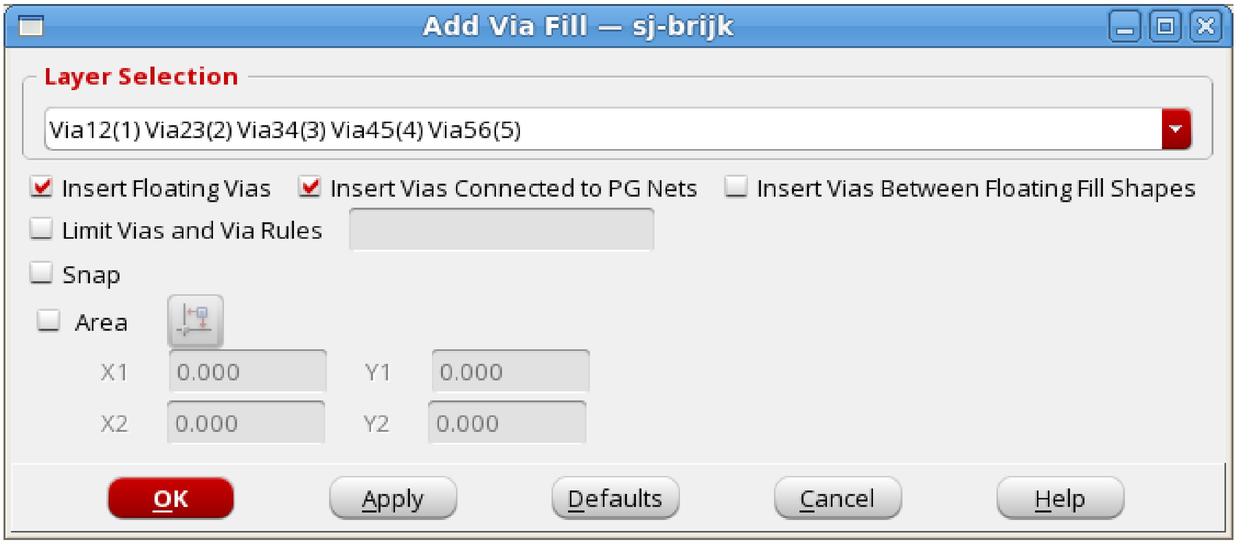
Add

Use the Add command in the Via Fill submenu to access the Add Via Fill form.

Add Via Fill

Use the Add Via Fill form to specify the layers, mode, and area for adding via fill.

- Choose *Route - Via Fill - Add*.


Add Via Fill — sj-brijk
Layer Selection
Via12(1) Via23(2) Via34(3) Via45(4) Via56(5)
Insert Floating Vias
Insert Vias Connected to PG Nets
Insert Vias Between Floating Fill Shapes
Limit Vias and Via Rules
Snap
Area
X1
0.000
Y1
0.000
X2
0.000
Y2
0.000
OK
Apply
Defaults
Cancel
Help

Add Via Fill Fields and Options

Layer Selection	Specifies the cut layers where via fill is added. Deselect the layers in which you do not want to add via fill. *Default: All Layers* Click the *Deselect All Layers* button to deselect all layer check boxes quickly. Click the *All Layers* button to select all layer check boxes quickly.
Insert Floating Vias	Adds unconnected via fill. This is equivalent to `addViaFill -mode floating`. *Default: Selected*
Insert Vias Connected to PG Nets	
	Adds connected via fill to PG. This is equivalent to `addViaFill -mode connectToPG`. *Default: Selected*
Insert Vias Between Floating Fill Shapes	
	Adds connected via fill between floating metal fill. This is equivalent to `addViaFill -mode connectBetweenFill`.
Limit Vias and Via Rules	
	Specifies a list of vias (VIA in LEF) to be included or via rules (VIARULE GENERATE in LEF) to be used or a combination of the two. This is equivalent to `addViaFill -includeVia`.
Snap	Snaps edges of via fill shapes and centers of cuts to a user-defined snap grid that is a multiple of the manufacturing grid. When via shapes are snapped to this grid, the edges and centers of the via shapes lie on the grid. If a grid is not specified, the software snaps the shapes to the manufacturing grid. You can define a grid using the `setSnapGrid` command.
Area	Specifies a set of coordinates within which to add via fill.

Related Text Commands

`addViaFill`

12

Timing Menu

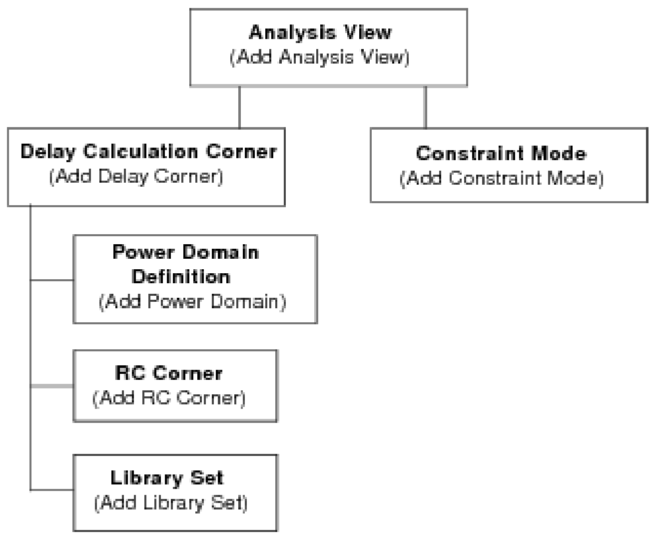
- Timing Debug Preferences - Bottleneck Analysis
- Timing Debug Preferences - Select Color
- Timing Debug Preferences - Cell Coloring
- Timing Debug Preferences - Highlight Path
- Timing Debug - Analysis
- Path Analysis (Path Group Analysis)
- Path Analysis (Clock Analysis)
- Path Analysis (Hierarchical Floorplan)
- Path Analysis (Hierarchical Port)
- Path Analysis (View Analysis)
- Path Analysis (Critical False Path)
- Path Analysis (Bottleneck Analysis)
- Path Analysis (DRV Analysis)
- Path Analysis (Noise Result Analysis)
- Hierarchical Analysis Viewer
- Clock Matrix Viewer
- Create Path Category
- Timing Path Analyzer
- Timing Path Analyzer - Data Path
- Timing Path Analyzer - Launch Clock
- Timing Path Analyzer - Capture Clock
- Timing Path Analyzer - Path SDC
- Timing Path Analyzer - Timing Interpretation
- Edit Timing Interpretation
- Timing Path Analyzer - Schematics
- Create Black Box/Blob Model
- Black Box-Blob What-If Timing Analysis - Browser

MMMC Browser

Timing Debug - Analysis

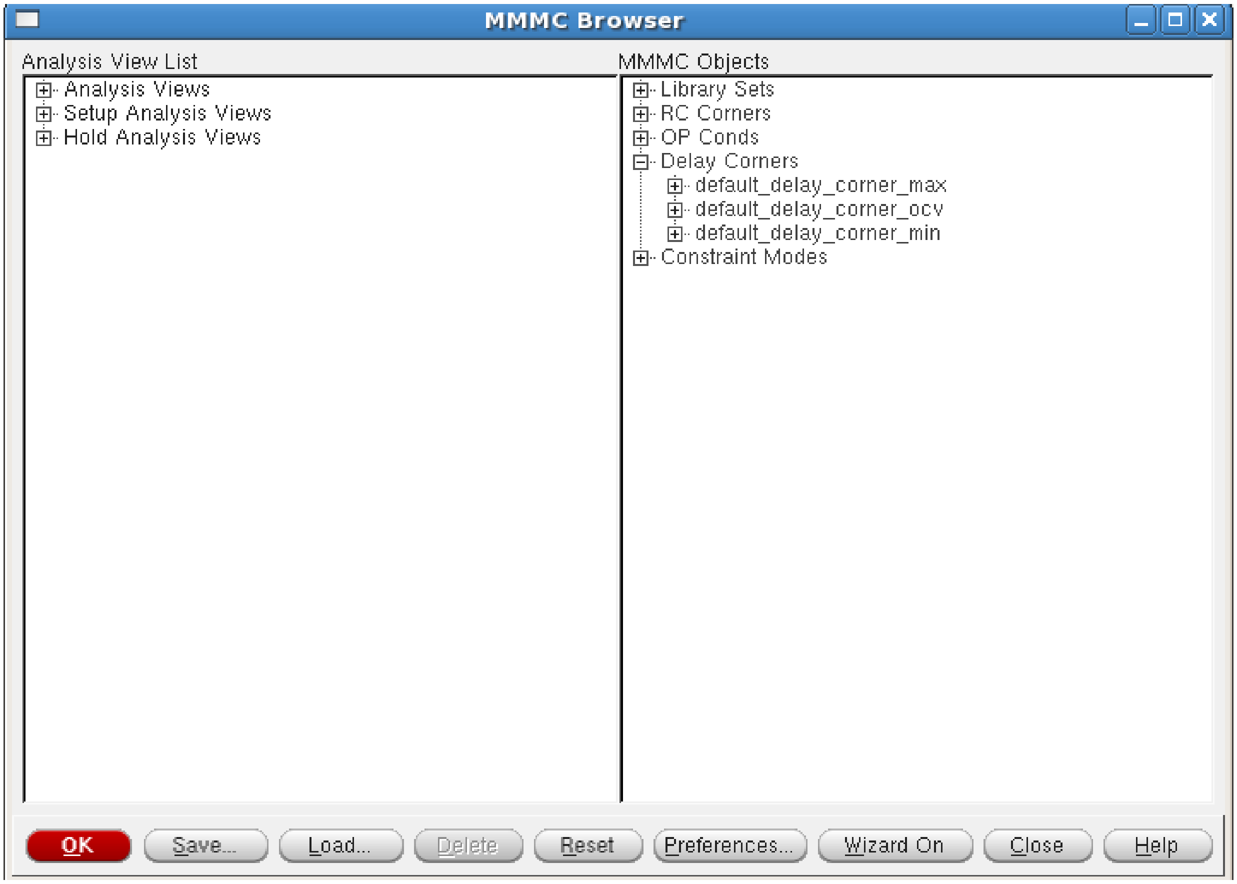
Use the MMMC Browser to hierarchically create the view configurations necessary for multi-mode multi-corner analysis. Each top-level set of information is called an analysis view, and is composed of a delay calculation corner and a constraint mode. The active analysis views defined in the software represent the different design variations that will be analyzed.

Figure 12-1 Hierarchical Analysis View Configuration



Note: You can access the MMMC Browser from the *Design Import* form, and from the *Timing* menu. Use the MMMC Browser accessed from the *Design Import* form to create a new multi-mode multi-corner configuration for the design. Use the MMMC Browser accessed from the *Timing* menu to add new objects and control analysis views to the existing multi-mode multi-corner configuration that is in memory for the design.

The configurations that you create are stored as tcl commands in a view definition file that can then be loaded into the design.
→ Choose *Timing - MMMC Browser*.



You can access the following forms from the MMMC Browser by double clicking on the generic object or view name:

- Add RC Corner
- Add Delay Corner
- Add OP Conds
- Add Analysis View
- Add Setup Analysis View
- Add Hold Analysis View

You also can access the following editing forms from the MMMC Browser by double clicking on a specific object name.

- Edit Library Set
- Edit RC Corner
- Edit Constraint Mode

- Edit Delay Corner

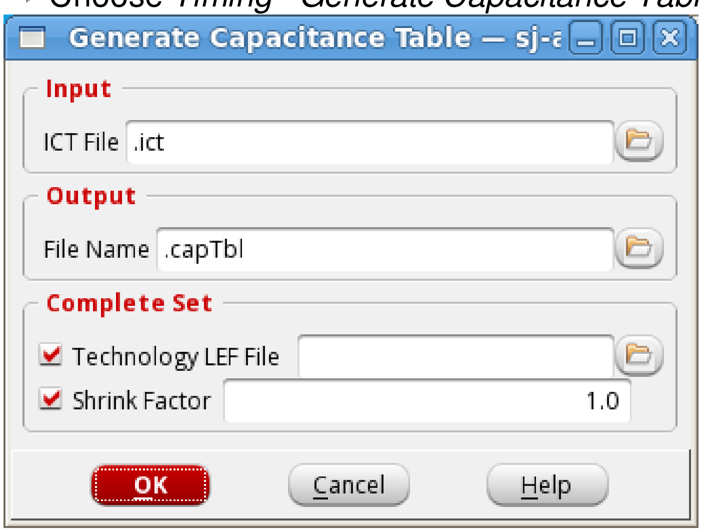
Note: The editing forms are available only before the multi-mode multi-corner view definition file is loaded into the database. After the software processes the file, the objects can no longer be edited; however, you can still control the selection of active analysis views.

Generate Capacitance Table

Use the Generate Capacitance Table form to create a capacitance table file containing process information, resistance information, and capacitance coefficients needed by PreRoute and PostRoute -effortlevel low extraction engines. Without a capacitance file, these extractors can only provide a rough estimate of the parasitics based on hardwired process data.

> Generating a capacitance table is CPU-intensive, and can take several hours to run for newer technologies. Setting up distributed processing prior to starting the captable generation is recommended to reduce runtime. Alternatively, use the `generateCapTbl` standalone executable which can be found in the `/bin` directory of your Innovus hierarchy. The standalone executable runs independent of Innovus; it has the same syntax as the `generateCapTbl` command but distributed processing is not supported with the standalone executable.

→ Choose *Timing - Generate Capacitance Table*.



Generate Capacitance Table Fields and Options

ICT File	Specifies the name of the input process file.
File Name	Specifies the output file name for the capacitance table.
Technology LEF File	Specifies the name of the technology LEF file. If the LEF is provided, routing pitch, wire widths, and non-default routing rule information will be used to optimize the capacitance table generation.
Shrink Factor	Specifies the value by which the measurements in the optional LEF file have to be shrunk to match the technology used with this design. The default value is 1. If the shrink factor is already specified in the header of the ICT file, as is customary for half node processes, you do not need to specify the shrink factor.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `generateCapTbl`

For more information, see "Timing Commands" in the *Innovus Text Command Reference*.

Related Topics

For information on the following topic, see the RC Extraction chapter in the *Innovus User Guide*:

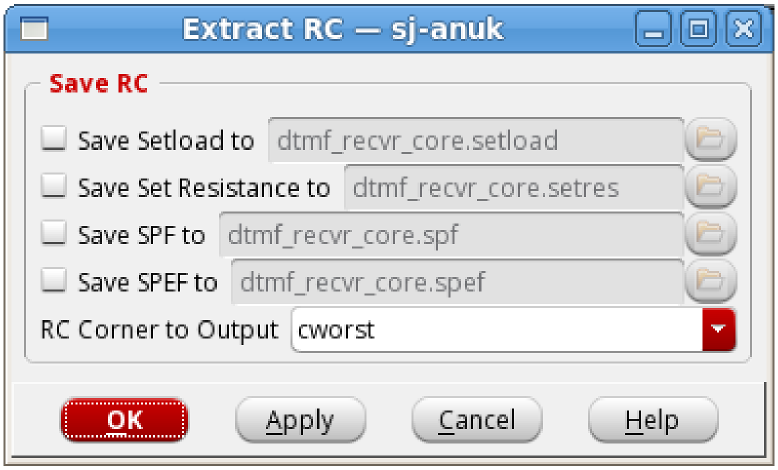
- Generating a Capacitance Table

For information on the following topic, see the Creating the ICT File chapter in the *Innovus User Guide*:

- Creating the ICT File

Extract RC

Use the Extract RC form to run RC extraction.
→ Choose *Timing - Extract RC*.



Extract RC Fields and Options

Save Setload to	Specifies the name of the `set_load` formatted file in which the value of lump sum capacitance on nets is stored.
Save Set Resistance to	Specifies the name of the `set_resistance` formatted file in which the resistance value on nets is stored.
Save SPF to	Specifies the name of the Standard Parasitic Format file. This format only supports decoupled RC output.
Save SPEF to	Specifies the name of the Standard Parasitic Exchange Format file.
RC Corner to Output	Specifies the RC corner that is used to generate the parasitic output file in the MMMC flow. If you do not specify the corner, the software will use the first corner.

Related Text Commands

The following command and attributes provide equivalent or additional functionality:

- extract_rc Category Attributes
- `rcOut`

For more information, see RC Extraction Commands and Global Variable in the *Innovus Text Command Reference*.

Related Topics

For information on the following topics, see the RC Extraction chapter in the *Innovus User Guide*:

- PreRoute Extraction
- PostRoute Extraction

Report Timing

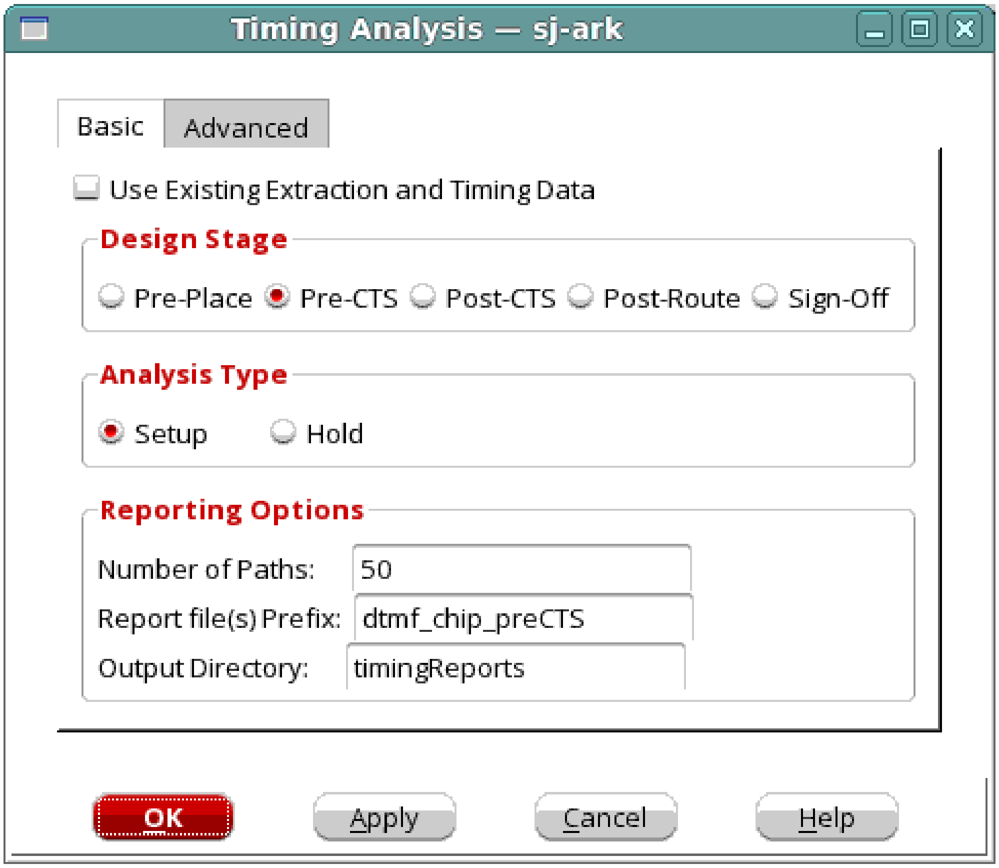
Use the *Report Timing* menu item to access the Timing Analysis form. This form helps you build the timing graph for the design and generate a slack report and a detailed timing violation report. Load both the Timing Library and the timing constraints file (`dc_shell`) during design import.

The Timing Analysis form contains the following pages:

- Timing Analysis - Basic
- Timing Analysis - Advanced

Timing Analysis - Basic

Use the *Basic* page of the Timing Analysis form to set up reporting options.
→ Choose *Timing - Report Timing.* The *Basic* tab opens by default.



Timing Analysis - Basic Fields and Options

Pre-Place	Generates timing reports before the design is placed. In this mode, the software ignores the net load while building the timing graph and runs timing analysis for generating timing reports. The DRV report files are not generated in this mode. The *Pre-Place* option sets the `setAnalysisMode` to `-clkSrcPath false` and `-clockPropagation forcedIdeal`.
Pre-CTS	Generates timing reports for a design before the clock tree is created. By default, in this mode the software runs earlyGlobalRoute, preRoute extraction, and timing analysis for generating timing reports. The *Pre-CTS* option sets the `setAnalysisMode` to `-clkSrcPath false` and `-clockPropagation forcedIdeal`

Post-CTS	Generates timing reports for a design whose clock tree has been created. By default, in this mode the software runs earlyGlobalRoute, preRoute extraction, and timing analysis for generating timing reports. The *Post-CTS* option sets the `setAnalysisMode` to `-clkSrcPath true` and `-clockPropagation sdcControl`.
Post-Route	Generates timing reports for a design whose routing is complete. By default, in this mode the software runs postRoute extraction, and timing analysis for generating timing reports. The *Post-Route* option sets the `setAnalysisMode` to `-clkSrcPath true` and `-clockPropagation sdcControl`.
Sign-Off	Generates timing reports for sign-off timing analysis. By default, in this mode the software runs QRC standalone extraction. **Note:** To use this parameter, you must ensure that the Innovus configuration file contains data for QRC standalone extraction.
Setup	Reports setup violation only.
Hold	Reports hold violation only. *Default:* Reports setup violations.
Use Existing Extraction and Timing Data	
	Specifies the use of existing extraction and timing analysis data. When you select this option, the software does not run extraction and timing analysis. The timing analysis data must match the stage of the design that you have specified using the *Pre-Place*, *Pre-CTS*, *Post-CTS*, *Post-Route*, or *Sign-Off* options.
Number of Paths	Specifies the number of paths to report in the detailed path violations. *Default:* `50`
Report file(s) Prefix	Specifies a prefix for the timing report file names. *Default:* *`DesignName_DesignStage`*
Output Directory	Specifies the name of the output directory that contains all the generated reports. *Default:* `timingReports`

Related Text Commands

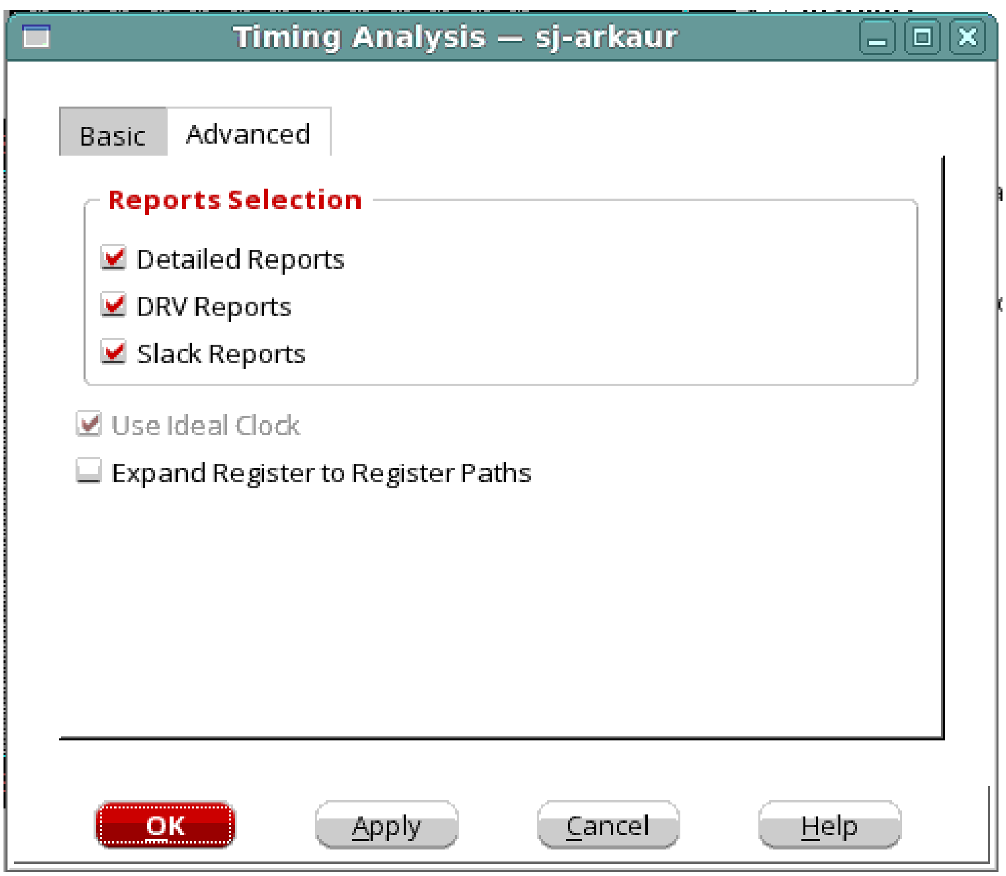
The following text commands provide equivalent or additional functionality:

- timeDesign

For more information, see "Timing Analysis Commands" in the *Innovus Text Command Reference*.

Timing Analysis - Advanced

Use the *Advanced* page of the Timing Analysis form to set up the path groups along with advanced reporting options.
→ Choose *Timing - Report Timing* and click the *Advanced* tab.



Timing Analysis - Advanced Fields and Options

Detailed Reports	Generates a detailed timing report file containing the top critical timing paths. In addition, it generates report files for each of the path groups (For example, reg2reg/default).
DRV Reports	Generate design rule violation (DRV) reports only.
Slack Reports	Generate slack reports only.
Use Ideal Clock	Performs ideal clock analysis irrespective of the design stage. *Default:* The software performs propagated clock analysis with the *Post-CTS* and *Post-Route* options. The software performs ideal clock analysis with the *Pre-Place* and *Pre - CTS* options.
Expand Register to Register Paths	
	Specifies that the register to register path groups are divided into the following detailed path groups for generating reports: • Flop to flop • Macro to flop or latch • Flop to macro or latch • Macro to macro

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `timeDesign`

For more information, see "Timing Analysis Commands" in the *Innovus Text Command Reference*.

Debug Timing

The *Debug Timing* menu item provides options for debugging the timing results. The timing debug feature provides easy cross-probing between the Timing Debug forms and Innovus design display area.

Innovus provides different timing debug features depending on the timing mode that you have selected.
➝ To generate a timing report, choose *Timing - Debug Timing* on the Innovus Timing menu and use the following form:

- File - Timing Debug Preferences
  The Timing Debug Preferences form displays the results generated.
- Timing Debug - Browser
  The Timing Debug - Browser form is displayed when you right-click on any path in the Timing Debug Browser:
- Timing Debug

➝ To take a snapshot of the histogram when you right-click any part of Path Histogram:

- The Timing Debug - Path Histogram form appears.

➝ To edit table columns, right-click on any path in the Timing Debug Browser:

- The Timing Debug - Edit Table Column form appears.

➝ To load global timing debug preferences, use the following form:

- Timing Debug - Edit Table Columns - Load GTD Preferences File

➝ To view Timing Debug Analysis, use the following form:

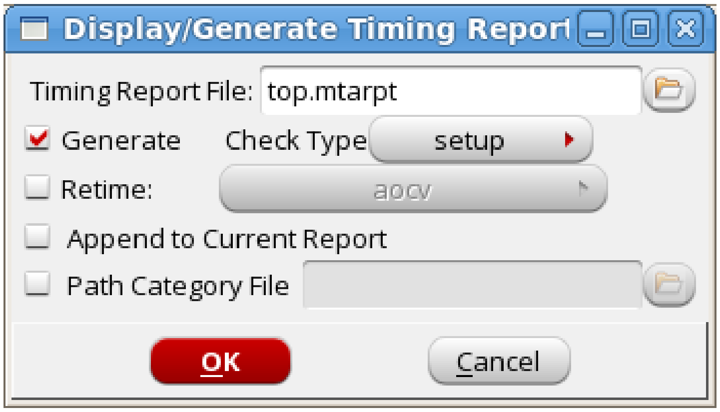
- Timing Debug - Analysis

Display/Generate Timing Report

Use the Display/Generate Timing Report form to specify the violation report to be read in for debugging timing results. Alternatively you can choose to generate the violation report using the Generate option in this form.

Note: The violation report that you specify in this form has a special machine readable format. Use the `report_timing -machine_readable` command to generate the machine readable violation report. If you want to generate a text-format report, generate a machine-readable report using this form, the run the `write_text_timing_report` command.

→ Choose *Timing - Debug Timing*, and click the Browser icon .



Display/Generate Timing Report Fields and Options

Timing Report File	Specify a filename, or click the file folder icon to choose a file.
Generate	Generates a violation report file in machine readable format. *Default:* `top.mtarpt`
Retime	Reanalyzes the specified set of paths using one of the following methods - aocv, ssta, path_slew_propagation, aocv_path_slew_propagation.
Check Type	Can be selected for the type of Check: *Setup* or *Hold*. Previously this was available only from the command line.
Append to Current Report	
	Appends the specified report to the report that you have already loaded in a timing debug session. This feature is useful to collate reports from several views into one timing debug session.
Path Category File	Specifies the path category file. The path category file contains category definitions that you saved in an earlier timing debug analysis.

Related Text Commands

The following text command provides equivalent or additional functionality:

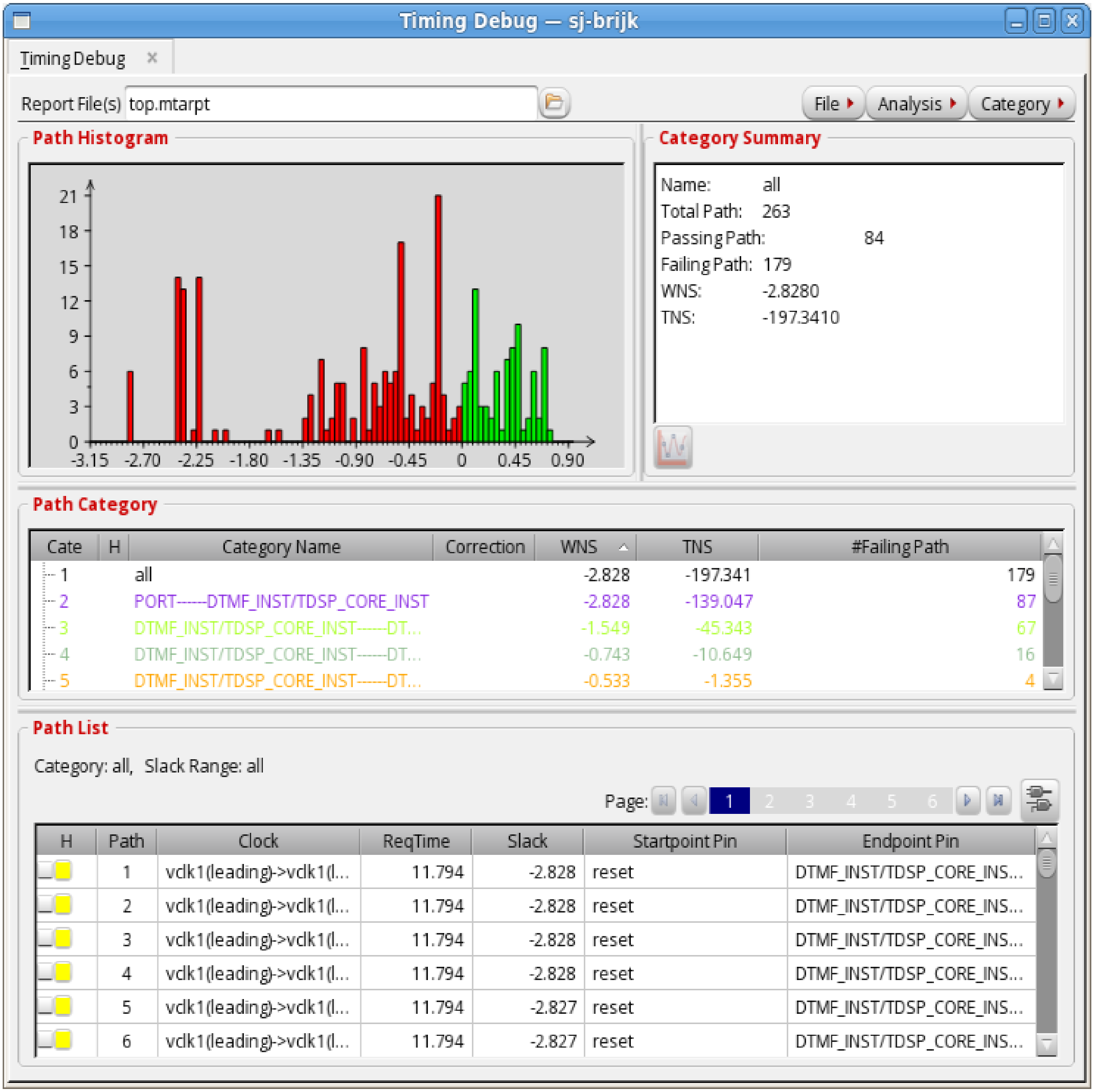
`load_timing_debug_report`

For more information, see "Timing Debug Commands" in the *Text Command Reference* document.

Timing Debug - Browser

Use the browser window to display the violation and slack information that you generate during timing analysis.

→ Choose *Timing - Debug Timing.*



The browser window consists of following three panes:

- *Critical Paths*
  Displays critical paths in the violation reports. You can select a path in this window to highlight it in the design display area and display the details in the *Detailed Paths* pane. For

more information on cross-probing, see Debugging Timing Results in *Innovus User Guide*.

- *Timing Bar*
  Displays the instance and net bars. The size of the bar indicates the delay associated with that element. Moving the cursor on these elements displays the details of instances or nets. You can click on a single element to highlight it in the design display area. You can select each element consecutively to trace the entire path in the design display area.

  You can colorize the instances displayed in the timing bar based on the number of times the instances appear in violating paths. See "Timing Debug Preferences - Bottleneck Analysis" .

  Note: Clear the highlights (*Edit - Clear Highlight - Clear All*) and selections (*Edit - Deselect All*) before using this feature.

  Right-click on the *Timing Bar* to display the following options:

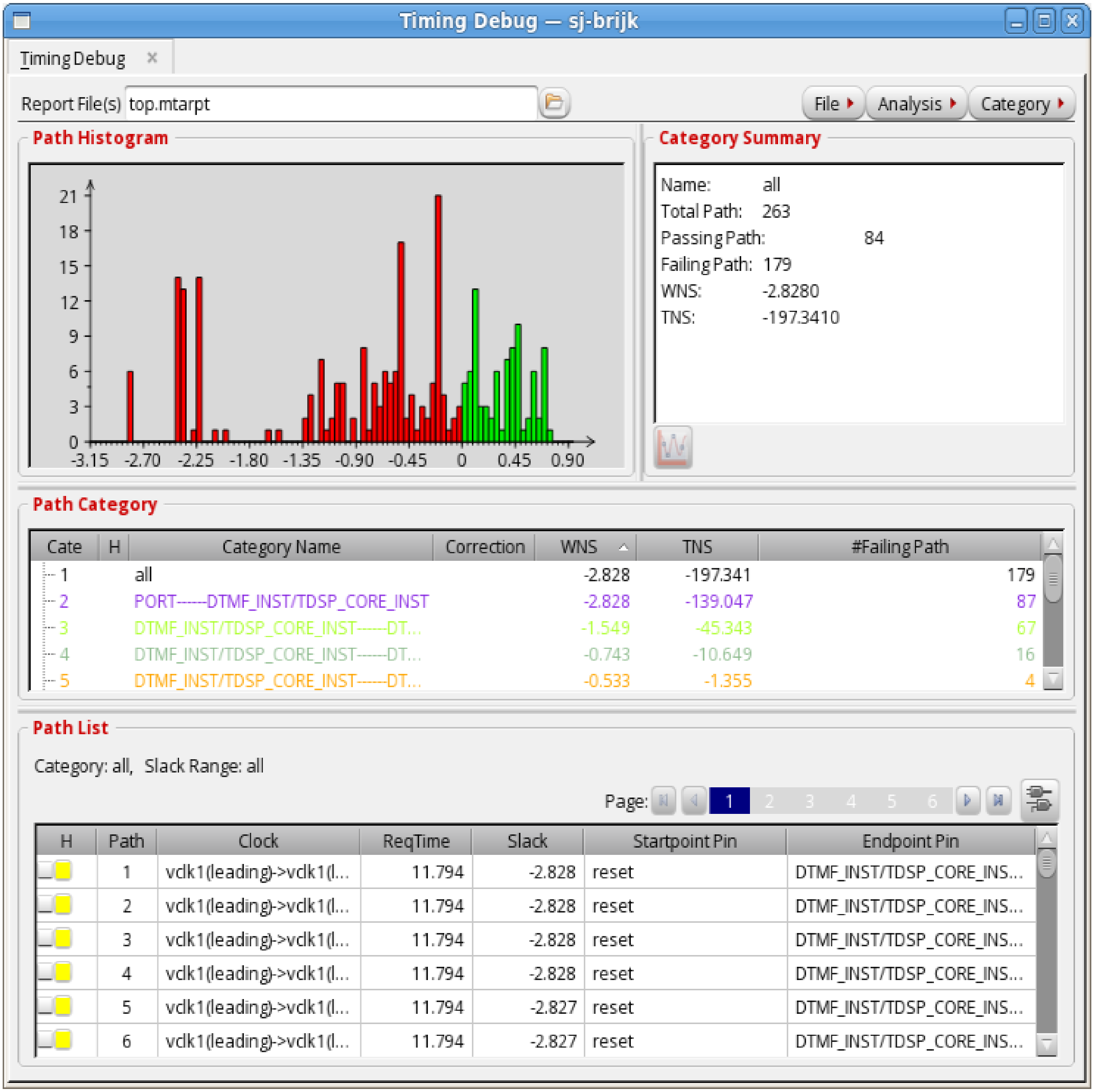
Fit	Displays the bars for the entire path.
Zoom In	Displays more details about a bar.
Zoom Out	Displays more bars in the set area.
Preference	Displays the Timing Debug Preference form. Use this form to specify the statistics for the histogram and number of pages to be displayed in the Timing Debug form. You can also set the color of the various elements in the Timing Debug forms. The Timing Debug Preference form has the following option:
	Show Schematic View
	Select this option to display the schematic. The Schematic Viewer displays the RTL-level or gate-level schematic view of the critical path that you select in the Timing Debug - Browser window. To display the schematic, select this option, and double-click on the critical path in the Timing Debug - Browser window.
Snapshot	Allows you to select the directory in which you want to save the snapshot you create and name the snapshot. The snapshot is a .gif image of the histogram.

Category	Creates the category of a single selected bar. To create a category, left click (twice) to choose the bar for which create is to be created, then right click the selected bar to create a category for the selected bar.

- *Path Details*
  Displays the details of the critical paths that you select in the *Critical Paths* pane. You can click on a single detail to display it in the design display area.

Timing Debug

Use the Timing Debug form to display the violation information, categories defined to group violation types, graphical display of violations, and category summary.
→ Choose *Timing - Debug Timing.*



Timing Debug Fields and Options

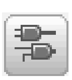
File	Provides the following menu options:

	Write Text Report	
		Displays the Write Text Report form. Write a text file containing information about paths that have been loaded from a `.mtarpt` file.
	Write Category Summary	
		Displays the Write Category Report File form to write a text file containing information related to the category paths.
	Preferences	Displays the Timing Debug Preferences form. For more information on the Timing Debug Preferences form, see "Timing Debug - Timing Debug Preferences" .
Analysis	Displays menu options to create standard categories for timing debug. Following options are displayed:	
	Path Group Analysis	
		Displays Path Analysis form. Use this form to create standard path categories according to basic path groups. For more information, see "Path Group Analysis" .
	Clock Analysis	
		Displays Path Analysis form. Use this form to create categories according to launch clocks - capture clock combinations. For more information, see "Path Analysis (Clock Analysis)" .
	Hierarchical Floorplan	
		Displays the Path Analysis form. Use this form to create categories according to the hierarchical floorplan characteristics of the paths.
	Hierarchical Port	
		Displays the Path Analysis form. Use this form to create categories according to the hierarchical port characteristics of the paths.

	View Analysis	
		Displays the Path Analysis form. Use this form to create categories according to the views that were defined for multi-mode multi-corner analysis. For more information, see "Path Analysis (View Analysis)" .
	Critical False Path	
		Displays the path analysis form. Use this form to create a category containing paths identified as false during the critical path analysis by Conformal Constraint Designer (`ccd`). **Note:** `ccd` should be in the command search path to access this menu.
	Bottleneck Analysis	
		Displays the Path Analysis form. Use this form to create categories according to the bottleneck analysis of the critical paths. For more information, see "Path Analysis (Critical Path Analysis)" .
	DRV Analysis	
		Displays the Path Analysis form. Use this form to categorize paths according to DRV report file.
	Noise Result Analysis	
		Displays the Path Analysis form. Use this form to display the noise results.
	Hierarchical Analysis Viewer	
		Displays the Hierarchical Analysis Viewer form. Use this form to view the results from hierarchical analysis that is done while creating the hierarchical paths category.
	Clock Matrix Viewer	

		Displays the Hierarchical Analysis Viewer form. Use this form to display the relationship of source and destination clocks.
Category	Displays menu options for creating and managing categories. Following options are displayed:	
	Create	Displays the Create Category form. Use this form to specify definitions for categories as per your design requirements. For more information, see "Create Path Category" .
	Save	Saves the category definitions in a file. You can use this file to load a set of predefined categories into a new timing debug session.
	Load	Loads the category definition file.
Path Histogram	Displays the end point histogram. The failing endpoints are displayed in red and the passing endpoints are displayed in green color. Right-click on the histogram to display the following options:	
	Fit	Displays the entire histogram in Path Histogram area. Use the *F* key on your keyboard to enable it.
	Zoom	Displays smaller or larger area of the histogram in greater or lesser detail. Use the *Z* key on your keyboard to Zoom-in and *Shift+Z* key to Zoom-out.
	Pan	Displays areas to the top, bottom, left or right of the displayed histogram.
	Preference	Displays the Timing Debug Preferences form. Use this form to specify the statistics for the histogram and number of pages of report to be displayed in the form. For more information on the Timing Debug Preferences form, see "Timing Debug - Timing Debug Preferences" .
Category Summary	Displays the summary of a single selected category. To select a category, double-click on the category name in the *Path Category* field.	

Path Category	A tree so that the nested category can collapse/uncollapse. The entries display the category information. The columns in this field include, name of the category, worst negative slack (WNS), total negative slack (TNS), and number of failing paths. Right click on the category name to display the following options:	
	List Paths (Category Name)	
		Displays the detailed path information in the *Path List* field.
	Add Category to Histogram	
		Displays the selected category as histogram. The added category is displayed in a different color. Use this option to identify paths grouped under a specific category.
	Hide Category in Histogram	
		Removes the category from the histogram, but does not delete it. Hidden categories are indicated with the letter "H" to the left of the category name.
	Set Category Slack Correction	
		Displays the Set Category Slack Correction form. Use this form to specify the estimated slack correction for the selected category of paths. For more information, see "Manual Slack Correction of Categories" in the *Innovus User Guide*.
	Edit Category	Displays the Create Path Category form. Use this form to change category definition as per your requirements. For more information, see Create Category form.
	Delete Category	
		Deletes the selected category.
	Delete All Category	
		Deletes all categories that you have created.
	Change Category Color	

		Displays Color Category Name form. Use this form to specify the color to be used in the Path Histogram for the selected category.
	Interact ECO/Whatif	
		Right-click to find options: *Change Cell, Add Repeater, Delete Repeater*. For more details see Interactive ECO. After the ECO operations are completed, the timing report will be updated, and added to Timing Debug as a category.
	Copy Cell	Copies the name of the category in the Path Category table. Use this feature to copy and paste the text from Path Category to Create Category form.
	Edit Table Column	
		Displays the Edit Table Column form. Use this form to customize columns in the *Timing Debug* and *Timing Path Analyzer* windows.
Path List	Displays the list of paths (startpoint, endpoint and slack) in the selected category. Double-click on a path to display the Timing Path Analyzer form. Use this form for detailed analysis of a single path. For more information on Timing Path Analyzer form, see "Timing Path Analyzer" . When you load multiple debug reports in a single timing debug session, the paths are displayed in different colors corresponding to the report file they are coming from. You can move the cursor over a path to display the name of the report file.	
	Displays the schematic view of the selected path.	

Related Text Commands

The following text command provides equivalent or additional functionality:

- `analyze_paths_by_basic_path_group`
- `analyze_paths_by_bottleneck`
- `analyze_paths_by_clock_domain`

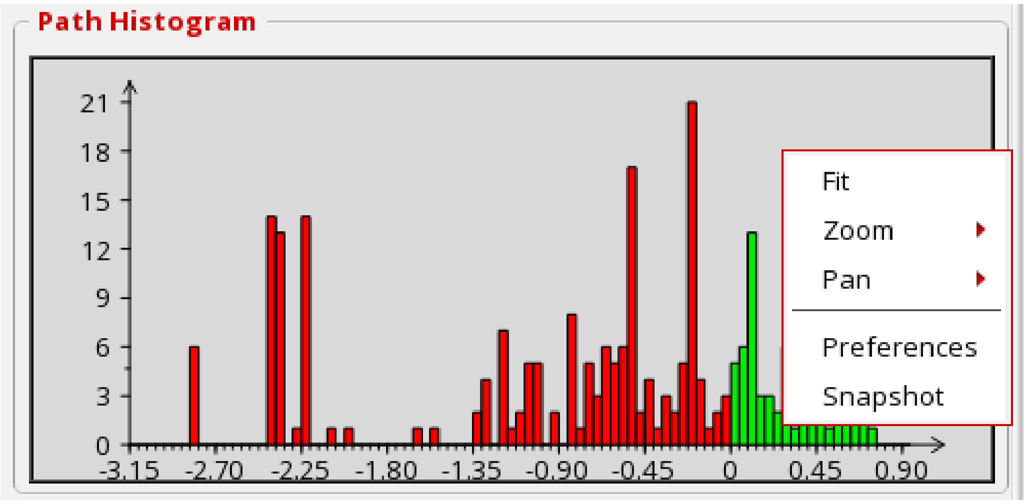
- analyze_paths_by_critical_false_path
- analyze_paths_by_hierarchy
- analyze_paths_by_view
- create_path_category
- delete_path_category
- load_path_categories
- load_timing_debug_report
- save_path_categories

For more information, see "Timing Debug Commands" in the *Text Command Reference* document.

Timing Debug - Path Histogram

Use the *Path Histogram* form to take a screenshot from the right-click menu on the Path Histogram area of the Timing Debug form.

1. Open the *Timing Debug* form, then right-click on a histogram. A drop-down menu is displayed.
2. Select *Snapshot*.



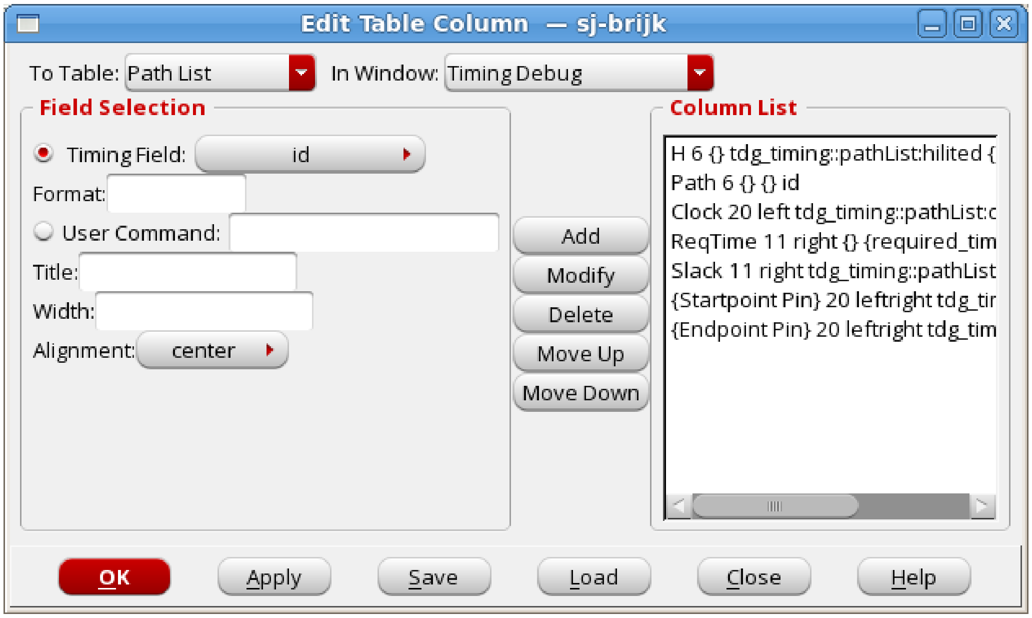
Fields and Options

Fit	Fits the histogram within the design display area. Use the *F* key on your keyboard to enable it.
Zoom	Helps you zoom in or out of the histogram. Use the *Z* key on your keyboard to Zoom-in and *Shift+Z* key to Zoom-out.
Pan	Helps you move the histogram screen area and see parts of it that are beyond the viewable area.
Preferences	Helps you set preferences. See Timing Debug Preferences - General .
Snapshot	Allows you to select the directory in which you want to save the snapshot you create and name the snapshot. The snapshot is a .gif image of the histogram. You can also choose to save the histogram in CSV format. Right-Click in the histogram and select Snapshot. From the panel you can choose to save the histogram data in CSV format.

Timing Debug - Edit Table Column

Use the *Edit Table Column* form to customize columns in the *Timing Debug* and *Timing Path Analyzer* windows.

1. Open the *Timing Debug* or *Timing Path Browser* form, then right-click on a path. A drop-down menu is displayed.
2. Select *Edit Table Column*.



Edit Table Column Fields and Options

Window Name	Specifies the name of the window that contains the table column you want to edit. Choose from Innovus, Timing Debug, or Timing Path Analyzer.
Column Item	Specifies the type of information to include in the column. Choose from *delay*, *name*, *incr_delay*, *arrival*, *required*, *stolen*, *type*, *arc*, *cell*, *slew*, *fedge, wire length, tedge*, *constraint*, *load*, *pin,* or *fanout.*
Format	Specifies a table format. For example, specify `%.3f` if you only want to display three decimal digits.

<table>
<tr><td>Command</td><td colspan="2">Specifies the procedure you want to use to determine the information you want to include in the column. In the procedure, you must pass the instance as a parameter. You must source the file containing procedure before specifying the procedure here.

For example:
<pre>
Combine fedge (from edge) and tedge (to edge) #information into a single field

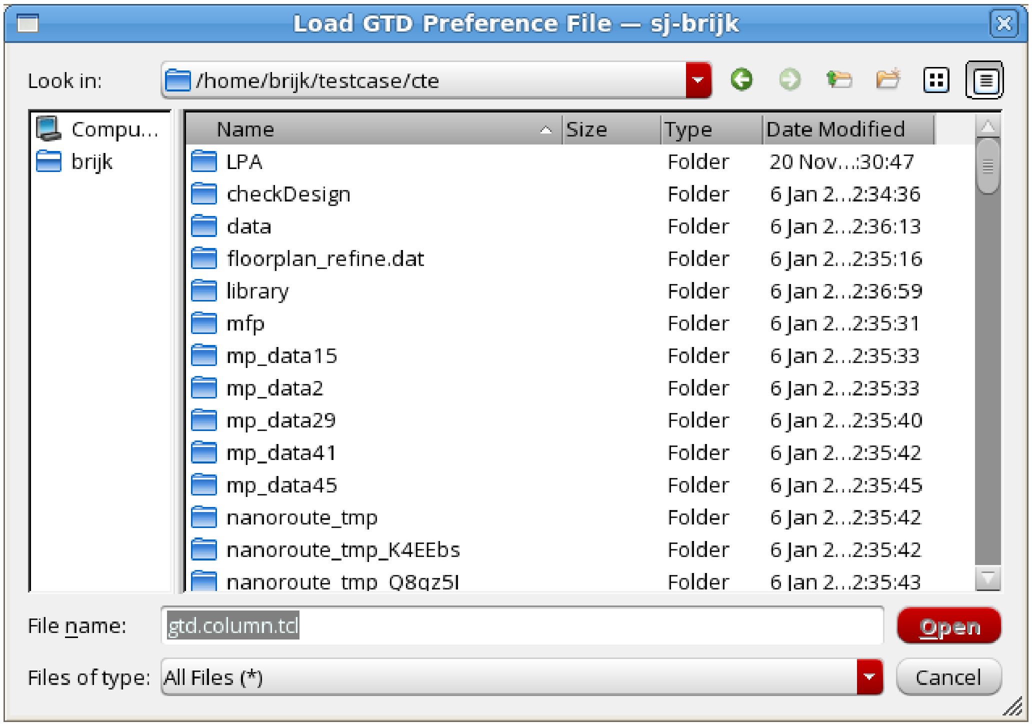
proc my_get_edge {id var} {
     upvar #0 $var p
     if {p(type) == "inst"} {
        return "$p(fedge) -> $p(tedge)"
     } elseif {$p(type) == "port" } {
        return $p(fedge)
     } else {
        return ""
     }
}
</pre></td></tr>
<tr><td></td><td>Title</td><td>Specifies the column title.</td></tr>
<tr><td></td><td>Width</td><td>Specifies the column width.</td></tr>
<tr><td></td><td>Align</td><td>Specifies the alignment of the column. Choose from center, left, right, and leftright.</td></tr>
<tr><td>Table Name</td><td colspan="2">Choose the table whose columns you want to modify:
For the Timing Path Analyzer window choose Data Path, Capture Clock, or Launch Clock.
For the Timing Debug window, choose Path Category or Path List.
For the Innovus window, choose Data Path, or Path List.</td></tr>
</table>

Column List	Lists the columns in the order in which they appear in the table, left to right. Each entry has the following information: • Column title (for example, Name, Arc, Delay) • The width of the column • The alignment of text in column (center, left, right, leftright) • Procedure, if any • The existing value from the path information
Add	Adds a column to the column list.
Modify	Let you modify characteristics. Click on a column in the column list. Edit the information, then click modify.
Delete	Deletes a column from the column list.
Move Up	Moves a column up in the column list. This effectively moves a column to the left in the table.
Move Down	Moves a column down in the column list. This effectively moves a column to the right table.
Load	Opens the GTD Preferences form.

Timing Debug - Edit Table Columns - Load GTD Preferences File

Use the *Load GTD Preferences* form to load a tcl command file to use for editing table columns.

1. On the *Timing Debug* or *Timing Path Browser* form, then right-click on a path. Select *Edit Table Column*. The *Edit Table Column* form is displayed.
2. Click *Load*.



Timing Debug - Edit Table Columns - Load GTD Preferences File Fields and Options

File name	Specifies the file to load.

Timing Debug - File

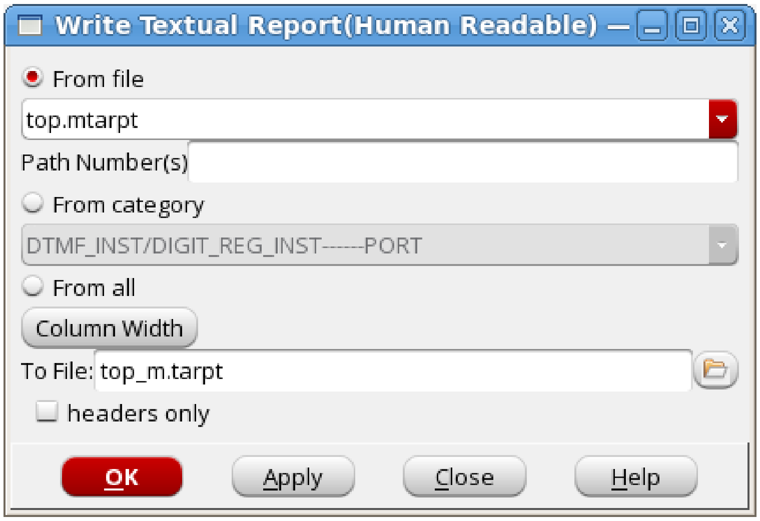
The Timing Debug - File lets you choose the following forms:

- Timing Debug - File - Write Text Report
- Timing Debug - File - Column Width Table
- Timing Debug - File - Write Category Report File
- Timing Debug - Timing Debug Preferences

Timing Debug - File - Write Text Report

Use the Write Text Report form to write a text file containing information about paths that have been loaded from a `.mtarpt` file from Timing Debug.

Note: The generated report cannot be read back into the timing debug environment.
→ Choose *Write Text Report* from the *File* menu of the Timing Debug report form.



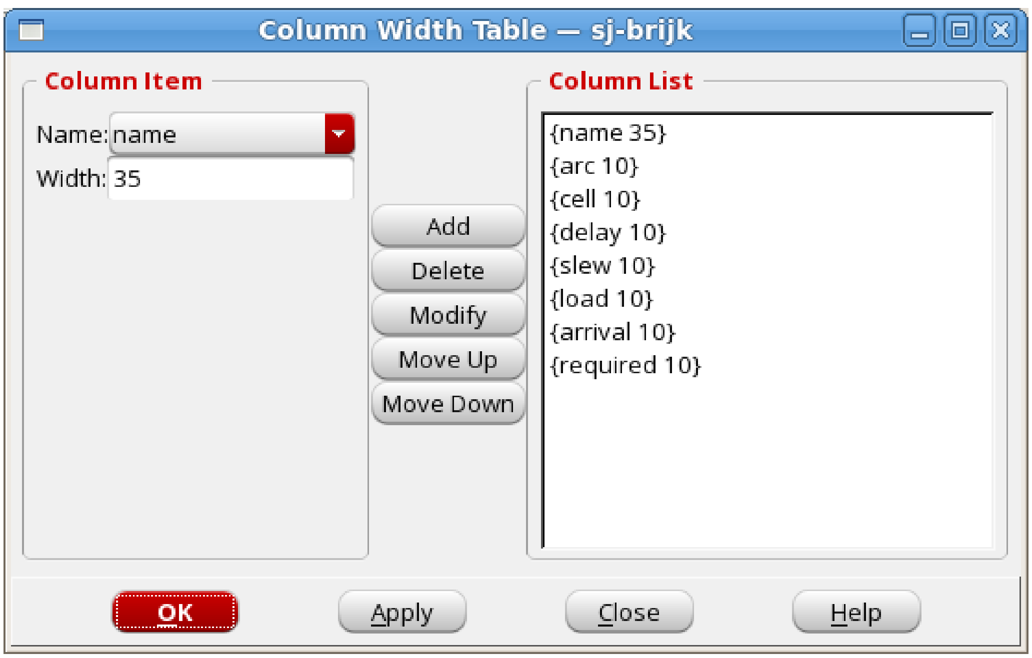
Timing Debug - Write Textual Report File Fields and Options

From file	Specifies the name of the `.mtarpt` file to read and convert to a text file. You cannot specify this parameter if you specify *From category*.
Path Number(s)	Writes a single number or path range separated by blank space " "or a comma ",". A path range is two numbers separated by a minus "-" sign. You can use this parameter only if a single file is specified or loaded.
From category	Specifies the category of paths to write to the text file.
From all	Writes all categories to the report file.
Column Width	Displays the Column Width Table form.

To File	Specifies the name of the text output file.
headers only	Writes the file header only. Use this parameter if you do not need a detailed table.

Timing Debug - File - Column Width Table

Use the Column Width Table form to change the width of the columns in the file created by the Write Textual Report form, and to specify the order in which you want to columns to appear.
→ Choose *Write Text Report* from the *File* menu on the Timing Debug form, then click on the *Column Width* button.



Write Text Report - Column Width Table Fields and Options

Name	Specifies the name of the column to add, modify, or move in the column list.
Width	Specifies the width of the column.

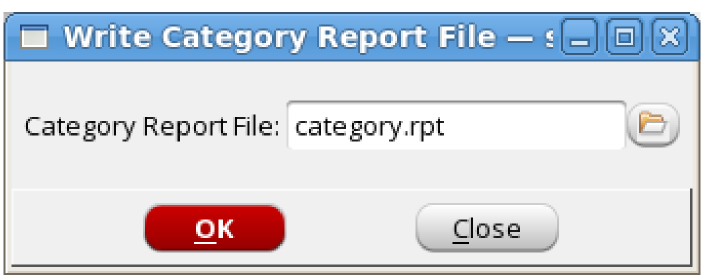
Column List	Specifies a list of columns to create in the report generated by the Write Textual Report form.
Add	Adds a column to the column list.
Delete	Deletes a column from the column list.
Modify	Enables you to modify the width of a selected column.
Move Up	Moves the selected column up one position in the column list.
Move Down	Moves the selected column down one position in the column list.

Timing Debug - File - Write Category Report File

Use the Write Category Report File form to write a text file containing the following information:

- Category name
- Total number of paths
- Number of passing paths
- Number of failing paths
- Worst negative slack
- Total negative slack
- TNS

→ Choose *File - Write Category Summary* on the Timing Debug form.



Timing Debug - Write Category Report Fields and Options

Category Report File	Specifies the name of the category output file. *Default*: `category.rpt`

Timing Debug - Timing Debug Preferences

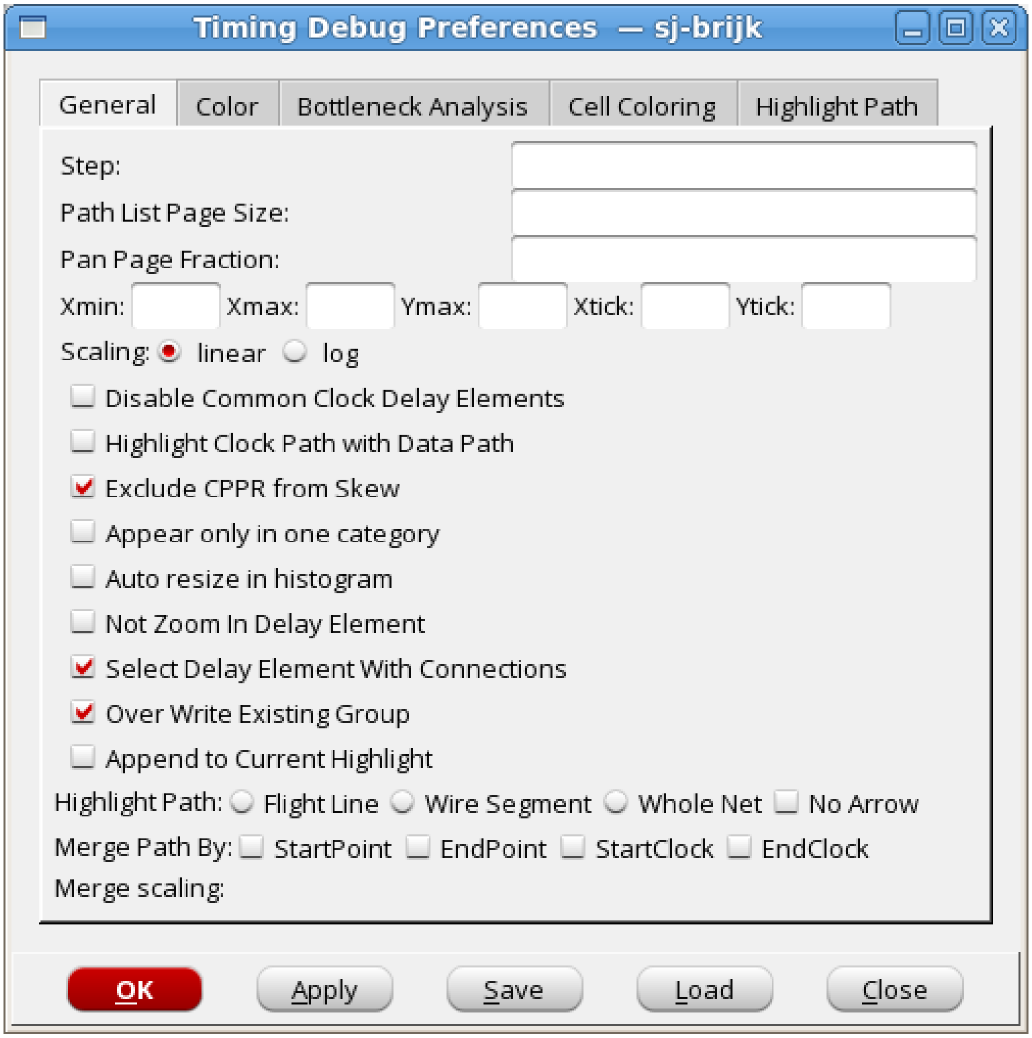
The Timing Debug Preferences form enables you to set general display settings and colors for various elements.

The Timing Debug Preferences form contains the following pages:

- Timing Debug Preferences - General
- Timing Debug Preferences - Color
- Timing Debug Preferences - Color - Select Color
- Timing Debug Preferences - Bottleneck Analysis
- Timing Debug Preferences - Select Color
- Timing Debug Preferences - Cell Coloring
- Timing Debug Preferences - Highlight Path

Timing Debug Preferences - General

Use the *General* page of the Timing Debug Preferences form to specify the statistics for the histogram, number of pages of report to be displayed in the form, and highlighting options.
→ Choose *Timing - Debug Timing - File - Preferences.*



Timing Debug Preferences Fields and Options

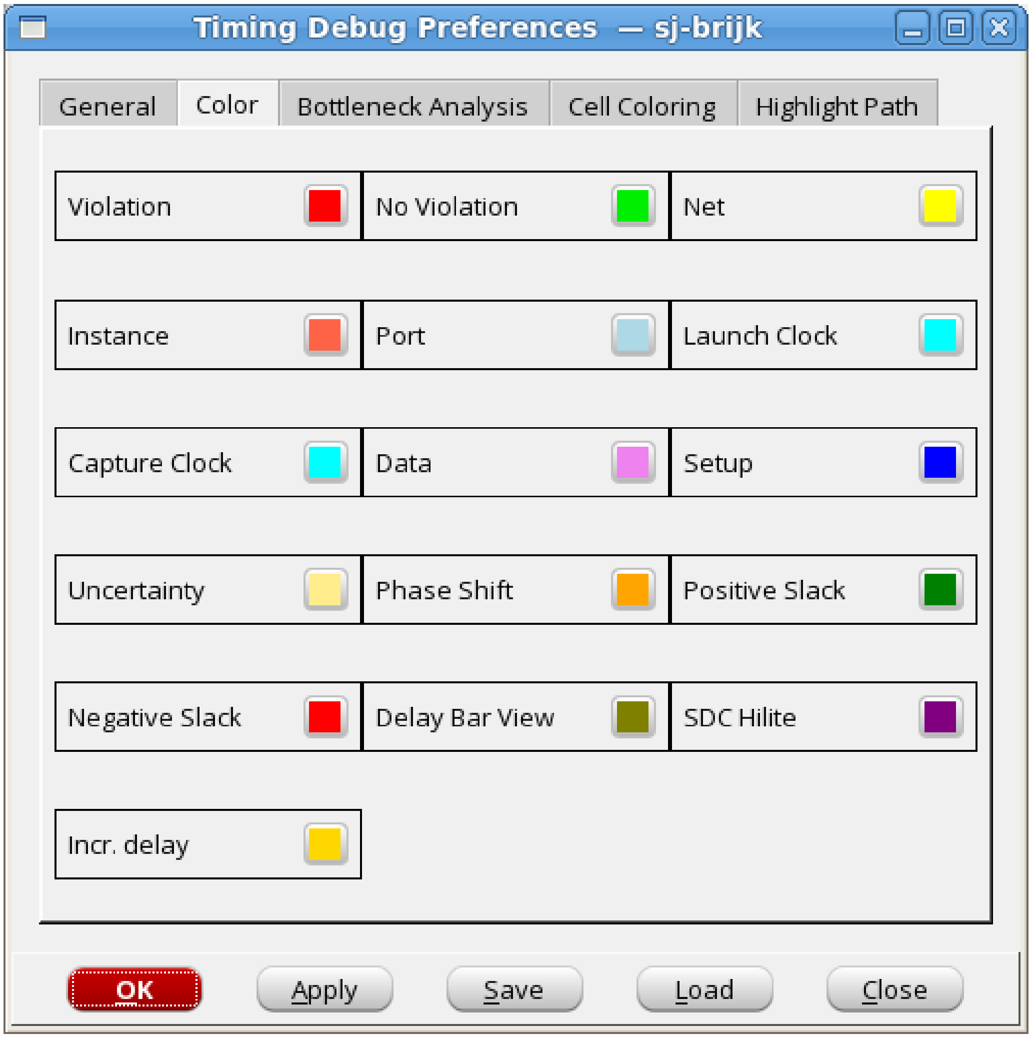
Step	Specifies the step size for the histogram.
Path List Page Size	Specifies number of pages of report to be displayed in the form.
Pan Page Fraction	Specifies the amount by which the histogram will be moved when you pan-in using the right-click options in the *Path Histogram* field in the Timing Debug window.
Disable Common Clock Delay Elements	

	Disables paths common to launch and capture clock in the *Data Delay* field of the *Timing Path Analyzer* form.
Highlight Clock Path with Data Path	
	Highlights clocks paths along with the data paths in the Design Display Area. By default, only data paths are highlighted.
Exclude CPPR from Skew	
	To exclude CPPR from Skew
Appear Only In One Category	
	If selected, the path will only appear in one category.
Auto resize in Histogram	
	Automatically resizes the histogram after minimizing or maximizing it.
Not Zoom In Delay Element	
	Zooms into the clicked instance or wire.
Select Delay Element With Connections	
	Displays the delay elements in the histogram.
Over Write Existing Group	
	Overwrites the existing path group with a new one.
Append to Current Highlight	
	Appends highlights to currently highlighted path.
Highlight Path	Specifies the preference for highlighting various paths. The color code used to highlight path is as follows: Red: Launch clock path Green: Paths specific to capture clock White: Data path Choose from one of the following options:

	Flight Line	Creates highlighted lines between the pins of the path.
	Wire Segment	Highlights the wire segment.
	Whole Net	Highlights all segments of the routing. The thickness of the highlight represents if the routing is part of the wire segments of the path (thicker) or if it is outside (thinner).
	No Arrow	In some case arrow markers will make actual path invisible, this check-box provides an option to turn off the arrow markers in highlighted path display.
Merger Path By	Specify the method to merge same path in views. Choose from one of the following options:	
	StartPoin	Merge the paths according to StartPoint.
	EndPoint	Merge the paths according to EndPoint.
	StartClock	Merge the paths according to launching clock.
	EndClock	Merge the paths according to capturing clock.
Merge Scaling	Specify the scaling number for each view. You can use this option after merging same path in views.	

Timing Debug Preferences - Color

Use the *Color* page of the Timing Debug Preferences form to specify the colors for the slack calculation bar elements in the Timing Path Analyzer form.
→ Choose *Timing - Debug Timing - File - Preferences*, and click on the *Color* tab.

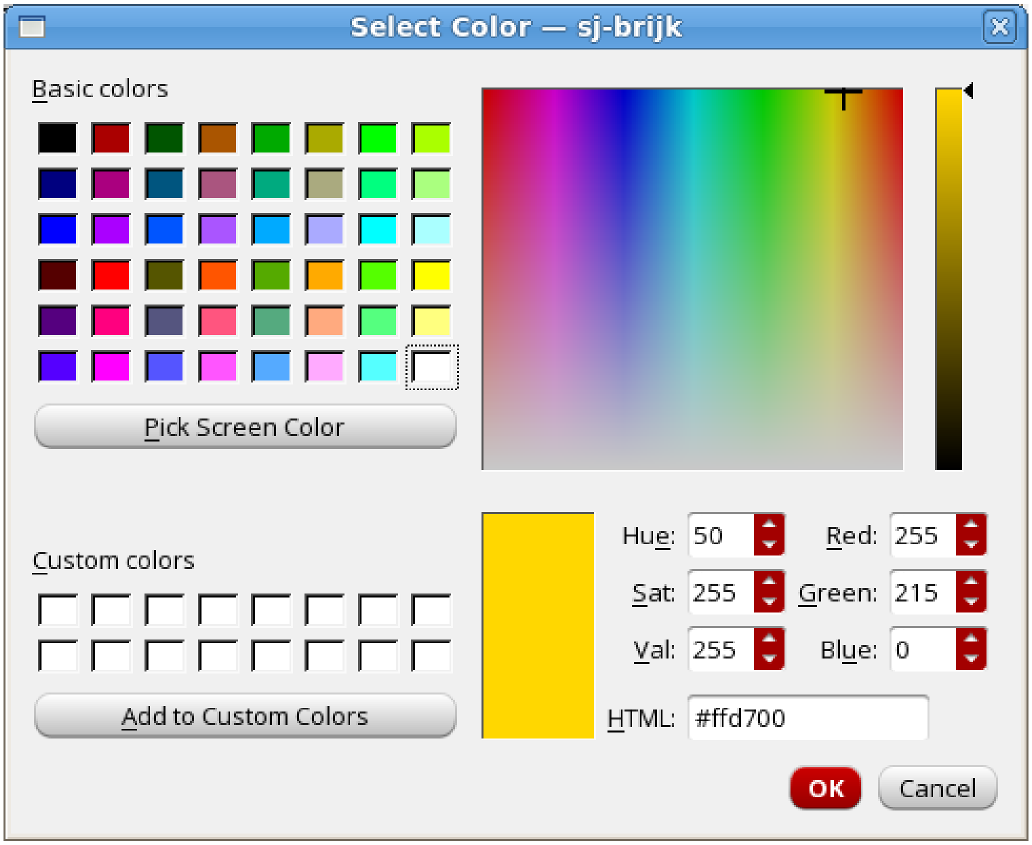

Timing Debug Preferences — sj-brijk
General
Color
Bottleneck Analysis
Cell Coloring
Highlight Path
Violation
No Violation
Net
Instance
Port
Launch Clock
Capture Clock
Data
Setup
Uncertainty
Phase Shift
Positive Slack
Negative Slack
Delay Bar View
SDC Hilite
Incr. delay
OK
Apply
Save
Load
Close

Timing Debug Preferences - Color Fields and Options

Elements	Displays the element name and the corresponding color that is used in the Slack Calculation field of the Timing Path Analyzer form. Click on a color square to display the *Set Color* form, which enables you to customize a color.
OK	Applies the selection and closes the form.
Apply	Stores the selected color information without closing the form.
Save	Saves the selection.
Load	Loads the selected color information in the tool.
Close	Closes the form without saving the selection.

Timing Debug Preferences - Color - Select Color

Use the *Select Color <Element Name>* form lets you customize the colors displayed on the Timing *Debug Preferences - Color* page.
→ Choose *Timing - Debug Timing - File - Preferences*, click on the *Color* tab, then click on any colored square.

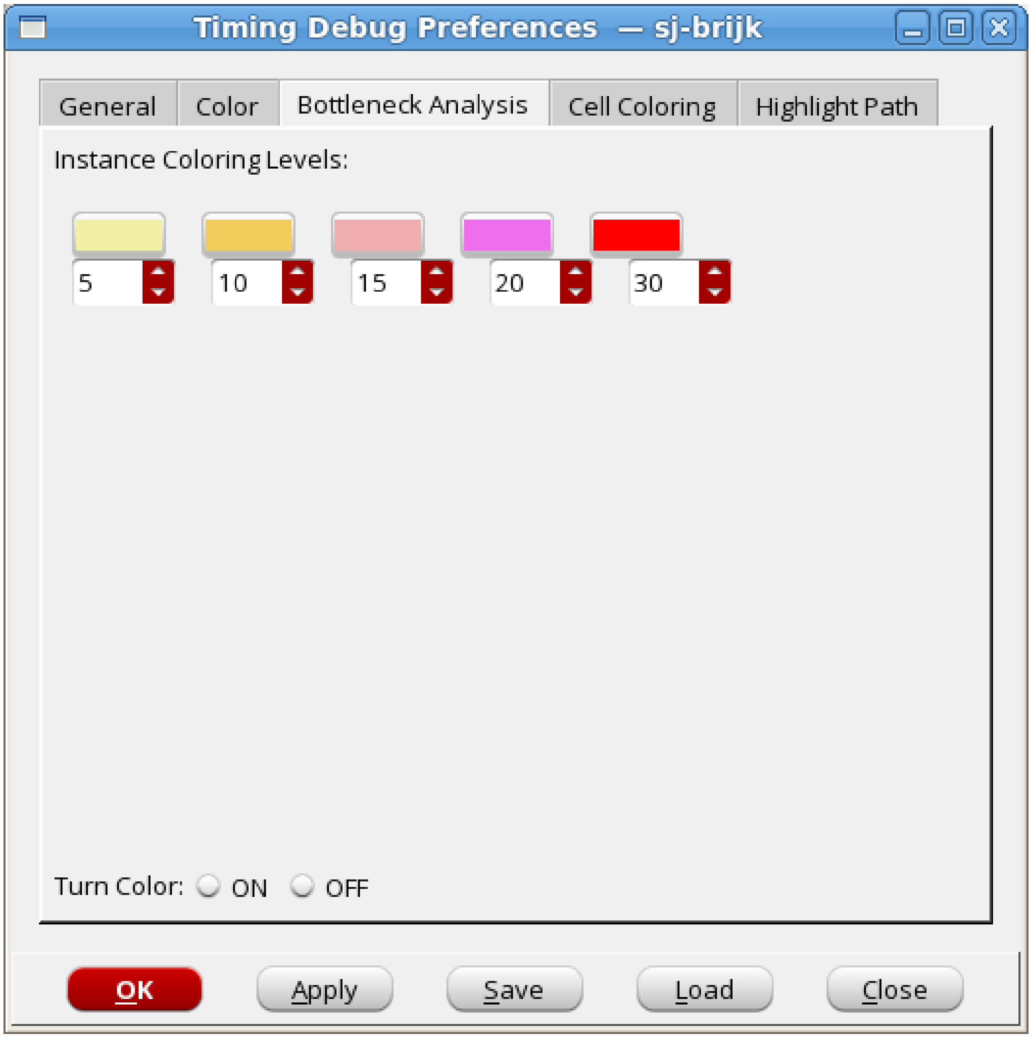


Timing Debug Preferences - Color - Set Color Violation Fields and Options

Elements	Sliders let you set the hue for the red, green, and blue colors comprising your custom color.

Timing Debug Preferences - Bottleneck Analysis

Use the *Bottleneck* page of the Timing Debug Preferences form to colorize cells based on the occurrences of violating paths.
→ Choose *Timing - Debug Timing - File - Preferences*, and click on the *Bottleneck Analysis* tab.


Timing Debug Preferences — sj-brijk
General
Color
Bottleneck Analysis
Cell Coloring
Highlight Path
Instance Coloring Levels:
5
10
15
20
30
Turn Color:
ON
OFF
OK
Apply
Save
Load
Close

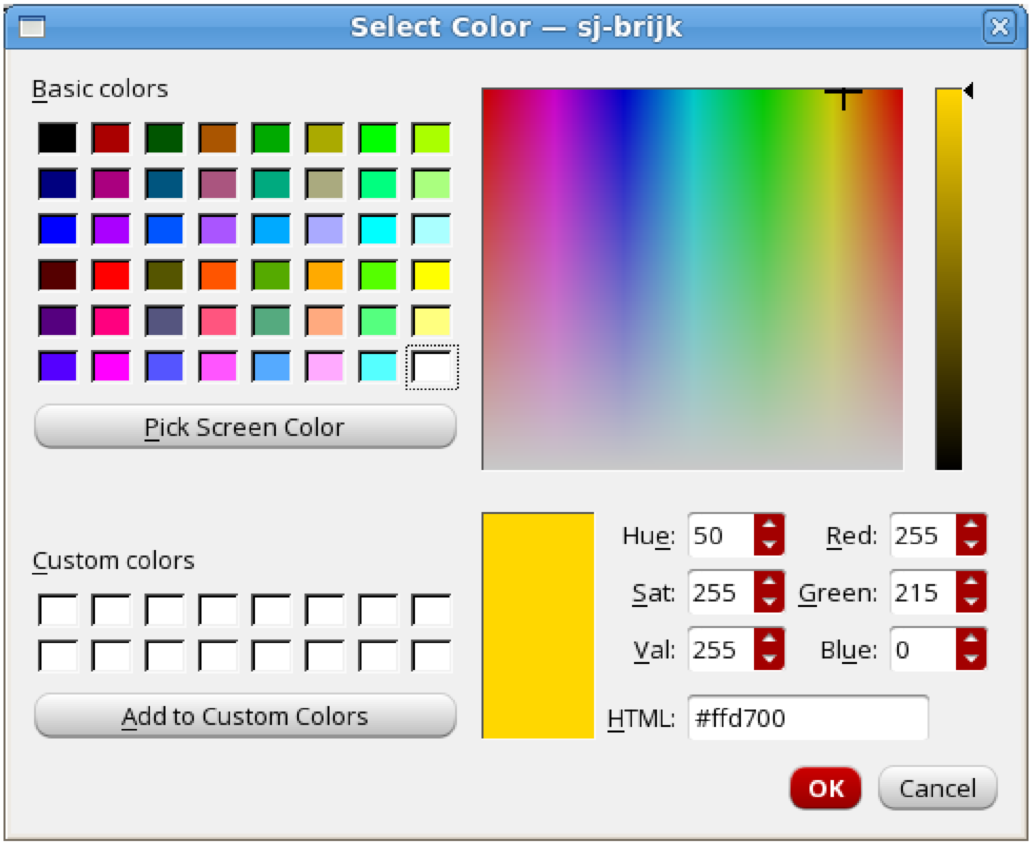
Timing Debug Preferences - Bottleneck Analysis Fields and Options

Instance Coloring Levels		
	Specifies color corresponding to the number of times an instance can appear in the violating path. In the delay bar in on the Timing Path Analyzer GUI, the tool colorizes cells accordingly. In this example, cells appearing in greater than five and 10 violating paths will be colored yellow. Cells appearing in between 10 and 15 times will be colored orange. Cells appearing in between 15 and 20 times will be colored pink. Cells appearing in between 20 and 30 times will be colored fuchsia and cells appearing more than 30 or more times will be colored red.	
Turn Color	Specifies how the tool colorizes the instances.	
	ON	Displays the colors you selected.
	OFF	Uses the default colors.
OK	Closes the form with saving your color information preferences.	
Apply	Stores the selected color information.	
Save	Saves the GTD preference file to your machine.	
Load	Allows you to select a GTD preference file from your machine for loading.	
Close	Closes the form.	

Timing Debug Preferences - Select Color

Use the *Select Color* form to set custom colors for the *Bottleneck Analysis* and *Cell Coloring* form.
➝ Choose *Timing - Debug Timing - File - Preferences*, click on the *Bottleneck Analysis* tab, then click on a color.

or
➝ Choose *Timing - Debug Timing File - Preferences*, click on the *Cell Coloring* tab, then click on a color.



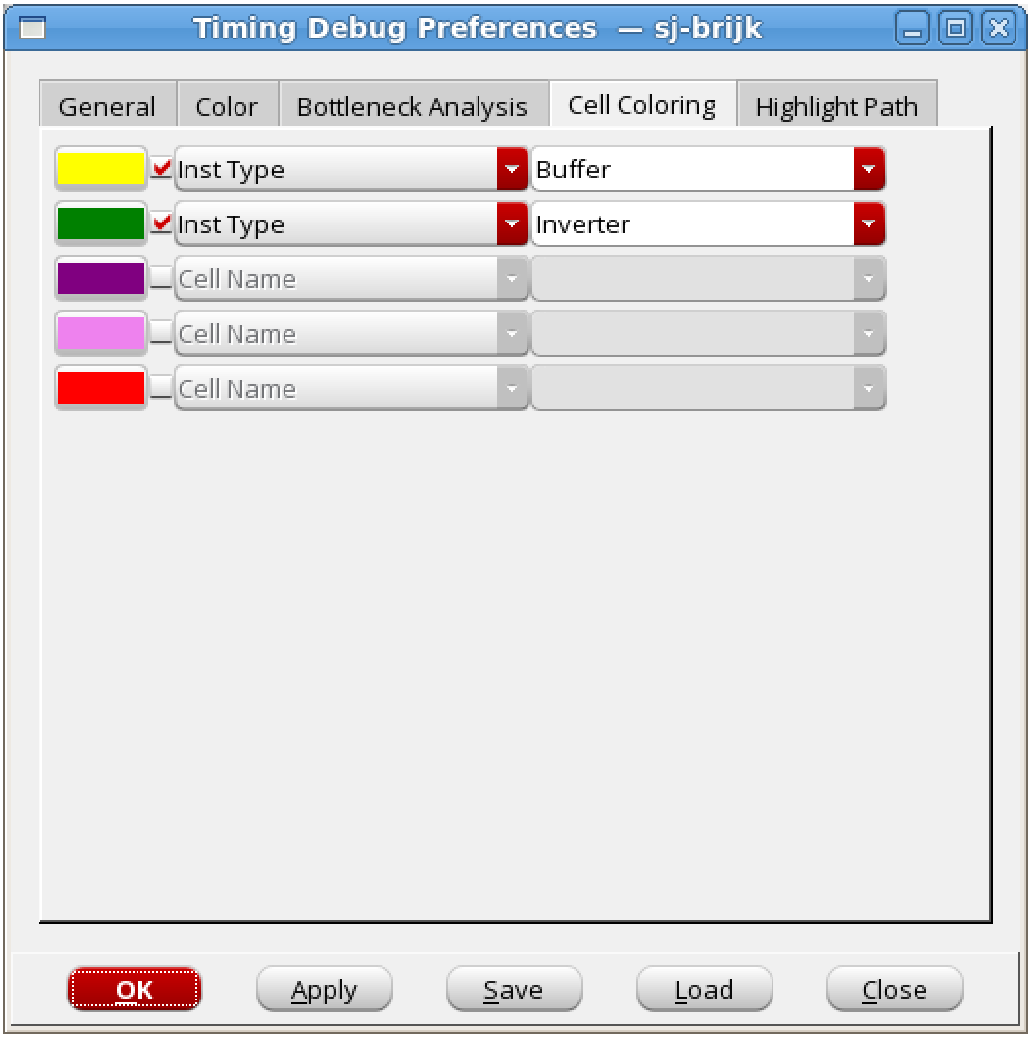
Timing Preferences - Set Color Fields and Options

Elements	Sliders let you set the hue for the red, green, and blue colors comprising your custom color.

Timing Debug Preferences - Cell Coloring

Use the *Cell Coloring* page of the Timing Debug Preferences form to choose colors for specific cells in the delay bar. Color precedence is top to bottom in this form. If you set coloring in a session, the software saves the settings and restores them in the next session.

→ Choose *Timing - Debug Timing - File - Preferences*, and click on the *Cell Coloring* tab.

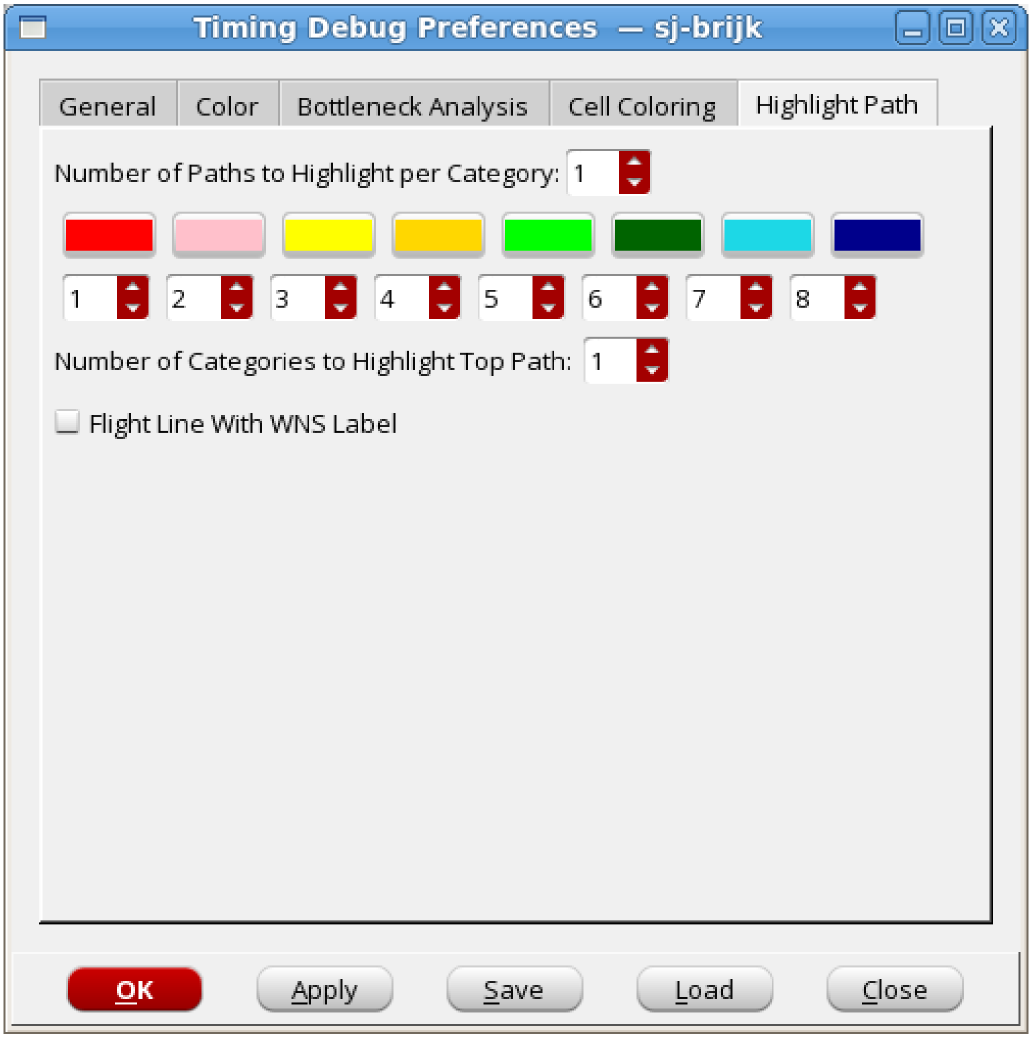

Timing Debug Preferences — sj-brijk
General
Color
Bottleneck Analysis
Cell Coloring
Highlight Path
Inst Type
Buffer
Inst Type
Inverter
Cell Name
Cell Name
Cell Name
OK
Apply
Save
Load
Close

Timing Debug Preferences - Cell Coloring Fields and Options

Color elements	Shows the available colors. To customize colors, click on the color. The *Set Color* form is displayed.
Check Box Elements	Indicates whether you want to apply the color to the specified cells.
Cell Name Selection Elements	For each color, you can choose to provide one of the following • Cell name • Instance • Procedure that you have defined. The procedure is invoked with the full instance name as the argument. You must source the file containing the procedure before you use this feature. For an example, see "Cell Coloring."
Name Elements	Lets you enter the cell names or procedure name. You can use wildcards when you specify cells, for example: `INV*`, `BUF*`, `DLY*`, `HVT*`.

Timing Debug Preferences - Highlight Path

Use the Highlight Path page of the Timing Debug Preferences form to specify the colors and category numbers for color coded critical paths highlighting of categories.
→ *Choose Timing - Debug Timing - File - Preferences, and click on the Highlight Path tab.*


Timing Debug Preferences — sj-brijk
General
Color
Bottleneck Analysis
Cell Coloring
Highlight Path
Number of Paths to Highlight per Category: 1
1
2
3
4
5
6
7
8
Number of Categories to Highlight Top Path: 1
Flight Line With WNS Label
OK
Apply
Save
Load
Close

Timing Debug Preferences - Highlight Path Fields and Options

Number of Paths of Highlight per category	
	Specify the number of paths per category to be highlighted. The valid value should be from 0 to 30. *Default:* 8. It means 8 critical paths per category will be highlighted.
Number of Categories to Highlight Top Path	
	Specify the number of categories to be highlighted. The valid value should be from 0 to 30. *Default:* 8. It means 8 categories will be highlighted.
Flight Line With WNS Label	
	Specify whether to add WNS Label when highlighting a path with the flight line.

Timing Debug - Analysis

The Timing Debug - Analysis menu provide the following forms for timing path analysis:

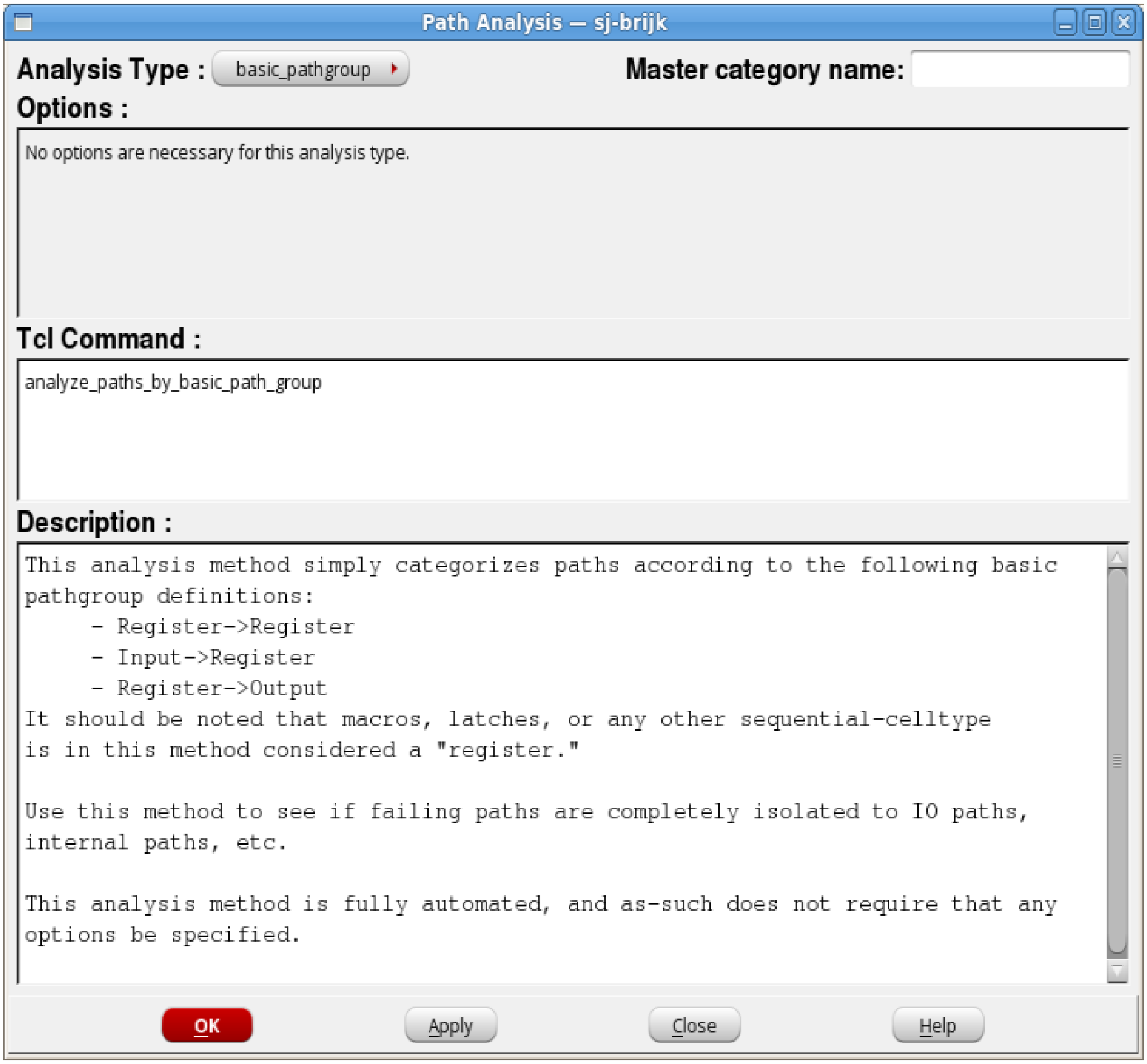
- Path Analysis (Path Group Analysis)
- Path Analysis (Clock Analysis)
- Path Analysis (Hierarchical Floorplan)
- Path Analysis (Hierarchical Port)
- Path Analysis (View Analysis)
- Path Analysis (Critical False Path)
- Path Analysis (Bottleneck Analysis)
- Path Analysis (DRV Analysis)
- Path Analysis (Noise Result Analysis)
- Path Analysis (Hierarchical Analysis Viewer)
- Path Analysis (Clock Matrix Viewer)

Path Analysis (Path Group Analysis)

Use the Path Analysis form to create standard path categories according to basic path groups. The basic path groups are:

- Register to register
- Input to register
- Register to output
- Input to Output

Registers can be macros, latches, or sequential-celltypes.
→ Choose *Timing - Debug Timing - Analysis - Path Group Analysis.*



Path Group Analysis Fields and Options

Options	There are no additional options for this analysis.
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `analyze_paths_by_basic_path_group`

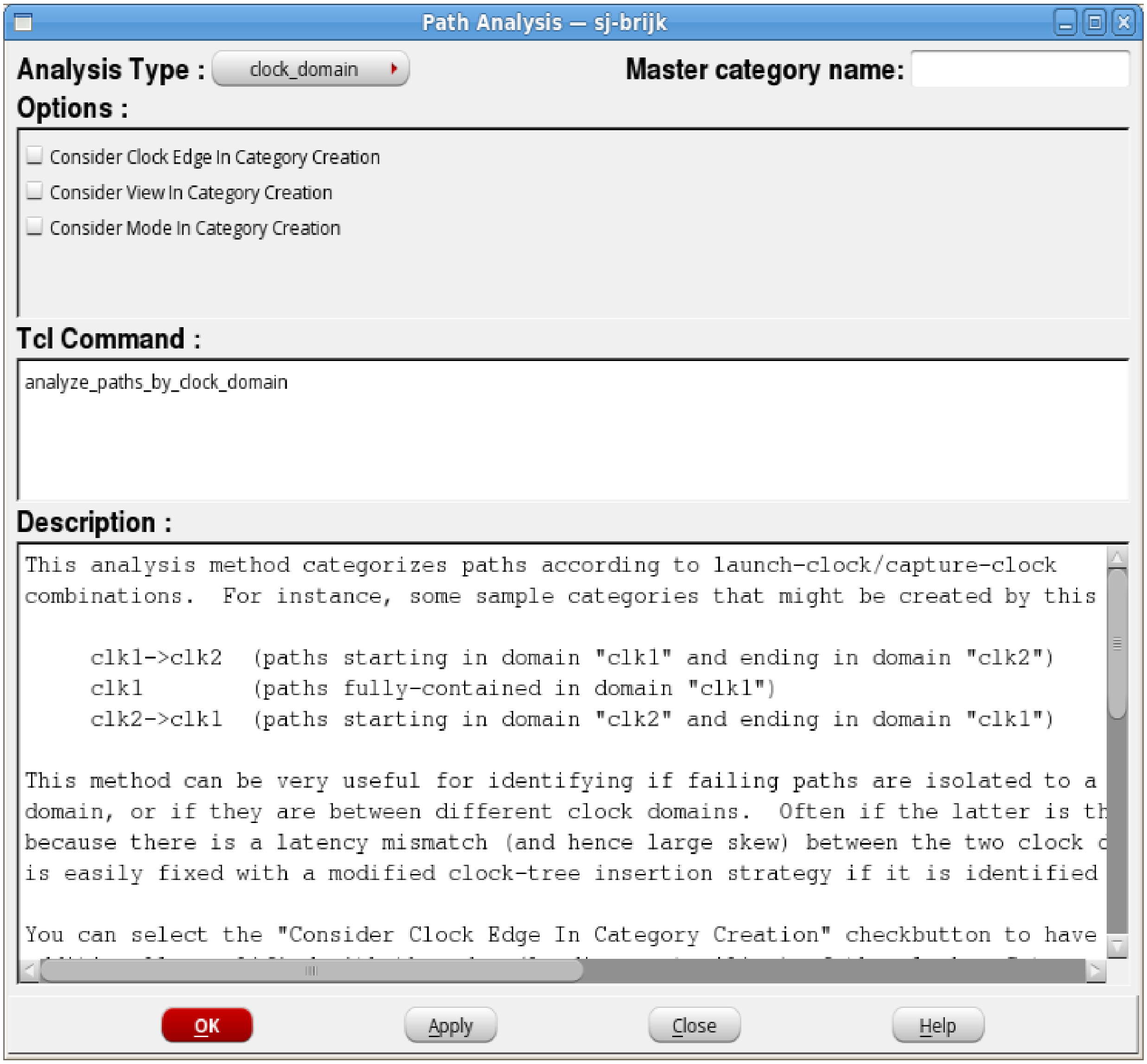
For more information, see "Timing Debug Commands" in the *Text Command Reference* document.

Path Analysis (Clock Analysis)

Use the Path Analysis form to create categories according to launch clock-capture clock combinations. Following categories are created:

- Paths with clock fully contained in a single domain, clk1.
- Paths with clocks starting one clock domain and ending at another, clk1->clk2.

→ Choose *Timing - Debug Timing - Analysis - Clock Analysis.*


Path Analysis — sj-brijk
Analysis Type :
clock_domain
Master category name:
Options :
Consider Clock Edge In Category Creation
Consider View In Category Creation
Consider Mode In Category Creation
Tcl Command :
analyze_paths_by_clock_domain
Description :
This analysis method categorizes paths according to launch-clock/capture-clock
combinations. For instance, some sample categories that might be created by this
clk1->clk2 (paths starting in domain "clk1" and ending in domain "clk2")
clk1 (paths fully-contained in domain "clk1")
clk2->clk1 (paths starting in domain "clk2" and ending in domain "clk1")
This method can be very useful for identifying if failing paths are isolated to a
domain, or if they are between different clock domains. Often if the latter is th
because there is a latency mismatch (and hence large skew) between the two clock c
is easily fixed with a modified clock-tree insertion strategy if it is identified
You can select the "Consider Clock Edge In Category Creation" checkbutton to have
OK
Apply
Close
Help

Path Analysis (Clock Analysis) Fields and Options

Consider Clock Edge in Category creation (Optional)	
	Considers leading or trailing edge of the clock while defining categories.
Consider View in Category Creation	
	Considers views while defining categories. The paths are sorted according to the clock(s) and the view, for example: Clock1<View1> Clock1<View2> ...
Consider Mode in Category Creation	
	Considers modes while defining categories. The mode is retrieved from the view definition loaded into the design, then the paths are sorted according to the clocks and the mode, for example: Clock1<Mode1> Clock1<Mode2>...
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Related Text Commands

The following text command provides equivalent or additional functionality:

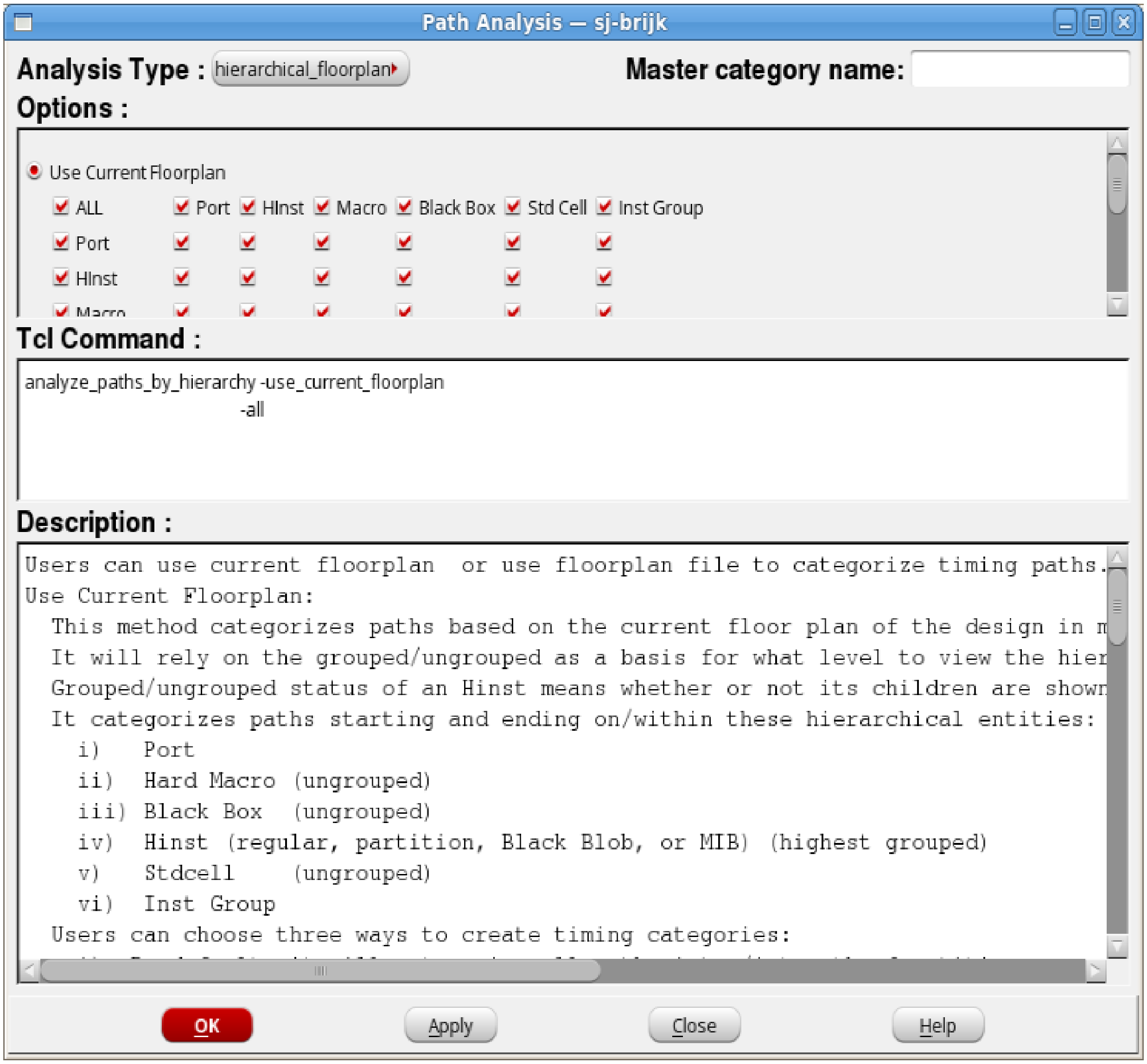
- `analyze_paths_by_clock_domain`

For more information, see "Timing Debug Commands" in the *Text Command Reference* document.

Path Analysis (Hierarchical Floorplan)

Use the Path Analysis form to create categories according to the hierarchical floorplan characteristics of the paths. The software uses the floorplan files to extract information for guides, fences or Macros.

→ Choose *Timing - Debug Timing - Analysis - Hierarchical Floorplan.*

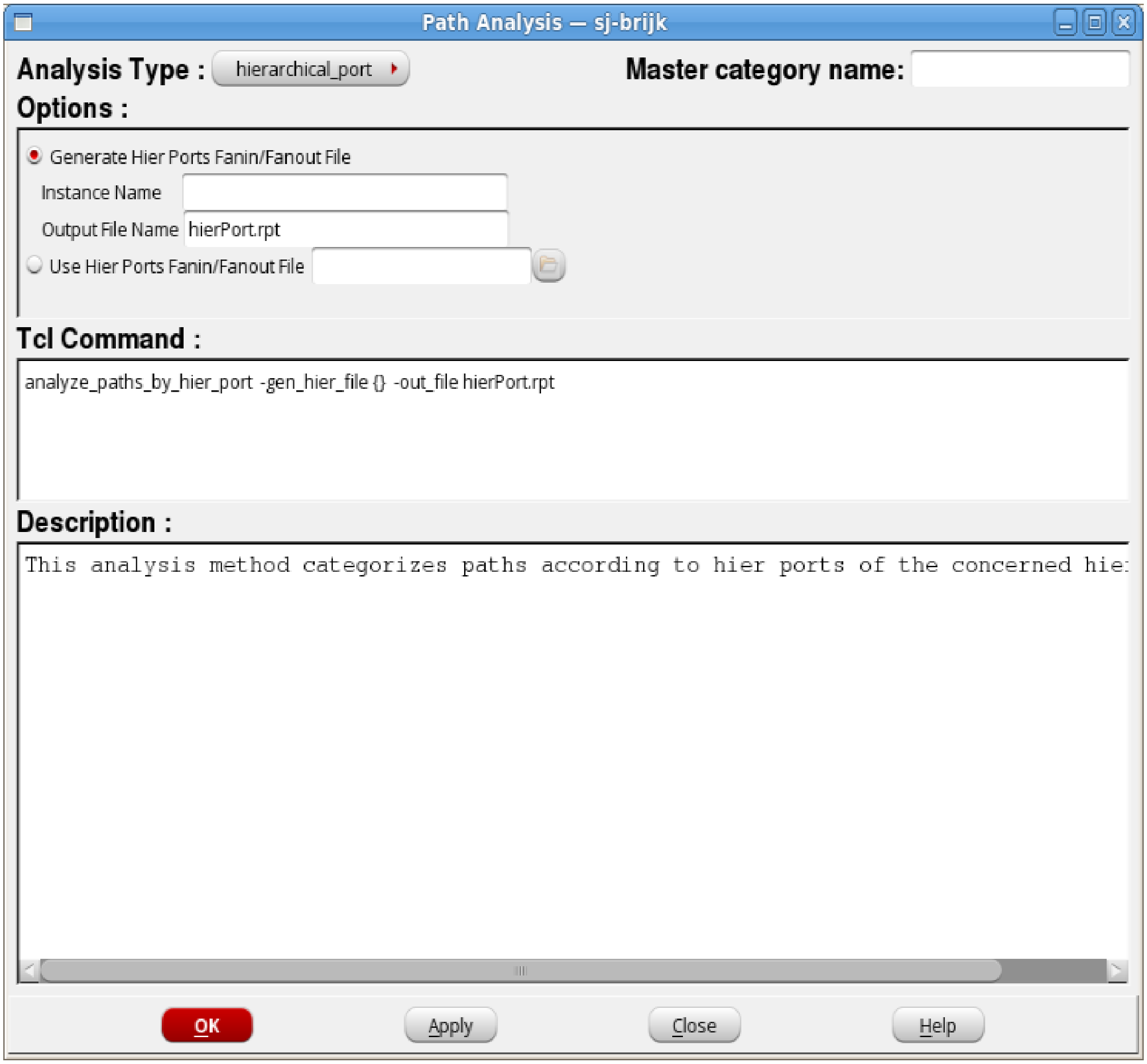

Path Analysis — sj-brijk
Analysis Type : hierarchical_floorplan
Master category name:
Options :
Use Current Floorplan
ALL Port HInst Macro Black Box Std Cell Inst Group
Port
HInst
Tcl Command :
analyze_paths_by_hierarchy -use_current_floorplan
-all
Description :
Users can use current floorplan or use floorplan file to categorize timing paths.
Use Current Floorplan:
This method categorizes paths based on the current floor plan of the design in m
It will rely on the grouped/ungrouped as a basis for what level to view the hier
Grouped/ungrouped status of an Hinst means whether or not its children are shown
It categorizes paths starting and ending on/within these hierarchical entities:
i) Port
ii) Hard Macro (ungrouped)
iii) Black Box (ungrouped)
iv) Hinst (regular, partition, Black Blob, or MIB) (highest grouped)
v) Stdcell (ungrouped)
vi) Inst Group
Users can choose three ways to create timing categories:
OK
Apply
Close
Help

Path Analysis (Hierarchical Floorplan) Fields and Options

Use Current Floorplan	Uses the current floorplan for hierarchical analysis.
Check Box	Specifies different types of combination of categories and can be used when using the current floorplan. *Default:* All types.
Use Floorplan File	Specify the name of the floorplanning file to be used for extracting the object information.
Consider Macros In Category Creation	
	Considers macros in addition to guides and fences for creating categories.Can be used when using floorplan file. By default, macros are not considered.
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Path Analysis (Hierarchical Port)

Use the Path Analysis form to create categories according to the hierarchical port characteristics of the paths. The software uses the port files to extract information for guides, fences or Macros.
→ Choose *Timing - Debug Timing - Analysis - Hierarchical Port.*



Note: The hierarchical ports Fanin/Fanout file is mutually related to the Timing Debug report.

Path Analysis (Hierarchical Port) Fields and Options

Generate Hier Ports Fanin/Fanout File	Hier ports are generated through the Fanin/Fanout file on selecting this radio button.
Instance Name	Specifies the instance name for the hier ports to be generated.
Output File Name	Specifies the output file name for the hier ports to be generated.
Use Hier Ports Fanin/Fanout File	Allows you to select a Fanin/Fanout file for generating the hier ports.
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Related Text Commands

The following text command provides equivalent or additional functionality:

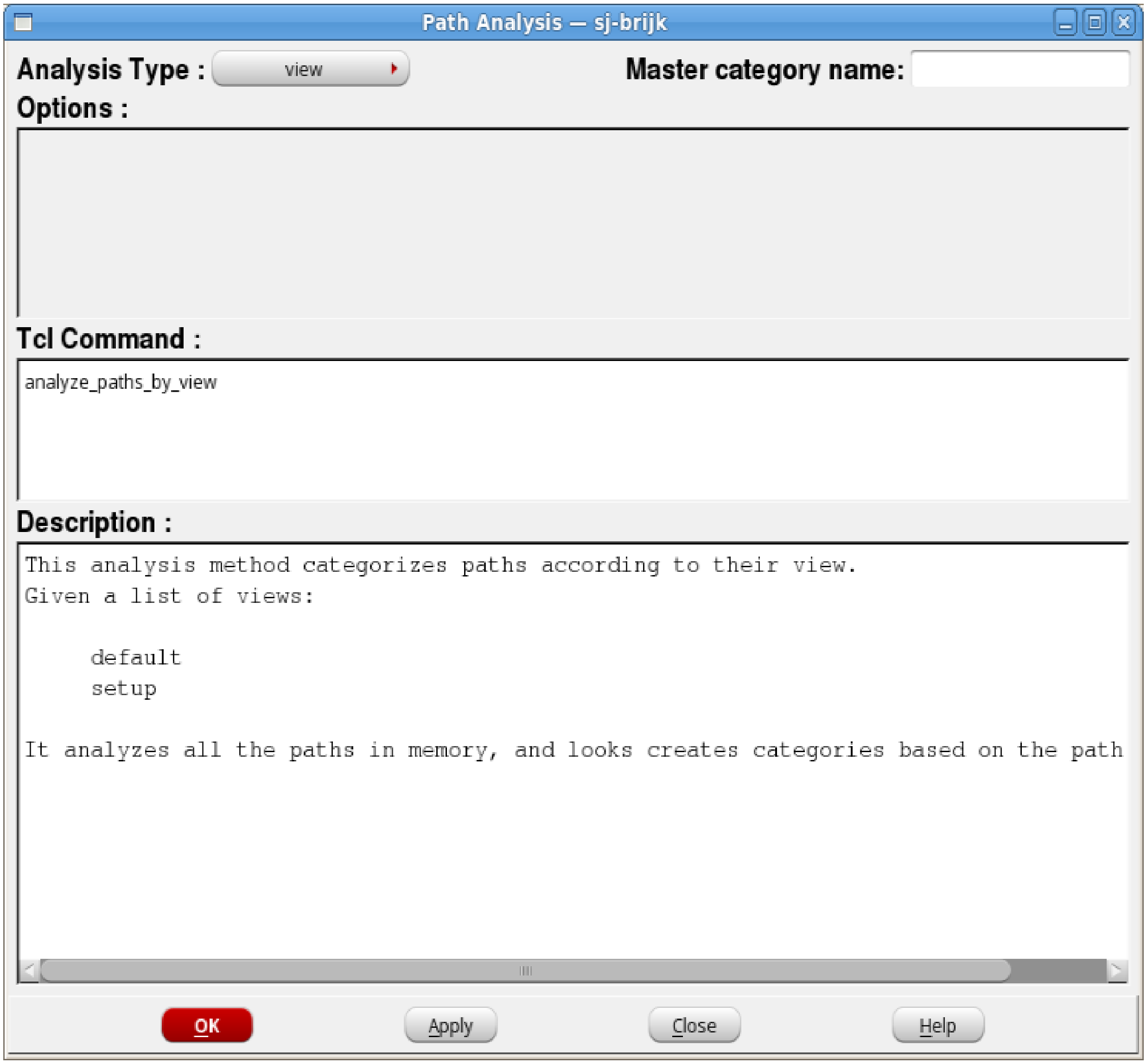
- `analyze_paths_by_hierarchy`

For more information, see "Timing Debug Commands" in the *Text Command Reference* document.

Path Analysis (View Analysis)

Use the Path Analysis form to create categories according to the view that each path is related to. You can analyze the impact of each view on the performance using this category.

Note: In a single report (report containing all views together) each endpoint is reported once. On the other hand, when you load several reports that were generated for different views, each endpoint may appear in each report with a different slack value.
→ Choose *Timing - Debug Timing - Analysis - View Analysis.*



Path Analysis (View Analysis) Fields and Options

Options	There are no additional options for this analysis.
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Related Text Commands

The following text command provides equivalent or additional functionality:

analyze_paths_by_view

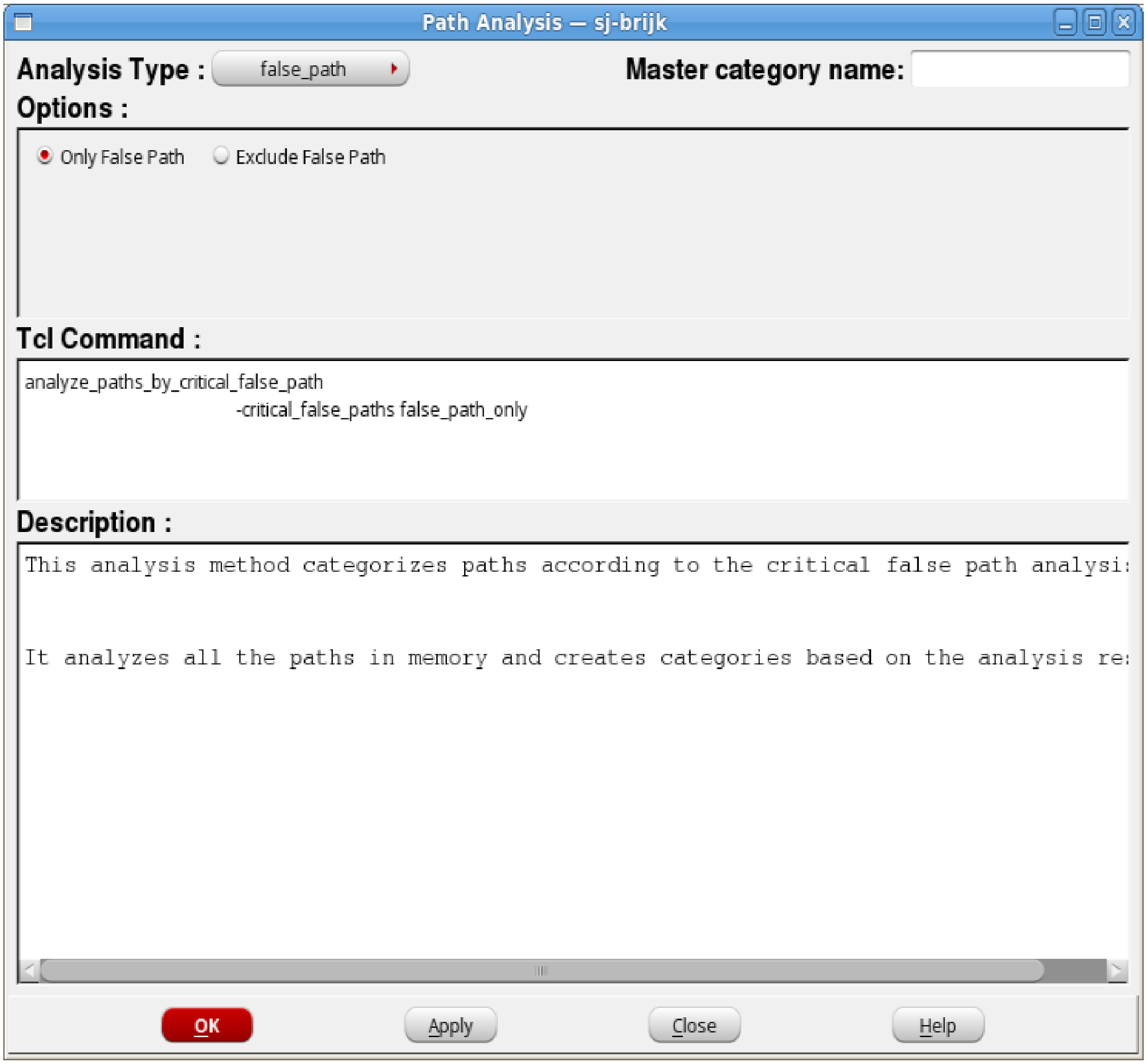
For more information, see "Timing Debug Commands" in the *Text Command Reference* document.

Path Analysis (Critical False Path)

Use the Path Analysis form to determine whether the reported paths are real critical paths. The analysis is performed by the Conformal Constraint Designer (CCD). As a result of this analysis, the tool creates a category in the *Global Timing Debug* window that contains either the violating paths only, or violating paths except for false paths.

→ Choose *Timing - Debug Timing - Analysis - Critical False Path.*

→ Choose analysis type as false_path.


Path Analysis — sj-brijk
Analysis Type :
false_path
Master category name:
Options :
Only False Path
Exclude False Path
Tcl Command :
analyze_paths_by_critical_false_path
-critical_false_paths false_path_only
Description :
This analysis method categorizes paths according to the critical false path analysi
It analyzes all the paths in memory and creates categories based on the analysis re
OK
Apply
Close
Help

Path Analysis (Critical False Path) Fields and Options

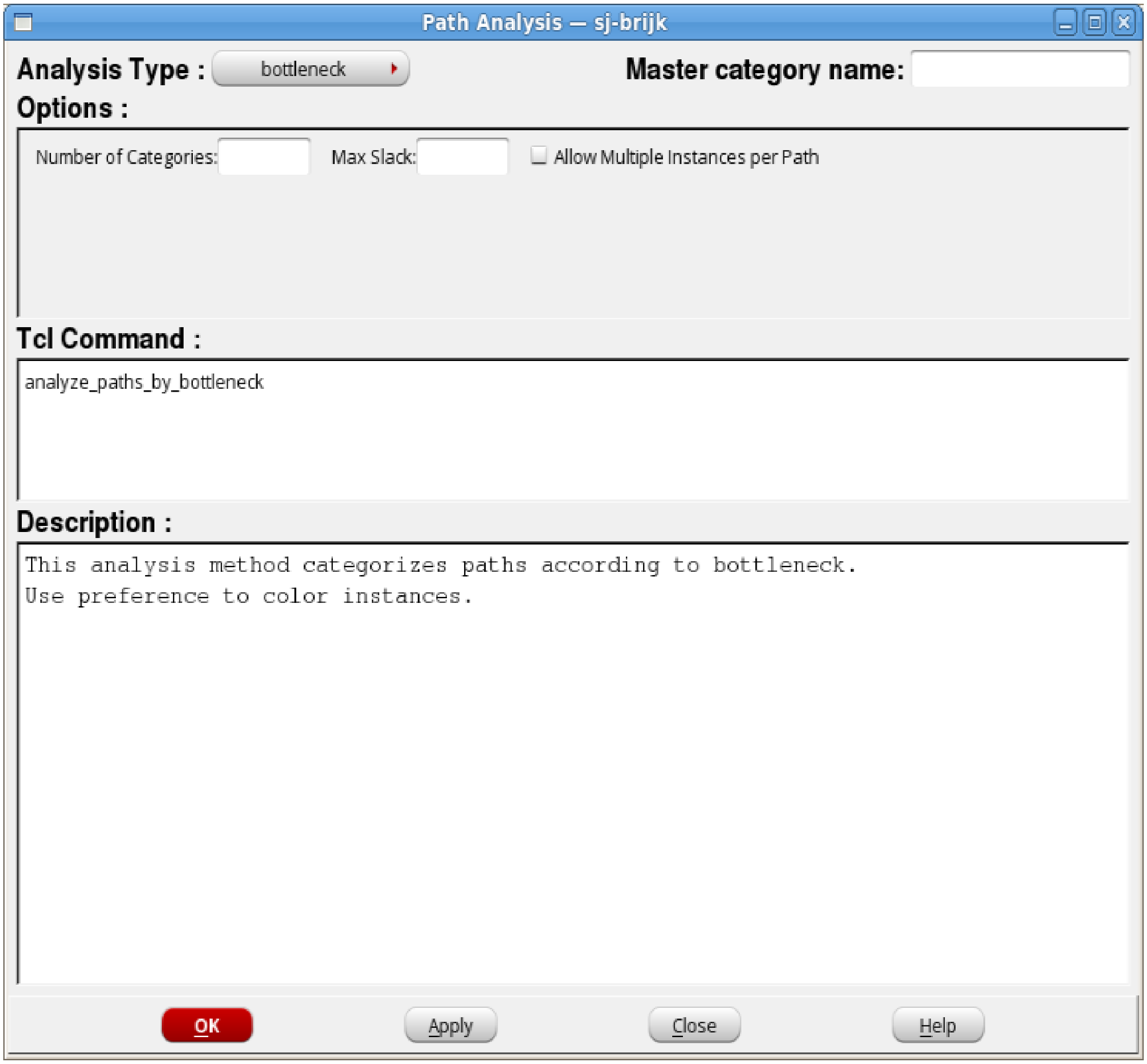
Only False Path	Creates a category containing violating false paths only.
Exclude False Path	Creates a category containing all paths other than false paths.
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Path Analysis (Bottleneck Analysis)

Use the Path Analysis form to create categories according to the bottleneck analysis of the critical paths. Bottleneck Analysis detects the instances that are often involved in the critical paths in the design. Any change in timing for these instances impacts multiple critical paths in the design. Therefore you can use this information to change your design (floorplan, placement, constraints etc.) around these instances. The bottleneck analysis computes the number of occurrences that an instance appears in the paths that you display in the Timing Debug window, and provides the following output:

- Colors most used instance based on number of occurrences.
- Creates N number of path categories for the instances with the highest number of occurrences. N is the number you specify in the Path Analysis form.

→ Choose *Timing - Debug Timing - Analysis - Bottleneck Analysis.*

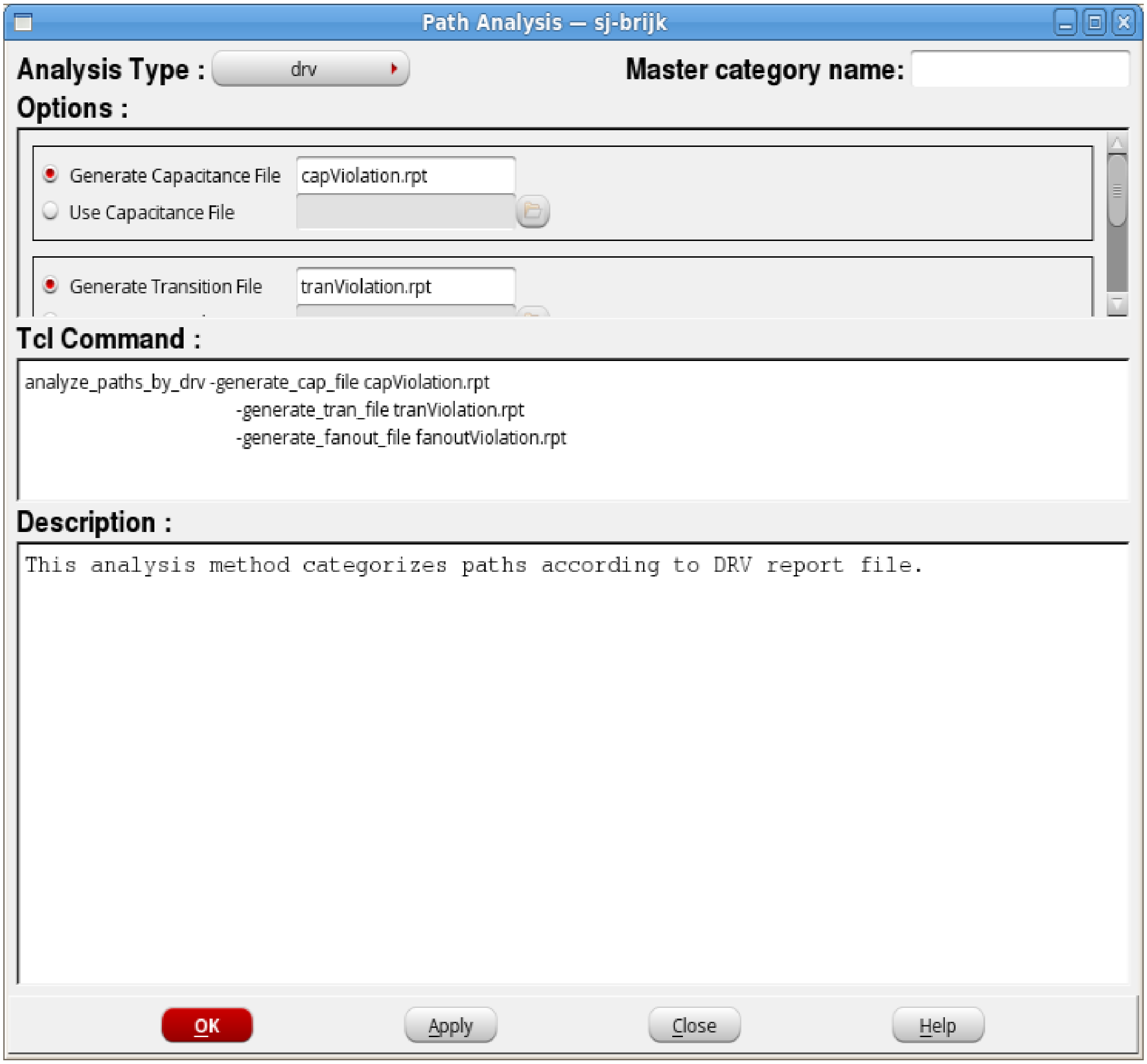

Path Analysis — sj-brijk
Analysis Type :
bottleneck
Master category name:
Options :
Number of Categories:
Max Slack:
Allow Multiple Instances per Path
Tcl Command :
analyze_paths_by_bottleneck
Description :
This analysis method categorizes paths according to bottleneck.
Use preference to color instances.
OK
Apply
Close
Help

Path Analysis (Bottleneck Analysis) Fields and Options

Number of Categories	Specifies the number of categories to be created for most occurring instances. To specify the number of instances to be grouped in one category and related colors, use the Timing Debug preferences form. For more information on the Timing Debug Preferences form, see "Timing Debug - Timing Debug Preferences" .
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Path Analysis (DRV Analysis)

Use the Path Analysis form to read or generate a report containing max transition, max capacitance, and max fanout violations. Paths that are affected by the selected DRV type are grouped into a category.
→ Choose *Timing - Debug Timing - Analysis - DRV Analysis.*


Path Analysis — sj-brijk
Analysis Type :
drv
Master category name:
Options :
Generate Capacitance File
capViolation.rpt
Use Capacitance File
Generate Transition File
tranViolation.rpt
Tcl Command :
analyze_paths_by_drv -generate_cap_file capViolation.rpt
-generate_tran_file tranViolation.rpt
-generate_fanout_file fanoutViolation.rpt
Description :
This analysis method categorizes paths according to DRV report file.
OK
Apply
Close
Help

Path Analysis (drv) Fields and Option

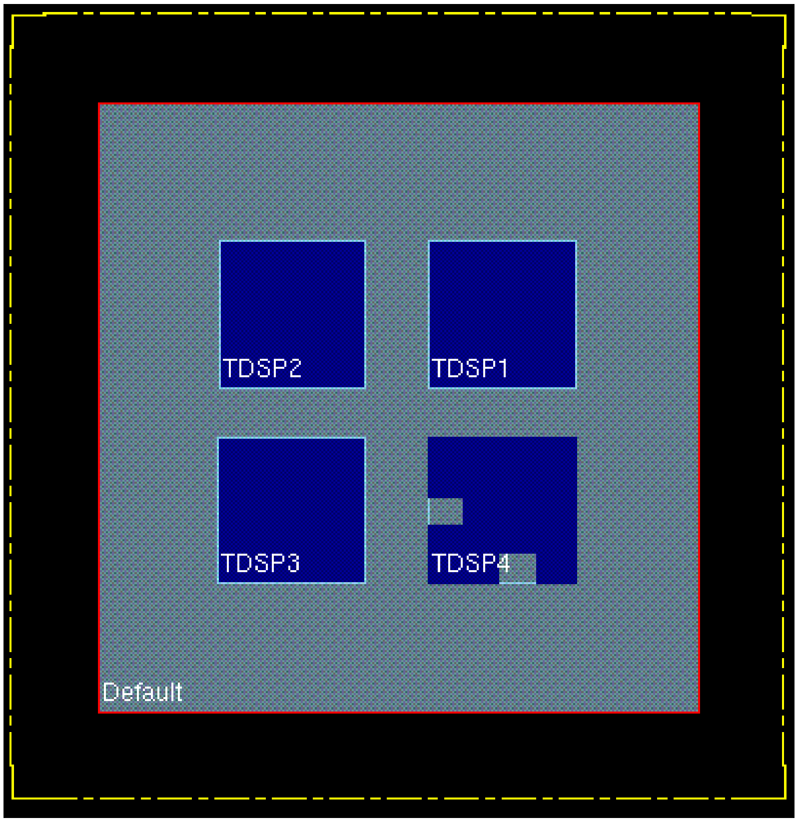
Generate Capacitance File	
	Generates a file containing a list of paths containing max capacitance violations.
Use Capacitance File	
	Reads a file containing a list of paths containing max capacitance violations.
Generate Transition File	
	Generates a file containing a list of paths containing max transition violations.
Use Transition File	
	Reads a file containing a list of paths containing max transition violations.
Generate Fanout File	
	Generates a file containing a list of paths containing max fanout violations.
Use Fanout File	Reads a file containing a list of paths containing max fanout violations.

Path Analysis (Noise Result Analysis)

Use the Path Analysis form to read or display the noise results.
→ Choose *Timing - Debug Timing - Analysis - Noise Result Analysis.*

Hierarchical Analysis Viewer

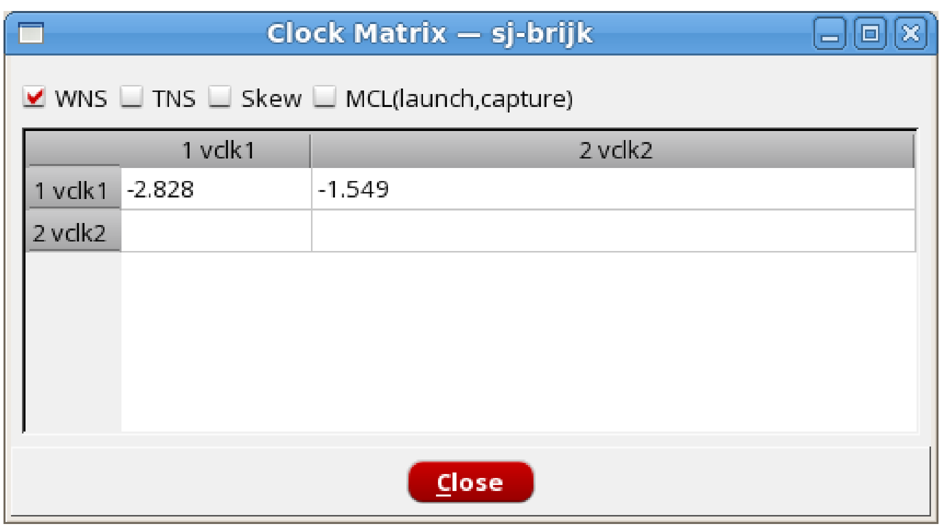
Use the Hierarchical Analysis Viewer form to view the results from hierarchical analysis that is done when you create the hierarchical paths category.
→ Choose *Timing - Debug Timing - Analysis - Hierarchical Analysis Viewer.*



Clock Matrix Viewer

Use the Clock Matrix Viewer to show the relationship of source and destination clocks. Call this tool under the menu of Analysis in Global Timing Debug.

→ *Choose Timing - Debug Timing - Analysis - Clock Matrix Viewer.*

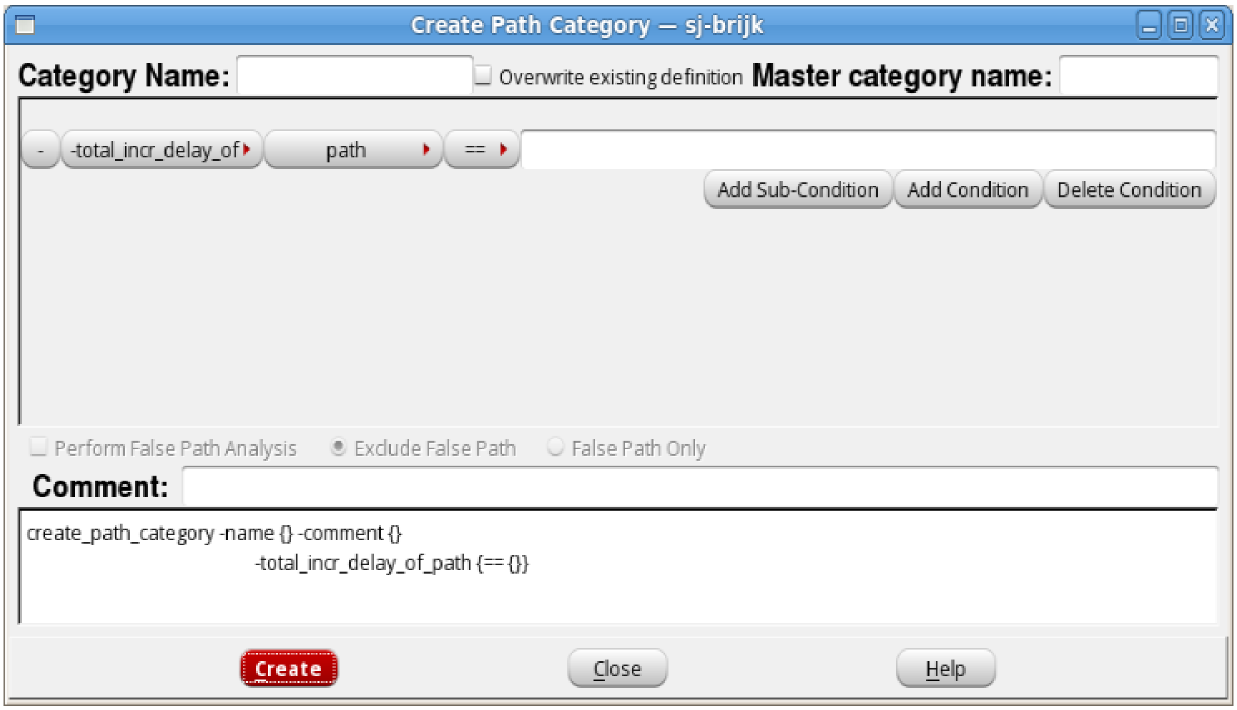


Note: MCL(launch,capture) is Max clock latency for launch or capture clock path.

Create Path Category

Use the Create Path Category form to define the categories as per your design requirements. You can use the Timing Path Analyzer form to analyze the critical paths and identify possible problems with the design. You can then use the Create Path Category form to define a category or categories to group all paths with same problem.

→ Choose *Timing - Debug Timing - Category - Create.*



Create Path Category Fields and Options

Category Name	Specify the name of the category. **Note:** The values that you specify in this form are reflected as Tcl command in the display area at the bottom of the form.
Overwrite existing definition	
	Overwrites any predefined category with the same name in your category list.

<table>
<tr><td>Definition</td><td colspan="2">Define category using the pull down menu options beginning with -from and inst.
Choose from the following options:</td></tr>
<tr><td></td><td>-from
-not_from
-through
-not_through
-to
-not_to</td><td></td></tr>
<tr><td></td><td></td><td>Choose from the following options:
inst
pin
cell
clock
port
For example, you can choose -from cell <code>XYZ</code> .</td></tr>
<tr><td></td><td colspan="2">-slack
-uncertainty
-skew
-launch_latency
-capture_latency</td></tr>
</table>

		Choose from the following options: • *==* • *!=* • *>* • *<* • *>=* • *<=* For example, you can choose *-uncertainty >=* `0.4` .
	-check_type	Choose from the following options: • *Setup Check* • *Hold Check* • *Clock Gating Setup Check* • *Library Clock Gating Setup Check* • *Clock Gating Hold Check* • *Library Clock Gating Hold Check* • *External Delay Assertion* • *Latch Borrowed Time Check* • *PulseWidth Check* • *ClockPeriod Check* • *Recovery Check* • *Removal Check*

	-number_of	Specify number of instances with required operator. Optionally you can choose from the following options: • *of_name* • *not_of_name* • *of_celltype* • *not_of_celltype* For example, you can specify *-number_of insts of_name* `INST1` *!=* `4`.
	-delay_of	Specify the value for one of the following options: • *any_inst* • *any_net* • *every_inst* • *every_net* For instances, you can optionally choose from the following options: • *of_name* • *not_of_name* • *of_celltype* • *not_of_celltype* For example, you can specify *-delay_of any_inst of_name* `INST1` = `0.5`. For nets, you can optionally choose from the following option: • *of_name* • *not_of_name* For example, you can specify *-delay_of any_net of_name* `clk` = `0.1`.

	-total_delay_of	Specify the value for one of the following options: path insts nets For instances, you can optionally choose from the following options: • *of_name* • *not_of_name* • *of_celltype* • *not_of_celltype* For example, you can specify *- total_delay_of inst of_name* `INST1` = `0.5`. For nets, you can optionally choose from the following options: • *of_name* • *not_of_name* For example, you can specify *- total_delay_of net of_name* `clk` = `0.1`.
	-view	Specify the name of the view. The paths related to the specified view are grouped under this category.
	-file	Specify the name of the file that contains definitions for creating categories.

	-sdc	Specify the name of the SDC constraint. The paths related to the specified SDC constraint are grouped under this category. You can create a constraint category directly from an SDC constraint by right-clicking on the constraint in the Timing Path Analyzer - Path SDC form. The Create Path Category form displays, showing the line number (from the SDC file) and the name of the constraint.
Master Category name	Creates the category as a nested category for the existing category that you specify in this field. For more information on nested categories, see Creating Sub-Categories in Debugging Timing Results in the *Innovus User Guide*. If you do not specify any value this field, the category is not created as a sub-category.	
Add Sub-Condition	Adds a row for definition an OR sub-condition for the named category.	
Add Condition	Adds a row for definition an AND sub-condition for the named category.	
Delete Condition	Deletes defined condition.	
Comment	Allows you to enter any comment to associate with the condition.	

Related Text Commands

The following text command provides equivalent or additional functionality:

`create_path_category`

For more information, see "Timing Debug Commands" in the *Text Command Reference* document.

Timing Path Analyzer

Use the Timing Path Analyzer form to analyze a single path in detail. The various elements in the form help in identifying possible issues related to a particular path.

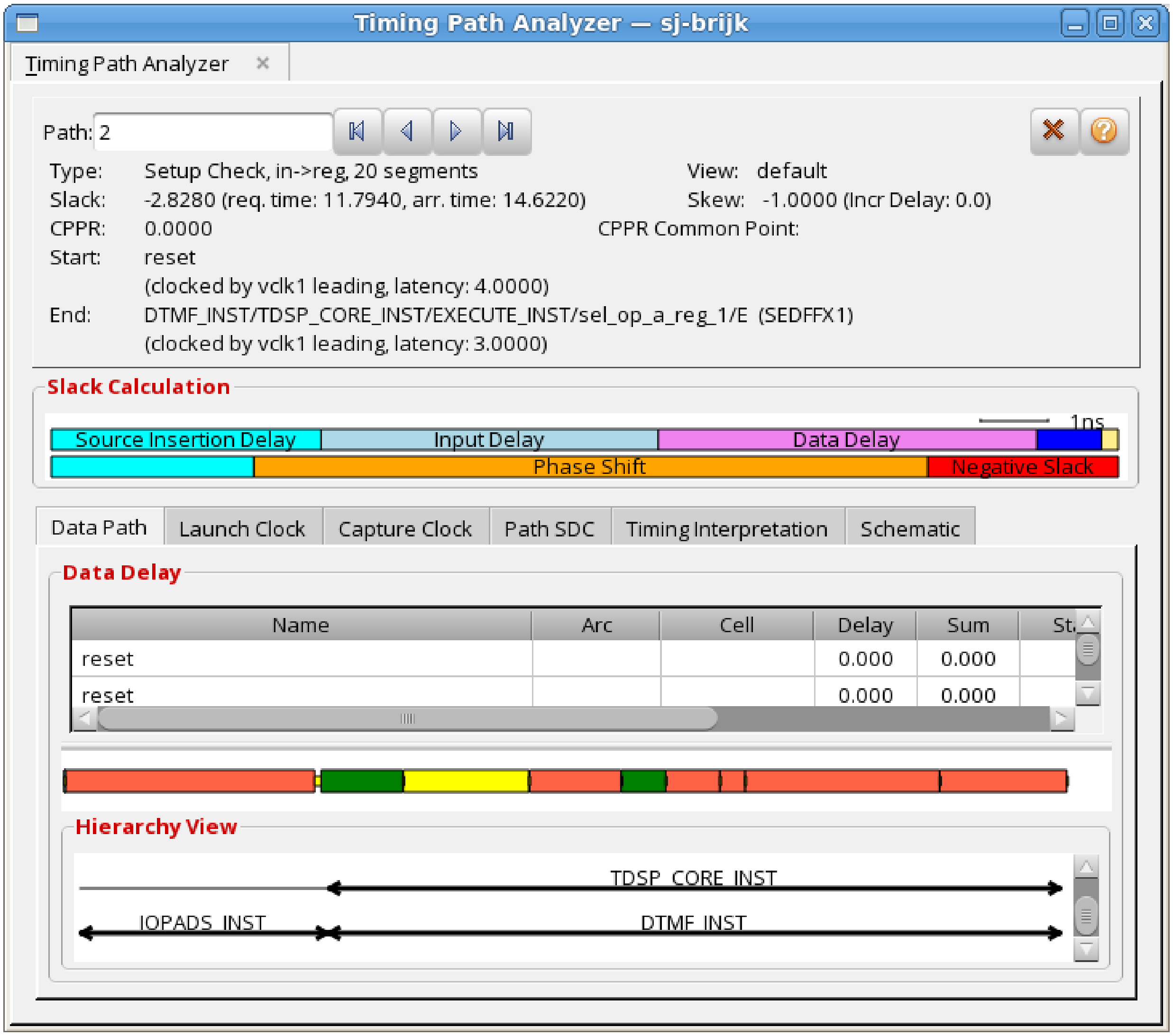
The Timing Path Analyzer form has the following five tabs:

- Timing Path Analyzer - Data Path
- Timing Path Analyzer - Launch Clock
- Timing Path Analyzer - Capture Clock
- Timing Path Analyzer - Path SDC
- Timing Path Analyzer - Timing Interpretation
- Edit Timing Interpretation
- Timing Path Analyzer - Schematics

Timing Path Analyzer - Data Path

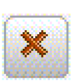
Use the Timing Path Analyzer - Data Path form to identify issues related to a path using slack calculation bars, timing bar, and hierarchy view.

1. Choose *Timing - Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.



Timing Path Analyzer - Data Path Fields and Options

Path	Specifies the number of path as listed in the Timing Debug window.
Type	Displays the type of selected path.
Start	Displays the starting point of the path.
End	Displays the ending point of the path.
Skew	Displays the skew of the path.

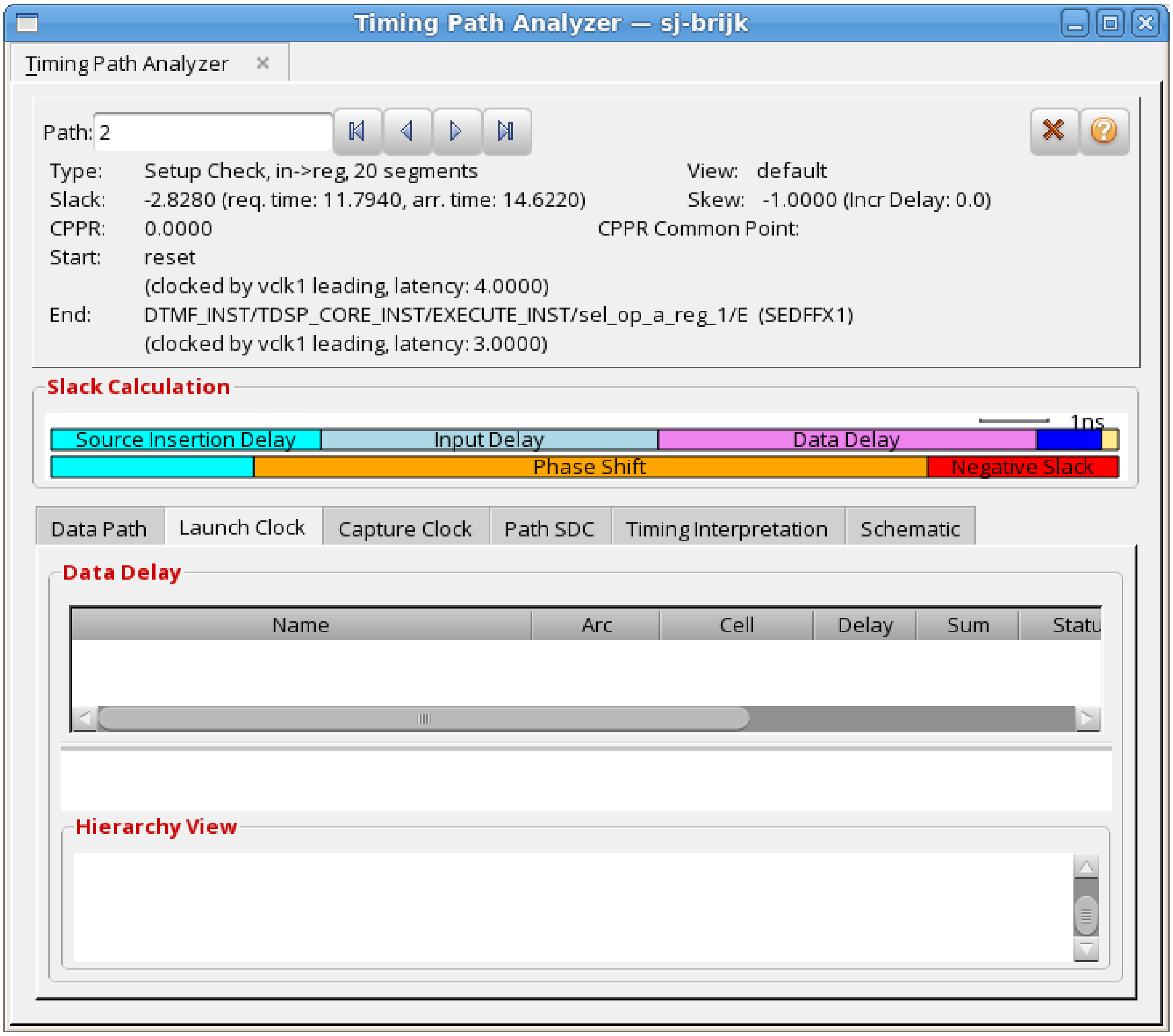
Slack	Displays the slack of the path. The path has a timescale on top of slack calculation bar. The time scale stands for the timing unit.
Slack Calculation	Displays path arrival time and required time calculations in color bars. The top bar displays the arrival time and the bottom bar displays the required time calculation. For example, arrival time can be represented as consisting of data delay (In pink), Setup time (in blue), and uncertainty (in yellow). You can inspect various aspects of calculation to identify possible problem(s) associated with a path. You can move you cursor over the color bars to display the values associated with each bar element. Use this feature to identify issues related to clock skew, latency balancing or large clock uncertainties.
Data Delay	Displays the details of the selected path in the violation reports. You can click on a single element to display it in the design display area. You can select each element consecutively to trace the entire path in the design display area.
Timing Bar	Displays the instance and net delays. The size of the bar indicates the delay associated with that element. Moving the cursor on these elements displays the details of instances or nets. The instance delays are represented in red and the net delays are represented in yellow color. Use this feature to identify issues related to large instance or net delays, repeater chains, paths with large number of buffers, and large macro delays.
Hierarchy View	Displays a path's traversal of logical hierarchy on a time-axis. This is useful for identifying issues related to inter-partition paths or paths that go through a partition.
	Closes the form.

Timing Path Analyzer - Launch Clock

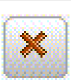
Use the Timing Path Analyzer - Launch Clock form to identify issues related to a path using the launch clock details. The Launch Clock form displays the details of a complete launch clock path.

1. Choose *Timing - Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.

3. Choose *Launch Clock* tab in the Timing Path Analyzer form.



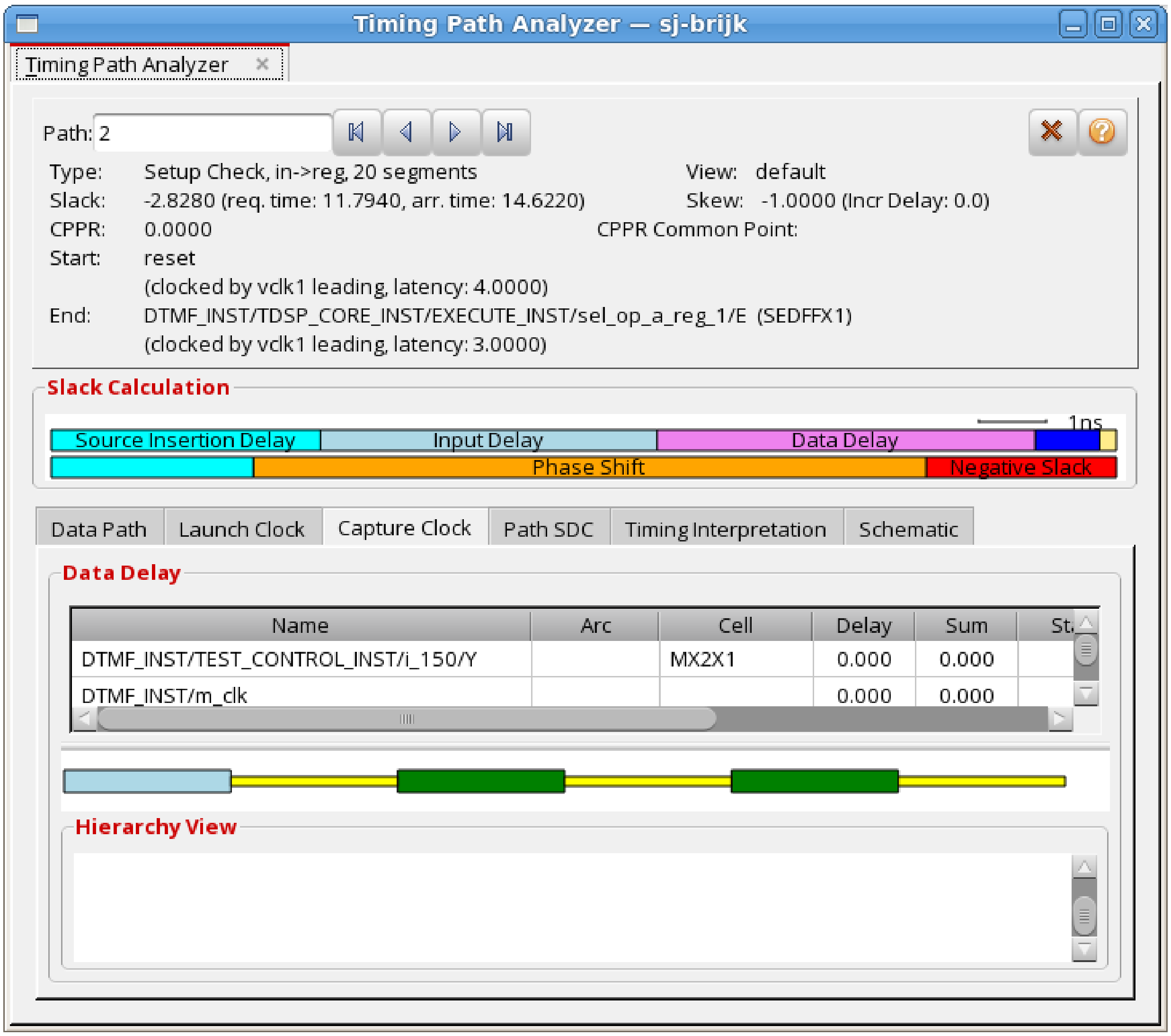
Timing Path Analyzer - Launch Clock Fields and Options

Data Delay	Displays the details of the launch clock of the selected path. You can click on a single item in the table to highlight the clock in the design display area. The *Timing Bar* and *Hierarchy View* display the characteristics of the launch clock path.
	Closes the form.

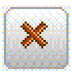
Timing Path Analyzer - Capture Clock

Use the Timing Path Analyzer - Capture Clock form to identify issues related to a path using the capture clock details. The Capture Clock form displays the details of a complete capture clock path.

1. Choose *Timing - Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.
3. Choose *Capture Clock* tab in the Timing Path Analyzer form.



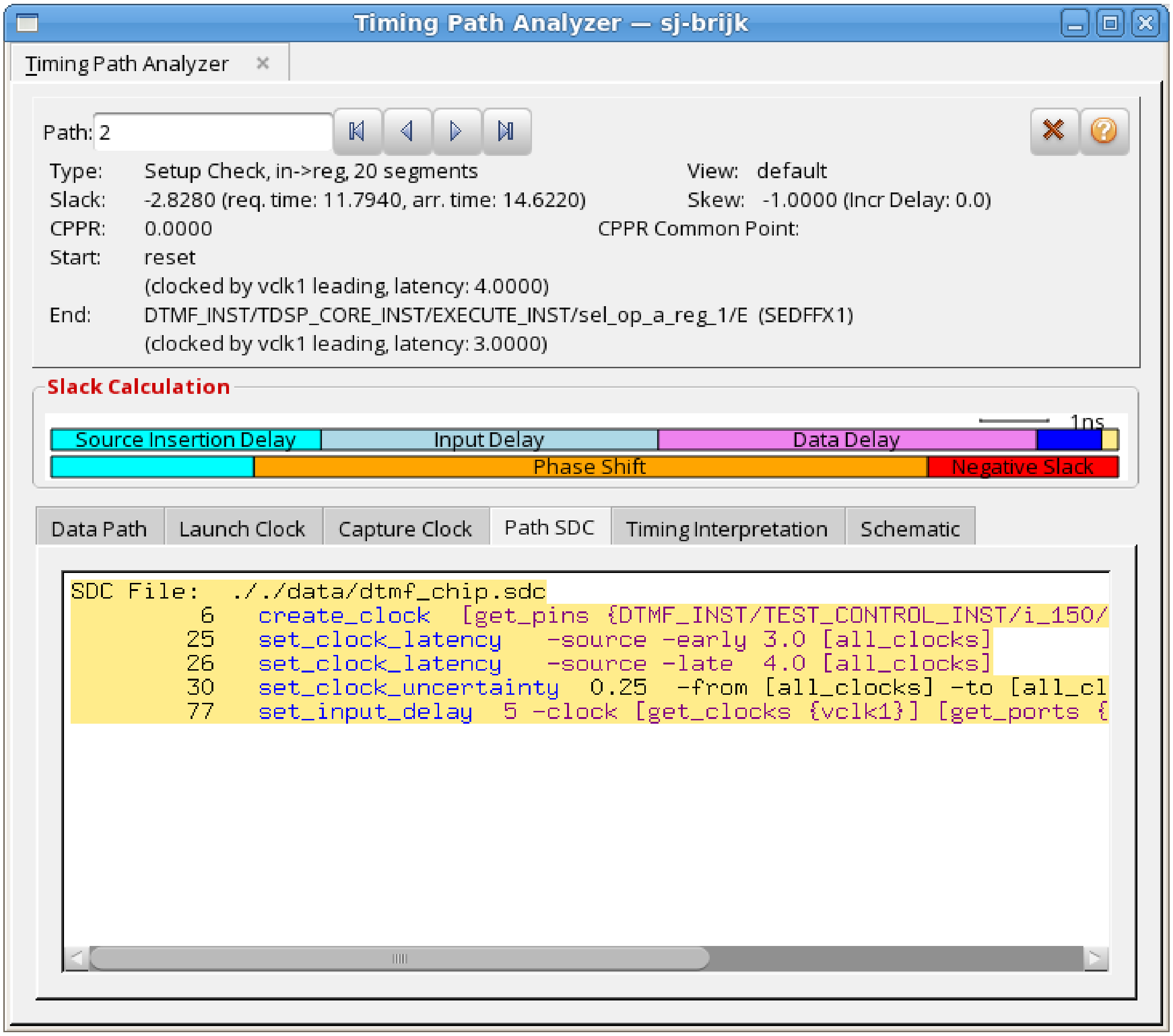
Timing Path Analyzer - Capture Clock Fields and Options

Data Delay	Displays the details of the capture clock of the selected path. You can click on a single item in the table to highlight the clock in the design display area. The *Timing Bar* and *Hierarchy View* display the characteristics of the capture clock path.
	Closes the form.

Timing Path Analyzer - Path SDC

Use the Timing Path Analyzer - Path SDC form to identify issues related to the SDC constraints associated with the selected path.

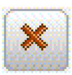
1. Choose *Timing - Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.
3. Choose *Path SDC* tab in the Timing Path Analyzer form.


Timing Path Analyzer — sj-brijk
Timing Path Analyzer
Path: 2
Type: Setup Check, in->reg, 20 segments
View: default
Slack: -2.8280 (req. time: 11.7940, arr. time: 14.6220)
Skew: -1.0000 (Incr Delay: 0.0)
CPPR: 0.0000
CPPR Common Point:
Start: reset
(clocked by vclk1 leading, latency: 4.0000)
End: DTMF_INST/TDSP_CORE_INST/EXECUTE_INST/sel_op_a_reg_1/E (SEDFFX1)
(clocked by vclk1 leading, latency: 3.0000)
Slack Calculation
1ns
Source Insertion Delay
Input Delay
Data Delay
Phase Shift
Negative Slack
Data Path
Launch Clock
Capture Clock
Path SDC
Timing Interpretation
Schematic
SDC File: ././data/dtmf_chip.sdc
6 create_clock [get_pins {DTMF_INST/TEST_CONTROL_INST/i_150/
25 set_clock_latency -source -early 3.0 [all_clocks]
26 set_clock_latency -source -late 4.0 [all_clocks]
30 set_clock_uncertainty 0.25 -from [all_clocks] -to [all_cl
77 set_input_delay 5 -clock [get_clocks {vclk1}] [get_ports {

Timing Path Analyzer - Path SDC Fields and Options

<table>
<tr><td>SDC File</td><td>Displays the list of SDC constraints associated with the selected path. The list contains the name of the SDC file, the line number that indicates the position of the constraint in the SDC file, and the constraint definition.

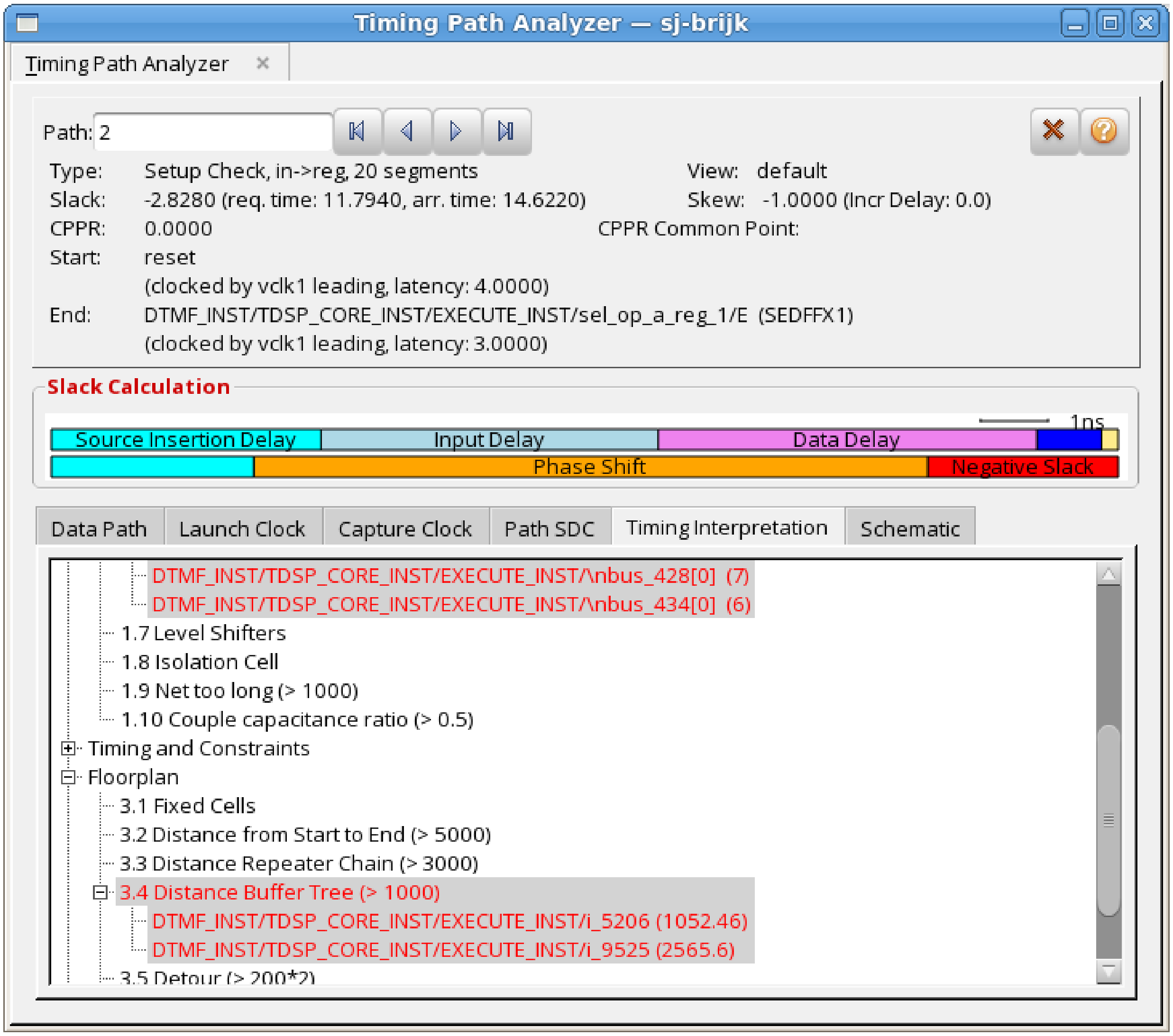
Use this from to identify issues related to the constraint definition for a path.

<table><tr><td></td><td>Tip</td><td>You can create a path category directly from SDC constraints in the Path SDC form. When you right-click on a constraint and select Create Path Category, the <u>Create Path Category</u> form displays, showing the line number (from the SDC file) and the name of the constraint.</td></tr></table>
</td></tr>
<tr><td></td><td>Closes the form.</td></tr>
</table>

Timing Path Analyzer - Timing Interpretation

Use the Timing Path Analyzer - Timing Interpretation form to identify the possible sources of timing problems associated with a selected path. Potential problems are highlighted in red.

1. Choose *Timing - Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.
3. Choose the *Timing Interpretation* tab in the Timing Path Analyzer form.



Timing Path Analyzer - Timing Interpretation Fields and Options

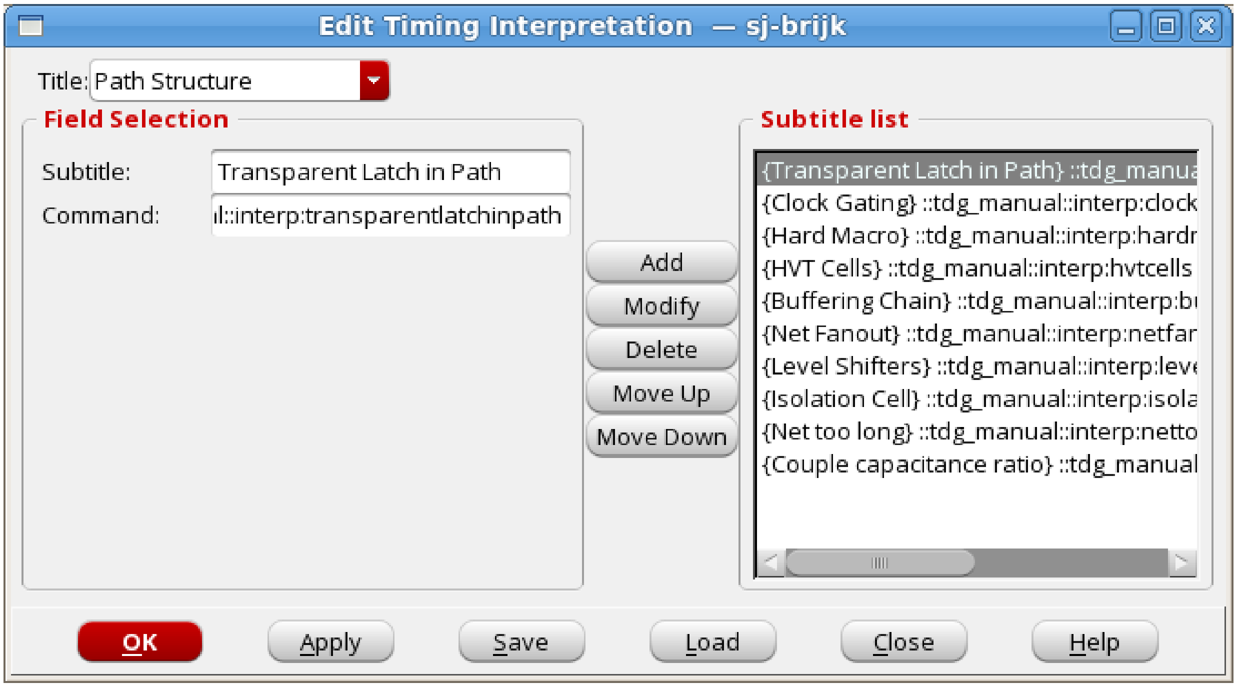
Path Structure	Shows the presence of structures that could cause timing issues in the path: • *Transparent Latch in Path* • *Clock Gating* • *Hard Macros* • *HVT Cells* • *Buffering Chain* • *Net Fanout* • *Level Shifters* • *Isolation Cell* • *Net too long (>1000)* • *Couple capacitance ratio (>0.5)*
Timing and Constraints	
	Shows values that exceed preset limits for timing and constraints: • *Large Skew* • *Total SI Delay* • *SI Delay* • *External Delay* • *Divider in Clock Path*

Floorplan	Shows the presence of the following floorplan elements that could be source of problems in the timing path: • *Fixed Cells* • *Multiple Power Domains* Also shows violations for preset limits for the distances: • *Distance from Start to End* • *Distance Repeater* • *Distance Buffer Tree* • *Detour*
DRVs	Shows max_tran, max_cap, and max_fanout values exceeding the preset limits: • *Max Transition* • *Max Capacitance* • *Max Fanout* • *Slack Transition/Capacitance/Fanout*

Edit Timing Interpretation

Use the Edit Timing Interpretation form to change the type of information displayed on the Timing Interpretation table of the Timing Path Analyzer.

1. To open the Edit Timing Interpretation form, open the Timing Path Analyzer form.
2. Click on the Timing Interpretation tab.
3. Right-click on any element in the table and select *Edit Timing Interpretation*.



Timing Path Analyzer - Edit Timing Interpretation Fields and Options

Title	Specifies the title of the path element: • Path Structure • Timing and Constraints • Floorplan • DRV: Work after DRV

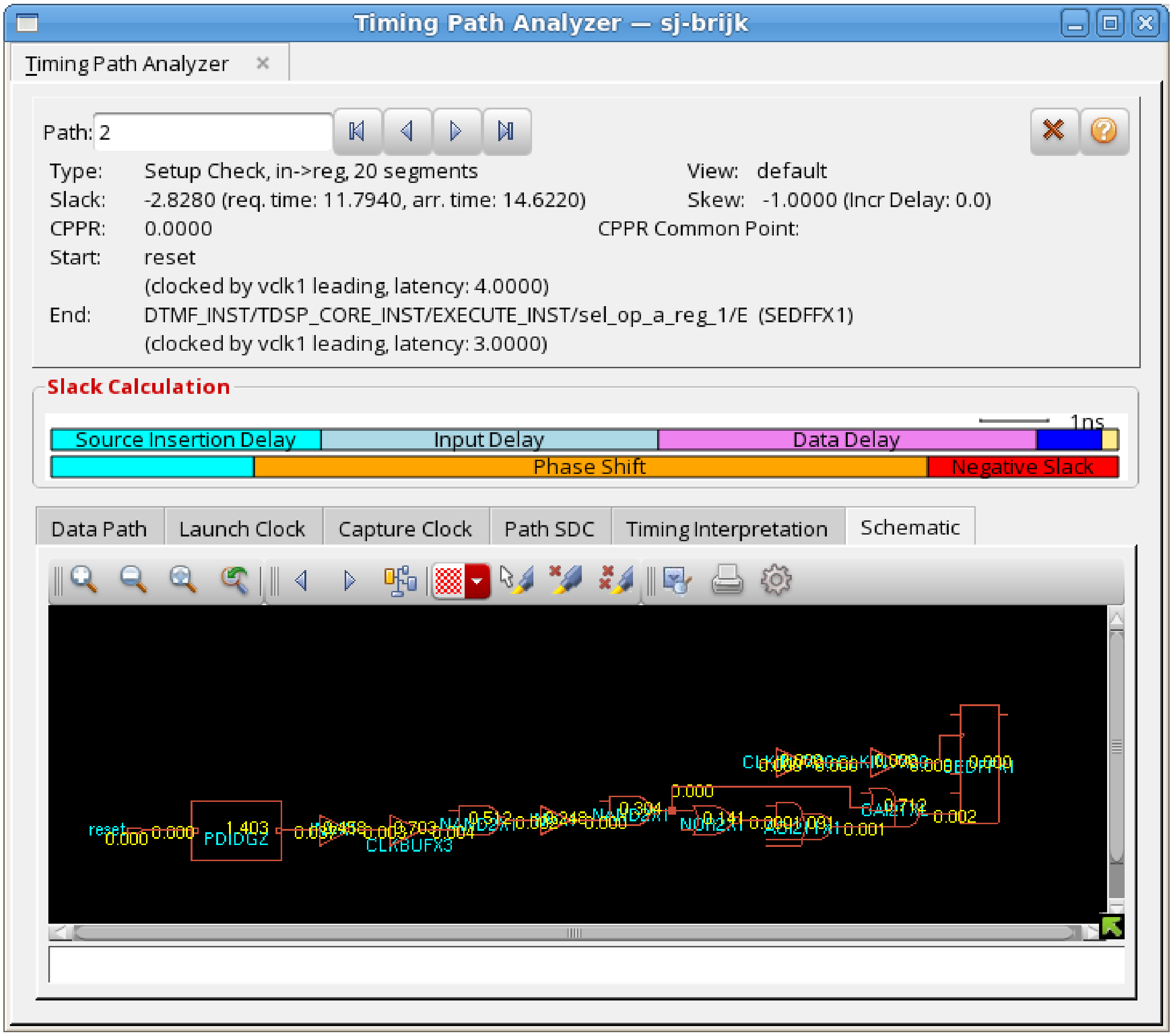
Subtitle	Specifies the name of the subtitle to modify. For Path Structure: • Transparent Latch in Path • Clock Gating • Hard Macro • HVT Cells • Buffering Chain • Net Fanout • Level Shifters For Timing and Constraints: • Large Skew • Divider in Clock Path • Total SI Delay • SI Delay • External Delay For Floorplan: • Fixed Cells • Distance from Start to End • Distance Repeater Chain • Distance Buffer Tree • Detour • Multi Power Domains For DRV: Word after DRV Analysis • Max Transition • Max Capacitance • Max Fanout
Command	Specifies a procedure to create the subtitle.

Condition	Specifies a condition value.
Subtitle list	Displays a subtitle you selected, or lets you specify the name of the subtitle you would like to add.
Add	Adds the subtitle to the Subtitle list an subtitle that you added or changed in the Field Selection pane.
Modify	Modifies the selected subtitle.
Delete	Deletes the subtitle.
Move Up	Moves the subtitle up the list of subtitles in the Timing Interpretation table.
Move Down	Moves the subtitle down the list of subtitles in the Timing Interpretation table.

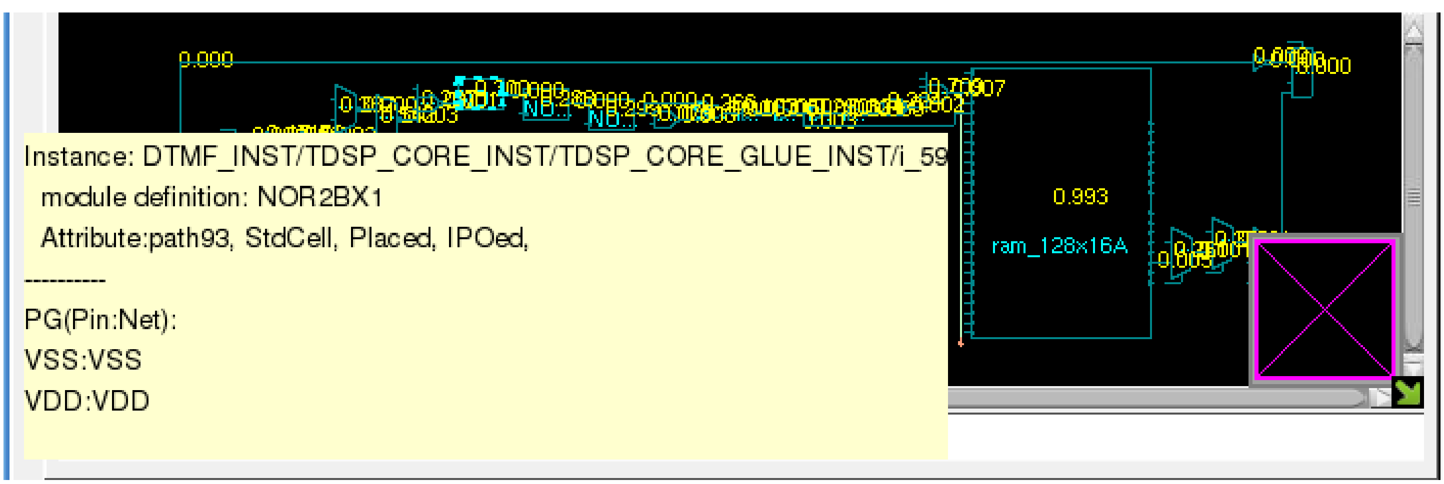
Timing Path Analyzer - Schematics

Use the Timing Path Analyzer - Schematics form to display the schematic view of the selected path.

1. Choose *Timing - Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.
3. Choose *Schematics* tab in the Timing Path Analyzer form.



Note: To see timing information (slew and load) of instance output pin move the mouse on the instance's output pin on the Schematic viewer of critical path.



Timing Path Analyzer - Schematics Fields and Options

For more information about fields and options, see "Schematics" in the Tools Menu chapter.

Create Black Box/Blob Model

Use the Black Box/Blob What-if Timing Analysis form to view details of blackboxes and blackblobs, and perform what-if analysis of the blackboxes or blackblobs.

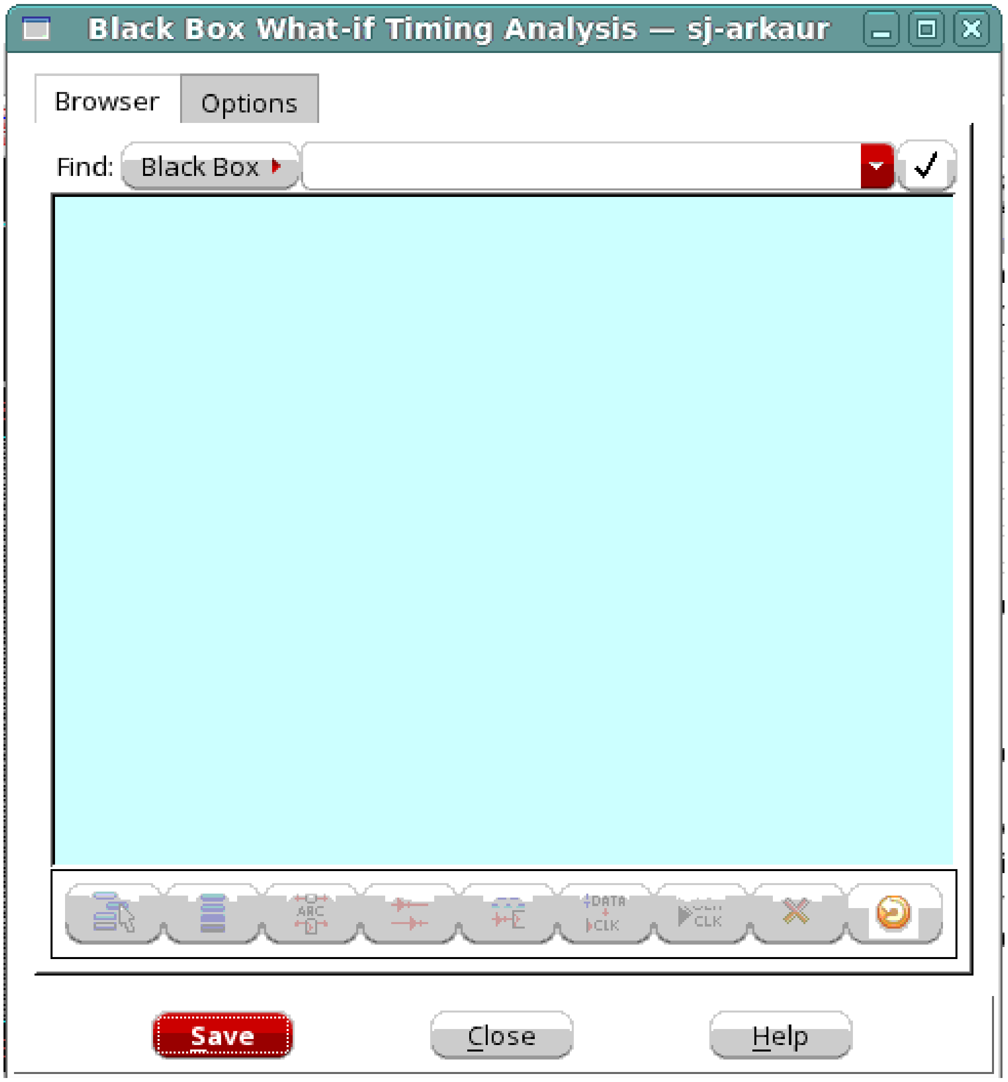
The Black Box What-if Timing Analysis form contains the following two pages:

- Black Box-Blob What-If Timing Analysis - Browser
- Black Box What-If Timing Analysis - Options

Black Box-Blob What-If Timing Analysis - Browser

Use the *Browser* page of the Black Box What-If Timing Analysis form to navigate through the blackbox or pin specifications. The *Browser* page makes it easier to interactively display and set various values related to blackboxes.

The browser displays the blackboxes and blackblobs used in the design. The input and output ports of the blackbox or blackblob are grouped under input and output of a block. The browser also displays the timing arcs for each pin and the What-if information. The clock pins are displayed in the color blue.
→ Choose *Timing - Create Black Box/Blob Model* and click on the *Browser* tab.


Black Box What-if Timing Analysis — sj-arkaur
Browser
Options
Find:
Black Box
Save
Close
Help

Black Box/Blob What-If Timing Analysis Fields and Options

Find	Allows you to view timing information for a specific blackbox, blackblob or pin. The text field supports the use of wildcard entries. You can use an asterisk (*) with regular characters to list the matching object names.
	*Show selected Black Boxes/Blobs*--Displays the selected blackboxes and/or blackblobs in the Black Box/Blob What-if Timing Analysis window.
	*Show all Black Boxes/Blobs*--Displays all blackboxes or blackblobs in the Black Box/Blob What-if Timing Analysis window.
	*Set/Create timing arcs*--Opens the Create Timing Arc form. This button is activated when you select a pin name. For more information, see "Create Timing Arcs" . If the timing arc is already defined for a pin, clicking on the *Set/ Create timing arcs* widget displays the Set Timing Arc form. For detailed information on the Set Timing Arc form, see "Set Timing Arc" .
	*Set output driver*--Opens the Set Output Driver form. This button is activated when you select an output pin. For more information, see "Set Output Driver" .
	*Set clock latency*--Opens the Set Clock Latency form. This button is activated when you select a clock pin. For more information, see "Set Clock Latency" .
	*Set black box/blob clock port*--Opens the Set Black Box/Blob Clock Port form. This button is activated when you select an input pin. For more information, see "Set Black Box Clock Port" .
	*Generate internal clock*--Creates an internal pin and defines a generated clock on the pin. For more information, see "Create Internal Generated Clock".
	*Delete timing arcs*--Deletes selected timing arcs.
	*Refresh browser*--Refreshes the Browser display.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `createWhatIfInternalGeneratedClock`

- [deleteWhatIfTimingAssertions]
- [saveWhatIfTimingAssertions]
- [setWhatIfClockLatency]
- [setWhatIfDriveType]

For more information, see "What-If Timing Commands" in the *Innovus Text Command Reference*.

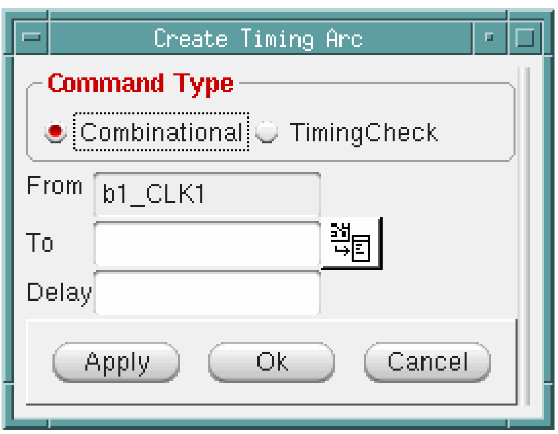
Related Topics

For information on the following topic, see "What-If Timing Analysis" in the *Innovus User Guide*.

- Performing What-If Timing Analysis

Create Timing Arcs

Use the Create Timing Arc form to create timing arcs for the pins.
→ Choose *Timing - Create Black Box/Blob Model* and then click on the *Set/Create timing arcs* widget on the Black Box Timing Analysis form.



Create Timing Arc Fields and Options

Combinational	Sets the delay for purely combinatorial paths from input ports to the output ports. In the intrinsic timing model mode, the delay corresponds to the delay from the input port to the input of the driver. In the normalized timing model mode, the delay corresponds to the delay from the input port to the output port including the driver delay. If you do not specify the drive type on the output port, a constant timing table is created. In a constant timing table, delay is constant. It does not vary with respect to input slew and output capacitance. When you select this option, the Create Timing Arc form is expanded to display options for specifying the delay value.
Timing Check	Sets the delay from the clock input port to the data input port. The delay value contains the clock latency. To create a new timing check arc which does not already exist in the timing model, the clock port that you specify in this command must be already referenced as a clock pin in the timing model. When you select this option, the Create Timing Arc form is expanded to display options for specifying the delay value.
From	Specify the name of the clock input port. If you do not specify this parameter, the delay is set for all input and bidirectional clock ports.
To	Specify the name of the data input port.
Delay	Specify the delay value.
Clock Edge	Select the *Clock Edge* as *Rising* or *Falling*. These options specify the transition on the clock input relevant to the sequential delay arc definition.
Time Analysis	Select the *Timing Analysis* as *Setup* or *Hold*. These options specify the setup or hold time for the timing check.

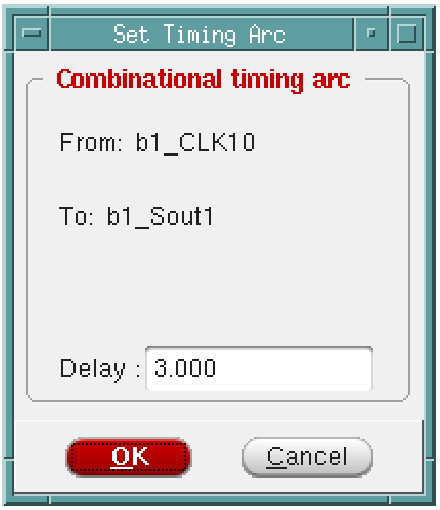
Related Topics

For information on the following topic, see "What-If Timing Analysis" in the *Innovus User Guide*.

- What-If Timing Analysis

Set Timing Arc

If the timing arc is already defined for a pin, use the Set Timing Arc form (Black Box What-If Timing Analysis - Browser - Set timing arcs) to change the delay value.
➝ Choose *Timing - Create Black Box/Blob Model* and then click on the *Set/Create timing arcs* widget on the Black Box Timing Analysis form.



Set Timing Arc Fields and Options

From	Displays the name of the clock input port.
To	Displays the name of the data input port.
Delay	Specify the delay value.

Related Topics

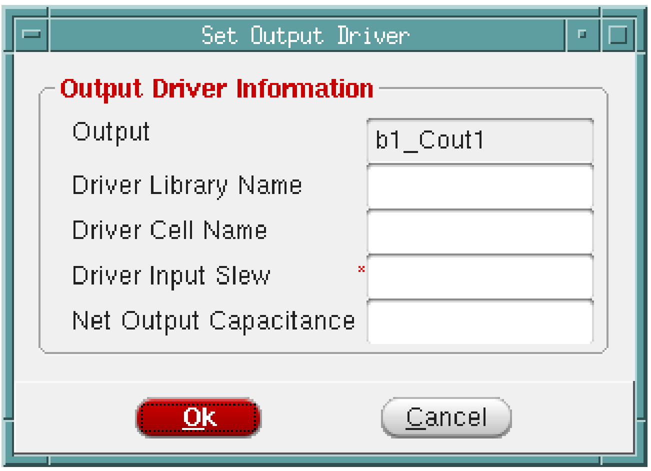
For information on the following topic, see "What-If Timing Analysis" in the *Innovus User Guide*.

- Blackbox What-If Timing Analysis

Set Output Driver

Use the Set Output Driver form to specify the output and bidirectional ports that have the specified type of cell within the blackbox as drivers on the interface nets. You cannot specify two different drivers for two timing arcs ending at the same output port. Innovus stores the drive type specification, and uses it to create a timing arc after you specify the delay.

→ Choose *Timing - Create Black Box/Blob Model* and then click on the *Set Output Driver* widget on the Black Box Timing Analysis form.



Set Output Driver Fields and Options

Output	Displays the name of the output port.
Driver Library Name	Specifies the name of the timing library.
Driver Cell Name	Specifies the name of the cell. If there are two cells with the same name, the software uses the first one found. The software considers only buffers and inverters.
Driver Input Slew	Specifies the slew at the input of the driver cell. If you specify the slew value, the software creates a one-dimensional timing table depending on the output capacitance. If you do not specify the slew value, the software creates a two-dimensional timing table with input slew and output capacitance values. In this case, the software assumes that there is no slew variation between the blackbox input port and the driver input pin. You must use this parameter in the normalized timing model mode.
Net Output Capacitance	Specifies the value of the output capacitance on the port.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setWhatIfDriveType`

For more information, see "Blackbox Timing Commands" in the *Innovus Text Command Reference*.

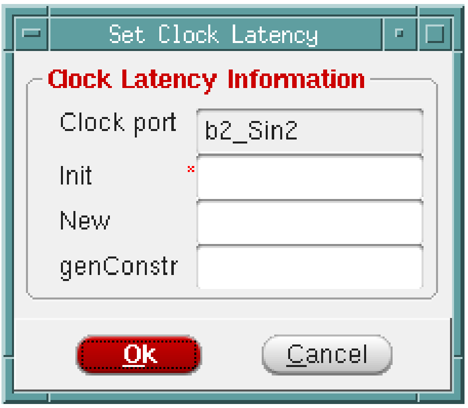
Related Topics

For information on the following topic, see "What-If Timing Analysis" in the *Innovus User Guide*.

- Blackbox What-If Timing Analysis

Set Clock Latency

Use the Set Clock Latency form to specify the clock insertion delay from a clock input port to register clock input pins within a blackbox.
→ Choose *Timing - Create Black Box/Blob Model* and then click on the *Set Clock Latency* widget on the Black Box Timing Analysis form.



Set Clock Latency Fields and Options

Init	Specifies the current clock insertion delay value. This value indicates the clock insertion delay used when the software generates the original timing model. This value is used for timing checks or sequential timing arcs. You must specify this value before modifying a timing check or a sequential timing arc. If you modify at least one timing arc, you cannot directly change the clock latency value. You must first delete the timing arc specifications of the blackboxes using the `deleteWhatIfTimingAssertions` command.
New	Specifies the new clock latency value. This value modifies the clock insertion delay. Innovus adds the difference between the current and new clock latency value to all timing arcs starting from the specified clock port. Therefore all timing arcs starting from the specified clock port, including the timing arcs that were not modified using the blackbox timing commands, are modified.
genConstr	Specifies the latency to consider in the blackbox timing constraints generation. By default, the value is automatically set to the current clock insertion delay. If you do not modify the latency value, the generated SDC constraints reflect the timing analysis done at the top level. If you set a latency value other than current clock insertion delay, the timing analysis is not impacted.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setwhatIfClockLatency`

For more information, see "Blackbox Timing Commands" in the *Innovus Text Command Reference*.

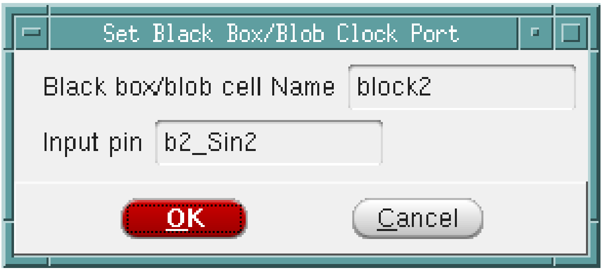
Related Topics

For information on the following topic, see "What-If Timing Analysis" in the *Innovus User Guide*.

- Blackbox What-If Timing Analysis

Set Black Box Clock Port

Use the Set Black Box Clock Port form to define a port as a clock port. The form displays the port information.
→ Choose *Timing - Create Black Box/Blob Model* and then click on the *Set black box clock port* widget on the Black Box Timing Analysis form.



Set Black Box Clock Port Fields and Options

Black box cell Name	Displays the name of the blackbox.
Input pin	Displays the name of the input pin that will get set as the clock port.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setWhatIfClockPort`

For more information, see "Blackbox Timing Commands" in the *Innovus Text Command Reference*.

Related Topics

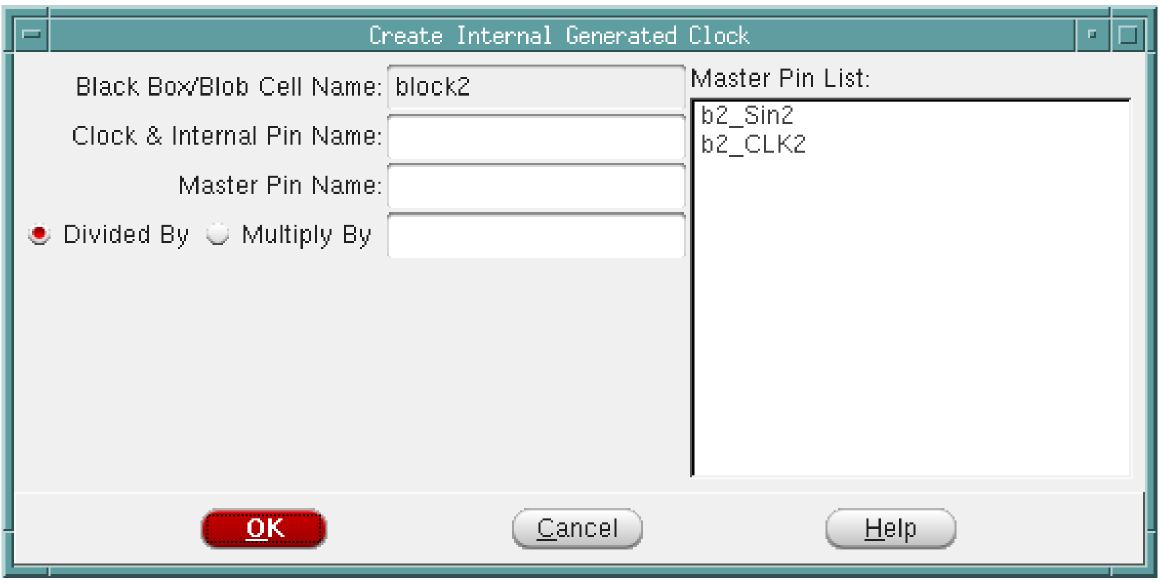
For information on the following topic, see "What-If Timing Analysis" in the *Innovus User Guide*.

- What-If Timing Analysis

Create Internal Generated Clock

Use the Create Internal Generated Clock form to create a pin inside a blackbox or a blackblob and to define a generated clock on the pin.

1. Choose *Timing - Create Black Box/Blob Model.*
2. In the Browser, select the blackbox or the blackblob inside which you want to create the internal pin, and then click on the *Generate Internal Clock* widget. The Create Internal Generated Clock form appears.



Create Internal Generated Clock Fields and Options

Black Box/Blob Cell Name	Displays the name of the blackbox or blackblob.
Clock & Internal Pin Name	Specifies the name of the internal pin that will get created inside the blackbox or the blackblob. The same name is used for the generated clock that will be defined on the pin.
Master Pin Name	Specifies the source from which the derived clock is generated. **Note:** The source must be an existing clock port and a clock should be available on this port. You can select a source from the list of existing clock sources displayed in *Master Pin List.*
Divided By	Specifies the frequency division factor. The generated clock period is equal to the master clock period multiplied by this parameter. For example, if the value of this parameter is `2`, the generated clock period is two times the master clock period.
Multiply By	Specifies the frequency multiplication factor. The generated clock period is equal to the master clock period divided by this parameter. For example, if the value of this parameter is `2`, the generated clock period is half the master clock period.
Master Pin List	Displays the available clock sources.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `createWhatIfInternalGeneratedClock`

For more information, see "Blackbox Timing Commands" in the *Innovus Text Command Reference*.

Related Topics

For information on the following topic, see "What-If Timing Analysis" in the *Innovus User Guide*.

- What-If Timing Analysis

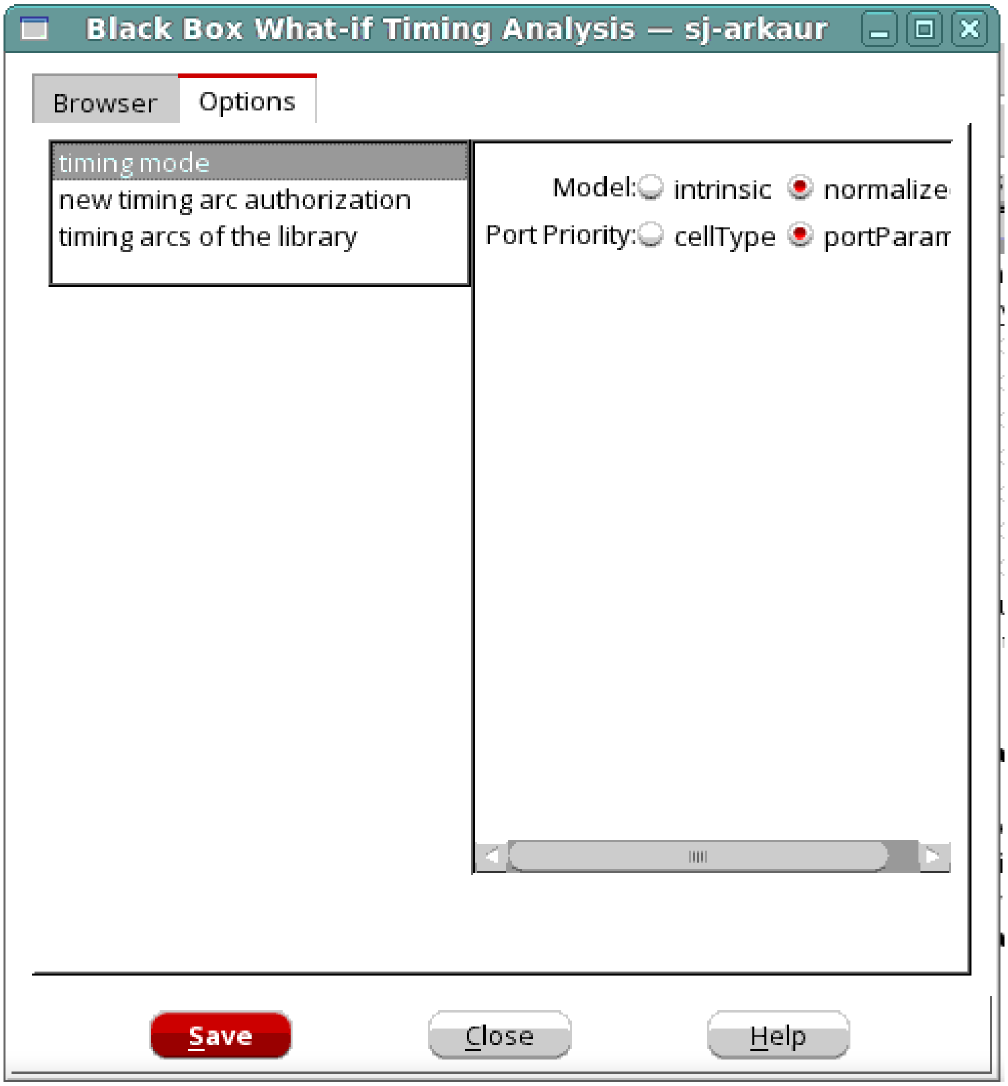
Black Box What-If Timing Analysis - Options

The *Options* page of the Black Box What-If Timing Analysis form enables you to specify timing mode, set new timing arc, and enable the set timing arcs option. The *Options* page contains the following subpages:

- Black Box What-If Timing Analysis - Options - timing mode
- Black Box What-If Timing Analysis - Options - new timing arc authorization
- Black Box What-If Timing Analysis - Options - timing arcs of the library

Black Box What-If Timing Analysis - Options - timing mode

Use the *timing mode* page of the Black Box What-If Timing Analysis form to specify the type of timing model for blackbox analysis.
→ Click on the *Options* page of the Black Box What-if Timing Analysis form.


Black Box What-if Timing Analysis — sj-arkaur
Browser
Options
timing mode
new timing arc authorization
timing arcs of the library
Model:
intrinsic
normalize
Port Priority:
cellType
portParam
Save
Close
Help

Black Box What-If Timing Analysis Fields and Options

Model	Select the timing model (*intrinsic* or *normalized*).
intrinsic	Specifies the intrinsic timing model mode.
normalized	Specifies the normalized timing model mode. This is the default mode.
Port Priority	On output and input ports, parameters such as capacitance value, maximum capacitance values, maximum transition value, or the maximum fanout value can come from the driver (`setWhatIfDriveType` command or `setWhatIfLoadType` command) or they can be set through the `setWhatIfPortParameters` command. Use the Port Priority option to specify which of these values take precedence in case of a conflict. Important: *The value of the portPriority parameter is frozen once a what-if timing arc has been defined. This avoids inconsistencies between the timing analysis files and the files that you can generate (such as whatif assertions, timing model, or SDC) if you change the port priority subsequently.*
cellType	Specifies that the parameter values set through the `setWhatIfDriveType` command or `setWhatIfLoadType` command take precedence.
portParam	Specifies that the parameter values set through the `setWhatIfPortParameters` command take precedence.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setWhatIfTimingMode`

For more information, see "Blackbox Timing Commands" in the *Innovus Text Command Reference*.

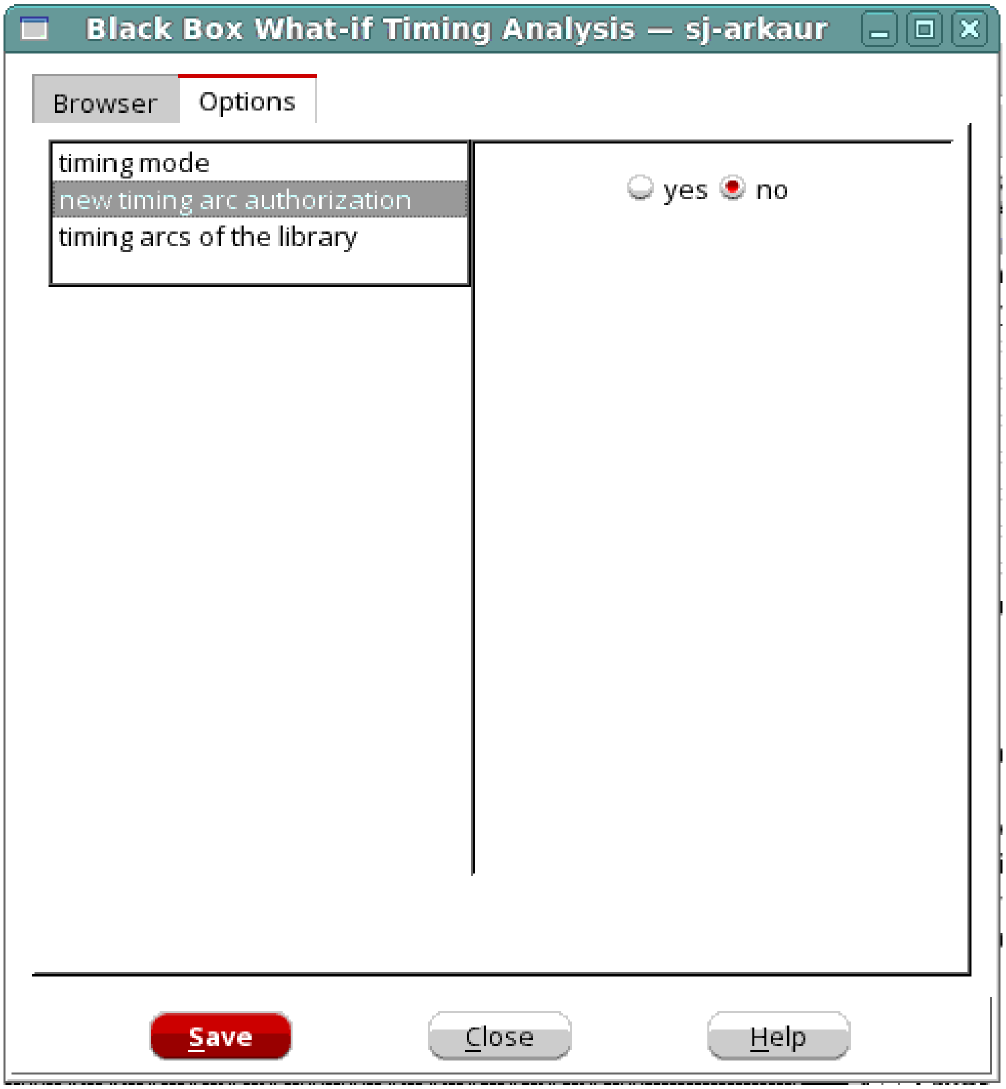
Related Topics

For information on the following topic, see "What-If Timing Analysis" in the *Innovus User Guide*.

- Performing What-If Timing Analysis

Black Box What-If Timing Analysis - Options - new timing arc authorization

Use the *new timing arc authorization* page of the Black Box What-If Timing Analysis form to enable creation of new timing arcs.
→ From the *Options* page, select the *new timing arc authorization* category.



Black Box What-If Timing Analysis - Options - new timing arc authorization Fields and Options

yes	Enables creation of new timing arcs.
no	Disables creation of new timing arcs.

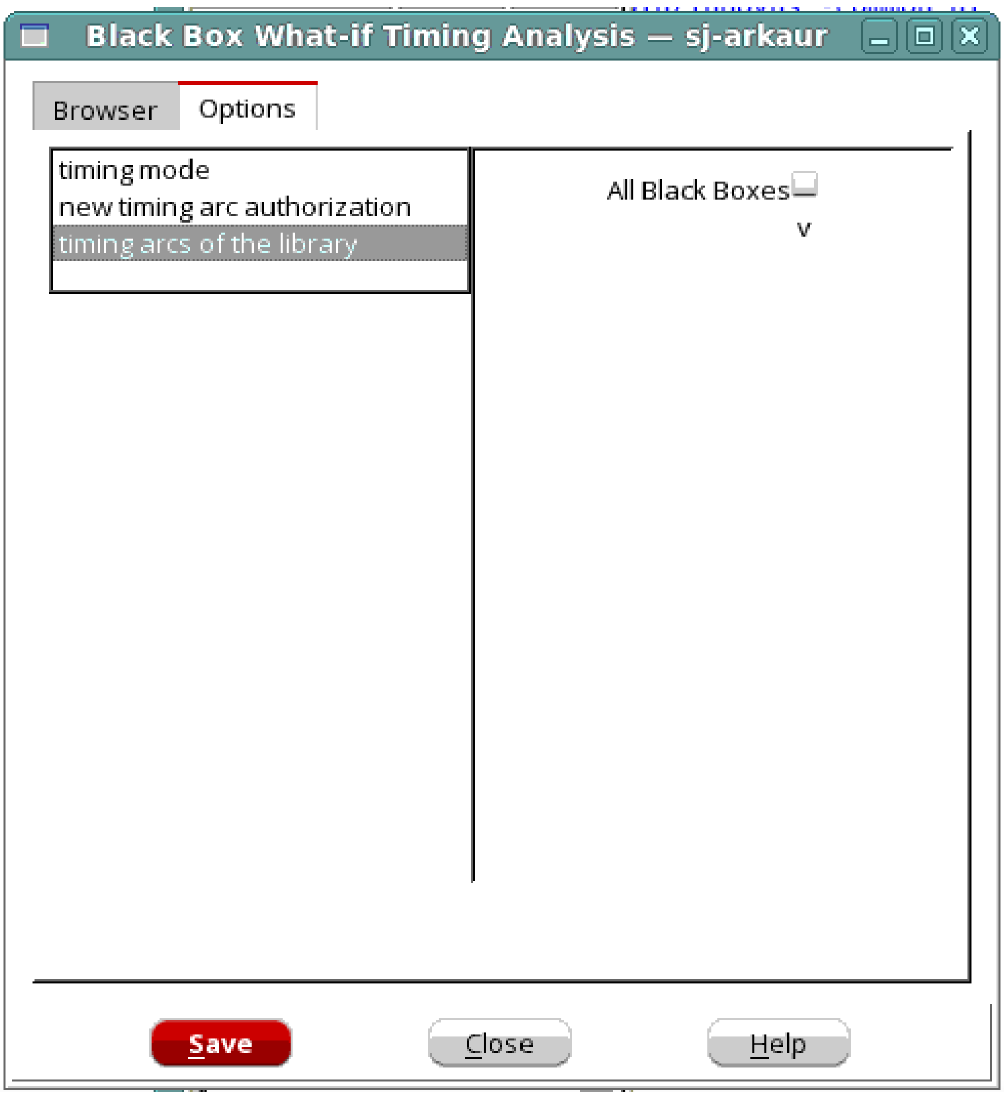
Related Topics

For information on the following topic, see "What-If Timing Analysis" in the *Innovus User Guide*.

- What-If Timing Analysis

Black Box What-If Timing Analysis - Options - timing arcs of the library

Use the *timing arcs of the library* page of the Black Box/Blob What-If Timing Analysis form to display the original timing arcs from the timing model in the *Browser* page.
→ From the *Options* page, select the *timing arcs of the library* category.



Black Box What-If Timing Analysis - Options - timing arcs of the library Fields and Options

All Black Boxes	Allows you to display timing arcs for all blackboxes.
Blackbox selections	Select the specific black boxes for which you want to display the timing arcs.

Related Text Commands

There is no related text command.

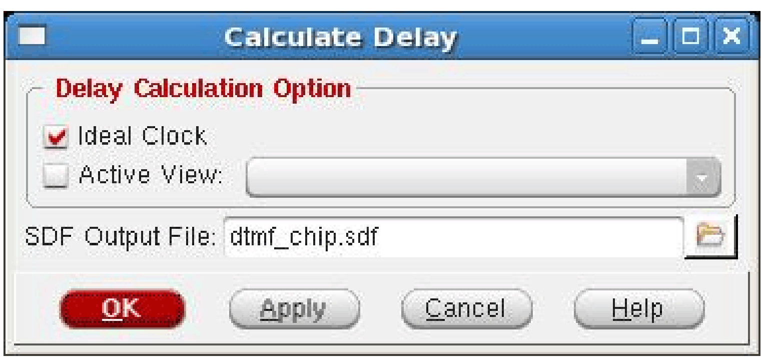
Related Topics

For information on the following topic, see "What-If Timing Analysis" in the *Innovus User Guide*.

- What-If Timing Analysis

Write SDF

Use the Calculate Delay form to calculate delays and generate an SDF file containing delay information.
→ Choose *Timing - Write SDF*.



Calculate Delay Fields and Options

Active View	Displays a list of active views that were created using the `set_analysis_view` command.
Ideal Clock	Forces the clock nets on each flip-flop clock input pin to use 0 ps. You can change the ideal default clock transition time in the *Timing* page in the Design Import form. The clock buffer delays are read from the timing library.
SDF Output File	Specifies the name of the SDF file to which to output the calculation results. Alternatively, click the file folder icon to choose a file. *Default:* `topModule .sdf`.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `write_sdf`
- `set_analysis_view`

For more information, see "Timing Analysis Commands" in the *Innovus Text Command Reference*.

Related Topics

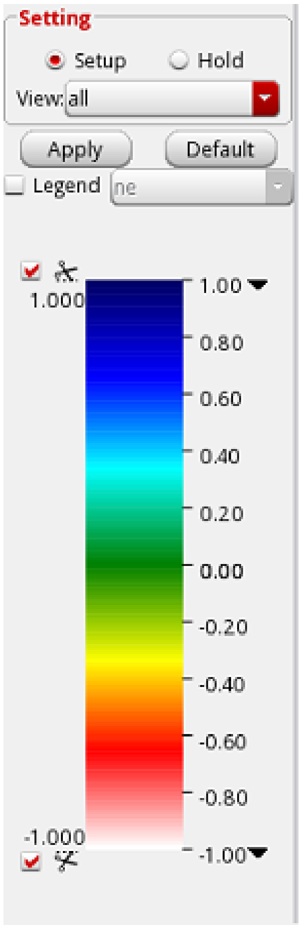
For information on the following topic, see "Calculating Delay" in the *Innovus User Guide*.

- Base Delay Analysis

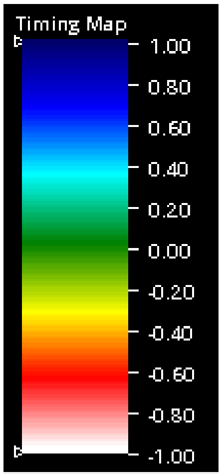
Display Timing Map

Use the Display Timing Map form to set color-coded slack threshold values for worst timing paths.
→ Choose *Timing - Display Timing Map*

This option allows you to sets color-coded slack threshold values for worst timing paths. You can specify a range of threshold values. When set, the instances as seen on the Timing Debug form are color-coded according to the worst timing slack threshold value.


Setting
Setup
Hold
View: all
Apply
Default
Legend
1.000
-1.000
1.00
0.80
0.60
0.40
0.20
0.00
-0.20
-0.40
-0.60
-0.80
-1.00

Display Timing Map Fields and Options

Setup	Specifies to display Setup timing paths.
Hold	Specifies to display Hold timing paths.
Apply	Stores the selected color-coded slack threshold values.
Default	Applies default settings.
Legend	Displays the legend colors and range details of the timing map. When selected, the legends box of the timing map is displayed in the layout area, as shown below.  You can select one of the following options to specify the horizontal alignment of the legend box within the design layout area: • `ne`: North east • `nw`: North west • `se`: South east • `sw`: South west *Default*: ne

⚠ Innovus will switch between Setup and Hold mode seamlessly and easily without re-calculation, once timing calculation for each mode is done.

Related Text Commands

The following text command provides equivalent or additional functionality:

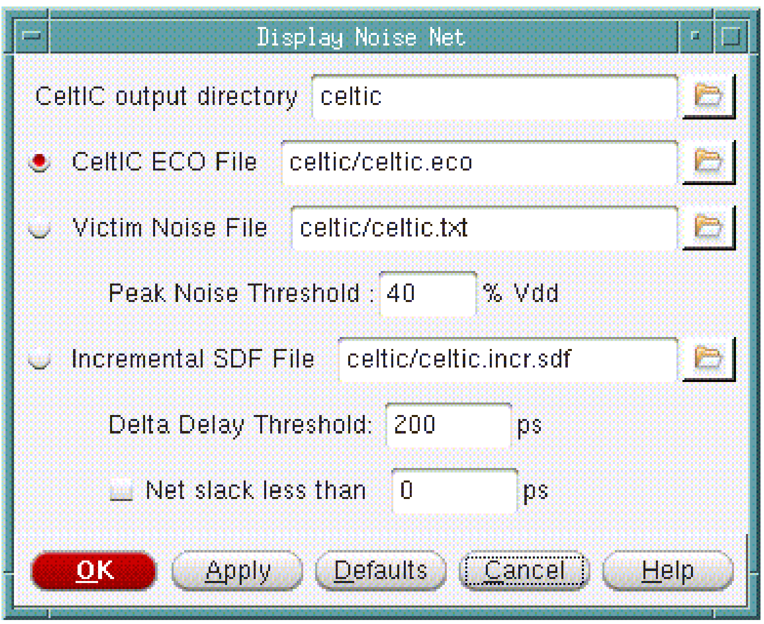
- display_timing_map

For more information, see "Timing Analysis Commands" in the *Innovus Text Command Reference*.

Display Noise Net

Use the Display Noise Net form to specify the files and parameters for displaying net noise. Clicking *OK* or *Apply* opens the CeltIC Result Browser form, which you can then use to browse net noise. For more information, see the CeltIC Result Browser.

→ Choose *Timing* - *Display Noise Net* .



Display Noise Net Fields and Options

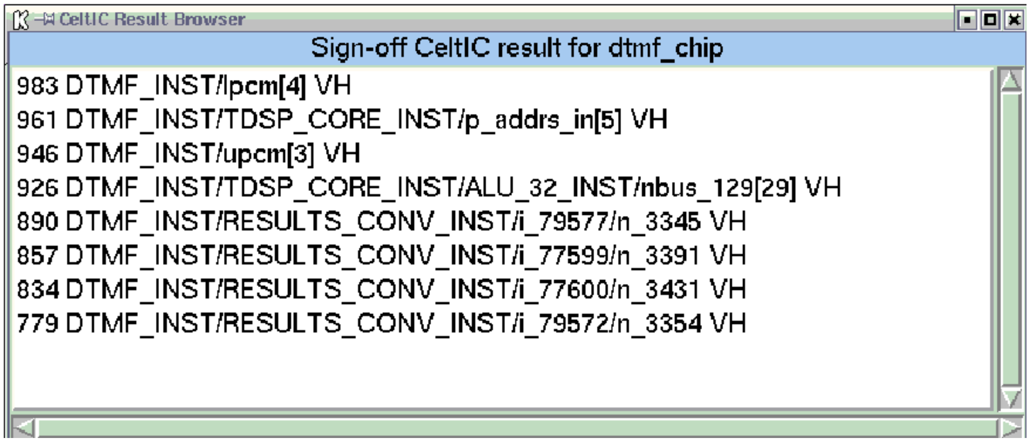
CeltIC output directory	Specifies the CeltIC directory in which to find the CeltIC noise analysis report files.	
CeltIC ECO File	Displays glitch violations recorded in the specified CeltIC ECO file. *Default:* celtic/celtic.eco	
Victim Noise File	Specifies the victim/aggressor net file to be used in the browser. *Default:* celtic/celtic.txt	
	Peak Noise Threshold:	Displays glitch violations based on the victim peak noise as a percentage of VDD. *Default:* 40
Incremental SDF File	Displays noise-induced delay violations based on the specified incremental SDF file. *Default:* celtic/celtic.incr.sdf	
	Delta Delay Threshold:	Displays nets with delta delays equal to or greater than the specified threshold value. *Default:* 200 ps
	Net slack less than	Displays nets with slacks that are less than the specified value. *Default:* 0 ps

Related Topics

For more information, see the "Analyzing and Repairing Crosstalk" chapter in the *Innovus User Guide*.

CeltIC Result Browser

The CeltIC Result Browser displays a sorted list of victim nets that suffer from the greatest amount of coupling noise.



Using CeltIC Result Browser

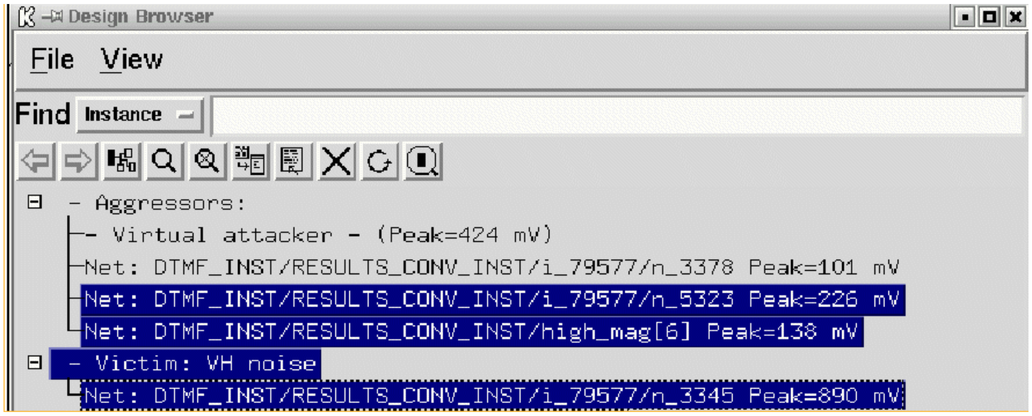
1. Use the Display Noise Net form to set up the options for the CeltIC Result Browser form. Click *OK* or *Apply* .

   After the report is read, the CeltIC Result Browser form opens.

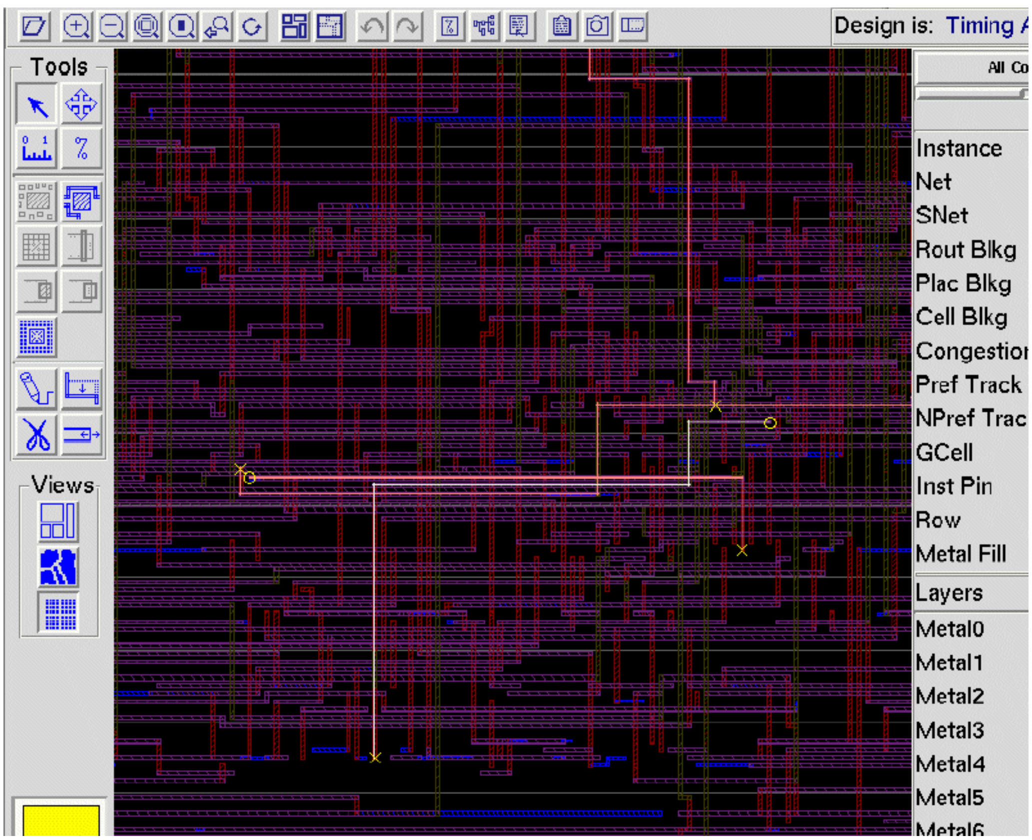
   Note: The report will depend on which of the three radio buttons is selected in the Display Noise Net form (*Peak Noise Threshold* , *CeltIC ECO File* , or *Incremental SDF File*).

2. To view a net in the design display area, double-click on one of the nets in the list.
   The net is selected and zoomed-in automatically.
3. To highlight aggressors and victim nets at the same time, click the *Browse Aggressors* button.
   The *Design Browser* window will open. Press `Ctrl` and click on multiple nets in the design browser, then choose *View - Zoom Selected*.

4. To view the highlighted nets in the design display area, click on any of the nets in the *Design Browser* window, then choose *View - Zoom Selected .*



5. To view all victim and aggressor nets, use the Design Browser and press `Ctrl` or `Shift`, then click with the mouse. The victims net are shown in white; the aggressor nets are shown in red.



6. To get information about coupling capacitance on selected nets, click *Report Coupling Caps* from the *CeltIC Result Browser* form.

Timing Debug Preferences

13

Verify Menu

Verify Geometry

Use the Verify Geometry form to verify the widths, spacing, and internal geometry of the objects and wiring between them. The `verifyGeometry` command will be obsolete soon and will be replaced by verify_drc.

The Verify Geometry form has two pages:

- Verify Geometry - Basic
- Verify Geometry - Advanced

Verify Geometry - Basic

Use the *Basic* page of the Verify Geometry form to specify options for basic geometry checks.

- Choose *Verify - Verify Geometry.* The *Basic* tab is selected, by default.

Verify Geometry - Basic Fields and Options

Verification Area	Select one of the following options:	
	Entire Area	Verifies all geometries in the whole design, based on the settings on this form.

	Specify	Verifies geometries in the area you specify by using one of the following methods: • Using the *Draw* button and your mouse to create a rectangular area in the design. The software displays the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields. • Manually enter the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields. • Using the *View Area* button to retrieve the coordinates of the current viewing area in the Innovus design display window.
Layer Range	Specifies the layer range for verifying geometry. To verify geometry within only a specific layer range in the design, select the *Layer Range* check box and specify the top and bottom layers of the range using the *Top Layer* and *Bottom Layer* drop-down list.	
Check	Select one or more of the following options:	
	Minimum Width	Checks that special wire geometries in the design are not smaller than the minimum default size for that layer, as specified in the LEF file.
	Minimum Area	Checks objects smaller than the AREA specified in the LAYER section of the LEF file. If AREA is not defined for a layer in LEF, and TOPOFSTACKONLY via is defined, Verify Geometry sets the value of AREA for that layer as the area of the bottom rectangle of the TOPOFSTACKONLY via.
	Short	Checks for shorts between two geometries belonging to different nets.
	Cell Overlap	Checks for overlapping cells in the routed design, as well as overlapping blockages from different components.
	Insufficient Metal Overlap	Checks that the overlap of two geometries meets the minimum size requirement for the layer.

	MinHole	Checks violations where the minimum area of the hole is less than the minimum enclosed area defined in the LEF file.
	Minimum Cut	Checks whether vias have the number of cuts specified by the `MINIMUMCUT` rule. The rule specifies the number of cuts a via must have when it is on a wide wire or pin whose width is greater than width. The rule applies to all vias touching a particular metal layer.
	Via Enclosure	Checks whether via enclosures meet the specified required x and y enclosure values for the bottom and top metal layers.
	Minimum Spacing	Checks that the spacing between two geometries does not violate the minimum spacing rule in the LEF file. If this option is deselected, all spacing rules are ignored.
	Same Net Spacing	Checks for violations between two geometries belonging to the same net. These violations can occur when minimum spacing is less than the value defined by the SAMENET SPACING rule in the LEF file or stack via with no corresponding STACK keyword in the SAMENET SPACING rule are present.
	Geometry Antenna	Checks for wires that do not terminate at wires, pins or vias and vias that do not terminate at wires, vias, or pins.
	Off Routing Grid	Checks whether each geometry covers at least one grid point on the routing grid. This check reports two kinds of violations: non-grid and off-grid. • Non-grid violations are reported for blockages, pins, special wires, and special vias that do not enclose a grid-point. • Off-grid violations are reported for regular vias whose centers do not lie on-grid and for regular wires whose start and end points do not lie on-grid.
	Off Manufacturing Grid	Checks for objects whose corners are off the manufacturing grid.

	Implant Check	Checks violations on implant layers. Use this parameter when you run `verifyGeometry` before inserting filler cells.
	MinStep	Checks for minimum step violations.
	Merged MGrid Check	Checks for objects whose edges are covered by other on-grid shapes. By default, Verify Geometry checks and reports violations of these edges.
Allow	Select one or more of the following options:	
	Pin In Blockage	Allows pin and obstruction shorts on the same component.
	Same Cell Violations	Allows same-cell violations. This parameter is disabled when *Different Cell Violations* is selected.
	Different Cell Violations	Allows violations between two different cells. When this option is selected, the following three parameter are disabled: • *Same Cell Violations* • *Overlap of Routing Blockages And Pins* • *Overlap of Routing Blockage and Cell Blockage*
	Overlap of Pad Filler Cells	Allows overlap violations between pad filler cells.
	Blockage Overlap of Routing Blockages And Pins	
		Allows a routing obstruction to overlap a pin. This parameter is disabled when *Different Cell Violations* is selected.
	Overlap of Routing Blockage and Cell Blockage	
		Allows overlapping cell and routing obstructions. This parameter is disabled when *Different Cell Violations* is selected.

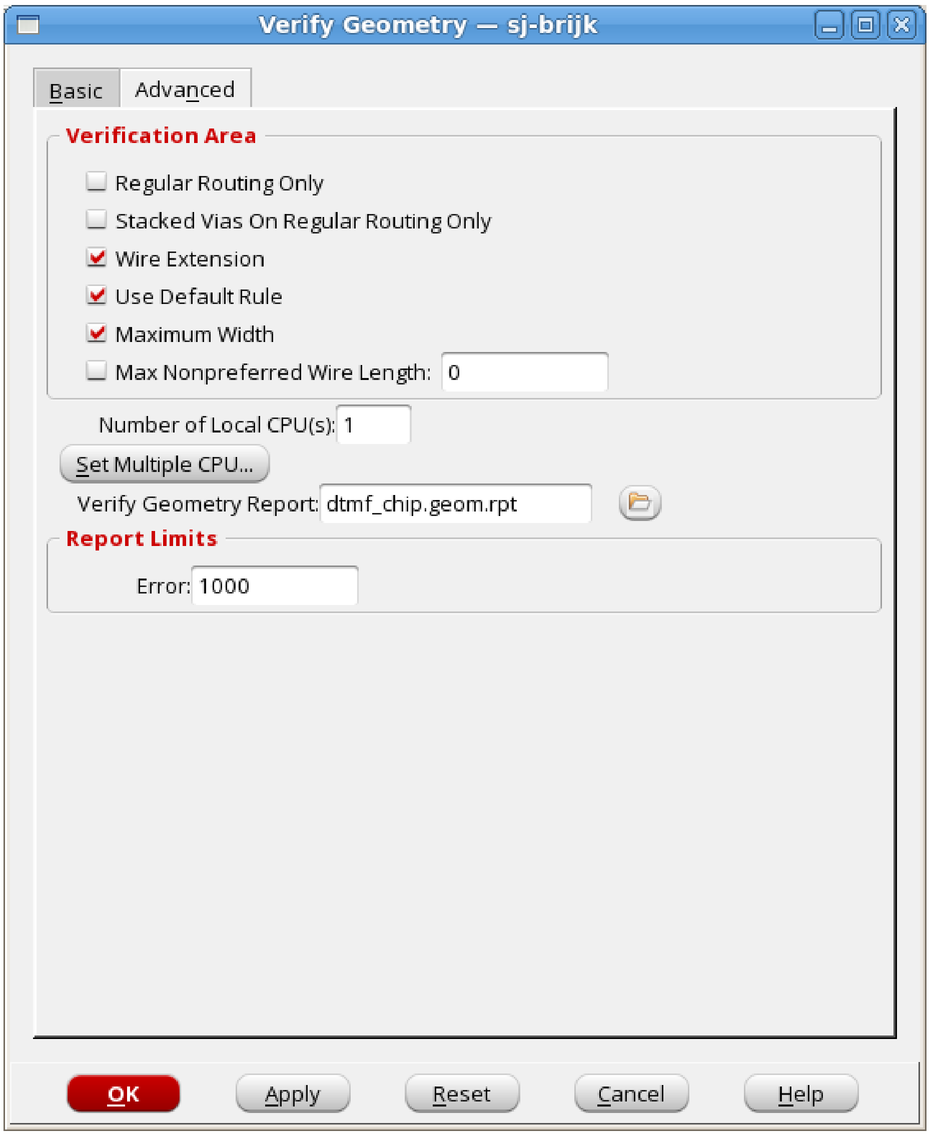
Related Text Commands

- `verifyGeometry`

Verify Geometry - Advanced

Use the *Advanced* page of the Verify Geometry form to specify advanced checks.

- Choose *Verify - Verify Geometry* and click on the *Advanced* tab.



Verify Geometry - Advanced Fields and Options

Regular Routing Only	Checks for violations in regular routing only. All violations between special geometries are ignored.
Stacked Vias On Regular Routing Only	
	Checks for stacked vias in regular routing only. All stacked via violations in special routing are ignored.
Wire Extension	Checks that wires are extended by the amount specified in the `WIREEXTENSION` definition in the Layer (Routing) section of the LEF file, and checks that vias dropped onto pins also satisfy wire extension.
Use Default Rule	Ignores nondefault spacing rules for spacing violations. Uses default rules for spacing violations. By default, spacing larger than the minimum spacing in nondefault rules are "soft" rules, that is, preferred spacing rules that are not enforced by the router and not checked by `verifyGeometry`. If you do not select this option, `verifyGeometry` treats non-default spacing rules as "hard" rules and creates violations whenever they are not met.
Maximum Width	Checks objects whose widths are greater than the `MAXWIDTH` specified in the Layer section of the LEF file.
Max Nonpreferred Wire Length	
	Sets the maximum length for wires in the nonpreferred routing direction. *Default:* 0
Number of Local CPU(s)	Displays the number of CPUs on the local machine used for verifying geometry. This option is required for multi-threading. This is a non-editable field.
Set Multiple CPU	Opens the Set Multiple CPU Processing form, which allows you to specify options for multi-threading.
Verify Geometry Report	Specifies the filename for the Verify Geometry Report. The file contains detailed information that is suitable for debug purposes only. For a concise list of violations, use the Violation Browser report file.

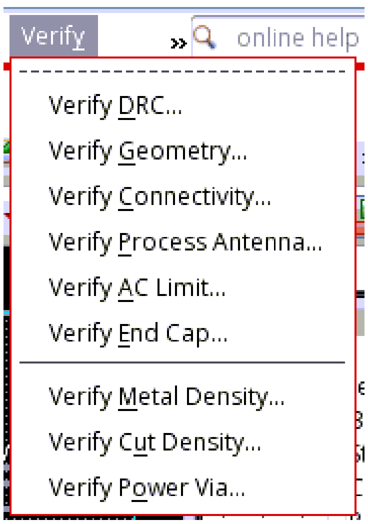
Error	Specifies the maximum number of errors to report. The software generates a warning message if this number is exceeded. *Default:* `1000`

Related Text Commands

- `verifyGeometry`

Verify DRC

The `verify_drc` command supports all the tech nodes. Use the Verify DRC form to check the DRC violations.



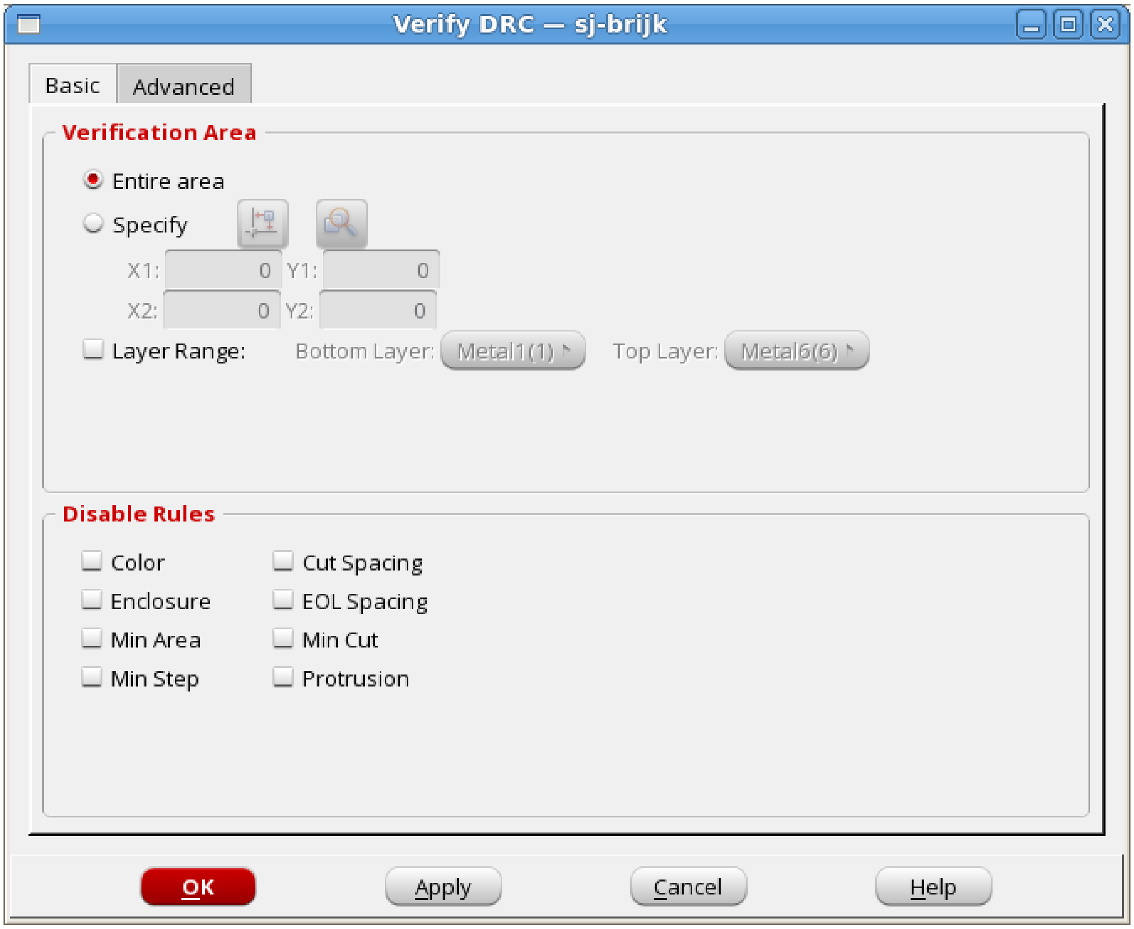
The Verify DRC form has two pages:

- Verify DRC - Basic
- Verify DRC - Advanced

Verify DRC - Basic

Use the *Basic* page of the Verify DRC form to specify options for basic DRC checks.

- Choose *Verify - Verify* DRC. The *Basic* tab opens by default.



Verify DRC - Basic Fields and Options

Verification Area	Select one of the following options:	
	Entire Area	Checks for DRC violations in the whole design, based on the settings on this form. This is the default option.

	Specify	Checks for DRC violations in the area you specify by using one of the following methods: • Using the *Draw* button and your mouse to create a rectangular area in the design. The software displays the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields. • Manually enter the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields. • Using the *View Area* button to retrieve the coordinates of the current viewing area in the Innovus design display window.
Layer Range	Specifies the layer range for reporting DRC violations. To report DRC violations within only a specific layer range in the design, select the *Layer Range* check box and specify the top and bottom layers of the range using the *Top Layer* and *Bottom Layer* drop-down list. The default value of *Top Layer* is the top layer of the design, while the default value of *Bottom Layer* is the bottom layer of the design. *Default*: Off	
Color	Specifies whether or not the color rule will be checked. *Default*: Off	
Cut Spacing	Specifies whether or not cut spacing rule will be checked. *Default*: Off	
Enclosure	Specifies whether or not the enclosure rule will be checked. *Default*: Off	
EOL Spacing	Specifies whether or not the EOL spacing rule will be checked. *Default*: Off	
Min Area	Specifies whether or not the min area rule will be checked. *Default*: Off	
Min Cut	Specifies whether or not the min cut rule will be checked. *Default*: Off	
Min Step	Specifies whether or not the min step rule will be checked. *Default*: Off	

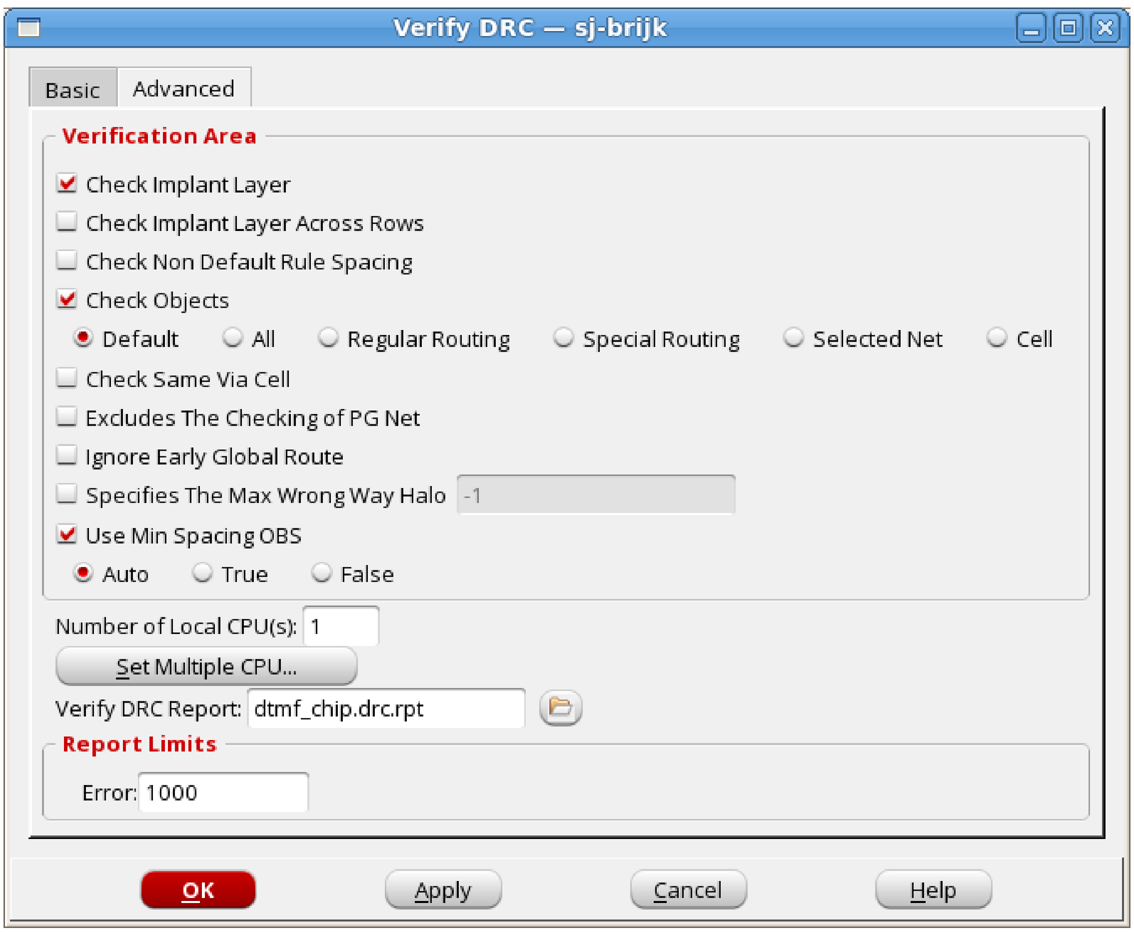
Protrusion	Specifies whether or not the protrusion rule will be checked. *Default*: Off

Related Text Commands

- verify_drc
- get_verify_drc_mode
- set_verify_drc_mode

Verify DRC - Advanced

Use the *Advanced* page of the Verify DRC form to specify advanced DRC checks.



Verify DRC - Advanced Fields and Options

<table>
<tr><td>Check Implant Layer</td><td colspan="2">Checks for violations on implant layers.
Default: On</td></tr>
<tr><td>Check Implant Layer Across Rows</td><td colspan="2">Performs implant checks across rows.
Default: Off</td></tr>
<tr><td>Check Non Default Rule Spacing</td><td colspan="2">Checks non-default rule spacing as a hard rule.
Default: Off</td></tr>
<tr><td>Check Objects</td><td colspan="2">Specifies the type of shapes to be checked. Select one of the following options:
Default: Off</td></tr>
<tr><td></td><td>All</td><td>Reports violations between all routing shapes (regular and special) and all other shapes (including routing blockages, and cell pin/obs shapes). This is the default value if Check Objects is selected.</td></tr>
<tr><td></td><td>Regular Routing</td><td>Reports only the violations between regular routing shapes (normally created by NanoRoute) and all other shapes. It does not report violations between special routes, routing blockages, and cell shapes. Use this option if you want to find only the violations caused by NanoRoute.</td></tr>
<tr><td></td><td>Special Routing</td><td>Reports only the violations between special routes and all other shapes. It does not report violations between regular routes, routing blockages, and cell shapes. Use this option when you want to check power routing or pre-routed special routes and isolate these errors from other violations.</td></tr>
<tr><td>Check Same Via Cell</td><td colspan="2">Checks the cut spacing from the same via.
Default: Off</td></tr>
</table>

Excludes The Checking of PG Net	Excludes the checking of power and ground nets. *Default*: Off
Ignore Trial Route	Ignores early global route when checking drc. *Default*: Off
Specifies The Max Wrong Way Halo	Specifies the length up to which short jog shapes in halo area can be ignored. Routing halos are used to avoid cross-coupling between top-level and inside-the-block routes, and short jogs do not affect cross-coupling much. Normally, it is better to have some short jogs rather than more vias. When this option is specified, any segment with length less than the specified length is ignored for wrong way check, even if it overlaps with the halo region. Verify DRC reports violations only for jog shapes with lengths greater than the specified halo length.
Use Min Spacing OBS	Checks all the Macro OBS with minSpacing. *Default: Auto*
Number of Local CPU(s)	Displays the number of CPUs on the local machine used for verifying geometry. This option is required for multi-threading. This is a non-editable field. The initial value is 1.
Set Multiple CPU	Opens the Set Multiple CPU Processing form, which allows you to specify options for multi-threading.
Verify DRC Report	Specifies the file name for the Verify DRC report. The file contains detailed information that can be used for debugging. *Default*: `<DesignName>.drc.rpt`
Error	Specifies the maximum number of errors to report. The software generates a warning message if this number is exceeded. *Default:* 1000

Related Text Commands

- verify_drc
- get_verify_drc_mode
- set_verify_drc_mode

Verify Connectivity

Use the Verify Connectivity form to detect conditions such as opens, unconnected wires (geometric antennas), unconnected pins, loops, partial routing, and unrouted nets. When you verify connectivity, the software generates violation markers in the design window and reports violations. Verifying connectivity does not have database impact unless you save the design, which also saves the violation markers.

Types of Violations Reported

- Antennas (Dangling Wires)
  Unconnected wires (dangling wires). For more information, see the 'Types of Antenna Violations Reported' section in the "Identifying and Viewing Violations" chapter of the *Innovus User Guide*.
- Opens
  Parts of nets, such as wires or pins, that are connected to each other but are missing a connection to the net as a whole. Marks each part of a net that is missing a connection as an open and displays a violation marker between the parts.
- Loops
- Unconnected pins
  Pins that are not connected to any other objects

Checks for Opens, Unconnected Pins, and Unrouted Nets

The following combinations of connectivity checks are not enabled:

Open	***Unconnected Pin***	***Unrouted Net***

Off	On	On
Off	On	Off
Off	Off	On

- Choose *Verify - Verify Connectivity*.

Verify Connectivity Fields and Options

Net Type	Select one of the following options. *Default: All*	
	All	Checks all nets, including those that have been previously verified.
	Regular Only	Checks only regular nets.
	Special Only	Checks only special nets.
Nets	Select one of the following options. *Default: All*	
	All	Checks all nets of the type specified in the *Net Type* panel.
	Selected	Checks only nets in the selected set that are of the type specified in the *Net Type* panel.
	Named	Checks only nets of the name specified that are of the type specified in the *Net Type* panel. You can use wildcards (`*` and `?`) when you specify the net names.
Check	Select one or more of the following options:	
	Open	Checks for open violations. Opens are parts of nets, such as wires or pins, that are connected to each other but are missing a connection to the net as a whole.
	UnConnected Pin	Checks for pins that are not connected to any objects.
	Unrouted Net	Checks for nets that are not routed.

	Connectivity Loop	Checks for connectivity loops in regular wires. The software detects connectivity loops based on the end points of the center line of a regular wire segment or the center of a via. *Connectivity Loop*, *Geometry Loop*, and *Geometry Connectivity* are mutually exclusive.
	DanglingWire Antenna	Checks for violations due to unconnected wires (also called geometrical antennas or dangling wires). For more information, see the 'Types of Antenna Violations Reported' section in the "Identifying and Viewing Violations" chapter of the *Innovus User Guide*.
	Weakly Connected Pin	Checks for routing to more than one port of the weakly connected pin ports. When this option is selected, Verify Connectivity marks a Weakly Connected Pin violation in one of the ports of the pin.
	Geometry Loop	Checks for loop violations of regular nets using a geometrical model. The nets do not have to overlap on the center line. When you specify this option, the software does not perform any other connectivity checks. Select this option if you use a third-party router that does not route using the centerline connection routing technique. In this case, *Connectivity Loop* might not detect connectivity loop violations. *Connectivity Loop*, *Geometry Loop*, and *Geometry Connectivity* are mutually exclusive.

	Geometry Connectivity	Checks for connectivity violations of regular wires. Uses a geometrical model instead of the center-line model. In other words, if the wires overlap at any point, they are considered to be connected--they do not have to connect at the center line. Use this parameter if you manually change the routing or use a third-party router that does not route using the center-line connection routing technique. *Connectivity Loop*, *Geometry Loop*, and *Geometry Connectivity* are mutually exclusive.
	Keep Previous Results	Displays incremental results in the Violation Browser. When this option is selected, Verify Connectivity appends violation markers to the previous results instead of overwriting them.
	Divide Power Net	Divides power nets into four subareas for connectivity verification. Use this option to decrease memory usage in 32-bit machines with limited memory. This option might increase or decrease the run time, depending on the design.
	Soft PG Connect	Checks soft Power/Ground connects on masterslice layers. This option is enabled by default. Deselect this option if you want connectivity on masterslice layers to be ignored.
	Raw Violations Mark	Displays violation markers for opens as the bounding box of the island. By default, violation markers for opens are displayed as polygons that include all wires, pins, and vias that connect to the island.
	Use Virtual Connection	Implies a virtual connection for all bumps and external I/O pins of the same net. Select this option to override default behavior of Verify Connectivity in which bumps and external I/O pins of the same net are not considered to be interconnected. It is useful in flip chip designs, where the power bumps are connected outside the chip.
	TSV Die Abstract File	Specifies the input file for TSV die.

Verify Connectivity Report		
	Specifies the report file for connectivity violation data.	
Report Limits	Specifies error and warning limits	
	Error	Specifies the maximum number of errors to report. The software generates a warning message if this number is exceeded. *Default:* `1000`
	Warning	Specifies the maximum number of warnings to report. *Default*: `50`
Set Multiple CPU	Displays the Multiple CPU Processing form in which you can specify multi-threading settings for verifying connectivity.	

Related Text Commands

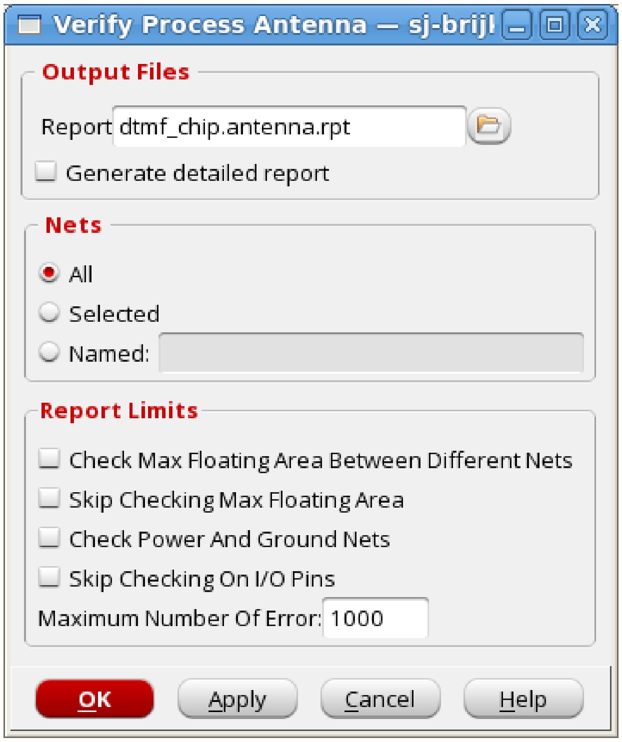
`verifyConnectivity`

Verify Process Antenna

Use the Verify Process Antenna form to verify Process Antenna Effect (PAE) violations in the routed design.

Note: Verify Process Antenna also checks for maximum floating area violations in the design. For more information, see `verifyProcessAntenna` in the *Innovus Text Command Reference*.

- Choose *Verify - Verify Process Antenna*.



Verify Process Antenna Fields and Options

Output Files	Displays the names of the output files this command creates.
Report	Specifies the report file. *Default:* `design.antenna.rpt`
Generate detailed report	Generates a detailed report containing process antenna information for all nets, including those without violations. For more information, see "Sample Process Antenna Report" in the *Innovus User Guide*.
Nets	Select one of the following options:
All	Reports violations for all the nets in the design.
Selected	Reports violations for selected nets only.
Named	Reports violations for only the nets named in this field. Separate names with a space.

Report Limits	Lets you specify what to check and the maximum number of errors to report.
Check Max Floating Area Between Diff Nets	
	Checks the maximum floating area between different nets. *Default:* Off
Skip Checking Max Floating Area	
	Disables check for maximum floating area violations. *Default:* Off
Check Power and Ground Nets	Checks tie-high and tie-low nets for process antenna violations. *Default:* Off
Skip Checking on I/O Pins	Does not check I/O pins for errors. The following LEF keywords are not applied to the I/O pins in the design: • `ANTENNAINPUTGATEAREA` • `ANTENNAINOUTDIFFAREA` • `ANTENNAOUTPUTDIFFAREA`
Maximum Number of Error	Specifies the maximum number of errors to report. The software generates a warning message if this number is exceeded. *Default:* `1000`

Related Text Commands

`verifyProcessAntenna`

Verify AC Limit

Use the Verify AC Limit form to check for AC current violations on signal nets.

Calculates the root mean square current (Irms) at the driver output and compares it to the

ACCURRENTDENSITY tables in the LEF file that contain the Irms limits for routing layers. Generates an error and attaches a violation marker to a net if the calculated Irms for a net exceeds the ACCURRENTDENSITY Irms limit for a routing layer or width used by the net.

Computes the root mean square current (Irms) from the slew rates of the signal, the capacitance of the net, and the toggle-rate frequency as computed by timing analysis commands like buildTimingGraph and check_timing (and the values can be written out with the -report parameter). If there is more than one timing view in use, uses the default setup view (controlled by set_default_view -setup *viewName* command).

setup view (controlled by set_default_view -setup *viewName* command).

Tip: For increased accuracy on long wires, use SignalStorm® to calculate Irms. In the AC Limit report file, Irms values that are calculated using SignalStorm end with dollar signs ($). To enable SignalStorm calculation, run the following command before running verifyACLimit:

```
setDelayCalMode -engine signalStorm
```

For more information, see setDelayCalMode in the *Innovus Text Command Reference*.

verifyACLimit checks each routing segment separately, eliminating false violations that might be caused by assuming the same current for the entire route. This feature is useful for calculating current at the inputs where it is not as strong due to branching and tapering of wires.

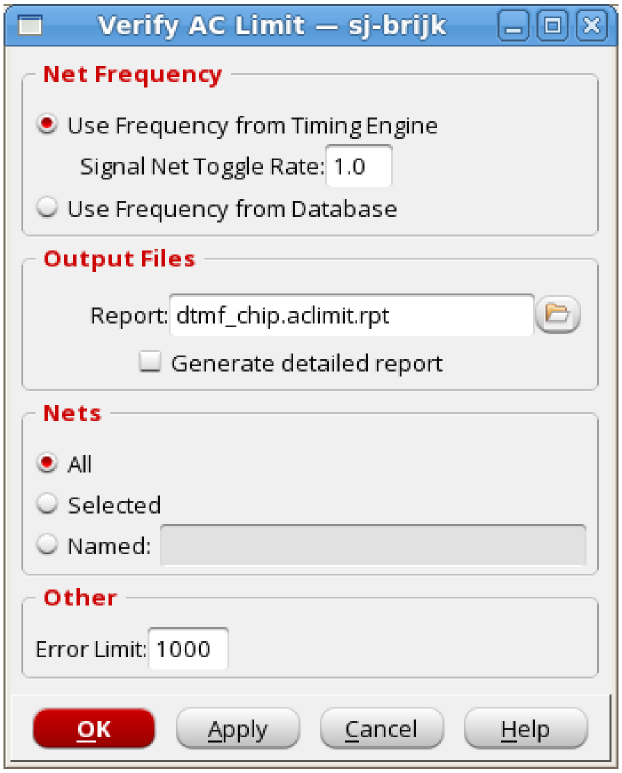
Routing with loops in it, like a clock-mesh, is ignored although the initial driver output and wiring Irms that connect to a mesh can be computed if SignalStorm delay calculation is used.

verifyACLimit also checks the ACCURRENTDENSITY tables for the following conditions and takes the following actions:

- If there is no table for a routing layer, the software gives a warning and assumes an infinite limit for the layer.
- If PEAK and AVERAGE tables are present, the software ignores them.

Note: This command reports the AC current density in mA. The LEF file specifies it in mA/micron. To convert the LEF specification, the verifyACLimit command reads the value in mA/micron and multiplies it by the wire width.

- Choose *Verify - Verify AC Limit.*



Verify AC Limit Fields and Options

Use Frequency from Timing Engine		
	Uses the frequency from the timing engine as the effective frequency (F_{eff}) per net. The software estimates the effective frequency from the timing analysis engine by using the frequency of the associated clock. The effective frequency of the net is half the associated clock frequency times the toggle rate, because the output of a flip-flop and downstream logic only changes at half the rate of the input clock. Specify the following option to set the toggle rate for signal nets:	
	Signal Net Toggle Rate	Specifies the toggle rate for signal nets. A value of 1.0 means that if a flip-flop is clocked by a 20 Mhz clock, it changes state on 100% of the clock cycles. Therefore the signal has 20 million transitions which is half the number of transitions of the input clock. Therefore the final signal net frequency is 10 Mhz. *Range:* 0.0 to 1.0. *Default:* 1.0

Use Frequency from Database		
	Uses the database frequency value as the effective frequency per net. You cannot use this option if you set a value in the *Signal Net Toggle Rate* field. You use the `verifyACLimitSetFreq` command to set the effective frequency on each net in the database from the timing analysis results. You can then use the `dbNetFrequency` and `dbSetNetFrequency` Tcl functions to check or modify any given net before using the *Use Frequency from Database* option. The frequency values are stored in Hertz in the database.	
Report	Specifies the report file. The default file name is *`design`*`.aclimit.rpt`. The report file includes name of the net, Irms, interpolated `ACCURRENTDENSITY` limit (I_{limit}), layer, width, X and Y location, rise and fall time, effective frequency for the net (F_{eff}), Cnet and Vdd for each net. Specify the following option to generate a detailed report:	
	Generate detailed report	Generates a detailed AC limit report containing the information for all nets, including those without violations.
Nets	Select one of the following options:	
	All	Reports violations for all the nets in the design.
	Selected	Reports violations for selected nets only.
	Named	Reports violations for only the nets named in this field. Separate names with a space.
Others	Specify the following options:	
	Error Limit	Specifies maximum number of errors to report. The software generates a warning message if this number is exceeded. *Range:* 0 to 1000000 *Default:* 1000.

	Irms Scale Factor	Specifies the scale factor for root mean square current (I_{rms}). The software multiplies Irms value by the scale factor before checking for violations. The software uses a square wave to approximate current. To use a triangular wave approximation, specify 1.15. *Range:* 0.0 to 10.0 *Default:* 1.0

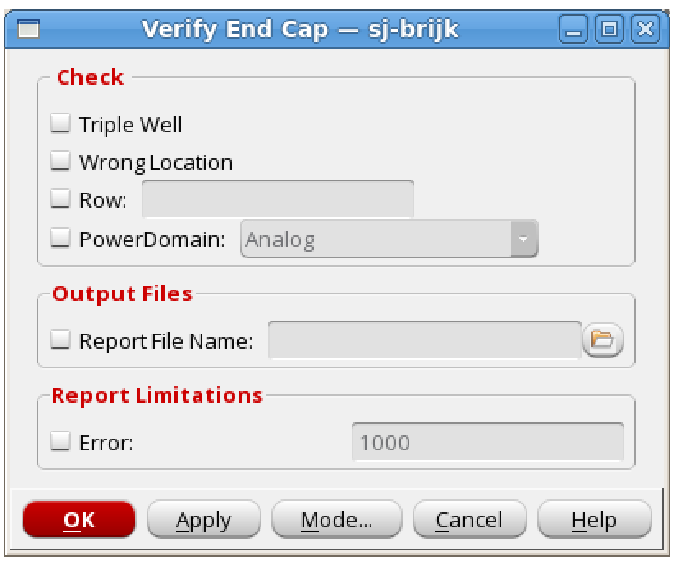
Related Text Commands

- `verifyACLimit`
- `verifyACLimitSetFreq`

Verify End Cap

Use the Verify End Cap form to check whether pre/post cap cells have been inserted correctly based on `setEndCapMode` settings.

- Choose *Verify - Verify End Cap*.



Verify End Cap Fields and Options

Triple Well	Checks triple well insertion. Only checks the cell lists specified in `setEndCapMode`.
Wrong Location	Checks for cap cells that are not inserted in the right location. Places a violation marker at any cap cell that is: • Not on the beginning/end of the row or • Not on the boundary of the design/block design
Row	Specifies the rows to be checked.
Power Domain	Specifies the power domains to be checked. Select this option to check end cap cells inserted for the specified power domain.
Report File Name	Specifies the file name for the Verify End Cap report.
Error	Specifies the maximum number of errors to report. *Default*: 1000

Related Text Commands

`verifyEndCap`

Verify Metal Density

Use the Verify Metal Density form to check the metal density for each routing layer and the density of large macros. When you verify the metal density, the software checks the density against the values specified by the LEF file or the `setMetalFill` command. If the density is not specified, the software uses internal default settings.

The `verifyMetalDensity` command can run without `setMetalFill`. The sequence is

- If the LEF file has window size and density defined, the Innovus database also has them, so `verifyMetalDensity` gets them from the database.

- If the LEF file does not have window size and density defined, the `verifyMetalDensity`uses internal default values.

  Note: The `setMetalFill` command is a user-override command that provides constraints at the run time for each session. These constraints have precedence over the LEF/database values.

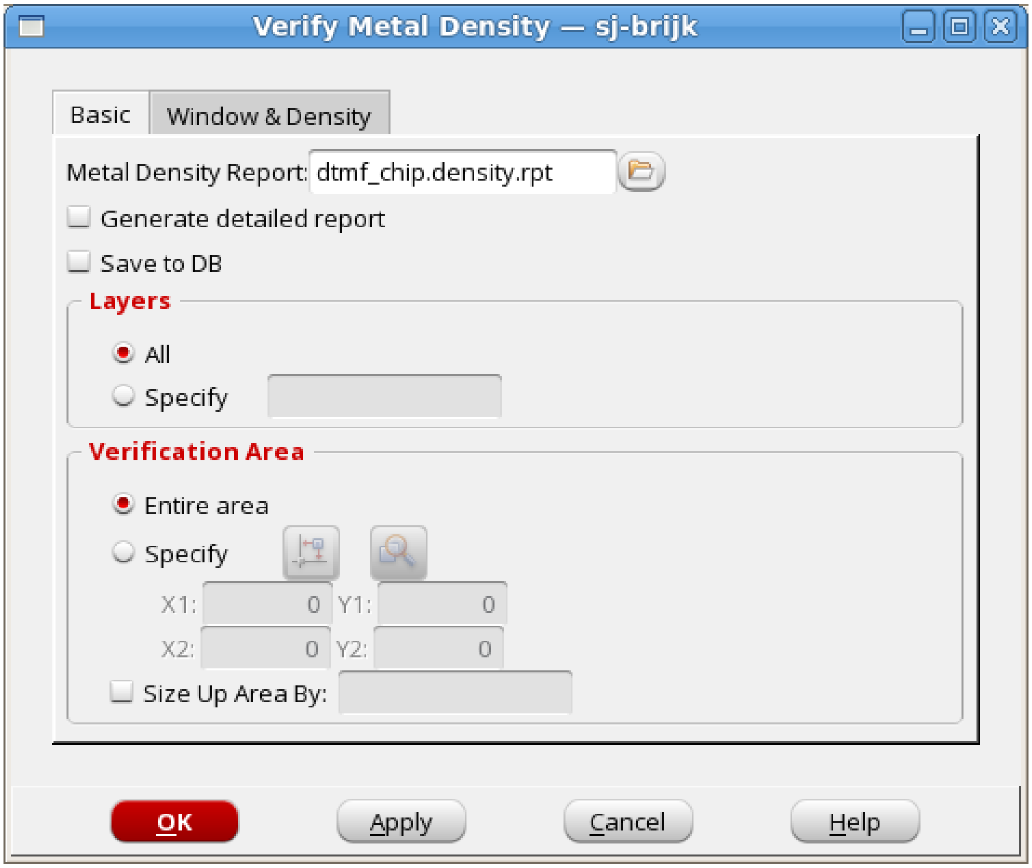
The Verify Metal Density form has two pages:

- Verify Metal Density - Basic
- Verify Metal Density - Window & Density

Verify Metal Density - Basic

Use the *Basic* page of the Verify Metal Density form to set options for specify options for the metal density report and the area on which to perform the metal density check.

- Choose *Verify - Verify Metal Density*.



Verify Metal Density - Basic Fields and Options

Metal Density Report	Specifies the report file. The default file name is `designName.density.rpt`.	
Generate detailed report		
	Generates a detailed metal density report.	
Save to DB	Saves density information to the Innovus database. The `write_lef_abstract` command outputs the density information into LEF macro density constructs.	
Layers	Select one of the following options:	
	All	Verifies all layers.
	Specify	Verifies the names of the layers that you specify.

Verification Area	Specifies whether you want to verify the entire or a specifc area. You can also choose to size up the area to be verified by a specific offset value.	
	Entire area	Verifies the entire area.
	Specify	Verifies metal density in the area you specify by using one of the following methods: • Using the *Draw* button and your mouse to create a rectangular area in the design. The software displays the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields. • Manually enter the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields. • Using the *View Area* button to retrieve the coordinates of the current viewing area in the design display window.
	Size Up Area By	Specifies an offset value for the area to verify. The value is in user units (not in DBU), and can be positive or negative. A positive value adds to the area that is verified. For example, if the design covers the area from (0,0) to (100,100) and you specify *Size Up Area By* value of 10, the tool checks the area from (-10,-10) to (110,110).

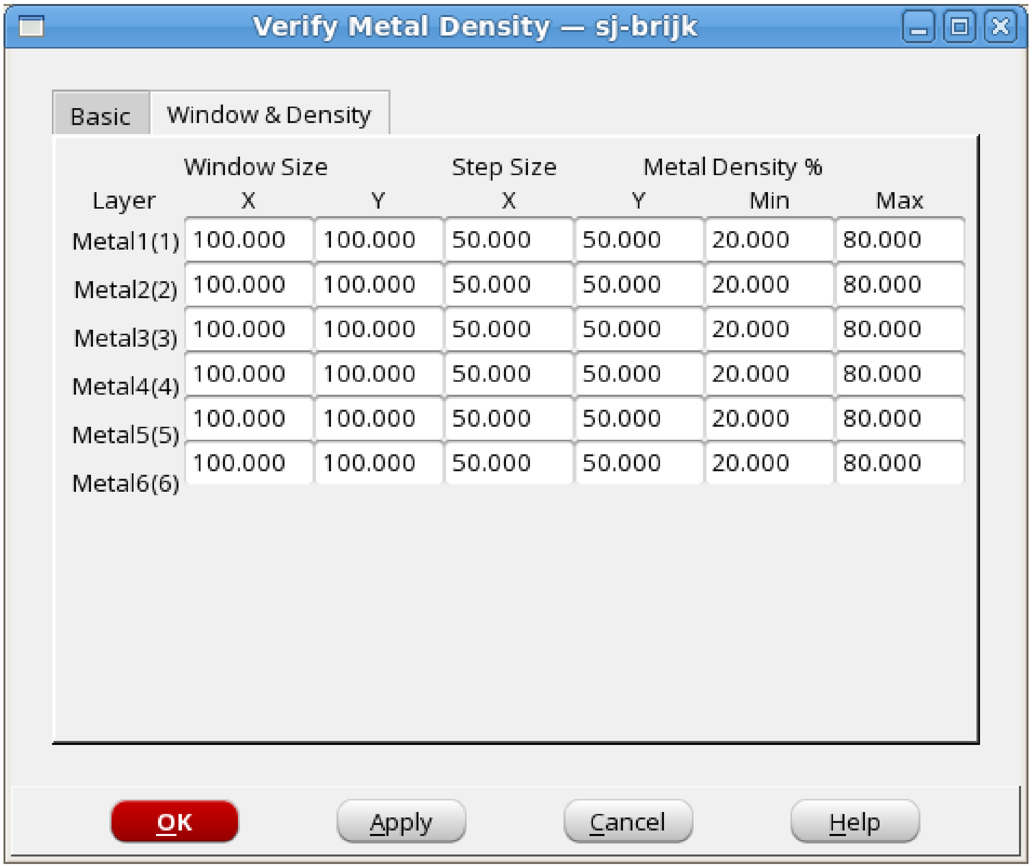
Related Text Commands

- `verifyMetalDensity`
- `setMetalFill`

Verify Metal Density - Window & Density

Use the *Window & Density* page of the Verify Metal Density form to specify window size, step size, and metal density percentage for each layer.

- Choose *Verify - Verify Metal Density* and click on the *Windows & Density* tab.



Verify Metal Density - Window & Density Fields and Options

Window Size	Specify the X and Y coordinates for each layer of the design.
Step Size	Specify the X and Y coordinates for each layer of the design.
Metal Density %	Specify the minimum and maximum values for each layer of the design.

Note: The values that you specify here are updated in the form that is displayed using the *Metal Fill* command in the *Route* menu.

Related Text Commands

- `verifyMetalDensity`
- `setMetalFill`

Verify Cut Density

The Verify Cut Density form enables you to check the density of specified cut layers or areas of cut layers, or the cut density of the whole chip.

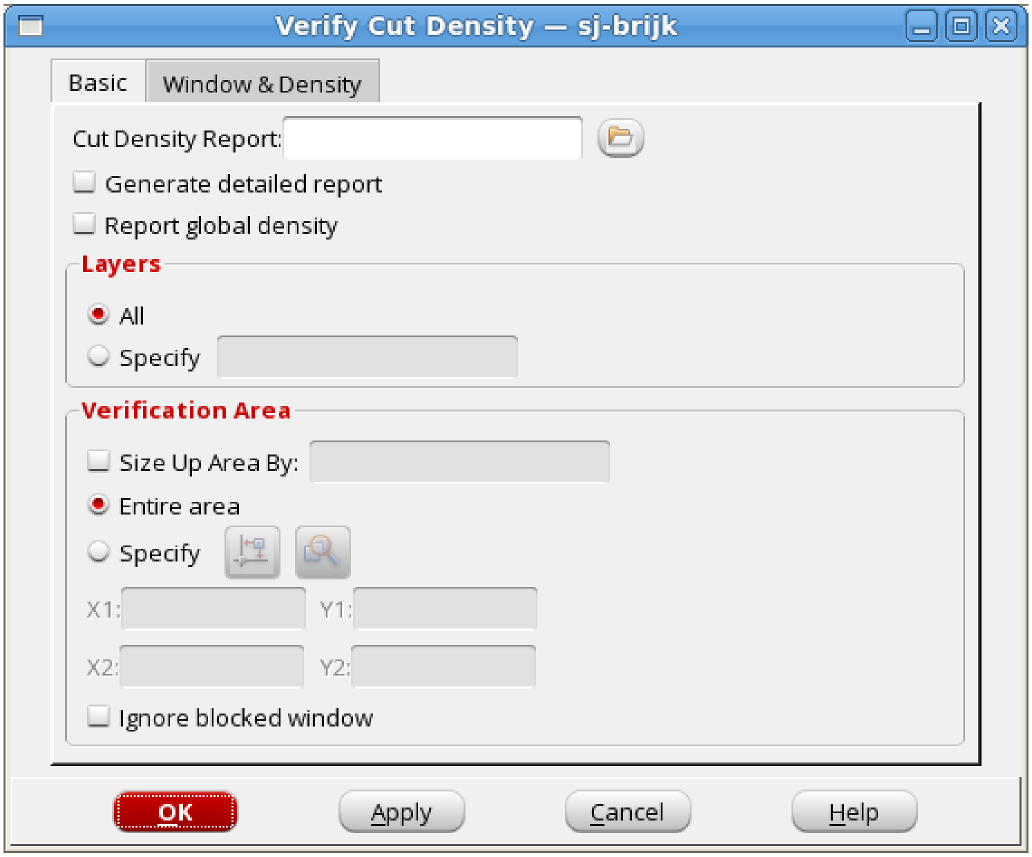
The Verify Cut Density form contains the following pages:

- Verify Cut Density - Basic
- Verify Cut Density - Window & Density

Verify Cut Density - Basic

Use the *Basic* page of the Verify Cut Density form specify options for the cut density report and the area to check.

- Choose *Verify - Verify Cut Density* and click the *Basic* tab.



Verify Cut Density - Basic Fields and Options

Cut Density Report	Specifies the report file for the cut density violation information. *Default:* `designName.cutdensity.rpt`	
	Generate detailed report	
		Generates a detailed cut density report.
	Report global density	
		Checks the density across the entire design for the specified cut layers and writes the results to the report file.
Layers	Specifies the cut layers to verify. Select one of the following options:	
	All	Check density on all cut layers.

	Specify	Checks density only on the specified layers. Use the following format to specify layer names: {V12 V23}
Verification Area	Specifies whether you want to verify the entire or a specifc area. You can also choose to size up the area to be verified by a specific offset value.	
	Size Up Area By	Specifies an offset value for the area to verify. The value is in user units (not in DBU), and can be positive or negative. A positive value adds to the area that is verified. For example, if the design covers the area from `(0,0)` to `(100,100)` and you specify `10`, the software checks the area from `(-10,-10)` to `(110,110)`.
	Entire	Checks the entire area on the specified layers.
	Specify	Checks the area within the bounding box you specify by using one of the following methods: • Using the *Draw* button and your mouse to create a rectangular area in the design. The software displays the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields. • Manually enter the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields. • Using the *View Area* button to retrieve the coordinates of the current viewing area in the design display window.
	Ignore blocked window	
		Disables checking of windows that are fully covered by block or pad obstructions.

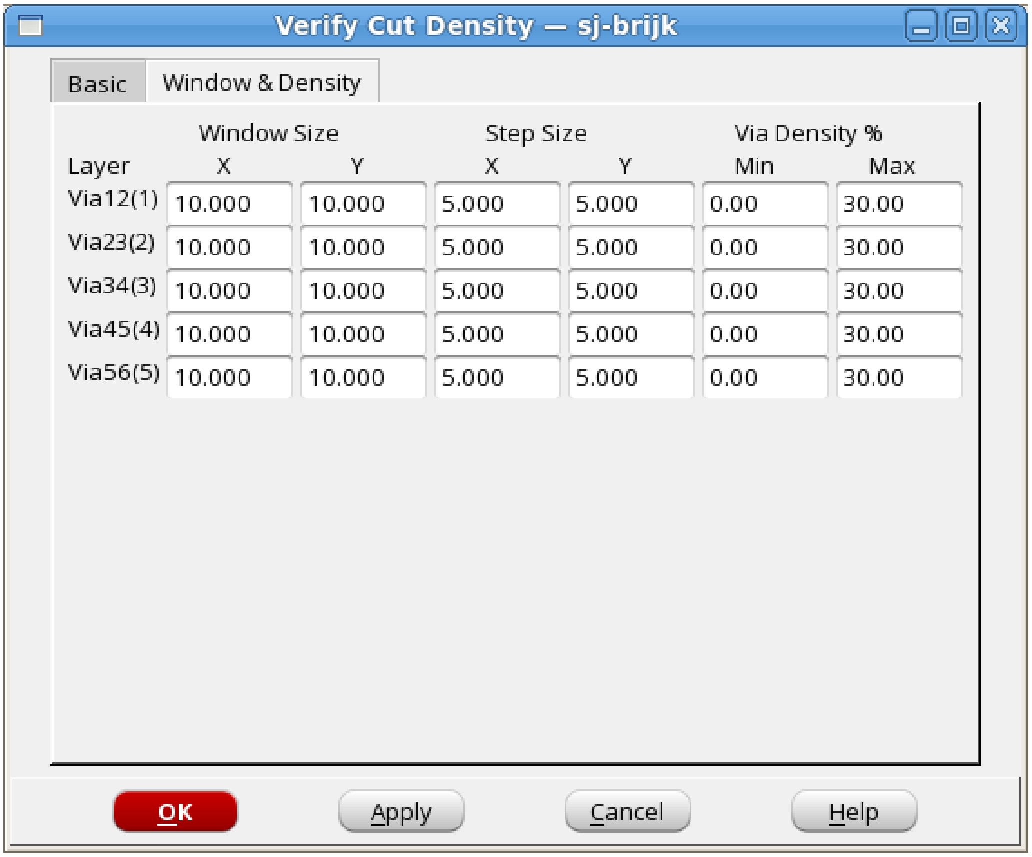
Related Text Commands

`verifyCutDensity`

Verify Cut Density - Window & Density

Use the Window & Density page of the Verify Cut Density form to specify window size, step size, and metal density percentage for each layer.

- Choose *Verify - Verify Cut Density* and click the *Window & Density* tab.



Verify Cut Density - Window & Density Fields and Options

Window Size	Specify the X and Y coordinates for each cut layer.
Step Size	Specify the X and Y coordinates for each cut layer.
Via Density %	Specify the minimum and maximum values for each cut layer.

Related Text Commands

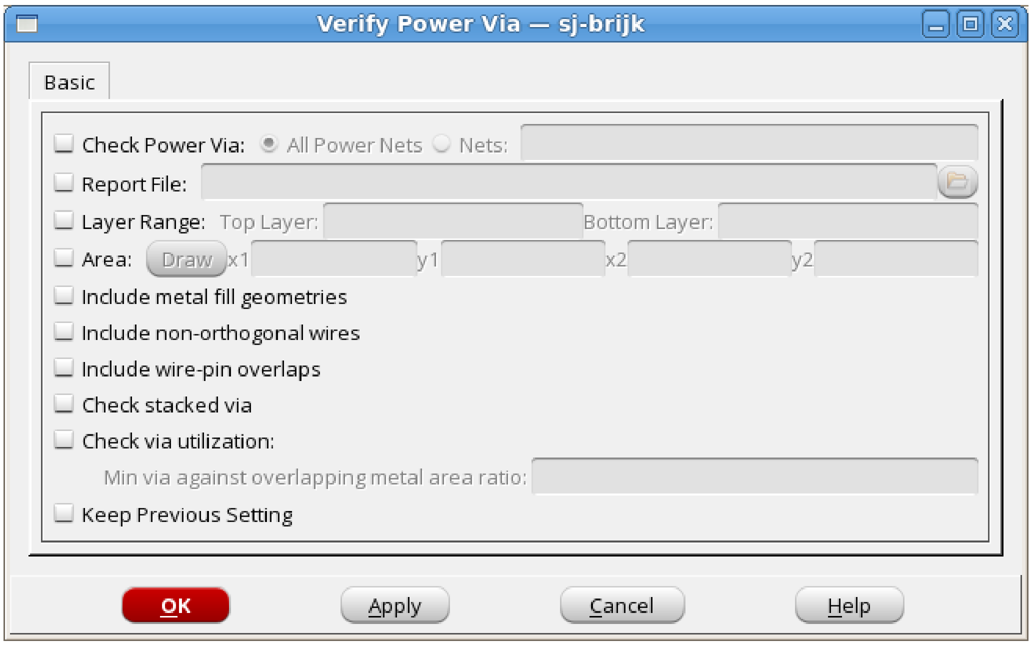
`verifyCutDensity`

Verify Power Via

Checks for metal geometry overlap on power-grid nets and for missing or open vias in the design.

Note: To verify the design, the power-grid must be routed.

- Choose *Verify - Verify Power Via*.



Fields and Descriptions

Check Power Via	• *All Power Nets*: Verifies power vias in all the power nets. This is the default option. • *Nets*: Verifies power vias in the specified net(s).
Report File	Specifies the name of the output file for the report.

Layer Range: *Top Layer* *Bottom Layer*	Optional. The layer range checks for missing stacked vias between only bottom and top layers. It also checks for missing vias between all intermediate layer intersections. You can specify standard metal layer names, such as `(1)`, `(2)`, and so on, or metal layer names as defined in the LEF file. *Default*: All layers. If *Bottom Layer* is specified but *Top Layer* is not , it assumes one layer up.
Area: *Draw x1 y1 x2 y2*	When selected, enables you to draw a box in the display canvas to fill in *`x1 y1 x2 y2`* values automatically. Optionally, you can also specify *`x1 y1 x2 y2`* coordinates.
Include metal fill geometries	Specifies that metal fill should also be checked. *Default*: Metal fill will be ignored.
Include non-orthogonal wires	Specifies that non-orthogonal crossing wires should also be checked. *Default*: Non-orthogonal wires will be ignored.
Include wire-pin overlaps	Specifies that wire-pin overlaps should also be checked. *Default*: Wire-pin overlaps will be ignored.
Check stacked via	Checks for missing vias between all non-adjacent as well as adjacent layers. *Default*: Missing stacked vias will be ignored.
Check via utilization	Checks the via utilization.
Min via against overlapping metal area ratio	Specifies the minimum via area against overlapping metal geometry ratio. The value must be between `0` and `1`.
Keep Previous Setting	Specifies that all previous `verifyPowerVia` settings will be kept. *Default*: Previous settings are not kept.

Related Text Commands

`verifyPowerVia`

14

Pegasus Menu

Pegasus

If the Innovus software finds a Pegasus installation in your search path, a Pegasus pull-down menu appears on the Innovus toolbar. Using this menu, you can submit Pegasus Design Rule Check (DRC), Electrical Rule Check (ERC), Programmable Electrical Rule Check (PERC), Layout vs. Schematic (LVS), XOR (sometimes known as LVL - Layout vs. Layout), and FastXOR jobs, and then debug errors using the Pegasus debugging GUI within the Innovus environment.

For detailed information on Pegasus, see the following documents:

- *Cadence Pegasus User Guide*
- *Cadence Pegasus Developer Guide*

15

PVS Menu

Physical Verification System (PVS)

If the Innovus software finds a PVS installation in your search path, a PVS pull-down menu appears on the Innovus toolbar. Using this menu, you can submit PVS Design Rule Check (DRC), Electrical Rule Check (ERC), Programmable Electrical Rule Check (PERC), Layout vs. Schematic (LVS), XOR (sometimes known as LVL - Layout vs. Layout), and FastXOR jobs, and then debug errors using the PVS debugging GUI within the Innovus environment.

For detailed information on PVS, see the following documents:

- *Cadence Physical Verification System User Guide*
- *Cadence Physical Verification System Developer Guide*

16

Tools Menu

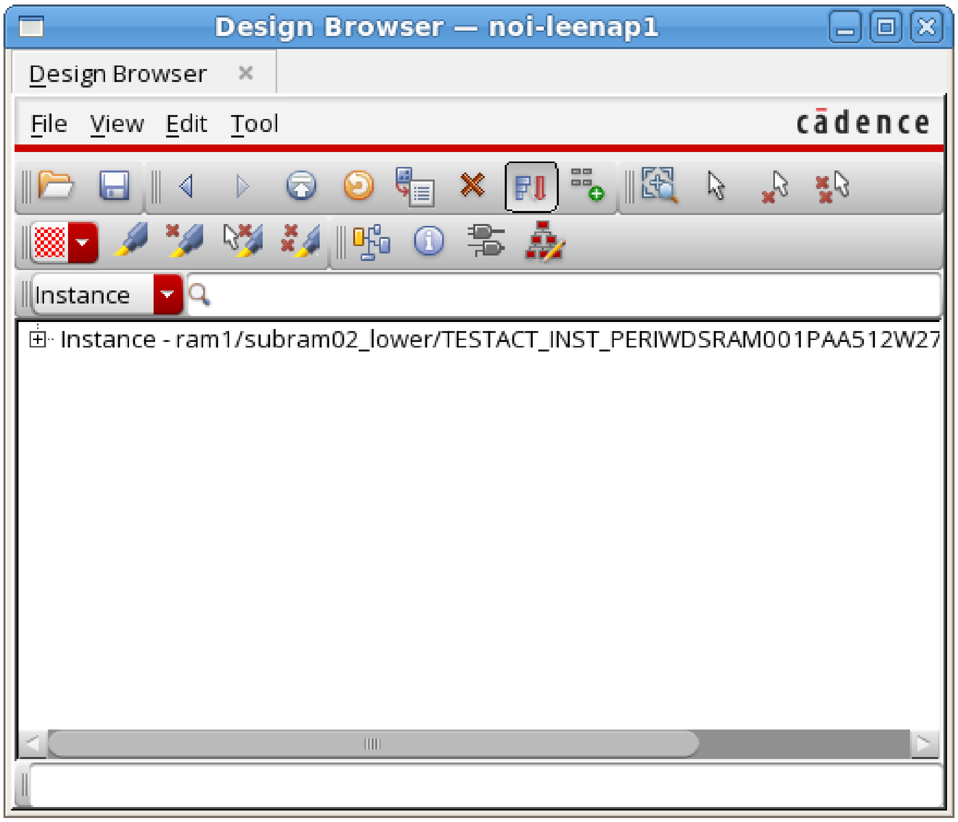
- Conformal Compare Constraints
- Conformal Derive Critical False Path
- Conformal Promote Constraints
- DFM
  - Litho Verify - Routing Layers
  - Litho Verify - Sign-Off
  - CMP Verify - Sign-Off
- Snapshot
  - Create Snapshot
  - View Snapshot
- Screen Capture
  - Write To GIF File
  - Screen Dump
  - Display Screen Dump
- Create Ruler
  - Create Ruler Preferences
- Clear All Rulers

Design Browser

Use the Design Browser to navigate through the chip's design hierarchy. You can use the Design Browser to view the design hierarchy tree at any time after the design is imported. The Design Browser also makes it easier to highlight specific modules, instances, or nets in the design display area.

You can use the widgets in the Design Browser to open forms to navigate through displays, and perform actions. From the Design Browser, you can access the Connectivity Browser to display the number of nets between instances, and the Attribute Editor to display an object's type, name, and attributes.

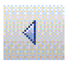
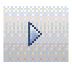
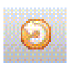
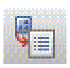
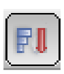
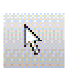
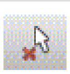
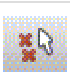
- Choose *Tools - Design Browser*, or click the Design Browser widget on the toolbar.

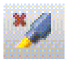
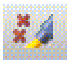
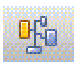
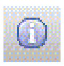
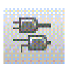
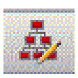


Note: If you select an object in the main window before opening Design Browser, the browser is automatically populated with the details of that object. If multiple objects are selected in the main window, Design Browser automatically displays details of all selected objects.

Design Browser Tool Widgets

You can use the widgets in the Design Browser to navigate through displays, open tools, make selections, and perform actions. The widgets are categorized into groups. You can right-click any empty space on the toolbars and choose which group of widgets to display.

File Widgets	
	*Load* - Displays the Load Design Browser File form, where you can enter the filename and the format of the placement file.
	*Save As* - Displays the Save Design Browser File form, where you can specify the filename. The recommended extension is `.dbf`.
View Widgets	
	*Previous Page* - Displays viewable data in a reverse direction.
	*Next Page* - Displays viewable data in a forward direction.
	*Top Page* - Returns to the top of the design.
	*Refresh* - Refreshes the Design Browser display.
	*Get Selected* - Gets the selected object and displays it in the Design Browser.
	*Delete Group/Group Member* - Deletes an individual instance from a user-defined group or an entire user-defined group.
	*Sort By Size* - Displays instances in the order of the number of cells in the instances. This toggle button is selected by default. Deselect this button to display instances sorted alphabetically by name.
	*Accumulate Results* - Traces the hierarchical path for the selected object in the design display area.
Select Widgets	
	*Zoom Selected* - Zooms in on the object (that you have selected in the Design Browser) in the design display area.
	*Select* - Selects an object in the design display area.
	*Deselect* - Deselects an object in the design display area.
	*Deselect All* - Deselects all objects in the design display area.
Highlight Widgets	
	*Edit Highlight Color* - Allows you to select a highlight color from the available choices in the drop-down menu.

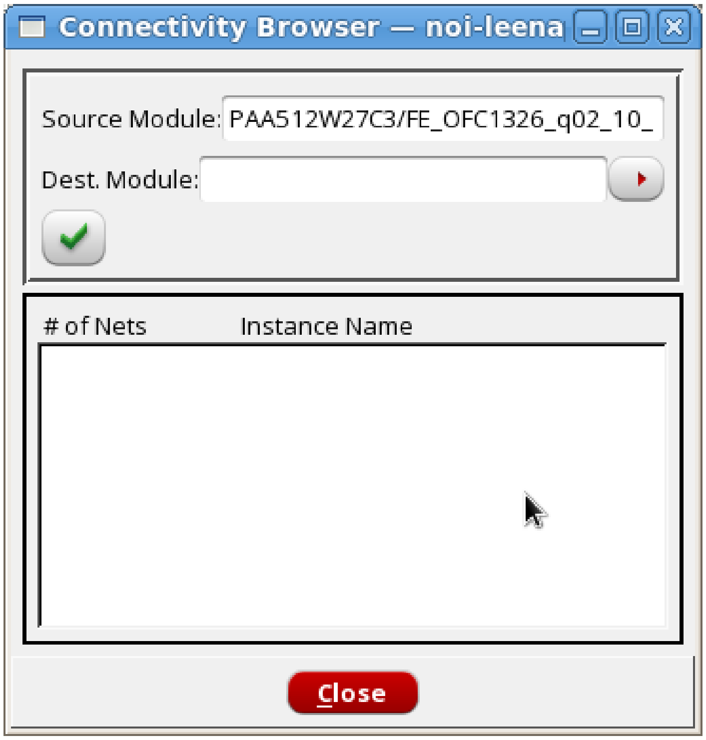
	*Highlight* - Highlights an object in the design display area.
	*Dehighlight* - Dehighlights an object in the design display area.
	*Dehighlight Selected* - Dehighlights the selected object.
	*Dehighlight All* - Dehighlights all objects in the design display area.
Tool Widgets	
	*Connectivity Browser* - Opens the Connectivity Browser. For more information, see Connectivity Browser.
	*Attribute Editor* - Opens the Attribute Editor for the selected object. For more information, see Attribute Editor in *Edit Menu* chapter of the *Menu Reference* .
	*Show Cone Schematic (New)* - Opens the Schematic Viewer to display schematic in flattened mode.
	*Show Module Schematic (New)* - Opens the Schematic Viewer to display schematic in hierarchical mode.
Find Bar	
	Enables you to search and display hierarchy information for the object you specify in the adjacent text input box. You can use wildcards to specify object names in the text input box. When you enter text in the text input box, the Clear button () is displayed next to the text input box. Use this button to clear any existing text in the input box. You can view information on the following object types: • *Instance*: Enables you to search for an instance and display its hierarchy in the Design Browser window. You can traverse to the next hierarchy by double-clicking on the instance name. Along with the instance name, the instance's cell type and number of cells are displayed. • *Net* : Enables you to search for a net and display its hierarchy in the Design Browser window. Double-clicking the net name displays the net connection. • *Group* : Enables you to search for an existing instance group and display its hierarchy in the Design Browser window. • *Cell*: Enables you to search for a cell and display its hierarchy in the Design Browser window.

State Bar	
	Displays the name of selected object on the bar at the bottom of the browser.

Connectivity Browser

Use the Connectivity Browser to display connections from a source module to a destination module, including module guides, blocks, I/O blocks, and standard cells.

1. Choose *Tools* - *Design Browser*, or click the *Design Browser* widget on the toolbar.
2. Highlight a module in the Design Browser and click the *Connectivity Browser* widget.



Connectivity Browser Fields and Options

Source Module Instance	Specify the name of the instance
Destination Module	Use this pull-down menu to select the destination module.
Check	Displays the connection information.

Set Mode

Use the *Set Mode* submenu in the *Tools* menu to access the following menu items:

- Mode Setup
- Specify Operating Condition/PVT...
- Specify Analysis Mode
- Set Timing Derate
- Set Interactive ECO Mode

Mode Setup

The Mode Setup form enables you to set global parameters for specific applications in the Innovus software. To access the Mode Setup form:

- Choose *Tools - Set Mode - Mode Setup*.

The Mode Setup form contains the following pages:

- Mode Setup - CTS
- Mode Setup - EarlyGlobalRoute
- Mode Setup - Filler
- Mode Setup - NanoRoute
- Mode Setup - OasisOut
- Mode Setup - Optimization
- Mode Setup - Placement
- Mode Setup - ScanReorder
- Mode Setup - StreamOut
- Mode Setup - TieHiLo

Mode Setup - CTS

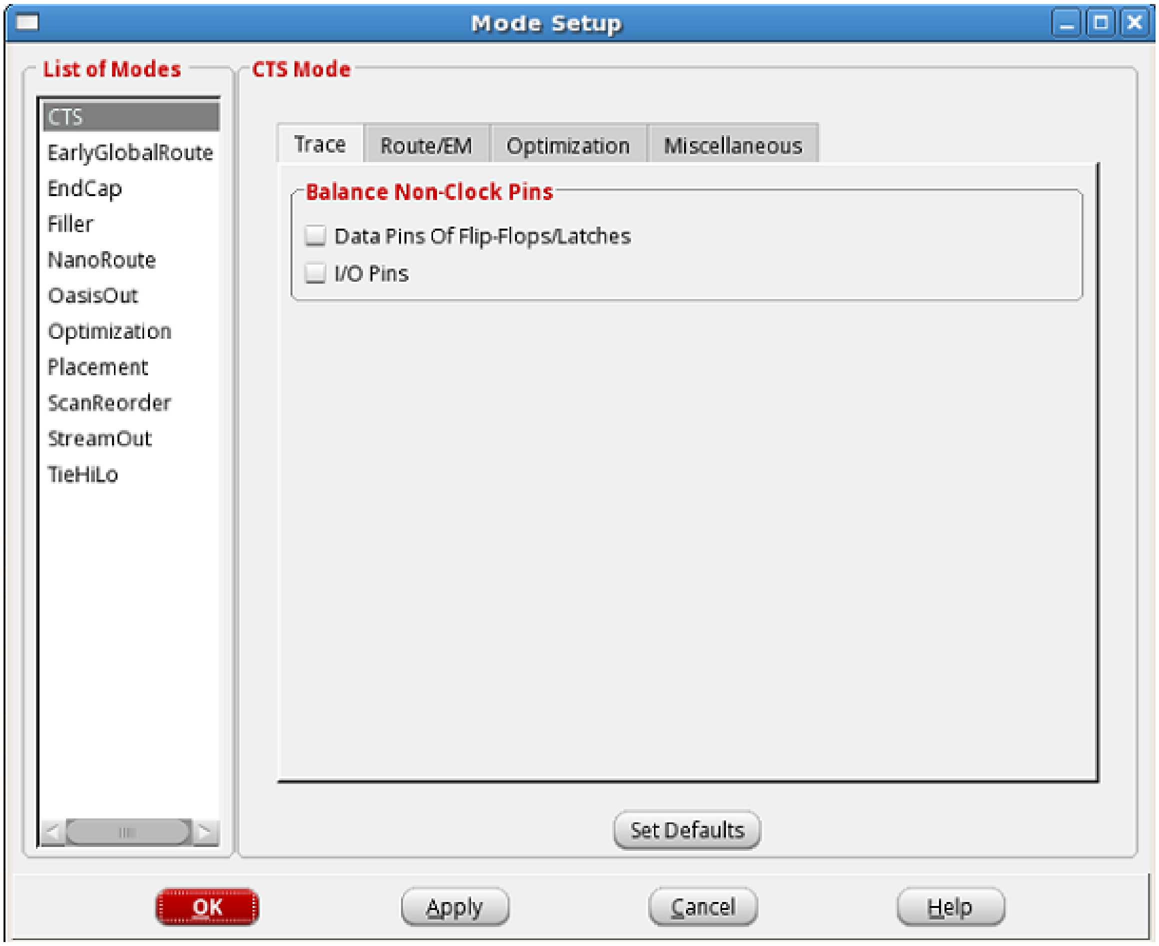
The Mode Setup - CTS page enables you to specify global parameters for performing clock tree synthesis (CTS).

The Mode Setup - CTS page contains the following subpages:

- CTS - Trace
- CTS - Route/EM
- CTS - Optimization
- CTS - Miscellaneous

CTS - Trace

Use the *Trace* page to specify how CTS should treat pins when tracing through the clock tree.
Choose *Tools - Set Mode - Mode Setup* and select *CTS*. The *Trace* page opens by default.



Fields and Options

Data Pins of Flip-Flop/Latches	
	Treats Data pins of flip-flops and latches as synchronous pins, instead of as excluded pins. Data pins include: • Data pins • Enable pins • Scan-in pins • Scan-enable pins • Synchronous set and reset pins *Default:* Off

I/O Pins	Treats I/O pins as synchronous pins, instead of as excluded pins. *Default:* Off

CTS - Route/EM

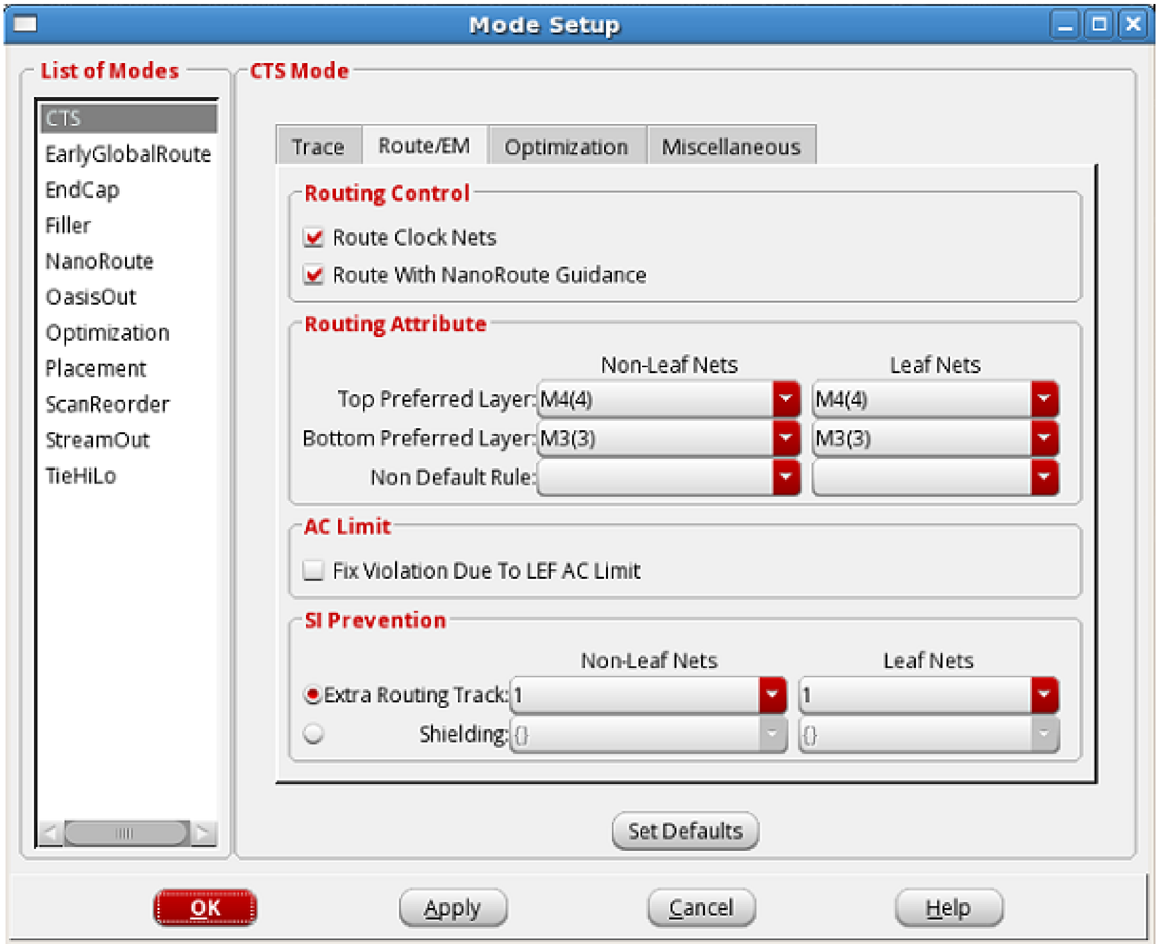
Use the *Route/EM* page to define routing attributes that CTS should use if no routing attribute section is specified for a clock tree in the clock tree specification file.

Note: CTS applies any routing constraints that you set using the *Route/EM* page globally to the design. However, any routing constraints that you set with the RouteType statement in the clock tree specification file take precedence over settings you make with this page.

Follow these general guidelines when you are considering routing constraints for your design:

- Use the RouteType statement in the clock tree specification file to set routing constraints on *particular clocks* in your design.
- Use the *Route/EM* page to set routing constraints on *all other* clocks in your design.

Choose *Tools* - *Set Mode* - *Mode Setup* and select *CTS*. Then, click the *Route/EM* tab.



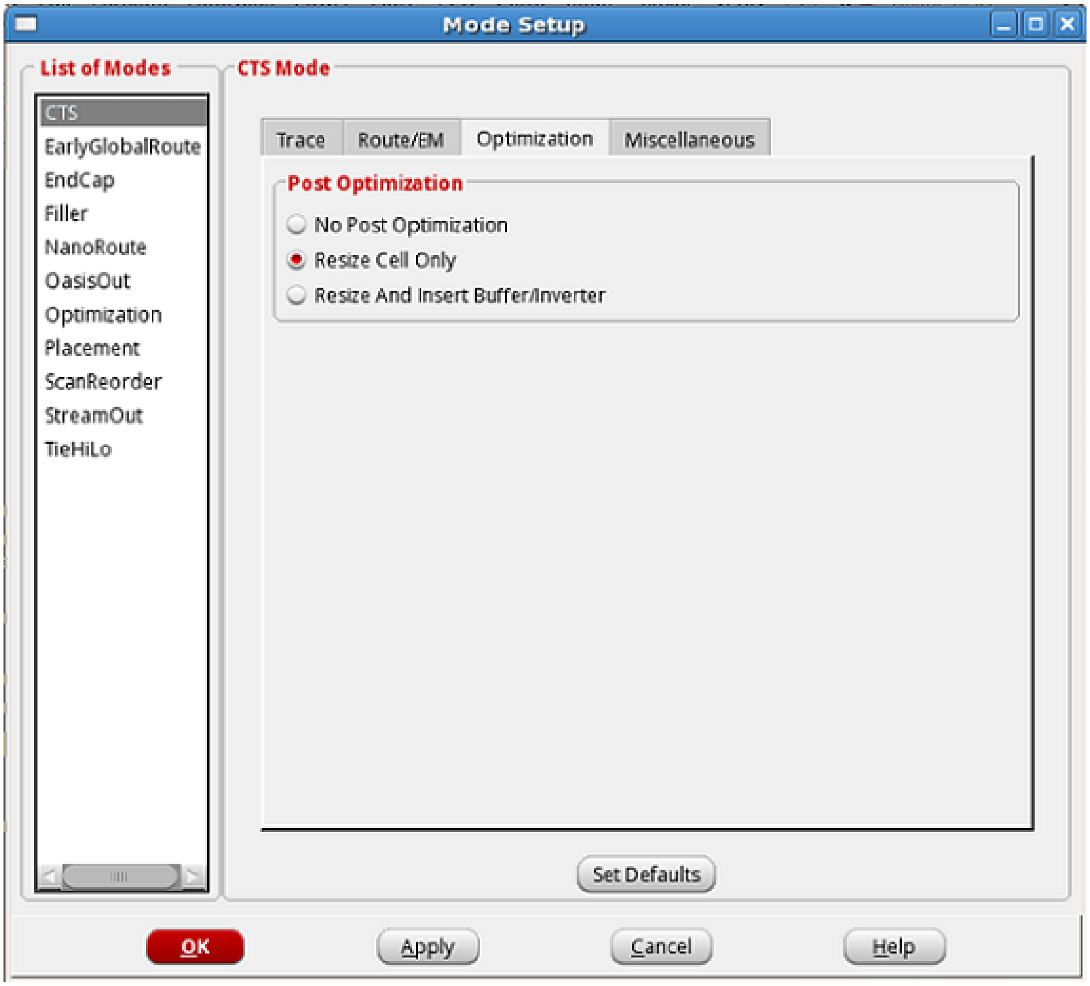
Fields and Options

Route Clock Nets	Routes clock nets. *Default:* Off
Route With NanoRoute Guidance	
	Specifies that Nanoroute should use the CTS-generated route guide file when routing clock nets. The route guide marks routable gcells for the trunk portion of the net, and provides a list of pins per clock net that should be connected first, to maintain a balanced route topology. **Note:** This option only takes effect if the *Route Clock Nets* option is selected. *Default:* On

Top Preferred Layer	Specifies the top preferred metal layer for routing non leaf-level nets and leaf-level nets. *Default:* 4
Bottom Preferred Layer	Specifies the bottom preferred metal layer for routing non leaf-level nets and leaf-level nets. *Default:* 3
Non default Rule	Specifies the LEF NONDEFAULTRULE statement that the router should use for routing non leaf-level nets and leaf-level nets. Default: {}
Fix Violation Due To LEF AC Limit	
	Attempts to minimize EM violations during synthesis by resizing or inserting buffers to enhance the electrical current flow through the wires. If any wire exceeds the library value, CTS reports the violation in the standard CTS report. **Note:** In order to perform EM analysis and optimization, your LEF file must contain an AC Limit table. You must also specify the Period statement in the clock specification file. *Default:* Off
Extra Routing Track	Specifies the extra space (in tracks) to add around clock wires, when routing non leaf-level nets and leaf-level nets. *Default:* 1
Shielding	Specifies the ground net for routing non leaf-level nets and leaf-level nets. *Default:* Off

CTS - Optimization

Use the *Optimization* page to specify how CTS should handle post clock tree synthesis optimization. Choose *Tools - Set Mode - Mode Setup* and select *CTS.* Then, select *Optimization*.

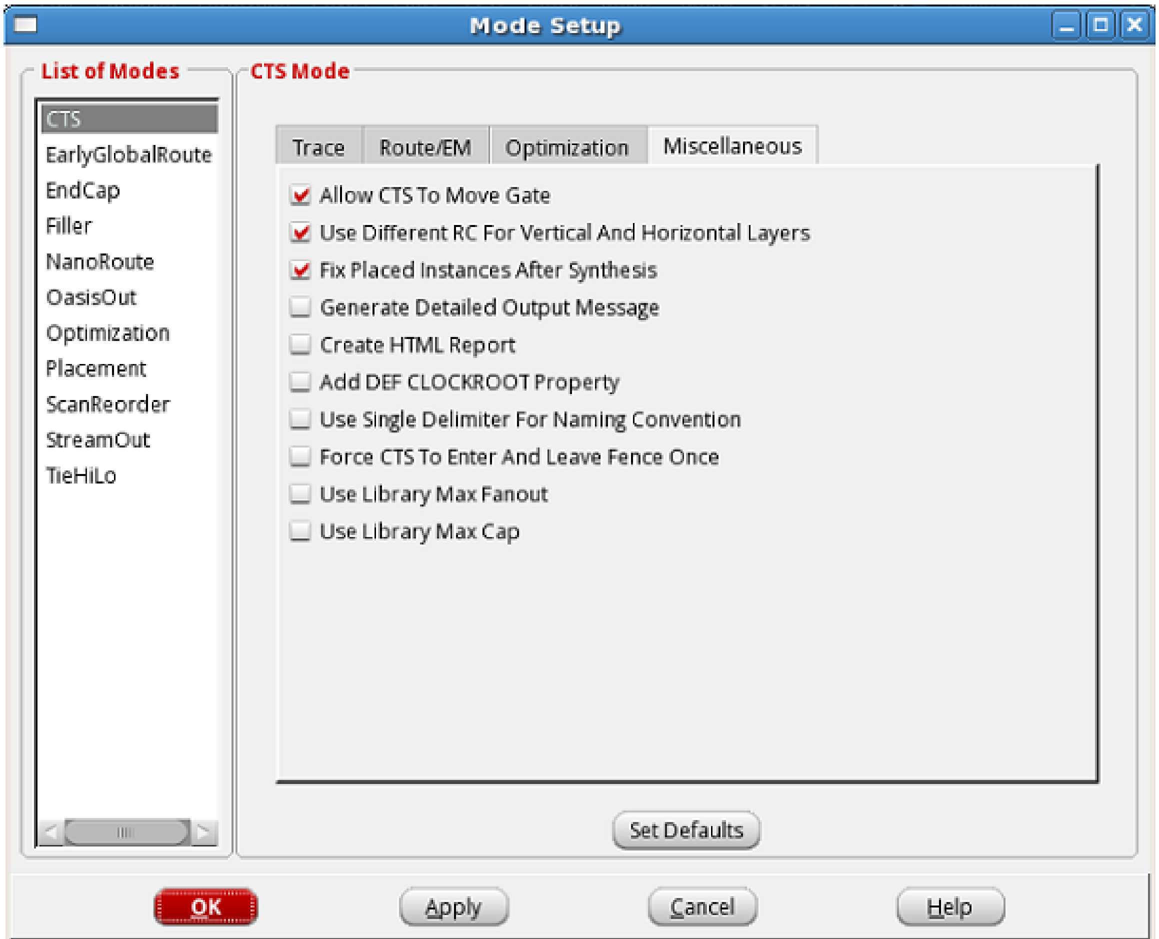


Fields and Options

No Post Optimization	Does not resize buffers or inverters, refine placement, or correct routing for signal and clock wires. *Default:* Off
Resize Cell Only	Resizes buffers or inverters only; the software does not refine placement or correct routing. *Default:* On
Resize And Insert Buffer/Inverter	
	Inserts and resizes buffers or inverters, refines placement, and corrects routing for signal and clock wires. *Default:* Off

CTS - Miscellaneous

Use the *Miscellaneous* page to set various other global parameters for CTS.
Choose *Tools - Set Mode - Mode Setup* and select *CTS.* Then, select *Miscellaneous*.



Fields and Options

Allow CTS To Move Gate	
	Moves driving gates during clock tree synthesis. *Default:* On
Use Different RC For Vertical And Horizontal Layers	

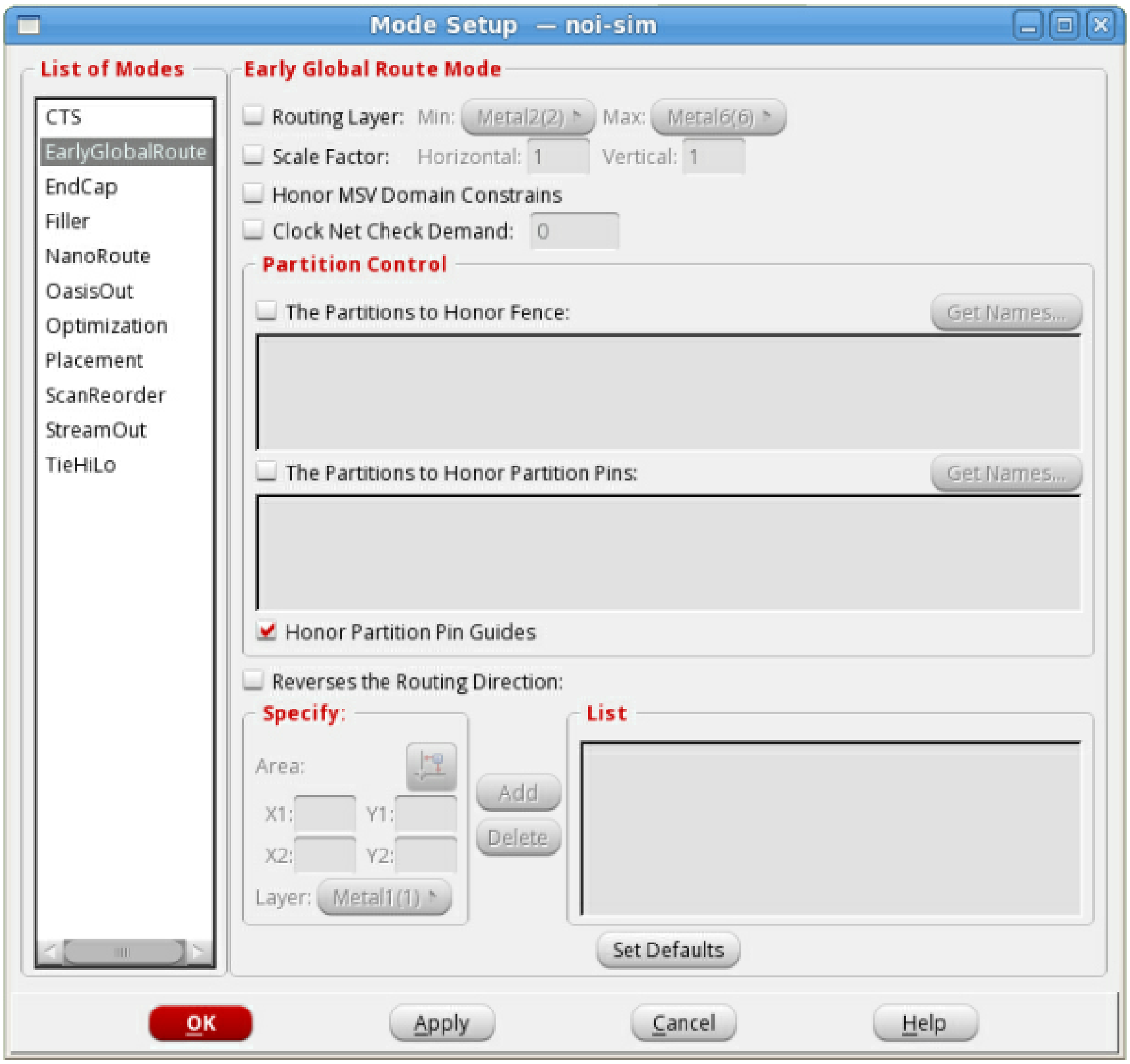
	Uses separate average RC values for horizontal and vertical layers. This is useful for when your design has very different R and C values for horizontal and vertical layers. *Default:* On
Fix Placed Instances After Synthesis	
	Changes the placement status of instances from PLACED to FIXED after clock tree synthesis. *Default:* On
Generate Detailed Output Message	
	Generates more detailed information in the Innovus console and the log files during CTS. *Default:* Off
Create HTML Report	Generates HTML versions of the CTS reports. *Default:* Off
Add DEF CLOCKROOT Property	
	Adds the CLOCKROOT property to each clock that CTS inserts in a design. *Default:* Off
Use Single Delimiter For Naming Convention	
	Uses single name delimiters after the first element in clock root and net names. CTS normally inserts double (or, in some cases, multiple) name delimiters after the first element of clock root or net names. If you select this option, CTS inserts a single underscore (_) in clock root and net names. *Default:* Off
Force CTS To Enter And Leave Fence Once	
	Forces CTS to enter only once into a fence in hierarchical designs. If you select this option, CTS will not enter into a fence more than once, and CTS will create only one clock port for each fence after partitioning. *Default:* Off
Use Library Max Fanout	

	Uses the maximum fanout limit specified in the timing library. If you do not select this option, the software uses the MaxFanout value from the clock tree specification file. If the clock tree spec file does not contain a MaxFanout value, the software uses a maximum fanout limit of 50. *Default:* Off
Use Library Max Cap	Uses the maximum capacitance values in the timing library for buffers, inverters, or gating cells. If you do not select this option, the software uses the MaxCap values from the clock tree specification file. *Default:* Off

Mode Setup - EarlyGlobalRoute

The Mode Setup - Early Global Route Mode page enables you to set global parameters for the Early Global Route program. Parameters that you specify with this form are then used automatically whenever you run Early Global Route, either explicitly through the `earlyGlobalRoute` command or Early Global Route form, or internally during in-place optimization, partitioning, or placement.

→ Choose *Tools - Set Mode - Mode Setup* and select *EarlyGlobalRoute* .



Fields and Options

Routing Layer	Select to specify the routing layer limits.	
	Min	Limits routing to layers at and above the specified layer. However, layers below the specified layer can still be used for routing if necessary, such as for short connections to pins. *Default:* Bottom-most layer

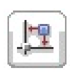
	Max	Limits routing to layers at and below the specified layer. All metal layers above the specified metal number are not routed. *Default:* Top-most layer
Scale Factor	Select to specify the scale factor values.	
	Horizontal	Scale the horizontal track supply by the specified value. *Default* : `1`
	Vertical	Scales the vertical track supply by the specified value *Default*: `1`
Honor MSV Domain Constrains	Honors MSV domain constraints. Select this option to enable Early Global Route to honor power domain settings. By default, Early Global Route ignores the power domain settings and routes as flat design. When enabled, Early Global Route honors power domain settings and routes wires inside preferred power domain as much as possible.	
Clock Net Check Demand	Select to specify the special width for clock wires. *Default*: `0`	
The Partitions to Honor Fence	Select to honor partition fences with a single-entry constraint and also honor fixed pins. Under the single-entry constraint once a hierarchical route enters a partition fence it does not cross the boundary again. The *Partitions to Honor Fence* option routes a net belonging to more than one partition so that the routing does not violate partition boundaries, in addition to routing intra-partition and global nets using the specifications of the partitions. For example, if a net belongs to partitions `P1` and `P3`, but not `P2`, the net is routed without going over the `P2` partition boundary. Click *Get Name* to display the *Get Partitions* form that enables you to specify the list of partitions. **Notes:** • Supports designs with up to 180 partitions. • Early Global Route supports nested partitions. *Default* : ""	

<table>
<tr><td>The Partitions to Honor Partition Pins</td><td colspan="2">Select to honor partition fences with single-entry constraint and pre-assigned pins (pins marked <code>FIXED</code>) and assigned pins (pins marked <code>PLACED</code>).

Click Get Name to display the Get Partitions form that enables you to specify the list of partitions.

Default: ""</td></tr>
<tr><td>Honor Partition Pin Guides</td><td colspan="2">Select to honor partition pin guides. It uses the pin guide statements in the floorplan file to guide the routing through partition pin points.
Note: Fixed pins and pin guides are only honored when this option is enabled.</td></tr>
<tr><td>Reverses the Routing Direction</td><td colspan="2">Reverses the routing direction in the given area on the specified layer-range. It specifies an Area in which Early Global Route routes wires in the non-preferred direction.

Note: You can define the reverse direction routing area by <code>“(x1 y1 x2 y2)”</code> and routing layer by <code>“Metal2:Metal2”</code> . The Early Global Router only supports a single layer with this option. Consequently, <code>“Metal2:Metal3”</code> is not supported. The <code>-reverseDirection</code> parameter only has impact on the congestion value calculation. By routing on reverse direction, you can reduce the routing capacity on the specified layer and add extract resource on the above and below layers.
Innovus does not display the routing wires in reverse direction routing region.</td></tr>
<tr><td></td><td>Area</td><td>Specify the reverse direction routing area coordinates in the x1, y1, x2, y2 boxes.

Alternatively, click the  button to draw a rectangle to specify area. It automatically populates the x1 , y1 , x2 , and y2 boxes with the coordinates of the rectangle you draw on the main window.</td></tr>
<tr><td></td><td>Layer</td><td>Specify the routing layer.

Note: The Early Global Router only supports a single layer with this option. Consequently, <code>“Metal2:Metal3”</code> is not supported.</td></tr>
<tr><td></td><td>Add</td><td>Click to add a selected area to the reverse routing direction list.</td></tr>
<tr><td></td><td>Delete</td><td>Click to delete a selected area from the reverse routing direction list.</td></tr>
<tr><td>Set Defaults</td><td colspan="2">Sets the default values of all the options.</td></tr>
</table>

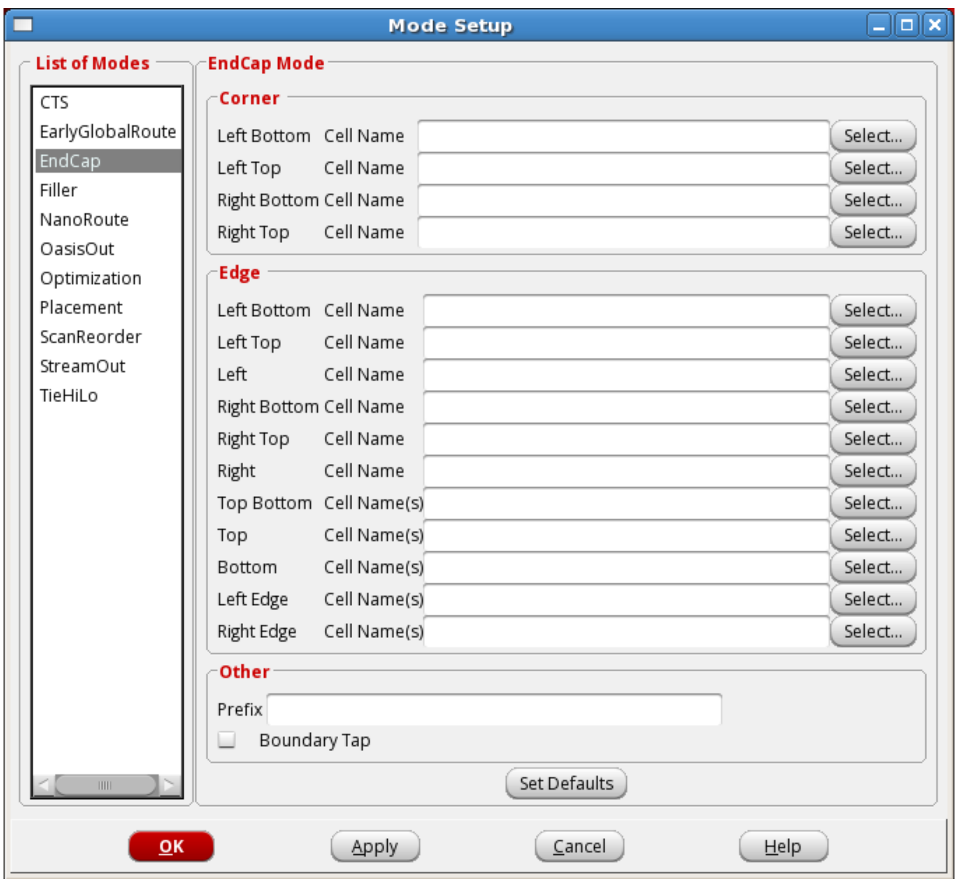
Related Text Commands

- `setRouteMode`
- `earlyGlobalRoute`

Mode Setup - EndCap

Use the *Mode Setup - EndCap* page to specify options for end-cap or triple-well cap insertion.

- Choose *Tools - Set Mode - Mode Setup* and select *EndCap*.



Fields and Options

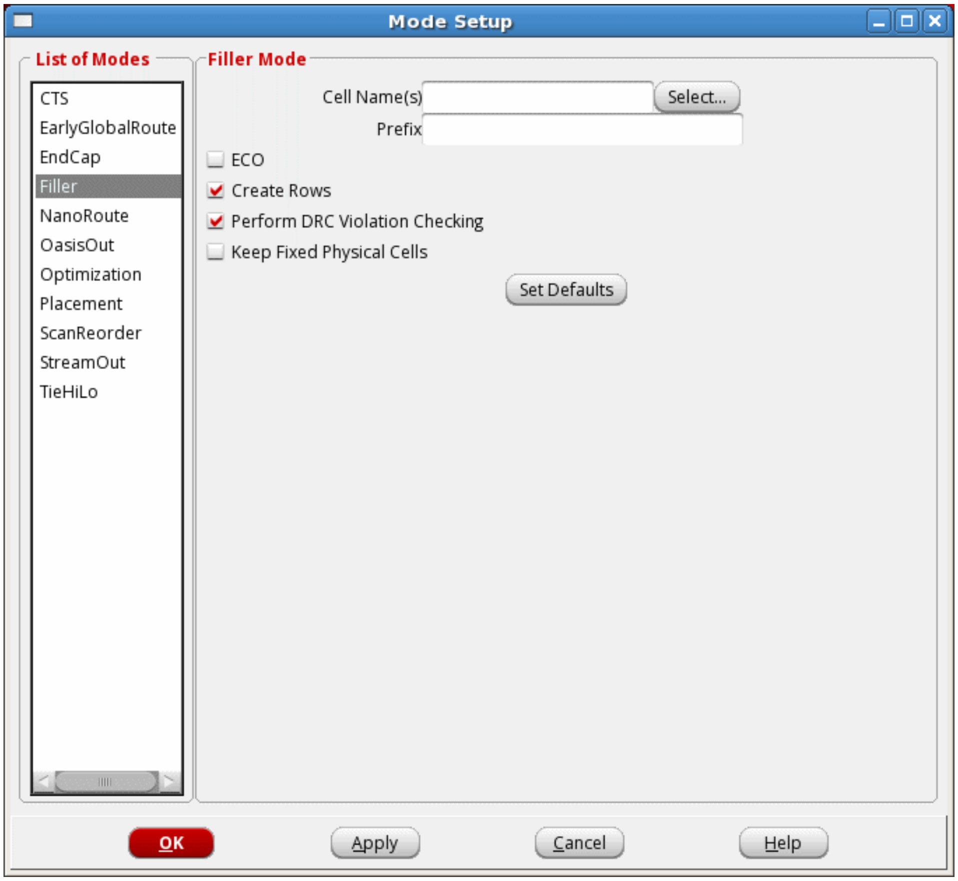
Corner	
Left Bottom Cell Name	Specifies the cell which has n-well cap on its left-bottom corner when in R0 orientation. These cells are added on inner corners of core or concave corner of a rectilinear hard macro.
Left Top Cell Name	Specifies the cell that has n-well cap on its left top corner when in R0 orientation. Therefore, this cell is added on inner corners of core or concave corner of a rectilinear hard macro.
Right Bottom Cell Name	Specifies the cell that has n-well cap on its right bottom corner when in R0 orientation. Therefore, this cell is added on inner corners of core or concave corner of a rectilinear hard macro.
Right Top Cell Name	Specifies the cell that has n-well cap on their right top corner when in R0 orientation. Therefore, this cell, in R0, is added on right corner of core or concave corner of a rectilinear hard macro.
Edge	
Left Bottom Cell Name	Specifies the one cell that has n-well cap on its left-bottom edge when in R0 orientation. Therefore, this cell, in R0 orientation, can be used to cap a row ending at left-bottom convex corner of a hard macro or rectilinear core. If this cell is allowed to flip in Y, it can be used on MY rows that end in left-top convex corner. With both X and Y symmetry, it can cap all convex corners, though only R0 rows at bottom, and MY rows for top corners.
Left Top Cell Name	Specifies the cell that has n-well cap on its top-left edge when in R0 orientation. Therefore, in R0 orient, it is the flipped-in-Y version of left-bottom edge cell.
Left	Specifies the one cell that has n-well cap on its left edge when in R0 orientation. Therefore, this cell is used to cap right edge of the core rows, or rows ending at left edge of a hard macro. This would be same as a post-cap, in a two well process.
Right Bottom Cell Name	Specifies the cell that has n-well cap on its right bottom edge when in R0 orientation. Therefore, these cells are the flipped-in-X version of leftBottomEdge cell. Usually one of these two is sufficient for a library.
Right Top Cell Name	Specifies the cell that has n-well cap on its right top edge when in R0 orientation. Therefore, this cell is the R180 version of leftBottomEdge.
Right	Specifies the cell that has n-well cap on its right edge when in R0 orientation. Therefore, these cells are used to cap the left edge of the core-rows in R0.

Top Bottom Cell Name(s)	Specifies the cell that has an n-well cap on its top edge as well as bottom edge when in R0 orientation.
Top Cell Name(s)	Specifies the list of cells that have n-well cap on their top edge when in R0 orientation. Therefore, these cells are used to cap the bottom-core row or row at top of a hard macro.
Bottom Cell Name(s)	Specifies the list of cells that have n-well cap on their bottom-edge when in R0 orientation. Therefore, these cells are used to cap a top-core row, or row at the bottom of a hard macro.
Left Edge Cell Name(s)	Specifies the one cell that has n-well cap on its left edge when in R0 orientation. Therefore, this cell is used to cap right edge of the core rows, or rows ending at left edge of a hard macro.
Right Edge Cell Name(s)	Specifies the cell that has n-well cap on its right edge when in R0 orientation. Therefore, these cells are used to cap the left edge of the core-rows in R0.
Other	
Prefix	Adds prefix of EndCap cells.
Boundary Tap	Specifies the boundary tap.
Set Defaults	Sets the default values of all the options.

Mode Setup - Filler

Use the *Mode Setup - Filler* page to specify options for adding filler cells.

- Choose *Tools - Set Mode - Mode Setup* and select *Filler*.


Mode Setup
List of Modes
CTS
EarlyGlobalRoute
EndCap
Filler
NanoRoute
OasisOut
Optimization
Placement
ScanReorder
StreamOut
TieHiLo
Filler Mode
Cell Name(s)
Select...
Prefix
ECO
Create Rows
Perform DRC Violation Checking
Keep Fixed Physical Cells
Set Defaults
OK
Apply
Cancel
Help

Fields and Options

Cell Name(s)	Specifies the filler cells to add.z *Default:* "" (empty string)
Prefix	Specifies the prefix for the added filler cells. *Default:* FILLER
Create Rows	Creates rows in the floor plan. By default, if a cell's site does not have rows in the floor plan, addFiller creates the rows. *Default:* Selected
Perform DRC Violation Checking	
	When Add Filler is called after routing, instructs the software to run DRC checks of filler pins with signal net wires. *Default:* Selected
Fill Boundary	Fills the space between the ending standard cell and the core area (box). If this option is not selected, the software adds filler cells between the standard cell instances only. *Default:* Selected
Keep Fixed Physical Cells	
	Keeps filler cells marked FIXED in the database. *Default:* End-cap and well-tap cells are marked FIXED, and deleteFiller can delete them.
Set Defaults	Restores all the values of the options on this page to their default values.

Mode Setup - NanoRoute

The *Mode Setup - NanoRoute* page enables you to specify global parameters for the NanoRoute® router.

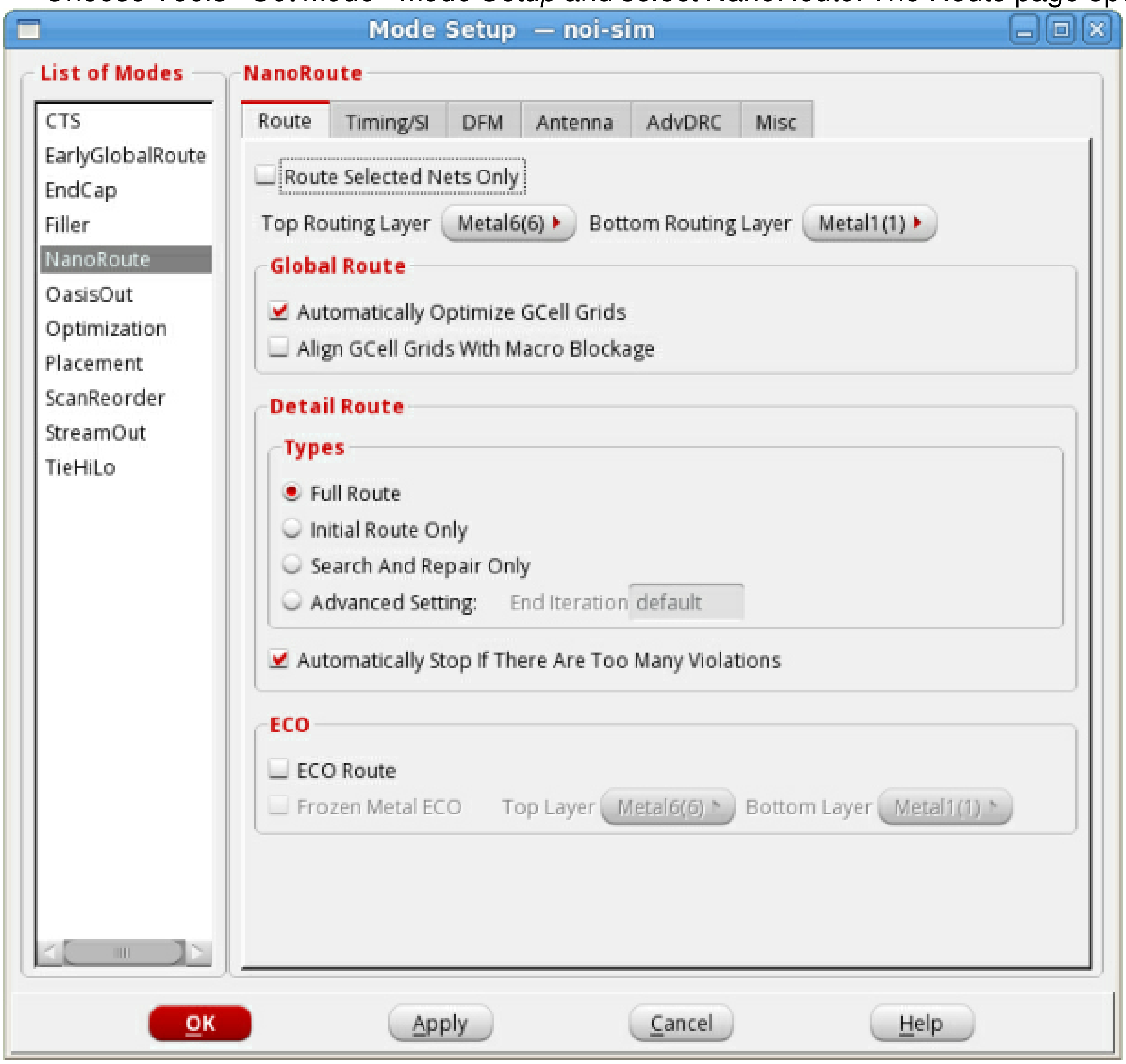
The *Mode Setup - NanoRoute* page contains the following subpages:

- NanoRoute - Route
- NanoRoute - Timing/SI

- NanoRoute - DFM
- NanoRoute - Antenna
- NanoRoute - AdvDRC
- NanoRoute - Misc

NanoRoute - Route

Use the *Route* page to specify options for global, detailed, and ECO routing.
→ Choose *Tools - Set Mode - Mode Setup* and select *NanoRoute.* The *Route* page opens by default.



Fields and Options

Route Selected Nets Only	
	Specifies whether NanoRoute routes all nets at once or routes selected nets only. To route critical nets as short as possible, select the critical nets and select this option. When this option is selected, NanoRoute does the following: • Removes incomplete nets unless they are marked + FIXED or have a -skip_routing net attribute. • Routes the remaining selected nets. *Default:* Off
Top Routing Layer	
	Specifies the highest layer the router uses for global and detailed routing. This option sets a hard limit, that is, NanoRoute does not route nets above the specified layer. **Note:** To set a soft limit, use the *Top Layer* attribute. *Default:* The number of the highest routing layer specified in the LEF LAYER (Routing) statement.
Bottom Routing Layer	
	Specifies the lowest layer the router uses for global and detailed routing. If the design has pins below the layer specified by this parameter, and if the tracks for the in-between layers are aligned to allow stacked vias to be dropped directly on top of the pins, the router uses stacked vias. However, if the tracks are not aligned, the router adds a short piece of wire before dropping a via to go to the next layer. **Note:** To set a soft limit, use the *Bottom Layer* attribute. *Default: Metal1*
Automatically Optimize GCell Grids	
	Overwrites the GCELLGRID defined in the DEF file with a grid that is optimized for the NanoRoute router. Selecting this option helps resolve congestion and over-the-macro violations if you see routability issues due to hot spots. *Default:* On
Align GCell Grids With Macro Blockage	

	Generates global routing cells (gcells) aligned to blockages in macros. Select this option prior to global routing, to improve the alignment of gcells with pins. *Default:* Off	
Full Route	Runs all detailed routing steps. *Default:* On	
Initial Route Only		
	Runs initial detailed routing only. During initial detailed routing, the router builds the detailed routing database. *Default:* Off	
Search And Repair Only		
	Runs a search-and-repair step. During search and repair, the router locates shorts and spacing violations and reroutes the affected areas to eliminate as many of the violations as possible. You must have already run detailed routing in order to run search-and-repair. *Default:* Off	
Advanced Setting		
	Divides detailed routing into intermediate steps. *Default:* Off	
	End Iteration	Specifies the last pass in a detailed routing step or the beginning of postroute optimization. **Note:** Setting *End Iteration* to a value higher than 20 generally does not improve results. *Default:* default
Automatically Stop If There Are Too Many Violations		
	Controls whether NanoRoute continues routing if there are many violations. In highly congested designs, NanoRoute stops if the number of violations is too high. If you deselect this option, NanoRoute continues routing until there is no improvement. By default, this option is selected. *Default:* On	

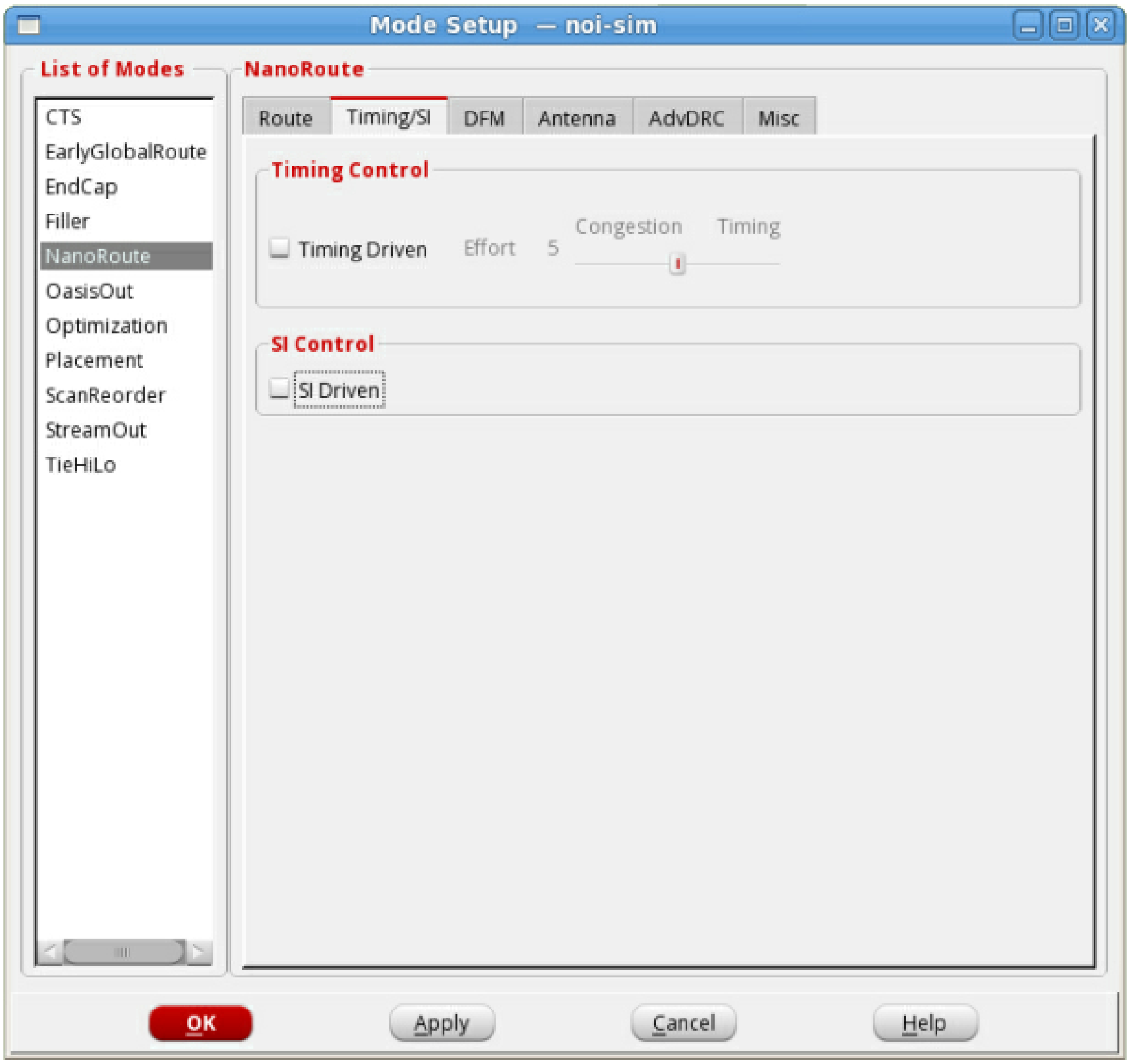
Elapsed Time Limit	Specifies a run-time limit for detailed routing. The time-limit is based on the elapsed time (the wall-clock time), not the CPU time. If the router reaches the limit during initial routing iteration, it stops when it finishes the routing iteration and keeps the routing result. If it reaches the limit during search and repair or postroute optimization, it stops immediately and keeps the routing result at that time. *Default:* 0 (no time limit)	
ECO Route	Specifies engineering change order (ECO) mode. During ECO mode, NanoRoute completes partial routes with added logic, while maintaining the existing wire segments as much as possible. **Note:** Select *ECO Route* only if you are running both global and detailed routing. *Default:* Off	
Frozen Metal ECO		
	Specifies the routing layers for ECO routing. Routing on all other layers is frozen. *Default:* Off	
	Top Layer	Specifies the top routing layer.
	Bottom Layer	Specifies the bottom routing layer.

Related Text Commands

- getNanoRouteMode
- setNanoRouteMode

NanoRoute - Timing/SI

Use the *Timing/SI* page to specify options for timing-driven routing and signal-integrity-driven routing, and signal integrity repair.
→ Choose *Tools - Set Mode - Mode Setup* and select *NanoRoute.* Then, select *Timing/SI*.


Mode Setup — noi-sim
List of Modes
CTS
EarlyGlobalRoute
EndCap
Filler
NanoRoute
OasisOut
Optimization
Placement
ScanReorder
StreamOut
TieHiLo
NanoRoute
Route
Timing/SI
DFM
Antenna
AdvDRC
Misc
Timing Control
Timing Driven
Effort
5
Congestion
Timing
SI Control
SI Driven
OK
Apply
Cancel
Help

Fields and Options

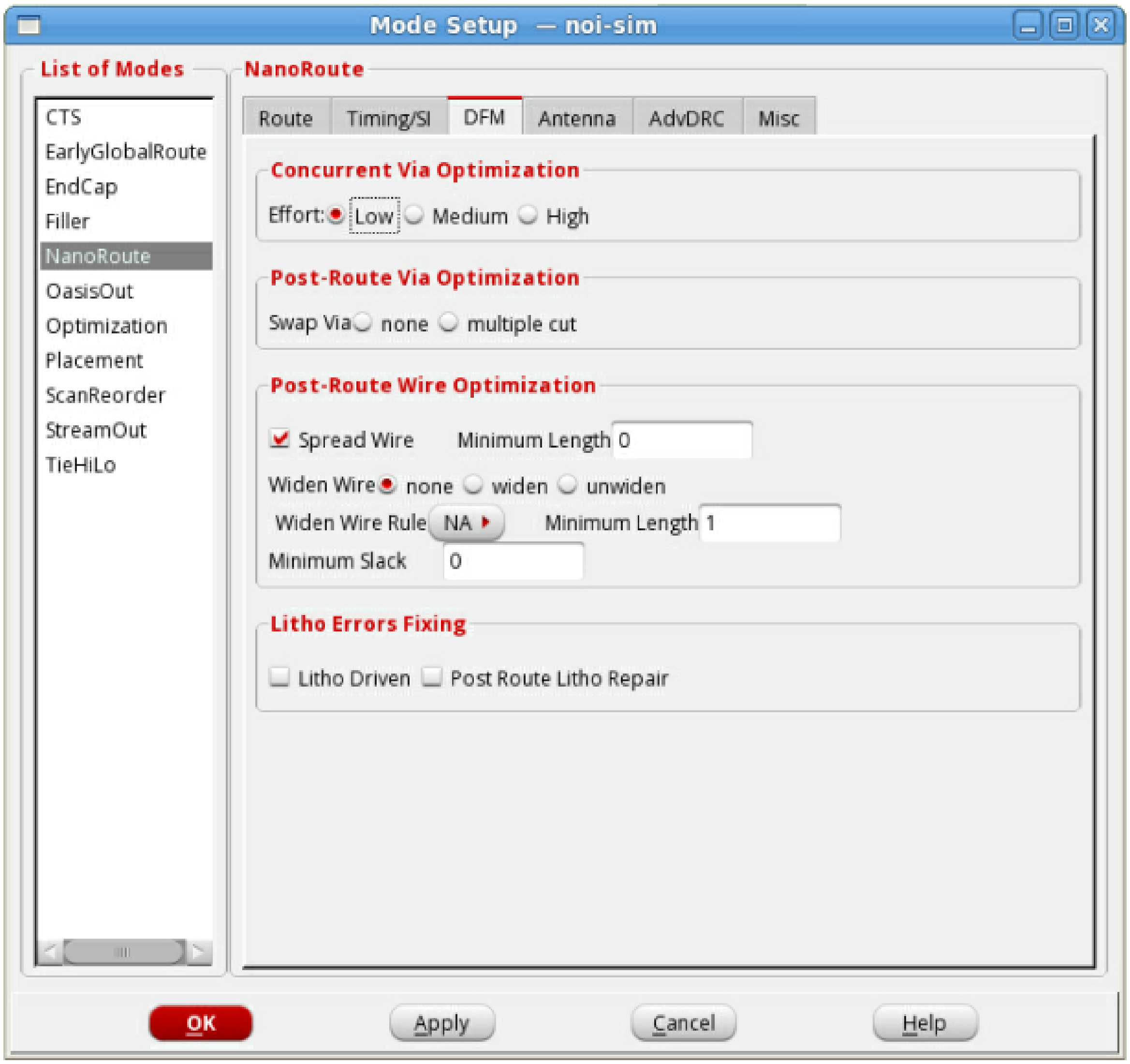
<table>
<tr><td colspan="3">Timing Driven</td></tr>
<tr><td></td><td colspan="2">Minimizes timing violations by analyzing the timing slack for each path, the drive strengths of each cell in the library, and the maximum capacitance and maximum transition limits. During timing-driven routing, NanoRoute routes multi-pin nets to the most critical sink first, performs wire optimization by reducing resistance and coupling, and continually adjusts detouring.
Default: Off</td></tr>
<tr><td></td><td>Effort</td><td>Specifies how aggressively the router works to meet timing constraints. A higher value increases the effort toward meeting timing constraints and decreases the effort toward relieving congestion.
Range: 0 - 10</td></tr>
<tr><td>SI Driven</td><td colspan="2">Prevents or reduces crosstalk. Works in conjunction with timing-driven routing.
When Timing Driven is selected, uses SMART routing to identify victim nets and minimize crosstalk by wire spacing, layer hopping, net ordering, and minimizing the use of long parallel wires.
When Timing Driven is not selected, uses an older signal integrity engine to identify victim nets and minimize crosstalk by preventing or reducing the use of long parallel wires.
Default: Off</td></tr>
</table>

Related Text Commands

- `getNanoRouteMode`
- `setNanoRouteMode`

NanoRoute - DFM

Use the *DFM* page to set via optimization options.
→ Choose *Tools - Set Mode - Mode Setup* and select *NanoRoute.* Then, select *DFM*.



Fields and Options

Effort	Specifies the effort level toward increasing the ratio of double-cut vias to single-cut vias concurrently with routing. Increasing the effort level increases the double-cut via ratio and decreases the total number of vias in the design, which means that it also decreases the number of single-cut vias.	
	Low	Specifies normal routing, so the router uses single-cut vias only. *Default:* On

	Medium	Balances the need for a high double-cut via ratio with run time and congestion. Specifying this parameter increases the run time somewhat compared with the low parameter. The router inserts some double-cut vias, although not as many as if the high parameter were specified. *Default:* Off
	High	Specifies the highest yield possible for vias, as the router puts its best effort toward achieving the highest possible double-cut via ratio at the expense of run time and congestion. *Default:* Off
Swap Via	Swaps single-cut vias for multiple-cut vias or reverses swapping on critical nets in a fully routed design, so that multiple-cut vias are swapped for single-cut vias on those nets. Does not swap multiple-cut vias in nondefault rule routing. A net with a pin on a critical path is considered a critical net if the pin slack, plus the value specified for *Minimum Slack*, is less than or equal to 0. *Default: none*	
	none	Does not swap vias.
	multiple cut	Replaces single-cut vias with multiple-cut vias in a fully routed design without regard to timing.
Spread Wire	Turns on postroute wire spreading. Type the minimum length for wires to move in the text box next to *Minimum Length*. The router moves the wires without moving the vias. Specifying true for this parameter might increase the overall routing run time but helps avoid yield lost caused by shorts. *Default:* Off	
	Minimum Length	
		Specifies the minimum length for wires to move during wire spreading.
Widen Wire	Turns on postroute wire widening. Selecting this option might increase the overall routing run time, but helps avoid yield loss caused by opens. Select the nondefault rule for widening wires in the text box next to *Widen Wire Rule*. *Default:* Off	
	none	Turns off this option.
	widen	Turns on postroute wire widening.
	unwiden	Turns off postroute wire widening.

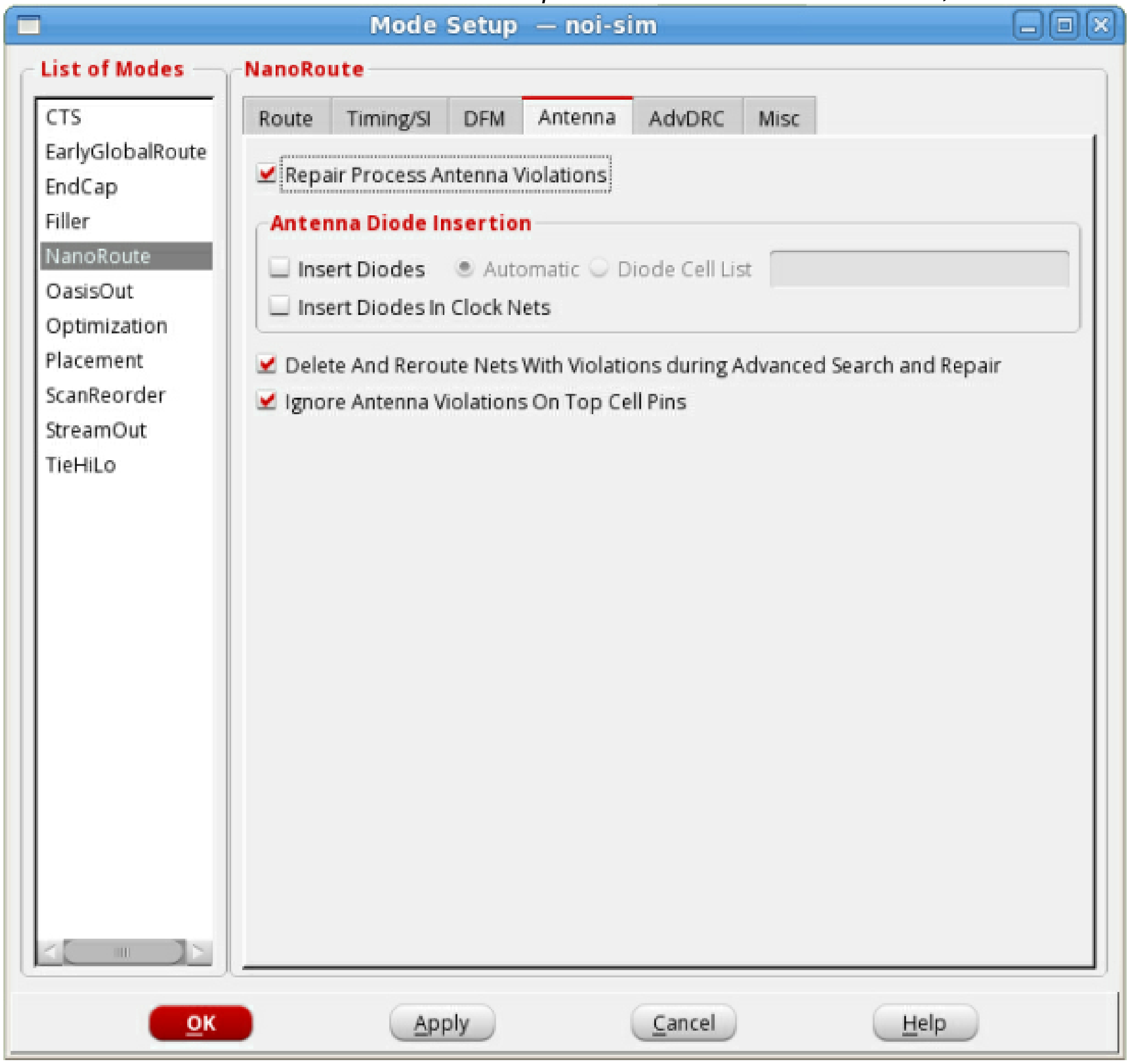
Widen Wire Rule	Specifies the nondefault rule for widening wires. The rule is specified in the LEF file.	
	Minimum Length	
		Specifies the minimum length in microns for a wire segment of a net before the segment is a candidate for widening. Wires are widened by an amount defined by a nondefault rule. They are not widened unless they meeting the following criteria: • Timing is not adversely affected • Routing resources are available • No overflow is created • No design rule or process antenna violations are created Widening wires helps avoid design rule violations, signal integrity problems, and yield loss.
Minimum Slack	Specifies the minimum slack on pins associated with nets that are candidates for wire spreading or wire widening. Using this parameter reduces the timing impact of wire spreading, wire widening, and via swapping, and helps reduce congestion and the yield loss due to shorts and opens.	
Litho Errors Fixing	Select one or both of the following options to minimize lithography problems.	
Litho Driven	Avoids lithography problems during routing by avoiding certain routing patterns that might lead to the creation of lithography hotspots. *Default:* Off	
Post Route Litho Repair		
	Corrects bridging, necking, and line-end shortening problems caused by lithography. Prior to running the router with this parameter, import a hotspot interface format (HIF file) with the `loadViolationReport` command or by using the Load Violation Report form.	

Related Text Commands

- `getNanoRouteMode`
- `setNanoRouteMode`

NanoRoute - Antenna

Use the *Antenna* page to specify when and how to repair process antenna violations.
→ Choose *Tools - Set Mode - Mode Setup* and select *NanoRoute.* Then, select *Antenna*.



Fields and Options

<table>
<tr><td colspan="3">Repair Process Antenna Violations</td></tr>
<tr><td></td><td colspan="2">Repairs process antenna violations by jumping layers (antenna stapling). The router repairs process antenna violations if it can do so without creating DRC violations. The router might need to make several passes before repairing all antenna violations.

Default: On</td></tr>
<tr><td>Insert Diodes</td><td colspan="2">Inserts and places antenna diode cells during postroute optimization if there are available placement locations for the cells. By default, NanoRoute repairs antenna violations by changing layers (also called antenna stapling or layer hopping), but it can also repair antenna violations by inserting diodes as close as possible to input gates to discharge current.

Default: Off</td></tr>
<tr><td></td><td>Automatic</td><td>searches the LEF file and inserts the first MACRO with CLASS CORE ANTENNACELL it finds with the appropriate SITE definition.

Default: On</td></tr>
<tr><td></td><td>Diode Cell List</td><td>Routes antenna diode cells with the specified name during postroute optimization. The antenna diode cells must have the same LEF SITE definition as the standard cells.

Default: Off</td></tr>
<tr><td colspan="3">Insert Diodes In Clock Nets</td></tr>
<tr><td></td><td colspan="2">Inserts diodes to repair process antenna violations on clock nets that are in the regular net section of the DEF file.

Default: Off</td></tr>
<tr><td colspan="3">Delete And Reroute Nets With Violations during Advanced Search and Repair</td></tr>
<tr><td></td><td colspan="2">Deletes and reroutes nets with process antenna violations. This option is not enabled if you are using LEF 5.3 or older, or if the design has more than 100 DRC violations.

Default: On</td></tr>
<tr><td colspan="3">Ignore Antenna Violations On Top Cell Pins</td></tr>
<tr><td></td><td colspan="2">Ignores antenna violations on top-level I/O block pins, but repairs antenna violations elsewhere. Do not select this option when you route a block whose top level is going to have diodes inserted.

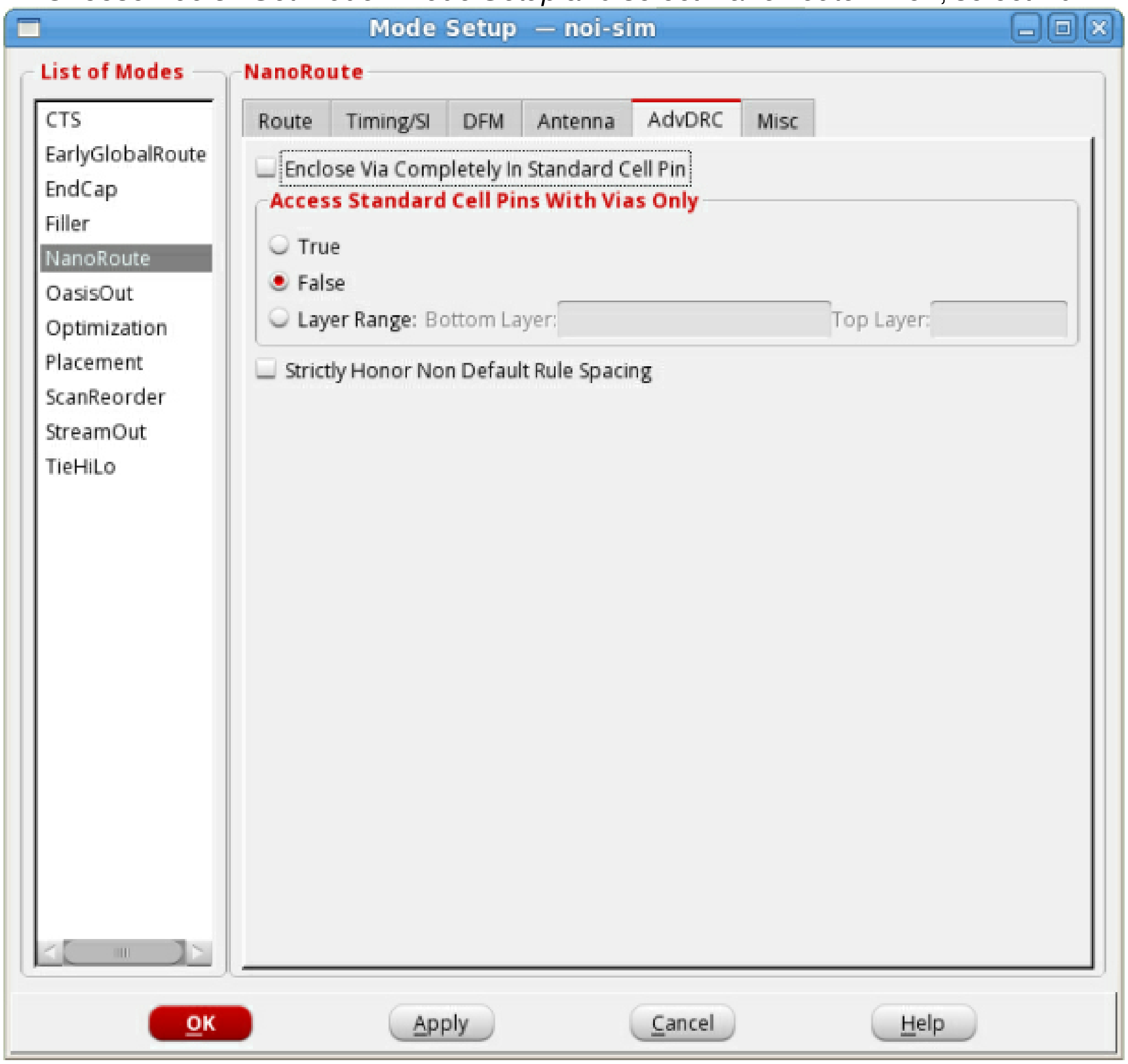
Default: On</td></tr>
</table>

Related Text Commands

- getNanoRouteMode
- setNanoRouteMode

NanoRoute - AdvDRC

Use the *AdvDRC* page to specify advanced options for checking design rules.
→ Choose *Tools - Set Mode - Mode Setup* and select *NanoRoute.* Then, select *AdvDRC*.



Fields and Options

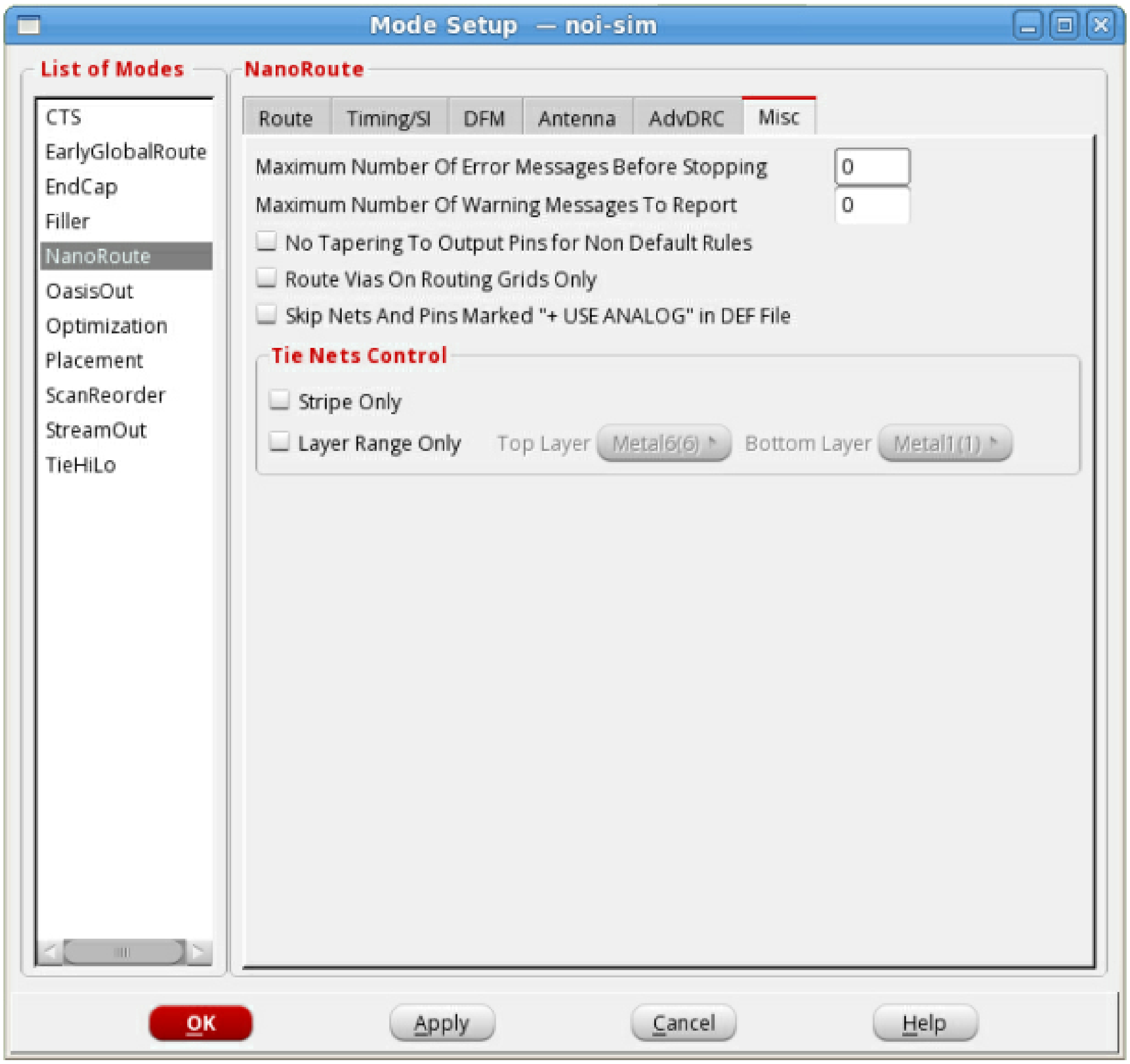
Enclose Via Completely In Standard Cell Pin		
	Encloses via geometries completely inside standard cell pins. Select this option to avoid MINSTEP violations for standard cell pin access. *Default:* Off	
Access Standard Cell Pins With Vias Only		
	Allows via access only to standard cell pins. Does not allow planar access. *Default: False*	
	True	Allows via access only. Does not allow planar access.
	False	Allows both via and planar access.
	Layer Range:	Lets you specify the layer range for limiting via access.
Strictly Honor Non Default Rule Spacing		
	Uses nondefault spacing rules for wide wires. If vias are tapered, still uses default vias. By default, the router treats nondefault rule spacing as a soft attribute; that is, when routing resources are available, it honors the nondefault rule. If the area is too congested, and resources are not available, the router might not honor nondefault spacing rules. You can override this behavior by selecting this option. You define nondefault routing rules in the NONDEFAULTRULE statement of the LEF file. *Default:* Off	

Related Text Commands

- `getNanoRouteMode`
- `setNanoRouteMode`

NanoRoute - Misc

Use the *Misc* page to specify additional NanoRoute options.
→ Choose *Tools - Set Mode - Mode Setup* and select *NanoRoute.* Then, select *Misc*.



Fields and Options

Maximum Number Of Error Messages Before Stopping	
	Specifies the maximum number of error messages for any one command written to the log file before stopping processing. *Default:* 1
Maximum Number Of Warning Messages To Report	

	Specifies the maximum number of warning messages for any one command reported to the log file. After reaching this number, the router continues processing, but does not report warnings for this command. *Default:* 20
No Tapering to Output Pins for Non Default Rules	
	Prohibits the router from tapering at standard cells, macro cells, and block output pins. *Default:* Off
Route Vias On Routing Grids Only	
	Centers vias on routing grids by dropping them at track intersections. *Default:* Off
Skip Nets And Pins Marked "+ USE ANALOG" in DEF File	
	Skips routing nets or pins marked + USE ANALOG in the DEF file. *Default:* Off
Stripe Only	Specifies targets for tie-high and tie-low nets. • When off, connects tie nets to nearby stripes, ring pins, or core rings. • When on, connects tie nets to the same targets as when on, plus macro (power and ground) pins, cover macro pins, and standard cell followpins. I/O pad pins and pad ring pins are excluded from tie-net connections. *Default:* If the design contains stripes, the behavior is the same a when off. If the design does not contain stripes, the behavior is the same as when on.
Layer Range Only	Specifies the range of routing layers for stripes.
Honor Partition	
	Routes nets belonging to a partition completely inside that partition and nets that are part of the top-level glue logic completely within the top-level channels. *Default:* Off

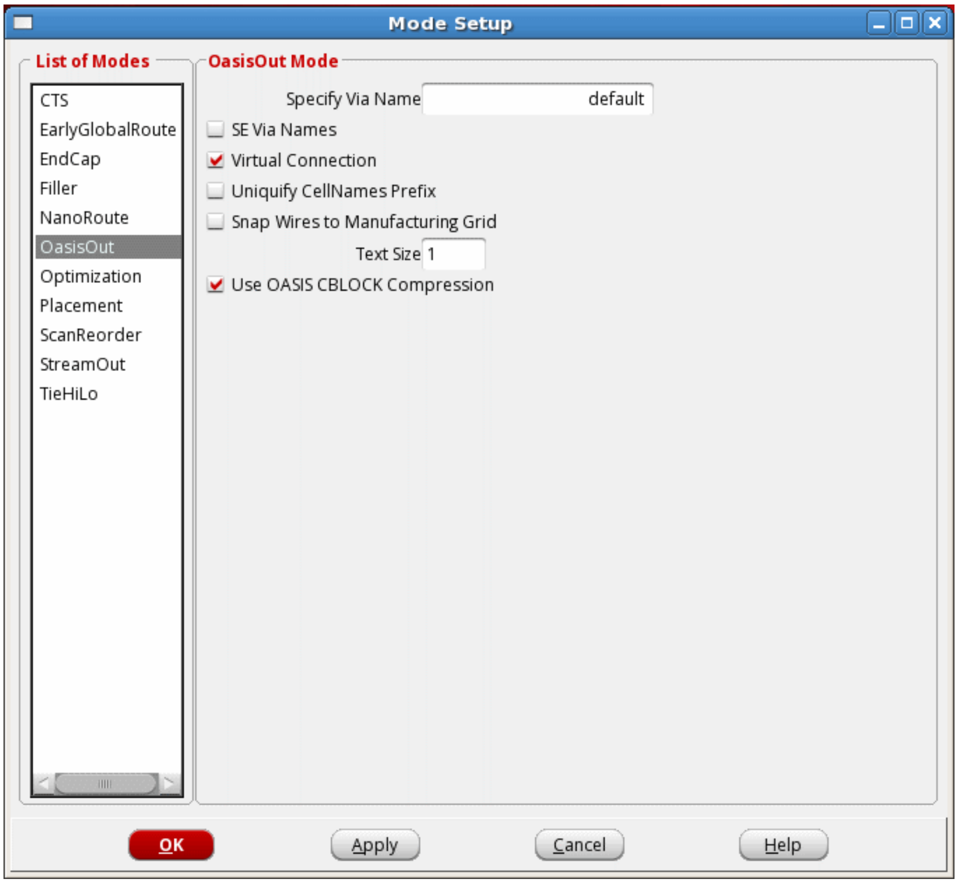
Related Text Commands

- `getNanoRouteMode`
- `setNanoRouteMode`

Mode Setup - OasisOut

Use the *Mode Setup - OasisOut* page to control certain aspects of how the software generates OASIS files.

- Choose *Tools - Set Mode - Mode Setup* and select *OasisOut*.



Fields and Options

Specify Via Name	Specifies the naming convention that the oasisOut command uses for via cells declared in the DEF file. **Note:** Via names are truncated if they are longer than 32 characters. The software automatically appends a unique identifier to names if there is a name conflict. You can use any of the following characters to specify a format string to generate names that give you information about the cell contents. Separate the characters with underscores (_) to improve readability. You can list them in any order. • %c Specifies the number of columns. • %l(lcu) Specifies the via layers. For the lower layer, use %l or %l(l). For the cut layer, use %l(c). For the upper layer, use %l(u). You can specify one, two, or all three layers. Enclose the l, c, and u in parentheses, as in the following examples: %l(c), %l(lu). • %n Specifies the number of cut rows and columns that make up a cut array. • %r Specifies the number of cut rows. • %t Specifies the top structure name. • %u Specifies a unique number for the via. • %v Specifies the via name in the DEF file.
SE Via Names	Determines the naming convention used for vias declared in the LEF file. If you select this option, the software creates unique names. If you do not select this option, the software retains the LEF via names. *Default:* Off
Virtual Connection	Appends a colon (:) label to pin names for DEF pins with the .extra*N* syntax and to LEF pins with multiple ports (if *Output Macros* is selected for LEF pin ports that have disjoint shapes). *Default:* On
Uniquify Cellnames Prefix	

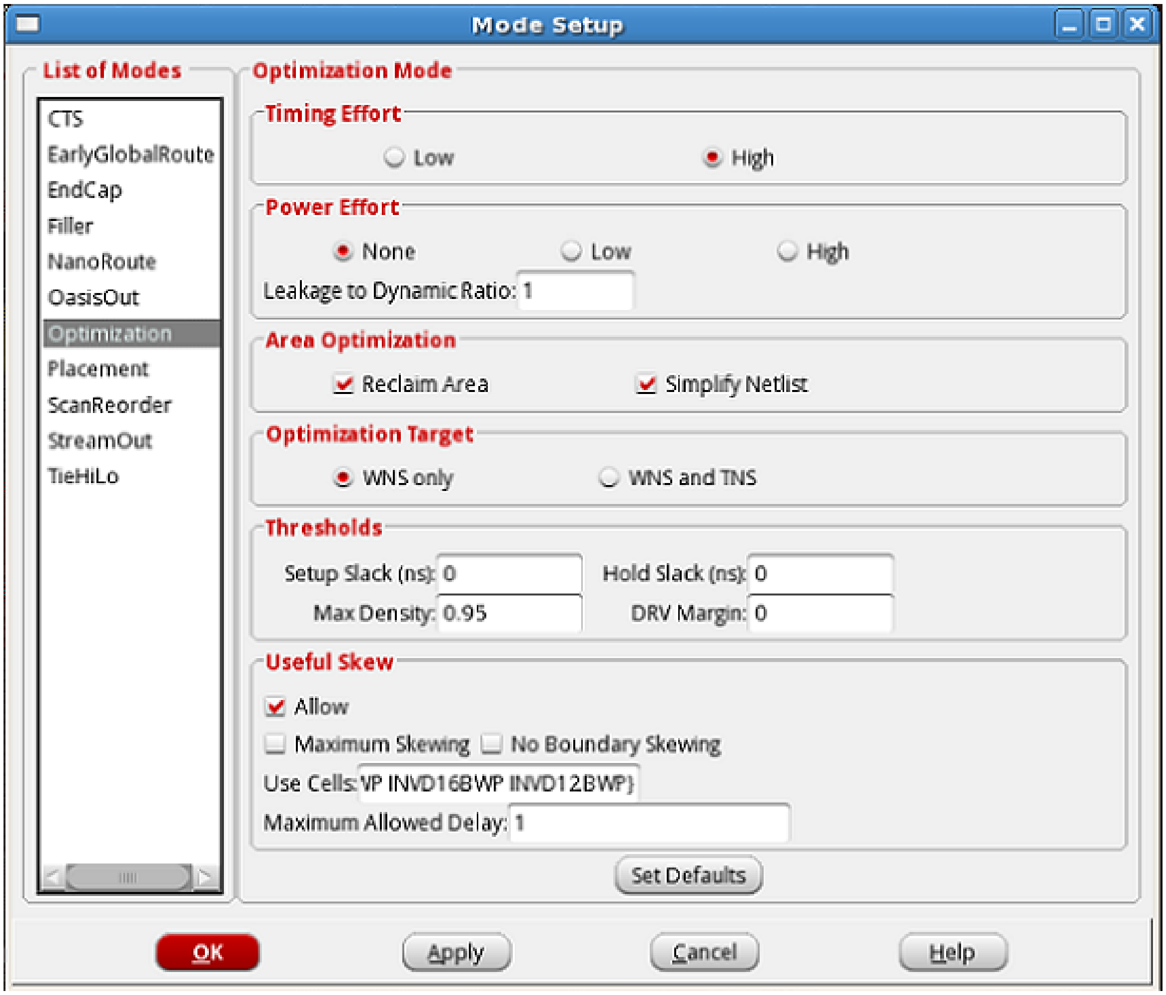
	Adds a prefix, instead of a suffix, to uniquified cell names. The prefix is the source filename. *Default:* Off (The software adds a suffix (also the source filename) to uniquified cell names)
Snap Wires to Manufacturing Grid	
	Snaps the nets' wires to the manufacturing grid. *Default:* Off
Text Size	Changes the size of the text used in the text labels in the OASIS file written by the Innovus software. • To increase the size of the text, specify a positive real number that is greater than 1. • To decrease the size of the text specify a positive real number that is less than 1. *Default:* 1
Use OASIS CBLOCK Compression	
	Reduces file size by using cblock compression. The streamOut command can process merged OASIS files with cblocks, even if this option is not selected. *Default:* On

Related Text Commands

- `getStreamOutMode`
- `setStreamOutMode`
- `streamOut`

Mode Setup - Optimization

Use the *Mode Setup - Optimization* page to set effort levels for timing, leakage, and yield; specify area optimization options, thresholds for slack and density and a margin for DRV; and set useful skew options. Choose *Tools - Set Mode - Mode Setup* and then select *Optimization*.



Optimization Fields and Options

Timing Effort	Specifies the effort level the software uses for timing optimization. *Default: High*	
	Low	Specifies low effort level. Use this level for design prototyping. This level triggers global resizing and buffering steps in order to obtain a good timing result in the fastest run time.
	High	Specifies high effort level. Use this level to reach timing closure for challenging designs. This level activates all the physical synthesis optimization transforms.
Power Effort		

	Specifies the power-driven optimization functionality in Innovus. This option provides the effort level for optimizing leakage power and dynamic power in the design. Power-driven optimization implies that the `optDesign` command now performs Power, Performance, and Area (PPA) trade-offs at the transform level at every step of timing optimization. This option is used along with the *Leakage to Dynamic Ratio* option. *Default: None* You can specify any one of the following options:	
	None	Specifies that no power optimization is to be performed.
	Low	Specifies that power optimization is not the highest priority. When this is specified, power optimization is performed only at certain stages of the `optDesign` flow, which is dependent on the value of the the specified *Leakage to Dynamic Ratio* . When the *Leakage to Dynamic Ratio* is 1.0, optDesign will optimize leakage power after each timing optimization step and no high leakage cells are inserted during hold fixing. When *Leakage to Dynamic Ratio* is 0.0, optDesign will optimize dynamic power at the preCTS stage. For all values of *Leakage to Dynamic Ratio* between 0.0 and 1.0, both of the above are done.
	High	Specifies that power optimization is the highest priority. Using the high effort level option indicates that power optimization is performed during all calls to `optDesign` , which is dependent on the value of the *Leakage to Dynamic Ratio* . Timing Optimization is power aware and uses high-effort techniques when choosing the best timing optimization fixes to implement.
Area Optimization		
	Reclaim Area	Creates additional space in the design by downsizing gates or deleting buffers, while maintaining worst slack and total negative slack. *Default:* On **Note:** This option is not enabled when *Timing Effort* is set to *Low*.

	Simplify Netlist	Determines whether to simplify the netlist during timing optimization. The software recovers area, decreases congestion, and improves runtime by simplifying the netlist in the following ways: • Removing dangling output instances • Propagating constants • Removing unobservable logic • Remapping useless logic The software respects the set_dont_touch constraint, so it does not remove the constrained flip-flops, and does not touch non-uniquified modules. *Default:* Off **Note:** This option is not enabled when *Timing Effort* is set to *Low*.
Optimization Target		
WNS Only	Applies `setOptMode -allEndPoints false`. *Default*: on	
WNS and TNS	Applies `setOptMode -allEndPoints true` *Default*: off	
Thresholds Setup Slack (ns)	Specifies a target slack value in nanoseconds for setup analysis. During setup violation repair, the setup target slack is *setupTargetSlack* and the hold target slack is set to 0. Generally, you use both *Setup Slack* and *Hold Slack* for hold analysis. If you specify *Hold Slack* only, the *Setup Slack* value is 0. *Default*:0	
Hold Slack (ns)	Specifies a target slack value in nanoseconds for hold analysis only. During setup violation repair, the setup target slack is *setupTargetSlack* and the hold target slack is set to 0. Generally, you use both *Setup Slack* and *Hold Slack* for hold analysis. If you specify *Hold Slack* only, the *Setup Slack* value is 0. *Default:* 0	
Max Density	Specifies the maximum area of utilization during timing optimization. *Default:* 0.95	

DRV Margin	Scales the maximum capacitance and maximum transition constraints according to the *margin* specified decimal value. For example, a margin of 0.2 (20 percent) multiplies the constraints by 0.8. The margin can be positive or negative. Introducing this margin of pessimism improves correlation between the number of DRC violations before and after routing. *Default:* 0.0
UsefulSkew Allow	Enables useful skew and lets you select useful skew options. *Default:* Off
Maximum Skewing	Advances sequential elements more aggressively than by default, without degrading the worst negative slack. This option and the *Maximum Allowed Delay* option are complementary: If you select both options, the software uses the aggressive algorithm while respecting the *Maximum Allowed Delay* limit. *Default:* Off
No Boundary Skewing	
	Excludes boundary sequential cells in useful skew calculations. *Default:* Off
Use Cells	Specifies the cells for useful skew to use during post-CTS buffer insertion. *Default:* The software uses any cells.
Maximum Allowed Delay	
	Limits the amount of slack (in nanoseconds) the software can borrow from neighboring flip-flops when performing useful skew operations. The Innovus delay calculation and RC extraction methods might differ from those of sign-off tools, so other setup violations might occur if the software borrows too much slack. By having control over slack borrowing, you can prevent these setup violations. Limiting borrowed skew also limits the clock tree skew and avoids large hold violations. This option and the *Maximum Skewing* option are complementary: If you select both options, the software uses the aggressive algorithm while respecting the *Maximum Allowed Delay* limit. *Default:* The software borrows the amout of slack needed to reduce setup violations--there is no maximum.

Related Text Commands

- `getOptMode`
- `setOptMode`

Mode Setup - Placement

Use the *Mode Setup - Placement* page to set global parameters for placing standard cells and refining placement.

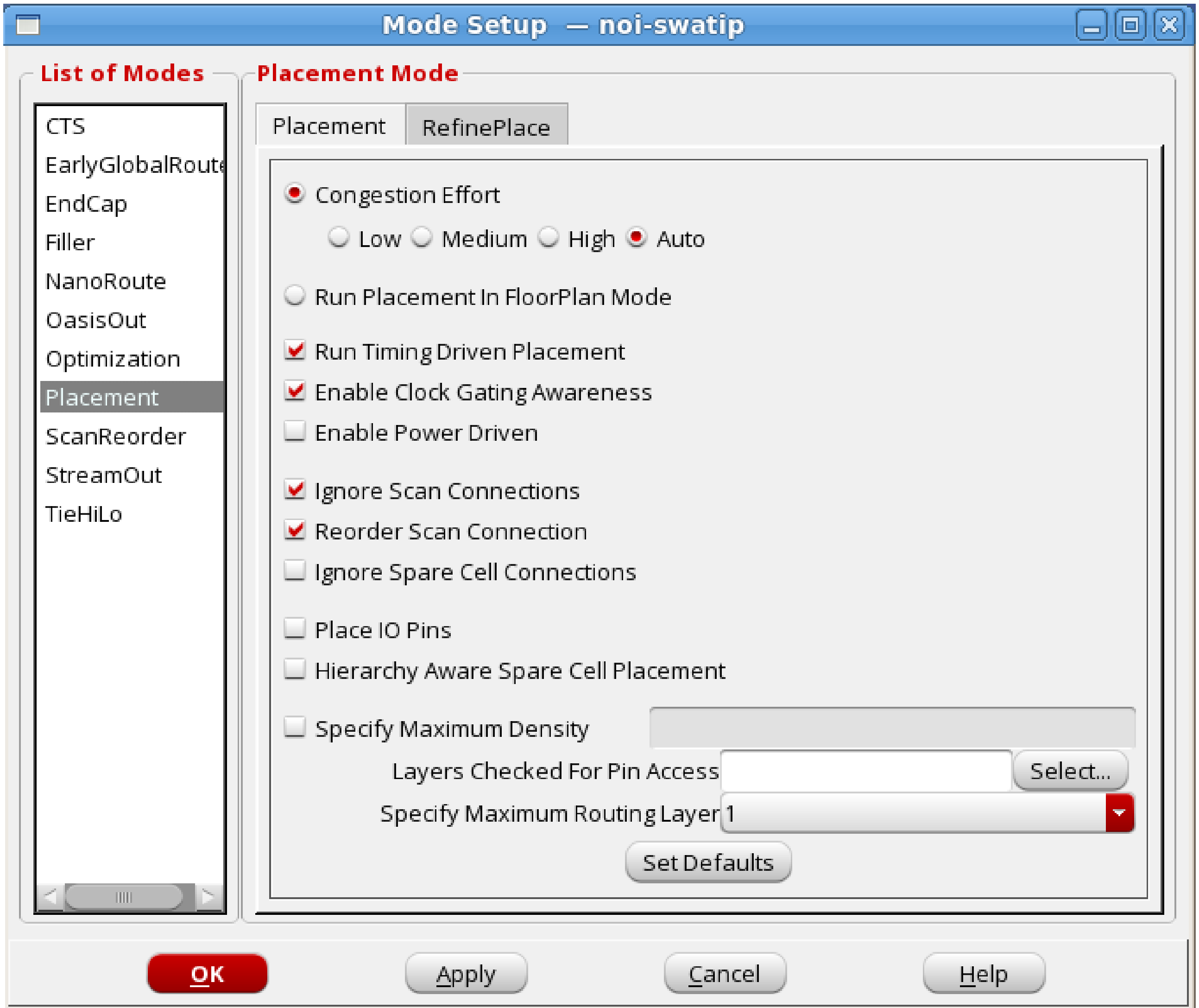
The Mode Setup - Placement page contains the following subpages:

- Placement
- RefinePlace

Placement

Use the *Placement* page to set global parameters for placement of standard cells .

Choose *Tools - Set Mode - Mode Setup* and then select *Placement*.



Fields and Options

Congestion Effort	Specifies the effort level for decreasing congestion. In general, a congestion effort increases the run time. *Default: Auto*	
	Low	Runs fewer iterations of placement to arrive quickly at a legal placement. This parameter might decrease placement quality.
	Medium	Runs placement on designs in a normal effort level.
	High	Runs more iterations of placement in an effort to achieve better congestion results. This parameter increases the run time.

	Auto	Automatically determines whether the design is congested and performs extra congestion driven effort for highly congested designs.
Run Placement in Floorplan Mode		
	Runs a quick placement to gauge the feasibility of the netlist, but might not place components in legal locations. This mode assumes non-timing-driven placement.	
Run Timing Driven Placement		
	Takes timing into account during placement to improve the placement of instances on timing critical paths. Before using this parameter, make sure the timing constraints are loaded in the design. This option is disabled if you select *Run Placement in Floorplan Mode*.	
Enable Clock Gating Awareness		
	Specifies that placement is aware of clock gate cells in the design. Load the clock tree specification file before running the placement command with this option selected. *Default*: Off	
Enable Power Driven	Identifies and constrains power-critical nets to reduce switching power. In most cases, timing is not degraded. However, in some cases, a trade-off between power and timing is required. **Note:** This option is not enabled if *Run Placement in Floorplan Mode* is selected or if you have not loaded an activity file (TCF or VCD) to supply the net switching information. Load the activity file using the `read_activity_file` command.	
Ignore Scan Connections		
	Disregards the scan connections while placing the scan groups. Before you place the design, you must already have specified the scan cells with the specifyScanCell command, or the scan cell information must be in the timing library. *Default*: On	
Reorder Scan Connections		

	Ignores the scan chain connectivity during placement and performs scan chain reordering after placement. If this option is not selected, the software considers scan chain connectivity during placement and does not perform scan chain reordering after placement. *Default*: On
Ignore Spare Cell Connections	
	Does not consider spare cell connections when placing spare cells. Before you place the design, you must already have specified the spare cells with the specifySpareGate command, or the spare cell information must be in the timing library. *Default*: On **Note:** The placer disconnects high-fanout (nets with more than 75 terminals) from spare cells, even when this option is not selected.
Place IO Pins	Moves placed and unplaced I/O pins, based on the placement of connected instances in an attempt to find a better I/O pin placement than the one specified in the I/O pin placement or floorplan file. At the end of global placement, the I/O pin location is legalized. When this option is off, I/O pins are ignored during global placement and no legalization is done at the end. *Default*: On ⓘ If the placer does not place standard cells, for example if all instances are fixed or if there is no placeable area, it also skips pin assignment.
Hierarchy Aware Spare Cell Placement	
	Places spare cells in the netlist within a hierarchical module, even if no region or fence constraints are specified. • If you select this option, spare cells in a hierarchical module are placed within the bounds of the hierarchy. • If you do not select this option, spare cells are spread out within the placement area, and are not bound to the hierarchy. *Default:* Off
Specify Maximum Density	

	Controls local density during global placement. Sets the maximum placement density of the core area so that the placement engine aggressively minimizes the wirelength, while satisfying the maximum density constraint. This helps to achieve better timing results in low utilization designs. After global placement, the density control is removed. Use a value between 0 (zero percent) and 1 (100 percent). For example, a value of 0.5 indicates that the maximum utilization of the entire design will be 50% or less.
Layers Checked For Pin Access	
	Specifies the layers to check for pin access. Click the *Select* button to open the Select Layer form to add or delete layers.
Specify Maximum Routing Layer	
	Constrains placement up to the specified layer for congestion and routability estimation.
Set Defaults	Resets the values of the options on this page to the default values.

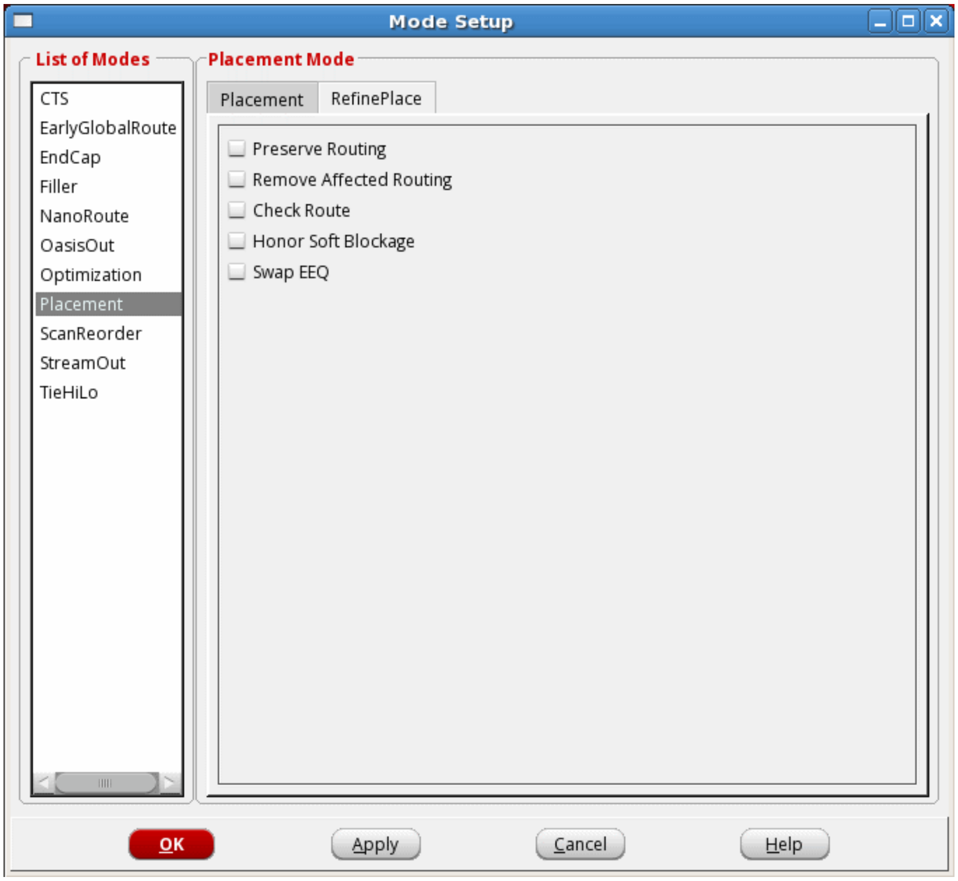
Related Text Commands

- `getPlaceMode`
- `setPlaceMode`

RefinePlace

Use the *RefinePlace* page to set global parameters for correcting and reporting flawed cell locations and instance overlap problems.

- Choose *Tools - Set Mode - Mode Setup* and select *Placement.* Then, select *RefinePlace*.


Mode Setup
List of Modes
CTS
EarlyGlobalRoute
EndCap
Filler
NanoRoute
OasisOut
Optimization
Placement
ScanReorder
StreamOut
TieHiLo
Placement Mode
Placement
RefinePlace
Preserve Routing
Remove Affected Routing
Check Route
Honor Soft Blockage
Swap EEQ
OK
Apply
Cancel
Help

Fields and Options

Preserve Routing	Preserves all routed wires. *Default:* Off
Remove Affected Routing	
	Removes all wires connected to moved cells. *Default:* Off
Check Route	Considers pre-routed FIXED signal wires and avoids creating DRC violations between FIXED signal wires and instance pins. When this parameter is not specified, refinePlace ignores FIXED signal wires. Using this option might result in longer run time. *Default:* Off
Honor Soft Blockage	Specifies that soft blockage will be considered when running the command. By default, the soft placement blockage is only considered during global placement, and is ignored in refinePlace and optimization stages. *Default:* Off
Swap EEQ	Allows replacement of master cells by EEQ cells during detailed placement to improve routability. After detailed placement, the software reports the number of replacements. EEQ cells are defined in the LEF file. *Default:* Off

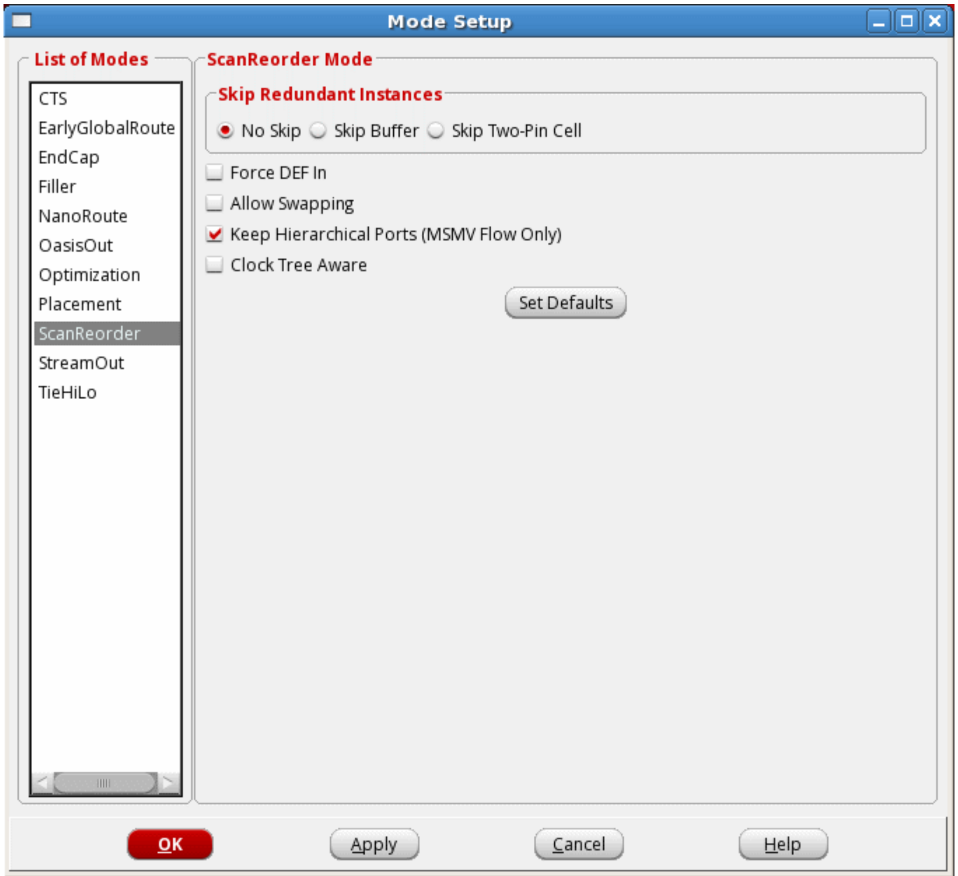
Related Text Commands

- `getPlaceMode`
- `setPlaceMode`

Mode Setup - ScanReorder

Use the *Mode Setup - ScanReorder* page to set global parameters for scan reordering.

- Choose *Tools - Set Mode - Mode Setup* and then select *ScanReorder*.


Mode Setup
List of Modes
CTS
EarlyGlobalRoute
EndCap
Filler
NanoRoute
OasisOut
Optimization
Placement
ScanReorder
StreamOut
TieHiLo
ScanReorder Mode
Skip Redundant Instances
No Skip
Skip Buffer
Skip Two-Pin Cell
Force DEF In
Allow Swapping
Keep Hierarchical Ports (MSMV Flow Only)
Clock Tree Aware
Set Defaults
OK
Apply
Cancel
Help

Fields and Options

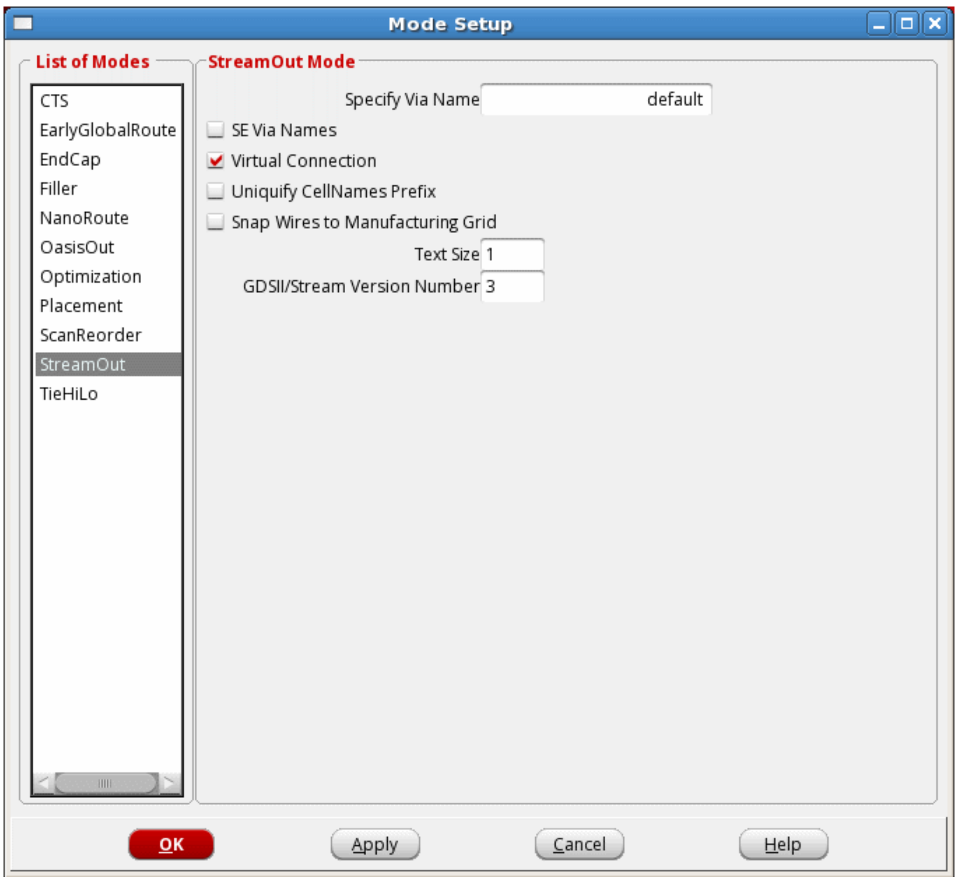
Skip Redundant Instances		
	Specifies how scan reordering handles buffers and inverters in the scan chain. *Default: No Skip*	
	No Skip	Specifies that buffers and inverters remain after the scan chain reorder.
	Skip Buffer	Ignores buffers in the scan chain. If a buffer or inverter is not connected elsewhere in the design, scanReorder removes the buffer.
	Skip Two-Pin Cell	
		Ignores buffers and inverters in the scan chain. If a buffer or inverter is not connected elsewhere in the design, scanReorder removes the buffer or inverter.
Allow Swapping	Allows the software to swap scan elements between scan chains. *Default:*Off	
Keep Hierarchical Ports (MSMV Flow Only)		
	Maintains or corrects the hierarchical ports without deleting or inserting shifters, and reorders the remaining scan chain. *Default:* Off	
Clock Tree Aware	Specifies whether scan reordering is clock tree aware. If this parameter is not specified, or if 0 is specified for this parameter, scan reordering is not clock tree aware and is completely wirelength driven. If a value is specified, the value must be a floating point number between 0 and 1, where 0 means scan reordering is completely wirelength driven and 1 means it is completely clock tree driven. The closer the value is to 1, the more importance is given to clock trees over wirelength. *Value:* Specify a floating number between 0 and 1. Specifying a value is optional. *Default:* Off (The software is not clock tree aware.) If this option is selected, the default value is 1.	
Set Defaults	Resets the options on this page to the default values.	

Related Text Commands

- getScanReorderMode
- setScanReorderMode

Mode Setup - StreamOut

Use the *Mode Setup - StreamOut* page to set the global options for creating a GDSII Stream file of the current database.
Choose *Tools - Set Mode - Mode Setup* and select *StreamOut*.



Fields and Options

Specify Via Name	Specifies the naming convention that the software uses for via cells declared in the DEF file. **Note:** When the version of the GDS file is 3 (this is the default version), via names are truncated if they are longer than 32 characters. The software automatically appends a unique identifier to names if there is a name conflict. You can use any of the following characters to specify a format string to generate names that give you information about the cell contents. Separate the characters with underscores (_) to improve readability. You can list them in any order. • %c Specifies the number of columns. • %l(lcu) Specifies the via layers. For the lower layer, use %l or %l(l). For the cut layer, use %l(c). For the upper layer, use %l(u). You can specify one, two, or all three layers. You must enclose the l, c, and u in parentheses, as in the following examples: %l(c), %l(lu). • %n Specifies the number of cut rows and columns that make up a cut array. • %r Specifies the number of cut rows. • %t Specifies the top structure name. • %v Specifies the via name in the DEF file.
SE Via Names	Determines the naming convention used for vias declared in the LEF file. If you select this option, the software creates unique names. If you do not select this option, the software retains the LEF via names. *Default:* Off
Virtual Connection	Appends a colon (:) label to pin names for DEF pins with the .extra*N* syntax and to LEF pins with multiple ports (if *Output Macros* is selected for LEF pin ports that have disjoint shapes). *Default:* On
Uniquify CellNames Prefix	
	Adds a prefix, instead of a suffix, to uniquified cell names. The prefix is the source filename. *Default:* Off (The software adds a suffix (also the source filename) to uniquified cell names)

Snap Wires to Manufacturing Grid	
	Snaps the nets' wires to the manufacturing grid. *Default:* Off
Text Size	Changes the size of the text used in the text labels in the GDSII Stream file written by the Innovus software. • To increase the size of the text, specify a positive real number that is greater than 1. • To decrease the size of the text specify a positive real number that is less than 1. *Default:* 1
GDSII/Stream Version Number	
	Specifies the version for a created GDSII Stream file. *Default:* 3

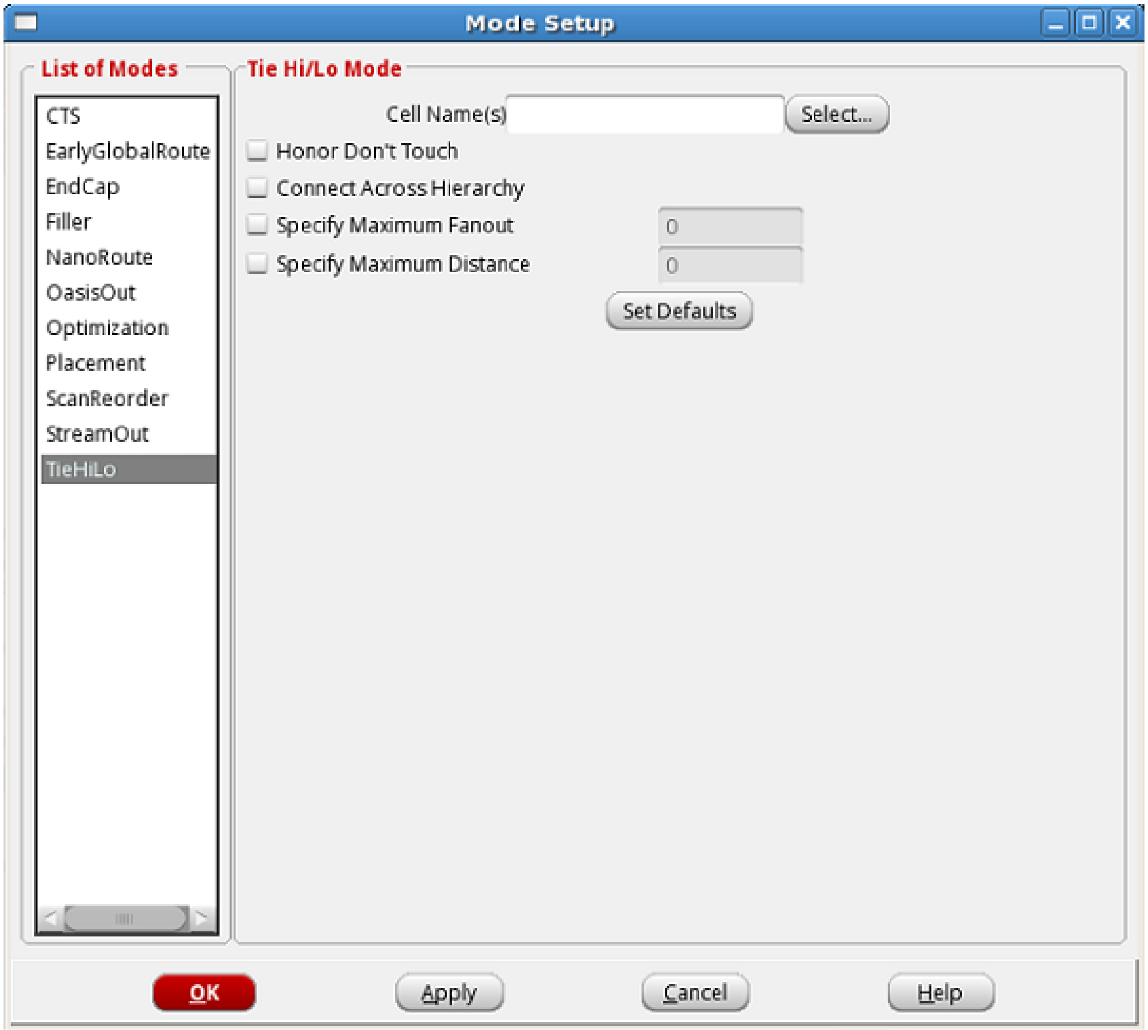
Related Text Commands

- `getStreamOutMode`
- `setStreamOutMode`
- `streamOut`

Mode Setup - TieHiLo

Use the *Mode Setup - TieHiLo* page to set global parameters for the Tie HI/LO commands.

- Choose *Tools - Set Mode - Mode Setup* and select *TieHiLo*.


Mode Setup
List of Modes
CTS
EarlyGlobalRoute
EndCap
Filler
NanoRoute
OasisOut
Optimization
Placement
ScanReorder
StreamOut
TieHiLo
Tie Hi/Lo Mode
Cell Name(s)
Select...
Honor Don't Touch
Connect Across Hierarchy
Specify Maximum Fanout
0
Specify Maximum Distance
0
Set Defaults
OK
Apply
Cancel
Help

Fields and Options

Cell name(s)	Specifies the tie cell names to be used by the addTieHiLo command. You can specify a maximum of two tie-cells, where one cell must be a tie-high driver, and the other a tie-low driver. The two tie-cell names must be in quotation marks. *Default:* "" (empty string)
Honor Don't Touch	Allows both addTieHiLo and deleteTieHiLo commands to honor the dont_touch property set on instances, nets, cells, and modules. For instances that need to be tied off, the dont_touch property has no effect, because the operation is on the net connected to one of its terms. *Default:* Off
Create Hierarchy Port	
	Allows the added tie cells to connect to tie pins across hierarchical boundaries if other constraints, such as maximum fanout and maximum distance, allow it. Logs port connections to a file named tiehilo.rpt.
Specify Maximum Fanout	
	Specifies the number of tie-pins a tie-net can drive. A value of 0 implies no fanout constraint. *Default*: 0
Specify Maximum Distance	
	Specifies the distance, in microns, between the tie-cell driver and the tie-pins. A value of 0 implies no distance constraint. *Default*: 0
Set Defaults	Specifies the distance, in microns, between the tie-cell driver and the tie-pins. A value of 0 implies no distance constraint. *Default*: 0

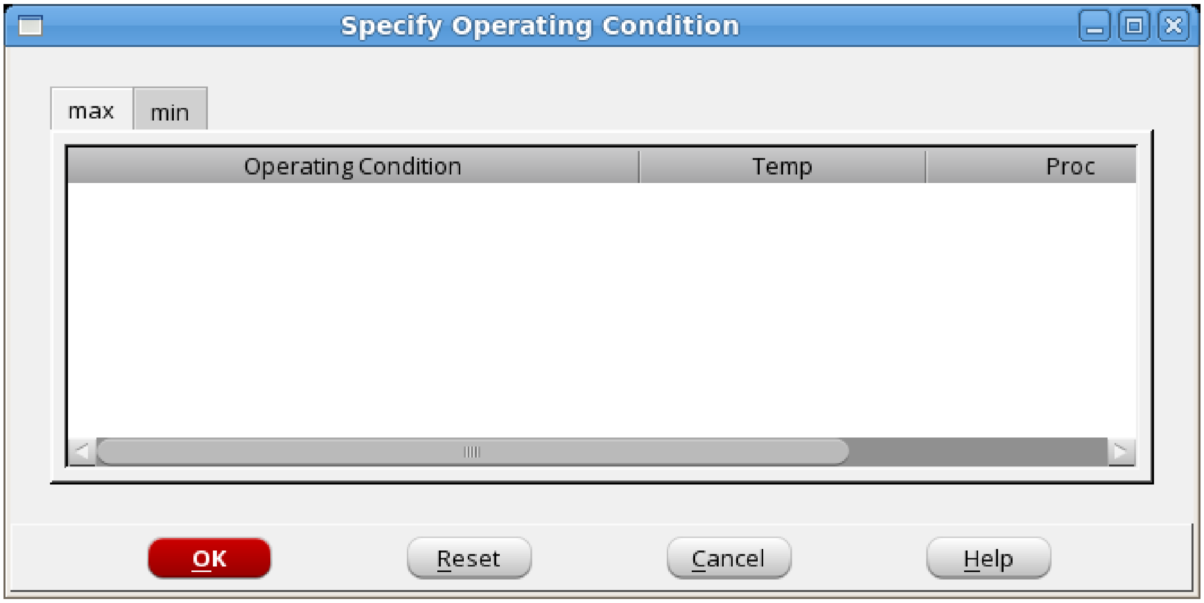
Related Text Commands

- `getTieHiLoMode`
- `setTieHiLoMode`

Specify Operating Condition/PVT

Use the Specify Operating Condition form to select the operating temperature, process, or voltage conditions for the design. The operating conditions are contained in the timing library, which are normally read in during design import.

- Choose *Tools - Set Mode - Specify Operating Condition/PVT* and click on either the Min or Max tab to select the operating condition you want to specify.



Specify Operating Condition Fields and Options

Operating Condition	Displays the name of the operating condition. By default, the operating condition selected under the *Max* tab is used for setup analysis and the operating condition selected under the *Min* tab is used for hold analysis. When using the SignalStorm integration, it is advisable to keep the operating conditions consistent with the process corners selected for SignalStorm analysis.
Temp	Displays either the minimum or maximum temperature for the operating condition.
Proc	Displays either the minimum or maximum process parameter for the operating condition.
Volt	Displays either the minimum or maximum voltage for the operating condition.

Related Text Commands

For more information, see "Timing Commands" in the *Innovus Text Command Reference*.

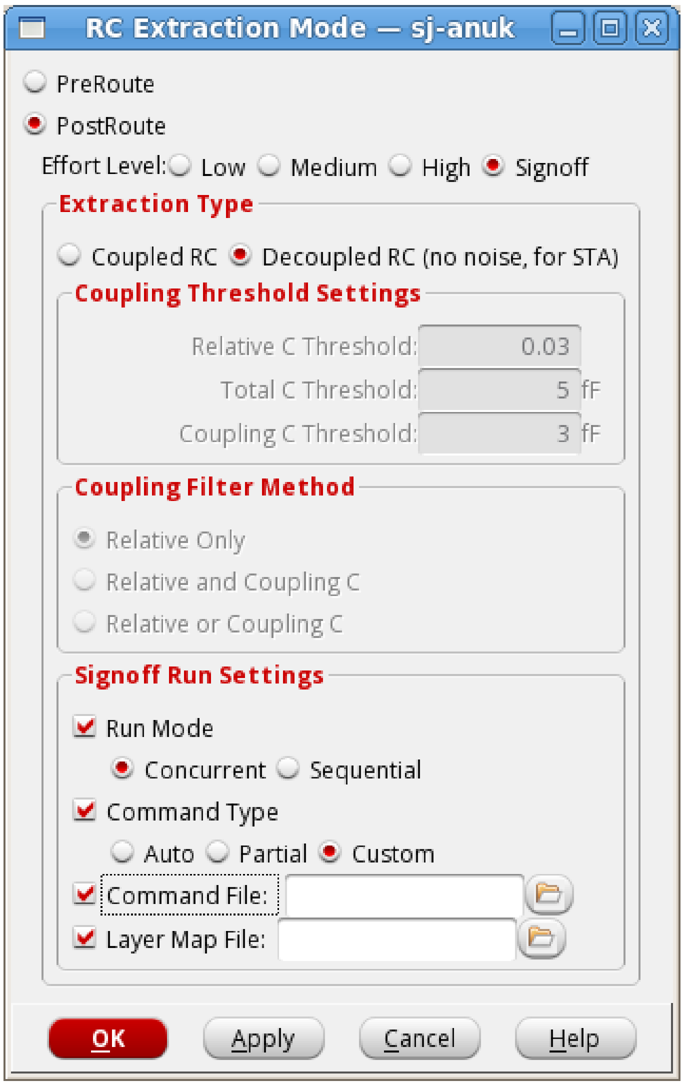
Related Topics

For information on the following topics, see the RC Extraction chapter in *Innovus User Guide*:

- PreRoute Extraction
- PostRoute Extraction

Specify RC Extraction Mode

Use the *RC Extraction Mode* form to set the RC extract mode, and select the extraction engine.
Choose *Tools - Set Mode - Specify RC Extraction Mode*.



RC Extraction Mode Fields and Options

PreRoute	Uses preRoute mode. This mode should only be used during an early prototyping stage where more detailed extraction is not needed. In this mode, the coupling capacitances are grounded.	
PostRoute	Uses postRoute mode. This is used for RC parasitic extraction after detailed routing.	
	Effort Level	Specifies the postRoute engine variant that you want to use for performing RC extraction. **Note:** The effort levels and corresponding extraction engines are as follows: • low = Native (detail) engine • medium = Turbo Quantus (TQuantus) • high = Integrated Quantus (IQuantus) • signoff = Standalone Quantus (Quantus QRC)
	Low	Invokes the native detailed extraction engine.
	Medium	Uses the TQuantus extraction mode. TQuantus performance and accuracy falls between native detailed extraction and IQuantus engine. This engine supports distributed processing. TQuantus engine is recommended for process nodes < 65nm. This option requires a Quantus techfile but does not require an extra license.
	High	Uses the IQuantus extraction engine. IQuantus provides superior accuracy compared to TQuantus. IQuantus is recommended for extraction after ECO. In addition, IQuantus also supports distributed processing. This option requires a Quantus QRC techfile and a Quantus license.
	Signoff	Uses the Standalone Quantus extraction engine. This engine choice provides the highest accuracy. This option requires a Quantus techfile and a Quantus license. EXT installation is also required to get access to the Quantus executable.
The following options are only available in the postRoute mode:		
Coupled RC	Coupling capacitance to neighboring wires is reported separately. You must enter threshold data for the capacitance values (*Coupled RC* panel). Use coupled RC for (signal Integrity (SI) analysis.	

Decoupled RC	Coupling capacitances to neighboring wires is grounded. Use decoupled RC for Static Timing Analysis (STA).	
The following information is required when you select *Coupled RC* in the *Coupled RC* panel.		
Coupling Threshold Settings		
	Relative C Threshold (0-0.2)	
		The coupling between net A and B is recorded when it is higher than the specified fraction of the total capacitance of net A and B. The default value is 0.03 (3%), unless overwritten by the previous setDesignMode or setExtractRCMode command.
	Total C Threshold (fF)	
		If the total capacitance of a net is smaller than this value, the software grounds any coupling capacitance for this net. The default value is 5 fF, unless overwritten by the previous setDesignMode or setExtractRCMode command.
	Coupling C Threshold (fF)	
		The threshold value that determines when the extractor lumps a net's coupling capacitance to ground. The software decouples the coupling capacitance of nets when the total coupling capacitance between the pair of nets is lower than the threshold specified with this option. The default value is 3 fF, unless overwritten by the previous setDesignMode or setExtractRCMode command.
Coupling Filter Method	Specifies the coupling filtering mode. The filtering modes are conditions which define how to use the *Coupling C Threshold* and *Relative C Threshold* values, or their combination. Based on the filtering mode specified, the software determines which coupling capacitance is grounded. *Default*: For TQuantus,IQuantus, and Standalone Quantus extraction, the default option is *Relative and Coupling C*. For postRoute extraction with *Effort Level Low*, the default value is dependent on the process node, as specified in the setDesignMode command. If the process node is 130nm or below, the default value is *Relative and Coupling C* and if the process node is above 130nm, the default value is *Relative Only*.	
	Relative Only	Grounds the coupling capacitance of nets based on the threshold value set by the *Relative C Threshold* option.
	Relative and Coupling C	
		Grounds the coupling capacitance of nets only when it is lower than the threshold value specified with the *Relative C Threshold* option as well as the *Coupling C Threshold* option. In this mode, you enforce maximum restriction on grounding the coupling capacitances.

	Relative or Coupling C	
		Grounds the coupling capacitance of nets if it is lower than the threshold value specified with the *Relative C Threshold* or *Coupling C Threshold* option.
The following information is required when you select *Effort Level Signoff* in the postRoute mode.		
Signoff Run Settings		
	Run Mode Specifies the Quantus run mode in MMMC designs. The options, *Concurrent* and *Sequential* are available.	
		Concurrent Runs Quantus for all corners concurrently.
		Sequential Runs Quantus for all corners sequentially. **Note:** This mode is not supported when the *Command Type* selected is *Custom.*
	Command Type Specifies whether the settings for running Quantus are derived from the software settings, or from user-created command file. The options, *Auto*, *Partial*, and *Custom* are available.	
		Auto Derives the Quantus settings automatically from the Innovus parameter settings.
		Partial Appends user commands from the qrcCmdFile to the settings derived from the Innovus parameter settings. The partial mode command file must be provided in CCL syntax. This command type is used only when you add extraction directives for those options that cannot be set in Innovus. For details regarding some important restrictions to keep in mind while using this *Command Type*, see the -qrcCmdType parameter of the `setExtractRCMode` command.

		Custom Gets the complete Quantus settings from the user-created command file. Except for input and output, no settings from Innovus parameters are used. The complete qrc cmd file must be provided in CCL syntax. For details regarding some important restrictions to keep in mind while using this *Command Type*, see the -qrcCmdType parameter of the `setExtractRCMode` command.
	Command File	
		Specifies the user-created Quantus command file to be used for running Standalone Quantus. The command file must be provided in CCL syntax. **Note:** This option is only valid for *Partial* or *Custom* command type.
	Layer Map File	
		Specifies the location of the optional layermap file for use with the TQuantus, IQuantus, and standalone Quantus engines. The layermap file must be provided in CCL syntax. For details, see the -lefTechFileMap parameter of the `setExtractRCMode` command.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setExtractRCMode`
- `setDesignMode`

For more information, see "RC Extraction Commands" in the *Innovus Text Command Reference*.

Related Topics

For information on the following topics, see the RC Extraction chapter in *Innovus User Guide*:

- PreRoute Extraction
- PostRoute Extraction

Specify Analysis Mode

Use the Specify Analysis Mode form to set the global analysis modes for timing analysis.

- Choose *Tools - Set Mode - Specify Analysis Mode*...

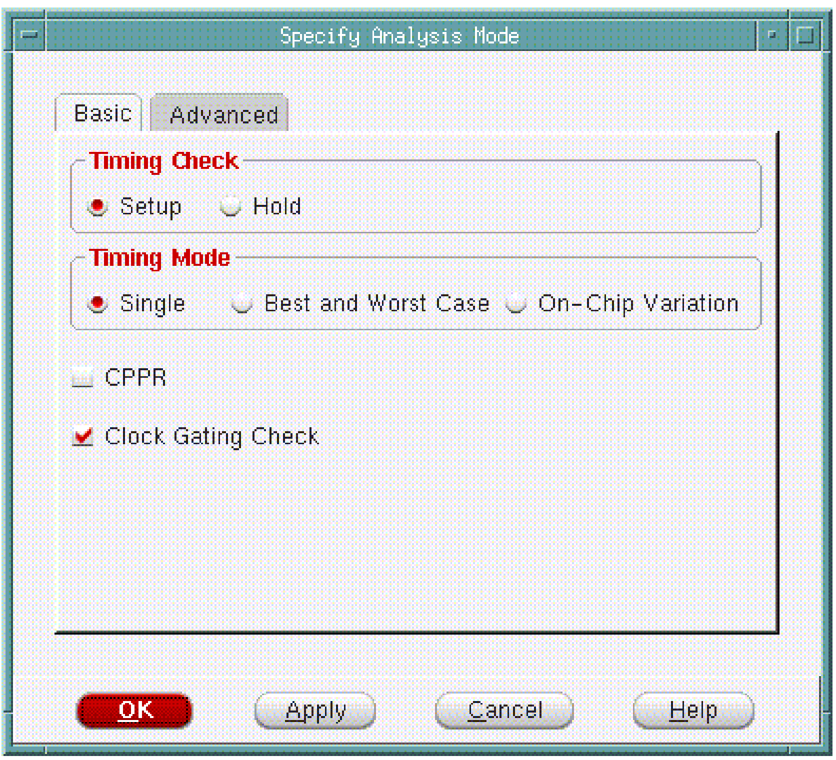
The Specify Analysis Mode form contains the following pages:

- SpecifyAnalysisModeBasic
- SpecifyAnalysisModeAdvanced

Specify Analysis Mode - Basic

Use the *Basic* page of the Specify Analysis Mode form to specify setup or hold check, and timing analysis mode.

- Choose *Tools - Set Mode - Specify Analysis Mode*.



Specify Analysis Mode - Basic Fields and Options

Setup	Specifies to check setup violation only.
Hold	Specifies to check hold violations only.
Single	Sets the timing analysis mode to single. In the single analysis mode, the software scales the delay values based on one operating condition. For more information, see "Single Timing Analysis Mode" in the *Innovus User Guide*.
Best and Worst Case	Sets the timing analysis mode to best case worst case. In the best case worst case analysis mode, the software checks the design for two extreme operating conditions. The software uses the maximum delays for all paths during setup checks and minimum delays for all paths during hold checks. For more information, see "Best-Case Worst-Case (BC-WC) Timing Analysis Mode" in the *Innovus User Guide*.
On-Chip Variation	Sets the timing analysis mode to on-chip variation. In the on-chip variation analysis mode, the software calculates the delay for one path based on maximum operating condition while calculating the delay for another path based on minimum operating condition for setup or hold checks. For more information, see "On-Chip Variation (OCV) Timing Analysis Mode" in the *Innovus User Guide*.
CPPR	Considers clock reconvergence pessimism during timing analysis.
Clock Gating Check	Reports the gating checks.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setAnalysisMode`

For more information, see "Timing Commands" in the *Innovus Text Command Reference*.

Related Topics

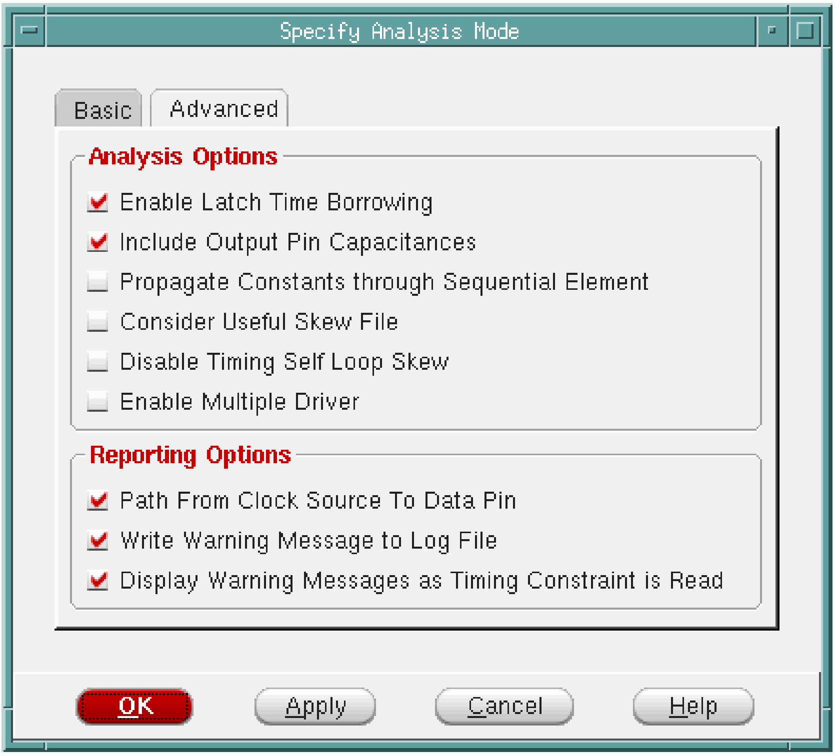
For information on the following topics, see "Timing Analysis" in the *Innovus User Guide*.

- "Timing Analysis Modes"

Specify Analysis Mode - Advanced

Use the *Advanced* page of the Specify Analysis Mode form to specify additional parameters for timing analysis checks.

- Choose *Tools - Set Mode - Specify Analysis Mode*, and click the *Advanced* tab.



Specify Analysis Mode - Advanced Fields and Options

Enable Latch Time Borrowing	
	Considers time borrowing during timing analysis. Time borrowing is the amount of time borrowed by a previous logic. *Default:* On
Include Output Pin Capacitance	
	Includes the output pin capacitance when calculating delay values. If you do not select this option, the Innovus software excludes only the pin capacitance of the driver for which you are calculating the delay. *Default:* On
Propagate Constants through Sequential Element	

	Sets the constants to be propagated while building the timing graph. The software reads the constants from the timing constraints file or the netlist. *Default:* Off (Disables the propagation of the constants and does not use the constants from the SDC file.)
Consider Useful Skew File	
	Considers clock skew while performing timing analysis. *Default:* Off
Disable Timing Self Loop Skew	
	Disables the consideration of clock skew due to clock uncertainty for a path starting and ending at the same register. If the clock skew is considered, the timing for such paths is pessimistic. *Default:* Off
Enable Multiple Driver	
	Enables the multiple-driver support for reporting. *Default:* On
Path From Clock Source To Data Pin	
	Specifies whether to report the path from the clock source to the D input pin of a register path. *Default:* On
Write Warning Message to Log File	
	Writes warning messages to the log file. *Default:* On
Display Warning Messages as Timing Constraint is Read	
	Displays warning messages as the timing constraints file is read. *Default:* On

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setAnalysisMode`

- `getAnalysisMode`

For more information, see "Timing Commands" in the *Innovus Text Command Reference*.

Related Topics

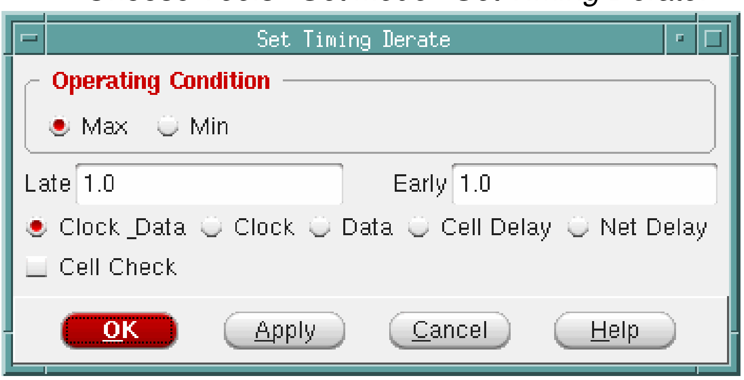
For information on the following topics, see "Timing Analysis" in the *Innovus User Guide*.

- "Specifying Timing Analysis Modes"

Set Timing Derate

Use the Set Timing Derate form to set the scaling or derating factors for early and late paths in the current design. The timing scaling factors affect the delay values generated in the timing reports. You can set scaling factors for data paths, clock paths, minimum and maximum operating conditions.

- Choose *Tools - Set Mode - Set Timing Derate.*



Set Timing Derate Fields and Options

Max	Applies the derating factor to the maximum operating condition.
Min	Applies the derating factor to the minimum operating condition.
Late	Specifies the derating factor for late paths. *Default:* `1.0`
Early	Specifies the derating factor for early paths. *Default:* `1.0`
Clock & Data	Applies the derating factors to both clock and data paths.
Clock	Applies the derating factors to clock paths only.
Data	Applies the derating factors to data paths only.
Cell Delay	Specifies scaling on cell delays. If neither the *Cell Delay* nor the *Net Delay* option is specified, the specified scaling factor applies to both types of delays.
Net Delay	Specifies scaling on net delays.
Cell Check	Specifies scaling on timing checks. Select this option with the *Min* option to specify scaling on hold arcs and with the *Max* option to specify scaling on setup arcs.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `set_timing_derate`

For more information, see "Timing Commands" in the *Innovus Text Command Reference*.

Related Topics

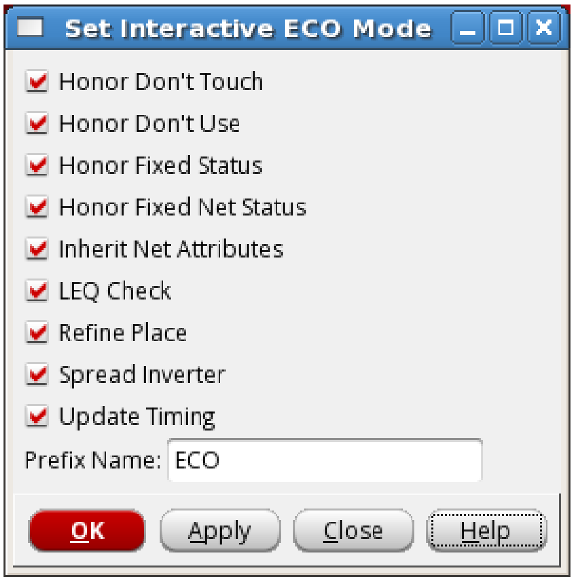
For information on the following topics, see "Timing Analysis" in the *Innovus User Guide*.

- "Specifying Timing Analysis Modes"

Set Interactive ECO Mode

Use the Set Interactive ECO Mode form to select different modes to control the behavior of ECO commands.

- Choose *Tools - Set Mode - Set Interactive ECO Mode.*



Set Interactive ECO Mode Fields and Options

Honor Don't Touch	Checks for the don't touch attribute on nets and instances.
Honor Don't Use	Checks for the don't use attribute on cells.
Honor Fixed Status	Does not allow preplaced, fixed instances to be resized.
Honor Fixed Net Status	Checks for fixed net wires. It restricts the addition or deletion on fixed net so that the fixed status of the wires is not altered.
Inherit Net Attributes	Inherits the net attribute.
LEQ Check	Enables functionality checking when swapping cells. The software can swap cells that are logically equivalent.
Refine Place	Legalizes placement whenever ecoAddRepeater or ecoChangeCell are used.
Spread Inverter	Distributes an inverter pair evenly between the driver and the first bifurcation point.
Update Timing	Controls whether the ECO commands recompute timing.
Prefix Name	Adds a prefix to the inserted cells.

Related Text Commands

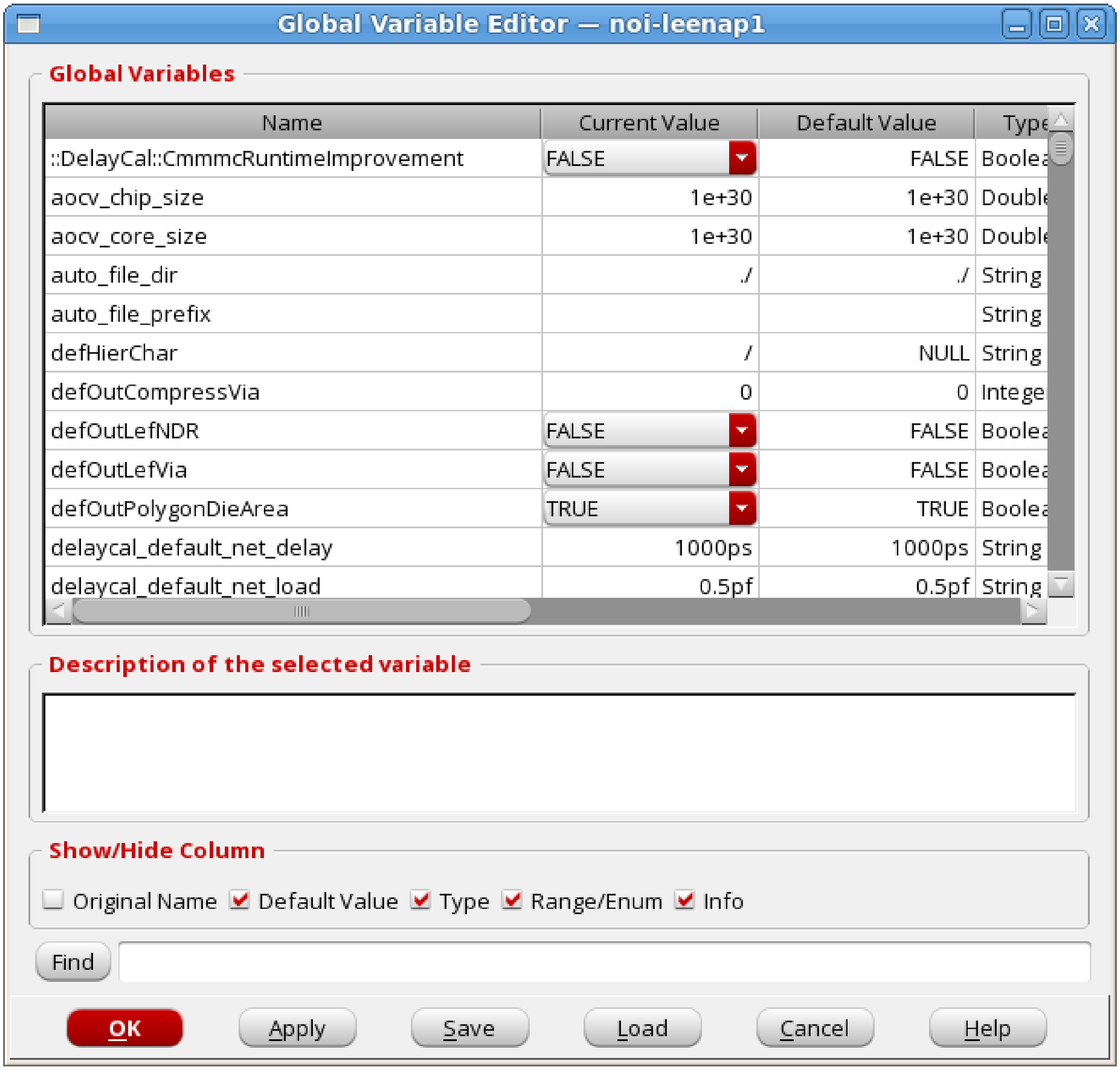
The following text command provides equivalent or additional functionality:

- `setEcoMode`

Set Global Variable

Use the *Set Global Variable* command to open the Global Variable Editor form. You can use this form to set and view the values of the global variables.

- Choose *Tools - Set Global Variable*.


Global Variable Editor — noi-leenap1
Global Variables
Name
Current Value
Default Value
Type
::DelayCal::CmmmcRuntimeImprovement
FALSE
FALSE
aocv_chip_size
1e+30
1e+30
aocv_core_size
1e+30
1e+30
auto_file_dir
./
./
String
auto_file_prefix
String
defHierChar
/
NULL
String
defOutCompressVia
0
0
defOutLefNDR
FALSE
FALSE
defOutLefVia
FALSE
FALSE
defOutPolygonDieArea
TRUE
TRUE
delaycal_default_net_delay
1000ps
1000ps
String
delaycal_default_net_load
0.5pf
0.5pf
String
Description of the selected variable
Show/Hide Column
Original Name
Default Value
Type
Range/Enum
Info
Find
OK
Apply
Save
Load
Cancel
Help

Global Variable Editor - Fields and Options

<table>
<tr><td>Name</td><td>Displays a selectable list of the global variables.</td></tr>
<tr><td>Current Value</td><td>Specifies the current value of the global variable.</td></tr>
<tr><td>Default Value</td><td>Specifies the default value of the global variable.</td></tr>
<tr><td>Type</td><td>Specifies the type of the global variable.</td></tr>
<tr><td>Range/Enum</td><td>Specifies the range of the global variable. For variables of type Enum, specifies possible values.</td></tr>
<tr><td>Info</td><td>Displays a brief description of how the variable is used.</td></tr>
<tr><td>Description of the selected variable</td><td>Displays a detailed description of the global variable currently selected in the Name field.</td></tr>
<tr><td>Show/Hide Column</td><td>Enables you to control the columns that are displayed in the editor. You can choose to show/hide the following columns:
Original Name
Default Value
Type
Range/Enum
Info</td></tr>
<tr><td>Find</td><td>Finds a global variable and displays it at the top of the Name field. To find a variable, type the name in the text field next to the Find button, and the click Find.

If you do not remember the complete name of the variable, you can type part of the name and the wildcard * to retrieve all variables with the specified string. For instance, to find all public and all changed private globals beginning with dbg, type dbg* in the Find text box and click Find.

Note: The variable name is case-sensitive.</td></tr>
</table>

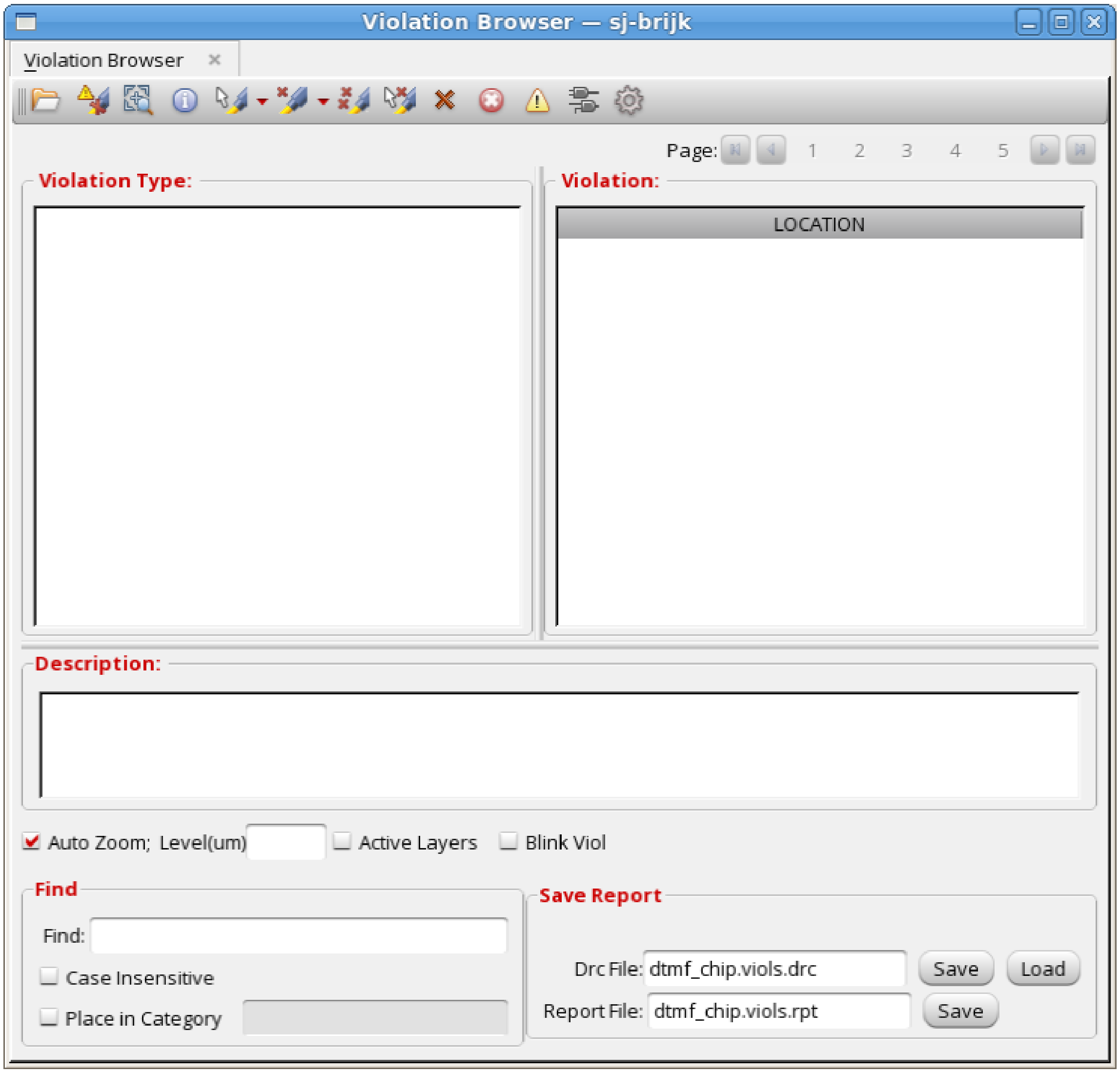
Violation Browser

Use the Violation Browser to display violations and lithography hotspots, mark violation markers as false or true, delete violation markers, and specify a report file.

The Violation Browser also provides access to the following forms:

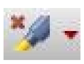
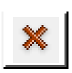
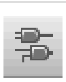
- Violation Browser Settings
- Load Violation Report

To open Violation Browser, choose *Tools - Violation Browser*.



Violation Browser Fields and Options

	*Load Violation Report* - Opens the Load Violation Report form. Use this form to load a violation marker file and then view the markers in the Violation Browser.

	*Clear Violation* - Clears all the violation markers in your design.
	*Fit Violation* - Displays the violation within the design display area.
	*Attribute Editor* - Opens the *Attribute Editor* and populates it with the highlighted violations. Double click on a violation to update fields in the Attribute Editor.
	*Highlight Selected* - Highlights the selected violation(s) in the design display area as well as in the *Violation* list on the right pane of the Violation Browser. You can select an individual violation in the right pane of the Violation Browser or select violations by type or subtype in the left pane of the browser. To highlight a selected violation or a selected type/subtype of violations, select the highlight color from the color palette and then click the *Highlight Selected* button.
	*Clear Highlight* - Removes the highlight from the selected violation in the design display area and enables to select the highlight color from the color palette again.
	*Clear All Highlight* - Removes all the highlight from the selected violation or selected type/subtype of violations in the design display area.
	*Clear Selected Highlight* - Removes only the last selected highlight from the selected violation or selected type/subtype of violations in the design display area.
	*Delete Violations* - Deletes all selected violations from the design database. Markers are also removed from the design display area and the list of violations.
	*Mark Violations as False* - Marks the selected violation as a false violation. These violations are stored in the database as false violations. To view the violations that you mark as false, click  in the Violation Browser, select the *View False Violations* check box in the Violation Browser Settings form, and click *OK*.
	*Mark Violations as True* -- Marks the selected violation as a true violation.
	*Show MSV Violation Schematic* – Displays schematics associated with the highlighted violation in the Schematic Viewer form.
	*Setting* - Opens the Violation Browser Settings form.

Violation Type	Lists the violation types in a hierarchy window. To show or hide a violation, select it in the *Violation* or *Violation Type* window and click the right mouse button. Select *Show* or *Hide* from the pop-up window. The numbers in parentheses after each violation type represent the number of violations of that type displayed in the main window and the total number of violations of that type. The count includes true and false violations. For example, if *Verify - Connectivity - Open (479/503)* means that there are 503 Open violations and 479 of those violations are shown the main window.
Violation	For the highlighted *Violation Type*, displays the names of the objects with violation markers and their locations.
Description	Displays the layer, bounding box, and Non-Default Rule (NDR) name for the violation. **Note:** Layer is not included for placement violations. You can select text in the *Description* text box and copy and paste it to another window. You cannot edit text in the *Description* text box.
Auto Zoom	Automatically zooms in to the selected violations as you browse through the violations. This check box is selected by default.
Zoom Level (um)	Controls the level of zoom for Auto Zoom. When you specify the zoom level, Violation Browser uses the same value for all listed violations so that you do not have to zoom out each time you select a violation.
Active Layers	Keeps only the violation layer(s) visible when you zoom into a violation. If this check box is not selected, the Auto Zoom mode displays layers as per the layer visibility settings on the Layer Control bar.
Only Show Selected	Displays markers for only selected violations. This option is useful if there are many violations in the design. By selecting this option, you can turn off other violation makers in the main window and focus on only the violations you have selected in the browser.
Blink Viol	Makes the marker for the selected violation blink in the main window.
Find	Searches for the specified text and highlights it in the *Violation* window. This field recognizes pattern matching, so you can type `*153*` to search for all objects with the string `153` as part of their *LOCATION*. Press *Enter* to find the specified text.

Case Insensitive	Specifies whether the text in the *Find* text entry box is case sensitive.
Place in Category	Creates a category in the *Violation Type* window and adds the highlighted object to the category. Categories are not saved.
Drc File - Save	Opens a form that allows you to specify the path and name for saving the DRC file. This is equivalent to using the `saveDrc` command.
Drc File - Load	Opens a form in which you can browse and select the DRC file to be loaded. This is equivalent to using the `loadDrc -incremental` command.
Report File - Save	Specifies the report file that contains all the violation information. The browser and the report file list the violations in the same order.

Related Text Commands

- `checkPlace`
- `createMarker`
- `violationBrowser`
- `violationBrowserReport`

Related Topics

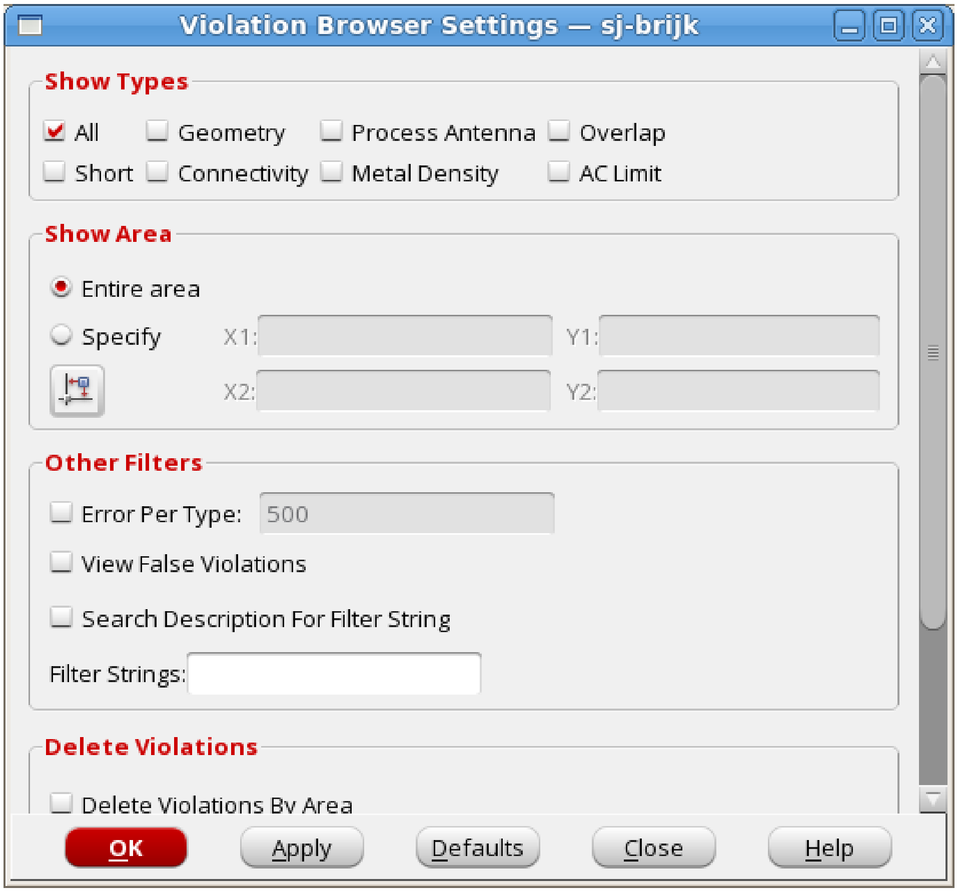
For more information on using the Violation Browser, see the following topic in the Identifying and Viewing Violations chapter of the *Innovus User Guide*:

- Viewing Violations with the Violation Browser

Violation Browser Settings

Use the Violation Browser Settings form to specify the settings for displaying violations and lithography hotspots.

- Choose *Tools - Violation Browser* and click the  button.



Violation Browser - Settings Fields and Options

Show Types	Lists the types of violations to display or hide in the Violation Browser. Select one or more of the following options:	
	All	Displays all violations.
	Geometry	Displays geometry violations.
	Process Antenna	Displays process antenna violations.
	Overlap	Displays overlap violations.
	Short	Displays short violations.
	Connectivity	Displays connectivity violations.

	Metal Density	Displays metal density violations.
	AC Limit	Displays AC limit violations.
Show Area	Displays violations in the entire area or a specified portion of the area. Specify the portion of the area by using one of the following methods: • Using the *Draw* button and your mouse to create a rectangular area in the design. The software displays the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields. • Manually enter the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields.	
Other Filters	Specify additional conditions by selecting one or more of the following options:	
	Error Per Type	Specifies a limit for the number of violations parsed by the browser for each violation type. If this check box is not selected, the Violation Browser parses and displays all violations.
	View False Violations	
		Displays violations that you have marked as false.
	Search Description For Filter String	
		Searches for text in the violation message (in the bottom portion of the Violation Browser window) and the violation description (in the top portion of the Violation Browser window).
	Filter Strings	

		Specifies a text string for filtering violations. When you specify a text string, the Violation Browser searches the message of each violation and displays only the violations whose messages match the search conditions. To specify a list of strings, separate each string with a space. To specify a literal string with space in it, enclose the string in double quotation marks. For example, you can specify strings such as the following: • `M5` • `(600, 500)` • `M3 (700, 400)` • `"Pin of Net"` You can specify the AND, OR, and NOT conditions with the search strings. Use: • `&&` between strings to specify the AND condition. • `||` between strings to specify the OR condition. • ! before a string to specify the NOT condition.
Delete Violations	Enables you to delete all violations or delete violations in the specified area only.	
Delete Violations By Area		
	Enables you to delete violations in the area you specify on this form or the area you select with the mouse.	
	Entire area	Deletes the types of violations specified in the entire core design area.
	Specify	Specifies an area from which to delete violations. Only the types of violations specified by this form are deleted.
	Draw …	Lets you use the mouse to outline an area from which to delete violations.

Related Text Commands

- `createMarker`

- violationBrowser
- violationBrowserReport

Related Topics

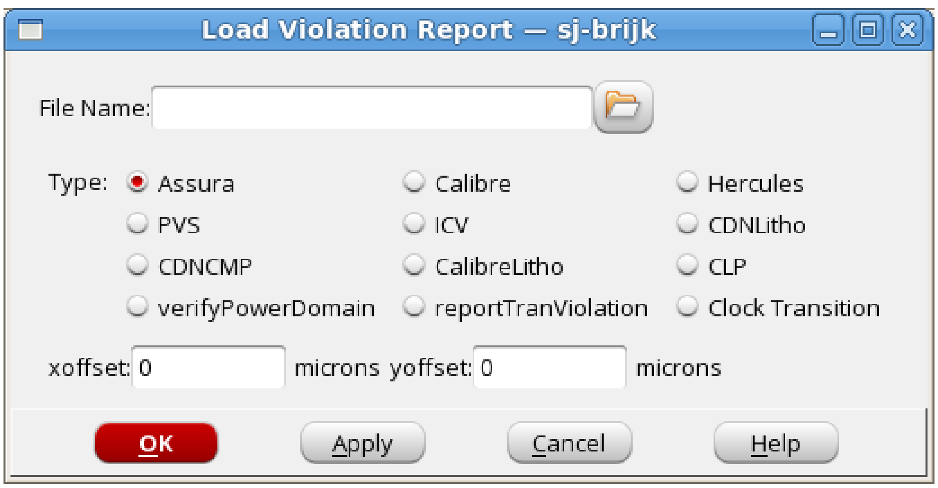
For more information on using the Violation Browser, see the following topic in the Identifying and Viewing Violations chapter of the *Innovus User Guide*:

- Viewing Violations with the Violation Browser

Load Violation Report

Use the Load Violation Report form to load a violation marker file or a hotspot interface format (HIF) file and create markers that the Innovus software can interpret. After you load the file, you can view the markers in the Violation Browser. The Auto Query feature displays the rule names for the markers.

- Choose *Tools - Violation Browser* and click the *Load Violation Report* button.



Load Violation Report Fields and Options

File Name	Specifies the marker file to load.

Type	Specifies the type of marker file. The following file types contain violation markers: • *Assura* - For Assura violations • *Calibre* - For Calibre violations • *Hercules* - For Hercules violations • *ICV* - For ICValidator violations • *Pegasus* - For Pegasus violations • *PVS* - For PVS violations • *CDNCMP* - For Cadence CMP Predictor (CCP) violations • *CLP*, *verifyPowerDomain*, and *Clock Transition* - For low power violations • *reportTranViolation* - For DRV transition violations The following types contain hotspot markers, which are used to identify areas susceptible to lithography problems: • *CDNLitho* (for LPA and NanoRoute litho HIF files) • *CalibreLitho*
xoffset	Specifies the X offset. When you specify the X and Y offsets, Violation Browser displays the violations at the correct coordinates after accounting for the offsets.
yoffset	Specifies the Y offset, which Violation Browser takes into account to displays violations at the correct coordinates.

Related Text Commands

`loadViolationReport` `read_markers`

Related Topics

For more information on using the Violation Browser, see the following topic in the Identifying and Viewing Violations chapter of the *Innovus User Guide*:

- Viewing Violations with the Violation Browser

Clear Violation

Use the *Clear Violation* button in the Violation Browser to clear all the violation markers in your design.

- Choose *Tools - Violation Browser* and click the *Clear Violation* button.

There is no GUI form for this command.

Related Text Commands

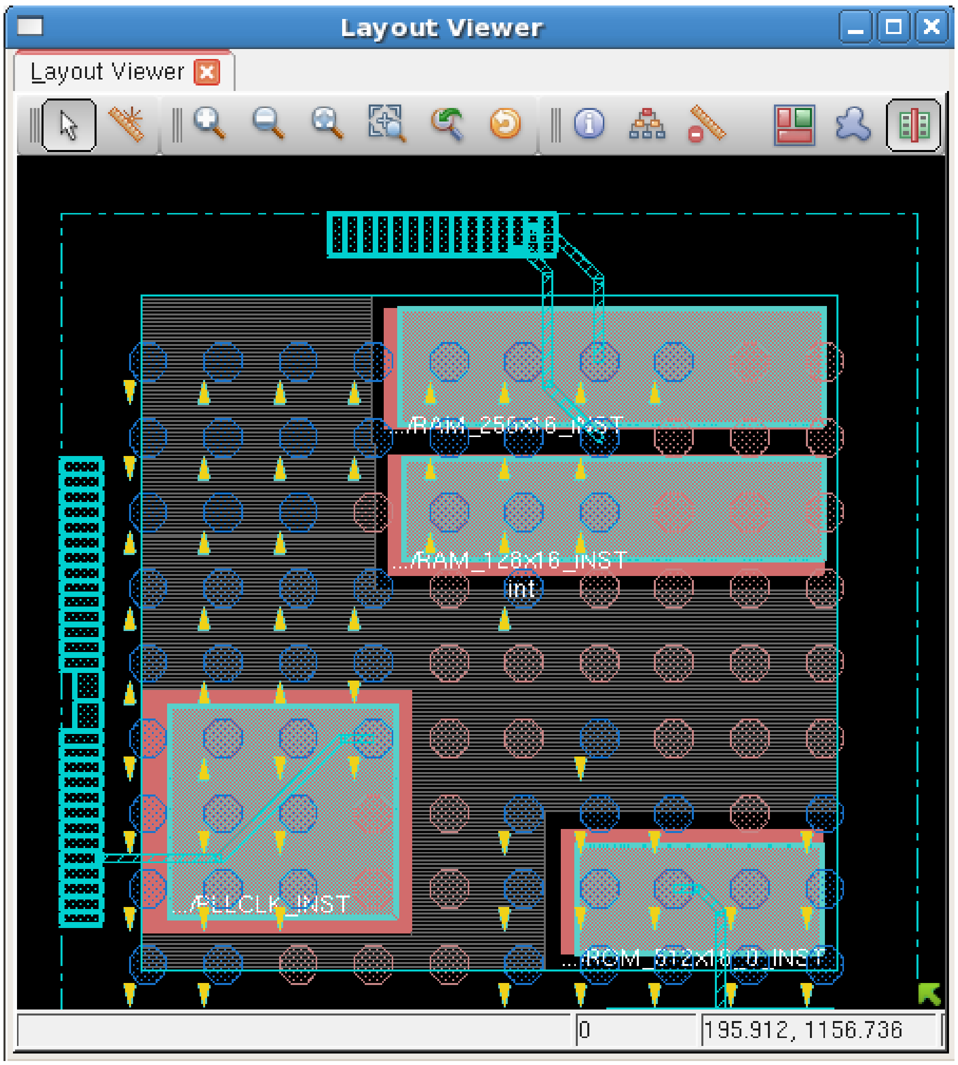
There are no related text commands. This feature is available only through the *Innovus* Tools menu.

Layout Viewer

Use the *Layout Viewer* menu item to open the layout in a view-only window. You can launch multiple view-only windows in a single Innovus session. This is useful when debugging as it allows you to view and zoom into different portions of a design simultaneously.

The Layout Viewer window supports all viewing related features, such as *Zoom* and *Pan*. In addition, it supports functions and tools that do not modify the design, such as Attribute Editor and Design Browser.

- Choose *Tools - Layout Viewer*.



Layout Viewer Tool Widgets

You can use the widgets in Layout Viewer to navigate through displays, open tools, and make selections.

Widget	Description
	Select - Selects an object in the design display area.
	Create Ruler - Click this widget, then left-click in the design display area and drag the mouse to add a ruler (in micrometers), and left-click again to end the ruler. To move the ruler, click and drag it to a new location. Click the ruler again to keep it in the new location.
	In by 2 - Click this widget to display a smaller area of the design in greater detail. Each click zooms in two levels.
	Out by 2 - Click this widget to display a larger area of the design in less detail. Each click zooms out two levels.
	Fit - Click this widget to display the entire placed design within the design display area.
	Selected - Zooms in on a highlighted selection.
	Previous - Click this widget to toggle the display between the previous location/zoom level and the current location/zoom level.
	Redraw - Refreshes the Layout Viewer display.
	Attribute Editor - Opens the Attribute Editor for the highlighted object.
	Design Browser - Opens the Design Browser form.
	Clear All Rulers - Clears all rulers from the display area. **Note**: To remove a single ruler, place the mouse cursor over the ruler and press `Delete`.
	Floorplan View - Switches to the Floorplan view of the design.
	Amoeba View - Switches to the Amoeba view of the design.
	Physical View - Switches to the Physical view of the design.

Cell Viewer

The Cell Viewer provides an artwork window for viewing the following objects:

- any LEF library cell
- any via cell
- any OpenAccess database cell view
- abstract view of any partition in the design
- power grid view

The Cell Viewer displays the content from the Innovus library database. The Cell Viewer provides a convenient way to view the content of a cell, cell view or partition without having to zoom into the design.

The Cell Viewer has the following tabs:

- Cell Viewer - LEF
- Cell Viewer - Via
- Cell Viewer - OA
- Cell Viewer - Ptn
- Cell Viewer - PGV

Cell Viewer Widgets

The Cell Viewer supports the following widgets: Zoom In, Zoom Out, Fit, View Last, Redraw, Clear All Rulers, Select and Ruler.

For a description of the these widgets, see the Toolbar Widgets section in The Main Window chapter of this document.

Setting Layer Visibility Preferences

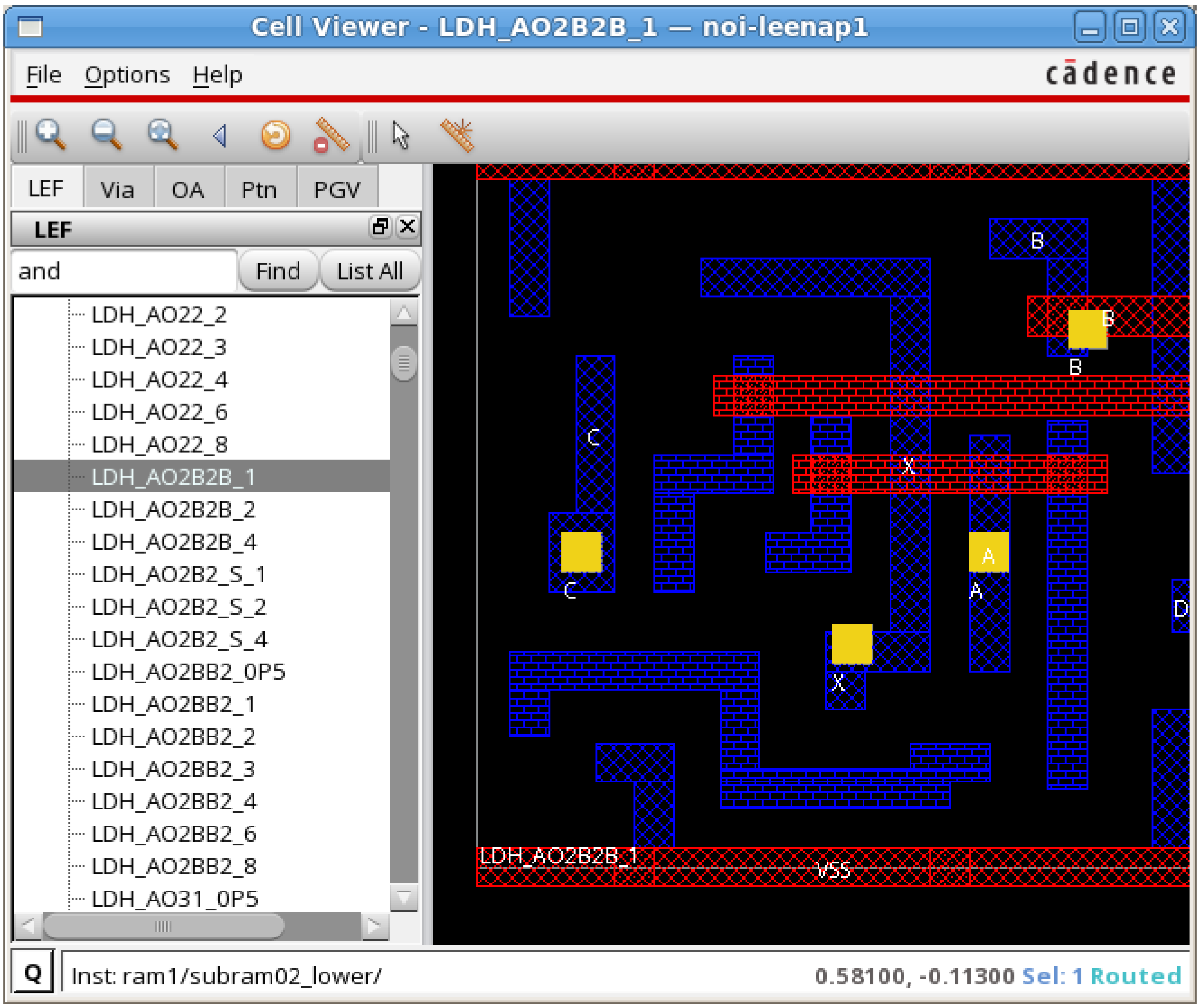
Use the Layer Control Bar in the main window to set the visibility of layers in the Cell Viewer. For example, you can turn off the visibility of the layer METAL 3. For more information on the Layer Control Bar, see the Layer Control Bar section in The Main Window chapter of this document.

Related Commands

- gui_close_cell_view
- gui_open_cell_view

Cell Viewer - LEF

- Choose *Tools - Cell Viewer*, and click on the LEF page if it is not already selected.

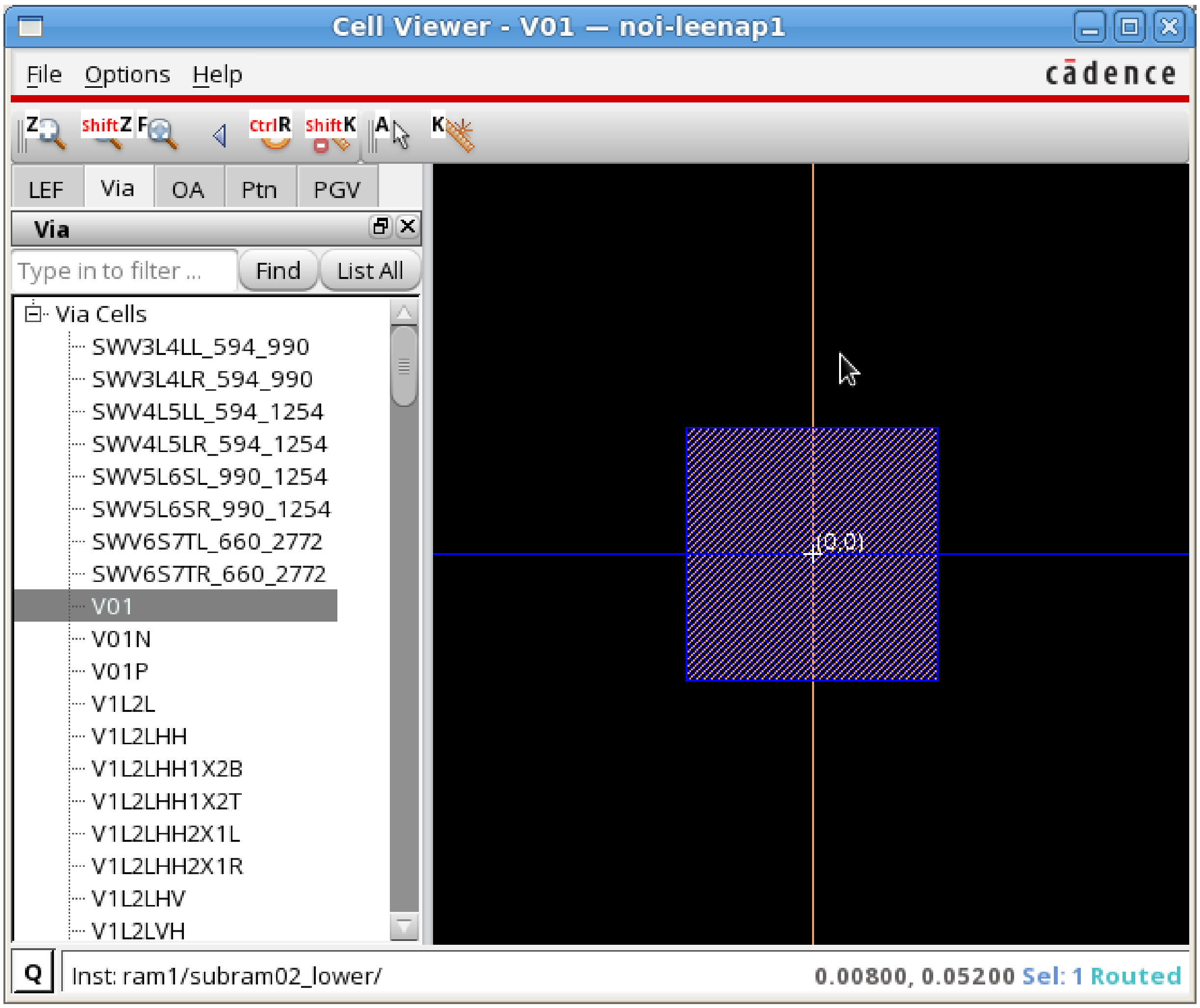


The LEF page displays the details of library cells using the information in the LEF file.

You can navigate to a cell using the Library Browser, which is in the left side of the Cell Viewer. The details of the cell are displayed in the Display Area, which is in the right side of the Cell Viewer.

Cell Viewer - Via

- Choose *Tools - Cell Viewer*, and click on the Via page.

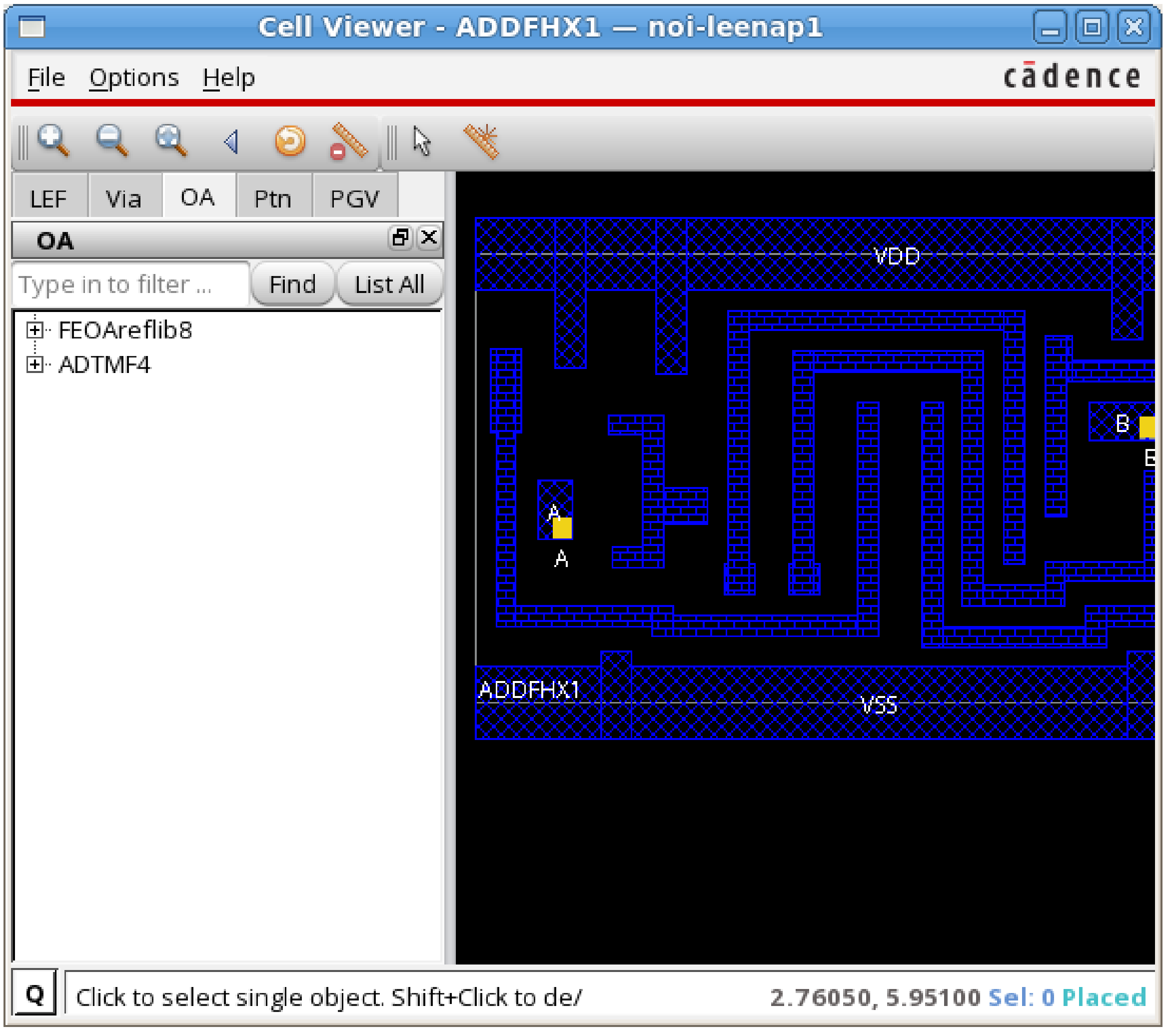


The Via page displays the details of via cells in the design.

You can navigate to a cell using the Library Browser, which is in the left side of the Cell Viewer. The details of the cell are displayed in the Display Area, which is in the right side of the Cell Viewer.

Cell Viewer - OA

- Choose *Tools - Cell Viewer*, and click on the OA page.

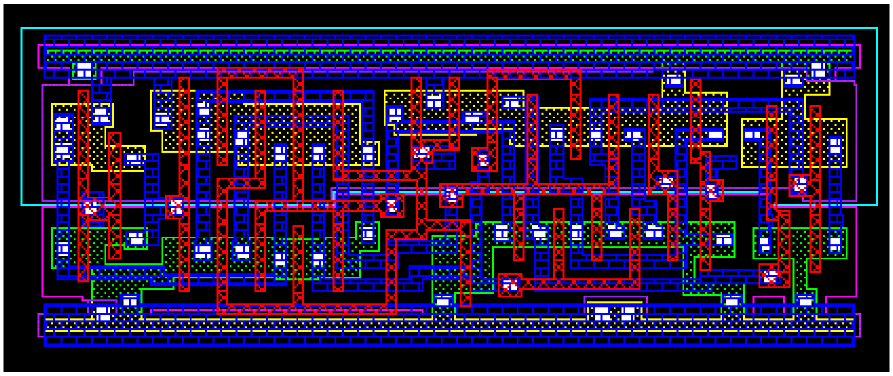


You can view an OA cell in the following modes, if available:

- Layout
- Abstract

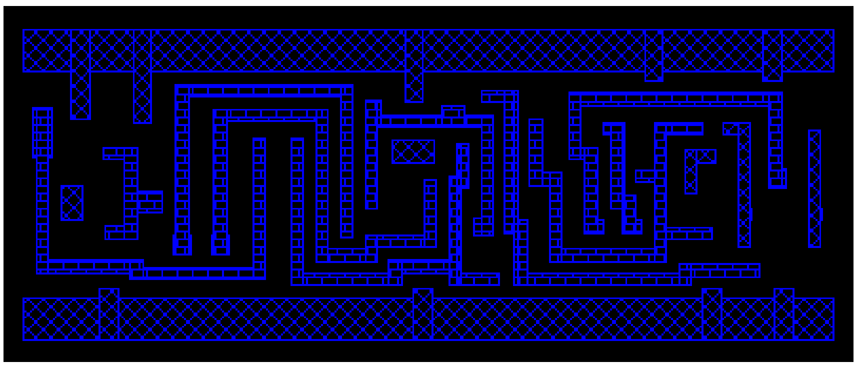
OA-Layout View

- In the Library Browser, select the OA cell, and then click Layout.



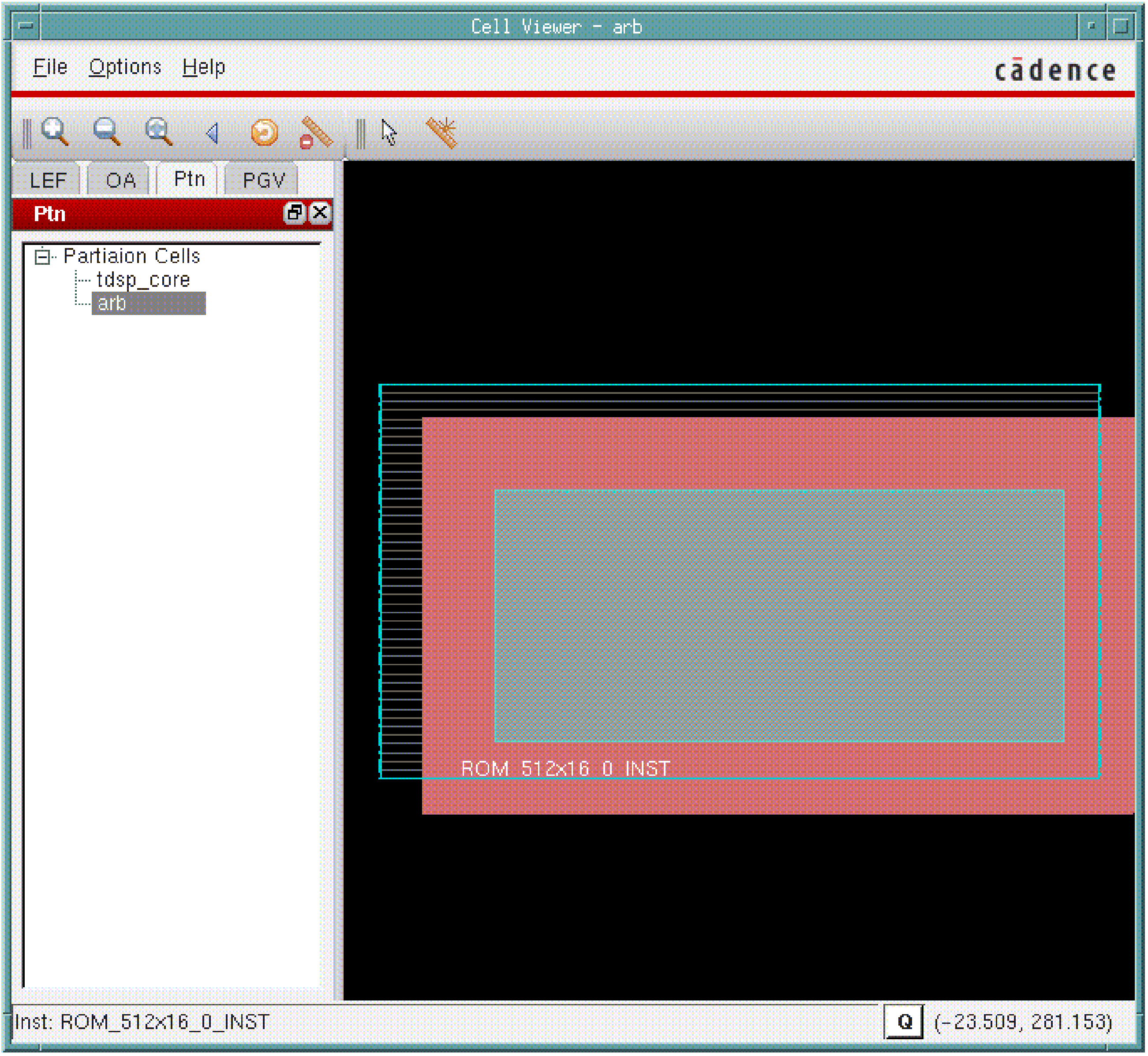
OA-Abstract View

- In the Library Browser, select the OA cell, and then click Abstract.



Cell Viewer - Ptn

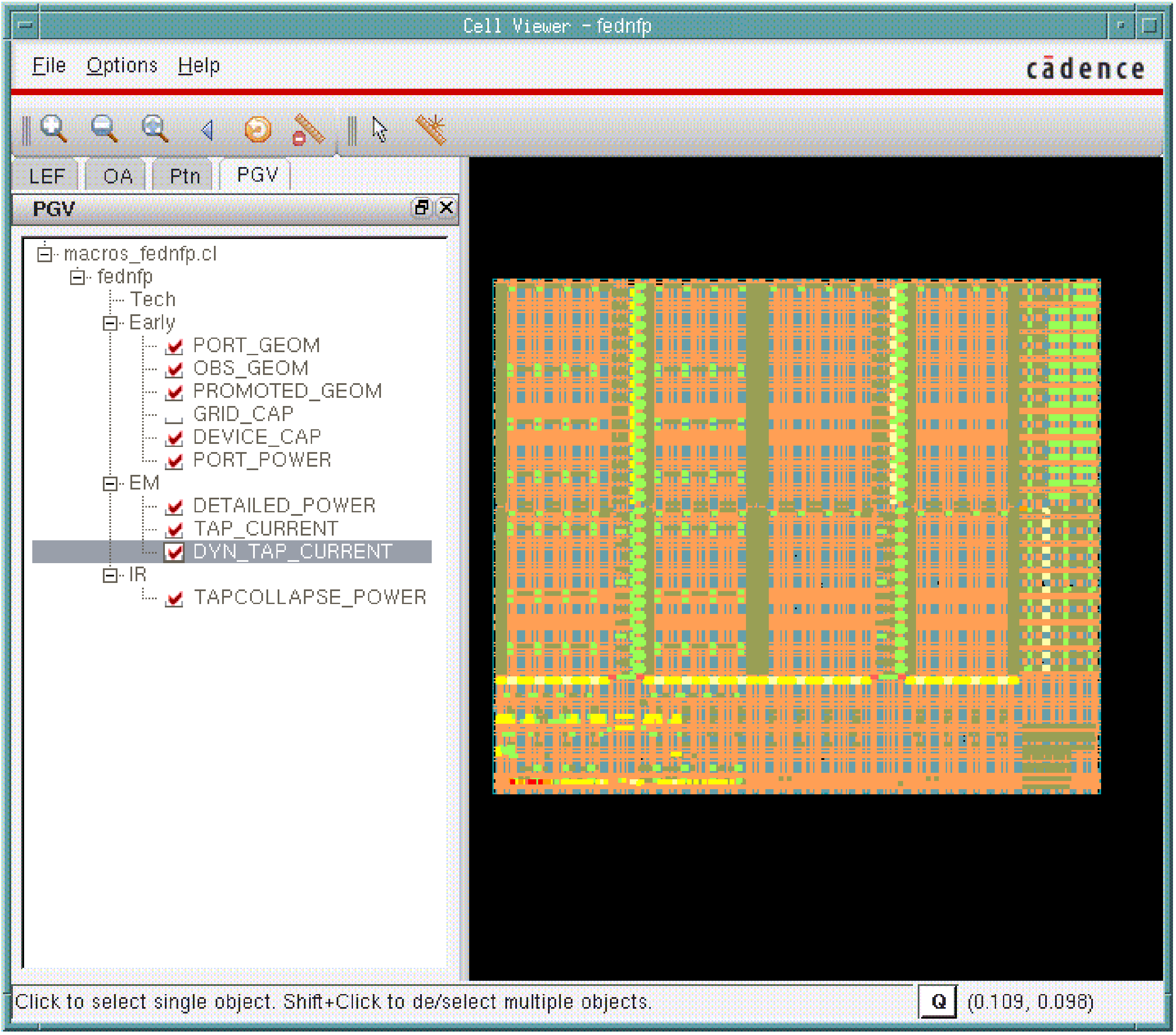
- Choose *Tools - Cell Viewer*, and click on the Ptn page.



Use the Ptn page to display the abstract of any partition in the design. You can navigate to a partition through the Library Browser in the left side of the Cell Viewer.

Cell Viewer - PGV

- Choose *Tools - Cell Viewer*, and click on the PGV page.



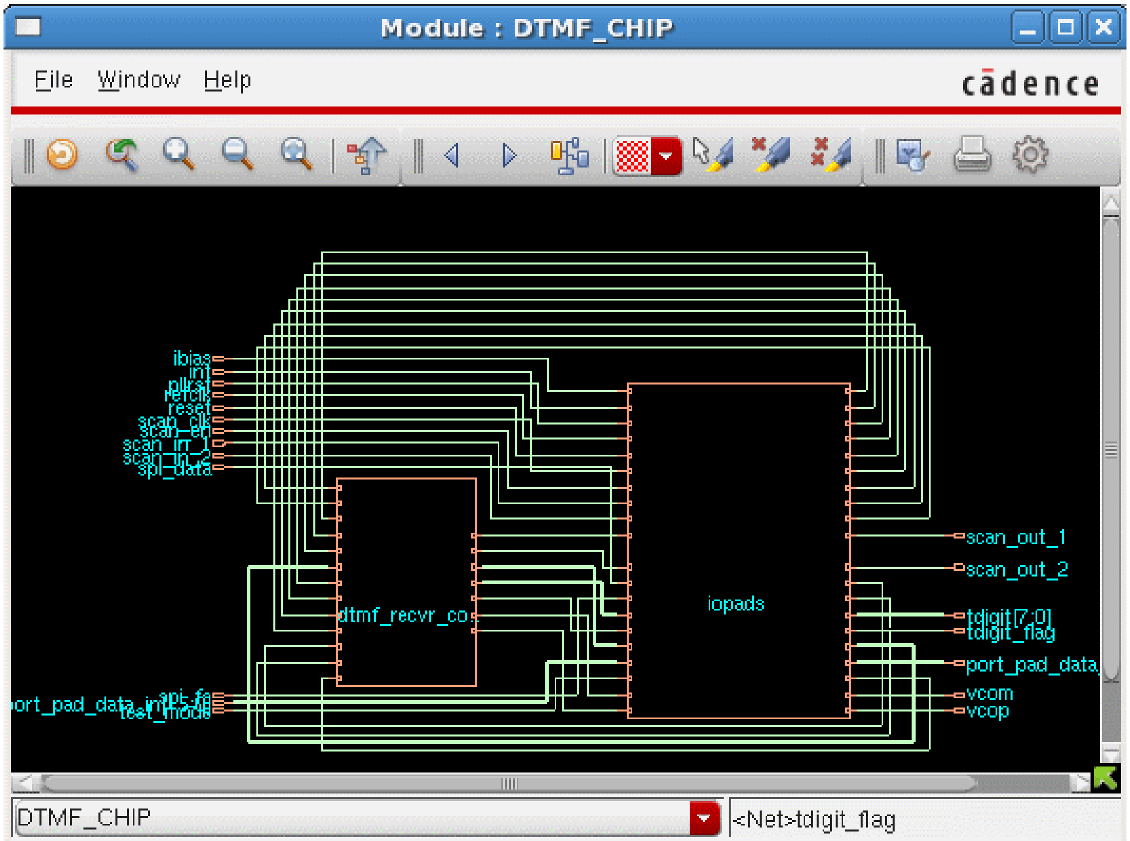
Use the PGV page to view and debug power-grid libraries. This form allows you to take a physical layout and overlay it with a power-grid resistor network extracted by Power-Grid Library Generator. You can expand a cell to view the default views corresponding to each PGV type (Tech, Early, EM, and IR).

Schematic Viewer

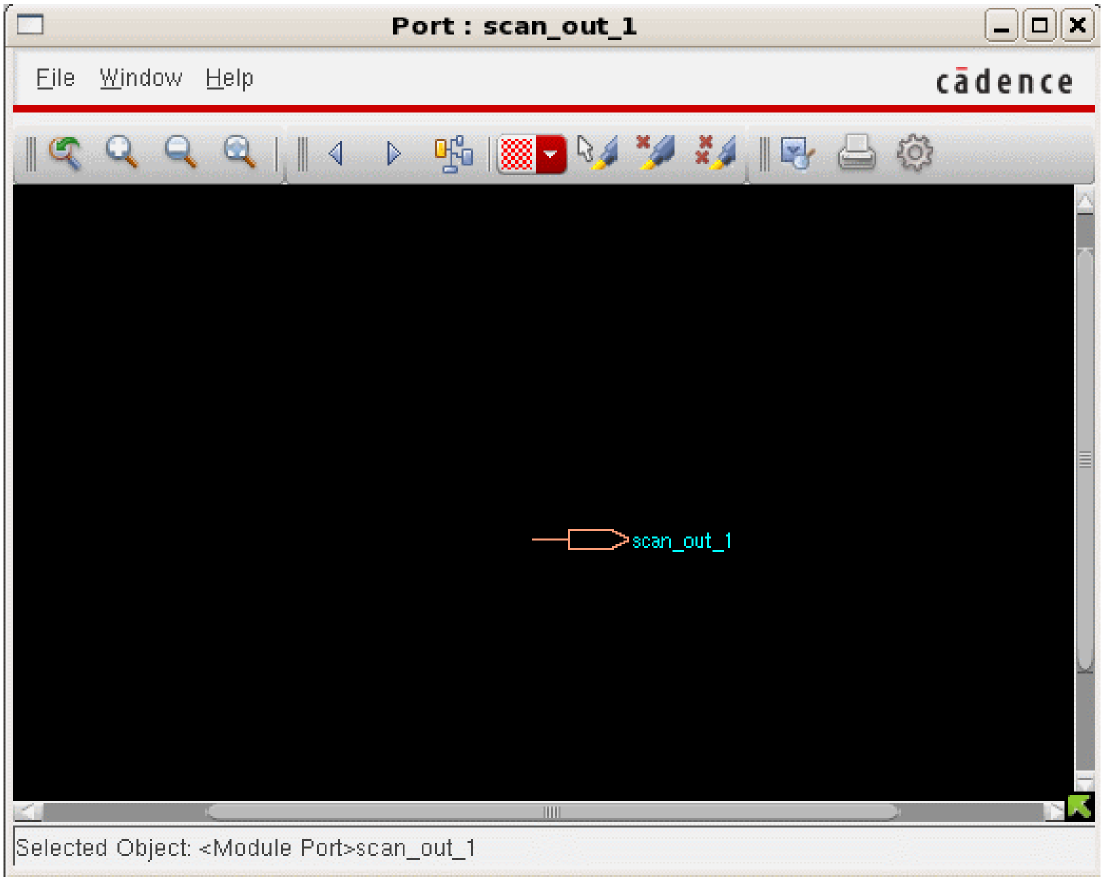
Use the Schematic Viewer with the Design Browser to explore a design's connectivity, the relationship of modules and instances, and design changes, such as CTS, OPT, and ECO. You can use the `h` bindkey to cross-probe from the Schematic Viewer to the main window display. Using this bindkey, you can highlight the selected net or instance in the main window. This gives you flexibility and immediate feedback to debug and diagnose your design.

The Schematic Viewer has two main views:

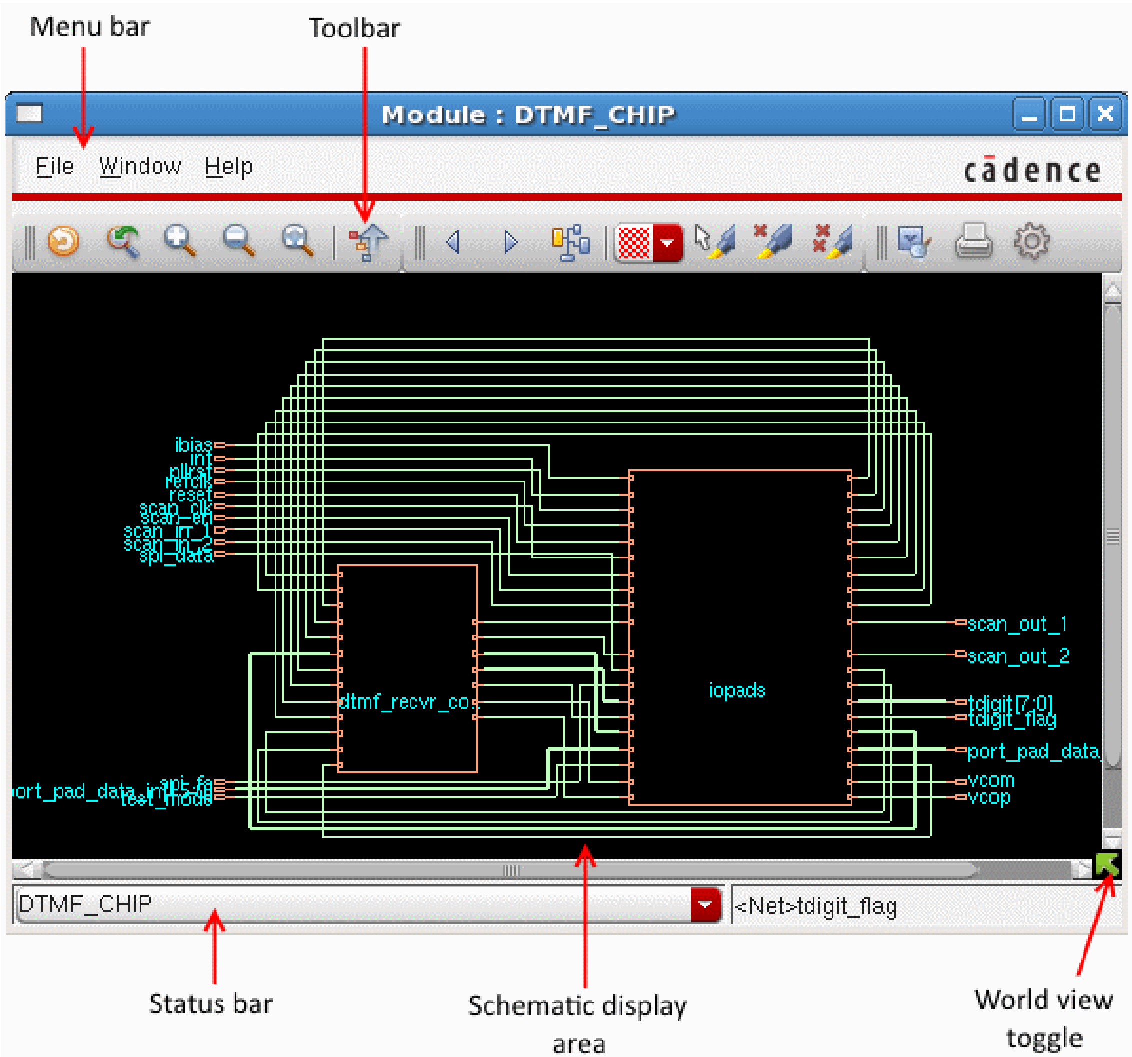
- Hierarchical view - To open Schematic Viewer in Hierarchical view:
- Choose *Tools* - *Schematic Viewer* from the main window.
- Select a module, instance, net, or pin in Design Browser and click the *Show Hierarchical Schematic* widget.
- Select an MSV violation in Violation Browser and click the *Show MSV Violation Schematic* widget.
- In the Timing Debug environment (*Timing* - *Debug Timing*)
- Double-click a path on the timing critical path list to open the Timing Analyzer form and select the Schematic tab to change the view to schematic.
- Select a path on the timing critical path list and click the *Schematic* icon.



- Flattened view - To open Schematic Viewer in Flattened view, select an instance, net, or pin in Design Browser and click the *Show Instance Based Schematic* widget.


Port : scan_out_1
File
Window
Help
cādence
scan_out_1
Selected Object: <Module Port>scan_out_1

Schematic Viewer Components



Menu Bar

- File Menu
- Window Menu

File Menu

The File menu enables you to print schematics and close the Schematic Viewer window.

Options	**Description**
Preferences	Opens the Preferences form where you can set *Display*, *Color*, and *Font* preferences.
Print	Opens the Print Schematic form where you can choose printer options.
Quit	Closes the Schematic Viewer window.

Window Menu

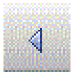
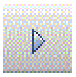
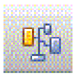
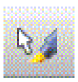
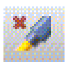
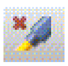
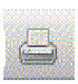
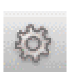
The Windows menu lists all the active Schematic viewer windows for your session. Click on a window name to bring it to the front of your screen.

Choose *Cascade Window* to refresh your desktop and display the main window on top with all other open windows in a cascading view to the left of the main window.

Toolbar

The Schematic Viewer toolbar provides a quick way to access the most commonly used commands. This section describes the toolbar items, which are available for flattened and module schematics, except where noted.

Icon	**Action**	**Description**
	Reload View	Reloads or refreshes the current view.
	Last View	Toggles the display between the previous location or zoom level and the current location or zoom level.
	Zoom In	Displays a smaller area of the schematic in greater detail. Each click zooms in one level. The equivalent bindkey is `Z` (`Shift-Z`).
	Zoom Out	Displays a larger area of the schematic in less detail. Each click zooms out one level. The equivalent bindkey is `z`.
	Zoom to Full Window	Displays the entire schematic within the display area. The equivalent bindkey is `f`.
	Push View Up	Displays the parent-level hierarchy. To push the view up to a higher-level schematic, select an object in the schematic display area and click this widget.

	Trace Driver	Traces all possible drivers of the selected object and highlights them in the schematic display area. The default highlight color for drivers is yellow.
	Trace Load	Traces all possible loads of the seobject and highlights them in the schematic display area. The default highlight color for loads is red.
	Trace Connectivity	Traces all possible drivers and loads of the selected object and highlights connectivity from the object's drivers to its loads. The default highlight colors for drivers and loads are yellow and red, respectively.
	Edit Highlight Color	Allows you to select a highlight color from the available choices in the drop-down menu.
	Highlight Selected	Highlights selected object in the schematic display area.
	Dehighlight	Dehighlights an object in the schematic display area.
	Dehighlight All	Dehighlights all objects in the schematic display area.
	Find	Click this widget to open the Find Schematic Object form to find and highlight a specific object in the schematic display area.
	Print	Opens the Print Schematic form, which enables you to print the required schematic display.
	Preferences	Opens the Preferences form where you can set *Display*, *Color*, and *Font* preferences.

Schematic Display Area

The schematic display area constitutes the major portion of the Schematic Viewer window. The schematics of the selected object is displayed here in flattened or hierarchical view. To change the default display properties for objects in the display area, use the *Color* tab on the Preferences form.

World View Window

The world view window identifies the location of the current view in the schematic display area, relative to the entire area. The world view is identified by the pink crossbox. When you display an entire schematic in the area, the crossbox encompasses the world view window. When you zoom and pan through the schematic in the display area, the crossbox identifies where you are relative to the entire schematic.

- To define a new world view, left-click and drag the mouse to create a new crossbox in the world view window.
- To pan left, right, up, or down in the schematic display, right-click and drag the crossbox in the world view window.

Status Bar

The *Status Bar* is located at the bottom of the Schematic Viewer. When you select or hover over an object, this bar displays the object type, name, and ID number.

Context Menu

To access the context menu, right-click an object in the Schematic Viewer window. The options available in context menu varies depending on the:

- Current view of Schematic Viewer - Hierarchical or Flattened
- Object you have selected in the schematic display area

Hierarchical View Context Menu

The following table describes the options that are available in the context menu of the Schematic viewer when it is opened in Hierarchical view.

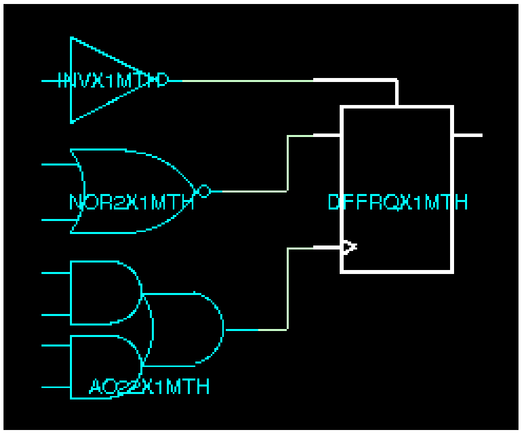
Options	Description
Attribute Editor	Opens the Attribute Editor for the selected object.
Design Browser	Opens the object in Design Browser.
Highlight	Highlights the selected object in the color or pattern you select from the submenu.
Dehighlight	Removes highlight.
Copy Name	Copies the object name.

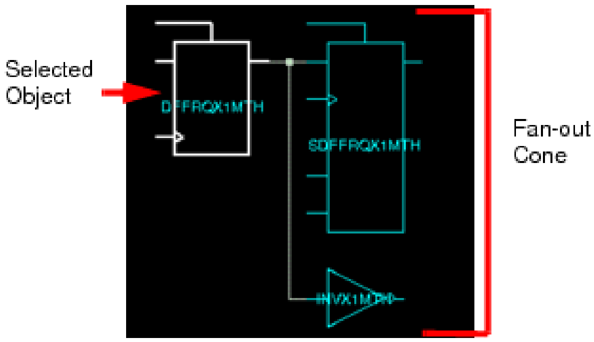
Open In	Allows you to open selected object in one of the following: • *Schematic Viewer (new)* • *Schematic Viewer (cone)* • *Schematic Viewer (cone append)*
Color Net Segment	Opens the Select Color form from which you can select a different color for the net segment. This option is available only if you right-click a net in the display area.
Open Next Level Instance View	Displays next-level views for instances. This option is available only if you right-click an instance in the display area.
Close Next Level Instance View	Closes a next-level instance view. This option is available only if you right-click an instance in the display area.
Trace Previous Driver	Traces the previous driver of the selected port or instance pin. This option is available only if you right-click a port or instance pin in the display area.
Trace Next Load	Traces the next load of the selected port or instance pin. This option is available only if you right-click a port or instance pin in the display area.
Port to Port Trace	Traces all connections to and from a port and highlights them in the color you select in the Select Color form. This option is available only if you right-click a port in the display area.
Show Critical Path	Displays the critical path.
Change Color	Opens a submenu from which you can change the color of the selected object.
Default Color	Resets the selected object type to the default color.

Flattened View Context Menu

The following table describes the options that are available from the Flattened view context menu of Schematic Viewer.

Options	**Description**
Attribute Editor	Opens the Attribute Editor for the selected object.

Design Browser	Opens the object in Design Browser.
Highlight	Highlights the selected object in the color or pattern you select from the submenu.
Dehighlight	Removes highlight.
Copy Name	Copies the object name.
Open In	Allows you to open selected object in one of the following: • *Schematic Viewer (cone)* • *Schematic Viewer (cone append)*
Open Fan-in Cone	Opens the fan-in cone of the selected object. This option is available in the context menu of instances and block ports. 
Close Fan-in Cone	Closes the fan-in cone of an object.

Open Fan-out Cone	Opens the fan-out cone of the selected object. This option is available in the context menu of instances and block ports. 
Close Fan-out Cone	Closes the fan-out cone of an object.
Open Fan-in&out Cone	Opens both the fan-in and fan-out cones of the selected object.
Open Fan-in&out Cone	Closes the fan-in and fan-out cones of an object.

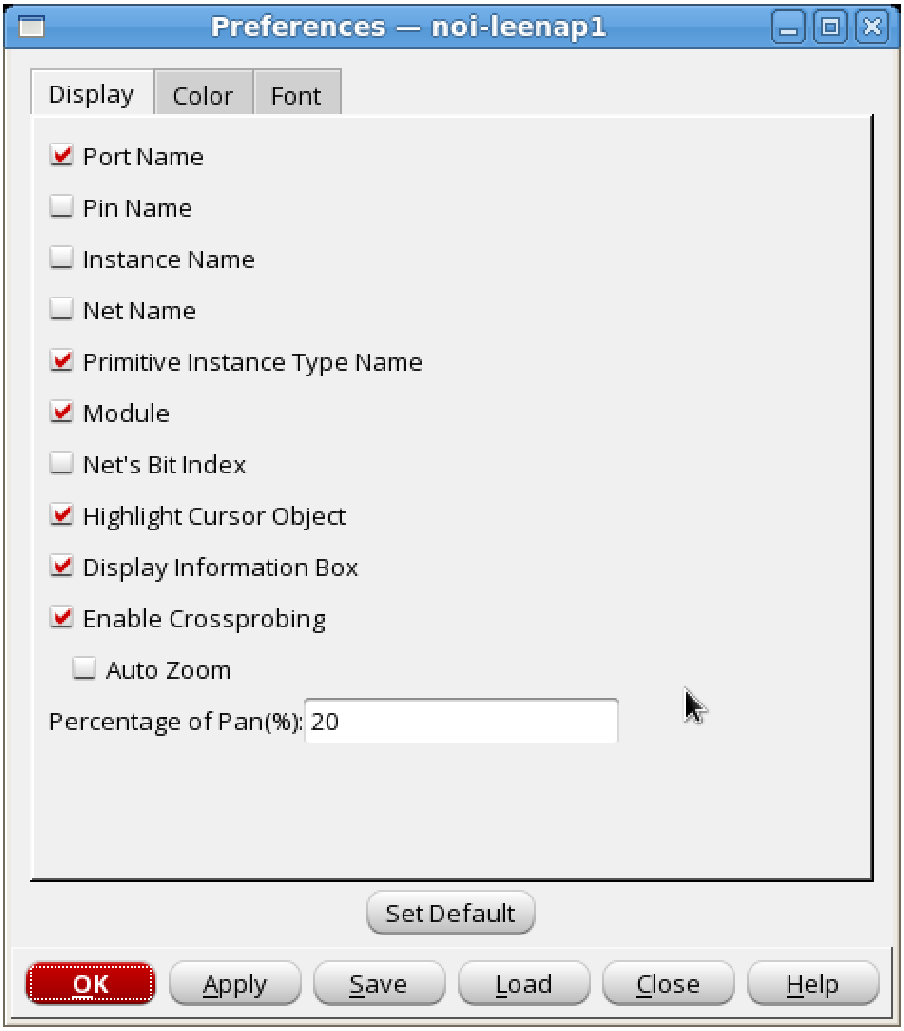
Preferences

The Preferences form enables you to customize the display, colors, and fonts in the schematic display area. It has the following tabs:

- *Display*
- *Color*
- *Font*

Display Tab

Use the *Display* tab to customize the display in the schematic display area.



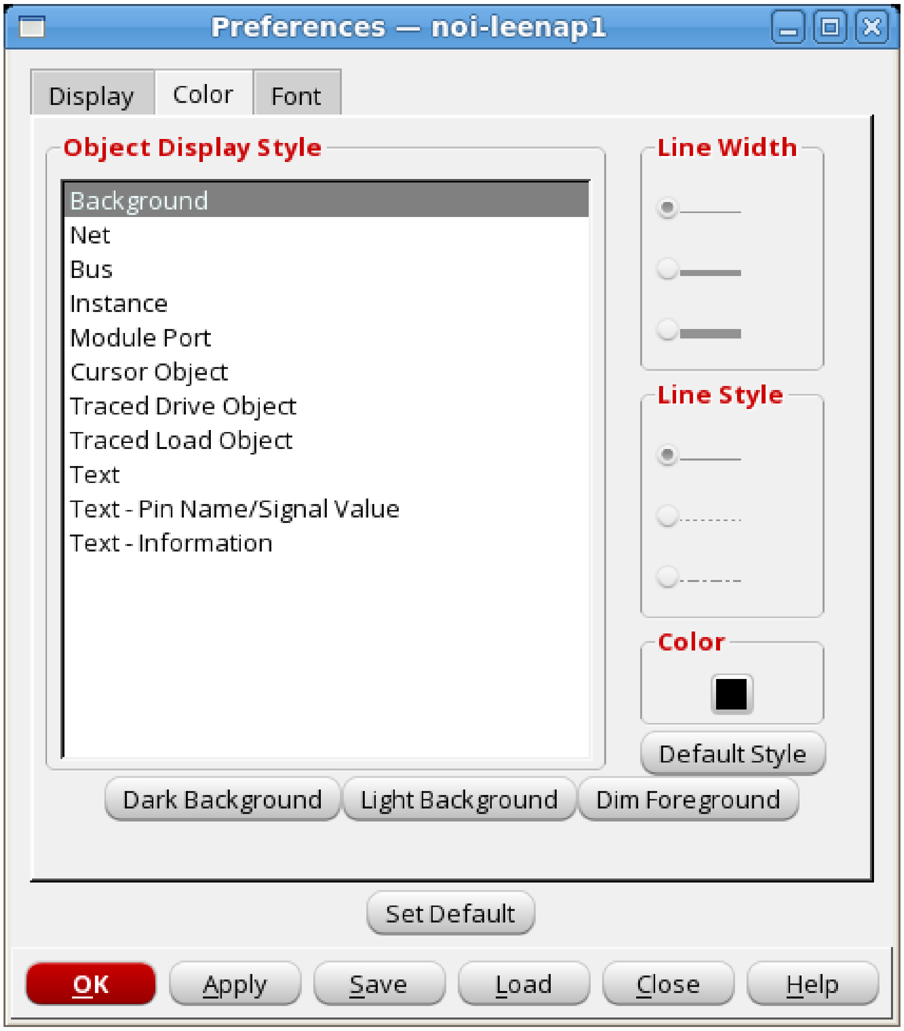
Display Tab Fields and Options

Port Name	Displays instance/block port names in the schematic display area. Deselect this check box if you do not want to display port names. *Default*: Selected
Pin Name	Displays I/O pin names in the schematic display area. *Default*: Unchecked

Instance Name	Displays instance names in the schematic display area. *Default*: Unchecked
Net Name	Displays net names in the schematic display area. *Default*: Unchecked
Primitive Instance Type Name	Displays primitive instance type names. *Default*: Selected
Module	Displays module names in the schematic display area. *Default* : Selected
Net's Bit Index	Displays bit index for nets in the schematic display area. *Default* : Unchecked
Highlight Cursor Object	Highlights objects as you move the cursor over them. *Default*: Selected
Display Information Box	Displays an information box that states the name of the object over which the cursor is currently placed and lists pertinent details about that object. *Default*: Selected
Enable Crossprobing	Allows cross-probing between the main window and Schematic Viewer. Select or highlight any instance in Schematic Viewer; it will be selected/highlighted in the main window automatically. *Default* : Selected
Percentage of Pan	Specifies percentage of pan. *Default*: 20

Color Tab

Use the *Color* tab to change color and line settings for objects in the schematic display area.

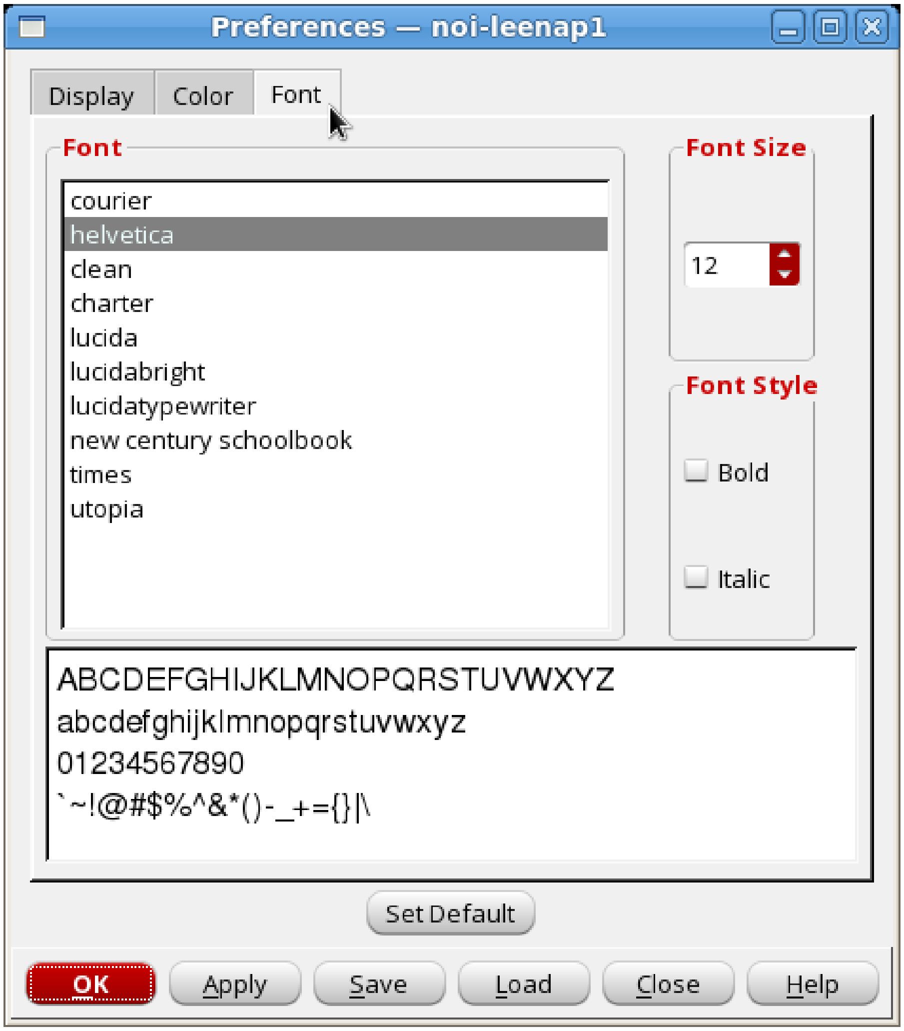

Preferences — noi-leenap1
Display
Color
Font
Object Display Style
Background
Net
Bus
Instance
Module Port
Cursor Object
Traced Drive Object
Traced Load Object
Text
Text - Pin Name/Signal Value
Text - Information
Line Width
Line Style
Color
Default Style
Dark Background
Light Background
Dim Foreground
Set Default
OK
Apply
Save
Load
Close
Help

Color Tab Fields and Options

Object Display Style	Specifies the object type for which you want to change color and line settings. Select any object type from this list and choose appropriate color and line settings, as required.
Line Width	Specifies the line width of the object type selected in *Object Display Style* list box.
Line Style	Specifies the line style of the object type selected in *Object Display Style* list box.
Color	Specifies the color of the object selected in *Object Display Style* list box. Click on the color box to open the Select Color form and choose a new color for the selected object type.
Default Style	Resets the selected object type to the default style.
Dark Background | *Light Background* | *Dim Background*	
	Specifies the background scheme for the *Schematic Display Area*. The default is *Dark Background*.
Set Default	Sets the current selection as the default preference.

Font Tab

Use the *Font* tab to change the font size and style settings for the schematic display.



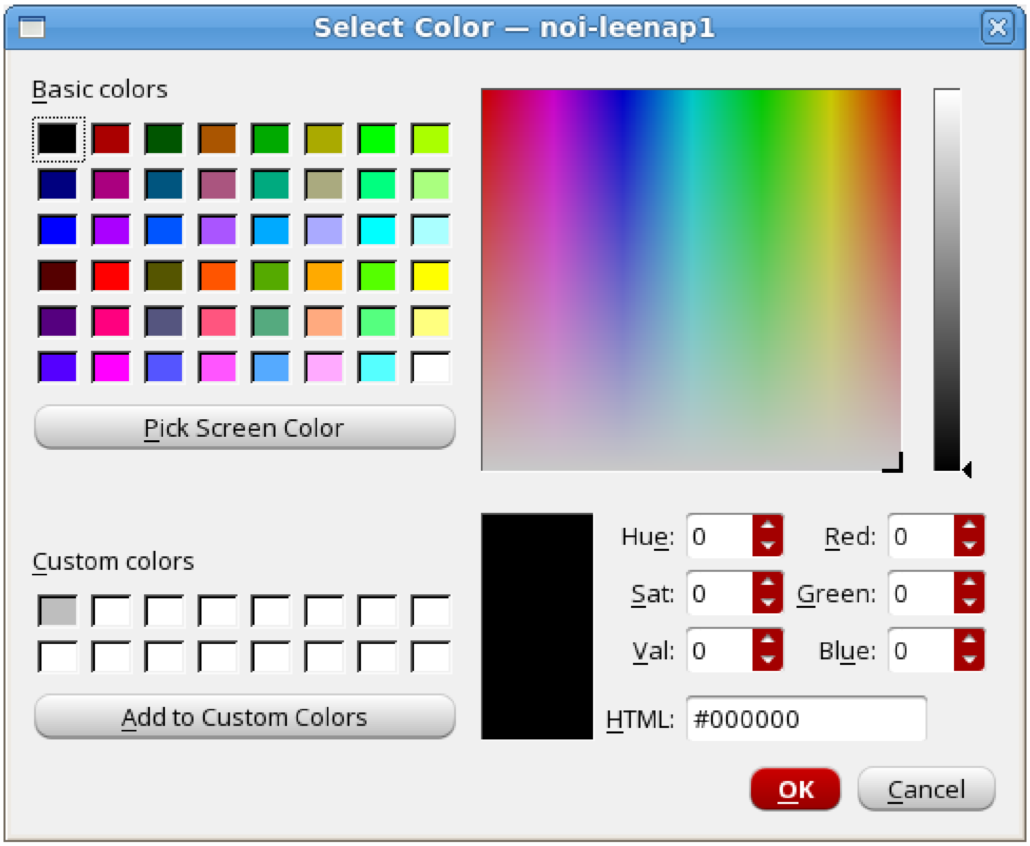
Font Settings Fields and Options

Font	Specifies the font for the text displayed in the schematic display area.
Font Size	Specifies the size of the schematic display font.
Font Style	Specifies the style to be applied to the schematic display font.
Set Default	Sets the current selection as the default preference.

Select Color

Use the Select Color form to change the color of an object in the schematic viewer.

1. Click an object to select it, and choose *View - Change Color*.
2. Select the required color from the color palette and click *OK.*

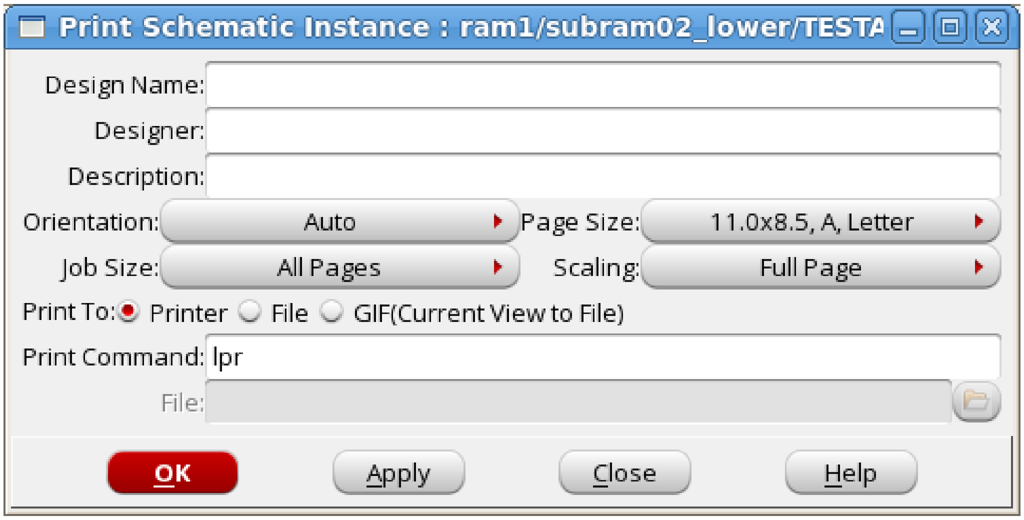


Note: To apply the next available color on the palette, you do not have to re-select the object. Instead, choose *View* - *Next Color*. You can do this repeatedly.

Print Schematic

Use the Print Schematic form to print the schematic in the display area.

- Choose *File* - *Print*.



Print Schematic Fields and Options

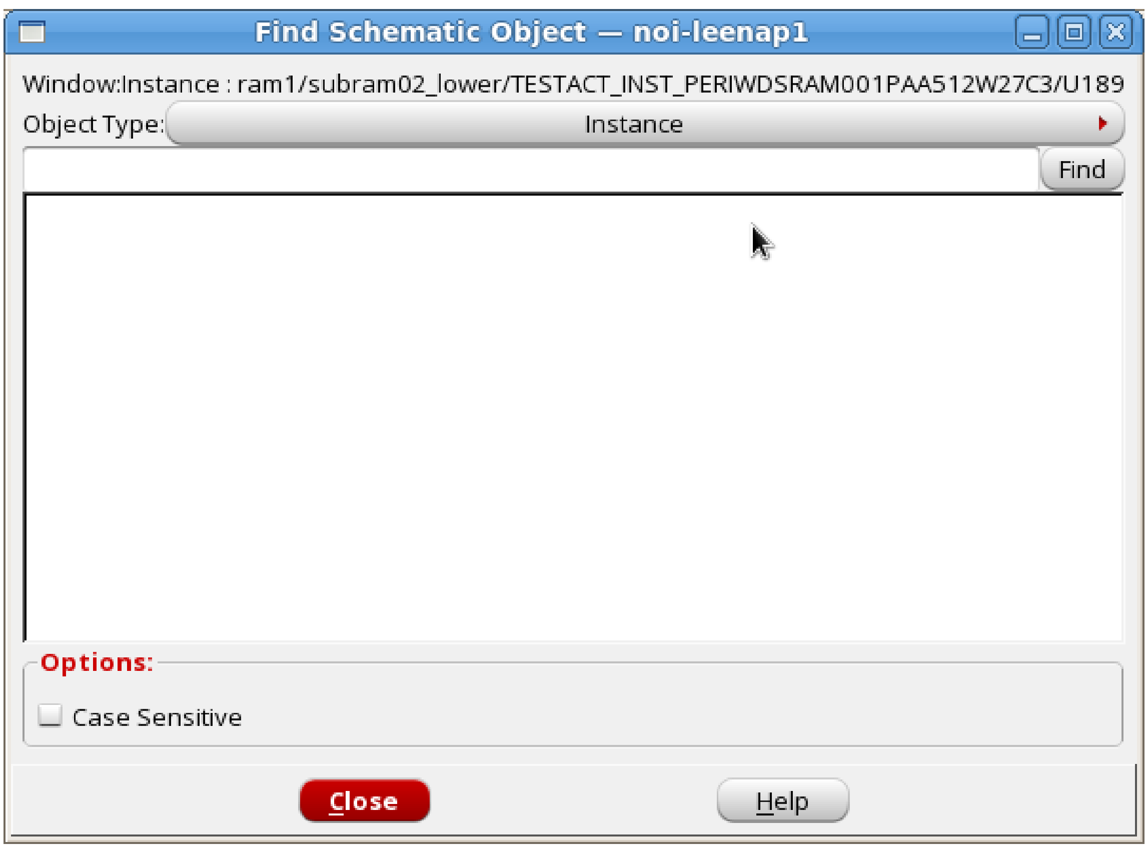
Design Name	Specifies the name of the design. This information appears in the bottom left corner of the printout.
Designer	Specifies the designer name. This information appears in the bottom left corner of the printout.
Description	Specifies a description. This information appears in the bottom left corner of the printout.
Orientation	Specifies the page orientation. Choose *Portrait* or *Landscape*.
Page Size	Specifies the page size. Choose a standard page size of *8.5X11* or use the pull-down menu to specify a custom size.
Job Size	Specifies the job size. Choose to print all the pages or only the current page.
Scaling	Specifies the scaling. Choose *Full Page* or *Current View*.

Print To	Specifies the print output destination. Choose one of the following: • *Printer* - If you choose this option, type the appropriate print command in the *Print Command* text box. • *File* - If you choose this option, the *File* text box at the bottom is enabled. Type a filename in the *File* text box or use the adjacent folder button to select the appropriate file. • *GIF (Current View to File)* - Choose this option to print the current view to the specified file.

Find Schematic Object

Use the Find Schematic Object form to find and highlight a specified object in the schematic display area.

- Click the *Find* widget on the toolbar.



Find Schematic Object Fields and Options

Window	Identifies which schematic window was active when you selected this option.
Object Type	Specifies the object type you want to find.
Find	Specifies the object name or a portion of the name with wildcard characters. Type the object name in the adjacent text box and click *Find*. The search results are displayed in the list box below this field. Double-click a name to highlight the object in the schematic display area.
Case Sensitive	Allows you to make the search case sensitive.

Log Viewer

Use the *Log Viewer* menu command to open up a log file in a separate console window for viewing.

- Choose *Tools - Log Viewer*, select the log file you want to view, then click *Open*.

The log file displayed contains `[+]` and `[-]` markers that expand and collapse command information, so that you can control how much detail you want to read. Log messages are color coded for easier identification: blue messages denote warnings, red messages denote errors.

By default, the software opens the current log file, and updates it in real time. If you specify a log file name, the software opens up the specified log file.

You can use the *Log Viewer* menu command more than once to view multiple log files in separate console windows simultaneously. However, you cannot open multiple versions of the current log file.

Menu Bar

- File Menu
- Edit Menu

File Menu

Open	Opens a log file in a separate console window.
Close	Closes the log file.

Edit Menu

Find	Opens the Find in this log file form, which can be used to search the log file content for specific words and commands.
Expand All	Expands all command information in the log file.
Suppress All	Collapses command information in the log file.

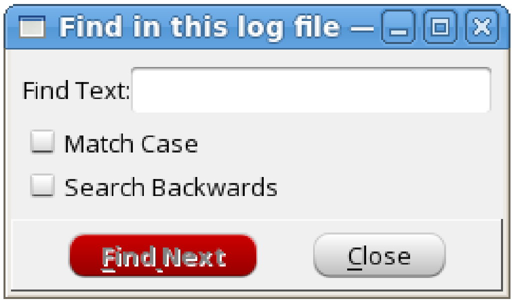
Related Text Commands

- `viewLog`

Find in this log file

Use the Find in this log file form to search the log file contents for strings, words, and commands.

- From the *Log Viewer* console window menu, choose *Edit - Find*.



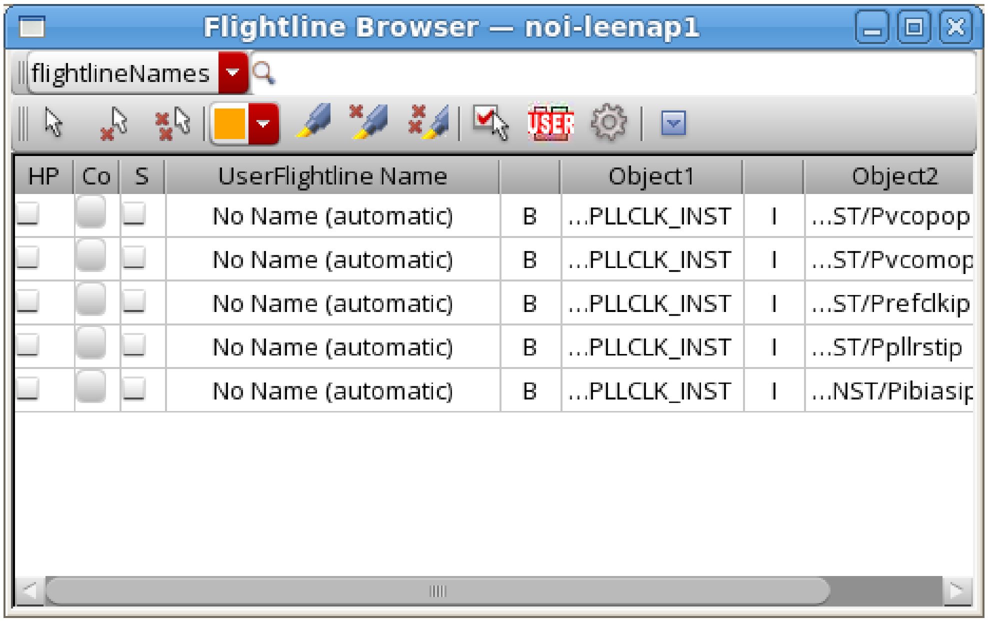
Find in this log file Fields and Options

Find Text	Searches the log file contents for the specified text.
Match Case	Specifies that the software should search only for content that matches the specified text exactly.
Search Backwards	Searches backward through the log file.

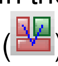
Flightline Browser

Use the Flightline Browser to browse, select, and save flightline objects. This enables you to query connection information in the netlist for analyzing the floorplan.

- Choose *Tools - Flightline Browser*.



As soon as you open the Flightline Browser, the software enters the Flightline mode. In this mode, you can select the flightlines and other floorplan objects using the mouse in the same way as in the Select mode.

You can switch to the Flightline mode directly by clicking the *Select Flightline* widget () on the toolbar.

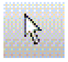
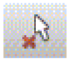
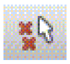
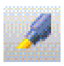
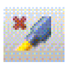
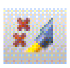
The Flightline Browser displays flightline info in a tabular format, which makes it possible for you to find relevant information about flightlines at a glance. It also lets you sort flightlines by name, object, net, or slack.

Double-clicking on a flightline record opens the Flightline Net Window form.

Note: All flightlines that appear in the Amoeba design view are automatically reported in the Flightline Browser. You do not need to select them in the Amoeba view.

Flightline Browser Fields and Options

	Enables you to find specified flightline or hInstance. When you enter text in the text input box, the Clear button () is displayed next to the text input box. Use this button to clear any existing text in the input box.

	*Select* --Selects the corresponding flightline in the design display area for the flightline record selected in the Flightline Browser table.
	*Deselect* --Deselects the corresponding flightline in the design display area for the flightline record selected in the Flightline Browser table..
	*Deselect All* --Deselects all flightlines in the design display area.
	*Edit Highlight Color*-- Enables you to change the highlight color of selected flightline or hInstance.
	*Highlight* --Changes the color of selected flightline record to current highlight color and highlights the corresponding flightline in the design display area with the same color.
	*Dehighlight* --Dehighlights a flightline in the design display area.
	*Dehighlight All* --Dehighlights all flightlines in the design display area, including ones that are highlighted permanently.
	*Only Selected Flightlines*--Displays only selected flightline records when turned on. This button is off by default.
	*Only User Flightlines*--Displays only user flightlines when turned on. This button is off by default.
	Opens the *Flightline* page of the Preferences form. You can use this page to modify various flightline settings, such as color and width.
	*Show Timing*-- Displays the following two additional columns in the Flightline Browser table to shows timing information: • *NbViolNet:* • *WorstSlk:* Displays worst slack.
HP	*Highlight Permanently*--Enables you to highlight a flightline permanently. If you select this check box for a flightline, the flightline is highlighted permanently with the color selected on the *Hilite Color* bar. When a color is applied to a flightline using the *Highlight* button, the *HP* check box is turned on automatically for that flightline.
Co	*Color*--Displays the color in which a flightline is highlighted.

S	*Select* column–Enables you to select or deselect a flightline by clicking on the corresponding selection check box. This column has to be updated after you make any selection or deselection directly in the *Amoeba View*.
UserFlightline Name	Displays the name of the flightline for user-defined flightlines. For bundles, the name is displayed as *Bundle_net_name (Bundle).* For regular flightlines, displays *No Name (automatic).* **Note**: The *Copy Cell* option in the right-click context menu for this column enables you to copy the cell information.
Indicator column for *Object1*	Displays type of *Object1*. Type can be *M* (Module), *B* (Block), or *IO* (Pad).

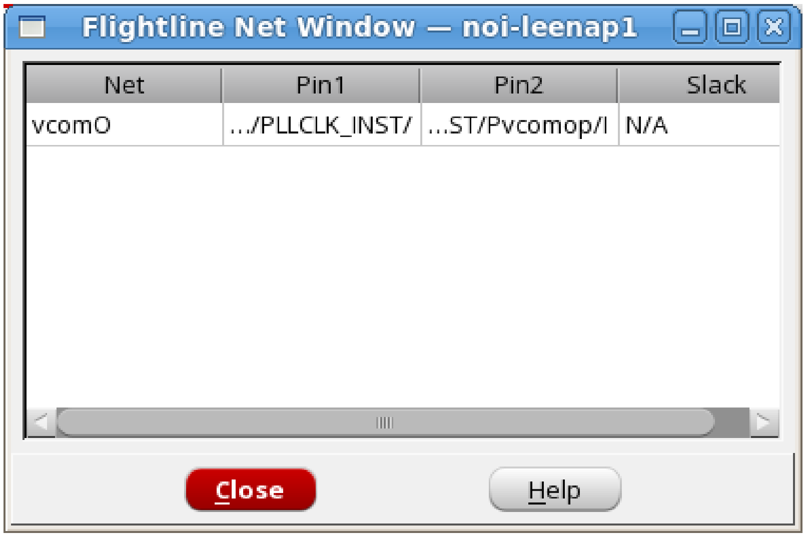
Object1	Specifies the name of object which is the start point of the nets.
	
	Note: If an object name is not completely visible, you can place the cursor over it to see rollover text as shown below.
	
	`FlightLine: No Name (automatic)`
	`hInst1: Module3`
	`hInst2: Module1/M1_7`
	
	You can also resize the column or the window to see the complete name.

Indicator column for *Object2*	Displays type of *Object2*. Type can be *M* (Module), *B* (Block), or *IO* (Pad).
Object2	Specifies the name of object which is the end point of the nets.
NrNets	Shows the number of nets
NbViolNet	Shows the number of violation nets.
WorstSlk	Specifies worst slack.

Flightline Net Window

Use the Flightline Net Window to display net information related to a specific flightline.

- Double-click on a flightline record in the Flightline Browser to open the Flightline Net Window.



Flightline Net Window Fields and Options

Net	Specifies net name.
Pin1	Specifies the name of the pin that connects to the net.
Pin2	Specifies the name of the pin that connects to the net.
Slack	Specifies the slack value.

Mixed Signal

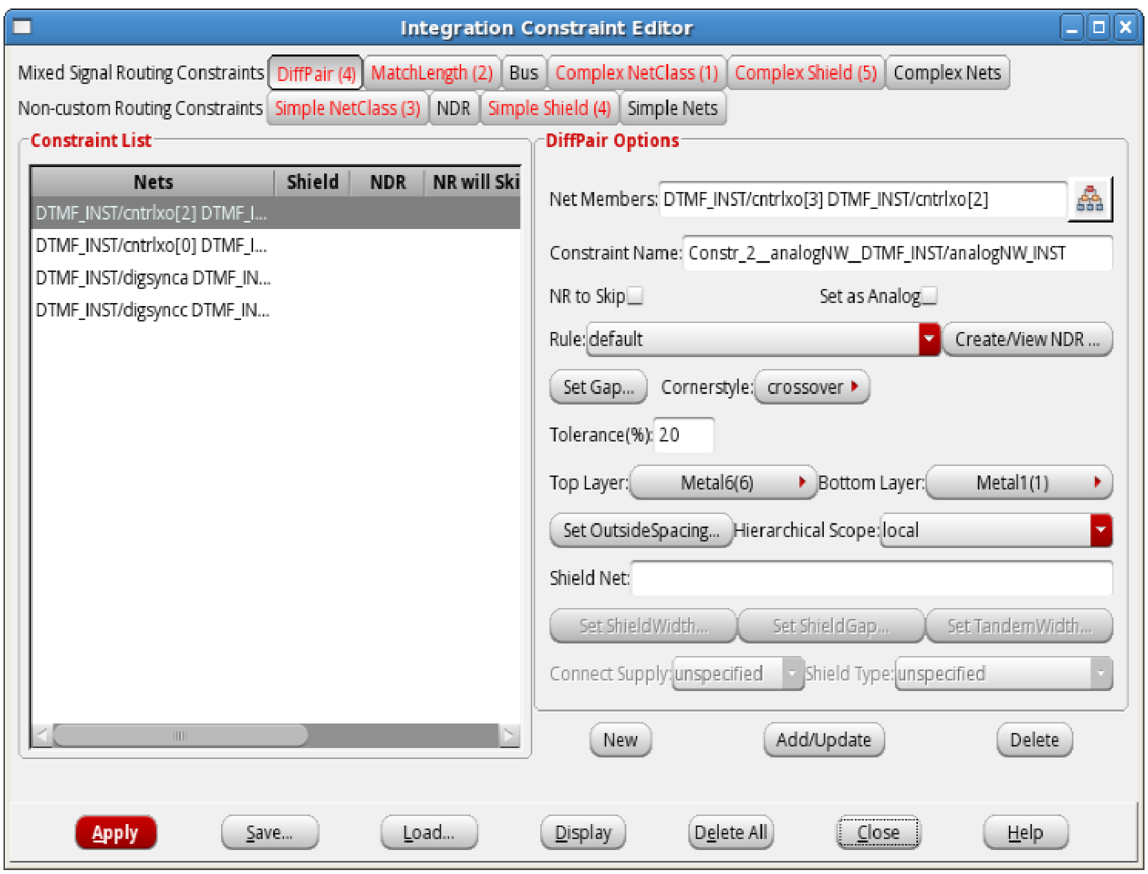
Use the Mixed Signal submenu to perform critical tasks in the mixed signal flow. The Mixed Signal submenu provides access to the following forms:

- Integration Constraint Editor
- Run VSR
- Pull Block Constraint

Integration Constraint Editor

The Integration Constraint Editor (ICE) enables you to apply specialty routing constraints in the database for nets in the designs.

- Choose *Tools - Mixed Signal - Integration Constraint Editor*.



The Integration Constraint Editor is organized in such a way as to make it easy for you to distinguish between different types of routing constraints:

- *Mixed Signal Routing Constraints* - Tabs in this row display nets that are routed using custom routing techniques. These nets have a property identifying them as Mixed Signal nets, instructing all applications in the Innovus environment to ignore them. The tabs in this row are:

  - *DiffPair*
  - *MatchLength*
  - *Bus*
  - *Complex NetClass*
  - *Complex Shield*
  - *Complex Nets*

- *Non-Custom Routing Constraints* - Tabs in this row display nets that can be routed in Innovus using NanoRoute. For example, if you have created a netClass constraint for a group of nets that need to be routed as simple shielding, or with a simple Non-Default Rule (NDR), or with top/bottom layers defined, then you do not really need an external router. In these cases, NanoRoute can be used to route such nets provided that the skip routing attribute is not set on the nets belonging to these types of netClasses. The tabs in this row are:
  - *Simple NetClass*
  - *NDR*
  - *Simple Shield*
  - *Simple Nets*
- The active constraint tabs in the Integration Constraint Editor are labeled in red to make it easy for you to identify them. In addition, the Integration Constraint Editor also displays the constraint count on each active constraint tab.

If a net has multiple constraints, Innovus uses the following precedence rule to determine the tab on which the net is displayed:

1. *DiffPair*
2. *MatchLength*
3. *Bus*
4. *Complex NetClass*
5. *Complex Shield*
6. *Complex Nets*
7. *Simple NetClass*
8. *NDR*
9. *Simple Shield*

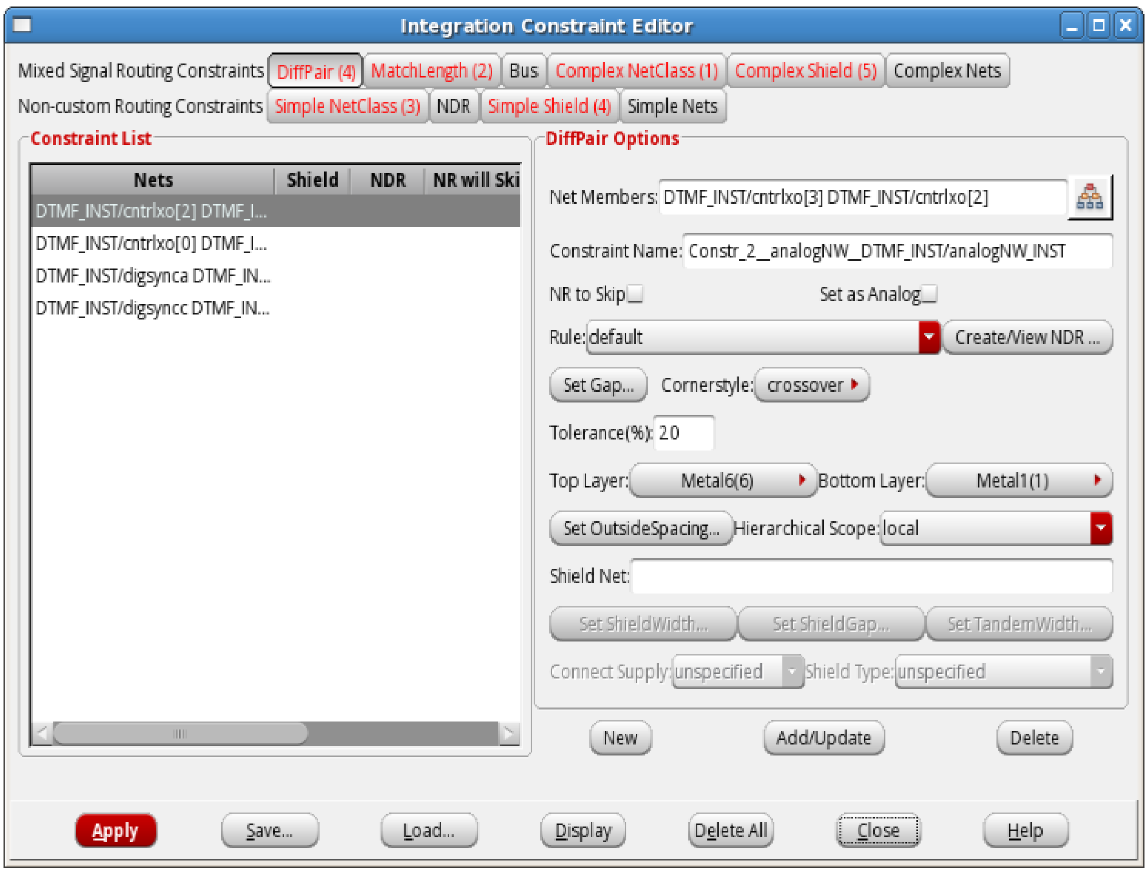
10. *Simple Nets*

Based on this rule, if a net belongs to a DiffPair constraint group and also has a complex shield constraint, it will show up only on the *DiffPair* tab of the Integration Constraint Editor. Similarly, if a net has a simple Non-Default Rule and also has a shield constraint, it will be displayed only on the *NDR* tab and not on the *Simple Shield* tab.

ICE - DiffPair Tab

Use the *DiffPair* tab to specify a `diffPair` group constraint. A diffPair group has only two nets as its members. The net members of a `diffPair` group show up in the Constraint List only when the *DiffPair* tab is selected. Even if the `diffPair` has a complex shield, the net members of the `diffPair` group do not show up on the *Complex Shield* tab in accordance with the precedence rule.

The net members of a diffPair group have a property identifying them as Mixed-Signal nets, instructing all applications in the Innovus environment to ignore such nets.



ICE - DiffPair Fields and Options

Constraint List	Displays the list of constraints. You can sort the list by one of the following columns: **Note:** These columns appear grayed out as they cannot be modified. They can be used only for sorting.	
	Nets	Displays the net name and enables you to sort constraints by net name.
	Shield	Specifies whether the net is shielded and enables you to sort by shielding.
	NDR	Specifies whether the net has a non-default rule (NDR).
	NR will Skip	Specifies whether NanoRoute will skip the net. This check box is shown as selected if the MS bit is set on the constraint group or skip-routing is set on that particular net. Such nets are routed using custom routing techniques.
	Analog	Specifies whether the net has `oaSigType` set to `analog`. Many Virtuoso users use the `analog` attribute in their designs. This column makes it easy to determine whether or not a net has the `analog` attribute set from within the Innovus tool.
DiffPair Options		
	Net Members	Specifies the list of net names that are to be routed. Use the *Design Browser* button to open the Select Net Members form and select desired nets.
	Constraint Name	Displays the name of the constraint, as assigned in OpenAccess.
	NR to Skip	Specifies that NanoRoute will skip the net and that the net will be routed using custom routing techniques. This check box is selected by default on the *DiffPair* tab because the MS bit is set on the diffPair constraint group. **Note:** This field is grayed out and cannot be modified on the *DiffPair* tab.
	Set as Analog	Sets the `analog` attribute set for the net, if selected.
	Rule	Specifies the name of the routing rule that is used for routing a particular type of net(s).
	Create/View NDR	Lets you create a new NDR or view an existing NDR that is to be used for routing.

	Set Gap	Indicates the layer names and the gap-spacing values for the nets routed as diffPair. For any layer not listed, the minimum legal spacing for that layer is used.
	Cornerstyle	Specifies the type of corner style that the differential pair route should follow when changing directions. You can specify the corner style as *crossover* or *river.* The *crossover* style is the default.
	Tolerance	Indicates the percentage difference in length that is allowed when routing nets as diffPair.
	Top Layer	Specifies the top routing layer that is to be used for routing.
	Bottom Layer	Specifies the bottom routing layer that is to be used during routing.
	Set OutsideSpacing	Maps the Virtuoso group to the external group constraints and indicates the spacing between the nets in this net group, and other nets in a design.
	Hierarchical Scope	Specifies whether the particular constraint is local, and/or can be pulled (above) or pushed (below) across the hierarchy. Setting this option to all possible values enables pull and push. If set to local, it is not saved to the database.
	Shield Net	Indicates that the net group should be shielded by the specified net(s). Valid net names are all power and ground net names in the design. You can specify different shield nets for different sides of a wire. The routers then determine which shield net should be used on which side of the wire. **Note:** You can specify two shield net names for only the following shield types: • `side` • `topSide` • `bottomSide` • `coaxial` For the `top`, `bottom`, or `topBottom` shield types, you can specify only one shield net. **Note:** The *Shield Net* and *Set OutsideSpacing* fields are mutually exclusive.
	Set ShieldWidth	Specifies the width of the shield wire in microns per layer.

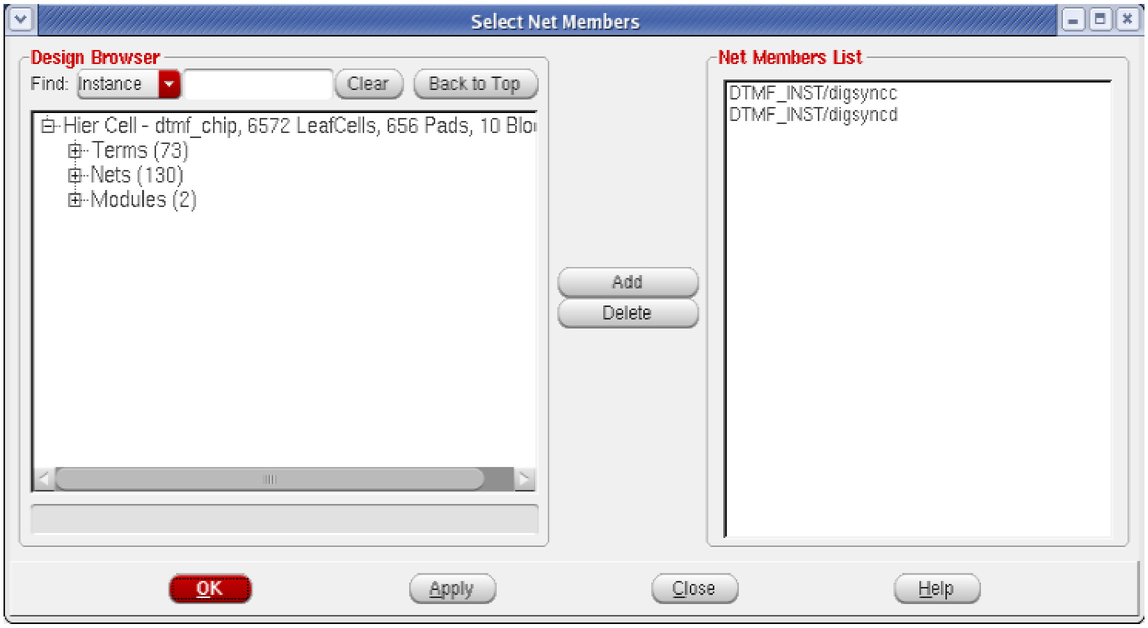
	Set ShieldGap	Specifies the spacing between a shielded wire and a shield net.
	Set TandemWidth	Specifies the overhang value for the shields on the top and bottom layers so as to extend them to overlap the side shields.
	Connect Supply	Indicates how the shield wires will be connected to the supply line. The default option, `anyPoint`, tells the router to connect the wire to supply, anywhere along the length of the shield wire.
	Shield Type	Specifies the shielding type for the net(s) being routed.
	New	Specifies the new diffpair constraint that is to be created.
	Add/Update	Lets you add or modify an existing diffpair constraint.
	Delete	Lets you delete a diffpair.

-

Select Net Members

Use the Select Net Members form to select nets for a constraint. To open the form:

1. Choose *Tools - Mixed Signal - Integration Constraint Editor.*
2. Click the *Design Browser* button next to the *Net Members* field on any tab of the Integration Constraint Editor form.

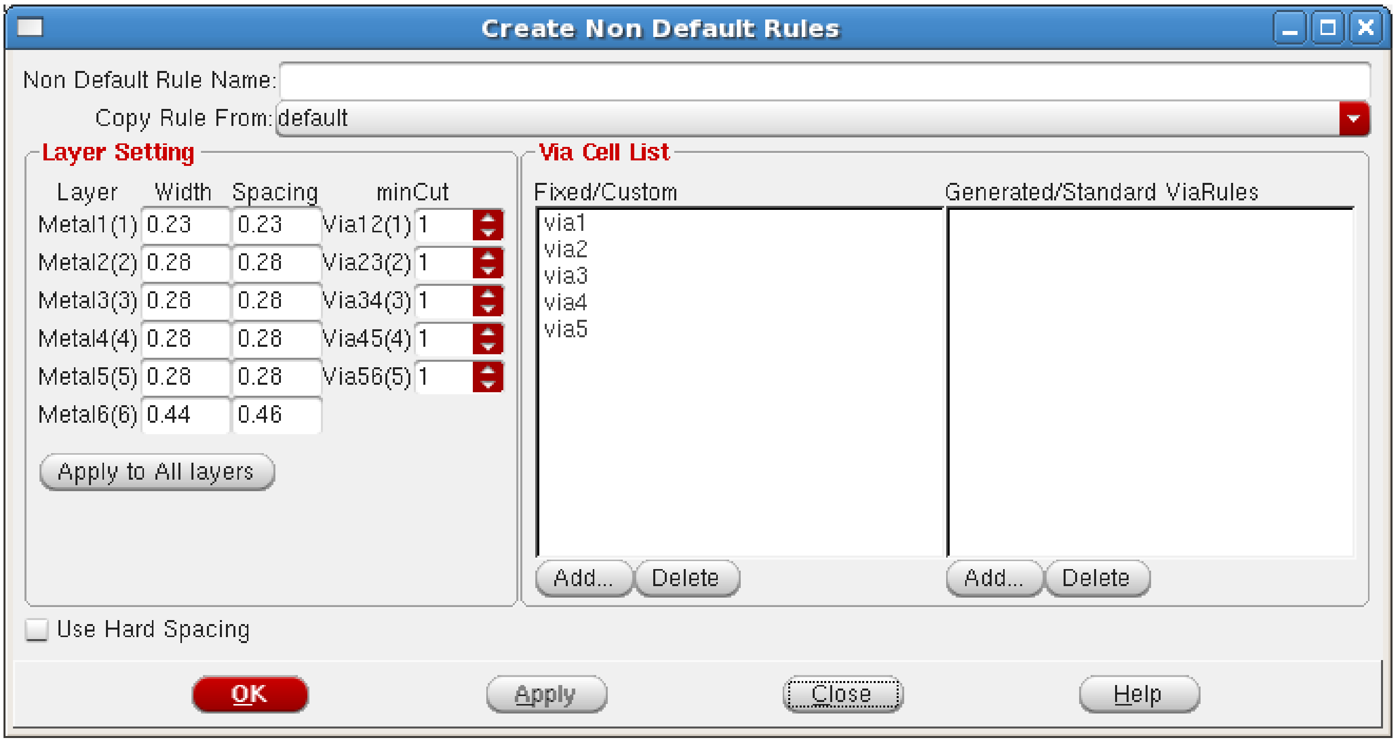


Design Browser	Enables you to navigate through the chip's design hierarchy.	
	Find	Enables you to search and display hierarchy information for the object you specify in the adjacent text input box. You can use wildcards to specify object names in the text input box. Use the *Clear* button to clear any existing text in the input box. You can view information on the following object types: • *Instance* • *Net* • *Group* • *Cell*
	Design Browser list box	Displays the design hierarchy tree and enables you to select net members of a constraint: 1. Expand the *Nets* list to view the nets in the design. 2. Select the net you want to add as member to the constraint. 3. Click the *Add* button to add the selected net to the *Net Members List*. 4. Click *OK*.
Net Members List	Lists the net members of a constraint. To remove a net from this list, select it and click the *Delete* button.	

Create Non Default Rules

Use the Create Non Default Rules form to create non-default rules. To open the form:

1. Choose *Tools - Mixed Signal - Integration Constraint Editor.*
2. Click the *Create/View NDR* button on any tab of the Integration Constraint Editor form.



Create Non Default Rules Fields and Options

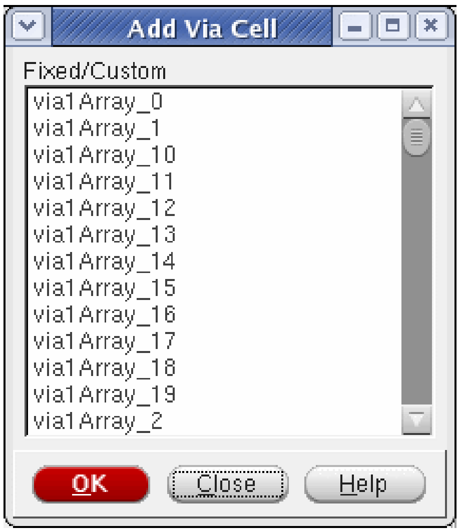
Non Default Rule Name	Specifies the non-default rule name.
Copy Rule From	Specifies the default rule that is copied from an existing LEF technology.
Layer Setting	Specifies the layer name, width and spacing relationship in a tabular format.
Via Cell List	Displays the list of the via cells from the current editing rule.
Fixed/Custom	Specifies the via cells that have the `DEFAULT` keyword against the via names. These via cells are mainly used by signal routes. Click the *Add* button below this text box to open the Add Via Cell form to select the via cells to be added. Use the *Delete* button below the *Fixed/Custom* text box to delete the selected via cell from the text box.
Generated/Standard Via Rules	Specifies the VIA cells that do not have the `DEFAULT` keyword against the via names. The tool usually generates its own via based on these rules. Examples of these kinds of vias are non-default vias and power vias. Click the *Add* button below this text box to open the Add Via Rule form to select the via rules to be added. Use the *Delete* button below the *Generated/Standard Via Rules* text box to delete the selected via rule from the text box.
Use Hard Spacing	Honors NDR spacing even if the design is congested. Typically, the spacing rules for NDR are considered soft, meaning that the router will honor the spacing only if the design is not congested. If the design is congested, the router does not honor soft spacing rules.

Add Via Cell

Use the Add Via Cell form to add vias cells in the design to the *Fixed/Custom* text box in the Create Non Default Rules form.

To open the Add Via Cell form:

1. Choose *Tools - Mixed Signal - Integration Constraint Editor.*
2. Click the *Create/View NDR* button on any tab of the Integration Constraint Editor form.
3. Click the *Add* button below the *Fixed/Custom* text box in the Create Non Default Rules form.

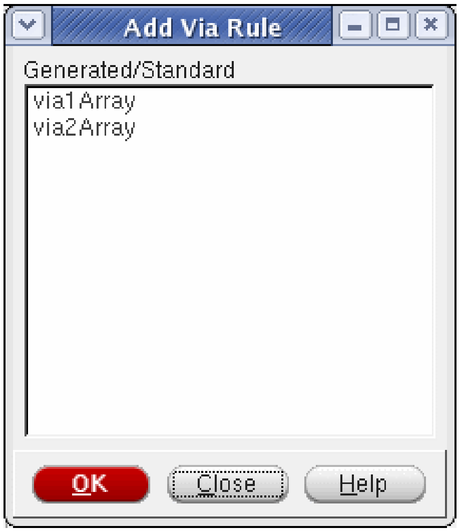


Add Via Rule

Use the *Add Via Rule* form to add a generated/standard via rule from the design to the *Generated/Standard Via Rules* text box in the Create Non Default Rules form for reference.

To open the Add Via Rule form:

1. Choose *Tools - Mixed Signal - Integration Constraint Editor.*
2. Click the *Create/View NDR* button on any tab of the Integration Constraint Editor form.
3. Click the *Add* button below the *Generated/Standard Via Rules* text box in the Create Non Default Rules form.



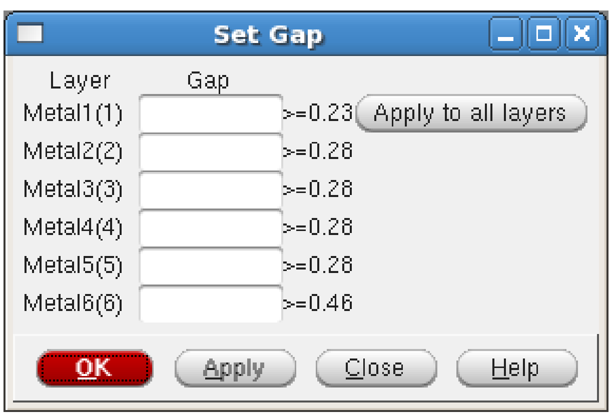
Add Via Rule Fields and Options

Generated/Standard	Displays the list of vias that connect layers.

Set Gap

Use the Set Gap form to specify the gap between layers. To open the Set Gap form:

1. Choose *Tools - Mixed Signal - Integration Constraint Editor*.
2. Click the *Set Gap* button on the *DiffPair* or *Bus* tab of the Integration Constraint Editor form.



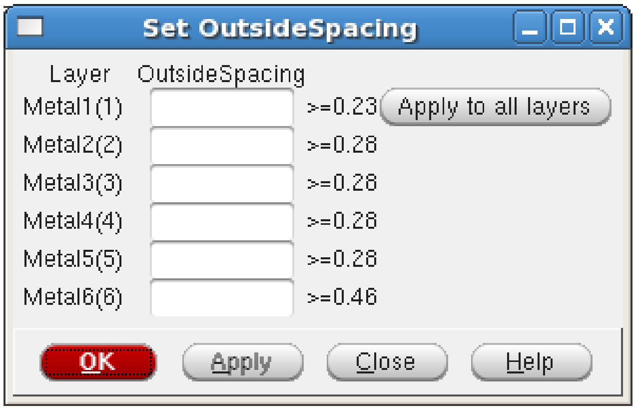
Set Gap Fields and Options

Layer	Displays the layer name.
Gap	Specifies the gap between layers.
Apply to all layers	Applies the value entered for a metal layer to all the metal layers.

Set Outside Spacing

Use the *Set OutsideSpacing* form to map Virtuoso group constraints to non-Virtuoso group constraints. To open the form:

1. Choose *Tools - Mixed Signal - Integration Constraint Editor.*
2. Click the *Set OutsideSpacing* button on the Integration Constraint Editor form. This button is available on the *DiffPair, MatchLength, Bus, Complex NetClass*, and *Complex Nets* tabs of the form.



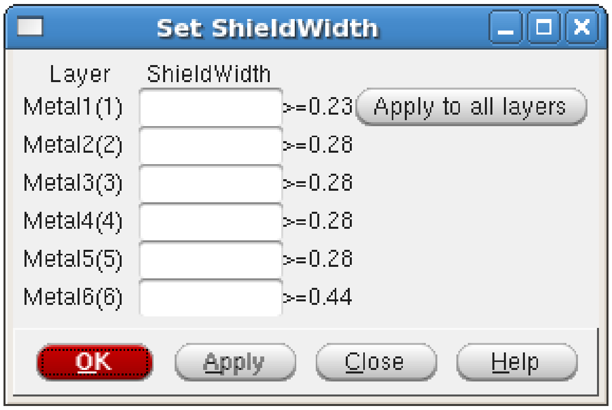
Set OutsideSpacing Fields and Options

Layer	Specifies the layer name.
OutsideSpacing	Specifies the outside spacing between the Virtuoso group constraint nets and other nets in a design.
Apply to all layers	Applies the same spacing values to all the layers on the form.

Set ShieldWidth

Use the *Set ShieldWidth* form to specify the width of the shield wire in microns per layer. To open the form:

1. Choose *Tools - Mixed Signal - Integration Constraint Editor.*
2. Specify a net in the *Shield Net* text box on any tab of the Integration Constraint Editor form.
3. Click the *Set ShieldWidth* button.



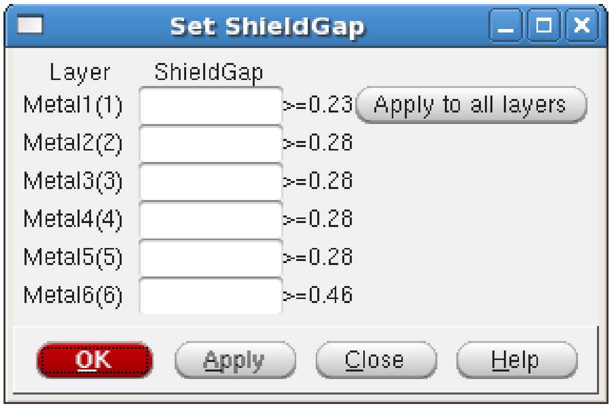
Set ShieldWidth Fields and Options

Layer	Specifies the layer name.
ShieldWidth	Specifies the shield wire width in microns per layer. The values apply only to side shields.
Apply to all layers	Applies the same values to all the layers on the form.

Set Shield Gap

Use the *Set ShieldGap* form to specify spacing between a shielded wire and a shield net. To open the form:

1. Choose *Tools - Mixed Signal - Integration Constraint Editor.*
2. Specify a net in the *Shield Net* text box on any tab of the Integration Constraint Editor form.
3. Click the *Set ShieldGap* button.



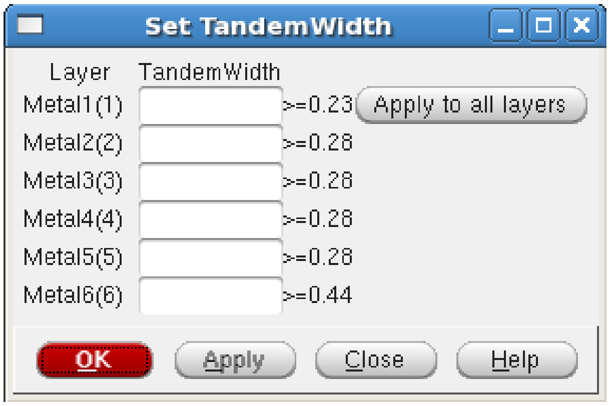
Set ShieldGap Fields and Options

Layer	Specifies the layer name.
ShieldGap	Specifies the spacing between a shielded wire and a shield net.
Apply to all layers	Applies the same values to all the layers on the form.

Set TandemWidth

Use the *Set TandemWidth* form to specify the overhang value for the shields on the top and bottom layers so as to extend them to overlap the side shields. To open the form:

1. Choose *Tools - Mixed Signal - Integration Constraint Editor.*
2. Specify a net in the *Shield Net* text box on any tab of the Integration Constraint Editor form.
3. Specify *Shield Type* as any one of the follows: *top, bottom, topSide, bottomSide, topBottom,* or coaxial. When you do so, the *Set TandemWidth* button becomes active.
4. Click the *Set TandemWidth* button.



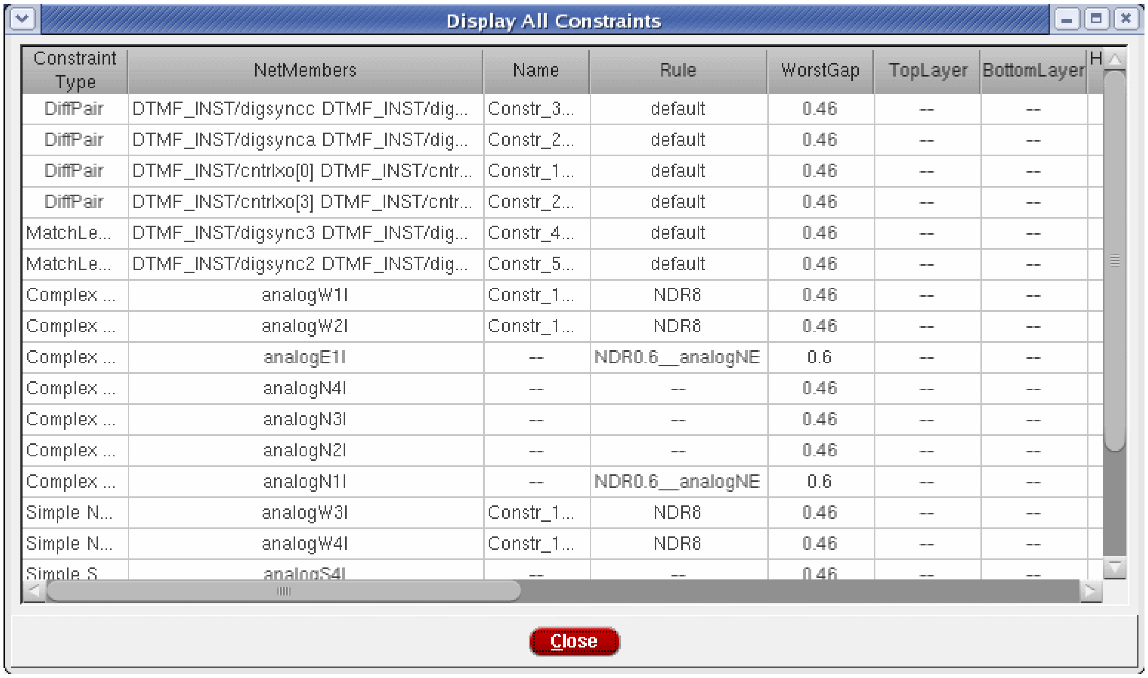
Set TandemWidth Fields and Options

Layer	Specifies the layer name.
TandemWidth	Specifies the width of tandem shield wires.
Apply to all layers	Applies the same values to all the layers on the form.

Display All Constraints

Use the Display All Constraints form to display information on all routing constraints in the design. To open the form:

1. Choose *Tools - Mixed Signal - Integration Constraint Editor.*
2. Click the *Display* button at the bottom of the Integration Constraint Editor form.

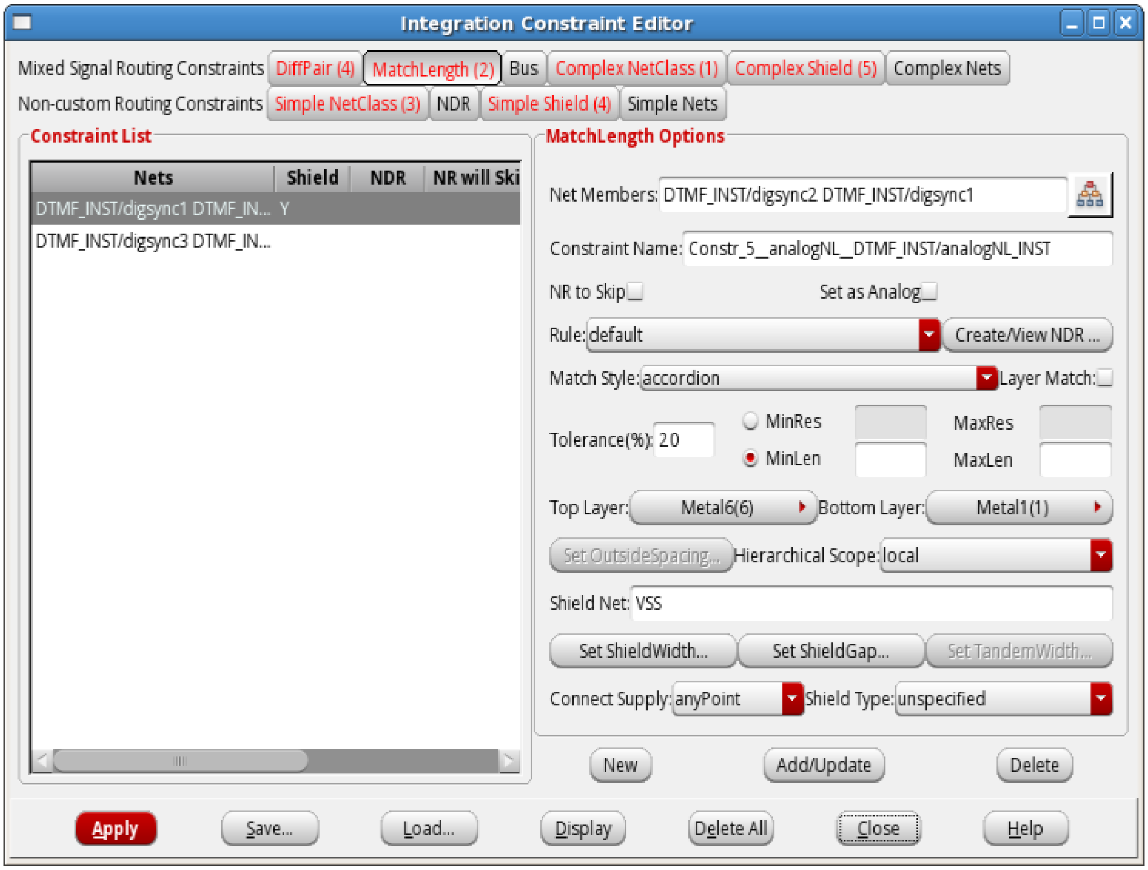


Constraint Type	NetMembers	Name	Rule	WorstGap	TopLayer	BottomLayer	H
DiffPair	DTMF_INST/digsyncc DTMF_INST/dig...	Constr_3...	default	0.46	--	--	
DiffPair	DTMF_INST/digsynca DTMF_INST/dig...	Constr_2...	default	0.46	--	--	
DiffPair	DTMF_INST/cntrlxo[0] DTMF_INST/cntr...	Constr_1...	default	0.46	--	--	
DiffPair	DTMF_INST/cntrlxo[3] DTMF_INST/cntr...	Constr_2...	default	0.46	--	--	
MatchLe...	DTMF_INST/digsync3 DTMF_INST/dig...	Constr_4...	default	0.46	--	--	
MatchLe...	DTMF_INST/digsync2 DTMF_INST/dig...	Constr_5...	default	0.46	--	--	
Complex ...	analogW1I	Constr_1...	NDR8	0.46	--	--	
Complex ...	analogW2I	Constr_1...	NDR8	0.46	--	--	
Complex ...	analogE1I	--	NDR0.6__analogNE	0.6	--	--	
Complex ...	analogN4I	--	--	0.46	--	--	
Complex ...	analogN3I	--	--	0.46	--	--	
Complex ...	analogN2I	--	--	0.46	--	--	
Complex ...	analogN1I	--	NDR0.6__analogNE	0.6	--	--	
Simple N...	analogW3I	Constr_1...	NDR8	0.46	--	--	
Simple N...	analogW4I	Constr_1...	NDR8	0.46	--	--	
Simple S...	analogS4I	--	--	0.46	--	--	

ICE - MatchLength

Use the *MatchLength* tab to specify constraints for match pair nets. A match pair is a MatchedNetGroup with many nets as members. The constraint is used by the router to match the lengths of all nets to within a certain tolerance. The net members of the match pair group show up in the Constraint List only when the *MatchLength* tab is selected. Even if the match pair has a complex shield, the net members of the match pair group do not show up on the *Complex Shield* tab in accordance with the precedence rule.

The net members of a match pair group have a property identifying them as Mixed-Signal nets, instructing all applications in the Innovus environment to ignore such nets.



ICE - MatchLength Fields and Options

Constraint List	Displays the list of constraints. You can sort the list by one of the following columns: **Note:** These columns appear grayed out as they cannot be modified. They can be used only for sorting.	
	Nets	Displays the net name and enables you to sort constraints by net name.
	Shield	Specifies whether the net is shielded and enables you to sort by shielding.
	NDR	Specifies whether the net has a non-default rule (NDR).

	NR will Skip	Specifies whether NanoRoute will skip the net. This check box is shown as selected if the MS bit is set on the constraint group or skip-routing is set on that particular net. Such nets are routed using custom routing techniques.
	Analog	Specifies whether the net has `oaSigType` set to `analog`. Many Virtuoso users use the `analog` attribute in their designs. This column makes it easy to determine whether or not a net has the `analog` attribute set from within the Innovus tool.
MatchLength Options		
	Net Members	Specifies the list of net names that are to be routed.
	Constraint Name	Displays the name of the constraint, as assigned in OpenAccess.
	NR to Skip	Specifies that NanoRoute will skip the net and that the net will be routed using custom routing techniques. This check box is selected by default on the *MatchLength* tab because the MS bit is set on the matchLength constraint group. **Note:** This field is grayed out and cannot be modified on the *MatchLength* tab.
	Set as Analog	Sets the `analog` attribute set for the net, if selected.
	Rule	Specifies the name of the routing rule that is used for routing a particular type of net(s).
	Create/View NDR	Lets you create a new NDR or view an existing NDR that is to be used for routing.
	Match Style	Indicates the routing topology to be used for matching the nets routed as *matchLength* . It can be *Accordion* or *Trombone*.
	Layer Match	Specifies whether each separate layer should be matched for the *matchLength* nets.
	Tolerance	Indicates the percentage difference in length that is allowed when routing nets as *matchLength*.

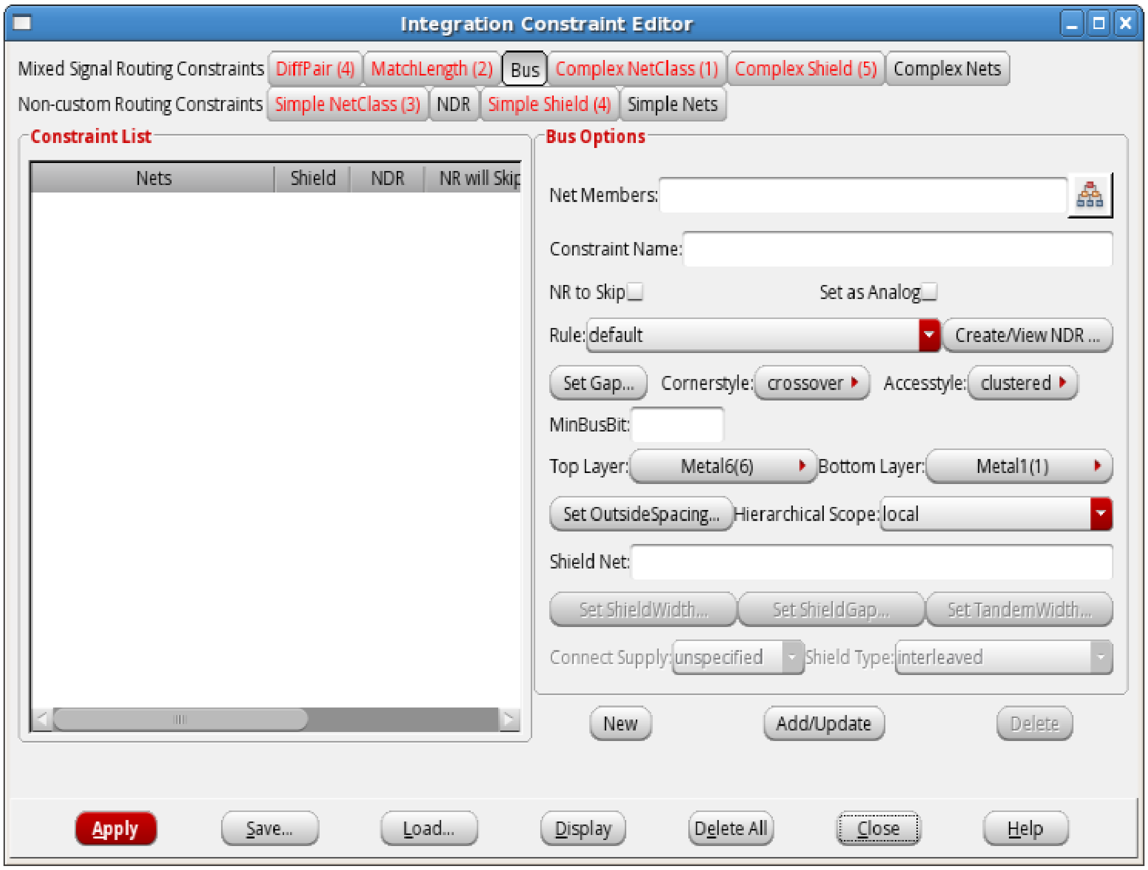
	MinRes	Specifies the minimum resistance to be used by the Virtuoso Space-based Router (VSR) for the nets with a `matchLength` constraint.
	MaxRes	Specifies the maximum resistance to be used by VSR for the nets with a `matchLength` constraint.
	MinLen	
	MaxLen	
	Top Layer	Specifies the top routing layer that is to be used for routing.
	Bottom Layer	Specifies the bottom routing layer that is to be used during routing.
	Set OutsideSpacing	Maps the Virtuoso group to the external group constraints and indicates the spacing between the nets in this net group, and other nets in a design.
	Hierarchical Scope	Specifies whether the particular constraint is local, and/or can be pulled (above) or pushed (below) across the hierarchy. Setting this option to all possible values enables pull and push. If set to local, it is not saved to the database.

	Shield Net	Indicates that the net group should be shielded by the specified net(s). Valid net names are all power and ground net names in the design. You can specify different shield nets for different sides of a wire. The routers then determine which shield net should be used on which side of the wire. **Note:** You can specify two shield net names for only the following shield types: • `side` • `topSide` • `bottomSide` • `coaxial` For the `top`, `bottom`, or `topBottom` shield types, you can specify only one shield net. **Note:** The *Shield Net* and *Set OutsideSpacing* fields are mutually exclusive.
	Set ShieldWidth	Specifies the width of the shield wire in microns per layer.
	Set ShieldGap	Specifies the spacing between a shielded wire and a shield net.
	Set TandemWidth	Specifies the overhang value for the shields on the top and bottom layers so as to extend them to overlap the side shields.
	Connect Supply	Indicates how the shield wires will be connected to the supply line. The default option, `anyPoint`, tells the router to connect the wire to supply, anywhere along the length of the shield wire.
	Shield Type	Specifies the shielding type for the net(s) being routed.
	New	Specifies the new match pair that is to be created.
	Add/Update	Lets you add or modify an existing match pair constraint.
	Delete	Lets you delete a match pair.

ICE - Bus

Use the *Bus* tab of the Integration Constraint Editor to specify bus routing constraints. The bus constraints created using this tab are interpreted as valid bus constraints only for the VSR router.

The net members of a bus constraint have a property identifying them as Mixed-Signal nets, instructing all applications in the Innovus environment to ignore such nets.



ICE - Bus Fields and Options

Constraint List	Displays the list of constraints. You can sort the list by one of the following columns: **Note:** These columns appear grayed out as they cannot be modified. They can be used only for sorting.	
	Nets	Displays the net name and enables you to sort constraints by net name.
	Shield	Specifies whether the net is shielded and enables you to sort by shielding.
	NDR	Specifies whether the net has a non-default rule (NDR).

	NR will Skip	Specifies whether NanoRoute will skip the net. This check box is shown as selected if the MS bit is set on the constraint group or skip-routing is set on that particular net. Such nets are routed using custom routing techniques.
	Analog	Specifies whether the net has `oaSigType` set to `analog`. Many Virtuoso users use the `analog` attribute in their designs. This column makes it easy to determine whether or not a net has the `analog` attribute set from within the Innovus tool.
Bus Options		
	Net Members	Specifies the list of net names that are to be routed.
	Constraint Name	Displays the name of the constraint, as assigned in OpenAccess.
	NR to Skip	Specifies that NanoRoute will skip the net and that the net will be routed using custom routing techniques. This check box is selected by default on the *Bus* tab because the MS bit is set on the bus constraint group. **Note:** This field is grayed out and cannot be modified on the *Bus* tab.
	Set as Analog	Sets the `analog` attribute set for the net, if selected.
	Rule	Specifies the name of the routing rule that is used for routing a particular type of net(s).
	Create/View NDR	Lets you create a new NDR or view an existing NDR that is to be used for routing.
	Set Gap	Indicates the layer names and the gap-spacing values for the nets routed as *bus* . For any layer not listed, the minimum legal spacing for that layer is used.
	Cornerstyle	Specifies the type of corner style that the bus should follow when changing directions. You can specify the corner style as *crossover* or *river.* The *crossover* style is the default.
	Accesstyle	Specifies the preferred style for routing the bus after connecting to the bus pins. You can specify the access style as *straight* or *clustered.* The *clustered* style is the default.

	MinBusBit	Indicates the minimum bits allowed for the router to split a bus. As channels get narrower, it becomes challenging to accommodate all the bus bits in the same channel. By default, *MinBusBit* value is undefined, not `0`. If you specify an integer value for *MinBusBit,* the router splits a bundle with a minimum of this value.
	Top Layer	Specifies the top routing layer that is to be used for routing.
	Bottom Layer	Specifies the bottom routing layer that is to be used during routing.
	Set OutsideSpacing	Maps the Virtuoso group to the external group constraints and indicates the spacing between the nets in this net group, and other nets in a design.
	Hierarchical Scope	Specifies whether the particular constraint is local, and/or can be pulled (above) or pushed (below) across the hierarchy. Setting this option to all possible values enables pull and push. If set to local, it is not saved to the database.
	Shield Net	Indicates that the net group should be shielded by the specified net(s). Valid net names are all power and ground net names in the design. You can specify different shield nets for different sides of a wire. The routers then determine which shield net should be used on which side of the wire. **Note:** You can specify two shield net names for only the following shield types: • `side` • `topSide` • `bottomSide` • `coaxial` For the `top`, `bottom`, or `topBottom` shield types, you can specify only one shield net. **Note**: The *Shield Net* and *Set OutsideSpacing* fields are mutually exclusive.
	Set ShieldWidth	Specifies the width of the shield wire in microns per layer.
	Set ShieldGap	Specifies the spacing between a shielded wire and a shield net.
	Set TandemWidth	Specifies the overhang value for the shields on the top and bottom layers so as to extend them to overlap the side shields.

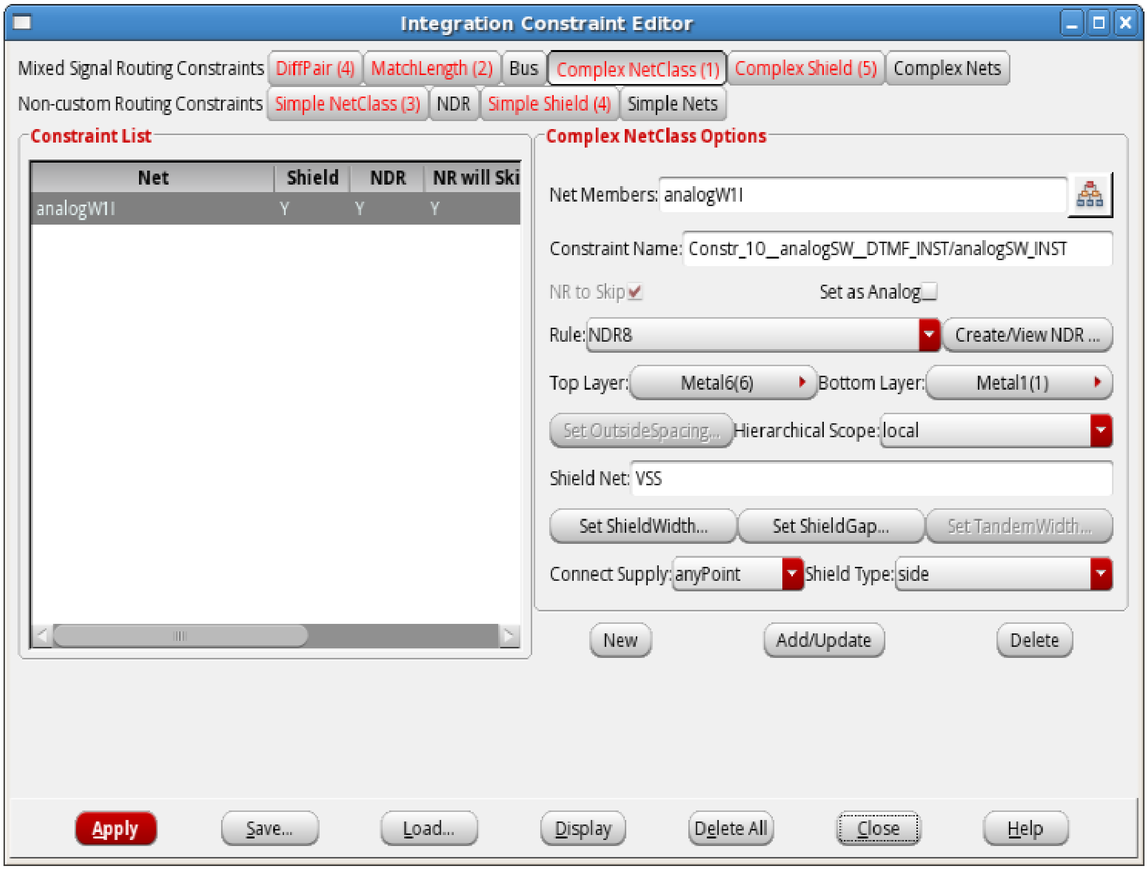
	Connect Supply	Indicates how the shield wires will be connected to the supply line. The default option, `anyPoint`, tells the router to connect the wire to supply, anywhere along the length of the shield wire.
	Shield Type	Specifies the shielding type for the net(s) being routed. By default, the type of shield for the bus is *Interleave*. This style shields each bit.
	New	Lets you specify a new bus constraint.
	Add/Update	Lets you add or modify an existing bus constraint.
	Delete	Lets you delete a bus constraint.

ICE - Complex NetClass

Use the Complex NetClass tab of the Integration Constraint Editor to specify complex netClass constraints. A complex netClass is a netClass that:

- Cannot be identified as a simple netClass according to the rules specified for a simple netClass in the ICE - Simple NetClass section.
  Or
- Has mismatches between the NDRs of any net member and the NDR of the netClass.
  Or
- Has mismatches between the shield nets or shield constraint groups of net members of the netClass.
  Or
- Has a net member with a complex shield constraint group (for example, with Shield Type as coaxial or with Shield Width/Shield Gap defined).
  Or
- Has a default constraint group that has anything other than oacValidRoutingLayer hard/soft constraint.

The net members of a complex netClass constraint have a property identifying them as Mixed-Signal nets, instructing all applications in the Innovus environment to ignore such nets.



ICE - Complex NetClass Fields and Options

Constraint List	Displays the list of constraints. You can sort the list by one of the following columns: **Note:** These columns appear grayed out as they cannot be modified. They can be used only for sorting.	
	Nets	Displays the net name and enables you to sort constraints by net name.
	Shield	Specifies whether the net is shielded and enables you to sort by shielding.
	NDR	Specifies whether the net has a non-default rule (NDR).
	NR will Skip	Specifies whether NanoRoute will skip the net. This check box is shown as selected if the MS bit is set on the constraint group or skip-routing is set on that particular net. Such nets are routed using custom routing techniques.

	Analog	Specifies whether the net has `oaSigType` set to `analog`. Many Virtuoso users use the `analog` attribute in their designs. This column makes it easy to determine whether or not a net has the `analog` attribute set from within the Innovus tool.
Bus Options		
	Net Members	Specifies the list of net names that are to be routed.
	Constraint Name	Displays the name of the constraint, as assigned in OpenAccess.
	NR to Skip	Specifies that NanoRoute will skip the net and that the net will be routed using custom routing techniques. This check box is selected by default on the *Complex NetClass* tab because the MS bit is set on the this constraint group. **Note:** This field is grayed out and cannot be modified on the *Complex NetClass* tab.
	Set as Analog	Sets the `analog` attribute set for the net, if selected.
	Rule	Specifies the name of the routing rule that is used for routing a particular type of net(s).
	Create/View NDR	Lets you create a new NDR or view an existing NDR that is to be used for routing.
	Top Layer	Specifies the top routing layer that is to be used for routing.
	Bottom Layer	Specifies the bottom routing layer that is to be used during routing.
	Set OutsideSpacing	Maps the Virtuoso group to the external group constraints and indicates the spacing between the nets in this net group, and other nets in a design.
	Hierarchical Scope	Specifies whether the particular constraint is local, and/or can be pulled (above) or pushed (below) across the hierarchy. Setting this option to all possible values enables pull and push. If set to local, it is not saved to the database.

	Shield Net	Indicates that the net group should be shielded by the specified net(s). Valid net names are all power and ground net names in the design. You can specify different shield nets for different sides of a wire. The routers then determine which shield net should be used on which side of the wire. **Note:** You can specify two shield net names for only the following shield types: • `side` • `topSide` • `bottomSide` • `coaxial` For the `top`, `bottom`, or `topBottom` shield types, you can specify only one shield net. **Note:** The *Shield Net* and *Set OutsideSpacing* fields are mutually exclusive.
	Set ShieldWidth	Specifies the width of the shield wire in microns per layer.
	Set ShieldGap	Specifies the spacing between a shielded wire and a shield net.
	Set TandemWidth	Specifies the overhang value for the shields on the top and bottom layers so as to extend them to overlap the side shields.
	Connect Supply	Indicates how the shield wires will be connected to the supply line. The default option, `anyPoint`, tells the router to connect the wire to supply, anywhere along the length of the shield wire.
	Shield Type	Specifies the shielding type for the net(s) being routed.
	New	Lets you specify a new complex netClass constraint.
	Add/Update	Lets you add or modify an existing complex netClass constraint.
	Delete	Lets you delete a complex netClass constraint.

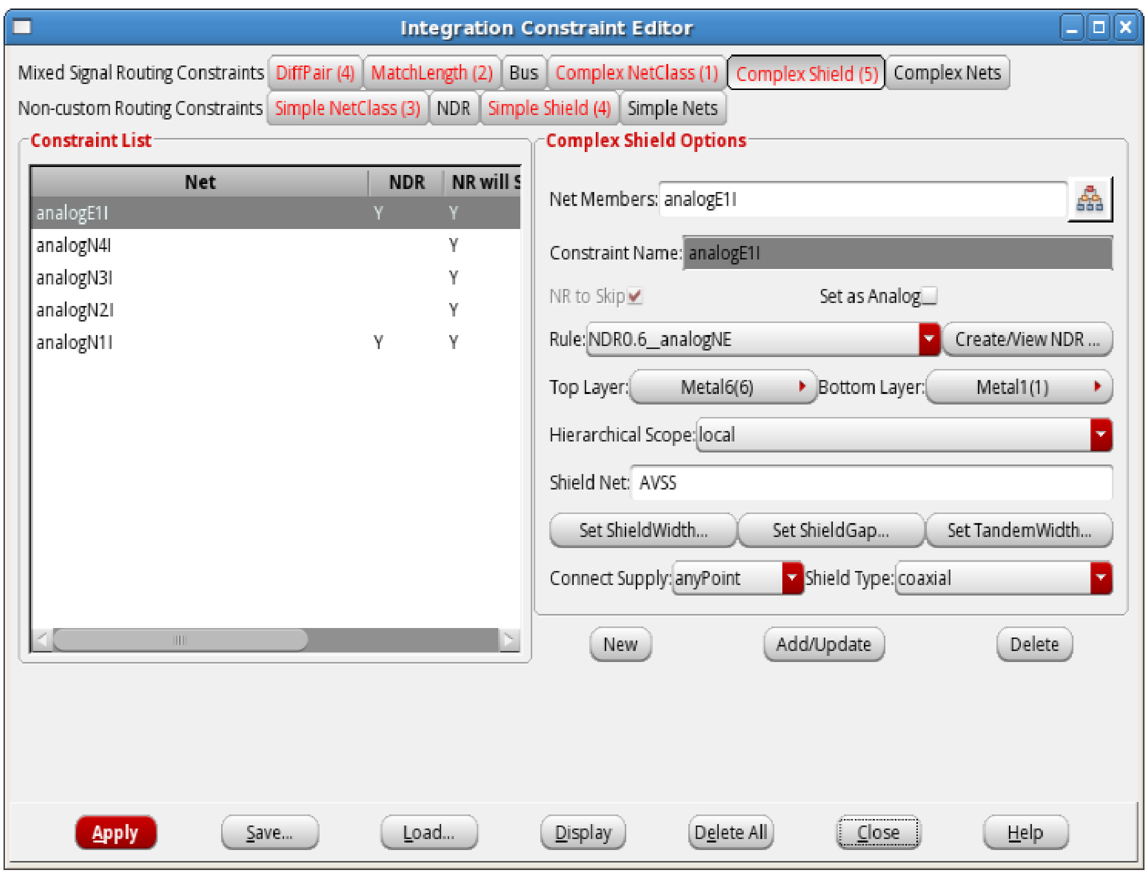
ICE - Complex Shield

Use the *Complex Shield* tab of the Integration Constraint Editor to specify complex shield constraints. A complex shield constraint is a shield constraint that cannot be identified as simple shield by the rules specified in the ICE - Simple Shield section.

Some conditions that make a shield complex are:

- The `shieldStyle` is set to anything other than `Parallel` or `Not Specified` in Virtuoso. That is, *Shield Type* is set to anything other than *none* in Innovus.
  Or
- *Connect Supply* (`msConnectSupply`) is set to `float`.
  Or
- A value has been specified for any of the following: ShieldWidth (oacMinWidth), ShieldGap (oacMinSpacing), TandemWidth (msOverhang), or msSupplyDistance.

The net members of a complex shield constraint have a property identifying them as Mixed-Signal nets, instructing all applications in the Innovus environment to ignore such nets.



ICE - Complex Shield Fields and Options

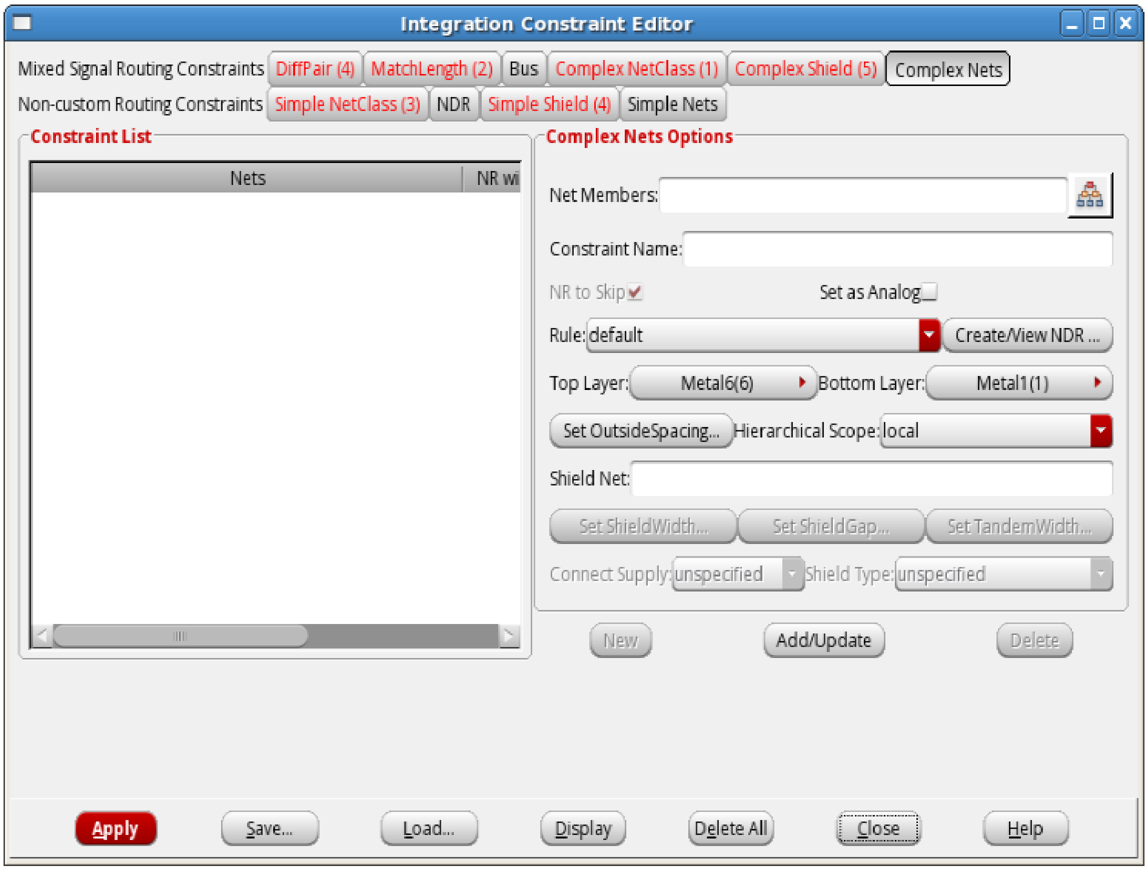
Constraint List	Displays the list of constraints. You can sort the list by one of the following columns: **Note:** These columns appear grayed out as they cannot be modified. They can be used only for sorting.	
	Nets	Displays the net name and enables you to sort constraints by net name.
	NDR	Specifies whether the net has a non-default rule (NDR).
	NR will Skip	Specifies whether NanoRoute will skip the net. This check box is shown as selected if the MS bit is set on the constraint group or skip-routing is set on that particular net. Such nets are routed using custom routing techniques.
	Analog	Specifies whether the net has `oaSigType` set to `analog`. Many Virtuoso users use the `analog` attribute in their designs. This column makes it easy to determine whether or not a net has the `analog` attribute set from within the Innovus tool.
Complex Shield Options		
	Net Members	Specifies the list of net names that are to be routed.
	Constraint Name	Displays the name of the constraint, as assigned in OpenAccess.
	NR to Skip	Specifies that NanoRoute will skip the net and that the net will be routed using custom routing techniques. This check box is selected by default on the *Complex Shield* tab because the MS bit is set on the this constraint group. **Note:** This field is grayed out and cannot be modified on the *Complex Shield* tab.
	Set as Analog	Sets the `analog` attribute set for the net, if selected.
	Rule	Specifies the name of the routing rule that is used for routing a particular type of net(s).
	Create/View NDR	Lets you create a new NDR or view an existing NDR that is to be used for routing.
	Top Layer	Specifies the top routing layer that is to be used for routing.
	Bottom Layer	Specifies the bottom routing layer that is to be used during routing.

	Hierarchical Scope	Specifies whether the particular constraint is local, and/or can be pulled (above) or pushed (below) across the hierarchy. Setting this option to all possible values enables pull and push. If set to local, it is not saved to the database.
	Shield Net	Indicates that the net group should be shielded by the specified net(s). Valid net names are all power and ground net names in the design. You can specify different shield nets for different sides of a wire. The routers then determine which shield net should be used on which side of the wire. **Note:** You can specify two shield net names for only the following shield types: • `side` • `topSide` • `bottomSide` • `coaxial` For the `top`, `bottom`, or `topBottom` shield types, you can specify only one shield net.
	Set ShieldWidth	Specifies the width of the shield wire in microns per layer.
	Set ShieldGap	Specifies the spacing between a shielded wire and a shield net.
	Set TandemWidth	Specifies the overhang value for the shields on the top and bottom layers so as to extend them to overlap the side shields.
	Connect Supply	Indicates how the shield wires will be connected to the supply line. The default option, `anyPoint`, tells the router to connect the wire to supply, anywhere along the length of the shield wire.
	Shield Type	Specifies the shielding type for the net(s) being routed.
	New	Lets you specify a new complex shield constraint.
	Add/Update	Lets you add or modify an existing complex shield constraint.
	Delete	Lets you delete a complex shield constraint.

ICE - Complex Nets

Use the *Complex Nets* tab of the Integration Constraint Editor to specify complex net constraints. A complex net is any net that has routing constraints that are not recognized by Innovus.

The net members of a complex net constraint have a property identifying them as Mixed-Signal nets, instructing all applications in the Innovus environment to ignore such nets.



ICE - Complex Nets Fields and Options

Constraint List	Displays the list of constraints. You can sort the list by one of the following columns: **Note:** These columns appear grayed out as they cannot be modified. They can be used only for sorting.	
	Nets	Displays the net name and enables you to sort constraints by net name.

	NR will Skip	Specifies whether NanoRoute will skip the net. This check box is shown as selected if the MS bit is set on the constraint group or skip-routing is set on that particular net. Such nets are routed using custom routing techniques.
	Analog	Specifies whether the net has `oaSigType` set to `analog`. Many Virtuoso users use the `analog` attribute in their designs. This column makes it easy to determine whether or not a net has the `analog` attribute set from within the Innovus tool.
Complex Nets Options		
	Net Members	Specifies the list of net names that are to be routed.
	Constraint Name	Displays the name of the constraint, as assigned in OpenAccess.
	NR to Skip	Specifies that NanoRoute will skip the net and that the net will be routed using custom routing techniques. This check box is selected by default on the *Complex Nets* tab because the MS bit is set on the this constraint group. **Note:** This field is grayed out and cannot be modified on the *Complex Nets* tab.
	Set as Analog	Sets the `analog` attribute set for the net, if selected.
	Rule	Specifies the name of the routing rule that is used for routing a particular type of net(s).
	Create/View NDR	Lets you create a new NDR or view an existing NDR that is to be used for routing.
	Top Layer	Specifies the top routing layer that is to be used for routing.
	Bottom Layer	Specifies the bottom routing layer that is to be used during routing.
	Set OutsideSpacing	Maps the Virtuoso group to the external group constraints and indicates the spacing between the nets in this net group, and other nets in a design.
	Hierarchical Scope	Specifies whether the particular constraint is local, and/or can be pulled (above) or pushed (below) across the hierarchy. Setting this option to all possible values enables pull and push. If set to local, it is not saved to the database.

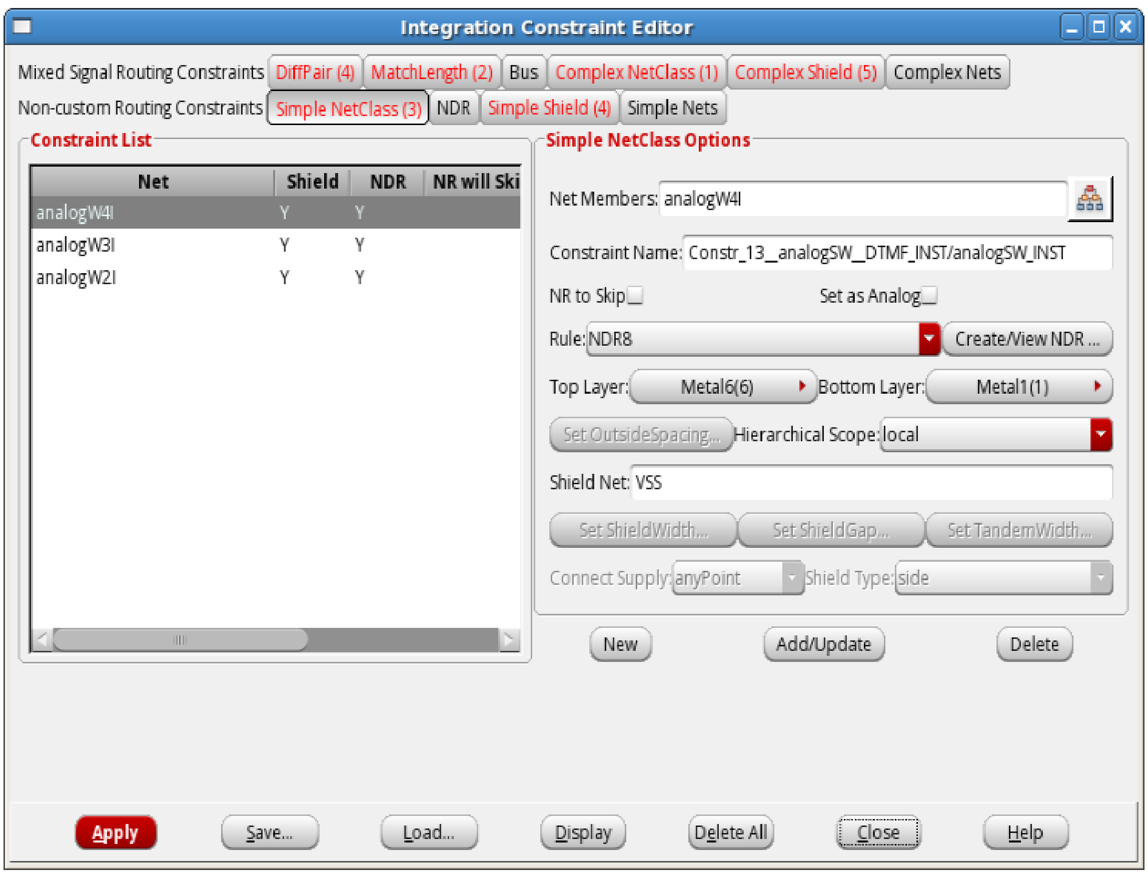
	Shield Net	Indicates that the net group should be shielded by the specified net(s). Valid net names are all power and ground net names in the design. You can specify different shield nets for different sides of a wire. The routers then determine which shield net should be used on which side of the wire. **Note:** You can specify two shield net names for only the following shield types: • `side` • `topSide` • `bottomSide` • `coaxial` For the `top`, `bottom`, or `topBottom` shield types, you can specify only one shield net. **Note:** The *Shield Net* and *Set OutsideSpacing* fields are mutually exclusive.
	Set ShieldWidth	Specifies the width of the shield wire in microns per layer.
	Set ShieldGap	Specifies the spacing between a shielded wire and a shield net.
	Set TandemWidth	Specifies the overhang value for the shields on the top and bottom layers so as to extend them to overlap the side shields.
	Connect Supply	Indicates how the shield wires will be connected to the supply line. The default option, `anyPoint`, tells the router to connect the wire to supply, anywhere along the length of the shield wire.
	Shield Type	Specifies the shielding type for the net(s) being routed.
	New	Lets you specify a new complex net constraint.
	Add/Update	Lets you add or modify an existing complex net constraint.
	Delete	Lets you delete a complex net constraint.

ICE - Simple NetClass

Use the *Simple NetClass* tab of the Integration Constraint Editor to specify simple netClass constraints that can be recognized by NanoRoute. Such constraints include:

- A netClass with an NDR.
  Or
- A netClass with a simple shield constraint group
  Or
- A netClass with the oacValidRoutingLayer defined in the Default Constraint Group of the netClass. Innovus copies the oacValidRouting layer to every net member of the netClass.

Note: OpenAccess does not allow you to place a shielding constraint on an `oaNetGroup` or a netClass. However, in Innovus, you can specify a shielding constraint using the *Simple NetClass* tab. Innovus then sets the same shielding internally on all the net members of a netClass. The shielding constraint is applicable for the nets in the netClass and not on the netClass itself.



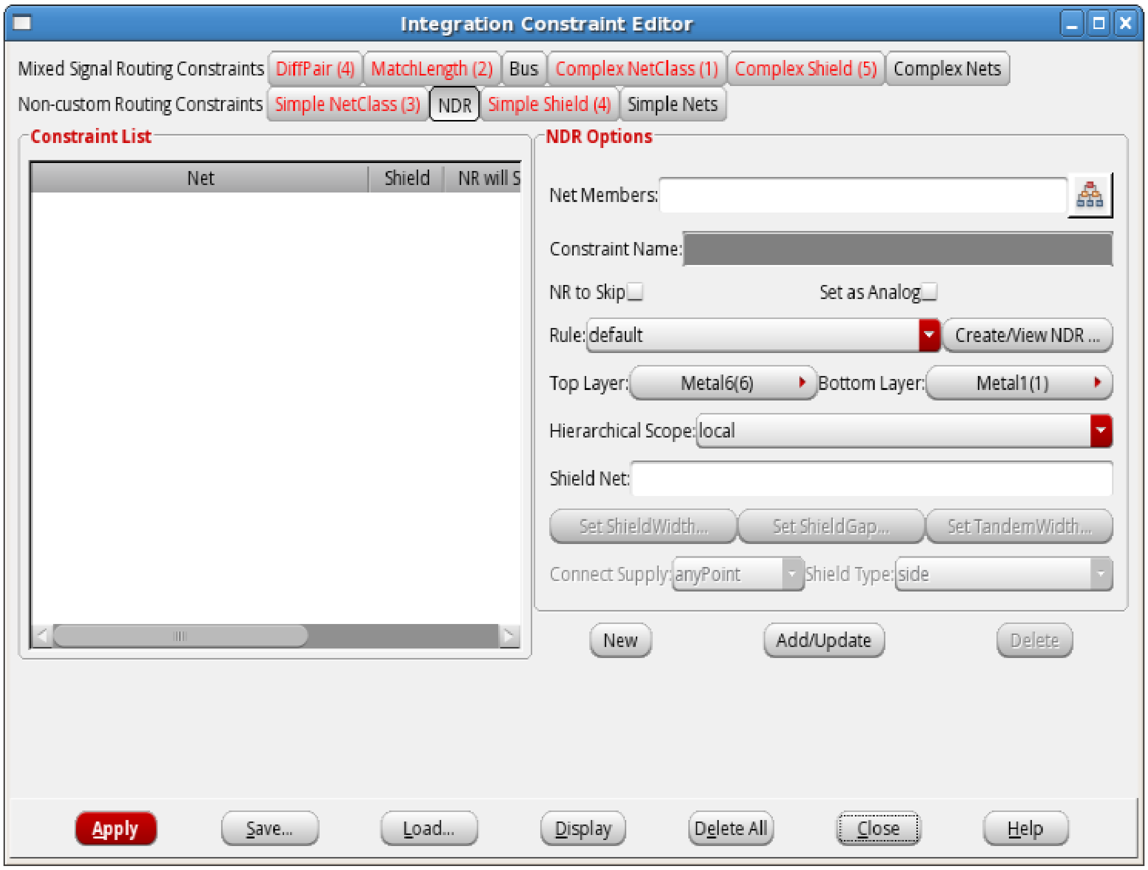
ICE - Simple NetClass Fields and Options

Constraint List	Displays the list of constraints. You can sort the list by one of the following columns: **Note:** These columns appear grayed out as they cannot be modified. They can be used only for sorting.	
	Nets	Displays the net name and enables you to sort constraints by net name.
	Shield	Specifies whether the net is shielded and enables you to sort by shielding. This check box is selected by default for nets on this tab as these nets have a simple shield constraint.
	NDR	Specifies whether the net has a non-default rule (NDR).
	NR will Skip	Specifies whether NanoRoute will skip the net. This check box is shown as selected if skip-routing is set on that particular net. Such nets are routed using custom routing techniques.
	Analog	Specifies whether the net has `sigType` set to `analog`. Many Virtuoso users use the `analog` attribute in their designs. This column makes it easy to determine whether or not a net has the `analog` attribute set from within the Innovus tool.
Simple NetClass Options		
	Net Members	Specifies the list of net names that are to be routed.
	Constraint Name	Displays the name of the constraint, as assigned in OpenAccess.
	NR to Skip	Sets skip-routing for the net so that NanoRoute will skip the net. Select this check box if you want the net to be routed using custom routing techniques.
	Set as Analog	Sets the `analog` attribute set for the net, if selected.
	Rule	Specifies the name of the routing rule that is used for routing a particular type of net(s).
	Create/View NDR	Lets you create a new NDR or view an existing NDR that is to be used for routing.
	Top Layer	Specifies the top routing layer that is to be used for routing.
	Bottom Layer	Specifies the bottom routing layer that is to be used during routing.

	Hierarchical Scope	Specifies whether the particular constraint is local, and/or can be pulled (above) or pushed (below) across the hierarchy. Setting this option to all possible values enables pull and push. If set to local, it is not saved to the database.
	Shield Net	Indicates that the net group should be shielded by the specified net(s). Valid net names are all power and ground net names in the design. You can specify different shield nets for different sides of a wire. The routers then determine which shield net should be used on which side of the wire. For a simple netClass constraint, the only allowed shield types are `side`, `none`, and `unspecified`. You can specify two shield net names for the `side` shield type.
	Set ShieldWidth	Specifies the width of the shield wire in microns per layer. You cannot specify shield width for a simple netClass constraint.
	Set ShieldGap	Specifies the spacing between a shielded wire and a shield net. You cannot specify shield gap for a simple netClass constraint.
	Set TandemWidth	Specifies the overhang value for the shields on the top and bottom layers so as to extend them to overlap the side shields. You cannot set tandem width for a simple netClass constraint.
	Connect Supply	Indicates how the shield wires will be connected to the supply line. The default option, `anyPoint`, tells the router to connect the wire to supply, anywhere along the length of the shield wire.
	Shield Type	Specifies the shielding type for the net(s) being routed. For a simple netClass constraint, the only allowed shield types are `side`, `none`, and `unspecified`.
	New	Lets you specify a new simple netClass constraint.
	Add/Update	Lets you add or modify an existing simple netClass constraint.
	Delete	Lets you delete a simple netClass constraint.

ICE - NDR

Use the NDR tab of the Integration Constraint Editor to specify constraints for nets with a valid non-default rule. Note that such nets show up in the Constraint List only when the NDR tab is selected. Even if these nets have a shield net assigned (making them also a simple shield net), the net names do not show up on the *Simple Shield* tab in accordance with the precedence rule.



ICE - NDR Fields and Options

Constraint List	Displays the list of constraints. You can sort the list by one of the following columns: **Note:** These columns appear grayed out as they cannot be modified. They can be used only for sorting.	
	Nets	Displays the net name and enables you to sort constraints by net name. **Note**: If the `oacValidRoutingLayers` attribute in the default constraint group of a net has been modified, the net will be show up in this column on the *NDR* tab.

	Shield	Specifies whether the net is shielded and enables you to sort by shielding. This check box is shown as selected for those nets on this tab that have a simple shield constraint.
	NR will Skip	Specifies whether NanoRoute will skip the net. This check box is shown as selected if skip-routing is set on that particular net. Such nets are routed using custom routing techniques.
	Analog	Specifies whether the net has `sigType` set to `analog`. Many Virtuoso users use the `analog` attribute in their designs. This column makes it easy to determine whether or not a net has the `analog` attribute set from within the Innovus tool.
NDR Options		
	Net Members	Specifies the list of net names that are to be routed.
	Constraint Name	Displays the name of the constraint, as assigned in OpenAccess.
	NR to Skip	Sets skip-routing for the net so that NanoRoute will skip the net. Select this check box if you want the net to be routed using custom routing techniques.
	Set as Analog	Sets the `analog` attribute set for the net, if selected.
	Rule	Specifies the name of the routing rule that is used for routing a particular type of net(s).
	Create/View NDR	Lets you create a new NDR or view an existing NDR that is to be used for routing.
	Top Layer	Specifies the top routing layer that is to be used for routing.
	Bottom Layer	Specifies the bottom routing layer that is to be used during routing.
	Hierarchical Scope	Specifies whether the particular constraint is local, and/or can be pulled (above) or pushed (below) across the hierarchy. Setting this option to all possible values enables pull and push. If set to local, it is not saved to the database.

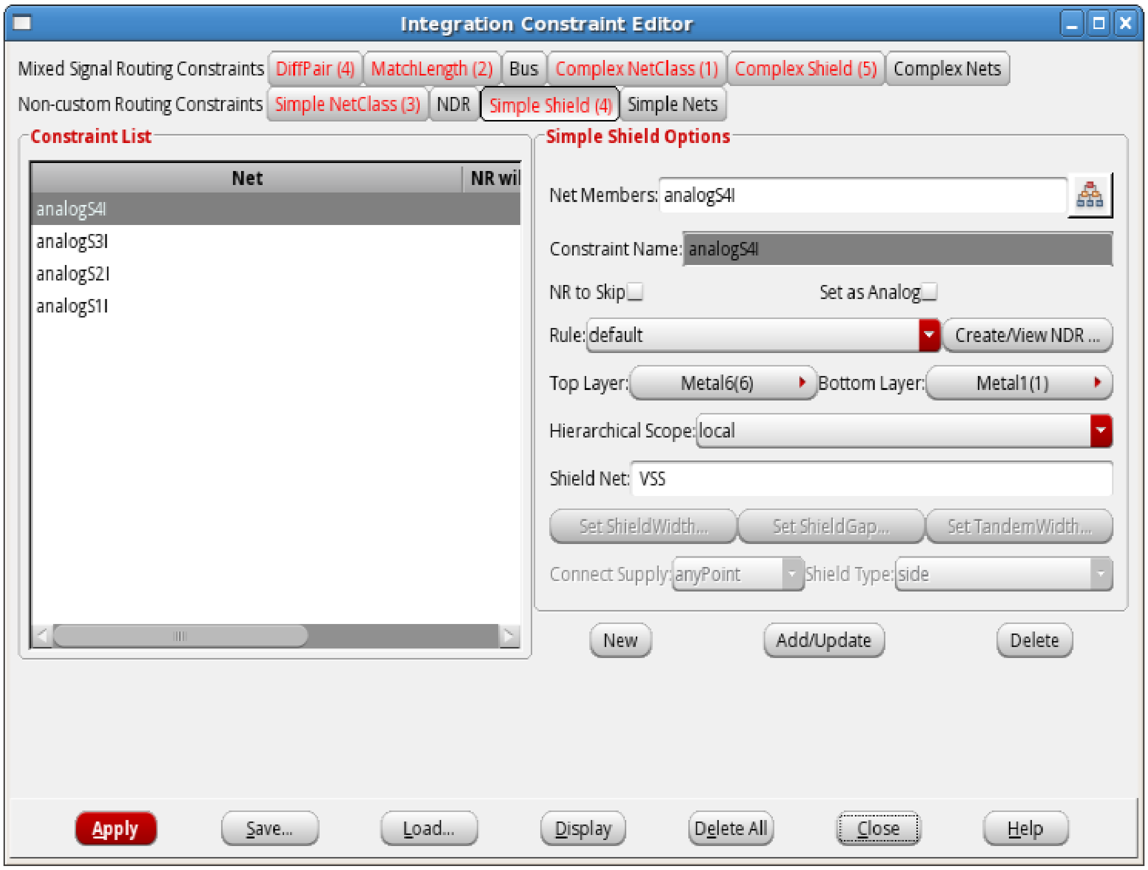
	Shield Net	Indicates that the net group should be shielded by the specified net(s). Valid net names are all power and ground net names in the design. You can specify different shield nets for different sides of a wire. The routers then determine which shield net should be used on which side of the wire. For an NDR constraint, the only allowed shield types are `side`, `none`, and `unspecified`. You can specify two shield net names for the `side` shield type.
	Set ShieldWidth	Specifies the width of the shield wire in microns per layer. You cannot specify shield width for an NDR constraint.
	Set ShieldGap	Specifies the spacing between a shielded wire and a shield net. You cannot specify shield gap for an NDR constraint.
	Set TandemWidth	Specifies the overhang value for the shields on the top and bottom layers so as to extend them to overlap the side shields. You cannot set tandem width for an NDR constraint.
	Connect Supply	Indicates how the shield wires will be connected to the supply line. The default option, `anyPoint`, tells the router to connect the wire to supply, anywhere along the length of the shield wire.
	Shield Type	Specifies the shielding type for the net(s) being routed. For an NDR constraint, the only allowed shield types are `side`, `none`, and `unspecified`.
	New	Lets you specify a new NDR constraint.
	Add/Update	Lets you add or modify an existing NDR constraint.
	Delete	Lets you delete an NDR constraint.

ICE - Simple Shield

Use the *Simple Shield* tab of the Integration Constraint Editor to specify simple shield constraints. A simple shield constraint is a shield constraint that:

- Has a shield net set on the net
  And
- Has no shield constraint group
  Or

Has a shield constraint group with shieldStyle set to *Parallel* or *Not Specified* in Virtuoso (that is, *Shield Type* set to none in Innovus).
And/Or
Has *Connect Supply* (msConnectSupply) set to `anyPoint` in the shield constraint group. The reason for this condition is that NanoRoute connects to the supply by default, and there is no way to leave a shield net unconnected to supply in NanoRoute.



ICE - Simple Shield Fields and Options

Constraint List	Displays the list of constraints. You can sort the list by one of the following columns: **Note:** These columns appear grayed out as they cannot be modified. They can be used only for sorting.	
	Net	Displays the net name and enables you to sort constraints by net name.
	NR will Skip	Specifies whether NanoRoute will skip the net. This check box is shown as selected if skip-routing is set on that particular net. Such nets are routed using custom routing techniques.

	Analog	Specifies whether the net has `sigType` set to `analog`. Many Virtuoso users use the `analog` attribute in their designs. This column makes it easy to determine whether or not a net has the `analog` attribute set from within the Innovus tool.
Simple Shield Options		
	Net Members	Specifies the list of net names that are to be routed.
	Constraint Name	Displays the name of the constraint, as assigned in OpenAccess.
	NR to Skip	Sets skip-routing for the net so that NanoRoute will skip the net. Select this check box if you want the net to be routed using custom routing techniques.
	Set as Analog	Sets the `analog` attribute set for the net, if selected.
	Rule	Specifies the name of the routing rule that is used for routing a particular type of net(s).
	Create/View NDR	Lets you create a new NDR or view an existing NDR that is to be used for routing.
	Top Layer	Specifies the top routing layer that is to be used for routing.
	Bottom Layer	Specifies the bottom routing layer that is to be used during routing.
	Hierarchical Scope	Specifies whether the particular constraint is local, and/or can be pulled (above) or pushed (below) across the hierarchy. Setting this option to all possible values enables pull and push. If set to local, it is not saved to the database.
	Shield Net	Indicates that the net group should be shielded by the specified net(s). Valid net names are all power and ground net names in the design. You can specify different shield nets for different sides of a wire. The routers then determine which shield net should be used on which side of the wire. For a simple shield constraint, the only allowed shield types are `side`, `none`, and `unspecified`. You can specify two shield net names for the `side` shield type.
	Set ShieldWidth	Specifies the width of the shield wire in microns per layer. You cannot specify shield width for a simple shield constraint.

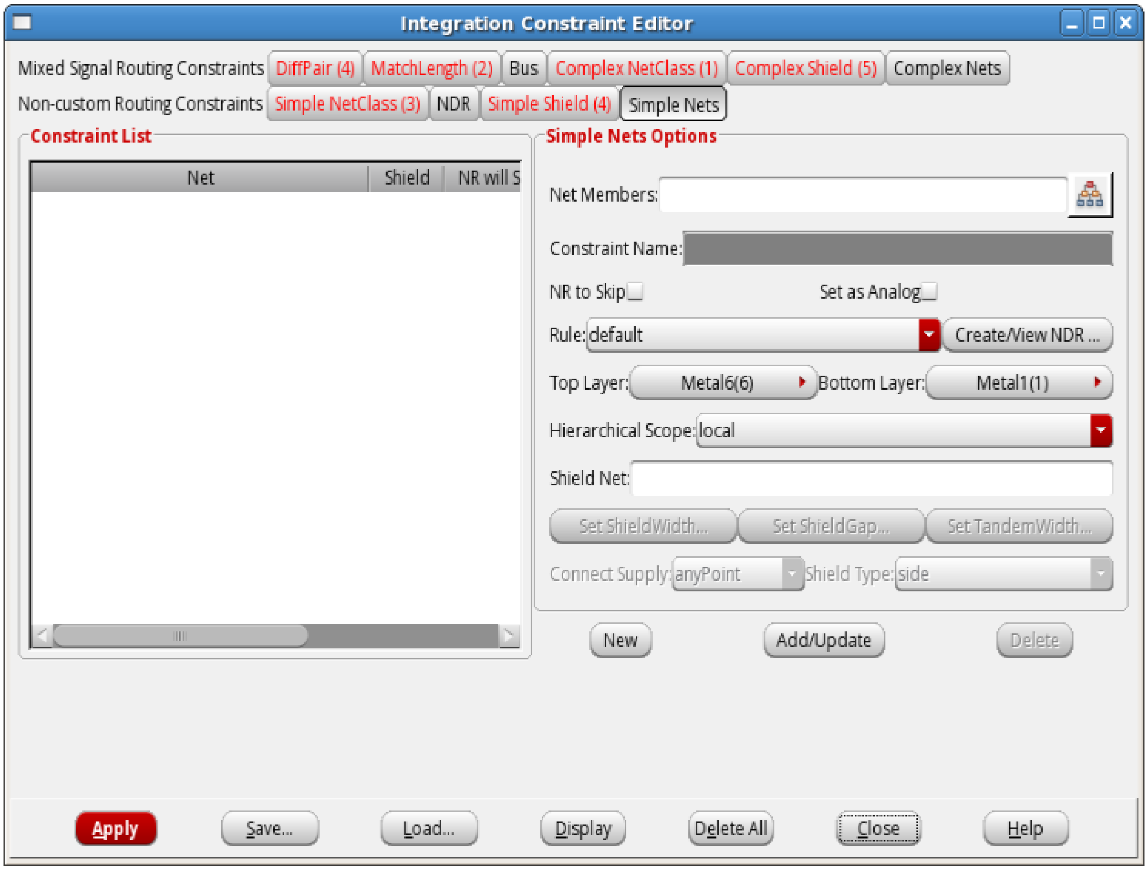
	Set ShieldGap	Specifies the spacing between a shielded wire and a shield net. You cannot specify shield gap for a simple shield constraint.
	Set TandemWidth	Specifies the overhang value for the shields on the top and bottom layers so as to extend them to overlap the side shields. You cannot set tandem width for a simple shield constraint.
	Connect Supply	Indicates how the shield wires will be connected to the supply line. The default option, `anyPoint`, tells the router to connect the wire to supply, anywhere along the length of the shield wire.
	Shield Type	Specifies the shielding type for the net(s) being routed. For a simple shield constraint, the only allowed shield types are `side`, `none`, and `unspecified`.
	New	Lets you specify a new simple shield constraint.
	Add/Update	Lets you add or modify an existing simple shield constraint.
	Delete	Lets you delete a simple shield constraint.

ICE - Simple Nets

Use the *Simple Nets* tab of the Integration Constraint Editor to specify simple net constraints. A simple net is a net that:

- Has *Rule* set to `default`.
- Has the top and bottom layers defined as valid routing layers for Innovus. This means no Poly layer is defined as a valid routing layer.
  Or
  Does not have top or bottom layers defined.
- Can optionally have the *NR to Skip* or *Set as Analog* attribute set.
- Can have any choice for *Hierarchical Scope*.

These types of Nets will all be routed using NR, unless the user has specified the “NR to Skip” attribute.



ICE - Simple Nets Fields and Options

Constraint List	Displays the list of constraints. You can sort the list by one of the following columns: **Note:** These columns appear grayed out as they cannot be modified. They can be used only for sorting.	
	Net	Displays the net name and enables you to sort constraints by net name.
	Shield	Specifies whether the net is shielded and enables you to sort by shielding. This check box is shown as selected for those nets on this tab that have a simple shield constraint.
	NR will Skip	Specifies whether NanoRoute will skip the net. This check box is shown as selected if skip-routing is set on that particular net. Such nets are routed using custom routing techniques.

	Analog	Specifies whether the net has `sigType` set to `analog`. Many Virtuoso users use the `analog` attribute in their designs. This column makes it easy to determine whether or not a net has the `analog` attribute set from within the Innovus tool.
Simple Net Options		
	Net Members	Specifies the list of net names that are to be routed.
	Constraint Name	Displays the name of the constraint, as assigned in OpenAccess.
	NR to Skip	Sets skip-routing for the net so that NanoRoute will skip the net. Select this check box if you want the net to be routed using custom routing techniques.
	Set as Analog	Sets the `analog` attribute set for the net, if selected.
	Rule	Specifies the name of the routing rule that is used for routing a particular type of net(s). For simple nets, *Rule* is always set to `default`.
	Create/View NDR	Lets you create a new NDR or view an existing NDR that is to be used for routing.
	Top Layer	Specifies the top routing layer that is to be used for routing.
	Bottom Layer	Specifies the bottom routing layer that is to be used during routing.
	Hierarchical Scope	Specifies whether the particular constraint is local, and/or can be pulled (above) or pushed (below) across the hierarchy. Setting this option to all possible values enables pull and push. If set to local, it is not saved to the database.
	Shield Net	Indicates that the net group should be shielded by the specified net(s). Valid net names are all power and ground net names in the design. You can specify different shield nets for different sides of a wire. The routers then determine which shield net should be used on which side of the wire. For a simple net constraint, the only allowed shield types are `side`, `none`, and `unspecified`. You can specify two shield net names for the `side` shield type.
	Set ShieldWidth	Specifies the width of the shield wire in microns per layer. You cannot specify shield width for a simple net constraint.
	Set ShieldGap	Specifies the spacing between a shielded wire and a shield net. You cannot specify shield gap for a simple net constraint.

	Set TandemWidth	Specifies the overhang value for the shields on the top and bottom layers so as to extend them to overlap the side shields. You cannot set tandem width for a simple net constraint.
	Connect Supply	Indicates how the shield wires will be connected to the supply line. The default option, `anyPoint`, tells the router to connect the wire to supply, anywhere along the length of the shield wire.
	Shield Type	Specifies the shielding type for the net(s) being routed. For a simple net constraint, the only allowed shield types are `side`, `none`, and `unspecified`.
	New	Lets you specify a new simple net constraint.
	Add/Update	Lets you add or modify an existing simple net constraint.
	Delete	Lets you delete a simple net constraint.

Related Text Commands

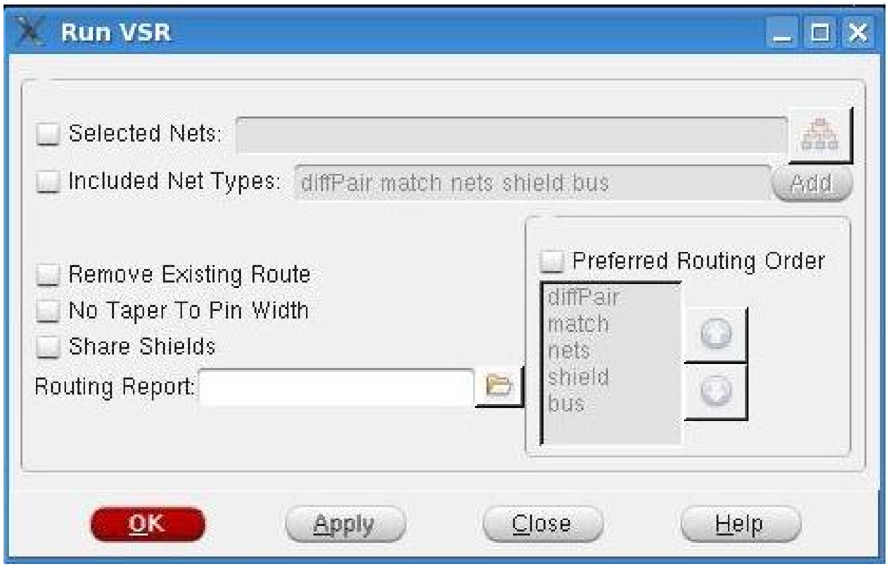
For information on the following command, see "Mixed Signal Commands" in the *Text Command Reference*.

- `setIntegRouteConstraint`

Run VSR

Use the Run Virtuoso Space-based Router (VSR) to route the nets. It routes the selected nets in the following order: *diffPair*, *match*, *nets*, *shield,* and *bus*.

- Choose *Tools - Mixed Signal - Run VSR*



Run VSR Fields and Options

Selected Nets	Specifies the list of nets names which have to be routed.
Included Net Types	Specifies the list of net types for VSR to route.
Remove Existing Route	Deletes the nets (`fixed`, `normal`), including shield, and excluding power nets, which are specified by *Selected Nets* before routing.
No Taper To Pin Width	Does not perform tapering based on the pin width. For instance, if the rule applied on a mixed signal net is NDR1 whose width exceeds the pin width for a particular layer, then VSR automatically tapers the wire to match the pin width. If this option is specified, then tapering is not done.
Share Shields	Shares the shielded nets. Using this parameter, you can selectively specify the list of shared shielded nets.
Routing Report	Specifies the file name for writing the routing report.
Preferred Routing Order	Specifies the list of valid constraint types in the preferred routing order.

Related Text Commands

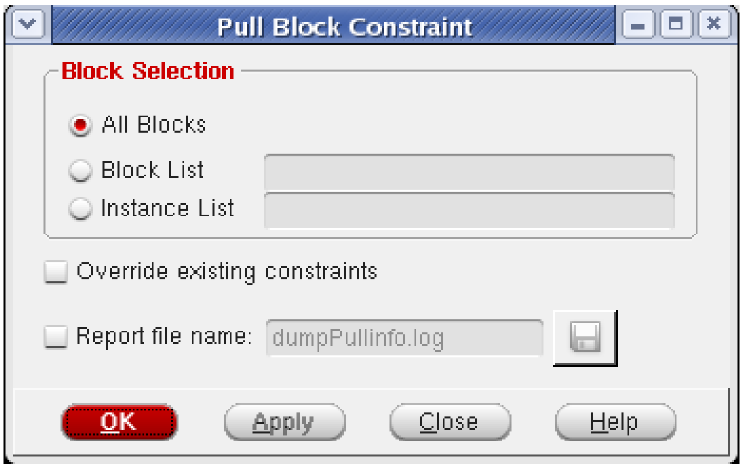
For information on the following command, see Mixed Signal Commands in the *Text Command Reference*.

- `run_vsr`

Pull Block Constraint

Use the Pull Block Constraint form to pull the routing constraints stored on the interface nets of blocks in a design, to their corresponding top-level nets.

- Choose *Tools - Mixed Signal - Pull Block Constraint.*



Block Selection	Defines the list of block names of the instances in the design for which the constraints will be pulled.
Override existing constraints	Specifies that the lower-level net constraints will override any constraints that might exist on the top-level nets.
Report file name	Specifies the report file name. Given that the standard out report is in the abbreviated format, more details are written out in this mode indicating: • The lower, and upper level net names, the type of constraints pulled. • All the associated parameters. • Any conflicts that need to be resolved. • Which constraint were written to a particular net.

Related Text Commands

For information on the following command, see Mixed Signal Commands in the *Text Command Reference*.

- `pull_block_constraint`

Set Multiple CPU Usage

Use the *Options - Set Multiple CPU Usage* command to acess the Multiple CPU Processing form. Using this form, you can set options for multi-threading, distributed processing, and Superthreading.

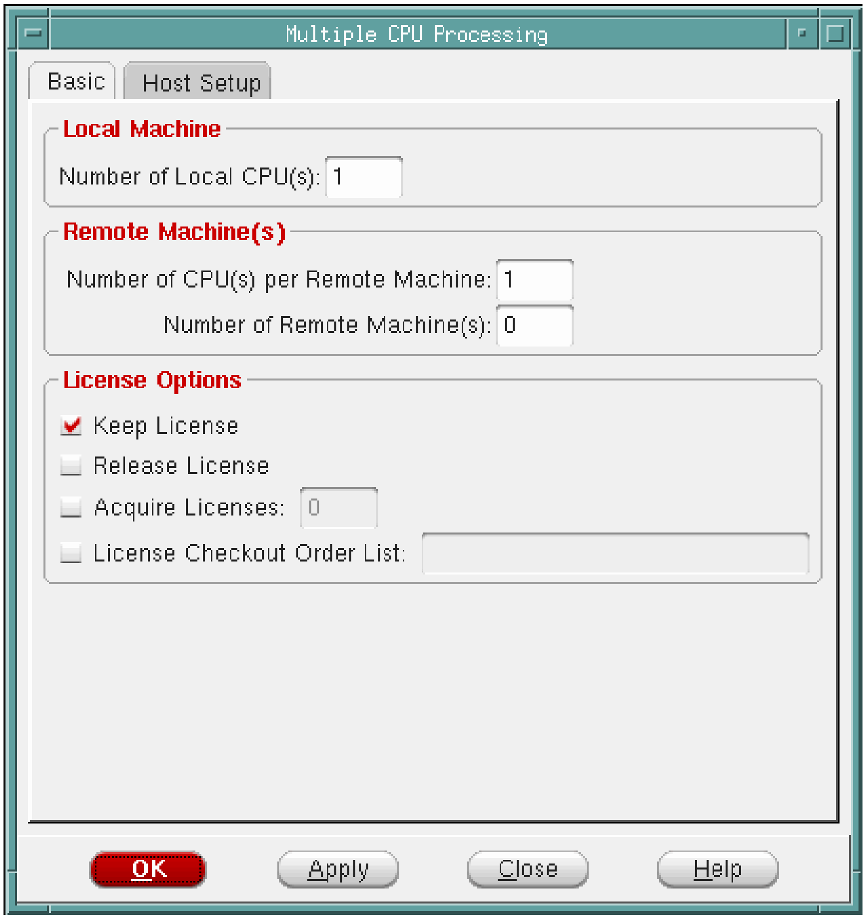
The Multiple CPU Processing form contains the following pages:

- Multiple CPU Processing - Basic
- Multiple CPU Processing - Host Setup

Multiple CPU Processing - Basic

Use the *Basic* page of the Multiple CPU Processing form to specify options for multi-threading, distributed processing, and Superthreading.

- Choose *Options - Set Multiple CPU Usage* and click the *Basic* tab.



Multiple CPU Processing - Basic Fields and Options

Local Machine *Number of Local CPU(s)*	
	Specifies the number of CPUs on the local machine. This option is required for multi-threading. *Default:* 1
Remote Machine(s) *Number of CPU(s) per Remote Machine*	

	Specifies the number of CPUs on each of the remote machines. This option is required for superthreading. For Superthreading, you must use this option in conjunction with the *Number of Remote Machine(s)* option. *Default:* 1
Number of Remote Machine(s)	
	Specifies the number of remote machines. This option is required for distributed processing and superthreading. *Default:* 0
License Options	
Keep License	Specifies whether to keep the acquired multiple CPU-licenses until the current session ends. Select this option before running any commands that require multiple-CPU applications. To release all multiple-CPU licenses immediately, select the Release License option.
Release License	Releases all multiple-CPU license(s) immediately. By default, the software holds multiple-CPU licenses until the end of the current session. To specify that the software should release multiple-CPU licenses after every multiple-CPU command runs, select the Keep License option.
Acquire License	Acquires licenses to enable the specified number of CPUs. For example, if you specify 5, the software checks out enough licenses to enable 5 CPUs. After the licenses are checked out, they can be used for multi-threading, distributed processing, or superthreading.
License Checkout Order List	
	Specifies the list or order of licenses the software should use for checking out licenses during multiple-CPU processing.

Related Text Command

- setMultiCpuUsage

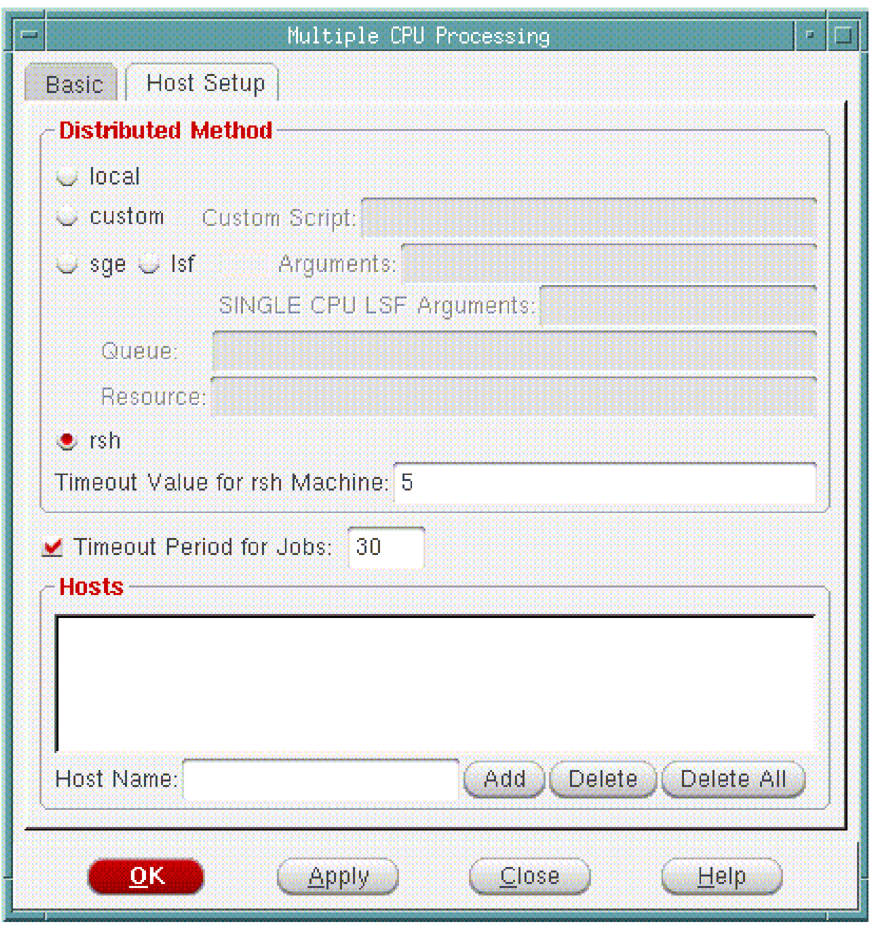
Related Topics

- Accelerating the Design Process By Using Multiple-CPU Processing chapter in the *Innovus User Guide*

Multiple CPU Processing - Host Setup

Use the *Host Setup* page of the Multiple CPU Processing form to specify options for distributed processing and Superthreading.

- Choose *Options - Set Multiple CPU Usage* and click the *Host Setup* tab.



Multiple CPU Processing - Host Setup Fields and Options

Distributed Method	Specifies the type of distributed processing to run. Select one of the following options:	
	local	Runs all distributed processing jobs on the master machine.
	custom	Specifies a custom configuration.
		Custom Script
		Specifies a custom script to run distributed processing.
	lsf	Specifies a Load Sharing Facility configuration. If you do not specify any values in the *LSF Arguments* text entry box, the software uses default settings. To use this option, LSF must already be set up (typically by specifying theLSF_ENVDIR and LSF_SERVERDIRenvironment variables) and bsub must be in your search path. Contact your LSF administrator for details.
	sge	Specifies a Sun Grid Engine configuration. For more information, see the SGE documentation.
		Arguments
		Specifies any additional arguments you need to provide to the Sun Grid Engine (SGE) or Load Sharing Facility (LSF) job submission command.
		Single CPU LSF Arguments
		Specifies the bsub options. For information, see the LSF documentation. You must use this option to adjust the LSF argument for a single CPU application.
	Queue	
		Specifies the queue for the LSF or SGE configuration. The software uses the default queue name if you do not specify one.
	Resource	

		Specifies a resource string for the LSF or SGE queue. Icon The correct resource string is specific to your installation. Contact your LSF administrator for the appropriate parameters and values.
	rsh	Creates or modifies a remote shell (rsh) configuration.
Timeout Value for rsh Machine		
	Specifies the number of seconds the host machine waits for other machines to become available for multiple-CPU processing. *Default:* 5 This field will be enabled only when *rsh* is selected.	
Timeout Period for Jobs		
	Specifies the default timeout (in seconds) for a submitted job that will never start. This functionality prevents the master machine from hanging when the slaves do not come up for some reason. *Default:* 30 (local/rsh/custom) and 3600 (lsf/sge)	
Hosts	Specifies the remote hosts to use for distributed processing.	
	Host Name	Specifies the hosts to add or remove.

Related Text Command

- `setDistributeHost`

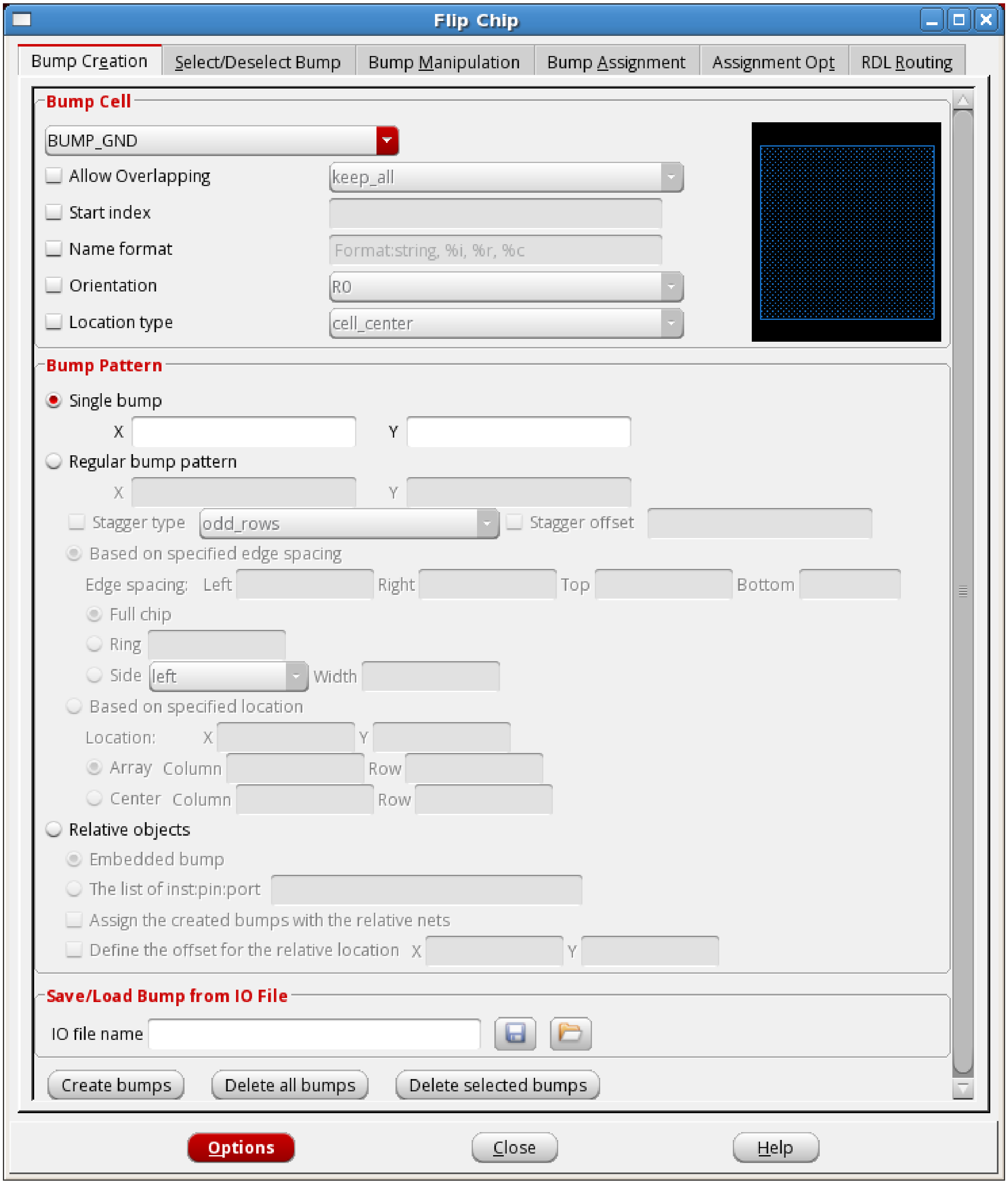
Related Topics

- Accelerating the Design Process By Using Multiple-CPU Processing chapter in the *Innovus User Guide*

Flip Chip

Use the Flip Chip form to perform all flip chip design flow tasks. The Flip Chip form is based on the flip chip design flow.

- To open the Flip Chip form, choose *Tools* - *Flip Chip*.



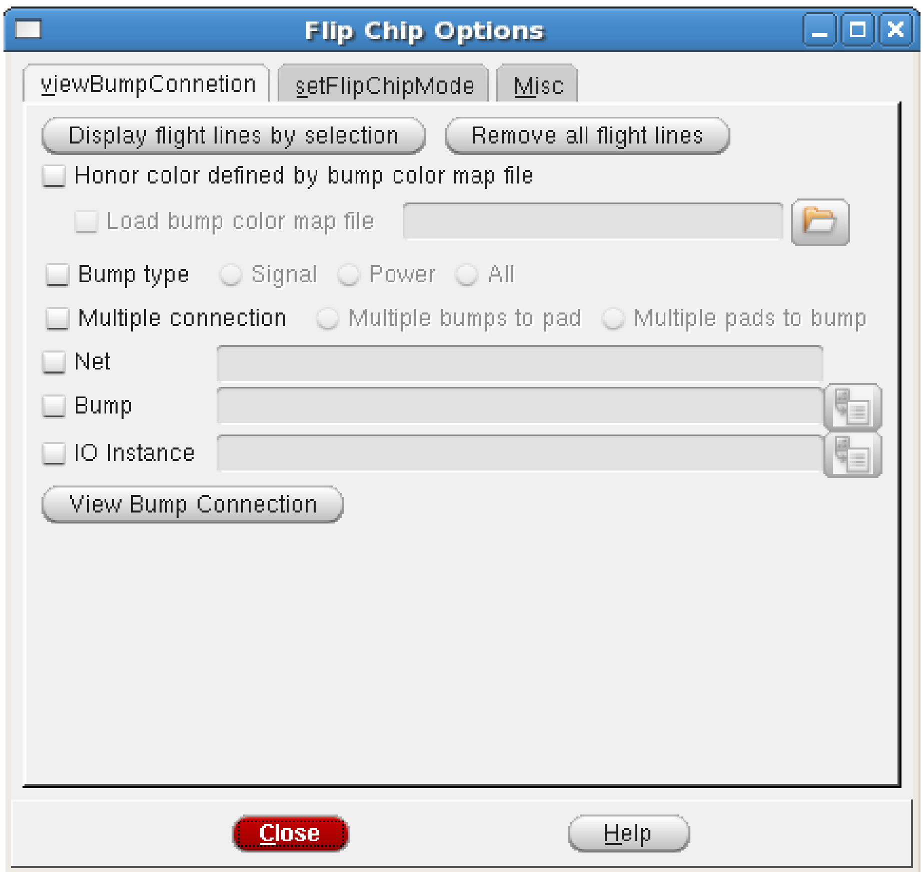
The Flip Chip has the following tabs:

- Bump Creation
- Select/Deselect Bump
- Bump Manipulation

- Bump Assignment
- Assignment Opt
- RDL Routing

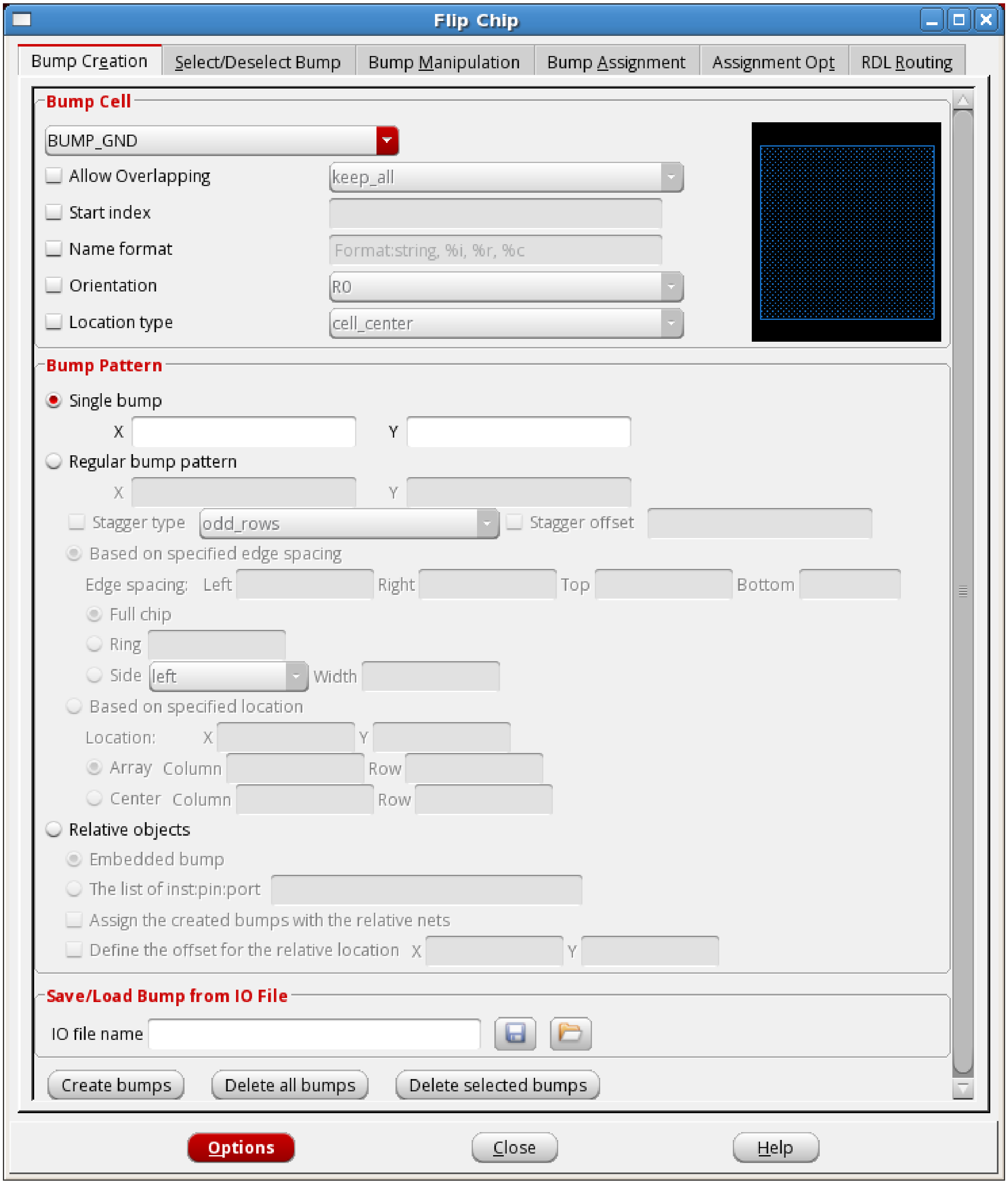
In addition, you can click the *Options* button to access the Flip Chip Options form, which provides the following pages:

- viewBumpConnection
- setFlipChipMode
- Misc



Bump Creation

Use the Bump Creation page in the Flip Chip form to create bumps or delete bumps.



Bump Creation Fields and Options

Bump Cell	Specifies the name of the bump cell, which is used to create bumps. A drop-down list is available to enable you to select a specific bump cell. The shape of the selected bump cell is displayed on the right. *Default*: `BUMP_GND`
Allow overlapping	Allows overlapping bumps in bump generation. By default, if a bump overlaps with another bump in geometry, it will not be created. If this option is specified, existing bumps will be ignored. *Default*: Off
Start index	Specifies the starting number of the index for the bumps to be created. *Default*: Off
Name format	Specifies the format for the bump name like a `printf` format, except that it uses `%i` for index, `%r` for row number, and `%c` for column number. The index starts at one more than the number of existing bumps in the design, unless *Start index* is specified and increments for each bump created. This means if there are no bumps in the design, the index starts at `1` and if there are 100 bumps in the design, the index starts at 101. The default name format is `Bump_%i`. Therefore, if there are no bumps in the design, the tool generates bumps named `Bump_1`, `Bump_2`, and so on, by default. Some examples of the possible format are: • *`prefix_`*`%i`*`_string_`*`%r_%c`*`_suffix`* • `%i` • *`bumpname`* If there are any name collisions, an ERROR occurs and the bump pattern is not created.
Orientation	Specifies the orientation of the bump for bump generation. A drop-down list is available to enable you to select a specific orientation. For more information, see Orientation. Use this option if you are creating a pillar bump. A pillar bump can be rectangular and you may rotate the pillar bump by 90/180/270 degrees to alleviate package and chip routing problem. *Default:* `R0` **Note**: If you are creating a regular C4 bump, which is either octagonal or square in shape, rotation does not change its footprint in silicon.

Location type	Specifies the location type for bump creation. A drop-down list is available to enable you to select a specific location type. *Default*: `cell_center`	
Bump Pattern		
Single bump	Creates a single bump at the specified *Location* coordinates. This is the default *Bump Pattern* option. *Default*: On	
	X Y	Specifies the X and Y coordinates of the bump to be created.
Regular bump pattern	Creates bumps in a specific pattern depending on other options you specify.	
	X Y	Specifies the distance between bump centers in microns. Bump pitch is interpreted in different ways for different bump patterns. For *Full chip* and *Side* patterns: • *X* represents the distance between the bump centers in a row or horizontal. • *Y* means the distance between the bump centers in a column or vertical. For *Ring*: • *X* represents the distance between the bump centers in the ring. • *Y* represents the distance between rings from the bump center.

<table>
<tr><td></td><td>Stagger type</td><td colspan="2">Specifies the stagger type pattern. This option cannot be used with Ring pattern.

The allowed values for the Stagger type are:
<code>odd_rows</code> - Creates a bump array with the odd rows shifted to the right by the specified stagger offset value.
<code>odd_columns</code> - Creates a bump array with the odd columns shifted up by the specified stagger offset value.
<code>even_rows</code> - Creates a bump array with the even rows shifted to the right by the specified stagger offset value.
<code>even_columns</code> - Creates a bump array with the even columns shifted up by the specified stagger offset value.
<code>trapezoid</code> - Creates bumps are created in a trapezium pattern. This stagger type is supported only with <code>-pattern_side</code>.
You can use the Stagger offset option along with Stagger type to specify the offset of bumps between rows or columns in the generated bump pattern.</td></tr>
<tr><td></td><td>Stagger offset</td><td colspan="2">Specifies the offset of bumps between rows or columns in the generated bump pattern. Its value is specified in microns. This option is used with Stagger type.</td></tr>
<tr><td></td><td>Based on specified edge spacing</td><td colspan="2">Specifies that the array of bumps should be created based on the edge spacing options you specify.</td></tr>
<tr><td></td><td></td><td>Edge spacing</td><td>Specifies the minimum distances in microns to the edge of the chip from the lower left or center of the outermost bumps. The Location type value determines which point of the bump (lower-left or center of the cell or geometry) is used to compute the distance to the edge. The arrays start at the left, bottom location and extend to the right and top.</td></tr>
<tr><td></td><td></td><td>Full chip</td><td>Creates an array of bumps covering the chip. The array starts at the closest to boundary point set by Edge spacing and extends until within the Edge spacing values of the chip boundary for the opposite sides. You can optionally directly specify the Location values for the starting point, in which case Edge spacing affects only the two opposite edges of the array.</td></tr>
</table>

		Ring	Creates a ring of bumps around the boundary of the chip that is as many bumps wide as the specified integer value. The ring extends until within *Edge spacing* value of the chip boundary, starting at the lower-left *Edge spacing* value. The *X* value is the spacing between bumps inside one ring, and the *Y* value is the spacing between two rings.
		Side	Creates an array of bumps along the specified side of the chip. A drop-down list is available to enable you to select a specific side. The array is the length of the specified side, and *Width* bumps wide, where *Width* is an integer value. The array starts at the lower-left *Edge spacing* value, and extends until within the *Edge spacing* values of the top/right sides. *Default*: `left`
	Based on specified location	Specifies that the array of bumps should be created based on the location values you specify.	
		Location	*X* - Specifies the X coordinate of the first bump in the array. *Y* - Specifies the Y coordinate of the first bump in the array.
		Array	Creates an array of bumps. The lower-left bump starts at the specified *Location* coordinates. The array extends to the number of *Column* and *Row* values specified.
		Center	Creates an array of bumps that is centered on the center of the chip and that extends for the number of *Column* and *Row* values specified. The center point can optionally be set directly with the specified *Location* coordinates. The location of the lower-left bump is determined as follows: `{(Column-1)/2*(Bump Pitch X) (Row-1)/2*(Bump Pitch Y)}`
	Relative objects	Creates bumps based on specified relative object.	

		Embedded bump	Specifies that an embedded bump is the relative object. When this option is selected, the tool automatically creates a bump at the same location as the embedded bump. The bump is named *`$blockName/$pinName/embeddedBump_$index`* , where: • *`$blockName`* is the name of the block in the top design that has the corresponding embedded bump. • *`$pinName`* is the name of the pin in LEF that has the corresponding embedded bump. You can reset the default settings by using the *Start index* and *Name format* options. If there are already overlapping bumps for some embedded bumps, the tool skips creating bumps for those embedded bumps but continues to create bumps for remaining embedded bumps and issues the following warning message. `WARNING (#): There is(are) overlap bump(s) with the embedded bump $blockName/$pinName located at {x2 y2} with relative offset {x y}. Skip creating bump for it.`
		The list of inst:pin:port	Indicates that the inst:pin:port list specified in the field provided is the relative object for creating bumps. The inst:pin:port list supports wild cards. The format is `{inst:pin:port ...}` and `port` is of type integer. When this option is specified, bumps are created by default at the geometry center of the specified ports. The bump is named *`$blockName-$pinName-Port_$portNumber-embeddedBump_$index`* , where: • *`$blockName`* is the name of the block in the top design which has the corresponding embedded bump. • *`$pinName`* is the name of the pin in LEF which has the corresponding embedded bump. • *`$portNumber`* is the number of the port on which the created bump is based. **Example**: `Avd_test_1-DQ0-Port_1-embeddedBump_1` You can reset the default settings by using the *Start index* and *Name format* options.

<table>
<tr><td></td><td></td><td>Assign the created bumps with the relative nets</td><td>Assigns the corresponding net of the relative object to the bump being created.
If the Embedded bump option is selected, the tool searches the top netlist for the net connected to the pin of the embedded bump and assigns it to the created bump.
If The list of inst:pin:port is selected and the inst:pin:port details specified, the tool searches the top netlist for the net connected to the specified pin and assigns it to the created bump.</td></tr>
<tr><td></td><td></td><td>Define the offset for the relative location</td><td>Specifies the X and Y offset values of the bump location compared with the relative object. The geometry center of the created bump is the geometry center of the relative object plus the offset.</td></tr>
<tr><td>IO file name</td><td colspan="3">Specifies I/O file name. Use the Save button to save bumps to the I/O file. Use the Load button to load bumps from the I/O file.</td></tr>
<tr><td>Create bumps</td><td colspan="3">Creates bumps based on the options you have specified.</td></tr>
<tr><td>Delete all bumps</td><td colspan="3">Deletes all bumps.</td></tr>
<tr><td>Delete selected bumps</td><td colspan="3">Deletes selected bumps. You must select the bumps in the design display area before using this option.</td></tr>
</table>

Orientation Key

Use the following table as a key to row orientation.

Value	Definition
R0	No rotation
MX	Mirror through the x axis
MY	Mirror through the y axis

R180	Rotate counter-clockwise 180 degrees
MX90	Mirror through the x axis and rotate counter-clockwise 90 degrees
R90	Rotate counter-clockwise 90 degrees
R270	Rotate counter-clockwise 270 degrees
MY90	Mirror through the y axis and rotate counter-clockwise 90 degrees

Related Topics

- Flip Chip Methodologies

Select/Deselect Bump

Use the *Select/Deselect Bump* page to select or deselect bumps.

- To open the *Select/Deselect Bump* page, choose *Tools - Flip Chip* and select *Select/Deselect Bump*.

Select/Deselect Bump Fields and Options

<table>
<tr><td>All</td><td colspan="2">Selects or deselects all bumps in the design.</td></tr>
<tr><td>Floating</td><td colspan="2">Selects or deselects only the unassigned or floating bumps.</td></tr>
<tr><td>Assigned</td><td colspan="2">Selects or deselects only the bumps that are assigned.</td></tr>
<tr><td>By Bump Cell Name</td><td colspan="2">Specifies names of bump cells and the bumps with these bump cells are selected/deselected. You can use wildcards in the bump cell list.</td></tr>
<tr><td>By Bump Name</td><td colspan="2">Specifies names of the bumps to be selected or deselected. You can use wildcards in the bump list.</td></tr>
<tr><td>By Net</td><td colspan="2">Specifies names of nets and the related bumps are selected or deselected. You can use wildcards in the net list.</td></tr>
<tr><td>By Type</td><td colspan="2">Selects or deselects bumps by type. You can choose one of the following options:
• Signal
• Power
• Ground
Default: Signal</td></tr>
<tr><td>By Side</td><td colspan="2">Selects or deselects bumps relative to the specified side. You can choose one of the following options:
• Top
• Bottom
• Left
• Right
Default: Top</td></tr>
<tr><td></td><td>Maximum distance to side</td><td>Specifies the maximum distance away from the side in microns. When specified, only the bumps with geometries completely in that region are selected/deselected.
By default, half the width/height of the die is used as the maximum distance to each side.
For <code>distance</code>, minimum value is <code>0</code> and maximum is <code>1e+20</code>.</td></tr>
</table>

Alternate Bump Pattern	Specifies the alternate bump pattern, which can be either *Row* or *Column*. You have to select an area to be alternate-selected (or deselected) before using this option.	
	Start lower left	If you are selecting bumps (*Select Bumps*), specifies the start point of alternate selection. If it is not specified, the lower-left point is considered the start point of alternate deselection. If you are deselecting bumps (*Des elect Bumps*), specifies the start point of alternate deselection. If it is not specified, the lower-left point is considered the start point of alternate selection.
Select Bumps	Selects bumps based on the options you have specified.	
Deselect Bumps	Deselects bumps based on the options you have specified.	

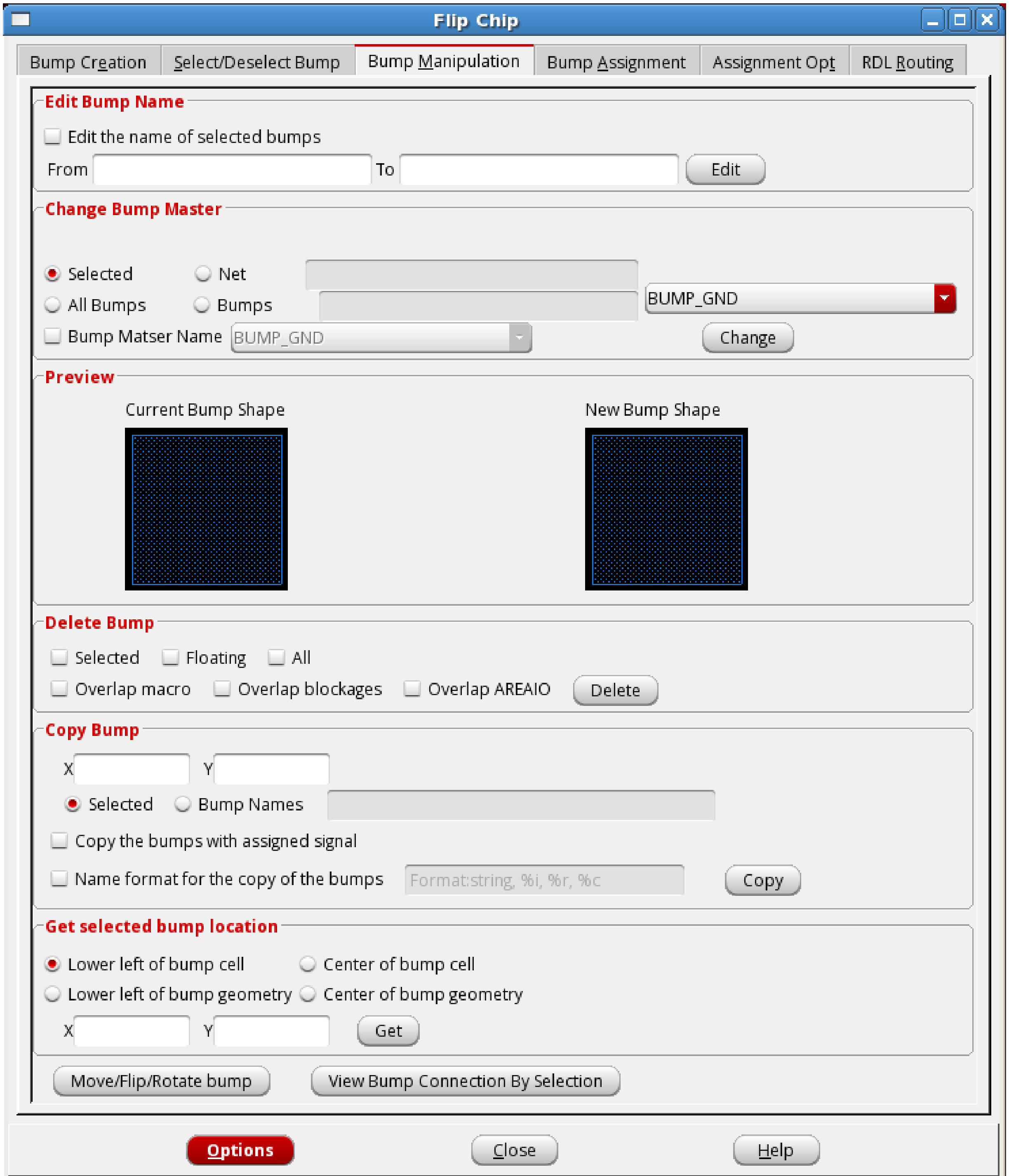
Related Topics

- Flip Chip Methodologies

Bump Manipulation

Use the *Bump Manipulation* page to edit, delete, or copy bumps and view bump connections.

- To open the *Bump Manipulation* page, choose *Tools* - *Flip Chip* and select *Bump Manipulation*.



Bump Manipulation Fields and Options

Edit Bump Name

Edit the name of selected bumps	Modifies the names of selected bumps.	
From	Specifies the name of a single bump or a pattern for the names of the bumps to be edited. The pattern is a regular expression, such as `{Bump_\d+}` or `{Bump_(\d)(\w+)}`, which can be referred in TCL. When specifying a pattern, the opening and closing braces are required.	
To	Specifies the new name or name format for target bumps. When specifying a name format, the opening and closing braces are required.	
Edit	Changes the names of selected or specified bumps according to the specified pattern.	
Change Bump Master		
From Bump Master Name	Provides options for specifying bumps for which bump master needs to be replaced.	
	Selected	Changes the bump master of selected bumps to the new cell master.
	Net	Specifies that all bumps connected to the specified net will use the new cell master. For example, if you specify VDD in the *Net* text box, all bumps connected to VDD will use the cell master specified with *New Bump Master Name*.
	All Bumps	Specifies that all bumps will use the new cell master specified with *New Bump Master Name*.
	Bumps	Specifies the list of bumps for which you want to change the bump master. Use this option if you want to change the cell master of specific bumps, which may or may not have the same cell master originally.
	Bump Master Name	Specifies the name of the old cell master. Use this option to replace the cell master of bumps using a specific bump master.
Change	Replaces the cell master for specified bumps. You can select the name of the new cell master from the associated drop-down list.	
Preview	Displays the shape of the current bump master as well as the new bump master you select in the *New Bump Master Name* field.	
Delete Bump		
Selected	Deletes selected bumps. You must first select the bumps in the design display area, then use this option to delete the bumps.	

Floating	Deletes bumps which are not assigned to any nets.
All	Deletes all bumps.
Overlap macro	Deletes all bumps that overlap the selected macros. You must first select the macros in the design display area, then use this option to delete the bumps.
Overlap blockages	Deletes all bumps that overlap routing blockages on the same layer. For example, if a bump on layer M7 overlaps a routing blockage on layer M7, the bump is deleted when you use this option.
Overlap AREAIO	Deletes bumps that overlap with the area I/O cells. You must first select the area I/O cells in the design display area, then use this option to delete the bumps.
Delete	Removes the specified bumps from the design.
Copy Bump	
X Y	Specifies the distance in microns from the source location to the target location in *X*/*Y* direction.
Selected	Copies only the selected bumps.
Bump Names	Specifies names of the bumps to be copied. You can use wildcards in the bump list.
Copy the bumps with assigned signal	Copies the bumps and their assigned signals.
Name format for the copy of the bumps	Specifies the name format for the target bumps. The format is similar to the `printf` format, except that it uses `%i` for index and `%o` for original name of source bump. `%i` mean the index of bump, which starts at one more than the number of existing bumps in the design.
Copy	Copies bumps to the specified location with the same pitch constraint. By default, the target bumps after copy are unassigned and named with the default format `Bump_%i` by the tool. If there are any name collisions, an error is given and the bumps are not copied.
Get selected bump location	
Lower left of bump cell	Gets coordinates of lower-left corner of selected bump cell.
Center of bump cell	Gets coordinates of center of selected bump cell.

Lower left of bump geometry	Gets coordinates of lower-left corner of geometry of selected bump.
Center of bump geometry	Gets coordinates of center of geometry of selected bump.
X Y	Displays *X* and *Y* coordinates as per specified option for selected bump when you click *Get*.
Get	Gets coordinates for the selected bump as per specified option.
Move/Flip/Rotate bump	Opens the Floorplan toolbox, which you can then use to move, flip, or rotate a bump.
View Bump Connection by Selection	Displays flightlines for selected bumps and IO instances in bold.

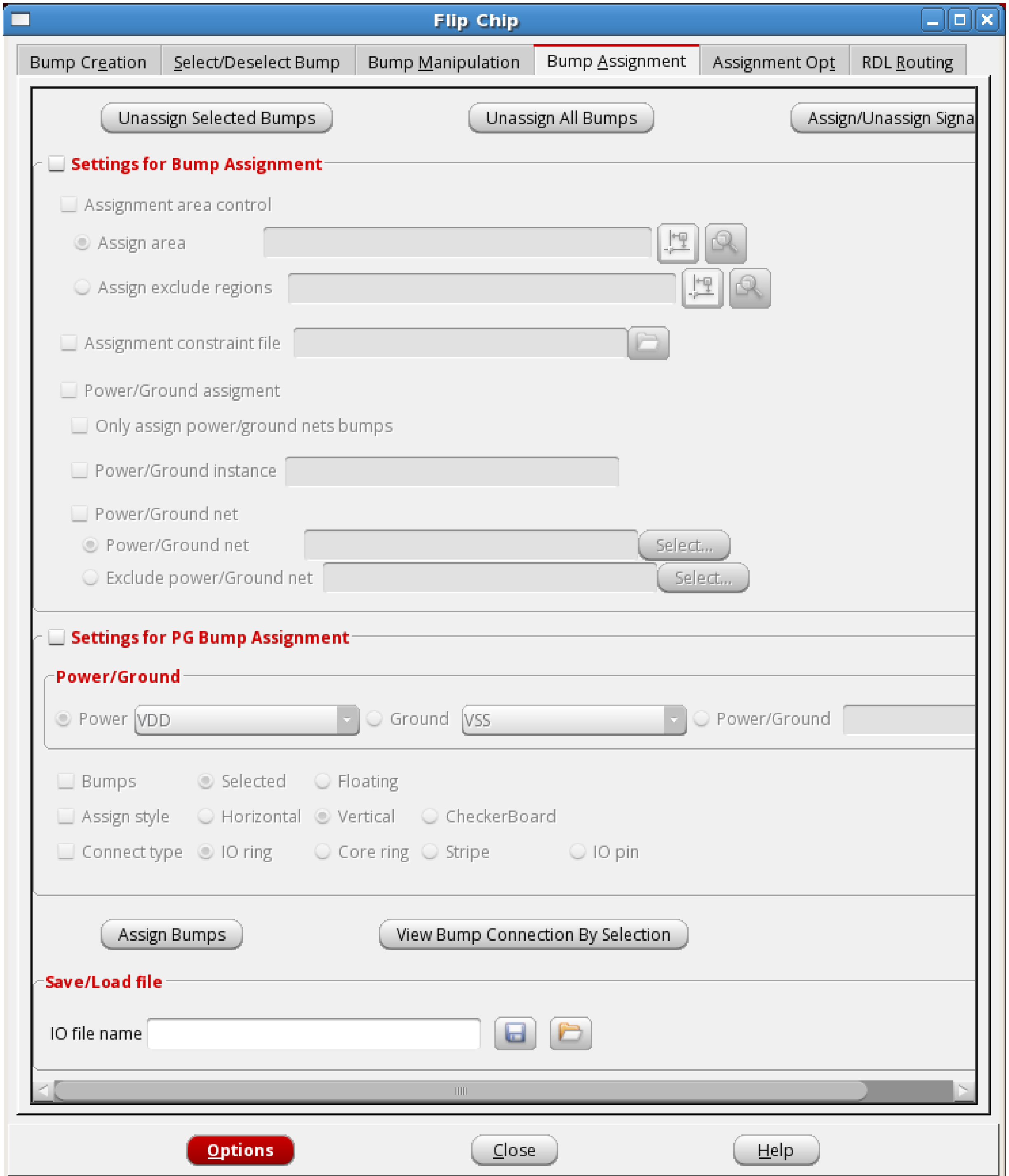
Related Topics

- Flip Chip Methodologies

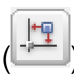
Bump Assignment

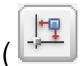
Use the *Bump Assignment* page to assign or unassign bumps.

- To open the *Bump Assignment* page, choose *Tools* - *Flip Chip* and select *Bump Assignment*.



Bump Assignment Fields and Options

Unassign Selected Bumps	Unassigns the bump(s) selected in the design in the main window. Removes the Verilog signal names from the selected bumps, which removes the connection between bumps and I/O pins. The original connection remains in the Verilog and is connected when the bump is reassigned. If the bump is assigned, it will appear in the DEF `SPECIALNETS` section with the signal (net) name.	
Unassign All Bumps	Removes all the connections between bumps and I/O pins and removes the signal assignment of the bumps.	
Settings for Bump Assignment		
Assignment area control	Specifies options for assignment based on area.	
	Assign area	Assigns objects in the specified area. To specify the area, you can: • Enter coordinates in the text box provided. Or • Click the *Draw to specify area* () button to interactively select an area in the design display window. Or • Click the *View area* () button to enter the coordinates of the area currently displayed in the display area. Assignments are made as follows: • If the specified area includes only bumps, the tool assigns the selected bumps to IO cells based on the total shortest distance. • If the specified area includes only IO cells, the tool assigns the selected IO cells to bumps based on the total shortest distance. • If the specified area includes both IO cells and bumps, then the tool assigns the selected IO cells to the selected bumps. If the number of bumps are not enough, the tool issues a warning.

	Assign exclude regions	Excludes bumps in the area specified during assignment. To specify the area to be excluded, you can: • Enter coordinates in the text box provided. Or • Click the *Draw to specify area* () button to interactively select an area in the design display window. Or • Click the *View area* () button to enter the coordinates of the area currently displayed in the display area.
Assignment constraint file	Specifies the path to the file containing bump assignment constraints. At present, the following types of bump assignment constraints are supported: • `SHARE_FIND_PORT` constraint to filter unnecessary ports • `ASSIGN_ANALOG_PG_NETS` constraint to specify which signal nets are analog PG nets • `SHARE_IGNORE_*` constraint to exclude instances or macros for assignment • `ASSIGN_IGNORE_*` constraint to exclude pins or nets for assignment	
Power/Ground assignment	Provides the following options for power/ground assignment.	
	Only assign power/ground nets bumps	Assigns only power/ground nets to bumps. When this option is specified, signals are not assigned to bumps.
	Power/Ground instance	Specifies the names of power/ground instances to which the power bumps are assigned. The instance names should be enclosed in double quotation marks (" ") or braces {}.

	Power/Ground net	Allows you to choose one of the following options: • *Power/Ground net* - Specifies the names of the power/ground nets to which the bumps are assigned. By default, bumps are assigned to all pads whose ports are connected to power/ground nets. Use the *Select* button to open the *Select Filler Power/Ground net* form in which you can select the required nets from the *Power/Ground net list* box. • *Exclude Power/Ground net* - Specifies the names of the power/ground nets that must be excluded from bump assignment. Use the *Select* button to open the *Select Filler Power/Ground net* form in which you can select the required nets from the *Power/Ground net list* box.
Settings for PG Bump Assignment		
Power/Ground	Specifies the net to which bumps are to be assigned. You can choose one of the following options to specify the net names: • *Power* - Select a power net from the drop-down list. • *Ground* - Select a ground net from the drop-down list. • *Power/Ground* - Specify the power/ground net in the text box.	
Bumps	Provides the following options for choosing the bumps to be assigned:	
	Selected	Specifies that the bumps you have selected will be assigned to the power/ground net selected in the *Power/Ground* panel.
	Floating	Specifies that all floating bumps you have selected will be assigned to the power/ground net selected in the *Power/Ground* panel.
Assign style	Specifies the style of bump assignment, when you define multiple nets in the *Power/Ground* panel.	
	Horizontal	Specifies the horizontal style of bump assignment when you define multiple power/ground nets.
	Vertical	Specifies the vertical style of bump assignment when you define multiple power/ground nets.
	Checkerboard	Specifies the checkerboard style of bump assignment when you define multiple power/ground nets.

Connect type	Specifies the bump connect type when assigning power/ground bumps. Connection type can be: • *IO ring* • *Core ring* • *Stripe* • *IO pin*
Assign Bumps	Assigns bumps to power/ground nets as per the options you have specified to connect flip chip I/O pins.
View Bump Connection by Selection	Displays flightlines for selected bumps and IO instances in bold.
IO file name	Specifies the I/O file name. Use the *Save* button to save bumps to the I/O file. Use the *Load* button to load bumps from the I/O file.

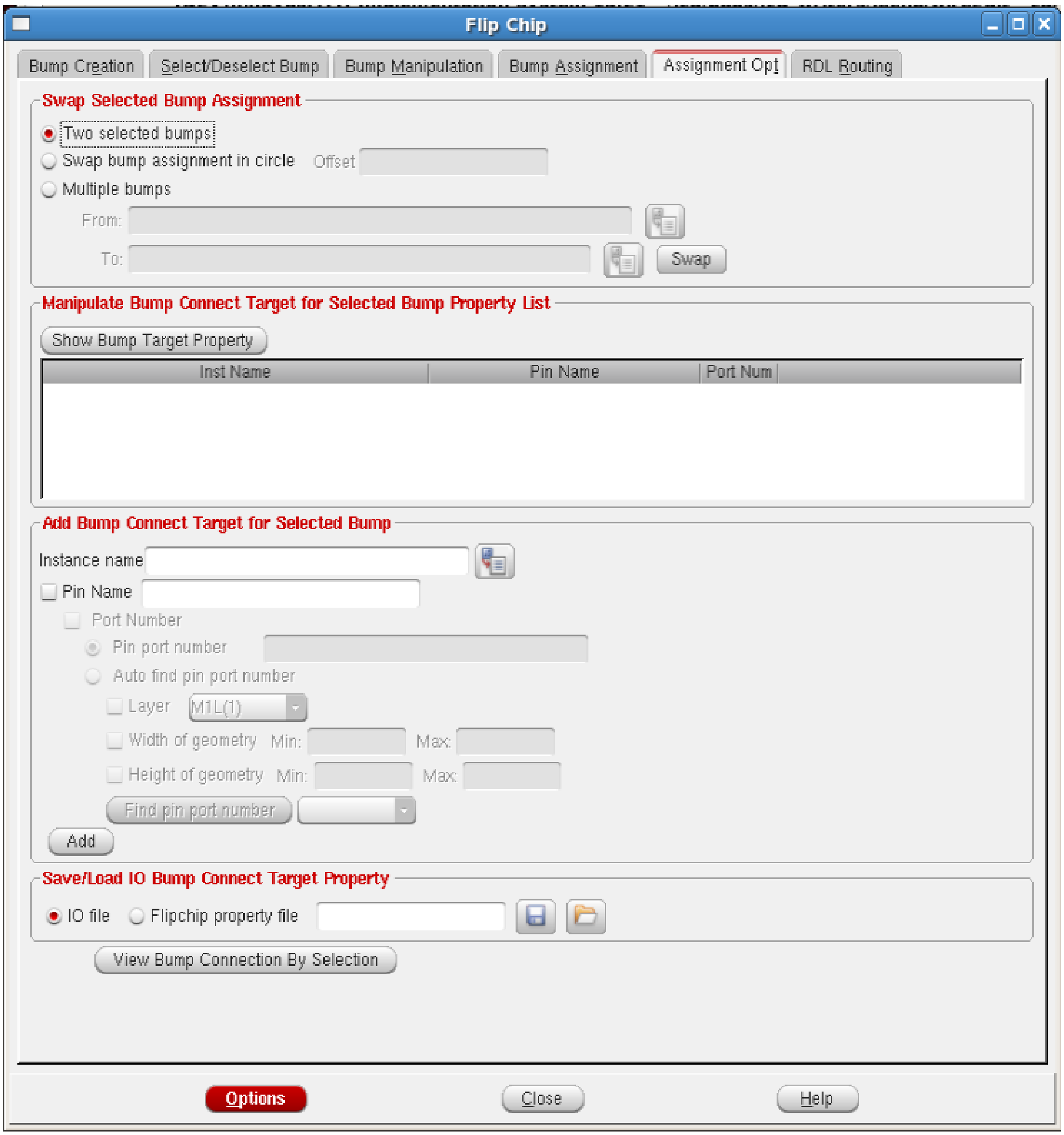
Related Topics

- Flip Chip Methodologies

Assignment Opt

Use the *Assignment Opt* page to swap bump assignments and work with bump connect targets.

- To open the *Assignment Opt* page, choose *Tools - Flip Chip* and select *Assignment Opt*.



Swap Selected Bump Assignment		
Two selected bumps	Specifies that signals have to be swapped between two selected bumps. This is the default option. Either one or both of these bumps must be assigned.	
Swap bump assignment in circle	Specifies that bump assignments have to be swapped in a circle using the specified *Offset* value.	
Multiple bumps	Specifies that signals have to be swapped between multiple bumps, as specified in the *From* and *To* fields.	
	From	Specifies names of bumps from which signal is to be swapped.
	To	Specifies names of bumps to which signal is to be swapped.
Swap	Swaps signals between bumps based on the options you have specified.	
Manipulate Bump Connect Target for Selected Bump Property List		
Show Bump Target Property	Lists the bump connect target properties defined on the selected bumps. Select the bump connect target property that you want to change from the list.	
Delete Bump Connect Target for Selected Bump		
All property	Specifies that all bump connect target properties for selected bumps are to be deleted. If a bump has multiple values for the property, you can use the *Instance property*, *Pin property* and *Port property* options to filter out the matched property value for deletion.	
Instance property	Deletes the bump connect target constraint related to the specified instance.	
Pin property	Deletes the bump connect target constraint related to the specified pin.	
Port property	Deletes the bump connect target constraint related to the specified port.	
Delete	Deletes existing properties on selected bumps.	
Add/Edit Bump Connect Target for Selected Bump		

Instance Name	Specifies the connect target instance. While adding bump connect target constraint, if only *Instance Name* is specified and *Pin Name* is not specified, the tool automatically finds the most suitable geometries in the specified instance.		
Pin Name	Specifies the connect target pin name.		
Port Number	Provides you options for specifying port number.		
	Pin Port Number	Specifies the connect target port number.	
	Auto Find Pin Port Number	Finds a port that is suitable for flip chip routing with its number on an instance based on pin name or nets on the specified layer and/or in a specified area.	
		Layer	Specifies the layer on which the target port is located.
		Width of Geometry	Specifies the minimum and maximum values of the width of the target port's geometry. If you specify only one value, the width is taken as equal to the specified value. Only ports that match the specified width criterion are returned.
		Height of Geometry	Specifies the minimum and maximum values for the height of the target port's geometry. If you specify only one value, the height is taken as equal to the specified value. Only ports that match the specified height criterion are returned.
		Find Pin Port Number	Lists all target ports of the specified instance based on specified options. You can select one of the listed ports for adding bump connect target constraint.
Add	Adds a string property to bumps based on the options you have specified. If any of the specified/selected bump has a property value already, Innovus checks whether the new property value is exactly the same as the existing one. If not, the new property value is concatenated to the existing property string and separated by a space.		
Edit	Modifies the property values on bumps based on the options you have specified.		
Save/Load IO Bump Connect Target Property			
IO file	Specifies the I/O file name. Use the *Save* button to save bump connect target properties to the I/O file. Use the *Load* button to load bump connect target properties from the I/O file.		

Flipchip property file	Specifies the flip chip property file name. Use the *Save* button to save bump connect target properties to the file. Use the *Load* button to load bump connect target properties from the file.
View Bump Connection by Selection	Displays flightlines for selected bumps and IO instances in bold.

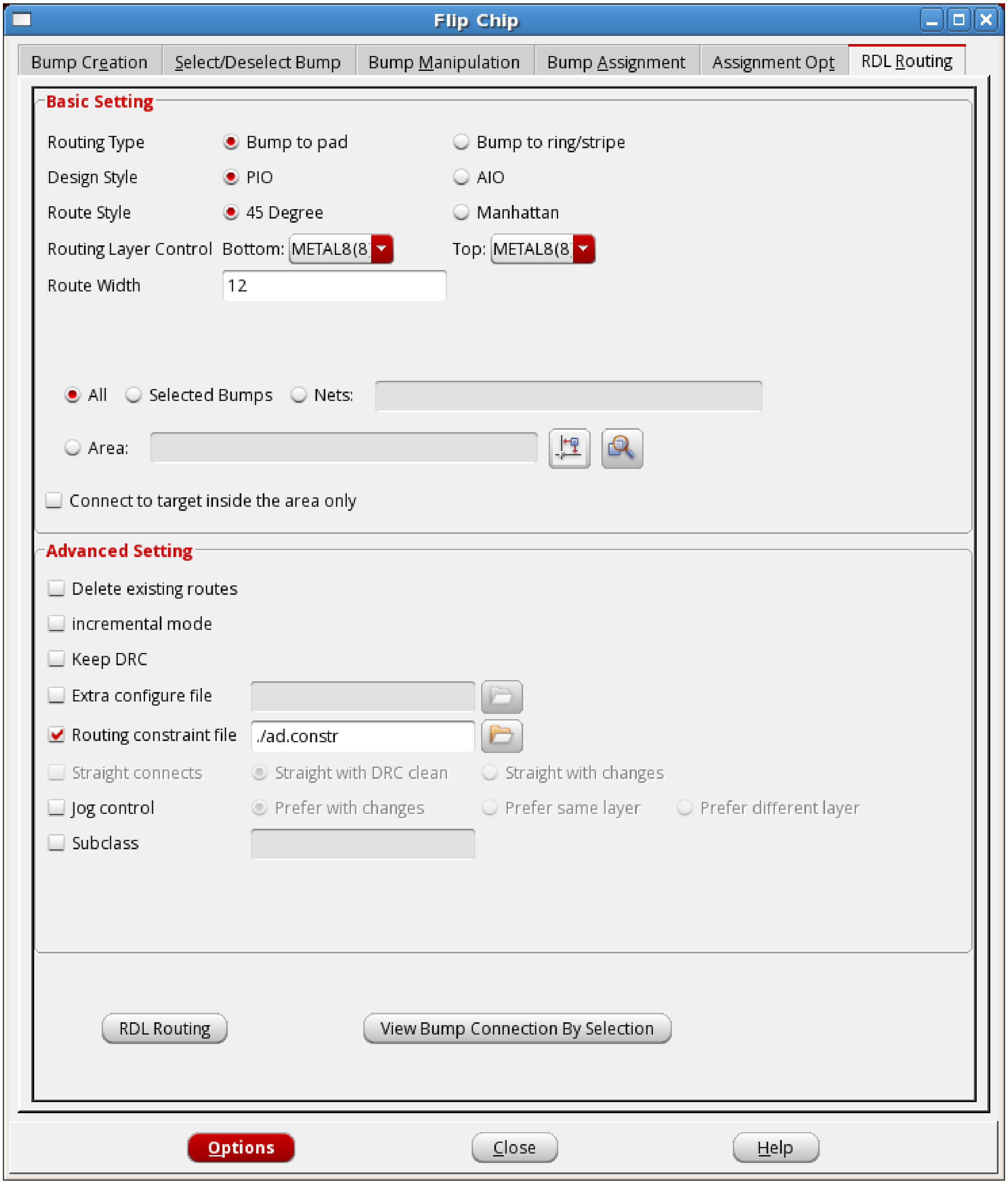
Related Topics

- Flip Chip Methodologies

RDL Routing

Use the *RDL Routing* page to specify options for routing.

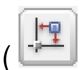
- To open the *RDL Routing* page, choose *Tools* - *Flip Chip* and select *RDL Routing*.



RDL Routing Fields and Options

Basic Setting

Routing Type	Specifies option for connecting power between a bump and I/O pad or a ring/stripe. *Default: Bump to pad*	
	Bump to pad	Connects power from bump to pad.
	Bump to ring/stripe	Connects power from bump to I/O ring or stripe.
Design Style	Specifies the design style. *Default: PIO*	
	PIO	Specifies routing should be in peripheral I/O design style.
	AIO	Specifies routing should be in area I/O design style.
Route Style	Specifies the routing style, which can be *45 Degree* or *Manhattan* . *Default: 45 Degree*	
Routing Layer Control	Specifies the layer range.	
	Bottom	Specifies the bottom-most metal layer that the software can use when routing power bumps. The power bumps on lower layers are not connected. *Default: M8*
	Top	Specifies the top-most metal layer that the software can use when routing power bumps. The power bumps on higher layers are not connected. *Default: M8*
Route Width	Connects wires to bumps using the specified width only, regardless of the size of the bump or the source to which the bump connects. *Default: 12*	
Routing Target	Provides the following options for specifying routing target. *Default: All*	
	All	Specifies that all bumps are to be routed.
	Selected Bumps	Specifies that the selected bumps are to be routed. The selected bumps can be either power bumps or signal bumps.

<table>
<tr><td></td><td>Nets</td><td>Specifies the nets to be connected.
Default: If you select this option but do not specify the net list, the software connects all power and ground nets in the design.</td></tr>
<tr><td></td><td>Area</td><td>If selected, restricts routing to the specified portion of the design. To specify the area, you can:
• Enter coordinates in the text box provided.
Or
• Click the Draw to specify area () button to interactively select an area in the design display window.
Or
• Click the View area () button to enter the coordinates of the area currently displayed in the display area.</td></tr>
<tr><td></td><td>Connect to target inside the area only</td><td>If selected, connections from all sources within the specified area can connect only to power bumps that are also inside that area. If deselected, the software makes connections from all sources within the specified area to power bumps both inside and outside the specified area. This is the default.</td></tr>
<tr><td colspan="3">Advanced Setting</td></tr>
<tr><td>Delete existing routes</td><td colspan="2">Removes existing connections when you click RDL Routing.
Default: Existing connections are left untouched each time you perform RDL routing.
Note: If you select Area, existing routes are always preserved, even if you also select the Delete existing routes check box.</td></tr>
<tr><td>incremental mode</td><td colspan="2">Runs the PIO mode incrementally when pre-routes are already in the design, without deleting or re-routing the pre-routes.</td></tr>
<tr><td>Keep DRC</td><td colspan="2">If specified, the command <code>clearDrc</code> will not run implicitly when you click RDL Routing, therefore retaining the DRC violations.
Default: The <code>clearDrc</code> command runs implicitly when you click RDL Routing, purging all the violation markers.</td></tr>
<tr><td>Extra configure file</td><td colspan="2">Specifies the name of the file that contains extra configuration options.</td></tr>
</table>

Routing constraint file	Specifies the file that contains constraints for flip chip routing.	
Straight connects	Specifies that only straight connections are made between targets, and that jogs are not allowed during routing. This option is only available with *Bump to ring/stripe* routing type. You can also specify one of the following options:	
	Straight with DRC clean	Leaves a route open if a straight connection cannot reach a target without causing a DRC violation. If you do not specify this option, the software makes a straight connection to a target, even if the route creates a DRC violations. This is the default option.
	Straight with changes	Permits the route to change to another layer to avoid DRC violations. If you do not specify this option, the software makes only straight connections on the same layer.
Jog control	Specifies that jogs are allowed during routing to avoid DRC violations. You can also specify one of the following options:	
	Prefer with changes	Specify this option if you prefer the software to make straight connections between targets, and to change layers instead of jog to avoid DRC violations. If you do not specify this option, the route uses both layer changes and jogging to avoid DRC violations. This is the default option.
	Prefer same layer	If the route must jog to avoid a DRC violation, the jog occurs on the same layer whenever possible. This can result in routing in the non-preferred direction.
	Prefer different layer	If the route must jog to avoid a DRC violation, the jog occurs on the layer that is in the preferred routing direction whenever possible.
Subclass	Assigns the specified string as a subclass name to the wires and vias created.	
RDL Routing	Completes RDL routing based on the options you have specified.	
View Bump Connection By Selection	Displays flightlines for selected bumps and IO instances in bold.	

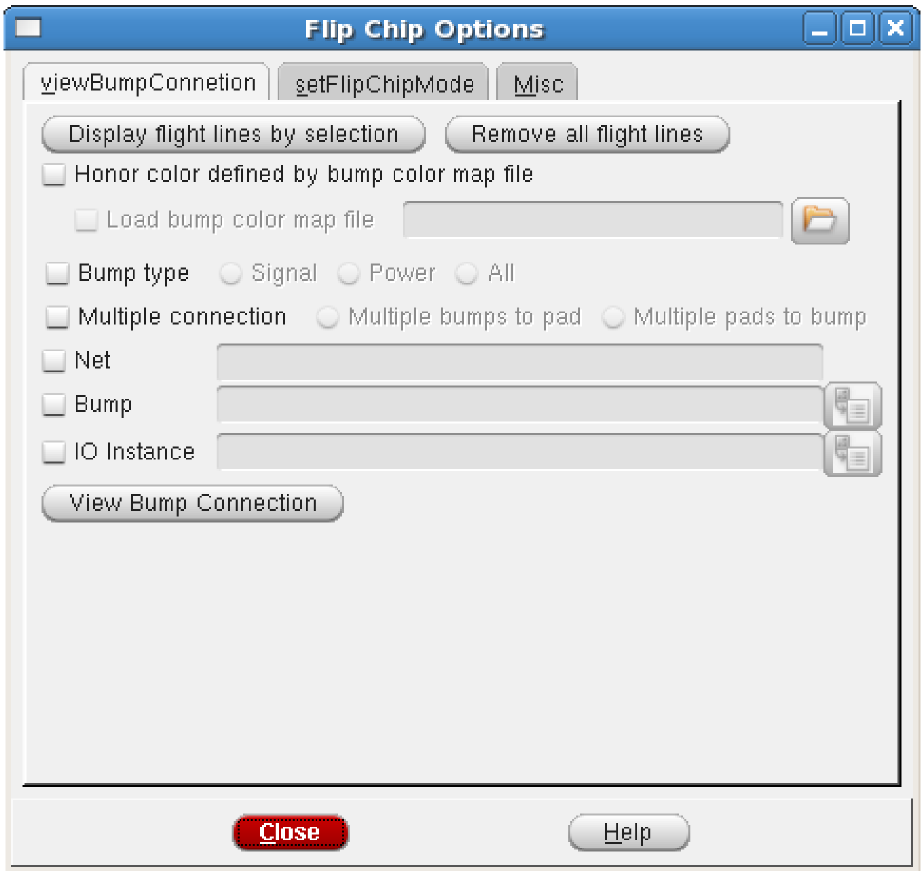
Related Topics

- Flip Chip Methodologies

viewBumpConnection

Use the *viewBumpConnection* page in the Flip Chip Options form to specify options for viewing flip chip flight lines.

- To open the *viewBumpConnection* page, choose *Tools - Flip Chip* and click the *Options* button.



viewBumpConnection Fields and Options

Display flight lines by selection	Displays flight lines for selected bumps and IO instances in bold.	
Remove all flight lines	Removes the bump connections.	
Honor color defined by bump color map file	Colors flight lines according to the settings defined in the bump color map file, which can be loaded with the `ciopLoadBumpColorMapFile` command.	
	Load bump color map file	Loads the bump color map file.
Bump Type	Specifies the type of bumps for which flight lines are to be displayed.	
	Signal	Specifies that flight lines are to be displayed for signal bumps only.
	Power	Specifies that flight lines are to be displayed for power bumps only.
	All	Specifies that all flip chip flight lines are to be displayed.
Multiple Connection	Specifies whether multiple connections are allowed.	
	Multiple bumps to pad	Connects multiple bumps to one pad.
	Multiple pads to bump	Connects multiple pads to one bump.
Net	Specifies nets for which flightlines are to be displayed.	
Bump	Specifies bumps for which flightlines are to be displayed. Click the *Get Selected Bump* button to enter list of selected bumps automatically.	
IO inst	Specifies IO instances or blocks for which flightlines are to be displayed. Click the *Get Selected IO Inst* button to enter list of selected instances automatically.	
View Bump Connection	Displays flip chip flightlines based on the options you have specified.	

Related Text Commands

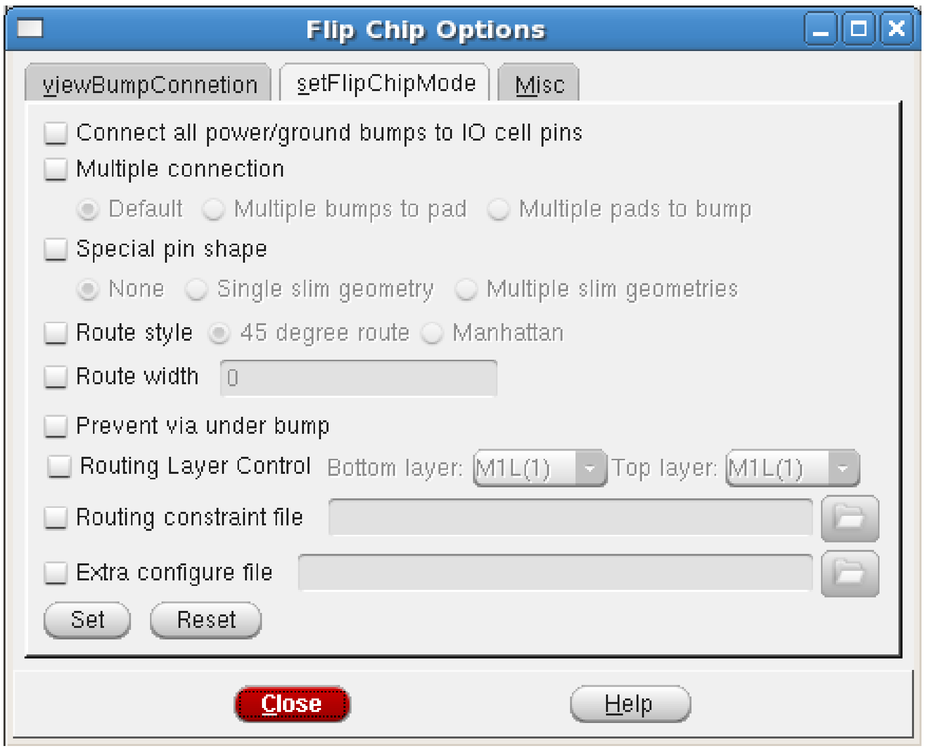
- `ciopLoadBumpColorMapFile`

- `viewBumpConnection`
- Flip Chip Methodologies

setFlipChipMode

Use the *setFlipChipMode* page in the Flip Chip Options form to specify options for viewing flip chip flight lines.

- To open the *setFlipChipMode* page, choose *Tools - Flip Chip*, click the *Options* button, and then select *setFlipChipMode*.



setFlipChipMode Fields and Options

<table>
<tr><td>Connect all power/ground bumps to IO cell pins</td><td colspan="2">Connects all power bumps to the I/O cell pin. It does not connect to a power or ground stripe or ring.

When used with the <code>fcroute -type signal</code> parameter, you can connect power bumps to I/O power pads. To make this type of connection, you need the following information:

• The Verilog netlist must contain the I/O power pad, for example:
VDDCELL VDD_INST (.PAD());

• The LEF macro pin must contain the USE POWER statement, for example:
MACRO VDDCELL
PIN PAD
USE POWER;

To improve the quality of routing in situations where there may be many power bumps in the design, you can pair power bumps to power cells by using this parameter in conjunction with the Routing constraint file option.</td></tr>
<tr><td>Multiple connection</td><td colspan="2">Specifies routing connections between multiple pads and bumps. Choose one of the following options:</td></tr>
<tr><td></td><td>Default</td><td>Enables routing from one bump to one pad in parallel. This means there is no multiple connection.</td></tr>
<tr><td></td><td>Multiple bumps to pad</td><td>Enables routing from multiple bumps to one pad in parallel. This parameter is supported by both, <code>fcroute</code> AIO and PIO routing styles.</td></tr>
<tr><td></td><td>Multiple pads to bump</td><td>Enables routing from multiple pads to one bump in parallel. This parameter is supported by both, <code>fcroute</code> AIO and PIO routing styles.</td></tr>
<tr><td>Special pin shape</td><td colspan="2">Specifies whether special pin shapes are supported. Choose one of the following options:</td></tr>
<tr><td></td><td>None</td><td>Does not support special pin shapes. This is the default option.</td></tr>
<tr><td></td><td>Single slim geometry</td><td>Supports slim pin shape with MINPINSIZE -2. With this option, <code>fcroute</code> can control connection location to avoid the dropped via out of the pin geometry.</td></tr>
<tr><td></td><td>Multiple slim geometries</td><td>Supports slot pin shape with MINPINSIZE -1. With this option, <code>fcroute</code> can drop vias on all slim geometries defined under one port.</td></tr>
</table>

Route style	Determines the type of routing, which can be either: • *45 degree route* • *Manhattan* *Default: 45 degree route*	
Route width	Connects wires to bumps using the specified route width not wider than the I/O pad pin. *Default: 12*	
Prevent via under bump	Specifies that vias are generated next to the bump instead of directly on the bump. If you do not specify this option, the vias generated connect directly to the bump.	
Routing Layer Control	Specifies the layer range.	
	Bottom Layer	Specifies the bottom-most metal layer that the software can use when routing bumps. The bumps on lower layers are not connected. *Default: M8*
	Top Layer	Specifies the top-most metal layer that the software can use when routing bumps. The bumps on higher layers are not connected. *Default: M8*
Routing constraint file	Specifies the file that contains constraints for flip chip routing.	
Extra configure file	Specifies the extra configuration file for flip chip routing.	

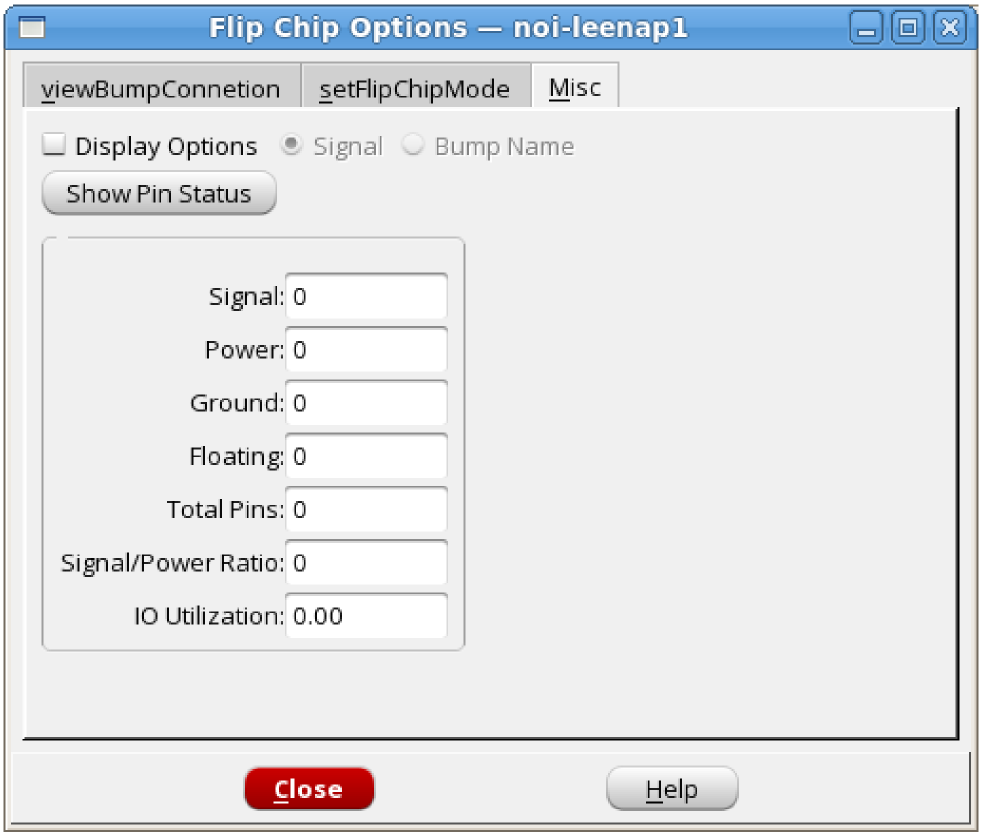
Related Text Commands

- `fcroute`
- setFlipChipMode
- Flip Chip Methodologies

Misc

Use the *Misc* page in the Flip Chip Options form to specify options for viewing flip chip flight lines.

- To open the *Misc* page, choose *Tools - Flip Chip*, click the *Options* button, and then select *Misc*.



Display Options	Provides options to view the bump information contained in a tile.	
	Signal	Displays signal names of bumps.
	Bump Name	Displays names of bumps.
Show Pin Status	Displays statistical information about signals, tiles, and bumps.	
	Signal	Shows the total number of signals.
	Power	Shows the total number of power signals.

	Ground	Shows the total number of ground signals.
	Floating	Shows the total number of floating signals.
	Total Pins	Shows the total number of pins.
	Signal/Power Ratio	Shows the total number of signals divided by the total number of power and ground signals.
	IO Utilization	Shows the utilization number (I/O driver area divided by the I/O row area).

TSV

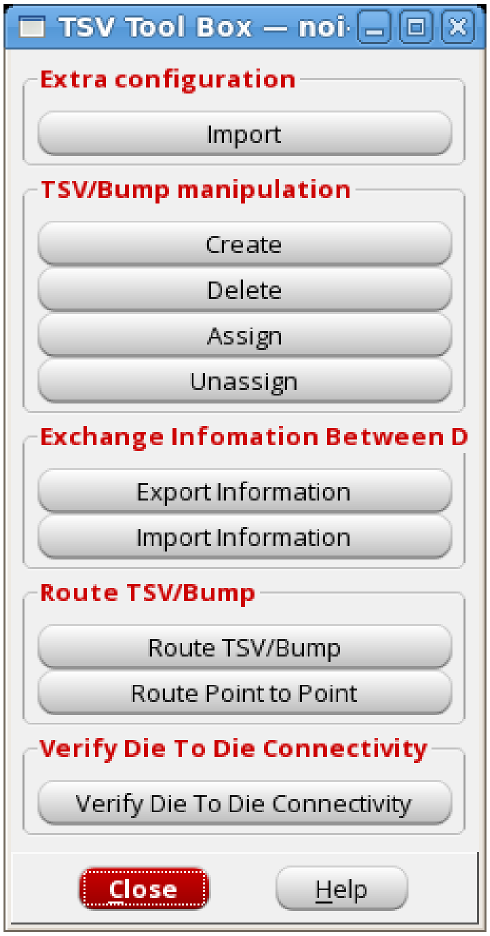
The *TSV* submenu provides access to the following features:

- TSV Tool Box
- Load Stacked Die Config
- Stacked Config Editor
- Create TSV/Bump
- Delete TSV
- Assign TSV/Bump
- Unassign TSV
- Export Die Information
- Import Adjacent Dies Information

TSV Tool Box

You can use the *TSV Tool Box* to perform various TSV design flow tasks. The *TSV Tool Box* contains the forms used in the TSV design flow, including TSV/Bump manipulation, data exchange, TSV/Bump routing, and design verification.

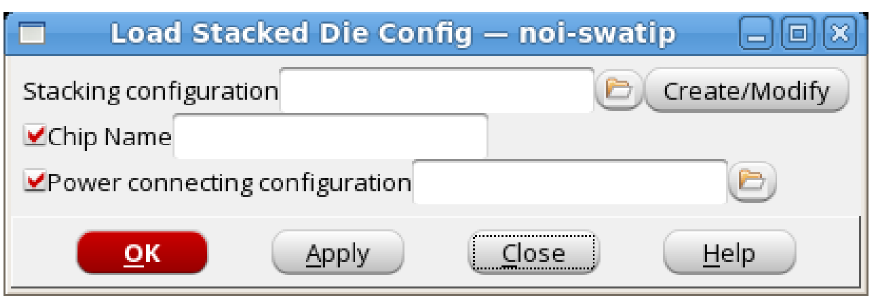
- Choose *Tools - TSV*.



Load Stacked Die Config

Use the *Load Stacked Die Config* form to specify or create the extra configuration for 3D design, including stacking configuration and power connecting configuration.

- Choose *Tools - TSV - Import*.



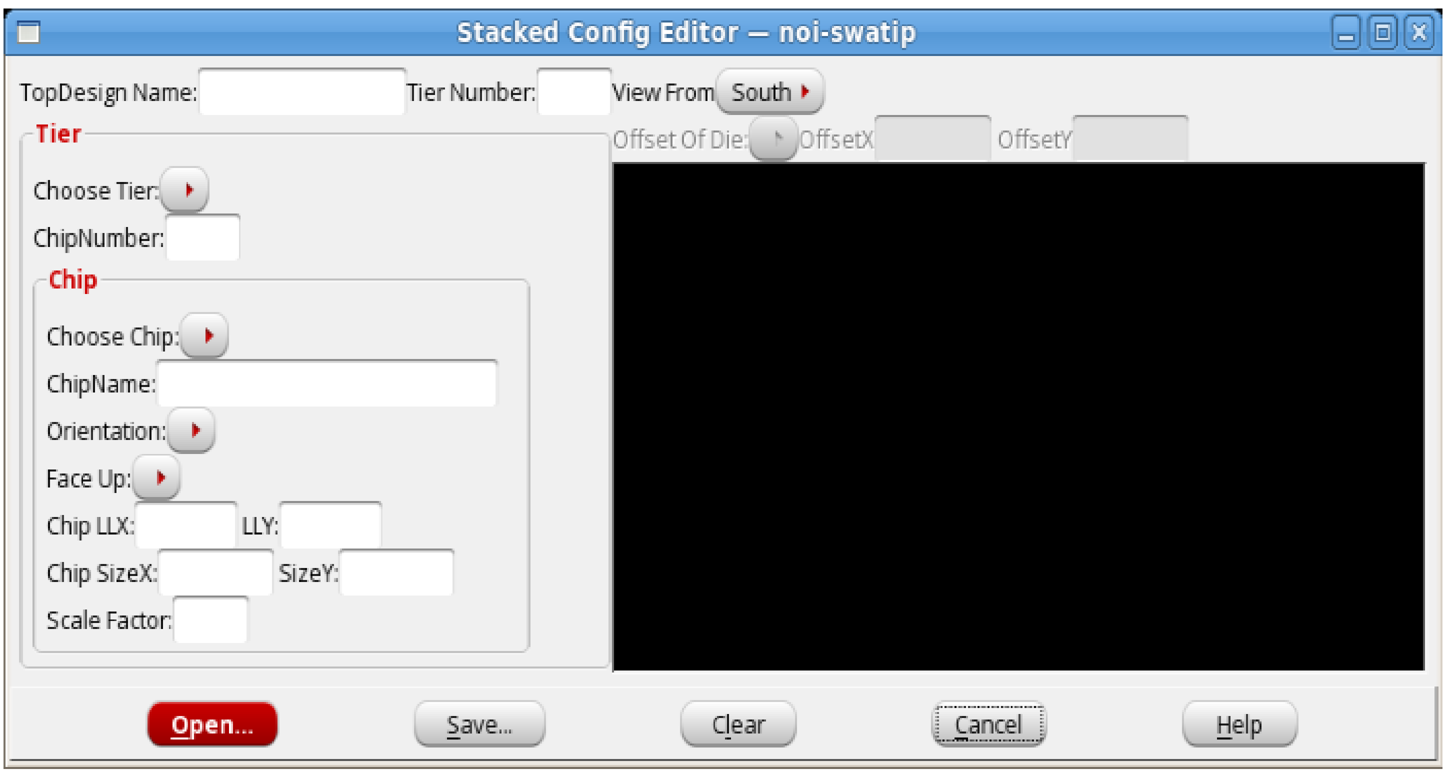
Load Stacked Die Config - Fields and Options

Stacking Configuration	Specifies the Stacking Configuration file.
Create/Modify	Opens the Stacked Config Editor form.
Chip Name	Specifies the chip name of the current design.
Power Connecting Configuration	
	Specifies Power Connecting Configuration file.

Stacked Config Editor

Use the Stacked Config Editor form to create or edit the stacking configuration files.

- Choose *Tools - TSV - Import - Create/Modify*.



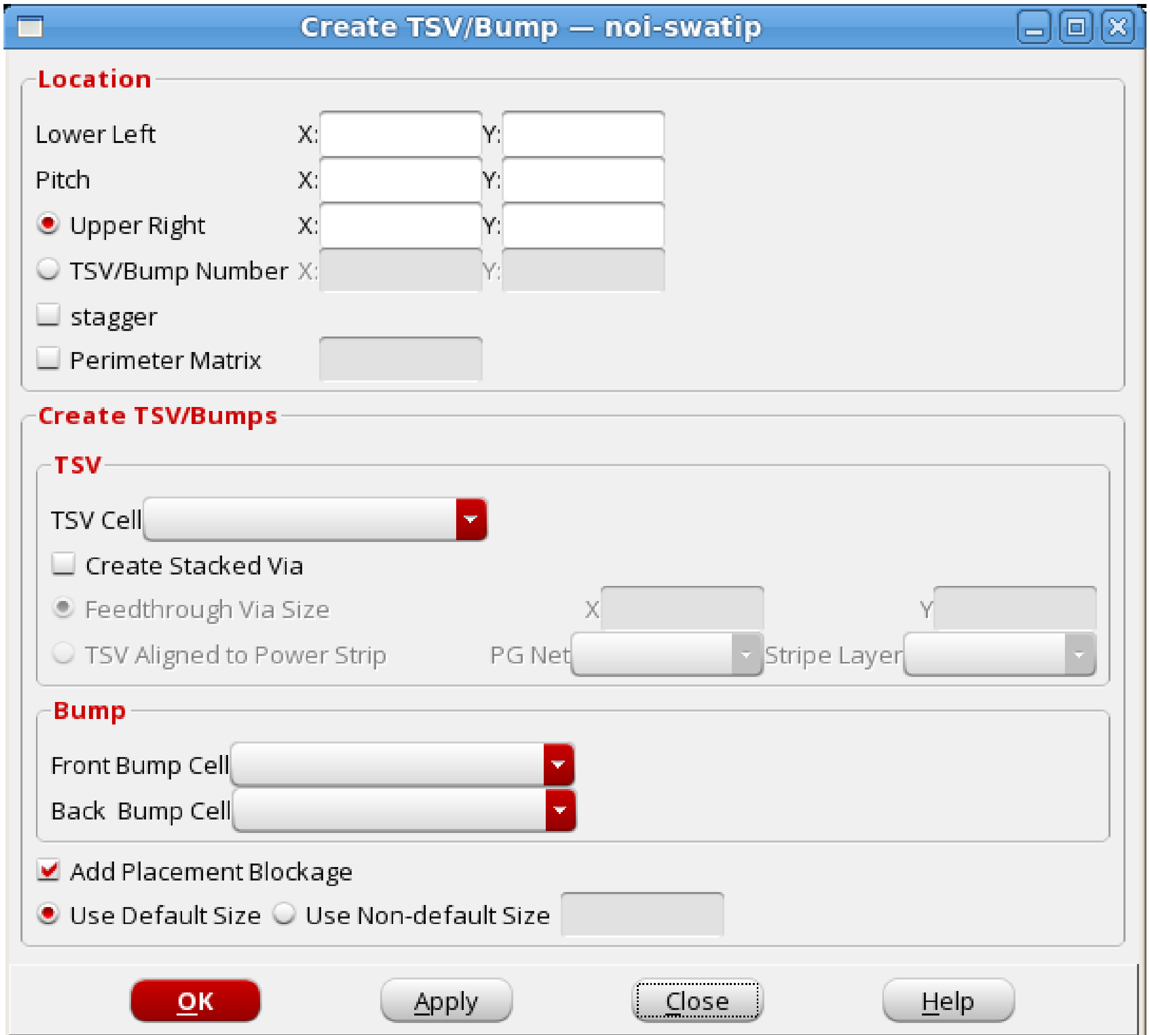
Stacked Config Editor - Fields and Options

TopDesign Name	Specifies the name of the wrapper cells.
Tier Number	Specifies the number of tiers in the 3D stacked die system.
View From	Specifies the view angle or view point. There are 5 view angles: south, north, west, east, and top. Except for the different view angle, user is able to select the view point, that is, fix one die and view the other dies from the fixed die.
Offset Of Die	Choose one die to observe its offset related to the fixed die specified by the *View From* field.
OffsetX	The offset in X direction.
OffsetY	The offset in Y direction.
Choose Tier	Specifies the tier to be edited.
ChipNumber	Specifies the number of chips on the active tier.
Choose Chip	Specifies the die to be edited.
ChipName	Specifies the name of the active chip. The chip name should be consistent with the name in the top level netlist. The top level netlist describes the interconnection between chips.
Orientation	Specifies the orientation of the active die.
Face Up	If the die faces down, then the face up value should be selected as no, otherwise the value should be yes.
Chip LLX	Specifies the offset in X direction of the active die related to the package.
LLY	Specifies the offset in Y direction of the active die related to the package.
Chip SizeX	Specifies the size in X direction of the active die. The sizeX is measured on the x direction when the die is not rotated.
SizeY	Specifies the size in Y direction of the active die. The sizeY is measured on the y direction when the die is not rotated.
Scale Factor	Specifies the scale factor for the half node technology. The real dimension equals the dimension should in Innovus multiple the scale factor.

Create TSV/Bump

Use the *Create TSV/Bump* form to add TSVs, frontside bumps, and backside bumps under specified conditions.

- Choose *Tools - TSV - Create*.



Create TSV/Bump - Fields and Options

Lower Left	Specifies the lower left coordinate of the box in which TSV/Bumps will be created.
Pitch	Specifies the distance between TSV/Bump centers, in microns, in the x and y direction.

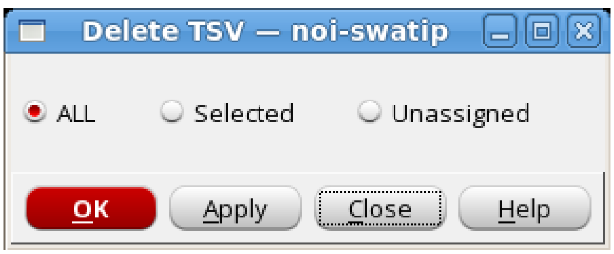
Upper Right	Specifies the upper right coordinate of the box in which TSV/Bumps will be created.
TSV/Bump Number	Specifies the count of the TSV/bump in horizontal and vertical direction.
Stagger	Staggers (offsets) the TSV /bump array. For Example: * * * * * * * * * * * *
Perimeter Matrix	Creates TSV/Bump along rings on the perimeter based on user's definition.
TSV Cell	Specifies the name for TSV via defined in the LEF file. If this option is not specified, no TSV will be created.
Create Stacked Via	If selected, two types of stacked via may be created. The first type is the stacked via between the TSV and top metal. Together with the TSV, the stacked via forms a feedthrough. The second type is the stacked via between the TSV and the power stripe, which connects the TSV and power stripe.
Feedthrough Via Size	Specifies the dimension for the stacked via for feedthrough.
TSV Aligned to Power Strip	
	If selected, the stacked via between the TSV and the power stripe, which connects the TSV and power stripe will be created. User also needs to specify the power/ground net and the layer of the power stripe if this radio button is selected.
PG Net	Specifies the power/ground net of the stripe beneath which the TSVs will be dropped.
Stripe Layer	Specifies the layer of the stripe beneath which the TSVs will be dropped.
Front Bump Cell	Specifies the name for the frontside bump cell. If this option is not specified, no frontside bump will be created.
Back Bump Cell	Specifies the name for the backside bump cell. If this option is not specified, no backside bump will be created.
Add Placement Blockage	

	The placement blockage overlapped with TSV cut will be added if it is selected. This check box is selected by default.
Use Default Size	If it is selected, the placement blockage with default size will be created. The default size = TSV cut size + spacing * 2, the value of spacing is defined with "SPACING num LAYER OVERLAP ;" in TSV session, which means that TSV should keep a certain spacing from the active cells.
Use Non-default Size	Specifies the non-default spacing rather than the one defined in lef. The placement blockage size equals TSV size plus spacing * 2.

Delete TSV

Use the *Delete TSV* form to delete the specified TSVs. If the TSV belongs to a feedthrough, the whole feedthrough will be deleted.

- Choose *Tools - TSV - Delete*.



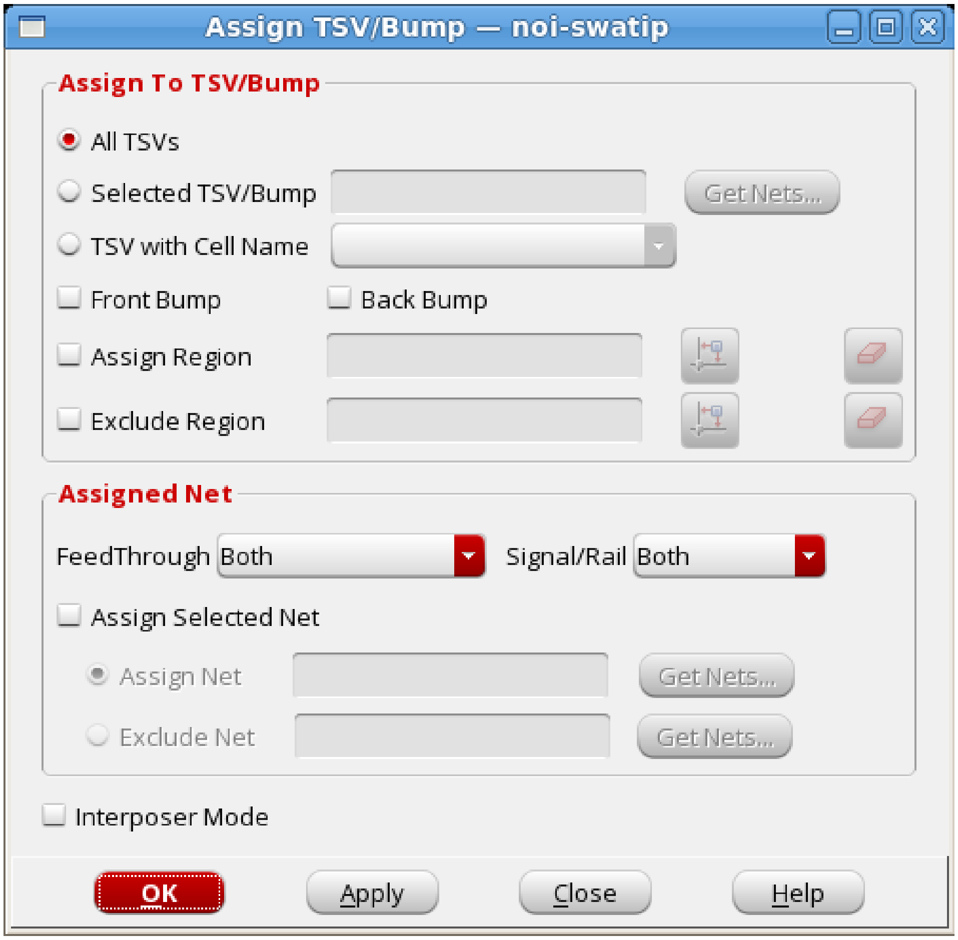
Delete TSV - Fields and Options

All	Select this radio button to delete all the TSVs.
Selected	Select this radio button to delete the selected TSVs.
Unassigned	Select this radio button to delete the unassigned TSVs.

Assign TSV/Bump

Use the *Assign TSV/Bump* form to assign the nets to TSVs, and/or frontside and backside bumps, and/or feedthroughs. Use this form after the instance connected with the IO pins are placed.

- Choose *Tools - TSV - Assign*.



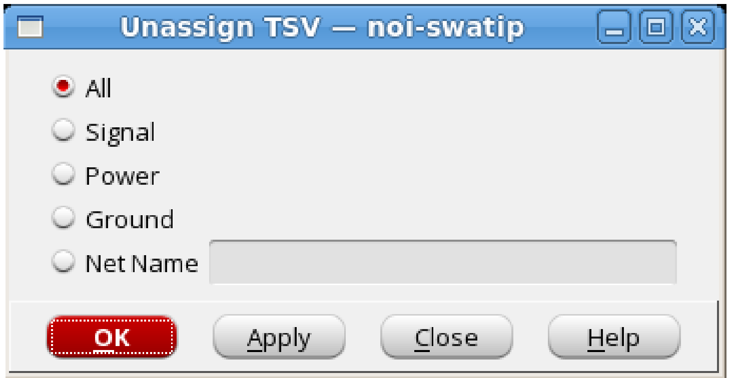
Assign TSV/Bump - Fields and Options

All TSVs	Specify that all the TSVs are the candidates to be assigned with the net automatically.
Selected TSV	Use this option to assign the specified net to the selected TSVs.
TSV with Cell Name	Specify that only TSV with the selected Via Cell name will be assigned.
Front Bump	Specify that the frontside bumps will be assigned with the IO pins automatically.
Back Bump	Specify that the backside bumps will be assigned with the IO pins automatically.
Assign Region	Assign TSV/Bump within the region only.
Exclude Region	Do not assign TSV/Bumps within the specified region. **Note:** The user can select *Assign Region* and *Exclude Region* at the same time, but these two options are exclusive to *Selected TSV/Bump*.
FeedThrough	Choose the net type to be assigned, feedthrough net, normal net or both.
Signal/Rail	Specify net type to be assigned, signal net, power/ground net or both.
Assign Net	Assign the specified nets to TSV/Bumps.
Exclude Net	Do not assign the specified nets to TSV/Bumps. **Note:** The two options *Assign Net* and *Exclude Net* are exclusive to each other, and they are also exclusive to *Selected TSV/Bump*.
Interposer Mode	Declare that the assignment is done in silicon interposer which does not have any instance.

Unassign TSV

Choose *Unassign TSV* form to unassign the specified TSV.

Choose *Tools - TSV - Unassign*.



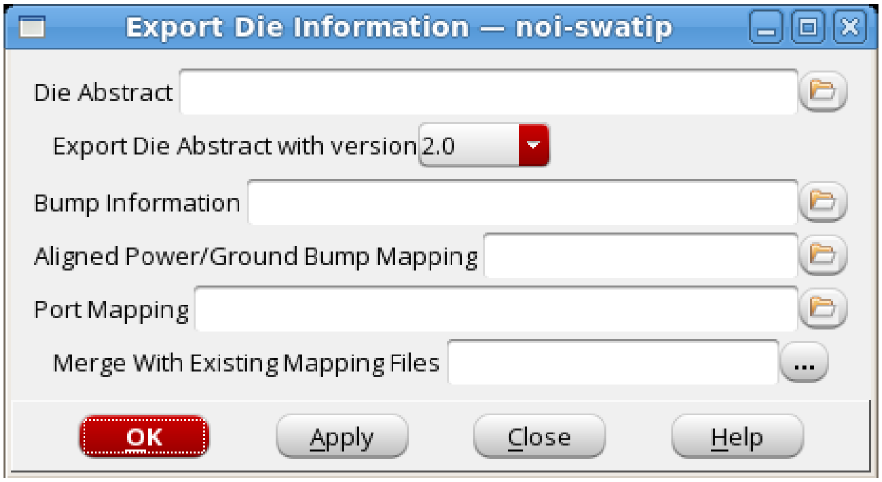
Unassign TSV - Fields and Options

All	Unassigns all nets from TSVs.
Signal	Unassigns the signal net from TSVs.
Power	Unassigns the power net from TSVs.
Ground	Unassigns the ground net from TSVs.
Net Name	Unassigns the specified net from TSVs.

Export Die Information

Choose the *Export Die Information* form to export the information of current die and the interface between the current die and adjacent die.

- Choose *Tools - TSV - Export Information*.



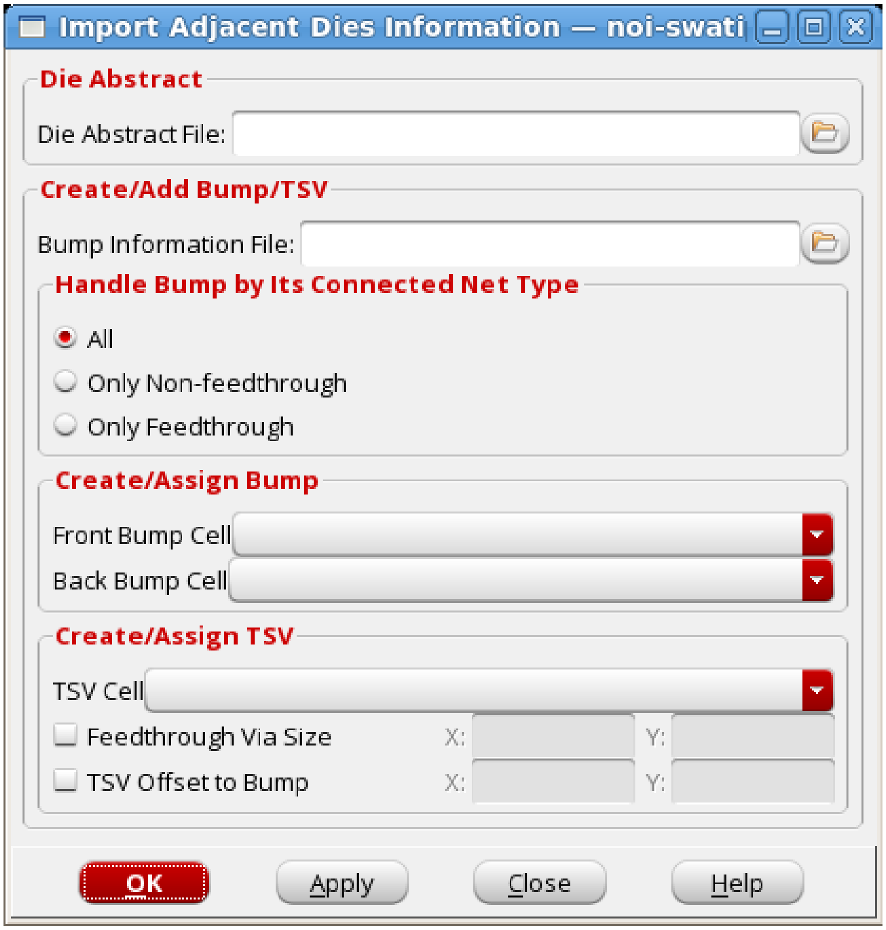
Export Die Information - Fields and Options

Die Abstract	Writes the abstract of current die to a file.
Export Die Abstract with Version	
	The default version is 2.0. Comparing with 1.0, more contents are included in 1.0.
Bump Information	Writes the bump (including frontside bump and backside bump) information to a file.
Aligned Power/Ground Bump Mapping	
	Writes the bump mapping file for Voltage Storm use. Use this function after the `readBumpLocation` command.
Port Mapping	Writes the micro bump mapping file for QRC, voltage storm and Pegasus/PVS use. Use this command after the `readBumpLocation` command.
Merge with Existing Mapping Files	
	If there are more than two dies in the design, the port mapping file may be exported more than one time. This function should be called at the time of last export to merge the previously generated files.

Import Adjacent Dies Information

Choose the *Import Adjacent Dies Information* form to import the adjacent die information.

- Choose *Tools - TSV - Import Information*.



Import Adjacent Dies Information - Fields and Options

Die Abstract File	Specifies the die abstract file of the adjacent die.
Bump Information File	Specifies the die abstract file of the adjacent die.
All	Selects this radio button to import the bump from the adjacent die with all the types.

Only Non-feedthrough	Imports the bump from the adjacent die with only normal net.
Only Feedthrough	Selects this radio button to import the bump from the adjacent die with only feedthrough net. The reason to provide the flexibility to handle feedthrough and normal net separately is that user may want to create the TSV + stacked via for feedthrough net in additional, which is not necessary and reasonable for normal net.
Front Bump Cell	Creates or assigns the front side bump at location aligned to the bumps on the adjacent die.
Back Bump Cell	Creates or assigns the back side bump at location aligned to the bumps on the adjacent die.
TSV Cell	Creates or assigns the TSV at location aligned (with offset) to the bumps on the adjacent die.
Feedthrough Via Size	Specifies the size for the stacked via of feedthrough.
TSV Offset to Bump	Specifies the offset from the TSV to the corresponding bump.

Flip Chip Route

Use the Flip Chip Route form to create special route wires to power bumps and create regular route wires to signal bumps. To open the *Flip Chip Route* form, choose *Tools* - *TSV* and select *Route TSV/Bump*.

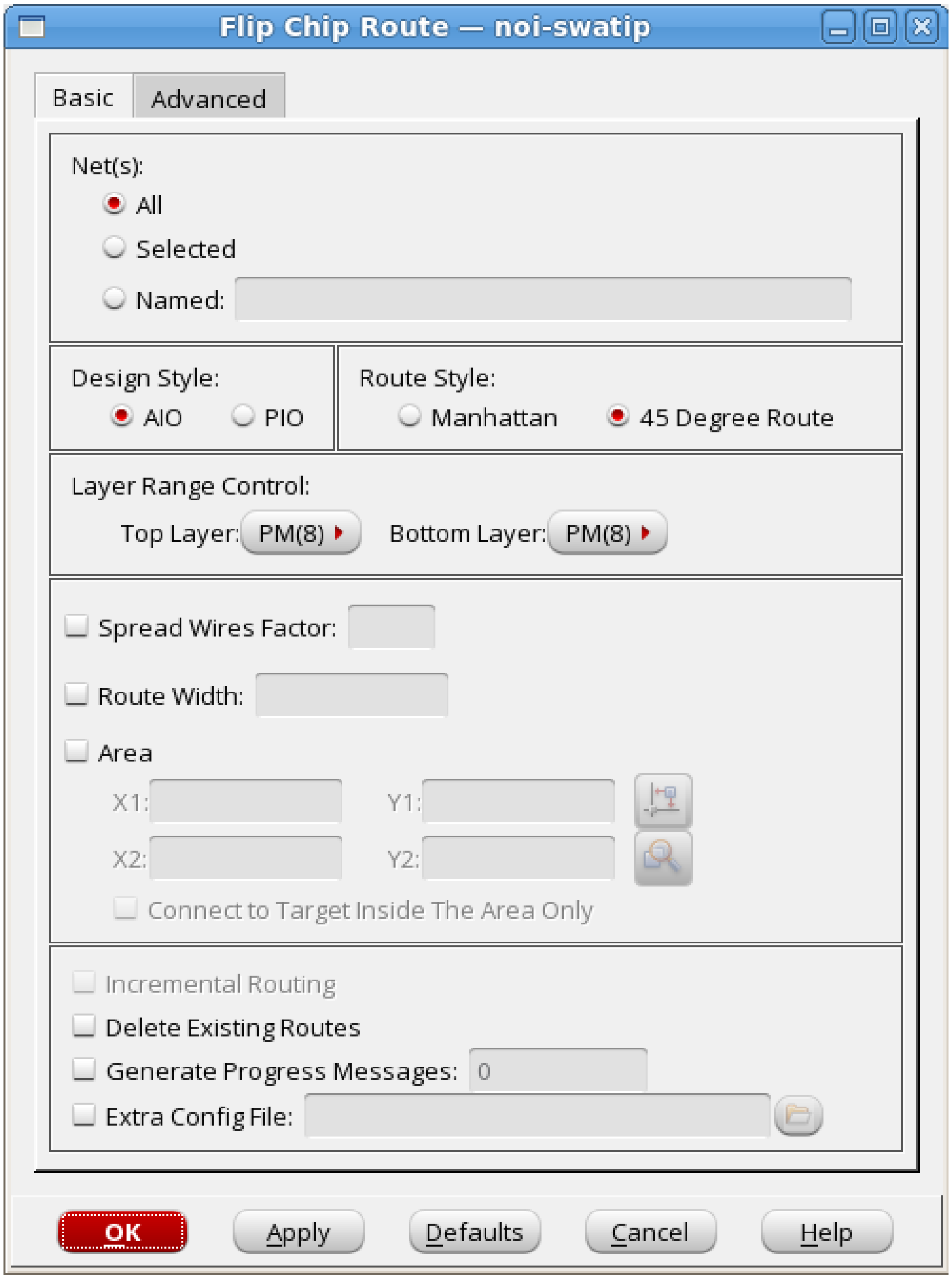
The Flip Chip Route form contains the following two pages:

- Flip Chip Route - Basic
- FlipChipRouteAdvanced

Flip Chip Route - Basic

Use the *Basic* page of the *Flip Chip Route* form to create special route wires to power bumps.

- To open the *Basic* page of the *Flip Chip Route* form, choose *Tools* - *TSV* and select *Route TSV/Bump*. Click the *Basic* tab.



Flip Chip Route - Basic Fields and Options

Net(s)	Specifies which nets are to be connected to the bumps:	
	All	Connects to bumps belonging to all nets in the design. This is the default.

	Selected	Connects to bumps belonging to the nets that you select interactively in the design display area.
	Named	Connects to bumps belonging to the nets that you specify in the text entry field.
Design Style	Specifies the design style. Select between area I/O and peripheral I/O design styles. You can run fcroute in the PIO mode when pre-routes are already in the design, without deleting or re-routing the pre-routes.	
Route Style	Specifies the routing style. Select either *Manhattan* or *45 Degree Route* styles. *Default* : *45 Degree Route*	
Layer Range Control		
	Top Layer	The top-most metal layer that the software can use when routing power bumps. Power bumps on higher layers are not connected.
	Bottom Layer	The bottom-most metal layer that the software can use when routing power bumps. Power bumps on lower layers are not connected.
	Note: If the top and the bottom layer is the same, routing occurs in PIO mode. If the top and bottom layers are different, then routing occurs in the AIO mode.	
Spread Wires Factor	Specifies automatic spreading of wires during bump routing in order to prevent any SI violations. The value is applied as a multiple of the minimum spacing that is required.	
Route Width		
	If selected, wires that connect to the bumps always use the width that you specify in the text entry field, regardless of the size of the bump or the source to which the bump connects. If deselected, the width of the route is the smaller of either the bump or the pin that is connected to the bump. This is the default.	

Area	If selected, restricts routing to the specified portion of the design. To specify the area, you can: • ◦ Enter coordinates in the *X1* , *X2* , *Y1* , and *Y2* fields. Or ◦ Click the *Draw* button to interactively select an area in the design display window. Or ◦ Click the *View Area* button to enter the coordinates of the area currently displayed in the display area. If deselected, the software performs routing for the entire design area. This is the default. **Note:** Selecting the *Area* option always preserves existing connections. If you select *Area* , the *Delete Existing Routes* option is disabled.
Connect To Target Inside The Area Only	
	If selected, connections from all sources within the specified area can connect only to power bumps that are also inside that area. If deselected, the software makes connections from all sources within the specified area to power bumps both inside and outside the specified area. This is the default. **Note:** This option is only available if you also select the *Area* option.
Incremental Routing	Runs the PIO mode incrementally when pre-routes are already in the design, without deleting or re-routing the preroutes. **Note:** This option is disabled if you select the *AIO* option.
Delete Existing Routes	
	If selected, removes existing connections when you click *Apply* or *OK* . If deselected, existing connections are left untouched each time you use the Route Flip Chip Power form. This is the default. **Note:** This option is disabled if you select the *Area* option.
Generate Progress Messages	
	If selected, you can see all messages displayed while power routing takes place. Enter a value to specify the interval at which progress messages are generated. If you specify 1, the software generates every progress message; if you specify 2, the software generates every other progress message, and so on. If you do not select this option, or if you specify a value of 0, routing messages do not display in the Innovus console. This is the default.

Extra Config File	
	The name of the file that contains extra configuration options. **⚠ *You should only use the extra configuration file if you are familiar with its use.*** The following variables can be used in the extra configuration file: • srouteMaxViaArraySize *percent* The default is 100. • srouteReduceLayerChanges *integer* The default is 0. • srouteStraightConnections [straight routing style (layer change, DRC clean)] • srouteTimeLimit *seconds* The default is 100. • srouteTrivialRouteOnly {true | false} The default is false.

Related Text Commands

For information on the following command, see the Flip Chip Commands in the *Text Command Reference*
.

- `fcroute`

Related Topics

For information on the flip chip AIO and PIO flow, see Flip Chip Methodologies in the *Innovus User Guide* .

Flip Chip Route - Advanced

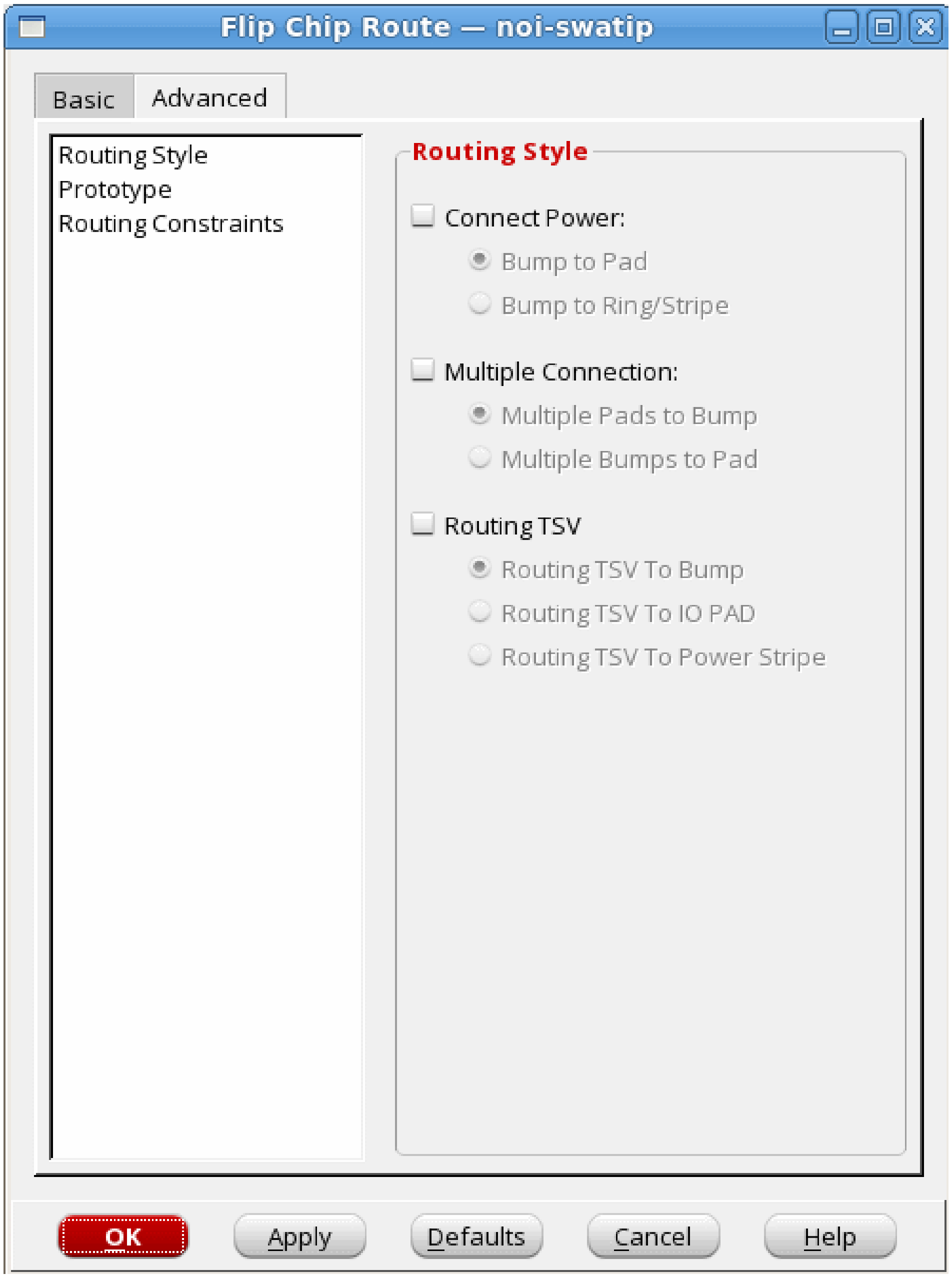
Use the *Advanced* page of the Flip Chip Route form to create regular route wires to signal bumps. The Flip Chip Route form contains the following pages:

Flip Chip Route - Advanced - Routing Style

Use the *Advanced - Routing Style* page of the *Flip Chip Route* form to specify options for power connections.

Note: By default, the `fcroute` engine uses the 45 degree routing style. However, you can specify the manhattan routing style using the `fcroute` -routeStyle manhattan command and option.

To open the *Advanced - Routing Style* page of the *Flip Chip Route* form, choose *Tools* - *TSV* and select *Route TSV/Bump* . Click the *Advanced* tab.



Flip Chip Route - Advanced - Routing Style Fields and Options

Connect Power	Provides 2 options to connect power between a bump and I/O pad, and ring/stripe.

Bump To Pad	Connects power from bump to pad.
Bump To Ring/Stripe	
	Connects power from bump to I/O ring or stripe.
Multiple Connection	
Multiple Pads to Bump	
	Establishes power routing from multiple pads to one bump.
Multiple Bumps to Pad	
	Establishes power routing from multiple bumps to a single pad.
Routing TSV	
Routing TSV To Bump	
	Connects TSVs to signal bumps.
Routing TSV To IO PAD	
	Connects TSVs to IO pads.
Routing TSV To Power Stripe	
	Connects TSV with power net to the power mesh. For more information, see "TSV/Bump/Back Side Metal Modeling in Innovus" section of the Design Methodology for 3D IC with Through Silicon Via Via chapter in the *Innovus User Guide* .

Related Text Commands

For information on the following command, see " Flip Chip Commands" in the *Text Command Reference* .

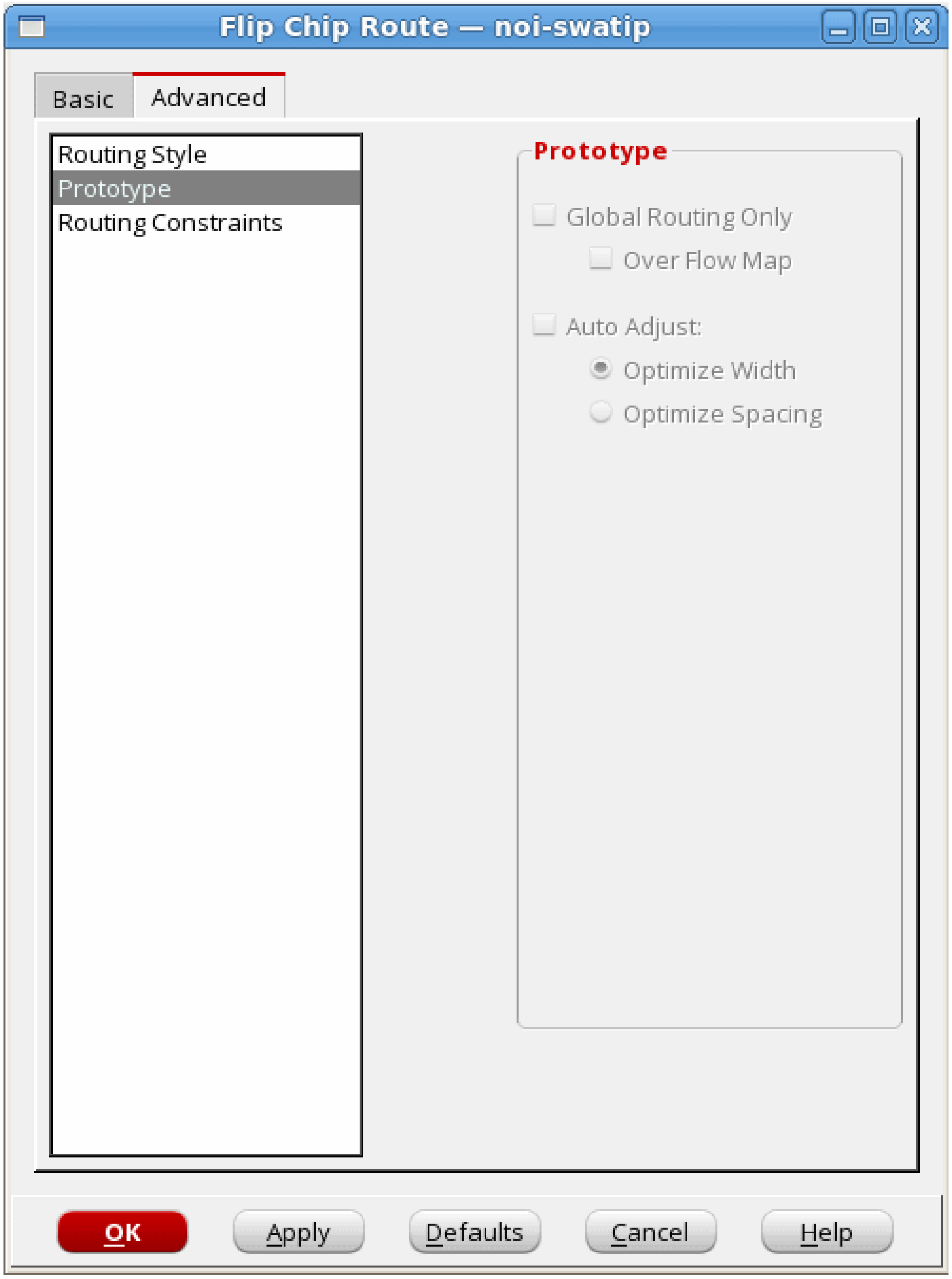
- `fcroute`

-

Flip Chip Route - Advanced - Prototype

Use the *Advanced - Prototype* page of the *Flip Chip Route* form to specify options for global routing and auto adjust the net width and spacing.

- To open the *Advanced - Prototype* page of the *Flip Chip Route* form, choose *Tools - TSV* and select *Route TSV/Bump*. Click the *Advanced* tab and select *Prototype*.



Flip Chip Route - Advanced - Prototype Fields and Options

Global Routing Only	
	Performs global routing only. Plans the interconnect by breaking the routing portion of the design into rectangles called global routing cells (gcells) and assigning the signal nets to the gcells.
Over Flow Map	Displays the thermal map using the width and spacing parameters specified in the extra configuration file.
Auto Adjust	
Optimize Width	Adjusts the width and spacing of each net in the design.
Optimize Spacing	Adjusts the spacing of each net in the design. This option uses the minimum width value of the RDL layer from the LEF file, then increases the spacing for all nets until the maximum allowable spacing is reached. The maximum allowable spacing value is written to the log file as: SPACING *max_value* . **Note:** You do not need a constraint file as input to adjust spacing.

Related Text Commands

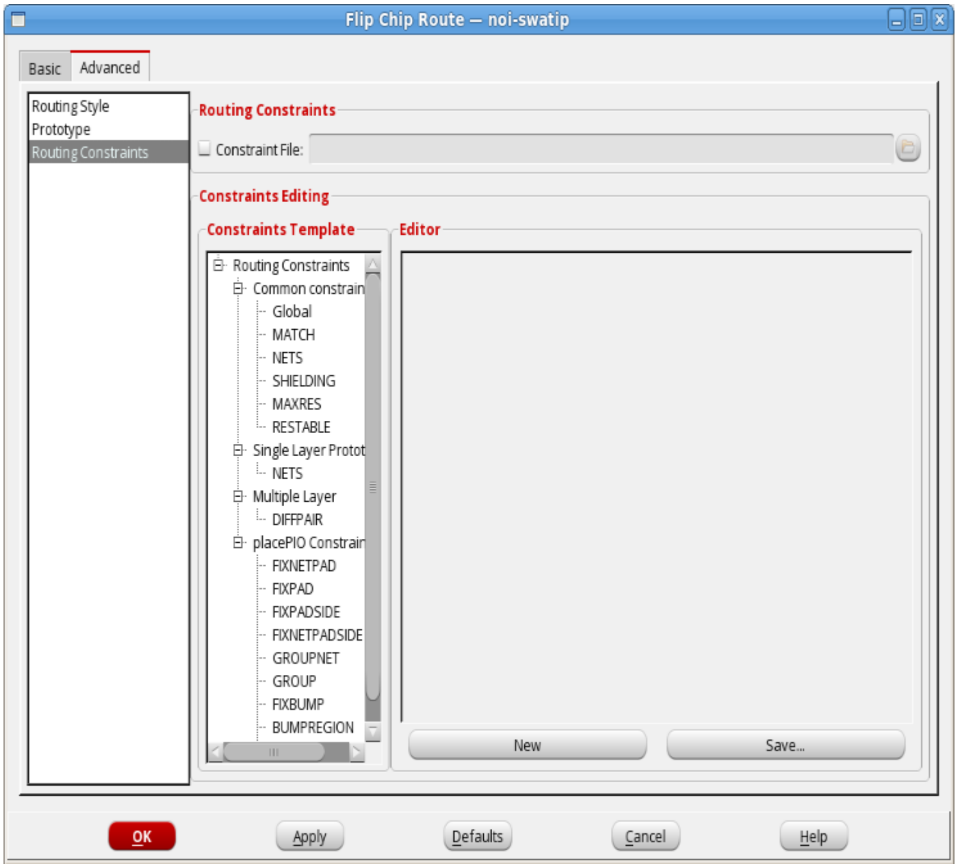
For information on the following command, see "Power Route Commands" in the *Text Command Reference* .

- `fcroute`

Flip Chip Route - Advanced - Routing Constraints

Use the *Advanced - Routing Constraints* page of the Flip Chip Route form to specify and edit the common, single layer prototyping, multiple layer, and placePIO routing constraints.

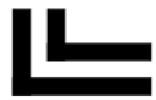
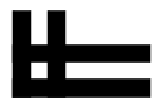
- To open the *Advanced - Routing Constraints* page of the *Flip Chip Route* form, choose *Tools - TSV* and select *Route TSV/Bump* . Click the *Advanced* tab. and select *Routing Constraints* .



Flip Chip Route - Advanced - Routing Constraints Fields and Options

Constraint File	Specifies the file that contains constraints for flip chip routing.
Constraints Template	Provides the list of routing constraints. The *Constraints Template* is divided into separate editable routing constraint blocks: • *Common Constraints* • *Single Layer Prototyping* • *Multiple Layer* • *placePIO Constraint*
Common Constraints Editor	Includes the following:

	Global	The *Global* constraints are:	
		`WIDTH`	Specifies the routing width, in microns. Connects wires to bumps using the specified width only, regardless of the size of the bump or the source to which the bump connects. *Default:* When using the peripheral I/O routing style, flip chip route determines the width of the route as the bump width or I/O cell pin width that is connected to the bump, whichever is smaller. When using the area I/O routing style, flip chip route does not restrict the size of the RDL route to the width of the I/O cell pin and can route a wire that is larger in width than the specified I/O cell pin width.
		`WIDTHRANGE`	Specifies the `minimum:maximum` width range allowed when using the `MAXRES` constraint.
		`SPACING`	Specifies the distance in microns between the net routed by the flip chip router and all other routes. The router uses the spacing value to limit the effect of coupling capacitance on the total capacitance of the net. *Default:* `SPACING` or `SPACINGTABLE` value from the LEF file.

		`SPLITSTYLE`	Specifies the interleaving style used for the split wires. Choose one of the following: `River`: The split wires do not have an interleaving pattern. This is the default. The following illustration shows the pattern for the split wires.  `Mesh`: The split wires interleave with one another, as shown in the following illustration: 
		`SPLITWIDTH`	Specifies the width of the split wire segment.
		`SPLITGAP`	Specifies the gap between split wire segments. If you specify this option, ensure that the distance between the split wire segments must be greater than the specified gap value. If you do not specify this option, the distance between split wire segments is the default minimum spacing value that does not cause DRC violations.
		`MINESCAPE`	Specifies the minimum distance from the edge of the pin to the edge of the wire segment.
		`NOBUMPVIA`	Select `TRUE` if via cannot be placed under a bump. Select `FALSE` if via can be placed under a bump.
		`TAPERING`	Specifies the tapering pin width for routing nets. Tapering is enabled in the area I/O mode. For more information, see " Route Nets with Tapering Pin Widths" in the Flip Chip Methodologies chapter.
	MATCH	The *MATCH* constraints are:	

		`TOLERANCE`	Specifies the tolerance factor between all nets. All the nets must meet the specified tolerance value, else Innovus reports a warning message. *Default:* 0.2
		<2 or more nets>	Specifies 2 or more nets to match tolerance.
	NETS	The *NETS* constraints are:	
		`WIDTH`	Specifies the width of constrained nets, measured in microns. *Default:* 0 (minimum width)
		`WIDTHRANGE`	Specifies the `minimum:maximum` width range allowed when using the `MAXRES` constraint.
		`SPACING`	Specifies the distance in microns between the net routed by the flip chip router and all other routes. The router uses the spacing value to limit the effect of coupling capacitance on the total capacitance of the net. *Default:* `SPACING` or `SPACINGTABLE` value from the LEF file.
		`ROUTELAYERS`	Specifies the layers (layer1:layer2) to which the router is restricted.
		`TAPERING`	Specifies the tapering pin width for routing nets. Tapering is enabled in the area I/O mode.
		<nets>	Specifies the nets used for routing.
	SHIELDING	The *SHIELDING* constraints are:	
		`SHIELDBUMP`	Specifies *TRUE* to shield above the bump and *FALSE* to shield below the bump.
		`SHIELDWIDTH`	Specifies the width of the *Shield Net* , measured in microns.
		`SHIELDGAP`	Specifies the distance in microns between the shield (the special net) and the shielded net (the signal net).

		`SHIELDSTYLE`	Specifies where you want the shield to be placed, *Above* or *Below* or on the *Common* layer.
		`SHIELDNET`	Specifies a special net (typically VSS) used to shield the net which has flip chip constraints.
		<nets>	The first net you specify is the type of net used for the shield (VSS), and the second net is the net to be shielded.
	MAXRES	The *MAXRES* constraints are:	
		`MAXRES`	Specifies the maximum resistance allowed between a bump and an I/O cell. During routing, `fcroute` uses the resistance constraint and sizes the wire width to meet the constraint. If it fails to meet the constraint, the `fcroute` reports failure using the `fcroute -extraConfig` , `srouteFcReportRes fcroute.res` command.
		<nets>	Specifies nets with maximum resistance values.
	RESTABLE	The *RESTABLE* constraints are:	
		<net>	Specifies nets listed in the RESTABLE.
		<value>	Specifies resistance value of the net in the RESTABLE.
Single Layer Prototyping	Includes the following:		
	NETS	The *NETS* constraints are:	
		`WIDTHRANGE`	Specifies the `minimum:maximum` width range allowed when using the `MAXRES` constraint.

		WIDTHSTEP	Specifies a value to increment, within the width range. For example, if the width range is 5:10 and the width step is 1, the width range starts increasing by 1, starting with 5 microns, 6 microns, and so on...until the global routing is complete, with the largest allowed width value. This helps in determining the largest wire width that can be used to complete global routing.
		<nets>	Specifies the nets used for routing.
Multiple Layer	Includes the following:		
	DIFFPAIR	The *DIFFPAIR* constraints are:	
		THRESHOLD	Specifies a value for the difference in target spacing, so the router attempts to meet the specified gap, but does not create a violation if it misses the gap by less than the threshold. *Default:* 20%. The threshold is calculated by using the following formula: $\text{Threshold} = \dfrac{\textit{Length of the longer net} - \textit{Length of the shorter net}}{\textit{Length of the shorter net}}$ For example, if the constrained nets are 24 microns and 20 microns, the threshold would be calculated as (24 - 20) / 20 = 0.2 = 20%. *Default:* Minimum spacing value in the LEF file. **Note:** Gap is the distance in microns between the two differential pair nets.
		<2 nets>	Specifies 2 or more nets to calculate threshold value.
placePIO Constraint	Includes the following:		
	FIXNETPAD	Includes:	
		<nets>	Specifies net pad to assign fixed status.
	FIXPAD		

		<pad instance names>	Assigns fixed status to the specified pad instances.
	FIXPADSIDE	Assigns fixed status to the specified pad side: • *EAST* • *WEST* • *NORTH* • *SOUTH*	
		< *pad instance names* >	Assigns fixed status to the specified pad instances.
	FIXNETPADSIDE	Assigns fixed status to the specified pad side: • *EAST* • *WEST* • *NORTH* • *SOUTH*	
		<nets>	Specifies nets to fix pads.
	GROUPNET	Includes:	
			Specifies nets to be grouped.
	GROUP	Includes:	
		< *pad instance names* >	Specifies pad instances to be grouped.
	FIXBUMP	Includes:	
		<nets>	Specifies nets to fix bumps.

	BUMPREGION	Allows you to specify multiple bump regions to restrict the assignment of specified bumps such as VDD bumps, closest to the I/O pads, if that is where the regions are specified. This is only a soft-constraint and bumps can be moved outside the region to improve routability. The regions must be specified from bottom-left to top-right. The BUMPREGION syntax is described as follows: BUMPREGION AREA *minx1 miny1 maxx1 maxy2* *nets* END AREA END BUMPREGION **Command Flow and Example** : • setFlipChipMode -connectPowerCellToBump true -constraintFile area.constr -layerChangeBotLayer 8 -layerChangeTopLayer 8 -routeWidth 10 • placePIO -assignBump -noRandomPlacement Constraint syntax: area.constr: BUMPREGION AREA 3942.0 3545.0 3903.0 -3979.0 -3868.0 -3932.0 3774.0 -3521.0 VDD* END AREA END BUMPREGION	
		`AREA`	Adds a bump region defined by area coordinates: • *X1 - Specifies the lower-left X coordinate* • *Y1 - Specifies the lower-left Y coordinate* • *X2 - Specifies the upper-right X coordinate* • *Y2 - Specifies the upper-right Y coordinate*
		<nets>	Specifies nets to define the bump region.
	PAIR	Includes:	

		<*net*>	Specifies the net to which the power bump(s) and the I/O instance(s) belongs.
		<*pad instance names*>	Specifies the name(s) of the I/O instance(s).
		<*bump_instance names*>	Specifies the name(s) of the bump(s).

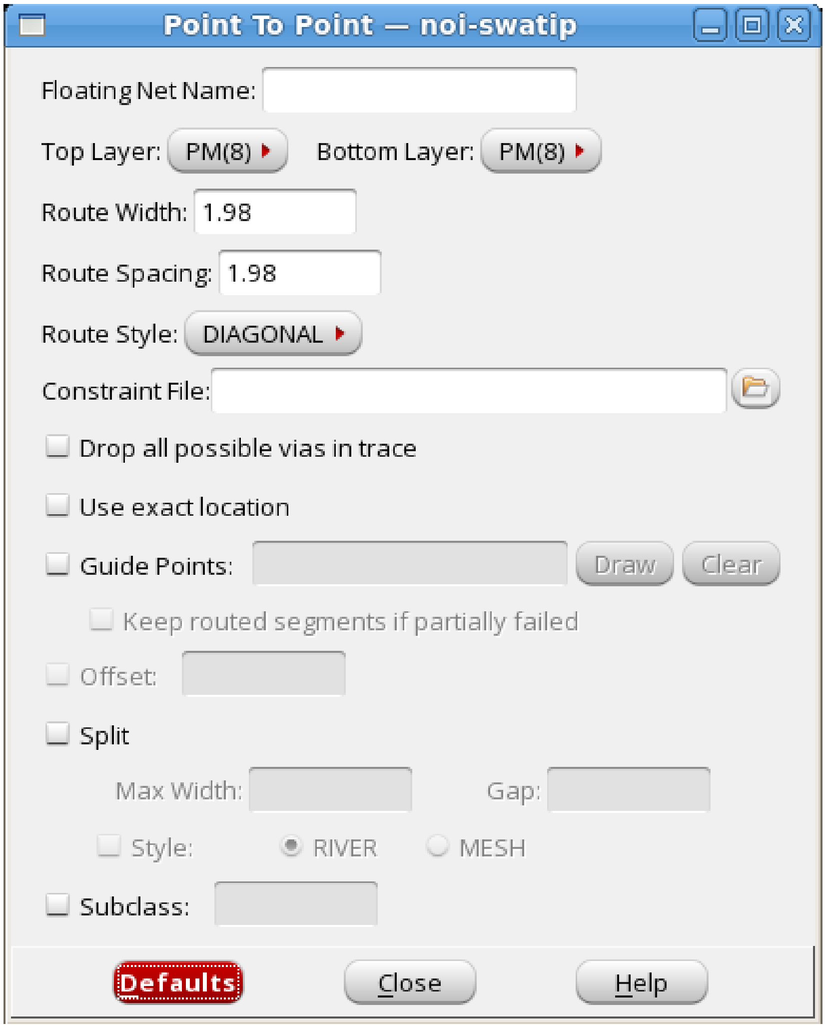
Point To Point Route

Use the Point To Point Route form to create point-to-point routing between an I/O pad pin and bump, or a wire and a bump, or a bump and a stripe, for SPECIALNETS (only) that are defined in the DEF file.

- Choose *Tools* - *TSV* and select *Route Point to Point* .

OR

- Select the *Point To Point Route* icon  and press the *F3* key.



Point-To-Point Fields and Options

Floating Net Name	Specifies the floating net name (SPECIALNET) defined in the DEF file. **Note:** Normally, you need not specify the net name since the router automatically picks up the net name in the GUI.
Top Layer	Specifies the top routing layer for point-to-point routing.
Bottom Layer	Specifies the bottom routing layer for point-to-point routing.
Route Width	Specifies the width of the wires that connect to the bumps, regardless of the size of the bump or the source to which the bump connects.

Route Spacing	Specifies the spacing between the routing wires that connect the bumps and I/O pad pins, or bumps and wires.	
Route Style	Specifies the routing style options for performing the point-to-point routing. • DIAGONAL • DOUBLEBEND • MANHATTAN *Default* : DIAGONAL	
Constraint File	Specifies the routing constraint file.	
Drop all possible vias in trace	Drops all possible vias in the trace	
Use exact location	Uses the exact location that you click to perform routing. If the location does not fulfill the pin access requirements, P2P router performs an auto search to find a new access point.	
Guide Points	Specifies guiding points for routing. Click the *Draw* button and then click the required guide points in the chip area in the main window. Press the Esc key when you are done. The location of all the points you click in the main window are recorded in the *Guide Points* text box and are taken into account for routing. **Note:** You can also press the Shift key to start recording guide points instead of clicking *Draw* . In this case, as you click each guide point in the main window, it is automatically recorded in the *Guide Points* text box so you do not have to press Esc at the end. Click the *Clear* button to clear the contents in the *Guide Points* text box.	
	Keep routed segments if partially failed	Keeps routed segments when routing with guide points fails partially.
Offset	Defines the maximum search offset from the original click location. Select the Use exact location check box and then specify the maximum offset value in the *Offset* text box.	
Split	Specifies whether or not the wire segment should be split.	
	Max Width	Specifies the maximum width for splitting.
	Gap	Specifies the splitting gap.

	Style	Specifies the splitting style. • *RIVER:* Allows only one crossing of the split wire • *MESH:* Allows all split wires to be crossed and also drops all the crossing sections *Default: RIVER*
Subclass	Assigns the specified string as a subclass name to the wires and vias created.	

Related Text Commands

- `routePointToPoint`

Verify Connectivity

To view the details of the Verify Connectivity form, refer to the *Verify Connectivity* section under Verify Menu

Conformal

The *Conformal* submenu provides access to the following features:

- Run LEC
- Conformal Check Constraints
- Conformal Check Budget Constraints
- Conformal Check Assembled Constraints
- Conformal Compare Constraints
- Conformal Derive Critical False Path
- Conformal Promote Constraints

Run LEC

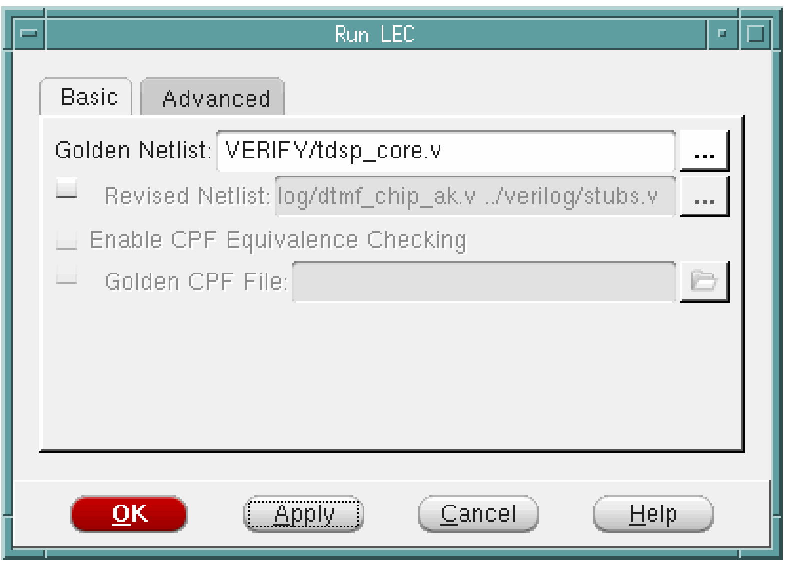
Use the *Run LEC* form to compare the current design netlist against a golden netlist using Conformal Logical Equivalence Checking (LEC).

- Run LEC - Basic
- Run LEC - Advanced

Run LEC - Basic

Use the *Basic* page of the *Run LEC* form to to compare the current design netlist against a golden netlist using Conformal Logical Equivalence Checking. This reports any differences between the two netlists.

- Choose *Tools* - *Conformal* - *Run LEC,* then click the *Basic* tab.



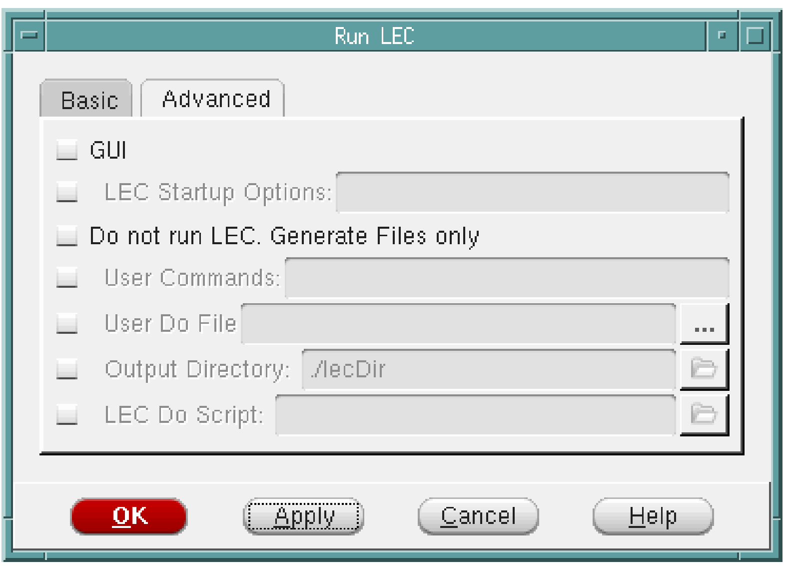
Run LEC - Basic Fields and Options

Golden Netlist	Specifies the golden netlist files.You can type the file names or click... to select the files.
Revised Netlist	Specifies the revised netlist files. You can type the file names or click... to select the files. *Default* : Current netlist file. If the design has changed since loading or saving the design, a new netlist is written out and passed to the software.
Enable CPF Equivalence Checking	Specifies that CPF equivalence checking should be performed. **Note:** This feature requires a low power license for LEC.
Golden CPF File	Specifies the CPF golden file that is to be passed to the LEC software. You can enter the name or click the Browser icon select a file. It requires the `-cpfEc` parameter to be used.

Run LEC - Advanced

Use the *Advanced page* of *Run LEC* form to to specify additional checking options to compare netlists.

- Choose *Tools* - *Conformal* - *Run LEC,* then click the *Advanced* tab.



Run LEC - Advanced Fields and Options

GUI	Runs the Conformal software in GUI mode. This process runs as a parallel job that is separate from the Innovus session. You can continue to run additional Innovus commands while the LEC GUI mode session is running in parallel.
LEC Startup Options	Specifies the extra LEC command options to be used on software startup.
Do not run LEC Generate Files Only	Specifies that the LEC software does not start, however, the LEC script is generated. You can use this option if you need to customize LEC run scripts.
User Commands	Allows the specification of user commands to be added to the LEC script after design import. You can specify multiple commands.
User Do File	Specifies user dofiles to execute as part of the dofile generated by this command. Use this parameter to add custom settings before the LEC software begins mapping.
Output Directory	Specifies the directory in which to generate LEC script and log files.
LEC Do Script	Specifies a dofile script that is to be passed to the LEC software for execution.

Conformal Check Constraints

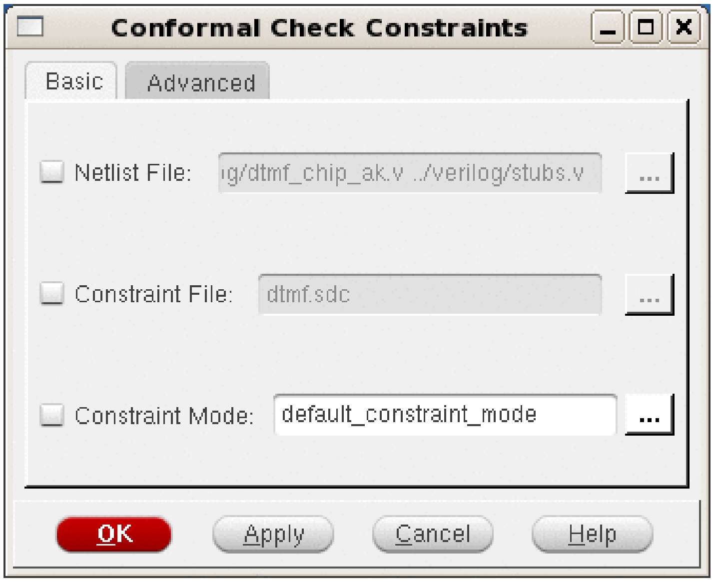
The Conformal Check Constraints form contains the following pages:

- Conformal Check Constraints - Basic
- Conformal Check Constraints - Advanced

Conformal Check Constraints - Basic

Use the *Basic* page of the Conformal Check Constraints form to check the quality of constraints for the current design using the Conformal Constraint Designer software. This performs checks for exceptions, clocks, unconstrained ports and invalid SDC command syntax.

- Choose *Tools* - *Conformal* - *Check Constraints*, then click the *Basic* tab.



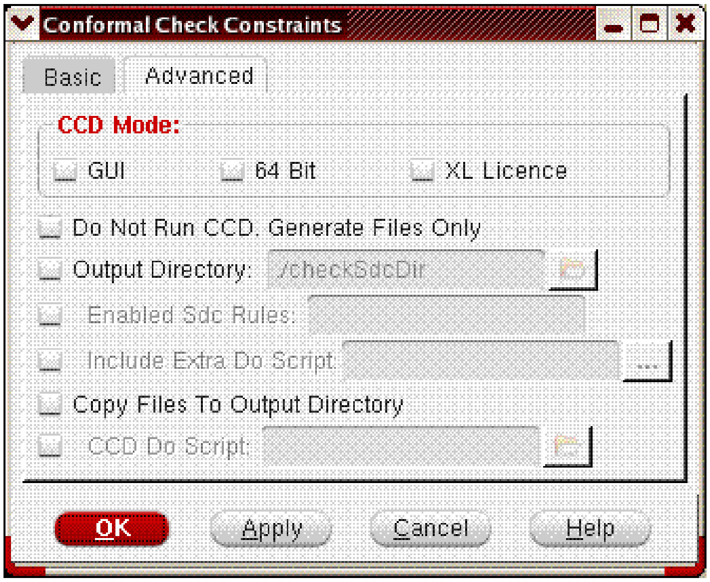
Conformal Check Constraints - Basic Fields and Options

Netlist File	Specifies the name of the netlist file. For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Netlist Files browser window.
Constraint File	Specifies the constraint file(s) to analyze using Conformal Constraint Designer. For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Constraint Files browser window.
Constraint Mode	Specifies the constraint mode.

Conformal Check Constraints - Advanced

Use the *Advanced* page of the Conformal Check Constraints form to specify additional constraint checking options.

- Choose *Tools - Conformal - Check Constraints*, then click the *Advanced* tab.



Conformal Check Constraints - Advanced Fields and Options

GUI	Runs the Conformal Constraint Designer software in GUI mode. This runs as a parallel job separate from the Innovus session--you can continue to run additional Innovus commands while the CCD GUI mode session is running in parallel. The software does not exit at the end of the session, so you can continue interactive debugging in the standalone Conformal GUI after completion of the CCD script. Conformal log messages are not echoed to the Innovus log file. The software creates a separate Conformal log file in the CCD run directory (see the *Output Directory* option). *Default:* Off. The Conformal Constraint Designer software exits at the end of the session. In non-GUI mode, the software is not run as a parallel job, therefore no Innovus command is executed until the CCD script has completed.
64 Bit	Specifies 64-bit CCD. *Default:* 32-bit CCD, or 64-bit if the Innovus software starts in 64-bit mode.
XL License	Runs the Conformal Constraint Designer software with the XL license. *Default:* CCD L license

Do Not Run CCD. Generate Files Only	Specifies that the Conformal Constraint Designer software does not start, however, the CCD script is generated. You can use this option if you need to customize CCD run scripts.
Include Extra Do Script	
	Specifies user do-files to execute as part of the do-file generated by this command. You can specify one or more files.
Output Directory	Specifies the name of the directory in which to generate CCD script and log files. You can enter the name or click the *Browser* icon select a directory from the Output Directory browser window. *Default* :`./checkSdcDir`
Copy Files to Output Directory	Copies design files in the Conformal script to the Conformal run directory. Use the *Output Directory* option to specify the run directory.

Conformal Check Budget Constraints

Use the Conformal Check Constraints form to check the time budget directory's top and block constraints against their pre-partitioned original chip SDCs. Conformal Constraint Designer performs checks for hierarchical constraint mismatches, exceptions, clocks, unconstrained ports, and invalid SDC command syntax.

For more information on SDC checks that the Conformal Constraint Designer software uses to verify SDC data, see the "SDC Rule Checks" chapter of the *Innovus Conformal Constraint Designer Reference Manual*.

You can use this form after running the `savePartition` command.

To use this feature, specify the path to the Conformal Constraint Designer installation before running Innovus .

Note: You must have previously run `deriveTimingBudget -ccd` to generate time budget CCD dofiles and CCD clock map files. These dofile scripts are automatically detected by this form in the *Partition Directory*.

The Conformal Check Constraints form contains the following pages:

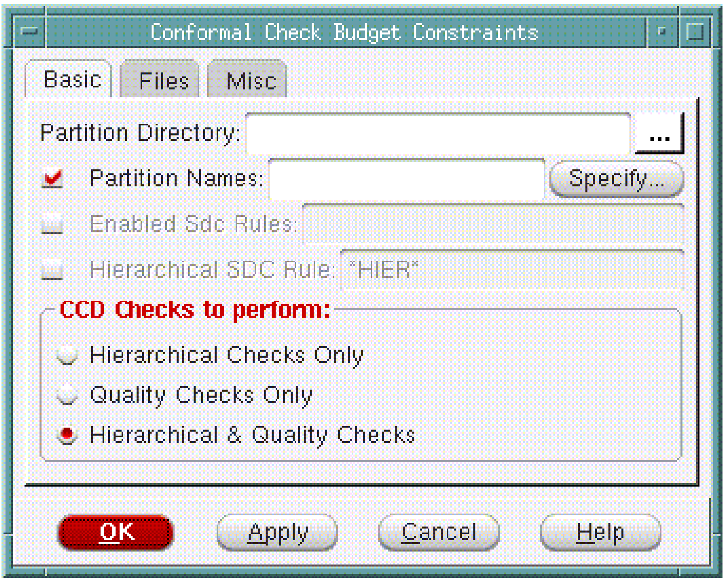
- Conformal Check Budget Constraints - Basic
- Conformal Check Budget Constraints - Files

- Conformal Check Budget Constraints - Misc

Conformal Check Budget Constraints - Basic

Use the *Basic* page of the Conformal Check Constraints form to specify most common settings.

- Choose *Tools* - *Conformal* - *Check Budget Constraints*, then click the *Basic* tab.



Conformal Check Budget Constraints - Basic Fields and Options

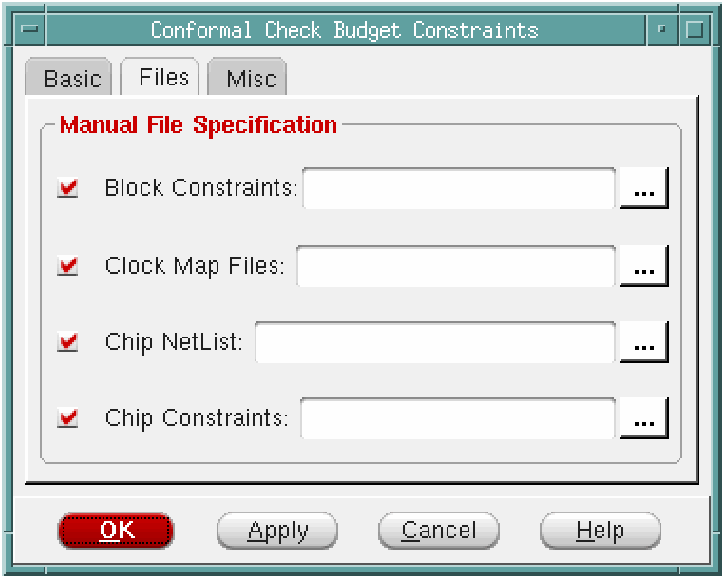
Partition Directory	Specifies the budget or partition directory. Time budget constraints and clockmap files are automatically detected by the `checkBudgetSdcCCD` command in the specified partition directory. You can enter the name or click ... to select a directory.
Partition Names	Specifies the partition names whose constraints should be checked against the original pre-partition chip SDCs. You can enter the name or click the *Specify* button to select a partition name. *Default* : All top and block level partitions under the user- specified partition directory are checked by the CCD software against their original pre-partition chip constraints.
Enabled SDC Rules	Allows specification of user-enabled or disabled rules in CCD to be used during quality rule checking of partition constraints. You can define multiple added and deleted disabled rules. *Default* : A default set of rules are defined on script initialization. The user-enabled rules are added after this default set of rules.
Hierarchical SDC Rule	Specifies the rules to be checked during hierarchical rule checking. *Default* : `*HIER*`
Hierarchical Checks Only	Specifies that only hierarchical rule checking be performed by the CCD software.
Quality Checks Only	Specifies that only quality rule checking for each partition be performed by the CCD software.
Hierarchical & Quality Checks	Specifies that both hierarchical and quality rule checking be performed by the CCD software.

Conformal Check Budget Constraints - Files

Use the *Files* page of the Conformal Check Constraints form to specify constraint, mapping, and netlist files manually. You can use this page after saving the partition information to the current or specified directory

Note: You must have previously run `deriveTimingBudget – ccd` to generate time budget CCD dofiles. These dofile scripts are automatically detected by this form in the *Partition Directory*.

- Choose *Tools - Conformal - Check Budget Constraints*, then click the *Files* tab.



Conformal Check Budget Constraints - Files Fields and Options

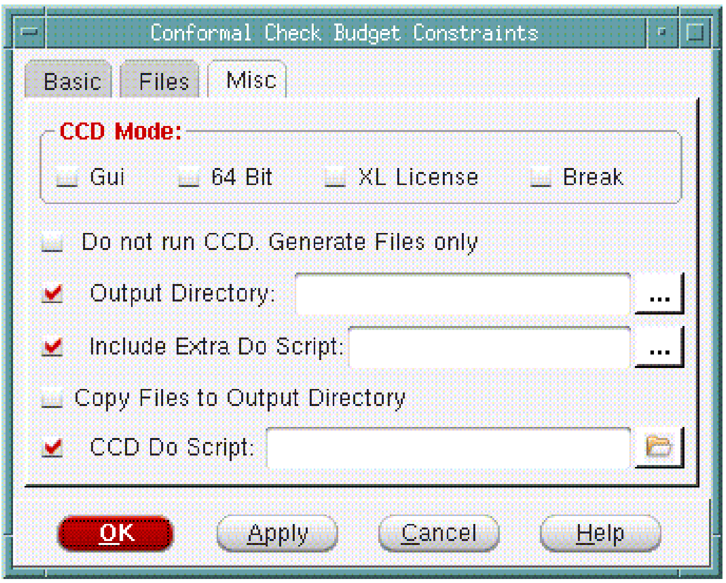
Block Constraints	Allows manual specification of the budgeted constraints files to be used during Conformal Constraint Designer analysis. You can enter the name or click ... to select a file or files. *Default* : Constraints are automatically detected in the partition directory.
Clock Map Files	Allows manual specification of the clock map file(s) that contain hierarchically equivalent clocks. This option is useful for overriding clock map files. You can enter the name or click ... to select a file or files. *Default* : The netlist is automatically detected from the Innovus database. In most cases, the clock map file(s) are automatically detected from the Innovus database and passed to CCD without having to use this option.
Chip Netlist	Allows manual specification of the original chip netlist file(s) to analyze using CCD. This option is useful for overriding chip netlist settings You can enter the name or click ... to select a file or files. *Default* : The netlist is automatically detected from the Innovus database.
Chip Constraints	Allows manual specification of the original chip constraints file(s) to analyze using CCD. This option is useful for overriding chip constraints. You can enter the name or click ... to select a file or files. *Default:* Constraints are automatically detected from the Innovus database.

Conformal Check Budget Constraints - Misc

Use the *Misc* page of the Conformal Check Constraints form to specify additional options for checking the time budget directory's top and block constraints against their pre-partitioned original chip SDCs. You can use this page after saving the partition information to the current or specified directory.

Note: You must have previously run `deriveTimingBudget -ccd` to generate time budget CCD dofiles. These dofile scripts are automatically detected by this form in the *Partition Directory*.

- Choose *Tools* - *Conformal* - *Check Budget Constraints*, then click the *Misc* tab.



Conformal Check Budget Constraints - Misc Fields and Options

Gui	Runs the Conformal Constraint Designer software in GUI mode. This runs as a parallel job separate from the Innovus session--you can continue to run additional Innovus commands while the CCD GUI mode session is running in parallel. The software does not exit at the end of the session, so you can continue interactive debugging in the standalone Conformal GUI after completion of the CCD script. Conformal log messages are not echoed to the Innovus log file. The software creates a separate Conformal log file in the CCD run directory (see the *Output Directory* option). *Default:* Off. The Conformal Constraint Designer software exits at the end of the session. In non-GUI mode, the software is not run as a parallel job, therefore no Innovus command is executed until the CCD script has completed.
64 Bit	Specifies 64-bit CCD. *Default:* 32-bit CCD, or 64-bit if the Innovus software starts in 64-bit mode.
XL License	Runs the Conformal Constraint Designer software with the XL license. *Default:* CCD L license

Break	Specifies that the generated dofile should contain a "break" command after checking each partition constraints file. This is useful for interactive debug of partition constraints using the SDC Rule Manager. After browsing quality checks in the SDC Rule Manager, type `continue` to proceed on the CCD command line.
	
	The CCD software will then proceed to check the next partition and then break again, until finally all partition constraints have been checked.
	
	Note: This option is only available with the *Gui* option.
	
	Default : CCD will not perform any breaks. Interactive debug of partition constraint's quality checks using the SDC Rule Manager will not be possible. The SDC Rule Manager will only display hierarchical rule check results.
	
	Quality checks can be examined instead in the individual partition reports in the following file:
	
	`checkBudgetSdcDir/`
	`rule_check.quality.<partitionName>.rpt`

Do Not Run CCD. Generate Files Only	Specifies that the Conformal Constraint Designer software does not start, however, the CCD script is generated. You can use this option if you need to customize CCD run scripts.
Output Directory	Specifies the name of the directory in which to generate CCD script and log files. You can enter the name or click ... to select a directory. *Default* : `./checkBudgetSdcDir`
Copy Files to Output Directory	Copies design files in the Conformal script to the Conformal run directory. Use the *Output Directory* option to specify the run directory.
Include Extra Do Script	
	Specifies user do-files to execute as part of the do-file generated by this command. You can specify one or more files.
CCD Do Script	Specifies an existing dofile script that should be passed to the CCD software for execution. You can enter the name or click the *Browser* icon select a file. *Default* : A new dofile script is generated based on user specified `checkBudgetSdcCCD` options and used to run the CCD software.

Conformal Check Assembled Constraints

The Conformal Check Assembled Constraints form contains the following pages:

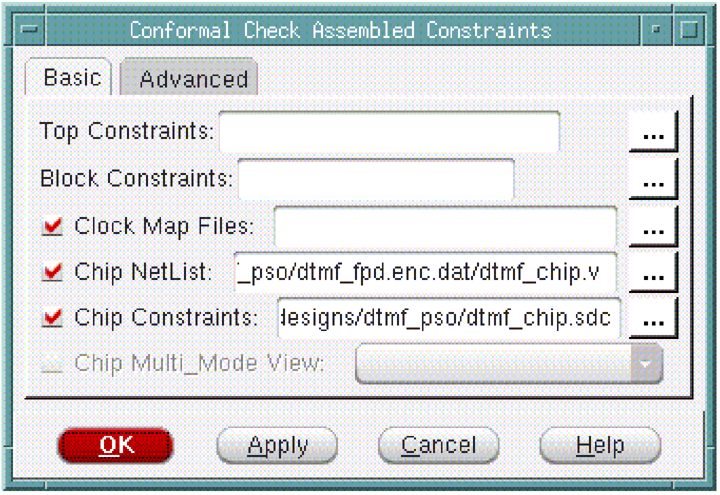
- Conformal Check Assembled Constraints - Basic
- Conformal Check Assembled Constraints - Advanced

Conformal Check Assembled Constraints - Basic

Use the *Basic* page of the Conformal Assembled Check Constraints form to check pre-assembled design top and block constraints against post-assembled design chip constraints. The Conformal Constraint Designer performs checks for hierarchical constraint mismatches, exceptions, clocks, unconstrained ports, and invalid SDC command syntax. You can use this form after running the `assembleDesign` command.

For more information on SDC checks that the Conformal Constraint Designer uses to verify SDC data, see the "SDC Rule Checks" chapter of the *Innovus Conformal Constraint Designer Reference Manual*.

- Choose *Tools* - *Conformal* - *Check Assembled Constraints*, then click the *Basic* tab.



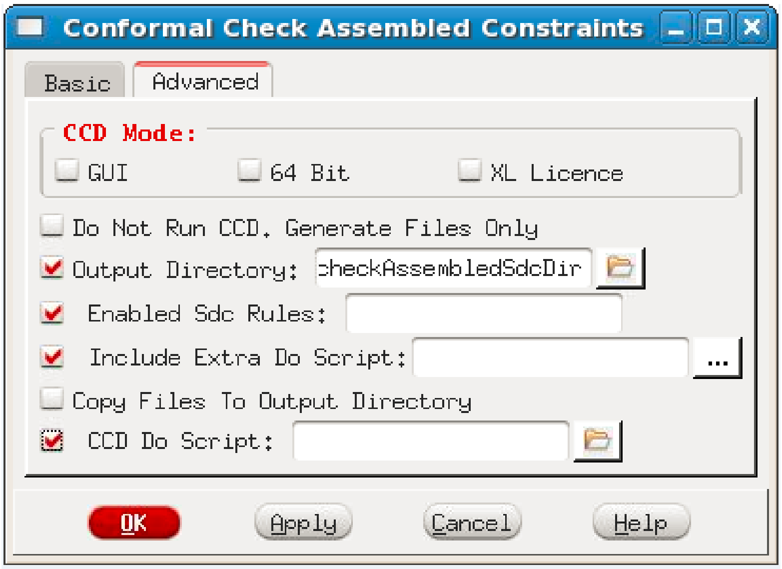
Conformal Check Assembled Constraints - Basic Fields and Options

Top Constraints	Specifies the pre-assembly top level constraint file(s). For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Top Constraints Files browser window.
Block Constraints	Specifies the pre-assembly block constraints. You must provide either one combination or multiple combinations of both instance name(s) and corresponding constraint file name(s). For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Block Hierarchical Instances & Constraints browser window.
Clock Map Files	Specifies clock map file(s) that contain hierarchically equivalent clocks. For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Clock Map File browser window. **Note:** Use the clock map files previously generated when running the `deriveTimingBudget –ccd` command. *Default:* Partition map file.
Chip Netlist	Specifies the chip netlist file(s). For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Chip Netlist browser window. *Default:* Current netlist file. If the design has changed since loading or saving the design, a new netlist is written out and passed to the software.
Chip Constraints	Specifies the chip constraint file(s). For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Chip Constraint File browser window. *Default:* Current SDC file.
Chip Multi_Mode View	Specifies the multi-mode chip-level view name. If a design has multiple modes, you can specify which set of view constraints to pass to Conformal with this option. **Note:** Multi-mode constraints and views must already be specified.

Conformal Check Assembled Constraints - Advanced

Use the *Advanced* page of the Conformal Check Assembled Constraints form to specify additional options for checking pre-assembled design top and block constraints against post-assembled design chip constraints.

- Choose *Tools - Conformal - Check Assembled Constraints*, then click the *Advanced* tab.



Conformal Check Assembled Constraints - Advanced Fields and Options

GUI	Runs the Conformal Constraint Designer software in GUI mode. This runs as a parallel job separate from the Innovus session--you can continue to run additional Innovus commands while the CCD GUI mode session is running in parallel. The software does not exit at the end of the session, so you can continue interactive debugging in the standalone Conformal GUI after completion of the CCD script. Conformal log messages are not echoed to the Innovus log file. The software creates a separate Conformal log file in the CCD run directory (see the *Output Directory* option). *Default:* Off. The Conformal Constraint Designer software exits at the end of the session. In non-GUI mode, the software is not run as a parallel job, therefore no Innovus command is executed until the CCD script has completed.

64 Bit	Specifies 64-bit CCD. *Default:* 32-bit CCD, or 64-bit if the Innovus software starts in 64-bit mode.
XL License	Runs the Conformal Constraint Designer software with the XL license. *Default:* CCD L license
Do Not Run CCD. Generate Files Only	Specifies that the Conformal Constraint Designer software does not start, however, the CCD script is generated. You can use this option if you need to customize CCD run scripts.
Output Directory	Specifies the name of the directory in which to generate CCD script and log files. You can enter the name or click the *Browser* icon select a directory from the Output Directory browser window. *Default* :.`/checkAssembledSdcDir`
Enabled Sdc Rules	Allows specification of user-enabled or disabled rules in CCD to be used during rule checking constraints.
Include Extra Do Script	Specifies user do-files to execute as part of the do-file generated by this command. You can specify one or more files.
Copy Files to Output Directory	Copies design files in the Conformal script to the Conformal run directory. Use the *Output Directory* option to specify the run directory.
CCD Do Script	Specifies a dofile script that is used to run the CCD software. This option runs `checkAssembledSdcCCD -script`.

Conformal Compare Constraints

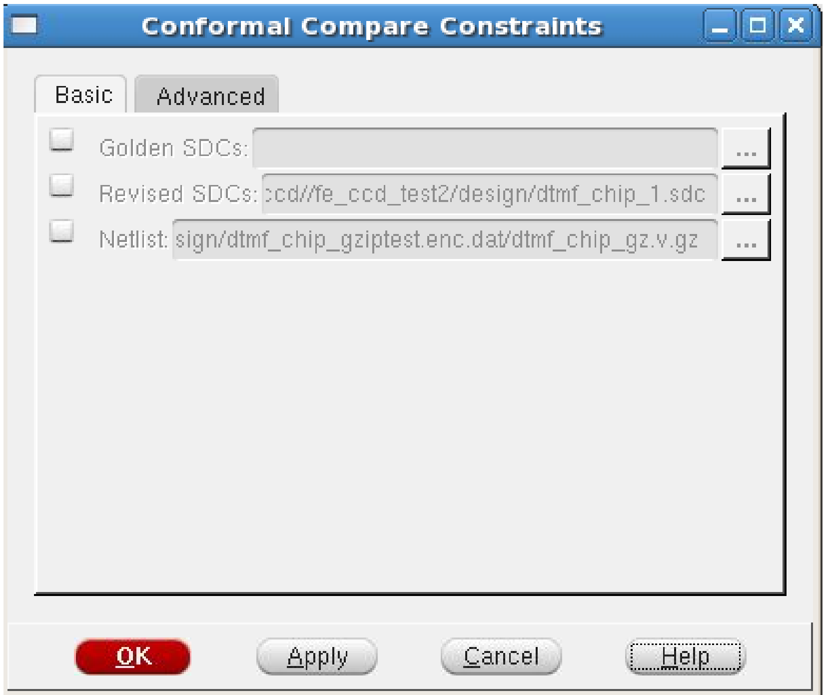
The Conformal Compare Constraints form contains the following pages:

- Conformal Compare Constraints - Basic
- Conformal Compare Constraints - Advanced

Conformal Compare Constraints - Basic

Use the Basic page of the *Conformal Compare Constraints* form to:

- Choose *Tools* - *Conformal* - *Compare Constraints*, and then click the *Basic* tab.

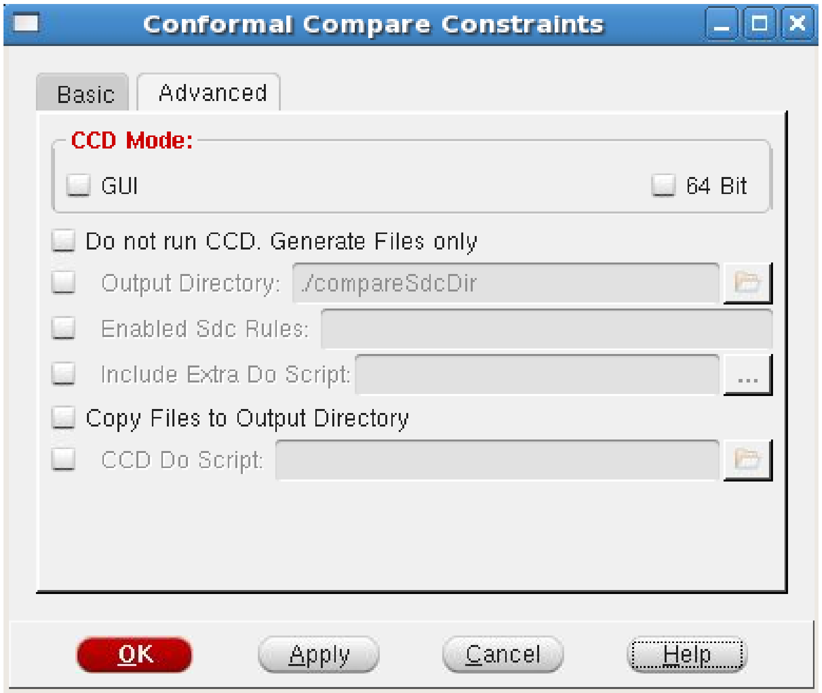


Conformal Compare Constraints - Basic Fields and Options

Golden SDCs	Specifies the golden SDC constraint files to pass to the software.
Revised SDCs	Specifies the revised constraint files to pass to the software.
Netlist	Specifies the netlist files.

Conformal Compare Constraints - Advanced

- Choose Tools - Conformal - Compare Constraints, and then click the Advanced tab.


Conformal Compare Constraints
Basic
Advanced
CCD Mode:
GUI
64 Bit
Do not run CCD. Generate Files only
Output Directory:
./compareSdcDir
Enabled Sdc Rules:
Include Extra Do Script:
Copy Files to Output Directory
CCD Do Script:
OK
Apply
Cancel
Help

Conformal Compare Constraints - Advanced Fields and Options

GUI	Runs the CCD software in GUI mode.
64 Bit	Runs CCD in 64-bit mode.
Do not run CCD. Generate Files only.	Generates a CCD script without starting the CCD software.
Output Directory	Specifies the directory in which to generate CCD script and log files.
Enabled Sdc Rules	Allows specification of user-enabled or disabled rules in CCD to be used during rule checking constraints. You can define multiple added and deleted disabled rules.
Include Extra Do Script	Specifies user dofiles to execute as part of the dofile generated by this command
Copy Files to Output Directory	Copies design files in the Conformal script to the Conformal run directory. Use the -outputDir parameter to specify the run directory.
CCD Do Script	Specifies a dofile script to pass to the CCD software for execution.

Conformal Derive Critical False Path

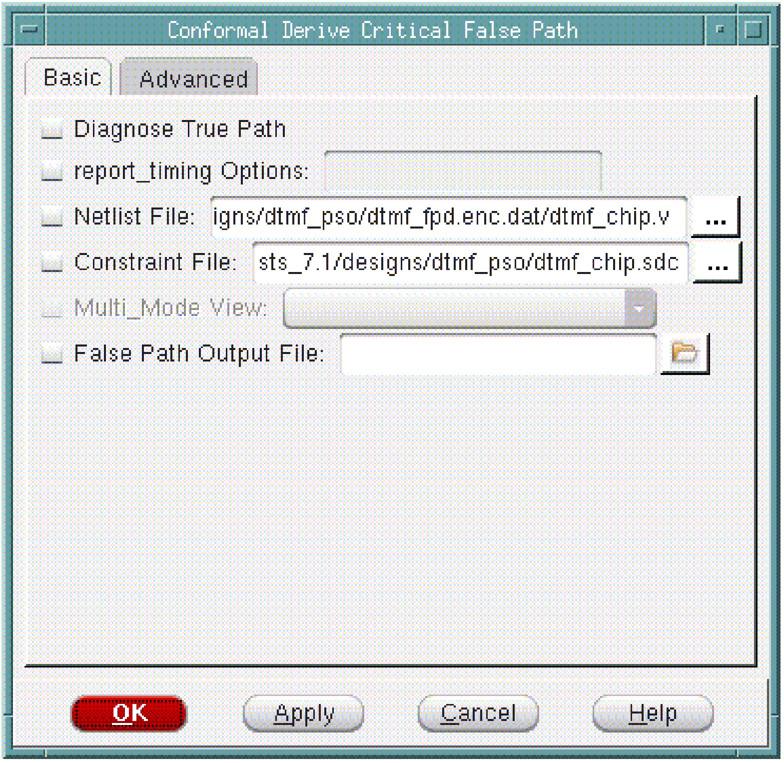
The Conformal Derive Critical False Path form contains the following pages:

- Conformal Derive Critical False Path - Basic
- Conformal Derive Critical False Path - Advanced

Conformal Derive Critical False Path - Basic

Use the *Basic* page of the Conformal Derive Critical False Path form to analyze critical false paths based on the Innovus CTE timing information and constraints. A set of false paths are output which can be loaded into Innovus. These false paths can eliminate unnecessary netlist optimizations and can improve design area and timing. You can use this form after loading design with timing constraints.

- Choose *Tools - Conformal - Derive Critical False Paths*.


Conformal Derive Critical False Path
Basic
Advanced
Diagnose True Path
report_timing Options:
Netlist File:
igns/dtmf_pso/dtmf_fpd.enc.dat/dtmf_chip.v
Constraint File:
sts_7.1/designs/dtmf_pso/dtmf_chip.sdc
Multi_Mode View:
False Path Output File:
OK
Apply
Cancel
Help

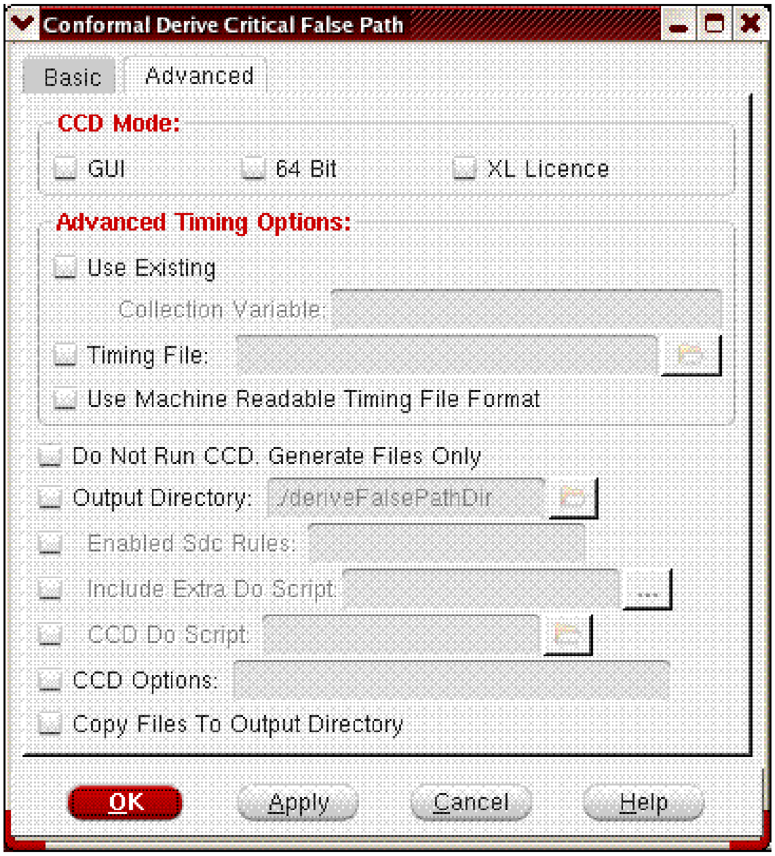
Conformal Derive Critical False Path - Basic Fields and Options

Diagnose True Path	Instructs the software to analyze chosen timing paths and diagnose each one as true or false. Generates a report, including the justification for each diagnosis. *Default:* Analyzes only the worst timing path.
report_timing Options	Specifies the `report_timing` options to use when generating the timing file information to pass to CCD software.
Netlist File	Specifies the name of the netlist file. For multiple files, separate each filename with a space. You can enter the name(s) or click *...* to select them from the Netlist Files browser window. *Default* : Passes the existing design netlist to the software. If the design has changed since previously loading or saving the design, a new netlist is written out and passed to the Conformal Constraint Designer software.
Constraint File	Specifies the constraint file(s) to analyze using Conformal Constraint Designer. For multiple files, separate each filename with a space. You can enter the name(s) or click *...* to select them from the Constraint Files browser window. *Default* : Passes the existing design constraints to the software. If the design has changed since previously loading or saving the design, a new constraint file is written out and passed to the software.
Multi_Mode View	Specifies the multi-mode view name. If a design has multiple modes, you can specify which set of view constraints to pass to Conformal with this option. This view is also used by CTE to generate the timing debug file to pass to the Conformal Constraint Designer software. **Note:** Multi-mode constraints and views must already be specified. *Default* : If you do not select *Constraint File*, the current design SDC file is passed to the Conformal software for analysis.
False Path Output File	Specifies the name of the output false-path file. You can enter the name or click the *Browser* icon select a file from the False Path Output File browser window. *Default* : `criticalFalsePaths.sdc`. This file is generated in output directory specified by the Output Directory option.

Conformal Derive Critical False Path - Advanced

Use the *Advanced* page of the Conformal Derive Critical False Path form to specify additional options to analyze critical false paths in CCD based on Innovus-CTE timing information and constraints.

- Choose *Tools* - *Conformal* - *Derive Critical False Paths*, then click the *Advanced* tab.



Conformal Derive Critical False Path - Advanced Fields and Options

CCD Mode	Select one of the following modes:

	GUI	Runs the CCD software in GUI mode. CCD runs as a parallel job, separate from the Innovus session--you can continue to run additional Innovus commands while the CCD session is running in parallel. Because there is no exit command at the end of the CCD script when called with this option, you can continue interactive debugging in the Conformal GUI after completion of the CCD script. Conformal log messages are not echoed to the Innovus log file in GUI mode; instead, the software creates a separate Conformal log file in the CCD run directory. Specify the run directory with the *Output Directory* option. *Default* : Runs the CCD software in non-GUI mode and exits upon completion of the CCD script. CCD log messages are echoed to the Innovus log file. In non-GUI mode, CCD is not run as a parallel job, therefore no Innovus commands are executed until the CCD script completes.
	64 Bit	Specifies 64-bit CCD. *Default* : 32-bit CCD, or 64-bit if the Innovus software starts in 64-bit mode.
	XL License	Runs the Conformal Constraint Designer software with the XL license. *Default:* CCD L license
Advanced Timing Options		
Use Existing	Specifies a previously generated collection of timing paths to use to pass timing information to the CCD software. The timing paths contained in the user-defined collection are then passed to the CCD software in a Standard Format Timing File. Specify the collection of timing paths by selecting the *Collection Variable* option, along with your own set of reporting options as required. *Default* : The software performs timing analysis. A collection containing the timing paths is used to generate a standard format timing file to pass to the CCD software.	
	Collection Variable	Generates a collection of timing paths for use by the *Use Existing* option.

Timing File	Specifies a previously generated timing debug file to pass to the Conformal Constraint Designer software. Enter the name or click the *Browser* icon select a file from the Timing File browser window.
	
	You can generate this file. For example, to generate a machine-readable file for maximum slack value, run the following command:
	
	`report_timing -machine_readable -max_points 30000 \`
	`  -nworst 100 -max_slack 0.20 > timing_debug.rpt`
	
	Default : Timing analysis generates a machine-readable timing file to pass to the software.

Use Machine Readable Timing File Format	Uses the machine-readable format when passing timing file information to the CCD software. *Default* : The CCD standard format is used to pass timing file information to the CCD software.
Do Not Run CCD. Generate Files Only.	Generates a CCD script without starting the Conformal Constraint Designer software. Use this option to customize CCD run scripts.
Output Directory	Specifies the name of the directory in which to generate CCD script and log files. Enter the name or click the *Browser* icon to select a directory from the Output Directory browser window. *Default* :`./deriveFalsePathDir`
Include Extra Do Script	Specifies user do-files to execute as part of the do-file generated by this command. You can specify one or more files.
CCD Options	Specifies how you want the Conformal Constraint Designer software to handle exception validation and exception generation.
Copy Files to Output Directory	Copies design files in the Conformal script to the Conformal run directory. Use the *Output Directory* option to specify the run directory.

Conformal Promote Constraints

The Conformal Promote Constraints form contains the following pages:

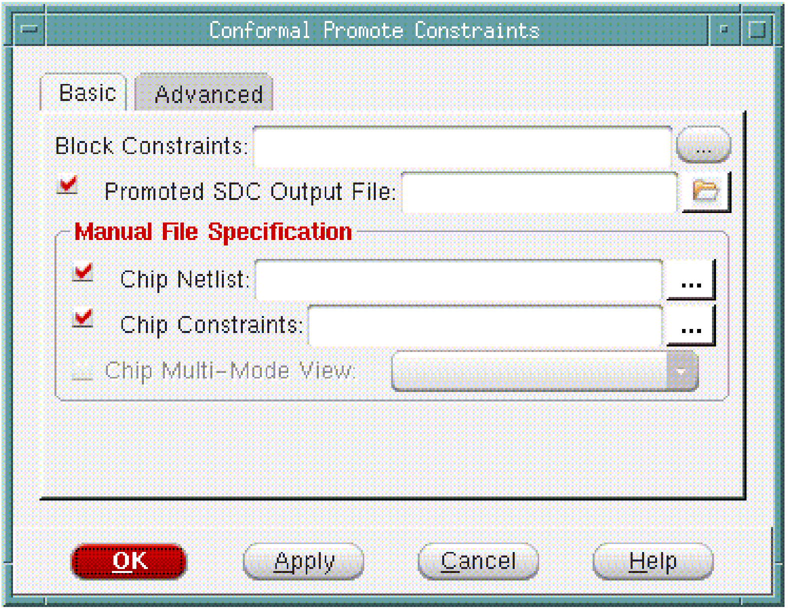
- Conformal Promote Constraints - Basic
- Conformal Promote Constraints - Advanced

Conformal Promote Constraints - Basic

Use the *Basic* page of the Conformal Promote Constraints form to generate top level constraints using Conformal Constraint Designer by promoting block-level constraints to the top level, integrating them with any existing chip-level constraints.

To use this feature, specify the path to the Conformal Constraint Designer installation before running Innovus.

- Choose *Tools* - *Conformal* - *Promote Constraints*.



Conformal Promote Constraints - Basic Fields and Options

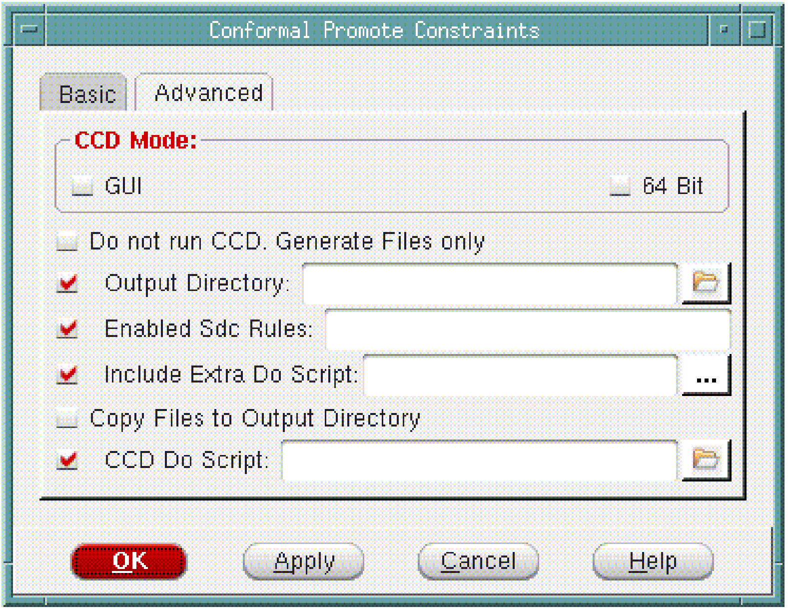
Block Constraints	Specifies the block constraints to be passed to Conformal Constraint Designer for SDC promotion. You must provide either one combination or multiple combinations of both instance name(s) and corresponding constraint file name(s).
Promoted SDC Output File	Specifies the output SDC file. *Default* : `promotedChip.sdc`. This file is generated in output directory specified by the *Output Directory* option in this form's *Advanced* page.
Chip Netlist	Allows manual specification of the original chip netlist file(s) to analyze using Conformal Constraint Designer. This option is useful for overriding chip netlist settings. You can enter the name or click ... to select a file or files. *Default:* The netlist is automatically detected from Innovus database.
Chip Constraints	Specifies the SDC chip constraint file(s) to be passed to Conformal Constraint Designer for SDC promotion. You can enter the name or click ... to select a file or files. **Note:** This option cannot be used in conjunction with *Chip Multi-Mode View.* *Default:* Passes the existing design constraints to the software. If the design has changed since loading or saving the design, a new constraint file is written out and passed to the software.
Chip Multi-Mode View	Specifies the multi-mode chip-level view name. If a design has multiple modes, you can specify which set of view constraints to pass to Conformal with this option. **Note:** Multi-mode constraints and views must already be specified. *Default:* If you do not use the *Chip Constraints* option, the current design SDC file is passed to the Conformal software for analysis.

-

Conformal Promote Constraints - Advanced

Use the *Advanced* page of the Conformal Promote Constraints form to specify additional options to promote block-level constraints to the top level.

- Choose *Tools* - *Conformal* - *Promote Constraints*, then click the *Advanced* tab.



Conformal Promote Constraints - Advanced Fields and Options

GUI	Runs the Conformal Constraint Designer software in GUI mode. This runs as a parallel job separate from the Innovus session--you can continue to run additional Innovus commands while the CCD GUI mode session is running in parallel. The software does not exit at the end of the session, so you can continue interactive debugging in the standalone Conformal GUI after completion of the CCD script. Conformal log messages are not echoed to the Innovus log file. The software creates a separate Conformal log file in the CCD run directory (see the *Output Directory* option). *Default:* Off. The Conformal Constraint Designer software exits at the end of the session. In non-GUI mode, the software is not run as a parallel job, therefore no Innovus command is executed until the CCD script has completed.
64 Bit	Specifies 64-bit CCD. *Default:* 32-bit CCD, or 64-bit if the Innovus software starts in 64-bit mode.

Do not run CCD. Generate Files only	Specifies that Conformal Constraint Designer software does not start, however, the CCD script is generated. You can use this option if you need to customize CCD run scripts.
Output Directory	Specifies the name of the directory in which to generate CCD script and log files. *Default* :`./promoteSdcDir`.
Enabled SDC rules	Allows specification of user-enabled or disabled rules in CCD to be specified during CCD do file initialization. You can define multiple added and deleted disabled rules. *Default* : The following default set of rules are defined on script initialization: `add rule instance –def` The user-enabled rules are added after this default set of rules.
Include Extra Do Script	Specifies user do-files to execute as part of the do-file generated by this command. You can specify one or more files.
Copy Files to Output Directory	Copies design files in the Conformal script to the Conformal run directory. Use the *Output Directory* option to specify the run directory. *Default* : Design files are not copied to the CCD run directory.
CCD Do Script	Specifies an existing dofile script that should be passed to the CCD software for execution. *Default* : A new dofile script is generated based on user specified `checkBudgetSdcCCD` options and used to run the CCD software.

DFM

The *Tools -> DFM* menu allows you to use the LPA and CCP tools from within Innovus to perform the foundry-recommended or mandatory lithography and CMP checks at the block and chip level in your design, much earlier in the development cycle.

LPA enables you to identify litho hotspots and predict contours across process windows based on foundry-qualified technology files. It accurately predicts manufacturing variations associated with lithography and etch. CCP, on the other hand, allows you to identify the potential yield issues that are due to the variations in interconnect thickness caused by Chemical and Mechanical Polishing (CMP). CCP accurately predicts the thickness of the interconnect and dielectric for any design and any manufacturing process that has been calibrated. The resulting prediction is then used to minimize performance loss and to identify thickness-related yield issues.

You can specify the settings for the LPA run by using the *Tools -> DFM -> Litho -> Verify Litho* menu option. This opens up the *Verify Litho* form in which you can specify the LPA run settings for Routing Layers Only mode and Sign-Off mode. This form also allows you to submit the LPA run to identify litho hotspots as per the defined settings. You can view the hotspots in the Innovus *Violation Browser*, once the LPA run is complete.

The *Tools - DFM - CMP - Verify CMP* menu option allows you to specify the settings for the CMP run in the *Verify CMP* form. This form allows you to submit the CMP run as per the defined settings and view the identified hotspots in the *Violation Browser*, once the CMP run is complete. You can use CMP for hotspot identification in the Sign-Off mode only.

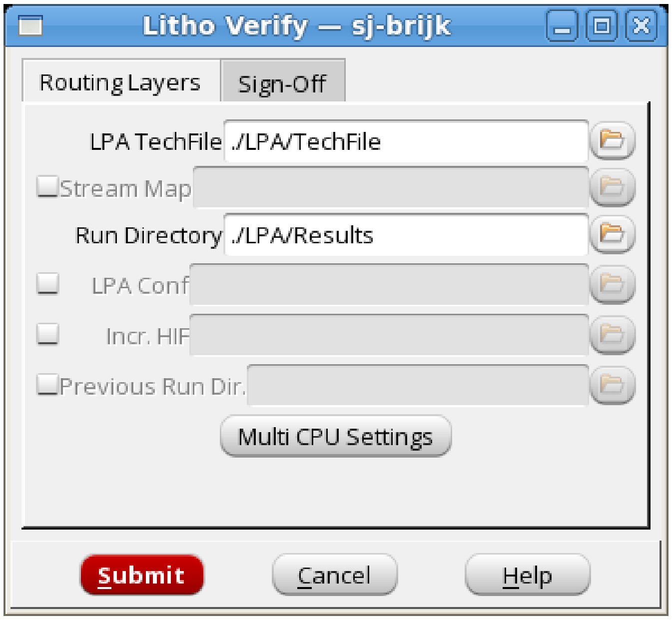
The following forms can be invoked from the *Tools -> DFM* menu to set the run options for LPA and CMP and submit the LPA and CMP simulations:

- Litho Verify - Routing Layers
- Litho Verify - Sign-Off
- CMP Verify - Sign-Off

Litho Verify - Routing Layers

Use the *Routing Layers* tab of the *Litho Verify* form to specify the settings for running LPA in Routing Layers Only mode. This is a faster mode of flagging L1 hotspots in a design before the Sign-Off phase. By running LPA in Routing Layers Only mode, you obtain information about most of the litho hotspots at the block level and can fix these hotspots inside Innovus.

Note: LPA in Routing Layers Only mode is enabled only when you have the Encounter DFM GXL Option license.



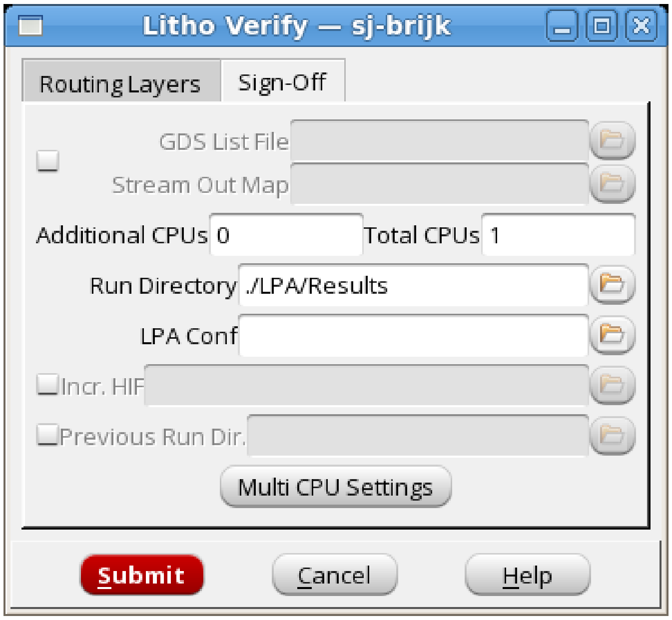
Litho Verify - Routing Layers Fields and Options

LPA TechFile	Specify the qualified LPA Mx- technology file that includes process-specific hotspot checking options and the LPA model. This model captures the GDSII-to-silicon flow of the targeted process, enabling LPA to predict the variations and hotspots due to lithography, defocus conditions, RET (resolution enhancement techniques), OPC (optical proximity correction), PSM (phase shift mask), and retargeting directly from the design database. Alternatively, to enable the GLOBALFOUNDRIES DRC+ flow, you specify the path to the Pattern technology file in the *LPA TechFile* field. Important: LPA enables both simulation-based and pattern-based litho checks. Consult your foundry support to get the appropriate LPA technology file.
Stream Map	Specifies the name and path of the stream out map file, which maps the GDS stream to the layers in the Innovus database. **Note:** The GDS layer numbers in the stream out layer map should match the numbers in the LPA layer map.
Run Directory	Specify the LPA output directory. This directory contains one subdirectory for each layer. The individual subdirectories for each layer are created when LPA is run with the configuration file for that layer.

LPA Conf	(Optional) Select this check box to specify the name and path of the LPA custom configuration file. This file, if specified, controls all run options of LPA. It can also specify different instructions for each layer.
Incr. HIF	(Optional) Select this check box and specify the name and path of the HIF file that you want to use for incremental validation. This HIF file includes the locations that identify the areas affected by each hotspot fix. LPA reads these locations and performs incremental checking only in these areas. This reduces the time for validation.
Previous Run Dir	(Optional) Select this check box to specify the path to the run directory of a previous Verify Litho run that you want to use for XOR-based incremental validation. When this option is selected, the previous run results are compared to the new design and LPA is run only in locations where the layout has changed and where hotspots previously existed, thereby reducing the overall validation run time. This flow is recommended when the design has been changed but no HIF file that identifies the changed areas is available. If the layout changes are from litho fixing, an HIF containing the change of areas should be saved and the *Incr HIF* option should be used instead of the *Previous Run Dir* option. If both the *Previous Run Dir* and the *Incr HIF* options are specified, only the *Previous Run Dir* will be considered and the *Incr HIF* will be ignored.
Multi CPU Settings	Click to specify the LSF settings for the LPA run. By default, LPA will use the LSF settings from *Multi-CPU Settings* GUI in Innovus. However, if you change the multi-CPU settings for the LPA run, this will change the distributed options for all Innovus commands.
Submit	Launch the LPA run with the specified settings.
Cancel	Cancel the LPA run and close the GUI.

Litho Verify - Sign-Off

Use the *Sign-Off* tab of the *Litho Verify* form to specify the settings to run LPA for Litho Sign-Off, as mandated by foundries. By running LPA in the Sign-Off mode, you obtain hotspot information at the block level and can fix these hotspots inside Innovus.



Litho Verify - Sign-Off Fields and Options

GDS List File	(Optional) Specify the name and path of the text file containing the list of GDS files for LEF abstracts. By default, LPA runs on the interconnect layers in Sign-Off mode but if the GDS List file and Stream Out Map file are specified, LPA runs on the potential IP blocks defined in these files.
Stream Out Map	(Optional) Specify the name and path of the Stream Out Map file created by Innovus to map the GDS stream to the layers in the Innovus database. If the GDS List file and Stream Out Map file are specified, LPA runs on the potential IP blocks defined in these files.
Additional CPUs	Specify the number of additional CPUs for the current sign-off LPA run. This number is in addition to the total number of CPUs specified in the *Total CPUs* field. A higher number of additional CPUs results in decreased run time.
Total CPUs	Specify the total number of CPUs available for the sign-off LPA run.
Run Directory	Specify the LPA output directory. This directory contains one subdirectory for each layer. The individual subdirectories for each layer are created when LPA is run with the configuration file for that layer.

LPA Conf	Specify the name and path of the LPA configuration file containing the Techfile and other settings. This file controls all run options of LPA. It can also specify different instructions for each layer. Alternatively, to enable the GLOBALFOUNDRIES DRC+ flow, specify the path to the configuration file that points to the Pattern technology file provided by GLOBALFOUNDRIES. Important: The LPA Pattern matching flows are much faster than full simulation-based flows and provide comparable accuracy results.
Incr. HIF	(Optional) Select this check box and specify the name and path of the HIF file that you want to use for incremental validation. This HIF file includes the locations that identify the areas affected by each hotspot fix. LPA reads these locations and performs incremental checking only in these areas. This reduces the time for validation.
Previous Run Dir	(Optional) Select this check box to specify the path to the run directory of a previous Verify Litho run that you want to use for XOR-based incremental validation. When this option is selected, the previous run results are compared to the new design and LPA is run only in locations where the layout has changed and where hotspots previously existed, thereby reducing the overall validation run time. This flow is recommended when the design has been changed but no HIF file that identifies the changed areas is available. If the layout changes are from litho fixing, an HIF containing the change of areas should be saved and the *Incr HIF* option should be used instead of the *Previous Run Dir* option. If both the *Previous Run Dir* and the *Incr HIF* options are specified, only the *Previous Run Dir* will be considered and the *Incr HIF* will be ignored.
Multi CPU Settings	Click to specify the LSF settings for the LPA run. By default, LPA will use the LSF settings from the Multi-CPU Settings GUI in Innovus. However, if you change the multi-CPU settings for the LPA run, this will change the distributed options for all Innovus commands.
Submit	Launch the LPA run with the specified settings.
Cancel	Cancel the LPA run and close the GUI.

CMP Verify - Sign-Off

Use the *CMP Verify* form to specify the settings to run CMP analysis at block level or chip level during the Sign-Off phase. You can use the *CMP Verify* form to set the options to run CMP simulation using the Cadence flow.

CMP Verify - Sign-Off Fields and Options

GDS List File	(Optional) Specify the name and path of the text file containing the list of GDS files for LEF abstracts. By default, CMP analysis runs on the interconnect layers in Sign-Off mode but if the GDS List file and Stream Out Map file are specified, CMP runs on the potential IP blocks defined in these files.
Stream Out Map	(Optional) Specify the name and path of the Stream Out map file created by Innovus to map the GDS stream to the layers in the Innovus database. If the GDS List file and Stream Out Map file are specified, CMP runs on the potential IP blocks defined in these files.

VMP Files	Specify the name and path of the `vmp.xml` file to be used for the CMP run. The extraction and prediction results of the CMP analysis are based on the specifications in your vmp file.
Output Directory	Specify the output directory path. This directory contains the extraction and prediction results of the CMP run.
VMP Name	Specify the name of the vmp process calibration from the `vmp.xml` file.
CCP Conf	(Optional) Specify the name and path of the CMP configuration file. This file controls all run options of the CMP simulation.
Start Level	(Optional) Specify the starting metal level for the CMP simulation. You can use this field along with the *End Level* field to control the number of layers for prediction.
End Level	(Optional) Specify the end metal level for the CMP simulation. You can use this field along with the *Start Level* field to control the number of layers for prediction.
DP Setting	Click this button to set the multiple CPU options for the CMP run. By default, the multiple CPU settings of Innovus are used for the CMP run. If you modify the multi-CPU settings for the CMP run, this will change the distributed options for all Innovus commands.
TSMC Process	Select this check box if you do not want to use the Cadence model.
VCMP Engine	Specify the location and name of the VCMP engine. This field is enabled only when you select the *TSMC Process* check box.
Process File	Specify the location and name of the VCMP process file. This field is enabled only when you select the *TSMC Process* check box.
Submit	Launch the CMP simulation run with the specified settings.
Cancel	Cancel the CMP run and close the GUI.

Snapshot

You can use the SnapShot feature to create and view snapshots of your designs. Use the *Create SnapShot* form to save a snapshot of your design at any stage of flow, including in the batch mode. The feature also allows you to view snap shots through either the *View SnapShot* form or in batch mode.

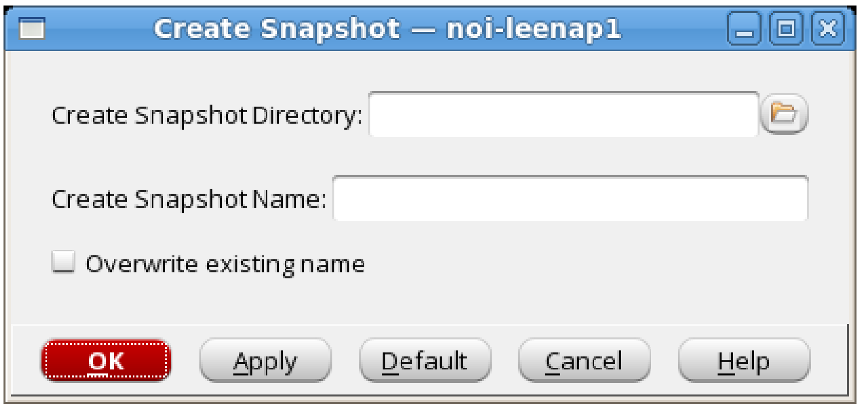
In this section we discuss the following:

- Create Snapshot
- View Snapshot

Create Snapshot

The Create Snapshot screen allows you to select the directory in which you want to save the snapshots you create and name the snapshots. The snapshot are.gif images of the design in the floorplan, amoeba, and physical views. If the metrics (WNS, TNS, congestion, and overlaps) cannot be extracted because of unavailability of data, the snapshots will be created but the metrics column will be populated with N/A.

- Go to *Tools - Snapshot - Create Snapshot*.



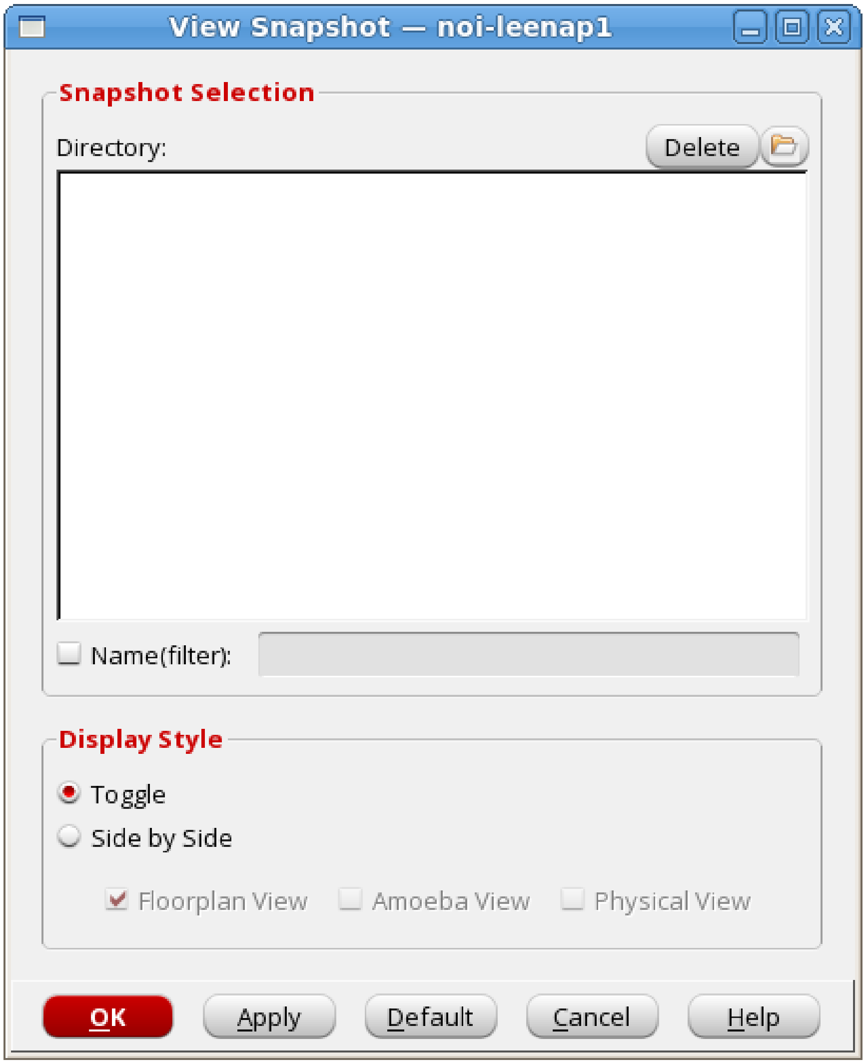
Create Snapshot Fields and Options

Create Snapshot Directory	Select the directory where you want to create the snapshots.
Create Snapshot Name	Provide a name to the snapshot.
Overwrite Existing Name	If the name you provide is unique you do not have to click this button. The system automatically overwrites old files.

View Snapshot

Use the View Snapshot form to view a snapshot that you had saved earlier.

- Go to *Tools - Snapshot - View Snapshot*.

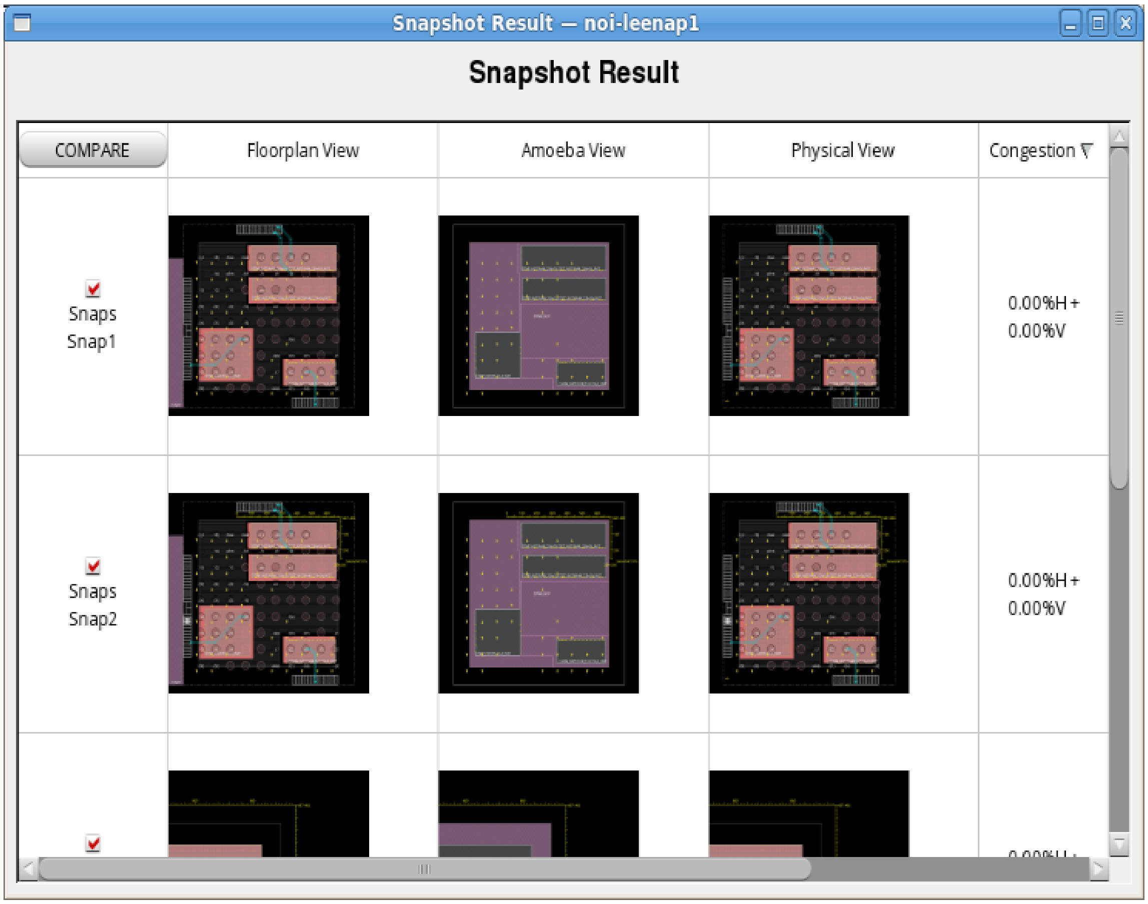


View Snapshot Fields and Options

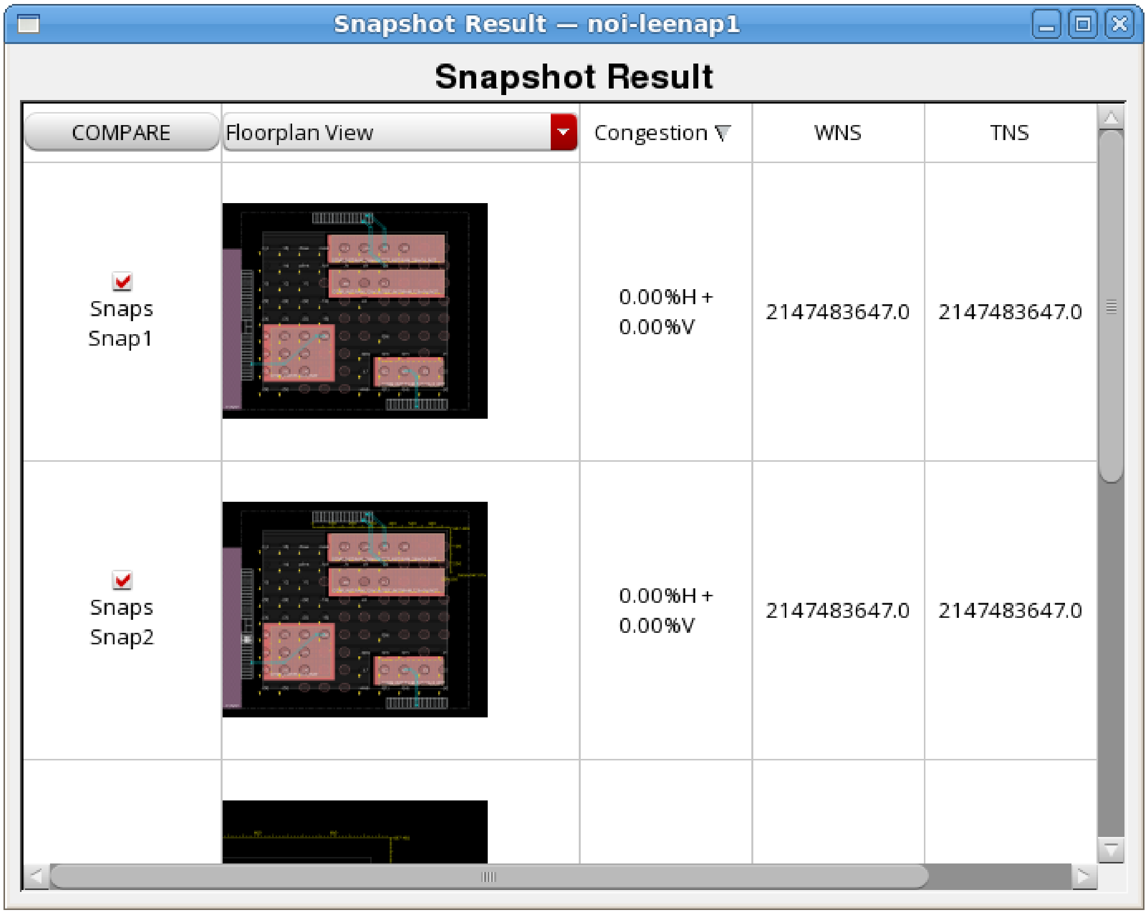
Directory	Allows you to select the directory from where you want to view the snapshot.
Delete	Deletes directory or file.
Name	Provides the name of the snapshot you want to view.
Toggle	Shows snapshots in Toggle mode where you can toggle between Floorplan, Amoeba, and Physical views.
Side by Side	Shows snapshots in selected views (Floorplan, Amoeba, and Physical) side by side.

Note: In the Side by Side view you can select either of these or any two of these or all three of these by clicking the relevant check box. The views are: Floorplan, Amoeba, or Physical. The default view is Floorplan.

An example of the side-by-side view:



An example of the toggle view:



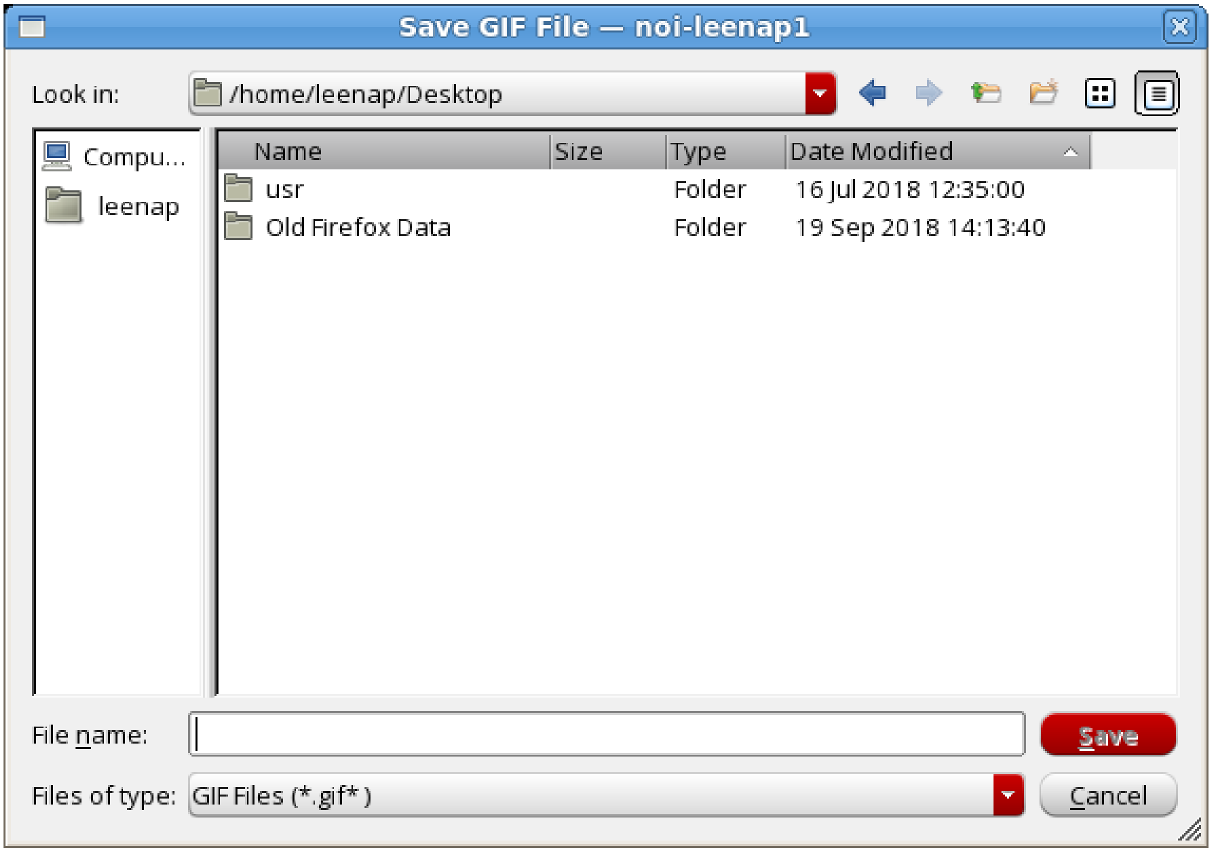
Screen Capture

- Write To GIF File
- Screen Dump
- Display Screen Dump

Write To GIF File

Use the Write To GIF File menu command to save the snapshot of the current screen to a GIF file in the current directory.

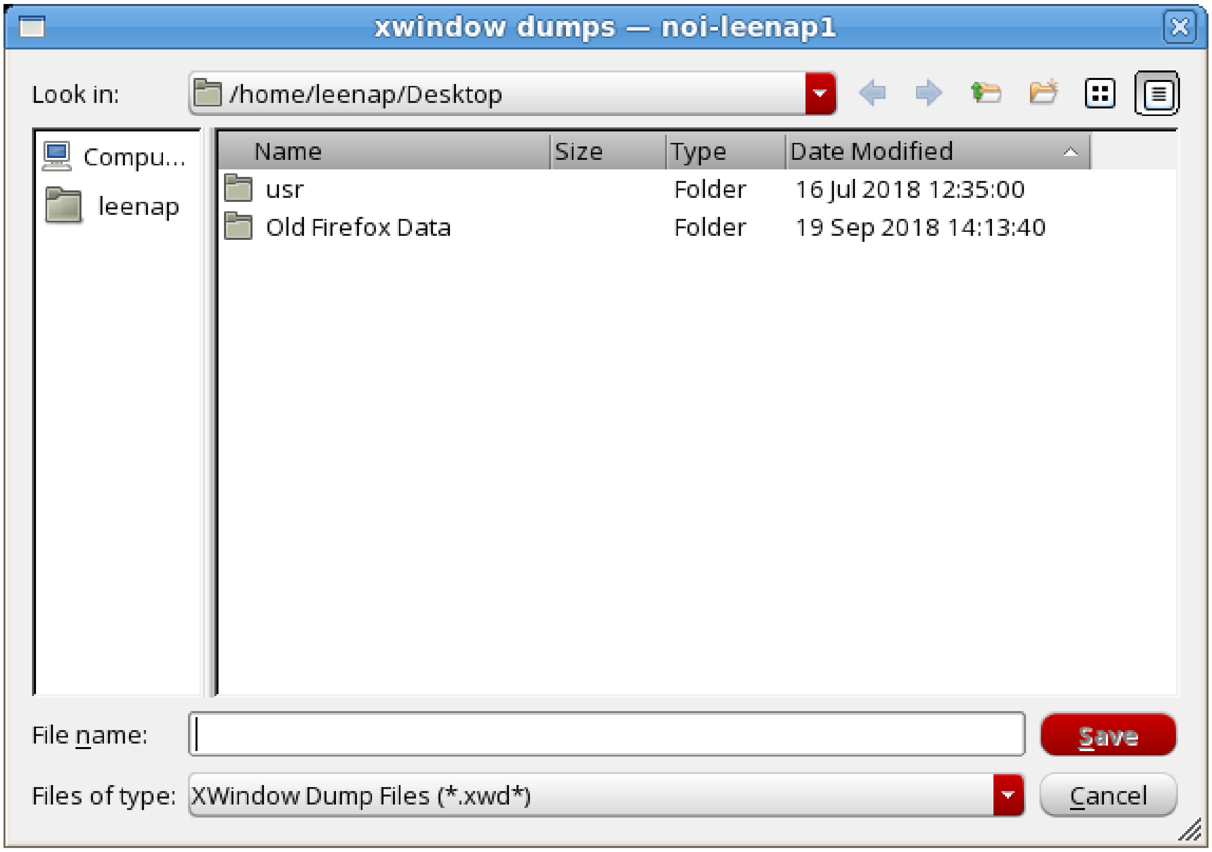
- Choose *Tools - Screen Capture - Write To GIF File*.



Screen Dump

Use the Screen Dump menu command to take a snapshot of the current screen. The file name is in timestamp format that shows when the snapshot was taken. The gzipped file, with the `.gz` extension, is listed in the text window.

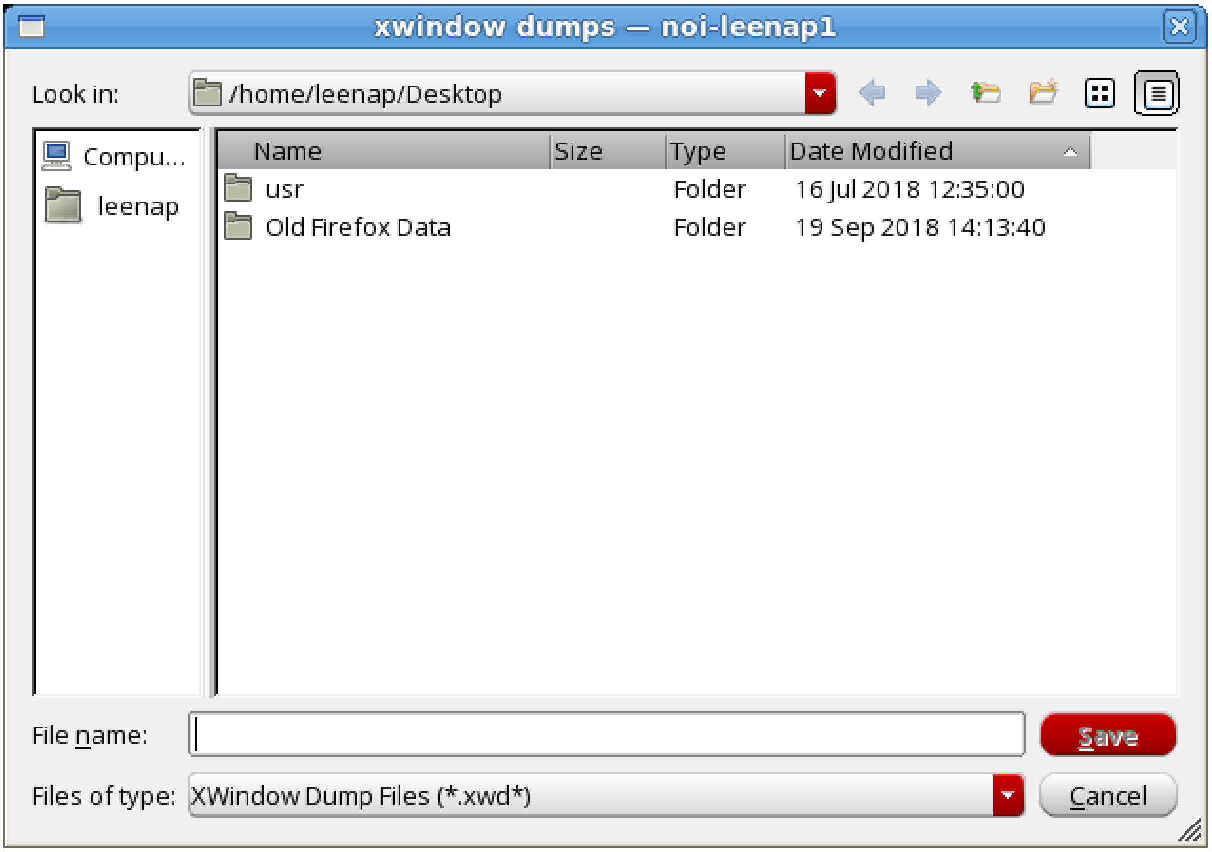
- Choose *Tools - Screen Capture - Screen Dump*.



Display Screen Dump

Use the Display Screen Dump menu command to view snapshots that you have taken earlier.

- Choose *Tools - Screen Capture - Display Screen Dump*.



Create Ruler

Use the Create Ruler menu command to add a ruler using the Create Ruler Preferences form.

Create Ruler Preferences

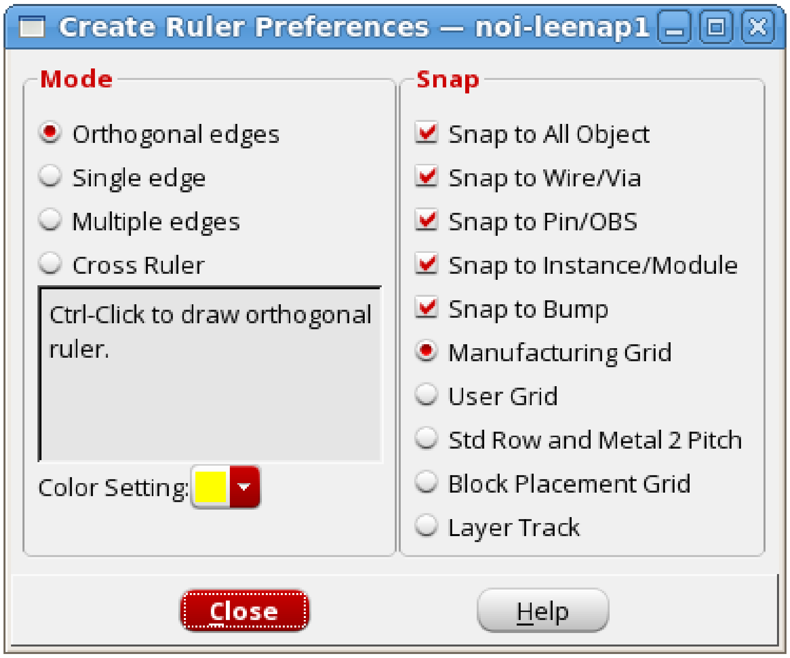
Use the Create Ruler Preferences form to set the direction in which ruler lines are drawn.

To open the Create Ruler Preferences form:

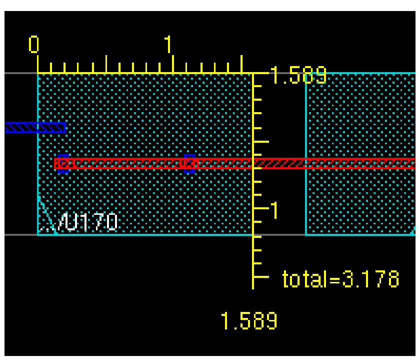
- Choose *Tools - Create Ruler*.

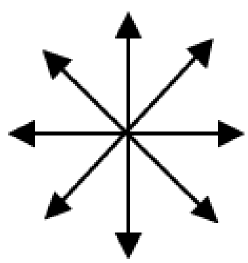
or

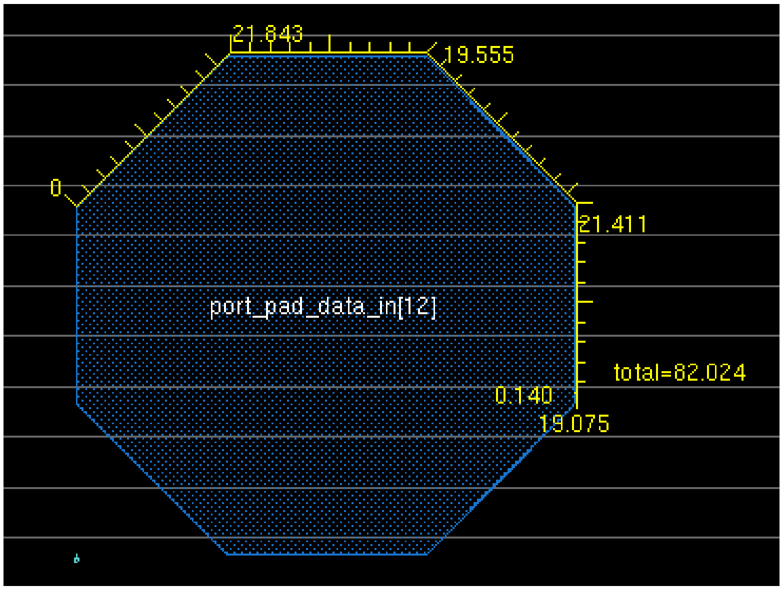
- Click the *Create Ruler* widget  and press the `F3` key.

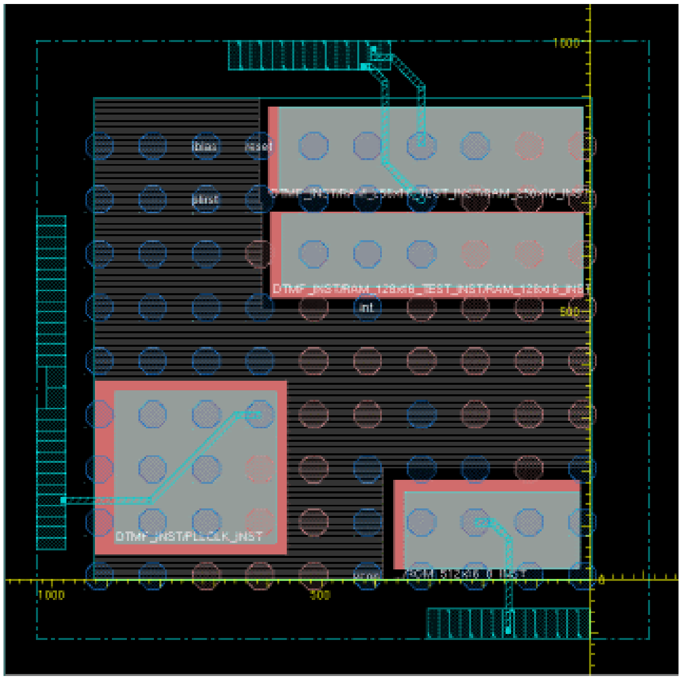


Create Ruler Preferences - Fields and Options

Mode	Specifies the direction of the ruler.	
	Orthogonal edges	Specifies that ruler lines can be drawn in horizontal as well as vertical directions. Use this option if you want to measure orthogonal edges, such as follows:  **Note**: This is the default ruler mode. Click the *Create Ruler* widget and start drawing the ruler to measure orthogonal edges. To end the ruler, click or press `Enter`.

	Single edge	Specifies that ruler line can be drawn in a single direction. Use this option if you want to measure a single edge in one of the following directions: • Vertical • Horizontal • Diagonal (45 degrees, 135 degrees) • Any angle To draw a vertical, horizontal, or diagonal (45 or 135 degrees) ruler, simply click at the point where you want the ruler to start and move the mouse in the required direction. The ruler line will follow one of the following defined directions automatically.  To draw a ruler at an angle other than the above eight directions, keep the `Shift` key pressed and then start drawing the ruler at the required angle. To end a Single edge ruler, either click at the point where you want to end the ruler or press `Enter`.

	Multiple edges	Specifies that ruler lines can be turned in multiple directions. Use this option if you want to measure multiple segments in a complex pattern.  To draw a *Multiple edges* ruler, click at the point where you want the ruler to start. Move the mouse in the required direction, clicking at every point you want the ruler to turn. To end the ruler, double-click or press `Enter`. **Note**: To draw a ruler in a direction other than horizontal, vertical or diagonal (45 or 135 degrees), keep the `Shift` key pressed and then start drawing the ruler at the required angle.

	Cross Ruler	Specifies that ruler lines can be drawn in a + shape. Use this option to measure two edges at the same time, see the overall X and Y length, or to check alignment of macros.  To draw a cross ruler, click anywhere in the design. A + ruler is displayed occupying the entire display area in both X and Y directions. The center of the + moves with the cursor. Move the center of the + to the point where you want the origin of the ruler. Press Enter to place and end the ruler.

Snap	Specifies the snap settings for the ruler. You can choose which design object to snap to by selecting one or more of the following options: • *Snap to All Object* • *Snap to Wire/Via* • *Snap to Pin/OBS* • *Snap to Instance/Module* • *Snap to Bump* You can also choose one of the following options for snapping: • *Manufacturing Grid* (Default) • *User Grid* • *Std Row and Metal 2 Pitch* • *Block Placement Grid* • *Layer Track*
Color Setting	Allows you to choose a new color for the ruler.

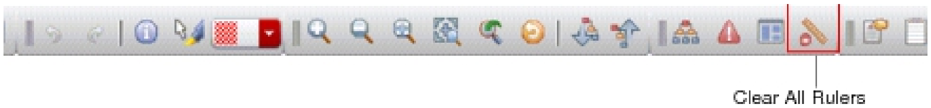
Related Commands

- createRuler

Clear All Rulers

Select *Tools - Clear All Rulers* to clear all ruler lines.

You can also clear the ruler lines with the Clear All Rulers icon in the main window.



Related Commands

- clearAllRulers

17

Windows Menu

Workspaces

Innovus enables you to save and load your customized window settings easily through workspaces. A workspace contains customized main window settings including:

- Size and placement of window
- Specific orientation of toolbars
- Docking status
- Visibility settings

Use the *Workspaces* submenu to manage your workspaces. To access this submenu:

- Choose *Windows - Workspaces*.

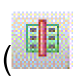
The *Workspaces* submenu contains the following menu items:

- Physical
- Amoeba
- Floorplan
- Design Browser + Physical
- Violation Browser + Physical
- Save Workspace
- Delete
- Set Default

Physical

Use the *Physical* menu item to switch to the Physical view of your current workspace. The Physical view displays the detailed placements of the module's blocks, standard cells, nets, and interconnects. You can move standard cells, blocks, and power and ground objects in this view as well as the Floorplan view.

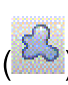
- Choose *Windows* - *Workspaces* - *Physical*.

This is equivalent to selecting the Physical view widget ()on the toolbar.

Amoeba

Use the *Amoeba* menu item to switch to the Amoeba design view of your current workspace. The Amoeba view displays the outline of the modules and submodules after placement, showing physical locality of the module.

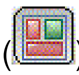
- Choose *Windows* - *Workspaces* - *Amoeba*.

This is equivalent to selecting the Amoeba view widget ()on the toolbar.

Floorplan

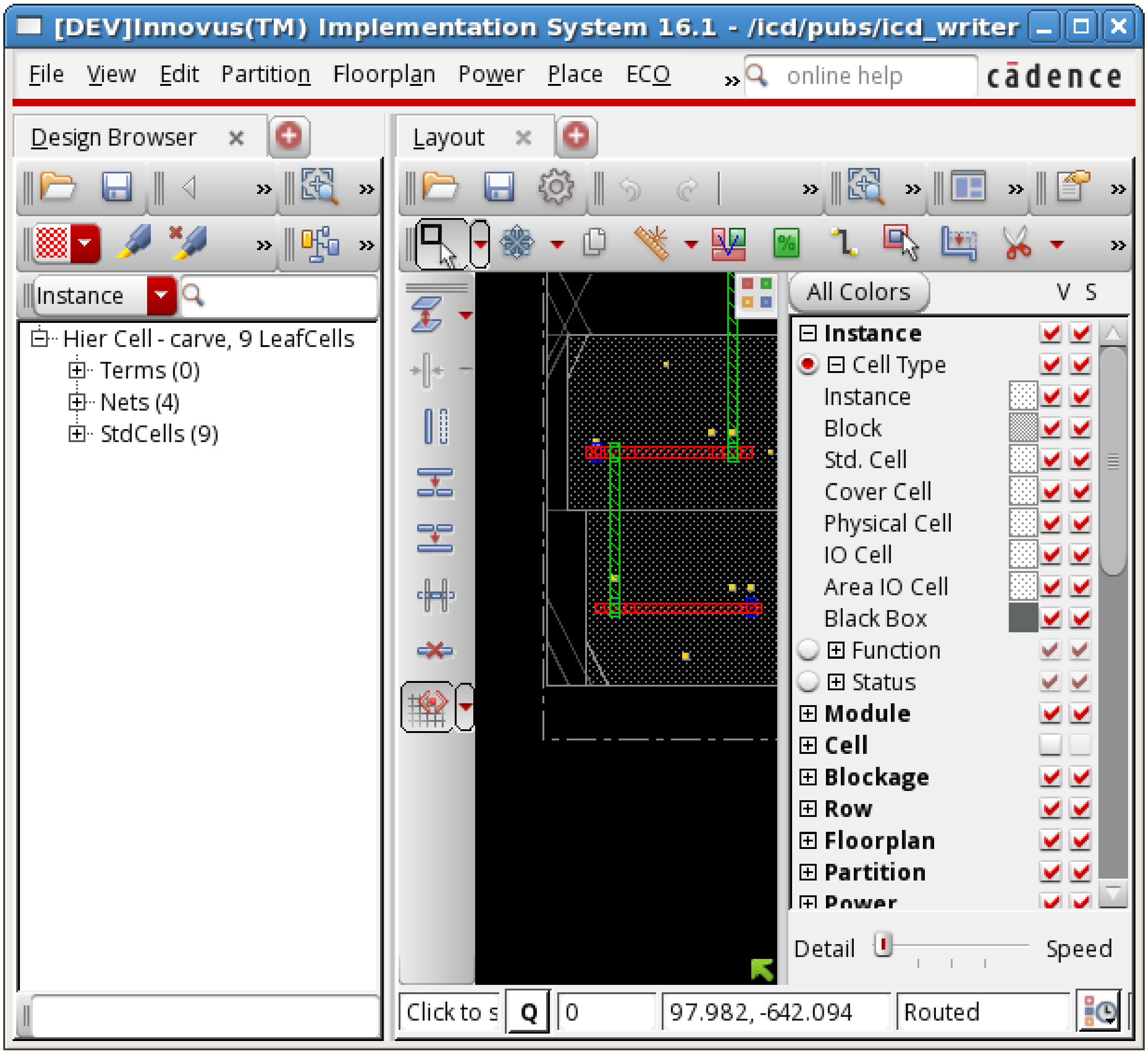
Use the *Floorplan* menu item to switch to the Floorplan view of your current workspace. The Floorplan view displays the hierarchical module and block guides, connection flight lines, and floorplan objects, including block placement, and power and ground nets.

- Choose *Windows - Workspaces - Floorplan*.

This is equivalent to selecting the Floorplan view widget ()on the toolbar.

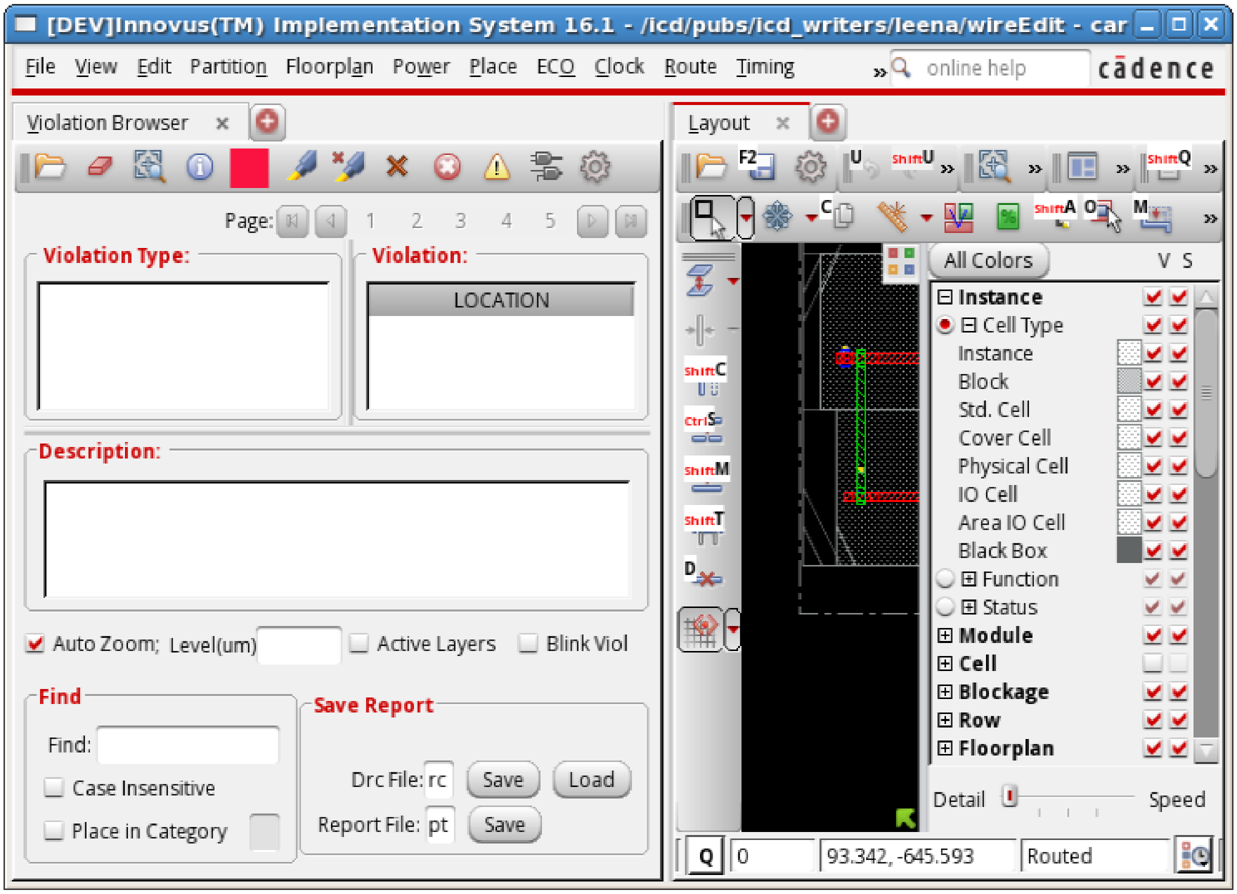
Design Browser + Physical

Use the *Design Browser + Physical* menu item to see the Design Browser and the physical view of the design, side by side.



Violation Browser + Physical

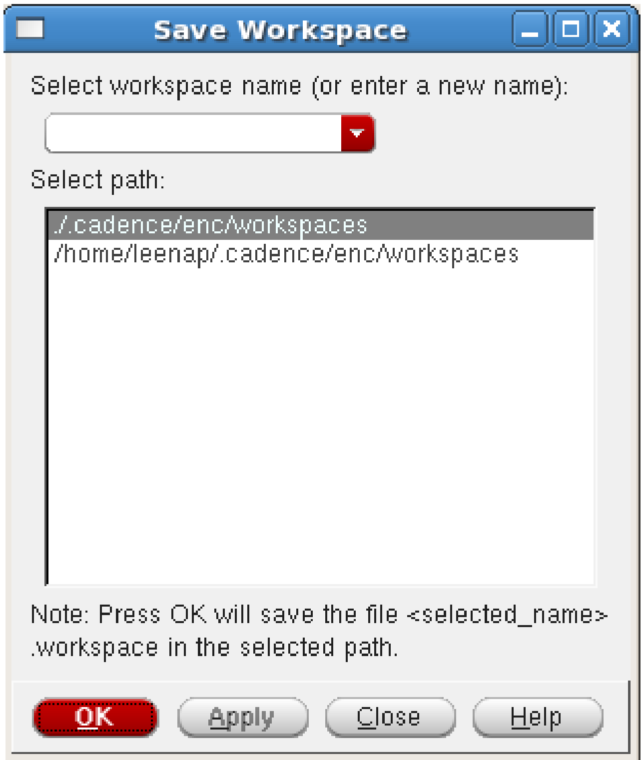
Use the *Violation Browser + Physical* menu item to see the Violation Browser and the phyiscal view of the design, side by side.



Save Workspace

Use the Save Workspace form to save your workspace to a specific directory. You can then load the workspace whenever you want from the specified directory.

- Choose *Windows - Workspaces - Save Workspace*.



Save Workspace Fields and Options

Select workspace name (or enter a new name)	Specifies the name of the workspace you are saving. You can type a new name or, if you have previously saved workspaces, choose an existing name from the drop-down list. The drop-down lists all the workspaces in the selected path.
Select Path	Specifies the location for saving the workspace. You can choose to save the workspace in the current working directory or your home directory. If the workspace is saved to the current directory, it is applied to the current design only. If the workspace is saved to your home directory, it is applicable for all designs. *Default*: Current working directory

After you have saved a workspace, the saved workspace name appears on the *Workspaces* submenu. Whenever you want to load a workspace, simply click the saved workspace name in the *Workspaces* submenu.

If there are multiple workspaces, the one set as default is loaded automatically. If you have not set any workspace as default, the one that you saved last is loaded automatically. You can then switch to another workspace by selecting the corresponding check box in the *Workspaces* submenu.

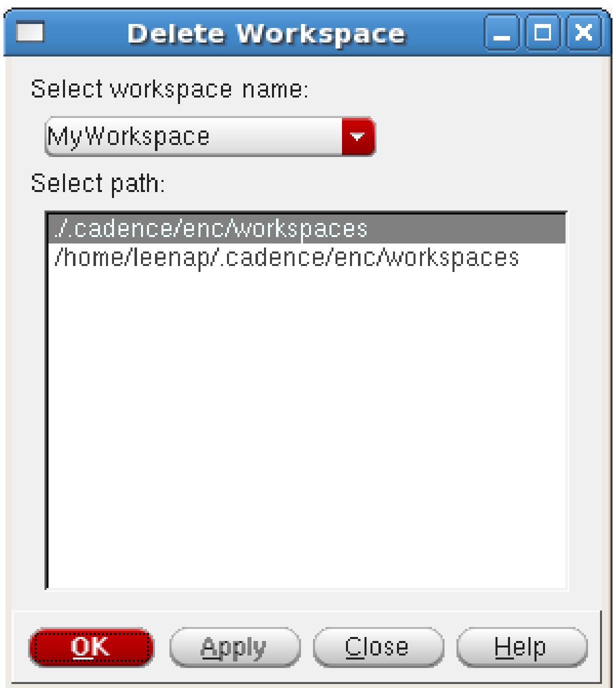
Related Text Commands

- `saveWorkspace`
- `loadWorkspace`

Delete

Use the *Delete Workspace* form to delete the selected workspace.

- Choose *Windows - Workspaces - Delete*.



Delete Workspace Fields and Options

Select workspace name	Specifies the name of the workspace you are deleting. The drop-down lists all the workspaces in the selected path.
Select Path	Specifies the location of the workspace. *Default*: Current working directory

Related Text Commands

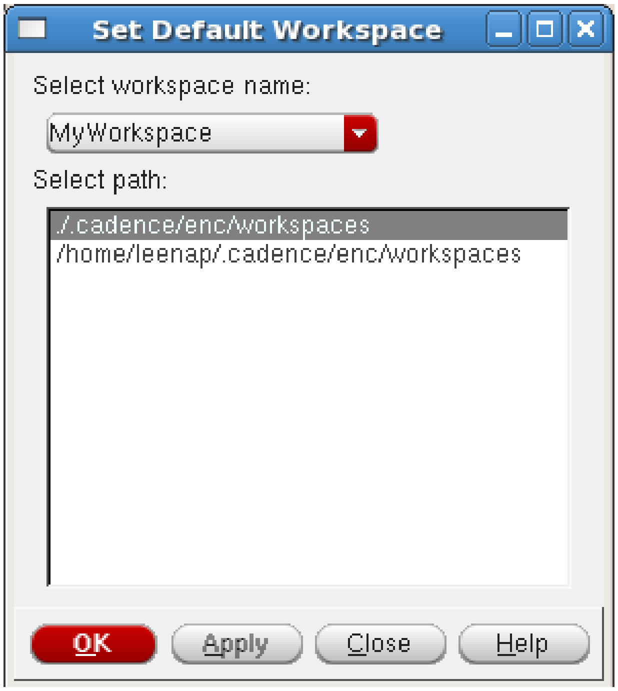
- `deleteWorkspace`

Set Default

Use the Set Default Workspace form to set the selected workspace as default.

- Choose *Windows - Workspaces - Set Default*.

The default workspace is loaded automatically when starting up the software. So if you want Innovus to load a workspace automatically, you need to first save it as default.



Set Default Workspace Fields and Options

Select workspace name	Specifies the name of the workspace you are setting as default. The drop-down lists all the workspaces in the selected path.
Select Path	Specifies the location of the workspace. *Default*: Current working directory

Related Text Commands

- `setDefaultWorkspace`

Menus

Use the *Menus* submenu to show or hide specific menus, as required.

Toolbars

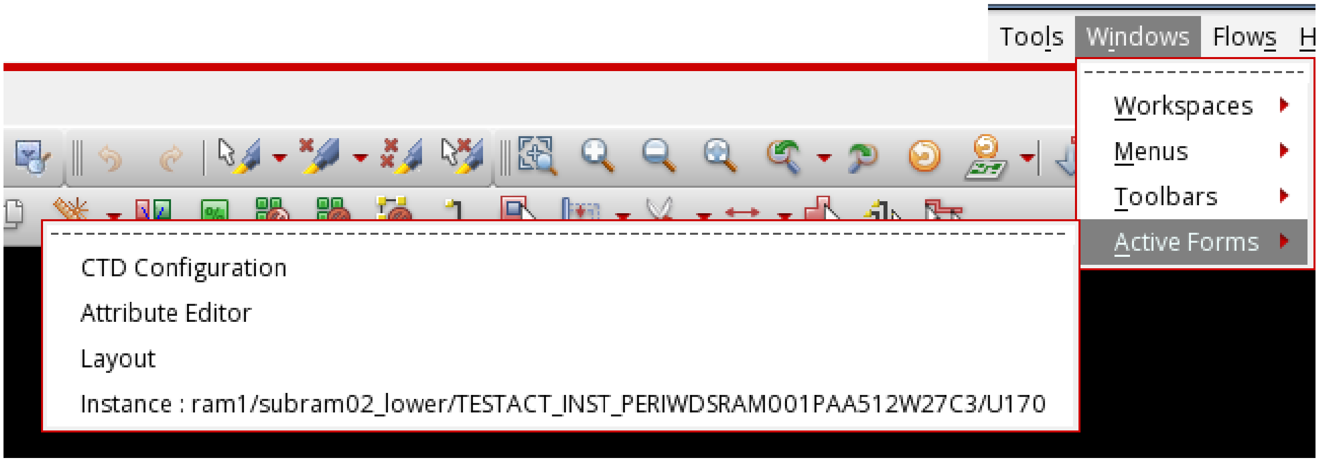
Use the *Toolbars - Layout* submenu to show or hide specific toolbars, as required.

- *File* - Controls the display of widgets related to the File menu in the Toolbar Widget area above the design display area. See Toolbar Widgets for more information.
- *Edit* - Controls the display of widgets related to the Edit menu in the Toolbar Widget area above the design display area. See Toolbar Widgets for more information.
- *View* - Controls the display of widgets related to the View menu in the Toolbar Widget area above the design display area. See Toolbar Widgets for more information.
- *Tools* - Controls the display of widgets related to the Tools menu in the Toolbar Widget area above the design display area. See Toolbar Widgets for more information.
- *Report* - Controls the display of widgets related to the *File - Report* submenu in the Toolbar Widget area above the design display area.
- *Tool box* - Controls the tool widget display above the design display area. See Tool Widgets for more information.
- *Wire Edit* - Controls the display of the Wire Edit toolbar. See Wire Edit Toolbar for more information.
- *Select Bar* - Controls the display of the *Select Bar* in the main window. This toolbar is turned off by default. See Select Bar for more information

Note: To save toolbars selected or deselected in the *Toolbars - Layout* submenu, you can save it to the `enc.pref.tcl` file from the *Preferences - Windows* form. See Preferences - Windows for more information.

Active Forms

Use the *Active Forms* submenu to switch between forms quickly. The *Active Forms* submenu lists all open windows associated with the current session as shown below:



This makes it easier for you to check currently open windows and switch between them. Simply click on the required window title in the *Active Forms* submenu to bring it to the front.

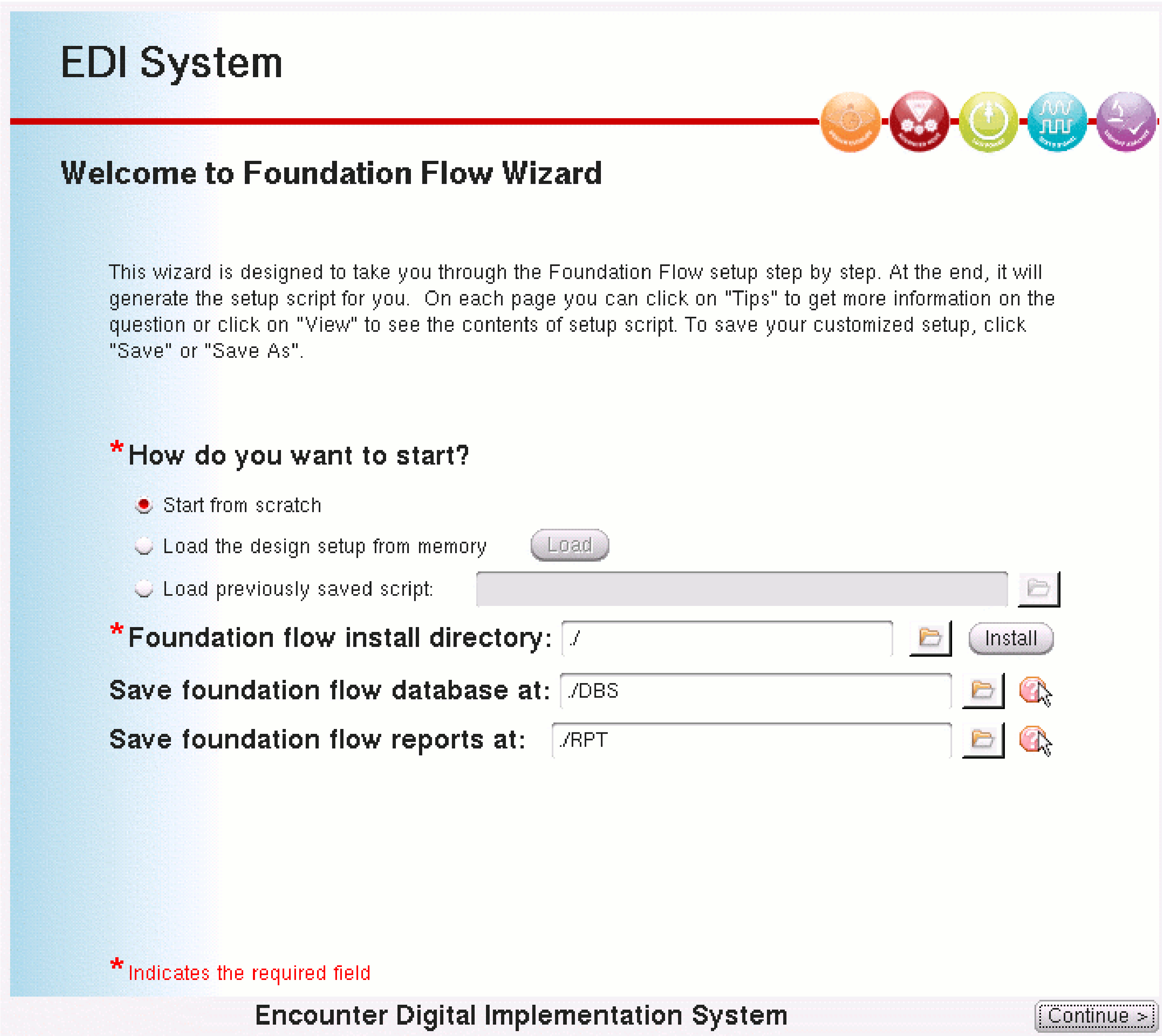
18

Flows Menu

- Foundation Flow Wizard
- Create Foundation Flow Template
- Foundation Flow Demo
- Foundation Flow Documentation

Foundation Flow Wizard

The first option leads you to the Foundation Flow Wizard. Click *Foundation Flow Wizard* to run the Wizard.



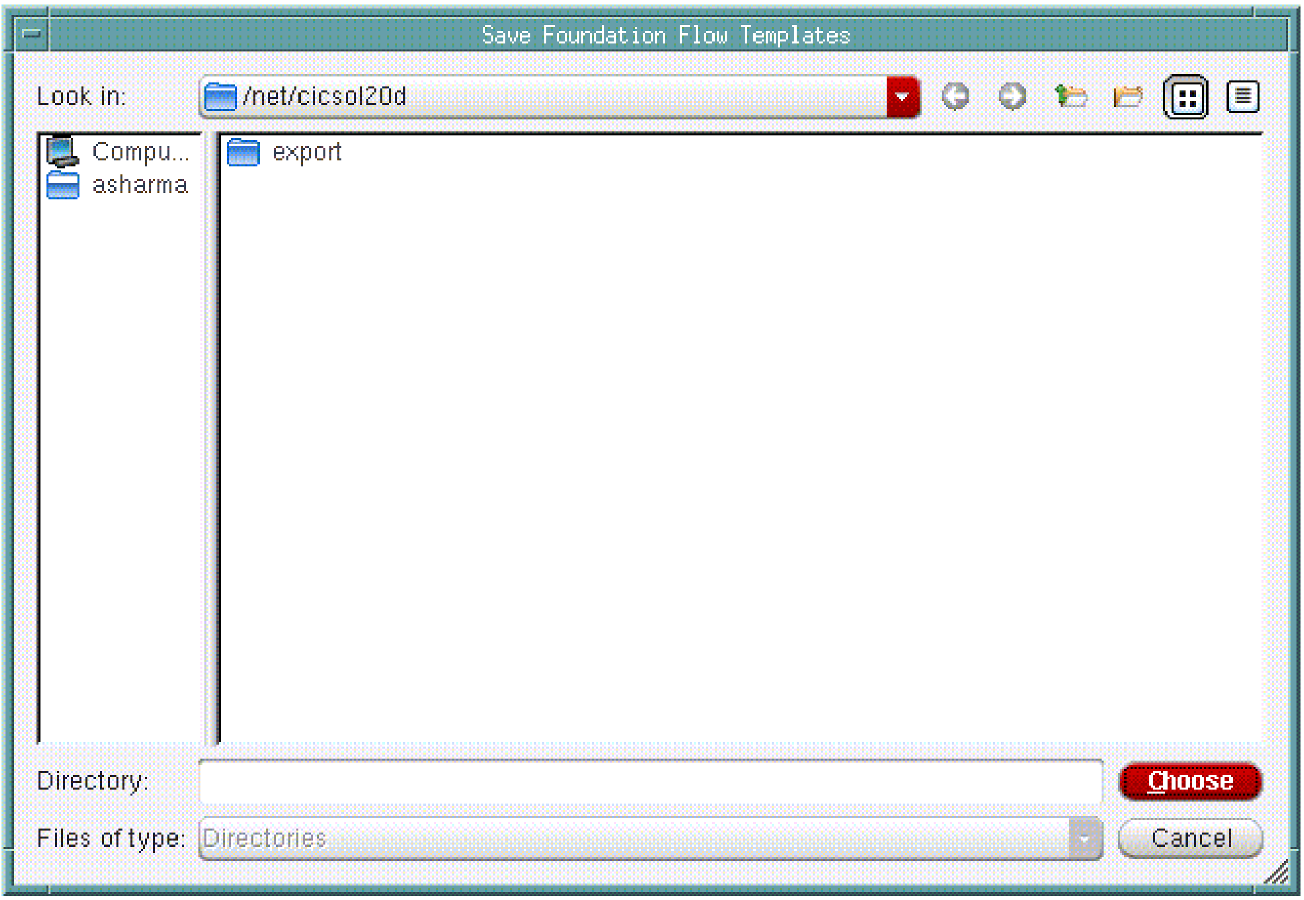
Related Topics

Innovus Foundation Flows User Guide

Create Foundation Flow Template

In Innovus, you can enable customized Foundation Flow templates.
→ *Choose Flow - Create Foundation Flow Template - Save.*

Use this menu item to save the flow templates to a specified directory. The templates consist of a set of Tcl scripts you can customize for your design and technology needs.



Related Topics

- [Innovus Foundation Flows User Guide]

Foundation Flow Demo

The tab takes you to the Foundation Flow with the following options to view the respective demos:

- Getting Started - Flat Design: This training provides an overview of Flat Implementation

Foundation Flow implementation environment. The guided demo shows how to create a foundation flow environment, create and review setup and configuration files, and run the flat implementation foundation flow. It also touches upon flow databases and results. Click the tab to see the flow.

- Hierarchical Design: This training provides an overview of the Hierarchical Foundation Fow implementation environment. You need the following additional information to run the flow: how to update the configuration files, the steps to run the hierarchical flow using the `make` file, and how to view results of all the completed steps. Click the tab to see the flow.
- Low Power Design: This training provides an overview of the scope of the CPF-based Low Power Foundation Flow Implementation environment. You need the following additional information required to run the low power flow: an understanding on how to leverage the utilities provided with the Low Power Foundation Flow, power shut-off or switch cell insertion, power domain modification and shaping, secondary power routing, domain specific tie or filler or well tap insertion, and steps to run the Low Power Foundation Flow. Click the tab to see the flow.
- Advanced Flow Usage: This training provides an understanding on how to enable some of the more common flow options, to handle: defining Pre- or Post- CTS Timing constraints, dealing with congestion issues, low power designs, difficult Timing Closure designs, extraction or signal integrity analysis, additional settings, third party correlations, and design for manufacturing requirements. Click the tab to see the flow.

Foundation Flow Documentation

The tab takes you to the Foundation Flow documentation.
→ *Choose Flow - Foundation Flow Documentation - Flat Design*

To view the Innovus Foundation Flow: Flat Implementation Flow Guide
→ *Choose Flow - Foundation Flow Documentation - Hierarchical Design*

To view the Innovus Foundation Flow: Hierarchical Implementation Flow Guide
→ *Choose Flow - Foundation Flow Documentation - Low Power*

To view the Innovus Foundation Flow: CPF-based Low Power Implementation Flow Guide
→ *Choose Flow - Foundation Flow Documentation - Template User Guide*

To view the Innovus Foundation Flows User Guide