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TECHNOLOGY 28FDSOI
- PEX MODELS -
Manual for StarRC

Version 2.4
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ABSTRACT

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The intent of this document is to provide information about the starRC module PEX_models_28fd@2.4 release.

StarRC PEX MODELS release are aligned with DRM CMOS028FDSOI rev0.4.7

These models have been generated and validated with starRC release n-2017.12-sp3-1.

1. Manual

1.1. Post Layout Extraction

The Post layout extraction flow is aimed to provide spice transistor flat netlist back annotated with parasitic C's and R's extracted on interconnections. This flow is based on Calibre-StarRCXT tools.

RCmodels represent the analytical models used on the fly by starRCXT to compute the resistances and capacitances. RCmodels computation is based on the interconnect stack parameters described in the DRM.

1.2. Supported Corner

The table below summarizes the supported corner for backend of line.

Name	Definition		Metal Thick.	Metal width	Via Thick.	Via Res.
nominal	**typical** values for all C's and R's	Process target	typ	typ	typ	typ
FuncCmin	**best C's,** worst R_{wire} and best R_{via}	3σ on input parameter	min	min	max	min
SigCmin		3σ on output RC				
FuncCmax	**worst C's**, best R_{wire} and worst R_{via}	3σ on input parameter	max	max	min	max
SigCmax		3σ on output RC				
FuncRCmin	**best R's** and worst lateral C	3σ on input parameter	max	max	max	min
SigRCmin		3σ on output RC				
FuncRCmax	**worst R's** and best lateral C	3σ on input parameter	min	min	min	max
SigRCmax		3σ on output RC				

The table below summarizes the corner definition for MIM.

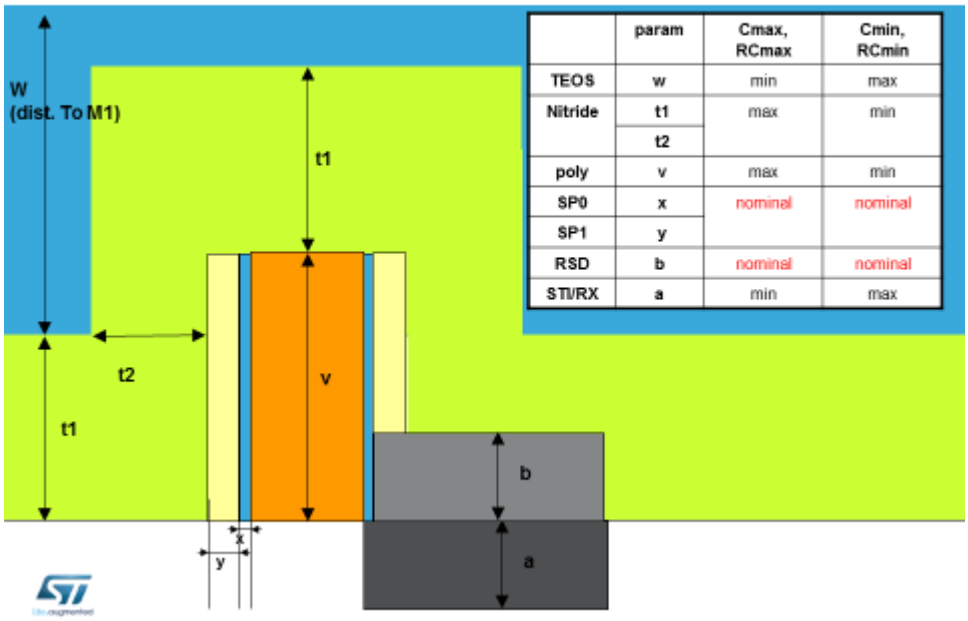
MIM corner definition

	Cmin	RCmin	Cmax	RCmax
Metal thickness (BOT/TOPMIM)	min	max	max	min
Mim dielectric thickness	max	max	min	min
Metal RSH	min	max	max	min
Via R	min	min	max	max
Rmim (Via+Line)	min	~	max	~
Cmim	min	min	max	max

- No Sigma variation on MIM

The illustration below summarizes the FEOL corner definition. There is no sigma variation for FEOL (for ex : SigCmax = FuncCmax).

FEOL corner definition



	param	Cmax, RCmax	Cmin, RCmin
TEOS	w	min	max
Nitride	t1	max	min
	t2		
poly	v	max	min
SP0	x	nominal	nominal
SP1	y		
RSD	b	nominal	nominal
STI/RX	a	min	max

1.3. Gate to contact computation

The gate to contact spacing is computed by the formula:

SiliconPC2CA=($Drawn\ \ PC2CA\ -global\ \ PCcompensation+MOS\ \ flavor\ PCcompensation\ -specific\ PC\ compensation)*0.9$

1.4. FEOL description

Due to itf limitation, following assumptions on FEOL description have been made:

- No stair epitaxy description
- Square contact
- No epitaxy growth in W direction
- No CESL faceting
- No CA enclosure in epitaxy
- No conformal gate oxide