C28SOI_SC_12_CORE_LL

Release Notes and Known Problems and Solutions

12 track Standard Cell Library comprising commonly used booleans and sequential cells

1 Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library name	C28SOI_SC_12_CORE_LL
Library version	5.1
Library type	Standard Cells
Technology	CMOS028_FDSOI

1.2 Related Documentation

- StandardCell_Notes.pdf Present in Design Package
- User Manual C28SOI_SC_12_CORE_LL_um.pdf present in doc directory of Product itself.
- Datasheets C28SOI_SC_12_CORE_LL_*_ds.pdf present in doc directory of Product itself.

2 Release Details

2.1 Current Release Details, Version 5.1

- Cells have been re-characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.
- Verilog Model for below cells have been updated to enable proper checking of E-CP timing checks.

C12T28SOI_LL_DFPHQNX17_P*	C12T28SOI_LL_DFPHQNX33_P*
C12T28SOI_LL_DFPHQNX8_P*	C12T28SOI_LL_DFPHQX17_P*
C12T28SOI_LL_DFPHQX33_P*	C12T28SOI_LL_DFPHQX8_P*
C12T28SOI_LL_SDFPHRQNX17_P*	C12T28SOI_LL_SDFPHRQNX33_P*
C12T28SOI_LL_SDFPHRQNX8_P*	C12T28SOI_LL_SDFPHRQX17_P*
C12T28SOI_LL_SDFPHRQX33_P*	C12T28SOI_LL_SDFPHRQX8_P*
C12T28SOI_LLHF_SDFPHRQNX4_P*	C12T28SOI_LLHF_SDFPHRQX4_P*

- To enable support for Cadence Voltus Flow, CCS-Power has been added.
- Characterization corners have been re-defined in-line with DP Specifications.
- The product is aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.

2.2 Version 5.0

- Dummy Poly in layout across various cells has been cut for DFM robustness.
- Total 48 cells have been updated for Robustness relative to contact punch through effect. Minimum Enclosure of 20nm for RX/CA has been ensured. There is no change in Cell Area and Abstract because of contact robustness update.
  - Updated cells are-

C12T28SOI_LL_AND2X25_P0	C12T28SOI_LL_AND3X25_P0
C12T28SOI_LL_AND4X27_P0	C12T28SOI_LL_AND4X4_P0
C12T28SOI_LL_AO112X8_P0	C12T28SOI_LL_AOI13X38_P0
C12T28SOI_LL_AOI211X17_P0	C12T28SOI_LL_BFX29_P0
C12T28SOI_LL_BFX33_P0	C12T28SOI_LLBR0P6_NAND3X12_P0
C12T28SOI_LL_CB4I1X17_P0	C12T28SOI_LL_DFPQNX30_P0
C12T28SOI_LL_DFPQX17_P0	C12T28SOI_LL_DFPQX30_P0
C12T28SOI_LL_DFPQX33_P0	C12T28SOI_LL_DFPRQNX17_P0
C12T28SOI_LL_DFPRQNX30_P0	C12T28SOI_LL_DFPRQX17_P0
C12T28SOI_LL_DFPRQX30_P0	C12T28SOI_LL_DFPSQX30_P0
C12T28SOI_LLHF_SDFPRQX4_P0	C12T28SOI_LL_IVX4_P0
C12T28SOI_LL_MUX21X8_P0	C12T28SOI_LL_MUX41X8_P0
C12T28SOI_LL_MUXI21X5_P0	C12T28SOI_LL_MX41X27_P0
C12T28SOI_LL_MX41X7_P0	C12T28SOI_LL_NAND2X50_P0
C12T28SOI_LL_NAND3AX24_P0	C12T28SOI_LL_NOR2X3_P0
C12T28SOI_LL_NOR4ABX13_P0	C12T28SOI_LL_NOR4X32_P0
C12T28SOI_LL_OAI112X10_P0	C12T28SOI_LL_OAI112X21_P0
C12T28SOI_LL_OAI211X10_P0	C12T28SOI_LL_OAI211X21_P0
C12T28SOI_LL_OAI222X9_P0	C12T28SOI_LL_OAI22X10_P0

C12T28SOI_LL_OAI22X15_P0	C12T28SOI_LL_OR2ABX16_P0
C12T28SOI_LL_OR2ABX24_P0	C12T28SOI_LL_OR2X8_P0
C12T28SOI_LLS1_FA1X8_P0	C12T28SOI_LL_SDFPRQNTX17_P0
C12T28SOI_LL_SDFPRQNTX33_P0	C12T28SOI_LL_SDFPRQNTX8_P0
C12T28SOI_LL_SDFPRQTX17_P0	C12T28SOI_LLS_NOR2X34_P0

- Cells has been characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.
- The product has been aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Global Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.3 Version 4.0

- Total 37 cells have been added to further enrich the offer.
  - Cells addition for better drive granularity.

C12T28SOI_LL_BFX13_P0	C12T28SOI_LL_BFX21_P0
C12T28SOI_LL_BFX29_P0	C12T28SOI_LL_BFX58_P0
C12T28SOI_LL_BFX6_P0	C12T28SOI_LL_BFX75_P0
C12T28SOI_LL_BFX84_P0	C12T28SOI_LL_IVX13_P0
C12T28SOI_LL_IVX21_P0	C12T28SOI_LL_IVX29_P0
C12T28SOI_LL_IVX75_P0	C12T28SOI_LL_IVX84_P0
C12T28SOI_LL_NAND2X10_P0	C12T28SOI_LL_NAND2X17_P0
C12T28SOI_LL_NAND2X24_P0	C12T28SOI_LL_NAND2X47_P0
C12T28SOI_LL_NAND2X58_P0	C12T28SOI_LL_NAND2X5_P0
C12T28SOI_LL_NAND2X67_P0	C12T28SOI_LL_NAND3X15_P0
C12T28SOI_LL_NAND3X21_P0	C12T28SOI_LL_NAND3X4_P0
C12T28SOI_LL_NAND3X9_P0	C12T28SOI_LL_NOR2X10_P0
C12T28SOI_LL_NOR2X17_P0	C12T28SOI_LL_NOR2X24_P0
C12T28SOI_LL_NOR2X5_P0	C12T28SOI_LL_NOR3X16_P0
C12T28SOI_LL_NOR3X22_P0	C12T28SOI_LL_NOR3X4_P0
C12T28SOI_LL_NOR3X9_P0	

  - Addition of new functionality: Set-Reset Flip Flops

C12T28SOI_LL_SDFPRSQNTX17_P0	C12T28SOI_LL_SDFPRSQNTX33_P0
C12T28SOI_LL_SDFPRSQNTX8_P0	C12T28SOI_LL_SDFPRSQTX17_P0
C12T28SOI_LL_SDFPRSQTX33_P0	C12T28SOI_LL_SDFPRSQTX8_P0

- The product has been aligned to DP28FDSOI 2.4 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.

- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.4 Version 3.0

- The product has been aligned to DP28FDSOI 2.3 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.5 Version 2.2

- Continued with Previous release, Further 51 cells has been updated to have better manufacturability. Abstract is changed for all these cells. But there is no Impact on Cell Area. Updated Cells are -

C12T28SOI_LLBR0P6_NAND3X35_P0	C12T28SOI_LLHF_SDFPHRQNX4_P0
C12T28SOI_LLHF_SDFPHRQX4_P0	C12T28SOI_LLHF_SDFPQX4_P0
C12T28SOI_LLHF_SDFPRQTX4_P0	C12T28SOI_LLHF_SDFPSQNTX4_P0
C12T28SOI_LLHF_SDFPSQTX4_P0	C12T28SOI_LLHF_SDFPSQX4_P0
C12T28SOI_LL_MUX21X8_P0	C12T28SOI_LL_NOR3AX13_P0
C12T28SOI_LL_NOR3AX25_P0	C12T28SOI_LLS1_FA1X33_P0
C12T28SOI_LL_SDFPHRQNX17_P0	C12T28SOI_LL_SDFPHRQNX33_P0
C12T28SOI_LL_SDFPHRQNX8_P0	C12T28SOI_LL_SDFPHRQX17_P0
C12T28SOI_LL_SDFPHRQX33_P0	C12T28SOI_LL_SDFPHRQX8_P0
C12T28SOI_LL_SDFPQNX17_P0	C12T28SOI_LL_SDFPQNX33_P0
C12T28SOI_LL_SDFPQTX17_P0	C12T28SOI_LL_SDFPQTX33_P0
C12T28SOI_LL_SDFPQX17_P0	C12T28SOI_LL_SDFPQX33_P0
C12T28SOI_LL_SDFPQX8_P0	C12T28SOI_LL_SDFPRQNTX17_P0
C12T28SOI_LL_SDFPRQNTX33_P0	C12T28SOI_LL_SDFPRQNTX8_P0
C12T28SOI_LL_SDFPRQNX17_P0	C12T28SOI_LL_SDFPRQNX33_P0
C12T28SOI_LL_SDFPRQTX17_P0	C12T28SOI_LL_SDFPRQTX33_P0
C12T28SOI_LL_SDFPRQTX8_P0	C12T28SOI_LL_SDFPRQX17_P0
C12T28SOI_LL_SDFPRQX33_P0	C12T28SOI_LL_SDFPRQX8_P0
C12T28SOI_LL_SDFPSQNTX17_P0	C12T28SOI_LL_SDFPSQNTX33_P0
C12T28SOI_LL_SDFPSQNTX8_P0	C12T28SOI_LL_SDFPSQNX17_P0
C12T28SOI_LL_SDFPSQNX25_P0	C12T28SOI_LL_SDFPSQNX33_P0
C12T28SOI_LL_SDFPSQNX8_P0	C12T28SOI_LL_SDFPSQTX17_P0
C12T28SOI_LL_SDFPSQTX33_P0	C12T28SOI_LL_SDFPSQTX8_P0
C12T28SOI_LL_SDFPSQX17_P0	C12T28SOI_LL_SDFPSQX25_P0
C12T28SOI_LL_SDFPSQX33_P0	C12T28SOI_LL_SDFPSQX8_P0
C12T28SOI_LLS_XOR3X4_P0	

- There is minimal impact on cell's Performance for these Updated Cells. Therefore Library has not be re-characterized for these updated cells. Timing/Power Data is same as of Previous Release.
- The Product remains aligned to DP28FDSOI_7ML 1.0.

2.6 Version 2.1

- Total 19 cells has been re-designed to have better manufacturability. Abstract is changed
- for all these cells. Updated Cells are -

C12T28SOI_LL_SDFPQNTX8_P0	C12T28SOI_LL_SDFPQNTX33_P0
C12T28SOI_LL_SDFPQNTX17_P0	C12T28SOI_LL_NOR2X40_P0
C12T28SOI_LL_MUXI21X21_P0	C12T28SOI_LL_DFPQNX17_P0
C12T28SOI_LLS_XNOR3X4_P0	C12T28SOI_LLHF_SDFPHRQNX4_P0
C12T28SOI_LLHF_SDFPHRQX4_P0	C12T28SOI_LLHF_SDFPQNTX4_P0
C12T28SOI_LLHF_SDFPQNX4_P0	C12T28SOI_LLHF_SDFPQTX4_P0
C12T28SOI_LLHF_SDFPQX4_P0	C12T28SOI_LLHF_SDFPRQNTX4_P0
C12T28SOI_LLHF_SDFPRQNX4_P0	C12T28SOI_LLHF_SDFPRQX4_P0
C12T28SOI_LLHF_SDFPSQNX4_P0	C12T28SOI_LLHF_SDFPSQX4_P0
C12T28SOI_LL_DFPQX33_P0	

- Out of these total 19 cells, there is one cell for which Cell Area is also Impacted. Cell is -
  - C12T28SOI_LL_DFPQX33_P0
- Library has been re-characterized only for these updated cells and all views has been updated accordingly.
- The Product remains aligned to DP28FDSOI_7ML 1.0.

2.7 Version 2.0

- The Product is aligned to DP28FDSOI_7ML 1.0. Refer to Design Package Documents for more details.
- For Standard Cell Library Specific Features, Refer to StandardCell_Notes.pdf Present in Design Package.

3 Known Problems and Solutions

3.1 DP related Generic Problems

- For Generic Standard cell Library related problem for this DP, please refer to KPS section inside StandardCell_Notes.pdf Present in Design Package.

3.2 Placement Restriction

➥ Specific Placement restriction due to Poly Landing pad

☞ Placement restriction has been modelled in CADENCE LEF - through “Symmetry property” and in SYNOPSYS FRAM - through “spacing_label property” for the following cells:

- C12T28SOI_LL_IVX4_P0
- C12T28SOI_LL_IVX6_P0
- C12T28SOI_LL_IVX8_P0

	*As mentioned above, modelling the placement constraint is different between Synopsys and Cadence. Therefore Need to be careful, if You do P&R with Synopsys and then go inside Cadence, the placement created by ICC could be declared as invalid by Encounter tool.*

4 Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.

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