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C28SOI_SC_12_COREPBP4_LR Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 4 nm

Overview

- C28SOI_SC_12_COREPBP4_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

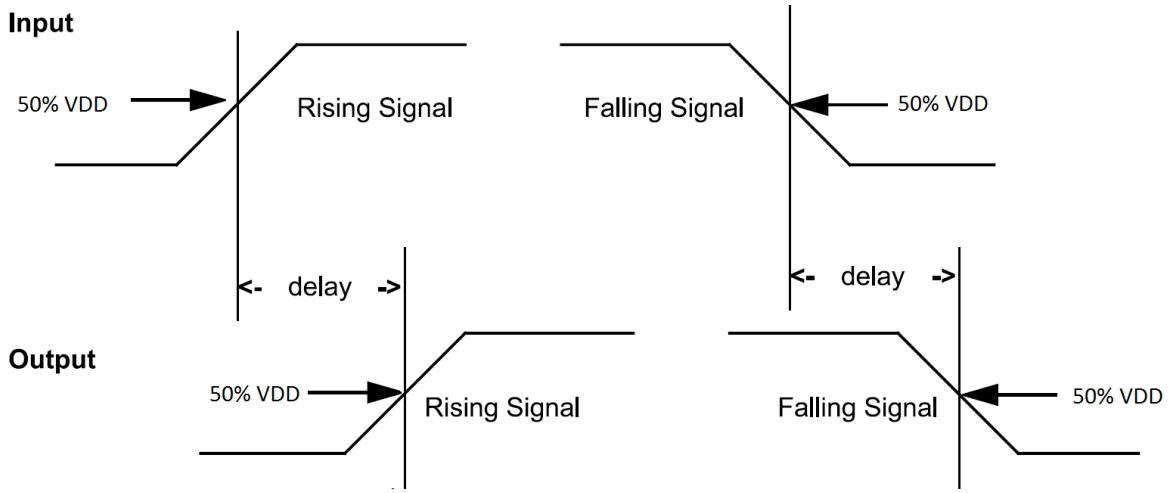


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

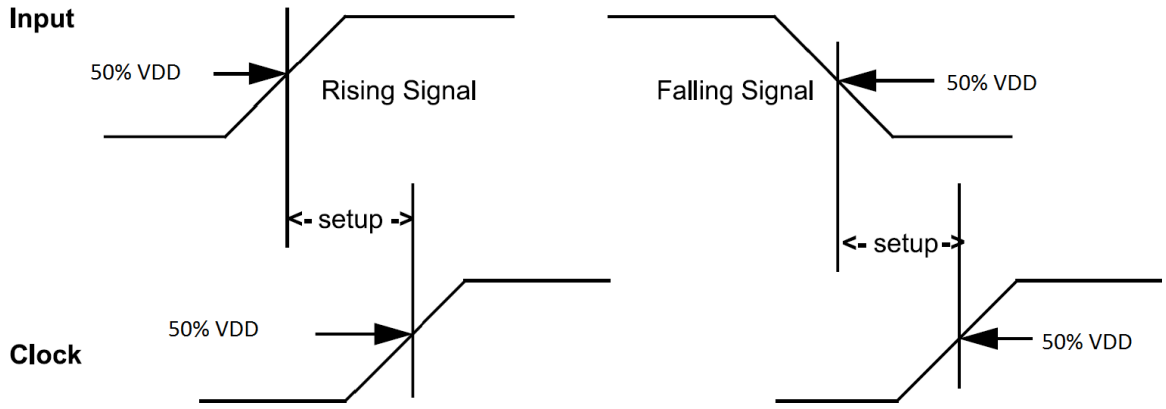


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

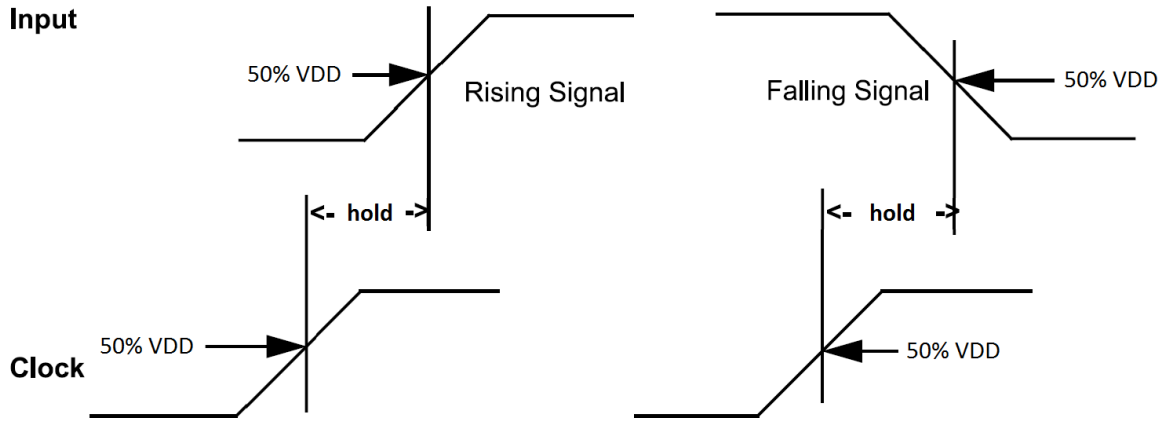


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

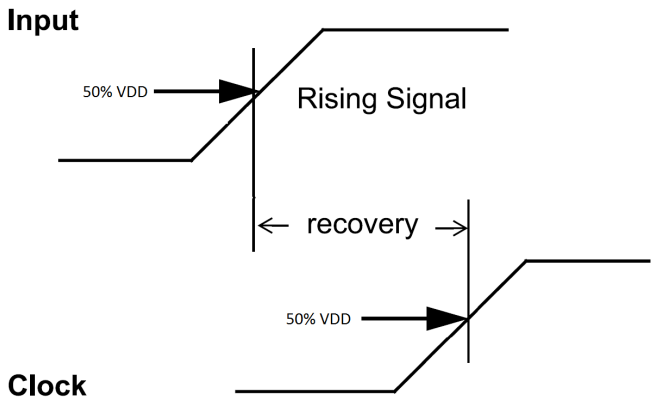


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

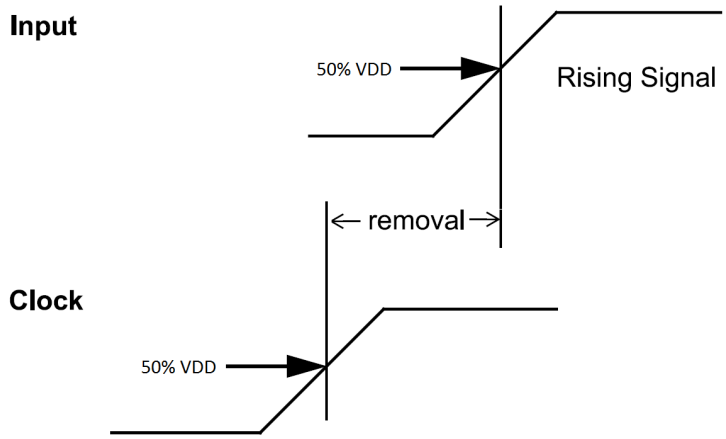


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

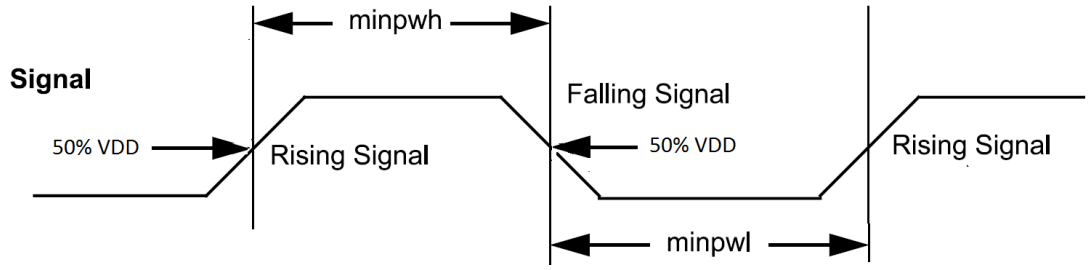


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

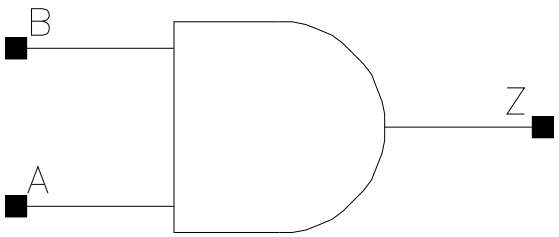
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X25_P4	1.200	1.088	1.3056
X33_P4	1.200	1.360	1.6320
X42_P4	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0007	0.0011	0.0016	0.0020
B	0.0006	0.0010	0.0015	0.0020
	X42_P4			
A	0.0019			
B	0.0019			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0354	0.0300	1.8364	0.9323
A to Z ↑	0.0270	0.0253	3.3967	1.6412
B to Z ↓	0.0338	0.0285	1.8371	0.9311
B to Z ↑	0.0281	0.0261	3.3942	1.6415
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0306	0.0298	0.6190	0.4606

A to Z ↑	0.0249	0.0256	1.0857	0.8191
B to Z ↓	0.0293	0.0277	0.6198	0.4597
B to Z ↑	0.0257	0.0257	1.0857	0.8199
	X42_P4		**X42_P4**	
A to Z ↓	0.0319		0.3745	
A to Z ↑	0.0275		0.6554	
B to Z ↓	0.0298		0.3746	
B to Z ↑	0.0279		0.6562	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	1.393e-07	1.771e-12
X16_P4	2.601e-07	2.023e-12
X25_P4	3.828e-07	2.779e-12
X33_P4	5.186e-07	3.282e-12
X42_P4	5.870e-07	3.539e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	1.415e-05	2.603e-05	4.012e-05	7.463e-05
B (output stable)	4.340e-05	7.990e-05	1.257e-04	3.983e-04
A to Z	2.286e-03	3.748e-03	5.758e-03	7.536e-03
B to Z	2.151e-03	3.507e-03	5.384e-03	6.785e-03
	X42_P4			
A (output stable)	7.445e-05			
B (output stable)	4.006e-04			
A to Z	8.990e-03			
B to Z	8.220e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

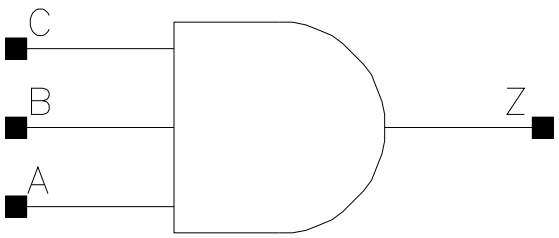
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	6.780e-08	3.548e-08	1.640e-08	-1.450e-08
B (output stable)	5.580e-08	2.211e-08	-2.480e-08	-3.350e-08
A to Z	-2.032e-07	7.920e-08	-5.786e-07	-1.958e-07
B to Z	-3.109e-07	-1.471e-07	1.219e-07	-5.142e-07
	X42_P4			
A (output stable)	-1.230e-08			
B (output stable)	-3.210e-08			
A to Z	-6.190e-08			
B to Z	-5.140e-07			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X25_P4	1.200	1.360	1.6320
X33_P4	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0007	0.0010	0.0017	0.0020
B	0.0006	0.0010	0.0015	0.0019
C	0.0006	0.0010	0.0014	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0382	0.0327	1.8593	0.9094
A to Z ↑	0.0344	0.0320	3.4154	1.6229
B to Z ↓	0.0370	0.0314	1.8602	0.9083
B to Z ↑	0.0351	0.0327	3.4166	1.6236
C to Z ↓	0.0356	0.0299	1.8576	0.9074
C to Z ↑	0.0357	0.0326	3.4164	1.6262
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0325	0.0312	0.6265	0.4678

A to Z ↑	0.0313	0.0301	1.1105	0.8324
B to Z ↓	0.0313	0.0299	0.6259	0.4675
B to Z ↑	0.0321	0.0309	1.1121	0.8332
C to Z ↓	0.0298	0.0285	0.6261	0.4677
C to Z ↑	0.0322	0.0311	1.1111	0.8331

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	1.281e-07	2.024e-12
X17_P4	2.502e-07	2.276e-12
X25_P4	3.650e-07	3.284e-12
X33_P4	4.840e-07	3.535e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	8.128e-06	1.420e-05	1.931e-05	2.551e-05
B (output stable)	3.597e-05	6.918e-05	1.005e-04	1.342e-04
C (output stable)	3.121e-05	5.276e-05	8.076e-05	1.051e-04
A to Z	2.522e-03	4.337e-03	6.267e-03	8.009e-03
B to Z	2.388e-03	4.102e-03	5.912e-03	7.537e-03
C to Z	2.276e-03	3.854e-03	5.548e-03	7.038e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

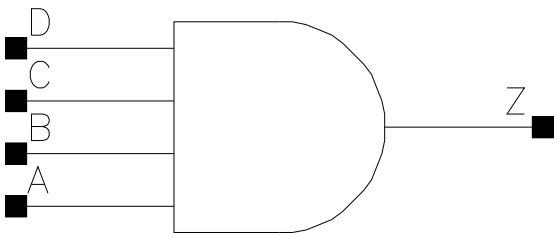
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	6.939e-08	3.316e-08	1.287e-08	-1.670e-08
B (output stable)	7.489e-08	2.146e-08	-2.373e-08	-5.133e-08
C (output stable)	6.837e-08	-1.451e-08	-5.510e-08	-1.028e-07
A to Z	-4.113e-07	3.470e-08	-4.410e-07	-5.269e-07
B to Z	-1.175e-07	-2.606e-07	-4.640e-07	-6.637e-07
C to Z	-3.042e-07	-1.665e-07	-2.692e-07	-2.359e-07

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X6_P4	1.200	1.088	1.3056
X20_P4	1.200	2.312	2.7744
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P4	X6_P4	X20_P4	X27_P4
A	0.0005	0.0008	0.0017	0.0019
B	0.0005	0.0007	0.0017	0.0019
C	0.0005	0.0008	0.0017	0.0019
D	0.0005	0.0007	0.0017	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X6_P4	X4_P4	X6_P4
A to Z ↓	0.0403	0.0344	3.4310	2.2358
A to Z ↑	0.0383	0.0298	12.7764	6.9121
B to Z ↓	0.0391	0.0325	3.4323	2.2347
B to Z ↑	0.0396	0.0304	12.7861	6.9136
C to Z ↓	0.0416	0.0367	3.3980	2.2493
C to Z ↑	0.0371	0.0287	12.7920	6.9266

D to Z ↓	0.0405	0.0344	3.4007	2.2503
D to Z ↑	0.0391	0.0294	12.7995	6.9285
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0331	0.0314	0.6571	0.4654
A to Z ↑	0.0302	0.0337	2.3060	1.7531
B to Z ↓	0.0306	0.0293	0.6565	0.4649
B to Z ↑	0.0302	0.0339	2.3069	1.7532
C to Z ↓	0.0326	0.0306	0.6629	0.4679
C to Z ↑	0.0265	0.0288	2.3088	1.7539
D to Z ↓	0.0297	0.0286	0.6622	0.4682
D to Z ↑	0.0262	0.0290	2.3095	1.7539

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	1.248e-07	2.780e-12
X6_P4	2.272e-07	2.780e-12
X20_P4	6.384e-07	5.050e-12
X27_P4	7.670e-07	5.554e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	4.315e-04	6.564e-04	1.931e-03	2.424e-03
B (output stable)	3.987e-04	5.895e-04	1.662e-03	2.116e-03
C (output stable)	4.104e-04	6.610e-04	1.647e-03	2.058e-03
D (output stable)	3.799e-04	5.882e-04	1.392e-03	1.733e-03
A to Z	1.731e-03	2.638e-03	7.785e-03	1.014e-02
B to Z	1.646e-03	2.467e-03	7.096e-03	9.417e-03
C to Z	1.680e-03	2.638e-03	6.556e-03	8.237e-03
D to Z	1.597e-03	2.455e-03	5.816e-03	7.497e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

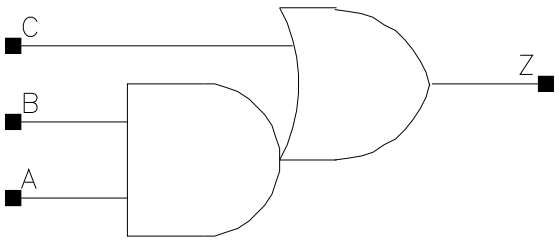
Pin Cycle (vdds)	X4_P4	X6_P4	X20_P4	X27_P4
A (output stable)	-4.634e-06	-7.622e-06	-2.826e-05	-5.134e-05
B (output stable)	-3.208e-06	-5.276e-06	-1.883e-05	-3.502e-05
C (output stable)	6.231e-06	1.133e-05	3.959e-05	6.892e-05
D (output stable)	7.953e-07	2.166e-06	3.008e-06	3.897e-06
A to Z	-1.603e-06	-2.707e-06	-9.053e-06	-1.682e-05
B to Z	-1.582e-06	-2.612e-06	-9.207e-06	-1.706e-05
C to Z	-1.564e-07	-3.398e-07	-4.658e-07	-5.160e-07
D to Z	-1.591e-07	-2.184e-07	-7.523e-07	-9.457e-07

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0020
B	0.0007	0.0010	0.0018
C	0.0007	0.0011	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0458	0.0411	1.8955	0.9291
A to Z ↑	0.0278	0.0250	3.2913	1.6151
B to Z ↓	0.0426	0.0383	1.8903	0.9264
B to Z ↑	0.0292	0.0263	3.2913	1.6146
C to Z ↓	0.0458	0.0415	1.8854	0.9243
C to Z ↑	0.0252	0.0237	3.2727	1.6068
	X33_P4		**X33_P4**	
A to Z ↓	0.0412		0.4724	
A to Z ↑	0.0256		0.8146	

B to Z ↓	0.0384		0.4723	
B to Z ↑	0.0263		0.8133	
C to Z ↓	0.0415		0.4707	
C to Z ↑	0.0234		0.8101	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	1.809e-07	2.024e-12
X17_P4	3.319e-07	2.276e-12
X33_P4	6.619e-07	3.788e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	6.155e-06	1.082e-05	2.612e-05
B (output stable)	2.528e-05	3.938e-05	1.333e-04
C (output stable)	8.754e-05	1.297e-04	2.880e-04
A to Z	2.311e-03	3.889e-03	7.720e-03
B to Z	2.182e-03	3.650e-03	7.118e-03
C to Z	2.598e-03	4.402e-03	8.682e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

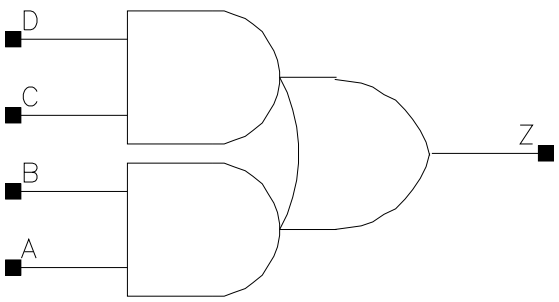
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	2.198e-06	4.808e-06	6.502e-06
B (output stable)	1.600e-05	2.651e-05	5.038e-05
C (output stable)	-1.474e-05	-1.831e-05	-3.524e-05
A to Z	-2.191e-07	-2.652e-07	-2.544e-07
B to Z	-1.246e-07	-2.098e-07	-6.912e-07
C to Z	-8.686e-06	-1.248e-05	-2.273e-05

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0019
B	0.0007	0.0010	0.0017
C	0.0006	0.0009	0.0019
D	0.0007	0.0010	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0529	0.0465	1.8282	0.9212
A to Z ↑	0.0345	0.0312	3.2461	1.6126
B to Z ↓	0.0496	0.0436	1.8230	0.9187
B to Z ↑	0.0354	0.0325	3.2449	1.6126

C to Z ↓	0.0470	0.0418	1.8233	0.9186
C to Z ↑	0.0302	0.0273	3.2357	1.6081
D to Z ↓	0.0451	0.0398	1.8195	0.9177
D to Z ↑	0.0319	0.0287	3.2384	1.6087
	X33_P4		**X33_P4**	
A to Z ↓	0.0446		0.4723	
A to Z ↑	0.0288		0.8172	
B to Z ↓	0.0425		0.4721	
B to Z ↑	0.0303		0.8168	
C to Z ↓	0.0398		0.4714	
C to Z ↑	0.0256		0.8143	
D to Z ↓	0.0377		0.4713	
D to Z ↑	0.0267		0.8145	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.026e-07	2.513e-12
X17_P4	3.736e-07	2.779e-12
X33_P4	6.982e-07	4.291e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	3.421e-05	5.281e-05	7.662e-05
B (output stable)	5.958e-05	8.763e-05	9.934e-05
C (output stable)	9.126e-06	1.804e-05	3.164e-05
D (output stable)	2.770e-05	5.101e-05	1.041e-04
A to Z	3.091e-03	5.069e-03	9.475e-03
B to Z	2.864e-03	4.718e-03	8.970e-03
C to Z	2.581e-03	4.242e-03	7.778e-03
D to Z	2.465e-03	4.018e-03	7.283e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

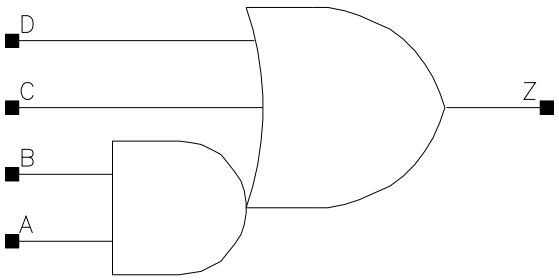
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	-2.093e-07	-1.843e-06	-4.940e-06
B (output stable)	-1.384e-06	-1.874e-06	-4.785e-06
C (output stable)	1.539e-07	7.471e-07	1.718e-06
D (output stable)	9.439e-07	2.017e-06	2.963e-06
A to Z	-3.562e-06	-6.202e-06	-1.573e-05
B to Z	-5.145e-06	-7.897e-06	-2.157e-05
C to Z	-1.271e-07	-3.347e-07	-3.095e-07
D to Z	-5.593e-08	-2.275e-07	-5.299e-07

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	0.952	1.1424
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0017
B	0.0006	0.0009	0.0018
C	0.0007	0.0009	0.0018
D	0.0006	0.0010	0.0017

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0603	0.0527	1.9987	0.9879
A to Z ↑	0.0299	0.0271	3.2752	1.6774
B to Z ↓	0.0577	0.0492	1.9959	0.9858
B to Z ↑	0.0314	0.0279	3.2722	1.6762
C to Z ↓	0.0649	0.0572	1.9911	0.9833
C to Z ↑	0.0271	0.0252	3.2590	1.6684

D to Z ↓	0.0638	0.0568	1.9919	0.9841
D to Z ↑	0.0268	0.0252	3.2569	1.6678
	X33_P4		**X33_P4**	
A to Z ↓	0.0531		0.4945	
A to Z ↑	0.0268		0.8137	
B to Z ↓	0.0480		0.4925	
B to Z ↑	0.0273		0.8151	
C to Z ↓	0.0581		0.4920	
C to Z ↑	0.0246		0.8113	
D to Z ↓	0.0565		0.4922	
D to Z ↑	0.0239		0.8103	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	1.905e-07	2.276e-12
X17_P4	3.543e-07	2.528e-12
X33_P4	7.197e-07	4.542e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.760e-06	4.832e-06	1.811e-05
B (output stable)	8.277e-06	1.500e-05	6.596e-05
C (output stable)	1.358e-04	2.497e-04	6.781e-04
D (output stable)	9.508e-06	1.675e-05	3.846e-05
A to Z	2.526e-03	4.139e-03	8.178e-03
B to Z	2.414e-03	3.886e-03	7.446e-03
C to Z	2.966e-03	4.939e-03	9.928e-03
D to Z	2.780e-03	4.626e-03	9.061e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

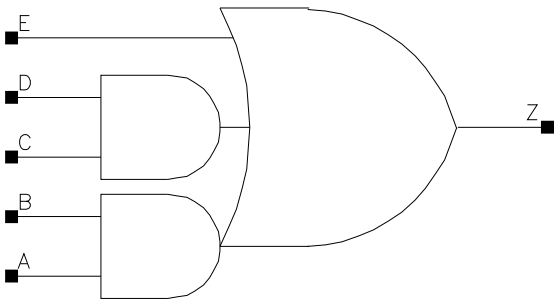
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	1.634e-06	2.600e-06	4.866e-06
B (output stable)	6.861e-06	1.177e-05	2.307e-05
C (output stable)	-2.648e-05	-4.778e-05	-1.249e-04
D (output stable)	4.821e-06	1.049e-05	3.245e-05
A to Z	-3.003e-07	-4.669e-07	-8.497e-07
B to Z	-3.172e-07	-3.800e-07	-7.644e-07
C to Z	-7.875e-06	-1.290e-05	-3.085e-05
D to Z	-5.634e-06	-8.915e-06	-1.624e-05

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.088	1.3056
X17_P4	1.200	1.224	1.4688
X33_P4	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0019
B	0.0006	0.0009	0.0017
C	0.0007	0.0011	0.0019
D	0.0006	0.0009	0.0018
E	0.0006	0.0009	0.0017

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0751	0.0650	1.9072	0.9558
A to Z ↑	0.0358	0.0313	3.2136	1.6218

B to Z ↓	0.0726	0.0622	1.9022	0.9542
B to Z ↑	0.0380	0.0330	3.2131	1.6214
C to Z ↓	0.0623	0.0549	1.8979	0.9529
C to Z ↑	0.0315	0.0273	3.1879	1.6129
D to Z ↓	0.0582	0.0504	1.8911	0.9489
D to Z ↑	0.0330	0.0285	3.1881	1.6130
E to Z ↓	0.0660	0.0573	1.8868	0.9481
E to Z ↑	0.0283	0.0250	3.1686	1.6038
	X33_P4		**X33_P4**	
A to Z ↓	0.0638		0.4936	
A to Z ↑	0.0320		0.8192	
B to Z ↓	0.0604		0.4930	
B to Z ↑	0.0336		0.8189	
C to Z ↓	0.0531		0.4921	
C to Z ↑	0.0273		0.8138	
D to Z ↓	0.0490		0.4906	
D to Z ↑	0.0284		0.8143	
E to Z ↓	0.0560		0.4899	
E to Z ↑	0.0250		0.8093	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.309e-07	2.780e-12
X17_P4	4.221e-07	3.032e-12
X33_P4	7.810e-07	5.038e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	1.966e-05	4.096e-05	8.768e-05
B (output stable)	6.747e-05	9.585e-05	2.184e-04
C (output stable)	1.248e-05	1.611e-05	3.989e-05
D (output stable)	9.576e-06	1.880e-05	4.905e-05
E (output stable)	1.011e-04	1.349e-04	3.208e-04
A to Z	3.522e-03	5.614e-03	1.102e-02
B to Z	3.429e-03	5.377e-03	1.041e-02
C to Z	2.719e-03	4.362e-03	8.454e-03
D to Z	2.586e-03	4.096e-03	7.850e-03
E to Z	3.040e-03	4.842e-03	9.373e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	-2.620e-06	-5.918e-06	-1.241e-05
B (output stable)	-1.142e-05	-1.679e-05	-3.539e-05
C (output stable)	7.092e-06	1.258e-05	2.444e-05
D (output stable)	1.402e-06	4.000e-06	4.811e-06
E (output stable)	-2.552e-06	-2.539e-06	-1.116e-05
A to Z	-9.583e-06	-1.408e-05	-2.905e-05
B to Z	-1.125e-05	-1.610e-05	-3.471e-05
C to Z	-2.591e-07	-1.795e-07	-9.719e-07
D to Z	-1.599e-07	-3.367e-07	-7.601e-07

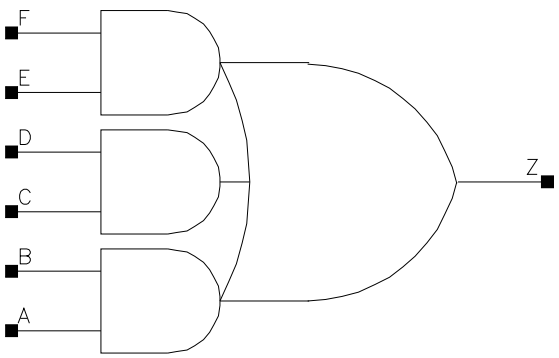
E to Z	-6.054e-06	-9.189e-06	-1.768e-05

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.360	1.6320
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
A	0.0006	0.0007	0.0009	0.0019

B	0.0006	0.0007	0.0012	0.0017
C	0.0006	0.0007	0.0009	0.0018
D	0.0006	0.0007	0.0009	0.0017
E	0.0006	0.0007	0.0009	0.0019
F	0.0006	0.0007	0.0010	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0753	0.0714	3.5817	1.9000
A to Z ↑	0.0377	0.0365	6.3589	3.2819
B to Z ↓	0.0699	0.0666	3.5658	1.8919
B to Z ↑	0.0386	0.0376	6.3511	3.2784
C to Z ↓	0.0687	0.0656	3.5718	1.8956
C to Z ↑	0.0348	0.0336	6.3230	3.2624
D to Z ↓	0.0658	0.0628	3.5621	1.8897
D to Z ↑	0.0367	0.0355	6.3236	3.2628
E to Z ↓	0.0560	0.0547	3.5545	1.8872
E to Z ↑	0.0303	0.0293	6.2964	3.2482
F to Z ↓	0.0524	0.0513	3.5449	1.8812
F to Z ↑	0.0316	0.0307	6.2956	3.2503
	X17_P4	X33_P4	X17_P4	X33_P4
A to Z ↓	0.0690	0.0659	0.9589	0.4917
A to Z ↑	0.0339	0.0339	1.6264	0.8219
B to Z ↓	0.0653	0.0626	0.9545	0.4910
B to Z ↑	0.0358	0.0355	1.6264	0.8217
C to Z ↓	0.0641	0.0614	0.9570	0.4912
C to Z ↑	0.0314	0.0320	1.6184	0.8177
D to Z ↓	0.0609	0.0584	0.9537	0.4905
D to Z ↑	0.0332	0.0335	1.6189	0.8177
E to Z ↓	0.0532	0.0536	0.9526	0.4897
E to Z ↑	0.0274	0.0284	1.6133	0.8154
F to Z ↓	0.0499	0.0498	0.9498	0.4883
F to Z ↑	0.0287	0.0298	1.6137	0.8155

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	2.032e-07	3.284e-12
X8_P4	2.852e-07	3.284e-12
X17_P4	4.581e-07	3.536e-12
X33_P4	8.322e-07	5.552e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	6.319e-05	7.736e-05	9.938e-05	2.018e-04
B (output stable)	2.085e-04	2.505e-04	3.146e-04	5.984e-04
C (output stable)	3.163e-05	3.931e-05	5.396e-05	9.282e-05
D (output stable)	4.468e-05	5.611e-05	7.190e-05	1.474e-04
E (output stable)	2.909e-05	3.183e-05	3.717e-05	5.232e-05
F (output stable)	2.983e-05	3.452e-05	4.632e-05	9.689e-05

A to Z	3.300e-03	4.264e-03	6.317e-03	1.192e-02
B to Z	3.060e-03	3.978e-03	5.948e-03	1.128e-02
C to Z	2.800e-03	3.663e-03	5.514e-03	1.039e-02
D to Z	2.682e-03	3.512e-03	5.264e-03	9.806e-03
E to Z	2.217e-03	3.014e-03	4.552e-03	8.893e-03
F to Z	2.091e-03	2.849e-03	4.304e-03	8.314e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

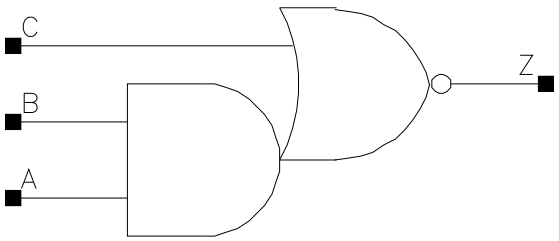
Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X33_P4
A (output stable)	-7.147e-06	-9.698e-06	-1.380e-05	-2.895e-05
B (output stable)	-2.671e-05	-3.221e-05	-4.461e-05	-9.205e-05
C (output stable)	-3.181e-06	-3.716e-06	-4.297e-06	-3.403e-06
D (output stable)	-1.045e-06	-1.077e-06	-8.929e-07	9.856e-06
E (output stable)	1.692e-05	2.103e-05	2.994e-05	5.264e-05
F (output stable)	1.210e-05	1.511e-05	2.167e-05	4.375e-05
A to Z	-1.148e-05	-1.370e-05	-1.857e-05	-3.516e-05
B to Z	-1.188e-05	-1.412e-05	-1.889e-05	-3.563e-05
C to Z	-7.717e-06	-8.912e-06	-1.163e-05	-1.616e-05
D to Z	-6.798e-06	-7.935e-06	-1.008e-05	-1.328e-05
E to Z	-4.577e-07	-4.531e-07	-6.353e-07	-1.246e-06
F to Z	-2.562e-07	-2.733e-07	-4.444e-07	-8.842e-07

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008
X44_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X33_P4	X44_P4
A	0.0008	0.0023	0.0045	0.0062
B	0.0007	0.0021	0.0042	0.0057
C	0.0008	0.0024	0.0048	0.0062

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0117	0.0121	3.3560	1.1456
A to Z ↑	0.0219	0.0223	7.0661	2.3621
B to Z ↓	0.0111	0.0114	3.3951	1.1625
B to Z ↑	0.0183	0.0182	6.9650	2.3620
C to Z ↓	0.0112	0.0115	1.8909	0.6533
C to Z ↑	0.0237	0.0238	6.4561	2.1762
	X33_P4	**X44_P4**	**X33_P4**	**X44_P4**
A to Z ↓	0.0125	0.0124	0.5833	0.4427

A to Z ↑	0.0224	0.0224	1.1829	0.8974
B to Z ↓	0.0113	0.0113	0.5925	0.4497
B to Z ↑	0.0181	0.0180	1.1809	0.8933
C to Z ↓	0.0128	0.0129	0.3887	0.3026
C to Z ↑	0.0241	0.0240	1.0883	0.8242

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P4	1.505e-07	1.773e-12
X17_P4	4.179e-07	3.287e-12
X33_P4	7.863e-07	5.556e-12
X44_P4	1.045e-06	7.060e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	1.096e-05	4.208e-05	8.684e-05	1.178e-04
B (output stable)	4.148e-05	1.813e-04	3.958e-04	5.144e-04
C (output stable)	1.267e-04	3.977e-04	8.595e-04	1.126e-03
A to Z	1.076e-03	3.427e-03	6.935e-03	9.165e-03
B to Z	8.395e-04	2.472e-03	4.913e-03	6.475e-03
C to Z	1.571e-03	4.726e-03	9.628e-03	1.267e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

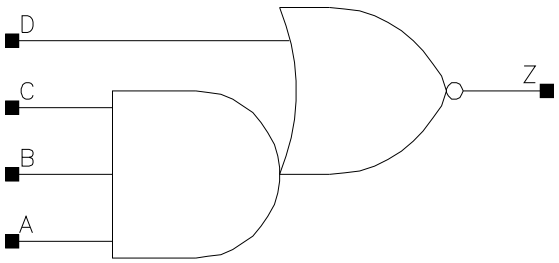
Pin Cycle (vdds)	X6_P4	X17_P4	X33_P4	X44_P4
A (output stable)	3.567e-06	1.209e-05	1.957e-05	2.752e-05
B (output stable)	2.419e-05	5.729e-05	1.272e-04	1.616e-04
C (output stable)	-1.692e-05	-4.180e-05	-9.237e-05	-1.180e-04
A to Z	1.500e-09	-6.970e-07	-4.300e-07	-4.610e-07
B to Z	-6.750e-08	-2.960e-07	-1.725e-06	-2.035e-06
C to Z	-1.136e-05	-3.065e-05	-6.279e-05	-8.323e-05

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X29_P4	1.200	3.536	4.2432
X38_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X29_P4	X38_P4
A	0.0008	0.0046	0.0061
B	0.0007	0.0044	0.0058
C	0.0007	0.0042	0.0056
D	0.0008	0.0048	0.0059

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X29_P4	X5_P4	X29_P4
A to Z ↓	0.0163	0.0175	4.8451	0.8449
A to Z ↑	0.0275	0.0276	7.0602	1.1697
B to Z ↓	0.0165	0.0170	4.8624	0.8491
B to Z ↑	0.0248	0.0245	7.0640	1.1794
C to Z ↓	0.0156	0.0154	4.8897	0.8545
C to Z ↑	0.0215	0.0207	6.9741	1.1878
D to Z ↓	0.0133	0.0150	1.9342	0.3911

D to Z ↑	0.0268	0.0273	6.0308	1.0110
	X38_P4		**X38_P4**	
A to Z ↓	0.0172		0.6536	
A to Z ↑	0.0270		0.8815	
B to Z ↓	0.0169		0.6576	
B to Z ↑	0.0241		0.8909	
C to Z ↓	0.0153		0.6629	
C to Z ↑	0.0203		0.9000	
D to Z ↓	0.0156		0.3243	
D to Z ↑	0.0267		0.7633	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P4	1.657e-07	2.024e-12
X29_P4	8.762e-07	7.313e-12
X38_P4	1.125e-06	9.326e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P4	X29_P4	X38_P4
A (output stable)	1.108e-05	1.000e-04	1.230e-04
B (output stable)	2.765e-05	2.037e-04	2.666e-04
C (output stable)	4.850e-05	4.750e-04	5.908e-04
D (output stable)	5.454e-04	4.096e-03	5.389e-03
A to Z	1.643e-03	1.036e-02	1.322e-02
B to Z	1.411e-03	8.456e-03	1.083e-02
C to Z	1.169e-03	6.445e-03	8.160e-03
D to Z	2.061e-03	1.261e-02	1.617e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

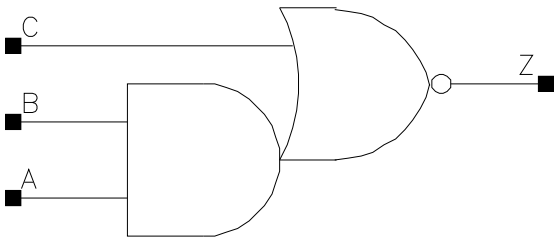
Pin Cycle (vdds)	X5_P4	X29_P4	X38_P4
A (output stable)	1.211e-05	8.889e-05	1.143e-04
B (output stable)	1.639e-06	1.035e-05	1.413e-05
C (output stable)	1.512e-06	6.376e-06	7.271e-06
D (output stable)	-7.772e-05	-6.424e-04	-8.200e-04
A to Z	1.230e-07	-2.650e-07	-4.820e-07
B to Z	1.820e-07	-2.400e-08	1.290e-07
C to Z	-1.540e-07	-1.647e-06	-3.306e-06
D to Z	-9.394e-06	-7.433e-05	-9.754e-05

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X11_P4	1.200	1.088	1.3056
X16_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P4	X11_P4	X16_P4	X23_P4
A	0.0008	0.0017	0.0025	0.0033
B	0.0008	0.0016	0.0023	0.0031
C	0.0008	0.0015	0.0022	0.0031
	X46_P4			
A	0.0063			
B	0.0060			
C	0.0061			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X11_P4	X6_P4	X11_P4
A to Z ↓	0.0132	0.0143	3.2327	1.6502
A to Z ↑	0.0254	0.0267	7.0520	3.4435
B to Z ↓	0.0134	0.0137	3.2690	1.6720

B to Z ↑	0.0228	0.0233	6.9662	3.4509
C to Z ↓	0.0082	0.0085	1.9512	1.1481
C to Z ↑	0.0180	0.0175	6.4317	3.1682
	X16_P4	**X23_P4**	**X16_P4**	**X23_P4**
A to Z ↓	0.0137	0.0140	1.1439	0.8609
A to Z ↑	0.0253	0.0257	2.3178	1.7554
B to Z ↓	0.0136	0.0135	1.1601	0.8723
B to Z ↑	0.0219	0.0223	2.3145	1.7600
C to Z ↓	0.0087	0.0078	0.8008	0.5049
C to Z ↑	0.0170	0.0173	2.1296	1.6144
	X46_P4		**X46_P4**	
A to Z ↓	0.0137		0.4433	
A to Z ↑	0.0249		0.9092	
B to Z ↓	0.0132		0.4493	
B to Z ↑	0.0214		0.9062	
C to Z ↓	0.0080		0.2595	
C to Z ↑	0.0172		0.8342	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P4	1.549e-07	1.772e-12
X11_P4	3.068e-07	2.780e-12
X16_P4	4.183e-07	3.284e-12
X23_P4	5.956e-07	4.293e-12
X46_P4	1.144e-06	7.317e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	3.512e-05	8.643e-05	1.183e-04	1.626e-04
B (output stable)	1.701e-04	4.665e-04	5.563e-04	7.815e-04
C (output stable)	5.177e-05	1.335e-04	1.790e-04	2.745e-04
A to Z	1.611e-03	3.578e-03	4.865e-03	6.650e-03
B to Z	1.368e-03	2.880e-03	3.868e-03	5.252e-03
C to Z	7.937e-04	1.607e-03	2.220e-03	3.048e-03
	X46_P4			
A (output stable)	3.045e-04			
B (output stable)	1.357e-03			
C (output stable)	3.928e-04			
A to Z	1.224e-02			
B to Z	9.583e-03			
C to Z	5.648e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X6_P4	X11_P4	X16_P4	X23_P4
A (output stable)	-3.187e-06	-8.013e-06	-8.510e-06	-1.096e-05
B (output stable)	-2.833e-05	-7.376e-05	-7.351e-05	-1.020e-04
C (output stable)	7.156e-05	1.844e-04	1.845e-04	2.537e-04
A to Z	-5.791e-06	-1.594e-05	-1.656e-05	-1.930e-05
B to Z	-5.542e-06	-1.584e-05	-1.545e-05	-2.109e-05
C to Z	7.163e-08	2.863e-07	-1.537e-07	6.310e-07

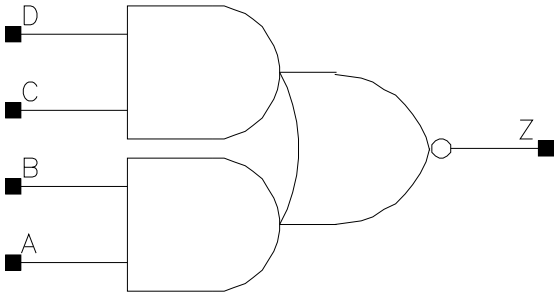
	X46_P4			
A (output stable)	-1.995e-05			
B (output stable)	-1.717e-04			
C (output stable)	4.332e-04			
A to Z	-3.506e-05			
B to Z	-3.827e-05			
C to Z	3.510e-06			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P4	X10_P4	X16_P4	X21_P4
A	0.0007	0.0017	0.0025	0.0032
B	0.0007	0.0015	0.0023	0.0031
C	0.0006	0.0016	0.0023	0.0031
D	0.0007	0.0014	0.0022	0.0029
	X42_P4			
A	0.0064			
B	0.0060			
C	0.0061			
D	0.0057			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X10_P4**	**X4_P4**	**X10_P4**
A to Z ↓	0.0147	0.0145	4.0131	1.5840
A to Z ↑	0.0317	0.0276	9.6251	3.1828
B to Z ↓	0.0152	0.0152	4.0599	1.6043
B to Z ↑	0.0288	0.0256	9.5895	3.2523
C to Z ↓	0.0118	0.0113	4.1125	1.5924
C to Z ↑	0.0247	0.0218	9.5233	3.1700
D to Z ↓	0.0116	0.0111	4.1732	1.6188
D to Z ↑	0.0215	0.0190	9.4923	3.2124
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0157	0.0156	1.1508	0.8652
A to Z ↑	0.0287	0.0285	2.1463	1.6568
B to Z ↓	0.0160	0.0155	1.1643	0.8759
B to Z ↑	0.0257	0.0254	2.1440	1.6576
C to Z ↓	0.0122	0.0124	1.1474	0.8650
C to Z ↑	0.0225	0.0229	2.1249	1.6386
D to Z ↓	0.0116	0.0112	1.1674	0.8796
D to Z ↑	0.0190	0.0190	2.1268	1.6407
	X42_P4		**X42_P4**	
A to Z ↓	0.0163		0.4510	
A to Z ↑	0.0288		0.8318	
B to Z ↓	0.0159		0.4565	
B to Z ↑	0.0254		0.8281	
C to Z ↓	0.0129		0.4447	
C to Z ↑	0.0230		0.8243	
D to Z ↓	0.0117		0.4526	
D to Z ↑	0.0192		0.8219	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	1.440e-07	2.025e-12
X10_P4	3.754e-07	3.282e-12
X16_P4	5.216e-07	4.042e-12
X21_P4	7.044e-07	5.300e-12
X42_P4	1.371e-06	9.329e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	2.871e-05	7.239e-05	1.371e-04	1.829e-04
B (output stable)	4.037e-05	1.025e-04	1.933e-04	2.651e-04
C (output stable)	1.236e-05	3.228e-05	7.922e-05	1.173e-04
D (output stable)	3.882e-05	9.953e-05	2.653e-04	4.012e-04
A to Z	1.664e-03	4.042e-03	6.384e-03	8.265e-03
B to Z	1.462e-03	3.561e-03	5.415e-03	6.945e-03
C to Z	9.637e-04	2.363e-03	3.769e-03	5.043e-03
D to Z	7.743e-04	1.888e-03	2.805e-03	3.654e-03
	X42_P4			
A (output stable)	3.465e-04			
B (output stable)	4.985e-04			
C (output stable)	2.108e-04			
D (output stable)	7.296e-04			

A to Z	1.622e-02			
B to Z	1.362e-02			
C to Z	9.832e-03			
D to Z	7.191e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

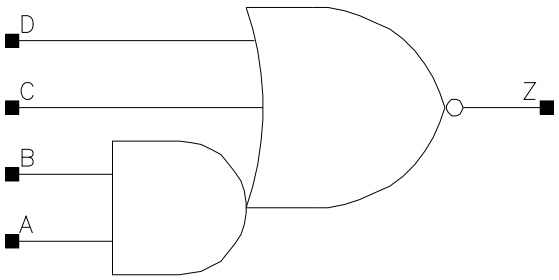
Pin Cycle (vdds)	X4_P4	X10_P4	X16_P4	X21_P4
A (output stable)	-2.147e-06	-4.819e-06	-6.956e-06	-8.139e-06
B (output stable)	-1.991e-06	-4.724e-06	-6.999e-06	-9.642e-06
C (output stable)	3.571e-07	1.600e-06	1.800e-06	4.661e-06
D (output stable)	8.951e-07	3.296e-06	4.502e-06	4.942e-06
A to Z	-8.709e-06	-1.678e-05	-2.510e-05	-2.886e-05
B to Z	-1.131e-05	-2.206e-05	-3.308e-05	-4.197e-05
C to Z	-2.185e-07	-1.570e-07	-7.953e-07	-2.677e-07
D to Z	-9.020e-08	-2.400e-07	-6.320e-07	-7.483e-07
	X42_P4			
A (output stable)	-1.482e-05			
B (output stable)	-1.819e-05			
C (output stable)	8.211e-06			
D (output stable)	1.114e-05			
A to Z	-5.384e-05			
B to Z	-8.102e-05			
C to Z	-8.970e-07			
D to Z	-3.225e-06			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X35_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P4	X35_P4
A	0.0008	0.0059
B	0.0008	0.0055
C	0.0008	0.0057
D	0.0008	0.0054

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X35_P4	X5_P4	X35_P4
A to Z ↓	0.0132	0.0138	3.3914	0.5026
A to Z ↑	0.0285	0.0271	10.7478	1.3686
B to Z ↓	0.0131	0.0131	3.4410	0.5121
B to Z ↑	0.0243	0.0221	10.6795	1.3691
C to Z ↓	0.0134	0.0168	2.0230	0.3889
C to Z ↑	0.0341	0.0336	10.1555	1.2969
D to Z ↓	0.0129	0.0156	2.0410	0.3882

D to Z ↑	0.0331	0.0316	10.1648	1.2992

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P4	1.509e-07	2.025e-12
X35_P4	9.467e-07	9.332e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P4	X35_P4
A (output stable)	4.665e-06	5.793e-05
B (output stable)	1.497e-05	1.808e-04
C (output stable)	2.410e-04	2.376e-03
D (output stable)	1.535e-05	1.534e-04
A to Z	1.316e-03	9.603e-03
B to Z	1.079e-03	7.206e-03
C to Z	2.127e-03	1.656e-02
D to Z	1.797e-03	1.316e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

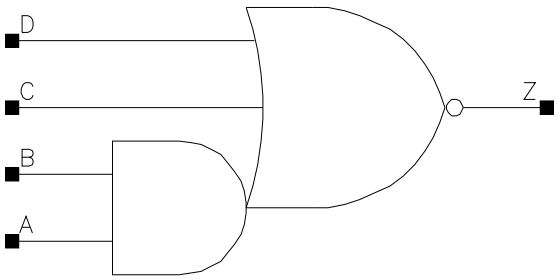
Pin Cycle (vdds)	X5_P4	X35_P4
A (output stable)	2.961e-06	2.435e-05
B (output stable)	1.130e-05	6.887e-05
C (output stable)	-4.589e-05	-3.565e-04
D (output stable)	9.993e-06	8.662e-05
A to Z	-1.817e-07	-1.922e-06
B to Z	-2.795e-07	-3.036e-06
C to Z	-1.235e-05	-9.044e-05
D to Z	-8.243e-06	-5.182e-05

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.680	0.8160
X17_P4	1.200	2.448	2.9376
X34_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P4	X17_P4	X34_P4
A	0.0008	0.0032	0.0065
B	0.0008	0.0031	0.0061
C	0.0007	0.0028	0.0055
D	0.0007	0.0026	0.0051

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X17_P4	X4_P4	X17_P4
A to Z ↓	0.0151	0.0162	3.6690	0.9758
A to Z ↑	0.0340	0.0356	10.7940	2.6591
B to Z ↓	0.0159	0.0163	3.7120	0.9868
B to Z ↑	0.0307	0.0312	10.6892	2.6602
C to Z ↓	0.0140	0.0137	3.2221	0.7838
C to Z ↑	0.0259	0.0272	10.1288	2.5088

D to Z ↓	0.0119	0.0108	3.2852	0.7884
D to Z ↑	0.0222	0.0204	10.1655	2.5183
	X34_P4		**X34_P4**	
A to Z ↓	0.0160		0.5014	
A to Z ↑	0.0351		1.3534	
B to Z ↓	0.0163		0.5071	
B to Z ↑	0.0307		1.3478	
C to Z ↓	0.0139		0.4153	
C to Z ↑	0.0266		1.2742	
D to Z ↓	0.0110		0.4198	
D to Z ↑	0.0201		1.2797	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	1.339e-07	2.026e-12
X17_P4	5.246e-07	5.302e-12
X34_P4	1.004e-06	9.334e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P4	X17_P4	X34_P4
A (output stable)	3.736e-05	1.666e-04	3.310e-04
B (output stable)	8.787e-05	4.136e-04	8.066e-04
C (output stable)	8.646e-05	6.231e-04	1.163e-03
D (output stable)	4.402e-06	8.624e-05	1.466e-04
A to Z	2.025e-03	8.755e-03	1.690e-02
B to Z	1.808e-03	7.428e-03	1.441e-02
C to Z	1.225e-03	5.308e-03	1.009e-02
D to Z	8.575e-04	3.179e-03	6.035e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

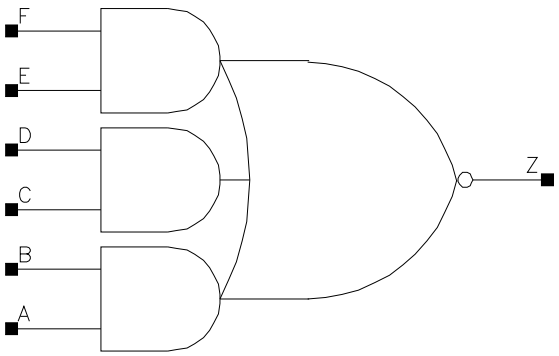
Pin Cycle (vdds)	X4_P4	X17_P4	X34_P4
A (output stable)	-5.590e-06	-1.807e-05	-3.557e-05
B (output stable)	-1.596e-05	-5.192e-05	-1.022e-04
C (output stable)	7.671e-07	-5.632e-05	-8.639e-05
D (output stable)	1.415e-05	8.156e-05	1.421e-04
A to Z	-9.932e-06	-3.612e-05	-6.853e-05
B to Z	-1.060e-05	-4.249e-05	-7.970e-05
C to Z	-3.054e-06	-1.813e-05	-3.364e-05
D to Z	2.947e-08	-1.139e-06	-1.877e-06

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.088	1.3056
X8_P4	1.200	2.176	2.6112
X13_P4	1.200	2.720	3.2640
X17_P4	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P4	X8_P4	X13_P4	X17_P4
A	0.0008	0.0016	0.0024	0.0032

B	0.0008	0.0015	0.0023	0.0030
C	0.0008	0.0016	0.0023	0.0030
D	0.0008	0.0015	0.0022	0.0028
E	0.0010	0.0015	0.0022	0.0029
F	0.0008	0.0014	0.0020	0.0027

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0171	0.0201	3.2530	1.8879
A to Z ↑	0.0470	0.0463	10.3363	4.7902
B to Z ↓	0.0185	0.0207	3.2869	1.9031
B to Z ↑	0.0436	0.0423	10.3152	4.7966
C to Z ↓	0.0160	0.0185	3.2238	1.9025
C to Z ↑	0.0415	0.0418	10.3659	4.7979
D to Z ↓	0.0169	0.0192	3.2679	1.9238
D to Z ↑	0.0380	0.0378	10.3115	4.7942
E to Z ↓	0.0127	0.0148	3.1687	1.9021
E to Z ↑	0.0308	0.0309	10.2301	4.7488
F to Z ↓	0.0127	0.0146	3.2275	1.9334
F to Z ↑	0.0270	0.0267	10.2916	4.7522
	X13_P4	X17_P4	X13_P4	X17_P4
A to Z ↓	0.0193	0.0195	1.2877	0.9834
A to Z ↑	0.0433	0.0436	3.1679	2.4200
B to Z ↓	0.0204	0.0201	1.2975	0.9913
B to Z ↑	0.0399	0.0396	3.1758	2.4190
C to Z ↓	0.0179	0.0180	1.2970	0.9725
C to Z ↑	0.0387	0.0392	3.1769	2.4292
D to Z ↓	0.0187	0.0181	1.3103	0.9833
D to Z ↑	0.0352	0.0351	3.1785	2.4231
E to Z ↓	0.0144	0.0144	1.2913	0.9728
E to Z ↑	0.0292	0.0293	3.1500	2.4002
F to Z ↓	0.0142	0.0135	1.3107	0.9892
F to Z ↑	0.0251	0.0250	3.1536	2.4092

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	2.447e-07	2.780e-12
X8_P4	4.711e-07	4.797e-12
X13_P4	6.576e-07	5.803e-12
X17_P4	8.805e-07	7.568e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

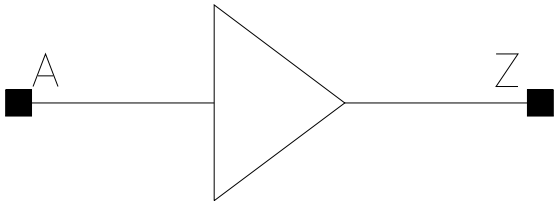
Pin Cycle (vdd)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	9.584e-05	2.156e-04	3.046e-04	4.021e-04
B (output stable)	3.092e-04	6.881e-04	9.103e-04	1.206e-03
C (output stable)	4.891e-05	1.154e-04	1.514e-04	2.112e-04
D (output stable)	6.938e-05	1.901e-04	2.296e-04	3.360e-04
E (output stable)	2.593e-05	7.085e-05	9.651e-05	1.313e-04
F (output stable)	3.830e-05	1.238e-04	1.528e-04	2.319e-04

A to Z	3.213e-03	6.761e-03	9.366e-03	1.241e-02
B to Z	2.971e-03	6.086e-03	8.504e-03	1.111e-02
C to Z	2.426e-03	5.296e-03	7.110e-03	9.487e-03
D to Z	2.176e-03	4.653e-03	6.281e-03	8.205e-03
E to Z	1.503e-03	3.433e-03	4.615e-03	6.109e-03
F to Z	1.275e-03	2.810e-03	3.774e-03	4.855e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X4_P4	X8_P4	X13_P4	X17_P4
A (output stable)	-1.567e-05	-3.476e-05	-4.105e-05	-5.401e-05
B (output stable)	-5.496e-05	-1.133e-04	-1.307e-04	-1.728e-04
C (output stable)	-4.582e-06	-1.131e-05	-1.034e-05	-1.312e-05
D (output stable)	2.385e-06	-1.588e-06	2.718e-07	-3.904e-06
E (output stable)	3.135e-05	7.174e-05	8.151e-05	1.115e-04
F (output stable)	2.613e-05	5.552e-05	6.454e-05	8.563e-05
A to Z	-2.186e-05	-4.583e-05	-5.169e-05	-7.036e-05
B to Z	-2.431e-05	-4.740e-05	-5.342e-05	-7.241e-05
C to Z	-1.334e-05	-2.667e-05	-3.104e-05	-4.047e-05
D to Z	-9.871e-06	-2.311e-05	-2.456e-05	-3.386e-05
E to Z	-5.883e-07	-1.100e-06	-2.304e-06	-1.555e-06
F to Z	-4.590e-07	-9.031e-07	-9.264e-07	-1.716e-06

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.408	0.4896
X6_P4	1.200	0.408	0.4896
X8_P4	1.200	0.408	0.4896
X13_P4	1.200	0.544	0.6528
X16_P4	1.200	0.544	0.6528
X21_P4	1.200	0.680	0.8160
X25_P4	1.200	0.680	0.8160
X29_P4	1.200	0.952	1.1424
X33_P4	1.200	0.952	1.1424
X42_P4	1.200	1.088	1.3056
X50_P4	1.200	1.224	1.4688
X58_P4	1.200	1.496	1.7952
X67_P4	1.200	1.632	1.9584
X75_P4	1.200	1.768	2.1216
X84_P4	1.200	1.904	2.2848
X100_P4	1.200	2.312	2.7744
X134_P4	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0008	0.0008	0.0008	0.0008
	X16_P4	X21_P4	X25_P4	X29_P4
A	0.0008	0.0011	0.0011	0.0015
	X33_P4	X42_P4	X50_P4	X58_P4
A	0.0014	0.0016	0.0019	0.0029

	X67_P4	X75_P4	X84_P4	X100_P4
A	0.0029	0.0029	0.0028	0.0038
	X134_P4			
A	0.0047			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0288	0.0290	3.3223	2.4397
A to Z ↑	0.0212	0.0211	6.2520	4.5885
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0300	0.0336	1.8142	1.1708
A to Z ↑	0.0217	0.0242	3.2915	2.1410
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0355	0.0304	0.9344	0.7204
A to Z ↑	0.0253	0.0223	1.6473	1.2918
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0318	0.0303	0.6222	0.5237
A to Z ↑	0.0232	0.0216	1.0853	0.9222
	X33_P4	**X42_P4**	**X33_P4**	**X42_P4**
A to Z ↓	0.0318	0.0309	0.4660	0.3783
A to Z ↑	0.0226	0.0226	0.8107	0.6528
	X50_P4	**X58_P4**	**X50_P4**	**X58_P4**
A to Z ↓	0.0304	0.0285	0.3141	0.2713
A to Z ↑	0.0221	0.0210	0.5409	0.4653
	X67_P4	**X75_P4**	**X67_P4**	**X75_P4**
A to Z ↓	0.0296	0.0312	0.2383	0.2153
A to Z ↑	0.0218	0.0229	0.4081	0.3650
	X84_P4	**X100_P4**	**X84_P4**	**X100_P4**
A to Z ↓	0.0325	0.0306	0.1952	0.1639
A to Z ↑	0.0238	0.0225	0.3291	0.2761
	X134_P4		**X134_P4**	
A to Z ↓	0.0319		0.1279	
A to Z ↑	0.0237		0.2111	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	1.110e-07	1.478e-12
X6_P4	1.317e-07	1.519e-12
X8_P4	1.548e-07	1.518e-12
X13_P4	2.040e-07	1.771e-12
X16_P4	2.433e-07	1.771e-12
X21_P4	3.270e-07	2.021e-12
X25_P4	3.548e-07	2.022e-12
X29_P4	4.324e-07	2.528e-12
X33_P4	4.500e-07	2.526e-12
X42_P4	5.524e-07	2.775e-12
X50_P4	6.600e-07	3.028e-12
X58_P4	8.130e-07	3.538e-12
X67_P4	8.896e-07	3.786e-12
X75_P4	9.662e-07	4.048e-12

X84_P4	1.043e-06	4.298e-12
X100_P4	1.273e-06	5.051e-12
X134_P4	1.656e-06	6.307e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	1.596e-03	1.771e-03	2.077e-03	2.722e-03
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	3.178e-03	4.418e-03	4.919e-03	5.509e-03
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	6.108e-03	7.602e-03	8.876e-03	1.099e-02
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	1.203e-02	1.362e-02	1.480e-02	1.762e-02
	X134_P4			
A to Z	2.375e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

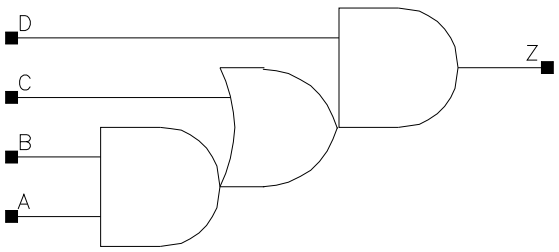
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	-1.133e-07	-1.961e-07	-1.130e-08	-1.833e-07
	X16_P4	X21_P4	X25_P4	X29_P4
A to Z	-9.850e-08	-2.745e-07	-3.230e-07	-1.551e-07
	X33_P4	X42_P4	X50_P4	X58_P4
A to Z	-5.013e-07	-6.770e-07	-3.020e-07	-1.520e-07
	X67_P4	X75_P4	X84_P4	X100_P4
A to Z	-1.009e-06	8.700e-08	-1.070e-07	-2.030e-07
	X134_P4			
A to Z	-2.332e-06			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.632	1.9584
X25_P4	1.200	1.768	2.1216
X33_P4	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0009	0.0020	0.0020	0.0019
B	0.0009	0.0018	0.0018	0.0017
C	0.0010	0.0023	0.0022	0.0022
D	0.0015	0.0019	0.0019	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0409	0.0388	1.8566	0.9229
A to Z ↑	0.0327	0.0309	3.3235	1.6179
B to Z ↓	0.0381	0.0358	1.8516	0.9216
B to Z ↑	0.0327	0.0303	3.3212	1.6176
C to Z ↓	0.0341	0.0316	1.8470	0.9194
C to Z ↑	0.0250	0.0229	3.2977	1.6068

D to Z ↓	0.0321	0.0286	1.8267	0.9102
D to Z ↑	0.0288	0.0254	3.3020	1.6079
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0425	0.0448	0.6298	0.4750
A to Z ↑	0.0338	0.0353	1.0973	0.8231
B to Z ↓	0.0396	0.0425	0.6288	0.4749
B to Z ↑	0.0334	0.0355	1.0966	0.8227
C to Z ↓	0.0355	0.0382	0.6270	0.4724
C to Z ↑	0.0255	0.0271	1.0866	0.8150
D to Z ↓	0.0309	0.0325	0.6183	0.4641
D to Z ↑	0.0277	0.0290	1.0880	0.8158

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.515e-07	2.528e-12
X17_P4	4.735e-07	3.787e-12
X25_P4	5.440e-07	4.039e-12
X33_P4	6.145e-07	4.291e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	4.721e-05	1.042e-04	1.035e-04	9.848e-05
B (output stable)	8.742e-05	1.494e-04	1.506e-04	1.522e-04
C (output stable)	2.965e-04	4.947e-04	4.952e-04	4.725e-04
D (output stable)	8.185e-05	9.900e-05	9.806e-05	9.796e-05
A to Z	3.545e-03	6.462e-03	7.969e-03	9.077e-03
B to Z	3.289e-03	5.805e-03	7.314e-03	8.535e-03
C to Z	2.716e-03	4.610e-03	6.131e-03	7.306e-03
D to Z	3.611e-03	6.136e-03	7.639e-03	8.752e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

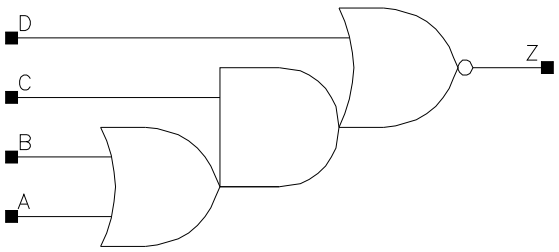
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	-3.016e-06	-5.793e-06	-5.814e-06	-5.669e-06
B (output stable)	-3.673e-06	-6.404e-06	-6.515e-06	-6.352e-06
C (output stable)	-3.261e-06	-5.981e-06	-5.977e-06	-5.377e-06
D (output stable)	2.848e-06	4.300e-06	4.335e-06	3.402e-06
A to Z	-6.412e-06	-1.176e-05	-1.283e-05	-1.220e-05
B to Z	-6.629e-06	-1.275e-05	-1.291e-05	-1.260e-05
C to Z	-2.601e-07	-2.319e-07	-4.725e-07	-6.184e-07
D to Z	-2.100e-06	-3.167e-06	-3.311e-06	-3.389e-06

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.952	1.1424
X11_P4	1.200	1.496	1.7952
X16_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X16_P4	X21_P4
A	0.0009	0.0016	0.0025	0.0032
B	0.0008	0.0015	0.0024	0.0032
C	0.0008	0.0016	0.0023	0.0031
D	0.0011	0.0016	0.0023	0.0031

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0158	0.0152	3.1866	1.6860
A to Z ↑	0.0403	0.0376	10.5861	5.4907
B to Z ↓	0.0153	0.0149	3.0975	1.6531
B to Z ↑	0.0383	0.0361	10.5909	5.5004
C to Z ↓	0.0141	0.0135	2.9439	1.5606
C to Z ↑	0.0256	0.0237	6.9132	3.5482

D to Z ↓	0.0091	0.0078	1.8787	0.9528
D to Z ↑	0.0218	0.0190	7.4552	3.8368
	X16_P4	**X21_P4**	**X16_P4**	**X21_P4**
A to Z ↓	0.0152	0.0155	1.1393	0.8794
A to Z ↑	0.0354	0.0372	3.5354	2.7254
B to Z ↓	0.0146	0.0150	1.1464	0.8809
B to Z ↑	0.0346	0.0355	3.5412	2.7282
C to Z ↓	0.0137	0.0138	1.0752	0.8250
C to Z ↑	0.0232	0.0234	2.3449	1.7601
D to Z ↓	0.0079	0.0079	0.6682	0.5107
D to Z ↑	0.0179	0.0180	2.5167	1.9040

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P4	1.992e-07	2.529e-12
X11_P4	3.742e-07	3.537e-12
X16_P4	5.106e-07	4.042e-12
X21_P4	6.847e-07	5.301e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	4.503e-05	8.278e-05	1.095e-04	1.784e-04
B (output stable)	6.337e-05	1.329e-04	1.922e-04	2.643e-04
C (output stable)	2.743e-04	5.367e-04	7.471e-04	1.068e-03
D (output stable)	3.800e-05	7.769e-05	9.417e-05	1.612e-04
A to Z	2.588e-03	4.514e-03	6.341e-03	8.913e-03
B to Z	2.111e-03	3.716e-03	5.373e-03	7.289e-03
C to Z	1.765e-03	3.000e-03	4.334e-03	5.986e-03
D to Z	1.006e-03	1.663e-03	2.242e-03	2.990e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

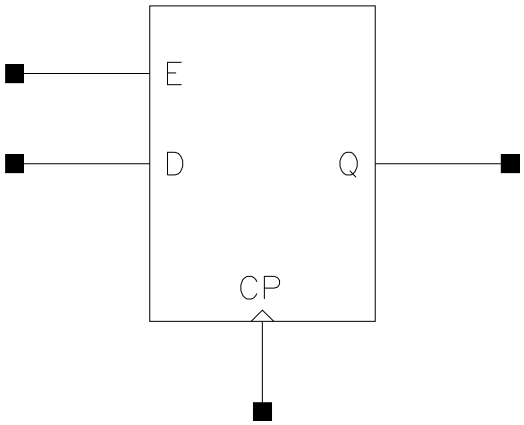
Pin Cycle (vdds)	X5_P4	X11_P4	X16_P4	X21_P4
A (output stable)	-7.552e-06	-1.124e-05	-1.515e-05	-2.537e-05
B (output stable)	-3.999e-06	-1.097e-05	-9.115e-06	-1.518e-05
C (output stable)	-3.546e-05	-6.462e-05	-9.076e-05	-1.337e-04
D (output stable)	4.711e-05	9.846e-05	1.301e-04	1.871e-04
A to Z	-1.235e-05	-2.041e-05	-2.813e-05	-4.403e-05
B to Z	-6.190e-06	-1.338e-05	-1.744e-05	-2.245e-05
C to Z	-8.434e-06	-1.582e-05	-2.065e-05	-3.088e-05
D to Z	-1.213e-07	1.912e-06	7.026e-07	-7.188e-07

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.128	3.7536
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0011	0.0011	0.0011

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0444	0.0510	1.8544	0.9639
CP to Q ↑	0.0525	0.0556	3.3425	1.6731
	X33_P4		**X33_P4**	
CP to Q ↓	0.0742		0.4739	
CP to Q ↑	0.0890		0.8297	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0653	0.0653	0.0653
CP ↑	min_pulse_width to CP	0.0358	0.0444	0.0310
D ↓	hold_rising to CP	-0.0259	-0.0259	-0.0259
D ↑	hold_rising to CP	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.0710	0.0710	0.0709
D ↑	setup_rising to CP	0.0334	0.0334	0.0334
E ↓	hold_rising to CP	-0.0184	-0.0184	-0.0184
E ↑	hold_rising to CP	-0.0035	-0.0035	-0.0035
E ↓	setup_rising to CP	0.0627	0.0627	0.0627
E ↑	setup_rising to CP	0.0708	0.0708	0.0708

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	6.804e-07	6.310e-12
X17_P4	7.629e-07	6.561e-12
X33_P4	1.027e-06	7.572e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

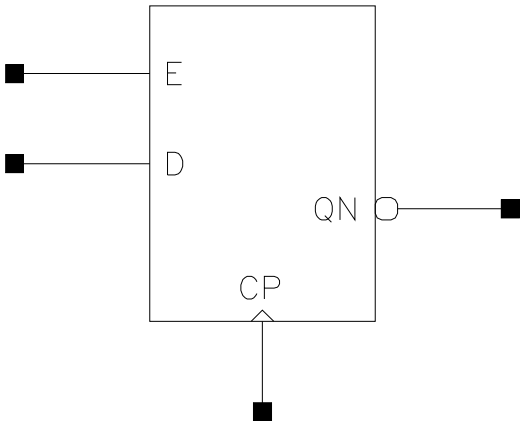
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.827e-03	3.828e-03	3.832e-03
Clock 100Mhz Data 25Mhz	8.171e-03	8.745e-03	1.139e-02
Clock 100Mhz Data 50Mhz	1.251e-02	1.366e-02	1.895e-02
Clock = 0 Data 100Mhz	4.885e-03	4.886e-03	4.886e-03
Clock = 1 Data 100Mhz	1.378e-03	1.378e-03	1.378e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.992	3.5904
X17_P4	1.200	3.264	3.9168
X33_P4	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006
E	0.0009	0.0011	0.0011

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0733	0.0689	1.9025	0.9078
CP to QN ↑	0.0580	0.0602	3.3797	1.6246
	X33_P4		**X33_P4**	
CP to QN ↓	0.0732		0.4745	
CP to QN ↑	0.0665		0.8321	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0653	0.0653	0.0653
CP ↑	min_pulse_width to CP	0.0310	0.0358	0.0395
D ↓	hold_rising to CP	-0.0259	-0.0259	-0.0259
D ↑	hold_rising to CP	-0.0065	-0.0068	-0.0068
D ↓	setup_rising to CP	0.0710	0.0710	0.0709
D ↑	setup_rising to CP	0.0334	0.0334	0.0334
E ↓	hold_rising to CP	-0.0184	-0.0184	-0.0184
E ↑	hold_rising to CP	-0.0035	-0.0035	-0.0035
E ↓	setup_rising to CP	0.0627	0.0627	0.0627
E ↑	setup_rising to CP	0.0708	0.0708	0.0708

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	6.777e-07	6.324e-12
X17_P4	8.063e-07	6.813e-12
X33_P4	1.006e-06	7.572e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

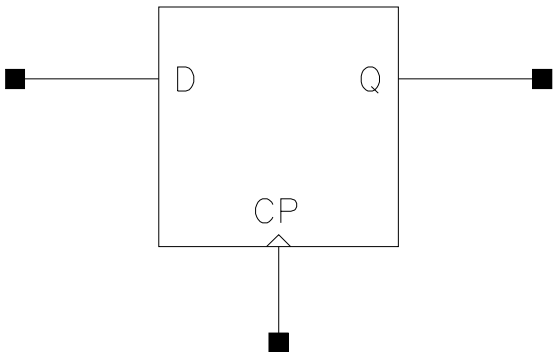
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.825e-03	3.825e-03	3.826e-03
Clock 100Mhz Data 25Mhz	8.234e-03	9.353e-03	1.113e-02
Clock 100Mhz Data 50Mhz	1.264e-02	1.488e-02	1.844e-02
Clock = 0 Data 100Mhz	4.913e-03	4.913e-03	4.911e-03
Clock = 1 Data 100Mhz	1.376e-03	1.376e-03	1.376e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.176	2.6112
X17_P4	1.200	2.448	2.9376
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0459	0.0507	1.8479	0.9562
CP to Q ↑	0.0530	0.0583	3.2337	1.6422
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to Q ↓	0.0639	0.0669	0.5730	0.5220
CP to Q ↑	0.0648	0.0666	0.9231	0.8423

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0556	0.0567	0.0567	0.0567
CP ↑	min_pulse_width to CP	0.0358	0.0406	0.0540	0.0589
D ↓	hold_rising to CP	0.0031	0.0031	0.0031	0.0031
D ↑	hold_rising to CP	0.0078	0.0078	0.0078	0.0078
D ↓	setup_rising to CP	0.0364	0.0392	0.0392	0.0392
D ↑	setup_rising to CP	0.0171	0.0167	0.0167	0.0167

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	5.427e-07	4.796e-12
X17_P4	6.322e-07	5.300e-12
X30_P4	7.743e-07	5.806e-12
X33_P4	7.875e-07	5.806e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

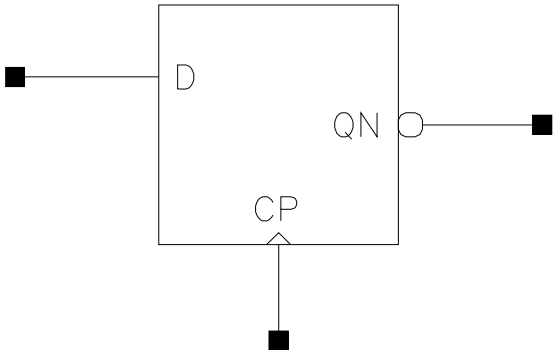
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	4.016e-03	4.036e-03	4.044e-03	4.048e-03
Clock 100Mhz Data 25Mhz	7.245e-03	8.176e-03	9.415e-03	9.703e-03
Clock 100Mhz Data 50Mhz	1.047e-02	1.232e-02	1.479e-02	1.536e-02
Clock = 0 Data 100Mhz	3.313e-03	3.419e-03	3.451e-03	3.468e-03
Clock = 1 Data 100Mhz	4.415e-05	4.437e-05	4.451e-05	4.457e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X30_P4	1.200	2.720	3.2640
X33_P4	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X30_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0443	0.0527	1.9111	0.9907
CP to QN ↑	0.0468	0.0494	3.2268	1.6404
	X30_P4	**X33_P4**	**X30_P4**	**X33_P4**

CP to QN ↓	0.0733	0.0735	0.5215	0.4738
CP to QN ↑	0.0614	0.0713	0.8937	0.8320

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X30_P4	X33_P4
CP ↓	min_pulse_width to CP	0.0519	0.0519	0.0567	0.0567
CP ↑	min_pulse_width to CP	0.0348	0.0406	0.0358	0.0406
D ↓	hold_rising to CP	0.0105	0.0101	0.0034	0.0056
D ↑	hold_rising to CP	0.0100	0.0131	0.0078	0.0078
D ↓	setup_rising to CP	0.0267	0.0264	0.0392	0.0364
D ↑	setup_rising to CP	0.0219	0.0222	0.0167	0.0171

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	4.980e-07	4.293e-12
X17_P4	5.824e-07	4.544e-12
X30_P4	8.247e-07	5.804e-12
X33_P4	8.699e-07	6.056e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

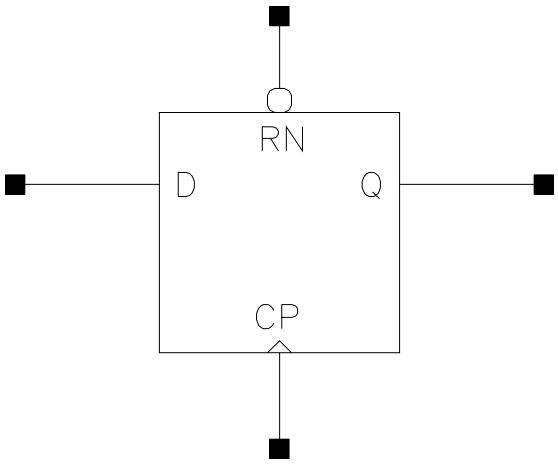
Pin Cycle	X8_P4	X17_P4	X30_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.867e-03	3.868e-03	3.940e-03	3.969e-03
Clock 100Mhz Data 25Mhz	6.847e-03	7.472e-03	9.722e-03	1.019e-02
Clock 100Mhz Data 50Mhz	9.828e-03	1.108e-02	1.550e-02	1.641e-02
Clock = 0 Data 100Mhz	2.910e-03	2.910e-03	3.115e-03	3.167e-03
Clock = 1 Data 100Mhz	4.434e-05	4.424e-05	4.453e-05	4.467e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0530	0.0658	0.9655	0.5828
CP to Q ↑	0.0601	0.0665	1.6468	0.9273
RN to Q ↓	0.0822	0.1069	1.0330	0.6262

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0604	0.0604
CP ↑	min_pulse_width to CP	0.0443	0.0540
D ↓	hold_rising to CP	0.0034	0.0034
D ↑	hold_rising to CP	0.0078	0.0078
D ↓	setup_rising to CP	0.0413	0.0413
D ↑	setup_rising to CP	0.0219	0.0219
RN ↓	min_pulse_width to RN	0.1045	0.1311
RN ↑	recovery_rising to CP	0.0219	0.0219
RN ↑	removal_rising to CP	-0.0073	-0.0073

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P4	6.953e-07	6.561e-12
X30_P4	8.230e-07	7.065e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

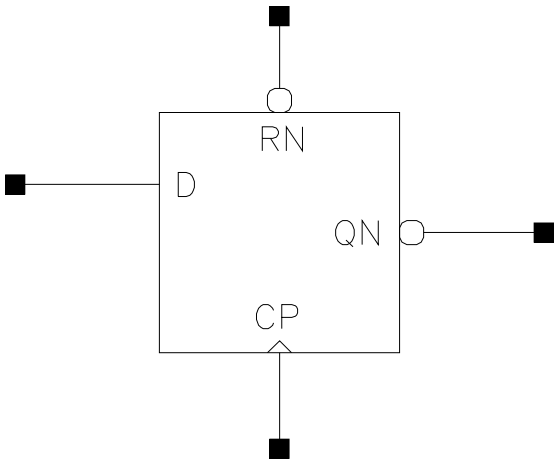
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	4.340e-03	4.336e-03
Clock 100Mhz Data 25Mhz	8.758e-03	9.962e-03
Clock 100Mhz Data 50Mhz	1.318e-02	1.559e-02
Clock = 0 Data 100Mhz	4.071e-03	4.074e-03
Clock = 1 Data 100Mhz	4.576e-05	4.586e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0010	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0705	0.0761	0.9005	0.5234
CP to QN ↑	0.0599	0.0646	1.6131	0.8987
RN to QN ↑	0.0879	0.0935	1.6155	0.9010

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0604	0.0604
CP ↑	min_pulse_width to CP	0.0358	0.0358
D ↓	hold_rising to CP	0.0034	0.0034
D ↑	hold_rising to CP	0.0078	0.0078
D ↓	setup_rising to CP	0.0413	0.0413
D ↑	setup_rising to CP	0.0219	0.0219
RN ↓	min_pulse_width to RN	0.0845	0.0894
RN ↑	recovery_rising to CP	0.0219	0.0223
RN ↑	removal_rising to CP	-0.0073	-0.0073

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P4	7.846e-07	6.561e-12
X30_P4	9.355e-07	7.065e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

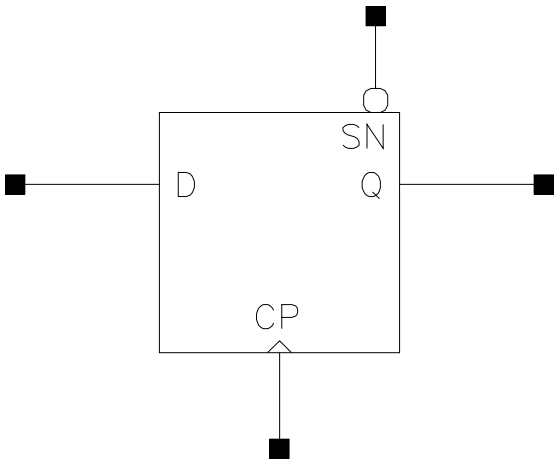
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	4.350e-03	4.356e-03
Clock 100Mhz Data 25Mhz	9.324e-03	1.052e-02
Clock 100Mhz Data 50Mhz	1.430e-02	1.669e-02
Clock = 0 Data 100Mhz	4.125e-03	4.111e-03
Clock = 1 Data 100Mhz	5.581e-05	5.590e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to Q ↓	0.0534	0.0669	0.9679	0.5798
CP to Q ↑	0.0596	0.0664	1.6484	0.9272
SN to Q ↑	0.0619	0.0701	1.6533	0.9308

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0653	0.0653
CP ↑	min_pulse_width to CP	0.0443	0.0540
D ↓	hold_rising to CP	0.0034	0.0034
D ↑	hold_rising to CP	0.0078	0.0078
D ↓	setup_rising to CP	0.0466	0.0466
D ↑	setup_rising to CP	0.0222	0.0222
SN ↓	min_pulse_width to SN	0.0593	0.0696
SN ↑	recovery_rising to CP	0.0103	0.0103
SN ↑	removal_rising to CP	0.0259	0.0259

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P4	7.343e-07	6.560e-12
X30_P4	8.865e-07	7.065e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

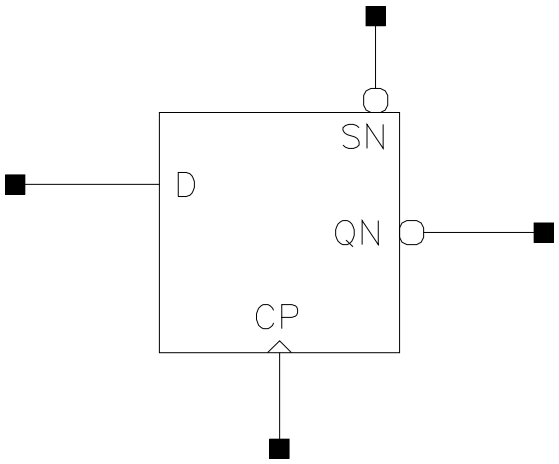
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	4.372e-03	4.362e-03
Clock 100Mhz Data 25Mhz	8.812e-03	1.002e-02
Clock 100Mhz Data 50Mhz	1.325e-02	1.568e-02
Clock = 0 Data 100Mhz	4.060e-03	4.059e-03
Clock = 1 Data 100Mhz	4.275e-05	4.285e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	3.128	3.7536
X30_P4	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P4	X30_P4
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P4	X30_P4	X17_P4	X30_P4
CP to QN ↓	0.0699	0.0755	0.9036	0.5247
CP to QN ↑	0.0604	0.0646	1.6082	0.8968
SN to QN ↓	0.0720	0.0778	0.9039	0.5246

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P4	X30_P4
CP ↓	min_pulse_width to CP	0.0653	0.0653
CP ↑	min_pulse_width to CP	0.0358	0.0358
D ↓	hold_rising to CP	0.0034	0.0034
D ↑	hold_rising to CP	0.0078	0.0078
D ↓	setup_rising to CP	0.0466	0.0466
D ↑	setup_rising to CP	0.0222	0.0219
SN ↓	min_pulse_width to SN	0.0566	0.0566
SN ↑	recovery_rising to CP	0.0103	0.0103
SN ↑	removal_rising to CP	0.0259	0.0259

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P4	7.522e-07	6.560e-12
X30_P4	8.766e-07	7.065e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

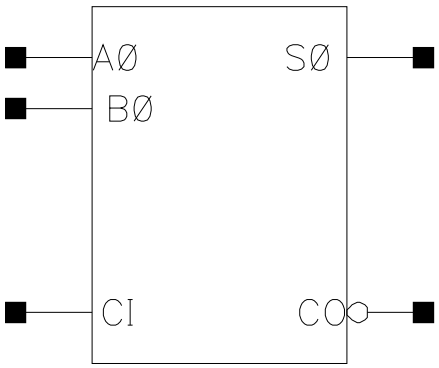
Pin Cycle	X17_P4	X30_P4
Clock 100Mhz Data 0Mhz	4.402e-03	4.398e-03
Clock 100Mhz Data 25Mhz	9.355e-03	1.053e-02
Clock 100Mhz Data 50Mhz	1.431e-02	1.666e-02
Clock = 0 Data 100Mhz	4.053e-03	4.055e-03
Clock = 1 Data 100Mhz	4.499e-05	4.498e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_FA1X8_P4	1.200	2.176	2.6112
C12T28SOI_LR_FA1X33_-P4	1.200	4.896	5.8752
C12T28SOI_LRS1_FA1X8_-P4	1.200	3.672	4.4064
C12T28SOI_LRS1_-FA1X33_P4	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LR_-FA1X8_P4	C12T28SOI_LR_-FA1X33_P4	C12T28SOI_LRS1_-FA1X8_P4	C12T28SOI_LRS1_-FA1X33_P4
A0	0.0032	0.0063	0.0028	0.0055
B0	0.0028	0.0062	0.0031	0.0053
CI	0.0021	0.0047	0.0021	0.0038

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-FA1X8_P4	**C12T28SOI_LR_-FA1X33_P4**	**C12T28SOI_LR_-FA1X8_P4**	**C12T28SOI_LR_-FA1X33_P4**
A0 to CO ↓	0.0533	0.0574	1.9246	0.5117
A0 to CO ↑	0.0349	0.0358	3.3277	0.8578
A0 to S0 ↓	0.0526	0.0658	1.8959	0.4993
A0 to S0 ↑	0.0538	0.0645	3.2984	0.8442
B0 to CO ↓	0.0518	0.0572	1.9333	0.5152
B0 to CO ↑	0.0356	0.0371	3.3296	0.8537
B0 to S0 ↓	0.0526	0.0665	1.8948	0.4991
B0 to S0 ↑	0.0534	0.0650	3.3001	0.8445
CI to CO ↓	0.0497	0.0551	1.9420	0.5152
CI to CO ↑	0.0354	0.0361	3.3284	0.8580
CI to S0 ↓	0.0517	0.0654	1.8942	0.4989
CI to S0 ↑	0.0530	0.0647	3.2990	0.8441
	C12T28SOI_LRS1_-FA1X8_P4	**C12T28SOI_LRS1_-FA1X33_P4**	**C12T28SOI_LRS1_-FA1X8_P4**	**C12T28SOI_LRS1_-FA1X33_P4**
A0 to CO ↓	0.0346	0.0421	3.7615	0.6540
A0 to CO ↑	0.0267	0.0304	3.3852	0.8447
A0 to S0 ↓	0.0691	0.0837	2.0506	0.5231
A0 to S0 ↑	0.0624	0.0672	3.4356	0.8620
B0 to CO ↓	0.0350	0.0428	3.7631	0.6541
B0 to CO ↑	0.0253	0.0295	3.3830	0.8447
B0 to S0 ↓	0.0693	0.0856	2.0499	0.5228
B0 to S0 ↑	0.0627	0.0691	3.4350	0.8624
CI to CO ↓	0.0338	0.0562	3.7551	0.6652
CI to CO ↑	0.0281	0.0332	3.4740	0.8509
CI to S0 ↓	0.0404	0.0517	2.0525	0.5233
CI to S0 ↑	0.0338	0.0339	3.4334	0.8621

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_FA1X8_P4	6.301e-07	4.796e-12
C12T28SOI_LR_FA1X33_P4	1.558e-06	9.848e-12
C12T28SOI_LRS1_FA1X8_P4	1.103e-06	7.570e-12
C12T28SOI_LRS1_FA1X33_P4	2.432e-06	1.563e-11

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-FA1X8_P4	C12T28SOI_LR_-FA1X33_P4	C12T28SOI_LRS1_-FA1X8_P4	C12T28SOI_LRS1_-FA1X33_P4
A0 to CO	3.765e-03	1.014e-02	5.687e-03	1.377e-02
A0 to S0	3.784e-03	1.051e-02	7.635e-03	1.711e-02
B0 to CO	3.670e-03	1.005e-02	5.732e-03	1.398e-02
B0 to S0	3.568e-03	1.018e-02	7.715e-03	1.738e-02
CI to CO	3.623e-03	9.962e-03	4.030e-03	1.211e-02
CI to S0	3.509e-03	1.007e-02	4.531e-03	1.304e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-FA1X8_P4	C12T28SOI_LR_-FA1X33_P4	C12T28SOI_LRS1_-FA1X8_P4	C12T28SOI_LRS1_-FA1X33_P4
A0 to CO	-2.758e-05	-5.369e-05	4.447e-06	9.850e-06

A0 to S0	-2.126e-05	-4.105e-05	7.235e-06	1.466e-05
B0 to CO	-8.253e-06	-1.524e-05	-8.512e-06	-1.783e-05
B0 to S0	3.134e-06	5.441e-06	-1.152e-05	-2.392e-05
CI to CO	1.445e-05	2.741e-05	-8.526e-07	-1.136e-06
CI to S0	4.091e-06	5.485e-06	-7.276e-07	4.684e-07

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X33_P4	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P4	X33_P4
A0	0.0011	0.0031
B0	0.0010	0.0027

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
A0 to CO ↓	0.0382	0.0354	1.8935	0.4707
A0 to CO ↑	0.0327	0.0298	3.2907	0.8480
A0 to S0 ↓	0.0484	0.0463	1.8541	0.4714
A0 to S0 ↑	0.0452	0.0493	3.2559	0.8370
B0 to CO ↓	0.0372	0.0330	1.8926	0.4672
B0 to CO ↑	0.0345	0.0306	3.2910	0.8479
B0 to S0 ↓	0.0492	0.0453	1.8537	0.4709
B0 to S0 ↑	0.0446	0.0473	3.2539	0.8366

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	3.211e-07	3.031e-12
X33_P4	1.145e-06	6.306e-12

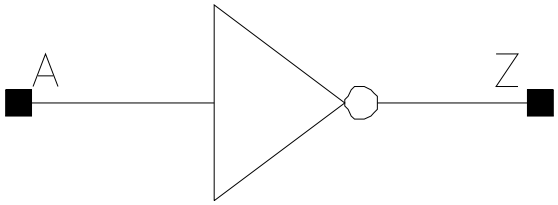
Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X33_P4
A0 to CO	2.852e-03	9.284e-03
A0 to S0	2.600e-03	8.814e-03
B0 to CO	2.831e-03	8.975e-03
B0 to S0	2.519e-03	8.260e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X8_P4	X33_P4
A0 to CO	-8.021e-06	-4.904e-05
A0 to S0	-5.030e-06	-2.960e-05
B0 to CO	6.983e-06	4.255e-05
B0 to S0	3.476e-06	2.094e-05

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.272	0.3264
X6_P4	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X13_P4	1.200	0.408	0.4896
X17_P4	1.200	0.408	0.4896
X21_P4	1.200	0.544	0.6528
X25_P4	1.200	0.544	0.6528
X29_P4	1.200	0.680	0.8160
X33_P4	1.200	0.680	0.8160
X50_P4	1.200	0.952	1.1424
X58_P4	1.200	1.088	1.3056
X67_P4	1.200	1.224	1.4688
X75_P4	1.200	1.360	1.6320
X84_P4	1.200	1.496	1.7952
X100_P4	1.200	1.768	2.1216
X134_P4	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X13_P4
A	0.0006	0.0007	0.0008	0.0013
	X17_P4	X21_P4	X25_P4	X29_P4
A	0.0016	0.0021	0.0023	0.0028
	X33_P4	X50_P4	X58_P4	X67_P4
A	0.0031	0.0047	0.0055	0.0064
	X75_P4	X84_P4	X100_P4	X134_P4

A	0.0072	0.0081	0.0099	0.0138

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0086	0.0080	3.5117	2.7203
A to Z ↑	0.0155	0.0144	6.3956	4.8358
	X8_P4	**X13_P4**	**X8_P4**	**X13_P4**
A to Z ↓	0.0071	0.0062	1.8603	1.2052
A to Z ↑	0.0132	0.0121	3.3451	2.2059
	X17_P4	**X21_P4**	**X17_P4**	**X21_P4**
A to Z ↓	0.0061	0.0066	0.9275	0.7458
A to Z ↑	0.0116	0.0122	1.6503	1.3268
	X25_P4	**X29_P4**	**X25_P4**	**X29_P4**
A to Z ↓	0.0065	0.0061	0.6379	0.5411
A to Z ↑	0.0119	0.0115	1.1105	0.9481
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0061	0.0062	0.4798	0.3247
A to Z ↑	0.0112	0.0112	0.8309	0.5575
	X58_P4	**X67_P4**	**X58_P4**	**X67_P4**
A to Z ↓	0.0066	0.0064	0.2820	0.2479
A to Z ↑	0.0116	0.0113	0.4805	0.4208
	X75_P4	**X84_P4**	**X75_P4**	**X84_P4**
A to Z ↓	0.0069	0.0069	0.2240	0.2026
A to Z ↑	0.0117	0.0117	0.3771	0.3416
	X100_P4	**X134_P4**	**X100_P4**	**X134_P4**
A to Z ↓	0.0076	0.0083	0.1730	0.1354
A to Z ↑	0.0122	0.0128	0.2882	0.2217

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	5.879e-08	1.268e-12
X6_P4	7.189e-08	1.268e-12
X8_P4	1.006e-07	1.267e-12
X13_P4	1.566e-07	1.519e-12
X17_P4	1.947e-07	1.518e-12
X21_P4	2.432e-07	1.770e-12
X25_P4	2.733e-07	1.770e-12
X29_P4	3.263e-07	2.022e-12
X33_P4	3.497e-07	2.022e-12
X50_P4	5.024e-07	2.523e-12
X58_P4	5.790e-07	2.780e-12
X67_P4	6.556e-07	3.039e-12
X75_P4	7.322e-07	3.284e-12
X84_P4	8.088e-07	3.539e-12
X100_P4	9.620e-07	4.037e-12
X134_P4	1.268e-06	5.046e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X13_P4

A to Z	4.245e-04	5.001e-04	6.105e-04	8.024e-04
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	9.879e-04	1.407e-03	1.591e-03	1.714e-03
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	1.852e-03	2.742e-03	3.457e-03	3.623e-03
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	4.318e-03	4.543e-03	5.486e-03	7.479e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

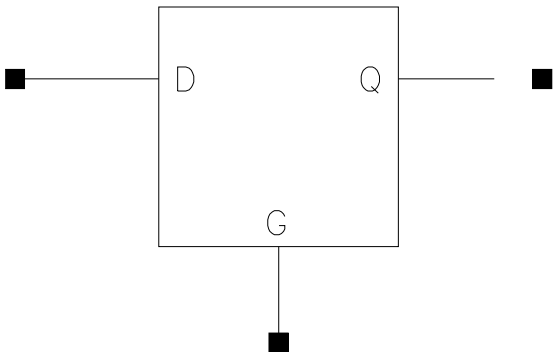
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X13_P4
A to Z	1.649e-07	3.113e-07	1.634e-06	1.809e-06
	X17_P4	X21_P4	X25_P4	X29_P4
A to Z	2.123e-07	8.562e-07	3.780e-07	1.401e-06
	X33_P4	X50_P4	X58_P4	X67_P4
A to Z	1.265e-06	5.330e-07	7.933e-06	6.940e-06
	X75_P4	X84_P4	X100_P4	X134_P4
A to Z	1.339e-05	4.900e-07	2.067e-06	1.161e-05

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X23_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P4	X23_P4
D	0.0005	0.0013
G	0.0012	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X23_P4	X8_P4	X23_P4
D to Q ↓	0.0591	0.0469	1.9561	0.9060
D to Q ↑	0.0346	0.0345	3.2442	0.8589
G to Q ↓	0.0594	0.0459	1.9509	0.9055
G to Q ↑	0.0336	0.0313	3.2454	0.8590

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P4	X23_P4
D ↓	hold_falling to G	-0.0162	-0.0064
D ↑	hold_falling to G	0.0001	0.0001
D ↓	setup_falling to G	0.0581	0.0410
D ↑	setup_falling to G	0.0351	0.0400
G ↑	min_pulse_width to G	0.0502	0.0428

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.926e-07	3.032e-12
X23_P4	5.501e-07	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X23_P4
D (output stable)	2.146e-05	9.264e-05
G (output stable)	9.364e-04	1.807e-03
D to Q	4.339e-03	8.344e-03
G to Q	3.969e-03	7.300e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

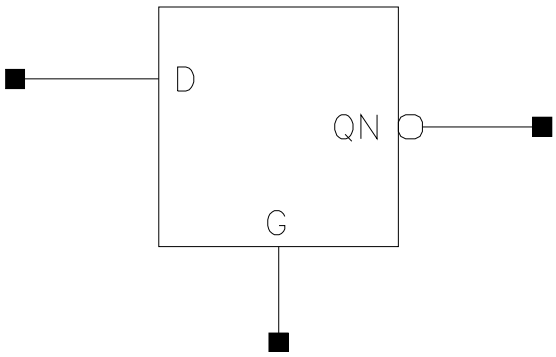
Pin Cycle (vdds)	X8_P4	X23_P4
D (output stable)	-2.133e-06	-7.807e-06
G (output stable)	-3.195e-08	2.493e-07
D to Q	-4.051e-06	-8.721e-06
G to Q	3.773e-05	2.265e-04

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P4	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P4
D	0.0006
G	0.0013

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P4	X17_P4
D to QN ↓	0.0459	0.9060
D to QN ↑	0.0643	1.6007
G to QN ↓	0.0442	0.9053
G to QN ↑	0.0623	1.6002

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X17_P4
D ↓	hold_falling to G	-0.0215
D ↑	hold_falling to G	-0.0054
D ↓	setup_falling to G	0.0459
D ↑	setup_falling to G	0.0303
G ↑	min_pulse_width to G	0.0395

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X17_P4	4.204e-07	3.284e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X17_P4
D (output stable)	4.070e-05
G (output stable)	1.040e-03
D to QN	5.564e-03
G to QN	5.043e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

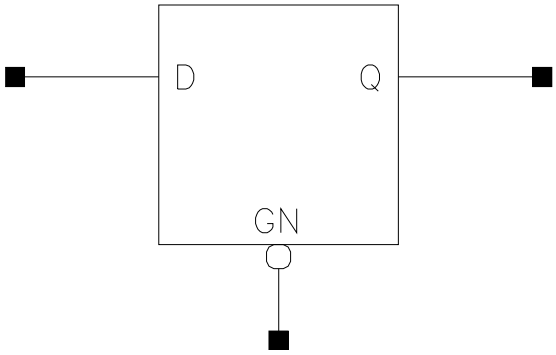
Pin Cycle (vdds)	X17_P4
D (output stable)	-8.909e-06
G (output stable)	5.802e-06
D to QN	-3.928e-06
G to QN	7.417e-05

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X33_P4	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
D	0.0005	0.0008	0.0017
GN	0.0011	0.0014	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D to Q ↓	0.0597	0.0521	1.9634	0.9601
D to Q ↑	0.0353	0.0329	3.2501	1.6659
GN to Q ↓	0.0532	0.0457	1.9657	0.9618
GN to Q ↑	0.0533	0.0511	3.2427	1.6623

	X33_P4		X33_P4	
D to Q ↓	0.0504		0.4903	
D to Q ↑	0.0286		0.8361	
GN to Q ↓	0.0434		0.4911	
GN to Q ↑	0.0405		0.8348	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X33_P4
D ↓	hold_rising to GN	-0.0213	-0.0140	-0.0140
D ↑	hold_rising to GN	0.0007	0.0029	0.0085
D ↓	setup_rising to GN	0.0659	0.0589	0.0536
D ↑	setup_rising to GN	0.0316	0.0285	0.0268
GN ↓	min_pulse_width to GN	0.0683	0.0626	0.0578

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.789e-07	3.033e-12
X17_P4	4.143e-07	3.536e-12
X33_P4	6.673e-07	4.545e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
D (output stable)	2.496e-05	4.299e-05	1.039e-04
GN (output stable)	9.340e-04	1.282e-03	1.491e-03
D to Q	4.345e-03	6.048e-03	9.858e-03
GN to Q	6.224e-03	8.412e-03	1.234e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

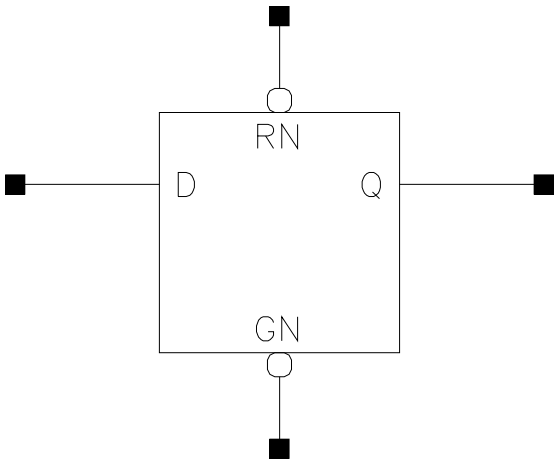
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
D (output stable)	-2.083e-06	-3.586e-06	-7.780e-06
GN (output stable)	-7.835e-08	2.400e-07	-1.931e-07
D to Q	-4.030e-06	-5.318e-06	-8.725e-06
GN to Q	-4.940e-05	-3.063e-05	-4.285e-05

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.496	1.7952
X33_P4	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P4	X33_P4
D	0.0006	0.0013
GN	0.0013	0.0023
RN	0.0005	0.0006

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X33_P4	X8_P4	X33_P4
D to Q ↓	0.0560	0.0507	1.9008	0.4944
D to Q ↑	0.0448	0.0552	3.3011	0.8594

GN to Q ↓	0.0504	0.0466	1.9011	0.4947
GN to Q ↑	0.0598	0.0603	3.3018	0.8583
RN to Q ↓	0.0430	0.0758	1.8256	0.5435
RN to Q ↑	0.0470	0.0599	3.2999	0.8594

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P4	X33_P4
D ↓	hold_rising to GN	-0.0189	-0.0140
D ↑	hold_rising to GN	-0.0068	-0.0188
D ↓	setup_rising to GN	0.0585	0.0536
D ↑	setup_rising to GN	0.0413	0.0582
GN ↓	min_pulse_width to GN	0.0636	0.0627
RN ↓	min_pulse_width to RN	0.0535	0.0920
RN ↑	recovery_rising to GN	0.0466	0.0655
RN ↑	removal_rising to GN	-0.0286	-0.0434

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.800e-07	3.536e-12
X33_P4	5.962e-07	5.303e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X33_P4
D (output stable)	9.087e-05	1.511e-04
GN (output stable)	1.091e-03	1.629e-03
RN (output stable)	2.201e-05	4.171e-05
D to Q	4.291e-03	1.049e-02
GN to Q	6.321e-03	1.353e-02
RN to Q	3.435e-03	7.988e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

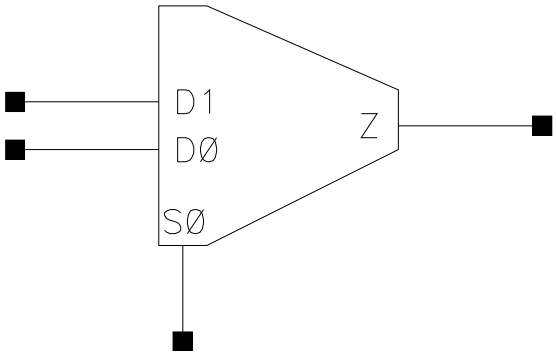
Pin Cycle (vdds)	X8_P4	X33_P4
D (output stable)	-6.338e-06	-1.757e-05
GN (output stable)	2.379e-06	8.630e-06
RN (output stable)	1.973e-06	2.315e-06
D to Q	-6.124e-06	-1.012e-05
GN to Q	-5.821e-05	9.318e-06
RN to Q	3.016e-06	-2.607e-05

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
D0	0.0007	0.0011	0.0014	0.0019
D1	0.0007	0.0010	0.0014	0.0019
S0	0.0013	0.0014	0.0016	0.0024

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
D0 to Z ↓	0.0452	0.0406	1.8924	0.9295
D0 to Z ↑	0.0331	0.0304	3.3328	1.6311
D1 to Z ↓	0.0433	0.0402	1.8882	0.9281
D1 to Z ↑	0.0304	0.0286	3.3275	1.6287
S0 to Z ↓	0.0383	0.0370	1.8829	0.9259
S0 to Z ↑	0.0354	0.0353	3.3274	1.6307

	X25_P4	X33_P4	X25_P4	X33_P4
D0 to Z ↓	0.0429	0.0391	0.6429	0.4816
D0 to Z ↑	0.0329	0.0302	1.0975	0.8208
D1 to Z ↓	0.0460	0.0408	0.6461	0.4822
D1 to Z ↑	0.0314	0.0290	1.0959	0.8216
S0 to Z ↓	0.0422	0.0388	0.6427	0.4811
S0 to Z ↑	0.0394	0.0361	1.0971	0.8218

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	3.208e-07	3.032e-12
X17_P4	5.182e-07	3.283e-12
X25_P4	7.304e-07	5.048e-12
X33_P4	9.741e-07	5.299e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	8.507e-04	1.216e-03	1.311e-03	1.738e-03
D1 (output stable)	6.815e-04	1.112e-03	1.480e-03	1.833e-03
S0 (output stable)	1.134e-03	1.285e-03	1.672e-03	2.036e-03
D0 to Z	3.019e-03	4.827e-03	7.436e-03	9.319e-03
D1 to Z	2.767e-03	4.668e-03	7.494e-03	9.198e-03
S0 to Z	3.465e-03	5.159e-03	8.352e-03	1.021e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

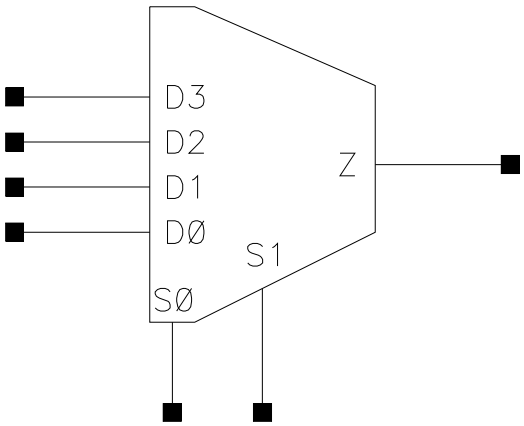
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
D0 (output stable)	3.120e-08	3.043e-07	-1.172e-07	1.466e-07
D1 (output stable)	2.994e-07	8.105e-08	2.040e-08	1.515e-07
S0 (output stable)	1.905e-07	1.379e-07	3.029e-07	1.350e-07
D0 to Z	-1.525e-07	-1.201e-07	-7.242e-07	-7.210e-07
D1 to Z	1.315e-07	2.680e-07	-5.365e-07	-8.630e-07
S0 to Z	-1.932e-08	-1.813e-07	-2.141e-07	-4.955e-08

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	2.312	2.7744
X31_P4	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P4	X31_P4
D0	0.0005	0.0014
D1	0.0005	0.0014
D2	0.0005	0.0014
D3	0.0006	0.0014
S0	0.0019	0.0037
S1	0.0012	0.0023

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X31_P4	X8_P4	X31_P4

D0 to Z ↓	0.0798	0.0816	1.9983	0.5569
D0 to Z ↑	0.0457	0.0474	3.3439	0.9010
D1 to Z ↓	0.0792	0.0818	1.9962	0.5572
D1 to Z ↑	0.0459	0.0472	3.3452	0.9010
D2 to Z ↓	0.0854	0.0766	2.0102	0.5513
D2 to Z ↑	0.0479	0.0438	3.3518	0.8950
D3 to Z ↓	0.0850	0.0760	2.0100	0.5505
D3 to Z ↑	0.0473	0.0451	3.3506	0.8986
S0 to Z ↓	0.0854	0.0859	1.9999	0.5532
S0 to Z ↑	0.0578	0.0603	3.3490	0.9001
S1 to Z ↓	0.0597	0.0585	2.0029	0.5538
S1 to Z ↑	0.0436	0.0441	3.3431	0.8983

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	3.852e-07	5.048e-12
X31_P4	1.078e-06	9.334e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X31_P4
D0 (output stable)	5.202e-05	2.182e-04
D1 (output stable)	5.304e-05	2.316e-04
D2 (output stable)	5.405e-05	1.651e-04
D3 (output stable)	4.751e-05	2.054e-04
S0 (output stable)	1.806e-03	4.265e-03
S1 (output stable)	1.104e-03	2.268e-03
D0 to Z	3.206e-03	1.065e-02
D1 to Z	3.200e-03	1.072e-02
D2 to Z	3.438e-03	9.987e-03
D3 to Z	3.427e-03	9.949e-03
S0 to Z	5.166e-03	1.489e-02
S1 to Z	3.470e-03	9.549e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

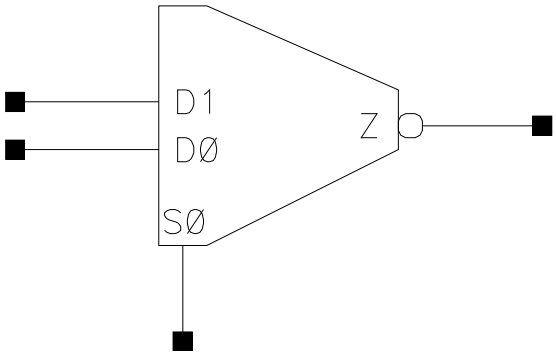
Pin Cycle (vdds)	X8_P4	X31_P4
D0 (output stable)	-5.600e-06	-2.238e-05
D1 (output stable)	-5.614e-06	-2.346e-05
D2 (output stable)	-7.961e-06	-2.229e-05
D3 (output stable)	-5.784e-06	-2.018e-05
S0 (output stable)	-3.274e-05	-1.142e-04
S1 (output stable)	2.068e-05	7.970e-05
D0 to Z	-5.324e-06	-2.021e-05
D1 to Z	-5.715e-06	-2.080e-05
D2 to Z	-5.467e-06	-1.688e-05
D3 to Z	-5.497e-06	-1.531e-05
S0 to Z	-2.515e-05	-8.523e-05
S1 to Z	2.059e-05	9.114e-05

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.816	0.9792
X5_P4	1.200	0.952	1.1424
X10_P4	1.200	1.768	2.1216
X16_P4	1.200	2.448	2.9376
X21_P4	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P4	X5_P4	X10_P4	X16_P4
D0	0.0005	0.0008	0.0016	0.0025
D1	0.0005	0.0008	0.0016	0.0024
S0	0.0011	0.0019	0.0025	0.0038
	X21_P4			
D0	0.0033			
D1	0.0032			
S0	0.0043			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X5_P4	X3_P4	X5_P4
D0 to Z ↓	0.0149	0.0148	6.0664	3.7854

D0 to Z ↑	0.0281	0.0257	14.8113	7.6188
D1 to Z ↓	0.0147	0.0142	6.0066	3.5792
D1 to Z ↑	0.0291	0.0269	14.8242	7.9024
S0 to Z ↓	0.0229	0.0192	6.0208	3.6722
S0 to Z ↑	0.0255	0.0211	14.8012	7.7599
	X10_P4	**X16_P4**	**X10_P4**	**X16_P4**
D0 to Z ↓	0.0164	0.0154	1.7828	1.1667
D0 to Z ↑	0.0278	0.0266	3.5563	2.3448
D1 to Z ↓	0.0149	0.0148	1.7185	1.1364
D1 to Z ↑	0.0279	0.0273	3.6101	2.3673
S0 to Z ↓	0.0232	0.0202	1.7473	1.1502
S0 to Z ↑	0.0248	0.0216	3.5830	2.3566
	X21_P4		**X21_P4**	
D0 to Z ↓	0.0152		0.8927	
D0 to Z ↑	0.0261		1.7768	
D1 to Z ↓	0.0148		0.8634	
D1 to Z ↑	0.0274		1.7672	
S0 to Z ↓	0.0212		0.8766	
S0 to Z ↑	0.0222		1.7712	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P4	1.403e-07	2.276e-12
X5_P4	2.580e-07	2.528e-12
X10_P4	4.536e-07	4.040e-12
X16_P4	6.932e-07	5.299e-12
X21_P4	8.579e-07	6.559e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	2.591e-05	5.549e-05	1.988e-04	2.843e-04
D1 (output stable)	4.188e-05	1.959e-04	2.278e-04	3.513e-04
S0 (output stable)	9.483e-04	1.332e-03	2.369e-03	3.615e-03
D0 to Z	9.470e-04	1.577e-03	3.914e-03	5.499e-03
D1 to Z	9.461e-04	1.567e-03	3.728e-03	5.426e-03
S0 to Z	1.623e-03	2.248e-03	4.760e-03	6.568e-03
	X21_P4			
D0 (output stable)	3.774e-04			
D1 (output stable)	5.068e-04			
S0 (output stable)	4.056e-03			
D0 to Z	7.044e-03			
D1 to Z	7.185e-03			
S0 to Z	8.066e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X3_P4	X5_P4	X10_P4	X16_P4
D0 (output stable)	-2.318e-06	-4.246e-06	-1.022e-05	-2.114e-05
D1 (output stable)	-9.515e-06	-4.309e-05	-3.923e-05	-6.251e-05
S0 (output stable)	6.470e-06	3.460e-05	2.620e-05	3.715e-05
D0 to Z	-1.684e-06	-2.514e-06	-6.269e-06	-1.387e-05

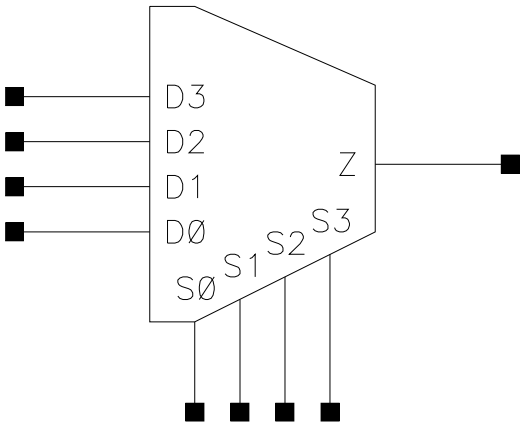
D1 to Z	-1.829e-06	-5.399e-06	-7.715e-06	-1.182e-05
S0 to Z	6.797e-06	1.335e-05	2.822e-05	6.039e-05
	X21_P4			
D0 (output stable)	-2.638e-05			
D1 (output stable)	-1.032e-04			
S0 (output stable)	6.529e-05			
D0 to Z	-1.630e-05			
D1 to Z	-1.914e-05			
S0 to Z	6.937e-05			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	1.768	2.1216
X27_P4	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P4	X27_P4
D0	0.0006	0.0019
D1	0.0007	0.0020
D2	0.0006	0.0019
D3	0.0007	0.0020
S0	0.0006	0.0018
S1	0.0007	0.0019
S2	0.0007	0.0018
S3	0.0007	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	X27_P4	X7_P4	X27_P4
D0 to Z ↓	0.0601	0.0507	3.1302	0.8648
D0 to Z ↑	0.0386	0.0327	3.2631	0.8153
D1 to Z ↓	0.0543	0.0459	3.1276	0.8643
D1 to Z ↑	0.0354	0.0294	3.2545	0.8125
D2 to Z ↓	0.0602	0.0483	3.1423	0.8665
D2 to Z ↑	0.0379	0.0307	3.2774	0.8183
D3 to Z ↓	0.0545	0.0434	3.1351	0.8655
D3 to Z ↑	0.0348	0.0274	3.2690	0.8157
S0 to Z ↓	0.0581	0.0482	3.1307	0.8636
S0 to Z ↑	0.0406	0.0340	3.2648	0.8156
S1 to Z ↓	0.0527	0.0433	3.1257	0.8632
S1 to Z ↑	0.0372	0.0303	3.2535	0.8130
S2 to Z ↓	0.0583	0.0457	3.1394	0.8662
S2 to Z ↑	0.0399	0.0320	3.2775	0.8193
S3 to Z ↓	0.0530	0.0408	3.1335	0.8647
S3 to Z ↑	0.0365	0.0283	3.2677	0.8161

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X7_P4	3.286e-07	4.040e-12
X27_P4	1.143e-06	7.569e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X7_P4	X27_P4
D0 (output stable)	5.235e-04	1.638e-03
D1 (output stable)	4.048e-04	1.222e-03
D2 (output stable)	5.225e-04	1.622e-03
D3 (output stable)	3.824e-04	1.143e-03
S0 (output stable)	5.406e-04	1.644e-03
S1 (output stable)	4.004e-04	1.198e-03
S2 (output stable)	4.900e-04	1.463e-03
S3 (output stable)	3.627e-04	1.049e-03
D0 to Z	3.941e-03	1.209e-02
D1 to Z	3.447e-03	1.039e-02
D2 to Z	3.801e-03	1.047e-02
D3 to Z	3.312e-03	8.752e-03
S0 to Z	3.837e-03	1.146e-02
S1 to Z	3.338e-03	9.787e-03
S2 to Z	3.693e-03	9.824e-03
S3 to Z	3.202e-03	8.148e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

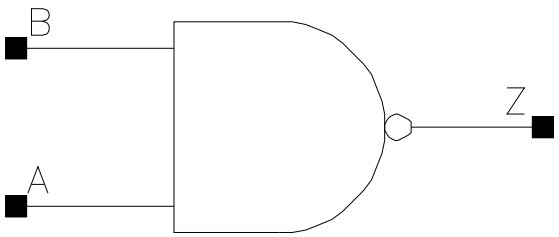
Pin Cycle (vdds)	X7_P4	X27_P4
D0 (output stable)	-4.078e-06	-1.153e-05
D1 (output stable)	2.709e-07	1.785e-06
D2 (output stable)	-9.695e-06	-2.668e-05
D3 (output stable)	7.707e-06	2.354e-05
S0 (output stable)	-8.982e-06	-2.427e-05
S1 (output stable)	7.062e-06	2.119e-05
S2 (output stable)	-5.663e-06	-1.542e-05
S3 (output stable)	2.340e-06	8.068e-06
D0 to Z	-7.147e-06	-1.647e-05
D1 to Z	-2.663e-07	-2.746e-07
D2 to Z	-7.218e-06	-1.693e-05
D3 to Z	1.696e-08	-6.352e-07
S0 to Z	-7.700e-06	-1.854e-05
S1 to Z	-1.870e-07	-2.143e-07
S2 to Z	-6.861e-06	-1.699e-05
S3 to Z	-4.847e-08	-4.209e-07

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND2X3_P4	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X5_P4	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X7_P4	1.200	0.408	0.4896
C12T28SOI_LR_-NAND2X10_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X13_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND2X17_P4	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X20_P4	1.200	0.952	1.1424
C12T28SOI_LR_-NAND2X24_P4	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X27_P4	1.200	1.224	1.4688
C12T28SOI_LR_-NAND2X42_P4	1.200	1.360	1.6320
C12T28SOI_LR_-NAND2X47_P4	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X50_P4	1.200	1.496	1.7952
C12T28SOI_LR_-NAND2X58_P4	1.200	1.632	1.9584
C12T28SOI_LR_-NAND2X67_P4	1.200	1.768	2.1216
C12T28SOI_LRBR0D8_-NAND2X7_P4	1.200	0.952	1.1424
C12T28SOI_LRBR0D8_-NAND2X14_P4	1.200	1.224	1.4688

C12T28SOI_LRS_-NAND2X40_P4	1.200	1.768	2.1216
C12T28SOI_LRS_-NAND2X54_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND2X3_P4	C12T28SOI_LR_-NAND2X5_P4	C12T28SOI_LR_-NAND2X7_P4	C12T28SOI_LR_-NAND2X10_P4
A	0.0005	0.0007	0.0008	0.0013
B	0.0006	0.0007	0.0008	0.0012
	C12T28SOI_LR_-NAND2X13_P4	C12T28SOI_LR_-NAND2X17_P4	C12T28SOI_LR_-NAND2X20_P4	C12T28SOI_LR_-NAND2X24_P4
A	0.0016	0.0021	0.0024	0.0029
B	0.0015	0.0020	0.0022	0.0027
	C12T28SOI_LR_-NAND2X27_P4	C12T28SOI_LR_-NAND2X42_P4	C12T28SOI_LR_-NAND2X47_P4	C12T28SOI_LR_-NAND2X50_P4
A	0.0032	0.0010	0.0010	0.0010
B	0.0030	0.0010	0.0010	0.0010
	C12T28SOI_LR_-NAND2X58_P4	C12T28SOI_LR_-NAND2X67_P4	C12T28SOI_-LRBR0D8_-NAND2X7_P4	C12T28SOI_-LRBR0D8_-NAND2X14_P4
A	0.0010	0.0010	0.0008	0.0016
B	0.0010	0.0010	0.0008	0.0015
	C12T28SOI_LRS_-NAND2X40_P4	C12T28SOI_LRS_-NAND2X54_P4		
A	0.0048	0.0064		
B	0.0045	0.0060		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND2X3_P4	**C12T28SOI_LR_-NAND2X5_P4**	**C12T28SOI_LR_-NAND2X3_P4**	**C12T28SOI_LR_-NAND2X5_P4**
A to Z ↓	0.0117	0.0106	5.9082	3.8035
A to Z ↑	0.0181	0.0167	6.4161	4.1162
B to Z ↓	0.0119	0.0104	5.9916	3.8688
B to Z ↑	0.0166	0.0148	6.4585	4.1447
	C12T28SOI_LR_-NAND2X7_P4	**C12T28SOI_LR_-NAND2X10_P4**	**C12T28SOI_LR_-NAND2X7_P4**	**C12T28SOI_LR_-NAND2X10_P4**
A to Z ↓	0.0105	0.0121	3.2068	2.1375
A to Z ↑	0.0162	0.0173	3.3283	2.1787
B to Z ↓	0.0103	0.0103	3.2423	2.1684
B to Z ↑	0.0143	0.0143	3.3597	2.1977
	C12T28SOI_LR_-NAND2X13_P4	**C12T28SOI_LR_-NAND2X17_P4**	**C12T28SOI_LR_-NAND2X13_P4**	**C12T28SOI_LR_-NAND2X17_P4**
A to Z ↓	0.0117	0.0115	1.6495	1.3094

A to Z ↑	0.0165	0.0166	1.6365	1.3181
B to Z ↓	0.0099	0.0103	1.6726	1.3261
B to Z ↑	0.0136	0.0140	1.6494	1.3283
	C12T28SOI_LR_-NAND2X20_P4	**C12T28SOI_LR_-NAND2X24_P4**	**C12T28SOI_LR_-NAND2X20_P4**	**C12T28SOI_LR_-NAND2X24_P4**
A to Z ↓	0.0113	0.0117	1.1320	0.9638
A to Z ↑	0.0162	0.0165	1.1024	0.9400
B to Z ↓	0.0103	0.0100	1.1460	0.9776
B to Z ↑	0.0137	0.0135	1.1130	0.9476
	C12T28SOI_LR_-NAND2X27_P4	**C12T28SOI_LR_-NAND2X42_P4**	**C12T28SOI_LR_-NAND2X27_P4**	**C12T28SOI_LR_-NAND2X42_P4**
A to Z ↓	0.0115	0.0386	0.8600	0.3806
A to Z ↑	0.0161	0.0418	0.8267	0.6509
B to Z ↓	0.0098	0.0394	0.8718	0.3807
B to Z ↑	0.0131	0.0403	0.8339	0.6518
	C12T28SOI_LR_-NAND2X47_P4	**C12T28SOI_LR_-NAND2X50_P4**	**C12T28SOI_LR_-NAND2X47_P4**	**C12T28SOI_LR_-NAND2X50_P4**
A to Z ↓	0.0396	0.0399	0.3383	0.3178
A to Z ↑	0.0423	0.0425	0.5661	0.5438
B to Z ↓	0.0404	0.0408	0.3381	0.3180
B to Z ↑	0.0408	0.0411	0.5655	0.5439
	C12T28SOI_LR_-NAND2X58_P4	**C12T28SOI_LR_-NAND2X67_P4**	**C12T28SOI_LR_-NAND2X58_P4**	**C12T28SOI_LR_-NAND2X67_P4**
A to Z ↓	0.0418	0.0431	0.2758	0.2431
A to Z ↑	0.0439	0.0447	0.4679	0.4110
B to Z ↓	0.0427	0.0439	0.2757	0.2431
B to Z ↑	0.0425	0.0432	0.4675	0.4112
	C12T28SOI_-LRBR0D8_-NAND2X7_P4	**C12T28SOI_-LRBR0D8_-NAND2X14_P4**	**C12T28SOI_-LRBR0D8_-NAND2X7_P4**	**C12T28SOI_-LRBR0D8_-NAND2X14_P4**
A to Z ↓	0.0091	0.0102	2.4150	1.2814
A to Z ↑	0.0190	0.0194	4.4189	2.1603
B to Z ↓	0.0082	0.0077	2.4626	1.3118
B to Z ↑	0.0163	0.0148	4.5709	2.2062
	C12T28SOI_LRS_-NAND2X40_P4	**C12T28SOI_LRS_-NAND2X54_P4**	**C12T28SOI_LRS_-NAND2X40_P4**	**C12T28SOI_LRS_-NAND2X54_P4**
A to Z ↓	0.0115	0.0115	0.5839	0.4424
A to Z ↑	0.0160	0.0161	0.5541	0.4181
B to Z ↓	0.0099	0.0101	0.5933	0.4486
B to Z ↑	0.0131	0.0133	0.5594	0.4220

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_NAND2X3_P4	6.601e-08	1.520e-12
C12T28SOI_LR_NAND2X5_P4	9.936e-08	1.520e-12
C12T28SOI_LR_NAND2X7_P4	1.164e-07	1.520e-12
C12T28SOI_LR_NAND2X10_P4	1.721e-07	2.024e-12
C12T28SOI_LR_NAND2X13_P4	2.181e-07	2.024e-12
C12T28SOI_LR_NAND2X17_P4	2.753e-07	2.528e-12
C12T28SOI_LR_NAND2X20_P4	3.143e-07	2.528e-12
C12T28SOI_LR_NAND2X24_P4	3.782e-07	3.032e-12
C12T28SOI_LR_NAND2X27_P4	4.108e-07	3.032e-12

C12T28SOI_LR_NAND2X42_P4	7.075e-07	3.283e-12
C12T28SOI_LR_NAND2X47_P4	7.943e-07	3.533e-12
C12T28SOI_LR_NAND2X50_P4	7.921e-07	3.533e-12
C12T28SOI_LR_NAND2X58_P4	8.767e-07	3.782e-12
C12T28SOI_LR_NAND2X67_P4	9.613e-07	4.037e-12
C12T28SOI_LRBR0D8_NAND2X7_P4	1.291e-07	2.774e-12
C12T28SOI_LRBR0D8_NAND2X14_-P4	2.394e-07	3.304e-12
C12T28SOI_LRS_NAND2X40_P4	6.039e-07	4.041e-12
C12T28SOI_LRS_NAND2X54_P4	7.971e-07	5.052e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND2X3_P4	C12T28SOI_LR_-NAND2X5_P4	C12T28SOI_LR_-NAND2X7_P4	C12T28SOI_LR_-NAND2X10_P4
A (output stable)	1.399e-05	2.150e-05	2.528e-05	6.222e-05
B (output stable)	3.993e-05	6.222e-05	7.489e-05	3.309e-04
A to Z	6.353e-04	8.362e-04	9.819e-04	1.768e-03
B to Z	5.163e-04	6.424e-04	7.520e-04	1.161e-03
	C12T28SOI_LR_-NAND2X13_P4	C12T28SOI_LR_-NAND2X17_P4	C12T28SOI_LR_-NAND2X20_P4	C12T28SOI_LR_-NAND2X24_P4
A (output stable)	7.501e-05	9.933e-05	1.117e-04	1.404e-04
B (output stable)	3.796e-04	3.909e-04	4.477e-04	6.401e-04
A to Z	2.141e-03	2.698e-03	3.053e-03	3.753e-03
B to Z	1.402e-03	1.863e-03	2.116e-03	2.470e-03
	C12T28SOI_LR_-NAND2X27_P4	C12T28SOI_LR_-NAND2X42_P4	C12T28SOI_LR_-NAND2X47_P4	C12T28SOI_LR_-NAND2X50_P4
A (output stable)	1.540e-04	2.747e-05	2.763e-05	2.756e-05
B (output stable)	6.868e-04	8.110e-05	8.079e-05	8.134e-05
A to Z	4.038e-03	1.064e-02	1.144e-02	1.171e-02
B to Z	2.614e-03	1.040e-02	1.120e-02	1.147e-02
	C12T28SOI_LR_-NAND2X58_P4	C12T28SOI_LR_-NAND2X67_P4	C12T28SOI_-LRBR0D8_-NAND2X7_P4	C12T28SOI_-LRBR0D8_-NAND2X14_P4
A (output stable)	2.760e-05	2.780e-05	3.255e-05	9.202e-05
B (output stable)	8.179e-05	8.114e-05	9.933e-05	4.848e-04
A to Z	1.325e-02	1.436e-02	1.026e-03	2.229e-03
B to Z	1.301e-02	1.412e-02	7.104e-04	1.248e-03
	C12T28SOI_LRS_-NAND2X40_P4	C12T28SOI_LRS_-NAND2X54_P4		
A (output stable)	2.311e-04	2.975e-04		
B (output stable)	9.601e-04	1.243e-03		
A to Z	5.972e-03	7.930e-03		
B to Z	3.889e-03	5.245e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND2X3_P4	C12T28SOI_LR_-NAND2X5_P4	C12T28SOI_LR_-NAND2X7_P4	C12T28SOI_LR_-NAND2X10_P4
A (output stable)	6.870e-08	4.530e-08	3.299e-08	3.684e-07
B (output stable)	3.640e-08	1.620e-08	-7.170e-09	-2.373e-06
A to Z	8.750e-08	-9.970e-08	1.698e-07	-2.886e-07
B to Z	2.822e-07	7.120e-08	6.960e-08	8.000e-08

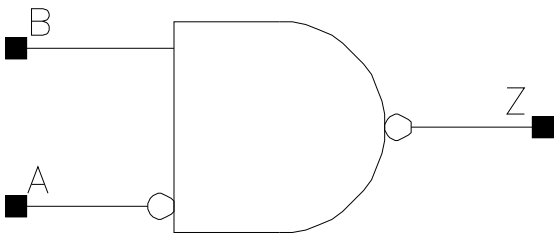
	C12T28SOI_LR_-NAND2X13_P4	C12T28SOI_LR_-NAND2X17_P4	C12T28SOI_LR_-NAND2X20_P4	C12T28SOI_LR_-NAND2X24_P4
A (output stable)	3.480e-07	2.901e-07	-8.280e-08	5.507e-07
B (output stable)	-2.365e-06	-2.140e-06	-1.052e-07	-4.326e-06
A to Z	3.920e-07	2.900e-07	4.880e-07	8.080e-07
B to Z	-4.090e-07	1.150e-07	-1.268e-06	-7.360e-07
	C12T28SOI_LR_-NAND2X27_P4	C12T28SOI_LR_-NAND2X42_P4	C12T28SOI_LR_-NAND2X47_P4	C12T28SOI_LR_-NAND2X50_P4
A (output stable)	4.627e-07	3.769e-08	3.801e-08	3.825e-08
B (output stable)	-3.991e-06	8.300e-10	1.270e-09	1.560e-09
A to Z	7.960e-07	-5.540e-07	-3.630e-07	-5.280e-07
B to Z	-2.820e-07	-1.610e-07	-2.500e-07	-4.050e-07
	C12T28SOI_LR_-NAND2X58_P4	C12T28SOI_LR_-NAND2X67_P4	C12T28SOI_-LRBR0D8_-NAND2X7_P4	C12T28SOI_-LRBR0D8_-NAND2X14_P4
A (output stable)	3.876e-08	3.901e-08	4.421e-08	1.421e-06
B (output stable)	1.870e-09	2.250e-09	2.268e-08	-9.242e-06
A to Z	-1.136e-06	-5.190e-07	8.031e-07	3.770e-07
B to Z	-1.095e-06	-1.202e-06	1.333e-07	1.577e-06
	C12T28SOI_LRS_-NAND2X40_P4	C12T28SOI_LRS_-NAND2X54_P4		
A (output stable)	5.267e-07	7.480e-07		
B (output stable)	-5.180e-06	-7.338e-06		
A to Z	1.083e-06	2.977e-06		
B to Z	-2.490e-07	-1.159e-06		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X7_P4	1.200	0.544	0.6528
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X40_P4	1.200	2.312	2.7744
X54_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P4	X7_P4	X13_P4	X27_P4
A	0.0008	0.0008	0.0010	0.0019
B	0.0006	0.0008	0.0015	0.0030
	X40_P4	X54_P4		
A	0.0029	0.0038		
B	0.0044	0.0059		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0309	0.0326	5.8642	3.1821
A to Z ↑	0.0228	0.0236	6.2354	3.2832
B to Z ↓	0.0122	0.0103	6.0482	3.2688
B to Z ↑	0.0167	0.0143	6.4590	3.3902
	X13_P4	**X27_P4**	**X13_P4**	**X27_P4**

A to Z ↓	0.0304	0.0297	1.7234	0.8600
A to Z ↑	0.0223	0.0219	1.6889	0.8171
B to Z ↓	0.0097	0.0097	1.7761	0.8856
B to Z ↑	0.0134	0.0131	1.6887	0.8351
	X40_P4	**X54_P4**	**X40_P4**	**X54_P4**
A to Z ↓	0.0301	0.0299	0.5737	0.4358
A to Z ↑	0.0223	0.0221	0.5442	0.4112
B to Z ↓	0.0097	0.0098	0.5906	0.4487
B to Z ↑	0.0130	0.0130	0.5616	0.4244

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P4	1.152e-07	1.772e-12
X7_P4	1.650e-07	1.772e-12
X13_P4	3.230e-07	2.528e-12
X27_P4	5.971e-07	3.789e-12
X40_P4	8.673e-07	5.051e-12
X54_P4	1.137e-06	6.310e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	1.011e-03	1.284e-03	2.115e-03	4.122e-03
B (output stable)	4.050e-05	7.507e-05	3.588e-04	6.376e-04
A to Z	1.735e-03	2.388e-03	4.353e-03	8.528e-03
B to Z	5.243e-04	7.494e-04	1.358e-03	2.633e-03
	X40_P4	X54_P4		
A (output stable)	6.322e-03	8.186e-03		
B (output stable)	9.330e-04	1.233e-03		
A to Z	1.282e-02	1.677e-02		
B to Z	3.850e-03	5.105e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

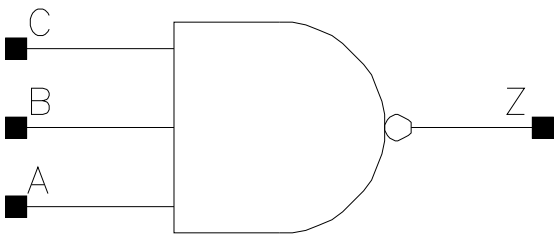
Pin Cycle (vdds)	X3_P4	X7_P4	X13_P4	X27_P4
A (output stable)	2.070e-07	2.520e-08	1.465e-07	2.387e-06
B (output stable)	3.630e-08	-8.750e-09	-3.880e-08	-2.677e-06
A to Z	6.704e-08	-2.680e-08	-9.020e-08	2.730e-07
B to Z	1.402e-07	1.540e-08	6.430e-07	1.665e-06
	X40_P4	X54_P4		
A (output stable)	3.637e-06	5.818e-06		
B (output stable)	-4.003e-06	-6.484e-06		
A to Z	4.040e-07	4.700e-07		
B to Z	-1.020e-07	-8.500e-08		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-NAND3X4_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X6_P4	1.200	0.680	0.8160
C12T28SOI_LR_-NAND3X9_P4	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X12_P4	1.200	1.088	1.3056
C12T28SOI_LR_-NAND3X15_P4	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X18_P4	1.200	1.360	1.6320
C12T28SOI_LR_-NAND3X21_P4	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X24_P4	1.200	1.904	2.2848
C12T28SOI_LR_-NAND3X35_P4	1.200	2.720	3.2640
C12T28SOI_LR_-NAND3X47_P4	1.200	3.536	4.2432
C12T28SOI_LRBR0P6_-NAND3X6_P4	1.200	1.224	1.4688
C12T28SOI_LRBR0P6_-NAND3X12_P4	1.200	1.632	1.9584
C12T28SOI_LRBR0P6_-NAND3X18_P4	1.200	1.904	2.2848
C12T28SOI_LRBR0P6_-NAND3X24_P4	1.200	2.448	2.9376
C12T28SOI_LRBR0P6_-NAND3X35_P4	1.200	3.264	3.9168
C12T28SOI_LRBR0P6_-NAND3X47_P4	1.200	4.080	4.8960

C12T28SOIDV_LRBR0P6_-NAND3X18_P4	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A	0.0007	0.0008	0.0013	0.0016
B	0.0007	0.0008	0.0013	0.0015
C	0.0006	0.0008	0.0012	0.0015
	C12T28SOI_LR_-NAND3X15_P4	C12T28SOI_LR_-NAND3X18_P4	C12T28SOI_LR_-NAND3X21_P4	C12T28SOI_LR_-NAND3X24_P4
A	0.0021	0.0024	0.0029	0.0032
B	0.0020	0.0023	0.0027	0.0030
C	0.0019	0.0022	0.0026	0.0029
	C12T28SOI_LR_-NAND3X35_P4	C12T28SOI_LR_-NAND3X47_P4	C12T28SOI_-LRBR0P6_-NAND3X6_P4	C12T28SOI_-LRBR0P6_-NAND3X12_P4
A	0.0048	0.0063	0.0008	0.0016
B	0.0045	0.0061	0.0009	0.0015
C	0.0044	0.0058	0.0008	0.0015
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	C12T28SOI_-LRBR0P6_-NAND3X24_P4	C12T28SOI_-LRBR0P6_-NAND3X35_P4	C12T28SOI_-LRBR0P6_-NAND3X47_P4
A	0.0024	0.0032	0.0047	0.0064
B	0.0022	0.0030	0.0044	0.0059
C	0.0021	0.0029	0.0043	0.0057
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4			
A	0.0024			
B	0.0023			
C	0.0022			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4
A to Z ↓	0.0176	0.0161	6.2853	4.5019
A to Z ↑	0.0224	0.0205	4.6771	3.2330
B to Z ↓	0.0186	0.0167	6.3093	4.5206
B to Z ↑	0.0215	0.0194	4.6882	3.2417
C to Z ↓	0.0162	0.0146	6.3437	4.5459
C to Z ↑	0.0188	0.0170	4.6906	3.2633

	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A to Z ↓	0.0178	0.0168	3.0662	2.3951
A to Z ↑	0.0215	0.0203	2.1935	1.6549
B to Z ↓	0.0170	0.0162	3.0783	2.4031
B to Z ↑	0.0197	0.0186	2.1996	1.6597
C to Z ↓	0.0147	0.0139	3.0983	2.4191
C to Z ↑	0.0169	0.0159	2.1919	1.6465
	C12T28SOI_LR_-NAND3X15_P4	**C12T28SOI_LR_-NAND3X18_P4**	**C12T28SOI_LR_-NAND3X15_P4**	**C12T28SOI_LR_-NAND3X18_P4**
A to Z ↓	0.0162	0.0159	1.9262	1.6601
A to Z ↑	0.0199	0.0194	1.3174	1.0994
B to Z ↓	0.0161	0.0159	1.9366	1.6683
B to Z ↑	0.0182	0.0178	1.3215	1.1030
C to Z ↓	0.0141	0.0138	1.9474	1.6778
C to Z ↑	0.0158	0.0153	1.3316	1.1116
	C12T28SOI_LR_-NAND3X21_P4	**C12T28SOI_LR_-NAND3X24_P4**	**C12T28SOI_LR_-NAND3X21_P4**	**C12T28SOI_LR_-NAND3X24_P4**
A to Z ↓	0.0167	0.0165	1.4043	1.2566
A to Z ↑	0.0201	0.0197	0.9455	0.8325
B to Z ↓	0.0163	0.0160	1.4101	1.2617
B to Z ↑	0.0184	0.0180	0.9479	0.8346
C to Z ↓	0.0141	0.0139	1.4195	1.2699
C to Z ↑	0.0157	0.0154	0.9496	0.8353
	C12T28SOI_LR_-NAND3X35_P4	**C12T28SOI_LR_-NAND3X47_P4**	**C12T28SOI_LR_-NAND3X35_P4**	**C12T28SOI_LR_-NAND3X47_P4**
A to Z ↓	0.0158	0.0162	0.8586	0.6542
A to Z ↑	0.0192	0.0195	0.5578	0.4215
B to Z ↓	0.0157	0.0160	0.8626	0.6574
B to Z ↑	0.0175	0.0177	0.5584	0.4208
C to Z ↓	0.0136	0.0140	0.8699	0.6617
C to Z ↑	0.0149	0.0151	0.5621	0.4232
	C12T28SOI_-LRBR0P6_-NAND3X6_P4	**C12T28SOI_-LRBR0P6_-NAND3X12_P4**	**C12T28SOI_-LRBR0P6_-NAND3X6_P4**	**C12T28SOI_-LRBR0P6_-NAND3X12_P4**
A to Z ↓	0.0133	0.0139	3.0542	1.6184
A to Z ↑	0.0273	0.0272	5.0763	2.5952
B to Z ↓	0.0133	0.0126	3.0821	1.6353
B to Z ↑	0.0249	0.0236	5.0935	2.6029
C to Z ↓	0.0104	0.0094	3.1241	1.6574
C to Z ↑	0.0200	0.0182	5.1193	2.6112
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	**C12T28SOI_-LRBR0P6_-NAND3X24_P4**	**C12T28SOI_-LRBR0P6_-NAND3X18_P4**	**C12T28SOI_-LRBR0P6_-NAND3X24_P4**
A to Z ↓	0.0130	0.0135	1.1234	0.8486
A to Z ↑	0.0259	0.0264	1.7263	1.3047
B to Z ↓	0.0124	0.0123	1.1337	0.8567
B to Z ↑	0.0225	0.0229	1.7322	1.3084
C to Z ↓	0.0096	0.0094	1.1498	0.8698
C to Z ↑	0.0177	0.0177	1.7459	1.3105
	C12T28SOI_-LRBR0P6_-NAND3X35_P4	**C12T28SOI_-LRBR0P6_-NAND3X47_P4**	**C12T28SOI_-LRBR0P6_-NAND3X35_P4**	**C12T28SOI_-LRBR0P6_-NAND3X47_P4**

A to Z ↓	0.0131	0.0133	0.5813	0.4447
A to Z ↑	0.0263	0.0264	0.8971	0.6789
B to Z ↓	0.0123	0.0124	0.5868	0.4491
B to Z ↑	0.0227	0.0228	0.8989	0.6797
C to Z ↓	0.0094	0.0097	0.5955	0.4555
C to Z ↑	0.0174	0.0177	0.9088	0.6828
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4		**C12T28SOIDV_-LRBR0P6_-NAND3X18_P4**	
A to Z ↓	0.0138		1.0878	
A to Z ↑	0.0262		1.6327	
B to Z ↓	0.0124		1.0959	
B to Z ↑	0.0227		1.6374	
C to Z ↓	0.0091		1.1137	
C to Z ↑	0.0172		1.6249	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
C12T28SOI_LR_NAND3X4_P4	9.023e-08	2.024e-12
C12T28SOI_LR_NAND3X6_P4	1.244e-07	2.024e-12
C12T28SOI_LR_NAND3X9_P4	1.806e-07	2.780e-12
C12T28SOI_LR_NAND3X12_P4	2.300e-07	2.780e-12
C12T28SOI_LR_NAND3X15_P4	2.782e-07	3.285e-12
C12T28SOI_LR_NAND3X18_P4	3.215e-07	3.284e-12
C12T28SOI_LR_NAND3X21_P4	3.960e-07	4.293e-12
C12T28SOI_LR_NAND3X24_P4	4.346e-07	4.298e-12
C12T28SOI_LR_NAND3X35_P4	6.402e-07	5.812e-12
C12T28SOI_LR_NAND3X47_P4	8.445e-07	7.316e-12
C12T28SOI_LRBR0P6_NAND3X6_P4	1.390e-07	3.444e-12
C12T28SOI_LRBR0P6_NAND3X12_-P4	2.600e-07	4.259e-12
C12T28SOI_LRBR0P6_NAND3X18_-P4	3.606e-07	4.804e-12
C12T28SOI_LRBR0P6_NAND3X24_-P4	4.957e-07	5.891e-12
C12T28SOI_LRBR0P6_NAND3X35_-P4	7.335e-07	7.519e-12
C12T28SOI_LRBR0P6_NAND3X47_-P4	9.698e-07	9.159e-12
C12T28SOIDV_LRBR0P6_-NAND3X18_P4	4.097e-07	3.963e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A (output stable)	1.538e-05	2.101e-05	3.454e-05	4.231e-05
B (output stable)	7.294e-05	9.212e-05	1.611e-04	1.932e-04
C (output stable)	8.617e-05	1.032e-04	1.475e-04	1.715e-04
A to Z	1.450e-03	1.763e-03	2.905e-03	3.420e-03
B to Z	1.303e-03	1.547e-03	2.353e-03	2.767e-03
C to Z	9.976e-04	1.179e-03	1.730e-03	2.032e-03

	C12T28SOI_LR_-NAND3X15_P4	C12T28SOI_LR_-NAND3X18_P4	C12T28SOI_LR_-NAND3X21_P4	C12T28SOI_LR_-NAND3X24_P4
A (output stable)	4.698e-05	5.293e-05	7.423e-05	7.985e-05
B (output stable)	2.289e-04	2.598e-04	3.354e-04	3.595e-04
C (output stable)	1.879e-04	2.055e-04	2.793e-04	2.881e-04
A to Z	4.113e-03	4.642e-03	5.862e-03	6.397e-03
B to Z	3.338e-03	3.769e-03	4.744e-03	5.161e-03
C to Z	2.519e-03	2.789e-03	3.491e-03	3.787e-03
	C12T28SOI_LR_-NAND3X35_P4	C12T28SOI_LR_-NAND3X47_P4	C12T28SOI_-LRBR0P6_-NAND3X6_P4	C12T28SOI_-LRBR0P6_-NAND3X12_P4
A (output stable)	9.653e-05	1.401e-04	2.860e-05	5.876e-05
B (output stable)	5.106e-04	6.777e-04	1.338e-04	2.810e-04
C (output stable)	4.351e-04	5.357e-04	1.368e-04	2.430e-04
A to Z	9.105e-03	1.220e-02	1.897e-03	3.718e-03
B to Z	7.269e-03	9.804e-03	1.562e-03	2.771e-03
C to Z	5.156e-03	7.163e-03	1.021e-03	1.649e-03
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	C12T28SOI_-LRBR0P6_-NAND3X24_P4	C12T28SOI_-LRBR0P6_-NAND3X35_P4	C12T28SOI_-LRBR0P6_-NAND3X47_P4
A (output stable)	7.611e-05	1.120e-04	1.493e-04	2.000e-04
B (output stable)	3.840e-04	5.262e-04	7.442e-04	9.945e-04
C (output stable)	2.816e-04	4.283e-04	6.299e-04	8.183e-04
A to Z	5.008e-03	6.931e-03	1.003e-02	1.325e-02
B to Z	3.721e-03	5.145e-03	7.406e-03	9.807e-03
C to Z	2.324e-03	3.077e-03	4.376e-03	5.831e-03
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4			
A (output stable)	8.338e-05			
B (output stable)	4.325e-04			
C (output stable)	3.614e-04			
A to Z	5.445e-03			
B to Z	4.044e-03			
C to Z	2.369e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LR_-NAND3X4_P4	C12T28SOI_LR_-NAND3X6_P4	C12T28SOI_LR_-NAND3X9_P4	C12T28SOI_LR_-NAND3X12_P4
A (output stable)	6.433e-08	4.130e-08	8.046e-07	-1.573e-08
B (output stable)	5.088e-08	4.318e-08	8.114e-07	-2.130e-08
C (output stable)	3.623e-08	7.003e-09	-1.200e-06	-8.440e-08
A to Z	-3.400e-07	-5.250e-07	7.080e-07	-1.345e-06
B to Z	-1.300e-08	2.150e-07	3.910e-07	5.590e-07
C to Z	2.080e-07	-4.600e-08	-6.800e-08	-1.153e-06
	C12T28SOI_LR_-NAND3X15_P4	C12T28SOI_LR_-NAND3X18_P4	C12T28SOI_LR_-NAND3X21_P4	C12T28SOI_LR_-NAND3X24_P4
A (output stable)	6.764e-07	6.352e-07	2.799e-06	1.268e-06
B (output stable)	5.214e-07	4.484e-07	8.473e-08	9.991e-07
C (output stable)	-1.148e-06	-1.108e-06	-2.396e-06	-2.008e-06
A to Z	-1.144e-06	-1.727e-06	1.185e-06	1.029e-06
B to Z	1.003e-06	1.009e-06	1.181e-06	1.289e-06

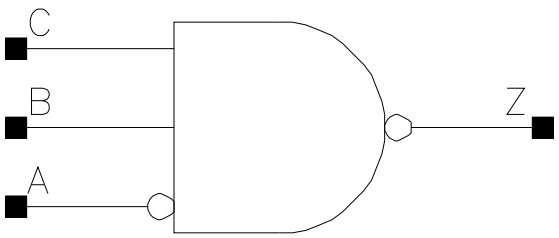
C to Z	-6.590e-07	4.780e-07	-9.480e-07	-1.227e-06
	C12T28SOI_LR_-NAND3X35_P4	C12T28SOI_LR_-NAND3X47_P4	C12T28SOI_-LRBR0P6_-NAND3X6_P4	C12T28SOI_-LRBR0P6_-NAND3X12_P4
A (output stable)	1.866e-06	4.010e-06	1.561e-06	4.725e-06
B (output stable)	1.449e-06	2.799e-07	1.423e-06	-2.473e-07
C (output stable)	-3.127e-06	-3.984e-06	-2.538e-06	-3.105e-06
A to Z	2.600e-07	-5.500e-06	5.390e-07	1.201e-06
B to Z	1.969e-06	2.875e-06	6.790e-07	6.110e-07
C to Z	1.079e-06	-1.898e-06	-7.900e-08	5.860e-07
	C12T28SOI_-LRBR0P6_-NAND3X18_P4	C12T28SOI_-LRBR0P6_-NAND3X24_P4	C12T28SOI_-LRBR0P6_-NAND3X35_P4	C12T28SOI_-LRBR0P6_-NAND3X47_P4
A (output stable)	-3.027e-08	5.600e-06	2.802e-06	3.549e-06
B (output stable)	-3.833e-08	-1.037e-07	2.101e-06	2.590e-06
C (output stable)	-8.307e-08	-4.026e-06	-4.051e-06	-5.076e-06
A to Z	-1.882e-06	1.630e-07	-3.372e-06	-4.921e-06
B to Z	5.200e-07	1.000e-06	1.351e-06	1.751e-06
C to Z	8.950e-07	1.862e-06	4.520e-07	3.620e-07
	C12T28SOIDV_-LRBR0P6_-NAND3X18_P4			
A (output stable)	-3.967e-09			
B (output stable)	-4.067e-09			
C (output stable)	-9.813e-08			
A to Z	5.470e-07			
B to Z	5.410e-07			
C to Z	5.690e-07			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.816	0.9792
X12_P4	1.200	1.224	1.4688
X18_P4	1.200	1.496	1.7952
X24_P4	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0008	0.0011	0.0011	0.0019
B	0.0008	0.0015	0.0023	0.0030
C	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X12_P4**	**X6_P4**	**X12_P4**
A to Z ↓	0.0363	0.0349	4.5058	2.4176
A to Z ↑	0.0254	0.0244	3.1887	1.5991
B to Z ↓	0.0149	0.0155	4.5484	2.4389
B to Z ↑	0.0179	0.0176	3.2532	1.6380
C to Z ↓	0.0142	0.0130	4.5774	2.4557
C to Z ↑	0.0161	0.0148	3.2728	1.6517
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0400	0.0340	1.6603	1.2594

A to Z ↑	0.0280	0.0233	1.0778	0.8078
B to Z ↓	0.0158	0.0155	1.6734	1.2699
B to Z ↑	0.0177	0.0174	1.1041	0.8298
C to Z ↓	0.0139	0.0131	1.6857	1.2804
C to Z ↑	0.0154	0.0146	1.1131	0.8372

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P4	1.649e-07	2.276e-12
X12_P4	3.224e-07	3.032e-12
X18_P4	4.102e-07	3.536e-12
X24_P4	6.307e-07	5.047e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	1.224e-03	2.150e-03	2.962e-03	3.961e-03
B (output stable)	3.074e-05	9.509e-05	1.566e-04	2.282e-04
C (output stable)	6.691e-05	2.415e-04	2.901e-04	4.562e-04
A to Z	2.907e-03	5.630e-03	8.209e-03	1.081e-02
B to Z	1.290e-03	2.498e-03	3.767e-03	4.826e-03
C to Z	1.045e-03	1.732e-03	2.786e-03	3.366e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

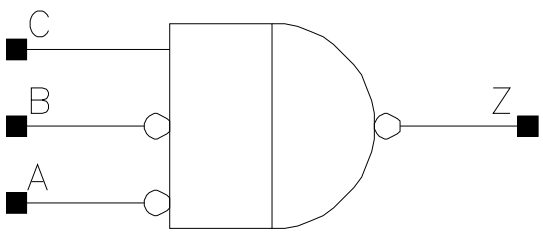
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	1.470e-08	5.212e-07	-2.421e-07	1.872e-06
B (output stable)	1.985e-08	6.641e-07	-1.081e-07	-3.397e-07
C (output stable)	-1.646e-08	-1.268e-06	-1.718e-07	-2.287e-06
A to Z	3.000e-08	4.120e-07	7.000e-09	1.105e-06
B to Z	4.400e-08	6.620e-07	9.310e-07	1.344e-06
C to Z	6.200e-08	4.150e-07	5.920e-07	-1.373e-06

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P4	1.200	0.816	0.9792
X13_P4	1.200	1.088	1.3056
X20_P4	1.200	1.632	1.9584
X27_P4	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P4	X13_P4	X20_P4	X27_P4
A	0.0009	0.0009	0.0018	0.0017
B	0.0011	0.0010	0.0019	0.0018
C	0.0008	0.0015	0.0022	0.0030

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P4	**X13_P4**	**X7_P4**	**X13_P4**
A to Z ↓	0.0365	0.0439	3.0602	1.6438
A to Z ↑	0.0217	0.0247	3.1604	1.5885
B to Z ↓	0.0358	0.0436	3.0618	1.6400
B to Z ↑	0.0205	0.0236	3.1587	1.5881
C to Z ↓	0.0101	0.0096	3.1363	1.6745
C to Z ↑	0.0142	0.0133	3.2639	1.6487
	X20_P4	**X27_P4**	**X20_P4**	**X27_P4**
A to Z ↓	0.0403	0.0442	1.1213	0.8553
A to Z ↑	0.0230	0.0272	1.0738	0.8060
B to Z ↓	0.0375	0.0421	1.1204	0.8543

B to Z ↑	0.0213	0.0260	1.0718	0.8044
C to Z ↓	0.0106	0.0102	1.1465	0.8734
C to Z ↑	0.0140	0.0136	1.1126	0.8351

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X7_P4	2.285e-07	2.277e-12
X13_P4	3.134e-07	2.781e-12
X20_P4	4.960e-07	3.790e-12
X27_P4	5.507e-07	4.293e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	7.311e-04	9.991e-04	1.673e-03	1.980e-03
B (output stable)	5.733e-04	8.126e-04	1.184e-03	1.514e-03
C (output stable)	6.397e-05	2.102e-04	2.464e-04	3.071e-04
A to Z	3.202e-03	5.227e-03	8.332e-03	1.034e-02
B to Z	2.848e-03	4.883e-03	7.224e-03	9.371e-03
C to Z	7.716e-04	1.361e-03	2.256e-03	2.924e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

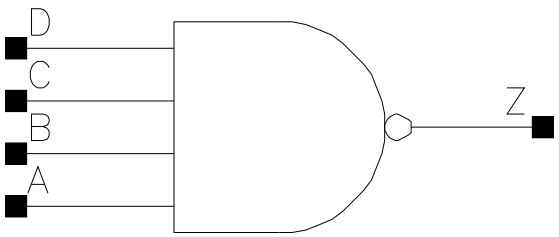
Pin Cycle (vdds)	X7_P4	X13_P4	X20_P4	X27_P4
A (output stable)	-4.128e-06	-4.138e-06	-1.374e-05	-1.351e-05
B (output stable)	1.972e-06	2.006e-06	1.933e-06	1.804e-06
C (output stable)	-9.102e-08	-1.801e-07	-3.149e-07	-4.306e-07
A to Z	-3.089e-06	-3.098e-06	-1.126e-05	-1.148e-05
B to Z	-6.109e-08	-2.880e-08	-2.100e-08	-6.700e-07
C to Z	1.321e-07	1.740e-07	-5.520e-07	-1.000e-06

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0006	0.0006	0.0008	0.0009
B	0.0007	0.0007	0.0008	0.0010
C	0.0006	0.0007	0.0009	0.0010
D	0.0007	0.0007	0.0009	0.0010

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0537	0.0528	1.8477	0.9231
A to Z ↑	0.0429	0.0461	3.2315	1.6031
B to Z ↓	0.0547	0.0546	1.8482	0.9235
B to Z ↑	0.0415	0.0455	3.2322	1.6030
C to Z ↓	0.0538	0.0513	1.8501	0.9234
C to Z ↑	0.0443	0.0479	3.2322	1.6000

D to Z ↓	0.0551	0.0524	1.8494	0.9235
D to Z ↑	0.0434	0.0462	3.2294	1.5997
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0554	0.0511	0.6401	0.4783
A to Z ↑	0.0448	0.0437	1.0829	0.8110
B to Z ↓	0.0566	0.0520	0.6401	0.4782
B to Z ↑	0.0436	0.0424	1.0816	0.8109
C to Z ↓	0.0506	0.0468	0.6400	0.4779
C to Z ↑	0.0455	0.0441	1.0814	0.8100
D to Z ↓	0.0518	0.0478	0.6396	0.4779
D to Z ↑	0.0440	0.0427	1.0813	0.8087

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.972e-07	3.033e-12
X17_P4	4.357e-07	3.537e-12
X25_P4	6.303e-07	4.294e-12
X33_P4	7.810e-07	4.545e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	5.200e-04	6.596e-04	9.756e-04	1.155e-03
B (output stable)	4.749e-04	6.191e-04	8.890e-04	1.043e-03
C (output stable)	5.156e-04	6.275e-04	9.414e-04	1.073e-03
D (output stable)	4.706e-04	5.708e-04	8.068e-04	9.165e-04
A to Z	3.778e-03	5.625e-03	8.801e-03	1.065e-02
B to Z	3.653e-03	5.511e-03	8.624e-03	1.041e-02
C to Z	3.874e-03	5.515e-03	8.225e-03	9.877e-03
D to Z	3.761e-03	5.382e-03	8.034e-03	9.639e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

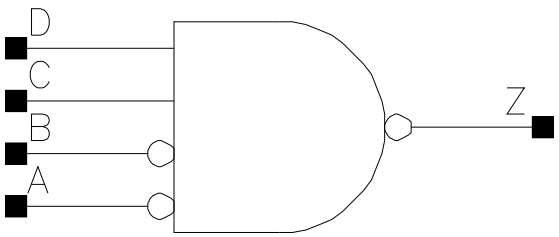
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	-4.350e-06	-7.639e-06	-2.359e-05	-2.829e-05
B (output stable)	-2.999e-06	-5.305e-06	-1.575e-05	-1.890e-05
C (output stable)	5.636e-06	1.137e-05	2.855e-05	3.539e-05
D (output stable)	7.246e-07	2.201e-06	1.357e-06	2.421e-06
A to Z	-1.613e-06	-2.952e-06	-8.466e-06	-9.620e-06
B to Z	-1.445e-06	-2.540e-06	-7.874e-06	-9.592e-06
C to Z	-1.246e-07	-5.375e-07	-6.400e-07	-6.730e-07
D to Z	1.416e-07	-9.610e-08	-3.450e-07	-2.610e-07

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X12_P4	1.200	1.496	1.7952
X18_P4	1.200	2.040	2.4480
X24_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P4	X12_P4	X18_P4	X24_P4
A	0.0010	0.0010	0.0019	0.0017
B	0.0010	0.0014	0.0019	0.0018
C	0.0008	0.0015	0.0022	0.0031
D	0.0008	0.0015	0.0022	0.0030

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X12_P4	X6_P4	X12_P4
A to Z ↓	0.0383	0.0506	4.6521	2.4221
A to Z ↑	0.0229	0.0275	3.1594	1.5927
B to Z ↓	0.0369	0.0494	4.6507	2.4233
B to Z ↑	0.0210	0.0262	3.1590	1.5901
C to Z ↓	0.0151	0.0153	4.6934	2.4383
C to Z ↑	0.0180	0.0176	3.4550	1.6376

D to Z ↓	0.0140	0.0129	4.7212	2.4542
D to Z ↑	0.0161	0.0147	3.4765	1.6512
	X18_P4	**X24_P4**	**X18_P4**	**X24_P4**
A to Z ↓	0.0442	0.0493	1.6559	1.2611
A to Z ↑	0.0246	0.0308	1.0745	0.8067
B to Z ↓	0.0414	0.0472	1.6561	1.2613
B to Z ↑	0.0229	0.0294	1.0728	0.8056
C to Z ↓	0.0155	0.0160	1.6698	1.2678
C to Z ↑	0.0176	0.0178	1.1088	0.8280
D to Z ↓	0.0137	0.0138	1.6789	1.2763
D to Z ↑	0.0152	0.0152	1.1333	0.8357

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P4	2.052e-07	2.530e-12
X12_P4	3.126e-07	3.536e-12
X18_P4	4.916e-07	4.544e-12
X24_P4	5.367e-07	5.300e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	8.154e-04	1.358e-03	2.063e-03	2.489e-03
B (output stable)	6.349e-04	1.118e-03	1.548e-03	2.022e-03
C (output stable)	5.240e-05	1.370e-04	2.081e-04	2.846e-04
D (output stable)	5.942e-05	1.989e-04	2.245e-04	3.221e-04
A to Z	3.435e-03	6.485e-03	9.682e-03	1.269e-02
B to Z	3.086e-03	6.004e-03	8.623e-03	1.171e-02
C to Z	1.254e-03	2.485e-03	3.662e-03	5.096e-03
D to Z	1.002e-03	1.718e-03	2.739e-03	3.688e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

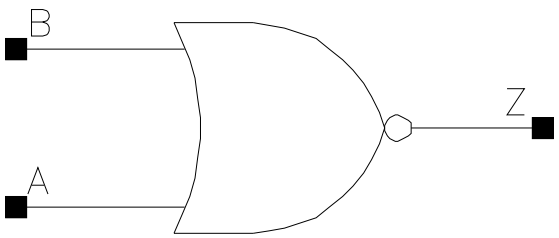
Pin Cycle (vdds)	X6_P4	X12_P4	X18_P4	X24_P4
A (output stable)	-4.015e-06	-8.772e-06	-1.340e-05	-1.349e-05
B (output stable)	2.999e-06	2.130e-06	4.414e-06	4.214e-06
C (output stable)	-4.898e-08	7.027e-07	4.581e-07	1.351e-06
D (output stable)	-7.465e-08	-1.398e-06	-1.402e-06	-2.792e-06
A to Z	-2.998e-06	-7.367e-06	-1.003e-05	-1.099e-05
B to Z	3.737e-07	2.520e-07	3.770e-07	-1.300e-08
C to Z	-2.300e-08	6.910e-07	1.239e-06	1.404e-06
D to Z	8.000e-09	3.990e-07	6.600e-07	8.430e-07

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.408	0.4896
X5_P4	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X10_P4	1.200	0.680	0.8160
X14_P4	1.200	0.680	0.8160
X17_P4	1.200	0.952	1.1424
X21_P4	1.200	0.952	1.1424
X24_P4	1.200	1.224	1.4688
X27_P4	1.200	1.224	1.4688
X34_P4	1.200	1.496	1.7952
X40_P4	1.200	1.360	1.6320
X41_P4	1.200	1.768	2.1216
X49_P4	1.200	1.496	1.7952
X53_P4	1.200	1.904	2.2848
X55_P4	1.200	2.312	2.7744
X57_P4	1.200	1.904	2.2848
X65_P4	1.200	2.040	2.4480
X84_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P4	X5_P4	X7_P4	X10_P4
A	0.0005	0.0006	0.0008	0.0013
B	0.0005	0.0006	0.0008	0.0012
	X14_P4	X17_P4	X21_P4	X24_P4

A	0.0017	0.0021	0.0025	0.0029
B	0.0015	0.0020	0.0023	0.0027
	X27_P4	X34_P4	X40_P4	X41_P4
A	0.0032	0.0041	0.0009	0.0049
B	0.0030	0.0037	0.0011	0.0046
	X49_P4	X53_P4	X55_P4	X57_P4
A	0.0009	0.0010	0.0065	0.0010
B	0.0010	0.0009	0.0061	0.0009
	X65_P4	X84_P4		
A	0.0010	0.0011		
B	0.0009	0.0010		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X5_P4**	**X3_P4**	**X5_P4**
A to Z ↓	0.0105	0.0099	3.5169	2.5614
A to Z ↑	0.0219	0.0205	13.3610	9.7667
B to Z ↓	0.0094	0.0085	3.6044	2.5854
B to Z ↑	0.0207	0.0189	13.4347	9.8083
	X7_P4	**X10_P4**	**X7_P4**	**X10_P4**
A to Z ↓	0.0095	0.0100	1.8888	1.2245
A to Z ↑	0.0195	0.0218	6.9245	4.6104
B to Z ↓	0.0081	0.0075	1.9161	1.2401
B to Z ↑	0.0176	0.0165	6.9576	4.6372
	X14_P4	**X17_P4**	**X14_P4**	**X17_P4**
A to Z ↓	0.0097	0.0099	0.9351	0.7499
A to Z ↑	0.0207	0.0208	3.4306	2.7639
B to Z ↓	0.0073	0.0079	0.9475	0.7583
B to Z ↑	0.0157	0.0168	3.4524	2.7792
	X21_P4	**X24_P4**	**X21_P4**	**X24_P4**
A to Z ↓	0.0098	0.0098	0.6412	0.5461
A to Z ↑	0.0201	0.0205	2.3062	2.0078
B to Z ↓	0.0079	0.0075	0.6477	0.5529
B to Z ↑	0.0164	0.0161	2.3211	2.0198
	X27_P4	**X34_P4**	**X27_P4**	**X34_P4**
A to Z ↓	0.0097	0.0101	0.4856	0.3925
A to Z ↑	0.0200	0.0203	1.7715	1.4098
B to Z ↓	0.0073	0.0078	0.4922	0.3970
B to Z ↑	0.0156	0.0164	1.7822	1.4187
	X40_P4	**X41_P4**	**X40_P4**	**X41_P4**
A to Z ↓	0.0343	0.0098	0.3881	0.3270
A to Z ↑	0.0525	0.0200	0.6653	1.1682
B to Z ↓	0.0331	0.0074	0.3883	0.3312
B to Z ↑	0.0523	0.0155	0.6641	1.1757
	X49_P4	**X53_P4**	**X49_P4**	**X53_P4**
A to Z ↓	0.0356	0.0370	0.3231	0.2958
A to Z ↑	0.0534	0.0616	0.5531	0.5113
B to Z ↓	0.0343	0.0358	0.3232	0.2959
B to Z ↑	0.0532	0.0609	0.5525	0.5114
	X55_P4	**X57_P4**	**X55_P4**	**X57_P4**
A to Z ↓	0.0099	0.0373	0.2474	0.2782
A to Z ↑	0.0199	0.0617	0.8800	0.4756

B to Z ↓	0.0076	0.0360	0.2511	0.2784
B to Z ↑	0.0157	0.0610	0.8868	0.4758
	X65_P4	**X84_P4**	**X65_P4**	**X84_P4**
A to Z ↓	0.0380	0.0398	0.2441	0.1948
A to Z ↑	0.0620	0.0627	0.4162	0.3300
B to Z ↓	0.0368	0.0387	0.2441	0.1946
B to Z ↑	0.0614	0.0623	0.4156	0.3301

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P4	6.878e-08	1.520e-12
X5_P4	9.103e-08	1.520e-12
X7_P4	1.197e-07	1.520e-12
X10_P4	1.779e-07	2.024e-12
X14_P4	2.244e-07	2.024e-12
X17_P4	2.844e-07	2.528e-12
X21_P4	3.234e-07	2.528e-12
X24_P4	3.894e-07	3.032e-12
X27_P4	4.227e-07	3.032e-12
X34_P4	5.222e-07	3.536e-12
X40_P4	6.478e-07	3.284e-12
X41_P4	6.216e-07	4.041e-12
X49_P4	7.173e-07	3.535e-12
X53_P4	8.785e-07	4.291e-12
X55_P4	8.205e-07	5.049e-12
X57_P4	9.109e-07	4.291e-12
X65_P4	9.803e-07	4.543e-12
X84_P4	1.109e-06	5.052e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	3.045e-05	4.131e-05	5.782e-05	1.367e-04
B (output stable)	5.264e-06	6.301e-06	8.648e-06	6.144e-05
A to Z	6.700e-04	8.121e-04	1.062e-03	1.882e-03
B to Z	4.888e-04	5.653e-04	7.130e-04	9.941e-04
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	1.677e-04	2.105e-04	2.422e-04	2.885e-04
B (output stable)	6.872e-05	8.217e-05	7.863e-05	9.520e-05
A to Z	2.318e-03	2.917e-03	3.324e-03	3.955e-03
B to Z	1.229e-03	1.718e-03	1.952e-03	2.222e-03
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	3.160e-04	3.998e-04	5.807e-05	4.953e-04
B (output stable)	9.838e-05	1.099e-04	8.540e-06	1.659e-04
A to Z	4.290e-03	5.511e-03	1.043e-02	6.517e-03
B to Z	2.357e-03	3.239e-03	1.010e-02	3.509e-03
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	5.825e-05	6.098e-05	6.406e-04	6.098e-05
B (output stable)	8.446e-06	9.107e-06	1.967e-04	9.108e-06
A to Z	1.153e-02	1.453e-02	8.485e-03	1.488e-02
B to Z	1.119e-02	1.417e-02	4.705e-03	1.452e-02
	X65_P4	X84_P4		

A (output stable)	6.107e-05	6.246e-05		
B (output stable)	9.209e-06	9.662e-06		
A to Z	1.589e-02	1.876e-02		
B to Z	1.552e-02	1.833e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

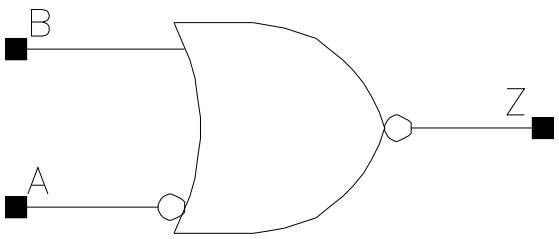
Pin Cycle (vdds)	X3_P4	X5_P4	X7_P4	X10_P4
A (output stable)	-2.473e-06	-3.337e-06	-4.594e-06	-1.351e-05
B (output stable)	1.277e-05	1.753e-05	2.396e-05	8.080e-05
A to Z	-1.653e-06	-2.036e-06	-2.749e-06	-1.023e-05
B to Z	1.555e-07	4.000e-09	-8.900e-09	1.062e-06
	X14_P4	X17_P4	X21_P4	X24_P4
A (output stable)	-1.654e-05	-1.340e-05	-1.467e-05	-2.444e-05
B (output stable)	1.009e-04	7.787e-05	8.265e-05	1.394e-04
A to Z	-1.236e-05	-9.916e-06	-1.038e-05	-1.737e-05
B to Z	1.865e-06	2.125e-06	2.798e-06	2.859e-06
	X27_P4	X34_P4	X40_P4	X41_P4
A (output stable)	-2.717e-05	-2.545e-05	-4.548e-06	-3.833e-05
B (output stable)	1.552e-04	1.384e-04	2.383e-05	2.142e-04
A to Z	-1.958e-05	-1.757e-05	-3.305e-06	-2.736e-05
B to Z	5.298e-06	3.733e-06	8.200e-08	7.226e-06
	X49_P4	X53_P4	X55_P4	X57_P4
A (output stable)	-4.548e-06	-4.683e-06	-4.397e-05	-4.683e-06
B (output stable)	2.372e-05	2.563e-05	2.406e-04	2.563e-05
A to Z	-3.234e-06	-3.211e-06	-3.117e-05	-3.012e-06
B to Z	-1.030e-07	-2.010e-07	7.050e-06	-4.160e-07
	X65_P4	X84_P4		
A (output stable)	-4.682e-06	-4.809e-06		
B (output stable)	2.563e-05	2.617e-05		
A to Z	-3.527e-06	-3.886e-06		
B to Z	-4.800e-07	-6.020e-07		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X7_P4	1.200	0.680	0.8160
X13_P4	1.200	0.952	1.1424
X27_P4	1.200	1.632	1.9584
X41_P4	1.200	2.312	2.7744
X55_P4	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X7_P4	X13_P4
A	0.0008	0.0008	0.0008	0.0011
B	0.0006	0.0008	0.0008	0.0015
	X27_P4	X41_P4	X55_P4	
A	0.0020	0.0029	0.0038	
B	0.0030	0.0046	0.0061	

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0291	0.0318	3.3489	2.2103
A to Z ↑	0.0268	0.0267	13.2427	6.8838
B to Z ↓	0.0096	0.0092	3.5743	2.3727
B to Z ↑	0.0210	0.0176	13.4078	6.9749

	X7_P4	X13_P4	X7_P4	X13_P4
A to Z ↓	0.0321	0.0292	1.7653	0.9628
A to Z ↑	0.0289	0.0274	6.8197	3.6132
B to Z ↓	0.0083	0.0076	1.8323	0.9975
B to Z ↑	0.0186	0.0169	6.8863	3.6565
	X27_P4	**X41_P4**	**X27_P4**	**X41_P4**
A to Z ↓	0.0284	0.0291	0.4612	0.3128
A to Z ↑	0.0264	0.0268	1.7328	1.1626
B to Z ↓	0.0075	0.0076	0.4945	0.3334
B to Z ↑	0.0162	0.0161	1.7547	1.1770
	X55_P4		**X55_P4**	
A to Z ↓	0.0285		0.2368	
A to Z ↑	0.0263		0.8771	
B to Z ↓	0.0076		0.2528	
B to Z ↑	0.0160		0.8880	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P4	1.175e-07	1.771e-12
X6_P4	1.574e-07	1.772e-12
X7_P4	1.865e-07	1.993e-12
X13_P4	3.260e-07	2.527e-12
X27_P4	6.094e-07	3.787e-12
X41_P4	8.852e-07	5.048e-12
X55_P4	1.161e-06	6.306e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	9.927e-04	1.249e-03	1.323e-03	2.108e-03
B (output stable)	7.374e-07	1.950e-06	1.662e-06	3.229e-06
A to Z	1.737e-03	2.386e-03	2.771e-03	4.630e-03
B to Z	5.012e-04	7.054e-04	8.393e-04	1.348e-03
	X27_P4	X41_P4	X55_P4	
A (output stable)	4.144e-03	6.339e-03	8.168e-03	
B (output stable)	6.193e-06	9.427e-06	1.250e-05	
A to Z	9.204e-03	1.374e-02	1.779e-02	
B to Z	2.597e-03	3.803e-03	5.007e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

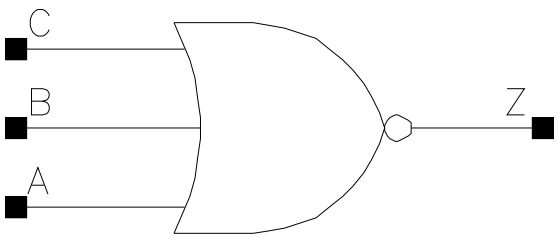
Pin Cycle (vdds)	X3_P4	X6_P4	X7_P4	X13_P4
A (output stable)	-2.407e-06	-4.286e-06	-8.448e-06	-1.403e-05
B (output stable)	3.102e-07	8.642e-07	6.901e-07	1.039e-06
A to Z	-1.279e-06	-2.518e-06	-6.027e-06	-1.033e-05
B to Z	-7.900e-09	2.080e-07	4.182e-07	1.391e-06
	X27_P4	X41_P4	X55_P4	
A (output stable)	-2.431e-05	-3.385e-05	-4.002e-05	
B (output stable)	1.528e-06	2.224e-06	2.751e-06	
A to Z	-1.796e-05	-2.462e-05	-2.854e-05	
B to Z	3.859e-06	5.156e-06	6.403e-06	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	0.544	0.6528
X6_P4	1.200	0.544	0.6528
X9_P4	1.200	0.952	1.1424
X13_P4	1.200	0.952	1.1424
X16_P4	1.200	1.360	1.6320
X19_P4	1.200	1.496	1.7952
X22_P4	1.200	1.768	2.1216
X25_P4	1.200	1.904	2.2848
X37_P4	1.200	2.584	3.1008
X49_P4	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P4	X6_P4	X9_P4	X13_P4
A	0.0007	0.0008	0.0013	0.0016
B	0.0006	0.0008	0.0014	0.0017
C	0.0007	0.0008	0.0012	0.0015
	X16_P4	X19_P4	X22_P4	X25_P4
A	0.0021	0.0024	0.0029	0.0032
B	0.0021	0.0028	0.0031	0.0038
C	0.0019	0.0022	0.0027	0.0029
	X37_P4	X49_P4		
A	0.0049	0.0065		
B	0.0049	0.0066		

C	0.0043	0.0061		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0119	0.0114	2.5989	1.9173
A to Z ↑	0.0304	0.0284	14.9470	10.6032
B to Z ↓	0.0112	0.0106	2.6047	1.9215
B to Z ↑	0.0288	0.0265	14.9602	10.6193
C to Z ↓	0.0100	0.0093	2.6232	1.9437
C to Z ↑	0.0255	0.0227	15.0057	10.6526
	X9_P4	**X13_P4**	**X9_P4**	**X13_P4**
A to Z ↓	0.0116	0.0114	1.2665	0.9776
A to Z ↑	0.0306	0.0290	7.0243	5.2616
B to Z ↓	0.0110	0.0105	1.2313	0.9341
B to Z ↑	0.0301	0.0278	7.0326	5.2619
C to Z ↓	0.0087	0.0082	1.2433	0.9529
C to Z ↑	0.0211	0.0196	7.0503	5.2805
	X16_P4	**X19_P4**	**X16_P4**	**X19_P4**
A to Z ↓	0.0116	0.0114	0.7555	0.6407
A to Z ↑	0.0296	0.0293	4.2399	3.5202
B to Z ↓	0.0111	0.0109	0.7582	0.6263
B to Z ↑	0.0285	0.0289	4.2391	3.5203
C to Z ↓	0.0090	0.0088	0.7629	0.6544
C to Z ↑	0.0219	0.0208	4.2543	3.5331
	X22_P4	**X25_P4**	**X22_P4**	**X25_P4**
A to Z ↓	0.0115	0.0114	0.5577	0.4892
A to Z ↑	0.0292	0.0291	3.0265	2.6468
B to Z ↓	0.0109	0.0107	0.5473	0.4696
B to Z ↑	0.0284	0.0287	3.0298	2.6492
C to Z ↓	0.0085	0.0083	0.5540	0.4901
C to Z ↑	0.0205	0.0197	3.0408	2.6570
	X37_P4	**X49_P4**	**X37_P4**	**X49_P4**
A to Z ↓	0.0114	0.0115	0.3360	0.2553
A to Z ↑	0.0285	0.0285	1.7729	1.3353
B to Z ↓	0.0107	0.0108	0.3321	0.2526
B to Z ↑	0.0271	0.0271	1.7741	1.3358
C to Z ↓	0.0086	0.0088	0.3372	0.2561
C to Z ↑	0.0197	0.0201	1.7800	1.3408

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	9.069e-08	1.771e-12
X6_P4	1.203e-07	1.772e-12
X9_P4	1.827e-07	2.527e-12
X13_P4	2.332e-07	2.526e-12
X16_P4	2.949e-07	3.283e-12
X19_P4	3.542e-07	3.533e-12
X22_P4	4.076e-07	4.040e-12
X25_P4	4.644e-07	4.291e-12
X37_P4	6.684e-07	5.574e-12

X49_P4	8.866e-07	7.070e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	1.492e-04	2.084e-04	4.247e-04	5.420e-04
B (output stable)	2.046e-05	2.736e-05	1.819e-04	2.023e-04
C (output stable)	3.488e-06	4.660e-06	2.779e-05	2.984e-05
A to Z	1.243e-03	1.578e-03	2.633e-03	3.242e-03
B to Z	1.002e-03	1.244e-03	2.196e-03	2.612e-03
C to Z	7.516e-04	8.838e-04	1.248e-03	1.458e-03
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	6.225e-04	7.848e-04	9.200e-04	1.086e-03
B (output stable)	1.959e-04	2.734e-04	3.313e-04	4.089e-04
C (output stable)	3.125e-05	3.717e-05	4.717e-05	5.287e-05
A to Z	4.188e-03	4.956e-03	5.741e-03	6.509e-03
B to Z	3.405e-03	4.098e-03	4.688e-03	5.354e-03
C to Z	2.180e-03	2.421e-03	2.761e-03	2.954e-03
	X37_P4	X49_P4		
A (output stable)	1.524e-03	2.016e-03		
B (output stable)	4.850e-04	6.265e-04		
C (output stable)	7.800e-05	9.987e-05		
A to Z	9.431e-03	1.258e-02		
B to Z	7.514e-03	1.001e-02		
C to Z	4.309e-03	5.846e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

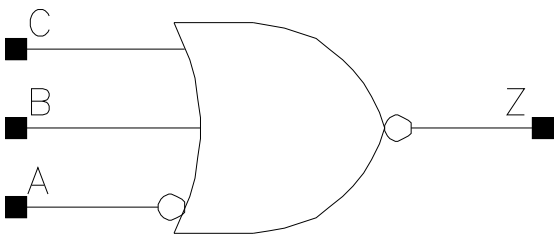
Pin Cycle (vdds)	X4_P4	X6_P4	X9_P4	X13_P4
A (output stable)	-2.539e-05	-3.504e-05	-7.471e-05	-9.558e-05
B (output stable)	6.771e-06	9.675e-06	-1.003e-06	8.510e-07
C (output stable)	1.235e-05	1.718e-05	5.658e-05	6.979e-05
A to Z	-5.075e-06	-6.313e-06	-1.717e-05	-2.075e-05
B to Z	-2.176e-06	-2.895e-06	-1.126e-05	-1.172e-05
C to Z	-1.257e-07	-9.050e-08	-4.505e-07	-4.565e-07
	X16_P4	X19_P4	X22_P4	X25_P4
A (output stable)	-9.350e-05	-1.231e-04	-1.484e-04	-1.798e-04
B (output stable)	1.797e-05	2.749e-05	1.939e-05	3.029e-05
C (output stable)	5.443e-05	7.400e-05	9.526e-05	1.165e-04
A to Z	-1.943e-05	-2.547e-05	-3.155e-05	-3.855e-05
B to Z	-1.012e-05	-1.348e-05	-1.818e-05	-2.141e-05
C to Z	-4.259e-07	-5.030e-07	-8.682e-07	-8.877e-07
	X37_P4	X49_P4		
A (output stable)	-2.432e-04	-3.168e-04		
B (output stable)	3.717e-05	5.130e-05		
C (output stable)	1.497e-04	1.909e-04		
A to Z	-5.102e-05	-6.581e-05		
B to Z	-2.731e-05	-3.486e-05		
C to Z	1.265e-06	-1.461e-06		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.680	0.8160
X13_P4	1.200	1.224	1.4688
X19_P4	1.200	1.496	1.7952
X25_P4	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0008	0.0010	0.0011	0.0020
B	0.0008	0.0017	0.0025	0.0033
C	0.0008	0.0015	0.0022	0.0030

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X13_P4**	**X6_P4**	**X13_P4**
A to Z ↓	0.0320	0.0306	1.8397	1.0330
A to Z ↑	0.0358	0.0352	10.7180	5.2542
B to Z ↓	0.0108	0.0105	1.9310	0.9397
B to Z ↑	0.0269	0.0279	10.7509	5.2626
C to Z ↓	0.0094	0.0082	1.9447	0.9536
C to Z ↑	0.0232	0.0197	10.7817	5.2801
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0348	0.0306	0.6261	0.4756

A to Z ↑	0.0380	0.0351	3.5317	2.6488
B to Z ↓	0.0110	0.0107	0.6548	0.4884
B to Z ↑	0.0273	0.0271	3.5432	2.6558
C to Z ↓	0.0088	0.0083	0.6553	0.4932
C to Z ↑	0.0209	0.0198	3.5532	2.6657

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P4	1.705e-07	2.025e-12
X13_P4	3.401e-07	3.033e-12
X19_P4	4.314e-07	3.537e-12
X25_P4	6.466e-07	4.796e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	1.468e-03	2.743e-03	3.682e-03	5.385e-03
B (output stable)	1.676e-05	7.130e-05	8.761e-05	1.283e-04
C (output stable)	2.388e-06	2.953e-05	1.767e-05	3.818e-05
A to Z	2.962e-03	5.818e-03	8.079e-03	1.122e-02
B to Z	1.257e-03	2.629e-03	3.821e-03	5.022e-03
C to Z	9.026e-04	1.473e-03	2.407e-03	2.940e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

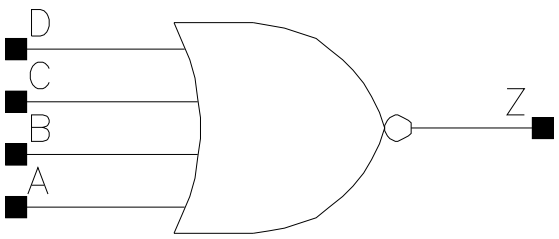
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	-4.363e-05	-1.120e-04	-1.422e-04	-2.051e-04
B (output stable)	1.618e-05	3.794e-05	6.253e-05	8.103e-05
C (output stable)	1.022e-05	3.732e-05	3.538e-05	5.867e-05
A to Z	-6.027e-06	-1.765e-05	-2.044e-05	-3.164e-05
B to Z	-3.047e-06	-1.003e-05	-1.102e-05	-1.732e-05
C to Z	1.642e-07	4.684e-07	5.200e-07	1.221e-06

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X25_P4	1.200	1.904	2.2848
X32_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X32_P4
A	0.0007	0.0007	0.0007	0.0009
B	0.0007	0.0007	0.0008	0.0011
C	0.0006	0.0006	0.0008	0.0009
D	0.0006	0.0006	0.0008	0.0009

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0358	0.0354	1.8015	0.8873
A to Z ↑	0.0571	0.0611	3.2817	1.6225
B to Z ↓	0.0345	0.0344	1.8007	0.8864
B to Z ↑	0.0563	0.0608	3.2838	1.6218
C to Z ↓	0.0352	0.0354	1.7979	0.8853
C to Z ↑	0.0578	0.0628	3.2790	1.6225

D to Z ↓	0.0347	0.0350	1.7983	0.8850
D to Z ↑	0.0576	0.0630	3.2787	1.6203
	X25_P4	**X32_P4**	**X25_P4**	**X32_P4**
A to Z ↓	0.0361	0.0382	0.6195	0.4871
A to Z ↑	0.0601	0.0585	1.1103	0.8398
B to Z ↓	0.0352	0.0370	0.6198	0.4868
B to Z ↑	0.0601	0.0579	1.1119	0.8410
C to Z ↓	0.0349	0.0374	0.6178	0.4854
C to Z ↑	0.0597	0.0589	1.1110	0.8402
D to Z ↓	0.0338	0.0356	0.6180	0.4852
D to Z ↑	0.0594	0.0582	1.1114	0.8401

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.447e-07	3.032e-12
X17_P4	3.504e-07	3.284e-12
X25_P4	5.186e-07	4.293e-12
X32_P4	6.300e-07	4.545e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	5.284e-04	6.426e-04	8.789e-04	1.121e-03
B (output stable)	4.307e-04	5.489e-04	7.562e-04	9.497e-04
C (output stable)	5.188e-04	6.233e-04	9.419e-04	1.201e-03
D (output stable)	4.077e-04	5.160e-04	7.896e-04	9.985e-04
A to Z	3.629e-03	5.434e-03	8.278e-03	1.041e-02
B to Z	3.434e-03	5.259e-03	8.008e-03	1.007e-02
C to Z	3.681e-03	5.424e-03	7.794e-03	9.823e-03
D to Z	3.481e-03	5.247e-03	7.545e-03	9.481e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

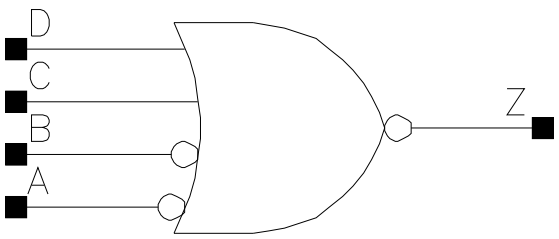
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X32_P4
A (output stable)	-2.059e-06	-2.109e-06	-2.938e-06	-3.877e-06
B (output stable)	8.242e-07	7.773e-07	1.684e-06	2.748e-06
C (output stable)	-6.284e-06	-6.091e-06	-8.650e-06	-1.119e-05
D (output stable)	4.272e-06	4.098e-06	6.228e-06	8.422e-06
A to Z	-1.564e-06	-1.835e-06	-2.444e-06	-3.014e-06
B to Z	-7.570e-08	-1.023e-07	1.220e-07	2.124e-07
C to Z	-1.991e-06	-1.651e-06	-2.571e-06	-3.045e-06
D to Z	-2.560e-07	1.355e-07	-8.800e-09	7.250e-08

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X13_P4	1.200	1.496	1.7952
X19_P4	1.200	2.040	2.4480
X25_P4	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P4	X13_P4	X19_P4	X25_P4
A	0.0010	0.0010	0.0019	0.0019
B	0.0010	0.0015	0.0019	0.0020
C	0.0008	0.0016	0.0023	0.0031
D	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	X13_P4	X6_P4	X13_P4
A to Z ↓	0.0280	0.0345	1.7940	0.8976
A to Z ↑	0.0361	0.0438	10.3357	5.3261
B to Z ↓	0.0263	0.0333	1.7930	0.8971
B to Z ↑	0.0362	0.0446	10.3333	5.3324
C to Z ↓	0.0112	0.0107	1.9661	0.9390
C to Z ↑	0.0271	0.0281	10.3676	5.3439

D to Z ↓	0.0096	0.0084	1.9681	0.9502
D to Z ↑	0.0229	0.0204	10.3982	5.3583
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0304	0.0332	0.6173	0.4654
A to Z ↑	0.0397	0.0427	3.5349	2.6689
B to Z ↓	0.0281	0.0313	0.6166	0.4651
B to Z ↑	0.0394	0.0430	3.5359	2.6703
C to Z ↓	0.0110	0.0109	0.6555	0.4910
C to Z ↑	0.0271	0.0272	3.5398	2.6760
D to Z ↓	0.0088	0.0084	0.6559	0.4929
D to Z ↑	0.0209	0.0197	3.5551	2.6846

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P4	2.101e-07	2.529e-12
X13_P4	3.230e-07	3.538e-12
X19_P4	5.089e-07	4.545e-12
X25_P4	6.022e-07	5.301e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	8.782e-04	1.612e-03	2.393e-03	2.982e-03
B (output stable)	7.796e-04	1.446e-03	2.060e-03	2.653e-03
C (output stable)	1.238e-05	5.047e-05	8.162e-05	1.131e-04
D (output stable)	5.801e-06	3.235e-05	3.533e-05	6.291e-05
A to Z	3.534e-03	6.695e-03	9.913e-03	1.274e-02
B to Z	3.297e-03	6.355e-03	9.160e-03	1.208e-02
C to Z	1.311e-03	2.641e-03	3.783e-03	4.968e-03
D to Z	9.374e-04	1.553e-03	2.405e-03	2.898e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

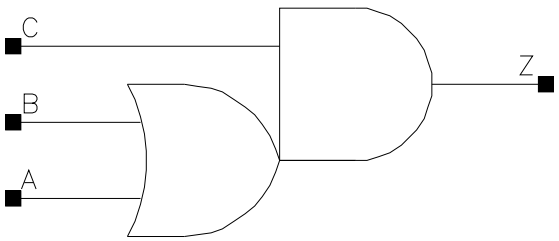
Pin Cycle (vdds)	X6_P4	X13_P4	X19_P4	X25_P4
A (output stable)	-2.302e-05	-5.907e-05	-7.873e-05	-1.086e-04
B (output stable)	-1.968e-05	-5.093e-05	-6.567e-05	-9.124e-05
C (output stable)	1.945e-05	3.145e-05	5.321e-05	6.904e-05
D (output stable)	1.255e-05	3.670e-05	4.105e-05	6.085e-05
A to Z	-6.764e-06	-2.091e-05	-2.474e-05	-3.834e-05
B to Z	-6.499e-06	-2.208e-05	-2.555e-05	-3.883e-05
C to Z	-2.866e-06	-1.020e-05	-1.166e-05	-1.684e-05
D to Z	1.142e-07	-4.960e-07	-4.840e-07	-7.030e-07

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.680	0.8160
X17_P4	1.200	0.816	0.9792
X33_P4	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0009	0.0009	0.0018
B	0.0010	0.0011	0.0020
C	0.0010	0.0010	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
A to Z ↓	0.0333	0.0383	1.8635	0.9329
A to Z ↑	0.0250	0.0277	3.3016	1.6258
B to Z ↓	0.0324	0.0379	1.8642	0.9336
B to Z ↑	0.0229	0.0259	3.2994	1.6248
C to Z ↓	0.0282	0.0310	1.8402	0.9140
C to Z ↑	0.0241	0.0264	3.3005	1.6237
	X33_P4		**X33_P4**	
A to Z ↓	0.0395		0.4747	
A to Z ↑	0.0295		0.8160	

B to Z ↓	0.0389		0.4747	
B to Z ↑	0.0271		0.8153	
C to Z ↓	0.0316		0.4641	
C to Z ↑	0.0272		0.8150	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.190e-07	2.023e-12
X17_P4	3.005e-07	2.276e-12
X33_P4	5.986e-07	3.793e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	1.336e-04	1.345e-04	2.700e-04
B (output stable)	3.679e-05	3.641e-05	6.615e-05
C (output stable)	6.414e-05	6.432e-05	1.320e-04
A to Z	2.693e-03	3.856e-03	7.922e-03
B to Z	2.343e-03	3.508e-03	7.233e-03
C to Z	2.927e-03	4.072e-03	8.279e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

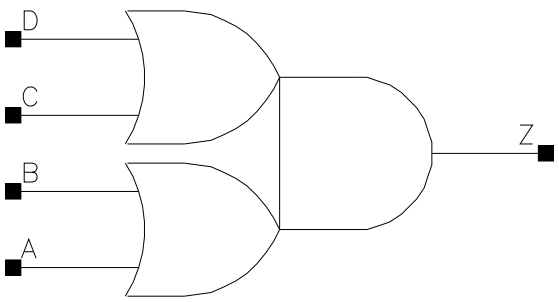
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	-3.562e-06	-3.731e-06	-7.511e-06
B (output stable)	-1.410e-06	-1.460e-06	-2.968e-06
C (output stable)	1.809e-06	2.101e-06	3.710e-06
A to Z	-3.098e-06	-3.353e-06	-6.452e-06
B to Z	-7.371e-08	-1.027e-07	-6.744e-07
C to Z	-1.067e-06	-1.139e-06	-2.452e-06

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X17_P4	1.200	1.088	1.3056
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0006	0.0009	0.0018
B	0.0007	0.0010	0.0018
C	0.0007	0.0010	0.0019
D	0.0006	0.0010	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0539	0.0464	1.8236	0.9270
A to Z ↑	0.0337	0.0298	3.2360	1.6190
B to Z ↓	0.0541	0.0462	1.8238	0.9272
B to Z ↑	0.0326	0.0285	3.2329	1.6183

C to Z ↓	0.0475	0.0415	1.8125	0.9238
C to Z ↑	0.0327	0.0297	3.2373	1.6191
D to Z ↓	0.0467	0.0407	1.8132	0.9243
D to Z ↑	0.0309	0.0276	3.2349	1.6159
	X33_P4		**X33_P4**	
A to Z ↓	0.0470		0.4789	
A to Z ↑	0.0299		0.8139	
B to Z ↓	0.0449		0.4792	
B to Z ↑	0.0280		0.8123	
C to Z ↓	0.0413		0.4763	
C to Z ↑	0.0291		0.8136	
D to Z ↓	0.0388		0.4772	
D to Z ↑	0.0268		0.8124	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.105e-07	2.527e-12
X17_P4	3.883e-07	2.797e-12
X33_P4	7.318e-07	4.544e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.676e-05	4.971e-05	1.328e-04
B (output stable)	1.685e-05	2.372e-05	4.805e-05
C (output stable)	5.637e-05	1.066e-04	3.426e-04
D (output stable)	7.739e-05	1.005e-04	2.463e-04
A to Z	3.095e-03	4.955e-03	9.828e-03
B to Z	2.921e-03	4.598e-03	8.814e-03
C to Z	2.688e-03	4.368e-03	8.598e-03
D to Z	2.497e-03	4.010e-03	7.550e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

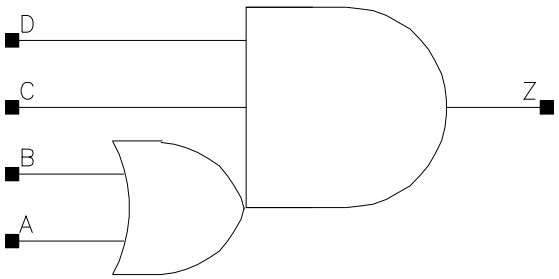
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	-1.855e-06	-3.666e-06	-1.254e-05
B (output stable)	4.606e-07	4.070e-07	-1.461e-06
C (output stable)	-7.633e-06	-1.365e-05	-5.112e-05
D (output stable)	4.391e-06	9.805e-06	3.416e-05
A to Z	-2.619e-06	-4.381e-06	-1.524e-05
B to Z	-8.153e-07	-1.405e-06	-4.672e-06
C to Z	-2.482e-06	-4.323e-06	-1.486e-05
D to Z	-6.584e-07	-1.122e-06	-4.646e-06

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X17_P4	1.200	1.088	1.3056
X25_P4	1.200	1.904	2.2848
X33_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P4	X17_P4	X25_P4	X33_P4
A	0.0006	0.0010	0.0016	0.0019
B	0.0006	0.0010	0.0016	0.0019
C	0.0007	0.0010	0.0016	0.0019
D	0.0006	0.0010	0.0016	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0463	0.0438	1.9156	0.9357
A to Z ↑	0.0391	0.0364	3.3423	1.6208
B to Z ↓	0.0462	0.0421	1.9187	0.9364
B to Z ↑	0.0373	0.0334	3.3458	1.6174
C to Z ↓	0.0368	0.0342	1.8621	0.9135

C to Z ↑	0.0374	0.0343	3.3393	1.6167
D to Z ↓	0.0358	0.0331	1.8618	0.9120
D to Z ↑	0.0387	0.0354	3.3385	1.6175
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**
A to Z ↓	0.0454	0.0444	0.6389	0.4789
A to Z ↑	0.0371	0.0381	1.1017	0.8250
B to Z ↓	0.0436	0.0426	0.6394	0.4791
B to Z ↑	0.0345	0.0352	1.1005	0.8244
C to Z ↓	0.0358	0.0348	0.6231	0.4666
C to Z ↑	0.0353	0.0355	1.0990	0.8231
D to Z ↓	0.0341	0.0334	0.6221	0.4659
D to Z ↑	0.0355	0.0361	1.0989	0.8235

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	1.482e-07	2.276e-12
X17_P4	2.861e-07	2.780e-12
X25_P4	4.553e-07	4.292e-12
X33_P4	5.694e-07	4.545e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	6.349e-05	1.269e-04	2.301e-04	2.583e-04
B (output stable)	4.766e-05	1.052e-04	1.727e-04	1.966e-04
C (output stable)	1.133e-05	1.999e-05	6.179e-05	8.521e-05
D (output stable)	2.725e-05	6.306e-05	1.483e-04	1.489e-04
A to Z	2.574e-03	4.515e-03	7.294e-03	9.112e-03
B to Z	2.403e-03	4.051e-03	6.571e-03	8.202e-03
C to Z	2.814e-03	4.847e-03	8.008e-03	9.760e-03
D to Z	2.692e-03	4.620e-03	7.440e-03	9.193e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

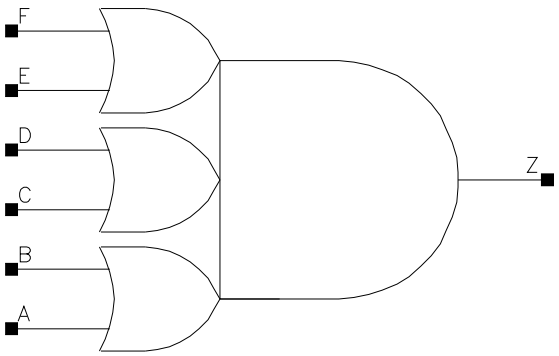
Pin Cycle (vdds)	X8_P4	X17_P4	X25_P4	X33_P4
A (output stable)	-1.807e-06	-5.386e-06	-6.600e-06	-7.595e-06
B (output stable)	-1.047e-06	-3.278e-06	-4.669e-06	-4.671e-06
C (output stable)	5.451e-07	5.829e-07	7.421e-07	-4.140e-08
D (output stable)	6.203e-07	5.760e-07	1.177e-06	3.994e-08
A to Z	-1.891e-06	-6.631e-06	-9.731e-06	-1.065e-05
B to Z	-6.463e-08	-3.958e-07	-3.247e-07	-4.700e-07
C to Z	-6.652e-07	-2.341e-06	-2.696e-06	-3.437e-06
D to Z	-6.892e-07	-2.489e-06	-3.023e-06	-3.801e-06

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	1.224	1.4688
X17_P4	1.200	1.360	1.6320
X33_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
A	0.0007	0.0009	0.0016
B	0.0006	0.0009	0.0018
C	0.0006	0.0009	0.0017
D	0.0007	0.0009	0.0018
E	0.0007	0.0010	0.0017
F	0.0006	0.0009	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	X17_P4	X8_P4	X17_P4
A to Z ↓	0.0612	0.0524	1.9642	0.9537
A to Z ↑	0.0430	0.0388	3.3170	1.6342
B to Z ↓	0.0611	0.0526	1.9651	0.9541
B to Z ↑	0.0416	0.0376	3.3173	1.6348
C to Z ↓	0.0562	0.0498	1.9528	0.9522
C to Z ↑	0.0432	0.0388	3.3189	1.6345
D to Z ↓	0.0564	0.0496	1.9537	0.9527
D to Z ↑	0.0416	0.0371	3.3170	1.6341
E to Z ↓	0.0490	0.0441	1.9393	0.9481
E to Z ↑	0.0400	0.0366	3.3171	1.6343
F to Z ↓	0.0493	0.0434	1.9418	0.9484
F to Z ↑	0.0383	0.0346	3.3144	1.6329
	X33_P4		X33_P4	
A to Z ↓	0.0527		0.4889	
A to Z ↑	0.0398		0.8247	
B to Z ↓	0.0530		0.4891	
B to Z ↑	0.0374		0.8232	
C to Z ↓	0.0488		0.4860	
C to Z ↑	0.0394		0.8244	
D to Z ↓	0.0488		0.4865	
D to Z ↑	0.0373		0.8228	
E to Z ↓	0.0431		0.4840	
E to Z ↑	0.0373		0.8237	
F to Z ↓	0.0430		0.4843	
F to Z ↑	0.0349		0.8226	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.241e-07	3.032e-12
X17_P4	4.100e-07	3.287e-12
X33_P4	7.816e-07	5.556e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X17_P4	X33_P4
A (output stable)	2.149e-05	4.284e-05	7.285e-05
B (output stable)	8.557e-06	1.803e-05	2.660e-05
C (output stable)	4.480e-05	7.332e-05	1.513e-04
D (output stable)	4.171e-05	6.752e-05	1.430e-04
E (output stable)	4.696e-05	7.974e-05	1.465e-04
F (output stable)	1.168e-04	1.718e-04	3.316e-04
A to Z	3.553e-03	5.788e-03	1.121e-02
B to Z	3.369e-03	5.462e-03	1.059e-02
C to Z	3.235e-03	5.340e-03	1.025e-02
D to Z	3.060e-03	5.001e-03	9.608e-03
E to Z	2.811e-03	4.712e-03	9.021e-03
F to Z	2.648e-03	4.365e-03	8.398e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

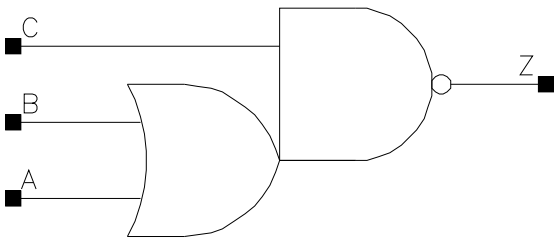
Pin Cycle (vdds)	X8_P4	X17_P4	X33_P4
A (output stable)	-1.431e-06	-3.163e-06	-4.950e-06
B (output stable)	4.666e-07	2.012e-06	4.192e-06
C (output stable)	-3.601e-06	-7.215e-06	-1.387e-05
D (output stable)	2.009e-06	4.649e-06	8.036e-06
E (output stable)	-3.899e-06	-6.703e-06	-1.320e-05
F (output stable)	3.352e-07	2.497e-06	3.017e-06
A to Z	-3.060e-06	-5.863e-06	-9.010e-06
B to Z	-1.356e-06	-2.777e-06	-4.902e-06
C to Z	-3.208e-06	-5.692e-06	-1.091e-05
D to Z	-1.323e-06	-2.386e-06	-4.768e-06
E to Z	-3.022e-06	-5.071e-06	-9.857e-06
F to Z	-1.236e-06	-2.015e-06	-3.875e-06

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.544	0.6528
X17_P4	1.200	1.360	1.6320
X34_P4	1.200	2.720	3.2640
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P4	X17_P4	X34_P4	X46_P4
A	0.0008	0.0023	0.0047	0.0061
B	0.0008	0.0021	0.0042	0.0057
C	0.0008	0.0024	0.0049	0.0065

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X17_P4**	**X6_P4**	**X17_P4**
A to Z ↓	0.0134	0.0139	3.5414	1.1616
A to Z ↑	0.0206	0.0219	6.9160	2.3444
B to Z ↓	0.0111	0.0115	3.4615	1.1691
B to Z ↑	0.0187	0.0187	6.9529	2.3594
C to Z ↓	0.0134	0.0135	3.1994	1.0619
C to Z ↑	0.0184	0.0183	3.3389	1.1094
	X34_P4	**X46_P4**	**X34_P4**	**X46_P4**
A to Z ↓	0.0145	0.0145	0.5931	0.4536

A to Z ↑	0.0226	0.0224	1.1695	0.8982
B to Z ↓	0.0118	0.0119	0.6017	0.4618
B to Z ↑	0.0190	0.0191	1.1777	0.9040
C to Z ↓	0.0140	0.0139	0.5449	0.4175
C to Z ↑	0.0186	0.0185	0.5545	0.4245

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P4	1.414e-07	1.772e-12
X17_P4	3.973e-07	3.284e-12
X34_P4	7.902e-07	5.804e-12
X46_P4	1.039e-06	7.313e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	1.252e-04	4.076e-04	8.445e-04	1.067e-03
B (output stable)	3.921e-05	1.096e-04	2.263e-04	2.981e-04
C (output stable)	5.399e-05	1.965e-04	3.997e-04	4.976e-04
A to Z	1.188e-03	3.868e-03	8.118e-03	1.046e-02
B to Z	8.396e-04	2.552e-03	5.290e-03	6.876e-03
C to Z	1.407e-03	4.337e-03	9.028e-03	1.165e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

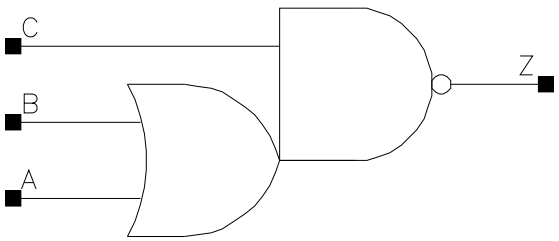
Pin Cycle (vdds)	X6_P4	X17_P4	X34_P4	X46_P4
A (output stable)	-2.905e-06	-1.132e-05	-2.696e-05	-3.266e-05
B (output stable)	-1.231e-06	-5.347e-06	-1.302e-05	-1.558e-05
C (output stable)	3.495e-08	3.523e-06	9.304e-06	1.164e-05
A to Z	-2.997e-06	-1.127e-05	-2.448e-05	-3.209e-05
B to Z	-1.162e-07	-5.120e-07	-1.325e-06	-2.644e-06
C to Z	-6.064e-07	-4.839e-06	-9.805e-06	-1.116e-05

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.544	0.6528
X11_P4	1.200	0.952	1.1424
X17_P4	1.200	1.360	1.6320
X23_P4	1.200	1.904	2.2848
X46_P4	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P4	X11_P4	X17_P4	X23_P4
A	0.0008	0.0016	0.0024	0.0033
B	0.0008	0.0016	0.0023	0.0030
C	0.0008	0.0016	0.0023	0.0031
	X46_P4			
A	0.0066			
B	0.0061			
C	0.0063			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X11_P4	X5_P4	X11_P4
A to Z ↓	0.0144	0.0147	3.5683	1.6668
A to Z ↑	0.0248	0.0251	7.2716	3.4390
B to Z ↓	0.0128	0.0129	3.4983	1.6181

B to Z ↑	0.0234	0.0237	7.3075	3.4557
C to Z ↓	0.0111	0.0111	3.3362	1.5513
C to Z ↑	0.0145	0.0144	3.5745	1.6835
	X17_P4	**X23_P4**	**X17_P4**	**X23_P4**
A to Z ↓	0.0142	0.0148	1.1604	0.8584
A to Z ↑	0.0239	0.0261	2.2793	1.7385
B to Z ↓	0.0124	0.0128	1.1562	0.8583
B to Z ↑	0.0222	0.0231	2.2901	1.7464
C to Z ↓	0.0108	0.0110	1.0930	0.8074
C to Z ↑	0.0136	0.0139	1.1187	0.8522
	X46_P4		**X46_P4**	
A to Z ↓	0.0148		0.4496	
A to Z ↑	0.0256		0.8776	
B to Z ↓	0.0126		0.4445	
B to Z ↑	0.0227		0.8823	
C to Z ↓	0.0111		0.4210	
C to Z ↑	0.0137		0.4309	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P4	1.503e-07	1.771e-12
X11_P4	2.997e-07	2.323e-12
X17_P4	4.380e-07	3.286e-12
X23_P4	5.946e-07	4.291e-12
X46_P4	1.142e-06	7.317e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	3.825e-05	8.476e-05	1.247e-04	2.194e-04
B (output stable)	1.505e-05	3.573e-05	5.145e-05	9.098e-05
C (output stable)	2.704e-04	6.299e-04	7.885e-04	1.197e-03
A to Z	1.536e-03	3.311e-03	4.575e-03	6.917e-03
B to Z	1.174e-03	2.569e-03	3.408e-03	4.914e-03
C to Z	8.373e-04	1.822e-03	2.474e-03	3.617e-03
	X46_P4			
A (output stable)	4.212e-04			
B (output stable)	1.764e-04			
C (output stable)	2.206e-03			
A to Z	1.332e-02			
B to Z	9.366e-03			
C to Z	6.926e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X5_P4	X11_P4	X17_P4	X23_P4
A (output stable)	-2.769e-06	-4.884e-06	-8.365e-06	-1.489e-05
B (output stable)	-1.159e-06	-2.404e-06	-3.792e-06	-8.307e-06
C (output stable)	5.784e-08	-4.239e-06	-3.076e-06	-5.984e-06
A to Z	-3.348e-06	-7.208e-06	-1.059e-05	-2.119e-05
B to Z	3.280e-08	-1.527e-06	-1.303e-06	-2.456e-06
C to Z	-7.120e-07	-1.460e-06	-2.958e-06	-6.273e-06

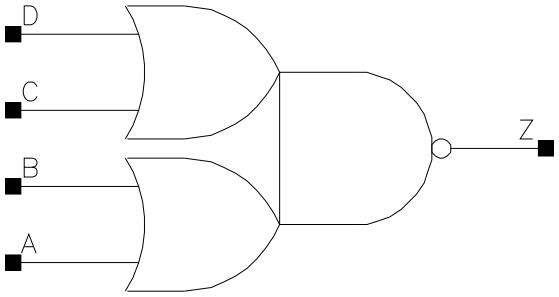
	X46_P4			
A (output stable)	-2.682e-05			
B (output stable)	-1.488e-05			
C (output stable)	-1.007e-05			
A to Z	-3.669e-05			
B to Z	-4.596e-06			
C to Z	-1.109e-05			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.680	0.8160
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.448	2.9376
X42_P4	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0008	0.0016	0.0024	0.0033
B	0.0008	0.0015	0.0022	0.0030
C	0.0008	0.0015	0.0023	0.0032
D	0.0007	0.0014	0.0021	0.0029
	X42_P4			
A	0.0067			
B	0.0060			
C	0.0062			
D	0.0058			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0157	0.0166	3.2770	1.6310
A to Z ↑	0.0284	0.0287	7.6440	3.5129
B to Z ↓	0.0143	0.0147	3.1976	1.6344
B to Z ↑	0.0267	0.0254	7.6667	3.5294
C to Z ↓	0.0138	0.0147	3.3423	1.6501
C to Z ↑	0.0216	0.0231	7.4754	3.5193
D to Z ↓	0.0117	0.0120	3.2508	1.6609
D to Z ↑	0.0196	0.0186	7.5171	3.5464
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0161	0.0163	1.1200	0.8078
A to Z ↑	0.0271	0.0280	2.3628	1.7440
B to Z ↓	0.0145	0.0143	1.1231	0.8059
B to Z ↑	0.0248	0.0250	2.3748	1.7519
C to Z ↓	0.0143	0.0143	1.1348	0.8178
C to Z ↑	0.0218	0.0220	2.3691	1.7449
D to Z ↓	0.0120	0.0117	1.1481	0.8212
D to Z ↑	0.0183	0.0181	2.3869	1.7579
	X42_P4		**X42_P4**	
A to Z ↓	0.0167		0.4257	
A to Z ↑	0.0282		0.8875	
B to Z ↓	0.0147		0.4197	
B to Z ↑	0.0254		0.8913	
C to Z ↓	0.0151		0.4319	
C to Z ↑	0.0225		0.8815	
D to Z ↓	0.0124		0.4277	
D to Z ↑	0.0187		0.8884	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P4	1.795e-07	2.031e-12
X10_P4	3.634e-07	3.285e-12
X15_P4	5.129e-07	4.036e-12
X21_P4	7.015e-07	5.300e-12
X42_P4	1.366e-06	9.328e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	4.522e-05	1.308e-04	1.796e-04	2.584e-04
B (output stable)	1.758e-05	4.304e-05	5.409e-05	7.355e-05
C (output stable)	1.004e-04	3.501e-04	4.140e-04	6.281e-04
D (output stable)	8.887e-05	2.246e-04	2.843e-04	4.161e-04
A to Z	1.871e-03	4.276e-03	5.833e-03	8.255e-03
B to Z	1.521e-03	3.214e-03	4.462e-03	6.229e-03
C to Z	1.291e-03	3.094e-03	4.192e-03	5.791e-03
D to Z	9.618e-04	2.029e-03	2.826e-03	3.812e-03
	X42_P4			
A (output stable)	5.160e-04			
B (output stable)	1.537e-04			
C (output stable)	1.221e-03			
D (output stable)	8.092e-04			

A to Z	1.647e-02			
B to Z	1.251e-02			
C to Z	1.181e-02			
D to Z	7.934e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

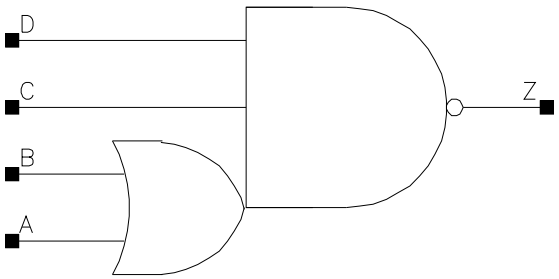
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	-3.332e-06	-1.225e-05	-1.114e-05	-2.075e-05
B (output stable)	6.824e-07	-1.126e-06	-8.232e-08	-1.462e-06
C (output stable)	-1.299e-05	-5.365e-05	-4.373e-05	-8.489e-05
D (output stable)	8.548e-06	3.579e-05	2.832e-05	5.540e-05
A to Z	-4.644e-06	-1.472e-05	-1.358e-05	-2.349e-05
B to Z	-1.042e-06	-4.350e-06	-4.292e-06	-7.708e-06
C to Z	-3.550e-06	-1.508e-05	-1.305e-05	-2.538e-05
D to Z	-9.397e-07	-3.663e-06	-3.727e-06	-6.400e-06
	X42_P4			
A (output stable)	-3.687e-05			
B (output stable)	-2.314e-06			
C (output stable)	-1.510e-04			
D (output stable)	9.895e-05			
A to Z	-4.064e-05			
B to Z	-1.387e-05			
C to Z	-4.643e-05			
D to Z	-1.264e-05			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X21_P4	1.200	2.448	2.9376
X31_P4	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X21_P4	X31_P4
A	0.0008	0.0015	0.0030	0.0046
B	0.0010	0.0014	0.0028	0.0041
C	0.0008	0.0016	0.0032	0.0049
D	0.0008	0.0015	0.0031	0.0046

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0189	0.0182	4.5537	2.4472
A to Z ↑	0.0267	0.0249	6.9237	3.4829
B to Z ↓	0.0169	0.0150	4.6009	2.4562
B to Z ↑	0.0250	0.0214	6.9756	3.5067
C to Z ↓	0.0180	0.0185	4.2968	2.3026

C to Z ↑	0.0219	0.0214	3.2484	1.6362
D to Z ↓	0.0189	0.0182	4.3169	2.3149
D to Z ↑	0.0210	0.0197	3.2922	1.6395
	X21_P4	**X31_P4**	**X21_P4**	**X31_P4**
A to Z ↓	0.0185	0.0187	1.2809	0.8707
A to Z ↑	0.0244	0.0244	1.7408	1.1685
B to Z ↓	0.0152	0.0153	1.2869	0.8776
B to Z ↑	0.0210	0.0210	1.7520	1.1763
C to Z ↓	0.0185	0.0186	1.2066	0.8215
C to Z ↑	0.0211	0.0212	0.8299	0.5601
D to Z ↓	0.0184	0.0186	1.2129	0.8257
D to Z ↑	0.0195	0.0196	0.8311	0.5594

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P4	1.482e-07	2.278e-12
X10_P4	2.813e-07	3.284e-12
X21_P4	5.363e-07	5.299e-12
X31_P4	7.919e-07	7.315e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	1.273e-04	2.733e-04	5.205e-04	7.699e-04
B (output stable)	1.070e-04	2.070e-04	3.900e-04	5.706e-04
C (output stable)	2.256e-05	5.971e-05	1.044e-04	1.507e-04
D (output stable)	5.873e-05	1.560e-04	2.844e-04	4.124e-04
A to Z	1.866e-03	3.242e-03	6.290e-03	9.356e-03
B to Z	1.379e-03	2.217e-03	4.265e-03	6.396e-03
C to Z	2.183e-03	4.144e-03	7.955e-03	1.186e-02
D to Z	1.970e-03	3.486e-03	6.718e-03	1.002e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

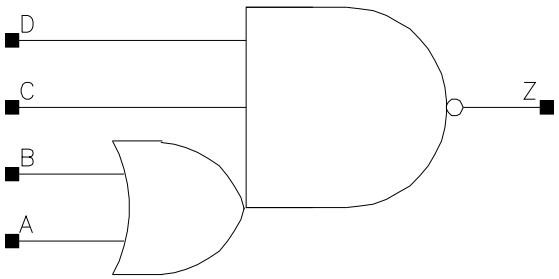
Pin Cycle (vdds)	X5_P4	X10_P4	X21_P4	X31_P4
A (output stable)	-5.637e-06	-9.108e-06	-1.610e-05	-2.238e-05
B (output stable)	-4.009e-06	-5.587e-06	-1.002e-05	-1.372e-05
C (output stable)	5.724e-07	9.396e-07	2.039e-06	2.614e-06
D (output stable)	6.159e-07	1.510e-06	3.052e-06	3.762e-06
A to Z	-7.077e-06	-1.092e-05	-1.878e-05	-2.528e-05
B to Z	-1.730e-07	2.210e-07	4.920e-07	6.610e-07
C to Z	-2.166e-06	-3.463e-06	-5.908e-06	-5.733e-06
D to Z	-1.687e-06	-3.675e-06	-6.109e-06	-1.106e-05

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.200	0.816	0.9792
X10_P4	1.200	1.360	1.6320
X15_P4	1.200	1.768	2.1216
X21_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X15_P4	X21_P4
A	0.0009	0.0017	0.0025	0.0033
B	0.0008	0.0015	0.0023	0.0030
C	0.0008	0.0015	0.0024	0.0031
D	0.0008	0.0015	0.0022	0.0030

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0184	0.0197	4.6483	2.4313
A to Z ↑	0.0285	0.0307	6.7271	3.4280
B to Z ↓	0.0165	0.0173	4.5548	2.4314
B to Z ↑	0.0275	0.0283	6.7519	3.4409
C to Z ↓	0.0152	0.0169	4.3822	2.3125

C to Z ↑	0.0178	0.0186	3.3114	1.6745
D to Z ↓	0.0145	0.0151	4.4147	2.3300
D to Z ↑	0.0159	0.0161	3.3350	1.6873
	X15_P4	**X21_P4**	**X15_P4**	**X21_P4**
A to Z ↓	0.0194	0.0196	1.6781	1.2657
A to Z ↑	0.0297	0.0302	2.3079	1.7503
B to Z ↓	0.0173	0.0172	1.6686	1.2632
B to Z ↑	0.0275	0.0281	2.3179	1.7561
C to Z ↓	0.0166	0.0168	1.5907	1.2010
C to Z ↑	0.0180	0.0182	1.1156	0.8404
D to Z ↓	0.0149	0.0153	1.6033	1.2097
D to Z ↑	0.0155	0.0158	1.1246	0.8468

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X5_P4	1.622e-07	2.276e-12
X10_P4	3.196e-07	3.284e-12
X15_P4	4.527e-07	4.040e-12
X21_P4	6.184e-07	5.553e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	2.504e-05	6.625e-05	9.416e-05	1.267e-04
B (output stable)	2.556e-05	9.292e-05	1.167e-04	1.678e-04
C (output stable)	7.408e-05	1.431e-04	2.229e-04	2.878e-04
D (output stable)	1.672e-04	5.296e-04	6.576e-04	9.532e-04
A to Z	2.125e-03	4.649e-03	6.576e-03	8.993e-03
B to Z	1.737e-03	3.629e-03	5.112e-03	7.009e-03
C to Z	1.358e-03	3.076e-03	4.269e-03	5.885e-03
D to Z	1.109e-03	2.350e-03	3.303e-03	4.508e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

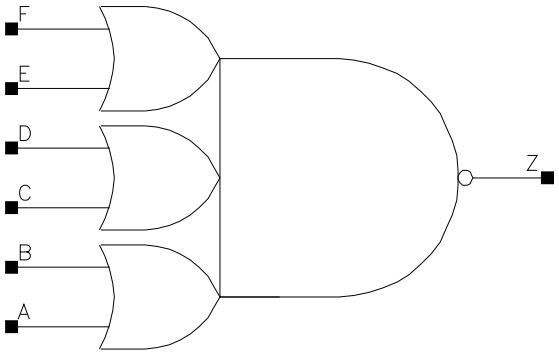
Pin Cycle (vdds)	X5_P4	X10_P4	X15_P4	X21_P4
A (output stable)	-2.470e-06	-7.858e-06	-7.518e-06	-1.349e-05
B (output stable)	-6.931e-07	-4.822e-06	-4.239e-06	-8.021e-06
C (output stable)	8.374e-09	1.764e-06	7.673e-07	3.110e-06
D (output stable)	2.666e-08	-2.457e-06	-2.867e-06	-4.595e-06
A to Z	-2.675e-06	-1.289e-05	-1.216e-05	-2.217e-05
B to Z	3.400e-08	-2.457e-06	-3.284e-06	-5.045e-06
C to Z	-8.723e-07	-2.709e-06	-2.809e-06	-4.064e-06
D to Z	-7.707e-07	-3.226e-06	-2.640e-06	-4.770e-06

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	1.200	1.088	1.3056
X9_P4	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X9_P4
A	0.0007	0.0017
B	0.0007	0.0015
C	0.0007	0.0016
D	0.0006	0.0015
E	0.0007	0.0016
F	0.0007	0.0014

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X9_P4	X3_P4	X9_P4
A to Z ↓	0.0228	0.0240	5.3323	2.2106
A to Z ↑	0.0371	0.0356	9.4171	3.4447
B to Z ↓	0.0216	0.0217	5.3666	2.2099
B to Z ↑	0.0371	0.0332	9.4403	3.4557
C to Z ↓	0.0222	0.0228	5.3743	2.2216
C to Z ↑	0.0325	0.0312	9.4410	3.4382
D to Z ↓	0.0205	0.0203	5.4093	2.2247
D to Z ↑	0.0322	0.0285	9.4740	3.4526
E to Z ↓	0.0187	0.0197	5.4128	2.2252
E to Z ↑	0.0259	0.0255	9.4671	3.4405
F to Z ↓	0.0171	0.0168	5.4540	2.2298
F to Z ↑	0.0251	0.0218	9.5207	3.4627

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X3_P4	1.899e-07	2.780e-12
X9_P4	4.737e-07	4.545e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X3_P4	X9_P4
A (output stable)	2.821e-05	1.075e-04
B (output stable)	1.131e-05	4.206e-05
C (output stable)	5.606e-05	2.248e-04
D (output stable)	6.218e-05	1.905e-04
E (output stable)	6.049e-05	2.187e-04
F (output stable)	1.567e-04	3.732e-04
A to Z	2.468e-03	6.443e-03
B to Z	2.217e-03	5.395e-03
C to Z	2.022e-03	5.276e-03
D to Z	1.771e-03	4.290e-03
E to Z	1.467e-03	4.022e-03
F to Z	1.227e-03	3.003e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

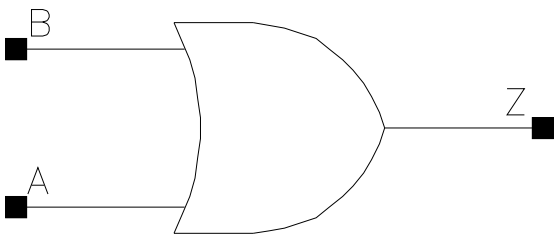
Pin Cycle (vdds)	X3_P4	X9_P4
A (output stable)	-2.105e-06	-1.033e-05
B (output stable)	1.122e-06	6.171e-07
C (output stable)	-5.087e-06	-2.677e-05
D (output stable)	3.255e-06	1.461e-05
E (output stable)	-5.101e-06	-2.625e-05
F (output stable)	9.401e-07	6.857e-06
A to Z	-4.026e-06	-1.635e-05
B to Z	-2.046e-06	-6.930e-06
C to Z	-4.036e-06	-1.923e-05
D to Z	-1.949e-06	-7.791e-06
E to Z	-3.221e-06	-1.900e-05
F to Z	-1.211e-06	-7.232e-06

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.544	0.6528
X16_P4	1.200	0.680	0.8160
X33_P4	1.200	1.360	1.6320
X50_P4	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P4	X16_P4	X33_P4	X50_P4
A	0.0008	0.0009	0.0018	0.0018
B	0.0006	0.0009	0.0019	0.0019

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0425	0.0383	1.8727	0.9454
A to Z ↑	0.0237	0.0246	3.2646	1.6443
B to Z ↓	0.0414	0.0374	1.8741	0.9468
B to Z ↑	0.0226	0.0231	3.2630	1.6458
	X33_P4	**X50_P4**	**X33_P4**	**X50_P4**
A to Z ↓	0.0394	0.0457	0.4689	0.3243
A to Z ↑	0.0243	0.0243	0.8027	0.5424
B to Z ↓	0.0370	0.0438	0.4694	0.3246
B to Z ↑	0.0225	0.0229	0.8019	0.5424

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	1.765e-07	1.771e-12
X16_P4	3.039e-07	2.025e-12
X33_P4	5.980e-07	3.286e-12
X50_P4	7.918e-07	3.786e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	3.166e-05	6.149e-05	1.606e-04	1.538e-04
B (output stable)	6.000e-06	8.340e-06	9.284e-05	8.148e-05
A to Z	2.361e-03	3.783e-03	7.900e-03	1.046e-02
B to Z	2.162e-03	3.432e-03	6.881e-03	9.502e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

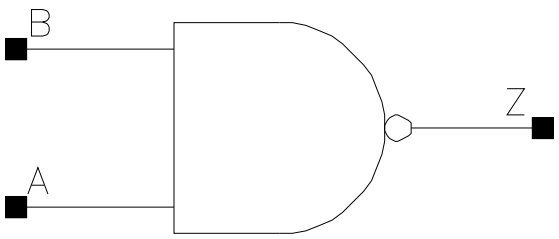
Pin Cycle (vdds)	X8_P4	X16_P4	X33_P4	X50_P4
A (output stable)	-2.529e-06	-4.691e-06	-1.558e-05	-1.557e-05
B (output stable)	1.360e-05	2.559e-05	9.434e-05	9.264e-05
A to Z	-1.917e-06	-3.150e-06	-1.248e-05	-1.233e-05
B to Z	3.900e-09	-2.917e-07	-3.358e-07	-2.080e-07

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.816	0.9792
X16_P4	1.200	0.952	1.1424
X24_P4	1.200	1.088	1.3056
X32_P4	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P4	X16_P4	X24_P4	X32_P4
A	0.0009	0.0010	0.0010	0.0009
B	0.0010	0.0011	0.0011	0.0011

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0320	0.0333	1.8087	0.9445
A to Z ↑	0.0364	0.0372	3.3045	1.6876
B to Z ↓	0.0329	0.0342	1.8085	0.9445
B to Z ↑	0.0349	0.0352	3.3004	1.6869
	X24_P4	**X32_P4**	**X24_P4**	**X32_P4**
A to Z ↓	0.0367	0.0371	0.6405	0.4805
A to Z ↑	0.0396	0.0406	1.1275	0.8421
B to Z ↓	0.0376	0.0382	0.6406	0.4799
B to Z ↑	0.0375	0.0391	1.1272	0.8417

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	3.081e-07	2.277e-12
X16_P4	4.042e-07	2.527e-12
X24_P4	4.931e-07	2.779e-12
X32_P4	6.121e-07	3.028e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	2.538e-05	2.548e-05	2.558e-05	2.610e-05
B (output stable)	7.347e-05	7.368e-05	7.379e-05	7.531e-05
A to Z	4.606e-03	5.320e-03	6.675e-03	8.802e-03
B to Z	4.384e-03	5.107e-03	6.470e-03	8.578e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

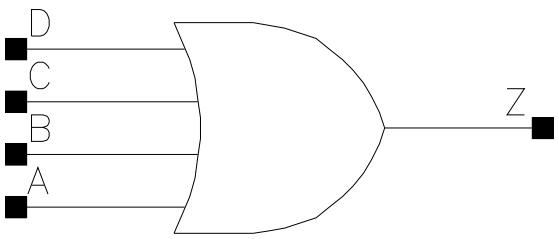
Pin Cycle (vdds)	X8_P4	X16_P4	X24_P4	X32_P4
A (output stable)	3.074e-08	3.310e-08	3.327e-08	4.173e-08
B (output stable)	-8.420e-09	-7.780e-09	-7.290e-09	-9.550e-09
A to Z	-3.272e-07	7.050e-08	-4.000e-07	-2.850e-07
B to Z	1.467e-07	-2.200e-08	-6.000e-08	-2.042e-07

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P4	1.200	2.176	2.6112
X27_P4	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P4	X27_P4
A	0.0016	0.0019
B	0.0015	0.0019
C	0.0016	0.0019
D	0.0015	0.0020

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P4	X27_P4	X20_P4	X27_P4
A to Z ↓	0.0433	0.0452	1.1386	0.8516
A to Z ↑	0.0253	0.0245	1.0758	0.8018
B to Z ↓	0.0414	0.0427	1.1378	0.8519
B to Z ↑	0.0241	0.0229	1.0749	0.8002
C to Z ↓	0.0416	0.0437	1.1378	0.8500
C to Z ↑	0.0241	0.0240	1.0778	0.8034
D to Z ↓	0.0397	0.0416	1.1382	0.8504
D to Z ↑	0.0229	0.0227	1.0766	0.8032

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X20_P4	5.674e-07	4.796e-12
X27_P4	7.813e-07	5.553e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X20_P4	X27_P4
A (output stable)	1.803e-03	2.467e-03
B (output stable)	1.439e-03	1.944e-03
C (output stable)	1.753e-03	2.523e-03
D (output stable)	1.296e-03	1.895e-03
A to Z	7.515e-03	1.051e-02
B to Z	6.788e-03	9.450e-03
C to Z	6.564e-03	9.100e-03
D to Z	5.833e-03	8.151e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

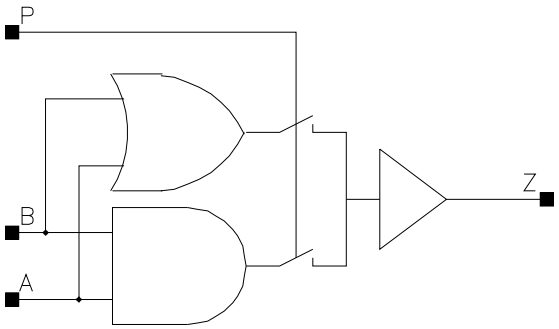
Pin Cycle (vdds)	X20_P4	X27_P4
A (output stable)	-6.986e-06	-1.353e-05
B (output stable)	2.150e-06	4.284e-06
C (output stable)	-2.170e-05	-4.686e-05
D (output stable)	1.465e-05	3.017e-05
A to Z	-6.236e-06	-1.230e-05
B to Z	-1.700e-08	2.000e-08
C to Z	-5.750e-06	-1.193e-05
D to Z	3.900e-08	3.120e-07

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	0.952	1.1424
X16_P4	1.200	1.224	1.4688
X25_P4	1.200	2.040	2.4480
X33_P4	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P4	X16_P4	X25_P4	X33_P4
A	0.0012	0.0017	0.0030	0.0030
B	0.0011	0.0017	0.0034	0.0034
P	0.0006	0.0009	0.0018	0.0018

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0510	0.0467	1.9134	0.9363
A to Z ↑	0.0315	0.0294	3.3055	1.6540
B to Z ↓	0.0503	0.0462	1.9254	0.9438
B to Z ↑	0.0324	0.0303	3.3101	1.6564
P to Z ↓	0.0456	0.0423	1.9310	0.9463
P to Z ↑	0.0314	0.0295	3.3090	1.6547
	X25_P4	**X33_P4**	**X25_P4**	**X33_P4**

A to Z ↓	0.0449	0.0478	0.6378	0.4834
A to Z ↑	0.0294	0.0308	1.1132	0.8339
B to Z ↓	0.0442	0.0468	0.6419	0.4861
B to Z ↑	0.0306	0.0318	1.1154	0.8341
P to Z ↓	0.0410	0.0438	0.6431	0.4873
P to Z ↑	0.0291	0.0305	1.1130	0.8327

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	2.049e-07	2.528e-12
X16_P4	3.930e-07	3.037e-12
X25_P4	6.654e-07	4.543e-12
X33_P4	7.455e-07	4.796e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	5.678e-05	1.053e-04	2.074e-04	2.096e-04
B (output stable)	1.747e-04	3.058e-04	5.556e-04	5.630e-04
P (output stable)	1.264e-04	2.075e-04	3.694e-04	3.759e-04
A to Z	2.743e-03	4.605e-03	8.018e-03	9.185e-03
B to Z	2.644e-03	4.438e-03	7.636e-03	8.814e-03
P to Z	2.364e-03	4.030e-03	7.026e-03	8.184e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

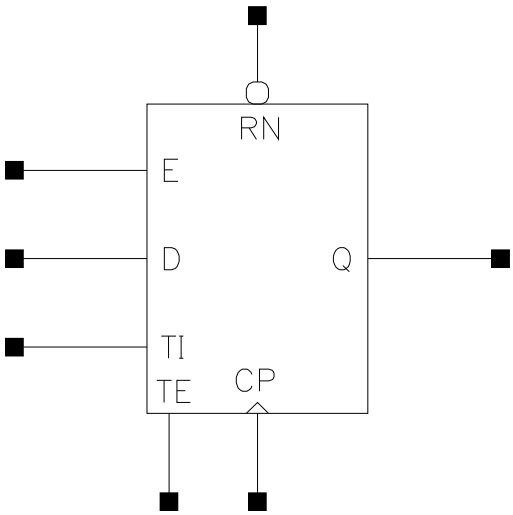
Pin Cycle (vdds)	X8_P4	X16_P4	X25_P4	X33_P4
A (output stable)	-3.401e-06	-6.954e-06	-1.210e-05	-1.213e-05
B (output stable)	-2.003e-05	-3.409e-05	-3.970e-05	-4.007e-05
P (output stable)	1.985e-05	3.915e-05	5.578e-05	5.661e-05
A to Z	-4.280e-06	-7.397e-06	-1.020e-05	-1.046e-05
B to Z	-3.476e-06	-5.639e-06	-8.218e-06	-8.516e-06
P to Z	-8.827e-07	-1.602e-06	-3.483e-06	-3.415e-06

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.488	5.3856
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0006	0.0006	0.0006
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0007	0.0007	0.0008
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.0911	0.0473	4.1903	1.8693
CP to Q ↑	0.0701	0.0595	6.6600	3.2787
RN to Q ↓	0.0754	0.0628	3.5154	1.9834
	X17_P4	X33_P4	X17_P4	X33_P4
CP to Q ↓	0.0793	0.0832	0.9031	0.4770
CP to Q ↑	0.0968	0.1009	1.6103	0.8213
RN to Q ↓	0.1059	0.1096	0.9014	0.4763

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1378	0.0919	0.0919	0.0919
CP ↑	min_pulse_width to CP	0.0820	0.0396	0.0358	0.0358
D ↓	hold_rising to CP	-0.1450	-0.0748	-0.0748	-0.0748
D ↑	hold_rising to CP	-0.0698	-0.0208	-0.0239	-0.0239
D ↓	setup_rising to CP	0.2016	0.1295	0.1295	0.1291
D ↑	setup_rising to CP	0.1044	0.0560	0.0560	0.0560
E ↓	hold_rising to CP	-0.0818	-0.0840	-0.0840	-0.0840
E ↑	hold_rising to CP	-0.0680	-0.0237	-0.0237	-0.0237
E ↓	setup_rising to CP	0.1677	0.1681	0.1681	0.1681
E ↑	setup_rising to CP	0.1905	0.1319	0.1319	0.1319
RN ↓	min_pulse_width to RN	0.0823	0.0876	0.0779	0.0779
RN ↑	recovery_rising to CP	0.0244	0.0219	0.0219	0.0219
RN ↑	removal_rising to CP	-0.0144	-0.0099	-0.0099	-0.0099
TE ↓	hold_rising to CP	-0.0620	-0.0503	-0.0503	-0.0503
TE ↑	hold_rising to CP	-0.0454	-0.0259	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1340	0.1051	0.1051	0.1051
TE ↑	setup_rising to CP	0.2372	0.1635	0.1635	0.1635
TI ↓	hold_rising to CP	-0.1807	-0.0964	-0.0964	-0.0964
TI ↑	hold_rising to CP	-0.0547	-0.0277	-0.0275	-0.0275
TI ↓	setup_rising to CP	0.2348	0.1542	0.1542	0.1542
TI ↑	setup_rising to CP	0.0898	0.0637	0.0637	0.0637

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	7.320e-07	9.677e-12
X8_P4	7.747e-07	9.081e-12
X17_P4	9.198e-07	9.584e-12
X33_P4	1.091e-06	1.009e-11

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

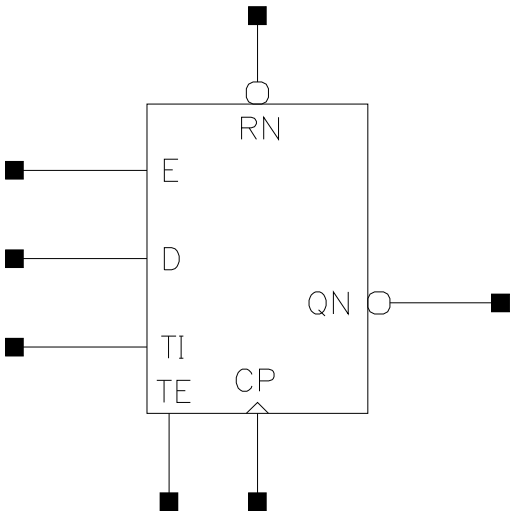
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	4.355e-03	4.388e-03	4.396e-03	4.400e-03
Clock 100Mhz Data 25Mhz	7.066e-03	7.232e-03	7.930e-03	8.682e-03
Clock 100Mhz Data 50Mhz	9.776e-03	1.008e-02	1.146e-02	1.296e-02
Clock = 0 Data 100Mhz	6.144e-03	6.019e-03	5.979e-03	5.960e-03
Clock = 1 Data 100Mhz	2.430e-03	2.455e-03	2.465e-03	2.470e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.760	5.7120
X8_P4	1.200	4.624	5.5488
X17_P4	1.200	4.760	5.7120
X33_P4	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0006	0.0006	0.0006
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.0870	0.0809	3.4265	1.7977
CP to QN ↑	0.1009	0.0616	6.5443	3.1868
RN to QN ↑	0.0907	0.0900	6.5209	3.1818
	X17_P4	X33_P4	X17_P4	X33_P4
CP to QN ↓	0.0766	0.0808	0.9051	0.4772
CP to QN ↑	0.0652	0.0706	1.6097	0.8228
RN to QN ↑	0.0887	0.0969	1.6154	0.8249

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1378	0.0919	0.0919	0.0919
CP ↑	min_pulse_width to CP	0.0589	0.0358	0.0406	0.0406
D ↓	hold_rising to CP	-0.1475	-0.0748	-0.0748	-0.0748
D ↑	hold_rising to CP	-0.0698	-0.0239	-0.0208	-0.0212
D ↓	setup_rising to CP	0.2047	0.1295	0.1291	0.1291
D ↑	setup_rising to CP	0.1044	0.0560	0.0560	0.0560
E ↓	hold_rising to CP	-0.0815	-0.0840	-0.0840	-0.0815
E ↑	hold_rising to CP	-0.0680	-0.0237	-0.0237	-0.0237
E ↓	setup_rising to CP	0.1702	0.1681	0.1681	0.1681
E ↑	setup_rising to CP	0.1932	0.1319	0.1319	0.1319
RN ↓	min_pulse_width to RN	0.0774	0.0779	0.0872	0.0942
RN ↑	recovery_rising to CP	0.0244	0.0244	0.0219	0.0219
RN ↑	removal_rising to CP	-0.0144	-0.0126	-0.0099	-0.0099
TE ↓	hold_rising to CP	-0.0645	-0.0503	-0.0507	-0.0477
TE ↑	hold_rising to CP	-0.0454	-0.0286	-0.0259	-0.0259
TE ↓	setup_rising to CP	0.1340	0.1051	0.1051	0.1051
TE ↑	setup_rising to CP	0.2372	0.1660	0.1660	0.1691
TI ↓	hold_rising to CP	-0.1807	-0.0964	-0.0949	-0.0949
TI ↑	hold_rising to CP	-0.0547	-0.0275	-0.0277	-0.0277
TI ↓	setup_rising to CP	0.2348	0.1542	0.1542	0.1542
TI ↑	setup_rising to CP	0.0898	0.0637	0.0637	0.0637

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	7.519e-07	9.677e-12
X8_P4	8.007e-07	9.333e-12
X17_P4	9.488e-07	9.585e-12
X33_P4	1.136e-06	1.009e-11

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

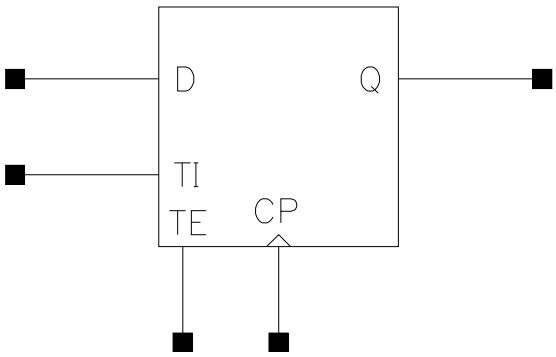
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	4.339e-03	4.372e-03	4.377e-03	4.380e-03
Clock 100Mhz Data 25Mhz	7.052e-03	7.269e-03	7.862e-03	8.598e-03
Clock 100Mhz Data 50Mhz	9.765e-03	1.017e-02	1.135e-02	1.282e-02
Clock = 0 Data 100Mhz	6.140e-03	6.017e-03	5.978e-03	5.959e-03
Clock = 1 Data 100Mhz	2.429e-03	2.455e-03	2.466e-03	2.471e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.400	4.0800
X8_P4	1.200	3.128	3.7536
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0743	0.0440	3.9385	1.8677
CP to Q ↑	0.0629	0.0541	6.7134	3.2342
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0654	0.0712	0.8856	0.4683
CP to Q ↑	0.0940	0.0988	1.6049	0.8193

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1185	0.1210	0.1210	0.1210
CP ↑	min_pulse_width to CP	0.0577	0.0347	0.0310	0.0310
D ↓	hold_rising to CP	-0.0889	-0.0413	-0.0410	-0.0410
D ↑	hold_rising to CP	-0.0252	-0.0016	-0.0042	-0.0042
D ↓	setup_rising to CP	0.1312	0.0879	0.0879	0.0879
D ↑	setup_rising to CP	0.0557	0.0317	0.0317	0.0317
TE ↓	hold_rising to CP	-0.0473	-0.0330	-0.0330	-0.0330
TE ↑	hold_rising to CP	-0.0357	-0.0215	-0.0215	-0.0215
TE ↓	setup_rising to CP	0.1118	0.0852	0.0852	0.0852
TE ↑	setup_rising to CP	0.2075	0.1691	0.1691	0.1691
TI ↓	hold_rising to CP	-0.1710	-0.1062	-0.1062	-0.1062
TI ↑	hold_rising to CP	-0.0414	-0.0226	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.2153	0.1617	0.1617	0.1617
TI ↑	setup_rising to CP	0.0711	0.0539	0.0539	0.0539

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	5.722e-07	7.064e-12
X8_P4	6.229e-07	6.561e-12
X17_P4	8.236e-07	7.317e-12
X33_P4	9.786e-07	7.821e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

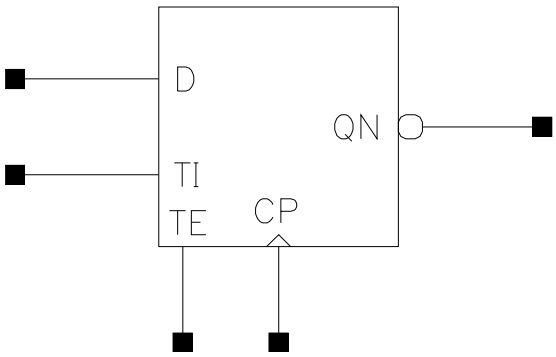
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.888e-03	3.898e-03	3.898e-03	3.897e-03
Clock 100Mhz Data 25Mhz	5.793e-03	5.891e-03	6.579e-03	7.182e-03
Clock 100Mhz Data 50Mhz	7.699e-03	7.885e-03	9.260e-03	1.047e-02
Clock = 0 Data 100Mhz	4.864e-03	4.615e-03	4.531e-03	4.490e-03
Clock = 1 Data 100Mhz	1.381e-03	7.322e-04	5.160e-04	4.079e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.536	4.2432
X8_P4	1.200	3.264	3.9168
X17_P4	1.200	3.536	4.2432
X33_P4	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0813	0.0857	3.9285	1.8608
CP to QN ↑	0.0810	0.0565	6.6730	3.1970
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0655	0.0719	0.8871	0.4683
CP to QN ↑	0.0571	0.0623	1.6062	0.8187

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1167	0.1210	0.1210	0.1210
CP ↑	min_pulse_width to CP	0.0443	0.0310	0.0358	0.0358
D ↓	hold_rising to CP	-0.0889	-0.0410	-0.0413	-0.0413
D ↑	hold_rising to CP	-0.0252	-0.0042	-0.0016	-0.0016
D ↓	setup_rising to CP	0.1315	0.0879	0.0879	0.0879
D ↑	setup_rising to CP	0.0557	0.0317	0.0317	0.0317
TE ↓	hold_rising to CP	-0.0473	-0.0330	-0.0330	-0.0330
TE ↑	hold_rising to CP	-0.0357	-0.0215	-0.0215	-0.0215
TE ↓	setup_rising to CP	0.1118	0.0852	0.0852	0.0852
TE ↑	setup_rising to CP	0.2082	0.1660	0.1691	0.1691
TI ↓	hold_rising to CP	-0.1710	-0.1062	-0.1062	-0.1062
TI ↑	hold_rising to CP	-0.0409	-0.0241	-0.0226	-0.0226
TI ↓	setup_rising to CP	0.2158	0.1617	0.1617	0.1617
TI ↑	setup_rising to CP	0.0746	0.0539	0.0540	0.0540

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	5.794e-07	7.316e-12
X8_P4	6.290e-07	6.813e-12
X17_P4	8.176e-07	7.317e-12
X33_P4	9.726e-07	7.821e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

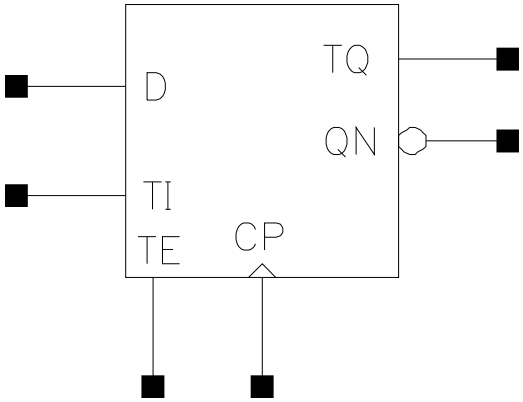
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.843e-03	3.884e-03	3.897e-03	3.904e-03
Clock 100Mhz Data 25Mhz	5.807e-03	5.981e-03	6.533e-03	7.146e-03
Clock 100Mhz Data 50Mhz	7.770e-03	8.077e-03	9.168e-03	1.039e-02
Clock = 0 Data 100Mhz	4.901e-03	4.646e-03	4.562e-03	4.519e-03
Clock = 1 Data 100Mhz	1.375e-03	7.399e-04	5.283e-04	4.226e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.536	4.2432
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0012	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010

TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0897	0.0764	3.5457	1.8076
CP to QN ↑	0.0985	0.0597	6.5961	3.2185
CP to TQ ↓	0.0692	0.0409	4.9485	3.4277
CP to TQ ↑	0.0647	0.0539	12.6212	8.9670
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0721	0.0780	0.9093	0.4808
CP to QN ↑	0.0613	0.0658	1.6298	0.8381
CP to TQ ↓	0.0425	0.0444	4.5492	4.5720
CP to TQ ↑	0.0548	0.0561	11.7046	12.3946

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1166	0.1210	0.1210	0.1210
CP ↑	min_pulse_width to CP	0.0589	0.0358	0.0358	0.0358
D ↓	hold_rising to CP	-0.0889	-0.0413	-0.0413	-0.0413
D ↑	hold_rising to CP	-0.0255	-0.0016	-0.0016	-0.0016
D ↓	setup_rising to CP	0.1316	0.0849	0.0849	0.0849
D ↑	setup_rising to CP	0.0557	0.0317	0.0317	0.0317
TE ↓	hold_rising to CP	-0.0473	-0.0330	-0.0330	-0.0333
TE ↑	hold_rising to CP	-0.0357	-0.0215	-0.0215	-0.0215
TE ↓	setup_rising to CP	0.1096	0.0856	0.0852	0.0856
TE ↑	setup_rising to CP	0.2082	0.1660	0.1660	0.1660
TI ↓	hold_rising to CP	-0.1710	-0.1067	-0.1067	-0.1067
TI ↑	hold_rising to CP	-0.0414	-0.0241	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.2158	0.1617	0.1617	0.1617
TI ↑	setup_rising to CP	0.0711	0.0540	0.0540	0.0540

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	6.341e-07	7.834e-12
X8_P4	6.939e-07	7.317e-12
X17_P4	7.912e-07	7.569e-12
X33_P4	9.759e-07	8.073e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4

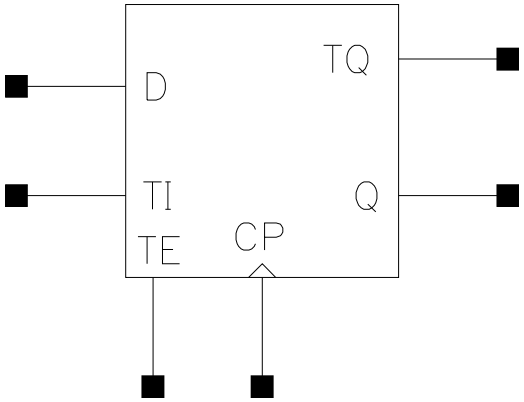
Clock 100Mhz Data 0Mhz	3.949e-03	3.926e-03	3.916e-03	3.911e-03
Clock 100Mhz Data 25Mhz	6.097e-03	6.266e-03	6.531e-03	7.254e-03
Clock 100Mhz Data 50Mhz	8.245e-03	8.607e-03	9.147e-03	1.060e-02
Clock = 0 Data 100Mhz	4.878e-03	4.625e-03	4.543e-03	4.501e-03
Clock = 1 Data 100Mhz	1.382e-03	7.122e-04	4.888e-04	3.772e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.672	4.4064
X8_P4	1.200	3.400	4.0800
X17_P4	1.200	3.672	4.4064
X33_P4	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007

TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0971	0.0494	4.1942	1.8641
CP to Q ↑	0.0716	0.0573	6.8062	3.2541
CP to TQ ↓	0.0947	0.0523	4.1663	4.6765
CP to TQ ↑	0.0735	0.0629	9.0347	12.5823
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0669	0.0730	0.9143	0.4791
CP to Q ↑	0.0955	0.1003	1.6397	0.8246
CP to TQ ↓	0.0697	0.0774	4.4488	4.5380
CP to TQ ↑	0.1009	0.1079	12.1350	12.2782

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1185	0.1210	0.1210	0.1210
CP ↑	min_pulse_width to CP	0.0831	0.0358	0.0310	0.0310
D ↓	hold_rising to CP	-0.0889	-0.0413	-0.0410	-0.0410
D ↑	hold_rising to CP	-0.0252	-0.0016	-0.0042	-0.0042
D ↓	setup_rising to CP	0.1312	0.0849	0.0879	0.0879
D ↑	setup_rising to CP	0.0557	0.0317	0.0317	0.0317
TE ↓	hold_rising to CP	-0.0473	-0.0333	-0.0330	-0.0330
TE ↑	hold_rising to CP	-0.0357	-0.0215	-0.0215	-0.0215
TE ↓	setup_rising to CP	0.1118	0.0852	0.0852	0.0852
TE ↑	setup_rising to CP	0.2079	0.1660	0.1691	0.1691
TI ↓	hold_rising to CP	-0.1710	-0.1067	-0.1062	-0.1062
TI ↑	hold_rising to CP	-0.0414	-0.0185	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.2153	0.1617	0.1617	0.1617
TI ↑	setup_rising to CP	0.0706	0.0539	0.0539	0.0539

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	6.315e-07	7.568e-12
X8_P4	6.644e-07	7.065e-12
X17_P4	8.561e-07	7.569e-12
X33_P4	1.010e-06	8.073e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

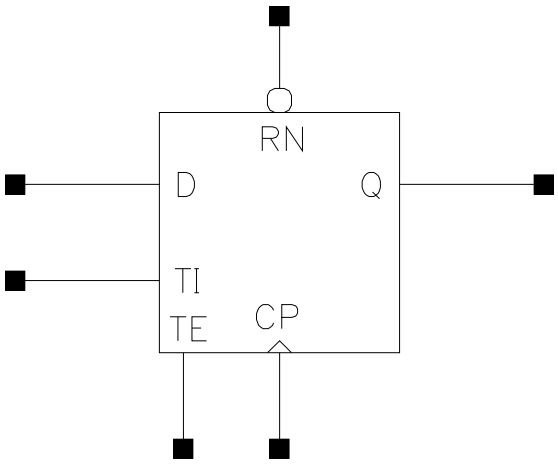
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	3.861e-03	3.879e-03	3.884e-03	3.886e-03
Clock 100Mhz Data 25Mhz	6.068e-03	6.095e-03	6.753e-03	7.405e-03
Clock 100Mhz Data 50Mhz	8.275e-03	8.311e-03	9.622e-03	1.092e-02
Clock = 0 Data 100Mhz	4.859e-03	4.610e-03	4.529e-03	4.489e-03
Clock = 1 Data 100Mhz	1.372e-03	7.073e-04	4.859e-04	3.752e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.672	4.4064
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006
RN	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.0894	0.0472	4.2706	1.8747
CP to Q ↑	0.0693	0.0583	6.7060	3.2744
RN to Q ↓	0.0744	0.0635	3.5734	1.9689
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0687	0.0750	0.8984	0.4764
CP to Q ↑	0.0857	0.0901	1.6051	0.8197
RN to Q ↓	0.0957	0.1020	0.8949	0.4749

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1311	0.1258	0.1301	0.1301
CP ↑	min_pulse_width to CP	0.0734	0.0358	0.0310	0.0310
D ↓	hold_rising to CP	-0.0822	-0.0315	-0.0315	-0.0315
D ↑	hold_rising to CP	-0.0335	-0.0068	-0.0090	-0.0090
D ↓	setup_rising to CP	0.1315	0.0856	0.0856	0.0856
D ↑	setup_rising to CP	0.0655	0.0390	0.0387	0.0387
RN ↓	min_pulse_width to RN	0.0774	0.0801	0.0779	0.0779
RN ↑	recovery_rising to CP	0.0244	0.0244	0.0244	0.0244
RN ↑	removal_rising to CP	-0.0175	-0.0126	-0.0126	-0.0126
TE ↓	hold_rising to CP	-0.0525	-0.0259	-0.0259	-0.0259
TE ↑	hold_rising to CP	-0.0457	-0.0264	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1118	0.0801	0.0831	0.0831
TE ↑	setup_rising to CP	0.2082	0.1612	0.1642	0.1642
TI ↓	hold_rising to CP	-0.1561	-0.0921	-0.0915	-0.0915
TI ↑	hold_rising to CP	-0.0496	-0.0290	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.2158	0.1568	0.1609	0.1609
TI ↑	setup_rising to CP	0.0849	0.0637	0.0635	0.0635

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	6.492e-07	8.072e-12
X8_P4	6.866e-07	7.568e-12
X17_P4	8.699e-07	8.325e-12
X33_P4	1.011e-06	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	4.356e-03	4.393e-03	4.427e-03	4.444e-03

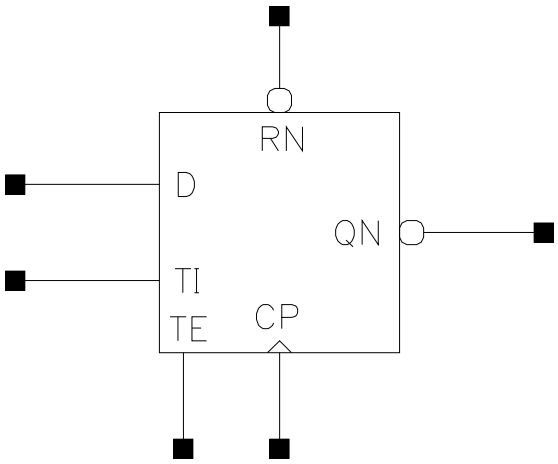
Clock 100Mhz Data 25Mhz	6.521e-03	6.535e-03	7.370e-03	8.023e-03
Clock 100Mhz Data 50Mhz	8.685e-03	8.678e-03	1.031e-02	1.160e-02
Clock = 0 Data 100Mhz	5.042e-03	4.705e-03	4.593e-03	4.537e-03
Clock = 1 Data 100Mhz	1.407e-03	7.855e-04	5.777e-04	4.741e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	3.944	4.7328
X33_P4	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0785	0.0720	3.3370	1.7460
CP to QN ↑	0.0925	0.0558	6.5434	3.1729
RN to QN ↑	0.0843	0.0848	6.5172	3.1666
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0712	0.0777	0.8981	0.4751
CP to QN ↑	0.0627	0.0683	1.6189	0.8293
RN to QN ↑	0.0868	0.0943	1.6234	0.8320

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1330	0.1258	0.1283	0.1283
CP ↑	min_pulse_width to CP	0.0540	0.0310	0.0396	0.0406
D ↓	hold_rising to CP	-0.0822	-0.0315	-0.0315	-0.0315
D ↑	hold_rising to CP	-0.0331	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1312	0.0856	0.0856	0.0856
D ↑	setup_rising to CP	0.0655	0.0390	0.0390	0.0390
RN ↓	min_pulse_width to RN	0.0774	0.0779	0.0894	0.0920
RN ↑	recovery_rising to CP	0.0244	0.0241	0.0244	0.0244
RN ↑	removal_rising to CP	-0.0175	-0.0126	-0.0126	-0.0126
TE ↓	hold_rising to CP	-0.0522	-0.0259	-0.0259	-0.0259
TE ↑	hold_rising to CP	-0.0454	-0.0289	-0.0264	-0.0264
TE ↓	setup_rising to CP	0.1118	0.0801	0.0801	0.0801
TE ↑	setup_rising to CP	0.2079	0.1612	0.1612	0.1612
TI ↓	hold_rising to CP	-0.1561	-0.0921	-0.0921	-0.0921
TI ↑	hold_rising to CP	-0.0511	-0.0290	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.2158	0.1554	0.1568	0.1568
TI ↑	setup_rising to CP	0.0859	0.0637	0.0635	0.0635

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	6.737e-07	8.163e-12
X8_P4	7.126e-07	7.820e-12
X17_P4	8.788e-07	8.072e-12
X33_P4	1.043e-06	8.576e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	4.283e-03	4.254e-03	4.244e-03	4.238e-03

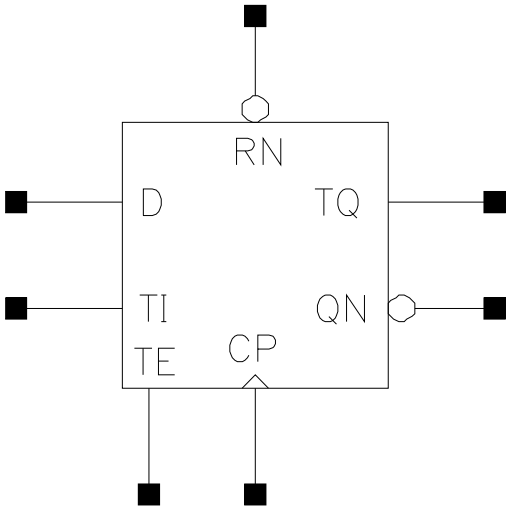
Clock 100Mhz Data 25Mhz	6.436e-03	6.482e-03	7.089e-03	7.695e-03
Clock 100Mhz Data 50Mhz	8.588e-03	8.710e-03	9.935e-03	1.115e-02
Clock = 0 Data 100Mhz	5.059e-03	4.723e-03	4.615e-03	4.562e-03
Clock = 1 Data 100Mhz	1.408e-03	7.494e-04	5.301e-04	4.205e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006

RN	0.0010	0.0007	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0873	0.0747	3.3405	1.8419
CP to QN ↑	0.1208	0.0629	5.8470	3.3032
CP to TQ ↓	0.0862	0.0434	4.4811	3.5483
CP to TQ ↑	0.0720	0.0588	10.1973	9.4285
RN to QN ↑	0.0835	0.0831	5.9102	3.2970
RN to TQ ↓	0.0583	0.0570	3.9434	3.7425
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0770	0.0830	0.9175	0.4877
CP to QN ↑	0.0635	0.0670	1.6560	0.8335
CP to TQ ↓	0.0452	0.0469	4.4488	4.3540
CP to TQ ↑	0.0589	0.0602	8.8491	8.9924
RN to QN ↑	0.0855	0.0909	1.6542	0.8326
RN to TQ ↓	0.0609	0.0636	4.6355	4.5709

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1311	0.1258	0.1282	0.1282
CP ↑	min_pulse_width to CP	0.0782	0.0358	0.0358	0.0396
D ↓	hold_rising to CP	-0.0822	-0.0315	-0.0315	-0.0315
D ↑	hold_rising to CP	-0.0331	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1312	0.0856	0.0856	0.0856
D ↑	setup_rising to CP	0.0655	0.0390	0.0387	0.0387
RN ↓	min_pulse_width to RN	0.0823	0.0823	0.0845	0.0894
RN ↑	recovery_rising to CP	0.0244	0.0244	0.0244	0.0244
RN ↑	removal_rising to CP	-0.0200	-0.0126	-0.0126	-0.0126
TE ↓	hold_rising to CP	-0.0522	-0.0259	-0.0259	-0.0259
TE ↑	hold_rising to CP	-0.0454	-0.0264	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1118	0.0801	0.0801	0.0801
TE ↑	setup_rising to CP	0.2082	0.1612	0.1612	0.1612
TI ↓	hold_rising to CP	-0.1561	-0.0921	-0.0921	-0.0921
TI ↑	hold_rising to CP	-0.0511	-0.0290	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.2158	0.1568	0.1568	0.1568
TI ↑	setup_rising to CP	0.0859	0.0637	0.0635	0.0635

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	7.096e-07	8.324e-12
X8_P4	7.503e-07	7.821e-12
X17_P4	8.666e-07	8.324e-12
X33_P4	1.057e-06	8.828e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

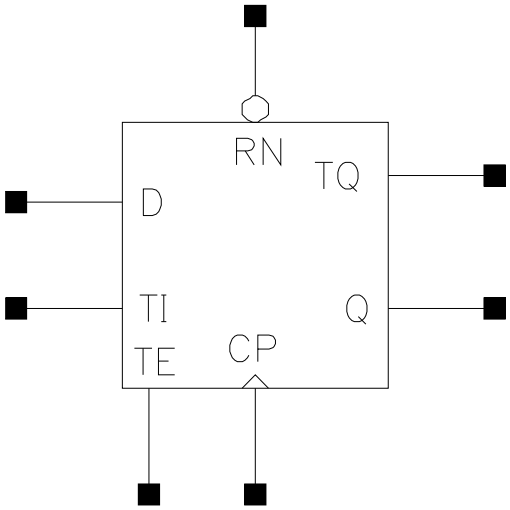
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	4.289e-03	4.288e-03	4.310e-03	4.321e-03
Clock 100Mhz Data 25Mhz	6.648e-03	6.674e-03	7.011e-03	7.768e-03
Clock 100Mhz Data 50Mhz	9.006e-03	9.061e-03	9.712e-03	1.121e-02
Clock = 0 Data 100Mhz	5.033e-03	4.698e-03	4.584e-03	4.527e-03
Clock = 1 Data 100Mhz	1.406e-03	7.596e-04	5.441e-04	4.365e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0006	0.0006	0.0006

RN	0.0008	0.0008	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.1008	0.0513	4.5579	1.9353
CP to Q ↑	0.0737	0.0606	6.9730	3.3939
CP to TQ ↓	0.0980	0.0524	5.6517	4.7355
CP to TQ ↑	0.0762	0.0638	13.8029	12.5346
RN to Q ↓	0.0771	0.0716	3.7815	2.0396
RN to TQ ↓	0.0762	0.0728	4.8213	4.9346
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0706	0.0773	0.9100	0.4838
CP to Q ↑	0.0860	0.0909	1.6107	0.8219
CP to TQ ↓	0.0734	0.0826	4.4811	4.5632
CP to TQ ↑	0.0911	0.0991	12.2790	12.3472
RN to Q ↓	0.0976	0.1044	0.9081	0.4822
RN to TQ ↓	0.1004	0.1097	4.4800	4.5624

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1312	0.1259	0.1258	0.1258
CP ↑	min_pulse_width to CP	0.0868	0.0396	0.0310	0.0310
D ↓	hold_rising to CP	-0.0792	-0.0315	-0.0315	-0.0315
D ↑	hold_rising to CP	-0.0335	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.1315	0.0856	0.0856	0.0856
D ↑	setup_rising to CP	0.0655	0.0390	0.0390	0.0390
RN ↓	min_pulse_width to RN	0.0823	0.0898	0.0779	0.0779
RN ↑	recovery_rising to CP	0.0244	0.0241	0.0244	0.0244
RN ↑	removal_rising to CP	-0.0144	-0.0126	-0.0126	-0.0126
TE ↓	hold_rising to CP	-0.0522	-0.0262	-0.0259	-0.0259
TE ↑	hold_rising to CP	-0.0457	-0.0264	-0.0286	-0.0286
TE ↓	setup_rising to CP	0.1118	0.0801	0.0801	0.0801
TE ↑	setup_rising to CP	0.2082	0.1612	0.1612	0.1612
TI ↓	hold_rising to CP	-0.1561	-0.0921	-0.0921	-0.0921
TI ↑	hold_rising to CP	-0.0496	-0.0290	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.2158	0.1568	0.1568	0.1568
TI ↑	setup_rising to CP	0.0859	0.0637	0.0637	0.0637

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	6.772e-07	8.324e-12
X8_P4	7.153e-07	7.820e-12
X17_P4	8.886e-07	8.324e-12
X33_P4	1.030e-06	8.829e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

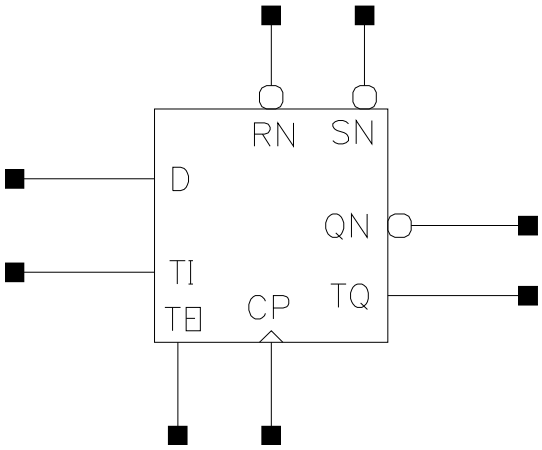
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	4.342e-03	4.380e-03	4.393e-03	4.398e-03
Clock 100Mhz Data 25Mhz	6.643e-03	6.668e-03	7.480e-03	8.171e-03
Clock 100Mhz Data 50Mhz	8.944e-03	8.956e-03	1.057e-02	1.194e-02
Clock = 0 Data 100Mhz	5.035e-03	4.700e-03	4.589e-03	4.533e-03
Clock = 1 Data 100Mhz	1.407e-03	7.233e-04	4.955e-04	3.817e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.352	5.2224
X17_P4	1.200	4.488	5.3856
X33_P4	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0008

SN	0.0012	0.0012	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to QN ↓	0.0827	0.0877	1.7838	0.9248
CP to QN ↑	0.0663	0.0691	3.1911	1.6140
CP to TQ ↓	0.0509	0.0509	5.5866	5.6004
CP to TQ ↑	0.0683	0.0685	16.0605	16.0732
RN to QN ↓	0.0906	0.0956	1.7842	0.9243
RN to QN ↑	0.0932	0.0973	3.1959	1.6183
RN to TQ ↓	0.0716	0.0714	6.0484	6.0485
RN to TQ ↑	0.0767	0.0768	16.0365	16.0502
SN to QN ↓	0.0971	0.1030	1.7930	0.9274
SN to TQ ↑	0.0810	0.0809	16.2091	16.2288
	X33_P4		**X33_P4**	
CP to QN ↓	0.0999		0.4966	
CP to QN ↑	0.0760		0.8278	
CP to TQ ↓	0.0510		5.6055	
CP to TQ ↑	0.0687		16.1102	
RN to QN ↓	0.1076		0.4973	
RN to QN ↑	0.1065		0.8294	
RN to TQ ↓	0.0714		6.0581	
RN to TQ ↑	0.0769		16.0947	
SN to QN ↓	0.1164		0.4969	
SN to TQ ↑	0.0811		16.2953	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1331	0.1331	0.1331
CP ↑	min_pulse_width to CP	0.0406	0.0406	0.0406
D ↓	hold_rising to CP	-0.0315	-0.0315	-0.0315
D ↑	hold_rising to CP	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.0905	0.0905	0.0905
D ↑	setup_rising to CP	0.0414	0.0414	0.0414
RN ↓	min_pulse_width to RN	0.0894	0.0920	0.0969
RN ↑	non_seq_hold_rising to SN	-0.0333	-0.0333	-0.0333
RN ↑	non_seq_setup_rising to SN	0.0760	0.0760	0.0760
RN ↑	recovery_rising to CP	0.0338	0.0338	0.0338
RN ↑	removal_rising to CP	-0.0193	-0.0193	-0.0193
SN ↓	min_pulse_width to SN	0.0762	0.0762	0.0789
SN ↑	recovery_rising to CP	0.0128	0.0128	0.0128
SN ↑	removal_rising to CP	0.0339	0.0339	0.0339

TE ↓	hold_rising to CP	-0.0259	-0.0259	-0.0259
TE ↑	hold_rising to CP	-0.0289	-0.0289	-0.0264
TE ↓	setup_rising to CP	0.0849	0.0849	0.0849
TE ↑	setup_rising to CP	0.1635	0.1635	0.1635
TI ↓	hold_rising to CP	-0.0921	-0.0921	-0.0921
TI ↑	hold_rising to CP	-0.0290	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.1604	0.1604	0.1604
TI ↑	setup_rising to CP	0.0691	0.0691	0.0691

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	8.402e-07	8.855e-12
X17_P4	9.335e-07	9.107e-12
X33_P4	1.095e-06	9.612e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

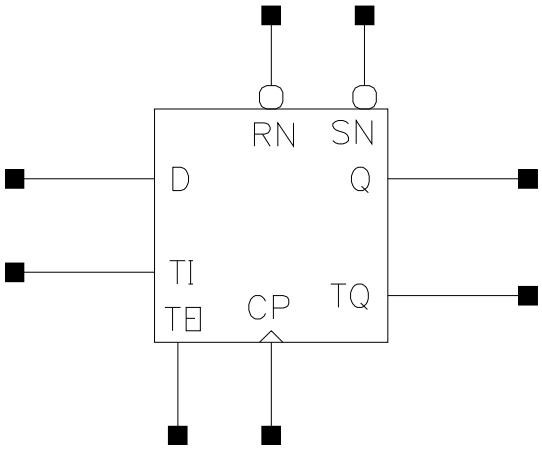
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	4.548e-03	4.549e-03	4.550e-03
Clock 100Mhz Data 25Mhz	7.004e-03	7.292e-03	8.008e-03
Clock 100Mhz Data 50Mhz	9.459e-03	1.004e-02	1.147e-02
Clock = 0 Data 100Mhz	4.583e-03	4.582e-03	4.582e-03
Clock = 1 Data 100Mhz	1.651e-04	1.649e-04	1.649e-04

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P4	1.200	4.216	5.0592
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009
D	0.0005	0.0005	0.0005
RN	0.0008	0.0008	0.0008

SN	0.0012	0.0013	0.0012
TE	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P4	**X17_P4**	**X8_P4**	**X17_P4**
CP to Q ↓	0.0561	0.0626	1.8739	0.9807
CP to Q ↑	0.0664	0.0693	3.2675	1.6618
CP to TQ ↓	0.0585	0.0669	5.6914	5.7694
CP to TQ ↑	0.0732	0.0801	15.8242	15.9357
RN to Q ↓	0.0812	0.0929	2.1416	1.1267
RN to Q ↑	0.0587	0.0650	3.3738	1.7293
RN to TQ ↓	0.0841	0.0981	6.2087	6.3594
RN to TQ ↑	0.0697	0.0823	15.9591	16.0786
SN to Q ↑	0.0801	0.0862	3.3726	1.7266
SN to TQ ↑	0.0911	0.1035	15.9624	16.0869
	X33_P4		**X33_P4**	
CP to Q ↓	0.0789		0.5351	
CP to Q ↑	0.0778		0.8639	
CP to TQ ↓	0.0820		6.0038	
CP to TQ ↑	0.0931		16.1142	
RN to Q ↓	0.1213		0.6276	
RN to Q ↑	0.0814		0.9070	
RN to TQ ↓	0.1230		6.7840	
RN to TQ ↑	0.1061		16.3057	
SN to Q ↑	0.1023		0.9078	
SN to TQ ↑	0.1271		16.3097	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1331	0.1331	0.1331
CP ↑	min_pulse_width to CP	0.0443	0.0491	0.0685
D ↓	hold_rising to CP	-0.0315	-0.0315	-0.0290
D ↑	hold_rising to CP	-0.0068	-0.0068	-0.0068
D ↓	setup_rising to CP	0.0905	0.0905	0.0905
D ↑	setup_rising to CP	0.0414	0.0439	0.0439
RN ↓	min_pulse_width to RN	0.0969	0.1138	0.1458
RN ↑	non_seq_hold_rising to SN	-0.0359	-0.0430	-0.0579
RN ↑	non_seq_setup_rising to SN	0.0739	0.0739	0.0916
RN ↑	recovery_rising to CP	0.0321	0.0321	0.0321
RN ↑	removal_rising to CP	-0.0171	-0.0171	-0.0175
SN ↓	min_pulse_width to SN	0.0767	0.0842	0.1064
SN ↑	recovery_rising to CP	0.0128	0.0128	0.0128
SN ↑	removal_rising to CP	0.0339	0.0339	0.0339

TE ↓	hold_rising to CP	-0.0262	-0.0262	-0.0266
TE ↑	hold_rising to CP	-0.0264	-0.0264	-0.0264
TE ↓	setup_rising to CP	0.0849	0.0849	0.0849
TE ↑	setup_rising to CP	0.1635	0.1635	0.1635
TI ↓	hold_rising to CP	-0.0921	-0.0921	-0.0882
TI ↑	hold_rising to CP	-0.0290	-0.0290	-0.0290
TI ↓	setup_rising to CP	0.1604	0.1604	0.1604
TI ↑	setup_rising to CP	0.0691	0.0691	0.0691

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X8_P4	8.158e-07	8.594e-12
X17_P4	8.989e-07	8.846e-12
X33_P4	1.048e-06	9.350e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

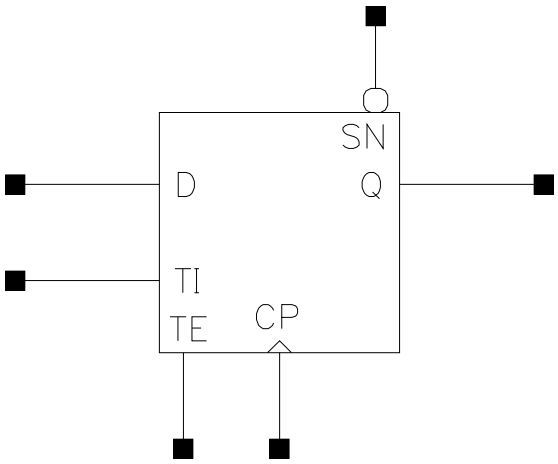
Pin Cycle	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	4.506e-03	4.507e-03	4.508e-03
Clock 100Mhz Data 25Mhz	6.847e-03	7.163e-03	7.945e-03
Clock 100Mhz Data 50Mhz	9.188e-03	9.820e-03	1.138e-02
Clock = 0 Data 100Mhz	4.560e-03	4.561e-03	4.560e-03
Clock = 1 Data 100Mhz	1.217e-04	1.220e-04	1.222e-04

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0014	0.0014	0.0013	0.0013
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0009			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to Q ↓	0.0900	0.0493	4.2932	1.8618
CP to Q ↑	0.0722	0.0612	6.7565	3.2531
SN to Q ↑	0.0566	0.0640	6.6099	3.2563
	X17_P4	X25_P4	X17_P4	X25_P4
CP to Q ↓	0.0680	0.0714	0.8968	0.6258
CP to Q ↑	0.0861	0.0886	1.6044	1.0900
SN to Q ↑	0.0888	0.0914	1.6021	1.0903
	X33_P4		X33_P4	
CP to Q ↓	0.0743		0.4766	
CP to Q ↑	0.0906		0.8201	
SN to Q ↑	0.0933		0.8198	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.1355	0.1331	0.1331	0.1331
CP ↑	min_pulse_width to CP	0.0771	0.0358	0.0310	0.0310
D ↓	hold_rising to CP	-0.0818	-0.0308	-0.0364	-0.0364
D ↑	hold_rising to CP	-0.0308	-0.0038	-0.0038	-0.0038
D ↓	setup_rising to CP	0.1334	0.0905	0.0905	0.0905
D ↑	setup_rising to CP	0.0606	0.0338	0.0342	0.0342
SN ↓	min_pulse_width to SN	0.0518	0.0615	0.0588	0.0588
SN ↑	recovery_rising to CP	0.0124	0.0128	0.0128	0.0128
SN ↑	removal_rising to CP	0.0241	0.0339	0.0308	0.0308
TE ↓	hold_rising to CP	-0.0525	-0.0315	-0.0311	-0.0311
TE ↑	hold_rising to CP	-0.0405	-0.0237	-0.0237	-0.0237
TE ↓	setup_rising to CP	0.1145	0.0880	0.0880	0.0880
TE ↑	setup_rising to CP	0.2075	0.1688	0.1688	0.1688
TI ↓	hold_rising to CP	-0.1561	-0.0969	-0.0964	-0.0964
TI ↑	hold_rising to CP	-0.0463	-0.0241	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.2168	0.1658	0.1658	0.1658
TI ↑	setup_rising to CP	0.0810	0.0553	0.0553	0.0553
		X33_P4			

CP ↓	min_pulse_width to CP	0.1331			
CP ↑	min_pulse_width to CP	0.0310			
D ↓	hold_rising to CP	-0.0364			
D ↑	hold_rising to CP	-0.0038			
D ↓	setup_rising to CP	0.0905			
D ↑	setup_rising to CP	0.0338			
SN ↓	min_pulse_width to SN	0.0588			
SN ↑	recovery_rising to CP	0.0124			
SN ↑	removal_rising to CP	0.0339			
TE ↓	hold_rising to CP	-0.0311			
TE ↑	hold_rising to CP	-0.0237			
TE ↓	setup_rising to CP	0.0880			
TE ↑	setup_rising to CP	0.1688			
TI ↓	hold_rising to CP	-0.0964			
TI ↑	hold_rising to CP	-0.0241			
TI ↓	setup_rising to CP	0.1658			
TI ↑	setup_rising to CP	0.0553			

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	6.812e-07	8.072e-12
X8_P4	7.298e-07	7.818e-12
X17_P4	8.985e-07	8.322e-12
X25_P4	9.808e-07	8.574e-12
X33_P4	1.062e-06	8.826e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	4.217e-03	4.259e-03	4.273e-03	4.280e-03
Clock 100Mhz Data 25Mhz	6.371e-03	6.485e-03	7.233e-03	7.587e-03
Clock 100Mhz Data 50Mhz	8.525e-03	8.711e-03	1.019e-02	1.089e-02
Clock = 0 Data 100Mhz	4.912e-03	4.665e-03	4.583e-03	4.542e-03
Clock = 1 Data 100Mhz	1.407e-03	7.518e-04	5.335e-04	4.244e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	4.284e-03			

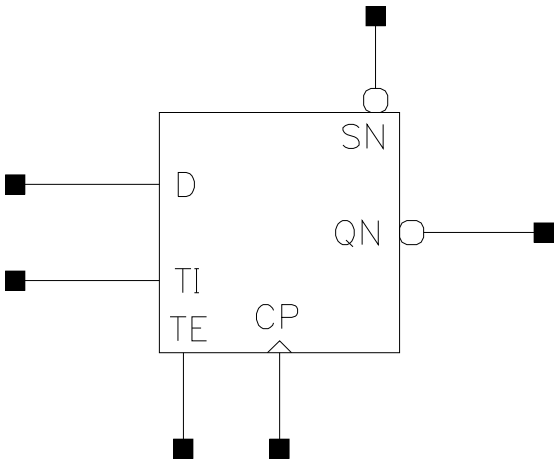
Clock 100Mhz Data 25Mhz	7.886e-03			
Clock 100Mhz Data 50Mhz	1.149e-02			
Clock = 0 Data 100Mhz	4.518e-03			
Clock = 1 Data 100Mhz	3.590e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	3.944	4.7328
X8_P4	1.200	3.808	4.5696
X17_P4	1.200	4.080	4.8960
X25_P4	1.200	4.216	5.0592
X33_P4	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X25_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0014	0.0014	0.0014	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P4			

CP	0.0009			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
CP to QN ↓	0.0818	0.0730	3.3360	1.7484
CP to QN ↑	0.0934	0.0558	6.5381	3.1839
SN to QN ↓	0.0675	0.0756	3.3286	1.7479
	X17_P4	X25_P4	X17_P4	X25_P4
CP to QN ↓	0.0761	0.0801	0.9021	0.6279
CP to QN ↑	0.0670	0.0705	1.6054	1.0911
SN to QN ↓	0.0800	0.0841	0.9016	0.6278
	X33_P4		X33_P4	
CP to QN ↓	0.0834		0.4786	
CP to QN ↑	0.0729		0.8200	
SN to QN ↓	0.0873		0.4786	

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X25_P4
CP ↓	min_pulse_width to CP	0.1355	0.1331	0.1331	0.1331
CP ↑	min_pulse_width to CP	0.0577	0.0310	0.0395	0.0406
D ↓	hold_rising to CP	-0.0818	-0.0364	-0.0308	-0.0308
D ↑	hold_rising to CP	-0.0308	-0.0038	-0.0038	-0.0038
D ↓	setup_rising to CP	0.1334	0.0905	0.0905	0.0905
D ↑	setup_rising to CP	0.0606	0.0342	0.0338	0.0342
SN ↓	min_pulse_width to SN	0.0518	0.0588	0.0615	0.0615
SN ↑	recovery_rising to CP	0.0124	0.0124	0.0124	0.0124
SN ↑	removal_rising to CP	0.0241	0.0339	0.0339	0.0339
TE ↓	hold_rising to CP	-0.0525	-0.0311	-0.0315	-0.0315
TE ↑	hold_rising to CP	-0.0405	-0.0237	-0.0237	-0.0237
TE ↓	setup_rising to CP	0.1145	0.0880	0.0880	0.0880
TE ↑	setup_rising to CP	0.2075	0.1688	0.1688	0.1688
TI ↓	hold_rising to CP	-0.1576	-0.0964	-0.0969	-0.0969
TI ↑	hold_rising to CP	-0.0463	-0.0241	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.2168	0.1658	0.1658	0.1658
TI ↑	setup_rising to CP	0.0810	0.0553	0.0553	0.0553
		X33_P4			

CP ↓	min_pulse_width to CP	0.1331			
CP ↑	min_pulse_width to CP	0.0406			
D ↓	hold_rising to CP	-0.0308			
D ↑	hold_rising to CP	-0.0038			
D ↓	setup_rising to CP	0.0905			
D ↑	setup_rising to CP	0.0338			
SN ↓	min_pulse_width to SN	0.0642			
SN ↑	recovery_rising to CP	0.0124			
SN ↑	removal_rising to CP	0.0339			
TE ↓	hold_rising to CP	-0.0315			
TE ↑	hold_rising to CP	-0.0237			
TE ↓	setup_rising to CP	0.0880			
TE ↑	setup_rising to CP	0.1688			
TI ↓	hold_rising to CP	-0.0969			
TI ↑	hold_rising to CP	-0.0241			
TI ↓	setup_rising to CP	0.1658			
TI ↑	setup_rising to CP	0.0553			

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	6.653e-07	8.072e-12
X8_P4	7.043e-07	7.818e-12
X17_P4	8.800e-07	8.322e-12
X25_P4	9.499e-07	8.574e-12
X33_P4	1.021e-06	8.826e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

Pin Cycle	X4_P4	X8_P4	X17_P4	X25_P4
Clock 100Mhz Data 0Mhz	4.193e-03	4.235e-03	4.244e-03	4.248e-03
Clock 100Mhz Data 25Mhz	6.308e-03	6.457e-03	7.193e-03	7.541e-03
Clock 100Mhz Data 50Mhz	8.422e-03	8.680e-03	1.014e-02	1.083e-02
Clock = 0 Data 100Mhz	4.910e-03	4.668e-03	4.586e-03	4.544e-03
Clock = 1 Data 100Mhz	1.409e-03	7.574e-04	5.401e-04	4.316e-04
	X33_P4			
Clock 100Mhz Data 0Mhz	4.251e-03			

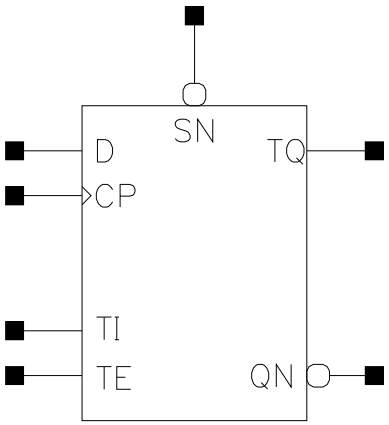
Clock 100Mhz Data 25Mhz	7.821e-03			
Clock 100Mhz Data 50Mhz	1.139e-02			
Clock = 0 Data 100Mhz	4.519e-03			
Clock = 1 Data 100Mhz	3.666e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.216	5.0592
X8_P4	1.200	4.080	4.8960
X17_P4	1.200	4.352	5.2224
X33_P4	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0016	0.0015	0.0015
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to QN ↓	0.0936	0.0764	3.3276	1.7579
CP to QN ↑	0.1217	0.0633	6.4408	3.2563
CP to TQ ↓	0.0874	0.0443	5.0840	4.1259
CP to TQ ↑	0.0722	0.0580	9.0143	8.8004
SN to QN ↓	0.0638	0.0607	3.3265	1.7580
SN to TQ ↑	0.0451	0.0438	8.8803	8.7792
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to QN ↓	0.0761	0.0837	0.9258	0.4725
CP to QN ↑	0.0722	0.0788	1.6191	0.8261
CP to TQ ↓	0.0550	0.0548	4.3204	4.3243
CP to TQ ↑	0.0645	0.0646	8.8524	8.8773
SN to QN ↓	0.0666	0.0740	0.9264	0.4721
SN to TQ ↑	0.0546	0.0545	8.8489	8.8819

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1354	0.1331	0.1331	0.1331
CP ↑	min_pulse_width to CP	0.0820	0.0358	0.0443	0.0455
D ↓	hold_rising to CP	-0.0818	-0.0364	-0.0308	-0.0308
D ↑	hold_rising to CP	-0.0308	-0.0038	-0.0038	-0.0038
D ↓	setup_rising to CP	0.1364	0.0905	0.0905	0.0905
D ↑	setup_rising to CP	0.0606	0.0342	0.0342	0.0342
SN ↓	min_pulse_width to SN	0.0469	0.0491	0.0518	0.0518
SN ↑	recovery_rising to CP	0.0124	0.0128	0.0128	0.0128
SN ↑	removal_rising to CP	0.0241	0.0308	0.0339	0.0339
TE ↓	hold_rising to CP	-0.0525	-0.0311	-0.0315	-0.0315
TE ↑	hold_rising to CP	-0.0405	-0.0237	-0.0237	-0.0237
TE ↓	setup_rising to CP	0.1145	0.0880	0.0880	0.0880
TE ↑	setup_rising to CP	0.2075	0.1688	0.1688	0.1688
TI ↓	hold_rising to CP	-0.1561	-0.0964	-0.0969	-0.0969
TI ↑	hold_rising to CP	-0.0463	-0.0241	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.2168	0.1658	0.1658	0.1658
TI ↑	setup_rising to CP	0.0810	0.0553	0.0553	0.0553

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	7.303e-07	8.575e-12
X8_P4	7.686e-07	8.324e-12
X17_P4	9.444e-07	8.828e-12
X33_P4	1.085e-06	9.332e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

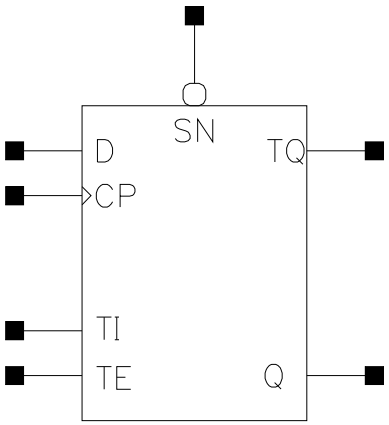
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	4.201e-03	4.292e-03	4.323e-03	4.339e-03
Clock 100Mhz Data 25Mhz	6.603e-03	6.734e-03	7.393e-03	8.046e-03
Clock 100Mhz Data 50Mhz	9.005e-03	9.176e-03	1.046e-02	1.175e-02
Clock = 0 Data 100Mhz	4.912e-03	4.664e-03	4.581e-03	4.539e-03
Clock = 1 Data 100Mhz	1.406e-03	7.266e-04	5.002e-04	3.871e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	4.080	4.8960
X8_P4	1.200	3.944	4.7328
X17_P4	1.200	4.216	5.0592
X33_P4	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X33_P4
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0013	0.0014	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
CP to Q ↓	0.1030	0.0529	4.4276	1.9090
CP to Q ↑	0.0767	0.0633	6.8049	3.2915
CP to TQ ↓	0.1029	0.0560	6.3539	4.7508
CP to TQ ↑	0.0758	0.0698	9.0751	12.6413
SN to Q ↑	0.0478	0.0666	6.6371	3.2967
SN to TQ ↑	0.0470	0.0740	8.9040	12.6288
	X17_P4	**X33_P4**	**X17_P4**	**X33_P4**
CP to Q ↓	0.0694	0.0759	0.9249	0.4864
CP to Q ↑	0.0872	0.0917	1.6120	0.8237
CP to TQ ↓	0.0722	0.0813	4.4796	4.5560
CP to TQ ↑	0.0924	0.0998	12.2877	12.3572
SN to Q ↑	0.0898	0.0943	1.6126	0.8233
SN to TQ ↑	0.0951	0.1024	12.2909	12.3602

Timing Constraints (ns) at 25C, 1.00V, Typ process

Pin	Constraint	X4_P4	X8_P4	X17_P4	X33_P4
CP ↓	min_pulse_width to CP	0.1355	0.1331	0.1331	0.1331
CP ↑	min_pulse_width to CP	0.0879	0.0396	0.0310	0.0310
D ↓	hold_rising to CP	-0.0818	-0.0308	-0.0364	-0.0364
D ↑	hold_rising to CP	-0.0308	-0.0038	-0.0038	-0.0038
D ↓	setup_rising to CP	0.1364	0.0905	0.0905	0.0905
D ↑	setup_rising to CP	0.0606	0.0338	0.0338	0.0342
SN ↓	min_pulse_width to SN	0.0469	0.0642	0.0588	0.0588
SN ↑	recovery_rising to CP	0.0124	0.0128	0.0128	0.0128
SN ↑	removal_rising to CP	0.0241	0.0339	0.0339	0.0308
TE ↓	hold_rising to CP	-0.0525	-0.0315	-0.0311	-0.0311
TE ↑	hold_rising to CP	-0.0405	-0.0237	-0.0237	-0.0237
TE ↓	setup_rising to CP	0.1145	0.0880	0.0880	0.0880
TE ↑	setup_rising to CP	0.2075	0.1688	0.1688	0.1688
TI ↓	hold_rising to CP	-0.1561	-0.0969	-0.0964	-0.0964
TI ↑	hold_rising to CP	-0.0463	-0.0241	-0.0241	-0.0241
TI ↓	setup_rising to CP	0.2168	0.1658	0.1658	0.1658
TI ↑	setup_rising to CP	0.0810	0.0553	0.0553	0.0553

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	7.253e-07	8.324e-12
X8_P4	7.655e-07	8.070e-12
X17_P4	9.341e-07	8.574e-12
X33_P4	1.098e-06	9.078e-12

Internal Energy (uW/MHz) at 25C, 1.00V, Typ process

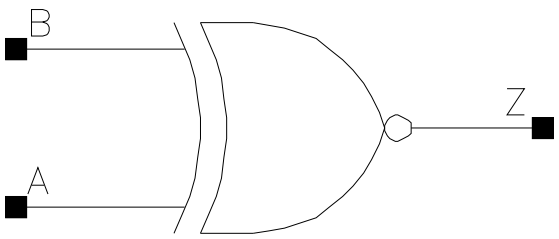
Pin Cycle	X4_P4	X8_P4	X17_P4	X33_P4
Clock 100Mhz Data 0Mhz	4.201e-03	4.306e-03	4.341e-03	4.358e-03
Clock 100Mhz Data 25Mhz	6.523e-03	6.691e-03	7.468e-03	8.162e-03
Clock 100Mhz Data 50Mhz	8.845e-03	9.076e-03	1.060e-02	1.197e-02
Clock = 0 Data 100Mhz	4.910e-03	4.657e-03	4.573e-03	4.531e-03
Clock = 1 Data 100Mhz	1.408e-03	7.277e-04	5.008e-04	3.875e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.360	1.6320
X17_P4	1.200	1.496	1.7952
X25_P4	1.200	2.312	2.7744
X33_P4	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P4	X8_P4	X17_P4	X25_P4
A	0.0016	0.0007	0.0009	0.0014
B	0.0015	0.0014	0.0018	0.0024
	X33_P4			
A	0.0016			
B	0.0027			

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P4	**X8_P4**	**X6_P4**	**X8_P4**
A to Z ↓	0.0233	0.0535	3.3168	1.9061
A to Z ↑	0.0256	0.0461	5.3152	3.3582
B to Z ↓	0.0221	0.0374	3.3169	1.8951
B to Z ↑	0.0251	0.0342	5.3283	3.3508
	X17_P4	**X25_P4**	**X17_P4**	**X25_P4**
A to Z ↓	0.0509	0.0509	0.9425	0.6507
A to Z ↑	0.0424	0.0429	1.6470	1.0966

B to Z ↓	0.0389	0.0378	0.9403	0.6496
B to Z ↑	0.0342	0.0332	1.6444	1.0939
	X33_P4		**X33_P4**	
A to Z ↓	0.0482		0.4881	
A to Z ↑	0.0415		0.8243	
B to Z ↓	0.0364		0.4869	
B to Z ↑	0.0329		0.8222	

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X6_P4	2.783e-07	2.528e-12
X8_P4	3.666e-07	3.282e-12
X17_P4	5.395e-07	3.535e-12
X25_P4	8.650e-07	5.046e-12
X33_P4	1.089e-06	5.297e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	2.679e-03	4.805e-03	6.700e-03	1.073e-02
B to Z	2.473e-03	3.283e-03	4.968e-03	7.782e-03
	X33_P4			
A to Z	1.302e-02			
B to Z	9.726e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

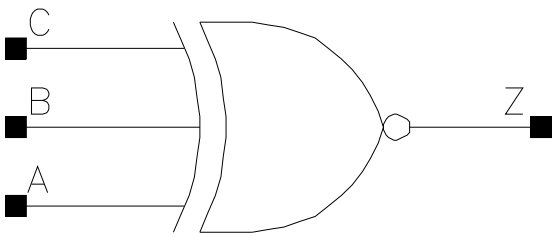
Pin Cycle (vdds)	X6_P4	X8_P4	X17_P4	X25_P4
A to Z	-1.482e-05	-1.824e-07	-4.431e-07	-6.332e-07
B to Z	1.229e-05	6.100e-09	1.218e-07	6.830e-08
	X33_P4			
A to Z	-6.897e-07			
B to Z	-3.198e-07			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	2.176	2.6112
X16_P4	1.200	2.720	3.2640
X25_P4	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X16_P4	X25_P4
A	0.0027	0.0023	0.0028	0.0041
B	0.0030	0.0021	0.0028	0.0038
C	0.0019	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0374	0.0626	3.9653	2.0328
A to Z ↑	0.0363	0.0561	7.8559	3.3252
B to Z ↓	0.0379	0.0622	3.9654	2.0315
B to Z ↑	0.0361	0.0560	7.8490	3.3267
C to Z ↓	0.0368	0.0804	3.9667	2.0304
C to Z ↑	0.0345	0.0730	7.8256	3.3239
	X16_P4	**X25_P4**	**X16_P4**	**X25_P4**
A to Z ↓	0.0627	0.0630	1.0433	0.6694
A to Z ↑	0.0606	0.0605	1.7423	1.1004
B to Z ↓	0.0625	0.0636	1.0422	0.6689

B to Z ↑	0.0606	0.0616	1.7430	1.1006
C to Z ↓	0.0844	0.0899	1.0422	0.6686
C to Z ↑	0.0811	0.0869	1.7432	1.1006

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	3.959e-07	4.544e-12
X8_P4	4.060e-07	4.797e-12
X16_P4	6.241e-07	5.805e-12
X25_P4	8.875e-07	8.073e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	3.011e-03	3.804e-03	6.092e-03	9.203e-03
B to Z	2.755e-03	3.701e-03	5.938e-03	9.035e-03
C to Z	2.652e-03	5.689e-03	8.377e-03	1.266e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

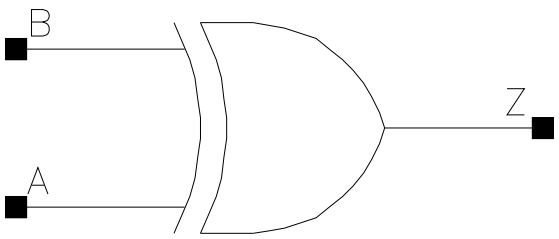
Pin Cycle (vdds)	X4_P4	X8_P4	X16_P4	X25_P4
A to Z	-4.537e-05	-1.501e-05	-2.396e-05	-3.665e-05
B to Z	2.210e-06	-8.795e-06	-5.572e-06	-5.859e-06
C to Z	1.386e-05	6.594e-06	6.291e-06	5.880e-06

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	1.224	1.4688
X6_P4	1.200	0.952	1.1424
X8_P4	1.200	1.224	1.4688
X16_P4	1.200	1.360	1.6320
X25_P4	1.200	2.176	2.6112
X31_P4	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P4	X6_P4	X8_P4	X16_P4
A	0.0007	0.0015	0.0010	0.0011
B	0.0012	0.0014	0.0014	0.0016
	X25_P4	X31_P4		
A	0.0014	0.0018		
B	0.0024	0.0032		

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X6_P4**	**X4_P4**	**X6_P4**
A to Z ↓	0.0480	0.0248	3.3958	2.5435
A to Z ↑	0.0434	0.0259	6.3783	6.9534
B to Z ↓	0.0346	0.0243	3.3843	2.5639
B to Z ↑	0.0338	0.0245	6.3681	6.9491
	X8_P4	**X16_P4**	**X8_P4**	**X16_P4**
A to Z ↓	0.0431	0.0449	1.8563	0.9632

A to Z ↑	0.0376	0.0394	3.2695	1.6478
B to Z ↓	0.0336	0.0347	1.8532	0.9616
B to Z ↑	0.0311	0.0326	3.2693	1.6476
	X25_P4	**X31_P4**	**X25_P4**	**X31_P4**
A to Z ↓	0.0480	0.0450	0.6463	0.5182
A to Z ↑	0.0420	0.0399	1.0947	0.8818
B to Z ↓	0.0370	0.0346	0.6459	0.5176
B to Z ↑	0.0326	0.0311	1.0944	0.8820

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	3.087e-07	3.031e-12
X6_P4	2.917e-07	2.536e-12
X8_P4	4.324e-07	3.030e-12
X16_P4	5.880e-07	3.283e-12
X25_P4	8.488e-07	4.796e-12
X31_P4	1.068e-06	5.051e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	3.690e-03	2.654e-03	4.383e-03	6.212e-03
B to Z	2.796e-03	2.391e-03	3.555e-03	5.089e-03
	X25_P4	X31_P4		
A to Z	9.765e-03	1.191e-02		
B to Z	6.829e-03	8.274e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

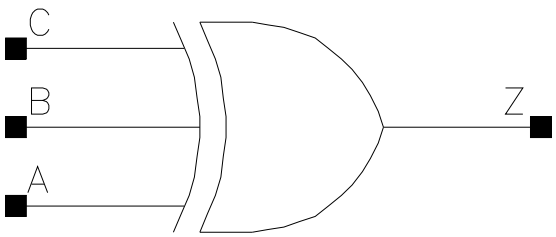
Pin Cycle (vdds)	X4_P4	X6_P4	X8_P4	X16_P4
A to Z	-5.519e-08	-2.120e-05	-1.076e-07	-1.862e-07
B to Z	-9.800e-08	9.085e-06	-5.125e-08	1.570e-08
	X25_P4	X31_P4		
A to Z	-5.475e-07	-4.833e-07		
B to Z	-3.030e-08	6.652e-07		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.200	2.040	2.4480
X8_P4	1.200	1.904	2.2848
X17_P4	1.200	2.040	2.4480
X24_P4	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P4	X8_P4	X17_P4	X24_P4
A	0.0023	0.0023	0.0028	0.0050
B	0.0023	0.0021	0.0026	0.0042
C	0.0007	0.0016	0.0021	0.0033

Propagation Delay at 25C, 1.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0381	0.0625	4.1816	2.0318
A to Z ↑	0.0365	0.0560	8.5743	3.3223
B to Z ↓	0.0382	0.0623	4.1824	2.0311
B to Z ↑	0.0363	0.0560	8.5672	3.3234
C to Z ↓	0.0622	0.0605	4.1534	2.0301
C to Z ↑	0.0607	0.0538	8.5455	3.3239
	X17_P4	**X24_P4**	**X17_P4**	**X24_P4**
A to Z ↓	0.0574	0.0664	0.9687	0.7009
A to Z ↑	0.0555	0.0502	1.6208	1.1032
B to Z ↓	0.0571	0.0664	0.9681	0.6999

B to Z ↑	0.0554	0.0501	1.6219	1.1036
C to Z ↓	0.0560	0.0638	0.9681	0.6993
C to Z ↑	0.0542	0.0491	1.6215	1.1036

Average Leakage Power (mW) at 25C, 1.00V, Typ process

	vdd	vdds
X4_P4	4.375e-07	4.544e-12
X8_P4	3.479e-07	4.292e-12
X17_P4	5.607e-07	4.544e-12
X24_P4	9.678e-07	7.822e-12

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdd)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	2.724e-03	3.834e-03	5.905e-03	1.006e-02
B to Z	2.620e-03	3.683e-03	5.657e-03	9.690e-03
C to Z	5.370e-03	3.543e-03	5.570e-03	9.304e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V, Typ process

Pin Cycle (vdds)	X4_P4	X8_P4	X17_P4	X24_P4
A to Z	-2.403e-05	-1.925e-05	-3.298e-05	-6.376e-05
B to Z	-9.806e-06	-2.638e-06	3.150e-07	-1.929e-05
C to Z	8.590e-06	4.638e-06	1.070e-05	3.362e-05

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