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C28SOI_SC_8_COREPBP16_LL Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 16 nm

Overview

- C28SOI_SC_8_COREPBP16_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

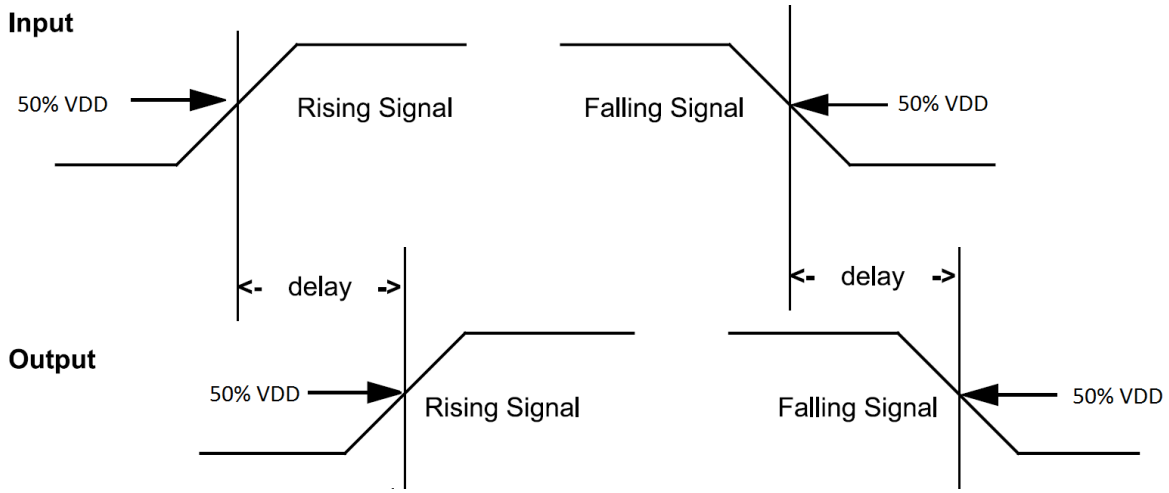


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

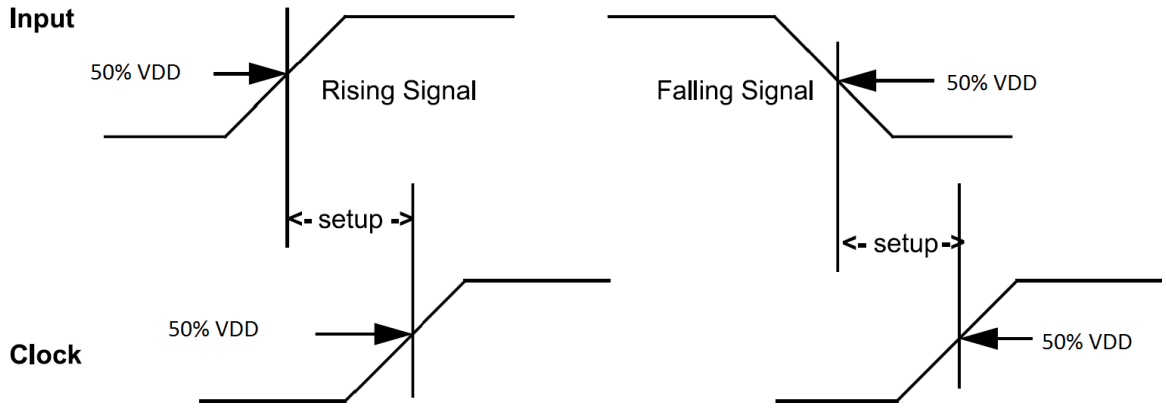


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

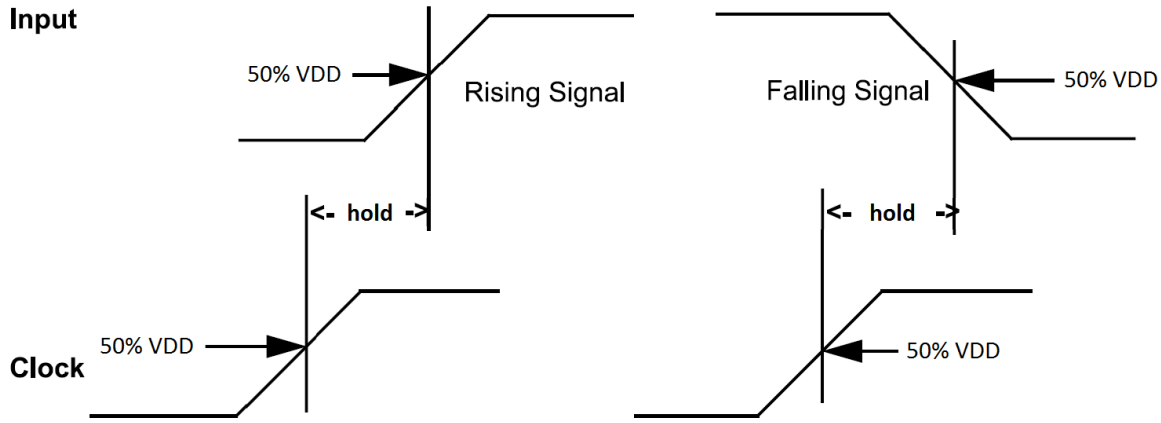


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

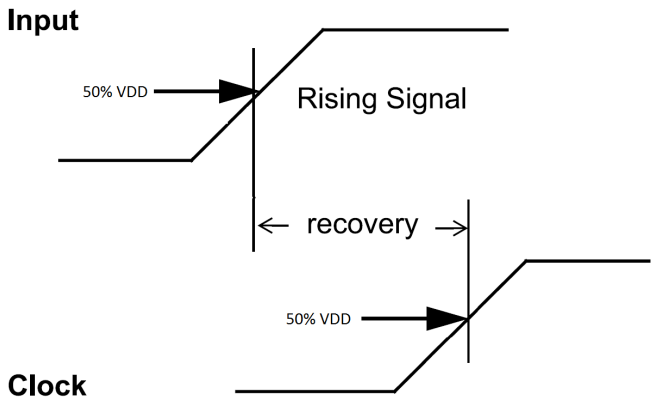


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

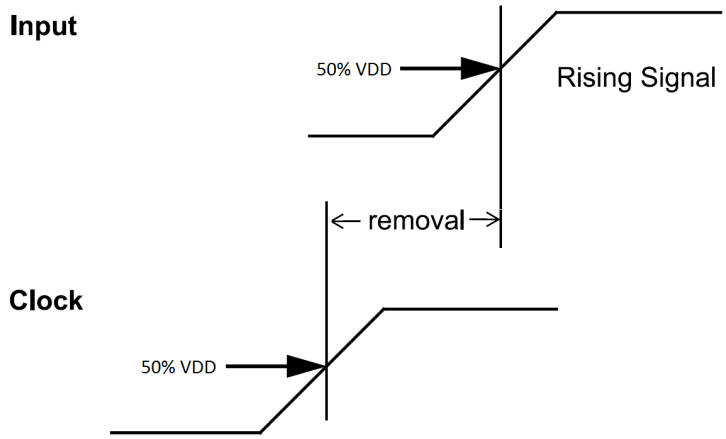


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

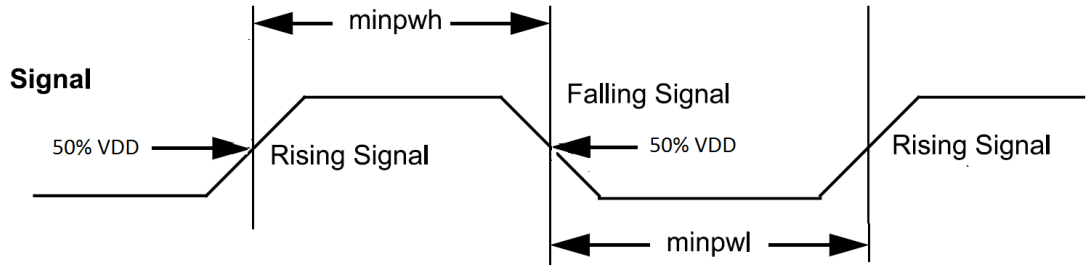


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

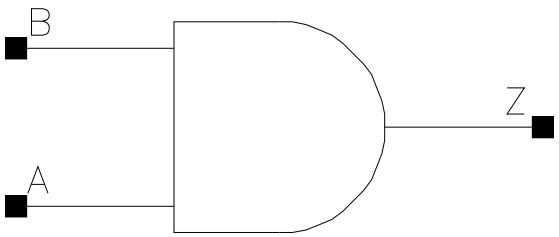
The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description	Logical Symbol
2 input AND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.544	0.4352
X10_P16	0.800	0.680	0.5440
X11_P16	1.600	0.544	0.8704
X19_P16	0.800	1.224	0.9792
X24_P16	0.800	1.360	1.0880
X29_P16	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X11_P16	X19_P16
A	0.0005	0.0008	0.0010	0.0015
B	0.0005	0.0007	0.0010	0.0014
	X24_P16	X29_P16		
A	0.0015	0.0015		
B	0.0014	0.0014		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0360	0.0295	3.4734	1.6633
A to Z ↑	0.0281	0.0262	5.3807	2.5840
B to Z ↓	0.0344	0.0276	3.4800	1.6611
B to Z ↑	0.0299	0.0276	5.3890	2.5837
	X11_P16	**X19_P16**	**X11_P16**	**X19_P16**

A to Z ↓	0.0319	0.0288	1.3161	0.8582
A to Z ↑	0.0246	0.0257	2.4834	1.3019
B to Z ↓	0.0296	0.0275	1.3142	0.8589
B to Z ↑	0.0261	0.0273	2.4811	1.3022
	X24_P16	**X29_P16**	**X24_P16**	**X29_P16**
A to Z ↓	0.0312	0.0329	0.6988	0.5824
A to Z ↑	0.0281	0.0298	1.0445	0.8682
B to Z ↓	0.0301	0.0319	0.6996	0.5838
B to Z ↑	0.0299	0.0318	1.0441	0.8674

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.092e-07	1.000e-20
X10_P16	2.293e-07	1.000e-20
X11_P16	2.721e-07	1.000e-20
X19_P16	4.423e-07	1.000e-20
X24_P16	5.099e-07	1.000e-20
X29_P16	5.776e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X11_P16	X19_P16
A (output stable)	6.598e-06	1.288e-05	1.674e-05	2.344e-05
B (output stable)	2.546e-05	4.718e-05	6.727e-05	9.817e-05
A to Z	1.586e-03	2.621e-03	3.206e-03	5.121e-03
B to Z	1.491e-03	2.459e-03	2.961e-03	4.778e-03
	X24_P16	X29_P16		
A (output stable)	2.371e-05	2.377e-05		
B (output stable)	9.906e-05	9.925e-05		
A to Z	6.223e-03	7.057e-03		
B to Z	5.884e-03	6.728e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

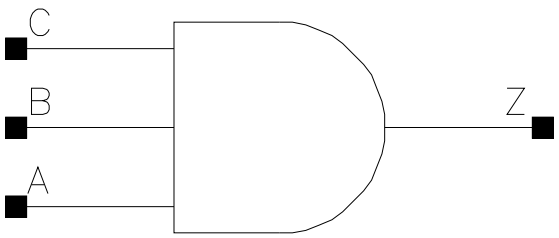
Pin Cycle (vdds)	X5_P16	X10_P16	X11_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P16	X29_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.680	0.5440
X10_P16	0.800	0.816	0.6528
X14_P16	0.800	1.360	1.0880
X19_P16	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0005	0.0008	0.0013	0.0016
B	0.0005	0.0007	0.0011	0.0014
C	0.0005	0.0008	0.0010	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0404	0.0329	3.5197	1.6754
A to Z ↑	0.0378	0.0346	5.4535	2.6147
B to Z ↓	0.0394	0.0313	3.5231	1.6736
B to Z ↑	0.0387	0.0350	5.4524	2.6185
C to Z ↓	0.0377	0.0297	3.5158	1.6719
C to Z ↑	0.0399	0.0357	5.4526	2.6166
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0332	0.0315	1.1610	0.8610

A to Z ↑	0.0335	0.0326	1.7801	1.3165
B to Z ↓	0.0317	0.0299	1.1607	0.8597
B to Z ↑	0.0341	0.0333	1.7817	1.3166
C to Z ↓	0.0301	0.0282	1.1601	0.8606
C to Z ↑	0.0350	0.0339	1.7820	1.3156

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.116e-07	1.000e-20
X10_P16	2.351e-07	1.000e-20
X14_P16	3.373e-07	1.000e-20
X19_P16	4.600e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	4.799e-06	9.458e-06	1.163e-05	1.517e-05
B (output stable)	2.301e-05	4.401e-05	6.016e-05	8.624e-05
C (output stable)	1.815e-05	3.315e-05	4.653e-05	6.575e-05
A to Z	1.847e-03	3.050e-03	4.457e-03	5.799e-03
B to Z	1.755e-03	2.881e-03	4.203e-03	5.457e-03
C to Z	1.671e-03	2.715e-03	3.964e-03	5.107e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

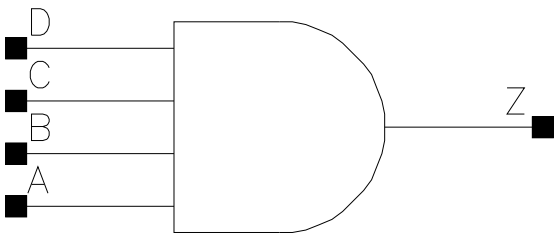
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.088	0.8704
X3_P16	0.800	1.088	0.8704
X10_P16	0.800	2.176	1.7408
X13_P16	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P16	X3_P16	X10_P16	X13_P16
A	0.0005	0.0006	0.0012	0.0013
B	0.0005	0.0005	0.0012	0.0014
C	0.0005	0.0005	0.0011	0.0014
D	0.0006	0.0005	0.0011	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	X3_P16	X2_P16	X3_P16
A to Z ↓	0.0320	0.0342	6.3280	4.2152
A to Z ↑	0.0327	0.0326	19.8117	10.3796
B to Z ↓	0.0299	0.0329	6.3261	4.2172
B to Z ↑	0.0341	0.0343	19.8316	10.3833
C to Z ↓	0.0324	0.0349	6.3348	4.2367
C to Z ↑	0.0317	0.0315	19.8465	10.4049

D to Z ↓	0.0307	0.0340	6.3277	4.2345
D to Z ↑	0.0336	0.0344	19.8767	10.4020
	X10_P16	**X13_P16**	**X10_P16**	**X13_P16**
A to Z ↓	0.0324	0.0323	1.4583	1.0839
A to Z ↑	0.0316	0.0341	3.4450	2.6466
B to Z ↓	0.0310	0.0296	1.4590	1.0832
B to Z ↑	0.0331	0.0345	3.4481	2.6467
C to Z ↓	0.0322	0.0306	1.4496	1.0889
C to Z ↑	0.0297	0.0289	3.4492	2.6452
D to Z ↓	0.0293	0.0280	1.4477	1.0863
D to Z ↑	0.0299	0.0292	3.4496	2.6453

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P16	1.215e-07	1.000e-20
X3_P16	1.517e-07	1.000e-20
X10_P16	4.388e-07	1.000e-20
X13_P16	5.900e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P16	X3_P16	X10_P16	X13_P16
A (output stable)	3.533e-04	4.282e-04	1.136e-03	1.560e-03
B (output stable)	3.214e-04	3.951e-04	1.043e-03	1.367e-03
C (output stable)	3.496e-04	3.923e-04	1.052e-03	1.320e-03
D (output stable)	3.172e-04	3.668e-04	9.163e-04	1.127e-03
A to Z	1.312e-03	1.747e-03	4.936e-03	6.675e-03
B to Z	1.220e-03	1.650e-03	4.685e-03	6.151e-03
C to Z	1.305e-03	1.656e-03	4.223e-03	5.238e-03
D to Z	1.216e-03	1.591e-03	3.784e-03	4.717e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

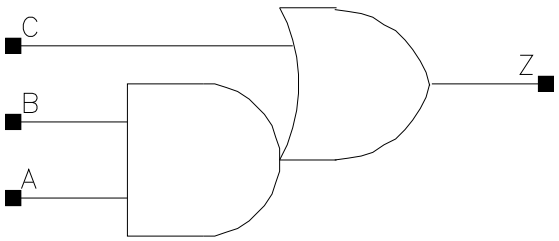
Pin Cycle (vdds)	X2_P16	X3_P16	X10_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	0.952	0.7616
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0004	0.0006	0.0013
B	0.0005	0.0007	0.0012
C	0.0005	0.0007	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0489	0.0429	3.3628	1.6815
A to Z ↑	0.0312	0.0284	5.0136	2.5520
B to Z ↓	0.0459	0.0401	3.3536	1.6765
B to Z ↑	0.0335	0.0306	5.0140	2.5516
C to Z ↓	0.0498	0.0420	3.3432	1.6720
C to Z ↑	0.0292	0.0267	4.9735	2.5316
	X19_P16		**X19_P16**	
A to Z ↓	0.0415		0.8796	
A to Z ↑	0.0310		1.2878	

B to Z ↓	0.0398		0.8802	
B to Z ↑	0.0332		1.2879	
C to Z ↓	0.0412		0.8767	
C to Z ↑	0.0285		1.2747	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.296e-07	1.000e-20
X10_P16	2.490e-07	1.000e-20
X19_P16	4.426e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	2.854e-06	6.322e-06	1.076e-05
B (output stable)	1.143e-05	2.229e-05	4.245e-05
C (output stable)	4.733e-05	5.875e-05	1.410e-04
A to Z	1.779e-03	2.895e-03	5.546e-03
B to Z	1.692e-03	2.739e-03	5.300e-03
C to Z	2.021e-03	3.193e-03	6.162e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

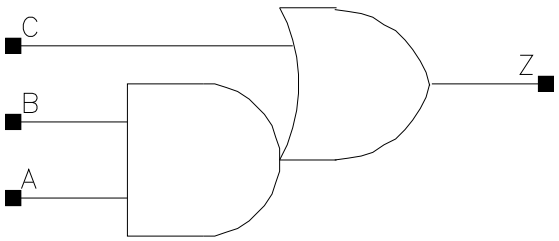
Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	0.952	0.7616
X14_P16	0.800	1.632	1.3056
X19_P16	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0004	0.0007	0.0014	0.0014
B	0.0005	0.0007	0.0014	0.0014
C	0.0005	0.0007	0.0014	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0515	0.0450	3.3483	1.6943
A to Z ↑	0.0338	0.0314	5.1158	2.5716
B to Z ↓	0.0492	0.0428	3.3365	1.6941
B to Z ↑	0.0367	0.0336	5.1134	2.5732
C to Z ↓	0.0442	0.0397	3.3241	1.6867
C to Z ↑	0.0257	0.0235	5.0531	2.5446
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0409	0.0437	1.1581	0.8706

A to Z ↑	0.0291	0.0308	1.7522	1.3053
B to Z ↓	0.0371	0.0401	1.1542	0.8678
B to Z ↑	0.0301	0.0320	1.7513	1.3055
C to Z ↓	0.0333	0.0364	1.1515	0.8654
C to Z ↑	0.0208	0.0222	1.7325	1.2892

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.315e-07	1.000e-20
X10_P16	2.377e-07	1.000e-20
X14_P16	4.422e-07	1.000e-20
X19_P16	4.986e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	1.272e-05	1.650e-05	5.339e-05	5.319e-05
B (output stable)	7.072e-05	7.544e-05	2.754e-04	2.750e-04
C (output stable)	3.477e-05	4.720e-05	9.926e-05	9.960e-05
A to Z	2.013e-03	3.096e-03	5.573e-03	6.451e-03
B to Z	1.933e-03	2.941e-03	5.056e-03	5.938e-03
C to Z	1.657e-03	2.585e-03	4.210e-03	5.090e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

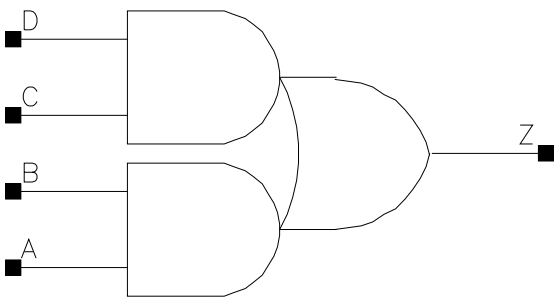
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.088	0.8704
X10_P16	0.800	1.088	0.8704
X14_P16	0.800	1.768	1.4144
X19_P16	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0005	0.0007	0.0014	0.0014
B	0.0005	0.0009	0.0013	0.0013
C	0.0005	0.0007	0.0015	0.0015
D	0.0005	0.0007	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0523	0.0445	3.3564	1.6898
A to Z ↑	0.0358	0.0332	5.1524	2.5537
B to Z ↓	0.0481	0.0409	3.3442	1.6839

B to Z ↑	0.0367	0.0344	5.1553	2.5549
C to Z ↓	0.0468	0.0405	3.3442	1.6832
C to Z ↑	0.0302	0.0277	5.1464	2.5482
D to Z ↓	0.0445	0.0383	3.3389	1.6821
D to Z ↑	0.0326	0.0298	5.1465	2.5495
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0404	0.0433	1.1581	0.8744
A to Z ↑	0.0295	0.0313	1.7560	1.3136
B to Z ↓	0.0378	0.0408	1.1566	0.8743
B to Z ↑	0.0314	0.0334	1.7560	1.3136
C to Z ↓	0.0367	0.0399	1.1545	0.8726
C to Z ↑	0.0254	0.0274	1.7510	1.3101
D to Z ↓	0.0343	0.0376	1.1550	0.8726
D to Z ↑	0.0269	0.0291	1.7500	1.3106

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.564e-07	1.000e-20
X10_P16	2.910e-07	1.000e-20
X14_P16	4.929e-07	1.000e-20
X19_P16	5.548e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	2.294e-05	2.924e-05	4.318e-05	4.313e-05
B (output stable)	4.830e-05	5.951e-05	6.318e-05	6.351e-05
C (output stable)	8.703e-06	1.157e-05	2.123e-05	1.996e-05
D (output stable)	1.970e-05	3.254e-05	6.159e-05	6.427e-05
A to Z	2.322e-03	3.540e-03	5.814e-03	6.788e-03
B to Z	2.102e-03	3.197e-03	5.432e-03	6.407e-03
C to Z	1.919e-03	2.927e-03	4.700e-03	5.688e-03
D to Z	1.819e-03	2.770e-03	4.367e-03	5.338e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

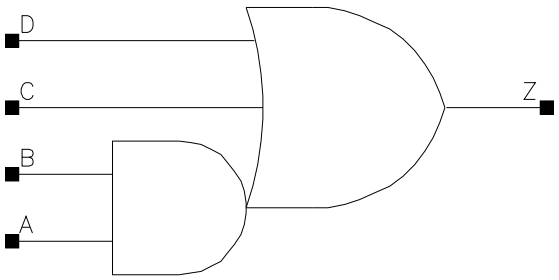
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	1.088	0.8704
X19_P16	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0005	0.0007	0.0012
B	0.0005	0.0007	0.0012
C	0.0005	0.0006	0.0014
D	0.0005	0.0006	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0606	0.0517	3.7505	1.7668
A to Z ↑	0.0323	0.0280	5.3470	2.5678
B to Z ↓	0.0578	0.0480	3.7466	1.7614
B to Z ↑	0.0347	0.0300	5.3506	2.5650
C to Z ↓	0.0642	0.0549	3.7377	1.7612
C to Z ↑	0.0297	0.0363	5.3043	2.5698

D to Z ↓	0.0636	0.0552	3.7397	1.7617
D to Z ↑	0.0296	0.0358	5.3078	2.5679
	X19_P16		**X19_P16**	
A to Z ↓	0.0506		0.9164	
A to Z ↑	0.0304		1.2755	
B to Z ↓	0.0457		0.9134	
B to Z ↑	0.0312		1.2757	
C to Z ↓	0.0526		0.9133	
C to Z ↑	0.0301		1.2665	
D to Z ↓	0.0518		0.9134	
D to Z ↑	0.0297		1.2665	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.217e-07	1.000e-20
X10_P16	2.332e-07	1.000e-20
X19_P16	4.392e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	1.873e-06	3.240e-06	1.410e-05
B (output stable)	6.096e-06	9.837e-06	4.163e-05
C (output stable)	8.273e-05	1.530e-04	2.733e-04
D (output stable)	4.874e-06	1.060e-05	1.621e-05
A to Z	1.857e-03	3.022e-03	5.794e-03
B to Z	1.776e-03	2.852e-03	5.294e-03
C to Z	2.160e-03	3.623e-03	6.805e-03
D to Z	2.037e-03	3.413e-03	6.327e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

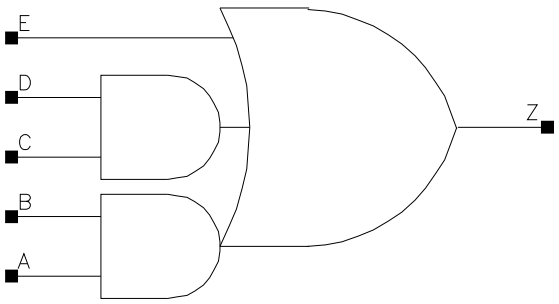
Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.088	0.8704
X10_P16	0.800	1.224	0.9792
X19_P16	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0004	0.0007	0.0013
B	0.0005	0.0007	0.0012
C	0.0005	0.0008	0.0013
D	0.0005	0.0007	0.0012
E	0.0005	0.0007	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0767	0.0611	3.5569	1.7567
A to Z ↑	0.0406	0.0347	5.2096	2.5824

B to Z ↓	0.0752	0.0584	3.5506	1.7545
B to Z ↑	0.0442	0.0371	5.2069	2.5806
C to Z ↓	0.0671	0.0537	3.5419	1.7507
C to Z ↑	0.0357	0.0295	5.1696	2.5630
D to Z ↓	0.0630	0.0488	3.5287	1.7439
D to Z ↑	0.0382	0.0313	5.1721	2.5620
E to Z ↓	0.0679	0.0539	3.5229	1.7441
E to Z ↑	0.0316	0.0272	5.1162	2.5442
	X19_P16		**X19_P16**	
A to Z ↓	0.0592		0.9089	
A to Z ↑	0.0359		1.2954	
B to Z ↓	0.0564		0.9082	
B to Z ↑	0.0385		1.2953	
C to Z ↓	0.0506		0.9045	
C to Z ↑	0.0298		1.2861	
D to Z ↓	0.0476		0.9033	
D to Z ↑	0.0320		1.2859	
E to Z ↓	0.0520		0.9026	
E to Z ↑	0.0333		1.2804	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.500e-07	1.000e-20
X10_P16	2.954e-07	1.000e-20
X19_P16	5.244e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	1.292e-05	2.455e-05	5.109e-05
B (output stable)	3.825e-05	4.819e-05	9.649e-05
C (output stable)	7.834e-06	9.794e-06	1.931e-05
D (output stable)	6.452e-06	1.447e-05	2.421e-05
E (output stable)	6.434e-05	7.637e-05	1.636e-04
A to Z	2.588e-03	4.012e-03	7.668e-03
B to Z	2.533e-03	3.838e-03	7.328e-03
C to Z	2.103e-03	3.168e-03	5.919e-03
D to Z	2.009e-03	2.970e-03	5.627e-03
E to Z	2.248e-03	3.452e-03	6.549e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

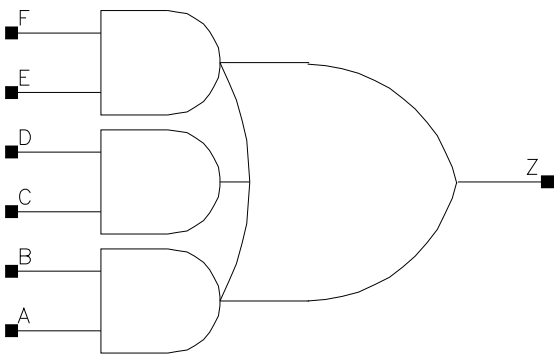
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.360	1.0880
X5_P16	0.800	1.360	1.0880
X10_P16	0.800	1.632	1.3056
X19_P16	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P16	X5_P16	X10_P16	X19_P16
A	0.0005	0.0005	0.0008	0.0013

B	0.0006	0.0005	0.0008	0.0012
C	0.0007	0.0007	0.0006	0.0012
D	0.0005	0.0005	0.0006	0.0011
E	0.0007	0.0007	0.0007	0.0013
F	0.0006	0.0006	0.0006	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X5_P16**	**X2_P16**	**X5_P16**
A to Z ↓	0.0591	0.0611	6.5800	3.6064
A to Z ↑	0.0397	0.0392	10.5948	5.4489
B to Z ↓	0.0564	0.0584	6.5607	3.5968
B to Z ↑	0.0426	0.0423	10.5885	5.4477
C to Z ↓	0.0552	0.0573	6.5697	3.6021
C to Z ↑	0.0369	0.0365	10.4999	5.4069
D to Z ↓	0.0507	0.0528	6.5518	3.5946
D to Z ↑	0.0388	0.0385	10.4983	5.4082
E to Z ↓	0.0456	0.0476	6.5376	3.5871
E to Z ↑	0.0307	0.0304	10.4483	5.3847
F to Z ↓	0.0417	0.0441	6.5239	3.5799
F to Z ↑	0.0323	0.0322	10.4418	5.3837
	X10_P16	**X19_P16**	**X10_P16**	**X19_P16**
A to Z ↓	0.0653	0.0612	1.7513	0.9056
A to Z ↑	0.0422	0.0385	2.5964	1.3019
B to Z ↓	0.0617	0.0588	1.7445	0.9052
B to Z ↑	0.0439	0.0412	2.5960	1.3016
C to Z ↓	0.0601	0.0568	1.7471	0.9045
C to Z ↑	0.0374	0.0355	2.5817	1.2933
D to Z ↓	0.0577	0.0547	1.7430	0.9042
D to Z ↑	0.0402	0.0382	2.5807	1.2929
E to Z ↓	0.0526	0.0510	1.7407	0.9014
E to Z ↑	0.0322	0.0310	2.5704	1.2888
F to Z ↓	0.0493	0.0478	1.7353	0.8998
F to Z ↑	0.0344	0.0332	2.5710	1.2888

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P16	1.719e-07	1.000e-20
X5_P16	2.054e-07	1.000e-20
X10_P16	3.198e-07	1.000e-20
X19_P16	6.078e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P16	X5_P16	X10_P16	X19_P16
A (output stable)	5.422e-05	5.417e-05	6.558e-05	1.189e-04
B (output stable)	1.499e-04	1.497e-04	1.844e-04	3.049e-04
C (output stable)	2.536e-05	2.531e-05	3.117e-05	4.513e-05
D (output stable)	3.083e-05	3.077e-05	4.456e-05	6.613e-05
E (output stable)	1.596e-05	1.602e-05	2.019e-05	2.929e-05
F (output stable)	2.114e-05	2.118e-05	2.682e-05	4.616e-05

A to Z	2.662e-03	2.987e-03	4.491e-03	8.277e-03
B to Z	2.548e-03	2.872e-03	4.207e-03	7.950e-03
C to Z	2.196e-03	2.520e-03	3.887e-03	7.196e-03
D to Z	2.050e-03	2.373e-03	3.749e-03	6.916e-03
E to Z	1.661e-03	1.981e-03	3.295e-03	6.209e-03
F to Z	1.544e-03	1.864e-03	3.144e-03	5.898e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

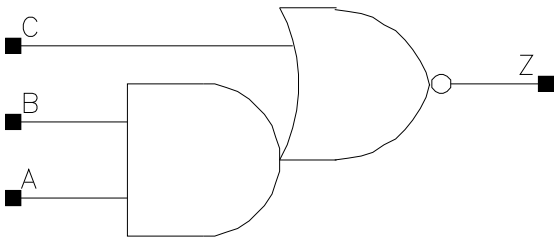
Pin Cycle (vdds)	X2_P16	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X10_P16	0.800	1.360	1.0880
X19_P16	0.800	2.584	2.0672
X25_P16	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P16	X10_P16	X19_P16	X25_P16
A	0.0007	0.0017	0.0033	0.0043
B	0.0006	0.0015	0.0030	0.0040
C	0.0006	0.0018	0.0033	0.0044

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X10_P16**	**X3_P16**	**X10_P16**
A to Z ↓	0.0110	0.0119	5.6927	2.0676
A to Z ↑	0.0201	0.0206	9.9428	3.3990
B to Z ↓	0.0114	0.0118	5.7730	2.0971
B to Z ↑	0.0165	0.0162	9.8059	3.3927
C to Z ↓	0.0120	0.0123	3.4281	1.1971
C to Z ↑	0.0209	0.0213	9.0494	3.1183
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0126	0.0124	1.0533	0.8042

A to Z ↑	0.0212	0.0209	1.7386	1.2939
B to Z ↓	0.0118	0.0118	1.0693	0.8165
B to Z ↑	0.0164	0.0163	1.7389	1.3094
C to Z ↓	0.0139	0.0140	0.7301	0.5600
C to Z ↑	0.0216	0.0215	1.5970	1.1950

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.197e-07	1.000e-20
X10_P16	3.344e-07	1.000e-20
X19_P16	6.360e-07	1.000e-20
X25_P16	8.360e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X10_P16	X19_P16	X25_P16
A (output stable)	7.356e-06	2.458e-05	5.449e-05	6.371e-05
B (output stable)	2.394e-05	1.234e-04	2.635e-04	3.346e-04
C (output stable)	6.232e-05	2.049e-04	4.039e-04	5.572e-04
A to Z	7.201e-04	2.282e-03	4.753e-03	6.158e-03
B to Z	5.572e-04	1.598e-03	3.255e-03	4.300e-03
C to Z	1.069e-03	3.212e-03	6.393e-03	8.532e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

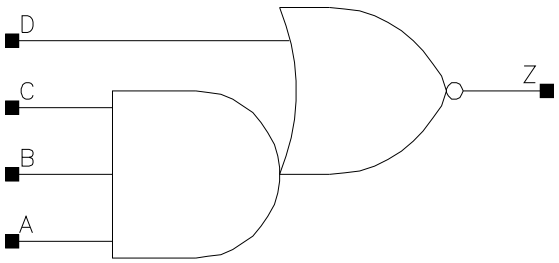
Pin Cycle (vdds)	X3_P16	X10_P16	X19_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X17_P16	0.800	3.536	2.8288
X22_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X17_P16	X22_P16
A	0.0006	0.0033	0.0044
B	0.0006	0.0031	0.0041
C	0.0007	0.0029	0.0039
D	0.0007	0.0034	0.0043

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X17_P16	X3_P16	X17_P16
A to Z ↓	0.0163	0.0177	8.0407	1.5371
A to Z ↑	0.0262	0.0255	9.9573	1.6735
B to Z ↓	0.0166	0.0174	8.0695	1.5432
B to Z ↑	0.0235	0.0227	9.9745	1.7002
C to Z ↓	0.0176	0.0159	8.1256	1.5536
C to Z ↑	0.0216	0.0184	9.9956	1.7121
D to Z ↓	0.0144	0.0161	3.3453	0.7192

D to Z ↑	0.0258	0.0244	8.5341	1.4478
	X22_P16		**X22_P16**	
A to Z ↓	0.0176		1.1680	
A to Z ↑	0.0252		1.2506	
B to Z ↓	0.0171		1.1732	
B to Z ↑	0.0223		1.2755	
C to Z ↓	0.0158		1.1821	
C to Z ↑	0.0182		1.2874	
D to Z ↓	0.0167		0.5955	
D to Z ↑	0.0238		1.0822	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.402e-07	1.000e-20
X17_P16	7.139e-07	1.000e-20
X22_P16	9.257e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X17_P16	X22_P16
A (output stable)	8.553e-06	6.227e-05	8.381e-05
B (output stable)	1.900e-05	1.431e-04	1.811e-04
C (output stable)	3.641e-05	3.091e-04	4.084e-04
D (output stable)	4.169e-04	2.299e-03	2.973e-03
A to Z	1.184e-03	6.855e-03	8.924e-03
B to Z	1.009e-03	5.529e-03	7.158e-03
C to Z	8.529e-04	4.083e-03	5.280e-03
D to Z	1.558e-03	8.428e-03	1.096e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

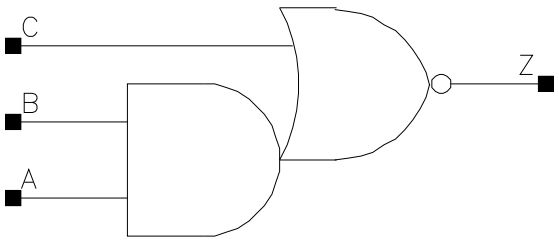
Pin Cycle (vdds)	X3_P16	X17_P16	X22_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X6_P16	0.800	1.088	0.8704
X9_P16	0.800	1.360	1.0880
X12_P16	0.800	1.904	1.5232
X25_P16	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X9_P16	X12_P16
A	0.0005	0.0012	0.0018	0.0025
B	0.0005	0.0012	0.0017	0.0023
C	0.0006	0.0010	0.0015	0.0020
	X25_P16			
A	0.0049			
B	0.0044			
C	0.0039			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0150	0.0150	7.4621	3.0034
A to Z ↑	0.0233	0.0246	11.3593	5.0432
B to Z ↓	0.0166	0.0149	7.5189	3.0385

B to Z ↑	0.0210	0.0208	11.2107	5.0584
C to Z ↓	0.0101	0.0088	4.5413	2.1641
C to Z ↑	0.0175	0.0160	10.4530	4.6760
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0144	0.0149	2.0668	1.5490
A to Z ↑	0.0233	0.0235	3.3784	2.4942
B to Z ↓	0.0148	0.0147	2.0933	1.5688
B to Z ↑	0.0194	0.0196	3.3792	2.5263
C to Z ↓	0.0088	0.0087	1.4782	1.1062
C to Z ↑	0.0153	0.0154	3.1340	2.3312
	X25_P16		**X25_P16**	
A to Z ↓	0.0148		0.8090	
A to Z ↑	0.0229		1.2657	
B to Z ↓	0.0148		0.8186	
B to Z ↑	0.0191		1.2713	
C to Z ↓	0.0085		0.5635	
C to Z ↑	0.0149		1.1789	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	9.627e-08	1.000e-20
X6_P16	2.336e-07	1.000e-20
X9_P16	3.297e-07	1.000e-20
X12_P16	4.465e-07	1.000e-20
X25_P16	8.648e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	1.769e-05	5.326e-05	6.744e-05	9.870e-05
B (output stable)	8.355e-05	2.742e-04	3.187e-04	4.722e-04
C (output stable)	3.260e-05	8.231e-05	1.115e-04	1.639e-04
A to Z	9.908e-04	2.450e-03	3.361e-03	4.640e-03
B to Z	8.601e-04	1.938e-03	2.611e-03	3.548e-03
C to Z	5.148e-04	1.105e-03	1.498e-03	2.083e-03
	X25_P16			
A (output stable)	1.860e-04			
B (output stable)	8.617e-04			
C (output stable)	3.075e-04			
A to Z	8.822e-03			
B to Z	6.789e-03			
C to Z	3.883e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

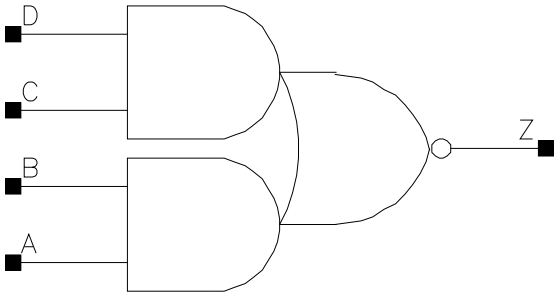
	X25_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.680	0.5440
X6_P16	0.800	1.224	0.9792
X9_P16	0.800	1.768	1.4144
X12_P16	0.800	2.448	1.9584
X24_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P16	X6_P16	X9_P16	X12_P16
A	0.0005	0.0013	0.0018	0.0025
B	0.0005	0.0011	0.0017	0.0023
C	0.0005	0.0013	0.0017	0.0022
D	0.0004	0.0010	0.0015	0.0021
	X24_P16			
A	0.0048			
B	0.0046			
C	0.0044			
D	0.0041			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X6_P16**	**X2_P16**	**X6_P16**
A to Z ↓	0.0151	0.0155	7.5887	2.8909
A to Z ↑	0.0291	0.0255	14.3088	4.6083
B to Z ↓	0.0166	0.0167	7.6699	2.9188
B to Z ↑	0.0260	0.0227	14.2783	4.7022
C to Z ↓	0.0112	0.0110	7.6102	2.9038
C to Z ↑	0.0227	0.0201	14.3022	4.6015
D to Z ↓	0.0118	0.0115	7.7228	2.9449
D to Z ↑	0.0193	0.0171	14.2744	4.7387
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0167	0.0173	2.0731	1.5589
A to Z ↑	0.0266	0.0271	3.0875	2.3197
B to Z ↓	0.0178	0.0177	2.0943	1.5748
B to Z ↑	0.0234	0.0235	3.0917	2.2907
C to Z ↓	0.0120	0.0127	2.0679	1.5619
C to Z ↑	0.0211	0.0216	3.0852	2.3001
D to Z ↓	0.0121	0.0119	2.1007	1.5861
D to Z ↑	0.0173	0.0174	3.0866	2.3108
	X24_P16		**X24_P16**	
A to Z ↓	0.0172		0.8043	
A to Z ↑	0.0266		1.1691	
B to Z ↓	0.0179		0.8126	
B to Z ↑	0.0232		1.1605	
C to Z ↓	0.0127		0.7869	
C to Z ↑	0.0216		1.1642	
D to Z ↓	0.0120		0.7998	
D to Z ↑	0.0174		1.1699	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P16	9.911e-08	1.000e-20
X6_P16	2.840e-07	1.000e-20
X9_P16	4.171e-07	1.000e-20
X12_P16	5.604e-07	1.000e-20
X24_P16	1.099e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P16	X6_P16	X9_P16	X12_P16
A (output stable)	1.609e-05	4.325e-05	7.935e-05	1.185e-04
B (output stable)	2.393e-05	6.351e-05	1.259e-04	1.846e-04
C (output stable)	6.797e-06	2.050e-05	4.534e-05	7.889e-05
D (output stable)	2.077e-05	6.081e-05	1.582e-04	2.654e-04
A to Z	1.055e-03	2.766e-03	4.398e-03	6.035e-03
B to Z	9.135e-04	2.371e-03	3.678e-03	5.029e-03
C to Z	5.903e-04	1.547e-03	2.553e-03	3.584e-03
D to Z	4.646e-04	1.220e-03	1.896e-03	2.590e-03
	X24_P16			
A (output stable)	2.148e-04			
B (output stable)	3.273e-04			
C (output stable)	1.615e-04			
D (output stable)	5.137e-04			

A to Z	1.167e-02			
B to Z	9.784e-03			
C to Z	6.969e-03			
D to Z	5.100e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

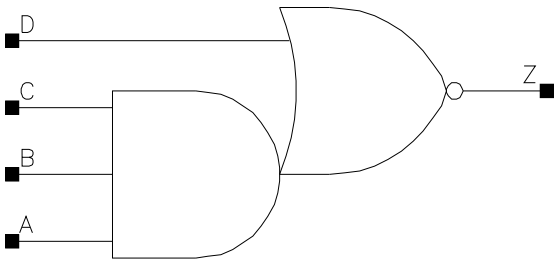
Pin Cycle (vdds)	X2_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X12_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X12_P16
A	0.0006	0.0024
B	0.0006	0.0023
C	0.0008	0.0022
D	0.0006	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X12_P16	X3_P16	X12_P16
A to Z ↓	0.0191	0.0202	8.0537	2.2826
A to Z ↑	0.0286	0.0276	9.7343	2.5321
B to Z ↓	0.0199	0.0199	8.0774	2.2879
B to Z ↑	0.0268	0.0249	9.8719	2.5313
C to Z ↓	0.0220	0.0191	8.1250	2.3000
C to Z ↑	0.0258	0.0213	9.9330	2.5487
D to Z ↓	0.0095	0.0082	3.4240	0.9358
D to Z ↑	0.0186	0.0162	8.4490	2.1749

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.470e-07	1.000e-20
X12_P16	5.301e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X12_P16
A (output stable)	5.540e-05	1.908e-04
B (output stable)	2.568e-05	1.152e-04
C (output stable)	4.461e-05	2.306e-04
D (output stable)	5.793e-05	2.280e-04
A to Z	1.601e-03	5.965e-03
B to Z	1.431e-03	5.001e-03
C to Z	1.302e-03	4.005e-03
D to Z	7.507e-04	2.357e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

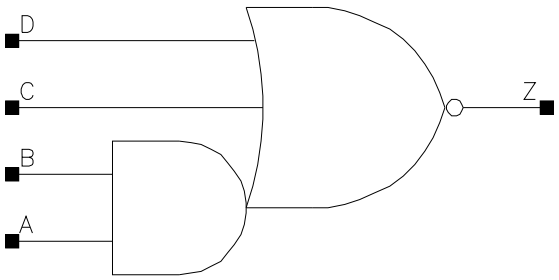
Pin Cycle (vdds)	X3_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X20_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P16	X20_P16
A	0.0006	0.0043
B	0.0005	0.0039
C	0.0006	0.0042
D	0.0006	0.0039

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X20_P16	X3_P16	X20_P16
A to Z ↓	0.0127	0.0140	5.5841	0.9103
A to Z ↑	0.0263	0.0250	14.4557	1.8696
B to Z ↓	0.0138	0.0140	5.6550	0.9234
B to Z ↑	0.0229	0.0198	14.5956	1.8726
C to Z ↓	0.0142	0.0188	3.4022	0.7124
C to Z ↑	0.0318	0.0303	13.7421	1.7638
D to Z ↓	0.0138	0.0173	3.4011	0.7110

D to Z ↑	0.0319	0.0283	13.7672	1.7685

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.332e-07	1.000e-20
X20_P16	8.072e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X20_P16
A (output stable)	3.604e-06	4.402e-05
B (output stable)	1.139e-05	1.321e-04
C (output stable)	1.562e-04	1.426e-03
D (output stable)	1.077e-05	6.025e-05
A to Z	9.606e-04	6.580e-03
B to Z	7.991e-04	4.894e-03
C to Z	1.576e-03	1.169e-02
D to Z	1.364e-03	9.150e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

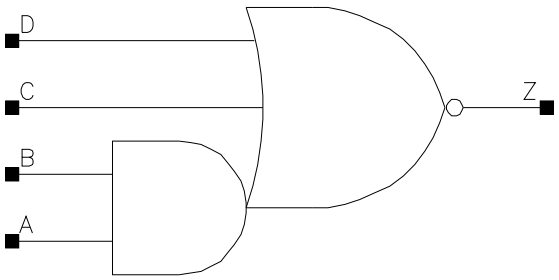
Pin Cycle (vdds)	X3_P16	X20_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.816	0.6528
X10_P16	0.800	2.448	1.9584
X19_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P16	X10_P16	X19_P16
A	0.0006	0.0023	0.0046
B	0.0006	0.0022	0.0043
C	0.0007	0.0019	0.0038
D	0.0005	0.0018	0.0034

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	X10_P16	X2_P16	X10_P16
A to Z ↓	0.0168	0.0175	6.6107	1.7726
A to Z ↑	0.0335	0.0318	15.2925	3.7327
B to Z ↓	0.0186	0.0181	6.6793	1.7892
B to Z ↑	0.0302	0.0272	15.3513	3.7445
C to Z ↓	0.0154	0.0143	5.6854	1.4367
C to Z ↑	0.0251	0.0235	14.5306	3.5385

D to Z ↓	0.0129	0.0109	5.7382	1.4537
D to Z ↑	0.0222	0.0185	14.5798	3.5586
	X19_P16		**X19_P16**	
A to Z ↓	0.0171		0.9098	
A to Z ↑	0.0311		1.8935	
B to Z ↓	0.0180		0.9192	
B to Z ↑	0.0266		1.8946	
C to Z ↓	0.0148		0.7748	
C to Z ↑	0.0228		1.7931	
D to Z ↓	0.0112		0.7847	
D to Z ↑	0.0177		1.8040	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P16	1.088e-07	1.000e-20
X10_P16	4.263e-07	1.000e-20
X19_P16	8.278e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P16	X10_P16	X19_P16
A (output stable)	2.571e-05	1.042e-04	2.044e-04
B (output stable)	4.918e-05	2.130e-04	4.038e-04
C (output stable)	3.344e-05	2.521e-04	4.842e-04
D (output stable)	5.134e-06	6.434e-05	1.184e-04
A to Z	1.532e-03	5.837e-03	1.122e-02
B to Z	1.369e-03	4.875e-03	9.404e-03
C to Z	9.053e-04	3.491e-03	6.601e-03
D to Z	6.752e-04	2.158e-03	3.996e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

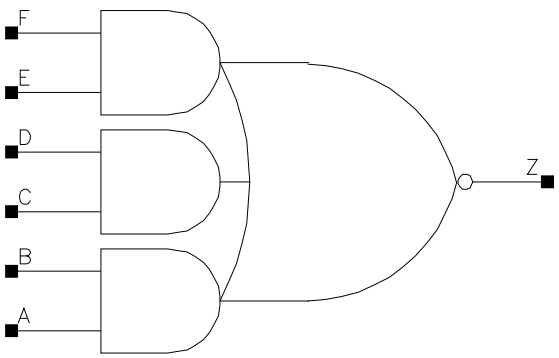
Pin Cycle (vdds)	X2_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.088	0.8704
X5_P16	0.800	2.040	1.6320
X7_P16	0.800	2.720	2.1760
X9_P16	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P16	X5_P16	X7_P16	X9_P16
A	0.0006	0.0011	0.0018	0.0023

B	0.0006	0.0012	0.0016	0.0021
C	0.0006	0.0010	0.0016	0.0024
D	0.0006	0.0012	0.0015	0.0021
E	0.0007	0.0011	0.0016	0.0020
F	0.0005	0.0009	0.0014	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X5_P16**	**X2_P16**	**X5_P16**
A to Z ↓	0.0178	0.0214	5.9093	3.3756
A to Z ↑	0.0428	0.0400	14.8241	6.7411
B to Z ↓	0.0198	0.0238	5.9680	3.3954
B to Z ↑	0.0392	0.0376	14.8910	6.6932
C to Z ↓	0.0166	0.0194	5.9545	3.3547
C to Z ↑	0.0377	0.0358	14.9004	6.7515
D to Z ↓	0.0183	0.0213	6.0313	3.3829
D to Z ↑	0.0341	0.0335	14.8929	6.7235
E to Z ↓	0.0128	0.0148	5.9946	3.2945
E to Z ↑	0.0290	0.0284	14.8846	6.7024
F to Z ↓	0.0135	0.0158	6.0933	3.3291
F to Z ↑	0.0243	0.0249	14.8573	6.7250
	X7_P16	**X9_P16**	**X7_P16**	**X9_P16**
A to Z ↓	0.0213	0.0218	2.3473	1.7873
A to Z ↑	0.0392	0.0401	4.4170	3.3225
B to Z ↓	0.0229	0.0230	2.3634	1.7994
B to Z ↑	0.0359	0.0363	4.5128	3.3741
C to Z ↓	0.0194	0.0201	2.3548	1.7744
C to Z ↑	0.0354	0.0368	4.4989	3.3724
D to Z ↓	0.0208	0.0204	2.3770	1.7906
D to Z ↑	0.0315	0.0318	4.4609	3.3463
E to Z ↓	0.0143	0.0145	2.3519	1.7767
E to Z ↑	0.0270	0.0271	4.4491	3.3526
F to Z ↓	0.0150	0.0143	2.3854	1.8035
F to Z ↑	0.0233	0.0225	4.4911	3.3514

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P16	1.847e-07	1.000e-20
X5_P16	3.579e-07	1.000e-20
X7_P16	5.204e-07	1.000e-20
X9_P16	6.897e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

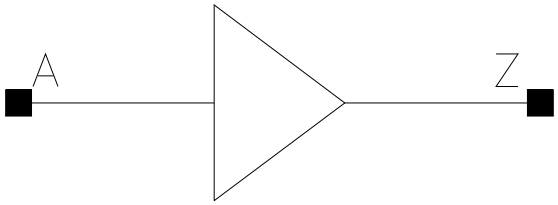
Pin Cycle (vdd)	X2_P16	X5_P16	X7_P16	X9_P16
A (output stable)	5.927e-05	1.198e-04	1.870e-04	2.640e-04
B (output stable)	1.777e-04	3.433e-04	5.054e-04	7.182e-04
C (output stable)	2.773e-05	5.233e-05	8.425e-05	1.343e-04
D (output stable)	4.298e-05	8.387e-05	1.350e-04	1.923e-04
E (output stable)	1.552e-05	2.909e-05	5.810e-05	8.552e-05
F (output stable)	2.511e-05	4.634e-05	9.731e-05	1.594e-04

A to Z	2.093e-03	4.275e-03	6.290e-03	8.589e-03
B to Z	1.915e-03	4.020e-03	5.651e-03	7.659e-03
C to Z	1.562e-03	3.272e-03	4.782e-03	6.497e-03
D to Z	1.389e-03	3.017e-03	4.191e-03	5.655e-03
E to Z	9.578e-04	2.203e-03	3.057e-03	4.062e-03
F to Z	7.982e-04	1.906e-03	2.507e-03	3.208e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P16	X5_P16	X7_P16	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.544	0.4352
X5_P16	0.800	0.544	0.4352
X9_P16	0.800	0.680	0.5440
X11_P16	1.600	0.408	0.6528
X13_P16	0.800	0.680	0.5440
X19_P16	0.800	0.952	0.7616
X23_P16	1.600	0.544	0.8704
X24_P16	0.800	1.088	0.8704
X29_P16	0.800	1.224	0.9792
X34_P16	1.600	0.680	1.0880
X38_P16	0.800	1.632	1.3056
X46_P16	1.600	0.952	1.5232
X57_P16	0.800	2.312	1.8496
X68_P16	1.600	1.224	1.9584
X91_P16	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P16	X5_P16	X9_P16	X11_P16
A	0.0006	0.0006	0.0006	0.0009
	X13_P16	X19_P16	X23_P16	X24_P16
A	0.0008	0.0011	0.0013	0.0013
	X29_P16	X34_P16	X38_P16	X46_P16
A	0.0015	0.0016	0.0022	0.0022
	X57_P16	X68_P16	X91_P16	
A	0.0029	0.0031	0.0040	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X5_P16**	**X2_P16**	**X5_P16**
A to Z ↓	0.0292	0.0301	6.2739	3.4276
A to Z ↑	0.0227	0.0226	10.3673	5.2830
	X9_P16	**X11_P16**	**X9_P16**	**X11_P16**
A to Z ↓	0.0363	0.0336	1.7654	1.3245
A to Z ↑	0.0270	0.0244	2.6373	2.4755
	X13_P16	**X19_P16**	**X13_P16**	**X19_P16**
A to Z ↓	0.0318	0.0320	1.2152	0.8579
A to Z ↑	0.0253	0.0238	1.8358	1.2799
	X23_P16	**X24_P16**	**X23_P16**	**X24_P16**
A to Z ↓	0.0324	0.0314	0.6422	0.7000
A to Z ↑	0.0236	0.0244	1.2454	1.0258
	X29_P16	**X34_P16**	**X29_P16**	**X34_P16**
A to Z ↓	0.0301	0.0315	0.5796	0.4426
A to Z ↑	0.0238	0.0236	0.8621	0.8500
	X38_P16	**X46_P16**	**X38_P16**	**X46_P16**
A to Z ↓	0.0296	0.0312	0.4389	0.3323
A to Z ↑	0.0236	0.0230	0.6345	0.6408
	X57_P16	**X68_P16**	**X57_P16**	**X68_P16**
A to Z ↓	0.0307	0.0305	0.2956	0.2260
A to Z ↑	0.0244	0.0229	0.4256	0.4284
	X91_P16		**X91_P16**	
A to Z ↓	0.0321		0.1750	
A to Z ↑	0.0239		0.3225	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P16	6.546e-08	1.000e-20
X5_P16	1.033e-07	1.000e-20
X9_P16	1.668e-07	1.000e-20
X11_P16	2.220e-07	1.000e-20
X13_P16	2.518e-07	1.000e-20
X19_P16	3.368e-07	1.000e-20
X23_P16	4.290e-07	1.000e-20
X24_P16	4.183e-07	1.000e-20
X29_P16	5.066e-07	1.000e-20
X34_P16	6.140e-07	1.000e-20
X38_P16	6.873e-07	1.000e-20
X46_P16	7.938e-07	1.000e-20
X57_P16	9.886e-07	1.000e-20
X68_P16	1.170e-06	1.000e-20
X91_P16	1.511e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P16	X5_P16	X9_P16	X11_P16
A to Z	1.109e-03	1.434e-03	2.269e-03	2.756e-03
	X13_P16	X19_P16	X23_P16	X24_P16
A to Z	3.296e-03	4.435e-03	5.012e-03	5.497e-03
	X29_P16	X34_P16	X38_P16	X46_P16

A to Z	6.384e-03	7.454e-03	8.834e-03	9.634e-03
	X57_P16	X68_P16	X91_P16	
A to Z	1.287e-02	1.400e-02	1.884e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

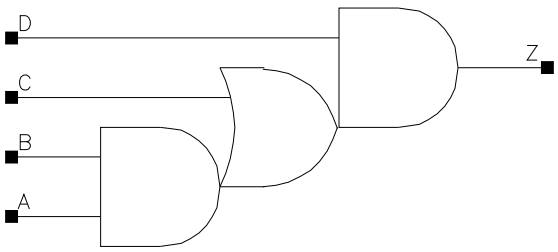
Pin Cycle (vdds)	X2_P16	X5_P16	X9_P16	X11_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P16	X19_P16	X23_P16	X24_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P16	X34_P16	X38_P16	X46_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P16	X68_P16	X91_P16	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.952	0.7616
X10_P16	0.800	1.632	1.3056
X14_P16	0.800	1.768	1.4144
X19_P16	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0007	0.0014	0.0014	0.0014
B	0.0007	0.0013	0.0013	0.0013
C	0.0007	0.0016	0.0016	0.0016
D	0.0011	0.0014	0.0014	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0397	0.0366	3.5061	1.6591
A to Z ↑	0.0360	0.0329	5.4281	2.5727
B to Z ↓	0.0369	0.0337	3.4998	1.6576
B to Z ↑	0.0367	0.0332	5.4273	2.5727
C to Z ↓	0.0337	0.0306	3.4922	1.6529
C to Z ↑	0.0272	0.0244	5.3784	2.5501

D to Z ↓	0.0327	0.0284	3.4576	1.6371
D to Z ↑	0.0314	0.0268	5.3864	2.5524
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0406	0.0435	1.1636	0.8732
A to Z ↑	0.0366	0.0392	1.7306	1.2987
B to Z ↓	0.0379	0.0409	1.1633	0.8732
B to Z ↑	0.0372	0.0397	1.7276	1.2974
C to Z ↓	0.0346	0.0376	1.1581	0.8695
C to Z ↑	0.0274	0.0295	1.7076	1.2802
D to Z ↓	0.0309	0.0327	1.1411	0.8536
D to Z ↑	0.0296	0.0314	1.7110	1.2825

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.926e-07	1.000e-20
X10_P16	3.854e-07	1.000e-20
X14_P16	4.510e-07	1.000e-20
X19_P16	5.167e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	2.379e-05	5.136e-05	5.276e-05	5.303e-05
B (output stable)	5.401e-05	9.659e-05	9.737e-05	9.752e-05
C (output stable)	1.951e-04	3.301e-04	3.279e-04	3.274e-04
D (output stable)	6.340e-05	8.497e-05	8.643e-05	8.740e-05
A to Z	2.445e-03	4.435e-03	5.615e-03	6.545e-03
B to Z	2.274e-03	4.039e-03	5.214e-03	6.138e-03
C to Z	1.886e-03	3.254e-03	4.379e-03	5.281e-03
D to Z	2.478e-03	4.306e-03	5.411e-03	6.266e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

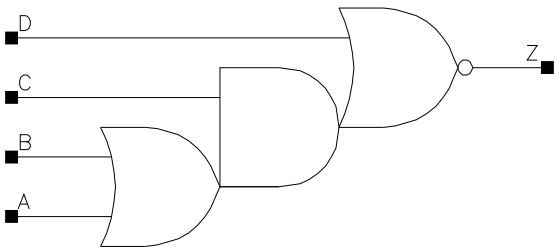
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X6_P16	0.800	1.496	1.1968
X9_P16	0.800	1.768	1.4144
X12_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X9_P16	X12_P16
A	0.0006	0.0012	0.0019	0.0024
B	0.0006	0.0011	0.0018	0.0023
C	0.0006	0.0011	0.0017	0.0022
D	0.0008	0.0011	0.0016	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0175	0.0162	5.8181	2.9703
A to Z ↑	0.0347	0.0343	14.4622	7.6099
B to Z ↓	0.0166	0.0160	5.6478	2.9906
B to Z ↑	0.0344	0.0331	14.4728	7.6230
C to Z ↓	0.0157	0.0148	5.3795	2.7893
C to Z ↑	0.0225	0.0214	9.9378	5.1455

D to Z ↓	0.0097	0.0080	3.4395	1.7521
D to Z ↑	0.0202	0.0173	10.5978	5.5109
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0164	0.0168	2.0493	1.5954
A to Z ↑	0.0322	0.0340	4.9115	3.7798
B to Z ↓	0.0157	0.0160	2.0663	1.5938
B to Z ↑	0.0319	0.0325	4.9157	3.7841
C to Z ↓	0.0151	0.0152	1.9364	1.4944
C to Z ↑	0.0207	0.0209	3.3392	2.5417
D to Z ↓	0.0081	0.0081	1.2251	0.9402
D to Z ↑	0.0163	0.0161	3.5698	2.7262

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.503e-07	1.000e-20
X6_P16	2.940e-07	1.000e-20
X9_P16	4.132e-07	1.000e-20
X12_P16	5.533e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	1.947e-05	4.939e-05	5.856e-05	1.062e-04
B (output stable)	1.810e-05	5.277e-05	7.373e-05	1.153e-04
C (output stable)	1.473e-04	3.412e-04	4.617e-04	6.895e-04
D (output stable)	1.494e-05	6.135e-05	6.383e-05	1.139e-04
A to Z	1.663e-03	3.157e-03	4.417e-03	6.163e-03
B to Z	1.433e-03	2.582e-03	3.747e-03	5.037e-03
C to Z	1.137e-03	2.072e-03	2.981e-03	4.070e-03
D to Z	6.985e-04	1.129e-03	1.561e-03	2.043e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

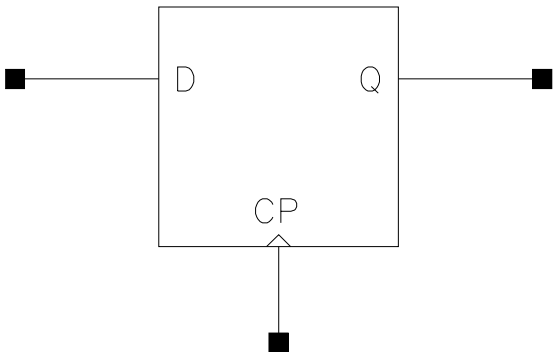
Pin Cycle (vdds)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	1.600	1.496	2.3936
X19_P16	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P16	X19_P16
CP	0.0009	0.0009
D	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P16	X19_P16	X10_P16	X19_P16
CP to Q ↓	0.0592	0.0797	1.7486	0.9607
CP to Q ↑	0.0667	0.0763	2.5442	1.3119

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P16	X19_P16
CP ↓	min_pulse_width to CP	0.0570	0.0570
CP ↑	min_pulse_width to CP	0.0499	0.0689
D ↓	hold_rising to CP	0.0123	0.0123
D ↑	hold_rising to CP	0.0081	0.0081
D ↓	setup_rising to CP	0.0321	0.0321
D ↑	setup_rising to CP	0.0200	0.0200

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P16	5.402e-07	1.000e-20
X19_P16	6.617e-07	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

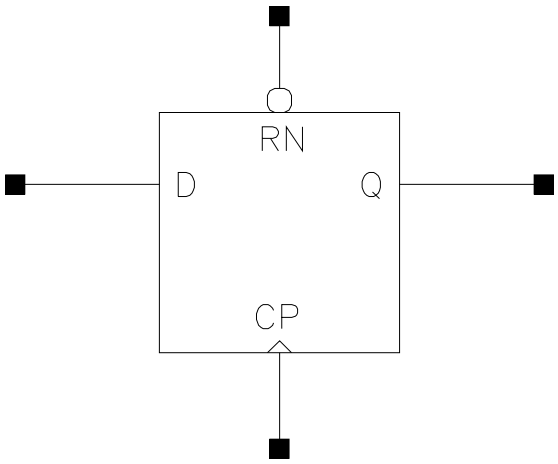
Pin Cycle	X10_P16	X19_P16
Clock 100Mhz Data 0Mhz	7.821e-03	7.825e-03
Clock 100Mhz Data 25Mhz	9.392e-03	1.081e-02
Clock 100Mhz Data 50Mhz	1.096e-02	1.379e-02
Clock = 0 Data 100Mhz	3.279e-03	3.279e-03
Clock = 1 Data 100Mhz	3.778e-05	3.785e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	1.600	1.768	2.8288
X19_P16	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P16	X19_P16
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P16	X19_P16	X10_P16	X19_P16
CP to Q ↓	0.0641	0.0831	1.7789	0.9524
CP to Q ↑	0.0693	0.0789	2.5463	1.3066
RN to Q ↓	0.0662	0.0859	1.7460	0.9164

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P16	X19_P16
CP ↓	min_pulse_width to CP	0.0570	0.0570
CP ↑	min_pulse_width to CP	0.0498	0.0701
D ↓	hold_rising to CP	0.0123	0.0123
D ↑	hold_rising to CP	0.0048	0.0048
D ↓	setup_rising to CP	0.0321	0.0321
D ↑	setup_rising to CP	0.0222	0.0222
RN ↓	min_pulse_width to RN	0.0806	0.1045
RN ↑	recovery_rising to CP	0.0125	0.0125
RN ↑	removal_rising to CP	-0.0077	-0.0077

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P16	6.311e-07	1.000e-20
X19_P16	7.730e-07	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

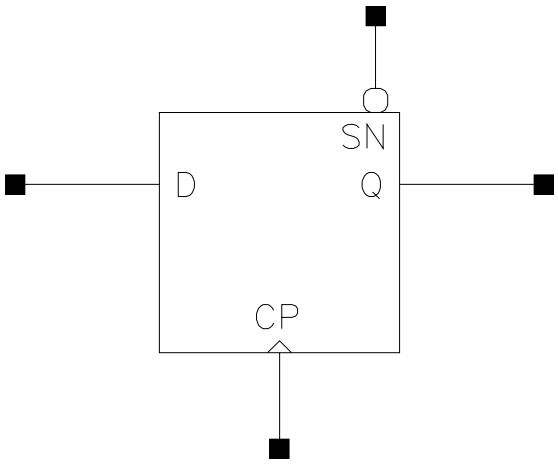
Pin Cycle	X10_P16	X19_P16
Clock 100Mhz Data 0Mhz	7.968e-03	7.968e-03
Clock 100Mhz Data 25Mhz	9.660e-03	1.109e-02
Clock 100Mhz Data 50Mhz	1.135e-02	1.421e-02
Clock = 0 Data 100Mhz	3.346e-03	3.346e-03
Clock = 1 Data 100Mhz	3.724e-05	3.733e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	1.600	1.768	2.8288
X19_P16	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P16	X19_P16
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P16	X19_P16	X10_P16	X19_P16
CP to Q ↓	0.0607	0.0813	1.7640	0.9446
CP to Q ↑	0.0688	0.0792	2.5415	1.3078
SN to Q ↑	0.0428	0.0487	2.4909	1.2650

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P16	X19_P16
CP ↓	min_pulse_width to CP	0.0584	0.0584
CP ↑	min_pulse_width to CP	0.0499	0.0689
D ↓	hold_rising to CP	0.0123	0.0123
D ↑	hold_rising to CP	0.0081	0.0081
D ↓	setup_rising to CP	0.0343	0.0343
D ↑	setup_rising to CP	0.0200	0.0200
SN ↓	min_pulse_width to SN	0.0469	0.0496
SN ↑	recovery_rising to CP	0.0058	0.0054
SN ↑	removal_rising to CP	0.0303	0.0303

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P16	6.523e-07	1.000e-20
X19_P16	7.811e-07	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

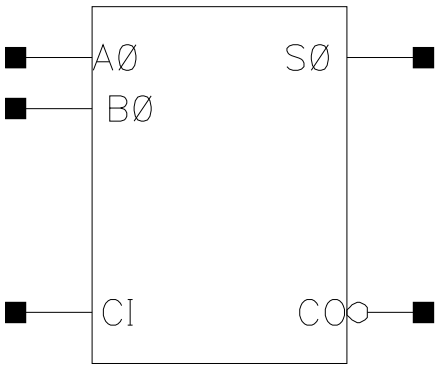
Pin Cycle	X10_P16	X19_P16
Clock 100Mhz Data 0Mhz	7.742e-03	7.745e-03
Clock 100Mhz Data 25Mhz	9.397e-03	1.089e-02
Clock 100Mhz Data 50Mhz	1.105e-02	1.404e-02
Clock = 0 Data 100Mhz	3.225e-03	3.225e-03
Clock = 1 Data 100Mhz	2.405e-05	2.416e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_-P16	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_-P16	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_-P16	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_-P16	1.600	2.720	4.3520
C8T28SOIDV_LLS1_-FA1X4_P16	1.600	2.040	3.2640
C8T28SOIDV_LLS1_-FA1X9_P16	1.600	3.128	5.0048
C8T28SOIDV_LLS1_-FA1X18_P16	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P16	C8T28SOIDV_LL_-FA1X9_P16	C8T28SOIDV_LL_-FA1X14_P16	C8T28SOIDV_LL_-FA1X19_P16
A0	0.0025	0.0027	0.0042	0.0045
B0	0.0021	0.0022	0.0038	0.0041
CI	0.0016	0.0017	0.0029	0.0032
	C8T28SOIDV_LLS1_-FA1X4_P16	C8T28SOIDV_LLS1_-FA1X9_P16	C8T28SOIDV_LLS1_-FA1X18_P16	
A0	0.0023	0.0032	0.0034	
B0	0.0023	0.0036	0.0040	
CI	0.0017	0.0025	0.0030	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P16	**C8T28SOIDV_LL_-FA1X9_P16**	**C8T28SOIDV_LL_-FA1X5_P16**	**C8T28SOIDV_LL_-FA1X9_P16**
A0 to CO ↓	0.0518	0.0553	3.6005	1.8501
A0 to CO ↑	0.0377	0.0402	5.0475	2.5752
A0 to S0 ↓	0.0558	0.0613	3.5286	1.8247
A0 to S0 ↑	0.0573	0.0622	5.0489	2.5305
B0 to CO ↓	0.0518	0.0554	3.6185	1.8612
B0 to CO ↑	0.0391	0.0415	5.0522	2.5796
B0 to S0 ↓	0.0562	0.0619	3.5273	1.8236
B0 to S0 ↑	0.0579	0.0630	5.0533	2.5325
CI to CO ↓	0.0492	0.0524	3.6247	1.8631
CI to CO ↑	0.0385	0.0409	5.0489	2.5767
CI to S0 ↓	0.0557	0.0616	3.5285	1.8233
CI to S0 ↑	0.0575	0.0626	5.0488	2.5318
	C8T28SOIDV_LL_-FA1X14_P16	**C8T28SOIDV_LL_-FA1X19_P16**	**C8T28SOIDV_LL_-FA1X14_P16**	**C8T28SOIDV_LL_-FA1X19_P16**
A0 to CO ↓	0.0530	0.0580	1.2113	0.9252
A0 to CO ↑	0.0385	0.0399	1.7722	1.3240
A0 to S0 ↓	0.0642	0.0650	1.2032	0.8927
A0 to S0 ↑	0.0653	0.0677	1.7076	1.2750
B0 to CO ↓	0.0521	0.0571	1.2160	0.9278
B0 to CO ↑	0.0391	0.0406	1.7720	1.3233
B0 to S0 ↓	0.0645	0.0653	1.2027	0.8925
B0 to S0 ↑	0.0655	0.0679	1.7089	1.2762
CI to CO ↓	0.0494	0.0542	1.2162	0.9279
CI to CO ↑	0.0382	0.0397	1.7728	1.3242
CI to S0 ↓	0.0632	0.0642	1.2020	0.8920
CI to S0 ↑	0.0644	0.0669	1.7084	1.2752
	C8T28SOIDV_-LLS1_FA1X4_P16	**C8T28SOIDV_-LLS1_FA1X9_P16**	**C8T28SOIDV_-LLS1_FA1X4_P16**	**C8T28SOIDV_-LLS1_FA1X9_P16**
A0 to CO ↓	0.0349	0.0320	6.7474	2.2579
A0 to CO ↑	0.0309	0.0290	5.1049	2.5765
A0 to S0 ↓	0.0729	0.0794	3.7702	1.3891
A0 to S0 ↑	0.0679	0.0670	5.3380	2.5199
B0 to CO ↓	0.0327	0.0329	6.7430	2.2585
B0 to CO ↑	0.0263	0.0274	5.0912	2.5743
B0 to S0 ↓	0.0736	0.0827	3.7684	1.3892
B0 to S0 ↑	0.0688	0.0704	5.3401	2.5196
CI to CO ↓	0.0330	0.0447	6.7393	2.2785
CI to CO ↑	0.0286	0.0269	5.1027	2.5932

CI to S0 ↓	0.0415	0.0498	3.7720	1.3908
CI to S0 ↑	0.0363	0.0370	5.3418	2.5208
	C8T28SOIDV_-LLS1_FA1X18_P16		**C8T28SOIDV_-LLS1_FA1X18_P16**	
A0 to CO ↓	0.0404		1.1920	
A0 to CO ↑	0.0306		1.2665	
A0 to S0 ↓	0.0840		0.7206	
A0 to S0 ↑	0.0683		1.2655	
B0 to CO ↓	0.0419		1.1932	
B0 to CO ↑	0.0290		1.2654	
B0 to S0 ↓	0.0853		0.7192	
B0 to S0 ↑	0.0705		1.2657	
CI to CO ↓	0.0558		1.2051	
CI to CO ↑	0.0316		1.2691	
CI to S0 ↓	0.0523		0.7222	
CI to S0 ↑	0.0346		1.2663	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P16	4.903e-07	1.000e-20
C8T28SOIDV_LL_FA1X9_P16	6.476e-07	1.000e-20
C8T28SOIDV_LL_FA1X14_P16	9.961e-07	1.000e-20
C8T28SOIDV_LL_FA1X19_P16	1.218e-06	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P16	8.083e-07	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P16	1.299e-06	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P16	2.002e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P16	C8T28SOIDV_LL_-FA1X9_P16	C8T28SOIDV_LL_-FA1X14_P16	C8T28SOIDV_LL_-FA1X19_P16
A0 to CO	2.743e-03	3.701e-03	6.183e-03	7.373e-03
A0 to S0	2.797e-03	3.636e-03	6.257e-03	7.498e-03
B0 to CO	2.684e-03	3.656e-03	6.071e-03	7.273e-03
B0 to S0	2.651e-03	3.505e-03	6.023e-03	7.229e-03
CI to CO	2.648e-03	3.595e-03	5.964e-03	7.211e-03
CI to S0	2.628e-03	3.473e-03	5.922e-03	7.131e-03
	C8T28SOIDV_LLS1_-FA1X4_P16	C8T28SOIDV_LLS1_-FA1X9_P16	C8T28SOIDV_LLS1_-FA1X18_P16	
A0 to CO	4.169e-03	6.331e-03	9.965e-03	
A0 to S0	5.654e-03	8.196e-03	1.241e-02	
B0 to CO	4.430e-03	6.459e-03	1.001e-02	
B0 to S0	6.051e-03	8.377e-03	1.255e-02	
CI to CO	2.954e-03	5.202e-03	8.581e-03	
CI to S0	3.350e-03	5.796e-03	9.362e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P16	C8T28SOIDV_LL_-FA1X9_P16	C8T28SOIDV_LL_-FA1X14_P16	C8T28SOIDV_LL_-FA1X19_P16
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P16	C8T28SOIDV_LLS1_-FA1X9_P16	C8T28SOIDV_LLS1_-FA1X18_P16	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P16	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P16	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P16	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P16	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P16	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P16	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P16	C8T28SOI_LL_-HA1X9_P16	C8T28SOI_LLS1_-HA1X5_P16	C8T28SOIDV_LL_-HA1X14_P16
A0	0.0008	0.0012	0.0014	0.0017
B0	0.0007	0.0012	0.0013	0.0015
	C8T28SOIDV_LL_-HA1X19_P16	C8T28SOIDV_LLS1_-HA1X11_P16		
A0	0.0021	0.0021		
B0	0.0018	0.0021		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P16	**C8T28SOI_LL_-HA1X9_P16**	**C8T28SOI_LL_-HA1X5_P16**	**C8T28SOI_LL_-HA1X9_P16**
A0 to CO ↓	0.0404	0.0347	3.5403	1.7461
A0 to CO ↑	0.0364	0.0323	5.3850	2.6008
A0 to S0 ↓	0.0520	0.0474	3.3815	1.7255
A0 to S0 ↑	0.0484	0.0445	5.2263	2.5868
B0 to CO ↓	0.0395	0.0338	3.5491	1.7461
B0 to CO ↑	0.0388	0.0348	5.3837	2.6016
B0 to S0 ↓	0.0536	0.0482	3.3819	1.7261
B0 to S0 ↑	0.0478	0.0437	5.2253	2.5874
	C8T28SOI_LLS1_-HA1X5_P16	**C8T28SOIDV_LL_-HA1X14_P16**	**C8T28SOI_LLS1_-HA1X5_P16**	**C8T28SOIDV_LL_-HA1X14_P16**
A0 to CO ↓	0.0327	0.0358	3.4608	1.1954
A0 to CO ↑	0.0292	0.0321	5.3172	1.7480
A0 to S0 ↓	0.0445	0.0523	3.4498	1.2055
A0 to S0 ↑	0.0489	0.0487	5.3412	1.7216
B0 to CO ↓	0.0311	0.0334	3.4584	1.1911
B0 to CO ↑	0.0309	0.0327	5.3167	1.7482
B0 to S0 ↓	0.0463	0.0513	3.4504	1.2053
B0 to S0 ↑	0.0481	0.0466	5.3429	1.7227
	C8T28SOIDV_LL_-HA1X19_P16	**C8T28SOIDV_-LLS1_HA1X11_P16**	**C8T28SOIDV_LL_-HA1X19_P16**	**C8T28SOIDV_-LLS1_HA1X11_P16**
A0 to CO ↓	0.0332	0.0316	0.8789	1.2504
A0 to CO ↑	0.0308	0.0313	1.3236	2.5494
A0 to S0 ↓	0.0482	0.0399	0.8724	1.2706
A0 to S0 ↑	0.0451	0.0414	1.2917	2.5676
B0 to CO ↓	0.0311	0.0298	0.8763	1.2491
B0 to CO ↑	0.0318	0.0335	1.3235	2.5493
B0 to S0 ↓	0.0481	0.0415	0.8724	1.2704
B0 to S0 ↑	0.0433	0.0414	1.2918	2.5662

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_HA1X5_P16	2.412e-07	1.000e-20
C8T28SOI_LL_HA1X9_P16	4.900e-07	1.000e-20
C8T28SOI_LLS1_HA1X5_P16	2.951e-07	1.000e-20
C8T28SOIDV_LL_HA1X14_P16	7.016e-07	1.000e-20
C8T28SOIDV_LL_HA1X19_P16	9.582e-07	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P16	6.938e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

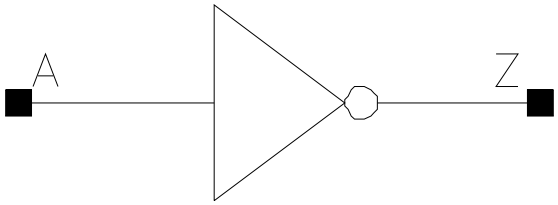
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P16	C8T28SOI_LL_-HA1X9_P16	C8T28SOI_LLS1_-HA1X5_P16	C8T28SOIDV_LL_-HA1X14_P16
A0 to CO	2.044e-03	3.315e-03	2.458e-03	5.348e-03
A0 to S0	1.828e-03	3.133e-03	2.159e-03	5.259e-03
B0 to CO	2.040e-03	3.307e-03	2.444e-03	5.131e-03
B0 to S0	1.781e-03	2.987e-03	2.074e-03	4.994e-03
	C8T28SOIDV_LL_-HA1X19_P16	C8T28SOIDV_LLS1_-HA1X11_P16		
A0 to CO	6.387e-03	4.488e-03		
A0 to S0	6.299e-03	4.048e-03		

B0 to CO	6.194e-03	4.335e-03		
B0 to S0	6.030e-03	4.315e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P16	C8T28SOI_LL_-HA1X9_P16	C8T28SOI_LLS1_-HA1X5_P16	C8T28SOIDV_LL_-HA1X14_P16
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P16	C8T28SOIDV_LLS1_-HA1X11_P16		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P16	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P16	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P16	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P16	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P16	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P16	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P16	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P16	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P16	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P16	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P16	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P16	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P16	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P16	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P16	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P16	C8T28SOI_LL_IVX3_-P16	C8T28SOI_LL_IVX5_-P16	C8T28SOI_LL_-IVX10_P16

A	0.0004	0.0005	0.0006	0.0011
	C8T28SOI_LL_-IVX14_P16	C8T28SOI_LL_-IVX19_P16	C8T28SOI_LL_-IVX29_P16	C8T28SOI_LL_-IVX34_P16
A	0.0017	0.0022	0.0033	0.0039
	C8T28SOI_LL_-IVX38_P16	C8T28SOIDV_LL_-IVX11_P16	C8T28SOIDV_LL_-IVX23_P16	C8T28SOIDV_LL_-IVX34_P16
A	0.0044	0.0013	0.0024	0.0036
	C8T28SOIDV_LL_-IVX46_P16	C8T28SOIDV_LL_-IVX68_P16	C8T28SOIDV_LL_-IVX91_P16	
A	0.0048	0.0073	0.0101	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P16	**C8T28SOI_LL_-IVX3_P16**	**C8T28SOI_LL_-IVX2_P16**	**C8T28SOI_LL_-IVX3_P16**
A to Z ↓	0.0092	0.0087	6.4845	5.0716
A to Z ↑	0.0153	0.0139	10.6096	7.9290
	C8T28SOI_LL_-IVX5_P16	**C8T28SOI_LL_-IVX10_P16**	**C8T28SOI_LL_-IVX5_P16**	**C8T28SOI_LL_-IVX10_P16**
A to Z ↓	0.0079	0.0064	3.5262	1.6977
A to Z ↑	0.0123	0.0104	5.4302	2.5795
	C8T28SOI_LL_-IVX14_P16	**C8T28SOI_LL_-IVX19_P16**	**C8T28SOI_LL_-IVX14_P16**	**C8T28SOI_LL_-IVX19_P16**
A to Z ↓	0.0066	0.0070	1.1833	0.9042
A to Z ↑	0.0104	0.0108	1.7324	1.3294
	C8T28SOI_LL_-IVX29_P16	**C8T28SOI_LL_-IVX34_P16**	**C8T28SOI_LL_-IVX29_P16**	**C8T28SOI_LL_-IVX34_P16**
A to Z ↓	0.0070	0.0065	0.6058	0.5160
A to Z ↑	0.0105	0.0100	0.8812	0.7523
	C8T28SOI_LL_-IVX38_P16	**C8T28SOIDV_LL_-IVX11_P16**	**C8T28SOI_LL_-IVX38_P16**	**C8T28SOIDV_LL_-IVX11_P16**
A to Z ↓	0.0068	0.0065	0.4579	1.3541
A to Z ↑	0.0102	0.0118	0.6669	2.6211
	C8T28SOIDV_LL_-IVX23_P16	**C8T28SOIDV_LL_-IVX34_P16**	**C8T28SOIDV_LL_-IVX23_P16**	**C8T28SOIDV_LL_-IVX34_P16**
A to Z ↓	0.0056	0.0060	0.6605	0.4539
A to Z ↑	0.0106	0.0108	1.2774	0.8567
	C8T28SOIDV_LL_-IVX46_P16	**C8T28SOIDV_LL_-IVX68_P16**	**C8T28SOIDV_LL_-IVX46_P16**	**C8T28SOIDV_LL_-IVX68_P16**
A to Z ↓	0.0059	0.0059	0.3417	0.2329
A to Z ↑	0.0104	0.0103	0.6424	0.4315
	C8T28SOIDV_LL_-IVX91_P16		**C8T28SOIDV_LL_-IVX91_P16**	
A to Z ↓	0.0064		0.1805	
A to Z ↑	0.0106		0.3278	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_IVX2_P16	3.434e-08	1.000e-20
C8T28SOI_LL_IVX3_P16	4.598e-08	1.000e-20
C8T28SOI_LL_IVX5_P16	6.874e-08	1.000e-20
C8T28SOI_LL_IVX10_P16	1.418e-07	1.000e-20

C8T28SOI_LL_IVX14_P16	2.032e-07	1.000e-20
C8T28SOI_LL_IVX19_P16	2.633e-07	1.000e-20
C8T28SOI_LL_IVX29_P16	3.835e-07	1.000e-20
C8T28SOI_LL_IVX34_P16	4.438e-07	1.000e-20
C8T28SOI_LL_IVX38_P16	5.040e-07	1.000e-20
C8T28SOIDV_LL_IVX11_P16	1.674e-07	1.000e-20
C8T28SOIDV_LL_IVX23_P16	3.330e-07	1.000e-20
C8T28SOIDV_LL_IVX34_P16	4.767e-07	1.000e-20
C8T28SOIDV_LL_IVX46_P16	6.169e-07	1.000e-20
C8T28SOIDV_LL_IVX68_P16	8.971e-07	1.000e-20
C8T28SOIDV_LL_IVX91_P16	1.178e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P16	C8T28SOI_LL_IVX3_-P16	C8T28SOI_LL_IVX5_-P16	C8T28SOI_LL_-IVX10_P16
A to Z	3.037e-04	3.587e-04	4.291e-04	7.201e-04
	C8T28SOI_LL_-IVX14_P16	C8T28SOI_LL_-IVX19_P16	C8T28SOI_LL_-IVX29_P16	C8T28SOI_LL_-IVX34_P16
A to Z	1.127e-03	1.561e-03	2.236e-03	2.440e-03
	C8T28SOI_LL_-IVX38_P16	C8T28SOIDV_LL_-IVX11_P16	C8T28SOIDV_LL_-IVX23_P16	C8T28SOIDV_LL_-IVX34_P16
A to Z	2.873e-03	9.052e-04	1.539e-03	2.412e-03
	C8T28SOIDV_LL_-IVX46_P16	C8T28SOIDV_LL_-IVX68_P16	C8T28SOIDV_LL_-IVX91_P16	
A to Z	2.962e-03	4.406e-03	5.903e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

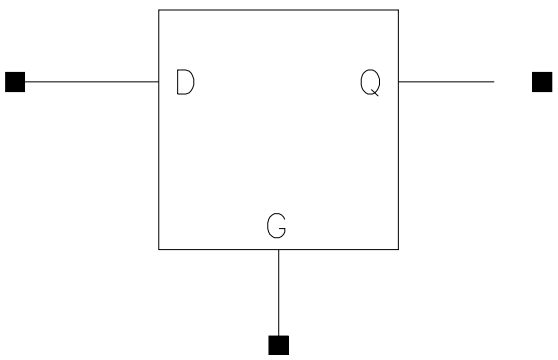
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P16	C8T28SOI_LL_IVX3_-P16	C8T28SOI_LL_IVX5_-P16	C8T28SOI_LL_-IVX10_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P16	C8T28SOI_LL_-IVX19_P16	C8T28SOI_LL_-IVX29_P16	C8T28SOI_LL_-IVX34_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P16	C8T28SOIDV_LL_-IVX11_P16	C8T28SOIDV_LL_-IVX23_P16	C8T28SOIDV_LL_-IVX34_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P16	C8T28SOIDV_LL_-IVX68_P16	C8T28SOIDV_LL_-IVX91_P16	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.360	1.0880
X9_P16	1.600	0.952	1.5232
X19_P16	1.600	1.224	1.9584
X28_P16	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16	X28_P16
D	0.0004	0.0007	0.0010	0.0017
G	0.0009	0.0009	0.0019	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D to Q ↓	0.0589	0.0556	3.6583	1.8574
D to Q ↑	0.0329	0.0386	5.2018	2.5492
G to Q ↓	0.0627	0.0579	3.6559	1.8551

G to Q ↑	0.0321	0.0361	5.2128	2.5509
	X19_P16	**X28_P16**	**X19_P16**	**X28_P16**
D to Q ↓	0.0457	0.0482	0.8866	0.5978
D to Q ↑	0.0333	0.0337	1.2810	0.8612
G to Q ↓	0.0504	0.0462	0.8858	0.5963
G to Q ↑	0.0311	0.0313	1.2822	0.8615

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P16	X9_P16	X19_P16	X28_P16
D ↓	hold_falling to G	-0.0139	-0.0143	-0.0045	-0.0094
D ↑	hold_falling to G	-0.0003	-0.0052	-0.0003	0.0003
D ↓	setup_falling to G	0.0537	0.0543	0.0391	0.0440
D ↑	setup_falling to G	0.0351	0.0399	0.0373	0.0373
G ↑	min_pulse_width to G	0.0504	0.0456	0.0440	0.0427

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.059e-07	1.000e-20
X9_P16	3.082e-07	1.000e-20
X19_P16	5.143e-07	1.000e-20
X28_P16	6.933e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	1.119e-05	5.386e-05	3.476e-05	1.031e-04
G (output stable)	7.833e-04	9.287e-04	1.530e-03	1.345e-03
D to Q	2.995e-03	4.676e-03	6.981e-03	1.027e-02
G to Q	2.719e-03	4.247e-03	6.248e-03	8.653e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

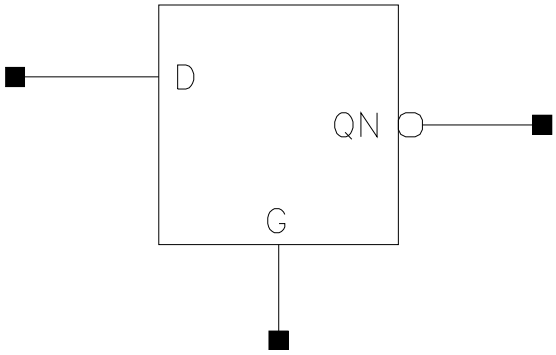
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P16
D	0.0004
G	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P16	X10_P16
D to QN ↓	0.0508	1.6714
D to QN ↑	0.0686	2.5318
G to QN ↓	0.0497	1.6698
G to QN ↑	0.0717	2.5283

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X10_P16
D ↓	hold_falling to G	-0.0240
D ↑	hold_falling to G	-0.0052
D ↓	setup_falling to G	0.0489
D ↑	setup_falling to G	0.0334
G ↑	min_pulse_width to G	0.0456

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P16	2.910e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X10_P16
D (output stable)	1.931e-05
G (output stable)	8.210e-04
D to QN	4.092e-03
G to QN	3.731e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

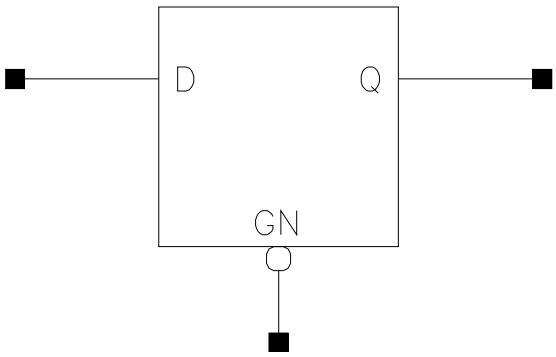
Pin Cycle (vdds)	X10_P16
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.360	1.0880
X9_P16	1.600	0.952	1.5232
X19_P16	1.600	1.224	1.9584
X28_P16	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16	X28_P16
D	0.0004	0.0007	0.0010	0.0015
GN	0.0009	0.0010	0.0014	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D to Q ↓	0.0594	0.0546	3.6691	1.8659
D to Q ↑	0.0332	0.0381	5.2023	2.5537
GN to Q ↓	0.0528	0.0515	3.6699	1.8661

GN to Q ↑	0.0563	0.0535	5.2009	2.5455
	X19_P16	**X28_P16**	**X19_P16**	**X28_P16**
D to Q ↓	0.0462	0.0461	0.8839	0.5956
D to Q ↑	0.0351	0.0344	1.2765	0.8533
GN to Q ↓	0.0413	0.0396	0.8845	0.5958
GN to Q ↑	0.0478	0.0475	1.2743	0.8524

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P16	X9_P16	X19_P16	X28_P16
D ↓	hold_rising to GN	-0.0220	-0.0171	-0.0123	-0.0123
D ↑	hold_rising to GN	0.0027	-0.0022	0.0036	0.0032
D ↓	setup_rising to GN	0.0640	0.0569	0.0521	0.0526
D ↑	setup_rising to GN	0.0261	0.0367	0.0313	0.0319
GN ↓	min_pulse_width to GN	0.0678	0.0634	0.0558	0.0513

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.048e-07	1.000e-20
X9_P16	3.070e-07	1.000e-20
X19_P16	5.249e-07	1.000e-20
X28_P16	6.879e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	1.206e-05	2.161e-05	4.120e-05	1.017e-04
GN (output stable)	7.838e-04	9.001e-04	1.274e-03	1.339e-03
D to Q	2.988e-03	4.683e-03	7.198e-03	9.937e-03
GN to Q	4.530e-03	6.367e-03	9.314e-03	1.186e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

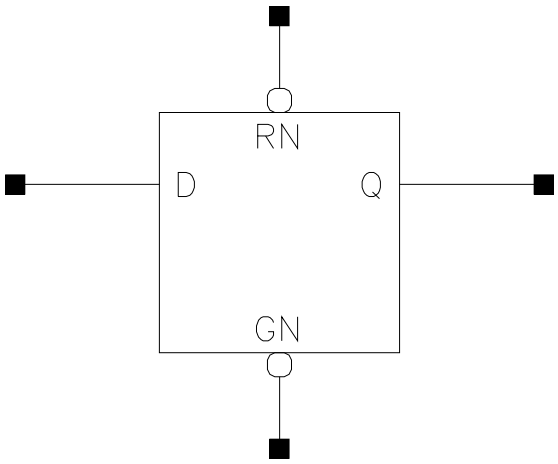
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.632	1.3056
X9_P16	1.600	1.224	1.9584
X19_P16	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16
D	0.0004	0.0006	0.0012
GN	0.0011	0.0011	0.0015
RN	0.0005	0.0005	0.0005

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D to Q ↓	0.0601	0.0572	3.5900	1.8077

D to Q ↑	0.0525	0.0577	5.4247	2.6538
GN to Q ↓	0.0550	0.0528	3.5951	1.8078
GN to Q ↑	0.0720	0.0683	5.4247	2.6602
RN to Q ↓	0.0485	0.0609	3.4388	1.8070
RN to Q ↑	0.0572	0.0617	5.4200	2.6546
	X19_P16		**X19_P16**	
D to Q ↓	0.0481		0.8891	
D to Q ↑	0.0617		1.3441	
GN to Q ↓	0.0434		0.8898	
GN to Q ↑	0.0651		1.3480	
RN to Q ↓	0.0786		0.9670	
RN to Q ↑	0.0671		1.3447	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P16	X9_P16	X19_P16
D ↓	hold_rising to GN	-0.0220	-0.0162	-0.0117
D ↑	hold_rising to GN	-0.0120	-0.0164	-0.0208
D ↓	setup_rising to GN	0.0663	0.0614	0.0517
D ↑	setup_rising to GN	0.0540	0.0588	0.0659
GN ↓	min_pulse_width to GN	0.0725	0.0695	0.0669
RN ↓	min_pulse_width to RN	0.0610	0.0708	0.0925
RN ↑	recovery_rising to GN	0.0590	0.0660	0.0729
RN ↑	removal_rising to GN	-0.0369	-0.0413	-0.0484

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.112e-07	1.000e-20
X9_P16	3.071e-07	1.000e-20
X19_P16	5.073e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16
D (output stable)	6.880e-05	5.805e-05	7.941e-05
GN (output stable)	8.933e-04	8.431e-04	1.064e-03
RN (output stable)	2.403e-05	2.283e-05	2.409e-05
D to Q	3.649e-03	5.119e-03	7.738e-03
GN to Q	5.308e-03	6.727e-03	9.625e-03
RN to Q	2.905e-03	3.998e-03	6.054e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

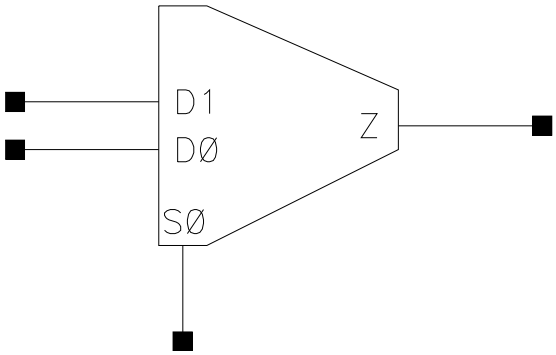
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.360	1.0880
X9_P16	0.800	1.496	1.1968
X14_P16	0.800	2.176	1.7408
X19_P16	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P16	X9_P16	X14_P16	X19_P16
D0	0.0006	0.0008	0.0010	0.0014
D1	0.0005	0.0008	0.0010	0.0014
S0	0.0011	0.0010	0.0013	0.0016

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D0 to Z ↓	0.0435	0.0407	3.5680	1.8131
D0 to Z ↑	0.0337	0.0332	5.3299	2.7155
D1 to Z ↓	0.0442	0.0399	3.5652	1.8086
D1 to Z ↑	0.0332	0.0314	5.3397	2.7121
S0 to Z ↓	0.0413	0.0362	3.5591	1.8073
S0 to Z ↑	0.0385	0.0355	5.3327	2.7123

	X14_P16	X19_P16	X14_P16	X19_P16
D0 to Z ↓	0.0442	0.0389	1.2573	0.9059
D0 to Z ↑	0.0352	0.0324	1.8391	1.3280
D1 to Z ↓	0.0452	0.0403	1.2573	0.9066
D1 to Z ↑	0.0334	0.0313	1.8345	1.3291
S0 to Z ↓	0.0426	0.0393	1.2531	0.9042
S0 to Z ↑	0.0411	0.0374	1.8366	1.3283

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.206e-07	1.000e-20
X9_P16	3.534e-07	1.000e-20
X14_P16	4.836e-07	1.000e-20
X19_P16	6.933e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X9_P16	X14_P16	X19_P16
D0 (output stable)	5.010e-04	9.347e-04	1.049e-03	1.249e-03
D1 (output stable)	4.761e-04	7.744e-04	1.103e-03	1.350e-03
S0 (output stable)	8.405e-04	7.602e-04	1.247e-03	1.452e-03
D0 to Z	2.214e-03	3.407e-03	5.409e-03	6.568e-03
D1 to Z	2.152e-03	3.196e-03	5.253e-03	6.506e-03
S0 to Z	2.702e-03	3.362e-03	5.965e-03	7.160e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

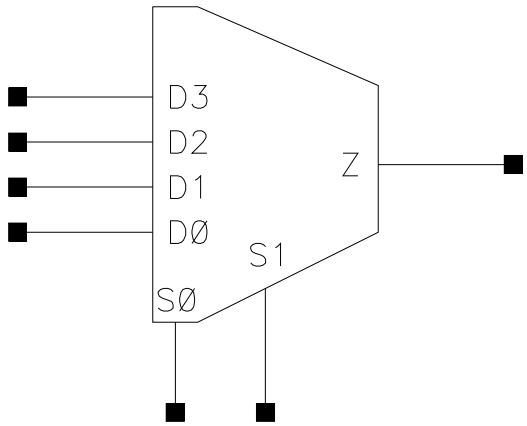
Pin Cycle (vdds)	X5_P16	X9_P16	X14_P16	X19_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.600	1.496	2.3936
X9_P16	1.600	1.768	2.8288
X13_P16	1.600	2.312	3.6992
X18_P16	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P16	X9_P16	X13_P16	X18_P16
D0	0.0005	0.0007	0.0010	0.0010
D1	0.0004	0.0006	0.0011	0.0010
D2	0.0004	0.0007	0.0010	0.0010
D3	0.0004	0.0006	0.0010	0.0010
S0	0.0014	0.0018	0.0025	0.0025
S1	0.0008	0.0010	0.0014	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X9_P16	X4_P16	X9_P16
D0 to Z ↓	0.0939	0.0786	3.9266	1.9256
D0 to Z ↑	0.0562	0.0518	5.5051	2.7291
D1 to Z ↓	0.0928	0.0783	3.9214	1.9269
D1 to Z ↑	0.0563	0.0516	5.4953	2.7288
D2 to Z ↓	0.0864	0.0794	3.8658	1.9309
D2 to Z ↑	0.0545	0.0514	5.4698	2.7269
D3 to Z ↓	0.0875	0.0783	3.8734	1.9302
D3 to Z ↑	0.0553	0.0514	5.4724	2.7264
S0 to Z ↓	0.0977	0.0872	3.8941	1.9261
S0 to Z ↑	0.0676	0.0654	5.4995	2.7330
S1 to Z ↓	0.0603	0.0581	3.8911	1.9274
S1 to Z ↑	0.0467	0.0472	5.4719	2.7255
	X13_P16	X18_P16	X13_P16	X18_P16
D0 to Z ↓	0.0768	0.0836	1.3474	1.0113
D0 to Z ↑	0.0470	0.0507	1.8255	1.3834
D1 to Z ↓	0.0771	0.0840	1.3478	1.0111
D1 to Z ↑	0.0483	0.0521	1.8261	1.3836
D2 to Z ↓	0.0704	0.0765	1.3253	0.9931
D2 to Z ↑	0.0468	0.0506	1.8207	1.3807
D3 to Z ↓	0.0700	0.0761	1.3242	0.9924
D3 to Z ↑	0.0471	0.0508	1.8189	1.3797
S0 to Z ↓	0.0820	0.0885	1.3352	1.0013
S0 to Z ↑	0.0602	0.0640	1.8252	1.3831
S1 to Z ↓	0.0554	0.0619	1.3354	1.0014
S1 to Z ↑	0.0434	0.0471	1.8216	1.3810

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	2.817e-07	1.000e-20
X9_P16	4.355e-07	1.000e-20
X13_P16	7.570e-07	1.000e-20
X18_P16	8.240e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X9_P16	X13_P16	X18_P16
D0 (output stable)	9.679e-05	1.038e-04	1.887e-04	1.869e-04
D1 (output stable)	9.535e-05	1.196e-04	1.729e-04	1.713e-04
D2 (output stable)	4.376e-05	4.470e-05	6.099e-05	6.088e-05
D3 (output stable)	6.506e-05	9.690e-05	1.256e-04	1.257e-04
S0 (output stable)	1.317e-03	1.638e-03	2.670e-03	2.669e-03
S1 (output stable)	8.674e-04	9.869e-04	1.582e-03	1.580e-03
D0 to Z	2.770e-03	4.017e-03	6.617e-03	7.877e-03
D1 to Z	2.746e-03	4.014e-03	6.690e-03	7.949e-03
D2 to Z	2.606e-03	4.001e-03	6.381e-03	7.606e-03
D3 to Z	2.637e-03	3.996e-03	6.400e-03	7.623e-03
S0 to Z	4.144e-03	5.844e-03	9.483e-03	1.073e-02
S1 to Z	2.580e-03	3.790e-03	6.130e-03	7.352e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

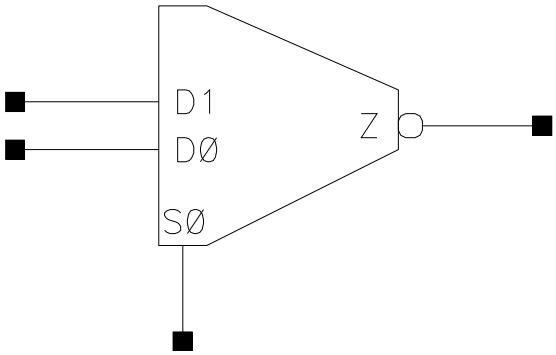
Pin Cycle (vdds)	X4_P16	X9_P16	X13_P16	X18_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P16	0.800	0.952	0.7616
X2_P16	0.800	0.952	0.7616
X6_P16	0.800	1.904	1.5232
X9_P16	0.800	2.448	1.9584
X12_P16	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P16	X2_P16	X6_P16	X9_P16
D0	0.0004	0.0006	0.0012	0.0018
D1	0.0004	0.0005	0.0012	0.0018
S0	0.0010	0.0014	0.0020	0.0029
	X12_P16			
D0	0.0024			
D1	0.0023			
S0	0.0033			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P16	X2_P16	X1_P16	X2_P16
D0 to Z ↓	0.0151	0.0147	9.8898	6.7478

D0 to Z ↑	0.0293	0.0231	22.8732	12.1460
D1 to Z ↓	0.0145	0.0137	9.7550	6.6076
D1 to Z ↑	0.0297	0.0243	22.8757	12.3221
S0 to Z ↓	0.0266	0.0186	9.7834	6.6719
S0 to Z ↑	0.0300	0.0199	22.7881	12.2358
	X6_P16	**X9_P16**	**X6_P16**	**X9_P16**
D0 to Z ↓	0.0163	0.0152	3.0472	2.0482
D0 to Z ↑	0.0243	0.0233	5.0291	3.5105
D1 to Z ↓	0.0156	0.0151	2.9787	2.0622
D1 to Z ↑	0.0258	0.0241	5.2042	3.4300
S0 to Z ↓	0.0222	0.0191	3.0108	2.0561
S0 to Z ↑	0.0229	0.0202	5.1136	3.4739
	X12_P16		**X12_P16**	
D0 to Z ↓	0.0158		1.5696	
D0 to Z ↑	0.0233		2.6491	
D1 to Z ↓	0.0150		1.5630	
D1 to Z ↑	0.0239		2.5804	
S0 to Z ↓	0.0208		1.5663	
S0 to Z ↑	0.0216		2.6156	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X1_P16	1.008e-07	1.000e-20
X2_P16	1.739e-07	1.000e-20
X6_P16	3.525e-07	1.000e-20
X9_P16	5.442e-07	1.000e-20
X12_P16	6.701e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X1_P16	X2_P16	X6_P16	X9_P16
D0 (output stable)	1.244e-05	2.544e-05	9.793e-05	1.514e-04
D1 (output stable)	1.808e-05	1.241e-04	1.502e-04	2.023e-04
S0 (output stable)	8.233e-04	8.746e-04	1.619e-03	2.380e-03
D0 to Z	7.335e-04	9.598e-04	2.551e-03	3.448e-03
D1 to Z	7.292e-04	9.559e-04	2.564e-03	3.530e-03
S0 to Z	1.407e-03	1.399e-03	3.072e-03	4.234e-03
	X12_P16			
D0 (output stable)	1.827e-04			
D1 (output stable)	2.227e-04			
S0 (output stable)	2.890e-03			
D0 to Z	4.669e-03			
D1 to Z	4.628e-03			
S0 to Z	5.461e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X1_P16	X2_P16	X6_P16	X9_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

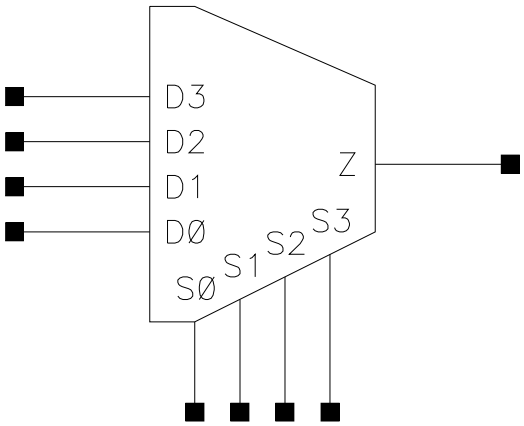
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P16			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.600	0.952	1.5232
X15_P16	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P16	X15_P16
D0	0.0006	0.0015
D1	0.0006	0.0013
D2	0.0006	0.0015
D3	0.0006	0.0013
S0	0.0006	0.0014
S1	0.0006	0.0015
S2	0.0006	0.0014
S3	0.0007	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X15_P16	X4_P16	X15_P16
D0 to Z ↓	0.0485	0.0521	5.7963	1.5337
D0 to Z ↑	0.0393	0.0384	5.0111	1.2696
D1 to Z ↓	0.0444	0.0470	5.7942	1.5327
D1 to Z ↑	0.0341	0.0339	4.9881	1.2637
D2 to Z ↓	0.0471	0.0499	5.8111	1.5369
D2 to Z ↑	0.0381	0.0362	5.0350	1.2775
D3 to Z ↓	0.0425	0.0450	5.8035	1.5349
D3 to Z ↑	0.0329	0.0320	5.0104	1.2719
S0 to Z ↓	0.0462	0.0477	5.7944	1.5327
S0 to Z ↑	0.0417	0.0389	5.0125	1.2688
S1 to Z ↓	0.0416	0.0431	5.7927	1.5319
S1 to Z ↑	0.0360	0.0343	4.9904	1.2635
S2 to Z ↓	0.0454	0.0460	5.8094	1.5355
S2 to Z ↑	0.0406	0.0370	5.0357	1.2769
S3 to Z ↓	0.0412	0.0412	5.8029	1.5334
S3 to Z ↑	0.0354	0.0322	5.0124	1.2707

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	3.125e-07	1.000e-20
X15_P16	9.159e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X15_P16
D0 (output stable)	4.293e-04	1.222e-03
D1 (output stable)	3.081e-04	8.937e-04
D2 (output stable)	4.431e-04	1.225e-03
D3 (output stable)	3.123e-04	8.645e-04
S0 (output stable)	4.300e-04	1.215e-03
S1 (output stable)	3.040e-04	8.850e-04
S2 (output stable)	4.100e-04	1.100e-03
S3 (output stable)	2.941e-04	7.941e-04
D0 to Z	3.133e-03	8.920e-03
D1 to Z	2.626e-03	7.559e-03
D2 to Z	2.835e-03	7.754e-03
D3 to Z	2.338e-03	6.413e-03
S0 to Z	3.000e-03	8.279e-03
S1 to Z	2.502e-03	6.968e-03
S2 to Z	2.727e-03	7.175e-03
S3 to Z	2.238e-03	5.825e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

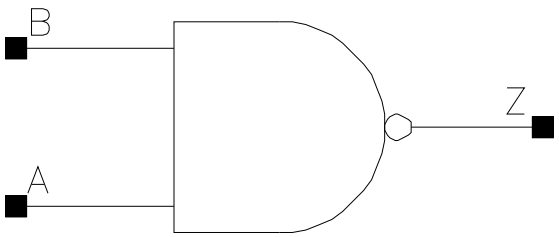
Pin Cycle (vdds)	X4_P16	X15_P16
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P16	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P16	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P16	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P16	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P16	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P16	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P16	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P16	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P16	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P16	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P16	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P16	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P16	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P16	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P16	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P16	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P16	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P16	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P16	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P16	C8T28SOI_LL_-NAND2X4_P16	C8T28SOI_LL_-NAND2X8_P16	C8T28SOI_LL_-NAND2X12_P16
A	0.0004	0.0006	0.0012	0.0017
B	0.0004	0.0006	0.0011	0.0016
	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X24_P16	C8T28SOI_-LLBR0P8_-NAND2X4_P16
A	0.0023	0.0028	0.0008	0.0007
B	0.0021	0.0026	0.0007	0.0006
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	C8T28SOI_-LLBR0P8_-NAND2X12_P16	C8T28SOI_-LLBR0P8_-NAND2X16_P16	C8T28SOI_LLS_-NAND2X8_P16
A	0.0012	0.0018	0.0023	0.0012
B	0.0011	0.0016	0.0021	0.0011
	C8T28SOI_LLS_-NAND2X15_P16	C8T28SOI_LLS_-NAND2X23_P16	C8T28SOI_LLS_-NAND2X31_P16	C8T28SOIDV_LL_-NAND2X9_P16
A	0.0023	0.0035	0.0047	0.0012
B	0.0022	0.0032	0.0043	0.0013
	C8T28SOIDV_LL_-NAND2X18_P16	C8T28SOIDV_LL_-NAND2X27_P16	C8T28SOIDV_LL_-NAND2X36_P16	
A	0.0025	0.0037	0.0050	
B	0.0023	0.0035	0.0046	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND2X2_P16	**C8T28SOI_LL_-NAND2X4_P16**	**C8T28SOI_LL_-NAND2X2_P16**	**C8T28SOI_LL_-NAND2X4_P16**
A to Z ↓	0.0117	0.0103	10.6040	5.8557
A to Z ↑	0.0180	0.0151	10.5280	5.4186
B to Z ↓	0.0131	0.0109	10.7153	5.9192
B to Z ↑	0.0164	0.0131	10.5927	5.4865
	C8T28SOI_LL_-NAND2X8_P16	**C8T28SOI_LL_-NAND2X12_P16**	**C8T28SOI_LL_-NAND2X8_P16**	**C8T28SOI_LL_-NAND2X12_P16**
A to Z ↓	0.0117	0.0112	2.9869	2.0478
A to Z ↑	0.0153	0.0150	2.5737	1.7569
B to Z ↓	0.0101	0.0107	3.0264	2.0731
B to Z ↑	0.0117	0.0121	2.5976	1.7835

	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16
A to Z ↓	0.0115	0.0112	1.5516	1.2548
A to Z ↑	0.0150	0.0150	1.3219	1.0710
B to Z ↓	0.0102	0.0107	1.5740	1.2719
B to Z ↑	0.0116	0.0119	1.3406	1.0872
	C8T28SOI_LL_-NAND2X24_P16	**C8T28SOI_-LLBR0P8_-NAND2X4_P16**	**C8T28SOI_LL_-NAND2X24_P16**	**C8T28SOI_-LLBR0P8_-NAND2X4_P16**
A to Z ↓	0.0416	0.0090	0.7003	4.1480
A to Z ↑	0.0427	0.0189	1.0496	6.9217
B to Z ↓	0.0429	0.0090	0.7011	4.2230
B to Z ↑	0.0408	0.0156	1.0495	6.9745
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	**C8T28SOI_-LLBR0P8_-NAND2X12_P16**	**C8T28SOI_-LLBR0P8_-NAND2X8_P16**	**C8T28SOI_-LLBR0P8_-NAND2X12_P16**
A to Z ↓	0.0101	0.0099	2.2868	1.5669
A to Z ↑	0.0189	0.0190	3.4816	2.3569
B to Z ↓	0.0079	0.0087	2.3337	1.5982
B to Z ↑	0.0136	0.0143	3.5146	2.3775
	C8T28SOI_-LLBR0P8_-NAND2X16_P16	**C8T28SOI_LLS_-NAND2X8_P16**	**C8T28SOI_-LLBR0P8_-NAND2X16_P16**	**C8T28SOI_LLS_-NAND2X8_P16**
A to Z ↓	0.0098	0.0117	1.1967	2.9753
A to Z ↑	0.0184	0.0154	1.7614	2.6098
B to Z ↓	0.0077	0.0101	1.2221	3.0149
B to Z ↑	0.0131	0.0118	1.7819	2.6461
	C8T28SOI_LLS_-NAND2X15_P16	**C8T28SOI_LLS_-NAND2X23_P16**	**C8T28SOI_LLS_-NAND2X15_P16**	**C8T28SOI_LLS_-NAND2X23_P16**
A to Z ↓	0.0116	0.0116	1.5470	1.0448
A to Z ↑	0.0150	0.0149	1.2990	0.8665
B to Z ↓	0.0103	0.0105	1.5695	1.0595
B to Z ↑	0.0116	0.0116	1.3114	0.8742
	C8T28SOI_LLS_-NAND2X31_P16	**C8T28SOIDV_LL_-NAND2X9_P16**	**C8T28SOI_LLS_-NAND2X31_P16**	**C8T28SOIDV_LL_-NAND2X9_P16**
A to Z ↓	0.0115	0.0098	0.7913	2.2872
A to Z ↑	0.0149	0.0157	0.6523	2.5237
B to Z ↓	0.0106	0.0099	0.8023	2.3197
B to Z ↑	0.0117	0.0131	0.6580	2.5719
	C8T28SOIDV_LL_-NAND2X18_P16	**C8T28SOIDV_LL_-NAND2X27_P16**	**C8T28SOIDV_LL_-NAND2X18_P16**	**C8T28SOIDV_LL_-NAND2X27_P16**
A to Z ↓	0.0110	0.0107	1.1669	0.7960
A to Z ↑	0.0162	0.0161	1.2669	0.8549
B to Z ↓	0.0092	0.0100	1.1853	0.8087
B to Z ↑	0.0122	0.0128	1.2785	0.8618
	C8T28SOIDV_LL_-NAND2X36_P16		**C8T28SOIDV_LL_-NAND2X36_P16**	
A to Z ↓	0.0110		0.5995	
A to Z ↑	0.0161		0.6393	
B to Z ↓	0.0094		0.6096	
B to Z ↑	0.0122		0.6457	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P16	4.234e-08	1.000e-20
C8T28SOI_LL_NAND2X4_P16	8.402e-08	1.000e-20
C8T28SOI_LL_NAND2X8_P16	1.679e-07	1.000e-20
C8T28SOI_LL_NAND2X12_P16	2.444e-07	1.000e-20
C8T28SOI_LL_NAND2X15_P16	3.212e-07	1.000e-20
C8T28SOI_LL_NAND2X19_P16	3.980e-07	1.000e-20
C8T28SOI_LL_NAND2X24_P16	5.033e-07	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P16	9.627e-08	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P16	1.770e-07	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_-P16	2.561e-07	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_-P16	3.355e-07	1.000e-20
C8T28SOI_LLS_NAND2X8_P16	1.679e-07	1.000e-20
C8T28SOI_LLS_NAND2X15_P16	3.212e-07	1.000e-20
C8T28SOI_LLS_NAND2X23_P16	4.748e-07	1.000e-20
C8T28SOI_LLS_NAND2X31_P16	6.284e-07	1.000e-20
C8T28SOIDV_LL_NAND2X9_P16	2.031e-07	1.000e-20
C8T28SOIDV_LL_NAND2X18_P16	3.908e-07	1.000e-20
C8T28SOIDV_LL_NAND2X27_P16	5.689e-07	1.000e-20
C8T28SOIDV_LL_NAND2X36_P16	7.474e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P16	C8T28SOI_LL_-NAND2X4_P16	C8T28SOI_LL_-NAND2X8_P16	C8T28SOI_LL_-NAND2X12_P16
A (output stable)	6.163e-06	1.183e-05	4.084e-05	5.687e-05
B (output stable)	2.403e-05	4.386e-05	2.586e-04	2.846e-04
A to Z	4.441e-04	6.483e-04	1.470e-03	2.091e-03
B to Z	3.596e-04	4.918e-04	9.096e-04	1.426e-03
	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X24_P16	C8T28SOI_-LLBR0P8_-NAND2X4_P16
A (output stable)	7.790e-05	9.469e-05	1.348e-05	1.604e-05
B (output stable)	4.596e-04	4.621e-04	4.749e-05	6.203e-05
A to Z	2.820e-03	3.457e-03	7.322e-03	7.604e-04
B to Z	1.783e-03	2.340e-03	7.159e-03	5.317e-04
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	C8T28SOI_-LLBR0P8_-NAND2X12_P16	C8T28SOI_-LLBR0P8_-NAND2X16_P16	C8T28SOI_LLS_-NAND2X8_P16
A (output stable)	5.025e-05	6.395e-05	1.000e-04	4.169e-05
B (output stable)	3.173e-04	3.488e-04	5.617e-04	2.693e-04
A to Z	1.574e-03	2.336e-03	2.945e-03	1.480e-03
B to Z	8.526e-04	1.427e-03	1.603e-03	9.183e-04
	C8T28SOI_LLS_-NAND2X15_P16	C8T28SOI_LLS_-NAND2X23_P16	C8T28SOI_LLS_-NAND2X31_P16	C8T28SOIDV_LL_-NAND2X9_P16
A (output stable)	8.254e-05	1.242e-04	1.592e-04	2.928e-05
B (output stable)	4.717e-04	6.705e-04	8.369e-04	1.119e-04
A to Z	2.857e-03	4.250e-03	5.617e-03	1.540e-03
B to Z	1.810e-03	2.745e-03	3.680e-03	1.124e-03
	C8T28SOIDV_LL_-NAND2X18_P16	C8T28SOIDV_LL_-NAND2X27_P16	C8T28SOIDV_LL_-NAND2X36_P16	
A (output stable)	9.322e-05	1.261e-04	1.858e-04	

B (output stable)	6.001e-04	5.759e-04	1.177e-03	
A to Z	3.277e-03	4.826e-03	6.462e-03	
B to Z	1.992e-03	3.293e-03	3.973e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

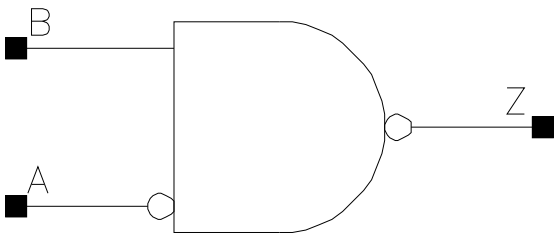
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P16	C8T28SOI_LL_-NAND2X4_P16	C8T28SOI_LL_-NAND2X8_P16	C8T28SOI_LL_-NAND2X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X24_P16	C8T28SOI_-LLBR0P8_-NAND2X4_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	C8T28SOI_-LLBR0P8_-NAND2X12_P16	C8T28SOI_-LLBR0P8_-NAND2X16_P16	C8T28SOI_LLS_-NAND2X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P16	C8T28SOI_LLS_-NAND2X23_P16	C8T28SOI_LLS_-NAND2X31_P16	C8T28SOIDV_LL_-NAND2X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P16	C8T28SOIDV_LL_-NAND2X27_P16	C8T28SOIDV_LL_-NAND2X36_P16	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.544	0.4352
X4_P16	0.800	0.680	0.5440
X9_P16	1.600	0.544	0.8704
X13_P16	1.600	0.816	1.3056
X17_P16	1.600	0.816	1.3056
X23_P16	0.800	2.312	1.8496
X27_P16	1.600	1.088	1.7408
X31_P16	0.800	2.992	2.3936
X36_P16	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P16	X4_P16	X9_P16	X13_P16
A	0.0006	0.0006	0.0010	0.0010
B	0.0004	0.0006	0.0012	0.0018
	X17_P16	X23_P16	X27_P16	X31_P16
A	0.0010	0.0021	0.0016	0.0028
B	0.0023	0.0032	0.0035	0.0041
	X36_P16			
A	0.0016			
B	0.0046			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X4_P16**	**X2_P16**	**X4_P16**
A to Z ↓	0.0305	0.0318	10.5875	5.9115
A to Z ↑	0.0240	0.0242	10.3030	5.2572
B to Z ↓	0.0134	0.0110	10.8427	6.0456
B to Z ↑	0.0165	0.0130	10.5967	5.4827
	X9_P16	**X13_P16**	**X9_P16**	**X13_P16**
A to Z ↓	0.0313	0.0379	2.3464	1.4843
A to Z ↑	0.0238	0.0286	2.4867	1.6863
B to Z ↓	0.0102	0.0101	2.4085	1.5214
B to Z ↑	0.0132	0.0136	2.5899	1.7808
	X17_P16	**X23_P16**	**X17_P16**	**X23_P16**
A to Z ↓	0.0414	0.0301	1.1768	1.0376
A to Z ↑	0.0299	0.0242	1.2748	0.8672
B to Z ↓	0.0097	0.0102	1.2019	1.0643
B to Z ↑	0.0128	0.0116	1.3488	0.9012
	X27_P16	**X31_P16**	**X27_P16**	**X31_P16**
A to Z ↓	0.0351	0.0299	0.7926	0.7849
A to Z ↑	0.0267	0.0239	0.8454	0.6320
B to Z ↓	0.0095	0.0104	0.8131	0.8043
B to Z ↑	0.0124	0.0117	0.8659	0.6776
	X36_P16		**X36_P16**	
A to Z ↓	0.0403		0.6004	
A to Z ↑	0.0303		0.6358	
B to Z ↓	0.0094		0.6130	
B to Z ↑	0.0121		0.6510	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P16	7.155e-08	1.000e-20
X4_P16	1.167e-07	1.000e-20
X9_P16	2.802e-07	1.000e-20
X13_P16	3.595e-07	1.000e-20
X17_P16	4.549e-07	1.000e-20
X23_P16	6.730e-07	1.000e-20
X27_P16	7.176e-07	1.000e-20
X31_P16	8.870e-07	1.000e-20
X36_P16	8.985e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P16	X4_P16	X9_P16	X13_P16
A (output stable)	6.871e-04	8.934e-04	1.737e-03	2.639e-03
B (output stable)	2.371e-05	4.326e-05	1.153e-04	2.823e-04
A to Z	1.171e-03	1.604e-03	3.451e-03	5.472e-03
B to Z	3.627e-04	4.883e-04	1.144e-03	1.757e-03
	X17_P16	X23_P16	X27_P16	X31_P16
A (output stable)	3.037e-03	4.566e-03	4.723e-03	6.033e-03
B (output stable)	3.447e-04	6.001e-04	5.905e-04	8.006e-04
A to Z	6.497e-03	9.135e-03	9.676e-03	1.214e-02
B to Z	2.123e-03	2.738e-03	3.066e-03	3.625e-03
	X36_P16			
A (output stable)	6.254e-03			

B (output stable)	8.884e-04			
A to Z	1.275e-02			
B to Z	3.916e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

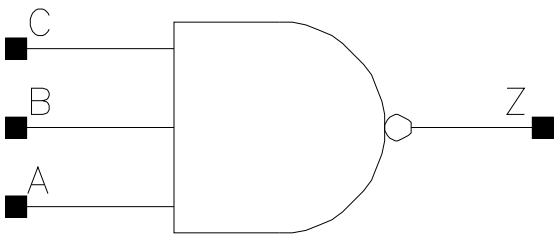
Pin Cycle (vdds)	X2_P16	X4_P16	X9_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P16	X23_P16	X27_P16	X31_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P16	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P16	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P16	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P16	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P16	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P16	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P16	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P16	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P16	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P16	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P16	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P16	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P16	C8T28SOI_LL_-NAND3X7_P16	C8T28SOI_LL_-NAND3X10_P16	C8T28SOI_LL_-NAND3X14_P16
A	0.0006	0.0012	0.0018	0.0023
B	0.0006	0.0011	0.0017	0.0022
C	0.0006	0.0011	0.0016	0.0021
	C8T28SOI_LL_-NAND3X20_P16	C8T28SOI_LL_-NAND3X27_P16	C8T28SOI_-LLBR0P6_-NAND3X3_P16	C8T28SOI_-LLBR0P6_-NAND3X7_P16
A	0.0035	0.0046	0.0007	0.0012
B	0.0033	0.0044	0.0006	0.0011
C	0.0031	0.0041	0.0006	0.0010
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	C8T28SOI_-LLBR0P6_-NAND3X14_P16	C8T28SOI_-LLBR0P6_-NAND3X20_P16	C8T28SOI_-LLBR0P6_-NAND3X27_P16
A	0.0018	0.0024	0.0035	0.0047
B	0.0016	0.0021	0.0032	0.0043
C	0.0016	0.0021	0.0031	0.0041

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-NAND3X3_P16	**C8T28SOI_LL_-NAND3X7_P16**	**C8T28SOI_LL_-NAND3X3_P16**	**C8T28SOI_LL_-NAND3X7_P16**
A to Z ↓	0.0151	0.0173	8.5355	4.3167
A to Z ↑	0.0187	0.0193	5.4684	2.6741
B to Z ↓	0.0154	0.0166	8.5652	4.3328
B to Z ↑	0.0171	0.0175	5.4950	2.6804
C to Z ↓	0.0155	0.0146	8.6150	4.3577
C to Z ↑	0.0152	0.0142	5.5373	2.5965
	C8T28SOI_LL_-NAND3X10_P16	**C8T28SOI_LL_-NAND3X14_P16**	**C8T28SOI_LL_-NAND3X10_P16**	**C8T28SOI_LL_-NAND3X14_P16**
A to Z ↓	0.0165	0.0170	2.9810	2.2517
A to Z ↑	0.0182	0.0187	1.7193	1.3464
B to Z ↓	0.0164	0.0162	2.9924	2.2604
B to Z ↑	0.0167	0.0168	1.7775	1.3462
C to Z ↓	0.0147	0.0145	3.0117	2.2740
C to Z ↑	0.0139	0.0138	1.7923	1.3336
	C8T28SOI_LL_-NAND3X20_P16	**C8T28SOI_LL_-NAND3X27_P16**	**C8T28SOI_LL_-NAND3X20_P16**	**C8T28SOI_LL_-NAND3X27_P16**
A to Z ↓	0.0165	0.0166	1.5318	1.1654
A to Z ↑	0.0180	0.0180	0.8657	0.6529
B to Z ↓	0.0163	0.0163	1.5376	1.1698
B to Z ↑	0.0163	0.0163	0.8660	0.6518
C to Z ↓	0.0144	0.0146	1.5476	1.1771
C to Z ↑	0.0134	0.0135	0.8930	0.6727
	C8T28SOI_-LLBR0P6_-NAND3X3_P16	**C8T28SOI_-LLBR0P6_-NAND3X7_P16**	**C8T28SOI_-LLBR0P6_-NAND3X3_P16**	**C8T28SOI_-LLBR0P6_-NAND3X7_P16**
A to Z ↓	0.0119	0.0145	5.3737	3.0240
A to Z ↑	0.0258	0.0276	8.2328	4.1992
B to Z ↓	0.0114	0.0132	5.4289	3.0444
B to Z ↑	0.0224	0.0237	8.2537	4.2120

C to Z ↓	0.0107	0.0106	5.5027	3.0814
C to Z ↑	0.0183	0.0178	8.3242	4.1772
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	**C8T28SOI_-LLBR0P6_-NAND3X14_P16**	**C8T28SOI_-LLBR0P6_-NAND3X10_P16**	**C8T28SOI_-LLBR0P6_-NAND3X14_P16**
A to Z ↓	0.0133	0.0141	2.0222	1.5355
A to Z ↑	0.0262	0.0268	2.7974	2.1193
B to Z ↓	0.0123	0.0126	2.0396	1.5476
B to Z ↑	0.0222	0.0226	2.8112	2.1225
C to Z ↓	0.0102	0.0098	2.0665	1.5698
C to Z ↑	0.0169	0.0166	2.8372	2.1208
	C8T28SOI_-LLBR0P6_-NAND3X20_P16	**C8T28SOI_-LLBR0P6_-NAND3X27_P16**	**C8T28SOI_-LLBR0P6_-NAND3X20_P16**	**C8T28SOI_-LLBR0P6_-NAND3X27_P16**
A to Z ↓	0.0135	0.0136	1.0387	0.7966
A to Z ↑	0.0262	0.0262	1.4084	1.0620
B to Z ↓	0.0125	0.0125	1.0464	0.8022
B to Z ↑	0.0223	0.0221	1.4107	1.0619
C to Z ↓	0.0098	0.0099	1.0617	0.8138
C to Z ↑	0.0162	0.0162	1.4226	1.0711

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P16	8.406e-08	1.000e-20
C8T28SOI_LL_NAND3X7_P16	1.764e-07	1.000e-20
C8T28SOI_LL_NAND3X10_P16	2.505e-07	1.000e-20
C8T28SOI_LL_NAND3X14_P16	3.374e-07	1.000e-20
C8T28SOI_LL_NAND3X20_P16	5.000e-07	1.000e-20
C8T28SOI_LL_NAND3X27_P16	6.609e-07	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P16	9.971e-08	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P16	1.962e-07	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_-P16	2.736e-07	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_-P16	3.705e-07	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_-P16	5.470e-07	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_-P16	7.210e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P16	C8T28SOI_LL_-NAND3X7_P16	C8T28SOI_LL_-NAND3X10_P16	C8T28SOI_LL_-NAND3X14_P16
A (output stable)	7.551e-06	3.544e-05	3.385e-05	5.727e-05
B (output stable)	4.120e-05	1.355e-04	1.872e-04	2.482e-04
C (output stable)	3.395e-05	1.021e-04	1.285e-04	1.829e-04
A to Z	1.013e-03	2.319e-03	3.215e-03	4.378e-03
B to Z	8.500e-04	1.853e-03	2.559e-03	3.474e-03
C to Z	6.901e-04	1.335e-03	1.860e-03	2.488e-03
	C8T28SOI_LL_-NAND3X20_P16	C8T28SOI_LL_-NAND3X27_P16	C8T28SOI_-LLBR0P6_-NAND3X3_P16	C8T28SOI_-LLBR0P6_-NAND3X7_P16

A (output stable)	7.165e-05	9.138e-05	1.096e-05	4.319e-05
B (output stable)	3.522e-04	4.700e-04	6.632e-05	1.852e-04
C (output stable)	2.827e-04	3.634e-04	5.404e-05	1.487e-04
A to Z	6.328e-03	8.409e-03	1.143e-03	2.625e-03
B to Z	5.041e-03	6.676e-03	8.828e-04	1.954e-03
C to Z	3.544e-03	4.735e-03	6.084e-04	1.205e-03
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	C8T28SOI_-LLBR0P6_-NAND3X14_P16	C8T28SOI_-LLBR0P6_-NAND3X20_P16	C8T28SOI_-LLBR0P6_-NAND3X27_P16
A (output stable)	4.406e-05	7.676e-05	8.915e-05	1.175e-04
B (output stable)	2.548e-04	3.629e-04	5.129e-04	6.836e-04
C (output stable)	1.789e-04	2.621e-04	3.877e-04	4.966e-04
A to Z	3.564e-03	4.948e-03	7.117e-03	9.437e-03
B to Z	2.563e-03	3.545e-03	5.112e-03	6.724e-03
C to Z	1.592e-03	2.084e-03	2.963e-03	3.936e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

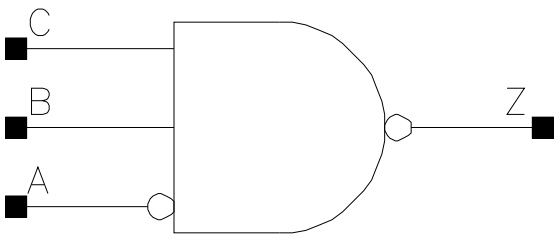
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P16	C8T28SOI_LL_-NAND3X7_P16	C8T28SOI_LL_-NAND3X10_P16	C8T28SOI_LL_-NAND3X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P16	C8T28SOI_LL_-NAND3X27_P16	C8T28SOI_-LLBR0P6_-NAND3X3_P16	C8T28SOI_-LLBR0P6_-NAND3X7_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	C8T28SOI_-LLBR0P6_-NAND3X14_P16	C8T28SOI_-LLBR0P6_-NAND3X20_P16	C8T28SOI_-LLBR0P6_-NAND3X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X7_P16	0.800	1.360	1.0880
X10_P16	0.800	1.632	1.3056
X14_P16	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X10_P16	X14_P16
A	0.0007	0.0010	0.0009	0.0008
B	0.0006	0.0011	0.0017	0.0022
C	0.0006	0.0011	0.0015	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0382	0.0372	8.5383	4.3375
A to Z ↑	0.0273	0.0277	5.2605	2.5390
B to Z ↓	0.0150	0.0164	8.6264	4.3736
B to Z ↑	0.0167	0.0168	5.5029	2.6034
C to Z ↓	0.0151	0.0141	8.6787	4.3993
C to Z ↑	0.0147	0.0137	5.5533	2.6012
	X10_P16	**X14_P16**	**X10_P16**	**X14_P16**
A to Z ↓	0.0411	0.0445	2.9697	2.2629

A to Z ↑	0.0309	0.0338	1.7378	1.2979
B to Z ↓	0.0163	0.0159	2.9906	2.2767
B to Z ↑	0.0166	0.0163	1.7803	1.3308
C to Z ↓	0.0146	0.0140	3.0096	2.2907
C to Z ↑	0.0139	0.0132	1.7959	1.3354

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.137e-07	1.000e-20
X7_P16	2.436e-07	1.000e-20
X10_P16	3.165e-07	1.000e-20
X14_P16	4.051e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	8.990e-04	1.648e-03	2.156e-03	2.642e-03
B (output stable)	1.666e-05	6.253e-05	9.988e-05	1.223e-04
C (output stable)	4.059e-05	1.539e-04	1.874e-04	2.666e-04
A to Z	1.940e-03	4.105e-03	5.727e-03	7.352e-03
B to Z	8.033e-04	1.765e-03	2.554e-03	3.311e-03
C to Z	6.406e-04	1.229e-03	1.848e-03	2.324e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

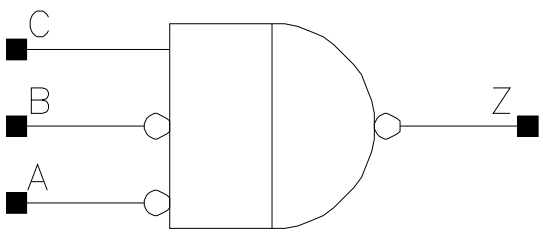
Pin Cycle (vdds)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	0.816	0.6528
X8_P16	0.800	1.088	0.8704
X12_P16	0.800	1.632	1.3056
X15_P16	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X12_P16	X15_P16
A	0.0007	0.0007	0.0014	0.0012
B	0.0008	0.0007	0.0014	0.0013
C	0.0006	0.0011	0.0016	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0343	0.0425	5.5428	2.9705
A to Z ↑	0.0234	0.0271	5.0209	2.5085
B to Z ↓	0.0345	0.0429	5.5424	2.9703
B to Z ↑	0.0219	0.0258	5.0192	2.5061
C to Z ↓	0.0112	0.0103	5.6575	3.0177
C to Z ↑	0.0132	0.0120	5.0952	2.6220
	X12_P16	**X15_P16**	**X12_P16**	**X15_P16**
A to Z ↓	0.0391	0.0428	2.0285	1.5489
A to Z ↑	0.0250	0.0293	1.6724	1.2597
B to Z ↓	0.0369	0.0410	2.0294	1.5492

B to Z ↑	0.0229	0.0270	1.6693	1.2578
C to Z ↓	0.0111	0.0102	2.0656	1.5770
C to Z ↑	0.0126	0.0115	1.7820	1.3078

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	1.656e-07	1.000e-20
X8_P16	2.252e-07	1.000e-20
X12_P16	3.654e-07	1.000e-20
X15_P16	4.014e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	4.918e-04	7.055e-04	1.181e-03	1.372e-03
B (output stable)	3.983e-04	5.880e-04	8.635e-04	1.041e-03
C (output stable)	4.208e-05	1.368e-04	1.686e-04	2.352e-04
A to Z	2.232e-03	3.702e-03	5.882e-03	7.092e-03
B to Z	2.003e-03	3.475e-03	5.148e-03	6.381e-03
C to Z	5.548e-04	9.418e-04	1.551e-03	1.820e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

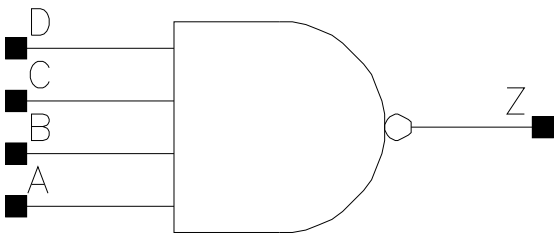
Pin Cycle (vdds)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.224	0.9792
X10_P16	0.800	1.360	1.0880
X14_P16	0.800	1.904	1.5232
X18_P16	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X18_P16
A	0.0005	0.0005	0.0006	0.0006
B	0.0005	0.0005	0.0006	0.0009
C	0.0005	0.0005	0.0006	0.0007
D	0.0005	0.0005	0.0006	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0560	0.0526	3.3567	1.6951
A to Z ↑	0.0452	0.0466	5.0575	2.5639
B to Z ↓	0.0580	0.0549	3.3586	1.6945
B to Z ↑	0.0437	0.0459	5.0531	2.5643
C to Z ↓	0.0572	0.0531	3.3613	1.6947
C to Z ↑	0.0467	0.0489	5.0541	2.5613

D to Z ↓	0.0598	0.0557	3.3593	1.6935
D to Z ↑	0.0461	0.0485	5.0554	2.5607
	X14_P16	**X18_P16**	**X14_P16**	**X18_P16**
A to Z ↓	0.0567	0.0528	1.1749	0.9466
A to Z ↑	0.0465	0.0454	1.7639	1.3971
B to Z ↓	0.0591	0.0549	1.1748	0.9467
B to Z ↑	0.0451	0.0443	1.7643	1.3975
C to Z ↓	0.0540	0.0483	1.1737	0.9461
C to Z ↑	0.0469	0.0444	1.7595	1.3953
D to Z ↓	0.0564	0.0500	1.1733	0.9461
D to Z ↑	0.0461	0.0429	1.7606	1.3953

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.863e-07	1.000e-20
X10_P16	2.718e-07	1.000e-20
X14_P16	4.040e-07	1.000e-20
X18_P16	4.870e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	3.603e-04	4.423e-04	6.750e-04	7.350e-04
B (output stable)	3.328e-04	4.138e-04	6.286e-04	6.865e-04
C (output stable)	3.797e-04	4.284e-04	6.602e-04	6.479e-04
D (output stable)	3.520e-04	3.988e-04	5.881e-04	5.715e-04
A to Z	2.665e-03	3.818e-03	5.959e-03	6.939e-03
B to Z	2.585e-03	3.735e-03	5.846e-03	6.805e-03
C to Z	2.795e-03	3.860e-03	5.628e-03	6.373e-03
D to Z	2.730e-03	3.782e-03	5.514e-03	6.227e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

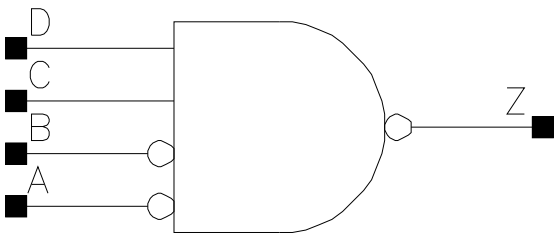
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.952	0.7616
X7_P16	0.800	1.360	1.0880
X10_P16	0.800	2.040	1.6320
X14_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P16	X7_P16	X10_P16	X14_P16
A	0.0008	0.0008	0.0014	0.0012
B	0.0008	0.0007	0.0014	0.0013
C	0.0007	0.0011	0.0017	0.0022
D	0.0006	0.0011	0.0015	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X7_P16	X3_P16	X7_P16
A to Z ↓	0.0393	0.0465	8.1853	4.3404
A to Z ↑	0.0255	0.0293	5.0959	2.5501
B to Z ↓	0.0390	0.0466	8.1903	4.3418
B to Z ↑	0.0238	0.0276	5.0938	2.5466
C to Z ↓	0.0155	0.0162	8.2783	4.3638
C to Z ↑	0.0171	0.0167	5.2464	2.6076

D to Z ↓	0.0149	0.0140	8.3175	4.3900
D to Z ↑	0.0147	0.0136	5.2525	2.6022
	X10_P16	**X14_P16**	**X10_P16**	**X14_P16**
A to Z ↓	0.0435	0.0477	2.9675	2.2690
A to Z ↑	0.0269	0.0332	1.7185	1.2692
B to Z ↓	0.0413	0.0465	2.9683	2.2694
B to Z ↑	0.0247	0.0312	1.7161	1.2678
C to Z ↓	0.0162	0.0159	2.9871	2.2800
C to Z ↑	0.0166	0.0163	1.7812	1.3328
D to Z ↓	0.0145	0.0141	3.0050	2.2944
D to Z ↑	0.0138	0.0133	1.7969	1.3376

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.617e-07	1.000e-20
X7_P16	2.230e-07	1.000e-20
X10_P16	3.686e-07	1.000e-20
X14_P16	4.004e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	5.995e-04	8.307e-04	1.453e-03	1.721e-03
B (output stable)	4.930e-04	7.348e-04	1.121e-03	1.429e-03
C (output stable)	5.768e-05	9.964e-05	1.493e-04	1.981e-04
D (output stable)	3.787e-05	1.232e-04	1.601e-04	2.058e-04
A to Z	2.637e-03	4.360e-03	6.830e-03	8.652e-03
B to Z	2.412e-03	4.142e-03	6.110e-03	8.001e-03
C to Z	8.658e-04	1.752e-03	2.522e-03	3.308e-03
D to Z	6.981e-04	1.217e-03	1.828e-03	2.339e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

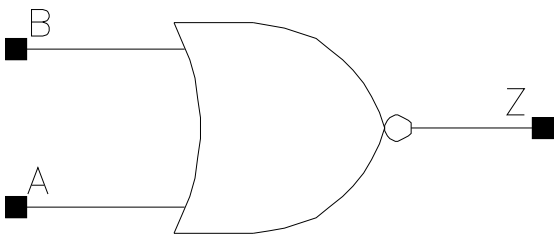
Pin Cycle (vdds)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.408	0.3264
X4_P16	0.800	0.408	0.3264
X8_P16	0.800	0.680	0.5440
X9_P16	1.600	0.408	0.6528
X12_P16	0.800	0.952	0.7616
X16_P16	0.800	1.224	0.9792
X19_P16	1.600	0.680	1.0880
X20_P16	0.800	1.496	1.1968
X23_P16	0.800	1.496	1.1968
X24_P16	0.800	1.768	1.4144
X27_P16	0.800	1.632	1.3056
X29_P16	1.600	0.952	1.5232
X31_P16	0.800	2.312	1.8496
X34_P16	0.800	2.040	1.6320
X38_P16	0.800	2.176	1.7408
X39_P16	1.600	1.224	1.9584
X46_P16	1.600	1.224	1.9584
X57_P16	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P16	X4_P16	X8_P16	X9_P16
A	0.0004	0.0006	0.0012	0.0013
B	0.0004	0.0006	0.0011	0.0012
	X12_P16	X16_P16	X19_P16	X20_P16

A	0.0018	0.0023	0.0025	0.0030
B	0.0016	0.0021	0.0023	0.0026
	X23_P16	X24_P16	X27_P16	X29_P16
A	0.0008	0.0035	0.0008	0.0038
B	0.0007	0.0032	0.0007	0.0035
	X31_P16	X34_P16	X38_P16	X39_P16
A	0.0046	0.0008	0.0008	0.0051
B	0.0043	0.0007	0.0007	0.0046
	X46_P16	X57_P16		
A	0.0008	0.0008		
B	0.0009	0.0009		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X4_P16**	**X2_P16**	**X4_P16**
A to Z ↓	0.0114	0.0109	6.4621	3.5625
A to Z ↑	0.0205	0.0185	19.9161	10.6407
B to Z ↓	0.0101	0.0092	6.5138	3.5972
B to Z ↑	0.0205	0.0178	20.0106	10.6924
	X8_P16	**X9_P16**	**X8_P16**	**X9_P16**
A to Z ↓	0.0102	0.0094	1.7185	1.3637
A to Z ↑	0.0181	0.0171	5.0326	4.8137
B to Z ↓	0.0073	0.0078	1.7227	1.4134
B to Z ↑	0.0140	0.0163	5.0663	4.8380
	X12_P16	**X16_P16**	**X12_P16**	**X16_P16**
A to Z ↓	0.0104	0.0104	1.1797	0.8772
A to Z ↑	0.0175	0.0180	3.3041	2.5223
B to Z ↓	0.0079	0.0076	1.1934	0.8883
B to Z ↑	0.0145	0.0142	3.3270	2.5413
	X19_P16	**X20_P16**	**X19_P16**	**X20_P16**
A to Z ↓	0.0101	0.0107	0.6906	0.7218
A to Z ↑	0.0195	0.0177	2.4627	2.0035
B to Z ↓	0.0080	0.0080	0.6984	0.7308
B to Z ↑	0.0162	0.0145	2.4758	2.0181
	X23_P16	**X24_P16**	**X23_P16**	**X24_P16**
A to Z ↓	0.0380	0.0105	0.7340	0.5975
A to Z ↑	0.0526	0.0177	1.0613	1.6899
B to Z ↓	0.0361	0.0077	0.7338	0.6056
B to Z ↑	0.0524	0.0141	1.0610	1.7018
	X27_P16	**X29_P16**	**X27_P16**	**X29_P16**
A to Z ↓	0.0399	0.0098	0.6128	0.4570
A to Z ↑	0.0545	0.0184	0.8872	1.6521
B to Z ↓	0.0380	0.0076	0.6128	0.4620
B to Z ↑	0.0543	0.0157	0.8863	1.6622
	X31_P16	**X34_P16**	**X31_P16**	**X34_P16**
A to Z ↓	0.0106	0.0413	0.4464	0.5021
A to Z ↑	0.0179	0.0610	1.2659	0.7244
B to Z ↓	0.0079	0.0394	0.4525	0.5020
B to Z ↑	0.0143	0.0613	1.2763	0.7241
	X38_P16	**X39_P16**	**X38_P16**	**X39_P16**
A to Z ↓	0.0425	0.0100	0.4377	0.3487
A to Z ↑	0.0621	0.0188	0.6356	1.2392

B to Z ↓	0.0406	0.0077	0.4377	0.3537
B to Z ↑	0.0623	0.0155	0.6349	1.2470
	X46_P16	**X57_P16**	**X46_P16**	**X57_P16**
A to Z ↓	0.0479	0.0520	0.3347	0.2751
A to Z ↑	0.0636	0.0667	0.6307	0.5086
B to Z ↓	0.0464	0.0504	0.3350	0.2754
B to Z ↑	0.0645	0.0676	0.6313	0.5087

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P16	4.440e-08	1.000e-20
X4_P16	8.607e-08	1.000e-20
X8_P16	1.768e-07	1.000e-20
X9_P16	2.118e-07	1.000e-20
X12_P16	2.582e-07	1.000e-20
X16_P16	3.398e-07	1.000e-20
X19_P16	4.108e-07	1.000e-20
X20_P16	4.214e-07	1.000e-20
X23_P16	5.201e-07	1.000e-20
X24_P16	5.030e-07	1.000e-20
X27_P16	5.852e-07	1.000e-20
X29_P16	6.000e-07	1.000e-20
X31_P16	6.663e-07	1.000e-20
X34_P16	7.511e-07	1.000e-20
X38_P16	8.187e-07	1.000e-20
X39_P16	7.896e-07	1.000e-20
X46_P16	8.852e-07	1.000e-20
X57_P16	1.038e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P16	X4_P16	X8_P16	X9_P16
A (output stable)	1.510e-05	2.580e-05	9.670e-05	5.633e-05
B (output stable)	2.706e-06	4.309e-06	4.396e-05	1.021e-05
A to Z	4.684e-04	7.636e-04	1.543e-03	1.537e-03
B to Z	3.531e-04	5.454e-04	8.167e-04	1.089e-03
	X12_P16	X16_P16	X19_P16	X20_P16
A (output stable)	1.385e-04	1.944e-04	2.018e-04	2.323e-04
B (output stable)	6.059e-05	7.982e-05	9.759e-05	9.254e-05
A to Z	2.265e-03	3.074e-03	3.497e-03	3.819e-03
B to Z	1.325e-03	1.699e-03	2.187e-03	2.221e-03
	X23_P16	X24_P16	X27_P16	X29_P16
A (output stable)	2.757e-05	2.851e-04	2.767e-05	2.729e-04
B (output stable)	4.615e-06	1.063e-04	4.719e-06	1.096e-04
A to Z	7.290e-03	4.530e-03	8.171e-03	4.861e-03
B to Z	7.072e-03	2.548e-03	7.954e-03	3.061e-03
	X31_P16	X34_P16	X38_P16	X39_P16
A (output stable)	3.808e-04	2.928e-05	2.938e-05	3.967e-04
B (output stable)	1.455e-04	5.142e-06	5.244e-06	1.650e-04
A to Z	6.046e-03	1.075e-02	1.168e-02	6.648e-03
B to Z	3.430e-03	1.052e-02	1.144e-02	4.065e-03
	X46_P16	X57_P16		

A (output stable)	3.047e-05	3.068e-05		
B (output stable)	6.188e-06	6.387e-06		
A to Z	1.263e-02	1.530e-02		
B to Z	1.242e-02	1.509e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

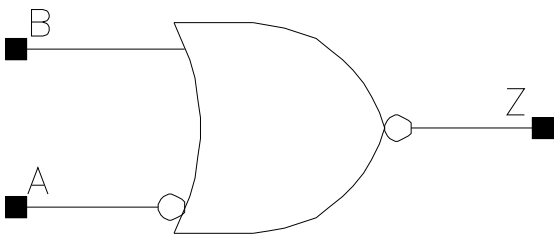
Pin Cycle (vdds)	X2_P16	X4_P16	X8_P16	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P16	X16_P16	X19_P16	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P16	X24_P16	X27_P16	X29_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P16	X34_P16	X38_P16	X39_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P16	X57_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.544	0.4352
X3_P16	0.800	0.544	0.4352
X4_P16	0.800	0.544	0.4352
X10_P16	1.600	0.544	0.8704
X14_P16	1.600	0.816	1.3056
X19_P16	1.600	0.816	1.3056
X29_P16	1.600	1.088	1.7408
X39_P16	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P16	X3_P16	X4_P16	X10_P16
A	0.0006	0.0006	0.0006	0.0010
B	0.0004	0.0004	0.0005	0.0012
	X14_P16	X19_P16	X29_P16	X39_P16
A	0.0010	0.0010	0.0017	0.0016
B	0.0019	0.0023	0.0035	0.0045

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	X3_P16	X2_P16	X3_P16
A to Z ↓	0.0297	0.0299	6.2674	4.7685
A to Z ↑	0.0275	0.0273	19.7986	16.6994
B to Z ↓	0.0099	0.0089	6.5648	4.9763

B to Z ↑	0.0197	0.0187	20.0064	16.8468
	X4_P16	**X10_P16**	**X4_P16**	**X10_P16**
A to Z ↓	0.0309	0.0306	3.6798	1.3446
A to Z ↑	0.0271	0.0266	12.0153	4.7487
B to Z ↓	0.0084	0.0079	3.8379	1.3524
B to Z ↑	0.0168	0.0167	12.1226	4.7978
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0370	0.0397	0.8467	0.6640
A to Z ↑	0.0306	0.0317	3.2421	2.3837
B to Z ↓	0.0075	0.0072	0.9363	0.7367
B to Z ↑	0.0157	0.0146	3.2791	2.4110
	X29_P16	**X39_P16**	**X29_P16**	**X39_P16**
A to Z ↓	0.0341	0.0389	0.4460	0.3355
A to Z ↑	0.0300	0.0320	1.6505	1.2139
B to Z ↓	0.0075	0.0072	0.4633	0.3644
B to Z ↑	0.0155	0.0144	1.6688	1.2281

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P16	7.414e-08	1.000e-20
X3_P16	8.763e-08	1.000e-20
X4_P16	1.099e-07	1.000e-20
X10_P16	2.973e-07	1.000e-20
X14_P16	3.749e-07	1.000e-20
X19_P16	4.888e-07	1.000e-20
X29_P16	7.497e-07	1.000e-20
X39_P16	9.433e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P16	X3_P16	X4_P16	X10_P16
A (output stable)	6.905e-04	7.545e-04	8.567e-04	1.769e-03
B (output stable)	2.583e-06	3.717e-06	7.124e-06	2.244e-05
A to Z	1.194e-03	1.318e-03	1.543e-03	3.522e-03
B to Z	3.299e-04	3.656e-04	4.312e-04	1.148e-03
	X14_P16	X19_P16	X29_P16	X39_P16
A (output stable)	2.691e-03	3.132e-03	4.639e-03	5.992e-03
B (output stable)	2.695e-05	4.573e-05	6.120e-05	9.112e-05
A to Z	5.187e-03	6.229e-03	9.906e-03	1.219e-02
B to Z	1.511e-03	1.836e-03	3.019e-03	3.622e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P16	X3_P16	X4_P16	X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P16	X19_P16	X29_P16	X39_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

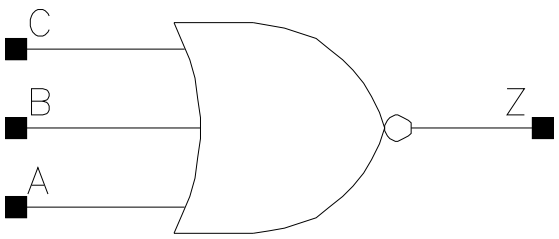
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.544	0.4352
X7_P16	0.800	0.952	0.7616
X11_P16	0.800	1.360	1.0880
X14_P16	0.800	1.768	1.4144
X21_P16	0.800	2.584	2.0672
X29_P16	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X11_P16	X14_P16
A	0.0006	0.0011	0.0018	0.0023
B	0.0006	0.0012	0.0017	0.0025
C	0.0006	0.0010	0.0016	0.0021
	X21_P16	X29_P16		
A	0.0037	0.0048		
B	0.0036	0.0048		
C	0.0032	0.0042		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0122	0.0124	3.6158	1.9017
A to Z ↑	0.0246	0.0257	14.9143	7.6919

B to Z ↓	0.0115	0.0115	3.6436	1.8263
B to Z ↑	0.0232	0.0254	14.9453	7.7011
C to Z ↓	0.0099	0.0085	3.6931	1.8474
C to Z ↑	0.0209	0.0176	15.0012	7.7285
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0124	0.0124	1.1923	0.9164
A to Z ↑	0.0260	0.0254	5.0641	3.6848
B to Z ↓	0.0116	0.0115	1.2048	0.8898
B to Z ↑	0.0236	0.0248	5.0732	3.6911
C to Z ↓	0.0091	0.0087	1.2021	0.9047
C to Z ↑	0.0192	0.0178	5.0900	3.7060
	X21_P16	**X29_P16**	**X21_P16**	**X29_P16**
A to Z ↓	0.0124	0.0125	0.6105	0.4585
A to Z ↑	0.0252	0.0253	2.4737	1.8604
B to Z ↓	0.0115	0.0116	0.5992	0.4533
B to Z ↑	0.0244	0.0245	2.4770	1.8630
C to Z ↓	0.0089	0.0090	0.6114	0.4622
C to Z ↑	0.0180	0.0181	2.4871	1.8703

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	9.439e-08	1.000e-20
X7_P16	1.828e-07	1.000e-20
X11_P16	2.853e-07	1.000e-20
X14_P16	3.799e-07	1.000e-20
X21_P16	5.650e-07	1.000e-20
X29_P16	7.508e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	1.208e-04	3.180e-04	4.991e-04	6.407e-04
B (output stable)	-2.609e-06	9.256e-05	3.288e-05	1.579e-04
C (output stable)	2.608e-06	2.170e-05	2.097e-05	4.193e-05
A to Z	1.044e-03	2.136e-03	3.369e-03	4.398e-03
B to Z	8.240e-04	1.754e-03	2.504e-03	3.588e-03
C to Z	5.946e-04	9.562e-04	1.656e-03	2.036e-03
	X21_P16	X29_P16		
A (output stable)	9.304e-04	1.243e-03		
B (output stable)	2.080e-04	2.796e-04		
C (output stable)	6.400e-05	9.016e-05		
A to Z	6.510e-03	8.689e-03		
B to Z	5.251e-03	7.016e-03		
C to Z	3.054e-03	4.094e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

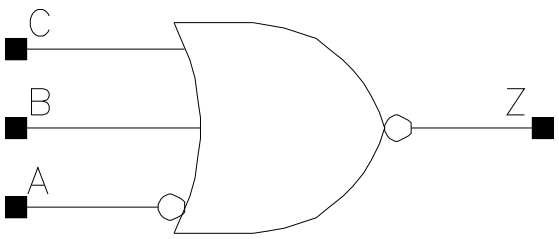
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P16	X29_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X7_P16	0.800	1.360	1.0880
X11_P16	0.800	1.632	1.3056
X14_P16	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X11_P16	X14_P16
A	0.0007	0.0008	0.0010	0.0015
B	0.0006	0.0012	0.0017	0.0022
C	0.0006	0.0011	0.0016	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0332	0.0299	3.4889	1.6401
A to Z ↑	0.0357	0.0359	14.9581	7.3090
B to Z ↓	0.0115	0.0114	3.6617	1.7314
B to Z ↑	0.0230	0.0248	15.0341	7.3378
C to Z ↓	0.0099	0.0088	3.7014	1.7467
C to Z ↑	0.0208	0.0184	15.0913	7.3623
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0364	0.0291	1.1642	0.8591

A to Z ↑	0.0401	0.0353	5.0730	3.7349
B to Z ↓	0.0116	0.0113	1.2061	0.8981
B to Z ↑	0.0235	0.0237	5.0933	3.7518
C to Z ↓	0.0089	0.0087	1.2051	0.9097
C to Z ↑	0.0189	0.0180	5.1106	3.7665

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.260e-07	1.000e-20
X7_P16	2.750e-07	1.000e-20
X11_P16	3.504e-07	1.000e-20
X14_P16	5.130e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	1.031e-03	1.973e-03	2.671e-03	3.657e-03
B (output stable)	9.263e-07	3.138e-05	3.314e-05	7.806e-05
C (output stable)	3.714e-06	2.785e-05	2.509e-05	4.531e-05
A to Z	2.030e-03	4.226e-03	5.820e-03	7.998e-03
B to Z	8.163e-04	1.816e-03	2.498e-03	3.389e-03
C to Z	5.877e-04	1.079e-03	1.608e-03	2.026e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

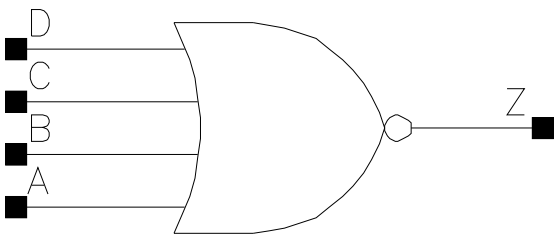
Pin Cycle (vdds)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.224	0.9792
X10_P16	0.800	1.632	1.3056
X14_P16	0.800	1.904	1.5232
X18_P16	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X18_P16
A	0.0005	0.0004	0.0005	0.0006
B	0.0006	0.0006	0.0007	0.0008
C	0.0005	0.0005	0.0006	0.0007
D	0.0006	0.0005	0.0006	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0367	0.0412	3.4669	1.6630
A to Z ↑	0.0584	0.0659	5.3414	2.5657
B to Z ↓	0.0358	0.0414	3.4668	1.6626
B to Z ↑	0.0589	0.0686	5.3396	2.5665
C to Z ↓	0.0373	0.0419	3.4649	1.6600
C to Z ↑	0.0617	0.0711	5.3414	2.5666

D to Z ↓	0.0370	0.0405	3.4609	1.6600
D to Z ↑	0.0633	0.0713	5.3388	2.5667
	X14_P16	**X18_P16**	**X14_P16**	**X18_P16**
A to Z ↓	0.0402	0.0419	1.1507	0.9093
A to Z ↑	0.0611	0.0597	1.7710	1.3334
B to Z ↓	0.0397	0.0405	1.1498	0.9088
B to Z ↑	0.0627	0.0601	1.7719	1.3317
C to Z ↓	0.0391	0.0416	1.1469	0.9065
C to Z ↑	0.0610	0.0601	1.7708	1.3330
D to Z ↓	0.0379	0.0398	1.1470	0.9072
D to Z ↑	0.0617	0.0604	1.7698	1.3310

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.140e-07	1.000e-20
X10_P16	3.001e-07	1.000e-20
X14_P16	4.402e-07	1.000e-20
X18_P16	5.572e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	3.878e-04	5.111e-04	6.395e-04	7.921e-04
B (output stable)	3.301e-04	4.652e-04	5.751e-04	6.932e-04
C (output stable)	4.142e-04	4.961e-04	6.551e-04	8.300e-04
D (output stable)	3.530e-04	4.343e-04	5.735e-04	7.202e-04
A to Z	2.665e-03	4.178e-03	5.945e-03	7.565e-03
B to Z	2.544e-03	4.075e-03	5.785e-03	7.361e-03
C to Z	2.742e-03	4.070e-03	5.541e-03	7.068e-03
D to Z	2.647e-03	3.959e-03	5.388e-03	6.853e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

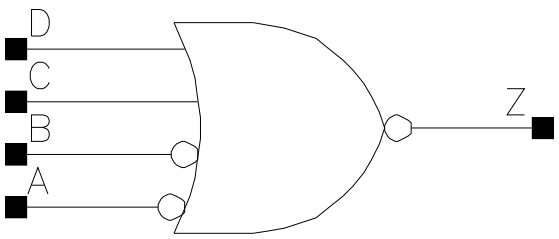
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	1.224	0.9792
X7_P16	0.800	1.496	1.1968
X11_P16	0.800	2.040	1.6320
X14_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P16	X7_P16	X11_P16	X14_P16
A	0.0008	0.0008	0.0015	0.0014
B	0.0008	0.0008	0.0015	0.0015
C	0.0006	0.0011	0.0016	0.0022
D	0.0006	0.0011	0.0016	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X7_P16	X4_P16	X7_P16
A to Z ↓	0.0325	0.0346	3.2301	1.6698
A to Z ↑	0.0438	0.0438	14.3646	7.4122
B to Z ↓	0.0300	0.0320	3.2286	1.6679
B to Z ↑	0.0439	0.0440	14.3748	7.4143
C to Z ↓	0.0117	0.0114	3.3463	1.7460
C to Z ↑	0.0242	0.0246	14.4202	7.4436

D to Z ↓	0.0101	0.0088	3.3725	1.7467
D to Z ↑	0.0219	0.0185	14.4508	7.4679
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0312	0.0343	1.1473	0.8619
A to Z ↑	0.0405	0.0440	5.0119	3.7232
B to Z ↓	0.0283	0.0318	1.1455	0.8604
B to Z ↑	0.0404	0.0447	5.0123	3.7246
C to Z ↓	0.0116	0.0116	1.2053	0.8966
C to Z ↑	0.0234	0.0240	5.0284	3.7358
D to Z ↓	0.0090	0.0088	1.2054	0.8997
D to Z ↑	0.0189	0.0183	5.0467	3.7503

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	1.873e-07	1.000e-20
X7_P16	2.732e-07	1.000e-20
X11_P16	4.359e-07	1.000e-20
X14_P16	5.230e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X7_P16	X11_P16	X14_P16
A (output stable)	8.482e-04	1.055e-03	1.644e-03	2.054e-03
B (output stable)	7.419e-04	9.533e-04	1.432e-03	1.857e-03
C (output stable)	4.829e-05	2.217e-05	4.740e-05	7.040e-05
D (output stable)	3.153e-05	3.756e-05	5.075e-05	8.070e-05
A to Z	3.295e-03	4.588e-03	6.988e-03	9.102e-03
B to Z	3.016e-03	4.313e-03	6.418e-03	8.584e-03
C to Z	9.241e-04	1.784e-03	2.509e-03	3.456e-03
D to Z	6.939e-04	1.073e-03	1.622e-03	2.097e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

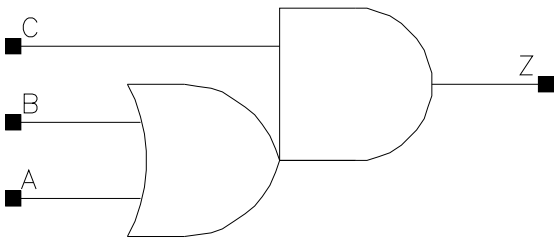
Pin Cycle (vdds)	X4_P16	X7_P16	X11_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.680	0.5440
X10_P16	0.800	0.952	0.7616
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0006	0.0007	0.0013
B	0.0007	0.0007	0.0015
C	0.0008	0.0009	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0324	0.0371	3.3485	1.6771
A to Z ↑	0.0265	0.0314	5.9086	2.5714
B to Z ↓	0.0328	0.0377	3.3488	1.6788
B to Z ↑	0.0244	0.0289	5.9008	2.5682
C to Z ↓	0.0296	0.0322	3.3024	1.6457
C to Z ↑	0.0254	0.0290	5.8994	2.5671
	X19_P16		**X19_P16**	
A to Z ↓	0.0385		0.8766	
A to Z ↑	0.0328		1.3133	

B to Z ↓	0.0391		0.8768	
B to Z ↑	0.0300		1.3094	
C to Z ↓	0.0324		0.8572	
C to Z ↑	0.0294		1.3102	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.641e-07	1.000e-20
X10_P16	2.573e-07	1.000e-20
X19_P16	4.885e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	7.441e-05	7.801e-05	1.532e-04
B (output stable)	2.078e-05	2.257e-05	3.588e-05
C (output stable)	4.862e-05	4.939e-05	1.018e-04
A to Z	1.785e-03	2.892e-03	5.840e-03
B to Z	1.593e-03	2.671e-03	5.414e-03
C to Z	1.991e-03	3.055e-03	6.055e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

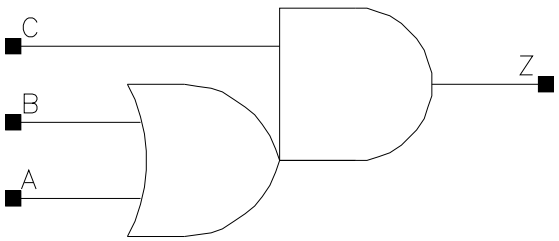
Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	1.360	1.0880
X14_P16	0.800	1.496	1.1968
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0007	0.0014	0.0014	0.0014
B	0.0007	0.0013	0.0013	0.0013
C	0.0007	0.0014	0.0014	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0399	0.0338	3.2659	1.6541
A to Z ↑	0.0274	0.0254	5.0945	2.4937
B to Z ↓	0.0403	0.0337	3.2698	1.6555
B to Z ↑	0.0254	0.0235	5.0878	2.4948
C to Z ↓	0.0269	0.0225	3.2022	1.6287
C to Z ↑	0.0251	0.0227	5.0867	2.4930
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0373	0.0406	1.1579	0.8750

A to Z ↑	0.0277	0.0297	1.6914	1.2692
B to Z ↓	0.0375	0.0409	1.1582	0.8745
B to Z ↑	0.0259	0.0280	1.6904	1.2682
C to Z ↓	0.0251	0.0274	1.1347	0.8535
C to Z ↑	0.0254	0.0277	1.6877	1.2673

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.905e-07	1.000e-20
X10_P16	3.818e-07	1.000e-20
X14_P16	4.467e-07	1.000e-20
X19_P16	5.105e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	2.035e-05	4.527e-05	4.562e-05	4.505e-05
B (output stable)	7.271e-06	1.589e-05	1.589e-05	1.611e-05
C (output stable)	2.018e-04	3.935e-04	3.940e-04	3.955e-04
A to Z	2.309e-03	4.101e-03	5.162e-03	6.162e-03
B to Z	2.098e-03	3.603e-03	4.670e-03	5.674e-03
C to Z	1.818e-03	3.065e-03	4.095e-03	5.046e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

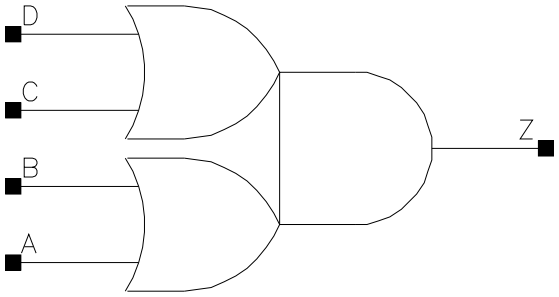
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.952	0.7616
X10_P16	0.800	1.088	0.8704
X14_P16	0.800	1.904	1.5232
X19_P16	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0005	0.0007	0.0013	0.0013
B	0.0005	0.0007	0.0013	0.0013
C	0.0005	0.0007	0.0014	0.0014
D	0.0005	0.0007	0.0014	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0555	0.0449	3.4007	1.6910
A to Z ↑	0.0370	0.0324	5.1150	2.5519
B to Z ↓	0.0563	0.0456	3.4016	1.6914

B to Z ↑	0.0354	0.0306	5.1074	2.5486
C to Z ↓	0.0472	0.0397	3.3754	1.6847
C to Z ↑	0.0359	0.0324	5.1089	2.5501
D to Z ↓	0.0476	0.0398	3.3774	1.6855
D to Z ↑	0.0338	0.0301	5.1033	2.5478
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0431	0.0454	1.1775	0.8841
A to Z ↑	0.0309	0.0321	1.6963	1.2752
B to Z ↓	0.0419	0.0443	1.1786	0.8847
B to Z ↑	0.0285	0.0297	1.6928	1.2720
C to Z ↓	0.0368	0.0393	1.1726	0.8800
C to Z ↑	0.0300	0.0315	1.6946	1.2745
D to Z ↓	0.0349	0.0375	1.1736	0.8814
D to Z ↑	0.0271	0.0286	1.6916	1.2706

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.443e-07	1.000e-20
X10_P16	2.887e-07	1.000e-20
X14_P16	4.961e-07	1.000e-20
X19_P16	5.543e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	1.354e-05	2.364e-05	7.593e-05	7.635e-05
B (output stable)	1.303e-05	1.662e-05	3.985e-05	4.045e-05
C (output stable)	2.332e-05	4.280e-05	1.684e-04	1.695e-04
D (output stable)	5.301e-05	6.338e-05	1.478e-04	1.468e-04
A to Z	2.246e-03	3.525e-03	6.095e-03	6.855e-03
B to Z	2.126e-03	3.286e-03	5.431e-03	6.193e-03
C to Z	1.933e-03	3.096e-03	5.198e-03	5.961e-03
D to Z	1.815e-03	2.868e-03	4.509e-03	5.271e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

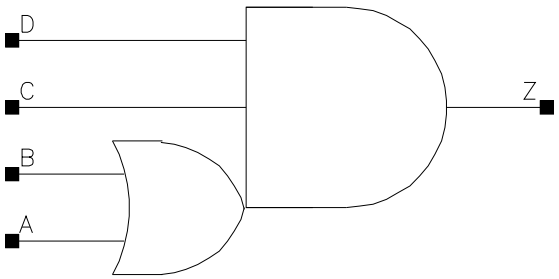
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	0.816	0.6528
X10_P16	0.800	1.088	0.8704
X14_P16	0.800	1.904	1.5232
X19_P16	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P16	X10_P16	X14_P16	X19_P16
A	0.0005	0.0010	0.0011	0.0013
B	0.0005	0.0007	0.0011	0.0014
C	0.0005	0.0008	0.0012	0.0014
D	0.0005	0.0007	0.0011	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X10_P16	X4_P16	X10_P16
A to Z ↓	0.0470	0.0452	3.7057	1.7263
A to Z ↑	0.0414	0.0430	5.4352	2.6041
B to Z ↓	0.0483	0.0426	3.7055	1.7267
B to Z ↑	0.0396	0.0377	5.4373	2.6030
C to Z ↓	0.0395	0.0353	3.5899	1.6839

C to Z ↑	0.0395	0.0383	5.4272	2.5989
D to Z ↓	0.0387	0.0340	3.5909	1.6821
D to Z ↑	0.0411	0.0394	5.4300	2.6012
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0446	0.0425	1.1800	0.8760
A to Z ↑	0.0414	0.0422	1.7337	1.2985
B to Z ↓	0.0430	0.0412	1.1801	0.8766
B to Z ↑	0.0377	0.0383	1.7296	1.2942
C to Z ↓	0.0369	0.0353	1.1515	0.8570
C to Z ↑	0.0386	0.0388	1.7281	1.2951
D to Z ↓	0.0349	0.0336	1.1486	0.8552
D to Z ↑	0.0387	0.0389	1.7293	1.2956

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	1.246e-07	1.000e-20
X10_P16	2.544e-07	1.000e-20
X14_P16	3.888e-07	1.000e-20
X19_P16	5.072e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X10_P16	X14_P16	X19_P16
A (output stable)	4.609e-05	8.253e-05	1.520e-04	1.758e-04
B (output stable)	2.810e-05	5.553e-05	9.303e-05	1.034e-04
C (output stable)	9.613e-06	1.895e-05	4.903e-05	5.680e-05
D (output stable)	2.162e-05	3.725e-05	1.145e-04	1.221e-04
A to Z	1.891e-03	3.404e-03	5.209e-03	6.448e-03
B to Z	1.788e-03	3.007e-03	4.670e-03	5.783e-03
C to Z	2.105e-03	3.542e-03	5.670e-03	6.928e-03
D to Z	2.008e-03	3.377e-03	5.257e-03	6.461e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

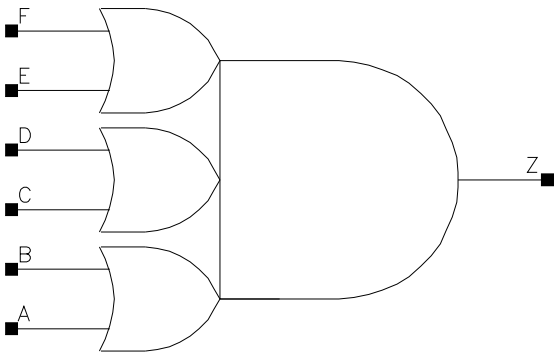
Pin Cycle (vdds)	X4_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	1.360	1.0880
X9_P16	0.800	1.496	1.1968
X19_P16	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P16	X9_P16	X19_P16
A	0.0005	0.0007	0.0011
B	0.0006	0.0009	0.0013
C	0.0005	0.0007	0.0012
D	0.0004	0.0006	0.0013
E	0.0005	0.0007	0.0012
F	0.0005	0.0007	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X9_P16	X4_P16	X9_P16
A to Z ↓	0.0654	0.0544	3.7770	1.8642
A to Z ↑	0.0483	0.0458	5.5808	2.7463
B to Z ↓	0.0679	0.0563	3.7771	1.8642
B to Z ↑	0.0479	0.0443	5.5869	2.7452
C to Z ↓	0.0600	0.0494	3.7550	1.8533
C to Z ↑	0.0484	0.0447	5.5888	2.7467
D to Z ↓	0.0605	0.0500	3.7552	1.8536
D to Z ↑	0.0460	0.0421	5.5831	2.7432
E to Z ↓	0.0512	0.0435	3.7237	1.8441
E to Z ↑	0.0445	0.0423	5.5787	2.7431
F to Z ↓	0.0524	0.0445	3.7256	1.8453
F to Z ↑	0.0428	0.0403	5.5756	2.7399
	X19_P16		X19_P16	
A to Z ↓	0.0531		0.8963	
A to Z ↑	0.0442		1.2984	
B to Z ↓	0.0543		0.8965	
B to Z ↑	0.0412		1.2947	
C to Z ↓	0.0488		0.8910	
C to Z ↑	0.0436		1.2981	
D to Z ↓	0.0498		0.8913	
D to Z ↑	0.0411		1.2940	
E to Z ↓	0.0429		0.8868	
E to Z ↑	0.0417		1.2961	
F to Z ↓	0.0438		0.8873	
F to Z ↑	0.0389		1.2925	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	1.640e-07	1.000e-20
X9_P16	3.103e-07	1.000e-20
X19_P16	6.234e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X9_P16	X19_P16
A (output stable)	1.118e-05	1.905e-05	3.602e-05
B (output stable)	7.803e-06	1.261e-05	1.511e-05
C (output stable)	2.351e-05	3.374e-05	7.243e-05
D (output stable)	2.770e-05	4.255e-05	8.449e-05
E (output stable)	2.197e-05	3.217e-05	6.595e-05
F (output stable)	8.752e-05	1.136e-04	2.146e-04
A to Z	2.684e-03	4.203e-03	8.139e-03
B to Z	2.599e-03	4.024e-03	7.731e-03
C to Z	2.417e-03	3.812e-03	7.434e-03
D to Z	2.296e-03	3.584e-03	7.015e-03
E to Z	2.074e-03	3.378e-03	6.589e-03
F to Z	1.976e-03	3.182e-03	6.198e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

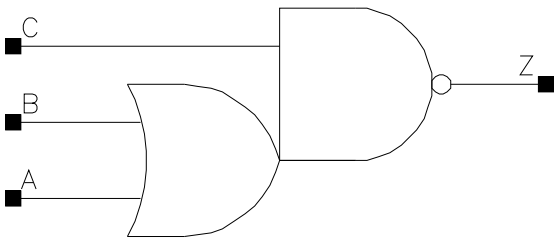
Pin Cycle (vdds)	X4_P16	X9_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.544	0.4352
X10_P16	0.800	1.360	1.0880
X20_P16	0.800	2.720	2.1760
X26_P16	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P16	X10_P16	X20_P16	X26_P16
A	0.0005	0.0017	0.0033	0.0044
B	0.0005	0.0015	0.0030	0.0040
C	0.0005	0.0017	0.0035	0.0047

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X10_P16**	**X3_P16**	**X10_P16**
A to Z ↓	0.0137	0.0150	6.6201	2.0871
A to Z ↑	0.0184	0.0191	12.1304	3.3514
B to Z ↓	0.0112	0.0118	6.4996	2.1031
B to Z ↑	0.0178	0.0165	12.1907	3.3773
C to Z ↓	0.0130	0.0136	5.9927	1.9104
C to Z ↑	0.0181	0.0170	6.4346	1.7827
	X20_P16	**X26_P16**	**X20_P16**	**X26_P16**
A to Z ↓	0.0156	0.0157	1.0678	0.8084

A to Z ↑	0.0197	0.0196	1.7168	1.2910
B to Z ↓	0.0123	0.0124	1.0792	0.8205
B to Z ↑	0.0171	0.0172	1.7284	1.3003
C to Z ↓	0.0142	0.0142	0.9794	0.7428
C to Z ↑	0.0173	0.0172	0.8744	0.6567

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	9.217e-08	1.000e-20
X10_P16	3.140e-07	1.000e-20
X20_P16	6.254e-07	1.000e-20
X26_P16	8.256e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X10_P16	X20_P16	X26_P16
A (output stable)	6.774e-05	2.450e-04	4.953e-04	6.409e-04
B (output stable)	2.103e-05	6.524e-05	1.264e-04	1.673e-04
C (output stable)	4.339e-05	1.299e-04	2.946e-04	3.736e-04
A to Z	6.656e-04	2.569e-03	5.326e-03	7.071e-03
B to Z	4.813e-04	1.619e-03	3.495e-03	4.666e-03
C to Z	8.455e-04	2.921e-03	6.144e-03	8.117e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

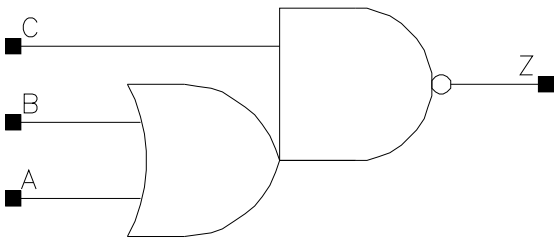
Pin Cycle (vdds)	X3_P16	X10_P16	X20_P16	X26_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X7_P16	0.800	0.952	0.7616
X10_P16	0.800	1.360	1.0880
X13_P16	0.800	1.904	1.5232
X26_P16	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X10_P16	X13_P16
A	0.0006	0.0011	0.0019	0.0024
B	0.0006	0.0012	0.0017	0.0021
C	0.0008	0.0011	0.0016	0.0022
	X26_P16			
A	0.0048			
B	0.0042			
C	0.0042			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X7_P16	X3_P16	X7_P16
A to Z ↓	0.0165	0.0150	5.7705	3.0069
A to Z ↑	0.0247	0.0222	9.6657	4.9724
B to Z ↓	0.0145	0.0127	5.7900	2.9253

B to Z ↑	0.0245	0.0216	9.7133	4.9955
C to Z ↓	0.0135	0.0117	5.4737	2.7932
C to Z ↑	0.0151	0.0130	5.2553	2.7486
	X10_P16	**X13_P16**	**X10_P16**	**X13_P16**
A to Z ↓	0.0147	0.0154	2.0352	1.5537
A to Z ↑	0.0215	0.0235	3.2774	2.5164
B to Z ↓	0.0124	0.0126	2.0267	1.5561
B to Z ↑	0.0208	0.0210	3.2956	2.5299
C to Z ↓	0.0114	0.0115	1.9187	1.4621
C to Z ↑	0.0123	0.0123	1.8060	1.3662
	X26_P16		**X26_P16**	
A to Z ↓	0.0153		0.8029	
A to Z ↑	0.0231		1.2680	
B to Z ↓	0.0124		0.8002	
B to Z ↑	0.0206		1.2757	
C to Z ↓	0.0117		0.7538	
C to Z ↑	0.0121		0.6893	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.289e-07	1.000e-20
X7_P16	2.363e-07	1.000e-20
X10_P16	3.480e-07	1.000e-20
X13_P16	4.696e-07	1.000e-20
X26_P16	9.132e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X7_P16	X10_P16	X13_P16
A (output stable)	2.151e-05	4.508e-05	6.129e-05	1.297e-04
B (output stable)	7.414e-06	1.506e-05	2.167e-05	4.150e-05
C (output stable)	2.172e-04	3.939e-04	5.372e-04	7.666e-04
A to Z	1.342e-03	2.174e-03	3.155e-03	4.620e-03
B to Z	1.085e-03	1.676e-03	2.378e-03	3.227e-03
C to Z	7.572e-04	1.220e-03	1.706e-03	2.394e-03
	X26_P16			
A (output stable)	2.374e-04			
B (output stable)	7.956e-05			
C (output stable)	1.436e-03			
A to Z	8.951e-03			
B to Z	6.146e-03			
C to Z	4.590e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P16	X7_P16	X10_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

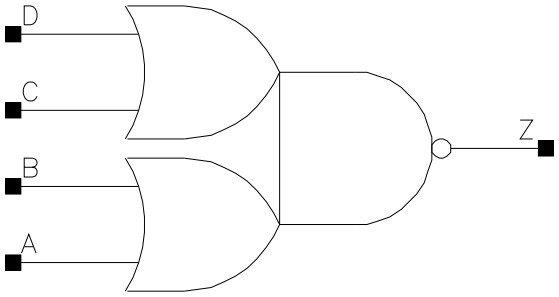
	X26_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X6_P16	0.800	1.360	1.0880
X8_P16	0.800	1.768	1.4144
X11_P16	0.800	2.448	1.9584
X24_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X8_P16	X11_P16
A	0.0006	0.0012	0.0018	0.0023
B	0.0005	0.0011	0.0016	0.0021
C	0.0006	0.0011	0.0016	0.0021
D	0.0005	0.0010	0.0015	0.0019
	X24_P16			
A	0.0049			
B	0.0043			
C	0.0045			
D	0.0041			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X6_P16**	**X3_P16**	**X6_P16**
A to Z ↓	0.0157	0.0181	5.4259	2.9565
A to Z ↑	0.0271	0.0272	12.0039	5.2465
B to Z ↓	0.0141	0.0156	5.3807	2.9649
B to Z ↑	0.0270	0.0248	12.0377	5.2733
C to Z ↓	0.0133	0.0159	5.5332	2.9791
C to Z ↑	0.0189	0.0206	12.0459	5.2698
D to Z ↓	0.0114	0.0125	5.4906	3.0135
D to Z ↑	0.0182	0.0168	12.1006	5.3112
	X8_P16	**X11_P16**	**X8_P16**	**X11_P16**
A to Z ↓	0.0174	0.0176	2.0256	1.5360
A to Z ↑	0.0256	0.0259	3.5153	2.6364
B to Z ↓	0.0152	0.0150	2.0377	1.5387
B to Z ↑	0.0239	0.0239	3.5367	2.6514
C to Z ↓	0.0156	0.0160	2.0519	1.5546
C to Z ↑	0.0193	0.0199	3.5081	2.6554
D to Z ↓	0.0128	0.0127	2.0815	1.5633
D to Z ↑	0.0166	0.0167	3.5416	2.6800
	X24_P16		**X24_P16**	
A to Z ↓	0.0177		0.7532	
A to Z ↑	0.0258		1.2704	
B to Z ↓	0.0150		0.7481	
B to Z ↑	0.0240		1.2777	
C to Z ↓	0.0163		0.7629	
C to Z ↑	0.0197		1.2726	
D to Z ↓	0.0129		0.7612	
D to Z ↑	0.0167		1.2840	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.346e-07	1.000e-20
X6_P16	2.788e-07	1.000e-20
X8_P16	4.010e-07	1.000e-20
X11_P16	5.402e-07	1.000e-20
X24_P16	1.122e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X6_P16	X8_P16	X11_P16
A (output stable)	2.019e-05	7.701e-05	9.805e-05	1.428e-04
B (output stable)	1.381e-05	3.618e-05	4.446e-05	6.249e-05
C (output stable)	3.841e-05	1.738e-04	2.050e-04	3.185e-04
D (output stable)	6.546e-05	1.522e-04	1.967e-04	2.658e-04
A to Z	1.251e-03	2.944e-03	4.072e-03	5.522e-03
B to Z	1.039e-03	2.245e-03	3.105e-03	4.181e-03
C to Z	7.600e-04	2.040e-03	2.789e-03	3.891e-03
D to Z	5.762e-04	1.326e-03	1.882e-03	2.568e-03
	X24_P16			
A (output stable)	2.821e-04			
B (output stable)	1.140e-04			
C (output stable)	6.182e-04			
D (output stable)	5.182e-04			

A to Z	1.134e-02			
B to Z	8.626e-03			
C to Z	7.996e-03			
D to Z	5.350e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

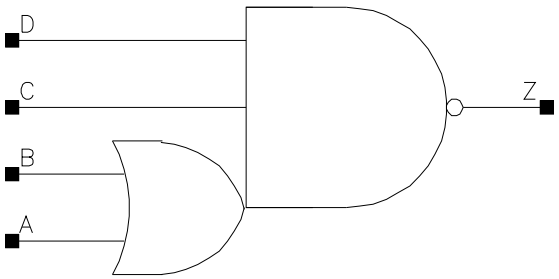
Pin Cycle (vdds)	X3_P16	X6_P16	X8_P16	X11_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X6_P16	0.800	1.360	1.0880
X12_P16	0.800	2.448	1.9584
X18_P16	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X12_P16	X18_P16
A	0.0008	0.0011	0.0022	0.0032
B	0.0006	0.0010	0.0020	0.0030
C	0.0006	0.0012	0.0023	0.0036
D	0.0006	0.0011	0.0022	0.0033

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0231	0.0198	8.1531	4.3916
A to Z ↑	0.0264	0.0219	10.0256	5.0418
B to Z ↓	0.0173	0.0156	8.1801	4.4133
B to Z ↑	0.0221	0.0191	10.0597	5.0757
C to Z ↓	0.0194	0.0197	7.6682	4.1379

C to Z ↑	0.0213	0.0205	5.0626	2.6056
D to Z ↓	0.0207	0.0192	7.7005	4.1559
D to Z ↑	0.0205	0.0188	5.2106	2.6125
	X12_P16	**X18_P16**	**X12_P16**	**X18_P16**
A to Z ↓	0.0202	0.0204	2.2872	1.5460
A to Z ↑	0.0217	0.0216	2.5242	1.6914
B to Z ↓	0.0158	0.0162	2.3007	1.5572
B to Z ↑	0.0188	0.0190	2.5435	1.7042
C to Z ↓	0.0194	0.0196	2.1553	1.4584
C to Z ↑	0.0202	0.0200	1.3277	0.8731
D to Z ↓	0.0192	0.0193	2.1647	1.4644
D to Z ↑	0.0184	0.0184	1.3235	0.8833

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.126e-07	1.000e-20
X6_P16	2.164e-07	1.000e-20
X12_P16	4.171e-07	1.000e-20
X18_P16	6.181e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X6_P16	X12_P16	X18_P16
A (output stable)	8.674e-05	1.781e-04	3.362e-04	4.946e-04
B (output stable)	6.039e-05	1.045e-04	1.926e-04	2.707e-04
C (output stable)	1.567e-05	4.828e-05	7.803e-05	1.106e-04
D (output stable)	3.867e-05	1.047e-04	1.849e-04	2.904e-04
A to Z	1.344e-03	2.114e-03	4.159e-03	6.202e-03
B to Z	9.250e-04	1.440e-03	2.784e-03	4.209e-03
C to Z	1.552e-03	2.877e-03	5.467e-03	8.192e-03
D to Z	1.402e-03	2.371e-03	4.542e-03	6.746e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

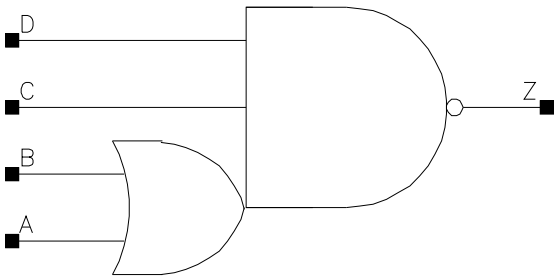
Pin Cycle (vdds)	X3_P16	X6_P16	X12_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X6_P16	0.800	1.360	1.0880
X9_P16	0.800	1.768	1.4144
X12_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X9_P16	X12_P16
A	0.0006	0.0012	0.0019	0.0024
B	0.0006	0.0011	0.0016	0.0024
C	0.0006	0.0011	0.0017	0.0022
D	0.0006	0.0011	0.0016	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0202	0.0208	8.7756	4.3322
A to Z ↑	0.0262	0.0279	10.1574	5.0309
B to Z ↓	0.0175	0.0175	8.6207	4.3544
B to Z ↑	0.0262	0.0261	10.1967	5.0510
C to Z ↓	0.0157	0.0169	8.2855	4.1321

C to Z ↑	0.0167	0.0170	5.5000	2.7083
D to Z ↓	0.0159	0.0155	8.3372	4.1618
D to Z ↑	0.0147	0.0141	5.5491	2.7312
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0211	0.0211	2.9833	2.2663
A to Z ↑	0.0272	0.0277	3.3157	2.5838
B to Z ↓	0.0179	0.0178	2.9853	2.2714
B to Z ↑	0.0258	0.0265	3.3311	2.5978
C to Z ↓	0.0167	0.0170	2.8384	2.1568
C to Z ↑	0.0165	0.0167	1.7861	1.3547
D to Z ↓	0.0158	0.0157	2.8583	2.1728
D to Z ↑	0.0140	0.0138	1.8027	1.3710

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P16	1.184e-07	1.000e-20
X6_P16	2.507e-07	1.000e-20
X9_P16	3.597e-07	1.000e-20
X12_P16	4.841e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	1.221e-05	3.532e-05	4.950e-05	6.458e-05
B (output stable)	6.689e-06	2.942e-05	3.698e-05	5.927e-05
C (output stable)	4.729e-05	1.040e-04	1.477e-04	1.842e-04
D (output stable)	1.074e-04	3.627e-04	4.359e-04	6.730e-04
A to Z	1.408e-03	3.083e-03	4.514e-03	6.023e-03
B to Z	1.159e-03	2.375e-03	3.462e-03	4.624e-03
C to Z	8.777e-04	1.976e-03	2.812e-03	3.831e-03
D to Z	7.143e-04	1.491e-03	2.162e-03	2.858e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

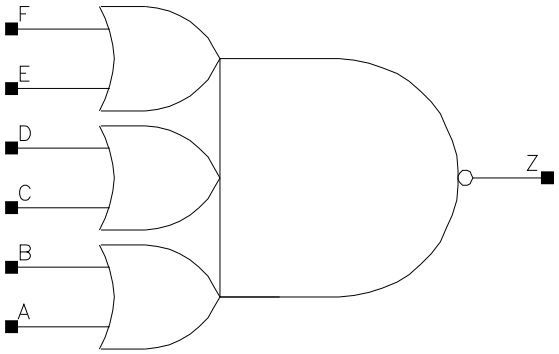
Pin Cycle (vdds)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.224	0.9792
X3_P16	0.800	1.224	0.9792
X5_P16	0.800	2.040	1.6320
X8_P16	0.800	2.720	2.1760
X10_P16	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P16	X3_P16	X5_P16	X8_P16
A	0.0005	0.0006	0.0012	0.0018
B	0.0005	0.0006	0.0011	0.0016
C	0.0005	0.0006	0.0012	0.0017
D	0.0005	0.0005	0.0011	0.0016

E	0.0005	0.0006	0.0011	0.0016
F	0.0004	0.0005	0.0010	0.0015
	X10_P16			
A	0.0024			
B	0.0022			
C	0.0023			
D	0.0021			
E	0.0022			
F	0.0020			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X3_P16**	**X2_P16**	**X3_P16**
A to Z ↓	0.0258	0.0249	9.5670	7.4575
A to Z ↑	0.0366	0.0319	13.9062	9.5757
B to Z ↓	0.0241	0.0230	9.5906	7.4996
B to Z ↑	0.0374	0.0327	13.9375	9.6058
C to Z ↓	0.0250	0.0245	9.6056	7.4732
C to Z ↑	0.0318	0.0285	13.9087	9.7346
D to Z ↓	0.0237	0.0219	9.6949	7.5686
D to Z ↑	0.0334	0.0284	13.9689	9.7621
E to Z ↓	0.0216	0.0211	9.6651	7.5131
E to Z ↑	0.0249	0.0224	13.9289	9.7564
F to Z ↓	0.0198	0.0188	9.7459	7.6160
F to Z ↑	0.0253	0.0221	13.9993	9.8047
	X5_P16	**X8_P16**	**X5_P16**	**X8_P16**
A to Z ↓	0.0263	0.0260	3.9866	2.7175
A to Z ↑	0.0333	0.0322	5.0289	3.3284
B to Z ↓	0.0232	0.0230	4.0066	2.7203
B to Z ↑	0.0317	0.0314	5.0490	3.3410
C to Z ↓	0.0240	0.0248	4.0082	2.7309
C to Z ↑	0.0282	0.0279	5.0818	3.4060
D to Z ↓	0.0209	0.0216	4.0201	2.7360
D to Z ↑	0.0267	0.0273	5.1059	3.4211
E to Z ↓	0.0223	0.0222	4.0417	2.7475
E to Z ↑	0.0229	0.0221	5.0831	3.4186
F to Z ↓	0.0186	0.0187	4.0607	2.7468
F to Z ↑	0.0203	0.0206	5.1182	3.4423
	X10_P16		**X10_P16**	
A to Z ↓	0.0265		2.0632	
A to Z ↑	0.0328		2.5278	
B to Z ↓	0.0234		2.0673	
B to Z ↑	0.0315		2.5389	
C to Z ↓	0.0245		2.0716	
C to Z ↑	0.0281		2.5777	
D to Z ↓	0.0214		2.0772	
D to Z ↑	0.0269		2.5914	
E to Z ↓	0.0224		2.0834	
E to Z ↑	0.0225		2.5703	
F to Z ↓	0.0191		2.0962	
F to Z ↑	0.0206		2.5895	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P16	1.399e-07	1.000e-20
X3_P16	1.957e-07	1.000e-20
X5_P16	3.802e-07	1.000e-20
X8_P16	5.504e-07	1.000e-20
X10_P16	7.345e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P16	X3_P16	X5_P16	X8_P16
A (output stable)	1.438e-05	2.054e-05	7.082e-05	8.513e-05
B (output stable)	6.491e-06	9.498e-06	3.178e-05	3.891e-05
C (output stable)	2.740e-05	4.099e-05	1.098e-04	1.416e-04
D (output stable)	3.759e-05	4.360e-05	1.130e-04	1.443e-04
E (output stable)	2.681e-05	3.393e-05	1.070e-04	1.276e-04
F (output stable)	1.038e-04	1.250e-04	2.280e-04	3.327e-04
A to Z	1.758e-03	2.138e-03	4.355e-03	6.269e-03
B to Z	1.591e-03	1.905e-03	3.645e-03	5.280e-03
C to Z	1.434e-03	1.766e-03	3.431e-03	5.030e-03
D to Z	1.287e-03	1.519e-03	2.801e-03	4.188e-03
E to Z	1.055e-03	1.306e-03	2.670e-03	3.780e-03
F to Z	9.051e-04	1.083e-03	2.034e-03	2.974e-03
	X10_P16			
A (output stable)	1.251e-04			
B (output stable)	5.770e-05			
C (output stable)	2.095e-04			
D (output stable)	2.100e-04			
E (output stable)	1.917e-04			
F (output stable)	4.306e-04			
A to Z	8.486e-03			
B to Z	7.106e-03			
C to Z	6.743e-03			
D to Z	5.522e-03			
E to Z	5.180e-03			
F to Z	4.022e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X2_P16	X3_P16	X5_P16	X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P16			

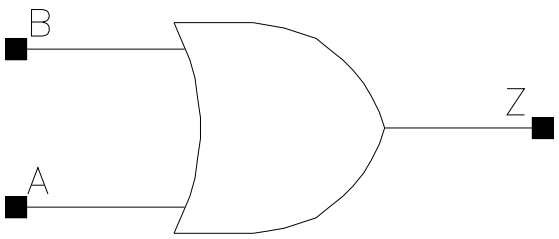
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.544	0.4352
X9_P16	0.800	0.680	0.5440
X19_P16	0.800	1.360	1.0880
X29_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16	X29_P16
A	0.0006	0.0007	0.0013	0.0013
B	0.0005	0.0007	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X9_P16**	**X5_P16**	**X9_P16**
A to Z ↓	0.0418	0.0370	3.5480	1.7930
A to Z ↑	0.0252	0.0265	5.2868	2.6739
B to Z ↓	0.0419	0.0367	3.5492	1.7930
B to Z ↑	0.0241	0.0248	5.2840	2.6735
	X19_P16	**X29_P16**	**X19_P16**	**X29_P16**
A to Z ↓	0.0377	0.0444	0.8611	0.5926
A to Z ↑	0.0264	0.0300	1.2632	0.8476
B to Z ↓	0.0357	0.0429	0.8615	0.5925
B to Z ↑	0.0239	0.0278	1.2613	0.8475

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.079e-07	1.000e-20
X9_P16	1.921e-07	1.000e-20
X19_P16	3.957e-07	1.000e-20
X29_P16	5.011e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16	X29_P16
A (output stable)	1.593e-05	2.824e-05	1.006e-04	1.006e-04
B (output stable)	3.072e-06	4.091e-06	5.609e-05	5.581e-05
A to Z	1.656e-03	2.636e-03	5.576e-03	7.633e-03
B to Z	1.531e-03	2.411e-03	4.850e-03	6.937e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

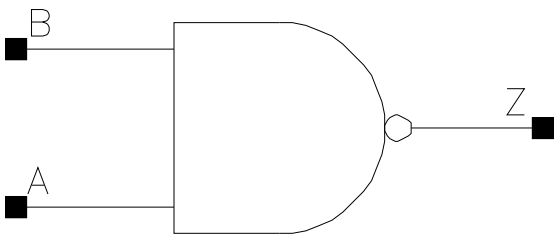
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16	X29_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X9_P16	0.800	0.952	0.7616
X14_P16	0.800	1.088	0.8704
X18_P16	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P16	X9_P16	X14_P16	X18_P16
A	0.0008	0.0007	0.0007	0.0006
B	0.0007	0.0008	0.0008	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X9_P16**	**X5_P16**	**X9_P16**
A to Z ↓	0.0326	0.0376	3.1899	1.7506
A to Z ↑	0.0354	0.0389	5.0687	2.6801
B to Z ↓	0.0336	0.0393	3.1909	1.7504
B to Z ↑	0.0332	0.0374	5.0750	2.6789
	X14_P16	**X18_P16**	**X14_P16**	**X18_P16**
A to Z ↓	0.0417	0.0443	1.2164	0.9222
A to Z ↑	0.0418	0.0431	1.7738	1.3740
B to Z ↓	0.0435	0.0459	1.2174	0.9216
B to Z ↑	0.0403	0.0415	1.7728	1.3748

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	2.334e-07	1.000e-20
X9_P16	2.759e-07	1.000e-20
X14_P16	3.282e-07	1.000e-20
X18_P16	3.585e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X9_P16	X14_P16	X18_P16
A (output stable)	1.269e-05	1.200e-05	1.212e-05	1.229e-05
B (output stable)	4.774e-05	4.441e-05	4.453e-05	4.297e-05
A to Z	3.060e-03	3.928e-03	5.029e-03	5.587e-03
B to Z	2.896e-03	3.782e-03	4.882e-03	5.438e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

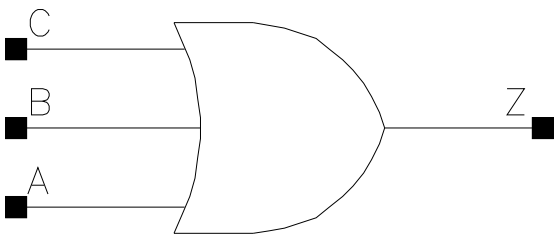
Pin Cycle (vdds)	X5_P16	X9_P16	X14_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.680	0.5440
X10_P16	0.800	0.952	0.7616
X14_P16	0.800	1.496	1.1968
X19_P16	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0005	0.0008	0.0012	0.0020
B	0.0005	0.0007	0.0014	0.0019
C	0.0005	0.0007	0.0013	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0560	0.0501	3.6923	1.7596
A to Z ↑	0.0290	0.0260	5.3127	2.5189
B to Z ↓	0.0547	0.0489	3.6953	1.7616
B to Z ↑	0.0284	0.0248	5.3078	2.5170
C to Z ↓	0.0538	0.0471	3.6947	1.7617
C to Z ↑	0.0272	0.0233	5.3025	2.5141
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0468	0.0455	1.1786	0.9024

A to Z ↑	0.0240	0.0239	1.7212	1.3199
B to Z ↓	0.0469	0.0438	1.1795	0.9032
B to Z ↑	0.0228	0.0230	1.7178	1.3172
C to Z ↓	0.0408	0.0403	1.1787	0.9031
C to Z ↑	0.0206	0.0209	1.7162	1.3164

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.095e-07	1.000e-20
X10_P16	2.126e-07	1.000e-20
X14_P16	3.711e-07	1.000e-20
X19_P16	5.156e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	7.586e-05	1.291e-04	3.107e-04	4.947e-04
B (output stable)	2.527e-07	-1.237e-06	9.103e-05	2.982e-05
C (output stable)	1.518e-06	2.927e-06	3.406e-05	2.049e-05
A to Z	1.961e-03	3.199e-03	5.285e-03	7.628e-03
B to Z	1.825e-03	2.965e-03	4.909e-03	6.776e-03
C to Z	1.703e-03	2.733e-03	4.154e-03	5.925e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

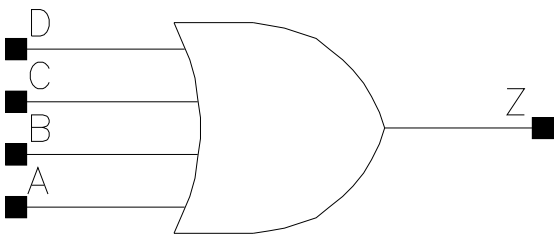
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	1.224	0.9792
X8_P16	0.800	1.496	1.1968
X12_P16	0.800	2.176	1.7408
X15_P16	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X12_P16	X15_P16
A	0.0005	0.0007	0.0012	0.0014
B	0.0005	0.0007	0.0011	0.0013
C	0.0005	0.0007	0.0012	0.0014
D	0.0005	0.0008	0.0011	0.0014

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
A to Z ↓	0.0435	0.0414	5.6030	2.9735
A to Z ↑	0.0263	0.0268	4.9435	2.6411
B to Z ↓	0.0446	0.0421	5.6058	2.9725
B to Z ↑	0.0253	0.0255	4.9460	2.6391
C to Z ↓	0.0459	0.0401	5.6137	2.9696
C to Z ↑	0.0268	0.0259	5.0685	2.6492

D to Z ↓	0.0475	0.0410	5.6171	2.9704
D to Z ↑	0.0260	0.0247	5.0613	2.6485
	X12_P16	**X15_P16**	**X12_P16**	**X15_P16**
A to Z ↓	0.0423	0.0424	2.0594	1.5434
A to Z ↑	0.0273	0.0259	1.6860	1.2926
B to Z ↓	0.0413	0.0406	2.0594	1.5435
B to Z ↑	0.0258	0.0239	1.6842	1.2912
C to Z ↓	0.0407	0.0404	2.0570	1.5412
C to Z ↑	0.0259	0.0247	1.6802	1.3006
D to Z ↓	0.0398	0.0389	2.0582	1.5419
D to Z ↑	0.0244	0.0228	1.6797	1.2989

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	1.531e-07	1.000e-20
X8_P16	2.995e-07	1.000e-20
X12_P16	3.995e-07	1.000e-20
X15_P16	5.754e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	4.629e-04	8.078e-04	1.267e-03	1.701e-03
B (output stable)	4.088e-04	7.075e-04	1.052e-03	1.369e-03
C (output stable)	4.534e-04	7.784e-04	1.194e-03	1.635e-03
D (output stable)	3.946e-04	6.671e-04	9.422e-04	1.263e-03
A to Z	1.869e-03	3.715e-03	5.306e-03	7.033e-03
B to Z	1.762e-03	3.502e-03	4.853e-03	6.312e-03
C to Z	1.845e-03	3.199e-03	4.598e-03	5.882e-03
D to Z	1.746e-03	2.990e-03	4.153e-03	5.236e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

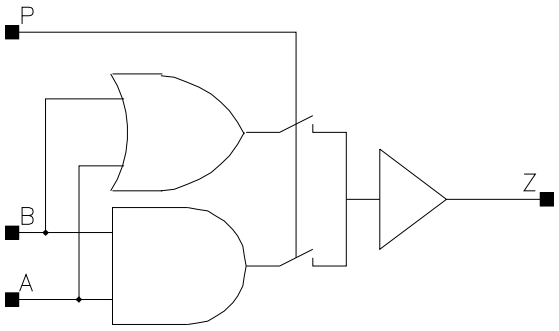
Pin Cycle (vdds)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.952	0.7616
X10_P16	1.600	0.816	1.3056
X14_P16	1.600	1.224	1.9584
X19_P16	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0010	0.0012	0.0024	0.0024
B	0.0010	0.0013	0.0025	0.0025
P	0.0005	0.0008	0.0014	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0518	0.0467	3.6068	1.6805
A to Z ↑	0.0288	0.0332	5.3224	2.5432
B to Z ↓	0.0513	0.0475	3.6269	1.6909
B to Z ↑	0.0300	0.0349	5.3308	2.5453
P to Z ↓	0.0464	0.0446	3.6299	1.6949
P to Z ↑	0.0288	0.0341	5.3312	2.5446
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**

A to Z ↓	0.0432	0.0464	1.1586	0.8658
A to Z ↑	0.0321	0.0337	1.7401	1.3017
B to Z ↓	0.0414	0.0444	1.1730	0.8745
B to Z ↑	0.0319	0.0337	1.7426	1.3040
P to Z ↓	0.0392	0.0429	1.1783	0.8774
P to Z ↑	0.0317	0.0338	1.7438	1.3049

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.720e-07	1.000e-20
X10_P16	3.318e-07	1.000e-20
X14_P16	5.635e-07	1.000e-20
X19_P16	6.299e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	3.886e-05	7.511e-05	1.653e-04	1.606e-04
B (output stable)	1.081e-04	1.701e-04	5.090e-04	4.431e-04
P (output stable)	1.072e-04	1.449e-04	2.472e-04	2.435e-04
A to Z	2.018e-03	3.713e-03	6.105e-03	7.138e-03
B to Z	1.938e-03	3.631e-03	5.645e-03	6.689e-03
P to Z	1.716e-03	3.330e-03	5.318e-03	6.414e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

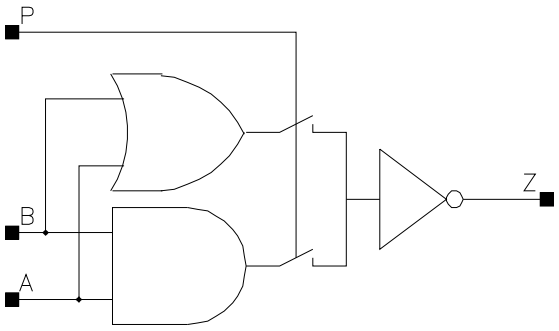
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.600	0.544	0.8704
X10_P16	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P16	X10_P16
A	0.0012	0.0023
B	0.0011	0.0020
P	0.0007	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0172	0.0165	5.6495	2.9566
A to Z ↑	0.0273	0.0258	9.7092	4.9168
B to Z ↓	0.0181	0.0159	5.5903	2.9673
B to Z ↑	0.0270	0.0232	9.6871	4.9840
P to Z ↓	0.0177	0.0146	5.7375	2.9978
P to Z ↑	0.0249	0.0201	9.7943	4.9532

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	1.846e-07	1.000e-20
X10_P16	3.513e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P16	X10_P16
A (output stable)	5.883e-05	1.721e-04
B (output stable)	1.615e-04	4.581e-04
P (output stable)	1.204e-04	2.811e-04
A to Z	1.524e-03	2.737e-03
B to Z	1.392e-03	2.193e-03
P to Z	1.136e-03	1.826e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

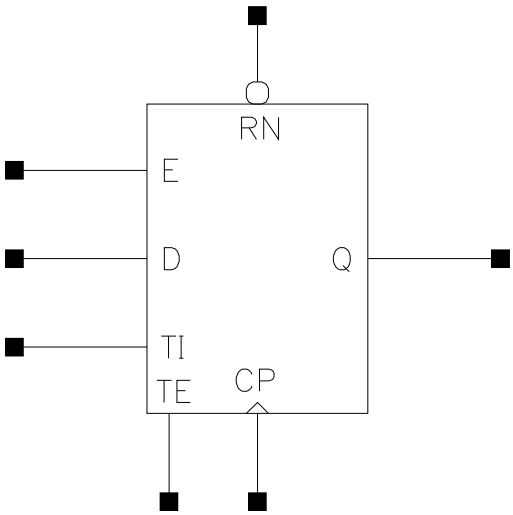
Pin Cycle (vdds)	X5_P16	X10_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.600	2.992	4.7872
X10_P16	1.600	3.128	5.0048
X19_P16	1.600	3.264	5.2224
X23_P16	1.600	3.264	5.2224
X29_P16	1.600	3.536	5.6576
X34_P16	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16	X23_P16
CP	0.0006	0.0006	0.0006	0.0006
D	0.0006	0.0006	0.0006	0.0006
E	0.0012	0.0012	0.0012	0.0012

RN	0.0010	0.0009	0.0010	0.0009
TE	0.0010	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004	0.0004
	X29_P16	X34_P16		
CP	0.0006	0.0006		
D	0.0006	0.0006		
E	0.0012	0.0012		
RN	0.0009	0.0009		
TE	0.0010	0.0010		
TI	0.0004	0.0004		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
CP to Q ↓	0.0634	0.1011	3.3204	1.6484
CP to Q ↑	0.0856	0.1359	5.0216	2.5367
RN to Q ↓	0.0553	0.1001	3.3380	1.6470
	X19_P16	**X23_P16**	**X19_P16**	**X23_P16**
CP to Q ↓	0.1093	0.1100	0.8579	0.6484
CP to Q ↑	0.1407	0.1391	1.2841	1.2558
RN to Q ↓	0.1012	0.1021	0.8581	0.6484
	X29_P16	**X34_P16**	**X29_P16**	**X34_P16**
CP to Q ↓	0.0956	0.0949	0.5660	0.4470
CP to Q ↑	0.1139	0.1148	0.8504	0.8486
RN to Q ↓	0.0895	0.0887	0.5661	0.4471

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P16	X10_P16	X19_P16	X23_P16
CP ↓	min_pulse_width to CP	0.0844	0.0844	0.0844	0.0844
CP ↑	min_pulse_width to CP	0.0527	0.0529	0.0529	0.0529
D ↓	hold_rising to CP	-0.0582	-0.0582	-0.0582	-0.0582
D ↑	hold_rising to CP	-0.0218	-0.0218	-0.0218	-0.0218
D ↓	setup_rising to CP	0.1084	0.1079	0.1084	0.1084
D ↑	setup_rising to CP	0.0492	0.0492	0.0492	0.0492
E ↓	hold_rising to CP	-0.0506	-0.0506	-0.0506	-0.0506
E ↑	hold_rising to CP	-0.0218	-0.0218	-0.0218	-0.0218
E ↓	setup_rising to CP	0.1344	0.1344	0.1344	0.1344
E ↑	setup_rising to CP	0.1052	0.1052	0.1052	0.1052
RN ↓	min_pulse_width to RN	0.0757	0.0664	0.0708	0.0708
RN ↑	recovery_rising to CP	0.0031	0.0037	0.0010	0.0010
RN ↑	removal_rising to CP	0.0064	0.0064	0.0064	0.0064
TE ↓	hold_rising to CP	-0.0285	-0.0285	-0.0285	-0.0285

TE ↑	hold_rising to CP	-0.0142	-0.0142	-0.0142	-0.0142
TE ↓	setup_rising to CP	0.0856	0.0856	0.0861	0.0861
TE ↑	setup_rising to CP	0.1056	0.1056	0.1056	0.1056
TI ↓	hold_rising to CP	-0.0550	-0.0550	-0.0550	-0.0550
TI ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120	-0.0120
TI ↓	setup_rising to CP	0.1037	0.1037	0.1037	0.1037
TI ↑	setup_rising to CP	0.0417	0.0419	0.0419	0.0419
		X29_P16	X34_P16		
CP ↓	min_pulse_width to CP	0.0851	0.0851		
CP ↑	min_pulse_width to CP	0.0528	0.0528		
D ↓	hold_rising to CP	-0.0582	-0.0582		
D ↑	hold_rising to CP	-0.0218	-0.0218		
D ↓	setup_rising to CP	0.1079	0.1079		
D ↑	setup_rising to CP	0.0492	0.0492		
E ↓	hold_rising to CP	-0.0506	-0.0506		
E ↑	hold_rising to CP	-0.0218	-0.0218		
E ↓	setup_rising to CP	0.1344	0.1344		
E ↑	setup_rising to CP	0.1052	0.1052		
RN ↓	min_pulse_width to RN	0.0730	0.0730		
RN ↑	recovery_rising to CP	0.0031	0.0031		
RN ↑	removal_rising to CP	0.0064	0.0064		
TE ↓	hold_rising to CP	-0.0285	-0.0285		
TE ↑	hold_rising to CP	-0.0142	-0.0142		
TE ↓	setup_rising to CP	0.0861	0.0856		
TE ↑	setup_rising to CP	0.1056	0.1056		
TI ↓	hold_rising to CP	-0.0550	-0.0550		
TI ↑	hold_rising to CP	-0.0120	-0.0120		
TI ↓	setup_rising to CP	0.1037	0.1037		
TI ↑	setup_rising to CP	0.0417	0.0417		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	6.277e-07	1.000e-20
X10_P16	7.395e-07	1.000e-20
X19_P16	9.253e-07	1.000e-20
X23_P16	9.755e-07	1.000e-20

X29_P16	1.157e-06	1.000e-20
X34_P16	1.240e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

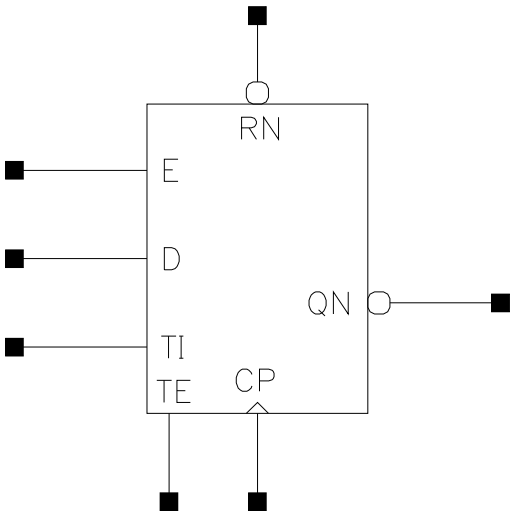
Pin Cycle	X5_P16	X10_P16	X19_P16	X23_P16
Clock 100Mhz Data 0Mhz	8.128e-03	8.116e-03	8.122e-03	8.126e-03
Clock 100Mhz Data 25Mhz	8.403e-03	8.872e-03	9.573e-03	9.633e-03
Clock 100Mhz Data 50Mhz	8.678e-03	9.627e-03	1.102e-02	1.114e-02
Clock = 0 Data 100Mhz	4.813e-03	4.814e-03	4.813e-03	4.813e-03
Clock = 1 Data 100Mhz	1.978e-03	1.978e-03	1.978e-03	1.978e-03
	X29_P16	X34_P16		
Clock 100Mhz Data 0Mhz	8.126e-03	8.127e-03		
Clock 100Mhz Data 25Mhz	1.042e-02	1.061e-02		
Clock 100Mhz Data 50Mhz	1.271e-02	1.309e-02		
Clock = 0 Data 100Mhz	4.813e-03	4.813e-03		
Clock = 1 Data 100Mhz	1.978e-03	1.978e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.600	2.992	4.7872
X10_P16	1.600	3.128	5.0048
X19_P16	1.600	3.264	5.2224
X23_P16	1.600	3.264	5.2224
X29_P16	1.600	3.536	5.6576
X34_P16	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16	X23_P16
CP	0.0006	0.0006	0.0006	0.0006
D	0.0006	0.0006	0.0006	0.0006
E	0.0012	0.0013	0.0013	0.0013

RN	0.0009	0.0009	0.0009	0.0010
TE	0.0010	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004	0.0004
	X29_P16	X34_P16		
CP	0.0006	0.0006		
D	0.0006	0.0006		
E	0.0013	0.0012		
RN	0.0009	0.0009		
TE	0.0010	0.0010		
TI	0.0004	0.0004		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
CP to QN ↓	0.1192	0.1032	3.3246	1.6450
CP to QN ↑	0.0841	0.0802	5.0088	2.5362
RN to QN ↑	0.0827	0.0740	5.0100	2.5387
	X19_P16	**X23_P16**	**X19_P16**	**X23_P16**
CP to QN ↓	0.1085	0.1095	0.8504	0.6490
CP to QN ↑	0.0880	0.0858	1.2857	1.2553
RN to QN ↑	0.0820	0.0796	1.2861	1.2574
	X29_P16	**X34_P16**	**X29_P16**	**X34_P16**
CP to QN ↓	0.1489	0.1463	0.5658	0.4404
CP to QN ↑	0.1134	0.1124	0.8515	0.8483
RN to QN ↑	0.1117	0.1113	0.8506	0.8475

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X5_P16	X10_P16	X19_P16	X23_P16
CP ↓	min_pulse_width to CP	0.0851	0.0851	0.0851	0.0851
CP ↑	min_pulse_width to CP	0.0528	0.0528	0.0528	0.0542
D ↓	hold_rising to CP	-0.0582	-0.0582	-0.0582	-0.0582
D ↑	hold_rising to CP	-0.0218	-0.0218	-0.0218	-0.0218
D ↓	setup_rising to CP	0.1079	0.1079	0.1079	0.1079
D ↑	setup_rising to CP	0.0492	0.0492	0.0492	0.0492
E ↓	hold_rising to CP	-0.0506	-0.0506	-0.0506	-0.0506
E ↑	hold_rising to CP	-0.0218	-0.0218	-0.0218	-0.0218
E ↓	setup_rising to CP	0.1344	0.1371	0.1371	0.1371
E ↑	setup_rising to CP	0.1052	0.1052	0.1052	0.1052
RN ↓	min_pulse_width to RN	0.0686	0.0708	0.0779	0.0779
RN ↑	recovery_rising to CP	0.0037	0.0031	0.0031	0.0031
RN ↑	removal_rising to CP	0.0064	0.0064	0.0064	0.0064
TE ↓	hold_rising to CP	-0.0285	-0.0285	-0.0285	-0.0285

TE ↑	hold_rising to CP	-0.0142	-0.0142	-0.0142	-0.0142
TE ↓	setup_rising to CP	0.0856	0.0861	0.0856	0.0856
TE ↑	setup_rising to CP	0.1056	0.1056	0.1056	0.1056
TI ↓	hold_rising to CP	-0.0550	-0.0550	-0.0550	-0.0550
TI ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120	-0.0120
TI ↓	setup_rising to CP	0.1037	0.1037	0.1037	0.1037
TI ↑	setup_rising to CP	0.0417	0.0417	0.0417	0.0417
		X29_P16	X34_P16		
CP ↓	min_pulse_width to CP	0.0844	0.0844		
CP ↑	min_pulse_width to CP	0.0529	0.0529		
D ↓	hold_rising to CP	-0.0582	-0.0582		
D ↑	hold_rising to CP	-0.0218	-0.0218		
D ↓	setup_rising to CP	0.1084	0.1084		
D ↑	setup_rising to CP	0.0492	0.0492		
E ↓	hold_rising to CP	-0.0506	-0.0506		
E ↑	hold_rising to CP	-0.0218	-0.0218		
E ↓	setup_rising to CP	0.1371	0.1344		
E ↑	setup_rising to CP	0.1052	0.1052		
RN ↓	min_pulse_width to RN	0.0686	0.0686		
RN ↑	recovery_rising to CP	0.0010	0.0010		
RN ↑	removal_rising to CP	0.0064	0.0064		
TE ↓	hold_rising to CP	-0.0285	-0.0285		
TE ↑	hold_rising to CP	-0.0142	-0.0142		
TE ↓	setup_rising to CP	0.0861	0.0861		
TE ↑	setup_rising to CP	0.1056	0.1056		
TI ↓	hold_rising to CP	-0.0550	-0.0550		
TI ↑	hold_rising to CP	-0.0120	-0.0120		
TI ↓	setup_rising to CP	0.1037	0.1037		
TI ↑	setup_rising to CP	0.0419	0.0420		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P16	6.253e-07	1.000e-20
X10_P16	7.300e-07	1.000e-20
X19_P16	9.094e-07	1.000e-20
X23_P16	9.741e-07	1.000e-20

X29_P16	1.125e-06	1.000e-20
X34_P16	1.218e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

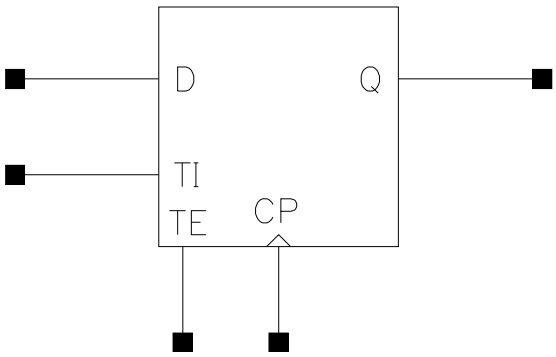
Pin Cycle	X5_P16	X10_P16	X19_P16	X23_P16
Clock 100Mhz Data 0Mhz	7.978e-03	7.985e-03	7.987e-03	7.986e-03
Clock 100Mhz Data 25Mhz	8.380e-03	8.773e-03	9.499e-03	9.540e-03
Clock 100Mhz Data 50Mhz	8.783e-03	9.561e-03	1.101e-02	1.109e-02
Clock = 0 Data 100Mhz	4.800e-03	4.800e-03	4.800e-03	4.800e-03
Clock = 1 Data 100Mhz	1.978e-03	1.979e-03	1.979e-03	1.979e-03
	X29_P16	X34_P16		
Clock 100Mhz Data 0Mhz	7.986e-03	7.986e-03		
Clock 100Mhz Data 25Mhz	1.038e-02	1.057e-02		
Clock 100Mhz Data 50Mhz	1.278e-02	1.315e-02		
Clock = 0 Data 100Mhz	4.800e-03	4.799e-03		
Clock = 1 Data 100Mhz	1.979e-03	1.979e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P16	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P16	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P16	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P16	C8T28SOI_LLHF_-SDFPQX3_P16	C8T28SOIDV_LL_-SDFPQX5_P16	C8T28SOIDV_LL_-SDFPQX10_P16
CP	0.0008	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P16	C8T28SOIDV_LL_-SDFPQX23_P16	C8T28SOIDV_LL_-SDFPQX29_P16	
CP	0.0005	0.0005	0.0005	
D	0.0005	0.0005	0.0005	
TE	0.0010	0.0010	0.0010	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P16	**C8T28SOI_LLHF_-SDFPQX3_P16**	**C8T28SOI_LL_-SDFPQX5_P16**	**C8T28SOI_LLHF_-SDFPQX3_P16**
CP to Q ↓	0.0673	0.0578	3.5062	5.3609
CP to Q ↑	0.0630	0.0732	5.0617	7.8588
	C8T28SOIDV_LL_-SDFPQX5_P16	**C8T28SOIDV_LL_-SDFPQX10_P16**	**C8T28SOIDV_LL_-SDFPQX5_P16**	**C8T28SOIDV_LL_-SDFPQX10_P16**
CP to Q ↓	0.0596	0.0827	3.3185	1.5930
CP to Q ↑	0.0739	0.1078	5.0142	2.5048
	C8T28SOIDV_LL_-SDFPQX19_P16	**C8T28SOIDV_LL_-SDFPQX23_P16**	**C8T28SOIDV_LL_-SDFPQX19_P16**	**C8T28SOIDV_LL_-SDFPQX23_P16**
CP to Q ↓	0.0901	0.0929	0.8338	0.6432
CP to Q ↑	0.1143	0.1167	1.2684	1.2570
	C8T28SOIDV_LL_-SDFPQX29_P16		**C8T28SOIDV_LL_-SDFPQX29_P16**	
CP to Q ↓	0.0894		0.5598	
CP to Q ↑	0.1088		0.8414	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P16	C8T28SOI_-LLHF_-SDFPQX3_P16	C8T28SOIDV_-LL_SDFPQX5_-P16	C8T28SOIDV_-LL_SDFPQX10_-P16
CP ↓	min_pulse_width to CP	0.1101	0.1084	0.0973	0.0973
CP ↑	min_pulse_width to CP	0.0545	0.0453	0.0481	0.0435
D ↓	hold_rising to CP	-0.0539	-0.1066	-0.0143	-0.0169
D ↑	hold_rising to CP	-0.0137	-0.0110	-0.0013	-0.0013
D ↓	setup_rising to CP	0.0954	0.1559	0.0693	0.0693
D ↑	setup_rising to CP	0.0417	0.0433	0.0319	0.0319
TE ↓	hold_rising to CP	-0.0333	-0.0355	-0.0127	-0.0127
TE ↑	hold_rising to CP	-0.0114	-0.0083	-0.0114	-0.0114
TE ↓	setup_rising to CP	0.0928	0.1268	0.0636	0.0636
TE ↑	setup_rising to CP	0.1154	0.1492	0.1208	0.1182

TI ↓	hold_rising to CP	-0.0740	-0.1029	-0.0613	-0.0613
TI ↑	hold_rising to CP	-0.0117	-0.0104	-0.0126	-0.0126
TI ↓	setup_rising to CP	0.1141	0.1458	0.1148	0.1148
TI ↑	setup_rising to CP	0.0417	0.0361	0.0433	0.0417
		C8T28SOIDV_-LL_SDFPQX19_-P16	C8T28SOIDV_-LL_SDFPQX23_-P16	C8T28SOIDV_-LL_SDFPQX29_-P16	
CP ↓	min_pulse_width to CP	0.0973	0.0973	0.0973	
CP ↑	min_pulse_width to CP	0.0435	0.0470	0.0482	
D ↓	hold_rising to CP	-0.0169	-0.0169	-0.0165	
D ↑	hold_rising to CP	-0.0013	-0.0013	-0.0013	
D ↓	setup_rising to CP	0.0693	0.0693	0.0689	
D ↑	setup_rising to CP	0.0319	0.0319	0.0319	
TE ↓	hold_rising to CP	-0.0127	-0.0127	-0.0127	
TE ↑	hold_rising to CP	-0.0114	-0.0114	-0.0114	
TE ↓	setup_rising to CP	0.0636	0.0636	0.0636	
TE ↑	setup_rising to CP	0.1182	0.1182	0.1203	
TI ↓	hold_rising to CP	-0.0613	-0.0613	-0.0613	
TI ↑	hold_rising to CP	-0.0126	-0.0126	-0.0126	
TI ↓	setup_rising to CP	0.1148	0.1148	0.1140	
TI ↑	setup_rising to CP	0.0417	0.0417	0.0417	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P16	5.079e-07	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P16	4.562e-07	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P16	4.793e-07	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P16	6.223e-07	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P16	7.464e-07	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P16	8.047e-07	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P16	9.376e-07	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P16	C8T28SOI_LLHF_-SDFPQX3_P16	C8T28SOIDV_LL_-SDFPQX5_P16	C8T28SOIDV_LL_-SDFPQX10_P16
Clock 100Mhz Data 0Mhz	7.576e-03	7.375e-03	7.082e-03	6.930e-03
Clock 100Mhz Data 25Mhz	7.319e-03	7.104e-03	6.959e-03	7.327e-03
Clock 100Mhz Data 50Mhz	7.061e-03	6.833e-03	6.836e-03	7.724e-03

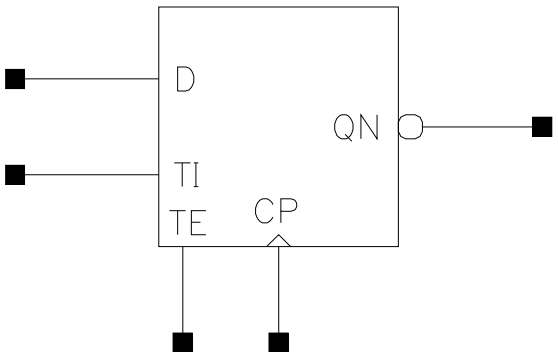
Clock = 0 Data 100Mhz	3.660e-03	3.775e-03	3.620e-03	3.540e-03
Clock = 1 Data 100Mhz	8.066e-05	5.318e-04	3.810e-04	3.056e-04
	C8T28SOIDV_LL_-SDFPQX19_P16	C8T28SOIDV_LL_-SDFPQX23_P16	C8T28SOIDV_LL_-SDFPQX29_P16	
Clock 100Mhz Data 0Mhz	6.842e-03	6.784e-03	6.744e-03	
Clock 100Mhz Data 25Mhz	7.823e-03	7.851e-03	8.442e-03	
Clock 100Mhz Data 50Mhz	8.803e-03	8.918e-03	1.014e-02	
Clock = 0 Data 100Mhz	3.490e-03	3.456e-03	3.436e-03	
Clock = 1 Data 100Mhz	2.603e-04	2.302e-04	2.085e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P16	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P16	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P16	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P16	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P16	C8T28SOI_LLHF_-SDFPQNX3_P16	C8T28SOIDV_LL_-SDFPQNX5_P16	C8T28SOIDV_LL_-SDFPQNX10_P16

CP	0.0008	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P16	C8T28SOIDV_LL_-SDFPQNX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P16	**C8T28SOI_LLHF_-SDFPQNX3_P16**	**C8T28SOI_LL_-SDFPQNX5_P16**	**C8T28SOI_LLHF_-SDFPQNX3_P16**
CP to QN ↓	0.0835	0.0900	3.3447	4.9941
CP to QN ↑	0.0728	0.0696	5.4875	7.6523
	C8T28SOIDV_LL_-SDFPQNX5_P16	**C8T28SOIDV_LL_-SDFPQNX10_P16**	**C8T28SOIDV_LL_-SDFPQNX5_P16**	**C8T28SOIDV_LL_-SDFPQNX10_P16**
CP to QN ↓	0.0926	0.0869	3.2366	1.6086
CP to QN ↑	0.0671	0.0741	4.9586	2.5089
	C8T28SOIDV_LL_-SDFPQNX19_P16	**C8T28SOIDV_LL_-SDFPQNX29_P16**	**C8T28SOIDV_LL_-SDFPQNX19_P16**	**C8T28SOIDV_LL_-SDFPQNX29_P16**
CP to QN ↓	0.0976	0.1137	0.8439	0.5723
CP to QN ↑	0.0870	0.0977	1.2900	0.8480

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P16	C8T28SOI_-LLHF_-SDFPQNX3_P16	C8T28SOIDV_-LL_SDFPQNX5_-P16	C8T28SOIDV_-LL_-SDFPQNX10_-P16
CP ↓	min_pulse_width to CP	0.1101	0.1042	0.0973	0.0973
CP ↑	min_pulse_width to CP	0.0437	0.0406	0.0435	0.0482
D ↓	hold_rising to CP	-0.0534	-0.1066	-0.0169	-0.0143
D ↑	hold_rising to CP	-0.0137	-0.0110	-0.0039	-0.0013
D ↓	setup_rising to CP	0.0954	0.1533	0.0689	0.0693
D ↑	setup_rising to CP	0.0417	0.0433	0.0319	0.0319
TE ↓	hold_rising to CP	-0.0333	-0.0355	-0.0127	-0.0127
TE ↑	hold_rising to CP	-0.0114	-0.0083	-0.0120	-0.0114
TE ↓	setup_rising to CP	0.0928	0.1241	0.0636	0.0636
TE ↑	setup_rising to CP	0.1150	0.1470	0.1208	0.1208
TI ↓	hold_rising to CP	-0.0740	-0.1029	-0.0613	-0.0613
TI ↑	hold_rising to CP	-0.0117	-0.0104	-0.0120	-0.0126
TI ↓	setup_rising to CP	0.1141	0.1461	0.1140	0.1148

TI ↑	setup_rising to CP	0.0417	0.0361	0.0382	0.0417
		C8T28SOIDV_-LL_-SDFPQNX19_-P16	C8T28SOIDV_-LL_-SDFPQNX29_-P16		
CP ↓	min_pulse_width to CP	0.0973	0.0973		
CP ↑	min_pulse_width to CP	0.0528	0.0470		
D ↓	hold_rising to CP	-0.0143	-0.0169		
D ↑	hold_rising to CP	-0.0013	-0.0013		
D ↓	setup_rising to CP	0.0693	0.0693		
D ↑	setup_rising to CP	0.0319	0.0319		
TE ↓	hold_rising to CP	-0.0127	-0.0127		
TE ↑	hold_rising to CP	-0.0114	-0.0114		
TE ↓	setup_rising to CP	0.0636	0.0636		
TE ↑	setup_rising to CP	0.1182	0.1208		
TI ↓	hold_rising to CP	-0.0613	-0.0613		
TI ↑	hold_rising to CP	-0.0126	-0.0126		
TI ↓	setup_rising to CP	0.1148	0.1148		
TI ↑	setup_rising to CP	0.0417	0.0417		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P16	5.037e-07	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P16	4.619e-07	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P16	4.839e-07	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P16	6.108e-07	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P16	7.474e-07	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P16	1.053e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P16	C8T28SOI_LLHF_-SDFPQNX3_P16	C8T28SOIDV_LL_-SDFPQNX5_P16	C8T28SOIDV_LL_-SDFPQNX10_P16
Clock 100Mhz Data 0Mhz	7.626e-03	7.444e-03	7.126e-03	6.955e-03
Clock 100Mhz Data 25Mhz	7.334e-03	7.204e-03	6.947e-03	7.279e-03
Clock 100Mhz Data 50Mhz	7.041e-03	6.963e-03	6.769e-03	7.603e-03
Clock = 0 Data 100Mhz	3.714e-03	3.837e-03	3.683e-03	3.601e-03
Clock = 1 Data 100Mhz	9.853e-05	5.437e-04	3.996e-04	3.276e-04

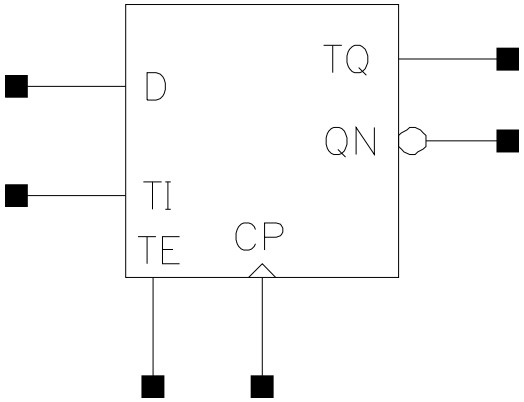
	C8T28SOIDV_LL_-SDFPQNX19_P16	C8T28SOIDV_LL_-SDFPQNX29_P16		
Clock 100Mhz Data 0Mhz	6.856e-03	6.788e-03		
Clock 100Mhz Data 25Mhz	7.889e-03	8.993e-03		
Clock 100Mhz Data 50Mhz	8.923e-03	1.120e-02		
Clock = 0 Data 100Mhz	3.548e-03	3.516e-03		
Clock = 1 Data 100Mhz	2.844e-04	2.556e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P16	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P16	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P16	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P16	C8T28SOI_LLHF_-SDFPQNTX3_P16	C8T28SOIDV_LL_-SDFPQNTX5_P16	C8T28SOIDV_LL_-SDFPQNTX10_P16
CP	0.0008	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P16	C8T28SOIDV_LL_-SDFPQNTX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNTX5_P16	**C8T28SOI_LLHF_-SDFPQNTX3_P16**	**C8T28SOI_LL_-SDFPQNTX5_P16**	**C8T28SOI_LLHF_-SDFPQNTX3_P16**
CP to QN ↓	0.0942	0.0985	3.4639	5.0783
CP to QN ↑	0.0943	0.0870	5.4823	7.6606
CP to TQ ↓	0.0773	0.0608	9.0488	5.8877
CP to TQ ↑	0.0788	0.0726	25.8745	13.9251
	C8T28SOIDV_LL_-SDFPQNTX5_P16	**C8T28SOIDV_LL_-SDFPQNTX10_P16**	**C8T28SOIDV_LL_-SDFPQNTX5_P16**	**C8T28SOIDV_LL_-SDFPQNTX10_P16**
CP to QN ↓	0.0994	0.0965	3.1822	1.6251
CP to QN ↑	0.0797	0.0806	4.9543	2.5132
CP to TQ ↓	0.0559	0.0585	5.8272	6.0924
CP to TQ ↑	0.0738	0.0756	10.9726	11.5078
	C8T28SOIDV_LL_-SDFPQNTX19_P16	**C8T28SOIDV_LL_-SDFPQNTX29_P16**	**C8T28SOIDV_LL_-SDFPQNTX19_P16**	**C8T28SOIDV_LL_-SDFPQNTX29_P16**
CP to QN ↓	0.0996	0.1164	0.8409	0.5737
CP to QN ↑	0.0879	0.1041	1.2801	0.8451
CP to TQ ↓	0.0610	0.0591	5.9591	6.1321
CP to TQ ↑	0.0779	0.0784	11.6825	15.1144

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_-P16	C8T28SOI_-LLHF_-SDFPQNTX3_-P16	C8T28SOIDV_-LL_-SDFPQNTX5_-P16	C8T28SOIDV_-LL_-SDFPQNTX10_-P16
CP ↓	min_pulse_width to CP	0.1101	0.1043	0.0973	0.0973
CP ↑	min_pulse_width to CP	0.0592	0.0499	0.0482	0.0496
D ↓	hold_rising to CP	-0.0539	-0.1039	-0.0169	-0.0143
D ↑	hold_rising to CP	-0.0137	-0.0110	-0.0013	-0.0013
D ↓	setup_rising to CP	0.0954	0.1538	0.0689	0.0693

D ↑	setup_rising to CP	0.0417	0.0466	0.0319	0.0319
TE ↓	hold_rising to CP	-0.0333	-0.0350	-0.0127	-0.0127
TE ↑	hold_rising to CP	-0.0114	-0.0116	-0.0093	-0.0114
TE ↓	setup_rising to CP	0.0928	0.1241	0.0636	0.0636
TE ↑	setup_rising to CP	0.1154	0.1470	0.1208	0.1182
TI ↓	hold_rising to CP	-0.0740	-0.1014	-0.0613	-0.0613
TI ↑	hold_rising to CP	-0.0117	-0.0104	-0.0120	-0.0126
TI ↓	setup_rising to CP	0.1127	0.1461	0.1140	0.1148
TI ↑	setup_rising to CP	0.0417	0.0361	0.0382	0.0417
		C8T28SOIDV_-LL_-SDFPQNTX19_-P16	C8T28SOIDV_-LL_-SDFPQNTX29_-P16		
CP ↓	min_pulse_width to CP	0.0973	0.0973		
CP ↑	min_pulse_width to CP	0.0543	0.0482		
D ↓	hold_rising to CP	-0.0143	-0.0169		
D ↑	hold_rising to CP	-0.0013	-0.0013		
D ↓	setup_rising to CP	0.0693	0.0693		
D ↑	setup_rising to CP	0.0319	0.0319		
TE ↓	hold_rising to CP	-0.0127	-0.0127		
TE ↑	hold_rising to CP	-0.0114	-0.0114		
TE ↓	setup_rising to CP	0.0636	0.0636		
TE ↑	setup_rising to CP	0.1208	0.1208		
TI ↓	hold_rising to CP	-0.0613	-0.0613		
TI ↑	hold_rising to CP	-0.0126	-0.0126		
TI ↓	setup_rising to CP	0.1148	0.1148		
TI ↑	setup_rising to CP	0.0417	0.0417		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P16	5.322e-07	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P16	4.918e-07	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P16	5.141e-07	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P16	5.901e-07	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P16	7.444e-07	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P16	1.076e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

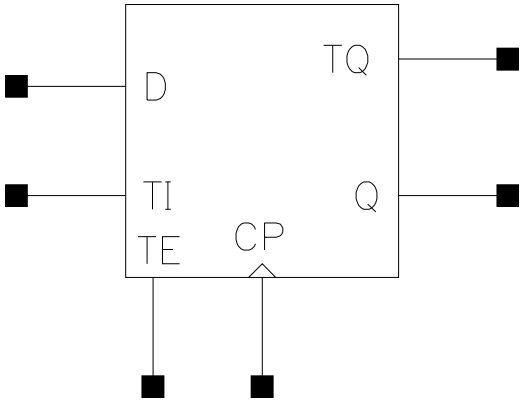
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P16	C8T28SOI_LLHF_-SDFPQNTX3_P16	C8T28SOIDV_LL_-SDFPQNTX5_P16	C8T28SOIDV_LL_-SDFPQNTX10_P16
Clock 100Mhz Data 0Mhz	7.539e-03	7.381e-03	7.085e-03	6.927e-03
Clock 100Mhz Data 25Mhz	7.586e-03	7.388e-03	7.140e-03	7.244e-03
Clock 100Mhz Data 50Mhz	7.633e-03	7.395e-03	7.196e-03	7.561e-03
Clock = 0 Data 100Mhz	3.659e-03	3.783e-03	3.633e-03	3.551e-03
Clock = 1 Data 100Mhz	3.668e-05	5.148e-04	3.567e-04	2.778e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P16	C8T28SOIDV_LL_-SDFPQNTX29_P16		
Clock 100Mhz Data 0Mhz	6.833e-03	6.768e-03		
Clock 100Mhz Data 25Mhz	7.812e-03	9.139e-03		
Clock 100Mhz Data 50Mhz	8.790e-03	1.151e-02		
Clock = 0 Data 100Mhz	3.502e-03	3.470e-03		
Clock = 1 Data 100Mhz	2.304e-04	1.989e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P16	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P16	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P16	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P16	C8T28SOI_LLHF_-SDFPQTX3_P16	C8T28SOIDV_LL_-SDFPQTX5_P16	C8T28SOIDV_LL_-SDFPQTX10_P16
CP	0.0008	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P16	C8T28SOIDV_LL_-SDFPQTX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQTX5_P16	**C8T28SOI_LLHF_-SDFPQTX3_P16**	**C8T28SOI_LL_-SDFPQTX5_P16**	**C8T28SOI_LLHF_-SDFPQTX3_P16**
CP to Q ↓	0.0797	0.0730	3.7478	5.5849
CP to Q ↑	0.0686	0.0740	5.1079	7.9741
CP to TQ ↓	0.0960	0.0727	9.8683	6.0873
CP to TQ ↑	0.0873	0.0781	26.0770	14.1324
	C8T28SOIDV_LL_-SDFPQTX5_P16	**C8T28SOIDV_LL_-SDFPQTX10_P16**	**C8T28SOIDV_LL_-SDFPQTX5_P16**	**C8T28SOIDV_LL_-SDFPQTX10_P16**
CP to Q ↓	0.0653	0.0852	3.4168	1.6028
CP to Q ↑	0.0767	0.1098	5.0904	2.5101
CP to TQ ↓	0.0653	0.0881	6.0246	6.0991
CP to TQ ↑	0.0791	0.1143	12.0634	11.9806
	C8T28SOIDV_LL_-SDFPQTX19_P16	**C8T28SOIDV_LL_-SDFPQTX29_P16**	**C8T28SOIDV_LL_-SDFPQTX19_P16**	**C8T28SOIDV_LL_-SDFPQTX29_P16**
CP to Q ↓	0.0924	0.1018	0.8382	0.5439
CP to Q ↑	0.1153	0.1139	1.2726	0.8379
CP to TQ ↓	0.0970	0.0622	6.1589	6.3145
CP to TQ ↑	0.1221	0.0800	12.0237	15.1170

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P16	C8T28SOI_-LLHF_-SDFPQTX3_P16	C8T28SOIDV_-LL_SDFPQTX5_-P16	C8T28SOIDV_-LL_-SDFPQTX10_-P16
CP ↓	min_pulse_width to CP	0.1101	0.1043	0.0973	0.0973
CP ↑	min_pulse_width to CP	0.0688	0.0545	0.0528	0.0435
D ↓	hold_rising to CP	-0.0534	-0.1066	-0.0143	-0.0169
D ↑	hold_rising to CP	-0.0142	-0.0110	-0.0013	-0.0013
D ↓	setup_rising to CP	0.0954	0.1533	0.0693	0.0693

D ↑	setup_rising to CP	0.0417	0.0433	0.0319	0.0319
TE ↓	hold_rising to CP	-0.0333	-0.0355	-0.0127	-0.0127
TE ↑	hold_rising to CP	-0.0114	-0.0083	-0.0114	-0.0114
TE ↓	setup_rising to CP	0.0928	0.1241	0.0636	0.0636
TE ↑	setup_rising to CP	0.1154	0.1470	0.1208	0.1182
TI ↓	hold_rising to CP	-0.0740	-0.1014	-0.0613	-0.0613
TI ↑	hold_rising to CP	-0.0117	-0.0104	-0.0126	-0.0126
TI ↓	setup_rising to CP	0.1141	0.1468	0.1148	0.1148
TI ↑	setup_rising to CP	0.0417	0.0361	0.0433	0.0417
		C8T28SOIDV_-LL_-SDFPQTX19_-P16	C8T28SOIDV_-LL_-SDFPQTX29_-P16		
CP ↓	min_pulse_width to CP	0.0973	0.0973		
CP ↑	min_pulse_width to CP	0.0435	0.0543		
D ↓	hold_rising to CP	-0.0169	-0.0169		
D ↑	hold_rising to CP	-0.0013	-0.0013		
D ↓	setup_rising to CP	0.0693	0.0689		
D ↑	setup_rising to CP	0.0319	0.0319		
TE ↓	hold_rising to CP	-0.0127	-0.0127		
TE ↑	hold_rising to CP	-0.0114	-0.0114		
TE ↓	setup_rising to CP	0.0636	0.0636		
TE ↑	setup_rising to CP	0.1182	0.1203		
TI ↓	hold_rising to CP	-0.0613	-0.0613		
TI ↑	hold_rising to CP	-0.0126	-0.0126		
TI ↓	setup_rising to CP	0.1148	0.1140		
TI ↑	setup_rising to CP	0.0417	0.0433		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P16	5.370e-07	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P16	4.917e-07	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P16	5.109e-07	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P16	6.517e-07	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P16	7.872e-07	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P16	9.919e-07	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

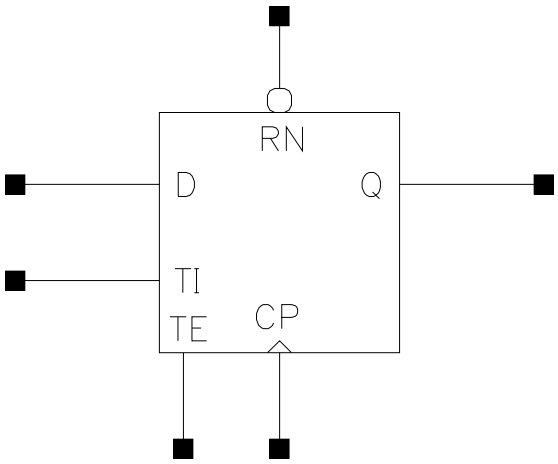
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P16	C8T28SOI_LLHF_-SDFPQTX3_P16	C8T28SOIDV_LL_-SDFPQTX5_P16	C8T28SOIDV_LL_-SDFPQTX10_P16
Clock 100Mhz Data 0Mhz	7.531e-03	7.345e-03	7.058e-03	6.907e-03
Clock 100Mhz Data 25Mhz	7.559e-03	7.326e-03	7.114e-03	7.488e-03
Clock 100Mhz Data 50Mhz	7.588e-03	7.306e-03	7.171e-03	8.070e-03
Clock = 0 Data 100Mhz	3.664e-03	3.787e-03	3.630e-03	3.548e-03
Clock = 1 Data 100Mhz	3.909e-05	5.149e-04	3.570e-04	2.781e-04
	C8T28SOIDV_LL_-SDFPQTX19_P16	C8T28SOIDV_LL_-SDFPQTX29_P16		
Clock 100Mhz Data 0Mhz	6.822e-03	6.769e-03		
Clock 100Mhz Data 25Mhz	8.010e-03	8.675e-03		
Clock 100Mhz Data 50Mhz	9.198e-03	1.058e-02		
Clock = 0 Data 100Mhz	3.496e-03	3.467e-03		
Clock = 1 Data 100Mhz	2.308e-04	1.993e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P16	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P16	C8T28SOI_LLHF_-SDFPRQX3_P16	C8T28SOIDV_LL_-SDFPRQX5_P16	C8T28SOIDV_LL_-SDFPRQX10_P16
CP	0.0008	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
RN	0.0009	0.0008	0.0010	0.0009
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P16	C8T28SOIDV_LL_-SDFPRQX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0009	0.0009		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P16	**C8T28SOI_LLHF_-SDFPRQX3_P16**	**C8T28SOI_LL_-SDFPRQX5_P16**	**C8T28SOI_LLHF_-SDFPRQX3_P16**
CP to Q ↓	0.0767	0.0697	3.5403	5.3943
CP to Q ↑	0.0655	0.0732	5.0668	7.7726
RN to Q ↓	0.0697	0.0683	3.2509	5.0074
	C8T28SOIDV_LL_-SDFPRQX5_P16	**C8T28SOIDV_LL_-SDFPRQX10_P16**	**C8T28SOIDV_LL_-SDFPRQX5_P16**	**C8T28SOIDV_LL_-SDFPRQX10_P16**
CP to Q ↓	0.0603	0.0848	3.3083	1.6111
CP to Q ↑	0.0770	0.1116	5.0110	2.5132
RN to Q ↓	0.0572	0.0882	3.2876	1.6116
	C8T28SOIDV_LL_-SDFPRQX19_P16	**C8T28SOIDV_LL_-SDFPRQX29_P16**	**C8T28SOIDV_LL_-SDFPRQX19_P16**	**C8T28SOIDV_LL_-SDFPRQX29_P16**
CP to Q ↓	0.0909	0.0926	0.8356	0.5707
CP to Q ↑	0.1171	0.1221	1.2894	0.8771
RN to Q ↓	0.0944	0.0960	0.8356	0.5704

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P16	C8T28SOI_-LLHF_-SDFPRQX3_P16	C8T28SOIDV_-LL_SDFPRQX5_-P16	C8T28SOIDV_-LL_-SDFPRQX10_-P16
CP ↓	min_pulse_width to CP	0.1118	0.1043	0.0997	0.0997
CP ↑	min_pulse_width to CP	0.0592	0.0546	0.0482	0.0483
D ↓	hold_rising to CP	-0.0507	-0.1044	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0169	-0.0169	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0986	0.1510	0.0684	0.0684
D ↑	setup_rising to CP	0.0438	0.0465	0.0319	0.0319
RN ↓	min_pulse_width to RN	0.0757	0.0735	0.0659	0.0610
RN ↑	recovery_rising to CP	0.0108	0.0076	0.0080	0.0080

RN ↑	removal_rising to CP	0.0021	0.0021	0.0021	0.0021
TE ↓	hold_rising to CP	-0.0359	-0.0408	-0.0126	-0.0126
TE ↑	hold_rising to CP	-0.0147	-0.0142	-0.0169	-0.0169
TE ↓	setup_rising to CP	0.0928	0.1245	0.0668	0.0668
TE ↑	setup_rising to CP	0.1150	0.1470	0.1182	0.1182
TI ↓	hold_rising to CP	-0.0697	-0.1014	-0.0597	-0.0613
TI ↑	hold_rising to CP	-0.0126	-0.0120	-0.0166	-0.0182
TI ↓	setup_rising to CP	0.1141	0.1425	0.1140	0.1140
TI ↑	setup_rising to CP	0.0466	0.0402	0.0466	0.0466
		C8T28SOIDV_-LL_-SDFPRQX19_-P16	C8T28SOIDV_-LL_-SDFPRQX29_-P16		
CP ↓	min_pulse_width to CP	0.0997	0.0997		
CP ↑	min_pulse_width to CP	0.0483	0.0483		
D ↓	hold_rising to CP	-0.0169	-0.0169		
D ↑	hold_rising to CP	-0.0071	-0.0071		
D ↓	setup_rising to CP	0.0684	0.0684		
D ↑	setup_rising to CP	0.0319	0.0319		
RN ↓	min_pulse_width to RN	0.0610	0.0632		
RN ↑	recovery_rising to CP	0.0085	0.0059		
RN ↑	removal_rising to CP	0.0021	0.0016		
TE ↓	hold_rising to CP	-0.0153	-0.0153		
TE ↑	hold_rising to CP	-0.0169	-0.0169		
TE ↓	setup_rising to CP	0.0668	0.0668		
TE ↑	setup_rising to CP	0.1182	0.1182		
TI ↓	hold_rising to CP	-0.0613	-0.0613		
TI ↑	hold_rising to CP	-0.0182	-0.0182		
TI ↓	setup_rising to CP	0.1140	0.1140		
TI ↑	setup_rising to CP	0.0466	0.0466		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P16	5.586e-07	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P16	5.182e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P16	5.327e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P16	6.654e-07	1.000e-20

C8T28SOIDV_LL_SDFPRQX19_P16	8.075e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P16	9.929e-07	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

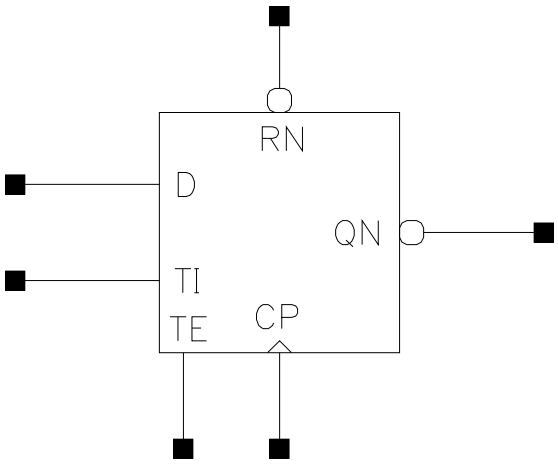
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P16	C8T28SOI_LLHF_-SDFPRQX3_P16	C8T28SOIDV_LL_-SDFPRQX5_P16	C8T28SOIDV_LL_-SDFPRQX10_P16
Clock 100Mhz Data 0Mhz	7.969e-03	7.673e-03	7.383e-03	7.238e-03
Clock 100Mhz Data 25Mhz	7.664e-03	7.427e-03	7.175e-03	7.593e-03
Clock 100Mhz Data 50Mhz	7.358e-03	7.182e-03	6.966e-03	7.948e-03
Clock = 0 Data 100Mhz	3.570e-03	3.730e-03	3.631e-03	3.583e-03
Clock = 1 Data 100Mhz	1.210e-04	5.587e-04	4.208e-04	3.518e-04
	C8T28SOIDV_LL_-SDFPRQX19_P16	C8T28SOIDV_LL_-SDFPRQX29_P16		
Clock 100Mhz Data 0Mhz	7.151e-03	7.094e-03		
Clock 100Mhz Data 25Mhz	8.071e-03	8.805e-03		
Clock 100Mhz Data 50Mhz	8.991e-03	1.052e-02		
Clock = 0 Data 100Mhz	3.554e-03	3.536e-03		
Clock = 1 Data 100Mhz	3.106e-04	2.831e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P16	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P16	C8T28SOI_LLHF_-SDFPRQNX3_P16	C8T28SOIDV_LL_-SDFPRQNX5_P16	C8T28SOIDV_LL_-SDFPRQNX10_P16
CP	0.0008	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
RN	0.0009	0.0008	0.0010	0.0009
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P16	C8T28SOIDV_LL_-SDFPRQNX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0008		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNX5_P16	**C8T28SOI_LLHF_-SDFPRQNX3_P16**	**C8T28SOI_LL_-SDFPRQNX5_P16**	**C8T28SOI_LLHF_-SDFPRQNX3_P16**
CP to QN ↓	0.0877	0.0934	3.4307	5.0071
CP to QN ↑	0.0808	0.0759	5.2262	7.6505
RN to QN ↑	0.0806	0.0792	5.2205	7.6378
	C8T28SOIDV_LL_-SDFPRQNX5_P16	**C8T28SOIDV_LL_-SDFPRQNX10_P16**	**C8T28SOIDV_LL_-SDFPRQNX5_P16**	**C8T28SOIDV_LL_-SDFPRQNX10_P16**
CP to QN ↓	0.0993	0.0901	3.1718	1.6142
CP to QN ↑	0.0743	0.0747	4.9460	2.5138
RN to QN ↑	0.0708	0.0723	4.9516	2.5157
	C8T28SOIDV_LL_-SDFPRQNX19_P16	**C8T28SOIDV_LL_-SDFPRQNX29_P16**	**C8T28SOIDV_LL_-SDFPRQNX19_P16**	**C8T28SOIDV_LL_-SDFPRQNX29_P16**
CP to QN ↓	0.1001	0.1067	0.8567	0.5742
CP to QN ↑	0.0828	0.0937	1.2947	0.8726
RN to QN ↑	0.0776	0.0903	1.2933	0.8715

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P16	C8T28SOI_-LLHF_-SDFPRQNX3_-P16	C8T28SOIDV_-LL_-SDFPRQNX5_-P16	C8T28SOIDV_-LL_-SDFPRQNX10_-P16
CP ↓	min_pulse_width to CP	0.1118	0.1059	0.0997	0.0997
CP ↑	min_pulse_width to CP	0.0484	0.0452	0.0483	0.0482
D ↓	hold_rising to CP	-0.0539	-0.1017	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0169	-0.0169	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0954	0.1510	0.0684	0.0684
D ↑	setup_rising to CP	0.0438	0.0465	0.0319	0.0319
RN ↓	min_pulse_width to RN	0.0735	0.0735	0.0632	0.0703
RN ↑	recovery_rising to CP	0.0108	0.0076	0.0080	0.0080

RN ↑	removal_rising to CP	0.0021	0.0021	0.0021	0.0021
TE ↓	hold_rising to CP	-0.0359	-0.0408	-0.0153	-0.0126
TE ↑	hold_rising to CP	-0.0147	-0.0142	-0.0143	-0.0169
TE ↓	setup_rising to CP	0.0928	0.1245	0.0668	0.0668
TE ↑	setup_rising to CP	0.1150	0.1470	0.1182	0.1182
TI ↓	hold_rising to CP	-0.0697	-0.1014	-0.0613	-0.0597
TI ↑	hold_rising to CP	-0.0169	-0.0113	-0.0169	-0.0166
TI ↓	setup_rising to CP	0.1141	0.1425	0.1140	0.1140
TI ↑	setup_rising to CP	0.0466	0.0417	0.0430	0.0466
		C8T28SOIDV_-LL_-SDFPRQNX19_-P16	C8T28SOIDV_-LL_-SDFPRQNX29_-P16		
CP ↓	min_pulse_width to CP	0.1021	0.1021		
CP ↑	min_pulse_width to CP	0.0529	0.0623		
D ↓	hold_rising to CP	-0.0148	-0.0148		
D ↑	hold_rising to CP	-0.0071	-0.0071		
D ↓	setup_rising to CP	0.0684	0.0684		
D ↑	setup_rising to CP	0.0319	0.0319		
RN ↓	min_pulse_width to RN	0.0703	0.0872		
RN ↑	recovery_rising to CP	0.0059	0.0027		
RN ↑	removal_rising to CP	0.0048	0.0048		
TE ↓	hold_rising to CP	-0.0094	-0.0094		
TE ↑	hold_rising to CP	-0.0142	-0.0142		
TE ↓	setup_rising to CP	0.0668	0.0668		
TE ↑	setup_rising to CP	0.1182	0.1182		
TI ↓	hold_rising to CP	-0.0607	-0.0607		
TI ↑	hold_rising to CP	-0.0169	-0.0169		
TI ↓	setup_rising to CP	0.1140	0.1140		
TI ↑	setup_rising to CP	0.0466	0.0466		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P16	5.521e-07	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P16	5.212e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P16	5.320e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P16	6.586e-07	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P16	7.667e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P16	9.543e-07	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

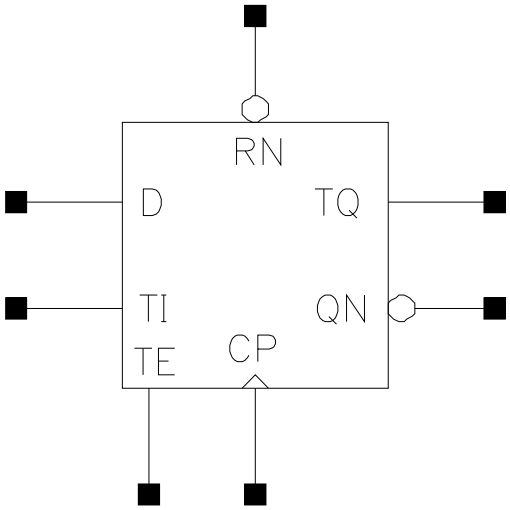
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P16	C8T28SOI_LLHF_-SDFPRQNX3_P16	C8T28SOIDV_LL_-SDFPRQNX5_P16	C8T28SOIDV_LL_-SDFPRQNX10_P16
Clock 100Mhz Data 0Mhz	7.594e-03	7.429e-03	7.085e-03	6.911e-03
Clock 100Mhz Data 25Mhz	7.402e-03	7.270e-03	7.046e-03	7.358e-03
Clock 100Mhz Data 50Mhz	7.210e-03	7.112e-03	7.007e-03	7.805e-03
Clock = 0 Data 100Mhz	3.583e-03	3.743e-03	3.668e-03	3.629e-03
Clock = 1 Data 100Mhz	6.502e-05	5.306e-04	3.792e-04	3.034e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P16	C8T28SOIDV_LL_-SDFPRQNX29_P16		
Clock 100Mhz Data 0Mhz	6.866e-03	6.862e-03		
Clock 100Mhz Data 25Mhz	7.893e-03	8.763e-03		
Clock 100Mhz Data 50Mhz	8.921e-03	1.066e-02		
Clock = 0 Data 100Mhz	3.599e-03	3.579e-03		
Clock = 1 Data 100Mhz	2.580e-04	2.278e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P16	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P16	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P16	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P16	C8T28SOI_LLHF_-SDFPRQNTX3_P16	C8T28SOIDV_LL_-SDFPRQNTX5_P16	C8T28SOIDV_LL_-SDFPRQNTX10_P16
CP	0.0008	0.0007	0.0005	0.0005
D	0.0005	0.0006	0.0005	0.0005
RN	0.0009	0.0008	0.0010	0.0010
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P16	C8T28SOIDV_LL_-SDFPRQNTX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0009	0.0008		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPRQNTX5_P16	**C8T28SOI_LLHF_-SDFPRQNTX3_P16**	**C8T28SOI_LL_-SDFPRQNTX5_P16**	**C8T28SOI_LLHF_-SDFPRQNTX3_P16**
CP to QN ↓	0.0972	0.1017	3.3760	5.0667
CP to QN ↑	0.1026	0.0937	5.4867	7.6590
CP to TQ ↓	0.0863	0.0675	9.4719	5.9401
CP to TQ ↑	0.0803	0.0757	25.8722	13.9457
RN to QN ↑	0.0890	0.0860	5.4924	7.7051
RN to TQ ↓	0.0765	0.0675	9.1557	5.6529
	C8T28SOIDV_LL_-SDFPRQNTX5_P16	**C8T28SOIDV_LL_-SDFPRQNTX10_P16**	**C8T28SOIDV_LL_-SDFPRQNTX5_P16**	**C8T28SOIDV_LL_-SDFPRQNTX10_P16**
CP to QN ↓	0.1049	0.1115	3.2120	1.6768
CP to QN ↑	0.0822	0.0868	4.9358	2.5042
CP to TQ ↓	0.0571	0.0580	5.8397	5.8864
CP to TQ ↑	0.0777	0.0777	10.9793	10.9859
RN to QN ↑	0.0795	0.0846	4.9359	2.5022
RN to TQ ↓	0.0527	0.0539	5.8582	5.9092
	C8T28SOIDV_LL_-SDFPRQNTX19_P16	**C8T28SOIDV_LL_-SDFPRQNTX29_P16**	**C8T28SOIDV_LL_-SDFPRQNTX19_P16**	**C8T28SOIDV_LL_-SDFPRQNTX29_P16**
CP to QN ↓	0.1048	0.1070	0.8409	0.5739
CP to QN ↑	0.0898	0.1014	1.2676	0.8645
CP to TQ ↓	0.0629	0.0772	5.9525	6.8193
CP to TQ ↑	0.0825	0.0917	11.0127	12.7291
RN to QN ↑	0.0845	0.0967	1.2672	0.8623
RN to TQ ↓	0.0563	0.0713	5.9372	6.6932

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P16	C8T28SOI_-LLHF_-SDFPRQNTX3_-P16	C8T28SOIDV_-LL_-SDFPRQNTX5_-P16	C8T28SOIDV_-LL_SDF-PRQNTX10_P16
CP ↓	min_pulse_width to CP	0.1118	0.1043	0.1003	0.0997
CP ↑	min_pulse_width to CP	0.0640	0.0546	0.0482	0.0529
D ↓	hold_rising to CP	-0.0507	-0.1017	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0137	-0.0169	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0954	0.1510	0.0684	0.0684
D ↑	setup_rising to CP	0.0438	0.0465	0.0319	0.0319
RN ↓	min_pulse_width to RN	0.0779	0.0757	0.0730	0.0752
RN ↑	recovery_rising to CP	0.0134	0.0076	0.0080	0.0080
RN ↑	removal_rising to CP	0.0021	0.0021	0.0021	0.0021
TE ↓	hold_rising to CP	-0.0359	-0.0408	-0.0126	-0.0126
TE ↑	hold_rising to CP	-0.0147	-0.0142	-0.0142	-0.0169
TE ↓	setup_rising to CP	0.0928	0.1245	0.0668	0.0668
TE ↑	setup_rising to CP	0.1150	0.1470	0.1203	0.1182
TI ↓	hold_rising to CP	-0.0697	-0.1014	-0.0613	-0.0597
TI ↑	hold_rising to CP	-0.0126	-0.0113	-0.0169	-0.0166
TI ↓	setup_rising to CP	0.1141	0.1468	0.1140	0.1140
TI ↑	setup_rising to CP	0.0430	0.0417	0.0430	0.0466
		C8T28SOIDV_-LL_SDF-PRQNTX19_P16	C8T28SOIDV_-LL_SDF-PRQNTX29_P16		
CP ↓	min_pulse_width to CP	0.1021	0.1021		
CP ↑	min_pulse_width to CP	0.0542	0.0671		
D ↓	hold_rising to CP	-0.0148	-0.0148		
D ↑	hold_rising to CP	-0.0071	-0.0071		
D ↓	setup_rising to CP	0.0684	0.0684		
D ↑	setup_rising to CP	0.0319	0.0319		
RN ↓	min_pulse_width to RN	0.0779	0.0920		
RN ↑	recovery_rising to CP	0.0059	0.0085		
RN ↑	removal_rising to CP	0.0048	0.0015		
TE ↓	hold_rising to CP	-0.0094	-0.0094		
TE ↑	hold_rising to CP	-0.0142	-0.0142		

TE ↓	setup_rising to CP	0.0668	0.0668		
TE ↑	setup_rising to CP	0.1182	0.1182		
TI ↓	hold_rising to CP	-0.0607	-0.0607		
TI ↑	hold_rising to CP	-0.0166	-0.0166		
TI ↓	setup_rising to CP	0.1140	0.1140		
TI ↑	setup_rising to CP	0.0466	0.0466		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P16	5.842e-07	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P16	5.494e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P16	5.652e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_P16	6.210e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_P16	7.700e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_P16	9.820e-07	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

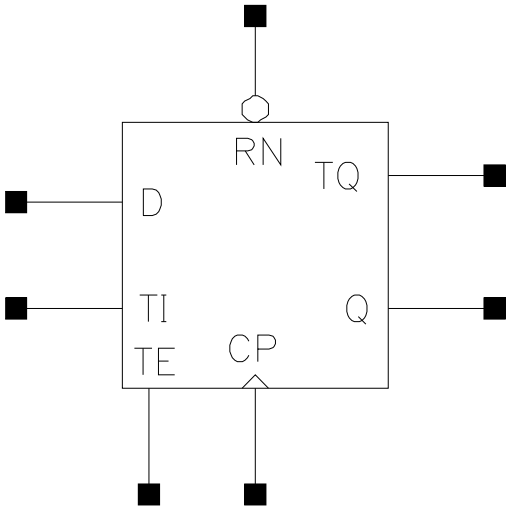
Pin Cycle	C8T28SOI_LL_SDFPRQNTX5_P16	C8T28SOI_LLHF_SDFPRQNTX3_P16	C8T28SOIDV_LL_SDFPRQNTX5_P16	C8T28SOIDV_LL_SDFPRQNTX10_P16
Clock 100Mhz Data 0Mhz	7.799e-03	7.594e-03	7.240e-03	7.053e-03
Clock 100Mhz Data 25Mhz	7.799e-03	7.574e-03	7.315e-03	7.422e-03
Clock 100Mhz Data 50Mhz	7.799e-03	7.554e-03	7.390e-03	7.792e-03
Clock = 0 Data 100Mhz	3.556e-03	3.726e-03	3.635e-03	3.586e-03
Clock = 1 Data 100Mhz	9.037e-05	5.456e-04	3.995e-04	3.263e-04
	C8T28SOIDV_LL_SDFPRQNTX19_P16	C8T28SOIDV_LL_SDFPRQNTX29_P16		
Clock 100Mhz Data 0Mhz	7.003e-03	6.960e-03		
Clock 100Mhz Data 25Mhz	7.968e-03	8.933e-03		
Clock 100Mhz Data 50Mhz	8.932e-03	1.090e-02		
Clock = 0 Data 100Mhz	3.555e-03	3.535e-03		
Clock = 1 Data 100Mhz	2.824e-04	2.531e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P16	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P16	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P16	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P16	C8T28SOI_LLHF_-SDFPRQTX3_P16	C8T28SOIDV_LL_-SDFPRQTX5_P16	C8T28SOIDV_LL_-SDFPRQTX10_P16
CP	0.0008	0.0007	0.0005	0.0005
D	0.0005	0.0006	0.0005	0.0005
RN	0.0009	0.0008	0.0010	0.0009
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P16	C8T28SOIDV_LL_-SDFPRQTX29_P16		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0010	0.0009		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQTX5_P16	**C8T28SOI_LLHF_-SDFPRQTX3_P16**	**C8T28SOI_LL_-SDFPRQTX5_P16**	**C8T28SOI_LLHF_-SDFPRQTX3_P16**
CP to Q ↓	0.0901	0.0778	3.8165	5.6139
CP to Q ↑	0.0708	0.0765	5.1138	7.9798
CP to TQ ↓	0.1072	0.0770	9.9509	6.1181
CP to TQ ↑	0.0895	0.0804	25.9163	14.1403
RN to Q ↓	0.0642	0.0717	3.5581	5.1781
RN to TQ ↓	0.0797	0.0716	9.5906	5.7758
	C8T28SOIDV_LL_-SDFPRQTX5_P16	**C8T28SOIDV_LL_-SDFPRQTX10_P16**	**C8T28SOIDV_LL_-SDFPRQTX5_P16**	**C8T28SOIDV_LL_-SDFPRQTX10_P16**
CP to Q ↓	0.0657	0.0864	3.4219	1.6390
CP to Q ↑	0.0797	0.1126	5.0576	2.5057
CP to TQ ↓	0.0667	0.0897	6.0162	5.8224
CP to TQ ↑	0.0826	0.1171	11.1430	11.0569
RN to Q ↓	0.0633	0.0904	3.3889	1.6400
RN to TQ ↓	0.0644	0.0937	5.9700	5.8228
	C8T28SOIDV_LL_-SDFPRQTX19_P16	**C8T28SOIDV_LL_-SDFPRQTX29_P16**	**C8T28SOIDV_LL_-SDFPRQTX19_P16**	**C8T28SOIDV_LL_-SDFPRQTX29_P16**
CP to Q ↓	0.0966	0.0932	0.8689	0.5804
CP to Q ↑	0.1200	0.1223	1.2752	0.8703
CP to TQ ↓	0.1016	0.0963	5.8909	5.7944
CP to TQ ↑	0.1266	0.1280	11.0574	11.4388
RN to Q ↓	0.0941	0.0968	0.8687	0.5806
RN to TQ ↓	0.0991	0.0999	5.8916	5.7938

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_-P16	C8T28SOI_-LLHF_-SDFPRQTX3_-P16	C8T28SOIDV_-LL_-SDFPRQTX5_-P16	C8T28SOIDV_-LL_-SDFPRQTX10_-P16
CP ↓	min_pulse_width to CP	0.1118	0.1043	0.0997	0.0997
CP ↑	min_pulse_width to CP	0.0783	0.0593	0.0529	0.0483
D ↓	hold_rising to CP	-0.0507	-0.1017	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0137	-0.0169	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0954	0.1510	0.0684	0.0684
D ↑	setup_rising to CP	0.0438	0.0465	0.0319	0.0319
RN ↓	min_pulse_width to RN	0.0850	0.0757	0.0730	0.0610
RN ↑	recovery_rising to CP	0.0134	0.0076	0.0080	0.0059
RN ↑	removal_rising to CP	0.0021	0.0021	0.0021	0.0016
TE ↓	hold_rising to CP	-0.0359	-0.0408	-0.0126	-0.0153
TE ↑	hold_rising to CP	-0.0147	-0.0142	-0.0169	-0.0169
TE ↓	setup_rising to CP	0.0928	0.1245	0.0668	0.0668
TE ↑	setup_rising to CP	0.1150	0.1470	0.1182	0.1182
TI ↓	hold_rising to CP	-0.0697	-0.1014	-0.0599	-0.0613
TI ↑	hold_rising to CP	-0.0126	-0.0113	-0.0166	-0.0182
TI ↓	setup_rising to CP	0.1141	0.1468	0.1140	0.1140
TI ↑	setup_rising to CP	0.0430	0.0417	0.0466	0.0466
		C8T28SOIDV_-LL_-SDFPRQTX19_-P16	C8T28SOIDV_-LL_-SDFPRQTX29_-P16		
CP ↓	min_pulse_width to CP	0.0997	0.0997		
CP ↑	min_pulse_width to CP	0.0483	0.0483		
D ↓	hold_rising to CP	-0.0169	-0.0169		
D ↑	hold_rising to CP	-0.0071	-0.0071		
D ↓	setup_rising to CP	0.0684	0.0684		
D ↑	setup_rising to CP	0.0319	0.0319		
RN ↓	min_pulse_width to RN	0.0632	0.0610		
RN ↑	recovery_rising to CP	0.0059	0.0059		
RN ↑	removal_rising to CP	0.0021	0.0016		
TE ↓	hold_rising to CP	-0.0153	-0.0153		
TE ↑	hold_rising to CP	-0.0169	-0.0169		

TE ↓	setup_rising to CP	0.0668	0.0668		
TE ↑	setup_rising to CP	0.1182	0.1182		
TI ↓	hold_rising to CP	-0.0613	-0.0613		
TI ↑	hold_rising to CP	-0.0182	-0.0182		
TI ↓	setup_rising to CP	0.1140	0.1140		
TI ↑	setup_rising to CP	0.0466	0.0466		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P16	5.932e-07	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P16	5.478e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P16	5.653e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P16	7.023e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P16	8.336e-07	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P16	1.028e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

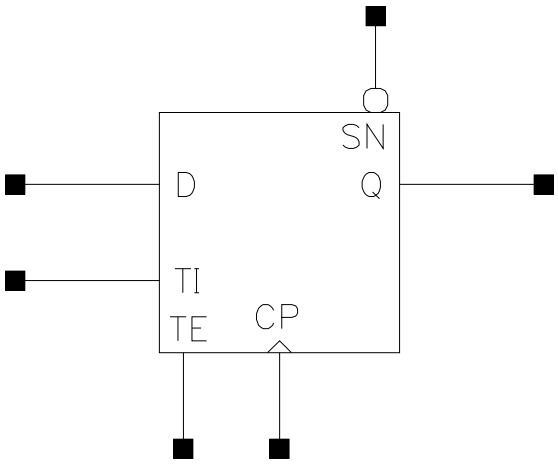
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P16	C8T28SOI_LLHF_-SDFPRQTX3_P16	C8T28SOIDV_LL_-SDFPRQTX5_P16	C8T28SOIDV_LL_-SDFPRQTX10_P16
Clock 100Mhz Data 0Mhz	7.971e-03	7.657e-03	7.368e-03	7.224e-03
Clock 100Mhz Data 25Mhz	7.919e-03	7.583e-03	7.327e-03	7.786e-03
Clock 100Mhz Data 50Mhz	7.866e-03	7.509e-03	7.286e-03	8.349e-03
Clock = 0 Data 100Mhz	3.560e-03	3.727e-03	3.630e-03	3.582e-03
Clock = 1 Data 100Mhz	2.711e-05	5.141e-04	3.531e-04	2.726e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P16	C8T28SOIDV_LL_-SDFPRQTX29_P16		
Clock 100Mhz Data 0Mhz	7.137e-03	7.080e-03		
Clock 100Mhz Data 25Mhz	8.266e-03	8.895e-03		
Clock 100Mhz Data 50Mhz	9.394e-03	1.071e-02		
Clock = 0 Data 100Mhz	3.553e-03	3.535e-03		
Clock = 1 Data 100Mhz	2.243e-04	1.922e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P16	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P16	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P16	C8T28SOI_LLHF_-SDFPSQX3_P16	C8T28SOIDV_LL_-SDFPSQX5_P16	C8T28SOIDV_LL_-SDFPSQX10_P16
CP	0.0008	0.0007	0.0005	0.0006
D	0.0003	0.0005	0.0004	0.0004
SN	0.0014	0.0014	0.0011	0.0011
TE	0.0011	0.0010	0.0010	0.0011
TI	0.0004	0.0006	0.0005	0.0004
	C8T28SOIDV_LL_-SDFPSQX14_P16	C8T28SOIDV_LL_-SDFPSQX19_P16	C8T28SOIDV_LL_-SDFPSQX29_P16	
CP	0.0006	0.0006	0.0006	
D	0.0004	0.0004	0.0004	
SN	0.0011	0.0011	0.0011	
TE	0.0011	0.0011	0.0011	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P16	**C8T28SOI_LLHF_-SDFPSQX3_P16**	**C8T28SOI_LL_-SDFPSQX5_P16**	**C8T28SOI_LLHF_-SDFPSQX3_P16**
CP to Q ↓	0.0792	0.0706	3.6397	5.4983
CP to Q ↑	0.0673	0.0747	5.1016	7.8004
SN to Q ↑	0.0558	0.0508	5.0392	7.7139
	C8T28SOIDV_LL_-SDFPSQX5_P16	**C8T28SOIDV_LL_-SDFPSQX10_P16**	**C8T28SOIDV_LL_-SDFPSQX5_P16**	**C8T28SOIDV_LL_-SDFPSQX10_P16**
CP to Q ↓	0.0594	0.0856	3.3056	1.5775
CP to Q ↑	0.0736	0.1193	5.0086	2.4963
SN to Q ↑	0.0509	0.0943	4.9952	2.4947
	C8T28SOIDV_LL_-SDFPSQX14_P16	**C8T28SOIDV_LL_-SDFPSQX19_P16**	**C8T28SOIDV_LL_-SDFPSQX14_P16**	**C8T28SOIDV_LL_-SDFPSQX19_P16**
CP to Q ↓	0.0865	0.0920	1.0872	0.8426
CP to Q ↑	0.1196	0.1237	1.6800	1.2687
SN to Q ↑	0.0941	0.0984	1.6782	1.2692
	C8T28SOIDV_LL_-SDFPSQX29_P16		**C8T28SOIDV_LL_-SDFPSQX29_P16**	
CP to Q ↓	0.0919		0.5707	
CP to Q ↑	0.1310		0.8420	
SN to Q ↑	0.1057		0.8423	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P16	C8T28SOI_-LLHF_-SDFPSQX3_P16	C8T28SOIDV_-LL_SDFPSQX5_-P16	C8T28SOIDV_-LL_-SDFPSQX10_-P16
CP ↓	min_pulse_width to CP	0.1190	0.1185	0.1051	0.1045
CP ↑	min_pulse_width to CP	0.0654	0.0546	0.0482	0.0449
D ↓	hold_rising to CP	-0.0556	-0.1115	-0.0246	-0.0290
D ↑	hold_rising to CP	-0.0142	-0.0110	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1025	0.1657	0.0791	0.0781
D ↑	setup_rising to CP	0.0417	0.0433	0.0319	0.0319

SN ↓	min_pulse_width to SN	0.0522	0.0447	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0106	0.0102	0.0005	0.0009
SN ↑	removal_rising to CP	0.0261	0.0304	0.0352	0.0384
TE ↓	hold_rising to CP	-0.0333	-0.0355	-0.0192	-0.0241
TE ↑	hold_rising to CP	-0.0120	-0.0083	-0.0045	-0.0120
TE ↓	setup_rising to CP	0.1009	0.1371	0.0765	0.0786
TE ↑	setup_rising to CP	0.1226	0.1590	0.1208	0.1133
TI ↓	hold_rising to CP	-0.0746	-0.1062	-0.0607	-0.0551
TI ↑	hold_rising to CP	-0.0120	-0.0104	-0.0056	-0.0120
TI ↓	setup_rising to CP	0.1232	0.1558	0.1134	0.1043
TI ↑	setup_rising to CP	0.0417	0.0361	0.0320	0.0374
		C8T28SOIDV_-LL_-SDFPSQX14_-P16	C8T28SOIDV_-LL_-SDFPSQX19_-P16	C8T28SOIDV_-LL_-SDFPSQX29_-P16	
CP ↓	min_pulse_width to CP	0.1045	0.1045	0.1045	
CP ↑	min_pulse_width to CP	0.0450	0.0450	0.0450	
D ↓	hold_rising to CP	-0.0290	-0.0290	-0.0290	
D ↑	hold_rising to CP	-0.0071	-0.0071	-0.0071	
D ↓	setup_rising to CP	0.0781	0.0781	0.0781	
D ↑	setup_rising to CP	0.0319	0.0319	0.0319	
SN ↓	min_pulse_width to SN	0.0474	0.0474	0.0500	
SN ↑	recovery_rising to CP	0.0009	0.0009	0.0009	
SN ↑	removal_rising to CP	0.0384	0.0384	0.0384	
TE ↓	hold_rising to CP	-0.0241	-0.0241	-0.0241	
TE ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120	
TE ↓	setup_rising to CP	0.0786	0.0786	0.0786	
TE ↑	setup_rising to CP	0.1133	0.1133	0.1133	
TI ↓	hold_rising to CP	-0.0551	-0.0551	-0.0551	
TI ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120	
TI ↓	setup_rising to CP	0.1043	0.1043	0.1086	
TI ↑	setup_rising to CP	0.0374	0.0374	0.0374	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds

C8T28SOI_LL_SDFPSQX5_P16	5.737e-07	1.000e-20
C8T28SOI_LLHF_SDFPSQX3_P16	5.356e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P16	5.626e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P16	7.057e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P16	7.715e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P16	8.498e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P16	1.014e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

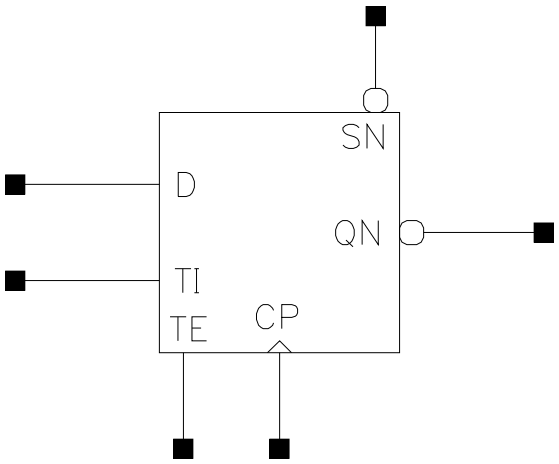
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P16	C8T28SOI_LLHF_-SDFPSQX3_P16	C8T28SOIDV_LL_-SDFPSQX5_P16	C8T28SOIDV_LL_-SDFPSQX10_P16
Clock 100Mhz Data 0Mhz	7.531e-03	7.357e-03	7.037e-03	6.883e-03
Clock 100Mhz Data 25Mhz	7.491e-03	7.241e-03	6.908e-03	7.415e-03
Clock 100Mhz Data 50Mhz	7.451e-03	7.125e-03	6.778e-03	7.947e-03
Clock = 0 Data 100Mhz	3.683e-03	3.837e-03	3.775e-03	3.759e-03
Clock = 1 Data 100Mhz	7.291e-05	5.310e-04	3.798e-04	3.047e-04
	C8T28SOIDV_LL_-SDFPSQX14_P16	C8T28SOIDV_LL_-SDFPSQX19_P16	C8T28SOIDV_LL_-SDFPSQX29_P16	
Clock 100Mhz Data 0Mhz	6.791e-03	6.730e-03	6.686e-03	
Clock 100Mhz Data 25Mhz	7.574e-03	7.927e-03	8.452e-03	
Clock 100Mhz Data 50Mhz	8.356e-03	9.124e-03	1.022e-02	
Clock = 0 Data 100Mhz	3.750e-03	3.743e-03	3.739e-03	
Clock = 1 Data 100Mhz	2.596e-04	2.296e-04	2.082e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P16	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P16	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P16	C8T28SOI_LLHF_-SDFPSQNX3_P16	C8T28SOIDV_LL_-SDFPSQNX5_P16	C8T28SOIDV_LL_-SDFPSQNX10_P16
CP	0.0008	0.0007	0.0005	0.0005
D	0.0003	0.0005	0.0004	0.0004
SN	0.0014	0.0014	0.0011	0.0012
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0004	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQNX14_P16	C8T28SOIDV_LL_-SDFPSQNX19_P16	C8T28SOIDV_LL_-SDFPSQNX23_P16	C8T28SOIDV_LL_-SDFPSQNX29_P16
CP	0.0005	0.0005	0.0005	0.0005
D	0.0004	0.0004	0.0004	0.0004
SN	0.0012	0.0012	0.0012	0.0011
TE	0.0010	0.0010	0.0010	0.0010
TI	0.0005	0.0005	0.0005	0.0005

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNX5_P16	**C8T28SOI_LLHF_-SDFPSQNX3_P16**	**C8T28SOI_LL_-SDFPSQNX5_P16**	**C8T28SOI_LLHF_-SDFPSQNX3_P16**
CP to QN ↓	0.0920	0.0933	3.5240	4.9809
CP to QN ↑	0.0856	0.0793	5.3115	7.6467
SN to QN ↓	0.0819	0.0704	3.5243	4.9739
	C8T28SOIDV_LL_-SDFPSQNX5_P16	**C8T28SOIDV_LL_-SDFPSQNX10_P16**	**C8T28SOIDV_LL_-SDFPSQNX5_P16**	**C8T28SOIDV_LL_-SDFPSQNX10_P16**
CP to QN ↓	0.0990	0.0926	3.1605	1.5986
CP to QN ↑	0.0777	0.0808	4.9560	2.4806
SN to QN ↓	0.0754	0.0672	3.1589	1.5988
	C8T28SOIDV_LL_-SDFPSQNX14_P16	**C8T28SOIDV_LL_-SDFPSQNX19_P16**	**C8T28SOIDV_LL_-SDFPSQNX14_P16**	**C8T28SOIDV_LL_-SDFPSQNX19_P16**
CP to QN ↓	0.0963	0.0991	1.0727	0.8218
CP to QN ↑	0.0834	0.0863	1.6670	1.2546
SN to QN ↓	0.0693	0.0729	1.0730	0.8203
	C8T28SOIDV_LL_-SDFPSQNX23_P16	**C8T28SOIDV_LL_-SDFPSQNX29_P16**	**C8T28SOIDV_LL_-SDFPSQNX23_P16**	**C8T28SOIDV_LL_-SDFPSQNX29_P16**
CP to QN ↓	0.1004	0.0969	0.6531	0.5639
CP to QN ↑	0.0861	0.0881	1.2492	0.8413
SN to QN ↓	0.0749	0.0745	0.6514	0.5642

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P16	C8T28SOI_-LLHF_-SDFPSQNX3_-P16	C8T28SOIDV_-LL_-SDFPSQNX5_-P16	C8T28SOIDV_-LL_-SDFPSQNX10_-P16
CP ↓	min_pulse_width to CP	0.1190	0.1185	0.1069	0.1069
CP ↑	min_pulse_width to CP	0.0498	0.0452	0.0482	0.0529
D ↓	hold_rising to CP	-0.0556	-0.1115	-0.0246	-0.0214
D ↑	hold_rising to CP	-0.0142	-0.0110	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1025	0.1657	0.0791	0.0791

D ↑	setup_rising to CP	0.0417	0.0466	0.0319	0.0319
SN ↓	min_pulse_width to SN	0.0496	0.0447	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0106	0.0102	0.0005	0.0005
SN ↑	removal_rising to CP	0.0261	0.0336	0.0352	0.0384
TE ↓	hold_rising to CP	-0.0333	-0.0350	-0.0192	-0.0192
TE ↑	hold_rising to CP	-0.0120	-0.0083	-0.0045	-0.0049
TE ↓	setup_rising to CP	0.1009	0.1371	0.0765	0.0786
TE ↑	setup_rising to CP	0.1226	0.1590	0.1208	0.1203
TI ↓	hold_rising to CP	-0.0789	-0.1062	-0.0607	-0.0607
TI ↑	hold_rising to CP	-0.0120	-0.0104	-0.0056	-0.0056
TI ↓	setup_rising to CP	0.1232	0.1558	0.1150	0.1134
TI ↑	setup_rising to CP	0.0417	0.0361	0.0320	0.0320
		C8T28SOIDV_-LL_-SDFPSQNX14_-P16	C8T28SOIDV_-LL_-SDFPSQNX19_-P16	C8T28SOIDV_-LL_-SDFPSQNX23_-P16	C8T28SOIDV_-LL_-SDFPSQNX29_-P16
CP ↓	min_pulse_width to CP	0.1069	0.1069	0.1069	0.1051
CP ↑	min_pulse_width to CP	0.0529	0.0529	0.0542	0.0576
D ↓	hold_rising to CP	-0.0214	-0.0214	-0.0214	-0.0246
D ↑	hold_rising to CP	-0.0071	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0791	0.0791	0.0791	0.0791
D ↑	setup_rising to CP	0.0319	0.0319	0.0319	0.0319
SN ↓	min_pulse_width to SN	0.0474	0.0474	0.0500	0.0522
SN ↑	recovery_rising to CP	0.0005	0.0005	0.0005	0.0005
SN ↑	removal_rising to CP	0.0384	0.0384	0.0384	0.0352
TE ↓	hold_rising to CP	-0.0192	-0.0192	-0.0192	-0.0192
TE ↑	hold_rising to CP	-0.0045	-0.0045	-0.0045	-0.0045
TE ↓	setup_rising to CP	0.0786	0.0786	0.0786	0.0765
TE ↑	setup_rising to CP	0.1203	0.1203	0.1203	0.1208
TI ↓	hold_rising to CP	-0.0607	-0.0607	-0.0607	-0.0607
TI ↑	hold_rising to CP	-0.0056	-0.0056	-0.0056	-0.0056
TI ↓	setup_rising to CP	0.1134	0.1134	0.1134	0.1150
TI ↑	setup_rising to CP	0.0320	0.0320	0.0320	0.0320

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P16	5.728e-07	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P16	5.357e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P16	5.706e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P16	7.192e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P16	7.784e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P16	8.619e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P16	9.151e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P16	1.041e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

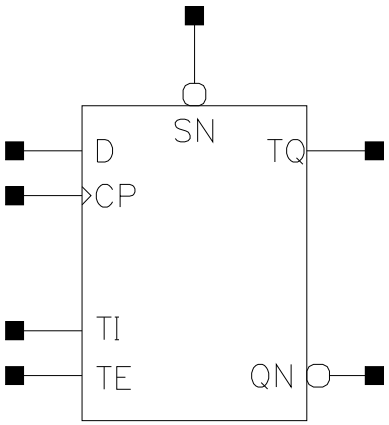
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P16	C8T28SOI_LLHF_-SDFPSQNX3_P16	C8T28SOIDV_LL_-SDFPSQNX5_P16	C8T28SOIDV_LL_-SDFPSQNX10_P16
Clock 100Mhz Data 0Mhz	7.589e-03	7.378e-03	7.026e-03	6.905e-03
Clock 100Mhz Data 25Mhz	7.475e-03	7.238e-03	7.032e-03	7.475e-03
Clock 100Mhz Data 50Mhz	7.361e-03	7.098e-03	7.037e-03	8.044e-03
Clock = 0 Data 100Mhz	3.684e-03	3.839e-03	3.777e-03	3.751e-03
Clock = 1 Data 100Mhz	8.713e-05	5.394e-04	3.906e-04	3.162e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P16	C8T28SOIDV_LL_-SDFPSQNX19_P16	C8T28SOIDV_LL_-SDFPSQNX23_P16	C8T28SOIDV_LL_-SDFPSQNX29_P16
Clock 100Mhz Data 0Mhz	6.830e-03	6.782e-03	6.748e-03	6.699e-03
Clock 100Mhz Data 25Mhz	7.653e-03	7.859e-03	7.937e-03	8.467e-03
Clock 100Mhz Data 50Mhz	8.476e-03	8.935e-03	9.127e-03	1.023e-02
Clock = 0 Data 100Mhz	3.736e-03	3.726e-03	3.718e-03	3.711e-03
Clock = 1 Data 100Mhz	2.717e-04	2.420e-04	2.207e-04	2.048e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P16	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P16	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P16	C8T28SOI_LLHF_-SDFPSQNTX3_P16	C8T28SOIDV_LL_-SDFPSQNTX5_P16	C8T28SOIDV_LL_-SDFPSQNTX10_P16
CP	0.0008	0.0008	0.0005	0.0005
D	0.0003	0.0005	0.0004	0.0004
SN	0.0014	0.0013	0.0011	0.0011
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0004	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQNTX19_P16	C8T28SOIDV_LL_-SDFPSQNTX23_P16	C8T28SOIDV_LL_-SDFPSQNTX29_P16	
CP	0.0005	0.0005	0.0005	
D	0.0004	0.0004	0.0004	
SN	0.0011	0.0011	0.0011	
TE	0.0010	0.0010	0.0010	
TI	0.0005	0.0005	0.0005	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P16	**C8T28SOI_LLHF_-SDFPSQNTX3_P16**	**C8T28SOI_LL_-SDFPSQNTX5_P16**	**C8T28SOI_LLHF_-SDFPSQNTX3_P16**
CP to QN ↓	0.1007	0.1004	3.5774	5.0314
CP to QN ↑	0.1021	0.0951	5.2275	7.6810
CP to TQ ↓	0.0843	0.0683	9.3739	5.9881
CP to TQ ↑	0.0823	0.0772	25.8555	13.9561
SN to QN ↓	0.0874	0.0751	3.5802	5.0364
SN to TQ ↑	0.0698	0.0531	25.8039	13.9089
	C8T28SOIDV_LL_-SDFPSQNTX5_P16	**C8T28SOIDV_LL_-SDFPSQNTX10_P16**	**C8T28SOIDV_LL_-SDFPSQNTX5_P16**	**C8T28SOIDV_LL_-SDFPSQNTX10_P16**
CP to QN ↓	0.0998	0.0935	3.2184	1.5898
CP to QN ↑	0.0815	0.0872	4.9533	2.4919
CP to TQ ↓	0.0577	0.0674	5.9037	6.0107
CP to TQ ↑	0.0748	0.0788	11.9207	12.0085
SN to QN ↓	0.0751	0.0703	3.2207	1.5909
SN to TQ ↑	0.0502	0.0556	11.9079	11.9542
	C8T28SOIDV_LL_-SDFPSQNTX19_P16	**C8T28SOIDV_LL_-SDFPSQNTX23_P16**	**C8T28SOIDV_LL_-SDFPSQNTX19_P16**	**C8T28SOIDV_LL_-SDFPSQNTX23_P16**
CP to QN ↓	0.0994	0.1019	0.8146	0.6502
CP to QN ↑	0.0927	0.0920	1.2591	1.2490
CP to TQ ↓	0.0673	0.0683	5.9941	6.0560
CP to TQ ↑	0.0788	0.0798	12.0070	12.0246
SN to QN ↓	0.0760	0.0785	0.8138	0.6494
SN to TQ ↑	0.0556	0.0565	11.9495	11.9648
	C8T28SOIDV_LL_-SDFPSQNTX29_P16		**C8T28SOIDV_LL_-SDFPSQNTX29_P16**	
CP to QN ↓	0.1015		0.5652	
CP to QN ↑	0.0952		0.8416	

CP to TQ ↓	0.0719		6.1873	
CP to TQ ↑	0.0848		13.8978	
SN to QN ↓	0.0780		0.5650	
SN to TQ ↑	0.0615		13.8217	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P16	C8T28SOI_-LLHF_-SDFPSQNTX3_-P16	C8T28SOIDV_-LL_-SDFPSQNTX5_-P16	C8T28SOIDV_-LL_SDFP-SQNTX10_P16
CP ↓	min_pulse_width to CP	0.1214	0.1185	0.1051	0.1069
CP ↑	min_pulse_width to CP	0.0640	0.0546	0.0482	0.0576
D ↓	hold_rising to CP	-0.0588	-0.1115	-0.0246	-0.0246
D ↑	hold_rising to CP	-0.0116	-0.0110	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1051	0.1657	0.0791	0.0791
D ↑	setup_rising to CP	0.0417	0.0466	0.0319	0.0319
SN ↓	min_pulse_width to SN	0.0571	0.0474	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0102	0.0102	0.0005	0.0005
SN ↑	removal_rising to CP	0.0238	0.0304	0.0352	0.0352
TE ↓	hold_rising to CP	-0.0333	-0.0355	-0.0192	-0.0192
TE ↑	hold_rising to CP	-0.0120	-0.0083	-0.0045	-0.0049
TE ↓	setup_rising to CP	0.1026	0.1371	0.0765	0.0765
TE ↑	setup_rising to CP	0.1248	0.1590	0.1208	0.1208
TI ↓	hold_rising to CP	-0.0789	-0.1062	-0.0607	-0.0607
TI ↑	hold_rising to CP	-0.0120	-0.0104	-0.0056	-0.0056
TI ↓	setup_rising to CP	0.1238	0.1558	0.1150	0.1150
TI ↑	setup_rising to CP	0.0417	0.0361	0.0320	0.0320
		C8T28SOIDV_-LL_SDFP-SQNTX19_P16	C8T28SOIDV_-LL_SDFP-SQNTX23_P16	C8T28SOIDV_-LL_SDFP-SQNTX29_P16	
CP ↓	min_pulse_width to CP	0.1069	0.1069	0.1051	
CP ↑	min_pulse_width to CP	0.0576	0.0576	0.0623	
D ↓	hold_rising to CP	-0.0246	-0.0246	-0.0246	
D ↑	hold_rising to CP	-0.0071	-0.0071	-0.0071	
D ↓	setup_rising to CP	0.0791	0.0791	0.0791	
D ↑	setup_rising to CP	0.0319	0.0319	0.0319	
SN ↓	min_pulse_width to SN	0.0500	0.0500	0.0549	

SN ↑	recovery_rising to CP	0.0005	0.0005	0.0005	
SN ↑	removal_rising to CP	0.0352	0.0352	0.0352	
TE ↓	hold_rising to CP	-0.0192	-0.0192	-0.0192	
TE ↑	hold_rising to CP	-0.0049	-0.0049	-0.0049	
TE ↓	setup_rising to CP	0.0765	0.0765	0.0765	
TE ↑	setup_rising to CP	0.1208	0.1208	0.1208	
TI ↓	hold_rising to CP	-0.0607	-0.0607	-0.0607	
TI ↑	hold_rising to CP	-0.0056	-0.0056	-0.0056	
TI ↓	setup_rising to CP	0.1150	0.1150	0.1150	
TI ↑	setup_rising to CP	0.0320	0.0320	0.0320	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P16	5.920e-07	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P16	5.671e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P16	6.050e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_-P16	7.515e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_-P16	8.979e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_-P16	9.554e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_-P16	1.071e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P16	C8T28SOI_LLHF_-SDFPSQNTX3_P16	C8T28SOIDV_LL_-SDFPSQNTX5_P16	C8T28SOIDV_LL_-SDFPSQNTX10_P16
Clock 100Mhz Data 0Mhz	7.654e-03	7.414e-03	7.156e-03	7.029e-03
Clock 100Mhz Data 25Mhz	7.735e-03	7.463e-03	7.206e-03	7.668e-03
Clock 100Mhz Data 50Mhz	7.817e-03	7.513e-03	7.256e-03	8.307e-03
Clock = 0 Data 100Mhz	3.672e-03	3.828e-03	3.760e-03	3.725e-03
Clock = 1 Data 100Mhz	4.077e-05	5.148e-04	3.568e-04	2.778e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P16	C8T28SOIDV_LL_-SDFPSQNTX23_P16	C8T28SOIDV_LL_-SDFPSQNTX29_P16	
Clock 100Mhz Data 0Mhz	6.951e-03	6.900e-03	6.865e-03	
Clock 100Mhz Data 25Mhz	8.056e-03	8.161e-03	8.708e-03	
Clock 100Mhz Data 50Mhz	9.161e-03	9.421e-03	1.055e-02	

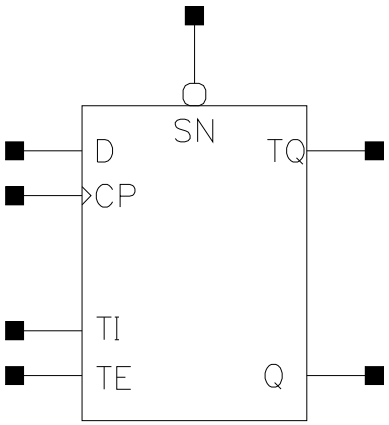
Clock = 0 Data 100Mhz	3.705e-03	3.692e-03	3.684e-03	
Clock = 1 Data 100Mhz	2.305e-04	1.990e-04	1.765e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P16	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P16	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P16	C8T28SOI_LLHF_-SDFPSQTX3_P16	C8T28SOIDV_LL_-SDFPSQTX5_P16	C8T28SOIDV_LL_-SDFPSQTX10_P16
CP	0.0008	0.0007	0.0005	0.0006
D	0.0003	0.0005	0.0004	0.0004
SN	0.0014	0.0013	0.0011	0.0011
TE	0.0011	0.0010	0.0010	0.0011
TI	0.0004	0.0006	0.0005	0.0004
	C8T28SOIDV_LL_-SDFPSQTX19_P16	C8T28SOIDV_LL_-SDFPSQTX29_P16		
CP	0.0006	0.0006		
D	0.0004	0.0004		
SN	0.0011	0.0011		
TE	0.0011	0.0011		
TI	0.0004	0.0004		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQTX5_P16	**C8T28SOI_LLHF_-SDFPSQTX3_P16**	**C8T28SOI_LL_-SDFPSQTX5_P16**	**C8T28SOI_LLHF_-SDFPSQTX3_P16**
CP to Q ↓	0.0868	0.0786	3.8574	5.6985
CP to Q ↑	0.0714	0.0779	5.1155	7.9890
CP to TQ ↓	0.1041	0.0777	9.9131	6.1805
CP to TQ ↑	0.0905	0.0818	25.8933	14.1538
SN to Q ↑	0.0587	0.0532	5.0337	7.8898
SN to TQ ↑	0.0755	0.0566	25.8085	14.0771
	C8T28SOIDV_LL_-SDFPSQTX5_P16	**C8T28SOIDV_LL_-SDFPSQTX10_P16**	**C8T28SOIDV_LL_-SDFPSQTX5_P16**	**C8T28SOIDV_LL_-SDFPSQTX10_P16**
CP to Q ↓	0.0667	0.0850	3.4152	1.6283
CP to Q ↑	0.0768	0.1183	5.0776	2.5217
CP to TQ ↓	0.0681	0.0877	6.0119	6.0629
CP to TQ ↑	0.0791	0.1231	12.0597	11.9599
SN to Q ↑	0.0536	0.0930	5.0562	2.5213
SN to TQ ↑	0.0559	0.0977	12.0092	11.9625
	C8T28SOIDV_LL_-SDFPSQTX19_P16	**C8T28SOIDV_LL_-SDFPSQTX29_P16**	**C8T28SOIDV_LL_-SDFPSQTX19_P16**	**C8T28SOIDV_LL_-SDFPSQTX29_P16**
CP to Q ↓	0.0921	0.1043	0.8480	0.5551
CP to Q ↑	0.1246	0.1363	1.2938	0.8575
CP to TQ ↓	0.0932	0.0585	5.2118	5.4196
CP to TQ ↑	0.1299	0.0817	13.8109	13.8901
SN to Q ↑	0.0990	0.1106	1.2943	0.8586
SN to TQ ↑	0.1045	0.0566	13.8049	13.8790

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_-P16	C8T28SOI_-LLHF_-SDFPSQTX3_-P16	C8T28SOIDV_-LL_-SDFPSQTX5_-P16	C8T28SOIDV_-LL_-SDFPSQTX10_-P16
CP ↓	min_pulse_width to CP	0.1214	0.1185	0.1069	0.1045
CP ↑	min_pulse_width to CP	0.0735	0.0593	0.0528	0.0449
D ↓	hold_rising to CP	-0.0588	-0.1115	-0.0246	-0.0290
D ↑	hold_rising to CP	-0.0116	-0.0110	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1051	0.1657	0.0791	0.0807
D ↑	setup_rising to CP	0.0417	0.0466	0.0319	0.0319
SN ↓	min_pulse_width to SN	0.0571	0.0474	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0102	0.0102	0.0037	0.0009
SN ↑	removal_rising to CP	0.0238	0.0304	0.0352	0.0384
TE ↓	hold_rising to CP	-0.0333	-0.0355	-0.0192	-0.0241
TE ↑	hold_rising to CP	-0.0120	-0.0083	-0.0049	-0.0120
TE ↓	setup_rising to CP	0.1026	0.1371	0.0765	0.0782
TE ↑	setup_rising to CP	0.1248	0.1590	0.1208	0.1160
TI ↓	hold_rising to CP	-0.0789	-0.1062	-0.0607	-0.0548
TI ↑	hold_rising to CP	-0.0120	-0.0104	-0.0056	-0.0120
TI ↓	setup_rising to CP	0.1238	0.1558	0.1150	0.1086
TI ↑	setup_rising to CP	0.0417	0.0361	0.0320	0.0417
		C8T28SOIDV_-LL_-SDFPSQTX19_-P16	C8T28SOIDV_-LL_-SDFPSQTX29_-P16		
CP ↓	min_pulse_width to CP	0.1045	0.1045		
CP ↑	min_pulse_width to CP	0.0450	0.0530		
D ↓	hold_rising to CP	-0.0290	-0.0295		
D ↑	hold_rising to CP	-0.0071	-0.0071		
D ↓	setup_rising to CP	0.0781	0.0781		
D ↑	setup_rising to CP	0.0319	0.0319		
SN ↓	min_pulse_width to SN	0.0474	0.0549		
SN ↑	recovery_rising to CP	0.0009	0.0005		
SN ↑	removal_rising to CP	0.0384	0.0384		
TE ↓	hold_rising to CP	-0.0241	-0.0241		
TE ↑	hold_rising to CP	-0.0120	-0.0094		

TE ↓	setup_rising to CP	0.0786	0.0786		
TE ↑	setup_rising to CP	0.1133	0.1133		
TI ↓	hold_rising to CP	-0.0551	-0.0551		
TI ↑	hold_rising to CP	-0.0120	-0.0120		
TI ↓	setup_rising to CP	0.1043	0.1086		
TI ↑	setup_rising to CP	0.0374	0.0374		

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P16	5.918e-07	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P16	5.662e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P16	6.008e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P16	7.323e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P16	8.627e-07	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P16	1.067e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

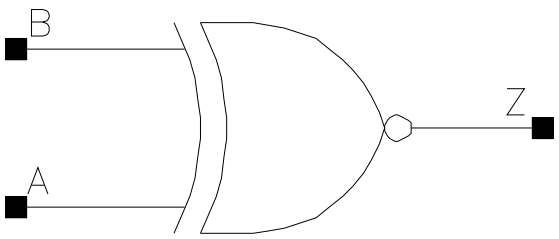
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P16	C8T28SOI_LLHF_-SDFPSQTX3_P16	C8T28SOIDV_LL_-SDFPSQTX5_P16	C8T28SOIDV_LL_-SDFPSQTX10_P16
Clock 100Mhz Data 0Mhz	7.646e-03	7.420e-03	7.156e-03	7.030e-03
Clock 100Mhz Data 25Mhz	7.704e-03	7.438e-03	7.176e-03	7.628e-03
Clock 100Mhz Data 50Mhz	7.762e-03	7.456e-03	7.197e-03	8.227e-03
Clock = 0 Data 100Mhz	3.672e-03	3.828e-03	3.759e-03	3.755e-03
Clock = 1 Data 100Mhz	4.176e-05	5.156e-04	3.573e-04	2.791e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P16	C8T28SOIDV_LL_-SDFPSQTX29_P16		
Clock 100Mhz Data 0Mhz	6.954e-03	6.905e-03		
Clock 100Mhz Data 25Mhz	8.128e-03	8.779e-03		
Clock 100Mhz Data 50Mhz	9.301e-03	1.065e-02		
Clock = 0 Data 100Mhz	3.745e-03	3.738e-03		
Clock = 1 Data 100Mhz	2.322e-04	2.009e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.600	0.544	0.8704
X5_P16	0.800	1.496	1.1968
X8_P16	1.600	1.088	1.7408
X9_P16	0.800	1.632	1.3056
X11_P16	1.600	1.360	2.1760
X14_P16	0.800	2.312	1.8496
X15_P16	1.600	1.904	3.0464
X19_P16	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P16	X5_P16	X8_P16	X9_P16
A	0.0011	0.0006	0.0019	0.0007
B	0.0011	0.0010	0.0015	0.0013
	X11_P16	X14_P16	X15_P16	X19_P16
A	0.0028	0.0010	0.0033	0.0013
B	0.0025	0.0017	0.0029	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X5_P16	X4_P16	X5_P16
A to Z ↓	0.0208	0.0587	4.5403	3.4191
A to Z ↑	0.0233	0.0513	7.2407	5.3795
B to Z ↓	0.0195	0.0440	4.5405	3.4031
B to Z ↑	0.0239	0.0394	7.2586	5.3750

	X8_P16	X9_P16	X8_P16	X9_P16
A to Z ↓	0.0246	0.0544	2.3993	1.7658
A to Z ↑	0.0284	0.0487	3.8554	2.7451
B to Z ↓	0.0234	0.0422	2.3974	1.7631
B to Z ↑	0.0279	0.0385	3.8670	2.7462
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0232	0.0519	1.6849	1.2027
A to Z ↑	0.0263	0.0457	2.5097	1.7691
B to Z ↓	0.0213	0.0395	1.6845	1.2007
B to Z ↑	0.0253	0.0363	2.5191	1.7653
	X15_P16	**X19_P16**	**X15_P16**	**X19_P16**
A to Z ↓	0.0253	0.0480	1.2777	0.8951
A to Z ↑	0.0289	0.0437	1.9131	1.3158
B to Z ↓	0.0233	0.0376	1.2763	0.8924
B to Z ↑	0.0279	0.0352	1.9195	1.3137

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P16	2.403e-07	1.000e-20
X5_P16	2.385e-07	1.000e-20
X8_P16	3.893e-07	1.000e-20
X9_P16	3.770e-07	1.000e-20
X11_P16	5.923e-07	1.000e-20
X14_P16	5.709e-07	1.000e-20
X15_P16	7.513e-07	1.000e-20
X19_P16	7.705e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P16	X5_P16	X8_P16	X9_P16
A to Z	1.714e-03	3.530e-03	3.485e-03	4.833e-03
B to Z	1.626e-03	2.786e-03	3.149e-03	3.818e-03
	X11_P16	X14_P16	X15_P16	X19_P16
A to Z	4.924e-03	7.691e-03	6.677e-03	9.281e-03
B to Z	4.483e-03	5.953e-03	6.037e-03	7.343e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

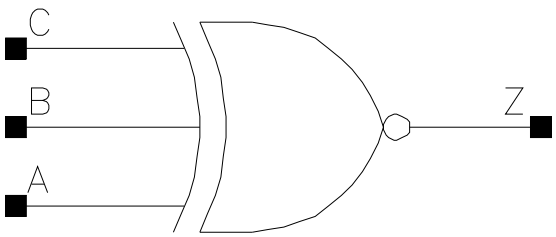
Pin Cycle (vdds)	X4_P16	X5_P16	X8_P16	X9_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P16	X14_P16	X15_P16	X19_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P16	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P16	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P16	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P16	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P16	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P16	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P16	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P16	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P16	C8T28SOIDV_LL_-XNOR3X4_P16	C8T28SOIDV_LL_-XNOR3X9_P16	C8T28SOIDV_LL_-XNOR3X13_P16
A	0.0017	0.0017	0.0022	0.0029
B	0.0016	0.0016	0.0021	0.0028
C	0.0007	0.0007	0.0007	0.0006
	C8T28SOIDV_LLS_-XNOR3X1_P16	C8T28SOIDV_LLS_-XNOR3X2_P16	C8T28SOIDV_LLS_-XNOR3X5_P16	C8T28SOIDV_LLS_-XNOR3X7_P16

A	0.0016	0.0019	0.0041	0.0063
B	0.0017	0.0019	0.0037	0.0058
C	0.0011	0.0014	0.0027	0.0040

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XNOR3X2_P16	C8T28SOIDV_LL_-XNOR3X4_P16	C8T28SOIDV_LL_-XNOR3X2_P16	C8T28SOIDV_LL_-XNOR3X4_P16
A to Z ↓	0.0601	0.0641	6.8121	3.7157
A to Z ↑	0.0563	0.0575	10.1703	5.4527
B to Z ↓	0.0604	0.0645	6.8108	3.7147
B to Z ↑	0.0571	0.0583	10.1748	5.4536
C to Z ↓	0.0809	0.0862	6.8081	3.7147
C to Z ↑	0.0769	0.0792	10.1703	5.4502
	C8T28SOIDV_LL_-XNOR3X9_P16	C8T28SOIDV_LL_-XNOR3X13_P16	C8T28SOIDV_LL_-XNOR3X9_P16	C8T28SOIDV_LL_-XNOR3X13_P16
A to Z ↓	0.0554	0.0627	1.8707	1.2858
A to Z ↑	0.0572	0.0643	2.6662	1.8576
B to Z ↓	0.0560	0.0632	1.8709	1.2852
B to Z ↑	0.0581	0.0655	2.6682	1.8576
C to Z ↓	0.0799	0.0946	1.8703	1.2850
C to Z ↑	0.0813	0.0966	2.6675	1.8577
	C8T28SOIDV_LLS_-XNOR3X1_P16	C8T28SOIDV_LLS_-XNOR3X2_P16	C8T28SOIDV_LLS_-XNOR3X1_P16	C8T28SOIDV_LLS_-XNOR3X2_P16
A to Z ↓	0.0362	0.0405	12.5582	7.0113
A to Z ↑	0.0378	0.0371	21.8233	11.3919
B to Z ↓	0.0371	0.0417	12.5637	7.0133
B to Z ↑	0.0386	0.0381	21.7917	11.3753
C to Z ↓	0.0357	0.0394	12.5494	7.0161
C to Z ↑	0.0376	0.0365	21.7216	11.3463
	C8T28SOIDV_LLS_-XNOR3X5_P16	C8T28SOIDV_LLS_-XNOR3X7_P16	C8T28SOIDV_LLS_-XNOR3X5_P16	C8T28SOIDV_LLS_-XNOR3X7_P16
A to Z ↓	0.0410	0.0354	3.3645	2.3382
A to Z ↑	0.0393	0.0345	5.6074	3.7536
B to Z ↓	0.0404	0.0342	3.3680	2.3427
B to Z ↑	0.0390	0.0339	5.5984	3.7484
C to Z ↓	0.0382	0.0328	3.3619	2.3416
C to Z ↑	0.0366	0.0320	5.5654	3.7335

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P16	2.507e-07	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P16	2.800e-07	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P16	4.573e-07	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P16	6.330e-07	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P16	1.925e-07	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P16	2.948e-07	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P16	6.629e-07	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P16	1.020e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P16	C8T28SOIDV_LL_-XNOR3X4_P16	C8T28SOIDV_LL_-XNOR3X9_P16	C8T28SOIDV_LL_-XNOR3X13_P16
A to Z	2.319e-03	2.687e-03	3.989e-03	6.502e-03
B to Z	2.258e-03	2.630e-03	3.912e-03	6.386e-03
C to Z	3.639e-03	4.061e-03	5.736e-03	9.182e-03
	C8T28SOIDV_LLS_-XNOR3X1_P16	C8T28SOIDV_LLS_-XNOR3X2_P16	C8T28SOIDV_LLS_-XNOR3X5_P16	C8T28SOIDV_LLS_-XNOR3X7_P16
A to Z	1.425e-03	2.065e-03	4.612e-03	6.357e-03
B to Z	1.338e-03	1.954e-03	4.234e-03	5.685e-03
C to Z	1.291e-03	1.920e-03	4.040e-03	5.455e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

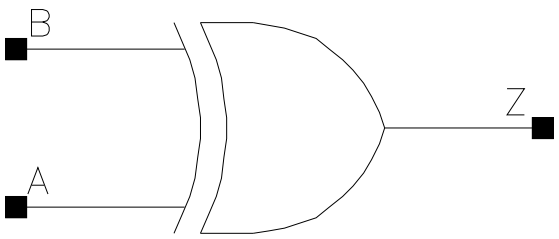
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P16	C8T28SOIDV_LL_-XNOR3X4_P16	C8T28SOIDV_LL_-XNOR3X9_P16	C8T28SOIDV_LL_-XNOR3X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P16	C8T28SOIDV_LLS_-XNOR3X2_P16	C8T28SOIDV_LLS_-XNOR3X5_P16	C8T28SOIDV_LLS_-XNOR3X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.360	1.0880
X4_P16	1.600	0.544	0.8704
X5_P16	0.800	1.360	1.0880
X8_P16	1.600	1.088	1.7408
X9_P16	0.800	1.496	1.1968
X12_P16	1.600	1.360	2.1760
X13_P16	0.800	2.176	1.7408
X15_P16	1.600	1.904	3.0464
X17_P16	0.800	2.312	1.8496
X18_P16	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P16	X4_P16	X5_P16	X8_P16
A	0.0005	0.0011	0.0007	0.0018
B	0.0011	0.0011	0.0012	0.0017
	X9_P16	X12_P16	X13_P16	X15_P16
A	0.0007	0.0029	0.0013	0.0034
B	0.0015	0.0022	0.0024	0.0028
	X17_P16	X18_P16		
A	0.0013	0.0017		
B	0.0024	0.0022		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X4_P16**	**X2_P16**	**X4_P16**
A to Z ↓	0.0505	0.0217	6.4883	3.4494
A to Z ↑	0.0468	0.0253	10.4679	9.6283
B to Z ↓	0.0383	0.0219	6.4426	3.4843
B to Z ↑	0.0387	0.0235	10.4626	9.6246
	X5_P16	**X8_P16**	**X5_P16**	**X8_P16**
A to Z ↓	0.0472	0.0280	3.5109	1.8834
A to Z ↑	0.0419	0.0300	5.2487	5.0461
B to Z ↓	0.0358	0.0288	3.4976	1.9031
B to Z ↑	0.0344	0.0284	5.2441	5.0420
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0460	0.0256	1.8513	1.2677
A to Z ↑	0.0423	0.0272	2.7349	3.3792
B to Z ↓	0.0354	0.0244	1.8461	1.2807
B to Z ↑	0.0342	0.0248	2.7350	3.3769
	X13_P16	**X15_P16**	**X13_P16**	**X15_P16**
A to Z ↓	0.0426	0.0276	1.2668	0.9879
A to Z ↑	0.0393	0.0310	1.8984	3.0069
B to Z ↓	0.0306	0.0262	1.2634	0.9987
B to Z ↑	0.0285	0.0284	1.8969	3.0042
	X17_P16	**X18_P16**	**X17_P16**	**X18_P16**
A to Z ↓	0.0450	0.0500	0.9615	0.9587
A to Z ↑	0.0410	0.0441	1.4219	1.3938
B to Z ↓	0.0332	0.0396	0.9598	0.9581
B to Z ↑	0.0304	0.0350	1.4212	1.3925

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X2_P16	1.845e-07	1.000e-20
X4_P16	2.390e-07	1.000e-20
X5_P16	2.805e-07	1.000e-20
X8_P16	3.857e-07	1.000e-20
X9_P16	4.326e-07	1.000e-20
X12_P16	5.891e-07	1.000e-20
X13_P16	7.029e-07	1.000e-20
X15_P16	7.126e-07	1.000e-20
X17_P16	7.586e-07	1.000e-20
X18_P16	7.687e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X2_P16	X4_P16	X5_P16	X8_P16
A to Z	2.653e-03	1.772e-03	3.330e-03	3.480e-03
B to Z	2.288e-03	1.629e-03	2.806e-03	3.372e-03
	X9_P16	X12_P16	X13_P16	X15_P16
A to Z	4.702e-03	5.042e-03	7.684e-03	6.504e-03
B to Z	4.049e-03	4.508e-03	4.890e-03	5.946e-03
	X17_P16	X18_P16		
A to Z	8.568e-03	9.492e-03		
B to Z	5.754e-03	7.085e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

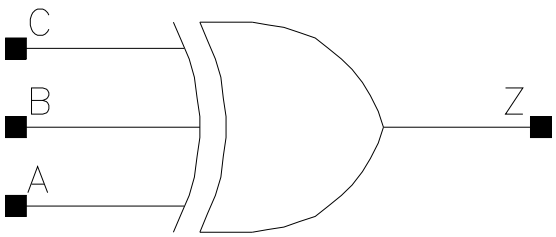
Pin Cycle (vdds)	X2_P16	X4_P16	X5_P16	X8_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P16	X12_P16	X13_P16	X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P16	X18_P16		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P16	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P16	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P16	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P16	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P16	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P16	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P16	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P16	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P16	C8T28SOIDV_LL_-XOR3X4_P16	C8T28SOIDV_LL_-XOR3X9_P16	C8T28SOIDV_LL_-XOR3X13_P16
A	0.0018	0.0017	0.0020	0.0029
B	0.0017	0.0017	0.0020	0.0027
C	0.0011	0.0011	0.0015	0.0023
	C8T28SOIDV_LLS_-XOR3X1_P16	C8T28SOIDV_LLS_-XOR3X2_P16	C8T28SOIDV_LLS_-XOR3X5_P16	C8T28SOIDV_LLS_-XOR3X7_P16

A	0.0018	0.0020	0.0033	0.0051
B	0.0019	0.0019	0.0031	0.0050
C	0.0006	0.0006	0.0006	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P16	**C8T28SOIDV_LL_-XOR3X4_P16**	**C8T28SOIDV_LL_-XOR3X2_P16**	**C8T28SOIDV_LL_-XOR3X4_P16**
A to Z ↓	0.0587	0.0644	6.8405	3.7282
A to Z ↑	0.0554	0.0593	10.4788	5.4579
B to Z ↓	0.0590	0.0653	6.8415	3.7277
B to Z ↑	0.0559	0.0606	10.4845	5.4619
C to Z ↓	0.0581	0.0642	6.8422	3.7273
C to Z ↑	0.0547	0.0590	10.4816	5.4628
	C8T28SOIDV_LL_-XOR3X9_P16	**C8T28SOIDV_LL_-XOR3X13_P16**	**C8T28SOIDV_LL_-XOR3X9_P16**	**C8T28SOIDV_LL_-XOR3X13_P16**
A to Z ↓	0.0584	0.0642	1.8579	1.2596
A to Z ↑	0.0586	0.0653	2.6826	1.8071
B to Z ↓	0.0595	0.0650	1.8574	1.2590
B to Z ↑	0.0598	0.0666	2.6849	1.8074
C to Z ↓	0.0580	0.0642	1.8573	1.2588
C to Z ↑	0.0578	0.0660	2.6851	1.8080
	C8T28SOIDV_LLS_-XOR3X1_P16	**C8T28SOIDV_LLS_-XOR3X2_P16**	**C8T28SOIDV_LLS_-XOR3X1_P16**	**C8T28SOIDV_LLS_-XOR3X2_P16**
A to Z ↓	0.0382	0.0420	8.9936	7.1624
A to Z ↑	0.0381	0.0371	15.6280	10.8762
B to Z ↓	0.0391	0.0427	9.0135	7.1629
B to Z ↑	0.0388	0.0375	15.6273	10.8640
C to Z ↓	0.0602	0.0651	8.9768	7.1190
C to Z ↑	0.0612	0.0610	15.6267	10.8281
	C8T28SOIDV_LLS_-XOR3X5_P16	**C8T28SOIDV_LLS_-XOR3X7_P16**	**C8T28SOIDV_LLS_-XOR3X5_P16**	**C8T28SOIDV_LLS_-XOR3X7_P16**
A to Z ↓	0.0555	0.0478	3.7100	2.5751
A to Z ↑	0.0459	0.0401	5.6560	3.8223
B to Z ↓	0.0532	0.0474	3.7157	2.5776
B to Z ↑	0.0449	0.0400	5.6463	3.8167
C to Z ↓	0.0899	0.0752	3.7175	2.5674
C to Z ↑	0.0820	0.0680	5.6449	3.8095

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P16	2.185e-07	1.000e-20
C8T28SOIDV_LL_XOR3X4_P16	2.507e-07	1.000e-20
C8T28SOIDV_LL_XOR3X9_P16	4.103e-07	1.000e-20
C8T28SOIDV_LL_XOR3X13_P16	6.008e-07	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P16	2.866e-07	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P16	3.296e-07	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P16	5.656e-07	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P16	8.641e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P16	C8T28SOIDV_LL_-XOR3X4_P16	C8T28SOIDV_LL_-XOR3X9_P16	C8T28SOIDV_LL_-XOR3X13_P16
A to Z	2.233e-03	2.706e-03	4.052e-03	6.921e-03
B to Z	2.128e-03	2.620e-03	3.933e-03	6.734e-03
C to Z	2.077e-03	2.563e-03	3.892e-03	6.710e-03
	C8T28SOIDV_LLS_-XOR3X1_P16	C8T28SOIDV_LLS_-XOR3X2_P16	C8T28SOIDV_LLS_-XOR3X5_P16	C8T28SOIDV_LLS_-XOR3X7_P16
A to Z	1.704e-03	2.086e-03	4.106e-03	5.792e-03
B to Z	1.674e-03	2.014e-03	3.911e-03	5.488e-03
C to Z	3.268e-03	3.740e-03	6.862e-03	9.677e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P16	C8T28SOIDV_LL_-XOR3X4_P16	C8T28SOIDV_LL_-XOR3X9_P16	C8T28SOIDV_LL_-XOR3X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P16	C8T28SOIDV_LLS_-XOR3X2_P16	C8T28SOIDV_LLS_-XOR3X5_P16	C8T28SOIDV_LLS_-XOR3X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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