DK CMOS028FDSOI

User Manual

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1 - IMPORTANT NOTE

The present document is designed to explain how to use Calibre DRC within the cmos028FDSOI DK.

2 - SET-UP

The Calibre Layout Verification Module is included in this Design Kit. No supplementary manipulation should be done to access the layout verification features. You must setup the Calibre version to the qualified version, indicated in the release notes.

Warning:
- Always read the release notes before using the related DRC.

3 - LAYOUT VERIFICATION RELATED FILES AND VARIABLES WITHIN THE DK

3.1 - ARCHITECTURE & FILES

- $DKITROOT/DATA/CALIBRE : contains all verification files
- $DKITROOT/doc : contains the DK documentation

3.2 - COMMON VARIABLES

Variable	Usage
DKITROOT/DATA/CALIBRE	Location of the Layout Verification Module
U2DK_CALIBRE_TVF_PACK	Location of all tvf files except antenna ones
U2DK_CALIBRE_ANTENNA_TVF_PACK	Location of all antenna tvf files

Note: TVF stands for TCL Verification Language. It is a higher level language, which is used by Calibre to generate a SVRF technology file.

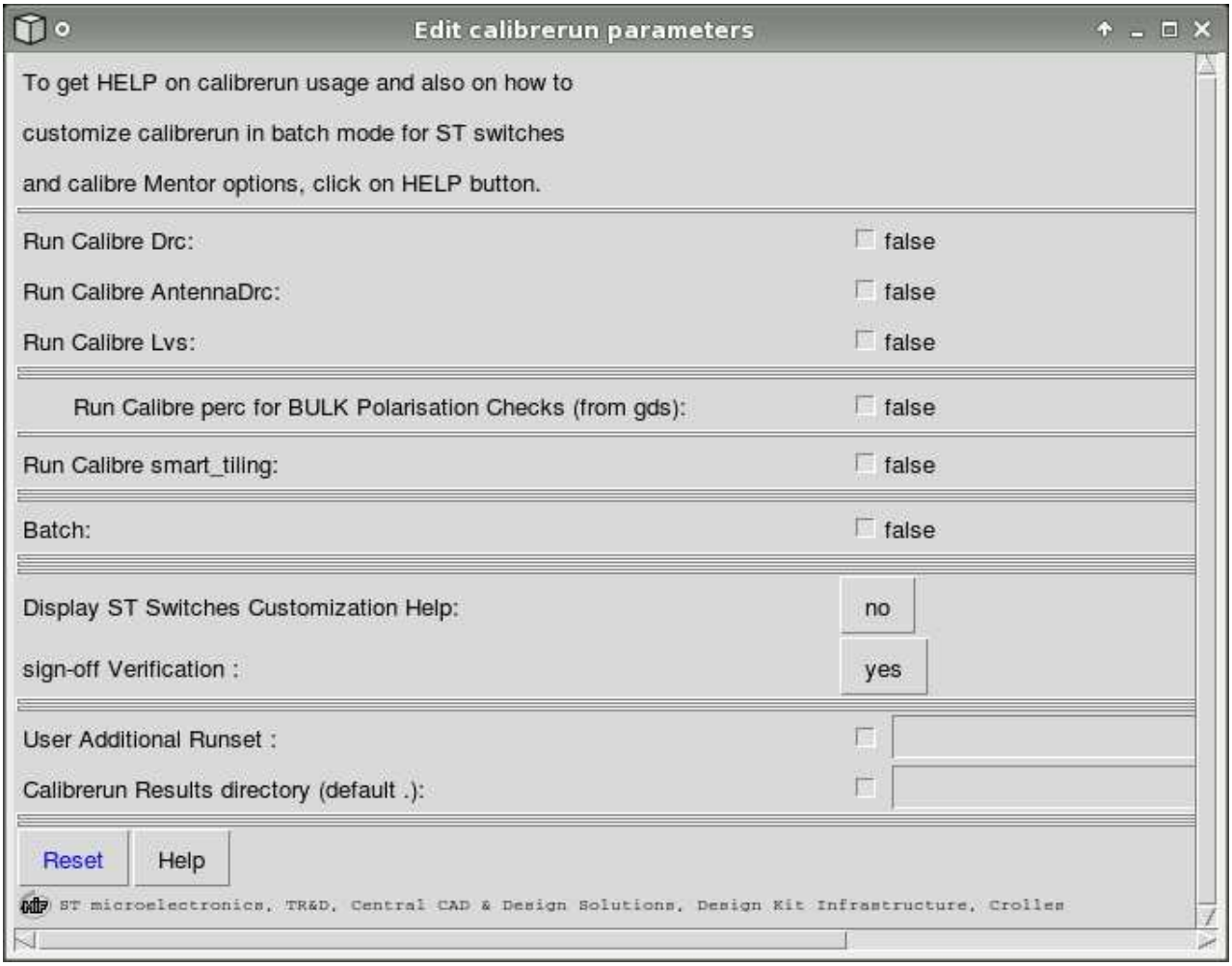
3.3 - DRC VARIABLES

Variable	Usage
MGC_CALIBRE_DRC_RUNSET_FILE	DRC calibre runset file
U2DK_CALIBRE_DRC_DECK	Full DRC TVF main file
U2DK_CALIBRE_ANTENNA_DRC_DECK	Antenna only DRC TVF main file
CTK_CALIBRE_DRC_GEN_TEMPLATE	Script used to generate template file

4 - LAYOUT VERIFICATION FROM UNIX: CALIBRERUN

4.1 - CALIBRERUN

Calibrerun is a DK interface which allows to run Calibre for DRC with secured behaviour.
From Unix terminal, you just have to execute: `calibrerun -gui`

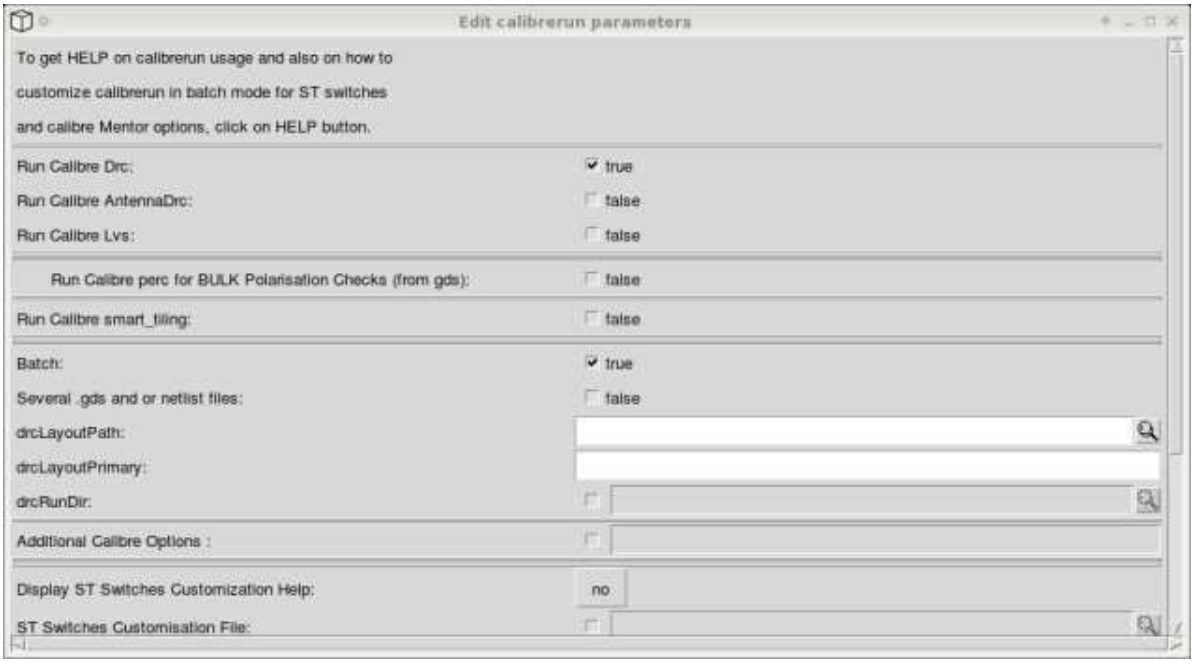


4.2 - GRAPHICAL USER INTERFACE

You just have to select the wanted feature:

- Run Calibre DRC: for a full DRC check
- Run Calibre AntennaDRC: for a antennal DRC check only

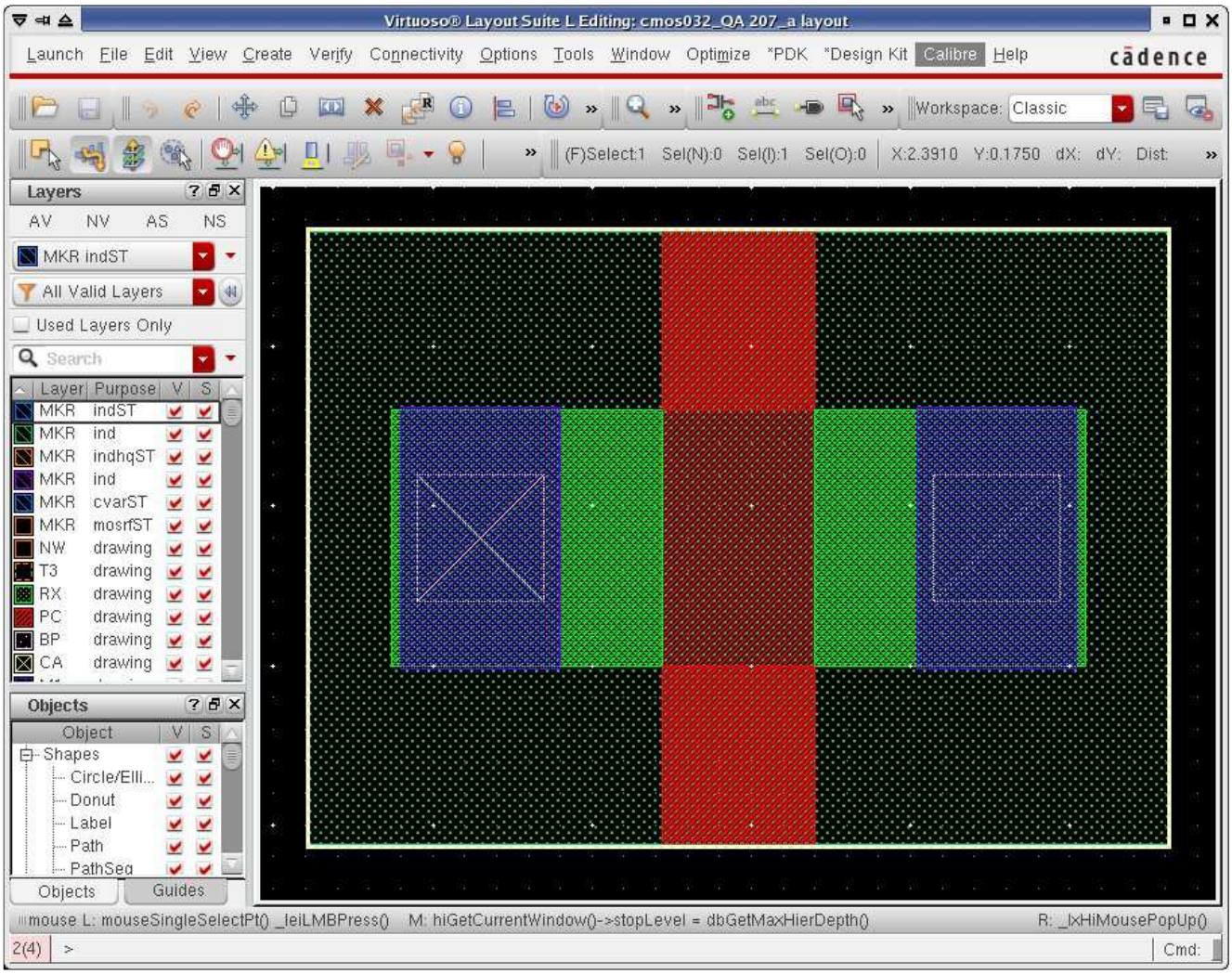
You can also select the mode into you want Calibre to be launched: Gui mode or batch mode.
If Batch mode is selected, some additional fields will appear:



Then click 'Ok' and Calibre Gui or Batch is executed.

5 - LAYOUT VERIFICATION FROM CADENCE VIRTUOSO

5.1 - CALIBRE MENU



Calibre Menu from Virtuoso

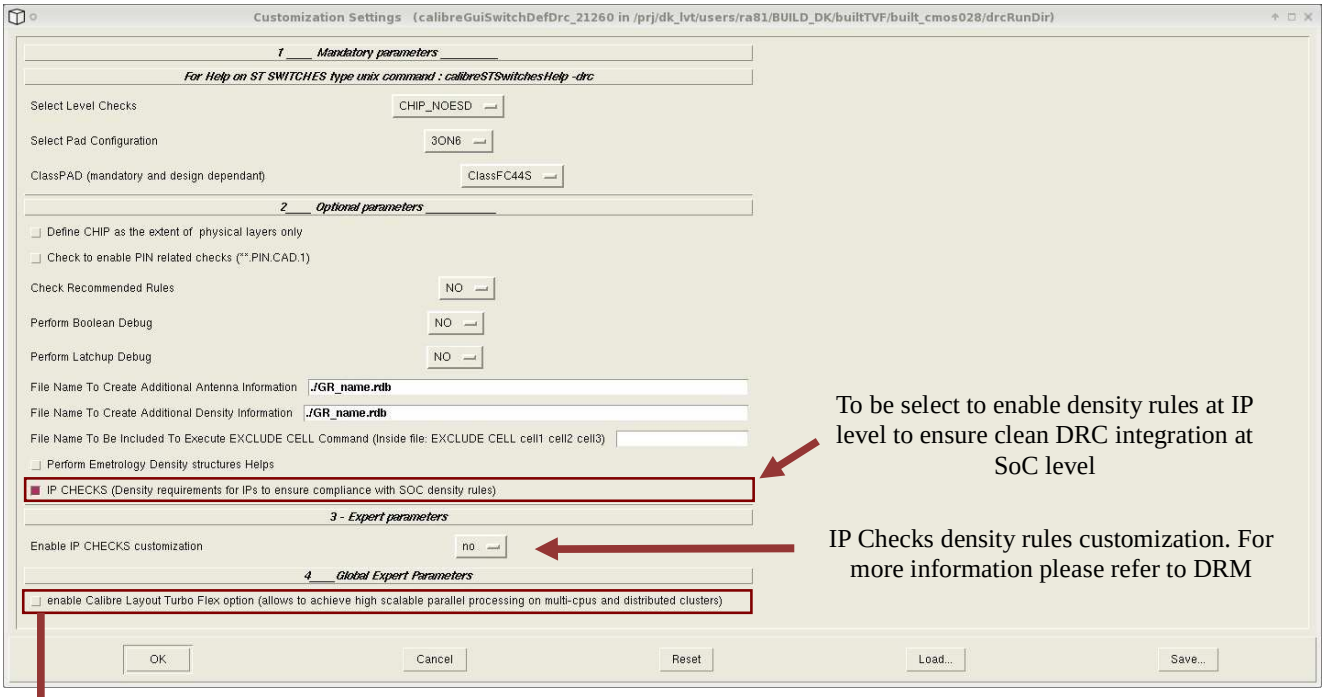
Click on 'Run DRC' for DRC.

6 - CALIBRE DRC

6.1 - ABOUT TVF

The DRC deck is partially coded in tvf and SVRF. The cockpit is in tvf (encrypted) and the DRC heart is in svrf (clear).

6.2 - CUSTOMIZATION CHOICES

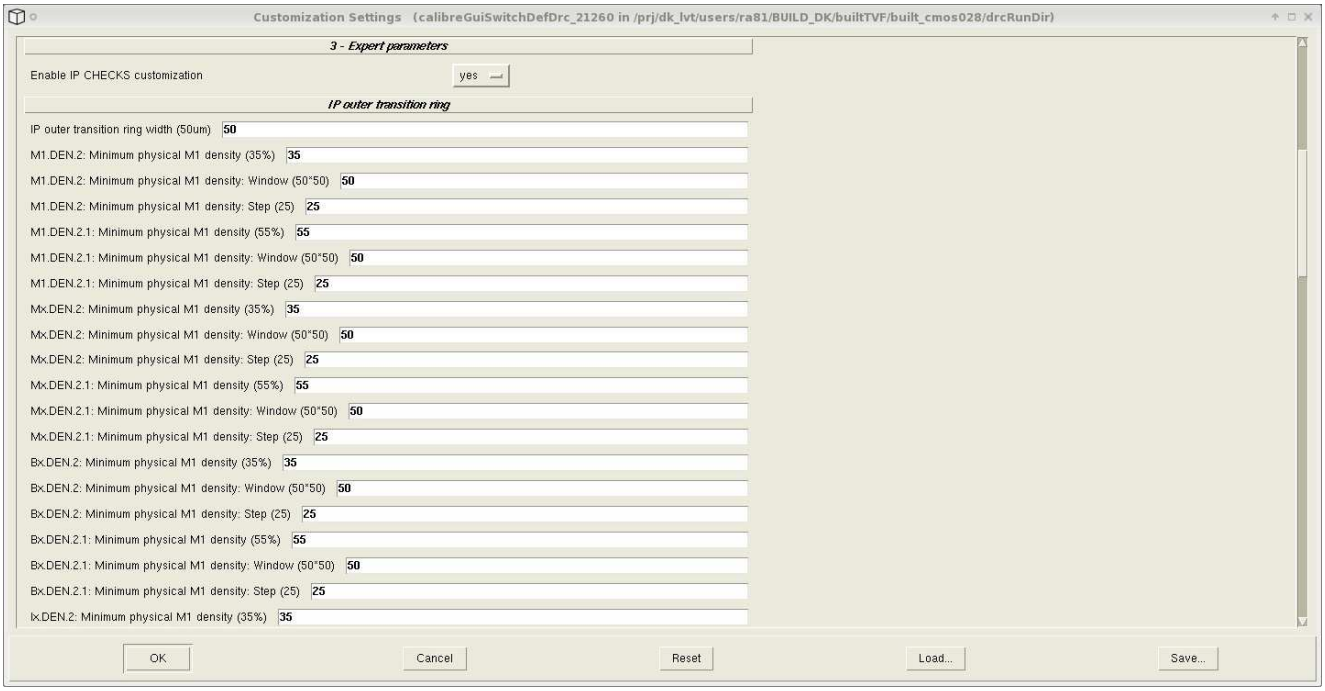


Customization window

Checked by default. Checked it generates the command **LAYOUT TURBO FLEX YES.** It is recommended to leave this option checked for large and very “hierarchical” circuits to reduce DRC runtime.

	*“Enable IP CHECKS customization” set to “yes” is* ***not Sign-Off***

	*When enable IP CHECKS customization?* • Only for the purpose of doing R&D • For IP designer, it makes sense to reduce the Step value (but increase runtime) but not the Window size



Customization window when IP CHECKS customization enabled

Note: STSwitchHelps utility is available from any UNIX terminal where the DesignKit has been loaded. It aims at providing help on switch usage of Layout Verification and Finishing features.

Usage: STSwitchHelps [-<EDATool>] [-<feature>]

Further help on STSwitchHelps feature is available with "STSwitchHelps -h" UNIX command.

6.3 - GUIDELINES FOR CALIBRE RUNS @ ST

The following guidelines are intended to help complete any Calibre run, PV (DRC, LVS) or DFM (SmartFill, CFA, CAA), overnight at first trial, with leveraging typical ST environment.

6.3.1 - SOFTWARE PREREQUISITES

Product	Version	Min	Recommended
OS	RHEL	5	6

DRM (Distributed Resource Manager)	Platform LSF	7	8
Calibre	Linux 64-bit	2013.2_18.13	last release

6.3.2 - LSF SERVER CONFIGURATION

- Queues should be preset with following user rights:

Job	Graphical user interface	Large memory usage (min 32GB, recommended 128GB)	Long run (even if low CPU usage)	Many CPUs (min 48, recommended 96)
Calibre Interactive	**X**		**X**	
Calibre master job		**X**	**X**	
Calibre slave jobs		**(X)**	**X**	**X**

- Log files on remote hosts should get automatically saved and stored in a directory which isn't removed at the end of the run.

6.3.3 - CALIBRE INTERACTIVE RUN CONTROL SETTINGS

The Calibre Interactive run control must be set like indicated in this part to allow to use large resources easily, in particular:

- **Mode**: all the following options must be set correctly
  - ✓ **Distributed (MTFlex)**
  - ✓ **Hyperscale**
  - ✓ **Remote Data Server (RDS)** with argument "**1**"
  - ✓ **Hyperscale Remote**
  - **Backup Data** may be left unselected by default
  - ✓ custom switch generating the command **LAYOUT TURBO FLEX YES**, selected by default.

- **Resources**:
  - ✓ **Show Details**
  - **Master Host Selection**

Min CPUs	Type	Min Memory	Resource Options	Submit Options	Matching Hosts	Wait	Port	Count	Min Count	Name
			select[type==%o] rusage[mem=%m] span[hosts=1]	**-q master -n %c**		300				

  - %c, %o, and %m respectively refer to the values in columns Min CPUs, Type and Min Memory.

- Wait ***300*** will let Calibre 5mn to acquire hosts (default 60 is usually too short for many CPUs on LSF).
- ***master*** should be substituted by the name of the queue (see paragraph 3 for rights).
- Count should be left empty so that the value Total CPUs (in Remote Hosts Selection) gets used. Indeed, if both are provided, Count value is used, which may be confusing in mode LAUNCH CLUSTER.
- Min Count defines the minimum number of CPUs which must be available on remote hosts to allow start when not all CPUs requested could get acquired. Typically it can be set to Total CPUs/2. When not provided, Min Count defaults to Total CPUs (or Count if provided).
- The same settings (without Details) should be separately preset as well in mode "Multi-Threaded".

- **Remote Host Selection**

Use	Total CPUs	Min CPUs Per Host	Type	Min Memory	Resource Options	Submit Options	Matching Hosts
					select[type==%o] rusage[mem=%m] span[ptile=%c]	-q **slave**	

- %c, %o, and %m respectively refer to the values in columns Min CPUs Per Host, Type and Min Memory (Per Host).
- ***slave*** should be substituted by the name of the queue (see paragraph 3 for rights).
- Multiple complete groups of %c CPUs can get acquired per remote host, based on availability (selection is up to LSF). For instance, on each 12-CPU remote host, %c=2 allows to acquire 2, 4, 6, 8, 10 or 12 CPUs, but %c=8 doesn't allow to select more or less than 8 CPUs.
- It is not needed to specify more Submit Options as Calibre Interactive will automatically generate the –n and –J options based on Total CPUs (%t) and Min CPUs Per Host (%c):
  ex1: %t=80, %c=4 generates the command ***bsub*** –o log **–J "calibre.job[1-20]" –n 4** –R "…[ptile=4]" –q slave _cluster.slave_ $host $port 4
  ex2: %t=150, %c=4 generates the commands ***bsub*** –o log **–J "calibre.job[1-36]" –n 4** –R "…[ptile=4]" –q slave _cluster.slave_ $host $port 4 ***bsub*** –o log **–J "calibre.job[37-38]" –n 3** –R "…[ptile=3]" –q slave _cluster.slave_ $host $port 3 Note that the configuration 36x4+2x3 is preferred over 37x4+1x2.
- For finer remote hosts selection, click Right Mouse Button > Add Hosts.

6.3.4 - GUIDELINES TO RUN OVERNIGHT

Performance primarily depends on technology node (minimum dimensions of the layout and complexity of the ruledeck). The following guidelines are intended to 32/28nm, based on experiments on ST ruledecks and designs.

- **Number of CPUs**

#CPUs	Min	Recommended
Total on master host	1 per ~50mm2	1 per ~5mm2
Total on remote hosts	4x #CPUs on master host	8x #CPUs on master host

Per remote host	1	4

E.g., for a 160mm² design, a 8-CPU master host + 12 4-CPU remote hosts is a correct configuration.

- **Memory**

Memory	Min	Recommended
On master host	4GB per CPU	8GB per CPU
On remote hosts	2GB per CPU	4GB per CPU

E.g. a 8-CPU master host should have at least 32GB, and each 4-CPU remote host should have at least 8GB.

- **Defaults**

As a trade-off between the ideal configuration to run any full chip overnight and the resources available at ST, we suggest the Design Kit to always default to the following values. Note, memory requirements are provided in MB.

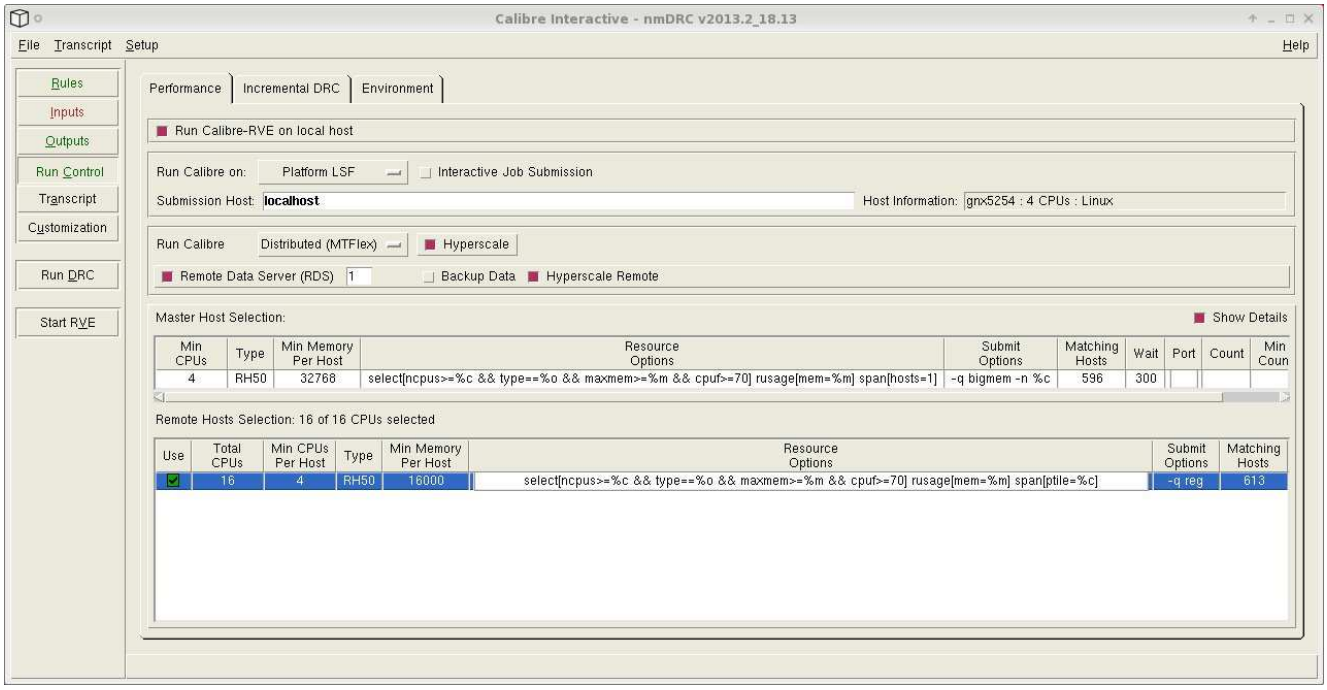
- **Master Host Selection**

Min CPUs	Type	Min Memory	Resource Options	Submit Options	Matching Hosts	Wait	Port	Count	Min Count	Name
8	**RH50**	**32768**	**select[type==%o] rusage[mem=%m] span[hosts=1]**	**-q master -n %c**		300			24	

- **Remote Host Selection**

Use	Total CPUs	Min CPUs Per Host	Type	Min Memory	Resource Options	Submit Options	Matching Hosts
I	**48**	**4**	**RH50**	**8192**	**select[type==%o] rusage[mem=%m] span[ptile=%c]**	-q **slave**	

- Optionally, multiple configurations can be proposed, with one of them being selected by default.



An example of a run control for a large chip

6.4 - HOW TO READ AND DEBUG ANTENNA RULES

For more comprehension, we are going to consider FD_131b_Gate_V1 antenna rule.

6.4.1 - HOW TO READ

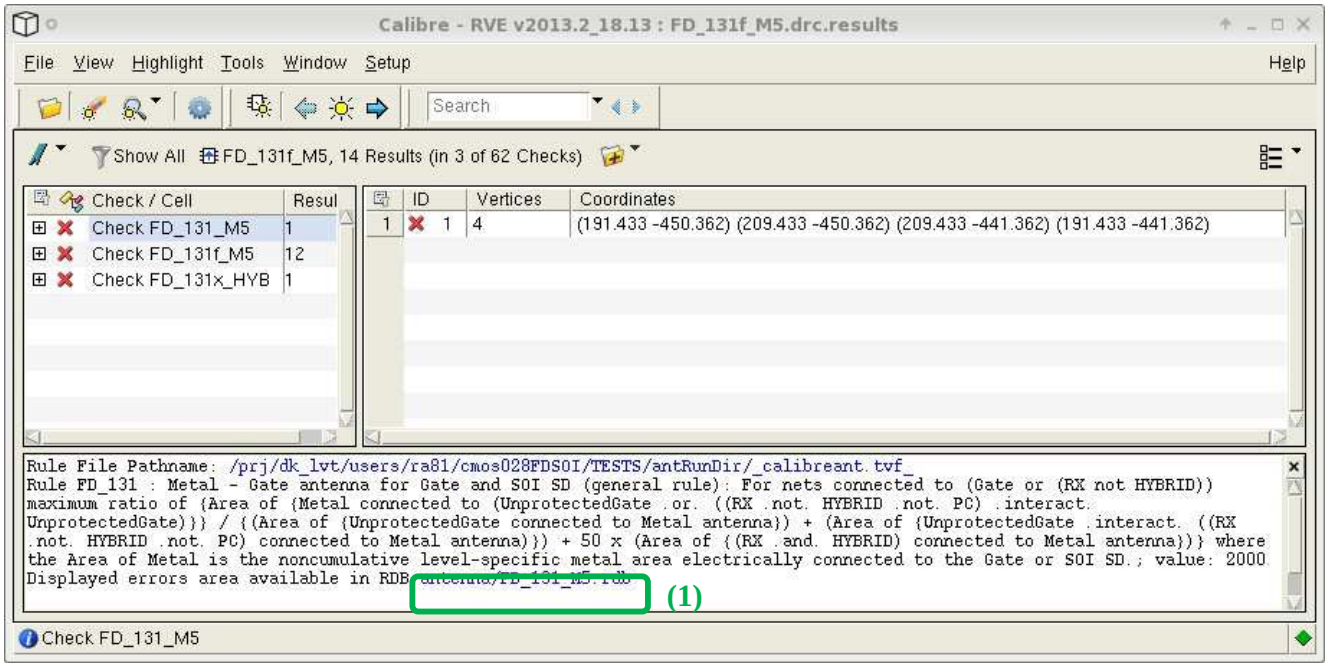
1/ Open DFM RDB file via Calibre -RVE of the rule if available (Cf. Figure)

2/ In the DFM RDB file you can have the area of all layer involved in the rule but also the value of the ratio. (Cf. Figure)

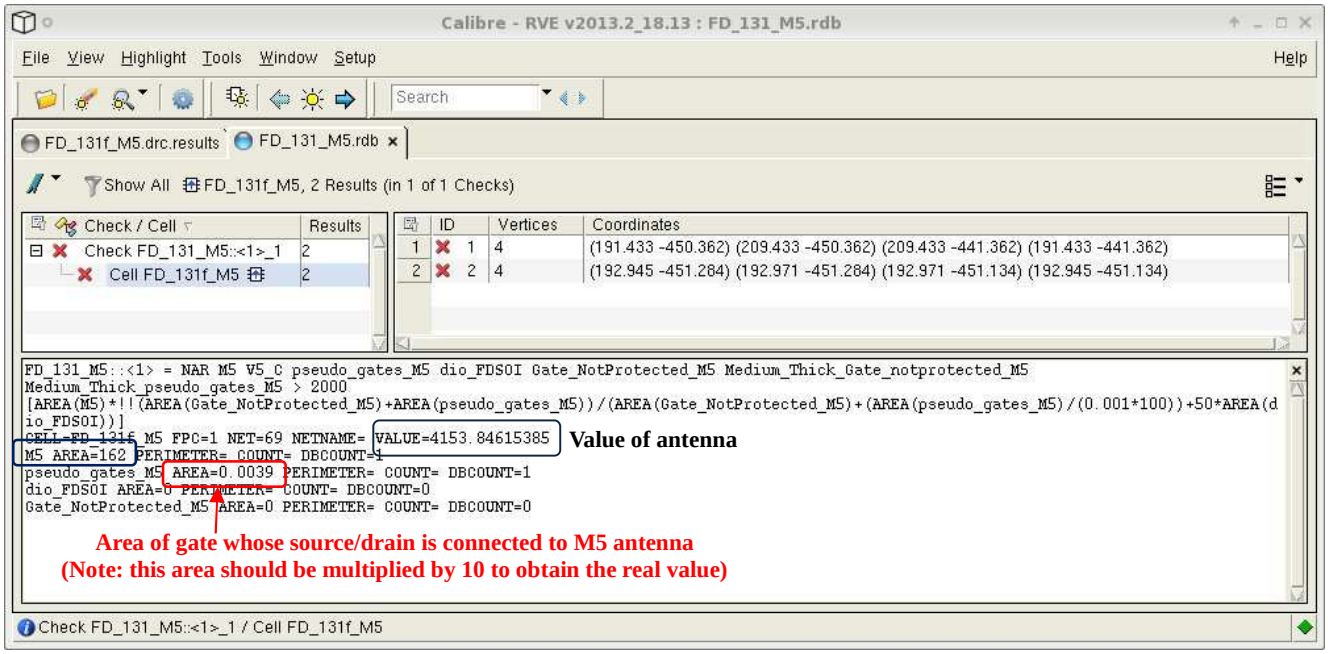
6.4.2 - HOW TO DEBUG

So far, only the gate is highlighted in the layout editor for FD_131_M5 DRC error but how to do to highlight all layers involved in the antenna error.

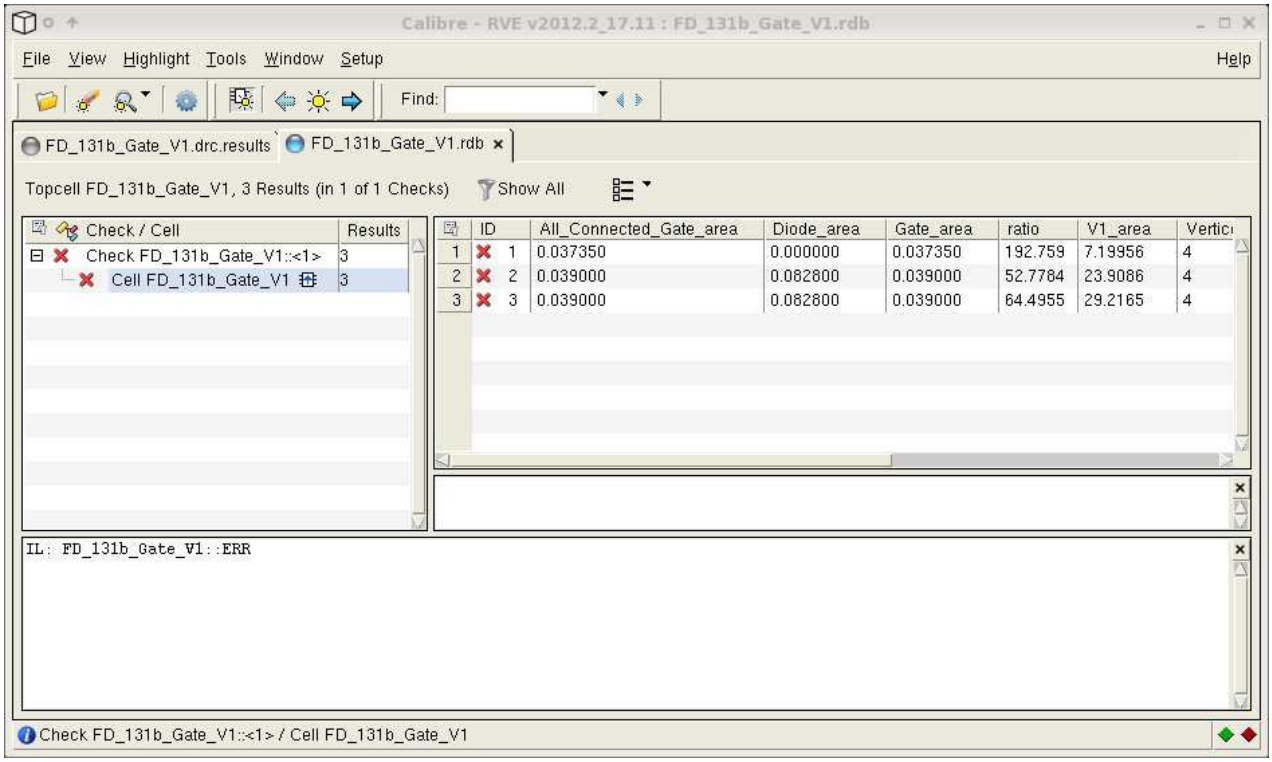
1/ we must access to the RDB data in a new tab by clicking on green rounded rectangle **(1)**



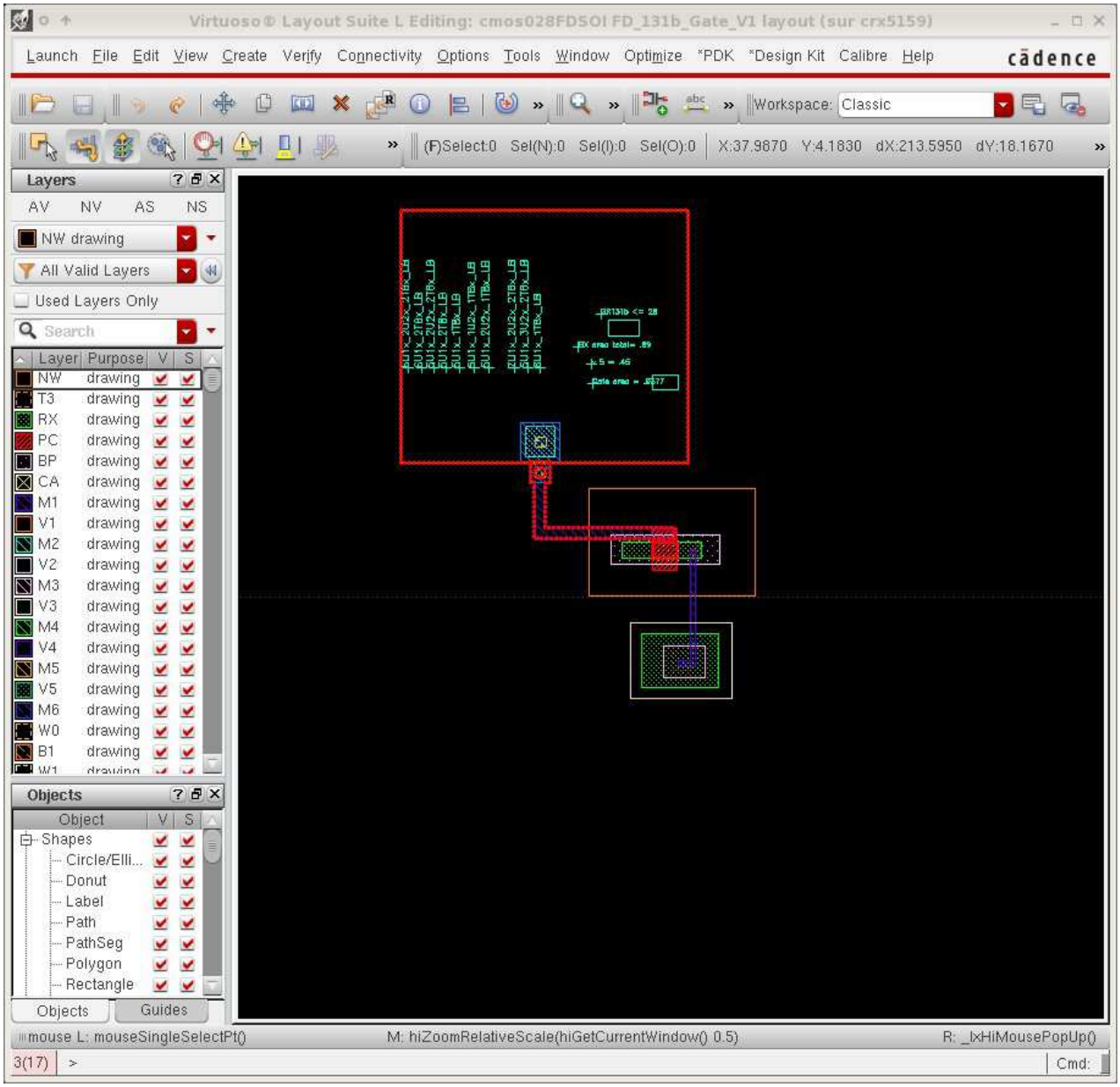
2/ Go in the new Tab, display the error shapes and have a look at the values



Area of M5 antenna



Example of DFM RDB file content



How all layer involved in antenna DRC errors are highlighted with Antenna Debug

NB: If you don't need to check Antenna rules, you can choose "CHIP_NOESD_NOANT" Level Checks.

6.5 - SWITCHES DESCRIPTION

Switch name	Default value	Choice	Description
DESIGN_TYPE	CHIP-SignOff (Sign-Off)	CHIP-SignOff IP-Validation CUSTOM	CHIP-SignOff (Selects full chip as well as anteanna rules; ESD checks are not selected.) Recommended for DRC at SoC level. It corresponds to the Sign-Off DRC where only ClassPAD can be customized. IP-Validation (Selects cell level checks as well as antenna rules; ESD checks are not selected). Recommended for DRC at IP level where only ClassPAD can be customized. CUSTOM (Selects full chip as well as anteanna rules; ESD checks are not selected). You can access sign-off switches and change their value. This can help during development phase in order to automatically unselect some type of rules.
MINIMUM_DENSITY_RULES_ENABLED	YES	YES NO	Enable minimum density rules
CHECK_PAD_ASSEMBLY	checked	Not checked Checked	Enable in order to run pad assembly rules
ClassPAD	ClassFC44S	ClassFC44S ClassFC61A ClassFC52A ClassWB47SR	Enable which type of ClassPAD rules you want to turn on
RECOMMENDED_RULES	NO	YES NO	If set to YES runs rules in the manual with an "R" suffix, (Recommended rules). Defaults to "NO", do not run Recommended rules.
BOOLEAN_DEBUG	NO	YES NO	If set to YES will output the generated boolean layers that touch a failing boolean check. Since the generated levels are fairly complicated, this option should aid in the debugging of the rule. Default is not to output this generated layer.
File Name To Create Additional Antenna Information	./GR_name.rdb	Not Applicable	Set environmental variable ANTENNA_RESULTS to the name of a file where additional antenna information will be

			created in a CalibreRVE format database in the start-up directory. Defaults to ./GR_name.rdb if not specified. (i.e. ./GR130a.rdb) Suggestion: "antenna.results"
File Name To Create Additional Density Information	**./GR_name.rdb**	**Not Applicable**	**Set environmental variable DENSITY_RESULTS to the name of a file where additional density information will be created in a CalibreRVE format database in the start-up directory. Defaults to ./GR_name.rdb if not specified. (i.e. ./GR40.rdb) Suggestion: "density.results"**
File Name Included To Execute The EXCLUDE CELL Command		**Not Applicable**	**Can be set in the environment to pass a string of a filename that will be included to execute the EXCLUDE CELL command. (Inside file: EXCLUDE CELL cell1 cell2 cell3) The default is no cells are excluded.**
Define CHIP as extent of physical layers only	**Not checked**	**Not checked Checked**	**If checked will modify the definition of CHIP layer which will become: CHIP=EXTENT ALL_PHYSICAL_LAYER**
LUP_DEBUG	**NO**	**YES NO**	**If set to YES will activated a few rules: - Corresponding to each LUP derived geometry listed in DRM - Corresponding to IO Pads and Supply Pads - Ex: LUP_Emitter_20um_around corresponding to 20um area around and Emitter. Useful for debug.**
IP CHECKS	**Not checked**	**Not checked Checked**	**If checked, this switch will add in the DK density checks at IP level. Density design rules must be checked on the IPs, before the tiles removal for the IP release. The compliance of those density rules at IP level will guarantee the compliance of the density design rules at SoC level. The non compliance with those density rules at IP level must be discussed with the SoC designer. You can after customize density check. IP Checks density rules group (*DENSITY_IP_CHECKS*) has been created to speed up IP verification.**
METRO_TILE	**checked**	**Not checked Checked**	**If checked will enable Placement Design Rules for embedded metrology structures (*Perform Emetrology Density structures checks*)**

METRO_HELP	**Not checked**	**Not checked** **Checked**	**If checked will enable Rules which will help to debug embedded metrology structures rules**
ANTENNA_DEBUG	**NO**	**YES** **NO**	**f set to YES will permit to catch the considered connection in the design**
VOLTAGE_DEBUG	**NO**	**YES** **NO**	**If set to YES this will perform high voltage** **Rules Debug**
EMET_POST_SWAP_RULES **_ENABLED**	**NO**	**YES** **NO**	**Active specific post SWAP rules**
density_STAT	**Not Checked**	**Not checked** **Checked**	**If set to YES, will generate all statistic density rdb files**
Advanced Pad Checker	**Not Checked**	**Not checked** **Checked**	**Allow advanced density rules for Pad**