C28SOI_SC_12_COREPBP16_LR

Release Notes and Known Problems and Solutions

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 16 nm

1 Release Notes

1.1 Product Release Information

Table 1. Product Identification

Parameter	Description
Library name	C28SOI_SC_12_COREPBP16_LR
Library version	5.1
Library type	Standard Cells
Technology	CMOS028_FDSOI

1.2 Related Documentation

- StandardCell_Notes.pdf Present in Design Package
- User Manual C28SOI_SC_12_COREPBP16_LR_um.pdf present in doc directory of Product itself.
- Datasheets C28SOI_SC_12_COREPBP16_LR_*_ds.pdf present in doc directory of Product itself.

2 Release Details

2.1 Current Release Details, Version 5.1

- Dummy Poly in layout across various cells has been cut for DFM robustness.
- Verilog Model for below cells have been updated to enable proper checking of E-CP timing checks.

C12T28SOI_LR_DFPHQNX17_P16	C12T28SOI_LR_DFPHQNX33_P16
C12T28SOI_LR_DFPHQNX8_P16	C12T28SOI_LR_DFPHQX17_P16
C12T28SOI_LR_DFPHQX33_P16	C12T28SOI_LR_DFPHQX8_P16
C12T28SOI_LR_SDFPHRQNX17_P16	C12T28SOI_LR_SDFPHRQNX33_P16
C12T28SOI_LRHF_SDFPHRQNX4_P16	C12T28SOI_LR_SDFPHRQNX8_P16
C12T28SOI_LR_SDFPHRQX17_P16	C12T28SOI_LR_SDFPHRQX33_P16
C12T28SOI_LRHF_SDFPHRQX4_P16	C12T28SOI_LR_SDFPHRQX8_P16

- Verilog Model for Combinational cells has been updated to enable simulation of ring oscillators and other combinatorial loop in non-timing mode i.e. without sdf timing.
- Total 48 cells have been updated for Robustness relative to contact punch through effect. Minimum Enclosure of 20nm for RX/CA has been ensured. There is no change in Cell Area and Abstract because of contact robustness update.
  - Updated cells are-

C12T28SOI_LR_AND2X25_P16	C12T28SOI_LR_AND3X25_P16
C12T28SOI_LR_AND4X27_P16	C12T28SOI_LR_AND4X4_P16
C12T28SOI_LR_AO112X8_P16	C12T28SOI_LR_AOI13X38_P16
C12T28SOI_LR_AOI211X17_P16	C12T28SOI_LR_BFX29_P16
C12T28SOI_LR_BFX33_P16	C12T28SOI_LRBR0P6_NAND3X12_P16
C12T28SOI_LR_CB4I1X17_P16	C12T28SOI_LR_DFPQNX30_P16
C12T28SOI_LR_DFPQX17_P16	C12T28SOI_LR_DFPQX30_P16
C12T28SOI_LR_DFPQX33_P16	C12T28SOI_LR_DFPRQNX17_P16
C12T28SOI_LR_DFPRQNX30_P16	C12T28SOI_LR_DFPRQX17_P16
C12T28SOI_LR_DFPRQX30_P16	C12T28SOI_LR_DFPSQX30_P16
C12T28SOI_LRHF_SDFPRQX4_P16	C12T28SOI_LR_IVX4_P16
C12T28SOI_LR_MUX21X8_P16	C12T28SOI_LR_MUX41X8_P16
C12T28SOI_LR_MUXI21X5_P16	C12T28SOI_LR_MX41X27_P16
C12T28SOI_LR_MX41X7_P16	C12T28SOI_LR_NAND2X50_P16
C12T28SOI_LR_NAND3AX24_P16	C12T28SOI_LR_NOR2X3_P16
C12T28SOI_LR_NOR4ABX13_P16	C12T28SOI_LR_NOR4X32_P16
C12T28SOI_LR_OAI112X10_P16	C12T28SOI_LR_OAI112X21_P16
C12T28SOI_LR_OAI211X10_P16	C12T28SOI_LR_OAI211X21_P16
C12T28SOI_LR_OAI222X9_P16	C12T28SOI_LR_OAI22X10_P16
C12T28SOI_LR_OAI22X15_P16	C12T28SOI_LR_OR2ABX16_P16
C12T28SOI_LR_OR2ABX24_P16	C12T28SOI_LR_OR2X8_P16
C12T28SOI_LRS1_FA1X8_P16	C12T28SOI_LR_SDFPRQNTX17_P16
C12T28SOI_LR_SDFPRQNTX33_P16	C12T28SOI_LR_SDFPRQNTX8_P16
C12T28SOI_LR_SDFPRQTX17_P16	C12T28SOI_LRS_NOR2X34_P16

- To enable support for Cadence Voltus Flow, CCS-Power has been added.

- Cells has been characterized with new Spice Cards. Therefore there is update in Timing & Power Information in libs.
- The product has been aligned to DP28FDSOI 2.5 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Global Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

2.2 Version 4.0

- The product is aligned to DP28FDSOI 2.4 in terms of Characterization Specifications and CAD views support. Refer to Design Package Documents for more details.
- For Specific Updates and Features related to Standard Cell Library, Refer to StandardCell_Notes.pdf Present in Design Package.

3 Known Problems and Solutions

3.1 DP related Generic Problems

- For Generic Standard cell Library related problem for this DP, please refer to KPS section inside StandardCell_Notes.pdf Present in Design Package.

3.2 Placement Restriction

➥ Specific Placement restriction due to Poly Landing pad

☞ Placement restriction has been modelled in CADENCE LEF - through “Symmetry property” and in SYNOPSYS FRAM - through “spacing_label property” for the following cells:

- C12T28SOI_LR_IVX4_P16
- C12T28SOI_LR_IVX6_P16
- C12T28SOI_LR_IVX8_P16

	*As mentioned above, modelling the placement constraint is different between Synopsys and Cadence. Therefore Need to be careful, if You do P&R with Synopsys and then go inside Cadence, the placement created by ICC could be declared as invalid by Encounter tool.*

4 Contact Information

For more information about this product/IP/Library or any problems or suggestions, please contact **HELPDESK** (http://col2.cro.st.com/helpdesk).

Non-ST users, please contact the respective Customer Support.

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