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C28SOI_SC_12_CLK_LR Databook

12 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

Overview

- C28SOI_SC_12_CLK_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 332 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

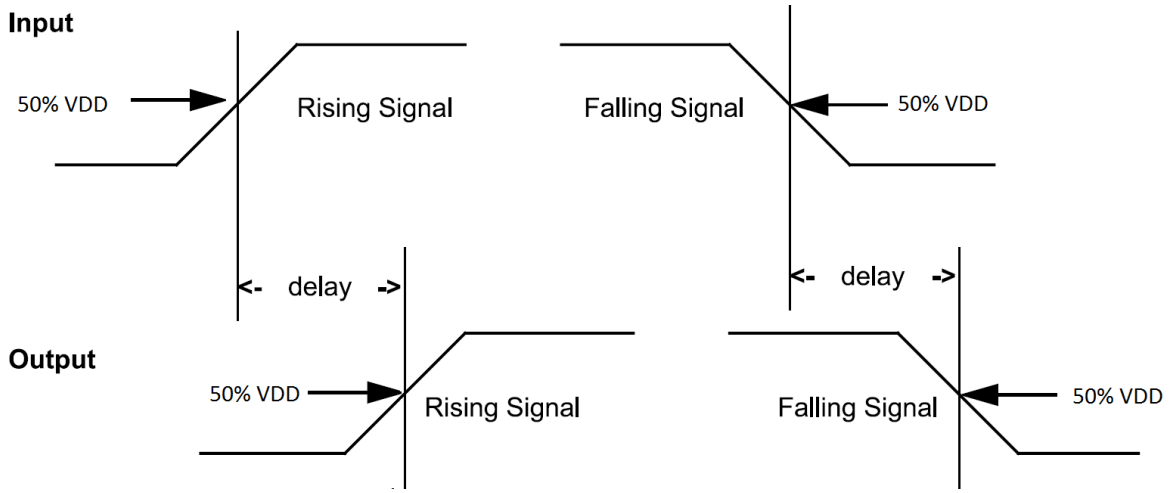


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

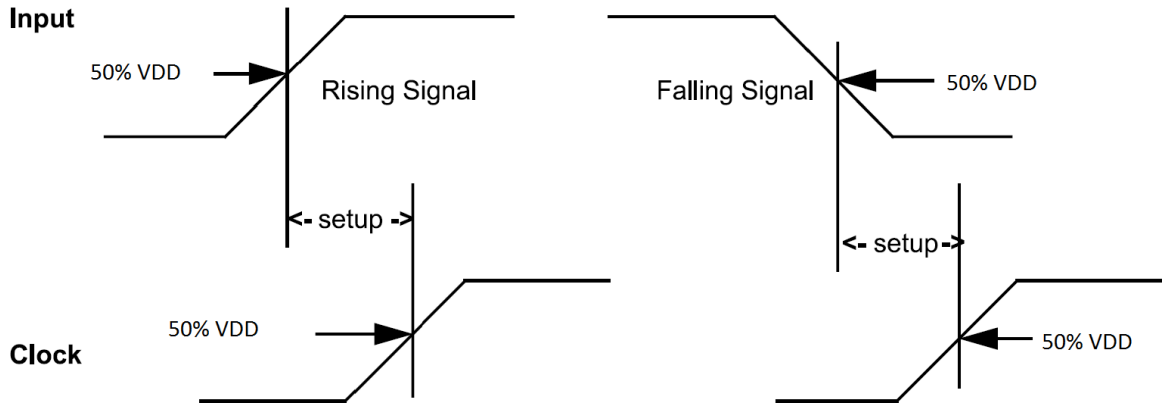


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

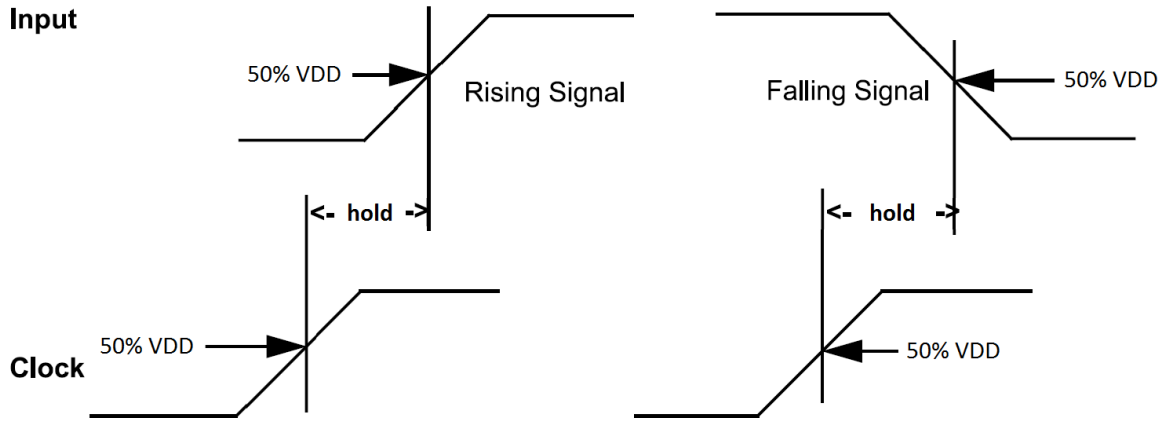


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

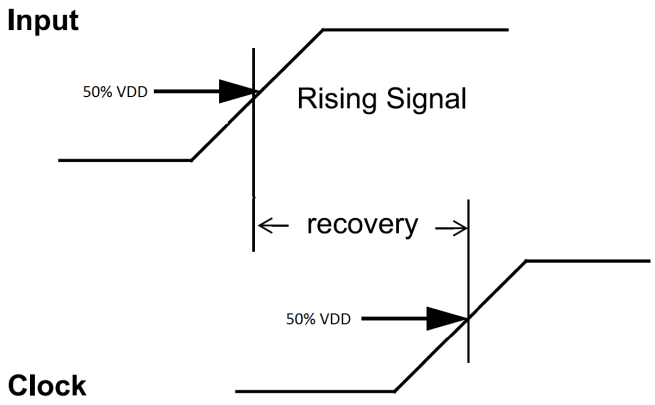


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

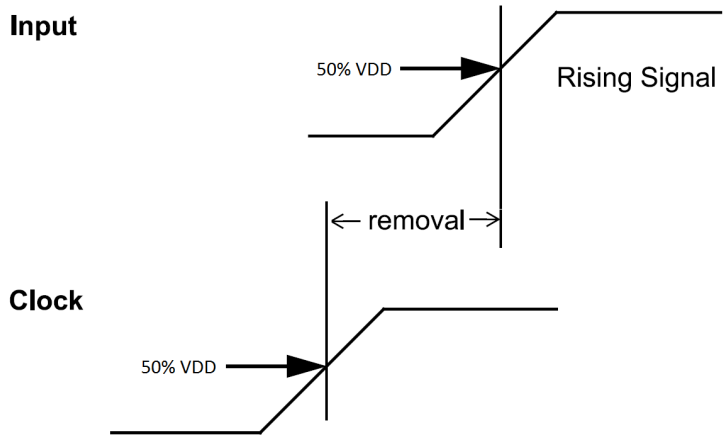


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

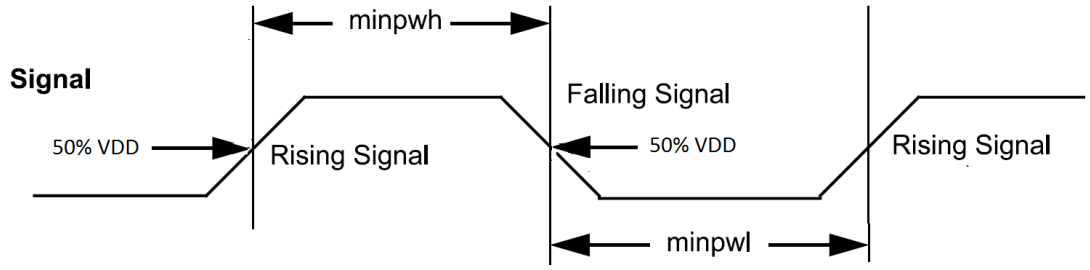


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

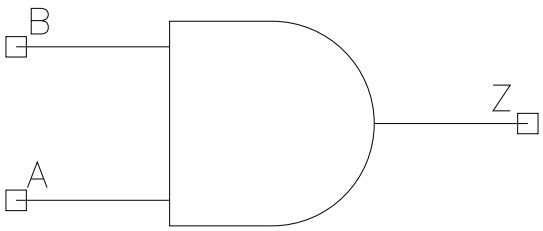
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

CNAND2

Cell Description

2 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.680	0.8160
X15_P4	1.200	0.680	0.8160
X15_P10	1.200	0.680	0.8160
X15_P16	1.200	0.680	0.8160
X20_P0	1.200	0.816	0.9792
X20_P4	1.200	0.816	0.9792
X20_P10	1.200	0.816	0.9792
X20_P16	1.200	0.816	0.9792
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0008	0.0008	0.0009	0.0009
B	0.0008	0.0008	0.0008	0.0009
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0008	0.0008	0.0009	0.0009
B	0.0008	0.0008	0.0008	0.0008
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0013	0.0014	0.0014	0.0015
B	0.0013	0.0014	0.0014	0.0015

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0339	0.0382	1.3624	1.4862
A to Z ↑	0.0280	0.0314	1.8766	2.0801
B to Z ↓	0.0325	0.0367	1.3630	1.4853
B to Z ↑	0.0287	0.0324	1.8780	2.0787
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0445	0.0511	1.6690	1.8373
A to Z ↑	0.0364	0.0417	2.4000	2.7310
B to Z ↓	0.0425	0.0489	1.6673	1.8336
B to Z ↑	0.0374	0.0429	2.3990	2.7330
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0383	0.0432	1.0120	1.1055
A to Z ↑	0.0320	0.0360	1.3906	1.5395
B to Z ↓	0.0370	0.0417	1.0121	1.1044
B to Z ↑	0.0330	0.0371	1.3919	1.5414
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0505	0.0580	1.2409	1.3662
A to Z ↑	0.0420	0.0481	1.7818	2.0297
B to Z ↓	0.0487	0.0560	1.2397	1.3651
B to Z ↑	0.0432	0.0495	1.7826	2.0272
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0372	0.0422	0.5751	0.6256
A to Z ↑	0.0278	0.0314	0.9492	1.0483
B to Z ↓	0.0344	0.0388	0.5730	0.6236
B to Z ↑	0.0277	0.0312	0.9481	1.0475
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0494	0.0567	0.6990	0.7666
A to Z ↑	0.0366	0.0417	1.2099	1.3733
B to Z ↓	0.0454	0.0519	0.6972	0.7647
B to Z ↑	0.0364	0.0414	1.2087	1.3722

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X15_P0	1.161e-05	9.409e-10
X15_P4	3.656e-06	9.409e-10
X15_P10	1.118e-06	9.409e-10
X15_P16	5.245e-07	9.409e-10
X20_P0	1.438e-05	1.060e-09
X20_P4	4.431e-06	1.060e-09
X20_P10	1.331e-06	1.060e-09
X20_P16	6.203e-07	1.060e-09
X33_P0	2.308e-05	1.536e-09
X33_P4	7.491e-06	1.536e-09
X33_P10	2.349e-06	1.536e-09
X33_P16	1.118e-06	1.536e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	2.083e-05	1.926e-05	1.771e-05	1.627e-05
B (output stable)	2.563e-05	3.064e-05	4.316e-05	4.561e-05
A to Z	2.722e-03	2.731e-03	2.786e-03	2.907e-03

B to Z	2.596e-03	2.591e-03	2.623e-03	2.739e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.095e-05	1.954e-05	1.787e-05	1.654e-05
B (output stable)	2.564e-05	3.106e-05	4.339e-05	4.705e-05
A to Z	3.659e-03	3.652e-03	3.730e-03	3.884e-03
B to Z	3.539e-03	3.508e-03	3.569e-03	3.716e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	8.454e-05	7.633e-05	6.595e-05	5.887e-05
B (output stable)	2.045e-04	2.575e-04	2.912e-04	2.991e-04
A to Z	5.568e-03	5.597e-03	5.724e-03	5.943e-03
B to Z	5.088e-03	5.068e-03	5.157e-03	5.345e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

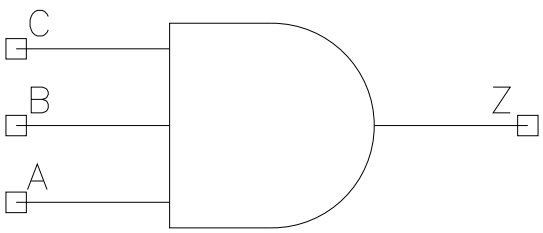
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	4.742e-08	4.196e-08	2.525e-08	4.220e-09
B (output stable)	4.457e-08	4.209e-08	7.200e-09	-1.130e-08
A to Z	-5.240e-08	-7.120e-08	-3.527e-07	-2.231e-07
B to Z	-2.658e-07	-1.146e-07	-1.415e-07	-2.185e-07
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	4.794e-08	4.689e-08	2.977e-08	1.606e-08
B (output stable)	4.493e-08	4.458e-08	8.600e-09	-8.900e-09
A to Z	-2.907e-07	-5.750e-08	-2.818e-07	-2.425e-07
B to Z	-3.032e-07	-2.685e-07	-3.660e-07	-4.564e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	4.610e-08	3.540e-08	1.550e-08	-2.190e-08
B (output stable)	2.510e-08	-8.800e-09	-4.830e-08	-9.290e-08
A to Z	-4.149e-07	-5.955e-07	-6.102e-07	-8.273e-07
B to Z	-2.467e-07	-4.774e-07	-2.794e-07	-4.067e-07

CNAND3

Cell Description

3 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X25_P0	1.200	1.360	1.6320
X25_P4	1.200	1.360	1.6320
X25_P10	1.200	1.360	1.6320
X25_P16	1.200	1.360	1.6320
X33_P0	1.200	1.768	2.1216
X33_P4	1.200	1.768	2.1216
X33_P10	1.200	1.768	2.1216
X33_P16	1.200	1.768	2.1216

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0008	0.0008	0.0008	0.0008
B	0.0008	0.0008	0.0008	0.0008
C	0.0008	0.0008	0.0008	0.0008
	X25_P0	X25_P4	X25_P10	X25_P16
A	0.0016	0.0016	0.0017	0.0018
B	0.0014	0.0015	0.0015	0.0016
C	0.0014	0.0014	0.0015	0.0016
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0018	0.0019	0.0020	0.0020
B	0.0017	0.0018	0.0018	0.0019

C	0.0016	0.0017	0.0018	0.0018

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0442	0.0496	1.1476	1.2516
A to Z ↑	0.0414	0.0466	1.3567	1.4998
B to Z ↓	0.0431	0.0482	1.1461	1.2507
B to Z ↑	0.0421	0.0469	1.3576	1.5001
C to Z ↓	0.0418	0.0467	1.1436	1.2474
C to Z ↑	0.0420	0.0470	1.3573	1.4998
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
A to Z ↓	0.0585	0.0670	1.4039	1.5474
A to Z ↑	0.0555	0.0639	1.7336	1.9723
B to Z ↓	0.0569	0.0651	1.4025	1.5447
B to Z ↑	0.0554	0.0634	1.7328	1.9737
C to Z ↓	0.0549	0.0627	1.4017	1.5422
C to Z ↑	0.0554	0.0633	1.7347	1.9727
	X25_P0	**X25_P4**	**X25_P0**	**X25_P4**
A to Z ↓	0.0334	0.0375	0.7722	0.8391
A to Z ↑	0.0325	0.0366	1.2808	1.4118
B to Z ↓	0.0321	0.0360	0.7718	0.8387
B to Z ↑	0.0331	0.0370	1.2816	1.4149
C to Z ↓	0.0305	0.0341	0.7707	0.8379
C to Z ↑	0.0330	0.0369	1.2825	1.4158
	X25_P10	**X25_P16**	**X25_P10**	**X25_P16**
A to Z ↓	0.0438	0.0499	0.9384	1.0290
A to Z ↑	0.0434	0.0498	1.6317	1.8528
B to Z ↓	0.0421	0.0479	0.9362	1.0282
B to Z ↑	0.0435	0.0496	1.6300	1.8519
C to Z ↓	0.0399	0.0453	0.9363	1.0267
C to Z ↑	0.0433	0.0495	1.6314	1.8536
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0353	0.0395	0.5676	0.6194
A to Z ↑	0.0358	0.0403	0.6615	0.7291
B to Z ↓	0.0342	0.0381	0.5676	0.6194
B to Z ↑	0.0366	0.0407	0.6617	0.7296
C to Z ↓	0.0330	0.0368	0.5670	0.6193
C to Z ↑	0.0367	0.0408	0.6610	0.7290
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0462	0.0526	0.6963	0.7676
A to Z ↑	0.0477	0.0546	0.8416	0.9557
B to Z ↓	0.0446	0.0506	0.6970	0.7657
B to Z ↑	0.0477	0.0545	0.8413	0.9563
C to Z ↓	0.0428	0.0486	0.6958	0.7661
C to Z ↑	0.0477	0.0544	0.8427	0.9564

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P0	1.344e-05	1.179e-09
X17_P4	3.839e-06	1.179e-09

X17_P10	1.096e-06	1.179e-09
X17_P16	5.052e-07	1.179e-09
X25_P0	1.670e-05	1.536e-09
X25_P4	5.117e-06	1.536e-09
X25_P10	1.557e-06	1.536e-09
X25_P16	7.434e-07	1.536e-09
X33_P0	2.780e-05	1.894e-09
X33_P4	8.063e-06	1.894e-09
X33_P10	2.323e-06	1.894e-09
X33_P16	1.076e-06	1.894e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	2.383e-05	2.154e-05	1.797e-05	1.519e-05
B (output stable)	2.937e-05	3.990e-05	4.846e-05	5.008e-05
C (output stable)	6.326e-05	7.971e-05	9.568e-05	9.512e-05
A to Z	4.073e-03	3.980e-03	4.095e-03	4.190e-03
B to Z	3.944e-03	3.838e-03	3.938e-03	4.020e-03
C to Z	3.821e-03	3.702e-03	3.784e-03	3.857e-03
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	4.412e-05	3.943e-05	3.282e-05	2.711e-05
B (output stable)	5.601e-05	7.698e-05	9.307e-05	9.673e-05
C (output stable)	1.260e-04	1.615e-04	1.913e-04	1.942e-04
A to Z	4.996e-03	5.001e-03	5.178e-03	5.372e-03
B to Z	4.722e-03	4.705e-03	4.855e-03	5.026e-03
C to Z	4.465e-03	4.410e-03	4.533e-03	4.684e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	5.421e-05	4.842e-05	3.989e-05	3.409e-05
B (output stable)	7.135e-05	9.697e-05	1.155e-04	1.192e-04
C (output stable)	1.625e-04	2.031e-04	2.386e-04	2.367e-04
A to Z	7.828e-03	7.750e-03	7.966e-03	8.221e-03
B to Z	7.512e-03	7.393e-03	7.578e-03	7.814e-03
C to Z	7.201e-03	7.044e-03	7.184e-03	7.395e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	6.619e-08	5.677e-08	3.488e-08	4.270e-08
B (output stable)	5.665e-08	4.665e-08	3.029e-08	2.195e-08
C (output stable)	5.093e-08	3.450e-08	2.103e-08	1.113e-08
A to Z	-3.524e-07	-9.540e-08	-1.528e-07	-1.834e-07
B to Z	-1.902e-07	-8.100e-08	-3.012e-07	-3.829e-07
C to Z	-4.050e-08	-2.464e-07	-5.820e-08	-4.485e-07
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	3.533e-08	4.800e-09	-2.563e-08	-7.267e-08
B (output stable)	2.627e-08	-8.333e-09	-3.307e-08	-5.660e-08
C (output stable)	2.883e-08	-4.200e-09	-3.337e-08	-7.940e-08
A to Z	-9.223e-07	-3.821e-07	-1.722e-07	-4.445e-07
B to Z	-6.445e-07	-4.210e-07	-6.444e-07	-5.699e-07
C to Z	-2.982e-07	-7.403e-07	-5.077e-07	-5.836e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	3.293e-08	-3.233e-09	-5.610e-08	-1.166e-07

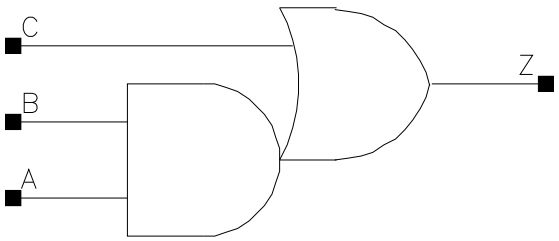
B (output stable)	1.260e-08	-2.973e-08	-7.283e-08	-1.067e-07
C (output stable)	1.602e-08	-3.052e-08	-8.167e-08	-1.456e-07
A to Z	-3.541e-07	-3.407e-07	-8.123e-07	-1.239e-06
B to Z	-2.839e-07	-1.148e-06	-6.287e-07	-9.777e-07
C to Z	-3.070e-07	-5.313e-07	-7.995e-07	-5.942e-07

CNAO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	1.632	1.9584
X33_P4	1.200	1.632	1.9584
X33_P10	1.200	1.632	1.9584
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0017	0.0017	0.0018	0.0018
B	0.0015	0.0015	0.0015	0.0016
C	0.0014	0.0014	0.0015	0.0016

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0396	0.0454	0.5795	0.6318
A to Z ↑	0.0336	0.0383	0.9500	1.0486
B to Z ↓	0.0376	0.0430	0.5793	0.6303
B to Z ↑	0.0344	0.0390	0.9493	1.0501
C to Z ↓	0.0410	0.0467	0.5774	0.6294
C to Z ↑	0.0344	0.0386	0.9457	1.0451
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0537	0.0615	0.7068	0.7765

A to Z ↑	0.0448	0.0510	1.2106	1.3740
B to Z ↓	0.0507	0.0577	0.7063	0.7755
B to Z ↑	0.0455	0.0514	1.2094	1.3757
C to Z ↓	0.0551	0.0630	0.7035	0.7732
C to Z ↑	0.0447	0.0502	1.2060	1.3694

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X33_P0	2.815e-05	1.775e-09
X33_P4	9.909e-06	1.775e-09
X33_P10	3.249e-06	1.775e-09
X33_P16	1.555e-06	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	9.163e-05	6.277e-05	3.381e-05	2.059e-05
B (output stable)	1.147e-04	9.864e-05	9.619e-05	9.433e-05
C (output stable)	2.060e-04	2.053e-04	2.079e-04	2.133e-04
A to Z	5.829e-03	5.846e-03	5.957e-03	6.098e-03
B to Z	5.547e-03	5.515e-03	5.587e-03	5.694e-03
C to Z	6.579e-03	6.624e-03	6.801e-03	6.994e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

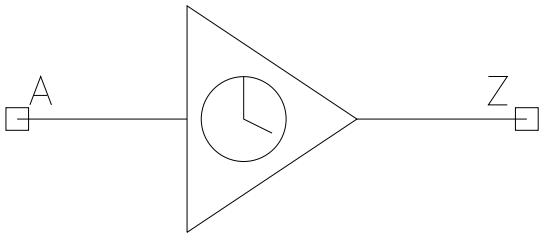
Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	2.925e-05	4.256e-05	2.026e-05	7.733e-06
B (output stable)	2.977e-05	4.253e-05	4.344e-05	3.944e-05
C (output stable)	-2.858e-07	-5.885e-06	-1.366e-05	-1.809e-05
A to Z	-5.564e-07	-5.845e-07	-8.310e-07	-1.072e-06
B to Z	-5.406e-07	-5.147e-07	-5.629e-07	-7.965e-07
C to Z	1.332e-06	5.353e-07	-5.754e-06	-1.215e-05

CNBF

Cell Description

Buffer with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X4_P4	1.200	0.408	0.4896
X4_P10	1.200	0.408	0.4896
X4_P16	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X15_P0	1.200	0.544	0.6528
X15_P4	1.200	0.544	0.6528
X15_P10	1.200	0.544	0.6528
X15_P16	1.200	0.544	0.6528
X22_P0	1.200	0.680	0.8160
X22_P4	1.200	0.680	0.8160
X22_P10	1.200	0.680	0.8160
X22_P16	1.200	0.680	0.8160
X30_P0	1.200	0.952	1.1424
X30_P4	1.200	0.952	1.1424
X30_P10	1.200	0.952	1.1424
X30_P16	1.200	0.952	1.1424
X38_P0	1.200	1.088	1.3056
X38_P4	1.200	1.088	1.3056
X38_P10	1.200	1.088	1.3056
X38_P16	1.200	1.088	1.3056
X44_P0	1.200	1.224	1.4688
X44_P4	1.200	1.224	1.4688
X44_P10	1.200	1.224	1.4688
X44_P16	1.200	1.224	1.4688
X52_P0	1.200	1.496	1.7952
X52_P4	1.200	1.496	1.7952
X52_P10	1.200	1.496	1.7952
X52_P16	1.200	1.496	1.7952
X59_P0	1.200	1.632	1.9584

X59_P4	1.200	1.632	1.9584
X59_P10	1.200	1.632	1.9584
X59_P16	1.200	1.632	1.9584
X70_P0	1.200	1.768	2.1216
X70_P4	1.200	1.768	2.1216
X70_P10	1.200	1.768	2.1216
X70_P16	1.200	1.768	2.1216
X94_P0	1.200	2.312	2.7744
X94_P4	1.200	2.312	2.7744
X94_P10	1.200	2.312	2.7744
X94_P16	1.200	2.312	2.7744
X133_P0	1.200	3.264	3.9168
X133_P4	1.200	3.264	3.9168
X133_P10	1.200	3.264	3.9168
X133_P16	1.200	3.264	3.9168

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X4_P4	X4_P10	X4_P16
A	0.0006	0.0006	0.0007	0.0007
	X7_P0	X7_P4	X7_P10	X7_P16
A	0.0006	0.0006	0.0007	0.0007
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0008	0.0008	0.0009	0.0009
	X22_P0	X22_P4	X22_P10	X22_P16
A	0.0009	0.0010	0.0010	0.0011
	X30_P0	X30_P4	X30_P10	X30_P16
A	0.0013	0.0014	0.0014	0.0015
	X38_P0	X38_P4	X38_P10	X38_P16
A	0.0016	0.0016	0.0017	0.0018
	X44_P0	X44_P4	X44_P10	X44_P16
A	0.0016	0.0017	0.0018	0.0019
	X52_P0	X52_P4	X52_P10	X52_P16
A	0.0021	0.0022	0.0024	0.0025
	X59_P0	X59_P4	X59_P10	X59_P16
A	0.0024	0.0025	0.0026	0.0028
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0025	0.0026	0.0027	0.0029
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0033	0.0034	0.0036	0.0038
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0049	0.0051	0.0054	0.0057

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X4_P4	X4_P0	X4_P4
A to Z ↓	0.0347	0.0392	4.9580	5.4312

A to Z ↑	0.0262	0.0294	6.9923	7.7978
	X4_P10	**X4_P16**	**X4_P10**	**X4_P16**
A to Z ↓	0.0458	0.0520	6.1193	6.7529
A to Z ↑	0.0341	0.0385	9.1014	10.4093
	X7_P0	**X7_P4**	**X7_P0**	**X7_P4**
A to Z ↓	0.0337	0.0382	2.6210	2.8562
A to Z ↑	0.0249	0.0281	4.0056	4.4332
	X7_P10	**X7_P16**	**X7_P10**	**X7_P16**
A to Z ↓	0.0447	0.0510	3.1958	3.5158
A to Z ↑	0.0325	0.0367	5.1241	5.8313
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0317	0.0359	1.3817	1.5053
A to Z ↑	0.0252	0.0284	1.8707	2.0684
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0416	0.0477	1.6894	1.8577
A to Z ↑	0.0326	0.0370	2.3911	2.7151
	X22_P0	**X22_P4**	**X22_P0**	**X22_P4**
A to Z ↓	0.0322	0.0366	0.9461	1.0323
A to Z ↑	0.0262	0.0296	1.2575	1.3890
	X22_P10	**X22_P16**	**X22_P10**	**X22_P16**
A to Z ↓	0.0422	0.0482	1.1582	1.2742
A to Z ↑	0.0338	0.0382	1.6044	1.8230
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**
A to Z ↓	0.0303	0.0342	0.6621	0.7230
A to Z ↑	0.0237	0.0266	0.9405	1.0388
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
A to Z ↓	0.0398	0.0455	0.8107	0.8925
A to Z ↑	0.0306	0.0346	1.1995	1.3646
	X38_P0	**X38_P4**	**X38_P0**	**X38_P4**
A to Z ↓	0.0301	0.0340	0.5336	0.5824
A to Z ↑	0.0238	0.0267	0.7545	0.8330
	X38_P10	**X38_P16**	**X38_P10**	**X38_P16**
A to Z ↓	0.0398	0.0454	0.6537	0.7196
A to Z ↑	0.0310	0.0350	0.9611	1.0931
	X44_P0	**X44_P4**	**X44_P0**	**X44_P4**
A to Z ↓	0.0307	0.0345	0.4617	0.5038
A to Z ↑	0.0242	0.0271	0.6637	0.7338
	X44_P10	**X44_P16**	**X44_P10**	**X44_P16**
A to Z ↓	0.0405	0.0462	0.5656	0.6227
A to Z ↑	0.0315	0.0356	0.8478	0.9636
	X52_P0	**X52_P4**	**X52_P0**	**X52_P4**
A to Z ↓	0.0301	0.0341	0.3980	0.4343
A to Z ↑	0.0255	0.0286	0.5542	0.6110
	X52_P10	**X52_P16**	**X52_P10**	**X52_P16**
A to Z ↓	0.0397	0.0452	0.4872	0.5358
A to Z ↑	0.0331	0.0374	0.7062	0.8022
	X59_P0	**X59_P4**	**X59_P0**	**X59_P4**
A to Z ↓	0.0301	0.0338	0.3483	0.3805
A to Z ↑	0.0241	0.0269	0.4908	0.5422
	X59_P10	**X59_P16**	**X59_P10**	**X59_P16**
A to Z ↓	0.0395	0.0449	0.4273	0.4697
A to Z ↑	0.0311	0.0350	0.6264	0.7106

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0316	0.0356	0.2913	0.3173
A to Z ↑	0.0249	0.0279	0.4234	0.4680
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0415	0.0473	0.3558	0.3912
A to Z ↑	0.0323	0.0363	0.5410	0.6144
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0310	0.0349	0.2221	0.2419
A to Z ↑	0.0246	0.0275	0.3221	0.3556
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0407	0.0462	0.2714	0.2980
A to Z ↑	0.0318	0.0357	0.4100	0.4648
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0311	0.0348	0.1634	0.1786
A to Z ↑	0.0249	0.0278	0.2326	0.2569
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0406	0.0460	0.2001	0.2196
A to Z ↑	0.0322	0.0362	0.2963	0.3358

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X4_P0	4.374e-06	7.027e-10
X4_P4	1.544e-06	7.027e-10
X4_P10	5.008e-07	7.027e-10
X4_P16	2.360e-07	7.027e-10
X7_P0	6.860e-06	7.027e-10
X7_P4	2.399e-06	7.027e-10
X7_P10	7.785e-07	7.027e-10
X7_P16	3.688e-07	7.027e-10
X15_P0	1.219e-05	8.218e-10
X15_P4	4.112e-06	8.218e-10
X15_P10	1.304e-06	8.218e-10
X15_P16	6.122e-07	8.218e-10
X22_P0	1.714e-05	9.409e-10
X22_P4	5.697e-06	9.409e-10
X22_P10	1.786e-06	9.409e-10
X22_P16	8.343e-07	9.409e-10
X30_P0	2.307e-05	1.179e-09
X30_P4	7.764e-06	1.179e-09
X30_P10	2.450e-06	1.179e-09
X30_P16	1.147e-06	1.179e-09
X38_P0	2.855e-05	1.298e-09
X38_P4	9.559e-06	1.298e-09
X38_P10	3.005e-06	1.298e-09
X38_P16	1.405e-06	1.298e-09
X44_P0	3.245e-05	1.417e-09
X44_P4	1.078e-05	1.417e-09
X44_P10	3.373e-06	1.417e-09
X44_P16	1.574e-06	1.417e-09
X52_P0	3.783e-05	1.655e-09
X52_P4	1.260e-05	1.655e-09
X52_P10	3.939e-06	1.655e-09

X52_P16	1.836e-06	1.655e-09
X59_P0	4.413e-05	1.775e-09
X59_P4	1.462e-05	1.775e-09
X59_P10	4.563e-06	1.775e-09
X59_P16	2.126e-06	1.775e-09
X70_P0	5.023e-05	1.894e-09
X70_P4	1.685e-05	1.894e-09
X70_P10	5.301e-06	1.894e-09
X70_P16	2.479e-06	1.894e-09
X94_P0	6.632e-05	2.370e-09
X94_P4	2.222e-05	2.370e-09
X94_P10	6.978e-06	2.370e-09
X94_P16	3.261e-06	2.370e-09
X133_P0	9.396e-05	3.204e-09
X133_P4	3.153e-05	3.204e-09
X133_P10	9.905e-06	3.204e-09
X133_P16	4.628e-06	3.204e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	1.169e-03	1.177e-03	1.211e-03	1.250e-03
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	1.501e-03	1.509e-03	1.555e-03	1.611e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	2.509e-03	2.496e-03	2.556e-03	2.672e-03
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	3.682e-03	3.731e-03	3.768e-03	3.934e-03
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	4.676e-03	4.658e-03	4.768e-03	4.976e-03
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	5.914e-03	5.905e-03	6.116e-03	6.381e-03
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	6.560e-03	6.526e-03	6.742e-03	7.029e-03
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	8.144e-03	8.174e-03	8.393e-03	8.726e-03
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	9.138e-03	9.090e-03	9.376e-03	9.734e-03
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	1.068e-02	1.068e-02	1.098e-02	1.142e-02
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	1.375e-02	1.377e-02	1.414e-02	1.464e-02
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	2.024e-02	2.008e-02	2.063e-02	2.130e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	-1.069e-07	1.000e-09	-8.950e-08	-1.017e-07
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	-8.850e-08	-8.360e-08	-1.725e-07	-1.462e-07
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	-8.770e-08	-1.372e-07	-1.611e-07	-1.820e-07

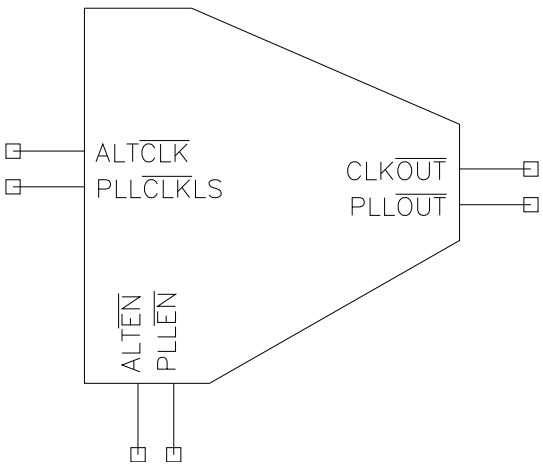
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	-2.300e-07	-3.708e-07	-3.706e-07	-6.361e-07
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	-2.369e-07	-5.282e-07	-8.065e-07	-6.009e-07
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	-4.910e-07	-1.059e-06	-1.236e-06	-1.076e-06
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	-2.221e-07	-4.728e-07	-7.729e-07	-9.536e-07
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	-5.130e-07	-1.024e-06	-1.693e-06	-1.450e-06
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	-6.649e-07	-1.459e-06	-1.811e-06	-1.327e-06
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	-1.081e-06	-1.749e-06	-1.150e-06	-1.225e-06
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	-6.920e-07	-1.752e-06	-1.832e-06	-2.118e-06
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	-1.077e-06	-2.041e-06	-2.285e-06	-1.154e-06

CNGFMUX21

Cell Description

2:1 Glitch-free MUX for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	2.400	2.856	6.8544
X15_P4	2.400	2.856	6.8544
X15_P10	2.400	2.856	6.8544
X15_P16	2.400	2.856	6.8544
X30_P0	2.400	3.944	9.4656
X30_P4	2.400	3.944	9.4656
X30_P10	2.400	3.944	9.4656
X30_P16	2.400	3.944	9.4656

Truth Table

PLL_CLK_LS	ALT_CLK	IPLL_EN_LD	IALT_EN_LD	CLK_OUT
0	-	-	0	0
0	0	-	-	0
-	0	0	-	0
PLL_CLK_LS	1	-	1	1
1	ALT_CLK	1	-	1
1	1	0	0	0

PLL_CLK_LS	PLL_OUT
PLL_CLK_LS	PLL_CLK_LS
1	1

PLL_EN	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

PLL_EN	0	-	PLL_EN
-	-	IPLL_EN_LD	IPLL_EN_LD
-	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

ALT_EN	ALT_CLK	IALT_EN_LD	IALT_EN_LD
ALT_EN	0	-	ALT_EN
-	-	IALT_EN_LD	IALT_EN_LD
-	ALT_CLK	IALT_EN_LD	IALT_EN_LD

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK	0.0022	0.0023	0.0025	0.0025
ALT_EN	0.0005	0.0005	0.0005	0.0006
PLL_CLK_LS	0.0029	0.0030	0.0031	0.0033
PLL_EN	0.0005	0.0005	0.0005	0.0005
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK	0.0035	0.0036	0.0038	0.0039
ALT_EN	0.0005	0.0005	0.0005	0.0006
PLL_CLK_LS	0.0048	0.0049	0.0052	0.0054
PLL_EN	0.0005	0.0005	0.0005	0.0005

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
ALT_CLK to CLK_OUT ↓	0.0421	0.0471	1.4983	1.6331
ALT_CLK to CLK_OUT ↑	0.0315	0.0354	2.1997	2.4357
PLL_CLK_LS to CLK_OUT ↓	0.0377	0.0422	1.5041	1.6404
PLL_CLK_LS to CLK_OUT ↑	0.0294	0.0331	2.1996	2.4401
PLL_CLK_LS to PLL_OUT ↓	0.0323	0.0364	1.3082	1.4264
PLL_CLK_LS to PLL_OUT ↑	0.0257	0.0288	1.8748	2.0725
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
ALT_CLK to CLK_OUT ↓	0.0551	0.0629	1.8373	2.0282
ALT_CLK to CLK_OUT ↑	0.0420	0.0482	2.8197	3.2121
PLL_CLK_LS to CLK_OUT ↓	0.0491	0.0558	1.8444	2.0339
PLL_CLK_LS to CLK_OUT ↑	0.0386	0.0439	2.8257	3.2170
PLL_CLK_LS to PLL_OUT ↓	0.0426	0.0486	1.5989	1.7577
PLL_CLK_LS to PLL_OUT ↑	0.0333	0.0375	2.3936	2.7203
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**

ALT_CLK to CLK_OUT ↓	0.0409	0.0458	0.7744	0.8437
ALT_CLK to CLK_OUT ↑	0.0319	0.0359	0.9803	1.0837
PLL_CLK_LS to CLK_OUT ↓	0.0370	0.0413	0.7805	0.8498
PLL_CLK_LS to CLK_OUT ↑	0.0300	0.0335	0.9855	1.0900
PLL_CLK_LS to PLL_OUT ↓	0.0277	0.0314	0.6704	0.7303
PLL_CLK_LS to PLL_OUT ↑	0.0222	0.0250	0.9405	1.0386
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
ALT_CLK to CLK_OUT ↓	0.0533	0.0602	0.9471	1.0436
ALT_CLK to CLK_OUT ↑	0.0423	0.0482	1.2521	1.4220
PLL_CLK_LS to CLK_OUT ↓	0.0478	0.0539	0.9538	1.0501
PLL_CLK_LS to CLK_OUT ↑	0.0389	0.0440	1.2582	1.4301
PLL_CLK_LS to PLL_OUT ↓	0.0363	0.0415	0.8170	0.8978
PLL_CLK_LS to PLL_OUT ↑	0.0286	0.0325	1.1989	1.3636

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0722	0.0779	0.0933	0.1076
ALT_EN ↓	hold_rising to ALT_CLK	-0.0339	-0.0440	-0.0535	-0.0658
ALT_EN ↑	hold_rising to ALT_CLK	-0.0086	-0.0139	-0.0188	-0.0293
ALT_EN ↓	setup_rising to ALT_CLK	0.0690	0.0787	0.0955	0.1101
ALT_EN ↑	setup_rising to ALT_CLK	0.0414	0.0491	0.0588	0.0686
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0722	0.0790	0.0933	0.1076
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0366	-0.0459	-0.0609	-0.0755
PLL_EN ↑	hold_rising to PLL_CLK_LS	-0.0090	-0.0139	-0.0188	-0.0293
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0690	0.0787	0.0955	0.1101
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0413	0.0487	0.0588	0.0685
		X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0684	0.0779	0.0933	0.1076
ALT_EN ↓	hold_rising to ALT_CLK	-0.0343	-0.0385	-0.0507	-0.0602

ALT_EN ↑	hold_rising to ALT_CLK	-0.0086	-0.0139	-0.0213	-0.0293
ALT_EN ↓	setup_rising to ALT_CLK	0.0690	0.0787	0.0955	0.1101
ALT_EN ↑	setup_rising to ALT_CLK	0.0462	0.0536	0.0686	0.0783
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0684	0.0779	0.0933	0.1076
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0388	-0.0489	-0.0633	-0.0804
PLL_EN ↑	hold_rising to PLL_CLK_LS	-0.0086	-0.0139	-0.0213	-0.0293
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0690	0.0787	0.0955	0.1101
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0487	0.0536	0.0686	0.0804

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X15_P0	6.237e-05	3.796e-09
X15_P4	2.190e-05	3.796e-09
X15_P10	7.205e-06	3.796e-09
X15_P16	3.470e-06	3.796e-09
X30_P0	1.004e-04	4.979e-09
X30_P4	3.460e-05	4.979e-09
X30_P10	1.126e-05	4.979e-09
X30_P16	5.413e-06	4.979e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	2.659e-03	2.692e-03	2.783e-03	2.882e-03
ALT_EN (output stable)	1.769e-03	1.788e-03	1.844e-03	1.909e-03
PLL_CLK_LS (output stable)	6.064e-03	5.438e-03	5.360e-03	5.492e-03
PLL_EN (output stable)	1.793e-03	1.796e-03	1.847e-03	1.913e-03
ALT_CLK to CLK_OUT	5.442e-03	5.521e-03	5.744e-03	5.991e-03
PLL_CLK_LS to CLK_OUT	4.576e-03	4.581e-03	4.706e-03	4.873e-03
PLL_CLK_LS to PLL_OUT	6.730e-03	5.720e-03	5.491e-03	5.576e-03
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	3.356e-03	3.410e-03	3.533e-03	3.671e-03
ALT_EN (output stable)	1.971e-03	2.014e-03	2.097e-03	2.175e-03
PLL_CLK_LS (output stable)	8.379e-03	7.970e-03	8.009e-03	8.330e-03

PLL_EN (output stable)	2.084e-03	2.108e-03	2.201e-03	2.280e-03
ALT_CLK to CLK_OUT	9.835e-03	1.001e-02	1.045e-02	1.077e-02
PLL_CLK_LS to CLK_OUT	6.058e-03	6.073e-03	6.227e-03	6.450e-03
PLL_CLK_LS to PLL_OUT	8.001e-03	7.182e-03	7.024e-03	7.188e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

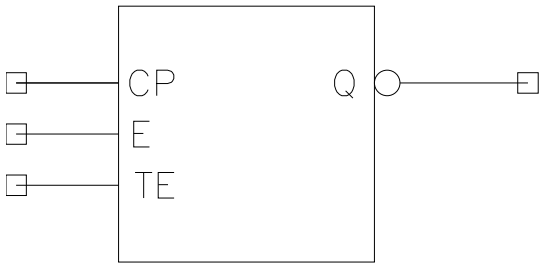
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	-7.736e-06	-6.504e-06	-6.303e-06	-5.988e-06
ALT_EN (output stable)	6.694e-08	-2.193e-07	-1.793e-06	-3.614e-06
PLL_CLK_LS (output stable)	-7.526e-07	-5.100e-07	-1.555e-06	-2.722e-06
PLL_EN (output stable)	8.991e-08	-2.321e-07	-1.721e-06	-3.331e-06
ALT_CLK to CLK_OUT	2.429e-05	2.407e-05	2.651e-05	1.597e-05
PLL_CLK_LS to CLK_OUT	2.590e-05	2.326e-05	1.830e-05	1.103e-05
PLL_CLK_LS to PLL_OUT	-1.811e-06	-8.609e-07	-1.637e-06	-2.666e-06
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	-2.358e-05	-1.950e-05	-1.739e-05	-1.954e-05
ALT_EN (output stable)	6.143e-08	-2.371e-07	-1.563e-06	-3.664e-06
PLL_CLK_LS (output stable)	1.590e-05	1.289e-05	1.342e-05	1.103e-05
PLL_EN (output stable)	7.788e-08	-2.397e-07	-1.707e-06	-3.312e-06
ALT_CLK to CLK_OUT	8.575e-05	9.296e-05	8.375e-05	7.826e-05
PLL_CLK_LS to CLK_OUT	5.537e-05	5.313e-05	4.642e-05	4.513e-05
PLL_CLK_LS to PLL_OUT	2.391e-05	2.626e-05	2.127e-05	1.707e-05

CNHLS

Cell Description

Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LRP_-CNHLSX7_P0	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX7_P4	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX7_P10	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX7_P16	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX15_P0	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX15_P4	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX15_P10	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX15_P16	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX22_P0	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX22_P4	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX22_P10	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX22_P16	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX29_P0	1.200	2.448	2.9376
C12T28SOI_LRP_-CNHLSX29_P4	1.200	2.448	2.9376
C12T28SOI_LRP_-CNHLSX29_P10	1.200	2.448	2.9376
C12T28SOI_LRP_-CNHLSX29_P16	1.200	2.448	2.9376

C12T28SOI_LRP_-CNHLSX36_P0	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX36_P4	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX36_P10	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX36_P16	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX51_P0	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX51_P4	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX51_P10	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX51_P16	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX58_P0	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX58_P4	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX58_P10	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX58_P16	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX71_P0	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX71_P4	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX71_P10	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX71_P16	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX93_P0	1.200	4.896	5.8752
C12T28SOI_LRP_-CNHLSX93_P4	1.200	4.896	5.8752
C12T28SOI_LRP_-CNHLSX93_P10	1.200	4.896	5.8752
C12T28SOI_LRP_-CNHLSX93_P16	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX29_P0	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX29_P4	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX29_P10	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX29_P16	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX36_P0	1.200	3.128	3.7536
C12T28SOI_LRPHP_-CNHLSX36_P4	1.200	3.128	3.7536

C12T28SOI_LRPHP_-CNHLSX36_P10	1.200	3.128	3.7536
C12T28SOI_LRPHP_-CNHLSX36_P16	1.200	3.128	3.7536
C12T28SOI_LRPHP_-CNHLSX44_P0	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX44_P4	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX44_P10	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX44_P16	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX51_P0	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX51_P4	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX51_P10	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX51_P16	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX58_P0	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX58_P4	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX58_P10	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX58_P16	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX71_P0	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX71_P4	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX71_P10	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX71_P16	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX86_P0	1.200	5.304	6.3648
C12T28SOI_LRPHP_-CNHLSX86_P4	1.200	5.304	6.3648
C12T28SOI_LRPHP_-CNHLSX86_P10	1.200	5.304	6.3648
C12T28SOI_LRPHP_-CNHLSX86_P16	1.200	5.304	6.3648

Truth Table

CP	E	TE	OLDIE	Q
0	-	-	-	0
1	-	-	OLDIE	OLDIE

OLDIE	OLDIE
OLDIE	OLDIE

Pin Capacitance

Pin	C12T28SOI_LRP_-CNHLSX7_P0	C12T28SOI_LRP_-CNHLSX7_P4	C12T28SOI_LRP_-CNHLSX7_P10	C12T28SOI_LRP_-CNHLSX7_P16
CP	0.0019	0.0019	0.0020	0.0021
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LRP_-CNHLSX15_P0	C12T28SOI_LRP_-CNHLSX15_P4	C12T28SOI_LRP_-CNHLSX15_P10	C12T28SOI_LRP_-CNHLSX15_P16
CP	0.0025	0.0025	0.0026	0.0028
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LRP_-CNHLSX22_P0	C12T28SOI_LRP_-CNHLSX22_P4	C12T28SOI_LRP_-CNHLSX22_P10	C12T28SOI_LRP_-CNHLSX22_P16
CP	0.0026	0.0027	0.0028	0.0030
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LRP_-CNHLSX29_P0	C12T28SOI_LRP_-CNHLSX29_P4	C12T28SOI_LRP_-CNHLSX29_P10	C12T28SOI_LRP_-CNHLSX29_P16
CP	0.0028	0.0029	0.0031	0.0032
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LRP_-CNHLSX36_P0	C12T28SOI_LRP_-CNHLSX36_P4	C12T28SOI_LRP_-CNHLSX36_P10	C12T28SOI_LRP_-CNHLSX36_P16
CP	0.0030	0.0032	0.0034	0.0035
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LRP_-CNHLSX51_P0	C12T28SOI_LRP_-CNHLSX51_P4	C12T28SOI_LRP_-CNHLSX51_P10	C12T28SOI_LRP_-CNHLSX51_P16
CP	0.0036	0.0037	0.0039	0.0041
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LRP_-CNHLSX58_P0	C12T28SOI_LRP_-CNHLSX58_P4	C12T28SOI_LRP_-CNHLSX58_P10	C12T28SOI_LRP_-CNHLSX58_P16
CP	0.0049	0.0051	0.0054	0.0057
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LRP_-CNHLSX71_P0	C12T28SOI_LRP_-CNHLSX71_P4	C12T28SOI_LRP_-CNHLSX71_P10	C12T28SOI_LRP_-CNHLSX71_P16
CP	0.0056	0.0059	0.0062	0.0065
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LRP_-CNHLSX93_P0	C12T28SOI_LRP_-CNHLSX93_P4	C12T28SOI_LRP_-CNHLSX93_P10	C12T28SOI_LRP_-CNHLSX93_P16
CP	0.0066	0.0069	0.0073	0.0077
E	0.0005	0.0005	0.0005	0.0006
TE	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP	0.0022	0.0023	0.0024	0.0025
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0008	0.0009	0.0009

	C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP	0.0024	0.0026	0.0027	0.0028
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0008	0.0009	0.0009
	C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP	0.0029	0.0030	0.0031	0.0033
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0008	0.0009	0.0009
	C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP	0.0029	0.0030	0.0032	0.0032
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0008	0.0009	0.0009
	C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP	0.0039	0.0041	0.0044	0.0045
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0008	0.0009	0.0009
	C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP	0.0048	0.0050	0.0053	0.0056
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0008	0.0009	0.0009
	C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP	0.0059	0.0060	0.0064	0.0067
E	0.0005	0.0006	0.0006	0.0006
TE	0.0008	0.0008	0.0009	0.0009

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LRP_-CNHLSX7_P0	**C12T28SOI_LRP_-CNHLSX7_P4**	**C12T28SOI_LRP_-CNHLSX7_P0**	**C12T28SOI_LRP_-CNHLSX7_P4**
CP to Q ↓	0.0392	0.0446	2.7568	3.0087
CP to Q ↑	0.0294	0.0332	3.7522	4.1530
	C12T28SOI_LRP_-CNHLSX7_P10	**C12T28SOI_LRP_-CNHLSX7_P16**	**C12T28SOI_LRP_-CNHLSX7_P10**	**C12T28SOI_LRP_-CNHLSX7_P16**
CP to Q ↓	0.0528	0.0606	3.3781	3.7161
CP to Q ↑	0.0389	0.0442	4.8048	5.4618
	C12T28SOI_LRP_-CNHLSX15_P0	**C12T28SOI_LRP_-CNHLSX15_P4**	**C12T28SOI_LRP_-CNHLSX15_P0**	**C12T28SOI_LRP_-CNHLSX15_P4**
CP to Q ↓	0.0329	0.0368	1.3873	1.5144
CP to Q ↑	0.0267	0.0298	1.8872	2.0860
	C12T28SOI_LRP_-CNHLSX15_P10	**C12T28SOI_LRP_-CNHLSX15_P16**	**C12T28SOI_LRP_-CNHLSX15_P10**	**C12T28SOI_LRP_-CNHLSX15_P16**

CP to Q ↓	0.0430	0.0487	1.6992	1.8684
CP to Q ↑	0.0349	0.0394	2.4097	2.7389
	C12T28SOI_LRP_-CNHLSX22_P0	**C12T28SOI_LRP_-CNHLSX22_P4**	**C12T28SOI_LRP_-CNHLSX22_P0**	**C12T28SOI_LRP_-CNHLSX22_P4**
CP to Q ↓	0.0333	0.0370	0.9603	1.0483
CP to Q ↑	0.0289	0.0322	1.2697	1.4042
	C12T28SOI_LRP_-CNHLSX22_P10	**C12T28SOI_LRP_-CNHLSX22_P16**	**C12T28SOI_LRP_-CNHLSX22_P10**	**C12T28SOI_LRP_-CNHLSX22_P16**
CP to Q ↓	0.0434	0.0492	1.1763	1.2941
CP to Q ↑	0.0380	0.0430	1.6238	1.8448
	C12T28SOI_LRP_-CNHLSX29_P0	**C12T28SOI_LRP_-CNHLSX29_P4**	**C12T28SOI_LRP_-CNHLSX29_P0**	**C12T28SOI_LRP_-CNHLSX29_P4**
CP to Q ↓	0.0329	0.0370	0.7210	0.7869
CP to Q ↑	0.0282	0.0317	0.9531	1.0538
	C12T28SOI_LRP_-CNHLSX29_P10	**C12T28SOI_LRP_-CNHLSX29_P16**	**C12T28SOI_LRP_-CNHLSX29_P10**	**C12T28SOI_LRP_-CNHLSX29_P16**
CP to Q ↓	0.0432	0.0494	0.8839	0.9719
CP to Q ↑	0.0368	0.0420	1.2174	1.3834
	C12T28SOI_LRP_-CNHLSX36_P0	**C12T28SOI_LRP_-CNHLSX36_P4**	**C12T28SOI_LRP_-CNHLSX36_P0**	**C12T28SOI_LRP_-CNHLSX36_P4**
CP to Q ↓	0.0325	0.0367	0.5765	0.6294
CP to Q ↑	0.0277	0.0311	0.7640	0.8429
	C12T28SOI_LRP_-CNHLSX36_P10	**C12T28SOI_LRP_-CNHLSX36_P16**	**C12T28SOI_LRP_-CNHLSX36_P10**	**C12T28SOI_LRP_-CNHLSX36_P16**
CP to Q ↓	0.0429	0.0491	0.7060	0.7762
CP to Q ↑	0.0362	0.0413	0.9745	1.1076
	C12T28SOI_LRP_-CNHLSX51_P0	**C12T28SOI_LRP_-CNHLSX51_P4**	**C12T28SOI_LRP_-CNHLSX51_P0**	**C12T28SOI_LRP_-CNHLSX51_P4**
CP to Q ↓	0.0351	0.0396	0.4216	0.4595
CP to Q ↑	0.0282	0.0320	0.5484	0.6066
	C12T28SOI_LRP_-CNHLSX51_P10	**C12T28SOI_LRP_-CNHLSX51_P16**	**C12T28SOI_LRP_-CNHLSX51_P10**	**C12T28SOI_LRP_-CNHLSX51_P16**
CP to Q ↓	0.0461	0.0525	0.5162	0.5668
CP to Q ↑	0.0371	0.0422	0.6998	0.7953
	C12T28SOI_LRP_-CNHLSX58_P0	**C12T28SOI_LRP_-CNHLSX58_P4**	**C12T28SOI_LRP_-CNHLSX58_P0**	**C12T28SOI_LRP_-CNHLSX58_P4**
CP to Q ↓	0.0313	0.0350	0.3690	0.4023
CP to Q ↑	0.0247	0.0276	0.4820	0.5324
	C12T28SOI_LRP_-CNHLSX58_P10	**C12T28SOI_LRP_-CNHLSX58_P16**	**C12T28SOI_LRP_-CNHLSX58_P10**	**C12T28SOI_LRP_-CNHLSX58_P16**
CP to Q ↓	0.0406	0.0463	0.4504	0.4951
CP to Q ↑	0.0320	0.0365	0.6144	0.6974
	C12T28SOI_LRP_-CNHLSX71_P0	**C12T28SOI_LRP_-CNHLSX71_P4**	**C12T28SOI_LRP_-CNHLSX71_P0**	**C12T28SOI_LRP_-CNHLSX71_P4**
CP to Q ↓	0.0305	0.0344	0.3061	0.3334
CP to Q ↑	0.0249	0.0282	0.3917	0.4330
	C12T28SOI_LRP_-CNHLSX71_P10	**C12T28SOI_LRP_-CNHLSX71_P16**	**C12T28SOI_LRP_-CNHLSX71_P10**	**C12T28SOI_LRP_-CNHLSX71_P16**
CP to Q ↓	0.0399	0.0452	0.3738	0.4107
CP to Q ↑	0.0327	0.0369	0.4993	0.5675
	C12T28SOI_LRP_-CNHLSX93_P0	**C12T28SOI_LRP_-CNHLSX93_P4**	**C12T28SOI_LRP_-CNHLSX93_P0**	**C12T28SOI_LRP_-CNHLSX93_P4**
CP to Q ↓	0.0317	0.0357	0.2417	0.2633

CP to Q ↑	0.0264	0.0297	0.3087	0.3402
	C12T28SOI_LRP_-CNHLSX93_P10	**C12T28SOI_LRP_-CNHLSX93_P16**	**C12T28SOI_LRP_-CNHLSX93_P10**	**C12T28SOI_LRP_-CNHLSX93_P16**
CP to Q ↓	0.0413	0.0471	0.2944	0.3236
CP to Q ↑	0.0344	0.0392	0.3924	0.4455
	C12T28SOI_-LRPHP_-CNHLSX29_P0	**C12T28SOI_-LRPHP_-CNHLSX29_P4**	**C12T28SOI_-LRPHP_-CNHLSX29_P0**	**C12T28SOI_-LRPHP_-CNHLSX29_P4**
CP to Q ↓	0.0313	0.0355	0.7300	0.7960
CP to Q ↑	0.0265	0.0300	0.9611	1.0594
	C12T28SOI_-LRPHP_-CNHLSX29_P10	**C12T28SOI_-LRPHP_-CNHLSX29_P16**	**C12T28SOI_-LRPHP_-CNHLSX29_P10**	**C12T28SOI_-LRPHP_-CNHLSX29_P16**
CP to Q ↓	0.0411	0.0468	0.8917	0.9816
CP to Q ↑	0.0347	0.0394	1.2220	1.3889
	C12T28SOI_-LRPHP_-CNHLSX36_P0	**C12T28SOI_-LRPHP_-CNHLSX36_P4**	**C12T28SOI_-LRPHP_-CNHLSX36_P0**	**C12T28SOI_-LRPHP_-CNHLSX36_P4**
CP to Q ↓	0.0308	0.0351	0.5828	0.6352
CP to Q ↑	0.0261	0.0296	0.7735	0.8526
	C12T28SOI_-LRPHP_-CNHLSX36_P10	**C12T28SOI_-LRPHP_-CNHLSX36_P16**	**C12T28SOI_-LRPHP_-CNHLSX36_P10**	**C12T28SOI_-LRPHP_-CNHLSX36_P16**
CP to Q ↓	0.0410	0.0467	0.7123	0.7830
CP to Q ↑	0.0344	0.0389	0.9827	1.1166
	C12T28SOI_-LRPHP_-CNHLSX44_P0	**C12T28SOI_-LRPHP_-CNHLSX44_P4**	**C12T28SOI_-LRPHP_-CNHLSX44_P0**	**C12T28SOI_-LRPHP_-CNHLSX44_P4**
CP to Q ↓	0.0314	0.0349	0.4892	0.5324
CP to Q ↑	0.0254	0.0282	0.6459	0.7118
	C12T28SOI_-LRPHP_-CNHLSX44_P10	**C12T28SOI_-LRPHP_-CNHLSX44_P16**	**C12T28SOI_-LRPHP_-CNHLSX44_P10**	**C12T28SOI_-LRPHP_-CNHLSX44_P16**
CP to Q ↓	0.0403	0.0457	0.5968	0.6558
CP to Q ↑	0.0325	0.0367	0.8203	0.9310
	C12T28SOI_-LRPHP_-CNHLSX51_P0	**C12T28SOI_-LRPHP_-CNHLSX51_P4**	**C12T28SOI_-LRPHP_-CNHLSX51_P0**	**C12T28SOI_-LRPHP_-CNHLSX51_P4**
CP to Q ↓	0.0332	0.0371	0.4234	0.4610
CP to Q ↑	0.0269	0.0300	0.5566	0.6130
	C12T28SOI_-LRPHP_-CNHLSX51_P10	**C12T28SOI_-LRPHP_-CNHLSX51_P16**	**C12T28SOI_-LRPHP_-CNHLSX51_P10**	**C12T28SOI_-LRPHP_-CNHLSX51_P16**
CP to Q ↓	0.0431	0.0490	0.5171	0.5681
CP to Q ↑	0.0348	0.0394	0.7068	0.8021
	C12T28SOI_-LRPHP_-CNHLSX58_P0	**C12T28SOI_-LRPHP_-CNHLSX58_P4**	**C12T28SOI_-LRPHP_-CNHLSX58_P0**	**C12T28SOI_-LRPHP_-CNHLSX58_P4**
CP to Q ↓	0.0294	0.0328	0.3676	0.4002
CP to Q ↑	0.0232	0.0259	0.4902	0.5397
	C12T28SOI_-LRPHP_-CNHLSX58_P10	**C12T28SOI_-LRPHP_-CNHLSX58_P16**	**C12T28SOI_-LRPHP_-CNHLSX58_P10**	**C12T28SOI_-LRPHP_-CNHLSX58_P16**

CP to Q ↓	0.0380	0.0433	0.4474	0.4916
CP to Q ↑	0.0300	0.0341	0.6216	0.7050
	C12T28SOI_-LRPHP_-CNHLSX71_P0	**C12T28SOI_-LRPHP_-CNHLSX71_P4**	**C12T28SOI_-LRPHP_-CNHLSX71_P0**	**C12T28SOI_-LRPHP_-CNHLSX71_P4**
CP to Q ↓	0.0290	0.0326	0.3061	0.3331
CP to Q ↑	0.0238	0.0268	0.3979	0.4381
	C12T28SOI_-LRPHP_-CNHLSX71_P10	**C12T28SOI_-LRPHP_-CNHLSX71_P16**	**C12T28SOI_-LRPHP_-CNHLSX71_P10**	**C12T28SOI_-LRPHP_-CNHLSX71_P16**
CP to Q ↓	0.0376	0.0431	0.3730	0.4101
CP to Q ↑	0.0308	0.0353	0.5045	0.5719
	C12T28SOI_-LRPHP_-CNHLSX86_P0	**C12T28SOI_-LRPHP_-CNHLSX86_P4**	**C12T28SOI_-LRPHP_-CNHLSX86_P0**	**C12T28SOI_-LRPHP_-CNHLSX86_P4**
CP to Q ↓	0.0284	0.0320	0.2587	0.2818
CP to Q ↑	0.0237	0.0267	0.3356	0.3699
	C12T28SOI_-LRPHP_-CNHLSX86_P10	**C12T28SOI_-LRPHP_-CNHLSX86_P16**	**C12T28SOI_-LRPHP_-CNHLSX86_P10**	**C12T28SOI_-LRPHP_-CNHLSX86_P16**
CP to Q ↓	0.0373	0.0422	0.3153	0.3464
CP to Q ↑	0.0311	0.0351	0.4256	0.4821

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	C12T28SOI_-LRP_CNHLSX7_-P0	C12T28SOI_-LRP_CNHLSX7_-P4	C12T28SOI_-LRP_CNHLSX7_-P10	C12T28SOI_-LRP_CNHLSX7_-P16
CP ↓	min_pulse_width to CP	0.0424	0.0482	0.0558	0.0640
E ↓	hold_rising to CP	-0.0199	-0.0245	-0.0343	-0.0414
E ↑	hold_rising to CP	0.0036	0.0014	-0.0035	-0.0060
E ↓	setup_rising to CP	0.0471	0.0542	0.0639	0.0761
E ↑	setup_rising to CP	0.0316	0.0390	0.0460	0.0539
TE ↓	hold_rising to CP	-0.0226	-0.0272	-0.0343	-0.0440
TE ↑	hold_rising to CP	0.0014	-0.0012	-0.0035	-0.0087
TE ↓	setup_rising to CP	0.0472	0.0569	0.0691	0.0755
TE ↑	setup_rising to CP	0.0338	0.0386	0.0490	0.0557
		C12T28SOI_-LRP_-CNHLSX15_P0	C12T28SOI_-LRP_-CNHLSX15_P4	C12T28SOI_-LRP_-CNHLSX15_P10	C12T28SOI_-LRP_-CNHLSX15_P16
CP ↓	min_pulse_width to CP	0.0395	0.0447	0.0547	0.0599
E ↓	hold_rising to CP	-0.0199	-0.0245	-0.0343	-0.0440
E ↑	hold_rising to CP	0.0036	0.0014	-0.0035	-0.0057
E ↓	setup_rising to CP	0.0471	0.0542	0.0639	0.0761
E ↑	setup_rising to CP	0.0316	0.0390	0.0491	0.0557
TE ↓	hold_rising to CP	-0.0226	-0.0272	-0.0395	-0.0462

TE ↑	hold_rising to CP	0.0014	-0.0012	-0.0060	-0.0087
TE ↓	setup_rising to CP	0.0472	0.0569	0.0691	0.0755
TE ↑	setup_rising to CP	0.0334	0.0386	0.0487	0.0557
		C12T28SOI_-LRP_-CNHLSX22_P0	C12T28SOI_-LRP_-CNHLSX22_P4	C12T28SOI_-LRP_-CNHLSX22_P10	C12T28SOI_-LRP_-CNHLSX22_P16
CP ↓	min_pulse_width to CP	0.0467	0.0514	0.0596	0.0691
E ↓	hold_rising to CP	-0.0245	-0.0294	-0.0414	-0.0511
E ↑	hold_rising to CP	0.0014	-0.0038	-0.0060	-0.0083
E ↓	setup_rising to CP	0.0542	0.0591	0.0710	0.0807
E ↑	setup_rising to CP	0.0365	0.0439	0.0540	0.0606
TE ↓	hold_rising to CP	-0.0272	-0.0321	-0.0440	-0.0538
TE ↑	hold_rising to CP	-0.0012	-0.0035	-0.0087	-0.0105
TE ↓	setup_rising to CP	0.0569	0.0617	0.0737	0.0834
TE ↑	setup_rising to CP	0.0390	0.0435	0.0536	0.0662
		C12T28SOI_-LRP_-CNHLSX29_P0	C12T28SOI_-LRP_-CNHLSX29_P4	C12T28SOI_-LRP_-CNHLSX29_P10	C12T28SOI_-LRP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0467	0.0519	0.0614	0.0697
E ↓	hold_rising to CP	-0.0245	-0.0343	-0.0410	-0.0511
E ↑	hold_rising to CP	0.0014	-0.0038	-0.0060	-0.0083
E ↓	setup_rising to CP	0.0542	0.0639	0.0736	0.0859
E ↑	setup_rising to CP	0.0390	0.0439	0.0540	0.0637
TE ↓	hold_rising to CP	-0.0272	-0.0343	-0.0440	-0.0535
TE ↑	hold_rising to CP	-0.0012	-0.0035	-0.0087	-0.0105
TE ↓	setup_rising to CP	0.0569	0.0639	0.0758	0.0882
TE ↑	setup_rising to CP	0.0387	0.0491	0.0558	0.0659
		C12T28SOI_-LRP_-CNHLSX36_P0	C12T28SOI_-LRP_-CNHLSX36_P4	C12T28SOI_-LRP_-CNHLSX36_P10	C12T28SOI_-LRP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0462	0.0520	0.0601	0.0715
E ↓	hold_rising to CP	-0.0272	-0.0343	-0.0440	-0.0508
E ↑	hold_rising to CP	0.0014	-0.0038	-0.0060	-0.0083
E ↓	setup_rising to CP	0.0538	0.0639	0.0761	0.0859
E ↑	setup_rising to CP	0.0365	0.0439	0.0540	0.0637
TE ↓	hold_rising to CP	-0.0272	-0.0343	-0.0440	-0.0560
TE ↑	hold_rising to CP	-0.0012	-0.0035	-0.0087	-0.0105

TE ↓	setup_rising to CP	0.0569	0.0639	0.0758	0.0882
TE ↑	setup_rising to CP	0.0387	0.0435	0.0558	0.0662
		C12T28SOI_-LRP_-CNHLSX51_P0	C12T28SOI_-LRP_-CNHLSX51_P4	C12T28SOI_-LRP_-CNHLSX51_P10	C12T28SOI_-LRP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0437	0.0495	0.0614	0.0685
E ↓	hold_rising to CP	-0.0223	-0.0294	-0.0392	-0.0462
E ↑	hold_rising to CP	0.0011	-0.0012	-0.0035	-0.0083
E ↓	setup_rising to CP	0.0520	0.0591	0.0688	0.0810
E ↑	setup_rising to CP	0.0365	0.0439	0.0536	0.0637
TE ↓	hold_rising to CP	-0.0223	-0.0294	-0.0392	-0.0511
TE ↑	hold_rising to CP	0.0014	-0.0035	-0.0057	-0.0108
TE ↓	setup_rising to CP	0.0520	0.0591	0.0688	0.0810
TE ↑	setup_rising to CP	0.0387	0.0435	0.0558	0.0655
		C12T28SOI_-LRP_-CNHLSX58_P0	C12T28SOI_-LRP_-CNHLSX58_P4	C12T28SOI_-LRP_-CNHLSX58_P10	C12T28SOI_-LRP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0467	0.0544	0.0669	0.0764
E ↓	hold_rising to CP	-0.0294	-0.0392	-0.0489	-0.0609
E ↑	hold_rising to CP	-0.0012	-0.0038	-0.0060	-0.0108
E ↓	setup_rising to CP	0.0594	0.0664	0.0789	0.0907
E ↑	setup_rising to CP	0.0414	0.0487	0.0588	0.0686
TE ↓	hold_rising to CP	-0.0321	-0.0392	-0.0489	-0.0609
TE ↑	hold_rising to CP	-0.0012	-0.0035	-0.0083	-0.0105
TE ↓	setup_rising to CP	0.0594	0.0666	0.0785	0.0907
TE ↑	setup_rising to CP	0.0439	0.0484	0.0606	0.0704
		C12T28SOI_-LRP_-CNHLSX71_P0	C12T28SOI_-LRP_-CNHLSX71_P4	C12T28SOI_-LRP_-CNHLSX71_P10	C12T28SOI_-LRP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0486	0.0581	0.0669	0.0764
E ↓	hold_rising to CP	-0.0294	-0.0392	-0.0489	-0.0609
E ↑	hold_rising to CP	-0.0012	-0.0038	-0.0060	-0.0108
E ↓	setup_rising to CP	0.0594	0.0664	0.0785	0.0907
E ↑	setup_rising to CP	0.0414	0.0487	0.0582	0.0704
TE ↓	hold_rising to CP	-0.0321	-0.0392	-0.0514	-0.0639
TE ↑	hold_rising to CP	-0.0012	-0.0035	-0.0083	-0.0105
TE ↓	setup_rising to CP	0.0594	0.0691	0.0785	0.0938

TE ↑	setup_rising to CP	0.0439	0.0484	0.0606	0.0704
		C12T28SOI_-LRP_-CNHLSX93_P0	C12T28SOI_-LRP_-CNHLSX93_P4	C12T28SOI_-LRP_-CNHLSX93_P10	C12T28SOI_-LRP_-CNHLSX93_P16
CP ↓	min_pulse_width to CP	0.0516	0.0611	0.0712	0.0855
E ↓	hold_rising to CP	-0.0324	-0.0392	-0.0511	-0.0609
E ↑	hold_rising to CP	-0.0012	-0.0038	-0.0060	-0.0108
E ↓	setup_rising to CP	0.0591	0.0688	0.0810	0.0929
E ↑	setup_rising to CP	0.0462	0.0536	0.0633	0.0753
TE ↓	hold_rising to CP	-0.0321	-0.0422	-0.0538	-0.0661
TE ↑	hold_rising to CP	-0.0012	-0.0035	-0.0083	-0.0105
TE ↓	setup_rising to CP	0.0618	0.0688	0.0837	0.0956
TE ↑	setup_rising to CP	0.0462	0.0536	0.0655	0.0783
		C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0576	0.0691	0.0845	0.0970
E ↓	hold_rising to CP	-0.0064	-0.0117	-0.0166	-0.0240
E ↑	hold_rising to CP	0.0266	0.0297	0.0318	0.0341
E ↓	setup_rising to CP	0.0437	0.0515	0.0612	0.0682
E ↑	setup_rising to CP	0.0320	0.0372	0.0439	0.0509
TE ↓	hold_rising to CP	-0.0098	-0.0113	-0.0162	-0.0267
TE ↑	hold_rising to CP	0.0273	0.0269	0.0293	0.0344
TE ↓	setup_rising to CP	0.0437	0.0511	0.0612	0.0709
TE ↑	setup_rising to CP	0.0316	0.0369	0.0439	0.0540
		C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0576	0.0691	0.0845	0.0971
E ↓	hold_rising to CP	-0.0064	-0.0113	-0.0191	-0.0240
E ↑	hold_rising to CP	0.0266	0.0297	0.0318	0.0341
E ↓	setup_rising to CP	0.0437	0.0508	0.0612	0.0678
E ↑	setup_rising to CP	0.0324	0.0341	0.0443	0.0487
TE ↓	hold_rising to CP	-0.0098	-0.0113	-0.0218	-0.0267
TE ↑	hold_rising to CP	0.0273	0.0269	0.0293	0.0344
TE ↓	setup_rising to CP	0.0437	0.0508	0.0608	0.0709
TE ↑	setup_rising to CP	0.0317	0.0369	0.0439	0.0540

		C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP ↓	min_pulse_width to CP	0.0601	0.0696	0.0845	0.0995
E ↓	hold_rising to CP	-0.0064	-0.0113	-0.0191	-0.0237
E ↑	hold_rising to CP	0.0266	0.0297	0.0318	0.0341
E ↓	setup_rising to CP	0.0459	0.0508	0.0630	0.0731
E ↑	setup_rising to CP	0.0317	0.0365	0.0439	0.0540
TE ↓	hold_rising to CP	-0.0098	-0.0113	-0.0218	-0.0264
TE ↑	hold_rising to CP	0.0273	0.0269	0.0293	0.0344
TE ↓	setup_rising to CP	0.0434	0.0539	0.0630	0.0727
TE ↑	setup_rising to CP	0.0316	0.0390	0.0460	0.0536
		C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0601	0.0696	0.0845	0.0995
E ↓	hold_rising to CP	-0.0064	-0.0113	-0.0191	-0.0237
E ↑	hold_rising to CP	0.0266	0.0297	0.0318	0.0341
E ↓	setup_rising to CP	0.0437	0.0508	0.0609	0.0678
E ↑	setup_rising to CP	0.0317	0.0365	0.0439	0.0540
TE ↓	hold_rising to CP	-0.0095	-0.0144	-0.0218	-0.0264
TE ↑	hold_rising to CP	0.0273	0.0269	0.0293	0.0344
TE ↓	setup_rising to CP	0.0437	0.0508	0.0605	0.0709
TE ↑	setup_rising to CP	0.0316	0.0390	0.0491	0.0561
		C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0606	0.0702	0.0894	0.1049
E ↓	hold_rising to CP	-0.0095	-0.0113	-0.0215	-0.0289
E ↑	hold_rising to CP	0.0266	0.0297	0.0318	0.0341
E ↓	setup_rising to CP	0.0486	0.0557	0.0654	0.0780
E ↑	setup_rising to CP	0.0317	0.0365	0.0466	0.0536
TE ↓	hold_rising to CP	-0.0091	-0.0144	-0.0215	-0.0289
TE ↑	hold_rising to CP	0.0273	0.0269	0.0293	0.0344
TE ↓	setup_rising to CP	0.0486	0.0557	0.0654	0.0776
TE ↑	setup_rising to CP	0.0316	0.0390	0.0491	0.0558

		C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0655	0.0750	0.0942	0.1073
E ↓	hold_rising to CP	-0.0143	-0.0162	-0.0263	-0.0338
E ↑	hold_rising to CP	0.0273	0.0269	0.0293	0.0344
E ↓	setup_rising to CP	0.0535	0.0605	0.0727	0.0825
E ↑	setup_rising to CP	0.0365	0.0414	0.0515	0.0607
TE ↓	hold_rising to CP	-0.0143	-0.0192	-0.0263	-0.0337
TE ↑	hold_rising to CP	0.0273	0.0269	0.0296	0.0323
TE ↓	setup_rising to CP	0.0535	0.0605	0.0758	0.0856
TE ↑	setup_rising to CP	0.0365	0.0439	0.0540	0.0637
		C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP ↓	min_pulse_width to CP	0.0655	0.0787	0.0924	0.1097
E ↓	hold_rising to CP	-0.0091	-0.0169	-0.0215	-0.0289
E ↑	hold_rising to CP	0.0273	0.0266	0.0318	0.0341
E ↓	setup_rising to CP	0.0508	0.0612	0.0706	0.0829
E ↑	setup_rising to CP	0.0365	0.0414	0.0515	0.0638
TE ↓	hold_rising to CP	-0.0091	-0.0165	-0.0211	-0.0315
TE ↑	hold_rising to CP	0.0273	0.0269	0.0293	0.0344
TE ↓	setup_rising to CP	0.0535	0.0583	0.0703	0.0825
TE ↑	setup_rising to CP	0.0365	0.0439	0.0540	0.0637

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LRP_CNHLSX7_P0	2.136e-05	1.894e-09
C12T28SOI_LRP_CNHLSX7_P4	7.330e-06	1.894e-09
C12T28SOI_LRP_CNHLSX7_P10	2.362e-06	1.894e-09
C12T28SOI_LRP_CNHLSX7_P16	1.124e-06	1.894e-09
C12T28SOI_LRP_CNHLSX15_P0	2.787e-05	2.013e-09
C12T28SOI_LRP_CNHLSX15_P4	9.396e-06	2.013e-09
C12T28SOI_LRP_CNHLSX15_P10	2.997e-06	2.013e-09
C12T28SOI_LRP_CNHLSX15_P16	1.422e-06	2.013e-09
C12T28SOI_LRP_CNHLSX22_P0	3.266e-05	2.370e-09
C12T28SOI_LRP_CNHLSX22_P4	1.074e-05	2.370e-09
C12T28SOI_LRP_CNHLSX22_P10	3.361e-06	2.370e-09
C12T28SOI_LRP_CNHLSX22_P16	1.580e-06	2.370e-09
C12T28SOI_LRP_CNHLSX29_P0	3.702e-05	2.489e-09
C12T28SOI_LRP_CNHLSX29_P4	1.219e-05	2.489e-09
C12T28SOI_LRP_CNHLSX29_P10	3.818e-06	2.489e-09
C12T28SOI_LRP_CNHLSX29_P16	1.798e-06	2.489e-09

C12T28SOI_LRP_CNHLSX36_P0	4.197e-05	2.608e-09
C12T28SOI_LRP_CNHLSX36_P4	1.377e-05	2.608e-09
C12T28SOI_LRP_CNHLSX36_P10	4.306e-06	2.608e-09
C12T28SOI_LRP_CNHLSX36_P16	2.027e-06	2.608e-09
C12T28SOI_LRP_CNHLSX51_P0	5.178e-05	3.085e-09
C12T28SOI_LRP_CNHLSX51_P4	1.703e-05	3.085e-09
C12T28SOI_LRP_CNHLSX51_P10	5.333e-06	3.085e-09
C12T28SOI_LRP_CNHLSX51_P16	2.512e-06	3.085e-09
C12T28SOI_LRP_CNHLSX58_P0	6.271e-05	4.131e-09
C12T28SOI_LRP_CNHLSX58_P4	2.091e-05	4.131e-09
C12T28SOI_LRP_CNHLSX58_P10	6.630e-06	4.131e-09
C12T28SOI_LRP_CNHLSX58_P16	3.146e-06	4.131e-09
C12T28SOI_LRP_CNHLSX71_P0	7.405e-05	4.613e-09
C12T28SOI_LRP_CNHLSX71_P4	2.467e-05	4.613e-09
C12T28SOI_LRP_CNHLSX71_P10	7.809e-06	4.613e-09
C12T28SOI_LRP_CNHLSX71_P16	3.700e-06	4.613e-09
C12T28SOI_LRP_CNHLSX93_P0	8.889e-05	5.089e-09
C12T28SOI_LRP_CNHLSX93_P4	2.936e-05	5.089e-09
C12T28SOI_LRP_CNHLSX93_P10	9.240e-06	5.089e-09
C12T28SOI_LRP_CNHLSX93_P16	4.370e-06	5.089e-09
C12T28SOI_LRPHP_CNHLSX29_P0	4.398e-05	2.966e-09
C12T28SOI_LRPHP_CNHLSX29_P4	1.469e-05	2.966e-09
C12T28SOI_LRPHP_CNHLSX29_P10	4.649e-06	2.966e-09
C12T28SOI_LRPHP_CNHLSX29_P16	2.195e-06	2.966e-09
C12T28SOI_LRPHP_CNHLSX36_P0	4.888e-05	3.085e-09
C12T28SOI_LRPHP_CNHLSX36_P4	1.627e-05	3.085e-09
C12T28SOI_LRPHP_CNHLSX36_P10	5.139e-06	3.085e-09
C12T28SOI_LRPHP_CNHLSX36_P16	2.426e-06	3.085e-09
C12T28SOI_LRPHP_CNHLSX44_P0	5.495e-05	3.442e-09
C12T28SOI_LRPHP_CNHLSX44_P4	1.833e-05	3.442e-09
C12T28SOI_LRPHP_CNHLSX44_P10	5.790e-06	3.442e-09
C12T28SOI_LRPHP_CNHLSX44_P16	2.734e-06	3.442e-09
C12T28SOI_LRPHP_CNHLSX51_P0	5.859e-05	3.561e-09
C12T28SOI_LRPHP_CNHLSX51_P4	1.942e-05	3.561e-09
C12T28SOI_LRPHP_CNHLSX51_P10	6.107e-06	3.561e-09
C12T28SOI_LRPHP_CNHLSX51_P16	2.878e-06	3.561e-09
C12T28SOI_LRPHP_CNHLSX58_P0	6.930e-05	4.608e-09
C12T28SOI_LRPHP_CNHLSX58_P4	2.328e-05	4.608e-09
C12T28SOI_LRPHP_CNHLSX58_P10	7.421e-06	4.608e-09
C12T28SOI_LRPHP_CNHLSX58_P16	3.525e-06	4.608e-09
C12T28SOI_LRPHP_CNHLSX71_P0	8.145e-05	5.015e-09
C12T28SOI_LRPHP_CNHLSX71_P4	2.719e-05	5.015e-09
C12T28SOI_LRPHP_CNHLSX71_P10	8.626e-06	5.015e-09
C12T28SOI_LRPHP_CNHLSX71_P16	4.088e-06	5.015e-09
C12T28SOI_LRPHP_CNHLSX86_P0	9.190e-05	5.447e-09
C12T28SOI_LRPHP_CNHLSX86_P4	3.063e-05	5.447e-09
C12T28SOI_LRPHP_CNHLSX86_P10	9.706e-06	5.447e-09
C12T28SOI_LRPHP_CNHLSX86_P16	4.600e-06	5.447e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LRP_-CNHLSX7_P0	C12T28SOI_LRP_-CNHLSX7_P4	C12T28SOI_LRP_-CNHLSX7_P10	C12T28SOI_LRP_-CNHLSX7_P16

CP (output stable)	1.753e-03	1.776e-03	1.846e-03	1.913e-03
E (output stable)	8.983e-04	8.791e-04	8.859e-04	9.031e-04
TE (output stable)	1.007e-03	1.013e-03	1.040e-03	1.075e-03
CP to Q	2.414e-03	2.410e-03	2.470e-03	2.548e-03
	C12T28SOI_LRP_-CNHLSX15_P0	C12T28SOI_LRP_-CNHLSX15_P4	C12T28SOI_LRP_-CNHLSX15_P10	C12T28SOI_LRP_-CNHLSX15_P16
CP (output stable)	2.037e-03	2.075e-03	2.158e-03	2.241e-03
E (output stable)	9.254e-04	9.084e-04	9.182e-04	9.393e-04
TE (output stable)	1.033e-03	1.042e-03	1.072e-03	1.110e-03
CP to Q	3.516e-03	3.491e-03	3.599e-03	3.703e-03
	C12T28SOI_LRP_-CNHLSX22_P0	C12T28SOI_LRP_-CNHLSX22_P4	C12T28SOI_LRP_-CNHLSX22_P10	C12T28SOI_LRP_-CNHLSX22_P16
CP (output stable)	2.297e-03	2.340e-03	2.429e-03	2.530e-03
E (output stable)	9.993e-04	9.831e-04	9.945e-04	1.017e-03
TE (output stable)	1.108e-03	1.116e-03	1.148e-03	1.188e-03
CP to Q	4.559e-03	4.487e-03	4.627e-03	4.762e-03
	C12T28SOI_LRP_-CNHLSX29_P0	C12T28SOI_LRP_-CNHLSX29_P4	C12T28SOI_LRP_-CNHLSX29_P10	C12T28SOI_LRP_-CNHLSX29_P16
CP (output stable)	2.392e-03	2.439e-03	2.558e-03	2.659e-03
E (output stable)	1.021e-03	1.004e-03	1.015e-03	1.036e-03
TE (output stable)	1.129e-03	1.138e-03	1.169e-03	1.208e-03
CP to Q	5.508e-03	5.469e-03	5.554e-03	5.796e-03
	C12T28SOI_LRP_-CNHLSX36_P0	C12T28SOI_LRP_-CNHLSX36_P4	C12T28SOI_LRP_-CNHLSX36_P10	C12T28SOI_LRP_-CNHLSX36_P16
CP (output stable)	2.555e-03	2.604e-03	2.727e-03	2.844e-03
E (output stable)	1.022e-03	1.005e-03	1.018e-03	1.041e-03
TE (output stable)	1.130e-03	1.139e-03	1.171e-03	1.212e-03
CP to Q	6.413e-03	6.369e-03	6.530e-03	6.782e-03
	C12T28SOI_LRP_-CNHLSX51_P0	C12T28SOI_LRP_-CNHLSX51_P4	C12T28SOI_LRP_-CNHLSX51_P10	C12T28SOI_LRP_-CNHLSX51_P16
CP (output stable)	2.801e-03	2.884e-03	3.024e-03	3.161e-03
E (output stable)	1.029e-03	1.016e-03	1.030e-03	1.056e-03
TE (output stable)	1.137e-03	1.149e-03	1.184e-03	1.227e-03
CP to Q	8.552e-03	8.567e-03	8.752e-03	9.077e-03
	C12T28SOI_LRP_-CNHLSX58_P0	C12T28SOI_LRP_-CNHLSX58_P4	C12T28SOI_LRP_-CNHLSX58_P10	C12T28SOI_LRP_-CNHLSX58_P16
CP (output stable)	3.642e-03	3.759e-03	3.961e-03	4.138e-03
E (output stable)	1.144e-03	1.132e-03	1.151e-03	1.180e-03
TE (output stable)	1.251e-03	1.264e-03	1.302e-03	1.349e-03
CP to Q	9.806e-03	9.695e-03	9.922e-03	1.033e-02
	C12T28SOI_LRP_-CNHLSX71_P0	C12T28SOI_LRP_-CNHLSX71_P4	C12T28SOI_LRP_-CNHLSX71_P10	C12T28SOI_LRP_-CNHLSX71_P16
CP (output stable)	4.092e-03	4.260e-03	4.471e-03	4.695e-03
E (output stable)	1.182e-03	1.173e-03	1.195e-03	1.228e-03
TE (output stable)	1.289e-03	1.305e-03	1.346e-03	1.397e-03
CP to Q	1.189e-02	1.195e-02	1.223e-02	1.267e-02
	C12T28SOI_LRP_-CNHLSX93_P0	C12T28SOI_LRP_-CNHLSX93_P4	C12T28SOI_LRP_-CNHLSX93_P10	C12T28SOI_LRP_-CNHLSX93_P16
CP (output stable)	4.657e-03	4.868e-03	5.134e-03	5.399e-03
E (output stable)	1.276e-03	1.268e-03	1.294e-03	1.330e-03
TE (output stable)	1.384e-03	1.402e-03	1.447e-03	1.501e-03
CP to Q	1.535e-02	1.530e-02	1.557e-02	1.623e-02

	C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP (output stable)	3.407e-03	3.503e-03	3.661e-03	3.801e-03
E (output stable)	9.451e-04	9.253e-04	9.318e-04	9.504e-04
TE (output stable)	1.052e-03	1.058e-03	1.085e-03	1.122e-03
CP to Q	6.882e-03	6.911e-03	7.029e-03	7.289e-03
	C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP (output stable)	3.552e-03	3.651e-03	3.830e-03	3.990e-03
E (output stable)	9.503e-04	9.315e-04	9.392e-04	9.587e-04
TE (output stable)	1.057e-03	1.064e-03	1.093e-03	1.131e-03
CP to Q	7.722e-03	7.770e-03	7.960e-03	8.221e-03
	C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP (output stable)	3.806e-03	3.943e-03	4.121e-03	4.302e-03
E (output stable)	9.855e-04	9.681e-04	9.782e-04	1.000e-03
TE (output stable)	1.092e-03	1.101e-03	1.132e-03	1.172e-03
CP to Q	8.905e-03	8.795e-03	8.911e-03	9.224e-03
	C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP (output stable)	3.838e-03	3.938e-03	4.132e-03	4.303e-03
E (output stable)	9.857e-04	9.682e-04	9.783e-04	1.000e-03
TE (output stable)	1.093e-03	1.101e-03	1.132e-03	1.172e-03
CP to Q	9.723e-03	9.638e-03	9.809e-03	1.015e-02
	C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP (output stable)	4.450e-03	4.589e-03	4.867e-03	5.059e-03
E (output stable)	1.040e-03	1.024e-03	1.037e-03	1.062e-03
TE (output stable)	1.146e-03	1.157e-03	1.190e-03	1.234e-03
CP to Q	1.063e-02	1.056e-02	1.076e-02	1.121e-02
	C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP (output stable)	4.956e-03	5.134e-03	5.404e-03	5.690e-03
E (output stable)	1.127e-03	1.112e-03	1.127e-03	1.155e-03
TE (output stable)	1.234e-03	1.245e-03	1.280e-03	1.327e-03
CP to Q	1.276e-02	1.274e-02	1.292e-02	1.357e-02
	C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP (output stable)	5.415e-03	5.585e-03	5.881e-03	6.199e-03
E (output stable)	1.149e-03	1.139e-03	1.156e-03	1.193e-03
TE (output stable)	1.256e-03	1.272e-03	1.310e-03	1.365e-03
CP to Q	1.461e-02	1.466e-02	1.508e-02	1.557e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	C12T28SOI_LRP_-CNHLSX7_P0	C12T28SOI_LRP_-CNHLSX7_P4	C12T28SOI_LRP_-CNHLSX7_P10	C12T28SOI_LRP_-CNHLSX7_P16
CP (output stable)	-2.421e-05	-2.200e-05	-1.681e-05	-1.459e-05
E (output stable)	2.320e-06	8.527e-06	9.711e-06	7.196e-06
TE (output stable)	2.218e-07	-2.456e-07	-1.257e-06	-3.715e-06
CP to Q	1.227e-05	1.283e-05	1.079e-05	9.845e-06
	C12T28SOI_LRP_-CNHLSX15_P0	C12T28SOI_LRP_-CNHLSX15_P4	C12T28SOI_LRP_-CNHLSX15_P10	C12T28SOI_LRP_-CNHLSX15_P16
CP (output stable)	-1.744e-05	-1.487e-05	-1.116e-05	-8.028e-06
E (output stable)	2.386e-06	8.574e-06	9.829e-06	7.215e-06
TE (output stable)	2.249e-07	-2.409e-07	-1.275e-06	-3.695e-06
CP to Q	6.142e-06	5.417e-06	3.386e-06	1.874e-06
	C12T28SOI_LRP_-CNHLSX22_P0	C12T28SOI_LRP_-CNHLSX22_P4	C12T28SOI_LRP_-CNHLSX22_P10	C12T28SOI_LRP_-CNHLSX22_P16
CP (output stable)	-6.074e-07	1.182e-06	4.487e-06	7.951e-06
E (output stable)	2.367e-06	8.567e-06	9.825e-06	7.205e-06
TE (output stable)	2.203e-07	-1.923e-07	-1.283e-06	-3.706e-06
CP to Q	1.695e-05	1.813e-05	1.414e-05	1.361e-05
	C12T28SOI_LRP_-CNHLSX29_P0	C12T28SOI_LRP_-CNHLSX29_P4	C12T28SOI_LRP_-CNHLSX29_P10	C12T28SOI_LRP_-CNHLSX29_P16
CP (output stable)	-1.426e-05	-1.262e-05	-7.326e-06	-2.645e-06
E (output stable)	2.329e-06	8.536e-06	9.806e-06	7.203e-06
TE (output stable)	1.818e-07	-2.332e-07	-1.268e-06	-3.721e-06
CP to Q	1.111e-05	1.193e-05	8.598e-06	6.469e-06
	C12T28SOI_LRP_-CNHLSX36_P0	C12T28SOI_LRP_-CNHLSX36_P4	C12T28SOI_LRP_-CNHLSX36_P10	C12T28SOI_LRP_-CNHLSX36_P16
CP (output stable)	-4.656e-06	-2.585e-06	2.269e-06	7.263e-06
E (output stable)	2.336e-06	8.549e-06	9.818e-06	7.189e-06
TE (output stable)	1.880e-07	-2.516e-07	-1.271e-06	-3.698e-06
CP to Q	2.720e-05	2.699e-05	2.245e-05	1.985e-05
	C12T28SOI_LRP_-CNHLSX51_P0	C12T28SOI_LRP_-CNHLSX51_P4	C12T28SOI_LRP_-CNHLSX51_P10	C12T28SOI_LRP_-CNHLSX51_P16
CP (output stable)	-1.102e-05	-8.126e-06	-2.703e-06	2.742e-06
E (output stable)	2.362e-06	8.566e-06	9.828e-06	7.212e-06
TE (output stable)	2.381e-07	-2.412e-07	-1.290e-06	-3.683e-06
CP to Q	3.488e-05	3.304e-05	2.797e-05	2.259e-05
	C12T28SOI_LRP_-CNHLSX58_P0	C12T28SOI_LRP_-CNHLSX58_P4	C12T28SOI_LRP_-CNHLSX58_P10	C12T28SOI_LRP_-CNHLSX58_P16
CP (output stable)	-3.874e-05	-3.565e-05	-2.828e-05	-2.330e-05
E (output stable)	2.375e-06	8.459e-06	9.612e-06	7.078e-06
TE (output stable)	1.737e-07	-2.359e-07	-1.264e-06	-3.708e-06
CP to Q	3.399e-05	3.399e-05	2.493e-05	2.405e-05
	C12T28SOI_LRP_-CNHLSX71_P0	C12T28SOI_LRP_-CNHLSX71_P4	C12T28SOI_LRP_-CNHLSX71_P10	C12T28SOI_LRP_-CNHLSX71_P16
CP (output stable)	-2.592e-05	-2.370e-05	-1.637e-05	-8.471e-06
E (output stable)	2.357e-06	8.467e-06	9.617e-06	7.090e-06
TE (output stable)	1.694e-07	-2.284e-07	-1.248e-06	-3.635e-06
CP to Q	2.965e-05	3.143e-05	2.347e-05	1.739e-05
	C12T28SOI_LRP_-CNHLSX93_P0	C12T28SOI_LRP_-CNHLSX93_P4	C12T28SOI_LRP_-CNHLSX93_P10	C12T28SOI_LRP_-CNHLSX93_P16
CP (output stable)	-3.018e-05	-2.652e-05	-1.698e-05	-9.552e-06
E (output stable)	2.351e-06	8.564e-06	9.843e-06	7.215e-06
TE (output stable)	1.773e-07	-2.281e-07	-1.261e-06	-3.650e-06

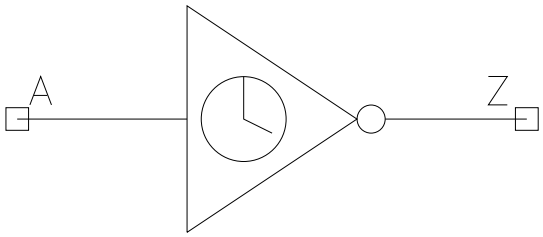
CP to Q	5.513e-05	5.197e-05	4.849e-05	3.822e-05
	C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP (output stable)	-2.319e-05	-1.999e-05	-1.531e-05	-1.046e-05
E (output stable)	2.209e-06	8.507e-06	9.525e-06	7.120e-06
TE (output stable)	2.071e-07	-1.538e-07	-1.373e-06	-3.590e-06
CP to Q	1.652e-05	1.645e-05	1.147e-05	9.647e-06
	C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP (output stable)	-1.454e-05	-1.144e-05	-6.127e-06	1.058e-06
E (output stable)	2.210e-06	8.513e-06	9.526e-06	7.122e-06
TE (output stable)	2.026e-07	-1.466e-07	-1.359e-06	-3.555e-06
CP to Q	2.470e-05	2.283e-05	2.064e-05	1.680e-05
	C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP (output stable)	-2.417e-05	-2.001e-05	-1.166e-05	-4.924e-06
E (output stable)	2.211e-06	8.515e-06	9.525e-06	7.123e-06
TE (output stable)	2.045e-07	-1.496e-07	-1.361e-06	-3.548e-06
CP to Q	2.375e-05	2.382e-05	1.766e-05	1.496e-05
	C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP (output stable)	-2.318e-05	-1.985e-05	-1.146e-05	-6.050e-06
E (output stable)	2.211e-06	8.518e-06	9.524e-06	7.120e-06
TE (output stable)	2.043e-07	-8.539e-08	-1.362e-06	-3.574e-06
CP to Q	3.207e-05	3.240e-05	2.416e-05	2.349e-05
	C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP (output stable)	-4.182e-05	-3.712e-05	-3.427e-05	-2.347e-05
E (output stable)	2.207e-06	8.513e-06	9.529e-06	7.121e-06
TE (output stable)	2.018e-07	-1.479e-07	-1.342e-06	-3.510e-06
CP to Q	3.510e-05	3.422e-05	2.606e-05	2.158e-05
	C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP (output stable)	-3.368e-05	-2.590e-05	-2.547e-05	-1.033e-05
E (output stable)	2.197e-06	8.503e-06	9.525e-06	7.131e-06
TE (output stable)	2.036e-07	-1.557e-07	-1.344e-06	-3.535e-06
CP to Q	3.393e-05	3.399e-05	2.716e-05	2.060e-05
	C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP (output stable)	-3.919e-05	-2.536e-05	-5.628e-06	-1.418e-05
E (output stable)	2.202e-06	8.516e-06	9.525e-06	7.137e-06
TE (output stable)	2.164e-07	-1.541e-07	-1.346e-06	-3.516e-06
CP to Q	3.935e-05	3.884e-05	2.165e-05	1.878e-05

CNIV

Cell Description

Inverter with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.272	0.3264
X5_P4	1.200	0.272	0.3264
X5_P10	1.200	0.272	0.3264
X5_P16	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X16_P0	1.200	0.408	0.4896
X16_P4	1.200	0.408	0.4896
X16_P10	1.200	0.408	0.4896
X16_P16	1.200	0.408	0.4896
X23_P0	1.200	0.544	0.6528
X23_P4	1.200	0.544	0.6528
X23_P10	1.200	0.544	0.6528
X23_P16	1.200	0.544	0.6528
X31_P0	1.200	0.680	0.8160
X31_P4	1.200	0.680	0.8160
X31_P10	1.200	0.680	0.8160
X31_P16	1.200	0.680	0.8160
X39_P0	1.200	0.816	0.9792
X39_P4	1.200	0.816	0.9792
X39_P10	1.200	0.816	0.9792
X39_P16	1.200	0.816	0.9792
X47_P0	1.200	0.952	1.1424
X47_P4	1.200	0.952	1.1424
X47_P10	1.200	0.952	1.1424
X47_P16	1.200	0.952	1.1424
X55_P0	1.200	1.088	1.3056
X55_P4	1.200	1.088	1.3056
X55_P10	1.200	1.088	1.3056
X55_P16	1.200	1.088	1.3056
X61_P0	1.200	1.224	1.4688

X61_P4	1.200	1.224	1.4688
X61_P10	1.200	1.224	1.4688
X61_P16	1.200	1.224	1.4688
X70_P0	1.200	1.360	1.6320
X70_P4	1.200	1.360	1.6320
X70_P10	1.200	1.360	1.6320
X70_P16	1.200	1.360	1.6320
X94_P0	1.200	1.768	2.1216
X94_P4	1.200	1.768	2.1216
X94_P10	1.200	1.768	2.1216
X94_P16	1.200	1.768	2.1216
X133_P0	1.200	2.448	2.9376
X133_P4	1.200	2.448	2.9376
X133_P10	1.200	2.448	2.9376
X133_P16	1.200	2.448	2.9376

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X5_P0	X5_P4	X5_P10	X5_P16
A	0.0005	0.0005	0.0005	0.0006
	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0007	0.0008	0.0008	0.0008
	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0014	0.0014	0.0015	0.0015
	X23_P0	X23_P4	X23_P10	X23_P16
A	0.0020	0.0021	0.0022	0.0023
	X31_P0	X31_P4	X31_P10	X31_P16
A	0.0026	0.0027	0.0029	0.0030
	X39_P0	X39_P4	X39_P10	X39_P16
A	0.0033	0.0034	0.0036	0.0037
	X47_P0	X47_P4	X47_P10	X47_P16
A	0.0041	0.0041	0.0043	0.0045
	X55_P0	X55_P4	X55_P10	X55_P16
A	0.0047	0.0047	0.0050	0.0052
	X61_P0	X61_P4	X61_P10	X61_P16
A	0.0051	0.0054	0.0056	0.0059
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0061	0.0063	0.0065	0.0069
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0084	0.0086	0.0090	0.0094
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0125	0.0127	0.0132	0.0136

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X5_P4	X5_P0	X5_P4
A to Z ↓	0.0091	0.0104	4.0430	4.3972

A to Z ↑	0.0155	0.0174	7.0992	7.8962
	X5_P10	**X5_P16**	**X5_P10**	**X5_P16**
A to Z ↓	0.0121	0.0136	4.9127	5.3883
A to Z ↑	0.0199	0.0221	9.1756	10.4749
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0081	0.0092	2.5388	2.7521
A to Z ↑	0.0127	0.0143	3.7793	4.1740
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0107	0.0120	3.0585	3.3411
A to Z ↑	0.0164	0.0182	4.8067	5.4505
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0066	0.0077	1.2513	1.3538
A to Z ↑	0.0109	0.0124	1.8884	2.0833
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0091	0.0103	1.5044	1.6423
A to Z ↑	0.0144	0.0161	2.3975	2.7154
	X23_P0	**X23_P4**	**X23_P0**	**X23_P4**
A to Z ↓	0.0072	0.0083	0.8946	0.9683
A to Z ↑	0.0111	0.0127	1.2815	1.4102
	X23_P10	**X23_P16**	**X23_P10**	**X23_P16**
A to Z ↓	0.0098	0.0109	1.0770	1.1764
A to Z ↑	0.0147	0.0164	1.6245	1.8398
	X31_P0	**X31_P4**	**X31_P0**	**X31_P4**
A to Z ↓	0.0067	0.0077	0.6483	0.7018
A to Z ↑	0.0106	0.0121	0.9591	1.0568
	X31_P10	**X31_P16**	**X31_P10**	**X31_P16**
A to Z ↓	0.0091	0.0103	0.7808	0.8523
A to Z ↑	0.0140	0.0157	1.2147	1.3743
	X39_P0	**X39_P4**	**X39_P0**	**X39_P4**
A to Z ↓	0.0072	0.0083	0.5244	0.5686
A to Z ↑	0.0110	0.0125	0.7716	0.8501
	X39_P10	**X39_P16**	**X39_P10**	**X39_P16**
A to Z ↓	0.0097	0.0109	0.6321	0.6906
A to Z ↑	0.0146	0.0162	0.9769	1.1053
	X47_P0	**X47_P4**	**X47_P0**	**X47_P4**
A to Z ↓	0.0071	0.0081	0.4365	0.4736
A to Z ↑	0.0108	0.0123	0.6428	0.7086
	X47_P10	**X47_P16**	**X47_P10**	**X47_P16**
A to Z ↓	0.0095	0.0108	0.5269	0.5755
A to Z ↑	0.0143	0.0160	0.8138	0.9210
	X55_P0	**X55_P4**	**X55_P0**	**X55_P4**
A to Z ↓	0.0075	0.0085	0.3773	0.4091
A to Z ↑	0.0112	0.0127	0.5521	0.6085
	X55_P10	**X55_P16**	**X55_P10**	**X55_P16**
A to Z ↓	0.0100	0.0112	0.4550	0.4973
A to Z ↑	0.0147	0.0164	0.6989	0.7910
	X61_P0	**X61_P4**	**X61_P0**	**X61_P4**
A to Z ↓	0.0075	0.0086	0.3396	0.3683
A to Z ↑	0.0111	0.0127	0.5003	0.5515
	X61_P10	**X61_P16**	**X61_P10**	**X61_P16**
A to Z ↓	0.0101	0.0113	0.4100	0.4480
A to Z ↑	0.0147	0.0164	0.6335	0.7176

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0079	0.0090	0.2976	0.3223
A to Z ↑	0.0115	0.0131	0.4334	0.4766
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0104	0.0116	0.3586	0.3917
A to Z ↑	0.0151	0.0168	0.5478	0.6189
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0089	0.0098	0.2286	0.2473
A to Z ↑	0.0123	0.0137	0.3300	0.3622
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0113	0.0127	0.2743	0.2989
A to Z ↑	0.0159	0.0177	0.4151	0.4691
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0104	0.0112	0.1684	0.1820
A to Z ↑	0.0136	0.0150	0.2383	0.2612
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0129	0.0143	0.2014	0.2192
A to Z ↑	0.0172	0.0192	0.2981	0.3364

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X5_P0	2.958e-06	5.836e-10
X5_P4	1.060e-06	5.836e-10
X5_P10	3.487e-07	5.836e-10
X5_P16	1.655e-07	5.836e-10
X8_P0	4.904e-06	5.836e-10
X8_P4	1.701e-06	5.836e-10
X8_P10	5.541e-07	5.836e-10
X8_P16	2.638e-07	5.836e-10
X16_P0	9.865e-06	7.027e-10
X16_P4	3.398e-06	7.027e-10
X16_P10	1.094e-06	7.027e-10
X16_P16	5.177e-07	7.027e-10
X23_P0	1.366e-05	8.218e-10
X23_P4	4.652e-06	8.218e-10
X23_P10	1.484e-06	8.218e-10
X23_P16	6.989e-07	8.218e-10
X31_P0	1.821e-05	9.409e-10
X31_P4	6.157e-06	9.409e-10
X31_P10	1.954e-06	9.409e-10
X31_P16	9.183e-07	9.409e-10
X39_P0	2.223e-05	1.060e-09
X39_P4	7.502e-06	1.060e-09
X39_P10	2.375e-06	1.060e-09
X39_P16	1.114e-06	1.060e-09
X47_P0	2.600e-05	1.179e-09
X47_P4	8.800e-06	1.179e-09
X47_P10	2.788e-06	1.179e-09
X47_P16	1.308e-06	1.179e-09
X55_P0	3.041e-05	1.298e-09
X55_P4	1.021e-05	1.298e-09
X55_P10	3.217e-06	1.298e-09

X55_P16	1.506e-06	1.298e-09
X61_P0	3.377e-05	1.417e-09
X61_P4	1.126e-05	1.417e-09
X61_P10	3.536e-06	1.417e-09
X61_P16	1.653e-06	1.417e-09
X70_P0	3.803e-05	1.536e-09
X70_P4	1.281e-05	1.536e-09
X70_P10	4.040e-06	1.536e-09
X70_P16	1.892e-06	1.536e-09
X94_P0	5.010e-05	1.894e-09
X94_P4	1.683e-05	1.894e-09
X94_P10	5.298e-06	1.894e-09
X94_P16	2.478e-06	1.894e-09
X133_P0	7.194e-05	2.489e-09
X133_P4	2.384e-05	2.489e-09
X133_P10	7.440e-06	2.489e-09
X133_P16	3.469e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	3.875e-04	3.654e-04	3.562e-04	3.566e-04
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	5.455e-04	4.967e-04	4.716e-04	4.640e-04
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	9.021e-04	7.958e-04	7.279e-04	7.029e-04
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	1.402e-03	1.257e-03	1.163e-03	1.132e-03
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	1.742e-03	1.528e-03	1.367e-03	1.342e-03
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	2.257e-03	2.006e-03	1.853e-03	1.788e-03
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	2.640e-03	2.332e-03	2.151e-03	2.069e-03
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	3.174e-03	2.819e-03	2.611e-03	2.523e-03
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	3.419e-03	3.014e-03	2.765e-03	2.669e-03
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	4.048e-03	3.601e-03	3.305e-03	3.195e-03
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	5.369e-03	4.684e-03	4.275e-03	4.115e-03
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	8.113e-03	6.987e-03	6.306e-03	6.050e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	1.535e-07	-2.190e-08	-1.342e-07	-7.970e-08
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	1.555e-07	3.797e-07	-3.018e-07	-3.600e-08
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	1.672e-06	9.478e-07	2.984e-07	4.190e-08

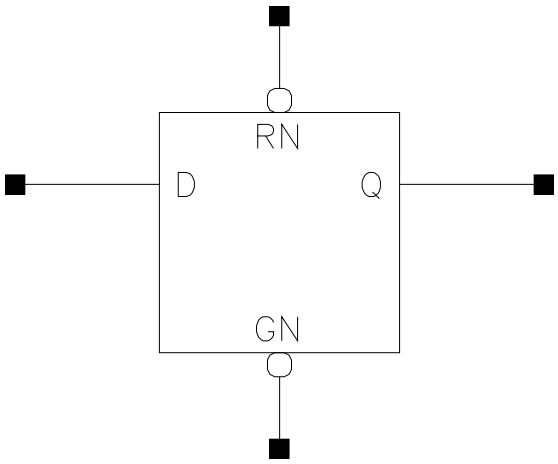
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	7.470e-07	1.500e-06	3.167e-07	-4.971e-07
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	3.385e-06	3.947e-07	9.880e-08	-2.107e-07
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	9.800e-07	6.250e-07	2.400e-07	-2.000e-09
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	8.770e-07	4.940e-07	1.116e-06	4.440e-08
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	1.026e-06	6.380e-07	2.290e-07	1.030e-07
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	7.690e-07	5.760e-07	1.120e-07	-2.080e-07
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	6.560e-07	-9.290e-07	-3.710e-07	-6.800e-07
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	2.669e-06	2.020e-07	-4.264e-06	-4.820e-07
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	-8.100e-08	-1.960e-06	-2.706e-06	7.180e-07

CNLDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
D	0.0010	0.0011	0.0011	0.0012
GN	0.0021	0.0021	0.0022	0.0024
RN	0.0006	0.0006	0.0006	0.0006

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	X33_P4	X33_P0	X33_P4

D to Q ↓	0.0638	0.0734	0.6251	0.6840
D to Q ↑	0.0595	0.0676	0.9975	1.1054
GN to Q ↓	0.0582	0.0666	0.6258	0.6842
GN to Q ↑	0.0669	0.0760	0.9992	1.1062
RN to Q ↓	0.0782	0.0889	0.6552	0.7205
RN to Q ↑	0.0656	0.0741	0.9994	1.1066
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D to Q ↓	0.0884	0.1036	0.7713	0.8511
D to Q ↑	0.0803	0.0931	1.2798	1.4574
GN to Q ↓	0.0793	0.0922	0.7710	0.8517
GN to Q ↑	0.0900	0.1040	1.2807	1.4579
RN to Q ↓	0.1062	0.1245	0.8169	0.9063
RN to Q ↑	0.0875	0.1009	1.2813	1.4579

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X33_P0	X33_P4	X33_P10	X33_P16
D ↓	hold_rising to GN	-0.0216	-0.0287	-0.0382	-0.0504
D ↑	hold_rising to GN	-0.0215	-0.0264	-0.0386	-0.0488
D ↓	setup_rising to GN	0.0686	0.0780	0.0982	0.1150
D ↑	setup_rising to GN	0.0658	0.0731	0.0877	0.1030
GN ↓	min_pulse_width to GN	0.0734	0.0829	0.0982	0.1136
RN ↓	min_pulse_width to RN	0.0925	0.1067	0.1262	0.1480
RN ↑	recovery_rising to GN	0.0704	0.0801	0.0947	0.1097
RN ↑	removal_rising to GN	-0.0455	-0.0557	-0.0658	-0.0756

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X33_P0	2.721e-05	2.489e-09
X33_P4	8.926e-06	2.489e-09
X33_P10	2.824e-06	2.489e-09
X33_P16	1.351e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	1.035e-04	1.137e-04	9.012e-05	8.582e-05
GN (output stable)	1.301e-03	1.296e-03	1.329e-03	1.362e-03
RN (output stable)	7.515e-05	6.110e-05	4.368e-05	3.779e-05
D to Q	8.678e-03	8.417e-03	8.373e-03	8.525e-03
GN to Q	1.108e-02	1.083e-02	1.084e-02	1.106e-02
RN to Q	6.675e-03	6.415e-03	6.325e-03	6.392e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	-3.252e-07	-7.861e-07	-2.813e-06	-6.197e-06

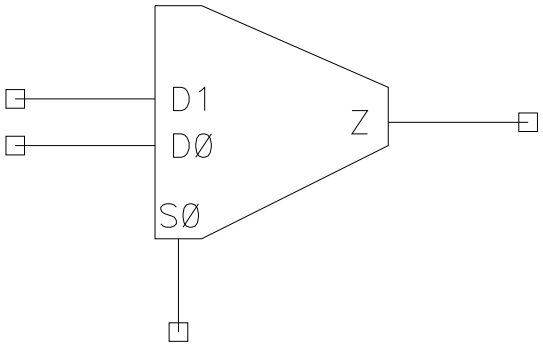
GN (output stable)	3.055e-06	7.752e-06	7.394e-06	5.446e-06
RN (output stable)	1.358e-07	1.794e-07	3.151e-07	6.932e-07
D to Q	-3.654e-07	-9.922e-07	-2.506e-06	-4.183e-06
GN to Q	7.316e-06	1.383e-05	1.989e-05	2.617e-05
RN to Q	-4.595e-06	-8.938e-06	-1.551e-05	-2.128e-05

CNMUX21

Cell Description

2:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320
X17_P4	1.200	1.360	1.6320
X17_P10	1.200	1.360	1.6320
X17_P16	1.200	1.360	1.6320
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0009	0.0010	0.0010	0.0011
D1	0.0009	0.0010	0.0010	0.0011
S0	0.0013	0.0014	0.0014	0.0015
	X33_P0	X33_P4	X33_P10	X33_P16
D0	0.0017	0.0018	0.0019	0.0020
D1	0.0017	0.0017	0.0018	0.0019
S0	0.0022	0.0023	0.0024	0.0026

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X17_P4	X17_P0	X17_P4

D0 to Z ↓	0.0418	0.0467	1.1447	1.2444
D0 to Z ↑	0.0328	0.0365	1.8885	2.0866
D1 to Z ↓	0.0415	0.0466	1.1430	1.2424
D1 to Z ↑	0.0309	0.0343	1.8890	2.0820
S0 to Z ↓	0.0386	0.0434	1.1402	1.2410
S0 to Z ↑	0.0372	0.0417	1.8872	2.0832
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0548	0.0625	1.3933	1.5298
D0 to Z ↑	0.0426	0.0483	2.4085	2.7351
D1 to Z ↓	0.0548	0.0628	1.3918	1.5287
D1 to Z ↑	0.0399	0.0452	2.4031	2.7315
S0 to Z ↓	0.0510	0.0583	1.3893	1.5271
S0 to Z ↑	0.0487	0.0553	2.4059	2.7329
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
D0 to Z ↓	0.0400	0.0451	0.5915	0.6443
D0 to Z ↑	0.0323	0.0364	0.9500	1.0501
D1 to Z ↓	0.0415	0.0470	0.5923	0.6444
D1 to Z ↑	0.0310	0.0347	0.9501	1.0479
S0 to Z ↓	0.0401	0.0453	0.5909	0.6429
S0 to Z ↑	0.0376	0.0423	0.9506	1.0497
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D0 to Z ↓	0.0530	0.0607	0.7215	0.7917
D0 to Z ↑	0.0425	0.0484	1.2129	1.3765
D1 to Z ↓	0.0551	0.0636	0.7221	0.7935
D1 to Z ↑	0.0402	0.0458	1.2107	1.3737
S0 to Z ↓	0.0531	0.0608	0.7211	0.7920
S0 to Z ↑	0.0492	0.0561	1.2110	1.3762

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P0	2.642e-05	1.536e-09
X17_P4	9.203e-06	1.536e-09
X17_P10	2.993e-06	1.536e-09
X17_P16	1.424e-06	1.536e-09
X33_P0	4.994e-05	2.489e-09
X33_P4	1.734e-05	2.489e-09
X33_P10	5.642e-06	2.489e-09
X33_P16	2.689e-06	2.489e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	1.014e-03	9.752e-04	9.547e-04	9.523e-04
D1 (output stable)	9.525e-04	9.079e-04	8.844e-04	8.798e-04
S0 (output stable)	1.017e-03	1.023e-03	1.050e-03	1.083e-03
D0 to Z	3.878e-03	3.792e-03	3.852e-03	3.944e-03
D1 to Z	3.766e-03	3.685e-03	3.743e-03	3.845e-03
S0 to Z	4.137e-03	4.069e-03	4.142e-03	4.252e-03
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	1.501e-03	1.410e-03	1.353e-03	1.335e-03
D1 (output stable)	1.577e-03	1.485e-03	1.429e-03	1.414e-03
S0 (output stable)	1.603e-03	1.608e-03	1.649e-03	1.710e-03

D0 to Z	7.446e-03	7.368e-03	7.463e-03	7.681e-03
D1 to Z	7.357e-03	7.274e-03	7.320e-03	7.584e-03
S0 to Z	8.132e-03	8.062e-03	8.179e-03	8.430e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

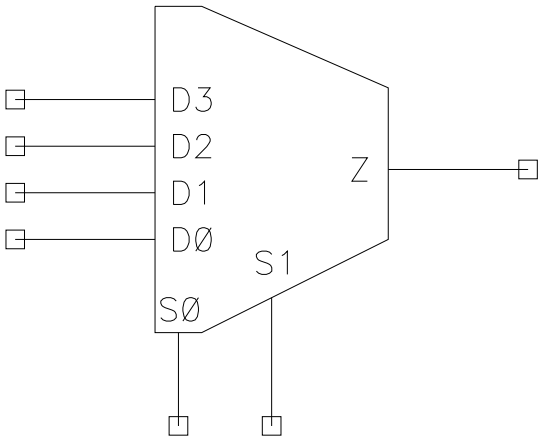
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	8.920e-08	-3.132e-07	-2.595e-07	-2.390e-07
D1 (output stable)	1.613e-07	-4.450e-09	-2.810e-07	-1.682e-07
S0 (output stable)	-3.075e-08	6.195e-08	-8.170e-08	-5.760e-08
D0 to Z	1.200e-09	-1.922e-07	-1.313e-07	-8.545e-08
D1 to Z	2.575e-08	-2.554e-07	-1.157e-07	-1.928e-07
S0 to Z	-5.185e-08	-1.077e-07	-1.365e-07	-2.115e-07
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	3.074e-07	2.083e-07	-4.927e-07	5.635e-08
D1 (output stable)	1.570e-07	4.910e-07	-5.835e-07	4.360e-07
S0 (output stable)	6.595e-08	-1.193e-07	1.100e-08	-1.674e-07
D0 to Z	-8.900e-08	-6.420e-07	-6.450e-07	-7.250e-07
D1 to Z	-2.370e-07	-6.385e-07	-6.905e-07	4.000e-08
S0 to Z	-2.755e-08	-2.263e-07	-1.796e-07	-6.090e-07

CNMUX41

Cell Description

4:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	2.400	2.176	5.2224
X17_P4	2.400	2.176	5.2224
X17_P10	2.400	2.176	5.2224
X17_P16	2.400	2.176	5.2224
X27_P0	2.400	2.312	5.5488
X27_P4	2.400	2.312	5.5488
X27_P10	2.400	2.312	5.5488
X27_P16	2.400	2.312	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0014	0.0014	0.0015	0.0015
D1	0.0013	0.0013	0.0014	0.0015
D2	0.0014	0.0014	0.0015	0.0015
D3	0.0014	0.0014	0.0015	0.0015
S0	0.0036	0.0037	0.0039	0.0041
S1	0.0020	0.0021	0.0023	0.0025

	X27_P0	X27_P4	X27_P10	X27_P16
D0	0.0013	0.0013	0.0014	0.0014
D1	0.0012	0.0012	0.0013	0.0014
D2	0.0012	0.0012	0.0013	0.0013
D3	0.0012	0.0012	0.0013	0.0013
S0	0.0031	0.0033	0.0034	0.0036
S1	0.0019	0.0020	0.0021	0.0022

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
D0 to Z ↓	0.0673	0.0772	1.1917	1.2979
D0 to Z ↑	0.0465	0.0523	1.9226	2.1204
D1 to Z ↓	0.0668	0.0766	1.1921	1.2970
D1 to Z ↑	0.0462	0.0519	1.9211	2.1213
D2 to Z ↓	0.0691	0.0792	1.1933	1.2989
D2 to Z ↑	0.0461	0.0517	1.9202	2.1181
D3 to Z ↓	0.0685	0.0786	1.1933	1.2981
D3 to Z ↑	0.0457	0.0513	1.9189	2.1161
S0 to Z ↓	0.0782	0.0896	1.1900	1.2953
S0 to Z ↑	0.0621	0.0701	1.9231	2.1230
S1 to Z ↓	0.0513	0.0587	1.1939	1.2988
S1 to Z ↑	0.0466	0.0523	1.9218	2.1220
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0918	0.1067	1.4508	1.5953
D0 to Z ↑	0.0610	0.0697	2.4482	2.7778
D1 to Z ↓	0.0911	0.1058	1.4508	1.5958
D1 to Z ↑	0.0605	0.0692	2.4480	2.7804
D2 to Z ↓	0.0944	0.1097	1.4533	1.5975
D2 to Z ↑	0.0602	0.0687	2.4448	2.7767
D3 to Z ↓	0.0937	0.1089	1.4531	1.5985
D3 to Z ↑	0.0598	0.0682	2.4434	2.7742
S0 to Z ↓	0.1070	0.1244	1.4493	1.5933
S0 to Z ↑	0.0825	0.0950	2.4491	2.7828
S1 to Z ↓	0.0695	0.0806	1.4531	1.5971
S1 to Z ↑	0.0606	0.0685	2.4481	2.7786
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0764	0.0876	0.7634	0.8320
D0 to Z ↑	0.0586	0.0661	1.2992	1.4341
D1 to Z ↓	0.0685	0.0783	0.7496	0.8164
D1 to Z ↑	0.0573	0.0646	1.2989	1.4339
D2 to Z ↓	0.0806	0.0927	0.7675	0.8374
D2 to Z ↑	0.0578	0.0652	1.2984	1.4335
D3 to Z ↓	0.0799	0.0919	0.7674	0.8373
D3 to Z ↑	0.0572	0.0644	1.2977	1.4319
S0 to Z ↓	0.0870	0.0996	0.7597	0.8283
S0 to Z ↑	0.0722	0.0817	1.3002	1.4352
S1 to Z ↓	0.0568	0.0650	0.7633	0.8326
S1 to Z ↑	0.0638	0.0719	1.2986	1.4330
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.1049	0.1221	0.9349	1.0303
D0 to Z ↑	0.0780	0.0897	1.6545	1.8794

D1 to Z ↓	0.0934	0.1082	0.9154	1.0080
D1 to Z ↑	0.0764	0.0879	1.6541	1.8793
D2 to Z ↓	0.1113	0.1298	0.9414	1.0394
D2 to Z ↑	0.0766	0.0880	1.6537	1.8783
D3 to Z ↓	0.1104	0.1287	0.9415	1.0385
D3 to Z ↑	0.0758	0.0871	1.6520	1.8756
S0 to Z ↓	0.1193	0.1387	0.9302	1.0251
S0 to Z ↑	0.0967	0.1116	1.6561	1.8805
S1 to Z ↓	0.0777	0.0904	0.9352	1.0299
S1 to Z ↑	0.0841	0.0957	1.6538	1.8783

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P0	3.487e-05	3.057e-09
X17_P4	1.237e-05	3.057e-09
X17_P10	4.153e-06	3.057e-09
X17_P16	2.049e-06	3.057e-09
X27_P0	3.641e-05	3.204e-09
X27_P4	1.286e-05	3.204e-09
X27_P10	4.286e-06	3.204e-09
X27_P16	2.098e-06	3.204e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	8.476e-05	6.703e-05	1.428e-04	1.723e-04
D1 (output stable)	7.211e-05	6.642e-05	1.232e-04	1.538e-04
D2 (output stable)	9.204e-05	7.507e-05	8.064e-05	9.560e-05
D3 (output stable)	1.006e-04	9.290e-05	1.384e-04	1.765e-04
S0 (output stable)	2.891e-03	2.996e-03	3.294e-03	3.605e-03
S1 (output stable)	2.476e-03	2.447e-03	2.456e-03	2.471e-03
D0 to Z	6.260e-03	6.305e-03	6.456e-03	6.655e-03
D1 to Z	6.239e-03	6.288e-03	6.456e-03	6.665e-03
D2 to Z	6.490e-03	6.540e-03	6.717e-03	6.915e-03
D3 to Z	6.401e-03	6.450e-03	6.638e-03	6.840e-03
S0 to Z	9.555e-03	9.751e-03	1.025e-02	1.072e-02
S1 to Z	6.846e-03	6.575e-03	6.611e-03	6.773e-03
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	7.705e-05	6.424e-05	1.405e-04	1.704e-04
D1 (output stable)	7.335e-05	6.871e-05	1.246e-04	1.536e-04
D2 (output stable)	8.249e-05	7.183e-05	7.776e-05	9.480e-05
D3 (output stable)	9.113e-05	9.000e-05	1.351e-04	1.700e-04
S0 (output stable)	2.689e-03	2.783e-03	3.066e-03	3.340e-03
S1 (output stable)	2.252e-03	2.226e-03	2.229e-03	2.236e-03
D0 to Z	7.501e-03	7.365e-03	7.436e-03	7.603e-03
D1 to Z	7.360e-03	7.258e-03	7.364e-03	7.550e-03
D2 to Z	7.648e-03	7.532e-03	7.597e-03	7.761e-03
D3 to Z	7.554e-03	7.437e-03	7.511e-03	7.684e-03
S0 to Z	1.046e-02	1.047e-02	1.085e-02	1.125e-02
S1 to Z	7.919e-03	7.512e-03	7.471e-03	7.636e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

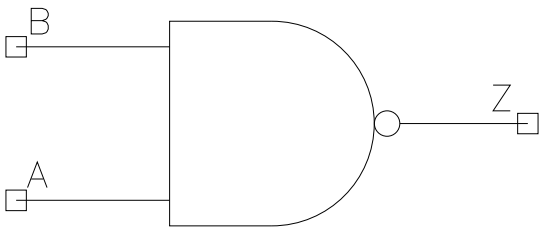
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	1.309e-05	1.727e-05	-2.511e-06	-8.998e-06
D1 (output stable)	8.878e-06	1.243e-05	2.445e-07	-7.224e-06
D2 (output stable)	1.301e-05	1.708e-05	9.545e-06	8.206e-07
D3 (output stable)	1.332e-05	1.733e-05	2.595e-06	-8.113e-06
S0 (output stable)	-7.426e-07	-1.174e-05	-4.775e-05	-7.328e-05
S1 (output stable)	1.031e-04	1.398e-04	9.319e-05	6.002e-05
D0 to Z	1.270e-06	1.058e-06	-5.407e-06	-1.110e-05
D1 to Z	2.505e-06	2.994e-06	-5.779e-06	-1.238e-05
D2 to Z	1.927e-06	1.642e-06	-7.088e-06	-1.323e-05
D3 to Z	2.633e-06	3.637e-06	-5.314e-06	-1.162e-05
S0 to Z	2.564e-06	-6.252e-06	-4.068e-05	-6.089e-05
S1 to Z	8.470e-05	1.360e-04	1.241e-04	8.696e-05
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	1.415e-05	1.574e-05	-3.272e-06	-9.439e-06
D1 (output stable)	8.555e-06	1.143e-05	-6.495e-07	-7.920e-06
D2 (output stable)	1.342e-05	1.442e-05	6.714e-06	-1.453e-06
D3 (output stable)	1.393e-05	1.441e-05	-1.083e-06	-1.017e-05
S0 (output stable)	-1.654e-06	-1.460e-05	-5.134e-05	-7.392e-05
S1 (output stable)	1.076e-04	1.344e-04	8.594e-05	5.597e-05
D0 to Z	1.363e-06	7.674e-07	-5.907e-06	-1.141e-05
D1 to Z	2.692e-06	1.663e-06	-7.575e-06	-1.414e-05
D2 to Z	2.176e-06	1.500e-07	-8.663e-06	-1.447e-05
D3 to Z	3.483e-06	2.079e-06	-7.016e-06	-1.287e-05
S0 to Z	1.945e-06	-8.057e-06	-4.317e-05	-6.070e-05
S1 to Z	8.736e-05	1.342e-04	1.198e-04	8.236e-05

CNNAND2

Cell Description

2 input NAND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X33_P0	1.200	1.224	1.4688
X33_P4	1.200	1.224	1.4688
X33_P10	1.200	1.224	1.4688
X33_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0017	0.0018	0.0019	0.0020
B	0.0016	0.0017	0.0018	0.0018
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0007	0.0007	0.0008	0.0008
B	0.0007	0.0007	0.0007	0.0008

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0108	0.0122	1.6439	1.7882
A to Z ↑	0.0174	0.0195	1.9478	2.1480
B to Z ↓	0.0095	0.0107	1.6642	1.8126
B to Z ↑	0.0142	0.0158	1.9605	2.1600
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0141	0.0157	2.0084	2.2087
A to Z ↑	0.0224	0.0250	2.4760	2.8076
B to Z ↓	0.0124	0.0138	2.0313	2.2352
B to Z ↑	0.0181	0.0200	2.4929	2.8267
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0432	0.0489	0.5781	0.6287
A to Z ↑	0.0493	0.0557	0.9460	1.0442
B to Z ↓	0.0441	0.0498	0.5774	0.6289
B to Z ↑	0.0480	0.0541	0.9463	1.0462
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0583	0.0677	0.7029	0.7718
A to Z ↑	0.0659	0.0759	1.2040	1.3691
B to Z ↓	0.0594	0.0687	0.7024	0.7721
B to Z ↑	0.0641	0.0738	1.2065	1.3700

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X15_P0	1.141e-05	1.179e-09
X15_P4	4.147e-06	1.179e-09
X15_P10	1.407e-06	1.179e-09
X15_P16	6.894e-07	1.179e-09
X33_P0	2.951e-05	1.417e-09
X33_P4	1.040e-05	1.417e-09
X33_P10	3.400e-06	1.417e-09
X33_P16	1.618e-06	1.417e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.116e-04	1.038e-04	9.244e-05	8.461e-05
B (output stable)	1.920e-04	2.623e-04	3.081e-04	3.199e-04
A to Z	1.924e-03	1.906e-03	1.942e-03	1.995e-03
B to Z	1.360e-03	1.260e-03	1.206e-03	1.189e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.787e-05	1.657e-05	1.520e-05	1.422e-05
B (output stable)	2.129e-05	2.494e-05	3.519e-05	3.831e-05
A to Z	6.591e-03	6.630e-03	6.955e-03	7.269e-03
B to Z	6.485e-03	6.508e-03	6.821e-03	7.120e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

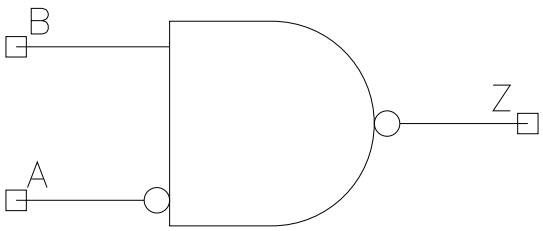
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	2.030e-08	5.600e-09	-4.140e-08	-1.227e-07
B (output stable)	-8.600e-09	-3.640e-08	-1.113e-07	-1.596e-07
A to Z	3.341e-07	2.153e-07	-2.785e-07	1.105e-07
B to Z	3.950e-07	7.464e-07	-2.506e-07	-1.625e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	5.225e-08	4.801e-08	3.060e-08	1.856e-08
B (output stable)	4.740e-08	3.080e-08	1.510e-08	1.620e-08
A to Z	-3.457e-07	-2.539e-07	-5.158e-07	-4.734e-07
B to Z	-3.205e-07	-5.498e-07	-4.141e-07	-5.912e-07

CNNAND2A

Cell Description

2 input NAND with A input inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0008	0.0008	0.0008	0.0008
B	0.0009	0.0009	0.0010	0.0010
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0011	0.0011	0.0012	0.0012
B	0.0008	0.0008	0.0009	0.0009

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0396	0.0451	1.1269	1.2273
A to Z ↑	0.0291	0.0325	1.8856	2.0841
B to Z ↓	0.0424	0.0482	1.1246	1.2264
B to Z ↑	0.0396	0.0446	1.8862	2.0825
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**

A to Z ↓	0.0541	0.0618	1.3748	1.5126
A to Z ↑	0.0379	0.0424	2.4069	2.7373
B to Z ↓	0.0584	0.0671	1.3761	1.5099
B to Z ↑	0.0526	0.0595	2.4052	2.7328
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0433	0.0493	0.6810	0.7435
A to Z ↑	0.0332	0.0372	1.2341	1.3678
B to Z ↓	0.0442	0.0504	0.6801	0.7426
B to Z ↑	0.0438	0.0496	1.2313	1.3635
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0588	0.0678	0.8356	0.9213
A to Z ↑	0.0435	0.0492	1.5844	1.8012
B to Z ↓	0.0605	0.0701	0.8354	0.9198
B to Z ↑	0.0584	0.0671	1.5774	1.7951

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X17_P0	1.977e-05	1.179e-09
X17_P4	7.109e-06	1.179e-09
X17_P10	2.352e-06	1.179e-09
X17_P16	1.124e-06	1.179e-09
X27_P0	2.776e-05	1.655e-09
X27_P4	9.967e-06	1.655e-09
X27_P10	3.273e-06	1.655e-09
X27_P16	1.551e-06	1.656e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	4.034e-05	4.025e-05	4.101e-05	6.482e-05
B (output stable)	9.379e-04	9.069e-04	9.053e-04	9.233e-04
A to Z	3.077e-03	3.065e-03	3.182e-03	3.243e-03
B to Z	4.143e-03	4.133e-03	4.304e-03	4.399e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.182e-04	1.150e-04	2.197e-04	2.887e-04
B (output stable)	1.091e-03	1.058e-03	1.049e-03	1.096e-03
A to Z	5.090e-03	5.043e-03	5.201e-03	5.362e-03
B to Z	5.962e-03	5.955e-03	6.148e-03	6.364e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

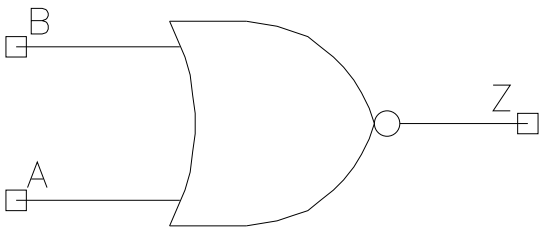
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	1.270e-07	-3.366e-07	-2.549e-06	-1.206e-05
B (output stable)	4.611e-06	1.833e-05	2.087e-05	1.914e-05
A to Z	-1.390e-08	-1.438e-07	-4.927e-07	-1.620e-06
B to Z	-1.460e-08	-1.722e-07	-2.849e-07	-2.466e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	-8.057e-08	-3.814e-06	-4.312e-05	-6.367e-05
B (output stable)	4.530e-05	6.335e-05	5.953e-05	5.899e-05
A to Z	8.803e-07	5.467e-07	-3.238e-06	-6.886e-06
B to Z	-1.907e-07	-3.780e-07	-2.547e-07	-4.224e-07

CNNOR2

Cell Description

2 input NOR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	0.952	1.1424
X14_P4	1.200	0.952	1.1424
X14_P10	1.200	0.952	1.1424
X14_P16	1.200	0.952	1.1424
X33_P0	1.200	1.496	1.7952
X33_P4	1.200	1.496	1.7952
X33_P10	1.200	1.496	1.7952
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0020	0.0020	0.0021	0.0022
B	0.0018	0.0018	0.0019	0.0020
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0008	0.0008	0.0009	0.0009
B	0.0008	0.0008	0.0009	0.0009

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0121	0.0136	1.2681	1.3726
A to Z ↑	0.0182	0.0208	2.8066	3.1122
B to Z ↓	0.0094	0.0105	1.2799	1.3876
B to Z ↑	0.0144	0.0162	2.8274	3.1355
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**

A to Z ↓	0.0156	0.0174	1.5262	1.6657
A to Z ↑	0.0240	0.0270	3.5773	4.0359
B to Z ↓	0.0122	0.0134	1.5418	1.6828
B to Z ↑	0.0189	0.0211	3.6030	4.0638
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0465	0.0528	0.5705	0.6214
A to Z ↑	0.0497	0.0567	0.9429	1.0411
B to Z ↓	0.0443	0.0506	0.5704	0.6199
B to Z ↑	0.0487	0.0555	0.9428	1.0401
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0624	0.0725	0.6954	0.7630
A to Z ↑	0.0670	0.0779	1.2010	1.3628
B to Z ↓	0.0598	0.0699	0.6950	0.7622
B to Z ↑	0.0652	0.0758	1.2014	1.3628

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X14_P0	1.174e-05	1.179e-09
X14_P4	3.841e-06	1.179e-09
X14_P10	1.204e-06	1.179e-09
X14_P16	5.703e-07	1.179e-09
X33_P0	3.397e-05	1.655e-09
X33_P4	1.163e-05	1.655e-09
X33_P10	3.731e-06	1.655e-09
X33_P16	1.768e-06	1.655e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	1.692e-04	1.768e-04	1.794e-04	1.858e-04
B (output stable)	2.176e-04	1.133e-04	6.625e-05	5.861e-05
A to Z	2.285e-03	2.281e-03	2.311e-03	2.389e-03
B to Z	1.373e-03	1.268e-03	1.212e-03	1.196e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	4.101e-05	4.156e-05	4.305e-05	4.395e-05
B (output stable)	5.099e-05	2.284e-05	9.598e-06	6.193e-06
A to Z	7.329e-03	7.437e-03	7.624e-03	8.010e-03
B to Z	7.089e-03	7.190e-03	7.343e-03	7.730e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

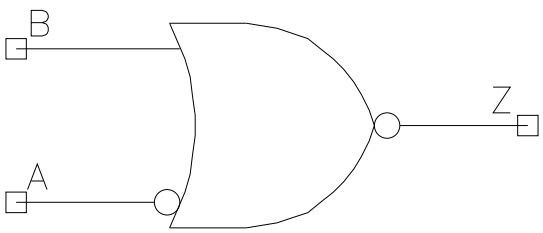
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	2.947e-07	-2.650e-06	-6.880e-06	-9.562e-06
B (output stable)	3.516e-05	6.894e-05	6.767e-05	6.097e-05
A to Z	1.295e-06	1.745e-06	-2.888e-06	-5.121e-06
B to Z	3.144e-07	-5.192e-07	-1.509e-07	-6.343e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.311e-07	-3.513e-07	-1.883e-06	-2.729e-06
B (output stable)	4.793e-06	1.830e-05	2.115e-05	1.947e-05
A to Z	-1.000e-09	-2.780e-07	-6.910e-07	-1.958e-06
B to Z	-1.140e-07	-3.760e-07	-5.070e-07	-5.976e-07

CNNOR2A

Cell Description

2 input NOR with A input Inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	1.224	1.4688
X15_P4	1.200	1.224	1.4688
X15_P10	1.200	1.224	1.4688
X15_P16	1.200	1.224	1.4688
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0012	0.0012	0.0013	0.0013
B	0.0008	0.0008	0.0009	0.0009
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0014	0.0014	0.0015	0.0016
B	0.0008	0.0009	0.0009	0.0010

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0384	0.0431	1.3985	1.5249
A to Z ↑	0.0277	0.0313	1.8893	2.0883
B to Z ↓	0.0375	0.0426	1.3912	1.5173
B to Z ↑	0.0389	0.0440	1.8866	2.0844
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0504	0.0575	1.7105	1.8780
A to Z ↑	0.0367	0.0419	2.4116	2.7389
B to Z ↓	0.0506	0.0585	1.7023	1.8733
B to Z ↑	0.0516	0.0589	2.4111	2.7410
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0330	0.0371	0.7932	0.8654
A to Z ↑	0.0290	0.0324	1.0054	1.1100
B to Z ↓	0.0376	0.0428	0.7933	0.8654
B to Z ↑	0.0417	0.0473	1.0029	1.1102
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0435	0.0493	0.9717	1.0688
A to Z ↑	0.0379	0.0430	1.2816	1.4558
B to Z ↓	0.0509	0.0588	0.9723	1.0701
B to Z ↑	0.0554	0.0633	1.2812	1.4560

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X15_P0	1.763e-05	1.417e-09
X15_P4	5.751e-06	1.417e-09
X15_P10	1.797e-06	1.417e-09
X15_P16	8.471e-07	1.417e-09
X27_P0	2.706e-05	1.655e-09
X27_P4	8.589e-06	1.655e-09
X27_P10	2.637e-06	1.656e-09
X27_P16	1.236e-06	1.656e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	6.884e-05	6.197e-05	5.290e-05	4.714e-05
B (output stable)	1.094e-03	1.114e-03	1.149e-03	1.181e-03
A to Z	3.270e-03	3.291e-03	3.391e-03	3.510e-03
B to Z	4.169e-03	4.203e-03	4.343e-03	4.501e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	9.617e-05	8.765e-05	7.670e-05	6.899e-05
B (output stable)	1.249e-03	1.308e-03	1.368e-03	1.432e-03
A to Z	5.224e-03	5.212e-03	5.390e-03	5.543e-03
B to Z	6.345e-03	6.389e-03	6.628e-03	6.872e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

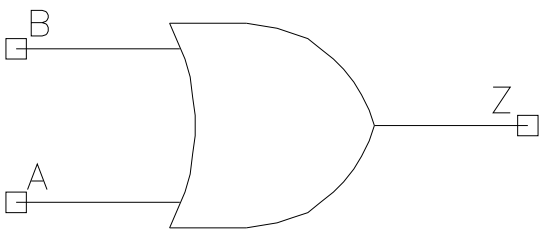
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	6.060e-08	7.330e-08	1.077e-07	1.699e-07
B (output stable)	-3.656e-07	-1.066e-06	-1.662e-06	-2.230e-06
A to Z	-2.187e-07	-9.090e-08	-2.387e-07	-1.394e-07
B to Z	2.843e-07	-5.200e-09	-5.710e-08	-2.789e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	4.110e-08	2.680e-08	-9.000e-10	-1.830e-08
B (output stable)	1.286e-07	-6.240e-08	-9.260e-08	-1.939e-07
A to Z	1.239e-07	-2.841e-07	-5.692e-07	-2.126e-07
B to Z	-2.029e-07	-6.688e-07	-5.060e-07	-5.486e-07

CNOR2

Cell Description

2 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X20_P0	1.200	1.360	1.6320
X20_P4	1.200	1.360	1.6320
X20_P10	1.200	1.360	1.6320
X20_P16	1.200	1.360	1.6320
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320
X37_P0	1.200	1.632	1.9584
X37_P4	1.200	1.632	1.9584
X37_P10	1.200	1.632	1.9584
X37_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0015	0.0015	0.0016	0.0017
B	0.0013	0.0014	0.0015	0.0015
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0022	0.0023	0.0024	0.0025
B	0.0023	0.0024	0.0025	0.0026
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0015	0.0016	0.0016	0.0017

B	0.0015	0.0016	0.0016	0.0017
	X37_P0	X37_P4	X37_P10	X37_P16
A	0.0022	0.0023	0.0024	0.0025
B	0.0022	0.0023	0.0024	0.0025

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0331	0.0374	1.2729	1.3863
A to Z ↑	0.0233	0.0259	1.9777	2.1868
B to Z ↓	0.0303	0.0342	1.2736	1.3875
B to Z ↑	0.0213	0.0236	1.9768	2.1826
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0444	0.0506	1.5527	1.7077
A to Z ↑	0.0300	0.0334	2.5322	2.8803
B to Z ↓	0.0405	0.0459	1.5564	1.7080
B to Z ↑	0.0275	0.0307	2.5266	2.8759
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0306	0.0351	0.9925	1.0814
A to Z ↑	0.0234	0.0262	1.3727	1.5172
B to Z ↓	0.0279	0.0319	0.9927	1.0822
B to Z ↑	0.0209	0.0234	1.3709	1.5153
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0410	0.0468	1.2120	1.3345
A to Z ↑	0.0300	0.0335	1.7540	1.9925
B to Z ↓	0.0374	0.0426	1.2145	1.3355
B to Z ↑	0.0269	0.0301	1.7500	1.9915
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0396	0.0451	0.5768	0.6278
A to Z ↑	0.0277	0.0309	0.9299	1.0298
B to Z ↓	0.0368	0.0418	0.5768	0.6273
B to Z ↑	0.0254	0.0284	0.9303	1.0275
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0533	0.0615	0.7033	0.7730
A to Z ↑	0.0356	0.0401	1.1883	1.3532
B to Z ↓	0.0493	0.0565	0.7037	0.7734
B to Z ↑	0.0328	0.0369	1.1861	1.3505
	X37_P0	**X37_P4**	**X37_P0**	**X37_P4**
A to Z ↓	0.0357	0.0410	0.5566	0.6065
A to Z ↑	0.0263	0.0295	0.7584	0.8370
B to Z ↓	0.0335	0.0385	0.5569	0.6073
B to Z ↑	0.0241	0.0270	0.7569	0.8365
	X37_P10	**X37_P16**	**X37_P10**	**X37_P16**
A to Z ↓	0.0483	0.0554	0.6811	0.7492
A to Z ↑	0.0338	0.0379	0.9655	1.0976
B to Z ↓	0.0452	0.0518	0.6809	0.7498
B to Z ↑	0.0310	0.0348	0.9641	1.0946

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X15_P0	1.633e-05	1.179e-09

X15_P4	5.793e-06	1.179e-09
X15_P10	1.892e-06	1.179e-09
X15_P16	8.982e-07	1.179e-09
X20_P0	2.501e-05	1.536e-09
X20_P4	8.726e-06	1.536e-09
X20_P10	2.827e-06	1.536e-09
X20_P16	1.340e-06	1.536e-09
X33_P0	2.844e-05	1.536e-09
X33_P4	1.040e-05	1.536e-09
X33_P10	3.481e-06	1.536e-09
X33_P16	1.671e-06	1.536e-09
X37_P0	3.438e-05	1.775e-09
X37_P4	1.218e-05	1.775e-09
X37_P10	3.975e-06	1.775e-09
X37_P16	1.884e-06	1.775e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	9.691e-05	9.904e-05	1.029e-04	1.056e-04
B (output stable)	1.282e-04	7.226e-05	4.986e-05	4.278e-05
A to Z	3.373e-03	3.352e-03	3.493e-03	3.596e-03
B to Z	2.827e-03	2.763e-03	2.856e-03	2.916e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	1.717e-04	1.756e-04	1.794e-04	1.869e-04
B (output stable)	2.225e-04	1.160e-04	6.533e-05	5.888e-05
A to Z	5.142e-03	5.212e-03	5.349e-03	5.556e-03
B to Z	4.195e-03	4.205e-03	4.283e-03	4.413e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.284e-04	1.299e-04	1.353e-04	1.365e-04
B (output stable)	1.872e-04	1.118e-04	8.333e-05	7.492e-05
A to Z	6.120e-03	6.105e-03	6.242e-03	6.485e-03
B to Z	5.404e-03	5.342e-03	5.424e-03	5.610e-03
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	1.722e-04	1.759e-04	1.815e-04	1.859e-04
B (output stable)	2.238e-04	1.164e-04	7.044e-05	5.899e-05
A to Z	7.304e-03	7.419e-03	7.595e-03	7.858e-03
B to Z	6.391e-03	6.433e-03	6.539e-03	6.753e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.357e-07	-1.623e-06	-4.408e-06	-5.864e-06
B (output stable)	2.329e-05	4.057e-05	4.103e-05	3.724e-05
A to Z	4.939e-07	3.522e-07	-1.506e-06	-3.185e-06
B to Z	-2.195e-07	-1.879e-07	-1.636e-07	-3.916e-07
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.599e-07	-2.575e-06	-7.091e-06	-9.916e-06
B (output stable)	3.709e-05	7.096e-05	6.770e-05	6.120e-05
A to Z	8.910e-07	6.400e-07	-3.157e-06	-5.518e-06
B to Z	-4.239e-07	-9.357e-07	-4.048e-07	-9.213e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	5.132e-08	-3.595e-06	-9.008e-06	-1.167e-05

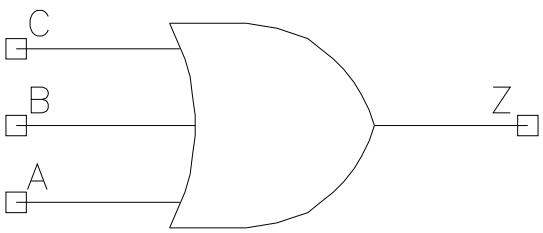
B (output stable)	5.118e-05	7.915e-05	8.068e-05	7.468e-05
A to Z	7.673e-07	8.573e-07	-3.538e-06	-7.577e-06
B to Z	-4.270e-07	-2.727e-07	-4.633e-07	-6.466e-07
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	2.533e-07	-2.600e-06	-7.164e-06	-9.898e-06
B (output stable)	3.753e-05	7.138e-05	6.808e-05	6.040e-05
A to Z	2.760e-08	1.129e-06	-2.738e-06	-5.863e-06
B to Z	-3.229e-07	-2.296e-07	-7.918e-07	-1.123e-06

CNOR3

Cell Description

3 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	1.360	1.6320
X14_P4	1.200	1.360	1.6320
X14_P10	1.200	1.360	1.6320
X14_P16	1.200	1.360	1.6320
X20_P0	1.200	1.632	1.9584
X20_P4	1.200	1.632	1.9584
X20_P10	1.200	1.632	1.9584
X20_P16	1.200	1.632	1.9584
X27_P0	1.200	2.040	2.4480
X27_P4	1.200	2.040	2.4480
X27_P10	1.200	2.040	2.4480
X27_P16	1.200	2.040	2.4480

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0008	0.0009	0.0009	0.0009
B	0.0008	0.0008	0.0009	0.0009
C	0.0008	0.0009	0.0009	0.0009
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0008	0.0008	0.0009	0.0009
B	0.0008	0.0008	0.0009	0.0009
C	0.0008	0.0009	0.0009	0.0009
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0011	0.0011	0.0011	0.0012
B	0.0011	0.0011	0.0011	0.0011

C	0.0009	0.0009	0.0009	0.0009

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0598	0.0684	1.3976	1.5264
A to Z ↑	0.0473	0.0537	1.9854	2.1966
B to Z ↓	0.0612	0.0701	1.3975	1.5266
B to Z ↑	0.0493	0.0560	1.9879	2.1958
C to Z ↓	0.0543	0.0618	1.3981	1.5255
C to Z ↑	0.0443	0.0504	1.9850	2.1922
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0813	0.0941	1.7123	1.8835
A to Z ↑	0.0633	0.0728	2.5372	2.8831
B to Z ↓	0.0835	0.0968	1.7121	1.8843
B to Z ↑	0.0659	0.0756	2.5351	2.8820
C to Z ↓	0.0730	0.0841	1.7134	1.8842
C to Z ↑	0.0594	0.0682	2.5330	2.8774
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0596	0.0676	1.0295	1.1219
A to Z ↑	0.0515	0.0584	1.3997	1.5459
B to Z ↓	0.0610	0.0693	1.0298	1.1215
B to Z ↑	0.0533	0.0603	1.3996	1.5457
C to Z ↓	0.0529	0.0597	1.0293	1.1217
C to Z ↑	0.0497	0.0562	1.4006	1.5473
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0804	0.0930	1.2571	1.3839
A to Z ↑	0.0695	0.0804	1.7853	2.0277
B to Z ↓	0.0827	0.0958	1.2567	1.3828
B to Z ↑	0.0717	0.0828	1.7828	2.0289
C to Z ↓	0.0708	0.0815	1.2576	1.3831
C to Z ↑	0.0669	0.0773	1.7861	2.0272
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0473	0.0541	0.9542	1.0421
A to Z ↑	0.0450	0.0507	1.1663	1.2918
B to Z ↓	0.0455	0.0519	0.9548	1.0435
B to Z ↑	0.0423	0.0475	1.1639	1.2907
C to Z ↓	0.0388	0.0436	0.9466	1.0332
C to Z ↑	0.0354	0.0396	0.9427	1.0445
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0643	0.0740	1.1716	1.2925
A to Z ↑	0.0594	0.0676	1.4940	1.7013
B to Z ↓	0.0615	0.0708	1.1705	1.2942
B to Z ↑	0.0554	0.0631	1.4923	1.6983
C to Z ↓	0.0507	0.0575	1.1608	1.2825
C to Z ↑	0.0458	0.0516	1.2063	1.3695

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X14_P0	2.384e-05	1.536e-09
X14_P4	8.540e-06	1.536e-09

X14_P10	2.828e-06	1.536e-09
X14_P16	1.355e-06	1.536e-09
X20_P0	2.899e-05	1.799e-09
X20_P4	1.048e-05	1.799e-09
X20_P10	3.480e-06	1.799e-09
X20_P16	1.665e-06	1.799e-09
X27_P0	2.530e-05	2.205e-09
X27_P4	9.265e-06	2.205e-09
X27_P10	3.157e-06	2.205e-09
X27_P16	1.543e-06	2.205e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	3.942e-04	3.775e-04	3.814e-04	3.939e-04
B (output stable)	4.662e-04	4.768e-04	4.987e-04	5.220e-04
C (output stable)	9.274e-04	9.218e-04	9.506e-04	9.798e-04
A to Z	4.867e-03	4.960e-03	5.133e-03	5.325e-03
B to Z	5.098e-03	5.215e-03	5.412e-03	5.622e-03
C to Z	4.815e-03	4.894e-03	5.051e-03	5.227e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	3.815e-04	3.644e-04	3.676e-04	3.788e-04
B (output stable)	4.506e-04	4.597e-04	4.803e-04	5.019e-04
C (output stable)	8.652e-04	8.540e-04	8.785e-04	9.037e-04
A to Z	5.910e-03	5.940e-03	6.163e-03	6.393e-03
B to Z	6.132e-03	6.186e-03	6.433e-03	6.680e-03
C to Z	5.833e-03	5.852e-03	6.067e-03	6.280e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.157e-03	1.196e-03	1.260e-03	1.322e-03
B (output stable)	1.029e-03	1.031e-03	1.072e-03	1.126e-03
C (output stable)	2.537e-03	2.715e-03	2.872e-03	3.017e-03
A to Z	7.091e-03	7.207e-03	7.501e-03	7.780e-03
B to Z	6.694e-03	6.786e-03	7.053e-03	7.323e-03
C to Z	5.810e-03	5.802e-03	5.890e-03	6.054e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	3.109e-06	1.208e-05	1.350e-05	6.472e-06
B (output stable)	1.254e-07	-1.906e-07	-1.335e-06	-2.306e-06
C (output stable)	1.445e-07	4.030e-08	1.196e-07	1.019e-07
A to Z	-9.253e-08	-3.078e-07	-2.733e-07	-3.506e-07
B to Z	2.480e-08	-1.838e-07	-4.395e-07	-1.635e-06
C to Z	2.207e-07	-1.529e-07	-2.026e-07	-2.176e-07
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	3.140e-06	1.161e-05	1.283e-05	6.027e-06
B (output stable)	1.055e-07	-2.269e-07	-1.309e-06	-2.225e-06
C (output stable)	-1.193e-08	3.650e-08	1.600e-09	8.947e-08
A to Z	-2.111e-07	-1.389e-07	-2.469e-07	-2.088e-07
B to Z	-2.083e-07	-1.331e-07	-5.346e-07	-1.645e-06
C to Z	2.800e-08	-1.133e-07	-2.611e-07	-1.984e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.234e-07	-5.391e-07	-2.654e-06	-4.173e-06

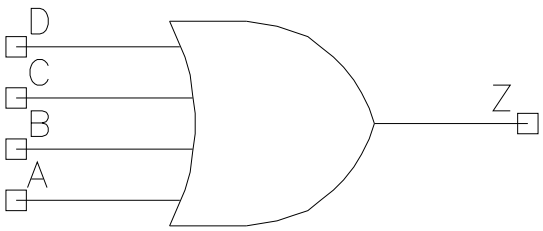
B (output stable)	8.543e-06	2.045e-05	2.005e-05	1.286e-05
C (output stable)	-2.810e-07	-1.169e-06	-2.149e-06	-2.571e-06
A to Z	-3.734e-07	-1.178e-07	-1.379e-06	-3.360e-06
B to Z	-5.320e-07	-6.120e-07	-7.490e-07	-5.500e-07
C to Z	1.030e-07	-6.100e-08	-1.970e-07	-1.140e-07

CNOR4

Cell Description

4 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X20_P4	1.200	2.176	2.6112
X20_P10	1.200	2.176	2.6112
X20_P16	1.200	2.176	2.6112
X27_P0	1.200	2.312	2.7744
X27_P4	1.200	2.312	2.7744
X27_P10	1.200	2.312	2.7744
X27_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0012	0.0012	0.0013	0.0013
B	0.0013	0.0013	0.0014	0.0014
C	0.0012	0.0013	0.0013	0.0013
D	0.0013	0.0013	0.0014	0.0014
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0012	0.0012	0.0012	0.0013
B	0.0013	0.0013	0.0013	0.0014
C	0.0012	0.0013	0.0013	0.0013
D	0.0014	0.0014	0.0015	0.0015

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0436	0.0500	1.0803	1.1769
A to Z ↑	0.0359	0.0404	1.6456	1.8218
B to Z ↓	0.0403	0.0463	1.0808	1.1765
B to Z ↑	0.0336	0.0379	1.6447	1.8196
C to Z ↓	0.0414	0.0470	1.0781	1.1737
C to Z ↑	0.0342	0.0381	1.6330	1.8121
D to Z ↓	0.0388	0.0440	1.0774	1.1745
D to Z ↑	0.0322	0.0357	1.6317	1.8118
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0589	0.0678	1.3241	1.4642
A to Z ↑	0.0469	0.0536	2.1100	2.4048
B to Z ↓	0.0545	0.0629	1.3243	1.4643
B to Z ↑	0.0439	0.0503	2.1100	2.3993
C to Z ↓	0.0559	0.0629	1.3206	1.4555
C to Z ↑	0.0442	0.0491	2.1013	2.3924
D to Z ↓	0.0524	0.0589	1.3205	1.4565
D to Z ↑	0.0415	0.0461	2.0997	2.3903
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0475	0.0542	0.8895	0.9701
A to Z ↑	0.0380	0.0425	1.2323	1.3654
B to Z ↓	0.0444	0.0507	0.8903	0.9702
B to Z ↑	0.0358	0.0401	1.2307	1.3639
C to Z ↓	0.0426	0.0489	0.8857	0.9653
C to Z ↑	0.0343	0.0385	1.2243	1.3585
D to Z ↓	0.0400	0.0459	0.8854	0.9644
D to Z ↑	0.0317	0.0357	1.2236	1.3570
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0641	0.0735	1.0922	1.2086
A to Z ↑	0.0495	0.0560	1.5804	1.8008
B to Z ↓	0.0601	0.0688	1.0918	1.2090
B to Z ↑	0.0469	0.0530	1.5803	1.7983
C to Z ↓	0.0576	0.0663	1.0869	1.2009
C to Z ↑	0.0443	0.0501	1.5734	1.7944
D to Z ↓	0.0541	0.0622	1.0870	1.1979
D to Z ↑	0.0411	0.0464	1.5725	1.7900

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X20_P0	2.358e-05	2.351e-09
X20_P4	8.742e-06	2.351e-09
X20_P10	3.024e-06	2.351e-09
X20_P16	1.497e-06	2.351e-09
X27_P0	2.610e-05	2.475e-09
X27_P4	9.755e-06	2.475e-09
X27_P10	3.396e-06	2.475e-09
X27_P16	1.686e-06	2.475e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	1.308e-03	1.359e-03	1.415e-03	1.492e-03

B (output stable)	1.123e-03	1.135e-03	1.167e-03	1.233e-03
C (output stable)	1.269e-03	1.341e-03	1.437e-03	1.490e-03
D (output stable)	1.080e-03	1.108e-03	1.173e-03	1.200e-03
A to Z	6.066e-03	6.227e-03	6.487e-03	6.797e-03
B to Z	5.646e-03	5.771e-03	5.996e-03	6.290e-03
C to Z	5.511e-03	5.543e-03	5.741e-03	5.819e-03
D to Z	5.088e-03	5.078e-03	5.243e-03	5.298e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.519e-03	1.566e-03	1.647e-03	1.722e-03
B (output stable)	1.334e-03	1.346e-03	1.404e-03	1.466e-03
C (output stable)	1.311e-03	1.405e-03	1.500e-03	1.574e-03
D (output stable)	1.120e-03	1.173e-03	1.237e-03	1.281e-03
A to Z	7.138e-03	7.247e-03	7.548e-03	7.841e-03
B to Z	6.721e-03	6.801e-03	7.073e-03	7.346e-03
C to Z	6.075e-03	6.149e-03	6.269e-03	6.502e-03
D to Z	5.669e-03	5.710e-03	5.798e-03	6.006e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

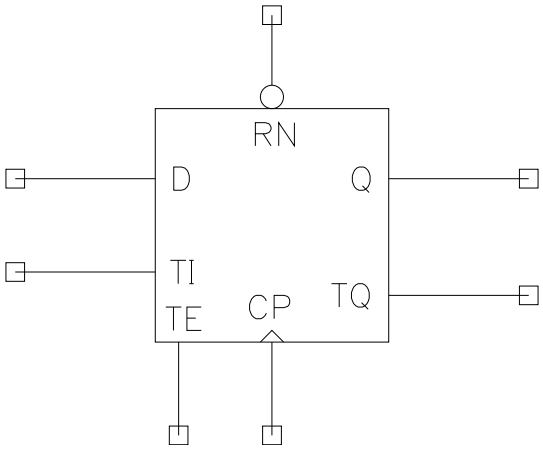
Pin Cycle (vdds)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.123e-07	-6.203e-07	-2.764e-06	-4.379e-06
B (output stable)	9.072e-06	1.906e-05	1.721e-05	1.082e-05
C (output stable)	7.456e-08	-1.147e-06	-4.485e-06	-8.839e-06
D (output stable)	8.192e-06	1.900e-05	1.889e-05	1.451e-05
A to Z	-8.960e-08	-2.322e-07	-1.329e-06	-3.172e-06
B to Z	-5.840e-07	-5.710e-07	-5.242e-07	-4.937e-07
C to Z	-2.010e-08	-7.960e-08	-1.155e-06	-2.649e-06
D to Z	-1.747e-07	-3.092e-07	-2.906e-07	-3.394e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.675e-07	-6.710e-07	-2.836e-06	-4.429e-06
B (output stable)	9.050e-06	1.896e-05	1.715e-05	1.080e-05
C (output stable)	1.197e-07	-1.078e-06	-4.439e-06	-8.739e-06
D (output stable)	8.392e-06	1.940e-05	1.908e-05	1.462e-05
A to Z	-7.190e-08	-1.984e-07	-1.359e-06	-3.375e-06
B to Z	-6.190e-07	-5.370e-07	-4.820e-07	-4.019e-07
C to Z	3.632e-07	2.330e-08	-8.218e-07	-3.225e-06
D to Z	-1.200e-07	-2.580e-07	-2.130e-07	-6.509e-07

CNSDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.080	4.8960
X15_P4	1.200	4.080	4.8960
X15_P10	1.200	4.080	4.8960
X15_P16	1.200	4.080	4.8960

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0007	0.0008	0.0008	0.0008
D	0.0006	0.0006	0.0006	0.0006
RN	0.0007	0.0007	0.0008	0.0008

TE	0.0009	0.0009	0.0010	0.0010
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	X15_P4	X15_P0	X15_P4
CP to Q ↓	0.0904	0.1030	1.4090	1.5355
CP to Q ↑	0.0925	0.1047	1.8568	2.0532
CP to TQ ↓	0.0938	0.1071	6.9072	7.5755
CP to TQ ↑	0.1001	0.1137	19.0632	21.7350
RN to Q ↓	0.1104	0.1271	1.4055	1.5305
RN to TQ ↓	0.1138	0.1312	6.9071	7.5737
	X15_P10	X15_P16	X15_P10	X15_P16
CP to Q ↓	0.1229	0.1424	1.7206	1.8891
CP to Q ↑	0.1241	0.1431	2.3693	2.6944
CP to TQ ↓	0.1280	0.1485	8.5402	9.4066
CP to TQ ↑	0.1352	0.1564	25.8287	29.8002
RN to Q ↓	0.1537	0.1800	1.7149	1.8835
RN to TQ ↓	0.1588	0.1861	8.5371	9.4051

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.1226	0.1448	0.1785	0.2104
CP ↑	min_pulse_width to CP	0.0474	0.0521	0.0617	0.0712
D ↓	hold_rising to CP	-0.0242	-0.0313	-0.0466	-0.0582
D ↑	hold_rising to CP	-0.0219	-0.0237	-0.0339	-0.0413
D ↓	setup_rising to CP	0.0786	0.0957	0.1155	0.1319
D ↑	setup_rising to CP	0.0589	0.0634	0.0790	0.0888
RN ↓	min_pulse_width to RN	0.0854	0.0974	0.1143	0.1316
RN ↑	recovery_rising to CP	0.0275	0.0346	0.0398	0.0471
RN ↑	removal_rising to CP	-0.0103	-0.0100	-0.0153	-0.0174
TE ↓	hold_rising to CP	-0.0245	-0.0291	-0.0414	-0.0534
TE ↑	hold_rising to CP	-0.0361	-0.0435	-0.0530	-0.0684
TE ↓	setup_rising to CP	0.0874	0.1024	0.1191	0.1414
TE ↑	setup_rising to CP	0.1594	0.1908	0.2400	0.2864
TI ↓	hold_rising to CP	-0.0908	-0.1116	-0.1473	-0.1779
TI ↑	hold_rising to CP	-0.0379	-0.0441	-0.0554	-0.0650
TI ↓	setup_rising to CP	0.1548	0.1853	0.2307	0.2753
TI ↑	setup_rising to CP	0.0776	0.0886	0.1047	0.1198

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X15_P0	3.777e-05	3.918e-09
X15_P4	1.324e-05	3.918e-09
X15_P10	4.337e-06	3.918e-09
X15_P16	2.080e-06	3.918e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

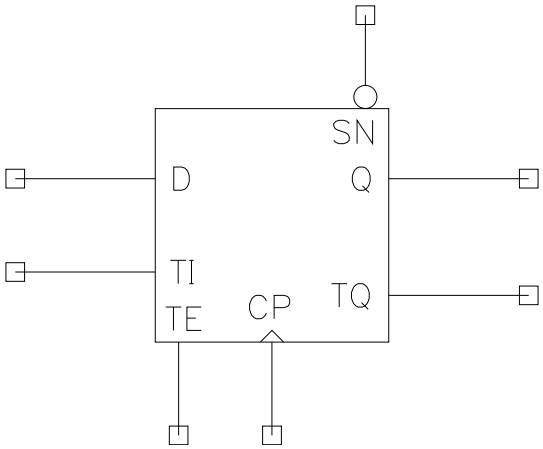
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	3.549e-03	3.583e-03	3.635e-03	3.692e-03
Clock 100Mhz Data 25Mhz	5.780e-03	5.843e-03	5.966e-03	6.098e-03
Clock 100Mhz Data 50Mhz	8.011e-03	8.103e-03	8.297e-03	8.505e-03
Clock = 0 Data 100Mhz	3.302e-03	3.329e-03	3.376e-03	3.427e-03
Clock = 1 Data 100Mhz	4.337e-05	4.214e-05	4.115e-05	4.041e-05

CNSDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.216	5.0592
X15_P4	1.200	4.216	5.0592
X15_P10	1.200	4.216	5.0592
X15_P16	1.200	4.216	5.0592

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0007	0.0008	0.0008	0.0008
D	0.0004	0.0004	0.0004	0.0005
SN	0.0014	0.0015	0.0015	0.0015

TE	0.0009	0.0009	0.0010	0.0010
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
CP to Q ↓	0.0908	0.1034	1.4080	1.5369
CP to Q ↑	0.0931	0.1054	1.8579	2.0514
CP to TQ ↓	0.0943	0.1076	6.9224	7.5883
CP to TQ ↑	0.1009	0.1146	19.0723	21.7364
SN to Q ↑	0.0924	0.1055	1.8555	2.0521
SN to TQ ↑	0.1003	0.1148	19.0737	21.7433
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
CP to Q ↓	0.1232	0.1427	1.7217	1.8921
CP to Q ↑	0.1248	0.1439	2.3721	2.6966
CP to TQ ↓	0.1285	0.1490	8.5541	9.4230
CP to TQ ↑	0.1361	0.1574	25.8484	29.8146
SN to Q ↑	0.1259	0.1459	2.3688	2.6963
SN to TQ ↑	0.1372	0.1594	25.8561	29.8264

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.1323	0.1563	0.1906	0.2267
CP ↑	min_pulse_width to CP	0.0511	0.0559	0.0617	0.0712
D ↓	hold_rising to CP	-0.0290	-0.0364	-0.0515	-0.0631
D ↑	hold_rising to CP	-0.0191	-0.0244	-0.0290	-0.0360
D ↓	setup_rising to CP	0.0883	0.1002	0.1253	0.1448
D ↑	setup_rising to CP	0.0487	0.0536	0.0637	0.0734
SN ↓	min_pulse_width to SN	0.0615	0.0664	0.0784	0.0881
SN ↑	recovery_rising to CP	0.0057	0.0079	0.0079	0.0104
SN ↑	removal_rising to CP	0.0380	0.0432	0.0505	0.0549
TE ↓	hold_rising to CP	-0.0263	-0.0339	-0.0459	-0.0582
TE ↑	hold_rising to CP	-0.0338	-0.0383	-0.0512	-0.0635
TE ↓	setup_rising to CP	0.0831	0.1005	0.1198	0.1421
TE ↑	setup_rising to CP	0.1691	0.2006	0.2519	0.2980
TI ↓	hold_rising to CP	-0.1007	-0.1214	-0.1571	-0.1911
TI ↑	hold_rising to CP	-0.0325	-0.0387	-0.0505	-0.0601
TI ↓	setup_rising to CP	0.1645	0.1951	0.2460	0.2899
TI ↑	setup_rising to CP	0.0686	0.0788	0.0900	0.1046

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X15_P0	3.874e-05	4.037e-09
X15_P4	1.376e-05	4.038e-09
X15_P10	4.533e-06	4.037e-09
X15_P16	2.175e-06	4.038e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

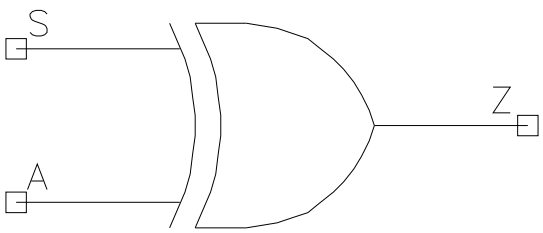
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	3.587e-03	3.620e-03	3.674e-03	3.730e-03
Clock 100Mhz Data 25Mhz	5.858e-03	5.923e-03	6.049e-03	6.181e-03
Clock 100Mhz Data 50Mhz	8.129e-03	8.226e-03	8.423e-03	8.631e-03
Clock = 0 Data 100Mhz	3.330e-03	3.357e-03	3.402e-03	3.453e-03
Clock = 1 Data 100Mhz	4.333e-05	4.223e-05	4.127e-05	4.072e-05

CNXOR2

Cell Description

2 input Exclusive OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X16_P0	1.200	1.360	1.6320
X16_P4	1.200	1.360	1.6320
X16_P10	1.200	1.360	1.6320
X16_P16	1.200	1.360	1.6320
X27_P0	1.200	2.040	2.4480
X27_P4	1.200	2.040	2.4480
X27_P10	1.200	2.040	2.4480
X27_P16	1.200	2.040	2.4480

Truth Table

A	S	Z
1	S	!S
0	S	S

Pin Capacitance

Pin	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0010	0.0010	0.0011	0.0011
S	0.0014	0.0015	0.0016	0.0017
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0014	0.0015	0.0015	0.0016
S	0.0020	0.0021	0.0022	0.0023

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0470	0.0530	1.1849	1.2884
A to Z ↑	0.0421	0.0471	1.9108	2.1150
S to Z ↓	0.0360	0.0404	1.1822	1.2872
S to Z ↑	0.0341	0.0382	1.9111	2.1100
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0627	0.0726	1.4437	1.5878

A to Z ↑	0.0549	0.0627	2.4442	2.7789
S to Z ↓	0.0476	0.0551	1.4419	1.5865
S to Z ↑	0.0446	0.0511	2.4445	2.7778
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0484	0.0549	0.7994	0.8728
A to Z ↑	0.0459	0.0518	1.0172	1.1252
S to Z ↓	0.0395	0.0449	0.7986	0.8731
S to Z ↑	0.0382	0.0433	1.0180	1.1242
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0652	0.0749	0.9816	1.0825
A to Z ↑	0.0610	0.0694	1.2978	1.4747
S to Z ↓	0.0530	0.0609	0.9815	1.0823
S to Z ↑	0.0508	0.0580	1.2982	1.4751

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X16_P0	3.174e-05	1.536e-09
X16_P4	1.097e-05	1.536e-09
X16_P10	3.540e-06	1.536e-09
X16_P16	1.674e-06	1.536e-09
X27_P0	4.650e-05	2.161e-09
X27_P4	1.549e-05	2.161e-09
X27_P10	4.858e-06	2.161e-09
X27_P16	2.267e-06	2.161e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	4.958e-03	4.889e-03	4.971e-03	5.145e-03
S to Z	4.101e-03	4.017e-03	4.073e-03	4.230e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	8.726e-03	8.635e-03	8.792e-03	8.992e-03
S to Z	6.424e-03	6.314e-03	6.387e-03	6.556e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

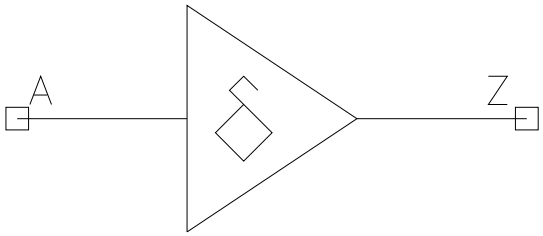
Pin Cycle (vdds)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	-7.250e-08	-1.555e-07	-1.837e-07	-3.421e-07
S to Z	1.741e-07	7.360e-08	-1.794e-07	-1.912e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	-3.385e-08	-3.118e-07	-3.741e-07	-6.179e-07
S to Z	-1.463e-07	-3.979e-08	-4.027e-07	-4.471e-07

DLYHF

Cell Description

Delay cell for Hold Time Fixing

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-DLYHFM4X7_P0	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X7_P4	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X7_P10	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X7_P16	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X15_P0	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM4X15_P4	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM4X15_P10	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM4X15_P16	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM8X7_P0	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X7_P4	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X7_P10	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X7_P16	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X15_P0	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X15_P4	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X15_P10	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X15_P16	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X54_P0	1.200	4.216	5.0592

C12T28SOI_LR_-DLYHFM8X54_P4	1.200	4.216	5.0592
C12T28SOI_LR_-DLYHFM8X54_P10	1.200	4.216	5.0592
C12T28SOI_LR_-DLYHFM8X54_P16	1.200	4.216	5.0592

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C12T28SOI_LR_-DLYHFM4X7_P0	C12T28SOI_LR_-DLYHFM4X7_P4	C12T28SOI_LR_-DLYHFM4X7_P10	C12T28SOI_LR_-DLYHFM4X7_P16
A	0.0007	0.0007	0.0007	0.0007
	C12T28SOI_LR_-DLYHFM4X15_P0	C12T28SOI_LR_-DLYHFM4X15_P4	C12T28SOI_LR_-DLYHFM4X15_P10	C12T28SOI_LR_-DLYHFM4X15_P16
A	0.0007	0.0007	0.0007	0.0007
	C12T28SOI_LR_-DLYHFM8X7_P0	C12T28SOI_LR_-DLYHFM8X7_P4	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A	0.0007	0.0007	0.0007	0.0007
	C12T28SOI_LR_-DLYHFM8X15_P0	C12T28SOI_LR_-DLYHFM8X15_P4	C12T28SOI_LR_-DLYHFM8X15_P10	C12T28SOI_LR_-DLYHFM8X15_P16
A	0.0006	0.0006	0.0007	0.0007
	C12T28SOI_LR_-DLYHFM8X54_P0	C12T28SOI_LR_-DLYHFM8X54_P4	C12T28SOI_LR_-DLYHFM8X54_P10	C12T28SOI_LR_-DLYHFM8X54_P16
A	0.0006	0.0006	0.0007	0.0007

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-DLYHFM4X7_P0	**C12T28SOI_LR_-DLYHFM4X7_P4**	**C12T28SOI_LR_-DLYHFM4X7_P0**	**C12T28SOI_LR_-DLYHFM4X7_P4**
A to Z ↓	0.1380	0.1598	2.7503	3.0122
A to Z ↑	0.1343	0.1555	4.3913	4.8660
	C12T28SOI_LR_-DLYHFM4X7_P10	**C12T28SOI_LR_-DLYHFM4X7_P16**	**C12T28SOI_LR_-DLYHFM4X7_P10**	**C12T28SOI_LR_-DLYHFM4X7_P16**
A to Z ↓	0.1941	0.2289	3.3947	3.7531
A to Z ↑	0.1895	0.2235	5.6341	6.4169
	C12T28SOI_LR_-DLYHFM4X15_P0	**C12T28SOI_LR_-DLYHFM4X15_P4**	**C12T28SOI_LR_-DLYHFM4X15_P0**	**C12T28SOI_LR_-DLYHFM4X15_P4**
A to Z ↓	0.1483	0.1719	1.3540	1.4866
A to Z ↑	0.1466	0.1702	2.0382	2.2591
	C12T28SOI_LR_-DLYHFM4X15_P10	**C12T28SOI_LR_-DLYHFM4X15_P16**	**C12T28SOI_LR_-DLYHFM4X15_P10**	**C12T28SOI_LR_-DLYHFM4X15_P16**
A to Z ↓	0.2094	0.2475	1.6814	1.8648
A to Z ↑	0.2080	0.2461	2.6183	2.9818
	C12T28SOI_LR_-DLYHFM8X7_P0	**C12T28SOI_LR_-DLYHFM8X7_P4**	**C12T28SOI_LR_-DLYHFM8X7_P0**	**C12T28SOI_LR_-DLYHFM8X7_P4**
A to Z ↓	0.2517	0.2935	2.7807	3.0467
A to Z ↑	0.2359	0.2741	4.0548	4.4868

	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A to Z ↓	0.3606	0.4275	3.4420	3.8073
A to Z ↑	0.3359	0.3967	5.1948	5.9138
	C12T28SOI_LR_-DLYHFM8X15_P0	**C12T28SOI_LR_-DLYHFM8X15_P4**	**C12T28SOI_LR_-DLYHFM8X15_P0**	**C12T28SOI_LR_-DLYHFM8X15_P4**
A to Z ↓	0.2596	0.3029	1.3591	1.4934
A to Z ↑	0.2480	0.2889	2.0413	2.2619
	C12T28SOI_LR_-DLYHFM8X15_P10	**C12T28SOI_LR_-DLYHFM8X15_P16**	**C12T28SOI_LR_-DLYHFM8X15_P10**	**C12T28SOI_LR_-DLYHFM8X15_P16**
A to Z ↓	0.3723	0.4421	1.6935	1.8817
A to Z ↑	0.3542	0.4193	2.6188	2.9849
	C12T28SOI_LR_-DLYHFM8X54_P0	**C12T28SOI_LR_-DLYHFM8X54_P4**	**C12T28SOI_LR_-DLYHFM8X54_P0**	**C12T28SOI_LR_-DLYHFM8X54_P4**
A to Z ↓	0.3307	0.3838	0.3540	0.3860
A to Z ↑	0.3014	0.3484	0.5802	0.6409
	C12T28SOI_LR_-DLYHFM8X54_P10	**C12T28SOI_LR_-DLYHFM8X54_P16**	**C12T28SOI_LR_-DLYHFM8X54_P10**	**C12T28SOI_LR_-DLYHFM8X54_P16**
A to Z ↓	0.4734	0.5596	0.4323	0.4755
A to Z ↑	0.4285	0.5055	0.7394	0.8390

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
C12T28SOI_LR_DLYHFM4X7_P0	5.446e-06	1.298e-09
C12T28SOI_LR_DLYHFM4X7_P4	1.998e-06	1.298e-09
C12T28SOI_LR_DLYHFM4X7_P10	6.936e-07	1.298e-09
C12T28SOI_LR_DLYHFM4X7_P16	3.492e-07	1.298e-09
C12T28SOI_LR_DLYHFM4X15_P0	1.022e-05	1.417e-09
C12T28SOI_LR_DLYHFM4X15_P4	3.609e-06	1.417e-09
C12T28SOI_LR_DLYHFM4X15_P10	1.206e-06	1.417e-09
C12T28SOI_LR_DLYHFM4X15_P16	5.908e-07	1.417e-09
C12T28SOI_LR_DLYHFM8X7_P0	6.020e-06	2.013e-09
C12T28SOI_LR_DLYHFM8X7_P4	2.265e-06	2.013e-09
C12T28SOI_LR_DLYHFM8X7_P10	8.122e-07	2.013e-09
C12T28SOI_LR_DLYHFM8X7_P16	4.196e-07	2.013e-09
C12T28SOI_LR_DLYHFM8X15_P0	1.090e-05	2.132e-09
C12T28SOI_LR_DLYHFM8X15_P4	3.918e-06	2.132e-09
C12T28SOI_LR_DLYHFM8X15_P10	1.337e-06	2.132e-09
C12T28SOI_LR_DLYHFM8X15_P16	6.658e-07	2.132e-09
C12T28SOI_LR_DLYHFM8X54_P0	3.634e-05	4.037e-09
C12T28SOI_LR_DLYHFM8X54_P4	1.287e-05	4.037e-09
C12T28SOI_LR_DLYHFM8X54_P10	4.351e-06	4.037e-09
C12T28SOI_LR_DLYHFM8X54_P16	2.170e-06	4.037e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

Pin Cycle (vdd)	C12T28SOI_LR_-DLYHFM4X7_P0	C12T28SOI_LR_-DLYHFM4X7_P4	C12T28SOI_LR_-DLYHFM4X7_P10	C12T28SOI_LR_-DLYHFM4X7_P16
A to Z	3.360e-03	3.396e-03	3.504e-03	3.634e-03
	C12T28SOI_LR_-DLYHFM4X15_P0	C12T28SOI_LR_-DLYHFM4X15_P4	C12T28SOI_LR_-DLYHFM4X15_P10	C12T28SOI_LR_-DLYHFM4X15_P16
A to Z	4.730e-03	4.645e-03	4.681e-03	4.802e-03

	C12T28SOI_LR_-DLYHFM8X7_P0	C12T28SOI_LR_-DLYHFM8X7_P4	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A to Z	5.331e-03	5.393e-03	5.576e-03	5.766e-03
	C12T28SOI_LR_-DLYHFM8X15_P0	C12T28SOI_LR_-DLYHFM8X15_P4	C12T28SOI_LR_-DLYHFM8X15_P10	C12T28SOI_LR_-DLYHFM8X15_P16
A to Z	6.679e-03	6.625e-03	6.725e-03	6.900e-03
	C12T28SOI_LR_-DLYHFM8X54_P0	C12T28SOI_LR_-DLYHFM8X54_P4	C12T28SOI_LR_-DLYHFM8X54_P10	C12T28SOI_LR_-DLYHFM8X54_P16
A to Z	2.109e-02	2.132e-02	2.231e-02	2.320e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V, Worst process

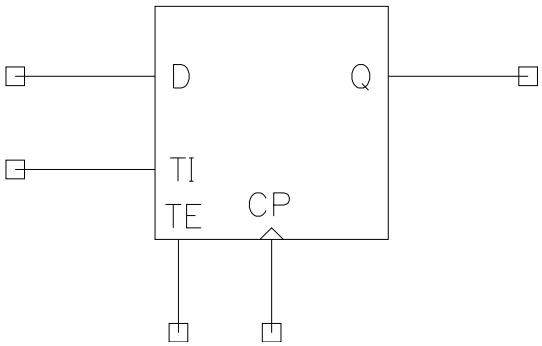
Pin Cycle (vdds)	C12T28SOI_LR_-DLYHFM4X7_P0	C12T28SOI_LR_-DLYHFM4X7_P4	C12T28SOI_LR_-DLYHFM4X7_P10	C12T28SOI_LR_-DLYHFM4X7_P16
A to Z	7.840e-08	-1.027e-06	-2.546e-06	-3.474e-06
	C12T28SOI_LR_-DLYHFM4X15_P0	C12T28SOI_LR_-DLYHFM4X15_P4	C12T28SOI_LR_-DLYHFM4X15_P10	C12T28SOI_LR_-DLYHFM4X15_P16
A to Z	9.170e-08	-1.100e-06	-2.624e-06	-3.527e-06
	C12T28SOI_LR_-DLYHFM8X7_P0	C12T28SOI_LR_-DLYHFM8X7_P4	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A to Z	2.530e-08	-1.708e-06	-3.941e-06	-5.308e-06
	C12T28SOI_LR_-DLYHFM8X15_P0	C12T28SOI_LR_-DLYHFM8X15_P4	C12T28SOI_LR_-DLYHFM8X15_P10	C12T28SOI_LR_-DLYHFM8X15_P16
A to Z	6.310e-08	-1.623e-06	-3.939e-06	-5.392e-06
	C12T28SOI_LR_-DLYHFM8X54_P0	C12T28SOI_LR_-DLYHFM8X54_P4	C12T28SOI_LR_-DLYHFM8X54_P10	C12T28SOI_LR_-DLYHFM8X54_P16
A to Z	5.640e-07	-3.697e-06	-1.453e-05	-2.159e-05

SDFSYNCPQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.400	8.1600
X8_P4	2.400	3.400	8.1600
X8_P10	2.400	3.400	8.1600
X8_P16	2.400	3.400	8.1600

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0008	0.0008	0.0009	0.0009
D	0.0006	0.0006	0.0006	0.0007
TE	0.0009	0.0009	0.0010	0.0010
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X8_P4	X8_P0	X8_P4
CP to Q ↓	0.1573	0.1822	2.1885	2.3830
CP to Q ↑	0.1718	0.1971	3.7418	4.1358

	X8_P10	X8_P16	X8_P10	X8_P16
CP to Q ↓	0.2223	0.2625	2.6704	2.9415
CP to Q ↑	0.2377	0.2788	4.7840	5.4381

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.2524	0.2968	0.3721	0.4436
CP ↑	min_pulse_width to CP	0.0877	0.0984	0.1224	0.1416
D ↓	hold_rising to CP	-0.0853	-0.1048	-0.1345	-0.1583
D ↑	hold_rising to CP	-0.0312	-0.0383	-0.0481	-0.0583
D ↓	setup_rising to CP	0.1468	0.1737	0.2127	0.2542
D ↑	setup_rising to CP	0.0609	0.0682	0.0780	0.0902
TE ↓	hold_rising to CP	-0.0702	-0.0822	-0.1012	-0.1211
TE ↑	hold_rising to CP	-0.0774	-0.0927	-0.1123	-0.1318
TE ↓	setup_rising to CP	0.1446	0.1689	0.2083	0.2473
TE ↑	setup_rising to CP	0.3010	0.3568	0.4472	0.5347
TI ↓	hold_rising to CP	-0.2177	-0.2681	-0.3327	-0.4011
TI ↑	hold_rising to CP	-0.0791	-0.0943	-0.1138	-0.1349
TI ↓	setup_rising to CP	0.2914	0.3465	0.4364	0.5203
TI ↑	setup_rising to CP	0.1139	0.1291	0.1500	0.1693

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	4.829e-05	4.390e-09
X8_P4	1.724e-05	4.390e-09
X8_P10	5.750e-06	4.389e-09
X8_P16	2.800e-06	4.390e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

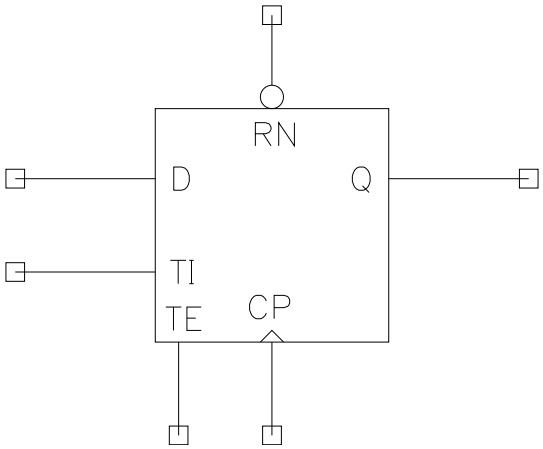
Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	6.987e-03	7.106e-03	7.265e-03	7.437e-03
Clock 100Mhz Data 25Mhz	1.060e-02	1.075e-02	1.104e-02	1.135e-02
Clock 100Mhz Data 50Mhz	1.421e-02	1.440e-02	1.482e-02	1.527e-02
Clock = 0 Data 100Mhz	6.741e-03	6.712e-03	6.721e-03	6.773e-03
Clock = 1 Data 100Mhz	3.547e-05	3.483e-05	3.642e-05	4.087e-05

SDFSYNCPRQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0008	0.0008	0.0009	0.0009
D	0.0006	0.0006	0.0006	0.0007
RN	0.0017	0.0017	0.0018	0.0019
TE	0.0009	0.0009	0.0010	0.0010
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
CP to Q ↓	0.1736	0.2013	2.1976	2.3998
CP to Q ↑	0.1730	0.1984	3.7262	4.1144
RN to Q ↓	0.1768	0.2074	2.1987	2.3991
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
CP to Q ↓	0.2455	0.2900	2.6940	2.9633
CP to Q ↑	0.2396	0.2815	4.7612	5.4203
RN to Q ↓	0.2570	0.3080	2.6906	2.9625

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.2481	0.2968	0.3678	0.4431
CP ↑	min_pulse_width to CP	0.0936	0.1117	0.1369	0.1610
D ↓	hold_rising to CP	-0.0831	-0.0999	-0.1293	-0.1541
D ↑	hold_rising to CP	-0.0335	-0.0414	-0.0506	-0.0604
D ↓	setup_rising to CP	0.1475	0.1688	0.2078	0.2472
D ↑	setup_rising to CP	0.0634	0.0713	0.0835	0.0933
RN ↓	min_pulse_width to RN	0.1458	0.1702	0.2043	0.2434
RN ↑	recovery_rising to CP	0.0144	0.0172	0.0227	0.0227
RN ↑	removal_rising to CP	-0.0100	-0.0125	-0.0178	-0.0178
TE ↓	hold_rising to CP	-0.0724	-0.0843	-0.1040	-0.1235
TE ↑	hold_rising to CP	-0.0805	-0.0920	-0.1120	-0.1341
TE ↓	setup_rising to CP	0.1424	0.1640	0.2034	0.2393
TE ↑	setup_rising to CP	0.2961	0.3520	0.4427	0.5305
TI ↓	hold_rising to CP	-0.2179	-0.2581	-0.3319	-0.3928
TI ↑	hold_rising to CP	-0.0832	-0.0938	-0.1148	-0.1342
TI ↓	setup_rising to CP	0.2865	0.3417	0.4302	0.5139
TI ↑	setup_rising to CP	0.1178	0.1291	0.1498	0.1744

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	4.805e-05	4.976e-09
X8_P4	1.705e-05	4.976e-09
X8_P10	5.709e-06	4.976e-09
X8_P16	2.811e-06	4.976e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	7.270e-03	7.395e-03	7.575e-03	7.777e-03

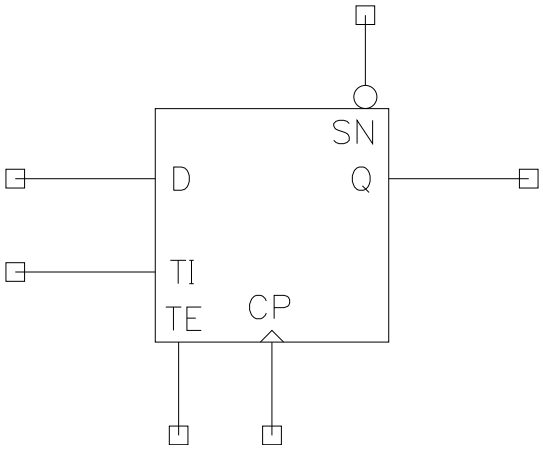
Clock 100Mhz Data 25Mhz	1.098e-02	1.115e-02	1.148e-02	1.184e-02
Clock 100Mhz Data 50Mhz	1.469e-02	1.490e-02	1.539e-02	1.591e-02
Clock = 0 Data 100Mhz	6.756e-03	6.741e-03	6.761e-03	6.812e-03
Clock = 1 Data 100Mhz	3.577e-05	3.618e-05	4.737e-05	5.951e-05

SDFSYNCPSQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0008	0.0008	0.0009	0.0009
D	0.0004	0.0004	0.0005	0.0005
SN	0.0015	0.0015	0.0016	0.0017
TE	0.0009	0.0009	0.0010	0.0010
TI	0.0003	0.0003	0.0004	0.0004

Propagation Delay at 125C, 0.90V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
CP to Q ↓	0.1287	0.1476	2.7527	3.0465
CP to Q ↑	0.1446	0.1656	3.9969	4.4291
SN to Q ↑	0.1827	0.2124	3.8523	4.2681
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
CP to Q ↓	0.1776	0.2075	3.4977	3.9243
CP to Q ↑	0.1996	0.2342	5.1355	5.8529
SN to Q ↑	0.2594	0.3069	4.9475	5.6315

Timing Constraints (ns) at 125C, 0.90V, Worst process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.2379	0.2823	0.3528	0.4237
CP ↑	min_pulse_width to CP	0.0973	0.1117	0.1369	0.1610
D ↓	hold_rising to CP	-0.0681	-0.0853	-0.1045	-0.1297
D ↑	hold_rising to CP	-0.0316	-0.0387	-0.0485	-0.0552
D ↓	setup_rising to CP	0.1370	0.1590	0.1957	0.2298
D ↑	setup_rising to CP	0.0637	0.0682	0.0808	0.0905
SN ↓	min_pulse_width to SN	0.1716	0.1987	0.2427	0.2866
SN ↑	recovery_rising to CP	0.0040	0.0009	0.0009	0.0033
SN ↑	removal_rising to CP	0.0525	0.0598	0.0723	0.0817
TE ↓	hold_rising to CP	-0.0632	-0.0748	-0.0970	-0.1190
TE ↑	hold_rising to CP	-0.0805	-0.0920	-0.1120	-0.1337
TE ↓	setup_rising to CP	0.1323	0.1539	0.1883	0.2251
TE ↑	setup_rising to CP	0.2885	0.3447	0.4304	0.5152
TI ↓	hold_rising to CP	-0.1997	-0.2435	-0.3085	-0.3682
TI ↑	hold_rising to CP	-0.0832	-0.0953	-0.1146	-0.1357
TI ↓	setup_rising to CP	0.2818	0.3373	0.4163	0.4998
TI ↑	setup_rising to CP	0.1186	0.1339	0.1547	0.1792

Average Leakage Power (mW) at 125C, 0.90V, Worst process

	vdd	vdds
X8_P0	4.947e-05	5.100e-09
X8_P4	1.824e-05	5.100e-09
X8_P10	6.227e-06	5.100e-09
X8_P16	3.074e-06	5.100e-09

Internal Energy (uW/MHz) at 125C, 0.90V, Worst process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	7.154e-03	7.280e-03	7.458e-03	7.653e-03

Clock 100Mhz Data 25Mhz	1.061e-02	1.075e-02	1.102e-02	1.133e-02
Clock 100Mhz Data 50Mhz	1.407e-02	1.422e-02	1.459e-02	1.502e-02
Clock = 0 Data 100Mhz	6.834e-03	6.851e-03	6.898e-03	6.973e-03
Clock = 1 Data 100Mhz	4.497e-05	4.374e-05	4.346e-05	4.795e-05

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