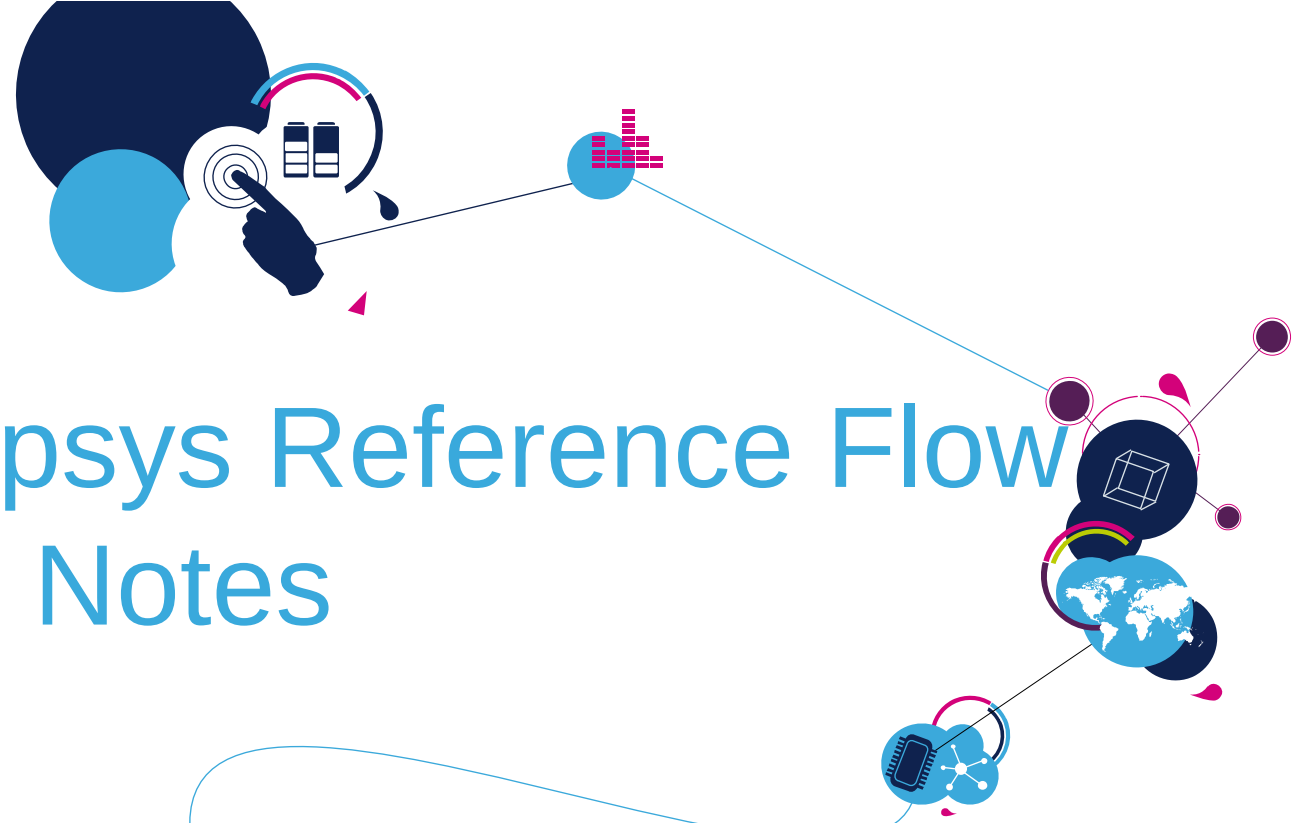

28nm FD-SOI Synopsys Reference Flow Sign-Off Application Notes

Version 3.1

Digital Design Flows & Methodologies

January 2019

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Revisions

Version	Date	Comment
3.1	January 2019	• No Change. Alignment with PnR 3.1
3.0	October 2018	• No Change. Alignment with PnR 3.0
2.0	March 2018	• Updated EDA tools versions • Vdd range is 0.8V to 1.2V • OCV derate factors have to be applied on both gate delays and wire delays • Updated hold data derates for PB0 & PB4 clock tree • Updated Primetime settings • Updated POCV PrimeTime settings
1.0	June 2017	Initial Version

Prerequisites : Documentation

- Please refer to the **Foundation_Synopsys_TechnoKit_cmos028FDSOI** User Manual for the description of the technology files

- Please refer to the **28nm FD-SOI Synopsys Reference Flow PnR Application Notes** for information regarding Place-and-Route flow

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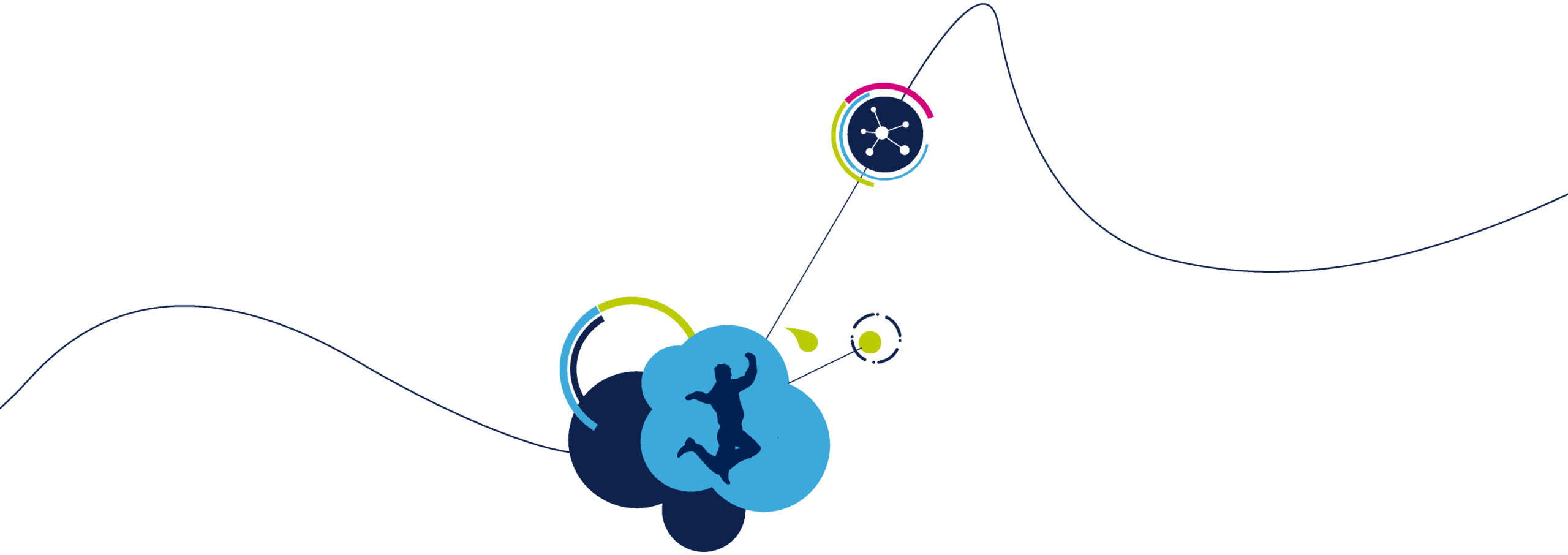
EDA Tools Versions

- The 28nm FD-SOI Synopsys Reference Flow has been qualified with the following EDA tools

Sign-Off Step	EDA Tool & Version
Gate-Level RC Extraction	StarRC m-2017.06-sp2
Static Timing Analysis	PrimeTime m-2017.06-sp3-2
Power Analysis	PrimeTime-PX m-2017.06-sp3-2

- EDA tools versions used for flow execution are left up to user discretion



Gate-Level RC Extraction

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8 Sign-Off Extraction Scenarios

#	RC	T
1	SigCmin	max T
2	SigCmin	min T
3	SigCmax	max T
4	SigCmax	min T
5	SigRCmin	max T
6	SigRCmin	min T
7	SigRCmax	max T
8	SigRCmax	min T

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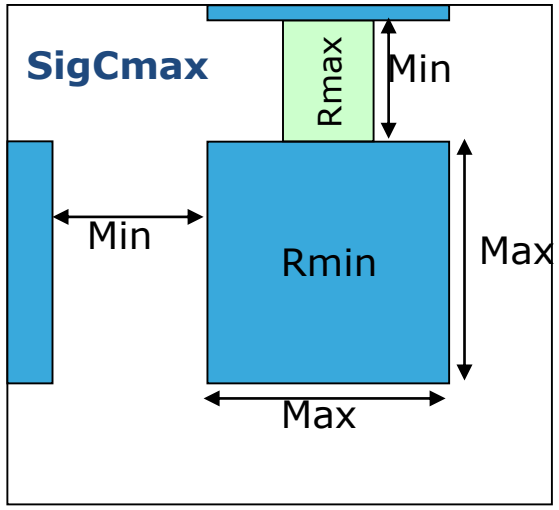
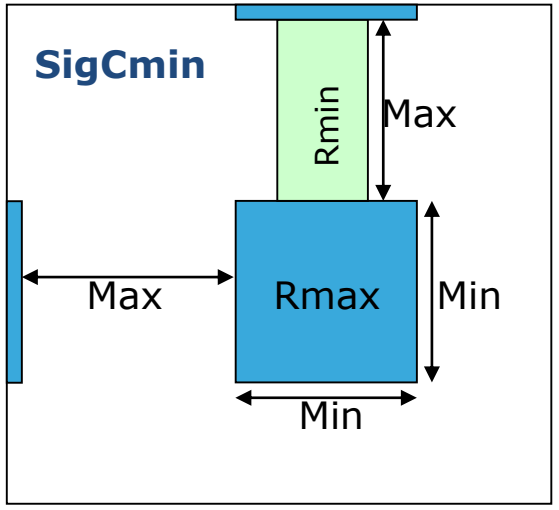
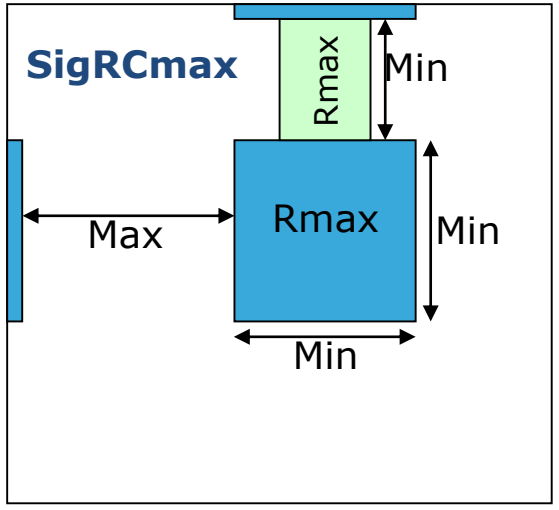
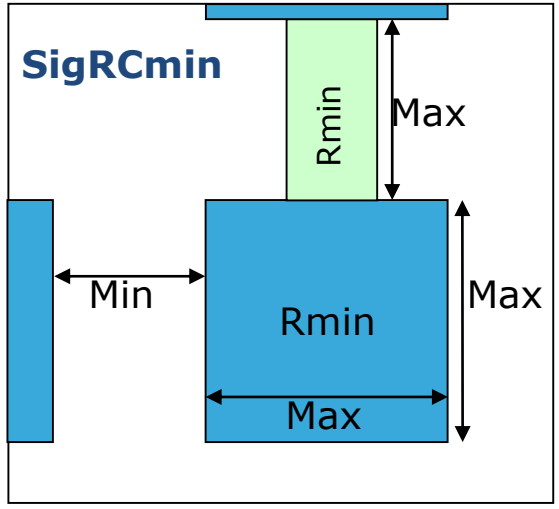
28nm FD-SOI RC Corners Description









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28nm FD-SOI RC Corners Summary

Name	Description	
	Capacitance	Resistance
SigCmin	Clateral MIN Cvertical MIN	Rwire MAX Rvia MIN
SigCmax	Clateral MAX Cvertical MAX	Rwire MIN Rvia MAX
SigRCmin	Clateral MAX Cvertical MIN	Rwire MIN Rvia MIN
SigRCmax	Clateral MIN Cvertical MAX	Rwire MAX Rvia MAX

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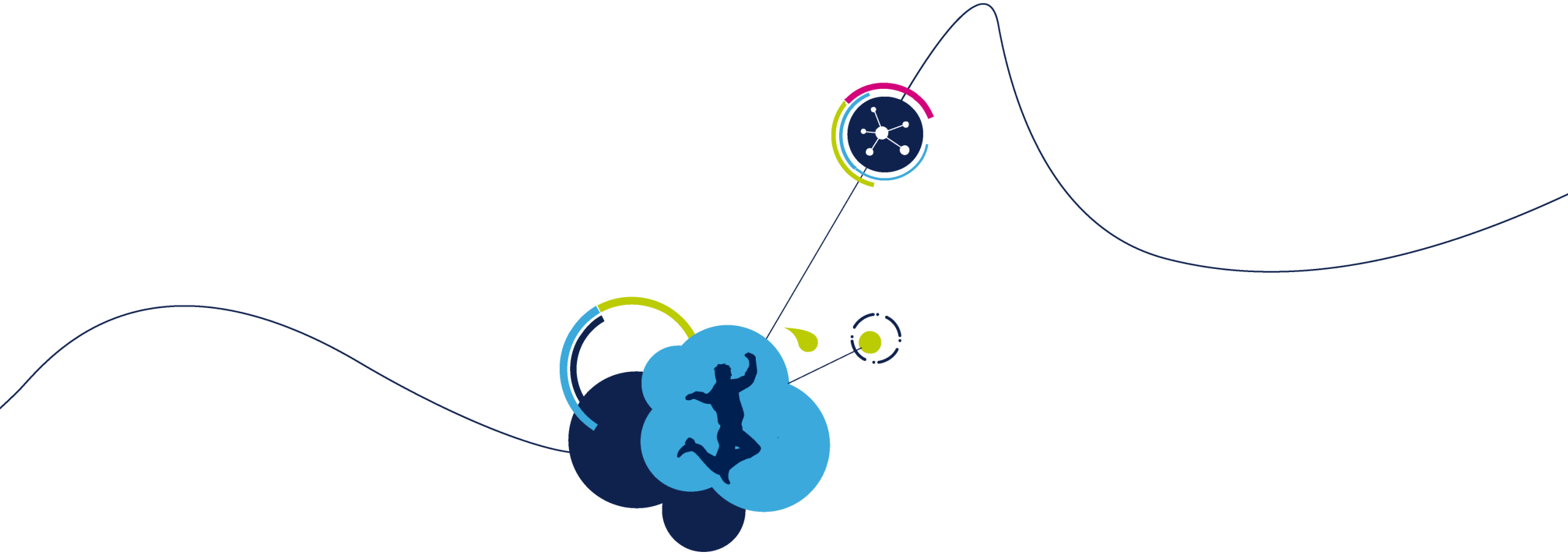

Static Timing Analysis

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16 Sign-Off STA Scenarios per timing mode

#	P	V	T	RC
1	ff28	max V	max T	SigCmin
2	ff28	max V	min T	SigCmin
3	ff28	max V	max T	SigCmax
4	ff28	max V	min T	SigCmax
5	ff28	max V	max T	SigRCmin
6	ff28	max V	min T	SigRCmin
7	ff28	max V	max T	SigRCmax
8	ff28	max V	min T	SigRCmax
9	ss28	min V	max T	SigCmin
10	ss28	min V	min T	SigCmin
11	ss28	min V	max T	SigCmax
12	ss28	min V	min T	SigCmax
13	ss28	min V	max T	SigRCmin
14	ss28	min V	min T	SigRCmin
15	ss28	min V	max T	SigRCmax
16	ss28	min V	min T	SigRCmax

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Max. transition constraint on clock

- The maximum transition check on clock depends on the operating voltage
- In case of multiple operating voltages, it is required to check the max. transition on clock **only at the lowest voltage**

Voltage	Clock Max. Transition Constraint
0.95 V	150 ps
0.90 V	160 ps
0.85 V	170 ps
0.80 V	200 ps

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Clock Tree Implementation Rules

Criteria	Value
Maximum clock transition	See previous slides
Clock tree cells	Only balanced clock cells (*CN* cells)
CTS	Only inverters
Vth	No Vth mix
	Use fastest Vth*
Poly Biasing	No Poly Biasing mix
	Use fastest PB*
Minimum drive strength allowed	X9
Maximum drive strength allowed (EMG constraints)	X70

* *Recommended*

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28nm FD-SOI OCV / POCV Strategy

- **Both OCV and POCV can be used for 28nm FD-SOI Sign-Off STA**

- **For OCV Sign-Off STA**
  - Use derating factors from slide #13 in case of PB0 clock tree
  - Use derating factors from slide #14 in case of PB4 clock tree
  - Use CCS libraries

- **For POCV Sign-Off STA**
  - Use derating factors from slide #15 in case of PB0 clock tree
  - Use derating factors from slide #16 in case of PB4 clock tree
  - For CLOCK libraries, use CCS libraries with LVF views (available in /electrical/lvf/ repository)

28nm FD-SOI OCV Derating Factors

PB0 Clock Tree

	Clock	Data Derate for Hold Checks	Technology Uncertainty	
			Setup	Hold
1.20 V	+/- 5 %	- 23 %	0 ps	20 ps
1.10 V				
1.00 V				
0.90 V				
0.85 V				
0.80 V				

- To be applied on both gate delays and wire delays
- Valid under compliance with “Clock Tree Implementation Rules”

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28nm FD-SOI OCV Derating Factors

PB4 Clock Tree

	Clock	Data Derate for Hold Checks	Technology Uncertainty	
			Setup	Hold
1.20 V	+/- 5 %	-18 %	0 ps	20 ps
1.10 V				
1.00 V				
0.90 V				
0.85 V				
0.80 V				

- To be applied on both gate delays and wire delays
- Valid under compliance with “Clock Tree Implementation Rules”

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28nm FD-SOI POCV Derating Factors

PB0 Clock Tree

	Clock	Data Derate for Hold Checks	Technology Uncertainty	
			Setup	Hold
1.20 V	+/- 1.5 %	- 23 %	0 ps	20 ps
1.10 V	+/- 1.6 %			
1.00 V	+/- 1.7 %			
0.90 V	+/- 1.8 %			
0.85 V	+/- 1.9 %			
0.80 V	+/- 2.0 %			

- To be applied on both gate delays and wire delays
- Valid under compliance with “Clock Tree Implementation Rules”

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28nm FD-SOI POCV Derating Factors

PB4 Clock Tree

	Clock	Data Derate for Hold Checks	Technology Uncertainty	
			Setup	Hold
1.20 V	+/- 1.5 %	- 18 %	0 ps	20 ps
1.10 V	+/- 1.6 %			
1.00 V	+/- 1.7 %			
0.90 V	+/- 1.8 %			
0.85 V	+/- 1.9 %			
0.80 V	+/- 2.0 %			

- To be applied on both gate delays and wire delays
- Valid under compliance with “Clock Tree Implementation Rules”

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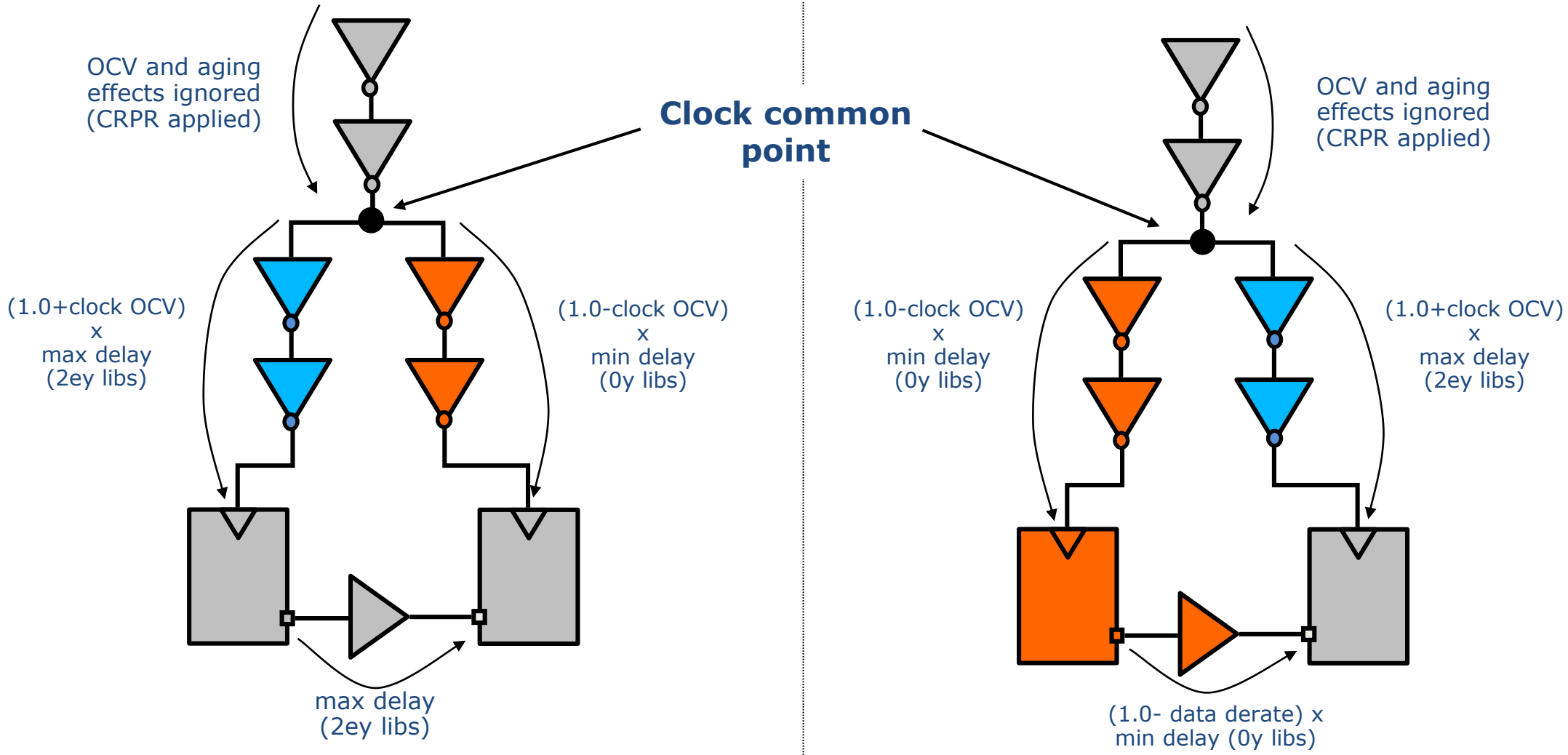
OCV & CRPR Strategy



Setup Checks

Hold Checks

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Required Settings for PrimeTime

- The following variables have to be set in PrimeTime for static timing analysis in 28nm FD-SOI:
  - set ccs_timing_vc_step_number 100000000
  - set timing_remove_clock_reconvergence_pessimism true
  - set timing_clock_reconvergence_pessimism same_transition
  - set timing_early_launch_at_borrowing_latches false
  - set si_enable_analysis true
  - set si_xtalk_double_switching_mode clock_network
  - set delay_calc_waveform_analysis_mode disabled
- CCS libraries mandatory (timing & noise)

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Setting STA 0y/2ey in PrimeTime

- In file: .synopsys_pt.setup (example for 2 library)
  - set link_path {* $my_working_path/LIBRARIES/C28SOI_SC_12_CORE_LL/ccs/C28SOI_SC_12_CORE_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C_2ey.db $my_working_path/LIBRARIES/C28SOI_SC_12_CLK_LL/ccs/C28SOI_SC_12_CLK_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C_2ey.db}
  - set link_path_per_instance [list \
  - [list instance1 "* lib1 lib2 …"]
  - [list instance2 "* lib1 lib2 …"]

- In script TIMING_ANALYSIS.pt (example for 2 library)
  - read_verilog TOP.v
  - current_design TOP
  - link_design
  - set_min_library -min_version $my_working_path/LIBRARIES/C28SOI_SC_12_CORE_LL/ccs/C28SOI_SC_12_CORE_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C.db $my_working_path/LIBRARIES/C28SOI_SC_12_CORE_LL/ccs/C28SOI_SC_12_CORE_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C_2ey.db
  - set_min_library -min_version $my_working_path/LIBRARIES/C28SOI_SC_12_CLK_LL/ccs/C28SOI_SC_12_CLK_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C.db $my_working_path/LIBRARIES/C28SOI_SC_12_CLK_LL/ccs/C28SOI_SC_12_CLK_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C_2ey.db
  - read_parasitics …

- To verify library relationships/settings: list_libs command
  - An uppercase 'M' (resp. A lowercase 'm') to the left of a library indicates that the library is the maximum (resp. minimum) library of a max/min library relationship created by the set_min_library command.
  - pt_shell> list_libraries -only_used
  - Library Registry:
  - *M C28SOI_SC_12_CLK_LL /path/ccs/C28SOI_SC_12_CLK_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C_2ey.db:C28SOI_SC_12_CLK_LL
  - m C28SOI_SC_12_CLK_LL /path/ccs/C28SOI_SC_12_CLK_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C.db:C28SOI_SC_12_CLK_LL

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POCV Settings for PrimeTime

- The following variables have to be set in PrimeTime to use POCV with LVF views in 28nm FD-SOI :
  - set timing_pocvm_enable_analysis true
  - set timing_enable_slew_variation true
  - set timing_enable_constraint_variation false
  - set timing_ocvm_enable_distance_analysis false
  - set timing_pocvm_corner_sigma 3
  - set timing_pocvm_report_sigma 3
- LVF views mandatory for CLOCK libraries

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POCV Settings for PrimeTime

- The following commands have to be applied in PrimeTime to set derating factors with POCV methodology in 28nm FD-SOI :
  - set_timing_derate -pocvm_coefficient_scale_factor -cell_delay -data -late 0.0
  - set_timing_derate -pocvm_coefficient_scale_factor -cell_delay -data -early 0.0

  - set_timing_derate -clock -early –increment -0.02
  - set_timing_derate -clock -late -increment +0.02
  - set_timing_derate -data -early -increment -0.18
  - set_timing_derate -data -late -increment 0.0

  - set_timing_derate -net_delay -clock -early -increment -dynamic 0.0
  - set_timing_derate -net_delay -clock -late -increment -dynamic 0.0
  - set_timing_derate -net_delay -data -early -increment -dynamic 0.0
  - set_timing_derate -net_delay -data -late -increment -dynamic 0.0

Values to be set depending on voltage (cf. slide 14)

Example given @ 0.8V :

- Clock OCV : +/- 2%
- Data OCV for hold: -18%
- Data OCV for setup: 0%

- It is mandatory to use « *–increment* » switch with *set_timing_derate* to avoid conflicts in PrimeTime for POCVM-based runs

Recommended PrimeTime Settings

- PrimeTime globals
  - set timing_crpr_threshold_ps 1
  - set timing_enable_max_capacitance_set_case_analysis true
  - set si_xtalk_delay_analysis_mode all_path_edges
  - set report_capacitance_use_ccs_receiver_model false
  - set pba_path_recalculation_limit_compatibility false
  - set timing_include_uncertainty_for_pulse_checks setup_only
  - set timing_save_pin_arrival_and_slack true

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Recommended PrimeTime Settings

- ECO
  - Define eco_instance_name_prefix/eco_net_name_prefix (avoid bug in PT)
  - In case of 3rd party tool used for PnR
    - set eco_strict_pin_name_equivalence true
  - Footprint constant cell swap
    - define_user_attribute -import -classes lib_cell -type string cell_footprint
    - set eco_alternative_cell_attribute_restrictions cell_footprint
- SI Analysis
  - set_noise_parameters -enable_propagation -analysis_mode report_at_endpoint

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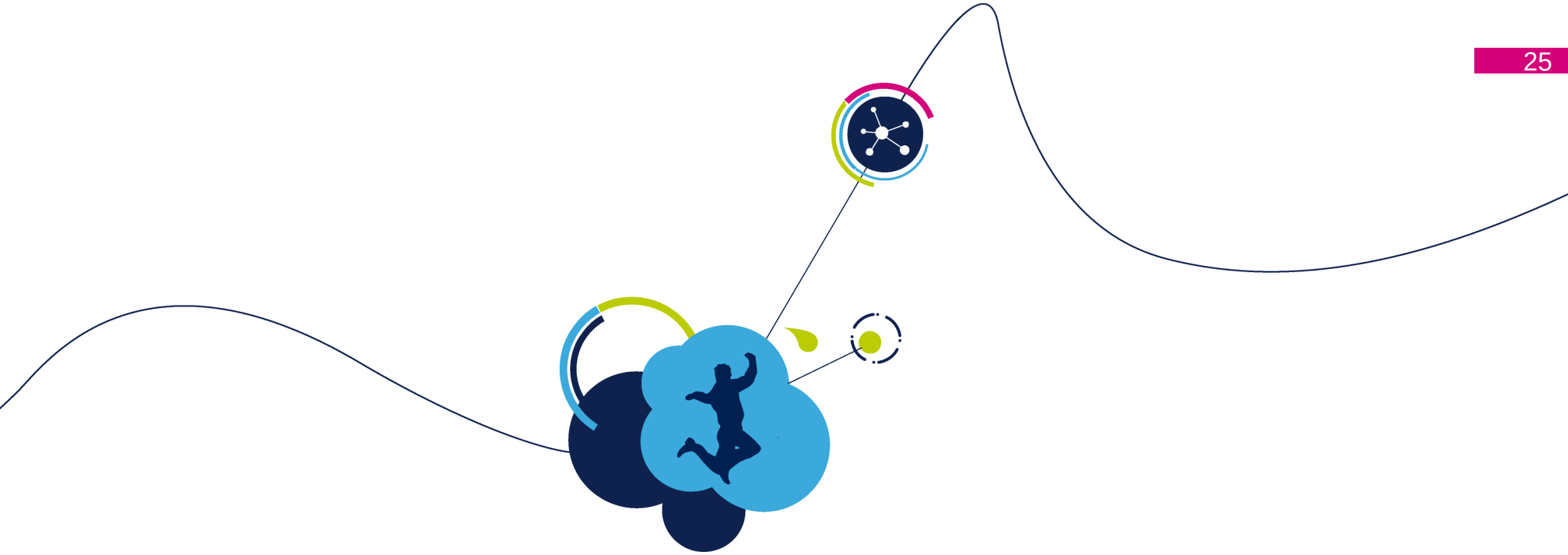

SDF Generation

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SDF Generation Methodology

- SDF can be generated in PrimeTime for back-annotated simulation purpose
- Using native SDF 3.0 flow, ST standards cells have empty mapping files : it is not required to use them in the PrimeTime *write_sdf* command
- Some memories and macros may have non empty mapping files
  - In that case those mapping files are compliant with SDF 3.0
  - They have to be loaded in the *write_sdf* command
- PrimeTime settings and commands
  - set timing_reduce_parallel_cell_arcs “false“
  - write_sdf -significant_digit 4 -input_port_nets -output_port_nets -context verilog -version 3.0 -include {SETUPHOLD RECREM} -compress gzip -map “” <design>.verilog.sdf.gz

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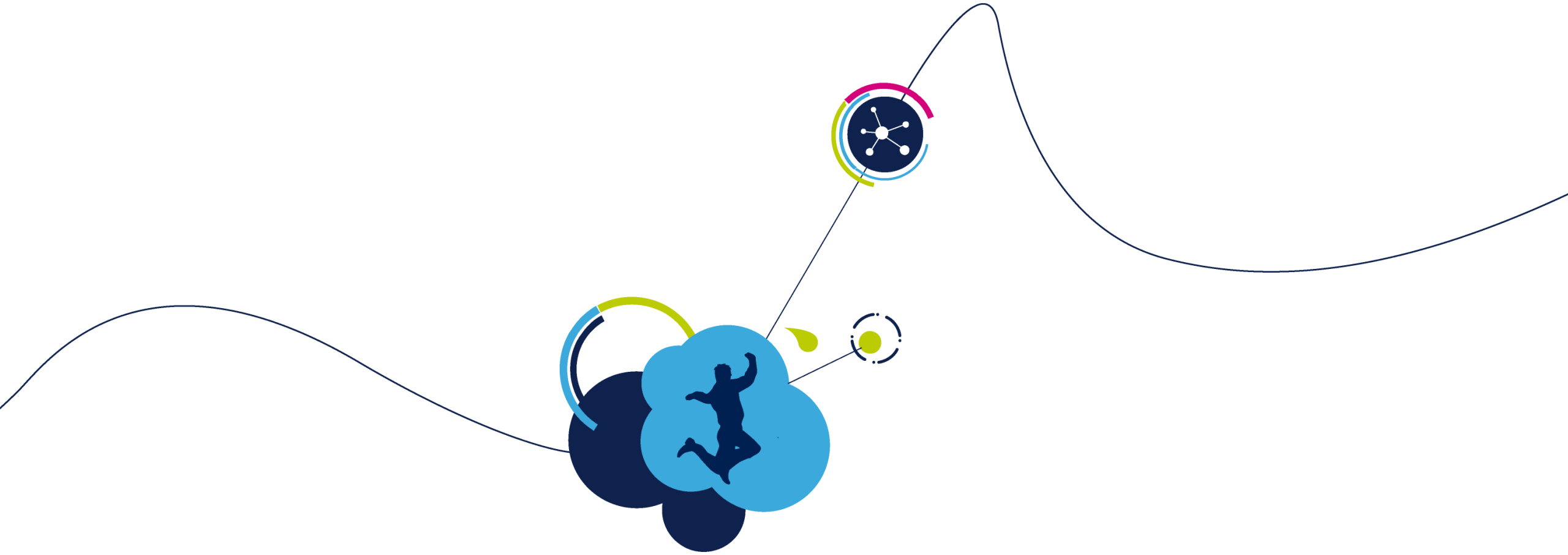

Power Analysis

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Sign-Off Power Analysis Scenarios Description

- The two following corners are typically used for power consumption measurements. However, power analysis scenarios may vary depending on chip specifications and power targets

#	Intent	P	V	T	RC
1	Typical Power Measurement	tt28	Nom. V	25°C	nominal
2	Maximum Power Measurement	ff28	Max. V	Max T	SigCmax

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Required Settings for PrimeTime-PX

- The following variables have to be set in PrimeTime-PX for power analysis in 28nm FD-SOI:
  - set power_enable_analysis true
  - set power_model_preference nlpm
  - set power_table_include_switching_power false
  - set power_use_ccsp_pin_capacitance false
  - set rc_ccs_extrapolation_range_compatibility false
  - set link_keep_unconnected_cells true
  - set link_keep_cells_with_pg_only_connection true

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