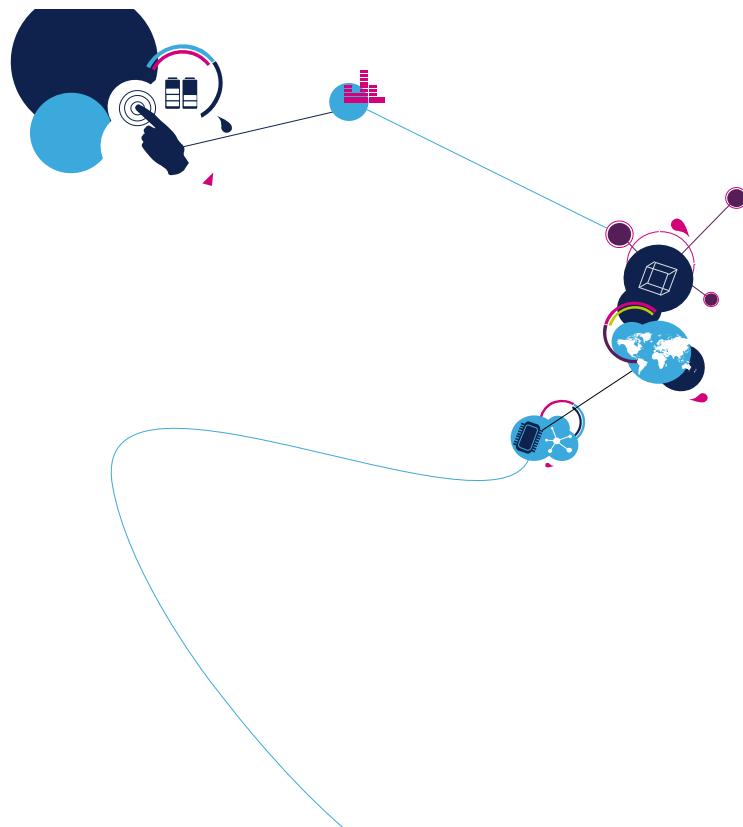




DK/PDK 28FDSOI_RF_mmW

v1.2

6U1x_2U2x_2T8x_LB/6U1x_2T8x_LB





Contents

1	Introduction.....	7
2	Installation.....	8
2.1	Delivery Contents	8
2.1.1	Libraries installed in the Design Kit	8
2.2	Setup	8
3	General Concepts.....	10
3.1	Flipwell/GP	10
3.2	Supported Netlisters.....	10
3.3	Inherited Connections	11
3.4	Layout PCells	12
3.4.1	Selecting Rule Sets	12
3.4.2	Default Rule Set Setup	14
3.4.3	Available Rule Sets.....	17
3.4.4	RuleSet lead by CDF	17
3.5	SKILL Utilities	18
3.5.1	Check/Update CDF Parameters	18
3.5.2	Freeze PCell Instances in Cell View (DK versions before 2.7)	18
3.5.3	Freeze PCell Instance in Library (DK versions before 2.7)	19
3.5.4	Compatible mode.....	20
3.5.5	Action of "par"	21
3.5.6	Action of "s"	22
3.6	Min/Max Value management	22
3.6.1	Fet.....	22
3.6.2	Resistors.....	23
3.6.3	Diode.....	24
3.6.4	ESD Diode	24
3.7	Prevent Tiling for CMOM	24
3.8	New switch to support specific layout configuration.....	25
3.8.1	BP extension on active	25
3.8.2	CA spacing 126	27
3.8.3	EXTENDED_T3	29
3.8.4	NW_EG_extensions	30
3.8.5	Extended_EG	33
3.8.6	NW_Extension_OD.....	34
3.9	DFM Pcell.....	36
3.10	GUI for cdf management.....	38
3.10.1	Parameters for schematic view	38
3.10.2	Interface for pcell parameters	40
3.11	Description of mosfet ruleSets and CDF	41
3.11.1	Gate Length adder.....	41
3.11.2	Gate Contact.....	44





3.11.3 Gate Spacing	45
3.11.4 HSSOI and BP Extension	47
3.11.5 Accurate mode	52
3.11.6 Simulation Option Expert	53
3.11.7 Advanced Matching Simulation	53
3.11.8 Nsig parameters	54
3.11.9 Mismatch	54
3.12 Fluid Guard Ring	55
3.13 Backannotation	58
3.14 VXL Connectivity Extractor	59
3.14.1 Strong connectivity extraction:	59
3.14.2 Soft/Substrate connectivity extraction:	60
3.15 Description of constraint groups in OA techfile	61
3.15.1 Design Kit default constraint group	62
3.15.2 Virtuoso default constraint groups	62
3.15.3 Other constraint groups for specific purposes	63
3.15.4 Foundry and rules in constraint groups	63
4 Devices	65
4.1 New devices in DK 1.2	65
4.1.1 sealringCS (crack sensor)	65
4.2 New devices in DK 1.1	65
4.2.1 Varactor NMOS GO1 (ST_C32_addon_DP)	65
4.2.2 esd low capacitors (cmos32lp)	66
4.3 New devices in DK 0.9	66
4.3.1 Inductances Iohq High Performances	66
4.3.2 Transmission Lines	67
4.4 New devices in DK 2.9	67
4.4.1 EDMOS	67
4.4.2 OPPPCRES Low Cost	70
4.4.3 HLVT mosfet	74
4.4.4 SRAM SP126	81
4.5 MOS RF	85
4.5.1 Supported Devices	85
4.5.2 Symbol	85
4.5.3 Pcell Parameters	86
4.5.4 Netlist Formats	88
4.5.5 Level of simulation	91
4.5.6 Layout view	91
4.6 MOSFET	92
4.6.1 Supported Device Types	92
4.6.2 Symbol	93
4.6.3 Inherited Connections	93
4.6.4 Device Parameters	93
4.6.5 Netlist Formats	98





4.6.6 Layout PCell	99
4.7 Resistors.....	101
4.7.1 Supported device types	101
4.7.2 Symbol.....	101
4.7.3 Inherited Connections.....	102
4.7.4 Device Parameters	102
4.7.5 Netlist Formats.....	103
4.7.6 Layout PCell	104
4.8 Capacitors	105
4.8.1 Supported device types	105
4.8.2 Symbol.....	105
4.8.3 Inherited Connections.....	105
4.8.4 Device Parameters	106
4.8.5 Netlist Formats.....	107
4.8.6 Layout PCell	108
4.9 SRAM	109
4.9.1 Supported device types	109
4.9.2 Symbol.....	110
4.9.3 Inherited Connections.....	110
4.9.4 Device Parameters	110
4.9.5 Netlist Formats.....	112
4.9.6 Layout PCell Rule Sets.....	112
4.10 Diodes	113
4.10.1 Supported device types	113
4.10.2 Symbol.....	113
4.10.3 Device Parameters	114
4.10.4 Netlist Formats.....	114
4.10.5 Layout PCell Rule Sets.....	115
4.11 BIPOLAR	116
4.11.1 Supported device types	116
4.11.2 Symbol.....	116
4.11.3 Device Parameters	116
4.11.4 Netlist Formats.....	117
4.11.5 Layout PCell Rule Sets.....	117
4.12 ESD	118
4.12.1 Supported device types	118
4.12.2 Symbol.....	119
4.13 ESD Hierarchical Cells	120
4.13.1 Supported device types	120
4.13.2 Symbol.....	121
4.13.3 Device Parameters	121
4.13.4 Netlist Formats.....	123
4.13.5 Layout view	124
5 ST_C32_addon_DP	125





5.1	Main purpose/content.....	125
5.2	Devices List in ST_C32_addon_DP	125
5.3	Sealring 10M	126
5.3.1	CDF parameter description:.....	128
5.4	STLogo	128
5.5	CMOM device 10M (6U1x_2U2x_2T8X).....	128
5.5.1	Symbol used:	130
5.5.2	Netlist:	131
5.5.3	CDF parameters description.....	131
5.6	NDriftOTP	132
5.6.1	Symbol used:	133
5.6.2	Netlist	133
5.6.3	CDF Parameters.....	134
5.7	Egpcap	135
5.7.1	Symbols	135
5.7.2	Netlists	135
5.7.3	Pins	135
5.7.4	CDF parameters	135
5.8	Varactors: cvar_eg, cvar_eg_diff, cvar_eg_atto	137
5.8.1	Symbols and pins	138
5.8.2	Netlists	138
5.8.3	CDF parameters	139
5.9	OTP capacitor	140
5.9.1	Supported devices:	140
5.9.2	Symbols	140
5.9.3	CDF Parameters.....	140
5.9.4	Netlist Formats.....	141
5.10	Metal Resistors.....	141
5.10.1	Supported device types :	141
5.10.2	Symbol:	142
5.10.3	Device Parameters:	142
5.10.4	Netlist Formats.....	143
5.11	Fringe Capacitors	143
5.11.1	Supported device types	143
5.11.2	Symbol.....	144
5.11.3	Device Parameters	144
5.11.4	Netlist Formats.....	144
5.11.5	Layout PCell	145
6	ST_C32_addon_AMS	146
6.1	Main purpose:.....	146
6.2	Devices List in ST_C32_addon_AMS	146
6.2.1	Cmim16acc.....	147
6.2.2	Inductances	150
6.2.3	Transmission Lines.....	154





Devices 159



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1 Introduction

This document describes the Cadence device library for the 28FDSOI process. The device library provides the technology file, symbol and layout views for full-custom circuit design within the Cadence Design Framework II.

The device library supports the Cadence IC-6.1.7 (OpenAccess) release. It has been created and tested with IC 617 version 06.17.721. Former IC versions are no longer supported.





2 Installation

2.1 Delivery Contents

The device library package has following directory structure:

Lib Core	\$DKITROOT/DATA/LIB/lib/6U1x_2U2x_2T8x_LB/cmos32lp
Lib Addon DP	\$DKITROOT/DATA/LIB/lib/6U1x_2U2x_2T8x_LB/ST_C32_addon_DP
Lib Addon AMS	\$DKITROOT/DATA/LIB/lib/6U1x_2U2x_2T8x_LB/ST_C32_addon_AMS
Lib Addon MMW	\$DKITROOT/DATA/LIB/lib/6U1x_2U2x_2T8x_LB/C28FDSOI_MMW_10ML
Doc	\$DKITROOT/doc

Table 1: Device library directory structure

The device library is available with two BEOL layer stacks: 6U1x_2U2x_2T8x and 6U1x_2T8x by providing Cadence technology files for this stack. All the technology files are located in the technology library directory cmos32lp_Tech under the path: \$DKITROOT/DATA/LIB/lib/<BEOL_STACK>/cmos32lp_Tech

2.1.1 Libraries installed in the Design Kit

Under the path \$DKITROOT/DATA/LIB/lib/<BEOL_STACK> we find the following libraries:

- **cmos32lp**: library inherited from 32n technology
- **ST_C32_addon_DP**: previous ST specific library. All specific files of this library have been added in the DK in order to keep the same behavior we had in the DKAddon_DP. This library contains ST specific devices and some elements of layout finishing (STLogo, sealring)
- **ST_C32_addon_AMS**: contains specific devices for RF design. Those devices are ST-specific and so they have all the ST specific features as ctkrev version support.
- **C28FDSOI_MMW_10/8ML**: library containing specific MMW devices such as custom mom_rf, macromosrf and mesh generator.
- **cmos32lp_Tech**: contains all the technology informations (layers, vias, layerMap...)

All the libraries and the skill files associated are loaded directly by the designKit.

2.2 Setup

In order to have access to designKit, you have to load the designKit whith IC 617 in your environment. Then before starting Virtuoso, create a cds.lib (your library manager file) file in your working directory.

In order to load all the libraries of the Design Kit, add this line to your cds.lib:
\$UCDPRJDIR/.ukcds5/\${UK_CDS_PREFIX}cds.lib





Where \$UCDPRJDIR represents the current path of your workingDir and \${UK_CDS_PREFIX} represents the user trigram. If you don't set this variable in your environment, first start Cadence which will create the ./ukcds5 directory and get back the name of the file *cds.lib to load the file in your cds.lib.

This file ./ukcds5/\${UK_CDS_PREFIX}cds.lib is used to load all the libraries defined in the design kit.

Once the DesignKit is properly setup, you can create a library for your own design.

This library must be attached to the core DK library "cmos32lp" in order to load all needed features (for example callbacks and display of layers).

Thanks to the Virtuoso feature incremental techfile, the core library "cmos32lp" is already attached to the techlib "cmos32lp_Tech".

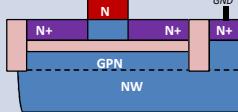
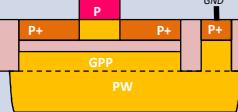
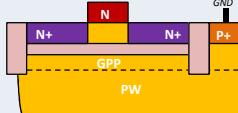
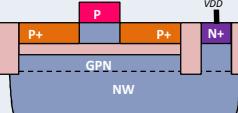
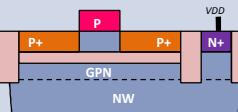
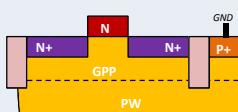
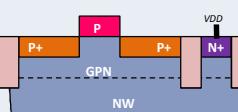


3 General Concepts

3.1 Flipwell/GP

All the supported devices have the following architecture:

MOS devices in 28FDSOI technology

Category	Architecture	NMOS	PMOS	Devices
LVT MOS devices (HSSOI)	Flip well			- LVT GO1/GO2 - ESD LVT MOS on SOI
RVT MOS devices	Flip GP			- RVT GO1/GO2 - ESD RVT MOS on SOI
SRAM array	Flip GP			- SRAM LL
Hybrid devices	Flip GP			- ESD MOS on Bulk

1

Table 2: Devices structures

3.2 Supported Netlisters

The device library provides stop views and siminfo CDF setup for following netlisters:

Name	Netlister	Siminfo/Stop View
CDL	Cadence auCdl	auCDL
HSpice	Cadence hSpice	hspiceD
Eldo	Cadence Eldo	eldoD
Spectre	Cadence Spectre	spectre



AMS	Cadence AMS	ams
Advance MS	Advance MS	eldoD

Table 3: Supported netlisters

3.3 Inherited Connections

The device library supports Inherited Connections to minimize the amount of power supply wiring in schematics.

All device cells, which have a bulk pin, come in 2 variants:

- Symbol view with an explicit bulk pin
- Symbol view without a bulk pin but a netExpression definition in the stop views

Cells with an explicit bulk pin have a “_b” postfix, e.g. “pfet_b”. The corresponding cell using a netExpression for the bulk pin is named e.g. “pfet”.

Table 4 contains all netExpressions defined throughout the device library.

Regular Devices	Bulk netExpression	Flipwell Devices	Bulk netExpression
NFET	[@lSup:%:VSS!]	NFET	[@lSup:%:VSS!]
PFET	[@hSup:%:VDD!]	PFET	[@hSup:%:VSS!]
Resistors	[@resbulk:%:VSS!]	Resistor	[@resbulk:%:VSS!]
Capacitors	[@capbulk:%:VSS!]	Capacitors	[@capbulk:%:VSS!]

Table 4: Summary of netExpressions defined in the device library

The device library provides additional power supply cells (category “supply”), which are useful if the complete power supply connectivity shall be established using Inherited Connections. The power supply cells just automatically add a predefined netExpression to the attached wire. Table 5 lists these power supply cells.

Power supply cell	netExpression
hSupCell	[@hSup:%:VDD!]
lSupCell	[@lSup:%:VSS!]

Table 5: Power supply cells and default netExpressions

A typical application of Inherited Connections is shown in Figure 1. This approach avoids global nets and still allows connecting the power supply nets of the cell to any desired net in the upper design hierarchy.



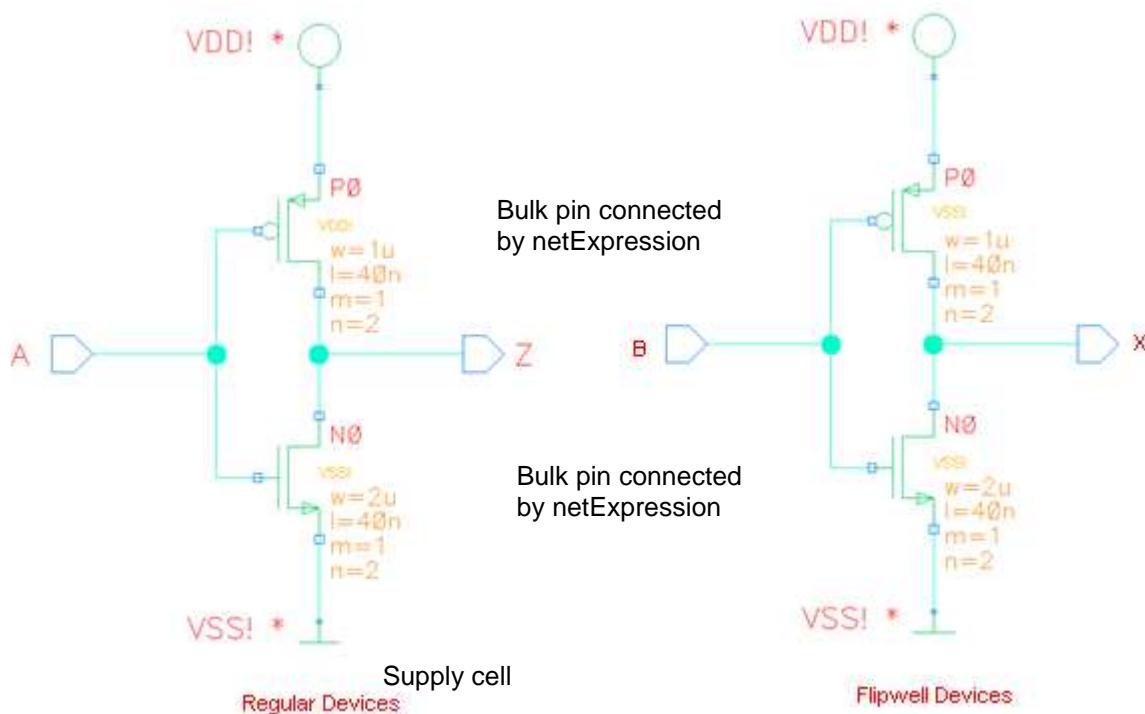


Figure 1: Typical usage of Inherited Connections

3.4 Layout PCells

3.4.1 Selecting Rule Sets

This part is kept for compatibility with 32lp in term of designs and design habits. But careful all the RuleSets aren't qualified by STMicroelectronics and come from ISDA only. So the use of ruleSet are NOT supported by STMicroelectronics as it can introduce some design errors. The use of this feature is accessible by using the button "Enable Editing Rule Sets".

The layout PCells support rule sets for selecting layout variants, e.g. for selecting recommended design rules. Rule sets are selected on instance base. It is possible to define default rule sets, which are automatically used when creating new instances.

Rule sets are defined by the instance parameter *Rule Sets* as a string of rule set names separated by a '+' character. The rule selection is supported by a rule browser, which can be opened via the button *Select Rule Sets*:



Figure 2: PCell rule set related parameters

The rule browser shows all available rule sets. The list of rule sets may have entries depending on devices type and device model. These rule sets are described in the documentation of the individual devices.

Within the rule browser 0, 1 or more rule sets can be selected by dragging or using the Shift/Ctrl key for multiple selections. When hitting the OK button of the rule browser all selected rules will be written to the *Rule Sets* parameter field.



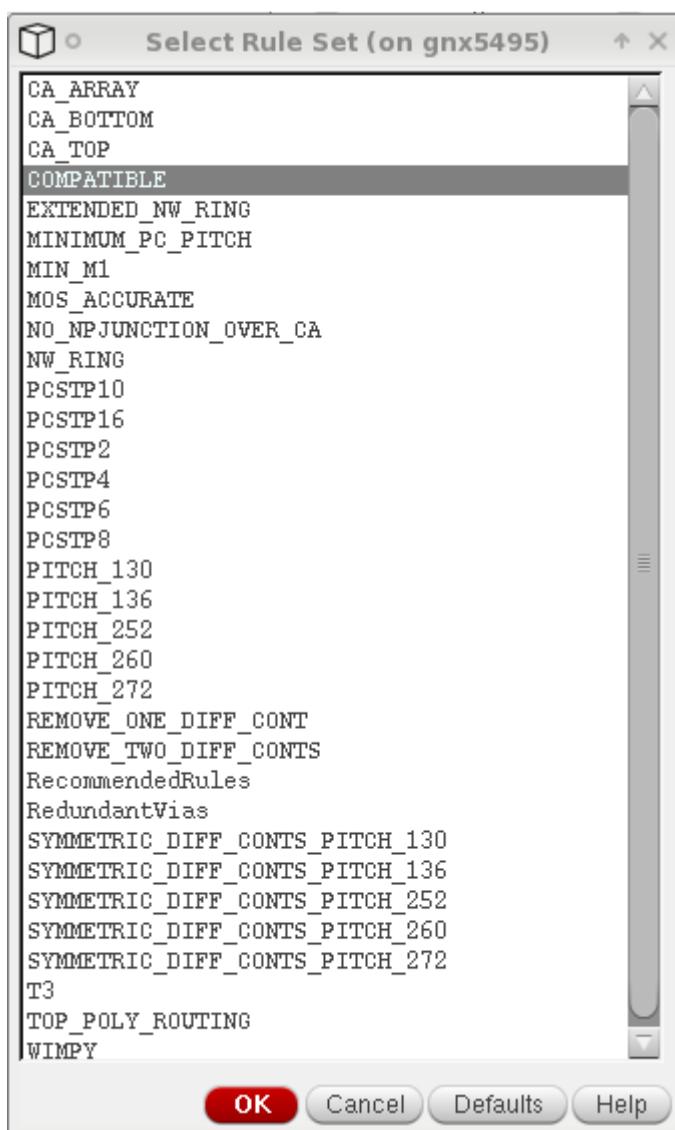


Figure 3: Rule set selection browser

3.4.2 Default Rule Set Setup

The device library offers 2 methods for defining default PCell rule sets:

- Device library installation specific setting: A list of default rule sets may be defined as a library property. In case of a read-only device library installation this method offers a fixed preset of rule sets, which cannot be altered by the user. This setting is not instance specific and is automatically applied to all evaluated PCells for new and existing instances.
- Virtuoso session specific setting: Default rule sets can be defined globally and specifically for devices. The setting can be saved permanently in an environment variable. The user has always full control about these settings. In contrast to the previous method this setting is instance specific and applies to newly created instance only.

3.4.2.1 Installation Specific Setting

Instructions for installation specific default PCell rule set setup:





1. Build a string of rule set names concatenated by a '+' character, e.g. "MIG+RecommendedRules".
2. Create a string property named GLOBAL_PCELL_RULESETS on the library and use the PCell rule set string from 1. as value (see Figure 4).
3. Restart Virtuoso.

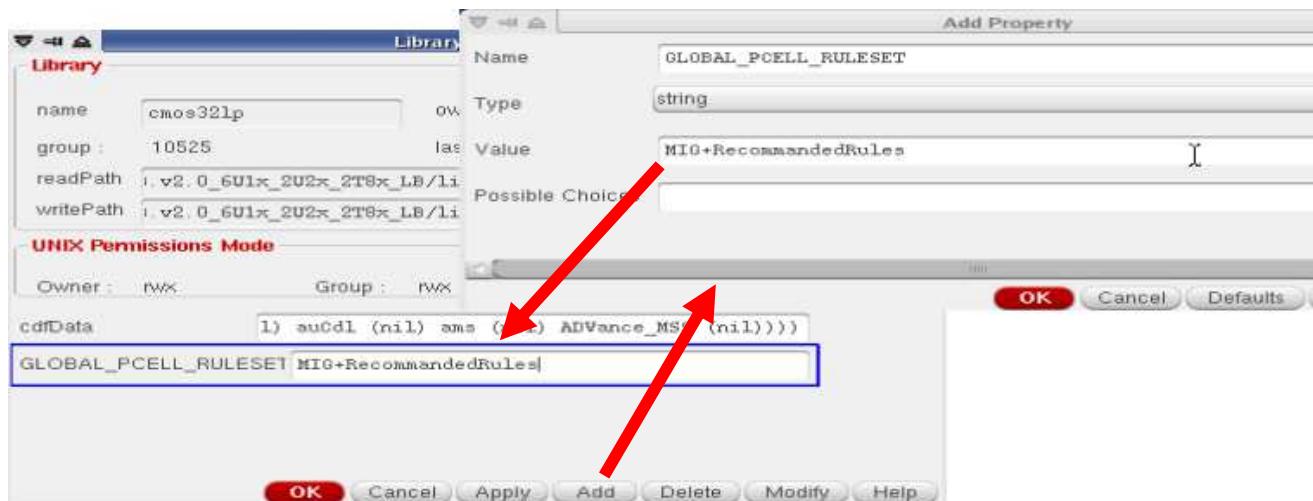


Figure 4: Setup of installation specific PCell rule set defaults

3.4.2.2 Virtuoso Session Specific Setting

This utility allows setting the default rule sets to be used when creating new PCell instances. Rule sets select a different design rule set for the PCell layout generator. The default rule sets can be set for all PCells or for individual PCells. When Virtuoso Layout Editor is launched, select: "PDK -> cmos32lp -> Select Default Rule Sets..." then the following form is launched:





Figure 5: Default rule set definition form

Click on the **all** line to select the defaults for all PCells or click on the individual PCell name to set the default just for this individual PCell. After clicking on a line the *Rule Select* form will appear:



Figure 6: Selected Rules Set

Here, you can select 0, 1 or more rule sets (use Shift/Ctrl key for multiple selections). Hit **OK** to accept the selection.

Hit **OK** in the *Select Rule Sets* form to make the selected rule sets active for the current virtuoso session. For permanently saving the selected rule an environment variable must be set. In order to do that, you only have





to press OK in the previous window, then the following form will appear, which gives you the right variable to set:

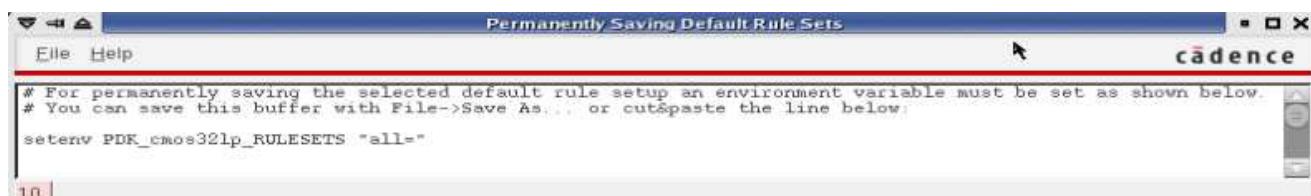


Figure 7: Default rule set definition form

3.4.3 Available Rule Sets

Following rule sets are available for all devices.

RecommendedRules	Selects all recommended rules marked with _R in the design manual.
Compatible	This Rule set is used to apply the Compatible Mode (see 4.5.3) on devices. This mode force the distance Poly-Contact in mosfet to be identical to the DK 32lp, for a clean migration.

Table 6: Common PCell rule sets

The others rules sets are device specific.

3.4.4 RuleSet lead by CDF

When you customize your instantiated device by using cdf, the change in the pcell is mainly done by changing the ruleSet used. So you can use only the cdf user interface to set all the proprieties you want for your instantiated device, it will automatically select the right set of ruleSet.

In the v2.3 this aspect is wildly used in the pcell. We have implemented new ruleSets to manage the pcell and we have defined a new interface to simplify the choices in the cdf.

All the new ruleSets and the new interface for CDF are described in part 4.





3.5 SKILL Utilities

The device library provides a couple of SKILL utilities, which are located in the window menu *PDK->cmos32lp in the Virtuoso Layout Editor.

3.5.1 Check/Update CDF Parameters

This utility performs automatic updates on device instance parameters (CDF parameters), which may be required when switching to a new version of the device library. Usually, electrical parameters change, which require recalculation of resistor and capacitor parameters.

For more information on the 'Check/Update CDF' functionality, please read the documentation "DesignKitMigration.pdf".

3.5.2 Freeze PCell Instances in Cell View (DK versions before 2.7)

WARNING: This functionality is no more available from version 2.7, it is replaced by the functionality update Pcell.

You can continue use frozen pcells from previous version in your design 2.7 but if you need to modify them, you will have remove it and re-instantiate a new pcell.

For more information on the 'Check/Update PCELL' functionality, please read the documentation "DesignKitMigration.pdf".

For version before 2.7, this utility can be used to freeze the layouts of PCell instances in the current cell view. The layout of frozen instances will not change if the underlying layout generator changes (e.g. when updating to a new device library version or Cadence version). The frozen layout data is stored in the current cell view. Thus, data management operations (check-in, check-out) will correctly also manage the layout of the frozen PCell instances.

After invoking the utility following form will appear:





Figure 8: PCell freeze utility

The table in the lower part of the form gives an overview over all PCell masters on which a freeze operation will be performed. It shows either all or selected freezable PCell masters depending on the *Freeze* radio button. If the selection was changed while the form was already open, the *Update Table Data* button can be used to update the table contents. Each line informs about the number of unfrozen and frozen instances of a PCell master. Any freeze operation will only be performed on instances of selected PCell master table entries. By default all table entries are selected.

The *Action* radio button controls if a freeze or an unfreeze operation will be performed. The actual operation is executed by hitting the *Ok* or *Apply* button of the form.

Hints:

- The freeze utility can only freeze PCell instances of the device library. It cannot freeze PCells of other libraries.
- Frozen PCell instances still require the device library.
- Parameter changes on frozen PCell instances have no effect. You have to unfreeze the instance first. This situation is not directly indicated to the user, except that the layout does not change if parameters are modified.
- The layout data of frozen instances is stored in the current cell view and will increase the memory and disk size of the cell view. No additional layout views will be created.

3.5.3 Freeze PCell Instance in Library (DK versions before 2.7)

This utility allows to freeze PCell instances for selected views in a design library. The freeze process is the same as described in section 3.5.2.





The utility is invoked via `*PDK->cmos32lp->Freeze PCell Instances In Library...` (`*PDK->cmos32g->Freeze PCell Instances In Library...` or `*PDK->cmos28lp->Freeze PCell Instances In Library...`). Following form will appear:

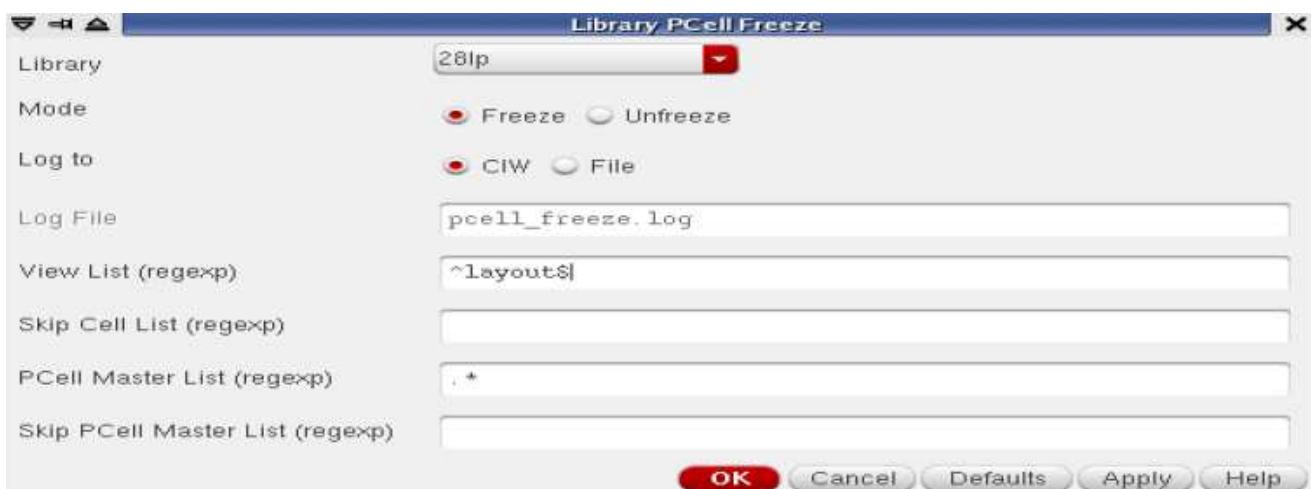


Figure 9: Freeze PCell Instances in Library GUI

After selecting the design library to operate on, the PCell freeze process can be started by pressing **OK** or **Apply**.

Explanation of form fields:

Library	Select library to operate on.
Mode	Freeze : Freeze PCell instances so that they become invariant to PDK changes Unfreeze : Revert freeze process, PCell instances will be re-evaluated
Log to	CIW : Action report will be written to CIW log window File : Action report will be written to a separate log file. The contents of the log file will be automatically displayed
Log file	Specify log file path. Only used if Log to File is selected.
View List	List of regular expression specifying view names to operate on.
Skip Cell List	List of regular expression specifying names of cells to exclude from the process.
PCell Master List	List of regular expression specifying device library cell names to freeze/unfreeze.
Skip PCell Master List	List of regular expression specifying device library cell names to ignore for freeze/unfreeze.

3.5.4 Compatible mode

For moving a design from another technology (32lp, 28lp) to this design kit, you can have to use this mode. For example from 32lp to 28FDSOI, distance Poly-contact in the mosfets has changed, so all the design will be modify and has to be re draw. By using this mode, you force the design to keep the 32lp distance values.

So after invoking the utility, `PDK->cmos32lp->Add Compatible Parameters...`, following window appears:



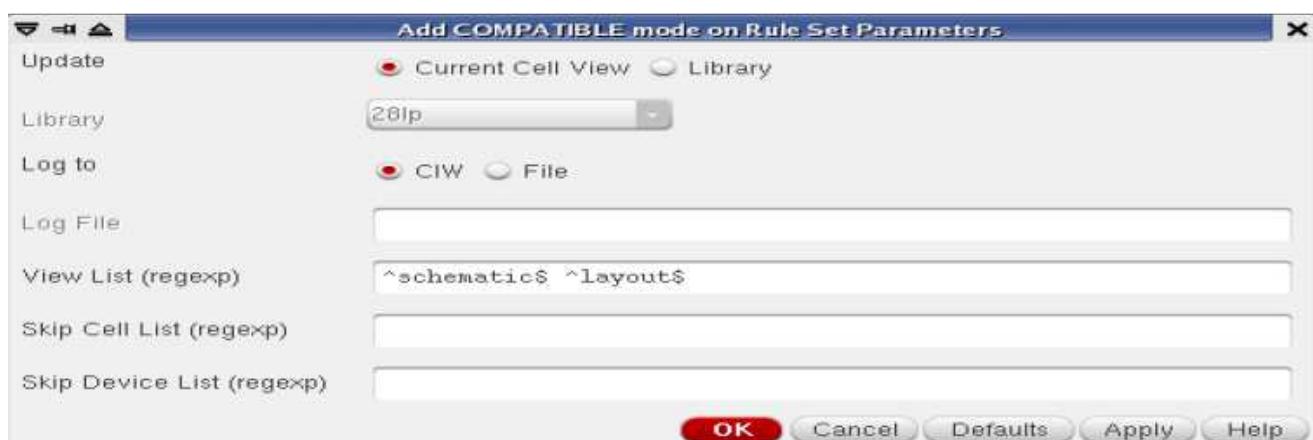


Figure 10: Compatible Mode

You can also use the compatible mode by setting the rule set “Compatible” for a complete library or some devices...

The following table details the different parameter to fill in:

Update	Current Cell View: action will be performed on currently active cell view only Library: action will be performed on all cells of a library
Library	Select library to operate on. Only used when applying this mode on a complete library.
Log to	CIW: Action report will be written to CIW log window File: Action report will be written to a separate log file. The contents of the log file will be automatically displayed
Log file	Specify log file path. Only used if Log to File is selected.
View List	List of regular expression specifying view names to operate on. Only used when applying compatible mode on a complete library.
Skip Cell List	List of regular expression specifying names of cells to exclude from the update process. Only used when updating a complete library.
Skip Device List	List of regular expression specifying device library cell names to exclude from the update process.

3.5.5 Action of “par”

The parameter “par” indicates the number of parallel resistive POLY shape in the device.

When “par” is modified:

- In Geometric mode: the resistor value is kept, W and L are updated to fit the resistor value
- In Electric mode: W and L are conserved and the resistor value is updated



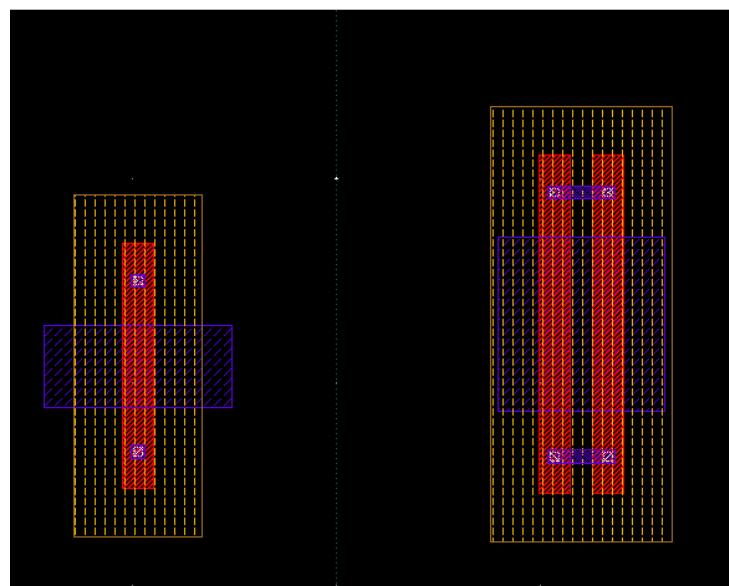


Figure 11: illustration par =1 and par =2 for resistors in geometric mode

3.5.6 Action of “s”

Exactly the same behavior than “par” but this parameter put the POLY shapes in serie and not in parallel.

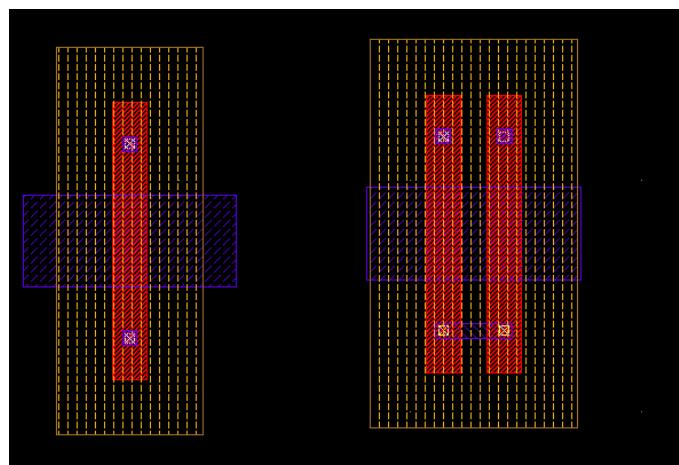


Figure 12: illustration s=1 and s=2 in electric mode

We can notice that this layout looks like pretty much as the one shown for “par” (fig 13). The main difference is the connection of the POLY shapes, which define parallel or serie shapes.

Note that the parameter ‘s’ is netlisted ‘s_rename’ for hspice, due to a limitation of this simulator (‘s’ is a reserved key word for scaling purpose).

3.6 Min/Max Value management

3.6.1 Fet

The min values are defined by the models and are specific for each type of devices.



The max values concerning the mosfets are defined by the models in term of finger width, not in term of total width.

The DRM defines 2 sorts of limitations for maximum values:

- The maximum gate area by finger which limits both length and width:

132	-	Gate maximum area (μm^2 , outside UPSIZE)	\leq	38.661
-----	---	---	--------	--------

- The maximum width is also limited by finger by the maximum width of the diffusion RX:

50b	-	RX maximum width, outside UPSIZE	\leq	35
-----	---	----------------------------------	--------	----

And the models also define maximum values of length and widths as 35um.

That's why the maximum L and W in fets is 35um.

As the dimension w_finger is defined by: $w_{\text{finger}} = w_{\text{total}} / (\text{nb_finger} * \text{gateSplitStripes})$, the numbers nb_finger and gateSplitStripes are also limited by the both previous constraints.

For a w_total given (*TotalWidth* mode), the minimum values of these parameters are limited by the w_min value of the device and the maximum values are limited by the maximum finger width (35u) of the device. If wrong values of gateSplitStripes and nb_finger, are given, they are recalculated to be at limit of the use of the device.

We don't put any limitation on the total width only because that kind of limitation will limits the number of possible configuration. This dimension must be limited by other constraints related with the design. Anyway w_total is still limited depending on the limitations of the others parameters.

We also don't forbid entries to be *string* values in order to permit the parameterization of the netlist, which is widely used in ST divisions. In this case, equations based on parametrized values are netlisted.

Also in some cases we use the functions pPar or iPar in the cdf entries in order to propagate one parameter from an entry to another, so it is impossible to forbid the use of string entry for a numeric parameter.

3.6.2 Resistors

3.6.2.1 Min values

The models limit the minimum values for resistor to 150n of width and 400n of length. When a lower value or an empty entry is given, the minimum values are set and the value is recalculated. This check works in both mode *Geometric* and *Electric*.

CDF Parameter	Value	Display
Description	ion OP P+ Poly resistor	off
Dimension by Geometry	<input checked="" type="checkbox"/>	off
value	3.30753K Ohms	off
Stripe Width	150n M	off
Stripe Length	400n M	off

3.6.2.2 Max values

The maximum values for resistors are : w=10u and L = 100u. In *Geometric* mode, if any superior values are given, the maximum are set and the value is recalculated. In *Electric* mode, the process is the same but





depending on "ser" and "par" if you enter a too big resistor value, the maximum value of length can be overtaken.

Description	ion OP P+ Poly resistor	off
Dimension by Geometry	<input checked="" type="checkbox"/>	off
value	10.3137K Ohms	off
Stripe Width	10u M	off
Stripe Length	100u M	off

3.6.3 Diode

Only minimum values are defined by models right, so there isn't any check yet on maximum values.

Area, perimeter, Width and Height are limited to the following values, when a lower value or an empty value is entered, the minimum value is set for the corresponding entry:

W_min = 1u

Height_min = 1u

Area_min = 1p

Perimeter_min = 4u

3.6.4 ESD Diode

Depending on the device selected, the extremum values are different. For esdnndsx(_eg) devices, width and length are limited in max/min values. For esdvpnp(_eg) and esdvpnn(_eg), only width can be limited (no length available).

If the value is outside the range accepted the default value is set.

3.7 Prevent Tilling for CMOM

For physical density issue, we added a switch on the CMOM to choose to prevent or not the tiling on the CMOM.

CMOM Density Design Rules			
MOM.L.2	Maximum CMOMST;mkR length	A	100
MOM.A.1	Maximum CMOMST;mkR area	B	2500
MOM-Mx.DEN.1.1	Minimum PhysicalMetal density (applicable to all Ix, Bx, Mx as well as M1) on a 200um x 200um window centered on CMOMST;mkR		10%

All metal dummies generation is prevented under the CMOMST;mkR marker for sake of model accuracy and RF performances. Only RX and PC dummies should be generated in a regular way under the 2 pins devices.

When the switch is unactive, it will retire layers M6/B1/B2/IA/IA;exclude which forbid to tile on that levels of metal. With the switch activated, these layers are added on the pcell and the tiling is forbidden on these metal levels.





Capacitance (F)	4.436e-15
fringes on big fingers	<input checked="" type="radio"/> 0 <input type="radio"/> 1
Fingers nb in X direction	10.0
Fingers nb in Y direction	10.0
Bottom level metal	2
Top level metal	5
Metal bottom connection	2
Metal top connection	4
Width mx Finger [Meter]	1e-07
distance between 2 Mx fingers[Meter]	1e-07
Prevent tiling over and under CMOM	<input checked="" type="checkbox"/>
Post Layout extraction	-1
Description	2 pins Stacked Fringe Capacitance without shield
Use label for MOM RF Parasitic Interaction	<input type="checkbox"/>
Safe Operating Area	<input type="radio"/> 0 <input checked="" type="radio"/> 1

Figure 13: prevent tiling parameter

3.8 New switch to support specific layout configuration

The way pcells were designed by ISDA coalition is not a way that gives necessary DRC clean configuration by default.

The default configuration of pcells is the smallest possible configuration, which respects enclosures but not necessary minArea or minWidth of all the layers. These errors were considered to be fixable by the designer depending on the configuration of his design.

The idea was to create the smallest configuration to increase density integration and to let designer fix the errors of covering layers the way he wants, in order to create the best configuration to fit to the design.

Anyway, we decided to add some layout switch in order to propose some clean configuration usually used by designers.

3.8.1 BP extension on active

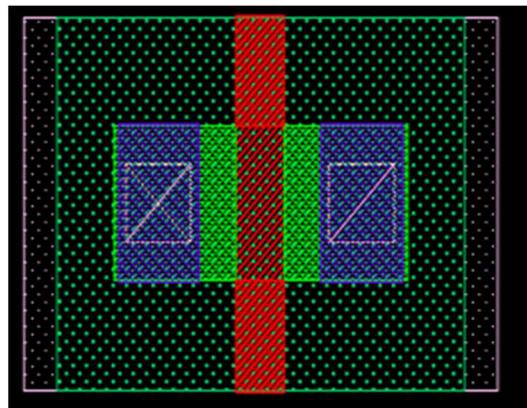
The switch “BP ext. on OD” is available only when “Robust Rules” is active.



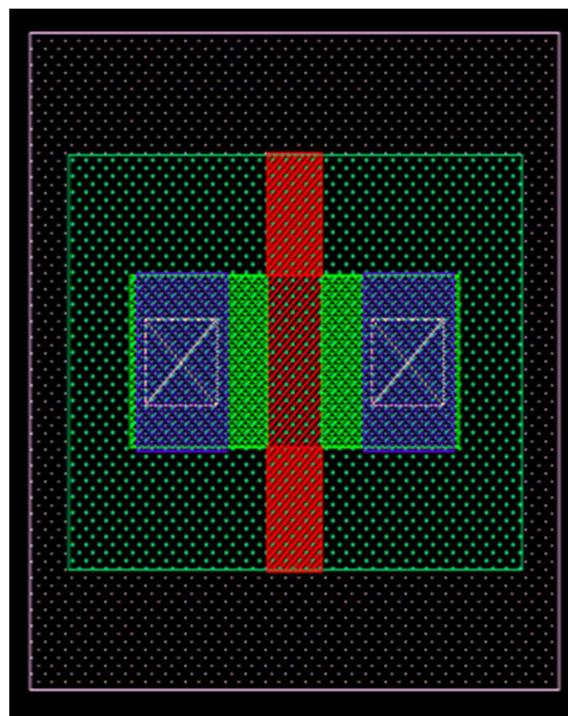


It allows to draw BP with reduced enclosures on active, compared to DFM enclosures.

Example with lvtpfet:

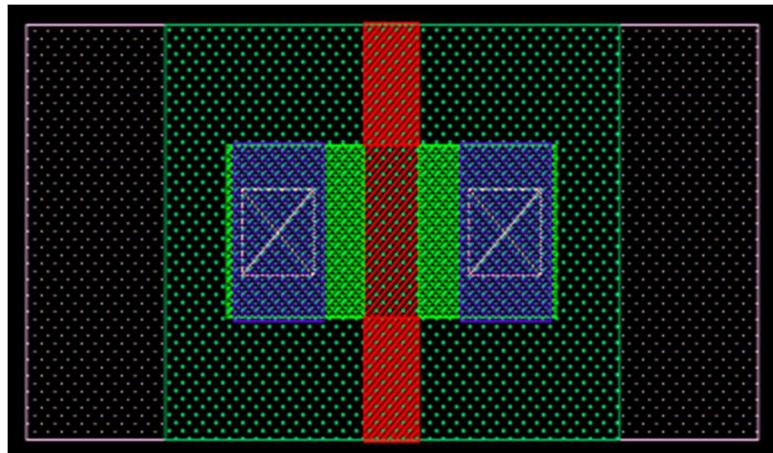


“BP ext. on OD” = None

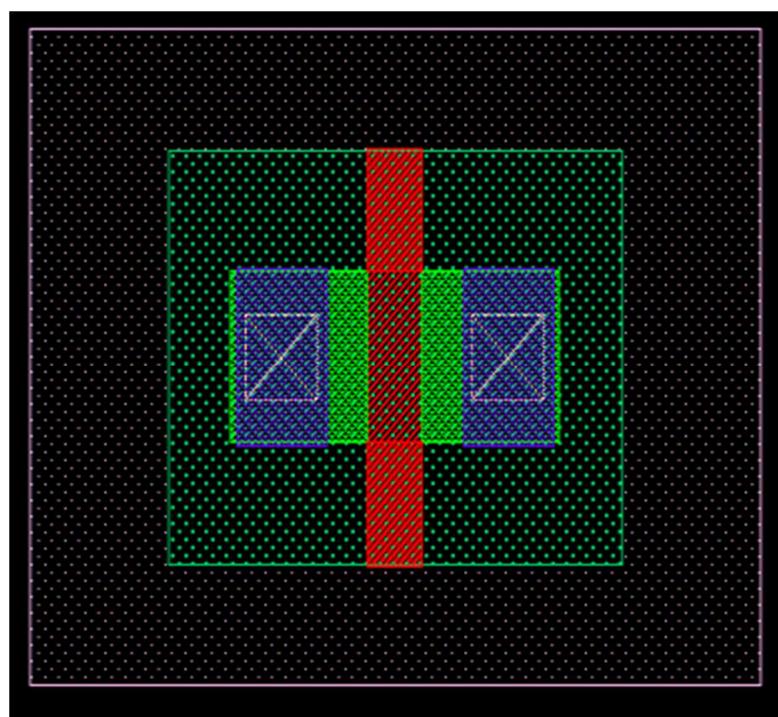


“BP ext. on OD” = Right/Left





“BP ext. on OD” = Top/Bottom



“BP ext. on OD” = Both

3.8.2 CA spacing 126

The following switch has been added to correct a DRC error which can appear in certain configurations. For mosfets used in SRAM periphery, a marker srmperi is added, in this configuration the spacing center to center between contacts must be 126nm. So when this spacing is not respected under MKR;srmperi the drc error CA.S.2 flash. The “CA spacing switch” gives the possibility to choose between 2 values of spacing (centerTocenter): 126 and 100n

Devices Name	switch	Values	ruleSet	Contact spacing center to center
All mosfets	CA_SPACING_126	On	CA_SPACING_126	126n
		OFF	nothing	100n

This switch gives the possibility to the designer to modify the spacing between contacts of the Source and the Drain. Usually the pitch used between contacts is 100nm, with this parameter it becomes 126nm:

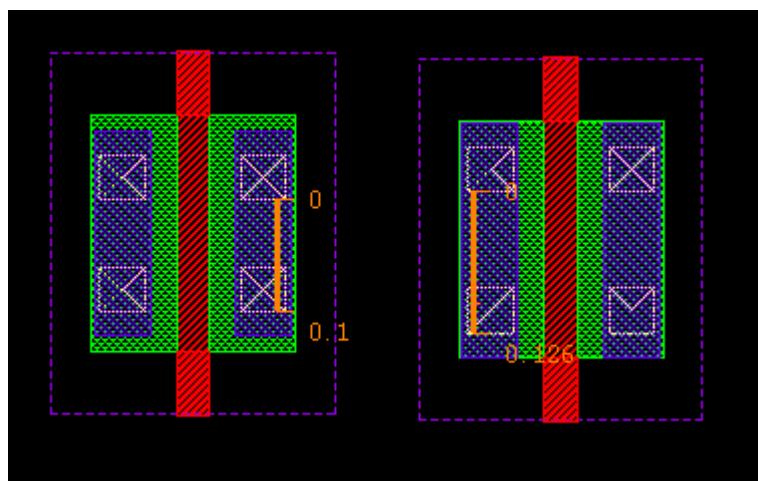


Figure 14: 2 possible configurations with CA spacing 126

When the device is too small to use this spacing of contacts, only one contact is drawn:

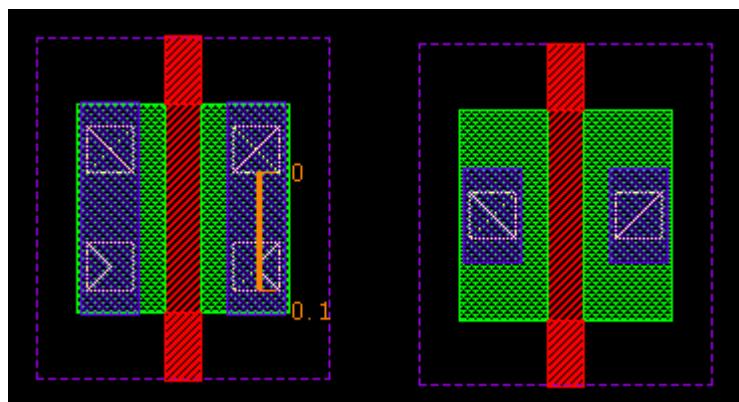


Figure 15: CA spacing too big for device width, only one contact drawn



3.8.3 EXTENDED_T3

Devices Name	switch	Values	ruleSet
Opppcres, opreres, Ivtpfet, eglvtvfet, egvlvtvfet	Extended_T3	On	EXTENDED_T3
		OFF	nothing

Table 7: Extended_T3 switch

Extended T3 was implemented to give the possibility to extend T3. When T3 is used in the device: whether “Triple Well” for the fet is activated or for the resistor, “Backpane Designation” should be at T3.

3T02	-	T3 minimum width.	\geq	1.45
B_N30	-	N3 (as generated by Boolean) minimum width.	\geq	1.45

The following pictures show the effect of this switch, on the right you have the previous configuration (option to add T3 are set), where T3 shape respects the different enclosures but not the minWidth of the metal, so designers can enlarge the T3 shape where it fits the best its design. And on the left you have a DRC clean configuration where T3 is centered on the pcell.



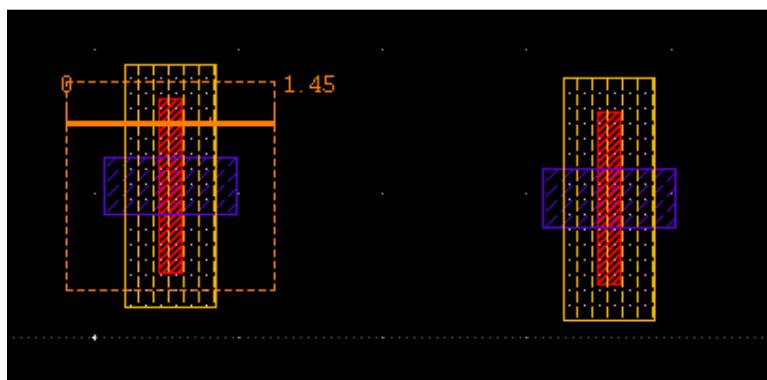


Figure 16: opppcres with and without T3 extension

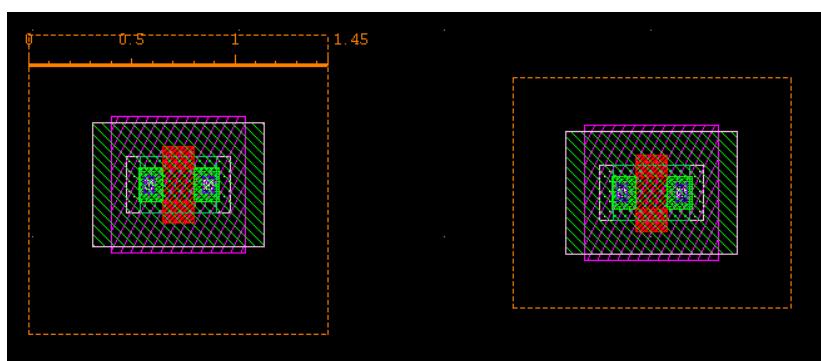


Figure 17: lvtpfet with and without T3 extension

3.8.4 NW_EG_extensions

Devices Name	switch	Values	ruleSet
Egvpfet(_b), egpfet (_b), egtdpdnw	NW_EG_extensions	None	COMPATIBLE
		NW_EG_Both_EG_BP_None	NW_Extension_EG_None_And_EG_Extension_BP_None
		NW_EG_None_EG_BP_Right_Left	NW_Extension_EG_None_And_EG_Extension_BP_Right_Left
		NW_EG_Right_Lef t_EG_BP_None	NW_Extension_EG_Right_Left_And_EG_Extension_BP_None
		NW_EG_Top_Bott om_EG_BP_None	NW_Extension_EG_Top_Bottom_And_EG_Extension_BP_None
		NW_EG_Top_Bott	NW_Extension_EG_Top_Bottom_And_EG_Extension_BP_None



		om_EG_BP_Righth_	Extension_BP_Right_
		NW_EG_Both_EG_	NW_Extension_EG_Both_And_EG_Extensi
		BP_Both	on_BP_None

Figure 18: NW_EG_Extension switch

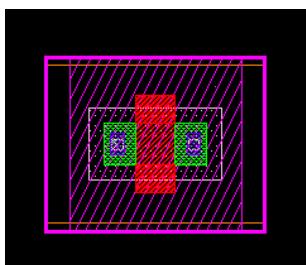
This switch propose different configuration that clean the DRC error NW.EX.1:

Additional NW Design Rules in STMicroelectronics Technology	
NW.EX.1	NW extension on EG, align if less

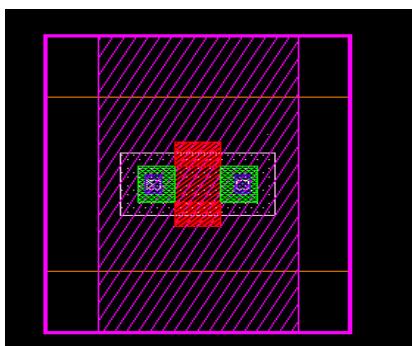
In this early access version, the switch is not yet implemented on egtdpdnw, but it will be in the official version. The switch is working fine on egvpfet(_b), egpfet(_b).

Here are the different possible configuration with that switch on an egpfet device depending on the switch value:

COMPATIBLE:

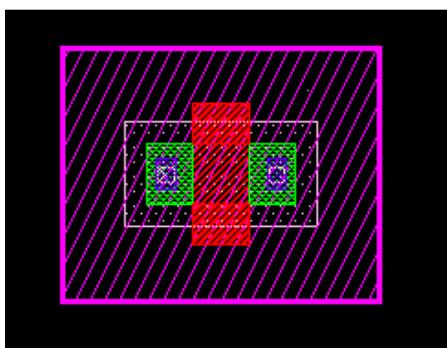


NW_Extension_EG_Both_And_EG_Extension_BP_Both:

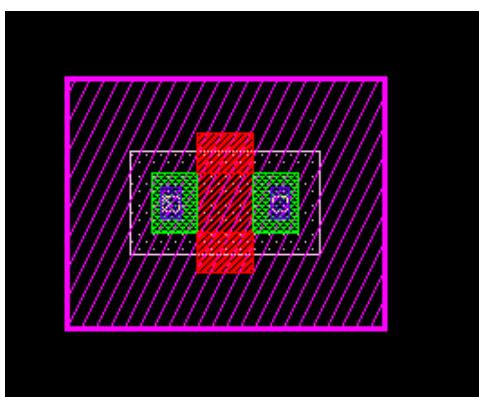


NW_Extension_EG_None_And_EG_Extension_BP_None:

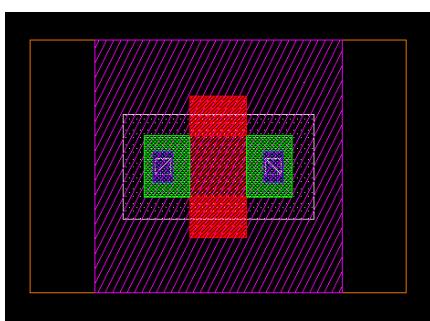




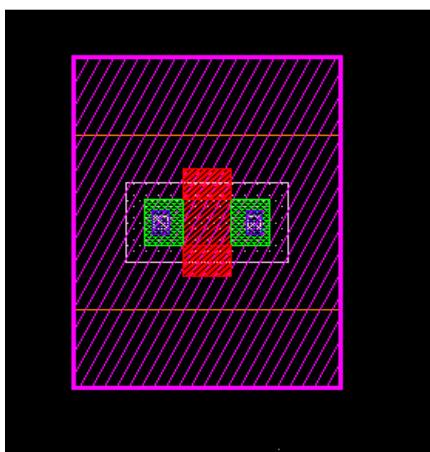
NW_Extension_EG_None_And_EG_Extension_BP_Right_Left:



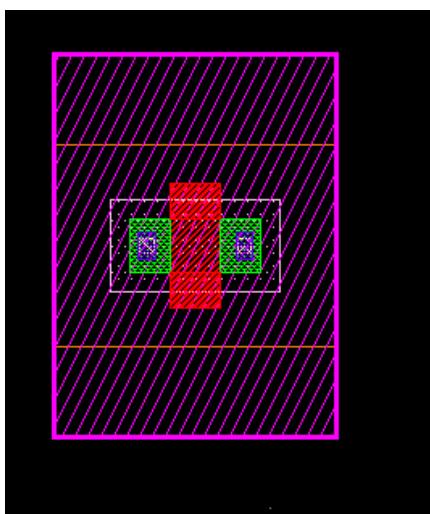
NW_Extension_EG_Right_Left_And_EG_Extension_BP_None



NW_Extension_EG_Top_Bottom_And_EG_Extension_BP_None



NW_Extension_EG_Top_Bottom_And_EG_Extension_BP_Right_Left:



3.8.5 Extended_EG

Devices Name	switch	Values	ruleSet
Egvnfet, egnfet (is available only if guardRing is activated)	Extended_EG	On	Extended_EG
Egtdndsx/Egtdpdnw		Off	nothing

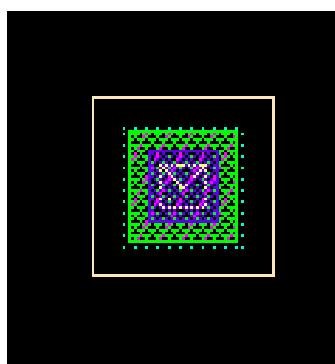
Figure 19: Extended_EG switch

This switch should fix the rule GREG34, there are several way to enlarge the EG plate depending on a design, here we choose to propose a center extension.

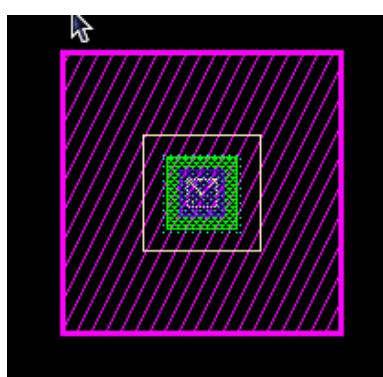


EG34	-	EG minimum overlap of NW with abutting permitted (for GP derivation).	≥	0.27
------	---	---	---	------

Default :



Extended_EG :



3.8.6 NW_Extension_OD

Devices Name	switch	Values	ruleSet
Pfet, tdpdnw, lvtlfet	NW_extension_OD	None	default
		Right_Left	NW_Extension_OD_Right_Left
		Top_Bottom	NW_Extension_OD_Top_Bottom
		Both	NW_Extension_OD_Both

Figure 20: NW_Extension switch

This switch was created to fix GR260a and NW.EN.2 error

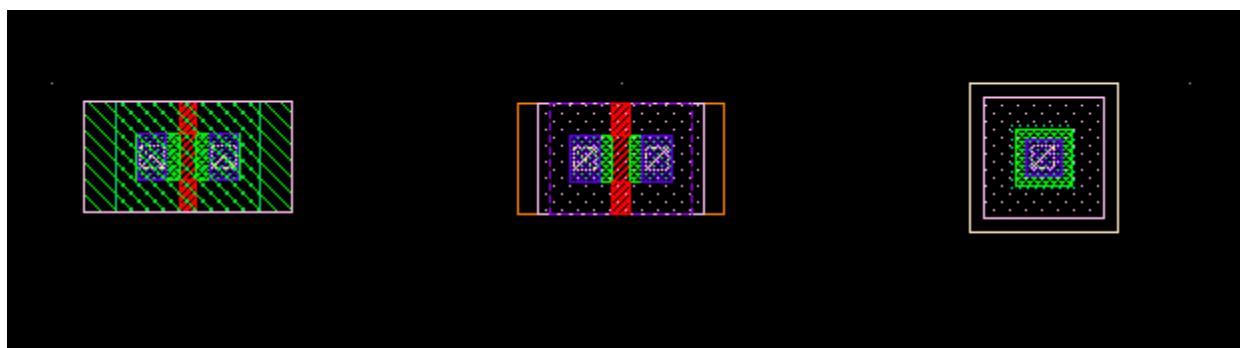
260a	-	RX p+ junction minimum within NW with at least one edge at each NW outer vertex.	≥	0.112
------	---	--	---	-------



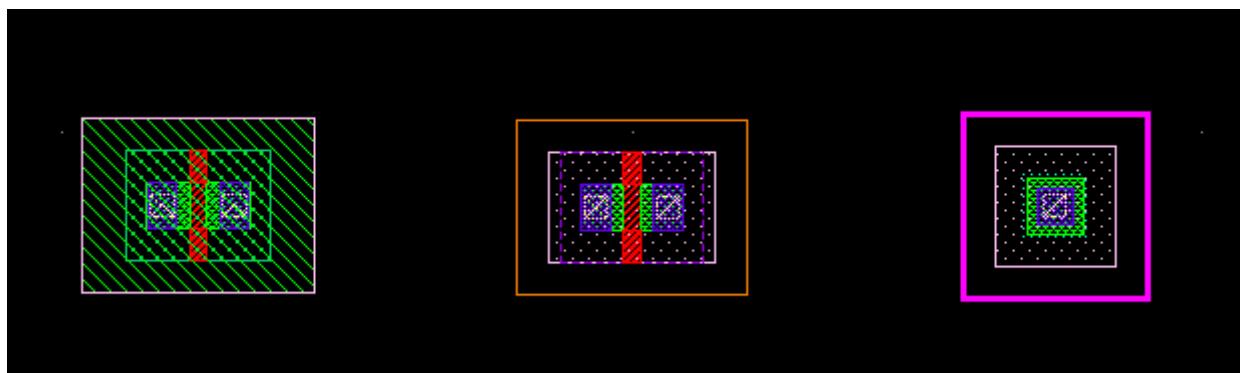


NW.EN.2	RX_N+junction enclosure by NW with at least one edge at each NW outer vertex	E2	0.112
---------	--	----	-------

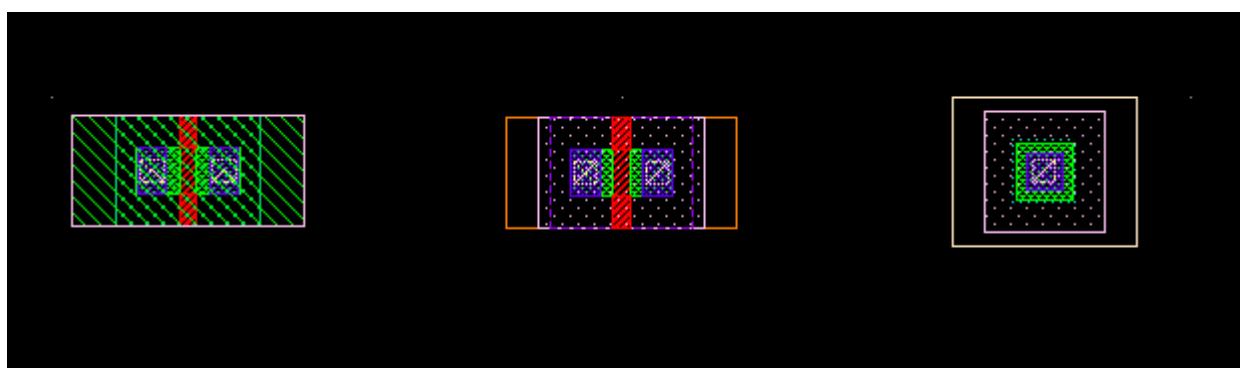
Default :



Both :

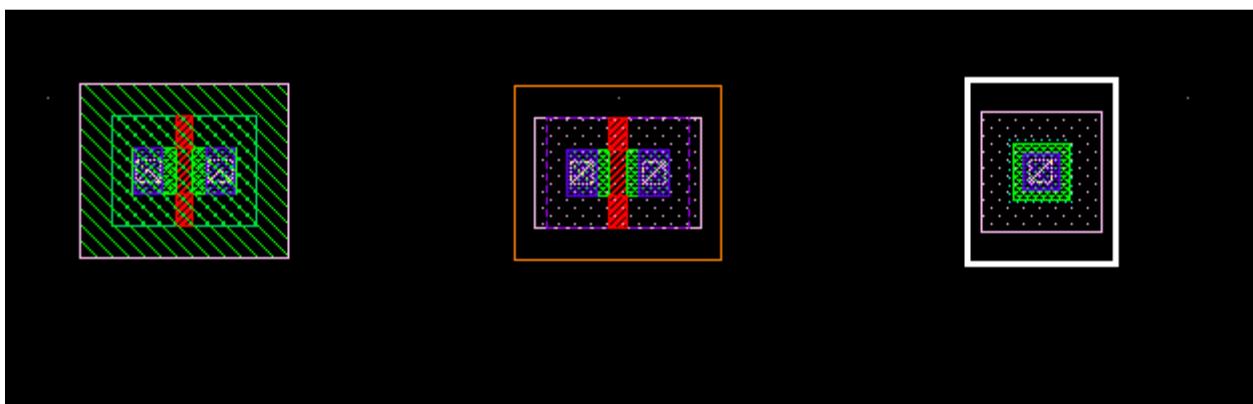


Right_Left



Top_Botom





3.9 DFM Pcell

To be compliant with the results of the SRD DFM checker, we add a switch to customize the following PCELLS:

- All CORE mosfets
- Egncap
- Diodes
- Bipolars
- RF mosfets
- Varactors

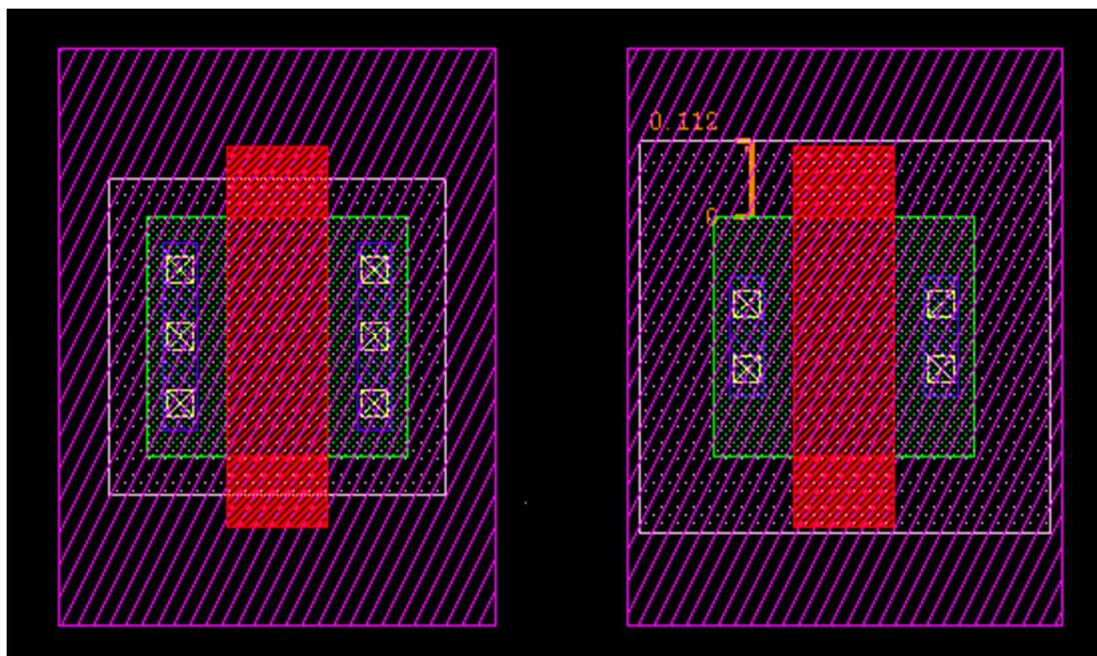
This switch is named “Robust Rules”. It applies some DFM rules on these devices and is active by default for new devices.

Device	Rule Set Name	Effect on layout
Mosfets	COMPATIBLE+DFM_RULES+REMOVE_ONE_DIFF_CONT	BP Enclosure 0.112 Vertical RX enclosure on CA is 0.03um
Egncap(_b)	DFM_RULES	Hybrid Enclosure on CA over PC is 0.60um.
Egtdndsx tdndsx	N/A	Hybrid enclosure on RX is 0.043um
Egtdpdnw	N/A	BP enclosure on RX is 0.112um

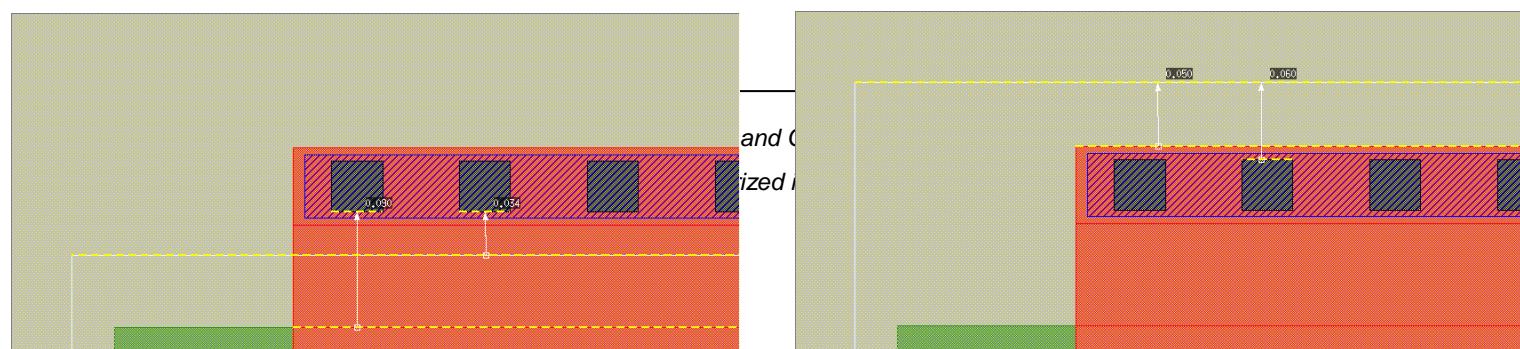


tdpdnw		
Vnpn	N/A	BP enclosure on RX is 0.112um
vppn		Hybrid enclosure on RX is 0.043um
RF mosfets	N/A	BP enclosure on RX is 0.112um Max range value for PC spacing is 126nm (except for discrete values 222nm and 242nm) PC dummies are added for all gatelength values <60nm
cvar_eg_diff	N/A	Hybrid enclosure on RX is 0.043um
cvar_eg_atto		
cvar_eg	N/A	Hybrid enclosure on RX is 0.043um Spacing RX to PC head is 0.03

Difference between DFM (left) and non DFM Egfpet:



Difference between DFM and non DFM Egncap:





3.10 GUI for cdf management

The 28FDSOI technology comes from 32lp technology, the list of parameters is in continuous improvement and cleaning is done regularly on the cdf with some factorizations of parameters.

3.10.1 Parameters for schematic view

Here is the interface for the mosfet schematic cdf :





CDF Parameter	Value	Display
Description	V IO (EG) LVT NFET 28A	off ▾
MosSelectKit		
Robust Rules	<input type="radio"/> 0 <input checked="" type="radio"/> 1	off ▾
Dimension Mode	TotalWidth ▾	off ▾
Total Gate Width	160n M	off ▾
Gate Finger Width	160n M	off ▾
Gate Length	150n M	off ▾
number of gate fingers	1	off ▾
Gate Split Y	1	off ▾
Multiplicity	1	off ▾
p_ia	0 M	off ▾
Drain Contact Selection	contact ▾	off ▾
Source Contact Selection	contact ▾	off ▾
Total Drain Area	19.2f	off ▾
Total Source Area	19.2f	off ▾
Total Drain Periphery	400n	off ▾
Total Source Periphery	400n	off ▾
Gate Contacts	NONE ▾	off ▾
Number of Gate Contacts	1	off ▾
Change STI Stress Estimation?	<input type="radio"/> Yes <input checked="" type="radio"/> No	off ▾
Simulation Option Expert	<input checked="" type="radio"/> 0 <input type="radio"/> 1	off ▾
X-coordinate of gate	-1 M	off ▾
Y-coordinate of gate	-1 M	off ▾
plorient	<input checked="" type="radio"/> 1 <input type="radio"/> 2	off ▾
Advanced Matching Simulation	<input checked="" type="radio"/> 0 <input type="radio"/> 1	off ▾
M1Route	<input type="checkbox"/>	off ▾
PolyRoute	<input type="checkbox"/>	off ▾
Activate nsig parameters	<input checked="" type="radio"/> 0 <input type="radio"/> 1	off ▾
Safe Operating Area	<input type="radio"/> 0 <input checked="" type="radio"/> 1	off ▾
Enable Editing Rule Sets(expert)	<input type="checkbox"/>	off ▾
Bulk	VSS!	off ▾
Source First	<input checked="" type="checkbox"/>	off ▾

Figure 21: cdf GUI for mosfet schematic

All unnecessary parameters have been hidden in order to simplify the GUI and its use. None parameters are deleted in order to keep compliancy during migrations.

Some parameters are enabled only if you validate a switch before. That way the GUI is more compact and more user friendly.

For example the STI Compression parameters are now only available by setting the switch “Change STI Stress Estimation” to YES.





Change STI Stress Estimation? Yes No

STI Compression (sa)	120n M
STI Compression (sb)	120n M

Figure 22: STI Stress Estimation management

There is also the feature about Drain/Source area and perimeter computation and management, the value of these cdf are editable only if you choose the mode USER, if not these parameters are automatically calculated and netlisted.

Drain Contact Selection	user
Source Contact Selection	user
ad	19.2f M
as	19.2f M
pd	400n M
ps	400n M

Figure 23: Drain/Source Contact selection and area/perimeter

3.10.1.1 Specific parameters:

These 2 specific buttons are available:

- *Enable Editing Rules Sets*
- *MosSelectKit*

The first one is here to prevent designers to use the ruleSet without knowing well this feature. This feature, inherited from ISDA, gives the possibility to designers to manage pcell configuration using pre-defined and specific configurations. A misuse of this feature can create not DRC clean configurations, furthermore some of configurations are not well supported by pcells. That's why we hide by default this feature. So we don't recommend to use this mode, as we can't support all the aspect of the feature. Anyway, the most used and useful ruleSets are now managed through the interface with the cdf parameters. In the documentation the link between ruleSet and cdf are explained.

Then the *MosSelectKit* is a feature which is enabled when the product AIK (Analog Implementation Kit) is loaded in the environment. This Kit is supported only for DK, not for PDK.

3.10.2 Interface for pcell parameters

The GUI has been simplified, all the unused parameters have been hidden. Furthermore we tried to arrange all the parameters by types and from the most important to the less important.



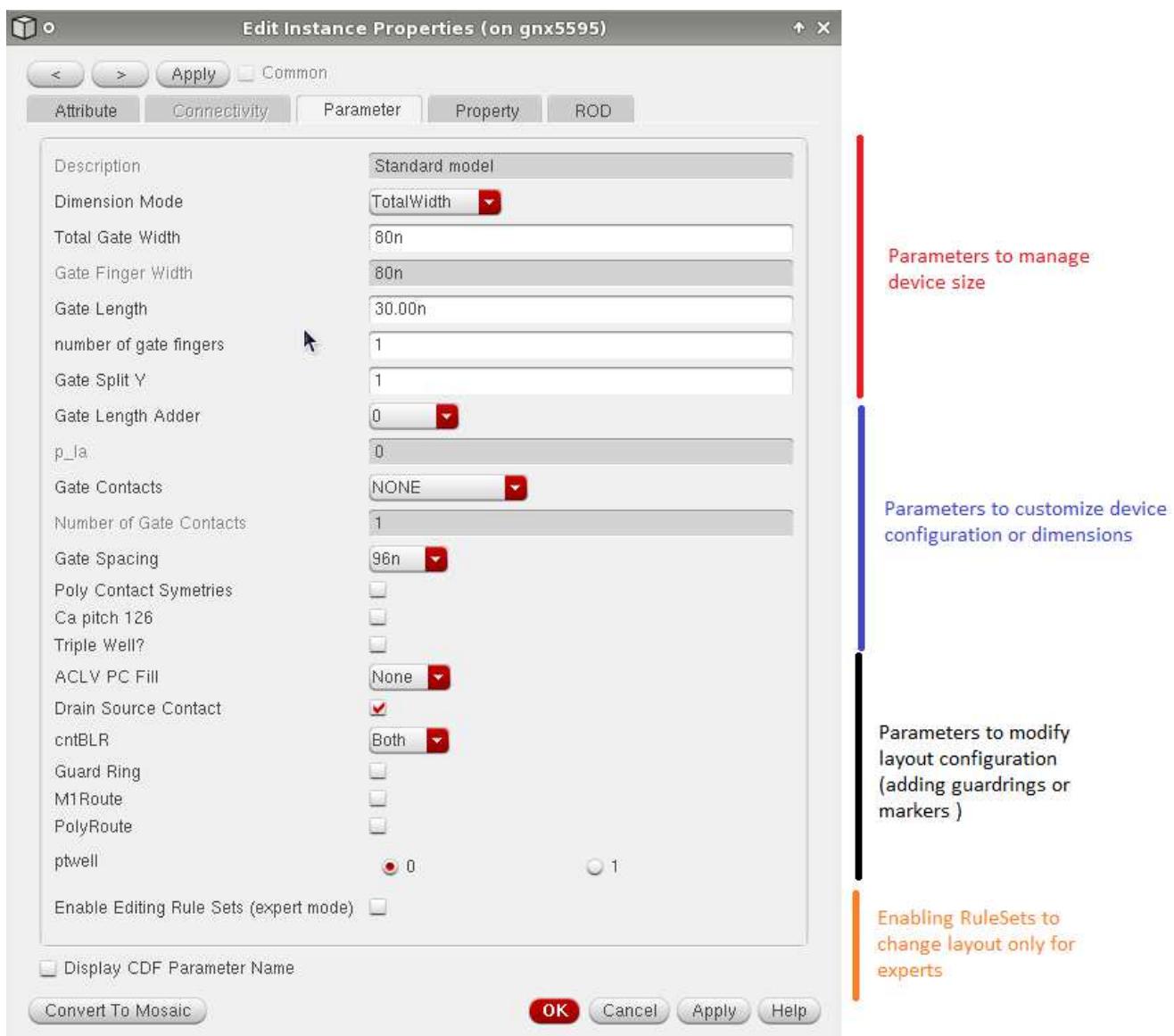


Figure 24: user interface for mosfet pcell

3.11 Description of mosfet ruleSets and CDF

3.11.1 Gate Length adder

the poly bias compensation is managed by using the parameter "Gate Length Adder".

The field "Gate Length Adder" is leading the cdf parameters p_la and p_la_select. These cdf can modify the length of the pcell by adding some markers.



**Figure 25: widget for Gate Length Adder**

As you can see there are different values to add from 4n to 16n and a specific value named wimpy.

Here is the following different relationship between the cdf values, the ruleSet used and the marker added:

Recommend rules	Gate length adder value	layer	Device
	0		
PCSTP2	2	POBIASP;drawing2	GO1
PCSTP4	4	POBIASP;drawing4	GO1
PCSTP6	6	POBIASP;drawing6	GO1
PCSTP8	8	POBIASP;drawing8	GO1
PCSTP10	10	POBIASP;drawing10	GO1
PCSTP16	16	POBIASP;drawing16	GO1
WIMPY	Wimpy	MKR;wimpy	GO1

Figure 26: truth table for Gate Length Adder

As you can see in the table, this feature is only available for GO1 mosfet: so for the RVT fet and the LVT fet.

The figure below shows the relationship previously explained between the cdf interface, the ruleSets automatically selected and the markers on pcell.



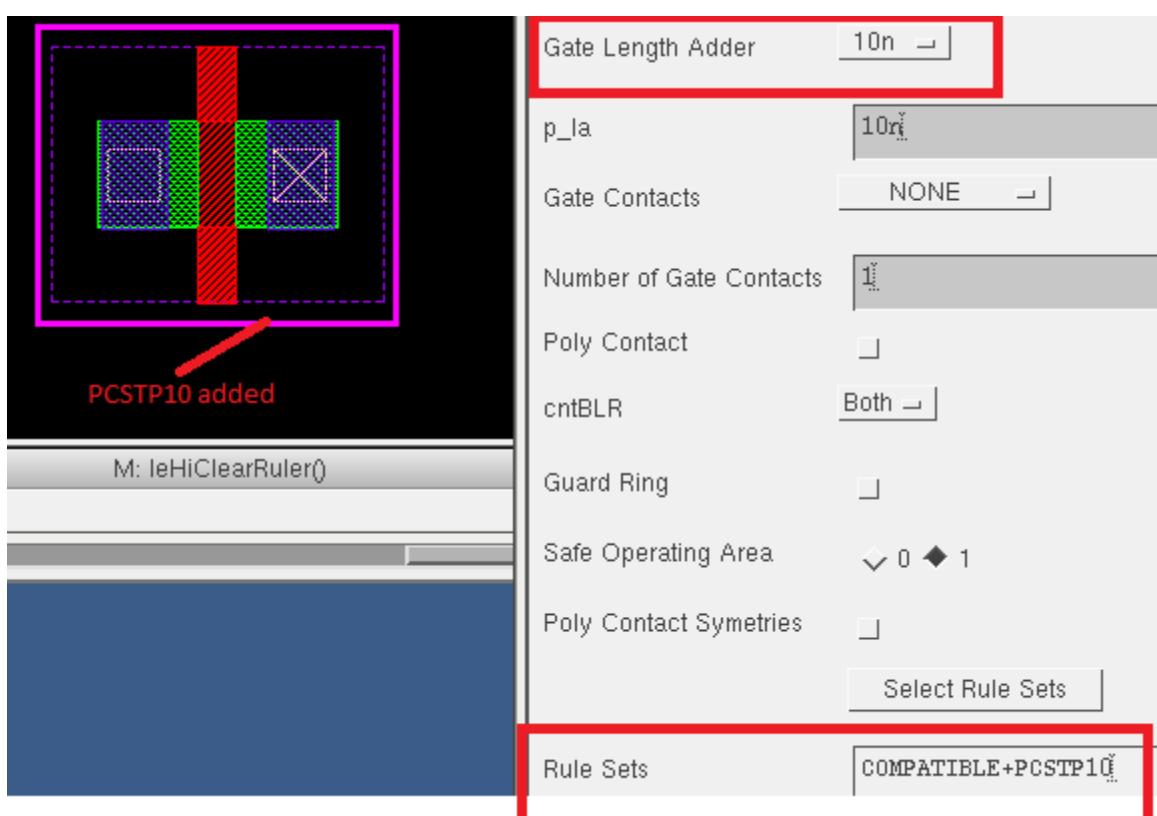


Figure 27: markers managed by cdf and ruleSet

The recommended rules add corresponding layer on MOS with respect of DRM rules:
(See DRM for complete rules)

b.b) POBIASPx markers design rules

Additional Design Rules		
POB.R.1	POBIASPx markers cannot intersect each others.	
POB.R.2	POBIASPx markers are prohibited over (ZG, EG, OP, ESD_CDM, ESD_HBM, PCAP, NCAP, EFUSE, CELLSNR, MKR; ROMST).	
POB.R.6	POBIASNx is prohibited.	
POB.R.4	POBIASPx must intersect gate	
POB.L.1	Gate length for gates covered by POBIASPx (min=max)	0.030
POB.EX.1	POBIASPx extension on gate in SD direction	0.121
POB.EN.1	POBIASPx enclosure of gate	0.072

Figure 28: POBIASPx marker rules

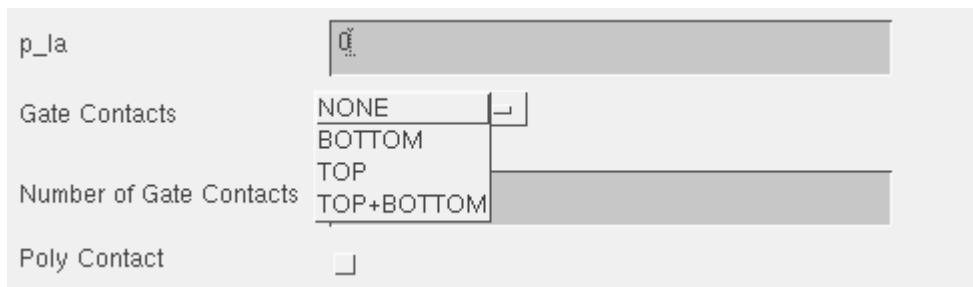


MKR;wimpy Design Rules			
WPY.R.1	MKR;wimpy must intersect Gate		
WPY.EN.1	MKR;wimpy enclosure of Gate		0
WPY.D.1	MKR;wimpy distance to Gate		0.010
WPY.R.2	MKR;wimpy must be covered by LVT or RVT		
WPY.R.3	MKR;wimpy must not interact (Gate .and. HYBRID), EG, POBIASPx, CELLSNR, MKR;ROMST		

Figure 29: wimpy marker rule

3.11.2 Gate Contact

This cdf give the possibility to the user to manage “ngcon” and “polyCnt”. But PolyCnt shouldn't not be modify by the user, only Gate Contact should modify ngcon and polyCnt.

**Figure 30: Gate Contact GUI**

So you can handle the number of gate contacts and the poly contact with the following truth table:

polyaccess	RuleSet	PolyCnt	ngcon
NONE	-	False	1
BOTTOM	-	True	1
TOP	TOP_POLY_ROUTING	False	1
TOP+BOTTOM	TOP_POLY_ROUTING	True	2

Figure 31: truth table of Gate Contact

The illustration below shows the relationship between the cdf, the ruleSet and the pcell.

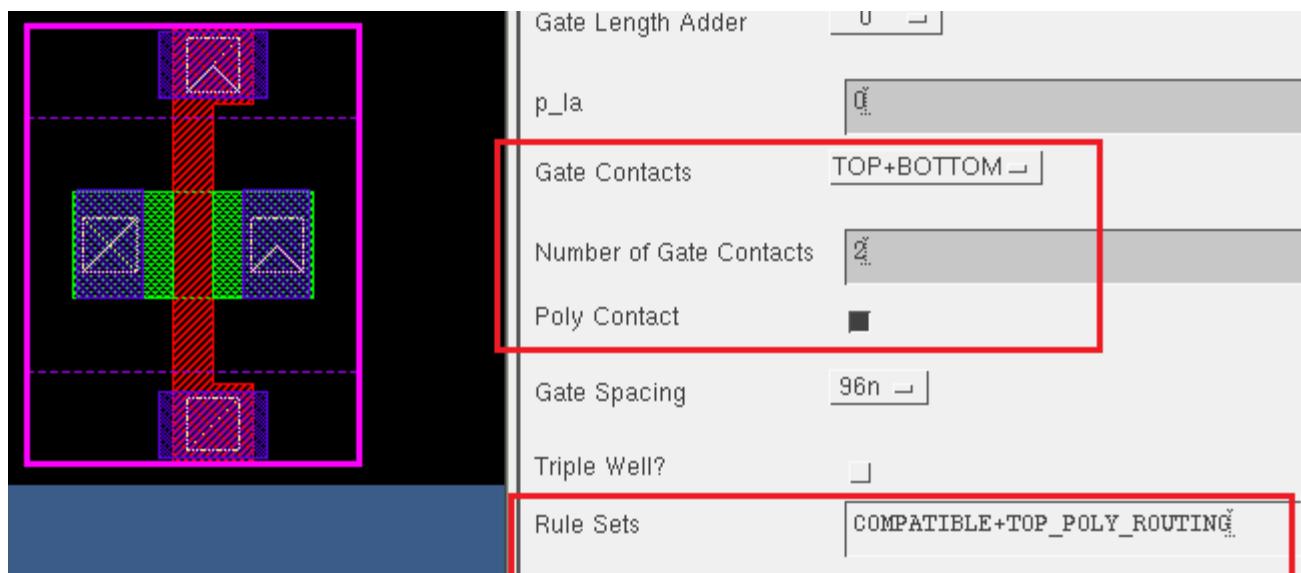


Figure 32: use of Gate Contacts

In the latest version of the design kit we retire the display of "polyCnt" because some users try to modify it when only "Gate Contact" should modify that value.

3.11.3 Gate Spacing

In this version, the designer can manage the distance between poly gate and contact in GO1 mosfets. For GO2 mosfets, this distance is fixed to 140n and is not editable.

When several fingers are used in the pcell, the user will have the choices between 10 different values of gate spacing between fingers from 96n to 242n. Furthermore he will have the possibility to apply this space on the extreme sides of the pcell with the switch "Poly Contact Symmetries".

Here is an example of use for this parameter:

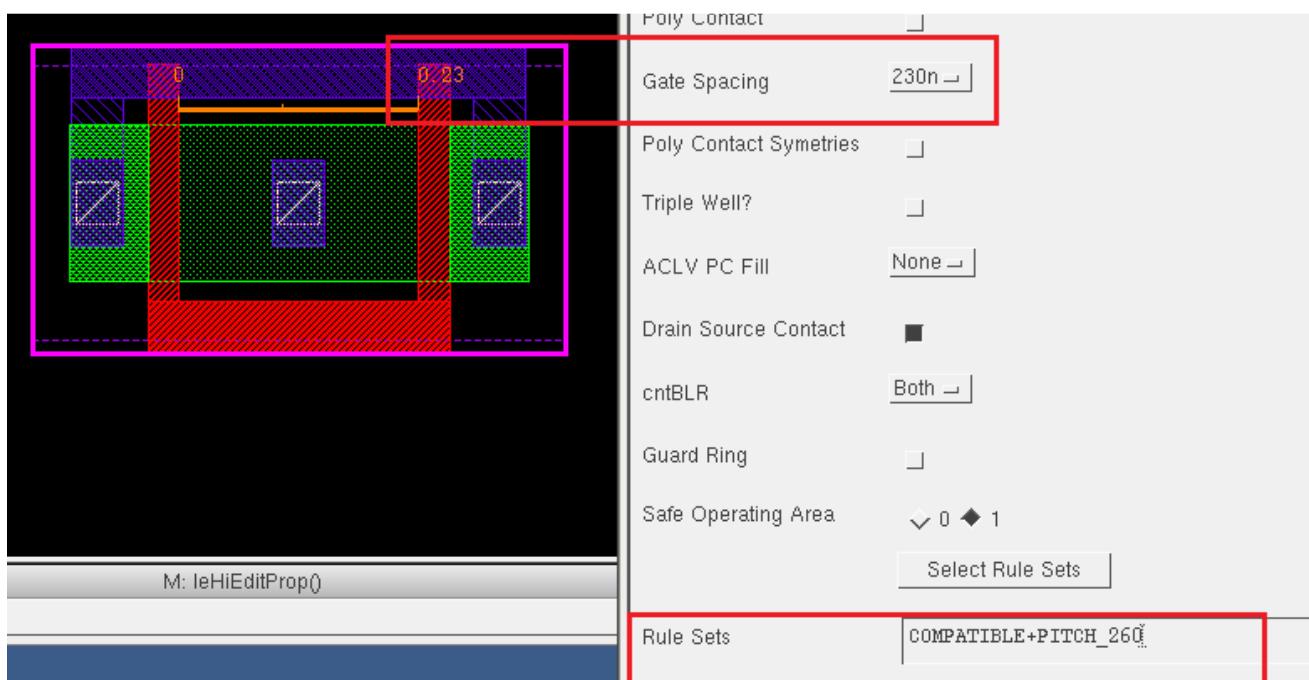


Figure 33: use of gate spacing

As you can see, the Gate Spacing represents the distance edge to edge (check the ruler) between 2 gates. The corresponding Rule Set is “COMPATIBLE+PITCH_260”, as we have previously said COMPATIBLE is the default value from 32n, then the rule set is named by the corresponding pitch between 2 gates when the gate length is 30n, the default value. That is why a 230n gate spacing corresponding to a pitch named 260, below are all the value of gate spacing with the corresponding rule.

Gate Spacing	Poly Contact Symmetry	RuleSet
96	False	-
98	False	PITCH_128
100	False	PITCH_130
102	False	PITCH_132
104	False	PITCH_134
106	False	PITCH_136
114	False	PITCH_144
222	False	PITCH_252
230	False	PITCH_260 (for L>=48nm)
242	False	PITCH_272 (for L>=48nm)
96	True	-
98	True	PITCH_128 + SYMMETRIC_DIFF_CONTS_PITCH_128
100	True	PITCH_130 + SYMMETRIC_DIFF_CONTS_PITCH_130

102	True	PITCH_132 + SYMMETRIC_DIFF_CONTS_PITCH_132
104	True	PITCH_134 + SYMMETRIC_DIFF_CONTS_PITCH_134
106	True	PITCH_136 + SYMMETRIC_DIFF_CONTS_PITCH_136
114	True	PITCH_144 + SYMMETRIC_DIFF_CONTS_PITCH_144
222	True	PITCH_252 + SYMMETRIC_DIFF_CONTS_PITCH_252
230	True	PITCH_260 + SYMMETRIC_DIFF_CONTS_PITCH_260
242	True	PITCH_272 + SYMMETRIC_DIFF_CONTS_PITCH_272

Figure 34: truth table gate spacing/Poly Contact Symmetries

The switch "Custom Gate Spacing" allows to enter values beyond 96nm for SRAM purpose.

Now you have the possibility, as shown in the table above, to symmetrize the space between contact and poly. You can see on figure 24 that the space to poly of the 3 contact are different, if you activate the Poly Contact Symmetries switch, you will symmetrize that distance and have the following configuration.

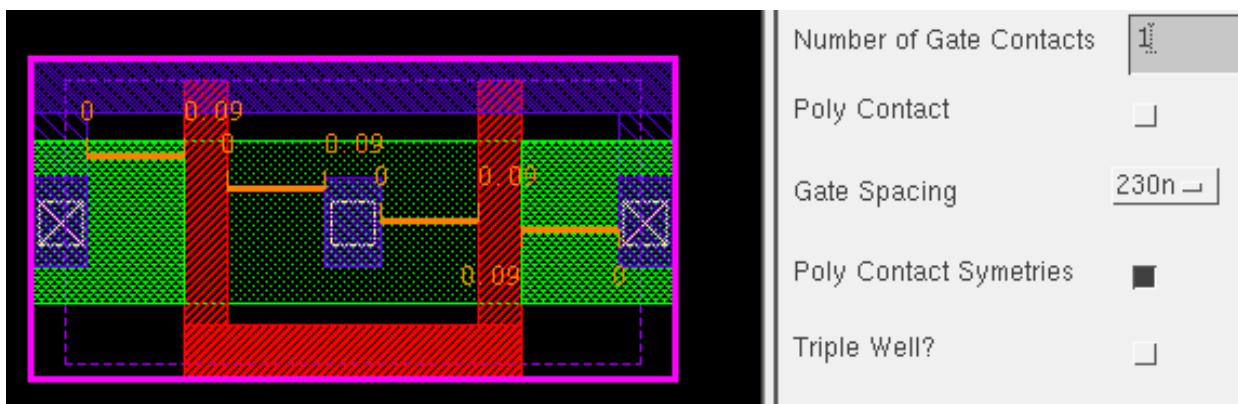


Figure 35: applying Poly Contact symmetries

If you watch carefully the ruler, you will see that all the distance poly to contact are now equal to 90n.

3.11.4 HSSOI and BP Extension

Warning: these cdf and ruleSets are exclusively used in EGLVT mosfet.

We are going to set ruleSet in the pcells that will allow the selection between several possible configurations. The aim to this feature is to give the possibility to the designer to use an extension of BP and HSSOI layer more or less important.

Depending on the design, the configuration can be drc clean or not. So to provide all the configurations (always drc clean or the smallest or a symmetric configuration...) we use the following switch:

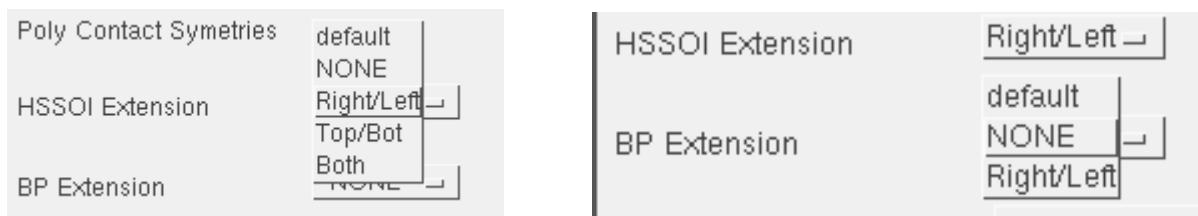


Figure 36: BP and HSSOI Extension GUI

Here we give all the possibilities to manage the HSSOI extension:

- **Default :**

Pcell identical to the one proposed in DK 2.2, it's not DRC Clean by default but could be DRC clean depending on the design for example if the pcell is placed on a HSSOI shape. It's also the configuration which offers the best integration density.

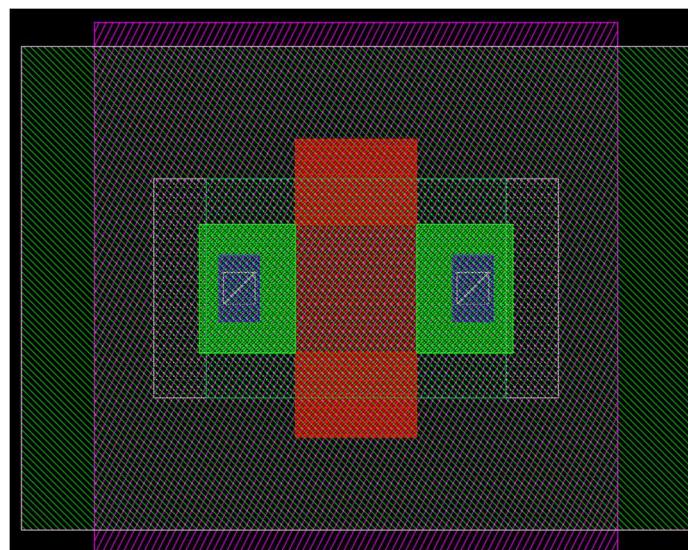


Figure 37: HSSOI "default" value

NW and EG are not aligned and the extensions are not properly set. This is the most compacted pcell, the DRC issues could be solved by the design using EG extension and/or NWELL extension.

- **HSSOI_Extension_EG_None**

Pcell DRC Clean, NW and EG are aligned on every sides (bottom; top, left and right), BP aligned with RX.



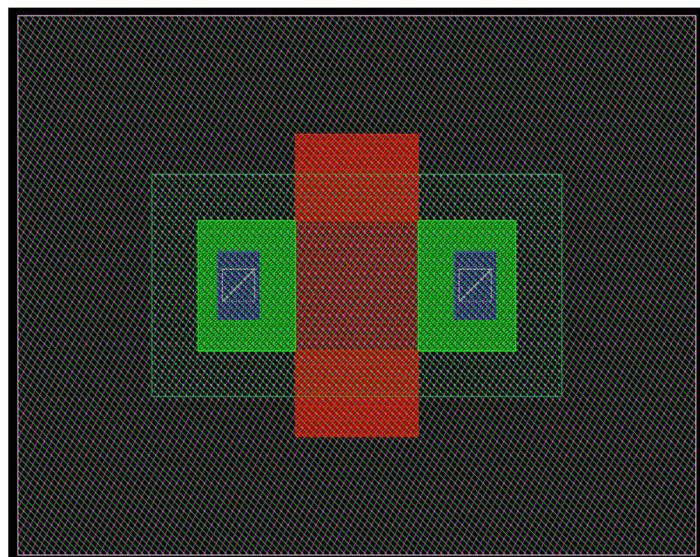


Figure 38: HSSOI Extension NONE

- **HSSOI_Extension_EG_Right_Left**

Pcell DRC Clean, NW and EG are aligned on top and bottom and the extension on NWELL on EG is set at the correct value on left/right.

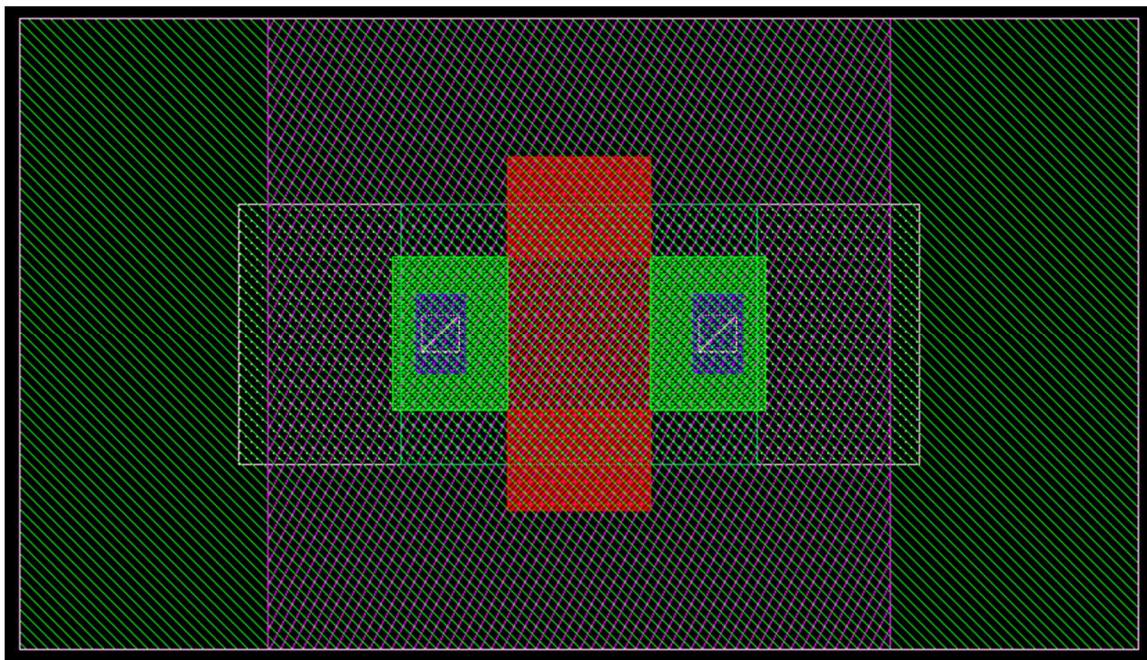


Figure 39: HSSOI Extension Right/Left



- **HSSOI_Extension_EG_Top_Bottom**

Pcell DRC Clean, NW and EG are aligned on left/right and the extension of EG on NWELL is properly set on top/bottom.

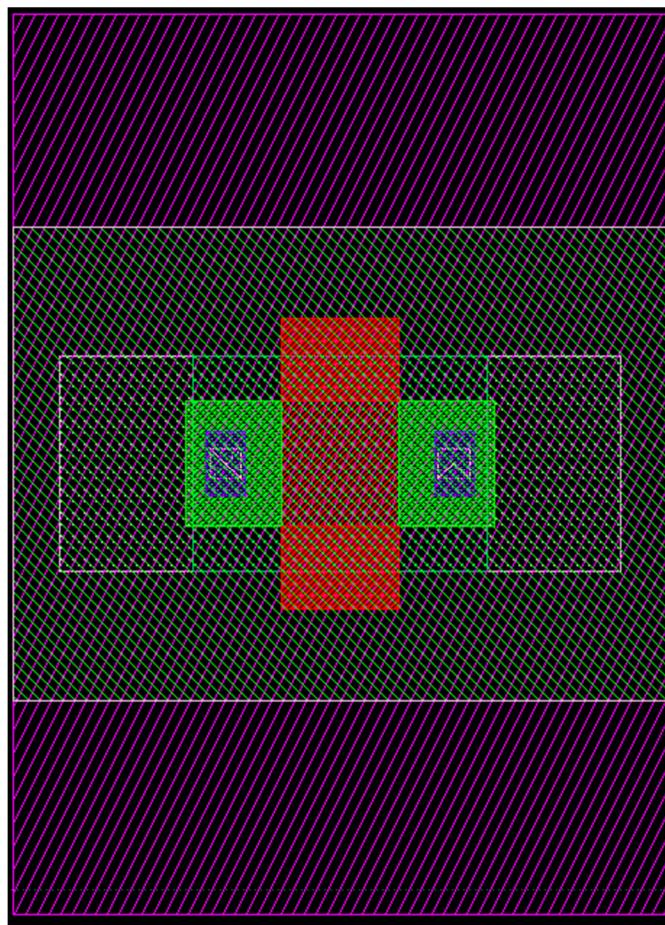


Figure 40: HSSOI Extension Top/Bottom

- **HSSOI_Extension_EG_ Both**

Pcell DRC Clean, the extensions of NW and EG are properly set on top/bottom and left/right.



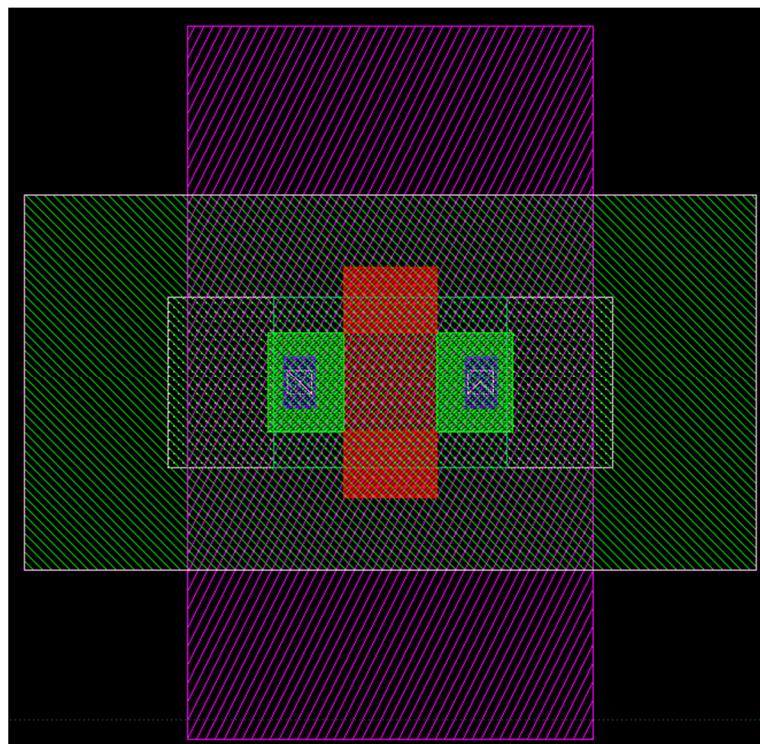


Figure 41: HSSOI Extension Both

All the values previously described are summarized in the following truth table:

Extension HSSOI :	RuleSet :
default	No ruleSet added
None	HSSOI_Extension_EG_None
Right/Left	HSSOI_Extension_EG_Right_Left
Top/Bot	HSSOI_Extension_EG_Top_Bottom
Both	HSSOI_Extension_EG_Both

Now if we use pfet EGLVT mos, we can also BP Extension, each extension depending on the other, we couldn't use the same ruleSet, now one ruleSet manage the both extension. When HSSOI is on the default configuration, BP must be in that configuration also, BP is forced to default. Then when HSSOI isn't on the default value, BP could not be default, so it's forced to NONE in that case. It gives the following truth table:

HSSOI Extension :	BP Extension	RuleSet :
Default	Forced to default	No ruleSet added
When HSSOI_Ext != "default"	Forced to «	HSSOI_Extension_EG_<value>_Extension_LVT_None



" and BP_Ext="default" =>BP forced to "NONE"	NONE »	
None	None	HSSOI_Extension_EG_None_And_BP_Extension_LVT_None
Right/Left	None	HSSOI_Extension_EG_Right_Left_And_BP_Extension_LVT_None
Top/Bot	None	HSSOI_Extension_EG_Top_Bottom_And_BP_Extension_LVT_None
Both	None	HSSOI_Extension_EG_Both_And_BP_Extension_LVT_None
None	Right/Left	HSSOI_Extension_EG_None_And_BP_Extension_LVT_Right_Left
Right/Left	Right/Left	HSSOI_Extension_EG_Right_Left_And_BP_Extension_LVT_Right_Left
Top/Bot	Right/Left	HSSOI_Extension_EG_Top_Bottom_And_BP_Extension_LVT_Right_Left
Both	Right/Left	HSSOI_Extension_EG_Both_And_BP_Extension_LVT_Right_Left

Figure 42: truth table HSSOI with BP Extension

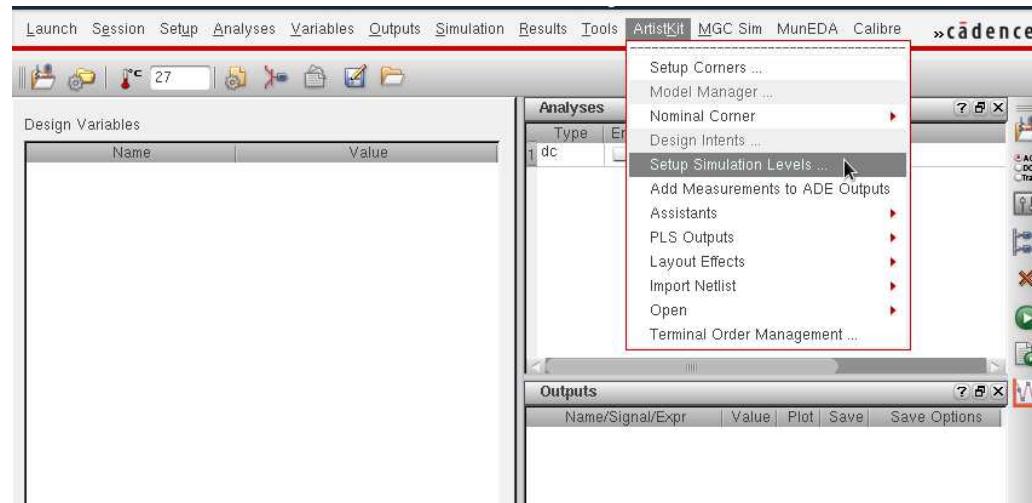
3.11.5 Accurate mode

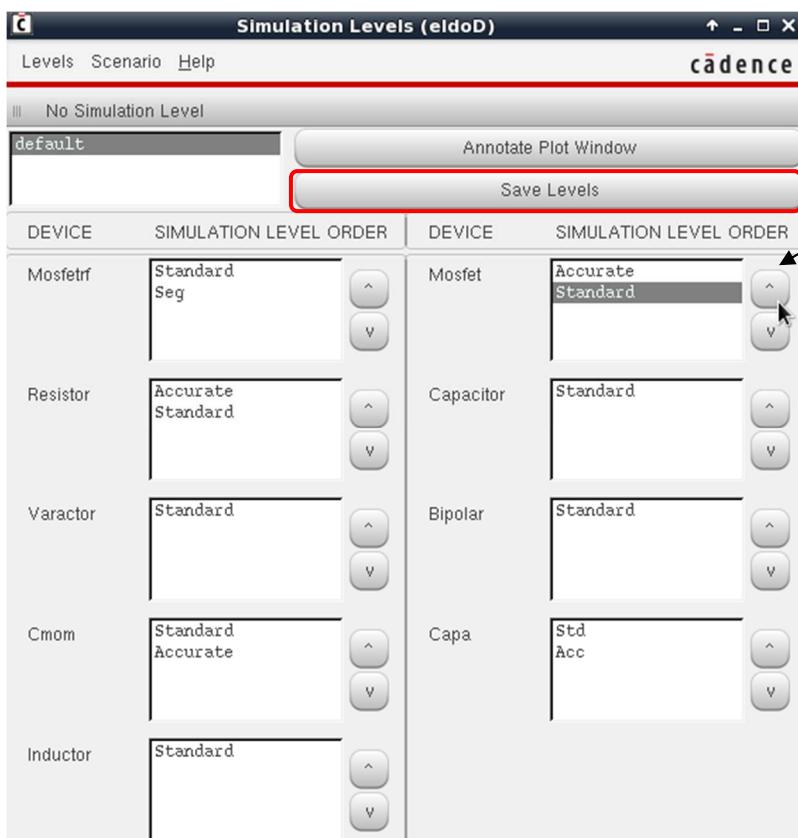
From DK2.8, the simulation Level "accurate" is available in all mosfets with the associated model.

This model is used by default.

You can change it and use the standard model from the ADE L - ArtistKit menu.

Launch ADE-L, then:





3.11.6 Simulation Option Expert

For all mosfets, you have the possibility to modify some model parameters using the switch “Simulation Option Expert” set to “1”:

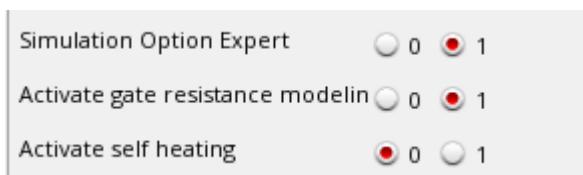


Figure 43.a: activate simulation expert parameters

The following parameters are available when this switch is activate:

- swrg: Activate Gate Resistance Modeling
- swshe: Activate Self Heating

You can check in the model documentation, what are the exact effects of these parameters.

3.11.7 Advanced Matching Simulation

For all mosfets, you have the possibility to modify some model parameters using the switch “Advanced Matching Simulation” set to “1”:



Advanced Matching Simulation	<input type="radio"/> 0 <input checked="" type="radio"/> 1
Activate mismatch	<input type="radio"/> 0 <input checked="" type="radio"/> 1
Number of transistors in X direct	1
Number of transistors in Y direct	1
Transistors pitch in X direction	-1 M
Transistors pitch in Y direction	-1 M

Figure 43.b: activate advanced matching parameters

The following parameters are available when this switch is activate:

- mismatch : activate mismatch
- mx: Number of transistors in X direction
- my: Number of transistors in Y direction
- deltax: transistors pitch in X direction
- deltay: transistors pitch in Y direction

You can check in the model documentation, what are the exact effects of these parameters.

3.11.8 Nsig parameters

After an update of the model, the previous nsig parameters : nsig_vto, nsig_uo, nsig_dibl, nsig_lvaro, nsig_wvaro has deleted and replaced by only 2 parameters: nsig_delvto_uo1 and nsig_delvto_uo2.

These 2 parameters are available only by setting the switch nsig to Yes:

Activate nsig parameters	<input type="radio"/> 0 <input checked="" type="radio"/> 1
nsig_delvto_uo1	0
nsig_delvto_uo2	0

Figure 43: activate nsig parameters

The aim of these parameter is to provide an easy access to the Monte Carlo simulation without having to set thousands of simulations. With these parameters, the Monte Carlo results are directly available.

3.11.9 Mismatch

The following parameters have been added in all mosfets for mismatch consideration:

- Xpos : X-coordinate of the gate
- Ypos : Y-coordinate of the gate
- Plorient : Orientation of the transistor.

These parameters are extracted during PLS phase.



3.12 Fluid Guard Ring

In order to give more flexibility to isolate a chip, the fluid guard ring (FGR) is now supported. This new feature replaces the previous MultiPartPath which is no more supported by the DesignKit team but it is still available for compatibility.

In this version, we provide 3 types of fluid guard ring: nFGR, pFGR and t3FGR to implement the 3 types of substrate isolation: nwell pwell and deep-nwell:

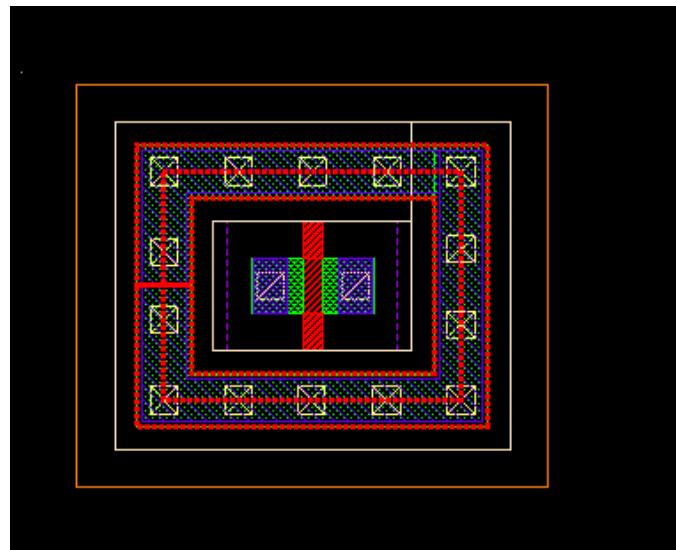


Figure 44: nwell fluid guard ring (nFGR)

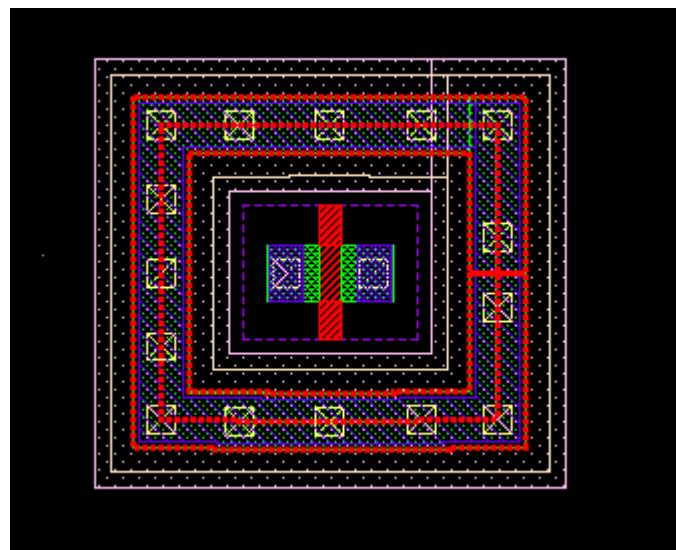


Figure 45: pwell fluid guardRing (pFGR)

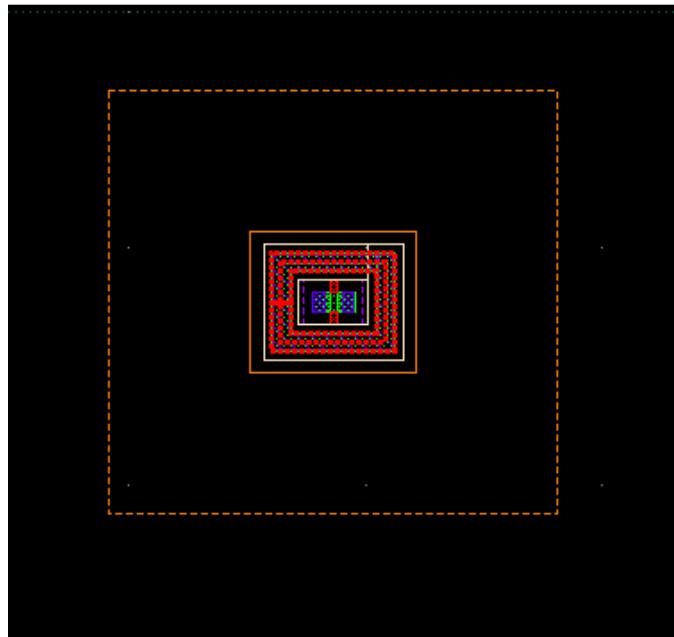


Figure 46: deep nwell fluid guard ring (t3FGR)

The previous illustrations are the implementation of the 3 types of fluidguard ring in the **Wrap** mode. There are 4 different modes to use fluid guard rings:

- **Wrap mode:** the FGR will wrap all the area selected with the minimum size
- **Path mode:** the user draw the FGR as a path
- **Rect Mode:** it will create a rectangle FGR, the user place it where he wants
- **Polygon:** the user can draw the polygon he wants for the FGR



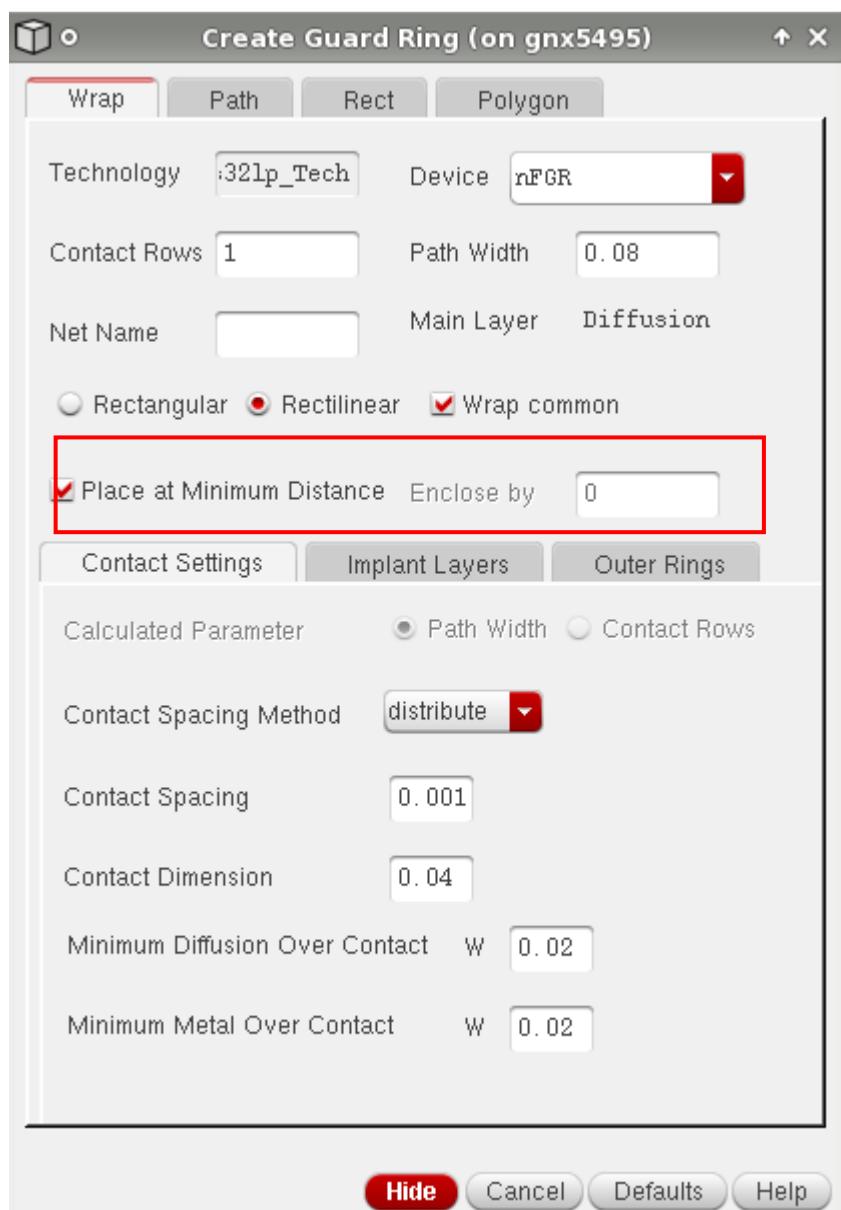


Figure 47: 4 different FGR modes

You can see the FGR defined in the techfile can be modified by the user, the following parameters can be modified for customization: enclosure, contact size and spacing, overlap on contact...

On the previous figure, in wrap mode, when the thick box: "Place at Minimum Distance" is selected, the FluidGuard ring will be placed at the minimum space around the device(s). If you only have one device to isolate, it could be not DRC clean depending on the size of the device, the enclosure in the FGR would be too small. In that case you would have several possibility:

- You can change the mode used
- You can add an enclosure by hand

Otherwise the FGR is DRC clean.

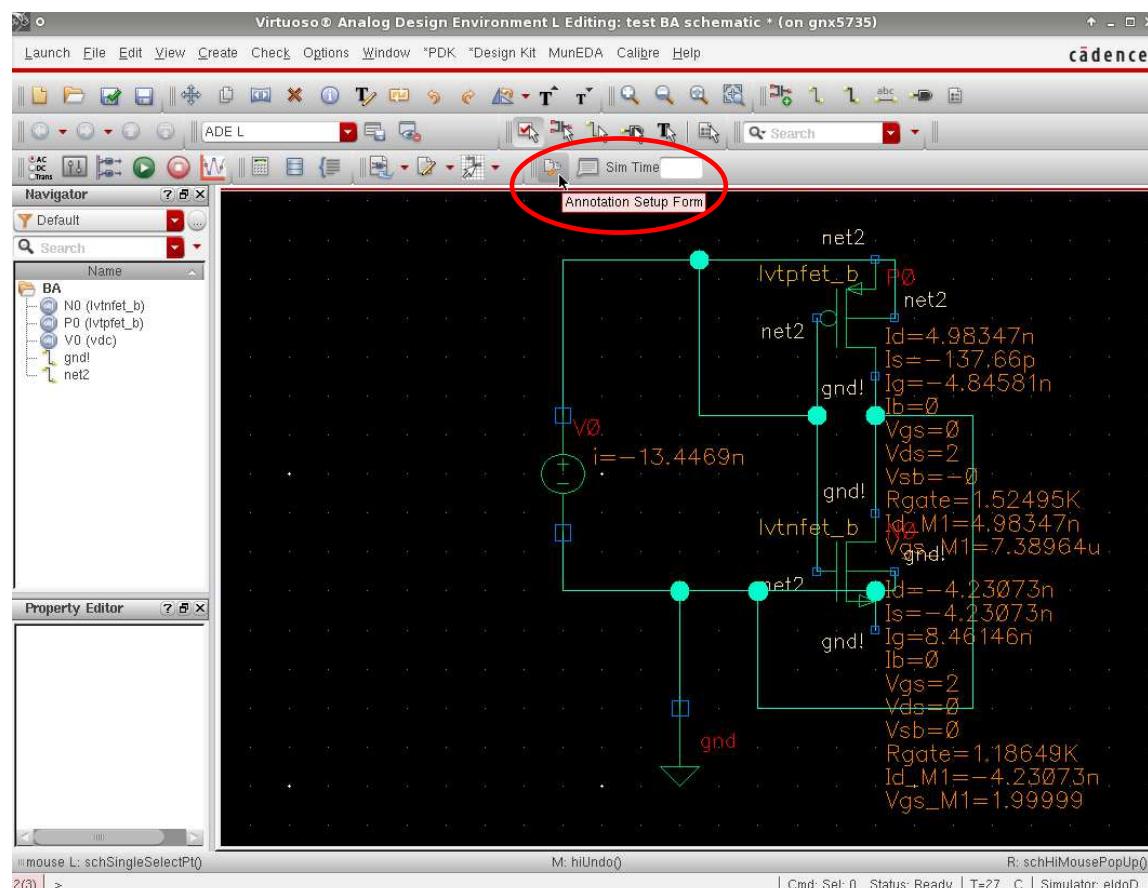
3.13 Backannotation

This feature is able to replay the different equations of a design to display the different parameters values for a device, for a specific simulation.

For a given design, simulate the schematic with eldoD and launched the backannotation with the following actions:

- Under Virtuoso Schematic Editor: *Launch-> ADE L*
- In the Analog Environment window: *ArtistKit->Setup Corners -> Save Model File*
- Tick “dc” box
- Double click on dc and under *Analyses-> Choose*: tick *Save DC*
- Then Run the simulation: *Simulation-> Netlist and Run*
- Select the menu *Results ->Annotate -> DC Operating Points*, and backannotated values will appear in your schematic

You can modify the list of backannotated parameters using the menu “Annotate Setup Form” from the schematic view:



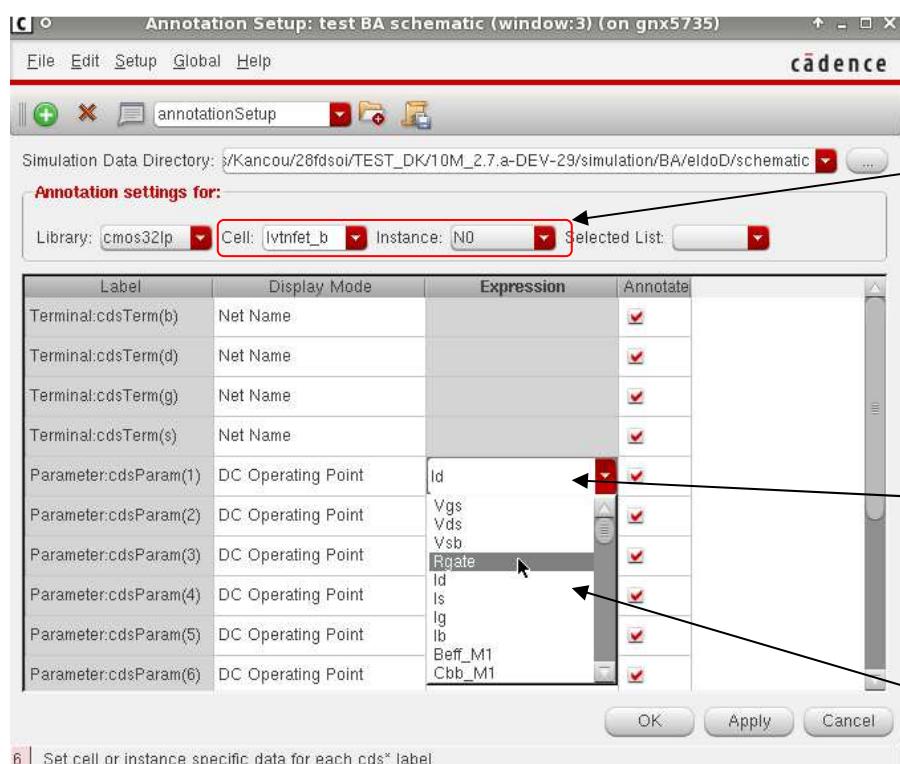


Figure 48: Parameters and display of backannotation

3.14 VXL Connectivity Extractor

Thanks to the “wire” layout object which is able to contain and propagate a net name, it’s possible to check if two terminals are correctly connected by a net and even perform a complete LVS of your design.

Of course, this LVS solution is NOT SIGN OFF but allow the designer to see easily how the instances of his design are connected together, where are the shorts and the incomplete nets and thus debug quickly his design. As it’s completely based on the OA database, user don’t have to go through intermediate formats like textual netlists or GDSII database, and it makes the check very quick. Moreover, the annotation browser is integrated in the design environment and you don’t have to juggle with several windows.

3.14.1 Strong connectivity extraction:

Before extracting your design, you have to choose the correct constraint group of the cmos32lp_Tech techno library. This constraint group lists the valid layers and vias through which the extractor is authorized to go when he follows a net and thus check a connectivity.

You can set this constraint group through the Virtuoso menu:

Options → LayoutXL → Extraction → Select “**virtuosoDefaultExtractorSetup**” constraint group if you’re performing an extraction.

Then you can launch the extraction of your design. Go in the following Virtuoso menu:

Connectivity → Update → Extract Layout

Once the design is extracted, an Annotation Browser shows the reported issues, explain the kind of issue you're facing and highlight the problematic net in the layout and in the schematic. The "Annotation Browser" of Virtuoso is available through the following menus: Window --> Assistants --> Annotation Browser.

An example of connectivity extraction is given in the following picture:

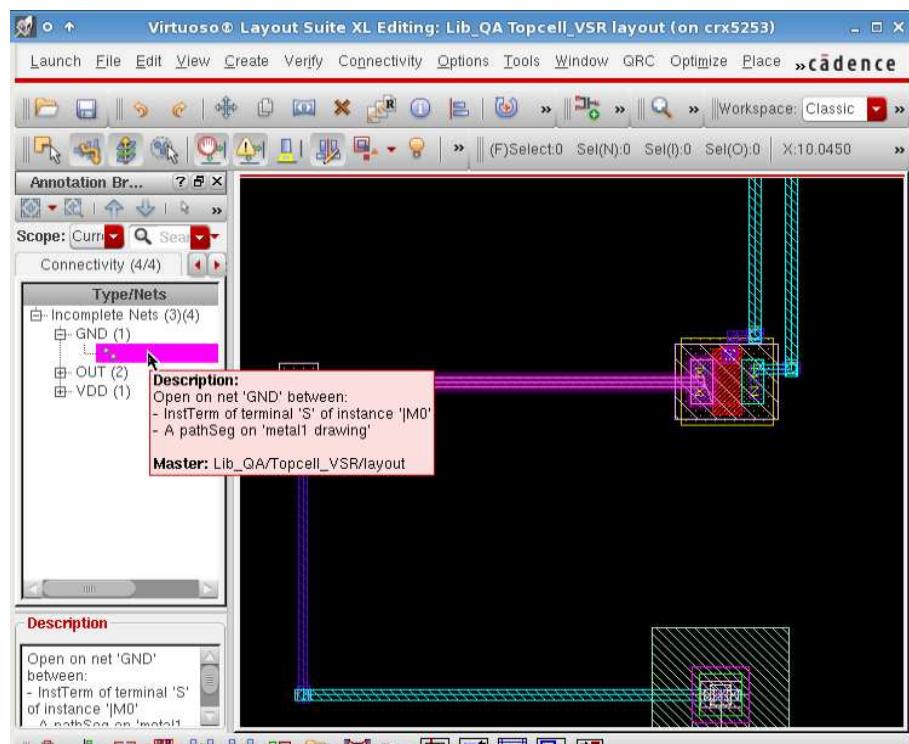


Figure 49: Example of flagged LVS errors in the Annotation Browser

3.14.2 Soft/Substrate connectivity extraction:

You can also decide to check the connections to the substrate (called "soft connections") and perform this way the Electrical Rules Check (ERC) to verify that for example a same bulk is not connected to 2 different nets which could be potentially two different powers.

The tool is exactly the same than in the previous section and thus, the steps to perform it are also identical except for two additional conditions that must be fulfilled to make it work:

- You must create a **PRBoundary** (Create → P&R Objects → P&R Boundary) around your design: this boundary will be considered as your PWELL bulk by the extractor
- You must set an additional switch has to be set in "Options → LayoutXL → Extraction → Select "Verify connections to substrate...as soft"

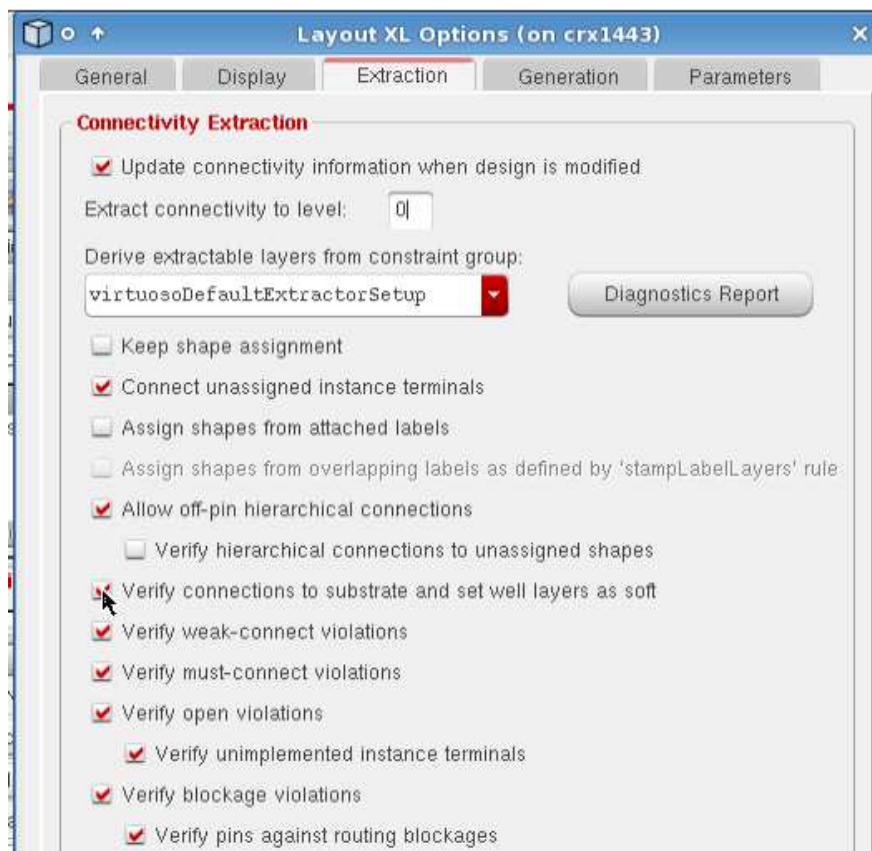


Figure 50: Pop up Layout XL window with the right Extraction settings

Once the design extracted, the way to debug your design is exactly the same than in the previous section.

- For more information about how to work with the Virtuoso Space Based Router, please refer to Cadence Documentation (Help) of IC617:

IC617 --> Virtuoso Layout Suite --> Virtuoso Router --> Virtuoso Space-based Router User Guide

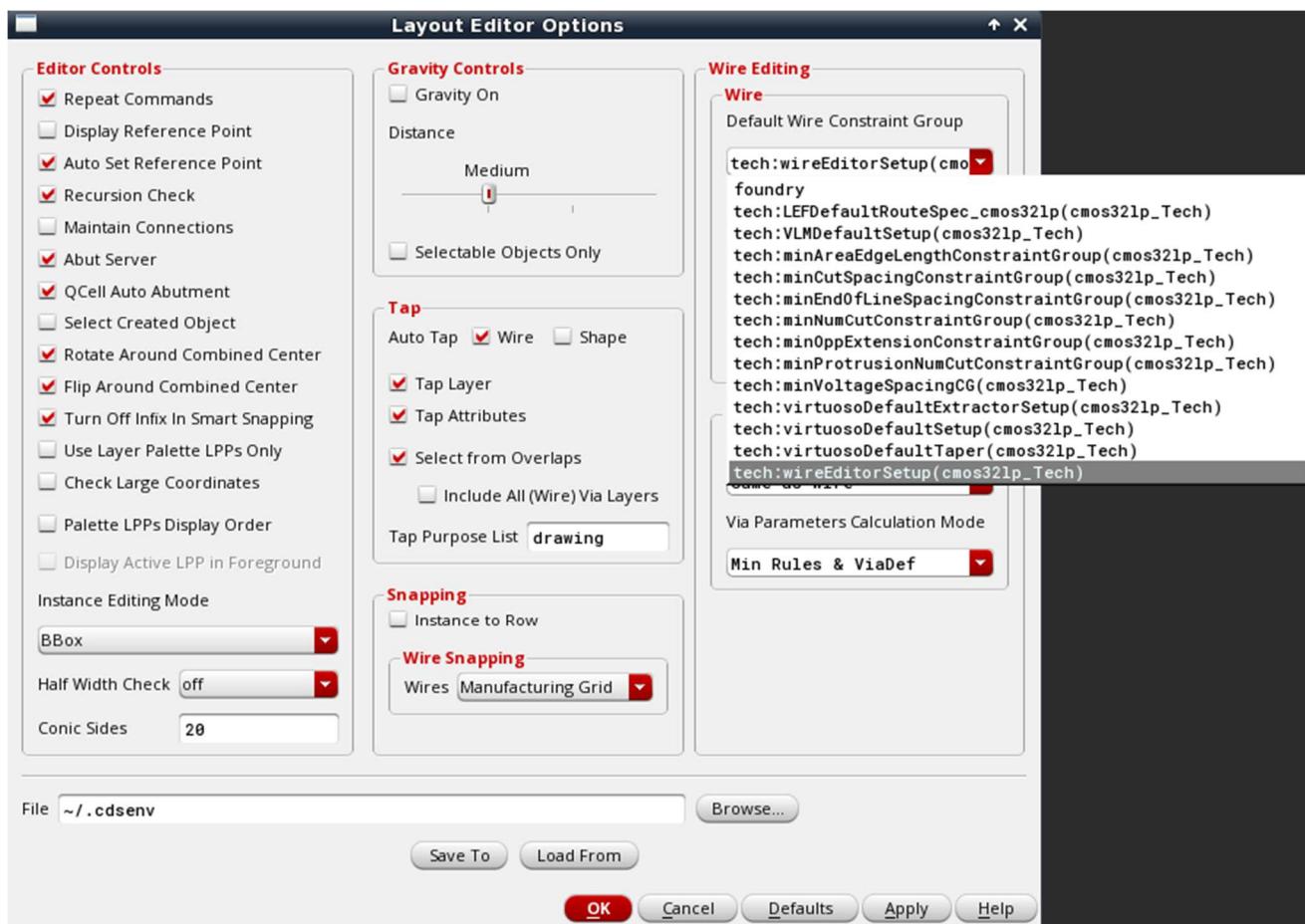
And for more specialized information concerning the Substrate extraction, please refer to Cadence Documentation (Help) of IC617:

IC617 --> Virtuoso Layout Suite --> Virtuoso Layout Suite –XL User Guide -> preparing your design for Routing --> Connectivity Extraction

3.15 Description of constraint groups in OA techfile



When opening the *Layout Editor Options* you can select different constraint groups for wires and vias edition during P&R:



3.15.1 Design Kit default constraint group

In 28FDSOI design Kit, the default is **wireEditorSetup**. It can be used for routing with all available specific vias (example for stack 10ML):

```
( validVias (RXCAM1 RXBPCAM1 RXNWCAM1 PCCAM1 M1V1M2 M1V1BARM2
M1V1BARM2LINE M1V1LRGM2 M1V1M2s M2V2M3 M2V2BARM3 M2V2BARM3LINE M2V2LRGM3
M2V2M3s M3V3M4 M3V3BARM4 M3V3BARM4LINE M3V3LRGM4 M3V3M4s M4V4M5 M4V4BARM5
M4V4BARM5LINE M4V4LRGM5 M4V4M5s M5V5M6 M5V5BARM6 M5V5BARM6 M5V5BARM6LINE
M5V5LRGM6 M5V5M6s IAXAIB IBVVLB ) )
```

Routing with PC is also possible with this constraint group.

3.15.2 Virtuoso default constraint groups

In case the design kit does not contain a specific constraint group, the tool will automatically use these three default constraint groups for P&R tools:





- ***virtuosoDefaultSetup***: only basic standard vias are available (example for stack 10ML):

(validVias (PCCAM1 M1V1M2 M2V2M3 M3V3M4 M4V4M5 M5V5M6 M6W0B1 B1W1B2 B2YZIA IAXAIB IBVVLB))

- ***virtuosoDefaultExtractorSetup*** for connectivity extraction as explained in §3.13, with a specific list of layers containing bulks, PC, pin and net purposes (example for stack 10ML):

(validLayers (sub1 sub2 TripleWell dGate PolyCutOxide d_PC_notCT dPc_nop (NW drawing) (NW pin) (NW net) HYBRID (RX drawing) (RX pin) (RX net) (BP drawing) (BP net) (BP pin) d_PC_notRes CA d_M1_notRes (V1 drawing) d_M2_notRes (V2 drawing) d_M3_notRes (V3 drawing) d_M4_notRes (V4 drawing) d_M5_notRes (V5 drawing) d_M6_notRes (W0 drawing) d_B1_notRes (W1 drawing) d_B2_notRes (YZ drawing) d_IA_notRes (XA drawing) d_IB_notRes (VV drawing) d_LB_notRes))

- ***virtuosoDefaultTaper*** used when there is not enough room to connect a pin to a metal, due to a layer conflict or a spacing conflict.

See Cadence documentation for more details:

IC6.1.7 → User Guide → Virtuoso Space-based Router User guide → Technology Requirements → Constraint Groups → Taper Constraint Group

Note that if you do not want to use ST specific constraint group *wireEditorSetup*, you can change it by yourself and choose *virtuosoDefaultSetup* instead.

Constraint groups *virtuosoDefaultExtractorSetup* and *virtuosoDefaultTaper* are used in any cases.

3.15.3 Other constraint groups for specific purposes

VLMDefaultSetup used for yield optimization. See Cadence documentation for more details:

IC6.1.7 → User Guide → Virtuoso Layout Migrate User Guide → Technology File Setup → Yield Optimisation using Virtuoso Technology Data.

LEFDefaultRouteSpec_cmos32Ip, called *LEFDefaultRouteSpec* inside the tool, is used to create LEF typically in digital standard cells applications.

It contains only metal layers and associated basic standard vias.

3.15.4 Foundry and rules in constraint groups

Other constraint groups should not be chosen specifically by the designer:

- Foundry
- minVoltageSpacingCG





- minEndOfLineSpacingConstraintGroup
- minProtrusionNumCutConstraintGroup
- minAreaEdgeLengthConstraintGroup
- minOppExtensionConstraintGroup
- minCutSpacingConstraintGroup
- minNumCutConstraintGroup

These constraint groups contain all technology rules needed for automatic routing, they are automatically used by the tools during P&R operations.

If you want a specific type of routing, you can select one of these constraint groups so that your design will respect only these types of rules, but we do not recommend this kind of use.





4 Devices

4.1 4.1 New devices in DK 1.2

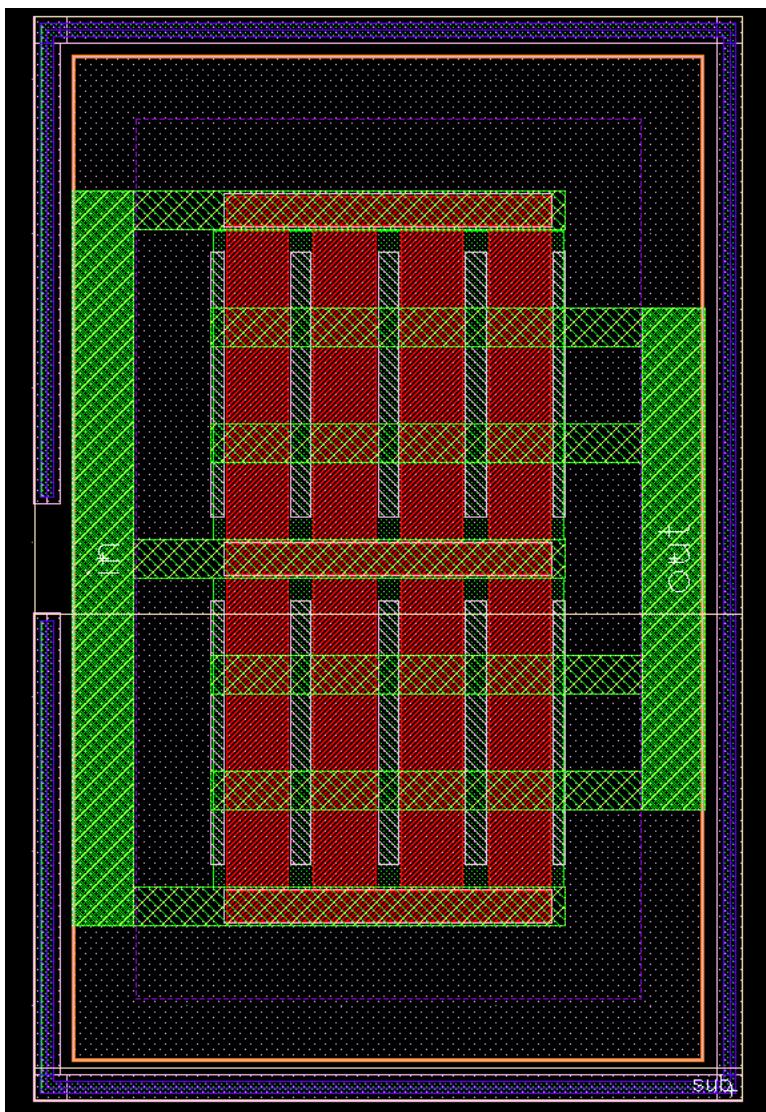
4.1.1 sealringCS (crack sensor)

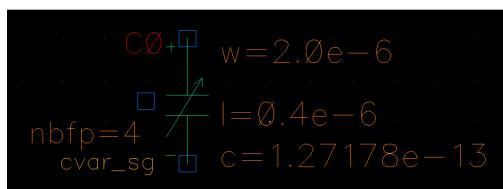
Please refer to related documentation "SealringCS_28FD_AN.pdf".

4.2 New devices in DK 1.1

4.2.1 Varactor NMOS GO1 (ST_C32_addon_DP)

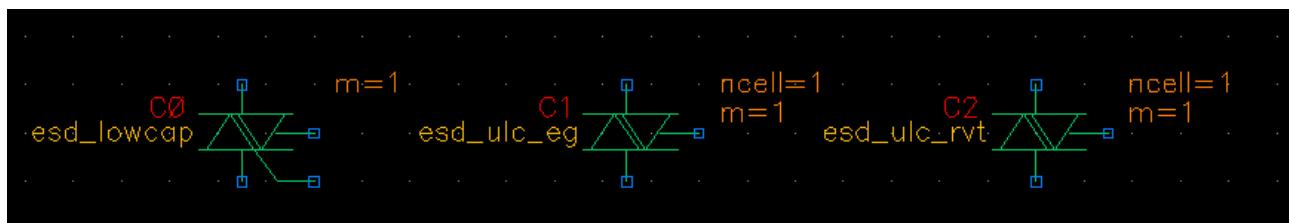
- cvar_sg





4.2.2 esd low capacitors (cmos32lp)

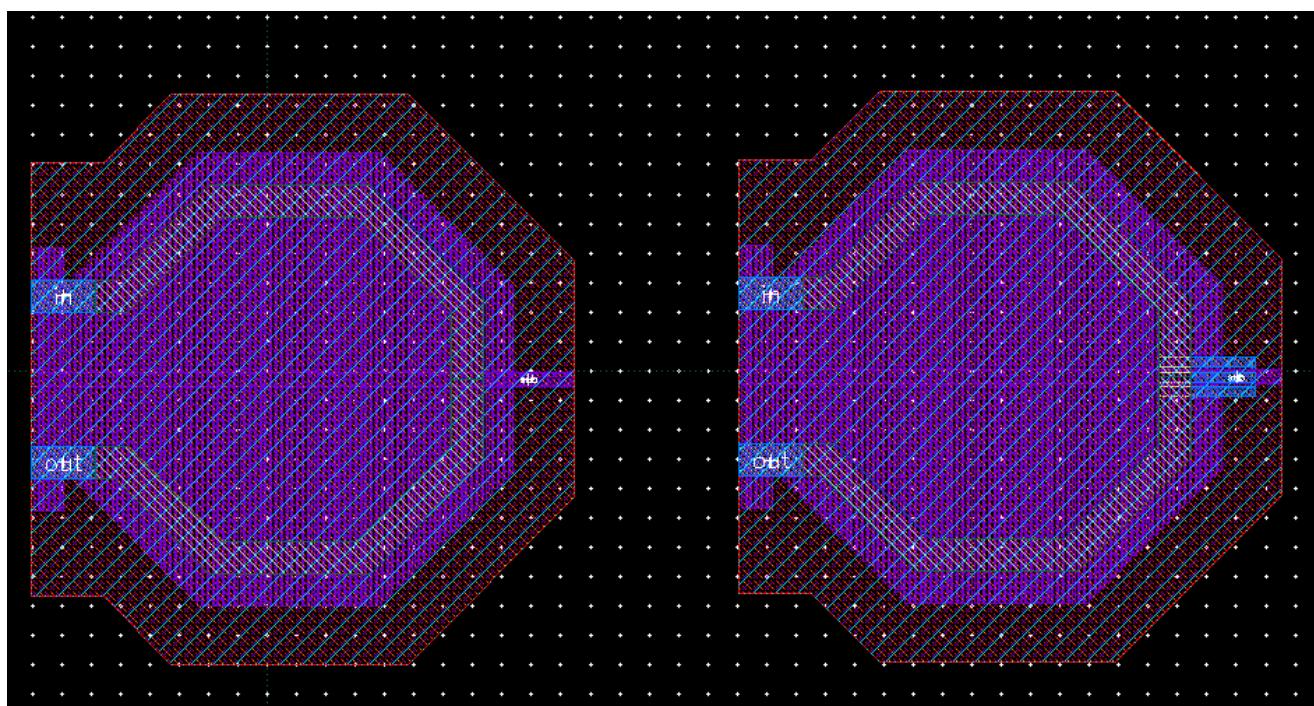
- esd_lowcap
- esd_ulc_rvt (ultra low cap RVT)
- esd_ulc_eg (ultra low cap EG)



4.3 New devices in DK 0.9

4.3.1 Inductances lohq High Performances

- ind_lohq_high_perf_6U1x_2T8x_LB
- inddif_lohq_high_perf_6U1x_2T8x_LB

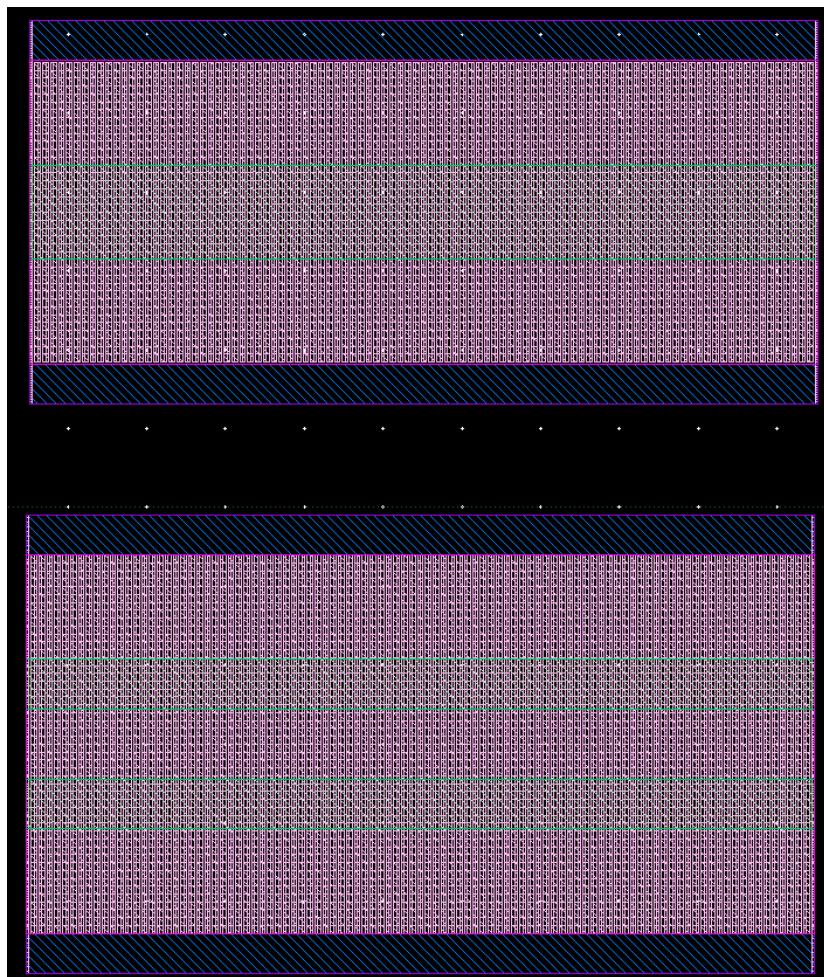




See details in section 6.2.2 (ST_C32_addon_AMS) inductances.

4.3.2 Transmission Lines

- microstrip_tline_6U1x_2T8x_LB
- differential_tline_6U1x_2T8x_LB



See details in section 6.2. (ST_C32_addon_AMS) Transmission Lines.

4.4 New devices in DK 2.9

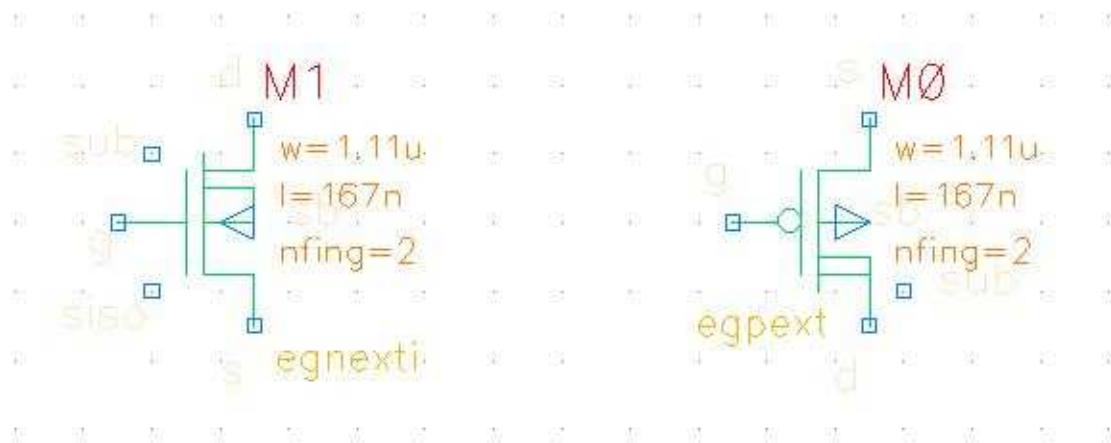
4.4.1 EDMOS

4.4.1.1 Supported Devices

- Egnexti
- Egpext



4.4.1.2 Symbol



⇒ Pins names and order :

- egnex*t* : d, g, s, sb, siso, sub
- egpext : d, g, s, sb, sub

4.4.1.3 Pcell Parameters

Parameter	Prompt	Unit	Description
description	Description		Gives the name of the model used for this device.
w	Width	m	Total gate width.
l	Length	m	Gate length
nfing	number of fingers		Number of gate fingers. This parameter must be set to an integer ≥ 1 for correct calculation of ad, as, pd and ps values. It cannot be parameterized using design variables or pPar expressions.



Parameter	Prompt	Unit	Description
Ngcon	Number of gate access		When 1 : gate contact on the bottom When 2 : gate contact on top and bottom
Ncrsd	Number of inner contact rows		When 1 : one CA column on inner sources and drains When 2 : two CA columns on inner sources and drains

4.4.1.4 Netlist Formats

The following paragraphs show the possible netlists with default parameters.

CDL :

```
.SUBCKT egnexti d g s sb siso sub w=1.11u l=167.000n m=1 nfing=2 ngcon=1 ncrsd=1
*.PININFO d:B g:B s:B sb:B siso:B sub:B
.ENDS
```

```
.SUBCKT egpext d g s sb sub w=1.11u l=167.000n m=1 nfing=2 ngcon=1 ncrsd=1
*.PININFO d:B g:B s:B sb:B sub:B
.ENDS
```

ELDO :

```
XM0 NET29 NET27 NET30 NET26 NET31 NET28 egnexti w=1.11u l=167n mult=1
+nfing=2 ngcon=1 ncrsd=1 as=133.2f ps=1.59u ad=707.07f pd=2.548u
+mismatch=1 pre_layout_local=-1 t=-274 trise=0 nsig_vto=0 nsig_uo=0 soa=1
XM1 NET33 NET35 NET32 NET34 NET36 egpext w=1.11u l=167n mult=1 nfing=2
+ngcon=1 ncrsd=1 as=133.2f ps=1.59u ad=707.07f pd=2.548u mismatch=1
+pre_layout_local=-1 t=-274 trise=0 nsig_vto=0 nsig_uo=0 soa=1
```

HSPICE :

```
xm0 net29 net27 net30 net26 net31 net28 egnexti w=1.11e-6 l=167e-9 mult=1 nfing=2 ngcon=1 ncrsd=1
as=133.2e-15 ps=1.59e-6 ad=707.07e-15 pd=2.548e-6 mismatch=1 pre_layout_local=-1 t=-274 trise=0
nsig_vto=0 nsig_uo=0 soa=1
xm1 net33 net35 net32 net34 net36 egpext w=1.11e-6 l=167e-9 mult=1 nfing=2 ngcon=1 ncrsd=1
as=133.2e-15 ps=1.59e-6 ad=707.07e-15 pd=2.548e-6 mismatch=1 pre_layout_local=-1 t=-274 trise=0
nsig_vto=0 nsig_uo=0 soa=1
```

SPECTRE :



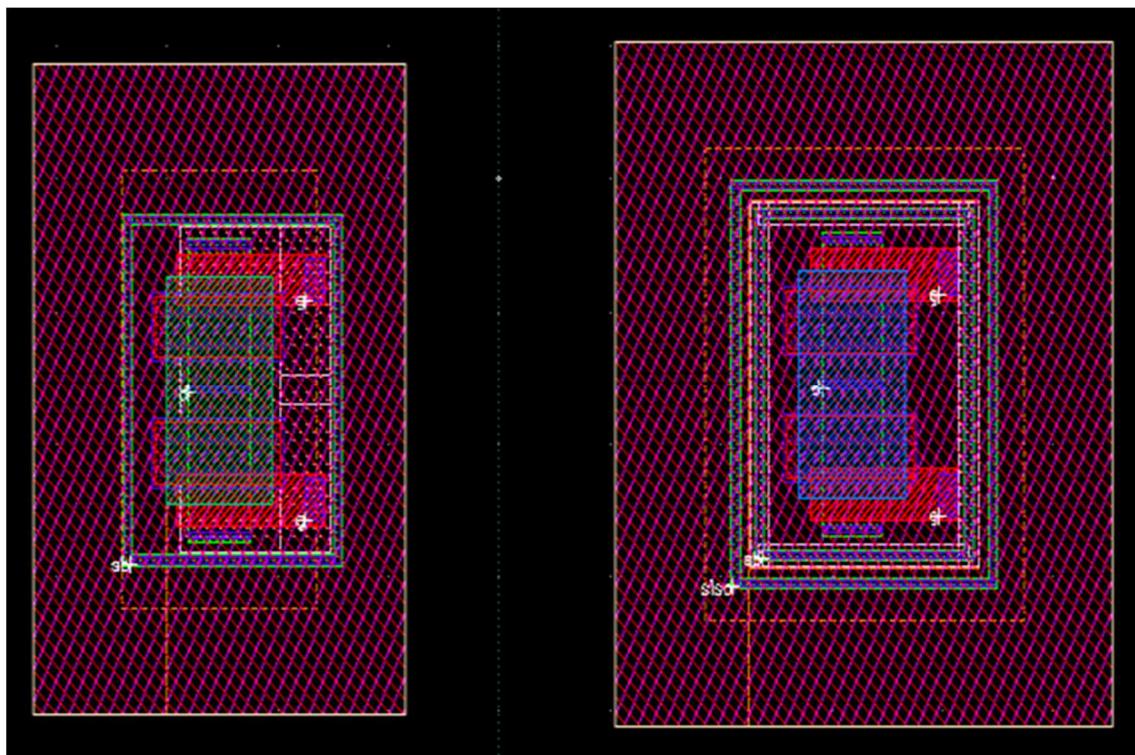


```
M0 (net27 net29 net30 net26 net31 net28) egnexti w=1.11u l=167n mult=1 nfing=2 ngcon=1 ncrsd=1  
as=133.2f ps=1.59u ad=707.07f pd=2.548u mismatch=1 pre_layout_local=-1 t=-274 trise=0 nsig_vto=0  
nsig_uo=0 soa=1
```

```
M1 (net35 net33 net32 net34 net36) egpext w=1.11u l=167n mult=1 nfing=2 ngcon=1 ncrsd=1 as=133.2f  
ps=1.59u ad=707.07f pd=2.548u mismatch=1 pre_layout_local=-1 t=-274 trise=0 nsig_vto=0 nsig_uo=0  
soa=1
```

4.4.1.5 Layout view

Example of default egpext and egnexti:



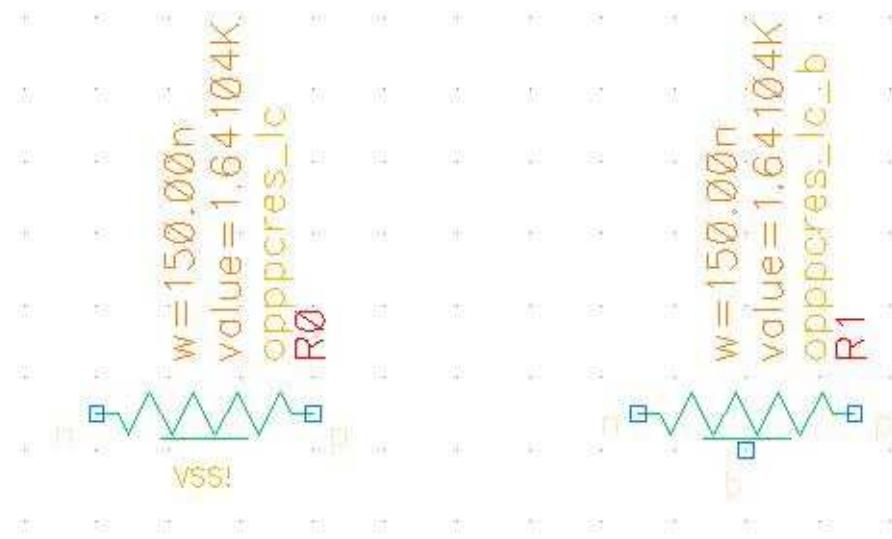
4.4.2 OPPPCRES Low Cost

4.4.2.1 Supported Devices

- Opppcres_lc
- Opppcres_lc_b



4.4.2.2 Symbol



⇒ Pins names and order :

- Opppcres_lc : p n
- Opppcres_lc_b : p n b

4.4.2.3 Pcell Parameters

Parameter	Prompt	Unit	Description
description	Description		Show the model used in this device
dimensionMode	Dimension by Geometry		Switch: User can define value and either length or width or w and l of the device
r	Value	Ohm	Total nominal resistance. Dependent on dimensionMode switch the value can be entered by the user or is calculated from given w, l, ser and par.
w	Stripe width	m	Width of one resistor stripe, can also be calculated based on l and r if switch dimensionMode is set to off.



I	Stripe length	m	Length of one resistor stripe, can also be calculated from w and r if switch dimensionMode is set to off.
ser	Series stripes		Number of resistor stripes in series. Either ser or par may be > 1.
par	Parallel stripes		Number of resistor stripes in parallel. Either ser or par may be > 1.
d	Stripe Distance	m	Pcell parameter: Distance of parallel or serial resistor stripes in layout. Minimum distance is ensured by PCell.
resbulk	Bulk		NetSet property for connecting the bulk pin. Default value is [@1Sup:%:VSS!]. Only available for cells without explicit bulk pin.
subres	Substrate Resistance	Ohm	User defined substrate resistance. Use "0" for model default.
selfHeating	Self Heating		Enable self heating in simulation model.
bp_select	Backplane Designation		Only available for polysilicon resistors. Selects resistor backplane. Options: NW, PW, T3
bp	Backplane designation		Only available for polysilicon resistors. Set by bp_select. Values: 1: NW 3: PW 4: T3 (triple well)
guardRing	Guard Ring		PCell parameter: Enables guard ring around device.
dummies	Create Dummies		PCell parameter: Places left & right dummy stripes next to device.
routingWidth	Routing width		Pcell parameter: Specifies the width of M1 routing used for connection multiple stripes. Note: Too big M1 widths will cause distance error to M1 of guard ring because of width dependent distance design rules.
contactRows	contact Rows		Pcell parameter: Specifies the numbers of CA rows in the resistor pin. Note: For all values except "1" the resulting layout will deviate from the stripe end resistance assumptions made in the simulation model.
RecommendedRulesSelect	Select Rule Sets		PCell parameter: Open rule set selection browser (see section 3.4.1).
Rule Sets	Rule Sets		PCell parameter: List of selected rule sets (see section 3.4.1).
rodObj	Enable ROD Objects		





SOA	Safe Operating Area		Check if the device conditions of use are in a safe mode
-----	---------------------	--	--

4.4.2.4 Netlist Formats

The following paragraphs show the possible netlists with default parameters.

CDL :

```
RR0 net024 net025 $SUB=VSS $[opppcres_lc] r=1.64104K w=150.00n l=400n pbar=1 s=1 bp=3 ncr=1
```

```
RR1 net038 net039 $SUB=net037 $[opppcres_lc] r=1.64104K w=150.00n l=400n pbar=1 s=1 bp=3 ncr=1
```

ELDO :

```
XR0 NET024 NET025 VSS! opppcres_lc w=150.00n l=400n r=1.64104K s=1 pbar=1
```

```
+rsx=50 bp=3 sh=1 ncr=1 mismatch=1 soa=1 acc=1 dr_mdev=0
```

```
XR1 NET038 NET039 NET037 opppcres_lc w=150.00n l=400n r=1.64104K s=1
```

```
+pbar=1 rsx=50 bp=3 sh=1 ncr=1 mismatch=1 soa=1 acc=1 dr_mdev=0
```

HSPICE :

```
xr0 net024 net025 vss! opppcres_lc w=150e-9 l=400e-9 r=1.64104e3 s_rename=1 pbar=1 rsx=50 bp=3  
sh=1 ncr=1 mismatch=1 soa=1 acc=1 dr_mdev=0
```

```
xr1 net038 net039 net037 opppcres_lc w=150e-9 l=400e-9 r=1.64104e3 s_rename=1 pbar=1 rsx=50 bp=3  
sh=1 ncr=1 mismatch=1 soa=1 acc=1 dr_mdev=0
```

SPECTRE :

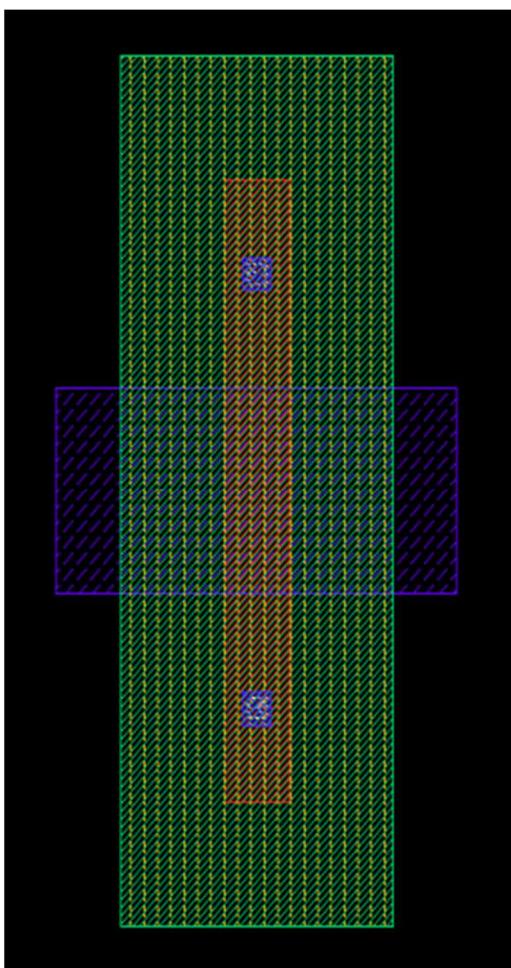
```
R0 (net024 net025 VSS!) opppcres_lc w=150.00n l=400n r=1.64104K s=1 pbar=1 rsx=50 bp=3 sh=1 ncr=1  
mismatch=1 soa=1 acc=1 dr_mdev=0
```

```
R1 (net038 net039 net037) opppcres_lc w=150.00n l=400n r=1.64104K s=1 pbar=1 rsx=50 bp=3 sh=1 ncr=1  
mismatch=1 soa=1 acc=1 dr_mdev=0
```

4.4.2.5 Layout view

Example of default opppcres_lc :





4.4.3 HLVT mosfet

HLVT mosfet is a SG flipwell mosfets.

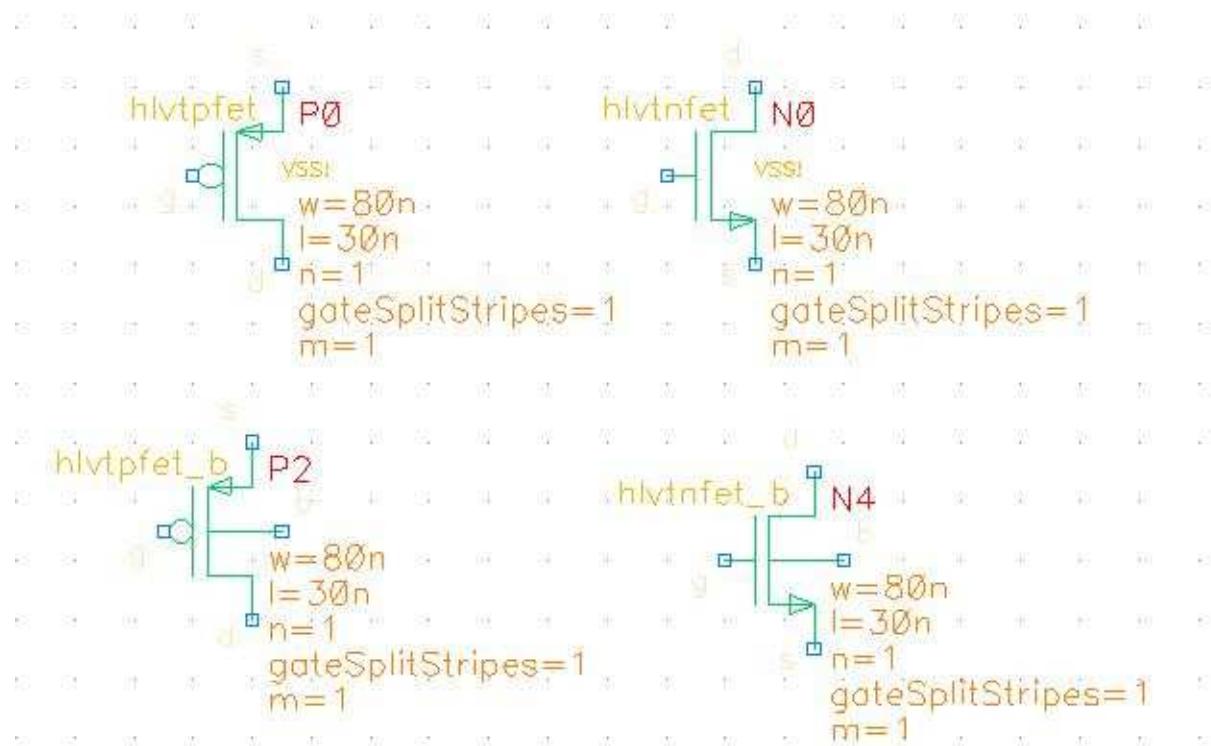
This mosfet type has the same layout view than other SG flipwell mosfets, except the marker HLVT. Device parameters are the same except matching parameters not available in models (xpos, ypos).

MOSFETS



Device	Name in DK	Flipwell	GPF	Bulk	Comment
HLVt NFET	hlvtlfet, hlvtlfet_b, hlvtlfetnp	x			ST-foundry devices for specific application. Please contact your ST support for more details
HLVt PFET	hlvtpfet, hlvtpfet_b, hlvtpfettw	x			ST-foundry devices for specific application. Please contact your ST support for more details

4.4.3.1 Symbol



Terminal order: d g s b



4.4.3.2 Inherited Connections

Cells without an explicit bulk pin use following netExpressions for the bulk pin:

Regular Devices	Bulk netExpression	Flipwell Devices	Bulk netExpression
NFET	[@lSup:%:VSS!]	NFET	[@lSup:%:VSS!]
PFET	[@hSup:%:VDD!]	PFET	[@hSup:%:VSS!]

4.4.3.3 Device Parameters

Parameter	Prompt	Unit	Description
description	Description		Gives the name of the model used for this device.
dimensionMode	Dimension Mode		Selects gate width dimension mode: TotalWidth: Enter total width, finger width is calculated FingerWidth: Enter finger width, total width is calculated
w	Total Gate Width	m	Total gate width. Editable if Dimension Mode is TotalWidth.
wf	Gate Finger Width	m	Gate finger width. Editable if Dimension Mode is FingerWidth.
l	Gate Length	m	Gate length
n	number of gate fingers		Number of gate fingers. Finger width is w/n. This parameter must be set to an integer ≥ 1 for correct calculation of ad, as, pd and ps values. It cannot be parameterized using design variables or pPar expressions.
gateSplitStripes	Gate Split Y		Number of gate splits in Y-direction. Produces individual RX shapes in device layout. Influences pd and ps calculation. This option can be used to get of the DRC rule 221D when the contact array is too long
wellSelect	Triple Well?		Local well proximity model switch. Only available for NFET regular devices and PFET flipwell devices. Selected: Triple well Unselected: Dual well
p_la_select			Selects option for gate length adder: 0: no gate length modification





Parameter	Prompt	Unit	Description
ptwell			Internal parameter for local well proximity switch. Controlled by wellSelect switch; used for netlisting. Values: 0: dual well proximity model 1: triple well proximity model
XdefDrain	XdefDrain		Specifies layout configuration of outer drain area for ad and pd calculation: Values: contact: No butting to other source/drain region (see Figure 52). stack: Drain will be abutted to another source/drain keeping contacts (see Figure 53). noStack: Drain will be abutted to another source/drain, no contacts are kept (see Figure 54). user: User have to specify ad and pd values explicitly
XdefSource	XdefSource		Same as XdefDrain for outer source area. Used for calculation of as and ps.
ad, as, ps, pd	Total Drain Area, Perimeter Total Source Area, Perimeter	m	Values for source/drain area and perimeter. Automatically computed unless 'user' is selected for XdefDrain/XdefSource. The values computed are based on the values of parameters w, n, gateSplitStripes, XdefDrain and XdefSource. Only editable if 'user' is selected for XdefDrain/XdefSource.
stiStress	Change STI Stress Estimation?		Switch for changing the STI stress estimation values. Controls display of parameters sa, sb and sd.
sa, sb, sd	STI Compression (sa), STI Compression (sb), STI Compression (sd)	m	STI compression values. sa, sb: Distance gate to RX edge for outer source/drain regions sd: Distance between gates.
dummyPoly	ACLV PC Fill		PCell parameter: Selects ACLV dummy PC generation in device layout: Values: none: no dummy PC Left: Dummy PC on left side Right: Dummy PC on right side Both: Dummy PC on left and right side





Parameter	Prompt	Unit	Description
cnt	cnt		PCell parameter: Controls creation of contacts (CA) in outer source/drain regions of device layout.
cntBLR	cntBLR		PCell parameter: Controls creation of contacts (CA) in left and right source/drain region. Only displayed if cnt is selected. Values: Both: Create contacts on left and right side. Left: Create contacts just on left side. Right: Create contacts just on right side.
polyCnt	Poly Contact		PCell parameter: Enables gate contact to M1.
PolyRoute	PolyRoute		PCell parameter: Enables PC routing of gates for multi finger devices.
Pw	Poly Route Width	m	PCell parameter: Controls width of PC routing. Minimum PC width is ensured by PCell.
guardRing	Guard Ring		PCell parameter: Enables guard ring around device.
gr_stubs	Guard Ring Segments		PCell parameter: Selects guard ring segments around device
gr_stubs2	Second Guard Ring Segments		PCell parameter: Selects guard ring segments around device
M1Route	M1Route		PCell parameter: Enables M1 routing of source/drain regions for multi finger devices.
minRoute	minRoute		PCell parameter: Controls width of M1 routing. If selected, minimum M1 width is used. Otherwise, routing width is adjusted to width of source/drain M1.
distRoute	distRoute	m	PCell parameter: Controls distance of M1 routing to adjacent source/drain M1. PCell ensures minimum distance.
Sw	Source Width	m	PCell parameter: Controls width of M1 on source.
Dw	Drain Width	m	PCell parameter: Controls width of M1 on drain.
BP_Extension	BP ext. on OD		Available only with Robust Rules. Allow to reduce BP enclosure.
sContSD	S/D contact spacing (um)	Um	Used to choose your own contact spacing on source/drain
eeDiffCont	RX min overlap past contact on top and bottom (um)	um	Use to choose your own min overlap of RX on CA for top and bottom sides. This option causes an impact on number of CA.
M1SD	Add M1 on S/D		M1 is drawn on not on contacts source, drain.
RecommendedRulesSelect	Select Rule Sets		PCell parameter: Open rule set selection browser (see section 3.4.1).



Parameter	Prompt	Unit	Description
RecommendedRules	Rule Sets		PCell parameter: List of selected rule sets (see section 3.4.1).
ngcon	Number of Gate Contacts		Switch for number of gate contacts. Valid values: 1, 2
plorient	plorient		Orientation of gate: 1: preferred orientation (gate width along x-axis) 2: non preferred orientation
par, psw_acv_sign, plnest, pdevdops, pdevlgeos, pdevwgeos, pld200, p_vta, cnr_switch, sca, scb, scc, u0_mult, pre_layout_local, p_la, lpccnr, covpccnr, wrxcnr			See Model Reference Guide for details.
m	Multiplicity		Number of parallel devices
SOA	Safe Operating Area		Check if the device conditions of use are in a safe mode

Table 8: MOSFET parameters

4.4.3.4 Netlist Formats

The following paragraphs show different netlist for a NFET whit default parameters.

CDL

```
MN0 net2 net3 net1 VSS hlvtnfet m=1 xpos=-1.0 ypos=-1.0 w=80n l=30n nf=1.0 plorient=1 ngcon=1 p_la=0
ptwell=0 swacc=-1 swrg=1 mismatch=1
```

```
MP0 net11 net9 net10 VSS hlvtperf m=1 xpos=-1.0 ypos=-1.0 w=80n l=30n nf=1.0 plorient=1 ngcon=1
p_la=0 ptwell=0 swacc=-1 swrg=1 mismatch=1
```

```
MN4 net040 net041 net042 net043 hlvtnfet m=1 xpos=-1.0 ypos=-1.0 w=80n l=30n nf=1.0 plorient=1
ngcon=1 p_la=0 ptwell=0 swacc=-1 swrg=1 mismatch=1
```

```
MP2 net047 net045 net046 net044 hlvtperf m=1 xpos=-1.0 ypos=-1.0 w=80n l=30n nf=1.0 plorient=1
ngcon=1 p_la=0 ptwell=0 swacc=-1 swrg=1 mismatch=1
```

ELDO

```
XN0 NET2 NET3 NET1 VSS! hlvtnfet w=80n l=30n as=6.08f ad=6.08f ps=232n
+pd=232n nf={(1)*(1)} sa=76n sb=76n sd=96n ptwell=0 par=1 sca=-1 scb=-1
+scc=-1 pre_layout_local=-1 p_la=0 lpccnr=0 covpccnr=0 ngcon=1 wrxcnr=0
+nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 mismatch=1 m=1
+xpos=-1 ypos=-1 plorient=1 plsnf=0
```

```
XP0 NET11 NET9 NET10 VSS! hlvtperf w=80n l=30n as=6.08f ad=6.08f ps=232n
+pd=232n nf={(1)*(1)} sa=76n sb=76n sd=96n ptwell=0 par=1 sca=-1 scb=-1
```





```
+scc=-1 pre_layout_local=-1 p_la=0 lpccnr=0 covpccnr=0 ngcon=1 wrxcnr=0
+nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 mismatch=1 m=1
+xpos=-1 ypos=-1 plorient=1 plsnf=0
XN4 NET040 NET041 NET042 NET043 hlvtlfet w=80n l=30n as=6.08f ad=6.08f
+ps=232n pd=232n nf={(1)*(1)} sa=76n sb=76n sd=96n ptwell=0 par=1 sca=-1
+scb=-1 scc=-1 pre_layout_local=-1 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
+wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1
+mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
XP2 NET047 NET045 NET046 NET044 hlvtlfet w=80n l=30n as=6.08f ad=6.08f
+ps=232n pd=232n nf={(1)*(1)} sa=76n sb=76n sd=96n ptwell=0 par=1 sca=-1
+scb=-1 scc=-1 pre_layout_local=-1 p_la=0 lpccnr=0 covpccnr=0 ngcon=1
+wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1
+mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
```

HSPICE

```
xn0 net2 net3 net1 vss! hlvtlfet w=80e-9 l=30e-9 as=6.08e-15 ad=6.08e-15 ps=232e-9 pd=232e-9 nf=1
sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 par=1 sca=-1 scb=-1 scc=-1 pre_layout_local=-1 p_la=0 lpccnr=0
covpccnr=0 ngcon=1 wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 mismatch=1
m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
```

```
xp0 net11 net9 net10 vss! hlvtlfet w=80e-9 l=30e-9 as=6.08e-15 ad=6.08e-15 ps=232e-9 pd=232e-9 nf=1
sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 par=1 sca=-1 scb=-1 scc=-1 pre_layout_local=-1 p_la=0 lpccnr=0
covpccnr=0 ngcon=1 wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 mismatch=1
m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
```

```
xn4 net040 net041 net042 net043 hlvtlfet w=80e-9 l=30e-9 as=6.08e-15 ad=6.08e-15 ps=232e-9 pd=232e-9
nf=1 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 par=1 sca=-1 scb=-1 scc=-1 pre_layout_local=-1 p_la=0
lpccnr=0 covpccnr=0 ngcon=1 wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1
mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
```

```
xp2 net047 net045 net046 net044 hlvtlfet w=80e-9 l=30e-9 as=6.08e-15 ad=6.08e-15 ps=232e-9 pd=232e-9
nf=1 sa=76e-9 sb=76e-9 sd=96e-9 ptwell=0 par=1 sca=-1 scb=-1 scc=-1 pre_layout_local=-1 p_la=0
lpccnr=0 covpccnr=0 ngcon=1 wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1
mismatch=1 m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
```

SPECTRE

```
N0 (net2 net3 net1 VSS!) hlvtlfet w=80n l=30n as=6.08f ad=6.08f ps=232n pd=232n nf={(1)*(1)} sa=76n
sb=76n sd=96n ptwell=0 par=1 sca=-1 scb=-1 scc=-1 pre_layout_local=-1 p_la=0 lpccnr=0 covpccnr=0
ngcon=1 wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 mismatch=1 m=1 xpos=
1 ypos=-1 plorient=1 plsnf=0
```

```
P0 (net11 net9 net10 VSS!) hlvtlfet w=80n l=30n as=6.08f ad=6.08f ps=232n pd=232n nf={(1)*(1)} sa=76n
sb=76n sd=96n ptwell=0 par=1 sca=-1 scb=-1 scc=-1 pre_layout_local=-1 p_la=0 lpccnr=0 covpccnr=0
ngcon=1 wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 mismatch=1 m=1 xpos=
1 ypos=-1 plorient=1 plsnf=0
```

```
N4 (net040 net041 net042 net043) hlvtlfet w=80n l=30n as=6.08f ad=6.08f ps=232n pd=232n nf={(1)*(1)}
sa=76n sb=76n sd=96n ptwell=0 par=1 sca=-1 scb=-1 scc=-1 pre_layout_local=-1 p_la=0 lpccnr=0
```



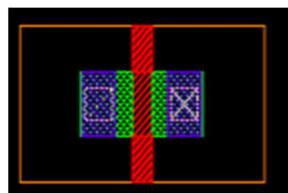


```
covpccnr=0 ngcon=1 wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 mismatch=1  
m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
```

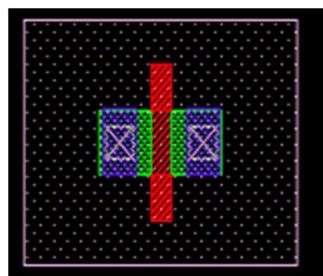
```
P2 (net047 net045 net046 net044) hlvtperfet w=80n l=30n as=6.08f ad=6.08f ps=232n pd=232n nf=(1)*(1)  
sa=76n sb=76n sd=96n ptwell=0 par=1 sca=-1 scb=-1 scc=-1 pre_layout_local=-1 p_la=0 lpccnr=0  
covpccnr=0 ngcon=1 wrxcnr=0 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 mismatch=1  
m=1 xpos=-1 ypos=-1 plorient=1 plsnf=0
```

4.4.3.5 Layout PCell

Example of pcell view with default parameters:



HLVTnfet:



HLVTpfet:

4.4.4 SRAM SP126

4.4.4.1 Supported device types

SRAM				
Device	Name in DK	Flipwell	GPF	Bulk
Single Well Dense Cell 0.126 PG NFET (SP0126SW)	dsxnftwl_b	x		

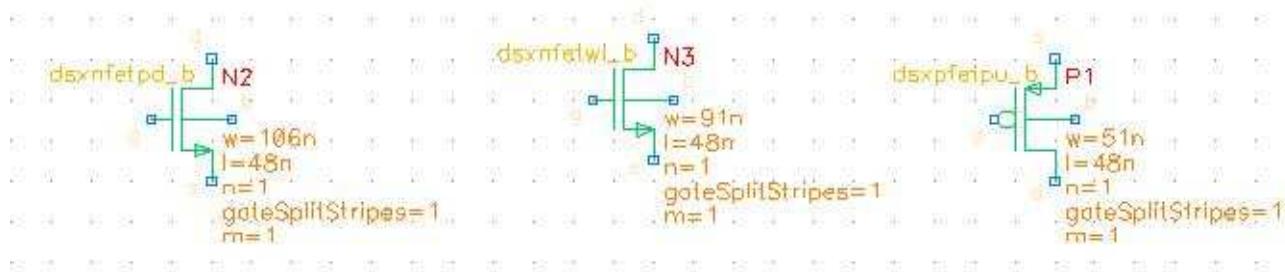




Single Well Dense Cell 0.126 PD NFET (SP0126SW)	dsxfetpd_b	x	
Single Well Dense Cell 0.126 PU PFET (SP0126SW)	dsxpfeipu_b	x	

ST-foundry devices for specific application. Please contact your ST support for more details

4.4.4.2 Symbol



Terminal order: d g s b

4.4.4.3 Device Parameters

Parameter	Prompt	Unit	Description
description	Description		Gives the name of the model used for this device.
dimensionMode	Dimension Mode		Selects gate width dimension mode: TotalWidth: Enter total width, finger width is calculated FingerWidth: Enter finger width, total width is calculated
w	Total Gate Width	m	Total gate width. Editable if Dimension Mode is TotalWidth.
wf	Gate Finger Width	m	Gate finger width. Editable if Dimension Mode is FingerWidth.
l	Gate Length	m	Gate length
n	number of gate fingers		Number of gate fingers. Finger width is w/n. This parameter must be set to an integer ≥ 1 for correct calculation of ad, as, pd and ps values. It cannot be parameterized using design variables or pPar expressions.
gateSplitStripes	Gate Split Y		Number of gate splits in Y-direction. Produces individual RX shapes in device layout. Influences pd and ps calculation.





Parameter	Prompt	Unit	Description
pccrit	pccrit		Internal parameter for ACLV parameter selection. Controlled by pccrit_select; used for netlisting. Value: 0: Aclv parameters set to non-critical values
XdefDrain	XdefDrain		Specifies layout configuration of outer drain area for ad and pd calculation: Values: contact: No butting to other source/drain region (see Figure 52). stack: Drain will be abutted to another source/drain keeping contacts (see Figure 53). noStack: Drain will be abutted to another source/drain, no contacts are kept (see Figure 54). user: User have to specify ad and pd values explicitly
XdefSource	XdefSource		Same as XdefDrain for outer source area. Used for calculation of as and ps.
ad, as, pd, ps	Total Drain Area, Total Source Area, Drain Periphery, Source Periphery	m	Values for source/drain area, perimeter. Automatically calculated unless 'user' is selected for XdefDrain/XdefSource. The values are calculated based on the values of parameters w, n, gateSplitStripes, XdefDrain and XdefSource. Only editable if 'user' is selected for XdefDrain/XdefSource.
plorient	plorient		Orientation of gate: 1: preferred orientation (gate width along x-axis) 2: non preferred orientation
par, psw_acv_sign, plnest, pdevdops, pdevlgeos, pdevwgeos, pld200, p_vta, cnr_switch, sca, scb, scc, u0_mult, pre_layout_local, p_la, lpccnr, covpccnr, wrxcnr			See Model Reference Guide for details.
m	Multiplicity		Number of parallel devices

4.4.4.4 Netlist Formats

CDL

```
MN2 net12 net13 net14 net15 dsxnftetpd m=1 w=106n l=48n nf=1.0 p_la=0 ngcon=1
MN3 net16 net17 net18 net19 dsxnftetwl m=1 w=91n l=48n nf=1.0 p_la=0 ngcon=1
MP1 net23 net21 net22 net20 dsxpfetpu m=1 w=51n l=48n nf=1.0 p_la=0 ngcon=1
```



ELDO

```
XN2 NET12 NET13 NET14 NET15 dsxnftetpd w=106n l=48n as=9.01f ad=9.01f
+ps=276n pd=276n nf={(1)*(1)} par=1 pre_layout_local=-1 nsig_delvto_uo1=0
+nsig_delvto_uo2=0 soa=1 mismatch=1 m=1
XN3 NET16 NET17 NET18 NET19 dsxnftetwl w=91n l=48n as=7.735f ad=7.735f
+ps=261n pd=261n nf={(1)*(1)} par=1 pre_layout_local=-1 nsig_delvto_uo1=0
+nsig_delvto_uo2=0 soa=1 mismatch=1 m=1
XP1 NET23 NET21 NET22 NET20 dsxpfetpu w=51n l=48n as=4.335f ad=4.335f
+ps=221n pd=221n nf={(1)*(1)} par=1 pre_layout_local=-1 nsig_delvto_uo1=0
+nsig_delvto_uo2=0 soa=1 mismatch=1 m=1
```

HSPICE

```
xn2 net12 net13 net14 net15 dsxnftetpd w=106e-9 l=48e-9 as=9.01e-15 ad=9.01e-15 ps=276e-9 pd=276e-9
nf=1 par=1 pre_layout_local=-1 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 mismatch=1 m=1
xn3 net16 net17 net18 net19 dsxnftetwl w=91e-9 l=48e-9 as=7.735e-15 ad=7.735e-15 ps=261e-9 pd=261e-9
nf=1 par=1 pre_layout_local=-1 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 mismatch=1 m=1
xp1 net23 net21 net22 net20 dsxpfetpu w=51e-9 l=48e-9 as=4.335e-15 ad=4.335e-15 ps=221e-9 pd=221e-9
nf=1 par=1 pre_layout_local=-1 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 mismatch=1 m=1
```

SPECTRE

```
N2 (net12 net13 net14 net15) dsxnftetpd w=106n l=48n as=9.01f ad=9.01f ps=276n pd=276n nf=(1)*(1)
par=1 pre_layout_local=-1 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 mismatch=1 m=1
N3 (net16 net17 net18 net19) dsxnftetwl w=91n l=48n as=7.735f ad=7.735f ps=261n pd=261n nf=(1)*(1)
par=1 pre_layout_local=-1 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 mismatch=1 m=1
P1 (net23 net21 net22 net20) dsxpfetpu w=51n l=48n as=4.335f ad=4.335f ps=221n pd=221n nf=(1)*(1)
par=1 pre_layout_local=-1 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 mismatch=1 m=1
```

4.4.4.5 Layout PCell Rule Sets

No layout for this type of device.



4.5 MOS RF

From DesignKit 2.8, the 28FDSOI offer includes specific mosfets optimized for RF designs.

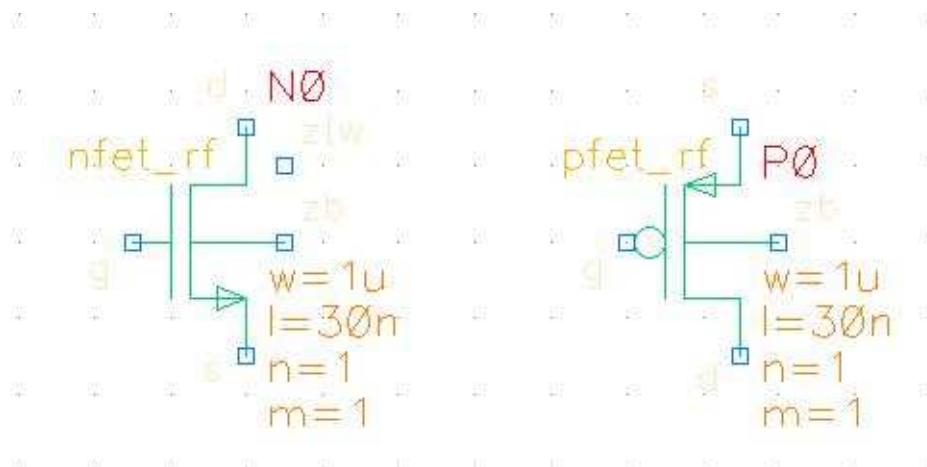
Main differences with standard mosfets are layout of the gate contact and the guardring.

Some additional pcell parameters on source and drain contacts allow more accurate designs.

4.5.1 Supported Devices

- nfet_rf
- pfet_rf
- lvtnfet_rf
- lvtpfet_rf
- eglvtnfet_rf
- eglvtpfet_rf
- egvlvtnfet_rf
- egvlvtpfet_rf

4.5.2 Symbol

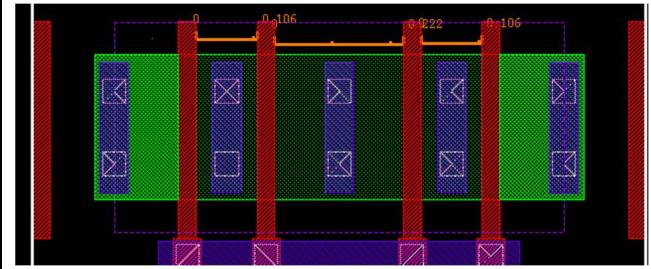


⇒ Pins names and order :

- Models :
 - lvtnfet, pfet, eglvtnfet, egvlvtnfet : d, g, s, b
 - lvtpfet, nfet, eglvtpfet, egvlvtpfet : d, g, s, b, tw
- pcell/symbol/LVS :
 - lvtnfet, pfet, eglvtnfet, egvlvtnfet : d, g, s, zb
 - lvtpfet, nfet, eglvtpfet, egvlvtpfet : d, g, s, zb, ztw

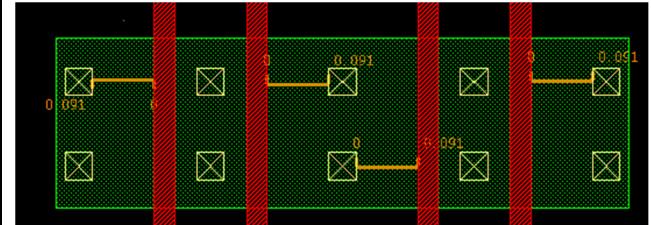
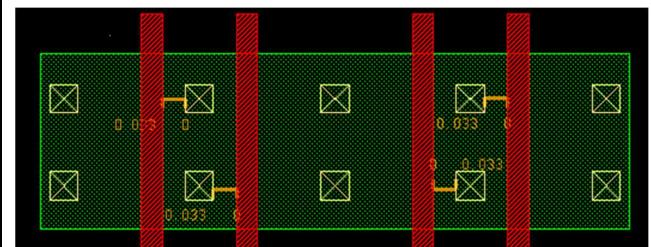


4.5.3 Pcell Parameters

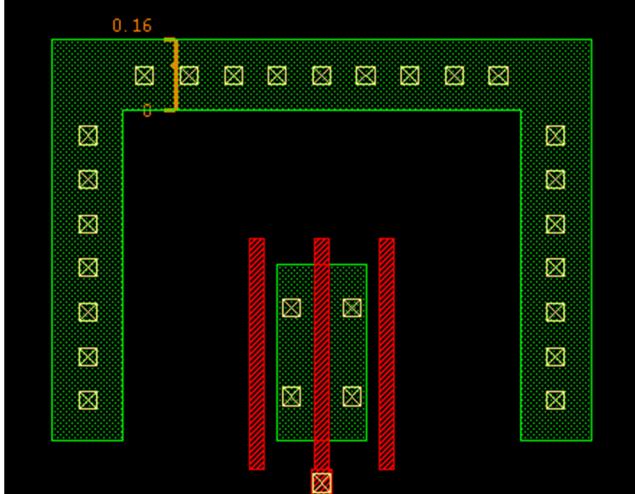
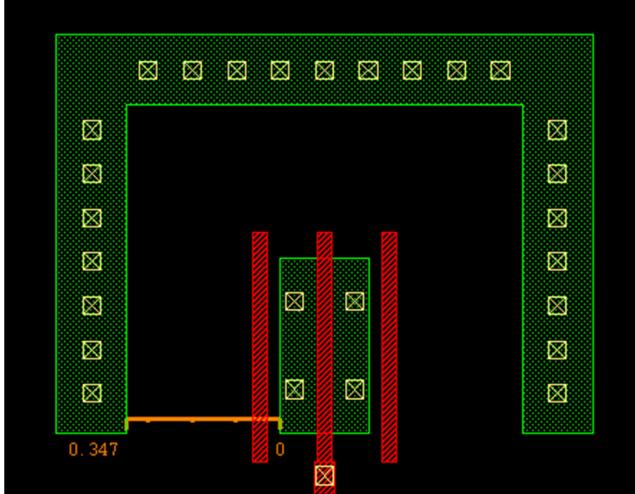
Parameter	Prompt	Unit	Description
description	Description		Gives the name of the model used for this device.
dimensionMode	Dimension Mode		Selects gate width dimension mode: TotalWidth: Enter total width, finger width is calculated FingerWidth: Enter finger width, total width is calculated
w	Total Gate Width	m	Total gate width. Editable if Dimension Mode is TotalWidth.
wf	Gate Finger Width	m	Gate finger width. Editable if Dimension Mode is FingerWidth.
l	Gate Length	m	Gate length
n	number of gate fingers		Number of gate fingers. Finger width is w/n. This parameter must be set to an integer ≥ 1 for correct calculation of ad, as, pd and ps values. It cannot be parameterized using design variables or pPar expressions.
Ngcon	Number of gate accesses		When 1 : gate contact on the bottom When 2 : gate contact on top and bottom
Sd	Average Poly Spacing	m	Average value off all poly spacings Example:  Sd is $(0.106\text{um}+0.222\text{um}+0.106\text{um})/3 = 0.1446667$ $\Leftrightarrow Sd=145\text{nm}.$
Ncrg	Number of gate contact rows		When 1 : one CA row on gate contact When 2 : two CA rows on gate contact
Ncrs	Number of contact rows on inner source		When 0 : no CA on inner sources When 1 : one CA column on inner sources When 2 : two CA columns on inner sources
Ncrd	Number of contact rows on inner drain		When 0 : no CA on inner drains When 1 : one CA column on inner drains When 2 : two CA columns on inner drains





Parameter	Prompt	Unit	Description
numcoMax	Maximum number of contacts		When true: numcos and numcod are non-editable and set to maximum allowed value according to current configuration.
Numcos	Number of contact per row on source		Number of CA contact per row on source
Pocos	Distance contact to gate on source	m	Example : pocos=91nm 
Numcod	Number of contact per row on drain		Number of CA contact per row on drain
Pocod	Distance contact to gate on drain	m	Example : pocod=33nm 
grStubs	Guardring segments		Selects guardring segments around device. L-shapes are not authorized
Strap	Netlisted strap		Each guardring shape (choice with grStubs parameter) corresponds to a netlisted value used in model: 3 = LTB or TBR 2 = TB 1 = T or B 0 = all -1 = L or R -2 = LR -3 = LTR or LBR
Ptwell	Presence of deep nwell		Deep nwell is not drawn in the pcell. The designer must put this parameter to 1 if he needs deep nwell in his design.



Parameter	Prompt	Unit	Description
Wstrap	Strap width	m	
Strap2rx	Distance strap to RX	m	
m	Multiplicity		Number of parallel devices

4.5.4 Netlist Formats

The following paragraphs show the possible netlists with default parameters.

- 4-pin devices: lvtnfet, pfet, eglvtnfet, egvlvtnfet

CDL :

```
*****
* Library Name: cmos32lp
* Cell Name: pfet_rf
* View Name: schematic
*****
```





```
.SUBCKT pfet_rf d g s zb w=1u l=30.00n plorient=1 ngcon=1 ptwell=0 soa=1 swrg=1 strap2rx=347n
wstrap=160n strap=2 ncrg=2 nf=1 m=1
*.PININFO d:B g:B s:B zb:B
.ENDS
```

```
*****
```

```
* Library Name: test
* Cell Name: schem3
* View Name: schematic
*****
```

```
.SUBCKT schem3
*.PININFO
XP0 net4 net2 net3 net1 pfet_rf m=1 w=1u l=30n plorient=1 ngcon=1 ptwell=0 soa=1 swrg=1
strap2rx=347n wstrap=160n strap=2 ncrg=2 nf=1
.ENDS
```

ELDO :

```
XP0 NET4 NET2 NET3 NET1 pfet_rf w=1u l=30n as=87f ad=87f ps=1.174u
+pd=1.174u nf=1 m=1 sa=87n sb=87n sd=106n ptwell=0 par=1 p_vta=0 sca=-1
+scb=-1 scc=-1 u0_mult=1 pre_layout_local=-1 ngcon=1 nsig_delvto_uo1=0
+nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 mismatch=1 numcos=10 pocos=33n
+numcod=10 pocod=33n xpos=-1 ypos=-1 plorient=1 ncrs=1 ncrd=1 ncrg=2
+strap=2 wstrap=160n plsnf=0 strap2rx=347n
```

HSPICE :

```
xp0 net4 net2 net3 net1 pfet_rf w=1e-6 l=30e-9 as=87e-15 ad=87e-15 ps=1.174e-6 pd=1.174e-6 nf=1
m=1 sa=87e-9 sb=87e-9 sd=106e-9 ptwell=0 par=1 p_vta=0 sca=-1 scb=-1 scc=-1 u0_mult=1
pre_layout_local=-1 ngcon=1 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1
mismatch=1 numcos=10 pocos=33e-9 numcod=10 pocod=33e-9 xpos=-1 ypos=-1 plorient=1 ncrs=1
ncrd=1 ncrg=2 strap=2 wstrap=160e-9 plsnf=0 strap2rx=347e-9
```

SPECTRE :

```
P0 (net4 net2 net3 net1) pfet_rf w=1u l=30n as=87f ad=87f ps=1.174u pd=1.174u nf=(1)*(1) m=1
sa=87n sb=87n sd=106n ptwell=0 par=1 p_vta=0 sca=-1 scb=-1 scc=-1 u0_mult=1 pre_layout_local=-1
ngcon=1 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 mismatch=1 numcos=10
pocos=33n numcod=10 pocod=33n xpos=-1 ypos=-1 plorient=1 ncrs=1 ncrd=1 ncrg=2 strap=2
wstrap=160n plsnf=0 strap2rx=347n
```





- 5-pin devices: lvtpfet, nfet, eglvtpfet, egvlvtpfet

CDL:

```
*****
```

```
* Library Name: cmos32lp
* Cell Name: nfet_rf
* View Name: schematic
```

```
*****
```

```
.SUBCKT nfet_rf d g s zb ztw m=1 w=1u l=30.00n plorient=1 ngcon=1 ptwell=0 soa=1 swrg=1
strap2rx=347n wstrap=160n strap=2 ncrg=2 nf=1
```

```
*.PININFO d:B g:B s:B zb:B ztw:B
.ENDS
```

```
*****
```

```
* Library Name: test
* Cell Name: schem3
* View Name: schematic
```

```
*****
```

```
.SUBCKT schem3
```

```
*.PININFO
XN0 net6 net7 net8 net5 net9 nfet_rf w=1u l=30n plorient=1 ngcon=1 ptwell=0 soa=1 swrg=1
strap2rx=347n wstrap=160n strap=2 ncrg=2 nf=1 m=1
.ENDS
```

ELDO:

```
XN0 NET6 NET7 NET8 NET5 NET9 nfet_rf w=1u l=30n as=87f ad=87f ps=1.174u
+pd=1.174u nf={(1)*(1)} m=1 sa=87n sb=87n sd=106n ptwell=0 par=1 p_vta=0
+sca=-1 scb=-1 scc=-1 u0_mult=1 pre_layout_local=-1 ngcon=1
+nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1 mismatch=1
+numcos=10 pocos=33n numcod=10 pocod=33n xpos=-1 ypos=-1 plorient=1 ncrs=1
+ncrd=1 ncrg=2 strap=2 wstrap=160n plsrf=0 strap2rx=347n
```

HSPICE:

```
xn0 net6 net7 net8 net5 net9 nfet_rf w=1e-6 l=30e-9 as=87e-15 ad=87e-15 ps=1.174e-6 pd=1.174e-6
nf=1 m=1 sa=87e-9 sb=87e-9 sd=106e-9 ptwell=0 par=1 p_vta=0 sca=-1 scb=-1 scc=-1 u0_mult=1
pre_layout_local=-1 ngcon=1 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1
```





```
mismatch=1 numcos=10 pocos=33e-9 numcod=10 pocod=33e-9 xpos=-1 ypos=-1 plorient=1 ncrs=1
ncrd=1 ncrg=2 strap=2 wstrap=160e-9 plsnf=0 strap2rx=347e-9
```

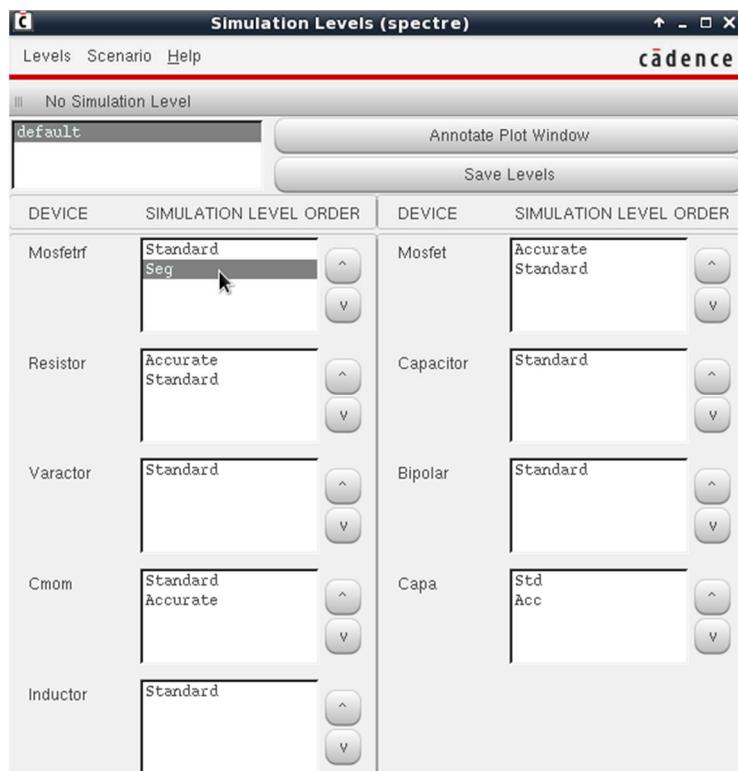
SPECTRE :

```
N0 (net6 net7 net8 net5 net9) nfet_rf w=1u l=30n as=87f ad=87f ps=1.174u pd=1.174u nf=(1)*(1)
m=1 sa=87n sb=87n sd=106n ptwell=0 par=1 p_vta=0 sca=-1 scb=-1 scc=-1 u0_mult=1
pre_layout_local=-1 ngcon=1 nsig_delvto_uo1=0 nsig_delvto_uo2=0 soa=1 swshe=0 swrg=1
mismatch=1 numcos=10 pocos=33n numcod=10 pocod=33n xpos=-1 ypos=-1 plorient=1 ncrs=1
ncrd=1 ncrg=2 strap=2 wstrap=160n plsnf=0 strap2rx=347n
```

4.5.5 Level of simulation

The default simLevel is the “standard” level.

The level “segment” is also available in the ArtistKit simLevel menu:

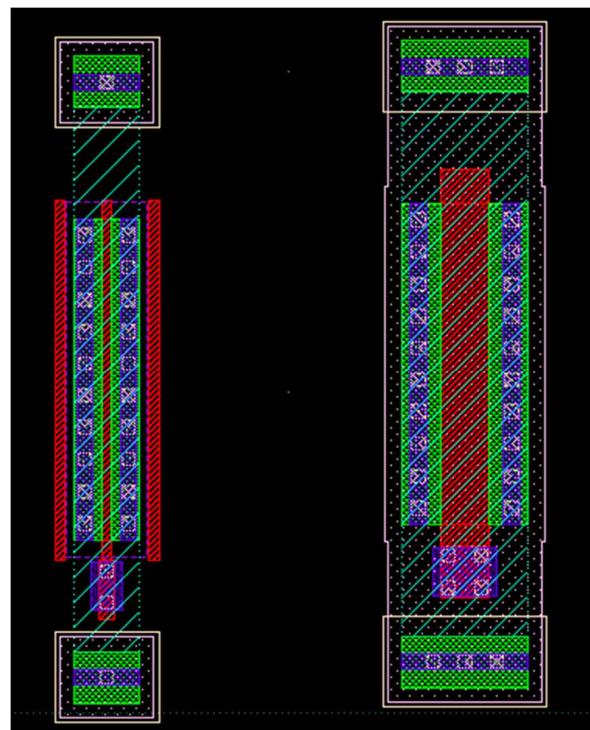


See model documentation for more information.

4.5.6 Layout view

Example of default nfet_rf and egpfet_rf:





4.6 MOSFET

4.6.1 Supported Device Types

MOSFETS					
Device	Name in DK	Flipwell	GPF	Bulk	Comment
Regular-Vt NFET	nfet, nfet_b, nfettw	x			
Regular-Vt PFET	pfet, pfet_b, pfetnp	x			
Low-Vt NFET	lvtnfet, lvtnfet_b, lvtnfetnp	x			
Low-Vt PFET	lvtpfet, lvtpfet_b, lvtpfettw	x			
1.5 V IO NFET 28A	egvnfet, egnfet_b, egnfettw		x		
1.5 V IO PFET 28A	egvpfet, egvpfet_b, egvpfetnp		x		
1.8 V IO NFET 28A	egnfet, egnfet_b, egnfettw		x		
1.8 V IO PFET 28A	egpfet, egpfet_b, egpfetnp		x		



1.8 V IO Low Vt NFET 28A	eglvtlfet, eglvtlfet_b, eglvtlfetnp	x		
1.8 V IO Low Vt PFET 28A	eglvtppfet, eglvtppfet_b, eglvtppfettw	x		
1.5 V IO Low Vt NFET 28A	eglvtlfet, eglvtlfet_b, eglvtlfetnp	x		
1.5 V IO Low Vt PFET 28A	eglvtppfet, eglvtppfet_b, eglvtppfettw	x		
Powerswitch PFET	eglvtppfet, eglvtppfet_b, eglvtppfettw	x		
OTP NMOS drift	ndriftotp		x	Anti-fuse application

Table 9: MOSFET device types and cells

4.6.2 Symbol

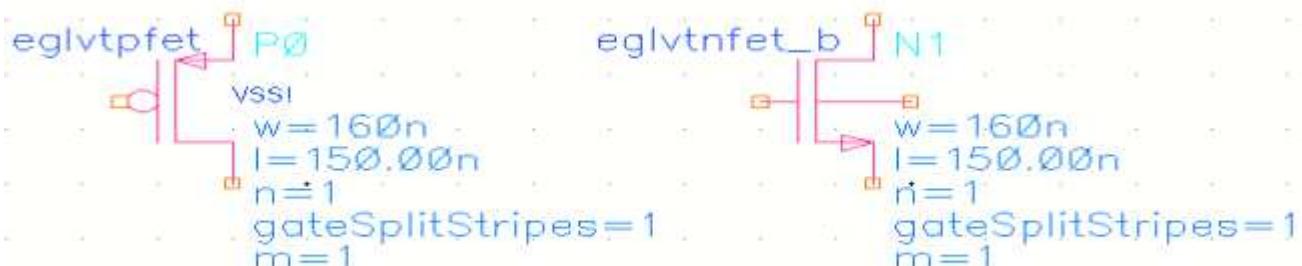


Figure 51: MOSFET symbol

Terminal order: d g s b

4.6.3 Inherited Connections

Cells without an explicit bulk pin use following netExpressions for the bulk pin:

Regular Devices	Bulk netExpression	Flipwell Devices	Bulk netExpression
NFET	[@lSup:%:VSS!]	NFET	[@lSup:%:VSS!]
PFET	[@hSup:%:VDD!]	PFET	[@hSup:%:VSS!]

4.6.4 Device Parameters

Parameter	Prompt	Unit	Description





Parameter	Prompt	Unit	Description
description	Description		Gives the name of the model used for this device.
dimensionMode	Dimension Mode		Selects gate width dimension mode: TotalWidth: Enter total width, finger width is calculated FingerWidth: Enter finger width, total width is calculated
w	Total Gate Width	m	Total gate width. Editable if Dimension Mode is TotalWidth.
wf	Gate Finger Width	m	Gate finger width. Editable if Dimension Mode is FingerWidth.
l	Gate Length	m	Gate length
n	number of gate fingers		Number of gate fingers. Finger width is w/n. This parameter must be set to an integer ≥ 1 for correct calculation of ad, as, pd and ps values. It cannot be parameterized using design variables or pPar expressions.
gateSplitStripes	Gate Split Y		Number of gate splits in Y-direction. Produces individual RX shapes in device layout. Influences pd and ps calculation. This option can be used to get of the DRC rule 221D when the contact array is too long
wellSelect	Triple Well?		Local well proximity model switch. Only available for NFET regular devices and PFET flipwell devices. Selected: Triple well Unselected: Dual well
tieDown	tieDown		Selects if tieDownPlacement parameter is displayed.
pccrit_select			ACLV parameter selection switch. If selected critical ACLV parameters are chosen for simulation and the PC/crit marking layer will be added to the device layout. Sets internal parameter pccrit and adds PCCRIT to Rule Sets. See Model Reference Guide for more details on simulation behavior.
pccrit	pccrit		Internal parameter for ACLV parameter selection. Controlled by pccrit_select; used for netlisting. Value: 0: Aclv parameters set to non-critical values
p_la_select			Selects option for gate length adder: 0: no gate length modification





Parameter	Prompt	Unit	Description
ptwell			<p>Internal parameter for local well proximity switch. Controlled by wellSelect switch; used for netlisting.</p> <p>Values:</p> <p>0: dual well proximity model 1: triple well proximity model</p>
tieDown	tieDown		Give the possibility to considerer tie down diode
tieDownPlacement	If tieDown = 1: tieDown Placement		<p>Controls tie-down diode generation in device layout.</p> <p>Values:</p> <p>none: layout will not have a tie-down diode intern: layout will have tie-down diode connected to the gate via M1; the location of the tie-down diode can be adjusted using a stretch handle</p>
XdefDrain	XdefDrain		<p>Specifies layout configuration of outer drain area for ad and pd calculation:</p> <p>Values:</p> <p>contact: No butting to other source/drain region (see Figure 52).</p> <p>stack: Drain will be abutted to another source/drain keeping contacts (see Figure 53).</p> <p>noStack: Drain will be abutted to another source/drain, no contacts are kept (see Figure 54).</p> <p>user: User have to specify ad and pd values explicitly</p>
XdefSource	XdefSource		Same as XdefDrain for outer source area. Used for calculation of as and ps.
ad, as	Total Drain Area Total Source Area	m	<p>Values for source/drain area. Automatically computed unless 'user' is selected for XdefDrain/XdefSource.</p> <p>The values computed are based on the values of parameters w, n, gateSplitStripes, XdefDrain and XdefSource.</p> <p>Only editable if 'user' is selected for XdefDrain/XdefSource.</p>
stiStress	Change STI Stress Estimation?		Switch for changing the STI stress estimation values. Controls display of parameters sa, sb and sd.
sa, sb, sd	STI Compression (sa), STI Compression (sb), STI Compression (sd)	m	<p>STI compression values.</p> <p>sa, sb: Distance gate to RX edge for outer source/drain regions</p> <p>sd: Distance between gates.</p>

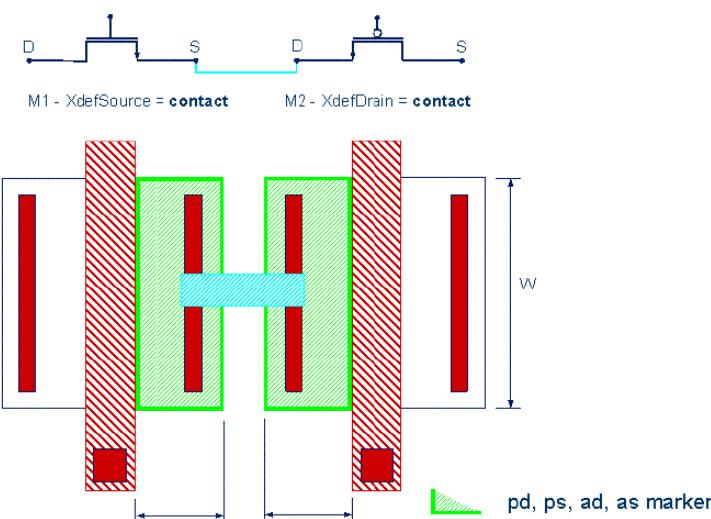




Parameter	Prompt	Unit	Description
dummyPoly	ACLV PC Fill		PCell parameter: Selects ACLV dummy PC generation in device layout: Values: none: no dummy PC Left: Dummy PC on left side Right: Dummy PC on right side Both: Dummy PC on left and right side
cnt	cnt		PCell parameter: Controls creation of contacts (CA) in outer source/drain regions of device layout.
cntBLR	cntBLR		PCell parameter: Controls creation of contacts (CA) in left and right source/drain region. Only displayed if cnt is selected. Values: Both: Create contacts on left and right side. Left: Create contacts just on left side. Right: Create contacts just on right side.
polyCnt	Poly Contact		PCell parameter: Enables gate contact to M1.
PolyRoute	PolyRoute		PCell parameter: Enables PC routing of gates for multi finger devices.
Pw	Poly Route Width	m	PCell parameter: Controls width of PC routing. Minimum PC width is ensured by PCell.
guardRing	Guard Ring		PCell parameter: Enables guard ring around device.
gr_stubs	Guard Ring Segments		PCell parameter: Selects guard ring segments around device
gr_stubs2	Second Guard Ring Segments		PCell parameter: Selects guard ring segments around device
M1Route	M1Route		PCell parameter: Enables M1 routing of source/drain regions for multi finger devices.
minRoute	minRoute		PCell parameter: Controls width of M1 routing. If selected, minimum M1 width is used. Otherwise, routing width is adjusted to width of source/drain M1.
distRoute	distRoute	m	PCell parameter: Controls distance of M1 routing to adjacent source/drain M1. PCell ensures minimum distance.
Sw	Source Width	m	PCell parameter: Controls width of M1 on source.
Dw	Drain Width	m	PCell parameter: Controls width of M1 on drain.
RecommendedRulesSelect	Select Rule Sets		PCell parameter: Open rule set selection browser (see section 3.4.1).
RecommendedRules	Rule Sets		PCell parameter: List of selected rule sets (see section 3.4.1).



Parameter	Prompt	Unit	Description
ngcon	Number of Gate Contacts		Switch for number of gate contacts. Valid values: 1, 2
plorient	plorient		Orientation of gate: 1: preferred orientation (gate width along x-axis) 2: non preferred orientation
par, psw_acv_sign, plnest, pdevdops, pdevlgeos, pdevwgeos, pld200, p_vta, cnr_switch, sca, scb, scc, u0_mult, pre_layout_local, p_la, lpccnr, covpccnr, wrxcnr			See Model Reference Guide for details.
m	Multiplicity		Number of parallel devices
SOA	Safe Operating Area		Check if the device conditions of use are in a safe mode

Table 10: MOSFET parameters**Figure 52: Definition XdefDrain/Source = contact (isolated contact geometry)**

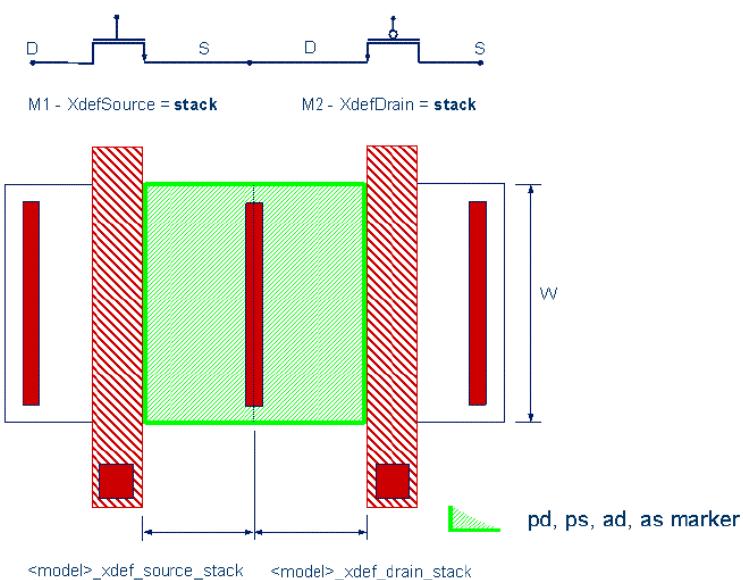


Figure 53: Definition XdefDrain/Source = stack (shared contact geometry)

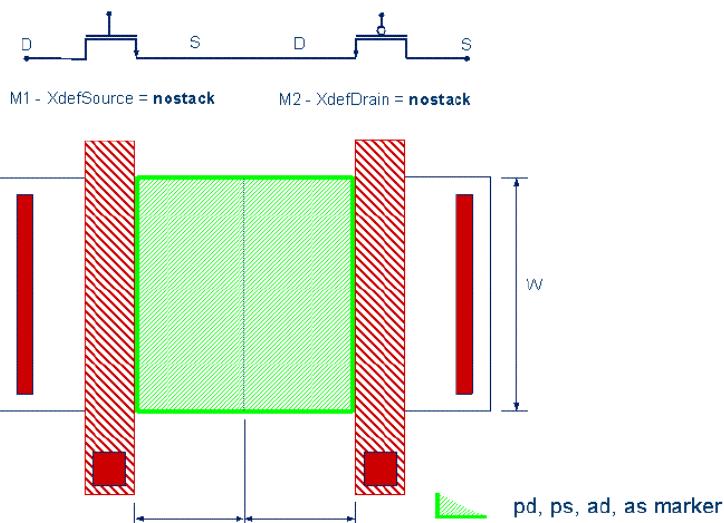


Figure 54: Definition XdefDrain/Source = noStack (merged contact geometry)

4.6.5 Netlist Formats

The 3 following paragraphs shows different netlist for a NFET whit default parameters.

4.6.5.1 Eldo

```
N (d g s b) <model> w= l= nf=<n>*<gateSplitStripes> \
ps= pd= ps= as= ad= sa= sb= sd= par= ptwell= \
plorient= pccrit= p_la= ngcon= soa= m= \
```





4.6.5.2 Hspice

```
x d g s b <model> w= l= nf= ps= pd= as= ad= sa= sb= sd= par= ptwell= plorient=
pccrit= p_la= ngcon= soa= m=
.END
```

4.6.5.3 CDL

```
M d g s b <model> m= w= l= n = nf=<n>*<gateSplitStripes> \
pccrit= plorient= ptwell= ngcon= p_la= soa=
```

4.6.6 Layout PCell

4.6.6.1 Rule Sets

Rule Set Name	Description
CA_ARRAY	Increases distance between CA to avoid CA array rule distance violations for instances with big width and high number of fingers.
CA_BOTTOM	Bottom alignment of CA on source and drain instead of centering.
CA_TOP	Top alignment of CA on source and drain instead of centering.
Compatible	
EXTENDED_NW_RING	Extends NW_RING to avoid spacing violations between substrate and isolated pwell.
MINIMUM_PC_PITCH	
MIN_M1	
NO_NPJUNCTION_OVER_CA	Avoids BP layer crossing CA of the gate contact.
NW_RING	When selected the T3 layer is drawn and extended to satisfy minimum width requirements and an NW ring is drawn around the T3 edges.
PCSTP4	Draws a marking layer PCSTP4 around each gate (valid for thin oxide fets)
PCSTP8	Draws a marking layer PCSTP8 around each gate (valid for thin oxide fets)
PITCH_130	Increases gate to gate spacing to 100n, when the gate length is less than 100n. It also sets dummy poly pitch to either 130n or 260n (not valid for 34nm gate length).
PITCH_252	Increases gate to gate spacing to 252n (not valid for 34nm gate length).
PITCH_260	Increases gate to gate spacing to 230n (not valid for 34nm gate length).
REMOVE_ONE_DIFF_CONT	
REMOVE_TWO_DIFF_CONTS	
RecommendedRules	
RedundantVias	Ensures that at least 2 CA are placed on source and drain.
MINIMUM_PC_PITCH	Changes the RX overlap over CA in order to place the ACLV PC fill on the closest available pitch.
T3	Creates triple well (T3) around device layout. This rule set is automatically added if the ptwell_select parameter is enabled.

Table 11: FET PCell rule sets





4.6.6.2 ROD Objects

Following named ROD objects will be created by the layout PCell if the 'rodObj' switch is enabled:

ROD Name	Object Type	Description
Grailpc	rectangle	PC rail connecting the gates of multi finger devices. Only defined if polyCnt is off and nf > 1.
Gpc.<number>	rectangle	Defined for each individual gate. <number> ranges from 1 to nf. Example: Gpc.1
Grailm1	rectangle	M1 rail connecting the gates of multi finger devices. Only defined if polyCnt is on and nf > 1.
Srailm1	rectangle	M1 rail connecting the source regions of multi finger devices. Only defined if M1Route is on and nf > 1.
Sm1.<number>	rectangle	Defined for each individual M1 rectangle on the source regions. <number> ranges from 1 to nf. Example: Sm1.1
Drailm1	rectangle	M1 rail connecting the drain regions of multi finger devices. Only defined if M1Route is on and nf > 1.
Dm1.<number>	rectangle	Defined for each individual M1 rectangle on the drain regions. <number> ranges from 1 to nf. Example: Dm1.1
rxRect.<number>	rectangle	Defined for each RX rectangle. <number> ranges from 1 to gateSplitStripes. Example: rxRect.1
nwRect	rectangle	NW enclosing a pfet or a nfet in triple well (PCell rule set N3).
n3Rect	rectangle	N3 enclosing nfet in triple well (PCell rule set N3).
bpRect	rectangle	BP enclosing pfet gate.
rvtRect	rectangle	RVT enclosing regular-vt pfet/nfet gate.
lvtRect	rectangle	LVT enclosing low-vt pfet/nfet gate.
slvtRect	rectangle	SLVT enclosing super low-vt pfet/nfet gate.
hvtRect	rectangle	HVT enclosing high-vt pfet/nfet gate.
egRect	rectangle	EG enclosing medium-oxide pfet/nfet gate.
egvRect	rectangle	EGV enclosing medium-oxide pfet/nfet gate.
zgRect	rectangle	ZG enclosing thick-oxide pfet/nfet gate.
zgvRect	rectangle	ZGV enclosing thick-oxide pfet/nfet gate.
overdriveRect	rectangle	OVERDRIVE enclosing thick-oxide pfet/nfet gate.
zvtRect	rectangle	ZVT enclosing zero-vt nfet gate.

Table 12: FET PCell ROD names



4.7 Resistors

4.7.1 Supported device types

Device	Name in DK	Comment
P+ OP Poly (p)	opppcres	With new silicium value
P+ OP Poly (p)	opppcres_b	With new silicium value
N+ OP Diffusion	opndres	
N+ OP Diffusion	opndres_b	
Nwell resistor	nwres	
Nwell resistor	nwres_b	
OP RE Polysilicon	opreres	With new silicium value
OP RE Polysilicon	opreres_b	With new silicium value

Table 13: Resistor device types and cells

4.7.2 Symbol



Terminal order: p n b



4.7.3 Inherited Connections

Resistor cells without an explicit bulk pin use following netExpression for the bulk pin:

Regular Devices	Bulk netExpression	Flipwell Devices	Bulk netExpression
Resistors	[@resbulk:%:VSS!]	Resistor	[@resbulk:%:VSS!]

4.7.4 Device Parameters

Parameter	Prompt	Unit	Description
description	Description		Show the model used in this device
dimensionMode	Dimension by Geometry		Switch: User can define value and either length or width or w and l of the device
r	Value	Ohm	Total nominal resistance. Dependent on dimensionMode switch the value can be entered by the user or is calculated from given w, l, ser and par.
w	Stripe width	m	Width of one resistor stripe, can also be calculated based on l and r if switch dimensionMode is set to off.
l	Stripe length	m	Length of one resistor stripe, can also be calculated from w and r if switch dimensionMode is set to off.
ser	Series stripes		Number of resistor stripes in series. Either ser or par may be > 1.
par	Parallel stripes		Number of resistor stripes in parallel. Either ser or par may be > 1.
d	Stripe Distance	m	Pcell parameter: Distance of parallel or serial resistor stripes in layout. Minimum distance is ensured by PCell.
resbulk	Bulk		NetSet property for connecting the bulk pin. Default value is [@lSup:%:VSS!]. Only available for cells without explicit bulk pin.
trise	Temperature deviation	°C	Deviation of device temperature from ambient.
subres	Substrate Resistance	Ohm	User defined substrate resistance. Use "0" for model default.
selfHeating	Self Heating		Enable self heating in simulation model.
bp_select	Backplane Designation		Only available for polysilicon resistors. Selects resistor backplane. Options: NW, PW, T3





bp	Backplane designation		Only available for polysilicon resistors. Set by bp_select. Values: 1: NW 3: PW 4: T3 (triple well)
guardRing	Guard Ring		PCell parameter: Enables guard ring around device.
dummies	Create Dummies		PCell parameter: Places left & right dummy stripes next to device.
routingWidth	Routing width		Pcell parameter: Specifies the width of M1 routing used for connection multiple stripes. Note: Too big M1 widths will cause distance error to M1 of guard ring because of width dependent distance design rules.
contactRows	contact Rows		Pcell parameter: Specifies the numbers of CA rows in the resistor pin. Note: For all values except "1" the resulting layout will deviate from the stripe end resistance assumptions made in the simulation model.
RecommendedRulesSelect	Select Rule Sets		PCell parameter: Open rule set selection browser (see section 3.4.1).
Rule Sets	Rule Sets		PCell parameter: List of selected rule sets (see section 3.4.1).
rodObj	Enable ROD Objects		
SOA	Safe Operating Area		Check if the device conditions of use are in a safe mode

Table 14: Resistor parameters

4.7.5 Netlist Formats

Parameter values are left out in the sample netlist lines below.

Parameter 'bp' is only listed for the opppcres and opreres device.

4.7.5.1 Eldo

```
x p n b <model> w= l= r= s= pbar= rsx= sh= bp= ncr= soa= m=
```

4.7.5.2 Hspice

```
x p n b <model> w= l= r= s= pbar= dtemp= rsx= sh= bp=
```

4.7.5.3 CDL

```
R p n $SUB=b ${<model>} m= r= w= l= pbar= s= bp= ncr= soa=
```





4.7.6 Layout PCell

4.7.6.1 Rule Sets

Rule Set Name	Description
T3	Draws a T3 layer around PC (only for opppcres)
NW_RING	Creates an NW ring around T3 shape (only for opppcres).
NW	Draws a NW layer around PC (only for opppcres)
RecommendedRules	

Table 15: Resistor PCell rule sets

4.7.6.2 ROD Objects

ROD Name	Object Type	Description
IN	rectangle	M1 on 'p' pin
OUT	rectangle	M1 on 'n' pin

Table 16: Resistor PCell ROD names



4.8 Capacitors

4.8.1 Supported device types

CAPACITORS			
Device	Name in DK	Flipwell	GPF
Bulk			
EG NCAP	egncap, egncap_b		x
EG PCAP	egpcap, egpcap_b		x
CMOM shielded with internal vias	cmom_6U1x_2U2x_2T8x_L_B_sh		x
CMOM 2 pins with internal vias	cmom_6U1x_2U2x_2T8x_L_B_2p		
CMOM shielded without internal vias	cmom_6U1x_2U2x_2T8x_L_B_wo_via_sh		x
CMOM 2 pins without internal vias	cmom_6U1x_2U2x_2T8x_L_B_wo_via_2p		

Table 17: Capacitor device types and cell names

4.8.2 Symbol

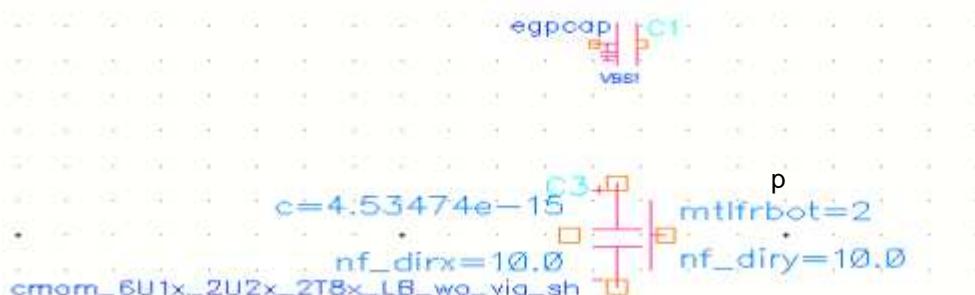


Figure 56: PCAP and CMOM symbol

Terminal order: PCAP: p n (b=inherited) / CMOM: minus plus psub shap

4.8.3 Inherited Connections

The ncap cell without an explicit bulk pin use following netExpression for the bulk pin:

[@capbulk:@:VSS!]



4.8.4 Device Parameters

Parameter	Prompt	Unit	Description
description	Description		Displays the model type of the device
dimensionMode	Dimension by Geometry		Switch: User can define value and either length or width or w and l of the device
value	value	F	Estimated nominal capacitance calculated from given w and l.
value_dep	value (depletion)	F	Estimated capacitance in depletion mode calculated from given w and l.
l	Gate Length	m	Length of the capacitor (polysilicon width).
w	Total Gate Width	m	Width of the capacitor (diffusion width).
nf	Number Of Gates		Number of gates per individual RX diffusion.
nrep	Number of RX Shapes		Number of individual RX diffusion shapes.
capbulk	Bulk		NetSet property for connecting the bulk pin. Default value is [@1 ^{Sup} :% :VSS!]. Only available for cells without explicit bulk pin.
trise	Device Temperature Deviation		Deviation of device temperature from ambient.
sizedup	Sized Up		
subres	Substrate Resistance	Ohm	Substrate/N-band resistance. Default is 50 Ohm.
setres	Resistance	Ohm	Resistance of M1 wiring. Use negative value to select model built-in estimation.
setind	Inductance	H	Inductance of M1 wiring. Use negative value to select model built-in estimation.
guardRing	Guard Ring		PCell parameter: Enables guard ring around device.
routing	M1 Routing?		Switch to enable horizontal M1 routing of source/drain and gate.
rails	M1 Rails?		Switch to enable M1 rails for p and n pins.
createPins	Create Pins w/o Routing?		
RecommendedRulesSelect	Select Rule Sets		PCell parameter: Open rule set selection browser (see section 3.4.1).
rodObj	Enable ROD Objects?		
m	Multiplicity		Number of devices in parallel
SOA	Safe Operating Area		Check if the condition of use are in safe area

Table 18: NCAP parameters





Parameter	Prompt	Unit	Description
c	Capacitance	(F)	Estimated nominal capacitance calculated from given w and l.
Fr_big_fingers	Fringes on big fingers		Switch: User can define value and either length or width or w and l of the device
nf_dirx	Fingers nb in X direction		
Nf_diry	Fingers nb in Y direction		
mtlfrbot	Bottom level metal		Indicates the lowest metal level of the device. Possible values of botlev are 1 through 6. Default 1 (M1).
mtlfrtop	Top level metal		Indicates the highest metal level of the device. Possible values are 1 to 6. toplev must be >= botlev.
mtlconbot	Metal Bottom Connexion		
mtlcontop	Metal top Connexion		
wfinger_mx	Width mx Finger	m	
Spacefinger_mx	Distance between 2 mx fingers	m	
mismatch	mismatch		
m	Nb of devices in //		
dc_mdev	Capacitor deviation		
Pre_layout_local	Post Layout extraction		
descriotion	Description		Short description of the device

Table 19: CMOM parameters

4.8.5 Netlist Formats

Parameter values are left out in the sample netlist lines below.





4.8.5.1 Eldo

- For PCAP:

```
xc p n b <model> w= l= nf= nrep= setres= setind= m= soa=
```

- For CMOM:

```
XC0 minus plus psub shap <model> nf_dirx= nf_diry= mtlfrbot= mtlfrtop= mtlconbot= mtlcontop= spacefinger_mx= wfinger_mx= mismatch= mult= pre_layout_local= dc_mdev= fr_big_finger= soa=
```

4.8.5.2 Hspice

- For PCAP

```
xc p n b <model> w= l= nf= nrep= setres= setind= m= soa=
```

- For CMOM

```
XC0 minus plus psub shap <model> nf_dirx= nf_diry= mtlfrbot= mtlfrtop= mtlconbot= mtlcontop= spacefinger_mx= wfinger_mx= mismatch= mult= pre_layout_local= dc_mdev= fr_big_finger= soa=
```

4.8.5.3 CDL

- For PCAP:

```
C p n <model> $SUB=b m= l= w= nf= nrep=
```

- For CMOM:

```
XC0 minus plus psub shap <model> nf_dirx= nf_diry= mtlfrbot= mtlfrtop= mtlconbot= mtlcontop= spacefinger_mx= wfinger_mx= fr_big_finger= soa=
```

4.8.6 Layout PCell

4.8.6.1 Rule Sets

No rule Set Defined for these devices

4.8.6.2 ROD Objects

ROD Name	Object Type	Description
sdTerm	rectangle	M1 rail connecting all gates (pin 'p').
gateTerm	rectangle	M1 rail connection all source/drain regions (pin 'n').
nwRect	rectangle	NW rectangle enclosing P- or N- capacitor

Table 20: Capacitor PCell ROD names





4.9 SRAM

4.9.1 Supported device types

SRAM			
Device	Name in DK	Flipwell	GPF
Bulk			
High Current Cell 0.152 PG NFET (SP0152LL / B152)	lshnfetwl_b	x	
High Current Cell 0.152 PD NFET (SP0152LL / B152)	lshnfetpd_b	x	
High Current Cell 0.152 PUPFET (SP0152LL / B152)	lshpfetpu_b	x	
Dense Cell 0.120 PG NFET (SP0120LL / D120)	dswnfetwl_b	x	
Dense Cell 0.120 PD NFET (SP0120LL / D120)	dswnfetpd_b	x	
Dense Cell 0.120 PU PFET (SP0120LL / D120)	dswpfetpu_b	x	
2-Port 0.251 Pass Gate NFET (TP251)	lslnfetwl_b	x	
2-Port 0.251 Pull Down NFET (TP251)	lslnfetpd_b	x	
2-Port 0.251 Pull Up PFET (TP251)	lslpfetpu_b	x	
2-Port 0.251 Regular-Vt NFET (TP251)	lslnfet_b	x	
High Performance Cell 0.152 PG NFET (SP0152HS / H152)	lsrnfetwl_b	x	
High Performance Cell 0.152 PD NFET (SP0152HS / H152)	lsrnfetpd_b	x	
High Performance Cell 0.152 PU PFET (SP0152HS / H152)	lsrpfetpu_b	x	
Dense Cell 0.197 PG NFET (SP0197LL/B197)	lsvnfetwl_b		
Dense Cell 0.197 PD NFET (SP0197LL/B197)	lsvnfetpd_b		
Dense Cell 0.197 PU PFET (SP0197LL/B197)	lsvpfpfetpu_b		



4.9.2 Symbol

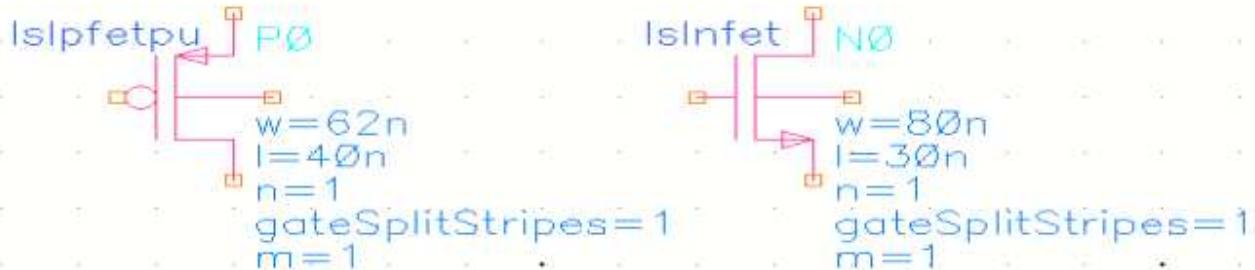


Figure 57: SRAM symbol

Terminal order: d g s b

4.9.3 Inherited Connections

No inherited connection on these devices.

4.9.4 Device Parameters

Parameter	Prompt	Unit	Description
description	Description		Gives the name of the model used for this device.
dimensionMode	Dimension Mode		Selects gate width dimension mode: TotalWidth: Enter total width, finger width is calculated FingerWidth: Enter finger width, total width is calculated
w	Total Gate Width	m	Total gate width. Editable if Dimension Mode is TotalWidth.
wf	Gate Finger Width	m	Gate finger width. Editable if Dimension Mode is FingerWidth.
l	Gate Length	m	Gate length
n	number of gate fingers		Number of gate fingers. Finger width is w/n . This parameter must be set to an integer ≥ 1 for correct calculation of ad, as, pd and ps values. It cannot be parameterized using design variables or pPar expressions.



Parameter	Prompt	Unit	Description
gateSplitStripes	Gate Split Y		Number of gate splits in Y-direction. Produces individual RX shapes in device layout. Influences pd and ps calculation.
pccrit	pccrit		Internal parameter for ACLV parameter selection. Controlled by pccrit_select; used for netlisting. Value: 0: Aclv parameters set to non-critical values
ptwell			Internal parameter for local well proximity switch. Controlled by wellSelect switch; used for netlisting. Values: 0: dual well proximity model 1: triple well proximity model
XdefDrain	XdefDrain		Specifies layout configuration of outer drain area for ad and pd calculation: Values: contact: No butting to other source/drain region (see Figure 52). stack: Drain will be abutted to another source/drain keeping contacts (see Figure 53). noStack: Drain will be abutted to another source/drain, no contacts are kept (see Figure 54). user: User have to specify ad and pd values explicitly
XdefSource	XdefSource		Same as XdefDrain for outer source area. Used for calculation of as and ps.
ad, as, pd, ps	Total Drain Area, Total Source Area, Drain Periphery, Source Periphery	m	Values for source/drain area, perimeter. Automatically calculated unless 'user' is selected for XdefDrain/XdefSource. The values are calculated based on the values of parameters w, n, gateSplitStripes, XdefDrain and XdefSource. Only editable if 'user' is selected for XdefDrain/XdefSource.
stiStress	Change STI Stress Estimation?		Switch for changing the STI stress estimation values. Controls display of parameters sa, sb and sd.
sa, sb, sd	STI Compression (sa), STI Compression (sb), STI Compression (sd)	m	STI compression values. sa, sb: Distance gate to RX edge for outer source/drain regions sd: Distance between gates.
trise	Temperature Deviation	°C	Deviation of device temperature from ambient.





Parameter	Prompt	Unit	Description
plorient	plorient		Orientation of gate: 1: preferred orientation (gate width along x-axis) 2: non preferred orientation
par, psw_acv_sign, plnest, pdevdops, pdevlgeos, pdevwgeos, pld200, p_vta, cnr_switch, sca, scb, scc, u0_mult, pre_layout_local, p_la, lpccnr, covpccnr, wrxcnr			See Model Reference Guide for details.
m	Multiplicity		Number of parallel devices

Table 21: SRAM parameters

4.9.5 Netlist Formats

Parameter values are left out in the sample netlist lines below.

4.9.5.1 Eldo

```
XN d g s b <model> w= l= nf= ps= pd= as= ad= par= ptwell= plorient=
pccrit= p_la= ngcon= m=
```

4.9.5.2 Hspice

```
xn d g s b <model> w= l= nf= ps= pd= as= ad= par= ptwell= plorient= pccrit=
p_la= ngcon= m=
```

4.9.5.3 CDL

```
MN d g s b <model> m= w= l= nf= pccrit= plorient= ngcon= p_la= ptwell=
```

4.9.6 Layout PCell Rule Sets

No layout for this type of device.



4.10 Diodes

4.10.1 Supported device types

DIODES			
Device	Name in DK	Flipwell	GPF
			Bulk
N+ to Substrate Junction Diode	diodenx		x
P+ Diffusion to Nwell Junction Diode	diodepnw		x
EG N+ to Substrate Junction Diode	egdiodenx		x
EG P+ Diffusion to Nwell Junction Diode	egdiodepnw		x
Nwell to Substrate Junction Diode	diodenwx		x
Nband to Substrate Junction Diode	diodetwx		x
Nband to Pwell Junction Diode	diodepwtw		x
N+ Floating Gate Tie-Down	tdndsx		x
P+ Floating Gate Tie-Down	tdpdnw		x
EG N+ Floating Gate Tie-Down	egtdndsx		x
EG P+ Floating Gate Tie-Down	egtdpdnw		x
Nwell to Substrate Junction Diode (negative bias)	diodenwx_lvs		x
Nband to Substrate Junction Diode (negative bias)	diodetwx_lvs		x
Nband to Pwell Junction Diode (negative bias)	diodepwtw_lvs		x

4.10.2 Symbol



Figure 58: Diode symbol

Terminal order: p n



4.10.3 Device Parameters

Parameter	Prompt	Unit	Description
Description	Description		Short description of the device
area	Area	m ²	Area of the diode. Automatically calculated if w or l is modified.
perimeter	Perimeter	m	Perimeter of the diode. Automatically calculated if w or l is modified.
trise	Device Temperature Deviation	°C	Deviation of device temperature from ambient
Sized Up	Sized Up		
width	Width (optional: only for tieDown diode & Recatngular shape actived)	m	PCell parameter: Width of diode
height	Height (optional: only for tieDown diode & Recatngular shape actived)	m	PCell parameter: Height of diode
RecommendedRulesSelect	Select Rule Sets		PCell parameter: Open rule set selection browser (see section 3.4.1).
RecommendedRules	Rule Sets		PCell parameter: List of selected rule sets (see section 3.4.1).
SOA	Safe Operating Area		Check if the device conditions of use are in a safe mode
m	Multiplicity		Number of parallel devices

Table 22: Diode parameters

4.10.4 Netlist Formats

Parameter values are left out in the sample netlist lines below.

4.10.4.1 Eldo

```
XD p n <model> area= perim= soa= m=
```

4.10.4.2 Hspice

```
xd p n <model> area= perim= soa= m=
```

4.10.4.3 CDL

```
dd p n <model> area= perim= soa= m=
```





4.10.5 Layout PCell Rule Sets

Only following cell have layout views: egtdndsx/egtdpdnw/tdndsx/tdpdnw

Rule Set Name	Description
RecommendedRules	Changes BFMOAT generation to fulfill GR IND07bR.
COINCIDENT_LAYERS	
NW	
RecommendedRules	
RedundantVias	Ensures that at least 2 CA are placed on source and drain

Table 23: Inductor PCell rule sets



4.11 BIPOLAR

As this technology is a full mosfet techno, we provide only one bipolar in order to provide a supply. This supply is a bandgap reference.

4.11.1 Supported device types

BIPOLAR					
Device	Name in DK	Flipwell	GPF	Bulk	Comment
VPNP	vppn		x		Bandgap reference

Table 24: VPPN

4.11.2 Symbol

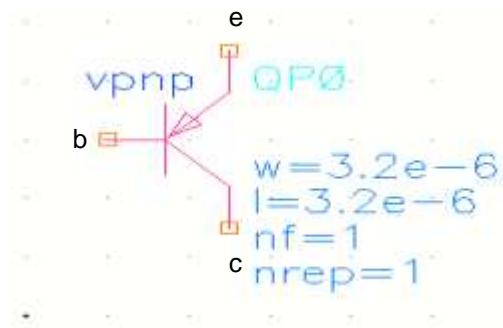


Figure 59: VPPN diode symbol

Terminal order: c b e

4.11.3 Device Parameters

Parameter	Prompt	Unit	Description
w	w	m	Emitter design width.
l	l	m	Emitter design length.
nf	Number of Emitters		Number of emitter fingers, currently fixed to 1.
nrep	Repetition		Number of fingers along length of device. Ignored if set to 0. Currently fixed to 0.
trise	Device Temperature	°C	Deviation of device temperature from ambient



Parameter	Prompt	Unit	Description
	Deviation		
RecommendedRulesSelect	Select Rule Sets		PCell parameter: Open rule set selection browser (see section 3.4.1).
RecommendedRules	Rule Sets		PCell parameter: List of selected rule sets (see section 3.4.1).
SOA	Safe Operating Area		Check if the device conditions of use are in a safe mode

Table 25: VPPNP diode parameters

4.11.4 Netlist Formats

Parameter values are left out in the sample netlist lines below.

4.11.4.1 Eldo

```
XQP c b e <model> nf= nrep= w= l= soa=
```

4.11.4.2 Hspice

```
xqp c b e <model> nf= nrep= w= l= soa=
```

4.11.4.3 CDL

```
QQP c b e <model> nf= nrep= w= l= soa=
```

4.11.5 Layout PCell Rule Sets

Only “RecommendedRules” is available for this device.





4.12 ESD

ESD FET devices are provided as non-primitive symbols and layout PCells. The symbol has an underlying schematic, which contains instances of resistors, FET and ESD shell devices, modeling the complete ESD FET behavior.

ESD FET device offer 3 variants of source/drain area silicide blocking (source and drain blocked, only source blocked, only drain blocked) by providing separate symbols for each variant, and offer to silicide block the gate for source and drain blocked variant controlled by a parameter.

4.12.1 Supported device types

ESD				
Device	Name in DK	Flipwell	GPF	Bulk
P+/NW Diode/Vetical PNP Bipolar	esdvnpn			x
N+/PW Diode (DW) (ESD N+ Junction)	esdndsx			x
N+/PW Diode/Vertical NPN Bipolar (TW)	esdvnpn			x
Poly bounded DW P+/NW ESD Diode - EG version	esdvnpn_eg			x
Poly bounded DW N+/PW ESD Diode - EG version	esdndsx_eg			x
Poly bounded TW N+/PW ESD Diode - EG version	esdvnpn_eg			x
Silicide-Block N-Diffusion Resistor	sblkndres_fdsoi	x	x	
ESD SBLK NFET	esdnfet			x
EG ESD SBLK NFET	esdegnfet			x



4.12.2 Symbol

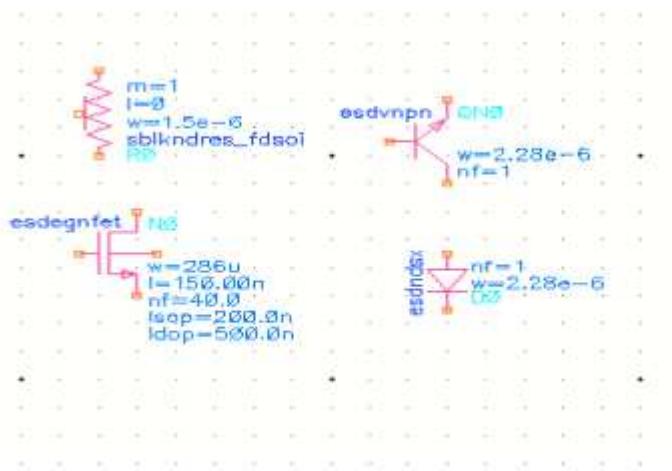


Figure 60: Different ESD symbols

Terminal order: refer to the corresponding device (e.g. for esdvpnp see § on vpnp)

4.13 ESD Hierarchical Cells

These devices are special ESD devices. They are composed of a mosfet protected by 2 resistors: sblkndres:

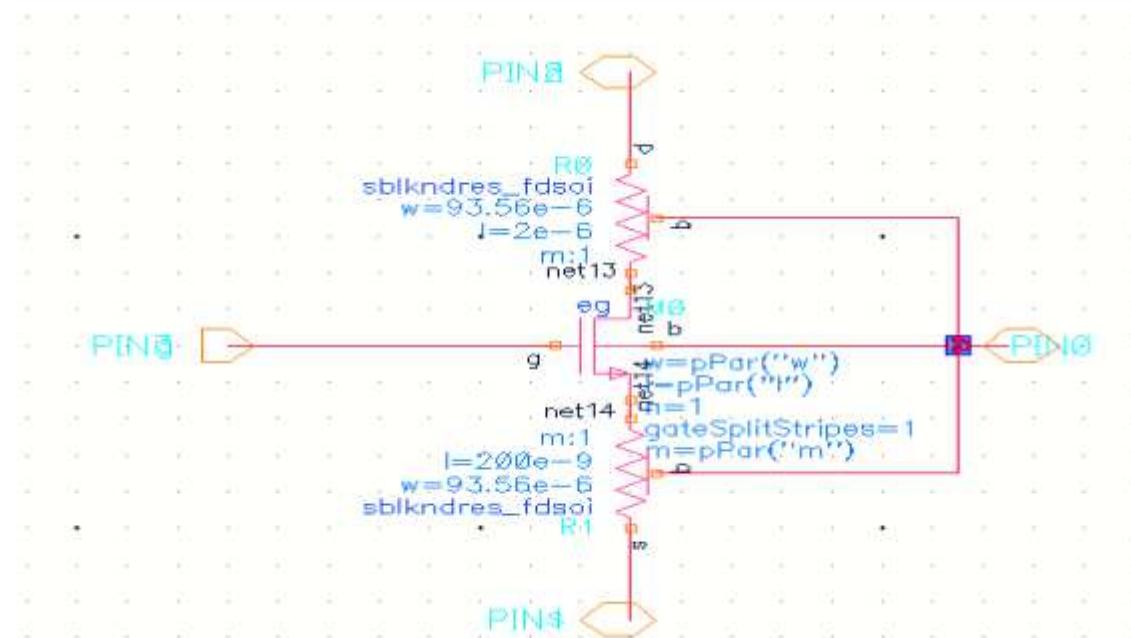


Figure 61: Schematic of a hierarchical device

This type of devices are composed of a symbol and a schematic only, the simulator views which are used to simulate a such devices are the views of the mosfet with its resistors.

4.13.1 Supported device types

ESD Hierarchical					
Device	Name in DK	Flipwell	GPF	Bulk	Comment
Silicide-Block Nfet	esdnfet_fds01	x			ESD application; Models nfet + sblkndres_fds01
Silicide-Block Low Vt Nfet	esdlvtnfet_fds01	x			ESD application; Models lvtnfet + sblkndres_fds01
Silicide-Block Nfet 28A	esdegnfet_fds01		x		ESD application; Models egnfet + sblkndres_fds01
Silicide-Block Low Vt Nfet 28A	esdegltvnfet_fds01	x			ESD application;

Models eglvtnfet +
sblkndres_fdsOI

4.13.2 Symbol

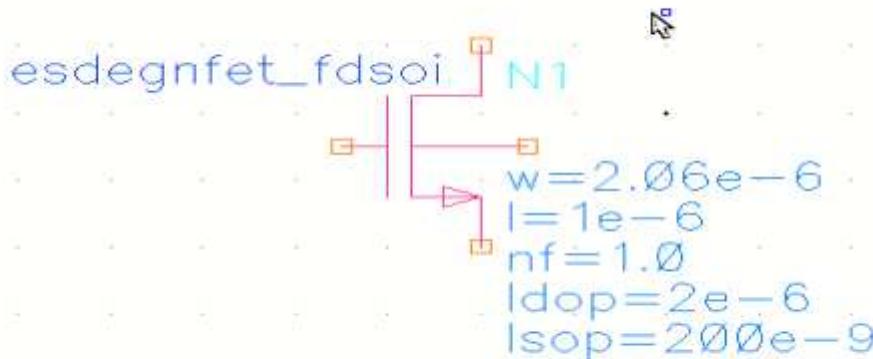


Figure 62: ESD Hierarchical symbol

Terminal order: b d g s

4.13.3 Device Parameters

Parameter	Prompt	Unit	Description
description	Description		Gives the name of the model used for this device.
dimensionMode	Dimension Mode		Selects gate width dimension mode: TotalWidth: Enter total width, finger width is calculated FingerWidth: Enter finger width, total width is calculated
w	Gate Width	m	Total gate width
l	Gate Length	m	Gate length
nf	Total Number of Fingers		Number of fingers used for netlisting. Currently fixed to 1.
n	Number of Fingers		Number of gate fingers on single diffusion shape, i.e. repetition in x-direction. Used by layout PCCell only. For each gate finger a separate symbol instances must be created in the schematic.



Parameter	Prompt	Unit	Description
gateSplitStripes	RX Repetition		Number of diffusion shapes, i.e. repetition in y-direction. Used by layout PCell only. For each gate finger a separate symbol instances must be created in the schematic.
gns	Silicide Blocked Gate		Controls silicide blocking of gate: 0: no SBLK over gate, gate will be silicided 1: gate 1 silicided, gate 2 non silicided 2: gate 1 not silicided, gate 2 silicided 3: both gates not silicided The PCell currently support only modes 0 and 3. Modes 1 and 1 will be treated like mode 3.
lsop	Source SBLK length	m	Length of silicide blocked region on source side. Only available for device variant with blocked source.
ldop	Drain SBLK length	m	Length of silicide blocked region on drain side. Only available for device variant with blocked drain.
guardRing	Guard Ring		PCell parameter: Enables guard ring around device. <ul style="list-style-type: none"> • none • one: diode ring connected to drain • two: substrate/well contact connected to source • three: substrate/well contact not connected to any FET terminal
trise	Temperature Deviation		Deviation of device temperature from ambient. Passed to underlying FET model and resistor models.
XdefDrain	XdefDrain		Specifies layout configuration of outer drain area for ad and pd calculation: Values: contact: No butting to other source/drain region (see Figure 52). stack: Drain will be abutted to another source/drain keeping contacts (see Figure 53). noStack: Drain will be abutted to another source/drain, no contacts are kept (see Figure 54). user: User have to specify ad and pd values explicitly
XdefSource	XdefSource		Same as XdefDrain for outer source area. Used for calculation of as and ps.





Parameter	Prompt	Unit	Description
ad, as, pd, ps	Total Drain Area, Total Source Area, Drain Periphery, Source Periphery	m	Values for source/drain area, perimeter. Automatically calculated unless 'user' is selected for XdefDrain/XdefSource. The values are calculated based on the values of parameters w, n, gateSplitStripes, XdefDrain and XdefSource. Only editable if 'user' is selected for XdefDrain/XdefSource.
stiStress	Change STI Stress Estimation?		Switch for changing the STI stress estimation values. Controls display of parameters sa, sb and sd.
plorient	plorient		Orientation of gate: 1: preferred orientation (gate width along x-axis) 2: non preferred orientation
RecommendedRules	Rule Sets		PCell parameter: List of selected rule sets.
ngcon	Number of Gate Contacts		Switch for number of gate contacts.
SOA	Safe Operating Area		Check if the device conditions of use are in a safe mode

Table 26: ESD Hierarchical parameters

4.13.4 Netlist Formats

For the following example, we put colors on the different part of the netlist as it is a hierarchical devices, all devices under the symbols are netlisted.

4.13.4.1 Eldo

```
.SUBCKT ESDEGNFET_FDSOI B D G S PARAM: W6u LDOP=2u LSOP=200.0n L=1u
+PS=0 PD=0 AS=0 AD=0 SA={(200.0n)+(290.00n)} SB={(2u)+(290.00n)} SD=0
+TRISE=0 NGCON=2

    XR0 D NET13 B sblkndres_fdsoi w=W l=LDOP s=1 pbar=1 sh=1 soa=1 m=1
    XR1 S NET14 B sblkndres_fdsoi w=W l=LSOP s=1 pbar=1 sh=1 soa=1 m=1
    XM0 NET13 G NET14 B egnfet w=W l=L nf={(1)*(1)} ps=PS pd=PD as=AS
    +ad=AD sa=SA sb=SB sd=SD par=1 dtemp=TRISE ptwell=0 plorient=1 pccrit=0
    +p_la=0 ngcon=NGCON soa=1 m=M
.ENDS
```





4.13.4.2 Hspice

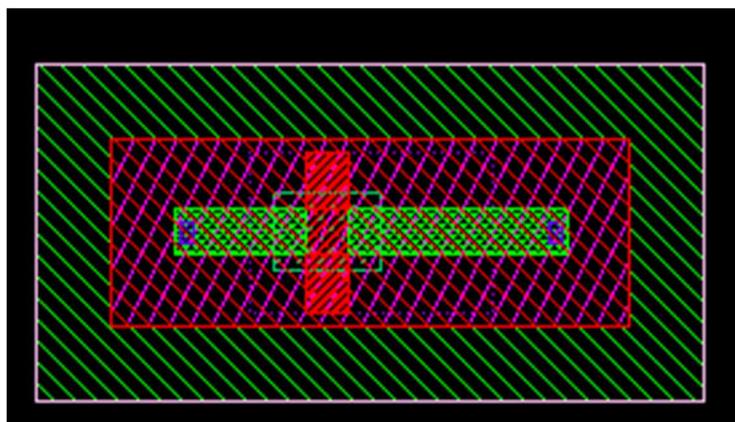
```
.subckt esdegnfet_fdsoi b d g s
xr0 d net13 b sblkndres_fdsoi w=w l=ldop s=1 pbar=1 sh=1 soa=1 m=1
xr1 s net14 b sblkndres_fdsoi w=w l=lsop s=1 pbar=1 sh=1 soa=1 m=1
xm0 net13 g net14 b egnfet w=w l=l nf=1 ps=ps pd=pd as=as ad=ad sa=sa sb=sb
sd=sd par=1 dtemp=trise ptwell=0 plorient=1 pccrit=0 p_la=0 ngcon=ngcon soa=1
m=m
.ends esdegnfet_fdsoi

xn0 net4 net1 net2 net3 esdegnfet_fdsoi w=93.56e-6 ldop=2e-6 lsop=200e-9 l=le-6
ps=188.1e-6 pd=4.00037882 as=45.8444e-12 ad=187.1202142524e-6 sa=490e-9
sb=2.29e-6 sd=0 trise=0 ngcon=5
```

4.13.4.3 CDL

```
.SUBCKT esdegnfet_fdsoi b d g s
*.PININFO g:I b:B d:B s:B
RR0 d net13 $SUB=b $[sblkndres_fdsoi] m=1 w=w l=ldop pbar=1 s=1 soa=1
RR1 s net14 $SUB=b $[sblkndres_fdsoi] m=1 w=w l=lsop pbar=1 s=1 soa=1
MM0 net13 g net14 b egnfet m=m w=w l=l nf=1.0 pccrit=0 plorient=1 ngcon=ngcon
+ p_la=0 ptwell=0 soa=1
.ENDS
```

4.13.5 Layout view





5 ST_C32_addon_DP

This library has been defined to permit and make easier migration between 28lp and 28FDSOI design but also to begin 28FDSOI design directly (some PCELL have been updated for Example)

5.1 Main purpose/content

>28FDSOI Devices list

- CMOM with and without via sh/2p
- DriftOTP NMOS
- SRAM 10T transistors (only symbols)
- OTP capacitance (nfeftotp)
- ST sealring: the version in this Design Kit, is not the final one. A PCELL update is necessary.

>Some FDSOI specificities have been implemented (compared to Addon 28lp DP)

- The CMOM sh has to be considered as an hybrid devices (on bulk area)
 - Layout/PCELL has been updated to add specific layers
- Same as CMOM situation, the PCELL of the Nmos Drift OTP device has been updated
- In the Release, the Sealring PCELL will be updated to add FDSOI MKR (no size update)

5.2 Devices List in ST_C32_addon_DP

Device	Description
Sealring 28FDSOI device	sealring_6U1x_2U2x_2T8x (new PCELL to add FDSOI layer)
STLogo	Logo for the layout finishing: pcell only, drawn in IB, year as a parameter
OTP capacitance 28FDSOI device	Nfetotp/ Nfetotp_fw (symbol only – like 28lp)
CMOM (except shield) 28FDSOI device	cmom_6U1x_2U2x_2T8x_LB_2p/cmom_6U1x_2U2x_2T8x_LB_wo_via_2p
CMOM Shield Hybrid devices	cmom_6U1x_2U2x_2T8x_LB_wo_via_sh/cmom_6U1x_2U2x_2T8x_LB_wo_via_sh (new PCELL to add specific Hybrid MKR)
Ndriftotp	ndriftotp





Hybrid devices	(new PCELL to add FDSOI specific Hybrid MKR)
Egpcap(_b)	PCAP Capacitor (new pcell,symbol/cb aligned on EGNCAP)
NW GO2 RF Varactor	cvar_eg (single with 3 pins) cvar_eg_diff (Diff with 4 pins)
NW G02 Attofarrad	cvar_eg_atto

Table 27: DeviceS OF ST_C32_addon_DP

Devices	FDSOI	Bulk/Hybrid
CMOM	✓	✓(for Shield CMOM only)
SRAM devices LVT	✓	
OTP Capacitance	✓	
NdriftOTP		✓
EGPCAP		✓

Table 28: Structure of the devices

For complete information about these devices and their structures, you can see the release note.

5.3 Sealring 10M

The purpose of this ST seal ring is to give information for achieving a moisture resistant die, without the possibility that cracks generated in the scribe lane during the saw can propagate into the die.

Check	Description
Device name(s)	sealring_6U1x_2U2x_2T8x_LB
Models	No model associated to this device (only PCELL/DRC/PLS)

Table 29: Sealring definition



The sealring layout is described below:

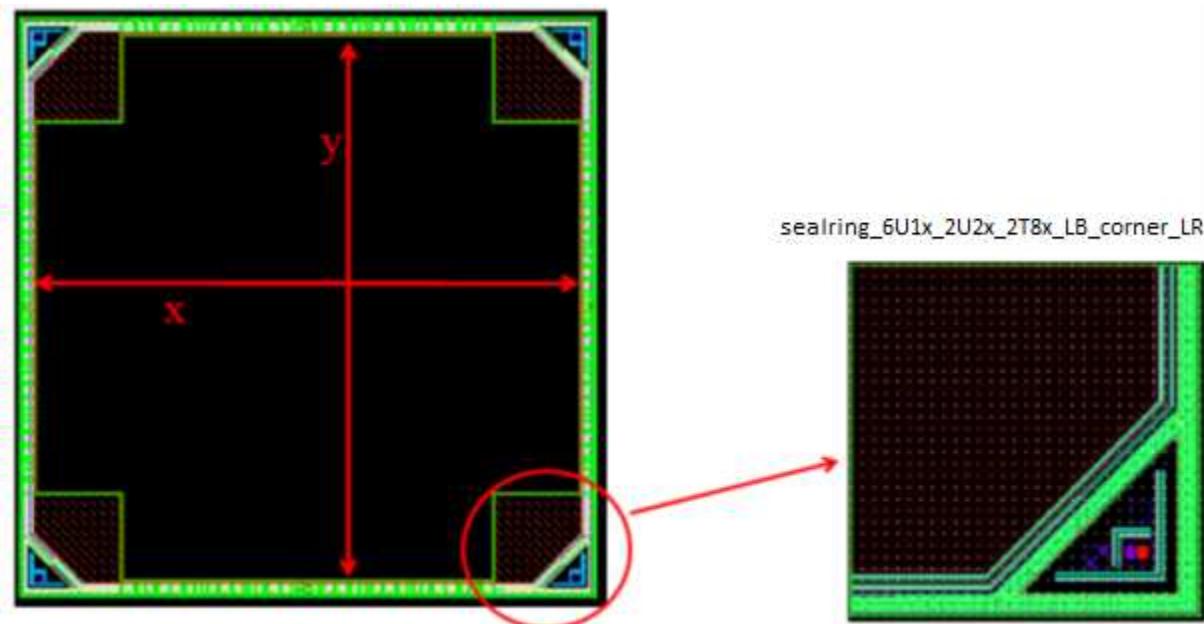


Figure 63: layout view sealring 10M

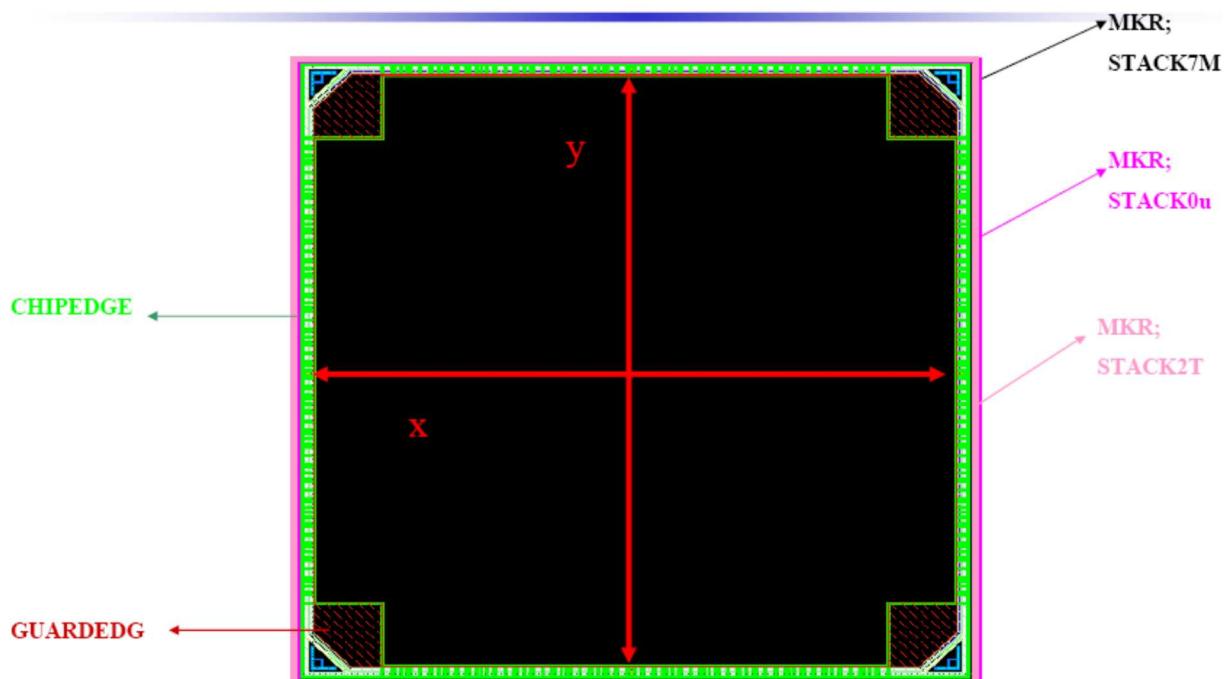


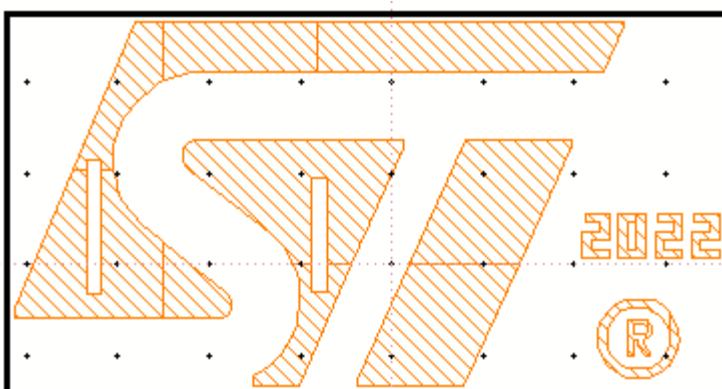
Figure 64: layers in sealring

5.3.1 CDF parameter description:

Parameter	Prompt	Unit	Description
descripiton	Description		Gives the name of the model used for this device.
x	Chip Width (m)	m	Width of the sealring, limited to the minimum value of 320um but no max value is set
y	Chip Length (m)	m	Length of the sealring, limited to the minimum value of 320um but no max value is set

5.4 STLogo

ST provides a pcell to create the STLogo for ST chip. The year is customizable. The layout generated is as follow:



5.5 CMOM device 10M (6U1x_2U2x_2T8X)

The CMOM capacitor is a free device (no extra masks) made with thin copper metal levels and inter-metal dielectric levels, optimized for analog/RF designs as well as for density.

The CMOM capacitance 6U1x_2U2x_2T8x_LB is defined from M1 to M5 level (the 10ML capacitance definition is under study). The monometal configuration is forbidden.

Four different devices are proposed for the CMOM:

- **With VIA and with shield (4 pins - plus, minus, shap, psub - cmom_6U1x_2U2x_2T8x_sh):** The shield is made of parallel RX and PC stripes on STI, in either X or Y direction and connected in M1 by a bus on both sides.



• **With VIA and stacked with (underneath) devices (2 pins - plus, minus cmom_6U1x_2U2x_2T8x_2p):** This device can be stacked on top of other devices, so that no parasitic is accounted for in the model. Therefore, the parasitic must be extracted by the user. In this case, a specific CMOMST;twopins marker must cover the CMOM (on top of CMOMST;mkr). All layers up to the metal just below the bottom metal used by the unit capacitor can be freely drawn. RX and PC dummies should be generated in a regular way

• **Without VIA and with shield (4 pins - plus, minus, shap, psub - cmom_6U1x_2U2x_2T8x_wo_via_sh):** The shield is made of parallel RX and PC stripes on STI, in either X or Y direction and connected in M1 by a bus on both sides.

• **Without VIA and stacked with (underneath) devices (2 pins - plus, minus cmom_6U1x_2U2x_2T8x_wo_via_2p):** This device can be stacked on top of other devices, so that no parasitic is accounted for in the model. Therefore, the parasitic must be extracted by the user. In this case, a specific CMOMST;twopins marker must cover the CMOM (on top of CMOMST;mkr). All layers up to the metal just below the bottom metal used by the unit capacitor can be freely drawn. RX and PC dummies should be generated in a regular way

Then, for each device, the CMOM capacitor is having several options (available in the pcell) and details in models documentation and Design Rule Manual.

Device name	cmom_6U1x_2U2x_2T8x_LB_2p, cmom_6U1x_2U2x_2T8x_LB_2p_acc
Pins	Plus minus

Device name	cmom_6U1x_2U2x_2T8x_LB_sh, cmom_6U1x_2U2x_2T8x_LB_sh_acc
Pins	plus minus psub shap

Device name	cmom_6U1x_2U2x_2T8x_LB_wo_via_2p, cmom_6U1x_2U2x_2T8x_LB_wo_via_2p_acc
Pins	Plus minus

Device name	cmom_6U1x_2U2x_2T8x_LB_wo_via_sh, cmom_6U1x_2U2x_2T8x_LB_wo_via_sh_acc
Pins	plus minus psub shap

→ Pins configurations

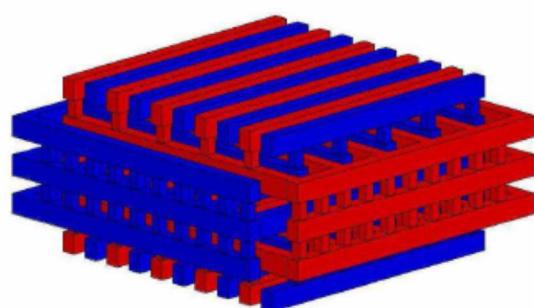
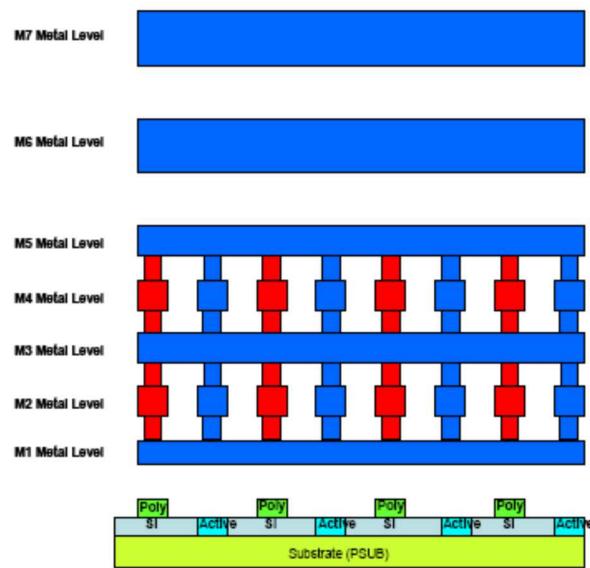
MOM capacitor is symmetrical. Pin number depends of topology:

· 2 pins for cmom_6U1x_2U2x_2T8x_LB_2p and cmom_6U1x_2U2x_2T8x_LB_wo_via_2p: *plus, minus*.



- 4 pins for cmom_6U1x_2U2x_2T8x_LB_sh and cmom_6U1x_2U2x_2T8x_LB_wo_via_sh: *plus*, *minus*, one pin for Poly/Active shield *shap*, one pin for substrate *psub*.

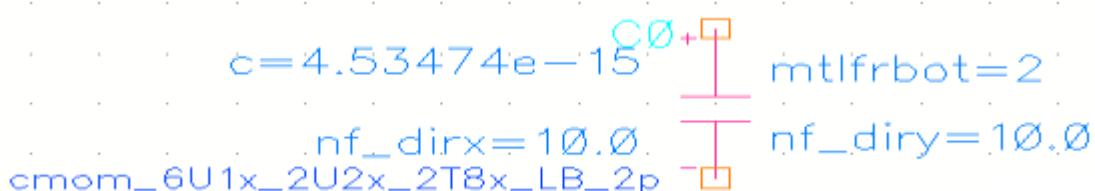
→ Cross section and 3D view



3D view of MOM capacitor
(M1 to M5 finger layers with M2 to
M4 connection layers)

Cross section of MOM capacitor
(Shield + M1 to M7 layers)

5.5.1 Symbol used:





5.5.2 Netlist:

→Eldo

```
XC0 NET7 NET8 cmon_6U1x_2U2x_2T8x_LB_2p nf_dirx=10.0 nf_diry=10.0
+mtlfrbot=2 mtlfrtop=5 mtlconbot=2 mtlcontop=4 spacefinger_mx=0.10e-6
+wfinger_mx=0.10e-6 mismatch=1 mult=1 pre_layout_local=-1 dc_mdev=0
+fr_big_finger=0 soa=1
```

→HSPICE

```
xc0 net7 net8 cmon_6U1x_2U2x_2T8x_LB_2p nf_dirx=10 nf_diry=10 mtlfrbot=2 mtlfrtop=5 mtlconbot=2
mtlcontop=4 spacefinger_mx=100e-9 wfinger_mx=100e-9 mismatch=1 mult=1 pre_layout_local=-1
dc_mdev=0 fr_big_finger=0 soa=1
```

→Spectre

```
C0 (net1 net2) cmon_6U1x_2U2x_2T8x_LB_2p nf_dirx=10.0 nf_diry=10.0 mtlfrbot=2 mtlfrtop=5
mtlconbot=2 mtlcontop=4 spacefinger_mx=1e-07 wfinger_mx=1e-07 mismatch=1 mult=1 pre_layout_local=-1
dc_mdev=0 fr_big_finger=0 soa=1
```

→CDL

```
XC0 net7 net8 cmon_6U1x_2U2x_2T8x_LB_2p nf_dirx=10.0 nf_diry=10.0 mtlfrbot=2
+ mtlfrtop=5 mtlconbot=2 mtlcontop=4 spacefinger_mx=0.10e-6 wfinger_mx=0.10e-6
+ fr_big_finger=0
```

5.5.3 CDF parameters description

Parameter	Prompt	Description
c	Capacitance (F)	Give value of the capa depending on the others parameters
Fr_big_finger	fringes on big fingers	
Nf_dirx	Fingers nb in X direction	Number of fingers on the horizontal plan
Nf_diry	Fingers nb in Y direction	Number of fingers on the vertical plan
m	Number of device in parallel	When m>1, the instance generated is put in parallel with himself "m" times. The layout will be automatically generated with m devices in parallel.
mtlfrbot	Bottom level metal	The lower metal used in this matrix capacitor





Parameter	Prompt	Description
mtlfrtop	Top level metal	The top metal used in this matrix capacitor, must be superior to "mtlfrbot". All metals between "mtlfrbot" and "mtlfrtop" are used in the capacitor
mtlconbot	Metal bottom connection	Metal used to provide the connection to the device on the bottom, should be between mtlfrbot and mtlcontop
mtlcontop	Metal Top Connexion	Metal used to provide the connection to the device on the top level, should be between mtlfrbot and mtlcontop
wfinger_mx	Width mx Finger (M)	Width of the finger used
spacefinger_mx	Distance Between 2 Mx fingers (M)	Space between fingers
mismatch	mismatch	Boolean which gives the information to models to take into account mismatch or not
dc_mdev	Capacitor deviation	Will disappear in 2.5
pre_layout_local	Post Layout extraction	Activate the default parasite in model
description	Description	Description of the device
soa	Safe Operating Area	Check that the device is correctly used, during the simulation if this option is set, warning are displayed in case of misusage.

5.6 NDriftOTP

This service is based on egndrift with some variation:

- L upsized (0.166um instead of 0.15um)
- Pwell block width allowed at 1.45um vs 1.5um (relaxed reliability constraint 6V 1')

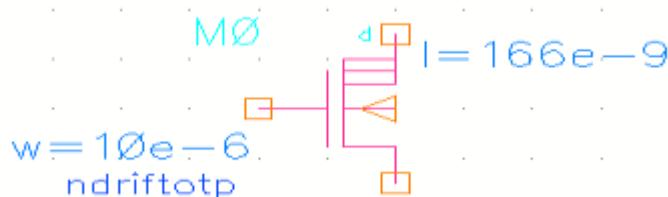
Check	Description
Device name(s)	ndriftotp
model codes	PSP102.2
pin	d g s b
default instantiation mode	geometric



Spice parameters	w, l, mult, sidenum, ngcon, t, trise, mismatch, dvt_mdev dmu_mdev, pre_layout_local
Extracted parameters	w, l, mult, sidenum, ngcon, t, trise, dvt_mdev dmu_mdev, pre_layout_local
LVS Compared parameters	W, l, sidenum, ngcon, mult
DiR	No DiR
Pre_layout switch (LPE/pre_layout_local)	
Corners list	TT, STSSA, STFFA, STSFA, STFSA, USER, statmotherfab, statmultifab,

Table 30: ndrifotp definition

5.6.1 Symbol used:

**Figure 65: ndrifotp symbol**

5.6.2 Netlist

→Eldo

```
XM0 NET4 NET1 NET2 NET3 ndrifotp w=10e-06 l=0.166e-06 mult=1 sidenum=1  
+ngcon=1 t=-274 trise=0 mismatch=1 pre_layout_local=-1 nsig_vto=0  
+nsig_uo=0 nsig_dibl=0 nsig_lvaro=0 nsig_wvaro=0 soa=1
```

→Hspice

```
xm0 net4 net1 net2 net3 ndrifotp w=10e-6 l=166e-9 mult=1 sidenum=1 ngcon=1 t=-274 trise=0 mismatch=1  
pre_layout_local=-1 nsig_vto=0 nsig_uo=0 nsig_dibl=0 nsig_lvaro=0 nsig_wvaro=0 soa=1
```

→Spectre



M0 (net4 net1 net2 net3) ndriftotp w=10e-06 l=0.166e-06 mult=1 sidenum=1 ngcon=1 t=-274 trise=0 mismatch=1 pre_layout_local=-1 nsig_vto=0 nsig_uo=0 nsig_dibl=0 nsig_lvaro=0 nsig_wvaro=0 soa=1

→CDL

MM0 net4 net1 net2 net3 ndriftotp w=10e-06 l=0.166e-06 sidenum=1 ngcon=1

+ \$LDD[ndriftotp]

5.6.3 CDF Parameters

Parameter	Prompt	Description
w	Width drawn (M)	Width of the transistor
l	Length drawn (M)	Length of the transistor
m	Nb of devices in //	Number of parallel devices generated when creating the layout
sidenum	Nb of sides	1 transistor on side or 2 on each side
ngcon	Nb of gate access	1 or 2 pin of metal1 to access to the grid
t	Operating temperature (deg. C)	Value of current temperature
trise	Temperature rise (deg. C)	Difference of temperature between of the circuit and the instance
mismatch	mismatch	Boolean which gives the information to models to take into account mismatch or not
pre_layout_local	Post Layout extraction	Activate the default parasite in model
nsig_vto	nsig_vto	Will disappear in 2.5
nsig_uo	nsig_uo	Will disappear in 2.5
nsig_dibl	nsig_dibl	Will disappear in 2.5
nsig_lvaro	nsig_lvaro	Will disappear in 2.5
nsig_wvaro	nsig_wvaro	Will disappear in 2.5
description	Description	Description given by the model
soa	Safe Operating Area	Check that the device is correctly used, during the simulation if this option is set, warning are displayed in case of misusage.



5.7 Egpcap

5.7.1 Symbols

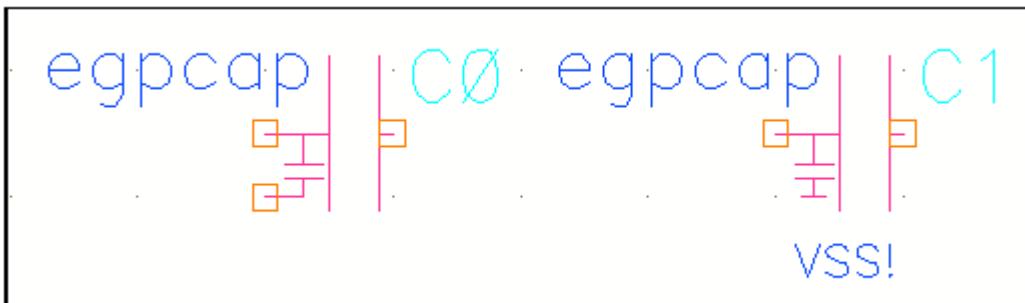


Figure 66: egpcab (right) and egpcap_b (left) symbols

On the egpcap symbol we can notice, the inherited pin for the bulk linked to VSS potential.

5.7.2 Netlists

→ **auCdl:**

```
CC1 net1 net2 $[egpcap] $SUB=VSS m=1 l=1u w=1u nf=1 nrep=1
```

```
CC0 net3 net4 $[egpcap] $SUB=net5 m=1 l=1u w=1u nf=1 nrep=1
```

→ **Eldo**

```
XC1 NET1 NET2 VSS! egpcap l=1u w=1u nf=1 nrep=1 setres=-2 setind=-2 m=1
```

```
+soa=1
```

```
XC0 NET3 NET4 NET5 egpcap l=1u w=1u nf=1 nrep=1 setres=-2 setind=-2 m=1
```

```
+soa=1
```

→ **Hspice**

```
xc1 net1 net2 vss! egpcap l=1e-6 w=1e-6 nf=1 nrep=1 setres=-2 setind=-2 m=1 soa=1
```

```
xc0 net3 net4 net5 egpcap l=1e-6 w=1e-6 nf=1 nrep=1 setres=-2 setind=-2 m=1 soa=1
```

→ **Spectre**

```
C1 (net1 net2 VSS!) egpcap l=1u w=1u nf=1 nrep=1 setres=-2 setind=-2 m=1 soa=1
```

```
C0 (net3 net4 net5) egpcap l=1u w=1u nf=1 nrep=1 setres=-2 setind=-2 m=1 soa=1
```

5.7.3 Pins

Device	Pins
egpcap	n, p and bulk inherited
Egpcap_b	n, p and b

5.7.4 CDF parameters





Parameter	Prompt	Description
m	Multiplicity	
descripiton	Description	Description of the model used
dimensionMode	Dimension by Geometry	Choosing dimension mode: electric or geometric
value	value	Value of the capacitor in accumulation mode
value_dep	value (depletion)	Value of the capacitor in depletion mode
l	Gate Length (M)	Length of the gate
w	Total Gate Width (M)	Width of the gate
nf	Number Of Gates	Number of parallel gate in the device
nrep	Number of RX Shapes	Multiply the shape of active in order to create gates in series
capbulk	Bulk	Polarization od the bulk pin which is inherited
trise	Temperature Deviation	
sizedup	Sized Up	
subres	Substrate Resistance	
setres	Resistance	
setind	Inductance	
guardRing	Guard Ring	Add an Nwel guardring aroud the device
routing	M1 Routing?	Route all the source and drain pin together with M1 metal



Parameter	Prompt	Description
rails	M1 Rails?	link the gates together
createPins	Create Pins w/o Routing?	Adding shapes of M1;pin on the pin of the device
RecommendedRulesSelect	Select Rule Sets	Choosing between 2 Rule Sets: RecommendedRules and Interdigitated. Interdigitated adds the LVS;drawing4 marker on the device, that way the LVS consider that all the gates under the marker are considered as 1 device
rodObj	Enable ROD Objects?	Enable the user to create a RODobjjet in Cadence Database
Soa	Safe Operating Area	Check that the device is correctly used, during the simulation if this option is set, warning are displayed in case of misusage.

5.8 Varactors: cvar_eg, cvar_eg_diff, cvar_eg_atto

The varactors are non-linear devices that provides a voltage dependent capacitance. The MOS varactors are N+poly/N-Well varactors. The devices described in this section do not require any additional processing or masks.

Single EG NMOS Varactor	cvar_eg	x					x	
Differential EG NMOS Varactor	cvar_eg_diff	x					x	
Attofarad EG NMOS Varactor	cvar_eg_atto	x					x	

Figure 67: 2 new varactors

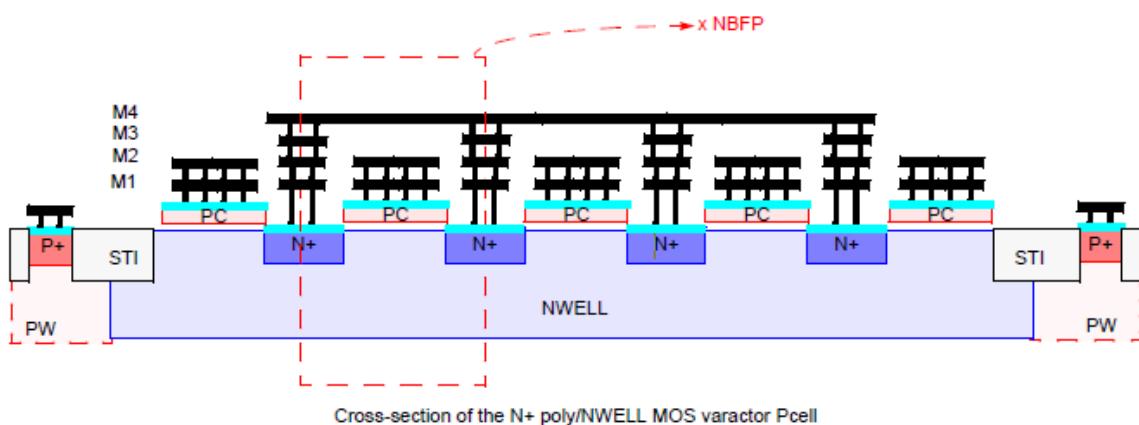


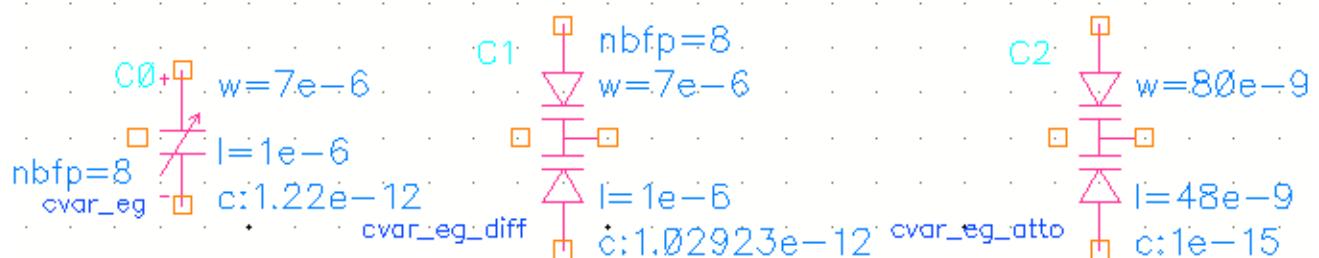
Figure 68: Cross section of the varactors

For these devices the following specific layers has been added:

Special CAD Levels (for reference only)		
Name	Number	Description
MKR;cvarST	201;91	Marker layer to cover RF varactor structure

Figure 69: specific layer

5.8.1 Symbols and pins



Device	Pin order
Cvar_eg	in out sub
Cvar_eg_diff	in1 in2 out1 sub
Cvar_eg_atto	in1 in2 out1 sub

5.8.2 Netlists

→ auCDL

```
XC0 net3 net2 net1 cvar_eg W=7.0e-6 L=1.0e-6 NBFP=8 NBCELL=2
XC1 net4 net7 net6 net5 cvar_eg_diff W=7.0e-6 L=1.0e-6 NBFP=8 NBCELL=2
XC2 net8 net11 net10 net9 cvar_eg_atto w=80e-9 nbline=2 nbcolumn=2
.ENDS
```

→ eldoD

```
XC0 NET3 NET2 NET1 cvar_eg l=1.0e-6 w=7.0e-6 nbfp=8 nbcell=2 mismatch=1
XC1 NET4 NET7 NET6 NET5 cvar_eg_diff l=1.0e-6 w=7.0e-6 nbfp=8 nbcell=2
+mismatch=1
XC2 NET8 NET11 NET10 NET9 cvar_eg_atto w=80e-9 nbline=2 nbcolumn=2
+mismatch=1
```

**→ Hspice**

```
xc0 net3 net2 net1 cvar_eg l=1e-6 w=7e-6 nbfp=8 nbcell=2 mismatch=1
xc1 net4 net7 net6 net5 cvar_eg_diff l=1e-6 w=7e-6 nbfp=8 nbcell=2 mismatch=1
xc2 net8 net11 net10 net9 cvar_eg_atto w=80e-9 nbline=2 nbcolumn=2 mismatch=1
.END
```

→ Spectre

```
C0 (net3 net2 net1) cvar_eg l=1.0e-6 w=7.0e-6 nbfp=8 nbcell=2 mismatch=1
C1 (net4 net7 net6 net5) cvar_eg_diff l=1.0e-6 w=7.0e-6 nbfp=8 nbcell=2 \
mismatch=1
C2 (net8 net11 net10 net9) cvar_eg_atto w=80e-9 nbline=2 nbcolumn=2 \
mismatch=1
```

5.8.3 CDF parameters

Parameter	Prompt	Unit	Description
c	Capacitance	F	Value of the capacitance resulting of the size of geometry of the device
w	Width	M	Width of the varactor
nbfp	Finger number		Number of fingers between 1 and 50
l	Length	M	Length of the varactor
mismatch	mismatch		Boolean which gives the information to models to take into account mismatch or not
nbcell	nbcell		Number of cell in the device in parallel
Description	ModelDescription		Description given by the model



5.9 OTP capacitor

5.9.1 Supported devices:

Miscellaneous					
Device	Name in DK	Flipwell	GPF	Bulk	Comment
OTP capacitor	nfetotp		x		Anti-fuse application
OTP capacitor on flipwell	nfetotp_fw	x			Anti-fuse application

5.9.2 Symbols

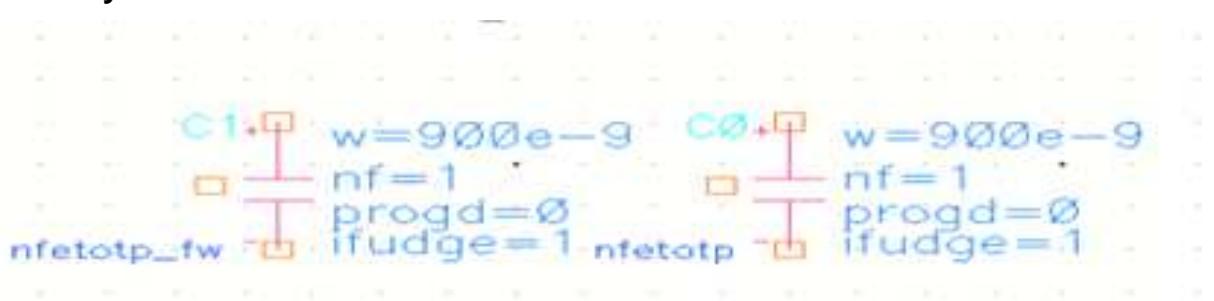


Figure 70: Symbols of devices from Miscellaneous category

5.9.3 CDF Parameters

Parameter	Prompt	Unit	Description
w	Width	M	Width of the resistor
nf	Number of fingers		Number of finger for the mos used as capacitance
m	Nb of Devices in //		Number of devices in parallel
ifudge	Mult factor for degraded current		Factor to apply on the equations ta take count of the degraded current
description	Description		Description given by the model

Table 31: nfetotp(_fw) parameters



5.9.4 Netlist Formats

Parameter values are left out in the sample netlist lines below.

5.9.4.1 Eldo

- nfetotp

XC plus minus sub nfetotp w= nf= mult= progd= ifudge

5.9.4.2 Hspice

- nfetotp

xc plus minus sub nfetotp w= nf= mult= progd= ifudge

5.9.4.3 CDL

- nfetotp

CC plus minus <model> SUB w= nf

5.10 Metal Resistors

5.10.1 Supported device types :

- rm1x :
 - o metals M1 to M6 available for stacks 8M and 10M
 - o metals M1 to M5 available for stacks 7M and 6M
- rm2x :
 - o metals B1 and B2 available for all stacks
- rm8x :
 - o metals IA and IB available for stacks 8M, 10M and 7M
 - o not available for stack 6M
- rmlb:
 - o metal LB available for all stacks



5.10.2 Symbol:

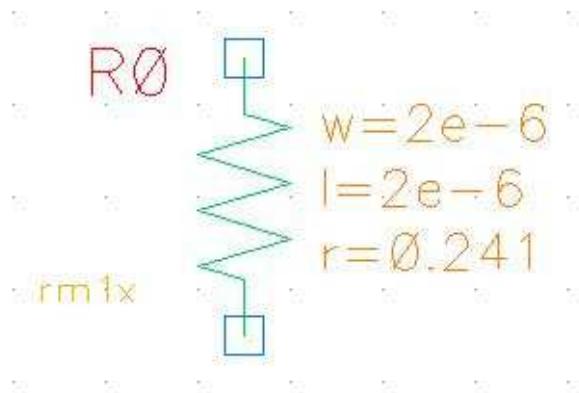


Figure 71: Resistor symbol

Terminal order: plus minus

5.10.3 Device Parameters:

Parameter	Prompt	Unit	Description
description	Description		Show the model used in this device
dimensionMode	Dimension by Geometry		Switch: User can define value and either length or width or w and l of the device
r	Value	Ohm	Total nominal resistance. Dependent on dimensionMode switch the value can be entered by the user or is calculated from given w, l, ser and par.
w	Width	m	Width of one resistor stripe, can also be calculated based on l and r if switch dimensionMode is set to off.
l	Length	m	Length of one resistor stripe, can also be calculated from w and r if switch dimensionMode is set to off.
metal	Metal Position		Used to select the metal level

Table 32: Resistor parameters



5.10.4 Netlist Formats

Parameter values are left out in the sample netlist lines below.

Eldo:

```
x plus minus <model> w= l=
```

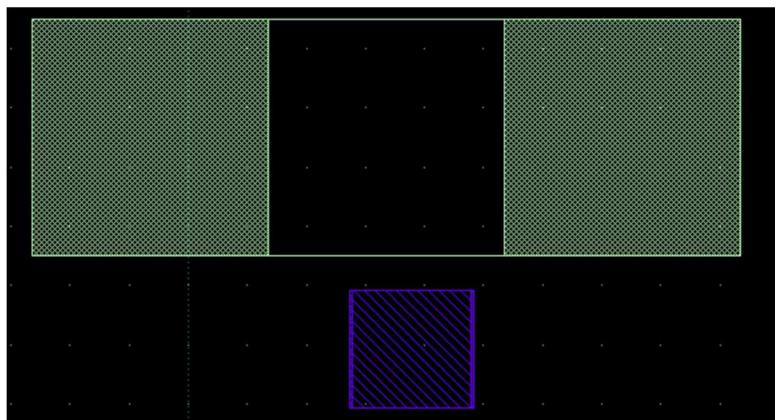
Hspice:

```
x plus minus <model> w= l=
```

CDL:

```
R plus minus $[<model>] w= l= metal=[1-6]
```

5.10.4.1 Layout PCell



5.11 Fringe Capacitors

5.11.1 Supported device types

- Cfrm1x:
 - o metals M1 to M6 available for stacks 8M and 10M
 - o metals M1 to M5 available for stacks 7M and 6M
- cfrm2x :
 - o metals B1 and B2 available for all stacks
- cfrm8x :
 - o metals IA and IB available for stacks 8M, 10M and 7M
 - o not available for stack 6M



5.11.2 Symbol

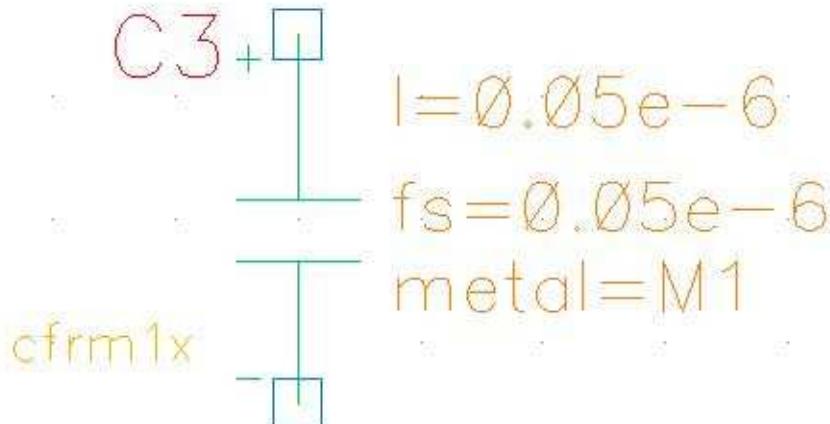


Figure 72: Fringe Capacitor symbol

Terminal order: plus minus

5.11.3 Device Parameters

Parameter	Prompt	Unit	Description
description	Description		Displays the model type of the device
l	Length	m	Length of the capacitor.
fs	Finger space	m	Metal spacing
metal	Metal Position		Metal level.

Table 33: Fringe capacitors parameters

5.11.4 Netlist Formats

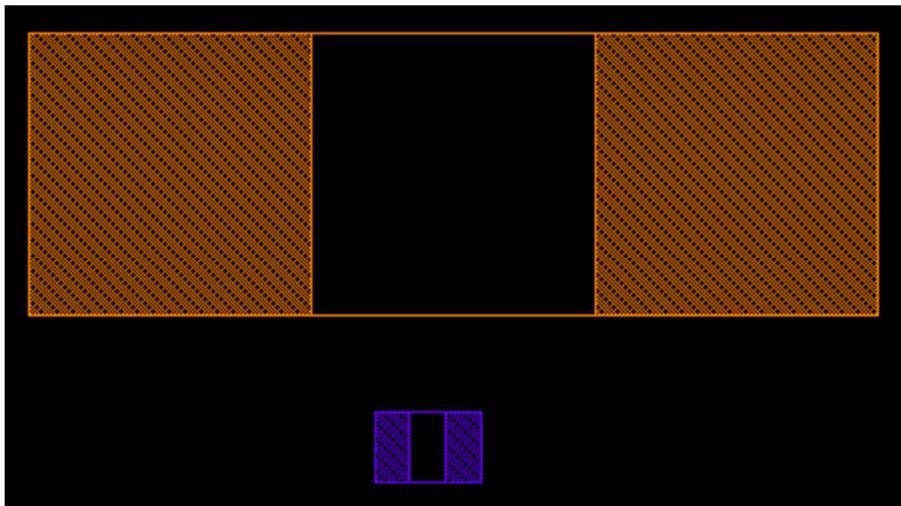
Parameter values are left out in the sample netlist lines below.



CDL

```
CC3 plus minus $[cfrm1x] l= fs= metal=[1-6]
```

5.11.5 Layout PCell





6 ST_C32_addon_AMS

The Design Kit now supports a new library for RF designs: ST_C32_addon_AMS. This library contains 6 inductors and 3 cmims and 2 transmission lines (in 8ML only)

6.1 Main purpose:

->ST_C32_addon_AMS Devices list

- **Inductance**: ind_lohq, inddif_lohq, ind_hq, inddif_lohq, ind_lohq_high_perf and inddif_lohq_high_perf
- **Cmim**: cmim16acc, cmim16acc_2p, cmim16_sh
- **Transmission Lines (8ML)**: microstripe_tline and differential_tline

6.2 Devices List in ST_C32_addon_AMS

Device	Description
Cmim16acc	MIM Well controlled for RF : Cmim16acc : 3pin= plus, minus, psub Cmim16acc_sh : 3pin= plus, minu, sh Cmim16acc_2p : 2pin= plus, minus ; parasitic by LVS
Ind_hq	Thick copper differential HQ inductors with patterned GND shield: ind_hq_6U1x_2U2x_2T8x_LB : 3 pins in out sub inddif_hq_6U1x_2U2x_2T8x_LB : 4 pins in mp out sub
Ind_lohq	Thick copper differential low HQ inductors with patterned GND shield ind_lohq_6U1x_2U2x_2T8x_LB : 3 pins in out sub inddif_lohq_6U1x_2U2x_2T8x_LB : 4 pins in mp out sub
Ind_lohq_high_perf	Thick copper differential low HQ High Perf inductors with patterned GND shield ind_lohq_high_perf_6U1x_2U2x_2T8x_LB : 3 pins in out sub inddif_lohq_high_perf_6U1x_2U2x_2T8x_LB : 4 pins in mp out sub
Transmission lines (8ML)	microstrip_tline_6U1x_2T8x_LB : 3 pins in out sub differential_tline_6U1x_2T8x_LB : 5 pins in1 in2 out1 out2 sub





6.2.1 Cmim16acc

6.2.1.1 MIM Well controlled for RF: CMIM

The MIM decoupling capacitance (DECAP) is a metal dielectric capacitor located between the first and the second 8x metallization levels (IA and IB respectively). The capacitance is connected through the via (XA) and metal level above the MIM (IB).

Layers Above/Below MIM		
Metallization Option	6U1x_2U2x_2T8x_LB	5U1x_2T8x_LB
Metal above MIM	IB	IB
VIA above MIM	XA .or. XABAR	XA .or. XABAR
Metal below MIM	IA	IA

MIM Capacitor - simplified cross-section

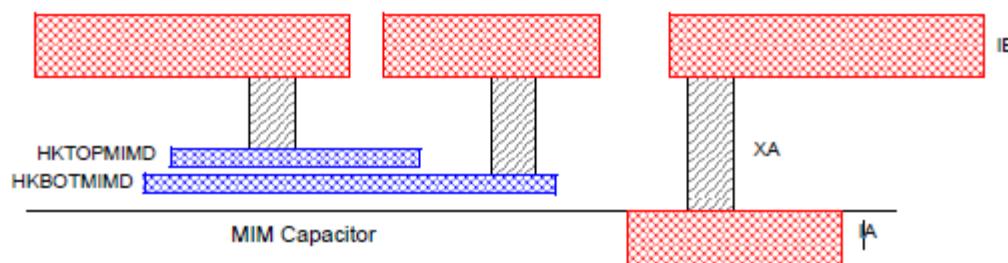


Figure 73: MIM capacitor simplified cross section

There are 3 types of cmim:

- Cmim16acc: 3pin= Top, Bot , Sub
- Cmim16acc_sh: 3pin= Top, Bot , Shield IA
- Cmim16acc_2p: 2pin= Top, Bot ; parasitic by LVS

Pin Order:

- Cmim16acc: minus plus psub
- Cmim16acc_2p: minus plus
- Cmim16acc_sh: minus plus sh

We can use this capacitor in the usual modes: square, Geometric and Value

- **Square:** only the capacitor value is available, w and l are calculated regarding c value and the limitations
- **Geometric:** user can choose the capacitor value and the width, then the length are calculated
- **Value:** the width and the length are set by the user then the c value is calculated

- **Limitations**

Area max: 20 000 μm^2

Area min = lmin*wmin= 1.96*1.96 μm^2



6.2.1.2 Symbols and pins

Devices	Pin Name
Cmim16acc	plus, minus
Cmim16acc_2p	Plus, minus
Cmim16acc_sh	plus, sh, minus

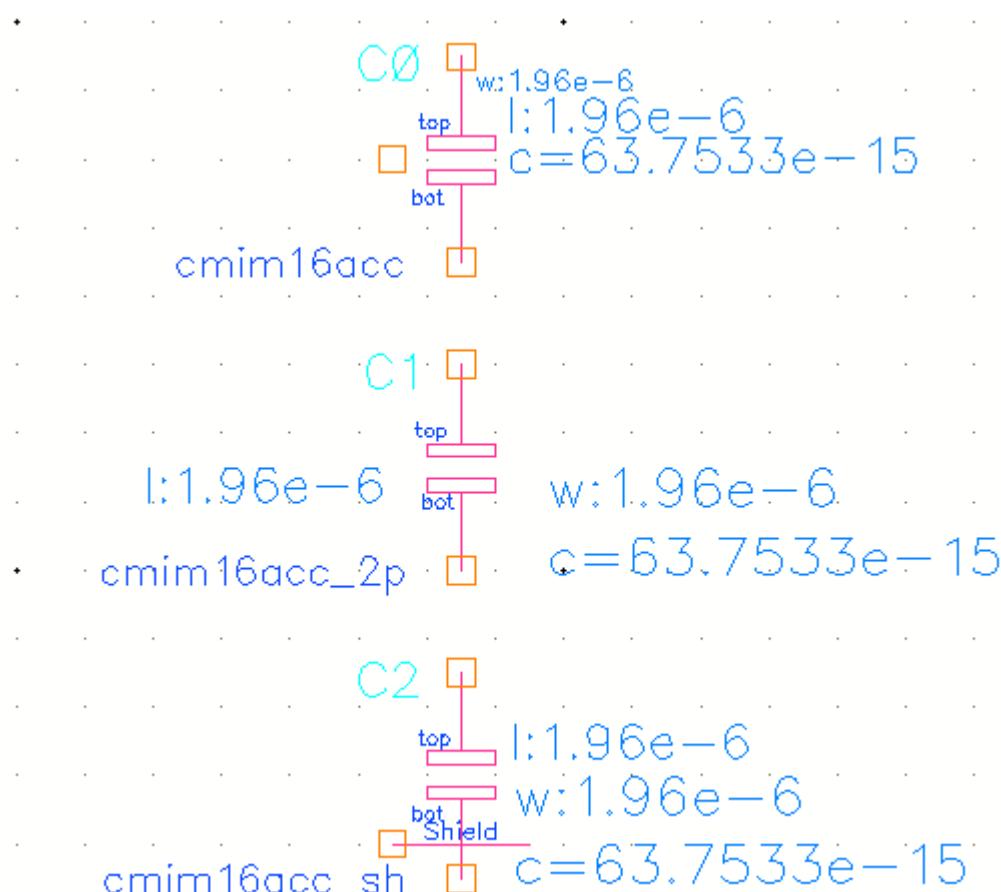


Figure 74: `cmim16acc` symbols

6.2.1.3 Netlists

Netlists with $x0=\text{cmim16acc}$, $x1=\text{cmim16acc_2p}$ and $x2=\text{cmim16acc_sh}$

→ auCDL:

CC0 net1 net2 cmim16acc w=1.96e-6 l=1.96e-6 m=1 \$SUB=net3

CC1 net4 net5 cmim16acc_2p w=1.96e-6 l=1.96e-6 m=1

CC2 net8 net7 cmim16acc_sh w=1.96e-6 l=1.96e-6 m=1 \$SUB=net6

**➔ eldoD:**

```
XC0 NET1 NET2 NET3 cmim16acc w=1.96e-6 l=1.96e-6 c=6.37533e-14 relax=0
```

```
+mult=1 mismatch=1 dc_mdev=0
```

```
XC1 NET4 NET5 cmim16acc_2p w=1.96e-6 l=1.96e-6 c=6.37533e-14 relax=0
```

```
+mult=1 mismatch=1 dc_mdev=0
```

```
XC2 NET8 NET7 NET6 cmim16acc_sh w=1.96e-6 l=1.96e-6 c=6.37533e-14 relax=0
```

```
+mult=1 mismatch=1 dc_mdev=0
```

➔ hspiceD:

```
xc0 net1 net2 net3 cmim16acc w=1.96e-6 l=1.96e-6 c=63.7533e-15 relax=0 mult=1 mismatch=1 dc_mdev=0
```

```
xc1 net4 net5 cmim16acc_2p w=1.96e-6 l=1.96e-6 c=63.7533e-15 relax=0 mult=1 mismatch=1 dc_mdev=0
```

```
xc2 net8 net7 net6 cmim16acc_sh w=1.96e-6 l=1.96e-6 c=63.7533e-15 relax=0 mult=1 mismatch=1 dc_mdev=0
```

➔ spectre:

```
C0 (net1 net2 net3) cmim16acc w=1.96e-6 l=1.96e-6 c=6.37533e-14 relax=0 mult=1 mismatch=1 dc_mdev=0
```

```
C1 (net4 net5) cmim16acc_2p w=1.96e-6 l=1.96e-6 c=6.37533e-14 relax=0 mult=1 mismatch=1 dc_mdev=0
```

```
C2 (net8 net7 net6) cmim16acc_sh w=1.96e-6 l=1.96e-6 c=6.37533e-14 relax=0 mult=1 mismatch=1 dc_mdev=0
```

6.2.1.4 CDF Parameters:

CDF name	Prompt	Description
calcmode	Recalculate Capacitor	Mode of calculation: <ul style="list-style-type: none">- Geometry: capa and w given => length, area and peri calculate- Value: w/l given by the user => c, area and peri
square	Square	Mode where designer choose a capacitance value, then the cmim is recalculate with a square geometry
c	Capacitance (F)	Capacitance value
w	Width (um)	Width of the device
l	Length (um)	Length of the device
mismatch	mismatch	Boolean which gives the information to models to take into account mismatch or not



m	Nb of devices in //	Number of devices in parallel when generating the layout
temp_condition	Temp Condition	Use the default: "model" or enter a specific value using "custom" mode
localtemp	Local Device temp (Celsius)	Local temperature of the device, not the chip
via_number	Number of via	Will disappear in 2.5
nviatop	Number of via top	Will disappear in 2.5
nviabot	Number of via bottom	Will disappear in 2.5
relax	Relaxation	Use relax circuit in model

6.2.2 Inductances

Inductors are realized by one or by stacking the several copper metal levels available in the core CMOS028 FDSOI process. The Alucap level (design level LB) is used to further reduce the coil resistance. A trench at PADOPEN (VV design level) connects the Alucap to the top-metal copper levels. The inductor coil is covered with an MKR;indSTmarker layer for DRC and LVS verification and to avoid dummy/tile generation on M1, Mx, Bx, Ix and LB.

To achieve high quality factors, inductor layouts for any metallization options shall always include at least Mtop. The use of additional metal levels or LB to reduce the series resistance is allowed.

In order to respect DRM density rules, the number of turns is limited to 2 or 3 and the width is limited to 11um when nbturn=3.

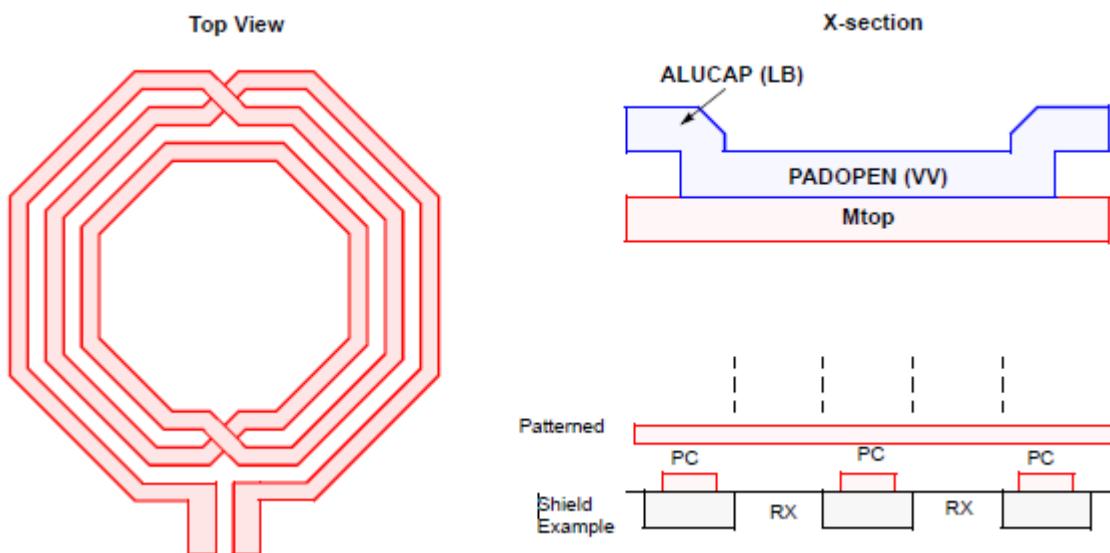


Figure 75: Inductor top view



Inductors		
Device	Name in DK	Comment
Low value High Q inductor	ind_lohq_6U1x_2U2x_2T8x_LB	6U1x_2U2x_2T8x_LB process only
Differential Low Value Q inductor	inddif_lohq_6U1x_2U2x_2T8x_LB	6U1x_2U2x_2T8x_LB process only
High Q inductor	ind_hq_6U1x_2U2x_2T8x_LB	6U1x_2U2x_2T8x_LB process only
Differential High Q inductor	inddif_hq_6U1x_2U2x_2T8x_LB	6U1x_2U2x_2T8x_LB process only
Low Value High Q High Performance inductor	ind_lohq_high_perf	6U1x_2T8x_LB only
Differential Low Value High Q High Performance inductor	inddif_lohq_high_perf	6U1x_2T8x_LB only

Figure 76: 4 different inductors

For these devices specific cad layers have been added:

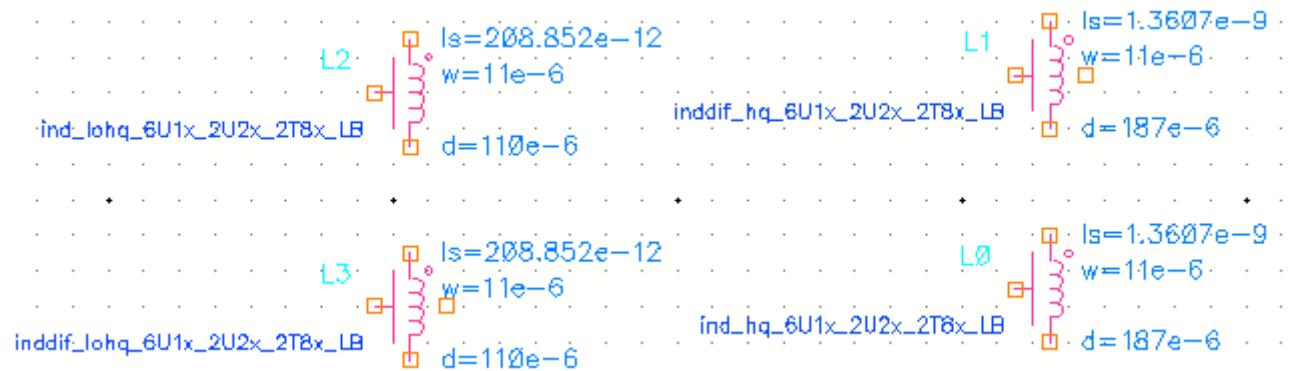
Special CAD Levels (for reference only)		
Name	Number	Description
MKR;indST	201;87	Marker layer covering the complete inductor
MKR;indlamwST	201;88	Marker layer covering the low area multi width inductor
MKR;indhqST	201;89	Marker layer covering the High Q inductor
MKR;indlohqST	202;44	Marker layer covering the low value High Q inductor

Figure 77: specific layers

6.2.2.1 Symbols and pins

Pin order:

- ind_lohq_6U1x_2U2x_2T8x_LB : in out sub
- inddif_lohq_6U1x_2U2x_2T8x_LB : in mp out sub
- inddif_hq_6U1x_2U2x_2T8x_LB : in mp out sub
- ind_hq_6U1x_2U2x_2T8x_LB : in out sub





6.2.2.2 Netlists:

L1: inddif_hq

L2:ind_lohq

L3: inddif_lohq

L4: ind_hd

→ auCdl

XL0 net3 net2 net1 ind_hq_6U1x_2U2x_2T8x_LB D=187e-6 W=11e-6 NBTURNS=2

XL2 net6 net5 net4 ind_lohq_6U1x_2U2x_2T8x_LB D=110e-6 W=11e-6

XL1 net9 net10 net8 net7 inddif_hq_6U1x_2U2x_2T8x_LB D=187e-6 W=11e-6

+ NBTURNS=2 MPOUT=1 WMP=13.2e-6

XL3 net13 net14 net12 net11 inddif_lohq_6U1x_2U2x_2T8x_LB D=110e-6 W=11e-6

+ MPOUT=1 WMP=13.2e-6

.ENDS

→ eldoD

XL0 NET3 NET2 NET1 ind_hq_6U1x_2U2x_2T8x_LB d=187e-6 w=11e-6 nbturns=2

+ls=1.3607E-09

XL2 NET6 NET5 NET4 ind_lohq_6U1x_2U2x_2T8x_LB d=110e-6 w=11e-6

+ls=0.2088519e-9

XL1 NET9 NET10 NET8 NET7 inddif_hq_6U1x_2U2x_2T8x_LB d=187e-6 w=11e-6

+nbturns=2 ls=1.3607E-09 mpout=1 wmp=13.2e-6

XL3 NET13 NET14 NET12 NET11 inddif_lohq_6U1x_2U2x_2T8x_LB d=110e-6 w=11e-6

+ls=0.2088519e-9 mpout=1 wmp=13.2e-6

→ Hspice

xl0 net3 net2 net1 ind_hq_6U1x_2U2x_2T8x_LB d=187e-6 w=11e-6 nbturns=2 ls=1.3607e-9

xl2 net6 net5 net4 ind_lohq_6U1x_2U2x_2T8x_LB d=110e-6 w=11e-6 ls=208.8519e-12

xl1 net9 net10 net8 net7 inddif_hq_6U1x_2U2x_2T8x_LB d=187e-6 w=11e-6 nbturns=2 ls=1.3607e-9
mpout=1 wmp=13.2e-6

xl3 net13 net14 net12 net11 inddif_lohq_6U1x_2U2x_2T8x_LB d=110e-6 w=11e-6 ls=208.8519e-12
mpout=1 wmp=13.2e-6

.END

→ spectre

L0 (net3 net2 net1) ind_hq_6U1x_2U2x_2T8x_LB d=187e-6 w=11e-6 nbturns=2 ls=1.3607E-09

L2 (net6 net5 net4) ind_lohq_6U1x_2U2x_2T8x_LB d=110e-6 w=11e-6 ls=0.2088519e-9

L1 (net9 net10 net8 net7) inddif_hq_6U1x_2U2x_2T8x_LB d=187e-6 w=11e-6 nbturns=2 ls=1.3607E-09
mpout=1 wmp=13.2e-6





L3 (net13 net14 net12 net11) inddif_lohq_6U1x_2U2x_2T8x_LB d=110e-6 w=11e-6 ls=0.2088519e-9
mpout=1 wmp=13.2e-6

6.2.2.3 CDF Parameters

→ Inddif_hq and inddif_lohq

CDF Name	Prompt	Description
calcmode	Recalculate Inductor	In Geometric mode, Diameter and length are recalculate depending on Inductance value, nturns and width In Value mode , Inductance value and length are recalculate depending on nturns, Length and width
ls	Inductance value (H)	Value of the inductance in Henry
nturns	Number of turns	Number of turn of the device
w	Width of Coil (M)	Width of the device
d	Diameter (M)	Diameter of the device
l	Length (M)	Length if the device
wmp	Middle point width (M)	Width of the middle point of the device
simp	Middle Point Access	Change the point access side, on the top it is a short one, one the bottom, it is a long one
ModelDescription	Description	Description given by the model

→ Ind_hq and ind_lohq

CDF Name	Prompt	Description
calcmode	Recalculate Inductor	In Geometric mode, Diameter and length are recalculate depending on Inductance value, nturns and width In Value mode , Inductance value and length are recalculate depending on nturns, Length and width
ls	Inductance value (H)	Value of the inductance in Henry
w	Width of Coil (M)	Width of the device
d	Diameter (M)	Diameter of the device



I	Length (M)	Length if the device
ModelDescription	Description	Description given by the model

6.2.3 Transmission Lines

Transmission lines are made of LB, with sidewalls and a patterned shield. This shield is made with M1, M2 and M3 stripes perpendicular to the TL, below the whole device (sidewalls + TL itself). The transmission line is covered with several marker layers for DRC and LVS verification and to avoid dummy/tile generation. The tile generation is blocked from LB to M1.

Two Transmission Line devices are available: one single transmission line or two transmission lines (Differential TL) between sidewalls are allowed.

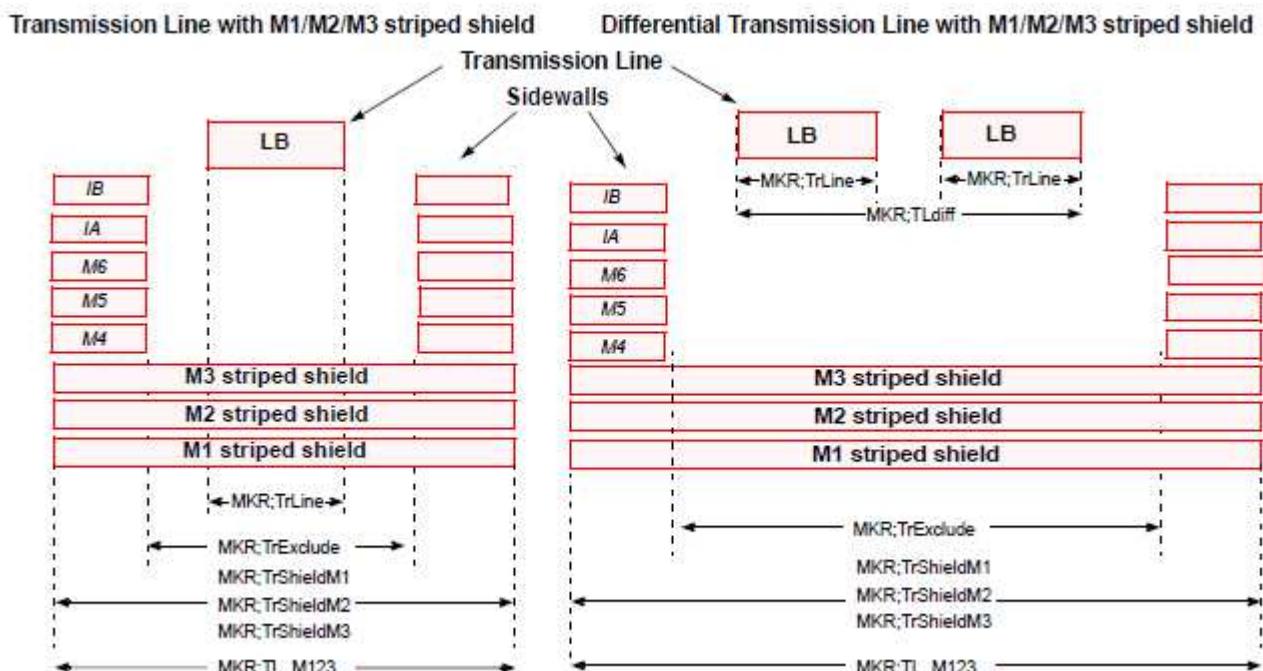


Figure 79: Cross-section of transmission lines

Transmission Lines		
Device	Name in DK	Comment
Transmission Line MicroStrip	microstrip_tline_6U1x_2T8x_LB	6U1x_2T8x_LB only
Differential Transmission Line	differential_tline_6U1x_2T8x_LB	6U1x_2T8x_LB only

Figure 80: 4 Different transmission lines

For these devices specific cad layers have been added:

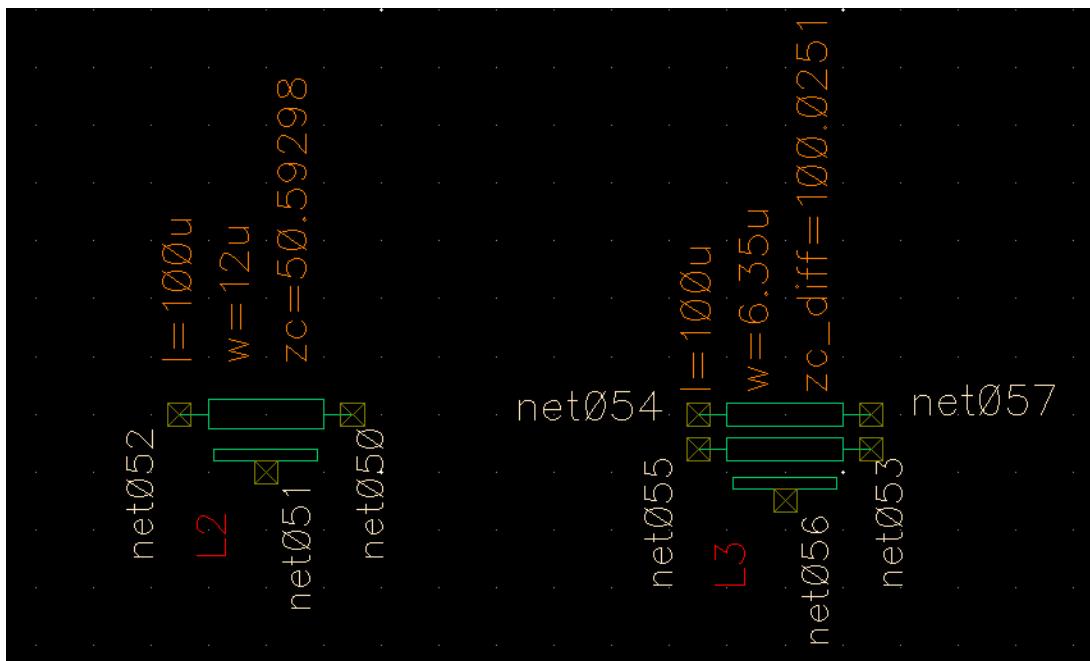
Special CAD Levels (for reference)		
Name	Number	Description
TrLine,mkr	204,215	Marker layer covering the transmission line
TLdiff,mkr	204,216	Recognition marker layer covering the Differential transmission line
TL_M123,mkr	204,218	Marker layer covering entire transmission line cell with M1/M2/M3 striped shield (TL + Side-walls)
TrShieldM1,mkr	204,249	Marker layer covering the M1 shield under the transmission line
TrShieldM2,mkr	204,250	Marker layer covering the M2 shield under the transmission line
TrShieldM3,mkr	204,251	Marker layer covering the M3 shield under the transmission line
TrExclude,mkr	204,253	Marker layer covering the Metal-empty area under the transmission line

Figure 81: specific layers

6.2.3.1 Symbols and pins

Pin order:

- microstrip_tline_6U1x_2T8x_LB: in out sub
- differential_tline_6U1x_2T8x_LB: in1 in2 out1 out2 sub

**Figure 82: tlines symbols**

6.2.3.2 Netlists:

L0: microstrip_tline_6U1x_2T8x_LB

L1: differential_tline_6U1x_2T8x_LB

→ auCdl

* Library Name: ST_C32_addon_AMS



* Cell Name: microstrip_tline_6U1x_2T8x_LB

* View Name: schematic

```
*****  
.SUBCKT microstrip_tline_6U1x_2T8x_LB in out sub l=100u w=12u
```

```
*.PININFO in:B out:B sub:B
```

```
.ENDS
```

```
*****  
* Library Name: ST_C32_addon_AMS
```

```
* Cell Name: differential_tline_6U1x_2T8x_LB
```

```
* View Name: schematic
```

```
*****  
.SUBCKT differential_tline_6U1x_2T8x_LB in1 in2 out1 out2 sub l=100u w=6.35u
```

```
*.PININFO in1:B in2:B out1:B out2:B sub:B
```

```
.ENDS
```

```
*****  
* Library Name: TEST
```

```
* Cell Name: test_tL
```

```
* View Name: schematic
```

```
*****  
.SUBCKT test_tL
```

```
*.PININFO
```

```
XL0 net3 net1 net2 microstrip_tline_6U1x_2T8x_LB l=100u w=12u
```

```
XL1 net5 net6 net8 net4 net7 differential_tline_6U1x_2T8x_LB l=100u w=6.35u
```

```
.ENDS
```

➔ eldoD

```
XL0 NET3 NET1 NET2 microstrip_tline_6U1x_2T8x_LB l=100u w=12u
```

```
XL1 NET5 NET6 NET8 NET4 NET7 differential_tline_6U1x_2T8x_LB l=100u
```

```
+w=6.35u
```

➔ Hspice

```
xl0 net3 net1 net2 microstrip_tline_6U1x_2T8x_LB l=100e-6 w=12e-6
```

```
xl1 net5 net6 net8 net4 net7 differential_tline_6U1x_2T8x_LB l=100e-6 w=6.35e-6
```

➔ spectre

```
L0 (net3 net1 net2) microstrip_tline_6U1x_2T8x_LB l=100u w=12u
```

```
L1 (net5 net6 net8 net4 net7) differential_tline_6U1x_2T8x_LB l=100u w=6.35u
```

6.2.3.3 CDF Parameters

➔ microstrip_tline_6U1x_2T8x_LB





CDF Name	Prompt	Description
zc	Characteristic impedance [ohms]	Impedance of the line
w	Line width	Width of the line
l	Line length	Length if the device
description	Description	Description given by the model

➔ **differential_tline_6U1x_2T8x_LB**

CDF Name	Prompt	Description
zc_diff	Characteristic impedance [ohms]	Impedance of the line
w	Lines width	Width of the 2 lines
l	Line length	Length if the device
description	Description	Description given by the model

6.2.3.4 Layout pcells

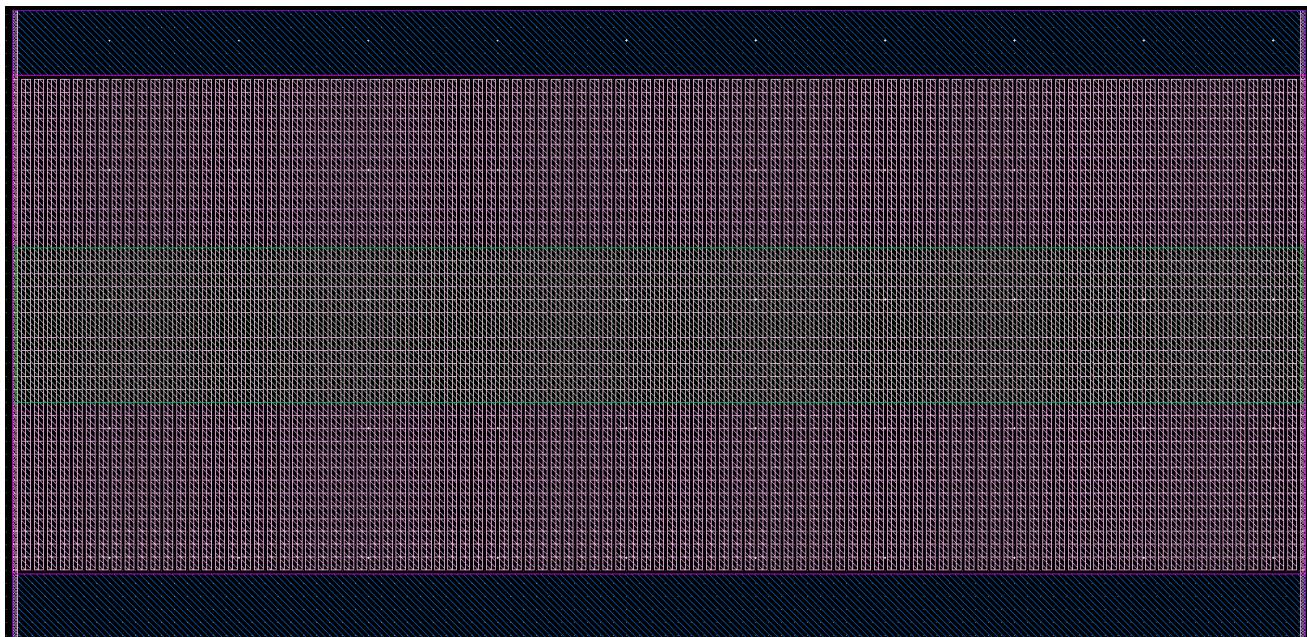


Figure 83: microstrip_tline_6U1x_2T8x_LB layout view



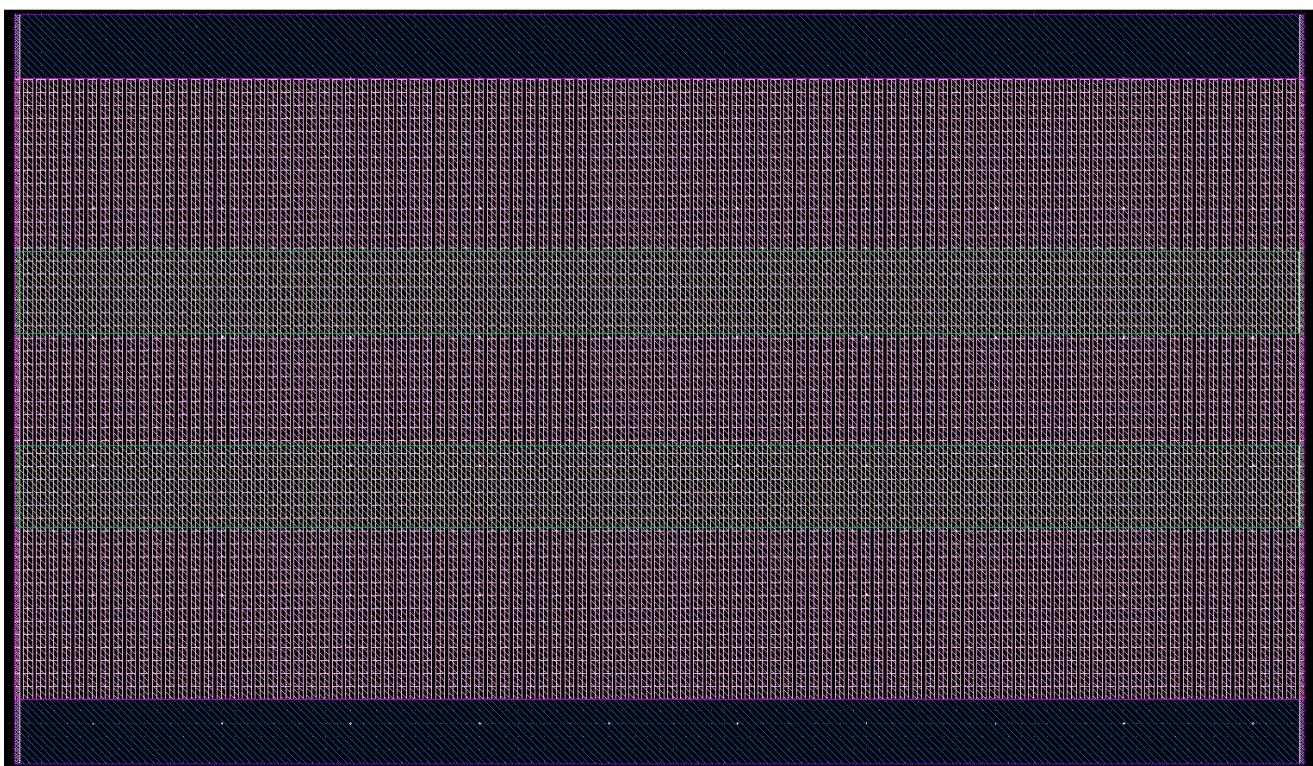


Figure 84: differential_tline_6U1x_2T8x_LB layout view





Devices





Device Category: BIOPOLARS (in library cmos32lp)

Device Type	Cells Names In Device Library
VPNP	vppn

Table: BIOPOLARS device types and cells

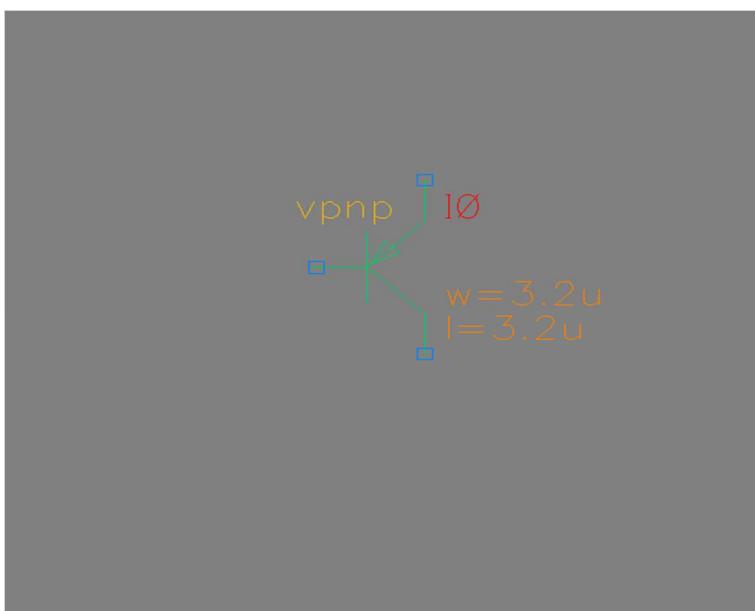
Device: vppn

Parameter	Prompt	Units	Default	Range
DFM_PCell	Robust Rules	-	0	'0, 1
w	w	m	3.2u	-
l	l	m	3.2u	-
nf	Number of Emitters	-	1	-
nrep	Repetition	-	1	-
trise	Temperature Deviation	-	-	-
sizedup	Sized Up	-	-	-
dic_mdev	Collector Current Deviation	-	0	-
dib_mdev	Base Current Deviation	-	0	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1



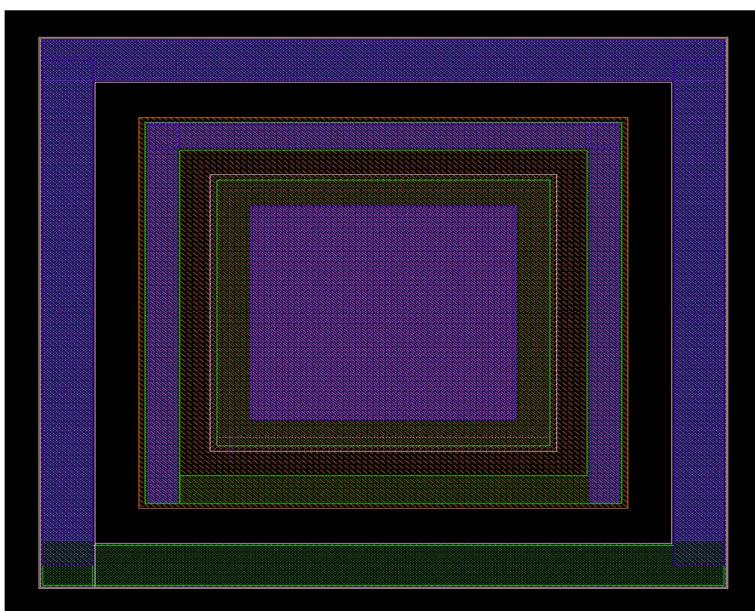


Symbol View:



Terminals order: c, b, e

Layout View:





Device Category: CAPACITORS (in library cmos32lp)

Device Type	Cells Names In Device Library
EG POLY N+ Nwell capacitor	egncap_b, egncap

Table: CAPACITORS device types and cells

Device: egncap_b

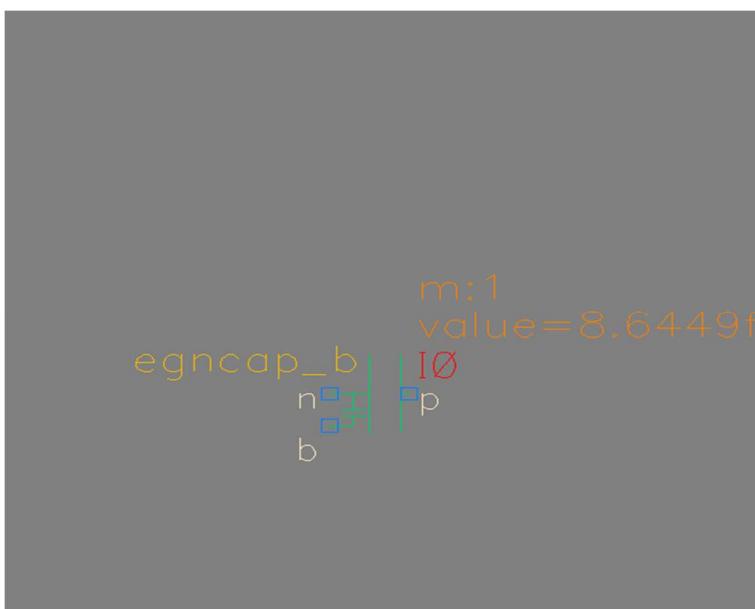
Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
value	Value at 1.8V	F	-	-
value_dep	Value (depletion) at -1.8V	F	-	-
l	l	m	1u	-
w	w	m	1u	-
nf	Number of Gates	-	1	-
nrep	Number of RX Shapes	-	1	-
setres	Resistance	Ohms	-2	-
setind	Inductance	H	-2	-
guardRing	Guard Ring	-	-	-
routing	M1 Routing?	-	t	-
rails	M1 Rails?	-	t	-
createPins	Create Pins w/o Routing?	-	t	-
DFM_PCell	Robust Rules	-	0	'0, 1
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rodObj	Enable ROD Objects?	-	-	-
soa	Safe Operating Area	-	1	'0, 1
rsx	Substrate Resistance	-	50	-





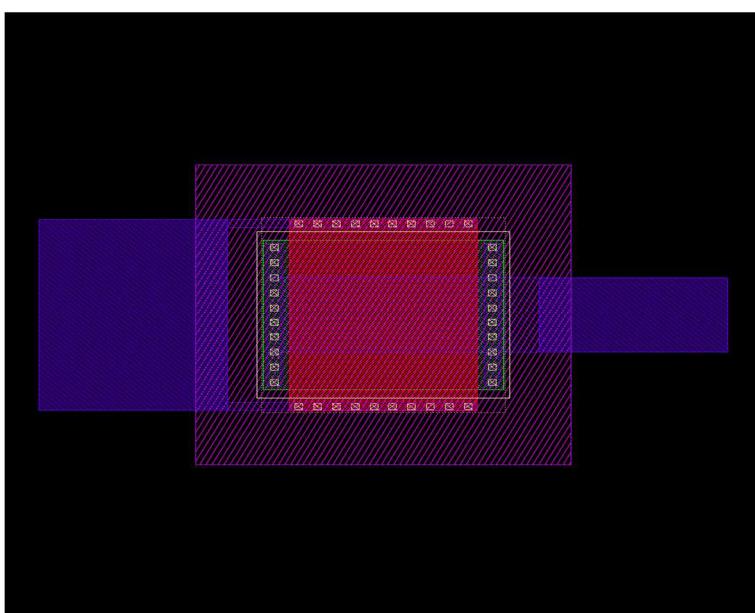


Symbol View:



Terminals order: p, n, b

Layout View:





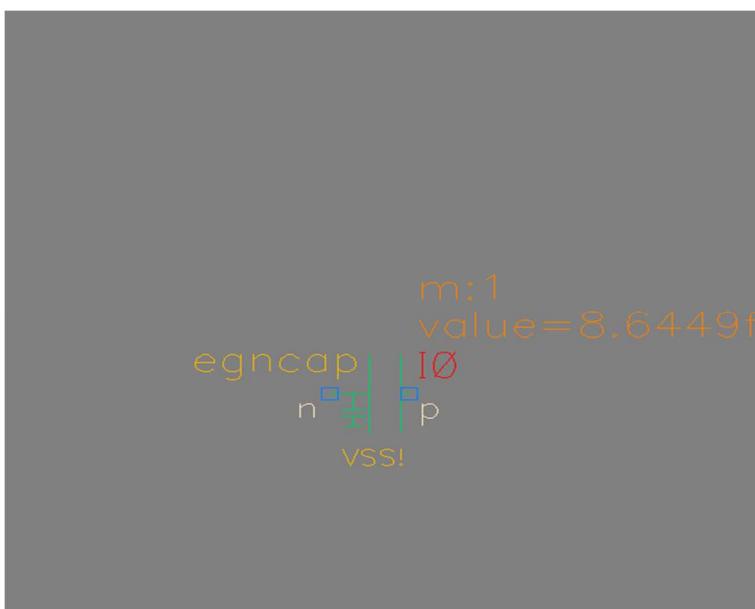
Device: egncap

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
value	Value at 1.8V	F	-	-
value_dep	Value (depletion) at -1.8V	F	-	-
l	l	m	1u	-
w	w	m	1u	-
nf	Number of Gates	-	1	-
nrep	Number of RX Shapes	-	1	-
capbulk	Bulk	-	[@lSup:%:VSS!]	-
setres	Resistance	Ohms	-2	-
setind	Inductance	H	-2	-
guardRing	Guard Ring	-	-	-
routing	M1 Routing?	-	t	-
rails	M1 Rails?	-	t	-
createPins	Create Pins w/o Routing?	-	t	-
DFM_PCell	Robust Rules	-	0	'0, 1
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rodObj	Enable ROD Objects?	-	-	-
soa	Safe Operating Area	-	1	'0, 1
rsx	Substrate Resistance	-	50	-



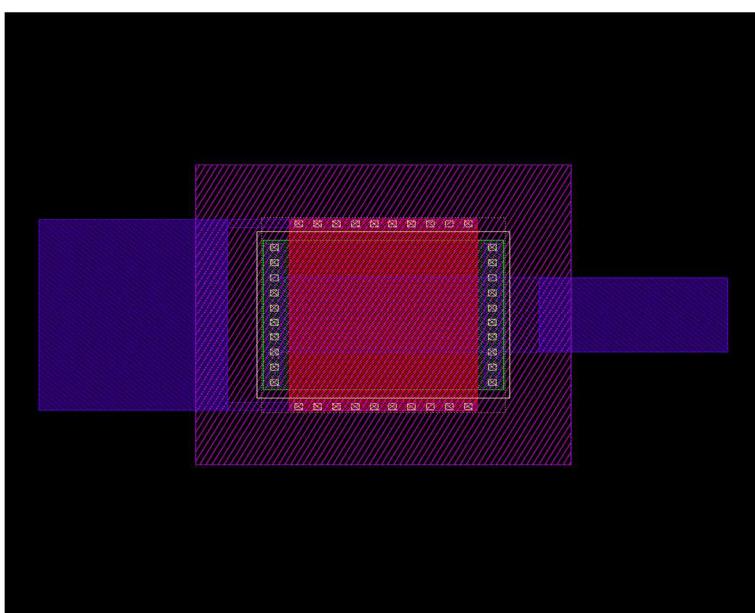


Symbol View:



Terminals order: p, n, b

Layout View:





Device Category: DIODES (in library cmos32lp)

Device Type	Cells Names In Device Library
Nwell/Psub Junction diode	diodenwx_lvs, diodenwx
P+ Floating Gate Tie-Down	tdpdnw
Pplus/Nwell Junction diode	egdiodenx, diodepnw
EG P+ Floating Gate Tie-Down	egtdpdnw
Niso/Psub Junction diode	diodetwx_lvs, diodetwx
EG N+ Floating Gate Tie-Down	egtdndsx
Pwell/Niso Junction diode	diodepwtw_lvs, diodepwtw
N+ Floating Gate Tie-Down	tdndsx
Nplus/Psub Junction diode	egdiodepnw, diodenx

Table: DIODES device types and cells

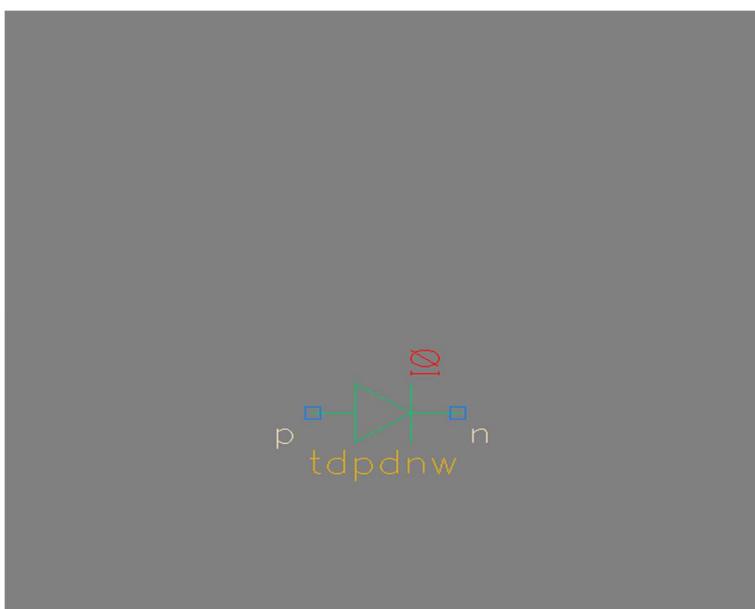
Device: tdpdnw

Parameter	Prompt	Units	Default	Range
DFM_PCell	Robust Rules	-	0	'0, 1
rectangle	Rectangular shape	-	t	-
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
width	Width (um)	-	1	-
height	Height (um)	-	1	-
NW_EXTENSION_OD	NW ext. on OD	-	None	'None, Right/Left, Top/Bot, Both
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1



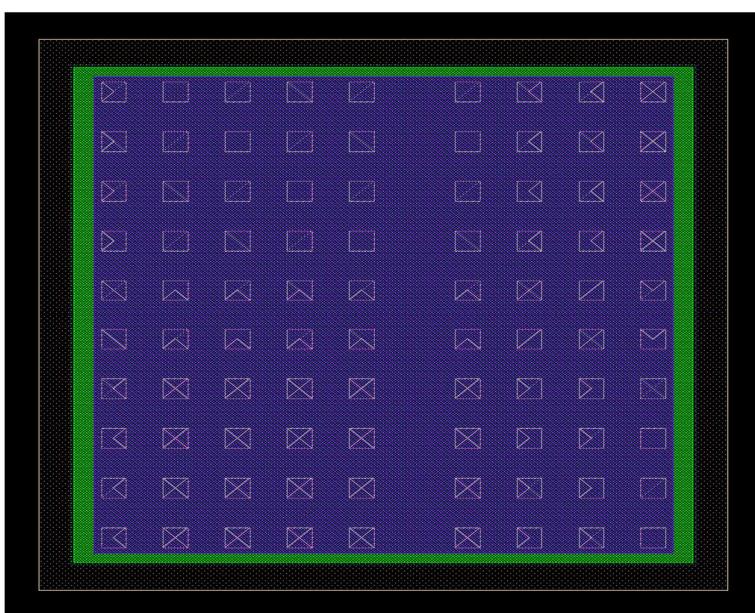


Symbol View:



Terminals order: p, n

Layout View:





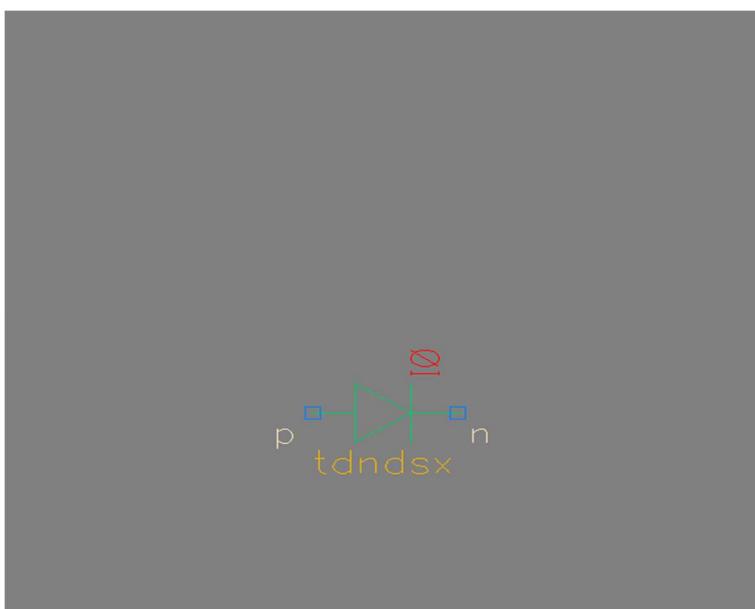
Device: tdndsx

Parameter	Prompt	Units	Default	Range
DFM_PCell	Robust Rules	-	0	'0, 1
rectangle	Rectangular shape	-	t	-
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
width	Width (um)	-	1	-
height	Height (um)	-	1	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1



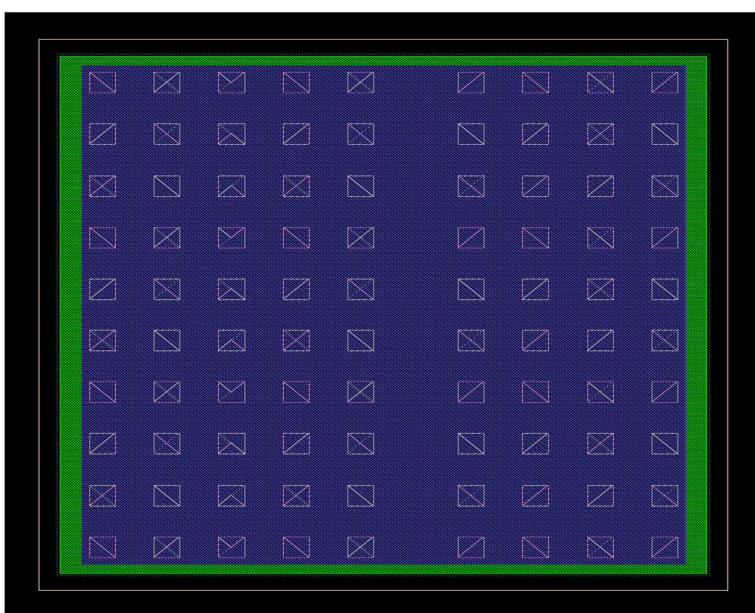


Symbol View:



Terminals order: p, n

Layout View:





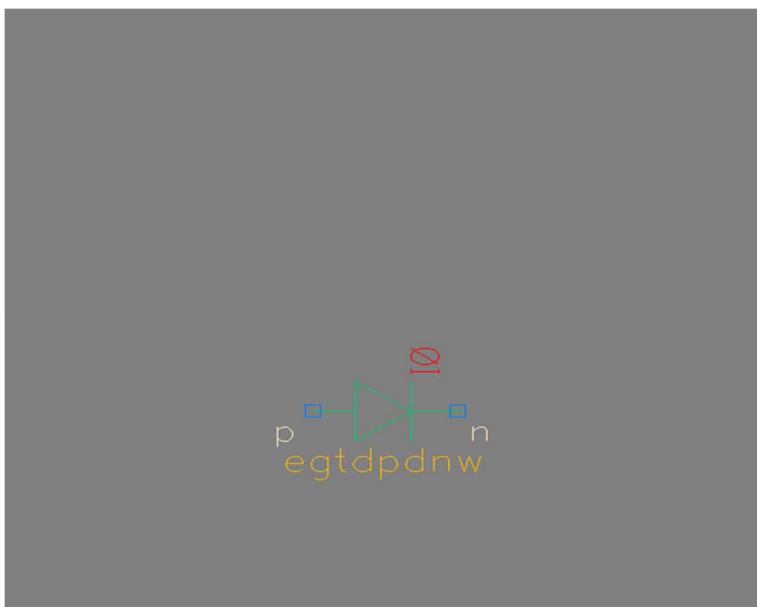
Device: egtpdnw

Parameter	Prompt	Units	Default	Range
DFM_PCell	Robust Rules	-	0	'0, 1
rectangle	Rectangular shape	-	t	-
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
width	Width (um)	-	1	-
height	Height (um)	-	1	-
Extended_EG	EG Extensions	-	-	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1



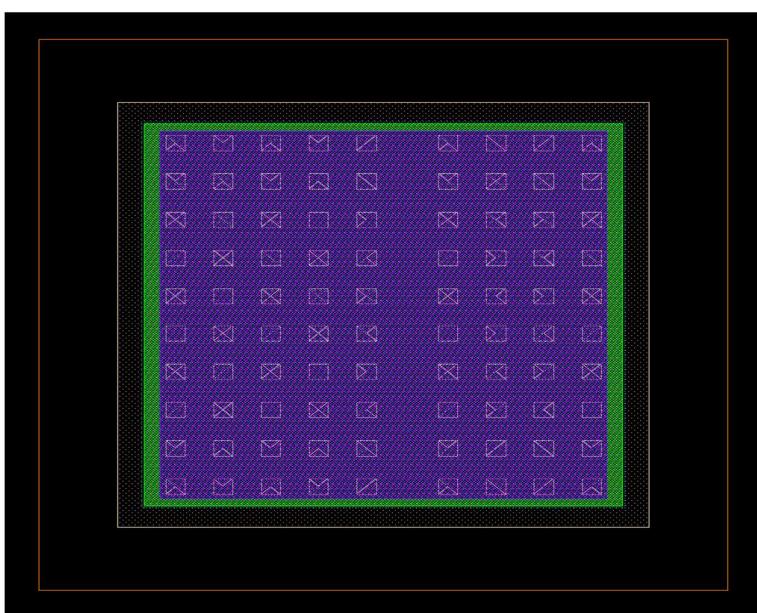


Symbol View:



Terminals order: p, n

Layout View:





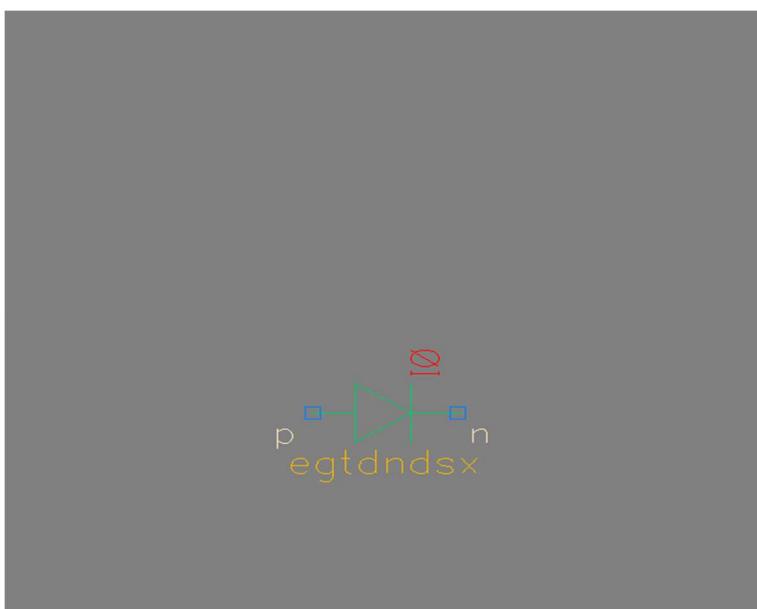
Device: egtdndsx

Parameter	Prompt	Units	Default	Range
DFM_PCell	Robust Rules	-	0	'0, 1
rectangle	Rectangular shape	-	t	-
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
width	Width (um)	-	1	-
height	Height (um)	-	1	-
Extended_EG	EG Extensions	-	-	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1



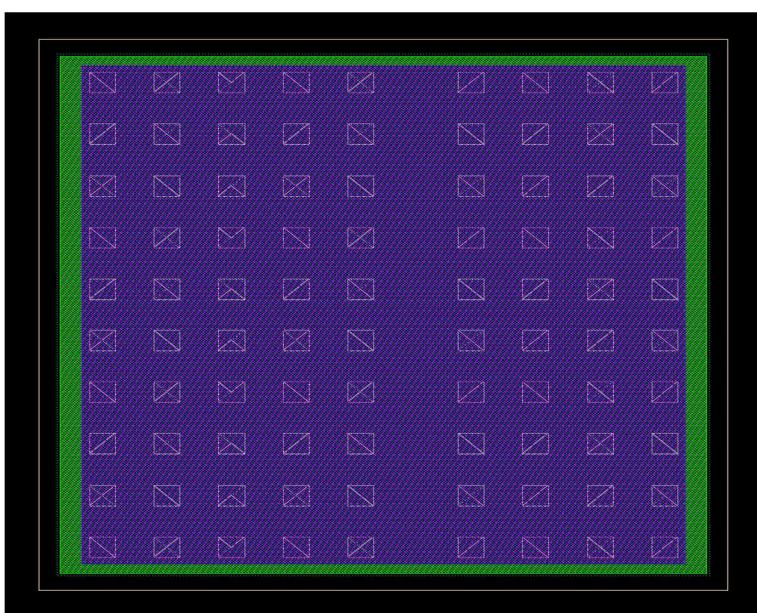


Symbol View:



Terminals order: p, n

Layout View:





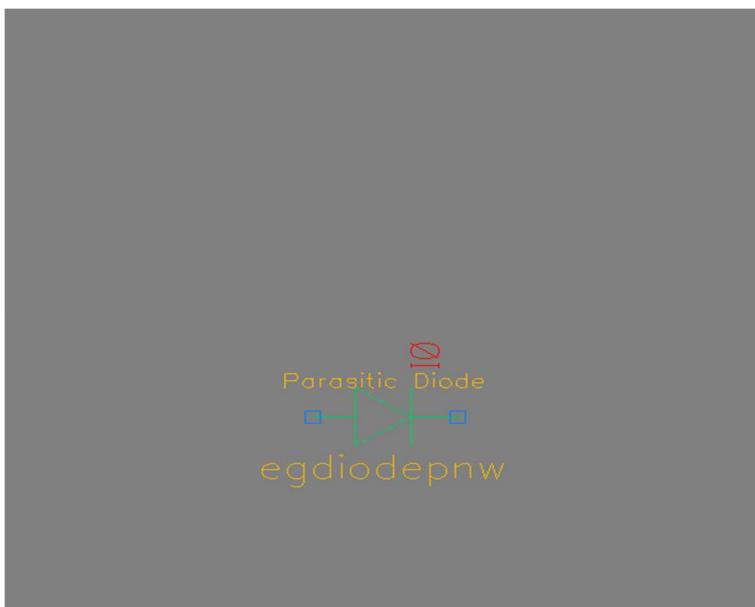
Device: egdiodepnw

Parameter	Prompt	Units	Default	Range
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1





Symbol View:



Terminals order: p, n

Layout View:

NO VIEW AVAILABLE





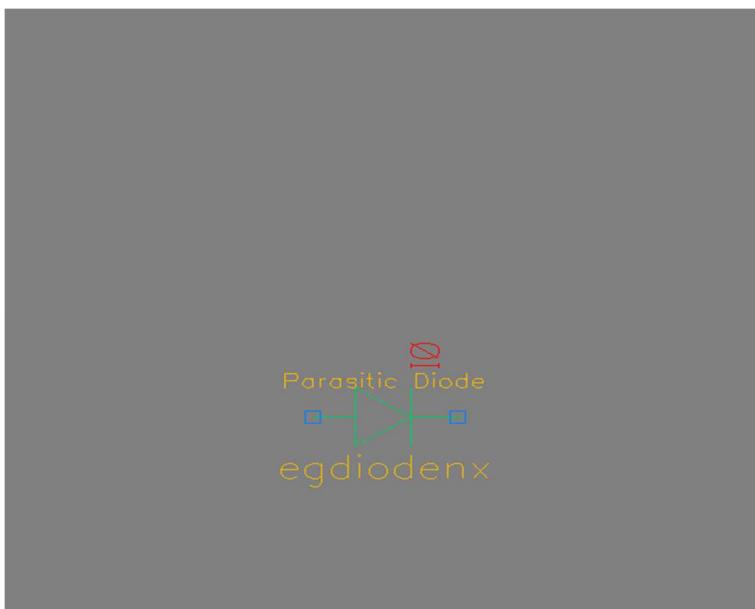
Device: egdiodenx

Parameter	Prompt	Units	Default	Range
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1





Symbol View:



Terminals order: p, n

Layout View:

NO VIEW AVAILABLE





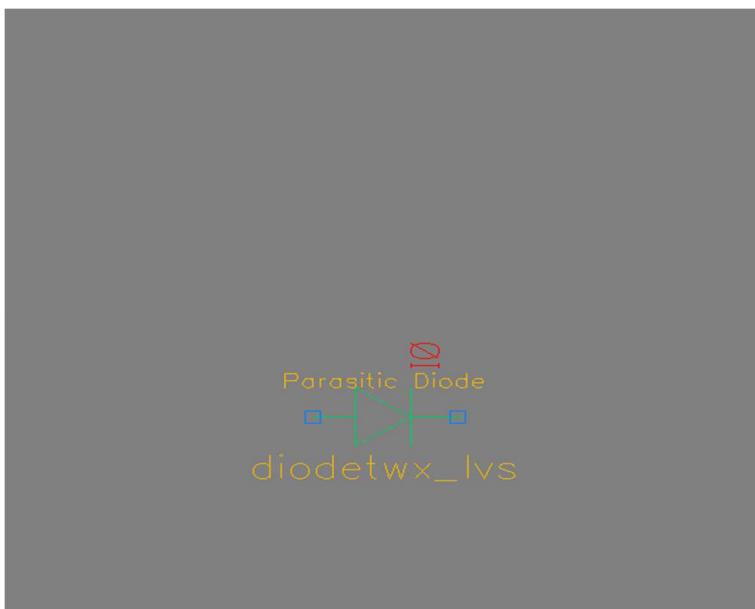
Device: diodetwx_lvs

Parameter	Prompt	Units	Default	Range
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1





Symbol View:



Terminals order: p, n

Layout View:

NO VIEW AVAILABLE





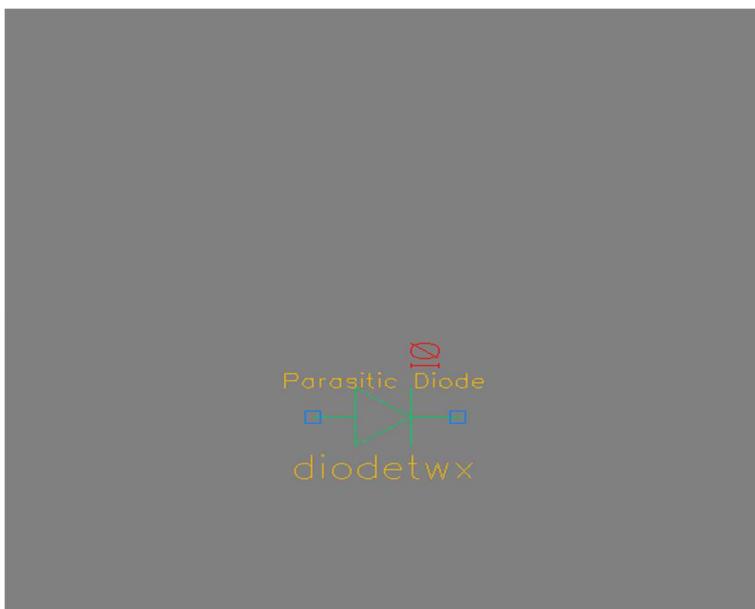
Device: diodetwx

Parameter	Prompt	Units	Default	Range
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1





Symbol View:



Terminals order: p, n

Layout View:

NO VIEW AVAILABLE





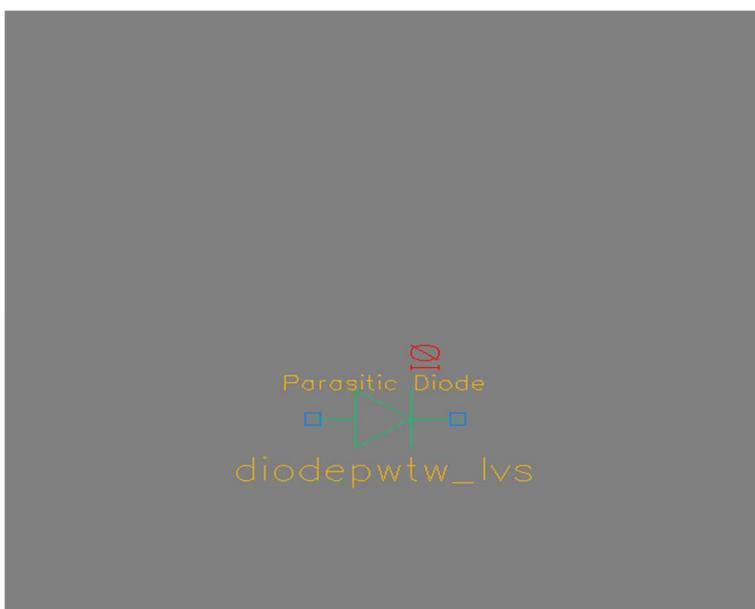
Device: diodepwtw_lvs

Parameter	Prompt	Units	Default	Range
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1





Symbol View:



Terminals order: p, n

Layout View:

NO VIEW AVAILABLE





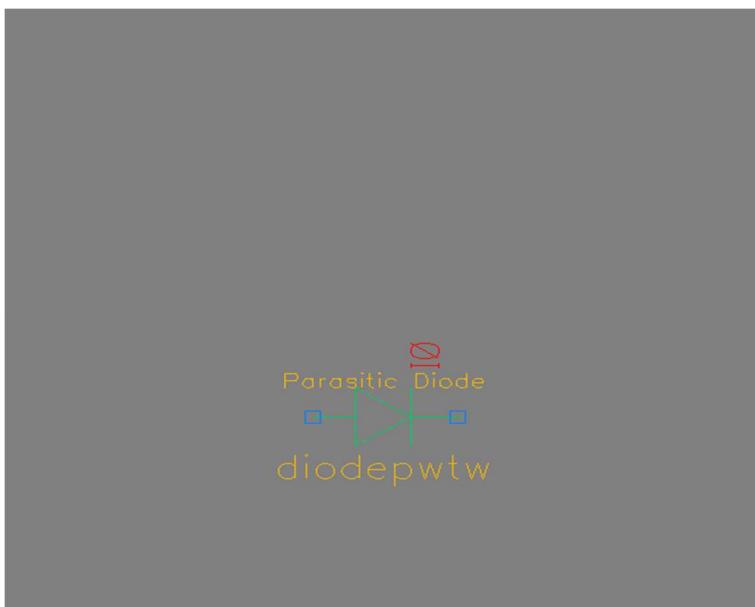
Device: diodepwtw

Parameter	Prompt	Units	Default	Range
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1





Symbol View:



Terminals order: p, n

Layout View:

NO VIEW AVAILABLE





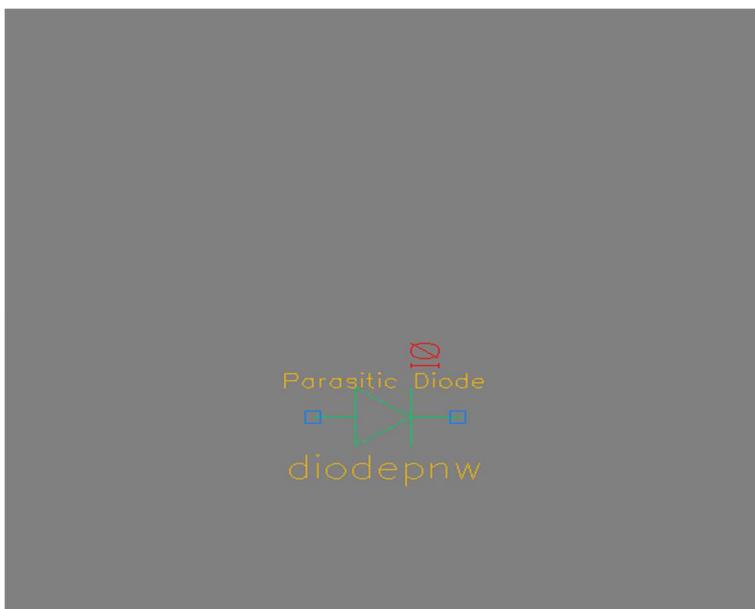
Device: diodepnw

Parameter	Prompt	Units	Default	Range
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1





Symbol View:



Terminals order: p, n

Layout View:

NO VIEW AVAILABLE





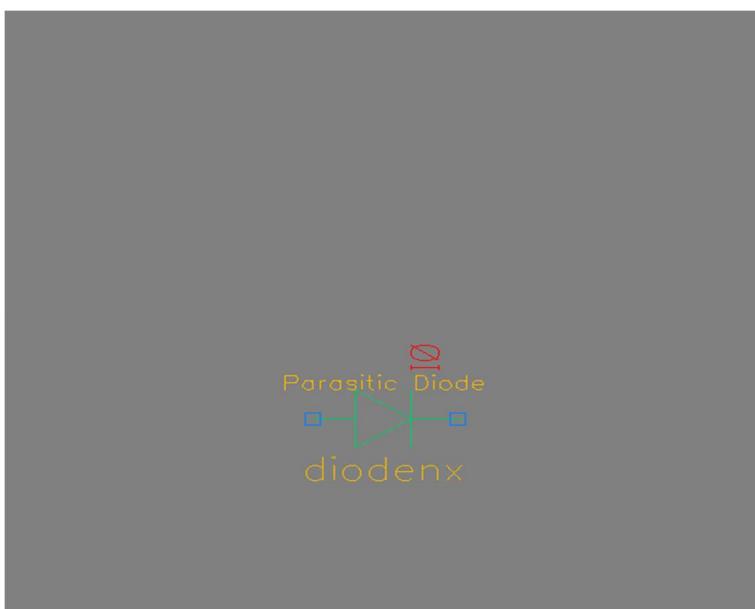
Device: diodenx

Parameter	Prompt	Units	Default	Range
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1





Symbol View:



Terminals order: p, n

Layout View:

NO VIEW AVAILABLE





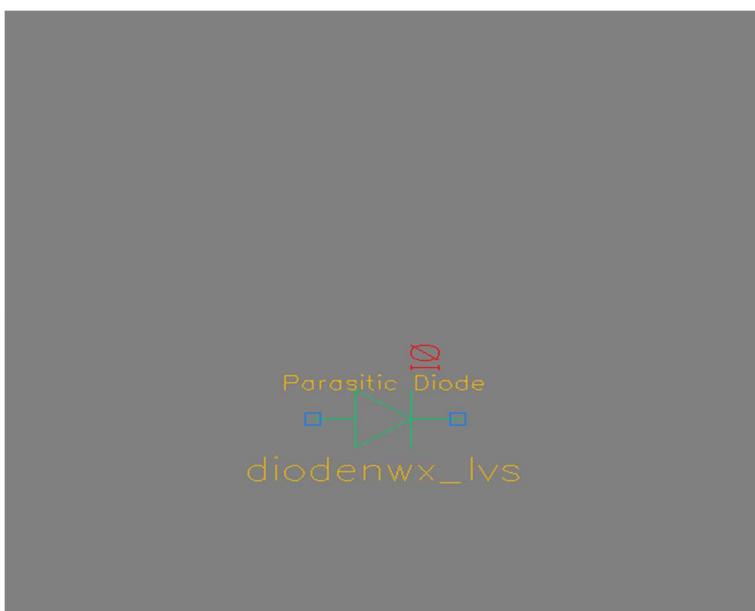
Device: diodenwx_lvs

Parameter	Prompt	Units	Default	Range
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1





Symbol View:



Terminals order: p, n

Layout View:

NO VIEW AVAILABLE





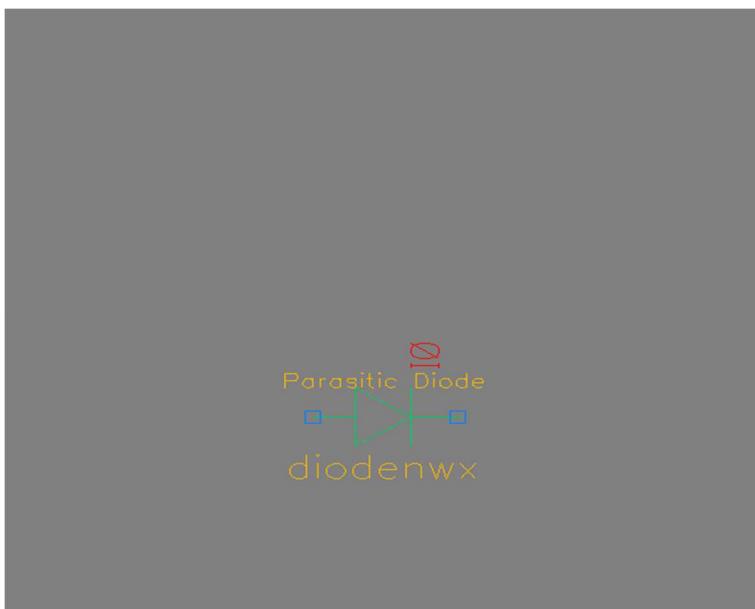
Device: diodenwx

Parameter	Prompt	Units	Default	Range
area	Area	m	1p	-
perimeter	Perimeter	m	4u	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1





Symbol View:



Terminals order: p, n

Layout View:

NO VIEW AVAILABLE





Device Category: ESD (in library cmos32lp)

Device Type	Cells Names In Device Library
Poly bounded DW P+/NW ESD Diode - EG version	esdvpnp_eg
Poly bounded DW N+/PW ESD Diode - EG version	esdnndsx_eg
RVT NFET after triggering	esdnfet
N+/PW Diode/Vertical NPN Bipolar (TW)	esdvpnp, esdvnpn
EG NFET after triggering	esdegnfet
Poly bounded TW N+/PW ESD Diode - EG version	esdvnpn_eg
N+/PW Diode (DW) (ESD N+ Junction)	esdnndsx
Silicide-Block N-Diffusion Resistor on SOI	sblkndres_fdsoi
Silicide-Block P-Diffusion Resistor on SOI	sblkpdres_fdsoi

Table: ESD device types and cells

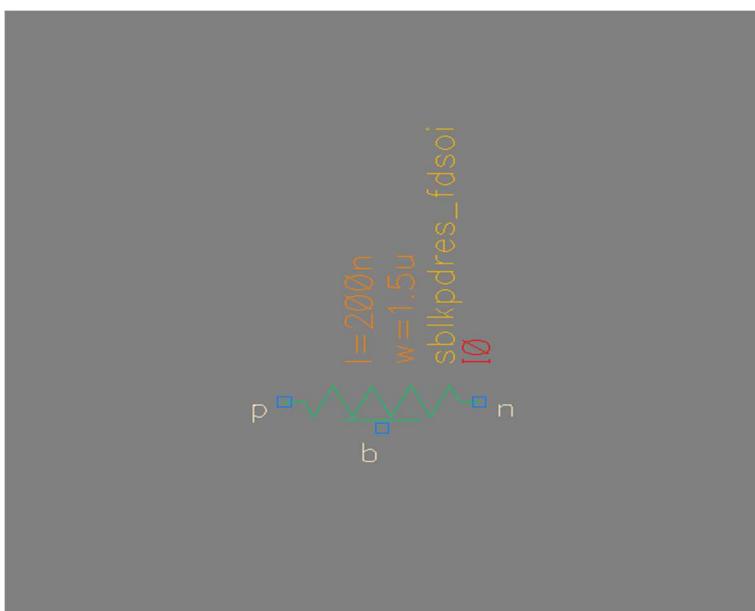
Device: sblkpdres_fdsoi

Parameter	Prompt	Units	Default	Range
w	Total Gate Width	m	1.5u	-
l	Gate Length	m	200.0n	-
ser	Series Stripes	-	1	-
par	Parallel Stripes	-	1	-
soa	Safe Operating Area	-	1	'0, 1
r	Resistance	-	-	-
rsx	Substrate Resistance	-	-	-
sh	Self Heating	-	-	-
mismatch	mismatch	-	1	'0, 1
dr_mdev	dr_mdev	-	-	-





Symbol View:



Terminals order: p, n, b

Layout View:

NO VIEW AVAILABLE





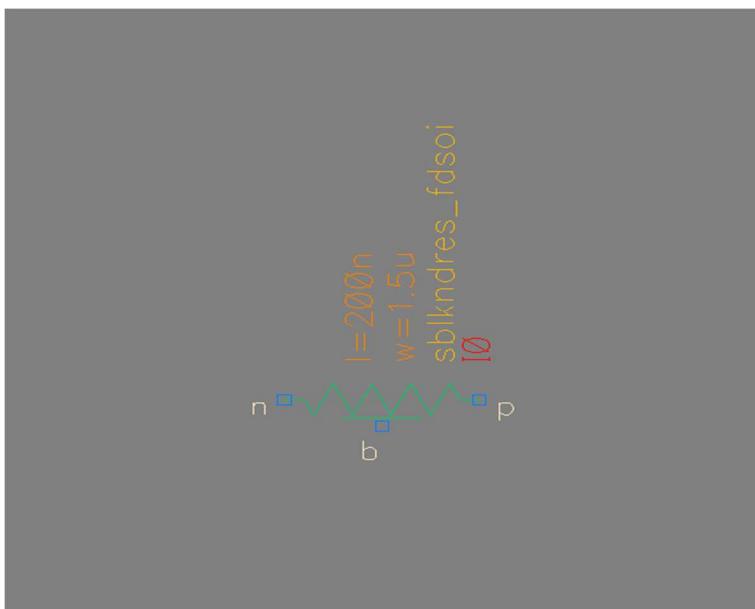
Device: sblkndres_fdsoi

Parameter	Prompt	Units	Default	Range
w	Total Gate Width	m	1.5u	-
l	Gate Length	m	200.0n	-
ser	Series Stripes	-	1	-
par	Parallel Stripes	-	1	-
subres	Substrate Resistance	Ohms	0	-
soa	Safe Operating Area	-	1	'0, 1
r	Resistance	-	-	-
rsx	Substrate Resistance	-	-	-
sh	Self Heating	-	-	-
mismatch	mismatch	-	1	'0, 1
dr_mdev	dr_mdev	-	-	-





Symbol View:



Terminals order: p, n, b

Layout View:

NO VIEW AVAILABLE





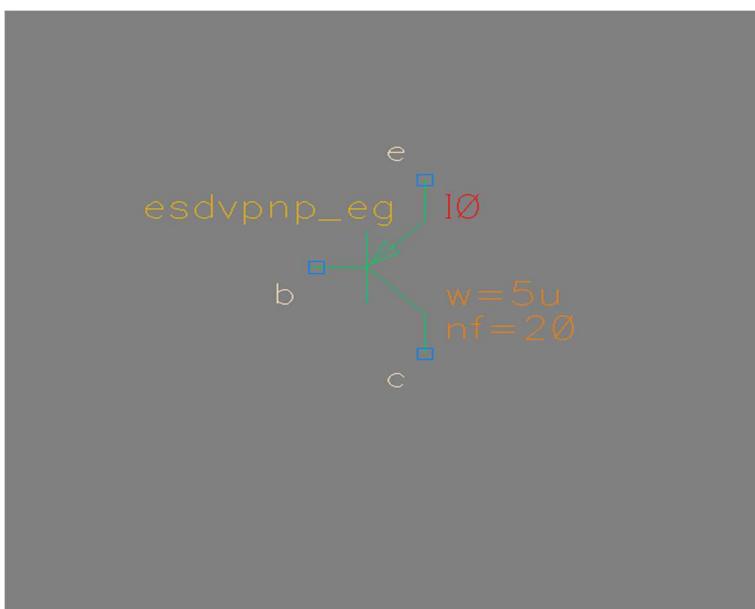
Device: esdvpnp_eg

Parameter	Prompt	Units	Default	Range
w	Poly Finger Width	m	5u	-
l	Poly Finger Length (sac)	m	160.0n	-
nf	Number of Poly Fingers	-	20	-
auto_area_perim	auto_area_perim	-	auto	'auto, user
area	Area	m	7.5p	-
perimeter	Perimeter	m	10.3u	-
areab	Base Area	m	38.92p	-
perimeterb	Base Perimeter	m	25.1u	-
area_disp	Area	-	-	-
perimeter_disp	Perimeter	-	-	-
areab_disp	Base Area	-	-	-
perimeterb_disp	Base Perimeter	-	-	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rwire	Wire Resistance	-	-1	-
rsx	Substrate Resistance	-	0	-
spgr	Spacing guardring	-	0	-
bkeuser	bkuser	-	0	-
soa	Safe Operating Area	-	1	'0, 1



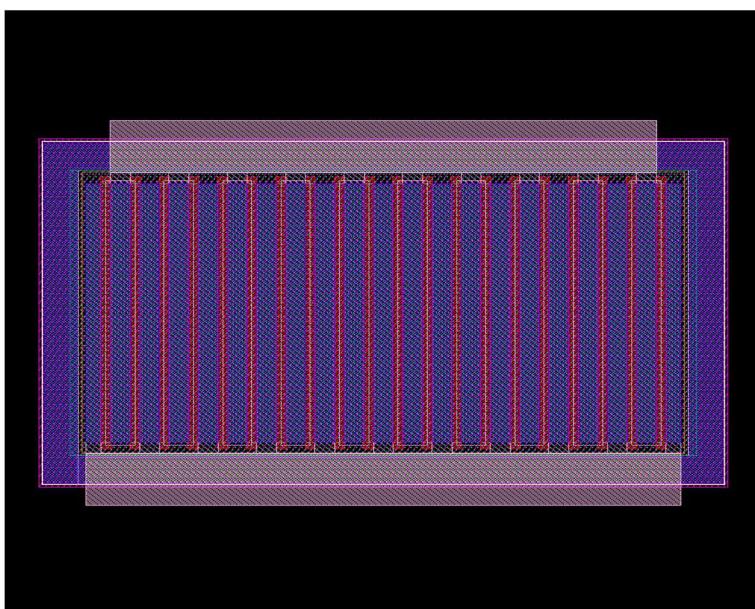


Symbol View:



Terminals order: c, b, e

Layout View:





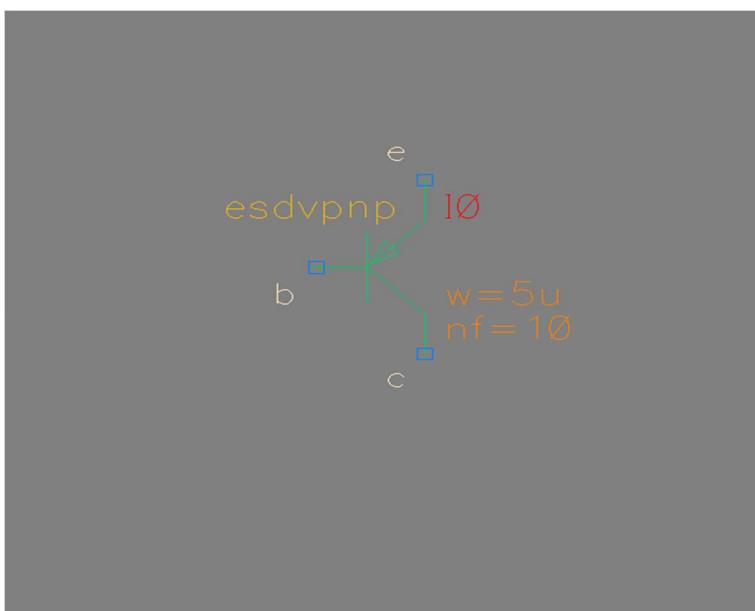
Device: esdvpnp

Parameter	Prompt	Units	Default	Range
w	Emitter Width	m	5u	-
l	Emitter Length	m	122n	-
nf	Number of Emitters	-	10	-
auto_area_perim	auto_area_perim	-	auto	'auto, user
area	Area	m	6.1p	-
perimeter	Perimeter	m	102.44u	-
areab	Base Area	m	26.667p	-
perimeterb	Base Perimeter	m	20.724u	-
area_disp	Area	-	-	-
perimeter_disp	Perimeter	-	-	-
areab_disp	Base Area	-	-	-
perimeterb_disp	Base Perimeter	-	-	-
rwire	Wiring Resistance	Ohms	-1	-
rsx	Substrate Resistance	Ohms	0	-
sac	P diff RX to N diff RX spacing	m	80.00n	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
spgr	Spacing guardring	-	0	-
bkeuser	bkuser	-	0	-
soa	Safe Operating Area	-	1	'0, 1



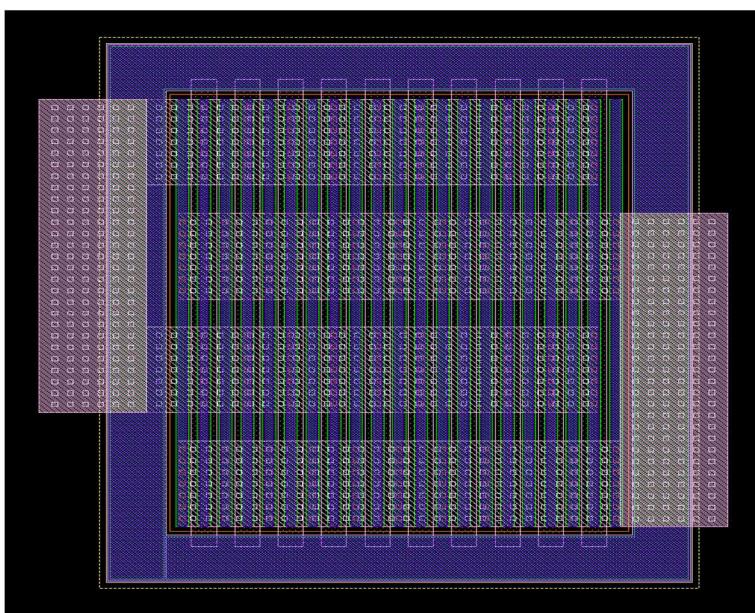


Symbol View:



Terminals order: c, b, e

Layout View:





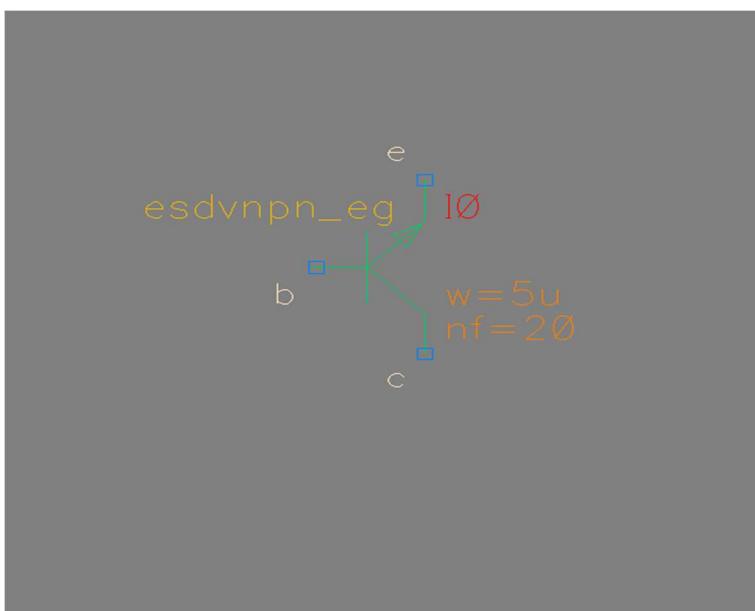
Device: esdvnpn_eg

Parameter	Prompt	Units	Default	Range
w	Poly Finger Width	m	5u	-
l	Poly Finger Length (sac)	m	160.0n	-
nf	Number of Poly Fingers	-	20	-
auto_area_perim	auto_area_perim	-	auto	'auto, user
area	Area	m	7.5p	-
perimeter	Perimeter	m	103.0u	-
areab	Base Area	m	38.92p	-
perimeterb	Base Perimeter	m	25.1p	-
area_disp	Area	-	-	-
perimeter_disp	Perimeter	-	-	-
areab_disp	Base Area	-	-	-
perimeterb_disp	Base Perimeter	-	-	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rwire	Wire Resistance	-	-1	-
rnb	Substrate Resistance	-	0	-
spgr	Spacing Guardring	-	0	-
bkeuser	bkeuser	-	0	-
soa	Safe Operating Area	-	1	'0, 1



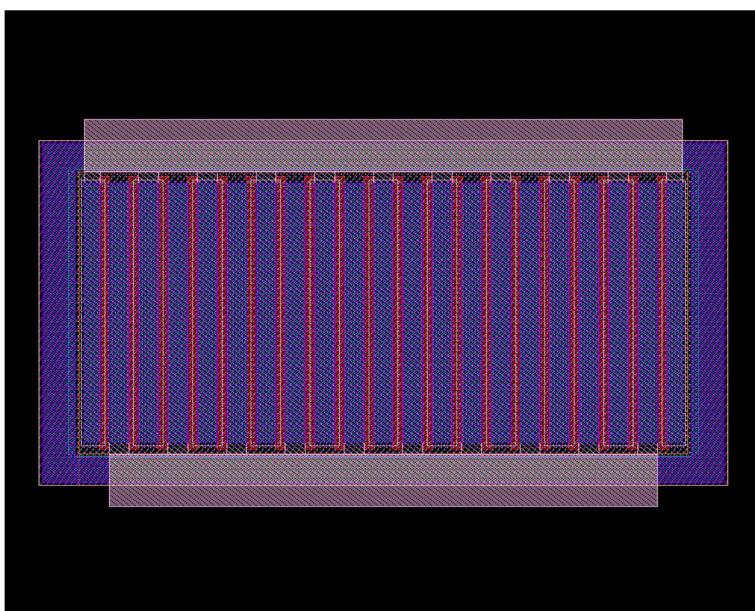


Symbol View:



Terminals order: c, b, e

Layout View:





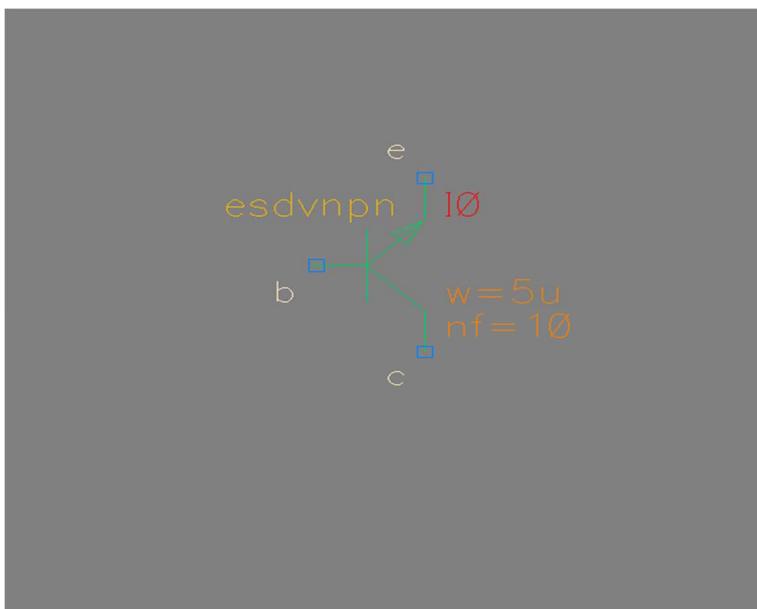
Device: esdvnpn

Parameter	Prompt	Units	Default	Range
w	Emitter Width	m	5u	-
l	Emitter Length	m	122n	-
nf	Number of Emitters	-	10	-
auto_area_perim	auto_area_perim	-	auto	'auto, user
area	Area	m	6.1p	-
perimeter	Perimeter	m	102.44u	-
areab	Base Area	m	26.667p	-
perimeterb	Base Perimeter	m	20.724u	-
area_disp	Area	-	-	-
perimeter_disp	Perimeter	-	-	-
areab_disp	Base Area	-	-	-
perimeterb_disp	Base Perimeter	-	-	-
rwire	Wiring Resistance	Ohms	-1	-
rnb	Nband Resistance	Ohms	0	-
sac	P diff RX to N diff RX spacing	m	80.00n	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
spgr	Spacing Guardring	-	0	-
bkeuser	bkeuser	-	0	-
soa	Safe Operating Area	-	1	'0, 1



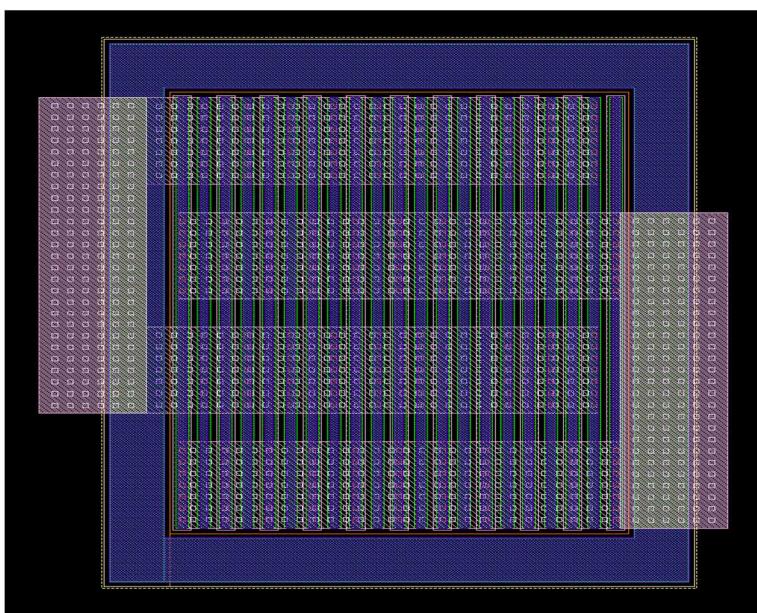


Symbol View:



Terminals order: c, b, e

Layout View:





Device: esdnfet

Parameter	Prompt	Units	Default	Range
w	Total Gate Width	m	286.0u	-
l	Gate Length	m	48.000n	-
ldop	Drain SBLK Length	m	200.0n	-
lsop	Source SBLK Length	m	200.0n	-
wf	Gate Finger Width	m	7.15u	-
n	number of gate fingers	-	40	-
gateSplitStripes	Gate Split Y	-	1	-
guardRing	Guard Ring	-	three	'none, one, two, three
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
pd	pd	m	0	-
ps	ps	m	0	-
ad_disp	Total Drain Area	m	11.44m	-
as_disp	Total Source Area	m	10.868m	-
pd_disp	Total Drain Periphery	m	80.01	-
ps_disp	Total Source Periphery	m	76.01	-
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	iPar("lsop") + iPar("geo_xdef_contact_src")	-
sb	STI Compression (sb)	m	iPar("ldop") + iPar("geo_xdef_contact_drn")	-
sd	STI Compression (sd)	m	0	-
plorient	plorient	-	1	'1, 2



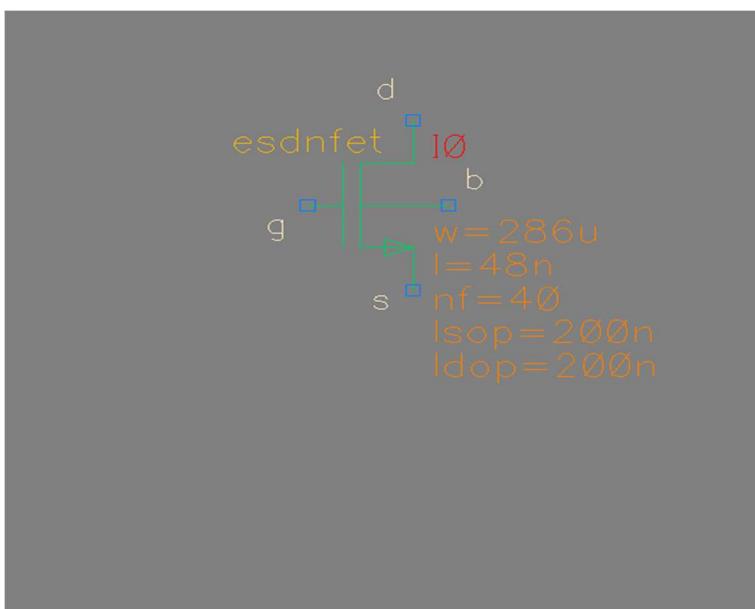


Parameter	Prompt	Units	Default	Range
ngcon	Number of Gate Contacts	-	1	'1, 2
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1



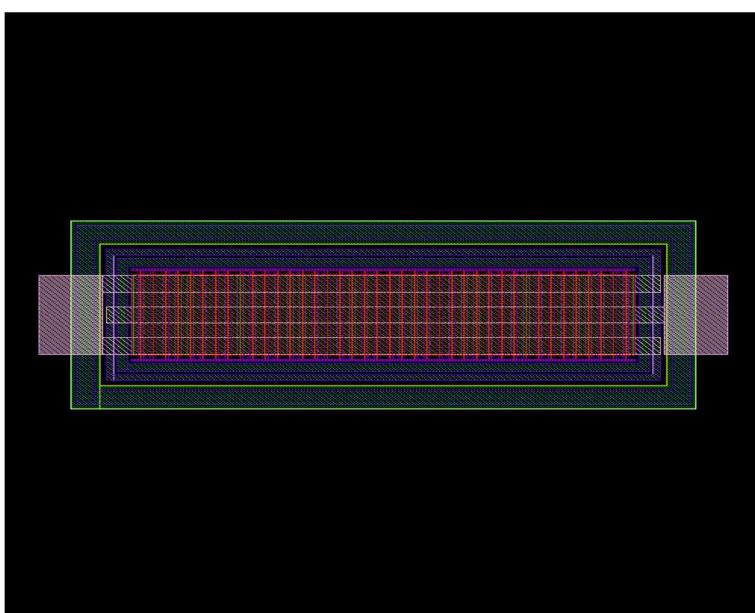


Symbol View:



Terminals order: d, g, s, b

Layout View:





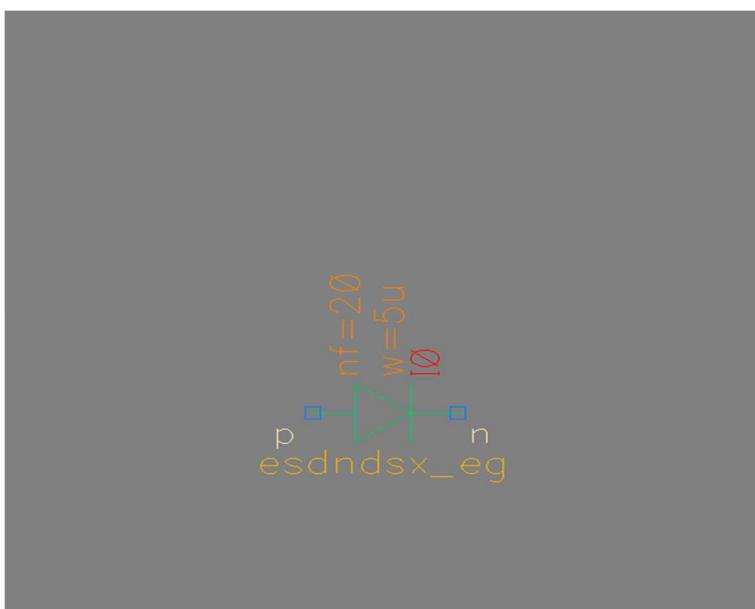
Device: esdndsx_eg

Parameter	Prompt	Units	Default	Range
rectangle	Rectangular shape	-	t	-
w	Poly Finger Width	m	5u	-
l	Poly Finger Length (sac)	m	160.0n	-
nf	Number of Poly Fingers	-	20	-
auto_area_perim	auto_area_perim	-	auto	'auto, user
area	Area	m	7.5p	-
perimeter	Perimeter	m	103.0u	-
area_disp	Area	-	-	-
perimeter_disp	Perimeter	-	-	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rwire	Wire Resistance	-	-1	-
bkeuser	bkeuser	-	0	-
soa	Safe Operating Area	-	1	'0, 1



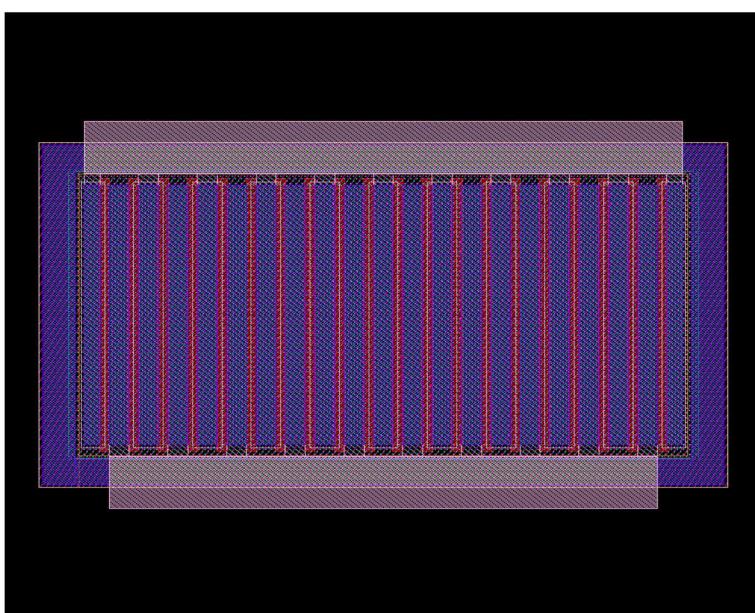


Symbol View:



Terminals order: p, n

Layout View:





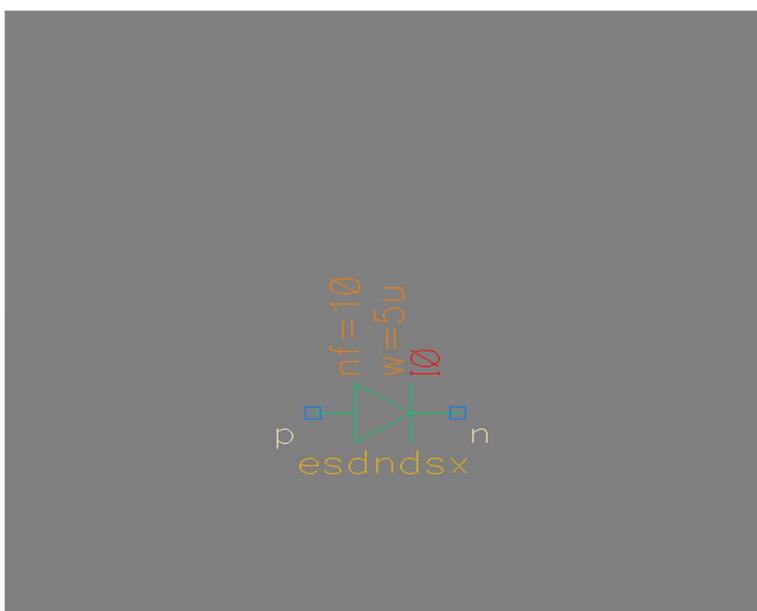
Device: esdnndsx

Parameter	Prompt	Units	Default	Range
rectangle	Rectangular shape	-	t	-
w	Diffusion Width	m	5u	-
l	Diffusion Length	m	122n	-
nf	Number of Fingers	-	10	-
auto_area_perim	auto_area_perim	-	auto	'auto, user
area	Area	m	6.1p	-
perimeter	Perimeter	m	102.44u	-
area_disp	Area	-	-	-
perimeter_disp	Perimeter	-	-	-
rwire	Wiring Resistance	Ohms	-1	-
sac	P diff RX to N diff RX spacing	m	80.00n	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
bkeuser	bkeuser	-	0	-
soa	Safe Operating Area	-	1	'0, 1



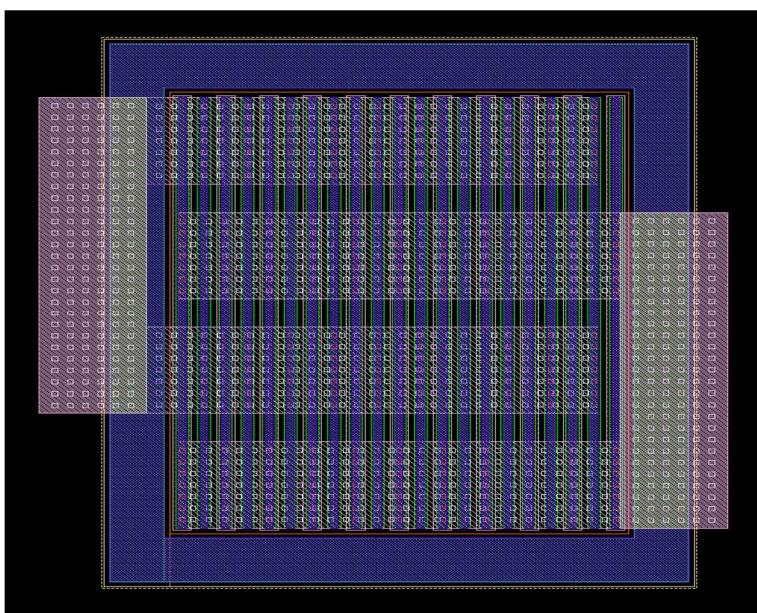


Symbol View:



Terminals order: p, n

Layout View:





Device: esdegnfet

Parameter	Prompt	Units	Default	Range
w	Total Gate Width	m	286.0u	-
l	Gate Length	m	150.00n	-
ldop	Drain SBLK Length	m	200.0n	-
lsop	Source SBLK Length	m	200.0n	-
wf	Gate Finger Width	m	7.15u	-
n	number of gate fingers	-	40	-
gateSplitStripes	Gate Split Y	-	1	-
guardRing	Guard Ring	-	three	'none, one, two, three
trise	Temperature Deviation	-	0	-
sizedup	Sized Up	-	0	'0, 1
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
pd	pd	m	0	-
ps	ps	m	0	-
ad_disp	Total Drain Area	m	11.44m	-
as_disp	Total Source Area	m	10.868m	-
pd_disp	Total Drain Periphery	m	80.01	-
ps_disp	Total Source Periphery	m	76.01	-
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	iPar("lsop") + iPar("geo_xdef_contact_src")	-
sb	STI Compression (sb)	m	iPar("ldop") + iPar("geo_xdef_contact_drn")	-



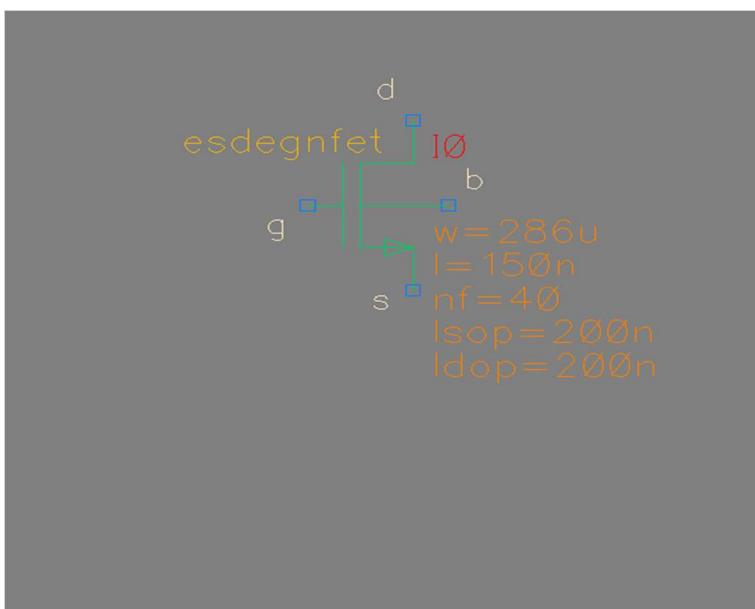


Parameter	Prompt	Units	Default	Range
sd	STI Compression (sd)	m	0	-
plorient	plorient	-	1	'1, 2
ngcon	Number of Gate Contacts	-	1	'1, 2
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
soa	Safe Operating Area	-	1	'0, 1



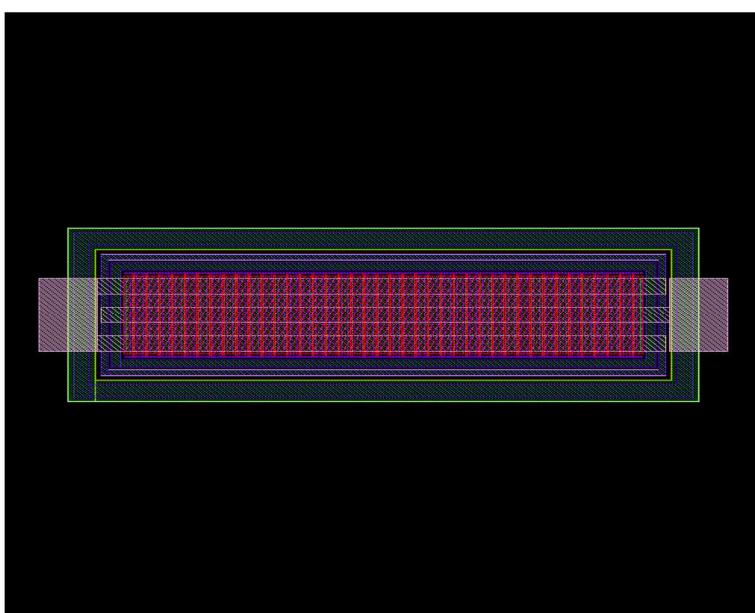


Symbol View:



Terminals order: d, g, s, b

Layout View:





Device Category: ESD_Hierarchical_Cells (in library cmos32lp)

Device Type	Cells Names In Device Library
ESD Low-Vt PFET	esdlvtpfet_fdsoi
ESD 1.8V IO NFET 28A	esdegvnfet_fdsoi, esdegvlvtpfet_fdsoi, esdegvlvtnfet_fdsoi, esdegnfet_fdsoi, esdeglvtnfet_fdsoi
ESD Low-Vt NFET	esdlvtnfet_fdsoi
ESD Regular-Vt NFET	esdnfet_fdsoi
ESD Regular-Vt PFET	esdpfet_fdsoi
ESD 1.8V IO PFET 28A	esdegvpfet_fdsoi, esdegpfet_fdsoi, esdeglvtpfet_fdsoi

Table: ESD_HIERARCHICAL_CELLS device types and cells

Device: esdpfet_fdsoi

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	80n	-
wf	Gate Finger Width	m	80n	-
l	Gate Length	m	48n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-





Parameter	Prompt	Units	Default	Range
SourceContColum n	SourceContColum n	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopC hoices	Source Metal Top	-	M1	'M1, M1-M2, M1- M3, M1-M4
DrainMetalTopCh oices	Drain Metal Top	-	M1	'M1, M1-M2, M1- M3, M1-M4
trise	Temperature Deviation	-	0	-
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig	-	0	'0, 1



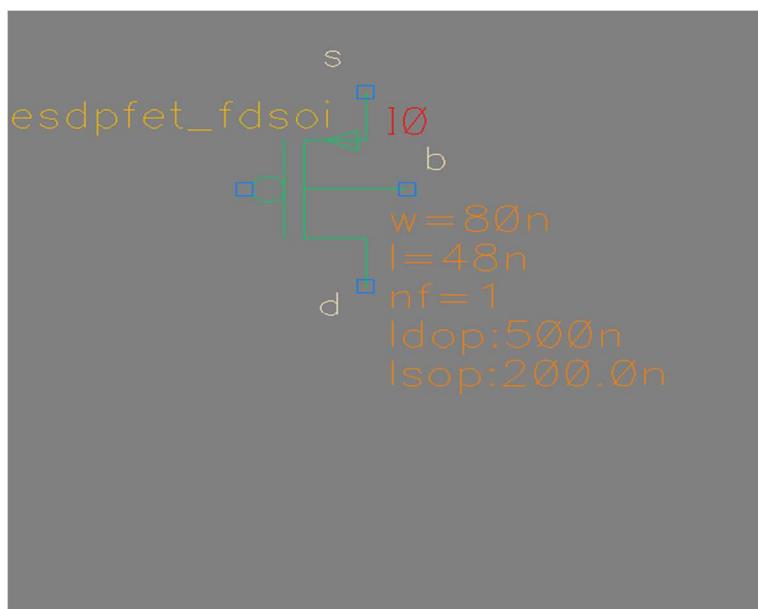


Parameter	Prompt	Units	Default	Range
	parameters			
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

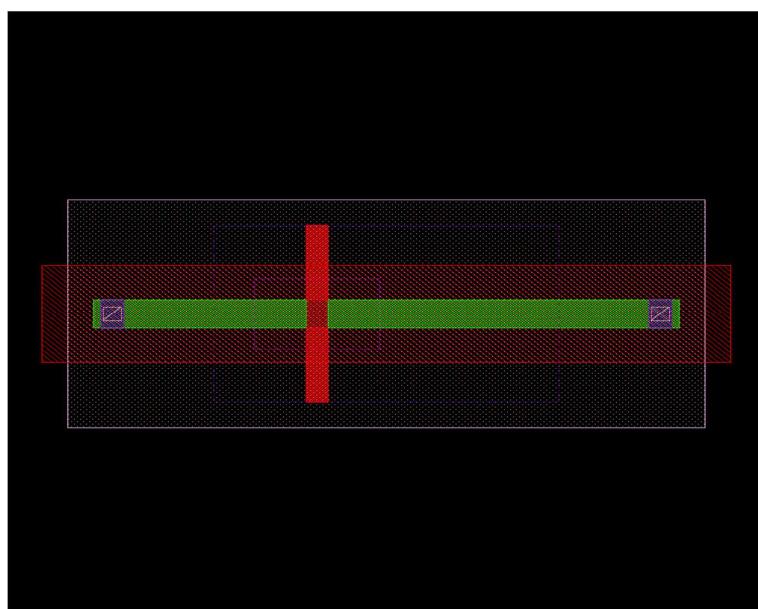




Symbol View:



Layout View:





Device: esdnfet_fdsOI

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	80n	-
wf	Gate Finger Width	m	80n	-
l	Gate Length	m	48n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-
SourceContColumn	SourceContColumn	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopChoices	Source Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
DrainMetalTopChoices	Drain Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
trise	Temperature Deviation	-	0	-
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-





Parameter	Prompt	Units	Default	Range
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig parameters	-	0	'0, 1
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

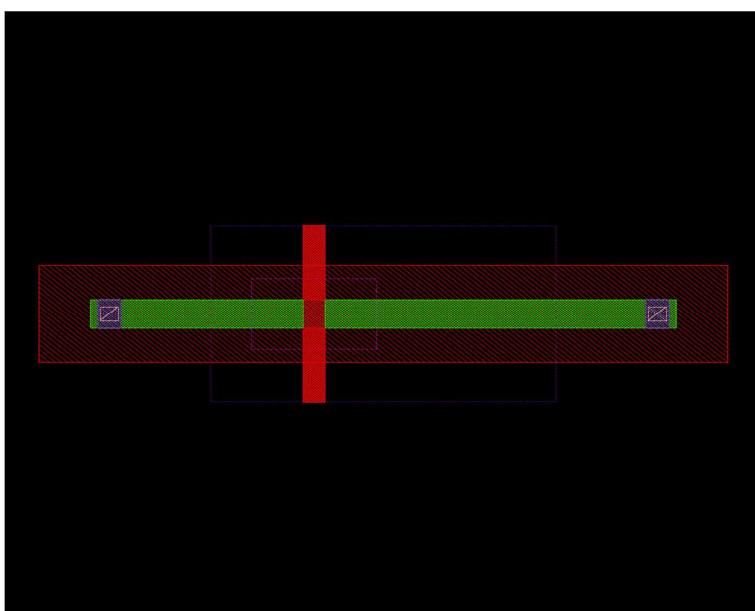




Symbol View:



Layout View:





Device: esdlvtpfet_fdsoi

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	80n	-
wf	Gate Finger Width	m	80n	-
l	Gate Length	m	48n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-
SourceContColumn	SourceContColumn	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopChoices	Source Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
DrainMetalTopChoices	Drain Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
trise	Temperature Deviation	-	0	-
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-



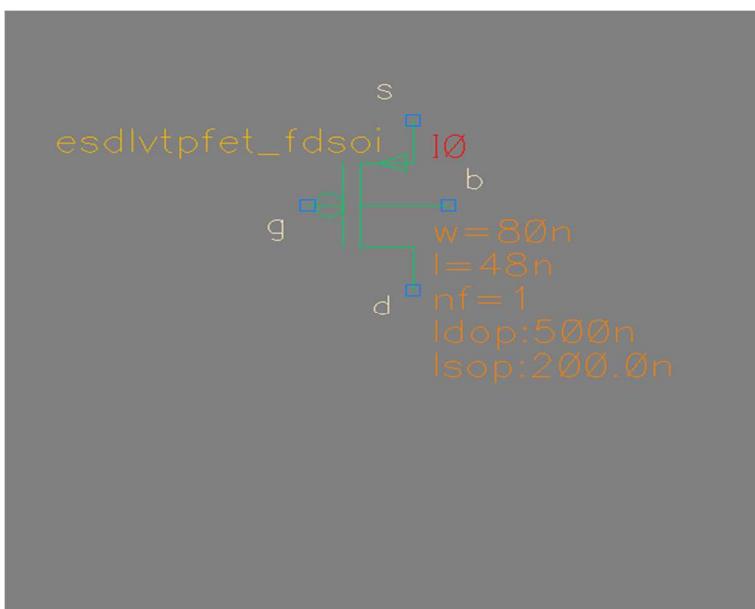


Parameter	Prompt	Units	Default	Range
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig parameters	-	0	'0, 1
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

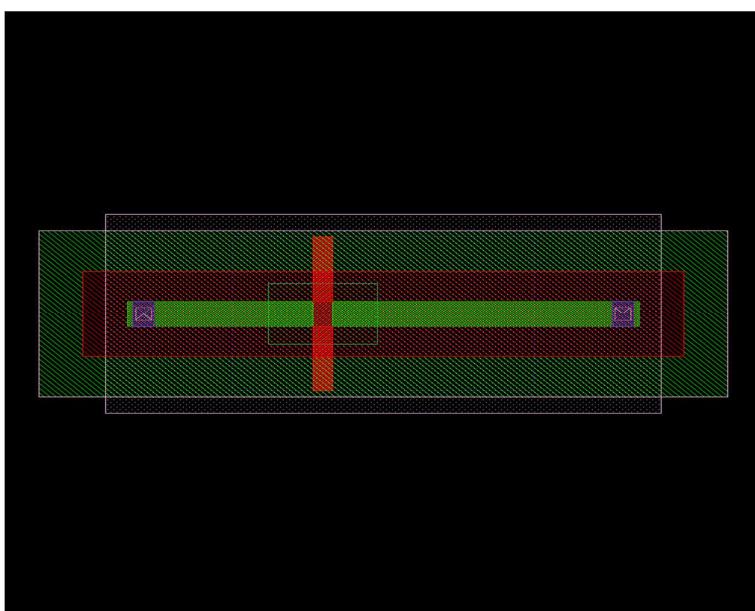




Symbol View:



Layout View:





Device: esdlvtnfet_fdsoi

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	80n	-
wf	Gate Finger Width	m	80n	-
l	Gate Length	m	48n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-
SourceContColumn	SourceContColumn	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopChoices	Source Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
DrainMetalTopChoices	Drain Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
trise	Temperature Deviation	-	0	-
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-





Parameter	Prompt	Units	Default	Range
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig parameters	-	0	'0, 1
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

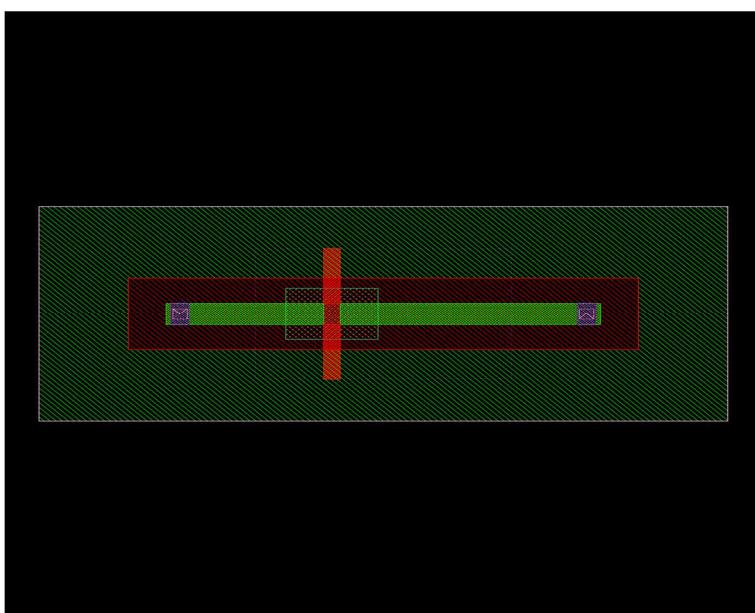




Symbol View:



Layout View:





Device: esdegvpfet_fdsoi

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	160n	-
wf	Gate Finger Width	m	160n	-
l	Gate Length	m	100n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-
SourceContColumn	SourceContColumn	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopChoices	Source Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
DrainMetalTopChoices	Drain Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
trise	Temperature Deviation	-	0	-
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-





Parameter	Prompt	Units	Default	Range
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig parameters	-	0	'0, 1
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

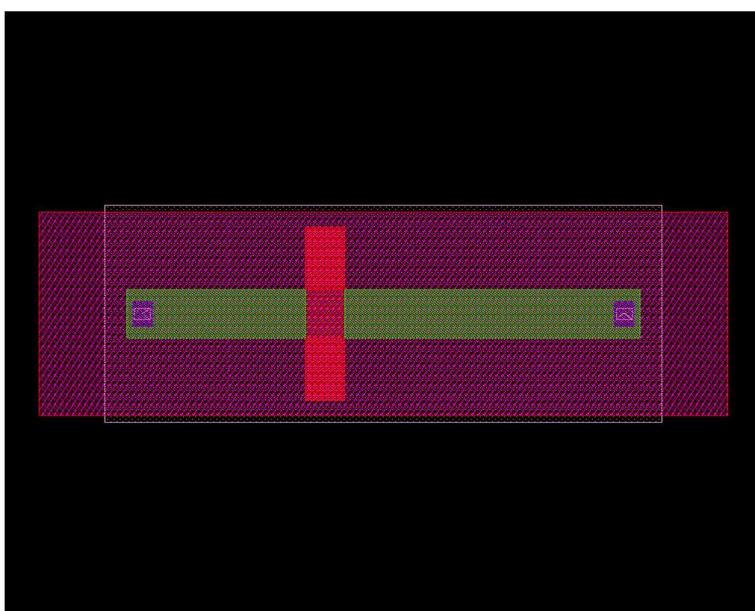




Symbol View:



Layout View:





Device: esdegvnfet_fdsoi

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	160n	-
wf	Gate Finger Width	m	160n	-
l	Gate Length	m	100n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-
SourceContColumn	SourceContColumn	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopChoices	Source Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
DrainMetalTopChoices	Drain Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
trise	Temperature Deviation	-	0	-
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-





Parameter	Prompt	Units	Default	Range
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig parameters	-	0	'0, 1
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

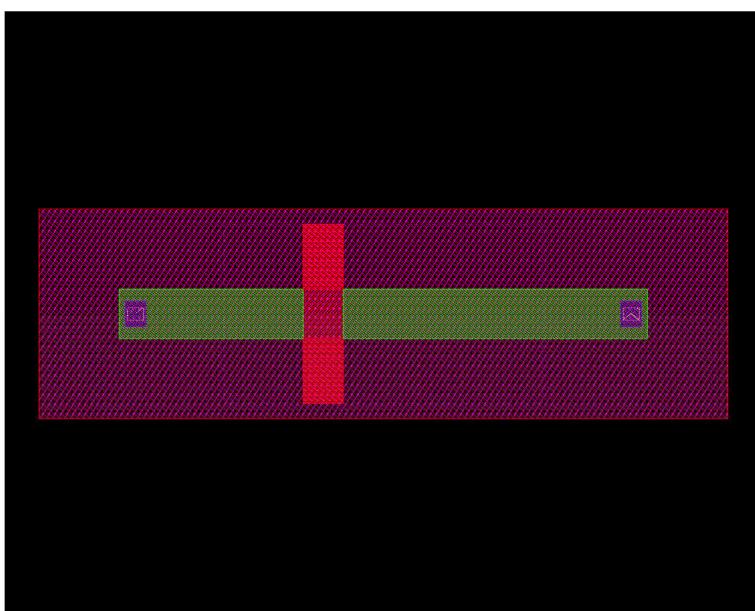




Symbol View:



Layout View:





Device: esdegvlvtpfet_fdsOI

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	160n	-
wf	Gate Finger Width	m	160n	-
l	Gate Length	m	100n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-
SourceContColumn	SourceContColumn	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopChoices	Source Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
DrainMetalTopChoices	Drain Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
trise	Temperature Deviation	-	0	-
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-



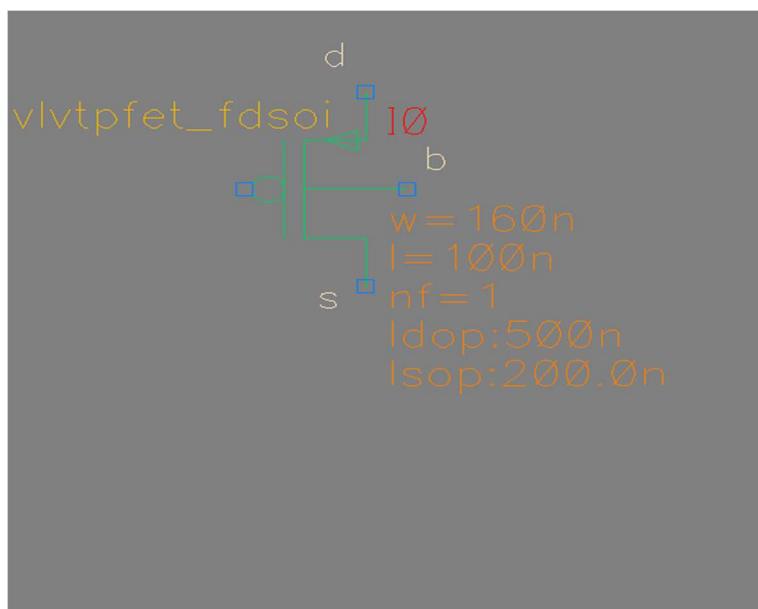


Parameter	Prompt	Units	Default	Range
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig parameters	-	0	'0, 1
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

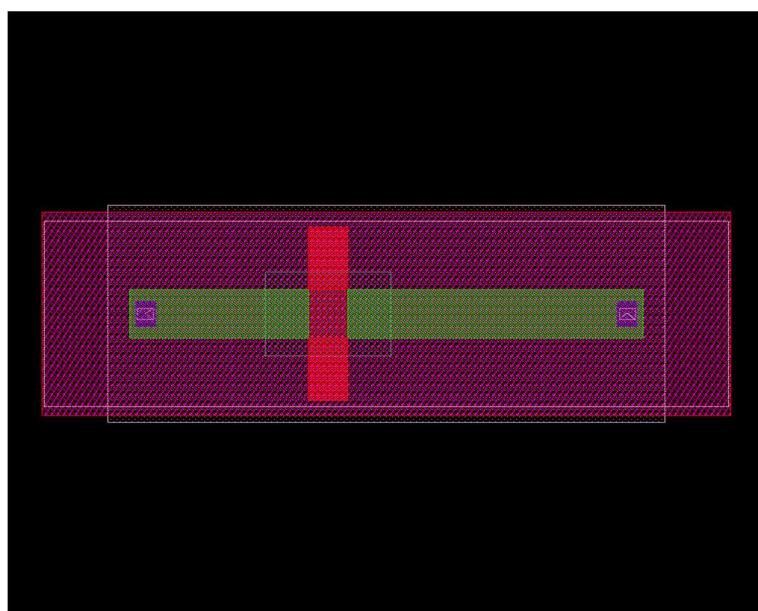




Symbol View:



Layout View:





Device: esdegvltnfet_fdsOI

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	160n	-
wf	Gate Finger Width	m	160n	-
l	Gate Length	m	100n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-
SourceContColumn	SourceContColumn	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopChoices	Source Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
DrainMetalTopChoices	Drain Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
trise	Temperature Deviation	-	0	-
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-





Parameter	Prompt	Units	Default	Range
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig parameters	-	0	'0, 1
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

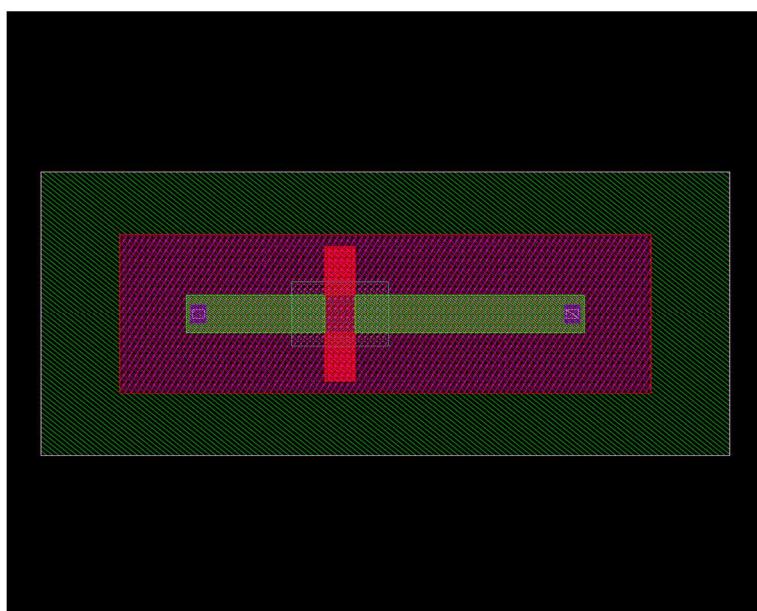




Symbol View:



Layout View:





Device: esdegpfet_fdsOI

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	160n	-
wf	Gate Finger Width	m	160n	-
l	Gate Length	m	150n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-
SourceContColumn	SourceContColumn	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopChoices	Source Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
DrainMetalTopChoices	Drain Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
trise	Temperature Deviation	-	0	-
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-



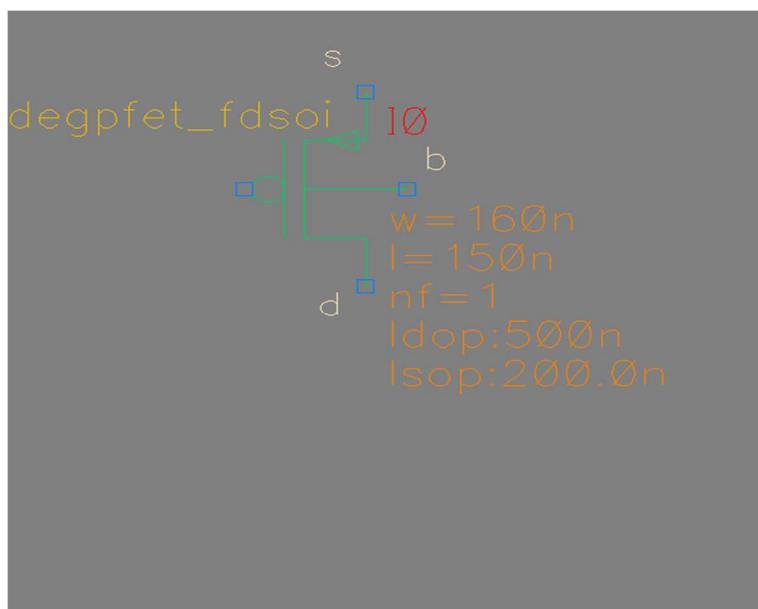


Parameter	Prompt	Units	Default	Range
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig parameters	-	0	'0, 1
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

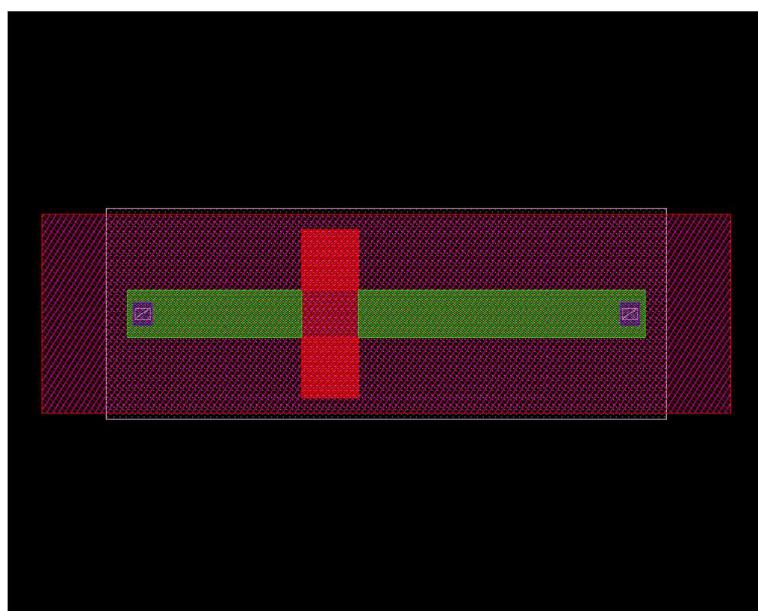




Symbol View:



Layout View:





Device: esdegnfet_fdsOI

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	160n	-
wf	Gate Finger Width	m	160n	-
l	Gate Length	m	160n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-
SourceContColumn	SourceContColumn	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopChoices	Source Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
DrainMetalTopChoices	Drain Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
trise	Temperature Deviation	-	0	-
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-





Parameter	Prompt	Units	Default	Range
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig parameters	-	0	'0, 1
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

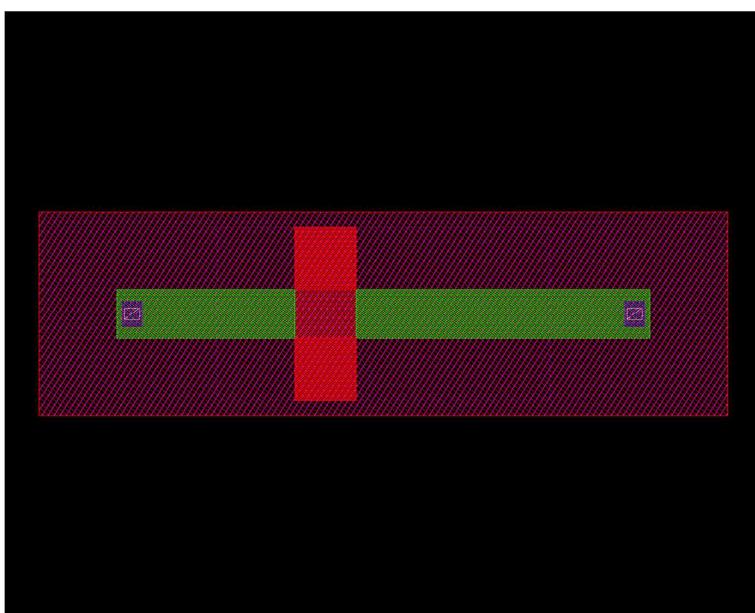




Symbol View:



Layout View:





Device: esdeglvtpfet_fdsoi

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	160n	-
wf	Gate Finger Width	m	160n	-
l	Gate Length	m	150n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-
trise	Temperature Deviation	-	0	-
SourceContColumn	SourceContColumn	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopChoices	Source Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
DrainMetalTopChoices	Drain Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-



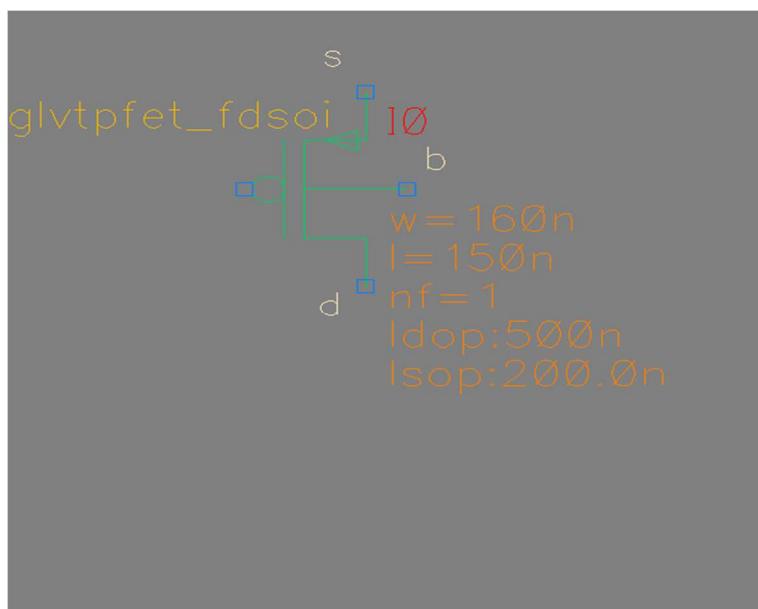


Parameter	Prompt	Units	Default	Range
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig parameters	-	0	'0, 1
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

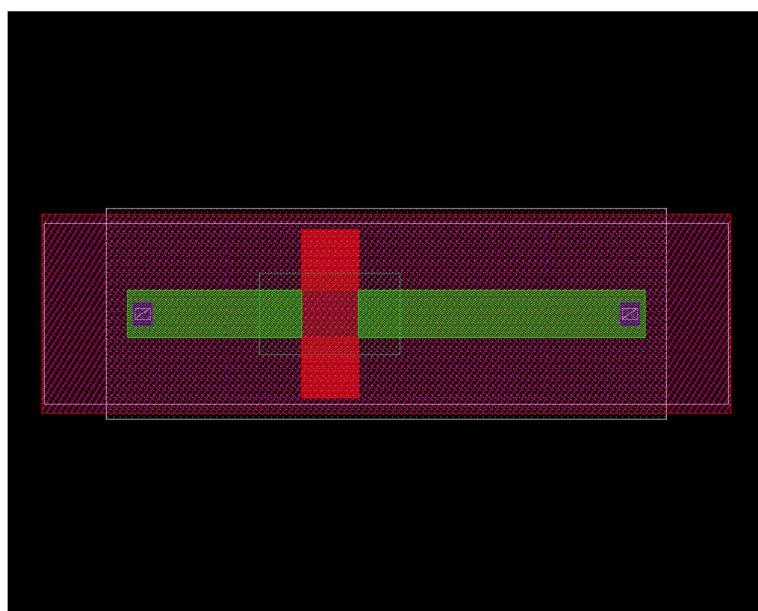




Symbol View:



Layout View:





Device: esdeglvtnfet_fdsoi

Parameter	Prompt	Units	Default	Range
AnalogMosSelectKit	MosSelectKit	-	-	-
w	Gate Width	m	160n	-
wf	Gate Finger Width	m	160n	-
l	Gate Length	m	150n	-
n	Number of Fingers	-	1	-
mult	Multiplicity	-	1	-
ldop	Drain SBLK Length	m	500n	-
lsop	Source SBLK Length	m	200.0n	-
guardRing	GuardRing	-	-	-
T3guardRing	T3 Guard Ring	-	-	-
polyAccess	Gate Contacts	-	NONE	'NONE, BOTTOM, TOP, TOP+BOTTOM
ngcon	Number of Gate Contacts	-	1	-
SourceContColumn	SourceContColumn	-	1	-
DrainContColumn	DrainContColumn	-	1	-
SourceMetalWidth	SourceMetalWidth	-	0.05u	-
DrainMetalWidth	DrainMetalWidth	-	0.05u	-
SourceMetalTopChoices	Source Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
DrainMetalTopChoices	Drain Metal Top	-	M1	'M1, M1-M2, M1-M3, M1-M4
trise	Temperature Deviation	-	0	-
XdefDrain	XdefDrain	-	contact	'contact, user
XdefSource	XdefSource	-	contact	'contact, user
ad	ad	m	0	-
as	as	m	0	-
ad_disp	Total Drain Area	m	4.7174p	-



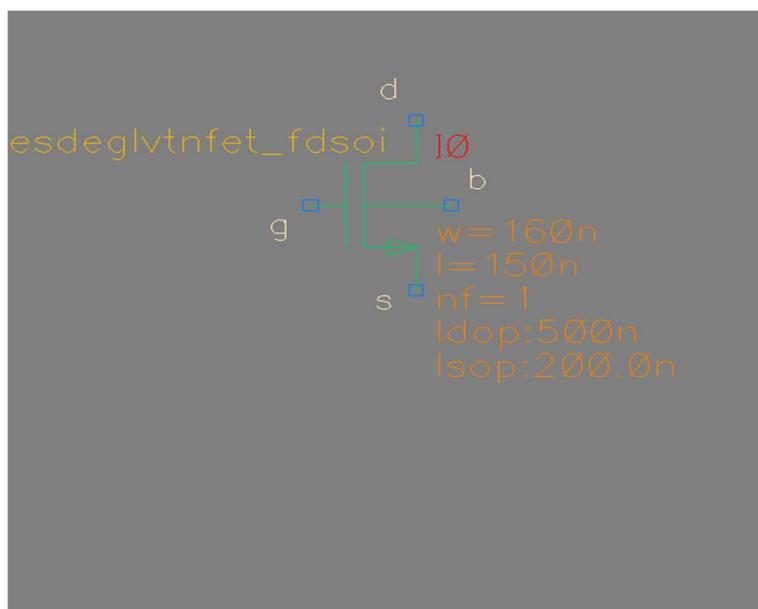


Parameter	Prompt	Units	Default	Range
as_disp	Total Source Area	m	1.0094p	-
ptwell	ptwell	-	0	'0, 1
stiStress	Change STI Stress Estimation?	-	No	'Yes, No
sa	STI Compression (sa)	m	460.00n	-
sb	STI Compression (sb)	m	760.00n	-
simAcc	Simulation Option Expert	-	0	'0, 1
swacc	Activate accurate modeling	-	-1	'-1, 0, 1
swrg	Activate gate resistance modeling	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1
nqs	Activate Non Quasi Static effects modeling	-	0	'0, 1
nsig	Activate nsig parameters	-	0	'0, 1
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
xpos	X-coordinate of gate	m	-1	-
ypos	Y-coordinate of gate	m	-1	-
plorient	plorient	-	1	'1, 2

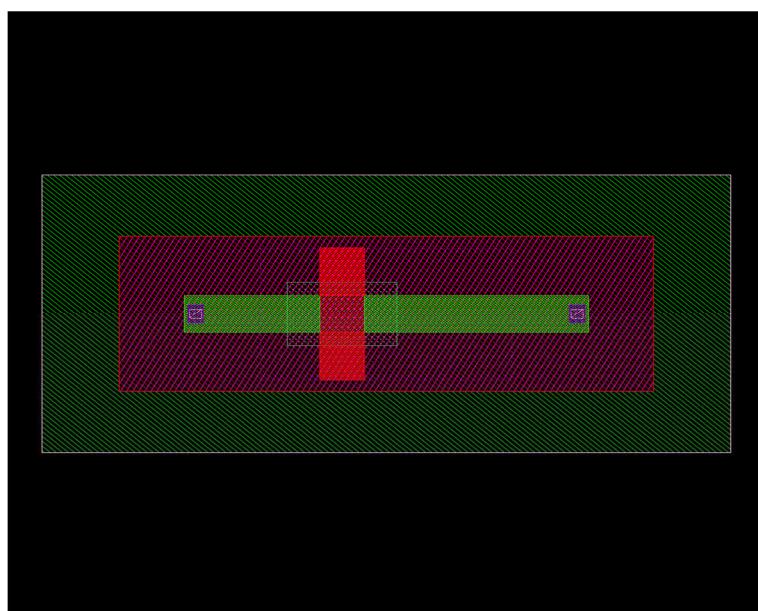




Symbol View:



Layout View:





Device Category: RESISTORS (in library cmos32lp)

Device Type	Cells Names In Device Library
N+ OP Diffusion	opndres_b, opndres
P+ OP Poly (p)	oppccres_b, oppccres
OP RE Polysilicon	opreres_b, opreres
Nwell resistor	nwres_b, nwres

Table: RESISTORS device types and cells

Device: opreres_b

Parameter	Prompt	Units	Default	Range
value	value	Ohms	3.41922K	-
NewWmax	Wmax=35u	-	-	-
w	Stripe Width	m	150.00n	-
l	Stripe Length	m	400n	-
ser	Series Stripes	-	1	-
par	Parallel Stripes	-	1	-
d	Stripe Distance	m	0	-
subres	Substrate Resistance	Ohms	50	-
selfHeating	Self Heating	-	1	-
bp_select	Backplane Designation	-	PW	'NW, PW, T3
Extended_T3	Extended T3	-	-	-
bp	bp	-	3	-
guardRing	Guard Ring	-	-	-
dummies	Create Dummies	-	-	-
routingWidth	Routing Width	m	0	-
contactRows	Contact Rows	-	1	-
dr_mdev	Resistance Deviation	-	0	-
RecommendedRulesSelect	Select Rule Sets	-	-	-



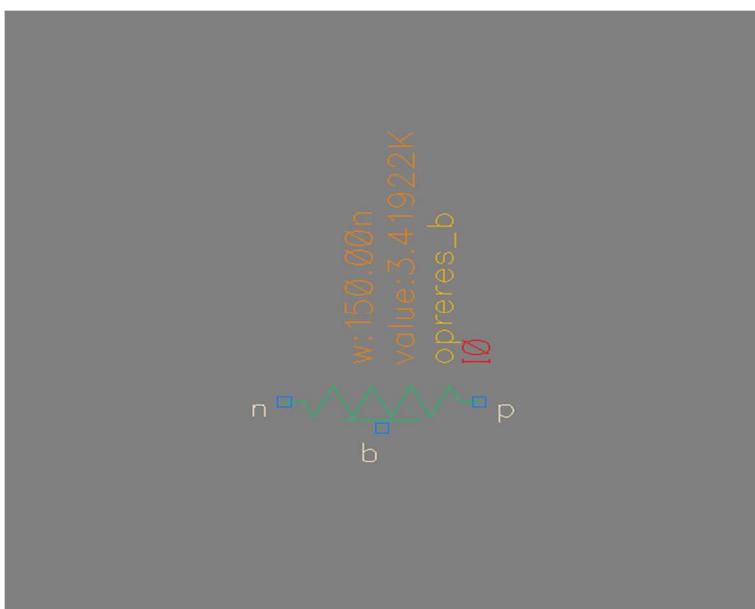


Parameter	Prompt	Units	Default	Range
RecommendedRules	Rule Sets	-	-	-
rodObj	Enable ROD Objects?	-	-	-
soa	Safe Operating Area	-	1	'0, 1
acc	Accurate Model	-	1	'0, 1
ModelNames	Model Name	-	opreres	'opreres, opreres_std
mismatch	mismatch	-	1	'0, 1



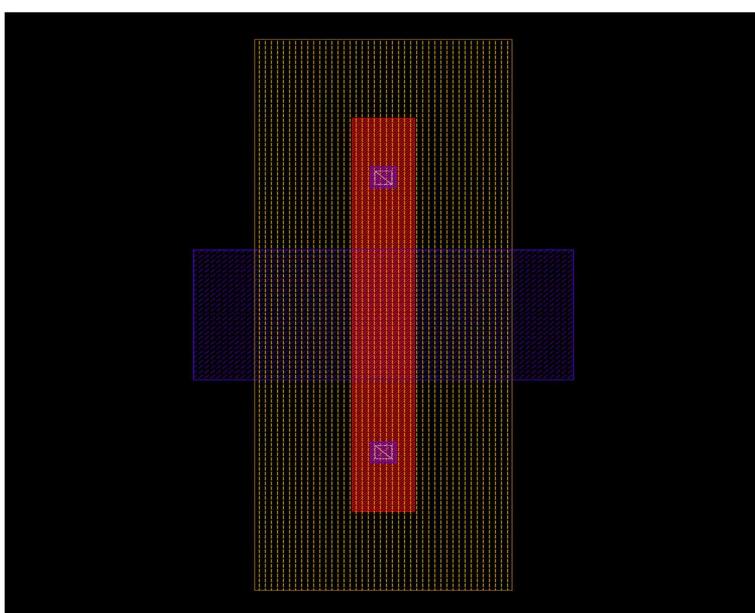


Symbol View:



Terminals order: p, n, b

Layout View:





Device: opreres

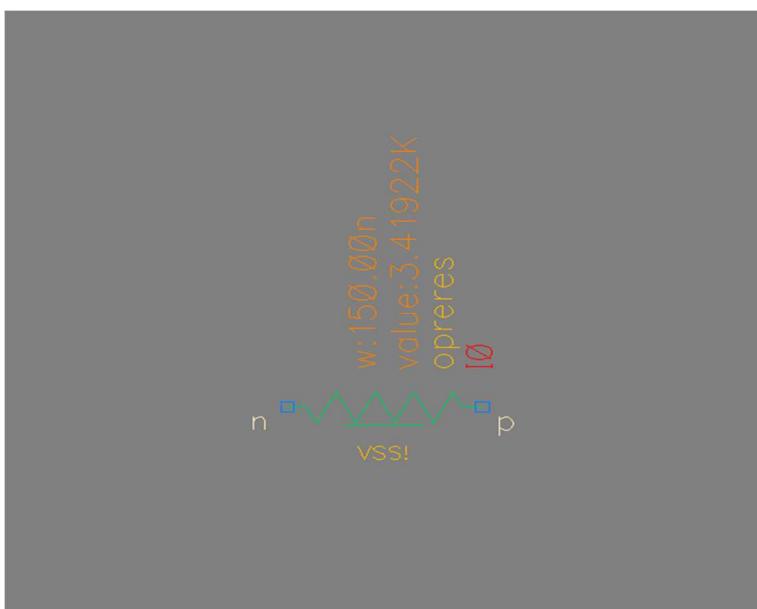
Parameter	Prompt	Units	Default	Range
value	value	Ohms	3.41922K	-
NewWmax	Wmax=35u	-	-	-
w	Stripe Width	m	150.00n	-
l	Stripe Length	m	400n	-
ser	Series Stripes	-	1	-
par	Parallel Stripes	-	1	-
d	Stripe Distance	m	0	-
resbulk	Bulk	-	[@lSup:%:VSS!]	-
subres	Substrate Resistance	Ohms	50	-
selfHeating	Self Heating	-	1	-
bp_select	Backplane Designation	-	PW	'NW, PW, T3
Extended_T3	Extended T3	-	-	-
bp	bp	-	3	-
guardRing	Guard Ring	-	-	-
dummies	Create Dummies	-	-	-
routingWidth	Routing Width	m	0	-
contactRows	Contact Rows	-	1	-
dr_mdev	Resistance Deviation	-	0	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rodObj	Enable ROD Objects?	-	-	-
soa	Safe Operating Area	-	1	'0, 1
acc	Accurate Model	-	1	'0, 1
ModelNames	Model Name	-	opreres	'opreres, opreres_std
mismatch	mismatch	-	1	'0, 1





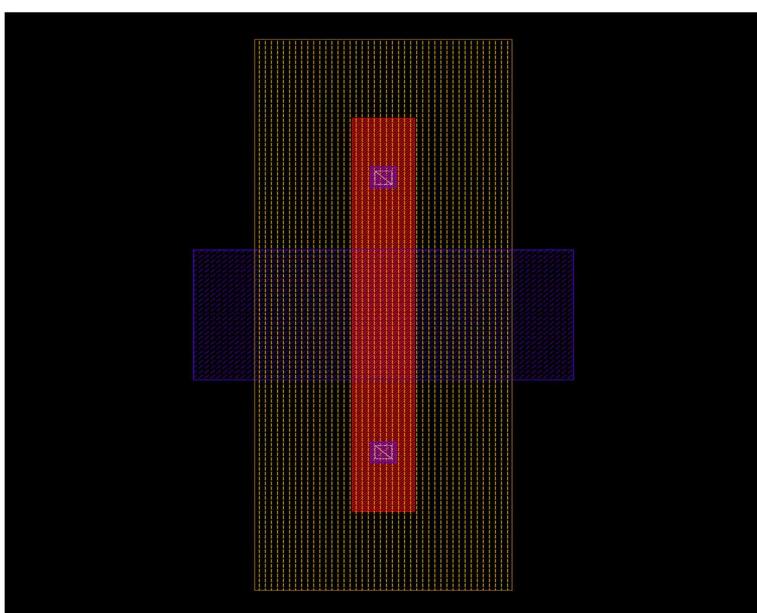


Symbol View:



Terminals order: p, n, b

Layout View:





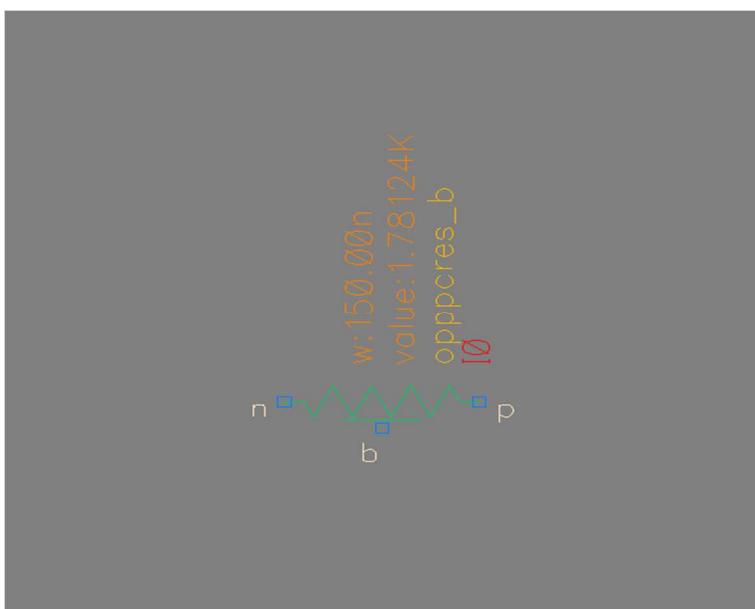
Device: opppcres_b

Parameter	Prompt	Units	Default	Range
value	value	Ohms	1.78124K	-
NewWmax	Wmax=35u	-	-	-
w	Stripe Width	m	150.00n	-
l	Stripe Length	m	400n	-
ser	Series Stripes	-	1	-
par	Parallel Stripes	-	1	-
d	Stripe Distance	m	0	-
subres	Substrate Resistance	Ohms	50	-
selfHeating	Self Heating	-	1	-
bp_select	Backplane Designation	-	PW	'NW, PW, T3
Extended_T3	Extended T3	-	-	-
bp	bp	-	3	-
guardRing	Guard Ring	-	-	-
dummies	Create Dummies	-	-	-
routingWidth	Routing Width	m	0	-
contactRows	Contact Rows	-	1	-
dr_mdev	Resistance Deviation	-	0	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rodObj	Enable ROD Objects?	-	-	-
soa	Safe Operating Area	-	1	'0, 1
acc	Accurate Model	-	1	'0, 1
ModelNames	Model Name	-	opppcres	'opppcres, opppcres_std
mismatch	mismatch	-	1	'0, 1



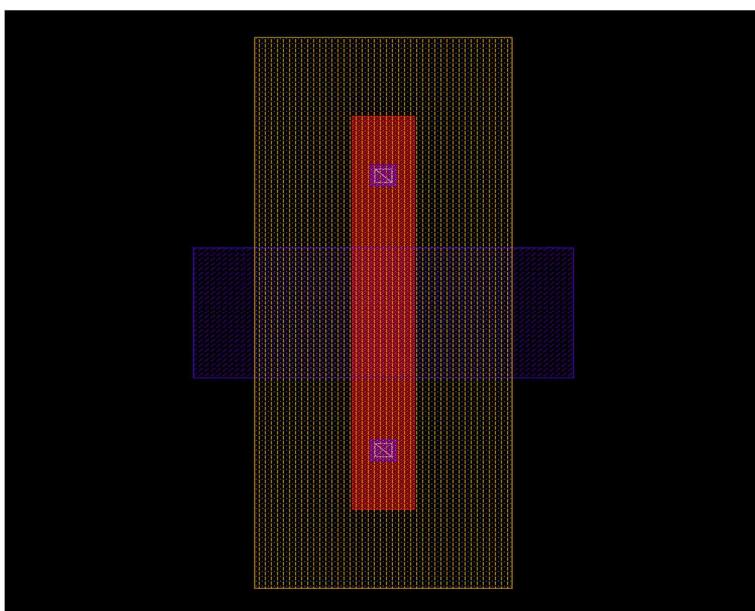


Symbol View:



Terminals order: p, n, b

Layout View:





Device: opppcres

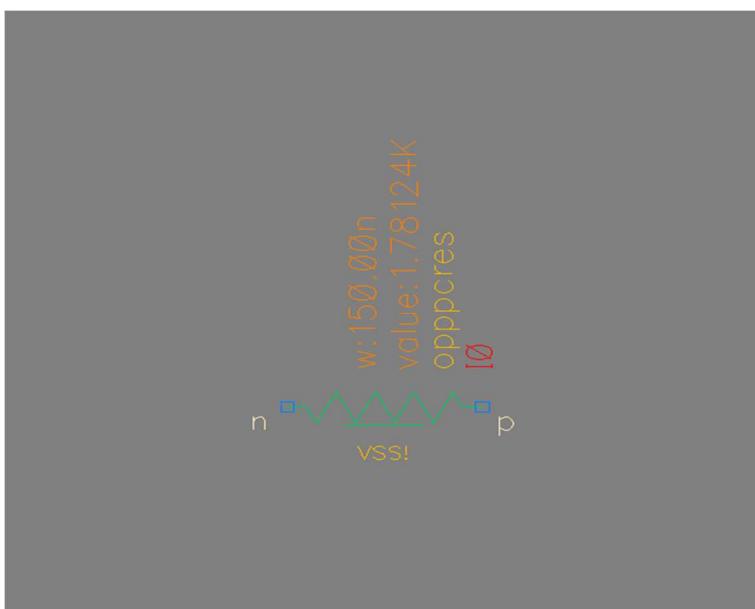
Parameter	Prompt	Units	Default	Range
value	value	Ohms	1.78124K	-
NewWmax	Wmax=35u	-	-	-
w	Stripe Width	m	150.00n	-
l	Stripe Length	m	400n	-
ser	Series Stripes	-	1	-
par	Parallel Stripes	-	1	-
d	Stripe Distance	m	0	-
resbulk	Bulk	-	[@lSup:%:VSS!]	-
subres	Substrate Resistance	Ohms	50	-
selfHeating	Self Heating	-	1	-
bp_select	Backplane Designation	-	PW	'NW, PW, T3
Extended_T3	Extended T3	-	-	-
bp	bp	-	3	-
guardRing	Guard Ring	-	-	-
dummies	Create Dummies	-	-	-
routingWidth	Routing Width	m	0	-
contactRows	Contact Rows	-	1	-
dr_mdev	Resistance Deviation	-	0	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rodObj	Enable ROD Objects?	-	-	-
soa	Safe Operating Area	-	1	'0, 1
acc	Accurate Model	-	1	'0, 1
ModelNames	Model Name	-	opppcres	'opppcres, opppcres_std
mismatch	mismatch	-	1	'0, 1





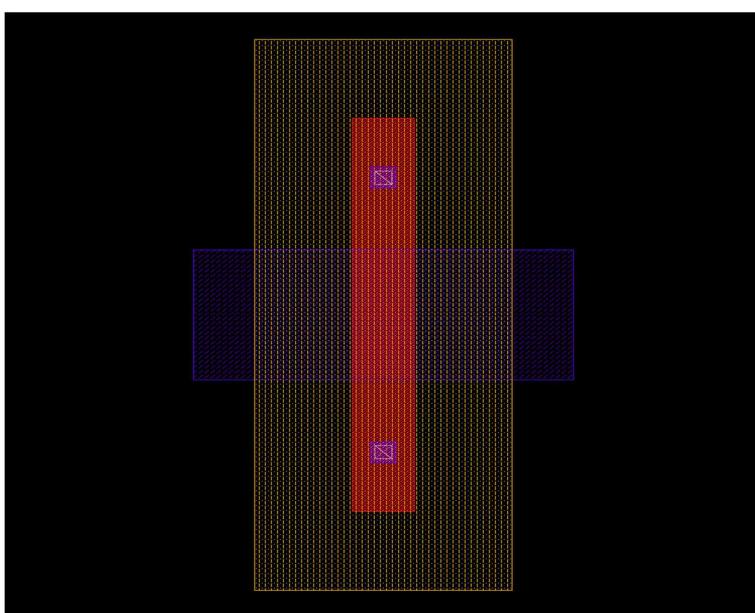


Symbol View:



Terminals order: p, n, b

Layout View:





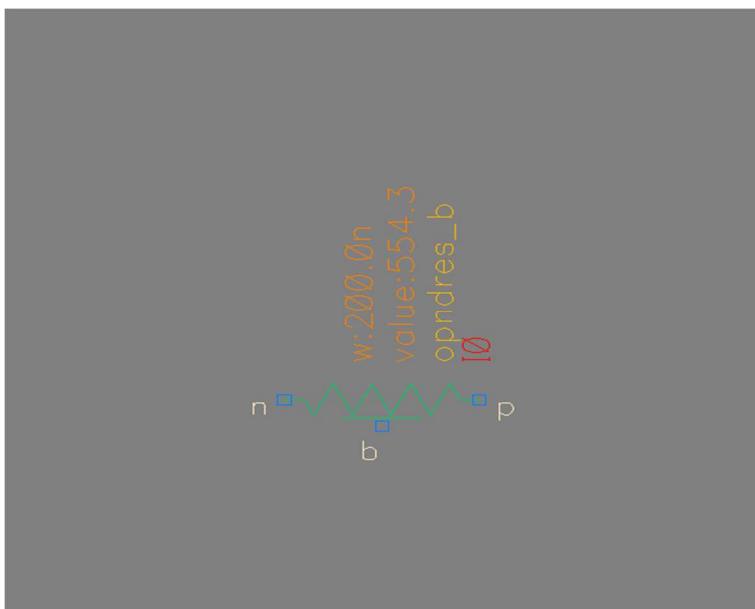
Device: opndres_b

Parameter	Prompt	Units	Default	Range
value	value	Ohms	554.3	-
NewWmax	Wmax=35u	-	-	-
w	Stripe Width	m	200.0n	-
l	Stripe Length	m	400n	-
ser	Series Stripes	-	1	-
par	Parallel Stripes	-	1	-
d	Stripe Distance	m	0	-
subres	Substrate Resistance	Ohms	50	-
selfHeating	Self Heating	-	1	-
guardRing	Guard Ring	-	-	-
dummies	Create Dummies	-	-	-
routingWidth	Routing Width	m	0	-
contactRows	Contact Rows	-	1	-
dr_mdev	Resistance Deviation	-	0	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rodObj	Enable ROD Objects?	-	-	-
soa	Safe Operating Area	-	1	'0, 1
acc	Accurate Model	-	1	'0, 1
ModelNames	Model Name	-	opndres	'opndres, opndres_std
mismatch	mismatch	-	1	'0, 1



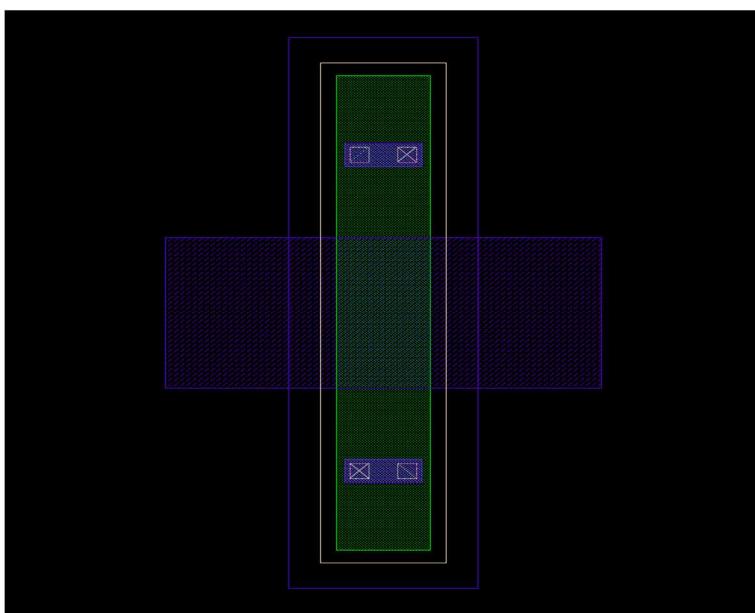


Symbol View:



Terminals order: p, n, b

Layout View:





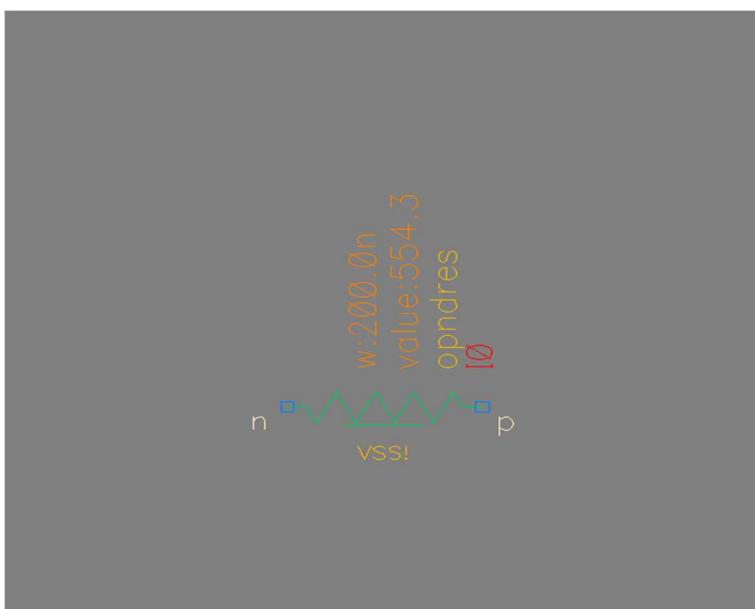
Device: opndres

Parameter	Prompt	Units	Default	Range
value	value	Ohms	554.3	-
NewWmax	Wmax=35u	-	-	-
w	Stripe Width	m	200.0n	-
l	Stripe Length	m	400n	-
ser	Series Stripes	-	1	-
par	Parallel Stripes	-	1	-
d	Stripe Distance	m	0	-
resbulk	Bulk	-	[@lSup:%:VSS!]	-
subres	Substrate Resistance	Ohms	50	-
selfHeating	Self Heating	-	1	-
guardRing	Guard Ring	-	-	-
dummies	Create Dummies	-	-	-
routingWidth	Routing Width	m	0	-
contactRows	Contact Rows	-	1	-
dr_mdev	Resistance Deviation	-	0	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rodObj	Enable ROD Objects?	-	-	-
soa	Safe Operating Area	-	1	'0, 1
acc	Accurate Model	-	1	'0, 1
ModelNames	Model Name	-	opndres	'opndres, opndres_std
mismatch	mismatch	-	1	'0, 1



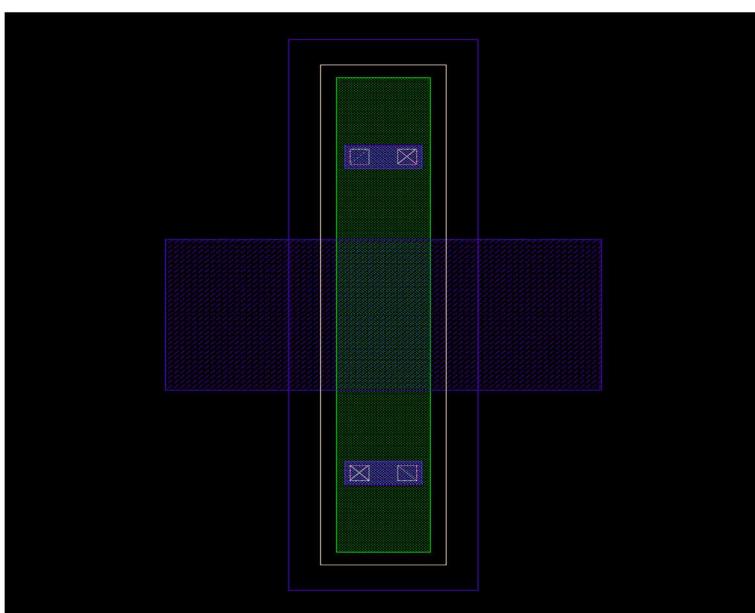


Symbol View:



Terminals order: p, n, b

Layout View:





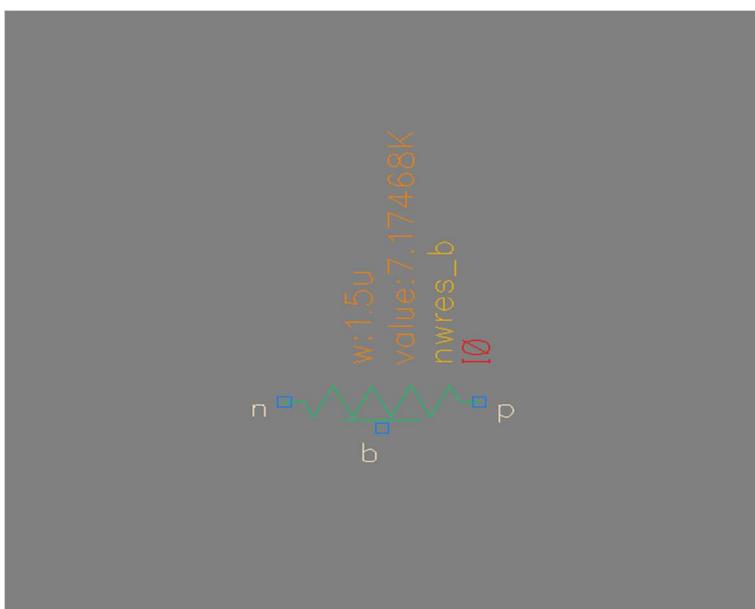
Device: nwres_b

Parameter	Prompt	Units	Default	Range
value	value	Ohms	7.17468K	-
NewWmax	Wmax=35u	-	-	-
w	Stripe Width	m	1.5u	-
l	Stripe Length	m	10u	-
ser	Series Stripes	-	1	-
par	Parallel Stripes	-	1	-
d	Stripe Distance	m	0	-
subres	Substrate Resistance	Ohms	50	-
selfHeating	Self Heating	-	1	-
guardRing	Guard Ring	-	-	-
dummies	Create Dummies	-	-	-
routingWidth	Routing Width	m	0	-
dr_mdev	Resistance Deviation	-	0	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rodObj	Enable ROD Objects?	-	-	-
soa	Safe Operating Area	-	1	'0, 1
acc	Accurate Model	-	1	'0, 1
ModelNames	Model Name	-	nwres	'nwres, nwres_std
mismatch	mismatch	-	1	'0, 1



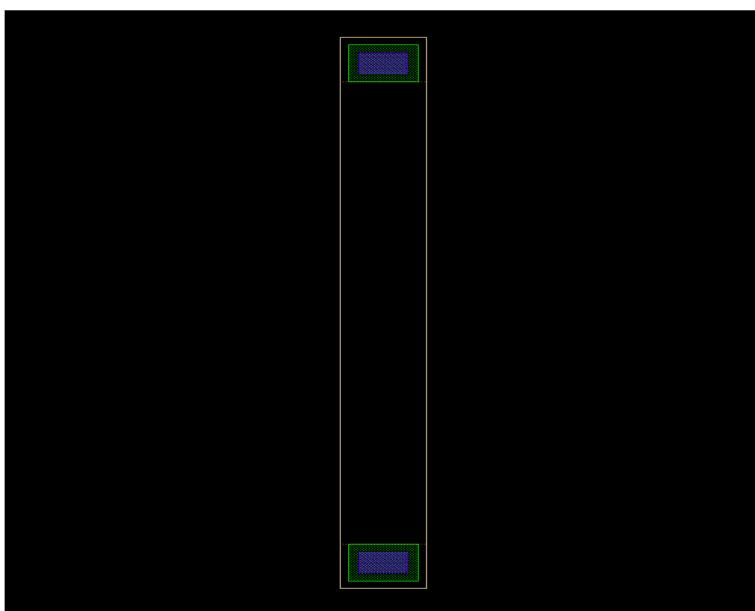


Symbol View:



Terminals order: p, n, b

Layout View:





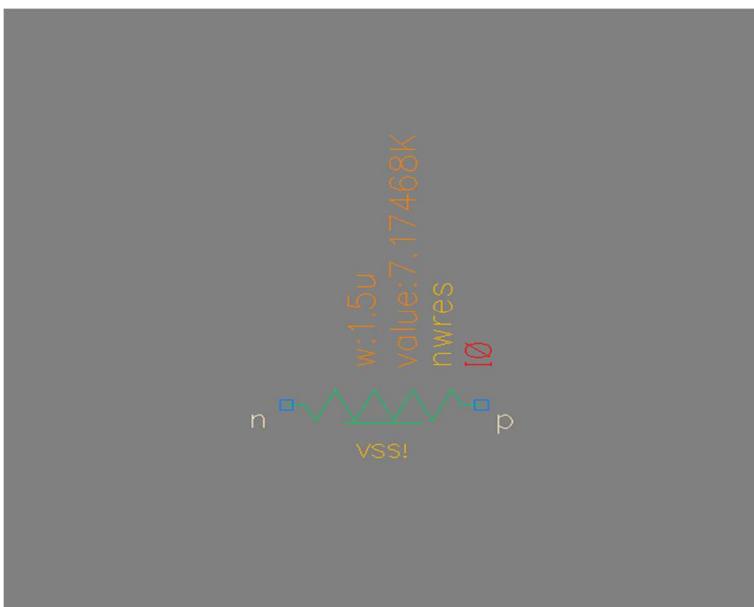
Device: nwres

Parameter	Prompt	Units	Default	Range
value	value	Ohms	7.17468K	-
NewWmax	Wmax=35u	-	-	-
w	Stripe Width	m	1.5u	-
l	Stripe Length	m	10u	-
ser	Series Stripes	-	1	-
par	Parallel Stripes	-	1	-
d	Stripe Distance	m	0	-
resbulk	Bulk	-	[@lSup:%:VSS!]	-
subres	Substrate Resistance	Ohms	50	-
selfHeating	Self Heating	-	1	-
guardRing	Guard Ring	-	-	-
dummies	Create Dummies	-	-	-
routingWidth	Routing Width	m	0	-
dr_mdev	Resistance Deviation	-	0	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rodObj	Enable ROD Objects?	-	-	-
soa	Safe Operating Area	-	1	'0, 1
acc	Accurate Model	-	1	'0, 1
ModelNames	Model Name	-	nwres	'nwres, nwres_std
mismatch	mismatch	-	1	'0, 1



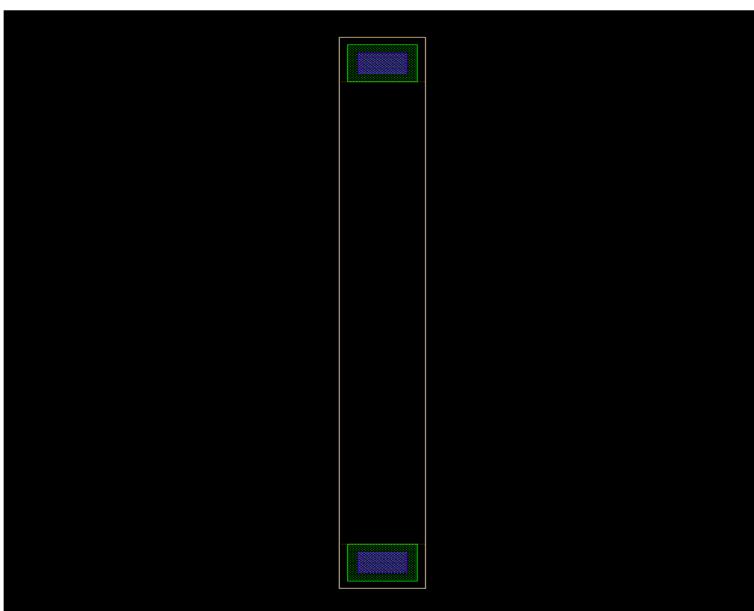


Symbol View:



Terminals order: p, n, b

Layout View:





Device Category: SRAM (in library cmos32lp)

Device Type	Cells Names In Device Library
28nm Dense Cell 0.120 SRAM Pull Down NFET	dswnfetpd_b, dsvnfetpd_b
28FDSOI High Speed 0.152 SRAM Pull Up PFET	lsdpfetpu_b
28nm Dense Cell 0.120 SRAM Pass Gate NFET	dswnfetwl_b, dsvnfetwl_b
28FDSOI High Speed SRAM Pass Gate NFET	lsdnfetwl_b
2-Port 0.251 Secondary Read-Port NFET (TP251)	lshnfet_b
28nm High Speed 0.152 SRAM Pull Up PFET	lsppfetpu_b
28nm 2-Port 0.251 SRAM Pull Up PFET	lsvpfetpu_b
28nm Dense Cell 0.120 SRAM Pull Up PFET	dswpfetpu_b, dsvpfetpu_b
28nm High Speed 0.152 SRAM Pull Down NFET	lspnfetpd_b, lsdnfetpd_b
28nm High Speed 0.152 SRAM Pass Gate NFET	lspnfetwl_b
28nm 2-Port 0.251 SRAM Pass Gate NFET	lsvnfetwl_b
28nm 2-Port 0.251 SRAM Pull Down NFET	lsvnfetpd_b

Table: SRAM device types and cells

Device: lsdpfetpu_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	62n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	42n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-





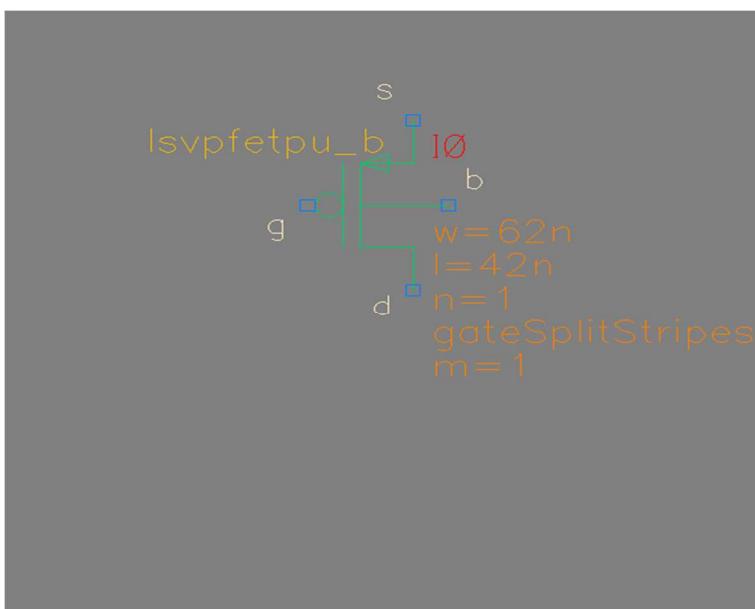
Parameter	Prompt	Units	Default	Range
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1







Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: lsvnfetwl_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	190n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	42n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-



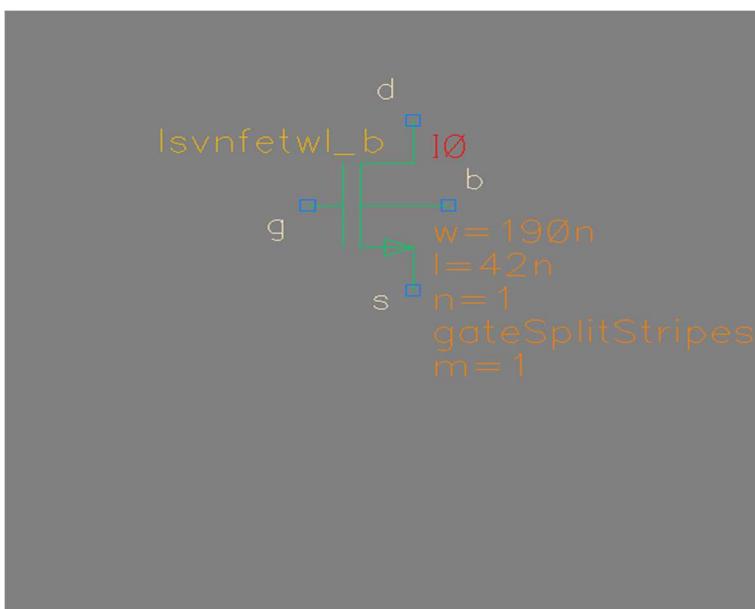


Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: lsvnfetpd_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	250n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	42n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-



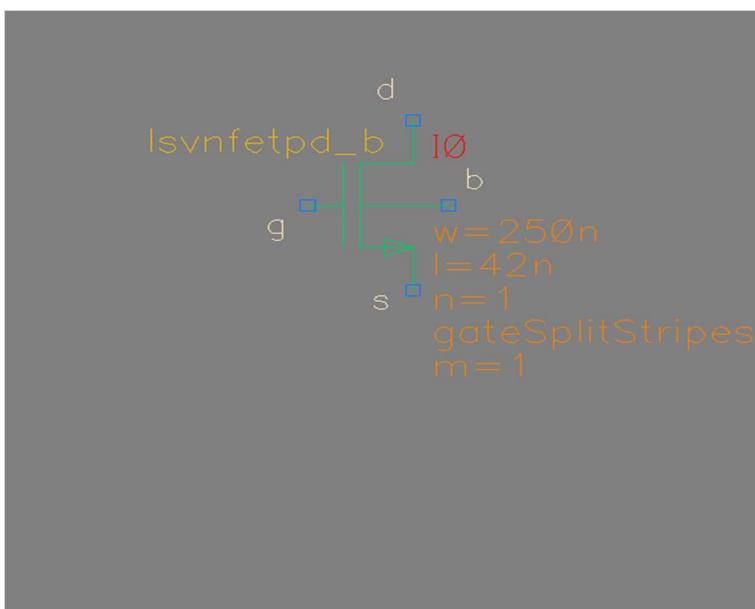


Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: lsppfetpu_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	62n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	40n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-



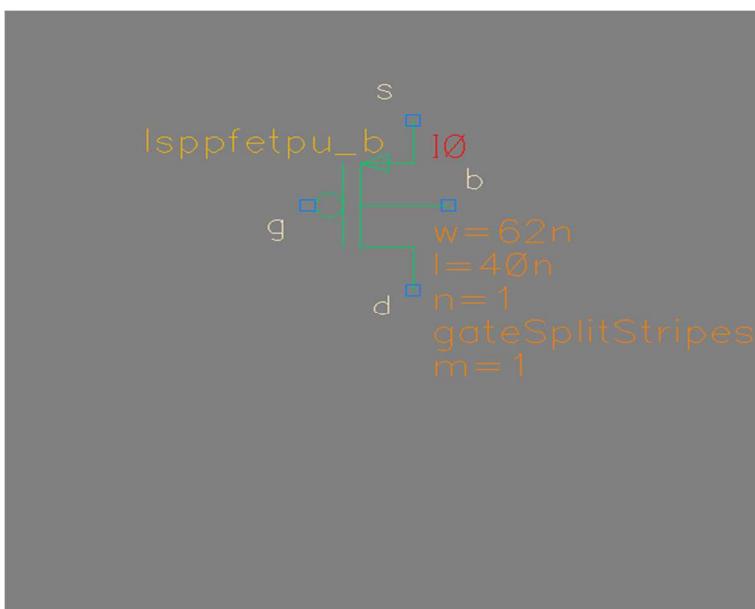


Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: lspnfetwl_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	133n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	40n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-





Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: lspnfetpd_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	162n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	40n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-



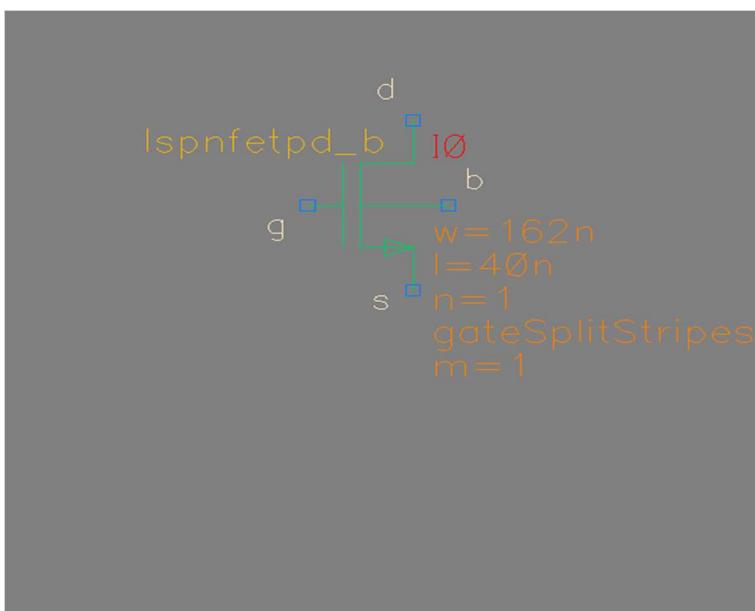


Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: IslInfet_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	240n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	40n	-
n	number of gate fingers	-	1	-
gateSplitStripes	Gate Split Y	-	1	-
pccrit_select	Critical Gate?	-	-	-
wellSelect	Triple Well?	-	-	-
tieDown	tieDown	-	-	-
tieDownPlacement	tieDown Placement	-	none	'none, intern
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
stiStress	Change STI Stress Estimation?	-	Yes	'Yes, No
sa	STI Compression (sa)	m	-	-
sb	STI Compression (sb)	m	-	-
sd	STI Compression (sd)	m	-	-





Parameter	Prompt	Units	Default	Range
dummyPoly	ACLV PC Fill	-	None	'Both, Left, Right, None
cnt	cnt	-	t	-
cntBLR	cntBLR	-	Both	'Both, Left, Right
polyCnt	Poly Contact	-	-	-
PolyRoute	PolyRoute	-	t	-
Pw	Poly Route Width	m	0	-
guardRing	Guard Ring	-	-	-
grStubs	Guardring Segments	-	LTBR	'None, L, R, LR, T, B, TB, LT, LB, TR, BR, LTR, LBR, LTB, TBR, LTBR
grStubs2	Second Guardring Segments	-	None	'None, L, R, LR, T, B, TB, LT, LB, TR, BR, LTR, LBR, LTB, TBR, LTBR
M1Route	M1Route	-	t	-
minRoute	minRoute	-	-	-
distRoute	distRoute	m	0	-
Sw	Source Width	m	0	-
Dw	Drain Width	m	0	-
diffStretchLeft	Diffusion Stretch Left	m	0	-
diffStretchRight	Diffusion Stretch Right	m	0	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
rodObj	Enable ROD Objects?	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2





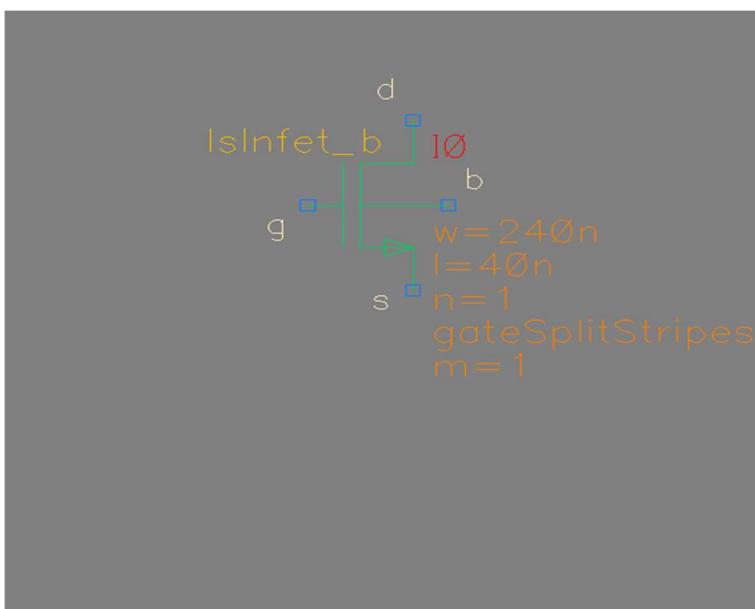
Parameter	Prompt	Units	Default	Range
ptwell	ptwell	-	0	'0, 1
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	-	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
p_vta	p_vta	V	-	-
sca	sca	-	-	-
scb	scb	-	-	-
scc	scc	-	-	-
u0_mult	u0_mult	-	-	-
stress_vt	stress_vt	V	-	-
pre_layout_local	pre_layout_local	-	-	-
lpccnr	lpccnr	-	-	-
covpccnr	covpccnr	-	-	-
wrxcnr	wrxcnr	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	-	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	-	-
mismatch	mismatch	-	1	'0, 1
soa	Safe Operating Area	-	1	'0, 1







Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: lsdpfetpu_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	105n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	38n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-



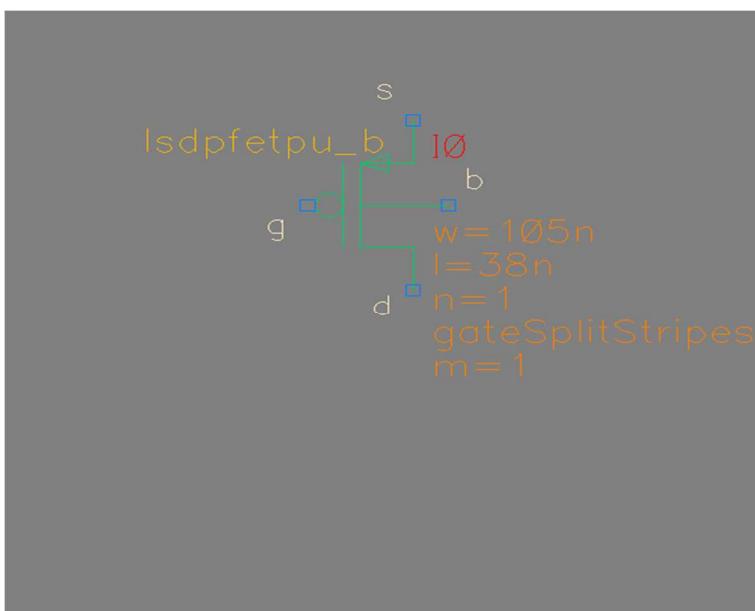


Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: lsdnfetwl_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	125n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	42n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-





Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: lsdnfetpd_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	305n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	38n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-





Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: dswpfetpu_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	51n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	40n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-



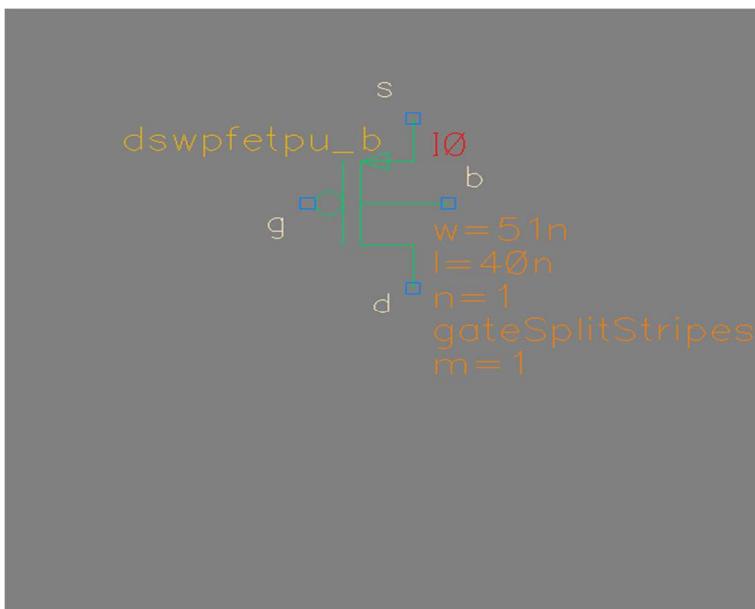


Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: dswnfetwl_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	91n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	44n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-





Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: dswnfetpd_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	106n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	40n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-



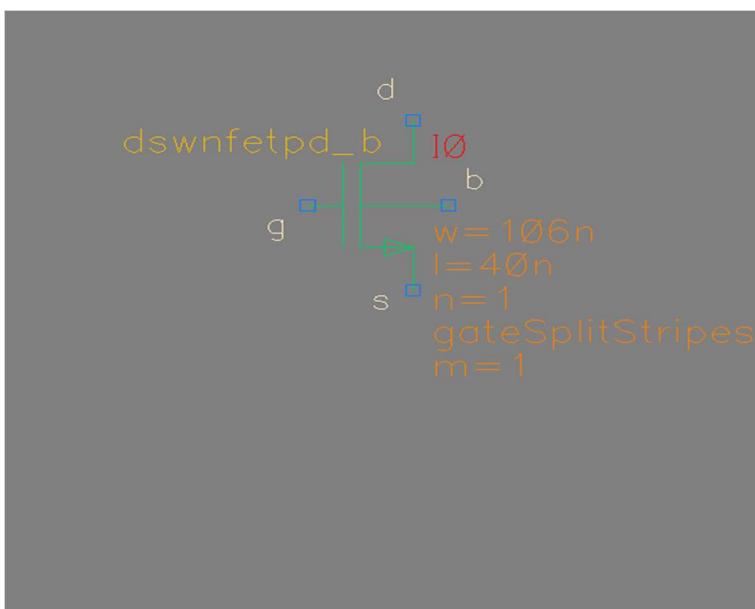


Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: dsvpfetpu_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	51n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	40n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-



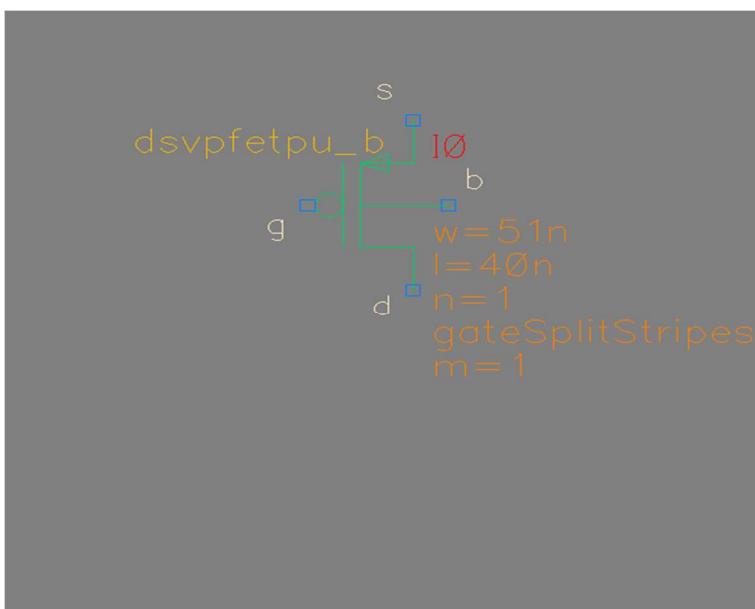


Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: dsvnfetwl_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	91n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	44n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-





Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device: dsvnfetpd_b

Parameter	Prompt	Units	Default	Range
m	Multiplicity	-	1	-
w	Total Gate Width	m	106n	-
wf	Gate Finger Width	m	-	-
l	Gate Length	m	40n	-
n	number of gate fingers	-	1	-
XdefDrain	XdefDrain	-	contact	'stack, noStack, contact, user
XdefSource	XdefSource	-	contact	'stack, noStack, contact, user
ad	ad	m	-	-
as	as	m	-	-
pd	pd	m	-	-
ps	ps	m	-	-
ad_disp	Total Drain Area	-	-	-
as_disp	Total Source Area	-	-	-
pd_disp	Total Drain Periphery	-	-	-
ps_disp	Total Source Periphery	-	-	-
ngcon	Number of Gate Contacts	-	1	-
plorient	plorient	-	1	'1, 2
pccrit	pccrit	-	0	-
p_la	p_la	m	0	-
par	par	-	1	-
psw_acv_sign	psw_acv_sign	-	1	-
plnest	plnest	-	-	-
pdevdops	pdevdops	-	-	-
pdevlgeos	pdevlgeos	-	-	-
pdevwgeos	pdevwgeos	-	-	-
pld200	pld200	-	-	-
stress_vt	stress_vt	V	0	-



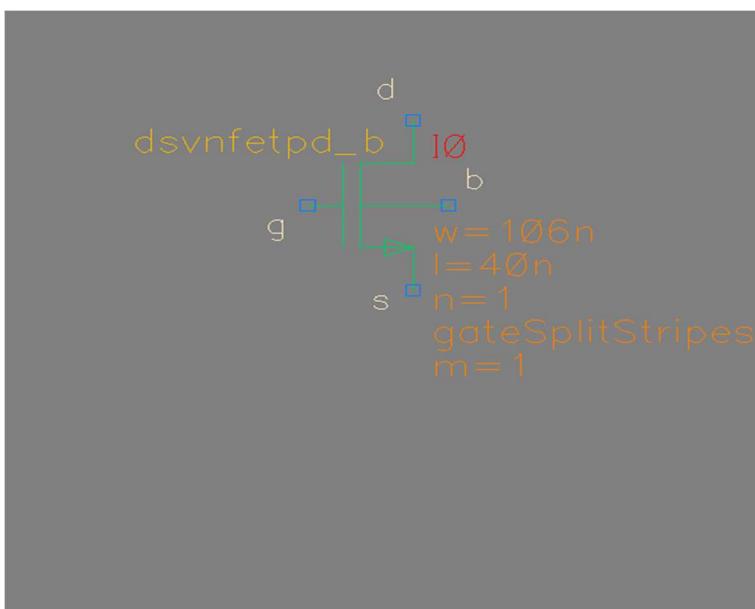


Parameter	Prompt	Units	Default	Range
pre_layout_local	pre_layout_local	-	-	-
nsig_vto	nsig_vto	-	0	-
nsig_uo	nsig_uo	-	0	-
nsig_dibl	nsig_dibl	-	0	-
nsig_lvaro	nsig_lvaro	-	0	-
nsig_wvaro	nsig_wvaro	-	0	-
nsig_delvto_uo1	Flat-Band Voltage Deviation	-	0	-
nsig_delvto_uo2	Zero Field Mobility Deviation	-	0	-
soa	Safe Operating Area	-	1	'0, 1
mismatch	mismatch	-	1	'0, 1





Symbol View:



Terminals order: d, g, s, b

Layout View:

NO VIEW AVAILABLE





Device Category: Wire_Models (in library cmos32lp)

Device Type	Cells Names In Device Library
TBD	mxlvsres, lvsres

Table: WIRE_MODELS device types and cells

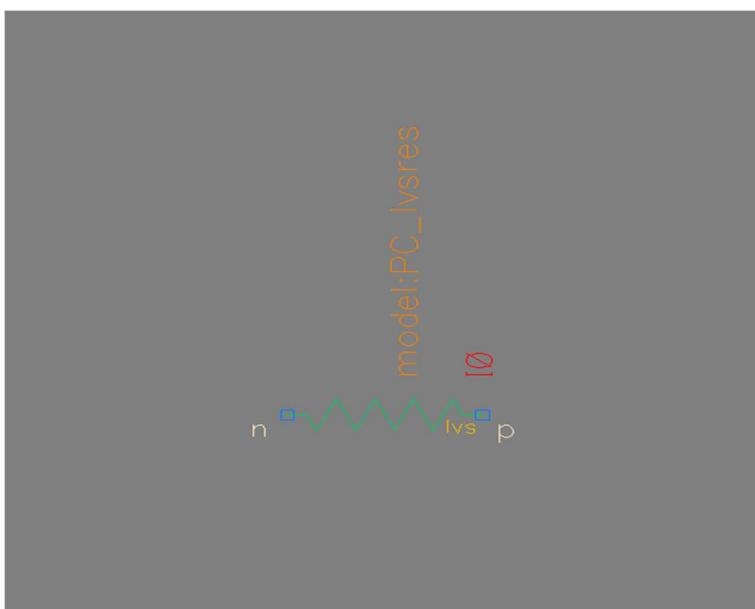
Device: mxlvsres

Parameter	Prompt	Units	Default	Range
w	w	m	50n	-
l	l	m	200n	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
model	Layout model	-	PC_lvsres	'PC_lvsres



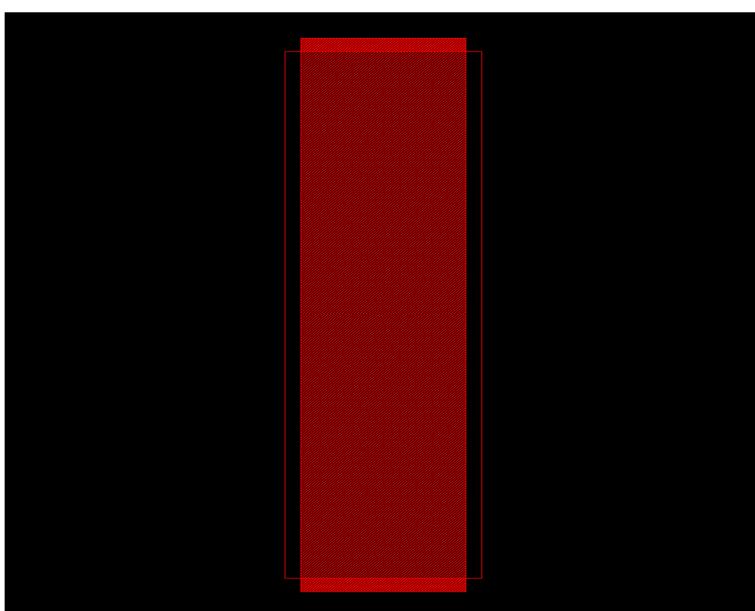


Symbol View:



Terminals order: p, n

Layout View:





Device: lvsres

Parameter	Prompt	Units	Default	Range
w	w	m	50n	-
l	l	m	200n	-
RecommendedRulesSelect	Select Rule Sets	-	-	-
RecommendedRules	Rule Sets	-	-	-
model	Layout model	-	PC_lvsres	'PC_lvsres





Symbol View:



Terminals order: p, n

Layout View:

