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Device sub-circuit and DC Operating Point related information

28FDSOI devices covered in this document:

lvtnfet_acc lvtpfet_acc nfet_acc pfet_acc egnfet_acc egpfet_acc egvnfet_acc egvpfet_acc eglvtnfet_acc eglvtpfet_acc eglvtvnfet_acc eglvtvpfet_acc lvtnfet_rf lvtpfet_rf nfet_rf pfet_rf eglvtnfet_rf eglvtpfet_rf egvlvtnfet_rf egvlvtpfet_rf lvtnfet_rfseg lvtpfet_rfseg nfet_rfseg pfet_rfseg eglvtnfet_rfseg eglvtpfet_rfseg egvlvtnfet_rfseg egvlvtpfet_rfseg

Document Revision History*

Release	Date	Authors	Comments
1.0.0	July 19th, 2018	Salim EL GHOULI	Initial draft release

** See corresponding model status document for related model release*

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Device cross-section & modeling

To accurately model the electrical behavior of a device[1], SPICE modelers implement an equivalent circuit (sub-circuit) that reproduces its measured characteristics and figures of merit. Compact and usually standardized models (PSP, BSIM, UTSOI[2] …) are used in these sub-circuits.

I. Device cross-section view

In Fig. 1, cross-sectional views are given for thin oxide (SG) and thick oxide (EG) supported MOSFETs and for both Regular V_T and Low V_T families in 28FDSOI technology. Please refer to the Design Manual for more detail.

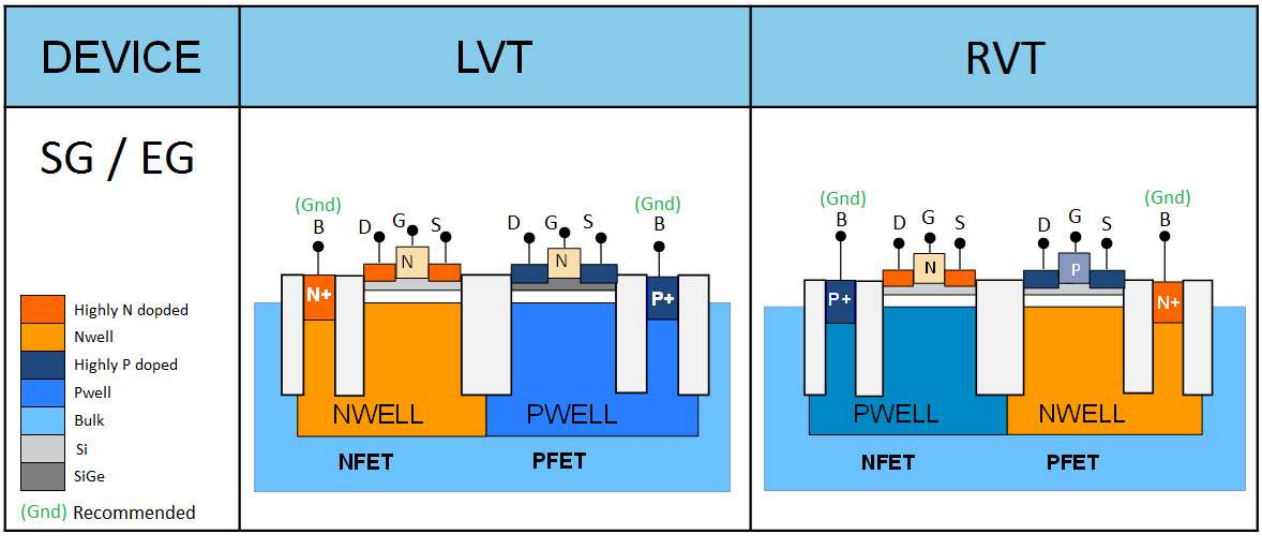

Fig. 1 – SG and EG MOSFETs cross sections.

II. Device sub-circuit

In STMicroelectronics 28FDSOI technology, MOSFET models (sub-circuits) are based on Leti-UTSOI2 compact model. In order to cover several applications, two main model sets are proposed: (1) _acc models for standard usage including digital and low frequency analog design, and (2) _rf models for Radio Frequency (RF) and mm-Wave usage. For RF and mm-Wave applications, a second simulation level _rfseg is also proposed for Non-Quasi-Static (NQS) operation which is typically dominant at high

[1] An electrical device could be Active such as the Low-V_T logic MOSFET or passive such as the poly resistor. The complete supported device list in a given technology represents the Technology Offer.
[2] UTSOI is the surface potential based compact model for Ultra-Thin fully depleted SOI MOSFET. Latest version is the Leti-UTSOI2 V2.2.

frequency for L > 100 nm. RF models are accounting for the distributed nature of the gate resistance (RC implementation).

_acc models:

For low frequency accurate models (with "_acc" suffix), the main MOSFET effects are modeled using "M_1" main MOSFET spice instance. Gate resistance R_G and drain to source capacitance C_{sdext} are added in pre-layout circuits to take into account external contributions that are usually managed by the Parastic EXtraction (PEX) in the post-layout circuit simulations. Please note that only pre-layout case is covered in this document.

The following circuit diagram is a representation of the following supported devices:

lvtnfet_acc lvtpfet_acc nfet_acc pfet_acc egnfet_acc egpfet_acc egvnfet_acc egvpfet_acc eglvtnfet_acc eglvtpfet_acc eglvtvnfet_acc eglvtvpfet_acc

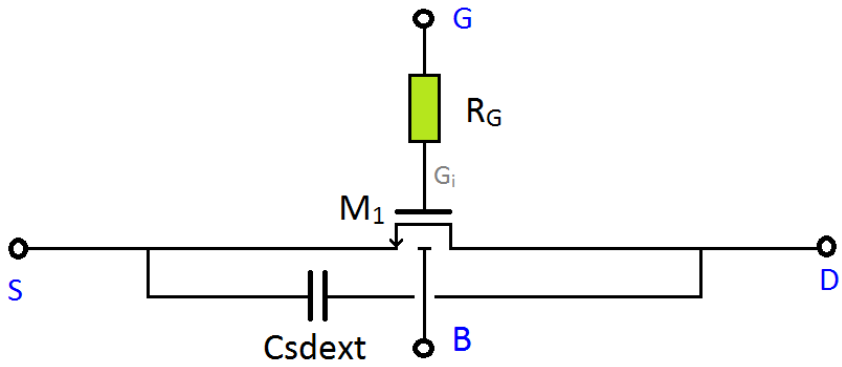

Fig. 2 – Circuit diagram representation of the _acc device sub-circuit.

_rf models:

For _rf models, the distributed nature of the gate resistance is modeled using RC circuit. A simplified version of the NQS effect can be enabled using SWNQS flag. The following circuit diagram is a representations of the following supported devices:

lvtnfet_rf lvtpfet_rf nfet_rf pfet_rf eglvtnfet_rf eglvtpfet_rf egvlvtnfet_rf egvlvtpfet_rf

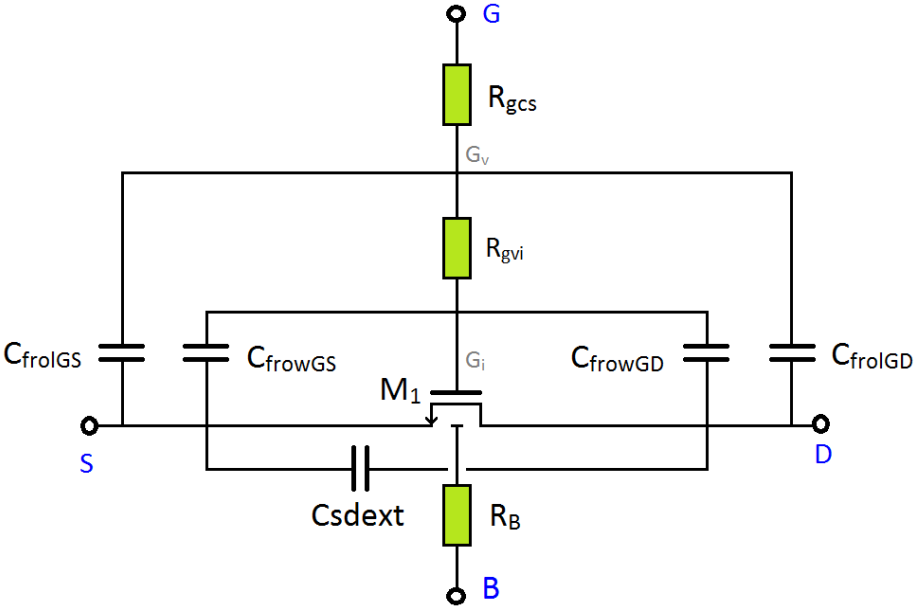

Fig. 3 – Circuit diagram representation of the _rf device sub-circuit.

WARNING: Be warned that external parasitic resistors and capacitors presence in the above circuit diagrams (_acc and _rf) is controlled by two instance parameters:

- SWRG: for external gate resistance presence control.
- PRE_LAYOUT_LOCAL: for external source and drain resistances and all parasitic capacitances presence control.

Instance parameter	Value	Impact on above circuit diagram
SWRG[3]	0	Gate resistance is removed
	1 (default)	Gate resistance is present
PRE_LAYOUT_LOCAL[4]	-1 (default)	All parasitic resistances and capacitances are present
	0	All parasitic resistances and capacitances are removed
	1	All parasitic resistances and capacitances are present (same as default -1)
	2	Parasitic capacitances are present and parasitic resistances are removed
	3	All parasitic resistances are present and capacitances are removed

[3] Device instance parameter switch for gate resistance.
[4] Device instance parameter switch for parasitic (post-layout) resistances and external parasitic capacitances.

_rfseg models:

In addition to the gate distributed effect modeling, the _rfseg is taking into account the distributed nature of the channel, which is commonly called NQS effect. The NQS effect is taken into account using channel segmentation (5 series MOSFETS are used). An additional M_{ext} MOSFET is used to account for fringing capacitances. The following circuit diagram is a representation of the following supported devices:

lvtnfet_rfseg lvtpfet_rfseg nfet_rfseg pfet_rfseg eglvtnfet_rfseg eglvtpfet_rfseg egvlvtnfet_rfseg egvlvtpfet_rfseg

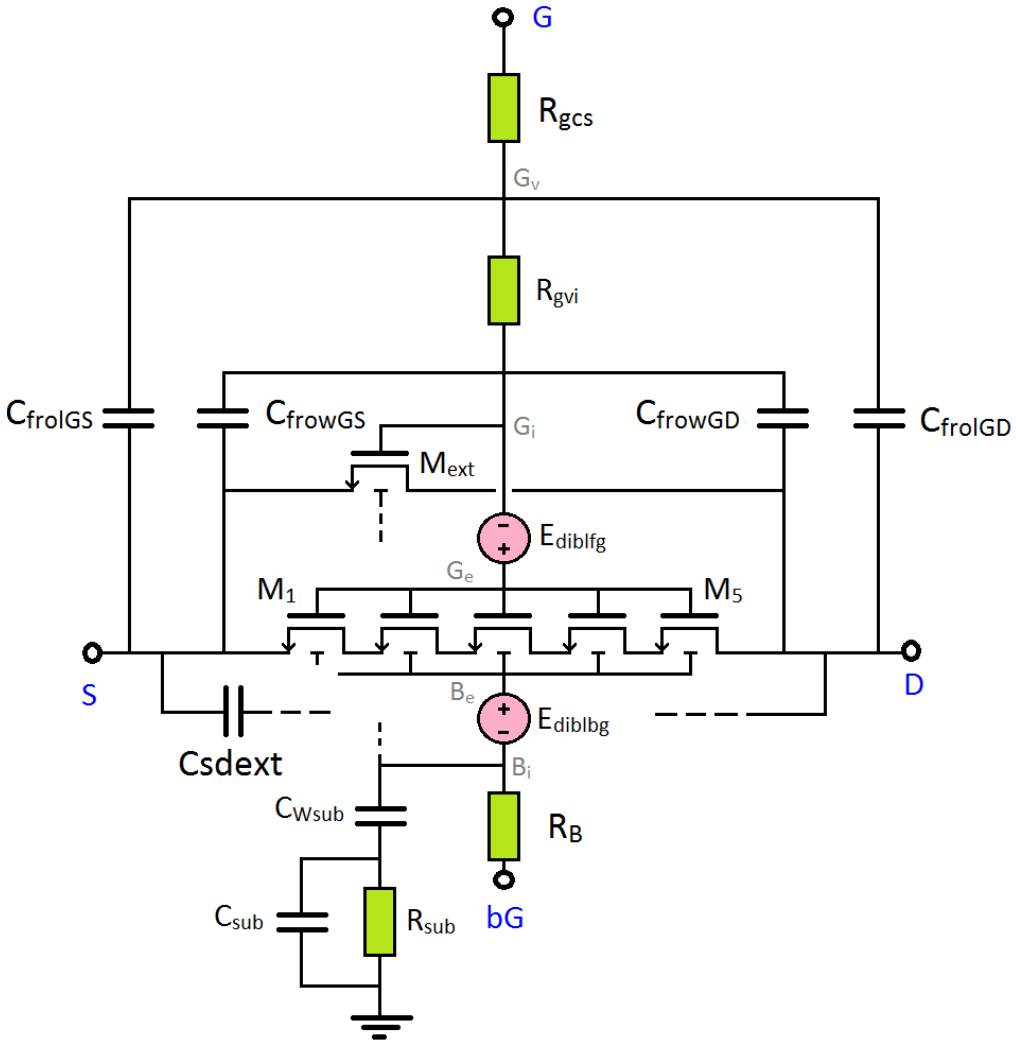

Fig. 4 – Circuit diagram representation of the _rfseg device sub-circuit.

DC Operating Point Information

Operating Point (OP) information is a set of parameters usually provided by SPICE simulators describing a device in steady-state condition. For a MOSFET, the information represents the unique equilibrium state at which the transistor settles when related bias conditions (i.e. DC voltages or currents) are held constant. The OP information is including terminal voltages and currents as well as small signal low frequency parameters (e.g. g_m, g_{ds}, C_{gd} and C_{gs}). The DC OP analysis is an intermediate step towards further simulator analysis (e.g. AC, Transient, and Noise).

The DC OP information is used by analog designers for sizing purposes, in particular to know the state of the transistor and its operation regime. The feature is convenient in providing quickly the required information within the circuit context, without the need for characterizing the device separately. The OP Info feature was proposed in early SPICE simulators and has not changed since.

DC OP parameters are provided to the designer in different formats. The commonly used one is the customized selection on the schematic view (drain current I_D, V_{TH}…) depicted in Fig. 5.

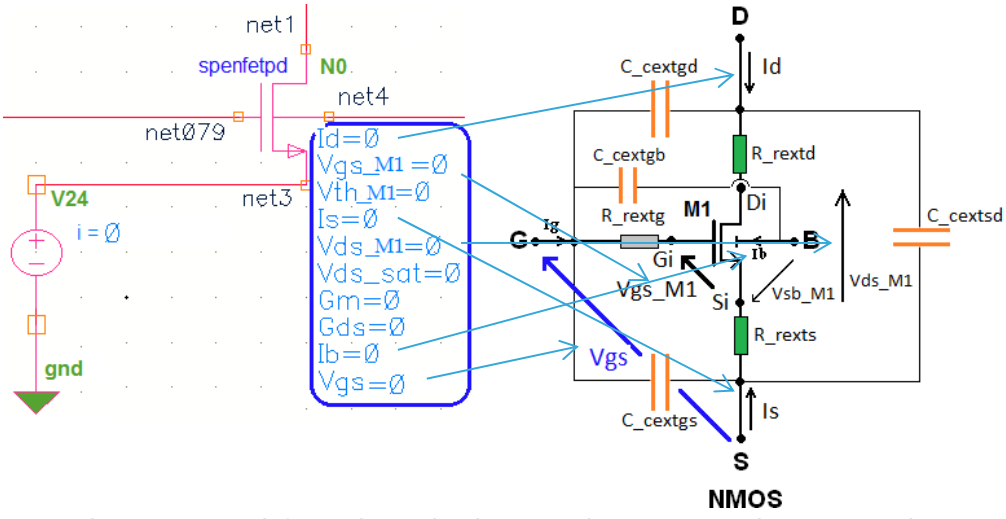

Fig. 5 – DC OP information or back-annotation correspondence example.

I. Classical DC OP Information limitations

In DC simulation, the classical OP information provided by circuit simulators only represents elementary components (i.e. intrinsic or core MOSFET, parasitic resistors and capacitors, etc.) separately. As the majority of RF MOSFET models are implemented using sub-circuits with various elements as explained earlier, almost no accurate information is retrieved for such complex RF devices based on simulators outputs. Moreover, simulators provide some parameters such as C_{gs} broken down into its components (i.e. overlap capacitance, fringe capacitance, etc.). For bulk PSP standard model for instance, simulators provide more than 200 parameters as the OP information while executing a simple operating point analysis. The majority of these parameters are useless for analog designers and most likely important for model developers. Therefore, designers run separate simulations to extract reliable information regarding steady-state conditions while working with RF MOSFETs. These attempts to find accurate OP information most likely distract designers from their design job.

Fig. 6 shows a simplified sub-circuit example of a RF MOSFET device with an external front gate resistor, series source and drain resistors and extrinsic capacitors. If DC V_{GS} and V_{DS} voltages are applied to the gate and drain terminals respectively while source and bulk / back gate are grounded, SPICE simulator provides OP information regarding all sub-circuit components separately (i.e. C_{gs} and V_{TH} of MOSFET M_1, R_S, C_{gse}, etc.). The voltage drop between the internal MOSFET terminals G_i and S_i is different from the real V_{GS} applied to the device. Thus, the threshold voltage provided by existing simulators for M_1 at the given V_{DS} voltage is not accurate. Moreover, the C_{gs} capacitance of the real device is not retrieved by a sum of the intrinsic and the extrinsic capacitance, as the R_s resistor is separating the two capacitors even at low frequency. Fig. 7 shows an example of comparison between the DC OP information C_{gs} provided by major SPICE simulators (namely ELDO from Mentor Graphics, SPECTRE from Cadence, HSPICE from Synopsys, and ADS from Keysight), compared to the extracted one. If the device is biased in same conditions within a circuit, the impedance between the gate and source terminals will have an imaginary part equal to the extracted values, and using the simulators information the designer is misled.

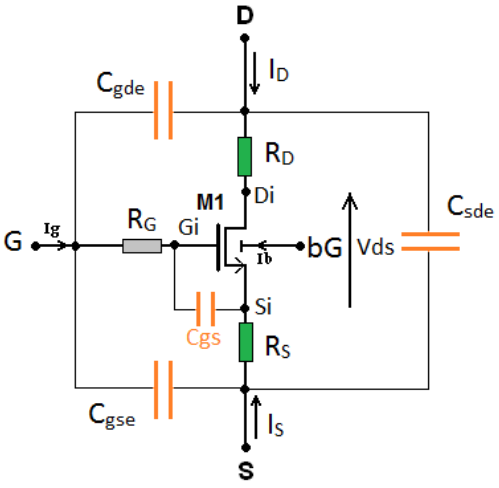

Fig. 6 - A simplified sub-circuit example of a RF MOSFET (bG = back Gate).

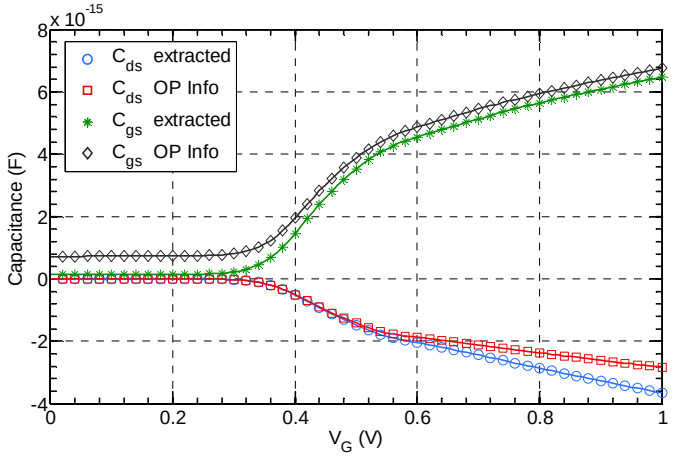

Fig. 7 - Comparison of OP Info capacitances and extracted counterparts in saturation V_{DS} = 1 V for NMOS (L = 1 µm and W = 0.5 µm).

In General, while simulating foundry customized sub-circuits such as the ones presented in the first section of this document (ST 28FDSOI MOSFETs), the DC Operating Point information provided by circuit simulators is not representative of these sub-circuits. However, if the two following conditions are satisfied, sub-circuit simulations might provide accurate DC operating point information:

- Only one main[5] compact model (spice entity) is used in the sub-circuit description (i.e. for RF distributed MOSFETs for example the dc OP information is not meaningful).

[5] Main compact model simulates principal device characteristics. Other device models might be added within a sub-circuit to simulate parasitic contributions.

- MOSFET figures of merit (V_{TH}, g_m, g_{ds}, Currents, Voltages, Capacitances...) can be recalculated using analytical expressions of the main MOS model parameters and parasitic components.

All DC Operating point output information is completely retrieved in the following cases for _acc models:

- SWRG=0 and PRE_LAYOUT_LOCAL=0
- SWRG=0 (default) and PRE_LAYOUT_LOCAL=2

Consequently DC OP information in these two cases accurately represents the whole _acc device (sub-circuit).

In addition to the DC OP information limitations explained above, DC OP outputted parameters don't take into account the dynamic part of self-heating effect (C_{th} effect is neglected). Consequently, in case self-heating effect is enabled (SWSHE=1), MOSFET capacitances provided in DC OP information are only taking into account thermal resistance effect although C_{th} effect is still a minor effect..

II. DC OP Information enhancement (using dedicated simulator option)

A survey of various design groups within STMicroelectronics was carried out in order to define the required DC OP information for analog design. The ST specification has been implemented in major simulators and requires dedicated simulator options (e.g. STD_OP option in ELDO) which is enabled by default within the Design Kit environment. The specification is also proposed to the Compact Model Coalition (CMC) for standardization in order to avoid using the simulators options. The proposed list is shown in Table II-1, and includes a restricted set of MOSFET FoMs. This specification can be applied to various existing logic and analog MOSFETs with 4 terminals (i.e. a source, a drain, a front gate, and a back gate or a bulk terminal) in several technologies (i.e. bulk, SOI, etc.). The specification is based on the following conventions:

1. MOSFET Drain and Source terminals determination convention

MOSFET source and drain terminals used in DC OP Information are defined according to the bias conditions applied:

- For NMOS: first terminal is drain and third terminal is source if $V_{DS} > 0$. First terminal is Source and third terminal is Drain if $V_{DS} < 0$.
- For PMOS: first terminal is Drain and third terminal is source if $V_{SD} > 0$. First terminal is Source and third terminal is Drain if $V_{SD} < 0$.

These assumptions are considered in DC OP parameters calculation in Table II-1.

WARNING: source and drain terminals used in DC OP definition might be different from the terminals specified in the Spice netlist. Source and drain might be swapped (i.e. NMOS with $V_{DS} < 0$).

2. Currents and Voltages sign conventions

DC OP currents definition is based on usual Spice convention: currents flowing into the device terminals are positive (negative if going out).

In Spice, voltages are given as follows: $V_{GS} = V_G - V_S$, $V_{DS} = V_D - V_S$, $V_{SB} = V_S - V_B$ ("S" and "D" are the source and the drain determined following previous bias based convention). Voltages are following Spice convention for NMOS (Vab = Va – Vb). However, for PMOS type, the voltages are defined in a way to have same signs as the corresponding biased NMOS (example: V_{GS} is given as $V_S - V_G$).

Table II-1 Operating Point information restricted list proposal for analog design (B = bG).

Name	Unit	Formulation	Description
Total currents			
I_D	A	-	Total DC drain current: - flowing into drain terminal for NMOS - flowing out of drain terminal for PMOS
I_G	A	-	Total DC gate current: - flowing into gate terminal for NMOS - flowing out of gate terminal for PMOS
I_S	A	-	Total DC source current:

			- flowing into source terminal for NMOS - flowing out of source terminal for PMOS
I_B	A	-	Total DC bulk current: - flowing into bulk terminal for NMOS - flowing out of bulk terminal for PMOS
Applied DC voltages			
V_{GS}	V	NMOS: $V_{GS} = V_G - V_S$ PMOS: $V_{GS} = V_S - V_G$	External gate-source DC voltage (with NMOS convention)
V_{DS}	V	NMOS: $V_{DS} = V_D - V_S$ PMOS: $V_{DS} = V_S - V_D$	External drain-source DC voltage (with NMOS convention)
V_{SB}	V	NMOS: $V_{SB} = Vs - V_B$ PMOS: $V_{SB} = V_B - V_S$	External source-bulk DC voltage (with NMOS convention)
Transconductances & MOSFET Conductance			
g_m	A/V	$\partial(I_D)/\partial(V_G)$	DC transconductance
g_{mb}	A/V	$\partial(I_D)/\partial(V_B)$	DC bulk or back gate transconductance
g_{ds}	A/V	$\partial(I_D)/\partial(V_D)$	DC output conductance
MOSFET Transcapacitances			
C_{gd}	F	$-\partial(Q_G)/\partial(V_D)$	AC Gate-Drain transcapacitance, including overlap capacitances
C_{gs}	F	$-\partial(Q_G)/\partial(V_S)$	AC Gate-Source transcapacitance, including overlap capacitances
C_{gb}	F	$-\partial(Q_G)/\partial(V_B)$	AC Gate-Bulk transcapacitance
C_{ds}	F	$-\partial(Q_D)/\partial(V_S)$	AC Drain-Source transcapacitance
C_{dg}	F	$-\partial(Q_D)/\partial(V_G)$	AC Drain-Gate transcapacitance
C_{db}	F	$-\partial(Q_D)/\partial(V_B)$	AC Drain-Bulk transcapacitance
C_{sd}	F	$-\partial(Q_S)/\partial(V_D)$	AC Source-Drain transcapacitance
C_{sg}	F	$-\partial(Q_S)/\partial(V_G)$	AC Source-Gate transcapacitance
C_{sb}	F	$-\partial(Q_S)/\partial(V_B)$	AC Source-Bulk transcapacitance
C_{bd}	F	$-\partial(Q_B)/\partial(V_D)$	AC Bulk-Drain transcapacitance
C_{bg}	F	$-\partial(Q_B)/\partial(V_G)$	AC Bulk-Gate transcapacitance
C_{bs}	F	$-\partial(Q_B)/\partial(V_S)$	AC Bulk-Source transcapacitance
MOSFET Capacitances			
C_{gg}	F	$\partial(Q_G)/\partial(V_G)$	AC Gate capacitance (including overlap)
C_{dd}	F	$\partial(Q_D)/\partial(V_D)$	AC Drain capacitance
C_{ss}	F	$\partial(Q_S)/\partial(V_S)$	AC Source capacitance
C_{bb}	F	$\partial(Q_B)/\partial(V_B)$	AC Bulk capacitance
Derived parameters			
V_{TH}	V	-	Threshold voltage: should represent V_{GS} at the onset of strong inversion in the MOSFET channel taking into account self-heating.
V_{TH_drive}	V	$V_{GS} - V_{TH}$	Effective gate drive voltage including back bias, drain bias effects and self-heating.
V_{DSAT}	V	$2/ (g_m/I_D)$	Drain saturation voltage
V_{DSAT_marg}	V	$V_{DS} - V_{DSAT}$	V_{DS} voltage margin
Self_gain	-	g_m/g_{ds}	MOSFET self-gain

R_{out}	Ohm	$1/g_{ds}$	AC output resistance
B_{eff}	A/(V*V)	$2*abs(I_D)/(V_{TH\_drive})^2$	Gain factor in saturation
f_T	Hz	$g_m/[2*\pi*C_{gg}]$	Transit frequency or unity current gain frequency
R_{gate}	Ohm	-	Total MOSFET gate resistance
Gmoverid	1/V	g_m/I_D	g_m over I_D
V_{EARLY}	V	$abs(I_D)/g_{ds}$	Equivalent Early voltage
Tk	K	-	MOSFET device temperature
Dtsh	K	-	MOSFET device temperature increase due to self-heating

Recently, a practical solution has been proposed in the simulator side for all MOSFET types in such a way that the standard elementary information is replaced by the accurate (advanced) equivalent one.

III. Advanced DC OP Information

Having the specification of the OP information defined, the issues/limitations regarding sub-circuit based devices can be tackled conveniently. An advanced feature is proposed to mitigate the classical DC OP information limitations. This advanced feature is present in latest simulators versions and related frameworks as depicted in Fig. 8 for ELDO.

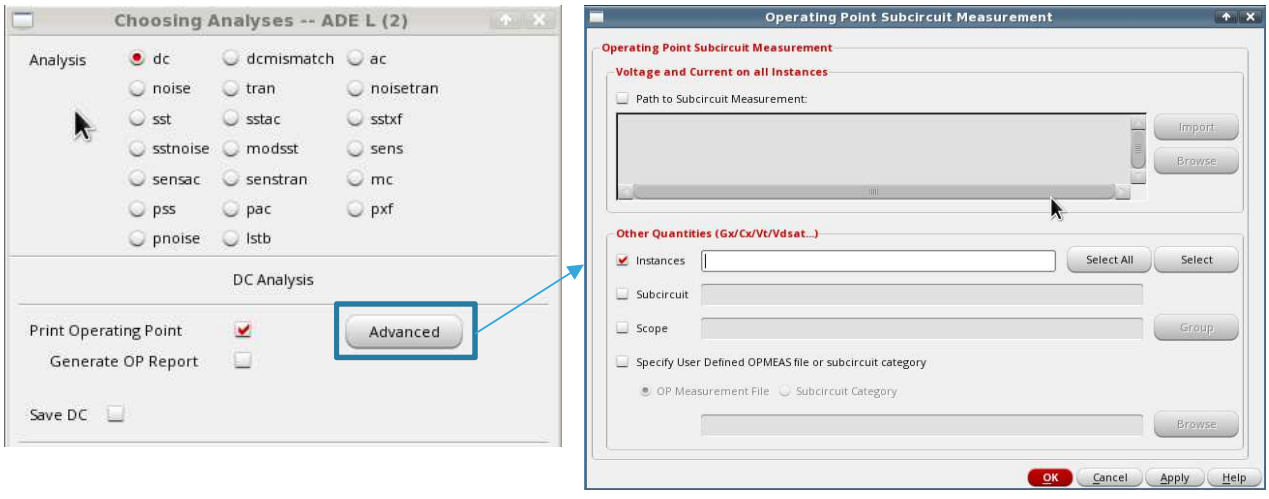

Fig. 8 - Advanced DC OP Information proposal.

In the advanced DC OP Information feature, the sub-circuit based device is considered as a black box MOSFET with 4 terminals. The simulator isolates the device

from its context (i.e. original circuit) and runs, in background, specific simulations on it, while keeping same bias conditions. Then, simulator provides the extracted FoMs (i.e. list of Table II-1) as a replacement of the detailed classical FoMs in the same output files and formats.

As detailed in the dedicated section of the simulator manual, the advanced feature requires an input file linking the foundary subckt elements to the method used for DC OP information extraction. Extraction methods are defined in a dedicated format and an example is given in the model package of this Design Kit (e.g. Nopmeas.ex file).

The cost of the proposed feature is some additional simulation CPU time (tens of milliseconds per device). However, the feature is only required in analog circuits where only a few devices need to be sized and their OP information to be accurately known. Consequently, in classical analog circuits, the additional CPU time is negligible and acceptable as a cost for accurate OP information.

The background specific simulation involves DC and AC analysis types, and is run using the isolated device. The DC simulation is a simple sweep of V_{GS} in order to extract the threshold voltage at a constant predefined current density. Three other V_{TH} definitions can also be used:

- g_{m_max} based method where a linear extrapolation on I_D-V_{GS} characteristic from the maximum g_m location is used.
- maximum $\delta C_{gs}/\delta V_{gs}$ based method originating from a unified charge-control MOSFET model.
- maximum $\delta(g_m/I_D)/\delta V_{gs}$ based method proposed in bulk.

The small signal AC simulation, with an applied small signal having a unit magnitude, is run at a default low frequency of 100 kHz, which can be modified by the user. Four instances of the same device are used with a small signal applied on each terminal in order to retrieve the 16 capacitances, the conductance, and the transconductance. The corresponding formulations are:

$$C_{xy} = \frac{\partial Q_x}{\partial V_y} = \frac{Im(i_x)}{|v_y|} = Im(i_x), \quad x \neq y$$
$$C_{xx} = -\frac{\partial Q_x}{\partial V_x} = -\frac{Im(i_x)}{|v_x|} = -Im(i_x), \quad x = y \qquad \text{(III.1)}$$

where C_{xy} and C_{xx} are, respectively, the transcapacitances between x and y terminals and capacitance at terminal x. $Im(i_x)$ is the imaginary part of the AC current at terminal x, and v_y is the AC voltage applied at terminal y with a magnitude of 1.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = -\frac{real(i_d)}{|v_g|} = -real(i_d), \qquad AC\ applied\ to\ gate$$
$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = -\frac{real(i_d)}{|v_b|} = -real(i_d), \qquad \text{(III.2)}$$
$$AC\ applied\ to\ bulk\ or\ back\ gate$$

where $V_{BS} = V_{bG}$ in the case of DG MOSFET.

$$g_{ds} = \frac{\partial I_D}{\partial V_{GS}} = -\frac{real(i_d)}{|v_d|} = -real(i_d), \qquad AC\ applied\ to\ drain \qquad \text{(III.3)}$$

In SI, the saturation voltage is estimated using:

$$V_{DSATSI} = \frac{2}{\left(\frac{g_m}{I_D}\right)} \qquad \text{(III.4)}$$

(III.4) is used to estimate V_{DSAT} for two geometries L = 2 µm and L = 100 nm. The result is shown in Fig. 9 and Fig. 11, respectively. For the long channel with less velocity saturation (L = 2 µm), the expression provides close results in SI to the definition of V_{DSAT} proposed by Leti-UTSOI2. This is also evidenced in Fig. 10 using I_D-V_{DS} output characteristic. For WI, the expression underestimates the V_{DSAT}, and a correction can be proposed in this region of operation:

$$V_{DSATWI} = \frac{3}{\left(\frac{g_m}{I_D}\right)} \approx 3U_T \qquad \text{(III.5)}$$

For short channel (e.g. L = 100 nm), the proposed SI expression provides lower V_{DSAT} values as shown in Fig. 11 but still acceptable for the onset of saturation. Expression (III.4) provides acceptable values for onset of saturation region.

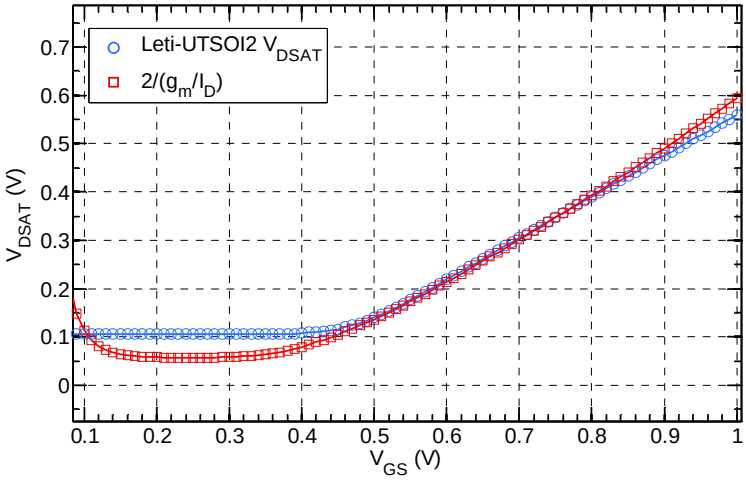

Fig. 9 - Comparison of the Leti-UTSOI2 and $2/(g_m/I_D)$ expression V_{DSAT} values versus V_{GS} in saturation for NMOS and L = 2µm.

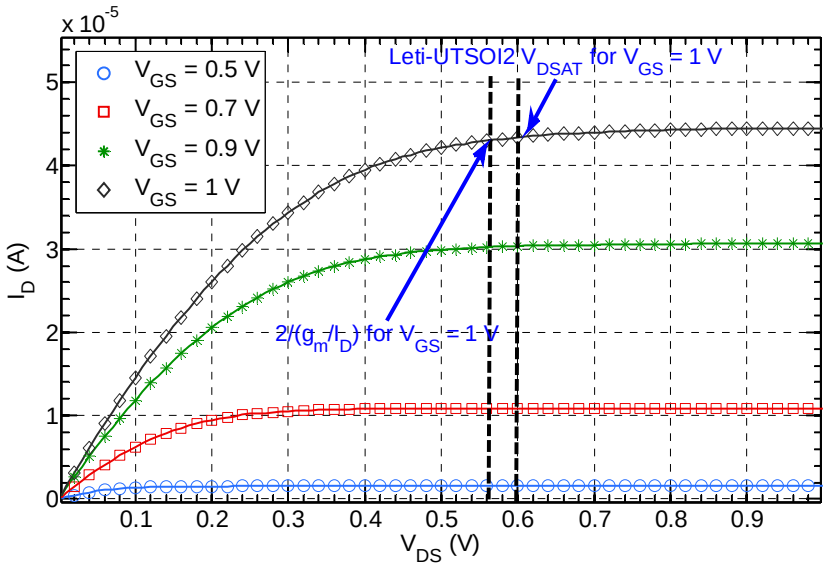

Fig. 10 - $I_D - V_{DS}$ characteristics for various V_{GS} and L = 2 µm showing two V_{DSAT} definitions (Leti-UTSOI2 and $2/(g_m/I_D)$ expression).

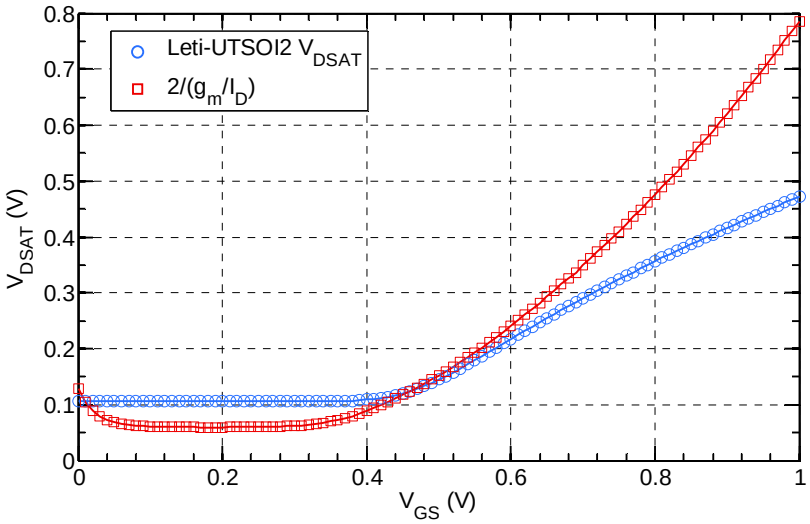

Fig. 11 - Comparison of the Leti-UTSOI2 and $2/(g_m/I_D)$ expression V_{DSAT} values versus V_{GS} in saturation for NMOS and L = 100 nm.

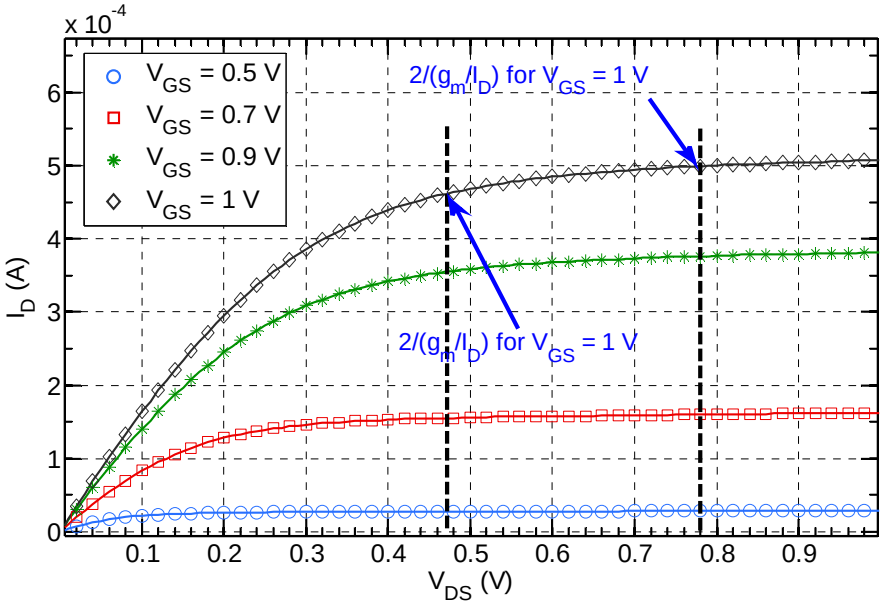

Fig. 12 - I_D – V_{DS} characteristics for various V_{GS} and L = 100 nm showing two V_{DSAT} definitions (Leti-UTSOI2 and $2/(g_m/I_D)$ expression).

The advanced DC OP information has been proposed to the main EDA vendors, namely Mentor Graphics, Synopsys and Cadence, and is already implemented in recent simulators versions for ELDO (production), and Hspice / Spectre (beta).

Small signal (AC) equivalent circuit

UTBB FDSOI small-signal equivalent schematic valid in low-frequency operation is depicted in Fig. 13. It includes intrinsic MOSFET components such as the front transconductance g_{m1} and extrinsic elements such as source and drain series resistances (i.e. R_S and R_D, respectively). The explicit series resistances shown in Fig. 13 are taken into account in UTSOI2 implicitly in the mobility reduction saving some CPU time during circuit simulations as two circuit nodes are skipped. Gate-to-source (C_{gs}), gate-to-drain (C_{gd}) and front-to-back gates (C_{gb}) capacitances are also included as shown in Fig. 13. It should be noted that the equivalent circuit elements (i.e. capacitances and resistances) include both intrinsic and extrinsic parts. It is important to distinguish between the intrinsic (denoted by 'i') and extrinsic (denoted by 'e') contributions that have different origins. The intrinsic part is related to the device itself and mainly useful for channel current modulation, while the extrinsic part is related to parasitic elements unnecessary for the device operation. The extrinsic part can be optimized using proper layout technics such as multi-finger layout but cannot be completely removed. At high frequency operation the extrinsic elements gain particular importance and must be carefully modeled. At mm-Wave operation, these parasitic elements can even dominate the device performance.

The small-signal equivalent circuit depicted in Fig. 13 is frequently used in the literature to model small-signal operation of the MOSFET. This circuit was first proposed by Meyer in early semiconductor modeling life and enriched gradually. It represents the main channel modulation effect through g_m along with the coupling effects of other terminals on MOSFET gate terminal through the three capacitances C_{gs}, C_{gd} and C_{gb}. All the coupling effects represented in this equivalent circuit are extracted and validated under quasi-static operation. The quasi-static operation is defined when an applied small signal varies sufficiently slowly that the carriers in the channel can follow the variation simultaneously.

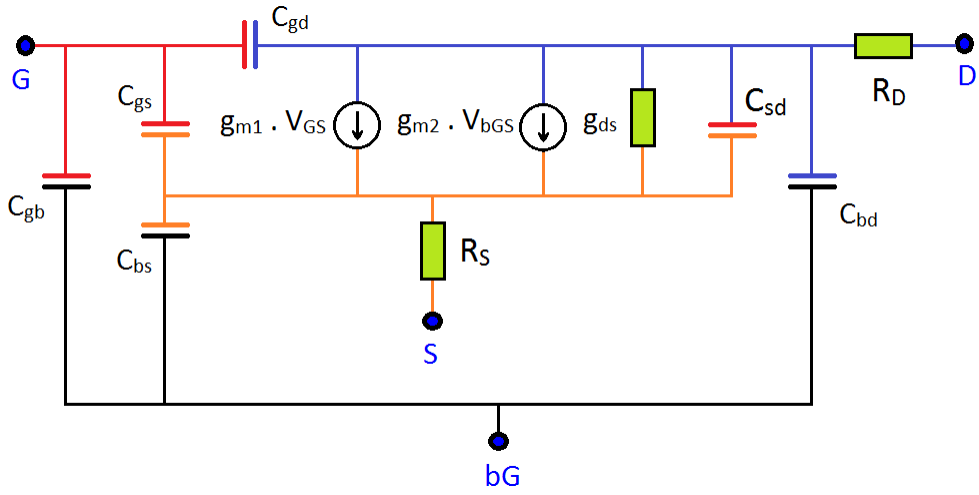

Fig. 13 - Equivalent schematic for small signal and low-frequency operation of the UTBB FDSOI including series resistances R_S and R_D ($C_{gd} = C_{gdi} + C_{gde}$ and $C_{gs} = C_{gsi} + C_{gse}$).

It is important not to associate the 16 capacitances presented in the previous section table (DC OP information parameters list) with any parallel plate structures in the MOSFET architecture. All 16 capacitances are values of fictitious capacitors used for device charge conservation.

One should also be careful while using the simple equivalent circuit in Fig. 13. Besides the lack of charge conservation in this equivalent circuit, it is only valid within the following assumptions:

- Transistor is used for amplification with the input signal entering to the gate terminal. The equivalent circuit cannot and should not be used to model a switch operation.
- The transistor configuration is common-source (CS).
- The coupling effect between drain and gate terminals is reciprocal which is rarely verified in saturation. In other words, one should verify that:

$$\frac{\partial Q_g}{\partial V_D} = \frac{\partial Q_d}{\partial V_G} \qquad \text{(III.6)}$$

The last assumption is equivalent to assuming $C_{gdi} = C_{dgi}$ and it is important but not always verified even at low frequency operation as shown in Fig. 14. In saturation for example, a variation of the drain terminal voltage will not produce any change on the

gate terminal charge because of pinch-off and consequently the intrinsic capacitance is equal to zero $C_{dgi} = 0$. However, a variation of the gate terminal voltage will produce a variation on the channel charge, which will produce a variation on drain charge through channel conduction, and thus $C_{dgi} \neq 0$. Fig. 14 shows the gate to drain transadmittance Y_{21} defined as the ratio of the two complex phasors representing the small current at the drain terminal and the small voltage at the gate terminal. Y_{21} expression is given by:

$$Y_{21} \equiv \left.\frac{\widehat{I_D}}{\widehat{V_G}}\right|_{V_i=0, i\neq G} \qquad \text{(III.7)}$$

Because of the reciprocal drain-gate capacitance in Fig. 13, the simple equivalent circuit provides different results compared to a compact model where charge conservation is verified. The difference is even observed at low frequency and is maximum at high frequency. Therefore, the difference between the two capacitances C_{gdi} and C_{dgi} must be taken into account and modeled. At high frequency operation the reciprocal C_{gdi} and C_{dgi} assumption is no more valid and these two coupling quantities diverge more because of non-quasi-static effects.

In general, the electrostatic couplings between the MOSFET terminals are not reciprocal, and for the dynamic operation modeling, 16 transcapacitances are required to agree with the charge conservation rule. Recent MOSFET compact models such as Leti-UTSOI2 account for the charge conservation, and the 16 transcapacitances are provided as part of the simulators DC OP information.

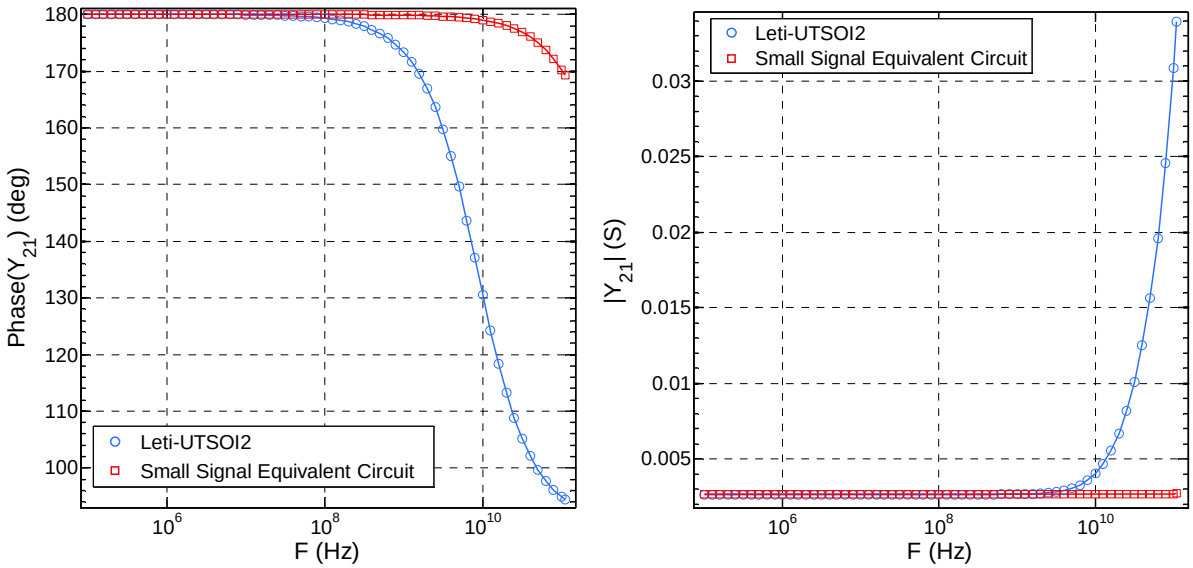

Fig. 14 - NMOS gate to drain transadmittance phase (left) and module (right) simulated using Leti-UTSOI2 and the small signal equivalent circuit in Fig. 13. L = 1 µm, W = 10 µm, N_F = 10, and V_{GS} = V_{DS} = 1 V.

The modeling of the non-reciprocal C_{gd} and C_{dg} capacitances effect can be done by adding an imaginary part C_m to the transconductance g_m (i.e. in parallel to it in an equivalent circuit). The proposed equivalent circuit is augmented using a mutual capacitance between the drain and the source terminals. The mutual capacitance is defined as:

$$C_m = \frac{\partial Q_d}{\partial V_G} - \frac{\partial Q_g}{\partial V_D} = C_{dg} - C_{gd} \qquad \text{(III.8)}$$

The new quasi static equivalent circuit is shown in Fig. 15 including series drain and source resistors. It should be noted that C_{sd} is included when required in particular for short channels. In saturation, the new equivalent circuit provides strictly the same results as the Leti-UTSOI2 model as shown in Fig. 16.

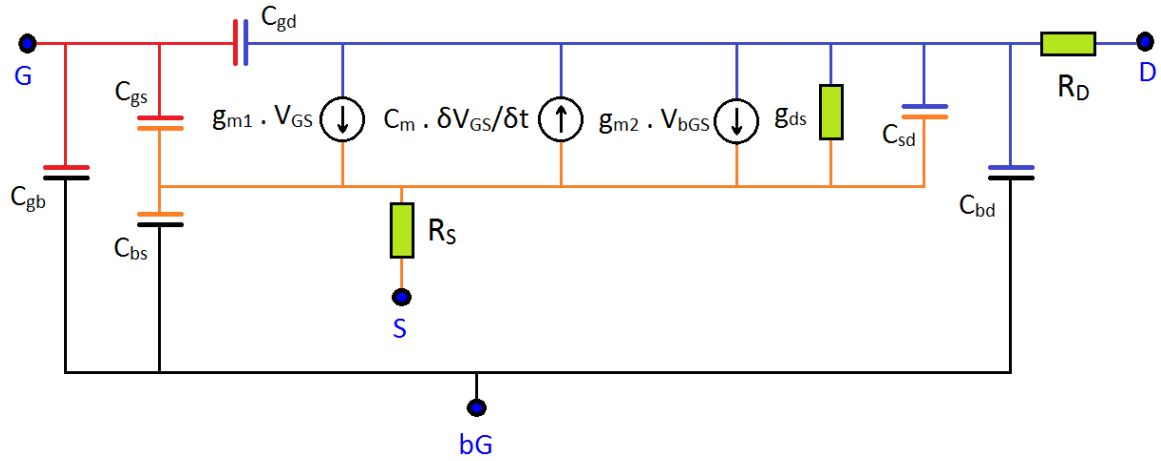

Fig. 15 - Equivalent schematic for small signal and quasi-static operation of the UTBB FDSOI MOSFET including series resistances R_S and R_D ($C_{gd} = C_{gdi} + C_{gde}$ and $C_{gs} = C_{gsi} + C_{gse}$).

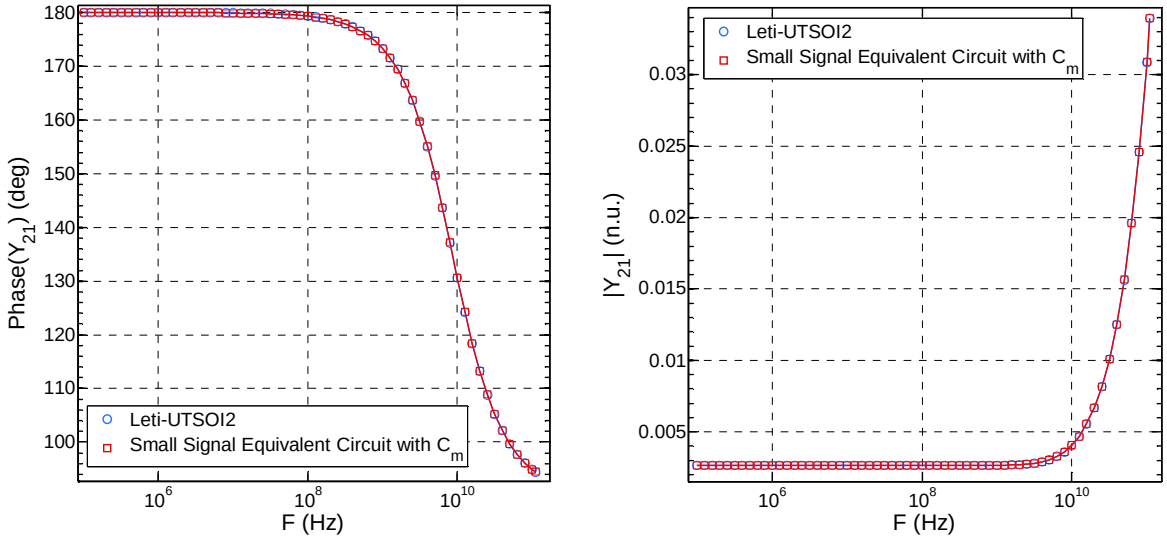

Fig. 16 - NMOS gate to drain transadmittance phase (left) and module (right) simulated using Leti-UTSOI2 and the quasi-static small signal equivalent circuit in Fig. 15. L = 1 µm, W = 10 µm, N_F = 10, and $V_{GS} = V_{DS}$ = 1 V.