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C28SOI_SC_8_COREPBP16_LL Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 16 nm

Overview

- C28SOI_SC_8_COREPBP16_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

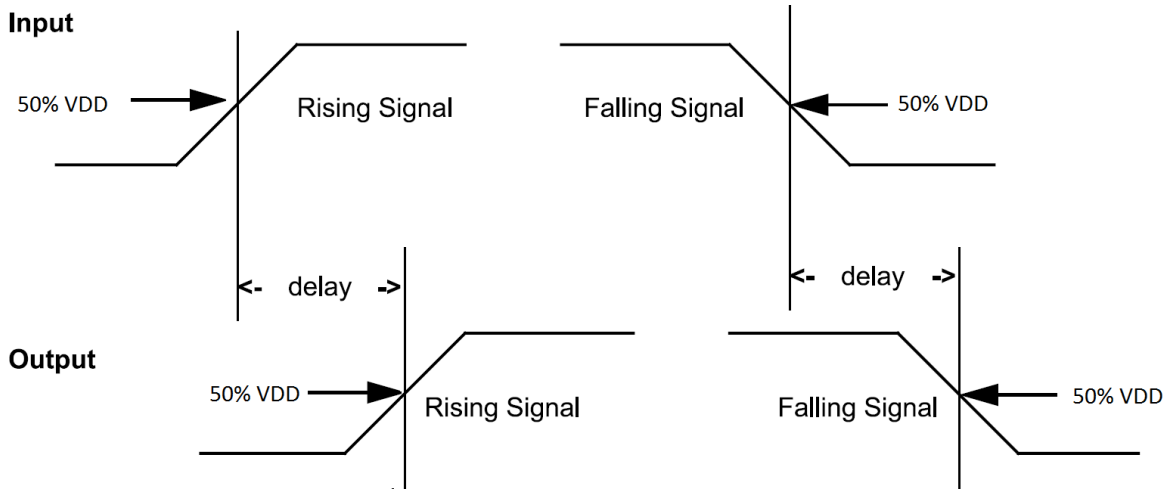


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

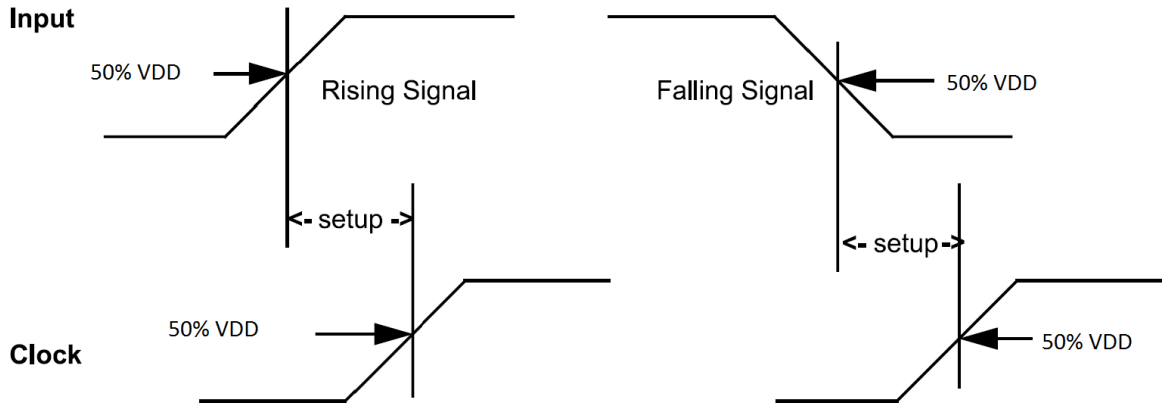


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

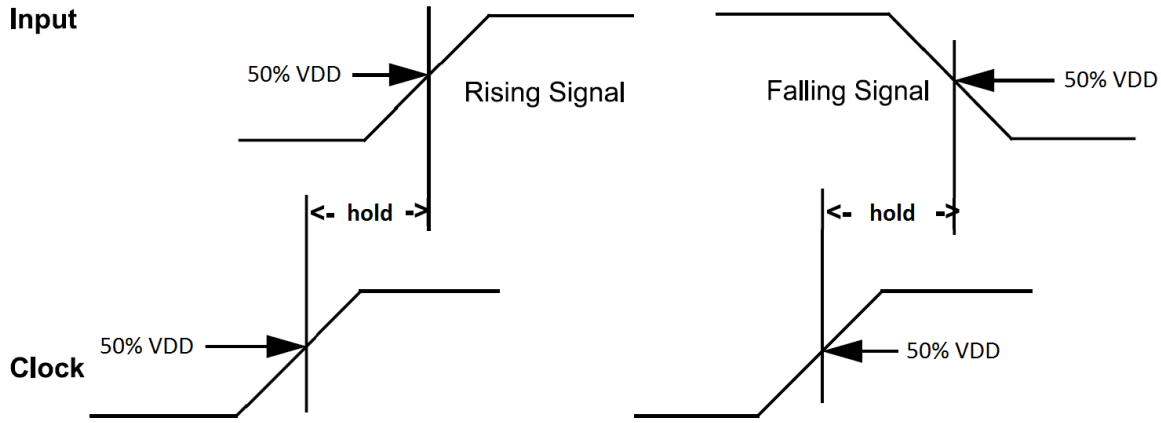


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

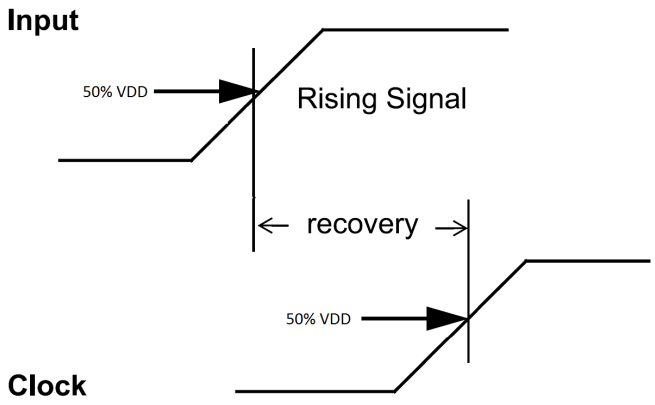


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

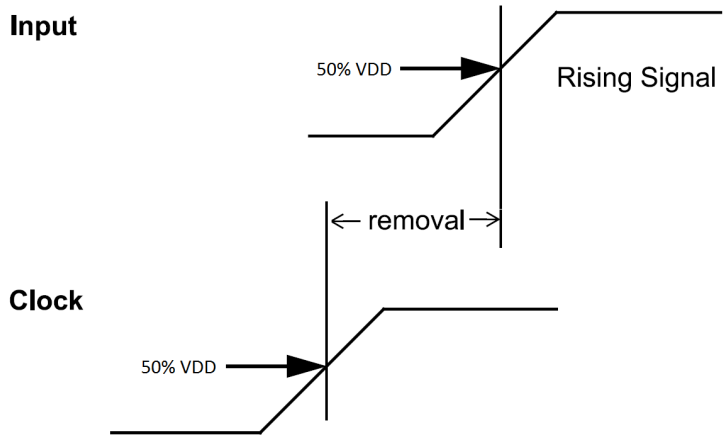


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

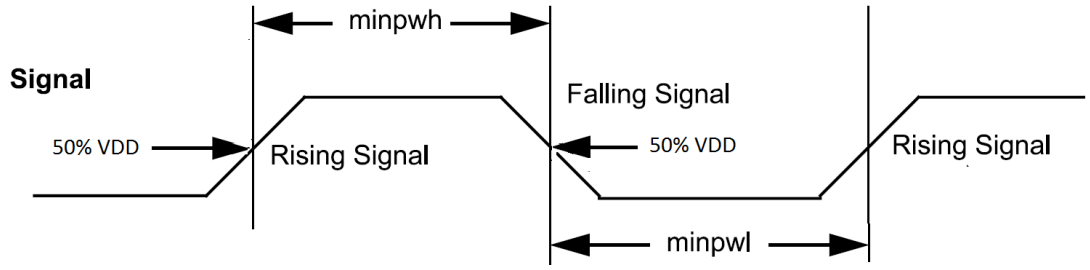


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

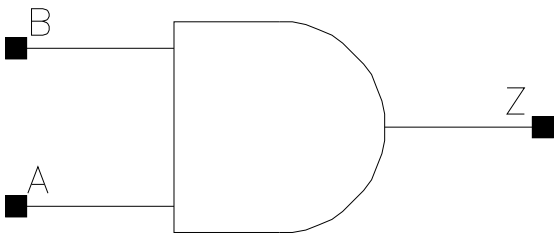
The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description	Logical Symbol
2 input AND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.544	0.4352
X10_P16	0.800	0.680	0.5440
X11_P16	1.600	0.544	0.8704
X19_P16	0.800	1.224	0.9792
X24_P16	0.800	1.360	1.0880
X29_P16	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X11_P16	X19_P16
A	0.0006	0.0009	0.0011	0.0017
B	0.0005	0.0008	0.0010	0.0015
	X24_P16	X29_P16		
A	0.0017	0.0017		
B	0.0015	0.0015		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0292	0.0247	3.1961	1.5267
A to Z ↑	0.0224	0.0216	4.7835	2.3033
B to Z ↓	0.0278	0.0229	3.1953	1.5259
B to Z ↑	0.0244	0.0234	4.7845	2.3015
	X11_P16	**X19_P16**	**X11_P16**	**X19_P16**

A to Z ↓	0.0271	0.0242	1.2282	0.7860
A to Z ↑	0.0202	0.0212	2.2215	1.1614
B to Z ↓	0.0250	0.0230	1.2251	0.7859
B to Z ↑	0.0219	0.0232	2.2215	1.1607
	X24_P16	**X29_P16**	**X24_P16**	**X29_P16**
A to Z ↓	0.0264	0.0281	0.6380	0.5326
A to Z ↑	0.0235	0.0252	0.9310	0.7743
B to Z ↓	0.0254	0.0272	0.6383	0.5328
B to Z ↑	0.0257	0.0275	0.9314	0.7741

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	8.077e-06	1.000e-20
X10_P16	1.744e-05	1.000e-20
X11_P16	1.942e-05	1.000e-20
X19_P16	3.369e-05	1.000e-20
X24_P16	3.915e-05	1.000e-20
X29_P16	4.462e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X11_P16	X19_P16
A (output stable)	7.557e-06	1.428e-05	1.920e-05	2.810e-05
B (output stable)	1.871e-05	3.409e-05	4.663e-05	6.918e-05
A to Z	2.296e-03	3.994e-03	4.742e-03	7.890e-03
B to Z	2.179e-03	3.796e-03	4.431e-03	7.482e-03
	X24_P16	X29_P16		
A (output stable)	2.819e-05	2.819e-05		
B (output stable)	6.927e-05	6.934e-05		
A to Z	9.716e-03	1.139e-02		
B to Z	9.324e-03	1.102e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

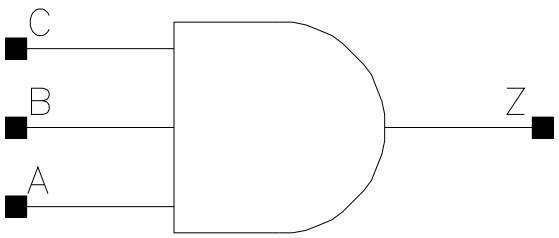
Pin Cycle (vdds)	X5_P16	X10_P16	X11_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P16	X29_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.680	0.5440
X10_P16	0.800	0.816	0.6528
X14_P16	0.800	1.360	1.0880
X19_P16	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0006	0.0009	0.0014	0.0017
B	0.0005	0.0008	0.0012	0.0016
C	0.0005	0.0008	0.0012	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0329	0.0276	3.2318	1.5380
A to Z ↑	0.0298	0.0284	4.8432	2.3338
B to Z ↓	0.0319	0.0261	3.2305	1.5364
B to Z ↑	0.0311	0.0294	4.8364	2.3308
C to Z ↓	0.0303	0.0246	3.2287	1.5343
C to Z ↑	0.0327	0.0305	4.8422	2.3327
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0277	0.0265	1.0625	0.7886

A to Z ↑	0.0272	0.0269	1.5840	1.1724
B to Z ↓	0.0262	0.0250	1.0614	0.7876
B to Z ↑	0.0283	0.0280	1.5827	1.1725
C to Z ↓	0.0248	0.0235	1.0599	0.7870
C to Z ↑	0.0296	0.0291	1.5832	1.1721

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	7.870e-06	1.000e-20
X10_P16	1.707e-05	1.000e-20
X14_P16	2.440e-05	1.000e-20
X19_P16	3.333e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	1.018e-05	1.975e-05	2.639e-05	3.568e-05
B (output stable)	2.356e-05	4.649e-05	6.431e-05	9.051e-05
C (output stable)	5.399e-05	1.044e-04	1.506e-04	2.154e-04
A to Z	2.683e-03	4.644e-03	6.831e-03	8.977e-03
B to Z	2.562e-03	4.427e-03	6.497e-03	8.527e-03
C to Z	2.450e-03	4.218e-03	6.190e-03	8.087e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

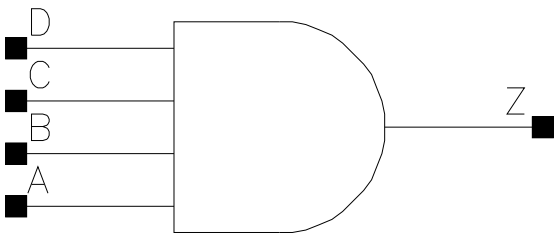
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.088	0.8704
X3_P16	0.800	1.088	0.8704
X10_P16	0.800	2.176	1.7408
X13_P16	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P16	X3_P16	X10_P16	X13_P16
A	0.0006	0.0006	0.0013	0.0015
B	0.0006	0.0005	0.0013	0.0015
C	0.0005	0.0005	0.0012	0.0015
D	0.0006	0.0006	0.0012	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	X3_P16	X2_P16	X3_P16
A to Z ↓	0.0259	0.0280	5.7049	3.8598
A to Z ↑	0.0253	0.0254	15.5094	8.4644
B to Z ↓	0.0240	0.0267	5.7090	3.8624
B to Z ↑	0.0269	0.0274	15.5169	8.4675
C to Z ↓	0.0262	0.0285	5.7082	3.8651
C to Z ↑	0.0249	0.0250	15.5333	8.4783

D to Z ↓	0.0246	0.0275	5.7031	3.8679
D to Z ↑	0.0270	0.0279	15.5313	8.4782
	X10_P16	**X13_P16**	**X10_P16**	**X13_P16**
A to Z ↓	0.0271	0.0272	1.3281	0.9901
A to Z ↑	0.0250	0.0272	2.8200	2.1626
B to Z ↓	0.0256	0.0247	1.3284	0.9881
B to Z ↑	0.0267	0.0282	2.8201	2.1632
C to Z ↓	0.0269	0.0258	1.3204	0.9926
C to Z ↑	0.0238	0.0235	2.8180	2.1583
D to Z ↓	0.0243	0.0233	1.3182	0.9903
D to Z ↑	0.0247	0.0245	2.8176	2.1577

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P16	7.332e-06	1.000e-20
X3_P16	9.537e-06	1.000e-20
X10_P16	2.807e-05	1.000e-20
X13_P16	3.798e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P16	X3_P16	X10_P16	X13_P16
A (output stable)	4.978e-04	5.962e-04	1.583e-03	2.113e-03
B (output stable)	4.555e-04	5.495e-04	1.459e-03	1.962e-03
C (output stable)	4.857e-04	5.373e-04	1.410e-03	1.791e-03
D (output stable)	4.425e-04	5.009e-04	1.291e-03	1.637e-03
A to Z	1.812e-03	2.419e-03	6.895e-03	9.274e-03
B to Z	1.698e-03	2.294e-03	6.575e-03	8.647e-03
C to Z	1.806e-03	2.330e-03	6.067e-03	7.620e-03
D to Z	1.693e-03	2.238e-03	5.549e-03	7.003e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

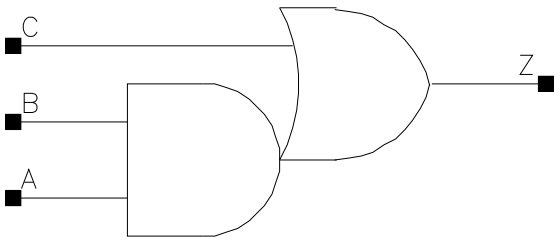
Pin Cycle (vdds)	X2_P16	X3_P16	X10_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	0.952	0.7616
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0005	0.0007	0.0015
B	0.0005	0.0008	0.0013
C	0.0006	0.0008	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0394	0.0356	3.0867	1.5448
A to Z ↑	0.0251	0.0236	4.4832	2.2780
B to Z ↓	0.0368	0.0330	3.0753	1.5383
B to Z ↑	0.0275	0.0259	4.4826	2.2782
C to Z ↓	0.0387	0.0336	3.0700	1.5376
C to Z ↑	0.0245	0.0228	4.4462	2.2616
	X19_P16		**X19_P16**	
A to Z ↓	0.0343		0.8032	
A to Z ↑	0.0259		1.1486	

B to Z ↓	0.0328		0.8034	
B to Z ↑	0.0283		1.1493	
C to Z ↓	0.0331		0.8016	
C to Z ↑	0.0246		1.1386	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	8.956e-06	1.000e-20
X10_P16	1.757e-05	1.000e-20
X19_P16	3.203e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	2.006e-05	4.075e-05	8.690e-05
B (output stable)	2.336e-05	4.858e-05	9.929e-05
C (output stable)	4.336e-05	5.858e-05	1.387e-04
A to Z	2.677e-03	4.586e-03	8.878e-03
B to Z	2.550e-03	4.360e-03	8.566e-03
C to Z	2.893e-03	4.819e-03	9.390e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

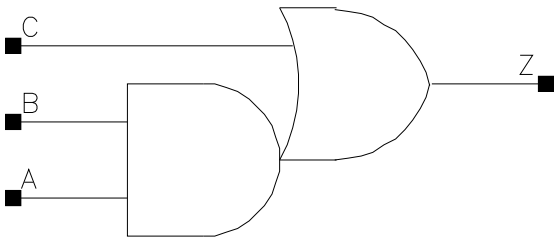
Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	0.952	0.7616
X14_P16	0.800	1.632	1.3056
X19_P16	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0005	0.0008	0.0016	0.0015
B	0.0005	0.0007	0.0015	0.0015
C	0.0006	0.0008	0.0016	0.0016

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0402	0.0359	3.0738	1.5535
A to Z ↑	0.0276	0.0263	4.5630	2.2957
B to Z ↓	0.0381	0.0340	3.0621	1.5524
B to Z ↑	0.0306	0.0287	4.5631	2.2959
C to Z ↓	0.0356	0.0329	3.0531	1.5459
C to Z ↑	0.0211	0.0197	4.5098	2.2718
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0326	0.0352	1.0625	0.7983

A to Z ↑	0.0243	0.0260	1.5624	1.1648
B to Z ↓	0.0292	0.0320	1.0571	0.7944
B to Z ↑	0.0257	0.0276	1.5615	1.1651
C to Z ↓	0.0277	0.0305	1.0546	0.7921
C to Z ↑	0.0172	0.0187	1.5444	1.1504

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	9.000e-06	1.000e-20
X10_P16	1.671e-05	1.000e-20
X14_P16	3.035e-05	1.000e-20
X19_P16	3.473e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	1.117e-05	1.458e-05	4.819e-05	4.821e-05
B (output stable)	1.532e-05	2.024e-05	1.013e-04	1.011e-04
C (output stable)	1.240e-04	1.863e-04	5.244e-04	5.248e-04
A to Z	2.946e-03	4.770e-03	8.146e-03	9.856e-03
B to Z	2.822e-03	4.562e-03	7.451e-03	9.156e-03
C to Z	2.466e-03	4.071e-03	6.493e-03	8.056e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

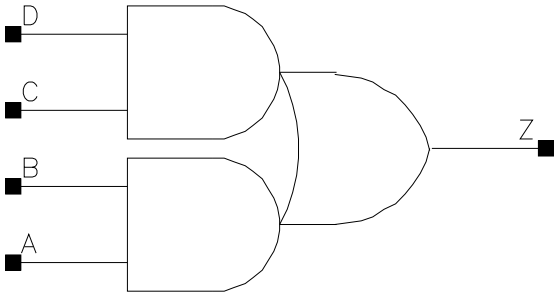
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.088	0.8704
X10_P16	0.800	1.088	0.8704
X14_P16	0.800	1.768	1.4144
X19_P16	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0006	0.0008	0.0016	0.0016
B	0.0006	0.0010	0.0015	0.0014
C	0.0006	0.0008	0.0016	0.0016
D	0.0006	0.0008	0.0015	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0411	0.0359	3.0901	1.5555
A to Z ↑	0.0294	0.0280	4.5991	2.2831
B to Z ↓	0.0375	0.0327	3.0729	1.5481

B to Z ↑	0.0308	0.0297	4.5974	2.2817
C to Z ↓	0.0378	0.0336	3.0761	1.5483
C to Z ↑	0.0245	0.0231	4.5876	2.2750
D to Z ↓	0.0358	0.0317	3.0675	1.5452
D to Z ↑	0.0269	0.0254	4.5853	2.2732
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0324	0.0350	1.0621	0.8013
A to Z ↑	0.0247	0.0265	1.5660	1.1717
B to Z ↓	0.0300	0.0327	1.0604	0.8001
B to Z ↑	0.0269	0.0289	1.5654	1.1712
C to Z ↓	0.0304	0.0332	1.0593	0.7987
C to Z ↑	0.0208	0.0227	1.5598	1.1670
D to Z ↓	0.0283	0.0312	1.0576	0.7974
D to Z ↑	0.0226	0.0247	1.5597	1.1669

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.061e-05	1.000e-20
X10_P16	2.039e-05	1.000e-20
X14_P16	3.405e-05	1.000e-20
X19_P16	3.898e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	2.517e-05	3.365e-05	4.274e-05	4.290e-05
B (output stable)	1.375e-04	1.384e-04	6.372e-05	6.404e-05
C (output stable)	3.200e-05	4.649e-05	1.088e-04	1.090e-04
D (output stable)	3.761e-05	5.991e-05	1.343e-04	1.345e-04
A to Z	3.353e-03	5.352e-03	8.523e-03	1.032e-02
B to Z	3.041e-03	4.891e-03	8.019e-03	9.812e-03
C to Z	2.854e-03	4.594e-03	7.175e-03	8.943e-03
D to Z	2.708e-03	4.381e-03	6.738e-03	8.492e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

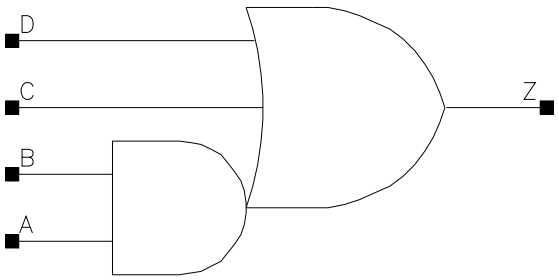
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	1.088	0.8704
X19_P16	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0005	0.0007	0.0014
B	0.0005	0.0008	0.0014
C	0.0006	0.0007	0.0015
D	0.0005	0.0007	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0482	0.0425	3.4156	1.6147
A to Z ↑	0.0259	0.0231	4.7577	2.2919
B to Z ↓	0.0459	0.0394	3.4068	1.6072
B to Z ↑	0.0284	0.0253	4.7547	2.2910
C to Z ↓	0.0490	0.0431	3.4030	1.6082
C to Z ↑	0.0249	0.0318	4.7205	2.2910

D to Z ↓	0.0492	0.0437	3.4048	1.6097
D to Z ↑	0.0247	0.0314	4.7221	2.2902
	X19_P16		**X19_P16**	
A to Z ↓	0.0416		0.8343	
A to Z ↑	0.0253		1.1406	
B to Z ↓	0.0376		0.8297	
B to Z ↑	0.0266		1.1390	
C to Z ↓	0.0414		0.8312	
C to Z ↑	0.0262		1.1327	
D to Z ↓	0.0412		0.8312	
D to Z ↑	0.0258		1.1317	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	7.525e-06	1.000e-20
X10_P16	1.552e-05	1.000e-20
X19_P16	2.900e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	2.447e-05	5.022e-05	1.015e-04
B (output stable)	2.530e-05	5.187e-05	1.267e-04
C (output stable)	2.112e-05	3.801e-05	8.014e-05
D (output stable)	2.366e-05	4.394e-05	8.565e-05
A to Z	2.830e-03	4.873e-03	9.459e-03
B to Z	2.707e-03	4.618e-03	8.779e-03
C to Z	3.153e-03	5.599e-03	1.054e-02
D to Z	3.000e-03	5.327e-03	9.938e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

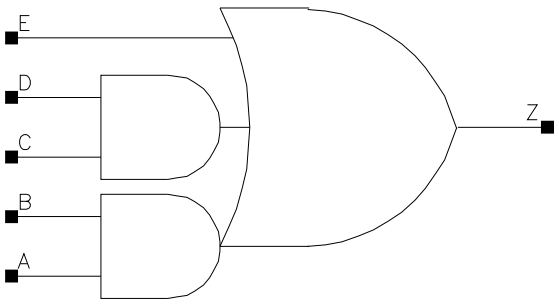
Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.088	0.8704
X10_P16	0.800	1.224	0.9792
X19_P16	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0005	0.0008	0.0015
B	0.0005	0.0008	0.0013
C	0.0005	0.0009	0.0015
D	0.0005	0.0008	0.0013
E	0.0005	0.0008	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0593	0.0485	3.2399	1.6081
A to Z ↑	0.0337	0.0295	4.6419	2.3034

B to Z ↓	0.0579	0.0460	3.2304	1.6050
B to Z ↑	0.0372	0.0321	4.6388	2.3036
C to Z ↓	0.0533	0.0442	3.2276	1.6036
C to Z ↑	0.0288	0.0246	4.6094	2.2873
D to Z ↓	0.0499	0.0401	3.2109	1.5948
D to Z ↑	0.0315	0.0265	4.6085	2.2873
E to Z ↓	0.0527	0.0429	3.2111	1.5968
E to Z ↑	0.0266	0.0233	4.5647	2.2714
	X19_P16		**X19_P16**	
A to Z ↓	0.0471		0.8291	
A to Z ↑	0.0308		1.1572	
B to Z ↓	0.0447		0.8275	
B to Z ↑	0.0336		1.1573	
C to Z ↓	0.0417		0.8252	
C to Z ↑	0.0250		1.1482	
D to Z ↓	0.0393		0.8228	
D to Z ↑	0.0273		1.1471	
E to Z ↓	0.0416		0.8234	
E to Z ↑	0.0291		1.1430	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	9.267e-06	1.000e-20
X10_P16	1.884e-05	1.000e-20
X19_P16	3.430e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	1.207e-05	2.076e-05	4.251e-05
B (output stable)	1.727e-05	2.436e-05	4.553e-05
C (output stable)	3.625e-05	5.762e-05	1.204e-04
D (output stable)	3.875e-05	6.712e-05	1.298e-04
E (output stable)	6.610e-05	1.170e-04	2.405e-04
A to Z	3.881e-03	6.193e-03	1.200e-02
B to Z	3.778e-03	5.939e-03	1.152e-02
C to Z	3.232e-03	5.095e-03	9.690e-03
D to Z	3.087e-03	4.804e-03	9.277e-03
E to Z	3.350e-03	5.319e-03	1.035e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

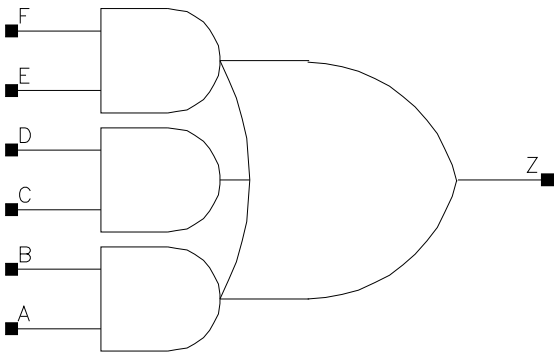
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.360	1.0880
X5_P16	0.800	1.360	1.0880
X10_P16	0.800	1.632	1.3056
X19_P16	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P16	X5_P16	X10_P16	X19_P16
A	0.0006	0.0006	0.0009	0.0015

B	0.0006	0.0006	0.0009	0.0013
C	0.0008	0.0008	0.0007	0.0014
D	0.0006	0.0006	0.0007	0.0013
E	0.0008	0.0008	0.0007	0.0015
F	0.0007	0.0007	0.0007	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X5_P16**	**X2_P16**	**X5_P16**
A to Z ↓	0.0458	0.0479	5.9571	3.3165
A to Z ↑	0.0331	0.0331	8.8178	4.8467
B to Z ↓	0.0433	0.0454	5.9329	3.3054
B to Z ↑	0.0362	0.0363	8.8139	4.8426
C to Z ↓	0.0426	0.0448	5.9512	3.3134
C to Z ↑	0.0304	0.0305	8.7343	4.8110
D to Z ↓	0.0388	0.0410	5.9276	3.3013
D to Z ↑	0.0325	0.0327	8.7302	4.8096
E to Z ↓	0.0363	0.0384	5.9190	3.2979
E to Z ↑	0.0247	0.0248	8.6808	4.7870
F to Z ↓	0.0331	0.0354	5.8970	3.2877
F to Z ↑	0.0264	0.0268	8.6827	4.7856
	X10_P16	**X19_P16**	**X10_P16**	**X19_P16**
A to Z ↓	0.0519	0.0489	1.6064	0.8268
A to Z ↑	0.0364	0.0332	2.3189	1.1621
B to Z ↓	0.0489	0.0468	1.5972	0.8254
B to Z ↑	0.0385	0.0361	2.3177	1.1617
C to Z ↓	0.0480	0.0455	1.6017	0.8259
C to Z ↑	0.0321	0.0303	2.3043	1.1542
D to Z ↓	0.0459	0.0437	1.5964	0.8244
D to Z ↑	0.0350	0.0331	2.3030	1.1541
E to Z ↓	0.0432	0.0421	1.5954	0.8227
E to Z ↑	0.0271	0.0260	2.2938	1.1500
F to Z ↓	0.0405	0.0394	1.5889	0.8204
F to Z ↑	0.0295	0.0284	2.2924	1.1499

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P16	1.052e-05	1.000e-20
X5_P16	1.303e-05	1.000e-20
X10_P16	2.109e-05	1.000e-20
X19_P16	4.014e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P16	X5_P16	X10_P16	X19_P16
A (output stable)	2.512e-05	2.512e-05	3.722e-05	5.733e-05
B (output stable)	2.822e-05	2.823e-05	9.598e-05	6.577e-05
C (output stable)	3.428e-05	3.431e-05	4.027e-05	8.233e-05
D (output stable)	4.166e-05	4.169e-05	4.793e-05	9.941e-05
E (output stable)	6.638e-05	6.650e-05	9.315e-05	1.541e-04
F (output stable)	7.370e-05	7.384e-05	9.760e-05	1.682e-04

A to Z	3.595e-03	4.237e-03	6.927e-03	1.286e-02
B to Z	3.425e-03	4.060e-03	6.513e-03	1.239e-02
C to Z	2.989e-03	3.616e-03	6.109e-03	1.139e-02
D to Z	2.798e-03	3.417e-03	5.901e-03	1.100e-02
E to Z	2.351e-03	2.948e-03	5.314e-03	1.009e-02
F to Z	2.192e-03	2.783e-03	5.095e-03	9.648e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

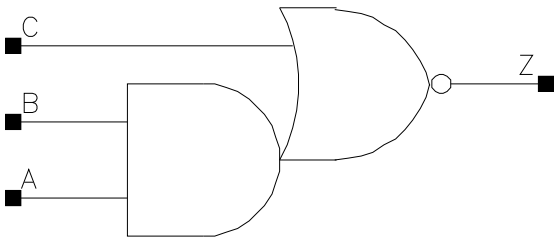
Pin Cycle (vdds)	X2_P16	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X10_P16	0.800	1.360	1.0880
X19_P16	0.800	2.584	2.0672
X25_P16	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P16	X10_P16	X19_P16	X25_P16
A	0.0007	0.0019	0.0037	0.0049
B	0.0006	0.0017	0.0034	0.0046
C	0.0007	0.0020	0.0037	0.0050

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X10_P16**	**X3_P16**	**X10_P16**
A to Z ↓	0.0080	0.0085	4.9898	1.8024
A to Z ↑	0.0165	0.0169	8.1361	2.7804
B to Z ↓	0.0088	0.0093	5.0634	1.8278
B to Z ↑	0.0133	0.0130	8.0257	2.7781
C to Z ↓	0.0094	0.0097	3.1629	1.0985
C to Z ↑	0.0156	0.0159	7.4119	2.5531
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0090	0.0090	0.9193	0.7012

A to Z ↑	0.0174	0.0171	1.4228	1.0589
B to Z ↓	0.0093	0.0093	0.9330	0.7120
B to Z ↑	0.0132	0.0131	1.4239	1.0728
C to Z ↓	0.0115	0.0115	0.6686	0.5116
C to Z ↑	0.0161	0.0160	1.3081	0.9789

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	7.627e-06	1.000e-20
X10_P16	2.112e-05	1.000e-20
X19_P16	4.044e-05	1.000e-20
X25_P16	5.334e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X10_P16	X19_P16	X25_P16
A (output stable)	4.137e-05	1.420e-04	2.875e-04	3.756e-04
B (output stable)	5.218e-05	1.975e-04	4.229e-04	5.400e-04
C (output stable)	6.236e-05	2.015e-04	3.930e-04	5.405e-04
A to Z	1.137e-03	3.499e-03	7.176e-03	9.375e-03
B to Z	9.384e-04	2.694e-03	5.457e-03	7.219e-03
C to Z	1.535e-03	4.592e-03	9.045e-03	1.205e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

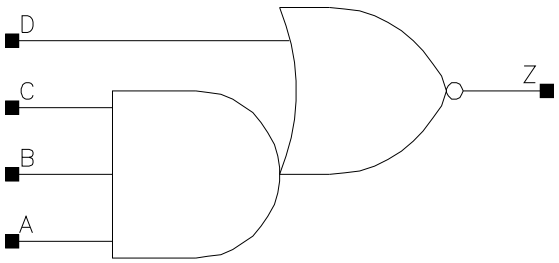
Pin Cycle (vdds)	X3_P16	X10_P16	X19_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X17_P16	0.800	3.536	2.8288
X22_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X17_P16	X22_P16
A	0.0006	0.0037	0.0050
B	0.0006	0.0035	0.0047
C	0.0007	0.0033	0.0044
D	0.0007	0.0039	0.0049

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X17_P16	X3_P16	X17_P16
A to Z ↓	0.0124	0.0133	6.8847	1.3141
A to Z ↑	0.0215	0.0208	8.1486	1.3715
B to Z ↓	0.0131	0.0135	6.9098	1.3201
B to Z ↑	0.0191	0.0184	8.1636	1.3933
C to Z ↓	0.0143	0.0132	6.9673	1.3280
C to Z ↑	0.0172	0.0147	8.1864	1.4032
D to Z ↓	0.0117	0.0135	3.0963	0.6586

D to Z ↑	0.0199	0.0186	6.9805	1.1863
	X22_P16		**X22_P16**	
A to Z ↓	0.0132		0.9983	
A to Z ↑	0.0206		1.0249	
B to Z ↓	0.0132		1.0035	
B to Z ↑	0.0181		1.0455	
C to Z ↓	0.0131		1.0098	
C to Z ↑	0.0145		1.0558	
D to Z ↓	0.0143		0.5453	
D to Z ↑	0.0180		0.8871	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	8.200e-06	1.000e-20
X17_P16	4.092e-05	1.000e-20
X22_P16	5.305e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X17_P16	X22_P16
A (output stable)	2.846e-05	1.887e-04	2.503e-04
B (output stable)	3.901e-05	3.068e-04	4.059e-04
C (output stable)	6.352e-05	6.090e-04	7.949e-04
D (output stable)	9.396e-05	5.703e-04	7.483e-04
A to Z	1.663e-03	9.604e-03	1.255e-02
B to Z	1.442e-03	7.920e-03	1.033e-02
C to Z	1.247e-03	6.281e-03	8.168e-03
D to Z	2.128e-03	1.157e-02	1.505e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

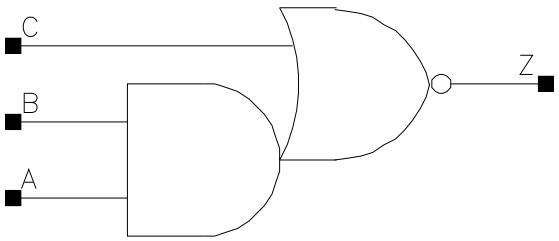
Pin Cycle (vdds)	X3_P16	X17_P16	X22_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X6_P16	0.800	1.088	0.8704
X9_P16	0.800	1.360	1.0880
X12_P16	0.800	1.904	1.5232
X25_P16	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X9_P16	X12_P16
A	0.0006	0.0014	0.0021	0.0028
B	0.0006	0.0013	0.0019	0.0026
C	0.0007	0.0012	0.0017	0.0023
	X25_P16			
A	0.0055			
B	0.0050			
C	0.0045			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0117	0.0115	6.4647	2.6286
A to Z ↑	0.0174	0.0187	9.2281	4.1323
B to Z ↓	0.0136	0.0122	6.5220	2.6585

B to Z ↑	0.0152	0.0150	9.1263	4.1518
C to Z ↓	0.0074	0.0066	4.1641	1.9834
C to Z ↑	0.0141	0.0130	8.5444	3.8520
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0110	0.0114	1.8012	1.3519
A to Z ↑	0.0175	0.0177	2.7690	2.0451
B to Z ↓	0.0121	0.0120	1.8235	1.3686
B to Z ↑	0.0139	0.0140	2.7739	2.0757
C to Z ↓	0.0066	0.0064	1.3497	1.0105
C to Z ↑	0.0124	0.0126	2.5826	1.9219
	X25_P16		**X25_P16**	
A to Z ↓	0.0113		0.7038	
A to Z ↑	0.0171		1.0378	
B to Z ↓	0.0121		0.7123	
B to Z ↑	0.0135		1.0439	
C to Z ↓	0.0064		0.5132	
C to Z ↑	0.0122		0.9721	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	6.155e-06	1.000e-20
X6_P16	1.473e-05	1.000e-20
X9_P16	2.073e-05	1.000e-20
X12_P16	2.803e-05	1.000e-20
X25_P16	5.441e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	1.480e-05	4.752e-05	6.309e-05	9.211e-05
B (output stable)	1.964e-05	1.001e-04	1.112e-04	1.926e-04
C (output stable)	1.960e-04	5.129e-04	6.437e-04	8.965e-04
A to Z	1.366e-03	3.336e-03	4.629e-03	6.352e-03
B to Z	1.198e-03	2.712e-03	3.727e-03	5.071e-03
C to Z	8.746e-04	1.934e-03	2.696e-03	3.712e-03
	X25_P16			
A (output stable)	1.748e-04			
B (output stable)	3.337e-04			
C (output stable)	1.685e-03			
A to Z	1.216e-02			
B to Z	9.781e-03			
C to Z	7.070e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

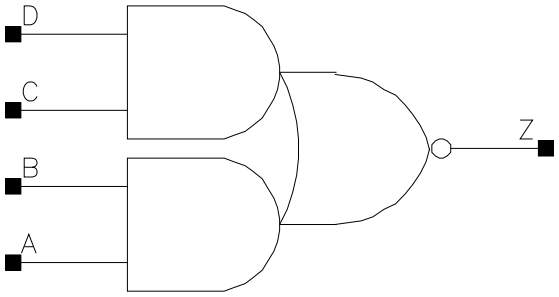
	X25_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.680	0.5440
X6_P16	0.800	1.224	0.9792
X9_P16	0.800	1.768	1.4144
X12_P16	0.800	2.448	1.9584
X24_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P16	X6_P16	X9_P16	X12_P16
A	0.0005	0.0014	0.0021	0.0028
B	0.0005	0.0012	0.0019	0.0026
C	0.0005	0.0014	0.0019	0.0025
D	0.0005	0.0011	0.0018	0.0024
	X24_P16			
A	0.0054			
B	0.0052			
C	0.0051			
D	0.0047			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X6_P16**	**X2_P16**	**X6_P16**
A to Z ↓	0.0118	0.0124	6.5764	2.5219
A to Z ↑	0.0224	0.0195	11.4093	3.7718
B to Z ↓	0.0135	0.0140	6.6538	2.5493
B to Z ↑	0.0195	0.0169	11.3994	3.8533
C to Z ↓	0.0080	0.0081	6.6030	2.5369
C to Z ↑	0.0186	0.0165	11.4739	3.7911
D to Z ↓	0.0091	0.0091	6.7085	2.5743
D to Z ↑	0.0155	0.0139	11.4571	3.9076
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0134	0.0138	1.8033	1.3584
A to Z ↑	0.0205	0.0209	2.5278	1.8996
B to Z ↓	0.0150	0.0150	1.8226	1.3726
B to Z ↑	0.0174	0.0176	2.5357	1.8793
C to Z ↓	0.0088	0.0094	1.8033	1.3634
C to Z ↑	0.0173	0.0177	2.5436	1.8974
D to Z ↓	0.0098	0.0097	1.8299	1.3836
D to Z ↑	0.0140	0.0140	2.5465	1.9071
	X24_P16		**X24_P16**	
A to Z ↓	0.0138		0.6998	
A to Z ↑	0.0206		0.9574	
B to Z ↓	0.0152		0.7073	
B to Z ↑	0.0173		0.9521	
C to Z ↓	0.0094		0.6861	
C to Z ↑	0.0177		0.9609	
D to Z ↓	0.0098		0.6971	
D to Z ↑	0.0140		0.9656	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P16	5.855e-06	1.000e-20
X6_P16	1.761e-05	1.000e-20
X9_P16	2.561e-05	1.000e-20
X12_P16	3.438e-05	1.000e-20
X24_P16	6.719e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P16	X6_P16	X9_P16	X12_P16
A (output stable)	1.672e-05	4.264e-05	8.271e-05	1.230e-04
B (output stable)	2.337e-05	6.410e-05	1.810e-04	3.131e-04
C (output stable)	3.932e-05	1.060e-04	1.831e-04	2.594e-04
D (output stable)	4.864e-05	1.341e-04	2.656e-04	4.286e-04
A to Z	1.428e-03	3.774e-03	5.933e-03	8.104e-03
B to Z	1.240e-03	3.278e-03	5.042e-03	6.876e-03
C to Z	9.026e-04	2.437e-03	3.871e-03	5.350e-03
D to Z	7.439e-04	2.023e-03	3.092e-03	4.215e-03
	X24_P16			
A (output stable)	2.266e-04			
B (output stable)	5.002e-04			
C (output stable)	5.008e-04			
D (output stable)	8.378e-04			

A to Z	1.574e-02			
B to Z	1.342e-02			
C to Z	1.047e-02			
D to Z	8.301e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

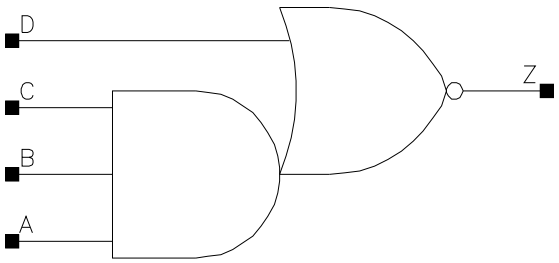
Pin Cycle (vdds)	X2_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X12_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X12_P16
A	0.0007	0.0027
B	0.0007	0.0026
C	0.0009	0.0024
D	0.0007	0.0026

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X12_P16	X3_P16	X12_P16
A to Z ↓	0.0151	0.0158	6.8877	1.9487
A to Z ↑	0.0222	0.0214	7.9716	2.0769
B to Z ↓	0.0162	0.0160	6.9082	1.9543
B to Z ↑	0.0204	0.0188	8.0891	2.0782
C to Z ↓	0.0183	0.0162	6.9591	1.9640
C to Z ↑	0.0192	0.0154	8.1505	2.0951
D to Z ↓	0.0069	0.0059	3.1721	0.8575
D to Z ↑	0.0152	0.0133	7.0122	1.8061

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	8.358e-06	1.000e-20
X12_P16	2.945e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X12_P16
A (output stable)	1.331e-05	7.325e-05
B (output stable)	2.378e-05	1.615e-04
C (output stable)	5.148e-05	3.308e-04
D (output stable)	3.944e-04	1.327e-03
A to Z	2.123e-03	7.949e-03
B to Z	1.896e-03	6.687e-03
C to Z	1.711e-03	5.521e-03
D to Z	1.228e-03	4.163e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

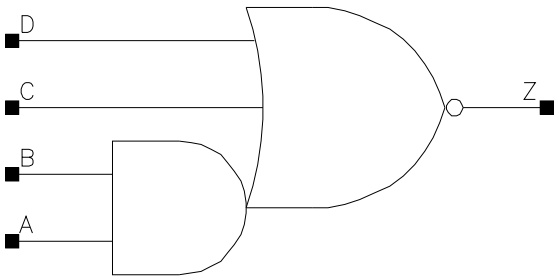
Pin Cycle (vdds)	X3_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X20_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P16	X20_P16
A	0.0006	0.0049
B	0.0006	0.0044
C	0.0007	0.0047
D	0.0007	0.0044

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X20_P16	X3_P16	X20_P16
A to Z ↓	0.0095	0.0105	4.9038	0.7944
A to Z ↑	0.0217	0.0204	11.4232	1.4810
B to Z ↓	0.0108	0.0113	4.9734	0.8063
B to Z ↑	0.0187	0.0160	11.5453	1.4841
C to Z ↓	0.0114	0.0163	3.1465	0.6524
C to Z ↑	0.0239	0.0226	10.8637	1.3979
D to Z ↓	0.0110	0.0148	3.1457	0.6515

D to Z ↑	0.0243	0.0212	10.8875	1.4028

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	7.231e-06	1.000e-20
X20_P16	4.550e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X20_P16
A (output stable)	5.230e-05	3.951e-04
B (output stable)	5.663e-05	4.537e-04
C (output stable)	3.845e-05	4.228e-04
D (output stable)	4.501e-05	5.116e-04
A to Z	1.399e-03	9.626e-03
B to Z	1.191e-03	7.635e-03
C to Z	2.129e-03	1.562e-02
D to Z	1.857e-03	1.250e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

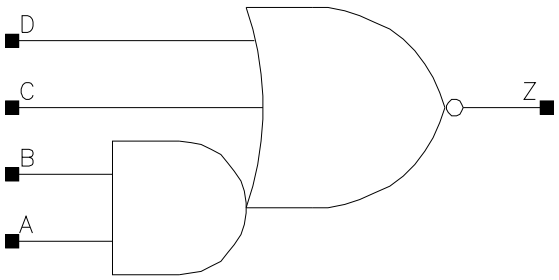
Pin Cycle (vdds)	X3_P16	X20_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.816	0.6528
X10_P16	0.800	2.448	1.9584
X19_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P16	X10_P16	X19_P16
A	0.0007	0.0026	0.0051
B	0.0006	0.0024	0.0048
C	0.0007	0.0022	0.0043
D	0.0006	0.0021	0.0039

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	X10_P16	X2_P16	X10_P16
A to Z ↓	0.0133	0.0138	5.7823	1.5400
A to Z ↑	0.0256	0.0240	12.0862	2.9623
B to Z ↓	0.0153	0.0150	5.8481	1.5555
B to Z ↑	0.0225	0.0199	12.1495	2.9755
C to Z ↓	0.0126	0.0118	5.1743	1.3003
C to Z ↑	0.0188	0.0172	11.5310	2.8208

D to Z ↓	0.0102	0.0085	5.2234	1.3161
D to Z ↑	0.0177	0.0149	11.5505	2.8299
	X19_P16		**X19_P16**	
A to Z ↓	0.0134		0.7897	
A to Z ↑	0.0234		1.5037	
B to Z ↓	0.0149		0.7986	
B to Z ↑	0.0193		1.5069	
C to Z ↓	0.0124		0.7046	
C to Z ↑	0.0166		1.4309	
D to Z ↓	0.0090		0.7135	
D to Z ↑	0.0142		1.4362	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P16	6.065e-06	1.000e-20
X10_P16	2.405e-05	1.000e-20
X19_P16	4.670e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P16	X10_P16	X19_P16
A (output stable)	1.804e-05	7.698e-05	1.492e-04
B (output stable)	1.877e-05	1.184e-04	2.220e-04
C (output stable)	4.445e-05	2.344e-04	4.656e-04
D (output stable)	9.858e-05	5.378e-04	1.041e-03
A to Z	2.026e-03	7.738e-03	1.493e-02
B to Z	1.811e-03	6.558e-03	1.267e-02
C to Z	1.279e-03	4.964e-03	9.419e-03
D to Z	1.028e-03	3.557e-03	6.637e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

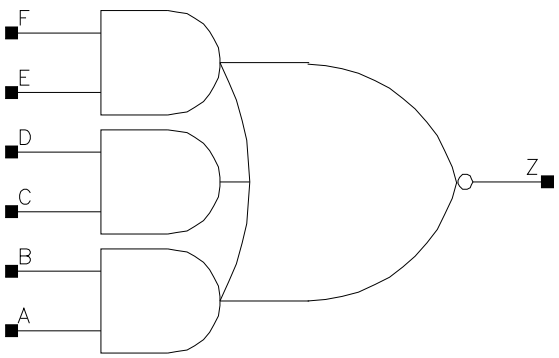
Pin Cycle (vdds)	X2_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.088	0.8704
X5_P16	0.800	2.040	1.6320
X7_P16	0.800	2.720	2.1760
X9_P16	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P16	X5_P16	X7_P16	X9_P16
A	0.0007	0.0012	0.0020	0.0026

B	0.0006	0.0013	0.0018	0.0024
C	0.0006	0.0012	0.0018	0.0027
D	0.0006	0.0013	0.0017	0.0023
E	0.0007	0.0012	0.0018	0.0023
F	0.0006	0.0010	0.0016	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X5_P16**	**X2_P16**	**X5_P16**
A to Z ↓	0.0147	0.0180	5.1794	2.9336
A to Z ↑	0.0335	0.0313	11.6967	5.3504
B to Z ↓	0.0169	0.0205	5.2382	2.9544
B to Z ↑	0.0301	0.0290	11.7642	5.3151
C to Z ↓	0.0134	0.0160	5.2016	2.9160
C to Z ↑	0.0294	0.0279	11.7782	5.3677
D to Z ↓	0.0154	0.0181	5.2764	2.9437
D to Z ↑	0.0260	0.0256	11.7834	5.3487
E to Z ↓	0.0098	0.0117	5.2409	2.8684
E to Z ↑	0.0239	0.0233	11.7974	5.3453
F to Z ↓	0.0109	0.0130	5.3358	2.9022
F to Z ↑	0.0199	0.0202	11.7779	5.3693
	X7_P16	**X9_P16**	**X7_P16**	**X9_P16**
A to Z ↓	0.0179	0.0184	2.0350	1.5480
A to Z ↑	0.0306	0.0312	3.5037	2.6378
B to Z ↓	0.0200	0.0202	2.0503	1.5595
B to Z ↑	0.0276	0.0278	3.5858	2.6831
C to Z ↓	0.0159	0.0167	2.0369	1.5377
C to Z ↑	0.0275	0.0287	3.5772	2.6832
D to Z ↓	0.0178	0.0176	2.0577	1.5525
D to Z ↑	0.0240	0.0242	3.5502	2.6648
E to Z ↓	0.0111	0.0112	2.0390	1.5424
E to Z ↑	0.0222	0.0222	3.5477	2.6768
F to Z ↓	0.0125	0.0119	2.0683	1.5659
F to Z ↑	0.0189	0.0183	3.5859	2.6757

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P16	1.012e-05	1.000e-20
X5_P16	2.068e-05	1.000e-20
X7_P16	3.001e-05	1.000e-20
X9_P16	3.942e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P16	X5_P16	X7_P16	X9_P16
A (output stable)	2.859e-05	5.405e-05	9.669e-05	1.347e-04
B (output stable)	3.385e-05	7.238e-05	1.469e-04	2.502e-04
C (output stable)	4.526e-05	9.262e-05	1.391e-04	1.930e-04
D (output stable)	5.306e-05	1.075e-04	2.014e-04	2.898e-04
E (output stable)	7.318e-05	1.646e-04	2.536e-04	3.559e-04
F (output stable)	8.656e-05	1.794e-04	3.042e-04	4.646e-04

A to Z	2.747e-03	5.622e-03	8.275e-03	1.126e-02
B to Z	2.502e-03	5.269e-03	7.458e-03	1.008e-02
C to Z	2.080e-03	4.356e-03	6.362e-03	8.628e-03
D to Z	1.855e-03	4.011e-03	5.616e-03	7.579e-03
E to Z	1.402e-03	3.131e-03	4.395e-03	5.818e-03
F to Z	1.197e-03	2.751e-03	3.714e-03	4.814e-03

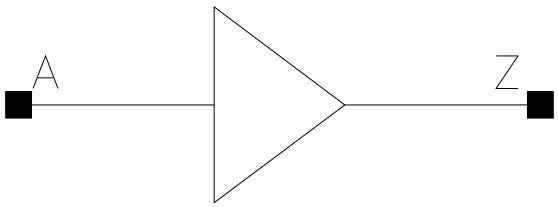
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X2_P16	X5_P16	X7_P16	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description
Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.544	0.4352
X5_P16	0.800	0.544	0.4352
X9_P16	0.800	0.680	0.5440
X11_P16	1.600	0.408	0.6528
X13_P16	0.800	0.680	0.5440
X19_P16	0.800	0.952	0.7616
X23_P16	1.600	0.544	0.8704
X24_P16	0.800	1.088	0.8704
X29_P16	0.800	1.224	0.9792
X34_P16	1.600	0.680	1.0880
X38_P16	0.800	1.632	1.3056
X46_P16	1.600	0.952	1.5232
X57_P16	0.800	2.312	1.8496
X68_P16	1.600	1.224	1.9584
X91_P16	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P16	X5_P16	X9_P16	X11_P16
A	0.0006	0.0007	0.0007	0.0009
	X13_P16	X19_P16	X23_P16	X24_P16
A	0.0009	0.0012	0.0014	0.0014
	X29_P16	X34_P16	X38_P16	X46_P16
A	0.0016	0.0018	0.0024	0.0024
	X57_P16	X68_P16	X91_P16	
A	0.0032	0.0034	0.0044	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X5_P16**	**X2_P16**	**X5_P16**
A to Z ↓	0.0234	0.0244	5.6672	3.1546
A to Z ↑	0.0181	0.0185	8.6002	4.7009
	X9_P16	**X11_P16**	**X9_P16**	**X11_P16**
A to Z ↓	0.0301	0.0282	1.6189	1.2327
A to Z ↑	0.0227	0.0205	2.3425	2.2144
	X13_P16	**X19_P16**	**X13_P16**	**X19_P16**
A to Z ↓	0.0269	0.0268	1.1100	0.7846
A to Z ↑	0.0215	0.0200	1.6248	1.1435
	X23_P16	**X24_P16**	**X23_P16**	**X24_P16**
A to Z ↓	0.0273	0.0265	0.5974	0.6387
A to Z ↑	0.0201	0.0207	1.1137	0.9164
	X29_P16	**X34_P16**	**X29_P16**	**X34_P16**
A to Z ↓	0.0257	0.0269	0.5293	0.4101
A to Z ↑	0.0203	0.0201	0.7692	0.7592
	X38_P16	**X46_P16**	**X38_P16**	**X46_P16**
A to Z ↓	0.0251	0.0265	0.4005	0.3081
A to Z ↑	0.0201	0.0195	0.5676	0.5714
	X57_P16	**X68_P16**	**X57_P16**	**X68_P16**
A to Z ↓	0.0262	0.0261	0.2694	0.2087
A to Z ↑	0.0209	0.0196	0.3805	0.3823
	X91_P16		**X91_P16**	
A to Z ↓	0.0275		0.1611	
A to Z ↑	0.0205		0.2879	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P16	5.043e-06	1.000e-20
X5_P16	7.963e-06	1.000e-20
X9_P16	1.301e-05	1.000e-20
X11_P16	1.625e-05	1.000e-20
X13_P16	1.980e-05	1.000e-20
X19_P16	2.630e-05	1.000e-20
X23_P16	3.130e-05	1.000e-20
X24_P16	3.283e-05	1.000e-20
X29_P16	3.979e-05	1.000e-20
X34_P16	4.516e-05	1.000e-20
X38_P16	5.401e-05	1.000e-20
X46_P16	5.862e-05	1.000e-20
X57_P16	7.773e-05	1.000e-20
X68_P16	8.659e-05	1.000e-20
X91_P16	1.119e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P16	X5_P16	X9_P16	X11_P16
A to Z	1.573e-03	2.088e-03	3.557e-03	4.167e-03
	X13_P16	X19_P16	X23_P16	X24_P16
A to Z	5.131e-03	7.024e-03	7.834e-03	8.695e-03
	X29_P16	X34_P16	X38_P16	X46_P16

A to Z	1.019e-02	1.160e-02	1.397e-02	1.515e-02
	X57_P16	X68_P16	X91_P16	
A to Z	2.067e-02	2.220e-02	2.991e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

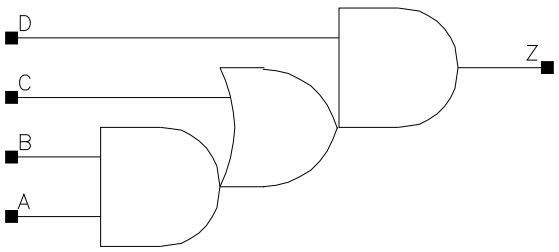
Pin Cycle (vdds)	X2_P16	X5_P16	X9_P16	X11_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P16	X19_P16	X23_P16	X24_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P16	X34_P16	X38_P16	X46_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P16	X68_P16	X91_P16	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.952	0.7616
X10_P16	0.800	1.632	1.3056
X14_P16	0.800	1.768	1.4144
X19_P16	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0007	0.0016	0.0016	0.0016
B	0.0008	0.0015	0.0015	0.0014
C	0.0008	0.0017	0.0017	0.0017
D	0.0011	0.0016	0.0016	0.0016

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0312	0.0287	3.2273	1.5249
A to Z ↑	0.0300	0.0276	4.8220	2.2997
B to Z ↓	0.0286	0.0262	3.2197	1.5235
B to Z ↑	0.0310	0.0284	4.8287	2.2975
C to Z ↓	0.0273	0.0250	3.2113	1.5195
C to Z ↑	0.0225	0.0204	4.7796	2.2759

D to Z ↓	0.0273	0.0238	3.1862	1.5069
D to Z ↑	0.0253	0.0217	4.7902	2.2813
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0323	0.0349	1.0644	0.7988
A to Z ↑	0.0310	0.0334	1.5447	1.1599
B to Z ↓	0.0299	0.0326	1.0635	0.7976
B to Z ↑	0.0320	0.0345	1.5454	1.1588
C to Z ↓	0.0285	0.0312	1.0595	0.7945
C to Z ↑	0.0231	0.0252	1.5252	1.1430
D to Z ↓	0.0261	0.0278	1.0458	0.7824
D to Z ↑	0.0243	0.0261	1.5288	1.1464

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.302e-05	1.000e-20
X10_P16	2.615e-05	1.000e-20
X14_P16	3.143e-05	1.000e-20
X19_P16	3.671e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	6.559e-05	1.263e-04	1.275e-04	1.279e-04
B (output stable)	8.966e-05	1.706e-04	1.718e-04	1.720e-04
C (output stable)	2.588e-04	4.323e-04	4.332e-04	4.334e-04
D (output stable)	6.998e-05	1.095e-04	1.106e-04	1.106e-04
A to Z	3.429e-03	6.367e-03	8.357e-03	1.021e-02
B to Z	3.197e-03	5.851e-03	7.830e-03	9.674e-03
C to Z	2.753e-03	4.950e-03	6.743e-03	8.410e-03
D to Z	3.461e-03	6.255e-03	7.973e-03	9.516e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

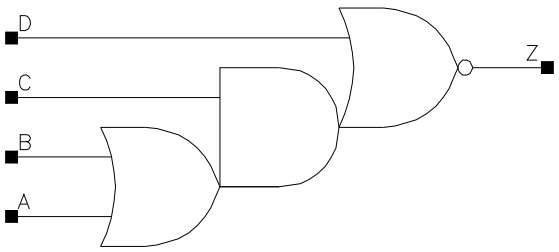
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X6_P16	0.800	1.496	1.1968
X9_P16	0.800	1.768	1.4144
X12_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X9_P16	X12_P16
A	0.0007	0.0014	0.0021	0.0027
B	0.0007	0.0013	0.0020	0.0026
C	0.0007	0.0013	0.0019	0.0025
D	0.0008	0.0013	0.0018	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0137	0.0125	5.1006	2.6044
A to Z ↑	0.0263	0.0261	11.4514	6.0418
B to Z ↓	0.0128	0.0123	4.9550	2.6180
B to Z ↑	0.0263	0.0254	11.4659	6.0532
C to Z ↓	0.0128	0.0120	4.7415	2.4562
C to Z ↑	0.0166	0.0157	8.1548	4.2214

D to Z ↓	0.0069	0.0054	3.1902	1.6216
D to Z ↑	0.0165	0.0144	8.6044	4.4737
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0126	0.0132	1.7865	1.3916
A to Z ↑	0.0243	0.0259	3.8953	3.0000
B to Z ↓	0.0119	0.0122	1.8002	1.3899
B to Z ↑	0.0243	0.0248	3.9009	3.0050
C to Z ↓	0.0123	0.0125	1.6957	1.3092
C to Z ↑	0.0150	0.0153	2.7443	2.0872
D to Z ↓	0.0057	0.0056	1.1261	0.8623
D to Z ↑	0.0135	0.0133	2.9000	2.2138

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	8.459e-06	1.000e-20
X6_P16	1.641e-05	1.000e-20
X9_P16	2.299e-05	1.000e-20
X12_P16	3.063e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	1.487e-05	3.558e-05	4.510e-05	7.620e-05
B (output stable)	1.480e-05	3.483e-05	4.483e-05	7.882e-05
C (output stable)	6.108e-05	1.358e-04	1.825e-04	2.478e-04
D (output stable)	2.066e-04	4.976e-04	7.068e-04	1.009e-03
A to Z	2.186e-03	4.189e-03	5.892e-03	8.180e-03
B to Z	1.894e-03	3.463e-03	5.029e-03	6.744e-03
C to Z	1.572e-03	2.910e-03	4.200e-03	5.708e-03
D to Z	1.137e-03	1.976e-03	2.803e-03	3.680e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

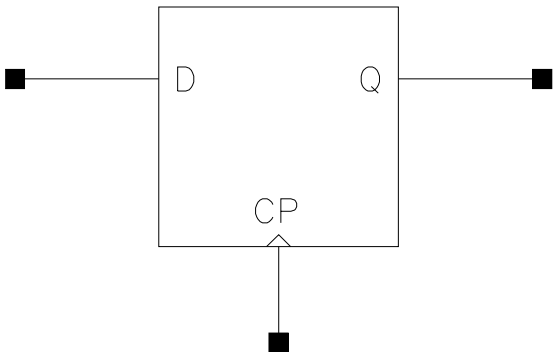
Pin Cycle (vdds)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	1.600	1.496	2.3936
X19_P16	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P16	X19_P16
CP	0.0010	0.0010
D	0.0008	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P16	X19_P16	X10_P16	X19_P16
CP to Q ↓	0.0493	0.0674	1.5923	0.8619
CP to Q ↑	0.0568	0.0660	2.2735	1.1659

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P16	X19_P16
CP ↓	min_pulse_width to CP	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0411	0.0599
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0224	0.0224
D ↑	setup_rising to CP	0.0142	0.0142

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P16	3.783e-05	1.000e-20
X19_P16	4.742e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

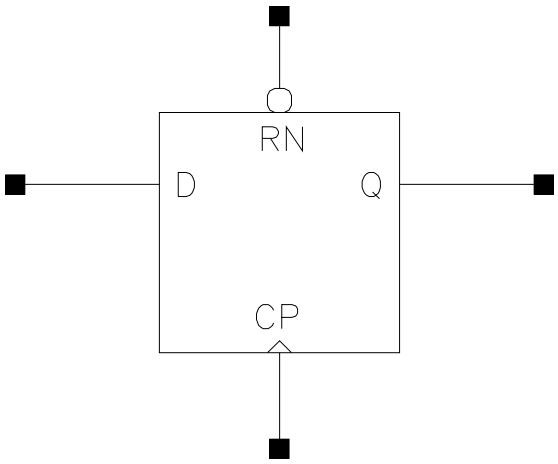
Pin Cycle	X10_P16	X19_P16
Clock 100Mhz Data 0Mhz	1.042e-02	1.043e-02
Clock 100Mhz Data 25Mhz	1.300e-02	1.621e-02
Clock 100Mhz Data 50Mhz	1.557e-02	2.198e-02
Clock = 0 Data 100Mhz	4.384e-03	4.384e-03
Clock = 1 Data 100Mhz	2.065e-05	2.076e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	1.600	1.768	2.8288
X19_P16	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P16	X19_P16
CP	0.0010	0.0010
D	0.0008	0.0008
RN	0.0010	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P16	X19_P16	X10_P16	X19_P16
CP to Q ↓	0.0530	0.0698	1.6165	0.8561
CP to Q ↑	0.0589	0.0681	2.2707	1.1606
RN to Q ↓	0.0512	0.0593	1.5354	0.7958

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P16	X19_P16
CP ↓	min_pulse_width to CP	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0423	0.0599
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0075	0.0075
D ↓	setup_rising to CP	0.0198	0.0224
D ↑	setup_rising to CP	0.0200	0.0200
RN ↓	min_pulse_width to RN	0.0664	0.0854
RN ↑	recovery_rising to CP	0.0103	0.0103
RN ↑	removal_rising to CP	-0.0029	-0.0029

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P16	4.357e-05	1.000e-20
X19_P16	5.501e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

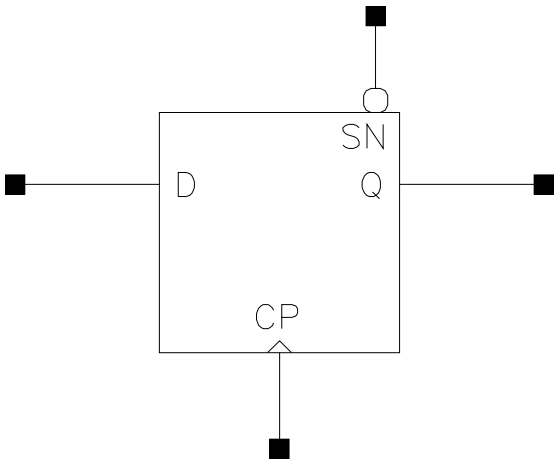
Pin Cycle	X10_P16	X19_P16
Clock 100Mhz Data 0Mhz	1.053e-02	1.053e-02
Clock 100Mhz Data 25Mhz	1.331e-02	1.651e-02
Clock 100Mhz Data 50Mhz	1.609e-02	2.250e-02
Clock = 0 Data 100Mhz	4.443e-03	4.444e-03
Clock = 1 Data 100Mhz	2.080e-05	2.093e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	1.600	1.768	2.8288
X19_P16	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P16	X19_P16
CP	0.0010	0.0010
D	0.0008	0.0008
SN	0.0012	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P16	X19_P16	X10_P16	X19_P16
CP to Q ↓	0.0504	0.0683	1.6042	0.8497
CP to Q ↑	0.0584	0.0683	2.2678	1.1604
SN to Q ↑	0.0361	0.0390	2.2250	1.1255

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P16	X19_P16
CP ↓	min_pulse_width to CP	0.0492	0.0492
CP ↑	min_pulse_width to CP	0.0410	0.0599
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0251	0.0251
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0398	0.0425
SN ↑	recovery_rising to CP	0.0010	0.0010
SN ↑	removal_rising to CP	0.0285	0.0285

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P16	4.384e-05	1.000e-20
X19_P16	5.373e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

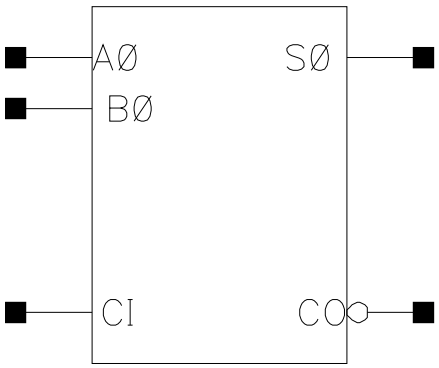
Pin Cycle	X10_P16	X19_P16
Clock 100Mhz Data 0Mhz	1.035e-02	1.036e-02
Clock 100Mhz Data 25Mhz	1.304e-02	1.636e-02
Clock 100Mhz Data 50Mhz	1.573e-02	2.235e-02
Clock = 0 Data 100Mhz	4.300e-03	4.300e-03
Clock = 1 Data 100Mhz	2.088e-05	2.096e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_-P16	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_-P16	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_-P16	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_-P16	1.600	2.720	4.3520
C8T28SOIDV_LLS1_-FA1X4_P16	1.600	2.040	3.2640
C8T28SOIDV_LLS1_-FA1X9_P16	1.600	3.128	5.0048
C8T28SOIDV_LLS1_-FA1X18_P16	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P16	C8T28SOIDV_LL_-FA1X9_P16	C8T28SOIDV_LL_-FA1X14_P16	C8T28SOIDV_LL_-FA1X19_P16
A0	0.0027	0.0029	0.0046	0.0050
B0	0.0023	0.0025	0.0042	0.0046
CI	0.0017	0.0018	0.0031	0.0034
	C8T28SOIDV_LLS1_-FA1X4_P16	C8T28SOIDV_LLS1_-FA1X9_P16	C8T28SOIDV_LLS1_-FA1X18_P16	
A0	0.0025	0.0035	0.0037	
B0	0.0025	0.0039	0.0044	
CI	0.0019	0.0027	0.0032	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P16	**C8T28SOIDV_LL_-FA1X9_P16**	**C8T28SOIDV_LL_-FA1X5_P16**	**C8T28SOIDV_LL_-FA1X9_P16**
A0 to CO ↓	0.0412	0.0448	3.3020	1.6902
A0 to CO ↑	0.0313	0.0341	4.5070	2.3012
A0 to S0 ↓	0.0451	0.0507	3.2376	1.6669
A0 to S0 ↑	0.0468	0.0517	4.5100	2.2622
B0 to CO ↓	0.0418	0.0455	3.3147	1.6980
B0 to CO ↑	0.0328	0.0356	4.5117	2.3037
B0 to S0 ↓	0.0458	0.0515	3.2368	1.6672
B0 to S0 ↑	0.0477	0.0528	4.5099	2.2632
CI to CO ↓	0.0404	0.0439	3.3144	1.6960
CI to CO ↑	0.0326	0.0354	4.5080	2.3003
CI to S0 ↓	0.0456	0.0515	3.2401	1.6676
CI to S0 ↑	0.0477	0.0529	4.5092	2.2623
	C8T28SOIDV_LL_-FA1X14_P16	**C8T28SOIDV_LL_-FA1X19_P16**	**C8T28SOIDV_LL_-FA1X14_P16**	**C8T28SOIDV_LL_-FA1X19_P16**
A0 to CO ↓	0.0425	0.0470	1.1046	0.8408
A0 to CO ↑	0.0324	0.0339	1.5779	1.1790
A0 to S0 ↓	0.0525	0.0538	1.0945	0.8128
A0 to S0 ↑	0.0541	0.0565	1.5243	1.1386
B0 to CO ↓	0.0424	0.0469	1.1080	0.8426
B0 to CO ↑	0.0332	0.0348	1.5775	1.1780
B0 to S0 ↓	0.0531	0.0543	1.0947	0.8132
B0 to S0 ↑	0.0548	0.0572	1.5251	1.1392
CI to CO ↓	0.0410	0.0454	1.1055	0.8408
CI to CO ↑	0.0329	0.0345	1.5773	1.1785
CI to S0 ↓	0.0526	0.0539	1.0952	0.8132
CI to S0 ↑	0.0543	0.0568	1.5246	1.1388
	C8T28SOIDV_-LLS1_FA1X4_P16	**C8T28SOIDV_-LLS1_FA1X9_P16**	**C8T28SOIDV_-LLS1_FA1X4_P16**	**C8T28SOIDV_-LLS1_FA1X9_P16**
A0 to CO ↓	0.0285	0.0256	5.8655	2.0073
A0 to CO ↑	0.0265	0.0244	4.5568	2.2974
A0 to S0 ↓	0.0597	0.0648	3.4474	1.2818
A0 to S0 ↑	0.0565	0.0554	4.7451	2.2509
B0 to CO ↓	0.0267	0.0269	5.8584	2.0106
B0 to CO ↑	0.0215	0.0227	4.5414	2.2955
B0 to S0 ↓	0.0598	0.0677	3.4463	1.2819
B0 to S0 ↑	0.0567	0.0584	4.7445	2.2505
CI to CO ↓	0.0277	0.0389	5.8564	2.0242
CI to CO ↑	0.0230	0.0216	4.5572	2.3124

CI to S0 ↓	0.0333	0.0406	3.4500	1.2843
CI to S0 ↑	0.0296	0.0308	4.7463	2.2512
	C8T28SOIDV_-LLS1_FA1X18_P16		**C8T28SOIDV_-LLS1_FA1X18_P16**	
A0 to CO ↓	0.0332		1.0581	
A0 to CO ↑	0.0256		1.1316	
A0 to S0 ↓	0.0698		0.6645	
A0 to S0 ↑	0.0569		1.1296	
B0 to CO ↓	0.0351		1.0594	
B0 to CO ↑	0.0240		1.1305	
B0 to S0 ↓	0.0719		0.6646	
B0 to S0 ↑	0.0590		1.1298	
CI to CO ↓	0.0493		1.0677	
CI to CO ↑	0.0261		1.1337	
CI to S0 ↓	0.0428		0.6655	
CI to S0 ↑	0.0290		1.1294	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P16	3.098e-05	1.000e-20
C8T28SOIDV_LL_FA1X9_P16	4.280e-05	1.000e-20
C8T28SOIDV_LL_FA1X14_P16	6.500e-05	1.000e-20
C8T28SOIDV_LL_FA1X19_P16	8.024e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P16	6.402e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P16	9.527e-05	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P16	1.440e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P16	C8T28SOIDV_LL_-FA1X9_P16	C8T28SOIDV_LL_-FA1X14_P16	C8T28SOIDV_LL_-FA1X19_P16
A0 to CO	3.816e-03	5.659e-03	9.190e-03	1.147e-02
A0 to S0	3.874e-03	5.563e-03	9.363e-03	1.165e-02
B0 to CO	3.867e-03	5.748e-03	9.271e-03	1.161e-02
B0 to S0	3.833e-03	5.548e-03	9.294e-03	1.158e-02
CI to CO	3.892e-03	5.738e-03	9.356e-03	1.176e-02
CI to S0	3.803e-03	5.526e-03	9.246e-03	1.151e-02
	C8T28SOIDV_LLS1_-FA1X4_P16	C8T28SOIDV_LLS1_-FA1X9_P16	C8T28SOIDV_LLS1_-FA1X18_P16	
A0 to CO	5.719e-03	8.912e-03	1.454e-02	
A0 to S0	7.736e-03	1.151e-02	1.815e-02	
B0 to CO	6.044e-03	9.070e-03	1.471e-02	
B0 to S0	8.302e-03	1.185e-02	1.852e-02	
CI to CO	4.131e-03	7.496e-03	1.316e-02	
CI to S0	4.692e-03	8.365e-03	1.429e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P16	C8T28SOIDV_LL_-FA1X9_P16	C8T28SOIDV_LL_-FA1X14_P16	C8T28SOIDV_LL_-FA1X19_P16
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P16	C8T28SOIDV_LLS1_-FA1X9_P16	C8T28SOIDV_LLS1_-FA1X18_P16	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P16	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P16	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P16	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P16	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P16	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P16	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P16	C8T28SOI_LL_-HA1X9_P16	C8T28SOI_LLS1_-HA1X5_P16	C8T28SOIDV_LL_-HA1X14_P16
A0	0.0009	0.0013	0.0015	0.0019
B0	0.0008	0.0013	0.0014	0.0016
	C8T28SOIDV_LL_-HA1X19_P16	C8T28SOIDV_LLS1_-HA1X11_P16		
A0	0.0024	0.0023		
B0	0.0020	0.0023		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P16	**C8T28SOI_LL_-HA1X9_P16**	**C8T28SOI_LL_-HA1X5_P16**	**C8T28SOI_LL_-HA1X9_P16**
A0 to CO ↓	0.0332	0.0295	3.2506	1.5997
A0 to CO ↑	0.0296	0.0271	4.7837	2.3182
A0 to S0 ↓	0.0417	0.0393	3.1202	1.5823
A0 to S0 ↑	0.0400	0.0381	4.6595	2.3074
B0 to CO ↓	0.0323	0.0286	3.2495	1.5997
B0 to CO ↑	0.0323	0.0298	4.7830	2.3180
B0 to S0 ↓	0.0438	0.0409	3.1203	1.5816
B0 to S0 ↑	0.0393	0.0372	4.6595	2.3074
	C8T28SOI_LLS1_-HA1X5_P16	**C8T28SOIDV_LL_-HA1X14_P16**	**C8T28SOI_LLS1_-HA1X5_P16**	**C8T28SOIDV_LL_-HA1X14_P16**
A0 to CO ↓	0.0266	0.0303	3.1837	1.0982
A0 to CO ↑	0.0234	0.0266	4.7307	1.5560
A0 to S0 ↓	0.0354	0.0429	3.1784	1.1077
A0 to S0 ↑	0.0404	0.0414	4.7508	1.5330
B0 to CO ↓	0.0251	0.0280	3.1825	1.0946
B0 to CO ↑	0.0254	0.0278	4.7275	1.5554
B0 to S0 ↓	0.0375	0.0431	3.1769	1.1071
B0 to S0 ↑	0.0395	0.0395	4.7508	1.5338
	C8T28SOIDV_LL_-HA1X19_P16	**C8T28SOIDV_-LLS1_HA1X11_P16**	**C8T28SOIDV_LL_-HA1X19_P16**	**C8T28SOIDV_-LLS1_HA1X11_P16**
A0 to CO ↓	0.0285	0.0264	0.8113	1.1696
A0 to CO ↑	0.0259	0.0264	1.1784	2.2748
A0 to S0 ↓	0.0401	0.0330	0.8068	1.1861
A0 to S0 ↑	0.0387	0.0355	1.1507	2.2928
B0 to CO ↓	0.0265	0.0247	0.8099	1.1675
B0 to CO ↑	0.0275	0.0287	1.1785	2.2746
B0 to S0 ↓	0.0409	0.0341	0.8069	1.1853
B0 to S0 ↑	0.0370	0.0354	1.1509	2.2925

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_HA1X5_P16	1.789e-05	1.000e-20
C8T28SOI_LL_HA1X9_P16	3.753e-05	1.000e-20
C8T28SOI_LLS1_HA1X5_P16	2.204e-05	1.000e-20
C8T28SOIDV_LL_HA1X14_P16	5.354e-05	1.000e-20
C8T28SOIDV_LL_HA1X19_P16	7.329e-05	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P16	4.995e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

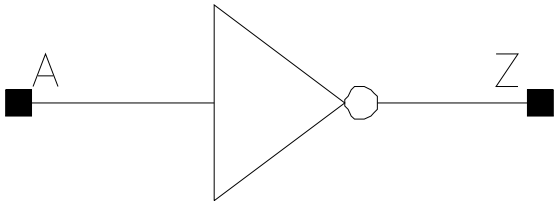
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P16	C8T28SOI_LL_-HA1X9_P16	C8T28SOI_LLS1_-HA1X5_P16	C8T28SOIDV_LL_-HA1X14_P16
A0 to CO	2.903e-03	4.859e-03	3.393e-03	7.709e-03
A0 to S0	2.652e-03	4.701e-03	3.044e-03	7.753e-03
B0 to CO	2.943e-03	5.032e-03	3.433e-03	7.750e-03
B0 to S0	2.611e-03	4.601e-03	2.953e-03	7.558e-03
	C8T28SOIDV_LL_-HA1X19_P16	C8T28SOIDV_LLS1_-HA1X11_P16		
A0 to CO	9.422e-03	6.684e-03		
A0 to S0	9.460e-03	6.033e-03		

B0 to CO	9.467e-03	6.133e-03		
B0 to S0	9.241e-03	6.161e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P16	C8T28SOI_LL_-HA1X9_P16	C8T28SOI_LLS1_-HA1X5_P16	C8T28SOIDV_LL_-HA1X14_P16
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P16	C8T28SOIDV_LLS1_-HA1X11_P16		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P16	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P16	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P16	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P16	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P16	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P16	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P16	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P16	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P16	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P16	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P16	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P16	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P16	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P16	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P16	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P16	C8T28SOI_LL_IVX3_-P16	C8T28SOI_LL_IVX5_-P16	C8T28SOI_LL_-IVX10_P16

A	0.0005	0.0005	0.0007	0.0013
	C8T28SOI_LL_-IVX14_P16	C8T28SOI_LL_-IVX19_P16	C8T28SOI_LL_-IVX29_P16	C8T28SOI_LL_-IVX34_P16
A	0.0020	0.0026	0.0038	0.0044
	C8T28SOI_LL_-IVX38_P16	C8T28SOIDV_LL_-IVX11_P16	C8T28SOIDV_LL_-IVX23_P16	C8T28SOIDV_LL_-IVX34_P16
A	0.0051	0.0014	0.0028	0.0041
	C8T28SOIDV_LL_-IVX46_P16	C8T28SOIDV_LL_-IVX68_P16	C8T28SOIDV_LL_-IVX91_P16	
A	0.0055	0.0084	0.0117	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P16	**C8T28SOI_LL_-IVX3_P16**	**C8T28SOI_LL_-IVX2_P16**	**C8T28SOI_LL_-IVX3_P16**
A to Z ↓	0.0063	0.0060	5.8952	4.6434
A to Z ↑	0.0119	0.0110	8.8202	6.8025
	C8T28SOI_LL_-IVX5_P16	**C8T28SOI_LL_-IVX10_P16**	**C8T28SOI_LL_-IVX5_P16**	**C8T28SOI_LL_-IVX10_P16**
A to Z ↓	0.0055	0.0043	3.2579	1.5649
A to Z ↑	0.0098	0.0083	4.8279	2.3025
	C8T28SOI_LL_-IVX14_P16	**C8T28SOI_LL_-IVX19_P16**	**C8T28SOI_LL_-IVX14_P16**	**C8T28SOI_LL_-IVX19_P16**
A to Z ↓	0.0046	0.0049	1.0858	0.8279
A to Z ↑	0.0083	0.0086	1.5455	1.1846
	C8T28SOI_LL_-IVX29_P16	**C8T28SOI_LL_-IVX34_P16**	**C8T28SOI_LL_-IVX29_P16**	**C8T28SOI_LL_-IVX34_P16**
A to Z ↓	0.0049	0.0046	0.5536	0.4719
A to Z ↑	0.0084	0.0079	0.7847	0.6702
	C8T28SOI_LL_-IVX38_P16	**C8T28SOIDV_LL_-IVX11_P16**	**C8T28SOI_LL_-IVX38_P16**	**C8T28SOIDV_LL_-IVX11_P16**
A to Z ↓	0.0048	0.0043	0.4184	1.2675
A to Z ↑	0.0081	0.0098	0.5936	2.3336
	C8T28SOIDV_LL_-IVX23_P16	**C8T28SOIDV_LL_-IVX34_P16**	**C8T28SOIDV_LL_-IVX23_P16**	**C8T28SOIDV_LL_-IVX34_P16**
A to Z ↓	0.0036	0.0040	0.6168	0.4220
A to Z ↑	0.0088	0.0089	1.1384	0.7630
	C8T28SOIDV_LL_-IVX46_P16	**C8T28SOIDV_LL_-IVX68_P16**	**C8T28SOIDV_LL_-IVX46_P16**	**C8T28SOIDV_LL_-IVX68_P16**
A to Z ↓	0.0039	0.0039	0.3174	0.2162
A to Z ↑	0.0087	0.0085	0.5728	0.3844
	C8T28SOIDV_LL_-IVX91_P16		**C8T28SOIDV_LL_-IVX91_P16**	
A to Z ↓	0.0045		0.1672	
A to Z ↑	0.0090		0.2918	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_IVX2_P16	2.637e-06	1.000e-20
C8T28SOI_LL_IVX3_P16	3.551e-06	1.000e-20
C8T28SOI_LL_IVX5_P16	5.283e-06	1.000e-20
C8T28SOI_LL_IVX10_P16	1.099e-05	1.000e-20

C8T28SOI_LL_IVX14_P16	1.582e-05	1.000e-20
C8T28SOI_LL_IVX19_P16	2.056e-05	1.000e-20
C8T28SOI_LL_IVX29_P16	3.003e-05	1.000e-20
C8T28SOI_LL_IVX34_P16	3.477e-05	1.000e-20
C8T28SOI_LL_IVX38_P16	3.951e-05	1.000e-20
C8T28SOIDV_LL_IVX11_P16	1.208e-05	1.000e-20
C8T28SOIDV_LL_IVX23_P16	2.421e-05	1.000e-20
C8T28SOIDV_LL_IVX34_P16	3.493e-05	1.000e-20
C8T28SOIDV_LL_IVX46_P16	4.542e-05	1.000e-20
C8T28SOIDV_LL_IVX68_P16	6.636e-05	1.000e-20
C8T28SOIDV_LL_IVX91_P16	8.734e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P16	C8T28SOI_LL_IVX3_-P16	C8T28SOI_LL_IVX5_-P16	C8T28SOI_LL_-IVX10_P16
A to Z	5.427e-04	6.733e-04	8.691e-04	1.662e-03
	C8T28SOI_LL_-IVX14_P16	C8T28SOI_LL_-IVX19_P16	C8T28SOI_LL_-IVX29_P16	C8T28SOI_LL_-IVX34_P16
A to Z	2.524e-03	3.393e-03	4.986e-03	5.678e-03
	C8T28SOI_LL_-IVX38_P16	C8T28SOIDV_LL_-IVX11_P16	C8T28SOIDV_LL_-IVX23_P16	C8T28SOIDV_LL_-IVX34_P16
A to Z	6.505e-03	1.906e-03	3.590e-03	5.424e-03
	C8T28SOIDV_LL_-IVX46_P16	C8T28SOIDV_LL_-IVX68_P16	C8T28SOIDV_LL_-IVX91_P16	
A to Z	7.002e-03	1.033e-02	1.392e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

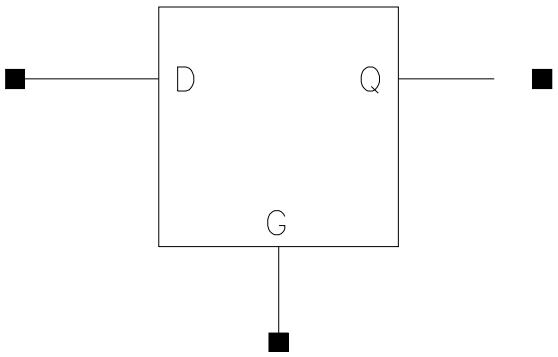
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P16	C8T28SOI_LL_IVX3_-P16	C8T28SOI_LL_IVX5_-P16	C8T28SOI_LL_-IVX10_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P16	C8T28SOI_LL_-IVX19_P16	C8T28SOI_LL_-IVX29_P16	C8T28SOI_LL_-IVX34_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P16	C8T28SOIDV_LL_-IVX11_P16	C8T28SOIDV_LL_-IVX23_P16	C8T28SOIDV_LL_-IVX34_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P16	C8T28SOIDV_LL_-IVX68_P16	C8T28SOIDV_LL_-IVX91_P16	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.360	1.0880
X9_P16	1.600	0.952	1.5232
X19_P16	1.600	1.224	1.9584
X28_P16	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16	X28_P16
D	0.0005	0.0008	0.0012	0.0019
G	0.0010	0.0010	0.0020	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D to Q ↓	0.0469	0.0453	3.3227	1.7095
D to Q ↑	0.0270	0.0323	4.6383	2.2741
G to Q ↓	0.0499	0.0480	3.3185	1.7076

G to Q ↑	0.0265	0.0303	4.6387	2.2747
	X19_P16	**X28_P16**	**X19_P16**	**X28_P16**
D to Q ↓	0.0371	0.0389	0.8188	0.5511
D to Q ↑	0.0287	0.0290	1.1454	0.7693
G to Q ↓	0.0415	0.0382	0.8166	0.5501
G to Q ↑	0.0263	0.0265	1.1458	0.7689

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P16	X9_P16	X19_P16	X28_P16
D ↓	hold_falling to G	-0.0072	-0.0072	0.0031	0.0009
D ↑	hold_falling to G	0.0072	0.0019	0.0041	0.0019
D ↓	setup_falling to G	0.0434	0.0419	0.0316	0.0344
D ↑	setup_falling to G	0.0280	0.0329	0.0334	0.0329
G ↑	min_pulse_width to G	0.0424	0.0412	0.0352	0.0365

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.451e-05	1.000e-20
X9_P16	2.243e-05	1.000e-20
X19_P16	3.783e-05	1.000e-20
X28_P16	5.109e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	1.072e-05	2.732e-05	3.260e-05	8.653e-05
G (output stable)	1.105e-03	1.348e-03	2.198e-03	2.159e-03
D to Q	4.583e-03	7.217e-03	1.105e-02	1.597e-02
G to Q	4.272e-03	6.755e-03	1.014e-02	1.401e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

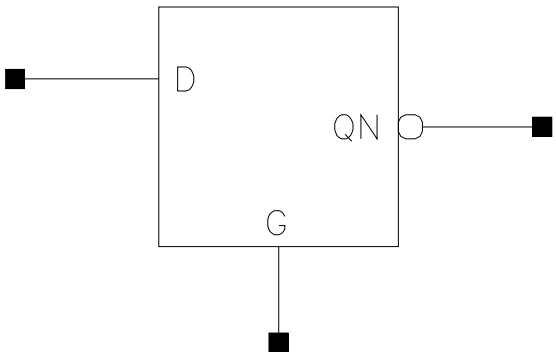
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P16	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P16
D	0.0005
G	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P16	X10_P16
D to QN ↓	0.0422	1.5347
D to QN ↑	0.0553	2.2568
G to QN ↓	0.0413	1.5342
G to QN ↑	0.0582	2.2576

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P16
D ↓	hold_falling to G	-0.0143
D ↑	hold_falling to G	-0.0014
D ↓	setup_falling to G	0.0418
D ↑	setup_falling to G	0.0290
G ↑	min_pulse_width to G	0.0377

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P16	2.130e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X10_P16
D (output stable)	1.061e-05
G (output stable)	1.224e-03
D to QN	5.962e-03
G to QN	5.622e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

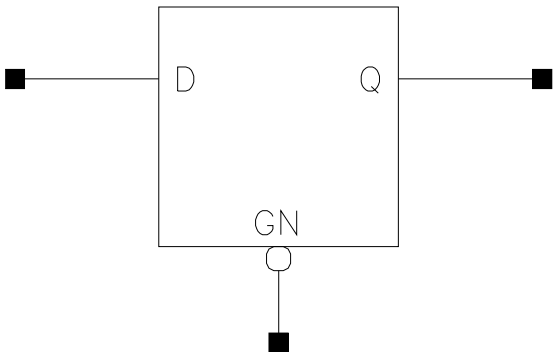
Pin Cycle (vdds)	X10_P16
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.360	1.0880
X9_P16	1.600	0.952	1.5232
X19_P16	1.600	1.224	1.9584
X28_P16	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16	X28_P16
D	0.0005	0.0008	0.0012	0.0017
GN	0.0010	0.0010	0.0015	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D to Q ↓	0.0473	0.0446	3.3304	1.7121
D to Q ↑	0.0272	0.0319	4.6335	2.2782
GN to Q ↓	0.0427	0.0426	3.3309	1.7150

GN to Q ↑	0.0465	0.0449	4.6289	2.2698
	X19_P16	**X28_P16**	**X19_P16**	**X28_P16**
D to Q ↓	0.0375	0.0372	0.8147	0.5496
D to Q ↑	0.0301	0.0295	1.1388	0.7612
GN to Q ↓	0.0336	0.0320	0.8157	0.5494
GN to Q ↑	0.0409	0.0406	1.1363	0.7610

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P16	X9_P16	X19_P16	X28_P16
D ↓	hold_rising to GN	-0.0095	-0.0078	-0.0030	-0.0030
D ↑	hold_rising to GN	0.0073	0.0057	0.0058	0.0053
D ↓	setup_rising to GN	0.0519	0.0445	0.0397	0.0401
D ↑	setup_rising to GN	0.0244	0.0288	0.0297	0.0239
GN ↓	min_pulse_width to GN	0.0551	0.0510	0.0437	0.0408

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.417e-05	1.000e-20
X9_P16	2.235e-05	1.000e-20
X19_P16	3.872e-05	1.000e-20
X28_P16	5.089e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	1.045e-05	1.669e-05	3.271e-05	7.481e-05
GN (output stable)	1.104e-03	1.322e-03	1.914e-03	2.062e-03
D to Q	4.591e-03	7.240e-03	1.139e-02	1.558e-02
GN to Q	6.611e-03	9.490e-03	1.421e-02	1.808e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

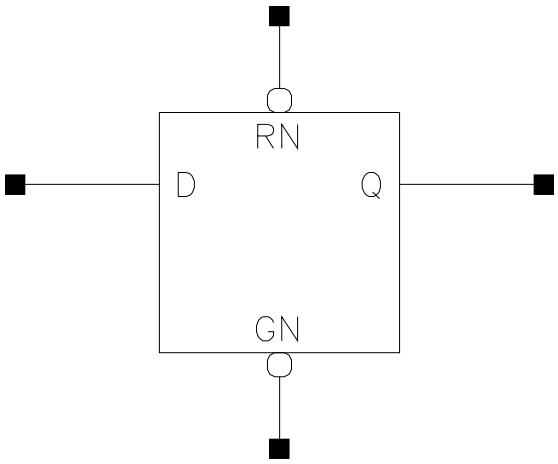
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16	X28_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.632	1.3056
X9_P16	1.600	1.224	1.9584
X19_P16	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16
D	0.0005	0.0007	0.0014
GN	0.0011	0.0012	0.0016
RN	0.0005	0.0006	0.0006

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D to Q ↓	0.0477	0.0464	3.2573	1.6649

D to Q ↑	0.0438	0.0486	4.7926	2.3547
GN to Q ↓	0.0442	0.0430	3.2581	1.6656
GN to Q ↑	0.0598	0.0572	4.7948	2.3557
RN to Q ↓	0.0397	0.0492	3.0757	1.6199
RN to Q ↑	0.0471	0.0515	4.7978	2.3572
	X19_P16		**X19_P16**	
D to Q ↓	0.0390		0.8213	
D to Q ↑	0.0530		1.1907	
GN to Q ↓	0.0351		0.8220	
GN to Q ↑	0.0555		1.1932	
RN to Q ↓	0.0615		0.8351	
RN to Q ↑	0.0581		1.1933	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P16	X9_P16	X19_P16
D ↓	hold_rising to GN	-0.0095	-0.0101	-0.0025
D ↑	hold_rising to GN	-0.0039	-0.0088	-0.0137
D ↓	setup_rising to GN	0.0547	0.0495	0.0430
D ↑	setup_rising to GN	0.0443	0.0482	0.0588
GN ↓	min_pulse_width to GN	0.0602	0.0574	0.0589
RN ↓	min_pulse_width to RN	0.0496	0.0615	0.0784
RN ↑	recovery_rising to GN	0.0461	0.0541	0.0628
RN ↑	removal_rising to GN	-0.0266	-0.0347	-0.0413

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.475e-05	1.000e-20
X9_P16	2.223e-05	1.000e-20
X19_P16	3.758e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16
D (output stable)	8.574e-05	8.430e-05	1.292e-04
GN (output stable)	1.247e-03	1.360e-03	1.746e-03
RN (output stable)	3.448e-05	4.554e-05	6.187e-05
D to Q	5.623e-03	8.157e-03	1.306e-02
GN to Q	7.810e-03	1.034e-02	1.563e-02
RN to Q	4.228e-03	6.212e-03	1.065e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

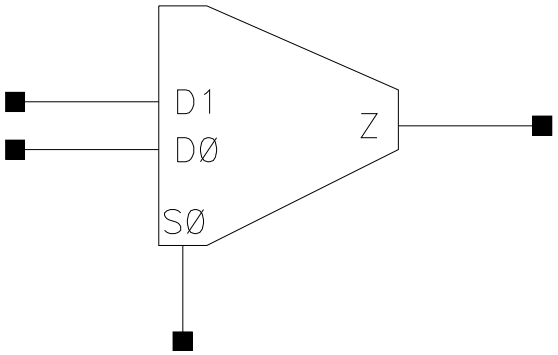
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.360	1.0880
X9_P16	0.800	1.496	1.1968
X14_P16	0.800	2.176	1.7408
X19_P16	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P16	X9_P16	X14_P16	X19_P16
D0	0.0007	0.0008	0.0011	0.0015
D1	0.0006	0.0008	0.0011	0.0015
S0	0.0011	0.0011	0.0014	0.0018

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X9_P16	X5_P16	X9_P16
D0 to Z ↓	0.0344	0.0331	3.2729	1.6617
D0 to Z ↑	0.0275	0.0277	4.7417	2.4091
D1 to Z ↓	0.0350	0.0324	3.2712	1.6587
D1 to Z ↑	0.0273	0.0262	4.7481	2.4044
S0 to Z ↓	0.0324	0.0293	3.2613	1.6545
S0 to Z ↑	0.0311	0.0293	4.7445	2.4070

	X14_P16	X19_P16	X14_P16	X19_P16
D0 to Z ↓	0.0357	0.0318	1.1450	0.8272
D0 to Z ↑	0.0289	0.0270	1.6288	1.1814
D1 to Z ↓	0.0362	0.0327	1.1454	0.8275
D1 to Z ↑	0.0278	0.0263	1.6264	1.1819
S0 to Z ↓	0.0343	0.0319	1.1410	0.8248
S0 to Z ↑	0.0338	0.0312	1.6267	1.1807

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.675e-05	1.000e-20
X9_P16	2.745e-05	1.000e-20
X14_P16	3.722e-05	1.000e-20
X19_P16	5.382e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X9_P16	X14_P16	X19_P16
D0 (output stable)	8.155e-04	1.435e-03	1.698e-03	2.179e-03
D1 (output stable)	7.770e-04	1.245e-03	1.756e-03	2.286e-03
S0 (output stable)	1.187e-03	1.106e-03	1.709e-03	2.063e-03
D0 to Z	3.215e-03	5.223e-03	8.277e-03	1.029e-02
D1 to Z	3.156e-03	4.939e-03	8.092e-03	1.023e-02
S0 to Z	3.889e-03	5.176e-03	9.004e-03	1.103e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

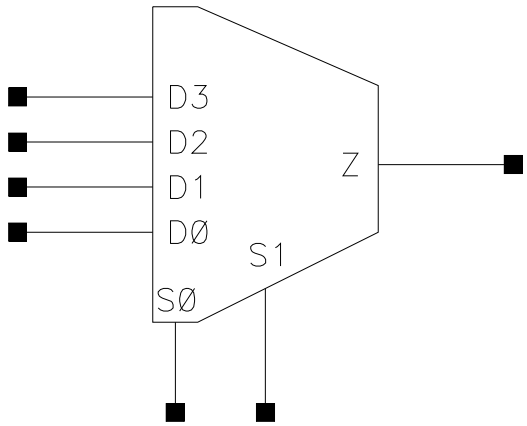
Pin Cycle (vdds)	X5_P16	X9_P16	X14_P16	X19_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.600	1.496	2.3936
X9_P16	1.600	1.768	2.8288
X13_P16	1.600	2.312	3.6992
X18_P16	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P16	X9_P16	X13_P16	X18_P16
D0	0.0005	0.0008	0.0012	0.0012
D1	0.0005	0.0006	0.0012	0.0012
D2	0.0005	0.0008	0.0012	0.0012
D3	0.0005	0.0006	0.0012	0.0012
S0	0.0015	0.0020	0.0028	0.0028
S1	0.0009	0.0010	0.0015	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X9_P16	X4_P16	X9_P16
D0 to Z ↓	0.0735	0.0628	3.5897	1.7578
D0 to Z ↑	0.0470	0.0445	4.8856	2.4231
D1 to Z ↓	0.0727	0.0626	3.5857	1.7595
D1 to Z ↑	0.0469	0.0442	4.8749	2.4218
D2 to Z ↓	0.0673	0.0633	3.5363	1.7635
D2 to Z ↑	0.0452	0.0440	4.8503	2.4206
D3 to Z ↓	0.0680	0.0623	3.5456	1.7623
D3 to Z ↑	0.0459	0.0439	4.8514	2.4209
S0 to Z ↓	0.0773	0.0704	3.5643	1.7600
S0 to Z ↑	0.0564	0.0558	4.8791	2.4258
S1 to Z ↓	0.0499	0.0482	3.5588	1.7595
S1 to Z ↑	0.0431	0.0431	4.8688	2.4201
	X13_P16	X18_P16	X13_P16	X18_P16
D0 to Z ↓	0.0617	0.0676	1.2294	0.9214
D0 to Z ↑	0.0398	0.0433	1.6210	1.2266
D1 to Z ↓	0.0619	0.0678	1.2300	0.9219
D1 to Z ↑	0.0408	0.0445	1.6225	1.2262
D2 to Z ↓	0.0560	0.0613	1.2082	0.9048
D2 to Z ↑	0.0396	0.0432	1.6177	1.2232
D3 to Z ↓	0.0557	0.0609	1.2070	0.9039
D3 to Z ↑	0.0398	0.0434	1.6164	1.2227
S0 to Z ↓	0.0669	0.0725	1.2182	0.9130
S0 to Z ↑	0.0512	0.0548	1.6217	1.2264
S1 to Z ↓	0.0462	0.0518	1.2177	0.9125
S1 to Z ↑	0.0391	0.0427	1.6195	1.2247

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	1.749e-05	1.000e-20
X9_P16	2.721e-05	1.000e-20
X13_P16	4.594e-05	1.000e-20
X18_P16	5.111e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X9_P16	X13_P16	X18_P16
D0 (output stable)	4.301e-05	4.889e-05	1.146e-04	1.134e-04
D1 (output stable)	5.932e-05	6.978e-05	9.362e-05	9.289e-05
D2 (output stable)	6.114e-05	7.272e-05	1.076e-04	1.072e-04
D3 (output stable)	4.568e-05	6.975e-05	9.108e-05	9.090e-05
S0 (output stable)	1.574e-03	1.940e-03	3.257e-03	3.257e-03
S1 (output stable)	1.558e-03	1.792e-03	2.914e-03	2.914e-03
D0 to Z	4.226e-03	6.529e-03	1.036e-02	1.307e-02
D1 to Z	4.178e-03	6.511e-03	1.046e-02	1.318e-02
D2 to Z	3.967e-03	6.510e-03	9.884e-03	1.246e-02
D3 to Z	4.013e-03	6.504e-03	9.897e-03	1.246e-02
S0 to Z	5.962e-03	8.842e-03	1.400e-02	1.667e-02
S1 to Z	4.538e-03	6.928e-03	1.084e-02	1.346e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

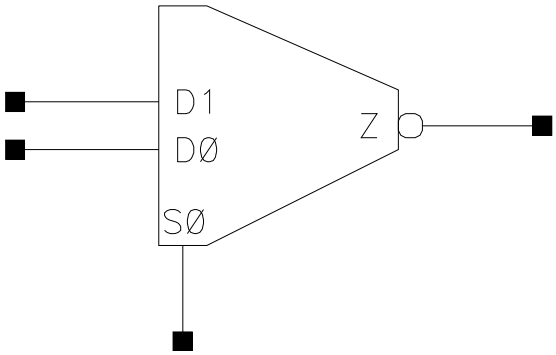
Pin Cycle (vdds)	X4_P16	X9_P16	X13_P16	X18_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P16	0.800	0.952	0.7616
X2_P16	0.800	0.952	0.7616
X6_P16	0.800	1.904	1.5232
X9_P16	0.800	2.448	1.9584
X12_P16	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P16	X2_P16	X6_P16	X9_P16
D0	0.0004	0.0006	0.0014	0.0020
D1	0.0004	0.0006	0.0013	0.0020
S0	0.0011	0.0015	0.0021	0.0031
	X12_P16			
D0	0.0027			
D1	0.0026			
S0	0.0035			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P16	X2_P16	X1_P16	X2_P16
D0 to Z ↓	0.0112	0.0109	8.5201	5.8964

D0 to Z ↑	0.0224	0.0178	17.7158	9.8209
D1 to Z ↓	0.0107	0.0103	8.4189	5.7654
D1 to Z ↑	0.0228	0.0184	17.7367	9.9810
S0 to Z ↓	0.0209	0.0153	8.4398	5.8332
S0 to Z ↑	0.0236	0.0162	17.6462	9.8802
	X6_P16	**X9_P16**	**X6_P16**	**X9_P16**
D0 to Z ↓	0.0124	0.0114	2.6713	1.7937
D0 to Z ↑	0.0185	0.0177	4.1234	2.8768
D1 to Z ↓	0.0118	0.0115	2.6147	1.8038
D1 to Z ↑	0.0198	0.0183	4.2562	2.8112
S0 to Z ↓	0.0184	0.0157	2.6378	1.7971
S0 to Z ↑	0.0191	0.0168	4.1780	2.8403
	X12_P16		**X12_P16**	
D0 to Z ↓	0.0118		1.3724	
D0 to Z ↑	0.0177		2.1694	
D1 to Z ↓	0.0113		1.3662	
D1 to Z ↑	0.0181		2.1164	
S0 to Z ↓	0.0172		1.3673	
S0 to Z ↑	0.0180		2.1392	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X1_P16	6.454e-06	1.000e-20
X2_P16	1.186e-05	1.000e-20
X6_P16	2.364e-05	1.000e-20
X9_P16	3.697e-05	1.000e-20
X12_P16	4.507e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X1_P16	X2_P16	X6_P16	X9_P16
D0 (output stable)	1.033e-05	2.242e-05	6.889e-05	9.713e-05
D1 (output stable)	9.989e-06	2.397e-05	7.393e-05	1.056e-04
S0 (output stable)	1.138e-03	1.374e-03	2.353e-03	3.702e-03
D0 to Z	9.983e-04	1.339e-03	3.452e-03	4.747e-03
D1 to Z	9.966e-04	1.330e-03	3.486e-03	4.840e-03
S0 to Z	1.954e-03	2.282e-03	4.711e-03	6.787e-03
	X12_P16			
D0 (output stable)	1.279e-04			
D1 (output stable)	1.314e-04			
S0 (output stable)	4.303e-03			
D0 to Z	6.404e-03			
D1 to Z	6.387e-03			
S0 to Z	8.517e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X1_P16	X2_P16	X6_P16	X9_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

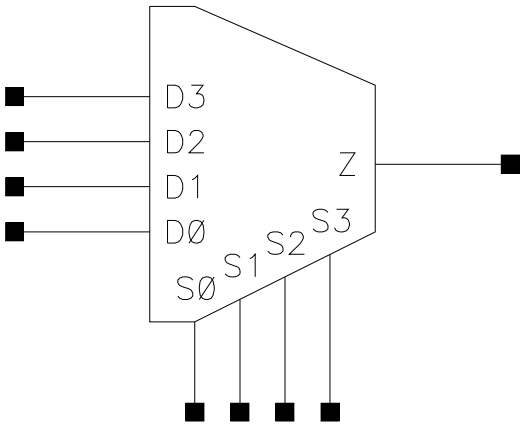
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P16			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.600	0.952	1.5232
X15_P16	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P16	X15_P16
D0	0.0007	0.0017
D1	0.0007	0.0014
D2	0.0007	0.0017
D3	0.0007	0.0015
S0	0.0007	0.0015
S1	0.0007	0.0017
S2	0.0007	0.0016
S3	0.0007	0.0016

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X15_P16	X4_P16	X15_P16
D0 to Z ↓	0.0383	0.0417	5.0821	1.3399
D0 to Z ↑	0.0330	0.0325	4.4925	1.1378
D1 to Z ↓	0.0358	0.0386	5.0787	1.3387
D1 to Z ↑	0.0278	0.0281	4.4652	1.1324
D2 to Z ↓	0.0376	0.0408	5.0899	1.3411
D2 to Z ↑	0.0318	0.0306	4.5100	1.1446
D3 to Z ↓	0.0348	0.0378	5.0815	1.3384
D3 to Z ↑	0.0268	0.0264	4.4851	1.1375
S0 to Z ↓	0.0362	0.0379	5.0790	1.3381
S0 to Z ↑	0.0356	0.0336	4.4916	1.1375
S1 to Z ↓	0.0333	0.0352	5.0767	1.3370
S1 to Z ↑	0.0300	0.0292	4.4694	1.1322
S2 to Z ↓	0.0360	0.0372	5.0874	1.3387
S2 to Z ↑	0.0344	0.0320	4.5070	1.1435
S3 to Z ↓	0.0335	0.0344	5.0817	1.3364
S3 to Z ↑	0.0294	0.0274	4.4873	1.1376

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	2.062e-05	1.000e-20
X15_P16	6.003e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X15_P16
D0 (output stable)	5.548e-04	1.567e-03
D1 (output stable)	4.566e-04	1.292e-03
D2 (output stable)	5.420e-04	1.508e-03
D3 (output stable)	4.469e-04	1.234e-03
S0 (output stable)	5.243e-04	1.515e-03
S1 (output stable)	4.318e-04	1.276e-03
S2 (output stable)	5.210e-04	1.471e-03
S3 (output stable)	4.271e-04	1.232e-03
D0 to Z	4.188e-03	1.246e-02
D1 to Z	3.561e-03	1.077e-02
D2 to Z	3.856e-03	1.118e-02
D3 to Z	3.248e-03	9.512e-03
S0 to Z	4.013e-03	1.164e-02
S1 to Z	3.402e-03	1.006e-02
S2 to Z	3.710e-03	1.042e-02
S3 to Z	3.113e-03	8.775e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

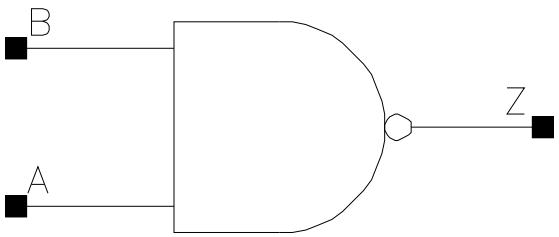
Pin Cycle (vdds)	X4_P16	X15_P16
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P16	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P16	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P16	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P16	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P16	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P16	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P16	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P16	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P16	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P16	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P16	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P16	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P16	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P16	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P16	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P16	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P16	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P16	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P16	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P16	C8T28SOI_LL_-NAND2X4_P16	C8T28SOI_LL_-NAND2X8_P16	C8T28SOI_LL_-NAND2X12_P16
A	0.0004	0.0007	0.0013	0.0020
B	0.0004	0.0006	0.0012	0.0018
	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X24_P16	C8T28SOI_-LLBR0P8_-NAND2X4_P16
A	0.0026	0.0032	0.0008	0.0008
B	0.0024	0.0030	0.0008	0.0007
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	C8T28SOI_-LLBR0P8_-NAND2X12_P16	C8T28SOI_-LLBR0P8_-NAND2X16_P16	C8T28SOI_LLS_-NAND2X8_P16
A	0.0013	0.0020	0.0026	0.0013
B	0.0012	0.0018	0.0023	0.0012
	C8T28SOI_LLS_-NAND2X15_P16	C8T28SOI_LLS_-NAND2X23_P16	C8T28SOI_LLS_-NAND2X31_P16	C8T28SOIDV_LL_-NAND2X9_P16
A	0.0027	0.0040	0.0054	0.0014
B	0.0025	0.0037	0.0049	0.0014
	C8T28SOIDV_LL_-NAND2X18_P16	C8T28SOIDV_LL_-NAND2X27_P16	C8T28SOIDV_LL_-NAND2X36_P16	
A	0.0028	0.0042	0.0057	
B	0.0026	0.0039	0.0052	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-NAND2X2_P16	**C8T28SOI_LL_-NAND2X4_P16**	**C8T28SOI_LL_-NAND2X2_P16**	**C8T28SOI_LL_-NAND2X4_P16**
A to Z ↓	0.0084	0.0074	9.0752	5.1259
A to Z ↑	0.0142	0.0121	8.7639	4.8082
B to Z ↓	0.0100	0.0086	9.1824	5.1859
B to Z ↑	0.0127	0.0102	8.8146	4.8745
	C8T28SOI_LL_-NAND2X8_P16	**C8T28SOI_LL_-NAND2X12_P16**	**C8T28SOI_LL_-NAND2X8_P16**	**C8T28SOI_LL_-NAND2X12_P16**
A to Z ↓	0.0083	0.0079	2.6141	1.7863
A to Z ↑	0.0122	0.0120	2.2984	1.5656
B to Z ↓	0.0081	0.0086	2.6432	1.8073
B to Z ↑	0.0091	0.0094	2.3179	1.5876

	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16
A to Z ↓	0.0081	0.0080	1.3537	1.0933
A to Z ↑	0.0120	0.0120	1.1797	0.9545
B to Z ↓	0.0082	0.0086	1.3709	1.1073
B to Z ↑	0.0089	0.0092	1.1946	0.9673
	C8T28SOI_LL_-NAND2X24_P16	**C8T28SOI_-LLBR0P8_-NAND2X4_P16**	**C8T28SOI_LL_-NAND2X24_P16**	**C8T28SOI_-LLBR0P8_-NAND2X4_P16**
A to Z ↓	0.0354	0.0057	0.6394	3.6769
A to Z ↑	0.0367	0.0158	0.9352	6.0147
B to Z ↓	0.0370	0.0063	0.6397	3.7452
B to Z ↑	0.0349	0.0128	0.9354	6.0542
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	**C8T28SOI_-LLBR0P8_-NAND2X12_P16**	**C8T28SOI_-LLBR0P8_-NAND2X8_P16**	**C8T28SOI_-LLBR0P8_-NAND2X12_P16**
A to Z ↓	0.0063	0.0062	2.0206	1.3809
A to Z ↑	0.0159	0.0159	3.0268	2.0472
B to Z ↓	0.0055	0.0061	2.0591	1.4073
B to Z ↑	0.0113	0.0118	3.0534	2.0639
	C8T28SOI_-LLBR0P8_-NAND2X16_P16	**C8T28SOI_LLS_-NAND2X8_P16**	**C8T28SOI_-LLBR0P8_-NAND2X16_P16**	**C8T28SOI_LLS_-NAND2X8_P16**
A to Z ↓	0.0060	0.0083	1.0540	2.6040
A to Z ↑	0.0153	0.0124	1.5315	2.3271
B to Z ↓	0.0054	0.0081	1.0748	2.6328
B to Z ↑	0.0108	0.0092	1.5491	2.3581
	C8T28SOI_LLS_-NAND2X15_P16	**C8T28SOI_LLS_-NAND2X23_P16**	**C8T28SOI_LLS_-NAND2X15_P16**	**C8T28SOI_LLS_-NAND2X23_P16**
A to Z ↓	0.0081	0.0081	1.3501	0.9108
A to Z ↑	0.0119	0.0119	1.1614	0.7742
B to Z ↓	0.0083	0.0085	1.3672	0.9219
B to Z ↑	0.0089	0.0089	1.1718	0.7817
	C8T28SOI_LLS_-NAND2X31_P16	**C8T28SOIDV_LL_-NAND2X9_P16**	**C8T28SOI_LLS_-NAND2X31_P16**	**C8T28SOIDV_LL_-NAND2X9_P16**
A to Z ↓	0.0081	0.0070	0.6895	2.0425
A to Z ↑	0.0119	0.0128	0.5824	2.2531
B to Z ↓	0.0086	0.0078	0.6978	2.0700
B to Z ↑	0.0090	0.0105	0.5880	2.2939
	C8T28SOIDV_LL_-NAND2X18_P16	**C8T28SOIDV_LL_-NAND2X27_P16**	**C8T28SOIDV_LL_-NAND2X18_P16**	**C8T28SOIDV_LL_-NAND2X27_P16**
A to Z ↓	0.0076	0.0075	1.0389	0.7073
A to Z ↑	0.0133	0.0132	1.1315	0.7630
B to Z ↓	0.0073	0.0079	1.0533	0.7172
B to Z ↑	0.0098	0.0102	1.1416	0.7694
	C8T28SOIDV_LL_-NAND2X36_P16		**C8T28SOIDV_LL_-NAND2X36_P16**	
A to Z ↓	0.0076		0.5323	
A to Z ↑	0.0132		0.5713	
B to Z ↓	0.0074		0.5401	
B to Z ↑	0.0096		0.5768	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P16	2.829e-06	1.000e-20
C8T28SOI_LL_NAND2X4_P16	5.713e-06	1.000e-20
C8T28SOI_LL_NAND2X8_P16	1.142e-05	1.000e-20
C8T28SOI_LL_NAND2X12_P16	1.660e-05	1.000e-20
C8T28SOI_LL_NAND2X15_P16	2.178e-05	1.000e-20
C8T28SOI_LL_NAND2X19_P16	2.697e-05	1.000e-20
C8T28SOI_LL_NAND2X24_P16	3.836e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P16	5.935e-06	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P16	1.086e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_-P16	1.564e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_-P16	2.044e-05	1.000e-20
C8T28SOI_LLS_NAND2X8_P16	1.142e-05	1.000e-20
C8T28SOI_LLS_NAND2X15_P16	2.178e-05	1.000e-20
C8T28SOI_LLS_NAND2X23_P16	3.216e-05	1.000e-20
C8T28SOI_LLS_NAND2X31_P16	4.253e-05	1.000e-20
C8T28SOIDV_LL_NAND2X9_P16	1.316e-05	1.000e-20
C8T28SOIDV_LL_NAND2X18_P16	2.525e-05	1.000e-20
C8T28SOIDV_LL_NAND2X27_P16	3.679e-05	1.000e-20
C8T28SOIDV_LL_NAND2X36_P16	4.833e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P16	C8T28SOI_LL_-NAND2X4_P16	C8T28SOI_LL_-NAND2X8_P16	C8T28SOI_LL_-NAND2X12_P16
A (output stable)	7.094e-06	1.331e-05	6.051e-05	7.595e-05
B (output stable)	1.667e-05	3.066e-05	2.422e-04	2.290e-04
A to Z	6.901e-04	1.091e-03	2.350e-03	3.409e-03
B to Z	5.824e-04	8.924e-04	1.742e-03	2.661e-03
	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X24_P16	C8T28SOI_-LLBR0P8_-NAND2X4_P16
A (output stable)	1.110e-04	1.243e-04	1.510e-05	1.820e-05
B (output stable)	4.184e-04	3.708e-04	3.417e-05	4.206e-05
A to Z	4.554e-03	5.625e-03	1.069e-02	1.209e-03
B to Z	3.425e-03	4.365e-03	1.050e-02	9.363e-04
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	C8T28SOI_-LLBR0P8_-NAND2X12_P16	C8T28SOI_-LLBR0P8_-NAND2X16_P16	C8T28SOI_LLS_-NAND2X8_P16
A (output stable)	7.233e-05	8.658e-05	1.372e-04	6.155e-05
B (output stable)	2.858e-04	2.648e-04	4.853e-04	2.580e-04
A to Z	2.441e-03	3.629e-03	4.625e-03	2.360e-03
B to Z	1.636e-03	2.601e-03	3.135e-03	1.748e-03
	C8T28SOI_LLS_-NAND2X15_P16	C8T28SOI_LLS_-NAND2X23_P16	C8T28SOI_LLS_-NAND2X31_P16	C8T28SOIDV_LL_-NAND2X9_P16
A (output stable)	1.174e-04	1.706e-04	2.191e-04	3.291e-05
B (output stable)	4.363e-04	6.109e-04	7.449e-04	7.644e-05
A to Z	4.598e-03	6.847e-03	9.076e-03	2.535e-03
B to Z	3.461e-03	5.206e-03	6.948e-03	2.050e-03
	C8T28SOIDV_LL_-NAND2X18_P16	C8T28SOIDV_LL_-NAND2X27_P16	C8T28SOIDV_LL_-NAND2X36_P16	
A (output stable)	1.323e-04	1.609e-04	2.703e-04	

B (output stable)	5.677e-04	4.366e-04	1.118e-03	
A to Z	5.227e-03	7.738e-03	1.032e-02	
B to Z	3.831e-03	6.025e-03	7.570e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

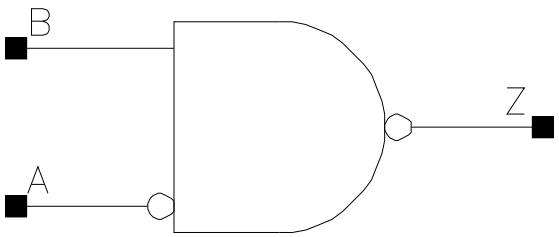
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P16	C8T28SOI_LL_-NAND2X4_P16	C8T28SOI_LL_-NAND2X8_P16	C8T28SOI_LL_-NAND2X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P16	C8T28SOI_LL_-NAND2X19_P16	C8T28SOI_LL_-NAND2X24_P16	C8T28SOI_-LLBR0P8_-NAND2X4_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P16	C8T28SOI_-LLBR0P8_-NAND2X12_P16	C8T28SOI_-LLBR0P8_-NAND2X16_P16	C8T28SOI_LLS_-NAND2X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P16	C8T28SOI_LLS_-NAND2X23_P16	C8T28SOI_LLS_-NAND2X31_P16	C8T28SOIDV_LL_-NAND2X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P16	C8T28SOIDV_LL_-NAND2X27_P16	C8T28SOIDV_LL_-NAND2X36_P16	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.544	0.4352
X4_P16	0.800	0.680	0.5440
X9_P16	1.600	0.544	0.8704
X13_P16	1.600	0.816	1.3056
X17_P16	1.600	0.816	1.3056
X23_P16	0.800	2.312	1.8496
X27_P16	1.600	1.088	1.7408
X31_P16	0.800	2.992	2.3936
X36_P16	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P16	X4_P16	X9_P16	X13_P16
A	0.0006	0.0007	0.0011	0.0011
B	0.0004	0.0006	0.0013	0.0021
	X17_P16	X23_P16	X27_P16	X31_P16
A	0.0011	0.0023	0.0018	0.0031
B	0.0026	0.0036	0.0040	0.0047
	X36_P16			
A	0.0018			
B	0.0052			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X4_P16**	**X2_P16**	**X4_P16**
A to Z ↓	0.0245	0.0258	9.0452	5.1650
A to Z ↑	0.0193	0.0200	8.5592	4.6686
B to Z ↓	0.0102	0.0087	9.2782	5.2861
B to Z ↑	0.0127	0.0101	8.8193	4.8725
	X9_P16	**X13_P16**	**X9_P16**	**X13_P16**
A to Z ↓	0.0263	0.0321	2.0836	1.3129
A to Z ↑	0.0200	0.0244	2.2175	1.4673
B to Z ↓	0.0080	0.0078	2.1420	1.3483
B to Z ↑	0.0105	0.0108	2.3068	1.5450
	X17_P16	**X23_P16**	**X17_P16**	**X23_P16**
A to Z ↓	0.0354	0.0250	1.0418	0.9041
A to Z ↑	0.0257	0.0205	1.1369	0.7725
B to Z ↓	0.0076	0.0083	1.0669	0.9273
B to Z ↑	0.0103	0.0089	1.1999	0.8021
	X27_P16	**X31_P16**	**X27_P16**	**X31_P16**
A to Z ↓	0.0297	0.0249	0.7016	0.6834
A to Z ↑	0.0231	0.0202	0.7547	0.5649
B to Z ↓	0.0075	0.0085	0.7207	0.7002
B to Z ↑	0.0098	0.0091	0.7728	0.6030
	X36_P16		**X36_P16**	
A to Z ↓	0.0343		0.5305	
A to Z ↑	0.0263		0.5667	
B to Z ↓	0.0074		0.5427	
B to Z ↑	0.0096		0.5806	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P16	5.078e-06	1.000e-20
X4_P16	8.261e-06	1.000e-20
X9_P16	1.904e-05	1.000e-20
X13_P16	2.369e-05	1.000e-20
X17_P16	3.011e-05	1.000e-20
X23_P16	4.767e-05	1.000e-20
X27_P16	4.789e-05	1.000e-20
X31_P16	6.279e-05	1.000e-20
X36_P16	5.962e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P16	X4_P16	X9_P16	X13_P16
A (output stable)	1.011e-03	1.283e-03	2.513e-03	3.581e-03
B (output stable)	1.677e-05	3.070e-05	8.001e-05	2.176e-04
A to Z	1.650e-03	2.258e-03	4.862e-03	7.678e-03
B to Z	5.816e-04	8.857e-04	2.060e-03	3.140e-03
	X17_P16	X23_P16	X27_P16	X31_P16
A (output stable)	4.066e-03	6.468e-03	6.439e-03	8.585e-03
B (output stable)	2.639e-04	5.131e-04	4.535e-04	6.794e-04
A to Z	9.346e-03	1.295e-02	1.370e-02	1.721e-02
B to Z	3.910e-03	5.199e-03	5.785e-03	6.910e-03
	X36_P16			
A (output stable)	8.237e-03			

B (output stable)	7.526e-04			
A to Z	1.837e-02			
B to Z	7.494e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

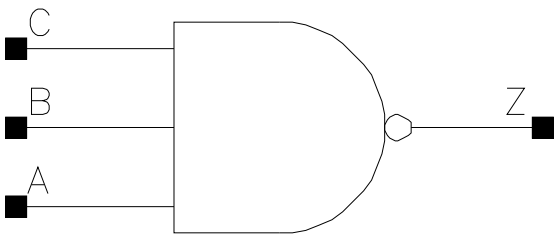
Pin Cycle (vdds)	X2_P16	X4_P16	X9_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P16	X23_P16	X27_P16	X31_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P16	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P16	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P16	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P16	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P16	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P16	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P16	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P16	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P16	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P16	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P16	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P16	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P16	C8T28SOI_LL_-NAND3X7_P16	C8T28SOI_LL_-NAND3X10_P16	C8T28SOI_LL_-NAND3X14_P16
A	0.0007	0.0013	0.0020	0.0026
B	0.0006	0.0013	0.0019	0.0025
C	0.0006	0.0012	0.0018	0.0023
	C8T28SOI_LL_-NAND3X20_P16	C8T28SOI_LL_-NAND3X27_P16	C8T28SOI_-LLBR0P6_-NAND3X3_P16	C8T28SOI_-LLBR0P6_-NAND3X7_P16
A	0.0040	0.0053	0.0008	0.0014
B	0.0037	0.0050	0.0007	0.0013
C	0.0035	0.0047	0.0007	0.0012
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	C8T28SOI_-LLBR0P6_-NAND3X14_P16	C8T28SOI_-LLBR0P6_-NAND3X20_P16	C8T28SOI_-LLBR0P6_-NAND3X27_P16
A	0.0020	0.0027	0.0040	0.0053
B	0.0018	0.0024	0.0036	0.0049
C	0.0018	0.0024	0.0035	0.0047

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND3X3_P16	**C8T28SOI_LL_-NAND3X7_P16**	**C8T28SOI_LL_-NAND3X3_P16**	**C8T28SOI_LL_-NAND3X7_P16**
A to Z ↓	0.0114	0.0130	7.2887	3.7068
A to Z ↑	0.0151	0.0156	4.8633	2.3832
B to Z ↓	0.0122	0.0128	7.3146	3.7209
B to Z ↑	0.0136	0.0139	4.8855	2.3893
C to Z ↓	0.0128	0.0123	7.3618	3.7370
C to Z ↑	0.0118	0.0110	4.9348	2.3242
	C8T28SOI_LL_-NAND3X10_P16	**C8T28SOI_LL_-NAND3X14_P16**	**C8T28SOI_LL_-NAND3X10_P16**	**C8T28SOI_LL_-NAND3X14_P16**
A to Z ↓	0.0123	0.0127	2.5465	1.9284
A to Z ↑	0.0147	0.0151	1.5401	1.2004
B to Z ↓	0.0126	0.0125	2.5575	1.9357
B to Z ↑	0.0132	0.0134	1.5867	1.2005
C to Z ↓	0.0123	0.0122	2.5704	1.9454
C to Z ↑	0.0107	0.0106	1.6005	1.1926
	C8T28SOI_LL_-NAND3X20_P16	**C8T28SOI_LL_-NAND3X27_P16**	**C8T28SOI_LL_-NAND3X20_P16**	**C8T28SOI_LL_-NAND3X27_P16**
A to Z ↓	0.0122	0.0124	1.3091	0.9956
A to Z ↑	0.0145	0.0145	0.7756	0.5847
B to Z ↓	0.0126	0.0126	1.3146	0.9997
B to Z ↑	0.0130	0.0129	0.7762	0.5841
C to Z ↓	0.0122	0.0123	1.3214	1.0048
C to Z ↑	0.0103	0.0103	0.7981	0.6009
	C8T28SOI_-LLBR0P6_-NAND3X3_P16	**C8T28SOI_-LLBR0P6_-NAND3X7_P16**	**C8T28SOI_-LLBR0P6_-NAND3X3_P16**	**C8T28SOI_-LLBR0P6_-NAND3X7_P16**
A to Z ↓	0.0080	0.0101	4.6673	2.6312
A to Z ↑	0.0219	0.0234	7.0357	3.5839
B to Z ↓	0.0079	0.0093	4.7181	2.6520
B to Z ↑	0.0188	0.0199	7.0429	3.5935

C to Z ↓	0.0077	0.0078	4.7895	2.6840
C to Z ↑	0.0150	0.0148	7.1080	3.5661
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	**C8T28SOI_-LLBR0P6_-NAND3X14_P16**	**C8T28SOI_-LLBR0P6_-NAND3X10_P16**	**C8T28SOI_-LLBR0P6_-NAND3X14_P16**
A to Z ↓	0.0091	0.0098	1.7494	1.3317
A to Z ↑	0.0222	0.0227	2.3895	1.8101
B to Z ↓	0.0085	0.0086	1.7667	1.3440
B to Z ↑	0.0186	0.0190	2.4009	1.8143
C to Z ↓	0.0074	0.0071	1.7905	1.3625
C to Z ↑	0.0140	0.0138	2.4223	1.8135
	C8T28SOI_-LLBR0P6_-NAND3X20_P16	**C8T28SOI_-LLBR0P6_-NAND3X27_P16**	**C8T28SOI_-LLBR0P6_-NAND3X20_P16**	**C8T28SOI_-LLBR0P6_-NAND3X27_P16**
A to Z ↓	0.0092	0.0093	0.8984	0.6887
A to Z ↑	0.0222	0.0222	1.2037	0.9077
B to Z ↓	0.0086	0.0085	0.9071	0.6950
B to Z ↑	0.0187	0.0186	1.2058	0.9081
C to Z ↓	0.0071	0.0072	0.9196	0.7046
C to Z ↑	0.0134	0.0134	1.2161	0.9150

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P16	4.781e-06	1.000e-20
C8T28SOI_LL_NAND3X7_P16	1.000e-05	1.000e-20
C8T28SOI_LL_NAND3X10_P16	1.403e-05	1.000e-20
C8T28SOI_LL_NAND3X14_P16	1.892e-05	1.000e-20
C8T28SOI_LL_NAND3X20_P16	2.787e-05	1.000e-20
C8T28SOI_LL_NAND3X27_P16	3.678e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P16	5.099e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P16	9.975e-06	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_-P16	1.361e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_-P16	1.851e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_-P16	2.708e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_-P16	3.558e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P16	C8T28SOI_LL_-NAND3X7_P16	C8T28SOI_LL_-NAND3X10_P16	C8T28SOI_LL_-NAND3X14_P16
A (output stable)	1.709e-05	6.611e-05	8.510e-05	1.260e-04
B (output stable)	4.010e-05	1.680e-04	2.271e-04	3.186e-04
C (output stable)	9.257e-05	4.259e-04	5.380e-04	7.848e-04
A to Z	1.475e-03	3.294e-03	4.634e-03	6.272e-03
B to Z	1.274e-03	2.709e-03	3.796e-03	5.134e-03
C to Z	1.081e-03	2.163e-03	3.048e-03	4.085e-03
	C8T28SOI_LL_-NAND3X20_P16	C8T28SOI_LL_-NAND3X27_P16	C8T28SOI_-LLBR0P6_-NAND3X3_P16	C8T28SOI_-LLBR0P6_-NAND3X7_P16

A (output stable)	1.677e-04	2.239e-04	2.641e-05	8.705e-05
B (output stable)	4.460e-04	5.971e-04	6.294e-05	2.138e-04
C (output stable)	1.178e-03	1.537e-03	1.484e-04	5.686e-04
A to Z	9.178e-03	1.216e-02	1.637e-03	3.658e-03
B to Z	7.537e-03	9.967e-03	1.306e-03	2.798e-03
C to Z	5.892e-03	7.854e-03	9.837e-04	1.948e-03
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	C8T28SOI_-LLBR0P6_-NAND3X14_P16	C8T28SOI_-LLBR0P6_-NAND3X20_P16	C8T28SOI_-LLBR0P6_-NAND3X27_P16
A (output stable)	1.120e-04	1.781e-04	2.300e-04	3.130e-04
B (output stable)	2.889e-04	4.505e-04	6.060e-04	8.130e-04
C (output stable)	7.188e-04	1.102e-03	1.580e-03	2.043e-03
A to Z	5.041e-03	6.964e-03	1.009e-02	1.337e-02
B to Z	3.767e-03	5.180e-03	7.527e-03	9.919e-03
C to Z	2.659e-03	3.517e-03	5.080e-03	6.730e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

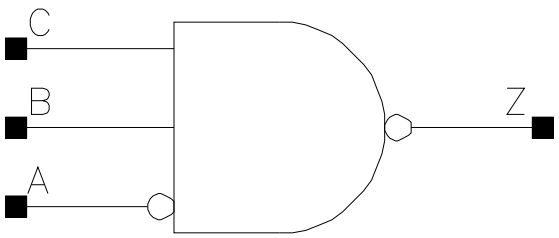
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P16	C8T28SOI_LL_-NAND3X7_P16	C8T28SOI_LL_-NAND3X10_P16	C8T28SOI_LL_-NAND3X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P16	C8T28SOI_LL_-NAND3X27_P16	C8T28SOI_-LLBR0P6_-NAND3X3_P16	C8T28SOI_-LLBR0P6_-NAND3X7_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P16	C8T28SOI_-LLBR0P6_-NAND3X14_P16	C8T28SOI_-LLBR0P6_-NAND3X20_P16	C8T28SOI_-LLBR0P6_-NAND3X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X7_P16	0.800	1.360	1.0880
X10_P16	0.800	1.632	1.3056
X14_P16	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X10_P16	X14_P16
A	0.0007	0.0011	0.0009	0.0009
B	0.0006	0.0013	0.0019	0.0025
C	0.0007	0.0012	0.0018	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0309	0.0308	7.2909	3.7144
A to Z ↑	0.0226	0.0236	4.6805	2.2685
B to Z ↓	0.0118	0.0126	7.3616	3.7482
B to Z ↑	0.0133	0.0134	4.8908	2.3278
C to Z ↓	0.0124	0.0118	7.4109	3.7638
C to Z ↑	0.0114	0.0105	4.9461	2.3286
	X10_P16	**X14_P16**	**X10_P16**	**X14_P16**
A to Z ↓	0.0343	0.0375	2.5359	1.9329

A to Z ↑	0.0266	0.0293	1.5495	1.1590
B to Z ↓	0.0126	0.0122	2.5558	1.9468
B to Z ↑	0.0132	0.0129	1.5887	1.1882
C to Z ↓	0.0122	0.0118	2.5683	1.9563
C to Z ↑	0.0107	0.0101	1.6039	1.1943

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	7.064e-06	1.000e-20
X7_P16	1.523e-05	1.000e-20
X10_P16	1.927e-05	1.000e-20
X14_P16	2.422e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	1.288e-03	2.411e-03	3.077e-03	3.735e-03
B (output stable)	4.148e-05	1.394e-04	2.368e-04	2.882e-04
C (output stable)	9.337e-05	4.383e-04	5.629e-04	7.777e-04
A to Z	2.652e-03	5.592e-03	7.792e-03	1.006e-02
B to Z	1.220e-03	2.611e-03	3.790e-03	4.963e-03
C to Z	1.026e-03	2.033e-03	3.035e-03	3.896e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

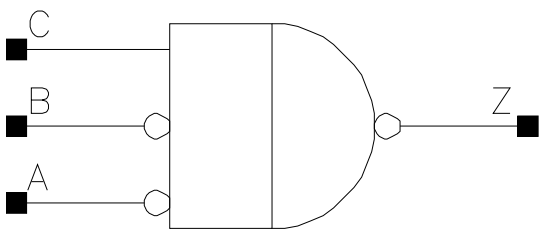
Pin Cycle (vdds)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	0.816	0.6528
X8_P16	0.800	1.088	0.8704
X12_P16	0.800	1.632	1.3056
X15_P16	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X12_P16	X15_P16
A	0.0008	0.0008	0.0015	0.0014
B	0.0009	0.0008	0.0016	0.0014
C	0.0007	0.0012	0.0018	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0269	0.0337	4.8603	2.5934
A to Z ↑	0.0197	0.0232	4.4888	2.2416
B to Z ↓	0.0281	0.0351	4.8606	2.5933
B to Z ↑	0.0181	0.0218	4.4846	2.2407
C to Z ↓	0.0089	0.0082	4.9616	2.6351
C to Z ↑	0.0103	0.0092	4.5511	2.3381
	X12_P16	**X15_P16**	**X12_P16**	**X15_P16**
A to Z ↓	0.0308	0.0339	1.7682	1.3488
A to Z ↑	0.0213	0.0253	1.4966	1.1266
B to Z ↓	0.0303	0.0336	1.7674	1.3484

B to Z ↑	0.0191	0.0230	1.4926	1.1259
C to Z ↓	0.0090	0.0082	1.8011	1.3733
C to Z ↑	0.0097	0.0088	1.5864	1.1692

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	1.100e-05	1.000e-20
X8_P16	1.484e-05	1.000e-20
X12_P16	2.402e-05	1.000e-20
X15_P16	2.680e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	6.865e-04	9.349e-04	1.581e-03	1.797e-03
B (output stable)	6.163e-04	8.624e-04	1.415e-03	1.630e-03
C (output stable)	3.352e-05	2.468e-04	2.351e-04	3.975e-04
A to Z	3.119e-03	5.178e-03	8.131e-03	9.956e-03
B to Z	2.865e-03	4.923e-03	7.342e-03	9.162e-03
C to Z	9.855e-04	1.775e-03	2.794e-03	3.471e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

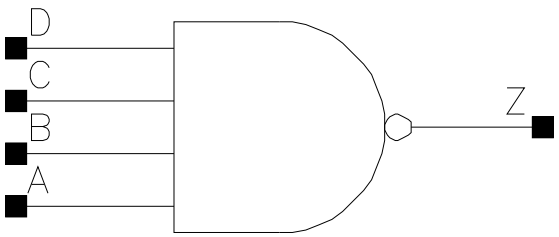
Pin Cycle (vdds)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.224	0.9792
X10_P16	0.800	1.360	1.0880
X14_P16	0.800	1.904	1.5232
X18_P16	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X18_P16
A	0.0005	0.0006	0.0006	0.0007
B	0.0006	0.0006	0.0007	0.0009
C	0.0005	0.0005	0.0006	0.0008
D	0.0006	0.0006	0.0007	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0441	0.0425	3.0784	1.5518
A to Z ↑	0.0377	0.0394	4.5154	2.2894
B to Z ↓	0.0463	0.0449	3.0758	1.5510
B to Z ↑	0.0362	0.0385	4.5177	2.2893
C to Z ↓	0.0453	0.0432	3.0769	1.5514
C to Z ↑	0.0388	0.0411	4.5113	2.2891

D to Z ↓	0.0480	0.0459	3.0746	1.5515
D to Z ↑	0.0380	0.0404	4.5125	2.2894
	X14_P16	**X18_P16**	**X14_P16**	**X18_P16**
A to Z ↓	0.0462	0.0434	1.0717	0.8619
A to Z ↑	0.0396	0.0391	1.5685	1.2361
B to Z ↓	0.0486	0.0456	1.0722	0.8624
B to Z ↑	0.0381	0.0379	1.5702	1.2368
C to Z ↓	0.0445	0.0401	1.0712	0.8618
C to Z ↑	0.0397	0.0382	1.5657	1.2340
D to Z ↓	0.0470	0.0420	1.0704	0.8624
D to Z ↑	0.0387	0.0366	1.5656	1.2337

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.205e-05	1.000e-20
X10_P16	1.837e-05	1.000e-20
X14_P16	2.621e-05	1.000e-20
X18_P16	3.349e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	5.067e-04	6.168e-04	9.075e-04	1.006e-03
B (output stable)	4.677e-04	5.730e-04	8.525e-04	9.460e-04
C (output stable)	5.242e-04	5.798e-04	8.861e-04	9.041e-04
D (output stable)	4.817e-04	5.369e-04	8.251e-04	8.321e-04
A to Z	3.768e-03	5.603e-03	8.650e-03	1.019e-02
B to Z	3.663e-03	5.491e-03	8.491e-03	1.002e-02
C to Z	3.917e-03	5.630e-03	8.207e-03	9.438e-03
D to Z	3.826e-03	5.530e-03	8.063e-03	9.255e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

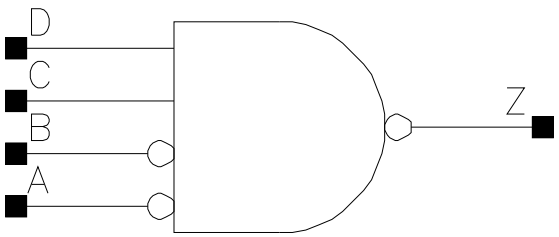
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.952	0.7616
X7_P16	0.800	1.360	1.0880
X10_P16	0.800	2.040	1.6320
X14_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P16	X7_P16	X10_P16	X14_P16
A	0.0008	0.0008	0.0016	0.0014
B	0.0008	0.0008	0.0016	0.0015
C	0.0008	0.0013	0.0019	0.0025
D	0.0006	0.0012	0.0018	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X7_P16	X3_P16	X7_P16
A to Z ↓	0.0311	0.0369	7.0253	3.7151
A to Z ↑	0.0216	0.0251	4.5469	2.2785
B to Z ↓	0.0318	0.0380	7.0299	3.7151
B to Z ↑	0.0198	0.0235	4.5414	2.2762
C to Z ↓	0.0122	0.0124	7.0997	3.7396
C to Z ↑	0.0137	0.0133	4.6888	2.3315

D to Z ↓	0.0124	0.0117	7.1321	3.7555
D to Z ↑	0.0114	0.0104	4.6928	2.3294
	X10_P16	**X14_P16**	**X10_P16**	**X14_P16**
A to Z ↓	0.0345	0.0379	2.5355	1.9393
A to Z ↑	0.0231	0.0289	1.5354	1.1357
B to Z ↓	0.0339	0.0378	2.5357	1.9393
B to Z ↑	0.0209	0.0267	1.5325	1.1345
C to Z ↓	0.0125	0.0122	2.5527	1.9501
C to Z ↑	0.0132	0.0130	1.5908	1.1901
D to Z ↓	0.0122	0.0119	2.5649	1.9596
D to Z ↑	0.0106	0.0102	1.6041	1.1961

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	9.947e-06	1.000e-20
X7_P16	1.310e-05	1.000e-20
X10_P16	2.180e-05	1.000e-20
X14_P16	2.368e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	8.534e-04	1.158e-03	2.018e-03	2.349e-03
B (output stable)	7.604e-04	1.064e-03	1.765e-03	2.110e-03
C (output stable)	8.665e-05	1.683e-04	2.626e-04	3.496e-04
D (output stable)	1.911e-04	5.059e-04	6.426e-04	9.007e-04
A to Z	3.593e-03	5.914e-03	9.256e-03	1.175e-02
B to Z	3.351e-03	5.676e-03	8.465e-03	1.099e-02
C to Z	1.309e-03	2.597e-03	3.760e-03	4.960e-03
D to Z	1.113e-03	2.020e-03	3.014e-03	3.910e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

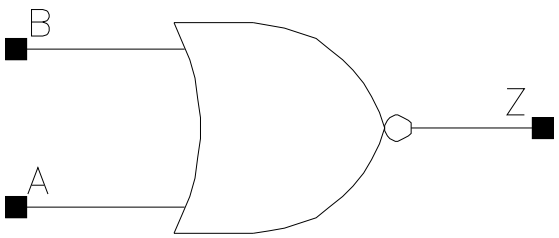
Pin Cycle (vdds)	X3_P16	X7_P16	X10_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.408	0.3264
X4_P16	0.800	0.408	0.3264
X8_P16	0.800	0.680	0.5440
X9_P16	1.600	0.408	0.6528
X12_P16	0.800	0.952	0.7616
X16_P16	0.800	1.224	0.9792
X19_P16	1.600	0.680	1.0880
X20_P16	0.800	1.496	1.1968
X23_P16	0.800	1.496	1.1968
X24_P16	0.800	1.768	1.4144
X27_P16	0.800	1.632	1.3056
X29_P16	1.600	0.952	1.5232
X31_P16	0.800	2.312	1.8496
X34_P16	0.800	2.040	1.6320
X38_P16	0.800	2.176	1.7408
X39_P16	1.600	1.224	1.9584
X46_P16	1.600	1.224	1.9584
X57_P16	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P16	X4_P16	X8_P16	X9_P16
A	0.0005	0.0007	0.0013	0.0014
B	0.0004	0.0006	0.0012	0.0014
	X12_P16	X16_P16	X19_P16	X20_P16

A	0.0021	0.0026	0.0028	0.0034
B	0.0018	0.0024	0.0027	0.0030
	X23_P16	X24_P16	X27_P16	X29_P16
A	0.0009	0.0040	0.0009	0.0043
B	0.0008	0.0037	0.0008	0.0040
	X31_P16	X34_P16	X38_P16	X39_P16
A	0.0053	0.0009	0.0009	0.0058
B	0.0049	0.0008	0.0008	0.0053
	X46_P16	X57_P16		
A	0.0008	0.0008		
B	0.0009	0.0009		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X4_P16**	**X2_P16**	**X4_P16**
A to Z ↓	0.0083	0.0081	5.8698	3.2906
A to Z ↑	0.0153	0.0138	15.5793	8.6605
B to Z ↓	0.0069	0.0064	5.9178	3.3226
B to Z ↑	0.0164	0.0145	15.6468	8.6997
	X8_P16	**X9_P16**	**X8_P16**	**X9_P16**
A to Z ↓	0.0075	0.0068	1.5862	1.2781
A to Z ↑	0.0130	0.0129	4.1279	3.9367
B to Z ↓	0.0048	0.0052	1.5915	1.3217
B to Z ↑	0.0116	0.0136	4.1444	3.9537
	X12_P16	**X16_P16**	**X12_P16**	**X16_P16**
A to Z ↓	0.0077	0.0077	1.0849	0.8075
A to Z ↑	0.0126	0.0129	2.7076	2.0690
B to Z ↓	0.0053	0.0051	1.0968	0.8171
B to Z ↑	0.0120	0.0117	2.7217	2.0784
	X19_P16	**X20_P16**	**X19_P16**	**X20_P16**
A to Z ↓	0.0074	0.0079	0.6434	0.6625
A to Z ↑	0.0144	0.0127	2.0160	1.6432
B to Z ↓	0.0053	0.0054	0.6503	0.6703
B to Z ↑	0.0136	0.0120	2.0229	1.6521
	X23_P16	**X24_P16**	**X23_P16**	**X24_P16**
A to Z ↓	0.0328	0.0078	0.6698	0.5488
A to Z ↑	0.0431	0.0127	0.9435	1.3853
B to Z ↓	0.0309	0.0051	0.6698	0.5557
B to Z ↑	0.0440	0.0117	0.9431	1.3921
	X27_P16	**X29_P16**	**X27_P16**	**X29_P16**
A to Z ↓	0.0346	0.0071	0.5586	0.4259
A to Z ↑	0.0448	0.0136	0.7880	1.3532
B to Z ↓	0.0327	0.0050	0.5588	0.4303
B to Z ↑	0.0458	0.0132	0.7880	1.3583
	X31_P16	**X34_P16**	**X31_P16**	**X34_P16**
A to Z ↓	0.0079	0.0360	0.4103	0.4575
A to Z ↑	0.0128	0.0504	1.0385	0.6476
B to Z ↓	0.0054	0.0342	0.4154	0.4576
B to Z ↑	0.0119	0.0516	1.0438	0.6476
	X38_P16	**X39_P16**	**X38_P16**	**X39_P16**
A to Z ↓	0.0371	0.0072	0.3993	0.3243
A to Z ↑	0.0513	0.0138	0.5680	1.0153

B to Z ↓	0.0352	0.0050	0.3994	0.3286
B to Z ↑	0.0526	0.0130	0.5681	1.0188
	X46_P16	**X57_P16**	**X46_P16**	**X57_P16**
A to Z ↓	0.0419	0.0457	0.3097	0.2534
A to Z ↑	0.0525	0.0555	0.5632	0.4535
B to Z ↓	0.0403	0.0441	0.3094	0.2535
B to Z ↑	0.0544	0.0573	0.5632	0.4535

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P16	2.835e-06	1.000e-20
X4_P16	5.670e-06	1.000e-20
X8_P16	1.183e-05	1.000e-20
X9_P16	1.340e-05	1.000e-20
X12_P16	1.725e-05	1.000e-20
X16_P16	2.268e-05	1.000e-20
X19_P16	2.587e-05	1.000e-20
X20_P16	2.811e-05	1.000e-20
X23_P16	4.072e-05	1.000e-20
X24_P16	3.355e-05	1.000e-20
X27_P16	4.605e-05	1.000e-20
X29_P16	3.782e-05	1.000e-20
X31_P16	4.441e-05	1.000e-20
X34_P16	5.853e-05	1.000e-20
X38_P16	6.399e-05	1.000e-20
X39_P16	4.978e-05	1.000e-20
X46_P16	6.555e-05	1.000e-20
X57_P16	7.722e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P16	X4_P16	X8_P16	X9_P16
A (output stable)	1.316e-05	2.238e-05	8.730e-05	4.881e-05
B (output stable)	2.334e-05	4.148e-05	2.218e-04	9.430e-05
A to Z	6.964e-04	1.163e-03	2.340e-03	2.445e-03
B to Z	5.682e-04	9.268e-04	1.608e-03	1.959e-03
	X12_P16	X16_P16	X19_P16	X20_P16
A (output stable)	1.191e-04	1.723e-04	1.835e-04	2.009e-04
B (output stable)	2.880e-04	4.197e-04	4.834e-04	4.566e-04
A to Z	3.480e-03	4.664e-03	5.254e-03	5.816e-03
B to Z	2.509e-03	3.269e-03	3.910e-03	4.185e-03
	X23_P16	X24_P16	X27_P16	X29_P16
A (output stable)	2.429e-05	2.512e-04	2.444e-05	2.375e-04
B (output stable)	4.567e-05	5.851e-04	4.587e-05	5.560e-04
A to Z	1.063e-02	6.901e-03	1.219e-02	7.464e-03
B to Z	1.040e-02	4.888e-03	1.196e-02	5.614e-03
	X31_P16	X34_P16	X38_P16	X39_P16
A (output stable)	3.355e-04	2.578e-05	2.588e-05	3.558e-04
B (output stable)	7.846e-04	4.872e-05	4.874e-05	8.874e-04
A to Z	9.234e-03	1.595e-02	1.756e-02	1.007e-02
B to Z	6.563e-03	1.569e-02	1.730e-02	7.434e-03
	X46_P16	X57_P16		

A (output stable)	2.633e-05	2.653e-05		
B (output stable)	5.004e-05	5.029e-05		
A to Z	1.935e-02	2.419e-02		
B to Z	1.912e-02	2.397e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

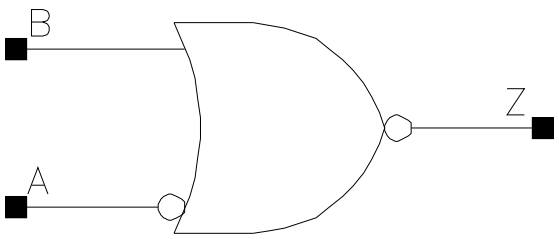
Pin Cycle (vdds)	X2_P16	X4_P16	X8_P16	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P16	X16_P16	X19_P16	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P16	X24_P16	X27_P16	X29_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P16	X34_P16	X38_P16	X39_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P16	X57_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	0.544	0.4352
X3_P16	0.800	0.544	0.4352
X4_P16	0.800	0.544	0.4352
X10_P16	1.600	0.544	0.8704
X14_P16	1.600	0.816	1.3056
X19_P16	1.600	0.816	1.3056
X29_P16	1.600	1.088	1.7408
X39_P16	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P16	X3_P16	X4_P16	X10_P16
A	0.0006	0.0006	0.0007	0.0011
B	0.0004	0.0005	0.0006	0.0013
	X14_P16	X19_P16	X29_P16	X39_P16
A	0.0011	0.0011	0.0018	0.0018
B	0.0021	0.0026	0.0040	0.0052

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	X3_P16	X2_P16	X3_P16
A to Z ↓	0.0240	0.0242	5.6614	4.3546
A to Z ↑	0.0216	0.0215	15.4836	13.2214
B to Z ↓	0.0067	0.0058	5.9551	4.5588

B to Z ↑	0.0157	0.0151	15.6418	13.3302
	X4_P16	**X10_P16**	**X4_P16**	**X10_P16**
A to Z ↓	0.0250	0.0258	3.3846	1.2467
A to Z ↑	0.0217	0.0217	9.7076	3.8847
B to Z ↓	0.0056	0.0052	3.5368	1.2635
B to Z ↑	0.0137	0.0138	9.7942	3.9198
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0314	0.0339	0.7877	0.6171
A to Z ↑	0.0252	0.0265	2.6102	1.9521
B to Z ↓	0.0048	0.0047	0.8681	0.6819
B to Z ↑	0.0130	0.0122	2.6368	1.9715
	X29_P16	**X39_P16**	**X29_P16**	**X39_P16**
A to Z ↓	0.0290	0.0332	0.4134	0.3111
A to Z ↑	0.0251	0.0269	1.3508	0.9943
B to Z ↓	0.0049	0.0047	0.4314	0.3373
B to Z ↑	0.0131	0.0121	1.3635	1.0038

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P16	5.147e-06	1.000e-20
X3_P16	5.959e-06	1.000e-20
X4_P16	7.546e-06	1.000e-20
X10_P16	1.968e-05	1.000e-20
X14_P16	2.407e-05	1.000e-20
X19_P16	3.182e-05	1.000e-20
X29_P16	4.900e-05	1.000e-20
X39_P16	6.139e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P16	X3_P16	X4_P16	X10_P16
A (output stable)	1.017e-03	1.101e-03	1.234e-03	2.565e-03
B (output stable)	2.343e-05	2.735e-05	3.756e-05	9.840e-05
A to Z	1.673e-03	1.840e-03	2.154e-03	4.943e-03
B to Z	5.403e-04	6.196e-04	7.667e-04	2.029e-03
	X14_P16	X19_P16	X29_P16	X39_P16
A (output stable)	3.707e-03	4.285e-03	6.519e-03	8.222e-03
B (output stable)	1.481e-04	1.974e-04	5.583e-04	3.886e-04
A to Z	7.302e-03	8.953e-03	1.390e-02	1.754e-02
B to Z	2.795e-03	3.523e-03	5.560e-03	6.977e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X2_P16	X3_P16	X4_P16	X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P16	X19_P16	X29_P16	X39_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

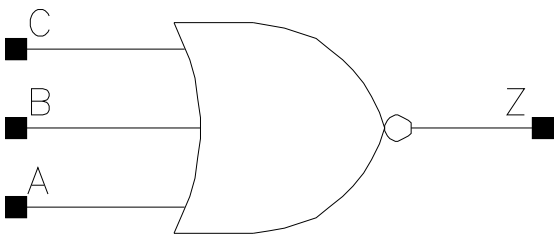
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.544	0.4352
X7_P16	0.800	0.952	0.7616
X11_P16	0.800	1.360	1.0880
X14_P16	0.800	1.768	1.4144
X21_P16	0.800	2.584	2.0672
X29_P16	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X11_P16	X14_P16
A	0.0007	0.0012	0.0020	0.0027
B	0.0007	0.0014	0.0019	0.0028
C	0.0007	0.0011	0.0018	0.0024
	X21_P16	X29_P16		
A	0.0041	0.0055		
B	0.0041	0.0054		
C	0.0036	0.0048		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0093	0.0094	3.3414	1.7455
A to Z ↑	0.0180	0.0186	11.7825	6.0874

B to Z ↓	0.0086	0.0085	3.3663	1.6831
B to Z ↑	0.0174	0.0184	11.8035	6.1004
C to Z ↓	0.0070	0.0057	3.4123	1.7027
C to Z ↑	0.0171	0.0147	11.8238	6.0999
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0093	0.0095	1.0979	0.8409
A to Z ↑	0.0191	0.0184	4.0235	2.9234
B to Z ↓	0.0087	0.0085	1.1063	0.8183
B to Z ↑	0.0175	0.0180	4.0318	2.9299
C to Z ↓	0.0062	0.0059	1.1063	0.8329
C to Z ↑	0.0159	0.0148	4.0342	2.9312
	X21_P16	**X29_P16**	**X21_P16**	**X29_P16**
A to Z ↓	0.0094	0.0095	0.5600	0.4204
A to Z ↑	0.0183	0.0184	1.9629	1.4764
B to Z ↓	0.0086	0.0087	0.5504	0.4161
B to Z ↑	0.0178	0.0178	1.9661	1.4792
C to Z ↓	0.0062	0.0062	0.5615	0.4241
C to Z ↑	0.0151	0.0150	1.9681	1.4805

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	5.156e-06	1.000e-20
X7_P16	1.002e-05	1.000e-20
X11_P16	1.547e-05	1.000e-20
X14_P16	2.073e-05	1.000e-20
X21_P16	3.073e-05	1.000e-20
X29_P16	4.080e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	2.843e-05	6.548e-05	1.190e-04	1.357e-04
B (output stable)	1.541e-05	4.755e-05	6.474e-05	9.264e-05
C (output stable)	6.513e-05	2.052e-04	2.541e-04	4.169e-04
A to Z	1.464e-03	2.964e-03	4.671e-03	6.126e-03
B to Z	1.206e-03	2.477e-03	3.632e-03	5.099e-03
C to Z	9.633e-04	1.681e-03	2.776e-03	3.544e-03
	X21_P16	X29_P16		
A (output stable)	2.028e-04	2.681e-04		
B (output stable)	1.387e-04	1.844e-04		
C (output stable)	6.048e-04	8.187e-04		
A to Z	9.088e-03	1.213e-02		
B to Z	7.521e-03	1.004e-02		
C to Z	5.304e-03	7.080e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

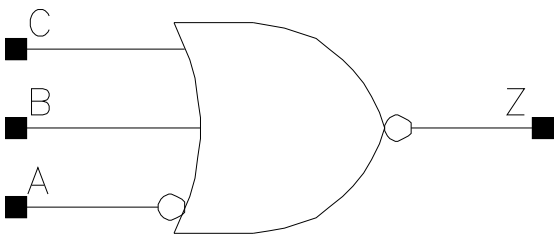
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P16	X29_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X7_P16	0.800	1.360	1.0880
X11_P16	0.800	1.632	1.3056
X14_P16	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X11_P16	X14_P16
A	0.0008	0.0008	0.0011	0.0016
B	0.0007	0.0013	0.0019	0.0025
C	0.0007	0.0012	0.0018	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0271	0.0252	3.2082	1.5156
A to Z ↑	0.0287	0.0295	11.8108	5.7927
B to Z ↓	0.0086	0.0085	3.3786	1.5997
B to Z ↑	0.0173	0.0182	11.8756	5.8210
C to Z ↓	0.0069	0.0060	3.4186	1.6138
C to Z ↑	0.0170	0.0154	11.8976	5.8227
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0308	0.0245	1.0663	0.7885

A to Z ↑	0.0331	0.0289	4.0287	2.9653
B to Z ↓	0.0086	0.0084	1.1075	0.8266
B to Z ↑	0.0173	0.0175	4.0481	2.9810
C to Z ↓	0.0061	0.0059	1.1089	0.8372
C to Z ↑	0.0158	0.0150	4.0512	2.9839

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	7.654e-06	1.000e-20
X7_P16	1.670e-05	1.000e-20
X11_P16	2.061e-05	1.000e-20
X14_P16	3.096e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	1.320e-03	2.351e-03	3.113e-03	4.404e-03
B (output stable)	2.084e-05	7.744e-05	9.420e-05	1.502e-04
C (output stable)	7.185e-05	2.562e-04	2.969e-04	4.616e-04
A to Z	2.771e-03	5.775e-03	7.885e-03	1.096e-02
B to Z	1.194e-03	2.593e-03	3.617e-03	4.909e-03
C to Z	9.563e-04	1.844e-03	2.728e-03	3.520e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

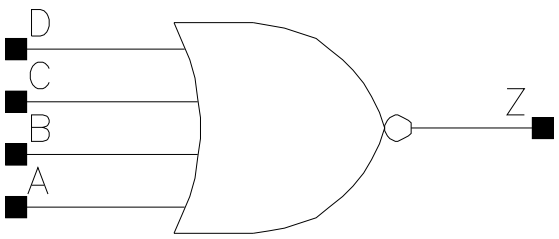
Pin Cycle (vdds)	X3_P16	X7_P16	X11_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	1.224	0.9792
X10_P16	0.800	1.632	1.3056
X14_P16	0.800	1.904	1.5232
X18_P16	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X18_P16
A	0.0006	0.0005	0.0006	0.0007
B	0.0006	0.0007	0.0008	0.0008
C	0.0006	0.0006	0.0006	0.0008
D	0.0006	0.0005	0.0007	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0299	0.0349	3.1852	1.5285
A to Z ↑	0.0462	0.0526	4.7427	2.2917
B to Z ↓	0.0289	0.0348	3.1853	1.5289
B to Z ↑	0.0478	0.0558	4.7423	2.2912
C to Z ↓	0.0304	0.0354	3.1810	1.5253
C to Z ↑	0.0491	0.0569	4.7450	2.2897

D to Z ↓	0.0298	0.0340	3.1786	1.5237
D to Z ↑	0.0514	0.0583	4.7414	2.2889
	X14_P16	**X18_P16**	**X14_P16**	**X18_P16**
A to Z ↓	0.0342	0.0362	1.0547	0.8323
A to Z ↑	0.0492	0.0485	1.5762	1.1851
B to Z ↓	0.0335	0.0347	1.0543	0.8318
B to Z ↑	0.0515	0.0498	1.5755	1.1843
C to Z ↓	0.0333	0.0359	1.0486	0.8294
C to Z ↑	0.0496	0.0493	1.5749	1.1842
D to Z ↓	0.0320	0.0341	1.0492	0.8292
D to Z ↑	0.0512	0.0505	1.5754	1.1841

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.435e-05	1.000e-20
X10_P16	2.144e-05	1.000e-20
X14_P16	3.182e-05	1.000e-20
X18_P16	4.111e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	5.390e-04	6.874e-04	8.845e-04	1.098e-03
B (output stable)	4.902e-04	6.467e-04	8.219e-04	1.005e-03
C (output stable)	5.525e-04	6.383e-04	8.689e-04	1.090e-03
D (output stable)	5.062e-04	5.892e-04	7.976e-04	9.937e-04
A to Z	3.686e-03	5.989e-03	8.515e-03	1.086e-02
B to Z	3.558e-03	5.870e-03	8.336e-03	1.063e-02
C to Z	3.768e-03	5.838e-03	7.979e-03	1.022e-02
D to Z	3.660e-03	5.715e-03	7.809e-03	9.974e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

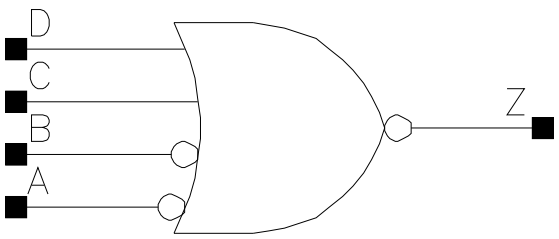
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	1.224	0.9792
X7_P16	0.800	1.496	1.1968
X11_P16	0.800	2.040	1.6320
X14_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P16	X7_P16	X11_P16	X14_P16
A	0.0009	0.0009	0.0016	0.0016
B	0.0009	0.0009	0.0016	0.0016
C	0.0006	0.0013	0.0019	0.0025
D	0.0006	0.0012	0.0018	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X7_P16	X4_P16	X7_P16
A to Z ↓	0.0273	0.0292	2.9834	1.5404
A to Z ↑	0.0349	0.0351	11.3718	5.8787
B to Z ↓	0.0249	0.0268	2.9810	1.5383
B to Z ↑	0.0358	0.0361	11.3786	5.8810
C to Z ↓	0.0088	0.0085	3.0981	1.6129
C to Z ↑	0.0184	0.0181	11.4106	5.9074

D to Z ↓	0.0072	0.0060	3.1219	1.6146
D to Z ↑	0.0179	0.0155	11.4221	5.9101
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0263	0.0290	1.0528	0.7916
A to Z ↑	0.0324	0.0353	3.9783	2.9556
B to Z ↓	0.0236	0.0267	1.0510	0.7900
B to Z ↑	0.0331	0.0366	3.9780	2.9558
C to Z ↓	0.0086	0.0087	1.1068	0.8244
C to Z ↑	0.0172	0.0176	3.9934	2.9668
D to Z ↓	0.0062	0.0060	1.1092	0.8289
D to Z ↑	0.0158	0.0152	3.9974	2.9696

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	1.101e-05	1.000e-20
X7_P16	1.523e-05	1.000e-20
X11_P16	2.461e-05	1.000e-20
X14_P16	2.884e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X7_P16	X11_P16	X14_P16
A (output stable)	1.029e-03	1.233e-03	2.002e-03	2.392e-03
B (output stable)	9.622e-04	1.167e-03	1.837e-03	2.249e-03
C (output stable)	6.711e-05	7.066e-05	1.076e-04	1.573e-04
D (output stable)	1.247e-04	2.516e-04	3.312e-04	5.003e-04
A to Z	4.385e-03	6.166e-03	9.462e-03	1.225e-02
B to Z	4.070e-03	5.847e-03	8.808e-03	1.162e-02
C to Z	1.338e-03	2.553e-03	3.635e-03	4.968e-03
D to Z	1.094e-03	1.833e-03	2.744e-03	3.598e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

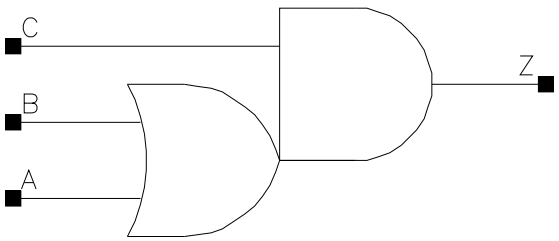
Pin Cycle (vdds)	X4_P16	X7_P16	X11_P16	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.680	0.5440
X10_P16	0.800	0.952	0.7616
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16
A	0.0007	0.0008	0.0014
B	0.0008	0.0008	0.0017
C	0.0009	0.0010	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0253	0.0297	3.0730	1.5403
A to Z ↑	0.0222	0.0269	5.2017	2.2944
B to Z ↓	0.0265	0.0311	3.0738	1.5397
B to Z ↑	0.0200	0.0245	5.1990	2.2892
C to Z ↓	0.0247	0.0273	3.0386	1.5153
C to Z ↑	0.0203	0.0240	5.1985	2.2906
	X19_P16		**X19_P16**	
A to Z ↓	0.0309		0.8009	
A to Z ↑	0.0282		1.1702	

B to Z ↓	0.0323		0.8009	
B to Z ↑	0.0254		1.1675	
C to Z ↓	0.0275		0.7857	
C to Z ↑	0.0244		1.1672	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.135e-05	1.000e-20
X10_P16	1.888e-05	1.000e-20
X19_P16	3.599e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X19_P16
A (output stable)	6.293e-05	6.441e-05	1.364e-04
B (output stable)	7.205e-05	7.604e-05	1.504e-04
C (output stable)	4.142e-05	4.267e-05	8.330e-05
A to Z	2.573e-03	4.493e-03	9.109e-03
B to Z	2.351e-03	4.220e-03	8.572e-03
C to Z	2.838e-03	4.595e-03	9.178e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

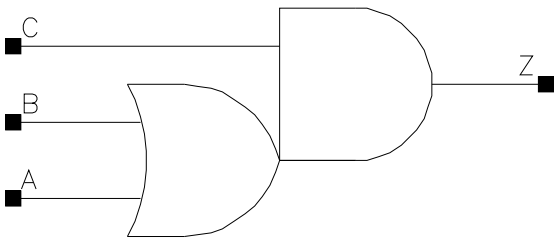
Pin Cycle (vdds)	X5_P16	X10_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X10_P16	0.800	1.360	1.0880
X14_P16	0.800	1.496	1.1968
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0007	0.0016	0.0016	0.0016
B	0.0008	0.0015	0.0015	0.0015
C	0.0008	0.0016	0.0015	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0316	0.0267	3.0176	1.5258
A to Z ↑	0.0222	0.0206	4.5518	2.2338
B to Z ↓	0.0330	0.0276	3.0168	1.5257
B to Z ↑	0.0202	0.0187	4.5414	2.2337
C to Z ↓	0.0221	0.0185	2.9542	1.5012
C to Z ↑	0.0208	0.0191	4.5423	2.2304
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0298	0.0327	1.0615	0.8012

A to Z ↑	0.0228	0.0248	1.5125	1.1356
B to Z ↓	0.0309	0.0340	1.0623	0.8013
B to Z ↑	0.0210	0.0231	1.5120	1.1359
C to Z ↓	0.0209	0.0230	1.0404	0.7819
C to Z ↑	0.0215	0.0236	1.5091	1.1329

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.279e-05	1.000e-20
X10_P16	2.609e-05	1.000e-20
X14_P16	3.127e-05	1.000e-20
X19_P16	3.638e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	1.585e-05	3.337e-05	3.354e-05	3.346e-05
B (output stable)	2.091e-05	4.891e-05	4.903e-05	4.940e-05
C (output stable)	1.833e-04	3.785e-04	3.784e-04	3.800e-04
A to Z	3.262e-03	5.919e-03	7.657e-03	9.474e-03
B to Z	3.016e-03	5.334e-03	7.071e-03	8.892e-03
C to Z	2.660e-03	4.709e-03	6.276e-03	7.875e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

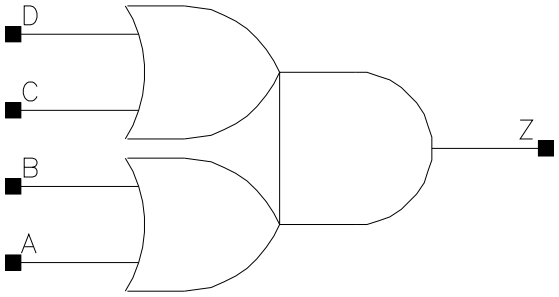
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.952	0.7616
X10_P16	0.800	1.088	0.8704
X14_P16	0.800	1.904	1.5232
X19_P16	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0005	0.0008	0.0015	0.0015
B	0.0005	0.0008	0.0015	0.0015
C	0.0006	0.0008	0.0015	0.0015
D	0.0005	0.0008	0.0015	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0437	0.0364	3.1233	1.5545
A to Z ↑	0.0303	0.0272	4.5662	2.2815
B to Z ↓	0.0454	0.0379	3.1234	1.5547

B to Z ↑	0.0287	0.0254	4.5611	2.2781
C to Z ↓	0.0368	0.0320	3.0907	1.5444
C to Z ↑	0.0299	0.0278	4.5576	2.2793
D to Z ↓	0.0384	0.0331	3.0894	1.5448
D to Z ↑	0.0279	0.0255	4.5553	2.2757
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0349	0.0371	1.0785	0.8087
A to Z ↑	0.0258	0.0271	1.5181	1.1401
B to Z ↓	0.0350	0.0373	1.0786	0.8090
B to Z ↑	0.0234	0.0247	1.5145	1.1383
C to Z ↓	0.0293	0.0317	1.0708	0.8033
C to Z ↑	0.0257	0.0272	1.5148	1.1392
D to Z ↓	0.0291	0.0316	1.0715	0.8033
D to Z ↑	0.0229	0.0245	1.5117	1.1361

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	9.758e-06	1.000e-20
X10_P16	2.005e-05	1.000e-20
X14_P16	3.382e-05	1.000e-20
X19_P16	3.839e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	1.575e-05	2.415e-05	7.211e-05	7.205e-05
B (output stable)	2.085e-05	3.589e-05	1.589e-04	1.589e-04
C (output stable)	6.375e-05	7.197e-05	1.676e-04	1.672e-04
D (output stable)	7.093e-05	8.475e-05	2.494e-04	2.495e-04
A to Z	3.320e-03	5.400e-03	8.961e-03	1.054e-02
B to Z	3.169e-03	5.103e-03	8.169e-03	9.732e-03
C to Z	2.870e-03	4.810e-03	7.745e-03	9.298e-03
D to Z	2.727e-03	4.533e-03	6.970e-03	8.505e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

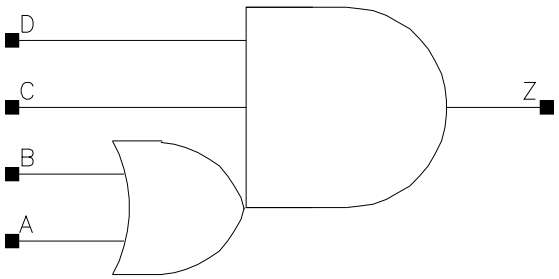
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	0.816	0.6528
X10_P16	0.800	1.088	0.8704
X14_P16	0.800	1.904	1.5232
X19_P16	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P16	X10_P16	X14_P16	X19_P16
A	0.0005	0.0011	0.0013	0.0015
B	0.0006	0.0008	0.0013	0.0016
C	0.0006	0.0008	0.0013	0.0015
D	0.0006	0.0008	0.0013	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X10_P16	X4_P16	X10_P16
A to Z ↓	0.0365	0.0360	3.3780	1.5786
A to Z ↑	0.0342	0.0368	4.8338	2.3223
B to Z ↓	0.0385	0.0351	3.3755	1.5765
B to Z ↑	0.0325	0.0322	4.8323	2.3178
C to Z ↓	0.0325	0.0299	3.2924	1.5459

C to Z ↑	0.0313	0.0316	4.8274	2.3170
D to Z ↓	0.0317	0.0287	3.2920	1.5440
D to Z ↑	0.0332	0.0330	4.8274	2.3178
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0354	0.0341	1.0766	0.8002
A to Z ↑	0.0354	0.0366	1.5460	1.1597
B to Z ↓	0.0352	0.0340	1.0763	0.8005
B to Z ↑	0.0319	0.0330	1.5420	1.1550
C to Z ↓	0.0311	0.0301	1.0553	0.7860
C to Z ↑	0.0317	0.0324	1.5425	1.1561
D to Z ↓	0.0293	0.0284	1.0523	0.7840
D to Z ↑	0.0322	0.0329	1.5423	1.1563

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	8.636e-06	1.000e-20
X10_P16	1.820e-05	1.000e-20
X14_P16	2.740e-05	1.000e-20
X19_P16	3.605e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X10_P16	X14_P16	X19_P16
A (output stable)	8.858e-05	1.326e-04	2.131e-04	2.350e-04
B (output stable)	8.510e-05	1.380e-04	2.306e-04	2.579e-04
C (output stable)	1.400e-05	2.618e-05	6.593e-05	7.423e-05
D (output stable)	3.354e-05	5.650e-05	2.039e-04	2.208e-04
A to Z	2.798e-03	5.248e-03	8.049e-03	1.021e-02
B to Z	2.666e-03	4.776e-03	7.370e-03	9.354e-03
C to Z	3.017e-03	5.337e-03	8.509e-03	1.064e-02
D to Z	2.886e-03	5.117e-03	7.948e-03	1.000e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

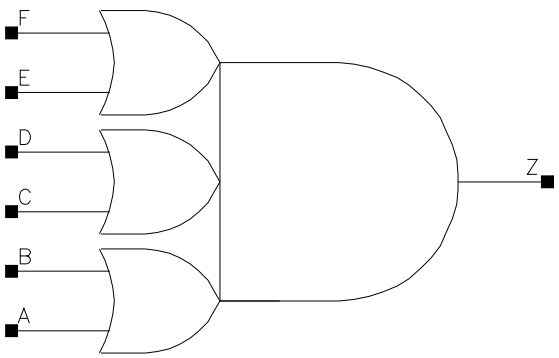
Pin Cycle (vdds)	X4_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	1.360	1.0880
X9_P16	0.800	1.496	1.1968
X19_P16	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P16	X9_P16	X19_P16
A	0.0006	0.0008	0.0013
B	0.0007	0.0010	0.0015
C	0.0005	0.0007	0.0013
D	0.0005	0.0007	0.0015
E	0.0006	0.0007	0.0013
F	0.0006	0.0008	0.0016

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X9_P16	X4_P16	X9_P16
A to Z ↓	0.0516	0.0443	3.4512	1.7026
A to Z ↑	0.0391	0.0383	4.9452	2.4362
B to Z ↓	0.0546	0.0468	3.4523	1.7027
B to Z ↑	0.0384	0.0367	4.9497	2.4342
C to Z ↓	0.0471	0.0401	3.4249	1.6905
C to Z ↑	0.0396	0.0377	4.9501	2.4358
D to Z ↓	0.0487	0.0415	3.4246	1.6907
D to Z ↑	0.0374	0.0353	4.9431	2.4326
E to Z ↓	0.0400	0.0351	3.3856	1.6778
E to Z ↑	0.0370	0.0364	4.9412	2.4326
F to Z ↓	0.0421	0.0369	3.3867	1.6790
F to Z ↑	0.0354	0.0345	4.9357	2.4292
	X19_P16		X19_P16	
A to Z ↓	0.0437		0.8188	
A to Z ↑	0.0372		1.1596	
B to Z ↓	0.0455		0.8185	
B to Z ↑	0.0343		1.1557	
C to Z ↓	0.0399		0.8123	
C to Z ↑	0.0371		1.1587	
D to Z ↓	0.0416		0.8128	
D to Z ↑	0.0346		1.1555	
E to Z ↓	0.0349		0.8066	
E to Z ↑	0.0361		1.1570	
F to Z ↓	0.0366		0.8071	
F to Z ↑	0.0334		1.1537	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	1.033e-05	1.000e-20
X9_P16	2.069e-05	1.000e-20
X19_P16	4.137e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X9_P16	X19_P16
A (output stable)	1.501e-05	2.422e-05	4.452e-05
B (output stable)	2.253e-05	3.445e-05	5.995e-05
C (output stable)	3.728e-05	4.960e-05	9.517e-05
D (output stable)	4.273e-05	5.713e-05	1.121e-04
E (output stable)	1.262e-04	1.560e-04	2.950e-04
F (output stable)	1.246e-04	1.634e-04	3.055e-04
A to Z	3.943e-03	6.448e-03	1.280e-02
B to Z	3.822e-03	6.198e-03	1.221e-02
C to Z	3.567e-03	5.888e-03	1.174e-02
D to Z	3.409e-03	5.594e-03	1.116e-02
E to Z	3.087e-03	5.279e-03	1.055e-02
F to Z	2.960e-03	5.027e-03	1.002e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

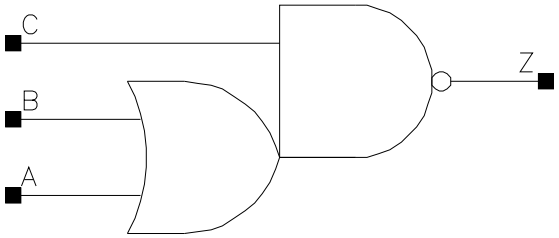
Pin Cycle (vdds)	X4_P16	X9_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.544	0.4352
X10_P16	0.800	1.360	1.0880
X20_P16	0.800	2.720	2.1760
X26_P16	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P16	X10_P16	X20_P16	X26_P16
A	0.0006	0.0019	0.0037	0.0050
B	0.0006	0.0017	0.0034	0.0046
C	0.0006	0.0020	0.0040	0.0054

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X10_P16**	**X3_P16**	**X10_P16**
A to Z ↓	0.0109	0.0122	5.7760	1.8213
A to Z ↑	0.0138	0.0139	9.8057	2.7480
B to Z ↓	0.0085	0.0093	5.6801	1.8328
B to Z ↑	0.0143	0.0132	9.8468	2.7656
C to Z ↓	0.0095	0.0101	5.2343	1.6661
C to Z ↑	0.0149	0.0139	5.6344	1.5886
	X20_P16	**X26_P16**	**X20_P16**	**X26_P16**
A to Z ↓	0.0127	0.0128	0.9305	0.7041

A to Z ↑	0.0144	0.0144	1.4077	1.0587
B to Z ↓	0.0097	0.0098	0.9411	0.7150
B to Z ↑	0.0138	0.0138	1.4152	1.0649
C to Z ↓	0.0106	0.0106	0.8541	0.6472
C to Z ↑	0.0142	0.0141	0.7814	0.5870

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	6.008e-06	1.000e-20
X10_P16	2.081e-05	1.000e-20
X20_P16	4.131e-05	1.000e-20
X26_P16	5.449e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X10_P16	X20_P16	X26_P16
A (output stable)	5.480e-05	2.042e-04	4.252e-04	5.461e-04
B (output stable)	6.506e-05	2.554e-04	5.408e-04	6.868e-04
C (output stable)	3.750e-05	1.308e-04	2.751e-04	3.586e-04
A to Z	1.005e-03	3.737e-03	7.665e-03	1.018e-02
B to Z	8.008e-04	2.716e-03	5.722e-03	7.612e-03
C to Z	1.272e-03	4.408e-03	9.118e-03	1.206e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

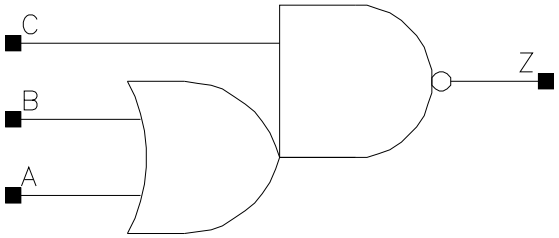
Pin Cycle (vdds)	X3_P16	X10_P16	X20_P16	X26_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X7_P16	0.800	0.952	0.7616
X10_P16	0.800	1.360	1.0880
X13_P16	0.800	1.904	1.5232
X26_P16	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P16	X7_P16	X10_P16	X13_P16
A	0.0007	0.0013	0.0021	0.0027
B	0.0007	0.0013	0.0019	0.0024
C	0.0009	0.0012	0.0018	0.0025
	X26_P16			
A	0.0054			
B	0.0048			
C	0.0049			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X7_P16	X3_P16	X7_P16
A to Z ↓	0.0126	0.0113	5.0691	2.6286
A to Z ↑	0.0191	0.0170	7.9090	4.0668
B to Z ↓	0.0105	0.0089	5.0931	2.5632

B to Z ↑	0.0199	0.0176	7.9402	4.0830
C to Z ↓	0.0109	0.0094	4.8300	2.4523
C to Z ↑	0.0120	0.0103	4.6953	2.4410
	X10_P16	**X13_P16**	**X10_P16**	**X13_P16**
A to Z ↓	0.0110	0.0117	1.7759	1.3578
A to Z ↑	0.0165	0.0179	2.6847	2.0628
B to Z ↓	0.0087	0.0089	1.7713	1.3625
B to Z ↑	0.0170	0.0172	2.6964	2.0719
C to Z ↓	0.0092	0.0093	1.6808	1.2820
C to Z ↑	0.0097	0.0097	1.6088	1.2169
	X26_P16		**X26_P16**	
A to Z ↓	0.0116		0.6999	
A to Z ↑	0.0176		1.0406	
B to Z ↓	0.0087		0.6990	
B to Z ↑	0.0168		1.0452	
C to Z ↓	0.0096		0.6592	
C to Z ↑	0.0096		0.6131	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	8.018e-06	1.000e-20
X7_P16	1.466e-05	1.000e-20
X10_P16	2.153e-05	1.000e-20
X13_P16	2.892e-05	1.000e-20
X26_P16	5.602e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X7_P16	X10_P16	X13_P16
A (output stable)	1.847e-05	3.370e-05	4.967e-05	9.176e-05
B (output stable)	2.428e-05	4.708e-05	6.971e-05	1.670e-04
C (output stable)	1.924e-04	3.759e-04	4.907e-04	7.305e-04
A to Z	1.822e-03	3.044e-03	4.439e-03	6.350e-03
B to Z	1.530e-03	2.503e-03	3.594e-03	4.833e-03
C to Z	1.224e-03	2.108e-03	3.023e-03	4.186e-03
	X26_P16			
A (output stable)	1.779e-04			
B (output stable)	3.088e-04			
C (output stable)	1.328e-03			
A to Z	1.234e-02			
B to Z	9.318e-03			
C to Z	8.103e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P16	X7_P16	X10_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

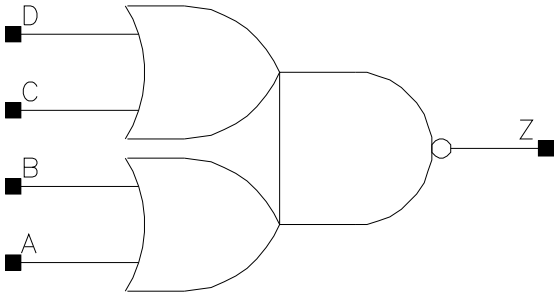
	X26_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X6_P16	0.800	1.360	1.0880
X8_P16	0.800	1.768	1.4144
X11_P16	0.800	2.448	1.9584
X24_P16	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X8_P16	X11_P16
A	0.0007	0.0013	0.0020	0.0026
B	0.0006	0.0012	0.0018	0.0023
C	0.0006	0.0013	0.0018	0.0024
D	0.0006	0.0011	0.0017	0.0022
	X24_P16			
A	0.0055			
B	0.0049			
C	0.0051			
D	0.0047			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X6_P16**	**X3_P16**	**X6_P16**
A to Z ↓	0.0118	0.0142	4.7524	2.5794
A to Z ↑	0.0215	0.0213	9.6949	4.2834
B to Z ↓	0.0102	0.0116	4.7206	2.5914
B to Z ↑	0.0225	0.0206	9.7161	4.2990
C to Z ↓	0.0105	0.0130	4.8707	2.6112
C to Z ↑	0.0144	0.0152	9.7392	4.3129
D to Z ↓	0.0085	0.0099	4.8358	2.6422
D to Z ↑	0.0150	0.0138	9.7730	4.3353
	X8_P16	**X11_P16**	**X8_P16**	**X11_P16**
A to Z ↓	0.0135	0.0138	1.7612	1.3352
A to Z ↑	0.0200	0.0202	2.8713	2.1539
B to Z ↓	0.0112	0.0112	1.7742	1.3402
B to Z ↑	0.0198	0.0198	2.8846	2.1631
C to Z ↓	0.0128	0.0131	1.7947	1.3592
C to Z ↑	0.0142	0.0146	2.8706	2.1722
D to Z ↓	0.0102	0.0101	1.8178	1.3675
D to Z ↑	0.0136	0.0136	2.8904	2.1868
	X24_P16		**X24_P16**	
A to Z ↓	0.0138		0.6555	
A to Z ↑	0.0201		1.0414	
B to Z ↓	0.0112		0.6522	
B to Z ↑	0.0200		1.0460	
C to Z ↓	0.0135		0.6675	
C to Z ↑	0.0145		1.0447	
D to Z ↓	0.0103		0.6665	
D to Z ↑	0.0137		1.0516	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	7.919e-06	1.000e-20
X6_P16	1.747e-05	1.000e-20
X8_P16	2.515e-05	1.000e-20
X11_P16	3.387e-05	1.000e-20
X24_P16	6.904e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X6_P16	X8_P16	X11_P16
A (output stable)	2.144e-05	7.417e-05	9.240e-05	1.345e-04
B (output stable)	3.111e-05	1.602e-04	1.838e-04	2.818e-04
C (output stable)	6.862e-05	1.704e-04	2.175e-04	2.986e-04
D (output stable)	8.244e-05	2.543e-04	3.095e-04	4.430e-04
A to Z	1.715e-03	3.948e-03	5.518e-03	7.459e-03
B to Z	1.476e-03	3.169e-03	4.442e-03	5.980e-03
C to Z	1.136e-03	2.856e-03	4.001e-03	5.501e-03
D to Z	9.330e-04	2.120e-03	3.030e-03	4.126e-03
	X24_P16			
A (output stable)	2.640e-04			
B (output stable)	5.414e-04			
C (output stable)	5.742e-04			
D (output stable)	8.423e-04			

A to Z	1.536e-02			
B to Z	1.237e-02			
C to Z	1.134e-02			
D to Z	8.572e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

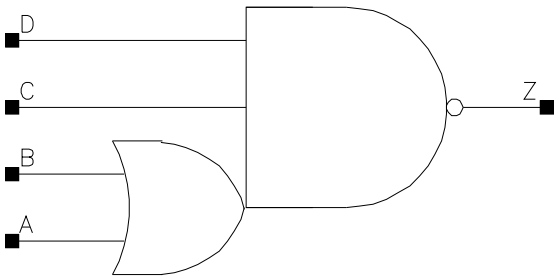
Pin Cycle (vdds)	X3_P16	X6_P16	X8_P16	X11_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.816	0.6528
X6_P16	0.800	1.360	1.0880
X12_P16	0.800	2.448	1.9584
X18_P16	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X12_P16	X18_P16
A	0.0009	0.0012	0.0024	0.0036
B	0.0006	0.0011	0.0022	0.0034
C	0.0007	0.0013	0.0026	0.0040
D	0.0007	0.0013	0.0025	0.0037

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0192	0.0167	6.9863	3.7606
A to Z ↑	0.0199	0.0163	8.2222	4.1333
B to Z ↓	0.0142	0.0129	7.0326	3.7818
B to Z ↑	0.0178	0.0153	8.2333	4.1541
C to Z ↓	0.0151	0.0151	6.5668	3.5412

C to Z ↑	0.0176	0.0170	4.5349	2.3308
D to Z ↓	0.0164	0.0151	6.6017	3.5573
D to Z ↑	0.0168	0.0153	4.6564	2.3371
	X12_P16	**X18_P16**	**X12_P16**	**X18_P16**
A to Z ↓	0.0170	0.0172	1.9540	1.3205
A to Z ↑	0.0161	0.0160	2.0702	1.3875
B to Z ↓	0.0131	0.0134	1.9671	1.3311
B to Z ↑	0.0150	0.0152	2.0832	1.3963
C to Z ↓	0.0150	0.0151	1.8406	1.2447
C to Z ↑	0.0167	0.0165	1.1866	0.7814
D to Z ↓	0.0152	0.0153	1.8492	1.2503
D to Z ↑	0.0150	0.0150	1.1838	0.7903

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	6.632e-06	1.000e-20
X6_P16	1.260e-05	1.000e-20
X12_P16	2.406e-05	1.000e-20
X18_P16	3.555e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X6_P16	X12_P16	X18_P16
A (output stable)	1.304e-04	2.657e-04	5.005e-04	7.075e-04
B (output stable)	1.359e-04	2.864e-04	5.280e-04	7.509e-04
C (output stable)	2.325e-05	7.140e-05	1.332e-04	2.107e-04
D (output stable)	5.422e-05	2.074e-04	3.685e-04	5.793e-04
A to Z	1.778e-03	2.931e-03	5.764e-03	8.601e-03
B to Z	1.339e-03	2.202e-03	4.267e-03	6.417e-03
C to Z	2.139e-03	3.994e-03	7.652e-03	1.146e-02
D to Z	1.932e-03	3.362e-03	6.474e-03	9.633e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

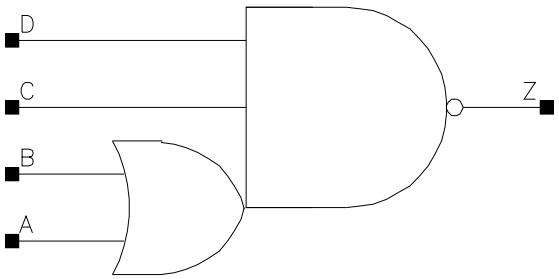
Pin Cycle (vdds)	X3_P16	X6_P16	X12_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	0.800	0.680	0.5440
X6_P16	0.800	1.360	1.0880
X9_P16	0.800	1.768	1.4144
X12_P16	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X9_P16	X12_P16
A	0.0007	0.0014	0.0021	0.0027
B	0.0006	0.0012	0.0018	0.0027
C	0.0006	0.0013	0.0019	0.0025
D	0.0006	0.0012	0.0018	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0156	0.0161	7.4921	3.7089
A to Z ↑	0.0204	0.0218	8.2889	4.1218
B to Z ↓	0.0131	0.0130	7.3652	3.7327
B to Z ↑	0.0213	0.0214	8.3157	4.1369
C to Z ↓	0.0124	0.0132	7.0856	3.5482

C to Z ↑	0.0134	0.0138	4.8877	2.4134
D to Z ↓	0.0132	0.0131	7.1332	3.5689
D to Z ↑	0.0115	0.0111	4.9409	2.4346
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0164	0.0164	2.5484	1.9370
A to Z ↑	0.0211	0.0216	2.7181	2.1178
B to Z ↓	0.0134	0.0132	2.5518	1.9444
B to Z ↑	0.0210	0.0217	2.7295	2.1274
C to Z ↓	0.0132	0.0133	2.4303	1.8482
C to Z ↑	0.0133	0.0135	1.5942	1.2085
D to Z ↓	0.0134	0.0132	2.4447	1.8598
D to Z ↑	0.0109	0.0107	1.6086	1.2223

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P16	6.249e-06	1.000e-20
X6_P16	1.319e-05	1.000e-20
X9_P16	1.873e-05	1.000e-20
X12_P16	2.518e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	1.375e-05	3.173e-05	4.882e-05	6.265e-05
B (output stable)	1.550e-05	4.882e-05	6.901e-05	9.371e-05
C (output stable)	5.137e-05	1.146e-04	1.828e-04	2.303e-04
D (output stable)	1.064e-04	3.859e-04	4.398e-04	7.102e-04
A to Z	1.893e-03	4.111e-03	6.026e-03	8.035e-03
B to Z	1.603e-03	3.303e-03	4.822e-03	6.431e-03
C to Z	1.321e-03	2.899e-03	4.158e-03	5.634e-03
D to Z	1.125e-03	2.357e-03	3.446e-03	4.549e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

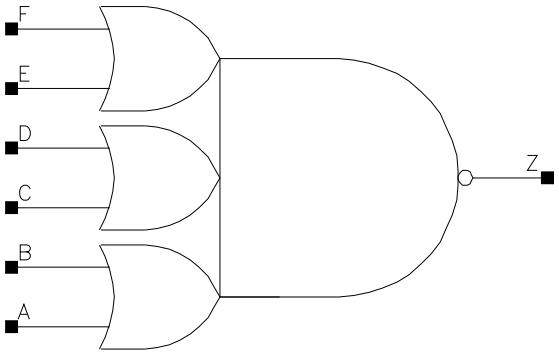
Pin Cycle (vdds)	X3_P16	X6_P16	X9_P16	X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.224	0.9792
X3_P16	0.800	1.224	0.9792
X5_P16	0.800	2.040	1.6320
X8_P16	0.800	2.720	2.1760
X10_P16	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P16	X3_P16	X5_P16	X8_P16
A	0.0006	0.0007	0.0014	0.0021
B	0.0005	0.0007	0.0012	0.0019
C	0.0005	0.0007	0.0013	0.0019
D	0.0006	0.0006	0.0012	0.0018

E	0.0005	0.0007	0.0012	0.0018
F	0.0005	0.0006	0.0011	0.0017
	X10_P16			
A	0.0027			
B	0.0025			
C	0.0025			
D	0.0023			
E	0.0024			
F	0.0023			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X3_P16**	**X2_P16**	**X3_P16**
A to Z ↓	0.0206	0.0199	8.1069	6.3842
A to Z ↑	0.0297	0.0260	11.1418	7.8317
B to Z ↓	0.0188	0.0180	8.1390	6.4296
B to Z ↑	0.0313	0.0276	11.1643	7.8526
C to Z ↓	0.0201	0.0199	8.1521	6.4047
C to Z ↑	0.0254	0.0228	11.1550	7.9644
D to Z ↓	0.0187	0.0174	8.2440	6.4961
D to Z ↑	0.0276	0.0238	11.2016	7.9850
E to Z ↓	0.0179	0.0178	8.2301	6.4558
E to Z ↑	0.0193	0.0174	11.1831	7.9902
F to Z ↓	0.0162	0.0156	8.3150	6.5559
F to Z ↑	0.0206	0.0181	11.2367	8.0269
	X5_P16	**X8_P16**	**X5_P16**	**X8_P16**
A to Z ↓	0.0214	0.0210	3.4145	2.3210
A to Z ↑	0.0272	0.0262	4.1198	2.7244
B to Z ↓	0.0184	0.0181	3.4374	2.3271
B to Z ↑	0.0268	0.0266	4.1314	2.7331
C to Z ↓	0.0197	0.0203	3.4360	2.3346
C to Z ↑	0.0225	0.0222	4.1653	2.7906
D to Z ↓	0.0167	0.0172	3.4514	2.3438
D to Z ↑	0.0224	0.0229	4.1813	2.8011
E to Z ↓	0.0189	0.0188	3.4757	2.3540
E to Z ↑	0.0176	0.0170	4.1743	2.8034
F to Z ↓	0.0156	0.0156	3.4957	2.3606
F to Z ↑	0.0167	0.0170	4.1968	2.8202
	X10_P16		**X10_P16**	
A to Z ↓	0.0215		1.7642	
A to Z ↑	0.0266		2.0706	
B to Z ↓	0.0185		1.7709	
B to Z ↑	0.0267		2.0778	
C to Z ↓	0.0201		1.7731	
C to Z ↑	0.0224		2.1123	
D to Z ↓	0.0171		1.7804	
D to Z ↑	0.0225		2.1211	
E to Z ↓	0.0191		1.7888	
E to Z ↑	0.0173		2.1099	
F to Z ↓	0.0161		1.8015	
F to Z ↑	0.0170		2.1229	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P16	7.701e-06	1.000e-20
X3_P16	1.128e-05	1.000e-20
X5_P16	2.167e-05	1.000e-20
X8_P16	3.118e-05	1.000e-20
X10_P16	4.155e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P16	X3_P16	X5_P16	X8_P16
A (output stable)	1.906e-05	2.401e-05	6.827e-05	9.039e-05
B (output stable)	2.457e-05	3.233e-05	1.237e-04	1.522e-04
C (output stable)	4.275e-05	5.104e-05	1.285e-04	1.735e-04
D (output stable)	4.892e-05	5.793e-05	1.825e-04	2.229e-04
E (output stable)	1.389e-04	1.697e-04	2.981e-04	4.553e-04
F (output stable)	1.464e-04	1.813e-04	3.534e-04	5.085e-04
A to Z	2.326e-03	2.847e-03	5.748e-03	8.309e-03
B to Z	2.119e-03	2.562e-03	4.907e-03	7.147e-03
C to Z	1.898e-03	2.353e-03	4.551e-03	6.695e-03
D to Z	1.716e-03	2.066e-03	3.846e-03	5.738e-03
E to Z	1.437e-03	1.801e-03	3.630e-03	5.189e-03
F to Z	1.261e-03	1.547e-03	2.929e-03	4.297e-03
	X10_P16			
A (output stable)	1.308e-04			
B (output stable)	2.287e-04			
C (output stable)	2.437e-04			
D (output stable)	3.381e-04			
E (output stable)	5.778e-04			
F (output stable)	6.734e-04			
A to Z	1.122e-02			
B to Z	9.589e-03			
C to Z	8.962e-03			
D to Z	7.579e-03			
E to Z	7.078e-03			
F to Z	5.787e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X2_P16	X3_P16	X5_P16	X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P16			

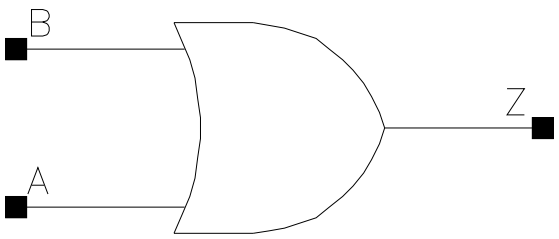
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.544	0.4352
X9_P16	0.800	0.680	0.5440
X19_P16	0.800	1.360	1.0880
X29_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P16	X9_P16	X19_P16	X29_P16
A	0.0006	0.0008	0.0014	0.0014
B	0.0005	0.0007	0.0015	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X9_P16**	**X5_P16**	**X9_P16**
A to Z ↓	0.0324	0.0294	3.2544	1.6407
A to Z ↑	0.0208	0.0226	4.6989	2.3726
B to Z ↓	0.0337	0.0302	3.2548	1.6409
B to Z ↑	0.0197	0.0209	4.7034	2.3733
	X19_P16	**X29_P16**	**X19_P16**	**X29_P16**
A to Z ↓	0.0301	0.0361	0.7884	0.5404
A to Z ↑	0.0226	0.0262	1.1288	0.7577
B to Z ↓	0.0296	0.0360	0.7889	0.5399
B to Z ↑	0.0203	0.0240	1.1278	0.7574

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	7.617e-06	1.000e-20
X9_P16	1.422e-05	1.000e-20
X19_P16	2.920e-05	1.000e-20
X29_P16	3.722e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X9_P16	X19_P16	X29_P16
A (output stable)	1.379e-05	2.463e-05	9.240e-05	9.259e-05
B (output stable)	2.707e-05	4.571e-05	2.427e-04	2.430e-04
A to Z	2.406e-03	4.030e-03	8.533e-03	1.242e-02
B to Z	2.270e-03	3.787e-03	7.722e-03	1.161e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

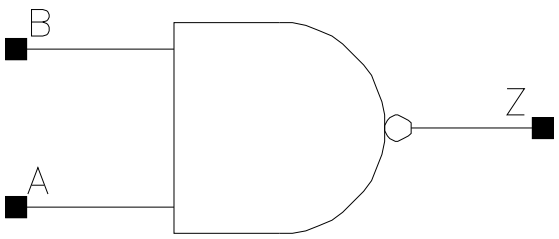
Pin Cycle (vdds)	X5_P16	X9_P16	X19_P16	X29_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.816	0.6528
X9_P16	0.800	0.952	0.7616
X14_P16	0.800	1.088	0.8704
X18_P16	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P16	X9_P16	X14_P16	X18_P16
A	0.0009	0.0008	0.0008	0.0007
B	0.0008	0.0009	0.0009	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X9_P16**	**X5_P16**	**X9_P16**
A to Z ↓	0.0270	0.0314	2.9478	1.6059
A to Z ↑	0.0300	0.0330	4.5288	2.3796
B to Z ↓	0.0284	0.0333	2.9489	1.6060
B to Z ↑	0.0278	0.0314	4.5288	2.3804
	X14_P16	**X18_P16**	**X14_P16**	**X18_P16**
A to Z ↓	0.0353	0.0378	1.1117	0.8404
A to Z ↑	0.0357	0.0371	1.5750	1.2182
B to Z ↓	0.0372	0.0396	1.1113	0.8405
B to Z ↑	0.0341	0.0354	1.5758	1.2176

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.733e-05	1.000e-20
X9_P16	2.064e-05	1.000e-20
X14_P16	2.467e-05	1.000e-20
X18_P16	2.707e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X9_P16	X14_P16	X18_P16
A (output stable)	1.418e-05	1.388e-05	1.399e-05	1.400e-05
B (output stable)	3.435e-05	3.130e-05	3.148e-05	3.005e-05
A to Z	4.259e-03	5.548e-03	7.271e-03	8.423e-03
B to Z	4.060e-03	5.361e-03	7.085e-03	8.243e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

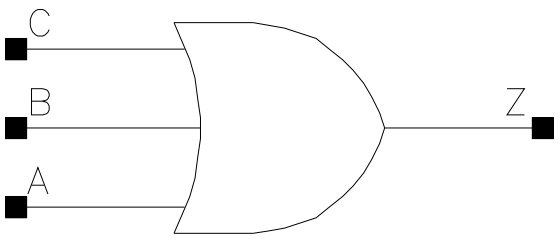
Pin Cycle (vdds)	X5_P16	X9_P16	X14_P16	X18_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.680	0.5440
X10_P16	0.800	0.952	0.7616
X14_P16	0.800	1.496	1.1968
X19_P16	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0006	0.0009	0.0014	0.0022
B	0.0005	0.0008	0.0016	0.0022
C	0.0006	0.0008	0.0015	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0425	0.0392	3.3660	1.6047
A to Z ↑	0.0242	0.0220	4.7226	2.2502
B to Z ↓	0.0422	0.0388	3.3673	1.6061
B to Z ↑	0.0236	0.0209	4.7209	2.2494
C to Z ↓	0.0427	0.0387	3.3665	1.6050
C to Z ↑	0.0223	0.0193	4.7225	2.2486
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**
A to Z ↓	0.0365	0.0354	1.0759	0.8224

A to Z ↑	0.0202	0.0200	1.5356	1.1763
B to Z ↓	0.0369	0.0345	1.0776	0.8233
B to Z ↑	0.0190	0.0192	1.5326	1.1723
C to Z ↓	0.0338	0.0333	1.0757	0.8231
C to Z ↑	0.0169	0.0171	1.5310	1.1716

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	7.050e-06	1.000e-20
X10_P16	1.394e-05	1.000e-20
X14_P16	2.367e-05	1.000e-20
X19_P16	3.258e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	1.770e-05	3.158e-05	6.575e-05	1.194e-04
B (output stable)	6.667e-06	1.876e-05	5.051e-05	6.494e-05
C (output stable)	3.442e-05	7.094e-05	2.234e-04	2.496e-04
A to Z	2.868e-03	4.912e-03	7.898e-03	1.119e-02
B to Z	2.703e-03	4.634e-03	7.405e-03	1.015e-02
C to Z	2.559e-03	4.368e-03	6.576e-03	9.208e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

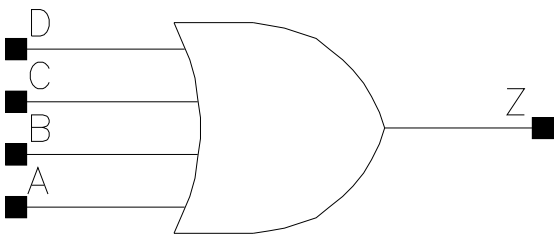
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	0.800	1.224	0.9792
X8_P16	0.800	1.496	1.1968
X12_P16	0.800	2.176	1.7408
X15_P16	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X12_P16	X15_P16
A	0.0005	0.0008	0.0014	0.0015
B	0.0006	0.0008	0.0012	0.0015
C	0.0005	0.0008	0.0013	0.0016
D	0.0006	0.0009	0.0012	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
A to Z ↓	0.0339	0.0328	4.9006	2.5962
A to Z ↑	0.0219	0.0228	4.4272	2.3509
B to Z ↓	0.0358	0.0343	4.9004	2.5955
B to Z ↑	0.0208	0.0215	4.4231	2.3470
C to Z ↓	0.0361	0.0323	4.9087	2.5895
C to Z ↑	0.0223	0.0220	4.5242	2.3569

D to Z ↓	0.0384	0.0340	4.9077	2.5896
D to Z ↑	0.0214	0.0208	4.5208	2.3568
	X12_P16	**X15_P16**	**X12_P16**	**X15_P16**
A to Z ↓	0.0331	0.0335	1.7913	1.3434
A to Z ↑	0.0231	0.0221	1.5080	1.1548
B to Z ↓	0.0335	0.0333	1.7913	1.3432
B to Z ↑	0.0216	0.0201	1.5069	1.1526
C to Z ↓	0.0325	0.0326	1.7886	1.3411
C to Z ↑	0.0219	0.0210	1.5027	1.1614
D to Z ↓	0.0329	0.0326	1.7883	1.3407
D to Z ↑	0.0204	0.0191	1.5017	1.1589

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	9.416e-06	1.000e-20
X8_P16	1.901e-05	1.000e-20
X12_P16	2.504e-05	1.000e-20
X15_P16	3.594e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	6.331e-04	1.128e-03	1.732e-03	2.327e-03
B (output stable)	5.856e-04	1.033e-03	1.558e-03	2.079e-03
C (output stable)	5.935e-04	1.039e-03	1.540e-03	2.090e-03
D (output stable)	5.465e-04	9.446e-04	1.366e-03	1.865e-03
A to Z	2.649e-03	5.203e-03	7.472e-03	9.925e-03
B to Z	2.527e-03	4.962e-03	6.972e-03	9.139e-03
C to Z	2.623e-03	4.612e-03	6.653e-03	8.604e-03
D to Z	2.508e-03	4.377e-03	6.161e-03	7.900e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

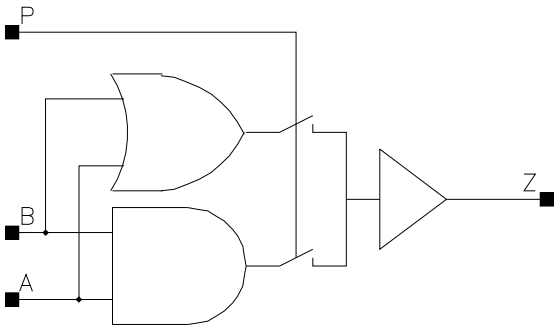
Pin Cycle (vdds)	X4_P16	X8_P16	X12_P16	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	0.800	0.952	0.7616
X10_P16	1.600	0.816	1.3056
X14_P16	1.600	1.224	1.9584
X19_P16	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P16	X10_P16	X14_P16	X19_P16
A	0.0011	0.0014	0.0027	0.0027
B	0.0011	0.0015	0.0028	0.0028
P	0.0006	0.0008	0.0015	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0405	0.0375	3.3059	1.5442
A to Z ↑	0.0231	0.0278	4.7404	2.2734
B to Z ↓	0.0407	0.0386	3.3171	1.5513
B to Z ↑	0.0243	0.0295	4.7462	2.2752
P to Z ↓	0.0378	0.0371	3.3125	1.5513
P to Z ↑	0.0237	0.0292	4.7414	2.2728
	X14_P16	**X19_P16**	**X14_P16**	**X19_P16**

A to Z ↓	0.0346	0.0374	1.0632	0.7982
A to Z ↑	0.0269	0.0283	1.5534	1.1614
B to Z ↓	0.0335	0.0363	1.0746	0.8044
B to Z ↑	0.0271	0.0287	1.5564	1.1627
P to Z ↓	0.0330	0.0361	1.0750	0.8039
P to Z ↑	0.0273	0.0291	1.5543	1.1618

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.041e-05	1.000e-20
X10_P16	2.194e-05	1.000e-20
X14_P16	3.644e-05	1.000e-20
X19_P16	4.151e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	3.364e-05	4.976e-05	1.441e-04	1.386e-04
B (output stable)	4.809e-05	7.860e-05	3.471e-04	3.359e-04
P (output stable)	1.501e-04	2.517e-04	4.677e-04	4.405e-04
A to Z	2.891e-03	5.574e-03	8.893e-03	1.075e-02
B to Z	2.800e-03	5.502e-03	8.415e-03	1.027e-02
P to Z	2.577e-03	5.209e-03	8.241e-03	1.016e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

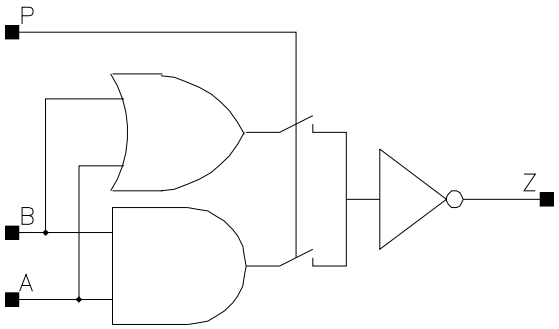
Pin Cycle (vdds)	X5_P16	X10_P16	X14_P16	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.600	0.544	0.8704
X10_P16	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P16	X10_P16
A	0.0013	0.0025
B	0.0012	0.0023
P	0.0008	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0135	0.0127	4.9456	2.5833
A to Z ↑	0.0211	0.0198	7.9388	4.0273
B to Z ↓	0.0144	0.0125	4.9092	2.5974
B to Z ↑	0.0212	0.0181	7.9365	4.0897
P to Z ↓	0.0147	0.0124	5.0246	2.6161
P to Z ↑	0.0205	0.0169	8.0130	4.0562

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	1.063e-05	1.000e-20
X10_P16	2.005e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P16	X10_P16
A (output stable)	4.751e-05	1.441e-04
B (output stable)	7.175e-05	3.378e-04
P (output stable)	2.126e-04	5.022e-04
A to Z	2.032e-03	3.667e-03
B to Z	1.882e-03	3.090e-03
P to Z	1.625e-03	2.784e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

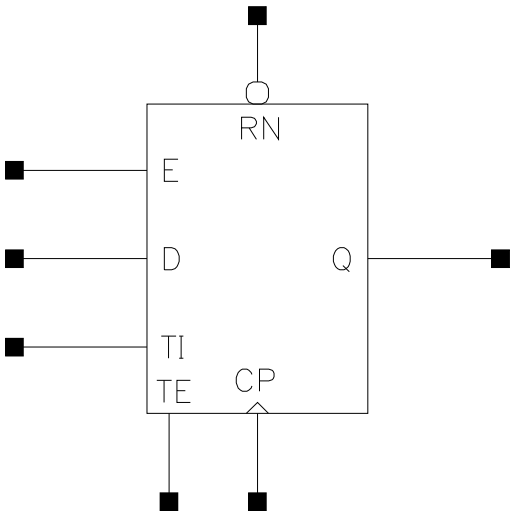
Pin Cycle (vdds)	X5_P16	X10_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.600	2.992	4.7872
X10_P16	1.600	3.128	5.0048
X19_P16	1.600	3.264	5.2224
X23_P16	1.600	3.264	5.2224
X29_P16	1.600	3.536	5.6576
X34_P16	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16	X23_P16
CP	0.0006	0.0006	0.0006	0.0006
D	0.0006	0.0006	0.0006	0.0006
E	0.0014	0.0013	0.0013	0.0013

RN	0.0010	0.0010	0.0010	0.0010
TE	0.0011	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004	0.0004
	X29_P16	X34_P16		
CP	0.0006	0.0006		
D	0.0006	0.0006		
E	0.0013	0.0013		
RN	0.0010	0.0010		
TE	0.0011	0.0011		
TI	0.0004	0.0004		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
CP to Q ↓	0.0525	0.0843	3.0427	1.5136
CP to Q ↑	0.0707	0.1108	4.4866	2.2655
RN to Q ↓	0.0503	0.0766	2.9274	1.5127
	X19_P16	**X23_P16**	**X19_P16**	**X23_P16**
CP to Q ↓	0.0919	0.0927	0.7855	0.6023
CP to Q ↑	0.1158	0.1143	1.1450	1.1215
RN to Q ↓	0.0842	0.0851	0.7854	0.6024
	X29_P16	**X34_P16**	**X29_P16**	**X34_P16**
CP to Q ↓	0.0808	0.0801	0.5232	0.4135
CP to Q ↑	0.0960	0.0969	0.7583	0.7568
RN to Q ↓	0.0762	0.0756	0.5221	0.4127

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P16	X10_P16	X19_P16	X23_P16
CP ↓	min_pulse_width to CP	0.0635	0.0641	0.0641	0.0641
CP ↑	min_pulse_width to CP	0.0454	0.0441	0.0441	0.0441
D ↓	hold_rising to CP	-0.0391	-0.0391	-0.0391	-0.0391
D ↑	hold_rising to CP	-0.0147	-0.0147	-0.0147	-0.0147
D ↓	setup_rising to CP	0.0734	0.0734	0.0734	0.0734
D ↑	setup_rising to CP	0.0422	0.0422	0.0422	0.0422
E ↓	hold_rising to CP	-0.0413	-0.0413	-0.0413	-0.0413
E ↑	hold_rising to CP	-0.0147	-0.0147	-0.0147	-0.0147
E ↓	setup_rising to CP	0.0981	0.0981	0.0981	0.0981
E ↑	setup_rising to CP	0.0732	0.0732	0.0764	0.0764
RN ↓	min_pulse_width to RN	0.0615	0.0544	0.0566	0.0566
RN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
RN ↑	removal_rising to CP	0.0091	0.0091	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0214	-0.0214	-0.0214	-0.0214

TE ↑	hold_rising to CP	-0.0071	-0.0067	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0586	0.0582	0.0582	0.0582
TE ↑	setup_rising to CP	0.0737	0.0737	0.0737	0.0737
TI ↓	hold_rising to CP	-0.0362	-0.0362	-0.0362	-0.0362
TI ↑	hold_rising to CP	-0.0079	-0.0079	-0.0079	-0.0079
TI ↓	setup_rising to CP	0.0708	0.0708	0.0708	0.0708
TI ↑	setup_rising to CP	0.0342	0.0342	0.0342	0.0342
		X29_P16	X34_P16		
CP ↓	min_pulse_width to CP	0.0641	0.0641		
CP ↑	min_pulse_width to CP	0.0454	0.0454		
D ↓	hold_rising to CP	-0.0391	-0.0391		
D ↑	hold_rising to CP	-0.0121	-0.0121		
D ↓	setup_rising to CP	0.0734	0.0734		
D ↑	setup_rising to CP	0.0422	0.0422		
E ↓	hold_rising to CP	-0.0381	-0.0381		
E ↑	hold_rising to CP	-0.0147	-0.0147		
E ↓	setup_rising to CP	0.0981	0.0981		
E ↑	setup_rising to CP	0.0764	0.0764		
RN ↓	min_pulse_width to RN	0.0615	0.0615		
RN ↑	recovery_rising to CP	-0.0017	-0.0017		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0214	-0.0214		
TE ↑	hold_rising to CP	-0.0071	-0.0071		
TE ↓	setup_rising to CP	0.0582	0.0582		
TE ↑	setup_rising to CP	0.0737	0.0737		
TI ↓	hold_rising to CP	-0.0362	-0.0362		
TI ↑	hold_rising to CP	-0.0036	-0.0036		
TI ↓	setup_rising to CP	0.0708	0.0708		
TI ↑	setup_rising to CP	0.0342	0.0342		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	4.113e-05	1.000e-20
X10_P16	4.995e-05	1.000e-20
X19_P16	6.446e-05	1.000e-20
X23_P16	6.650e-05	1.000e-20

X29_P16	8.324e-05	1.000e-20
X34_P16	8.708e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

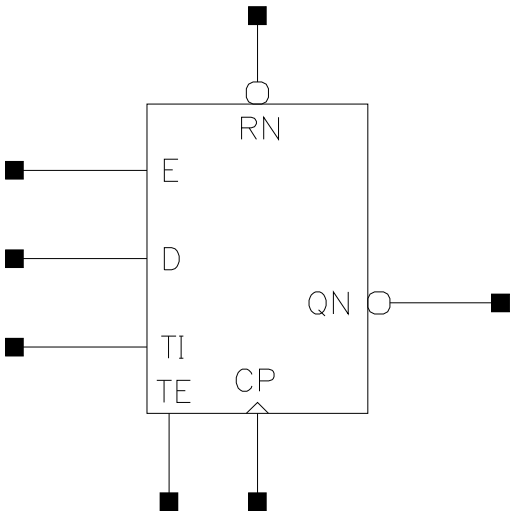
Pin Cycle	X5_P16	X10_P16	X19_P16	X23_P16
Clock 100Mhz Data 0Mhz	1.043e-02	1.041e-02	1.042e-02	1.043e-02
Clock 100Mhz Data 25Mhz	1.098e-02	1.164e-02	1.274e-02	1.287e-02
Clock 100Mhz Data 50Mhz	1.153e-02	1.287e-02	1.505e-02	1.531e-02
Clock = 0 Data 100Mhz	6.603e-03	6.603e-03	6.603e-03	6.603e-03
Clock = 1 Data 100Mhz	2.570e-03	2.571e-03	2.571e-03	2.571e-03
	X29_P16	X34_P16		
Clock 100Mhz Data 0Mhz	1.042e-02	1.043e-02		
Clock 100Mhz Data 25Mhz	1.384e-02	1.414e-02		
Clock 100Mhz Data 50Mhz	1.726e-02	1.786e-02		
Clock = 0 Data 100Mhz	6.603e-03	6.602e-03		
Clock = 1 Data 100Mhz	2.571e-03	2.571e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.600	2.992	4.7872
X10_P16	1.600	3.128	5.0048
X19_P16	1.600	3.264	5.2224
X23_P16	1.600	3.264	5.2224
X29_P16	1.600	3.536	5.6576
X34_P16	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P16	X10_P16	X19_P16	X23_P16
CP	0.0006	0.0006	0.0006	0.0006
D	0.0006	0.0006	0.0006	0.0006
E	0.0013	0.0015	0.0015	0.0015

RN	0.0010	0.0010	0.0010	0.0010
TE	0.0011	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004	0.0004
	X29_P16	X34_P16		
CP	0.0006	0.0006		
D	0.0006	0.0006		
E	0.0015	0.0013		
RN	0.0010	0.0010		
TE	0.0011	0.0011		
TI	0.0004	0.0004		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
CP to QN ↓	0.0967	0.0859	3.0375	1.5116
CP to QN ↑	0.0699	0.0670	4.4702	2.2637
RN to QN ↑	0.0619	0.0636	4.4651	2.2615
	X19_P16	**X23_P16**	**X19_P16**	**X23_P16**
CP to QN ↓	0.0914	0.0923	0.7777	0.6023
CP to QN ↑	0.0741	0.0719	1.1436	1.1214
RN to QN ↑	0.0684	0.0661	1.1424	1.1202
	X29_P16	**X34_P16**	**X29_P16**	**X34_P16**
CP to QN ↓	0.1230	0.1209	0.5230	0.4077
CP to QN ↑	0.0958	0.0951	0.7592	0.7566
RN to QN ↑	0.0877	0.0874	0.7597	0.7560

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P16	X10_P16	X19_P16	X23_P16
CP ↓	min_pulse_width to CP	0.0641	0.0641	0.0641	0.0641
CP ↑	min_pulse_width to CP	0.0440	0.0440	0.0454	0.0454
D ↓	hold_rising to CP	-0.0391	-0.0391	-0.0391	-0.0391
D ↑	hold_rising to CP	-0.0147	-0.0121	-0.0121	-0.0121
D ↓	setup_rising to CP	0.0734	0.0734	0.0734	0.0734
D ↑	setup_rising to CP	0.0422	0.0422	0.0422	0.0422
E ↓	hold_rising to CP	-0.0413	-0.0413	-0.0381	-0.0381
E ↑	hold_rising to CP	-0.0147	-0.0147	-0.0147	-0.0147
E ↓	setup_rising to CP	0.0981	0.0981	0.0981	0.0981
E ↑	setup_rising to CP	0.0764	0.0760	0.0760	0.0760
RN ↓	min_pulse_width to RN	0.0544	0.0566	0.0637	0.0637
RN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
RN ↑	removal_rising to CP	0.0091	0.0091	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0214	-0.0214	-0.0214	-0.0214

TE ↑	hold_rising to CP	-0.0067	-0.0071	-0.0071	-0.0071
TE ↓	setup_rising to CP	0.0582	0.0582	0.0582	0.0582
TE ↑	setup_rising to CP	0.0737	0.0737	0.0737	0.0737
TI ↓	hold_rising to CP	-0.0362	-0.0362	-0.0362	-0.0362
TI ↑	hold_rising to CP	-0.0079	-0.0036	-0.0036	-0.0036
TI ↓	setup_rising to CP	0.0708	0.0708	0.0708	0.0708
TI ↑	setup_rising to CP	0.0342	0.0342	0.0342	0.0342
		X29_P16	X34_P16		
CP ↓	min_pulse_width to CP	0.0641	0.0641		
CP ↑	min_pulse_width to CP	0.0441	0.0441		
D ↓	hold_rising to CP	-0.0391	-0.0391		
D ↑	hold_rising to CP	-0.0147	-0.0147		
D ↓	setup_rising to CP	0.0734	0.0734		
D ↑	setup_rising to CP	0.0422	0.0422		
E ↓	hold_rising to CP	-0.0413	-0.0413		
E ↑	hold_rising to CP	-0.0147	-0.0147		
E ↓	setup_rising to CP	0.0981	0.0981		
E ↑	setup_rising to CP	0.0764	0.0732		
RN ↓	min_pulse_width to RN	0.0544	0.0544		
RN ↑	recovery_rising to CP	-0.0017	-0.0017		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0214	-0.0214		
TE ↑	hold_rising to CP	-0.0071	-0.0071		
TE ↓	setup_rising to CP	0.0582	0.0586		
TE ↑	setup_rising to CP	0.0737	0.0737		
TI ↓	hold_rising to CP	-0.0362	-0.0362		
TI ↑	hold_rising to CP	-0.0079	-0.0079		
TI ↓	setup_rising to CP	0.0708	0.0708		
TI ↑	setup_rising to CP	0.0342	0.0342		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P16	4.072e-05	1.000e-20
X10_P16	4.879e-05	1.000e-20
X19_P16	6.260e-05	1.000e-20
X23_P16	6.555e-05	1.000e-20

X29_P16	7.885e-05	1.000e-20
X34_P16	8.435e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

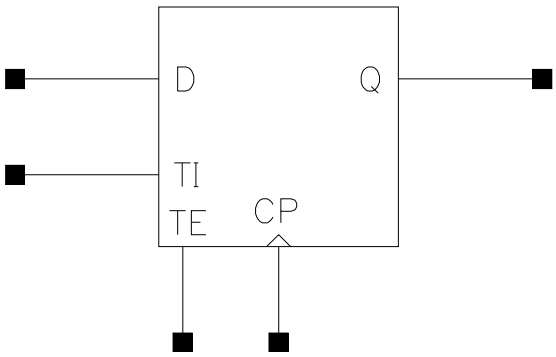
Pin Cycle	X5_P16	X10_P16	X19_P16	X23_P16
Clock 100Mhz Data 0Mhz	1.042e-02	1.043e-02	1.043e-02	1.043e-02
Clock 100Mhz Data 25Mhz	1.104e-02	1.161e-02	1.276e-02	1.287e-02
Clock 100Mhz Data 50Mhz	1.166e-02	1.279e-02	1.508e-02	1.532e-02
Clock = 0 Data 100Mhz	6.603e-03	6.604e-03	6.603e-03	6.603e-03
Clock = 1 Data 100Mhz	2.570e-03	2.571e-03	2.571e-03	2.571e-03
	X29_P16	X34_P16		
Clock 100Mhz Data 0Mhz	1.043e-02	1.043e-02		
Clock 100Mhz Data 25Mhz	1.388e-02	1.417e-02		
Clock 100Mhz Data 50Mhz	1.733e-02	1.792e-02		
Clock = 0 Data 100Mhz	6.603e-03	6.602e-03		
Clock = 1 Data 100Mhz	2.571e-03	2.571e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P16	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P16	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P16	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P16	C8T28SOI_LLHF_-SDFPQX3_P16	C8T28SOIDV_LL_-SDFPQX5_P16	C8T28SOIDV_LL_-SDFPQX10_P16
CP	0.0009	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
TE	0.0012	0.0010	0.0011	0.0011
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P16	C8T28SOIDV_LL_-SDFPQX23_P16	C8T28SOIDV_LL_-SDFPQX29_P16	
CP	0.0006	0.0006	0.0006	
D	0.0006	0.0006	0.0006	
TE	0.0011	0.0011	0.0011	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P16	**C8T28SOI_LLHF_-SDFPQX3_P16**	**C8T28SOI_LL_-SDFPQX5_P16**	**C8T28SOI_LLHF_-SDFPQX3_P16**
CP to Q ↓	0.0546	0.0468	3.1957	4.8292
CP to Q ↑	0.0532	0.0600	4.5231	6.7379
	C8T28SOIDV_LL_-SDFPQX5_P16	**C8T28SOIDV_LL_-SDFPQX10_P16**	**C8T28SOIDV_LL_-SDFPQX5_P16**	**C8T28SOIDV_LL_-SDFPQX10_P16**
CP to Q ↓	0.0494	0.0697	3.0381	1.4688
CP to Q ↑	0.0615	0.0894	4.4816	2.2415
	C8T28SOIDV_LL_-SDFPQX19_P16	**C8T28SOIDV_LL_-SDFPQX23_P16**	**C8T28SOIDV_LL_-SDFPQX19_P16**	**C8T28SOIDV_LL_-SDFPQX23_P16**
CP to Q ↓	0.0766	0.0785	0.7648	0.5990
CP to Q ↑	0.0954	0.0977	1.1313	1.1226
	C8T28SOIDV_LL_-SDFPQX29_P16		**C8T28SOIDV_LL_-SDFPQX29_P16**	
CP to Q ↓	0.0757		0.5127	
CP to Q ↑	0.0918		0.7520	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P16	C8T28SOI_-LLHF_-SDFPQX3_P16	C8T28SOIDV_-LL_SDFPQX5_-P16	C8T28SOIDV_-LL_SDFPQX10_-P16
CP ↓	min_pulse_width to CP	0.0843	0.0808	0.0745	0.0745
CP ↑	min_pulse_width to CP	0.0456	0.0364	0.0408	0.0394
D ↓	hold_rising to CP	-0.0365	-0.0773	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0098	-0.0041	-0.0001	-0.0001
D ↓	setup_rising to CP	0.0710	0.1170	0.0467	0.0467
D ↑	setup_rising to CP	0.0343	0.0337	0.0244	0.0244
TE ↓	hold_rising to CP	-0.0234	-0.0289	-0.0055	-0.0055
TE ↑	hold_rising to CP	-0.0072	-0.0046	-0.0076	-0.0076
TE ↓	setup_rising to CP	0.0689	0.0926	0.0446	0.0446
TE ↑	setup_rising to CP	0.0862	0.1106	0.0835	0.0835

TI ↓	hold_rising to CP	-0.0511	-0.0758	-0.0426	-0.0426
TI ↑	hold_rising to CP	-0.0095	-0.0029	-0.0092	-0.0092
TI ↓	setup_rising to CP	0.0857	0.1090	0.0821	0.0821
TI ↑	setup_rising to CP	0.0342	0.0286	0.0340	0.0340
		C8T28SOIDV_-LL_SDFPQX19_-P16	C8T28SOIDV_-LL_SDFPQX23_-P16	C8T28SOIDV_-LL_SDFPQX29_-P16	
CP ↓	min_pulse_width to CP	0.0745	0.0745	0.0752	
CP ↑	min_pulse_width to CP	0.0394	0.0394	0.0394	
D ↓	hold_rising to CP	-0.0072	-0.0072	-0.0072	
D ↑	hold_rising to CP	-0.0001	-0.0001	-0.0001	
D ↓	setup_rising to CP	0.0467	0.0467	0.0467	
D ↑	setup_rising to CP	0.0244	0.0244	0.0244	
TE ↓	hold_rising to CP	-0.0055	-0.0055	-0.0050	
TE ↑	hold_rising to CP	-0.0076	-0.0076	-0.0076	
TE ↓	setup_rising to CP	0.0446	0.0446	0.0446	
TE ↑	setup_rising to CP	0.0835	0.0835	0.0862	
TI ↓	hold_rising to CP	-0.0426	-0.0426	-0.0426	
TI ↑	hold_rising to CP	-0.0092	-0.0092	-0.0092	
TI ↓	setup_rising to CP	0.0821	0.0821	0.0821	
TI ↑	setup_rising to CP	0.0340	0.0340	0.0340	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P16	3.359e-05	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P16	3.007e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P16	3.166e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P16	4.272e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P16	5.250e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P16	5.529e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P16	6.796e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P16	C8T28SOI_LLHF_-SDFPQX3_P16	C8T28SOIDV_LL_-SDFPQX5_P16	C8T28SOIDV_LL_-SDFPQX10_P16
Clock 100Mhz Data 0Mhz	1.028e-02	9.814e-03	9.442e-03	9.251e-03
Clock 100Mhz Data 25Mhz	1.004e-02	9.578e-03	9.390e-03	9.870e-03
Clock 100Mhz Data 50Mhz	9.795e-03	9.341e-03	9.337e-03	1.049e-02

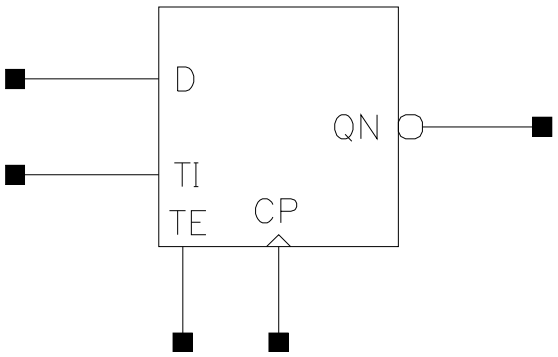
Clock = 0 Data 100Mhz	5.232e-03	5.447e-03	5.169e-03	5.027e-03
Clock = 1 Data 100Mhz	3.397e-05	6.511e-04	4.464e-04	3.442e-04
	C8T28SOIDV_LL_-SDFPQX19_P16	C8T28SOIDV_LL_-SDFPQX23_P16	C8T28SOIDV_LL_-SDFPQX29_P16	
Clock 100Mhz Data 0Mhz	9.140e-03	9.066e-03	9.015e-03	
Clock 100Mhz Data 25Mhz	1.070e-02	1.079e-02	1.159e-02	
Clock 100Mhz Data 50Mhz	1.225e-02	1.251e-02	1.417e-02	
Clock = 0 Data 100Mhz	4.940e-03	4.881e-03	4.843e-03	
Clock = 1 Data 100Mhz	2.828e-04	2.420e-04	2.128e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P16	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P16	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P16	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P16	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P16	C8T28SOI_LLHF_-SDFPQNX3_P16	C8T28SOIDV_LL_-SDFPQNX5_P16	C8T28SOIDV_LL_-SDFPQNX10_P16

CP	0.0009	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
TE	0.0012	0.0010	0.0011	0.0011
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P16	C8T28SOIDV_LL_-SDFPQNX29_P16		
CP	0.0006	0.0006		
D	0.0006	0.0006		
TE	0.0011	0.0011		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P16	**C8T28SOI_LLHF_-SDFPQNX3_P16**	**C8T28SOI_LL_-SDFPQNX5_P16**	**C8T28SOI_LLHF_-SDFPQNX3_P16**
CP to QN ↓	0.0692	0.0732	3.0754	4.5466
CP to QN ↑	0.0596	0.0565	4.8608	6.5643
	C8T28SOIDV_LL_-SDFPQNX5_P16	**C8T28SOIDV_LL_-SDFPQNX10_P16**	**C8T28SOIDV_LL_-SDFPQNX5_P16**	**C8T28SOIDV_LL_-SDFPQNX10_P16**
CP to QN ↓	0.0765	0.0729	2.9788	1.4803
CP to QN ↑	0.0562	0.0618	4.4273	2.2420
	C8T28SOIDV_LL_-SDFPQNX19_P16	**C8T28SOIDV_LL_-SDFPQNX29_P16**	**C8T28SOIDV_LL_-SDFPQNX19_P16**	**C8T28SOIDV_LL_-SDFPQNX29_P16**
CP to QN ↓	0.0826	0.0967	0.7722	0.5284
CP to QN ↑	0.0728	0.0829	1.1486	0.7560

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P16	C8T28SOI_-LLHF_-SDFPQNX3_P16	C8T28SOIDV_-LL_SDFPQNX5_-P16	C8T28SOIDV_-LL_-SDFPQNX10_-P16
CP ↓	min_pulse_width to CP	0.0843	0.0808	0.0745	0.0745
CP ↑	min_pulse_width to CP	0.0362	0.0317	0.0394	0.0408
D ↓	hold_rising to CP	-0.0365	-0.0777	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0098	-0.0041	-0.0000	-0.0001
D ↓	setup_rising to CP	0.0710	0.1137	0.0467	0.0467
D ↑	setup_rising to CP	0.0343	0.0337	0.0244	0.0244
TE ↓	hold_rising to CP	-0.0234	-0.0289	-0.0055	-0.0055
TE ↑	hold_rising to CP	-0.0072	-0.0046	-0.0043	-0.0076
TE ↓	setup_rising to CP	0.0689	0.0904	0.0446	0.0446
TE ↑	setup_rising to CP	0.0862	0.1106	0.0835	0.0835
TI ↓	hold_rising to CP	-0.0511	-0.0758	-0.0426	-0.0426
TI ↑	hold_rising to CP	-0.0095	-0.0022	-0.0036	-0.0092
TI ↓	setup_rising to CP	0.0857	0.1047	0.0821	0.0821

TI ↑	setup_rising to CP	0.0342	0.0286	0.0299	0.0340
		C8T28SOIDV_-LL_-SDFPQNX19_-P16	C8T28SOIDV_-LL_-SDFPQNX29_-P16		
CP ↓	min_pulse_width to CP	0.0745	0.0745		
CP ↑	min_pulse_width to CP	0.0454	0.0394		
D ↓	hold_rising to CP	-0.0072	-0.0072		
D ↑	hold_rising to CP	-0.0001	-0.0001		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0249	0.0244		
TE ↓	hold_rising to CP	-0.0055	-0.0055		
TE ↑	hold_rising to CP	-0.0076	-0.0076		
TE ↓	setup_rising to CP	0.0446	0.0446		
TE ↑	setup_rising to CP	0.0835	0.0835		
TI ↓	hold_rising to CP	-0.0426	-0.0426		
TI ↑	hold_rising to CP	-0.0092	-0.0092		
TI ↓	setup_rising to CP	0.0821	0.0821		
TI ↑	setup_rising to CP	0.0340	0.0340		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P16	3.322e-05	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P16	3.044e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P16	3.196e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P16	4.199e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P16	5.264e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P16	7.621e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P16	C8T28SOI_LLHF_-SDFPQNX3_P16	C8T28SOIDV_LL_-SDFPQNX5_P16	C8T28SOIDV_LL_-SDFPQNX10_P16
Clock 100Mhz Data 0Mhz	1.028e-02	9.923e-03	9.528e-03	9.314e-03
Clock 100Mhz Data 25Mhz	9.927e-03	9.670e-03	9.351e-03	9.868e-03
Clock 100Mhz Data 50Mhz	9.578e-03	9.417e-03	9.173e-03	1.042e-02
Clock = 0 Data 100Mhz	5.233e-03	5.469e-03	5.191e-03	5.045e-03
Clock = 1 Data 100Mhz	3.411e-05	6.548e-04	4.489e-04	3.460e-04

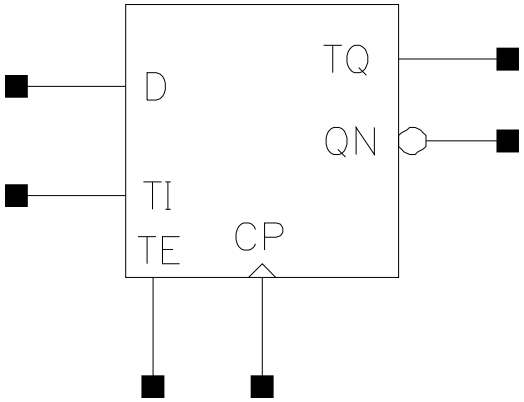
	C8T28SOIDV_LL_-SDFPQNX19_P16	C8T28SOIDV_LL_-SDFPQNX29_P16		
Clock 100Mhz Data 0Mhz	9.189e-03	9.103e-03		
Clock 100Mhz Data 25Mhz	1.090e-02	1.224e-02		
Clock 100Mhz Data 50Mhz	1.261e-02	1.537e-02		
Clock = 0 Data 100Mhz	4.952e-03	4.895e-03		
Clock = 1 Data 100Mhz	2.843e-04	2.432e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P16	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P16	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P16	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P16	C8T28SOI_LLHF_-SDFPQNTX3_P16	C8T28SOIDV_LL_-SDFPQNTX5_P16	C8T28SOIDV_LL_-SDFPQNTX10_P16
CP	0.0009	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
TE	0.0012	0.0010	0.0011	0.0011
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P16	C8T28SOIDV_LL_-SDFPQNTX29_P16		
CP	0.0006	0.0006		
D	0.0006	0.0006		
TE	0.0011	0.0011		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQNTX5_P16	**C8T28SOI_LLHF_-SDFPQNTX3_P16**	**C8T28SOI_LL_-SDFPQNTX5_P16**	**C8T28SOI_LLHF_-SDFPQNTX3_P16**
CP to QN ↓	0.0785	0.0802	3.1775	4.6147
CP to QN ↑	0.0763	0.0697	4.8632	6.5828
CP to TQ ↓	0.0610	0.0482	7.8360	5.3122
CP to TQ ↑	0.0654	0.0595	19.8847	11.1443
	C8T28SOIDV_LL_-SDFPQNTX5_P16	**C8T28SOIDV_LL_-SDFPQNTX10_P16**	**C8T28SOIDV_LL_-SDFPQNTX5_P16**	**C8T28SOIDV_LL_-SDFPQNTX10_P16**
CP to QN ↓	0.0821	0.0810	2.9276	1.4924
CP to QN ↑	0.0662	0.0673	4.4251	2.2433
CP to TQ ↓	0.0458	0.0477	5.2683	5.5098
CP to TQ ↑	0.0610	0.0625	9.0450	9.4372
	C8T28SOIDV_LL_-SDFPQNTX19_P16	**C8T28SOIDV_LL_-SDFPQNTX29_P16**	**C8T28SOIDV_LL_-SDFPQNTX19_P16**	**C8T28SOIDV_LL_-SDFPQNTX29_P16**
CP to QN ↓	0.0845	0.0992	0.7695	0.5300
CP to QN ↑	0.0739	0.0883	1.1407	0.7535
CP to TQ ↓	0.0496	0.0480	5.3929	5.5545
CP to TQ ↑	0.0645	0.0647	9.5935	11.9750

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_-P16	C8T28SOI_-LLHF_-SDFPQNTX3_-P16	C8T28SOIDV_-LL_-SDFPQNTX5_-P16	C8T28SOIDV_-LL_-SDFPQNTX10_-P16
CP ↓	min_pulse_width to CP	0.0843	0.0808	0.0745	0.0745
CP ↑	min_pulse_width to CP	0.0469	0.0411	0.0408	0.0408
D ↓	hold_rising to CP	-0.0365	-0.0745	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0098	-0.0041	-0.0000	-0.0001
D ↓	setup_rising to CP	0.0710	0.1142	0.0467	0.0467

D ↑	setup_rising to CP	0.0343	0.0337	0.0244	0.0244
TE ↓	hold_rising to CP	-0.0234	-0.0289	-0.0050	-0.0055
TE ↑	hold_rising to CP	-0.0072	-0.0046	-0.0043	-0.0076
TE ↓	setup_rising to CP	0.0689	0.0872	0.0446	0.0446
TE ↑	setup_rising to CP	0.0862	0.1106	0.0835	0.0835
TI ↓	hold_rising to CP	-0.0511	-0.0743	-0.0426	-0.0426
TI ↑	hold_rising to CP	-0.0095	-0.0022	-0.0036	-0.0092
TI ↓	setup_rising to CP	0.0857	0.1047	0.0821	0.0821
TI ↑	setup_rising to CP	0.0342	0.0286	0.0299	0.0340
		C8T28SOIDV_-LL_-SDFPQNTX19_-P16	C8T28SOIDV_-LL_-SDFPQNTX29_-P16		
CP ↓	min_pulse_width to CP	0.0745	0.0746		
CP ↑	min_pulse_width to CP	0.0454	0.0408		
D ↓	hold_rising to CP	-0.0072	-0.0072		
D ↑	hold_rising to CP	-0.0001	-0.0001		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0244	0.0244		
TE ↓	hold_rising to CP	-0.0055	-0.0055		
TE ↑	hold_rising to CP	-0.0076	-0.0076		
TE ↓	setup_rising to CP	0.0446	0.0446		
TE ↑	setup_rising to CP	0.0835	0.0835		
TI ↓	hold_rising to CP	-0.0426	-0.0426		
TI ↑	hold_rising to CP	-0.0092	-0.0092		
TI ↓	setup_rising to CP	0.0821	0.0821		
TI ↑	setup_rising to CP	0.0340	0.0340		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P16	3.395e-05	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P16	3.258e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P16	3.418e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P16	4.023e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P16	5.233e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P16	7.767e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

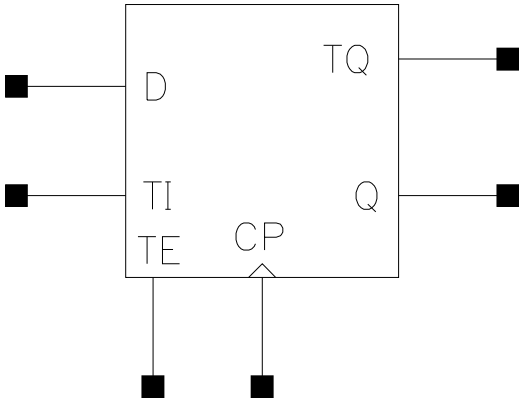
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P16	C8T28SOI_LLHF_-SDFPQNTX3_P16	C8T28SOIDV_LL_-SDFPQNTX5_P16	C8T28SOIDV_LL_-SDFPQNTX10_P16
Clock 100Mhz Data 0Mhz	1.028e-02	9.922e-03	9.520e-03	9.308e-03
Clock 100Mhz Data 25Mhz	1.036e-02	9.999e-03	9.658e-03	9.875e-03
Clock 100Mhz Data 50Mhz	1.044e-02	1.008e-02	9.795e-03	1.044e-02
Clock = 0 Data 100Mhz	5.230e-03	5.464e-03	5.191e-03	5.044e-03
Clock = 1 Data 100Mhz	3.374e-05	6.575e-04	4.507e-04	3.474e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P16	C8T28SOIDV_LL_-SDFPQNTX29_P16		
Clock 100Mhz Data 0Mhz	9.182e-03	9.092e-03		
Clock 100Mhz Data 25Mhz	1.083e-02	1.247e-02		
Clock 100Mhz Data 50Mhz	1.248e-02	1.585e-02		
Clock = 0 Data 100Mhz	4.956e-03	4.898e-03		
Clock = 1 Data 100Mhz	2.854e-04	2.441e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P16	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P16	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P16	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P16	C8T28SOI_LLHF_-SDFPQTX3_P16	C8T28SOIDV_LL_-SDFPQTX5_P16	C8T28SOIDV_LL_-SDFPQTX10_P16
CP	0.0009	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
TE	0.0012	0.0010	0.0011	0.0011
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P16	C8T28SOIDV_LL_-SDFPQTX29_P16		
CP	0.0006	0.0006		
D	0.0006	0.0006		
TE	0.0011	0.0011		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQTX5_P16	**C8T28SOI_LLHF_-SDFPQTX3_P16**	**C8T28SOI_LL_-SDFPQTX5_P16**	**C8T28SOI_LLHF_-SDFPQTX3_P16**
CP to Q ↓	0.0656	0.0592	3.3839	5.0098
CP to Q ↑	0.0585	0.0612	4.5585	6.8376
CP to TQ ↓	0.0746	0.0572	8.5517	5.4900
CP to TQ ↑	0.0726	0.0645	20.1123	11.3151
	C8T28SOIDV_LL_-SDFPQTX5_P16	**C8T28SOIDV_LL_-SDFPQTX10_P16**	**C8T28SOIDV_LL_-SDFPQTX5_P16**	**C8T28SOIDV_LL_-SDFPQTX10_P16**
CP to Q ↓	0.0542	0.0719	3.1153	1.4772
CP to Q ↑	0.0640	0.0913	4.5378	2.2442
CP to TQ ↓	0.0531	0.0739	5.4360	5.5191
CP to TQ ↑	0.0658	0.0948	9.8378	9.7652
	C8T28SOIDV_LL_-SDFPQTX19_P16	**C8T28SOIDV_LL_-SDFPQTX29_P16**	**C8T28SOIDV_LL_-SDFPQTX19_P16**	**C8T28SOIDV_LL_-SDFPQTX29_P16**
CP to Q ↓	0.0787	0.0854	0.7683	0.4998
CP to Q ↑	0.0966	0.0963	1.1364	0.7490
CP to TQ ↓	0.0815	0.0502	5.5789	5.7014
CP to TQ ↑	0.1019	0.0659	9.7990	11.9715

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P16	C8T28SOI_-LLHF_-SDFPQTX3_P16	C8T28SOIDV_-LL_SDFPQTX5_-P16	C8T28SOIDV_-LL_-SDFPQTX10_-P16
CP ↓	min_pulse_width to CP	0.0843	0.0808	0.0745	0.0745
CP ↑	min_pulse_width to CP	0.0550	0.0457	0.0455	0.0394
D ↓	hold_rising to CP	-0.0365	-0.0777	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0098	-0.0041	-0.0001	-0.0001
D ↓	setup_rising to CP	0.0710	0.1137	0.0467	0.0467

D ↑	setup_rising to CP	0.0343	0.0337	0.0244	0.0244
TE ↓	hold_rising to CP	-0.0234	-0.0289	-0.0055	-0.0055
TE ↑	hold_rising to CP	-0.0072	-0.0046	-0.0076	-0.0076
TE ↓	setup_rising to CP	0.0689	0.0872	0.0446	0.0446
TE ↑	setup_rising to CP	0.0862	0.1106	0.0835	0.0835
TI ↓	hold_rising to CP	-0.0511	-0.0743	-0.0426	-0.0426
TI ↑	hold_rising to CP	-0.0095	-0.0022	-0.0092	-0.0092
TI ↓	setup_rising to CP	0.0857	0.1047	0.0821	0.0821
TI ↑	setup_rising to CP	0.0342	0.0286	0.0340	0.0340
		C8T28SOIDV_-LL_-SDFPQTX19_-P16	C8T28SOIDV_-LL_-SDFPQTX29_-P16		
CP ↓	min_pulse_width to CP	0.0745	0.0752		
CP ↑	min_pulse_width to CP	0.0394	0.0454		
D ↓	hold_rising to CP	-0.0072	-0.0072		
D ↑	hold_rising to CP	-0.0001	-0.0001		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0244	0.0244		
TE ↓	hold_rising to CP	-0.0055	-0.0050		
TE ↑	hold_rising to CP	-0.0076	-0.0076		
TE ↓	setup_rising to CP	0.0446	0.0446		
TE ↑	setup_rising to CP	0.0835	0.0862		
TI ↓	hold_rising to CP	-0.0426	-0.0426		
TI ↑	hold_rising to CP	-0.0092	-0.0092		
TI ↓	setup_rising to CP	0.0821	0.0821		
TI ↑	setup_rising to CP	0.0340	0.0340		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P16	3.444e-05	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P16	3.258e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P16	3.401e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P16	4.492e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P16	5.540e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P16	7.168e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

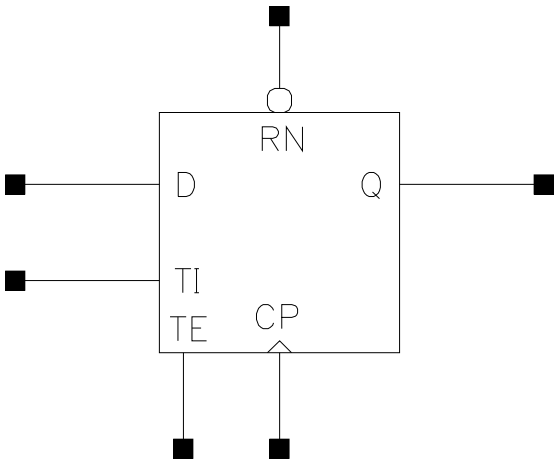
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P16	C8T28SOI_LLHF_-SDFPQTX3_P16	C8T28SOIDV_LL_-SDFPQTX5_P16	C8T28SOIDV_LL_-SDFPQTX10_P16
Clock 100Mhz Data 0Mhz	1.028e-02	9.932e-03	9.523e-03	9.311e-03
Clock 100Mhz Data 25Mhz	1.049e-02	1.006e-02	9.736e-03	1.016e-02
Clock 100Mhz Data 50Mhz	1.069e-02	1.018e-02	9.950e-03	1.101e-02
Clock = 0 Data 100Mhz	5.237e-03	5.469e-03	5.186e-03	5.040e-03
Clock = 1 Data 100Mhz	3.383e-05	6.556e-04	4.495e-04	3.465e-04
	C8T28SOIDV_LL_-SDFPQTX19_P16	C8T28SOIDV_LL_-SDFPQTX29_P16		
Clock 100Mhz Data 0Mhz	9.188e-03	9.110e-03		
Clock 100Mhz Data 25Mhz	1.106e-02	1.200e-02		
Clock 100Mhz Data 50Mhz	1.293e-02	1.488e-02		
Clock = 0 Data 100Mhz	4.950e-03	4.896e-03		
Clock = 1 Data 100Mhz	2.847e-04	2.436e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P16	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P16	C8T28SOI_LLHF_-SDFPRQX3_P16	C8T28SOIDV_LL_-SDFPRQX5_P16	C8T28SOIDV_LL_-SDFPRQX10_P16
CP	0.0009	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
RN	0.0010	0.0009	0.0011	0.0011
TE	0.0012	0.0010	0.0011	0.0011
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P16	C8T28SOIDV_LL_-SDFPRQX29_P16		
CP	0.0006	0.0006		
D	0.0006	0.0006		
RN	0.0010	0.0010		
TE	0.0011	0.0011		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P16	**C8T28SOI_LLHF_-SDFPRQX3_P16**	**C8T28SOI_LL_-SDFPRQX5_P16**	**C8T28SOI_LLHF_-SDFPRQX3_P16**
CP to Q ↓	0.0617	0.0557	3.2193	4.8663
CP to Q ↑	0.0553	0.0602	4.5245	6.6766
RN to Q ↓	0.0460	0.0427	3.0560	4.6774
	C8T28SOIDV_LL_-SDFPRQX5_P16	**C8T28SOIDV_LL_-SDFPRQX10_P16**	**C8T28SOIDV_LL_-SDFPRQX5_P16**	**C8T28SOIDV_LL_-SDFPRQX10_P16**
CP to Q ↓	0.0499	0.0712	3.0321	1.4839
CP to Q ↑	0.0640	0.0927	4.4745	2.2469
RN to Q ↓	0.0513	0.0679	2.9201	1.4842
	C8T28SOIDV_LL_-SDFPRQX19_P16	**C8T28SOIDV_LL_-SDFPRQX29_P16**	**C8T28SOIDV_LL_-SDFPRQX19_P16**	**C8T28SOIDV_LL_-SDFPRQX29_P16**
CP to Q ↓	0.0771	0.0787	0.7660	0.5219
CP to Q ↑	0.0979	0.1020	1.1480	0.7800
RN to Q ↓	0.0734	0.0753	0.7662	0.5219

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P16	C8T28SOI_-LLHF_-SDFPRQX3_P16	C8T28SOIDV_-LL_SDFPRQX5_-P16	C8T28SOIDV_-LL_-SDFPRQX10_-P16
CP ↓	min_pulse_width to CP	0.0859	0.0808	0.0753	0.0753
CP ↑	min_pulse_width to CP	0.0503	0.0411	0.0408	0.0394
D ↓	hold_rising to CP	-0.0365	-0.0724	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0098	-0.0099	0.0009	0.0009
D ↓	setup_rising to CP	0.0710	0.1121	0.0467	0.0467
D ↑	setup_rising to CP	0.0337	0.0396	0.0272	0.0272
RN ↓	min_pulse_width to RN	0.0593	0.0571	0.0566	0.0496
RN ↑	recovery_rising to CP	0.0054	0.0032	0.0032	0.0032

RN ↑	removal_rising to CP	0.0042	0.0042	0.0042	0.0042
TE ↓	hold_rising to CP	-0.0263	-0.0284	-0.0055	-0.0055
TE ↑	hold_rising to CP	-0.0072	-0.0062	-0.0092	-0.0092
TE ↓	setup_rising to CP	0.0689	0.0877	0.0442	0.0442
TE ↑	setup_rising to CP	0.0862	0.1057	0.0835	0.0835
TI ↓	hold_rising to CP	-0.0511	-0.0703	-0.0433	-0.0433
TI ↑	hold_rising to CP	-0.0092	-0.0037	-0.0100	-0.0100
TI ↓	setup_rising to CP	0.0857	0.1041	0.0806	0.0821
TI ↑	setup_rising to CP	0.0332	0.0326	0.0391	0.0391
		C8T28SOIDV_-LL_-SDFPRQX19_-P16	C8T28SOIDV_-LL_-SDFPRQX29_-P16		
CP ↓	min_pulse_width to CP	0.0753	0.0753		
CP ↑	min_pulse_width to CP	0.0394	0.0394		
D ↓	hold_rising to CP	-0.0072	-0.0072		
D ↑	hold_rising to CP	0.0009	0.0009		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0272	0.0272		
RN ↓	min_pulse_width to RN	0.0496	0.0518		
RN ↑	recovery_rising to CP	0.0032	0.0032		
RN ↑	removal_rising to CP	0.0042	0.0042		
TE ↓	hold_rising to CP	-0.0050	-0.0050		
TE ↑	hold_rising to CP	-0.0092	-0.0092		
TE ↓	setup_rising to CP	0.0442	0.0442		
TE ↑	setup_rising to CP	0.0835	0.0835		
TI ↓	hold_rising to CP	-0.0426	-0.0375		
TI ↑	hold_rising to CP	-0.0100	-0.0100		
TI ↓	setup_rising to CP	0.0806	0.0821		
TI ↑	setup_rising to CP	0.0391	0.0391		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P16	3.622e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P16	3.327e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P16	3.453e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P16	4.490e-05	1.000e-20

C8T28SOIDV_LL_SDFPRQX19_P16	5.611e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P16	7.079e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

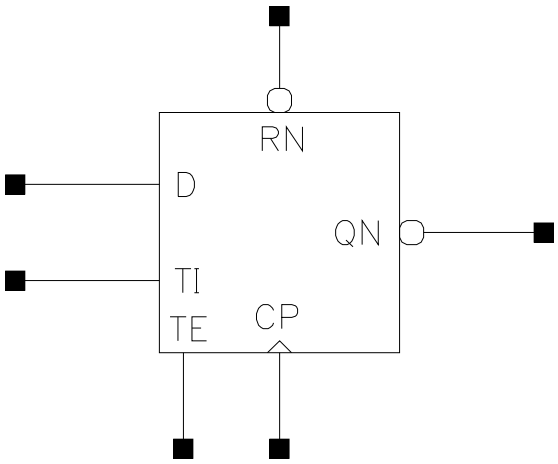
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P16	C8T28SOI_LLHF_-SDFPRQX3_P16	C8T28SOIDV_LL_-SDFPRQX5_P16	C8T28SOIDV_LL_-SDFPRQX10_P16
Clock 100Mhz Data 0Mhz	1.064e-02	1.019e-02	9.753e-03	9.536e-03
Clock 100Mhz Data 25Mhz	1.036e-02	9.951e-03	9.584e-03	1.011e-02
Clock 100Mhz Data 50Mhz	1.008e-02	9.714e-03	9.416e-03	1.068e-02
Clock = 0 Data 100Mhz	4.934e-03	5.220e-03	5.042e-03	4.955e-03
Clock = 1 Data 100Mhz	3.393e-05	6.588e-04	4.511e-04	3.473e-04
	C8T28SOIDV_LL_-SDFPRQX19_P16	C8T28SOIDV_LL_-SDFPRQX29_P16		
Clock 100Mhz Data 0Mhz	9.404e-03	9.319e-03		
Clock 100Mhz Data 25Mhz	1.090e-02	1.200e-02		
Clock 100Mhz Data 50Mhz	1.240e-02	1.467e-02		
Clock = 0 Data 100Mhz	4.901e-03	4.868e-03		
Clock = 1 Data 100Mhz	2.851e-04	2.437e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P16	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P16	C8T28SOI_LLHF_-SDFPRQNX3_P16	C8T28SOIDV_LL_-SDFPRQNX5_P16	C8T28SOIDV_LL_-SDFPRQNX10_P16
CP	0.0009	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
RN	0.0010	0.0009	0.0011	0.0010
TE	0.0012	0.0010	0.0011	0.0011
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P16	C8T28SOIDV_LL_-SDFPRQNX29_P16		
CP	0.0006	0.0006		
D	0.0006	0.0006		
RN	0.0009	0.0009		
TE	0.0011	0.0011		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNX5_P16	**C8T28SOI_LLHF_-SDFPRQNX3_P16**	**C8T28SOI_LL_-SDFPRQNX5_P16**	**C8T28SOI_LLHF_-SDFPRQNX3_P16**
CP to QN ↓	0.0727	0.0761	3.1507	4.5552
CP to QN ↑	0.0652	0.0613	4.6578	6.5616
RN to QN ↑	0.0534	0.0515	4.6487	6.5567
	C8T28SOIDV_LL_-SDFPRQNX5_P16	**C8T28SOIDV_LL_-SDFPRQNX10_P16**	**C8T28SOIDV_LL_-SDFPRQNX5_P16**	**C8T28SOIDV_LL_-SDFPRQNX10_P16**
CP to QN ↓	0.0818	0.0755	2.9231	1.4847
CP to QN ↑	0.0616	0.0622	4.4210	2.2461
RN to QN ↑	0.0579	0.0622	4.4242	2.2432
	C8T28SOIDV_LL_-SDFPRQNX19_P16	**C8T28SOIDV_LL_-SDFPRQNX29_P16**	**C8T28SOIDV_LL_-SDFPRQNX19_P16**	**C8T28SOIDV_LL_-SDFPRQNX29_P16**
CP to QN ↓	0.0846	0.0899	0.7821	0.5239
CP to QN ↑	0.0697	0.0781	1.1540	0.7758
RN to QN ↑	0.0662	0.0697	1.1523	0.7744

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P16	C8T28SOI_-LLHF_-SDFPRQNX3_-P16	C8T28SOIDV_-LL_-SDFPRQNX5_-P16	C8T28SOIDV_-LL_-SDFPRQNX10_-P16
CP ↓	min_pulse_width to CP	0.0859	0.0808	0.0753	0.0753
CP ↑	min_pulse_width to CP	0.0409	0.0364	0.0394	0.0408
D ↓	hold_rising to CP	-0.0365	-0.0724	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0098	-0.0099	0.0009	0.0009
D ↓	setup_rising to CP	0.0710	0.1121	0.0467	0.0467
D ↑	setup_rising to CP	0.0337	0.0396	0.0239	0.0272
RN ↓	min_pulse_width to RN	0.0571	0.0571	0.0518	0.0588
RN ↑	recovery_rising to CP	0.0054	0.0032	0.0032	0.0032

RN ↑	removal_rising to CP	0.0042	0.0048	0.0042	0.0042
TE ↓	hold_rising to CP	-0.0263	-0.0279	-0.0050	-0.0055
TE ↑	hold_rising to CP	-0.0072	-0.0062	-0.0098	-0.0098
TE ↓	setup_rising to CP	0.0689	0.0877	0.0442	0.0442
TE ↑	setup_rising to CP	0.0862	0.1057	0.0835	0.0835
TI ↓	hold_rising to CP	-0.0511	-0.0703	-0.0375	-0.0375
TI ↑	hold_rising to CP	-0.0092	-0.0037	-0.0092	-0.0100
TI ↓	setup_rising to CP	0.0857	0.1041	0.0821	0.0821
TI ↑	setup_rising to CP	0.0332	0.0326	0.0348	0.0391
		C8T28SOIDV_-LL_-SDFPRQNX19_-P16	C8T28SOIDV_-LL_-SDFPRQNX29_-P16		
CP ↓	min_pulse_width to CP	0.0769	0.0793		
CP ↑	min_pulse_width to CP	0.0440	0.0500		
D ↓	hold_rising to CP	-0.0072	-0.0023		
D ↑	hold_rising to CP	0.0005	0.0005		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0239	0.0239		
RN ↓	min_pulse_width to RN	0.0588	0.0708		
RN ↑	recovery_rising to CP	-0.0000	0.0005		
RN ↑	removal_rising to CP	0.0043	0.0043		
TE ↓	hold_rising to CP	-0.0001	-0.0001		
TE ↑	hold_rising to CP	-0.0098	-0.0098		
TE ↓	setup_rising to CP	0.0446	0.0446		
TE ↑	setup_rising to CP	0.0835	0.0835		
TI ↓	hold_rising to CP	-0.0377	-0.0377		
TI ↑	hold_rising to CP	-0.0092	-0.0092		
TI ↓	setup_rising to CP	0.0821	0.0821		
TI ↑	setup_rising to CP	0.0391	0.0391		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P16	3.552e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P16	3.349e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P16	3.415e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P16	4.422e-05	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P16	5.264e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P16	6.716e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

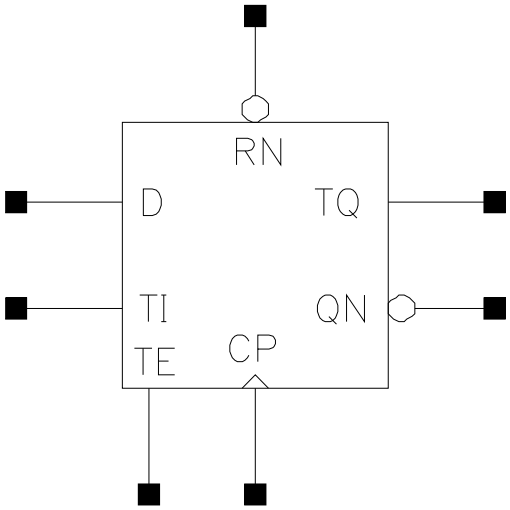
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P16	C8T28SOI_LLHF_-SDFPRQNX3_P16	C8T28SOIDV_LL_-SDFPRQNX5_P16	C8T28SOIDV_LL_-SDFPRQNX10_P16
Clock 100Mhz Data 0Mhz	1.062e-02	1.016e-02	9.737e-03	9.523e-03
Clock 100Mhz Data 25Mhz	1.022e-02	9.877e-03	9.602e-03	1.010e-02
Clock 100Mhz Data 50Mhz	9.814e-03	9.595e-03	9.467e-03	1.067e-02
Clock = 0 Data 100Mhz	4.932e-03	5.220e-03	5.048e-03	4.959e-03
Clock = 1 Data 100Mhz	3.396e-05	6.588e-04	4.511e-04	3.473e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P16	C8T28SOIDV_LL_-SDFPRQNX29_P16		
Clock 100Mhz Data 0Mhz	9.455e-03	9.438e-03		
Clock 100Mhz Data 25Mhz	1.101e-02	1.239e-02		
Clock 100Mhz Data 50Mhz	1.257e-02	1.534e-02		
Clock = 0 Data 100Mhz	4.903e-03	4.866e-03		
Clock = 1 Data 100Mhz	2.850e-04	2.436e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P16	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P16	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P16	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P16	C8T28SOI_LLHF_-SDFPRQNTX3_P16	C8T28SOIDV_LL_-SDFPRQNTX5_P16	C8T28SOIDV_LL_-SDFPRQNTX10_P16
CP	0.0009	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
RN	0.0010	0.0010	0.0011	0.0011
TE	0.0012	0.0010	0.0011	0.0011
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P16	C8T28SOIDV_LL_-SDFPRQNTX29_P16		
CP	0.0006	0.0006		
D	0.0006	0.0006		
RN	0.0009	0.0009		
TE	0.0011	0.0011		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPRQNTX5_P16	**C8T28SOI_LLHF_-SDFPRQNTX3_P16**	**C8T28SOI_LL_-SDFPRQNTX5_P16**	**C8T28SOI_LLHF_-SDFPRQNTX3_P16**
CP to QN ↓	0.0810	0.0830	3.0932	4.6018
CP to QN ↑	0.0822	0.0745	4.8645	6.5820
CP to TQ ↓	0.0675	0.0529	8.1848	5.3555
CP to TQ ↑	0.0668	0.0620	19.8949	11.1654
RN to QN ↑	0.0658	0.0614	4.8634	6.5829
RN to TQ ↓	0.0519	0.0405	7.9826	5.2251
	C8T28SOIDV_LL_-SDFPRQNTX5_P16	**C8T28SOIDV_LL_-SDFPRQNTX10_P16**	**C8T28SOIDV_LL_-SDFPRQNTX5_P16**	**C8T28SOIDV_LL_-SDFPRQNTX10_P16**
CP to QN ↓	0.0865	0.0926	2.9550	1.5319
CP to QN ↑	0.0682	0.0727	4.4075	2.2359
CP to TQ ↓	0.0467	0.0473	5.2811	5.3137
CP to TQ ↑	0.0642	0.0641	9.0470	9.0551
RN to QN ↑	0.0677	0.0716	4.4236	2.2398
RN to TQ ↓	0.0499	0.0504	5.1607	5.1974
	C8T28SOIDV_LL_-SDFPRQNTX19_P16	**C8T28SOIDV_LL_-SDFPRQNTX29_P16**	**C8T28SOIDV_LL_-SDFPRQNTX19_P16**	**C8T28SOIDV_LL_-SDFPRQNTX29_P16**
CP to QN ↓	0.0887	0.0906	0.7702	0.5240
CP to QN ↑	0.0757	0.0848	1.1307	0.7691
CP to TQ ↓	0.0512	0.0627	5.3722	6.1173
CP to TQ ↑	0.0681	0.0764	9.0790	10.3260
RN to QN ↑	0.0703	0.0727	1.1343	0.7701
RN to TQ ↓	0.0504	0.0564	5.2270	5.8193

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P16	C8T28SOI_-LLHF_-SDFPRQNTX3_-P16	C8T28SOIDV_-LL_-SDFPRQNTX5_-P16	C8T28SOIDV_-LL_SDF-PRQNTX10_P16
CP ↓	min_pulse_width to CP	0.0859	0.0808	0.0753	0.0753
CP ↑	min_pulse_width to CP	0.0516	0.0457	0.0408	0.0441
D ↓	hold_rising to CP	-0.0338	-0.0724	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0098	-0.0099	0.0009	0.0009
D ↓	setup_rising to CP	0.0711	0.1121	0.0467	0.0467
D ↑	setup_rising to CP	0.0337	0.0396	0.0239	0.0272
RN ↓	min_pulse_width to RN	0.0615	0.0566	0.0588	0.0615
RN ↑	recovery_rising to CP	0.0054	0.0032	0.0032	0.0032
RN ↑	removal_rising to CP	0.0042	0.0048	0.0042	0.0042
TE ↓	hold_rising to CP	-0.0263	-0.0279	-0.0055	-0.0055
TE ↑	hold_rising to CP	-0.0072	-0.0062	-0.0071	-0.0092
TE ↓	setup_rising to CP	0.0689	0.0877	0.0442	0.0442
TE ↑	setup_rising to CP	0.0862	0.1053	0.0835	0.0835
TI ↓	hold_rising to CP	-0.0475	-0.0703	-0.0375	-0.0433
TI ↑	hold_rising to CP	-0.0092	-0.0037	-0.0092	-0.0100
TI ↓	setup_rising to CP	0.0857	0.1041	0.0821	0.0821
TI ↑	setup_rising to CP	0.0332	0.0326	0.0391	0.0391
		C8T28SOIDV_-LL_SDF-PRQNTX19_P16	C8T28SOIDV_-LL_SDF-PRQNTX29_P16		
CP ↓	min_pulse_width to CP	0.0769	0.0769		
CP ↑	min_pulse_width to CP	0.0454	0.0547		
D ↓	hold_rising to CP	-0.0072	-0.0045		
D ↑	hold_rising to CP	0.0005	0.0005		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0239	0.0272		
RN ↓	min_pulse_width to RN	0.0637	0.0757		
RN ↑	recovery_rising to CP	-0.0000	0.0032		
RN ↑	removal_rising to CP	0.0043	0.0043		
TE ↓	hold_rising to CP	-0.0001	-0.0001		
TE ↑	hold_rising to CP	-0.0098	-0.0098		

TE ↓	setup_rising to CP	0.0446	0.0446		
TE ↑	setup_rising to CP	0.0835	0.0835		
TI ↓	hold_rising to CP	-0.0377	-0.0377		
TI ↑	hold_rising to CP	-0.0092	-0.0092		
TI ↓	setup_rising to CP	0.0821	0.0821		
TI ↑	setup_rising to CP	0.0391	0.0391		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P16	3.626e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P16	3.536e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P16	3.650e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_P16	4.093e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_P16	5.290e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_P16	6.910e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

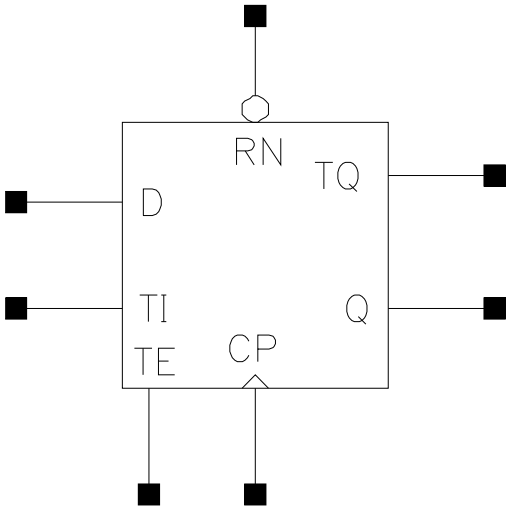
Pin Cycle	C8T28SOI_LL_SDFPRQNTX5_P16	C8T28SOI_LLHF_SDFPRQNTX3_P16	C8T28SOIDV_LL_SDFPRQNTX5_P16	C8T28SOIDV_LL_SDFPRQNTX10_P16
Clock 100Mhz Data 0Mhz	1.064e-02	1.017e-02	9.758e-03	9.540e-03
Clock 100Mhz Data 25Mhz	1.063e-02	1.021e-02	9.888e-03	1.018e-02
Clock 100Mhz Data 50Mhz	1.063e-02	1.026e-02	1.002e-02	1.083e-02
Clock = 0 Data 100Mhz	4.916e-03	5.217e-03	5.050e-03	4.960e-03
Clock = 1 Data 100Mhz	3.394e-05	6.616e-04	4.531e-04	3.488e-04
	C8T28SOIDV_LL_SDFPRQNTX19_P16	C8T28SOIDV_LL_SDFPRQNTX29_P16		
Clock 100Mhz Data 0Mhz	9.472e-03	9.417e-03		
Clock 100Mhz Data 25Mhz	1.108e-02	1.269e-02		
Clock 100Mhz Data 50Mhz	1.268e-02	1.597e-02		
Clock = 0 Data 100Mhz	4.906e-03	4.871e-03		
Clock = 1 Data 100Mhz	2.863e-04	2.446e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P16	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P16	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P16	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P16	C8T28SOI_LLHF_-SDFPRQTX3_P16	C8T28SOIDV_LL_-SDFPRQTX5_P16	C8T28SOIDV_LL_-SDFPRQTX10_P16
CP	0.0009	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
RN	0.0010	0.0009	0.0011	0.0010
TE	0.0012	0.0010	0.0011	0.0011
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P16	C8T28SOIDV_LL_-SDFPRQTX29_P16		
CP	0.0006	0.0006		
D	0.0006	0.0006		
RN	0.0010	0.0010		
TE	0.0011	0.0011		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQTX5_P16	**C8T28SOI_LLHF_-SDFPRQTX3_P16**	**C8T28SOI_LL_-SDFPRQTX5_P16**	**C8T28SOI_LLHF_-SDFPRQTX3_P16**
CP to Q ↓	0.0736	0.0626	3.4322	5.0334
CP to Q ↑	0.0603	0.0632	4.5619	6.8466
CP to TQ ↓	0.0826	0.0603	8.6251	5.5173
CP to TQ ↑	0.0744	0.0663	19.9459	11.3257
RN to Q ↓	0.0543	0.0483	3.2056	4.7872
RN to TQ ↓	0.0634	0.0463	8.2770	5.3176
	C8T28SOIDV_LL_-SDFPRQTX5_P16	**C8T28SOIDV_LL_-SDFPRQTX10_P16**	**C8T28SOIDV_LL_-SDFPRQTX5_P16**	**C8T28SOIDV_LL_-SDFPRQTX10_P16**
CP to Q ↓	0.0545	0.0729	3.1264	1.5083
CP to Q ↑	0.0665	0.0937	4.5180	2.2433
CP to TQ ↓	0.0544	0.0752	5.4335	5.2728
CP to TQ ↑	0.0686	0.0973	9.1766	9.1036
RN to Q ↓	0.0535	0.0688	2.9945	1.5080
RN to TQ ↓	0.0537	0.0711	5.2753	5.2733
	C8T28SOIDV_LL_-SDFPRQTX19_P16	**C8T28SOIDV_LL_-SDFPRQTX29_P16**	**C8T28SOIDV_LL_-SDFPRQTX19_P16**	**C8T28SOIDV_LL_-SDFPRQTX29_P16**
CP to Q ↓	0.0820	0.0794	0.7927	0.5300
CP to Q ↑	0.1006	0.1023	1.1395	0.7755
CP to TQ ↓	0.0850	0.0811	5.3364	5.2677
CP to TQ ↑	0.1057	0.1069	9.1059	9.3711
RN to Q ↓	0.0790	0.0760	0.7923	0.5304
RN to TQ ↓	0.0820	0.0777	5.3365	5.2684

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_-P16	C8T28SOI_-LLHF_-SDFPRQTX3_-P16	C8T28SOIDV_-LL_-SDFPRQTX5_-P16	C8T28SOIDV_-LL_-SDFPRQTX10_-P16
CP ↓	min_pulse_width to CP	0.0859	0.0808	0.0753	0.0753
CP ↑	min_pulse_width to CP	0.0597	0.0471	0.0455	0.0394
D ↓	hold_rising to CP	-0.0338	-0.0724	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0098	-0.0099	0.0009	0.0009
D ↓	setup_rising to CP	0.0711	0.1121	0.0467	0.0467
D ↑	setup_rising to CP	0.0337	0.0396	0.0272	0.0272
RN ↓	min_pulse_width to RN	0.0659	0.0615	0.0615	0.0496
RN ↑	recovery_rising to CP	0.0054	0.0028	0.0032	0.0032
RN ↑	removal_rising to CP	0.0042	0.0048	0.0042	0.0042
TE ↓	hold_rising to CP	-0.0263	-0.0279	-0.0055	-0.0050
TE ↑	hold_rising to CP	-0.0072	-0.0062	-0.0098	-0.0092
TE ↓	setup_rising to CP	0.0689	0.0877	0.0442	0.0442
TE ↑	setup_rising to CP	0.0862	0.1053	0.0835	0.0835
TI ↓	hold_rising to CP	-0.0475	-0.0703	-0.0433	-0.0426
TI ↑	hold_rising to CP	-0.0092	-0.0037	-0.0100	-0.0100
TI ↓	setup_rising to CP	0.0857	0.1041	0.0821	0.0806
TI ↑	setup_rising to CP	0.0332	0.0326	0.0391	0.0391
		C8T28SOIDV_-LL_-SDFPRQTX19_-P16	C8T28SOIDV_-LL_-SDFPRQTX29_-P16		
CP ↓	min_pulse_width to CP	0.0753	0.0753		
CP ↑	min_pulse_width to CP	0.0394	0.0394		
D ↓	hold_rising to CP	-0.0072	-0.0072		
D ↑	hold_rising to CP	0.0009	0.0009		
D ↓	setup_rising to CP	0.0467	0.0467		
D ↑	setup_rising to CP	0.0272	0.0272		
RN ↓	min_pulse_width to RN	0.0518	0.0518		
RN ↑	recovery_rising to CP	0.0032	0.0032		
RN ↑	removal_rising to CP	0.0042	0.0042		
TE ↓	hold_rising to CP	-0.0055	-0.0050		
TE ↑	hold_rising to CP	-0.0092	-0.0092		

TE ↓	setup_rising to CP	0.0442	0.0442		
TE ↑	setup_rising to CP	0.0835	0.0835		
TI ↓	hold_rising to CP	-0.0433	-0.0375		
TI ↑	hold_rising to CP	-0.0100	-0.0100		
TI ↓	setup_rising to CP	0.0821	0.0821		
TI ↑	setup_rising to CP	0.0391	0.0391		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P16	3.718e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P16	3.524e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P16	3.689e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P16	4.741e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P16	5.791e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P16	7.326e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

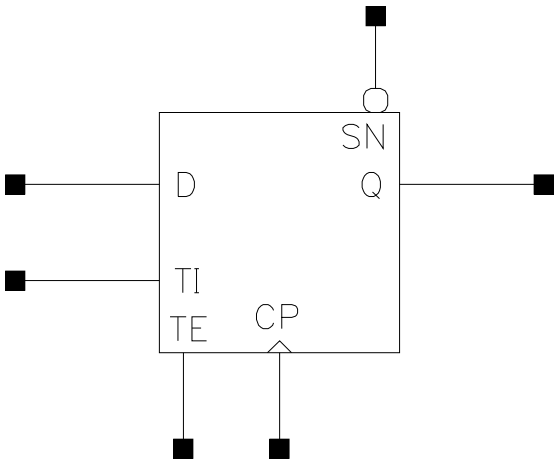
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P16	C8T28SOI_LLHF_-SDFPRQTX3_P16	C8T28SOIDV_LL_-SDFPRQTX5_P16	C8T28SOIDV_LL_-SDFPRQTX10_P16
Clock 100Mhz Data 0Mhz	1.065e-02	1.018e-02	9.748e-03	9.533e-03
Clock 100Mhz Data 25Mhz	1.081e-02	1.025e-02	9.874e-03	1.041e-02
Clock 100Mhz Data 50Mhz	1.098e-02	1.033e-02	1.000e-02	1.129e-02
Clock = 0 Data 100Mhz	4.921e-03	5.218e-03	5.043e-03	4.955e-03
Clock = 1 Data 100Mhz	3.383e-05	6.613e-04	4.528e-04	3.486e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P16	C8T28SOIDV_LL_-SDFPRQTX29_P16		
Clock 100Mhz Data 0Mhz	9.404e-03	9.319e-03		
Clock 100Mhz Data 25Mhz	1.127e-02	1.220e-02		
Clock 100Mhz Data 50Mhz	1.314e-02	1.507e-02		
Clock = 0 Data 100Mhz	4.903e-03	4.869e-03		
Clock = 1 Data 100Mhz	2.862e-04	2.446e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P16	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P16	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P16	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P16	C8T28SOI_LLHF_-SDFPSQX3_P16	C8T28SOIDV_LL_-SDFPSQX5_P16	C8T28SOIDV_LL_-SDFPSQX10_P16
CP	0.0009	0.0008	0.0006	0.0007
D	0.0003	0.0006	0.0004	0.0004
SN	0.0016	0.0015	0.0012	0.0012
TE	0.0012	0.0010	0.0011	0.0012
TI	0.0005	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQX14_P16	C8T28SOIDV_LL_-SDFPSQX19_P16	C8T28SOIDV_LL_-SDFPSQX29_P16	
CP	0.0007	0.0007	0.0007	
D	0.0004	0.0004	0.0004	
SN	0.0012	0.0012	0.0012	
TE	0.0012	0.0012	0.0012	
TI	0.0005	0.0005	0.0005	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P16	**C8T28SOI_LLHF_-SDFPSQX3_P16**	**C8T28SOI_LL_-SDFPSQX5_P16**	**C8T28SOI_LLHF_-SDFPSQX3_P16**
CP to Q ↓	0.0637	0.0562	3.2850	4.9330
CP to Q ↑	0.0567	0.0613	4.5489	6.6980
SN to Q ↑	0.0381	0.0356	4.4679	6.5908
	C8T28SOIDV_LL_-SDFPSQX5_P16	**C8T28SOIDV_LL_-SDFPSQX10_P16**	**C8T28SOIDV_LL_-SDFPSQX5_P16**	**C8T28SOIDV_LL_-SDFPSQX10_P16**
CP to Q ↓	0.0492	0.0716	3.0269	1.4547
CP to Q ↑	0.0611	0.0981	4.4732	2.2330
SN to Q ↑	0.0353	0.0695	4.4341	2.2328
	C8T28SOIDV_LL_-SDFPSQX14_P16	**C8T28SOIDV_LL_-SDFPSQX19_P16**	**C8T28SOIDV_LL_-SDFPSQX14_P16**	**C8T28SOIDV_LL_-SDFPSQX19_P16**
CP to Q ↓	0.0729	0.0779	1.0064	0.7802
CP to Q ↑	0.0987	0.1025	1.5005	1.1312
SN to Q ↑	0.0701	0.0740	1.5006	1.1304
	C8T28SOIDV_LL_-SDFPSQX29_P16		**C8T28SOIDV_LL_-SDFPSQX29_P16**	
CP to Q ↓	0.0780		0.5275	
CP to Q ↑	0.1079		0.7516	
SN to Q ↑	0.0791		0.7511	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P16	C8T28SOI_-LLHF_-SDFPSQX3_P16	C8T28SOIDV_-LL_SDFPSQX5_-P16	C8T28SOIDV_-LL_-SDFPSQX10_-P16
CP ↓	min_pulse_width to CP	0.0937	0.0902	0.0817	0.0800
CP ↑	min_pulse_width to CP	0.0551	0.0424	0.0408	0.0395
D ↓	hold_rising to CP	-0.0387	-0.0826	-0.0121	-0.0169
D ↑	hold_rising to CP	-0.0040	-0.0041	0.0009	0.0009
D ↓	setup_rising to CP	0.0786	0.1267	0.0564	0.0591
D ↑	setup_rising to CP	0.0347	0.0337	0.0298	0.0272

SN ↓	min_pulse_width to SN	0.0452	0.0403	0.0403	0.0403
SN ↑	recovery_rising to CP	0.0032	0.0052	-0.0017	-0.0043
SN ↑	removal_rising to CP	0.0212	0.0261	0.0309	0.0335
TE ↓	hold_rising to CP	-0.0240	-0.0230	-0.0099	-0.0147
TE ↑	hold_rising to CP	-0.0044	-0.0046	0.0031	-0.0044
TE ↓	setup_rising to CP	0.0733	0.0969	0.0543	0.0539
TE ↑	setup_rising to CP	0.0933	0.1204	0.0862	0.0835
TI ↓	hold_rising to CP	-0.0517	-0.0807	-0.0426	-0.0377
TI ↑	hold_rising to CP	-0.0036	-0.0029	0.0028	-0.0036
TI ↓	setup_rising to CP	0.0919	0.1145	0.0821	0.0808
TI ↑	setup_rising to CP	0.0342	0.0286	0.0280	0.0342
		C8T28SOIDV_-LL_-SDFPSQX14_-P16	C8T28SOIDV_-LL_-SDFPSQX19_-P16	C8T28SOIDV_-LL_-SDFPSQX29_-P16	
CP ↓	min_pulse_width to CP	0.0800	0.0800	0.0800	
CP ↑	min_pulse_width to CP	0.0395	0.0395	0.0395	
D ↓	hold_rising to CP	-0.0169	-0.0169	-0.0169	
D ↑	hold_rising to CP	0.0009	0.0009	0.0009	
D ↓	setup_rising to CP	0.0591	0.0591	0.0591	
D ↑	setup_rising to CP	0.0272	0.0272	0.0272	
SN ↓	min_pulse_width to SN	0.0403	0.0403	0.0403	
SN ↑	recovery_rising to CP	-0.0043	-0.0043	-0.0043	
SN ↑	removal_rising to CP	0.0335	0.0335	0.0335	
TE ↓	hold_rising to CP	-0.0147	-0.0147	-0.0147	
TE ↑	hold_rising to CP	-0.0044	-0.0044	-0.0044	
TE ↓	setup_rising to CP	0.0539	0.0539	0.0539	
TE ↑	setup_rising to CP	0.0835	0.0835	0.0835	
TI ↓	hold_rising to CP	-0.0377	-0.0377	-0.0377	
TI ↑	hold_rising to CP	-0.0036	-0.0036	-0.0036	
TI ↓	setup_rising to CP	0.0808	0.0808	0.0808	
TI ↑	setup_rising to CP	0.0342	0.0342	0.0342	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds

C8T28SOI_LL_SDFPSQX5_P16	3.657e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQX3_P16	3.425e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P16	3.536e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P16	4.656e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P16	5.132e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P16	5.684e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P16	6.975e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

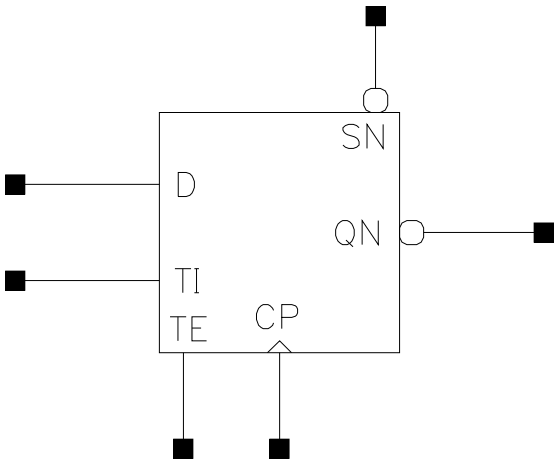
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P16	C8T28SOI_LLHF_-SDFPSQX3_P16	C8T28SOIDV_LL_-SDFPSQX5_P16	C8T28SOIDV_LL_-SDFPSQX10_P16
Clock 100Mhz Data 0Mhz	1.049e-02	9.926e-03	9.547e-03	9.341e-03
Clock 100Mhz Data 25Mhz	1.042e-02	9.824e-03	9.402e-03	1.006e-02
Clock 100Mhz Data 50Mhz	1.035e-02	9.723e-03	9.257e-03	1.079e-02
Clock = 0 Data 100Mhz	5.051e-03	5.348e-03	5.223e-03	5.187e-03
Clock = 1 Data 100Mhz	3.383e-05	6.547e-04	4.488e-04	3.460e-04
	C8T28SOIDV_LL_-SDFPSQX14_P16	C8T28SOIDV_LL_-SDFPSQX19_P16	C8T28SOIDV_LL_-SDFPSQX29_P16	
Clock 100Mhz Data 0Mhz	9.218e-03	9.136e-03	9.077e-03	
Clock 100Mhz Data 25Mhz	1.033e-02	1.089e-02	1.174e-02	
Clock 100Mhz Data 50Mhz	1.144e-02	1.265e-02	1.440e-02	
Clock = 0 Data 100Mhz	5.165e-03	5.151e-03	5.140e-03	
Clock = 1 Data 100Mhz	2.844e-04	2.433e-04	2.140e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P16	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P16	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P16	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P16	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P16	C8T28SOI_LLHF_-SDFPSQNX3_P16	C8T28SOIDV_LL_-SDFPSQNX5_P16	C8T28SOIDV_LL_-SDFPSQNX10_P16
CP	0.0009	0.0008	0.0006	0.0006
D	0.0003	0.0006	0.0004	0.0004
SN	0.0016	0.0015	0.0012	0.0013
TE	0.0012	0.0010	0.0011	0.0011
TI	0.0005	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQNX14_P16	C8T28SOIDV_LL_-SDFPSQNX19_P16	C8T28SOIDV_LL_-SDFPSQNX23_P16	C8T28SOIDV_LL_-SDFPSQNX29_P16
CP	0.0006	0.0006	0.0006	0.0006
D	0.0004	0.0004	0.0004	0.0004
SN	0.0013	0.0013	0.0013	0.0012
TE	0.0011	0.0011	0.0011	0.0011
TI	0.0005	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPSQNX5_P16	**C8T28SOI_LLHF_-SDFPSQNX3_P16**	**C8T28SOI_LL_-SDFPSQNX5_P16**	**C8T28SOI_LLHF_-SDFPSQNX3_P16**
CP to QN ↓	0.0760	0.0760	3.2298	4.5382
CP to QN ↑	0.0686	0.0636	4.7151	6.5710
SN to QN ↓	0.0575	0.0505	3.2318	4.5454
	C8T28SOIDV_LL_-SDFPSQNX5_P16	**C8T28SOIDV_LL_-SDFPSQNX10_P16**	**C8T28SOIDV_LL_-SDFPSQNX5_P16**	**C8T28SOIDV_LL_-SDFPSQNX10_P16**
CP to QN ↓	0.0815	0.0776	2.9127	1.4921
CP to QN ↑	0.0643	0.0671	4.4271	2.2179
SN to QN ↓	0.0544	0.0480	2.9162	1.4888
	C8T28SOIDV_LL_-SDFPSQNX14_P16	**C8T28SOIDV_LL_-SDFPSQNX19_P16**	**C8T28SOIDV_LL_-SDFPSQNX14_P16**	**C8T28SOIDV_LL_-SDFPSQNX19_P16**
CP to QN ↓	0.0810	0.0839	0.9877	0.7541
CP to QN ↑	0.0696	0.0725	1.4889	1.1203
SN to QN ↓	0.0503	0.0536	0.9866	0.7532
	C8T28SOIDV_LL_-SDFPSQNX23_P16	**C8T28SOIDV_LL_-SDFPSQNX29_P16**	**C8T28SOIDV_LL_-SDFPSQNX23_P16**	**C8T28SOIDV_LL_-SDFPSQNX29_P16**
CP to QN ↓	0.0851	0.0822	0.6063	0.5214
CP to QN ↑	0.0720	0.0736	1.1152	0.7504
SN to QN ↓	0.0545	0.0527	0.6058	0.5205

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P16	C8T28SOI_-LLHF_-SDFPSQNX3_-P16	C8T28SOIDV_-LL_-SDFPSQNX5_-P16	C8T28SOIDV_-LL_-SDFPSQNX10_-P16
CP ↓	min_pulse_width to CP	0.0937	0.0902	0.0817	0.0841
CP ↑	min_pulse_width to CP	0.0409	0.0364	0.0394	0.0440
D ↓	hold_rising to CP	-0.0414	-0.0822	-0.0121	-0.0121
D ↑	hold_rising to CP	-0.0040	-0.0041	0.0009	0.0009
D ↓	setup_rising to CP	0.0754	0.1267	0.0564	0.0564

D ↑	setup_rising to CP	0.0347	0.0337	0.0298	0.0239
SN ↓	min_pulse_width to SN	0.0425	0.0376	0.0381	0.0403
SN ↑	recovery_rising to CP	0.0032	0.0031	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0212	0.0261	0.0309	0.0335
TE ↓	hold_rising to CP	-0.0234	-0.0230	-0.0099	-0.0099
TE ↑	hold_rising to CP	-0.0044	-0.0046	0.0031	0.0031
TE ↓	setup_rising to CP	0.0733	0.0969	0.0543	0.0543
TE ↑	setup_rising to CP	0.0933	0.1204	0.0862	0.0862
TI ↓	hold_rising to CP	-0.0560	-0.0807	-0.0426	-0.0411
TI ↑	hold_rising to CP	-0.0036	-0.0029	0.0028	0.0028
TI ↓	setup_rising to CP	0.0919	0.1145	0.0821	0.0821
TI ↑	setup_rising to CP	0.0342	0.0286	0.0280	0.0280
		C8T28SOIDV_-LL_-SDFPSQNX14_-P16	C8T28SOIDV_-LL_-SDFPSQNX19_-P16	C8T28SOIDV_-LL_-SDFPSQNX23_-P16	C8T28SOIDV_-LL_-SDFPSQNX29_-P16
CP ↓	min_pulse_width to CP	0.0841	0.0841	0.0841	0.0817
CP ↑	min_pulse_width to CP	0.0440	0.0454	0.0454	0.0454
D ↓	hold_rising to CP	-0.0121	-0.0121	-0.0121	-0.0121
D ↑	hold_rising to CP	0.0009	0.0009	0.0009	0.0009
D ↓	setup_rising to CP	0.0564	0.0564	0.0564	0.0564
D ↑	setup_rising to CP	0.0239	0.0239	0.0239	0.0298
SN ↓	min_pulse_width to SN	0.0403	0.0403	0.0430	0.0452
SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0335	0.0335	0.0335	0.0309
TE ↓	hold_rising to CP	-0.0099	-0.0099	-0.0099	-0.0099
TE ↑	hold_rising to CP	0.0031	0.0031	0.0031	0.0031
TE ↓	setup_rising to CP	0.0543	0.0543	0.0543	0.0543
TE ↑	setup_rising to CP	0.0862	0.0862	0.0862	0.0884
TI ↓	hold_rising to CP	-0.0411	-0.0411	-0.0411	-0.0426
TI ↑	hold_rising to CP	0.0028	0.0028	0.0028	0.0028
TI ↓	setup_rising to CP	0.0821	0.0821	0.0821	0.0863
TI ↑	setup_rising to CP	0.0280	0.0280	0.0280	0.0280

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P16	3.674e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P16	3.425e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P16	3.620e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P16	4.757e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P16	5.255e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P16	5.897e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P16	6.124e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P16	7.366e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

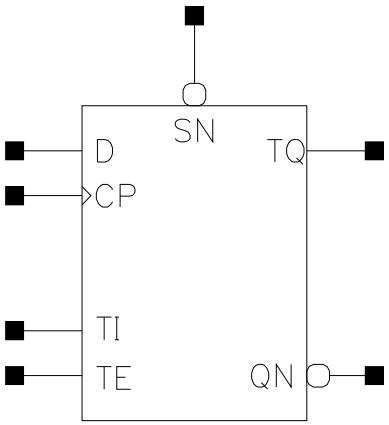
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P16	C8T28SOI_LLHF_-SDFPSQNX3_P16	C8T28SOIDV_LL_-SDFPSQNX5_P16	C8T28SOIDV_LL_-SDFPSQNX10_P16
Clock 100Mhz Data 0Mhz	1.047e-02	9.915e-03	9.536e-03	9.434e-03
Clock 100Mhz Data 25Mhz	1.023e-02	9.733e-03	9.516e-03	1.022e-02
Clock 100Mhz Data 50Mhz	9.986e-03	9.551e-03	9.496e-03	1.101e-02
Clock = 0 Data 100Mhz	5.053e-03	5.353e-03	5.227e-03	5.159e-03
Clock = 1 Data 100Mhz	3.371e-05	6.559e-04	4.496e-04	3.464e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P16	C8T28SOIDV_LL_-SDFPSQNX19_P16	C8T28SOIDV_LL_-SDFPSQNX23_P16	C8T28SOIDV_LL_-SDFPSQNX29_P16
Clock 100Mhz Data 0Mhz	9.371e-03	9.331e-03	9.302e-03	9.242e-03
Clock 100Mhz Data 25Mhz	1.056e-02	1.100e-02	1.114e-02	1.194e-02
Clock 100Mhz Data 50Mhz	1.175e-02	1.267e-02	1.298e-02	1.464e-02
Clock = 0 Data 100Mhz	5.119e-03	5.093e-03	5.073e-03	5.063e-03
Clock = 1 Data 100Mhz	2.846e-04	2.434e-04	2.139e-04	1.919e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P16	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P16	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P16	C8T28SOI_LLHF_-SDFPSQNTX3_P16	C8T28SOIDV_LL_-SDFPSQNTX5_P16	C8T28SOIDV_LL_-SDFPSQNTX10_P16
CP	0.0009	0.0008	0.0006	0.0006
D	0.0003	0.0006	0.0004	0.0004
SN	0.0016	0.0015	0.0012	0.0012
TE	0.0012	0.0010	0.0011	0.0011
TI	0.0005	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQNTX19_P16	C8T28SOIDV_LL_-SDFPSQNTX23_P16	C8T28SOIDV_LL_-SDFPSQNTX29_P16	
CP	0.0006	0.0006	0.0006	
D	0.0004	0.0004	0.0004	
SN	0.0012	0.0012	0.0012	
TE	0.0011	0.0011	0.0011	
TI	0.0005	0.0005	0.0005	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P16	**C8T28SOI_LLHF_-SDFPSQNTX3_P16**	**C8T28SOI_LL_-SDFPSQNTX5_P16**	**C8T28SOI_LLHF_-SDFPSQNTX3_P16**
CP to QN ↓	0.0836	0.0819	3.2775	4.5824
CP to QN ↑	0.0816	0.0754	4.6537	6.5898
CP to TQ ↓	0.0657	0.0533	8.0925	5.3868
CP to TQ ↑	0.0680	0.0631	19.8816	11.1734
SN to QN ↓	0.0606	0.0533	3.2872	4.5982
SN to TQ ↑	0.0474	0.0370	19.8192	11.1145
	C8T28SOIDV_LL_-SDFPSQNTX5_P16	**C8T28SOIDV_LL_-SDFPSQNTX10_P16**	**C8T28SOIDV_LL_-SDFPSQNTX5_P16**	**C8T28SOIDV_LL_-SDFPSQNTX10_P16**
CP to QN ↓	0.0825	0.0789	2.9629	1.4825
CP to QN ↑	0.0674	0.0722	4.4241	2.2259
CP to TQ ↓	0.0470	0.0547	5.3315	5.4240
CP to TQ ↑	0.0618	0.0654	9.7260	9.8021
SN to QN ↓	0.0540	0.0504	2.9760	1.4819
SN to TQ ↑	0.0353	0.0377	9.6834	9.7148
	C8T28SOIDV_LL_-SDFPSQNTX19_P16	**C8T28SOIDV_LL_-SDFPSQNTX23_P16**	**C8T28SOIDV_LL_-SDFPSQNTX19_P16**	**C8T28SOIDV_LL_-SDFPSQNTX23_P16**
CP to QN ↓	0.0847	0.0869	0.7482	0.6040
CP to QN ↑	0.0777	0.0767	1.1225	1.1147
CP to TQ ↓	0.0546	0.0554	5.4172	5.4619
CP to TQ ↑	0.0655	0.0663	9.8007	9.8127
SN to QN ↓	0.0556	0.0572	0.7482	0.6040
SN to TQ ↑	0.0378	0.0383	9.7191	9.7268
	C8T28SOIDV_LL_-SDFPSQNTX29_P16		**C8T28SOIDV_LL_-SDFPSQNTX29_P16**	
CP to QN ↓	0.0864		0.5221	
CP to QN ↑	0.0795		0.7500	

CP to TQ ↓	0.0582		5.5805	
CP to TQ ↑	0.0707		11.1479	
SN to QN ↓	0.0554		0.5215	
SN to TQ ↑	0.0409		11.0287	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P16	C8T28SOI_-LLHF_-SDFPSQNTX3_-P16	C8T28SOIDV_-LL_-SDFPSQNTX5_-P16	C8T28SOIDV_-LL_SDFP-SQNTX10_P16
CP ↓	min_pulse_width to CP	0.0937	0.0902	0.0817	0.0817
CP ↑	min_pulse_width to CP	0.0516	0.0457	0.0408	0.0454
D ↓	hold_rising to CP	-0.0414	-0.0826	-0.0121	-0.0121
D ↑	hold_rising to CP	-0.0040	-0.0041	0.0009	0.0009
D ↓	setup_rising to CP	0.0808	0.1267	0.0564	0.0564
D ↑	setup_rising to CP	0.0347	0.0337	0.0298	0.0272
SN ↓	min_pulse_width to SN	0.0474	0.0403	0.0403	0.0403
SN ↑	recovery_rising to CP	0.0052	0.0058	-0.0017	-0.0017
SN ↑	removal_rising to CP	0.0212	0.0261	0.0309	0.0309
TE ↓	hold_rising to CP	-0.0240	-0.0230	-0.0099	-0.0099
TE ↑	hold_rising to CP	-0.0044	-0.0046	0.0031	0.0031
TE ↓	setup_rising to CP	0.0787	0.0969	0.0543	0.0543
TE ↑	setup_rising to CP	0.0960	0.1204	0.0862	0.0884
TI ↓	hold_rising to CP	-0.0560	-0.0807	-0.0426	-0.0426
TI ↑	hold_rising to CP	-0.0036	-0.0029	0.0028	0.0028
TI ↓	setup_rising to CP	0.0954	0.1145	0.0821	0.0863
TI ↑	setup_rising to CP	0.0342	0.0286	0.0280	0.0280
		C8T28SOIDV_-LL_SDFP-SQNTX19_P16	C8T28SOIDV_-LL_SDFP-SQNTX23_P16	C8T28SOIDV_-LL_SDFP-SQNTX29_P16	
CP ↓	min_pulse_width to CP	0.0817	0.0817	0.0817	
CP ↑	min_pulse_width to CP	0.0487	0.0487	0.0500	
D ↓	hold_rising to CP	-0.0121	-0.0121	-0.0121	
D ↑	hold_rising to CP	0.0009	0.0009	0.0009	
D ↓	setup_rising to CP	0.0564	0.0564	0.0564	
D ↑	setup_rising to CP	0.0298	0.0298	0.0298	
SN ↓	min_pulse_width to SN	0.0430	0.0430	0.0479	

SN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	
SN ↑	removal_rising to CP	0.0309	0.0309	0.0309	
TE ↓	hold_rising to CP	-0.0099	-0.0099	-0.0099	
TE ↑	hold_rising to CP	0.0031	0.0031	0.0031	
TE ↓	setup_rising to CP	0.0543	0.0543	0.0543	
TE ↑	setup_rising to CP	0.0884	0.0884	0.0884	
TI ↓	hold_rising to CP	-0.0426	-0.0426	-0.0426	
TI ↑	hold_rising to CP	0.0028	0.0028	0.0028	
TI ↓	setup_rising to CP	0.0863	0.0863	0.0856	
TI ↑	setup_rising to CP	0.0280	0.0280	0.0280	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P16	3.720e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P16	3.665e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P16	3.890e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_-P16	5.009e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_-P16	6.176e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_-P16	6.429e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_-P16	7.594e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P16	C8T28SOI_LLHF_-SDFPSQNTX3_P16	C8T28SOIDV_LL_-SDFPSQNTX5_P16	C8T28SOIDV_LL_-SDFPSQNTX10_P16
Clock 100Mhz Data 0Mhz	1.017e-02	9.764e-03	9.440e-03	9.279e-03
Clock 100Mhz Data 25Mhz	1.037e-02	9.961e-03	9.620e-03	1.036e-02
Clock 100Mhz Data 50Mhz	1.058e-02	1.016e-02	9.800e-03	1.144e-02
Clock = 0 Data 100Mhz	5.045e-03	5.346e-03	5.221e-03	5.159e-03
Clock = 1 Data 100Mhz	3.395e-05	6.549e-04	4.489e-04	3.460e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P16	C8T28SOIDV_LL_-SDFPSQNTX23_P16	C8T28SOIDV_LL_-SDFPSQNTX29_P16	
Clock 100Mhz Data 0Mhz	9.182e-03	9.118e-03	9.073e-03	
Clock 100Mhz Data 25Mhz	1.113e-02	1.130e-02	1.216e-02	
Clock 100Mhz Data 50Mhz	1.308e-02	1.348e-02	1.525e-02	

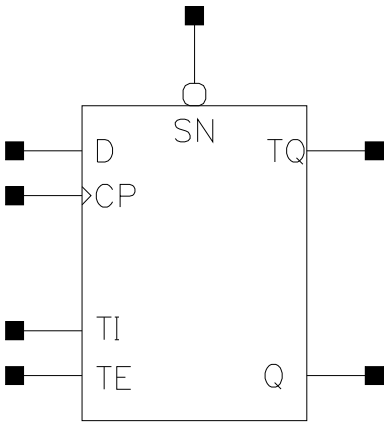
Clock = 0 Data 100Mhz	5.122e-03	5.097e-03	5.082e-03	
Clock = 1 Data 100Mhz	2.843e-04	2.431e-04	2.138e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P16	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P16	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P16	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P16	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P16	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P16	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P16	C8T28SOI_LLHF_-SDFPSQTX3_P16	C8T28SOIDV_LL_-SDFPSQTX5_P16	C8T28SOIDV_LL_-SDFPSQTX10_P16
CP	0.0009	0.0008	0.0006	0.0007
D	0.0003	0.0006	0.0004	0.0004
SN	0.0016	0.0015	0.0012	0.0012
TE	0.0012	0.0010	0.0011	0.0012
TI	0.0005	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQTX19_P16	C8T28SOIDV_LL_-SDFPSQTX29_P16		
CP	0.0007	0.0007		
D	0.0004	0.0004		
SN	0.0012	0.0012		
TE	0.0012	0.0012		
TI	0.0005	0.0005		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQTX5_P16	**C8T28SOI_LLHF_-SDFPSQTX3_P16**	**C8T28SOI_LL_-SDFPSQTX5_P16**	**C8T28SOI_LLHF_-SDFPSQTX3_P16**
CP to Q ↓	0.0711	0.0632	3.4564	5.0863
CP to Q ↑	0.0607	0.0643	4.5630	6.8535
CP to TQ ↓	0.0800	0.0607	8.5728	5.5590
CP to TQ ↑	0.0750	0.0674	19.9123	11.3373
SN to Q ↑	0.0395	0.0371	4.4726	6.7377
SN to TQ ↑	0.0506	0.0391	19.8364	11.2513
	C8T28SOIDV_LL_-SDFPSQTX5_P16	**C8T28SOIDV_LL_-SDFPSQTX10_P16**	**C8T28SOIDV_LL_-SDFPSQTX5_P16**	**C8T28SOIDV_LL_-SDFPSQTX10_P16**
CP to Q ↓	0.0551	0.0714	3.1190	1.4968
CP to Q ↑	0.0642	0.0976	4.5331	2.2518
CP to TQ ↓	0.0552	0.0733	5.4329	5.4935
CP to TQ ↑	0.0657	0.1013	9.8407	9.7438
SN to Q ↑	0.0372	0.0690	4.4860	2.2525
SN to TQ ↑	0.0378	0.0727	9.7700	9.7457
	C8T28SOIDV_LL_-SDFPSQTX19_P16	**C8T28SOIDV_LL_-SDFPSQTX29_P16**	**C8T28SOIDV_LL_-SDFPSQTX19_P16**	**C8T28SOIDV_LL_-SDFPSQTX29_P16**
CP to Q ↓	0.0781	0.0876	0.7764	0.5153
CP to Q ↑	0.1034	0.1128	1.1524	0.7641
CP to TQ ↓	0.0780	0.0471	4.7472	4.8979
CP to TQ ↑	0.1079	0.0671	11.0566	11.1340
SN to Q ↑	0.0748	0.0813	1.1532	0.7654
SN to TQ ↑	0.0793	0.0385	11.0535	11.0942

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_-P16	C8T28SOI_-LLHF_-SDFPSQTX3_-P16	C8T28SOIDV_-LL_-SDFPSQTX5_-P16	C8T28SOIDV_-LL_-SDFPSQTX10_-P16
CP ↓	min_pulse_width to CP	0.0937	0.0902	0.0817	0.0818
CP ↑	min_pulse_width to CP	0.0598	0.0505	0.0455	0.0395
D ↓	hold_rising to CP	-0.0414	-0.0826	-0.0121	-0.0169
D ↑	hold_rising to CP	-0.0040	-0.0041	0.0009	0.0009
D ↓	setup_rising to CP	0.0808	0.1267	0.0564	0.0613
D ↑	setup_rising to CP	0.0347	0.0337	0.0239	0.0298
SN ↓	min_pulse_width to SN	0.0500	0.0403	0.0403	0.0403
SN ↑	recovery_rising to CP	0.0080	0.0080	-0.0017	-0.0043
SN ↑	removal_rising to CP	0.0212	0.0261	0.0309	0.0335
TE ↓	hold_rising to CP	-0.0240	-0.0230	-0.0099	-0.0147
TE ↑	hold_rising to CP	-0.0044	-0.0046	0.0031	-0.0044
TE ↓	setup_rising to CP	0.0787	0.0969	0.0543	0.0539
TE ↑	setup_rising to CP	0.0960	0.1204	0.0888	0.0835
TI ↓	hold_rising to CP	-0.0560	-0.0807	-0.0426	-0.0377
TI ↑	hold_rising to CP	-0.0036	-0.0029	0.0028	-0.0036
TI ↓	setup_rising to CP	0.0954	0.1145	0.0821	0.0808
TI ↑	setup_rising to CP	0.0342	0.0286	0.0280	0.0342
		C8T28SOIDV_-LL_-SDFPSQTX19_-P16	C8T28SOIDV_-LL_-SDFPSQTX29_-P16		
CP ↓	min_pulse_width to CP	0.0800	0.0800		
CP ↑	min_pulse_width to CP	0.0395	0.0455		
D ↓	hold_rising to CP	-0.0169	-0.0169		
D ↑	hold_rising to CP	0.0009	0.0009		
D ↓	setup_rising to CP	0.0591	0.0591		
D ↑	setup_rising to CP	0.0272	0.0272		
SN ↓	min_pulse_width to SN	0.0403	0.0479		
SN ↑	recovery_rising to CP	-0.0043	-0.0017		
SN ↑	removal_rising to CP	0.0335	0.0335		
TE ↓	hold_rising to CP	-0.0147	-0.0147		
TE ↑	hold_rising to CP	-0.0044	-0.0044		

TE ↓	setup_rising to CP	0.0539	0.0539		
TE ↑	setup_rising to CP	0.0835	0.0835		
TI ↓	hold_rising to CP	-0.0377	-0.0377		
TI ↑	hold_rising to CP	-0.0036	-0.0036		
TI ↓	setup_rising to CP	0.0808	0.0808		
TI ↑	setup_rising to CP	0.0342	0.0342		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P16	3.702e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P16	3.660e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P16	3.834e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P16	4.880e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P16	5.868e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P16	7.352e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

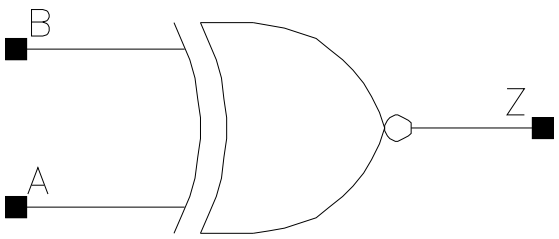
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P16	C8T28SOI_LLHF_-SDFPSQTX3_P16	C8T28SOIDV_LL_-SDFPSQTX5_P16	C8T28SOIDV_LL_-SDFPSQTX10_P16
Clock 100Mhz Data 0Mhz	1.018e-02	9.773e-03	9.449e-03	9.268e-03
Clock 100Mhz Data 25Mhz	1.052e-02	1.004e-02	9.683e-03	1.020e-02
Clock 100Mhz Data 50Mhz	1.086e-02	1.030e-02	9.917e-03	1.113e-02
Clock = 0 Data 100Mhz	5.046e-03	5.347e-03	5.221e-03	5.199e-03
Clock = 1 Data 100Mhz	3.384e-05	6.549e-04	4.489e-04	3.462e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P16	C8T28SOIDV_LL_-SDFPSQTX29_P16		
Clock 100Mhz Data 0Mhz	9.159e-03	9.088e-03		
Clock 100Mhz Data 25Mhz	1.107e-02	1.204e-02		
Clock 100Mhz Data 50Mhz	1.298e-02	1.499e-02		
Clock = 0 Data 100Mhz	5.175e-03	5.158e-03		
Clock = 1 Data 100Mhz	2.846e-04	2.435e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.600	0.544	0.8704
X5_P16	0.800	1.496	1.1968
X8_P16	1.600	1.088	1.7408
X9_P16	0.800	1.632	1.3056
X11_P16	1.600	1.360	2.1760
X14_P16	0.800	2.312	1.8496
X15_P16	1.600	1.904	3.0464
X19_P16	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P16	X5_P16	X8_P16	X9_P16
A	0.0013	0.0006	0.0020	0.0008
B	0.0011	0.0011	0.0016	0.0014
	X11_P16	X14_P16	X15_P16	X19_P16
A	0.0031	0.0012	0.0036	0.0014
B	0.0026	0.0019	0.0031	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X5_P16	X4_P16	X5_P16
A to Z ↓	0.0169	0.0463	4.0003	3.1380
A to Z ↑	0.0188	0.0423	6.1090	4.7807
B to Z ↓	0.0156	0.0338	4.0000	3.1212
B to Z ↑	0.0202	0.0319	6.1218	4.7770

	X8_P16	X9_P16	X8_P16	X9_P16
A to Z ↓	0.0203	0.0442	2.1119	1.6142
A to Z ↑	0.0230	0.0412	3.2515	2.4358
B to Z ↓	0.0192	0.0331	2.1103	1.6104
B to Z ↑	0.0237	0.0318	3.2572	2.4373
	X11_P16	**X14_P16**	**X11_P16**	**X14_P16**
A to Z ↓	0.0191	0.0418	1.4766	1.0972
A to Z ↑	0.0211	0.0383	2.1205	1.5731
B to Z ↓	0.0173	0.0310	1.4757	1.0934
B to Z ↑	0.0215	0.0297	2.1258	1.5715
	X15_P16	**X19_P16**	**X15_P16**	**X19_P16**
A to Z ↓	0.0210	0.0393	1.1207	0.8170
A to Z ↑	0.0233	0.0370	1.6162	1.1716
B to Z ↓	0.0192	0.0300	1.1192	0.8139
B to Z ↑	0.0238	0.0291	1.6196	1.1704

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P16	1.681e-05	1.000e-20
X5_P16	1.867e-05	1.000e-20
X8_P16	2.710e-05	1.000e-20
X9_P16	2.984e-05	1.000e-20
X11_P16	4.135e-05	1.000e-20
X14_P16	4.600e-05	1.000e-20
X15_P16	5.232e-05	1.000e-20
X19_P16	6.276e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P16	X5_P16	X8_P16	X9_P16
A to Z	2.431e-03	5.028e-03	4.683e-03	7.342e-03
B to Z	2.380e-03	4.041e-03	4.641e-03	6.012e-03
	X11_P16	X14_P16	X15_P16	X19_P16
A to Z	6.784e-03	1.154e-02	9.106e-03	1.416e-02
B to Z	6.627e-03	9.233e-03	8.941e-03	1.159e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

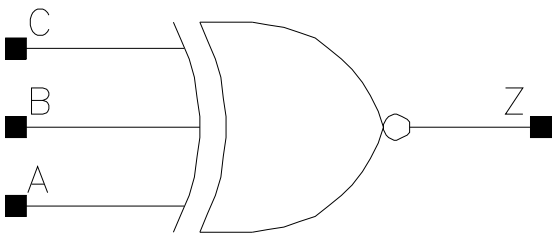
Pin Cycle (vdds)	X4_P16	X5_P16	X8_P16	X9_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P16	X14_P16	X15_P16	X19_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P16	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P16	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P16	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P16	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P16	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P16	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P16	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P16	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P16	C8T28SOIDV_LL_-XNOR3X4_P16	C8T28SOIDV_LL_-XNOR3X9_P16	C8T28SOIDV_LL_-XNOR3X13_P16
A	0.0019	0.0019	0.0024	0.0032
B	0.0018	0.0017	0.0022	0.0030
C	0.0008	0.0007	0.0007	0.0007
	C8T28SOIDV_LLS_-XNOR3X1_P16	C8T28SOIDV_LLS_-XNOR3X2_P16	C8T28SOIDV_LLS_-XNOR3X5_P16	C8T28SOIDV_LLS_-XNOR3X7_P16

A	0.0018	0.0021	0.0045	0.0069
B	0.0018	0.0021	0.0041	0.0064
C	0.0012	0.0015	0.0029	0.0044

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XNOR3X2_P16	**C8T28SOIDV_LL_-XNOR3X4_P16**	**C8T28SOIDV_LL_-XNOR3X2_P16**	**C8T28SOIDV_LL_-XNOR3X4_P16**
A to Z ↓	0.0469	0.0505	6.1235	3.3944
A to Z ↑	0.0448	0.0462	8.4835	4.8414
B to Z ↓	0.0476	0.0514	6.1244	3.3941
B to Z ↑	0.0457	0.0472	8.4900	4.8434
C to Z ↓	0.0652	0.0698	6.1187	3.3926
C to Z ↑	0.0633	0.0655	8.4847	4.8407
	C8T28SOIDV_LL_-XNOR3X9_P16	**C8T28SOIDV_LL_-XNOR3X13_P16**	**C8T28SOIDV_LL_-XNOR3X9_P16**	**C8T28SOIDV_LL_-XNOR3X13_P16**
A to Z ↓	0.0447	0.0504	1.7080	1.1697
A to Z ↑	0.0468	0.0533	2.3743	1.6458
B to Z ↓	0.0456	0.0514	1.7078	1.1697
B to Z ↑	0.0480	0.0548	2.3750	1.6474
C to Z ↓	0.0663	0.0784	1.7074	1.1693
C to Z ↑	0.0683	0.0821	2.3747	1.6470
	C8T28SOIDV_LLS_-XNOR3X1_P16	**C8T28SOIDV_LLS_-XNOR3X2_P16**	**C8T28SOIDV_LLS_-XNOR3X1_P16**	**C8T28SOIDV_LLS_-XNOR3X2_P16**
A to Z ↓	0.0284	0.0320	10.5797	6.0427
A to Z ↑	0.0297	0.0296	16.9948	9.2001
B to Z ↓	0.0294	0.0332	10.5944	6.0466
B to Z ↑	0.0306	0.0307	16.9848	9.1951
C to Z ↓	0.0286	0.0318	10.6196	6.0680
C to Z ↑	0.0300	0.0295	16.9891	9.2028
	C8T28SOIDV_LLS_-XNOR3X5_P16	**C8T28SOIDV_LLS_-XNOR3X7_P16**	**C8T28SOIDV_LLS_-XNOR3X5_P16**	**C8T28SOIDV_LLS_-XNOR3X7_P16**
A to Z ↓	0.0331	0.0287	2.9232	2.0204
A to Z ↑	0.0320	0.0279	4.5470	3.0440
B to Z ↓	0.0330	0.0280	2.9287	2.0259
B to Z ↑	0.0319	0.0275	4.5454	3.0441
C to Z ↓	0.0316	0.0274	2.9303	2.0288
C to Z ↑	0.0305	0.0265	4.5424	3.0437

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P16	1.489e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P16	1.715e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P16	2.865e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P16	4.028e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P16	1.030e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P16	1.640e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P16	3.762e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P16	5.769e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P16	C8T28SOIDV_LL_-XNOR3X4_P16	C8T28SOIDV_LL_-XNOR3X9_P16	C8T28SOIDV_LL_-XNOR3X13_P16
A to Z	3.101e-03	3.792e-03	5.915e-03	9.698e-03
B to Z	3.073e-03	3.767e-03	5.943e-03	9.751e-03
C to Z	4.930e-03	5.680e-03	8.341e-03	1.336e-02
	C8T28SOIDV_LLS_-XNOR3X1_P16	C8T28SOIDV_LLS_-XNOR3X2_P16	C8T28SOIDV_LLS_-XNOR3X5_P16	C8T28SOIDV_LLS_-XNOR3X7_P16
A to Z	1.835e-03	2.695e-03	5.873e-03	8.150e-03
B to Z	1.818e-03	2.731e-03	5.951e-03	8.073e-03
C to Z	1.783e-03	2.698e-03	5.827e-03	7.969e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

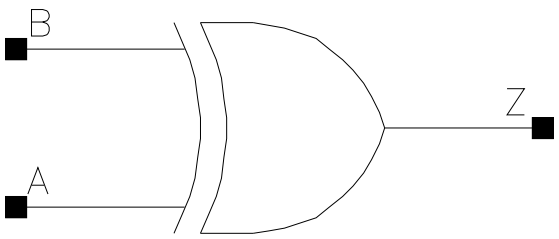
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P16	C8T28SOIDV_LL_-XNOR3X4_P16	C8T28SOIDV_LL_-XNOR3X9_P16	C8T28SOIDV_LL_-XNOR3X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P16	C8T28SOIDV_LLS_-XNOR3X2_P16	C8T28SOIDV_LLS_-XNOR3X5_P16	C8T28SOIDV_LLS_-XNOR3X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P16	0.800	1.360	1.0880
X4_P16	1.600	0.544	0.8704
X5_P16	0.800	1.360	1.0880
X8_P16	1.600	1.088	1.7408
X9_P16	0.800	1.496	1.1968
X12_P16	1.600	1.360	2.1760
X13_P16	0.800	2.176	1.7408
X15_P16	1.600	1.904	3.0464
X17_P16	0.800	2.312	1.8496
X18_P16	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P16	X4_P16	X5_P16	X8_P16
A	0.0006	0.0012	0.0008	0.0019
B	0.0011	0.0011	0.0013	0.0018
	X9_P16	X12_P16	X13_P16	X15_P16
A	0.0008	0.0031	0.0015	0.0037
B	0.0016	0.0024	0.0026	0.0030
	X17_P16	X18_P16		
A	0.0015	0.0019		
B	0.0026	0.0024		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P16	**X4_P16**	**X2_P16**	**X4_P16**
A to Z ↓	0.0394	0.0166	5.8693	3.0999
A to Z ↑	0.0382	0.0210	8.6958	7.8753
B to Z ↓	0.0301	0.0175	5.8179	3.1309
B to Z ↑	0.0308	0.0193	8.6927	7.8688
	X5_P16	**X8_P16**	**X5_P16**	**X8_P16**
A to Z ↓	0.0378	0.0217	3.2347	1.6845
A to Z ↑	0.0349	0.0251	4.6795	4.1307
B to Z ↓	0.0286	0.0233	3.2164	1.7029
B to Z ↑	0.0280	0.0237	4.6743	4.1247
	X9_P16	**X12_P16**	**X9_P16**	**X12_P16**
A to Z ↓	0.0377	0.0196	1.6938	1.1316
A to Z ↑	0.0357	0.0227	2.4289	2.7656
B to Z ↓	0.0288	0.0198	1.6880	1.1436
B to Z ↑	0.0283	0.0206	2.4285	2.7635
	X13_P16	**X15_P16**	**X13_P16**	**X15_P16**
A to Z ↓	0.0346	0.0213	1.1583	0.8817
A to Z ↑	0.0329	0.0260	1.6778	2.4451
B to Z ↓	0.0242	0.0211	1.1538	0.8913
B to Z ↑	0.0235	0.0237	1.6761	2.4415
	X17_P16	**X18_P16**	**X17_P16**	**X18_P16**
A to Z ↓	0.0368	0.0409	0.8774	0.8683
A to Z ↑	0.0346	0.0373	1.2560	1.1884
B to Z ↓	0.0264	0.0321	0.8749	0.8676
B to Z ↑	0.0253	0.0293	1.2551	1.1884

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P16	1.495e-05	1.000e-20
X4_P16	1.661e-05	1.000e-20
X5_P16	2.240e-05	1.000e-20
X8_P16	2.667e-05	1.000e-20
X9_P16	3.530e-05	1.000e-20
X12_P16	4.094e-05	1.000e-20
X13_P16	5.697e-05	1.000e-20
X15_P16	4.926e-05	1.000e-20
X17_P16	6.140e-05	1.000e-20
X18_P16	6.159e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P16	X4_P16	X5_P16	X8_P16
A to Z	3.679e-03	2.471e-03	4.754e-03	4.826e-03
B to Z	3.194e-03	2.378e-03	4.062e-03	4.792e-03
	X9_P16	X12_P16	X13_P16	X15_P16
A to Z	7.011e-03	6.875e-03	1.134e-02	8.818e-03
B to Z	6.132e-03	6.611e-03	7.936e-03	8.543e-03
	X17_P16	X18_P16		
A to Z	1.303e-02	1.450e-02		
B to Z	9.591e-03	1.150e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

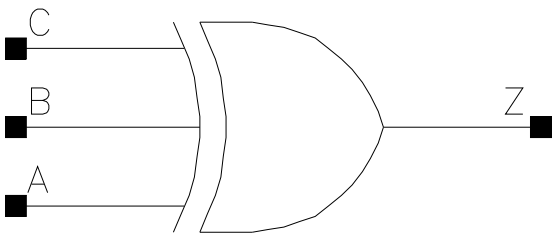
Pin Cycle (vdds)	X2_P16	X4_P16	X5_P16	X8_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P16	X12_P16	X13_P16	X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P16	X18_P16		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P16	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P16	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P16	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P16	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P16	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P16	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P16	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P16	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P16	C8T28SOIDV_LL_-XOR3X4_P16	C8T28SOIDV_LL_-XOR3X9_P16	C8T28SOIDV_LL_-XOR3X13_P16
A	0.0019	0.0018	0.0022	0.0032
B	0.0018	0.0019	0.0022	0.0030
C	0.0012	0.0012	0.0016	0.0024
	C8T28SOIDV_LLS_-XOR3X1_P16	C8T28SOIDV_LLS_-XOR3X2_P16	C8T28SOIDV_LLS_-XOR3X5_P16	C8T28SOIDV_LLS_-XOR3X7_P16

A	0.0020	0.0022	0.0036	0.0056
B	0.0020	0.0021	0.0035	0.0056
C	0.0007	0.0006	0.0006	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P16	**C8T28SOIDV_LL_-XOR3X4_P16**	**C8T28SOIDV_LL_-XOR3X2_P16**	**C8T28SOIDV_LL_-XOR3X4_P16**
A to Z ↓	0.0458	0.0508	6.1471	3.4030
A to Z ↑	0.0440	0.0475	8.7136	4.8443
B to Z ↓	0.0464	0.0519	6.1477	3.4028
B to Z ↑	0.0448	0.0489	8.7175	4.8452
C to Z ↓	0.0460	0.0513	6.1496	3.4047
C to Z ↑	0.0443	0.0480	8.7159	4.8455
	C8T28SOIDV_LL_-XOR3X9_P16	**C8T28SOIDV_LL_-XOR3X13_P16**	**C8T28SOIDV_LL_-XOR3X9_P16**	**C8T28SOIDV_LL_-XOR3X13_P16**
A to Z ↓	0.0474	0.0518	1.6961	1.1569
A to Z ↑	0.0477	0.0542	2.3878	1.6068
B to Z ↓	0.0485	0.0528	1.6964	1.1566
B to Z ↑	0.0491	0.0557	2.3890	1.6072
C to Z ↓	0.0476	0.0525	1.6972	1.1575
C to Z ↑	0.0479	0.0556	2.3883	1.6074
	C8T28SOIDV_LLS_-XOR3X1_P16	**C8T28SOIDV_LLS_-XOR3X2_P16**	**C8T28SOIDV_LLS_-XOR3X1_P16**	**C8T28SOIDV_LLS_-XOR3X2_P16**
A to Z ↓	0.0301	0.0331	7.6450	6.1659
A to Z ↑	0.0300	0.0294	12.3507	8.8117
B to Z ↓	0.0312	0.0341	7.6699	6.1699
B to Z ↑	0.0311	0.0302	12.3591	8.8079
C to Z ↓	0.0498	0.0539	7.6454	6.1488
C to Z ↑	0.0505	0.0506	12.3499	8.7770
	C8T28SOIDV_LLS_-XOR3X5_P16	**C8T28SOIDV_LLS_-XOR3X7_P16**	**C8T28SOIDV_LLS_-XOR3X5_P16**	**C8T28SOIDV_LLS_-XOR3X7_P16**
A to Z ↓	0.0444	0.0379	3.2033	2.2113
A to Z ↑	0.0372	0.0321	4.5873	3.1011
B to Z ↓	0.0428	0.0381	3.2118	2.2149
B to Z ↑	0.0368	0.0326	4.5883	3.1016
C to Z ↓	0.0752	0.0628	3.2145	2.2105
C to Z ↑	0.0690	0.0571	4.5783	3.0918

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P16	1.236e-05	1.000e-20
C8T28SOIDV_LL_XOR3X4_P16	1.490e-05	1.000e-20
C8T28SOIDV_LL_XOR3X9_P16	2.574e-05	1.000e-20
C8T28SOIDV_LL_XOR3X13_P16	3.746e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P16	1.660e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P16	1.929e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P16	3.287e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P16	5.008e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P16	C8T28SOIDV_LL_-XOR3X4_P16	C8T28SOIDV_LL_-XOR3X9_P16	C8T28SOIDV_LL_-XOR3X13_P16
A to Z	2.967e-03	3.789e-03	5.959e-03	1.011e-02
B to Z	2.932e-03	3.776e-03	5.993e-03	1.014e-02
C to Z	2.898e-03	3.732e-03	5.961e-03	1.015e-02
	C8T28SOIDV_LLS_-XOR3X1_P16	C8T28SOIDV_LLS_-XOR3X2_P16	C8T28SOIDV_LLS_-XOR3X5_P16	C8T28SOIDV_LLS_-XOR3X7_P16
A to Z	2.277e-03	2.762e-03	5.568e-03	7.792e-03
B to Z	2.277e-03	2.802e-03	5.686e-03	7.947e-03
C to Z	4.406e-03	5.066e-03	9.458e-03	1.333e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P16	C8T28SOIDV_LL_-XOR3X4_P16	C8T28SOIDV_LL_-XOR3X9_P16	C8T28SOIDV_LL_-XOR3X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P16	C8T28SOIDV_LLS_-XOR3X2_P16	C8T28SOIDV_LLS_-XOR3X5_P16	C8T28SOIDV_LLS_-XOR3X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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