C28SOI_SC_12_COREPBP10_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 10 nm

Overview

- C28SOI_SC_12_COREPBP10_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

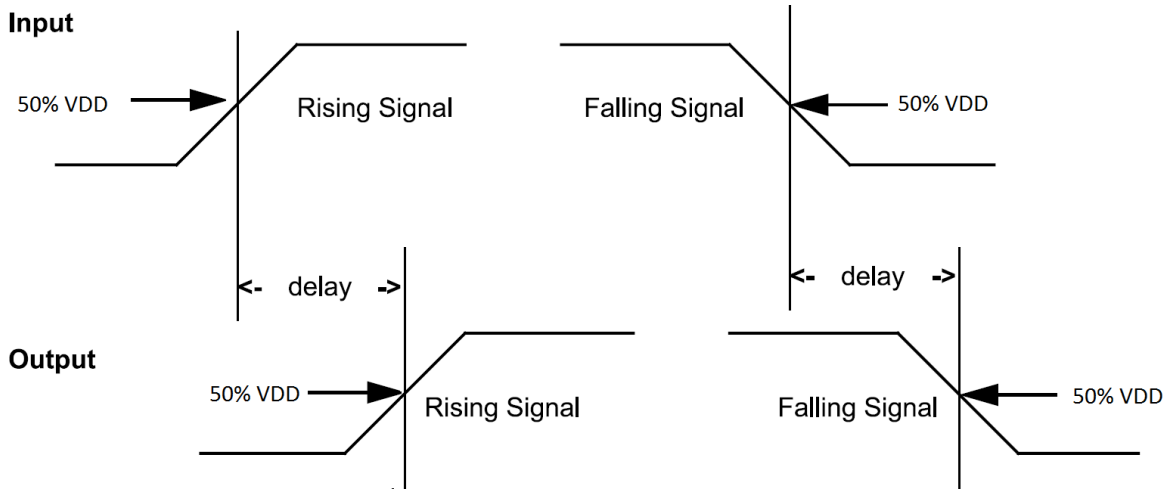


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

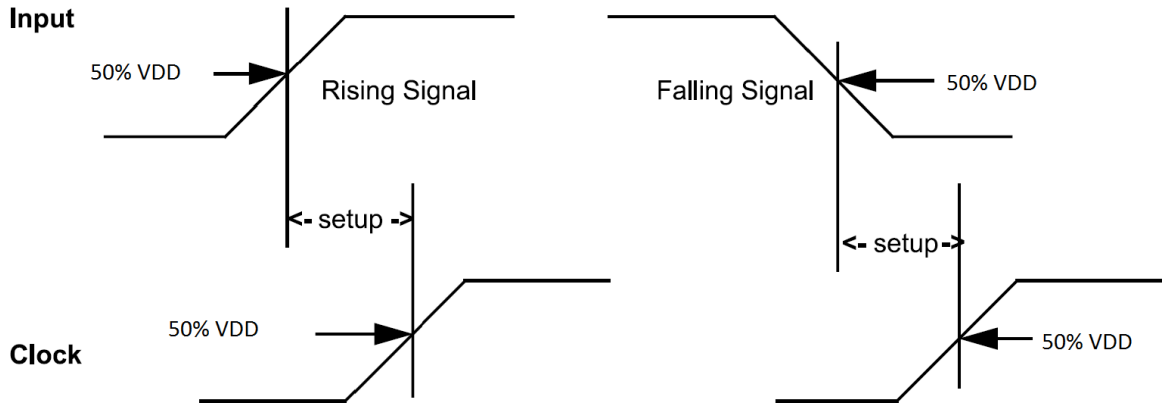


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

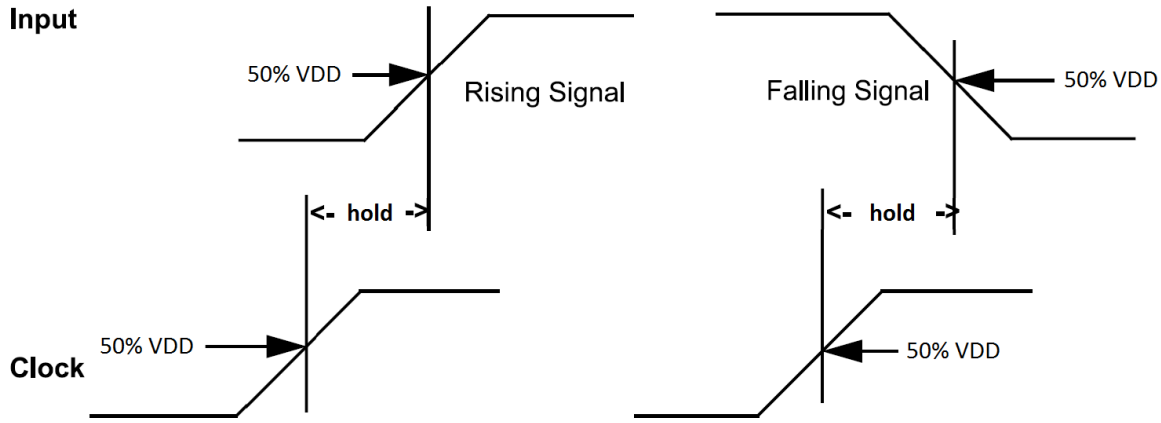


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

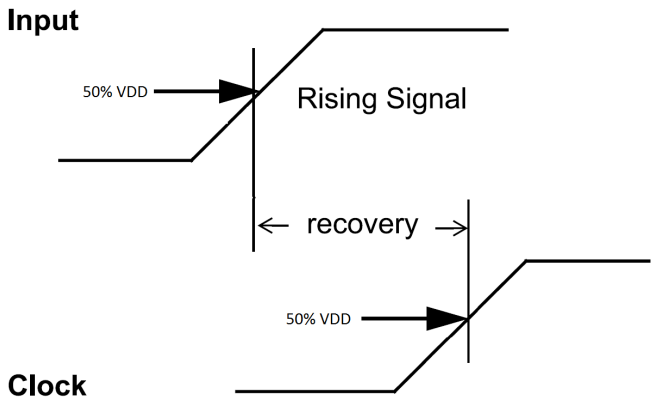


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

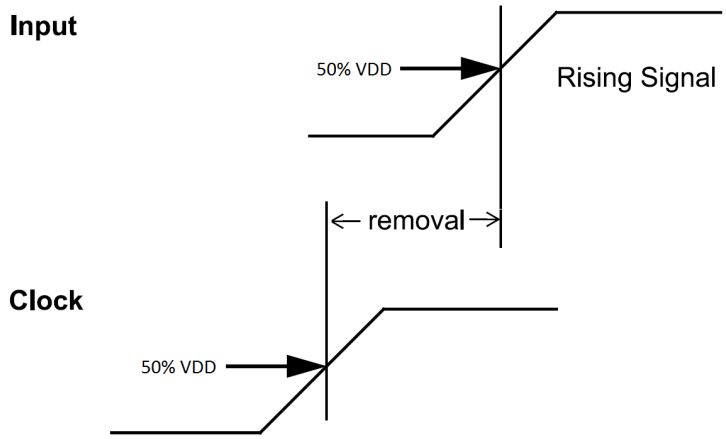


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

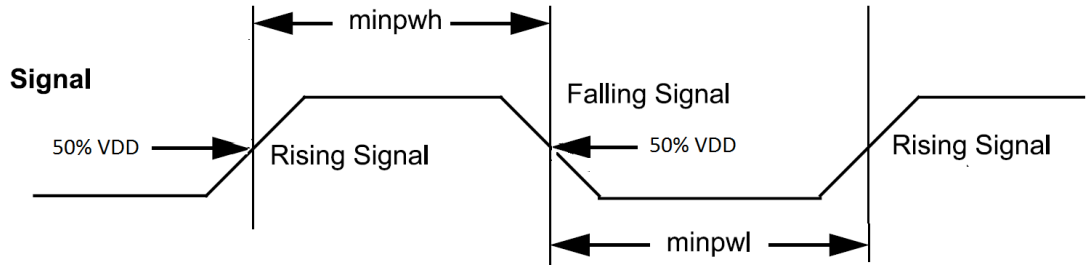


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

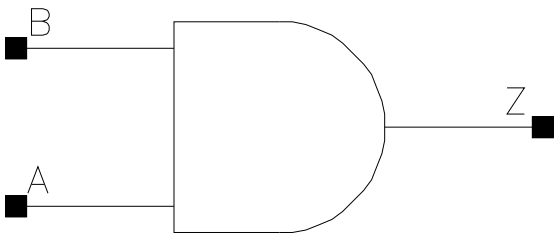
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X25_P10	1.200	1.088	1.3056
X33_P10	1.200	1.360	1.6320
X42_P10	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0008	0.0012	0.0018	0.0022
B	0.0007	0.0011	0.0017	0.0022
	X42_P10			
A	0.0022			
B	0.0022			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0303	0.0249	1.8030	0.9163
A to Z ↑	0.0242	0.0227	2.7370	1.3240
B to Z ↓	0.0287	0.0235	1.8058	0.9162
B to Z ↑	0.0257	0.0241	2.7335	1.3222
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0256	0.0247	0.6075	0.4518

A to Z ↑	0.0223	0.0231	0.8741	0.6604
B to Z ↓	0.0243	0.0226	0.6074	0.4515
B to Z ↑	0.0237	0.0236	0.8730	0.6600
	X42_P10		**X42_P10**	
A to Z ↓	0.0267		0.3669	
A to Z ↑	0.0251		0.5290	
B to Z ↓	0.0246		0.3670	
B to Z ↑	0.0257		0.5285	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	5.325e-07	1.000e-20
X16_P10	1.155e-06	1.000e-20
X25_P10	1.683e-06	1.000e-20
X33_P10	2.331e-06	1.000e-20
X42_P10	2.710e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	1.268e-05	2.449e-05	3.706e-05	7.652e-05
B (output stable)	4.499e-05	8.398e-05	1.309e-04	4.249e-04
A to Z	2.532e-03	4.188e-03	6.466e-03	8.478e-03
B to Z	2.392e-03	3.945e-03	6.078e-03	7.668e-03
	X42_P10			
A (output stable)	7.711e-05			
B (output stable)	4.235e-04			
A to Z	1.018e-02			
B to Z	9.362e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

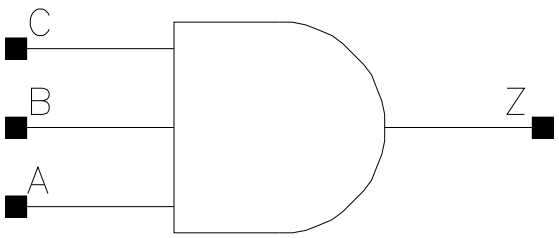
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X25_P10	1.200	1.360	1.6320
X33_P10	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0007	0.0012	0.0019	0.0023
B	0.0007	0.0011	0.0017	0.0021
C	0.0007	0.0011	0.0016	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0327	0.0275	1.8240	0.8923
A to Z ↑	0.0306	0.0290	2.7600	1.3106
B to Z ↓	0.0316	0.0262	1.8248	0.8915
B to Z ↑	0.0315	0.0299	2.7638	1.3124
C to Z ↓	0.0301	0.0248	1.8222	0.8919
C to Z ↑	0.0326	0.0304	2.7626	1.3114
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0275	0.0261	0.6145	0.4586

A to Z ↑	0.0281	0.0274	0.8986	0.6732
B to Z ↓	0.0264	0.0249	0.6140	0.4584
B to Z ↑	0.0291	0.0282	0.8994	0.6727
C to Z ↓	0.0249	0.0235	0.6139	0.4580
C to Z ↑	0.0297	0.0289	0.8987	0.6722

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	5.360e-07	1.000e-20
X17_P10	1.184e-06	1.000e-20
X25_P10	1.683e-06	1.000e-20
X33_P10	2.316e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	9.360e-06	1.864e-05	2.373e-05	3.383e-05
B (output stable)	4.300e-05	8.466e-05	1.200e-04	1.629e-04
C (output stable)	5.315e-05	9.995e-05	1.474e-04	2.026e-04
A to Z	2.801e-03	4.938e-03	7.110e-03	9.171e-03
B to Z	2.657e-03	4.680e-03	6.719e-03	8.641e-03
C to Z	2.530e-03	4.417e-03	6.327e-03	8.112e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

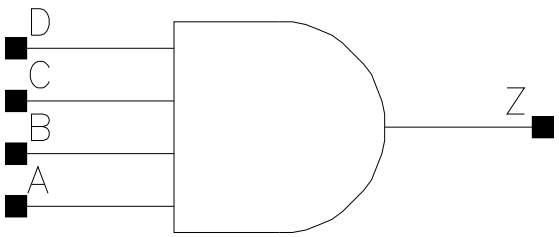
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X6_P10	1.200	1.088	1.3056
X20_P10	1.200	2.312	2.7744
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P10	X6_P10	X20_P10	X27_P10
A	0.0006	0.0008	0.0019	0.0022
B	0.0005	0.0008	0.0019	0.0022
C	0.0005	0.0008	0.0019	0.0022
D	0.0006	0.0008	0.0019	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X6_P10	X4_P10	X6_P10
A to Z ↓	0.0342	0.0296	3.3778	2.2079
A to Z ↑	0.0318	0.0253	9.4718	5.0513
B to Z ↓	0.0332	0.0277	3.3813	2.2073
B to Z ↑	0.0337	0.0263	9.4783	5.0556
C to Z ↓	0.0352	0.0314	3.3443	2.2197
C to Z ↑	0.0314	0.0248	9.4868	5.0663

D to Z ↓	0.0341	0.0291	3.3492	2.2189
D to Z ↑	0.0339	0.0260	9.4944	5.0636
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0286	0.0267	0.6459	0.4574
A to Z ↑	0.0264	0.0294	1.6928	1.2880
B to Z ↓	0.0262	0.0246	0.6455	0.4568
B to Z ↑	0.0268	0.0301	1.6936	1.2887
C to Z ↓	0.0279	0.0256	0.6505	0.4594
C to Z ↑	0.0235	0.0255	1.6937	1.2879
D to Z ↓	0.0252	0.0236	0.6497	0.4586
D to Z ↑	0.0237	0.0262	1.6934	1.2879

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	2.627e-07	1.000e-20
X6_P10	6.583e-07	1.000e-20
X20_P10	2.053e-06	1.000e-20
X27_P10	2.693e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	4.529e-04	7.081e-04	2.091e-03	2.578e-03
B (output stable)	4.258e-04	6.525e-04	1.893e-03	2.381e-03
C (output stable)	4.360e-04	7.181e-04	1.851e-03	2.290e-03
D (output stable)	4.121e-04	6.578e-04	1.678e-03	2.096e-03
A to Z	1.849e-03	2.874e-03	8.706e-03	1.126e-02
B to Z	1.760e-03	2.690e-03	7.925e-03	1.047e-02
C to Z	1.797e-03	2.860e-03	7.341e-03	9.122e-03
D to Z	1.708e-03	2.666e-03	6.541e-03	8.327e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

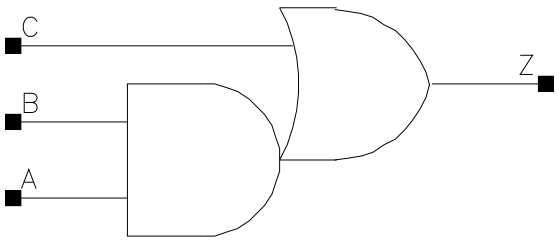
Pin Cycle (vdds)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0011	0.0023
B	0.0007	0.0011	0.0021
C	0.0008	0.0012	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0377	0.0337	1.8525	0.9083
A to Z ↑	0.0249	0.0228	2.6523	1.3002
B to Z ↓	0.0348	0.0311	1.8469	0.9059
B to Z ↑	0.0268	0.0245	2.6536	1.3001
C to Z ↓	0.0368	0.0329	1.8442	0.9047
C to Z ↑	0.0234	0.0223	2.6321	1.2914
	X33_P10		**X33_P10**	
A to Z ↓	0.0337		0.4614	
A to Z ↑	0.0232		0.6556	

B to Z ↓	0.0313		0.4610	
B to Z ↑	0.0244		0.6557	
C to Z ↓	0.0331		0.4601	
C to Z ↑	0.0220		0.6514	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	5.101e-07	1.000e-20
X17_P10	1.099e-06	1.000e-20
X33_P10	2.182e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.091e-05	2.151e-05	5.455e-05
B (output stable)	2.843e-05	4.581e-05	1.465e-04
C (output stable)	5.846e-05	9.988e-05	2.271e-04
A to Z	2.592e-03	4.496e-03	8.918e-03
B to Z	2.447e-03	4.222e-03	8.275e-03
C to Z	2.863e-03	4.967e-03	9.866e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

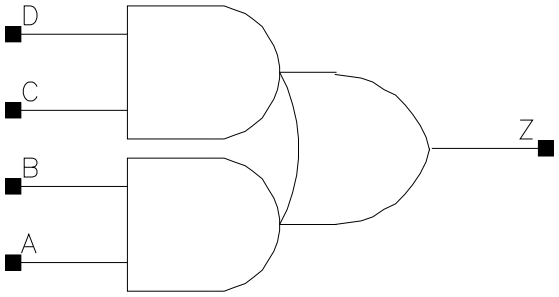
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0011	0.0021
B	0.0008	0.0011	0.0020
C	0.0006	0.0010	0.0022
D	0.0007	0.0011	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0427	0.0372	1.7872	0.9019
A to Z ↑	0.0318	0.0293	2.6186	1.3008
B to Z ↓	0.0397	0.0347	1.7807	0.9000
B to Z ↑	0.0330	0.0310	2.6195	1.3011

C to Z ↓	0.0388	0.0345	1.7816	0.8997
C to Z ↑	0.0269	0.0250	2.6112	1.2971
D to Z ↓	0.0369	0.0326	1.7781	0.8984
D to Z ↑	0.0290	0.0267	2.6118	1.2961
	X33_P10		**X33_P10**	
A to Z ↓	0.0356		0.4616	
A to Z ↑	0.0268		0.6580	
B to Z ↓	0.0336		0.4615	
B to Z ↑	0.0287		0.6583	
C to Z ↓	0.0328		0.4607	
C to Z ↑	0.0233		0.6558	
D to Z ↓	0.0309		0.4608	
D to Z ↑	0.0247		0.6561	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	6.282e-07	1.000e-20
X17_P10	1.339e-06	1.000e-20
X33_P10	2.571e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	3.517e-05	5.280e-05	7.211e-05
B (output stable)	8.126e-05	1.222e-04	1.392e-04
C (output stable)	1.708e-05	3.348e-05	6.713e-05
D (output stable)	3.605e-05	7.007e-05	1.448e-04
A to Z	3.449e-03	5.806e-03	1.076e-02
B to Z	3.175e-03	5.410e-03	1.019e-02
C to Z	2.899e-03	4.933e-03	9.009e-03
D to Z	2.769e-03	4.674e-03	8.485e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

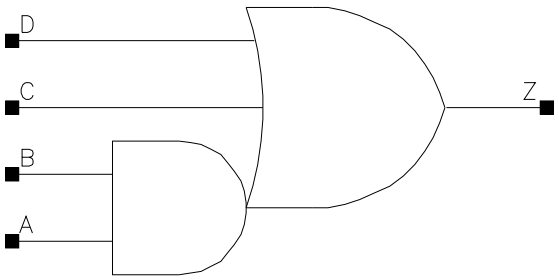
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	0.952	1.1424
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0011	0.0020
B	0.0007	0.0011	0.0020
C	0.0007	0.0011	0.0020
D	0.0007	0.0011	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0485	0.0424	1.9320	0.9574
A to Z ↑	0.0268	0.0248	2.6411	1.3530
B to Z ↓	0.0463	0.0396	1.9294	0.9562
B to Z ↑	0.0288	0.0261	2.6428	1.3531
C to Z ↓	0.0503	0.0438	1.9262	0.9548
C to Z ↑	0.0253	0.0238	2.6204	1.3444

D to Z ↓	0.0501	0.0440	1.9272	0.9552
D to Z ↑	0.0249	0.0236	2.6214	1.3453
	X33_P10		**X33_P10**	
A to Z ↓	0.0430		0.4793	
A to Z ↑	0.0246		0.6563	
B to Z ↓	0.0385		0.4774	
B to Z ↑	0.0254		0.6566	
C to Z ↓	0.0450		0.4773	
C to Z ↑	0.0233		0.6531	
D to Z ↓	0.0440		0.4776	
D to Z ↑	0.0224		0.6517	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	4.514e-07	1.000e-20
X17_P10	9.701e-07	1.000e-20
X33_P10	1.954e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	6.007e-06	1.348e-05	4.664e-05
B (output stable)	1.234e-05	2.492e-05	1.010e-04
C (output stable)	9.443e-05	1.421e-04	3.906e-04
D (output stable)	1.138e-05	1.971e-05	5.313e-05
A to Z	2.869e-03	4.840e-03	9.660e-03
B to Z	2.742e-03	4.561e-03	8.797e-03
C to Z	3.306e-03	5.599e-03	1.137e-02
D to Z	3.114e-03	5.270e-03	1.043e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

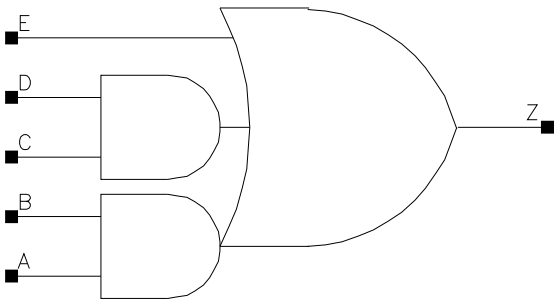
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.088	1.3056
X17_P10	1.200	1.224	1.4688
X33_P10	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0010	0.0021
B	0.0007	0.0010	0.0019
C	0.0008	0.0012	0.0021
D	0.0007	0.0010	0.0020
E	0.0007	0.0011	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0591	0.0506	1.8413	0.9289
A to Z ↑	0.0334	0.0294	2.5932	1.3076

B to Z ↓	0.0569	0.0481	1.8384	0.9275
B to Z ↑	0.0360	0.0314	2.5913	1.3077
C to Z ↓	0.0505	0.0445	1.8348	0.9262
C to Z ↑	0.0283	0.0248	2.5720	1.2998
D to Z ↓	0.0469	0.0407	1.8287	0.9226
D to Z ↑	0.0303	0.0264	2.5726	1.2987
E to Z ↓	0.0522	0.0449	1.8266	0.9228
E to Z ↑	0.0264	0.0234	2.5479	1.2895
	X33_P10		**X33_P10**	
A to Z ↓	0.0495		0.4787	
A to Z ↑	0.0301		0.6611	
B to Z ↓	0.0465		0.4783	
B to Z ↑	0.0319		0.6611	
C to Z ↓	0.0428		0.4772	
C to Z ↑	0.0247		0.6565	
D to Z ↓	0.0392		0.4760	
D to Z ↑	0.0261		0.6556	
E to Z ↓	0.0436		0.4759	
E to Z ↑	0.0233		0.6513	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	5.754e-07	1.000e-20
X17_P10	1.209e-06	1.000e-20
X33_P10	2.276e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.334e-05	3.661e-05	8.214e-05
B (output stable)	4.255e-05	4.984e-05	1.230e-04
C (output stable)	1.771e-05	2.760e-05	6.620e-05
D (output stable)	2.647e-05	4.645e-05	1.165e-04
E (output stable)	7.436e-05	7.157e-05	1.898e-04
A to Z	3.981e-03	6.436e-03	1.259e-02
B to Z	3.854e-03	6.148e-03	1.188e-02
C to Z	3.112e-03	5.122e-03	9.795e-03
D to Z	2.959e-03	4.819e-03	9.122e-03
E to Z	3.423e-03	5.555e-03	1.066e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

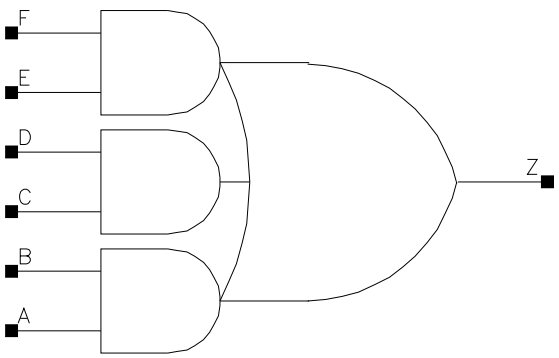
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.360	1.6320
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
A	0.0007	0.0008	0.0010	0.0021

B	0.0007	0.0008	0.0014	0.0019
C	0.0006	0.0008	0.0010	0.0020
D	0.0007	0.0008	0.0010	0.0019
E	0.0007	0.0008	0.0010	0.0021
F	0.0007	0.0008	0.0011	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0591	0.0561	3.4976	1.8438
A to Z ↑	0.0354	0.0342	5.2274	2.6495
B to Z ↓	0.0544	0.0520	3.4801	1.8357
B to Z ↑	0.0365	0.0356	5.2244	2.6488
C to Z ↓	0.0540	0.0517	3.4873	1.8398
C to Z ↑	0.0319	0.0308	5.1958	2.6329
D to Z ↓	0.0514	0.0493	3.4785	1.8348
D to Z ↑	0.0342	0.0331	5.1955	2.6336
E to Z ↓	0.0452	0.0444	3.4723	1.8325
E to Z ↑	0.0270	0.0263	5.1696	2.6211
F to Z ↓	0.0422	0.0414	3.4641	1.8274
F to Z ↑	0.0288	0.0280	5.1714	2.6208
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
A to Z ↓	0.0537	0.0515	0.9315	0.4767
A to Z ↑	0.0323	0.0321	1.3124	0.6638
B to Z ↓	0.0505	0.0488	0.9269	0.4762
B to Z ↑	0.0343	0.0340	1.3121	0.6638
C to Z ↓	0.0503	0.0481	0.9294	0.4765
C to Z ↑	0.0292	0.0297	1.3055	0.6602
D to Z ↓	0.0474	0.0455	0.9265	0.4759
D to Z ↑	0.0313	0.0315	1.3055	0.6599
E to Z ↓	0.0431	0.0432	0.9254	0.4751
E to Z ↑	0.0248	0.0257	1.2998	0.6585
F to Z ↓	0.0403	0.0401	0.9229	0.4738
F to Z ↑	0.0266	0.0276	1.3006	0.6581

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	4.566e-07	1.000e-20
X8_P10	7.943e-07	1.000e-20
X17_P10	1.429e-06	1.000e-20
X33_P10	2.669e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	6.220e-05	7.151e-05	8.261e-05	1.623e-04
B (output stable)	1.647e-04	1.723e-04	1.714e-04	2.680e-04
C (output stable)	3.279e-05	3.845e-05	4.413e-05	6.803e-05
D (output stable)	4.979e-05	5.966e-05	7.159e-05	1.509e-04
E (output stable)	3.742e-05	4.284e-05	5.218e-05	7.634e-05
F (output stable)	4.622e-05	5.483e-05	7.369e-05	1.475e-04

A to Z	3.607e-03	4.769e-03	7.218e-03	1.365e-02
B to Z	3.309e-03	4.422e-03	6.753e-03	1.293e-02
C to Z	3.040e-03	4.093e-03	6.315e-03	1.194e-02
D to Z	2.906e-03	3.922e-03	6.033e-03	1.127e-02
E to Z	2.430e-03	3.403e-03	5.292e-03	1.033e-02
F to Z	2.289e-03	3.220e-03	5.018e-03	9.703e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

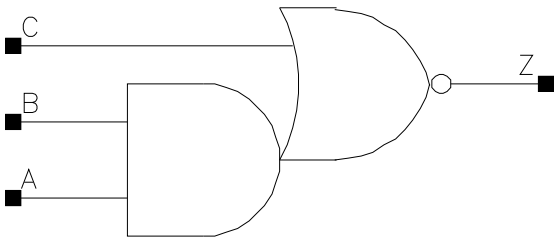
Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008
X44_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X33_P10	X44_P10
A	0.0008	0.0025	0.0051	0.0068
B	0.0008	0.0024	0.0047	0.0063
C	0.0009	0.0027	0.0053	0.0069

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0101	0.0105	3.2531	1.1040
A to Z ↑	0.0171	0.0175	5.1909	1.7412
B to Z ↓	0.0102	0.0104	3.2882	1.1205
B to Z ↑	0.0140	0.0137	5.1135	1.7421
C to Z ↓	0.0106	0.0107	1.8676	0.6429
C to Z ↑	0.0177	0.0175	4.7350	1.6024
	X33_P10	**X44_P10**	**X33_P10**	**X44_P10**
A to Z ↓	0.0108	0.0107	0.5619	0.4270

A to Z ↑	0.0174	0.0174	0.8718	0.6624
B to Z ↓	0.0104	0.0103	0.5707	0.4339
B to Z ↑	0.0137	0.0135	0.8703	0.6591
C to Z ↓	0.0121	0.0122	0.3823	0.2976
C to Z ↑	0.0177	0.0175	0.8005	0.6073

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P10	4.791e-07	1.000e-20
X17_P10	1.387e-06	1.000e-20
X33_P10	2.669e-06	1.000e-20
X44_P10	3.525e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	2.259e-05	7.256e-05	1.526e-04	2.022e-04
B (output stable)	4.768e-05	2.067e-04	4.402e-04	5.768e-04
C (output stable)	9.845e-05	2.963e-04	6.438e-04	8.442e-04
A to Z	1.205e-03	3.797e-03	7.639e-03	1.004e-02
B to Z	9.585e-04	2.765e-03	5.557e-03	7.249e-03
C to Z	1.710e-03	5.036e-03	1.014e-02	1.333e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

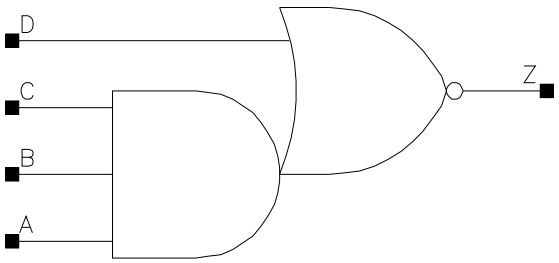
Pin Cycle (vdds)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X29_P10	1.200	3.536	4.2432
X38_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X29_P10	X38_P10
A	0.0009	0.0052	0.0068
B	0.0008	0.0049	0.0064
C	0.0008	0.0047	0.0061
D	0.0009	0.0053	0.0066

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X29_P10	X5_P10	X29_P10
A to Z ↓	0.0147	0.0158	4.6299	0.8037
A to Z ↑	0.0219	0.0219	5.1928	0.8622
B to Z ↓	0.0150	0.0153	4.6494	0.8074
B to Z ↑	0.0196	0.0193	5.1978	0.8693
C to Z ↓	0.0147	0.0143	4.6715	0.8133
C to Z ↑	0.0167	0.0159	5.1248	0.8764
D to Z ↓	0.0126	0.0144	1.9089	0.3847

D to Z ↑	0.0204	0.0207	4.4306	0.7439
	X38_P10		**X38_P10**	
A to Z ↓	0.0153		0.6232	
A to Z ↑	0.0212		0.6506	
B to Z ↓	0.0150		0.6264	
B to Z ↑	0.0187		0.6578	
C to Z ↓	0.0139		0.6311	
C to Z ↑	0.0152		0.6660	
D to Z ↓	0.0149		0.3210	
D to Z ↑	0.0199		0.5626	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	4.918e-07	1.000e-20
X29_P10	2.737e-06	1.000e-20
X38_P10	3.563e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X29_P10	X38_P10
A (output stable)	1.524e-05	1.307e-04	1.584e-04
B (output stable)	3.942e-05	2.964e-04	3.881e-04
C (output stable)	7.679e-05	6.879e-04	8.895e-04
D (output stable)	3.050e-04	2.689e-03	3.219e-03
A to Z	1.803e-03	1.135e-02	1.414e-02
B to Z	1.541e-03	9.192e-03	1.150e-02
C to Z	1.285e-03	7.047e-03	8.660e-03
D to Z	2.228e-03	1.360e-02	1.697e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

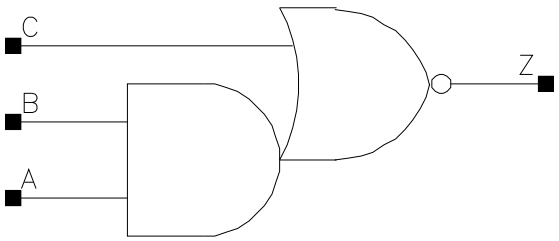
Pin Cycle (vdds)	X5_P10	X29_P10	X38_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X11_P10	1.200	1.088	1.3056
X16_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X11_P10	X16_P10	X23_P10
A	0.0009	0.0019	0.0028	0.0037
B	0.0009	0.0018	0.0026	0.0034
C	0.0009	0.0016	0.0024	0.0034
	X46_P10			
A	0.0071			
B	0.0067			
C	0.0067			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X11_P10	X6_P10	X11_P10
A to Z ↓	0.0122	0.0132	3.1401	1.5972
A to Z ↑	0.0193	0.0203	5.1737	2.5269
B to Z ↓	0.0130	0.0132	3.1704	1.6166

B to Z ↑	0.0168	0.0172	5.1040	2.5343
C to Z ↓	0.0074	0.0079	1.9252	1.1372
C to Z ↑	0.0140	0.0136	4.7578	2.3475
	X16_P10	**X23_P10**	**X16_P10**	**X23_P10**
A to Z ↓	0.0125	0.0128	1.1035	0.8298
A to Z ↑	0.0189	0.0192	1.7016	1.2908
B to Z ↓	0.0131	0.0129	1.1175	0.8402
B to Z ↑	0.0158	0.0160	1.7003	1.2959
C to Z ↓	0.0079	0.0070	0.7901	0.4967
C to Z ↑	0.0130	0.0134	1.5801	1.1983
	X46_P10		**X46_P10**	
A to Z ↓	0.0124		0.4268	
A to Z ↑	0.0186		0.6718	
B to Z ↓	0.0126		0.4322	
B to Z ↑	0.0153		0.6698	
C to Z ↓	0.0072		0.2546	
C to Z ↑	0.0133		0.6228	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P10	4.848e-07	1.000e-20
X11_P10	9.755e-07	1.000e-20
X16_P10	1.372e-06	1.000e-20
X23_P10	1.919e-06	1.000e-20
X46_P10	3.727e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	3.014e-05	7.878e-05	1.011e-04	1.416e-04
B (output stable)	5.712e-05	2.334e-04	2.239e-04	3.379e-04
C (output stable)	7.136e-05	1.793e-04	2.328e-04	3.424e-04
A to Z	1.768e-03	3.876e-03	5.246e-03	7.140e-03
B to Z	1.498e-03	3.114e-03	4.174e-03	5.607e-03
C to Z	9.609e-04	1.953e-03	2.671e-03	3.747e-03
	X46_P10			
A (output stable)	2.580e-04			
B (output stable)	5.754e-04			
C (output stable)	5.454e-04			
A to Z	1.327e-02			
B to Z	1.038e-02			
C to Z	6.954e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

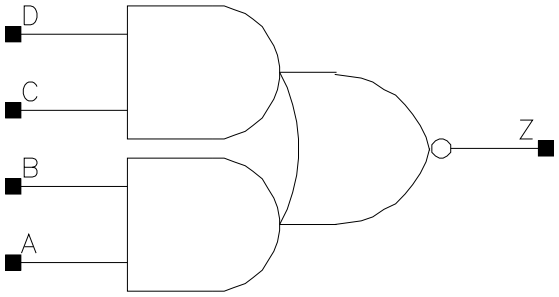
	X46_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P10	X10_P10	X16_P10	X21_P10
A	0.0008	0.0019	0.0028	0.0036
B	0.0008	0.0017	0.0026	0.0034
C	0.0007	0.0018	0.0025	0.0034
D	0.0007	0.0016	0.0024	0.0032
	X42_P10			
A	0.0072			
B	0.0067			
C	0.0068			
D	0.0064			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X10_P10**	**X4_P10**	**X10_P10**
A to Z ↓	0.0137	0.0135	3.8941	1.5355
A to Z ↑	0.0251	0.0211	7.1137	2.3363
B to Z ↓	0.0147	0.0147	3.9379	1.5538
B to Z ↑	0.0225	0.0192	7.0915	2.3964
C to Z ↓	0.0103	0.0098	3.9875	1.5446
C to Z ↑	0.0199	0.0172	7.1085	2.3519
D to Z ↓	0.0106	0.0103	4.0457	1.5691
D to Z ↑	0.0169	0.0146	7.0870	2.3883
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0146	0.0146	1.1086	0.8335
A to Z ↑	0.0219	0.0217	1.5754	1.2215
B to Z ↓	0.0154	0.0150	1.1213	0.8432
B to Z ↑	0.0191	0.0188	1.5748	1.2234
C to Z ↓	0.0106	0.0109	1.1077	0.8343
C to Z ↑	0.0176	0.0181	1.5759	1.2196
D to Z ↓	0.0106	0.0104	1.1257	0.8477
D to Z ↑	0.0144	0.0146	1.5788	1.2221
	X42_P10		**X42_P10**	
A to Z ↓	0.0152		0.4336	
A to Z ↑	0.0222		0.6130	
B to Z ↓	0.0155		0.4384	
B to Z ↑	0.0190		0.6101	
C to Z ↓	0.0114		0.4298	
C to Z ↑	0.0183		0.6136	
D to Z ↓	0.0109		0.4364	
D to Z ↑	0.0149		0.6117	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	3.718e-07	1.000e-20
X10_P10	1.191e-06	1.000e-20
X16_P10	1.679e-06	1.000e-20
X21_P10	2.253e-06	1.000e-20
X42_P10	4.410e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	2.998e-05	7.048e-05	1.305e-04	1.767e-04
B (output stable)	5.804e-05	1.416e-04	2.908e-04	3.903e-04
C (output stable)	2.131e-05	6.252e-05	1.190e-04	1.758e-04
D (output stable)	5.001e-05	1.360e-04	3.369e-04	4.904e-04
A to Z	1.811e-03	4.405e-03	6.908e-03	8.887e-03
B to Z	1.576e-03	3.837e-03	5.786e-03	7.407e-03
C to Z	1.067e-03	2.674e-03	4.161e-03	5.672e-03
D to Z	8.633e-04	2.162e-03	3.120e-03	4.204e-03
	X42_P10			
A (output stable)	3.426e-04			
B (output stable)	7.342e-04			
C (output stable)	3.293e-04			
D (output stable)	9.061e-04			

A to Z	1.761e-02			
B to Z	1.464e-02			
C to Z	1.103e-02			
D to Z	8.307e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

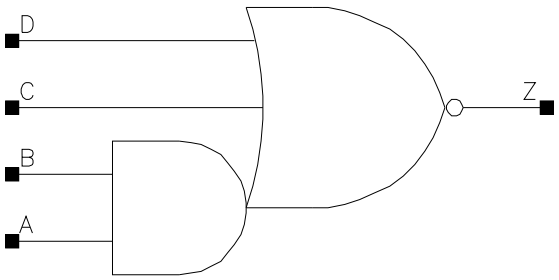
Pin Cycle (vdds)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X35_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P10	X35_P10
A	0.0008	0.0065
B	0.0009	0.0060
C	0.0009	0.0064
D	0.0009	0.0060

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X35_P10	X5_P10	X35_P10
A to Z ↓	0.0117	0.0122	3.2856	0.4851
A to Z ↑	0.0225	0.0211	7.6234	0.9807
B to Z ↓	0.0122	0.0122	3.3269	0.4926
B to Z ↑	0.0188	0.0169	7.5663	0.9800
C to Z ↓	0.0129	0.0165	1.9947	0.3819
C to Z ↑	0.0253	0.0248	7.1812	0.9249
D to Z ↓	0.0123	0.0151	2.0110	0.3818

D to Z ↑	0.0248	0.0234	7.1947	0.9283

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	4.327e-07	1.000e-20
X35_P10	3.054e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X35_P10
A (output stable)	1.361e-05	1.481e-04
B (output stable)	2.508e-05	2.910e-04
C (output stable)	1.397e-04	1.361e-03
D (output stable)	1.893e-05	2.125e-04
A to Z	1.459e-03	1.053e-02
B to Z	1.204e-03	8.025e-03
C to Z	2.314e-03	1.783e-02
D to Z	1.963e-03	1.418e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

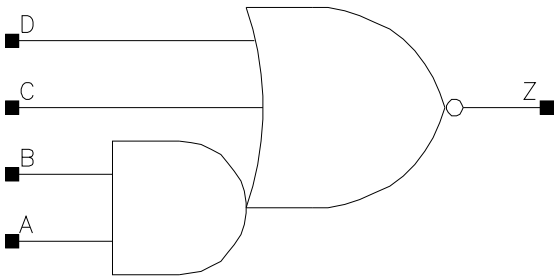
Pin Cycle (vdds)	X5_P10	X35_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X17_P10	1.200	2.448	2.9376
X34_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P10	X17_P10	X34_P10
A	0.0009	0.0036	0.0073
B	0.0009	0.0034	0.0069
C	0.0008	0.0031	0.0060
D	0.0008	0.0028	0.0055

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X17_P10	X4_P10	X17_P10
A to Z ↓	0.0142	0.0155	3.5467	0.9381
A to Z ↑	0.0255	0.0267	7.6632	1.8906
B to Z ↓	0.0155	0.0160	3.5864	0.9482
B to Z ↑	0.0226	0.0229	7.5804	1.8931
C to Z ↓	0.0131	0.0130	3.1483	0.7673
C to Z ↑	0.0187	0.0199	7.2308	1.7932

D to Z ↓	0.0109	0.0099	3.2209	0.7723
D to Z ↑	0.0168	0.0155	7.2667	1.8036
	X34_P10		**X34_P10**	
A to Z ↓	0.0153		0.4811	
A to Z ↑	0.0263		0.9652	
B to Z ↓	0.0161		0.4864	
B to Z ↑	0.0225		0.9611	
C to Z ↓	0.0134		0.4090	
C to Z ↑	0.0194		0.9133	
D to Z ↓	0.0102		0.4134	
D to Z ↑	0.0153		0.9189	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	3.958e-07	1.000e-20
X17_P10	1.579e-06	1.000e-20
X34_P10	3.094e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X17_P10	X34_P10
A (output stable)	3.282e-05	1.554e-04	3.079e-04
B (output stable)	4.032e-05	2.407e-04	4.543e-04
C (output stable)	3.749e-05	3.032e-04	5.551e-04
D (output stable)	2.318e-05	2.286e-04	4.154e-04
A to Z	2.186e-03	9.456e-03	1.828e-02
B to Z	1.933e-03	7.969e-03	1.544e-02
C to Z	1.323e-03	5.791e-03	1.102e-02
D to Z	9.624e-04	3.657e-03	6.962e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

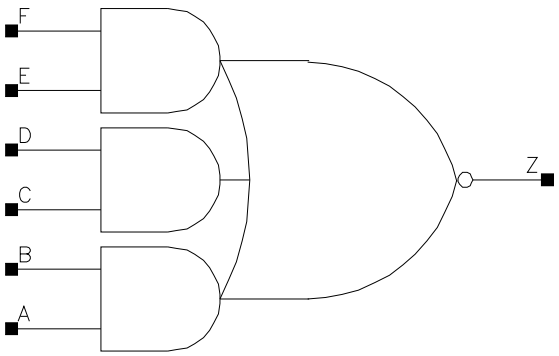
Pin Cycle (vdds)	X4_P10	X17_P10	X34_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X8_P10	1.200	2.176	2.6112
X13_P10	1.200	2.720	3.2640
X17_P10	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P10	X8_P10	X13_P10	X17_P10
A	0.0009	0.0018	0.0027	0.0036

B	0.0009	0.0017	0.0025	0.0033
C	0.0009	0.0017	0.0026	0.0033
D	0.0009	0.0016	0.0024	0.0031
E	0.0011	0.0017	0.0024	0.0032
F	0.0008	0.0015	0.0023	0.0030

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0166	0.0198	3.1479	1.8199
A to Z ↑	0.0362	0.0355	7.3592	3.4139
B to Z ↓	0.0184	0.0208	3.1791	1.8342
B to Z ↑	0.0332	0.0322	7.3485	3.4210
C to Z ↓	0.0150	0.0177	3.1252	1.8362
C to Z ↑	0.0319	0.0320	7.4033	3.4286
D to Z ↓	0.0164	0.0188	3.1644	1.8555
D to Z ↑	0.0287	0.0286	7.3620	3.4279
E to Z ↓	0.0114	0.0135	3.0847	1.8394
E to Z ↑	0.0248	0.0247	7.3341	3.4089
F to Z ↓	0.0119	0.0137	3.1386	1.8683
F to Z ↑	0.0215	0.0209	7.3889	3.4136
	X13_P10	**X17_P10**	**X13_P10**	**X17_P10**
A to Z ↓	0.0189	0.0191	1.2377	0.9441
A to Z ↑	0.0330	0.0332	2.2528	1.7278
B to Z ↓	0.0204	0.0201	1.2471	0.9516
B to Z ↑	0.0300	0.0297	2.2606	1.7279
C to Z ↓	0.0170	0.0171	1.2466	0.9358
C to Z ↑	0.0295	0.0299	2.2665	1.7402
D to Z ↓	0.0183	0.0177	1.2591	0.9455
D to Z ↑	0.0265	0.0264	2.2693	1.7362
E to Z ↓	0.0129	0.0129	1.2437	0.9382
E to Z ↑	0.0231	0.0232	2.2582	1.7261
F to Z ↓	0.0133	0.0127	1.2614	0.9522
F to Z ↑	0.0197	0.0195	2.2629	1.7343

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	6.766e-07	1.000e-20
X8_P10	1.383e-06	1.000e-20
X13_P10	1.962e-06	1.000e-20
X17_P10	2.617e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

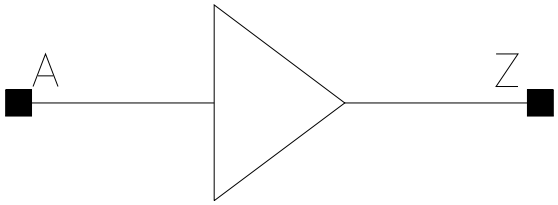
Pin Cycle (vdd)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	8.514e-05	1.878e-04	2.516e-04	3.288e-04
B (output stable)	1.525e-04	3.578e-04	4.177e-04	5.736e-04
C (output stable)	4.039e-05	9.531e-05	1.205e-04	1.715e-04
D (output stable)	6.839e-05	2.050e-04	2.340e-04	3.501e-04
E (output stable)	3.716e-05	9.463e-05	1.306e-04	1.842e-04
F (output stable)	5.971e-05	1.892e-04	2.331e-04	3.491e-04

A to Z	3.468e-03	7.305e-03	1.008e-02	1.339e-02
B to Z	3.171e-03	6.570e-03	9.092e-03	1.189e-02
C to Z	2.595e-03	5.699e-03	7.672e-03	1.023e-02
D to Z	2.328e-03	5.004e-03	6.776e-03	8.858e-03
E to Z	1.688e-03	3.825e-03	5.083e-03	6.763e-03
F to Z	1.436e-03	3.122e-03	4.184e-03	5.420e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.408	0.4896
X6_P10	1.200	0.408	0.4896
X8_P10	1.200	0.408	0.4896
X13_P10	1.200	0.544	0.6528
X16_P10	1.200	0.544	0.6528
X21_P10	1.200	0.680	0.8160
X25_P10	1.200	0.680	0.8160
X29_P10	1.200	0.952	1.1424
X33_P10	1.200	0.952	1.1424
X42_P10	1.200	1.088	1.3056
X50_P10	1.200	1.224	1.4688
X58_P10	1.200	1.496	1.7952
X67_P10	1.200	1.632	1.9584
X75_P10	1.200	1.768	2.1216
X84_P10	1.200	1.904	2.2848
X100_P10	1.200	2.312	2.7744
X134_P10	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0009	0.0009	0.0009	0.0009
	X16_P10	X21_P10	X25_P10	X29_P10
A	0.0009	0.0012	0.0012	0.0016
	X33_P10	X42_P10	X50_P10	X58_P10
A	0.0016	0.0019	0.0022	0.0033

	X67_P10	X75_P10	X84_P10	X100_P10
A	0.0033	0.0033	0.0032	0.0043
	X134_P10			
A	0.0053			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0238	0.0241	3.2948	2.4077
A to Z ↑	0.0191	0.0190	5.1065	3.7262
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0251	0.0284	1.7852	1.1521
A to Z ↑	0.0197	0.0224	2.6440	1.7399
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0305	0.0254	0.9180	0.7101
A to Z ↑	0.0237	0.0208	1.3285	1.0441
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0265	0.0255	0.6097	0.5140
A to Z ↑	0.0215	0.0199	0.8725	0.7443
	X33_P10	**X42_P10**	**X33_P10**	**X42_P10**
A to Z ↓	0.0267	0.0260	0.4563	0.3710
A to Z ↑	0.0206	0.0210	0.6510	0.5245
	X50_P10	**X58_P10**	**X50_P10**	**X58_P10**
A to Z ↓	0.0254	0.0236	0.3079	0.2656
A to Z ↑	0.0206	0.0194	0.4354	0.3744
	X67_P10	**X75_P10**	**X67_P10**	**X75_P10**
A to Z ↓	0.0247	0.0261	0.2332	0.2107
A to Z ↑	0.0202	0.0213	0.3282	0.2941
	X84_P10	**X100_P10**	**X84_P10**	**X100_P10**
A to Z ↓	0.0272	0.0258	0.1906	0.1605
A to Z ↑	0.0221	0.0212	0.2654	0.2228
	X134_P10		**X134_P10**	
A to Z ↓	0.0267		0.1246	
A to Z ↑	0.0221		0.1707	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	2.910e-07	1.000e-20
X6_P10	3.783e-07	1.000e-20
X8_P10	5.046e-07	1.000e-20
X13_P10	6.315e-07	1.000e-20
X16_P10	8.448e-07	1.000e-20
X21_P10	1.171e-06	1.000e-20
X25_P10	1.368e-06	1.000e-20
X29_P10	1.503e-06	1.000e-20
X33_P10	1.685e-06	1.000e-20
X42_P10	2.142e-06	1.000e-20
X50_P10	2.614e-06	1.000e-20
X58_P10	3.238e-06	1.000e-20
X67_P10	3.550e-06	1.000e-20
X75_P10	3.862e-06	1.000e-20

X84_P10	4.174e-06	1.000e-20
X100_P10	5.110e-06	1.000e-20
X134_P10	6.670e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	1.720e-03	1.930e-03	2.294e-03	3.070e-03
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	3.713e-03	5.014e-03	5.605e-03	6.303e-03
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	6.968e-03	8.773e-03	1.030e-02	1.244e-02
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	1.387e-02	1.560e-02	1.707e-02	2.085e-02
	X134_P10			
A to Z	2.781e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

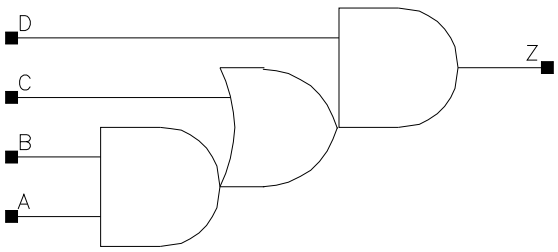
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P10			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.632	1.9584
X25_P10	1.200	1.768	2.1216
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0010	0.0022	0.0022	0.0022
B	0.0011	0.0020	0.0020	0.0020
C	0.0011	0.0025	0.0025	0.0025
D	0.0016	0.0021	0.0021	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0323	0.0306	1.8199	0.9050
A to Z ↑	0.0300	0.0286	2.6843	1.3052
B to Z ↓	0.0297	0.0278	1.8180	0.9041
B to Z ↑	0.0305	0.0284	2.6815	1.3051
C to Z ↓	0.0275	0.0255	1.8137	0.9020
C to Z ↑	0.0227	0.0208	2.6575	1.2934

D to Z ↓	0.0269	0.0239	1.7972	0.8944
D to Z ↑	0.0261	0.0229	2.6604	1.2952
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0336	0.0354	0.6150	0.4638
A to Z ↑	0.0314	0.0329	0.8846	0.6652
B to Z ↓	0.0309	0.0333	0.6153	0.4630
B to Z ↑	0.0314	0.0335	0.8849	0.6648
C to Z ↓	0.0287	0.0310	0.6136	0.4617
C to Z ↑	0.0233	0.0250	0.8756	0.6574
D to Z ↓	0.0260	0.0273	0.6064	0.4548
D to Z ↑	0.0252	0.0265	0.8772	0.6585

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	8.966e-07	1.000e-20
X17_P10	1.757e-06	1.000e-20
X25_P10	2.118e-06	1.000e-20
X33_P10	2.481e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	7.601e-05	1.460e-04	1.444e-04	1.494e-04
B (output stable)	1.050e-04	1.982e-04	1.992e-04	1.870e-04
C (output stable)	3.286e-04	5.598e-04	5.643e-04	5.380e-04
D (output stable)	9.078e-05	1.183e-04	1.158e-04	1.124e-04
A to Z	3.890e-03	7.156e-03	8.957e-03	1.037e-02
B to Z	3.597e-03	6.416e-03	8.202e-03	9.755e-03
C to Z	3.013e-03	5.216e-03	6.967e-03	8.416e-03
D to Z	3.951e-03	6.861e-03	8.579e-03	9.913e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

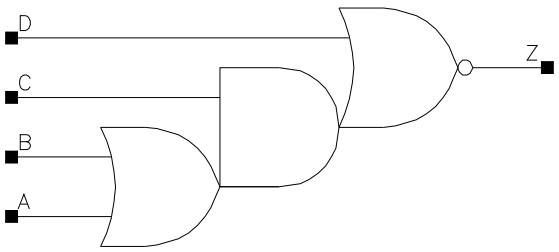
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.952	1.1424
X11_P10	1.200	1.496	1.7952
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X16_P10	X21_P10
A	0.0010	0.0018	0.0027	0.0036
B	0.0009	0.0017	0.0028	0.0035
C	0.0009	0.0017	0.0026	0.0035
D	0.0012	0.0017	0.0026	0.0034

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0151	0.0144	3.0940	1.6303
A to Z ↑	0.0303	0.0283	7.5161	3.9346
B to Z ↓	0.0144	0.0139	3.0161	1.5999
B to Z ↑	0.0289	0.0274	7.5288	3.9421
C to Z ↓	0.0137	0.0131	2.8654	1.5111
C to Z ↑	0.0190	0.0177	5.0795	2.6178

D to Z ↓	0.0083	0.0071	1.8610	0.9425
D to Z ↑	0.0169	0.0149	5.4481	2.8161
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0143	0.0147	1.0975	0.8464
A to Z ↑	0.0263	0.0278	2.5135	1.9476
B to Z ↓	0.0135	0.0139	1.1052	0.8489
B to Z ↑	0.0260	0.0267	2.5180	1.9507
C to Z ↓	0.0132	0.0133	1.0371	0.7955
C to Z ↑	0.0170	0.0172	1.7273	1.2966
D to Z ↓	0.0071	0.0071	0.6582	0.5024
D to Z ↑	0.0138	0.0138	1.8418	1.3953

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	5.765e-07	1.000e-20
X11_P10	1.098e-06	1.000e-20
X16_P10	1.542e-06	1.000e-20
X21_P10	2.053e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	3.944e-05	6.695e-05	8.596e-05	1.468e-04
B (output stable)	2.544e-06	7.743e-06	1.210e-06	1.573e-05
C (output stable)	1.925e-04	3.662e-04	4.857e-04	7.377e-04
D (output stable)	7.554e-05	1.441e-04	2.001e-04	2.992e-04
A to Z	2.803e-03	4.914e-03	6.869e-03	9.633e-03
B to Z	2.278e-03	4.047e-03	5.821e-03	7.871e-03
C to Z	1.905e-03	3.303e-03	4.707e-03	6.431e-03
D to Z	1.171e-03	2.005e-03	2.722e-03	3.629e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

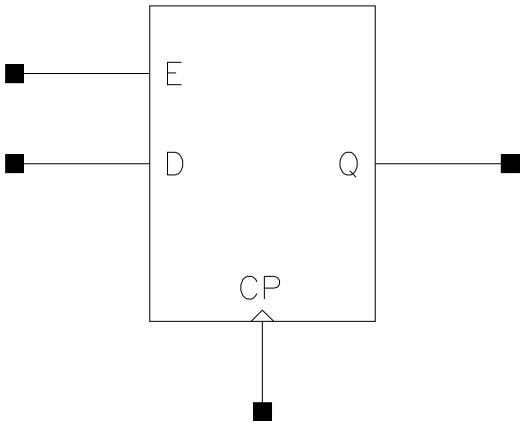
Pin Cycle (vdds)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.128	3.7536
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0012	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0382	0.0438	1.8097	0.9340
CP to Q ↑	0.0473	0.0505	2.6994	1.3516
	X33_P10		**X33_P10**	
CP to Q ↓	0.0650		0.4630	
CP to Q ↑	0.0798		0.6690	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0492	0.0492	0.0492
CP ↑	min_pulse_width to CP	0.0315	0.0361	0.0302
D ↓	hold_rising to CP	-0.0142	-0.0142	-0.0142
D ↑	hold_rising to CP	-0.0045	-0.0045	-0.0045
D ↓	setup_rising to CP	0.0489	0.0489	0.0522
D ↑	setup_rising to CP	0.0319	0.0319	0.0319
E ↓	hold_rising to CP	-0.0089	-0.0089	-0.0089
E ↑	hold_rising to CP	-0.0039	-0.0039	-0.0039
E ↓	setup_rising to CP	0.0560	0.0560	0.0560
E ↑	setup_rising to CP	0.0564	0.0564	0.0564

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	1.895e-06	1.000e-20
X17_P10	2.221e-06	1.000e-20
X33_P10	3.272e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

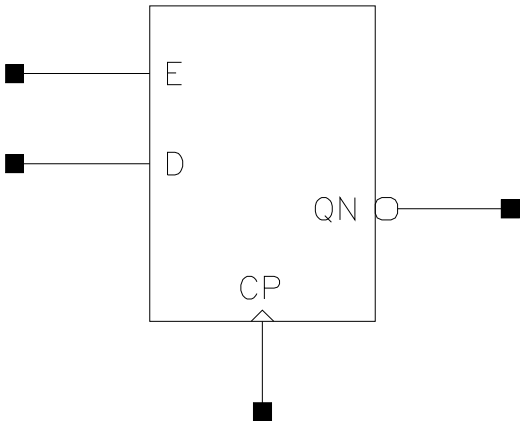
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	8.241e-03	8.244e-03	8.252e-03
Clock 100Mhz Data 25Mhz	1.085e-02	1.162e-02	1.444e-02
Clock 100Mhz Data 50Mhz	1.346e-02	1.500e-02	2.063e-02
Clock = 0 Data 100Mhz	5.279e-03	5.280e-03	5.280e-03
Clock = 1 Data 100Mhz	1.455e-03	1.455e-03	1.455e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.264	3.9168
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0012	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0654	0.0617	1.8604	0.8914
CP to QN ↑	0.0507	0.0520	2.7289	1.3068
	X33_P10		**X33_P10**	
CP to QN ↓	0.0660		0.4641	
CP to QN ↑	0.0572		0.6710	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0492	0.0492	0.0492
CP ↑	min_pulse_width to CP	0.0267	0.0314	0.0347
D ↓	hold_rising to CP	-0.0142	-0.0142	-0.0142
D ↑	hold_rising to CP	-0.0045	-0.0045	-0.0045
D ↓	setup_rising to CP	0.0522	0.0489	0.0522
D ↑	setup_rising to CP	0.0319	0.0319	0.0319
E ↓	hold_rising to CP	-0.0089	-0.0089	-0.0089
E ↑	hold_rising to CP	-0.0039	-0.0039	-0.0039
E ↓	setup_rising to CP	0.0560	0.0560	0.0560
E ↑	setup_rising to CP	0.0564	0.0564	0.0564

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	1.877e-06	1.000e-20
X17_P10	2.448e-06	1.000e-20
X33_P10	3.188e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

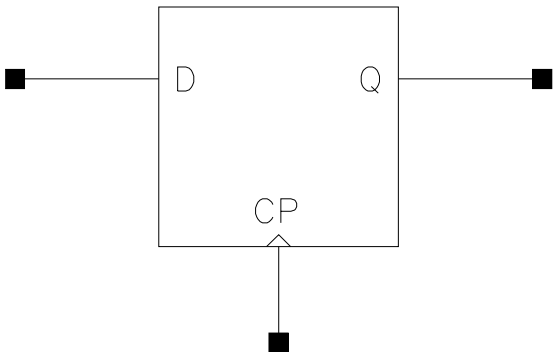
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	8.232e-03	8.235e-03	8.238e-03
Clock 100Mhz Data 25Mhz	1.089e-02	1.215e-02	1.423e-02
Clock 100Mhz Data 50Mhz	1.356e-02	1.606e-02	2.022e-02
Clock = 0 Data 100Mhz	5.284e-03	5.282e-03	5.282e-03
Clock = 1 Data 100Mhz	1.455e-03	1.455e-03	1.455e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.176	2.6112
X17_P10	1.200	2.448	2.9376
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0398	0.0439	1.7977	0.9252
CP to Q ↑	0.0476	0.0529	2.6051	1.3239
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to Q ↓	0.0554	0.0574	0.5513	0.5002
CP to Q ↑	0.0602	0.0613	0.7519	0.6817

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0431	0.0444	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0315	0.0361	0.0455	0.0468
D ↓	hold_rising to CP	0.0102	0.0107	0.0107	0.0107
D ↑	hold_rising to CP	0.0097	0.0098	0.0098	0.0098
D ↓	setup_rising to CP	0.0273	0.0272	0.0272	0.0272
D ↑	setup_rising to CP	0.0142	0.0142	0.0142	0.0142

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	1.480e-06	1.000e-20
X17_P10	1.843e-06	1.000e-20
X30_P10	2.344e-06	1.000e-20
X33_P10	2.471e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

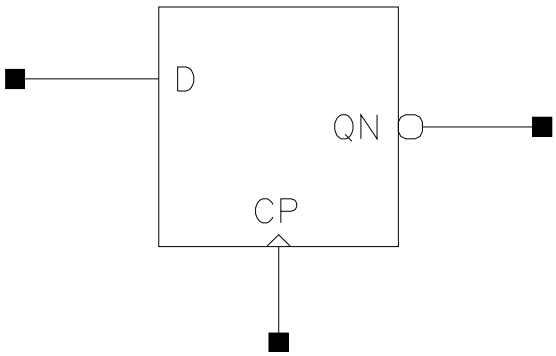
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	8.653e-03	8.714e-03	8.733e-03	8.742e-03
Clock 100Mhz Data 25Mhz	9.948e-03	1.109e-02	1.290e-02	1.331e-02
Clock 100Mhz Data 50Mhz	1.124e-02	1.347e-02	1.707e-02	1.788e-02
Clock = 0 Data 100Mhz	3.574e-03	3.680e-03	3.713e-03	3.730e-03
Clock = 1 Data 100Mhz	2.538e-05	2.531e-05	2.539e-05	2.543e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0389	0.0459	1.8582	0.9574
CP to QN ↑	0.0410	0.0436	2.5982	1.3258
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to QN ↓	0.0655	0.0661	0.5101	0.4632
CP to QN ↑	0.0534	0.0614	0.7229	0.6700

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0417	0.0431	0.0444	0.0431
CP ↑	min_pulse_width to CP	0.0314	0.0361	0.0314	0.0361
D ↓	hold_rising to CP	0.0124	0.0124	0.0107	0.0102
D ↑	hold_rising to CP	0.0124	0.0124	0.0098	0.0097
D ↓	setup_rising to CP	0.0197	0.0197	0.0272	0.0273
D ↑	setup_rising to CP	0.0168	0.0168	0.0142	0.0142

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	1.378e-06	1.000e-20
X17_P10	1.708e-06	1.000e-20
X30_P10	2.621e-06	1.000e-20
X33_P10	2.778e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

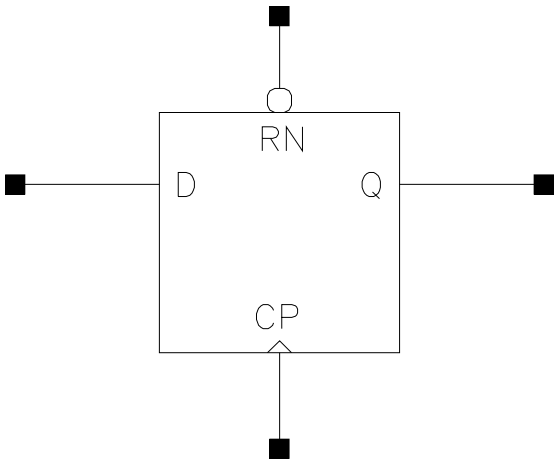
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	8.325e-03	8.327e-03	8.469e-03	8.528e-03
Clock 100Mhz Data 25Mhz	9.470e-03	1.032e-02	1.267e-02	1.330e-02
Clock 100Mhz Data 50Mhz	1.061e-02	1.231e-02	1.688e-02	1.808e-02
Clock = 0 Data 100Mhz	3.122e-03	3.123e-03	3.342e-03	3.401e-03
Clock = 1 Data 100Mhz	2.517e-05	2.522e-05	2.543e-05	2.554e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0010
D	0.0008	0.0008
RN	0.0010	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0458	0.0574	0.9345	0.5599
CP to Q ↑	0.0544	0.0615	1.3304	0.7554
RN to Q ↓	0.0738	0.0989	0.9816	0.5874

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0361	0.0468
D ↓	hold_rising to CP	0.0075	0.0107
D ↑	hold_rising to CP	0.0107	0.0107
D ↓	setup_rising to CP	0.0294	0.0294
D ↑	setup_rising to CP	0.0200	0.0200
RN ↓	min_pulse_width to RN	0.0925	0.1169
RN ↑	recovery_rising to CP	0.0173	0.0173
RN ↑	removal_rising to CP	-0.0050	-0.0050

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P10	2.077e-06	1.000e-20
X30_P10	2.641e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

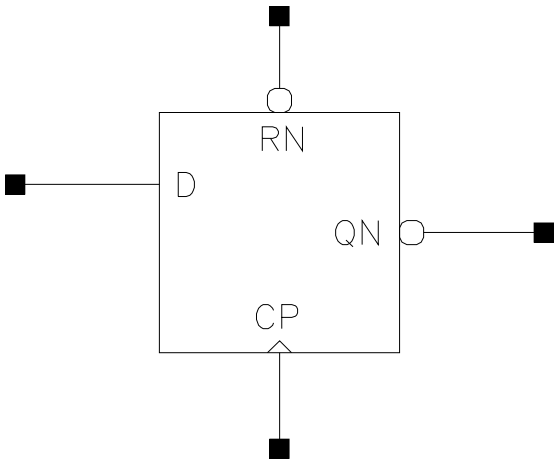
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	9.271e-03	9.268e-03
Clock 100Mhz Data 25Mhz	1.182e-02	1.361e-02
Clock 100Mhz Data 50Mhz	1.437e-02	1.796e-02
Clock = 0 Data 100Mhz	4.351e-03	4.355e-03
Clock = 1 Data 100Mhz	2.584e-05	2.594e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0010
D	0.0008	0.0008
RN	0.0010	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.0631	0.0681	0.8844	0.5118
CP to QN ↑	0.0519	0.0561	1.2958	0.7257
RN to QN ↑	0.0758	0.0811	1.3011	0.7293

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0478	0.0478
CP ↑	min_pulse_width to CP	0.0314	0.0314
D ↓	hold_rising to CP	0.0075	0.0075
D ↑	hold_rising to CP	0.0107	0.0107
D ↓	setup_rising to CP	0.0294	0.0294
D ↑	setup_rising to CP	0.0200	0.0200
RN ↓	min_pulse_width to RN	0.0730	0.0779
RN ↑	recovery_rising to CP	0.0173	0.0173
RN ↑	removal_rising to CP	-0.0050	-0.0054

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P10	2.268e-06	1.000e-20
X30_P10	2.697e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

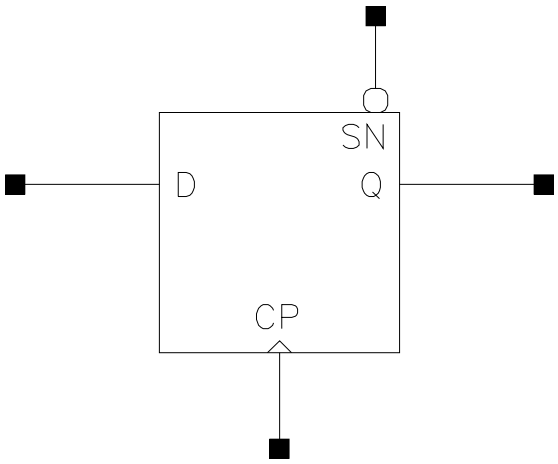
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	9.271e-03	9.270e-03
Clock 100Mhz Data 25Mhz	1.230e-02	1.372e-02
Clock 100Mhz Data 50Mhz	1.534e-02	1.816e-02
Clock = 0 Data 100Mhz	4.404e-03	4.389e-03
Clock = 1 Data 100Mhz	2.585e-05	2.590e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0010
D	0.0008	0.0008
SN	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0459	0.0574	0.9361	0.5558
CP to Q ↑	0.0539	0.0609	1.3312	0.7551
SN to Q ↑	0.0540	0.0629	1.3341	0.7558

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0525	0.0525
CP ↑	min_pulse_width to CP	0.0361	0.0468
D ↓	hold_rising to CP	0.0075	0.0075
D ↑	hold_rising to CP	0.0107	0.0102
D ↓	setup_rising to CP	0.0317	0.0321
D ↑	setup_rising to CP	0.0168	0.0168
SN ↓	min_pulse_width to SN	0.0527	0.0625
SN ↑	recovery_rising to CP	0.0054	0.0054
SN ↑	removal_rising to CP	0.0238	0.0238

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P10	1.967e-06	1.000e-20
X30_P10	2.400e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

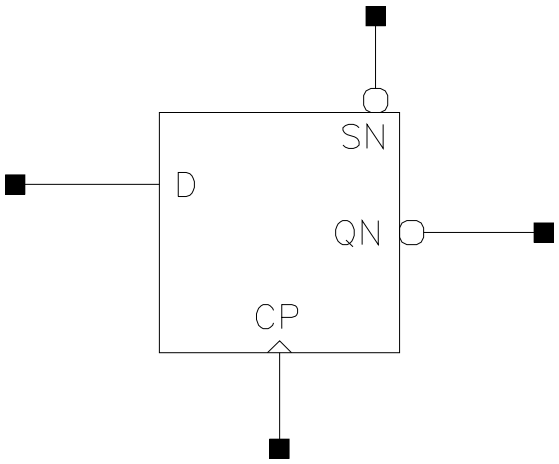
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	9.361e-03	9.342e-03
Clock 100Mhz Data 25Mhz	1.190e-02	1.362e-02
Clock 100Mhz Data 50Mhz	1.444e-02	1.789e-02
Clock = 0 Data 100Mhz	4.317e-03	4.316e-03
Clock = 1 Data 100Mhz	2.519e-05	2.528e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0010
D	0.0008	0.0008
SN	0.0013	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.0626	0.0676	0.8874	0.5133
CP to QN ↑	0.0521	0.0561	1.2924	0.7246
SN to QN ↓	0.0620	0.0673	0.8864	0.5135

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0525	0.0525
CP ↑	min_pulse_width to CP	0.0314	0.0314
D ↓	hold_rising to CP	0.0075	0.0075
D ↑	hold_rising to CP	0.0107	0.0107
D ↓	setup_rising to CP	0.0317	0.0317
D ↑	setup_rising to CP	0.0168	0.0168
SN ↓	min_pulse_width to SN	0.0452	0.0474
SN ↑	recovery_rising to CP	0.0054	0.0054
SN ↑	removal_rising to CP	0.0238	0.0238

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P10	2.349e-06	1.000e-20
X30_P10	2.903e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

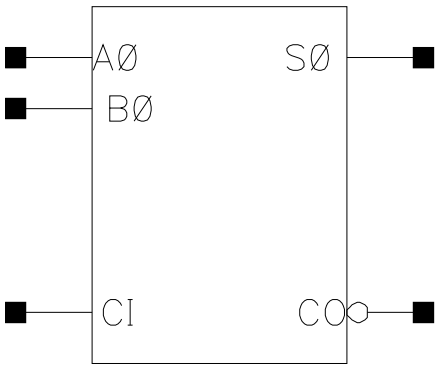
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	9.356e-03	9.351e-03
Clock 100Mhz Data 25Mhz	1.236e-02	1.376e-02
Clock 100Mhz Data 50Mhz	1.536e-02	1.817e-02
Clock = 0 Data 100Mhz	4.315e-03	4.316e-03
Clock = 1 Data 100Mhz	2.589e-05	2.596e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_P10	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_P10	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_P10	1.200	3.672	4.4064
C12T28SOI_LLS1_FA1X33_P10	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_FA1X8_P10	C12T28SOI_LL_FA1X33_P10	C12T28SOI_LLS1_FA1X8_P10	C12T28SOI_LLS1_FA1X33_P10
A0	0.0035	0.0071	0.0031	0.0061
B0	0.0032	0.0068	0.0034	0.0059
CI	0.0023	0.0053	0.0024	0.0042

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10
A0 to CO ↓	0.0423	0.0460	1.8770	0.4946
A0 to CO ↑	0.0321	0.0335	2.6952	0.6940
A0 to S0 ↓	0.0444	0.0557	1.8537	0.4828
A0 to S0 ↑	0.0454	0.0553	2.6579	0.6835
B0 to CO ↓	0.0417	0.0462	1.8823	0.4971
B0 to CO ↑	0.0331	0.0349	2.6974	0.6919
B0 to S0 ↓	0.0448	0.0567	1.8545	0.4826
B0 to S0 ↑	0.0455	0.0561	2.6591	0.6839
CI to CO ↓	0.0406	0.0454	1.8876	0.4963
CI to CO ↑	0.0328	0.0341	2.6965	0.6945
CI to S0 ↓	0.0443	0.0562	1.8547	0.4827
CI to S0 ↑	0.0456	0.0565	2.6576	0.6835
	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10
A0 to CO ↓	0.0280	0.0342	3.6522	0.6309
A0 to CO ↑	0.0246	0.0284	2.7371	0.6861
A0 to S0 ↓	0.0584	0.0720	2.0064	0.5053
A0 to S0 ↑	0.0534	0.0581	2.7693	0.6959
B0 to CO ↓	0.0288	0.0355	3.6537	0.6317
B0 to CO ↑	0.0228	0.0272	2.7353	0.6861
B0 to S0 ↓	0.0587	0.0739	2.0062	0.5052
B0 to S0 ↑	0.0537	0.0598	2.7695	0.6960
CI to CO ↓	0.0285	0.0489	3.6471	0.6394
CI to CO ↑	0.0252	0.0308	2.8144	0.6917
CI to S0 ↓	0.0342	0.0447	2.0078	0.5057
CI to S0 ↑	0.0293	0.0297	2.7700	0.6967

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_FA1X8_P10	1.985e-06	1.000e-20
C12T28SOI_LL_FA1X33_P10	5.212e-06	1.000e-20
C12T28SOI_LLS1_FA1X8_P10	3.998e-06	1.000e-20
C12T28SOI_LLS1_FA1X33_P10	8.400e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10
A0 to CO	4.041e-03	1.144e-02	6.149e-03	1.538e-02
A0 to S0	4.094e-03	1.192e-02	8.258e-03	1.912e-02
B0 to CO	4.037e-03	1.154e-02	6.189e-03	1.559e-02
B0 to S0	3.923e-03	1.167e-02	8.350e-03	1.943e-02
CI to CO	3.998e-03	1.152e-02	4.371e-03	1.381e-02
CI to S0	3.881e-03	1.162e-02	4.951e-03	1.486e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X33_P10	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X33_P10
A0	0.0012	0.0035
B0	0.0010	0.0030

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
A0 to CO ↓	0.0327	0.0298	1.8569	0.4615
A0 to CO ↑	0.0296	0.0271	2.6619	0.6873
A0 to S0 ↓	0.0419	0.0398	1.8162	0.4612
A0 to S0 ↑	0.0400	0.0445	2.6244	0.6775
B0 to CO ↓	0.0317	0.0274	1.8574	0.4579
B0 to CO ↑	0.0318	0.0283	2.6634	0.6873
B0 to S0 ↓	0.0434	0.0397	1.8176	0.4613
B0 to S0 ↑	0.0394	0.0425	2.6236	0.6778

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	1.136e-06	1.000e-20
X33_P10	4.837e-06	1.000e-20

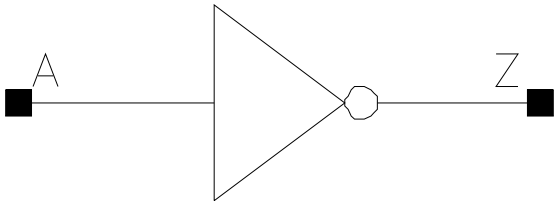
Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X33_P10
A0 to CO	3.115e-03	1.017e-02
A0 to S0	2.865e-03	9.865e-03
B0 to CO	3.135e-03	1.015e-02
B0 to S0	2.806e-03	9.459e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X8_P10	X33_P10
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.272	0.3264
X6_P10	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X13_P10	1.200	0.408	0.4896
X17_P10	1.200	0.408	0.4896
X21_P10	1.200	0.544	0.6528
X25_P10	1.200	0.544	0.6528
X29_P10	1.200	0.680	0.8160
X33_P10	1.200	0.680	0.8160
X50_P10	1.200	0.952	1.1424
X58_P10	1.200	1.088	1.3056
X67_P10	1.200	1.224	1.4688
X75_P10	1.200	1.360	1.6320
X84_P10	1.200	1.496	1.7952
X100_P10	1.200	1.768	2.1216
X134_P10	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0006	0.0007	0.0009	0.0014
	X17_P10	X21_P10	X25_P10	X29_P10
A	0.0018	0.0023	0.0026	0.0031
	X33_P10	X50_P10	X58_P10	X67_P10
A	0.0034	0.0052	0.0061	0.0070
	X75_P10	X84_P10	X100_P10	X134_P10

A	0.0080	0.0090	0.0111	0.0154

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0074	0.0070	3.4872	2.6794
A to Z ↑	0.0120	0.0110	5.2659	3.9441
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0063	0.0054	1.8410	1.1929
A to Z ↑	0.0099	0.0091	2.7060	1.7955
	X17_P10	**X21_P10**	**X17_P10**	**X21_P10**
A to Z ↓	0.0054	0.0059	0.9150	0.7380
A to Z ↑	0.0085	0.0092	1.3319	1.0785
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0058	0.0055	0.6279	0.5321
A to Z ↑	0.0088	0.0085	0.8969	0.7698
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0054	0.0057	0.4721	0.3187
A to Z ↑	0.0081	0.0083	0.6725	0.4502
	X58_P10	**X67_P10**	**X58_P10**	**X67_P10**
A to Z ↓	0.0059	0.0058	0.2766	0.2432
A to Z ↑	0.0084	0.0083	0.3882	0.3406
	X75_P10	**X84_P10**	**X75_P10**	**X84_P10**
A to Z ↓	0.0062	0.0064	0.2200	0.1990
A to Z ↑	0.0086	0.0088	0.3057	0.2768
	X100_P10	**X134_P10**	**X100_P10**	**X134_P10**
A to Z ↓	0.0072	0.0079	0.1695	0.1326
A to Z ↑	0.0095	0.0102	0.2337	0.1805

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.526e-07	1.000e-20
X6_P10	2.195e-07	1.000e-20
X8_P10	3.573e-07	1.000e-20
X13_P10	4.982e-07	1.000e-20
X17_P10	7.219e-07	1.000e-20
X21_P10	8.327e-07	1.000e-20
X25_P10	1.039e-06	1.000e-20
X29_P10	1.164e-06	1.000e-20
X33_P10	1.350e-06	1.000e-20
X50_P10	1.973e-06	1.000e-20
X58_P10	2.285e-06	1.000e-20
X67_P10	2.597e-06	1.000e-20
X75_P10	2.909e-06	1.000e-20
X84_P10	3.221e-06	1.000e-20
X100_P10	3.845e-06	1.000e-20
X134_P10	5.093e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10

A to Z	4.948e-04	6.019e-04	7.800e-04	1.062e-03
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	1.363e-03	1.841e-03	2.135e-03	2.352e-03
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	2.564e-03	3.888e-03	4.696e-03	5.112e-03
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	5.870e-03	6.473e-03	8.037e-03	1.106e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

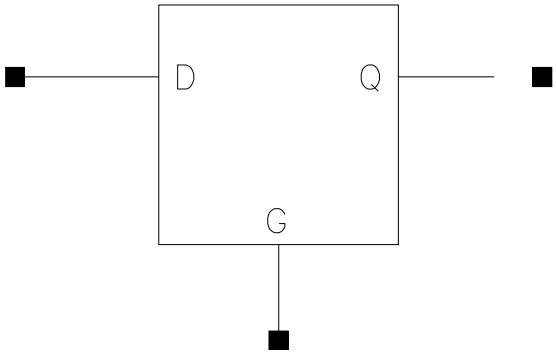
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X23_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P10	X23_P10
D	0.0006	0.0015
G	0.0013	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X23_P10	X8_P10	X23_P10
D to Q ↓	0.0477	0.0380	1.8792	0.8874
D to Q ↑	0.0316	0.0319	2.6240	0.7008
G to Q ↓	0.0499	0.0399	1.8763	0.8872
G to Q ↑	0.0308	0.0285	2.6219	0.7022

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P10	X23_P10
D ↓	hold_falling to G	-0.0094	-0.0023
D ↑	hold_falling to G	-0.0003	-0.0003
D ↓	setup_falling to G	0.0463	0.0318
D ↑	setup_falling to G	0.0351	0.0403
G ↑	min_pulse_width to G	0.0451	0.0439

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	8.170e-07	1.000e-20
X23_P10	1.992e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X23_P10
D (output stable)	1.763e-05	7.680e-05
G (output stable)	1.033e-03	2.029e-03
D to Q	4.889e-03	9.615e-03
G to Q	4.467e-03	8.509e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

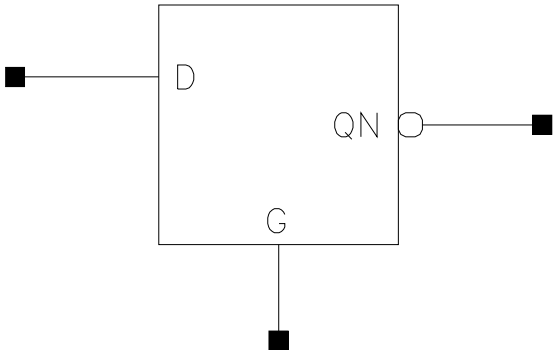
Pin Cycle (vdds)	X8_P10	X23_P10
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P10
D	0.0006
G	0.0015

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P10	X17_P10
D to QN ↓	0.0416	0.8885
D to QN ↑	0.0531	1.2851
G to QN ↓	0.0402	0.8885
G to QN ↑	0.0533	1.2865

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X17_P10
D ↓	hold_falling to G	-0.0116
D ↑	hold_falling to G	-0.0035
D ↓	setup_falling to G	0.0392
D ↑	setup_falling to G	0.0286
G ↑	min_pulse_width to G	0.0329

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P10	1.322e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X17_P10
D (output stable)	2.030e-05
G (output stable)	1.173e-03
D to QN	6.228e-03
G to QN	5.681e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

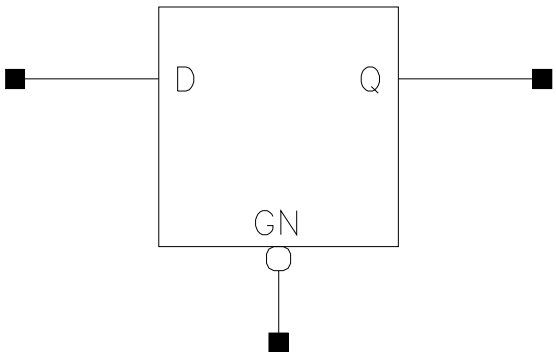
Pin Cycle (vdds)	X17_P10
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
D	0.0006	0.0008	0.0019
GN	0.0012	0.0015	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D to Q ↓	0.0482	0.0416	1.8869	0.9293
D to Q ↑	0.0322	0.0305	2.6229	1.3470
GN to Q ↓	0.0437	0.0373	1.8877	0.9306
GN to Q ↑	0.0464	0.0444	2.6220	1.3455

	X33_P10		X33_P10	
D to Q ↓	0.0404		0.4757	
D to Q ↑	0.0263		0.6754	
GN to Q ↓	0.0353		0.4765	
GN to Q ↑	0.0346		0.6751	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X33_P10
D ↓	hold_rising to GN	-0.0117	-0.0068	-0.0068
D ↑	hold_rising to GN	0.0032	0.0027	0.0085
D ↓	setup_rising to GN	0.0516	0.0472	0.0446
D ↑	setup_rising to GN	0.0319	0.0265	0.0244
GN ↓	min_pulse_width to GN	0.0588	0.0511	0.0467

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	8.156e-07	1.000e-20
X17_P10	1.352e-06	1.000e-20
X33_P10	2.365e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
D (output stable)	1.851e-05	3.007e-05	8.035e-05
GN (output stable)	1.029e-03	1.408e-03	1.765e-03
D to Q	4.907e-03	6.950e-03	1.129e-02
GN to Q	6.935e-03	9.507e-03	1.409e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

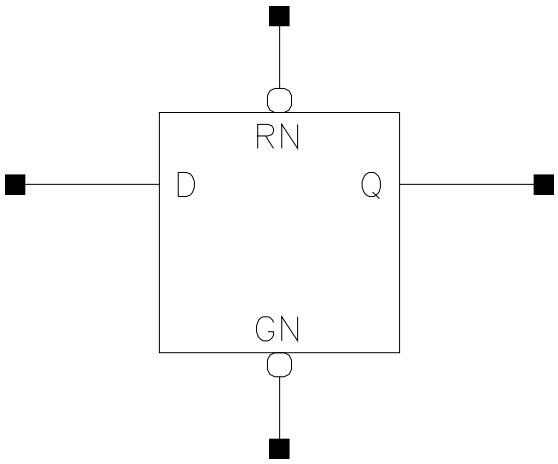
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.496	1.7952
X33_P10	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X33_P10
D	0.0006	0.0015
GN	0.0014	0.0025
RN	0.0006	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
D to Q ↓	0.0452	0.0407	1.8408	0.4786
D to Q ↑	0.0413	0.0529	2.6820	0.7007

GN to Q ↓	0.0414	0.0378	1.8432	0.4794
GN to Q ↑	0.0528	0.0550	2.6820	0.7005
RN to Q ↓	0.0374	0.0689	1.7837	0.5159
RN to Q ↑	0.0433	0.0579	2.6831	0.7006

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P10	X33_P10
D ↓	hold_rising to GN	-0.0096	-0.0047
D ↑	hold_rising to GN	-0.0071	-0.0159
D ↓	setup_rising to GN	0.0468	0.0420
D ↑	setup_rising to GN	0.0416	0.0615
GN ↓	min_pulse_width to GN	0.0543	0.0576
RN ↓	min_pulse_width to RN	0.0469	0.0806
RN ↑	recovery_rising to GN	0.0443	0.0632
RN ↑	removal_rising to GN	-0.0266	-0.0440

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	9.287e-07	1.000e-20
X33_P10	2.429e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X33_P10
D (output stable)	7.350e-05	8.644e-05
GN (output stable)	1.193e-03	1.825e-03
RN (output stable)	2.458e-05	4.748e-05
D to Q	4.904e-03	1.269e-02
GN to Q	7.083e-03	1.600e-02
RN to Q	3.874e-03	1.008e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

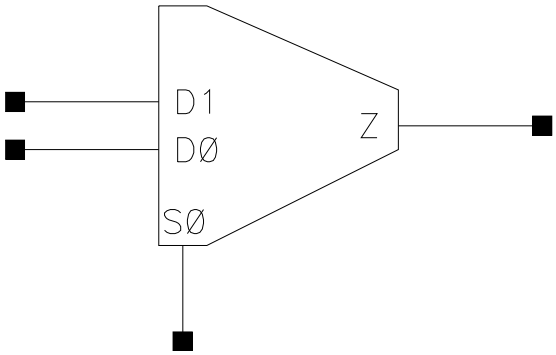
Pin Cycle (vdds)	X8_P10	X33_P10
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
D0	0.0008	0.0012	0.0015	0.0022
D1	0.0008	0.0012	0.0015	0.0021
S0	0.0014	0.0016	0.0018	0.0027

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D0 to Z ↓	0.0374	0.0331	1.8508	0.9081
D0 to Z ↑	0.0299	0.0275	2.6906	1.3148
D1 to Z ↓	0.0356	0.0327	1.8461	0.9065
D1 to Z ↑	0.0273	0.0260	2.6859	1.3132
S0 to Z ↓	0.0324	0.0313	1.8419	0.9043
S0 to Z ↑	0.0305	0.0307	2.6841	1.3136

	X25_P10	X33_P10	X25_P10	X33_P10
D0 to Z ↓	0.0357	0.0320	0.6257	0.4697
D0 to Z ↑	0.0294	0.0273	0.8846	0.6630
D1 to Z ↓	0.0382	0.0333	0.6284	0.4705
D1 to Z ↑	0.0283	0.0263	0.8843	0.6630
S0 to Z ↓	0.0360	0.0329	0.6255	0.4688
S0 to Z ↑	0.0341	0.0312	0.8840	0.6627

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	9.410e-07	1.000e-20
X17_P10	1.850e-06	1.000e-20
X25_P10	2.387e-06	1.000e-20
X33_P10	3.647e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	9.033e-04	1.348e-03	1.481e-03	2.039e-03
D1 (output stable)	7.444e-04	1.252e-03	1.644e-03	2.129e-03
S0 (output stable)	1.203e-03	1.376e-03	1.796e-03	2.217e-03
D0 to Z	3.346e-03	5.476e-03	8.520e-03	1.072e-02
D1 to Z	3.086e-03	5.319e-03	8.591e-03	1.057e-02
S0 to Z	3.820e-03	5.845e-03	9.527e-03	1.168e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

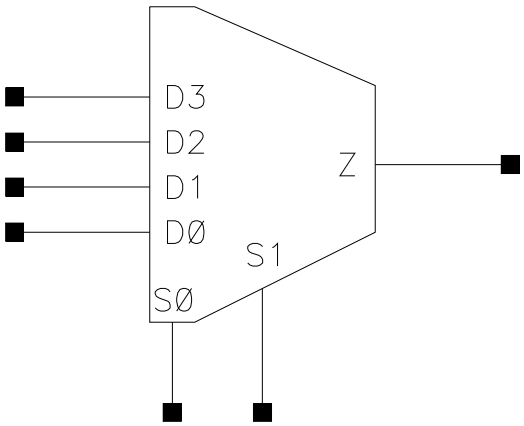
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.312	2.7744
X31_P10	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P10	X31_P10
D0	0.0006	0.0016
D1	0.0006	0.0016
D2	0.0006	0.0016
D3	0.0006	0.0016
S0	0.0021	0.0041
S1	0.0013	0.0026

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X31_P10	X8_P10	X31_P10

D0 to Z ↓	0.0628	0.0642	1.9298	0.5367
D0 to Z ↑	0.0424	0.0450	2.7109	0.7329
D1 to Z ↓	0.0623	0.0642	1.9281	0.5371
D1 to Z ↑	0.0426	0.0449	2.7108	0.7329
D2 to Z ↓	0.0671	0.0605	1.9393	0.5321
D2 to Z ↑	0.0447	0.0415	2.7185	0.7284
D3 to Z ↓	0.0669	0.0599	1.9389	0.5313
D3 to Z ↑	0.0442	0.0430	2.7149	0.7317
S0 to Z ↓	0.0688	0.0701	1.9307	0.5336
S0 to Z ↑	0.0520	0.0553	2.7148	0.7322
S1 to Z ↓	0.0497	0.0493	1.9334	0.5339
S1 to Z ↑	0.0401	0.0423	2.7126	0.7315

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	1.000e-06	1.000e-20
X31_P10	3.234e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X31_P10
D0 (output stable)	3.885e-05	1.549e-04
D1 (output stable)	3.896e-05	1.708e-04
D2 (output stable)	2.615e-05	6.769e-05
D3 (output stable)	4.019e-05	1.476e-04
S0 (output stable)	1.860e-03	4.284e-03
S1 (output stable)	1.261e-03	2.739e-03
D0 to Z	3.675e-03	1.252e-02
D1 to Z	3.666e-03	1.255e-02
D2 to Z	3.927e-03	1.175e-02
D3 to Z	3.914e-03	1.174e-02
S0 to Z	5.741e-03	1.696e-02
S1 to Z	4.082e-03	1.175e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

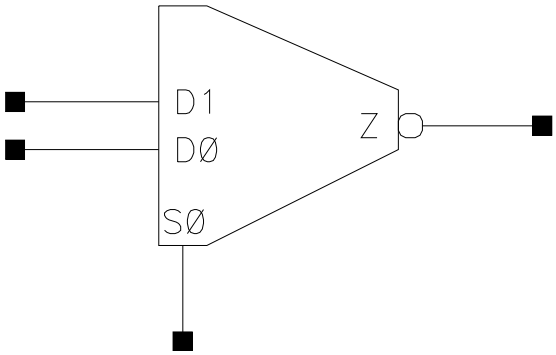
Pin Cycle (vdds)	X8_P10	X31_P10
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.816	0.9792
X5_P10	1.200	0.952	1.1424
X10_P10	1.200	1.768	2.1216
X16_P10	1.200	2.448	2.9376
X21_P10	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P10	X5_P10	X10_P10	X16_P10
D0	0.0006	0.0009	0.0018	0.0028
D1	0.0006	0.0009	0.0018	0.0027
S0	0.0012	0.0021	0.0028	0.0043
	X21_P10			
D0	0.0037			
D1	0.0036			
S0	0.0048			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X5_P10**	**X3_P10**	**X5_P10**
D0 to Z ↓	0.0133	0.0134	5.8419	3.6585

D0 to Z ↑	0.0217	0.0192	10.9966	5.6051
D1 to Z ↓	0.0130	0.0128	5.8014	3.4651
D1 to Z ↑	0.0224	0.0202	11.0091	5.8385
S0 to Z ↓	0.0197	0.0165	5.8088	3.5619
S0 to Z ↑	0.0211	0.0175	10.9832	5.7144
	X10_P10	**X16_P10**	**X10_P10**	**X16_P10**
D0 to Z ↓	0.0150	0.0140	1.7248	1.1270
D0 to Z ↑	0.0209	0.0200	2.6169	1.7253
D1 to Z ↓	0.0136	0.0135	1.6652	1.0981
D1 to Z ↑	0.0211	0.0205	2.6642	1.7455
S0 to Z ↓	0.0201	0.0174	1.6929	1.1124
S0 to Z ↑	0.0208	0.0180	2.6405	1.7358
	X21_P10		**X21_P10**	
D0 to Z ↓	0.0139		0.8617	
D0 to Z ↑	0.0197		1.3094	
D1 to Z ↓	0.0134		0.8336	
D1 to Z ↑	0.0206		1.3026	
S0 to Z ↓	0.0183		0.8472	
S0 to Z ↑	0.0186		1.3051	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	3.396e-07	1.000e-20
X5_P10	8.358e-07	1.000e-20
X10_P10	1.516e-06	1.000e-20
X16_P10	2.408e-06	1.000e-20
X21_P10	2.965e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	1.873e-05	3.944e-05	1.511e-04	2.170e-04
D1 (output stable)	2.053e-05	9.304e-05	9.856e-05	1.674e-04
S0 (output stable)	1.030e-03	1.517e-03	2.658e-03	4.123e-03
D0 to Z	1.010e-03	1.684e-03	4.189e-03	5.916e-03
D1 to Z	1.005e-03	1.671e-03	3.976e-03	5.829e-03
S0 to Z	1.749e-03	2.534e-03	5.257e-03	7.431e-03
	X21_P10			
D0 (output stable)	2.758e-04			
D1 (output stable)	2.483e-04			
S0 (output stable)	4.614e-03			
D0 to Z	7.642e-03			
D1 to Z	7.684e-03			
S0 to Z	9.106e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

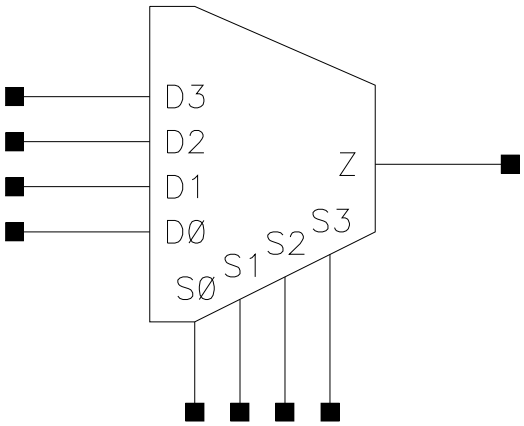
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P10			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	1.768	2.1216
X27_P10	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P10	X27_P10
D0	0.0007	0.0022
D1	0.0007	0.0022
D2	0.0007	0.0022
D3	0.0007	0.0022
S0	0.0007	0.0020
S1	0.0008	0.0021
S2	0.0007	0.0021
S3	0.0008	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	X27_P10	X7_P10	X27_P10
D0 to Z ↓	0.0484	0.0408	3.0251	0.8305
D0 to Z ↑	0.0353	0.0306	2.6371	0.6582
D1 to Z ↓	0.0445	0.0378	3.0231	0.8305
D1 to Z ↑	0.0317	0.0268	2.6269	0.6560
D2 to Z ↓	0.0489	0.0389	3.0327	0.8316
D2 to Z ↑	0.0345	0.0286	2.6490	0.6612
D3 to Z ↓	0.0451	0.0359	3.0276	0.8305
D3 to Z ↑	0.0310	0.0249	2.6407	0.6585
S0 to Z ↓	0.0467	0.0385	3.0250	0.8306
S0 to Z ↑	0.0378	0.0323	2.6368	0.6585
S1 to Z ↓	0.0430	0.0354	3.0234	0.8304
S1 to Z ↑	0.0339	0.0281	2.6282	0.6555
S2 to Z ↓	0.0472	0.0366	3.0315	0.8311
S2 to Z ↑	0.0370	0.0303	2.6480	0.6612
S3 to Z ↓	0.0437	0.0336	3.0267	0.8304
S3 to Z ↑	0.0332	0.0262	2.6376	0.6584

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X7_P10	9.291e-07	1.000e-20
X27_P10	3.948e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X7_P10	X27_P10
D0 (output stable)	5.570e-04	1.775e-03
D1 (output stable)	4.430e-04	1.381e-03
D2 (output stable)	5.320e-04	1.676e-03
D3 (output stable)	4.130e-04	1.285e-03
S0 (output stable)	5.656e-04	1.739e-03
S1 (output stable)	4.374e-04	1.359e-03
S2 (output stable)	5.121e-04	1.604e-03
S3 (output stable)	3.991e-04	1.243e-03
D0 to Z	4.257e-03	1.341e-02
D1 to Z	3.736e-03	1.155e-02
D2 to Z	4.091e-03	1.165e-02
D3 to Z	3.576e-03	9.820e-03
S0 to Z	4.135e-03	1.270e-02
S1 to Z	3.613e-03	1.090e-02
S2 to Z	3.965e-03	1.093e-02
S3 to Z	3.456e-03	9.181e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

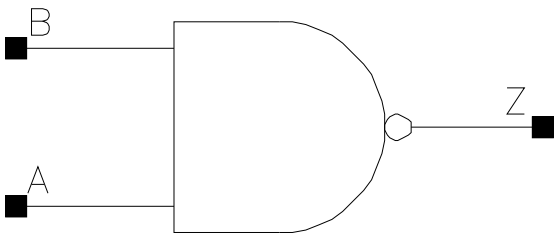
Pin Cycle (vdds)	X7_P10	X27_P10
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P10	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P10	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P10	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P10	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P10	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P10	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P10	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P10	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P10	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P10	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P10	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P10	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P10	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P10	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P10	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P10	C12T28SOI_LL_-NAND2X5_P10	C12T28SOI_LL_-NAND2X7_P10	C12T28SOI_LL_-NAND2X10_P10
A	0.0006	0.0008	0.0009	0.0015
B	0.0006	0.0008	0.0009	0.0014
	C12T28SOI_LL_-NAND2X13_P10	C12T28SOI_LL_-NAND2X17_P10	C12T28SOI_LL_-NAND2X20_P10	C12T28SOI_LL_-NAND2X24_P10
A	0.0018	0.0023	0.0027	0.0032
B	0.0017	0.0022	0.0025	0.0030
	C12T28SOI_LL_-NAND2X27_P10	C12T28SOI_LL_-NAND2X42_P10	C12T28SOI_LL_-NAND2X47_P10	C12T28SOI_LL_-NAND2X50_P10
A	0.0036	0.0011	0.0011	0.0011
B	0.0033	0.0012	0.0012	0.0012
	C12T28SOI_LL_-NAND2X58_P10	C12T28SOI_LL_-NAND2X67_P10	C12T28SOI_-LLBR0D8_-NAND2X7_P10	C12T28SOI_-LLBR0D8_-NAND2X14_P10
A	0.0011	0.0011	0.0009	0.0018
B	0.0012	0.0012	0.0009	0.0017
	C12T28SOI_LLS_-NAND2X40_P10	C12T28SOI_LLS_-NAND2X54_P10		
A	0.0053	0.0071		
B	0.0049	0.0066		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P10	**C12T28SOI_LL_-NAND2X5_P10**	**C12T28SOI_LL_-NAND2X3_P10**	**C12T28SOI_LL_-NAND2X5_P10**
A to Z ↓	0.0100	0.0092	5.7094	3.7118
A to Z ↑	0.0145	0.0131	5.2866	3.3522
B to Z ↓	0.0108	0.0096	5.7892	3.7610
B to Z ↑	0.0130	0.0113	5.3258	3.3770
	C12T28SOI_LL_-NAND2X7_P10	**C12T28SOI_LL_-NAND2X10_P10**	**C12T28SOI_LL_-NAND2X7_P10**	**C12T28SOI_LL_-NAND2X10_P10**
A to Z ↓	0.0091	0.0105	3.1154	2.0644
A to Z ↑	0.0127	0.0137	2.6953	1.7782
B to Z ↓	0.0095	0.0094	3.1503	2.0930
B to Z ↑	0.0108	0.0108	2.7187	1.7935
	C12T28SOI_LL_-NAND2X13_P10	**C12T28SOI_LL_-NAND2X17_P10**	**C12T28SOI_LL_-NAND2X13_P10**	**C12T28SOI_LL_-NAND2X17_P10**
A to Z ↓	0.0101	0.0100	1.5959	1.2685

A to Z ↑	0.0128	0.0131	1.3244	1.0739
B to Z ↓	0.0089	0.0096	1.6175	1.2855
B to Z ↑	0.0099	0.0106	1.3366	1.0829
	C12T28SOI_LL_-NAND2X20_P10	**C12T28SOI_LL_-NAND2X24_P10**	**C12T28SOI_LL_-NAND2X20_P10**	**C12T28SOI_LL_-NAND2X24_P10**
A to Z ↓	0.0098	0.0102	1.0918	0.9269
A to Z ↑	0.0126	0.0129	0.8922	0.7650
B to Z ↓	0.0096	0.0093	1.1058	0.9391
B to Z ↑	0.0102	0.0101	0.9014	0.7718
	C12T28SOI_LL_-NAND2X27_P10	**C12T28SOI_LL_-NAND2X42_P10**	**C12T28SOI_LL_-NAND2X27_P10**	**C12T28SOI_LL_-NAND2X42_P10**
A to Z ↓	0.0100	0.0349	0.8287	0.3732
A to Z ↑	0.0126	0.0357	0.6691	0.5228
B to Z ↓	0.0091	0.0362	0.8400	0.3731
B to Z ↑	0.0097	0.0342	0.6753	0.5233
	C12T28SOI_LL_-NAND2X47_P10	**C12T28SOI_LL_-NAND2X50_P10**	**C12T28SOI_LL_-NAND2X47_P10**	**C12T28SOI_LL_-NAND2X50_P10**
A to Z ↓	0.0359	0.0364	0.3314	0.3114
A to Z ↑	0.0363	0.0367	0.4567	0.4367
B to Z ↓	0.0372	0.0376	0.3314	0.3112
B to Z ↑	0.0348	0.0352	0.4559	0.4374
	C12T28SOI_LL_-NAND2X58_P10	**C12T28SOI_LL_-NAND2X67_P10**	**C12T28SOI_LL_-NAND2X58_P10**	**C12T28SOI_LL_-NAND2X67_P10**
A to Z ↓	0.0379	0.0395	0.2703	0.2376
A to Z ↑	0.0379	0.0390	0.3766	0.3310
B to Z ↓	0.0392	0.0409	0.2700	0.2378
B to Z ↑	0.0364	0.0376	0.3760	0.3309
	C12T28SOI_-LLBR0D8_-NAND2X7_P10	**C12T28SOI_-LLBR0D8_-NAND2X14_P10**	**C12T28SOI_-LLBR0D8_-NAND2X7_P10**	**C12T28SOI_-LLBR0D8_-NAND2X14_P10**
A to Z ↓	0.0075	0.0087	2.3563	1.2450
A to Z ↑	0.0156	0.0158	3.5788	1.7489
B to Z ↓	0.0073	0.0068	2.4001	1.2713
B to Z ↑	0.0127	0.0115	3.7048	1.7886
	C12T28SOI_LLS_-NAND2X40_P10	**C12T28SOI_LLS_-NAND2X54_P10**	**C12T28SOI_LLS_-NAND2X40_P10**	**C12T28SOI_LLS_-NAND2X54_P10**
A to Z ↓	0.0099	0.0099	0.5620	0.4255
A to Z ↑	0.0124	0.0124	0.4486	0.3384
B to Z ↓	0.0091	0.0093	0.5697	0.4314
B to Z ↑	0.0096	0.0097	0.4531	0.3422

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P10	1.630e-07	1.000e-20
C12T28SOI_LL_NAND2X5_P10	2.987e-07	1.000e-20
C12T28SOI_LL_NAND2X7_P10	3.830e-07	1.000e-20
C12T28SOI_LL_NAND2X10_P10	5.164e-07	1.000e-20
C12T28SOI_LL_NAND2X13_P10	7.476e-07	1.000e-20
C12T28SOI_LL_NAND2X17_P10	8.734e-07	1.000e-20
C12T28SOI_LL_NAND2X20_P10	1.088e-06	1.000e-20
C12T28SOI_LL_NAND2X24_P10	1.231e-06	1.000e-20
C12T28SOI_LL_NAND2X27_P10	1.429e-06	1.000e-20

C12T28SOI_LL_NAND2X42_P10	2.460e-06	1.000e-20
C12T28SOI_LL_NAND2X47_P10	2.655e-06	1.000e-20
C12T28SOI_LL_NAND2X50_P10	2.704e-06	1.000e-20
C12T28SOI_LL_NAND2X58_P10	2.949e-06	1.000e-20
C12T28SOI_LL_NAND2X67_P10	3.194e-06	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_-P10	3.613e-07	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_-P10	6.882e-07	1.000e-20
C12T28SOI_LLS_NAND2X40_P10	2.112e-06	1.000e-20
C12T28SOI_LLS_NAND2X54_P10	2.795e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND2X3_P10	C12T28SOI_LL_-NAND2X5_P10	C12T28SOI_LL_-NAND2X7_P10	C12T28SOI_LL_-NAND2X10_P10
A (output stable)	1.242e-05	1.928e-05	2.367e-05	6.167e-05
B (output stable)	4.130e-05	6.463e-05	7.840e-05	3.552e-04
A to Z	7.079e-04	9.608e-04	1.148e-03	1.999e-03
B to Z	5.814e-04	7.629e-04	9.082e-04	1.364e-03
	C12T28SOI_LL_-NAND2X13_P10	C12T28SOI_LL_-NAND2X17_P10	C12T28SOI_LL_-NAND2X20_P10	C12T28SOI_LL_-NAND2X24_P10
A (output stable)	7.520e-05	9.757e-05	1.093e-04	1.386e-04
B (output stable)	4.171e-04	4.205e-04	4.679e-04	6.989e-04
A to Z	2.434e-03	3.086e-03	3.528e-03	4.298e-03
B to Z	1.649e-03	2.221e-03	2.557e-03	2.956e-03
	C12T28SOI_LL_-NAND2X27_P10	C12T28SOI_LL_-NAND2X42_P10	C12T28SOI_LL_-NAND2X47_P10	C12T28SOI_LL_-NAND2X50_P10
A (output stable)	1.514e-04	2.584e-05	2.592e-05	2.593e-05
B (output stable)	7.469e-04	8.561e-05	8.582e-05	8.570e-05
A to Z	4.700e-03	1.185e-02	1.277e-02	1.324e-02
B to Z	3.214e-03	1.159e-02	1.252e-02	1.299e-02
	C12T28SOI_LL_-NAND2X58_P10	C12T28SOI_LL_-NAND2X67_P10	C12T28SOI_-LLBR0D8_-NAND2X7_P10	C12T28SOI_-LLBR0D8_-NAND2X14_P10
A (output stable)	2.603e-05	2.612e-05	3.015e-05	9.520e-05
B (output stable)	8.579e-05	8.623e-05	1.044e-04	5.209e-04
A to Z	1.495e-02	1.658e-02	1.192e-03	2.567e-03
B to Z	1.470e-02	1.633e-02	8.505e-04	1.529e-03
	C12T28SOI_LLS_-NAND2X40_P10	C12T28SOI_LLS_-NAND2X54_P10		
A (output stable)	2.165e-04	2.863e-04		
B (output stable)	1.048e-03	1.334e-03		
A to Z	6.897e-03	9.060e-03		
B to Z	4.767e-03	6.342e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND2X3_P10	C12T28SOI_LL_-NAND2X5_P10	C12T28SOI_LL_-NAND2X7_P10	C12T28SOI_LL_-NAND2X10_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

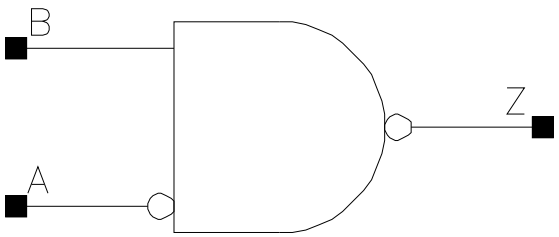
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X13_P10	C12T28SOI_LL_-NAND2X17_P10	C12T28SOI_LL_-NAND2X20_P10	C12T28SOI_LL_-NAND2X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P10	C12T28SOI_LL_-NAND2X42_P10	C12T28SOI_LL_-NAND2X47_P10	C12T28SOI_LL_-NAND2X50_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P10	C12T28SOI_LL_-NAND2X67_P10	C12T28SOI_-LLBR0D8_-NAND2X7_P10	C12T28SOI_-LLBR0D8_-NAND2X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P10	C12T28SOI_LLS_-NAND2X54_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X7_P10	1.200	0.544	0.6528
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X40_P10	1.200	2.312	2.7744
X54_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P10	X7_P10	X13_P10	X27_P10
A	0.0009	0.0009	0.0012	0.0022
B	0.0006	0.0009	0.0016	0.0033
	X40_P10	X54_P10		
A	0.0033	0.0043		
B	0.0049	0.0066		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0259	0.0276	5.6545	3.0874
A to Z ↑	0.0206	0.0215	5.1001	2.6350
B to Z ↓	0.0111	0.0096	5.8430	3.1716
B to Z ↑	0.0131	0.0108	5.3278	2.7452
	X13_P10	**X27_P10**	**X13_P10**	**X27_P10**

A to Z ↓	0.0254	0.0248	1.6688	0.8289
A to Z ↑	0.0206	0.0202	1.3619	0.6579
B to Z ↓	0.0089	0.0089	1.7171	0.8528
B to Z ↑	0.0098	0.0095	1.3707	0.6763
	X40_P10	**X54_P10**	**X40_P10**	**X54_P10**
A to Z ↓	0.0252	0.0250	0.5529	0.4194
A to Z ↑	0.0206	0.0204	0.4377	0.3306
B to Z ↓	0.0090	0.0091	0.5691	0.4317
B to Z ↑	0.0096	0.0096	0.4550	0.3438

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.957e-07	1.000e-20
X7_P10	5.143e-07	1.000e-20
X13_P10	1.107e-06	1.000e-20
X27_P10	2.134e-06	1.000e-20
X40_P10	3.129e-06	1.000e-20
X54_P10	4.124e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	1.103e-03	1.409e-03	2.377e-03	4.645e-03
B (output stable)	4.222e-05	7.882e-05	3.860e-04	6.818e-04
A to Z	1.885e-03	2.630e-03	4.828e-03	9.485e-03
B to Z	5.889e-04	8.973e-04	1.617e-03	3.211e-03
	X40_P10	X54_P10		
A (output stable)	7.079e-03	9.201e-03		
B (output stable)	1.002e-03	1.284e-03		
A to Z	1.429e-02	1.872e-02		
B to Z	4.740e-03	6.292e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

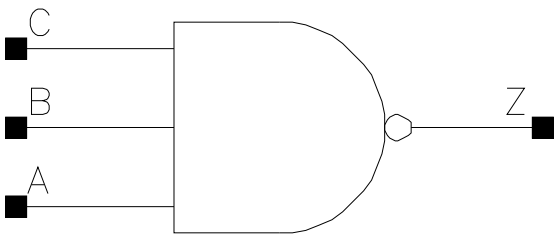
Pin Cycle (vdds)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P10	X54_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P10	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P10	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P10	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P10	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P10	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P10	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P10	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P10	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P10	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P10	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P10	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P10	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P10	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P10	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P10	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A	0.0007	0.0009	0.0015	0.0018
B	0.0008	0.0009	0.0014	0.0017
C	0.0007	0.0009	0.0014	0.0017
	C12T28SOI_LL_-NAND3X15_P10	C12T28SOI_LL_-NAND3X18_P10	C12T28SOI_LL_-NAND3X21_P10	C12T28SOI_LL_-NAND3X24_P10
A	0.0023	0.0027	0.0032	0.0036
B	0.0022	0.0026	0.0031	0.0034
C	0.0021	0.0024	0.0029	0.0032
	C12T28SOI_LL_-NAND3X35_P10	C12T28SOI_LL_-NAND3X47_P10	C12T28SOI_-LLBR0P6_-NAND3X6_P10	C12T28SOI_-LLBR0P6_-NAND3X12_P10
A	0.0054	0.0071	0.0009	0.0018
B	0.0051	0.0068	0.0010	0.0017
C	0.0049	0.0066	0.0009	0.0016
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	C12T28SOI_-LLBR0P6_-NAND3X24_P10	C12T28SOI_-LLBR0P6_-NAND3X35_P10	C12T28SOI_-LLBR0P6_-NAND3X47_P10
A	0.0027	0.0036	0.0054	0.0071
B	0.0025	0.0034	0.0050	0.0068
C	0.0023	0.0032	0.0047	0.0063
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10			
A	0.0028			
B	0.0026			
C	0.0025			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10
A to Z ↓	0.0160	0.0146	5.9996	4.3191
A to Z ↑	0.0183	0.0165	3.8207	2.6145
B to Z ↓	0.0170	0.0153	6.0224	4.3369
B to Z ↑	0.0174	0.0154	3.8318	2.6232
C to Z ↓	0.0152	0.0138	6.0554	4.3610
C to Z ↑	0.0149	0.0131	3.8367	2.6435

	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A to Z ↓	0.0161	0.0152	2.9276	2.2880
A to Z ↑	0.0173	0.0162	1.7905	1.3404
B to Z ↓	0.0154	0.0146	2.9420	2.2980
B to Z ↑	0.0157	0.0146	1.7943	1.3442
C to Z ↓	0.0137	0.0130	2.9590	2.3117
C to Z ↑	0.0131	0.0121	1.7898	1.3341
	C12T28SOI_LL_-NAND3X15_P10	**C12T28SOI_LL_-NAND3X18_P10**	**C12T28SOI_LL_-NAND3X15_P10**	**C12T28SOI_LL_-NAND3X18_P10**
A to Z ↓	0.0145	0.0140	1.8428	1.5815
A to Z ↑	0.0159	0.0152	1.0731	0.8910
B to Z ↓	0.0145	0.0140	1.8522	1.5893
B to Z ↑	0.0144	0.0137	1.0774	0.8936
C to Z ↓	0.0132	0.0126	1.8630	1.5982
C to Z ↑	0.0120	0.0113	1.0865	0.9013
	C12T28SOI_LL_-NAND3X21_P10	**C12T28SOI_LL_-NAND3X24_P10**	**C12T28SOI_LL_-NAND3X21_P10**	**C12T28SOI_LL_-NAND3X24_P10**
A to Z ↓	0.0150	0.0148	1.3344	1.1964
A to Z ↑	0.0160	0.0156	0.7700	0.6746
B to Z ↓	0.0146	0.0144	1.3407	1.2020
B to Z ↑	0.0145	0.0141	0.7717	0.6760
C to Z ↓	0.0132	0.0130	1.3485	1.2091
C to Z ↑	0.0120	0.0116	0.7734	0.6769
	C12T28SOI_LL_-NAND3X35_P10	**C12T28SOI_LL_-NAND3X47_P10**	**C12T28SOI_LL_-NAND3X35_P10**	**C12T28SOI_LL_-NAND3X47_P10**
A to Z ↓	0.0140	0.0142	0.8166	0.6218
A to Z ↑	0.0151	0.0153	0.4521	0.3421
B to Z ↓	0.0140	0.0141	0.8209	0.6249
B to Z ↑	0.0136	0.0136	0.4526	0.3412
C to Z ↓	0.0126	0.0127	0.8259	0.6289
C to Z ↑	0.0111	0.0111	0.4559	0.3434
	C12T28SOI_-LLBR0P6_-NAND3X6_P10	**C12T28SOI_-LLBR0P6_-NAND3X12_P10**	**C12T28SOI_-LLBR0P6_-NAND3X6_P10**	**C12T28SOI_-LLBR0P6_-NAND3X12_P10**
A to Z ↓	0.0117	0.0125	2.9303	1.5558
A to Z ↑	0.0232	0.0230	4.1232	2.1069
B to Z ↓	0.0118	0.0111	2.9556	1.5707
B to Z ↑	0.0209	0.0197	4.1383	2.1131
C to Z ↓	0.0094	0.0085	2.9949	1.5924
C to Z ↑	0.0162	0.0147	4.1665	2.1198
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	**C12T28SOI_-LLBR0P6_-NAND3X24_P10**	**C12T28SOI_-LLBR0P6_-NAND3X18_P10**	**C12T28SOI_-LLBR0P6_-NAND3X24_P10**
A to Z ↓	0.0115	0.0121	1.0781	0.8171
A to Z ↑	0.0218	0.0222	1.4007	1.0587
B to Z ↓	0.0108	0.0110	1.0888	0.8249
B to Z ↑	0.0186	0.0190	1.4053	1.0612
C to Z ↓	0.0085	0.0084	1.1023	0.8360
C to Z ↑	0.0141	0.0141	1.4170	1.0646
	C12T28SOI_-LLBR0P6_-NAND3X35_P10	**C12T28SOI_-LLBR0P6_-NAND3X47_P10**	**C12T28SOI_-LLBR0P6_-NAND3X35_P10**	**C12T28SOI_-LLBR0P6_-NAND3X47_P10**

A to Z ↓	0.0115	0.0117	0.5599	0.4283
A to Z ↑	0.0221	0.0221	0.7296	0.5521
B to Z ↓	0.0108	0.0108	0.5658	0.4326
B to Z ↑	0.0188	0.0187	0.7306	0.5529
C to Z ↓	0.0082	0.0086	0.5737	0.4383
C to Z ↑	0.0136	0.0140	0.7402	0.5552
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P10**	
A to Z ↓	0.0126		1.0571	
A to Z ↑	0.0220		1.3162	
B to Z ↓	0.0111		1.0663	
B to Z ↑	0.0188		1.3197	
C to Z ↓	0.0084		1.0808	
C to Z ↑	0.0137		1.3099	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P10	2.226e-07	1.000e-20
C12T28SOI_LL_NAND3X6_P10	3.541e-07	1.000e-20
C12T28SOI_LL_NAND3X9_P10	4.618e-07	1.000e-20
C12T28SOI_LL_NAND3X12_P10	6.584e-07	1.000e-20
C12T28SOI_LL_NAND3X15_P10	7.503e-07	1.000e-20
C12T28SOI_LL_NAND3X18_P10	9.289e-07	1.000e-20
C12T28SOI_LL_NAND3X21_P10	1.081e-06	1.000e-20
C12T28SOI_LL_NAND3X24_P10	1.251e-06	1.000e-20
C12T28SOI_LL_NAND3X35_P10	1.846e-06	1.000e-20
C12T28SOI_LL_NAND3X47_P10	2.439e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_-P10	3.417e-07	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P10	6.185e-07	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P10	8.435e-07	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P10	1.147e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P10	1.679e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P10	2.207e-06	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P10	1.058e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A (output stable)	1.799e-05	2.503e-05	4.856e-05	6.025e-05
B (output stable)	8.362e-05	1.049e-04	2.052e-04	2.455e-04
C (output stable)	1.353e-04	1.750e-04	2.413e-04	2.951e-04
A to Z	1.588e-03	1.974e-03	3.174e-03	3.790e-03
B to Z	1.414e-03	1.717e-03	2.557e-03	3.064e-03
C to Z	1.093e-03	1.331e-03	1.923e-03	2.302e-03

	C12T28SOI_LL_-NAND3X15_P10	C12T28SOI_LL_-NAND3X18_P10	C12T28SOI_LL_-NAND3X21_P10	C12T28SOI_LL_-NAND3X24_P10
A (output stable)	6.052e-05	6.742e-05	9.595e-05	1.083e-04
B (output stable)	2.877e-04	3.313e-04	4.196e-04	4.596e-04
C (output stable)	3.246e-04	3.731e-04	4.823e-04	5.211e-04
A to Z	4.539e-03	5.029e-03	6.461e-03	7.081e-03
B to Z	3.658e-03	4.029e-03	5.216e-03	5.706e-03
C to Z	2.809e-03	3.047e-03	3.939e-03	4.301e-03
	C12T28SOI_LL_-NAND3X35_P10	C12T28SOI_LL_-NAND3X47_P10	C12T28SOI_-LLBR0P6_-NAND3X6_P10	C12T28SOI_-LLBR0P6_-NAND3X12_P10
A (output stable)	1.328e-04	1.741e-04	3.368e-05	8.007e-05
B (output stable)	6.400e-04	8.298e-04	1.507e-04	3.631e-04
C (output stable)	7.820e-04	9.973e-04	2.512e-04	4.436e-04
A to Z	9.997e-03	1.322e-02	2.145e-03	4.205e-03
B to Z	8.045e-03	1.062e-02	1.750e-03	3.109e-03
C to Z	5.850e-03	7.830e-03	1.157e-03	1.910e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	C12T28SOI_-LLBR0P6_-NAND3X24_P10	C12T28SOI_-LLBR0P6_-NAND3X35_P10	C12T28SOI_-LLBR0P6_-NAND3X47_P10
A (output stable)	9.580e-05	1.456e-04	1.870e-04	2.496e-04
B (output stable)	4.678e-04	6.744e-04	9.383e-04	1.236e-03
C (output stable)	5.334e-04	7.827e-04	1.175e-03	1.474e-03
A to Z	5.646e-03	7.827e-03	1.121e-02	1.469e-02
B to Z	4.165e-03	5.778e-03	8.222e-03	1.078e-02
C to Z	2.676e-03	3.576e-03	4.886e-03	6.520e-03
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10			
A (output stable)	1.188e-04			
B (output stable)	5.492e-04			
C (output stable)	6.766e-04			
A to Z	6.226e-03			
B to Z	4.604e-03			
C to Z	2.822e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P10	C12T28SOI_LL_-NAND3X18_P10	C12T28SOI_LL_-NAND3X21_P10	C12T28SOI_LL_-NAND3X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

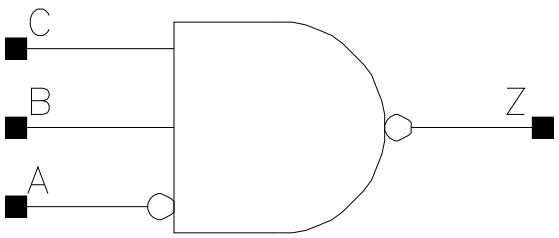
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P10	C12T28SOI_LL_-NAND3X47_P10	C12T28SOI_-LLBR0P6_-NAND3X6_P10	C12T28SOI_-LLBR0P6_-NAND3X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	C12T28SOI_-LLBR0P6_-NAND3X24_P10	C12T28SOI_-LLBR0P6_-NAND3X35_P10	C12T28SOI_-LLBR0P6_-NAND3X47_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.816	0.9792
X12_P10	1.200	1.224	1.4688
X18_P10	1.200	1.496	1.7952
X24_P10	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0008	0.0012	0.0012	0.0022
B	0.0009	0.0017	0.0026	0.0034
C	0.0009	0.0017	0.0024	0.0032

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X12_P10**	**X6_P10**	**X12_P10**
A to Z ↓	0.0312	0.0299	4.3089	2.3045
A to Z ↑	0.0230	0.0225	2.5624	1.2858
B to Z ↓	0.0132	0.0139	4.3562	2.3297
B to Z ↑	0.0139	0.0139	2.6351	1.3263
C to Z ↓	0.0132	0.0122	4.3808	2.3433
C to Z ↑	0.0123	0.0111	2.6516	1.3391
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0340	0.0290	1.5792	1.1974

A to Z ↑	0.0260	0.0214	0.8669	0.6497
B to Z ↓	0.0141	0.0137	1.5930	1.2096
B to Z ↑	0.0137	0.0136	0.8941	0.6722
C to Z ↓	0.0128	0.0122	1.6019	1.2169
C to Z ↑	0.0114	0.0109	0.9015	0.6786

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P10	4.712e-07	1.000e-20
X12_P10	1.012e-06	1.000e-20
X18_P10	1.274e-06	1.000e-20
X24_P10	1.976e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	1.370e-03	2.426e-03	3.295e-03	4.504e-03
B (output stable)	4.171e-05	1.042e-04	1.691e-04	2.546e-04
C (output stable)	1.158e-04	3.722e-04	4.291e-04	6.822e-04
A to Z	3.179e-03	6.241e-03	8.926e-03	1.194e-02
B to Z	1.416e-03	2.805e-03	4.081e-03	5.330e-03
C to Z	1.168e-03	2.005e-03	3.081e-03	3.835e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

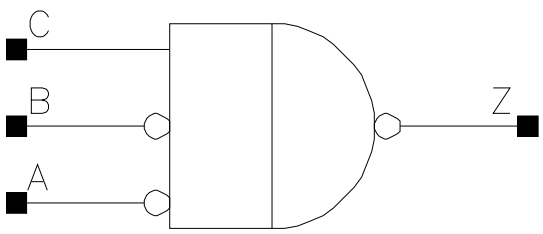
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	0.816	0.9792
X13_P10	1.200	1.088	1.3056
X20_P10	1.200	1.632	1.9584
X27_P10	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P10	X13_P10	X20_P10	X27_P10
A	0.0011	0.0011	0.0021	0.0020
B	0.0012	0.0012	0.0022	0.0021
C	0.0009	0.0017	0.0025	0.0033

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	**X13_P10**	**X7_P10**	**X13_P10**
A to Z ↓	0.0286	0.0346	2.9724	1.5850
A to Z ↑	0.0201	0.0230	2.5357	1.2779
B to Z ↓	0.0290	0.0354	2.9755	1.5850
B to Z ↑	0.0188	0.0218	2.5341	1.2764
C to Z ↓	0.0094	0.0086	3.0459	1.6194
C to Z ↑	0.0108	0.0096	2.6404	1.3355
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0320	0.0351	1.0806	0.8228
A to Z ↑	0.0215	0.0258	0.8628	0.6481
B to Z ↓	0.0304	0.0343	1.0807	0.8234

B to Z ↑	0.0194	0.0242	0.8612	0.6470
C to Z ↓	0.0098	0.0094	1.1058	0.8408
C to Z ↑	0.0105	0.0101	0.9008	0.6762

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X7_P10	7.015e-07	1.000e-20
X13_P10	9.403e-07	1.000e-20
X20_P10	1.532e-06	1.000e-20
X27_P10	1.700e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	7.893e-04	1.059e-03	1.803e-03	2.132e-03
B (output stable)	6.564e-04	9.211e-04	1.394e-03	1.754e-03
C (output stable)	8.281e-05	3.598e-04	4.145e-04	4.996e-04
A to Z	3.521e-03	5.730e-03	9.095e-03	1.134e-02
B to Z	3.182e-03	5.401e-03	7.960e-03	1.035e-02
C to Z	9.364e-04	1.596e-03	2.683e-03	3.510e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

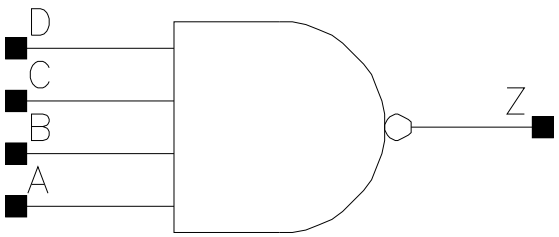
Pin Cycle (vdds)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0007	0.0007	0.0009	0.0011
B	0.0008	0.0008	0.0009	0.0012
C	0.0007	0.0008	0.0009	0.0011
D	0.0007	0.0007	0.0010	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0452	0.0449	1.8054	0.9030
A to Z ↑	0.0371	0.0402	2.5991	1.2888
B to Z ↓	0.0467	0.0472	1.8059	0.9034
B to Z ↑	0.0356	0.0395	2.5982	1.2876
C to Z ↓	0.0455	0.0447	1.8054	0.9031
C to Z ↑	0.0379	0.0417	2.5972	1.2877

D to Z ↓	0.0473	0.0463	1.8054	0.9035
D to Z ↑	0.0369	0.0401	2.5952	1.2861
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0476	0.0442	0.6242	0.4669
A to Z ↑	0.0388	0.0381	0.8693	0.6525
B to Z ↓	0.0493	0.0456	0.6238	0.4666
B to Z ↑	0.0376	0.0368	0.8690	0.6521
C to Z ↓	0.0440	0.0409	0.6236	0.4665
C to Z ↑	0.0390	0.0380	0.8678	0.6512
D to Z ↓	0.0457	0.0424	0.6236	0.4669
D to Z ↑	0.0374	0.0366	0.8672	0.6501

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	7.027e-07	1.000e-20
X17_P10	1.109e-06	1.000e-20
X25_P10	1.611e-06	1.000e-20
X33_P10	2.223e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	5.596e-04	7.001e-04	1.022e-03	1.223e-03
B (output stable)	5.210e-04	6.679e-04	9.671e-04	1.154e-03
C (output stable)	5.575e-04	6.766e-04	1.035e-03	1.185e-03
D (output stable)	5.172e-04	6.333e-04	9.471e-04	1.095e-03
A to Z	4.132e-03	6.321e-03	9.786e-03	1.202e-02
B to Z	3.995e-03	6.200e-03	9.586e-03	1.177e-02
C to Z	4.211e-03	6.210e-03	9.079e-03	1.113e-02
D to Z	4.086e-03	6.070e-03	8.876e-03	1.088e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

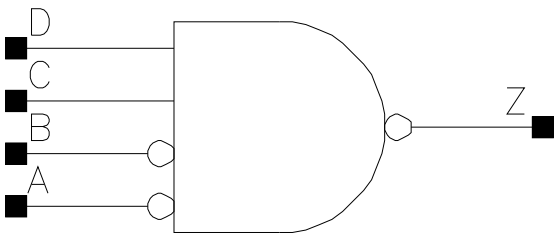
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X12_P10	1.200	1.496	1.7952
X18_P10	1.200	2.040	2.4480
X24_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0011	0.0011	0.0021	0.0019
B	0.0011	0.0015	0.0022	0.0020
C	0.0009	0.0018	0.0025	0.0035
D	0.0009	0.0017	0.0024	0.0034

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X12_P10	X6_P10	X12_P10
A to Z ↓	0.0305	0.0408	4.4415	2.3107
A to Z ↑	0.0211	0.0258	2.5372	1.2807
B to Z ↓	0.0303	0.0406	4.4405	2.3112
B to Z ↑	0.0190	0.0242	2.5376	1.2783
C to Z ↓	0.0134	0.0137	4.4876	2.3287
C to Z ↑	0.0141	0.0138	2.8083	1.3264

D to Z ↓	0.0130	0.0120	4.5122	2.3424
D to Z ↑	0.0123	0.0110	2.8273	1.3391
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0357	0.0394	1.5756	1.1985
A to Z ↑	0.0228	0.0287	0.8637	0.6490
B to Z ↓	0.0342	0.0385	1.5764	1.1992
B to Z ↑	0.0209	0.0270	0.8622	0.6480
C to Z ↓	0.0136	0.0142	1.5894	1.2077
C to Z ↑	0.0135	0.0138	0.8981	0.6707
D to Z ↓	0.0124	0.0127	1.5987	1.2149
D to Z ↑	0.0112	0.0112	0.9194	0.6778

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P10	6.144e-07	1.000e-20
X12_P10	8.671e-07	1.000e-20
X18_P10	1.412e-06	1.000e-20
X24_P10	1.527e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	8.863e-04	1.494e-03	2.281e-03	2.705e-03
B (output stable)	7.212e-04	1.254e-03	1.802e-03	2.257e-03
C (output stable)	7.989e-05	2.004e-04	2.927e-04	3.804e-04
D (output stable)	1.094e-04	3.643e-04	4.241e-04	6.187e-04
A to Z	3.745e-03	7.104e-03	1.049e-02	1.368e-02
B to Z	3.403e-03	6.598e-03	9.424e-03	1.267e-02
C to Z	1.376e-03	2.764e-03	3.925e-03	5.566e-03
D to Z	1.124e-03	1.968e-03	2.987e-03	4.095e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

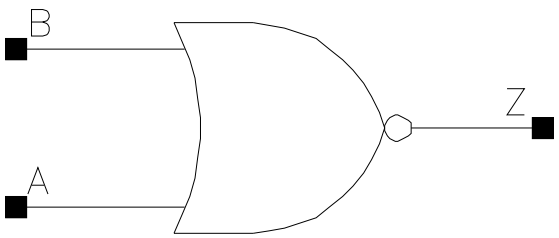
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.408	0.4896
X5_P10	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X10_P10	1.200	0.680	0.8160
X14_P10	1.200	0.680	0.8160
X17_P10	1.200	0.952	1.1424
X21_P10	1.200	0.952	1.1424
X24_P10	1.200	1.224	1.4688
X27_P10	1.200	1.224	1.4688
X34_P10	1.200	1.496	1.7952
X40_P10	1.200	1.360	1.6320
X41_P10	1.200	1.768	2.1216
X49_P10	1.200	1.496	1.7952
X53_P10	1.200	1.904	2.2848
X55_P10	1.200	2.312	2.7744
X57_P10	1.200	1.904	2.2848
X65_P10	1.200	2.040	2.4480
X84_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P10	X5_P10	X7_P10	X10_P10
A	0.0006	0.0007	0.0009	0.0015
B	0.0006	0.0007	0.0009	0.0013
	X14_P10	X17_P10	X21_P10	X24_P10

A	0.0019	0.0024	0.0027	0.0032
B	0.0017	0.0021	0.0025	0.0030
	X27_P10	X34_P10	X40_P10	X41_P10
A	0.0036	0.0045	0.0011	0.0055
B	0.0033	0.0041	0.0012	0.0051
	X49_P10	X53_P10	X55_P10	X57_P10
A	0.0010	0.0011	0.0073	0.0011
B	0.0012	0.0010	0.0067	0.0010
	X65_P10	X84_P10		
A	0.0011	0.0012		
B	0.0010	0.0011		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X5_P10**	**X3_P10**	**X5_P10**
A to Z ↓	0.0095	0.0090	3.4925	2.5334
A to Z ↑	0.0164	0.0150	9.9218	7.2127
B to Z ↓	0.0082	0.0075	3.5796	2.5559
B to Z ↑	0.0162	0.0146	9.9923	7.2488
	X7_P10	**X10_P10**	**X7_P10**	**X10_P10**
A to Z ↓	0.0088	0.0092	1.8670	1.2095
A to Z ↑	0.0140	0.0162	5.0678	3.4067
B to Z ↓	0.0072	0.0066	1.8921	1.2258
B to Z ↑	0.0135	0.0127	5.0979	3.4293
	X14_P10	**X17_P10**	**X14_P10**	**X17_P10**
A to Z ↓	0.0091	0.0092	0.9222	0.7420
A to Z ↑	0.0151	0.0152	2.5161	2.0389
B to Z ↓	0.0064	0.0071	0.9348	0.7498
B to Z ↑	0.0119	0.0130	2.5344	2.0536
	X21_P10	**X24_P10**	**X21_P10**	**X24_P10**
A to Z ↓	0.0091	0.0090	0.6312	0.5372
A to Z ↑	0.0144	0.0149	1.6940	1.4846
B to Z ↓	0.0071	0.0067	0.6380	0.5437
B to Z ↑	0.0126	0.0123	1.7056	1.4960
	X27_P10	**X34_P10**	**X27_P10**	**X34_P10**
A to Z ↓	0.0089	0.0093	0.4776	0.3859
A to Z ↑	0.0142	0.0145	1.3048	1.0381
B to Z ↓	0.0066	0.0070	0.4838	0.3902
B to Z ↑	0.0119	0.0124	1.3145	1.0454
	X40_P10	**X41_P10**	**X40_P10**	**X41_P10**
A to Z ↓	0.0318	0.0091	0.3807	0.3215
A to Z ↑	0.0426	0.0142	0.5353	0.8589
B to Z ↓	0.0304	0.0067	0.3806	0.3256
B to Z ↑	0.0435	0.0118	0.5357	0.8655
	X49_P10	**X53_P10**	**X49_P10**	**X53_P10**
A to Z ↓	0.0330	0.0344	0.3168	0.2898
A to Z ↑	0.0438	0.0495	0.4449	0.4121
B to Z ↓	0.0317	0.0331	0.3166	0.2901
B to Z ↑	0.0446	0.0502	0.4456	0.4122
	X55_P10	**X57_P10**	**X55_P10**	**X57_P10**
A to Z ↓	0.0092	0.0347	0.2432	0.2729
A to Z ↑	0.0143	0.0498	0.6477	0.3832

B to Z ↓	0.0067	0.0334	0.2468	0.2727
B to Z ↑	0.0118	0.0504	0.6528	0.3833
	X65_P10	**X84_P10**	**X65_P10**	**X84_P10**
A to Z ↓	0.0357	0.0369	0.2395	0.1902
A to Z ↑	0.0508	0.0511	0.3352	0.2663
B to Z ↓	0.0344	0.0356	0.2396	0.1903
B to Z ↑	0.0514	0.0518	0.3353	0.2663

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	1.660e-07	1.000e-20
X5_P10	2.550e-07	1.000e-20
X7_P10	3.937e-07	1.000e-20
X10_P10	5.323e-07	1.000e-20
X14_P10	7.733e-07	1.000e-20
X17_P10	9.027e-07	1.000e-20
X21_P10	1.128e-06	1.000e-20
X24_P10	1.274e-06	1.000e-20
X27_P10	1.484e-06	1.000e-20
X34_P10	1.840e-06	1.000e-20
X40_P10	2.805e-06	1.000e-20
X41_P10	2.195e-06	1.000e-20
X49_P10	3.187e-06	1.000e-20
X53_P10	3.653e-06	1.000e-20
X55_P10	2.907e-06	1.000e-20
X57_P10	3.902e-06	1.000e-20
X65_P10	4.284e-06	1.000e-20
X84_P10	5.056e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	2.473e-05	3.275e-05	4.447e-05	1.341e-04
B (output stable)	7.541e-06	1.023e-05	1.569e-05	7.627e-05
A to Z	7.303e-04	8.961e-04	1.194e-03	2.076e-03
B to Z	5.528e-04	6.633e-04	8.647e-04	1.202e-03
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	1.580e-04	1.879e-04	2.067e-04	2.578e-04
B (output stable)	9.035e-05	1.051e-04	1.037e-04	1.278e-04
A to Z	2.588e-03	3.234e-03	3.701e-03	4.392e-03
B to Z	1.523e-03	2.088e-03	2.407e-03	2.708e-03
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	2.747e-04	3.386e-04	4.511e-05	4.286e-04
B (output stable)	1.347e-04	1.470e-04	1.563e-05	2.111e-04
A to Z	4.741e-03	6.101e-03	1.163e-02	7.188e-03
B to Z	2.949e-03	3.955e-03	1.131e-02	4.416e-03
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	4.525e-05	4.632e-05	5.751e-04	4.632e-05
B (output stable)	1.553e-05	1.585e-05	2.792e-04	1.586e-05
A to Z	1.306e-02	1.608e-02	9.501e-03	1.660e-02
B to Z	1.274e-02	1.574e-02	5.823e-03	1.626e-02
	X65_P10	X84_P10		

A (output stable)	4.641e-05	4.788e-05		
B (output stable)	1.596e-05	1.704e-05		
A to Z	1.808e-02	2.111e-02		
B to Z	1.774e-02	2.071e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

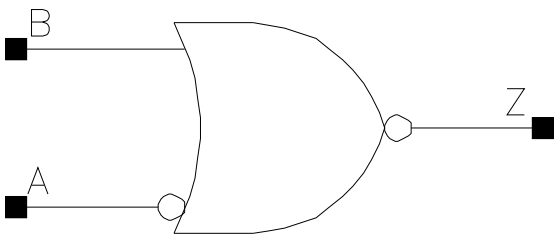
Pin Cycle (vdds)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P10	X84_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X7_P10	1.200	0.680	0.8160
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X41_P10	1.200	2.312	2.7744
X55_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X7_P10	X13_P10
A	0.0009	0.0009	0.0009	0.0012
B	0.0006	0.0009	0.0009	0.0016
	X27_P10	X41_P10	X55_P10	
A	0.0022	0.0033	0.0043	
B	0.0033	0.0050	0.0067	

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0244	0.0271	3.3149	2.1836
A to Z ↑	0.0231	0.0233	9.8043	5.0225
B to Z ↓	0.0084	0.0084	3.5500	2.3492
B to Z ↑	0.0163	0.0134	9.9699	5.1146

	X7_P10	X13_P10	X7_P10	X13_P10
A to Z ↓	0.0275	0.0246	1.7378	0.9483
A to Z ↑	0.0254	0.0242	4.9830	2.6608
B to Z ↓	0.0077	0.0069	1.8118	0.9839
B to Z ↑	0.0147	0.0131	5.0532	2.7044
	X27_P10	**X41_P10**	**X27_P10**	**X41_P10**
A to Z ↓	0.0238	0.0243	0.4530	0.3069
A to Z ↑	0.0232	0.0236	1.2687	0.8526
B to Z ↓	0.0067	0.0068	0.4867	0.3278
B to Z ↑	0.0123	0.0122	1.2906	0.8668
	X55_P10		**X55_P10**	
A to Z ↓	0.0238		0.2324	
A to Z ↑	0.0231		0.6434	
B to Z ↓	0.0067		0.2485	
B to Z ↑	0.0119		0.6547	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	2.992e-07	1.000e-20
X6_P10	5.032e-07	1.000e-20
X7_P10	5.775e-07	1.000e-20
X13_P10	1.119e-06	1.000e-20
X27_P10	2.187e-06	1.000e-20
X41_P10	3.211e-06	1.000e-20
X55_P10	4.235e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	1.093e-03	1.374e-03	1.473e-03	2.390e-03
B (output stable)	2.588e-05	5.145e-05	8.719e-05	1.819e-04
A to Z	1.885e-03	2.609e-03	3.033e-03	5.095e-03
B to Z	5.639e-04	8.440e-04	1.035e-03	1.661e-03
	X27_P10	X41_P10	X55_P10	
A (output stable)	4.689e-03	7.155e-03	9.290e-03	
B (output stable)	3.728e-04	5.632e-04	7.490e-04	
A to Z	1.010e-02	1.503e-02	1.954e-02	
B to Z	3.203e-03	4.674e-03	6.008e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

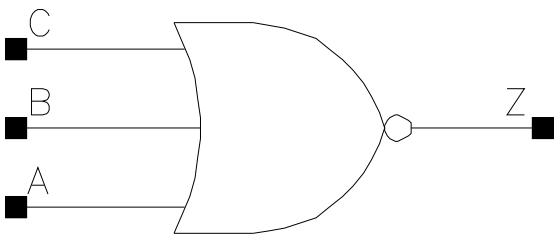
Pin Cycle (vdds)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P10	X41_P10	X55_P10	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X9_P10	1.200	0.952	1.1424
X13_P10	1.200	0.952	1.1424
X16_P10	1.200	1.360	1.6320
X19_P10	1.200	1.496	1.7952
X22_P10	1.200	1.768	2.1216
X25_P10	1.200	1.904	2.2848
X37_P10	1.200	2.584	3.1008
X49_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P10	X6_P10	X9_P10	X13_P10
A	0.0007	0.0009	0.0014	0.0017
B	0.0007	0.0009	0.0016	0.0019
C	0.0007	0.0009	0.0013	0.0016
	X16_P10	X19_P10	X22_P10	X25_P10
A	0.0024	0.0027	0.0032	0.0036
B	0.0023	0.0031	0.0034	0.0041
C	0.0021	0.0024	0.0029	0.0033
	X37_P10	X49_P10		
A	0.0054	0.0073		
B	0.0055	0.0073		

C	0.0048	0.0066		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0110	0.0107	2.5665	1.8929
A to Z ↑	0.0223	0.0204	10.6545	7.5076
B to Z ↓	0.0103	0.0099	2.5738	1.8984
B to Z ↑	0.0211	0.0191	10.6749	7.5229
C to Z ↓	0.0090	0.0083	2.5960	1.9196
C to Z ↑	0.0197	0.0174	10.7072	7.5446
	X9_P10	**X13_P10**	**X9_P10**	**X13_P10**
A to Z ↓	0.0110	0.0109	1.2472	0.9606
A to Z ↑	0.0226	0.0210	5.0142	3.7317
B to Z ↓	0.0102	0.0098	1.2164	0.9212
B to Z ↑	0.0224	0.0202	5.0254	3.7393
C to Z ↓	0.0077	0.0074	1.2301	0.9396
C to Z ↑	0.0163	0.0150	5.0390	3.7508
	X16_P10	**X19_P10**	**X16_P10**	**X19_P10**
A to Z ↓	0.0109	0.0108	0.7460	0.6306
A to Z ↑	0.0215	0.0211	3.0262	2.4990
B to Z ↓	0.0103	0.0101	0.7489	0.6177
B to Z ↑	0.0208	0.0210	3.0317	2.5037
C to Z ↓	0.0080	0.0079	0.7547	0.6443
C to Z ↑	0.0169	0.0160	3.0414	2.5120
	X22_P10	**X25_P10**	**X22_P10**	**X25_P10**
A to Z ↓	0.0108	0.0108	0.5475	0.4809
A to Z ↑	0.0212	0.0211	2.1607	1.8793
B to Z ↓	0.0100	0.0099	0.5387	0.4631
B to Z ↑	0.0205	0.0209	2.1652	1.8826
C to Z ↓	0.0074	0.0075	0.5459	0.4823
C to Z ↑	0.0154	0.0151	2.1725	1.8894
	X37_P10	**X49_P10**	**X37_P10**	**X49_P10**
A to Z ↓	0.0109	0.0110	0.3311	0.2507
A to Z ↑	0.0205	0.0206	1.2604	0.9497
B to Z ↓	0.0100	0.0101	0.3277	0.2484
B to Z ↑	0.0196	0.0196	1.2631	0.9516
C to Z ↓	0.0078	0.0080	0.3322	0.2518
C to Z ↑	0.0152	0.0154	1.2674	0.9552

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	2.269e-07	1.000e-20
X6_P10	3.500e-07	1.000e-20
X9_P10	4.801e-07	1.000e-20
X13_P10	7.002e-07	1.000e-20
X16_P10	8.179e-07	1.000e-20
X19_P10	1.056e-06	1.000e-20
X22_P10	1.158e-06	1.000e-20
X25_P10	1.391e-06	1.000e-20
X37_P10	2.027e-06	1.000e-20

X49_P10	2.692e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	1.020e-04	1.258e-04	3.295e-04	3.819e-04
B (output stable)	-1.173e-05	-1.738e-05	8.174e-05	4.875e-05
C (output stable)	7.637e-06	1.208e-05	4.187e-05	5.170e-05
A to Z	1.329e-03	1.702e-03	2.865e-03	3.538e-03
B to Z	1.072e-03	1.351e-03	2.386e-03	2.864e-03
C to Z	8.306e-04	1.010e-03	1.439e-03	1.740e-03
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	4.340e-04	5.274e-04	6.576e-04	7.557e-04
B (output stable)	2.247e-05	2.878e-05	7.841e-05	8.218e-05
C (output stable)	5.487e-05	6.941e-05	8.262e-05	9.599e-05
A to Z	4.511e-03	5.353e-03	6.165e-03	7.078e-03
B to Z	3.675e-03	4.428e-03	5.012e-03	5.828e-03
C to Z	2.492e-03	2.816e-03	3.122e-03	3.499e-03
	X37_P10	X49_P10		
A (output stable)	1.033e-03	1.365e-03		
B (output stable)	4.289e-05	4.139e-05		
C (output stable)	1.433e-04	1.863e-04		
A to Z	1.024e-02	1.369e-02		
B to Z	8.216e-03	1.096e-02		
C to Z	5.139e-03	6.929e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

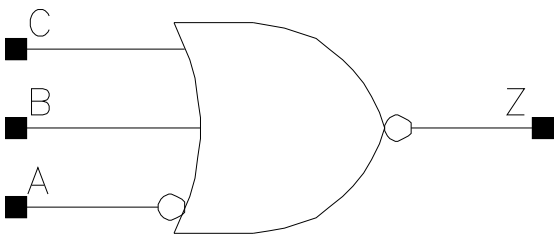
Pin Cycle (vdds)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P10	X49_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.680	0.8160
X13_P10	1.200	1.224	1.4688
X19_P10	1.200	1.496	1.7952
X25_P10	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0009	0.0012	0.0012	0.0022
B	0.0009	0.0019	0.0027	0.0036
C	0.0009	0.0017	0.0024	0.0033

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X13_P10**	**X6_P10**	**X13_P10**
A to Z ↓	0.0274	0.0260	1.8087	1.0126
A to Z ↑	0.0301	0.0297	7.5790	3.7213
B to Z ↓	0.0100	0.0098	1.9062	0.9267
B to Z ↑	0.0194	0.0202	7.6223	3.7395
C to Z ↓	0.0084	0.0073	1.9204	0.9408
C to Z ↑	0.0178	0.0149	7.6439	3.7510
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0296	0.0260	0.6132	0.4661

A to Z ↑	0.0325	0.0299	2.5073	1.8808
B to Z ↓	0.0102	0.0099	0.6442	0.4807
B to Z ↑	0.0196	0.0197	2.5217	1.8911
C to Z ↓	0.0078	0.0075	0.6452	0.4853
C to Z ↑	0.0160	0.0152	2.5299	1.8976

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P10	4.886e-07	1.000e-20
X13_P10	1.085e-06	1.000e-20
X19_P10	1.381e-06	1.000e-20
X25_P10	2.089e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	1.494e-03	2.808e-03	3.664e-03	5.482e-03
B (output stable)	8.741e-06	6.747e-05	6.640e-05	1.119e-04
C (output stable)	2.397e-05	9.334e-05	1.052e-04	1.637e-04
A to Z	3.218e-03	6.388e-03	8.808e-03	1.240e-02
B to Z	1.361e-03	2.866e-03	4.144e-03	5.515e-03
C to Z	1.029e-03	1.727e-03	2.800e-03	3.507e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

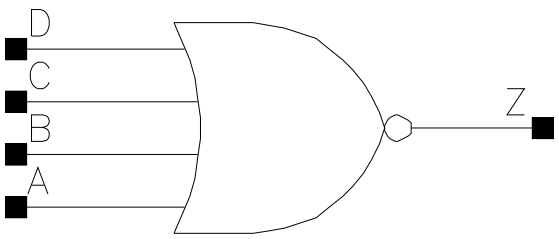
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	1.904	2.2848
X32_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X32_P10
A	0.0007	0.0007	0.0008	0.0010
B	0.0008	0.0007	0.0009	0.0013
C	0.0007	0.0006	0.0009	0.0010
D	0.0007	0.0007	0.0009	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0325	0.0323	1.7727	0.8729
A to Z ↑	0.0466	0.0502	2.6447	1.3076
B to Z ↓	0.0311	0.0313	1.7714	0.8721
B to Z ↑	0.0469	0.0508	2.6442	1.3075
C to Z ↓	0.0318	0.0323	1.7695	0.8715
C to Z ↑	0.0472	0.0514	2.6452	1.3073

D to Z ↓	0.0311	0.0317	1.7698	0.8708
D to Z ↑	0.0479	0.0524	2.6441	1.3071
	X25_P10	**X32_P10**	**X25_P10**	**X32_P10**
A to Z ↓	0.0334	0.0352	0.6078	0.4779
A to Z ↑	0.0496	0.0479	0.8960	0.6787
B to Z ↓	0.0324	0.0341	0.6080	0.4779
B to Z ↑	0.0504	0.0484	0.8957	0.6779
C to Z ↓	0.0323	0.0348	0.6054	0.4766
C to Z ↑	0.0489	0.0480	0.8956	0.6788
D to Z ↓	0.0311	0.0328	0.6059	0.4763
D to Z ↑	0.0497	0.0484	0.8963	0.6788

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	8.378e-07	1.000e-20
X17_P10	1.403e-06	1.000e-20
X25_P10	2.142e-06	1.000e-20
X32_P10	2.817e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	5.657e-04	6.981e-04	9.725e-04	1.225e-03
B (output stable)	4.780e-04	6.117e-04	8.558e-04	1.061e-03
C (output stable)	5.314e-04	6.441e-04	1.013e-03	1.296e-03
D (output stable)	4.443e-04	5.605e-04	8.902e-04	1.134e-03
A to Z	3.944e-03	6.040e-03	9.204e-03	1.151e-02
B to Z	3.760e-03	5.870e-03	8.944e-03	1.120e-02
C to Z	3.971e-03	6.004e-03	8.633e-03	1.087e-02
D to Z	3.779e-03	5.833e-03	8.393e-03	1.053e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

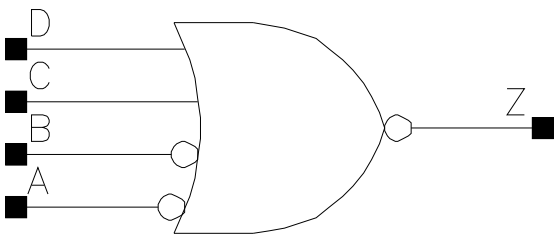
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X13_P10	1.200	1.496	1.7952
X19_P10	1.200	2.040	2.4480
X25_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0011	0.0012	0.0022	0.0021
B	0.0012	0.0016	0.0022	0.0022
C	0.0009	0.0018	0.0026	0.0035
D	0.0009	0.0017	0.0024	0.0033

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X13_P10	X6_P10	X13_P10
A to Z ↓	0.0237	0.0294	1.7618	0.8829
A to Z ↑	0.0298	0.0372	7.2995	3.7887
B to Z ↓	0.0219	0.0281	1.7613	0.8823
B to Z ↑	0.0305	0.0384	7.3000	3.7899
C to Z ↓	0.0104	0.0098	1.9397	0.9266
C to Z ↑	0.0195	0.0203	7.3452	3.8095

D to Z ↓	0.0086	0.0074	1.9440	0.9381
D to Z ↑	0.0175	0.0154	7.3639	3.8199
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0260	0.0284	0.6059	0.4564
A to Z ↑	0.0335	0.0363	2.5086	1.8974
B to Z ↓	0.0237	0.0265	0.6052	0.4560
B to Z ↑	0.0337	0.0370	2.5086	1.8976
C to Z ↓	0.0103	0.0101	0.6443	0.4825
C to Z ↑	0.0196	0.0196	2.5220	1.9065
D to Z ↓	0.0078	0.0075	0.6457	0.4848
D to Z ↑	0.0160	0.0151	2.5296	1.9125

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P10	6.854e-07	1.000e-20
X13_P10	1.007e-06	1.000e-20
X19_P10	1.632e-06	1.000e-20
X25_P10	1.915e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	9.032e-04	1.603e-03	2.400e-03	2.940e-03
B (output stable)	8.284e-04	1.505e-03	2.182e-03	2.751e-03
C (output stable)	6.110e-06	6.100e-05	7.977e-05	1.218e-04
D (output stable)	3.427e-05	1.376e-04	1.723e-04	2.882e-04
A to Z	3.867e-03	7.287e-03	1.089e-02	1.394e-02
B to Z	3.617e-03	6.889e-03	1.004e-02	1.319e-02
C to Z	1.415e-03	2.859e-03	4.128e-03	5.442e-03
D to Z	1.066e-03	1.771e-03	2.799e-03	3.439e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

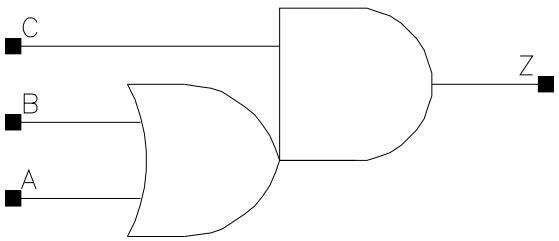
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0010	0.0011	0.0020
B	0.0012	0.0012	0.0023
C	0.0011	0.0012	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0257	0.0298	1.8277	0.9127
A to Z ↑	0.0231	0.0259	2.6613	1.3117
B to Z ↓	0.0258	0.0304	1.8289	0.9130
B to Z ↑	0.0208	0.0238	2.6551	1.3076
C to Z ↓	0.0235	0.0260	1.8093	0.8981
C to Z ↑	0.0217	0.0241	2.6564	1.3087
	X33_P10		**X33_P10**	
A to Z ↓	0.0313		0.4642	
A to Z ↑	0.0280		0.6586	

B to Z ↓	0.0319		0.4639	
B to Z ↑	0.0255		0.6572	
C to Z ↓	0.0267		0.4553	
C to Z ↑	0.0251		0.6572	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	8.197e-07	1.000e-20
X17_P10	1.213e-06	1.000e-20
X33_P10	2.404e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.323e-04	1.336e-04	2.613e-04
B (output stable)	6.565e-05	6.418e-05	1.242e-04
C (output stable)	7.459e-05	7.730e-05	1.514e-04
A to Z	2.946e-03	4.373e-03	9.231e-03
B to Z	2.602e-03	4.025e-03	8.546e-03
C to Z	3.236e-03	4.591e-03	9.529e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

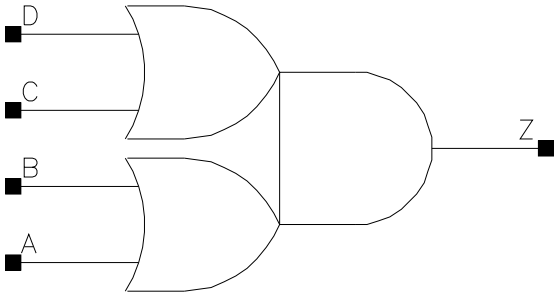
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0010	0.0021
B	0.0007	0.0011	0.0021
C	0.0007	0.0011	0.0021
D	0.0007	0.0011	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0433	0.0368	1.7764	0.9048
A to Z ↑	0.0309	0.0276	2.6094	1.3047
B to Z ↓	0.0444	0.0377	1.7773	0.9044
B to Z ↑	0.0296	0.0261	2.6065	1.3023

C to Z ↓	0.0377	0.0325	1.7668	0.9013
C to Z ↑	0.0301	0.0278	2.6070	1.3039
D to Z ↓	0.0381	0.0329	1.7674	0.9016
D to Z ↑	0.0282	0.0255	2.6041	1.3021
	X33_P10		**X33_P10**	
A to Z ↓	0.0375		0.4663	
A to Z ↑	0.0278		0.6561	
B to Z ↓	0.0368		0.4665	
B to Z ↑	0.0257		0.6549	
C to Z ↓	0.0325		0.4642	
C to Z ↑	0.0274		0.6556	
D to Z ↓	0.0314		0.4646	
D to Z ↑	0.0249		0.6542	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	6.094e-07	1.000e-20
X17_P10	1.305e-06	1.000e-20
X33_P10	2.498e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.269e-05	3.891e-05	1.222e-04
B (output stable)	1.937e-05	2.773e-05	9.308e-05
C (output stable)	4.756e-05	8.686e-05	2.449e-04
D (output stable)	8.296e-05	1.094e-04	2.748e-04
A to Z	3.468e-03	5.637e-03	1.115e-02
B to Z	3.280e-03	5.271e-03	1.014e-02
C to Z	2.991e-03	4.964e-03	9.752e-03
D to Z	2.802e-03	4.604e-03	8.699e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

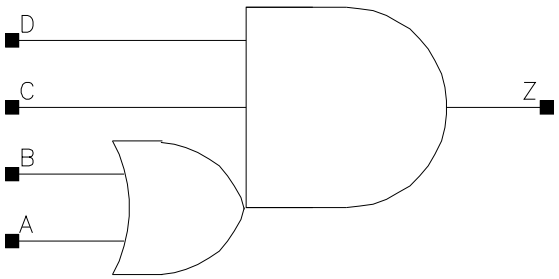
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	1.088	1.3056
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0007	0.0011	0.0017	0.0021
B	0.0007	0.0011	0.0018	0.0022
C	0.0008	0.0011	0.0018	0.0022
D	0.0007	0.0011	0.0018	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0368	0.0342	1.8702	0.9126
A to Z ↑	0.0361	0.0339	2.7067	1.3104
B to Z ↓	0.0377	0.0341	1.8693	0.9137
B to Z ↑	0.0341	0.0311	2.7070	1.3066
C to Z ↓	0.0314	0.0289	1.8255	0.8954

C to Z ↑	0.0335	0.0313	2.7029	1.3063
D to Z ↓	0.0305	0.0278	1.8254	0.8947
D to Z ↑	0.0350	0.0326	2.7014	1.3075
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0361	0.0344	0.6227	0.4654
A to Z ↑	0.0350	0.0353	0.8913	0.6676
B to Z ↓	0.0355	0.0337	0.6230	0.4661
B to Z ↑	0.0321	0.0320	0.8895	0.6656
C to Z ↓	0.0305	0.0290	0.6107	0.4570
C to Z ↑	0.0325	0.0322	0.8886	0.6653
D to Z ↓	0.0290	0.0277	0.6095	0.4561
D to Z ↑	0.0327	0.0327	0.8886	0.6655

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	5.725e-07	1.000e-20
X17_P10	1.251e-06	1.000e-20
X25_P10	1.866e-06	1.000e-20
X33_P10	2.475e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	7.733e-05	1.561e-04	2.772e-04	3.169e-04
B (output stable)	5.413e-05	1.089e-04	1.792e-04	2.078e-04
C (output stable)	1.258e-05	2.513e-05	6.856e-05	7.789e-05
D (output stable)	3.209e-05	7.184e-05	1.991e-04	2.127e-04
A to Z	2.883e-03	5.122e-03	8.324e-03	1.023e-02
B to Z	2.707e-03	4.706e-03	7.552e-03	9.226e-03
C to Z	3.117e-03	5.473e-03	9.055e-03	1.091e-02
D to Z	2.981e-03	5.215e-03	8.414e-03	1.024e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

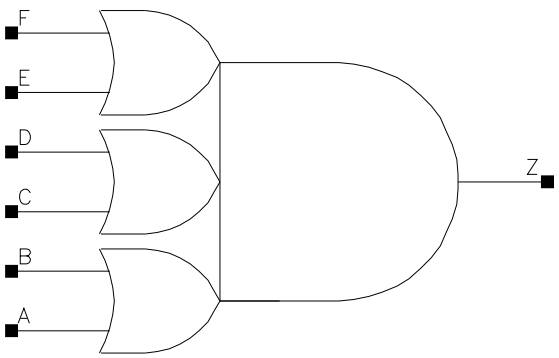
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0008	0.0010	0.0018
B	0.0007	0.0011	0.0020
C	0.0007	0.0010	0.0019
D	0.0007	0.0011	0.0021
E	0.0007	0.0011	0.0019
F	0.0007	0.0011	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0492	0.0419	1.9051	0.9266
A to Z ↑	0.0392	0.0362	2.6853	1.3222
B to Z ↓	0.0501	0.0431	1.9054	0.9267
B to Z ↑	0.0377	0.0348	2.6863	1.3224
C to Z ↓	0.0452	0.0398	1.8939	0.9257
C to Z ↑	0.0397	0.0362	2.6866	1.3224
D to Z ↓	0.0463	0.0407	1.8955	0.9261
D to Z ↑	0.0378	0.0343	2.6847	1.3221
E to Z ↓	0.0394	0.0352	1.8848	0.9220
E to Z ↑	0.0371	0.0346	2.6849	1.3217
F to Z ↓	0.0405	0.0356	1.8851	0.9226
F to Z ↑	0.0353	0.0324	2.6816	1.3197
	X33_P10		X33_P10	
A to Z ↓	0.0423		0.4743	
A to Z ↑	0.0371		0.6673	
B to Z ↓	0.0435		0.4745	
B to Z ↑	0.0345		0.6657	
C to Z ↓	0.0390		0.4718	
C to Z ↑	0.0369		0.6674	
D to Z ↓	0.0400		0.4721	
D to Z ↑	0.0345		0.6656	
E to Z ↓	0.0344		0.4700	
E to Z ↑	0.0353		0.6665	
F to Z ↓	0.0352		0.4704	
F to Z ↑	0.0327		0.6650	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	6.638e-07	1.000e-20
X17_P10	1.453e-06	1.000e-20
X33_P10	2.765e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.730e-05	3.256e-05	5.699e-05
B (output stable)	9.273e-06	2.131e-05	3.201e-05
C (output stable)	4.105e-05	6.535e-05	1.354e-04
D (output stable)	4.724e-05	7.570e-05	1.617e-04
E (output stable)	6.115e-05	1.055e-04	1.945e-04
F (output stable)	1.334e-04	1.981e-04	3.800e-04
A to Z	3.990e-03	6.623e-03	1.291e-02
B to Z	3.795e-03	6.280e-03	1.222e-02
C to Z	3.627e-03	6.102e-03	1.179e-02
D to Z	3.441e-03	5.745e-03	1.110e-02
E to Z	3.169e-03	5.427e-03	1.047e-02
F to Z	3.000e-03	5.071e-03	9.812e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

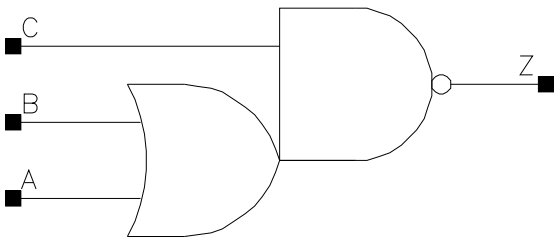
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X34_P10	1.200	2.720	3.2640
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X34_P10	X46_P10
A	0.0008	0.0026	0.0052	0.0068
B	0.0008	0.0024	0.0047	0.0063
C	0.0009	0.0027	0.0055	0.0072

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0127	0.0131	3.4262	1.1201
A to Z ↑	0.0148	0.0157	5.0678	1.7271
B to Z ↓	0.0103	0.0105	3.3593	1.1271
B to Z ↑	0.0142	0.0140	5.1017	1.7401
C to Z ↓	0.0120	0.0120	3.1082	1.0262
C to Z ↑	0.0146	0.0143	2.7026	0.8995
	X34_P10	**X46_P10**	**X34_P10**	**X46_P10**
A to Z ↓	0.0138	0.0138	0.5709	0.4359

A to Z ↑	0.0165	0.0162	0.8609	0.6631
B to Z ↓	0.0109	0.0110	0.5792	0.4441
B to Z ↑	0.0145	0.0145	0.8673	0.6680
C to Z ↓	0.0125	0.0124	0.5255	0.4019
C to Z ↑	0.0147	0.0146	0.4494	0.3441

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P10	4.672e-07	1.000e-20
X17_P10	1.368e-06	1.000e-20
X34_P10	2.717e-06	1.000e-20
X46_P10	3.586e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	1.216e-04	3.975e-04	8.337e-04	1.041e-03
B (output stable)	6.806e-05	2.077e-04	4.225e-04	5.346e-04
C (output stable)	6.376e-05	2.066e-04	4.610e-04	5.592e-04
A to Z	1.292e-03	4.113e-03	8.783e-03	1.129e-02
B to Z	9.594e-04	2.829e-03	5.989e-03	7.790e-03
C to Z	1.581e-03	4.783e-03	1.003e-02	1.294e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

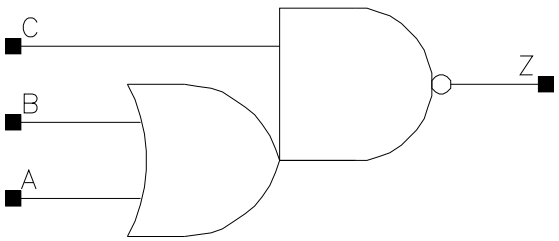
Pin Cycle (vdds)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.544	0.6528
X11_P10	1.200	0.952	1.1424
X17_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X17_P10	X23_P10
A	0.0009	0.0018	0.0027	0.0037
B	0.0008	0.0018	0.0026	0.0034
C	0.0009	0.0017	0.0025	0.0035
	X46_P10			
A	0.0074			
B	0.0068			
C	0.0069			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0133	0.0134	3.4549	1.6106
A to Z ↑	0.0188	0.0188	5.3462	2.5261
B to Z ↓	0.0113	0.0113	3.3948	1.5676

B to Z ↑	0.0186	0.0185	5.3749	2.5403
C to Z ↓	0.0104	0.0104	3.2330	1.5011
C to Z ↑	0.0111	0.0109	2.9132	1.3667
	X17_P10	**X23_P10**	**X17_P10**	**X23_P10**
A to Z ↓	0.0130	0.0136	1.1201	0.8285
A to Z ↑	0.0179	0.0197	1.6722	1.2762
B to Z ↓	0.0109	0.0113	1.1160	0.8282
B to Z ↑	0.0174	0.0181	1.6815	1.2844
C to Z ↓	0.0101	0.0103	1.0554	0.7797
C to Z ↑	0.0101	0.0105	0.9082	0.6920
	X46_P10		**X46_P10**	
A to Z ↓	0.0135		0.4326	
A to Z ↑	0.0192		0.6459	
B to Z ↓	0.0111		0.4282	
B to Z ↑	0.0177		0.6499	
C to Z ↓	0.0104		0.4055	
C to Z ↑	0.0102		0.3501	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	4.623e-07	1.000e-20
X11_P10	9.723e-07	1.000e-20
X17_P10	1.430e-06	1.000e-20
X23_P10	1.919e-06	1.000e-20
X46_P10	3.725e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	2.787e-05	6.365e-05	8.896e-05	1.772e-04
B (output stable)	1.429e-05	3.424e-05	4.887e-05	9.449e-05
C (output stable)	2.948e-04	6.858e-04	8.157e-04	1.299e-03
A to Z	1.688e-03	3.583e-03	5.000e-03	7.499e-03
B to Z	1.328e-03	2.850e-03	3.849e-03	5.477e-03
C to Z	9.870e-04	2.149e-03	2.935e-03	4.237e-03
	X46_P10			
A (output stable)	3.222e-04			
B (output stable)	1.833e-04			
C (output stable)	2.408e-03			
A to Z	1.441e-02			
B to Z	1.045e-02			
C to Z	8.113e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

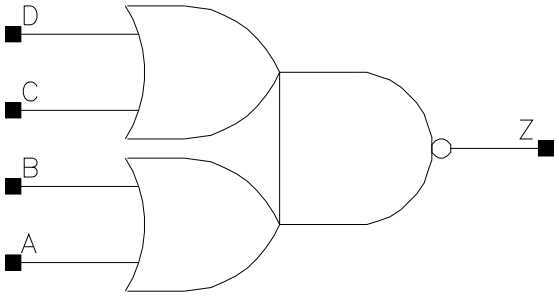
	X46_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0009	0.0018	0.0027	0.0037
B	0.0009	0.0017	0.0024	0.0033
C	0.0008	0.0017	0.0026	0.0035
D	0.0008	0.0016	0.0023	0.0032
	X42_P10			
A	0.0074			
B	0.0067			
C	0.0070			
D	0.0065			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0146	0.0156	3.1748	1.5797
A to Z ↑	0.0217	0.0220	5.6379	2.5836
B to Z ↓	0.0128	0.0134	3.1059	1.5842
B to Z ↑	0.0214	0.0203	5.6596	2.5993
C to Z ↓	0.0131	0.0142	3.2379	1.5970
C to Z ↑	0.0158	0.0172	5.5058	2.5915
D to Z ↓	0.0108	0.0112	3.1521	1.6078
D to Z ↑	0.0151	0.0142	5.5394	2.6160
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0149	0.0152	1.0820	0.7793
A to Z ↑	0.0206	0.0214	1.7403	1.2818
B to Z ↓	0.0129	0.0129	1.0854	0.7785
B to Z ↑	0.0195	0.0200	1.7519	1.2895
C to Z ↓	0.0137	0.0138	1.0960	0.7886
C to Z ↑	0.0157	0.0162	1.7472	1.2841
D to Z ↓	0.0111	0.0110	1.1078	0.7919
D to Z ↑	0.0137	0.0139	1.7640	1.2955
	X42_P10		**X42_P10**	
A to Z ↓	0.0154		0.4091	
A to Z ↑	0.0214		0.6539	
B to Z ↓	0.0131		0.4046	
B to Z ↑	0.0200		0.6578	
C to Z ↓	0.0144		0.4156	
C to Z ↑	0.0163		0.6502	
D to Z ↓	0.0114		0.4121	
D to Z ↑	0.0140		0.6563	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	5.523e-07	1.000e-20
X10_P10	1.175e-06	1.000e-20
X15_P10	1.695e-06	1.000e-20
X21_P10	2.318e-06	1.000e-20
X42_P10	4.544e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	3.546e-05	1.196e-04	1.519e-04	2.217e-04
B (output stable)	2.220e-05	8.728e-05	1.051e-04	1.430e-04
C (output stable)	8.211e-05	2.450e-04	2.885e-04	4.346e-04
D (output stable)	9.677e-05	2.509e-04	3.200e-04	4.603e-04
A to Z	2.039e-03	4.613e-03	6.305e-03	8.961e-03
B to Z	1.692e-03	3.567e-03	4.879e-03	6.928e-03
C to Z	1.393e-03	3.357e-03	4.462e-03	6.333e-03
D to Z	1.077e-03	2.294e-03	3.130e-03	4.400e-03
	X42_P10			
A (output stable)	4.331e-04			
B (output stable)	2.899e-04			
C (output stable)	8.444e-04			
D (output stable)	9.080e-04			

A to Z	1.765e-02			
B to Z	1.359e-02			
C to Z	1.256e-02			
D to Z	8.742e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

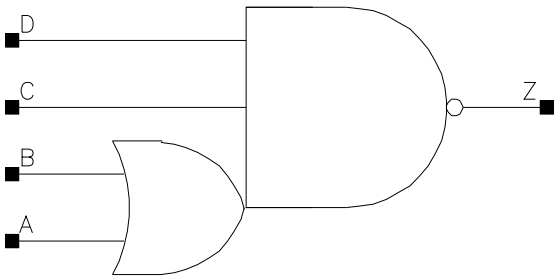
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X21_P10	1.200	2.448	2.9376
X31_P10	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X21_P10	X31_P10
A	0.0009	0.0017	0.0034	0.0050
B	0.0011	0.0016	0.0031	0.0046
C	0.0009	0.0018	0.0036	0.0054
D	0.0009	0.0017	0.0034	0.0051

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0181	0.0175	4.3567	2.3328
A to Z ↑	0.0199	0.0185	5.0821	2.5616
B to Z ↓	0.0157	0.0139	4.4133	2.3458
B to Z ↑	0.0192	0.0164	5.1274	2.5818
C to Z ↓	0.0165	0.0171	4.1141	2.1965

C to Z ↑	0.0177	0.0173	2.6375	1.3280
D to Z ↓	0.0174	0.0166	4.1357	2.2086
D to Z ↑	0.0168	0.0157	2.6736	1.3316
	X21_P10	**X31_P10**	**X21_P10**	**X31_P10**
A to Z ↓	0.0175	0.0176	1.2178	0.8271
A to Z ↑	0.0178	0.0176	1.2795	0.8598
B to Z ↓	0.0139	0.0139	1.2259	0.8354
B to Z ↑	0.0158	0.0156	1.2896	0.8670
C to Z ↓	0.0168	0.0168	1.1478	0.7808
C to Z ↑	0.0168	0.0168	0.6735	0.4551
D to Z ↓	0.0166	0.0167	1.1536	0.7848
D to Z ↑	0.0153	0.0153	0.6749	0.4548

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	4.369e-07	1.000e-20
X10_P10	8.326e-07	1.000e-20
X21_P10	1.596e-06	1.000e-20
X31_P10	2.361e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	1.573e-04	3.236e-04	6.152e-04	9.136e-04
B (output stable)	1.108e-04	2.097e-04	3.959e-04	5.871e-04
C (output stable)	2.623e-05	7.914e-05	1.357e-04	1.841e-04
D (output stable)	6.803e-05	2.150e-04	3.715e-04	5.217e-04
A to Z	1.977e-03	3.469e-03	6.606e-03	9.664e-03
B to Z	1.471e-03	2.435e-03	4.578e-03	6.719e-03
C to Z	2.375e-03	4.594e-03	8.667e-03	1.274e-02
D to Z	2.130e-03	3.819e-03	7.223e-03	1.066e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

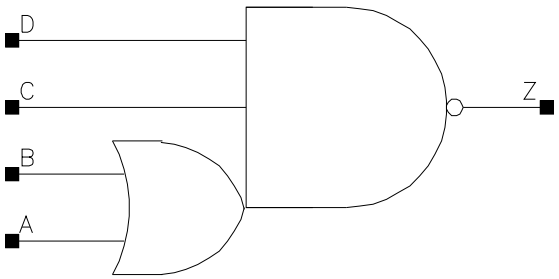
Pin Cycle (vdds)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0010	0.0019	0.0028	0.0037
B	0.0009	0.0017	0.0025	0.0034
C	0.0009	0.0017	0.0026	0.0035
D	0.0009	0.0017	0.0025	0.0033

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0172	0.0185	4.4415	2.3193
A to Z ↑	0.0216	0.0236	4.9344	2.5164
B to Z ↓	0.0149	0.0157	4.3622	2.3224
B to Z ↑	0.0217	0.0223	4.9566	2.5303
C to Z ↓	0.0136	0.0154	4.1983	2.2111

C to Z ↑	0.0139	0.0147	2.6905	1.3609
D to Z ↓	0.0136	0.0144	4.2285	2.2266
D to Z ↑	0.0121	0.0123	2.7112	1.3722
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0182	0.0184	1.5952	1.2043
A to Z ↑	0.0226	0.0232	1.6970	1.2876
B to Z ↓	0.0156	0.0156	1.5894	1.2026
B to Z ↑	0.0218	0.0222	1.7073	1.2943
C to Z ↓	0.0150	0.0153	1.5164	1.1454
C to Z ↑	0.0140	0.0143	0.9067	0.6824
D to Z ↓	0.0141	0.0145	1.5280	1.1534
D to Z ↑	0.0117	0.0121	0.9148	0.6885

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P10	4.520e-07	1.000e-20
X10_P10	8.851e-07	1.000e-20
X15_P10	1.264e-06	1.000e-20
X21_P10	1.713e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	1.814e-05	4.877e-05	6.256e-05	8.838e-05
B (output stable)	1.156e-05	3.611e-05	4.392e-05	6.265e-05
C (output stable)	8.014e-05	1.661e-04	2.353e-04	3.181e-04
D (output stable)	1.860e-04	5.903e-04	7.266e-04	1.060e-03
A to Z	2.314e-03	5.055e-03	7.126e-03	9.782e-03
B to Z	1.915e-03	3.962e-03	5.629e-03	7.675e-03
C to Z	1.496e-03	3.366e-03	4.669e-03	6.489e-03
D to Z	1.243e-03	2.650e-03	3.686e-03	5.091e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

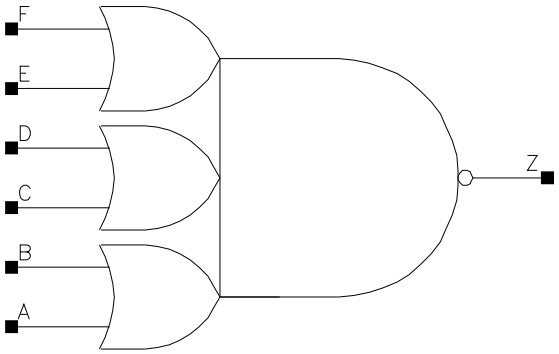
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	1.088	1.3056
X9_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X9_P10
A	0.0008	0.0019
B	0.0007	0.0017
C	0.0007	0.0018
D	0.0007	0.0016
E	0.0007	0.0017
F	0.0007	0.0016

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X9_P10	X3_P10	X9_P10
A to Z ↓	0.0216	0.0230	5.0995	2.1069
A to Z ↑	0.0289	0.0277	6.9613	2.5342
B to Z ↓	0.0201	0.0205	5.1400	2.1100
B to Z ↑	0.0298	0.0268	6.9872	2.5452
C to Z ↓	0.0209	0.0218	5.1470	2.1199
C to Z ↑	0.0251	0.0240	6.9843	2.5292
D to Z ↓	0.0191	0.0191	5.1896	2.1260
D to Z ↑	0.0257	0.0228	7.0178	2.5429
E to Z ↓	0.0180	0.0192	5.1880	2.1258
E to Z ↑	0.0195	0.0190	7.0123	2.5331
F to Z ↓	0.0162	0.0159	5.2353	2.1327
F to Z ↑	0.0197	0.0168	7.0638	2.5543

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X3_P10	4.929e-07	1.000e-20
X9_P10	1.433e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X3_P10	X9_P10
A (output stable)	2.241e-05	9.763e-05
B (output stable)	1.312e-05	7.090e-05
C (output stable)	5.736e-05	1.873e-04
D (output stable)	7.088e-05	2.059e-04
E (output stable)	8.774e-05	2.343e-04
F (output stable)	1.811e-04	4.391e-04
A to Z	2.659e-03	6.965e-03
B to Z	2.388e-03	5.914e-03
C to Z	2.153e-03	5.668e-03
D to Z	1.896e-03	4.674e-03
E to Z	1.557e-03	4.307e-03
F to Z	1.319e-03	3.280e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

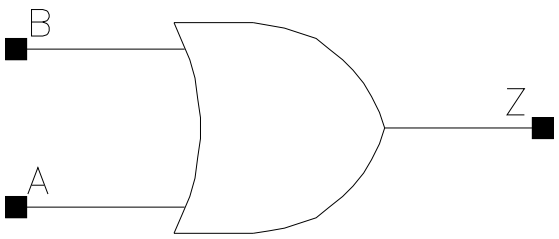
Pin Cycle (vdds)	X3_P10	X9_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X33_P10	1.200	1.360	1.6320
X50_P10	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P10	X16_P10	X33_P10	X50_P10
A	0.0008	0.0010	0.0020	0.0021
B	0.0007	0.0010	0.0021	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0337	0.0298	1.8342	0.9273
A to Z ↑	0.0218	0.0230	2.6228	1.3251
B to Z ↓	0.0339	0.0302	1.8339	0.9265
B to Z ↑	0.0206	0.0214	2.6255	1.3255
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0308	0.0364	0.4590	0.3160
A to Z ↑	0.0228	0.0230	0.6446	0.4365
B to Z ↓	0.0297	0.0358	0.4592	0.3161
B to Z ↑	0.0207	0.0214	0.6436	0.4360

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	4.618e-07	1.000e-20
X16_P10	9.096e-07	1.000e-20
X33_P10	1.830e-06	1.000e-20
X50_P10	2.377e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	2.564e-05	4.645e-05	1.558e-04	1.477e-04
B (output stable)	8.495e-06	1.533e-05	1.136e-04	9.850e-05
A to Z	2.613e-03	4.270e-03	8.899e-03	1.226e-02
B to Z	2.422e-03	3.935e-03	7.855e-03	1.127e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

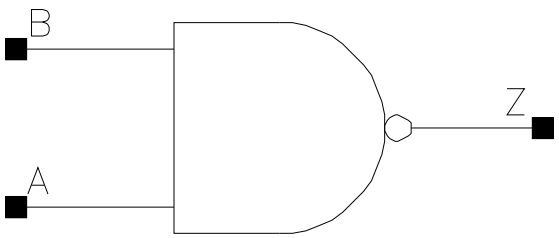
Pin Cycle (vdds)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X16_P10	1.200	0.952	1.1424
X24_P10	1.200	1.088	1.3056
X32_P10	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P10	X16_P10	X24_P10	X32_P10
A	0.0011	0.0011	0.0011	0.0011
B	0.0012	0.0012	0.0012	0.0012

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0287	0.0299	1.7843	0.9294
A to Z ↑	0.0307	0.0317	2.6571	1.3594
B to Z ↓	0.0299	0.0311	1.7835	0.9285
B to Z ↑	0.0292	0.0296	2.6581	1.3598
	X24_P10	**X32_P10**	**X24_P10**	**X32_P10**
A to Z ↓	0.0329	0.0342	0.6290	0.4714
A to Z ↑	0.0340	0.0349	0.9093	0.6789
B to Z ↓	0.0342	0.0357	0.6286	0.4717
B to Z ↑	0.0319	0.0335	0.9089	0.6781

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	1.075e-06	1.000e-20
X16_P10	1.342e-06	1.000e-20
X24_P10	1.592e-06	1.000e-20
X32_P10	2.143e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	2.391e-05	2.404e-05	2.412e-05	2.491e-05
B (output stable)	7.735e-05	7.742e-05	7.770e-05	7.963e-05
A to Z	5.012e-03	5.837e-03	7.410e-03	9.875e-03
B to Z	4.774e-03	5.609e-03	7.197e-03	9.638e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

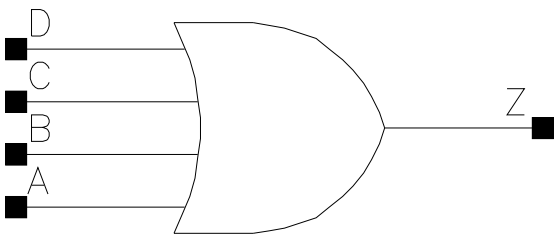
Pin Cycle (vdds)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P10	1.200	2.176	2.6112
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P10	X27_P10
A	0.0018	0.0021
B	0.0017	0.0021
C	0.0018	0.0022
D	0.0017	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P10	X27_P10	X20_P10	X27_P10
A to Z ↓	0.0344	0.0359	1.0948	0.8184
A to Z ↑	0.0236	0.0229	0.8650	0.6440
B to Z ↓	0.0338	0.0347	1.0951	0.8187
B to Z ↑	0.0222	0.0211	0.8644	0.6434
C to Z ↓	0.0330	0.0346	1.0936	0.8175
C to Z ↑	0.0224	0.0223	0.8665	0.6469
D to Z ↓	0.0324	0.0337	1.0936	0.8179
D to Z ↑	0.0209	0.0206	0.8652	0.6461

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X20_P10	1.558e-06	1.000e-20
X27_P10	2.296e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X20_P10	X27_P10
A (output stable)	1.962e-03	2.724e-03
B (output stable)	1.625e-03	2.222e-03
C (output stable)	1.828e-03	2.641e-03
D (output stable)	1.474e-03	2.151e-03
A to Z	8.271e-03	1.158e-02
B to Z	7.550e-03	1.046e-02
C to Z	7.196e-03	9.960e-03
D to Z	6.481e-03	8.968e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

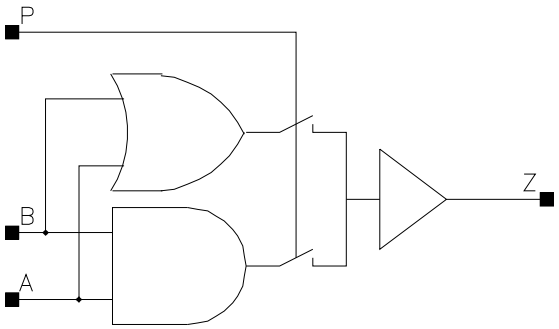
Pin Cycle (vdds)	X20_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X16_P10	1.200	1.224	1.4688
X25_P10	1.200	2.040	2.4480
X33_P10	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0013	0.0020	0.0034	0.0035
B	0.0013	0.0019	0.0039	0.0039
P	0.0007	0.0011	0.0020	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0410	0.0372	1.8686	0.9147
A to Z ↑	0.0288	0.0274	2.6692	1.3358
B to Z ↓	0.0409	0.0374	1.8777	0.9208
B to Z ↑	0.0298	0.0283	2.6730	1.3380
P to Z ↓	0.0376	0.0347	1.8789	0.9206
P to Z ↑	0.0289	0.0276	2.6699	1.3374
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**

A to Z ↓	0.0355	0.0376	0.6226	0.4705
A to Z ↑	0.0270	0.0282	0.8995	0.6731
B to Z ↓	0.0355	0.0372	0.6260	0.4730
B to Z ↑	0.0282	0.0292	0.9005	0.6740
P to Z ↓	0.0336	0.0357	0.6265	0.4732
P to Z ↑	0.0270	0.0282	0.8994	0.6731

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	5.919e-07	1.000e-20
X16_P10	1.298e-06	1.000e-20
X25_P10	2.190e-06	1.000e-20
X33_P10	2.516e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	5.484e-05	8.944e-05	1.819e-04	1.843e-04
B (output stable)	1.163e-04	1.425e-04	2.692e-04	2.684e-04
P (output stable)	1.385e-04	2.341e-04	4.036e-04	4.126e-04
A to Z	3.047e-03	5.248e-03	8.954e-03	1.030e-02
B to Z	2.947e-03	5.090e-03	8.543e-03	9.898e-03
P to Z	2.672e-03	4.687e-03	8.012e-03	9.372e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

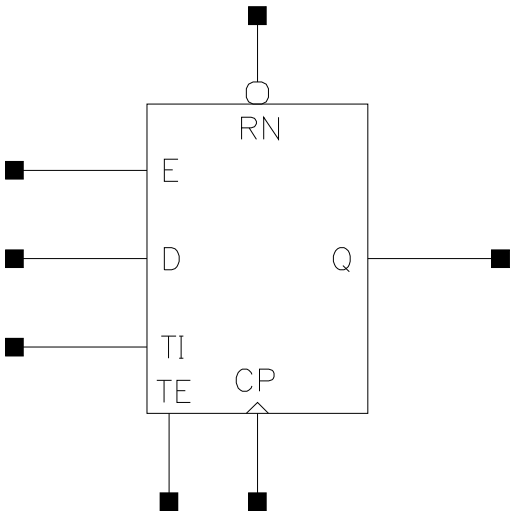
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.488	5.3856
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0011	0.0011
RN	0.0009	0.0008	0.0008	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to Q ↓	0.0747	0.0407	3.9441	1.8191
CP to Q ↑	0.0621	0.0533	5.4861	2.6438
RN to Q ↓	0.0644	0.0560	3.4473	1.9071
	X17_P10	X33_P10	X17_P10	X33_P10
CP to Q ↓	0.0696	0.0732	0.8884	0.4667
CP to Q ↑	0.0857	0.0898	1.2925	0.6608
RN to Q ↓	0.0922	0.0956	0.8875	0.4664

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1016	0.0675	0.0682	0.0682
CP ↑	min_pulse_width to CP	0.0676	0.0361	0.0314	0.0314
D ↓	hold_rising to CP	-0.1065	-0.0511	-0.0511	-0.0511
D ↑	hold_rising to CP	-0.0626	-0.0212	-0.0212	-0.0212
D ↓	setup_rising to CP	0.1485	0.0928	0.0928	0.0955
D ↑	setup_rising to CP	0.0951	0.0515	0.0515	0.0515
E ↓	hold_rising to CP	-0.0701	-0.0691	-0.0750	-0.0750
E ↑	hold_rising to CP	-0.0577	-0.0218	-0.0218	-0.0218
E ↓	setup_rising to CP	0.1285	0.1263	0.1263	0.1263
E ↑	setup_rising to CP	0.1394	0.0982	0.0982	0.0982
RN ↓	min_pulse_width to RN	0.0686	0.0757	0.0637	0.0659
RN ↑	recovery_rising to CP	0.0173	0.0173	0.0173	0.0173
RN ↑	removal_rising to CP	-0.0125	-0.0077	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0502	-0.0306	-0.0338	-0.0334
TE ↑	hold_rising to CP	-0.0382	-0.0235	-0.0262	-0.0262
TE ↓	setup_rising to CP	0.0949	0.0749	0.0781	0.0781
TE ↑	setup_rising to CP	0.1763	0.1242	0.1242	0.1275
TI ↓	hold_rising to CP	-0.1342	-0.0689	-0.0732	-0.0732
TI ↑	hold_rising to CP	-0.0488	-0.0266	-0.0266	-0.0266
TI ↓	setup_rising to CP	0.1738	0.1141	0.1141	0.1141
TI ↑	setup_rising to CP	0.0786	0.0563	0.0563	0.0563

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.705e-06	1.000e-20
X8_P10	1.970e-06	1.000e-20
X17_P10	2.528e-06	1.000e-20
X33_P10	3.358e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

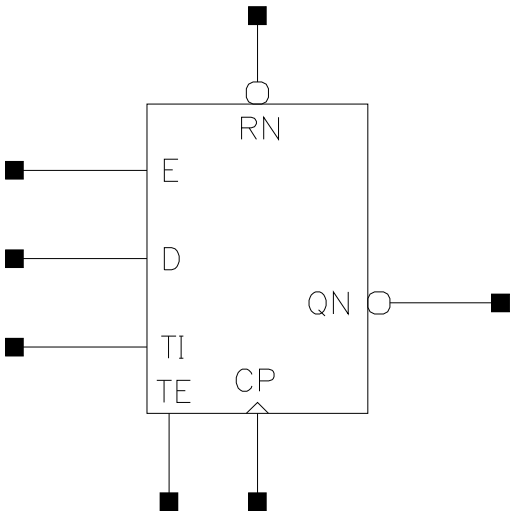
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	9.226e-03	9.301e-03	9.320e-03	9.330e-03
Clock 100Mhz Data 25Mhz	9.893e-03	1.006e-02	1.083e-02	1.173e-02
Clock 100Mhz Data 50Mhz	1.056e-02	1.082e-02	1.235e-02	1.413e-02
Clock = 0 Data 100Mhz	6.788e-03	6.587e-03	6.522e-03	6.491e-03
Clock = 1 Data 100Mhz	2.539e-03	2.593e-03	2.614e-03	2.625e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.624	5.5488
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0011	0.0011
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to QN ↓	0.0763	0.0720	3.3742	1.7572
CP to QN ↑	0.0830	0.0537	5.3653	2.5644
RN to QN ↑	0.0780	0.0779	5.3465	2.5615
	X17_P10	X33_P10	X17_P10	X33_P10
CP to QN ↓	0.0687	0.0724	0.8893	0.4662
CP to QN ↑	0.0559	0.0607	1.2940	0.6613
RN to QN ↑	0.0768	0.0845	1.2988	0.6638

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1016	0.0682	0.0682	0.0682
CP ↑	min_pulse_width to CP	0.0502	0.0314	0.0347	0.0360
D ↓	hold_rising to CP	-0.1092	-0.0511	-0.0511	-0.0511
D ↑	hold_rising to CP	-0.0626	-0.0212	-0.0212	-0.0212
D ↓	setup_rising to CP	0.1511	0.0928	0.0928	0.0923
D ↑	setup_rising to CP	0.0951	0.0515	0.0515	0.0515
E ↓	hold_rising to CP	-0.0701	-0.0750	-0.0691	-0.0691
E ↑	hold_rising to CP	-0.0577	-0.0218	-0.0218	-0.0218
E ↓	setup_rising to CP	0.1317	0.1269	0.1263	0.1263
E ↑	setup_rising to CP	0.1421	0.0982	0.0982	0.0982
RN ↓	min_pulse_width to RN	0.0659	0.0637	0.0779	0.0828
RN ↑	recovery_rising to CP	0.0173	0.0173	0.0173	0.0173
RN ↑	removal_rising to CP	-0.0125	-0.0076	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0502	-0.0338	-0.0306	-0.0306
TE ↑	hold_rising to CP	-0.0382	-0.0235	-0.0235	-0.0235
TE ↓	setup_rising to CP	0.0944	0.0781	0.0781	0.0781
TE ↑	setup_rising to CP	0.1759	0.1275	0.1275	0.1275
TI ↓	hold_rising to CP	-0.1342	-0.0732	-0.0689	-0.0689
TI ↑	hold_rising to CP	-0.0488	-0.0266	-0.0266	-0.0266
TI ↓	setup_rising to CP	0.1738	0.1141	0.1134	0.1134
TI ↑	setup_rising to CP	0.0786	0.0563	0.0563	0.0563

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.707e-06	1.000e-20
X8_P10	1.913e-06	1.000e-20
X17_P10	2.416e-06	1.000e-20
X33_P10	3.112e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

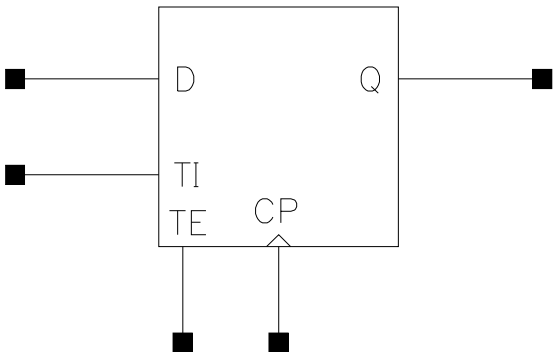
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	9.226e-03	9.302e-03	9.316e-03	9.324e-03
Clock 100Mhz Data 25Mhz	9.851e-03	1.011e-02	1.077e-02	1.166e-02
Clock 100Mhz Data 50Mhz	1.048e-02	1.093e-02	1.223e-02	1.400e-02
Clock = 0 Data 100Mhz	6.785e-03	6.584e-03	6.519e-03	6.487e-03
Clock = 1 Data 100Mhz	2.537e-03	2.595e-03	2.616e-03	2.627e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.400	4.0800
X8_P10	1.200	3.128	3.7536
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0614	0.0380	3.7273	1.8217
CP to Q ↑	0.0558	0.0487	5.5099	2.6053
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0571	0.0627	0.8725	0.4586
CP to Q ↑	0.0834	0.0885	1.2914	0.6600

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0888	0.0937	0.0937	0.0937
CP ↑	min_pulse_width to CP	0.0469	0.0314	0.0301	0.0302
D ↓	hold_rising to CP	-0.0653	-0.0240	-0.0240	-0.0240
D ↑	hold_rising to CP	-0.0230	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0998	0.0635	0.0635	0.0635
D ↑	setup_rising to CP	0.0535	0.0261	0.0261	0.0261
TE ↓	hold_rising to CP	-0.0408	-0.0218	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0337	-0.0159	-0.0191	-0.0191
TE ↓	setup_rising to CP	0.0798	0.0610	0.0610	0.0610
TE ↑	setup_rising to CP	0.1568	0.1275	0.1275	0.1275
TI ↓	hold_rising to CP	-0.1253	-0.0802	-0.0794	-0.0794
TI ↑	hold_rising to CP	-0.0390	-0.0172	-0.0172	-0.0172
TI ↓	setup_rising to CP	0.1592	0.1238	0.1238	0.1238
TI ↑	setup_rising to CP	0.0630	0.0479	0.0479	0.0479

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.385e-06	1.000e-20
X8_P10	1.653e-06	1.000e-20
X17_P10	2.390e-06	1.000e-20
X33_P10	3.018e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

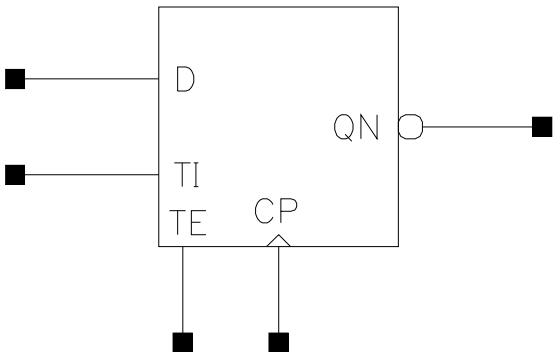
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	8.336e-03	8.419e-03	8.440e-03	8.450e-03
Clock 100Mhz Data 25Mhz	8.336e-03	8.471e-03	9.228e-03	1.000e-02
Clock 100Mhz Data 50Mhz	8.337e-03	8.523e-03	1.002e-02	1.156e-02
Clock = 0 Data 100Mhz	5.360e-03	5.056e-03	4.955e-03	4.904e-03
Clock = 1 Data 100Mhz	1.430e-03	7.416e-04	5.121e-04	3.974e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.536	4.2432
X8_P10	1.200	3.264	3.9168
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0715	0.0762	3.8332	1.8114
CP to QN ↑	0.0665	0.0493	5.4630	2.5689
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0591	0.0653	0.8734	0.4593
CP to QN ↑	0.0493	0.0546	1.2907	0.6593

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0881	0.0937	0.0937	0.0937
CP ↑	min_pulse_width to CP	0.0374	0.0301	0.0314	0.0314
D ↓	hold_rising to CP	-0.0653	-0.0240	-0.0240	-0.0240
D ↑	hold_rising to CP	-0.0230	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0966	0.0635	0.0635	0.0635
D ↑	setup_rising to CP	0.0535	0.0265	0.0261	0.0261
TE ↓	hold_rising to CP	-0.0399	-0.0218	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0337	-0.0191	-0.0163	-0.0163
TE ↓	setup_rising to CP	0.0804	0.0610	0.0610	0.0610
TE ↑	setup_rising to CP	0.1535	0.1275	0.1275	0.1275
TI ↓	hold_rising to CP	-0.1237	-0.0794	-0.0759	-0.0759
TI ↑	hold_rising to CP	-0.0390	-0.0172	-0.0172	-0.0172
TI ↓	setup_rising to CP	0.1592	0.1238	0.1238	0.1238
TI ↑	setup_rising to CP	0.0645	0.0479	0.0479	0.0479

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.397e-06	1.000e-20
X8_P10	1.662e-06	1.000e-20
X17_P10	2.375e-06	1.000e-20
X33_P10	3.003e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

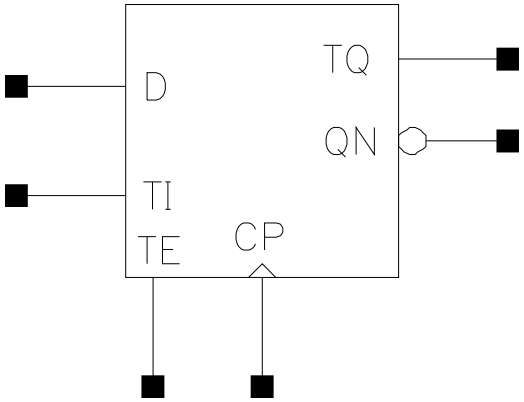
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	8.254e-03	8.401e-03	8.448e-03	8.473e-03
Clock 100Mhz Data 25Mhz	8.307e-03	8.575e-03	9.199e-03	9.996e-03
Clock 100Mhz Data 50Mhz	8.359e-03	8.748e-03	9.950e-03	1.152e-02
Clock = 0 Data 100Mhz	5.383e-03	5.066e-03	4.962e-03	4.910e-03
Clock = 1 Data 100Mhz	1.421e-03	7.598e-04	5.395e-04	4.294e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.536	4.2432
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0013	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
TE	0.0009	0.0011	0.0011	0.0011

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0794	0.0689	3.4890	1.7737
CP to QN ↑	0.0808	0.0515	5.3690	2.5818
CP to TQ ↓	0.0568	0.0350	4.7275	3.3017
CP to TQ ↑	0.0574	0.0485	10.3451	7.3182
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0651	0.0704	0.8918	0.4692
CP to QN ↑	0.0532	0.0573	1.3094	0.6748
CP to TQ ↓	0.0362	0.0376	4.3720	4.3901
CP to TQ ↑	0.0493	0.0507	9.5139	10.0313

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0881	0.0920	0.0937	0.0937
CP ↑	min_pulse_width to CP	0.0468	0.0314	0.0314	0.0314
D ↓	hold_rising to CP	-0.0653	-0.0240	-0.0240	-0.0240
D ↑	hold_rising to CP	-0.0235	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0975	0.0635	0.0635	0.0635
D ↑	setup_rising to CP	0.0535	0.0261	0.0261	0.0261
TE ↓	hold_rising to CP	-0.0408	-0.0218	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0337	-0.0191	-0.0191	-0.0191
TE ↓	setup_rising to CP	0.0804	0.0613	0.0610	0.0613
TE ↑	setup_rising to CP	0.1541	0.1275	0.1275	0.1275
TI ↓	hold_rising to CP	-0.1244	-0.0759	-0.0759	-0.0759
TI ↑	hold_rising to CP	-0.0390	-0.0172	-0.0172	-0.0172
TI ↓	setup_rising to CP	0.1592	0.1238	0.1238	0.1238
TI ↑	setup_rising to CP	0.0630	0.0479	0.0479	0.0479

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.477e-06	1.000e-20
X8_P10	1.833e-06	1.000e-20
X17_P10	2.237e-06	1.000e-20
X33_P10	2.981e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10

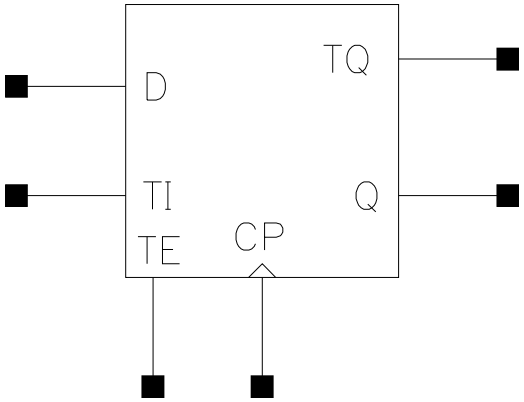
Clock 100Mhz Data 0Mhz	8.456e-03	8.482e-03	8.488e-03	8.495e-03
Clock 100Mhz Data 25Mhz	8.665e-03	8.891e-03	9.222e-03	1.011e-02
Clock 100Mhz Data 50Mhz	8.873e-03	9.301e-03	9.957e-03	1.172e-02
Clock = 0 Data 100Mhz	5.375e-03	5.068e-03	4.967e-03	4.917e-03
Clock = 1 Data 100Mhz	1.432e-03	7.399e-04	5.094e-04	3.942e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.400	4.0800
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007

TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to Q ↓	0.0803	0.0424	3.9351	1.8102
CP to Q ↑	0.0638	0.0517	5.5844	2.6239
CP to TQ ↓	0.0771	0.0435	3.9147	4.4809
CP to TQ ↑	0.0653	0.0566	7.3833	10.1590
	X17_P10	X33_P10	X17_P10	X33_P10
CP to Q ↓	0.0586	0.0641	0.8981	0.4684
CP to Q ↑	0.0849	0.0898	1.3211	0.6641
CP to TQ ↓	0.0608	0.0672	4.3419	4.4150
CP to TQ ↑	0.0900	0.0968	9.9166	10.0332

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0888	0.0937	0.0937	0.0937
CP ↑	min_pulse_width to CP	0.0693	0.0314	0.0301	0.0302
D ↓	hold_rising to CP	-0.0653	-0.0240	-0.0240	-0.0240
D ↑	hold_rising to CP	-0.0230	-0.0017	-0.0017	-0.0017
D ↓	setup_rising to CP	0.0998	0.0635	0.0635	0.0635
D ↑	setup_rising to CP	0.0535	0.0261	0.0261	0.0261
TE ↓	hold_rising to CP	-0.0408	-0.0218	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0337	-0.0163	-0.0191	-0.0191
TE ↓	setup_rising to CP	0.0798	0.0610	0.0610	0.0610
TE ↑	setup_rising to CP	0.1535	0.1275	0.1275	0.1275
TI ↓	hold_rising to CP	-0.1253	-0.0759	-0.0794	-0.0794
TI ↑	hold_rising to CP	-0.0390	-0.0175	-0.0172	-0.0172
TI ↓	setup_rising to CP	0.1592	0.1238	0.1238	0.1238
TI ↑	setup_rising to CP	0.0630	0.0479	0.0479	0.0479

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.508e-06	1.000e-20
X8_P10	1.730e-06	1.000e-20
X17_P10	2.449e-06	1.000e-20
X33_P10	3.074e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

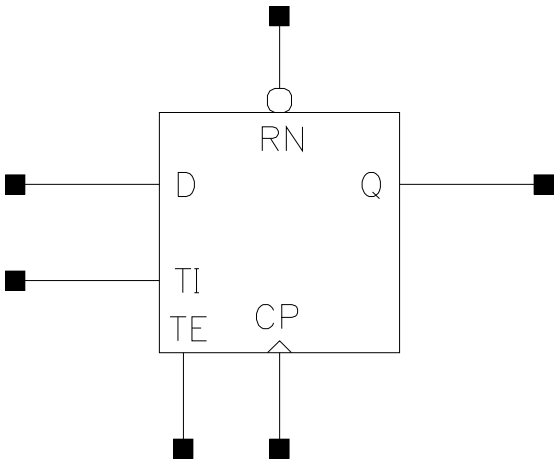
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	8.306e-03	8.399e-03	8.429e-03	8.443e-03
Clock 100Mhz Data 25Mhz	8.699e-03	8.702e-03	9.435e-03	1.024e-02
Clock 100Mhz Data 50Mhz	9.092e-03	9.004e-03	1.044e-02	1.203e-02
Clock = 0 Data 100Mhz	5.349e-03	5.047e-03	4.949e-03	4.900e-03
Clock = 1 Data 100Mhz	1.419e-03	7.336e-04	5.052e-04	3.911e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.672	4.4064
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
RN	0.0009	0.0007	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0734	0.0406	4.0044	1.8222
CP to Q ↑	0.0614	0.0523	5.5098	2.6443
RN to Q ↓	0.0636	0.0567	3.4926	1.8925
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0597	0.0657	0.8814	0.4654
CP to Q ↑	0.0760	0.0807	1.2886	0.6597
RN to Q ↓	0.0828	0.0888	0.8812	0.4649

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1000	0.0954	0.0984	0.0984
CP ↑	min_pulse_width to CP	0.0611	0.0314	0.0315	0.0315
D ↓	hold_rising to CP	-0.0551	-0.0143	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0284	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0998	0.0613	0.0639	0.0639
D ↑	setup_rising to CP	0.0584	0.0368	0.0368	0.0368
RN ↓	min_pulse_width to RN	0.0659	0.0708	0.0637	0.0637
RN ↑	recovery_rising to CP	0.0173	0.0173	0.0173	0.0173
RN ↑	removal_rising to CP	-0.0125	-0.0077	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0409	-0.0120	-0.0120	-0.0116
TE ↑	hold_rising to CP	-0.0382	-0.0240	-0.0266	-0.0266
TE ↓	setup_rising to CP	0.0804	0.0582	0.0640	0.0608
TE ↑	setup_rising to CP	0.1541	0.1226	0.1226	0.1226
TI ↓	hold_rising to CP	-0.1139	-0.0648	-0.0648	-0.0648
TI ↑	hold_rising to CP	-0.0437	-0.0279	-0.0279	-0.0279
TI ↓	setup_rising to CP	0.1592	0.1189	0.1189	0.1189
TI ↑	setup_rising to CP	0.0734	0.0576	0.0576	0.0576

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.575e-06	1.000e-20
X8_P10	1.798e-06	1.000e-20
X17_P10	2.491e-06	1.000e-20
X33_P10	3.201e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	9.239e-03	9.325e-03	9.393e-03	9.429e-03

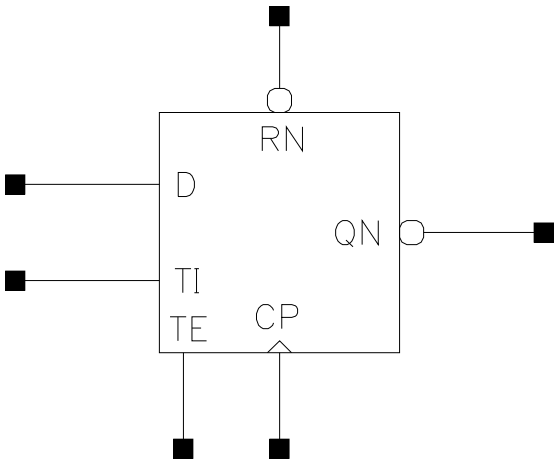
Clock 100Mhz Data 25Mhz	9.314e-03	9.327e-03	1.020e-02	1.103e-02
Clock 100Mhz Data 50Mhz	9.390e-03	9.329e-03	1.101e-02	1.263e-02
Clock = 0 Data 100Mhz	5.498e-03	5.105e-03	4.975e-03	4.910e-03
Clock = 1 Data 100Mhz	1.456e-03	7.811e-04	5.560e-04	4.438e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	3.944	4.7328
X33_P10	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0691	0.0644	3.3024	1.7166
CP to QN ↑	0.0757	0.0484	5.3491	2.5482
RN to QN ↑	0.0722	0.0732	5.3300	2.5440
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0639	0.0700	0.8826	0.4650
CP to QN ↑	0.0535	0.0591	1.3011	0.6688
RN to QN ↑	0.0756	0.0828	1.3047	0.6694

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1000	0.0954	0.0954	0.0954
CP ↑	min_pulse_width to CP	0.0455	0.0314	0.0314	0.0360
D ↓	hold_rising to CP	-0.0577	-0.0143	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0284	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0998	0.0613	0.0613	0.0613
D ↑	setup_rising to CP	0.0584	0.0342	0.0368	0.0368
RN ↓	min_pulse_width to RN	0.0632	0.0637	0.0752	0.0801
RN ↑	recovery_rising to CP	0.0173	0.0200	0.0173	0.0173
RN ↑	removal_rising to CP	-0.0125	-0.0099	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0409	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0382	-0.0266	-0.0240	-0.0240
TE ↓	setup_rising to CP	0.0804	0.0582	0.0582	0.0582
TE ↑	setup_rising to CP	0.1541	0.1226	0.1226	0.1226
TI ↓	hold_rising to CP	-0.1155	-0.0648	-0.0648	-0.0648
TI ↑	hold_rising to CP	-0.0437	-0.0279	-0.0279	-0.0279
TI ↓	setup_rising to CP	0.1592	0.1189	0.1189	0.1189
TI ↑	setup_rising to CP	0.0734	0.0576	0.0576	0.0576

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.593e-06	1.000e-20
X8_P10	1.740e-06	1.000e-20
X17_P10	2.408e-06	1.000e-20
X33_P10	2.943e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	9.150e-03	9.163e-03	9.165e-03	9.167e-03

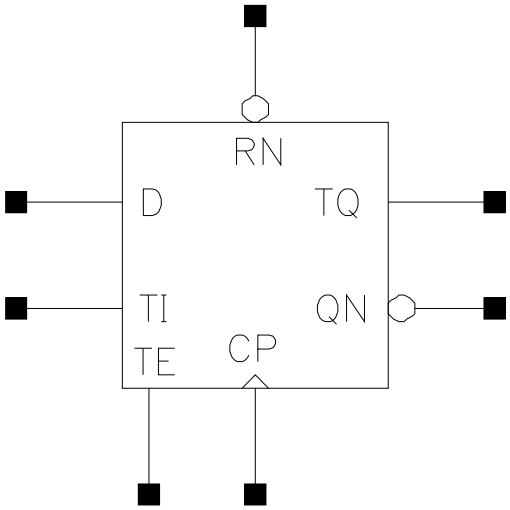
Clock 100Mhz Data 25Mhz	9.173e-03	9.254e-03	9.934e-03	1.071e-02
Clock 100Mhz Data 50Mhz	9.195e-03	9.344e-03	1.070e-02	1.224e-02
Clock = 0 Data 100Mhz	5.500e-03	5.106e-03	4.980e-03	4.916e-03
Clock = 1 Data 100Mhz	1.454e-03	7.521e-04	5.181e-04	4.012e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007

RN	0.0011	0.0008	0.0009	0.0009
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0771	0.0670	3.3104	1.8108
CP to QN ↑	0.0976	0.0540	4.7751	2.6559
CP to TQ ↓	0.0699	0.0371	4.2212	3.4580
CP to TQ ↑	0.0633	0.0527	8.2888	7.6858
RN to QN ↑	0.0715	0.0717	4.8179	2.6494
RN to TQ ↓	0.0500	0.0495	3.8283	3.6094
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0691	0.0747	0.9009	0.4763
CP to QN ↑	0.0549	0.0582	1.3282	0.6705
CP to TQ ↓	0.0384	0.0398	4.2879	4.1895
CP to TQ ↑	0.0527	0.0539	7.2004	7.2934
RN to QN ↑	0.0745	0.0798	1.3257	0.6694
RN to TQ ↓	0.0528	0.0552	4.4383	4.3654

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1000	0.0954	0.0984	0.0984
CP ↑	min_pulse_width to CP	0.0645	0.0314	0.0314	0.0314
D ↓	hold_rising to CP	-0.0551	-0.0143	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0284	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0998	0.0613	0.0613	0.0613
D ↑	setup_rising to CP	0.0584	0.0368	0.0368	0.0368
RN ↓	min_pulse_width to RN	0.0681	0.0681	0.0730	0.0779
RN ↑	recovery_rising to CP	0.0221	0.0173	0.0173	0.0173
RN ↑	removal_rising to CP	-0.0147	-0.0077	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0409	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0382	-0.0240	-0.0266	-0.0266
TE ↓	setup_rising to CP	0.0804	0.0582	0.0608	0.0608
TE ↑	setup_rising to CP	0.1541	0.1226	0.1226	0.1226
TI ↓	hold_rising to CP	-0.1155	-0.0648	-0.0648	-0.0648
TI ↑	hold_rising to CP	-0.0437	-0.0279	-0.0279	-0.0279
TI ↓	setup_rising to CP	0.1592	0.1189	0.1189	0.1189
TI ↑	setup_rising to CP	0.0734	0.0576	0.0576	0.0576

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.739e-06	1.000e-20
X8_P10	1.834e-06	1.000e-20
X17_P10	2.227e-06	1.000e-20
X33_P10	2.889e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

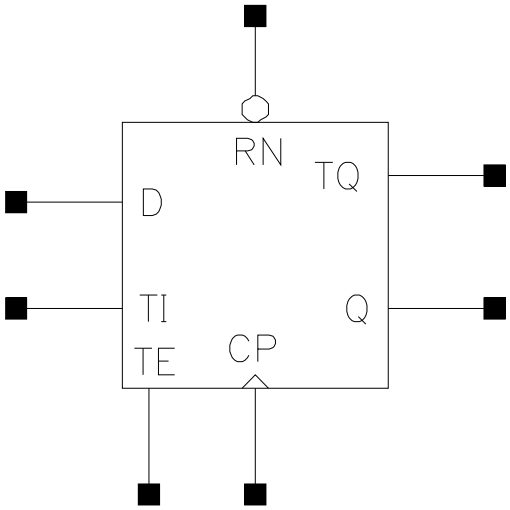
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	9.160e-03	9.196e-03	9.252e-03	9.281e-03
Clock 100Mhz Data 25Mhz	9.438e-03	9.460e-03	9.886e-03	1.081e-02
Clock 100Mhz Data 50Mhz	9.716e-03	9.724e-03	1.052e-02	1.235e-02
Clock = 0 Data 100Mhz	5.490e-03	5.101e-03	4.969e-03	4.902e-03
Clock = 1 Data 100Mhz	1.454e-03	7.809e-04	5.566e-04	4.444e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007

RN	0.0009	0.0009	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0828	0.0439	4.2207	1.8758
CP to Q ↑	0.0655	0.0546	5.7244	2.7518
CP to TQ ↓	0.0790	0.0438	5.2292	4.5297
CP to TQ ↑	0.0677	0.0575	11.1943	10.1502
RN to Q ↓	0.0658	0.0640	3.6543	1.9518
RN to TQ ↓	0.0645	0.0627	4.6043	4.6939
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0621	0.0678	0.8943	0.4721
CP to Q ↑	0.0772	0.0816	1.2947	0.6624
CP to TQ ↓	0.0643	0.0717	4.3683	4.4431
CP to TQ ↑	0.0820	0.0893	10.0386	10.0952
RN to Q ↓	0.0852	0.0909	0.8935	0.4714
RN to TQ ↓	0.0875	0.0948	4.3648	4.4397

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1000	0.0954	0.0954	0.0954
CP ↑	min_pulse_width to CP	0.0705	0.0361	0.0315	0.0314
D ↓	hold_rising to CP	-0.0551	-0.0143	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0284	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0998	0.0613	0.0613	0.0613
D ↑	setup_rising to CP	0.0584	0.0368	0.0368	0.0368
RN ↓	min_pulse_width to RN	0.0708	0.0779	0.0637	0.0637
RN ↑	recovery_rising to CP	0.0173	0.0173	0.0173	0.0173
RN ↑	removal_rising to CP	-0.0125	-0.0077	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0409	-0.0120	-0.0120	-0.0120
TE ↑	hold_rising to CP	-0.0382	-0.0240	-0.0266	-0.0266
TE ↓	setup_rising to CP	0.0804	0.0582	0.0582	0.0582
TE ↑	setup_rising to CP	0.1541	0.1226	0.1226	0.1226
TI ↓	hold_rising to CP	-0.1139	-0.0648	-0.0648	-0.0648
TI ↑	hold_rising to CP	-0.0437	-0.0264	-0.0279	-0.0279
TI ↓	setup_rising to CP	0.1592	0.1189	0.1189	0.1189
TI ↑	setup_rising to CP	0.0734	0.0576	0.0576	0.0576

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.640e-06	1.000e-20
X8_P10	1.865e-06	1.000e-20
X17_P10	2.529e-06	1.000e-20
X33_P10	3.240e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

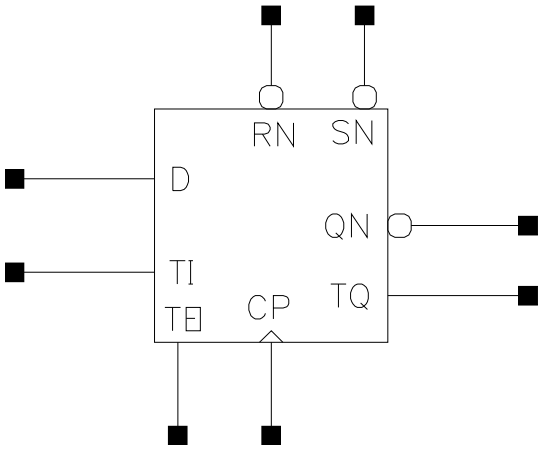
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	9.221e-03	9.312e-03	9.341e-03	9.355e-03
Clock 100Mhz Data 25Mhz	9.496e-03	9.490e-03	1.038e-02	1.120e-02
Clock 100Mhz Data 50Mhz	9.771e-03	9.668e-03	1.142e-02	1.305e-02
Clock = 0 Data 100Mhz	5.495e-03	5.103e-03	4.974e-03	4.909e-03
Clock = 1 Data 100Mhz	1.456e-03	7.511e-04	5.163e-04	3.990e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.352	5.2224
X17_P10	1.200	4.488	5.3856
X33_P10	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0009

SN	0.0014	0.0014	0.0014
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0739	0.0787	1.7526	0.9038
CP to QN ↑	0.0556	0.0583	2.5615	1.3012
CP to TQ ↓	0.0427	0.0426	5.4113	5.4202
CP to TQ ↑	0.0611	0.0611	13.1930	13.2029
RN to QN ↓	0.0800	0.0845	1.7527	0.9045
RN to QN ↑	0.0794	0.0835	2.5670	1.3026
RN to TQ ↓	0.0613	0.0610	5.7843	5.7820
RN to TQ ↑	0.0676	0.0676	13.1731	13.1763
SN to QN ↓	0.0848	0.0905	1.7619	0.9071
SN to TQ ↑	0.0702	0.0701	13.3432	13.3592
	X33_P10		**X33_P10**	
CP to QN ↓	0.0907		0.4827	
CP to QN ↑	0.0655		0.6688	
CP to TQ ↓	0.0427		5.4353	
CP to TQ ↑	0.0613		13.2414	
RN to QN ↓	0.0964		0.4825	
RN to QN ↑	0.0929		0.6685	
RN to TQ ↓	0.0610		5.8109	
RN to TQ ↑	0.0677		13.2086	
SN to QN ↓	0.1040		0.4831	
SN to TQ ↑	0.0702		13.4223	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1014	0.1014	0.1031
CP ↑	min_pulse_width to CP	0.0313	0.0347	0.0361
D ↓	hold_rising to CP	-0.0175	-0.0175	-0.0175
D ↑	hold_rising to CP	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0662	0.0662	0.0662
D ↑	setup_rising to CP	0.0368	0.0368	0.0368
RN ↓	min_pulse_width to RN	0.0752	0.0779	0.0828
RN ↑	non_seq_hold_rising to SN	-0.0287	-0.0288	-0.0288
RN ↑	non_seq_setup_rising to SN	0.0642	0.0642	0.0642
RN ↑	recovery_rising to CP	0.0270	0.0270	0.0270
RN ↑	removal_rising to CP	-0.0174	-0.0174	-0.0174
SN ↓	min_pulse_width to SN	0.0620	0.0647	0.0674
SN ↑	recovery_rising to CP	0.0103	0.0103	0.0103
SN ↑	removal_rising to CP	0.0287	0.0287	0.0287

TE ↓	hold_rising to CP	-0.0116	-0.0116	-0.0116
TE ↑	hold_rising to CP	-0.0240	-0.0240	-0.0240
TE ↓	setup_rising to CP	0.0635	0.0635	0.0635
TE ↑	setup_rising to CP	0.1275	0.1275	0.1275
TI ↓	hold_rising to CP	-0.0648	-0.0648	-0.0648
TI ↑	hold_rising to CP	-0.0279	-0.0279	-0.0279
TI ↓	setup_rising to CP	0.1238	0.1238	0.1238
TI ↑	setup_rising to CP	0.0576	0.0576	0.0576

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	2.041e-06	1.000e-20
X17_P10	2.357e-06	1.000e-20
X33_P10	2.932e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

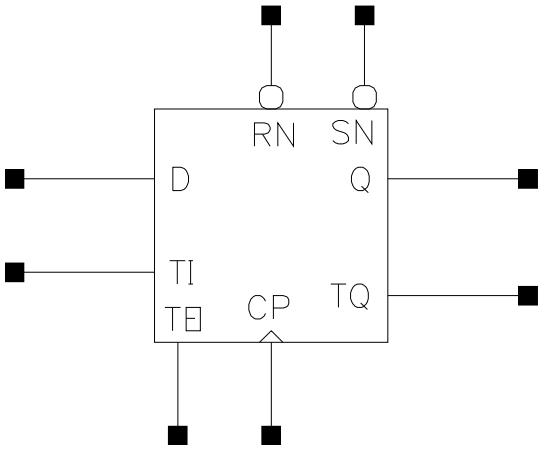
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	9.820e-03	9.820e-03	9.822e-03
Clock 100Mhz Data 25Mhz	9.972e-03	1.034e-02	1.133e-02
Clock 100Mhz Data 50Mhz	1.012e-02	1.086e-02	1.284e-02
Clock = 0 Data 100Mhz	4.898e-03	4.896e-03	4.897e-03
Clock = 1 Data 100Mhz	1.087e-04	1.089e-04	1.090e-04

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.216	5.0592
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010
D	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0009

SN	0.0014	0.0014	0.0014
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
CP to Q ↓	0.0477	0.0534	1.8182	0.9453
CP to Q ↑	0.0596	0.0630	2.6405	1.3485
CP to TQ ↓	0.0485	0.0549	5.5038	5.5756
CP to TQ ↑	0.0657	0.0724	12.8064	12.9058
RN to Q ↓	0.0724	0.0841	2.0349	1.0621
RN to Q ↑	0.0534	0.0607	2.7409	1.4039
RN to TQ ↓	0.0723	0.0842	5.9307	6.0685
RN to TQ ↑	0.0628	0.0753	12.9394	13.0540
SN to Q ↑	0.0706	0.0778	2.7424	1.4051
SN to TQ ↑	0.0800	0.0923	12.9477	13.0560
	X33_P10		X33_P10	
CP to Q ↓	0.0674		0.5100	
CP to Q ↑	0.0722		0.7020	
CP to TQ ↓	0.0662		5.7824	
CP to TQ ↑	0.0849		13.0788	
RN to Q ↓	0.1116		0.5820	
RN to Q ↑	0.0785		0.7398	
RN to TQ ↓	0.1053		6.4383	
RN to TQ ↑	0.0995		13.2442	
SN to Q ↑	0.0954		0.7397	
SN to TQ ↑	0.1163		13.2484	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1014	0.1031	0.1014
CP ↑	min_pulse_width to CP	0.0361	0.0420	0.0563
D ↓	hold_rising to CP	-0.0175	-0.0143	-0.0143
D ↑	hold_rising to CP	-0.0071	-0.0071	-0.0071
D ↓	setup_rising to CP	0.0662	0.0662	0.0662
D ↑	setup_rising to CP	0.0368	0.0368	0.0368
RN ↓	min_pulse_width to RN	0.0876	0.1023	0.1289
RN ↑	non_seq_hold_rising to SN	-0.0309	-0.0408	-0.0504
RN ↑	non_seq_setup_rising to SN	0.0621	0.0644	0.0847
RN ↑	recovery_rising to CP	0.0222	0.0222	0.0217
RN ↑	removal_rising to CP	-0.0125	-0.0125	-0.0125
SN ↓	min_pulse_width to SN	0.0674	0.0771	0.0994
SN ↑	recovery_rising to CP	0.0103	0.0103	0.0103
SN ↑	removal_rising to CP	0.0287	0.0287	0.0287

TE ↓	hold_rising to CP	-0.0121	-0.0121	-0.0121
TE ↑	hold_rising to CP	-0.0240	-0.0240	-0.0240
TE ↓	setup_rising to CP	0.0635	0.0635	0.0635
TE ↑	setup_rising to CP	0.1275	0.1275	0.1275
TI ↓	hold_rising to CP	-0.0648	-0.0648	-0.0648
TI ↑	hold_rising to CP	-0.0279	-0.0264	-0.0264
TI ↓	setup_rising to CP	0.1238	0.1238	0.1238
TI ↑	setup_rising to CP	0.0576	0.0576	0.0576

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P10	2.071e-06	1.000e-20
X17_P10	2.431e-06	1.000e-20
X33_P10	3.113e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

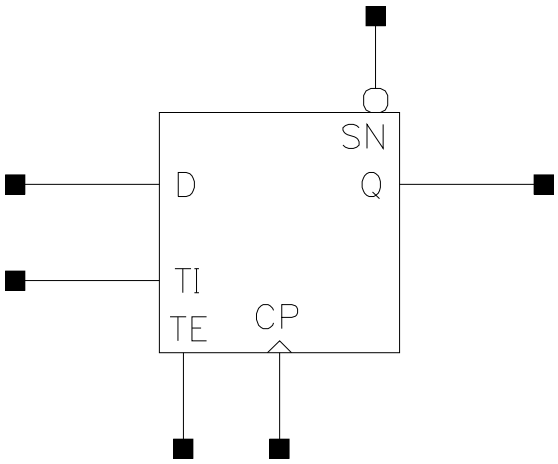
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	9.746e-03	9.747e-03	9.749e-03
Clock 100Mhz Data 25Mhz	9.833e-03	1.029e-02	1.151e-02
Clock 100Mhz Data 50Mhz	9.920e-03	1.083e-02	1.326e-02
Clock = 0 Data 100Mhz	4.893e-03	4.894e-03	4.894e-03
Clock = 1 Data 100Mhz	1.143e-04	1.143e-04	1.145e-04

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005
SN	0.0014	0.0015	0.0014	0.0015
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004
	X33_P10			

CP	0.0010			
D	0.0005			
SN	0.0015			
TE	0.0011			
TI	0.0004			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0738	0.0419	4.0152	1.8067
CP to Q ↑	0.0638	0.0547	5.5555	2.6262
SN to Q ↑	0.0487	0.0553	5.4171	2.6260
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
CP to Q ↓	0.0591	0.0622	0.8826	0.6134
CP to Q ↑	0.0768	0.0793	1.2888	0.8765
SN to Q ↑	0.0767	0.0793	1.2886	0.8750
	X33_P10		**X33_P10**	
CP to Q ↓	0.0646		0.4661	
CP to Q ↑	0.0810		0.6600	
SN to Q ↑	0.0810		0.6594	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.1006	0.1031	0.1031	0.1031
CP ↑	min_pulse_width to CP	0.0611	0.0315	0.0302	0.0302
D ↓	hold_rising to CP	-0.0604	-0.0191	-0.0191	-0.0191
D ↑	hold_rising to CP	-0.0289	-0.0013	-0.0013	-0.0013
D ↓	setup_rising to CP	0.0998	0.0684	0.0684	0.0684
D ↑	setup_rising to CP	0.0584	0.0320	0.0320	0.0320
SN ↓	min_pulse_width to SN	0.0425	0.0522	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0107	0.0107	0.0107	0.0107
SN ↑	removal_rising to CP	0.0212	0.0287	0.0287	0.0287
TE ↓	hold_rising to CP	-0.0431	-0.0169	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0386	-0.0218	-0.0218	-0.0218
TE ↓	setup_rising to CP	0.0852	0.0669	0.0669	0.0669
TE ↑	setup_rising to CP	0.1568	0.1296	0.1296	0.1296
TI ↓	hold_rising to CP	-0.1198	-0.0697	-0.0697	-0.0697
TI ↑	hold_rising to CP	-0.0439	-0.0231	-0.0231	-0.0231
TI ↓	setup_rising to CP	0.1641	0.1238	0.1238	0.1238
TI ↑	setup_rising to CP	0.0737	0.0528	0.0528	0.0528
		X33_P10			

CP ↓	min_pulse_width to CP	0.1031			
CP ↑	min_pulse_width to CP	0.0302			
D ↓	hold_rising to CP	-0.0191			
D ↑	hold_rising to CP	-0.0013			
D ↓	setup_rising to CP	0.0684			
D ↑	setup_rising to CP	0.0320			
SN ↓	min_pulse_width to SN	0.0474			
SN ↑	recovery_rising to CP	0.0107			
SN ↑	removal_rising to CP	0.0287			
TE ↓	hold_rising to CP	-0.0169			
TE ↑	hold_rising to CP	-0.0218			
TE ↓	setup_rising to CP	0.0669			
TE ↑	setup_rising to CP	0.1296			
TI ↓	hold_rising to CP	-0.0697			
TI ↑	hold_rising to CP	-0.0231			
TI ↓	setup_rising to CP	0.1238			
TI ↑	setup_rising to CP	0.0528			

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.550e-06	1.000e-20
X8_P10	1.804e-06	1.000e-20
X17_P10	2.469e-06	1.000e-20
X25_P10	2.737e-06	1.000e-20
X33_P10	3.003e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	8.971e-03	9.171e-03	9.235e-03	9.268e-03
Clock 100Mhz Data 25Mhz	9.097e-03	9.278e-03	1.010e-02	1.053e-02
Clock 100Mhz Data 50Mhz	9.222e-03	9.386e-03	1.097e-02	1.179e-02
Clock = 0 Data 100Mhz	5.299e-03	5.022e-03	4.930e-03	4.885e-03
Clock = 1 Data 100Mhz	1.455e-03	7.522e-04	5.180e-04	4.009e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	9.288e-03			

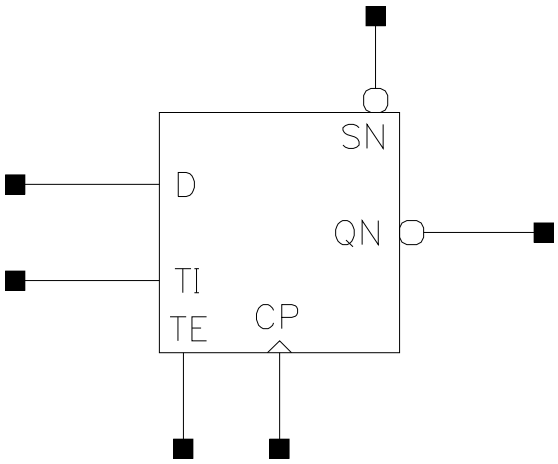
Clock 100Mhz Data 25Mhz	1.089e-02			
Clock 100Mhz Data 50Mhz	1.250e-02			
Clock = 0 Data 100Mhz	4.857e-03			
Clock = 1 Data 100Mhz	3.307e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005
SN	0.0015	0.0015	0.0015	0.0015
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004
	X33_P10			

CP	0.0010			
D	0.0005			
SN	0.0014			
TE	0.0011			
TI	0.0004			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0719	0.0651	3.3019	1.7201
CP to QN ↑	0.0762	0.0481	5.3398	2.5576
SN to QN ↓	0.0578	0.0649	3.2935	1.7181
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
CP to QN ↓	0.0680	0.0717	0.8862	0.6145
CP to QN ↑	0.0564	0.0598	1.2900	0.8776
SN to QN ↓	0.0692	0.0730	0.8854	0.6145
	X33_P10		**X33_P10**	
CP to QN ↓	0.0748		0.4676	
CP to QN ↑	0.0622		0.6607	
SN to QN ↓	0.0760		0.4672	

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.1006	0.1031	0.1031	0.1031
CP ↑	min_pulse_width to CP	0.0456	0.0302	0.0315	0.0361
D ↓	hold_rising to CP	-0.0604	-0.0191	-0.0191	-0.0191
D ↑	hold_rising to CP	-0.0289	-0.0013	-0.0013	-0.0013
D ↓	setup_rising to CP	0.0998	0.0684	0.0684	0.0684
D ↑	setup_rising to CP	0.0584	0.0320	0.0320	0.0320
SN ↓	min_pulse_width to SN	0.0425	0.0474	0.0522	0.0522
SN ↑	recovery_rising to CP	0.0107	0.0107	0.0107	0.0107
SN ↑	removal_rising to CP	0.0212	0.0287	0.0287	0.0287
TE ↓	hold_rising to CP	-0.0431	-0.0169	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0386	-0.0218	-0.0218	-0.0218
TE ↓	setup_rising to CP	0.0852	0.0663	0.0663	0.0663
TE ↑	setup_rising to CP	0.1568	0.1296	0.1296	0.1296
TI ↓	hold_rising to CP	-0.1198	-0.0694	-0.0697	-0.0697
TI ↑	hold_rising to CP	-0.0439	-0.0231	-0.0231	-0.0231
TI ↓	setup_rising to CP	0.1641	0.1238	0.1238	0.1238
TI ↑	setup_rising to CP	0.0737	0.0528	0.0528	0.0528
		X33_P10			

CP ↓	min_pulse_width to CP	0.1031			
CP ↑	min_pulse_width to CP	0.0361			
D ↓	hold_rising to CP	-0.0191			
D ↑	hold_rising to CP	-0.0013			
D ↓	setup_rising to CP	0.0684			
D ↑	setup_rising to CP	0.0320			
SN ↓	min_pulse_width to SN	0.0522			
SN ↑	recovery_rising to CP	0.0107			
SN ↑	removal_rising to CP	0.0287			
TE ↓	hold_rising to CP	-0.0169			
TE ↑	hold_rising to CP	-0.0218			
TE ↓	setup_rising to CP	0.0663			
TE ↑	setup_rising to CP	0.1296			
TI ↓	hold_rising to CP	-0.0697			
TI ↑	hold_rising to CP	-0.0231			
TI ↓	setup_rising to CP	0.1238			
TI ↑	setup_rising to CP	0.0528			

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.553e-06	1.000e-20
X8_P10	1.862e-06	1.000e-20
X17_P10	2.543e-06	1.000e-20
X25_P10	2.897e-06	1.000e-20
X33_P10	3.253e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	8.965e-03	9.120e-03	9.163e-03	9.185e-03
Clock 100Mhz Data 25Mhz	8.985e-03	9.209e-03	1.005e-02	1.048e-02
Clock 100Mhz Data 50Mhz	9.005e-03	9.298e-03	1.093e-02	1.177e-02
Clock = 0 Data 100Mhz	5.299e-03	5.026e-03	4.932e-03	4.886e-03
Clock = 1 Data 100Mhz	1.455e-03	7.725e-04	5.449e-04	4.312e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	9.198e-03			

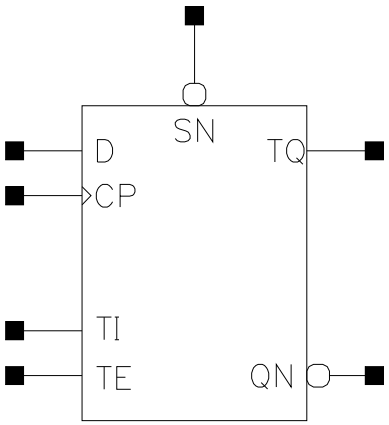
Clock 100Mhz Data 25Mhz	1.086e-02			
Clock 100Mhz Data 50Mhz	1.253e-02			
Clock = 0 Data 100Mhz	4.858e-03			
Clock = 1 Data 100Mhz	3.630e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.216	5.0592
X8_P10	1.200	4.080	4.8960
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005

SN	0.0016	0.0017	0.0017	0.0017
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0825	0.0682	3.2990	1.7287
CP to QN ↑	0.0982	0.0541	5.2576	2.6123
CP to TQ ↓	0.0709	0.0375	4.7542	4.0096
CP to TQ ↑	0.0634	0.0517	7.3659	7.1521
SN to QN ↓	0.0553	0.0526	3.2938	1.7287
SN to TQ ↑	0.0387	0.0376	7.2310	7.1255
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0682	0.0750	0.9105	0.4622
CP to QN ↑	0.0607	0.0669	1.3031	0.6655
CP to TQ ↓	0.0459	0.0458	4.1649	4.1658
CP to TQ ↑	0.0578	0.0579	7.2423	7.2588
SN to QN ↓	0.0586	0.0653	0.9103	0.4618
SN to TQ ↑	0.0479	0.0479	7.2303	7.2520

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1006	0.1031	0.1031	0.1031
CP ↑	min_pulse_width to CP	0.0652	0.0315	0.0361	0.0408
D ↓	hold_rising to CP	-0.0604	-0.0191	-0.0191	-0.0191
D ↑	hold_rising to CP	-0.0289	-0.0013	-0.0013	-0.0013
D ↓	setup_rising to CP	0.0998	0.0684	0.0684	0.0684
D ↑	setup_rising to CP	0.0584	0.0320	0.0320	0.0320
SN ↓	min_pulse_width to SN	0.0376	0.0425	0.0425	0.0452
SN ↑	recovery_rising to CP	0.0107	0.0086	0.0112	0.0112
SN ↑	removal_rising to CP	0.0212	0.0287	0.0287	0.0287
TE ↓	hold_rising to CP	-0.0431	-0.0169	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0386	-0.0218	-0.0218	-0.0218
TE ↓	setup_rising to CP	0.0852	0.0663	0.0663	0.0663
TE ↑	setup_rising to CP	0.1568	0.1296	0.1296	0.1296
TI ↓	hold_rising to CP	-0.1198	-0.0697	-0.0697	-0.0697
TI ↑	hold_rising to CP	-0.0439	-0.0231	-0.0231	-0.0231
TI ↓	setup_rising to CP	0.1641	0.1238	0.1235	0.1235
TI ↑	setup_rising to CP	0.0737	0.0528	0.0528	0.0528

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.736e-06	1.000e-20
X8_P10	2.040e-06	1.000e-20
X17_P10	2.721e-06	1.000e-20
X33_P10	3.431e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

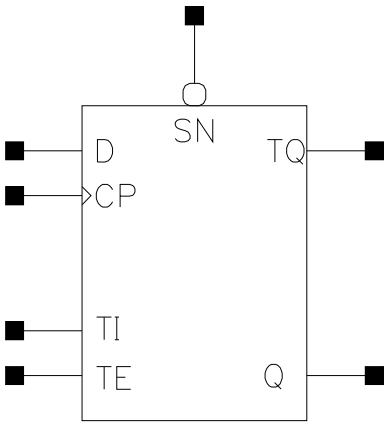
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	8.975e-03	9.224e-03	9.309e-03	9.351e-03
Clock 100Mhz Data 25Mhz	9.340e-03	9.531e-03	1.032e-02	1.113e-02
Clock 100Mhz Data 50Mhz	9.706e-03	9.838e-03	1.134e-02	1.291e-02
Clock = 0 Data 100Mhz	5.310e-03	5.032e-03	4.940e-03	4.894e-03
Clock = 1 Data 100Mhz	1.456e-03	7.541e-04	5.202e-04	4.034e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.944	4.7328
X17_P10	1.200	4.216	5.0592
X33_P10	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0005	0.0005	0.0005

SN	0.0016	0.0014	0.0015	0.0015
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0844	0.0450	4.1173	1.8476
CP to Q ↑	0.0679	0.0568	5.5913	2.6647
CP to TQ ↓	0.0837	0.0462	5.9247	4.5420
CP to TQ ↑	0.0669	0.0624	7.4263	10.2240
SN to Q ↑	0.0414	0.0578	5.4225	2.6635
SN to TQ ↑	0.0406	0.0642	7.2519	10.2032
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0607	0.0660	0.9071	0.4745
CP to Q ↑	0.0781	0.0821	1.2957	0.6627
CP to TQ ↓	0.0630	0.0700	4.3658	4.4309
CP to TQ ↑	0.0830	0.0898	10.0471	10.1014
SN to Q ↑	0.0780	0.0820	1.2937	0.6619
SN to TQ ↑	0.0830	0.0898	10.0441	10.1023

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1006	0.1031	0.1031	0.1031
CP ↑	min_pulse_width to CP	0.0740	0.0362	0.0302	0.0302
D ↓	hold_rising to CP	-0.0604	-0.0191	-0.0191	-0.0191
D ↑	hold_rising to CP	-0.0289	-0.0013	-0.0013	-0.0013
D ↓	setup_rising to CP	0.0998	0.0684	0.0684	0.0684
D ↑	setup_rising to CP	0.0584	0.0320	0.0320	0.0320
SN ↓	min_pulse_width to SN	0.0376	0.0549	0.0474	0.0474
SN ↑	recovery_rising to CP	0.0107	0.0107	0.0107	0.0107
SN ↑	removal_rising to CP	0.0212	0.0287	0.0287	0.0287
TE ↓	hold_rising to CP	-0.0431	-0.0169	-0.0169	-0.0169
TE ↑	hold_rising to CP	-0.0386	-0.0218	-0.0218	-0.0218
TE ↓	setup_rising to CP	0.0852	0.0669	0.0663	0.0669
TE ↑	setup_rising to CP	0.1568	0.1296	0.1296	0.1296
TI ↓	hold_rising to CP	-0.1198	-0.0697	-0.0697	-0.0697
TI ↑	hold_rising to CP	-0.0439	-0.0231	-0.0231	-0.0231
TI ↓	setup_rising to CP	0.1641	0.1238	0.1238	0.1238
TI ↑	setup_rising to CP	0.0737	0.0528	0.0528	0.0528

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.690e-06	1.000e-20
X8_P10	1.875e-06	1.000e-20
X17_P10	2.529e-06	1.000e-20
X33_P10	3.063e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

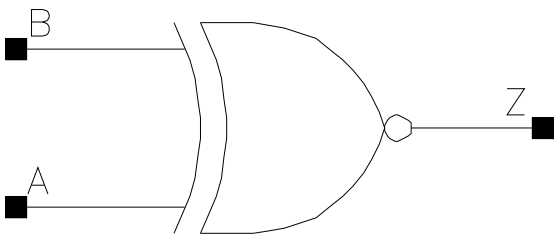
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	8.973e-03	9.219e-03	9.300e-03	9.340e-03
Clock 100Mhz Data 25Mhz	9.328e-03	9.507e-03	1.037e-02	1.119e-02
Clock 100Mhz Data 50Mhz	9.683e-03	9.794e-03	1.144e-02	1.304e-02
Clock = 0 Data 100Mhz	5.310e-03	5.028e-03	4.934e-03	4.887e-03
Clock = 1 Data 100Mhz	1.456e-03	7.540e-04	5.202e-04	4.033e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P10	X8_P10	X17_P10	X25_P10
A	0.0018	0.0007	0.0010	0.0016
B	0.0016	0.0015	0.0019	0.0027
	X33_P10			
A	0.0018			
B	0.0031			

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X8_P10**	**X6_P10**	**X8_P10**
A to Z ↓	0.0204	0.0450	3.2137	1.8632
A to Z ↑	0.0210	0.0405	4.0435	2.7147
B to Z ↓	0.0191	0.0313	3.2126	1.8504
B to Z ↑	0.0214	0.0294	4.0549	2.7036
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
A to Z ↓	0.0428	0.0433	0.9173	0.6328
A to Z ↑	0.0374	0.0378	1.3305	0.8846

B to Z ↓	0.0325	0.0316	0.9153	0.6316
B to Z ↑	0.0296	0.0288	1.3273	0.8825
	X33_P10		**X33_P10**	
A to Z ↓	0.0411		0.4751	
A to Z ↑	0.0368		0.6657	
B to Z ↓	0.0305		0.4740	
B to Z ↑	0.0286		0.6643	

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X6_P10	1.011e-06	1.000e-20
X8_P10	1.080e-06	1.000e-20
X17_P10	1.895e-06	1.000e-20
X25_P10	2.888e-06	1.000e-20
X33_P10	4.067e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	2.834e-03	5.232e-03	7.539e-03	1.206e-02
B to Z	2.706e-03	3.645e-03	5.736e-03	8.989e-03
	X33_P10			
A to Z	1.478e-02			
B to Z	1.140e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

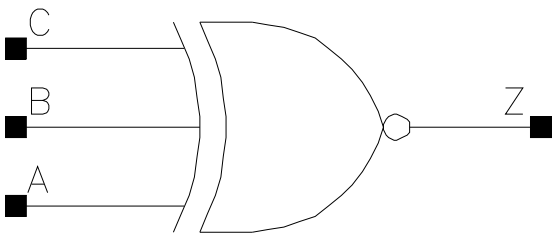
Pin Cycle (vdds)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P10			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	2.176	2.6112
X16_P10	1.200	2.720	3.2640
X25_P10	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X16_P10	X25_P10
A	0.0030	0.0025	0.0032	0.0046
B	0.0033	0.0023	0.0031	0.0042
C	0.0021	0.0007	0.0007	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0317	0.0520	3.7994	1.9747
A to Z ↑	0.0300	0.0478	5.7301	2.6838
B to Z ↓	0.0324	0.0520	3.8018	1.9747
B to Z ↑	0.0303	0.0481	5.7271	2.6843
C to Z ↓	0.0319	0.0687	3.8061	1.9739
C to Z ↑	0.0293	0.0640	5.7205	2.6831
	X16_P10	**X25_P10**	**X16_P10**	**X25_P10**
A to Z ↓	0.0522	0.0524	1.0137	0.6483
A to Z ↑	0.0516	0.0512	1.4111	0.8878
B to Z ↓	0.0524	0.0531	1.0134	0.6484

B to Z ↑	0.0519	0.0523	1.4117	0.8879
C to Z ↓	0.0727	0.0775	1.0131	0.6483
C to Z ↑	0.0712	0.0758	1.4118	0.8879

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.107e-06	1.000e-20
X8_P10	1.065e-06	1.000e-20
X16_P10	1.845e-06	1.000e-20
X25_P10	2.659e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	3.124e-03	4.162e-03	6.769e-03	1.023e-02
B to Z	2.941e-03	4.060e-03	6.660e-03	1.009e-02
C to Z	2.848e-03	6.229e-03	9.293e-03	1.400e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

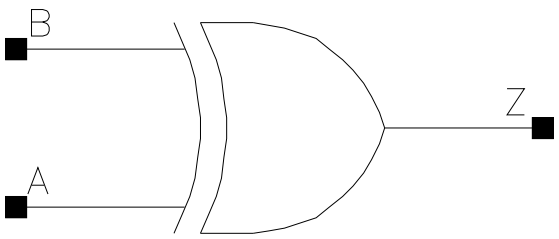
Pin Cycle (vdds)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.224	1.4688
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.224	1.4688
X16_P10	1.200	1.360	1.6320
X25_P10	1.200	2.176	2.6112
X31_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X16_P10
A	0.0008	0.0017	0.0011	0.0012
B	0.0013	0.0015	0.0016	0.0018
	X25_P10	X31_P10		
A	0.0016	0.0021		
B	0.0028	0.0036		

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0403	0.0202	3.3540	2.4776
A to Z ↑	0.0380	0.0218	5.2280	5.0884
B to Z ↓	0.0290	0.0206	3.3368	2.4964
B to Z ↑	0.0290	0.0203	5.2247	5.0893
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0365	0.0379	1.8232	0.9436

A to Z ↑	0.0331	0.0348	2.6341	1.3317
B to Z ↓	0.0283	0.0293	1.8174	0.9410
B to Z ↑	0.0268	0.0283	2.6318	1.3301
	X25_P10	**X31_P10**	**X25_P10**	**X31_P10**
A to Z ↓	0.0404	0.0381	0.6283	0.5043
A to Z ↑	0.0368	0.0352	0.8833	0.7153
B to Z ↓	0.0307	0.0288	0.6274	0.5039
B to Z ↑	0.0281	0.0270	0.8825	0.7147

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	8.452e-07	1.000e-20
X6_P10	9.586e-07	1.000e-20
X8_P10	1.409e-06	1.000e-20
X16_P10	2.192e-06	1.000e-20
X25_P10	2.880e-06	1.000e-20
X31_P10	4.056e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	3.944e-03	2.820e-03	4.824e-03	6.989e-03
B to Z	3.041e-03	2.631e-03	3.967e-03	5.813e-03
	X25_P10	X31_P10		
A to Z	1.100e-02	1.355e-02		
B to Z	7.949e-03	9.780e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

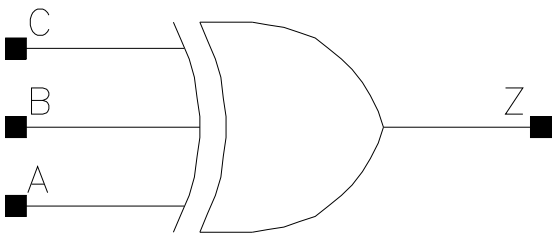
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P10	X31_P10		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X24_P10	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X24_P10
A	0.0026	0.0025	0.0032	0.0056
B	0.0026	0.0023	0.0029	0.0046
C	0.0008	0.0017	0.0024	0.0036

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0320	0.0520	4.0017	1.9739
A to Z ↑	0.0303	0.0478	6.2864	2.6806
B to Z ↓	0.0324	0.0522	4.0048	1.9740
B to Z ↑	0.0304	0.0481	6.2834	2.6817
C to Z ↓	0.0546	0.0509	3.9793	1.9750
C to Z ↑	0.0530	0.0467	6.2586	2.6818
	X17_P10	**X24_P10**	**X17_P10**	**X24_P10**
A to Z ↓	0.0479	0.0557	0.9442	0.6797
A to Z ↑	0.0476	0.0429	1.3071	0.8904
B to Z ↓	0.0481	0.0560	0.9440	0.6790

B to Z ↑	0.0478	0.0431	1.3070	0.8910
C to Z ↓	0.0474	0.0544	0.9440	0.6789
C to Z ↑	0.0472	0.0427	1.3070	0.8913

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P10	1.183e-06	1.000e-20
X8_P10	9.155e-07	1.000e-20
X17_P10	1.774e-06	1.000e-20
X24_P10	2.814e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	2.886e-03	4.182e-03	6.557e-03	1.120e-02
B to Z	2.815e-03	4.048e-03	6.390e-03	1.084e-02
C to Z	5.731e-03	3.931e-03	6.305e-03	1.060e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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