



HDL MODELS

MODEL USAGE GUIDELINES

MAY 2014

Version 1.0



Highlights

- Defines Model Usage Guidelines with compiler directives

UNICAD™ is a trademark of STMicroelectronics.

The following names are trademarks, registered trademarks, and service marks of other companies that appear in Unicad publications:

Adobe, the Adobe logo, FrameMaker, the Frame Maker logo, Acrobat, the Acrobat logo, Exchange, and PostScript are registered trademarks of Adobe Systems Incorporated.

ADS, AHB, AMBA, PrimeXsys, STD are trademarks of ARM, Ltd.

Alanza, Allegro, Ambit, Analog Artist, Assura, BuildGates, Cadence, Cadence Logo, CoBALT, Composer, Concept, Connection, Diva, Dracula, Envisia, Formal Check, Gate Ensemble, GDSII, HDL_ICE, MegaSim, Mercury, NC Verilog, Orcad, Orcad Capture, Orcad Layout, Palladium, Pearl, PowerSuite, PSpice, Q/Bridge, QPlace, Quest, Quickturn, Radium, Transaction Explorer, Test Builder, Verification Cockpit Vampire, Verilog, Verilog XL, Verifault, Verifault XL, NC-Verilog, Cell3 Ensemble, Silicon Ensemble, Virtuoso, Spectre, and Leapfrog are trademarks and registered trademarks of Cadence Design Systems, Inc. MemMaker, PureView, PureData are trademarks of Denali, Software Inc.

ApolloII, ApolloGAII, Apollo-DPII, Aurora, ASIC Synthesizer, AvanTestchip, AvanWaves, ChipPlanner, Columbia, Columbia-CE, Cyclelink, Davinci, DFM Workbench, Driveline, Dynamic Model Switcher, Electrically Aware, Enterprise, Evaccess, Hercules, Hercules-Explorer, HotPlace, HSPICE, HSPICE-LINK, Jupiter, LTL, Libra-Passport, Lynx, Lynx-LB, Lynx- VHDL, Mars, Mars-Rail, Mars-Xtalk, MASTER Toolbox, Medici, Michelangelo, Milkyway, Optimum Silicon, Passport, Pathfinder, Planet, Planet-PL, Planet-RTL, Polaris, Polaris-CBS, Polaris-MT, Progen, Prospector, Raphael, Raphael-NES, Saturn, Sirius, Silicon Blueprint, Smart Extraction, Solar, Solar II, Star, Star-Sim, Star-Hspice, Star-HspiceLink, Star-DC, Star- RC, Star-RCXT, Star-Power, Star-Time, Star-MTB, Star-XP, Taurus, Taurus-Device, Taurus-Layout, Taurus-Lithography, Taurus-OPC, Taurus-Process, Taurus-Topography, Taurus-Visual, Taurus- Workbench, TimeSlice, and TSUPREM-4 are trademarks of Avant! Corporation. Avant!, Avant! logo, AvanLabs, and avanticorp are trademarks and servicemarks of Avant! Corporation.

ASAP, Aspire, C-FAS, CMPI, Eldo-FAS, EldoHDL, Eldo-Opt, Eldo-UDM, EldoVHDL, Eldo-XL, Elga, Elib, Elib-Plus, ESim, Fidel, Fideldo, GENIE, GENLIB, HDLA, MDT, MGS-MEMT, MixVHDL, Model Generator Series (MGS), Opsim, SimLink, SimPilot, SpecEditor, Success, SystemEldo, VHDeLDO and Xelga are registered trademarks of ANACAD

Eldo, Calibre, ModelSim, FastScan, DFTAdvisor, Seamless, CVE, XRAY are registered trademarks of Mentor Graphics Corporation.

Debussy is a trademark of Novas Software, Inc.

DesignSync,

DesignSync DFII, ProjectSync, IPGear are registered trademarks of Synchronicity Software, Inc.

FLEXIm is a trademark of Globetrotter Software, Inc.

HSPICE is a registered trademark of Meta-Software, Inc.

IKOS and Voyager are registered trademarks of IKOS Systems, Inc.

Java and all Java-based trademarks and logos are trademarks or registered trademarks of Sun Microsystems, Inc.

NeoCell, NeoCircuit are registered trademarks of Neolinear, Inc.

Netscape is a trademark of Netscape Communications Corporation.

SPARC is a registered trademark, and SPARCstation is a trademark, of SPARC International, Inc. Sun Microsystems, Sun Workstation, and NeWS are registered trademarks of Sun Microsystems, Inc.

Sun, Sun-2, Sun-3, Sun-4, OpenWindows, SunOS, SunView, NFS, and NSE are trademarks of Sun Microsystems, Inc.

Synopsys, Design Compiler, Physical Compiler, DFT Compiler, Test Compiler, Power Compiler, Module Compiler, Library Compiler, PrimeTime, Formality, Arcadia, Liberty, TetraMAX, LEDA, PathMill, PowerMill, TimeMill, Chip Architect and VSS are trademarks or registered trademarks of Synopsys, Inc.

UNIX, Solaris and OPEN LOOK are registered trademarks of UNIX System Laboratories, Inc.

Verisity is a trademark of Verisity Ltd. or its subsidiaries (Verisity), registered in the United States and other jurisdictions. The Verisity logo, Specman, Specview, Specman Elite, Verification Advisor, eVC, Pure IP, InvisibleSpecman, SureLint, Lintprt, SureCov, and SureSight are trademarks of Verisity.

Versatec is a trademark of Xerox Engineering Systems, Inc.

Fire & Ice is a registered trademark, and Clock-Storm, ElectronStorm, VoltageStorm, SubstrateStorm, IceCaps, Rain, SI Report, QIC Engine, 3D Adaptive Analytical Extraction, Accura, PGS Exploration, PerturbingPath, NetConnect, and SoC Design Foundry are trademarks of Simplex Solutions, Inc. TransEDA, VeriSure, VHDLcover, HDLcover, CoverPlus, StateSure, Verification Navigator, State Navigator, TransEDA Verification Navigator and TransEDA State Navigator are trademarks of TransEDA Limited.

Other brand or product names that appear in Unicad publications are trademarks or registered trademarks of their respective holders.

Revision History

Date	Document Version	Comment
15-May-2014	1.0	First release



This page is intentionally left blank.



Table of Contents

1 General Description	1
2 Known Problems and Solutions (KPS)	1
3. Contact Information	3



This page is intentionally left blank.



1. General Description

In model, certain compiler directives / switches are defined to enable the user to perform faster simulations in digital domain. These switches, however, do not reflect the real design behavior. The users should use them at their own discretion.

2. Known Problems and Solutions (KPS)

2.1 Verilog Model Usage

2.1.1 Debug Level Usage

The display of messages is controlled by three methods. This is applicable to every compiled verilog module.

This can be achieved in three ways –

2.1.1.1 Message Control through compiler directive

The display of messages is controlled by providing a compiler directive from the command line during compilation:

+define+ST_NO_MSG_MODE to get no messages from the model.

+define+ST_ERROR_ONLY_MODE to get only ERROR messages from the model

+define+ST_ALL_MSG_MODE to get all messages i.e. ERROR + WARNING + INFO from the model.

By default, the model is set as to display ERROR + WARNING messages from the model.

2.1.1.2 Message Control by overriding a parameter (defparam)

The display of messages is controlled by overriding a parameter p_debug_level in the test bench to values 0, 1, 2, and 3 using the following method:

defparam <instance_name>.p_debug_level = <value>

2.1.1.3 Message Control by updating a model internal register

The display of messages can also be controlled by updating a model internal register to a certain value from the test environment:

<instance_name>.debug_level = <value>

The value to be overridden has the following definitions

2'b00: to get no messages from the model.

2'b01: to get only ERROR messages from the model.

2'b10: to get only ERROR + WARNING messages from the model.

2'b11: to get all messages (ERROR + WARNING +INFO) from the model.

By default, the debug_level in the model is set as 2'b10.

2.1.2 Message Display Control

There is another method for the controlling the display of messages, which is achieved by overriding a parameter available in the model, the same can be achieved by adapting any of the two methods mentioned below :



Compiler Directive**+define+ST_MSG_CONTROL_TIME=<desired_value in ns>****defparam****defparam <instance_name>.message_control_time = <desired_value in ns>**

It is to be understood that this features 'only' enables the display of messages from the desired time, whereas the output behavior remains intact.

2.1.3 Timescale

The time scale used in the model is 1 ns / 1 ps. The timescale of the model can be changed by providing a compiler directive from the command line during compilation in the following way

+define+ST_TIMESCALE='\timescale <time_scale>/<precision>' for single invoke commands**-define ST_TIMESCALE='\timescale\ <time_scale>V<precision> for multi command invoke**

The model is qualified on 1ns / 1ps, if the time scale is changed the model may behave incorrectly. This provision is given exclusively to improve the simulation time and doesn't reflect the design behavior. The user needs to use this feature with extreme caution.

2.1.4 Delay Mode Control

The model is developed and validated on 'delay_mode_path, where as in the model there is a provision to make the model work without a delay mode. The same can be achieved by providing a compiler directive from the command line during simulation:

+define+ST_NODELAYMODE

The model is qualified on 'delay_mode_path. The user needs to use this feature with extreme caution



3. Contact Information

For more information about this document, please write to [HELPDESK](#).

