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C28SOI_SC_8_CORE_LL Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells

Overview

- C28SOI_SC_8_CORE_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

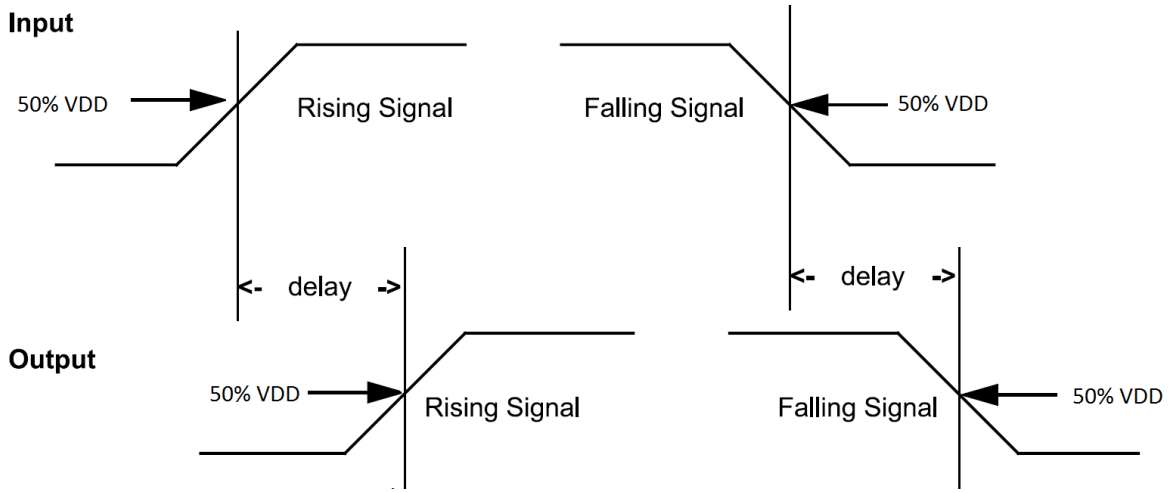


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

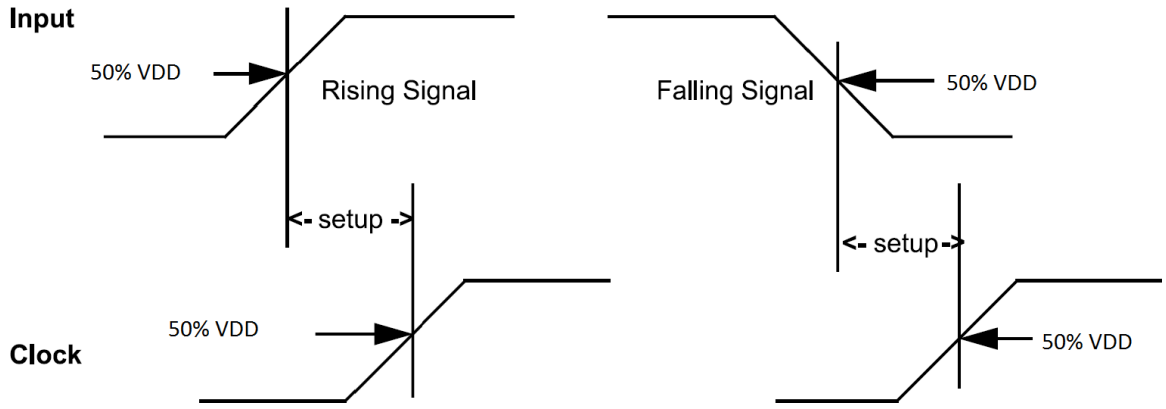


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

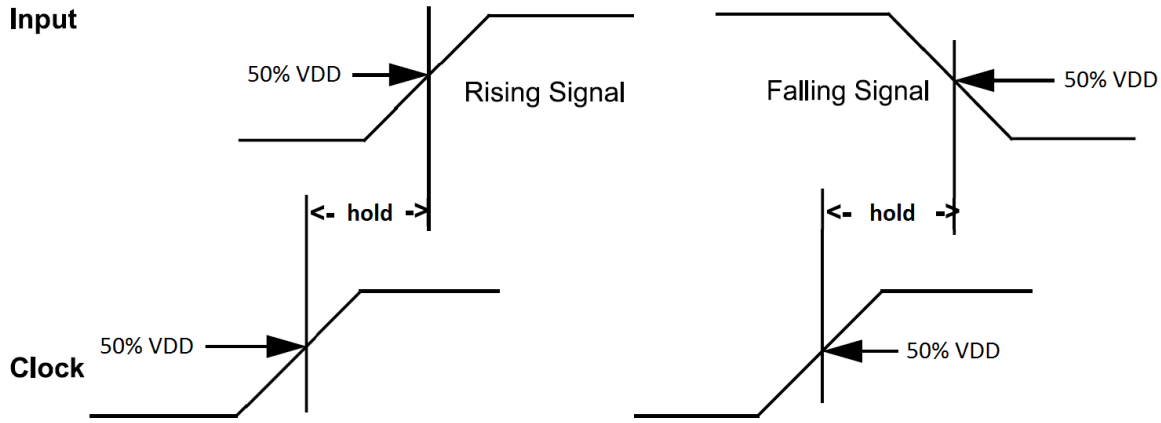


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

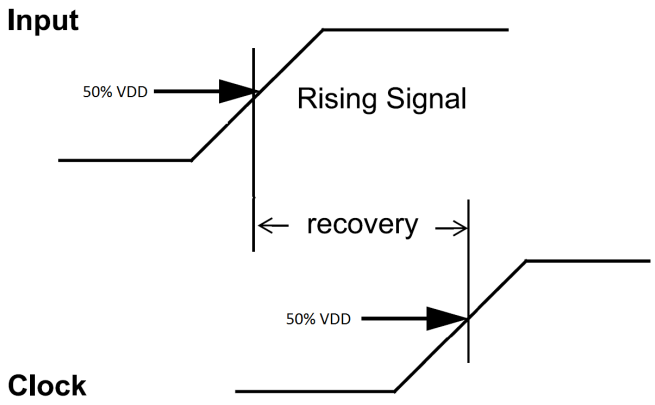


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

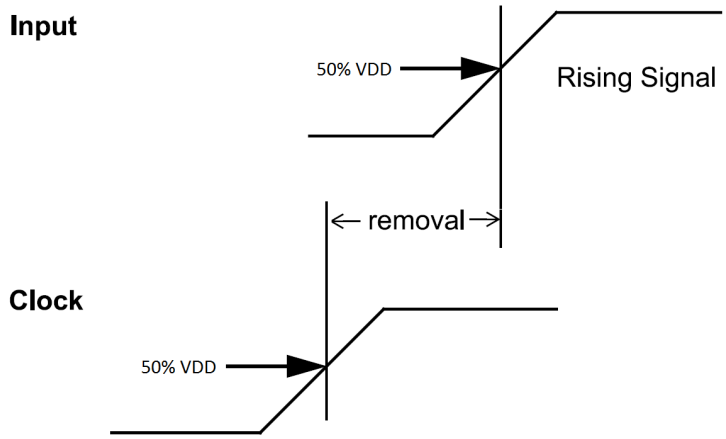


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

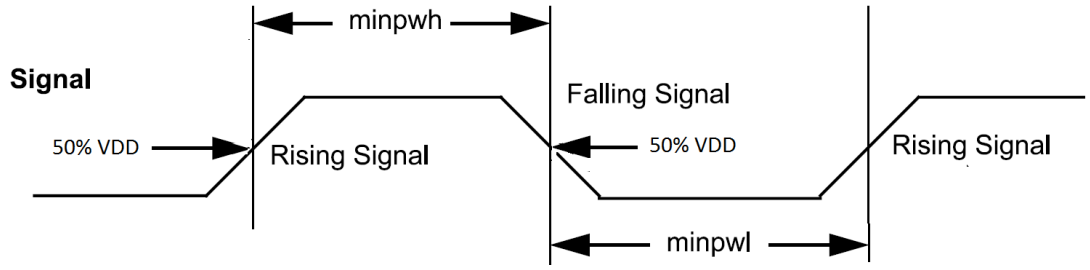


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

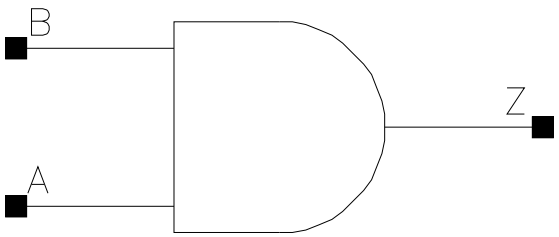
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.544	0.4352
X10_P0	0.800	0.680	0.5440
X11_P0	1.600	0.544	0.8704
X19_P0	0.800	1.224	0.9792
X24_P0	0.800	1.360	1.0880
X29_P0	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X11_P0	X19_P0
A	0.0005	0.0007	0.0009	0.0014
B	0.0004	0.0007	0.0009	0.0012
	X24_P0	X29_P0		
A	0.0014	0.0014		
B	0.0012	0.0012		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0184	0.0151	2.5411	1.2153
A to Z ↑	0.0144	0.0144	3.1612	1.5223
B to Z ↓	0.0174	0.0140	2.5435	1.2146
B to Z ↑	0.0163	0.0161	3.1517	1.5217
	X11_P0	**X19_P0**	**X11_P0**	**X19_P0**

A to Z ↓	0.0169	0.0149	0.9701	0.6242
A to Z ↑	0.0126	0.0142	1.4430	0.7661
B to Z ↓	0.0157	0.0143	0.9678	0.6239
B to Z ↑	0.0143	0.0160	1.4426	0.7647
	X24_P0	**X29_P0**	**X24_P0**	**X29_P0**
A to Z ↓	0.0162	0.0172	0.5073	0.4222
A to Z ↑	0.0157	0.0169	0.6143	0.5095
B to Z ↓	0.0157	0.0168	0.5071	0.4221
B to Z ↑	0.0175	0.0188	0.6145	0.5094

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	3.302e-04	1.000e-20
X10_P0	7.719e-04	1.000e-20
X11_P0	8.258e-04	1.000e-20
X19_P0	1.472e-03	1.000e-20
X24_P0	1.721e-03	1.000e-20
X29_P0	1.969e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X11_P0	X19_P0
A (output stable)	1.136e-05	2.136e-05	2.868e-05	4.273e-05
B (output stable)	1.950e-05	3.418e-05	4.736e-05	6.654e-05
A to Z	2.743e-03	4.998e-03	5.733e-03	9.952e-03
B to Z	2.671e-03	4.896e-03	5.539e-03	9.655e-03
	X24_P0	X29_P0		
A (output stable)	4.054e-05	4.300e-05		
B (output stable)	6.755e-05	6.964e-05		
A to Z	1.200e-02	1.421e-02		
B to Z	1.176e-02	1.402e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

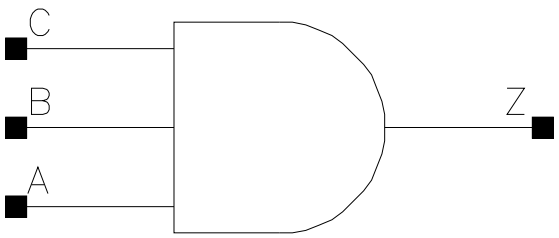
Pin Cycle (vdds)	X5_P0	X10_P0	X11_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P0	X29_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.680	0.5440
X10_P0	0.800	0.816	0.6528
X14_P0	0.800	1.360	1.0880
X19_P0	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0005	0.0007	0.0012	0.0014
B	0.0004	0.0006	0.0010	0.0013
C	0.0005	0.0007	0.0009	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0202	0.0165	2.5656	1.2211
A to Z ↑	0.0192	0.0187	3.1979	1.5431
B to Z ↓	0.0196	0.0157	2.5661	1.2216
B to Z ↑	0.0210	0.0202	3.1985	1.5434
C to Z ↓	0.0187	0.0148	2.5661	1.2197
C to Z ↑	0.0224	0.0213	3.1909	1.5429
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0169	0.0160	0.8425	0.6264

A to Z ↑	0.0178	0.0178	1.0486	0.7744
B to Z ↓	0.0159	0.0151	0.8427	0.6257
B to Z ↑	0.0194	0.0194	1.0477	0.7729
C to Z ↓	0.0151	0.0142	0.8414	0.6257
C to Z ↑	0.0207	0.0206	1.0470	0.7734

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	3.356e-04	1.000e-20
X10_P0	7.771e-04	1.000e-20
X14_P0	1.094e-03	1.000e-20
X19_P0	1.493e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	1.308e-05	2.442e-05	3.350e-05	4.464e-05
B (output stable)	1.955e-05	3.452e-05	4.901e-05	6.624e-05
C (output stable)	3.535e-05	6.464e-05	9.353e-05	1.343e-04
A to Z	3.117e-03	5.618e-03	8.314e-03	1.101e-02
B to Z	3.026e-03	5.466e-03	8.028e-03	1.064e-02
C to Z	2.962e-03	5.347e-03	7.846e-03	1.034e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

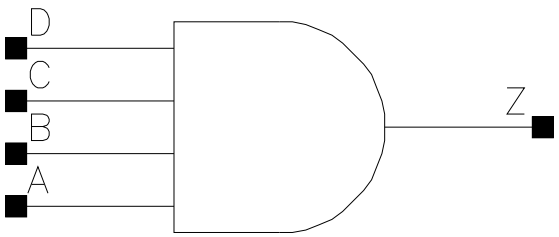
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.088	0.8704
X3_P0	0.800	1.088	0.8704
X10_P0	0.800	2.176	1.7408
X13_P0	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P0	X3_P0	X10_P0	X13_P0
A	0.0005	0.0005	0.0011	0.0012
B	0.0005	0.0005	0.0011	0.0012
C	0.0004	0.0004	0.0010	0.0012
D	0.0005	0.0005	0.0010	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	X3_P0	X2_P0	X3_P0
A to Z ↓	0.0159	0.0173	4.5662	3.0824
A to Z ↑	0.0161	0.0162	10.5282	5.8325
B to Z ↓	0.0148	0.0164	4.5643	3.0816
B to Z ↑	0.0177	0.0180	10.5320	5.8291
C to Z ↓	0.0164	0.0179	4.5707	3.0667
C to Z ↑	0.0167	0.0168	10.5349	5.8362

D to Z ↓	0.0153	0.0172	4.5638	3.0670
D to Z ↑	0.0185	0.0192	10.5283	5.8301
	X10_P0	**X13_P0**	**X10_P0**	**X13_P0**
A to Z ↓	0.0166	0.0166	1.0538	0.7873
A to Z ↑	0.0156	0.0174	1.9627	1.5059
B to Z ↓	0.0157	0.0150	1.0540	0.7864
B to Z ↑	0.0173	0.0187	1.9630	1.5045
C to Z ↓	0.0165	0.0159	1.0483	0.7875
C to Z ↑	0.0158	0.0159	1.9598	1.5006
D to Z ↓	0.0149	0.0144	1.0460	0.7858
D to Z ↑	0.0170	0.0172	1.9567	1.4995

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P0	2.492e-04	1.000e-20
X3_P0	3.412e-04	1.000e-20
X10_P0	1.065e-03	1.000e-20
X13_P0	1.455e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P0	X3_P0	X10_P0	X13_P0
A (output stable)	6.074e-04	6.790e-04	1.811e-03	2.371e-03
B (output stable)	5.722e-04	6.363e-04	1.701e-03	2.248e-03
C (output stable)	6.172e-04	6.546e-04	1.705e-03	2.168e-03
D (output stable)	5.787e-04	6.223e-04	1.611e-03	2.043e-03
A to Z	2.075e-03	2.673e-03	7.552e-03	1.014e-02
B to Z	1.993e-03	2.582e-03	7.307e-03	9.663e-03
C to Z	2.142e-03	2.733e-03	7.113e-03	9.133e-03
D to Z	2.046e-03	2.662e-03	6.736e-03	8.672e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

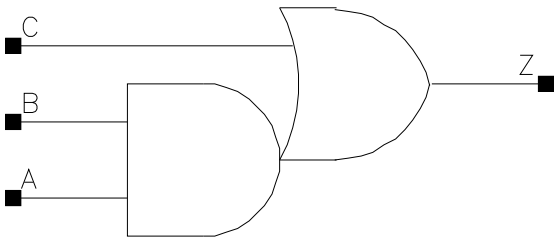
Pin Cycle (vdds)	X2_P0	X3_P0	X10_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	0.952	0.7616
X19_P0	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0004	0.0006	0.0012
B	0.0004	0.0006	0.0011
C	0.0005	0.0007	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0252	0.0229	2.4294	1.2190
A to Z ↑	0.0161	0.0153	2.9215	1.4941
B to Z ↓	0.0236	0.0213	2.4231	1.2169
B to Z ↑	0.0182	0.0173	2.9156	1.4932
C to Z ↓	0.0237	0.0209	2.4224	1.2167
C to Z ↑	0.0157	0.0148	2.8948	1.4838
	X19_P0		**X19_P0**	
A to Z ↓	0.0218		0.6342	
A to Z ↑	0.0171		0.7558	

B to Z ↓	0.0211		0.6338	
B to Z ↑	0.0191		0.7558	
C to Z ↓	0.0203		0.6334	
C to Z ↑	0.0162		0.7483	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	3.037e-04	1.000e-20
X10_P0	6.204e-04	1.000e-20
X19_P0	1.166e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	3.971e-05	5.103e-05	1.137e-04
B (output stable)	4.118e-05	5.926e-05	1.241e-04
C (output stable)	5.453e-05	7.932e-05	1.802e-04
A to Z	3.202e-03	5.661e-03	1.095e-02
B to Z	3.112e-03	5.505e-03	1.079e-02
C to Z	3.328e-03	5.778e-03	1.121e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

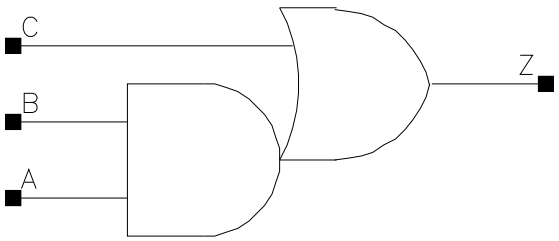
Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	0.952	0.7616
X14_P0	0.800	1.632	1.3056
X19_P0	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0006	0.0012	0.0012
B	0.0005	0.0006	0.0012	0.0013
C	0.0005	0.0007	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0242	0.0216	2.4232	1.2244
A to Z ↑	0.0179	0.0171	2.9891	1.5129
B to Z ↓	0.0230	0.0205	2.4200	1.2247
B to Z ↑	0.0203	0.0190	2.9830	1.5131
C to Z ↓	0.0232	0.0215	2.4129	1.2206
C to Z ↑	0.0133	0.0124	2.9514	1.4983
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0197	0.0212	0.8420	0.6308

A to Z ↑	0.0156	0.0168	1.0308	0.7679
B to Z ↓	0.0177	0.0194	0.8388	0.6284
B to Z ↑	0.0172	0.0185	1.0294	0.7673
C to Z ↓	0.0184	0.0201	0.8375	0.6273
C to Z ↑	0.0107	0.0118	1.0192	0.7573

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	3.058e-04	1.000e-20
X10_P0	6.048e-04	1.000e-20
X14_P0	1.069e-03	1.000e-20
X19_P0	1.228e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	1.545e-05	2.053e-05	6.500e-05	6.533e-05
B (output stable)	1.842e-05	2.480e-05	9.976e-05	1.001e-04
C (output stable)	1.504e-04	1.658e-04	4.849e-04	4.884e-04
A to Z	3.384e-03	5.658e-03	9.361e-03	1.154e-02
B to Z	3.297e-03	5.546e-03	8.887e-03	1.109e-02
C to Z	3.008e-03	5.129e-03	8.277e-03	1.021e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

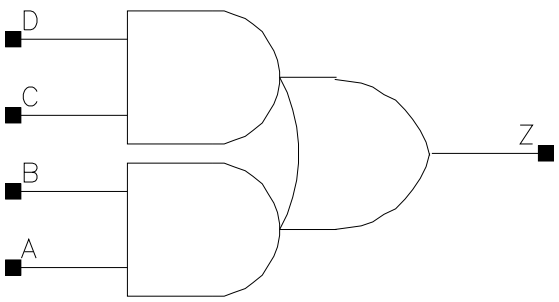
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.088	0.8704
X10_P0	0.800	1.088	0.8704
X14_P0	0.800	1.768	1.4144
X19_P0	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0005	0.0006	0.0013	0.0013
B	0.0005	0.0008	0.0012	0.0012
C	0.0005	0.0006	0.0013	0.0013
D	0.0005	0.0007	0.0012	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0250	0.0217	2.4398	1.2316
A to Z ↑	0.0189	0.0179	3.0180	1.4966
B to Z ↓	0.0228	0.0198	2.4298	1.2264

B to Z ↑	0.0205	0.0198	3.0153	1.4939
C to Z ↓	0.0242	0.0213	2.4312	1.2269
C to Z ↑	0.0159	0.0150	3.0102	1.4914
D to Z ↓	0.0231	0.0202	2.4272	1.2242
D to Z ↑	0.0180	0.0169	3.0105	1.4899
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0194	0.0211	0.8415	0.6330
A to Z ↑	0.0161	0.0174	1.0360	0.7748
B to Z ↓	0.0182	0.0199	0.8406	0.6328
B to Z ↑	0.0179	0.0193	1.0348	0.7739
C to Z ↓	0.0195	0.0212	0.8396	0.6318
C to Z ↑	0.0135	0.0148	1.0335	0.7729
D to Z ↓	0.0184	0.0202	0.8390	0.6313
D to Z ↑	0.0150	0.0165	1.0316	0.7709

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	3.889e-04	1.000e-20
X10_P0	7.881e-04	1.000e-20
X14_P0	1.319e-03	1.000e-20
X19_P0	1.524e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	3.535e-05	4.699e-05	6.114e-05	6.086e-05
B (output stable)	1.086e-04	1.117e-04	7.445e-05	7.417e-05
C (output stable)	3.963e-05	4.925e-05	1.185e-04	1.170e-04
D (output stable)	4.199e-05	5.932e-05	1.355e-04	1.351e-04
A to Z	3.736e-03	6.188e-03	9.772e-03	1.205e-02
B to Z	3.505e-03	5.840e-03	9.455e-03	1.176e-02
C to Z	3.385e-03	5.628e-03	8.785e-03	1.100e-02
D to Z	3.286e-03	5.497e-03	8.493e-03	1.073e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

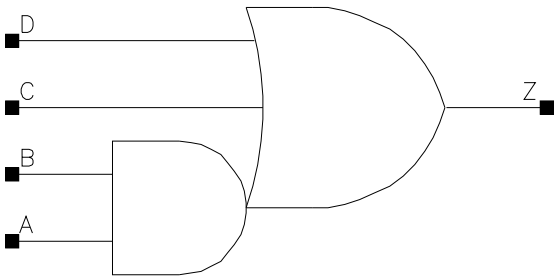
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	1.088	0.8704
X19_P0	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0004	0.0006	0.0012
B	0.0005	0.0007	0.0012
C	0.0005	0.0006	0.0013
D	0.0004	0.0006	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0312	0.0277	2.6669	1.2615
A to Z ↑	0.0165	0.0145	3.1185	1.5046
B to Z ↓	0.0301	0.0259	2.6616	1.2571
B to Z ↑	0.0185	0.0163	3.1218	1.5048
C to Z ↓	0.0295	0.0250	2.6607	1.2586
C to Z ↑	0.0159	0.0214	3.0942	1.5029

D to Z ↓	0.0306	0.0264	2.6599	1.2594
D to Z ↑	0.0156	0.0209	3.0947	1.5030
	X19_P0		**X19_P0**	
A to Z ↓	0.0273		0.6523	
A to Z ↑	0.0165		0.7489	
B to Z ↓	0.0250		0.6492	
B to Z ↑	0.0178		0.7481	
C to Z ↓	0.0248		0.6500	
C to Z ↑	0.0172		0.7421	
D to Z ↓	0.0257		0.6499	
D to Z ↑	0.0170		0.7413	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	2.206e-04	1.000e-20
X10_P0	4.956e-04	1.000e-20
X19_P0	9.307e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	5.095e-05	9.595e-05	1.591e-04
B (output stable)	4.958e-05	9.490e-05	1.782e-04
C (output stable)	2.702e-05	4.937e-05	1.029e-04
D (output stable)	3.312e-05	6.064e-05	1.135e-04
A to Z	3.363e-03	5.980e-03	1.181e-02
B to Z	3.291e-03	5.807e-03	1.129e-02
C to Z	3.550e-03	6.506e-03	1.243e-02
D to Z	3.444e-03	6.325e-03	1.201e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

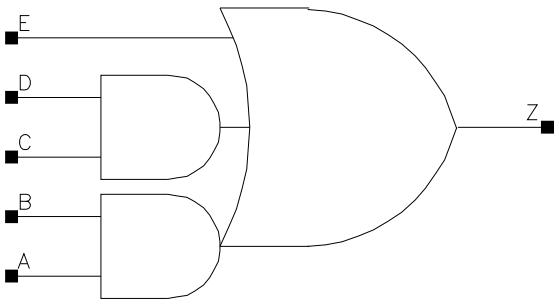
Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.088	0.8704
X10_P0	0.800	1.224	0.9792
X19_P0	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0004	0.0006	0.0012
B	0.0005	0.0006	0.0011
C	0.0005	0.0008	0.0013
D	0.0005	0.0006	0.0011
E	0.0004	0.0006	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0346	0.0282	2.5156	1.2592
A to Z ↑	0.0219	0.0189	3.0432	1.5129

B to Z ↓	0.0340	0.0270	2.5118	1.2576
B to Z ↑	0.0247	0.0210	3.0403	1.5099
C to Z ↓	0.0341	0.0286	2.5101	1.2571
C to Z ↑	0.0186	0.0158	3.0264	1.5036
D to Z ↓	0.0321	0.0261	2.5010	1.2512
D to Z ↑	0.0209	0.0174	3.0211	1.5017
E to Z ↓	0.0325	0.0267	2.4997	1.2525
E to Z ↑	0.0172	0.0148	2.9921	1.4912
	X19_P0		**X19_P0**	
A to Z ↓	0.0273		0.6475	
A to Z ↑	0.0197		0.7599	
B to Z ↓	0.0261		0.6470	
B to Z ↑	0.0220		0.7586	
C to Z ↓	0.0270		0.6453	
C to Z ↑	0.0161		0.7548	
D to Z ↓	0.0257		0.6441	
D to Z ↑	0.0180		0.7539	
E to Z ↓	0.0255		0.6442	
E to Z ↑	0.0194		0.7502	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	2.866e-04	1.000e-20
X10_P0	6.221e-04	1.000e-20
X19_P0	1.154e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	1.565e-05	2.689e-05	5.298e-05
B (output stable)	1.990e-05	2.878e-05	5.402e-05
C (output stable)	6.100e-05	7.224e-05	1.561e-04
D (output stable)	6.263e-05	8.566e-05	1.650e-04
E (output stable)	8.101e-05	1.191e-04	2.484e-04
A to Z	4.329e-03	7.037e-03	1.369e-02
B to Z	4.274e-03	6.900e-03	1.340e-02
C to Z	3.845e-03	6.219e-03	1.195e-02
D to Z	3.736e-03	6.009e-03	1.168e-02
E to Z	3.857e-03	6.305e-03	1.237e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

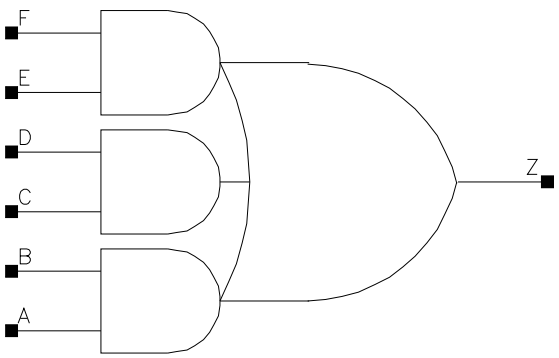
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.360	1.0880
X5_P0	0.800	1.360	1.0880
X10_P0	0.800	1.632	1.3056
X19_P0	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P0	X5_P0	X10_P0	X19_P0
A	0.0005	0.0005	0.0007	0.0012

B	0.0005	0.0005	0.0008	0.0011
C	0.0007	0.0007	0.0006	0.0012
D	0.0005	0.0005	0.0006	0.0011
E	0.0007	0.0007	0.0006	0.0013
F	0.0006	0.0006	0.0006	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	X5_P0	X2_P0	X5_P0
A to Z ↓	0.0267	0.0278	4.7077	2.6159
A to Z ↑	0.0217	0.0216	5.7395	3.1956
B to Z ↓	0.0254	0.0265	4.6943	2.6088
B to Z ↑	0.0243	0.0243	5.7302	3.1923
C to Z ↓	0.0261	0.0273	4.7056	2.6146
C to Z ↑	0.0198	0.0199	5.6878	3.1745
D to Z ↓	0.0239	0.0251	4.6903	2.6076
D to Z ↑	0.0217	0.0218	5.6784	3.1696
E to Z ↓	0.0239	0.0250	4.6843	2.6049
E to Z ↑	0.0161	0.0162	5.6582	3.1609
F to Z ↓	0.0221	0.0233	4.6723	2.5993
F to Z ↑	0.0177	0.0179	5.6525	3.1597
	X10_P0	X19_P0	X10_P0	X19_P0
A to Z ↓	0.0303	0.0283	1.2580	0.6453
A to Z ↑	0.0235	0.0215	1.5215	0.7631
B to Z ↓	0.0286	0.0274	1.2523	0.6446
B to Z ↑	0.0257	0.0238	1.5198	0.7616
C to Z ↓	0.0291	0.0277	1.2547	0.6447
C to Z ↑	0.0210	0.0196	1.5118	0.7584
D to Z ↓	0.0280	0.0268	1.2517	0.6441
D to Z ↑	0.0233	0.0219	1.5112	0.7576
E to Z ↓	0.0278	0.0271	1.2512	0.6430
E to Z ↑	0.0178	0.0170	1.5059	0.7558
F to Z ↓	0.0262	0.0255	1.2472	0.6416
F to Z ↑	0.0197	0.0190	1.5045	0.7551

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P0	3.502e-04	1.000e-20
X5_P0	4.434e-04	1.000e-20
X10_P0	7.394e-04	1.000e-20
X19_P0	1.446e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P0	X5_P0	X10_P0	X19_P0
A (output stable)	3.228e-05	3.248e-05	5.019e-05	7.442e-05
B (output stable)	3.352e-05	3.381e-05	8.500e-05	7.898e-05
C (output stable)	4.679e-05	4.696e-05	4.784e-05	9.812e-05
D (output stable)	5.072e-05	5.103e-05	5.379e-05	1.118e-04
E (output stable)	1.006e-04	1.014e-04	1.289e-04	2.045e-04
F (output stable)	1.089e-04	1.096e-04	1.289e-04	2.153e-04

A to Z	3.631e-03	4.467e-03	7.760e-03	1.447e-02
B to Z	3.507e-03	4.340e-03	7.444e-03	1.420e-02
C to Z	3.181e-03	3.988e-03	7.116e-03	1.334e-02
D to Z	3.047e-03	3.849e-03	6.987e-03	1.312e-02
E to Z	2.745e-03	3.497e-03	6.487e-03	1.235e-02
F to Z	2.625e-03	3.377e-03	6.339e-03	1.205e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

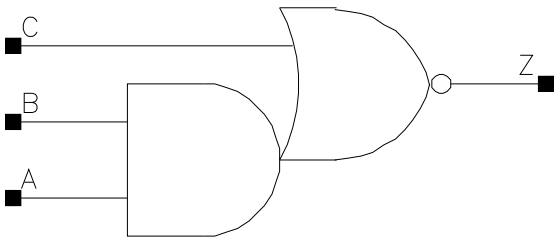
Pin Cycle (vdds)	X2_P0	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X10_P0	0.800	1.360	1.0880
X19_P0	0.800	2.584	2.0672
X25_P0	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P0	X10_P0	X19_P0	X25_P0
A	0.0006	0.0016	0.0032	0.0042
B	0.0005	0.0014	0.0029	0.0040
C	0.0006	0.0017	0.0032	0.0043

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X10_P0**	**X3_P0**	**X10_P0**
A to Z ↓	0.0047	0.0049	3.9064	1.4124
A to Z ↑	0.0116	0.0118	5.6352	1.9410
B to Z ↓	0.0057	0.0063	3.9582	1.4316
B to Z ↑	0.0096	0.0093	5.5010	1.9351
C to Z ↓	0.0054	0.0057	2.5713	0.8927
C to Z ↑	0.0101	0.0102	5.1194	1.7865
	X19_P0	**X25_P0**	**X19_P0**	**X25_P0**
A to Z ↓	0.0053	0.0053	0.7240	0.5527

A to Z ↑	0.0121	0.0119	0.9997	0.7434
B to Z ↓	0.0063	0.0063	0.7340	0.5609
B to Z ↑	0.0095	0.0094	0.9981	0.7551
C to Z ↓	0.0074	0.0074	0.5405	0.4124
C to Z ↑	0.0100	0.0099	0.9231	0.6919

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.764e-04	1.000e-20
X10_P0	7.402e-04	1.000e-20
X19_P0	1.422e-03	1.000e-20
X25_P0	1.889e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X10_P0	X19_P0	X25_P0
A (output stable)	4.918e-05	1.759e-04	3.541e-04	4.679e-04
B (output stable)	6.134e-05	2.143e-04	4.382e-04	5.651e-04
C (output stable)	8.275e-05	2.587e-04	5.032e-04	6.847e-04
A to Z	1.701e-03	5.055e-03	1.006e-02	1.332e-02
B to Z	1.589e-03	4.462e-03	8.908e-03	1.176e-02
C to Z	2.109e-03	6.110e-03	1.167e-02	1.551e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

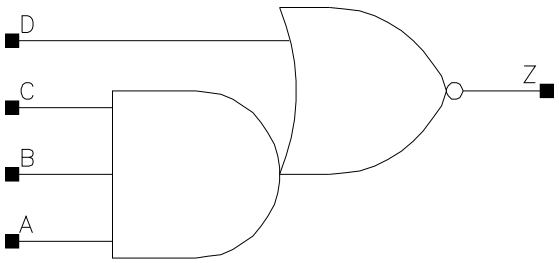
Pin Cycle (vdds)	X3_P0	X10_P0	X19_P0	X25_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X17_P0	0.800	3.536	2.8288
X22_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X17_P0	X22_P0
A	0.0005	0.0031	0.0043
B	0.0005	0.0030	0.0041
C	0.0007	0.0029	0.0040
D	0.0006	0.0033	0.0042

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X17_P0**	**X3_P0**	**X17_P0**
A to Z ↓	0.0080	0.0084	5.2698	1.0186
A to Z ↑	0.0144	0.0137	5.6267	0.9558
B to Z ↓	0.0093	0.0097	5.2973	1.0247
B to Z ↑	0.0129	0.0122	5.6405	0.9744
C to Z ↓	0.0106	0.0101	5.3407	1.0305
C to Z ↑	0.0120	0.0100	5.6760	0.9810
D to Z ↓	0.0073	0.0091	2.5185	0.5326

D to Z ↑	0.0127	0.0113	4.8650	0.8371
	X22_P0		**X22_P0**	
A to Z ↓	0.0084		0.7747	
A to Z ↑	0.0135		0.7150	
B to Z ↓	0.0095		0.7797	
B to Z ↑	0.0120		0.7317	
C to Z ↓	0.0101		0.7846	
C to Z ↑	0.0098		0.7400	
D to Z ↓	0.0098		0.4407	
D to Z ↑	0.0107		0.6275	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.800e-04	1.000e-20
X17_P0	1.376e-03	1.000e-20
X22_P0	1.799e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X17_P0	X22_P0
A (output stable)	4.198e-05	2.613e-04	3.457e-04
B (output stable)	4.606e-05	2.995e-04	3.940e-04
C (output stable)	5.526e-05	4.495e-04	5.874e-04
D (output stable)	1.230e-04	7.304e-04	9.691e-04
A to Z	2.046e-03	1.149e-02	1.509e-02
B to Z	1.874e-03	1.021e-02	1.336e-02
C to Z	1.733e-03	9.108e-03	1.195e-02
D to Z	2.565e-03	1.346e-02	1.737e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

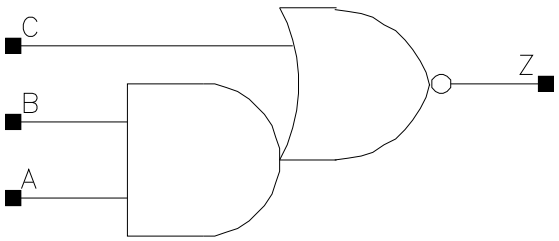
Pin Cycle (vdds)	X3_P0	X17_P0	X22_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X6_P0	0.800	1.088	0.8704
X9_P0	0.800	1.360	1.0880
X12_P0	0.800	1.904	1.5232
X25_P0	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X9_P0	X12_P0
A	0.0005	0.0011	0.0017	0.0023
B	0.0005	0.0011	0.0016	0.0022
C	0.0006	0.0010	0.0015	0.0020
	X25_P0			
A	0.0046			
B	0.0043			
C	0.0040			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0076	0.0071	5.0424	2.0620
A to Z ↑	0.0105	0.0113	6.3741	2.8801
B to Z ↓	0.0094	0.0082	5.0827	2.0836

B to Z ↑	0.0091	0.0090	6.2692	2.8939
C to Z ↓	0.0042	0.0038	3.3637	1.6018
C to Z ↑	0.0101	0.0094	5.8613	2.6756
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0067	0.0070	1.4134	1.0636
A to Z ↑	0.0106	0.0106	1.9292	1.4259
B to Z ↓	0.0082	0.0082	1.4308	1.0761
B to Z ↑	0.0082	0.0082	1.9323	1.4491
C to Z ↓	0.0038	0.0037	1.0905	0.8151
C to Z ↑	0.0089	0.0090	1.7943	1.3364
	X25_P0		**X25_P0**	
A to Z ↓	0.0069		0.5530	
A to Z ↑	0.0103		0.7271	
B to Z ↓	0.0083		0.5593	
B to Z ↑	0.0079		0.7316	
C to Z ↓	0.0037		0.4138	
C to Z ↑	0.0088		0.6790	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.284e-04	1.000e-20
X6_P0	5.255e-04	1.000e-20
X9_P0	7.494e-04	1.000e-20
X12_P0	9.974e-04	1.000e-20
X25_P0	1.944e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	1.980e-05	6.312e-05	8.242e-05	1.196e-04
B (output stable)	2.327e-05	9.622e-05	1.132e-04	1.795e-04
C (output stable)	1.772e-04	4.717e-04	5.705e-04	8.026e-04
A to Z	1.705e-03	4.024e-03	5.754e-03	7.797e-03
B to Z	1.582e-03	3.618e-03	5.103e-03	6.902e-03
C to Z	1.493e-03	3.317e-03	4.730e-03	6.443e-03
	X25_P0			
A (output stable)	2.293e-04			
B (output stable)	3.143e-04			
C (output stable)	1.491e-03			
A to Z	1.510e-02			
B to Z	1.349e-02			
C to Z	1.246e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

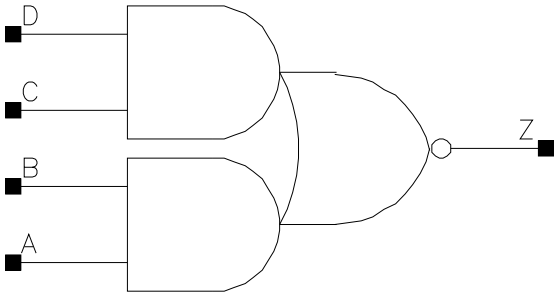
	X25_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.680	0.5440
X6_P0	0.800	1.224	0.9792
X9_P0	0.800	1.768	1.4144
X12_P0	0.800	2.448	1.9584
X24_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P0	X6_P0	X9_P0	X12_P0
A	0.0005	0.0012	0.0017	0.0023
B	0.0004	0.0010	0.0016	0.0023
C	0.0004	0.0012	0.0016	0.0021
D	0.0004	0.0010	0.0015	0.0021
	X24_P0			
A	0.0044			
B	0.0045			
C	0.0044			
D	0.0042			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X6_P0**	**X2_P0**	**X6_P0**
A to Z ↓	0.0073	0.0080	5.1404	1.9680
A to Z ↑	0.0135	0.0117	7.8692	2.6223
B to Z ↓	0.0090	0.0096	5.1990	1.9894
B to Z ↑	0.0119	0.0102	7.8414	2.6951
C to Z ↓	0.0045	0.0049	5.1688	1.9805
C to Z ↑	0.0129	0.0112	7.8471	2.6157
D to Z ↓	0.0058	0.0062	5.2457	2.0091
D to Z ↑	0.0110	0.0097	7.8119	2.7163
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0087	0.0090	1.4112	1.0657
A to Z ↑	0.0123	0.0125	1.7683	1.3314
B to Z ↓	0.0105	0.0107	1.4268	1.0768
B to Z ↑	0.0103	0.0104	1.7734	1.3146
C to Z ↓	0.0055	0.0059	1.4115	1.0700
C to Z ↑	0.0117	0.0119	1.7657	1.3179
D to Z ↓	0.0070	0.0069	1.4315	1.0845
D to Z ↑	0.0095	0.0096	1.7655	1.3241
	X24_P0		**X24_P0**	
A to Z ↓	0.0092		0.5504	
A to Z ↑	0.0123		0.6745	
B to Z ↓	0.0108		0.5566	
B to Z ↑	0.0102		0.6692	
C to Z ↓	0.0060		0.5393	
C to Z ↑	0.0121		0.6710	
D to Z ↓	0.0070		0.5475	
D to Z ↑	0.0096		0.6740	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P0	1.897e-04	1.000e-20
X6_P0	6.251e-04	1.000e-20
X9_P0	8.748e-04	1.000e-20
X12_P0	1.158e-03	1.000e-20
X24_P0	2.254e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P0	X6_P0	X9_P0	X12_P0
A (output stable)	2.302e-05	5.858e-05	1.080e-04	1.602e-04
B (output stable)	2.569e-05	7.182e-05	1.748e-04	2.775e-04
C (output stable)	5.050e-05	1.110e-04	1.985e-04	2.844e-04
D (output stable)	5.739e-05	1.318e-04	2.574e-04	3.944e-04
A to Z	1.611e-03	4.433e-03	6.686e-03	9.019e-03
B to Z	1.481e-03	4.047e-03	6.036e-03	8.219e-03
C to Z	1.282e-03	3.594e-03	5.413e-03	7.332e-03
D to Z	1.166e-03	3.230e-03	4.819e-03	6.532e-03
	X24_P0			
A (output stable)	2.936e-04			
B (output stable)	4.632e-04			
C (output stable)	5.445e-04			
D (output stable)	7.467e-04			

A to Z	1.763e-02			
B to Z	1.604e-02			
C to Z	1.442e-02			
D to Z	1.284e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

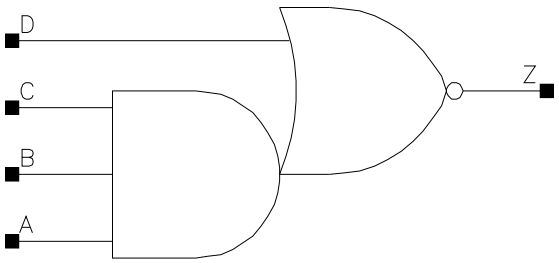
Pin Cycle (vdds)	X2_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X12_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X12_P0
A	0.0006	0.0022
B	0.0006	0.0021
C	0.0008	0.0020
D	0.0006	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X12_P0**	**X3_P0**	**X12_P0**
A to Z ↓	0.0097	0.0099	5.2683	1.5084
A to Z ↑	0.0130	0.0124	5.4799	1.4499
B to Z ↓	0.0114	0.0112	5.2943	1.5144
B to Z ↑	0.0120	0.0108	5.5747	1.4517
C to Z ↓	0.0132	0.0120	5.3340	1.5218
C to Z ↑	0.0113	0.0086	5.6312	1.4636
D to Z ↓	0.0037	0.0032	2.5776	0.6950
D to Z ↑	0.0110	0.0096	4.8004	1.2531

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.902e-04	1.000e-20
X12_P0	9.912e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X12_P0
A (output stable)	1.684e-05	9.052e-05
B (output stable)	2.147e-05	1.214e-04
C (output stable)	3.752e-05	2.050e-04
D (output stable)	3.385e-04	1.141e-03
A to Z	2.325e-03	8.516e-03
B to Z	2.151e-03	7.628e-03
C to Z	2.017e-03	6.889e-03
D to Z	1.978e-03	7.001e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

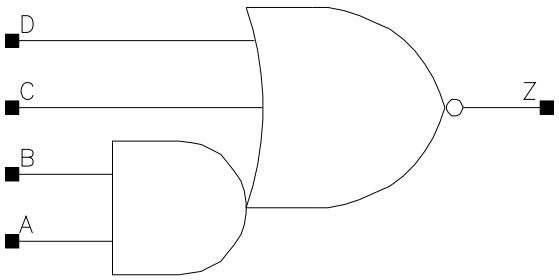
Pin Cycle (vdds)	X3_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X20_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P0	X20_P0
A	0.0005	0.0041
B	0.0005	0.0039
C	0.0006	0.0040
D	0.0006	0.0037

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X20_P0	X3_P0	X20_P0
A to Z ↓	0.0054	0.0064	3.8420	0.6257
A to Z ↑	0.0159	0.0146	8.0057	1.0527
B to Z ↓	0.0066	0.0076	3.8974	0.6357
B to Z ↑	0.0142	0.0119	8.0966	1.0534
C to Z ↓	0.0065	0.0111	2.5584	0.5271
C to Z ↑	0.0149	0.0129	7.6460	1.0001
D to Z ↓	0.0061	0.0099	2.5641	0.5274

D to Z ↑	0.0160	0.0133	7.6729	1.0042

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.389e-04	1.000e-20
X20_P0	1.518e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X20_P0
A (output stable)	9.311e-05	6.417e-04
B (output stable)	9.983e-05	6.832e-04
C (output stable)	4.959e-05	4.834e-04
D (output stable)	5.989e-05	6.344e-04
A to Z	1.827e-03	1.259e-02
B to Z	1.680e-03	1.117e-02
C to Z	2.389e-03	1.626e-02
D to Z	2.182e-03	1.417e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

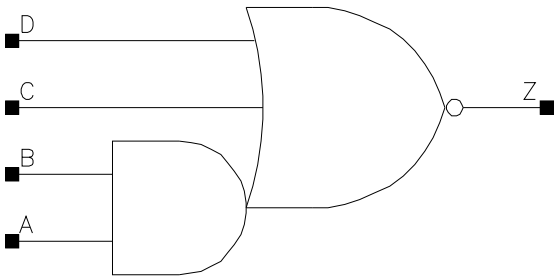
Pin Cycle (vdds)	X3_P0	X20_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.816	0.6528
X10_P0	0.800	2.448	1.9584
X19_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P0	X10_P0	X19_P0
A	0.0005	0.0021	0.0043
B	0.0005	0.0020	0.0041
C	0.0006	0.0018	0.0036
D	0.0005	0.0018	0.0034

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	X10_P0	X2_P0	X10_P0
A to Z ↓	0.0082	0.0083	4.5213	1.2043
A to Z ↑	0.0150	0.0136	8.4929	2.0935
B to Z ↓	0.0100	0.0098	4.5714	1.2163
B to Z ↑	0.0133	0.0112	8.5252	2.1038
C to Z ↓	0.0081	0.0074	4.1967	1.0501
C to Z ↑	0.0128	0.0110	8.0943	1.9944

D to Z ↓	0.0064	0.0051	4.2335	1.0622
D to Z ↑	0.0129	0.0109	8.1024	1.9992
	X19_P0		**X19_P0**	
A to Z ↓	0.0081		0.6181	
A to Z ↑	0.0132		1.0680	
B to Z ↓	0.0098		0.6250	
B to Z ↑	0.0108		1.0684	
C to Z ↓	0.0081		0.5677	
C to Z ↑	0.0104		1.0168	
D to Z ↓	0.0058		0.5745	
D to Z ↑	0.0103		1.0194	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P0	2.085e-04	1.000e-20
X10_P0	8.681e-04	1.000e-20
X19_P0	1.711e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P0	X10_P0	X19_P0
A (output stable)	2.233e-05	9.512e-05	1.858e-04
B (output stable)	2.213e-05	1.224e-04	2.272e-04
C (output stable)	6.059e-05	2.771e-04	5.547e-04
D (output stable)	1.138e-04	5.646e-04	1.084e-03
A to Z	2.121e-03	8.099e-03	1.574e-02
B to Z	1.974e-03	7.278e-03	1.424e-02
C to Z	1.642e-03	6.417e-03	1.212e-02
D to Z	1.492e-03	5.552e-03	1.044e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

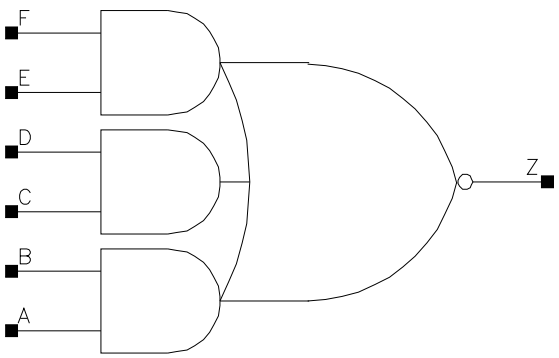
Pin Cycle (vdds)	X2_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.088	0.8704
X5_P0	0.800	2.040	1.6320
X7_P0	0.800	2.720	2.1760
X9_P0	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P0	X5_P0	X7_P0	X9_P0
A	0.0005	0.0010	0.0016	0.0021

B	0.0005	0.0011	0.0015	0.0020
C	0.0005	0.0009	0.0015	0.0023
D	0.0005	0.0011	0.0014	0.0019
E	0.0007	0.0011	0.0015	0.0020
F	0.0005	0.0009	0.0014	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X5_P0**	**X2_P0**	**X5_P0**
A to Z ↓	0.0093	0.0120	4.0488	2.2818
A to Z ↑	0.0194	0.0182	8.2589	3.8057
B to Z ↓	0.0112	0.0140	4.1005	2.2989
B to Z ↑	0.0176	0.0168	8.2950	3.7664
C to Z ↓	0.0083	0.0106	4.0728	2.2738
C to Z ↑	0.0184	0.0176	8.3134	3.8154
D to Z ↓	0.0100	0.0124	4.1357	2.2960
D to Z ↑	0.0165	0.0162	8.2947	3.7884
E to Z ↓	0.0059	0.0076	4.1065	2.2373
E to Z ↑	0.0168	0.0162	8.2669	3.7645
F to Z ↓	0.0070	0.0090	4.1811	2.2640
F to Z ↑	0.0145	0.0144	8.2290	3.7873
	X7_P0	**X9_P0**	**X7_P0**	**X9_P0**
A to Z ↓	0.0118	0.0122	1.5844	1.2077
A to Z ↑	0.0174	0.0179	2.4844	1.8813
B to Z ↓	0.0137	0.0140	1.5988	1.2177
B to Z ↑	0.0157	0.0159	2.5493	1.9154
C to Z ↓	0.0104	0.0110	1.5876	1.2013
C to Z ↑	0.0170	0.0178	2.5403	1.9168
D to Z ↓	0.0123	0.0122	1.6056	1.2135
D to Z ↑	0.0149	0.0150	2.5150	1.8977
E to Z ↓	0.0071	0.0072	1.5893	1.2057
E to Z ↑	0.0153	0.0154	2.4997	1.8962
F to Z ↓	0.0088	0.0084	1.6126	1.2231
F to Z ↑	0.0133	0.0130	2.5264	1.8922

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P0	3.206e-04	1.000e-20
X5_P0	7.027e-04	1.000e-20
X7_P0	1.039e-03	1.000e-20
X9_P0	1.289e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P0	X5_P0	X7_P0	X9_P0
A (output stable)	3.723e-05	7.201e-05	1.221e-04	1.686e-04
B (output stable)	3.940e-05	8.383e-05	1.548e-04	2.418e-04
C (output stable)	5.806e-05	1.102e-04	1.612e-04	2.311e-04
D (output stable)	6.321e-05	1.222e-04	2.037e-04	2.935e-04
E (output stable)	1.030e-04	2.230e-04	3.317e-04	4.876e-04
F (output stable)	1.243e-04	2.338e-04	3.690e-04	5.522e-04

A to Z	2.651e-03	5.442e-03	7.952e-03	1.071e-02
B to Z	2.484e-03	5.220e-03	7.365e-03	9.888e-03
C to Z	2.188e-03	4.590e-03	6.687e-03	8.941e-03
D to Z	2.029e-03	4.373e-03	6.150e-03	8.240e-03
E to Z	1.770e-03	3.872e-03	5.490e-03	7.226e-03
F to Z	1.625e-03	3.581e-03	4.957e-03	6.510e-03

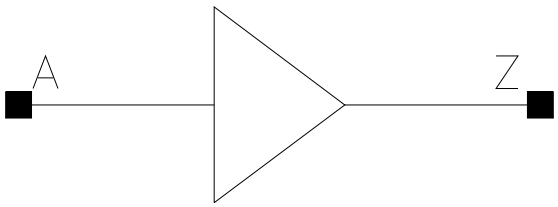
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X2_P0	X5_P0	X7_P0	X9_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description
Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.544	0.4352
X5_P0	0.800	0.544	0.4352
X9_P0	0.800	0.680	0.5440
X11_P0	1.600	0.408	0.6528
X13_P0	0.800	0.680	0.5440
X19_P0	0.800	0.952	0.7616
X23_P0	1.600	0.544	0.8704
X24_P0	0.800	1.088	0.8704
X29_P0	0.800	1.224	0.9792
X34_P0	1.600	0.680	1.0880
X38_P0	0.800	1.632	1.3056
X46_P0	1.600	0.952	1.5232
X57_P0	0.800	2.312	1.8496
X68_P0	1.600	1.224	1.9584
X91_P0	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P0	X5_P0	X9_P0	X11_P0
A	0.0006	0.0006	0.0006	0.0008
	X13_P0	X19_P0	X23_P0	X24_P0
A	0.0007	0.0010	0.0012	0.0011
	X29_P0	X34_P0	X38_P0	X46_P0
A	0.0013	0.0015	0.0020	0.0019
	X57_P0	X68_P0	X91_P0	
A	0.0026	0.0027	0.0036	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X5_P0**	**X2_P0**	**X5_P0**
A to Z ↓	0.0152	0.0158	4.5359	2.5191
A to Z ↑	0.0116	0.0119	5.5876	3.0844
	X9_P0	**X11_P0**	**X9_P0**	**X11_P0**
A to Z ↓	0.0188	0.0179	1.2808	0.9734
A to Z ↑	0.0148	0.0128	1.5258	1.4370
	X13_P0	**X19_P0**	**X13_P0**	**X19_P0**
A to Z ↓	0.0169	0.0169	0.8782	0.6209
A to Z ↑	0.0141	0.0130	1.0702	0.7506
	X23_P0	**X24_P0**	**X23_P0**	**X24_P0**
A to Z ↓	0.0170	0.0168	0.4700	0.5062
A to Z ↑	0.0126	0.0136	0.7279	0.6023
	X29_P0	**X34_P0**	**X29_P0**	**X34_P0**
A to Z ↓	0.0162	0.0169	0.4195	0.3234
A to Z ↑	0.0134	0.0128	0.5069	0.5003
	X38_P0	**X46_P0**	**X38_P0**	**X46_P0**
A to Z ↓	0.0159	0.0166	0.3175	0.2427
A to Z ↑	0.0132	0.0123	0.3726	0.3761
	X57_P0	**X68_P0**	**X57_P0**	**X68_P0**
A to Z ↓	0.0167	0.0165	0.2136	0.1645
A to Z ↑	0.0139	0.0127	0.2500	0.2516
	X91_P0		**X91_P0**	
A to Z ↓	0.0175		0.1262	
A to Z ↑	0.0133		0.1892	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P0	1.872e-04	1.000e-20
X5_P0	3.002e-04	1.000e-20
X9_P0	5.274e-04	1.000e-20
X11_P0	6.239e-04	1.000e-20
X13_P0	8.182e-04	1.000e-20
X19_P0	1.046e-03	1.000e-20
X23_P0	1.235e-03	1.000e-20
X24_P0	1.320e-03	1.000e-20
X29_P0	1.593e-03	1.000e-20
X34_P0	1.771e-03	1.000e-20
X38_P0	2.158e-03	1.000e-20
X46_P0	2.297e-03	1.000e-20
X57_P0	3.099e-03	1.000e-20
X68_P0	3.419e-03	1.000e-20
X91_P0	4.373e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P0	X5_P0	X9_P0	X11_P0
A to Z	2.044e-03	2.648e-03	4.455e-03	5.144e-03
	X13_P0	X19_P0	X23_P0	X24_P0
A to Z	6.468e-03	8.954e-03	9.808e-03	1.111e-02
	X29_P0	X34_P0	X38_P0	X46_P0

A to Z	1.303e-02	1.443e-02	1.779e-02	1.890e-02
	X57_P0	X68_P0	X91_P0	
A to Z	2.648e-02	2.815e-02	3.773e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

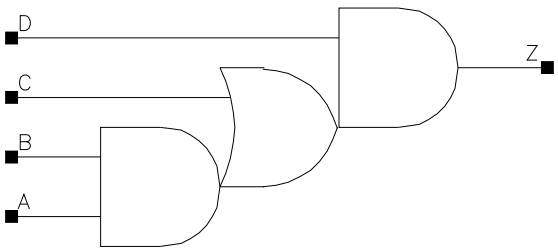
Pin Cycle (vdds)	X2_P0	X5_P0	X9_P0	X11_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P0	X19_P0	X23_P0	X24_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P0	X34_P0	X38_P0	X46_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P0	X68_P0	X91_P0	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.952	0.7616
X10_P0	0.800	1.632	1.3056
X14_P0	0.800	1.768	1.4144
X19_P0	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0006	0.0013	0.0013	0.0013
B	0.0006	0.0012	0.0012	0.0012
C	0.0007	0.0014	0.0014	0.0014
D	0.0010	0.0013	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0188	0.0171	2.5664	1.2115
A to Z ↑	0.0202	0.0187	3.1766	1.5162
B to Z ↓	0.0174	0.0158	2.5602	1.2121
B to Z ↑	0.0214	0.0197	3.1755	1.5141
C to Z ↓	0.0178	0.0164	2.5559	1.2082
C to Z ↑	0.0153	0.0139	3.1387	1.4974

D to Z ↓	0.0169	0.0147	2.5396	1.2008
D to Z ↑	0.0165	0.0142	3.1502	1.5021
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0192	0.0208	0.8422	0.6299
A to Z ↑	0.0209	0.0225	1.0167	0.7607
B to Z ↓	0.0181	0.0197	0.8410	0.6298
B to Z ↑	0.0220	0.0236	1.0163	0.7607
C to Z ↓	0.0185	0.0201	0.8389	0.6274
C to Z ↑	0.0158	0.0171	1.0024	0.7502
D to Z ↓	0.0161	0.0171	0.8308	0.6208
D to Z ↑	0.0160	0.0172	1.0061	0.7529

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	5.090e-04	1.000e-20
X10_P0	1.034e-03	1.000e-20
X14_P0	1.268e-03	1.000e-20
X19_P0	1.503e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	4.599e-05	8.648e-05	8.917e-05	8.914e-05
B (output stable)	5.662e-05	1.062e-04	1.097e-04	1.083e-04
C (output stable)	1.771e-04	2.876e-04	2.919e-04	2.934e-04
D (output stable)	8.873e-05	1.411e-04	1.445e-04	1.428e-04
A to Z	3.894e-03	7.435e-03	9.811e-03	1.222e-02
B to Z	3.739e-03	7.070e-03	9.452e-03	1.188e-02
C to Z	3.436e-03	6.431e-03	8.556e-03	1.068e-02
D to Z	3.987e-03	7.527e-03	9.494e-03	1.141e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

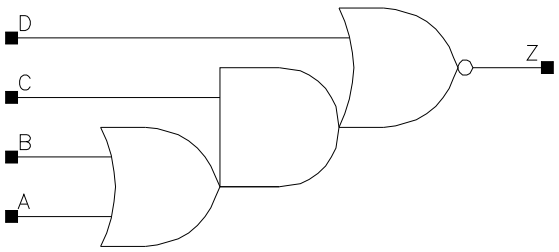
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X6_P0	0.800	1.496	1.1968
X9_P0	0.800	1.768	1.4144
X12_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X9_P0	X12_P0
A	0.0006	0.0011	0.0017	0.0022
B	0.0006	0.0010	0.0016	0.0022
C	0.0006	0.0011	0.0016	0.0021
D	0.0008	0.0011	0.0016	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0082	0.0072	3.9880	2.0470
A to Z ↑	0.0159	0.0156	8.0302	4.2955
B to Z ↓	0.0076	0.0071	3.8688	2.0586
B to Z ↑	0.0170	0.0164	8.0458	4.3073
C to Z ↓	0.0085	0.0079	3.7122	1.9331
C to Z ↑	0.0104	0.0096	5.6492	2.9489

D to Z ↓	0.0035	0.0023	2.6038	1.3259
D to Z ↑	0.0124	0.0111	5.9741	3.1336
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0073	0.0078	1.3966	1.0922
A to Z ↑	0.0143	0.0150	2.7465	2.1330
B to Z ↓	0.0068	0.0071	1.4120	1.0937
B to Z ↑	0.0153	0.0157	2.7534	2.1370
C to Z ↓	0.0082	0.0084	1.3308	1.0309
C to Z ↑	0.0089	0.0091	1.9139	1.4587
D to Z ↓	0.0026	0.0026	0.9160	0.7011
D to Z ↑	0.0102	0.0101	2.0230	1.5504

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.854e-04	1.000e-20
X6_P0	5.437e-04	1.000e-20
X9_P0	7.829e-04	1.000e-20
X12_P0	1.018e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	1.932e-05	4.583e-05	5.773e-05	9.377e-05
B (output stable)	2.362e-05	5.423e-05	7.487e-05	1.266e-04
C (output stable)	6.390e-05	1.430e-04	1.940e-04	2.668e-04
D (output stable)	1.948e-04	5.191e-04	7.137e-04	1.082e-03
A to Z	2.311e-03	4.415e-03	6.313e-03	8.455e-03
B to Z	2.112e-03	3.874e-03	5.700e-03	7.511e-03
C to Z	2.019e-03	3.780e-03	5.453e-03	7.326e-03
D to Z	1.819e-03	3.360e-03	4.861e-03	6.371e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

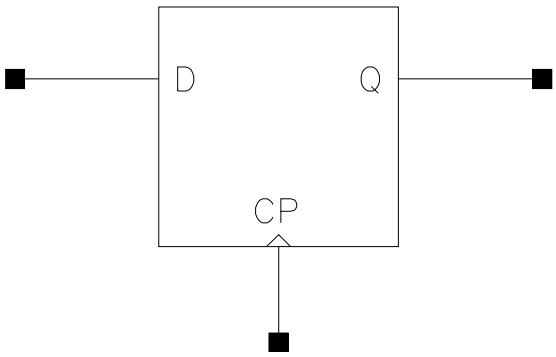
Pin Cycle (vdds)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	1.600	1.496	2.3936
X19_P0	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P0	X19_P0
CP	0.0008	0.0008
D	0.0007	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	X19_P0	X10_P0	X19_P0
CP to Q ↓	0.0301	0.0405	1.2341	0.6546
CP to Q ↑	0.0357	0.0416	1.4814	0.7597

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P0	X19_P0
CP ↓	min_pulse_width to CP	0.0294	0.0294
CP ↑	min_pulse_width to CP	0.0271	0.0365
D ↓	hold_rising to CP	0.0201	0.0201
D ↑	hold_rising to CP	0.0124	0.0124
D ↓	setup_rising to CP	0.0096	0.0096
D ↑	setup_rising to CP	0.0119	0.0119

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P0	1.357e-03	1.000e-20
X19_P0	1.738e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

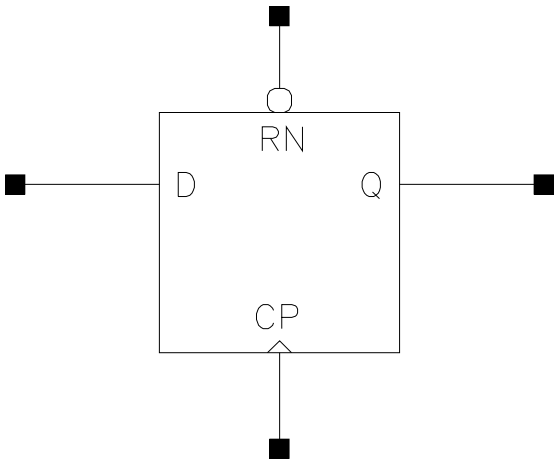
Pin Cycle	X10_P0	X19_P0
Clock 100Mhz Data 0Mhz	1.120e-02	1.121e-02
Clock 100Mhz Data 25Mhz	1.408e-02	1.825e-02
Clock 100Mhz Data 50Mhz	1.697e-02	2.529e-02
Clock = 0 Data 100Mhz	4.660e-03	4.661e-03
Clock = 1 Data 100Mhz	2.959e-05	2.700e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	1.600	1.768	2.8288
X19_P0	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P0	X19_P0
CP	0.0008	0.0008
D	0.0006	0.0006
RN	0.0008	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	X19_P0	X10_P0	X19_P0
CP to Q ↓	0.0324	0.0414	1.2513	0.6490
CP to Q ↑	0.0372	0.0427	1.4727	0.7510
RN to Q ↓	0.0320	0.0363	1.2071	0.6179

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P0	X19_P0
CP ↓	min_pulse_width to CP	0.0293	0.0293
CP ↑	min_pulse_width to CP	0.0271	0.0365
D ↓	hold_rising to CP	0.0200	0.0200
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0101	0.0101
D ↑	setup_rising to CP	0.0119	0.0119
RN ↓	min_pulse_width to RN	0.0425	0.0496
RN ↑	recovery_rising to CP	0.0054	0.0054
RN ↑	removal_rising to CP	-0.0007	-0.0007

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P0	1.656e-03	1.000e-20
X19_P0	2.203e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

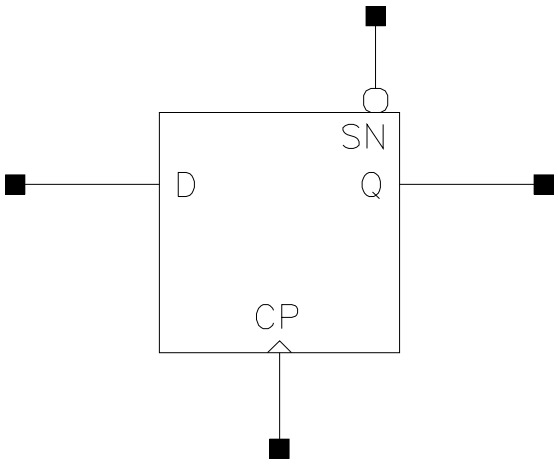
Pin Cycle	X10_P0	X19_P0
Clock 100Mhz Data 0Mhz	1.129e-02	1.129e-02
Clock 100Mhz Data 25Mhz	1.443e-02	1.854e-02
Clock 100Mhz Data 50Mhz	1.756e-02	2.580e-02
Clock = 0 Data 100Mhz	4.653e-03	4.652e-03
Clock = 1 Data 100Mhz	2.918e-05	2.955e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	1.600	1.768	2.8288
X19_P0	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P0	X19_P0
CP	0.0008	0.0008
D	0.0006	0.0006
SN	0.0010	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	X19_P0	X10_P0	X19_P0
CP to Q ↓	0.0307	0.0405	1.2415	0.6448
CP to Q ↑	0.0367	0.0427	1.4676	0.7513
SN to Q ↑	0.0233	0.0268	1.4432	0.7321

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P0	X19_P0
CP ↓	min_pulse_width to CP	0.0294	0.0307
CP ↑	min_pulse_width to CP	0.0271	0.0365
D ↓	hold_rising to CP	0.0201	0.0201
D ↑	hold_rising to CP	0.0152	0.0156
D ↓	setup_rising to CP	0.0096	0.0096
D ↑	setup_rising to CP	0.0129	0.0129
SN ↓	min_pulse_width to SN	0.0256	0.0283
SN ↑	recovery_rising to CP	-0.0043	-0.0043
SN ↑	removal_rising to CP	0.0210	0.0210

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P0	1.545e-03	1.000e-20
X19_P0	1.905e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

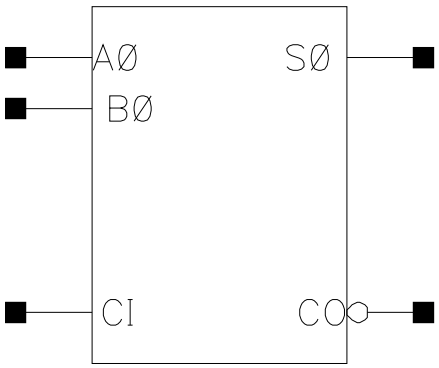
Pin Cycle	X10_P0	X19_P0
Clock 100Mhz Data 0Mhz	1.114e-02	1.115e-02
Clock 100Mhz Data 25Mhz	1.419e-02	1.841e-02
Clock 100Mhz Data 50Mhz	1.725e-02	2.567e-02
Clock = 0 Data 100Mhz	4.529e-03	4.529e-03
Clock = 1 Data 100Mhz	3.350e-05	3.120e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_P0	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_P0	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_P0	1.600	2.720	4.3520
C8T28SOIDV_LLS1_FA1X4_P0	1.600	2.040	3.2640
C8T28SOIDV_LLS1_FA1X9_P0	1.600	3.128	5.0048
C8T28SOIDV_LLS1_FA1X18_P0	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P0	C8T28SOIDV_LL_-FA1X9_P0	C8T28SOIDV_LL_-FA1X14_P0	C8T28SOIDV_LL_-FA1X19_P0
A0	0.0022	0.0023	0.0037	0.0040
B0	0.0019	0.0020	0.0034	0.0036
CI	0.0014	0.0014	0.0024	0.0026
	C8T28SOIDV_LLS1_-FA1X4_P0	C8T28SOIDV_LLS1_-FA1X9_P0	C8T28SOIDV_LLS1_-FA1X18_P0	
A0	0.0021	0.0029	0.0031	
B0	0.0020	0.0032	0.0037	
CI	0.0015	0.0023	0.0027	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P0	**C8T28SOIDV_LL_-FA1X9_P0**	**C8T28SOIDV_LL_-FA1X5_P0**	**C8T28SOIDV_LL_-FA1X9_P0**
A0 to CO ↓	0.0250	0.0273	2.5907	1.3204
A0 to CO ↑	0.0202	0.0223	2.9301	1.5049
A0 to S0 ↓	0.0277	0.0307	2.5577	1.3125
A0 to S0 ↑	0.0289	0.0317	2.9556	1.4824
B0 to CO ↓	0.0256	0.0280	2.5952	1.3246
B0 to CO ↑	0.0213	0.0234	2.9302	1.5061
B0 to S0 ↓	0.0285	0.0316	2.5594	1.3130
B0 to S0 ↑	0.0298	0.0327	2.9562	1.4817
CI to CO ↓	0.0254	0.0277	2.5938	1.3229
CI to CO ↑	0.0214	0.0236	2.9266	1.5035
CI to S0 ↓	0.0285	0.0318	2.5605	1.3137
CI to S0 ↑	0.0301	0.0330	2.9564	1.4820
	C8T28SOIDV_LL_-FA1X14_P0	**C8T28SOIDV_LL_-FA1X19_P0**	**C8T28SOIDV_LL_-FA1X14_P0**	**C8T28SOIDV_LL_-FA1X19_P0**
A0 to CO ↓	0.0258	0.0284	0.8637	0.6548
A0 to CO ↑	0.0210	0.0220	1.0408	0.7757
A0 to S0 ↓	0.0320	0.0327	0.8582	0.6380
A0 to S0 ↑	0.0336	0.0348	1.0008	0.7478
B0 to CO ↓	0.0259	0.0285	0.8654	0.6555
B0 to CO ↑	0.0217	0.0226	1.0402	0.7748
B0 to S0 ↓	0.0327	0.0334	0.8585	0.6383
B0 to S0 ↑	0.0343	0.0355	1.0014	0.7481
CI to CO ↓	0.0257	0.0283	0.8625	0.6536
CI to CO ↑	0.0218	0.0227	1.0392	0.7746
CI to S0 ↓	0.0327	0.0335	0.8591	0.6384
CI to S0 ↑	0.0343	0.0357	1.0012	0.7480
	C8T28SOIDV_-LLS1_FA1X4_P0	**C8T28SOIDV_-LLS1_FA1X9_P0**	**C8T28SOIDV_-LLS1_FA1X4_P0**	**C8T28SOIDV_-LLS1_FA1X9_P0**
A0 to CO ↓	0.0186	0.0163	4.5446	1.5440
A0 to CO ↑	0.0182	0.0162	2.9848	1.4996
A0 to S0 ↓	0.0387	0.0411	2.7237	0.9926
A0 to S0 ↑	0.0368	0.0354	3.0986	1.4699
B0 to CO ↓	0.0173	0.0174	4.5377	1.5454
B0 to CO ↑	0.0141	0.0148	2.9772	1.4995
B0 to S0 ↓	0.0383	0.0430	2.7228	0.9924
B0 to S0 ↑	0.0365	0.0373	3.0970	1.4690
CI to CO ↓	0.0179	0.0253	4.5370	1.5504
CI to CO ↑	0.0146	0.0127	2.9933	1.5121

CI to S0 ↓	0.0222	0.0263	2.7273	0.9942
CI to S0 ↑	0.0190	0.0196	3.1003	1.4690
	C8T28SOIDV_-LLS1_FA1X18_P0		**C8T28SOIDV_-LLS1_FA1X18_P0**	
A0 to CO ↓	0.0215		0.8181	
A0 to CO ↑	0.0164		0.7378	
A0 to S0 ↓	0.0441		0.5125	
A0 to S0 ↑	0.0362		0.7388	
B0 to CO ↓	0.0230		0.8186	
B0 to CO ↑	0.0150		0.7374	
B0 to S0 ↓	0.0453		0.5123	
B0 to S0 ↑	0.0374		0.7389	
CI to CO ↓	0.0314		0.8207	
CI to CO ↑	0.0162		0.7384	
CI to S0 ↓	0.0272		0.5132	
CI to S0 ↑	0.0183		0.7384	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P0	1.184e-03	1.000e-20
C8T28SOIDV_LL_FA1X9_P0	1.620e-03	1.000e-20
C8T28SOIDV_LL_FA1X14_P0	2.438e-03	1.000e-20
C8T28SOIDV_LL_FA1X19_P0	3.031e-03	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P0	2.691e-03	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P0	3.787e-03	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P0	5.745e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P0	C8T28SOIDV_LL_-FA1X9_P0	C8T28SOIDV_LL_-FA1X14_P0	C8T28SOIDV_LL_-FA1X19_P0
A0 to CO	4.143e-03	6.499e-03	1.034e-02	1.318e-02
A0 to S0	4.246e-03	6.426e-03	1.062e-02	1.347e-02
B0 to CO	4.183e-03	6.596e-03	1.044e-02	1.334e-02
B0 to S0	4.218e-03	6.439e-03	1.062e-02	1.346e-02
CI to CO	4.206e-03	6.597e-03	1.056e-02	1.352e-02
CI to S0	4.202e-03	6.434e-03	1.061e-02	1.345e-02
	C8T28SOIDV_LLS1_-FA1X4_P0	C8T28SOIDV_LLS1_-FA1X9_P0	C8T28SOIDV_LLS1_-FA1X18_P0	
A0 to CO	6.296e-03	9.912e-03	1.611e-02	
A0 to S0	8.438e-03	1.265e-02	1.980e-02	
B0 to CO	6.597e-03	9.997e-03	1.617e-02	
B0 to S0	8.962e-03	1.286e-02	2.000e-02	
CI to CO	4.754e-03	8.363e-03	1.500e-02	
CI to S0	5.465e-03	9.415e-03	1.641e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P0	C8T28SOIDV_LL_-FA1X9_P0	C8T28SOIDV_LL_-FA1X14_P0	C8T28SOIDV_LL_-FA1X19_P0
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P0	C8T28SOIDV_LLS1_-FA1X9_P0	C8T28SOIDV_LLS1_-FA1X18_P0	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P0	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P0	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P0	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P0	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P0	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P0	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P0	C8T28SOI_LL_-HA1X9_P0	C8T28SOI_LLS1_-HA1X5_P0	C8T28SOIDV_LL_-HA1X14_P0
A0	0.0007	0.0011	0.0013	0.0015
B0	0.0006	0.0011	0.0012	0.0013
	C8T28SOIDV_LL_-HA1X19_P0	C8T28SOIDV_LLS1_-HA1X11_P0		
A0	0.0018	0.0018		
B0	0.0016	0.0018		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P0	**C8T28SOI_LL_-HA1X9_P0**	**C8T28SOI_LL_-HA1X5_P0**	**C8T28SOI_LL_-HA1X9_P0**
A0 to CO ↓	0.0207	0.0179	2.5743	1.2641
A0 to CO ↑	0.0197	0.0180	3.1383	1.5194
A0 to S0 ↓	0.0257	0.0241	2.4800	1.2532
A0 to S0 ↑	0.0253	0.0241	3.0427	1.5238
B0 to CO ↓	0.0201	0.0175	2.5739	1.2637
B0 to CO ↑	0.0220	0.0202	3.1358	1.5184
B0 to S0 ↓	0.0277	0.0258	2.4791	1.2530
B0 to S0 ↑	0.0247	0.0235	3.0417	1.5234
	C8T28SOI_LLS1_-HA1X5_P0	**C8T28SOIDV_LL_-HA1X14_P0**	**C8T28SOI_LLS1_-HA1X5_P0**	**C8T28SOIDV_LL_-HA1X14_P0**
A0 to CO ↓	0.0166	0.0187	2.5380	0.8624
A0 to CO ↑	0.0156	0.0173	3.1072	1.0223
A0 to S0 ↓	0.0220	0.0263	2.5328	0.8739
A0 to S0 ↑	0.0265	0.0264	3.1275	1.0014
B0 to CO ↓	0.0156	0.0171	2.5379	0.8596
B0 to CO ↑	0.0174	0.0188	3.1036	1.0219
B0 to S0 ↓	0.0240	0.0274	2.5338	0.8732
B0 to S0 ↑	0.0258	0.0251	3.1279	1.0019
	C8T28SOIDV_LL_-HA1X19_P0	**C8T28SOIDV_-LLS1_HA1X11_P0**	**C8T28SOIDV_LL_-HA1X19_P0**	**C8T28SOIDV_-LLS1_HA1X11_P0**
A0 to CO ↓	0.0177	0.0161	0.6382	0.9231
A0 to CO ↑	0.0172	0.0178	0.7779	1.4928
A0 to S0 ↓	0.0246	0.0207	0.6365	0.9357
A0 to S0 ↑	0.0248	0.0233	0.7526	1.5101
B0 to CO ↓	0.0163	0.0149	0.6365	0.9227
B0 to CO ↑	0.0188	0.0197	0.7781	1.4915
B0 to S0 ↓	0.0259	0.0210	0.6361	0.9348
B0 to S0 ↑	0.0235	0.0232	0.7530	1.5092

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_HA1X5_P0	7.107e-04	1.000e-20
C8T28SOI_LL_HA1X9_P0	1.610e-03	1.000e-20
C8T28SOI_LLS1_HA1X5_P0	8.797e-04	1.000e-20
C8T28SOIDV_LL_HA1X14_P0	2.371e-03	1.000e-20
C8T28SOIDV_LL_HA1X19_P0	3.230e-03	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P0	2.031e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

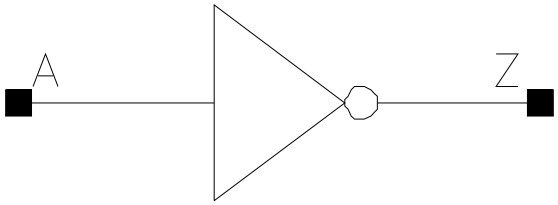
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P0	C8T28SOI_LL_-HA1X9_P0	C8T28SOI_LLS1_-HA1X5_P0	C8T28SOIDV_LL_-HA1X14_P0
A0 to CO	3.180e-03	5.457e-03	3.761e-03	8.606e-03
A0 to S0	3.033e-03	5.527e-03	3.495e-03	8.997e-03
B0 to CO	3.222e-03	5.635e-03	3.797e-03	8.666e-03
B0 to S0	3.007e-03	5.461e-03	3.429e-03	8.866e-03
	C8T28SOIDV_LL_-HA1X19_P0	C8T28SOIDV_LLS1_-HA1X11_P0		
A0 to CO	1.067e-02	7.470e-03		
A0 to S0	1.115e-02	7.080e-03		

B0 to CO	1.072e-02	7.027e-03		
B0 to S0	1.100e-02	7.166e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P0	C8T28SOI_LL_-HA1X9_P0	C8T28SOI_LLS1_-HA1X5_P0	C8T28SOIDV_LL_-HA1X14_P0
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P0	C8T28SOIDV_LLS1_-HA1X11_P0		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P0	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P0	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P0	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P0	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P0	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P0	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P0	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P0	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P0	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P0	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P0	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P0	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P0	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P0	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P0	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P0	C8T28SOI_LL_IVX3_-P0	C8T28SOI_LL_IVX5_-P0	C8T28SOI_LL_-IVX10_P0

A	0.0004	0.0005	0.0006	0.0011
	C8T28SOI_LL_-IVX14_P0	C8T28SOI_LL_-IVX19_P0	C8T28SOI_LL_-IVX29_P0	C8T28SOI_LL_-IVX34_P0
A	0.0017	0.0022	0.0033	0.0039
	C8T28SOI_LL_-IVX38_P0	C8T28SOIDV_LL_-IVX11_P0	C8T28SOIDV_LL_-IVX23_P0	C8T28SOIDV_LL_-IVX34_P0
A	0.0044	0.0012	0.0024	0.0035
	C8T28SOIDV_LL_-IVX46_P0	C8T28SOIDV_LL_-IVX68_P0	C8T28SOIDV_LL_-IVX91_P0	
A	0.0047	0.0071	0.0099	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P0	**C8T28SOI_LL_-IVX3_P0**	**C8T28SOI_LL_-IVX2_P0**	**C8T28SOI_LL_-IVX3_P0**
A to Z ↓	0.0035	0.0034	4.7834	3.7530
A to Z ↑	0.0083	0.0076	5.8004	4.4935
	C8T28SOI_LL_-IVX5_P0	**C8T28SOI_LL_-IVX10_P0**	**C8T28SOI_LL_-IVX5_P0**	**C8T28SOI_LL_-IVX10_P0**
A to Z ↓	0.0032	0.0024	2.6326	1.2640
A to Z ↑	0.0068	0.0056	3.2033	1.5248
	C8T28SOI_LL_-IVX14_P0	**C8T28SOI_LL_-IVX19_P0**	**C8T28SOI_LL_-IVX14_P0**	**C8T28SOI_LL_-IVX19_P0**
A to Z ↓	0.0027	0.0029	0.8764	0.6674
A to Z ↑	0.0055	0.0057	1.0283	0.7910
	C8T28SOI_LL_-IVX29_P0	**C8T28SOI_LL_-IVX34_P0**	**C8T28SOI_LL_-IVX29_P0**	**C8T28SOI_LL_-IVX34_P0**
A to Z ↓	0.0030	0.0027	0.4460	0.3801
A to Z ↑	0.0056	0.0053	0.5239	0.4470
	C8T28SOI_LL_-IVX38_P0	**C8T28SOIDV_LL_-IVX11_P0**	**C8T28SOI_LL_-IVX38_P0**	**C8T28SOIDV_LL_-IVX11_P0**
A to Z ↓	0.0029	0.0020	0.3369	1.0206
A to Z ↑	0.0054	0.0070	0.3971	1.5372
	C8T28SOIDV_LL_-IVX23_P0	**C8T28SOIDV_LL_-IVX34_P0**	**C8T28SOIDV_LL_-IVX23_P0**	**C8T28SOIDV_LL_-IVX34_P0**
A to Z ↓	0.0015	0.0019	0.4976	0.3401
A to Z ↑	0.0064	0.0064	0.7498	0.5039
	C8T28SOIDV_LL_-IVX46_P0	**C8T28SOIDV_LL_-IVX68_P0**	**C8T28SOIDV_LL_-IVX46_P0**	**C8T28SOIDV_LL_-IVX68_P0**
A to Z ↓	0.0019	0.0019	0.2558	0.1741
A to Z ↑	0.0063	0.0061	0.3779	0.2544
	C8T28SOIDV_LL_-IVX91_P0		**C8T28SOIDV_LL_-IVX91_P0**	
A to Z ↓	0.0024		0.1351	
A to Z ↑	0.0065		0.1940	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_IVX2_P0	9.571e-05	1.000e-20
C8T28SOI_LL_IVX3_P0	1.361e-04	1.000e-20
C8T28SOI_LL_IVX5_P0	1.985e-04	1.000e-20
C8T28SOI_LL_IVX10_P0	4.292e-04	1.000e-20

C8T28SOI_LL_IVX14_P0	6.182e-04	1.000e-20
C8T28SOI_LL_IVX19_P0	8.057e-04	1.000e-20
C8T28SOI_LL_IVX29_P0	1.181e-03	1.000e-20
C8T28SOI_LL_IVX34_P0	1.369e-03	1.000e-20
C8T28SOI_LL_IVX38_P0	1.557e-03	1.000e-20
C8T28SOIDV_LL_IVX11_P0	4.609e-04	1.000e-20
C8T28SOIDV_LL_IVX23_P0	9.412e-04	1.000e-20
C8T28SOIDV_LL_IVX34_P0	1.372e-03	1.000e-20
C8T28SOIDV_LL_IVX46_P0	1.799e-03	1.000e-20
C8T28SOIDV_LL_IVX68_P0	2.651e-03	1.000e-20
C8T28SOIDV_LL_IVX91_P0	3.504e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P0	C8T28SOI_LL_IVX3_-P0	C8T28SOI_LL_IVX5_-P0	C8T28SOI_LL_-IVX10_P0
A to Z	1.060e-03	1.342e-03	1.794e-03	3.695e-03
	C8T28SOI_LL_-IVX14_P0	C8T28SOI_LL_-IVX19_P0	C8T28SOI_LL_-IVX29_P0	C8T28SOI_LL_-IVX34_P0
A to Z	5.469e-03	7.187e-03	1.065e-02	1.231e-02
	C8T28SOI_LL_-IVX38_P0	C8T28SOIDV_LL_-IVX11_P0	C8T28SOIDV_LL_-IVX23_P0	C8T28SOIDV_LL_-IVX34_P0
A to Z	1.402e-02	4.050e-03	8.079e-03	1.195e-02
	C8T28SOIDV_LL_-IVX46_P0	C8T28SOIDV_LL_-IVX68_P0	C8T28SOIDV_LL_-IVX91_P0	
A to Z	1.575e-02	2.321e-02	3.116e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

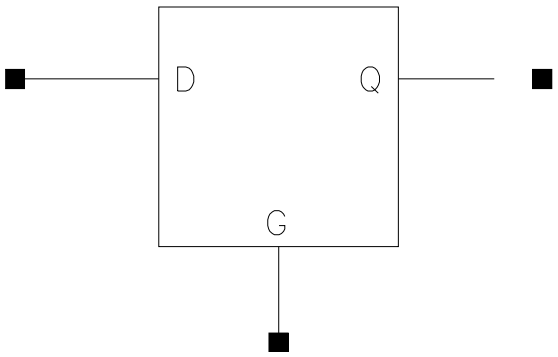
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P0	C8T28SOI_LL_IVX3_-P0	C8T28SOI_LL_IVX5_-P0	C8T28SOI_LL_-IVX10_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P0	C8T28SOI_LL_-IVX19_P0	C8T28SOI_LL_-IVX29_P0	C8T28SOI_LL_-IVX34_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P0	C8T28SOIDV_LL_-IVX11_P0	C8T28SOIDV_LL_-IVX23_P0	C8T28SOIDV_LL_-IVX34_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P0	C8T28SOIDV_LL_-IVX68_P0	C8T28SOIDV_LL_-IVX91_P0	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.360	1.0880
X9_P0	1.600	0.952	1.5232
X19_P0	1.600	1.224	1.9584
X28_P0	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0	X28_P0
D	0.0004	0.0007	0.0009	0.0016
G	0.0009	0.0009	0.0017	0.0017

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D to Q ↓	0.0286	0.0281	2.5730	1.3289
D to Q ↑	0.0170	0.0205	3.0467	1.4713
G to Q ↓	0.0295	0.0300	2.5682	1.3265

G to Q ↑	0.0169	0.0194	3.0497	1.4731
	X19_P0	**X28_P0**	**X19_P0**	**X28_P0**
D to Q ↓	0.0226	0.0231	0.6381	0.4306
D to Q ↑	0.0188	0.0188	0.7475	0.5027
G to Q ↓	0.0256	0.0230	0.6361	0.4292
G to Q ↑	0.0162	0.0161	0.7472	0.5023

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P0	X9_P0	X19_P0	X28_P0
D ↓	hold_falling to G	0.0048	0.0048	0.0122	0.0128
D ↑	hold_falling to G	0.0136	0.0115	0.0138	0.0106
D ↓	setup_falling to G	0.0266	0.0242	0.0193	0.0193
D ↑	setup_falling to G	0.0215	0.0231	0.0240	0.0234
G ↑	min_pulse_width to G	0.0237	0.0271	0.0224	0.0224

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	5.008e-04	1.000e-20
X9_P0	8.478e-04	1.000e-20
X19_P0	1.439e-03	1.000e-20
X28_P0	1.993e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	1.543e-05	3.870e-05	4.684e-05	1.137e-04
G (output stable)	1.483e-03	1.821e-03	2.991e-03	2.947e-03
D to Q	5.232e-03	8.457e-03	1.313e-02	1.864e-02
G to Q	5.281e-03	8.401e-03	1.258e-02	1.695e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

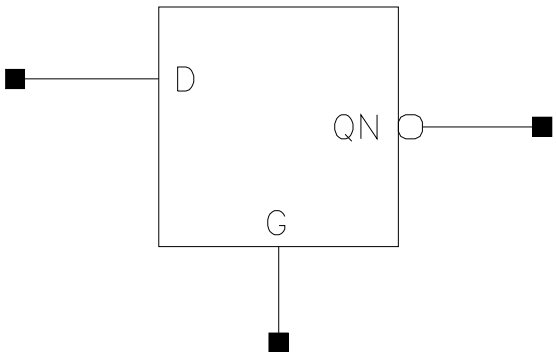
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P0
D	0.0004
G	0.0009

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P0	X10_P0
D to QN ↓	0.0252	1.2159
D to QN ↑	0.0344	1.4785
G to QN ↓	0.0249	1.2159
G to QN ↑	0.0356	1.4787

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P0
D ↓	hold_falling to G	0.0004
D ↑	hold_falling to G	0.0088
D ↓	setup_falling to G	0.0267
D ↑	setup_falling to G	0.0161
G ↑	min_pulse_width to G	0.0236

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P0	7.869e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X10_P0
D (output stable)	1.527e-05
G (output stable)	1.802e-03
D to QN	6.375e-03
G to QN	6.635e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

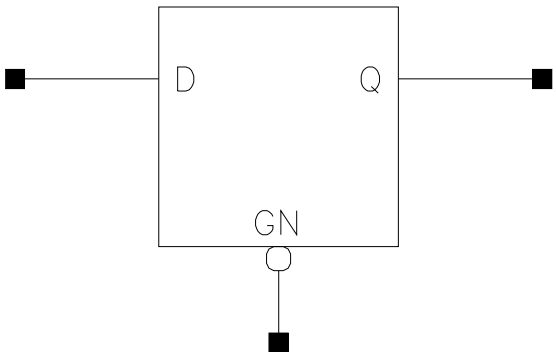
Pin Cycle (vdds)	X10_P0
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.360	1.0880
X9_P0	1.600	0.952	1.5232
X19_P0	1.600	1.224	1.9584
X28_P0	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0	X28_P0
D	0.0004	0.0007	0.0009	0.0014
GN	0.0008	0.0009	0.0013	0.0017

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D to Q ↓	0.0289	0.0278	2.5765	1.3303
D to Q ↑	0.0170	0.0205	3.0447	1.4731
GN to Q ↓	0.0271	0.0271	2.5801	1.3314

GN to Q ↑	0.0301	0.0289	3.0432	1.4671
	X19_P0	**X28_P0**	**X19_P0**	**X28_P0**
D to Q ↓	0.0230	0.0224	0.6345	0.4288
D to Q ↑	0.0196	0.0192	0.7383	0.4956
GN to Q ↓	0.0200	0.0189	0.6343	0.4290
GN to Q ↑	0.0265	0.0262	0.7364	0.4945

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P0	X9_P0	X19_P0	X28_P0
D ↓	hold_rising to GN	0.0019	0.0068	0.0090	0.0090
D ↑	hold_rising to GN	0.0148	0.0127	0.0128	0.0154
D ↓	setup_rising to GN	0.0350	0.0302	0.0286	0.0254
D ↑	setup_rising to GN	0.0146	0.0195	0.0195	0.0168
GN ↓	min_pulse_width to GN	0.0381	0.0345	0.0271	0.0263

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	5.101e-04	1.000e-20
X9_P0	8.832e-04	1.000e-20
X19_P0	1.592e-03	1.000e-20
X28_P0	2.124e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	1.452e-05	2.634e-05	5.059e-05	1.025e-04
GN (output stable)	1.470e-03	1.802e-03	2.710e-03	2.751e-03
D to Q	5.247e-03	8.519e-03	1.357e-02	1.852e-02
GN to Q	7.348e-03	1.076e-02	1.625e-02	2.063e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

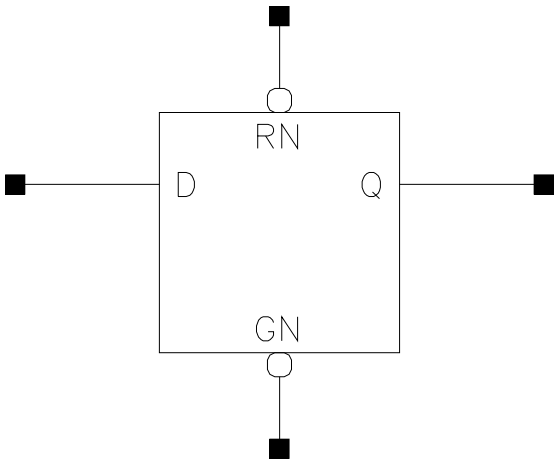
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0	X28_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.632	1.3056
X9_P0	1.600	1.224	1.9584
X19_P0	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0
D	0.0004	0.0006	0.0012
GN	0.0010	0.0010	0.0014
RN	0.0004	0.0005	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D to Q ↓	0.0290	0.0281	2.5238	1.2876

D to Q ↑	0.0293	0.0321	3.1387	1.5208
GN to Q ↓	0.0278	0.0265	2.5256	1.2885
GN to Q ↑	0.0391	0.0369	3.1352	1.5216
RN to Q ↓	0.0246	0.0302	2.4156	1.2539
RN to Q ↑	0.0301	0.0331	3.1382	1.5224
	X19_P0		**X19_P0**	
D to Q ↓	0.0230		0.6400	
D to Q ↑	0.0350		0.7681	
GN to Q ↓	0.0206		0.6402	
GN to Q ↑	0.0359		0.7696	
RN to Q ↓	0.0370		0.6413	
RN to Q ↑	0.0381		0.7706	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P0	X9_P0	X19_P0
D ↓	hold_rising to GN	0.0041	0.0041	0.0088
D ↑	hold_rising to GN	0.0058	0.0032	0.0010
D ↓	setup_rising to GN	0.0326	0.0336	0.0263
D ↑	setup_rising to GN	0.0287	0.0339	0.0387
GN ↓	min_pulse_width to GN	0.0400	0.0389	0.0403
RN ↓	min_pulse_width to RN	0.0305	0.0354	0.0474
RN ↑	recovery_rising to GN	0.0318	0.0340	0.0411
RN ↑	removal_rising to GN	-0.0169	-0.0164	-0.0239

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	5.944e-04	1.000e-20
X9_P0	9.640e-04	1.000e-20
X19_P0	1.672e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0
D (output stable)	5.815e-05	3.968e-05	7.157e-05
GN (output stable)	1.585e-03	1.781e-03	2.351e-03
RN (output stable)	4.870e-05	6.135e-05	8.024e-05
D to Q	6.640e-03	9.763e-03	1.601e-02
GN to Q	8.955e-03	1.211e-02	1.867e-02
RN to Q	4.556e-03	6.901e-03	1.241e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

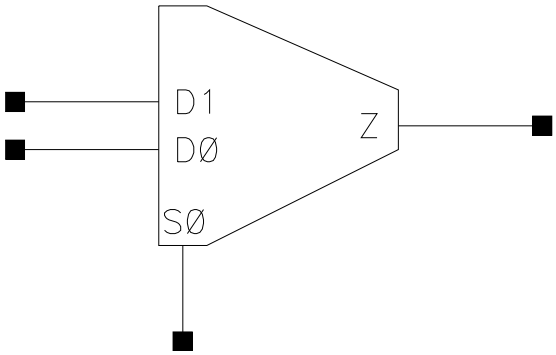
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.360	1.0880
X9_P0	0.800	1.496	1.1968
X14_P0	0.800	2.176	1.7408
X19_P0	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P0	X9_P0	X14_P0	X19_P0
D0	0.0006	0.0007	0.0009	0.0012
D1	0.0005	0.0007	0.0010	0.0012
S0	0.0010	0.0009	0.0012	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X9_P0	X5_P0	X9_P0
D0 to Z ↓	0.0221	0.0211	2.5944	1.3110
D0 to Z ↑	0.0183	0.0184	3.1122	1.5842
D1 to Z ↓	0.0223	0.0204	2.5927	1.3076
D1 to Z ↑	0.0181	0.0175	3.1169	1.5803
S0 to Z ↓	0.0211	0.0189	2.5865	1.3051
S0 to Z ↑	0.0201	0.0188	3.1143	1.5828

	X14_P0	X19_P0	X14_P0	X19_P0
D0 to Z ↓	0.0228	0.0204	0.8997	0.6513
D0 to Z ↑	0.0190	0.0179	1.0709	0.7758
D1 to Z ↓	0.0229	0.0208	0.8995	0.6522
D1 to Z ↑	0.0185	0.0176	1.0679	0.7753
S0 to Z ↓	0.0224	0.0210	0.8966	0.6503
S0 to Z ↑	0.0217	0.0201	1.0689	0.7751

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	6.148e-04	1.000e-20
X9_P0	1.099e-03	1.000e-20
X14_P0	1.483e-03	1.000e-20
X19_P0	2.143e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X9_P0	X14_P0	X19_P0
D0 (output stable)	1.396e-03	2.278e-03	2.895e-03	3.954e-03
D1 (output stable)	1.331e-03	2.072e-03	2.926e-03	4.004e-03
S0 (output stable)	1.565e-03	1.498e-03	2.048e-03	2.630e-03
D0 to Z	3.789e-03	6.391e-03	9.963e-03	1.264e-02
D1 to Z	3.731e-03	6.026e-03	9.762e-03	1.257e-02
S0 to Z	4.647e-03	6.353e-03	1.069e-02	1.328e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

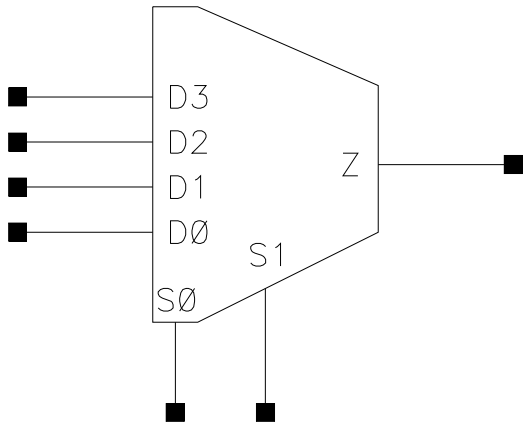
Pin Cycle (vdds)	X5_P0	X9_P0	X14_P0	X19_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.600	1.496	2.3936
X9_P0	1.600	1.768	2.8288
X13_P0	1.600	2.312	3.6992
X18_P0	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P0	X9_P0	X13_P0	X18_P0
D0	0.0005	0.0007	0.0010	0.0010
D1	0.0004	0.0005	0.0010	0.0010
D2	0.0004	0.0007	0.0010	0.0010
D3	0.0004	0.0006	0.0010	0.0010
S0	0.0013	0.0017	0.0022	0.0022
S1	0.0007	0.0008	0.0012	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X9_P0**	**X4_P0**	**X9_P0**
D0 to Z ↓	0.0442	0.0374	2.7614	1.3587
D0 to Z ↑	0.0306	0.0287	3.1825	1.5786
D1 to Z ↓	0.0435	0.0372	2.7587	1.3596
D1 to Z ↑	0.0304	0.0284	3.1779	1.5783
D2 to Z ↓	0.0401	0.0378	2.7246	1.3620
D2 to Z ↑	0.0293	0.0283	3.1606	1.5758
D3 to Z ↓	0.0406	0.0371	2.7291	1.3612
D3 to Z ↑	0.0297	0.0283	3.1606	1.5756
S0 to Z ↓	0.0456	0.0410	2.7439	1.3594
S0 to Z ↑	0.0355	0.0344	3.1793	1.5805
S1 to Z ↓	0.0315	0.0300	2.7410	1.3598
S1 to Z ↑	0.0285	0.0282	3.1722	1.5768
	X13_P0	**X18_P0**	**X13_P0**	**X18_P0**
D0 to Z ↓	0.0378	0.0413	0.9577	0.7153
D0 to Z ↑	0.0254	0.0277	1.0607	0.8011
D1 to Z ↓	0.0380	0.0415	0.9588	0.7156
D1 to Z ↑	0.0261	0.0285	1.0613	0.8010
D2 to Z ↓	0.0338	0.0368	0.9423	0.7028
D2 to Z ↑	0.0256	0.0279	1.0565	0.7986
D3 to Z ↓	0.0336	0.0365	0.9419	0.7027
D3 to Z ↑	0.0258	0.0281	1.0563	0.7986
S0 to Z ↓	0.0400	0.0431	0.9499	0.7092
S0 to Z ↑	0.0313	0.0336	1.0611	0.8016
S1 to Z ↓	0.0301	0.0333	0.9496	0.7092
S1 to Z ↑	0.0254	0.0277	1.0592	0.8002

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	6.003e-04	1.000e-20
X9_P0	9.766e-04	1.000e-20
X13_P0	1.658e-03	1.000e-20
X18_P0	1.868e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X9_P0	X13_P0	X18_P0
D0 (output stable)	5.613e-05	6.419e-05	1.244e-04	1.258e-04
D1 (output stable)	7.690e-05	7.964e-05	1.167e-04	1.180e-04
D2 (output stable)	6.933e-05	8.150e-05	1.157e-04	1.173e-04
D3 (output stable)	5.859e-05	8.064e-05	1.079e-04	1.084e-04
S0 (output stable)	1.809e-03	2.050e-03	3.280e-03	3.282e-03
S1 (output stable)	2.137e-03	2.301e-03	3.658e-03	3.679e-03
D0 to Z	4.827e-03	7.680e-03	1.200e-02	1.573e-02
D1 to Z	4.761e-03	7.659e-03	1.211e-02	1.586e-02
D2 to Z	4.510e-03	7.673e-03	1.132e-02	1.473e-02
D3 to Z	4.561e-03	7.668e-03	1.131e-02	1.471e-02
S0 to Z	6.591e-03	9.805e-03	1.508e-02	1.867e-02
S1 to Z	5.885e-03	8.735e-03	1.338e-02	1.691e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

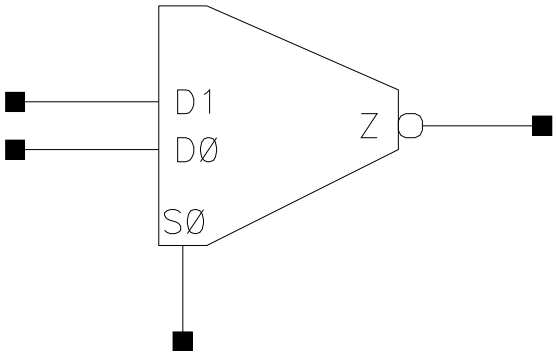
Pin Cycle (vdds)	X4_P0	X9_P0	X13_P0	X18_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P0	0.800	0.952	0.7616
X2_P0	0.800	0.952	0.7616
X6_P0	0.800	1.904	1.5232
X9_P0	0.800	2.448	1.9584
X12_P0	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P0	X2_P0	X6_P0	X9_P0
D0	0.0004	0.0005	0.0011	0.0017
D1	0.0004	0.0005	0.0011	0.0017
S0	0.0009	0.0013	0.0017	0.0025
	X12_P0			
D0	0.0022			
D1	0.0022			
S0	0.0029			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P0	**X2_P0**	**X1_P0**	**X2_P0**
D0 to Z ↓	0.0067	0.0064	6.7031	4.6231

D0 to Z ↑	0.0151	0.0119	11.8931	6.7170
D1 to Z ↓	0.0064	0.0063	6.6374	4.5126
D1 to Z ↑	0.0153	0.0116	11.9377	6.8806
S0 to Z ↓	0.0137	0.0101	6.6282	4.5490
S0 to Z ↑	0.0159	0.0112	11.9158	6.7949
	X6_P0	**X9_P0**	**X6_P0**	**X9_P0**
D0 to Z ↓	0.0078	0.0070	2.1000	1.4131
D0 to Z ↑	0.0120	0.0115	2.8665	2.0095
D1 to Z ↓	0.0073	0.0072	2.0613	1.4191
D1 to Z ↑	0.0126	0.0116	2.9645	1.9642
S0 to Z ↓	0.0120	0.0102	2.0740	1.4139
S0 to Z ↑	0.0129	0.0115	2.9160	1.9901
	X12_P0		**X12_P0**	
D0 to Z ↓	0.0073		1.0816	
D0 to Z ↑	0.0115		1.5169	
D1 to Z ↓	0.0072		1.0756	
D1 to Z ↑	0.0115		1.4828	
S0 to Z ↓	0.0111		1.0764	
S0 to Z ↑	0.0121		1.5024	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X1_P0	2.026e-04	1.000e-20
X2_P0	4.303e-04	1.000e-20
X6_P0	8.399e-04	1.000e-20
X9_P0	1.318e-03	1.000e-20
X12_P0	1.593e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X1_P0	X2_P0	X6_P0	X9_P0
D0 (output stable)	1.421e-05	3.095e-05	8.834e-05	1.265e-04
D1 (output stable)	1.396e-05	3.198e-05	9.736e-05	1.399e-04
S0 (output stable)	1.495e-03	2.063e-03	2.911e-03	5.067e-03
D0 to Z	1.214e-03	1.725e-03	4.254e-03	5.983e-03
D1 to Z	1.219e-03	1.695e-03	4.225e-03	6.002e-03
S0 to Z	2.445e-03	3.221e-03	5.886e-03	9.085e-03
	X12_P0			
D0 (output stable)	1.694e-04			
D1 (output stable)	1.772e-04			
S0 (output stable)	5.455e-03			
D0 to Z	8.009e-03			
D1 to Z	7.981e-03			
S0 to Z	1.090e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X1_P0	X2_P0	X6_P0	X9_P0
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

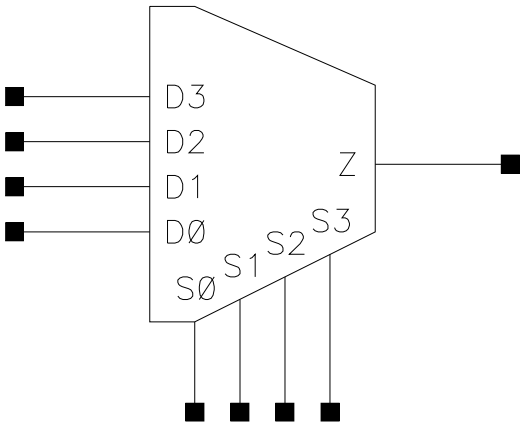
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P0			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.600	0.952	1.5232
X15_P0	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P0	X15_P0
D0	0.0006	0.0014
D1	0.0006	0.0012
D2	0.0006	0.0014
D3	0.0005	0.0012
S0	0.0006	0.0013
S1	0.0006	0.0014
S2	0.0006	0.0013
S3	0.0006	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X15_P0	X4_P0	X15_P0
D0 to Z ↓	0.0235	0.0253	3.9586	1.0422
D0 to Z ↑	0.0213	0.0207	2.9245	0.7432
D1 to Z ↓	0.0232	0.0247	3.9554	1.0411
D1 to Z ↑	0.0180	0.0177	2.9104	0.7389
D2 to Z ↓	0.0233	0.0254	3.9577	1.0415
D2 to Z ↑	0.0208	0.0199	2.9372	0.7466
D3 to Z ↓	0.0228	0.0249	3.9526	1.0398
D3 to Z ↑	0.0176	0.0172	2.9209	0.7419
S0 to Z ↓	0.0222	0.0231	3.9576	1.0413
S0 to Z ↑	0.0235	0.0220	2.9218	0.7416
S1 to Z ↓	0.0216	0.0228	3.9546	1.0399
S1 to Z ↑	0.0199	0.0191	2.9079	0.7384
S2 to Z ↓	0.0224	0.0233	3.9582	1.0402
S2 to Z ↑	0.0230	0.0214	2.9336	0.7456
S3 to Z ↓	0.0221	0.0228	3.9532	1.0387
S3 to Z ↑	0.0197	0.0184	2.9207	0.7411

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	7.708e-04	1.000e-20
X15_P0	2.214e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X15_P0
D0 (output stable)	5.584e-04	1.498e-03
D1 (output stable)	5.031e-04	1.325e-03
D2 (output stable)	5.492e-04	1.462e-03
D3 (output stable)	4.969e-04	1.297e-03
S0 (output stable)	5.341e-04	1.452e-03
S1 (output stable)	4.823e-04	1.306e-03
S2 (output stable)	5.326e-04	1.431e-03
S3 (output stable)	4.806e-04	1.285e-03
D0 to Z	4.349e-03	1.318e-02
D1 to Z	3.880e-03	1.189e-02
D2 to Z	4.131e-03	1.245e-02
D3 to Z	3.691e-03	1.120e-02
S0 to Z	4.224e-03	1.264e-02
S1 to Z	3.761e-03	1.141e-02
S2 to Z	4.035e-03	1.195e-02
S3 to Z	3.599e-03	1.068e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

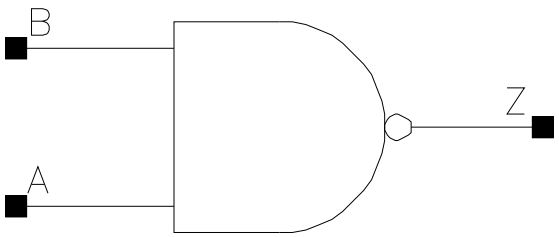
Pin Cycle (vdds)	X4_P0	X15_P0
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P0	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P0	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P0	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P0	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P0	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P0	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P0	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P0	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P0	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P0	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P0	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P0	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P0	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P0	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P0	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P0	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P0	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P0	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P0	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P0	C8T28SOI_LL_-NAND2X4_P0	C8T28SOI_LL_-NAND2X8_P0	C8T28SOI_LL_-NAND2X12_P0
A	0.0004	0.0005	0.0011	0.0017
B	0.0004	0.0005	0.0011	0.0016
	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X24_P0	C8T28SOI_-LLBR0P8_-NAND2X4_P0
A	0.0022	0.0028	0.0007	0.0007
B	0.0021	0.0027	0.0007	0.0006
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	C8T28SOI_-LLBR0P8_-NAND2X12_P0	C8T28SOI_-LLBR0P8_-NAND2X16_P0	C8T28SOI_LLS_-NAND2X8_P0
A	0.0011	0.0017	0.0023	0.0011
B	0.0010	0.0016	0.0020	0.0010
	C8T28SOI_LLS_-NAND2X15_P0	C8T28SOI_LLS_-NAND2X23_P0	C8T28SOI_LLS_-NAND2X31_P0	C8T28SOIDV_LL_-NAND2X9_P0
A	0.0023	0.0035	0.0046	0.0011
B	0.0021	0.0033	0.0043	0.0012
	C8T28SOIDV_LL_-NAND2X18_P0	C8T28SOIDV_LL_-NAND2X27_P0	C8T28SOIDV_LL_-NAND2X36_P0	
A	0.0023	0.0035	0.0047	
B	0.0022	0.0034	0.0045	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND2X2_P0	**C8T28SOI_LL_-NAND2X4_P0**	**C8T28SOI_LL_-NAND2X2_P0**	**C8T28SOI_LL_-NAND2X4_P0**
A to Z ↓	0.0056	0.0051	7.1078	4.0003
A to Z ↑	0.0092	0.0077	5.7627	3.1891
B to Z ↓	0.0073	0.0064	7.1882	4.0438
B to Z ↑	0.0081	0.0063	5.8107	3.2535
	C8T28SOI_LL_-NAND2X8_P0	**C8T28SOI_LL_-NAND2X12_P0**	**C8T28SOI_LL_-NAND2X8_P0**	**C8T28SOI_LL_-NAND2X12_P0**
A to Z ↓	0.0056	0.0054	2.0418	1.3973
A to Z ↑	0.0075	0.0073	1.5281	1.0469
B to Z ↓	0.0063	0.0066	2.0607	1.4124
B to Z ↑	0.0052	0.0055	1.5441	1.0663

	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0
A to Z ↓	0.0055	0.0055	1.0597	0.8559
A to Z ↑	0.0073	0.0073	0.7900	0.6408
B to Z ↓	0.0064	0.0067	1.0714	0.8659
B to Z ↑	0.0051	0.0054	0.8024	0.6525
	C8T28SOI_LL_-NAND2X24_P0	**C8T28SOI_-LLBR0P8_-NAND2X4_P0**	**C8T28SOI_LL_-NAND2X24_P0**	**C8T28SOI_-LLBR0P8_-NAND2X4_P0**
A to Z ↓	0.0222	0.0025	0.5082	2.8810
A to Z ↑	0.0226	0.0111	0.6214	3.9689
B to Z ↓	0.0237	0.0034	0.5084	2.9286
B to Z ↑	0.0215	0.0092	0.6214	3.9800
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	**C8T28SOI_-LLBR0P8_-NAND2X12_P0**	**C8T28SOI_-LLBR0P8_-NAND2X8_P0**	**C8T28SOI_-LLBR0P8_-NAND2X12_P0**
A to Z ↓	0.0029	0.0029	1.5945	1.0885
A to Z ↑	0.0108	0.0108	2.0067	1.3625
B to Z ↓	0.0031	0.0036	1.6202	1.1077
B to Z ↑	0.0080	0.0083	2.0274	1.3753
	C8T28SOI_-LLBR0P8_-NAND2X16_P0	**C8T28SOI_LLS_-NAND2X8_P0**	**C8T28SOI_-LLBR0P8_-NAND2X16_P0**	**C8T28SOI_LLS_-NAND2X8_P0**
A to Z ↓	0.0027	0.0055	0.8325	2.0367
A to Z ↑	0.0104	0.0076	1.0197	1.5506
B to Z ↓	0.0031	0.0062	0.8467	2.0566
B to Z ↑	0.0076	0.0054	1.0339	1.5824
	C8T28SOI_LLS_-NAND2X15_P0	**C8T28SOI_LLS_-NAND2X23_P0**	**C8T28SOI_LLS_-NAND2X15_P0**	**C8T28SOI_LLS_-NAND2X23_P0**
A to Z ↓	0.0055	0.0056	1.0575	0.7138
A to Z ↑	0.0073	0.0072	0.7761	0.5178
B to Z ↓	0.0065	0.0067	1.0688	0.7217
B to Z ↑	0.0051	0.0051	0.7838	0.5235
	C8T28SOI_LLS_-NAND2X31_P0	**C8T28SOIDV_LL_-NAND2X9_P0**	**C8T28SOI_LLS_-NAND2X31_P0**	**C8T28SOIDV_LL_-NAND2X9_P0**
A to Z ↓	0.0056	0.0045	0.5407	1.5877
A to Z ↑	0.0072	0.0083	0.3903	1.4756
B to Z ↓	0.0068	0.0055	0.5467	1.6070
B to Z ↑	0.0051	0.0068	0.3945	1.5116
	C8T28SOIDV_LL_-NAND2X18_P0	**C8T28SOIDV_LL_-NAND2X27_P0**	**C8T28SOIDV_LL_-NAND2X18_P0**	**C8T28SOIDV_LL_-NAND2X27_P0**
A to Z ↓	0.0046	0.0048	0.8115	0.5520
A to Z ↑	0.0085	0.0085	0.7449	0.5043
B to Z ↓	0.0052	0.0058	0.8206	0.5592
B to Z ↑	0.0062	0.0065	0.7522	0.5095
	C8T28SOIDV_LL_-NAND2X36_P0		**C8T28SOIDV_LL_-NAND2X36_P0**	
A to Z ↓	0.0046		0.4160	
A to Z ↑	0.0084		0.3776	
B to Z ↓	0.0054		0.4212	
B to Z ↑	0.0060		0.3820	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P0	9.388e-05	1.000e-20
C8T28SOI_LL_NAND2X4_P0	2.064e-04	1.000e-20
C8T28SOI_LL_NAND2X8_P0	4.212e-04	1.000e-20
C8T28SOI_LL_NAND2X12_P0	6.096e-04	1.000e-20
C8T28SOI_LL_NAND2X15_P0	7.983e-04	1.000e-20
C8T28SOI_LL_NAND2X19_P0	9.870e-04	1.000e-20
C8T28SOI_LL_NAND2X24_P0	1.449e-03	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P0	1.804e-04	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P0	3.302e-04	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_P0	4.729e-04	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_P0	6.159e-04	1.000e-20
C8T28SOI_LLS_NAND2X8_P0	4.211e-04	1.000e-20
C8T28SOI_LLS_NAND2X15_P0	7.985e-04	1.000e-20
C8T28SOI_LLS_NAND2X23_P0	1.176e-03	1.000e-20
C8T28SOI_LLS_NAND2X31_P0	1.554e-03	1.000e-20
C8T28SOIDV_LL_NAND2X9_P0	4.760e-04	1.000e-20
C8T28SOIDV_LL_NAND2X18_P0	9.230e-04	1.000e-20
C8T28SOIDV_LL_NAND2X27_P0	1.352e-03	1.000e-20
C8T28SOIDV_LL_NAND2X36_P0	1.782e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P0	C8T28SOI_LL_-NAND2X4_P0	C8T28SOI_LL_-NAND2X8_P0	C8T28SOI_LL_-NAND2X12_P0
A (output stable)	1.103e-05	1.861e-05	7.938e-05	9.841e-05
B (output stable)	1.543e-05	2.846e-05	1.980e-04	2.032e-04
A to Z	1.085e-03	1.852e-03	3.795e-03	5.565e-03
B to Z	9.920e-04	1.657e-03	3.358e-03	4.973e-03
	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X24_P0	C8T28SOI_-LLBR0P8_-NAND2X4_P0
A (output stable)	1.450e-04	1.625e-04	2.318e-05	2.691e-05
B (output stable)	3.404e-04	3.188e-04	3.836e-05	4.004e-05
A to Z	7.357e-03	9.139e-03	1.167e-02	1.891e-03
B to Z	6.503e-03	8.138e-03	1.155e-02	1.736e-03
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	C8T28SOI_-LLBR0P8_-NAND2X12_P0	C8T28SOI_-LLBR0P8_-NAND2X16_P0	C8T28SOI_LLS_-NAND2X8_P0
A (output stable)	9.600e-05	1.170e-04	1.789e-04	8.028e-05
B (output stable)	2.356e-04	2.423e-04	4.065e-04	2.065e-04
A to Z	3.694e-03	5.491e-03	7.107e-03	3.791e-03
B to Z	3.188e-03	4.808e-03	6.155e-03	3.349e-03
	C8T28SOI_LLS_-NAND2X15_P0	C8T28SOI_LLS_-NAND2X23_P0	C8T28SOI_LLS_-NAND2X31_P0	C8T28SOIDV_LL_-NAND2X9_P0
A (output stable)	1.524e-04	2.203e-04	2.855e-04	4.721e-05
B (output stable)	3.547e-04	4.740e-04	5.967e-04	7.167e-05
A to Z	7.449e-03	1.109e-02	1.470e-02	4.230e-03
B to Z	6.564e-03	9.780e-03	1.295e-02	3.844e-03
	C8T28SOIDV_LL_-NAND2X18_P0	C8T28SOIDV_LL_-NAND2X27_P0	C8T28SOIDV_LL_-NAND2X36_P0	
A (output stable)	1.741e-04	2.060e-04	3.448e-04	
B (output stable)	4.699e-04	3.896e-04	8.931e-04	
A to Z	8.413e-03	1.251e-02	1.652e-02	

B to Z	7.473e-03	1.125e-02	1.461e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

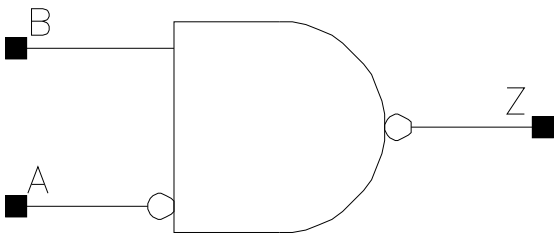
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P0	C8T28SOI_LL_-NAND2X4_P0	C8T28SOI_LL_-NAND2X8_P0	C8T28SOI_LL_-NAND2X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P0	C8T28SOI_LL_-NAND2X19_P0	C8T28SOI_LL_-NAND2X24_P0	C8T28SOI_-LLBR0P8_-NAND2X4_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P0	C8T28SOI_-LLBR0P8_-NAND2X12_P0	C8T28SOI_-LLBR0P8_-NAND2X16_P0	C8T28SOI_LLS_-NAND2X8_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P0	C8T28SOI_LLS_-NAND2X23_P0	C8T28SOI_LLS_-NAND2X31_P0	C8T28SOIDV_LL_-NAND2X9_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P0	C8T28SOIDV_LL_-NAND2X27_P0	C8T28SOIDV_LL_-NAND2X36_P0	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.544	0.4352
X4_P0	0.800	0.680	0.5440
X9_P0	1.600	0.544	0.8704
X13_P0	1.600	0.816	1.3056
X17_P0	1.600	0.816	1.3056
X23_P0	0.800	2.312	1.8496
X27_P0	1.600	1.088	1.7408
X31_P0	0.800	2.992	2.3936
X36_P0	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P0	X4_P0	X9_P0	X13_P0
A	0.0005	0.0006	0.0009	0.0009
B	0.0004	0.0005	0.0011	0.0018
	X17_P0	X23_P0	X27_P0	X31_P0
A	0.0009	0.0019	0.0015	0.0025
B	0.0022	0.0032	0.0034	0.0042
	X36_P0			
A	0.0014			
B	0.0045			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X4_P0**	**X2_P0**	**X4_P0**
A to Z ↓	0.0161	0.0166	7.0767	4.0153
A to Z ↑	0.0120	0.0123	5.5566	3.0519
B to Z ↓	0.0075	0.0066	7.2626	4.1222
B to Z ↑	0.0081	0.0062	5.8161	3.2514
	X9_P0	**X13_P0**	**X9_P0**	**X13_P0**
A to Z ↓	0.0171	0.0204	1.6062	1.0126
A to Z ↑	0.0121	0.0150	1.4399	0.9547
B to Z ↓	0.0058	0.0055	1.6594	1.0495
B to Z ↑	0.0067	0.0070	1.5203	1.0242
	X17_P0	**X23_P0**	**X17_P0**	**X23_P0**
A to Z ↓	0.0222	0.0162	0.7994	0.7066
A to Z ↑	0.0158	0.0129	0.7367	0.5112
B to Z ↓	0.0054	0.0065	0.8267	0.7265
B to Z ↑	0.0067	0.0052	0.7961	0.5407
	X27_P0	**X31_P0**	**X27_P0**	**X31_P0**
A to Z ↓	0.0187	0.0161	0.5431	0.5345
A to Z ↑	0.0141	0.0128	0.4949	0.3713
B to Z ↓	0.0055	0.0068	0.5618	0.5491
B to Z ↑	0.0062	0.0053	0.5123	0.4072
	X36_P0		**X36_P0**	
A to Z ↓	0.0214		0.4093	
A to Z ↑	0.0163		0.3700	
B to Z ↓	0.0054		0.4226	
B to Z ↑	0.0060		0.3846	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P0	1.811e-04	1.000e-20
X4_P0	3.056e-04	1.000e-20
X9_P0	7.243e-04	1.000e-20
X13_P0	8.810e-04	1.000e-20
X17_P0	1.122e-03	1.000e-20
X23_P0	1.790e-03	1.000e-20
X27_P0	1.823e-03	1.000e-20
X31_P0	2.357e-03	1.000e-20
X36_P0	2.270e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P0	X4_P0	X9_P0	X13_P0
A (output stable)	1.374e-03	1.579e-03	3.055e-03	3.804e-03
B (output stable)	1.589e-05	2.870e-05	7.705e-05	2.159e-04
A to Z	2.032e-03	2.656e-03	5.630e-03	8.419e-03
B to Z	9.861e-04	1.641e-03	3.841e-03	5.829e-03
	X17_P0	X23_P0	X27_P0	X31_P0
A (output stable)	4.069e-03	7.879e-03	6.947e-03	1.049e-02
B (output stable)	2.555e-04	4.170e-04	4.072e-04	5.521e-04
A to Z	1.023e-02	1.501e-02	1.504e-02	2.001e-02
B to Z	7.399e-03	9.763e-03	1.109e-02	1.293e-02
	X36_P0			
A (output stable)	8.242e-03			

B (output stable)	6.586e-04			
A to Z	2.009e-02			
B to Z	1.453e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

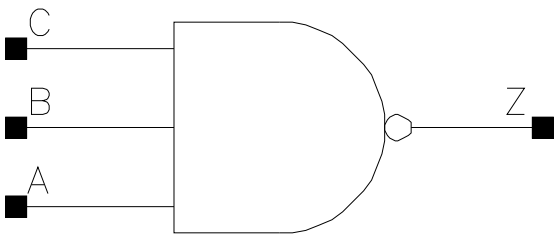
Pin Cycle (vdds)	X2_P0	X4_P0	X9_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P0	X23_P0	X27_P0	X31_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P0	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P0	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P0	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P0	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P0	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P0	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P0	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P0	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P0	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P0	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P0	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P0	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P0	C8T28SOI_LL_-NAND3X7_P0	C8T28SOI_LL_-NAND3X10_P0	C8T28SOI_LL_-NAND3X14_P0
A	0.0006	0.0011	0.0017	0.0022
B	0.0005	0.0011	0.0016	0.0021
C	0.0006	0.0010	0.0015	0.0021
	C8T28SOI_LL_-NAND3X20_P0	C8T28SOI_LL_-NAND3X27_P0	C8T28SOI_-LLBR0P6_-NAND3X3_P0	C8T28SOI_-LLBR0P6_-NAND3X7_P0
A	0.0034	0.0045	0.0007	0.0012
B	0.0032	0.0043	0.0006	0.0011
C	0.0031	0.0042	0.0006	0.0010
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	C8T28SOI_-LLBR0P6_-NAND3X14_P0	C8T28SOI_-LLBR0P6_-NAND3X20_P0	C8T28SOI_-LLBR0P6_-NAND3X27_P0
A	0.0017	0.0023	0.0033	0.0045
B	0.0015	0.0021	0.0031	0.0042
C	0.0016	0.0021	0.0031	0.0042

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND3X3_P0	**C8T28SOI_LL_-NAND3X7_P0**	**C8T28SOI_LL_-NAND3X3_P0**	**C8T28SOI_LL_-NAND3X7_P0**
A to Z ↓	0.0081	0.0088	5.5705	2.8614
A to Z ↑	0.0091	0.0094	3.2214	1.5930
B to Z ↓	0.0095	0.0098	5.6018	2.8728
B to Z ↑	0.0081	0.0082	3.2537	1.6004
C to Z ↓	0.0104	0.0102	5.6350	2.8829
C to Z ↑	0.0069	0.0061	3.3064	1.5493
	C8T28SOI_LL_-NAND3X10_P0	**C8T28SOI_LL_-NAND3X14_P0**	**C8T28SOI_LL_-NAND3X10_P0**	**C8T28SOI_LL_-NAND3X14_P0**
A to Z ↓	0.0084	0.0086	1.9621	1.4914
A to Z ↑	0.0086	0.0089	1.0266	0.8067
B to Z ↓	0.0098	0.0097	1.9730	1.4976
B to Z ↑	0.0075	0.0077	1.0649	0.8085
C to Z ↓	0.0102	0.0103	1.9814	1.5040
C to Z ↑	0.0058	0.0058	1.0757	0.8016
	C8T28SOI_LL_-NAND3X20_P0	**C8T28SOI_LL_-NAND3X27_P0**	**C8T28SOI_LL_-NAND3X20_P0**	**C8T28SOI_LL_-NAND3X27_P0**
A to Z ↓	0.0084	0.0085	1.0140	0.7723
A to Z ↑	0.0085	0.0085	0.5193	0.3926
B to Z ↓	0.0099	0.0100	1.0193	0.7761
B to Z ↑	0.0073	0.0072	0.5199	0.3919
C to Z ↓	0.0103	0.0105	1.0238	0.7796
C to Z ↑	0.0056	0.0055	0.5371	0.4051
	C8T28SOI_-LLBR0P6_-NAND3X3_P0	**C8T28SOI_-LLBR0P6_-NAND3X7_P0**	**C8T28SOI_-LLBR0P6_-NAND3X3_P0**	**C8T28SOI_-LLBR0P6_-NAND3X7_P0**
A to Z ↓	0.0036	0.0050	3.5857	2.0490
A to Z ↑	0.0145	0.0153	4.6179	2.3633
B to Z ↓	0.0043	0.0053	3.6333	2.0682
B to Z ↑	0.0127	0.0133	4.5993	2.3719

C to Z ↓	0.0046	0.0051	3.6807	2.0903
C to Z ↑	0.0107	0.0104	4.6338	2.3499
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	**C8T28SOI_-LLBR0P6_-NAND3X14_P0**	**C8T28SOI_-LLBR0P6_-NAND3X10_P0**	**C8T28SOI_-LLBR0P6_-NAND3X14_P0**
A to Z ↓	0.0042	0.0046	1.3559	1.0378
A to Z ↑	0.0145	0.0148	1.5790	1.2001
B to Z ↓	0.0047	0.0048	1.3713	1.0480
B to Z ↑	0.0124	0.0127	1.5862	1.2022
C to Z ↓	0.0047	0.0046	1.3876	1.0607
C to Z ↑	0.0099	0.0097	1.6018	1.2015
	C8T28SOI_-LLBR0P6_-NAND3X20_P0	**C8T28SOI_-LLBR0P6_-NAND3X27_P0**	**C8T28SOI_-LLBR0P6_-NAND3X20_P0**	**C8T28SOI_-LLBR0P6_-NAND3X27_P0**
A to Z ↓	0.0042	0.0043	0.7003	0.5380
A to Z ↑	0.0146	0.0145	0.7999	0.6051
B to Z ↓	0.0048	0.0049	0.7080	0.5437
B to Z ↑	0.0126	0.0124	0.8006	0.6040
C to Z ↓	0.0046	0.0048	0.7165	0.5502
C to Z ↑	0.0095	0.0094	0.8069	0.6080

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P0	1.578e-04	1.000e-20
C8T28SOI_LL_NAND3X7_P0	3.244e-04	1.000e-20
C8T28SOI_LL_NAND3X10_P0	4.618e-04	1.000e-20
C8T28SOI_LL_NAND3X14_P0	6.123e-04	1.000e-20
C8T28SOI_LL_NAND3X20_P0	9.002e-04	1.000e-20
C8T28SOI_LL_NAND3X27_P0	1.188e-03	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P0	1.253e-04	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P0	2.346e-04	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_P0	3.229e-04	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_P0	4.308e-04	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_P0	6.265e-04	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_P0	8.223e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P0	C8T28SOI_LL_-NAND3X7_P0	C8T28SOI_LL_-NAND3X10_P0	C8T28SOI_LL_-NAND3X14_P0
A (output stable)	2.095e-05	7.992e-05	1.018e-04	1.476e-04
B (output stable)	3.041e-05	1.130e-04	1.514e-04	2.056e-04
C (output stable)	5.663e-05	2.504e-04	3.037e-04	4.535e-04
A to Z	2.023e-03	4.223e-03	6.120e-03	8.119e-03
B to Z	1.845e-03	3.794e-03	5.394e-03	7.259e-03
C to Z	1.695e-03	3.455e-03	4.912e-03	6.575e-03
	C8T28SOI_LL_-NAND3X20_P0	C8T28SOI_LL_-NAND3X27_P0	C8T28SOI_-LLBR0P6_-NAND3X3_P0	C8T28SOI_-LLBR0P6_-NAND3X7_P0
A (output stable)	2.065e-04	2.746e-04	3.382e-05	1.063e-04
B (output stable)	3.041e-04	3.940e-04	4.626e-05	1.460e-04
C (output stable)	6.679e-04	8.587e-04	8.874e-05	3.338e-04

A to Z	1.211e-02	1.602e-02	2.034e-03	4.247e-03
B to Z	1.070e-02	1.416e-02	1.834e-03	3.673e-03
C to Z	9.566e-03	1.269e-02	1.639e-03	3.177e-03
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	C8T28SOI_-LLBR0P6_-NAND3X14_P0	C8T28SOI_-LLBR0P6_-NAND3X20_P0	C8T28SOI_-LLBR0P6_-NAND3X27_P0
A (output stable)	1.360e-04	2.129e-04	2.834e-04	3.800e-04
B (output stable)	1.931e-04	2.906e-04	4.059e-04	5.264e-04
C (output stable)	4.129e-04	6.181e-04	8.986e-04	1.154e-03
A to Z	6.007e-03	8.101e-03	1.193e-02	1.577e-02
B to Z	5.126e-03	6.936e-03	1.019e-02	1.344e-02
C to Z	4.488e-03	5.965e-03	8.690e-03	1.148e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

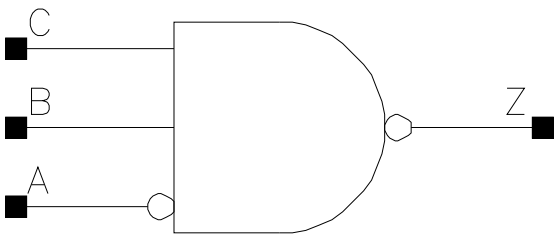
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P0	C8T28SOI_LL_-NAND3X7_P0	C8T28SOI_LL_-NAND3X10_P0	C8T28SOI_LL_-NAND3X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P0	C8T28SOI_LL_-NAND3X27_P0	C8T28SOI_-LLBR0P6_-NAND3X3_P0	C8T28SOI_-LLBR0P6_-NAND3X7_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P0	C8T28SOI_-LLBR0P6_-NAND3X14_P0	C8T28SOI_-LLBR0P6_-NAND3X20_P0	C8T28SOI_-LLBR0P6_-NAND3X27_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X7_P0	0.800	1.360	1.0880
X10_P0	0.800	1.632	1.3056
X14_P0	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X10_P0	X14_P0
A	0.0006	0.0009	0.0008	0.0008
B	0.0006	0.0011	0.0016	0.0021
C	0.0006	0.0010	0.0015	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0200	0.0197	5.5819	2.8709
A to Z ↑	0.0138	0.0147	3.0438	1.4794
B to Z ↓	0.0092	0.0098	5.6343	2.8951
B to Z ↑	0.0078	0.0077	3.2582	1.5521
C to Z ↓	0.0100	0.0099	5.6687	2.9041
C to Z ↑	0.0066	0.0057	3.3014	1.5531
	X10_P0	**X14_P0**	**X10_P0**	**X14_P0**
A to Z ↓	0.0217	0.0237	1.9546	1.4939

A to Z ↑	0.0165	0.0184	1.0141	0.7595
B to Z ↓	0.0097	0.0096	1.9713	1.5061
B to Z ↑	0.0075	0.0073	1.0663	0.7979
C to Z ↓	0.0102	0.0100	1.9790	1.5125
C to Z ↑	0.0059	0.0054	1.0777	0.8026

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.442e-04	1.000e-20
X7_P0	5.346e-04	1.000e-20
X10_P0	6.883e-04	1.000e-20
X14_P0	8.391e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	1.531e-03	2.852e-03	3.303e-03	3.790e-03
B (output stable)	3.067e-05	9.686e-05	1.549e-04	1.912e-04
C (output stable)	5.691e-05	2.590e-04	3.147e-04	4.411e-04
A to Z	2.881e-03	5.882e-03	7.989e-03	1.025e-02
B to Z	1.798e-03	3.720e-03	5.398e-03	7.133e-03
C to Z	1.652e-03	3.337e-03	4.920e-03	6.419e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

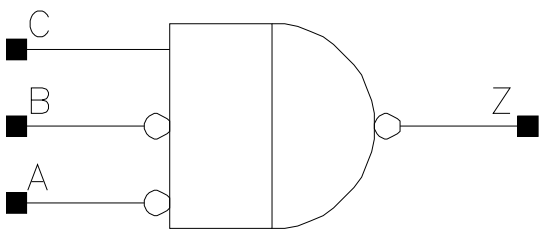
Pin Cycle (vdds)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	0.816	0.6528
X8_P0	0.800	1.088	0.8704
X12_P0	0.800	1.632	1.3056
X15_P0	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X12_P0	X15_P0
A	0.0006	0.0006	0.0012	0.0011
B	0.0007	0.0007	0.0013	0.0012
C	0.0006	0.0011	0.0016	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	**X8_P0**	**X4_P0**	**X8_P0**
A to Z ↓	0.0180	0.0217	3.7762	2.0163
A to Z ↑	0.0119	0.0141	2.9333	1.4637
B to Z ↓	0.0194	0.0232	3.7765	2.0157
B to Z ↑	0.0108	0.0131	2.9314	1.4627
C to Z ↓	0.0067	0.0064	3.8657	2.0591
C to Z ↑	0.0062	0.0054	2.9950	1.5602
	X12_P0	**X15_P0**	**X12_P0**	**X15_P0**
A to Z ↓	0.0198	0.0211	1.3771	1.0484
A to Z ↑	0.0129	0.0159	0.9791	0.7370
B to Z ↓	0.0207	0.0221	1.3765	1.0483

B to Z ↑	0.0114	0.0141	0.9781	0.7370
C to Z ↓	0.0070	0.0065	1.4084	1.0739
C to Z ↑	0.0058	0.0050	1.0634	0.7820

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	3.779e-04	1.000e-20
X8_P0	4.968e-04	1.000e-20
X12_P0	8.015e-04	1.000e-20
X15_P0	9.147e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	8.449e-04	1.015e-03	1.767e-03	1.872e-03
B (output stable)	7.848e-04	9.553e-04	1.675e-03	1.779e-03
C (output stable)	3.197e-05	1.969e-04	2.086e-04	3.302e-04
A to Z	3.708e-03	5.743e-03	9.115e-03	1.097e-02
B to Z	3.495e-03	5.549e-03	8.538e-03	1.035e-02
C to Z	1.821e-03	3.384e-03	5.107e-03	6.598e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

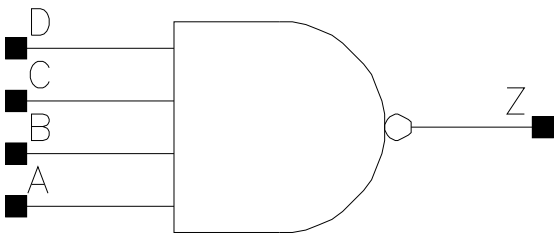
Pin Cycle (vdds)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.224	0.9792
X10_P0	0.800	1.360	1.0880
X14_P0	0.800	1.904	1.5232
X18_P0	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X18_P0
A	0.0004	0.0005	0.0005	0.0006
B	0.0005	0.0005	0.0006	0.0008
C	0.0004	0.0004	0.0005	0.0006
D	0.0005	0.0005	0.0006	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0271	0.0260	2.4317	1.2261
A to Z ↑	0.0235	0.0244	2.9722	1.5167
B to Z ↓	0.0290	0.0280	2.4322	1.2256
B to Z ↑	0.0226	0.0237	2.9722	1.5201
C to Z ↓	0.0289	0.0273	2.4319	1.2271
C to Z ↑	0.0248	0.0258	2.9704	1.5168

D to Z ↓	0.0311	0.0295	2.4307	1.2258
D to Z ↑	0.0241	0.0253	2.9725	1.5162
	X14_P0	**X18_P0**	**X14_P0**	**X18_P0**
A to Z ↓	0.0281	0.0266	0.8446	0.6785
A to Z ↑	0.0245	0.0241	1.0406	0.8133
B to Z ↓	0.0301	0.0284	0.8439	0.6792
B to Z ↑	0.0235	0.0234	1.0417	0.8126
C to Z ↓	0.0283	0.0252	0.8441	0.6789
C to Z ↑	0.0246	0.0236	1.0404	0.8124
D to Z ↓	0.0304	0.0269	0.8440	0.6794
D to Z ↑	0.0239	0.0226	1.0394	0.8129

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	3.639e-04	1.000e-20
X10_P0	5.596e-04	1.000e-20
X14_P0	7.959e-04	1.000e-20
X18_P0	1.104e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	6.148e-04	6.994e-04	9.925e-04	1.135e-03
B (output stable)	5.825e-04	6.599e-04	9.409e-04	1.092e-03
C (output stable)	6.546e-04	6.914e-04	1.000e-03	1.107e-03
D (output stable)	6.136e-04	6.520e-04	9.450e-04	1.047e-03
A to Z	4.120e-03	6.040e-03	9.221e-03	1.094e-02
B to Z	4.041e-03	5.955e-03	9.080e-03	1.085e-02
C to Z	4.335e-03	6.168e-03	8.900e-03	1.041e-02
D to Z	4.257e-03	6.091e-03	8.791e-03	1.027e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

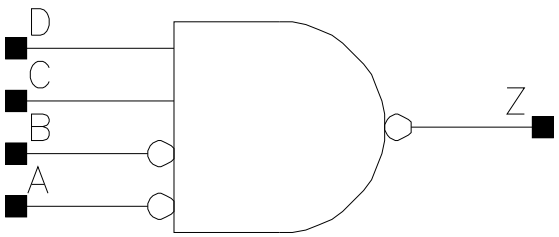
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.952	0.7616
X7_P0	0.800	1.360	1.0880
X10_P0	0.800	2.040	1.6320
X14_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P0	X7_P0	X10_P0	X14_P0
A	0.0007	0.0007	0.0013	0.0011
B	0.0007	0.0007	0.0013	0.0012
C	0.0007	0.0011	0.0016	0.0021
D	0.0006	0.0010	0.0015	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X7_P0	X3_P0	X7_P0
A to Z ↓	0.0203	0.0236	5.4010	2.8664
A to Z ↑	0.0129	0.0152	2.9497	1.4838
B to Z ↓	0.0216	0.0251	5.4021	2.8660
B to Z ↑	0.0116	0.0140	2.9519	1.4836
C to Z ↓	0.0096	0.0097	5.4535	2.8895
C to Z ↑	0.0081	0.0077	3.1343	1.5542

D to Z ↓	0.0101	0.0099	5.4727	2.8984
D to Z ↑	0.0065	0.0056	3.1255	1.5530
	X10_P0	**X14_P0**	**X10_P0**	**X14_P0**
A to Z ↓	0.0222	0.0237	1.9562	1.4986
A to Z ↑	0.0140	0.0180	1.0039	0.7413
B to Z ↓	0.0230	0.0247	1.9563	1.4982
B to Z ↑	0.0123	0.0166	1.0039	0.7404
C to Z ↓	0.0097	0.0096	1.9695	1.5085
C to Z ↑	0.0076	0.0074	1.0670	0.7993
D to Z ↓	0.0101	0.0101	1.9779	1.5149
D to Z ↑	0.0058	0.0054	1.0781	0.8047

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	3.382e-04	1.000e-20
X7_P0	4.228e-04	1.000e-20
X10_P0	7.014e-04	1.000e-20
X14_P0	7.632e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	1.051e-03	1.250e-03	2.255e-03	2.400e-03
B (output stable)	9.757e-04	1.180e-03	2.106e-03	2.255e-03
C (output stable)	5.202e-05	1.044e-04	1.601e-04	2.055e-04
D (output stable)	1.120e-04	2.787e-04	3.448e-04	4.850e-04
A to Z	3.973e-03	6.094e-03	9.776e-03	1.201e-02
B to Z	3.794e-03	5.935e-03	9.197e-03	1.144e-02
C to Z	1.899e-03	3.713e-03	5.395e-03	7.129e-03
D to Z	1.795e-03	3.337e-03	4.903e-03	6.429e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

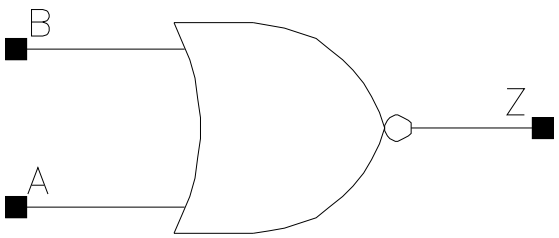
Pin Cycle (vdds)	X3_P0	X7_P0	X10_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.408	0.3264
X4_P0	0.800	0.408	0.3264
X8_P0	0.800	0.680	0.5440
X9_P0	1.600	0.408	0.6528
X12_P0	0.800	0.952	0.7616
X16_P0	0.800	1.224	0.9792
X19_P0	1.600	0.680	1.0880
X20_P0	0.800	1.496	1.1968
X23_P0	0.800	1.496	1.1968
X24_P0	0.800	1.768	1.4144
X27_P0	0.800	1.632	1.3056
X29_P0	1.600	0.952	1.5232
X31_P0	0.800	2.312	1.8496
X34_P0	0.800	2.040	1.6320
X38_P0	0.800	2.176	1.7408
X39_P0	1.600	1.224	1.9584
X46_P0	1.600	1.224	1.9584
X57_P0	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P0	X4_P0	X8_P0	X9_P0
A	0.0004	0.0005	0.0011	0.0011
B	0.0004	0.0005	0.0010	0.0011
	X12_P0	X16_P0	X19_P0	X20_P0

A	0.0017	0.0022	0.0023	0.0028
B	0.0016	0.0021	0.0022	0.0026
	X23_P0	X24_P0	X27_P0	X29_P0
A	0.0007	0.0033	0.0008	0.0035
B	0.0007	0.0032	0.0007	0.0034
	X31_P0	X34_P0	X38_P0	X39_P0
A	0.0044	0.0008	0.0008	0.0047
B	0.0042	0.0007	0.0007	0.0045
	X46_P0	X57_P0		
A	0.0007	0.0007		
B	0.0008	0.0008		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X4_P0**	**X2_P0**	**X4_P0**
A to Z ↓	0.0043	0.0042	4.7826	2.6646
A to Z ↑	0.0109	0.0099	10.5345	5.9715
B to Z ↓	0.0032	0.0029	4.8247	2.6919
B to Z ↑	0.0123	0.0110	10.5979	6.0004
	X8_P0	**X9_P0**	**X8_P0**	**X9_P0**
A to Z ↓	0.0038	0.0031	1.2884	1.0362
A to Z ↑	0.0088	0.0096	2.8729	2.6995
B to Z ↓	0.0017	0.0020	1.2912	1.0738
B to Z ↑	0.0091	0.0105	2.8850	2.7157
	X12_P0	**X16_P0**	**X12_P0**	**X16_P0**
A to Z ↓	0.0041	0.0040	0.8809	0.6556
A to Z ↑	0.0084	0.0086	1.8807	1.4430
B to Z ↓	0.0023	0.0021	0.8903	0.6630
B to Z ↑	0.0093	0.0091	1.8902	1.4500
	X19_P0	**X20_P0**	**X19_P0**	**X20_P0**
A to Z ↓	0.0035	0.0043	0.5214	0.5377
A to Z ↑	0.0100	0.0085	1.3936	1.1457
B to Z ↓	0.0020	0.0024	0.5271	0.5438
B to Z ↑	0.0107	0.0092	1.3982	1.1523
	X23_P0	**X24_P0**	**X23_P0**	**X24_P0**
A to Z ↓	0.0199	0.0041	0.5310	0.4456
A to Z ↑	0.0268	0.0085	0.6164	0.9682
B to Z ↓	0.0186	0.0021	0.5309	0.4510
B to Z ↑	0.0281	0.0090	0.6168	0.9734
	X27_P0	**X29_P0**	**X27_P0**	**X29_P0**
A to Z ↓	0.0209	0.0032	0.4420	0.3450
A to Z ↑	0.0277	0.0096	0.5143	0.9367
B to Z ↓	0.0195	0.0017	0.4421	0.3483
B to Z ↑	0.0291	0.0104	0.5152	0.9410
	X31_P0	**X34_P0**	**X31_P0**	**X34_P0**
A to Z ↓	0.0042	0.0222	0.3336	0.3639
A to Z ↑	0.0086	0.0311	0.7264	0.4252
B to Z ↓	0.0024	0.0208	0.3374	0.3637
B to Z ↑	0.0092	0.0327	0.7303	0.4252
	X38_P0	**X39_P0**	**X38_P0**	**X39_P0**
A to Z ↓	0.0228	0.0034	0.3168	0.2627
A to Z ↑	0.0318	0.0096	0.3726	0.7043

B to Z ↓	0.0214	0.0018	0.3171	0.2660
B to Z ↑	0.0333	0.0103	0.3729	0.7070
	X46_P0	**X57_P0**	**X46_P0**	**X57_P0**
A to Z ↓	0.0253	0.0272	0.2424	0.1978
A to Z ↑	0.0328	0.0344	0.3675	0.2963
B to Z ↓	0.0241	0.0260	0.2422	0.1978
B to Z ↑	0.0348	0.0364	0.3676	0.2965

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P0	9.452e-05	1.000e-20
X4_P0	2.006e-04	1.000e-20
X8_P0	4.303e-04	1.000e-20
X9_P0	4.835e-04	1.000e-20
X12_P0	6.237e-04	1.000e-20
X16_P0	8.168e-04	1.000e-20
X19_P0	9.387e-04	1.000e-20
X20_P0	1.010e-03	1.000e-20
X23_P0	1.834e-03	1.000e-20
X24_P0	1.204e-03	1.000e-20
X27_P0	2.099e-03	1.000e-20
X29_P0	1.376e-03	1.000e-20
X31_P0	1.590e-03	1.000e-20
X34_P0	2.451e-03	1.000e-20
X38_P0	2.699e-03	1.000e-20
X39_P0	1.814e-03	1.000e-20
X46_P0	2.847e-03	1.000e-20
X57_P0	3.395e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P0	X4_P0	X8_P0	X9_P0
A (output stable)	1.771e-05	3.119e-05	1.086e-04	7.125e-05
B (output stable)	2.419e-05	4.083e-05	2.272e-04	9.270e-05
A to Z	1.049e-03	1.800e-03	3.629e-03	4.001e-03
B to Z	9.424e-04	1.591e-03	3.114e-03	3.538e-03
	X12_P0	X16_P0	X19_P0	X20_P0
A (output stable)	1.527e-04	2.127e-04	2.274e-04	2.522e-04
B (output stable)	2.807e-04	4.250e-04	5.204e-04	4.431e-04
A to Z	5.427e-03	7.162e-03	8.007e-03	8.962e-03
B to Z	4.702e-03	6.168e-03	7.024e-03	7.738e-03
	X23_P0	X24_P0	X27_P0	X29_P0
A (output stable)	3.591e-05	3.134e-04	3.500e-05	3.014e-04
B (output stable)	4.764e-05	5.688e-04	4.500e-05	5.240e-04
A to Z	1.166e-02	1.062e-02	1.333e-02	1.173e-02
B to Z	1.151e-02	9.166e-03	1.317e-02	1.028e-02
	X31_P0	X34_P0	X38_P0	X39_P0
A (output stable)	4.170e-04	3.682e-05	4.318e-05	4.434e-04
B (output stable)	7.731e-04	5.000e-05	5.000e-05	8.691e-04
A to Z	1.419e-02	1.756e-02	1.939e-02	1.555e-02
B to Z	1.227e-02	1.737e-02	1.919e-02	1.359e-02
	X46_P0	X57_P0		

A (output stable)	4.318e-05	4.318e-05		
B (output stable)	5.000e-05	5.000e-05		
A to Z	2.135e-02	2.652e-02		
B to Z	2.120e-02	2.637e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

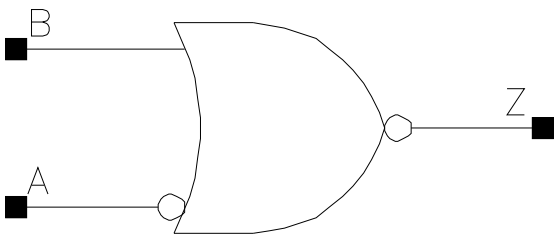
Pin Cycle (vdds)	X2_P0	X4_P0	X8_P0	X9_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P0	X16_P0	X19_P0	X20_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P0	X24_P0	X27_P0	X29_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P0	X34_P0	X38_P0	X39_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P0	X57_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	0.544	0.4352
X3_P0	0.800	0.544	0.4352
X4_P0	0.800	0.544	0.4352
X10_P0	1.600	0.544	0.8704
X14_P0	1.600	0.816	1.3056
X19_P0	1.600	0.816	1.3056
X29_P0	1.600	1.088	1.7408
X39_P0	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P0	X3_P0	X4_P0	X10_P0
A	0.0005	0.0005	0.0006	0.0009
B	0.0004	0.0004	0.0005	0.0011
	X14_P0	X19_P0	X29_P0	X39_P0
A	0.0009	0.0009	0.0015	0.0015
B	0.0018	0.0022	0.0034	0.0044

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	X3_P0	X2_P0	X3_P0
A to Z ↓	0.0153	0.0152	4.5345	3.4792
A to Z ↑	0.0133	0.0133	10.4976	9.0035
B to Z ↓	0.0030	0.0022	4.8497	3.7028

B to Z ↑	0.0118	0.0116	10.5902	9.0627
	X4_P0	**X10_P0**	**X4_P0**	**X10_P0**
A to Z ↓	0.0157	0.0163	2.6944	0.9834
A to Z ↑	0.0135	0.0132	6.6770	2.6621
B to Z ↓	0.0022	0.0019	2.8631	1.0227
B to Z ↑	0.0106	0.0108	6.7307	2.6837
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0192	0.0203	0.6185	0.4834
A to Z ↑	0.0158	0.0165	1.7881	1.3407
B to Z ↓	0.0016	0.0017	0.7043	0.5509
B to Z ↑	0.0102	0.0096	1.8063	1.3553
	X29_P0	**X39_P0**	**X29_P0**	**X39_P0**
A to Z ↓	0.0177	0.0203	0.3263	0.2444
A to Z ↑	0.0155	0.0174	0.9374	0.6865
B to Z ↓	0.0017	0.0016	0.3491	0.2723
B to Z ↑	0.0104	0.0096	0.9458	0.6933

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P0	1.847e-04	1.000e-20
X3_P0	2.118e-04	1.000e-20
X4_P0	2.759e-04	1.000e-20
X10_P0	7.400e-04	1.000e-20
X14_P0	8.943e-04	1.000e-20
X19_P0	1.195e-03	1.000e-20
X29_P0	1.847e-03	1.000e-20
X39_P0	2.335e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P0	X3_P0	X4_P0	X10_P0
A (output stable)	1.380e-03	1.443e-03	1.542e-03	3.117e-03
B (output stable)	2.445e-05	2.789e-05	3.835e-05	9.727e-05
A to Z	2.029e-03	2.192e-03	2.497e-03	5.617e-03
B to Z	9.156e-04	1.080e-03	1.392e-03	3.652e-03
	X14_P0	X19_P0	X29_P0	X39_P0
A (output stable)	3.926e-03	4.247e-03	7.064e-03	8.360e-03
B (output stable)	1.521e-04	1.972e-04	5.306e-04	3.822e-04
A to Z	8.035e-03	9.779e-03	1.494e-02	1.944e-02
B to Z	5.223e-03	6.746e-03	1.024e-02	1.332e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X2_P0	X3_P0	X4_P0	X10_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P0	X19_P0	X29_P0	X39_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

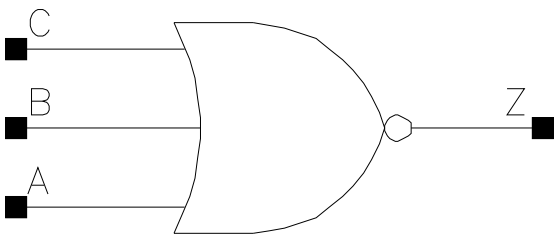
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.544	0.4352
X7_P0	0.800	0.952	0.7616
X11_P0	0.800	1.360	1.0880
X14_P0	0.800	1.768	1.4144
X21_P0	0.800	2.584	2.0672
X29_P0	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X11_P0	X14_P0
A	0.0006	0.0010	0.0017	0.0023
B	0.0006	0.0012	0.0016	0.0024
C	0.0006	0.0010	0.0015	0.0021
	X21_P0	X29_P0		
A	0.0035	0.0046		
B	0.0035	0.0046		
C	0.0031	0.0041		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0047	0.0048	2.7237	1.4154
A to Z ↑	0.0120	0.0117	8.2265	4.2825

B to Z ↓	0.0041	0.0039	2.7439	1.3676
B to Z ↑	0.0129	0.0127	8.2477	4.2952
C to Z ↓	0.0031	0.0020	2.7842	1.3874
C to Z ↑	0.0134	0.0120	8.2750	4.2866
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0047	0.0049	0.8933	0.6829
A to Z ↑	0.0121	0.0116	2.8636	2.0627
B to Z ↓	0.0042	0.0040	0.8993	0.6659
B to Z ↑	0.0127	0.0124	2.8685	2.0685
C to Z ↓	0.0024	0.0023	0.9017	0.6799
C to Z ↑	0.0129	0.0120	2.8705	2.0668
	X21_P0	**X29_P0**	**X21_P0**	**X29_P0**
A to Z ↓	0.0048	0.0049	0.4545	0.3412
A to Z ↑	0.0115	0.0116	1.3890	1.0458
B to Z ↓	0.0041	0.0042	0.4473	0.3380
B to Z ↑	0.0123	0.0124	1.3921	1.0481
C to Z ↓	0.0025	0.0026	0.4572	0.3452
C to Z ↑	0.0122	0.0122	1.3922	1.0486

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	1.696e-04	1.000e-20
X7_P0	3.412e-04	1.000e-20
X11_P0	4.999e-04	1.000e-20
X14_P0	6.904e-04	1.000e-20
X21_P0	1.011e-03	1.000e-20
X29_P0	1.340e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	3.325e-05	7.989e-05	1.367e-04	1.658e-04
B (output stable)	4.200e-05	1.168e-04	1.650e-04	2.327e-04
C (output stable)	8.009e-05	2.930e-04	3.479e-04	5.784e-04
A to Z	1.887e-03	3.657e-03	5.721e-03	7.562e-03
B to Z	1.693e-03	3.329e-03	4.970e-03	6.901e-03
C to Z	1.511e-03	2.851e-03	4.446e-03	5.865e-03
	X21_P0	X29_P0		
A (output stable)	2.399e-04	3.200e-04		
B (output stable)	3.384e-04	4.550e-04		
C (output stable)	8.066e-04	1.082e-03		
A to Z	1.127e-02	1.501e-02		
B to Z	1.019e-02	1.354e-02		
C to Z	8.734e-03	1.161e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

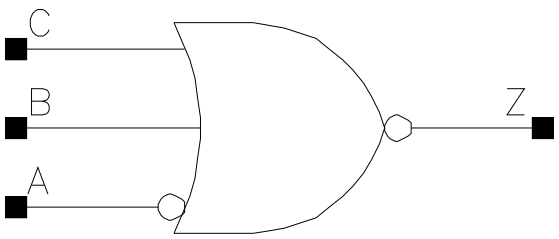
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P0	X29_P0		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X7_P0	0.800	1.360	1.0880
X11_P0	0.800	1.632	1.3056
X14_P0	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X11_P0	X14_P0
A	0.0007	0.0007	0.0009	0.0013
B	0.0006	0.0011	0.0015	0.0021
C	0.0006	0.0010	0.0015	0.0020

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X7_P0**	**X3_P0**	**X7_P0**
A to Z ↓	0.0167	0.0156	2.5501	1.2102
A to Z ↑	0.0175	0.0178	8.3204	4.1107
B to Z ↓	0.0041	0.0041	2.7522	1.3072
B to Z ↑	0.0128	0.0129	8.3224	4.1147
C to Z ↓	0.0030	0.0022	2.7885	1.3178
C to Z ↑	0.0133	0.0124	8.3475	4.1104
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0186	0.0150	0.8478	0.6284

A to Z ↑	0.0205	0.0176	2.8769	2.1186
B to Z ↓	0.0041	0.0040	0.9003	0.6758
B to Z ↑	0.0126	0.0124	2.8793	2.1208
C to Z ↓	0.0023	0.0022	0.9029	0.6837
C to Z ↑	0.0127	0.0122	2.8817	2.1211

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.674e-04	1.000e-20
X7_P0	5.867e-04	1.000e-20
X11_P0	7.089e-04	1.000e-20
X14_P0	1.078e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	1.596e-03	2.889e-03	3.334e-03	5.390e-03
B (output stable)	4.313e-05	1.294e-04	1.696e-04	2.458e-04
C (output stable)	8.041e-05	3.227e-04	3.490e-04	5.614e-04
A to Z	2.931e-03	5.967e-03	7.765e-03	1.126e-02
B to Z	1.676e-03	3.490e-03	4.952e-03	6.681e-03
C to Z	1.500e-03	3.027e-03	4.400e-03	5.812e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

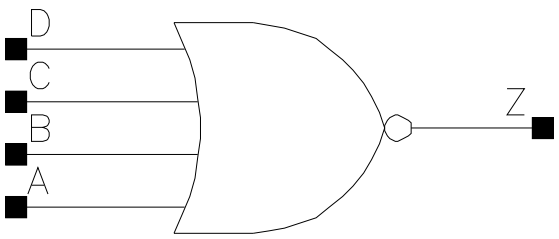
Pin Cycle (vdds)	X3_P0	X7_P0	X11_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	1.224	0.9792
X10_P0	0.800	1.632	1.3056
X14_P0	0.800	1.904	1.5232
X18_P0	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X18_P0
A	0.0005	0.0004	0.0005	0.0006
B	0.0005	0.0006	0.0007	0.0007
C	0.0005	0.0005	0.0005	0.0006
D	0.0005	0.0005	0.0006	0.0006

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0172	0.0213	2.5260	1.2165
A to Z ↑	0.0303	0.0336	3.1184	1.5136
B to Z ↓	0.0163	0.0211	2.5274	1.2160
B to Z ↑	0.0319	0.0362	3.1169	1.5151
C to Z ↓	0.0181	0.0216	2.5255	1.2152
C to Z ↑	0.0325	0.0363	3.1159	1.5126

D to Z ↓	0.0175	0.0207	2.5237	1.2150
D to Z ↑	0.0345	0.0378	3.1152	1.5144
	X14_P0	**X18_P0**	**X14_P0**	**X18_P0**
A to Z ↓	0.0206	0.0222	0.8366	0.6618
A to Z ↑	0.0309	0.0302	1.0458	0.7740
B to Z ↓	0.0200	0.0211	0.8365	0.6612
B to Z ↑	0.0330	0.0317	1.0466	0.7747
C to Z ↓	0.0202	0.0223	0.8341	0.6597
C to Z ↑	0.0313	0.0310	1.0438	0.7744
D to Z ↓	0.0193	0.0211	0.8343	0.6597
D to Z ↑	0.0329	0.0324	1.0454	0.7734

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	5.679e-04	1.000e-20
X10_P0	9.027e-04	1.000e-20
X14_P0	1.347e-03	1.000e-20
X18_P0	1.842e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	6.526e-04	7.354e-04	9.485e-04	1.171e-03
B (output stable)	6.103e-04	7.031e-04	8.971e-04	1.099e-03
C (output stable)	6.864e-04	7.078e-04	9.554e-04	1.182e-03
D (output stable)	6.424e-04	6.712e-04	9.026e-04	1.111e-03
A to Z	4.034e-03	6.475e-03	9.049e-03	1.158e-02
B to Z	3.937e-03	6.391e-03	8.927e-03	1.139e-02
C to Z	4.169e-03	6.403e-03	8.657e-03	1.115e-02
D to Z	4.077e-03	6.309e-03	8.532e-03	1.096e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

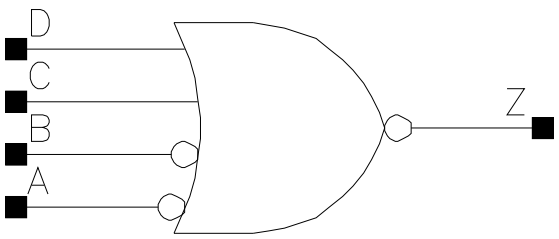
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	1.224	0.9792
X7_P0	0.800	1.496	1.1968
X11_P0	0.800	2.040	1.6320
X14_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P0	X7_P0	X11_P0	X14_P0
A	0.0007	0.0007	0.0013	0.0013
B	0.0007	0.0007	0.0013	0.0013
C	0.0005	0.0011	0.0015	0.0021
D	0.0005	0.0010	0.0015	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X7_P0	X4_P0	X7_P0
A to Z ↓	0.0169	0.0174	2.3786	1.2294
A to Z ↑	0.0221	0.0218	8.0246	4.1835
B to Z ↓	0.0155	0.0160	2.3788	1.2280
B to Z ↑	0.0233	0.0231	8.0290	4.1824
C to Z ↓	0.0043	0.0040	2.5166	1.3173
C to Z ↑	0.0137	0.0129	8.0136	4.1890

D to Z ↓	0.0032	0.0022	2.5342	1.3175
D to Z ↑	0.0141	0.0125	8.0250	4.1864
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0160	0.0174	0.8392	0.6318
A to Z ↑	0.0204	0.0222	2.8371	2.1084
B to Z ↓	0.0142	0.0160	0.8386	0.6302
B to Z ↑	0.0214	0.0236	2.8368	2.1075
C to Z ↓	0.0042	0.0042	0.8995	0.6736
C to Z ↑	0.0125	0.0124	2.8358	2.1085
D to Z ↓	0.0024	0.0023	0.9032	0.6778
D to Z ↑	0.0126	0.0123	2.8387	2.1082

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	3.863e-04	1.000e-20
X7_P0	5.205e-04	1.000e-20
X11_P0	8.356e-04	1.000e-20
X14_P0	9.608e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X7_P0	X11_P0	X14_P0
A (output stable)	1.227e-03	1.335e-03	2.306e-03	2.580e-03
B (output stable)	1.171e-03	1.286e-03	2.178e-03	2.463e-03
C (output stable)	7.831e-05	1.287e-04	1.894e-04	2.657e-04
D (output stable)	1.384e-04	3.281e-04	4.022e-04	6.375e-04
A to Z	4.639e-03	6.147e-03	9.757e-03	1.218e-02
B to Z	4.395e-03	5.931e-03	9.245e-03	1.168e-02
C to Z	1.845e-03	3.455e-03	4.987e-03	6.690e-03
D to Z	1.683e-03	3.007e-03	4.433e-03	5.878e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

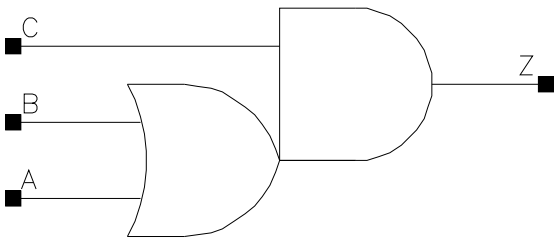
Pin Cycle (vdds)	X4_P0	X7_P0	X11_P0	X14_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.680	0.5440
X10_P0	0.800	0.952	0.7616
X19_P0	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0
A	0.0006	0.0006	0.0011
B	0.0006	0.0007	0.0014
C	0.0007	0.0008	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0162	0.0183	2.4373	1.2200
A to Z ↑	0.0144	0.0180	3.4106	1.5068
B to Z ↓	0.0177	0.0200	2.4406	1.2211
B to Z ↑	0.0129	0.0162	3.4117	1.5043
C to Z ↓	0.0154	0.0169	2.4175	1.2075
C to Z ↑	0.0131	0.0159	3.4086	1.5053
	X19_P0		**X19_P0**	
A to Z ↓	0.0191		0.6329	
A to Z ↑	0.0190		0.7721	

B to Z ↓	0.0208		0.6331	
B to Z ↑	0.0171		0.7705	
C to Z ↓	0.0171		0.6253	
C to Z ↑	0.0162		0.7717	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	4.469e-04	1.000e-20
X10_P0	7.663e-04	1.000e-20
X19_P0	1.462e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X19_P0
A (output stable)	5.356e-05	5.579e-05	1.161e-04
B (output stable)	5.897e-05	6.276e-05	1.251e-04
C (output stable)	5.586e-05	5.818e-05	1.169e-04
A to Z	3.172e-03	5.564e-03	1.115e-02
B to Z	2.998e-03	5.349e-03	1.079e-02
C to Z	3.418e-03	5.542e-03	1.102e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

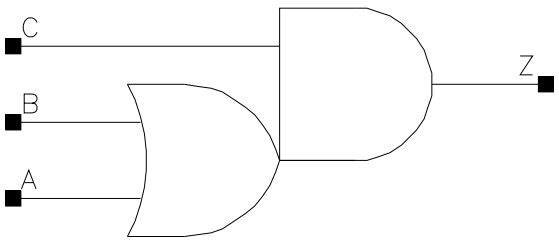
Pin Cycle (vdds)	X5_P0	X10_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X10_P0	0.800	1.360	1.0880
X14_P0	0.800	1.496	1.1968
X19_P0	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0006	0.0013	0.0013	0.0013
B	0.0006	0.0012	0.0012	0.0012
C	0.0007	0.0013	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0201	0.0168	2.3944	1.2165
A to Z ↑	0.0140	0.0131	2.9891	1.4619
B to Z ↓	0.0217	0.0180	2.3932	1.2152
B to Z ↑	0.0127	0.0118	2.9848	1.4622
C to Z ↓	0.0142	0.0115	2.3596	1.2017
C to Z ↑	0.0140	0.0131	2.9829	1.4600
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0187	0.0204	0.8428	0.6337

A to Z ↑	0.0146	0.0160	0.9927	0.7456
B to Z ↓	0.0201	0.0219	0.8420	0.6335
B to Z ↑	0.0135	0.0150	0.9923	0.7453
C to Z ↓	0.0131	0.0144	0.8302	0.6235
C to Z ↑	0.0148	0.0163	0.9896	0.7429

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	4.919e-04	1.000e-20
X10_P0	1.025e-03	1.000e-20
X14_P0	1.245e-03	1.000e-20
X19_P0	1.465e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	2.297e-05	4.811e-05	4.667e-05	4.855e-05
B (output stable)	2.547e-05	5.680e-05	5.764e-05	5.858e-05
C (output stable)	1.669e-04	3.380e-04	3.426e-04	3.455e-04
A to Z	3.799e-03	7.120e-03	9.196e-03	1.141e-02
B to Z	3.611e-03	6.640e-03	8.722e-03	1.096e-02
C to Z	3.418e-03	6.384e-03	8.213e-03	1.012e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

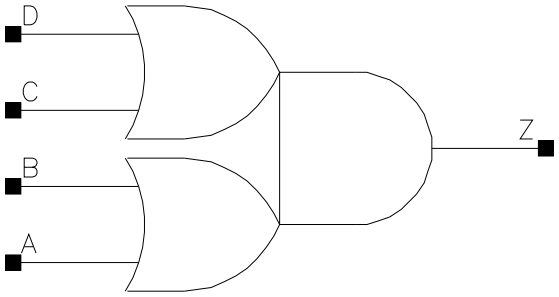
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.952	0.7616
X10_P0	0.800	1.088	0.8704
X14_P0	0.800	1.904	1.5232
X19_P0	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0006	0.0012	0.0012
B	0.0005	0.0007	0.0012	0.0012
C	0.0005	0.0007	0.0013	0.0013
D	0.0004	0.0007	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0271	0.0225	2.4565	1.2274
A to Z ↑	0.0195	0.0175	2.9958	1.4971
B to Z ↓	0.0290	0.0242	2.4557	1.2269

B to Z ↑	0.0185	0.0164	2.9951	1.4947
C to Z ↓	0.0232	0.0199	2.4368	1.2212
C to Z ↑	0.0199	0.0185	2.9905	1.4948
D to Z ↓	0.0249	0.0214	2.4356	1.2212
D to Z ↑	0.0185	0.0170	2.9867	1.4922
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0216	0.0229	0.8513	0.6369
A to Z ↑	0.0167	0.0176	0.9958	0.7484
B to Z ↓	0.0228	0.0241	0.8511	0.6367
B to Z ↑	0.0151	0.0161	0.9942	0.7467
C to Z ↓	0.0184	0.0198	0.8467	0.6332
C to Z ↑	0.0171	0.0182	0.9930	0.7470
D to Z ↓	0.0193	0.0208	0.8465	0.6330
D to Z ↑	0.0152	0.0164	0.9919	0.7454

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	3.414e-04	1.000e-20
X10_P0	7.362e-04	1.000e-20
X14_P0	1.222e-03	1.000e-20
X19_P0	1.397e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	2.197e-05	3.520e-05	9.373e-05	9.302e-05
B (output stable)	2.557e-05	4.027e-05	1.771e-04	1.766e-04
C (output stable)	5.487e-05	7.094e-05	1.626e-04	1.638e-04
D (output stable)	6.068e-05	7.785e-05	2.373e-04	2.381e-04
A to Z	3.790e-03	6.312e-03	1.025e-02	1.230e-02
B to Z	3.680e-03	6.090e-03	9.703e-03	1.175e-02
C to Z	3.428e-03	5.866e-03	9.346e-03	1.136e-02
D to Z	3.318e-03	5.654e-03	8.780e-03	1.078e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

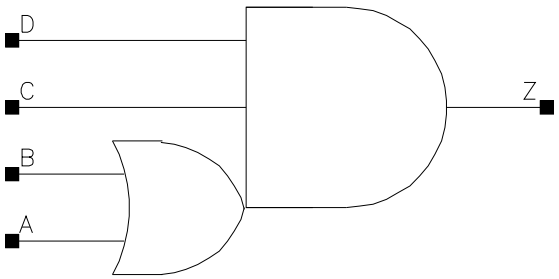
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	0.816	0.6528
X10_P0	0.800	1.088	0.8704
X14_P0	0.800	1.904	1.5232
X19_P0	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P0	X10_P0	X14_P0	X19_P0
A	0.0004	0.0009	0.0010	0.0012
B	0.0005	0.0007	0.0011	0.0013
C	0.0005	0.0007	0.0011	0.0012
D	0.0005	0.0007	0.0010	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X10_P0	X4_P0	X10_P0
A to Z ↓	0.0225	0.0218	2.6497	1.2460
A to Z ↑	0.0230	0.0249	3.1667	1.5274
B to Z ↓	0.0245	0.0223	2.6489	1.2431
B to Z ↑	0.0221	0.0220	3.1653	1.5232
C to Z ↓	0.0200	0.0181	2.6030	1.2262

C to Z ↑	0.0201	0.0206	3.1658	1.5220
D to Z ↓	0.0194	0.0174	2.6022	1.2253
D to Z ↑	0.0221	0.0223	3.1646	1.5226
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0215	0.0206	0.8498	0.6324
A to Z ↑	0.0240	0.0251	1.0139	0.7603
B to Z ↓	0.0224	0.0215	0.8494	0.6318
B to Z ↑	0.0218	0.0228	1.0118	0.7588
C to Z ↓	0.0191	0.0183	0.8375	0.6240
C to Z ↑	0.0203	0.0209	1.0127	0.7595
D to Z ↓	0.0180	0.0173	0.8356	0.6227
D to Z ↑	0.0217	0.0224	1.0123	0.7585

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	3.593e-04	1.000e-20
X10_P0	8.013e-04	1.000e-20
X14_P0	1.164e-03	1.000e-20
X19_P0	1.532e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X10_P0	X14_P0	X19_P0
A (output stable)	5.136e-05	7.943e-05	1.285e-04	1.438e-04
B (output stable)	4.932e-05	8.710e-05	1.498e-04	1.690e-04
C (output stable)	1.938e-05	3.509e-05	8.324e-05	9.195e-05
D (output stable)	2.622e-05	4.239e-05	1.416e-04	1.568e-04
A to Z	3.314e-03	6.328e-03	9.670e-03	1.238e-02
B to Z	3.227e-03	6.004e-03	9.163e-03	1.172e-02
C to Z	3.414e-03	6.233e-03	9.817e-03	1.243e-02
D to Z	3.309e-03	6.085e-03	9.414e-03	1.197e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

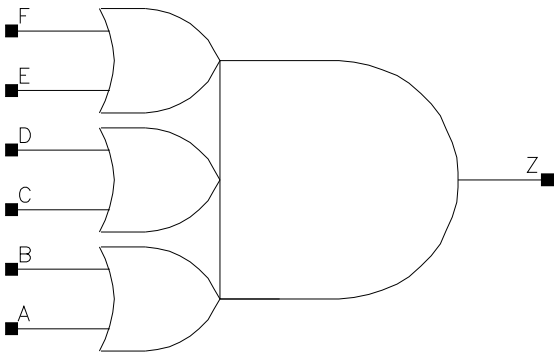
Pin Cycle (vdds)	X4_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	1.360	1.0880
X9_P0	0.800	1.496	1.1968
X19_P0	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P0	X9_P0	X19_P0
A	0.0005	0.0006	0.0010
B	0.0007	0.0009	0.0013
C	0.0005	0.0006	0.0011
D	0.0004	0.0006	0.0013
E	0.0005	0.0006	0.0011
F	0.0005	0.0007	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X9_P0	X4_P0	X9_P0
A to Z ↓	0.0314	0.0266	2.6906	1.3312
A to Z ↑	0.0245	0.0241	3.2451	1.5959
B to Z ↓	0.0343	0.0291	2.6909	1.3315
B to Z ↑	0.0242	0.0233	3.2484	1.5958
C to Z ↓	0.0288	0.0243	2.6741	1.3244
C to Z ↑	0.0260	0.0248	3.2462	1.5947
D to Z ↓	0.0307	0.0260	2.6726	1.3247
D to Z ↑	0.0246	0.0233	3.2430	1.5934
E to Z ↓	0.0248	0.0216	2.6483	1.3171
E to Z ↑	0.0249	0.0246	3.2404	1.5920
F to Z ↓	0.0269	0.0234	2.6484	1.3168
F to Z ↑	0.0240	0.0234	3.2388	1.5914
	X19_P0		X19_P0	
A to Z ↓	0.0264		0.6407	
A to Z ↑	0.0234		0.7610	
B to Z ↓	0.0284		0.6408	
B to Z ↑	0.0216		0.7586	
C to Z ↓	0.0243		0.6370	
C to Z ↑	0.0243		0.7599	
D to Z ↓	0.0262		0.6372	
D to Z ↑	0.0228		0.7580	
E to Z ↓	0.0215		0.6334	
E to Z ↑	0.0243		0.7585	
F to Z ↓	0.0233		0.6334	
F to Z ↑	0.0226		0.7566	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	3.707e-04	1.000e-20
X9_P0	8.226e-04	1.000e-20
X19_P0	1.587e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X9_P0	X19_P0
A (output stable)	2.130e-05	3.422e-05	6.283e-05
B (output stable)	2.880e-05	4.243e-05	7.345e-05
C (output stable)	3.477e-05	4.821e-05	9.529e-05
D (output stable)	3.946e-05	5.301e-05	1.062e-04
E (output stable)	8.781e-05	1.113e-04	2.102e-04
F (output stable)	8.709e-05	1.167e-04	2.178e-04
A to Z	4.316e-03	7.274e-03	1.452e-02
B to Z	4.240e-03	7.118e-03	1.409e-02
C to Z	4.006e-03	6.840e-03	1.366e-02
D to Z	3.898e-03	6.638e-03	1.323e-02
E to Z	3.612e-03	6.368e-03	1.275e-02
F to Z	3.523e-03	6.192e-03	1.234e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

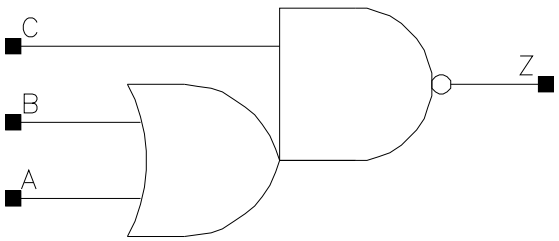
Pin Cycle (vdds)	X4_P0	X9_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.544	0.4352
X10_P0	0.800	1.360	1.0880
X20_P0	0.800	2.720	2.1760
X26_P0	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P0	X10_P0	X20_P0	X26_P0
A	0.0005	0.0016	0.0031	0.0042
B	0.0005	0.0014	0.0029	0.0040
C	0.0005	0.0017	0.0035	0.0047

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X10_P0**	**X3_P0**	**X10_P0**
A to Z ↓	0.0071	0.0084	4.5193	1.4308
A to Z ↑	0.0092	0.0086	6.7084	1.9096
B to Z ↓	0.0053	0.0064	4.4315	1.4367
B to Z ↑	0.0104	0.0093	6.7465	1.9217
C to Z ↓	0.0059	0.0067	4.1043	1.3103
C to Z ↑	0.0096	0.0087	3.7367	1.0653
	X20_P0	**X26_P0**	**X20_P0**	**X26_P0**
A to Z ↓	0.0088	0.0089	0.7317	0.5544

A to Z ↑	0.0090	0.0090	0.9841	0.7412
B to Z ↓	0.0067	0.0069	0.7407	0.5638
B to Z ↑	0.0098	0.0098	0.9896	0.7454
C to Z ↓	0.0072	0.0072	0.6728	0.5105
C to Z ↑	0.0089	0.0088	0.5252	0.3956

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.174e-04	1.000e-20
X10_P0	7.591e-04	1.000e-20
X20_P0	1.480e-03	1.000e-20
X26_P0	1.953e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X10_P0	X20_P0	X26_P0
A (output stable)	4.705e-05	1.713e-04	3.497e-04	4.535e-04
B (output stable)	5.243e-05	2.096e-04	4.358e-04	5.631e-04
C (output stable)	5.008e-05	1.678e-04	3.522e-04	4.542e-04
A to Z	1.487e-03	5.209e-03	1.046e-02	1.388e-02
B to Z	1.344e-03	4.501e-03	9.127e-03	1.211e-02
C to Z	1.819e-03	6.203e-03	1.259e-02	1.666e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

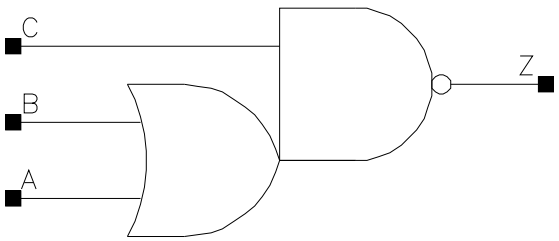
Pin Cycle (vdds)	X3_P0	X10_P0	X20_P0	X26_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X7_P0	0.800	0.952	0.7616
X10_P0	0.800	1.360	1.0880
X13_P0	0.800	1.904	1.5232
X26_P0	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P0	X7_P0	X10_P0	X13_P0
A	0.0006	0.0010	0.0017	0.0022
B	0.0006	0.0011	0.0016	0.0020
C	0.0008	0.0011	0.0016	0.0022
	X26_P0			
A	0.0044			
B	0.0041			
C	0.0043			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X7_P0	X3_P0	X7_P0
A to Z ↓	0.0078	0.0068	3.9839	2.0653
A to Z ↑	0.0125	0.0110	5.4202	2.8037
B to Z ↓	0.0064	0.0051	4.0044	2.0075

B to Z ↑	0.0138	0.0122	5.4477	2.8180
C to Z ↓	0.0080	0.0068	3.7899	1.9211
C to Z ↑	0.0077	0.0065	3.1314	1.6415
	X10_P0	**X13_P0**	**X10_P0**	**X13_P0**
A to Z ↓	0.0066	0.0072	1.3932	1.0688
A to Z ↑	0.0106	0.0112	1.8501	1.4385
B to Z ↓	0.0050	0.0051	1.3884	1.0732
B to Z ↑	0.0117	0.0119	1.8618	1.4452
C to Z ↓	0.0067	0.0069	1.3168	1.0073
C to Z ↑	0.0060	0.0060	1.0827	0.8212
	X26_P0		**X26_P0**	
A to Z ↓	0.0071		0.5516	
A to Z ↑	0.0109		0.7279	
B to Z ↓	0.0050		0.5508	
B to Z ↑	0.0117		0.7318	
C to Z ↓	0.0072		0.5185	
C to Z ↑	0.0060		0.4151	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.823e-04	1.000e-20
X7_P0	5.343e-04	1.000e-20
X10_P0	7.798e-04	1.000e-20
X13_P0	1.014e-03	1.000e-20
X26_P0	1.964e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X7_P0	X10_P0	X13_P0
A (output stable)	2.650e-05	4.875e-05	7.095e-05	1.191e-04
B (output stable)	2.810e-05	5.359e-05	8.055e-05	1.812e-04
C (output stable)	1.618e-04	3.277e-04	4.368e-04	6.361e-04
A to Z	2.229e-03	3.904e-03	5.809e-03	7.827e-03
B to Z	2.029e-03	3.579e-03	5.207e-03	6.856e-03
C to Z	1.971e-03	3.611e-03	5.269e-03	7.135e-03
	X26_P0			
A (output stable)	2.312e-04			
B (output stable)	3.306e-04			
C (output stable)	1.148e-03			
A to Z	1.530e-02			
B to Z	1.334e-02			
C to Z	1.387e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P0	X7_P0	X10_P0	X13_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

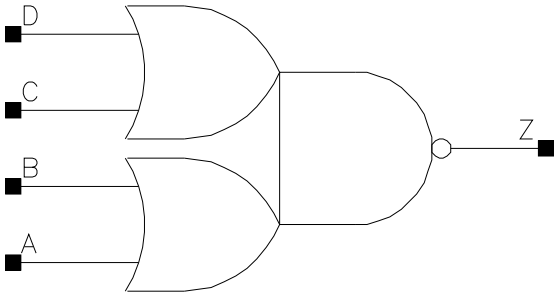
	X26_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X6_P0	0.800	1.360	1.0880
X8_P0	0.800	1.768	1.4144
X11_P0	0.800	2.448	1.9584
X24_P0	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X8_P0	X11_P0
A	0.0005	0.0011	0.0016	0.0021
B	0.0005	0.0010	0.0015	0.0020
C	0.0005	0.0010	0.0015	0.0021
D	0.0005	0.0009	0.0014	0.0019
	X24_P0			
A	0.0046			
B	0.0043			
C	0.0044			
D	0.0041			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	**X6_P0**	**X3_P0**	**X6_P0**
A to Z ↓	0.0067	0.0088	3.7501	2.0292
A to Z ↑	0.0142	0.0134	6.6124	2.9609
B to Z ↓	0.0055	0.0069	3.7208	2.0398
B to Z ↑	0.0156	0.0142	6.6407	2.9714
C to Z ↓	0.0064	0.0086	3.8316	2.0490
C to Z ↑	0.0101	0.0097	6.6384	2.9879
D to Z ↓	0.0049	0.0064	3.7977	2.0749
D to Z ↑	0.0112	0.0101	6.6747	3.0040
	X8_P0	**X11_P0**	**X8_P0**	**X11_P0**
A to Z ↓	0.0083	0.0085	1.3856	1.0514
A to Z ↑	0.0126	0.0126	1.9851	1.4924
B to Z ↓	0.0067	0.0066	1.3955	1.0557
B to Z ↑	0.0136	0.0136	1.9960	1.4995
C to Z ↓	0.0085	0.0088	1.4085	1.0676
C to Z ↑	0.0091	0.0093	1.9847	1.5059
D to Z ↓	0.0066	0.0066	1.4243	1.0744
D to Z ↑	0.0098	0.0099	1.9993	1.5153
	X24_P0		**X24_P0**	
A to Z ↓	0.0087		0.5198	
A to Z ↑	0.0127		0.7280	
B to Z ↓	0.0069		0.5169	
B to Z ↑	0.0138		0.7318	
C to Z ↓	0.0092		0.5287	
C to Z ↑	0.0092		0.7292	
D to Z ↓	0.0069		0.5272	
D to Z ↑	0.0100		0.7343	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.691e-04	1.000e-20
X6_P0	6.362e-04	1.000e-20
X8_P0	9.348e-04	1.000e-20
X11_P0	1.251e-03	1.000e-20
X24_P0	2.370e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X6_P0	X8_P0	X11_P0
A (output stable)	3.100e-05	9.426e-05	1.209e-04	1.691e-04
B (output stable)	3.524e-05	1.771e-04	1.875e-04	2.976e-04
C (output stable)	6.304e-05	1.589e-04	2.048e-04	2.849e-04
D (output stable)	7.166e-05	2.333e-04	2.723e-04	4.095e-04
A to Z	2.012e-03	4.439e-03	6.372e-03	8.526e-03
B to Z	1.836e-03	3.951e-03	5.622e-03	7.569e-03
C to Z	1.631e-03	3.735e-03	5.384e-03	7.255e-03
D to Z	1.470e-03	3.244e-03	4.681e-03	6.335e-03
	X24_P0			
A (output stable)	3.423e-04			
B (output stable)	5.529e-04			
C (output stable)	5.501e-04			
D (output stable)	7.581e-04			

A to Z	1.743e-02			
B to Z	1.547e-02			
C to Z	1.478e-02			
D to Z	1.291e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

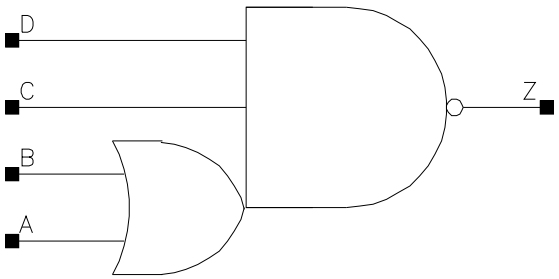
Pin Cycle (vdds)	X3_P0	X6_P0	X8_P0	X11_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P0			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.816	0.6528
X6_P0	0.800	1.360	1.0880
X12_P0	0.800	2.448	1.9584
X18_P0	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X12_P0	X18_P0
A	0.0008	0.0010	0.0020	0.0030
B	0.0005	0.0010	0.0019	0.0029
C	0.0006	0.0011	0.0022	0.0034
D	0.0006	0.0011	0.0022	0.0032

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0140	0.0124	5.3523	2.9032
A to Z ↑	0.0123	0.0099	5.6588	2.8528
B to Z ↓	0.0106	0.0099	5.4067	2.9194
B to Z ↑	0.0122	0.0103	5.6640	2.8681
C to Z ↓	0.0103	0.0101	5.0346	2.7325

C to Z ↑	0.0108	0.0103	2.9861	1.5547
D to Z ↓	0.0119	0.0112	5.0736	2.7477
D to Z ↑	0.0103	0.0091	3.0840	1.5621
	X12_P0	**X18_P0**	**X12_P0**	**X18_P0**
A to Z ↓	0.0127	0.0129	1.5134	1.0249
A to Z ↑	0.0096	0.0096	1.4350	0.9645
B to Z ↓	0.0101	0.0104	1.5234	1.0334
B to Z ↑	0.0101	0.0102	1.4446	0.9710
C to Z ↓	0.0101	0.0102	1.4244	0.9656
C to Z ↑	0.0101	0.0099	0.7969	0.5256
D to Z ↓	0.0113	0.0115	1.4329	0.9709
D to Z ↑	0.0089	0.0088	0.7958	0.5327

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.305e-04	1.000e-20
X6_P0	4.242e-04	1.000e-20
X12_P0	8.045e-04	1.000e-20
X18_P0	1.185e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X6_P0	X12_P0	X18_P0
A (output stable)	7.822e-05	1.529e-04	2.870e-04	3.996e-04
B (output stable)	8.609e-05	1.727e-04	3.140e-04	4.359e-04
C (output stable)	3.143e-05	8.910e-05	1.643e-04	2.563e-04
D (output stable)	4.240e-05	1.465e-04	2.523e-04	3.879e-04
A to Z	2.116e-03	3.693e-03	7.212e-03	1.073e-02
B to Z	1.838e-03	3.205e-03	6.227e-03	9.288e-03
C to Z	2.552e-03	4.728e-03	9.103e-03	1.359e-02
D to Z	2.366e-03	4.251e-03	8.200e-03	1.218e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

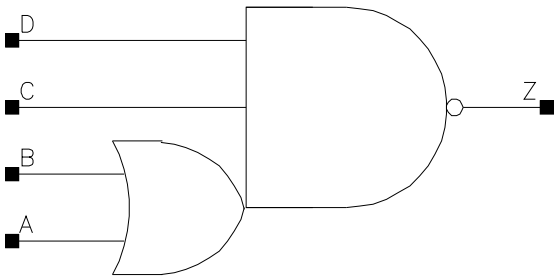
Pin Cycle (vdds)	X3_P0	X6_P0	X12_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P0	0.800	0.680	0.5440
X6_P0	0.800	1.360	1.0880
X9_P0	0.800	1.768	1.4144
X12_P0	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P0	X6_P0	X9_P0	X12_P0
A	0.0006	0.0011	0.0017	0.0022
B	0.0005	0.0010	0.0015	0.0023
C	0.0005	0.0011	0.0016	0.0021
D	0.0006	0.0010	0.0015	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P0	X6_P0	X3_P0	X6_P0
A to Z ↓	0.0098	0.0101	5.7595	2.8688
A to Z ↑	0.0127	0.0133	5.6581	2.8518
B to Z ↓	0.0082	0.0080	5.6375	2.8860
B to Z ↑	0.0140	0.0141	5.6846	2.8633
C to Z ↓	0.0094	0.0099	5.4360	2.7457

C to Z ↑	0.0080	0.0082	3.2540	1.6222
D to Z ↓	0.0103	0.0104	5.4721	2.7590
D to Z ↑	0.0069	0.0065	3.2972	1.6392
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0103	0.0103	1.9698	1.5010
A to Z ↑	0.0127	0.0131	1.8793	1.4744
B to Z ↓	0.0084	0.0082	1.9693	1.5064
B to Z ↑	0.0138	0.0143	1.8882	1.4832
C to Z ↓	0.0099	0.0100	1.8772	1.4323
C to Z ↑	0.0078	0.0080	1.0723	0.8157
D to Z ↓	0.0107	0.0106	1.8876	1.4404
D to Z ↑	0.0063	0.0061	1.0832	0.8262

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P0	2.066e-04	1.000e-20
X6_P0	4.271e-04	1.000e-20
X9_P0	6.121e-04	1.000e-20
X12_P0	8.076e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	1.865e-05	4.137e-05	6.254e-05	8.133e-05
B (output stable)	1.875e-05	5.629e-05	7.833e-05	1.054e-04
C (output stable)	4.627e-05	1.078e-04	1.588e-04	2.077e-04
D (output stable)	7.588e-05	2.706e-04	3.070e-04	4.831e-04
A to Z	2.139e-03	4.484e-03	6.573e-03	8.720e-03
B to Z	1.942e-03	3.967e-03	5.780e-03	7.665e-03
C to Z	1.874e-03	3.938e-03	5.706e-03	7.660e-03
D to Z	1.719e-03	3.574e-03	5.240e-03	6.903e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

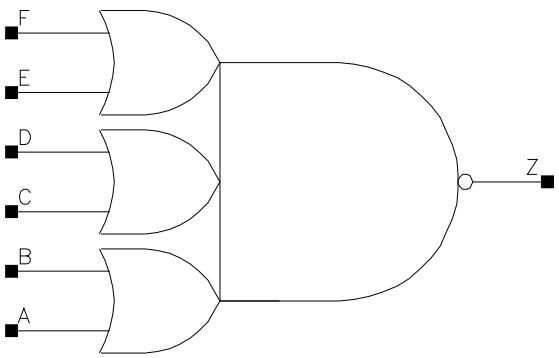
Pin Cycle (vdds)	X3_P0	X6_P0	X9_P0	X12_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.224	0.9792
X3_P0	0.800	1.224	0.9792
X5_P0	0.800	2.040	1.6320
X8_P0	0.800	2.720	2.1760
X10_P0	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P0	X3_P0	X5_P0	X8_P0
A	0.0005	0.0006	0.0011	0.0017
B	0.0005	0.0006	0.0010	0.0016
C	0.0004	0.0006	0.0011	0.0016
D	0.0005	0.0005	0.0010	0.0015

E	0.0004	0.0005	0.0010	0.0015
F	0.0004	0.0005	0.0010	0.0015
	X10_P0			
A	0.0022			
B	0.0021			
C	0.0021			
D	0.0020			
E	0.0020			
F	0.0020			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X3_P0**	**X2_P0**	**X3_P0**
A to Z ↓	0.0128	0.0125	6.2582	4.9306
A to Z ↑	0.0188	0.0163	7.5950	5.3367
B to Z ↓	0.0117	0.0114	6.2813	4.9641
B to Z ↑	0.0206	0.0181	7.6198	5.3578
C to Z ↓	0.0134	0.0134	6.3099	4.9592
C to Z ↑	0.0163	0.0145	7.6119	5.4419
D to Z ↓	0.0126	0.0119	6.3873	5.0338
D to Z ↑	0.0185	0.0158	7.6565	5.4621
E to Z ↓	0.0126	0.0127	6.3501	4.9819
E to Z ↑	0.0128	0.0113	7.6209	5.4568
F to Z ↓	0.0115	0.0113	6.4278	5.0688
F to Z ↑	0.0144	0.0125	7.6675	5.4893
	X5_P0	**X8_P0**	**X5_P0**	**X8_P0**
A to Z ↓	0.0136	0.0133	2.6482	1.8017
A to Z ↑	0.0168	0.0161	2.8509	1.8839
B to Z ↓	0.0117	0.0115	2.6661	1.8054
B to Z ↑	0.0178	0.0175	2.8591	1.8918
C to Z ↓	0.0134	0.0138	2.6703	1.8163
C to Z ↑	0.0142	0.0139	2.8830	1.9375
D to Z ↓	0.0116	0.0118	2.6813	1.8245
D to Z ↑	0.0152	0.0154	2.8967	1.9469
E to Z ↓	0.0136	0.0135	2.6976	1.8268
E to Z ↑	0.0112	0.0108	2.8922	1.9445
F to Z ↓	0.0114	0.0114	2.7134	1.8358
F to Z ↑	0.0119	0.0119	2.9086	1.9577
	X10_P0		**X10_P0**	
A to Z ↓	0.0137		1.3725	
A to Z ↑	0.0163		1.4362	
B to Z ↓	0.0118		1.3768	
B to Z ↑	0.0176		1.4417	
C to Z ↓	0.0137		1.3825	
C to Z ↑	0.0140		1.4678	
D to Z ↓	0.0118		1.3875	
D to Z ↑	0.0152		1.4759	
E to Z ↓	0.0138		1.3928	
E to Z ↑	0.0110		1.4665	
F to Z ↓	0.0118		1.4028	
F to Z ↑	0.0119		1.4762	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P0	2.474e-04	1.000e-20
X3_P0	3.922e-04	1.000e-20
X5_P0	7.201e-04	1.000e-20
X8_P0	1.037e-03	1.000e-20
X10_P0	1.368e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P0	X3_P0	X5_P0	X8_P0
A (output stable)	2.716e-05	3.405e-05	8.795e-05	1.200e-04
B (output stable)	2.979e-05	3.806e-05	1.395e-04	1.656e-04
C (output stable)	4.037e-05	5.092e-05	1.170e-04	1.604e-04
D (output stable)	4.431e-05	5.394e-05	1.635e-04	1.949e-04
E (output stable)	9.333e-05	1.174e-04	2.123e-04	3.126e-04
F (output stable)	9.856e-05	1.235e-04	2.593e-04	3.512e-04
A to Z	2.321e-03	2.898e-03	5.677e-03	8.262e-03
B to Z	2.179e-03	2.704e-03	5.145e-03	7.512e-03
C to Z	1.998e-03	2.524e-03	4.852e-03	7.088e-03
D to Z	1.878e-03	2.336e-03	4.398e-03	6.482e-03
E to Z	1.690e-03	2.168e-03	4.233e-03	6.110e-03
F to Z	1.569e-03	1.989e-03	3.766e-03	5.514e-03
	X10_P0			
A (output stable)	1.673e-04			
B (output stable)	2.542e-04			
C (output stable)	2.184e-04			
D (output stable)	3.005e-04			
E (output stable)	4.022e-04			
F (output stable)	4.785e-04			
A to Z	1.105e-02			
B to Z	1.001e-02			
C to Z	9.471e-03			
D to Z	8.577e-03			
E to Z	8.245e-03			
F to Z	7.373e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X2_P0	X3_P0	X5_P0	X8_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P0			

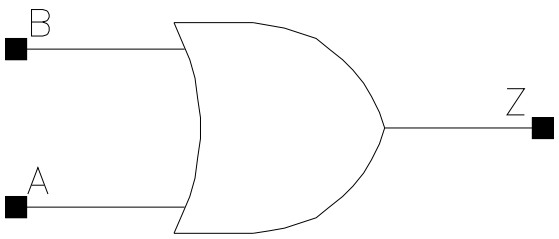
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.544	0.4352
X9_P0	0.800	0.680	0.5440
X19_P0	0.800	1.360	1.0880
X29_P0	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P0	X9_P0	X19_P0	X29_P0
A	0.0005	0.0007	0.0011	0.0011
B	0.0005	0.0006	0.0012	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X9_P0**	**X5_P0**	**X9_P0**
A to Z ↓	0.0208	0.0183	2.5770	1.2950
A to Z ↑	0.0131	0.0146	3.0916	1.5497
B to Z ↓	0.0223	0.0196	2.5754	1.2932
B to Z ↑	0.0121	0.0135	3.0923	1.5512
	X19_P0	**X29_P0**	**X19_P0**	**X29_P0**
A to Z ↓	0.0185	0.0220	0.6231	0.4245
A to Z ↑	0.0148	0.0172	0.7395	0.4976
B to Z ↓	0.0194	0.0230	0.6229	0.4244
B to Z ↑	0.0130	0.0156	0.7399	0.4967

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	2.435e-04	1.000e-20
X9_P0	5.015e-04	1.000e-20
X19_P0	9.935e-04	1.000e-20
X29_P0	1.252e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X9_P0	X19_P0	X29_P0
A (output stable)	1.911e-05	3.782e-05	1.145e-04	1.168e-04
B (output stable)	2.784e-05	4.605e-05	2.558e-04	2.570e-04
A to Z	2.895e-03	4.958e-03	1.047e-02	1.529e-02
B to Z	2.788e-03	4.809e-03	9.898e-03	1.471e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

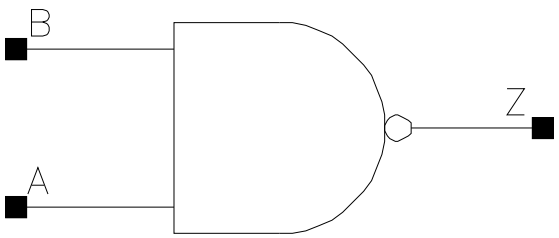
Pin Cycle (vdds)	X5_P0	X9_P0	X19_P0	X29_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.816	0.6528
X9_P0	0.800	0.952	0.7616
X14_P0	0.800	1.088	0.8704
X18_P0	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P0	X9_P0	X14_P0	X18_P0
A	0.0007	0.0006	0.0006	0.0006
B	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X9_P0**	**X5_P0**	**X9_P0**
A to Z ↓	0.0174	0.0199	2.3553	1.2780
A to Z ↑	0.0187	0.0208	2.9692	1.5666
B to Z ↓	0.0188	0.0217	2.3520	1.2778
B to Z ↑	0.0173	0.0198	2.9650	1.5671
	X14_P0	**X18_P0**	**X14_P0**	**X18_P0**
A to Z ↓	0.0220	0.0235	0.8800	0.6639
A to Z ↑	0.0225	0.0233	1.0288	0.8050
B to Z ↓	0.0237	0.0251	0.8796	0.6639
B to Z ↑	0.0215	0.0224	1.0277	0.8045

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	6.881e-04	1.000e-20
X9_P0	7.941e-04	1.000e-20
X14_P0	9.348e-04	1.000e-20
X18_P0	1.012e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X9_P0	X14_P0	X18_P0
A (output stable)	2.168e-05	1.968e-05	2.068e-05	1.986e-05
B (output stable)	3.336e-05	3.068e-05	3.068e-05	2.918e-05
A to Z	4.871e-03	6.218e-03	8.036e-03	9.431e-03
B to Z	4.731e-03	6.067e-03	7.885e-03	9.270e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

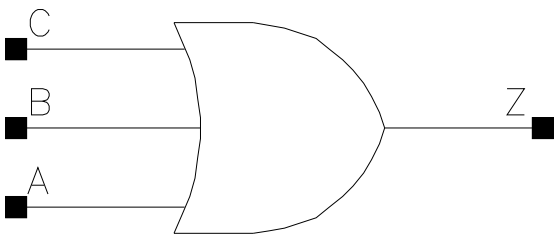
Pin Cycle (vdds)	X5_P0	X9_P0	X14_P0	X18_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.680	0.5440
X10_P0	0.800	0.952	0.7616
X14_P0	0.800	1.496	1.1968
X19_P0	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0005	0.0007	0.0011	0.0018
B	0.0004	0.0007	0.0013	0.0018
C	0.0005	0.0007	0.0012	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0260	0.0238	2.6442	1.2574
A to Z ↑	0.0155	0.0137	3.1035	1.4731
B to Z ↓	0.0271	0.0250	2.6441	1.2575
B to Z ↑	0.0150	0.0129	3.1095	1.4733
C to Z ↓	0.0284	0.0258	2.6438	1.2582
C to Z ↑	0.0141	0.0118	3.1116	1.4740
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**
A to Z ↓	0.0223	0.0219	0.8470	0.6492

A to Z ↑	0.0126	0.0123	1.0106	0.7814
B to Z ↓	0.0237	0.0228	0.8475	0.6495
B to Z ↑	0.0115	0.0118	1.0094	0.7798
C to Z ↓	0.0233	0.0234	0.8455	0.6490
C to Z ↑	0.0100	0.0103	1.0092	0.7790

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	2.009e-04	1.000e-20
X10_P0	4.218e-04	1.000e-20
X14_P0	7.004e-04	1.000e-20
X19_P0	9.565e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	2.077e-05	3.797e-05	8.061e-05	1.372e-04
B (output stable)	2.655e-05	4.592e-05	1.144e-04	1.655e-04
C (output stable)	4.955e-05	8.676e-05	3.024e-04	3.412e-04
A to Z	3.320e-03	5.864e-03	9.355e-03	1.315e-02
B to Z	3.206e-03	5.687e-03	9.004e-03	1.237e-02
C to Z	3.113e-03	5.505e-03	8.406e-03	1.173e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

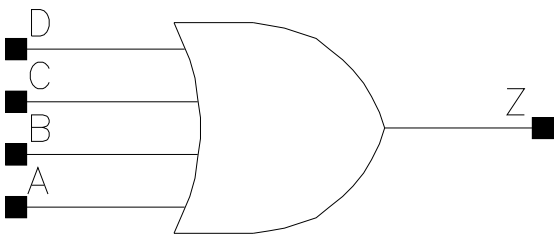
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	0.800	1.224	0.9792
X8_P0	0.800	1.496	1.1968
X12_P0	0.800	2.176	1.7408
X15_P0	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P0	X8_P0	X12_P0	X15_P0
A	0.0004	0.0006	0.0011	0.0012
B	0.0005	0.0007	0.0010	0.0013
C	0.0004	0.0006	0.0011	0.0013
D	0.0005	0.0007	0.0010	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X8_P0	X4_P0	X8_P0
A to Z ↓	0.0219	0.0211	3.7876	2.0159
A to Z ↑	0.0133	0.0142	2.8541	1.5489
B to Z ↓	0.0237	0.0227	3.7878	2.0146
B to Z ↑	0.0124	0.0133	2.8579	1.5493
C to Z ↓	0.0236	0.0210	3.7922	2.0107
C to Z ↑	0.0140	0.0139	2.9468	1.5568

D to Z ↓	0.0257	0.0228	3.7911	2.0094
D to Z ↑	0.0133	0.0131	2.9487	1.5556
	X12_P0	**X15_P0**	**X12_P0**	**X15_P0**
A to Z ↓	0.0209	0.0215	1.3897	1.0441
A to Z ↑	0.0143	0.0138	0.9859	0.7625
B to Z ↓	0.0220	0.0225	1.3894	1.0435
B to Z ↑	0.0132	0.0123	0.9857	0.7625
C to Z ↓	0.0207	0.0211	1.3877	1.0420
C to Z ↑	0.0136	0.0132	0.9809	0.7665
D to Z ↓	0.0218	0.0222	1.3872	1.0412
D to Z ↑	0.0126	0.0119	0.9804	0.7674

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	2.837e-04	1.000e-20
X8_P0	6.316e-04	1.000e-20
X12_P0	8.337e-04	1.000e-20
X15_P0	1.161e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	6.870e-04	1.236e-03	1.837e-03	2.482e-03
B (output stable)	6.495e-04	1.159e-03	1.716e-03	2.330e-03
C (output stable)	6.776e-04	1.182e-03	1.725e-03	2.324e-03
D (output stable)	6.413e-04	1.106e-03	1.606e-03	2.191e-03
A to Z	3.017e-03	5.810e-03	8.297e-03	1.115e-02
B to Z	2.914e-03	5.620e-03	7.931e-03	1.055e-02
C to Z	3.071e-03	5.440e-03	7.783e-03	1.020e-02
D to Z	2.977e-03	5.257e-03	7.413e-03	9.682e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

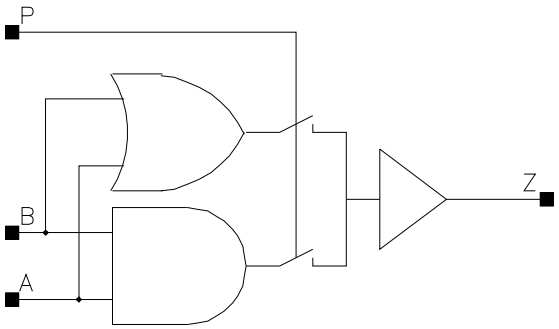
Pin Cycle (vdds)	X4_P0	X8_P0	X12_P0	X15_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	0.800	0.952	0.7616
X10_P0	1.600	0.816	1.3056
X14_P0	1.600	1.224	1.9584
X19_P0	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P0	X10_P0	X14_P0	X19_P0
A	0.0009	0.0011	0.0021	0.0021
B	0.0009	0.0012	0.0022	0.0023
P	0.0005	0.0007	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
A to Z ↓	0.0251	0.0230	2.6104	1.2174
A to Z ↑	0.0143	0.0182	3.1201	1.4877
B to Z ↓	0.0255	0.0240	2.6173	1.2216
B to Z ↑	0.0152	0.0194	3.1251	1.4904
P to Z ↓	0.0245	0.0237	2.6103	1.2199
P to Z ↑	0.0150	0.0195	3.1183	1.4867
	X14_P0	**X19_P0**	**X14_P0**	**X19_P0**

A to Z ↓	0.0212	0.0228	0.8410	0.6285
A to Z ↑	0.0177	0.0183	1.0270	0.7636
B to Z ↓	0.0209	0.0225	0.8475	0.6320
B to Z ↑	0.0179	0.0188	1.0272	0.7641
P to Z ↓	0.0218	0.0234	0.8462	0.6304
P to Z ↑	0.0186	0.0195	1.0252	0.7634

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	3.530e-04	1.000e-20
X10_P0	8.011e-04	1.000e-20
X14_P0	1.308e-03	1.000e-20
X19_P0	1.551e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	4.866e-05	7.373e-05	1.904e-04	1.846e-04
B (output stable)	5.756e-05	9.486e-05	3.635e-04	3.507e-04
P (output stable)	1.440e-04	2.251e-04	4.323e-04	3.978e-04
A to Z	3.293e-03	6.551e-03	1.033e-02	1.261e-02
B to Z	3.226e-03	6.517e-03	1.001e-02	1.228e-02
P to Z	3.076e-03	6.350e-03	1.007e-02	1.239e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

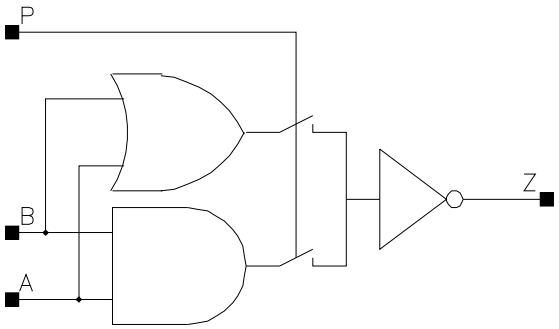
Pin Cycle (vdds)	X5_P0	X10_P0	X14_P0	X19_P0
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.600	0.544	0.8704
X10_P0	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P0	X10_P0
A	0.0010	0.0020
B	0.0010	0.0018
P	0.0007	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X10_P0	X5_P0	X10_P0
A to Z ↓	0.0089	0.0080	3.8577	2.0211
A to Z ↑	0.0136	0.0123	5.4469	2.7883
B to Z ↓	0.0096	0.0081	3.8200	2.0307
B to Z ↑	0.0140	0.0117	5.4302	2.8349
P to Z ↓	0.0101	0.0089	3.9090	2.0438
P to Z ↑	0.0141	0.0122	5.4929	2.8062

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	3.605e-04	1.000e-20
X10_P0	6.719e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P0	X10_P0
A (output stable)	6.947e-05	1.891e-04
B (output stable)	8.451e-05	3.492e-04
P (output stable)	1.904e-04	4.352e-04
A to Z	2.406e-03	4.379e-03
B to Z	2.291e-03	3.960e-03
P to Z	2.097e-03	3.781e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

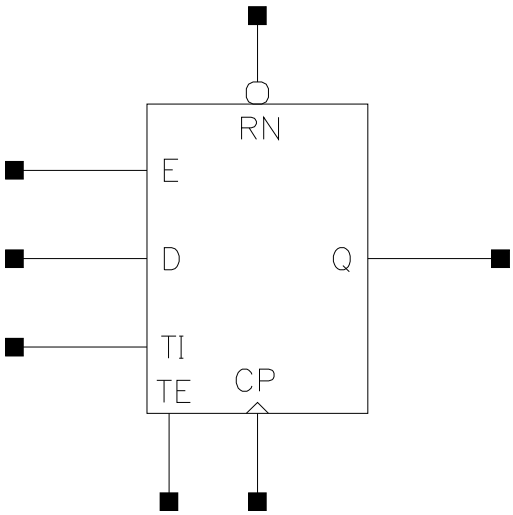
Pin Cycle (vdds)	X5_P0	X10_P0
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.600	2.992	4.7872
X10_P0	1.600	3.128	5.0048
X19_P0	1.600	3.264	5.2224
X23_P0	1.600	3.264	5.2224
X29_P0	1.600	3.536	5.6576
X34_P0	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0	X23_P0
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0012	0.0012	0.0012	0.0012

RN	0.0009	0.0009	0.0009	0.0009
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P0	X34_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0012	0.0012		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
CP to Q ↓	0.0339	0.0541	2.3822	1.2039
CP to Q ↑	0.0454	0.0688	2.9036	1.4903
RN to Q ↓	0.0314	0.0473	2.3140	1.2034
	X19_P0	**X23_P0**	**X19_P0**	**X23_P0**
CP to Q ↓	0.0586	0.0590	0.6212	0.4724
CP to Q ↑	0.0722	0.0709	0.7490	0.7310
RN to Q ↓	0.0520	0.0525	0.6213	0.4723
	X29_P0	**X34_P0**	**X29_P0**	**X34_P0**
CP to Q ↓	0.0499	0.0492	0.4132	0.3264
CP to Q ↑	0.0597	0.0603	0.4983	0.4974
RN to Q ↓	0.0460	0.0454	0.4127	0.3260

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P0	X10_P0	X19_P0	X23_P0
CP ↓	min_pulse_width to CP	0.0393	0.0393	0.0393	0.0393
CP ↑	min_pulse_width to CP	0.0318	0.0317	0.0318	0.0317
D ↓	hold_rising to CP	-0.0121	-0.0121	-0.0121	-0.0121
D ↑	hold_rising to CP	-0.0002	-0.0002	-0.0002	-0.0002
D ↓	setup_rising to CP	0.0387	0.0387	0.0387	0.0387
D ↑	setup_rising to CP	0.0271	0.0271	0.0271	0.0271
E ↓	hold_rising to CP	-0.0191	-0.0191	-0.0191	-0.0191
E ↑	hold_rising to CP	-0.0025	-0.0025	-0.0025	-0.0025
E ↓	setup_rising to CP	0.0564	0.0564	0.0564	0.0564
E ↑	setup_rising to CP	0.0422	0.0422	0.0422	0.0422
RN ↓	min_pulse_width to RN	0.0376	0.0354	0.0354	0.0376
RN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
RN ↑	removal_rising to CP	0.0091	0.0091	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0039	-0.0039	-0.0039	-0.0013

TE ↑	hold_rising to CP	-0.0000	-0.0000	-0.0000	-0.0000
TE ↓	setup_rising to CP	0.0370	0.0370	0.0370	0.0370
TE ↑	setup_rising to CP	0.0364	0.0364	0.0364	0.0364
TI ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120	-0.0120
TI ↑	hold_rising to CP	0.0034	0.0034	0.0034	0.0034
TI ↓	setup_rising to CP	0.0403	0.0403	0.0403	0.0403
TI ↑	setup_rising to CP	0.0209	0.0209	0.0209	0.0209
		X29_P0	X34_P0		
CP ↓	min_pulse_width to CP	0.0393	0.0393		
CP ↑	min_pulse_width to CP	0.0317	0.0317		
D ↓	hold_rising to CP	-0.0121	-0.0121		
D ↑	hold_rising to CP	-0.0002	-0.0002		
D ↓	setup_rising to CP	0.0387	0.0387		
D ↑	setup_rising to CP	0.0271	0.0271		
E ↓	hold_rising to CP	-0.0191	-0.0191		
E ↑	hold_rising to CP	-0.0025	-0.0025		
E ↓	setup_rising to CP	0.0564	0.0564		
E ↑	setup_rising to CP	0.0422	0.0422		
RN ↓	min_pulse_width to RN	0.0376	0.0376		
RN ↑	recovery_rising to CP	-0.0017	-0.0017		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0013	-0.0013		
TE ↑	hold_rising to CP	-0.0000	-0.0000		
TE ↓	setup_rising to CP	0.0370	0.0370		
TE ↑	setup_rising to CP	0.0364	0.0364		
TI ↓	hold_rising to CP	-0.0120	-0.0120		
TI ↑	hold_rising to CP	0.0034	0.0034		
TI ↓	setup_rising to CP	0.0403	0.0403		
TI ↑	setup_rising to CP	0.0209	0.0209		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	1.437e-03	1.000e-20
X10_P0	1.786e-03	1.000e-20
X19_P0	2.428e-03	1.000e-20
X23_P0	2.473e-03	1.000e-20

X29_P0	3.313e-03	1.000e-20
X34_P0	3.390e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

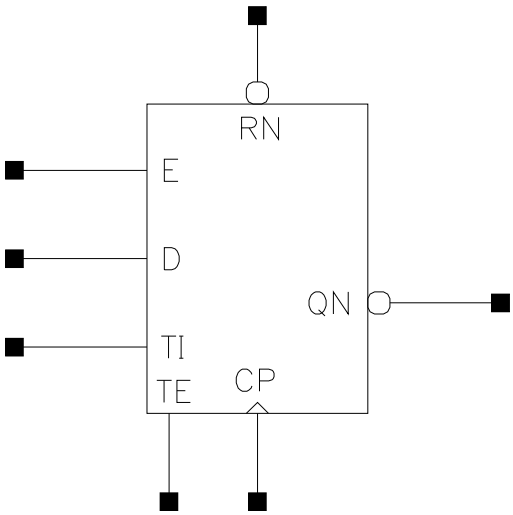
Pin Cycle	X5_P0	X10_P0	X19_P0	X23_P0
Clock 100Mhz Data 0Mhz	1.061e-02	1.060e-02	1.061e-02	1.061e-02
Clock 100Mhz Data 25Mhz	1.113e-02	1.177e-02	1.300e-02	1.310e-02
Clock 100Mhz Data 50Mhz	1.164e-02	1.295e-02	1.539e-02	1.559e-02
Clock = 0 Data 100Mhz	6.514e-03	6.514e-03	6.510e-03	6.510e-03
Clock = 1 Data 100Mhz	2.419e-03	2.417e-03	2.416e-03	2.416e-03
	X29_P0	X34_P0		
Clock 100Mhz Data 0Mhz	1.061e-02	1.061e-02		
Clock 100Mhz Data 25Mhz	1.392e-02	1.424e-02		
Clock 100Mhz Data 50Mhz	1.724e-02	1.786e-02		
Clock = 0 Data 100Mhz	6.509e-03	6.510e-03		
Clock = 1 Data 100Mhz	2.416e-03	2.417e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.600	2.992	4.7872
X10_P0	1.600	3.128	5.0048
X19_P0	1.600	3.264	5.2224
X23_P0	1.600	3.264	5.2224
X29_P0	1.600	3.536	5.6576
X34_P0	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P0	X10_P0	X19_P0	X23_P0
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
E	0.0012	0.0013	0.0013	0.0013

RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P0	X34_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
E	0.0013	0.0012		
RN	0.0009	0.0009		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	**X10_P0**	**X5_P0**	**X10_P0**
CP to QN ↓	0.0603	0.0537	2.3759	1.2031
CP to QN ↑	0.0462	0.0426	2.8936	1.4934
RN to QN ↑	0.0394	0.0371	2.8945	1.4919
	X19_P0	**X23_P0**	**X19_P0**	**X23_P0**
CP to QN ↓	0.0567	0.0574	0.6156	0.4731
CP to QN ↑	0.0466	0.0451	0.7497	0.7310
RN to QN ↑	0.0422	0.0406	0.7474	0.7309
	X29_P0	**X34_P0**	**X29_P0**	**X34_P0**
CP to QN ↓	0.0755	0.0739	0.4133	0.3216
CP to QN ↑	0.0610	0.0604	0.4993	0.4978
RN to QN ↑	0.0543	0.0538	0.4991	0.4975

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P0	X10_P0	X19_P0	X23_P0
CP ↓	min_pulse_width to CP	0.0393	0.0393	0.0393	0.0393
CP ↑	min_pulse_width to CP	0.0317	0.0317	0.0317	0.0317
D ↓	hold_rising to CP	-0.0121	-0.0121	-0.0121	-0.0121
D ↑	hold_rising to CP	-0.0002	-0.0002	-0.0002	-0.0002
D ↓	setup_rising to CP	0.0387	0.0387	0.0387	0.0387
D ↑	setup_rising to CP	0.0271	0.0271	0.0271	0.0271
E ↓	hold_rising to CP	-0.0191	-0.0191	-0.0191	-0.0191
E ↑	hold_rising to CP	-0.0025	-0.0025	-0.0025	-0.0025
E ↓	setup_rising to CP	0.0564	0.0564	0.0564	0.0564
E ↑	setup_rising to CP	0.0422	0.0422	0.0422	0.0422
RN ↓	min_pulse_width to RN	0.0354	0.0376	0.0376	0.0376
RN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
RN ↑	removal_rising to CP	0.0091	0.0091	0.0091	0.0091
TE ↓	hold_rising to CP	-0.0039	-0.0039	-0.0013	-0.0013

TE ↑	hold_rising to CP	-0.0000	-0.0000	-0.0000	-0.0000
TE ↓	setup_rising to CP	0.0370	0.0370	0.0370	0.0370
TE ↑	setup_rising to CP	0.0364	0.0396	0.0396	0.0396
TI ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120	-0.0120
TI ↑	hold_rising to CP	0.0034	0.0034	0.0034	0.0034
TI ↓	setup_rising to CP	0.0403	0.0403	0.0403	0.0403
TI ↑	setup_rising to CP	0.0209	0.0209	0.0209	0.0209
		X29_P0	X34_P0		
CP ↓	min_pulse_width to CP	0.0393	0.0393		
CP ↑	min_pulse_width to CP	0.0318	0.0317		
D ↓	hold_rising to CP	-0.0121	-0.0121		
D ↑	hold_rising to CP	-0.0002	-0.0002		
D ↓	setup_rising to CP	0.0387	0.0387		
D ↑	setup_rising to CP	0.0271	0.0271		
E ↓	hold_rising to CP	-0.0191	-0.0191		
E ↑	hold_rising to CP	-0.0025	-0.0025		
E ↓	setup_rising to CP	0.0564	0.0564		
E ↑	setup_rising to CP	0.0422	0.0422		
RN ↓	min_pulse_width to RN	0.0354	0.0354		
RN ↑	recovery_rising to CP	-0.0017	-0.0017		
RN ↑	removal_rising to CP	0.0091	0.0091		
TE ↓	hold_rising to CP	-0.0013	-0.0039		
TE ↑	hold_rising to CP	-0.0000	-0.0000		
TE ↓	setup_rising to CP	0.0370	0.0370		
TE ↑	setup_rising to CP	0.0364	0.0364		
TI ↓	hold_rising to CP	-0.0120	-0.0120		
TI ↑	hold_rising to CP	0.0034	0.0034		
TI ↓	setup_rising to CP	0.0403	0.0403		
TI ↑	setup_rising to CP	0.0209	0.0209		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P0	1.358e-03	1.000e-20
X10_P0	1.668e-03	1.000e-20
X19_P0	2.189e-03	1.000e-20
X23_P0	2.261e-03	1.000e-20

X29_P0	2.873e-03	1.000e-20
X34_P0	2.998e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

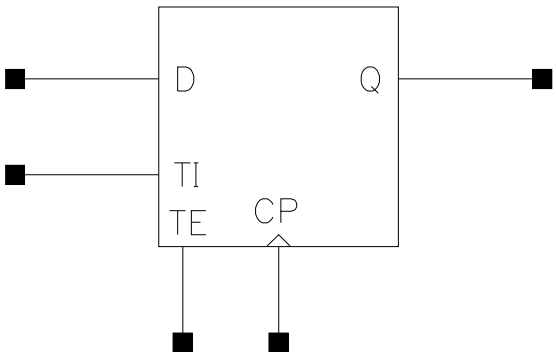
Pin Cycle	X5_P0	X10_P0	X19_P0	X23_P0
Clock 100Mhz Data 0Mhz	1.059e-02	1.060e-02	1.060e-02	1.060e-02
Clock 100Mhz Data 25Mhz	1.116e-02	1.172e-02	1.299e-02	1.315e-02
Clock 100Mhz Data 50Mhz	1.173e-02	1.285e-02	1.537e-02	1.570e-02
Clock = 0 Data 100Mhz	6.509e-03	6.511e-03	6.510e-03	6.508e-03
Clock = 1 Data 100Mhz	2.419e-03	2.416e-03	2.415e-03	2.414e-03
	X29_P0	X34_P0		
Clock 100Mhz Data 0Mhz	1.061e-02	1.060e-02		
Clock 100Mhz Data 25Mhz	1.395e-02	1.424e-02		
Clock 100Mhz Data 50Mhz	1.730e-02	1.788e-02		
Clock = 0 Data 100Mhz	6.509e-03	6.509e-03		
Clock = 1 Data 100Mhz	2.416e-03	2.417e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P0	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P0	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P0	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P0	C8T28SOI_LLHF_-SDFPQX3_P0	C8T28SOIDV_LL_-SDFPQX5_P0	C8T28SOIDV_LL_-SDFPQX10_P0
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P0	C8T28SOIDV_LL_-SDFPQX23_P0	C8T28SOIDV_LL_-SDFPQX29_P0	
CP	0.0005	0.0005	0.0005	
D	0.0005	0.0005	0.0005	
TE	0.0009	0.0009	0.0009	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P0	**C8T28SOI_LLHF_-SDFPQX3_P0**	**C8T28SOI_LL_-SDFPQX5_P0**	**C8T28SOI_LLHF_-SDFPQX3_P0**
CP to Q ↓	0.0342	0.0290	2.4778	3.7606
CP to Q ↑	0.0339	0.0375	2.9442	4.3950
	C8T28SOIDV_LL_-SDFPQX5_P0	**C8T28SOIDV_LL_-SDFPQX10_P0**	**C8T28SOIDV_LL_-SDFPQX5_P0**	**C8T28SOIDV_LL_-SDFPQX10_P0**
CP to Q ↓	0.0315	0.0441	2.3713	1.1725
CP to Q ↑	0.0388	0.0546	2.9035	1.4651
	C8T28SOIDV_LL_-SDFPQX19_P0	**C8T28SOIDV_LL_-SDFPQX23_P0**	**C8T28SOIDV_LL_-SDFPQX19_P0**	**C8T28SOIDV_LL_-SDFPQX23_P0**
CP to Q ↓	0.0477	0.0490	0.6044	0.4698
CP to Q ↑	0.0583	0.0599	0.7394	0.7338
	C8T28SOIDV_LL_-SDFPQX29_P0		**C8T28SOIDV_LL_-SDFPQX29_P0**	
CP to Q ↓	0.0470		0.4064	
CP to Q ↑	0.0559		0.4922	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P0	C8T28SOI_-LLHF_-SDFPQX3_P0	C8T28SOIDV_-LL_SDFPQX5_-P0	C8T28SOIDV_-LL_SDFPQX10_-P0
CP ↓	min_pulse_width to CP	0.0490	0.0493	0.0400	0.0400
CP ↑	min_pulse_width to CP	0.0283	0.0236	0.0270	0.0271
D ↓	hold_rising to CP	-0.0147	-0.0376	0.0053	0.0053
D ↑	hold_rising to CP	0.0030	0.0054	0.0074	0.0074
D ↓	setup_rising to CP	0.0392	0.0730	0.0246	0.0246
D ↑	setup_rising to CP	0.0217	0.0217	0.0178	0.0178
TE ↓	hold_rising to CP	-0.0066	-0.0116	0.0070	0.0070
TE ↑	hold_rising to CP	0.0056	0.0055	0.0027	0.0027
TE ↓	setup_rising to CP	0.0370	0.0558	0.0242	0.0242
TE ↑	setup_rising to CP	0.0440	0.0635	0.0445	0.0445

TI ↓	hold_rising to CP	-0.0217	-0.0396	-0.0153	-0.0153
TI ↑	hold_rising to CP	0.0041	0.0044	0.0041	0.0041
TI ↓	setup_rising to CP	0.0500	0.0643	0.0451	0.0451
TI ↑	setup_rising to CP	0.0208	0.0195	0.0224	0.0224
		C8T28SOIDV_-LL_SDFPQX19_-P0	C8T28SOIDV_-LL_SDFPQX23_-P0	C8T28SOIDV_-LL_SDFPQX29_-P0	
CP ↓	min_pulse_width to CP	0.0400	0.0400	0.0400	
CP ↑	min_pulse_width to CP	0.0271	0.0270	0.0270	
D ↓	hold_rising to CP	0.0053	0.0053	0.0053	
D ↑	hold_rising to CP	0.0074	0.0074	0.0074	
D ↓	setup_rising to CP	0.0246	0.0246	0.0246	
D ↑	setup_rising to CP	0.0178	0.0178	0.0178	
TE ↓	hold_rising to CP	0.0070	0.0070	0.0070	
TE ↑	hold_rising to CP	0.0027	0.0027	0.0027	
TE ↓	setup_rising to CP	0.0242	0.0242	0.0242	
TE ↑	setup_rising to CP	0.0445	0.0445	0.0445	
TI ↓	hold_rising to CP	-0.0169	-0.0169	-0.0169	
TI ↑	hold_rising to CP	0.0041	0.0041	0.0041	
TI ↓	setup_rising to CP	0.0451	0.0451	0.0467	
TI ↑	setup_rising to CP	0.0224	0.0224	0.0224	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P0	1.147e-03	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P0	9.960e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P0	1.096e-03	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P0	1.527e-03	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P0	1.934e-03	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P0	2.008e-03	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P0	2.620e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P0	C8T28SOI_LLHF_-SDFPQX3_P0	C8T28SOIDV_LL_-SDFPQX5_P0	C8T28SOIDV_LL_-SDFPQX10_P0
Clock 100Mhz Data 0Mhz	1.103e-02	1.052e-02	9.977e-03	9.703e-03
Clock 100Mhz Data 25Mhz	1.076e-02	1.022e-02	9.868e-03	1.020e-02
Clock 100Mhz Data 50Mhz	1.049e-02	9.930e-03	9.760e-03	1.070e-02

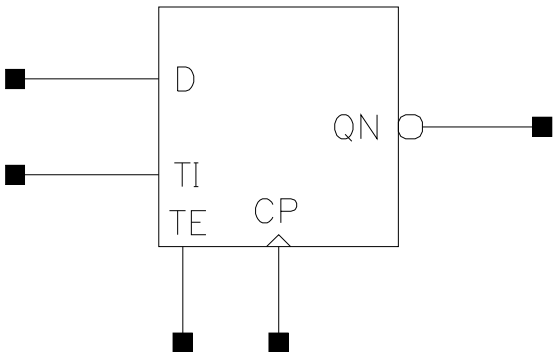
Clock = 0 Data 100Mhz	5.552e-03	5.843e-03	5.464e-03	5.270e-03
Clock = 1 Data 100Mhz	4.625e-05	6.586e-04	4.557e-04	3.543e-04
	C8T28SOIDV_LL_-SDFPQX19_P0	C8T28SOIDV_LL_-SDFPQX23_P0	C8T28SOIDV_LL_-SDFPQX29_P0	
Clock 100Mhz Data 0Mhz	9.541e-03	9.435e-03	9.360e-03	
Clock 100Mhz Data 25Mhz	1.108e-02	1.116e-02	1.191e-02	
Clock 100Mhz Data 50Mhz	1.262e-02	1.289e-02	1.445e-02	
Clock = 0 Data 100Mhz	5.152e-03	5.073e-03	5.018e-03	
Clock = 1 Data 100Mhz	2.939e-04	2.530e-04	2.241e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P0	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P0	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P0	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P0	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P0	C8T28SOI_LLHF_-SDFPQNX3_P0	C8T28SOIDV_LL_-SDFPQNX5_P0	C8T28SOIDV_LL_-SDFPQNX10_P0

CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P0	C8T28SOIDV_LL_-SDFPQNX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P0	**C8T28SOI_LLHF_-SDFPQNX3_P0**	**C8T28SOI_LL_-SDFPQNX5_P0**	**C8T28SOI_LLHF_-SDFPQNX3_P0**
CP to QN ↓	0.0424	0.0443	2.4270	3.6051
CP to QN ↑	0.0379	0.0356	3.1624	4.2641
	C8T28SOIDV_LL_-SDFPQNX5_P0	**C8T28SOIDV_LL_-SDFPQNX10_P0**	**C8T28SOIDV_LL_-SDFPQNX5_P0**	**C8T28SOIDV_LL_-SDFPQNX10_P0**
CP to QN ↓	0.0467	0.0449	2.3561	1.1784
CP to QN ↑	0.0362	0.0384	2.8711	1.4668
	C8T28SOIDV_LL_-SDFPQNX19_P0	**C8T28SOIDV_LL_-SDFPQNX29_P0**	**C8T28SOIDV_LL_-SDFPQNX19_P0**	**C8T28SOIDV_LL_-SDFPQNX29_P0**
CP to QN ↓	0.0503	0.0587	0.6094	0.4168
CP to QN ↑	0.0452	0.0512	0.7529	0.4932

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P0	C8T28SOI_-LLHF_-SDFPQNX3_P0	C8T28SOIDV_-LL_SDFPQNX5_-P0	C8T28SOIDV_-LL_-SDFPQNX10_P0
CP ↓	min_pulse_width to CP	0.0490	0.0493	0.0400	0.0401
CP ↑	min_pulse_width to CP	0.0270	0.0224	0.0271	0.0270
D ↓	hold_rising to CP	-0.0147	-0.0376	0.0053	0.0053
D ↑	hold_rising to CP	0.0030	0.0054	0.0074	0.0074
D ↓	setup_rising to CP	0.0392	0.0730	0.0246	0.0246
D ↑	setup_rising to CP	0.0217	0.0195	0.0178	0.0178
TE ↓	hold_rising to CP	-0.0066	-0.0116	0.0070	0.0070
TE ↑	hold_rising to CP	0.0056	0.0056	0.0080	0.0027
TE ↓	setup_rising to CP	0.0370	0.0558	0.0242	0.0242
TE ↑	setup_rising to CP	0.0440	0.0645	0.0445	0.0445
TI ↓	hold_rising to CP	-0.0217	-0.0388	-0.0169	-0.0153
TI ↑	hold_rising to CP	0.0041	0.0044	0.0031	0.0041
TI ↓	setup_rising to CP	0.0500	0.0643	0.0467	0.0451
TI ↑	setup_rising to CP	0.0208	0.0195	0.0216	0.0224

		C8T28SOIDV_-LL_-SDFPQNX19_P0	C8T28SOIDV_-LL_-SDFPQNX29_P0		
CP ↓	min_pulse_width to CP	0.0400	0.0400		
CP ↑	min_pulse_width to CP	0.0317	0.0271		
D ↓	hold_rising to CP	0.0053	0.0053		
D ↑	hold_rising to CP	0.0074	0.0074		
D ↓	setup_rising to CP	0.0246	0.0246		
D ↑	setup_rising to CP	0.0178	0.0178		
TE ↓	hold_rising to CP	0.0070	0.0070		
TE ↑	hold_rising to CP	0.0027	0.0027		
TE ↓	setup_rising to CP	0.0242	0.0242		
TE ↑	setup_rising to CP	0.0445	0.0445		
TI ↓	hold_rising to CP	-0.0169	-0.0169		
TI ↑	hold_rising to CP	0.0041	0.0041		
TI ↓	setup_rising to CP	0.0451	0.0451		
TI ↑	setup_rising to CP	0.0224	0.0224		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P0	1.136e-03	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P0	1.003e-03	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P0	1.107e-03	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P0	1.515e-03	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P0	1.946e-03	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P0	3.046e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P0	C8T28SOI_LLHF_-SDFPQNX3_P0	C8T28SOIDV_LL_-SDFPQNX5_P0	C8T28SOIDV_LL_-SDFPQNX10_P0
Clock 100Mhz Data 0Mhz	1.103e-02	1.061e-02	1.005e-02	9.754e-03
Clock 100Mhz Data 25Mhz	1.055e-02	1.024e-02	9.743e-03	1.025e-02
Clock 100Mhz Data 50Mhz	1.008e-02	9.867e-03	9.436e-03	1.075e-02
Clock = 0 Data 100Mhz	5.553e-03	5.871e-03	5.490e-03	5.289e-03
Clock = 1 Data 100Mhz	4.468e-05	6.645e-04	4.595e-04	3.570e-04
	C8T28SOIDV_LL_-SDFPQNX19_P0	C8T28SOIDV_LL_-SDFPQNX29_P0		
Clock 100Mhz Data 0Mhz	9.581e-03	9.462e-03		

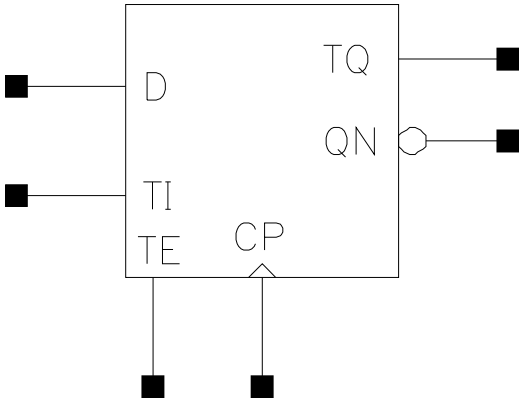
Clock 100Mhz Data 25Mhz	1.139e-02	1.241e-02		
Clock 100Mhz Data 50Mhz	1.320e-02	1.536e-02		
Clock = 0 Data 100Mhz	5.166e-03	5.087e-03		
Clock = 1 Data 100Mhz	2.960e-04	2.547e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P0	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P0	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P0	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P0	C8T28SOI_LLHF_-SDFPQNTX3_P0	C8T28SOIDV_LL_-SDFPQNTX5_P0	C8T28SOIDV_LL_-SDFPQNTX10_P0
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P0	C8T28SOIDV_LL_-SDFPQNTX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQNTX5_P0	**C8T28SOI_LLHF_-SDFPQNTX3_P0**	**C8T28SOI_LL_-SDFPQNTX5_P0**	**C8T28SOI_LLHF_-SDFPQNTX3_P0**
CP to QN ↓	0.0482	0.0485	2.5149	3.6500
CP to QN ↑	0.0470	0.0425	3.1758	4.2963
CP to TQ ↓	0.0384	0.0299	6.0995	4.2046
CP to TQ ↑	0.0417	0.0369	13.3851	7.3046
	C8T28SOIDV_LL_-SDFPQNTX5_P0	**C8T28SOIDV_LL_-SDFPQNTX10_P0**	**C8T28SOIDV_LL_-SDFPQNTX5_P0**	**C8T28SOIDV_LL_-SDFPQNTX10_P0**
CP to QN ↓	0.0502	0.0495	2.3136	1.1815
CP to QN ↑	0.0418	0.0420	2.8721	1.4694
CP to TQ ↓	0.0293	0.0303	4.2261	4.3698
CP to TQ ↑	0.0384	0.0393	5.9228	6.1258
	C8T28SOIDV_LL_-SDFPQNTX19_P0	**C8T28SOIDV_LL_-SDFPQNTX29_P0**	**C8T28SOIDV_LL_-SDFPQNTX19_P0**	**C8T28SOIDV_LL_-SDFPQNTX29_P0**
CP to QN ↓	0.0511	0.0604	0.6071	0.4196
CP to QN ↑	0.0457	0.0544	0.7466	0.4937
CP to TQ ↓	0.0314	0.0304	4.3248	4.4167
CP to TQ ↑	0.0405	0.0407	6.3281	7.7237

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_P0	C8T28SOI_-LLHF_-SDFPQNTX3_P0	C8T28SOIDV_-LL_-SDFPQNTX5_P0	C8T28SOIDV_-LL_-SDFPQNTX10_-P0
CP ↓	min_pulse_width to CP	0.0490	0.0493	0.0400	0.0401
CP ↑	min_pulse_width to CP	0.0317	0.0271	0.0270	0.0283
D ↓	hold_rising to CP	-0.0147	-0.0376	0.0053	0.0053
D ↑	hold_rising to CP	0.0030	0.0054	0.0074	0.0074
D ↓	setup_rising to CP	0.0392	0.0730	0.0246	0.0246

D ↑	setup_rising to CP	0.0217	0.0217	0.0178	0.0178
TE ↓	hold_rising to CP	-0.0066	-0.0110	0.0070	0.0070
TE ↑	hold_rising to CP	0.0056	0.0056	0.0080	0.0027
TE ↓	setup_rising to CP	0.0396	0.0562	0.0242	0.0242
TE ↑	setup_rising to CP	0.0440	0.0645	0.0445	0.0445
TI ↓	hold_rising to CP	-0.0217	-0.0388	-0.0169	-0.0169
TI ↑	hold_rising to CP	0.0041	0.0044	0.0031	0.0041
TI ↓	setup_rising to CP	0.0500	0.0643	0.0467	0.0451
TI ↑	setup_rising to CP	0.0208	0.0195	0.0216	0.0224
		C8T28SOIDV_-LL_-SDFPQNTX19_-P0	C8T28SOIDV_-LL_-SDFPQNTX29_-P0		
CP ↓	min_pulse_width to CP	0.0401	0.0401		
CP ↑	min_pulse_width to CP	0.0317	0.0270		
D ↓	hold_rising to CP	0.0053	0.0053		
D ↑	hold_rising to CP	0.0074	0.0074		
D ↓	setup_rising to CP	0.0246	0.0246		
D ↑	setup_rising to CP	0.0178	0.0178		
TE ↓	hold_rising to CP	0.0070	0.0070		
TE ↑	hold_rising to CP	0.0027	0.0027		
TE ↓	setup_rising to CP	0.0242	0.0242		
TE ↑	setup_rising to CP	0.0445	0.0445		
TI ↓	hold_rising to CP	-0.0169	-0.0153		
TI ↑	hold_rising to CP	0.0041	0.0041		
TI ↓	setup_rising to CP	0.0451	0.0451		
TI ↑	setup_rising to CP	0.0224	0.0224		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P0	1.131e-03	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P0	1.073e-03	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P0	1.184e-03	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P0	1.427e-03	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P0	1.921e-03	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P0	3.026e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

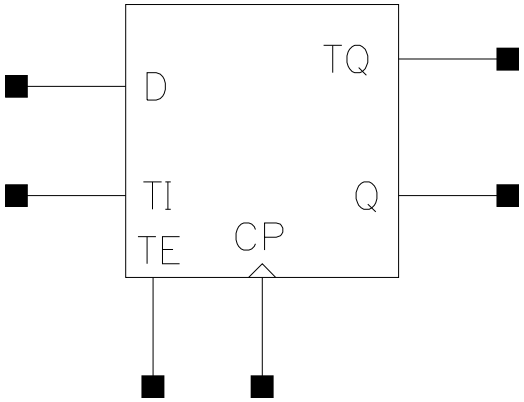
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P0	C8T28SOI_LLHF_-SDFPQNTX3_P0	C8T28SOIDV_LL_-SDFPQNTX5_P0	C8T28SOIDV_LL_-SDFPQNTX10_P0
Clock 100Mhz Data 0Mhz	1.104e-02	1.062e-02	1.005e-02	9.753e-03
Clock 100Mhz Data 25Mhz	1.100e-02	1.061e-02	1.009e-02	1.028e-02
Clock 100Mhz Data 50Mhz	1.095e-02	1.061e-02	1.013e-02	1.081e-02
Clock = 0 Data 100Mhz	5.554e-03	5.875e-03	5.494e-03	5.291e-03
Clock = 1 Data 100Mhz	4.509e-05	6.663e-04	4.613e-04	3.583e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P0	C8T28SOIDV_LL_-SDFPQNTX29_P0		
Clock 100Mhz Data 0Mhz	9.576e-03	9.455e-03		
Clock 100Mhz Data 25Mhz	1.131e-02	1.271e-02		
Clock 100Mhz Data 50Mhz	1.304e-02	1.597e-02		
Clock = 0 Data 100Mhz	5.169e-03	5.090e-03		
Clock = 1 Data 100Mhz	2.962e-04	2.549e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P0	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P0	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P0	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P0	C8T28SOI_LLHF_-SDFPQTX3_P0	C8T28SOIDV_LL_-SDFPQTX5_P0	C8T28SOIDV_LL_-SDFPQTX10_P0
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P0	C8T28SOIDV_LL_-SDFPQTX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQTX5_P0	**C8T28SOI_LLHF_-SDFPQTX3_P0**	**C8T28SOI_LL_-SDFPQTX5_P0**	**C8T28SOI_LLHF_-SDFPQTX3_P0**
CP to Q ↓	0.0404	0.0369	2.5973	3.8776
CP to Q ↑	0.0372	0.0382	2.9618	4.4696
CP to TQ ↓	0.0457	0.0350	6.6722	4.3274
CP to TQ ↑	0.0461	0.0404	13.6576	7.4415
	C8T28SOIDV_LL_-SDFPQTX5_P0	**C8T28SOIDV_LL_-SDFPQTX10_P0**	**C8T28SOIDV_LL_-SDFPQTX5_P0**	**C8T28SOIDV_LL_-SDFPQTX10_P0**
CP to Q ↓	0.0340	0.0452	2.4196	1.1755
CP to Q ↑	0.0403	0.0557	2.9509	1.4706
CP to TQ ↓	0.0332	0.0463	4.3398	4.4284
CP to TQ ↑	0.0415	0.0577	6.4611	6.3376
	C8T28SOIDV_LL_-SDFPQTX19_P0	**C8T28SOIDV_LL_-SDFPQTX29_P0**	**C8T28SOIDV_LL_-SDFPQTX19_P0**	**C8T28SOIDV_LL_-SDFPQTX29_P0**
CP to Q ↓	0.0488	0.0524	0.6062	0.3977
CP to Q ↑	0.0589	0.0587	0.7431	0.4904
CP to TQ ↓	0.0503	0.0320	4.4633	4.5364
CP to TQ ↑	0.0620	0.0416	6.3635	7.7411

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P0	C8T28SOI_-LLHF_-SDFPQTX3_P0	C8T28SOIDV_-LL_SDFPQTX5_-P0	C8T28SOIDV_-LL_-SDFPQTX10_P0
CP ↓	min_pulse_width to CP	0.0497	0.0493	0.0400	0.0400
CP ↑	min_pulse_width to CP	0.0364	0.0283	0.0317	0.0271
D ↓	hold_rising to CP	-0.0147	-0.0376	0.0053	0.0053
D ↑	hold_rising to CP	0.0030	0.0054	0.0074	0.0074
D ↓	setup_rising to CP	0.0392	0.0730	0.0246	0.0246

D ↑	setup_rising to CP	0.0217	0.0195	0.0178	0.0178
TE ↓	hold_rising to CP	-0.0066	-0.0116	0.0070	0.0070
TE ↑	hold_rising to CP	0.0056	0.0056	0.0027	0.0027
TE ↓	setup_rising to CP	0.0396	0.0558	0.0242	0.0242
TE ↑	setup_rising to CP	0.0440	0.0645	0.0445	0.0445
TI ↓	hold_rising to CP	-0.0217	-0.0388	-0.0153	-0.0153
TI ↑	hold_rising to CP	0.0041	0.0044	0.0041	0.0041
TI ↓	setup_rising to CP	0.0500	0.0643	0.0451	0.0451
TI ↑	setup_rising to CP	0.0208	0.0195	0.0224	0.0224
		C8T28SOIDV_-LL_-SDFPQTX19_P0	C8T28SOIDV_-LL_-SDFPQTX29_P0		
CP ↓	min_pulse_width to CP	0.0400	0.0400		
CP ↑	min_pulse_width to CP	0.0271	0.0317		
D ↓	hold_rising to CP	0.0053	0.0053		
D ↑	hold_rising to CP	0.0074	0.0074		
D ↓	setup_rising to CP	0.0246	0.0246		
D ↑	setup_rising to CP	0.0178	0.0178		
TE ↓	hold_rising to CP	0.0070	0.0070		
TE ↑	hold_rising to CP	0.0027	0.0027		
TE ↓	setup_rising to CP	0.0242	0.0242		
TE ↑	setup_rising to CP	0.0417	0.0445		
TI ↓	hold_rising to CP	-0.0169	-0.0169		
TI ↑	hold_rising to CP	0.0041	0.0041		
TI ↓	setup_rising to CP	0.0451	0.0467		
TI ↑	setup_rising to CP	0.0224	0.0224		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P0	1.157e-03	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P0	1.074e-03	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P0	1.178e-03	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P0	1.607e-03	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P0	2.011e-03	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P0	2.718e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

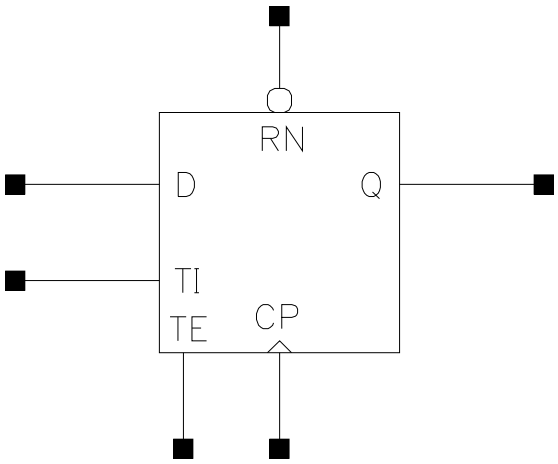
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P0	C8T28SOI_LLHF_-SDFPQTX3_P0	C8T28SOIDV_LL_-SDFPQTX5_P0	C8T28SOIDV_LL_-SDFPQTX10_P0
Clock 100Mhz Data 0Mhz	1.104e-02	1.063e-02	1.005e-02	9.760e-03
Clock 100Mhz Data 25Mhz	1.126e-02	1.078e-02	1.027e-02	1.049e-02
Clock 100Mhz Data 50Mhz	1.148e-02	1.093e-02	1.049e-02	1.122e-02
Clock = 0 Data 100Mhz	5.571e-03	5.878e-03	5.490e-03	5.288e-03
Clock = 1 Data 100Mhz	4.759e-05	6.659e-04	4.602e-04	3.577e-04
	C8T28SOIDV_LL_-SDFPQTX19_P0	C8T28SOIDV_LL_-SDFPQTX29_P0		
Clock 100Mhz Data 0Mhz	9.587e-03	9.478e-03		
Clock 100Mhz Data 25Mhz	1.146e-02	1.238e-02		
Clock 100Mhz Data 50Mhz	1.333e-02	1.528e-02		
Clock = 0 Data 100Mhz	5.165e-03	5.089e-03		
Clock = 1 Data 100Mhz	2.959e-04	2.546e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P0	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P0	C8T28SOI_LLHF_-SDFPRQX3_P0	C8T28SOIDV_LL_-SDFPRQX5_P0	C8T28SOIDV_LL_-SDFPRQX10_P0
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0008	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P0	C8T28SOIDV_LL_-SDFPRQX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0009	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P0	**C8T28SOI_LLHF_-SDFPRQX3_P0**	**C8T28SOI_LL_-SDFPRQX5_P0**	**C8T28SOI_LLHF_-SDFPRQX3_P0**
CP to Q ↓	0.0385	0.0348	2.4836	3.7818
CP to Q ↑	0.0354	0.0378	2.9500	4.3361
RN to Q ↓	0.0286	0.0267	2.3800	3.6540
	C8T28SOIDV_LL_-SDFPRQX5_P0	**C8T28SOIDV_LL_-SDFPRQX10_P0**	**C8T28SOIDV_LL_-SDFPRQX5_P0**	**C8T28SOIDV_LL_-SDFPRQX10_P0**
CP to Q ↓	0.0317	0.0449	2.3718	1.1831
CP to Q ↑	0.0407	0.0569	2.8994	1.4718
RN to Q ↓	0.0289	0.0415	2.3367	1.1827
	C8T28SOIDV_LL_-SDFPRQX19_P0	**C8T28SOIDV_LL_-SDFPRQX29_P0**	**C8T28SOIDV_LL_-SDFPRQX19_P0**	**C8T28SOIDV_LL_-SDFPRQX29_P0**
CP to Q ↓	0.0480	0.0492	0.6061	0.4143
CP to Q ↑	0.0603	0.0623	0.7534	0.5146
RN to Q ↓	0.0444	0.0457	0.6057	0.4145

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P0	C8T28SOI_-LLHF_-SDFPRQX3_P0	C8T28SOIDV_-LL_SDFPRQX5_-P0	C8T28SOIDV_-LL_-SDFPRQX10_P0
CP ↓	min_pulse_width to CP	0.0490	0.0479	0.0401	0.0401
CP ↑	min_pulse_width to CP	0.0317	0.0283	0.0271	0.0271
D ↓	hold_rising to CP	-0.0115	-0.0360	0.0048	0.0048
D ↑	hold_rising to CP	0.0004	0.0028	0.0080	0.0080
D ↓	setup_rising to CP	0.0392	0.0676	0.0246	0.0246
D ↑	setup_rising to CP	0.0244	0.0217	0.0169	0.0169
RN ↓	min_pulse_width to RN	0.0376	0.0354	0.0354	0.0305
RN ↑	recovery_rising to CP	0.0006	0.0010	0.0006	0.0006
RN ↑	removal_rising to CP	0.0073	0.0073	0.0074	0.0074

TE ↓	hold_rising to CP	-0.0098	-0.0110	0.0103	0.0103
TE ↑	hold_rising to CP	0.0030	0.0033	0.0032	0.0032
TE ↓	setup_rising to CP	0.0396	0.0530	0.0237	0.0237
TE ↑	setup_rising to CP	0.0445	0.0586	0.0423	0.0423
TI ↓	hold_rising to CP	-0.0202	-0.0347	-0.0110	-0.0110
TI ↑	hold_rising to CP	0.0025	0.0054	0.0025	0.0025
TI ↓	setup_rising to CP	0.0457	0.0637	0.0409	0.0409
TI ↑	setup_rising to CP	0.0222	0.0195	0.0265	0.0222
		C8T28SOIDV_-LL_-SDFPRQX19_P0	C8T28SOIDV_-LL_-SDFPRQX29_P0		
CP ↓	min_pulse_width to CP	0.0401	0.0401		
CP ↑	min_pulse_width to CP	0.0271	0.0271		
D ↓	hold_rising to CP	0.0048	0.0048		
D ↑	hold_rising to CP	0.0080	0.0080		
D ↓	setup_rising to CP	0.0246	0.0246		
D ↑	setup_rising to CP	0.0169	0.0169		
RN ↓	min_pulse_width to RN	0.0305	0.0305		
RN ↑	recovery_rising to CP	0.0006	0.0010		
RN ↑	removal_rising to CP	0.0074	0.0074		
TE ↓	hold_rising to CP	0.0103	0.0103		
TE ↑	hold_rising to CP	0.0032	0.0032		
TE ↓	setup_rising to CP	0.0237	0.0237		
TE ↑	setup_rising to CP	0.0423	0.0417		
TI ↓	hold_rising to CP	-0.0110	-0.0110		
TI ↑	hold_rising to CP	0.0028	0.0028		
TI ↓	setup_rising to CP	0.0409	0.0409		
TI ↑	setup_rising to CP	0.0264	0.0264		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P0	1.251e-03	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P0	1.104e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P0	1.227e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P0	1.637e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQX19_P0	2.136e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P0	2.739e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

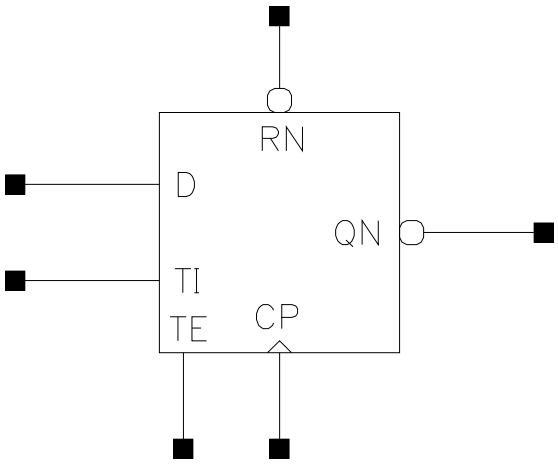
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P0	C8T28SOI_LLHF_-SDFPRQX3_P0	C8T28SOIDV_LL_-SDFPRQX5_P0	C8T28SOIDV_LL_-SDFPRQX10_P0
Clock 100Mhz Data 0Mhz	1.139e-02	1.088e-02	1.029e-02	9.997e-03
Clock 100Mhz Data 25Mhz	1.103e-02	1.054e-02	1.001e-02	1.039e-02
Clock 100Mhz Data 50Mhz	1.067e-02	1.019e-02	9.731e-03	1.078e-02
Clock = 0 Data 100Mhz	4.999e-03	5.363e-03	5.114e-03	4.990e-03
Clock = 1 Data 100Mhz	4.832e-05	6.701e-04	4.640e-04	3.607e-04
	C8T28SOIDV_LL_-SDFPRQX19_P0	C8T28SOIDV_LL_-SDFPRQX29_P0		
Clock 100Mhz Data 0Mhz	9.820e-03	9.703e-03		
Clock 100Mhz Data 25Mhz	1.126e-02	1.241e-02		
Clock 100Mhz Data 50Mhz	1.271e-02	1.513e-02		
Clock = 0 Data 100Mhz	4.917e-03	4.869e-03		
Clock = 1 Data 100Mhz	2.983e-04	2.568e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P0	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P0	C8T28SOI_LLHF_-SDFPRQNX3_P0	C8T28SOIDV_LL_-SDFPRQNX5_P0	C8T28SOIDV_LL_-SDFPRQNX10_P0
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0005
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0008	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P0	C8T28SOIDV_LL_-SDFPRQNX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0007	0.0007		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNX5_P0	**C8T28SOI_LLHF_-SDFPRQNX3_P0**	**C8T28SOI_LL_-SDFPRQNX5_P0**	**C8T28SOI_LLHF_-SDFPRQNX3_P0**
CP to QN ↓	0.0448	0.0465	2.4846	3.6112
CP to QN ↑	0.0412	0.0383	3.0341	4.2699
RN to QN ↑	0.0332	0.0319	3.0315	4.2679
	C8T28SOIDV_LL_-SDFPRQNX5_P0	**C8T28SOIDV_LL_-SDFPRQNX10_P0**	**C8T28SOIDV_LL_-SDFPRQNX5_P0**	**C8T28SOIDV_LL_-SDFPRQNX10_P0**
CP to QN ↓	0.0507	0.0469	2.3040	1.1825
CP to QN ↑	0.0396	0.0387	2.8646	1.4716
RN to QN ↑	0.0361	0.0359	2.8613	1.4702
	C8T28SOIDV_LL_-SDFPRQNX19_P0	**C8T28SOIDV_LL_-SDFPRQNX29_P0**	**C8T28SOIDV_LL_-SDFPRQNX19_P0**	**C8T28SOIDV_LL_-SDFPRQNX29_P0**
CP to QN ↓	0.0522	0.0558	0.6190	0.4160
CP to QN ↑	0.0434	0.0480	0.7576	0.5122
RN to QN ↑	0.0410	0.0429	0.7570	0.5112

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P0	C8T28SOI_-LLHF_-SDFPRQNX3_-P0	C8T28SOIDV_-LL_-SDFPRQNX5_-P0	C8T28SOIDV_-LL_-SDFPRQNX10_-P0
CP ↓	min_pulse_width to CP	0.0473	0.0479	0.0401	0.0401
CP ↑	min_pulse_width to CP	0.0270	0.0237	0.0271	0.0270
D ↓	hold_rising to CP	-0.0115	-0.0360	0.0048	0.0048
D ↑	hold_rising to CP	0.0004	0.0028	0.0080	0.0080
D ↓	setup_rising to CP	0.0392	0.0681	0.0246	0.0246
D ↑	setup_rising to CP	0.0244	0.0270	0.0169	0.0169
RN ↓	min_pulse_width to RN	0.0354	0.0354	0.0305	0.0354
RN ↑	recovery_rising to CP	0.0006	0.0010	0.0010	0.0006

RN ↑	removal_rising to CP	0.0073	0.0041	0.0074	0.0074
TE ↓	hold_rising to CP	-0.0098	-0.0110	0.0103	0.0103
TE ↑	hold_rising to CP	0.0030	0.0033	0.0032	0.0032
TE ↓	setup_rising to CP	0.0396	0.0530	0.0237	0.0237
TE ↑	setup_rising to CP	0.0445	0.0586	0.0423	0.0423
TI ↓	hold_rising to CP	-0.0202	-0.0347	-0.0110	-0.0110
TI ↑	hold_rising to CP	0.0025	0.0054	0.0025	0.0025
TI ↓	setup_rising to CP	0.0457	0.0637	0.0408	0.0409
TI ↑	setup_rising to CP	0.0224	0.0211	0.0222	0.0222
		C8T28SOIDV_-LL_-SDFPRQNX19_-P0	C8T28SOIDV_-LL_-SDFPRQNX29_-P0		
CP ↓	min_pulse_width to CP	0.0435	0.0442		
CP ↑	min_pulse_width to CP	0.0317	0.0330		
D ↓	hold_rising to CP	0.0081	0.0081		
D ↑	hold_rising to CP	0.0079	0.0079		
D ↓	setup_rising to CP	0.0246	0.0246		
D ↑	setup_rising to CP	0.0169	0.0169		
RN ↓	min_pulse_width to RN	0.0354	0.0425		
RN ↑	recovery_rising to CP	-0.0022	-0.0022		
RN ↑	removal_rising to CP	0.0074	0.0074		
TE ↓	hold_rising to CP	0.0103	0.0124		
TE ↑	hold_rising to CP	0.0032	0.0032		
TE ↓	setup_rising to CP	0.0237	0.0237		
TE ↑	setup_rising to CP	0.0423	0.0423		
TI ↓	hold_rising to CP	-0.0120	-0.0120		
TI ↑	hold_rising to CP	0.0025	0.0025		
TI ↓	setup_rising to CP	0.0409	0.0409		
TI ↑	setup_rising to CP	0.0222	0.0222		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P0	1.170e-03	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P0	1.074e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P0	1.146e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P0	1.566e-03	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P0	1.867e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P0	2.425e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

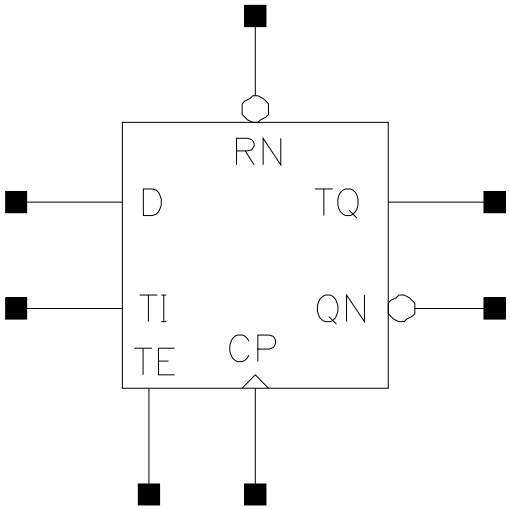
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P0	C8T28SOI_LLHF_-SDFPRQNX3_P0	C8T28SOIDV_LL_-SDFPRQNX5_P0	C8T28SOIDV_LL_-SDFPRQNX10_P0
Clock 100Mhz Data 0Mhz	1.138e-02	1.085e-02	1.027e-02	9.980e-03
Clock 100Mhz Data 25Mhz	1.079e-02	1.039e-02	9.957e-03	1.045e-02
Clock 100Mhz Data 50Mhz	1.020e-02	9.925e-03	9.643e-03	1.092e-02
Clock = 0 Data 100Mhz	4.998e-03	5.360e-03	5.117e-03	4.991e-03
Clock = 1 Data 100Mhz	4.341e-05	6.651e-04	4.584e-04	3.560e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P0	C8T28SOIDV_LL_-SDFPRQNX29_P0		
Clock 100Mhz Data 0Mhz	9.865e-03	9.816e-03		
Clock 100Mhz Data 25Mhz	1.146e-02	1.303e-02		
Clock 100Mhz Data 50Mhz	1.305e-02	1.625e-02		
Clock = 0 Data 100Mhz	4.915e-03	4.865e-03		
Clock = 1 Data 100Mhz	2.956e-04	2.539e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P0	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P0	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P0	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P0	C8T28SOI_LLHF_-SDFPRQNTX3_P0	C8T28SOIDV_LL_-SDFPRQNTX5_P0	C8T28SOIDV_LL_-SDFPRQNTX10_P0
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0008	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P0	C8T28SOIDV_LL_-SDFPRQNTX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0007		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNTX5_P0	**C8T28SOI_LLHF_-SDFPRQNTX3_P0**	**C8T28SOI_LL_-SDFPRQNTX5_P0**	**C8T28SOI_LLHF_-SDFPRQNTX3_P0**
CP to QN ↓	0.0500	0.0508	2.4449	3.6444
CP to QN ↑	0.0504	0.0457	3.1769	4.2963
CP to TQ ↓	0.0422	0.0328	6.3416	4.2314
CP to TQ ↑	0.0426	0.0390	13.3969	7.3249
RN to QN ↑	0.0400	0.0374	3.1748	4.3016
RN to TQ ↓	0.0322	0.0250	6.2063	4.1463
	C8T28SOIDV_LL_-SDFPRQNTX5_P0	**C8T28SOIDV_LL_-SDFPRQNTX10_P0**	**C8T28SOIDV_LL_-SDFPRQNTX5_P0**	**C8T28SOIDV_LL_-SDFPRQNTX10_P0**
CP to QN ↓	0.0533	0.0564	2.3327	1.2026
CP to QN ↑	0.0431	0.0460	2.8585	1.4567
CP to TQ ↓	0.0299	0.0303	4.2328	4.2592
CP to TQ ↑	0.0408	0.0408	5.9303	5.9355
RN to QN ↑	0.0398	0.0430	2.8576	1.4562
RN to TQ ↓	0.0263	0.0267	4.2173	4.2439
	C8T28SOIDV_LL_-SDFPRQNTX19_P0	**C8T28SOIDV_LL_-SDFPRQNTX29_P0**	**C8T28SOIDV_LL_-SDFPRQNTX19_P0**	**C8T28SOIDV_LL_-SDFPRQNTX29_P0**
CP to QN ↓	0.0545	0.0562	0.6086	0.4163
CP to QN ↑	0.0473	0.0518	0.7413	0.5074
CP to TQ ↓	0.0324	0.0389	4.2846	4.7750
CP to TQ ↑	0.0434	0.0486	5.9470	6.6880
RN to QN ↑	0.0438	0.0446	0.7418	0.5092
RN to TQ ↓	0.0315	0.0349	4.2005	4.6153

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P0	C8T28SOI_-LLHF_-SDFPRQNTX3_-P0	C8T28SOIDV_-LL_-SDFPRQNTX5_-P0	C8T28SOIDV_-LL_SDF-PRQNTX10_P0
CP ↓	min_pulse_width to CP	0.0473	0.0479	0.0401	0.0401
CP ↑	min_pulse_width to CP	0.0329	0.0283	0.0270	0.0318
D ↓	hold_rising to CP	-0.0120	-0.0360	0.0048	0.0048
D ↑	hold_rising to CP	0.0031	0.0028	0.0080	0.0080
D ↓	setup_rising to CP	0.0392	0.0676	0.0246	0.0246
D ↑	setup_rising to CP	0.0244	0.0270	0.0169	0.0169
RN ↓	min_pulse_width to RN	0.0376	0.0354	0.0376	0.0376
RN ↑	recovery_rising to CP	0.0006	0.0006	0.0006	0.0006
RN ↑	removal_rising to CP	0.0073	0.0041	0.0074	0.0074
TE ↓	hold_rising to CP	-0.0098	-0.0110	0.0103	0.0103
TE ↑	hold_rising to CP	0.0030	0.0033	0.0032	0.0032
TE ↓	setup_rising to CP	0.0370	0.0530	0.0237	0.0237
TE ↑	setup_rising to CP	0.0445	0.0586	0.0417	0.0423
TI ↓	hold_rising to CP	-0.0202	-0.0347	-0.0110	-0.0110
TI ↑	hold_rising to CP	0.0025	0.0054	0.0025	0.0025
TI ↓	setup_rising to CP	0.0457	0.0637	0.0408	0.0409
TI ↑	setup_rising to CP	0.0224	0.0211	0.0222	0.0222
		C8T28SOIDV_-LL_SDF-PRQNTX19_P0	C8T28SOIDV_-LL_SDF-PRQNTX29_P0		
CP ↓	min_pulse_width to CP	0.0418	0.0435		
CP ↑	min_pulse_width to CP	0.0317	0.0363		
D ↓	hold_rising to CP	0.0081	0.0048		
D ↑	hold_rising to CP	0.0079	0.0080		
D ↓	setup_rising to CP	0.0246	0.0246		
D ↑	setup_rising to CP	0.0169	0.0169		
RN ↓	min_pulse_width to RN	0.0376	0.0447		
RN ↑	recovery_rising to CP	-0.0022	-0.0022		
RN ↑	removal_rising to CP	0.0074	0.0074		
TE ↓	hold_rising to CP	0.0103	0.0103		
TE ↑	hold_rising to CP	0.0032	0.0032		

TE ↓	setup_rising to CP	0.0237	0.0237		
TE ↑	setup_rising to CP	0.0423	0.0423		
TI ↓	hold_rising to CP	-0.0120	-0.0120		
TI ↑	hold_rising to CP	0.0025	0.0025		
TI ↓	setup_rising to CP	0.0409	0.0409		
TI ↑	setup_rising to CP	0.0222	0.0222		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P0	1.166e-03	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P0	1.145e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P0	1.243e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_P0	1.392e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_P0	1.859e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_P0	2.504e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

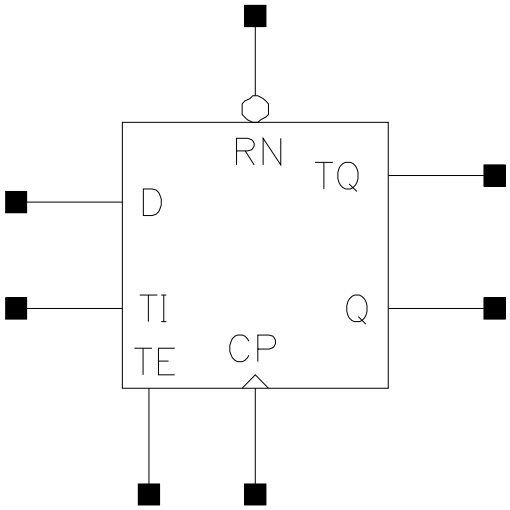
Pin Cycle	C8T28SOI_LL_SDFPRQNTX5_P0	C8T28SOI_LLHF_SDFPRQNTX3_P0	C8T28SOIDV_LL_SDFPRQNTX5_P0	C8T28SOIDV_LL_SDFPRQNTX10_P0
Clock 100Mhz Data 0Mhz	1.139e-02	1.086e-02	1.029e-02	9.996e-03
Clock 100Mhz Data 25Mhz	1.121e-02	1.078e-02	1.027e-02	1.062e-02
Clock 100Mhz Data 50Mhz	1.103e-02	1.071e-02	1.026e-02	1.124e-02
Clock = 0 Data 100Mhz	4.973e-03	5.353e-03	5.116e-03	4.992e-03
Clock = 1 Data 100Mhz	4.800e-05	6.715e-04	4.643e-04	3.601e-04
	C8T28SOIDV_LL_SDFPRQNTX19_P0	C8T28SOIDV_LL_SDFPRQNTX29_P0		
Clock 100Mhz Data 0Mhz	9.880e-03	9.792e-03		
Clock 100Mhz Data 25Mhz	1.156e-02	1.350e-02		
Clock 100Mhz Data 50Mhz	1.324e-02	1.720e-02		
Clock = 0 Data 100Mhz	4.917e-03	4.868e-03		
Clock = 1 Data 100Mhz	2.976e-04	2.560e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P0	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P0	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P0	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P0	C8T28SOI_LLHF_-SDFPRQTX3_P0	C8T28SOIDV_LL_-SDFPRQTX5_P0	C8T28SOIDV_LL_-SDFPRQTX10_P0
CP	0.0007	0.0007	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0008	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P0	C8T28SOIDV_LL_-SDFPRQTX29_P0		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0009	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPRQTX5_P0	**C8T28SOI_LLHF_-SDFPRQTX3_P0**	**C8T28SOI_LL_-SDFPRQTX5_P0**	**C8T28SOI_LLHF_-SDFPRQTX3_P0**
CP to Q ↓	0.0451	0.0388	2.6236	3.8879
CP to Q ↑	0.0384	0.0397	2.9650	4.4899
CP to TQ ↓	0.0503	0.0367	6.7120	4.3465
CP to TQ ↑	0.0471	0.0418	13.4395	7.4508
RN to Q ↓	0.0332	0.0300	2.4866	3.7312
RN to TQ ↓	0.0383	0.0282	6.4985	4.2180
	C8T28SOIDV_LL_-SDFPRQTX5_P0	**C8T28SOIDV_LL_-SDFPRQTX10_P0**	**C8T28SOIDV_LL_-SDFPRQTX5_P0**	**C8T28SOIDV_LL_-SDFPRQTX10_P0**
CP to Q ↓	0.0343	0.0459	2.4407	1.2014
CP to Q ↑	0.0422	0.0579	2.9313	1.4679
CP to TQ ↓	0.0339	0.0473	4.3458	4.2896
CP to TQ ↑	0.0434	0.0600	6.0413	6.0007
RN to Q ↓	0.0334	0.0421	2.3663	1.2021
RN to TQ ↓	0.0313	0.0434	4.2929	4.2894
	C8T28SOIDV_LL_-SDFPRQTX19_P0	**C8T28SOIDV_LL_-SDFPRQTX29_P0**	**C8T28SOIDV_LL_-SDFPRQTX19_P0**	**C8T28SOIDV_LL_-SDFPRQTX29_P0**
CP to Q ↓	0.0510	0.0494	0.6267	0.4219
CP to Q ↑	0.0622	0.0622	0.7474	0.5121
CP to TQ ↓	0.0528	0.0503	4.3275	4.2195
CP to TQ ↑	0.0653	0.0650	5.9857	6.0865
RN to Q ↓	0.0479	0.0459	0.6266	0.4219
RN to TQ ↓	0.0496	0.0468	4.3272	4.2192

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_P0	C8T28SOI_-LLHF_-SDFPRQTX3_P0	C8T28SOIDV_-LL_-SDFPRQTX5_P0	C8T28SOIDV_-LL_-SDFPRQTX10_-P0
CP ↓	min_pulse_width to CP	0.0473	0.0479	0.0401	0.0401
CP ↑	min_pulse_width to CP	0.0377	0.0318	0.0318	0.0271
D ↓	hold_rising to CP	-0.0120	-0.0360	0.0048	0.0048
D ↑	hold_rising to CP	0.0031	0.0028	0.0080	0.0080
D ↓	setup_rising to CP	0.0392	0.0676	0.0246	0.0246
D ↑	setup_rising to CP	0.0244	0.0270	0.0169	0.0169
RN ↓	min_pulse_width to RN	0.0425	0.0376	0.0376	0.0305
RN ↑	recovery_rising to CP	0.0006	0.0006	0.0006	0.0010
RN ↑	removal_rising to CP	0.0073	0.0041	0.0074	0.0074
TE ↓	hold_rising to CP	-0.0098	-0.0110	0.0103	0.0103
TE ↑	hold_rising to CP	0.0030	0.0033	0.0032	0.0032
TE ↓	setup_rising to CP	0.0396	0.0530	0.0237	0.0237
TE ↑	setup_rising to CP	0.0445	0.0586	0.0423	0.0423
TI ↓	hold_rising to CP	-0.0202	-0.0347	-0.0110	-0.0110
TI ↑	hold_rising to CP	0.0025	0.0054	0.0025	0.0025
TI ↓	setup_rising to CP	0.0457	0.0637	0.0409	0.0409
TI ↑	setup_rising to CP	0.0224	0.0211	0.0265	0.0264
		C8T28SOIDV_-LL_-SDFPRQTX19_-P0	C8T28SOIDV_-LL_-SDFPRQTX29_-P0		
CP ↓	min_pulse_width to CP	0.0401	0.0401		
CP ↑	min_pulse_width to CP	0.0271	0.0271		
D ↓	hold_rising to CP	0.0048	0.0048		
D ↑	hold_rising to CP	0.0080	0.0080		
D ↓	setup_rising to CP	0.0246	0.0246		
D ↑	setup_rising to CP	0.0169	0.0169		
RN ↓	min_pulse_width to RN	0.0327	0.0305		
RN ↑	recovery_rising to CP	0.0010	0.0010		
RN ↑	removal_rising to CP	0.0074	0.0074		
TE ↓	hold_rising to CP	0.0103	0.0103		
TE ↑	hold_rising to CP	0.0032	0.0032		

TE ↓	setup_rising to CP	0.0237	0.0237		
TE ↑	setup_rising to CP	0.0423	0.0417		
TI ↓	hold_rising to CP	-0.0110	-0.0110		
TI ↑	hold_rising to CP	0.0025	0.0028		
TI ↓	setup_rising to CP	0.0409	0.0409		
TI ↑	setup_rising to CP	0.0264	0.0264		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P0	1.265e-03	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P0	1.179e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P0	1.325e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P0	1.705e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P0	2.163e-03	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P0	2.799e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

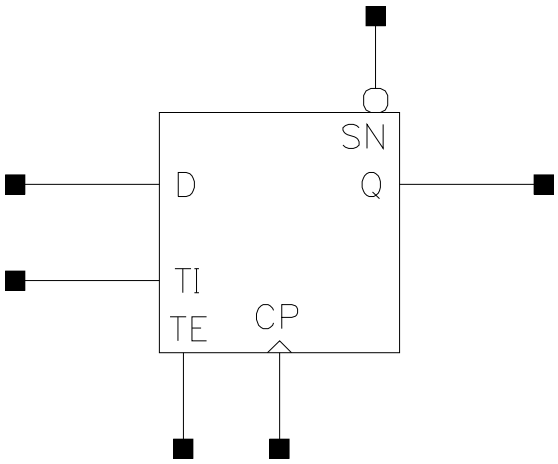
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P0	C8T28SOI_LLHF_-SDFPRQTX3_P0	C8T28SOIDV_LL_-SDFPRQTX5_P0	C8T28SOIDV_LL_-SDFPRQTX10_P0
Clock 100Mhz Data 0Mhz	1.140e-02	1.087e-02	1.028e-02	9.992e-03
Clock 100Mhz Data 25Mhz	1.153e-02	1.092e-02	1.036e-02	1.070e-02
Clock 100Mhz Data 50Mhz	1.167e-02	1.097e-02	1.044e-02	1.140e-02
Clock = 0 Data 100Mhz	4.984e-03	5.360e-03	5.114e-03	4.991e-03
Clock = 1 Data 100Mhz	4.550e-05	6.700e-04	4.631e-04	3.600e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P0	C8T28SOIDV_LL_-SDFPRQTX29_P0		
Clock 100Mhz Data 0Mhz	9.817e-03	9.698e-03		
Clock 100Mhz Data 25Mhz	1.167e-02	1.258e-02		
Clock 100Mhz Data 50Mhz	1.352e-02	1.546e-02		
Clock = 0 Data 100Mhz	4.917e-03	4.869e-03		
Clock = 1 Data 100Mhz	2.968e-04	2.562e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P0	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P0	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P0	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P0	C8T28SOI_LLHF_-SDFPSQX3_P0	C8T28SOIDV_LL_-SDFPSQX5_P0	C8T28SOIDV_LL_-SDFPSQX10_P0
CP	0.0007	0.0007	0.0005	0.0006
D	0.0003	0.0005	0.0003	0.0003
SN	0.0014	0.0013	0.0010	0.0010
TE	0.0010	0.0008	0.0009	0.0010
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQX14_P0	C8T28SOIDV_LL_-SDFPSQX19_P0	C8T28SOIDV_LL_-SDFPSQX29_P0	
CP	0.0006	0.0006	0.0006	
D	0.0003	0.0003	0.0003	
SN	0.0010	0.0010	0.0010	
TE	0.0010	0.0010	0.0010	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P0	**C8T28SOI_LLHF_-SDFPSQX3_P0**	**C8T28SOI_LL_-SDFPSQX5_P0**	**C8T28SOI_LLHF_-SDFPSQX3_P0**
CP to Q ↓	0.0401	0.0353	2.5217	3.8260
CP to Q ↑	0.0364	0.0386	2.9645	4.3550
SN to Q ↑	0.0242	0.0227	2.9133	4.2881
	C8T28SOIDV_LL_-SDFPSQX5_P0	**C8T28SOIDV_LL_-SDFPSQX10_P0**	**C8T28SOIDV_LL_-SDFPSQX5_P0**	**C8T28SOIDV_LL_-SDFPSQX10_P0**
CP to Q ↓	0.0315	0.0452	2.3655	1.1586
CP to Q ↑	0.0385	0.0602	2.8955	1.4596
SN to Q ↑	0.0224	0.0420	2.8735	1.4615
	C8T28SOIDV_LL_-SDFPSQX14_P0	**C8T28SOIDV_LL_-SDFPSQX19_P0**	**C8T28SOIDV_LL_-SDFPSQX14_P0**	**C8T28SOIDV_LL_-SDFPSQX19_P0**
CP to Q ↓	0.0454	0.0483	0.7970	0.6144
CP to Q ↑	0.0602	0.0627	0.9818	0.7377
SN to Q ↑	0.0420	0.0446	0.9818	0.7373
	C8T28SOIDV_LL_-SDFPSQX29_P0		**C8T28SOIDV_LL_-SDFPSQX29_P0**	
CP to Q ↓	0.0485		0.4165	
CP to Q ↑	0.0647		0.4906	
SN to Q ↑	0.0464		0.4902	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P0	C8T28SOI_-LLHF_-SDFPSQX3_P0	C8T28SOIDV_-LL_SDFPSQX5_-P0	C8T28SOIDV_-LL_-SDFPSQX10_P0
CP ↓	min_pulse_width to CP	0.0544	0.0575	0.0448	0.0449
CP ↑	min_pulse_width to CP	0.0364	0.0283	0.0270	0.0270
D ↓	hold_rising to CP	-0.0164	-0.0425	0.0004	-0.0017
D ↑	hold_rising to CP	0.0025	0.0048	0.0079	0.0079
D ↓	setup_rising to CP	0.0461	0.0773	0.0294	0.0347
D ↑	setup_rising to CP	0.0217	0.0217	0.0169	0.0169

SN ↓	min_pulse_width to SN	0.0305	0.0283	0.0283	0.0283
SN ↑	recovery_rising to CP	-0.0027	-0.0027	-0.0071	-0.0071
SN ↑	removal_rising to CP	0.0141	0.0169	0.0185	0.0217
TE ↓	hold_rising to CP	-0.0061	-0.0083	0.0026	-0.0000
TE ↑	hold_rising to CP	0.0046	0.0082	0.0101	0.0080
TE ↓	setup_rising to CP	0.0445	0.0628	0.0296	0.0290
TE ↑	setup_rising to CP	0.0547	0.0684	0.0471	0.0471
TI ↓	hold_rising to CP	-0.0266	-0.0452	-0.0182	-0.0169
TI ↑	hold_rising to CP	0.0031	0.0103	0.0101	0.0031
TI ↓	setup_rising to CP	0.0564	0.0748	0.0479	0.0467
TI ↑	setup_rising to CP	0.0208	0.0205	0.0146	0.0208
		C8T28SOIDV_-LL_-SDFPSQX14_P0	C8T28SOIDV_-LL_-SDFPSQX19_P0	C8T28SOIDV_-LL_-SDFPSQX29_P0	
CP ↓	min_pulse_width to CP	0.0449	0.0449	0.0449	
CP ↑	min_pulse_width to CP	0.0270	0.0270	0.0270	
D ↓	hold_rising to CP	-0.0017	-0.0017	-0.0017	
D ↑	hold_rising to CP	0.0079	0.0079	0.0079	
D ↓	setup_rising to CP	0.0347	0.0347	0.0347	
D ↑	setup_rising to CP	0.0169	0.0169	0.0169	
SN ↓	min_pulse_width to SN	0.0283	0.0283	0.0283	
SN ↑	recovery_rising to CP	-0.0071	-0.0071	-0.0071	
SN ↑	removal_rising to CP	0.0217	0.0217	0.0217	
TE ↓	hold_rising to CP	-0.0000	-0.0000	-0.0000	
TE ↑	hold_rising to CP	0.0080	0.0080	0.0080	
TE ↓	setup_rising to CP	0.0290	0.0290	0.0290	
TE ↑	setup_rising to CP	0.0471	0.0471	0.0471	
TI ↓	hold_rising to CP	-0.0169	-0.0169	-0.0169	
TI ↑	hold_rising to CP	0.0031	0.0031	0.0031	
TI ↓	setup_rising to CP	0.0467	0.0467	0.0467	
TI ↑	setup_rising to CP	0.0208	0.0208	0.0208	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQX5_P0	1.223e-03	1.000e-20

C8T28SOI_LLHF_SDFPSQX3_P0	1.121e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P0	1.187e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P0	1.612e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P0	1.823e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P0	2.038e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P0	2.572e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

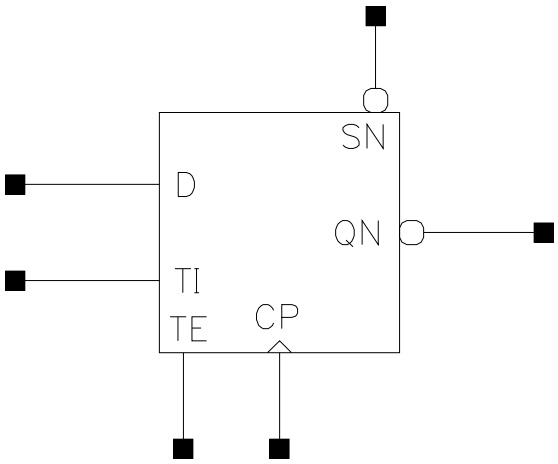
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P0	C8T28SOI_LLHF_-SDFPSQX3_P0	C8T28SOIDV_LL_-SDFPSQX5_P0	C8T28SOIDV_LL_-SDFPSQX10_P0
Clock 100Mhz Data 0Mhz	1.123e-02	1.061e-02	1.006e-02	9.782e-03
Clock 100Mhz Data 25Mhz	1.113e-02	1.045e-02	9.827e-03	1.037e-02
Clock 100Mhz Data 50Mhz	1.104e-02	1.030e-02	9.594e-03	1.096e-02
Clock = 0 Data 100Mhz	5.160e-03	5.552e-03	5.355e-03	5.294e-03
Clock = 1 Data 100Mhz	4.591e-05	6.655e-04	4.605e-04	3.581e-04
	C8T28SOIDV_LL_-SDFPSQX14_P0	C8T28SOIDV_LL_-SDFPSQX19_P0	C8T28SOIDV_LL_-SDFPSQX29_P0	
Clock 100Mhz Data 0Mhz	9.613e-03	9.502e-03	9.424e-03	
Clock 100Mhz Data 25Mhz	1.062e-02	1.124e-02	1.213e-02	
Clock 100Mhz Data 50Mhz	1.162e-02	1.297e-02	1.483e-02	
Clock = 0 Data 100Mhz	5.257e-03	5.233e-03	5.215e-03	
Clock = 1 Data 100Mhz	2.965e-04	2.554e-04	2.271e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P0	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P0	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P0	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P0	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P0	C8T28SOI_LLHF_-SDFPSQNX3_P0	C8T28SOIDV_LL_-SDFPSQNX5_P0	C8T28SOIDV_LL_-SDFPSQNX10_P0
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0005	0.0003	0.0003
SN	0.0014	0.0013	0.0010	0.0010
TE	0.0010	0.0008	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNX14_P0	C8T28SOIDV_LL_-SDFPSQNX19_P0	C8T28SOIDV_LL_-SDFPSQNX23_P0	C8T28SOIDV_LL_-SDFPSQNX29_P0
CP	0.0005	0.0005	0.0005	0.0005
D	0.0003	0.0003	0.0003	0.0003
SN	0.0010	0.0010	0.0010	0.0010
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNX5_P0	**C8T28SOI_LLHF_-SDFPSQNX3_P0**	**C8T28SOI_LL_-SDFPSQNX5_P0**	**C8T28SOI_LLHF_-SDFPSQNX3_P0**
CP to QN ↓	0.0471	0.0466	2.5551	3.6019
CP to QN ↑	0.0437	0.0399	3.0711	4.2703
SN to QN ↓	0.0352	0.0311	2.5566	3.6003
	C8T28SOIDV_LL_-SDFPSQNX5_P0	**C8T28SOIDV_LL_-SDFPSQNX10_P0**	**C8T28SOIDV_LL_-SDFPSQNX5_P0**	**C8T28SOIDV_LL_-SDFPSQNX10_P0**
CP to QN ↓	0.0504	0.0480	2.2946	1.1788
CP to QN ↑	0.0416	0.0422	2.8666	1.4404
SN to QN ↓	0.0335	0.0296	2.2941	1.1790
	C8T28SOIDV_LL_-SDFPSQNX14_P0	**C8T28SOIDV_LL_-SDFPSQNX19_P0**	**C8T28SOIDV_LL_-SDFPSQNX14_P0**	**C8T28SOIDV_LL_-SDFPSQNX19_P0**
CP to QN ↓	0.0498	0.0511	0.7808	0.5955
CP to QN ↑	0.0436	0.0452	0.9699	0.7283
SN to QN ↓	0.0308	0.0324	0.7803	0.5952
	C8T28SOIDV_LL_-SDFPSQNX23_P0	**C8T28SOIDV_LL_-SDFPSQNX29_P0**	**C8T28SOIDV_LL_-SDFPSQNX23_P0**	**C8T28SOIDV_LL_-SDFPSQNX29_P0**
CP to QN ↓	0.0520	0.0503	0.4765	0.4118
CP to QN ↑	0.0450	0.0454	0.7261	0.4893
SN to QN ↓	0.0330	0.0323	0.4761	0.4112

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P0	C8T28SOI_-LLHF_-SDFPSQNX3_-P0	C8T28SOIDV_-LL_-SDFPSQNX5_-P0	C8T28SOIDV_-LL_-SDFPSQNX10_-P0
CP ↓	min_pulse_width to CP	0.0544	0.0575	0.0448	0.0466
CP ↑	min_pulse_width to CP	0.0282	0.0237	0.0270	0.0317
D ↓	hold_rising to CP	-0.0164	-0.0425	0.0004	-0.0000
D ↑	hold_rising to CP	0.0025	0.0048	0.0079	0.0079
D ↓	setup_rising to CP	0.0461	0.0773	0.0294	0.0294

D ↑	setup_rising to CP	0.0217	0.0217	0.0169	0.0169
SN ↓	min_pulse_width to SN	0.0305	0.0256	0.0283	0.0283
SN ↑	recovery_rising to CP	-0.0027	-0.0027	-0.0071	-0.0071
SN ↑	removal_rising to CP	0.0141	0.0169	0.0185	0.0217
TE ↓	hold_rising to CP	-0.0061	-0.0083	0.0026	0.0026
TE ↑	hold_rising to CP	0.0046	0.0082	0.0101	0.0101
TE ↓	setup_rising to CP	0.0445	0.0628	0.0296	0.0296
TE ↑	setup_rising to CP	0.0547	0.0684	0.0471	0.0471
TI ↓	hold_rising to CP	-0.0266	-0.0445	-0.0182	-0.0166
TI ↑	hold_rising to CP	0.0031	0.0103	0.0101	0.0101
TI ↓	setup_rising to CP	0.0564	0.0748	0.0479	0.0479
TI ↑	setup_rising to CP	0.0208	0.0205	0.0146	0.0146
		C8T28SOIDV_-LL_-SDFPSQNX14_-P0	C8T28SOIDV_-LL_-SDFPSQNX19_-P0	C8T28SOIDV_-LL_-SDFPSQNX23_-P0	C8T28SOIDV_-LL_-SDFPSQNX29_-P0
CP ↓	min_pulse_width to CP	0.0466	0.0466	0.0466	0.0448
CP ↑	min_pulse_width to CP	0.0317	0.0317	0.0317	0.0317
D ↓	hold_rising to CP	-0.0000	-0.0000	-0.0000	0.0004
D ↑	hold_rising to CP	0.0079	0.0079	0.0079	0.0079
D ↓	setup_rising to CP	0.0294	0.0294	0.0294	0.0321
D ↑	setup_rising to CP	0.0169	0.0169	0.0169	0.0169
SN ↓	min_pulse_width to SN	0.0283	0.0283	0.0283	0.0332
SN ↑	recovery_rising to CP	-0.0071	-0.0071	-0.0071	-0.0039
SN ↑	removal_rising to CP	0.0217	0.0217	0.0217	0.0185
TE ↓	hold_rising to CP	0.0026	0.0026	0.0026	0.0026
TE ↑	hold_rising to CP	0.0101	0.0101	0.0101	0.0101
TE ↓	setup_rising to CP	0.0296	0.0296	0.0296	0.0296
TE ↑	setup_rising to CP	0.0471	0.0471	0.0471	0.0471
TI ↓	hold_rising to CP	-0.0166	-0.0166	-0.0166	-0.0182
TI ↑	hold_rising to CP	0.0101	0.0101	0.0101	0.0101
TI ↓	setup_rising to CP	0.0479	0.0479	0.0479	0.0472
TI ↑	setup_rising to CP	0.0146	0.0146	0.0146	0.0146

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P0	1.294e-03	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P0	1.160e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P0	1.272e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P0	1.743e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P0	1.971e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P0	2.242e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P0	2.294e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P0	2.984e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

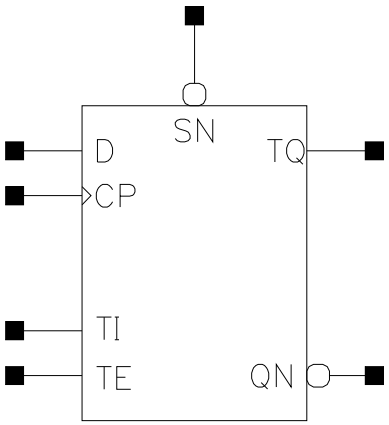
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P0	C8T28SOI_LLHF_-SDFPSQNX3_P0	C8T28SOIDV_LL_-SDFPSQNX5_P0	C8T28SOIDV_LL_-SDFPSQNX10_P0
Clock 100Mhz Data 0Mhz	1.120e-02	1.060e-02	1.005e-02	9.857e-03
Clock 100Mhz Data 25Mhz	1.082e-02	1.027e-02	9.876e-03	1.060e-02
Clock 100Mhz Data 50Mhz	1.043e-02	9.942e-03	9.704e-03	1.135e-02
Clock = 0 Data 100Mhz	5.160e-03	5.556e-03	5.358e-03	5.258e-03
Clock = 1 Data 100Mhz	4.441e-05	6.666e-04	4.616e-04	3.589e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P0	C8T28SOIDV_LL_-SDFPSQNX19_P0	C8T28SOIDV_LL_-SDFPSQNX23_P0	C8T28SOIDV_LL_-SDFPSQNX29_P0
Clock 100Mhz Data 0Mhz	9.742e-03	9.665e-03	9.610e-03	9.531e-03
Clock 100Mhz Data 25Mhz	1.096e-02	1.143e-02	1.162e-02	1.247e-02
Clock 100Mhz Data 50Mhz	1.218e-02	1.320e-02	1.363e-02	1.542e-02
Clock = 0 Data 100Mhz	5.197e-03	5.157e-03	5.128e-03	5.108e-03
Clock = 1 Data 100Mhz	2.973e-04	2.565e-04	2.271e-04	2.048e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P0	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P0	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P0	C8T28SOI_LLHF_-SDFPSQNTX3_P0	C8T28SOIDV_LL_-SDFPSQNTX5_P0	C8T28SOIDV_LL_-SDFPSQNTX10_P0
CP	0.0007	0.0007	0.0005	0.0005
D	0.0003	0.0005	0.0003	0.0003
SN	0.0014	0.0013	0.0010	0.0009
TE	0.0010	0.0008	0.0009	0.0009
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQNTX19_P0	C8T28SOIDV_LL_-SDFPSQNTX23_P0	C8T28SOIDV_LL_-SDFPSQNTX29_P0	
CP	0.0005	0.0005	0.0005	
D	0.0003	0.0003	0.0003	
SN	0.0009	0.0010	0.0010	
TE	0.0009	0.0009	0.0009	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P0	**C8T28SOI_LLHF_-SDFPSQNTX3_P0**	**C8T28SOI_LL_-SDFPSQNTX5_P0**	**C8T28SOI_LLHF_-SDFPSQNTX3_P0**
CP to QN ↓	0.0515	0.0502	2.5898	3.6346
CP to QN ↑	0.0501	0.0465	3.0383	4.3091
CP to TQ ↓	0.0410	0.0332	6.2572	4.2542
CP to TQ ↑	0.0433	0.0398	13.3773	7.3228
SN to QN ↓	0.0370	0.0330	2.5949	3.6402
SN to TQ ↑	0.0299	0.0236	13.3378	7.2853
	C8T28SOIDV_LL_-SDFPSQNTX5_P0	**C8T28SOIDV_LL_-SDFPSQNTX10_P0**	**C8T28SOIDV_LL_-SDFPSQNTX5_P0**	**C8T28SOIDV_LL_-SDFPSQNTX10_P0**
CP to QN ↓	0.0506	0.0487	2.3469	1.1746
CP to QN ↑	0.0427	0.0446	2.8736	1.4476
CP to TQ ↓	0.0303	0.0344	4.2787	4.3103
CP to TQ ↑	0.0390	0.0410	6.3673	6.4162
SN to QN ↓	0.0331	0.0313	2.3535	1.1753
SN to TQ ↑	0.0224	0.0238	6.3403	6.3679
	C8T28SOIDV_LL_-SDFPSQNTX19_P0	**C8T28SOIDV_LL_-SDFPSQNTX23_P0**	**C8T28SOIDV_LL_-SDFPSQNTX19_P0**	**C8T28SOIDV_LL_-SDFPSQNTX23_P0**
CP to QN ↓	0.0518	0.0531	0.5921	0.4758
CP to QN ↑	0.0482	0.0472	0.7311	0.7271
CP to TQ ↓	0.0343	0.0348	4.3129	4.3327
CP to TQ ↑	0.0409	0.0414	6.4168	6.4209
SN to QN ↓	0.0341	0.0350	0.5925	0.4755
SN to TQ ↑	0.0238	0.0241	6.3697	6.3729
	C8T28SOIDV_LL_-SDFPSQNTX29_P0		**C8T28SOIDV_LL_-SDFPSQNTX29_P0**	
CP to QN ↓	0.0531		0.4127	
CP to QN ↑	0.0488		0.4889	

CP to TQ ↓	0.0360		4.3995	
CP to TQ ↑	0.0441		7.2862	
SN to QN ↓	0.0343		0.4125	
SN to TQ ↑	0.0256		7.2201	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P0	C8T28SOI_-LLHF_-SDFPSQNTX3_-P0	C8T28SOIDV_-LL_-SDFPSQNTX5_-P0	C8T28SOIDV_-LL_SDFP-SQNTX10_P0
CP ↓	min_pulse_width to CP	0.0568	0.0575	0.0448	0.0448
CP ↑	min_pulse_width to CP	0.0329	0.0283	0.0283	0.0317
D ↓	hold_rising to CP	-0.0196	-0.0425	0.0004	0.0004
D ↑	hold_rising to CP	0.0025	0.0048	0.0079	0.0079
D ↓	setup_rising to CP	0.0461	0.0773	0.0294	0.0321
D ↑	setup_rising to CP	0.0217	0.0217	0.0169	0.0169
SN ↓	min_pulse_width to SN	0.0354	0.0305	0.0283	0.0283
SN ↑	recovery_rising to CP	0.0031	-0.0027	-0.0071	-0.0039
SN ↑	removal_rising to CP	0.0115	0.0169	0.0184	0.0217
TE ↓	hold_rising to CP	-0.0061	-0.0083	0.0026	0.0026
TE ↑	hold_rising to CP	0.0046	0.0082	0.0101	0.0101
TE ↓	setup_rising to CP	0.0440	0.0628	0.0296	0.0296
TE ↑	setup_rising to CP	0.0547	0.0684	0.0471	0.0471
TI ↓	hold_rising to CP	-0.0257	-0.0445	-0.0182	-0.0182
TI ↑	hold_rising to CP	0.0031	0.0103	0.0101	0.0101
TI ↓	setup_rising to CP	0.0554	0.0748	0.0479	0.0472
TI ↑	setup_rising to CP	0.0208	0.0205	0.0146	0.0146
		C8T28SOIDV_-LL_SDFP-SQNTX19_P0	C8T28SOIDV_-LL_SDFP-SQNTX23_P0	C8T28SOIDV_-LL_SDFP-SQNTX29_P0	
CP ↓	min_pulse_width to CP	0.0448	0.0448	0.0448	
CP ↑	min_pulse_width to CP	0.0316	0.0316	0.0316	
D ↓	hold_rising to CP	0.0004	0.0004	0.0004	
D ↑	hold_rising to CP	0.0079	0.0079	0.0079	
D ↓	setup_rising to CP	0.0321	0.0321	0.0321	
D ↑	setup_rising to CP	0.0169	0.0169	0.0169	
SN ↓	min_pulse_width to SN	0.0283	0.0283	0.0332	

SN ↑	recovery_rising to CP	-0.0039	-0.0039	-0.0039	
SN ↑	removal_rising to CP	0.0185	0.0185	0.0185	
TE ↓	hold_rising to CP	0.0026	0.0026	0.0026	
TE ↑	hold_rising to CP	0.0101	0.0101	0.0101	
TE ↓	setup_rising to CP	0.0296	0.0296	0.0296	
TE ↑	setup_rising to CP	0.0471	0.0471	0.0471	
TI ↓	hold_rising to CP	-0.0182	-0.0182	-0.0182	
TI ↑	hold_rising to CP	0.0101	0.0101	0.0101	
TI ↓	setup_rising to CP	0.0472	0.0472	0.0472	
TI ↑	setup_rising to CP	0.0146	0.0146	0.0146	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P0	1.276e-03	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P0	1.228e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P0	1.361e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_P0	1.815e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_P0	2.324e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_P0	2.382e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_P0	3.055e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

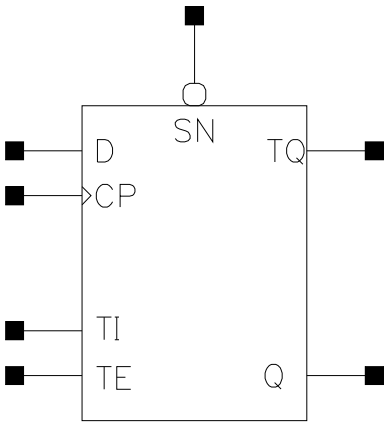
Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P0	C8T28SOI_LLHF_-SDFPSQNTX3_P0	C8T28SOIDV_LL_-SDFPSQNTX5_P0	C8T28SOIDV_LL_-SDFPSQNTX10_P0
Clock 100Mhz Data 0Mhz	1.093e-02	1.046e-02	9.962e-03	9.711e-03
Clock 100Mhz Data 25Mhz	1.098e-02	1.057e-02	1.001e-02	1.080e-02
Clock 100Mhz Data 50Mhz	1.104e-02	1.068e-02	1.007e-02	1.189e-02
Clock = 0 Data 100Mhz	5.148e-03	5.546e-03	5.351e-03	5.254e-03
Clock = 1 Data 100Mhz	4.532e-05	6.613e-04	4.580e-04	3.563e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P0	C8T28SOIDV_LL_-SDFPSQNTX23_P0	C8T28SOIDV_LL_-SDFPSQNTX29_P0	
Clock 100Mhz Data 0Mhz	9.560e-03	9.460e-03	9.390e-03	
Clock 100Mhz Data 25Mhz	1.172e-02	1.188e-02	1.286e-02	
Clock 100Mhz Data 50Mhz	1.387e-02	1.429e-02	1.633e-02	
Clock = 0 Data 100Mhz	5.196e-03	5.158e-03	5.131e-03	
Clock = 1 Data 100Mhz	2.952e-04	2.544e-04	2.259e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P0	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P0	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P0	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P0	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P0	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P0	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P0	C8T28SOI_LLHF_-SDFPSQTX3_P0	C8T28SOIDV_LL_-SDFPSQTX5_P0	C8T28SOIDV_LL_-SDFPSQTX10_P0
CP	0.0007	0.0007	0.0005	0.0006
D	0.0003	0.0005	0.0003	0.0003
SN	0.0014	0.0013	0.0010	0.0010
TE	0.0010	0.0008	0.0009	0.0010
TI	0.0004	0.0005	0.0004	0.0004
	C8T28SOIDV_LL_-SDFPSQTX19_P0	C8T28SOIDV_LL_-SDFPSQTX29_P0		
CP	0.0006	0.0006		
D	0.0003	0.0003		
SN	0.0010	0.0010		
TE	0.0010	0.0010		
TI	0.0004	0.0004		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPSQTX5_P0	**C8T28SOI_LLHF_-SDFPSQTX3_P0**	**C8T28SOI_LL_-SDFPSQTX5_P0**	**C8T28SOI_LLHF_-SDFPSQTX3_P0**
CP to Q ↓	0.0436	0.0393	2.6373	3.9232
CP to Q ↑	0.0385	0.0404	2.9655	4.4804
CP to TQ ↓	0.0486	0.0371	6.6315	4.3736
CP to TQ ↑	0.0474	0.0425	13.4045	7.4537
SN to Q ↑	0.0249	0.0237	2.9097	4.4138
SN to TQ ↑	0.0319	0.0249	13.3459	7.4111
	C8T28SOIDV_LL_-SDFPSQTX5_P0	**C8T28SOIDV_LL_-SDFPSQTX10_P0**	**C8T28SOIDV_LL_-SDFPSQTX5_P0**	**C8T28SOIDV_LL_-SDFPSQTX10_P0**
CP to Q ↓	0.0348	0.0446	2.4288	1.1868
CP to Q ↑	0.0406	0.0595	2.9517	1.4749
CP to TQ ↓	0.0346	0.0457	4.3432	4.4117
CP to TQ ↑	0.0411	0.0618	6.4588	6.3312
SN to Q ↑	0.0239	0.0415	2.9185	1.4763
SN to TQ ↑	0.0239	0.0437	6.4271	6.3298
	C8T28SOIDV_LL_-SDFPSQTX19_P0	**C8T28SOIDV_LL_-SDFPSQTX29_P0**	**C8T28SOIDV_LL_-SDFPSQTX19_P0**	**C8T28SOIDV_LL_-SDFPSQTX29_P0**
CP to Q ↓	0.0482	0.0539	0.6125	0.4078
CP to Q ↑	0.0631	0.0680	0.7583	0.5031
CP to TQ ↓	0.0479	0.0302	3.8221	3.9219
CP to TQ ↑	0.0658	0.0428	7.2485	7.3300
SN to Q ↑	0.0449	0.0481	0.7588	0.5039
SN to TQ ↑	0.0477	0.0245	7.2550	7.2988

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_P0	C8T28SOI_-LLHF_-SDFPSQTX3_P0	C8T28SOIDV_-LL_-SDFPSQTX5_P0	C8T28SOIDV_-LL_-SDFPSQTX10_-P0
CP ↓	min_pulse_width to CP	0.0568	0.0575	0.0448	0.0449
CP ↑	min_pulse_width to CP	0.0377	0.0330	0.0317	0.0270
D ↓	hold_rising to CP	-0.0164	-0.0425	0.0004	-0.0017
D ↑	hold_rising to CP	0.0025	0.0048	0.0079	0.0079
D ↓	setup_rising to CP	0.0461	0.0773	0.0294	0.0347
D ↑	setup_rising to CP	0.0217	0.0217	0.0169	0.0168
SN ↓	min_pulse_width to SN	0.0354	0.0305	0.0283	0.0283
SN ↑	recovery_rising to CP	0.0031	-0.0027	-0.0071	-0.0071
SN ↑	removal_rising to CP	0.0115	0.0169	0.0185	0.0217
TE ↓	hold_rising to CP	-0.0061	-0.0083	0.0026	-0.0000
TE ↑	hold_rising to CP	0.0046	0.0082	0.0101	0.0080
TE ↓	setup_rising to CP	0.0440	0.0628	0.0296	0.0290
TE ↑	setup_rising to CP	0.0547	0.0684	0.0471	0.0471
TI ↓	hold_rising to CP	-0.0257	-0.0445	-0.0182	-0.0169
TI ↑	hold_rising to CP	0.0031	0.0103	0.0101	0.0034
TI ↓	setup_rising to CP	0.0554	0.0748	0.0479	0.0467
TI ↑	setup_rising to CP	0.0208	0.0205	0.0146	0.0208
		C8T28SOIDV_-LL_-SDFPSQTX19_-P0	C8T28SOIDV_-LL_-SDFPSQTX29_-P0		
CP ↓	min_pulse_width to CP	0.0449	0.0449		
CP ↑	min_pulse_width to CP	0.0270	0.0317		
D ↓	hold_rising to CP	-0.0017	-0.0017		
D ↑	hold_rising to CP	0.0079	0.0079		
D ↓	setup_rising to CP	0.0347	0.0347		
D ↑	setup_rising to CP	0.0169	0.0169		
SN ↓	min_pulse_width to SN	0.0283	0.0332		
SN ↑	recovery_rising to CP	-0.0071	-0.0071		
SN ↑	removal_rising to CP	0.0217	0.0217		
TE ↓	hold_rising to CP	-0.0000	-0.0000		
TE ↑	hold_rising to CP	0.0080	0.0080		

TE ↓	setup_rising to CP	0.0290	0.0290		
TE ↑	setup_rising to CP	0.0471	0.0471		
TI ↓	hold_rising to CP	-0.0169	-0.0169		
TI ↑	hold_rising to CP	0.0031	0.0031		
TI ↓	setup_rising to CP	0.0467	0.0467		
TI ↑	setup_rising to CP	0.0208	0.0209		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P0	1.224e-03	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P0	1.190e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P0	1.280e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P0	1.712e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P0	2.053e-03	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P0	2.688e-03	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

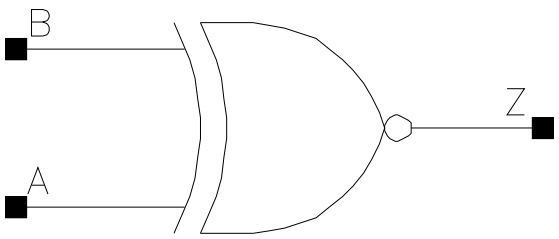
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P0	C8T28SOI_LLHF_-SDFPSQTX3_P0	C8T28SOIDV_LL_-SDFPSQTX5_P0	C8T28SOIDV_LL_-SDFPSQTX10_P0
Clock 100Mhz Data 0Mhz	1.094e-02	1.047e-02	9.970e-03	9.714e-03
Clock 100Mhz Data 25Mhz	1.128e-02	1.075e-02	1.018e-02	1.050e-02
Clock 100Mhz Data 50Mhz	1.161e-02	1.104e-02	1.040e-02	1.129e-02
Clock = 0 Data 100Mhz	5.147e-03	5.548e-03	5.351e-03	5.305e-03
Clock = 1 Data 100Mhz	4.425e-05	6.640e-04	4.594e-04	3.572e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P0	C8T28SOIDV_LL_-SDFPSQTX29_P0		
Clock 100Mhz Data 0Mhz	9.561e-03	9.459e-03		
Clock 100Mhz Data 25Mhz	1.145e-02	1.254e-02		
Clock 100Mhz Data 50Mhz	1.333e-02	1.561e-02		
Clock = 0 Data 100Mhz	5.266e-03	5.240e-03		
Clock = 1 Data 100Mhz	2.970e-04	2.561e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.600	0.544	0.8704
X5_P0	0.800	1.496	1.1968
X8_P0	1.600	1.088	1.7408
X9_P0	0.800	1.632	1.3056
X11_P0	1.600	1.360	2.1760
X14_P0	0.800	2.312	1.8496
X15_P0	1.600	1.904	3.0464
X19_P0	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P0	X5_P0	X8_P0	X9_P0
A	0.0010	0.0005	0.0016	0.0006
B	0.0009	0.0010	0.0013	0.0012
	X11_P0	X14_P0	X15_P0	X19_P0
A	0.0024	0.0010	0.0028	0.0011
B	0.0021	0.0016	0.0024	0.0018

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X5_P0	X4_P0	X5_P0
A to Z ↓	0.0105	0.0291	3.1077	2.4593
A to Z ↑	0.0124	0.0280	4.0939	3.1214
B to Z ↓	0.0095	0.0220	3.1127	2.4498
B to Z ↑	0.0138	0.0207	4.1064	3.1192

	X8_P0	X9_P0	X8_P0	X9_P0
A to Z ↓	0.0127	0.0279	1.6542	1.2627
A to Z ↑	0.0148	0.0275	2.2239	1.5989
B to Z ↓	0.0118	0.0214	1.6564	1.2606
B to Z ↑	0.0161	0.0208	2.2278	1.5988
	X11_P0	**X14_P0**	**X11_P0**	**X14_P0**
A to Z ↓	0.0121	0.0261	1.1571	0.8595
A to Z ↑	0.0135	0.0252	1.4461	1.0391
B to Z ↓	0.0107	0.0200	1.1583	0.8573
B to Z ↑	0.0146	0.0192	1.4497	1.0377
	X15_P0	**X19_P0**	**X15_P0**	**X19_P0**
A to Z ↓	0.0134	0.0246	0.8798	0.6420
A to Z ↑	0.0150	0.0245	1.1056	0.7728
B to Z ↓	0.0121	0.0195	0.8805	0.6401
B to Z ↑	0.0163	0.0189	1.1089	0.7718

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P0	6.685e-04	1.000e-20
X5_P0	6.854e-04	1.000e-20
X8_P0	1.036e-03	1.000e-20
X9_P0	1.151e-03	1.000e-20
X11_P0	1.614e-03	1.000e-20
X14_P0	1.829e-03	1.000e-20
X15_P0	2.002e-03	1.000e-20
X19_P0	2.563e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P0	X5_P0	X8_P0	X9_P0
A to Z	3.016e-03	5.680e-03	5.384e-03	8.655e-03
B to Z	2.940e-03	4.930e-03	5.330e-03	7.618e-03
	X11_P0	X14_P0	X15_P0	X19_P0
A to Z	8.037e-03	1.338e-02	1.060e-02	1.657e-02
B to Z	7.858e-03	1.158e-02	1.042e-02	1.462e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

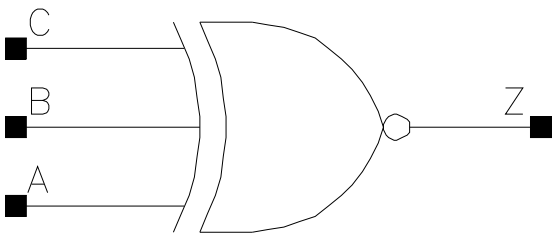
Pin Cycle (vdds)	X4_P0	X5_P0	X8_P0	X9_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P0	X14_P0	X15_P0	X19_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P0	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P0	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P0	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P0	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P0	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P0	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P0	C8T28SOIDV_LL_-XNOR3X4_P0	C8T28SOIDV_LL_-XNOR3X9_P0	C8T28SOIDV_LL_-XNOR3X13_P0
A	0.0015	0.0015	0.0019	0.0025
B	0.0015	0.0014	0.0018	0.0024
C	0.0007	0.0006	0.0006	0.0006
	C8T28SOIDV_LLS_-XNOR3X1_P0	C8T28SOIDV_LLS_-XNOR3X2_P0	C8T28SOIDV_LLS_-XNOR3X5_P0	C8T28SOIDV_LLS_-XNOR3X7_P0

A	0.0015	0.0017	0.0036	0.0055
B	0.0015	0.0018	0.0033	0.0051
C	0.0010	0.0012	0.0024	0.0035

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_XNOR3X2_P0	C8T28SOIDV_LL_XNOR3X4_P0	C8T28SOIDV_LL_XNOR3X2_P0	C8T28SOIDV_LL_XNOR3X4_P0
A to Z ↓	0.0285	0.0301	4.8304	2.6404
A to Z ↑	0.0280	0.0287	5.5081	3.1541
B to Z ↓	0.0294	0.0311	4.8310	2.6408
B to Z ↑	0.0289	0.0297	5.5137	3.1536
C to Z ↓	0.0401	0.0423	4.8302	2.6387
C to Z ↑	0.0395	0.0408	5.5156	3.1547
	C8T28SOIDV_LL_XNOR3X9_P0	C8T28SOIDV_LL_XNOR3X13_P0	C8T28SOIDV_LL_XNOR3X9_P0	C8T28SOIDV_LL_XNOR3X13_P0
A to Z ↓	0.0263	0.0305	1.3374	0.9162
A to Z ↑	0.0288	0.0336	1.5516	1.0877
B to Z ↓	0.0273	0.0316	1.3384	0.9168
B to Z ↑	0.0299	0.0349	1.5522	1.0879
C to Z ↓	0.0396	0.0480	1.3370	0.9165
C to Z ↑	0.0415	0.0512	1.5521	1.0877
	C8T28SOIDV_LLS_XNOR3X1_P0	C8T28SOIDV_LLS_XNOR3X2_P0	C8T28SOIDV_LLS_XNOR3X1_P0	C8T28SOIDV_LLS_XNOR3X2_P0
A to Z ↓	0.0177	0.0198	8.1741	4.6217
A to Z ↑	0.0185	0.0186	11.5303	6.3146
B to Z ↓	0.0187	0.0209	8.1981	4.6323
B to Z ↑	0.0194	0.0197	11.5416	6.3215
C to Z ↓	0.0185	0.0202	8.2233	4.6513
C to Z ↑	0.0191	0.0190	11.5555	6.3356
	C8T28SOIDV_LLS_XNOR3X5_P0	C8T28SOIDV_LLS_XNOR3X7_P0	C8T28SOIDV_LLS_XNOR3X5_P0	C8T28SOIDV_LLS_XNOR3X7_P0
A to Z ↓	0.0209	0.0180	2.2641	1.5617
A to Z ↑	0.0204	0.0174	3.1590	2.1140
B to Z ↓	0.0212	0.0180	2.2710	1.5678
B to Z ↑	0.0207	0.0175	3.1629	2.1179
C to Z ↓	0.0207	0.0180	2.2749	1.5712
C to Z ↑	0.0201	0.0171	3.1637	2.1199

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P0	5.107e-04	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P0	6.053e-04	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P0	1.051e-03	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P0	1.508e-03	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P0	3.287e-04	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P0	5.691e-04	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P0	1.286e-03	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P0	2.032e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P0	C8T28SOIDV_LL_-XNOR3X4_P0	C8T28SOIDV_LL_-XNOR3X9_P0	C8T28SOIDV_LL_-XNOR3X13_P0
A to Z	3.266e-03	4.110e-03	6.549e-03	1.090e-02
B to Z	3.260e-03	4.108e-03	6.602e-03	1.099e-02
C to Z	5.036e-03	5.911e-03	8.655e-03	1.408e-02
	C8T28SOIDV_LLS_-XNOR3X1_P0	C8T28SOIDV_LLS_-XNOR3X2_P0	C8T28SOIDV_LLS_-XNOR3X5_P0	C8T28SOIDV_LLS_-XNOR3X7_P0
A to Z	1.931e-03	2.872e-03	6.184e-03	8.687e-03
B to Z	1.922e-03	2.902e-03	6.314e-03	8.670e-03
C to Z	1.901e-03	2.870e-03	6.313e-03	8.686e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

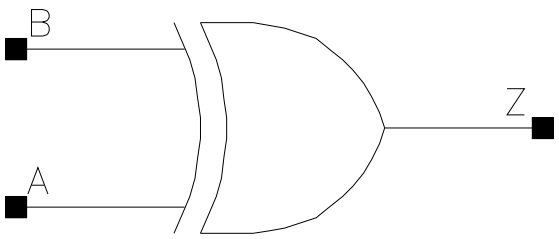
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P0	C8T28SOIDV_LL_-XNOR3X4_P0	C8T28SOIDV_LL_-XNOR3X9_P0	C8T28SOIDV_LL_-XNOR3X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P0	C8T28SOIDV_LLS_-XNOR3X2_P0	C8T28SOIDV_LLS_-XNOR3X5_P0	C8T28SOIDV_LLS_-XNOR3X7_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P0	0.800	1.360	1.0880
X4_P0	1.600	0.544	0.8704
X5_P0	0.800	1.360	1.0880
X8_P0	1.600	1.088	1.7408
X9_P0	0.800	1.496	1.1968
X12_P0	1.600	1.360	2.1760
X13_P0	0.800	2.176	1.7408
X15_P0	1.600	1.904	3.0464
X17_P0	0.800	2.312	1.8496
X18_P0	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P0	X4_P0	X5_P0	X8_P0
A	0.0005	0.0010	0.0007	0.0015
B	0.0010	0.0009	0.0011	0.0014
	X9_P0	X12_P0	X13_P0	X15_P0
A	0.0007	0.0025	0.0012	0.0029
B	0.0014	0.0018	0.0022	0.0023
	X17_P0	X18_P0		
A	0.0012	0.0016		
B	0.0022	0.0019		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P0	**X4_P0**	**X2_P0**	**X4_P0**
A to Z ↓	0.0248	0.0099	4.6496	2.4371
A to Z ↑	0.0251	0.0139	5.6783	5.4130
B to Z ↓	0.0198	0.0110	4.6163	2.4581
B to Z ↑	0.0199	0.0126	5.6651	5.4141
	X5_P0	**X8_P0**	**X5_P0**	**X8_P0**
A to Z ↓	0.0237	0.0129	2.5657	1.3264
A to Z ↑	0.0228	0.0168	3.0557	2.8785
B to Z ↓	0.0188	0.0146	2.5539	1.3416
B to Z ↑	0.0180	0.0156	3.0533	2.8794
	X9_P0	**X12_P0**	**X9_P0**	**X12_P0**
A to Z ↓	0.0235	0.0115	1.3341	0.8906
A to Z ↑	0.0235	0.0151	1.6048	1.9298
B to Z ↓	0.0187	0.0125	1.3283	0.8997
B to Z ↑	0.0183	0.0134	1.6013	1.9312
	X13_P0	**X15_P0**	**X13_P0**	**X15_P0**
A to Z ↓	0.0216	0.0125	0.9139	0.6962
A to Z ↑	0.0214	0.0175	1.1020	1.7181
B to Z ↓	0.0157	0.0133	0.9114	0.7038
B to Z ↑	0.0152	0.0157	1.1000	1.7187
	X17_P0	**X18_P0**	**X17_P0**	**X18_P0**
A to Z ↓	0.0229	0.0260	0.6894	0.6832
A to Z ↑	0.0224	0.0246	0.8233	0.7788
B to Z ↓	0.0170	0.0215	0.6876	0.6827
B to Z ↑	0.0164	0.0193	0.8229	0.7783

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P0	5.579e-04	1.000e-20
X4_P0	6.118e-04	1.000e-20
X5_P0	8.660e-04	1.000e-20
X8_P0	9.379e-04	1.000e-20
X9_P0	1.462e-03	1.000e-20
X12_P0	1.485e-03	1.000e-20
X13_P0	2.379e-03	1.000e-20
X15_P0	1.725e-03	1.000e-20
X17_P0	2.577e-03	1.000e-20
X18_P0	2.527e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P0	X4_P0	X5_P0	X8_P0
A to Z	4.121e-03	2.976e-03	5.393e-03	5.471e-03
B to Z	3.837e-03	2.901e-03	5.001e-03	5.424e-03
	X9_P0	X12_P0	X13_P0	X15_P0
A to Z	8.153e-03	7.940e-03	1.328e-02	9.881e-03
B to Z	7.696e-03	7.744e-03	1.100e-02	9.729e-03
	X17_P0	X18_P0		
A to Z	1.536e-02	1.730e-02		
B to Z	1.307e-02	1.529e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

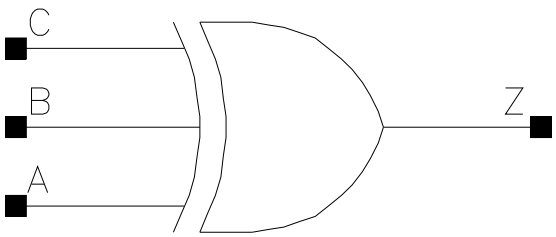
Pin Cycle (vdds)	X2_P0	X4_P0	X5_P0	X8_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P0	X12_P0	X13_P0	X15_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P0	X18_P0		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P0	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P0	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P0	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P0	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P0	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P0	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P0	C8T28SOIDV_LL_-XOR3X4_P0	C8T28SOIDV_LL_-XOR3X9_P0	C8T28SOIDV_LL_-XOR3X13_P0
A	0.0016	0.0015	0.0018	0.0025
B	0.0015	0.0016	0.0018	0.0024
C	0.0010	0.0010	0.0012	0.0020
	C8T28SOIDV_LLS_-XOR3X1_P0	C8T28SOIDV_LLS_-XOR3X2_P0	C8T28SOIDV_LLS_-XOR3X5_P0	C8T28SOIDV_LLS_-XOR3X7_P0

A	0.0016	0.0017	0.0029	0.0045
B	0.0017	0.0017	0.0029	0.0046
C	0.0006	0.0005	0.0005	0.0009

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P0	**C8T28SOIDV_LL_-XOR3X4_P0**	**C8T28SOIDV_LL_-XOR3X2_P0**	**C8T28SOIDV_LL_-XOR3X4_P0**
A to Z ↓	0.0277	0.0305	4.8517	2.6514
A to Z ↑	0.0273	0.0295	5.6705	3.1575
B to Z ↓	0.0285	0.0317	4.8553	2.6524
B to Z ↑	0.0281	0.0307	5.6697	3.1603
C to Z ↓	0.0283	0.0314	4.8566	2.6544
C to Z ↑	0.0281	0.0305	5.6697	3.1556
	C8T28SOIDV_LL_-XOR3X9_P0	**C8T28SOIDV_LL_-XOR3X13_P0**	**C8T28SOIDV_LL_-XOR3X9_P0**	**C8T28SOIDV_LL_-XOR3X13_P0**
A to Z ↓	0.0285	0.0315	1.3263	0.9058
A to Z ↑	0.0294	0.0342	1.5646	1.0525
B to Z ↓	0.0296	0.0325	1.3272	0.9059
B to Z ↑	0.0305	0.0354	1.5643	1.0519
C to Z ↓	0.0291	0.0325	1.3277	0.9069
C to Z ↑	0.0300	0.0356	1.5639	1.0525
	C8T28SOIDV_LLS_-XOR3X1_P0	**C8T28SOIDV_LLS_-XOR3X2_P0**	**C8T28SOIDV_LLS_-XOR3X1_P0**	**C8T28SOIDV_LLS_-XOR3X2_P0**
A to Z ↓	0.0187	0.0207	5.8479	4.7110
A to Z ↑	0.0187	0.0185	8.4055	6.0416
B to Z ↓	0.0197	0.0215	5.8766	4.7211
B to Z ↑	0.0197	0.0194	8.4163	6.0490
C to Z ↓	0.0310	0.0333	5.8123	4.6811
C to Z ↑	0.0313	0.0315	8.4053	6.0250
	C8T28SOIDV_LLS_-XOR3X5_P0	**C8T28SOIDV_LLS_-XOR3X7_P0**	**C8T28SOIDV_LLS_-XOR3X5_P0**	**C8T28SOIDV_LLS_-XOR3X7_P0**
A to Z ↓	0.0274	0.0235	2.4592	1.6986
A to Z ↑	0.0238	0.0204	3.1824	2.1580
B to Z ↓	0.0269	0.0241	2.4683	1.7035
B to Z ↑	0.0239	0.0211	3.1891	2.1617
C to Z ↓	0.0465	0.0387	2.4558	1.6916
C to Z ↑	0.0435	0.0358	3.1761	2.1533

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P0	4.095e-04	1.000e-20
C8T28SOIDV_LL_XOR3X4_P0	5.219e-04	1.000e-20
C8T28SOIDV_LL_XOR3X9_P0	9.615e-04	1.000e-20
C8T28SOIDV_LL_XOR3X13_P0	1.408e-03	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P0	5.792e-04	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P0	6.925e-04	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P0	1.140e-03	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P0	1.748e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P0	C8T28SOIDV_LL_-XOR3X4_P0	C8T28SOIDV_LL_-XOR3X9_P0	C8T28SOIDV_LL_-XOR3X13_P0
A to Z	3.108e-03	4.112e-03	6.608e-03	1.127e-02
B to Z	3.096e-03	4.119e-03	6.664e-03	1.135e-02
C to Z	3.078e-03	4.094e-03	6.635e-03	1.136e-02
	C8T28SOIDV_LLS_-XOR3X1_P0	C8T28SOIDV_LLS_-XOR3X2_P0	C8T28SOIDV_LLS_-XOR3X5_P0	C8T28SOIDV_LLS_-XOR3X7_P0
A to Z	2.435e-03	2.958e-03	5.999e-03	8.393e-03
B to Z	2.430e-03	2.985e-03	6.146e-03	8.563e-03
C to Z	4.379e-03	4.965e-03	9.424e-03	1.311e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P0	C8T28SOIDV_LL_-XOR3X4_P0	C8T28SOIDV_LL_-XOR3X9_P0	C8T28SOIDV_LL_-XOR3X13_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P0	C8T28SOIDV_LLS_-XOR3X2_P0	C8T28SOIDV_LLS_-XOR3X5_P0	C8T28SOIDV_LLS_-XOR3X7_P0
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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