



**This document explains how to do corners analysis in ADE-L in IC 6.1.6 with a ST PDK.**

To run corners simulation in ADE-L, follow this procedure:

1. Copy the following corners files in your working directory:

EldoD : \$PDKITROOT/DATA/MODELS/ELDO/CORNERS/corners.  
 HspiceD : \$PDKITROOT/DATA/MODELS/HSPICE/CORNERS/corners.  
 Spectre : \$PDKITROOT/DATA/MODELS/SPECTRE/CORNERS/corners.scs.  
 GoldenGate : \$PDKITROOT/DATA/MODELS/GOLDENGATE/CORNERS/corners.scs.

These files contain:

- The link to the models with the setting of the corners.
- The setting of mdev flags for each device family. When set to 1, the mismatch is taken into account during simulation for the corresponding family.
- The setting of SOA flags for each device family for eldoD, spectre and hspiceD simulators.

The corners file included in this PDK are configured with typical corners and with all flags deactivated

2. Modify the corners file by choosing the corners, and setting the flags you want for your simulation

The list of corners supported for each models is described under

\$PDKITROOT/doc/TECHNOLOGY/MODELS directory:

EldoD : **eldo\_models\_list.html** file  
 HspiceD: **hspice\_models\_list.html** file  
 Spectre: **spectre\_models\_list.html** file  
 GoldenGate : **GoldenGate\_models\_list.html** file

3. Add the following lines in your .cdsinit :

For eldoD :

```
asiSetEnvOptionVal(asiGetTool('eldoD') "modelFiles" list("<path of corners file updated in step2>/corners"))
```

For hspiceD:

```
asiSetEnvOptionVal(asiGetTool('hspiceD') "modelFiles" list("<path of corners file updated in step2>/corners"))
```

For spectre:

```
asiSetEnvOptionVal(asiGetTool('spectre') "modelFiles" list("<path of corners file updated in step2>/corners.scs"))
```

For GoldenGate:

```
asiSetEnvOptionVal(asiGetTool('GoldenGate') "modelFiles" list("<path of corners file updated in step2>/corners.scs"))
```

4. Launch virtuoso
5. Do the setup of your design in ADE-L and run Simulation:
  - a. Virtuoso (test bench cellview) --> Launch --> ADE L
  - b. Setup --> simulator --> <simulator> (eldoD,spectre,hspiceD or GoldenGate)
  - c. Analysis --> Choose your analysis
  - d. Simulation --> Netlist and Run
6. Verify that the corner file is included in your netlist:
  - a. Simulation --> Netlist → Create



```
File Edit View Help cadence
// Generated for: spectre
// Generated on: Nov 18 14:42:15 2015
// Design library name: cmos32lp_TopCells
// Design cell name:
// Vain_ST_G32_addon_AMS_ST_G32_addon_DP_cmos32lp_testbench
// Design view name: schematic
simulator lang=spectre
global 0 VSS!
parameters vss
include "/work/uptplusscache/areas/dk/vip/PDK_STM_cmos28FDSOI_AMS_6V1x_2U2x_2T8x_LB/2.5.h-DEV-03/DATA/MODELS/SPECTRE/CORNERS/corners.scs"
// Library name: cmos32lp
// Cell name: eglvtnfetnp
// View name: schematic
subckt eglvtnfetnp b d g s sx
parameters w=160.00n l=150.00n sa=ad _par0=1 gateSplitStripes=1 \
sa=(120n)+(0) sb=(120n)+(0) gateSpacing=140n ptwell=0 mult=1 \
ngcon=1 nsig delvto uo1=0 nsig delvto uo2=0 soa=1 svsh=0 swacc=-1 \
svrg=-1 _par1=1 sd=(2*(70n)) geo_nw_offset=167n \
geo_nw_offset=167n
N0 (d g s b) eglvtnfet u-v l=1 sa=sa ad=ad \
nf=( _par0)*(gateSplitStripes) sa=sa sb=sb sd=gateSpacing \
ptwell=ptwell par=mult p_la=0 ngcon=ngcon \
nsig delvto uo1=nsig delvto uo1 nsig delvto uo2=nsig delvto uo2 \
soa=soa svsh=svsh swacc=swacc svrg=svrg svsub=-1 mismatch=_par1 \
n=1
D0 (sx b) diodenrc_lvs \
area=(1*_par0*sa+sb+sd*( _par0-1)+2*geo_nw_offset)*(w/_par0+2*geo_nw_offset) \
perim=2*((1*_par0*sa+sb+sd*( _par0-1)+2*geo_nw_offset)+(w/_par0+2*geo_nw_offset)) \
```