C28SOI_SC_12_COREPBP10_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 10 nm

Overview

- C28SOI_SC_12_COREPBP10_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

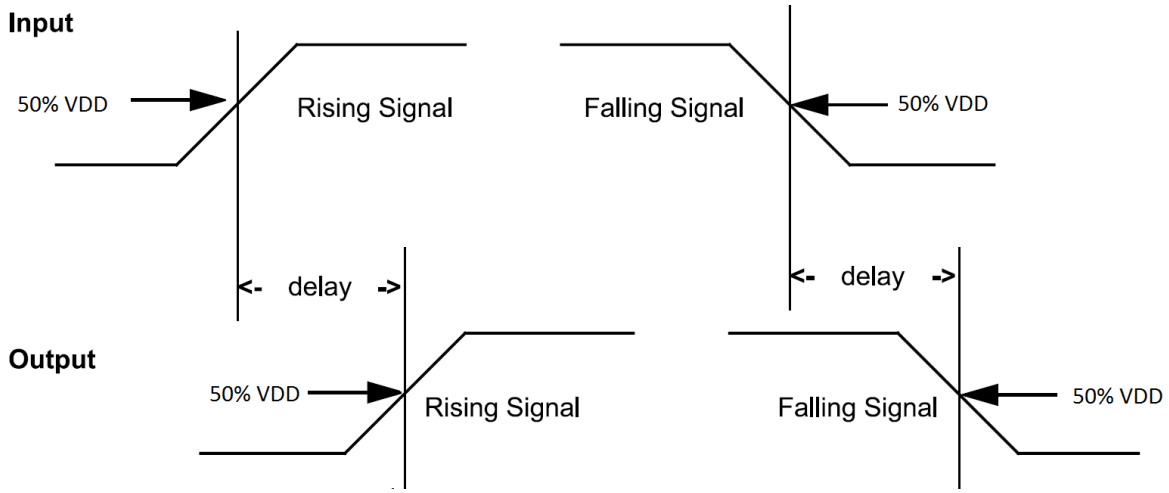


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

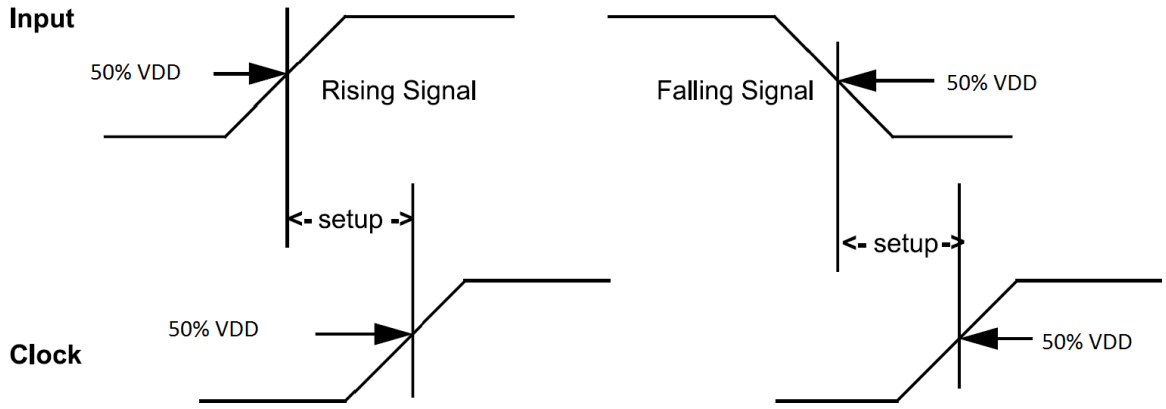


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

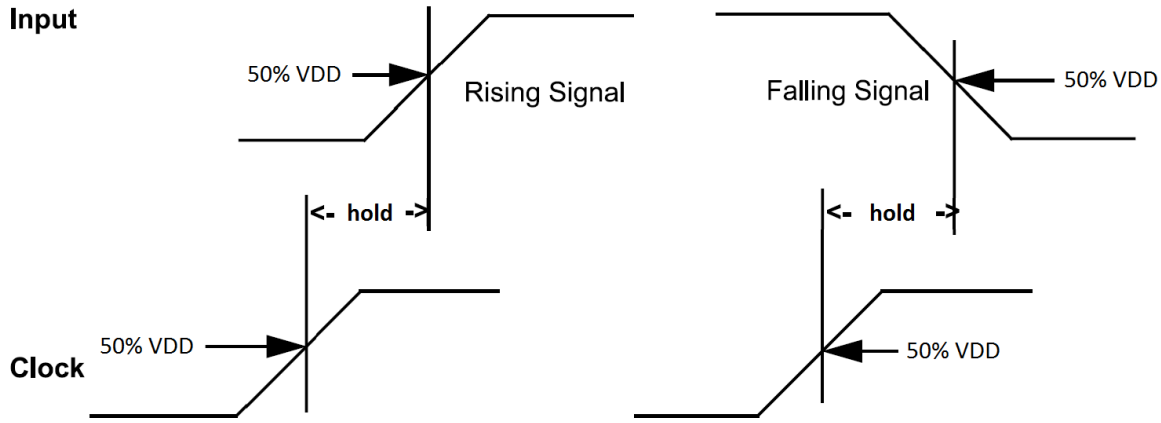


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

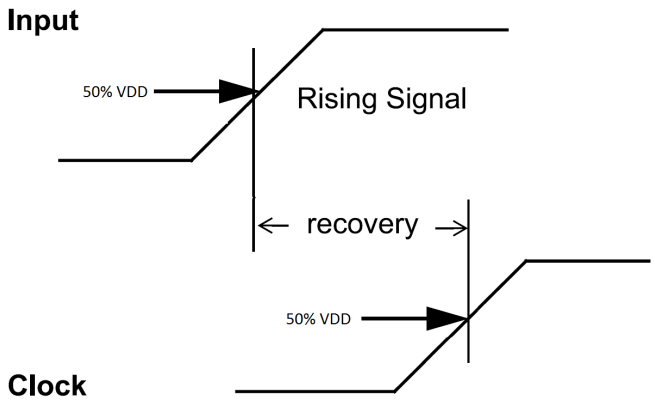


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

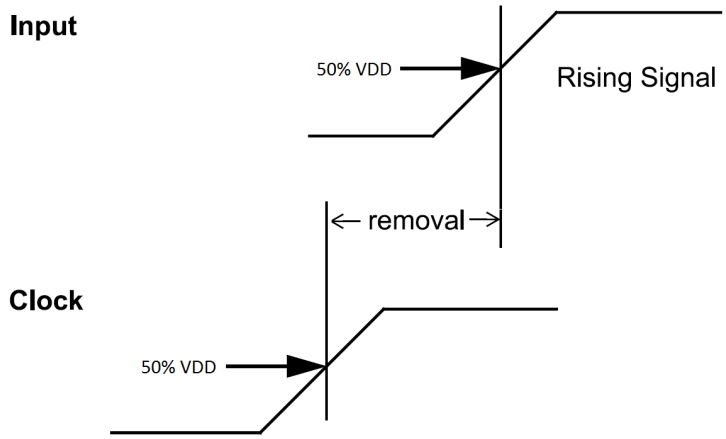


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

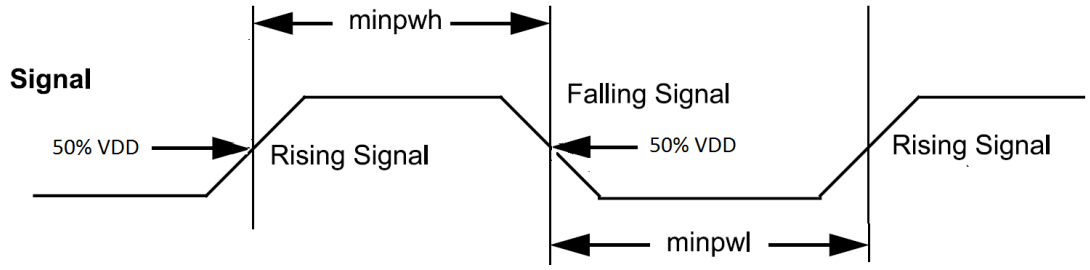


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

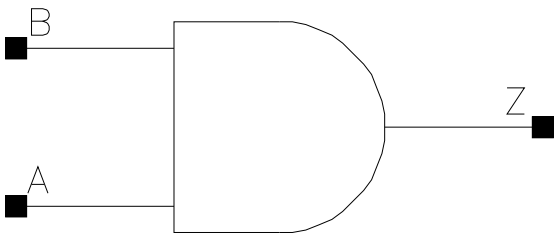
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X25_P10	1.200	1.088	1.3056
X33_P10	1.200	1.360	1.6320
X42_P10	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0008	0.0011	0.0017	0.0020
B	0.0007	0.0010	0.0016	0.0021
	X42_P10			
A	0.0020			
B	0.0020			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0370	0.0299	2.4616	1.2483
A to Z ↑	0.0301	0.0276	4.0154	1.9603
B to Z ↓	0.0352	0.0282	2.4568	1.2461
B to Z ↑	0.0316	0.0289	4.0167	1.9619
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0308	0.0296	0.8235	0.6125

A to Z ↑	0.0271	0.0277	1.2905	0.9726
B to Z ↓	0.0291	0.0270	0.8231	0.6116
B to Z ↑	0.0284	0.0280	1.2899	0.9725
	X42_P10		**X42_P10**	
A to Z ↓	0.0320		0.4971	
A to Z ↑	0.0302		0.7787	
B to Z ↓	0.0294		0.4964	
B to Z ↑	0.0305		0.7777	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	9.975e-06	1.000e-20
X16_P10	2.112e-05	1.000e-20
X25_P10	3.095e-05	1.000e-20
X33_P10	4.286e-05	1.000e-20
X42_P10	4.972e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	8.909e-06	1.756e-05	2.662e-05	6.812e-05
B (output stable)	1.913e-05	3.467e-05	5.398e-05	2.226e-04
A to Z	2.003e-03	3.299e-03	5.086e-03	6.676e-03
B to Z	1.906e-03	3.129e-03	4.816e-03	6.070e-03
	X42_P10			
A (output stable)	6.941e-05			
B (output stable)	2.200e-04			
A to Z	8.051e-03			
B to Z	7.430e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

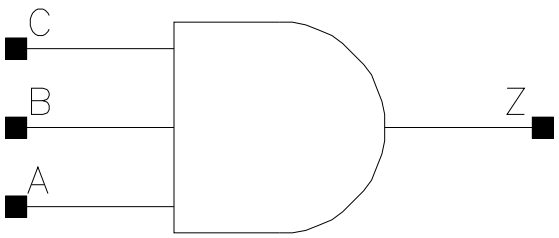
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X25_P10	1.200	1.360	1.6320
X33_P10	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0007	0.0011	0.0017	0.0021
B	0.0006	0.0010	0.0016	0.0020
C	0.0006	0.0011	0.0014	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0399	0.0330	2.4883	1.2146
A to Z ↑	0.0391	0.0362	4.0562	1.9391
B to Z ↓	0.0386	0.0316	2.4868	1.2140
B to Z ↑	0.0396	0.0367	4.0555	1.9411
C to Z ↓	0.0370	0.0300	2.4839	1.2132
C to Z ↑	0.0408	0.0371	4.0562	1.9405
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0330	0.0313	0.8317	0.6217

A to Z ↑	0.0351	0.0338	1.3172	0.9870
B to Z ↓	0.0317	0.0298	0.8301	0.6219
B to Z ↑	0.0358	0.0344	1.3160	0.9868
C to Z ↓	0.0299	0.0282	0.8306	0.6210
C to Z ↑	0.0363	0.0349	1.3159	0.9860

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	9.521e-06	1.000e-20
X17_P10	2.075e-05	1.000e-20
X25_P10	2.958e-05	1.000e-20
X33_P10	4.058e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	1.057e-05	2.210e-05	2.920e-05	4.109e-05
B (output stable)	1.390e-05	2.922e-05	4.120e-05	5.737e-05
C (output stable)	3.937e-05	8.011e-05	1.184e-04	1.668e-04
A to Z	2.221e-03	3.914e-03	5.612e-03	7.238e-03
B to Z	2.118e-03	3.727e-03	5.331e-03	6.849e-03
C to Z	2.033e-03	3.541e-03	5.054e-03	6.472e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

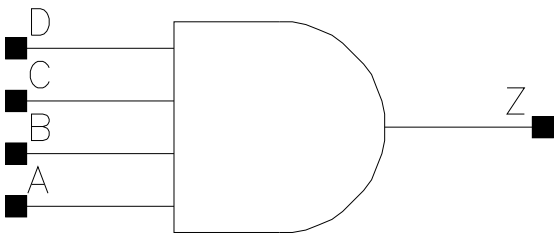
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X6_P10	1.200	1.088	1.3056
X20_P10	1.200	2.312	2.7744
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P10	X6_P10	X20_P10	X27_P10
A	0.0005	0.0008	0.0018	0.0020
B	0.0005	0.0007	0.0018	0.0020
C	0.0005	0.0008	0.0018	0.0020
D	0.0005	0.0007	0.0018	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X6_P10	X4_P10	X6_P10
A to Z ↓	0.0422	0.0359	4.6973	3.0393
A to Z ↑	0.0406	0.0312	13.7258	7.2514
B to Z ↓	0.0411	0.0338	4.6974	3.0379
B to Z ↑	0.0425	0.0323	13.7316	7.2530
C to Z ↓	0.0437	0.0385	4.6675	3.0533
C to Z ↑	0.0405	0.0308	13.7355	7.2638

D to Z ↓	0.0426	0.0358	4.6692	3.0460
D to Z ↑	0.0432	0.0320	13.7469	7.2623
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0346	0.0320	0.8787	0.6205
A to Z ↑	0.0322	0.0359	2.4074	1.8242
B to Z ↓	0.0315	0.0295	0.8773	0.6199
B to Z ↑	0.0323	0.0363	2.4075	1.8241
C to Z ↓	0.0337	0.0307	0.8838	0.6224
C to Z ↑	0.0284	0.0309	2.4077	1.8228
D to Z ↓	0.0304	0.0282	0.8816	0.6221
D to Z ↑	0.0284	0.0313	2.4072	1.8225

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	4.865e-06	1.000e-20
X6_P10	1.238e-05	1.000e-20
X20_P10	3.754e-05	1.000e-20
X27_P10	4.806e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	3.423e-04	5.389e-04	1.593e-03	1.965e-03
B (output stable)	3.211e-04	4.911e-04	1.433e-03	1.796e-03
C (output stable)	3.297e-04	5.477e-04	1.379e-03	1.702e-03
D (output stable)	3.128e-04	4.965e-04	1.203e-03	1.525e-03
A to Z	1.423e-03	2.221e-03	6.738e-03	8.721e-03
B to Z	1.363e-03	2.094e-03	6.160e-03	8.130e-03
C to Z	1.408e-03	2.251e-03	5.739e-03	7.143e-03
D to Z	1.347e-03	2.114e-03	5.145e-03	6.547e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

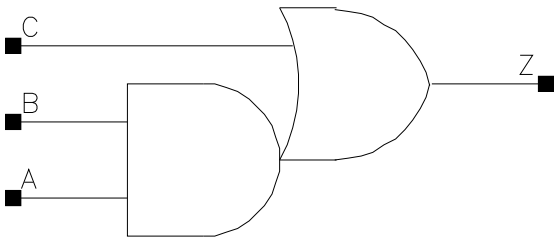
Pin Cycle (vdds)	X4_P10	X6_P10	X20_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0010	0.0021
B	0.0006	0.0010	0.0019
C	0.0007	0.0011	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0461	0.0404	2.5256	1.2360
A to Z ↑	0.0310	0.0276	3.9368	1.9244
B to Z ↓	0.0429	0.0375	2.5200	1.2326
B to Z ↑	0.0329	0.0294	3.9374	1.9208
C to Z ↓	0.0459	0.0404	2.5158	1.2314
C to Z ↑	0.0282	0.0264	3.9133	1.9136
	X33_P10		**X33_P10**	
A to Z ↓	0.0405		0.6256	
A to Z ↑	0.0281		0.9673	

B to Z ↓	0.0374		0.6249	
B to Z ↑	0.0292		0.9673	
C to Z ↓	0.0404		0.6239	
C to Z ↑	0.0258		0.9636	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.025e-05	1.000e-20
X17_P10	2.157e-05	1.000e-20
X33_P10	4.299e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.562e-05	4.913e-05	1.135e-04
B (output stable)	2.956e-05	5.762e-05	1.455e-04
C (output stable)	4.202e-05	7.172e-05	1.662e-04
A to Z	2.067e-03	3.583e-03	7.109e-03
B to Z	1.965e-03	3.385e-03	6.628e-03
C to Z	2.265e-03	3.925e-03	7.788e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

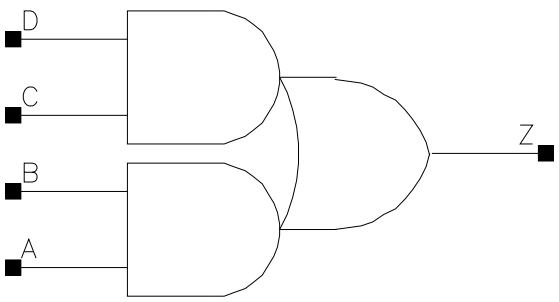
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0010	0.0020
B	0.0007	0.0010	0.0018
C	0.0006	0.0009	0.0020
D	0.0007	0.0010	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0535	0.0458	2.4317	1.2245
A to Z ↑	0.0397	0.0357	3.8753	1.9282
B to Z ↓	0.0498	0.0427	2.4212	1.2210
B to Z ↑	0.0406	0.0370	3.8750	1.9276

C to Z ↓	0.0476	0.0417	2.4232	1.2218
C to Z ↑	0.0335	0.0304	3.8650	1.9218
D to Z ↓	0.0456	0.0395	2.4168	1.2189
D to Z ↑	0.0358	0.0321	3.8630	1.9205
	X33_P10		**X33_P10**	
A to Z ↓	0.0434		0.6263	
A to Z ↑	0.0326		0.9729	
B to Z ↓	0.0410		0.6255	
B to Z ↑	0.0345		0.9728	
C to Z ↓	0.0392		0.6249	
C to Z ↑	0.0281		0.9691	
D to Z ↓	0.0369		0.6242	
D to Z ↑	0.0296		0.9684	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.205e-05	1.000e-20
X17_P10	2.530e-05	1.000e-20
X33_P10	4.835e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.476e-05	3.505e-05	4.892e-05
B (output stable)	1.045e-04	1.232e-04	6.976e-05
C (output stable)	2.938e-05	5.149e-05	1.160e-04
D (output stable)	3.428e-05	6.201e-05	1.422e-04
A to Z	2.752e-03	4.618e-03	8.511e-03
B to Z	2.539e-03	4.315e-03	8.092e-03
C to Z	2.321e-03	3.938e-03	7.159e-03
D to Z	2.231e-03	3.751e-03	6.779e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

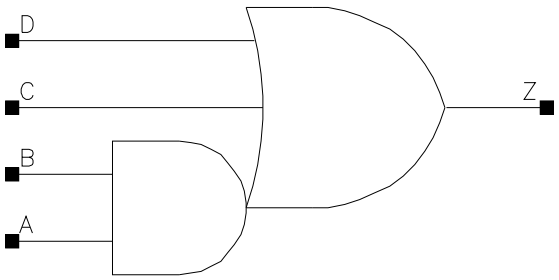
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	0.952	1.1424
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0010	0.0018
B	0.0006	0.0009	0.0018
C	0.0007	0.0010	0.0019
D	0.0006	0.0010	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0605	0.0517	2.6417	1.2980
A to Z ↑	0.0335	0.0299	3.9303	1.9761
B to Z ↓	0.0580	0.0483	2.6349	1.2939
B to Z ↑	0.0356	0.0313	3.9302	1.9766
C to Z ↓	0.0643	0.0547	2.6298	1.2924
C to Z ↑	0.0304	0.0280	3.9027	1.9653

D to Z ↓	0.0631	0.0543	2.6307	1.2929
D to Z ↑	0.0300	0.0277	3.8974	1.9658
	X33_P10		**X33_P10**	
A to Z ↓	0.0522		0.6498	
A to Z ↑	0.0297		0.9681	
B to Z ↓	0.0467		0.6456	
B to Z ↑	0.0303		0.9688	
C to Z ↓	0.0560		0.6462	
C to Z ↑	0.0272		0.9651	
D to Z ↓	0.0540		0.6464	
D to Z ↑	0.0263		0.9631	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	9.160e-06	1.000e-20
X17_P10	1.943e-05	1.000e-20
X33_P10	3.927e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	2.411e-05	5.458e-05	1.272e-04
B (output stable)	2.497e-05	5.493e-05	1.502e-04
C (output stable)	2.174e-05	4.087e-05	1.211e-04
D (output stable)	2.472e-05	4.927e-05	1.820e-04
A to Z	2.324e-03	3.910e-03	7.806e-03
B to Z	2.236e-03	3.704e-03	7.135e-03
C to Z	2.639e-03	4.463e-03	9.052e-03
D to Z	2.497e-03	4.218e-03	8.331e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

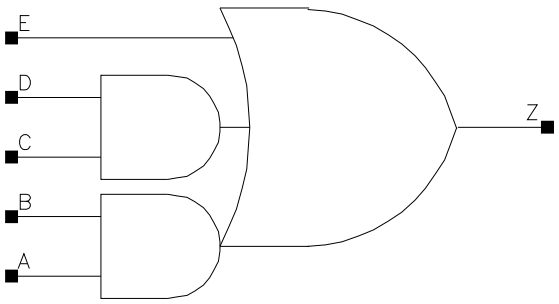
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.088	1.3056
X17_P10	1.200	1.224	1.4688
X33_P10	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0010	0.0019
B	0.0006	0.0009	0.0017
C	0.0007	0.0012	0.0019
D	0.0006	0.0009	0.0018
E	0.0006	0.0010	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0752	0.0626	2.5179	1.2598
A to Z ↑	0.0418	0.0359	3.8589	1.9360

B to Z ↓	0.0728	0.0596	2.5091	1.2569
B to Z ↑	0.0446	0.0379	3.8584	1.9363
C to Z ↓	0.0629	0.0537	2.5066	1.2565
C to Z ↑	0.0355	0.0303	3.8253	1.9231
D to Z ↓	0.0588	0.0493	2.4957	1.2507
D to Z ↑	0.0375	0.0319	3.8244	1.9231
E to Z ↓	0.0659	0.0550	2.4937	1.2511
E to Z ↑	0.0318	0.0278	3.7959	1.9109
	X33_P10		**X33_P10**	
A to Z ↓	0.0614		0.6490	
A to Z ↑	0.0368		0.9771	
B to Z ↓	0.0576		0.6473	
B to Z ↑	0.0384		0.9764	
C to Z ↓	0.0516		0.6468	
C to Z ↑	0.0301		0.9689	
D to Z ↓	0.0473		0.6441	
D to Z ↑	0.0314		0.9689	
E to Z ↓	0.0534		0.6442	
E to Z ↑	0.0275		0.9631	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.129e-05	1.000e-20
X17_P10	2.342e-05	1.000e-20
X33_P10	4.401e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.361e-05	2.209e-05	5.036e-05
B (output stable)	1.805e-05	2.566e-05	6.549e-05
C (output stable)	3.646e-05	6.234e-05	1.510e-04
D (output stable)	4.207e-05	7.487e-05	1.709e-04
E (output stable)	8.132e-05	1.149e-04	2.692e-04
A to Z	3.197e-03	5.151e-03	1.006e-02
B to Z	3.108e-03	4.937e-03	9.513e-03
C to Z	2.527e-03	4.138e-03	7.899e-03
D to Z	2.416e-03	3.912e-03	7.382e-03
E to Z	2.751e-03	4.444e-03	8.506e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

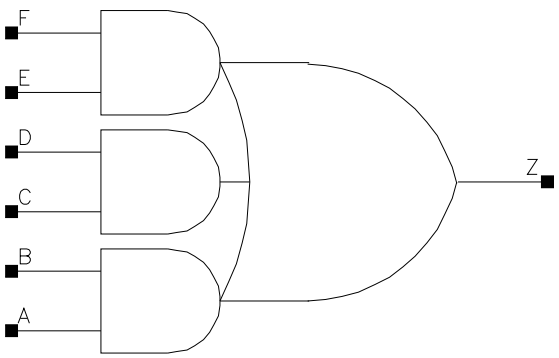
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.360	1.6320
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
A	0.0006	0.0007	0.0009	0.0019

B	0.0006	0.0007	0.0013	0.0017
C	0.0006	0.0007	0.0009	0.0019
D	0.0006	0.0007	0.0009	0.0017
E	0.0006	0.0007	0.0009	0.0019
F	0.0006	0.0007	0.0010	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0753	0.0708	4.9024	2.5119
A to Z ↑	0.0447	0.0426	7.7273	3.9132
B to Z ↓	0.0693	0.0656	4.8672	2.4947
B to Z ↑	0.0452	0.0434	7.7271	3.9110
C to Z ↓	0.0678	0.0644	4.8816	2.5025
C to Z ↑	0.0403	0.0383	7.6790	3.8910
D to Z ↓	0.0650	0.0617	4.8664	2.4943
D to Z ↑	0.0427	0.0407	7.6783	3.8893
E to Z ↓	0.0560	0.0546	4.8603	2.4930
E to Z ↑	0.0341	0.0327	7.6348	3.8716
F to Z ↓	0.0524	0.0512	4.8456	2.4846
F to Z ↑	0.0359	0.0345	7.6387	3.8714
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
A to Z ↓	0.0670	0.0639	1.2661	0.6475
A to Z ↑	0.0396	0.0393	1.9432	0.9804
B to Z ↓	0.0632	0.0604	1.2578	0.6457
B to Z ↑	0.0413	0.0410	1.9428	0.9802
C to Z ↓	0.0618	0.0591	1.2623	0.6468
C to Z ↑	0.0358	0.0364	1.9326	0.9744
D to Z ↓	0.0586	0.0557	1.2576	0.6451
D to Z ↑	0.0379	0.0380	1.9321	0.9741
E to Z ↓	0.0522	0.0523	1.2570	0.6450
E to Z ↑	0.0303	0.0314	1.9246	0.9706
F to Z ↓	0.0490	0.0486	1.2529	0.6424
F to Z ↑	0.0321	0.0331	1.9231	0.9713

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	8.749e-06	1.000e-20
X8_P10	1.506e-05	1.000e-20
X17_P10	2.702e-05	1.000e-20
X33_P10	5.027e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	2.576e-05	3.006e-05	3.840e-05	7.140e-05
B (output stable)	8.102e-05	8.808e-05	8.543e-05	9.944e-05
C (output stable)	2.716e-05	3.433e-05	4.386e-05	1.006e-04
D (output stable)	3.181e-05	4.044e-05	5.114e-05	1.362e-04
E (output stable)	5.856e-05	7.622e-05	1.089e-04	1.843e-04
F (output stable)	6.155e-05	7.902e-05	1.166e-04	2.122e-04

A to Z	2.829e-03	3.792e-03	5.777e-03	1.089e-02
B to Z	2.597e-03	3.519e-03	5.410e-03	1.034e-02
C to Z	2.388e-03	3.264e-03	5.070e-03	9.566e-03
D to Z	2.293e-03	3.139e-03	4.862e-03	9.061e-03
E to Z	1.916e-03	2.728e-03	4.268e-03	8.326e-03
F to Z	1.818e-03	2.597e-03	4.067e-03	7.851e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

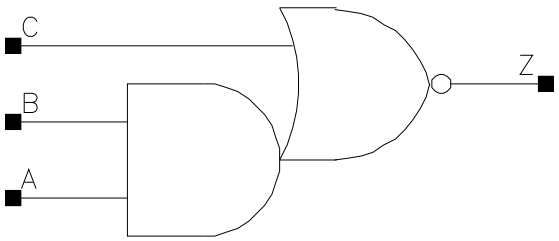
Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008
X44_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X33_P10	X44_P10
A	0.0008	0.0023	0.0046	0.0062
B	0.0007	0.0021	0.0042	0.0057
C	0.0008	0.0024	0.0048	0.0063

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0118	0.0123	4.4752	1.5135
A to Z ↑	0.0200	0.0203	7.3655	2.4461
B to Z ↓	0.0121	0.0122	4.5032	1.5263
B to Z ↑	0.0165	0.0161	7.2852	2.4472
C to Z ↓	0.0122	0.0123	2.5015	0.8524
C to Z ↑	0.0211	0.0207	6.7294	2.2501
	X33_P10	**X44_P10**	**X33_P10**	**X44_P10**
A to Z ↓	0.0126	0.0125	0.7662	0.5808

A to Z ↑	0.0203	0.0203	1.2244	0.9267
B to Z ↓	0.0121	0.0120	0.7735	0.5865
B to Z ↑	0.0161	0.0159	1.2230	0.9237
C to Z ↓	0.0138	0.0139	0.5082	0.3959
C to Z ↑	0.0210	0.0207	1.1248	0.8502

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P10	8.866e-06	1.000e-20
X17_P10	2.554e-05	1.000e-20
X33_P10	4.900e-05	1.000e-20
X44_P10	6.469e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	5.023e-05	1.504e-04	3.196e-04	4.162e-04
B (output stable)	5.665e-05	1.974e-04	4.223e-04	5.446e-04
C (output stable)	7.116e-05	2.137e-04	4.600e-04	6.053e-04
A to Z	9.458e-04	2.982e-03	6.010e-03	7.893e-03
B to Z	7.726e-04	2.231e-03	4.487e-03	5.853e-03
C to Z	1.337e-03	3.928e-03	7.916e-03	1.040e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

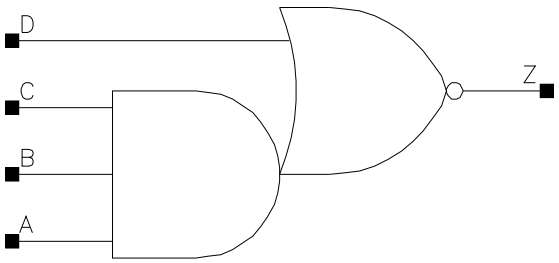
Pin Cycle (vdds)	X6_P10	X17_P10	X33_P10	X44_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X29_P10	1.200	3.536	4.2432
X38_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X29_P10	X38_P10
A	0.0008	0.0047	0.0061
B	0.0008	0.0045	0.0058
C	0.0007	0.0042	0.0055
D	0.0008	0.0048	0.0060

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X29_P10	X5_P10	X29_P10
A to Z ↓	0.0177	0.0190	6.4724	1.1067
A to Z ↑	0.0258	0.0257	7.3652	1.2154
B to Z ↓	0.0179	0.0182	6.4818	1.1100
B to Z ↑	0.0231	0.0227	7.3608	1.2215
C to Z ↓	0.0175	0.0169	6.4977	1.1143
C to Z ↑	0.0199	0.0188	7.2895	1.2283
D to Z ↓	0.0146	0.0165	2.5442	0.5122

D to Z ↑	0.0245	0.0248	6.2734	1.0442
	X38_P10		**X38_P10**	
A to Z ↓	0.0181		0.8517	
A to Z ↑	0.0247		0.9153	
B to Z ↓	0.0177		0.8542	
B to Z ↑	0.0219		0.9217	
C to Z ↓	0.0163		0.8576	
C to Z ↑	0.0179		0.9296	
D to Z ↓	0.0171		0.4276	
D to Z ↑	0.0237		0.7874	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	8.743e-06	1.000e-20
X29_P10	4.793e-05	1.000e-20
X38_P10	6.205e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X29_P10	X38_P10
A (output stable)	2.695e-05	2.201e-04	2.747e-04
B (output stable)	3.050e-05	2.759e-04	3.431e-04
C (output stable)	5.195e-05	5.564e-04	7.013e-04
D (output stable)	8.934e-05	6.786e-04	8.483e-04
A to Z	1.399e-03	8.840e-03	1.097e-02
B to Z	1.212e-03	7.228e-03	9.026e-03
C to Z	1.032e-03	5.666e-03	6.949e-03
D to Z	1.739e-03	1.061e-02	1.321e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

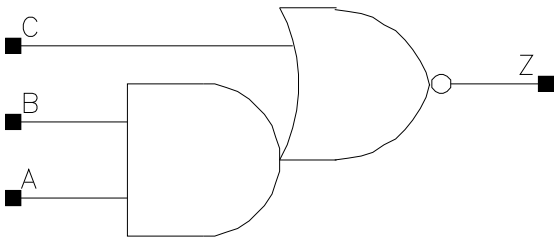
Pin Cycle (vdds)	X5_P10	X29_P10	X38_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X11_P10	1.200	1.088	1.3056
X16_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P10	X11_P10	X16_P10	X23_P10
A	0.0009	0.0017	0.0025	0.0034
B	0.0009	0.0016	0.0024	0.0031
C	0.0008	0.0015	0.0021	0.0030
	X46_P10			
A	0.0064			
B	0.0060			
C	0.0060			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X11_P10	X6_P10	X11_P10
A to Z ↓	0.0142	0.0154	4.3603	2.1959
A to Z ↑	0.0230	0.0241	7.3486	3.5888
B to Z ↓	0.0151	0.0152	4.3851	2.2109

B to Z ↑	0.0201	0.0205	7.2809	3.5973
C to Z ↓	0.0088	0.0093	2.5604	1.5125
C to Z ↑	0.0164	0.0159	6.7723	3.3245
	X16_P10	**X23_P10**	**X16_P10**	**X23_P10**
A to Z ↓	0.0146	0.0149	1.5118	1.1350
A to Z ↑	0.0224	0.0228	2.4092	1.8210
B to Z ↓	0.0150	0.0149	1.5238	1.1435
B to Z ↑	0.0188	0.0189	2.4090	1.8263
C to Z ↓	0.0094	0.0082	1.0560	0.6523
C to Z ↑	0.0151	0.0157	2.2315	1.6878
	X46_P10		**X46_P10**	
A to Z ↓	0.0144		0.5808	
A to Z ↑	0.0218		0.9370	
B to Z ↓	0.0145		0.5851	
B to Z ↑	0.0179		0.9356	
C to Z ↓	0.0083		0.3341	
C to Z ↑	0.0153		0.8664	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P10	8.876e-06	1.000e-20
X11_P10	1.777e-05	1.000e-20
X16_P10	2.482e-05	1.000e-20
X23_P10	3.499e-05	1.000e-20
X46_P10	6.775e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	1.849e-05	5.246e-05	6.496e-05	9.442e-05
B (output stable)	2.507e-05	1.010e-04	1.060e-04	1.635e-04
C (output stable)	2.148e-04	5.481e-04	6.090e-04	8.312e-04
A to Z	1.368e-03	3.007e-03	4.053e-03	5.523e-03
B to Z	1.177e-03	2.451e-03	3.269e-03	4.395e-03
C to Z	7.737e-04	1.565e-03	2.139e-03	3.007e-03
	X46_P10			
A (output stable)	1.724e-04			
B (output stable)	2.818e-04			
C (output stable)	1.418e-03			
A to Z	1.020e-02			
B to Z	8.090e-03			
C to Z	5.572e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X6_P10	X11_P10	X16_P10	X23_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

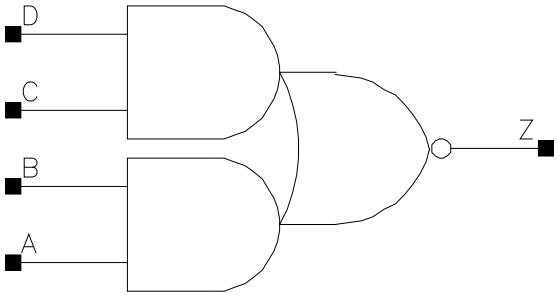
	X46_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P10	X10_P10	X16_P10	X21_P10
A	0.0007	0.0018	0.0025	0.0033
B	0.0007	0.0015	0.0023	0.0031
C	0.0006	0.0016	0.0023	0.0031
D	0.0007	0.0014	0.0022	0.0029
	X42_P10			
A	0.0066			
B	0.0061			
C	0.0061			
D	0.0057			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X10_P10**	**X4_P10**	**X10_P10**
A to Z ↓	0.0160	0.0158	5.4507	2.1317
A to Z ↑	0.0303	0.0252	10.1726	3.3059
B to Z ↓	0.0172	0.0172	5.4799	2.1451
B to Z ↑	0.0271	0.0228	10.1501	3.3671
C to Z ↓	0.0120	0.0115	5.5375	2.1383
C to Z ↑	0.0234	0.0200	10.1789	3.3245
D to Z ↓	0.0127	0.0121	5.5794	2.1575
D to Z ↑	0.0201	0.0172	10.1583	3.3623
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0171	0.0170	1.5189	1.1388
A to Z ↑	0.0262	0.0257	2.2241	1.7072
B to Z ↓	0.0178	0.0172	1.5284	1.1463
B to Z ↑	0.0228	0.0223	2.2247	1.7097
C to Z ↓	0.0124	0.0127	1.5160	1.1378
C to Z ↑	0.0205	0.0211	2.2275	1.7083
D to Z ↓	0.0124	0.0121	1.5305	1.1493
D to Z ↑	0.0169	0.0171	2.2307	1.7111
	X42_P10		**X42_P10**	
A to Z ↓	0.0176		0.5878	
A to Z ↑	0.0261		0.8556	
B to Z ↓	0.0177		0.5916	
B to Z ↑	0.0224		0.8533	
C to Z ↓	0.0131		0.5835	
C to Z ↑	0.0211		0.8577	
D to Z ↓	0.0126		0.5888	
D to Z ↑	0.0172		0.8561	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	7.039e-06	1.000e-20
X10_P10	2.195e-05	1.000e-20
X16_P10	3.079e-05	1.000e-20
X21_P10	4.143e-05	1.000e-20
X42_P10	8.090e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	2.061e-05	4.763e-05	9.489e-05	1.288e-04
B (output stable)	2.852e-05	7.020e-05	1.794e-04	2.655e-04
C (output stable)	4.692e-05	1.191e-04	2.060e-04	2.601e-04
D (output stable)	5.655e-05	1.456e-04	2.878e-04	3.960e-04
A to Z	1.394e-03	3.391e-03	5.329e-03	6.844e-03
B to Z	1.227e-03	2.986e-03	4.507e-03	5.756e-03
C to Z	8.299e-04	2.086e-03	3.247e-03	4.432e-03
D to Z	6.884e-04	1.730e-03	2.491e-03	3.359e-03
	X42_P10			
A (output stable)	2.490e-04			
B (output stable)	4.687e-04			
C (output stable)	5.010e-04			
D (output stable)	7.257e-04			

A to Z	1.354e-02			
B to Z	1.137e-02			
C to Z	8.615e-03			
D to Z	6.633e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

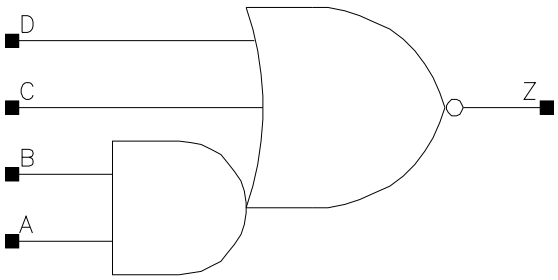
Pin Cycle (vdds)	X4_P10	X10_P10	X16_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X35_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P10	X35_P10
A	0.0008	0.0059
B	0.0008	0.0054
C	0.0008	0.0058
D	0.0008	0.0054

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X35_P10	X5_P10	X35_P10
A to Z ↓	0.0139	0.0144	4.5204	0.6584
A to Z ↑	0.0267	0.0248	10.7262	1.3572
B to Z ↓	0.0145	0.0143	4.5517	0.6643
B to Z ↑	0.0225	0.0200	10.6728	1.3566
C to Z ↓	0.0147	0.0188	2.6351	0.5085
C to Z ↑	0.0310	0.0302	10.1272	1.2818
D to Z ↓	0.0142	0.0174	2.6572	0.5077

D to Z ↑	0.0300	0.0279	10.1335	1.2843

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	7.405e-06	1.000e-20
X35_P10	5.253e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X35_P10
A (output stable)	5.207e-05	4.387e-04
B (output stable)	5.424e-05	4.831e-04
C (output stable)	3.953e-05	4.457e-04
D (output stable)	4.745e-05	5.541e-04
A to Z	1.150e-03	8.302e-03
B to Z	9.686e-04	6.474e-03
C to Z	1.796e-03	1.381e-02
D to Z	1.538e-03	1.108e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

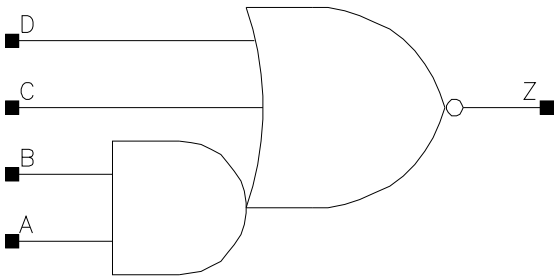
Pin Cycle (vdds)	X5_P10	X35_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.680	0.8160
X17_P10	1.200	2.448	2.9376
X34_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P10	X17_P10	X34_P10
A	0.0008	0.0033	0.0066
B	0.0008	0.0031	0.0062
C	0.0007	0.0028	0.0055
D	0.0007	0.0025	0.0050

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X17_P10	X4_P10	X17_P10
A to Z ↓	0.0166	0.0180	4.9361	1.2906
A to Z ↑	0.0308	0.0324	10.7722	2.6475
B to Z ↓	0.0180	0.0184	4.9658	1.2980
B to Z ↑	0.0273	0.0276	10.6941	2.6507
C to Z ↓	0.0153	0.0151	4.2905	1.0459
C to Z ↑	0.0222	0.0238	10.1740	2.5097

D to Z ↓	0.0129	0.0117	4.3846	1.0504
D to Z ↑	0.0199	0.0182	10.2022	2.5177
	X34_P10		**X34_P10**	
A to Z ↓	0.0178		0.6590	
A to Z ↑	0.0317		1.3436	
B to Z ↓	0.0184		0.6630	
B to Z ↑	0.0271		1.3402	
C to Z ↓	0.0155		0.5510	
C to Z ↑	0.0230		1.2715	
D to Z ↓	0.0120		0.5547	
D to Z ↑	0.0178		1.2758	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	6.685e-06	1.000e-20
X17_P10	2.665e-05	1.000e-20
X34_P10	5.213e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X17_P10	X34_P10
A (output stable)	1.744e-05	8.502e-05	1.689e-04
B (output stable)	1.965e-05	1.199e-04	2.234e-04
C (output stable)	5.580e-05	2.974e-04	5.744e-04
D (output stable)	1.041e-04	6.570e-04	1.229e-03
A to Z	1.674e-03	7.269e-03	1.403e-02
B to Z	1.494e-03	6.156e-03	1.193e-02
C to Z	1.033e-03	4.532e-03	8.604e-03
D to Z	7.711e-04	2.927e-03	5.569e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

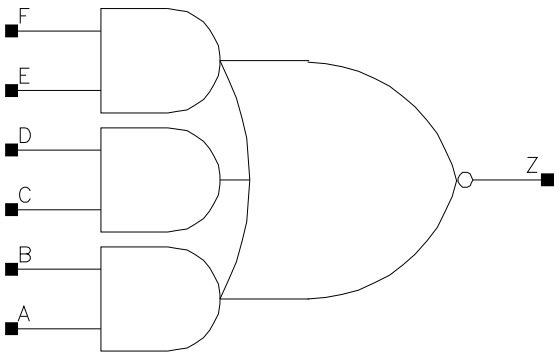
Pin Cycle (vdds)	X4_P10	X17_P10	X34_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.088	1.3056
X8_P10	1.200	2.176	2.6112
X13_P10	1.200	2.720	3.2640
X17_P10	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P10	X8_P10	X13_P10	X17_P10
A	0.0008	0.0016	0.0025	0.0033

B	0.0008	0.0015	0.0023	0.0030
C	0.0008	0.0016	0.0024	0.0030
D	0.0008	0.0015	0.0022	0.0028
E	0.0010	0.0015	0.0022	0.0029
F	0.0008	0.0014	0.0020	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0196	0.0235	4.3644	2.5135
A to Z ↑	0.0445	0.0435	10.3450	4.7588
B to Z ↓	0.0215	0.0244	4.3851	2.5227
B to Z ↑	0.0409	0.0394	10.3439	4.7676
C to Z ↓	0.0178	0.0212	4.3266	2.5171
C to Z ↑	0.0386	0.0388	10.3910	4.7747
D to Z ↓	0.0193	0.0221	4.3548	2.5306
D to Z ↑	0.0349	0.0346	10.3548	4.7736
E to Z ↓	0.0135	0.0162	4.2498	2.5172
E to Z ↑	0.0294	0.0293	10.3262	4.7564
F to Z ↓	0.0143	0.0163	4.2907	2.5389
F to Z ↑	0.0256	0.0248	10.3827	4.7605
	X13_P10	**X17_P10**	**X13_P10**	**X17_P10**
A to Z ↓	0.0224	0.0226	1.7046	1.2967
A to Z ↑	0.0403	0.0404	3.1508	2.4004
B to Z ↓	0.0237	0.0234	1.7105	1.3018
B to Z ↑	0.0366	0.0362	3.1597	2.4018
C to Z ↓	0.0203	0.0202	1.7157	1.2854
C to Z ↑	0.0356	0.0359	3.1647	2.4136
D to Z ↓	0.0215	0.0208	1.7245	1.2921
D to Z ↑	0.0320	0.0317	3.1683	2.4104
E to Z ↓	0.0154	0.0153	1.7112	1.2862
E to Z ↑	0.0272	0.0273	3.1574	2.4004
F to Z ↓	0.0159	0.0150	1.7243	1.2971
F to Z ↑	0.0233	0.0229	3.1622	2.4085

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	1.198e-05	1.000e-20
X8_P10	2.446e-05	1.000e-20
X13_P10	3.446e-05	1.000e-20
X17_P10	4.604e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

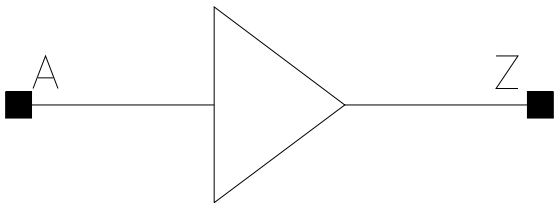
Pin Cycle (vdd)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	3.293e-05	7.777e-05	1.081e-04	1.457e-04
B (output stable)	3.811e-05	1.351e-04	1.511e-04	2.365e-04
C (output stable)	5.244e-05	1.150e-04	1.510e-04	2.039e-04
D (output stable)	5.937e-05	1.810e-04	1.987e-04	2.944e-04
E (output stable)	8.846e-05	2.181e-04	2.952e-04	4.043e-04
F (output stable)	1.015e-04	2.788e-04	3.455e-04	4.949e-04

A to Z	2.666e-03	5.618e-03	7.732e-03	1.026e-02
B to Z	2.454e-03	5.072e-03	7.007e-03	9.147e-03
C to Z	2.005e-03	4.416e-03	5.921e-03	7.885e-03
D to Z	1.817e-03	3.903e-03	5.271e-03	6.885e-03
E to Z	1.318e-03	2.999e-03	3.967e-03	5.281e-03
F to Z	1.141e-03	2.480e-03	3.318e-03	4.296e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X4_P10	X8_P10	X13_P10	X17_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.408	0.4896
X6_P10	1.200	0.408	0.4896
X8_P10	1.200	0.408	0.4896
X13_P10	1.200	0.544	0.6528
X16_P10	1.200	0.544	0.6528
X21_P10	1.200	0.680	0.8160
X25_P10	1.200	0.680	0.8160
X29_P10	1.200	0.952	1.1424
X33_P10	1.200	0.952	1.1424
X42_P10	1.200	1.088	1.3056
X50_P10	1.200	1.224	1.4688
X58_P10	1.200	1.496	1.7952
X67_P10	1.200	1.632	1.9584
X75_P10	1.200	1.768	2.1216
X84_P10	1.200	1.904	2.2848
X100_P10	1.200	2.312	2.7744
X134_P10	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0008	0.0008	0.0008	0.0008
	X16_P10	X21_P10	X25_P10	X29_P10
A	0.0008	0.0011	0.0011	0.0015
	X33_P10	X42_P10	X50_P10	X58_P10
A	0.0015	0.0017	0.0021	0.0030

	X67_P10	X75_P10	X84_P10	X100_P10
A	0.0030	0.0030	0.0030	0.0039
	X134_P10			
A	0.0049			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0291	0.0293	4.6113	3.3096
A to Z ↑	0.0234	0.0232	7.5656	5.5205
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0306	0.0345	2.4310	1.5827
A to Z ↑	0.0240	0.0269	3.9185	2.5739
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0373	0.0306	1.2471	0.9683
A to Z ↑	0.0284	0.0246	1.9646	1.5388
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0320	0.0307	0.8249	0.7005
A to Z ↑	0.0254	0.0234	1.2864	1.1000
	X33_P10	**X42_P10**	**X33_P10**	**X42_P10**
A to Z ↓	0.0321	0.0312	0.6196	0.5019
A to Z ↑	0.0243	0.0247	0.9630	0.7735
	X50_P10	**X58_P10**	**X50_P10**	**X58_P10**
A to Z ↓	0.0304	0.0280	0.4174	0.3596
A to Z ↑	0.0241	0.0226	0.6427	0.5521
	X67_P10	**X75_P10**	**X67_P10**	**X75_P10**
A to Z ↓	0.0295	0.0312	0.3158	0.2844
A to Z ↑	0.0236	0.0249	0.4841	0.4326
	X84_P10	**X100_P10**	**X84_P10**	**X100_P10**
A to Z ↓	0.0324	0.0309	0.2571	0.2161
A to Z ↑	0.0258	0.0248	0.3904	0.3268
	X134_P10		**X134_P10**	
A to Z ↓	0.0318		0.1668	
A to Z ↑	0.0256		0.2487	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	6.096e-06	1.000e-20
X6_P10	7.770e-06	1.000e-20
X8_P10	1.013e-05	1.000e-20
X13_P10	1.282e-05	1.000e-20
X16_P10	1.673e-05	1.000e-20
X21_P10	2.313e-05	1.000e-20
X25_P10	2.681e-05	1.000e-20
X29_P10	2.993e-05	1.000e-20
X33_P10	3.336e-05	1.000e-20
X42_P10	4.213e-05	1.000e-20
X50_P10	5.123e-05	1.000e-20
X58_P10	6.345e-05	1.000e-20
X67_P10	6.956e-05	1.000e-20
X75_P10	7.567e-05	1.000e-20

X84_P10	8.179e-05	1.000e-20
X100_P10	1.001e-04	1.000e-20
X134_P10	1.307e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	1.355e-03	1.522e-03	1.817e-03	2.430e-03
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	2.974e-03	3.959e-03	4.447e-03	4.964e-03
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	5.517e-03	6.934e-03	8.124e-03	9.785e-03
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	1.093e-02	1.232e-02	1.350e-02	1.646e-02
	X134_P10			
A to Z	2.174e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

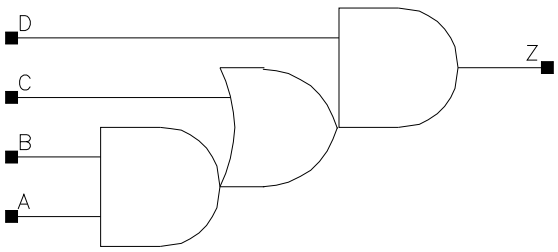
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P10	X21_P10	X25_P10	X29_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P10	X42_P10	X50_P10	X58_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P10	X75_P10	X84_P10	X100_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P10			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.632	1.9584
X25_P10	1.200	1.768	2.1216
X33_P10	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0010	0.0021	0.0020	0.0020
B	0.0010	0.0019	0.0018	0.0018
C	0.0011	0.0023	0.0023	0.0023
D	0.0015	0.0020	0.0020	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0396	0.0374	2.4781	1.2280
A to Z ↑	0.0370	0.0348	3.9696	1.9329
B to Z ↓	0.0367	0.0339	2.4718	1.2256
B to Z ↑	0.0373	0.0343	3.9775	1.9332
C to Z ↓	0.0332	0.0304	2.4692	1.2240
C to Z ↑	0.0275	0.0248	3.9353	1.9137

D to Z ↓	0.0328	0.0286	2.4494	1.2156
D to Z ↑	0.0323	0.0278	3.9437	1.9166
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0412	0.0435	0.8350	0.6294
A to Z ↑	0.0384	0.0402	1.3048	0.9816
B to Z ↓	0.0378	0.0408	0.8326	0.6293
B to Z ↑	0.0379	0.0405	1.3048	0.9809
C to Z ↓	0.0343	0.0372	0.8314	0.6270
C to Z ↑	0.0278	0.0297	1.2909	0.9697
D to Z ↓	0.0312	0.0328	0.8231	0.6190
D to Z ↑	0.0307	0.0323	1.2933	0.9711

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.644e-05	1.000e-20
X17_P10	3.204e-05	1.000e-20
X25_P10	3.870e-05	1.000e-20
X33_P10	4.537e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	5.272e-05	1.098e-04	1.112e-04	9.673e-05
B (output stable)	7.575e-05	1.633e-04	1.654e-04	1.400e-04
C (output stable)	2.351e-04	3.759e-04	3.804e-04	3.600e-04
D (output stable)	8.426e-05	1.219e-04	1.233e-04	1.212e-04
A to Z	3.057e-03	5.601e-03	7.081e-03	8.282e-03
B to Z	2.846e-03	5.054e-03	6.519e-03	7.825e-03
C to Z	2.394e-03	4.123e-03	5.533e-03	6.720e-03
D to Z	3.118e-03	5.371e-03	6.749e-03	7.831e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

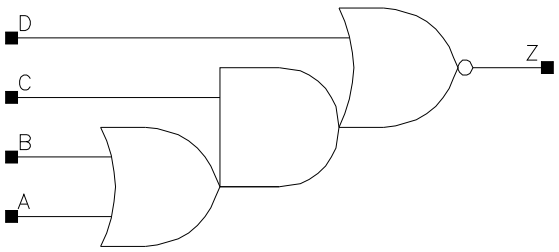
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.952	1.1424
X11_P10	1.200	1.496	1.7952
X16_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X16_P10	X21_P10
A	0.0009	0.0017	0.0025	0.0033
B	0.0009	0.0016	0.0025	0.0032
C	0.0008	0.0016	0.0024	0.0032
D	0.0011	0.0016	0.0023	0.0030

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0177	0.0168	4.2537	2.2260
A to Z ↑	0.0374	0.0343	10.5330	5.4446
B to Z ↓	0.0169	0.0163	4.1733	2.1977
B to Z ↑	0.0350	0.0327	10.5438	5.4474
C to Z ↓	0.0159	0.0151	3.9185	2.0546
C to Z ↑	0.0229	0.0210	7.1991	3.6765

D to Z ↓	0.0099	0.0084	2.4527	1.2449
D to Z ↑	0.0202	0.0175	7.6740	3.9271
	X16_P10	**X21_P10**	**X16_P10**	**X21_P10**
A to Z ↓	0.0166	0.0170	1.5093	1.1535
A to Z ↑	0.0318	0.0336	3.5238	2.7038
B to Z ↓	0.0158	0.0162	1.5145	1.1538
B to Z ↑	0.0312	0.0319	3.5252	2.7054
C to Z ↓	0.0152	0.0152	1.4116	1.0740
C to Z ↑	0.0202	0.0204	2.4363	1.8279
D to Z ↓	0.0083	0.0083	0.8673	0.6603
D to Z ↑	0.0163	0.0162	2.5851	1.9521

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	1.006e-05	1.000e-20
X11_P10	1.908e-05	1.000e-20
X16_P10	2.654e-05	1.000e-20
X21_P10	3.542e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	2.074e-05	3.766e-05	4.855e-05	8.004e-05
B (output stable)	2.528e-05	4.179e-05	5.452e-05	9.644e-05
C (output stable)	6.526e-05	1.312e-04	1.779e-04	2.467e-04
D (output stable)	2.581e-04	5.441e-04	7.816e-04	1.095e-03
A to Z	2.165e-03	3.775e-03	5.264e-03	7.392e-03
B to Z	1.772e-03	3.134e-03	4.500e-03	6.087e-03
C to Z	1.498e-03	2.587e-03	3.679e-03	5.033e-03
D to Z	9.470e-04	1.613e-03	2.194e-03	2.923e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

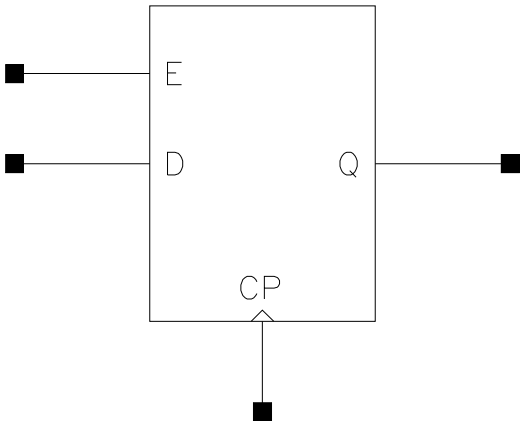
Pin Cycle (vdds)	X5_P10	X11_P10	X16_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.128	3.7536
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0010	0.0011	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0477	0.0550	2.4565	1.2688
CP to Q ↑	0.0599	0.0640	3.9519	1.9821
	X33_P10		**X33_P10**	
CP to Q ↓	0.0837		0.6268	
CP to Q ↑	0.1032		0.9803	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0666	0.0666	0.0666
CP ↑	min_pulse_width to CP	0.0361	0.0456	0.0348
D ↓	hold_rising to CP	-0.0240	-0.0214	-0.0240
D ↑	hold_rising to CP	-0.0120	-0.0094	-0.0120
D ↓	setup_rising to CP	0.0668	0.0662	0.0662
D ↑	setup_rising to CP	0.0390	0.0390	0.0362
E ↓	hold_rising to CP	-0.0165	-0.0165	-0.0165
E ↑	hold_rising to CP	-0.0088	-0.0088	-0.0088
E ↓	setup_rising to CP	0.0706	0.0706	0.0706
E ↑	setup_rising to CP	0.0737	0.0737	0.0737

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	3.782e-05	1.000e-20
X17_P10	4.425e-05	1.000e-20
X33_P10	6.478e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

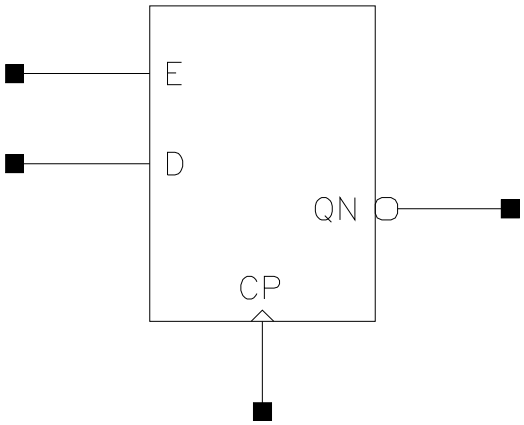
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	6.373e-03	6.375e-03	6.381e-03
Clock 100Mhz Data 25Mhz	8.433e-03	9.105e-03	1.129e-02
Clock 100Mhz Data 50Mhz	1.049e-02	1.183e-02	1.619e-02
Clock = 0 Data 100Mhz	4.112e-03	4.113e-03	4.113e-03
Clock = 1 Data 100Mhz	1.123e-03	1.123e-03	1.123e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.992	3.5904
X17_P10	1.200	3.264	3.9168
X33_P10	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0011	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0850	0.0796	2.5286	1.2130
CP to QN ↑	0.0645	0.0660	4.0074	1.9302
	X33_P10		**X33_P10**	
CP to QN ↓	0.0850		0.6292	
CP to QN ↑	0.0726		0.9821	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0666	0.0666	0.0666
CP ↑	min_pulse_width to CP	0.0348	0.0361	0.0407
D ↓	hold_rising to CP	-0.0240	-0.0240	-0.0214
D ↑	hold_rising to CP	-0.0120	-0.0120	-0.0094
D ↓	setup_rising to CP	0.0662	0.0662	0.0662
D ↑	setup_rising to CP	0.0390	0.0390	0.0390
E ↓	hold_rising to CP	-0.0165	-0.0165	-0.0165
E ↑	hold_rising to CP	-0.0088	-0.0088	-0.0088
E ↓	setup_rising to CP	0.0706	0.0706	0.0706
E ↑	setup_rising to CP	0.0737	0.0737	0.0737

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	3.746e-05	1.000e-20
X17_P10	4.843e-05	1.000e-20
X33_P10	6.315e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

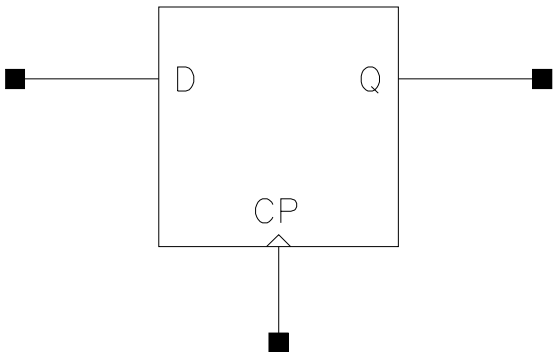
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	6.368e-03	6.370e-03	6.372e-03
Clock 100Mhz Data 25Mhz	8.465e-03	9.458e-03	1.116e-02
Clock 100Mhz Data 50Mhz	1.056e-02	1.255e-02	1.595e-02
Clock = 0 Data 100Mhz	4.114e-03	4.112e-03	4.112e-03
Clock = 1 Data 100Mhz	1.123e-03	1.123e-03	1.123e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.176	2.6112
X17_P10	1.200	2.448	2.9376
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0499	0.0550	2.4464	1.2586
CP to Q ↑	0.0609	0.0677	3.8557	1.9568
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to Q ↓	0.0700	0.0727	0.7486	0.6769
CP to Q ↑	0.0773	0.0786	1.1038	1.0020

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0583	0.0617	0.0617	0.0617
CP ↑	min_pulse_width to CP	0.0361	0.0455	0.0596	0.0596
D ↓	hold_rising to CP	0.0102	0.0075	0.0075	0.0075
D ↑	hold_rising to CP	0.0107	0.0107	0.0107	0.0107
D ↓	setup_rising to CP	0.0343	0.0375	0.0375	0.0375
D ↑	setup_rising to CP	0.0200	0.0200	0.0200	0.0200

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	2.982e-05	1.000e-20
X17_P10	3.688e-05	1.000e-20
X30_P10	4.674e-05	1.000e-20
X33_P10	4.925e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

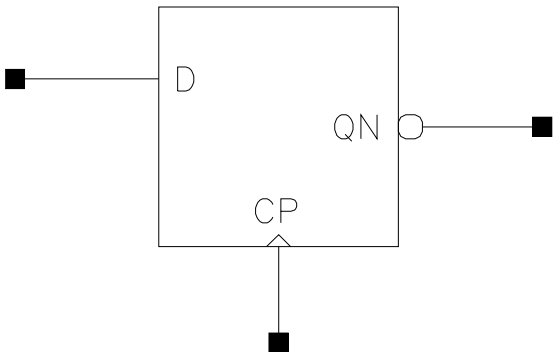
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	6.702e-03	6.744e-03	6.757e-03	6.763e-03
Clock 100Mhz Data 25Mhz	7.733e-03	8.693e-03	1.030e-02	1.068e-02
Clock 100Mhz Data 50Mhz	8.763e-03	1.064e-02	1.384e-02	1.459e-02
Clock = 0 Data 100Mhz	2.726e-03	2.811e-03	2.838e-03	2.851e-03
Clock = 1 Data 100Mhz	1.625e-05	1.626e-05	1.633e-05	1.636e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X30_P10	1.200	2.720	3.2640
X33_P10	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X30_P10	X33_P10
CP	0.0010	0.0010	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to QN ↓	0.0485	0.0573	2.5096	1.2959
CP to QN ↑	0.0521	0.0554	3.8497	1.9513
	X30_P10	**X33_P10**	**X30_P10**	**X33_P10**

CP to QN ↓	0.0853	0.0858	0.6944	0.6279
CP to QN ↑	0.0674	0.0781	1.0661	0.9814

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P10	X17_P10	X30_P10	X33_P10
CP ↓	min_pulse_width to CP	0.0509	0.0509	0.0617	0.0583
CP ↑	min_pulse_width to CP	0.0360	0.0455	0.0361	0.0454
D ↓	hold_rising to CP	0.0150	0.0173	0.0075	0.0102
D ↑	hold_rising to CP	0.0097	0.0097	0.0081	0.0107
D ↓	setup_rising to CP	0.0223	0.0219	0.0375	0.0343
D ↑	setup_rising to CP	0.0217	0.0217	0.0200	0.0200

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	2.786e-05	1.000e-20
X17_P10	3.438e-05	1.000e-20
X30_P10	5.197e-05	1.000e-20
X33_P10	5.523e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

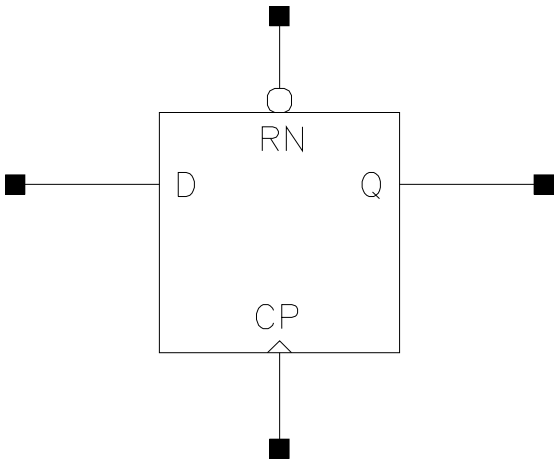
Pin Cycle	X8_P10	X17_P10	X30_P10	X33_P10
Clock 100Mhz Data 0Mhz	6.468e-03	6.470e-03	6.570e-03	6.611e-03
Clock 100Mhz Data 25Mhz	7.381e-03	8.113e-03	9.922e-03	1.046e-02
Clock 100Mhz Data 50Mhz	8.294e-03	9.755e-03	1.327e-02	1.431e-02
Clock = 0 Data 100Mhz	2.400e-03	2.401e-03	2.565e-03	2.605e-03
Clock = 1 Data 100Mhz	1.607e-05	1.606e-05	1.620e-05	1.629e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0009
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0574	0.0725	1.2699	0.7576
CP to Q ↑	0.0699	0.0791	1.9625	1.1072
RN to Q ↓	0.0970	0.1319	1.3399	0.7989

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0665	0.0665
CP ↑	min_pulse_width to CP	0.0455	0.0596
D ↓	hold_rising to CP	0.0075	0.0075
D ↑	hold_rising to CP	0.0049	0.0049
D ↓	setup_rising to CP	0.0392	0.0392
D ↑	setup_rising to CP	0.0249	0.0249
RN ↓	min_pulse_width to RN	0.1169	0.1511
RN ↑	recovery_rising to CP	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0054	-0.0054

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P10	4.052e-05	1.000e-20
X30_P10	5.094e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

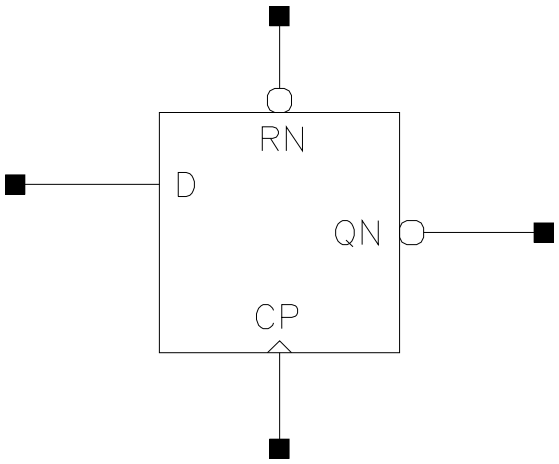
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	7.188e-03	7.186e-03
Clock 100Mhz Data 25Mhz	9.276e-03	1.088e-02
Clock 100Mhz Data 50Mhz	1.136e-02	1.457e-02
Clock = 0 Data 100Mhz	3.346e-03	3.349e-03
Clock = 1 Data 100Mhz	1.650e-05	1.658e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0010
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.0821	0.0890	1.2031	0.6962
CP to QN ↑	0.0657	0.0710	1.9171	1.0699
RN to QN ↑	0.0993	0.1063	1.9244	1.0736

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0665	0.0665
CP ↑	min_pulse_width to CP	0.0393	0.0407
D ↓	hold_rising to CP	0.0075	0.0075
D ↑	hold_rising to CP	0.0049	0.0049
D ↓	setup_rising to CP	0.0392	0.0392
D ↑	setup_rising to CP	0.0249	0.0249
RN ↓	min_pulse_width to RN	0.0947	0.0996
RN ↑	recovery_rising to CP	0.0200	0.0200
RN ↑	removal_rising to CP	-0.0054	-0.0054

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P10	4.546e-05	1.000e-20
X30_P10	5.456e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

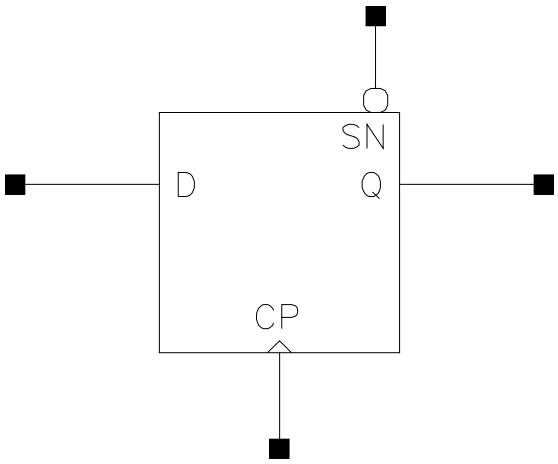
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	7.184e-03	7.183e-03
Clock 100Mhz Data 25Mhz	9.585e-03	1.074e-02
Clock 100Mhz Data 50Mhz	1.199e-02	1.430e-02
Clock = 0 Data 100Mhz	3.389e-03	3.376e-03
Clock = 1 Data 100Mhz	1.648e-05	1.656e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to Q ↓	0.0577	0.0727	1.2714	0.7532
CP to Q ↑	0.0693	0.0782	1.9609	1.1046
SN to Q ↑	0.0694	0.0812	1.9662	1.1080

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0712	0.0712
CP ↑	min_pulse_width to CP	0.0454	0.0595
D ↓	hold_rising to CP	0.0075	0.0075
D ↑	hold_rising to CP	0.0049	0.0049
D ↓	setup_rising to CP	0.0414	0.0418
D ↑	setup_rising to CP	0.0217	0.0222
SN ↓	min_pulse_width to SN	0.0674	0.0820
SN ↑	recovery_rising to CP	0.0103	0.0103
SN ↑	removal_rising to CP	0.0336	0.0335

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P10	3.957e-05	1.000e-20
X30_P10	4.873e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

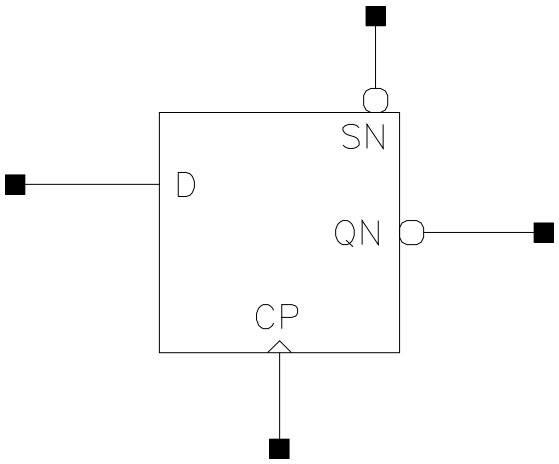
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	7.260e-03	7.245e-03
Clock 100Mhz Data 25Mhz	9.342e-03	1.087e-02
Clock 100Mhz Data 50Mhz	1.142e-02	1.450e-02
Clock = 0 Data 100Mhz	3.318e-03	3.318e-03
Clock = 1 Data 100Mhz	1.655e-05	1.658e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	3.128	3.7536
X30_P10	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P10	X30_P10
CP	0.0010	0.0010
D	0.0007	0.0007
SN	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P10	X30_P10	X17_P10	X30_P10
CP to QN ↓	0.0816	0.0884	1.2059	0.6979
CP to QN ↑	0.0662	0.0713	1.9146	1.0677
SN to QN ↓	0.0806	0.0878	1.2053	0.6980

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P10	X30_P10
CP ↓	min_pulse_width to CP	0.0712	0.0712
CP ↑	min_pulse_width to CP	0.0393	0.0407
D ↓	hold_rising to CP	0.0075	0.0075
D ↑	hold_rising to CP	0.0049	0.0049
D ↓	setup_rising to CP	0.0414	0.0440
D ↑	setup_rising to CP	0.0217	0.0217
SN ↓	min_pulse_width to SN	0.0571	0.0571
SN ↑	recovery_rising to CP	0.0103	0.0103
SN ↑	removal_rising to CP	0.0336	0.0336

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P10	4.537e-05	1.000e-20
X30_P10	5.564e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

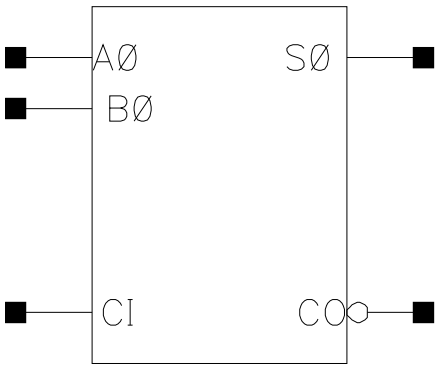
Pin Cycle	X17_P10	X30_P10
Clock 100Mhz Data 0Mhz	7.252e-03	7.247e-03
Clock 100Mhz Data 25Mhz	9.631e-03	1.078e-02
Clock 100Mhz Data 50Mhz	1.201e-02	1.431e-02
Clock = 0 Data 100Mhz	3.319e-03	3.319e-03
Clock = 1 Data 100Mhz	1.651e-05	1.660e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_-P10	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_-P10	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_-P10	1.200	3.672	4.4064
C12T28SOI_LLS1_-FA1X33_P10	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10
A0	0.0032	0.0066	0.0029	0.0057
B0	0.0029	0.0064	0.0032	0.0055
CI	0.0022	0.0050	0.0022	0.0039

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10
A0 to CO ↓	0.0529	0.0572	2.5523	0.6698
A0 to CO ↑	0.0400	0.0410	3.9766	1.0170
A0 to S0 ↓	0.0557	0.0698	2.5299	0.6559
A0 to S0 ↑	0.0572	0.0696	3.9343	1.0023
B0 to CO ↓	0.0520	0.0574	2.5599	0.6727
B0 to CO ↑	0.0409	0.0425	3.9790	1.0142
B0 to S0 ↓	0.0559	0.0708	2.5305	0.6559
B0 to S0 ↑	0.0573	0.0705	3.9375	1.0027
CI to CO ↓	0.0499	0.0556	2.5609	0.6714
CI to CO ↑	0.0402	0.0409	3.9766	1.0166
CI to S0 ↓	0.0551	0.0700	2.5295	0.6560
CI to S0 ↑	0.0570	0.0705	3.9361	1.0028
	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10
A0 to CO ↓	0.0341	0.0420	5.0983	0.8819
A0 to CO ↑	0.0296	0.0341	4.0011	1.0047
A0 to S0 ↓	0.0742	0.0914	2.7090	0.6803
A0 to S0 ↑	0.0680	0.0733	4.0960	1.0154
B0 to CO ↓	0.0349	0.0432	5.0994	0.8820
B0 to CO ↑	0.0277	0.0328	3.9972	1.0050
B0 to S0 ↓	0.0745	0.0934	2.7081	0.6805
B0 to S0 ↑	0.0683	0.0752	4.0977	1.0153
CI to CO ↓	0.0348	0.0611	5.0915	0.8931
CI to CO ↑	0.0309	0.0371	4.0777	1.0118
CI to S0 ↓	0.0417	0.0545	2.7103	0.6807
CI to S0 ↑	0.0360	0.0359	4.0935	1.0155

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_FA1X8_P10	3.603e-05	1.000e-20
C12T28SOI_LL_FA1X33_P10	9.620e-05	1.000e-20
C12T28SOI_LLS1_FA1X8_P10	7.837e-05	1.000e-20
C12T28SOI_LLS1_FA1X33_P10	1.619e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10
A0 to CO	3.188e-03	9.229e-03	4.823e-03	1.214e-02
A0 to S0	3.203e-03	9.590e-03	6.468e-03	1.506e-02
B0 to CO	3.235e-03	9.414e-03	4.850e-03	1.229e-02
B0 to S0	3.172e-03	9.579e-03	6.561e-03	1.537e-02
CI to CO	3.287e-03	9.557e-03	3.427e-03	1.098e-02
CI to S0	3.162e-03	9.565e-03	3.879e-03	1.176e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P10	C12T28SOI_LL_-FA1X33_P10	C12T28SOI_LLS1_-FA1X8_P10	C12T28SOI_LLS1_-FA1X33_P10
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X33_P10	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P10	X33_P10
A0	0.0011	0.0032
B0	0.0010	0.0029

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
A0 to CO ↓	0.0401	0.0357	2.5308	0.6244
A0 to CO ↑	0.0371	0.0329	3.9550	1.0065
A0 to S0 ↓	0.0533	0.0491	2.4782	0.6248
A0 to S0 ↑	0.0500	0.0546	3.9049	0.9973
B0 to CO ↓	0.0390	0.0330	2.5280	0.6201
B0 to CO ↑	0.0394	0.0338	3.9548	1.0069
B0 to S0 ↓	0.0547	0.0484	2.4803	0.6247
B0 to S0 ↑	0.0495	0.0525	3.9042	0.9973

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	2.183e-05	1.000e-20
X33_P10	9.085e-05	1.000e-20

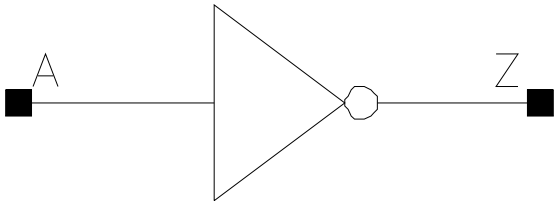
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X33_P10
A0 to CO	2.465e-03	8.073e-03
A0 to S0	2.274e-03	7.884e-03
B0 to CO	2.509e-03	8.258e-03
B0 to S0	2.240e-03	7.610e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X8_P10	X33_P10
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.272	0.3264
X6_P10	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X13_P10	1.200	0.408	0.4896
X17_P10	1.200	0.408	0.4896
X21_P10	1.200	0.544	0.6528
X25_P10	1.200	0.544	0.6528
X29_P10	1.200	0.680	0.8160
X33_P10	1.200	0.680	0.8160
X50_P10	1.200	0.952	1.1424
X58_P10	1.200	1.088	1.3056
X67_P10	1.200	1.224	1.4688
X75_P10	1.200	1.360	1.6320
X84_P10	1.200	1.496	1.7952
X100_P10	1.200	1.768	2.1216
X134_P10	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X13_P10
A	0.0005	0.0007	0.0008	0.0013
	X17_P10	X21_P10	X25_P10	X29_P10
A	0.0016	0.0020	0.0023	0.0028
	X33_P10	X50_P10	X58_P10	X67_P10
A	0.0031	0.0047	0.0054	0.0062
	X75_P10	X84_P10	X100_P10	X134_P10

A	0.0071	0.0080	0.0098	0.0135

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0089	0.0084	4.7632	3.6341
A to Z ↑	0.0143	0.0130	7.6898	5.7689
	X8_P10	**X13_P10**	**X8_P10**	**X13_P10**
A to Z ↓	0.0075	0.0064	2.4643	1.6054
A to Z ↑	0.0116	0.0106	3.9672	2.6174
	X17_P10	**X21_P10**	**X17_P10**	**X21_P10**
A to Z ↓	0.0063	0.0069	1.2189	0.9872
A to Z ↑	0.0100	0.0107	1.9448	1.5701
	X25_P10	**X29_P10**	**X25_P10**	**X29_P10**
A to Z ↓	0.0068	0.0065	0.8339	0.7109
A to Z ↑	0.0103	0.0099	1.3062	1.1196
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0063	0.0066	0.6282	0.4247
A to Z ↑	0.0094	0.0096	0.9788	0.6547
	X58_P10	**X67_P10**	**X58_P10**	**X67_P10**
A to Z ↓	0.0068	0.0067	0.3676	0.3227
A to Z ↑	0.0099	0.0096	0.5637	0.4941
	X75_P10	**X84_P10**	**X75_P10**	**X84_P10**
A to Z ↓	0.0071	0.0072	0.2908	0.2628
A to Z ↑	0.0100	0.0101	0.4419	0.3990
	X100_P10	**X134_P10**	**X100_P10**	**X134_P10**
A to Z ↓	0.0080	0.0087	0.2228	0.1725
A to Z ↑	0.0107	0.0113	0.3357	0.2567

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.195e-06	1.000e-20
X6_P10	4.462e-06	1.000e-20
X8_P10	7.055e-06	1.000e-20
X13_P10	1.003e-05	1.000e-20
X17_P10	1.419e-05	1.000e-20
X21_P10	1.656e-05	1.000e-20
X25_P10	2.042e-05	1.000e-20
X29_P10	2.300e-05	1.000e-20
X33_P10	2.653e-05	1.000e-20
X50_P10	3.874e-05	1.000e-20
X58_P10	4.485e-05	1.000e-20
X67_P10	5.096e-05	1.000e-20
X75_P10	5.707e-05	1.000e-20
X84_P10	6.318e-05	1.000e-20
X100_P10	7.541e-05	1.000e-20
X134_P10	9.985e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X13_P10

A to Z	3.993e-04	4.882e-04	6.326e-04	8.628e-04
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	1.110e-03	1.499e-03	1.742e-03	1.911e-03
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	2.086e-03	3.159e-03	3.823e-03	4.152e-03
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	4.770e-03	5.242e-03	6.441e-03	8.746e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

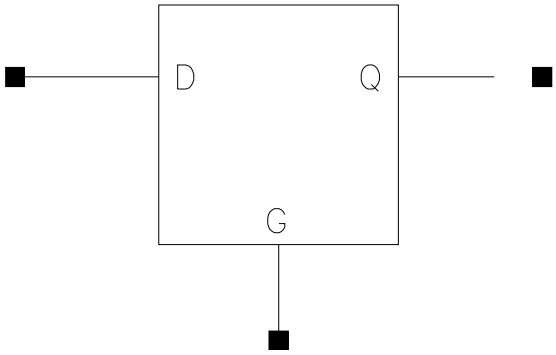
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P10	X21_P10	X25_P10	X29_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P10	X50_P10	X58_P10	X67_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P10	X84_P10	X100_P10	X134_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X23_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P10	X23_P10
D	0.0005	0.0013
G	0.0012	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X23_P10	X8_P10	X23_P10
D to Q ↓	0.0603	0.0469	2.5604	1.2336
D to Q ↑	0.0394	0.0391	3.8914	1.0292
G to Q ↓	0.0648	0.0502	2.5556	1.2337
G to Q ↑	0.0380	0.0339	3.8908	1.0307

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P10	X23_P10
D ↓	hold_falling to G	-0.0137	-0.0039
D ↑	hold_falling to G	-0.0025	-0.0025
D ↓	setup_falling to G	0.0586	0.0387
D ↑	setup_falling to G	0.0458	0.0473
G ↑	min_pulse_width to G	0.0551	0.0485

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.657e-05	1.000e-20
X23_P10	3.890e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X23_P10
D (output stable)	1.131e-05	4.967e-05
G (output stable)	8.073e-04	1.597e-03
D to Q	3.933e-03	7.662e-03
G to Q	3.653e-03	6.853e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

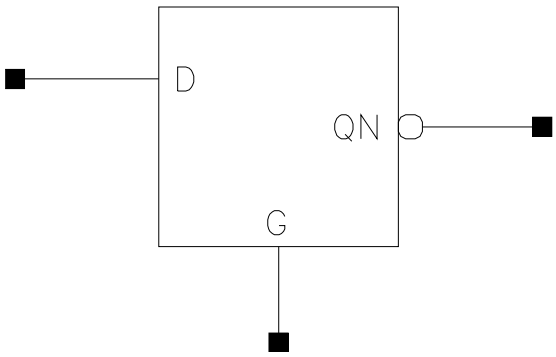
Pin Cycle (vdds)	X8_P10	X23_P10
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P10	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P10
D	0.0006
G	0.0014

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P10	X17_P10
D to QN ↓	0.0534	1.2097
D to QN ↑	0.0672	1.9103
G to QN ↓	0.0514	1.2099
G to QN ↑	0.0693	1.9104

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P10
D ↓	hold_falling to G	-0.0218
D ↑	hold_falling to G	-0.0110
D ↓	setup_falling to G	0.0489
D ↑	setup_falling to G	0.0351
G ↑	min_pulse_width to G	0.0423

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P10	2.648e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X17_P10
D (output stable)	1.138e-05
G (output stable)	9.186e-04
D to QN	4.907e-03
G to QN	4.539e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

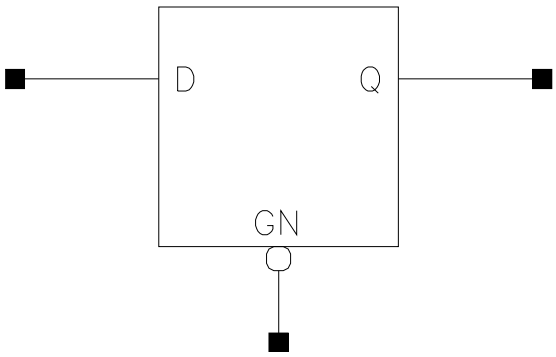
Pin Cycle (vdds)	X17_P10
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X33_P10	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
D	0.0005	0.0008	0.0018
GN	0.0011	0.0015	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D to Q ↓	0.0610	0.0517	2.5679	1.2632
D to Q ↑	0.0402	0.0375	3.8945	1.9916
GN to Q ↓	0.0546	0.0455	2.5697	1.2653
GN to Q ↑	0.0592	0.0560	3.8859	1.9909

	X33_P10		X33_P10	
D to Q ↓	0.0498		0.6453	
D to Q ↑	0.0317		0.9961	
GN to Q ↓	0.0425		0.6456	
GN to Q ↑	0.0426		0.9956	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P10	X17_P10	X33_P10
D ↓	hold_rising to GN	-0.0194	-0.0117	-0.0117
D ↑	hold_rising to GN	-0.0022	0.0004	0.0058
D ↓	setup_rising to GN	0.0666	0.0565	0.0543
D ↑	setup_rising to GN	0.0362	0.0368	0.0293
GN ↓	min_pulse_width to GN	0.0727	0.0604	0.0561

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.615e-05	1.000e-20
X17_P10	2.655e-05	1.000e-20
X33_P10	4.601e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
D (output stable)	1.102e-05	1.858e-05	5.302e-05
GN (output stable)	8.044e-04	1.111e-03	1.400e-03
D to Q	3.955e-03	5.603e-03	9.030e-03
GN to Q	5.537e-03	7.600e-03	1.120e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

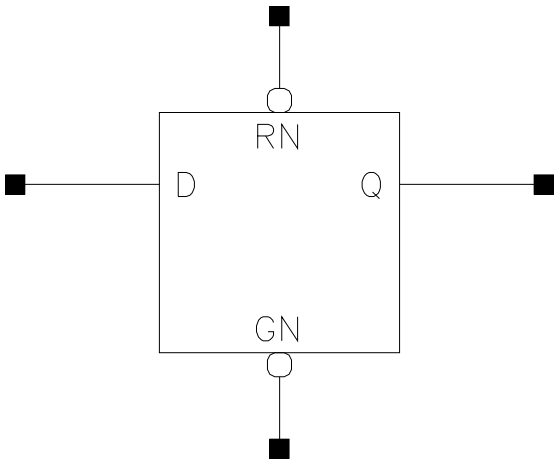
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.496	1.7952
X33_P10	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P10	X33_P10
D	0.0006	0.0013
GN	0.0013	0.0024
RN	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X33_P10	X8_P10	X33_P10
D to Q ↓	0.0568	0.0502	2.5088	0.6483
D to Q ↑	0.0522	0.0669	3.9646	1.0281

GN to Q ↓	0.0513	0.0460	2.5088	0.6490
GN to Q ↑	0.0681	0.0703	3.9700	1.0282
RN to Q ↓	0.0459	0.0876	2.4291	0.7011
RN to Q ↑	0.0557	0.0730	3.9673	1.0281

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P10	X33_P10
D ↓	hold_rising to GN	-0.0166	-0.0096
D ↑	hold_rising to GN	-0.0120	-0.0289
D ↓	setup_rising to GN	0.0618	0.0517
D ↑	setup_rising to GN	0.0513	0.0761
GN ↓	min_pulse_width to GN	0.0647	0.0729
RN ↓	min_pulse_width to RN	0.0540	0.1001
RN ↑	recovery_rising to GN	0.0541	0.0827
RN ↑	removal_rising to GN	-0.0342	-0.0533

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.740e-05	1.000e-20
X33_P10	4.496e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X33_P10
D (output stable)	5.576e-05	1.039e-04
GN (output stable)	9.214e-04	1.428e-03
RN (output stable)	3.427e-05	6.753e-05
D to Q	3.962e-03	1.052e-02
GN to Q	5.669e-03	1.311e-02
RN to Q	3.034e-03	8.515e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

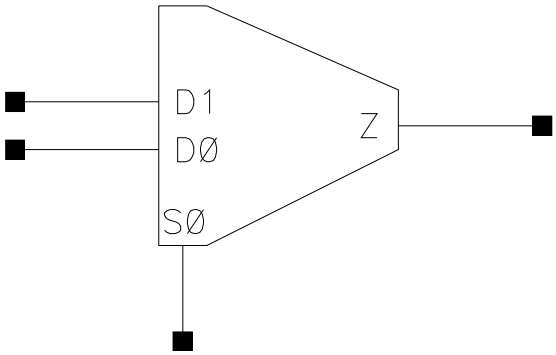
Pin Cycle (vdds)	X8_P10	X33_P10
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
D0	0.0007	0.0011	0.0014	0.0020
D1	0.0007	0.0011	0.0014	0.0019
S0	0.0013	0.0015	0.0017	0.0025

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
D0 to Z ↓	0.0462	0.0404	2.5188	1.2319
D0 to Z ↑	0.0369	0.0334	3.9753	1.9395
D1 to Z ↓	0.0437	0.0398	2.5105	1.2306
D1 to Z ↑	0.0336	0.0314	3.9685	1.9371
S0 to Z ↓	0.0394	0.0377	2.5080	1.2297
S0 to Z ↑	0.0376	0.0372	3.9706	1.9373

	X25_P10	X33_P10	X25_P10	X33_P10
D0 to Z ↓	0.0436	0.0389	0.8467	0.6349
D0 to Z ↑	0.0360	0.0330	1.3034	0.9747
D1 to Z ↓	0.0463	0.0401	0.8493	0.6361
D1 to Z ↑	0.0345	0.0315	1.3023	0.9756
S0 to Z ↓	0.0434	0.0393	0.8461	0.6345
S0 to Z ↑	0.0416	0.0376	1.3018	0.9756

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.922e-05	1.000e-20
X17_P10	3.647e-05	1.000e-20
X25_P10	4.795e-05	1.000e-20
X33_P10	7.151e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	7.265e-04	1.089e-03	1.186e-03	1.642e-03
D1 (output stable)	5.964e-04	1.012e-03	1.320e-03	1.715e-03
S0 (output stable)	9.546e-04	1.085e-03	1.407e-03	1.742e-03
D0 to Z	2.669e-03	4.379e-03	6.842e-03	8.572e-03
D1 to Z	2.456e-03	4.251e-03	6.898e-03	8.455e-03
S0 to Z	3.044e-03	4.665e-03	7.642e-03	9.324e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

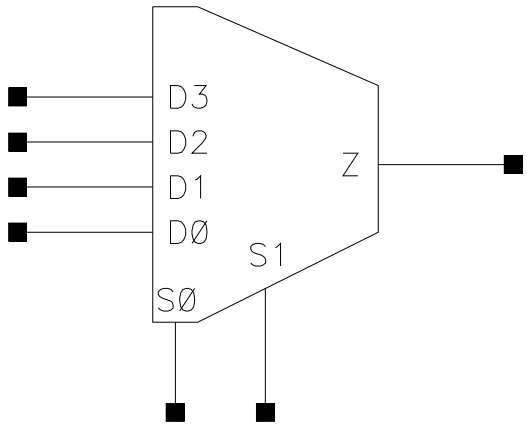
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	2.312	2.7744
X31_P10	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P10	X31_P10
D0	0.0005	0.0014
D1	0.0005	0.0014
D2	0.0005	0.0014
D3	0.0005	0.0014
S0	0.0019	0.0038
S1	0.0012	0.0025

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X31_P10	X8_P10	X31_P10

D0 to Z ↓	0.0796	0.0797	2.6417	0.7282
D0 to Z ↑	0.0538	0.0554	4.0181	1.0751
D1 to Z ↓	0.0790	0.0799	2.6396	0.7283
D1 to Z ↑	0.0540	0.0552	4.0192	1.0756
D2 to Z ↓	0.0857	0.0749	2.6588	0.7218
D2 to Z ↑	0.0570	0.0513	4.0346	1.0691
D3 to Z ↓	0.0854	0.0743	2.6582	0.7205
D3 to Z ↑	0.0564	0.0525	4.0331	1.0718
S0 to Z ↓	0.0886	0.0877	2.6461	0.7241
S0 to Z ↑	0.0669	0.0691	4.0287	1.0740
S1 to Z ↓	0.0639	0.0610	2.6502	0.7248
S1 to Z ↑	0.0517	0.0525	4.0257	1.0732

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.881e-05	1.000e-20
X31_P10	5.917e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X31_P10
D0 (output stable)	1.665e-05	9.590e-05
D1 (output stable)	1.651e-05	8.954e-05
D2 (output stable)	1.923e-05	9.157e-05
D3 (output stable)	1.927e-05	9.784e-05
S0 (output stable)	1.394e-03	3.195e-03
S1 (output stable)	1.119e-03	2.488e-03
D0 to Z	2.985e-03	1.023e-02
D1 to Z	2.975e-03	1.028e-02
D2 to Z	3.210e-03	9.583e-03
D3 to Z	3.200e-03	9.576e-03
S0 to Z	4.550e-03	1.352e-02
S1 to Z	3.544e-03	1.048e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

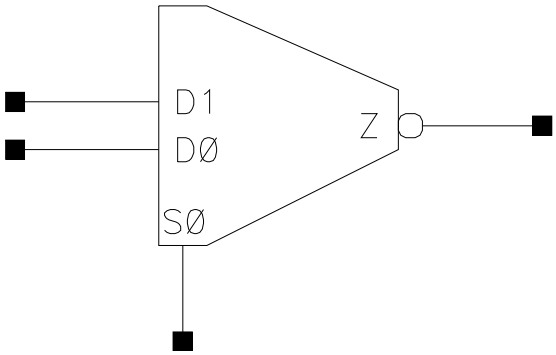
Pin Cycle (vdds)	X8_P10	X31_P10
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.816	0.9792
X5_P10	1.200	0.952	1.1424
X10_P10	1.200	1.768	2.1216
X16_P10	1.200	2.448	2.9376
X21_P10	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P10	X5_P10	X10_P10	X16_P10
D0	0.0005	0.0008	0.0017	0.0025
D1	0.0005	0.0008	0.0016	0.0025
S0	0.0012	0.0020	0.0027	0.0041
	X21_P10			
D0	0.0034			
D1	0.0033			
S0	0.0046			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X5_P10	X3_P10	X5_P10
D0 to Z ↓	0.0157	0.0158	8.3440	4.9728

D0 to Z ↑	0.0262	0.0231	15.9418	8.0088
D1 to Z ↓	0.0155	0.0150	8.2719	4.7891
D1 to Z ↑	0.0272	0.0242	15.9611	8.2343
S0 to Z ↓	0.0243	0.0199	8.2867	4.8757
S0 to Z ↑	0.0262	0.0212	15.9114	8.1105
	X10_P10	**X16_P10**	**X10_P10**	**X16_P10**
D0 to Z ↓	0.0178	0.0165	2.3281	1.5207
D0 to Z ↑	0.0253	0.0239	3.7031	2.4325
D1 to Z ↓	0.0160	0.0158	2.2691	1.4986
D1 to Z ↑	0.0254	0.0246	3.7503	2.4526
S0 to Z ↓	0.0244	0.0209	2.2924	1.5062
S0 to Z ↑	0.0254	0.0218	3.7195	2.4403
	X21_P10		**X21_P10**	
D0 to Z ↓	0.0164		1.1568	
D0 to Z ↑	0.0235		1.8393	
D1 to Z ↓	0.0157		1.1345	
D1 to Z ↑	0.0246		1.8314	
S0 to Z ↓	0.0219		1.1423	
S0 to Z ↑	0.0224		1.8330	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	6.838e-06	1.000e-20
X5_P10	1.613e-05	1.000e-20
X10_P10	2.892e-05	1.000e-20
X16_P10	4.598e-05	1.000e-20
X21_P10	5.645e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	1.124e-05	2.604e-05	7.828e-05	1.222e-04
D1 (output stable)	1.111e-05	2.748e-05	6.685e-05	1.176e-04
S0 (output stable)	8.091e-04	1.207e-03	2.062e-03	3.235e-03
D0 to Z	7.741e-04	1.306e-03	3.263e-03	4.574e-03
D1 to Z	7.736e-04	1.295e-03	3.087e-03	4.523e-03
S0 to Z	1.415e-03	2.134e-03	4.377e-03	6.241e-03
	X21_P10			
D0 (output stable)	1.593e-04			
D1 (output stable)	1.572e-04			
S0 (output stable)	3.595e-03			
D0 to Z	5.896e-03			
D1 to Z	5.963e-03			
S0 to Z	7.630e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P10	X5_P10	X10_P10	X16_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

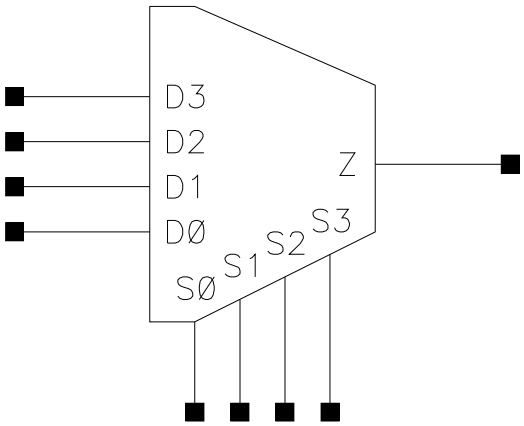
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P10			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	1.768	2.1216
X27_P10	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P10	X27_P10
D0	0.0006	0.0020
D1	0.0007	0.0020
D2	0.0006	0.0020
D3	0.0007	0.0020
S0	0.0006	0.0019
S1	0.0007	0.0019
S2	0.0007	0.0019
S3	0.0007	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	X27_P10	X7_P10	X27_P10
D0 to Z ↓	0.0609	0.0502	4.2161	1.1415
D0 to Z ↑	0.0448	0.0376	3.9176	0.9727
D1 to Z ↓	0.0552	0.0457	4.2115	1.1404
D1 to Z ↑	0.0401	0.0328	3.9015	0.9679
D2 to Z ↓	0.0619	0.0479	4.2238	1.1419
D2 to Z ↑	0.0439	0.0350	3.9336	0.9763
D3 to Z ↓	0.0563	0.0434	4.2182	1.1400
D3 to Z ↑	0.0393	0.0303	3.9150	0.9715
S0 to Z ↓	0.0590	0.0473	4.2146	1.1410
S0 to Z ↑	0.0474	0.0391	3.9165	0.9725
S1 to Z ↓	0.0537	0.0428	4.2100	1.1403
S1 to Z ↑	0.0426	0.0340	3.9008	0.9683
S2 to Z ↓	0.0600	0.0450	4.2217	1.1409
S2 to Z ↑	0.0465	0.0365	3.9326	0.9764
S3 to Z ↓	0.0548	0.0405	4.2171	1.1396
S3 to Z ↑	0.0417	0.0315	3.9154	0.9714

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X7_P10	1.760e-05	1.000e-20
X27_P10	7.294e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X7_P10	X27_P10
D0 (output stable)	4.224e-04	1.342e-03
D1 (output stable)	3.599e-04	1.114e-03
D2 (output stable)	3.924e-04	1.236e-03
D3 (output stable)	3.298e-04	1.011e-03
S0 (output stable)	4.117e-04	1.272e-03
S1 (output stable)	3.476e-04	1.056e-03
S2 (output stable)	3.813e-04	1.168e-03
S3 (output stable)	3.177e-04	9.550e-04
D0 to Z	3.345e-03	1.041e-02
D1 to Z	2.948e-03	8.984e-03
D2 to Z	3.250e-03	9.147e-03
D3 to Z	2.857e-03	7.743e-03
S0 to Z	3.264e-03	9.889e-03
S1 to Z	2.866e-03	8.509e-03
S2 to Z	3.165e-03	8.616e-03
S3 to Z	2.777e-03	7.272e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

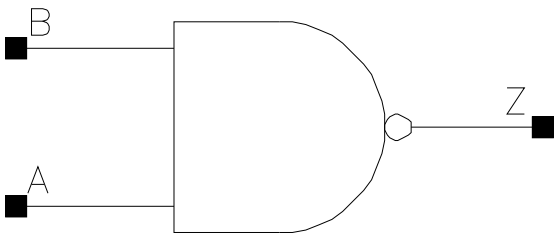
Pin Cycle (vdds)	X7_P10	X27_P10
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P10	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P10	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P10	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P10	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P10	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P10	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P10	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P10	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P10	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P10	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P10	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P10	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P10	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P10	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P10	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P10	C12T28SOI_LL_-NAND2X5_P10	C12T28SOI_LL_-NAND2X7_P10	C12T28SOI_LL_-NAND2X10_P10
A	0.0005	0.0007	0.0008	0.0013
B	0.0006	0.0007	0.0008	0.0012
	C12T28SOI_LL_-NAND2X13_P10	C12T28SOI_LL_-NAND2X17_P10	C12T28SOI_LL_-NAND2X20_P10	C12T28SOI_LL_-NAND2X24_P10
A	0.0016	0.0021	0.0024	0.0029
B	0.0015	0.0020	0.0022	0.0027
	C12T28SOI_LL_-NAND2X27_P10	C12T28SOI_LL_-NAND2X42_P10	C12T28SOI_LL_-NAND2X47_P10	C12T28SOI_LL_-NAND2X50_P10
A	0.0032	0.0010	0.0010	0.0010
B	0.0030	0.0011	0.0011	0.0011
	C12T28SOI_LL_-NAND2X58_P10	C12T28SOI_LL_-NAND2X67_P10	C12T28SOI_-LLBR0D8_-NAND2X7_P10	C12T28SOI_-LLBR0D8_-NAND2X14_P10
A	0.0010	0.0010	0.0008	0.0016
B	0.0011	0.0011	0.0008	0.0015
	C12T28SOI_LLS_-NAND2X40_P10	C12T28SOI_LLS_-NAND2X54_P10		
A	0.0048	0.0064		
B	0.0044	0.0059		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P10	**C12T28SOI_LL_-NAND2X5_P10**	**C12T28SOI_LL_-NAND2X3_P10**	**C12T28SOI_LL_-NAND2X5_P10**
A to Z ↓	0.0118	0.0107	8.1146	5.1716
A to Z ↑	0.0170	0.0152	7.6952	4.8865
B to Z ↓	0.0130	0.0114	8.1741	5.2124
B to Z ↑	0.0155	0.0133	7.7337	4.9143
	C12T28SOI_LL_-NAND2X7_P10	**C12T28SOI_LL_-NAND2X10_P10**	**C12T28SOI_LL_-NAND2X7_P10**	**C12T28SOI_LL_-NAND2X10_P10**
A to Z ↓	0.0107	0.0124	4.3187	2.8658
A to Z ↑	0.0147	0.0160	3.9428	2.5973
B to Z ↓	0.0113	0.0112	4.3458	2.8895
B to Z ↑	0.0127	0.0127	3.9756	2.6138
	C12T28SOI_LL_-NAND2X13_P10	**C12T28SOI_LL_-NAND2X17_P10**	**C12T28SOI_LL_-NAND2X13_P10**	**C12T28SOI_LL_-NAND2X17_P10**
A to Z ↓	0.0118	0.0117	2.1911	1.7524

A to Z ↑	0.0149	0.0152	1.9359	1.5635
B to Z ↓	0.0105	0.0113	2.2109	1.7658
B to Z ↑	0.0115	0.0125	1.9492	1.5727
	C12T28SOI_LL_-NAND2X20_P10	**C12T28SOI_LL_-NAND2X24_P10**	**C12T28SOI_LL_-NAND2X20_P10**	**C12T28SOI_LL_-NAND2X24_P10**
A to Z ↓	0.0115	0.0119	1.4946	1.2742
A to Z ↑	0.0146	0.0150	1.3003	1.1142
B to Z ↓	0.0112	0.0109	1.5065	1.2847
B to Z ↑	0.0119	0.0118	1.3096	1.1214
	C12T28SOI_LL_-NAND2X27_P10	**C12T28SOI_LL_-NAND2X42_P10**	**C12T28SOI_LL_-NAND2X27_P10**	**C12T28SOI_LL_-NAND2X42_P10**
A to Z ↓	0.0117	0.0436	1.1330	0.5046
A to Z ↑	0.0145	0.0436	0.9753	0.7710
B to Z ↓	0.0107	0.0448	1.1424	0.5045
B to Z ↑	0.0114	0.0418	0.9811	0.7724
	C12T28SOI_LL_-NAND2X47_P10	**C12T28SOI_LL_-NAND2X50_P10**	**C12T28SOI_LL_-NAND2X47_P10**	**C12T28SOI_LL_-NAND2X50_P10**
A to Z ↓	0.0449	0.0455	0.4495	0.4212
A to Z ↑	0.0443	0.0448	0.6732	0.6440
B to Z ↓	0.0462	0.0467	0.4497	0.4214
B to Z ↑	0.0425	0.0430	0.6724	0.6446
	C12T28SOI_LL_-NAND2X58_P10	**C12T28SOI_LL_-NAND2X67_P10**	**C12T28SOI_LL_-NAND2X58_P10**	**C12T28SOI_LL_-NAND2X67_P10**
A to Z ↓	0.0475	0.0497	0.3644	0.3211
A to Z ↑	0.0462	0.0477	0.5547	0.4869
B to Z ↓	0.0488	0.0510	0.3645	0.3211
B to Z ↑	0.0445	0.0460	0.5546	0.4872
	C12T28SOI_-LLBR0D8_-NAND2X7_P10	**C12T28SOI_-LLBR0D8_-NAND2X14_P10**	**C12T28SOI_-LLBR0D8_-NAND2X7_P10**	**C12T28SOI_-LLBR0D8_-NAND2X14_P10**
A to Z ↓	0.0087	0.0100	3.2378	1.6854
A to Z ↑	0.0183	0.0186	5.2505	2.5611
B to Z ↓	0.0086	0.0079	3.2723	1.7092
B to Z ↑	0.0152	0.0136	5.3886	2.6009
	C12T28SOI_LLS_-NAND2X40_P10	**C12T28SOI_LLS_-NAND2X54_P10**	**C12T28SOI_LLS_-NAND2X40_P10**	**C12T28SOI_LLS_-NAND2X54_P10**
A to Z ↓	0.0116	0.0115	0.7668	0.5793
A to Z ↑	0.0144	0.0143	0.6528	0.4914
B to Z ↓	0.0107	0.0109	0.7728	0.5841
B to Z ↑	0.0112	0.0113	0.6575	0.4948

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P10	3.290e-06	1.000e-20
C12T28SOI_LL_NAND2X5_P10	5.815e-06	1.000e-20
C12T28SOI_LL_NAND2X7_P10	7.342e-06	1.000e-20
C12T28SOI_LL_NAND2X10_P10	1.004e-05	1.000e-20
C12T28SOI_LL_NAND2X13_P10	1.424e-05	1.000e-20
C12T28SOI_LL_NAND2X17_P10	1.678e-05	1.000e-20
C12T28SOI_LL_NAND2X20_P10	2.068e-05	1.000e-20
C12T28SOI_LL_NAND2X24_P10	2.350e-05	1.000e-20
C12T28SOI_LL_NAND2X27_P10	2.713e-05	1.000e-20

C12T28SOI_LL_NAND2X42_P10	4.967e-05	1.000e-20
C12T28SOI_LL_NAND2X47_P10	5.377e-05	1.000e-20
C12T28SOI_LL_NAND2X50_P10	5.504e-05	1.000e-20
C12T28SOI_LL_NAND2X58_P10	6.041e-05	1.000e-20
C12T28SOI_LL_NAND2X67_P10	6.578e-05	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_-P10	7.248e-06	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_-P10	1.374e-05	1.000e-20
C12T28SOI_LLS_NAND2X40_P10	4.005e-05	1.000e-20
C12T28SOI_LLS_NAND2X54_P10	5.296e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND2X3_P10	C12T28SOI_LL_-NAND2X5_P10	C12T28SOI_LL_-NAND2X7_P10	C12T28SOI_LL_-NAND2X10_P10
A (output stable)	8.642e-06	1.377e-05	1.650e-05	5.605e-05
B (output stable)	1.682e-05	2.644e-05	3.288e-05	1.888e-04
A to Z	5.520e-04	7.515e-04	9.027e-04	1.568e-03
B to Z	4.657e-04	6.135e-04	7.319e-04	1.094e-03
	C12T28SOI_LL_-NAND2X13_P10	C12T28SOI_LL_-NAND2X17_P10	C12T28SOI_LL_-NAND2X20_P10	C12T28SOI_LL_-NAND2X24_P10
A (output stable)	6.758e-05	7.968e-05	8.778e-05	1.231e-04
B (output stable)	2.122e-04	1.959e-04	2.166e-04	3.482e-04
A to Z	1.913e-03	2.409e-03	2.765e-03	3.369e-03
B to Z	1.328e-03	1.794e-03	2.065e-03	2.380e-03
	C12T28SOI_LL_-NAND2X27_P10	C12T28SOI_LL_-NAND2X42_P10	C12T28SOI_LL_-NAND2X47_P10	C12T28SOI_LL_-NAND2X50_P10
A (output stable)	1.329e-04	1.884e-05	1.892e-05	1.884e-05
B (output stable)	3.696e-04	3.500e-05	3.507e-05	3.505e-05
A to Z	3.685e-03	9.247e-03	9.999e-03	1.038e-02
B to Z	2.599e-03	9.069e-03	9.823e-03	1.021e-02
	C12T28SOI_LL_-NAND2X58_P10	C12T28SOI_LL_-NAND2X67_P10	C12T28SOI_-LLBR0D8_-NAND2X7_P10	C12T28SOI_-LLBR0D8_-NAND2X14_P10
A (output stable)	1.894e-05	1.901e-05	2.151e-05	8.420e-05
B (output stable)	3.515e-05	3.517e-05	4.318e-05	2.582e-04
A to Z	1.177e-02	1.311e-02	9.339e-04	2.015e-03
B to Z	1.159e-02	1.294e-02	6.886e-04	1.236e-03
	C12T28SOI_LLS_-NAND2X40_P10	C12T28SOI_LLS_-NAND2X54_P10		
A (output stable)	1.888e-04	2.457e-04		
B (output stable)	5.017e-04	6.363e-04		
A to Z	5.421e-03	7.122e-03		
B to Z	3.857e-03	5.129e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND2X3_P10	C12T28SOI_LL_-NAND2X5_P10	C12T28SOI_LL_-NAND2X7_P10	C12T28SOI_LL_-NAND2X10_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

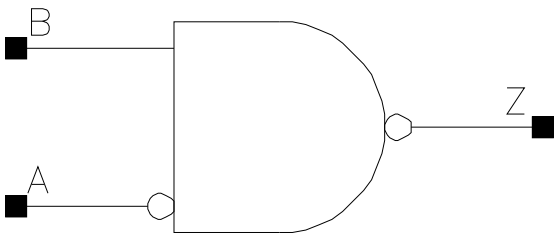
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X13_P10	C12T28SOI_LL_-NAND2X17_P10	C12T28SOI_LL_-NAND2X20_P10	C12T28SOI_LL_-NAND2X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P10	C12T28SOI_LL_-NAND2X42_P10	C12T28SOI_LL_-NAND2X47_P10	C12T28SOI_LL_-NAND2X50_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P10	C12T28SOI_LL_-NAND2X67_P10	C12T28SOI_-LLBR0D8_-NAND2X7_P10	C12T28SOI_-LLBR0D8_-NAND2X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P10	C12T28SOI_LLS_-NAND2X54_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X7_P10	1.200	0.544	0.6528
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X40_P10	1.200	2.312	2.7744
X54_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P10	X7_P10	X13_P10	X27_P10
A	0.0008	0.0008	0.0011	0.0020
B	0.0006	0.0008	0.0015	0.0030
	X40_P10	X54_P10		
A	0.0031	0.0039		
B	0.0044	0.0059		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0317	0.0336	8.1195	4.3187
A to Z ↑	0.0253	0.0262	7.5486	3.9087
B to Z ↓	0.0134	0.0114	8.2604	4.3792
B to Z ↑	0.0156	0.0127	7.7378	4.0015
	X13_P10	**X27_P10**	**X13_P10**	**X27_P10**

A to Z ↓	0.0306	0.0298	2.2788	1.1321
A to Z ↑	0.0247	0.0241	1.9942	0.9673
B to Z ↓	0.0104	0.0104	2.3180	1.1516
B to Z ↑	0.0115	0.0112	1.9968	0.9829
	X40_P10	**X54_P10**	**X40_P10**	**X54_P10**
A to Z ↓	0.0302	0.0299	0.7575	0.5734
A to Z ↑	0.0245	0.0242	0.6448	0.4860
B to Z ↓	0.0105	0.0106	0.7703	0.5834
B to Z ↑	0.0112	0.0112	0.6592	0.4964

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	6.062e-06	1.000e-20
X7_P10	1.012e-05	1.000e-20
X13_P10	2.130e-05	1.000e-20
X27_P10	4.100e-05	1.000e-20
X40_P10	6.005e-05	1.000e-20
X54_P10	7.908e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	8.582e-04	1.090e-03	1.784e-03	3.476e-03
B (output stable)	1.724e-05	3.294e-05	1.869e-04	3.221e-04
A to Z	1.460e-03	2.040e-03	3.730e-03	7.312e-03
B to Z	4.724e-04	7.253e-04	1.307e-03	2.599e-03
	X40_P10	X54_P10		
A (output stable)	5.317e-03	6.891e-03		
B (output stable)	4.659e-04	5.940e-04		
A to Z	1.102e-02	1.442e-02		
B to Z	3.833e-03	5.089e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

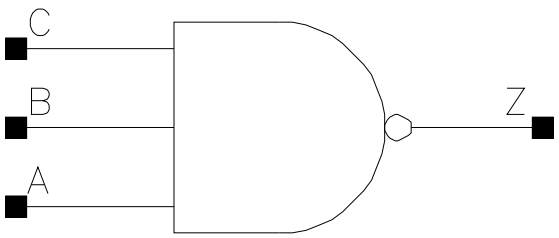
Pin Cycle (vdds)	X3_P10	X7_P10	X13_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P10	X54_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P10	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P10	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P10	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P10	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P10	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P10	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P10	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P10	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P10	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P10	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P10	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P10	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P10	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P10	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P10	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P10	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A	0.0007	0.0008	0.0013	0.0016
B	0.0007	0.0009	0.0013	0.0016
C	0.0006	0.0008	0.0012	0.0015
	C12T28SOI_LL_-NAND3X15_P10	C12T28SOI_LL_-NAND3X18_P10	C12T28SOI_LL_-NAND3X21_P10	C12T28SOI_LL_-NAND3X24_P10
A	0.0021	0.0024	0.0029	0.0032
B	0.0020	0.0023	0.0028	0.0031
C	0.0019	0.0022	0.0026	0.0029
	C12T28SOI_LL_-NAND3X35_P10	C12T28SOI_LL_-NAND3X47_P10	C12T28SOI_-LLBR0P6_-NAND3X6_P10	C12T28SOI_-LLBR0P6_-NAND3X12_P10
A	0.0049	0.0064	0.0008	0.0017
B	0.0046	0.0061	0.0009	0.0016
C	0.0044	0.0059	0.0008	0.0015
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	C12T28SOI_-LLBR0P6_-NAND3X24_P10	C12T28SOI_-LLBR0P6_-NAND3X35_P10	C12T28SOI_-LLBR0P6_-NAND3X47_P10
A	0.0024	0.0032	0.0049	0.0064
B	0.0023	0.0031	0.0046	0.0061
C	0.0021	0.0028	0.0042	0.0057
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10			
A	0.0026			
B	0.0024			
C	0.0022			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10
A to Z ↓	0.0196	0.0177	8.4805	6.0248
A to Z ↑	0.0217	0.0194	5.5830	3.8319
B to Z ↓	0.0208	0.0184	8.4978	6.0381
B to Z ↑	0.0208	0.0183	5.5920	3.8382
C to Z ↓	0.0184	0.0165	8.5193	6.0534
C to Z ↑	0.0179	0.0157	5.5941	3.8570

	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A to Z ↓	0.0195	0.0182	4.1046	3.1625
A to Z ↑	0.0204	0.0189	2.6103	1.9516
B to Z ↓	0.0184	0.0173	4.1146	3.1704
B to Z ↑	0.0185	0.0172	2.6132	1.9538
C to Z ↓	0.0164	0.0154	4.1270	3.1807
C to Z ↑	0.0157	0.0143	2.6070	1.9428
	C12T28SOI_LL_-NAND3X15_P10	**C12T28SOI_LL_-NAND3X18_P10**	**C12T28SOI_LL_-NAND3X15_P10**	**C12T28SOI_LL_-NAND3X18_P10**
A to Z ↓	0.0174	0.0166	2.5694	2.1850
A to Z ↑	0.0185	0.0176	1.5629	1.2989
B to Z ↓	0.0172	0.0164	2.5760	2.1908
B to Z ↑	0.0168	0.0159	1.5657	1.3013
C to Z ↓	0.0157	0.0149	2.5833	2.1974
C to Z ↑	0.0142	0.0133	1.5748	1.3089
	C12T28SOI_LL_-NAND3X21_P10	**C12T28SOI_LL_-NAND3X24_P10**	**C12T28SOI_LL_-NAND3X21_P10**	**C12T28SOI_LL_-NAND3X24_P10**
A to Z ↓	0.0180	0.0176	1.8466	1.6451
A to Z ↑	0.0187	0.0182	1.1194	0.9806
B to Z ↓	0.0172	0.0169	1.8516	1.6492
B to Z ↑	0.0169	0.0164	1.1207	0.9816
C to Z ↓	0.0156	0.0153	1.8571	1.6543
C to Z ↑	0.0142	0.0138	1.1224	0.9825
	C12T28SOI_LL_-NAND3X35_P10	**C12T28SOI_LL_-NAND3X47_P10**	**C12T28SOI_LL_-NAND3X35_P10**	**C12T28SOI_LL_-NAND3X47_P10**
A to Z ↓	0.0167	0.0168	1.1199	0.8501
A to Z ↑	0.0176	0.0176	0.6562	0.4947
B to Z ↓	0.0164	0.0165	1.1229	0.8524
B to Z ↑	0.0158	0.0158	0.6562	0.4940
C to Z ↓	0.0147	0.0149	1.1268	0.8553
C to Z ↑	0.0129	0.0129	0.6599	0.4964
	C12T28SOI_-LLBR0P6_-NAND3X6_P10	**C12T28SOI_-LLBR0P6_-NAND3X12_P10**	**C12T28SOI_-LLBR0P6_-NAND3X6_P10**	**C12T28SOI_-LLBR0P6_-NAND3X12_P10**
A to Z ↓	0.0138	0.0146	4.0456	2.1268
A to Z ↑	0.0278	0.0275	6.0625	3.0825
B to Z ↓	0.0139	0.0130	4.0670	2.1392
B to Z ↑	0.0252	0.0235	6.0759	3.0858
C to Z ↓	0.0111	0.0099	4.0973	2.1579
C to Z ↑	0.0196	0.0176	6.1037	3.0933
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	**C12T28SOI_-LLBR0P6_-NAND3X24_P10**	**C12T28SOI_-LLBR0P6_-NAND3X18_P10**	**C12T28SOI_-LLBR0P6_-NAND3X24_P10**
A to Z ↓	0.0133	0.0140	1.4731	1.1097
A to Z ↑	0.0259	0.0264	2.0522	1.5481
B to Z ↓	0.0125	0.0127	1.4816	1.1162
B to Z ↑	0.0221	0.0226	2.0560	1.5506
C to Z ↓	0.0100	0.0098	1.4927	1.1259
C to Z ↑	0.0168	0.0169	2.0685	1.5510
	C12T28SOI_-LLBR0P6_-NAND3X35_P10	**C12T28SOI_-LLBR0P6_-NAND3X47_P10**	**C12T28SOI_-LLBR0P6_-NAND3X35_P10**	**C12T28SOI_-LLBR0P6_-NAND3X47_P10**

A to Z ↓	0.0133	0.0135	0.7582	0.5776
A to Z ↑	0.0260	0.0260	1.0560	0.7970
B to Z ↓	0.0124	0.0124	0.7627	0.5809
B to Z ↑	0.0222	0.0221	1.0563	0.7966
C to Z ↓	0.0094	0.0098	0.7696	0.5859
C to Z ↑	0.0162	0.0165	1.0648	0.8002
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P10**	
A to Z ↓	0.0145		1.4168	
A to Z ↑	0.0262		1.9294	
B to Z ↓	0.0128		1.4250	
B to Z ↑	0.0224		1.9309	
C to Z ↓	0.0096		1.4367	
C to Z ↑	0.0164		1.9208	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P10	4.137e-06	1.000e-20
C12T28SOI_LL_NAND3X6_P10	6.436e-06	1.000e-20
C12T28SOI_LL_NAND3X9_P10	8.463e-06	1.000e-20
C12T28SOI_LL_NAND3X12_P10	1.188e-05	1.000e-20
C12T28SOI_LL_NAND3X15_P10	1.347e-05	1.000e-20
C12T28SOI_LL_NAND3X18_P10	1.654e-05	1.000e-20
C12T28SOI_LL_NAND3X21_P10	1.946e-05	1.000e-20
C12T28SOI_LL_NAND3X24_P10	2.239e-05	1.000e-20
C12T28SOI_LL_NAND3X35_P10	3.289e-05	1.000e-20
C12T28SOI_LL_NAND3X47_P10	4.336e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_-P10	6.641e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P10	1.196e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P10	1.609e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P10	2.199e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P10	3.202e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P10	4.200e-05	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P10	2.013e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A (output stable)	1.848e-05	2.523e-05	6.275e-05	7.373e-05
B (output stable)	3.416e-05	4.192e-05	1.124e-04	1.256e-04
C (output stable)	1.745e-04	2.036e-04	3.315e-04	3.759e-04
A to Z	1.242e-03	1.542e-03	2.478e-03	2.957e-03
B to Z	1.121e-03	1.359e-03	2.013e-03	2.413e-03
C to Z	8.801e-04	1.071e-03	1.545e-03	1.850e-03

	C12T28SOI_LL_-NAND3X15_P10	C12T28SOI_LL_-NAND3X18_P10	C12T28SOI_LL_-NAND3X21_P10	C12T28SOI_LL_-NAND3X24_P10
A (output stable)	8.023e-05	8.997e-05	1.237e-04	1.365e-04
B (output stable)	1.364e-04	1.552e-04	2.139e-04	2.318e-04
C (output stable)	3.838e-04	4.378e-04	6.200e-04	6.686e-04
A to Z	3.508e-03	3.898e-03	5.022e-03	5.508e-03
B to Z	2.866e-03	3.162e-03	4.094e-03	4.484e-03
C to Z	2.247e-03	2.450e-03	3.152e-03	3.450e-03
	C12T28SOI_LL_-NAND3X35_P10	C12T28SOI_LL_-NAND3X47_P10	C12T28SOI_-LLBR0P6_-NAND3X6_P10	C12T28SOI_-LLBR0P6_-NAND3X12_P10
A (output stable)	1.789e-04	2.335e-04	3.566e-05	1.044e-04
B (output stable)	3.024e-04	3.917e-04	5.873e-05	1.804e-04
C (output stable)	9.366e-04	1.202e-03	2.677e-04	5.327e-04
A to Z	7.755e-03	1.022e-02	1.667e-03	3.266e-03
B to Z	6.302e-03	8.310e-03	1.379e-03	2.438e-03
C to Z	4.705e-03	6.301e-03	9.350e-04	1.542e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	C12T28SOI_-LLBR0P6_-NAND3X24_P10	C12T28SOI_-LLBR0P6_-NAND3X35_P10	C12T28SOI_-LLBR0P6_-NAND3X47_P10
A (output stable)	1.258e-04	1.914e-04	2.549e-04	3.339e-04
B (output stable)	2.102e-04	3.308e-04	4.356e-04	5.744e-04
C (output stable)	5.859e-04	9.530e-04	1.368e-03	1.706e-03
A to Z	4.355e-03	6.061e-03	8.647e-03	1.132e-02
B to Z	3.245e-03	4.521e-03	6.419e-03	8.404e-03
C to Z	2.151e-03	2.877e-03	3.937e-03	5.247e-03
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10			
A (output stable)	1.543e-04			
B (output stable)	2.638e-04			
C (output stable)	7.597e-04			
A to Z	4.857e-03			
B to Z	3.625e-03			
C to Z	2.285e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P10	C12T28SOI_LL_-NAND3X6_P10	C12T28SOI_LL_-NAND3X9_P10	C12T28SOI_LL_-NAND3X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P10	C12T28SOI_LL_-NAND3X18_P10	C12T28SOI_LL_-NAND3X21_P10	C12T28SOI_LL_-NAND3X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

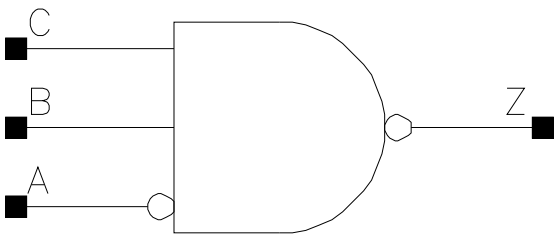
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P10	C12T28SOI_LL_-NAND3X47_P10	C12T28SOI_-LLBR0P6_-NAND3X6_P10	C12T28SOI_-LLBR0P6_-NAND3X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P10	C12T28SOI_-LLBR0P6_-NAND3X24_P10	C12T28SOI_-LLBR0P6_-NAND3X35_P10	C12T28SOI_-LLBR0P6_-NAND3X47_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.816	0.9792
X12_P10	1.200	1.224	1.4688
X18_P10	1.200	1.496	1.7952
X24_P10	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0008	0.0011	0.0011	0.0020
B	0.0008	0.0016	0.0023	0.0031
C	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X12_P10**	**X6_P10**	**X12_P10**
A to Z ↓	0.0383	0.0363	6.0715	3.1930
A to Z ↑	0.0282	0.0272	3.7956	1.9057
B to Z ↓	0.0157	0.0163	6.1040	3.2108
B to Z ↑	0.0163	0.0161	3.8480	1.9362
C to Z ↓	0.0158	0.0143	6.1252	3.2227
C to Z ↑	0.0145	0.0131	3.8663	1.9483
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0415	0.0350	2.1871	1.6497

A to Z ↑	0.0313	0.0258	1.2813	0.9598
B to Z ↓	0.0165	0.0161	2.1973	1.6591
B to Z ↑	0.0160	0.0157	1.3019	0.9782
C to Z ↓	0.0151	0.0143	2.2032	1.6648
C to Z ↑	0.0135	0.0127	1.3096	0.9846

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P10	8.876e-06	1.000e-20
X12_P10	1.874e-05	1.000e-20
X18_P10	2.325e-05	1.000e-20
X24_P10	3.661e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	1.066e-03	1.902e-03	2.570e-03	3.517e-03
B (output stable)	2.688e-05	1.015e-04	1.688e-04	2.363e-04
C (output stable)	7.631e-05	3.745e-04	4.440e-04	6.914e-04
A to Z	2.444e-03	4.811e-03	6.863e-03	9.181e-03
B to Z	1.113e-03	2.197e-03	3.195e-03	4.168e-03
C to Z	9.377e-04	1.615e-03	2.480e-03	3.076e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

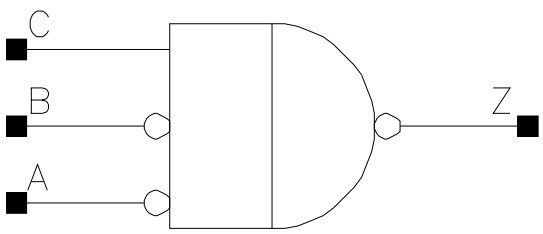
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P10	1.200	0.816	0.9792
X13_P10	1.200	1.088	1.3056
X20_P10	1.200	1.632	1.9584
X27_P10	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P10	X13_P10	X20_P10	X27_P10
A	0.0010	0.0010	0.0020	0.0018
B	0.0011	0.0011	0.0020	0.0019
C	0.0008	0.0015	0.0022	0.0030

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P10	**X13_P10**	**X7_P10**	**X13_P10**
A to Z ↓	0.0352	0.0427	4.1427	2.1917
A to Z ↑	0.0242	0.0275	3.7733	1.8981
B to Z ↓	0.0353	0.0431	4.1429	2.1900
B to Z ↑	0.0227	0.0262	3.7717	1.8946
C to Z ↓	0.0112	0.0102	4.1961	2.2133
C to Z ↑	0.0126	0.0112	3.8581	1.9483
	X20_P10	**X27_P10**	**X20_P10**	**X27_P10**
A to Z ↓	0.0389	0.0431	1.4886	1.1279
A to Z ↑	0.0256	0.0309	1.2774	0.9593
B to Z ↓	0.0365	0.0414	1.4886	1.1278

B to Z ↑	0.0234	0.0291	1.2739	0.9583
C to Z ↓	0.0115	0.0111	1.5068	1.1401
C to Z ↑	0.0123	0.0119	1.3089	0.9829

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X7_P10	1.369e-05	1.000e-20
X13_P10	1.855e-05	1.000e-20
X20_P10	3.002e-05	1.000e-20
X27_P10	3.357e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	6.063e-04	8.056e-04	1.371e-03	1.618e-03
B (output stable)	5.388e-04	7.388e-04	1.203e-03	1.477e-03
C (output stable)	3.528e-05	2.246e-04	2.108e-04	2.365e-04
A to Z	2.737e-03	4.458e-03	7.034e-03	8.804e-03
B to Z	2.493e-03	4.218e-03	6.193e-03	8.065e-03
C to Z	7.554e-04	1.290e-03	2.176e-03	2.838e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

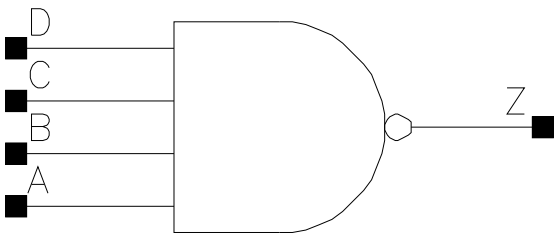
Pin Cycle (vdds)	X7_P10	X13_P10	X20_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0007	0.0006	0.0008	0.0010
B	0.0007	0.0007	0.0009	0.0011
C	0.0006	0.0007	0.0009	0.0010
D	0.0007	0.0007	0.0009	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0584	0.0571	2.4538	1.2283
A to Z ↑	0.0460	0.0496	3.8401	1.9110
B to Z ↓	0.0600	0.0597	2.4511	1.2287
B to Z ↑	0.0444	0.0490	3.8412	1.9111
C to Z ↓	0.0590	0.0572	2.4510	1.2286
C to Z ↑	0.0472	0.0519	3.8378	1.9080

D to Z ↓	0.0610	0.0588	2.4529	1.2287
D to Z ↑	0.0462	0.0500	3.8367	1.9088
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0602	0.0554	0.8448	0.6332
A to Z ↑	0.0477	0.0467	1.2850	0.9654
B to Z ↓	0.0621	0.0569	0.8436	0.6330
B to Z ↑	0.0464	0.0452	1.2840	0.9654
C to Z ↓	0.0556	0.0512	0.8436	0.6323
C to Z ↑	0.0481	0.0468	1.2824	0.9609
D to Z ↓	0.0573	0.0528	0.8442	0.6328
D to Z ↑	0.0463	0.0452	1.2823	0.9628

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.460e-05	1.000e-20
X17_P10	2.335e-05	1.000e-20
X25_P10	3.339e-05	1.000e-20
X33_P10	4.592e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	4.276e-04	5.329e-04	7.771e-04	9.319e-04
B (output stable)	3.949e-04	5.063e-04	7.291e-04	8.689e-04
C (output stable)	4.264e-04	5.165e-04	7.791e-04	8.856e-04
D (output stable)	3.938e-04	4.805e-04	7.246e-04	8.194e-04
A to Z	3.252e-03	4.981e-03	7.686e-03	9.443e-03
B to Z	3.160e-03	4.903e-03	7.548e-03	9.271e-03
C to Z	3.332e-03	4.922e-03	7.157e-03	8.772e-03
D to Z	3.250e-03	4.825e-03	7.015e-03	8.599e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

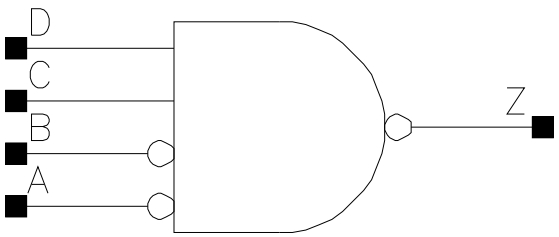
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X12_P10	1.200	1.496	1.7952
X18_P10	1.200	2.040	2.4480
X24_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P10	X12_P10	X18_P10	X24_P10
A	0.0010	0.0011	0.0020	0.0018
B	0.0010	0.0014	0.0020	0.0019
C	0.0008	0.0016	0.0023	0.0031
D	0.0008	0.0015	0.0022	0.0030

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X12_P10	X6_P10	X12_P10
A to Z ↓	0.0375	0.0507	6.2229	3.2009
A to Z ↑	0.0254	0.0311	3.7720	1.9020
B to Z ↓	0.0369	0.0498	6.2250	3.2015
B to Z ↑	0.0231	0.0294	3.7685	1.8989
C to Z ↓	0.0159	0.0162	6.2557	3.2109
C to Z ↑	0.0164	0.0161	4.0224	1.9363

D to Z ↓	0.0156	0.0141	6.2777	3.2217
D to Z ↑	0.0144	0.0130	4.0426	1.9482
	X18_P10	**X24_P10**	**X18_P10**	**X24_P10**
A to Z ↓	0.0436	0.0486	2.1822	1.6535
A to Z ↑	0.0274	0.0348	1.2772	0.9607
B to Z ↓	0.0414	0.0468	2.1825	1.6540
B to Z ↑	0.0252	0.0327	1.2756	0.9590
C to Z ↓	0.0160	0.0167	2.1913	1.6588
C to Z ↑	0.0156	0.0161	1.3058	0.9764
D to Z ↓	0.0146	0.0150	2.1981	1.6645
D to Z ↑	0.0131	0.0133	1.3273	0.9833

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P10	1.146e-05	1.000e-20
X12_P10	1.630e-05	1.000e-20
X18_P10	2.636e-05	1.000e-20
X24_P10	2.845e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	6.834e-04	1.158e-03	1.756e-03	2.079e-03
B (output stable)	5.883e-04	1.041e-03	1.506e-03	1.857e-03
C (output stable)	3.234e-05	1.104e-04	1.628e-04	2.342e-04
D (output stable)	9.211e-05	4.106e-04	4.777e-04	7.534e-04
A to Z	2.881e-03	5.490e-03	8.056e-03	1.054e-02
B to Z	2.634e-03	5.113e-03	7.273e-03	9.784e-03
C to Z	1.080e-03	2.164e-03	3.066e-03	4.359e-03
D to Z	9.011e-04	1.584e-03	2.396e-03	3.298e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

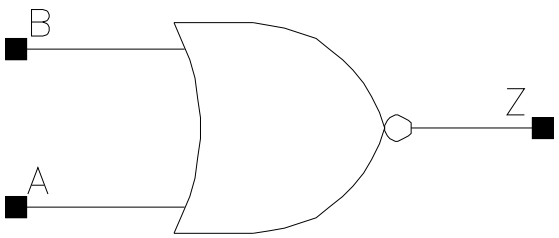
Pin Cycle (vdds)	X6_P10	X12_P10	X18_P10	X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.408	0.4896
X5_P10	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X10_P10	1.200	0.680	0.8160
X14_P10	1.200	0.680	0.8160
X17_P10	1.200	0.952	1.1424
X21_P10	1.200	0.952	1.1424
X24_P10	1.200	1.224	1.4688
X27_P10	1.200	1.224	1.4688
X34_P10	1.200	1.496	1.7952
X40_P10	1.200	1.360	1.6320
X41_P10	1.200	1.768	2.1216
X49_P10	1.200	1.496	1.7952
X53_P10	1.200	1.904	2.2848
X55_P10	1.200	2.312	2.7744
X57_P10	1.200	1.904	2.2848
X65_P10	1.200	2.040	2.4480
X84_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P10	X5_P10	X7_P10	X10_P10
A	0.0005	0.0007	0.0008	0.0013
B	0.0005	0.0006	0.0008	0.0012
	X14_P10	X17_P10	X21_P10	X24_P10

A	0.0017	0.0021	0.0025	0.0029
B	0.0015	0.0019	0.0023	0.0027
	X27_P10	X34_P10	X40_P10	X41_P10
A	0.0032	0.0041	0.0010	0.0050
B	0.0030	0.0037	0.0011	0.0045
	X49_P10	X53_P10	X55_P10	X57_P10
A	0.0010	0.0010	0.0066	0.0010
B	0.0011	0.0009	0.0060	0.0009
	X65_P10	X84_P10		
A	0.0010	0.0012		
B	0.0009	0.0010		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X5_P10**	**X3_P10**	**X5_P10**
A to Z ↓	0.0110	0.0104	4.7751	3.4209
A to Z ↑	0.0196	0.0179	14.3360	10.3528
B to Z ↓	0.0098	0.0089	4.8612	3.4424
B to Z ↑	0.0194	0.0174	14.3975	10.3853
	X7_P10	**X10_P10**	**X7_P10**	**X10_P10**
A to Z ↓	0.0102	0.0106	2.4963	1.6308
A to Z ↑	0.0166	0.0193	7.2524	4.8530
B to Z ↓	0.0086	0.0078	2.5238	1.6443
B to Z ↑	0.0160	0.0149	7.2781	4.8776
	X14_P10	**X17_P10**	**X14_P10**	**X17_P10**
A to Z ↓	0.0104	0.0105	1.2336	0.9952
A to Z ↑	0.0178	0.0180	3.5772	2.9010
B to Z ↓	0.0076	0.0083	1.2445	1.0036
B to Z ↑	0.0140	0.0153	3.5937	2.9126
	X21_P10	**X24_P10**	**X21_P10**	**X24_P10**
A to Z ↓	0.0104	0.0103	0.8417	0.7190
A to Z ↑	0.0172	0.0175	2.4017	2.0969
B to Z ↓	0.0083	0.0078	0.8484	0.7256
B to Z ↑	0.0148	0.0144	2.4116	2.1057
	X27_P10	**X34_P10**	**X27_P10**	**X34_P10**
A to Z ↓	0.0102	0.0106	0.6365	0.5135
A to Z ↑	0.0168	0.0172	1.8354	1.4626
B to Z ↓	0.0077	0.0082	0.6428	0.5180
B to Z ↑	0.0139	0.0146	1.8436	1.4687
	X40_P10	**X41_P10**	**X40_P10**	**X41_P10**
A to Z ↓	0.0390	0.0103	0.5165	0.4281
A to Z ↑	0.0530	0.0168	0.7899	1.2132
B to Z ↓	0.0374	0.0078	0.5165	0.4324
B to Z ↑	0.0535	0.0138	0.7901	1.2186
	X49_P10	**X53_P10**	**X49_P10**	**X53_P10**
A to Z ↓	0.0407	0.0421	0.4296	0.3944
A to Z ↑	0.0544	0.0619	0.6571	0.6072
B to Z ↓	0.0392	0.0406	0.4301	0.3945
B to Z ↑	0.0549	0.0619	0.6576	0.6071
	X55_P10	**X57_P10**	**X55_P10**	**X57_P10**
A to Z ↓	0.0104	0.0424	0.3233	0.3700
A to Z ↑	0.0169	0.0621	0.9134	0.5648

B to Z ↓	0.0078	0.0409	0.3270	0.3702
B to Z ↑	0.0138	0.0622	0.9174	0.5641
	X65_P10	**X84_P10**	**X65_P10**	**X84_P10**
A to Z ↓	0.0438	0.0453	0.3247	0.2571
A to Z ↑	0.0635	0.0636	0.4948	0.3912
B to Z ↓	0.0423	0.0438	0.3249	0.2571
B to Z ↑	0.0634	0.0638	0.4948	0.3910

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	3.242e-06	1.000e-20
X5_P10	4.897e-06	1.000e-20
X7_P10	7.424e-06	1.000e-20
X10_P10	1.014e-05	1.000e-20
X14_P10	1.453e-05	1.000e-20
X17_P10	1.707e-05	1.000e-20
X21_P10	2.118e-05	1.000e-20
X24_P10	2.399e-05	1.000e-20
X27_P10	2.784e-05	1.000e-20
X34_P10	3.451e-05	1.000e-20
X40_P10	5.254e-05	1.000e-20
X41_P10	4.117e-05	1.000e-20
X49_P10	5.937e-05	1.000e-20
X53_P10	6.898e-05	1.000e-20
X55_P10	5.451e-05	1.000e-20
X57_P10	7.331e-05	1.000e-20
X65_P10	8.015e-05	1.000e-20
X84_P10	9.472e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	1.486e-05	1.984e-05	2.746e-05	8.697e-05
B (output stable)	2.556e-05	3.388e-05	4.750e-05	2.043e-04
A to Z	5.689e-04	7.026e-04	9.400e-04	1.634e-03
B to Z	4.459e-04	5.372e-04	7.039e-04	9.712e-04
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	1.020e-04	1.191e-04	1.337e-04	1.646e-04
B (output stable)	2.553e-04	2.600e-04	2.643e-04	3.701e-04
A to Z	2.034e-03	2.536e-03	2.918e-03	3.445e-03
B to Z	1.238e-03	1.688e-03	1.956e-03	2.198e-03
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	1.763e-04	2.168e-04	2.792e-05	2.737e-04
B (output stable)	3.849e-04	4.196e-04	4.759e-05	5.675e-04
A to Z	3.733e-03	4.807e-03	9.102e-03	5.660e-03
B to Z	2.401e-03	3.214e-03	8.869e-03	3.596e-03
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	2.806e-05	2.903e-05	3.659e-04	2.898e-05
B (output stable)	4.754e-05	5.074e-05	7.469e-04	5.080e-05
A to Z	1.027e-02	1.265e-02	7.480e-03	1.308e-02
B to Z	1.004e-02	1.240e-02	4.741e-03	1.283e-02
	X65_P10	X84_P10		

A (output stable)	2.908e-05	3.015e-05		
B (output stable)	5.084e-05	5.184e-05		
A to Z	1.429e-02	1.674e-02		
B to Z	1.404e-02	1.643e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

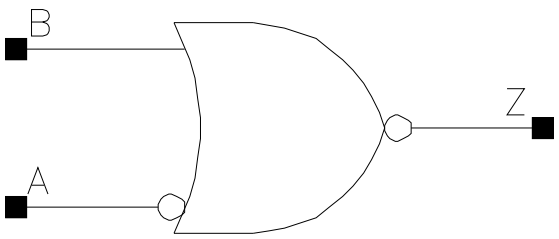
Pin Cycle (vdds)	X3_P10	X5_P10	X7_P10	X10_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P10	X17_P10	X21_P10	X24_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P10	X34_P10	X40_P10	X41_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P10	X53_P10	X55_P10	X57_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P10	X84_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X7_P10	1.200	0.680	0.8160
X13_P10	1.200	0.952	1.1424
X27_P10	1.200	1.632	1.9584
X41_P10	1.200	2.312	2.7744
X55_P10	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X7_P10	X13_P10
A	0.0008	0.0008	0.0008	0.0011
B	0.0005	0.0008	0.0008	0.0015
	X27_P10	X41_P10	X55_P10	
A	0.0021	0.0030	0.0040	
B	0.0030	0.0045	0.0060	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0297	0.0330	4.6454	2.9890
A to Z ↑	0.0287	0.0286	14.2375	7.2167
B to Z ↓	0.0101	0.0100	4.8453	3.1416
B to Z ↑	0.0196	0.0159	14.3754	7.2936

	X7_P10	X13_P10	X7_P10	X13_P10
A to Z ↓	0.0335	0.0294	2.3550	1.2768
A to Z ↑	0.0314	0.0292	7.1084	3.7527
B to Z ↓	0.0091	0.0081	2.4054	1.2995
B to Z ↑	0.0174	0.0153	7.1630	3.7872
	X27_P10	**X41_P10**	**X27_P10**	**X41_P10**
A to Z ↓	0.0284	0.0290	0.6149	0.4159
A to Z ↑	0.0280	0.0283	1.8024	1.2082
B to Z ↓	0.0079	0.0079	0.6429	0.4336
B to Z ↑	0.0145	0.0143	1.8200	1.2197
	X55_P10		**X55_P10**	
A to Z ↓	0.0284		0.3144	
A to Z ↑	0.0277		0.9102	
B to Z ↓	0.0078		0.3285	
B to Z ↑	0.0139		0.9193	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	6.032e-06	1.000e-20
X6_P10	9.778e-06	1.000e-20
X7_P10	1.116e-05	1.000e-20
X13_P10	2.134e-05	1.000e-20
X27_P10	4.164e-05	1.000e-20
X41_P10	6.111e-05	1.000e-20
X55_P10	8.057e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	8.462e-04	1.059e-03	1.133e-03	1.826e-03
B (output stable)	2.565e-05	4.736e-05	1.275e-04	2.256e-04
A to Z	1.463e-03	2.030e-03	2.373e-03	3.961e-03
B to Z	4.550e-04	6.837e-04	8.414e-04	1.345e-03
	X27_P10	X41_P10	X55_P10	
A (output stable)	3.569e-03	5.432e-03	7.042e-03	
B (output stable)	4.289e-04	5.812e-04	7.507e-04	
A to Z	7.815e-03	1.164e-02	1.510e-02	
B to Z	2.602e-03	3.797e-03	4.891e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

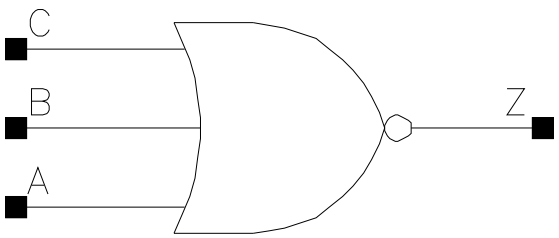
Pin Cycle (vdds)	X3_P10	X6_P10	X7_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P10	X41_P10	X55_P10	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	0.544	0.6528
X6_P10	1.200	0.544	0.6528
X9_P10	1.200	0.952	1.1424
X13_P10	1.200	0.952	1.1424
X16_P10	1.200	1.360	1.6320
X19_P10	1.200	1.496	1.7952
X22_P10	1.200	1.768	2.1216
X25_P10	1.200	1.904	2.2848
X37_P10	1.200	2.584	3.1008
X49_P10	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P10	X6_P10	X9_P10	X13_P10
A	0.0007	0.0008	0.0013	0.0016
B	0.0007	0.0008	0.0014	0.0017
C	0.0007	0.0008	0.0012	0.0015
	X16_P10	X19_P10	X22_P10	X25_P10
A	0.0021	0.0025	0.0029	0.0033
B	0.0021	0.0028	0.0031	0.0038
C	0.0019	0.0022	0.0026	0.0029
	X37_P10	X49_P10		
A	0.0049	0.0066		
B	0.0050	0.0067		

C	0.0043	0.0059		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0127	0.0122	3.4614	2.5300
A to Z ↑	0.0273	0.0247	15.1786	10.6232
B to Z ↓	0.0120	0.0114	3.4659	2.5307
B to Z ↑	0.0255	0.0229	15.1915	10.6300
C to Z ↓	0.0106	0.0099	3.4872	2.5530
C to Z ↑	0.0238	0.0209	15.2189	10.6478
	X9_P10	**X13_P10**	**X9_P10**	**X13_P10**
A to Z ↓	0.0124	0.0122	1.6765	1.2790
A to Z ↑	0.0275	0.0254	7.0991	5.2462
B to Z ↓	0.0118	0.0113	1.6395	1.2331
B to Z ↑	0.0271	0.0243	7.1074	5.2514
C to Z ↓	0.0091	0.0086	1.6491	1.2501
C to Z ↑	0.0194	0.0177	7.1148	5.2571
	X16_P10	**X19_P10**	**X16_P10**	**X19_P10**
A to Z ↓	0.0124	0.0122	1.0018	0.8394
A to Z ↑	0.0262	0.0256	4.2612	3.5079
B to Z ↓	0.0119	0.0117	1.0042	0.8242
B to Z ↑	0.0251	0.0253	4.2636	3.5103
C to Z ↓	0.0095	0.0093	1.0057	0.8526
C to Z ↑	0.0202	0.0190	4.2702	3.5160
	X22_P10	**X25_P10**	**X22_P10**	**X25_P10**
A to Z ↓	0.0122	0.0121	0.7316	0.6391
A to Z ↑	0.0256	0.0255	3.0374	2.6369
B to Z ↓	0.0115	0.0114	0.7206	0.6186
B to Z ↑	0.0246	0.0251	3.0409	2.6394
C to Z ↓	0.0088	0.0088	0.7258	0.6398
C to Z ↑	0.0183	0.0178	3.0446	2.6428
	X37_P10	**X49_P10**	**X37_P10**	**X49_P10**
A to Z ↓	0.0122	0.0124	0.4403	0.3327
A to Z ↑	0.0247	0.0248	1.7652	1.3283
B to Z ↓	0.0115	0.0116	0.4362	0.3299
B to Z ↑	0.0235	0.0235	1.7670	1.3294
C to Z ↓	0.0091	0.0093	0.4404	0.3333
C to Z ↑	0.0179	0.0182	1.7696	1.3319

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.911e-06	1.000e-20
X6_P10	6.039e-06	1.000e-20
X9_P10	8.241e-06	1.000e-20
X13_P10	1.202e-05	1.000e-20
X16_P10	1.403e-05	1.000e-20
X19_P10	1.816e-05	1.000e-20
X22_P10	1.985e-05	1.000e-20
X25_P10	2.390e-05	1.000e-20
X37_P10	3.481e-05	1.000e-20

X49_P10	4.622e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	2.291e-05	3.157e-05	5.796e-05	7.552e-05
B (output stable)	1.736e-05	2.732e-05	5.856e-05	7.762e-05
C (output stable)	4.979e-05	7.717e-05	1.827e-04	2.469e-04
A to Z	1.028e-03	1.320e-03	2.219e-03	2.747e-03
B to Z	8.424e-04	1.063e-03	1.879e-03	2.260e-03
C to Z	6.711e-04	8.180e-04	1.162e-03	1.410e-03
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	9.016e-05	1.087e-04	1.308e-04	1.506e-04
B (output stable)	8.724e-05	1.180e-04	1.313e-04	1.603e-04
C (output stable)	2.570e-04	3.465e-04	3.998e-04	4.860e-04
A to Z	3.498e-03	4.159e-03	4.779e-03	5.498e-03
B to Z	2.891e-03	3.496e-03	3.946e-03	4.597e-03
C to Z	2.017e-03	2.284e-03	2.525e-03	2.833e-03
	X37_P10	X49_P10		
A (output stable)	2.200e-04	2.942e-04		
B (output stable)	2.203e-04	2.907e-04		
C (output stable)	6.690e-04	8.791e-04		
A to Z	7.940e-03	1.062e-02		
B to Z	6.467e-03	8.628e-03		
C to Z	4.161e-03	5.614e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

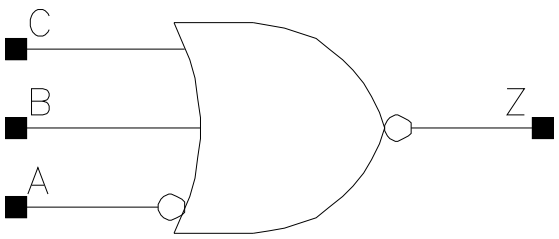
Pin Cycle (vdds)	X4_P10	X6_P10	X9_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P10	X19_P10	X22_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P10	X49_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.680	0.8160
X13_P10	1.200	1.224	1.4688
X19_P10	1.200	1.496	1.7952
X25_P10	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0008	0.0011	0.0011	0.0021
B	0.0008	0.0017	0.0024	0.0033
C	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X13_P10**	**X6_P10**	**X13_P10**
A to Z ↓	0.0333	0.0311	2.4652	1.3415
A to Z ↑	0.0374	0.0365	10.7268	5.2380
B to Z ↓	0.0115	0.0113	2.5442	1.2390
B to Z ↑	0.0233	0.0242	10.7634	5.2517
C to Z ↓	0.0100	0.0086	2.5557	1.2511
C to Z ↑	0.0213	0.0176	10.7778	5.2574
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0357	0.0311	0.8323	0.6300

A to Z ↑	0.0396	0.0364	3.5177	2.6391
B to Z ↓	0.0117	0.0113	0.8570	0.6398
B to Z ↑	0.0235	0.0235	3.5284	2.6458
C to Z ↓	0.0092	0.0088	0.8537	0.6429
C to Z ↑	0.0190	0.0180	3.5332	2.6507

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P10	8.938e-06	1.000e-20
X13_P10	1.954e-05	1.000e-20
X19_P10	2.449e-05	1.000e-20
X25_P10	3.762e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	1.094e-03	1.943e-03	2.544e-03	3.829e-03
B (output stable)	2.923e-05	8.460e-05	1.143e-04	1.606e-04
C (output stable)	7.922e-05	2.751e-04	3.265e-04	4.907e-04
A to Z	2.489e-03	4.923e-03	6.776e-03	9.547e-03
B to Z	1.073e-03	2.260e-03	3.262e-03	4.340e-03
C to Z	8.318e-04	1.398e-03	2.268e-03	2.837e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

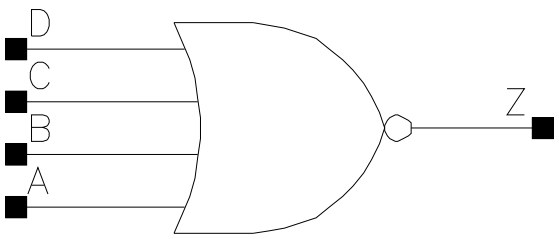
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X25_P10	1.200	1.904	2.2848
X32_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X32_P10
A	0.0007	0.0007	0.0008	0.0009
B	0.0007	0.0007	0.0009	0.0012
C	0.0006	0.0006	0.0008	0.0009
D	0.0006	0.0006	0.0008	0.0009

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0410	0.0403	2.4278	1.1917
A to Z ↑	0.0594	0.0634	3.9312	1.9305
B to Z ↓	0.0394	0.0391	2.4279	1.1918
B to Z ↑	0.0593	0.0636	3.9283	1.9308
C to Z ↓	0.0403	0.0403	2.4223	1.1896
C to Z ↑	0.0603	0.0652	3.9320	1.9285

D to Z ↓	0.0396	0.0396	2.4231	1.1891
D to Z ↑	0.0608	0.0659	3.9292	1.9278
	X25_P10	**X32_P10**	**X25_P10**	**X32_P10**
A to Z ↓	0.0413	0.0434	0.8245	0.6501
A to Z ↑	0.0618	0.0596	1.3127	0.9994
B to Z ↓	0.0402	0.0420	0.8240	0.6503
B to Z ↑	0.0623	0.0598	1.3128	0.9994
C to Z ↓	0.0398	0.0427	0.8206	0.6482
C to Z ↑	0.0612	0.0599	1.3109	0.9988
D to Z ↓	0.0385	0.0405	0.8210	0.6480
D to Z ↑	0.0615	0.0598	1.3118	0.9977

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.550e-05	1.000e-20
X17_P10	2.541e-05	1.000e-20
X25_P10	3.891e-05	1.000e-20
X32_P10	5.074e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	4.308e-04	5.310e-04	7.408e-04	9.390e-04
B (output stable)	3.816e-04	4.823e-04	6.758e-04	8.465e-04
C (output stable)	4.029e-04	4.826e-04	7.377e-04	9.455e-04
D (output stable)	3.553e-04	4.380e-04	6.692e-04	8.510e-04
A to Z	3.078e-03	4.737e-03	7.189e-03	9.016e-03
B to Z	2.947e-03	4.615e-03	7.007e-03	8.795e-03
C to Z	3.119e-03	4.742e-03	6.770e-03	8.543e-03
D to Z	2.985e-03	4.619e-03	6.600e-03	8.299e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

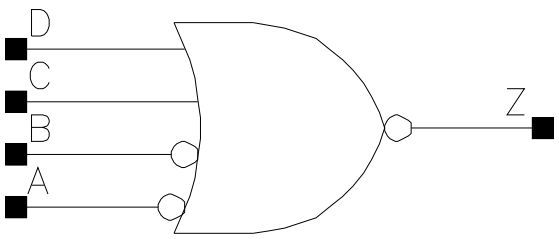
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X32_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X13_P10	1.200	1.496	1.7952
X19_P10	1.200	2.040	2.4480
X25_P10	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P10	X13_P10	X19_P10	X25_P10
A	0.0011	0.0011	0.0020	0.0020
B	0.0011	0.0015	0.0020	0.0021
C	0.0008	0.0016	0.0024	0.0031
D	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	X13_P10	X6_P10	X13_P10
A to Z ↓	0.0283	0.0356	2.4063	1.2017
A to Z ↑	0.0372	0.0462	10.3266	5.3040
B to Z ↓	0.0263	0.0341	2.4045	1.2002
B to Z ↑	0.0379	0.0473	10.3292	5.3040
C to Z ↓	0.0120	0.0113	2.5626	1.2376
C to Z ↑	0.0234	0.0243	10.3633	5.3193

D to Z ↓	0.0101	0.0087	2.5568	1.2472
D to Z ↑	0.0210	0.0182	10.3727	5.3257
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0312	0.0341	0.8225	0.6202
A to Z ↑	0.0415	0.0448	3.5202	2.6560
B to Z ↓	0.0283	0.0318	0.8210	0.6191
B to Z ↑	0.0414	0.0454	3.5203	2.6561
C to Z ↓	0.0118	0.0115	0.8579	0.6435
C to Z ↑	0.0235	0.0234	3.5301	2.6621
D to Z ↓	0.0092	0.0088	0.8542	0.6429
D to Z ↑	0.0190	0.0178	3.5344	2.6665

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P10	1.205e-05	1.000e-20
X13_P10	1.729e-05	1.000e-20
X19_P10	2.825e-05	1.000e-20
X25_P10	3.275e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	6.653e-04	1.130e-03	1.706e-03	2.050e-03
B (output stable)	5.987e-04	1.052e-03	1.524e-03	1.903e-03
C (output stable)	3.123e-05	9.429e-05	1.322e-04	1.817e-04
D (output stable)	9.451e-05	2.766e-04	3.606e-04	5.370e-04
A to Z	2.979e-03	5.630e-03	8.373e-03	1.074e-02
B to Z	2.802e-03	5.337e-03	7.750e-03	1.018e-02
C to Z	1.117e-03	2.254e-03	3.251e-03	4.288e-03
D to Z	8.632e-04	1.434e-03	2.269e-03	2.783e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

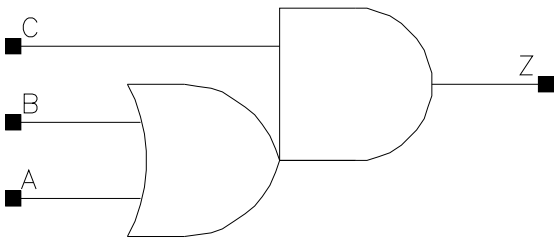
Pin Cycle (vdds)	X6_P10	X13_P10	X19_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.680	0.8160
X17_P10	1.200	0.816	0.9792
X33_P10	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0010	0.0010	0.0018
B	0.0011	0.0011	0.0021
C	0.0011	0.0011	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
A to Z ↓	0.0314	0.0365	2.4930	1.2399
A to Z ↑	0.0277	0.0307	3.9415	1.9344
B to Z ↓	0.0312	0.0367	2.4942	1.2392
B to Z ↑	0.0252	0.0285	3.9309	1.9310
C to Z ↓	0.0283	0.0313	2.4702	1.2206
C to Z ↑	0.0264	0.0290	3.9347	1.9295
	X33_P10		**X33_P10**	
A to Z ↓	0.0384		0.6285	
A to Z ↑	0.0331		0.9710	

B to Z ↓	0.0386		0.6285	
B to Z ↑	0.0304		0.9694	
C to Z ↓	0.0321		0.6173	
C to Z ↑	0.0302		0.9694	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.537e-05	1.000e-20
X17_P10	2.266e-05	1.000e-20
X33_P10	4.508e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	6.133e-05	6.265e-05	1.281e-04
B (output stable)	7.201e-05	7.340e-05	1.409e-04
C (output stable)	5.069e-05	5.266e-05	9.913e-05
A to Z	2.314e-03	3.475e-03	7.369e-03
B to Z	2.065e-03	3.217e-03	6.864e-03
C to Z	2.533e-03	3.613e-03	7.520e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

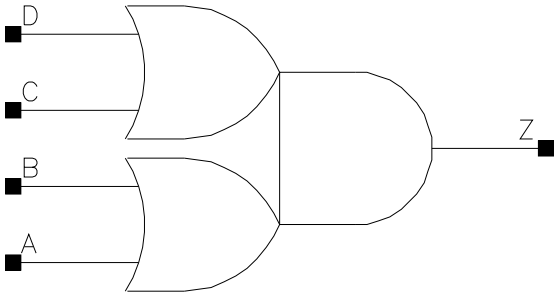
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X17_P10	1.200	1.088	1.3056
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0006	0.0010	0.0019
B	0.0007	0.0010	0.0019
C	0.0007	0.0010	0.0019
D	0.0006	0.0010	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0548	0.0456	2.4283	1.2301
A to Z ↑	0.0385	0.0335	3.8628	1.9313
B to Z ↓	0.0554	0.0459	2.4290	1.2302
B to Z ↑	0.0370	0.0316	3.8568	1.9286

C to Z ↓	0.0477	0.0401	2.4086	1.2234
C to Z ↑	0.0370	0.0331	3.8598	1.9282
D to Z ↓	0.0473	0.0400	2.4097	1.2230
D to Z ↑	0.0348	0.0306	3.8568	1.9266
	X33_P10		**X33_P10**	
A to Z ↓	0.0462		0.6325	
A to Z ↑	0.0334		0.9695	
B to Z ↓	0.0446		0.6333	
B to Z ↑	0.0309		0.9676	
C to Z ↓	0.0400		0.6288	
C to Z ↑	0.0325		0.9683	
D to Z ↓	0.0379		0.6290	
D to Z ↑	0.0295		0.9664	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.193e-05	1.000e-20
X17_P10	2.515e-05	1.000e-20
X33_P10	4.810e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.721e-05	2.789e-05	8.420e-05
B (output stable)	2.273e-05	3.907e-05	1.859e-04
C (output stable)	5.682e-05	6.804e-05	1.613e-04
D (output stable)	6.262e-05	7.963e-05	2.646e-04
A to Z	2.775e-03	4.491e-03	8.867e-03
B to Z	2.640e-03	4.216e-03	8.089e-03
C to Z	2.403e-03	3.970e-03	7.777e-03
D to Z	2.262e-03	3.700e-03	6.968e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

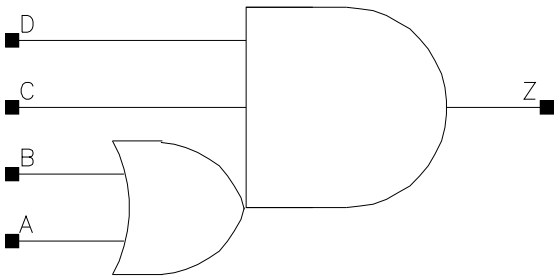
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X17_P10	1.200	1.088	1.3056
X25_P10	1.200	1.904	2.2848
X33_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P10	X17_P10	X25_P10	X33_P10
A	0.0006	0.0010	0.0016	0.0019
B	0.0006	0.0010	0.0016	0.0019
C	0.0007	0.0010	0.0017	0.0020
D	0.0006	0.0010	0.0016	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0463	0.0425	2.5475	1.2409
A to Z ↑	0.0451	0.0415	4.0090	1.9398
B to Z ↓	0.0467	0.0416	2.5509	1.2424
B to Z ↑	0.0426	0.0379	4.0014	1.9367
C to Z ↓	0.0383	0.0350	2.4918	1.2196

C to Z ↑	0.0428	0.0390	3.9996	1.9345
D to Z ↓	0.0372	0.0338	2.4922	1.2179
D to Z ↑	0.0441	0.0401	3.9973	1.9364
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**
A to Z ↓	0.0449	0.0424	0.8416	0.6309
A to Z ↑	0.0426	0.0426	1.3115	0.9843
B to Z ↓	0.0434	0.0409	0.8412	0.6309
B to Z ↑	0.0391	0.0386	1.3087	0.9804
C to Z ↓	0.0370	0.0349	0.8259	0.6192
C to Z ↑	0.0405	0.0397	1.3077	0.9808
D to Z ↓	0.0351	0.0333	0.8243	0.6183
D to Z ↑	0.0403	0.0399	1.3094	0.9813

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.028e-05	1.000e-20
X17_P10	2.220e-05	1.000e-20
X25_P10	3.341e-05	1.000e-20
X33_P10	4.410e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	5.817e-05	1.109e-04	1.851e-04	2.000e-04
B (output stable)	6.008e-05	1.230e-04	2.079e-04	2.253e-04
C (output stable)	1.377e-05	2.889e-05	7.224e-05	7.926e-05
D (output stable)	2.329e-05	4.714e-05	1.609e-04	1.688e-04
A to Z	2.326e-03	4.131e-03	6.715e-03	8.250e-03
B to Z	2.197e-03	3.811e-03	6.122e-03	7.476e-03
C to Z	2.469e-03	4.350e-03	7.194e-03	8.674e-03
D to Z	2.371e-03	4.159e-03	6.700e-03	8.155e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

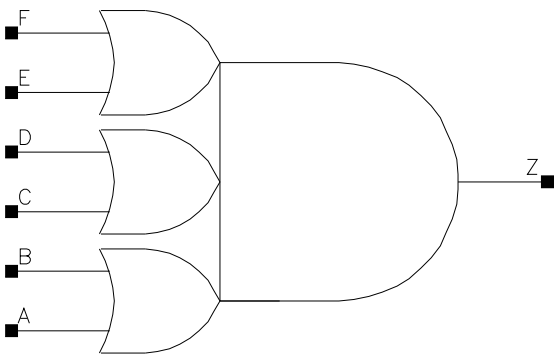
Pin Cycle (vdds)	X8_P10	X17_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	1.224	1.4688
X17_P10	1.200	1.360	1.6320
X33_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
A	0.0007	0.0009	0.0017
B	0.0006	0.0010	0.0018
C	0.0006	0.0009	0.0017
D	0.0006	0.0009	0.0018
E	0.0006	0.0010	0.0017
F	0.0006	0.0009	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
A to Z ↓	0.0626	0.0524	2.6031	1.2627
A to Z ↑	0.0498	0.0448	3.9863	1.9497
B to Z ↓	0.0627	0.0530	2.6038	1.2628
B to Z ↑	0.0478	0.0430	3.9846	1.9504
C to Z ↓	0.0575	0.0493	2.5868	1.2592
C to Z ↑	0.0498	0.0443	3.9880	1.9512
D to Z ↓	0.0580	0.0497	2.5868	1.2597
D to Z ↑	0.0475	0.0419	3.9814	1.9494
E to Z ↓	0.0499	0.0435	2.5654	1.2520
E to Z ↑	0.0459	0.0418	3.9823	1.9497
F to Z ↓	0.0507	0.0434	2.5670	1.2522
F to Z ↑	0.0438	0.0391	3.9789	1.9468
	X33_P10		X33_P10	
A to Z ↓	0.0526		0.6440	
A to Z ↑	0.0457		0.9834	
B to Z ↓	0.0533		0.6439	
B to Z ↑	0.0428		0.9809	
C to Z ↓	0.0484		0.6401	
C to Z ↑	0.0450		0.9831	
D to Z ↓	0.0490		0.6402	
D to Z ↑	0.0422		0.9808	
E to Z ↓	0.0426		0.6363	
E to Z ↑	0.0425		0.9823	
F to Z ↓	0.0431		0.6365	
F to Z ↑	0.0395		0.9800	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.235e-05	1.000e-20
X17_P10	2.665e-05	1.000e-20
X33_P10	5.082e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X17_P10	X33_P10
A (output stable)	1.522e-05	2.681e-05	5.038e-05
B (output stable)	1.914e-05	3.752e-05	6.666e-05
C (output stable)	2.739e-05	4.375e-05	8.890e-05
D (output stable)	3.275e-05	5.254e-05	1.054e-04
E (output stable)	9.643e-05	1.359e-04	2.588e-04
F (output stable)	9.766e-05	1.410e-04	2.731e-04
A to Z	3.193e-03	5.298e-03	1.035e-02
B to Z	3.048e-03	5.039e-03	9.824e-03
C to Z	2.912e-03	4.893e-03	9.474e-03
D to Z	2.777e-03	4.624e-03	8.952e-03
E to Z	2.555e-03	4.370e-03	8.448e-03
F to Z	2.432e-03	4.100e-03	7.949e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

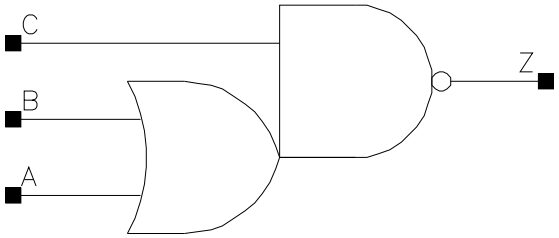
Pin Cycle (vdds)	X8_P10	X17_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.544	0.6528
X17_P10	1.200	1.360	1.6320
X34_P10	1.200	2.720	3.2640
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P10	X17_P10	X34_P10	X46_P10
A	0.0008	0.0023	0.0047	0.0062
B	0.0008	0.0022	0.0043	0.0057
C	0.0008	0.0024	0.0050	0.0064

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X17_P10**	**X6_P10**	**X17_P10**
A to Z ↓	0.0146	0.0151	4.6433	1.5210
A to Z ↑	0.0176	0.0187	7.2470	2.4337
B to Z ↓	0.0121	0.0124	4.5739	1.5328
B to Z ↑	0.0169	0.0166	7.2731	2.4451
C to Z ↓	0.0140	0.0140	4.2316	1.3984
C to Z ↑	0.0171	0.0167	3.9597	1.3063
	X34_P10	**X46_P10**	**X34_P10**	**X46_P10**
A to Z ↓	0.0159	0.0158	0.7733	0.5884

A to Z ↑	0.0197	0.0193	1.2148	0.9275
B to Z ↓	0.0128	0.0129	0.7810	0.5961
B to Z ↑	0.0171	0.0171	1.2201	0.9322
C to Z ↓	0.0147	0.0144	0.7121	0.5429
C to Z ↑	0.0172	0.0170	0.6530	0.4967

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P10	8.783e-06	1.000e-20
X17_P10	2.555e-05	1.000e-20
X34_P10	5.081e-05	1.000e-20
X46_P10	6.699e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	5.018e-05	1.821e-04	3.966e-04	4.739e-04
B (output stable)	6.122e-05	2.224e-04	5.185e-04	6.002e-04
C (output stable)	4.543e-05	1.537e-04	3.215e-04	4.026e-04
A to Z	1.012e-03	3.234e-03	6.909e-03	8.882e-03
B to Z	7.738e-04	2.283e-03	4.833e-03	6.293e-03
C to Z	1.235e-03	3.744e-03	7.863e-03	1.014e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

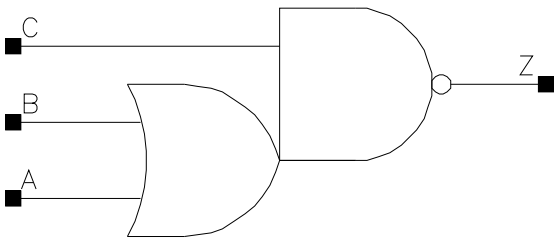
Pin Cycle (vdds)	X6_P10	X17_P10	X34_P10	X46_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.544	0.6528
X11_P10	1.200	0.952	1.1424
X17_P10	1.200	1.360	1.6320
X23_P10	1.200	1.904	2.2848
X46_P10	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P10	X11_P10	X17_P10	X23_P10
A	0.0008	0.0016	0.0025	0.0034
B	0.0008	0.0017	0.0023	0.0031
C	0.0008	0.0016	0.0023	0.0031
	X46_P10			
A	0.0068			
B	0.0061			
C	0.0062			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X11_P10	X5_P10	X11_P10
A to Z ↓	0.0155	0.0157	4.7383	2.2113
A to Z ↑	0.0224	0.0223	7.6314	3.5852
B to Z ↓	0.0133	0.0134	4.6779	2.1650

B to Z ↑	0.0219	0.0218	7.6552	3.5966
C to Z ↓	0.0122	0.0122	4.4017	2.0467
C to Z ↑	0.0130	0.0128	4.2154	1.9737
	X17_P10	**X23_P10**	**X17_P10**	**X23_P10**
A to Z ↓	0.0150	0.0159	1.5231	1.1296
A to Z ↑	0.0211	0.0235	2.3791	1.8081
B to Z ↓	0.0127	0.0132	1.5210	1.1292
B to Z ↑	0.0204	0.0212	2.3865	1.8141
C to Z ↓	0.0117	0.0121	1.4240	1.0539
C to Z ↑	0.0119	0.0123	1.3144	0.9969
	X46_P10		**X46_P10**	
A to Z ↓	0.0157		0.5853	
A to Z ↑	0.0229		0.9113	
B to Z ↓	0.0129		0.5809	
B to Z ↑	0.0207		0.9147	
C to Z ↓	0.0121		0.5447	
C to Z ↑	0.0120		0.5026	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	8.447e-06	1.000e-20
X11_P10	1.764e-05	1.000e-20
X17_P10	2.591e-05	1.000e-20
X23_P10	3.493e-05	1.000e-20
X46_P10	6.754e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	1.796e-05	3.903e-05	5.669e-05	1.060e-04
B (output stable)	2.266e-05	5.320e-05	7.532e-05	1.893e-04
C (output stable)	1.626e-04	3.862e-04	4.431e-04	7.229e-04
A to Z	1.304e-03	2.774e-03	3.855e-03	5.805e-03
B to Z	1.043e-03	2.241e-03	3.012e-03	4.296e-03
C to Z	7.890e-04	1.723e-03	2.353e-03	3.404e-03
	X46_P10			
A (output stable)	1.978e-04			
B (output stable)	3.461e-04			
C (output stable)	1.312e-03			
A to Z	1.115e-02			
B to Z	8.182e-03			
C to Z	6.515e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X5_P10	X11_P10	X17_P10	X23_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

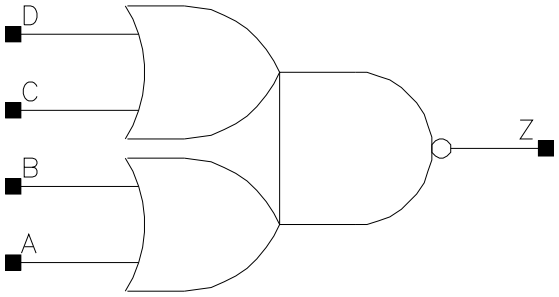
	X46_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.680	0.8160
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.448	2.9376
X42_P10	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0009	0.0017	0.0024	0.0034
B	0.0008	0.0015	0.0022	0.0030
C	0.0008	0.0016	0.0023	0.0032
D	0.0008	0.0014	0.0021	0.0029
	X42_P10			
A	0.0067			
B	0.0061			
C	0.0063			
D	0.0058			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0170	0.0183	4.2992	2.1600
A to Z ↑	0.0261	0.0265	7.9917	3.6727
B to Z ↓	0.0151	0.0157	4.2334	2.1634
B to Z ↑	0.0253	0.0240	8.0040	3.6848
C to Z ↓	0.0150	0.0165	4.3526	2.1722
C to Z ↑	0.0188	0.0205	7.8515	3.6802
D to Z ↓	0.0127	0.0132	4.2714	2.1821
D to Z ↑	0.0179	0.0169	7.8755	3.6993
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0174	0.0177	1.4752	1.0589
A to Z ↑	0.0247	0.0256	2.4659	1.8130
B to Z ↓	0.0151	0.0151	1.4820	1.0578
B to Z ↑	0.0229	0.0235	2.4745	1.8193
C to Z ↓	0.0157	0.0159	1.4855	1.0662
C to Z ↑	0.0187	0.0193	2.4727	1.8148
D to Z ↓	0.0130	0.0129	1.5026	1.0692
D to Z ↑	0.0162	0.0164	2.4855	1.8244
	X42_P10		**X42_P10**	
A to Z ↓	0.0179		0.5503	
A to Z ↑	0.0255		0.9195	
B to Z ↓	0.0152		0.5459	
B to Z ↑	0.0234		0.9226	
C to Z ↓	0.0164		0.5560	
C to Z ↑	0.0193		0.9160	
D to Z ↓	0.0132		0.5522	
D to Z ↑	0.0165		0.9207	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	1.014e-05	1.000e-20
X10_P10	2.146e-05	1.000e-20
X15_P10	3.078e-05	1.000e-20
X21_P10	4.227e-05	1.000e-20
X42_P10	8.273e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	2.490e-05	8.147e-05	1.056e-04	1.522e-04
B (output stable)	3.638e-05	1.806e-04	1.865e-04	3.022e-04
C (output stable)	5.522e-05	1.524e-04	1.902e-04	2.741e-04
D (output stable)	6.839e-05	2.518e-04	2.677e-04	4.195e-04
A to Z	1.574e-03	3.580e-03	4.866e-03	6.923e-03
B to Z	1.320e-03	2.791e-03	3.804e-03	5.407e-03
C to Z	1.088e-03	2.631e-03	3.493e-03	4.963e-03
D to Z	8.615e-04	1.837e-03	2.504e-03	3.519e-03
	X42_P10			
A (output stable)	2.996e-04			
B (output stable)	5.729e-04			
C (output stable)	5.391e-04			
D (output stable)	8.154e-04			

A to Z	1.362e-02			
B to Z	1.061e-02			
C to Z	9.819e-03			
D to Z	6.994e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

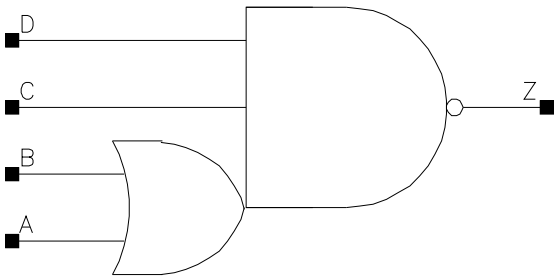
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X21_P10	1.200	2.448	2.9376
X31_P10	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X21_P10	X31_P10
A	0.0008	0.0015	0.0031	0.0046
B	0.0010	0.0014	0.0028	0.0042
C	0.0008	0.0017	0.0033	0.0049
D	0.0008	0.0016	0.0031	0.0046

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0216	0.0205	6.0913	3.2136
A to Z ↑	0.0243	0.0222	7.1975	3.6193
B to Z ↓	0.0189	0.0165	6.1240	3.2250
B to Z ↑	0.0231	0.0194	7.2384	3.6365
C to Z ↓	0.0199	0.0205	5.7541	3.0354

C to Z ↑	0.0209	0.0204	3.8469	1.9360
D to Z ↓	0.0209	0.0198	5.7709	3.0452
D to Z ↑	0.0198	0.0185	3.8827	1.9389
	X21_P10	**X31_P10**	**X21_P10**	**X31_P10**
A to Z ↓	0.0205	0.0205	1.6674	1.1288
A to Z ↑	0.0214	0.0211	1.8095	1.2129
B to Z ↓	0.0163	0.0163	1.6746	1.1365
B to Z ↑	0.0187	0.0185	1.8180	1.2193
C to Z ↓	0.0200	0.0200	1.5760	1.0679
C to Z ↑	0.0197	0.0196	0.9786	0.6582
D to Z ↓	0.0196	0.0196	1.5801	1.0708
D to Z ↑	0.0180	0.0179	0.9790	0.6574

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	7.869e-06	1.000e-20
X10_P10	1.495e-05	1.000e-20
X21_P10	2.848e-05	1.000e-20
X31_P10	4.203e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	1.058e-04	2.317e-04	4.255e-04	6.210e-04
B (output stable)	1.142e-04	2.525e-04	4.568e-04	6.770e-04
C (output stable)	2.715e-05	8.168e-05	1.535e-04	2.268e-04
D (output stable)	4.307e-05	1.731e-04	3.084e-04	4.433e-04
A to Z	1.563e-03	2.725e-03	5.180e-03	7.575e-03
B to Z	1.188e-03	1.954e-03	3.676e-03	5.393e-03
C to Z	1.853e-03	3.577e-03	6.725e-03	9.903e-03
D to Z	1.674e-03	2.991e-03	5.648e-03	8.331e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

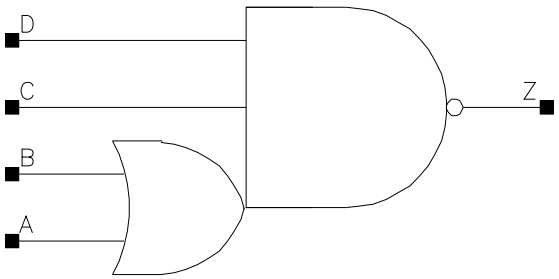
Pin Cycle (vdds)	X5_P10	X10_P10	X21_P10	X31_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.200	0.816	0.9792
X10_P10	1.200	1.360	1.6320
X15_P10	1.200	1.768	2.1216
X21_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X15_P10	X21_P10
A	0.0009	0.0017	0.0026	0.0034
B	0.0008	0.0016	0.0023	0.0031
C	0.0008	0.0016	0.0024	0.0031
D	0.0008	0.0015	0.0022	0.0030

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0206	0.0223	6.1979	3.2063
A to Z ↑	0.0260	0.0285	7.0475	3.5785
B to Z ↓	0.0179	0.0189	6.1242	3.2090
B to Z ↑	0.0256	0.0263	7.0676	3.5891
C to Z ↓	0.0161	0.0182	5.8563	3.0463

C to Z ↑	0.0162	0.0172	3.8991	1.9682
D to Z ↓	0.0162	0.0169	5.8798	3.0578
D to Z ↑	0.0143	0.0145	3.9207	1.9803
	X15_P10	**X21_P10**	**X15_P10**	**X21_P10**
A to Z ↓	0.0217	0.0220	2.1993	1.6553
A to Z ↑	0.0271	0.0278	2.4059	1.8185
B to Z ↓	0.0187	0.0186	2.1957	1.6536
B to Z ↑	0.0256	0.0261	2.4132	1.8241
C to Z ↓	0.0176	0.0181	2.0864	1.5704
C to Z ↑	0.0164	0.0168	1.3123	0.9864
D to Z ↓	0.0165	0.0170	2.0947	1.5761
D to Z ↑	0.0139	0.0142	1.3204	0.9928

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P10	7.713e-06	1.000e-20
X10_P10	1.512e-05	1.000e-20
X15_P10	2.137e-05	1.000e-20
X21_P10	2.907e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	1.586e-05	3.538e-05	5.180e-05	6.589e-05
B (output stable)	1.734e-05	5.828e-05	6.969e-05	1.032e-04
C (output stable)	4.663e-05	1.043e-04	1.555e-04	2.063e-04
D (output stable)	9.312e-05	3.265e-04	3.738e-04	5.674e-04
A to Z	1.775e-03	3.894e-03	5.472e-03	7.520e-03
B to Z	1.480e-03	3.072e-03	4.356e-03	5.940e-03
C to Z	1.170e-03	2.644e-03	3.654e-03	5.096e-03
D to Z	9.905e-04	2.116e-03	2.946e-03	4.077e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

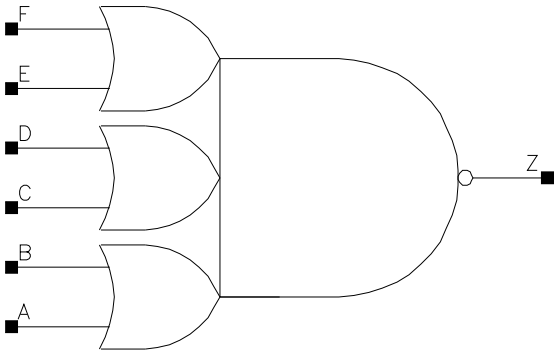
Pin Cycle (vdds)	X5_P10	X10_P10	X15_P10	X21_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	1.200	1.088	1.3056
X9_P10	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X9_P10
A	0.0007	0.0017
B	0.0007	0.0016
C	0.0007	0.0017
D	0.0006	0.0015
E	0.0007	0.0016
F	0.0006	0.0014

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X9_P10	X3_P10	X9_P10
A to Z ↓	0.0262	0.0277	7.1669	2.8970
A to Z ↑	0.0357	0.0339	9.9960	3.5992
B to Z ↓	0.0244	0.0246	7.2082	2.9001
B to Z ↑	0.0362	0.0321	10.0110	3.6073
C to Z ↓	0.0250	0.0259	7.2124	2.9093
C to Z ↑	0.0309	0.0293	10.0056	3.5914
D to Z ↓	0.0229	0.0226	7.2502	2.9151
D to Z ↑	0.0312	0.0273	10.0275	3.6013
E to Z ↓	0.0212	0.0225	7.2408	2.9100
E to Z ↑	0.0238	0.0230	10.0318	3.5948
F to Z ↓	0.0193	0.0188	7.2758	2.9153
F to Z ↑	0.0239	0.0201	10.0678	3.6112

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P10	8.812e-06	1.000e-20
X9_P10	2.532e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P10	X9_P10
A (output stable)	2.107e-05	7.659e-05
B (output stable)	2.648e-05	1.408e-04
C (output stable)	3.900e-05	1.152e-04
D (output stable)	4.374e-05	1.812e-04
E (output stable)	1.214e-04	3.035e-04
F (output stable)	1.283e-04	3.636e-04
A to Z	2.046e-03	5.399e-03
B to Z	1.851e-03	4.596e-03
C to Z	1.667e-03	4.388e-03
D to Z	1.482e-03	3.654e-03
E to Z	1.217e-03	3.368e-03
F to Z	1.049e-03	2.597e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

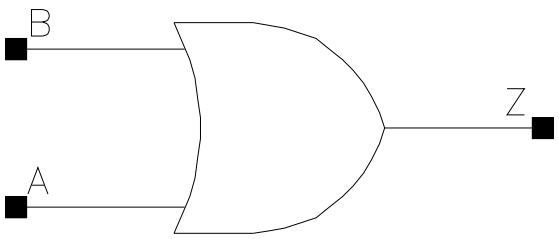
Pin Cycle (vdds)	X3_P10	X9_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.544	0.6528
X16_P10	1.200	0.680	0.8160
X33_P10	1.200	1.360	1.6320
X50_P10	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P10	X16_P10	X33_P10	X50_P10
A	0.0008	0.0010	0.0019	0.0019
B	0.0006	0.0009	0.0019	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0422	0.0366	2.5008	1.2606
A to Z ↑	0.0264	0.0273	3.9037	1.9615
B to Z ↓	0.0417	0.0364	2.5007	1.2611
B to Z ↑	0.0249	0.0255	3.9023	1.9614
	X33_P10	**X50_P10**	**X33_P10**	**X50_P10**
A to Z ↓	0.0377	0.0447	0.6212	0.4273
A to Z ↑	0.0270	0.0269	0.9570	0.6444
B to Z ↓	0.0356	0.0431	0.6222	0.4273
B to Z ↑	0.0246	0.0251	0.9555	0.6438

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	9.698e-06	1.000e-20
X16_P10	1.879e-05	1.000e-20
X33_P10	3.788e-05	1.000e-20
X50_P10	4.970e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	1.543e-05	2.893e-05	1.010e-04	9.417e-05
B (output stable)	2.812e-05	4.977e-05	2.637e-04	2.465e-04
A to Z	2.076e-03	3.387e-03	7.050e-03	9.823e-03
B to Z	1.938e-03	3.140e-03	6.259e-03	9.064e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

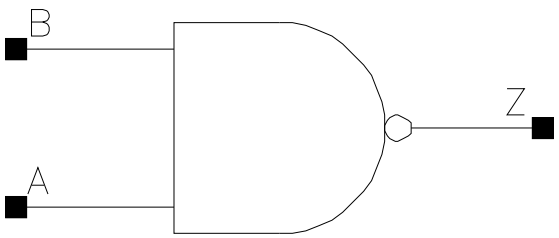
Pin Cycle (vdds)	X8_P10	X16_P10	X33_P10	X50_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.816	0.9792
X16_P10	1.200	0.952	1.1424
X24_P10	1.200	1.088	1.3056
X32_P10	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P10	X16_P10	X24_P10	X32_P10
A	0.0010	0.0010	0.0010	0.0010
B	0.0011	0.0011	0.0011	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0361	0.0374	2.4294	1.2587
A to Z ↑	0.0378	0.0385	3.9257	1.9928
B to Z ↓	0.0375	0.0389	2.4266	1.2586
B to Z ↑	0.0361	0.0364	3.9204	1.9905
	X24_P10	**X32_P10**	**X24_P10**	**X32_P10**
A to Z ↓	0.0415	0.0425	0.8513	0.6414
A to Z ↑	0.0414	0.0426	1.3314	0.9951
B to Z ↓	0.0430	0.0441	0.8514	0.6419
B to Z ↑	0.0392	0.0409	1.3313	0.9958

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	2.101e-05	1.000e-20
X16_P10	2.683e-05	1.000e-20
X24_P10	3.230e-05	1.000e-20
X32_P10	4.271e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	1.691e-05	1.699e-05	1.705e-05	1.829e-05
B (output stable)	3.205e-05	3.223e-05	3.232e-05	3.197e-05
A to Z	3.914e-03	4.542e-03	5.801e-03	7.681e-03
B to Z	3.750e-03	4.387e-03	5.658e-03	7.522e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

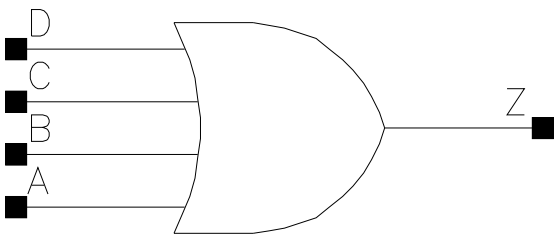
Pin Cycle (vdds)	X8_P10	X16_P10	X24_P10	X32_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P10	1.200	2.176	2.6112
X27_P10	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P10	X27_P10
A	0.0017	0.0019
B	0.0015	0.0019
C	0.0017	0.0020
D	0.0016	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P10	X27_P10	X20_P10	X27_P10
A to Z ↓	0.0424	0.0441	1.5088	1.1289
A to Z ↑	0.0283	0.0273	1.2809	0.9559
B to Z ↓	0.0409	0.0419	1.5091	1.1298
B to Z ↑	0.0266	0.0252	1.2791	0.9547
C to Z ↓	0.0407	0.0426	1.5059	1.1275
C to Z ↑	0.0267	0.0264	1.2821	0.9586
D to Z ↓	0.0392	0.0408	1.5061	1.1274
D to Z ↑	0.0250	0.0245	1.2798	0.9575

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X20_P10	3.034e-05	1.000e-20
X27_P10	4.428e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X20_P10	X27_P10
A (output stable)	1.492e-03	2.087e-03
B (output stable)	1.311e-03	1.817e-03
C (output stable)	1.330e-03	1.922e-03
D (output stable)	1.144e-03	1.697e-03
A to Z	6.409e-03	9.001e-03
B to Z	5.876e-03	8.155e-03
C to Z	5.647e-03	7.842e-03
D to Z	5.114e-03	7.096e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

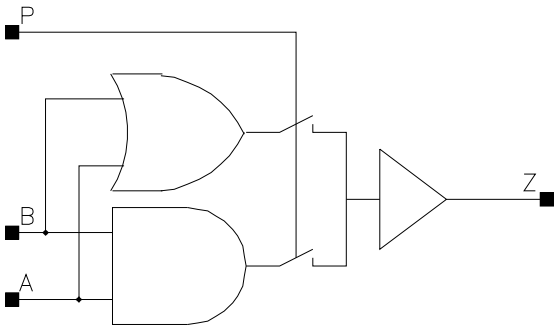
Pin Cycle (vdds)	X20_P10	X27_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	0.952	1.1424
X16_P10	1.200	1.224	1.4688
X25_P10	1.200	2.040	2.4480
X33_P10	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P10	X16_P10	X25_P10	X33_P10
A	0.0012	0.0018	0.0031	0.0032
B	0.0011	0.0018	0.0035	0.0035
P	0.0006	0.0009	0.0018	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0515	0.0461	2.5505	1.2459
A to Z ↑	0.0359	0.0335	3.9586	1.9754
B to Z ↓	0.0513	0.0461	2.5640	1.2520
B to Z ↑	0.0370	0.0345	3.9593	1.9780
P to Z ↓	0.0464	0.0422	2.5628	1.2519
P to Z ↑	0.0353	0.0331	3.9549	1.9759
	X25_P10	**X33_P10**	**X25_P10**	**X33_P10**

A to Z ↓	0.0437	0.0462	0.8446	0.6395
A to Z ↑	0.0328	0.0342	1.3262	0.9935
B to Z ↓	0.0434	0.0455	0.8492	0.6421
B to Z ↑	0.0340	0.0351	1.3268	0.9940
P to Z ↓	0.0407	0.0431	0.8489	0.6417
P to Z ↑	0.0324	0.0336	1.3237	0.9922

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	1.120e-05	1.000e-20
X16_P10	2.434e-05	1.000e-20
X25_P10	4.067e-05	1.000e-20
X33_P10	4.695e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	3.298e-05	5.309e-05	1.184e-04	1.196e-04
B (output stable)	4.356e-05	7.786e-05	2.138e-04	2.169e-04
P (output stable)	1.304e-04	2.392e-04	3.530e-04	3.635e-04
A to Z	2.422e-03	4.181e-03	7.075e-03	8.206e-03
B to Z	2.360e-03	4.086e-03	6.809e-03	7.942e-03
P to Z	2.141e-03	3.765e-03	6.399e-03	7.527e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

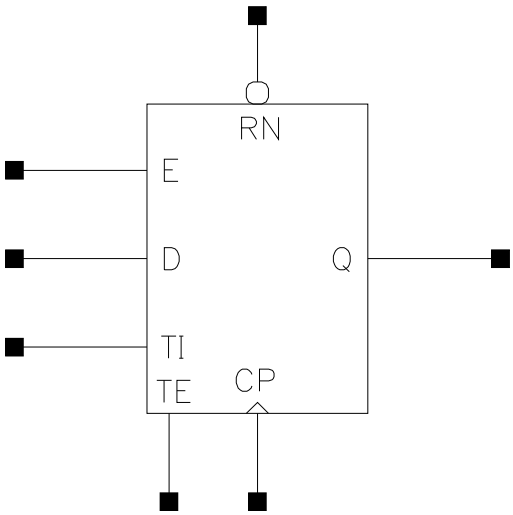
Pin Cycle (vdds)	X8_P10	X16_P10	X25_P10	X33_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.488	5.3856
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0007	0.0007	0.0008
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to Q ↓	0.1012	0.0511	5.5611	2.4688
CP to Q ↑	0.0814	0.0683	8.0922	3.9000
RN to Q ↓	0.0827	0.0712	4.8336	2.5988
	X17_P10	X33_P10	X17_P10	X33_P10
CP to Q ↓	0.0905	0.0951	1.2075	0.6309
CP to Q ↑	0.1123	0.1176	1.9138	0.9729
RN to Q ↓	0.1206	0.1251	1.2026	0.6304

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1366	0.0903	0.0903	0.0903
CP ↑	min_pulse_width to CP	0.0933	0.0407	0.0394	0.0394
D ↓	hold_rising to CP	-0.1434	-0.0706	-0.0706	-0.0706
D ↑	hold_rising to CP	-0.0870	-0.0342	-0.0342	-0.0342
D ↓	setup_rising to CP	0.1950	0.1199	0.1225	0.1221
D ↑	setup_rising to CP	0.1270	0.0688	0.0656	0.0656
E ↓	hold_rising to CP	-0.0990	-0.1043	-0.1039	-0.1039
E ↑	hold_rising to CP	-0.0874	-0.0315	-0.0315	-0.0310
E ↓	setup_rising to CP	0.1729	0.1685	0.1685	0.1685
E ↑	setup_rising to CP	0.1882	0.1296	0.1296	0.1296
RN ↓	min_pulse_width to RN	0.0876	0.0952	0.0833	0.0833
RN ↑	recovery_rising to CP	0.0222	0.0222	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0174	-0.0077	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0696	-0.0431	-0.0457	-0.0457
TE ↑	hold_rising to CP	-0.0577	-0.0386	-0.0382	-0.0382
TE ↓	setup_rising to CP	0.1246	0.0998	0.0998	0.0998
TE ↑	setup_rising to CP	0.2468	0.1763	0.1763	0.1763
TI ↓	hold_rising to CP	-0.1879	-0.1023	-0.1023	-0.1023
TI ↑	hold_rising to CP	-0.0681	-0.0397	-0.0413	-0.0413
TI ↓	setup_rising to CP	0.2421	0.1566	0.1566	0.1582
TI ↑	setup_rising to CP	0.1036	0.0759	0.0759	0.0759

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.370e-05	1.000e-20
X8_P10	3.870e-05	1.000e-20
X17_P10	4.965e-05	1.000e-20
X33_P10	6.514e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

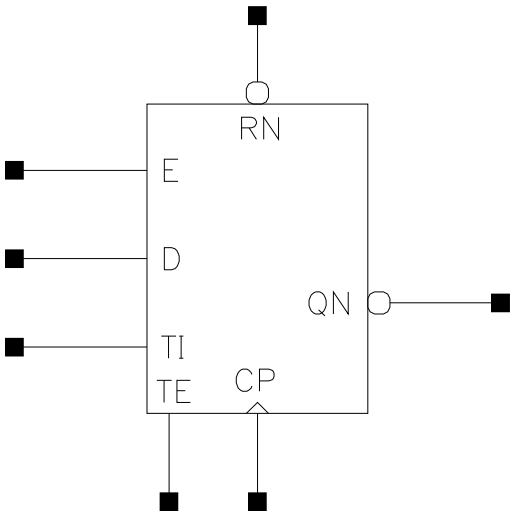
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	7.188e-03	7.240e-03	7.253e-03	7.260e-03
Clock 100Mhz Data 25Mhz	7.796e-03	7.876e-03	8.469e-03	9.195e-03
Clock 100Mhz Data 50Mhz	8.403e-03	8.511e-03	9.684e-03	1.113e-02
Clock = 0 Data 100Mhz	5.480e-03	5.227e-03	5.144e-03	5.104e-03
Clock = 1 Data 100Mhz	1.955e-03	1.995e-03	2.011e-03	2.019e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.760	5.7120
X8_P10	1.200	4.624	5.5488
X17_P10	1.200	4.760	5.7120
X33_P10	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007	0.0007
E	0.0009	0.0010	0.0010	0.0010
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
CP to QN ↓	0.1012	0.0944	4.7251	2.3996
CP to QN ↑	0.1124	0.0687	7.9288	3.8085
RN to QN ↑	0.1015	0.1009	7.8973	3.8105
	X17_P10	X33_P10	X17_P10	X33_P10
CP to QN ↓	0.0891	0.0939	1.2069	0.6309
CP to QN ↑	0.0709	0.0771	1.9160	0.9739
RN to QN ↑	0.0992	0.1095	1.9210	0.9755

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1350	0.0903	0.0903	0.0903
CP ↑	min_pulse_width to CP	0.0691	0.0394	0.0407	0.0454
D ↓	hold_rising to CP	-0.1430	-0.0706	-0.0706	-0.0674
D ↑	hold_rising to CP	-0.0870	-0.0342	-0.0342	-0.0342
D ↓	setup_rising to CP	0.1977	0.1199	0.1225	0.1221
D ↑	setup_rising to CP	0.1270	0.0688	0.0688	0.0688
E ↓	hold_rising to CP	-0.1011	-0.1039	-0.1043	-0.1043
E ↑	hold_rising to CP	-0.0874	-0.0315	-0.0315	-0.0315
E ↓	setup_rising to CP	0.1756	0.1685	0.1685	0.1685
E ↑	setup_rising to CP	0.1882	0.1296	0.1296	0.1296
RN ↓	min_pulse_width to RN	0.0828	0.0833	0.0947	0.1045
RN ↑	recovery_rising to CP	0.0222	0.0222	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0174	-0.0077	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0724	-0.0457	-0.0431	-0.0431
TE ↑	hold_rising to CP	-0.0577	-0.0382	-0.0386	-0.0386
TE ↓	setup_rising to CP	0.1246	0.0998	0.1024	0.1024
TE ↑	setup_rising to CP	0.2468	0.1763	0.1763	0.1763
TI ↓	hold_rising to CP	-0.1872	-0.1023	-0.1023	-0.1025
TI ↑	hold_rising to CP	-0.0681	-0.0413	-0.0397	-0.0397
TI ↓	setup_rising to CP	0.2424	0.1566	0.1582	0.1582
TI ↑	setup_rising to CP	0.1036	0.0759	0.0759	0.0759

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.416e-05	1.000e-20
X8_P10	3.842e-05	1.000e-20
X17_P10	4.865e-05	1.000e-20
X33_P10	6.275e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

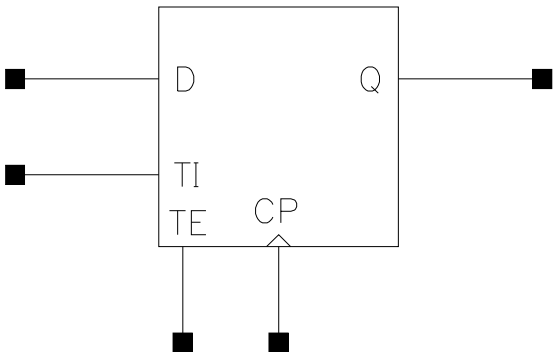
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	7.184e-03	7.237e-03	7.246e-03	7.251e-03
Clock 100Mhz Data 25Mhz	7.727e-03	7.911e-03	8.425e-03	9.151e-03
Clock 100Mhz Data 50Mhz	8.270e-03	8.585e-03	9.604e-03	1.105e-02
Clock = 0 Data 100Mhz	5.485e-03	5.230e-03	5.147e-03	5.106e-03
Clock = 1 Data 100Mhz	1.953e-03	1.997e-03	2.013e-03	2.021e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.400	4.0800
X8_P10	1.200	3.128	3.7536
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0821	0.0476	5.2087	2.4671
CP to Q ↑	0.0725	0.0619	8.1207	3.8568
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0735	0.0811	1.1858	0.6216
CP to Q ↑	0.1094	0.1160	1.9123	0.9712

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1202	0.1282	0.1282	0.1282
CP ↑	min_pulse_width to CP	0.0644	0.0361	0.0361	0.0361
D ↓	hold_rising to CP	-0.0897	-0.0370	-0.0365	-0.0365
D ↑	hold_rising to CP	-0.0386	-0.0071	-0.0066	-0.0066
D ↓	setup_rising to CP	0.1295	0.0862	0.0862	0.0862
D ↑	setup_rising to CP	0.0686	0.0369	0.0369	0.0369
TE ↓	hold_rising to CP	-0.0600	-0.0316	-0.0316	-0.0316
TE ↑	hold_rising to CP	-0.0484	-0.0315	-0.0315	-0.0315
TE ↓	setup_rising to CP	0.1074	0.0810	0.0810	0.0810
TE ↑	setup_rising to CP	0.2175	0.1768	0.1736	0.1736
TI ↓	hold_rising to CP	-0.1781	-0.1101	-0.1136	-0.1136
TI ↑	hold_rising to CP	-0.0534	-0.0312	-0.0328	-0.0328
TI ↓	setup_rising to CP	0.2226	0.1677	0.1677	0.1677
TI ↑	setup_rising to CP	0.0884	0.0626	0.0626	0.0626

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	2.753e-05	1.000e-20
X8_P10	3.262e-05	1.000e-20
X17_P10	4.705e-05	1.000e-20
X33_P10	5.940e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

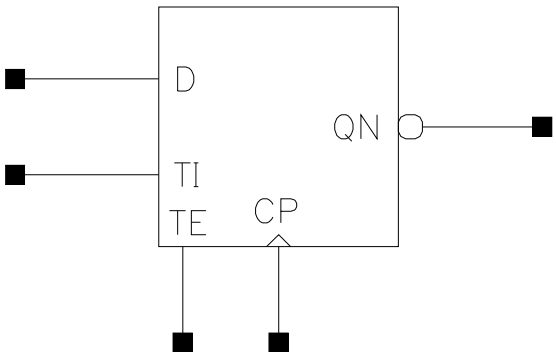
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	6.466e-03	6.521e-03	6.534e-03	6.540e-03
Clock 100Mhz Data 25Mhz	6.523e-03	6.589e-03	7.176e-03	7.813e-03
Clock 100Mhz Data 50Mhz	6.581e-03	6.657e-03	7.819e-03	9.086e-03
Clock = 0 Data 100Mhz	4.272e-03	3.997e-03	3.905e-03	3.859e-03
Clock = 1 Data 100Mhz	1.105e-03	5.691e-04	3.904e-04	3.011e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.536	4.2432
X8_P10	1.200	3.264	3.9168
X17_P10	1.200	3.536	4.2432
X33_P10	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0943	0.1007	5.3883	2.4765
CP to QN ↑	0.0886	0.0632	8.0719	3.8209
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0756	0.0839	1.1869	0.6219
CP to QN ↑	0.0622	0.0688	1.9107	0.9709

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1203	0.1282	0.1282	0.1282
CP ↑	min_pulse_width to CP	0.0501	0.0361	0.0360	0.0393
D ↓	hold_rising to CP	-0.0897	-0.0370	-0.0338	-0.0338
D ↑	hold_rising to CP	-0.0386	-0.0066	-0.0071	-0.0071
D ↓	setup_rising to CP	0.1262	0.0830	0.0862	0.0862
D ↑	setup_rising to CP	0.0681	0.0369	0.0369	0.0369
TE ↓	hold_rising to CP	-0.0600	-0.0316	-0.0316	-0.0316
TE ↑	hold_rising to CP	-0.0479	-0.0315	-0.0315	-0.0315
TE ↓	setup_rising to CP	0.1047	0.0810	0.0810	0.0810
TE ↑	setup_rising to CP	0.2175	0.1736	0.1736	0.1768
TI ↓	hold_rising to CP	-0.1781	-0.1143	-0.1101	-0.1101
TI ↑	hold_rising to CP	-0.0527	-0.0328	-0.0312	-0.0312
TI ↓	setup_rising to CP	0.2186	0.1677	0.1677	0.1677
TI ↑	setup_rising to CP	0.0881	0.0626	0.0626	0.0626

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	2.777e-05	1.000e-20
X8_P10	3.280e-05	1.000e-20
X17_P10	4.681e-05	1.000e-20
X33_P10	5.916e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

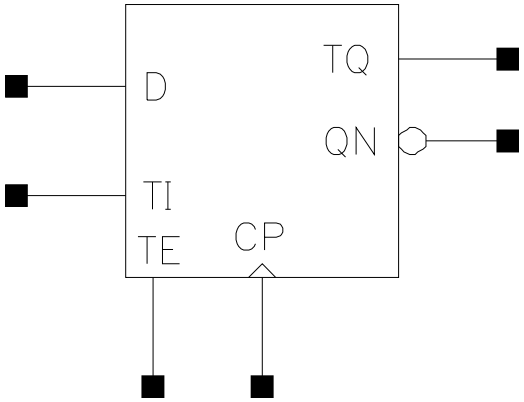
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	6.394e-03	6.481e-03	6.509e-03	6.523e-03
Clock 100Mhz Data 25Mhz	6.474e-03	6.663e-03	7.127e-03	7.778e-03
Clock 100Mhz Data 50Mhz	6.555e-03	6.846e-03	7.745e-03	9.033e-03
Clock = 0 Data 100Mhz	4.290e-03	4.002e-03	3.908e-03	3.861e-03
Clock = 1 Data 100Mhz	1.098e-03	5.655e-04	3.880e-04	2.993e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.536	4.2432
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0012	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010

TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1050	0.0893	4.8575	2.4080
CP to QN ↑	0.1077	0.0653	7.8893	3.8198
CP to TQ ↓	0.0748	0.0434	6.7359	4.5981
CP to TQ ↑	0.0750	0.0618	15.3368	10.8216
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0836	0.0903	1.2116	0.6335
CP to QN ↑	0.0671	0.0720	1.9303	0.9856
CP to TQ ↓	0.0450	0.0469	6.2214	6.2399
CP to TQ ↑	0.0630	0.0648	14.0838	14.8820

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1203	0.1282	0.1282	0.1282
CP ↑	min_pulse_width to CP	0.0644	0.0360	0.0360	0.0407
D ↓	hold_rising to CP	-0.0865	-0.0338	-0.0338	-0.0338
D ↑	hold_rising to CP	-0.0386	-0.0066	-0.0066	-0.0071
D ↓	setup_rising to CP	0.1241	0.0830	0.0830	0.0830
D ↑	setup_rising to CP	0.0686	0.0369	0.0369	0.0369
TE ↓	hold_rising to CP	-0.0604	-0.0316	-0.0316	-0.0316
TE ↑	hold_rising to CP	-0.0479	-0.0315	-0.0315	-0.0315
TE ↓	setup_rising to CP	0.1047	0.0810	0.0810	0.0810
TE ↑	setup_rising to CP	0.2149	0.1736	0.1736	0.1736
TI ↓	hold_rising to CP	-0.1781	-0.1085	-0.1085	-0.1085
TI ↑	hold_rising to CP	-0.0534	-0.0328	-0.0328	-0.0328
TI ↓	setup_rising to CP	0.2193	0.1677	0.1677	0.1677
TI ↑	setup_rising to CP	0.0884	0.0626	0.0626	0.0626

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	2.949e-05	1.000e-20
X8_P10	3.643e-05	1.000e-20
X17_P10	4.431e-05	1.000e-20
X33_P10	5.889e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10

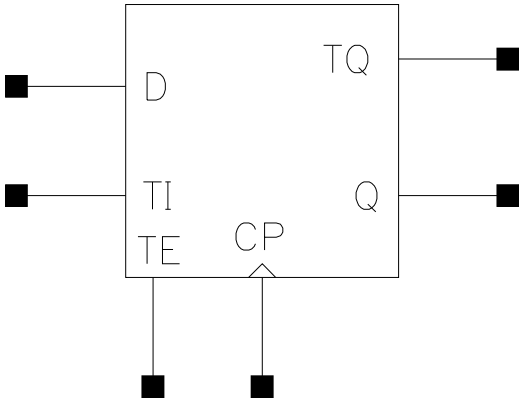
Clock 100Mhz Data 0Mhz	6.579e-03	6.577e-03	6.576e-03	6.577e-03
Clock 100Mhz Data 25Mhz	6.782e-03	6.920e-03	7.179e-03	7.901e-03
Clock 100Mhz Data 50Mhz	6.985e-03	7.263e-03	7.782e-03	9.226e-03
Clock = 0 Data 100Mhz	4.287e-03	4.008e-03	3.916e-03	3.870e-03
Clock = 1 Data 100Mhz	1.107e-03	5.699e-04	3.909e-04	3.015e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.672	4.4064
X8_P10	1.200	3.400	4.0800
X17_P10	1.200	3.672	4.4064
X33_P10	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007

TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1092	0.0533	5.5157	2.4613
CP to Q ↑	0.0835	0.0656	8.2158	3.8822
CP to TQ ↓	0.1037	0.0547	5.5076	6.3414
CP to TQ ↑	0.0859	0.0729	10.8663	15.0900
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0755	0.0831	1.2154	0.6325
CP to Q ↑	0.1113	0.1177	1.9429	0.9758
CP to TQ ↓	0.0783	0.0869	6.1319	6.2312
CP to TQ ↑	0.1186	0.1276	14.6657	14.7840

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1203	0.1282	0.1282	0.1282
CP ↑	min_pulse_width to CP	0.0927	0.0407	0.0361	0.0361
D ↓	hold_rising to CP	-0.0897	-0.0338	-0.0365	-0.0365
D ↑	hold_rising to CP	-0.0386	-0.0071	-0.0066	-0.0066
D ↓	setup_rising to CP	0.1295	0.0830	0.0862	0.0862
D ↑	setup_rising to CP	0.0686	0.0369	0.0369	0.0369
TE ↓	hold_rising to CP	-0.0600	-0.0316	-0.0316	-0.0316
TE ↑	hold_rising to CP	-0.0480	-0.0315	-0.0315	-0.0315
TE ↓	setup_rising to CP	0.1074	0.0810	0.0810	0.0810
TE ↑	setup_rising to CP	0.2175	0.1736	0.1736	0.1736
TI ↓	hold_rising to CP	-0.1781	-0.1085	-0.1136	-0.1136
TI ↑	hold_rising to CP	-0.0534	-0.0312	-0.0328	-0.0328
TI ↓	setup_rising to CP	0.2229	0.1677	0.1677	0.1677
TI ↑	setup_rising to CP	0.0884	0.0626	0.0626	0.0626

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.018e-05	1.000e-20
X8_P10	3.437e-05	1.000e-20
X17_P10	4.843e-05	1.000e-20
X33_P10	6.071e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

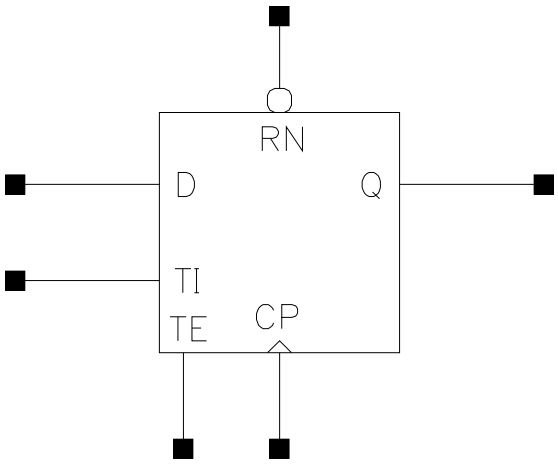
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	6.437e-03	6.503e-03	6.522e-03	6.531e-03
Clock 100Mhz Data 25Mhz	6.851e-03	6.775e-03	7.335e-03	7.998e-03
Clock 100Mhz Data 50Mhz	7.264e-03	7.048e-03	8.148e-03	9.464e-03
Clock = 0 Data 100Mhz	4.264e-03	3.989e-03	3.900e-03	3.855e-03
Clock = 1 Data 100Mhz	1.096e-03	5.646e-04	3.874e-04	2.989e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.672	4.4064
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
RN	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.0992	0.0510	5.6488	2.4759
CP to Q ↑	0.0801	0.0669	8.1306	3.8984
RN to Q ↓	0.0816	0.0723	4.8959	2.5777
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0769	0.0850	1.1978	0.6297
CP to Q ↑	0.0990	0.1051	1.9100	0.9712
RN to Q ↓	0.1076	0.1157	1.1966	0.6293

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1368	0.1312	0.1346	0.1346
CP ↑	min_pulse_width to CP	0.0880	0.0394	0.0361	0.0361
D ↓	hold_rising to CP	-0.0799	-0.0240	-0.0240	-0.0240
D ↑	hold_rising to CP	-0.0435	-0.0120	-0.0110	-0.0114
D ↓	setup_rising to CP	0.1295	0.0808	0.0808	0.0808
D ↑	setup_rising to CP	0.0783	0.0440	0.0466	0.0466
RN ↓	min_pulse_width to RN	0.0828	0.0903	0.0811	0.0811
RN ↑	recovery_rising to CP	0.0222	0.0222	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0174	-0.0109	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0550	-0.0224	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0581	-0.0391	-0.0413	-0.0413
TE ↓	setup_rising to CP	0.1080	0.0781	0.0807	0.0807
TE ↑	setup_rising to CP	0.2153	0.1691	0.1691	0.1691
TI ↓	hold_rising to CP	-0.1635	-0.0890	-0.0905	-0.0905
TI ↑	hold_rising to CP	-0.0632	-0.0367	-0.0426	-0.0426
TI ↓	setup_rising to CP	0.2177	0.1595	0.1595	0.1595
TI ↑	setup_rising to CP	0.0994	0.0772	0.0772	0.0772

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.082e-05	1.000e-20
X8_P10	3.502e-05	1.000e-20
X17_P10	4.861e-05	1.000e-20
X33_P10	6.175e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	7.193e-03	7.224e-03	7.266e-03	7.289e-03

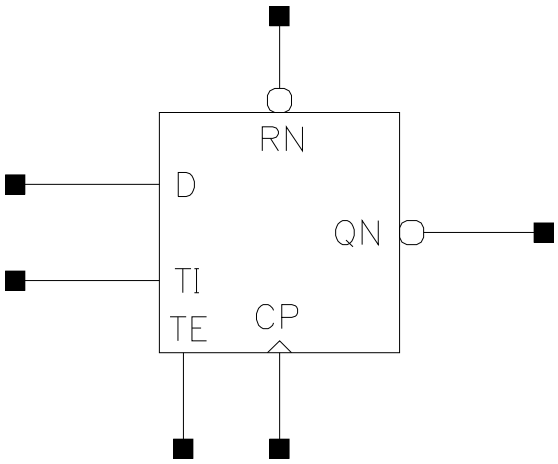
Clock 100Mhz Data 25Mhz	7.329e-03	7.257e-03	7.915e-03	8.590e-03
Clock 100Mhz Data 50Mhz	7.464e-03	7.290e-03	8.565e-03	9.891e-03
Clock = 0 Data 100Mhz	4.346e-03	4.001e-03	3.887e-03	3.830e-03
Clock = 1 Data 100Mhz	1.126e-03	5.808e-04	3.990e-04	3.082e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	3.944	4.7328
X33_P10	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0907	0.0837	4.6237	2.3445
CP to QN ↑	0.1020	0.0615	7.8955	3.7906
RN to QN ↑	0.0935	0.0945	7.8696	3.7887
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0822	0.0904	1.1993	0.6290
CP to QN ↑	0.0677	0.0747	1.9211	0.9802
RN to QN ↑	0.0975	0.1069	1.9251	0.9821

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1350	0.1312	0.1312	0.1312
CP ↑	min_pulse_width to CP	0.0644	0.0361	0.0407	0.0440
D ↓	hold_rising to CP	-0.0799	-0.0240	-0.0214	-0.0214
D ↑	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1295	0.0808	0.0808	0.0808
D ↑	setup_rising to CP	0.0783	0.0444	0.0466	0.0466
RN ↓	min_pulse_width to RN	0.0801	0.0811	0.0947	0.0996
RN ↑	recovery_rising to CP	0.0222	0.0249	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0174	-0.0126	-0.0109	-0.0109
TE ↓	hold_rising to CP	-0.0582	-0.0218	-0.0224	-0.0191
TE ↑	hold_rising to CP	-0.0577	-0.0387	-0.0391	-0.0391
TE ↓	setup_rising to CP	0.1080	0.0781	0.0781	0.0781
TE ↑	setup_rising to CP	0.2153	0.1665	0.1691	0.1691
TI ↓	hold_rising to CP	-0.1635	-0.0890	-0.0892	-0.0892
TI ↑	hold_rising to CP	-0.0632	-0.0426	-0.0410	-0.0410
TI ↓	setup_rising to CP	0.2177	0.1579	0.1595	0.1595
TI ↑	setup_rising to CP	0.0987	0.0772	0.0772	0.0772

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.158e-05	1.000e-20
X8_P10	3.473e-05	1.000e-20
X17_P10	4.778e-05	1.000e-20
X33_P10	5.906e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	7.129e-03	7.190e-03	7.209e-03	7.219e-03

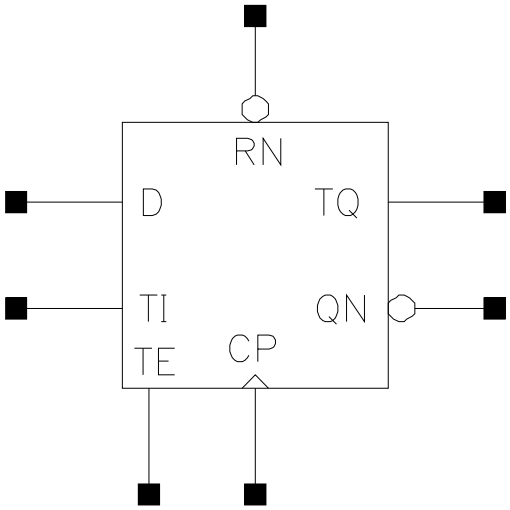
Clock 100Mhz Data 25Mhz	7.179e-03	7.246e-03	7.798e-03	8.440e-03
Clock 100Mhz Data 50Mhz	7.229e-03	7.302e-03	8.387e-03	9.662e-03
Clock = 0 Data 100Mhz	4.344e-03	3.998e-03	3.887e-03	3.831e-03
Clock = 1 Data 100Mhz	1.125e-03	5.801e-04	3.986e-04	3.079e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007

RN	0.0010	0.0007	0.0008	0.0008
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1014	0.0868	4.6366	2.4623
CP to QN ↑	0.1327	0.0688	7.0621	3.9240
CP to TQ ↓	0.0938	0.0463	5.9804	4.8334
CP to TQ ↑	0.0833	0.0679	12.2727	11.3591
RN to QN ↑	0.0922	0.0923	7.1247	3.9141
RN to TQ ↓	0.0631	0.0621	5.3806	5.0541
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0894	0.0964	1.2197	0.6401
CP to QN ↑	0.0696	0.0736	1.9495	0.9815
CP to TQ ↓	0.0482	0.0501	6.0438	5.9050
CP to TQ ↑	0.0679	0.0696	10.6236	10.7478
RN to QN ↑	0.0956	0.1025	1.9463	0.9794
RN to TQ ↓	0.0668	0.0701	6.2648	6.1597

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1350	0.1312	0.1346	0.1346
CP ↑	min_pulse_width to CP	0.0910	0.0360	0.0408	0.0408
D ↓	hold_rising to CP	-0.0799	-0.0240	-0.0214	-0.0214
D ↑	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1295	0.0808	0.0808	0.0808
D ↑	setup_rising to CP	0.0783	0.0466	0.0466	0.0466
RN ↓	min_pulse_width to RN	0.0850	0.0876	0.0898	0.0974
RN ↑	recovery_rising to CP	0.0275	0.0222	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0174	-0.0109	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0582	-0.0224	-0.0224	-0.0191
TE ↑	hold_rising to CP	-0.0581	-0.0391	-0.0413	-0.0413
TE ↓	setup_rising to CP	0.1074	0.0781	0.0807	0.0807
TE ↑	setup_rising to CP	0.2153	0.1665	0.1691	0.1691
TI ↓	hold_rising to CP	-0.1635	-0.0890	-0.0890	-0.0892
TI ↑	hold_rising to CP	-0.0632	-0.0410	-0.0426	-0.0426
TI ↓	setup_rising to CP	0.2177	0.1579	0.1595	0.1595
TI ↑	setup_rising to CP	0.1030	0.0772	0.0772	0.0772

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.445e-05	1.000e-20
X8_P10	3.658e-05	1.000e-20
X17_P10	4.474e-05	1.000e-20
X33_P10	5.834e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

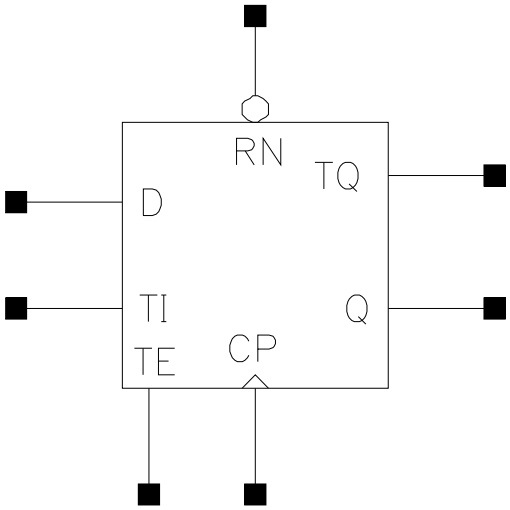
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	7.132e-03	7.188e-03	7.243e-03	7.272e-03
Clock 100Mhz Data 25Mhz	7.413e-03	7.388e-03	7.739e-03	8.504e-03
Clock 100Mhz Data 50Mhz	7.695e-03	7.589e-03	8.235e-03	9.737e-03
Clock = 0 Data 100Mhz	4.341e-03	3.998e-03	3.882e-03	3.824e-03
Clock = 1 Data 100Mhz	1.125e-03	5.801e-04	3.985e-04	3.078e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0007	0.0007	0.0007

RN	0.0008	0.0008	0.0007	0.0007
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1122	0.0553	5.9027	2.5338
CP to Q ↑	0.0857	0.0698	8.3746	4.0033
CP to TQ ↓	0.1051	0.0549	7.4218	6.3896
CP to TQ ↑	0.0894	0.0744	16.5571	15.0075
RN to Q ↓	0.0845	0.0824	5.0793	2.6480
RN to TQ ↓	0.0824	0.0795	6.4951	6.6464
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0801	0.0880	1.2158	0.6380
CP to Q ↑	0.1004	0.1061	1.9160	0.9743
CP to TQ ↓	0.0830	0.0929	6.1697	6.2568
CP to TQ ↑	0.1072	0.1167	14.7953	14.8528
RN to Q ↓	0.1109	0.1187	1.2126	0.6374
RN to TQ ↓	0.1138	0.1236	6.1646	6.2525

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1350	0.1312	0.1312	0.1312
CP ↑	min_pulse_width to CP	0.1021	0.0407	0.0361	0.0361
D ↓	hold_rising to CP	-0.0767	-0.0218	-0.0240	-0.0240
D ↑	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1300	0.0808	0.0808	0.0808
D ↑	setup_rising to CP	0.0783	0.0466	0.0440	0.0444
RN ↓	min_pulse_width to RN	0.0876	0.0974	0.0811	0.0811
RN ↑	recovery_rising to CP	0.0222	0.0222	0.0222	0.0222
RN ↑	removal_rising to CP	-0.0175	-0.0099	-0.0109	-0.0109
TE ↓	hold_rising to CP	-0.0550	-0.0191	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0577	-0.0391	-0.0413	-0.0413
TE ↓	setup_rising to CP	0.1047	0.0781	0.0781	0.0781
TE ↑	setup_rising to CP	0.2153	0.1691	0.1665	0.1665
TI ↓	hold_rising to CP	-0.1635	-0.0892	-0.0889	-0.0889
TI ↑	hold_rising to CP	-0.0632	-0.0367	-0.0426	-0.0426
TI ↓	setup_rising to CP	0.2177	0.1595	0.1579	0.1579
TI ↑	setup_rising to CP	0.0987	0.0772	0.0772	0.0772

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.215e-05	1.000e-20
X8_P10	3.634e-05	1.000e-20
X17_P10	4.941e-05	1.000e-20
X33_P10	6.257e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

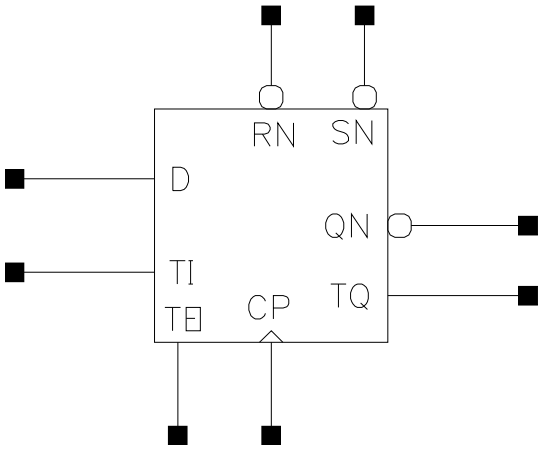
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	7.181e-03	7.214e-03	7.225e-03	7.230e-03
Clock 100Mhz Data 25Mhz	7.497e-03	7.394e-03	8.057e-03	8.731e-03
Clock 100Mhz Data 50Mhz	7.813e-03	7.573e-03	8.889e-03	1.023e-02
Clock = 0 Data 100Mhz	4.345e-03	4.000e-03	3.886e-03	3.828e-03
Clock = 1 Data 100Mhz	1.126e-03	5.809e-04	3.991e-04	3.083e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.352	5.2224
X17_P10	1.200	4.488	5.3856
X33_P10	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0008	0.0008	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	X17_P10	X8_P10	X17_P10
CP to QN ↓	0.0959	0.1021	2.3829	1.2288
CP to QN ↑	0.0712	0.0747	3.8088	1.9243
CP to TQ ↓	0.0540	0.0539	7.8191	7.8369
CP to TQ ↑	0.0796	0.0795	19.7960	19.8122
RN to QN ↓	0.1045	0.1106	2.3792	1.2289
RN to QN ↑	0.1034	0.1087	3.8124	1.9282
RN to TQ ↓	0.0783	0.0780	8.3588	8.3580
RN to TQ ↑	0.0886	0.0887	19.7679	19.7674
SN to QN ↓	0.1112	0.1187	2.3931	1.2320
SN to TQ ↑	0.0931	0.0929	19.9814	20.0143
	X33_P10		X33_P10	
CP to QN ↓	0.1181		0.6537	
CP to QN ↑	0.0842		0.9830	
CP to TQ ↓	0.0540		7.8472	
CP to TQ ↑	0.0798		19.8304	
RN to QN ↓	0.1262		0.6537	
RN to QN ↑	0.1215		0.9830	
RN to TQ ↓	0.0780		8.3921	
RN to TQ ↑	0.0889		19.8023	
SN to QN ↓	0.1369		0.6541	
SN to TQ ↑	0.0930		20.0819	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1400	0.1400	0.1400
CP ↑	min_pulse_width to CP	0.0407	0.0407	0.0455
D ↓	hold_rising to CP	-0.0240	-0.0240	-0.0240
D ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120
D ↓	setup_rising to CP	0.0883	0.0883	0.0883
D ↑	setup_rising to CP	0.0466	0.0466	0.0466
RN ↓	min_pulse_width to RN	0.0947	0.0996	0.1072
RN ↑	non_seq_hold_rising to SN	-0.0386	-0.0386	-0.0386
RN ↑	non_seq_setup_rising to SN	0.0839	0.0839	0.0839
RN ↑	recovery_rising to CP	0.0368	0.0368	0.0368
RN ↑	removal_rising to CP	-0.0223	-0.0223	-0.0223
SN ↓	min_pulse_width to SN	0.0793	0.0820	0.0869
SN ↑	recovery_rising to CP	0.0103	0.0103	0.0103
SN ↑	removal_rising to CP	0.0410	0.0410	0.0410

TE ↓	hold_rising to CP	-0.0218	-0.0218	-0.0218
TE ↑	hold_rising to CP	-0.0391	-0.0391	-0.0391
TE ↓	setup_rising to CP	0.0862	0.0856	0.0856
TE ↑	setup_rising to CP	0.1768	0.1736	0.1768
TI ↓	hold_rising to CP	-0.0905	-0.0905	-0.0905
TI ↑	hold_rising to CP	-0.0410	-0.0410	-0.0367
TI ↓	setup_rising to CP	0.1677	0.1677	0.1677
TI ↑	setup_rising to CP	0.0772	0.0772	0.0772

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	4.045e-05	1.000e-20
X17_P10	4.695e-05	1.000e-20
X33_P10	5.873e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

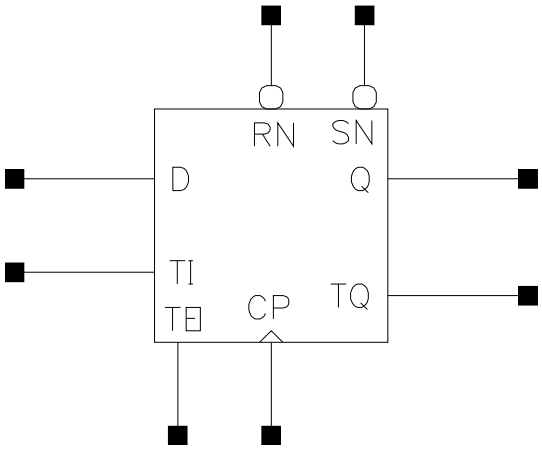
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	7.633e-03	7.633e-03	7.635e-03
Clock 100Mhz Data 25Mhz	7.754e-03	8.061e-03	8.930e-03
Clock 100Mhz Data 50Mhz	7.874e-03	8.490e-03	1.023e-02
Clock = 0 Data 100Mhz	3.792e-03	3.790e-03	3.791e-03
Clock = 1 Data 100Mhz	3.571e-05	3.577e-05	3.583e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P10	1.200	4.216	5.0592
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009
D	0.0006	0.0006	0.0006
RN	0.0008	0.0008	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P10	**X17_P10**	**X8_P10**	**X17_P10**
CP to Q ↓	0.0604	0.0677	2.4742	1.2839
CP to Q ↑	0.0764	0.0806	3.8983	1.9815
CP to TQ ↓	0.0616	0.0699	7.9278	8.0213
CP to TQ ↑	0.0854	0.0943	19.1592	19.2575
RN to Q ↓	0.0942	0.1101	2.7957	1.4588
RN to Q ↑	0.0690	0.0786	4.0353	2.0582
RN to TQ ↓	0.0927	0.1083	8.5793	8.7833
RN to TQ ↑	0.0839	0.1013	19.3436	19.4529
SN to Q ↑	0.0922	0.1015	4.0392	2.0587
SN to TQ ↑	0.1070	0.1243	19.3464	19.4577
	X33_P10		**X33_P10**	
CP to Q ↓	0.0859		0.6893	
CP to Q ↑	0.0921		1.0216	
CP to TQ ↓	0.0848		8.2802	
CP to TQ ↑	0.1112		19.4400	
RN to Q ↓	0.1479		0.7978	
RN to Q ↑	0.1021		1.0734	
RN to TQ ↓	0.1364		9.3078	
RN to TQ ↑	0.1356		19.6415	
SN to Q ↑	0.1249		1.0735	
SN to TQ ↑	0.1584		19.6434	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1400	0.1400	0.1400
CP ↑	min_pulse_width to CP	0.0455	0.0548	0.0738
D ↓	hold_rising to CP	-0.0240	-0.0218	-0.0218
D ↑	hold_rising to CP	-0.0120	-0.0120	-0.0120
D ↓	setup_rising to CP	0.0883	0.0883	0.0883
D ↑	setup_rising to CP	0.0466	0.0466	0.0466
RN ↓	min_pulse_width to RN	0.1094	0.1316	0.1707
RN ↑	non_seq_hold_rising to SN	-0.0406	-0.0505	-0.0673
RN ↑	non_seq_setup_rising to SN	0.0789	0.0840	0.1142
RN ↑	recovery_rising to CP	0.0320	0.0320	0.0320
RN ↑	removal_rising to CP	-0.0174	-0.0174	-0.0174
SN ↓	min_pulse_width to SN	0.0891	0.1038	0.1331
SN ↑	recovery_rising to CP	0.0103	0.0103	0.0103
SN ↑	removal_rising to CP	0.0410	0.0410	0.0410

TE ↓	hold_rising to CP	-0.0224	-0.0191	-0.0191
TE ↑	hold_rising to CP	-0.0391	-0.0391	-0.0359
TE ↓	setup_rising to CP	0.0862	0.0862	0.0856
TE ↑	setup_rising to CP	0.1736	0.1768	0.1768
TI ↓	hold_rising to CP	-0.0890	-0.0892	-0.0892
TI ↑	hold_rising to CP	-0.0370	-0.0377	-0.0377
TI ↓	setup_rising to CP	0.1677	0.1677	0.1677
TI ↑	setup_rising to CP	0.0772	0.0772	0.0772

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P10	4.044e-05	1.000e-20
X17_P10	4.731e-05	1.000e-20
X33_P10	6.025e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

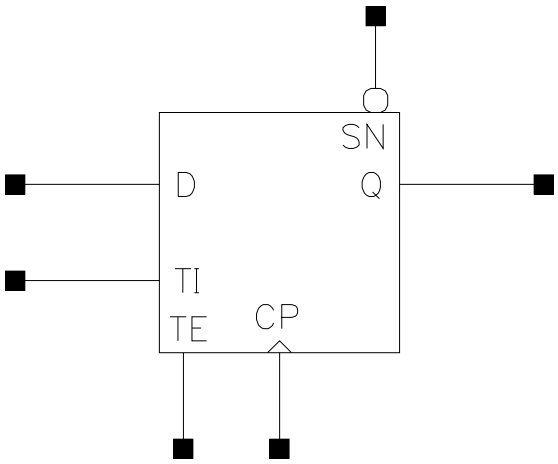
Pin Cycle	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	7.621e-03	7.623e-03	7.623e-03
Clock 100Mhz Data 25Mhz	7.696e-03	8.100e-03	9.202e-03
Clock 100Mhz Data 50Mhz	7.771e-03	8.578e-03	1.078e-02
Clock = 0 Data 100Mhz	3.788e-03	3.788e-03	3.788e-03
Clock = 1 Data 100Mhz	3.571e-05	3.571e-05	3.578e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0014	0.0014	0.0013	0.0013
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P10			

CP	0.0009			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1002	0.0530	5.6629	2.4593
CP to Q ↑	0.0842	0.0701	8.2030	3.8848
SN to Q ↑	0.0625	0.0711	7.9887	3.8859
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
CP to Q ↓	0.0762	0.0804	1.2006	0.8286
CP to Q ↑	0.0997	0.1030	1.9087	1.2914
SN to Q ↑	0.0998	0.1030	1.9083	1.2908
	X33_P10		**X33_P10**	
CP to Q ↓	0.0836		0.6303	
CP to Q ↑	0.1051		0.9710	
SN to Q ↑	0.1052		0.9713	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.1398	0.1416	0.1416	0.1416
CP ↑	min_pulse_width to CP	0.0880	0.0409	0.0362	0.0362
D ↓	hold_rising to CP	-0.0799	-0.0289	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0435	-0.0094	-0.0094	-0.0094
D ↓	setup_rising to CP	0.1343	0.0879	0.0879	0.0879
D ↑	setup_rising to CP	0.0730	0.0391	0.0391	0.0391
SN ↓	min_pulse_width to SN	0.0571	0.0642	0.0593	0.0620
SN ↑	recovery_rising to CP	0.0134	0.0102	0.0102	0.0102
SN ↑	removal_rising to CP	0.0309	0.0411	0.0411	0.0411
TE ↓	hold_rising to CP	-0.0604	-0.0272	-0.0267	-0.0267
TE ↑	hold_rising to CP	-0.0555	-0.0338	-0.0364	-0.0364
TE ↓	setup_rising to CP	0.1128	0.0859	0.0859	0.0859
TE ↑	setup_rising to CP	0.2202	0.1785	0.1785	0.1785
TI ↓	hold_rising to CP	-0.1686	-0.0990	-0.0987	-0.0987
TI ↑	hold_rising to CP	-0.0634	-0.0361	-0.0377	-0.0377
TI ↓	setup_rising to CP	0.2226	0.1735	0.1735	0.1735
TI ↑	setup_rising to CP	0.0981	0.0674	0.0674	0.0674
		X33_P10			

CP ↓	min_pulse_width to CP	0.1416			
CP ↑	min_pulse_width to CP	0.0362			
D ↓	hold_rising to CP	-0.0289			
D ↑	hold_rising to CP	-0.0094			
D ↓	setup_rising to CP	0.0879			
D ↑	setup_rising to CP	0.0391			
SN ↓	min_pulse_width to SN	0.0593			
SN ↑	recovery_rising to CP	0.0102			
SN ↑	removal_rising to CP	0.0411			
TE ↓	hold_rising to CP	-0.0267			
TE ↑	hold_rising to CP	-0.0364			
TE ↓	setup_rising to CP	0.0859			
TE ↑	setup_rising to CP	0.1785			
TI ↓	hold_rising to CP	-0.0987			
TI ↑	hold_rising to CP	-0.0377			
TI ↓	setup_rising to CP	0.1735			
TI ↑	setup_rising to CP	0.0674			

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.062e-05	1.000e-20
X8_P10	3.559e-05	1.000e-20
X17_P10	4.860e-05	1.000e-20
X25_P10	5.427e-05	1.000e-20
X33_P10	5.988e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	6.982e-03	7.147e-03	7.200e-03	7.228e-03
Clock 100Mhz Data 25Mhz	7.158e-03	7.254e-03	7.875e-03	8.221e-03
Clock 100Mhz Data 50Mhz	7.334e-03	7.361e-03	8.549e-03	9.214e-03
Clock = 0 Data 100Mhz	4.163e-03	3.921e-03	3.841e-03	3.802e-03
Clock = 1 Data 100Mhz	1.126e-03	5.805e-04	3.988e-04	3.080e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	7.244e-03			

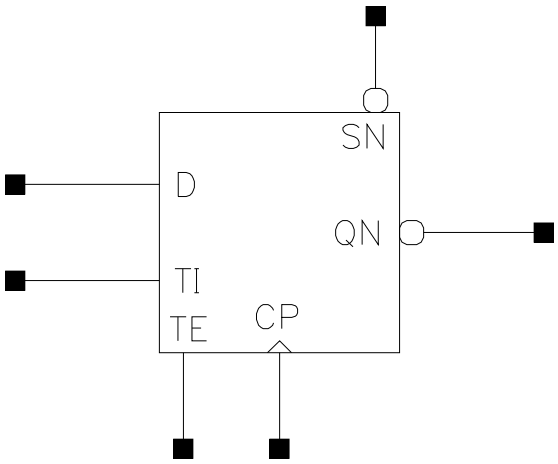
Clock 100Mhz Data 25Mhz	8.524e-03			
Clock 100Mhz Data 50Mhz	9.803e-03			
Clock = 0 Data 100Mhz	3.778e-03			
Clock = 1 Data 100Mhz	2.535e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	3.944	4.7328
X8_P10	1.200	3.808	4.5696
X17_P10	1.200	4.080	4.8960
X25_P10	1.200	4.216	5.0592
X33_P10	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X25_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004
SN	0.0014	0.0013	0.0014	0.0014
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004
	X33_P10			

CP	0.0009			
D	0.0004			
SN	0.0014			
TE	0.0010			
TI	0.0004			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.0949	0.0845	4.6255	2.3456
CP to QN ↑	0.1031	0.0613	7.8898	3.8039
SN to QN ↓	0.0748	0.0843	4.6115	2.3450
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
CP to QN ↓	0.0875	0.0925	1.2037	0.8310
CP to QN ↑	0.0719	0.0763	1.9105	1.2930
SN to QN ↓	0.0894	0.0945	1.2046	0.8303
	X33_P10		**X33_P10**	
CP to QN ↓	0.0965		0.6324	
CP to QN ↑	0.0794		0.9725	
SN to QN ↓	0.0985		0.6320	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X25_P10
CP ↓	min_pulse_width to CP	0.1398	0.1416	0.1416	0.1416
CP ↑	min_pulse_width to CP	0.0644	0.0361	0.0409	0.0455
D ↓	hold_rising to CP	-0.0799	-0.0289	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0435	-0.0094	-0.0094	-0.0094
D ↓	setup_rising to CP	0.1349	0.0879	0.0879	0.0879
D ↑	setup_rising to CP	0.0730	0.0359	0.0391	0.0391
SN ↓	min_pulse_width to SN	0.0544	0.0593	0.0669	0.0691
SN ↑	recovery_rising to CP	0.0102	0.0102	0.0102	0.0102
SN ↑	removal_rising to CP	0.0309	0.0411	0.0411	0.0411
TE ↓	hold_rising to CP	-0.0604	-0.0267	-0.0272	-0.0272
TE ↑	hold_rising to CP	-0.0555	-0.0364	-0.0338	-0.0338
TE ↓	setup_rising to CP	0.1128	0.0859	0.0859	0.0859
TE ↑	setup_rising to CP	0.2202	0.1785	0.1785	0.1785
TI ↓	hold_rising to CP	-0.1686	-0.0987	-0.0990	-0.0990
TI ↑	hold_rising to CP	-0.0634	-0.0377	-0.0361	-0.0361
TI ↓	setup_rising to CP	0.2226	0.1735	0.1733	0.1726
TI ↑	setup_rising to CP	0.0981	0.0674	0.0674	0.0674
		X33_P10			

CP ↓	min_pulse_width to CP	0.1416			
CP ↑	min_pulse_width to CP	0.0455			
D ↓	hold_rising to CP	-0.0289			
D ↑	hold_rising to CP	-0.0094			
D ↓	setup_rising to CP	0.0879			
D ↑	setup_rising to CP	0.0391			
SN ↓	min_pulse_width to SN	0.0691			
SN ↑	recovery_rising to CP	0.0102			
SN ↑	removal_rising to CP	0.0411			
TE ↓	hold_rising to CP	-0.0272			
TE ↑	hold_rising to CP	-0.0338			
TE ↓	setup_rising to CP	0.0859			
TE ↑	setup_rising to CP	0.1785			
TI ↓	hold_rising to CP	-0.0990			
TI ↑	hold_rising to CP	-0.0361			
TI ↓	setup_rising to CP	0.1726			
TI ↑	setup_rising to CP	0.0674			

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.026e-05	1.000e-20
X8_P10	3.584e-05	1.000e-20
X17_P10	4.921e-05	1.000e-20
X25_P10	5.576e-05	1.000e-20
X33_P10	6.235e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P10	X8_P10	X17_P10	X25_P10
Clock 100Mhz Data 0Mhz	6.983e-03	7.158e-03	7.210e-03	7.235e-03
Clock 100Mhz Data 25Mhz	7.026e-03	7.209e-03	7.897e-03	8.254e-03
Clock 100Mhz Data 50Mhz	7.070e-03	7.259e-03	8.585e-03	9.273e-03
Clock = 0 Data 100Mhz	4.163e-03	3.925e-03	3.843e-03	3.803e-03
Clock = 1 Data 100Mhz	1.126e-03	5.805e-04	3.988e-04	3.080e-04
	X33_P10			
Clock 100Mhz Data 0Mhz	7.251e-03			

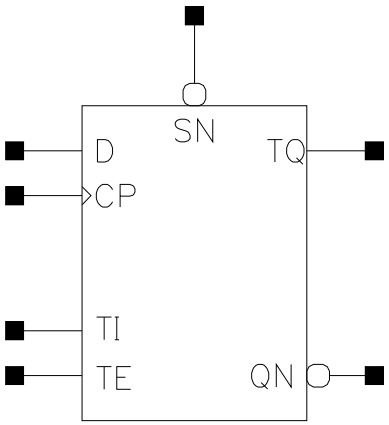
Clock 100Mhz Data 25Mhz	8.581e-03			
Clock 100Mhz Data 50Mhz	9.910e-03			
Clock = 0 Data 100Mhz	3.779e-03			
Clock = 1 Data 100Mhz	2.535e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.216	5.0592
X8_P10	1.200	4.080	4.8960
X17_P10	1.200	4.352	5.2224
X33_P10	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0016	0.0016	0.0016
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to QN ↓	0.1095	0.0890	4.6217	2.3549
CP to QN ↑	0.1339	0.0692	7.7711	3.8510
CP to TQ ↓	0.0960	0.0471	6.7560	5.6583
CP to TQ ↑	0.0839	0.0667	10.8537	10.5707
SN to QN ↓	0.0716	0.0676	4.6129	2.3561
SN to TQ ↑	0.0494	0.0472	10.6560	10.5361
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to QN ↓	0.0881	0.0972	1.2294	0.6265
CP to QN ↑	0.0775	0.0854	1.9186	0.9747
CP to TQ ↓	0.0582	0.0582	5.8661	5.8657
CP to TQ ↑	0.0750	0.0750	10.6790	10.7001
SN to QN ↓	0.0755	0.0845	1.2282	0.6257
SN to TQ ↑	0.0620	0.0619	10.6689	10.6914

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1397	0.1416	0.1416	0.1416
CP ↑	min_pulse_width to CP	0.0927	0.0361	0.0455	0.0501
D ↓	hold_rising to CP	-0.0799	-0.0289	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0435	-0.0094	-0.0094	-0.0094
D ↓	setup_rising to CP	0.1343	0.0879	0.0879	0.0879
D ↑	setup_rising to CP	0.0730	0.0391	0.0391	0.0391
SN ↓	min_pulse_width to SN	0.0474	0.0522	0.0549	0.0549
SN ↑	recovery_rising to CP	0.0134	0.0102	0.0102	0.0102
SN ↑	removal_rising to CP	0.0309	0.0411	0.0385	0.0385
TE ↓	hold_rising to CP	-0.0578	-0.0267	-0.0272	-0.0272
TE ↑	hold_rising to CP	-0.0555	-0.0338	-0.0342	-0.0338
TE ↓	setup_rising to CP	0.1128	0.0859	0.0859	0.0859
TE ↑	setup_rising to CP	0.2202	0.1785	0.1785	0.1785
TI ↓	hold_rising to CP	-0.1686	-0.0987	-0.0990	-0.0990
TI ↑	hold_rising to CP	-0.0634	-0.0361	-0.0318	-0.0318
TI ↓	setup_rising to CP	0.2226	0.1733	0.1726	0.1726
TI ↑	setup_rising to CP	0.0981	0.0674	0.0674	0.0674

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.424e-05	1.000e-20
X8_P10	3.972e-05	1.000e-20
X17_P10	5.310e-05	1.000e-20
X33_P10	6.624e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

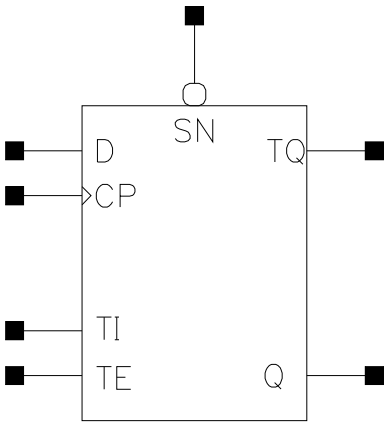
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	6.990e-03	7.155e-03	7.211e-03	7.239e-03
Clock 100Mhz Data 25Mhz	7.341e-03	7.413e-03	8.055e-03	8.723e-03
Clock 100Mhz Data 50Mhz	7.692e-03	7.670e-03	8.900e-03	1.021e-02
Clock = 0 Data 100Mhz	4.172e-03	3.930e-03	3.850e-03	3.810e-03
Clock = 1 Data 100Mhz	1.126e-03	5.806e-04	3.989e-04	3.081e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	4.080	4.8960
X8_P10	1.200	3.944	4.7328
X17_P10	1.200	4.216	5.0592
X33_P10	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X33_P10
CP	0.0009	0.0009	0.0009	0.0009
D	0.0008	0.0004	0.0004	0.0004

SN	0.0015	0.0014	0.0014	0.0013
TE	0.0009	0.0010	0.0010	0.0010
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
CP to Q ↓	0.1147	0.0570	5.8048	2.5063
CP to Q ↑	0.0897	0.0726	8.2330	3.9258
CP to TQ ↓	0.1138	0.0583	8.5322	6.4203
CP to TQ ↑	0.0884	0.0808	10.9335	15.1543
SN to Q ↑	0.0529	0.0742	7.9957	3.9237
SN to TQ ↑	0.0519	0.0837	10.6760	15.1204
	X17_P10	**X33_P10**	**X17_P10**	**X33_P10**
CP to Q ↓	0.0782	0.0856	1.2286	0.6403
CP to Q ↑	0.1014	0.1065	1.9170	0.9751
CP to TQ ↓	0.0812	0.0906	6.1666	6.2420
CP to TQ ↑	0.1084	0.1172	14.8028	14.8642
SN to Q ↑	0.1014	0.1065	1.9160	0.9751
SN to TQ ↑	0.1084	0.1172	14.8023	14.8627

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P10	X8_P10	X17_P10	X33_P10
CP ↓	min_pulse_width to CP	0.1391	0.1416	0.1416	0.1416
CP ↑	min_pulse_width to CP	0.1021	0.0422	0.0362	0.0362
D ↓	hold_rising to CP	-0.0799	-0.0289	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0435	-0.0094	-0.0094	-0.0094
D ↓	setup_rising to CP	0.1290	0.0879	0.0879	0.0879
D ↑	setup_rising to CP	0.0730	0.0391	0.0391	0.0391
SN ↓	min_pulse_width to SN	0.0474	0.0718	0.0593	0.0593
SN ↑	recovery_rising to CP	0.0102	0.0102	0.0102	0.0102
SN ↑	removal_rising to CP	0.0309	0.0411	0.0411	0.0411
TE ↓	hold_rising to CP	-0.0604	-0.0240	-0.0267	-0.0267
TE ↑	hold_rising to CP	-0.0549	-0.0338	-0.0364	-0.0364
TE ↓	setup_rising to CP	0.1096	0.0859	0.0859	0.0859
TE ↑	setup_rising to CP	0.2208	0.1785	0.1785	0.1785
TI ↓	hold_rising to CP	-0.1686	-0.0990	-0.0987	-0.0987
TI ↑	hold_rising to CP	-0.0634	-0.0361	-0.0377	-0.0377
TI ↓	setup_rising to CP	0.2226	0.1733	0.1735	0.1735
TI ↑	setup_rising to CP	0.0981	0.0674	0.0674	0.0674

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	3.366e-05	1.000e-20
X8_P10	3.737e-05	1.000e-20
X17_P10	5.015e-05	1.000e-20
X33_P10	6.140e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

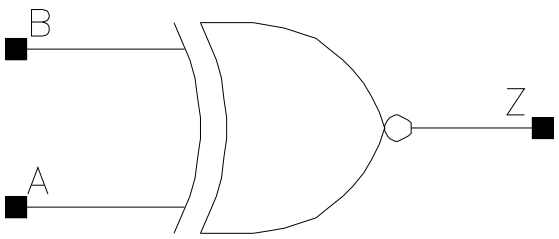
Pin Cycle	X4_P10	X8_P10	X17_P10	X33_P10
Clock 100Mhz Data 0Mhz	6.982e-03	7.148e-03	7.201e-03	7.229e-03
Clock 100Mhz Data 25Mhz	7.373e-03	7.417e-03	8.052e-03	8.728e-03
Clock 100Mhz Data 50Mhz	7.764e-03	7.685e-03	8.902e-03	1.023e-02
Clock = 0 Data 100Mhz	4.173e-03	3.927e-03	3.846e-03	3.804e-03
Clock = 1 Data 100Mhz	1.126e-03	5.807e-04	3.989e-04	3.081e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.360	1.6320
X17_P10	1.200	1.496	1.7952
X25_P10	1.200	2.312	2.7744
X33_P10	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P10	X8_P10	X17_P10	X25_P10
A	0.0017	0.0007	0.0009	0.0014
B	0.0016	0.0014	0.0018	0.0025
	X33_P10			
A	0.0016			
B	0.0029			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P10	**X8_P10**	**X6_P10**	**X8_P10**
A to Z ↓	0.0245	0.0566	4.4343	2.5387
A to Z ↑	0.0257	0.0508	5.7639	4.0137
B to Z ↓	0.0232	0.0381	4.4309	2.5207
B to Z ↑	0.0260	0.0363	5.7712	3.9999
	X17_P10	**X25_P10**	**X17_P10**	**X25_P10**
A to Z ↓	0.0534	0.0536	1.2480	0.8569
A to Z ↑	0.0463	0.0466	1.9577	1.3032

B to Z ↓	0.0391	0.0380	1.2446	0.8548
B to Z ↑	0.0359	0.0348	1.9544	1.3000
	X33_P10		**X33_P10**	
A to Z ↓	0.0505		0.6438	
A to Z ↑	0.0450		0.9789	
B to Z ↓	0.0364		0.6424	
B to Z ↑	0.0342		0.9779	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P10	1.912e-05	1.000e-20
X8_P10	2.254e-05	1.000e-20
X17_P10	3.829e-05	1.000e-20
X25_P10	5.920e-05	1.000e-20
X33_P10	8.161e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	2.218e-03	4.172e-03	6.058e-03	9.627e-03
B to Z	2.161e-03	2.899e-03	4.614e-03	7.179e-03
	X33_P10			
A to Z	1.181e-02			
B to Z	9.113e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

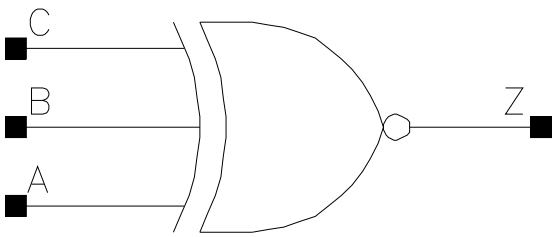
Pin Cycle (vdds)	X6_P10	X8_P10	X17_P10	X25_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P10			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	2.176	2.6112
X16_P10	1.200	2.720	3.2640
X25_P10	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X16_P10	X25_P10
A	0.0028	0.0023	0.0029	0.0043
B	0.0031	0.0021	0.0029	0.0040
C	0.0020	0.0007	0.0007	0.0007

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0394	0.0666	5.2678	2.6728
A to Z ↑	0.0371	0.0612	8.0807	3.9775
B to Z ↓	0.0403	0.0666	5.2681	2.6738
B to Z ↑	0.0373	0.0614	8.0732	3.9789
C to Z ↓	0.0393	0.0882	5.2715	2.6722
C to Z ↑	0.0359	0.0825	8.0748	3.9779
	X16_P10	**X25_P10**	**X16_P10**	**X25_P10**
A to Z ↓	0.0662	0.0661	1.3757	0.8754
A to Z ↑	0.0656	0.0646	2.0832	1.3079
B to Z ↓	0.0666	0.0673	1.3757	0.8754

B to Z ↑	0.0659	0.0661	2.0862	1.3077
C to Z ↓	0.0927	0.0983	1.3747	0.8751
C to Z ↑	0.0911	0.0966	2.0841	1.3085

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	1.921e-05	1.000e-20
X8_P10	1.990e-05	1.000e-20
X16_P10	3.413e-05	1.000e-20
X25_P10	4.925e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	2.366e-03	3.290e-03	5.415e-03	8.174e-03
B to Z	2.408e-03	3.265e-03	5.418e-03	8.240e-03
C to Z	2.367e-03	4.932e-03	7.444e-03	1.121e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

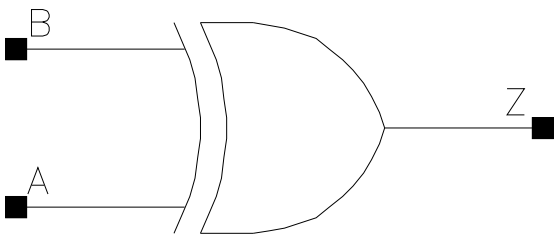
Pin Cycle (vdds)	X4_P10	X8_P10	X16_P10	X25_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	1.224	1.4688
X6_P10	1.200	0.952	1.1424
X8_P10	1.200	1.224	1.4688
X16_P10	1.200	1.360	1.6320
X25_P10	1.200	2.176	2.6112
X31_P10	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P10	X6_P10	X8_P10	X16_P10
A	0.0007	0.0016	0.0010	0.0011
B	0.0012	0.0015	0.0015	0.0016
	X25_P10	X31_P10		
A	0.0014	0.0019		
B	0.0026	0.0033		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X6_P10**	**X4_P10**	**X6_P10**
A to Z ↓	0.0502	0.0247	4.6898	3.4138
A to Z ↑	0.0475	0.0264	7.6907	7.2668
B to Z ↓	0.0353	0.0250	4.6668	3.4303
B to Z ↑	0.0359	0.0248	7.6834	7.2589
	X8_P10	**X16_P10**	**X8_P10**	**X16_P10**
A to Z ↓	0.0450	0.0466	2.4794	1.2812

A to Z ↑	0.0406	0.0425	3.9146	1.9710
B to Z ↓	0.0342	0.0350	2.4708	1.2787
B to Z ↑	0.0326	0.0340	3.9137	1.9686
	X25_P10	**X31_P10**	**X25_P10**	**X31_P10**
A to Z ↓	0.0498	0.0467	0.8485	0.6847
A to Z ↑	0.0450	0.0426	1.3011	1.0489
B to Z ↓	0.0365	0.0343	0.8481	0.6843
B to Z ↑	0.0336	0.0320	1.3002	1.0488

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	1.805e-05	1.000e-20
X6_P10	1.859e-05	1.000e-20
X8_P10	2.896e-05	1.000e-20
X16_P10	4.366e-05	1.000e-20
X25_P10	5.858e-05	1.000e-20
X31_P10	8.048e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	3.088e-03	2.205e-03	3.792e-03	5.549e-03
B to Z	2.385e-03	2.103e-03	3.139e-03	4.627e-03
	X25_P10	X31_P10		
A to Z	8.786e-03	1.080e-02		
B to Z	6.385e-03	7.831e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

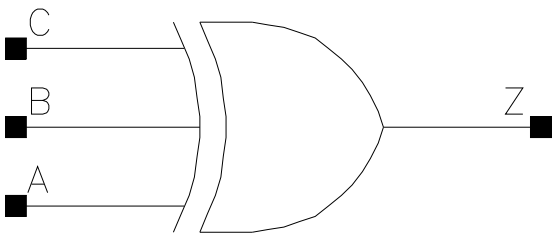
Pin Cycle (vdds)	X4_P10	X6_P10	X8_P10	X16_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P10	X31_P10		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.200	2.040	2.4480
X8_P10	1.200	1.904	2.2848
X17_P10	1.200	2.040	2.4480
X24_P10	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P10	X8_P10	X17_P10	X24_P10
A	0.0023	0.0023	0.0029	0.0052
B	0.0024	0.0021	0.0027	0.0044
C	0.0007	0.0016	0.0023	0.0035

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0396	0.0665	5.4983	2.6720
A to Z ↑	0.0373	0.0612	8.8237	3.9744
B to Z ↓	0.0401	0.0666	5.4991	2.6719
B to Z ↑	0.0377	0.0615	8.8188	3.9747
C to Z ↓	0.0690	0.0649	5.4869	2.6719
C to Z ↑	0.0666	0.0593	8.7979	3.9763
	X17_P10	**X24_P10**	**X17_P10**	**X24_P10**
A to Z ↓	0.0604	0.0705	1.2773	0.9211
A to Z ↑	0.0601	0.0532	1.9330	1.3092
B to Z ↓	0.0604	0.0708	1.2778	0.9207

B to Z ↑	0.0602	0.0533	1.9350	1.3099
C to Z ↓	0.0594	0.0685	1.2785	0.9208
C to Z ↑	0.0591	0.0524	1.9341	1.3097

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P10	2.111e-05	1.000e-20
X8_P10	1.677e-05	1.000e-20
X17_P10	3.217e-05	1.000e-20
X24_P10	5.157e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	2.221e-03	3.292e-03	5.204e-03	8.823e-03
B to Z	2.260e-03	3.266e-03	5.192e-03	8.805e-03
C to Z	4.524e-03	3.202e-03	5.189e-03	8.753e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X4_P10	X8_P10	X17_P10	X24_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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