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C28SOI_SC_12_CLK_LR Databook

12 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

Overview

- C28SOI_SC_12_CLK_LR is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 332 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

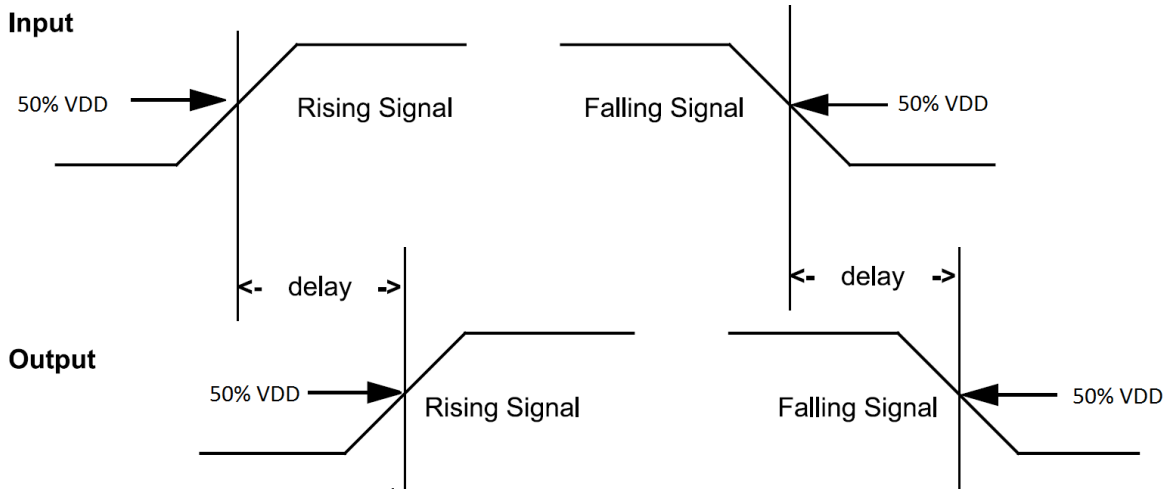


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

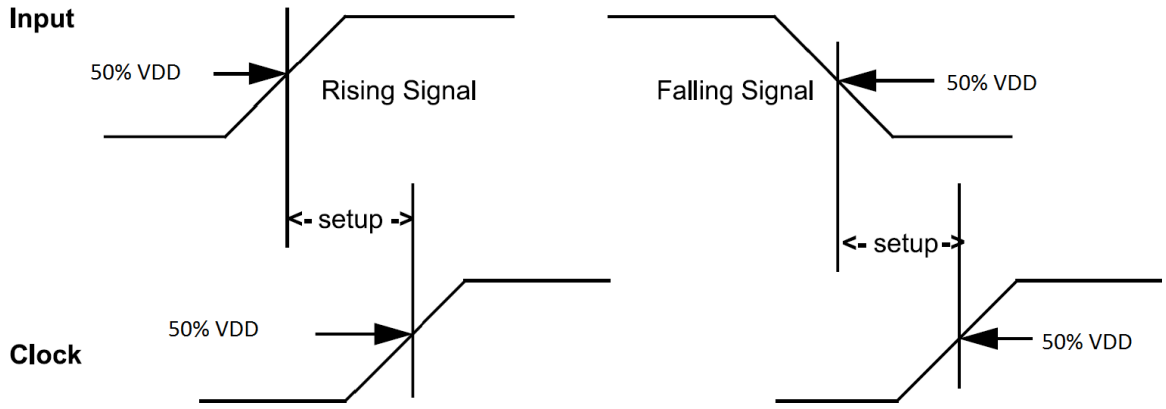


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

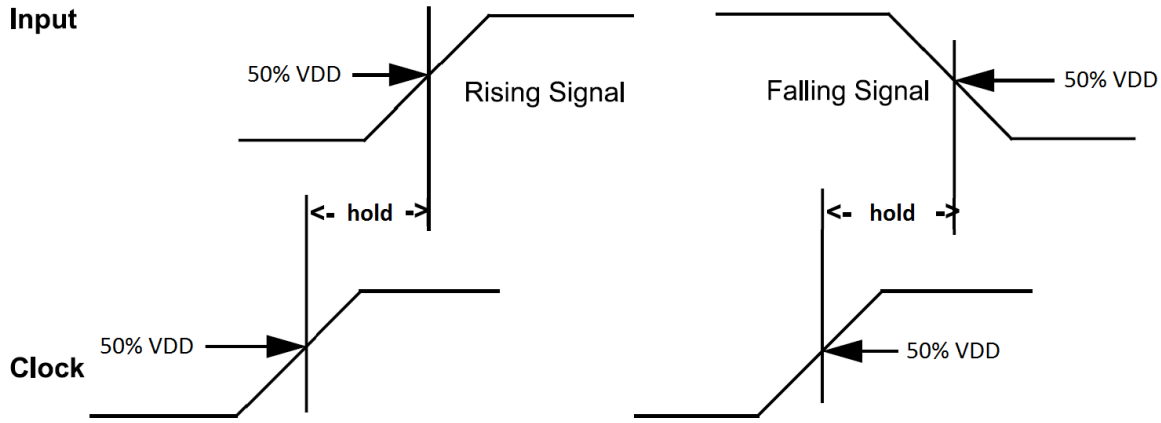


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

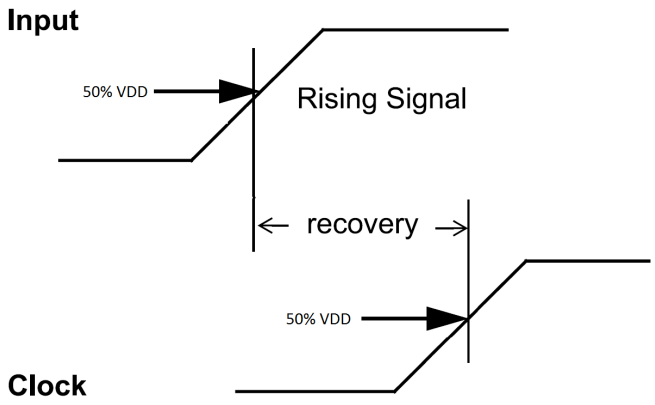


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

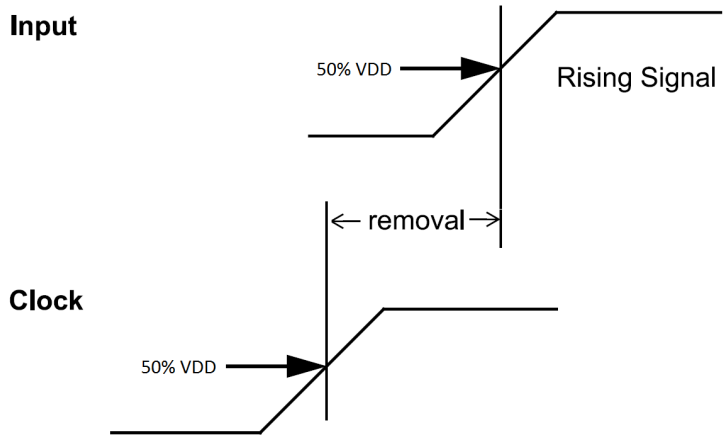


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

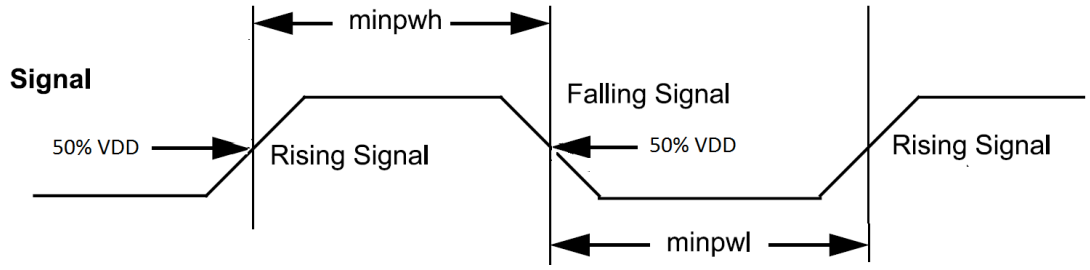


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

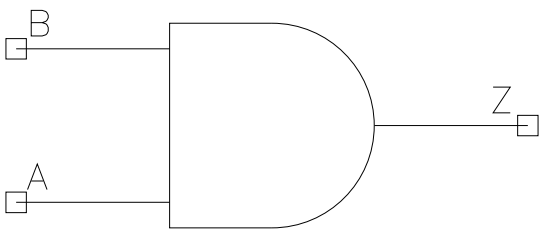
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

CNAND2

Cell Description

2 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.680	0.8160
X15_P4	1.200	0.680	0.8160
X15_P10	1.200	0.680	0.8160
X15_P16	1.200	0.680	0.8160
X20_P0	1.200	0.816	0.9792
X20_P4	1.200	0.816	0.9792
X20_P10	1.200	0.816	0.9792
X20_P16	1.200	0.816	0.9792
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0009	0.0010	0.0011	0.0011
B	0.0009	0.0009	0.0010	0.0011
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0009	0.0010	0.0011	0.0011
B	0.0009	0.0009	0.0010	0.0011
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0016	0.0017	0.0018	0.0019
B	0.0016	0.0016	0.0018	0.0019

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0216	0.0244	0.9038	0.9676
A to Z ↑	0.0163	0.0182	1.1151	1.2402
B to Z ↓	0.0205	0.0233	0.9024	0.9670
B to Z ↑	0.0175	0.0196	1.1141	1.2394
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0288	0.0332	1.0611	1.1467
A to Z ↑	0.0212	0.0245	1.4427	1.6390
B to Z ↓	0.0272	0.0315	1.0614	1.1467
B to Z ↑	0.0228	0.0262	1.4427	1.6401
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0245	0.0278	0.6660	0.7136
A to Z ↑	0.0190	0.0213	0.8222	0.9147
B to Z ↓	0.0236	0.0267	0.6659	0.7130
B to Z ↑	0.0205	0.0229	0.8215	0.9143
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0328	0.0379	0.7847	0.8487
A to Z ↑	0.0249	0.0286	1.0638	1.2103
B to Z ↓	0.0314	0.0363	0.7839	0.8472
B to Z ↑	0.0267	0.0306	1.0637	1.2087
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0239	0.0272	0.3847	0.4119
A to Z ↑	0.0163	0.0185	0.5647	0.6269
B to Z ↓	0.0220	0.0248	0.3839	0.4104
B to Z ↑	0.0171	0.0193	0.5646	0.6269
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0320	0.0369	0.4513	0.4871
A to Z ↑	0.0218	0.0251	0.7293	0.8268
B to Z ↓	0.0292	0.0336	0.4496	0.4850
B to Z ↑	0.0226	0.0259	0.7289	0.8268

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X15_P0	1.124e-04	1.310e-09
X15_P4	3.042e-05	1.310e-09
X15_P10	9.455e-06	1.310e-09
X15_P16	5.519e-06	1.310e-09
X20_P0	1.411e-04	1.476e-09
X20_P4	3.712e-05	1.476e-09
X20_P10	1.136e-05	1.476e-09
X20_P16	6.651e-06	1.476e-09
X33_P0	2.208e-04	2.139e-09
X33_P4	6.219e-05	2.139e-09
X33_P10	2.003e-05	2.139e-09
X33_P16	1.193e-05	2.139e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	3.194e-05	2.864e-05	2.602e-05	2.389e-05
B (output stable)	4.031e-05	4.106e-05	4.051e-05	5.192e-05
A to Z	5.726e-03	5.413e-03	5.263e-03	5.371e-03

B to Z	5.582e-03	5.218e-03	5.006e-03	5.077e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	3.266e-05	2.899e-05	2.649e-05	2.437e-05
B (output stable)	4.084e-05	4.117e-05	4.091e-05	5.311e-05
A to Z	7.829e-03	7.394e-03	7.205e-03	7.338e-03
B to Z	7.716e-03	7.208e-03	6.951e-03	7.042e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.249e-04	1.114e-04	9.975e-05	9.226e-05
B (output stable)	2.539e-04	2.571e-04	3.597e-04	4.221e-04
A to Z	1.203e-02	1.144e-02	1.119e-02	1.135e-02
B to Z	1.138e-02	1.065e-02	1.027e-02	1.032e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

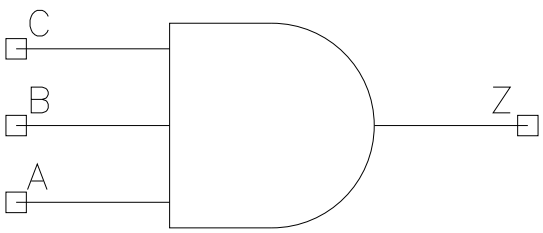
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	7.844e-08	7.193e-08	4.292e-08	8.400e-09
B (output stable)	9.110e-08	8.190e-08	4.330e-08	5.810e-08
A to Z	1.112e-06	5.801e-07	-1.504e-08	-1.791e-07
B to Z	4.937e-07	3.418e-07	5.100e-08	-1.945e-07
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	9.293e-08	7.371e-08	5.410e-08	1.850e-08
B (output stable)	9.300e-08	8.460e-08	5.550e-08	6.370e-08
A to Z	5.705e-07	3.890e-08	-4.708e-07	-2.906e-07
B to Z	1.038e-07	2.013e-07	-2.234e-07	-9.800e-08
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	9.500e-08	7.470e-08	4.100e-08	1.200e-09
B (output stable)	7.210e-08	6.000e-08	3.460e-08	-3.250e-08
A to Z	1.987e-06	6.124e-07	-1.244e-07	-3.242e-07
B to Z	1.229e-06	3.329e-07	4.800e-09	-6.820e-08

CNAND3

Cell Description

3 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X25_P0	1.200	1.360	1.6320
X25_P4	1.200	1.360	1.6320
X25_P10	1.200	1.360	1.6320
X25_P16	1.200	1.360	1.6320
X33_P0	1.200	1.768	2.1216
X33_P4	1.200	1.768	2.1216
X33_P10	1.200	1.768	2.1216
X33_P16	1.200	1.768	2.1216

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0009	0.0010	0.0010	0.0011
B	0.0009	0.0009	0.0010	0.0010
C	0.0009	0.0009	0.0010	0.0011
	X25_P0	X25_P4	X25_P10	X25_P16
A	0.0018	0.0019	0.0021	0.0022
B	0.0016	0.0017	0.0019	0.0020
C	0.0016	0.0017	0.0018	0.0020
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0021	0.0023	0.0024	0.0026
B	0.0020	0.0021	0.0023	0.0024

C	0.0019	0.0020	0.0022	0.0024

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0284	0.0320	0.7476	0.8020
A to Z ↑	0.0238	0.0266	0.8028	0.8920
B to Z ↓	0.0276	0.0310	0.7471	0.8018
B to Z ↑	0.0251	0.0278	0.8022	0.8925
C to Z ↓	0.0266	0.0298	0.7465	0.8004
C to Z ↑	0.0259	0.0287	0.8017	0.8922
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
A to Z ↓	0.0381	0.0439	0.8801	0.9532
A to Z ↑	0.0317	0.0366	1.0391	1.1804
B to Z ↓	0.0368	0.0424	0.8794	0.9524
B to Z ↑	0.0326	0.0373	1.0395	1.1810
C to Z ↓	0.0353	0.0405	0.8781	0.9509
C to Z ↑	0.0336	0.0382	1.0388	1.1807
	X25_P0	**X25_P4**	**X25_P0**	**X25_P4**
A to Z ↓	0.0212	0.0240	0.5172	0.5519
A to Z ↑	0.0182	0.0204	0.7632	0.8473
B to Z ↓	0.0202	0.0229	0.5164	0.5520
B to Z ↑	0.0195	0.0216	0.7632	0.8475
C to Z ↓	0.0190	0.0214	0.5159	0.5509
C to Z ↑	0.0202	0.0223	0.7635	0.8471
	X25_P10	**X25_P16**	**X25_P10**	**X25_P16**
A to Z ↓	0.0284	0.0327	0.6043	0.6511
A to Z ↑	0.0243	0.0282	0.9836	1.1143
B to Z ↓	0.0271	0.0311	0.6031	0.6510
B to Z ↑	0.0253	0.0290	0.9830	1.1150
C to Z ↓	0.0253	0.0290	0.6021	0.6497
C to Z ↑	0.0261	0.0298	0.9830	1.1151
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0229	0.0259	0.3701	0.3967
A to Z ↑	0.0207	0.0231	0.3942	0.4373
B to Z ↓	0.0220	0.0248	0.3696	0.3961
B to Z ↑	0.0222	0.0244	0.3940	0.4375
C to Z ↓	0.0211	0.0237	0.3691	0.3963
C to Z ↑	0.0232	0.0254	0.3934	0.4368
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0307	0.0353	0.4353	0.4711
A to Z ↑	0.0274	0.0315	0.5082	0.5756
B to Z ↓	0.0294	0.0337	0.4352	0.4705
B to Z ↑	0.0284	0.0324	0.5083	0.5761
C to Z ↓	0.0280	0.0321	0.4350	0.4698
C to Z ↑	0.0295	0.0334	0.5080	0.5761

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P0	1.343e-04	1.642e-09
X17_P4	3.217e-05	1.642e-09

X17_P10	9.701e-06	1.642e-09
X17_P16	6.057e-06	1.642e-09
X25_P0	1.626e-04	2.139e-09
X25_P4	4.301e-05	2.139e-09
X25_P10	1.434e-05	2.139e-09
X25_P16	9.384e-06	2.139e-09
X33_P0	2.737e-04	2.635e-09
X33_P4	6.709e-05	2.635e-09
X33_P10	2.065e-05	2.635e-09
X33_P16	1.303e-05	2.635e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	3.840e-05	3.477e-05	3.245e-05	2.980e-05
B (output stable)	4.600e-05	4.691e-05	7.277e-05	8.755e-05
C (output stable)	8.124e-05	9.299e-05	1.410e-04	1.642e-04
A to Z	8.867e-03	8.243e-03	8.142e-03	8.134e-03
B to Z	8.669e-03	8.009e-03	7.859e-03	7.815e-03
C to Z	8.509e-03	7.788e-03	7.576e-03	7.495e-03
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	7.188e-05	6.497e-05	5.976e-05	5.443e-05
B (output stable)	8.956e-05	8.949e-05	1.386e-04	1.678e-04
C (output stable)	1.645e-04	1.882e-04	2.832e-04	3.323e-04
A to Z	1.032e-02	9.807e-03	9.759e-03	9.966e-03
B to Z	9.870e-03	9.302e-03	9.180e-03	9.316e-03
C to Z	9.504e-03	8.842e-03	8.616e-03	8.678e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	8.750e-05	7.775e-05	7.200e-05	6.714e-05
B (output stable)	1.096e-04	1.125e-04	1.720e-04	2.057e-04
C (output stable)	2.059e-04	2.381e-04	3.528e-04	4.089e-04
A to Z	1.688e-02	1.587e-02	1.563e-02	1.579e-02
B to Z	1.638e-02	1.529e-02	1.494e-02	1.503e-02
C to Z	1.597e-02	1.476e-02	1.427e-02	1.426e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	1.017e-07	8.304e-08	6.600e-08	3.701e-08
B (output stable)	9.590e-08	8.923e-08	7.333e-08	3.887e-08
C (output stable)	1.043e-07	9.300e-08	6.177e-08	5.517e-08
A to Z	1.655e-07	9.880e-08	-1.930e-08	-1.340e-07
B to Z	8.240e-08	-4.790e-08	-1.710e-07	-2.683e-07
C to Z	1.272e-07	2.160e-07	-1.312e-07	-1.511e-07
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	6.883e-08	3.517e-08	-1.073e-08	-6.243e-08
B (output stable)	8.467e-08	4.927e-08	8.733e-09	-6.537e-08
C (output stable)	8.573e-08	6.007e-08	1.473e-08	-2.797e-08
A to Z	1.184e-06	6.209e-07	2.644e-08	-3.621e-07
B to Z	-3.865e-07	-2.753e-08	-2.589e-07	-3.464e-07
C to Z	-5.561e-07	-1.112e-07	-1.400e-07	-2.889e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	6.580e-08	3.633e-09	-3.747e-08	-9.947e-08

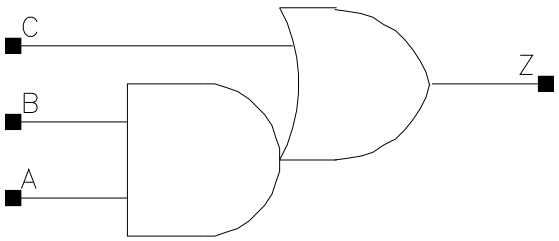
B (output stable)	6.903e-08	4.021e-08	-1.470e-08	-1.014e-07
C (output stable)	6.796e-08	3.761e-08	-6.200e-09	-7.043e-08
A to Z	4.168e-07	5.516e-07	-5.300e-08	-8.064e-07
B to Z	-2.582e-07	2.884e-07	-8.555e-07	-9.837e-07
C to Z	1.380e-08	7.094e-08	-4.417e-07	-4.485e-07

CNAO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	1.632	1.9584
X33_P4	1.200	1.632	1.9584
X33_P10	1.200	1.632	1.9584
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0019	0.0021	0.0022	0.0023
B	0.0017	0.0018	0.0020	0.0021
C	0.0017	0.0017	0.0019	0.0020

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0246	0.0281	0.3875	0.4150
A to Z ↑	0.0203	0.0228	0.5637	0.6266
B to Z ↓	0.0235	0.0268	0.3872	0.4145
B to Z ↑	0.0218	0.0245	0.5630	0.6257
C to Z ↓	0.0237	0.0275	0.3867	0.4138
C to Z ↑	0.0230	0.0257	0.5612	0.6236
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0333	0.0381	0.4557	0.4925

A to Z ↑	0.0266	0.0304	0.7286	0.8260
B to Z ↓	0.0315	0.0359	0.4546	0.4915
B to Z ↑	0.0284	0.0321	0.7285	0.8260
C to Z ↓	0.0329	0.0380	0.4539	0.4905
C to Z ↑	0.0297	0.0335	0.7249	0.8214

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X33_P0	2.612e-04	2.470e-09
X33_P4	8.211e-05	2.470e-09
X33_P10	2.665e-05	2.470e-09
X33_P16	1.469e-05	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	2.250e-04	1.511e-04	9.280e-05	5.638e-05
B (output stable)	2.556e-04	1.838e-04	1.427e-04	1.462e-04
C (output stable)	3.008e-04	2.959e-04	2.986e-04	2.996e-04
A to Z	1.287e-02	1.221e-02	1.187e-02	1.185e-02
B to Z	1.253e-02	1.175e-02	1.129e-02	1.119e-02
C to Z	1.378e-02	1.324e-02	1.310e-02	1.322e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

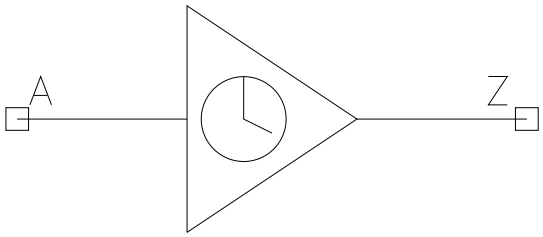
Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.328e-06	3.745e-05	5.959e-05	3.441e-05
B (output stable)	1.237e-06	3.834e-05	6.020e-05	6.159e-05
C (output stable)	1.400e-06	6.802e-07	-6.768e-06	-1.254e-05
A to Z	-3.226e-07	-3.218e-07	-6.621e-07	-8.638e-07
B to Z	-4.233e-07	-1.129e-07	-5.515e-07	-1.041e-06
C to Z	5.723e-07	1.220e-06	-7.750e-07	-4.787e-06

CNBF

Cell Description

Buffer with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X4_P4	1.200	0.408	0.4896
X4_P10	1.200	0.408	0.4896
X4_P16	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X15_P0	1.200	0.544	0.6528
X15_P4	1.200	0.544	0.6528
X15_P10	1.200	0.544	0.6528
X15_P16	1.200	0.544	0.6528
X22_P0	1.200	0.680	0.8160
X22_P4	1.200	0.680	0.8160
X22_P10	1.200	0.680	0.8160
X22_P16	1.200	0.680	0.8160
X30_P0	1.200	0.952	1.1424
X30_P4	1.200	0.952	1.1424
X30_P10	1.200	0.952	1.1424
X30_P16	1.200	0.952	1.1424
X38_P0	1.200	1.088	1.3056
X38_P4	1.200	1.088	1.3056
X38_P10	1.200	1.088	1.3056
X38_P16	1.200	1.088	1.3056
X44_P0	1.200	1.224	1.4688
X44_P4	1.200	1.224	1.4688
X44_P10	1.200	1.224	1.4688
X44_P16	1.200	1.224	1.4688
X52_P0	1.200	1.496	1.7952
X52_P4	1.200	1.496	1.7952
X52_P10	1.200	1.496	1.7952
X52_P16	1.200	1.496	1.7952
X59_P0	1.200	1.632	1.9584

X59_P4	1.200	1.632	1.9584
X59_P10	1.200	1.632	1.9584
X59_P16	1.200	1.632	1.9584
X70_P0	1.200	1.768	2.1216
X70_P4	1.200	1.768	2.1216
X70_P10	1.200	1.768	2.1216
X70_P16	1.200	1.768	2.1216
X94_P0	1.200	2.312	2.7744
X94_P4	1.200	2.312	2.7744
X94_P10	1.200	2.312	2.7744
X94_P16	1.200	2.312	2.7744
X133_P0	1.200	3.264	3.9168
X133_P4	1.200	3.264	3.9168
X133_P10	1.200	3.264	3.9168
X133_P16	1.200	3.264	3.9168

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X4_P4	X4_P10	X4_P16
A	0.0007	0.0007	0.0008	0.0008
	X7_P0	X7_P4	X7_P10	X7_P16
A	0.0007	0.0007	0.0008	0.0008
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0009	0.0010	0.0010	0.0011
	X22_P0	X22_P4	X22_P10	X22_P16
A	0.0011	0.0011	0.0012	0.0013
	X30_P0	X30_P4	X30_P10	X30_P16
A	0.0015	0.0016	0.0017	0.0019
	X38_P0	X38_P4	X38_P10	X38_P16
A	0.0018	0.0019	0.0021	0.0022
	X44_P0	X44_P4	X44_P10	X44_P16
A	0.0019	0.0020	0.0022	0.0023
	X52_P0	X52_P4	X52_P10	X52_P16
A	0.0025	0.0026	0.0028	0.0031
	X59_P0	X59_P4	X59_P10	X59_P16
A	0.0028	0.0029	0.0032	0.0035
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0029	0.0031	0.0033	0.0036
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0039	0.0041	0.0044	0.0047
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0058	0.0061	0.0065	0.0071

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X4_P4	X4_P0	X4_P4
A to Z ↓	0.0207	0.0233	3.1518	3.3809

A to Z ↑	0.0147	0.0166	4.0059	4.4403
	X4_P10	**X4_P16**	**X4_P10**	**X4_P16**
A to Z ↓	0.0273	0.0310	3.7151	4.0192
A to Z ↑	0.0196	0.0223	5.1687	5.8806
	X7_P0	**X7_P4**	**X7_P0**	**X7_P4**
A to Z ↓	0.0206	0.0233	1.7592	1.8798
A to Z ↑	0.0144	0.0165	2.3787	2.6392
	X7_P10	**X7_P16**	**X7_P10**	**X7_P16**
A to Z ↓	0.0274	0.0313	2.0620	2.2247
A to Z ↑	0.0194	0.0221	3.0738	3.4915
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0200	0.0227	0.9179	0.9829
A to Z ↑	0.0156	0.0175	1.1086	1.2330
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0266	0.0307	1.0766	1.1633
A to Z ↑	0.0204	0.0233	1.4365	1.6306
	X22_P0	**X22_P4**	**X22_P0**	**X22_P4**
A to Z ↓	0.0205	0.0235	0.6270	0.6714
A to Z ↑	0.0165	0.0187	0.7454	0.8303
	X22_P10	**X22_P16**	**X22_P10**	**X22_P16**
A to Z ↓	0.0273	0.0315	0.7359	0.7959
A to Z ↑	0.0216	0.0246	0.9655	1.0968
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**
A to Z ↓	0.0194	0.0219	0.4394	0.4704
A to Z ↑	0.0147	0.0165	0.5585	0.6207
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
A to Z ↓	0.0257	0.0296	0.5164	0.5584
A to Z ↑	0.0193	0.0221	0.7225	0.8196
	X38_P0	**X38_P4**	**X38_P0**	**X38_P4**
A to Z ↓	0.0193	0.0219	0.3538	0.3790
A to Z ↑	0.0149	0.0168	0.4487	0.4980
	X38_P10	**X38_P16**	**X38_P10**	**X38_P16**
A to Z ↓	0.0259	0.0298	0.4157	0.4492
A to Z ↑	0.0197	0.0225	0.5798	0.6575
	X44_P0	**X44_P4**	**X44_P0**	**X44_P4**
A to Z ↓	0.0198	0.0224	0.3052	0.3267
A to Z ↑	0.0154	0.0173	0.3936	0.4372
	X44_P10	**X44_P16**	**X44_P10**	**X44_P16**
A to Z ↓	0.0265	0.0305	0.3587	0.3878
A to Z ↑	0.0203	0.0231	0.5091	0.5774
	X52_P0	**X52_P4**	**X52_P0**	**X52_P4**
A to Z ↓	0.0193	0.0220	0.2632	0.2820
A to Z ↑	0.0162	0.0183	0.3292	0.3659
	X52_P10	**X52_P16**	**X52_P10**	**X52_P16**
A to Z ↓	0.0259	0.0297	0.3089	0.3338
A to Z ↑	0.0212	0.0241	0.4251	0.4820
	X59_P0	**X59_P4**	**X59_P0**	**X59_P4**
A to Z ↓	0.0195	0.0219	0.2302	0.2468
A to Z ↑	0.0153	0.0171	0.2920	0.3237
	X59_P10	**X59_P16**	**X59_P10**	**X59_P16**
A to Z ↓	0.0259	0.0296	0.2708	0.2923
A to Z ↑	0.0200	0.0227	0.3764	0.4269

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0206	0.0233	0.1933	0.2069
A to Z ↑	0.0160	0.0180	0.2525	0.2802
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0274	0.0314	0.2269	0.2456
A to Z ↑	0.0210	0.0238	0.3264	0.3699
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0204	0.0230	0.1476	0.1582
A to Z ↑	0.0160	0.0178	0.1923	0.2134
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0270	0.0308	0.1739	0.1878
A to Z ↑	0.0208	0.0235	0.2479	0.2808
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0208	0.0232	0.1090	0.1173
A to Z ↑	0.0165	0.0184	0.1397	0.1553
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0272	0.0310	0.1291	0.1399
A to Z ↑	0.0214	0.0242	0.1802	0.2042

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X4_P0	4.269e-05	9.792e-10
X4_P4	1.339e-05	9.792e-10
X4_P10	4.220e-06	9.792e-10
X4_P16	2.229e-06	9.792e-10
X7_P0	6.497e-05	9.792e-10
X7_P4	2.007e-05	9.792e-10
X7_P10	6.285e-06	9.792e-10
X7_P16	3.312e-06	9.792e-10
X15_P0	1.158e-04	1.145e-09
X15_P4	3.420e-05	1.145e-09
X15_P10	1.048e-05	1.145e-09
X15_P16	5.539e-06	1.145e-09
X22_P0	1.632e-04	1.310e-09
X22_P4	4.732e-05	1.310e-09
X22_P10	1.436e-05	1.310e-09
X22_P16	7.613e-06	1.310e-09
X30_P0	2.194e-04	1.642e-09
X30_P4	6.481e-05	1.642e-09
X30_P10	1.991e-05	1.642e-09
X30_P16	1.063e-05	1.642e-09
X38_P0	2.711e-04	1.807e-09
X38_P4	7.955e-05	1.807e-09
X38_P10	2.435e-05	1.807e-09
X38_P16	1.301e-05	1.807e-09
X44_P0	3.100e-04	1.973e-09
X44_P4	8.993e-05	1.973e-09
X44_P10	2.738e-05	1.973e-09
X44_P16	1.462e-05	1.973e-09
X52_P0	3.608e-04	2.304e-09
X52_P4	1.053e-04	2.304e-09
X52_P10	3.214e-05	2.304e-09

X52_P16	1.722e-05	2.304e-09
X59_P0	4.215e-04	2.470e-09
X59_P4	1.220e-04	2.470e-09
X59_P10	3.712e-05	2.470e-09
X59_P16	1.986e-05	2.470e-09
X70_P0	4.754e-04	2.635e-09
X70_P4	1.401e-04	2.635e-09
X70_P10	4.302e-05	2.635e-09
X70_P16	2.310e-05	2.635e-09
X94_P0	6.282e-04	3.298e-09
X94_P4	1.848e-04	3.298e-09
X94_P10	5.673e-05	3.298e-09
X94_P16	3.049e-05	3.298e-09
X133_P0	8.888e-04	4.457e-09
X133_P4	2.623e-04	4.457e-09
X133_P10	8.066e-05	4.457e-09
X133_P16	4.344e-05	4.457e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	2.237e-03	2.108e-03	2.069e-03	2.086e-03
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	3.001e-03	2.841e-03	2.778e-03	2.808e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	5.351e-03	4.972e-03	4.815e-03	4.886e-03
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	7.867e-03	7.445e-03	7.136e-03	7.239e-03
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	1.025e-02	9.539e-03	9.215e-03	9.341e-03
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	1.287e-02	1.200e-02	1.172e-02	1.186e-02
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	1.456e-02	1.352e-02	1.316e-02	1.330e-02
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	1.786e-02	1.668e-02	1.615e-02	1.629e-02
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	2.011e-02	1.869e-02	1.814e-02	1.827e-02
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	2.366e-02	2.213e-02	2.144e-02	2.162e-02
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	3.141e-02	2.936e-02	2.834e-02	2.833e-02
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	4.840e-02	4.559e-02	4.392e-02	4.357e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	1.516e-07	7.707e-07	1.522e-07	-6.860e-08
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	2.026e-06	-5.270e-08	1.387e-07	-1.479e-07
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	1.228e-06	6.043e-07	1.407e-07	-2.806e-08

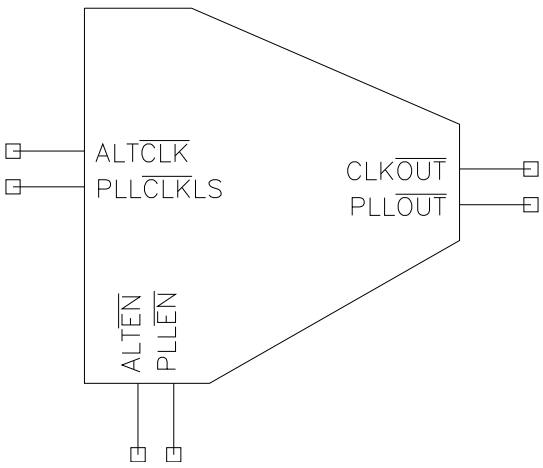
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	1.448e-06	6.646e-07	-5.930e-08	-2.165e-07
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	4.156e-06	1.568e-06	2.526e-07	-2.008e-07
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	4.804e-06	2.205e-06	1.790e-07	-1.410e-07
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	-8.760e-07	1.391e-06	1.410e-07	-6.450e-07
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	2.365e-06	-5.920e-07	-1.630e-07	-7.520e-07
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	5.627e-06	2.338e-06	1.907e-07	-6.209e-07
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	6.497e-06	1.704e-06	1.800e-08	-1.122e-06
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	5.525e-06	2.134e-06	1.770e-07	-1.108e-06
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	6.317e-06	3.471e-06	7.690e-07	-1.579e-06

CNGFMUX21

Cell Description

2:1 Glitch-free MUX for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	2.400	2.856	6.8544
X15_P4	2.400	2.856	6.8544
X15_P10	2.400	2.856	6.8544
X15_P16	2.400	2.856	6.8544
X30_P0	2.400	3.944	9.4656
X30_P4	2.400	3.944	9.4656
X30_P10	2.400	3.944	9.4656
X30_P16	2.400	3.944	9.4656

Truth Table

PLL_CLK_LS	ALT_CLK	IPLL_EN_LD	IALT_EN_LD	CLK_OUT
0	-	-	0	0
0	0	-	-	0
-	0	0	-	0
PLL_CLK_LS	1	-	1	1
1	ALT_CLK	1	-	1
1	1	0	0	0

PLL_CLK_LS	PLL_OUT
PLL_CLK_LS	PLL_CLK_LS
1	1

PLL_EN	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

PLL_EN	0	-	PLL_EN
-	-	IPLL_EN_LD	IPLL_EN_LD
-	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

ALT_EN	ALT_CLK	IALT_EN_LD	IALT_EN_LD
ALT_EN	0	-	ALT_EN
-	-	IALT_EN_LD	IALT_EN_LD
-	ALT_CLK	IALT_EN_LD	IALT_EN_LD

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK	0.0025	0.0026	0.0028	0.0030
ALT_EN	0.0006	0.0006	0.0007	0.0007
PLL_CLK_LS	0.0034	0.0036	0.0038	0.0040
PLL_EN	0.0006	0.0006	0.0006	0.0007
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK	0.0039	0.0041	0.0044	0.0047
ALT_EN	0.0006	0.0006	0.0007	0.0007
PLL_CLK_LS	0.0053	0.0056	0.0060	0.0064
PLL_EN	0.0006	0.0006	0.0006	0.0007

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
ALT_CLK to CLK_OUT ↓	0.0263	0.0295	0.8912	0.9566
ALT_CLK to CLK_OUT ↑	0.0178	0.0203	1.2958	1.4411
PLL_CLK_LS to CLK_OUT ↓	0.0240	0.0268	0.8947	0.9615
PLL_CLK_LS to CLK_OUT ↑	0.0174	0.0197	1.2972	1.4416
PLL_CLK_LS to PLL_OUT ↓	0.0203	0.0230	0.8727	0.9341
PLL_CLK_LS to PLL_OUT ↑	0.0158	0.0179	1.1126	1.2369
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
ALT_CLK to CLK_OUT ↓	0.0347	0.0398	1.0577	1.1524
ALT_CLK to CLK_OUT ↑	0.0245	0.0285	1.6789	1.9079
PLL_CLK_LS to CLK_OUT ↓	0.0312	0.0355	1.0618	1.1563
PLL_CLK_LS to CLK_OUT ↑	0.0234	0.0268	1.6810	1.9097
PLL_CLK_LS to PLL_OUT ↓	0.0271	0.0312	1.0237	1.1054
PLL_CLK_LS to PLL_OUT ↑	0.0209	0.0237	1.4398	1.6336
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**

ALT_CLK to CLK_OUT ↓	0.0256	0.0287	0.4617	0.4954
ALT_CLK to CLK_OUT ↑	0.0180	0.0205	0.5842	0.6487
PLL_CLK_LS to CLK_OUT ↓	0.0238	0.0265	0.4660	0.4999
PLL_CLK_LS to CLK_OUT ↑	0.0184	0.0206	0.5866	0.6518
PLL_CLK_LS to PLL_OUT ↓	0.0177	0.0201	0.4416	0.4730
PLL_CLK_LS to PLL_OUT ↑	0.0137	0.0155	0.5590	0.6216
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
ALT_CLK to CLK_OUT ↓	0.0337	0.0382	0.5464	0.5946
ALT_CLK to CLK_OUT ↑	0.0246	0.0284	0.7547	0.8557
PLL_CLK_LS to CLK_OUT ↓	0.0308	0.0348	0.5511	0.5991
PLL_CLK_LS to CLK_OUT ↑	0.0242	0.0275	0.7575	0.8595
PLL_CLK_LS to PLL_OUT ↓	0.0235	0.0271	0.5178	0.5594
PLL_CLK_LS to PLL_OUT ↑	0.0180	0.0207	0.7223	0.8197

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0471	0.0519	0.0577	0.0672
ALT_EN ↓	hold_rising to ALT_CLK	-0.0152	-0.0170	-0.0247	-0.0314
ALT_EN ↑	hold_rising to ALT_CLK	0.0058	0.0009	-0.0016	-0.0064
ALT_EN ↓	setup_rising to ALT_CLK	0.0399	0.0448	0.0545	0.0612
ALT_EN ↑	setup_rising to ALT_CLK	0.0221	0.0242	0.0291	0.0365
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0471	0.0519	0.0577	0.0672
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0152	-0.0201	-0.0268	-0.0369
PLL_EN ↑	hold_rising to PLL_CLK_LS	0.0058	0.0009	-0.0016	-0.0064
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0399	0.0448	0.0545	0.0612
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0220	0.0242	0.0294	0.0365
		X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0471	0.0519	0.0577	0.0672
ALT_EN ↓	hold_rising to ALT_CLK	-0.0152	-0.0170	-0.0247	-0.0321

ALT_EN ↑	hold_rising to ALT_CLK	0.0058	0.0006	-0.0016	-0.0064
ALT_EN ↓	setup_rising to ALT_CLK	0.0399	0.0448	0.0545	0.0612
ALT_EN ↑	setup_rising to ALT_CLK	0.0242	0.0295	0.0340	0.0411
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0471	0.0519	0.0577	0.0672
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0152	-0.0201	-0.0268	-0.0369
PLL_EN ↑	hold_rising to PLL_CLK_LS	0.0058	0.0006	-0.0046	-0.0064
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0399	0.0448	0.0545	0.0612
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0242	0.0294	0.0343	0.0414

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X15_P0	5.879e-04	5.272e-09
X15_P4	1.841e-04	5.272e-09
X15_P10	6.149e-05	5.272e-09
X15_P16	3.557e-05	5.272e-09
X30_P0	9.473e-04	6.913e-09
X30_P4	2.897e-04	6.913e-09
X30_P10	9.620e-05	6.913e-09
X30_P16	5.620e-05	6.913e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	4.938e-03	4.812e-03	4.835e-03	4.969e-03
ALT_EN (output stable)	3.373e-03	3.274e-03	3.323e-03	3.418e-03
PLL_CLK_LS (output stable)	1.461e-02	1.092e-02	9.855e-03	9.836e-03
PLL_EN (output stable)	3.464e-03	3.373e-03	3.394e-03	3.485e-03
ALT_CLK to CLK_OUT	1.056e-02	1.028e-02	1.038e-02	1.073e-02
PLL_CLK_LS to CLK_OUT	6.934e-03	6.577e-03	6.454e-03	6.533e-03
PLL_CLK_LS to PLL_OUT	1.519e-02	9.731e-03	7.982e-03	7.680e-03
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	6.256e-03	6.121e-03	6.186e-03	6.388e-03
ALT_EN (output stable)	3.683e-03	3.609e-03	3.689e-03	3.830e-03
PLL_CLK_LS (output stable)	2.306e-02	1.682e-02	1.518e-02	1.525e-02

PLL_EN (output stable)	3.912e-03	3.867e-03	3.973e-03	4.104e-03
ALT_CLK to CLK_OUT	1.875e-02	1.836e-02	1.866e-02	1.912e-02
PLL_CLK_LS to CLK_OUT	1.238e-02	1.177e-02	1.153e-02	1.168e-02
PLL_CLK_LS to PLL_OUT	2.604e-02	1.683e-02	1.392e-02	1.350e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

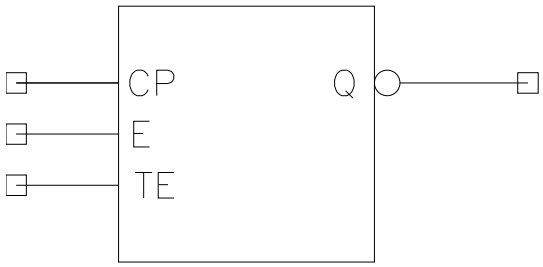
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	-1.242e-05	-1.125e-05	-9.373e-06	-8.213e-06
ALT_EN (output stable)	1.810e-07	1.697e-07	-2.236e-07	-1.111e-06
PLL_CLK_LS (output stable)	-1.506e-06	-1.686e-06	-8.657e-07	-2.801e-06
PLL_EN (output stable)	1.925e-07	1.933e-07	-2.135e-07	-1.175e-06
ALT_CLK to CLK_OUT	2.876e-05	2.646e-05	3.889e-05	2.837e-05
PLL_CLK_LS to CLK_OUT	1.950e-05	1.785e-05	1.833e-05	1.501e-05
PLL_CLK_LS to PLL_OUT	1.416e-05	1.278e-05	1.415e-05	1.229e-05
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	-3.568e-05	-3.020e-05	-2.326e-05	-2.548e-05
ALT_EN (output stable)	1.891e-07	1.813e-07	-1.996e-07	-1.106e-06
PLL_CLK_LS (output stable)	-5.609e-06	-9.908e-06	2.242e-05	1.927e-05
PLL_EN (output stable)	1.473e-07	1.482e-07	-2.647e-07	-1.224e-06
ALT_CLK to CLK_OUT	1.169e-04	1.266e-04	1.224e-04	1.173e-04
PLL_CLK_LS to CLK_OUT	7.809e-05	7.308e-05	6.744e-05	6.911e-05
PLL_CLK_LS to PLL_OUT	3.386e-05	3.454e-05	3.211e-05	2.873e-05

CNHLS

Cell Description

Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LRP_-CNHLSX7_P0	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX7_P4	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX7_P10	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX7_P16	1.200	1.768	2.1216
C12T28SOI_LRP_-CNHLSX15_P0	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX15_P4	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX15_P10	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX15_P16	1.200	1.904	2.2848
C12T28SOI_LRP_-CNHLSX22_P0	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX22_P4	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX22_P10	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX22_P16	1.200	2.312	2.7744
C12T28SOI_LRP_-CNHLSX29_P0	1.200	2.448	2.9376
C12T28SOI_LRP_-CNHLSX29_P4	1.200	2.448	2.9376
C12T28SOI_LRP_-CNHLSX29_P10	1.200	2.448	2.9376
C12T28SOI_LRP_-CNHLSX29_P16	1.200	2.448	2.9376

C12T28SOI_LRP_-CNHLSX36_P0	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX36_P4	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX36_P10	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX36_P16	1.200	2.584	3.1008
C12T28SOI_LRP_-CNHLSX51_P0	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX51_P4	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX51_P10	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX51_P16	1.200	3.128	3.7536
C12T28SOI_LRP_-CNHLSX58_P0	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX58_P4	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX58_P10	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX58_P16	1.200	3.808	4.5696
C12T28SOI_LRP_-CNHLSX71_P0	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX71_P4	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX71_P10	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX71_P16	1.200	4.352	5.2224
C12T28SOI_LRP_-CNHLSX93_P0	1.200	4.896	5.8752
C12T28SOI_LRP_-CNHLSX93_P4	1.200	4.896	5.8752
C12T28SOI_LRP_-CNHLSX93_P10	1.200	4.896	5.8752
C12T28SOI_LRP_-CNHLSX93_P16	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX29_P0	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX29_P4	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX29_P10	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX29_P16	1.200	2.992	3.5904
C12T28SOI_LRPHP_-CNHLSX36_P0	1.200	3.128	3.7536
C12T28SOI_LRPHP_-CNHLSX36_P4	1.200	3.128	3.7536

C12T28SOI_LRPHP_-CNHLSX36_P10	1.200	3.128	3.7536
C12T28SOI_LRPHP_-CNHLSX36_P16	1.200	3.128	3.7536
C12T28SOI_LRPHP_-CNHLSX44_P0	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX44_P4	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX44_P10	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX44_P16	1.200	3.536	4.2432
C12T28SOI_LRPHP_-CNHLSX51_P0	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX51_P4	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX51_P10	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX51_P16	1.200	3.672	4.4064
C12T28SOI_LRPHP_-CNHLSX58_P0	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX58_P4	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX58_P10	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX58_P16	1.200	4.352	5.2224
C12T28SOI_LRPHP_-CNHLSX71_P0	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX71_P4	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX71_P10	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX71_P16	1.200	4.896	5.8752
C12T28SOI_LRPHP_-CNHLSX86_P0	1.200	5.304	6.3648
C12T28SOI_LRPHP_-CNHLSX86_P4	1.200	5.304	6.3648
C12T28SOI_LRPHP_-CNHLSX86_P10	1.200	5.304	6.3648
C12T28SOI_LRPHP_-CNHLSX86_P16	1.200	5.304	6.3648

Truth Table

CP	E	TE	OLDIE	Q
0	-	-	-	0
1	-	-	OLDIE	OLDIE

OLDIE	OLDIE
OLDIE	OLDIE

Pin Capacitance

Pin	C12T28SOI_LRP_-CNHLSX7_P0	C12T28SOI_LRP_-CNHLSX7_P4	C12T28SOI_LRP_-CNHLSX7_P10	C12T28SOI_LRP_-CNHLSX7_P16
CP	0.0022	0.0022	0.0024	0.0025
E	0.0005	0.0006	0.0006	0.0006
TE	0.0010	0.0011	0.0012	0.0012
	C12T28SOI_LRP_-CNHLSX15_P0	C12T28SOI_LRP_-CNHLSX15_P4	C12T28SOI_LRP_-CNHLSX15_P10	C12T28SOI_LRP_-CNHLSX15_P16
CP	0.0028	0.0029	0.0030	0.0032
E	0.0005	0.0006	0.0006	0.0006
TE	0.0010	0.0011	0.0011	0.0012
	C12T28SOI_LRP_-CNHLSX22_P0	C12T28SOI_LRP_-CNHLSX22_P4	C12T28SOI_LRP_-CNHLSX22_P10	C12T28SOI_LRP_-CNHLSX22_P16
CP	0.0029	0.0031	0.0032	0.0034
E	0.0005	0.0006	0.0006	0.0006
TE	0.0010	0.0011	0.0011	0.0012
	C12T28SOI_LRP_-CNHLSX29_P0	C12T28SOI_LRP_-CNHLSX29_P4	C12T28SOI_LRP_-CNHLSX29_P10	C12T28SOI_LRP_-CNHLSX29_P16
CP	0.0031	0.0033	0.0035	0.0037
E	0.0005	0.0006	0.0006	0.0006
TE	0.0010	0.0011	0.0011	0.0012
	C12T28SOI_LRP_-CNHLSX36_P0	C12T28SOI_LRP_-CNHLSX36_P4	C12T28SOI_LRP_-CNHLSX36_P10	C12T28SOI_LRP_-CNHLSX36_P16
CP	0.0035	0.0036	0.0039	0.0041
E	0.0005	0.0006	0.0006	0.0006
TE	0.0010	0.0011	0.0011	0.0012
	C12T28SOI_LRP_-CNHLSX51_P0	C12T28SOI_LRP_-CNHLSX51_P4	C12T28SOI_LRP_-CNHLSX51_P10	C12T28SOI_LRP_-CNHLSX51_P16
CP	0.0042	0.0043	0.0045	0.0048
E	0.0005	0.0006	0.0006	0.0006
TE	0.0010	0.0011	0.0011	0.0012
	C12T28SOI_LRP_-CNHLSX58_P0	C12T28SOI_LRP_-CNHLSX58_P4	C12T28SOI_LRP_-CNHLSX58_P10	C12T28SOI_LRP_-CNHLSX58_P16
CP	0.0056	0.0059	0.0062	0.0066
E	0.0005	0.0006	0.0006	0.0006
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_LRP_-CNHLSX71_P0	C12T28SOI_LRP_-CNHLSX71_P4	C12T28SOI_LRP_-CNHLSX71_P10	C12T28SOI_LRP_-CNHLSX71_P16
CP	0.0064	0.0068	0.0072	0.0077
E	0.0005	0.0006	0.0006	0.0006
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_LRP_-CNHLSX93_P0	C12T28SOI_LRP_-CNHLSX93_P4	C12T28SOI_LRP_-CNHLSX93_P10	C12T28SOI_LRP_-CNHLSX93_P16
CP	0.0076	0.0080	0.0086	0.0092
E	0.0005	0.0006	0.0006	0.0006
TE	0.0010	0.0011	0.0011	0.0012
	C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP	0.0025	0.0027	0.0028	0.0030
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012

	C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP	0.0029	0.0030	0.0032	0.0034
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP	0.0034	0.0035	0.0037	0.0040
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP	0.0034	0.0035	0.0038	0.0040
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP	0.0046	0.0048	0.0052	0.0055
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012
	C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP	0.0056	0.0058	0.0062	0.0067
E	0.0006	0.0006	0.0007	0.0007
TE	0.0009	0.0010	0.0011	0.0012
	C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP	0.0067	0.0070	0.0075	0.0080
E	0.0006	0.0006	0.0007	0.0007
TE	0.0010	0.0010	0.0011	0.0012

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LRP_-CNHLSX7_P0	**C12T28SOI_LRP_-CNHLSX7_P4**	**C12T28SOI_LRP_-CNHLSX7_P0**	**C12T28SOI_LRP_-CNHLSX7_P4**
CP to Q ↓	0.0250	0.0282	1.8147	1.9417
CP to Q ↑	0.0167	0.0190	2.2255	2.4785
	C12T28SOI_LRP_-CNHLSX7_P10	**C12T28SOI_LRP_-CNHLSX7_P16**	**C12T28SOI_LRP_-CNHLSX7_P10**	**C12T28SOI_LRP_-CNHLSX7_P16**
CP to Q ↓	0.0330	0.0377	2.1345	2.3099
CP to Q ↑	0.0225	0.0258	2.8871	3.2782
	C12T28SOI_LRP_-CNHLSX15_P0	**C12T28SOI_LRP_-CNHLSX15_P4**	**C12T28SOI_LRP_-CNHLSX15_P0**	**C12T28SOI_LRP_-CNHLSX15_P4**
CP to Q ↓	0.0212	0.0237	0.9156	0.9801
CP to Q ↑	0.0161	0.0179	1.1213	1.2465
	C12T28SOI_LRP_-CNHLSX15_P10	**C12T28SOI_LRP_-CNHLSX15_P16**	**C12T28SOI_LRP_-CNHLSX15_P10**	**C12T28SOI_LRP_-CNHLSX15_P16**

CP to Q ↓	0.0278	0.0317	1.0760	1.1615
CP to Q ↑	0.0211	0.0240	1.4509	1.6461
	C12T28SOI_LRP_-CNHLSX22_P0	**C12T28SOI_LRP_-CNHLSX22_P4**	**C12T28SOI_LRP_-CNHLSX22_P0**	**C12T28SOI_LRP_-CNHLSX22_P4**
CP to Q ↓	0.0216	0.0241	0.6337	0.6786
CP to Q ↑	0.0175	0.0194	0.7548	0.8395
	C12T28SOI_LRP_-CNHLSX22_P10	**C12T28SOI_LRP_-CNHLSX22_P16**	**C12T28SOI_LRP_-CNHLSX22_P10**	**C12T28SOI_LRP_-CNHLSX22_P16**
CP to Q ↓	0.0284	0.0324	0.7444	0.8049
CP to Q ↑	0.0229	0.0261	0.9768	1.1087
	C12T28SOI_LRP_-CNHLSX29_P0	**C12T28SOI_LRP_-CNHLSX29_P4**	**C12T28SOI_LRP_-CNHLSX29_P0**	**C12T28SOI_LRP_-CNHLSX29_P4**
CP to Q ↓	0.0211	0.0238	0.4747	0.5077
CP to Q ↑	0.0172	0.0192	0.5661	0.6297
	C12T28SOI_LRP_-CNHLSX29_P10	**C12T28SOI_LRP_-CNHLSX29_P16**	**C12T28SOI_LRP_-CNHLSX29_P10**	**C12T28SOI_LRP_-CNHLSX29_P16**
CP to Q ↓	0.0279	0.0321	0.5573	0.6030
CP to Q ↑	0.0224	0.0257	0.7327	0.8313
	C12T28SOI_LRP_-CNHLSX36_P0	**C12T28SOI_LRP_-CNHLSX36_P4**	**C12T28SOI_LRP_-CNHLSX36_P0**	**C12T28SOI_LRP_-CNHLSX36_P4**
CP to Q ↓	0.0208	0.0235	0.3795	0.4065
CP to Q ↑	0.0172	0.0192	0.4541	0.5051
	C12T28SOI_LRP_-CNHLSX36_P10	**C12T28SOI_LRP_-CNHLSX36_P16**	**C12T28SOI_LRP_-CNHLSX36_P10**	**C12T28SOI_LRP_-CNHLSX36_P16**
CP to Q ↓	0.0276	0.0318	0.4461	0.4821
CP to Q ↑	0.0225	0.0257	0.5872	0.6659
	C12T28SOI_LRP_-CNHLSX51_P0	**C12T28SOI_LRP_-CNHLSX51_P4**	**C12T28SOI_LRP_-CNHLSX51_P0**	**C12T28SOI_LRP_-CNHLSX51_P4**
CP to Q ↓	0.0232	0.0261	0.2764	0.2965
CP to Q ↑	0.0177	0.0200	0.3262	0.3625
	C12T28SOI_LRP_-CNHLSX51_P10	**C12T28SOI_LRP_-CNHLSX51_P16**	**C12T28SOI_LRP_-CNHLSX51_P10**	**C12T28SOI_LRP_-CNHLSX51_P16**
CP to Q ↓	0.0306	0.0351	0.3250	0.3517
CP to Q ↑	0.0233	0.0266	0.4221	0.4787
	C12T28SOI_LRP_-CNHLSX58_P0	**C12T28SOI_LRP_-CNHLSX58_P4**	**C12T28SOI_LRP_-CNHLSX58_P0**	**C12T28SOI_LRP_-CNHLSX58_P4**
CP to Q ↓	0.0205	0.0230	0.2438	0.2609
CP to Q ↑	0.0153	0.0171	0.2871	0.3186
	C12T28SOI_LRP_-CNHLSX58_P10	**C12T28SOI_LRP_-CNHLSX58_P16**	**C12T28SOI_LRP_-CNHLSX58_P10**	**C12T28SOI_LRP_-CNHLSX58_P16**
CP to Q ↓	0.0268	0.0307	0.2859	0.3088
CP to Q ↑	0.0199	0.0229	0.3706	0.4201
	C12T28SOI_LRP_-CNHLSX71_P0	**C12T28SOI_LRP_-CNHLSX71_P4**	**C12T28SOI_LRP_-CNHLSX71_P0**	**C12T28SOI_LRP_-CNHLSX71_P4**
CP to Q ↓	0.0200	0.0226	0.2016	0.2160
CP to Q ↑	0.0156	0.0176	0.2337	0.2593
	C12T28SOI_LRP_-CNHLSX71_P10	**C12T28SOI_LRP_-CNHLSX71_P16**	**C12T28SOI_LRP_-CNHLSX71_P10**	**C12T28SOI_LRP_-CNHLSX71_P16**
CP to Q ↓	0.0264	0.0301	0.2371	0.2560
CP to Q ↑	0.0205	0.0233	0.3017	0.3416
	C12T28SOI_LRP_-CNHLSX93_P0	**C12T28SOI_LRP_-CNHLSX93_P4**	**C12T28SOI_LRP_-CNHLSX93_P0**	**C12T28SOI_LRP_-CNHLSX93_P4**
CP to Q ↓	0.0211	0.0238	0.1596	0.1710

CP to Q ↑	0.0171	0.0190	0.1848	0.2052
	C12T28SOI_LRP_-CNHLSX93_P10	**C12T28SOI_LRP_-CNHLSX93_P16**	**C12T28SOI_LRP_-CNHLSX93_P10**	**C12T28SOI_LRP_-CNHLSX93_P16**
CP to Q ↓	0.0276	0.0316	0.1876	0.2029
CP to Q ↑	0.0221	0.0252	0.2382	0.2698
	C12T28SOI_-LRPHP_-CNHLSX29_P0	**C12T28SOI_-LRPHP_-CNHLSX29_P4**	**C12T28SOI_-LRPHP_-CNHLSX29_P0**	**C12T28SOI_-LRPHP_-CNHLSX29_P4**
CP to Q ↓	0.0201	0.0228	0.4809	0.5152
CP to Q ↑	0.0164	0.0184	0.5753	0.6372
	C12T28SOI_-LRPHP_-CNHLSX29_P10	**C12T28SOI_-LRPHP_-CNHLSX29_P16**	**C12T28SOI_-LRPHP_-CNHLSX29_P10**	**C12T28SOI_-LRPHP_-CNHLSX29_P16**
CP to Q ↓	0.0267	0.0306	0.5645	0.6100
CP to Q ↑	0.0214	0.0245	0.7393	0.8371
	C12T28SOI_-LRPHP_-CNHLSX36_P0	**C12T28SOI_-LRPHP_-CNHLSX36_P4**	**C12T28SOI_-LRPHP_-CNHLSX36_P0**	**C12T28SOI_-LRPHP_-CNHLSX36_P4**
CP to Q ↓	0.0197	0.0225	0.3842	0.4114
CP to Q ↑	0.0163	0.0184	0.4633	0.5133
	C12T28SOI_-LRPHP_-CNHLSX36_P10	**C12T28SOI_-LRPHP_-CNHLSX36_P16**	**C12T28SOI_-LRPHP_-CNHLSX36_P10**	**C12T28SOI_-LRPHP_-CNHLSX36_P16**
CP to Q ↓	0.0264	0.0303	0.4508	0.4868
CP to Q ↑	0.0215	0.0245	0.5951	0.6731
	C12T28SOI_-LRPHP_-CNHLSX44_P0	**C12T28SOI_-LRPHP_-CNHLSX44_P4**	**C12T28SOI_-LRPHP_-CNHLSX44_P0**	**C12T28SOI_-LRPHP_-CNHLSX44_P4**
CP to Q ↓	0.0205	0.0229	0.3220	0.3444
CP to Q ↑	0.0158	0.0176	0.3871	0.4283
	C12T28SOI_-LRPHP_-CNHLSX44_P10	**C12T28SOI_-LRPHP_-CNHLSX44_P16**	**C12T28SOI_-LRPHP_-CNHLSX44_P10**	**C12T28SOI_-LRPHP_-CNHLSX44_P16**
CP to Q ↓	0.0267	0.0305	0.3769	0.4073
CP to Q ↑	0.0203	0.0232	0.4964	0.5613
	C12T28SOI_-LRPHP_-CNHLSX51_P0	**C12T28SOI_-LRPHP_-CNHLSX51_P4**	**C12T28SOI_-LRPHP_-CNHLSX51_P0**	**C12T28SOI_-LRPHP_-CNHLSX51_P4**
CP to Q ↓	0.0218	0.0245	0.2787	0.2983
CP to Q ↑	0.0170	0.0189	0.3337	0.3693
	C12T28SOI_-LRPHP_-CNHLSX51_P10	**C12T28SOI_-LRPHP_-CNHLSX51_P16**	**C12T28SOI_-LRPHP_-CNHLSX51_P10**	**C12T28SOI_-LRPHP_-CNHLSX51_P16**
CP to Q ↓	0.0287	0.0329	0.3267	0.3530
CP to Q ↑	0.0220	0.0251	0.4281	0.4842
	C12T28SOI_-LRPHP_-CNHLSX58_P0	**C12T28SOI_-LRPHP_-CNHLSX58_P4**	**C12T28SOI_-LRPHP_-CNHLSX58_P0**	**C12T28SOI_-LRPHP_-CNHLSX58_P4**
CP to Q ↓	0.0192	0.0216	0.2431	0.2598
CP to Q ↑	0.0145	0.0162	0.2942	0.3254
	C12T28SOI_-LRPHP_-CNHLSX58_P10	**C12T28SOI_-LRPHP_-CNHLSX58_P16**	**C12T28SOI_-LRPHP_-CNHLSX58_P10**	**C12T28SOI_-LRPHP_-CNHLSX58_P16**

CP to Q ↓	0.0252	0.0289	0.2845	0.3070
CP to Q ↑	0.0189	0.0216	0.3768	0.4257
	C12T28SOI_-LRPHP_-CNHLSX71_P0	**C12T28SOI_-LRPHP_-CNHLSX71_P4**	**C12T28SOI_-LRPHP_-CNHLSX71_P0**	**C12T28SOI_-LRPHP_-CNHLSX71_P4**
CP to Q ↓	0.0191	0.0215	0.2023	0.2164
CP to Q ↑	0.0152	0.0170	0.2394	0.2648
	C12T28SOI_-LRPHP_-CNHLSX71_P10	**C12T28SOI_-LRPHP_-CNHLSX71_P16**	**C12T28SOI_-LRPHP_-CNHLSX71_P10**	**C12T28SOI_-LRPHP_-CNHLSX71_P16**
CP to Q ↓	0.0250	0.0288	0.2368	0.2555
CP to Q ↑	0.0196	0.0226	0.3062	0.3465
	C12T28SOI_-LRPHP_-CNHLSX86_P0	**C12T28SOI_-LRPHP_-CNHLSX86_P4**	**C12T28SOI_-LRPHP_-CNHLSX86_P0**	**C12T28SOI_-LRPHP_-CNHLSX86_P4**
CP to Q ↓	0.0186	0.0210	0.1712	0.1830
CP to Q ↑	0.0152	0.0170	0.2023	0.2235
	C12T28SOI_-LRPHP_-CNHLSX86_P10	**C12T28SOI_-LRPHP_-CNHLSX86_P16**	**C12T28SOI_-LRPHP_-CNHLSX86_P10**	**C12T28SOI_-LRPHP_-CNHLSX86_P16**
CP to Q ↓	0.0247	0.0282	0.2003	0.2160
CP to Q ↑	0.0198	0.0225	0.2586	0.2919

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	C12T28SOI_-LRP_CNHLSX7_-P0	C12T28SOI_-LRP_CNHLSX7_-P4	C12T28SOI_-LRP_CNHLSX7_-P10	C12T28SOI_-LRP_CNHLSX7_-P16
CP ↓	min_pulse_width to CP	0.0259	0.0288	0.0341	0.0394
E ↓	hold_rising to CP	-0.0031	-0.0054	-0.0128	-0.0181
E ↑	hold_rising to CP	0.0106	0.0110	0.0058	0.0058
E ↓	setup_rising to CP	0.0309	0.0327	0.0376	0.0422
E ↑	setup_rising to CP	0.0168	0.0193	0.0246	0.0294
TE ↓	hold_rising to CP	-0.0036	-0.0054	-0.0103	-0.0152
TE ↑	hold_rising to CP	0.0107	0.0058	0.0058	0.0036
TE ↓	setup_rising to CP	0.0281	0.0303	0.0352	0.0456
TE ↑	setup_rising to CP	0.0193	0.0190	0.0239	0.0291
		C12T28SOI_-LRP_-CNHLSX15_P0	C12T28SOI_-LRP_-CNHLSX15_P4	C12T28SOI_-LRP_-CNHLSX15_P10	C12T28SOI_-LRP_-CNHLSX15_P16
CP ↓	min_pulse_width to CP	0.0259	0.0288	0.0335	0.0388
E ↓	hold_rising to CP	-0.0061	-0.0080	-0.0125	-0.0174
E ↑	hold_rising to CP	0.0106	0.0106	0.0058	0.0058
E ↓	setup_rising to CP	0.0309	0.0327	0.0373	0.0422
E ↑	setup_rising to CP	0.0168	0.0193	0.0246	0.0295
TE ↓	hold_rising to CP	-0.0032	-0.0054	-0.0103	-0.0152

TE ↑	hold_rising to CP	0.0107	0.0058	0.0058	0.0036
TE ↓	setup_rising to CP	0.0281	0.0334	0.0407	0.0453
TE ↑	setup_rising to CP	0.0193	0.0190	0.0239	0.0317
		C12T28SOI_-LRP_-CNHLSX22_P0	C12T28SOI_-LRP_-CNHLSX22_P4	C12T28SOI_-LRP_-CNHLSX22_P10	C12T28SOI_-LRP_-CNHLSX22_P16
CP ↓	min_pulse_width to CP	0.0270	0.0312	0.0359	0.0407
E ↓	hold_rising to CP	-0.0054	-0.0107	-0.0181	-0.0227
E ↑	hold_rising to CP	0.0110	0.0083	0.0058	0.0036
E ↓	setup_rising to CP	0.0327	0.0376	0.0425	0.0471
E ↑	setup_rising to CP	0.0193	0.0190	0.0264	0.0313
TE ↓	hold_rising to CP	-0.0054	-0.0106	-0.0152	-0.0201
TE ↑	hold_rising to CP	0.0083	0.0058	0.0036	0.0010
TE ↓	setup_rising to CP	0.0303	0.0352	0.0400	0.0505
TE ↑	setup_rising to CP	0.0190	0.0246	0.0295	0.0343
		C12T28SOI_-LRP_-CNHLSX29_P0	C12T28SOI_-LRP_-CNHLSX29_P4	C12T28SOI_-LRP_-CNHLSX29_P10	C12T28SOI_-LRP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0289	0.0312	0.0365	0.0418
E ↓	hold_rising to CP	-0.0080	-0.0103	-0.0174	-0.0223
E ↑	hold_rising to CP	0.0110	0.0083	0.0058	0.0036
E ↓	setup_rising to CP	0.0327	0.0376	0.0422	0.0496
E ↑	setup_rising to CP	0.0193	0.0221	0.0264	0.0313
TE ↓	hold_rising to CP	-0.0054	-0.0103	-0.0152	-0.0201
TE ↑	hold_rising to CP	0.0083	0.0058	0.0036	0.0010
TE ↓	setup_rising to CP	0.0330	0.0352	0.0452	0.0498
TE ↑	setup_rising to CP	0.0190	0.0246	0.0295	0.0366
		C12T28SOI_-LRP_-CNHLSX36_P0	C12T28SOI_-LRP_-CNHLSX36_P4	C12T28SOI_-LRP_-CNHLSX36_P10	C12T28SOI_-LRP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0289	0.0312	0.0365	0.0418
E ↓	hold_rising to CP	-0.0076	-0.0103	-0.0174	-0.0223
E ↑	hold_rising to CP	0.0110	0.0083	0.0058	0.0036
E ↓	setup_rising to CP	0.0327	0.0376	0.0422	0.0496
E ↑	setup_rising to CP	0.0193	0.0190	0.0264	0.0313
TE ↓	hold_rising to CP	-0.0085	-0.0103	-0.0152	-0.0223
TE ↑	hold_rising to CP	0.0083	0.0058	0.0036	0.0010

TE ↓	setup_rising to CP	0.0330	0.0352	0.0452	0.0498
TE ↑	setup_rising to CP	0.0190	0.0246	0.0295	0.0340
		C12T28SOI_-LRP_-CNHLSX51_P0	C12T28SOI_-LRP_-CNHLSX51_P4	C12T28SOI_-LRP_-CNHLSX51_P10	C12T28SOI_-LRP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0270	0.0312	0.0365	0.0418
E ↓	hold_rising to CP	-0.0054	-0.0107	-0.0156	-0.0230
E ↑	hold_rising to CP	0.0106	0.0083	0.0058	0.0036
E ↓	setup_rising to CP	0.0302	0.0355	0.0425	0.0471
E ↑	setup_rising to CP	0.0193	0.0190	0.0264	0.0343
TE ↓	hold_rising to CP	-0.0057	-0.0106	-0.0152	-0.0201
TE ↑	hold_rising to CP	0.0111	0.0058	0.0033	0.0040
TE ↓	setup_rising to CP	0.0306	0.0355	0.0400	0.0474
TE ↑	setup_rising to CP	0.0190	0.0246	0.0295	0.0340
		C12T28SOI_-LRP_-CNHLSX58_P0	C12T28SOI_-LRP_-CNHLSX58_P4	C12T28SOI_-LRP_-CNHLSX58_P10	C12T28SOI_-LRP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0307	0.0336	0.0389	0.0437
E ↓	hold_rising to CP	-0.0107	-0.0125	-0.0230	-0.0276
E ↑	hold_rising to CP	0.0110	0.0058	0.0058	0.0036
E ↓	setup_rising to CP	0.0351	0.0404	0.0474	0.0519
E ↑	setup_rising to CP	0.0190	0.0242	0.0295	0.0366
TE ↓	hold_rising to CP	-0.0081	-0.0134	-0.0201	-0.0275
TE ↑	hold_rising to CP	0.0058	0.0058	0.0036	0.0010
TE ↓	setup_rising to CP	0.0355	0.0404	0.0449	0.0554
TE ↑	setup_rising to CP	0.0190	0.0239	0.0313	0.0362
		C12T28SOI_-LRP_-CNHLSX71_P0	C12T28SOI_-LRP_-CNHLSX71_P4	C12T28SOI_-LRP_-CNHLSX71_P10	C12T28SOI_-LRP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0307	0.0336	0.0389	0.0461
E ↓	hold_rising to CP	-0.0107	-0.0125	-0.0230	-0.0272
E ↑	hold_rising to CP	0.0110	0.0058	0.0058	0.0036
E ↓	setup_rising to CP	0.0351	0.0404	0.0474	0.0545
E ↑	setup_rising to CP	0.0190	0.0242	0.0288	0.0362
TE ↓	hold_rising to CP	-0.0106	-0.0159	-0.0201	-0.0275
TE ↑	hold_rising to CP	0.0058	0.0058	0.0036	0.0010
TE ↓	setup_rising to CP	0.0355	0.0404	0.0449	0.0551

TE ↑	setup_rising to CP	0.0221	0.0239	0.0313	0.0392
		C12T28SOI_-LRP_-CNHLSX93_P0	C12T28SOI_-LRP_-CNHLSX93_P4	C12T28SOI_-LRP_-CNHLSX93_P10	C12T28SOI_-LRP_-CNHLSX93_P16
CP ↓	min_pulse_width to CP	0.0307	0.0360	0.0432	0.0485
E ↓	hold_rising to CP	-0.0103	-0.0156	-0.0223	-0.0297
E ↑	hold_rising to CP	0.0110	0.0058	0.0058	0.0036
E ↓	setup_rising to CP	0.0376	0.0425	0.0471	0.0575
E ↑	setup_rising to CP	0.0221	0.0239	0.0344	0.0392
TE ↓	hold_rising to CP	-0.0103	-0.0152	-0.0226	-0.0302
TE ↑	hold_rising to CP	0.0058	0.0058	0.0036	0.0010
TE ↓	setup_rising to CP	0.0352	0.0400	0.0505	0.0572
TE ↑	setup_rising to CP	0.0242	0.0295	0.0340	0.0414
		C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0331	0.0360	0.0456	0.0552
E ↓	hold_rising to CP	0.0060	0.0029	0.0007	-0.0015
E ↑	hold_rising to CP	0.0271	0.0271	0.0295	0.0295
E ↓	setup_rising to CP	0.0266	0.0287	0.0339	0.0388
E ↑	setup_rising to CP	0.0126	0.0175	0.0193	0.0246
TE ↓	hold_rising to CP	0.0082	0.0054	0.0029	-0.0019
TE ↑	hold_rising to CP	0.0271	0.0271	0.0298	0.0295
TE ↓	setup_rising to CP	0.0269	0.0293	0.0367	0.0419
TE ↑	setup_rising to CP	0.0144	0.0175	0.0246	0.0264
		C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0331	0.0360	0.0456	0.0546
E ↓	hold_rising to CP	0.0060	0.0032	0.0007	-0.0042
E ↑	hold_rising to CP	0.0271	0.0271	0.0295	0.0295
E ↓	setup_rising to CP	0.0266	0.0317	0.0339	0.0388
E ↑	setup_rising to CP	0.0126	0.0175	0.0193	0.0246
TE ↓	hold_rising to CP	0.0051	0.0029	0.0036	-0.0019
TE ↑	hold_rising to CP	0.0271	0.0271	0.0298	0.0295
TE ↓	setup_rising to CP	0.0265	0.0293	0.0367	0.0415
TE ↑	setup_rising to CP	0.0123	0.0175	0.0246	0.0264

		C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP ↓	min_pulse_width to CP	0.0331	0.0384	0.0461	0.0557
E ↓	hold_rising to CP	0.0060	0.0032	0.0007	-0.0042
E ↑	hold_rising to CP	0.0271	0.0271	0.0295	0.0295
E ↓	setup_rising to CP	0.0262	0.0314	0.0388	0.0437
E ↑	setup_rising to CP	0.0119	0.0175	0.0224	0.0295
TE ↓	hold_rising to CP	0.0054	0.0029	0.0036	-0.0019
TE ↑	hold_rising to CP	0.0246	0.0271	0.0302	0.0295
TE ↓	setup_rising to CP	0.0262	0.0318	0.0367	0.0415
TE ↑	setup_rising to CP	0.0144	0.0172	0.0246	0.0295
		C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0336	0.0389	0.0461	0.0557
E ↓	hold_rising to CP	0.0060	0.0032	0.0007	-0.0042
E ↑	hold_rising to CP	0.0271	0.0271	0.0295	0.0295
E ↓	setup_rising to CP	0.0266	0.0317	0.0335	0.0413
E ↑	setup_rising to CP	0.0122	0.0175	0.0224	0.0295
TE ↓	hold_rising to CP	0.0054	0.0029	0.0006	-0.0019
TE ↑	hold_rising to CP	0.0246	0.0271	0.0302	0.0295
TE ↓	setup_rising to CP	0.0265	0.0318	0.0367	0.0415
TE ↑	setup_rising to CP	0.0144	0.0172	0.0246	0.0295
		C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0355	0.0403	0.0480	0.0576
E ↓	hold_rising to CP	0.0029	0.0007	0.0014	-0.0042
E ↑	hold_rising to CP	0.0271	0.0271	0.0295	0.0295
E ↓	setup_rising to CP	0.0314	0.0335	0.0381	0.0459
E ↑	setup_rising to CP	0.0119	0.0175	0.0221	0.0295
TE ↓	hold_rising to CP	0.0054	0.0029	-0.0019	-0.0042
TE ↑	hold_rising to CP	0.0246	0.0246	0.0302	0.0295
TE ↓	setup_rising to CP	0.0293	0.0341	0.0415	0.0464
TE ↑	setup_rising to CP	0.0144	0.0197	0.0246	0.0295

		C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0355	0.0408	0.0510	0.0606
E ↓	hold_rising to CP	0.0007	0.0014	-0.0042	-0.0090
E ↑	hold_rising to CP	0.0271	0.0271	0.0302	0.0295
E ↓	setup_rising to CP	0.0336	0.0388	0.0437	0.0485
E ↑	setup_rising to CP	0.0175	0.0193	0.0242	0.0295
TE ↓	hold_rising to CP	0.0033	0.0006	-0.0012	-0.0065
TE ↑	hold_rising to CP	0.0250	0.0246	0.0246	0.0273
TE ↓	setup_rising to CP	0.0311	0.0367	0.0412	0.0482
TE ↑	setup_rising to CP	0.0172	0.0193	0.0239	0.0313
		C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP ↓	min_pulse_width to CP	0.0355	0.0408	0.0510	0.0624
E ↓	hold_rising to CP	0.0032	0.0007	-0.0042	-0.0064
E ↑	hold_rising to CP	0.0271	0.0271	0.0295	0.0295
E ↓	setup_rising to CP	0.0314	0.0363	0.0437	0.0485
E ↑	setup_rising to CP	0.0175	0.0193	0.0242	0.0344
TE ↓	hold_rising to CP	0.0029	0.0036	-0.0019	-0.0068
TE ↑	hold_rising to CP	0.0246	0.0246	0.0277	0.0295
TE ↓	setup_rising to CP	0.0314	0.0367	0.0412	0.0486
TE ↑	setup_rising to CP	0.0172	0.0193	0.0239	0.0344

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LRP_CNHLSX7_P0	2.031e-04	2.635e-09
C12T28SOI_LRP_CNHLSX7_P4	6.166e-05	2.635e-09
C12T28SOI_LRP_CNHLSX7_P10	1.988e-05	2.635e-09
C12T28SOI_LRP_CNHLSX7_P16	1.119e-05	2.635e-09
C12T28SOI_LRP_CNHLSX15_P0	2.648e-04	2.801e-09
C12T28SOI_LRP_CNHLSX15_P4	7.851e-05	2.801e-09
C12T28SOI_LRP_CNHLSX15_P10	2.506e-05	2.801e-09
C12T28SOI_LRP_CNHLSX15_P16	1.415e-05	2.801e-09
C12T28SOI_LRP_CNHLSX22_P0	3.137e-04	3.298e-09
C12T28SOI_LRP_CNHLSX22_P4	9.032e-05	3.298e-09
C12T28SOI_LRP_CNHLSX22_P10	2.841e-05	3.298e-09
C12T28SOI_LRP_CNHLSX22_P16	1.610e-05	3.298e-09
C12T28SOI_LRP_CNHLSX29_P0	3.559e-04	3.464e-09
C12T28SOI_LRP_CNHLSX29_P4	1.024e-04	3.464e-09
C12T28SOI_LRP_CNHLSX29_P10	3.228e-05	3.464e-09
C12T28SOI_LRP_CNHLSX29_P16	1.836e-05	3.464e-09

C12T28SOI_LRP_CNHLSX36_P0	4.039e-04	3.629e-09
C12T28SOI_LRP_CNHLSX36_P4	1.156e-04	3.629e-09
C12T28SOI_LRP_CNHLSX36_P10	3.637e-05	3.629e-09
C12T28SOI_LRP_CNHLSX36_P16	2.073e-05	3.629e-09
C12T28SOI_LRP_CNHLSX51_P0	4.965e-04	4.292e-09
C12T28SOI_LRP_CNHLSX51_P4	1.427e-04	4.292e-09
C12T28SOI_LRP_CNHLSX51_P10	4.503e-05	4.292e-09
C12T28SOI_LRP_CNHLSX51_P16	2.572e-05	4.292e-09
C12T28SOI_LRP_CNHLSX58_P0	5.975e-04	5.747e-09
C12T28SOI_LRP_CNHLSX58_P4	1.744e-04	5.747e-09
C12T28SOI_LRP_CNHLSX58_P10	5.557e-05	5.747e-09
C12T28SOI_LRP_CNHLSX58_P16	3.171e-05	5.747e-09
C12T28SOI_LRP_CNHLSX71_P0	7.049e-04	6.416e-09
C12T28SOI_LRP_CNHLSX71_P4	2.056e-04	6.416e-09
C12T28SOI_LRP_CNHLSX71_P10	6.545e-05	6.416e-09
C12T28SOI_LRP_CNHLSX71_P16	3.735e-05	6.416e-09
C12T28SOI_LRP_CNHLSX93_P0	8.482e-04	7.079e-09
C12T28SOI_LRP_CNHLSX93_P4	2.447e-04	7.079e-09
C12T28SOI_LRP_CNHLSX93_P10	7.753e-05	7.079e-09
C12T28SOI_LRP_CNHLSX93_P16	4.438e-05	7.079e-09
C12T28SOI_LRPHP_CNHLSX29_P0	4.214e-04	4.126e-09
C12T28SOI_LRPHP_CNHLSX29_P4	1.233e-04	4.126e-09
C12T28SOI_LRPHP_CNHLSX29_P10	3.895e-05	4.126e-09
C12T28SOI_LRPHP_CNHLSX29_P16	2.186e-05	4.126e-09
C12T28SOI_LRPHP_CNHLSX36_P0	4.688e-04	4.292e-09
C12T28SOI_LRPHP_CNHLSX36_P4	1.364e-04	4.292e-09
C12T28SOI_LRPHP_CNHLSX36_P10	4.306e-05	4.292e-09
C12T28SOI_LRPHP_CNHLSX36_P16	2.424e-05	4.292e-09
C12T28SOI_LRPHP_CNHLSX44_P0	5.246e-04	4.789e-09
C12T28SOI_LRPHP_CNHLSX44_P4	1.535e-04	4.789e-09
C12T28SOI_LRPHP_CNHLSX44_P10	4.863e-05	4.789e-09
C12T28SOI_LRPHP_CNHLSX44_P16	2.751e-05	4.789e-09
C12T28SOI_LRPHP_CNHLSX51_P0	5.605e-04	4.954e-09
C12T28SOI_LRPHP_CNHLSX51_P4	1.626e-04	4.954e-09
C12T28SOI_LRPHP_CNHLSX51_P10	5.130e-05	4.954e-09
C12T28SOI_LRPHP_CNHLSX51_P16	2.903e-05	4.954e-09
C12T28SOI_LRPHP_CNHLSX58_P0	6.585e-04	6.410e-09
C12T28SOI_LRPHP_CNHLSX58_P4	1.938e-04	6.410e-09
C12T28SOI_LRPHP_CNHLSX58_P10	6.179e-05	6.410e-09
C12T28SOI_LRPHP_CNHLSX58_P16	3.499e-05	6.410e-09
C12T28SOI_LRPHP_CNHLSX71_P0	7.758e-04	6.976e-09
C12T28SOI_LRPHP_CNHLSX71_P4	2.265e-04	6.976e-09
C12T28SOI_LRPHP_CNHLSX71_P10	7.188e-05	6.976e-09
C12T28SOI_LRPHP_CNHLSX71_P16	4.073e-05	6.976e-09
C12T28SOI_LRPHP_CNHLSX86_P0	8.742e-04	7.576e-09
C12T28SOI_LRPHP_CNHLSX86_P4	2.550e-04	7.576e-09
C12T28SOI_LRPHP_CNHLSX86_P10	8.103e-05	7.576e-09
C12T28SOI_LRPHP_CNHLSX86_P16	4.612e-05	7.576e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LRP_-CNHLSX7_P0	C12T28SOI_LRP_-CNHLSX7_P4	C12T28SOI_LRP_-CNHLSX7_P10	C12T28SOI_LRP_-CNHLSX7_P16

CP (output stable)	3.272e-03	3.207e-03	3.254e-03	3.345e-03
E (output stable)	1.780e-03	1.667e-03	1.589e-03	1.579e-03
TE (output stable)	1.907e-03	1.821e-03	1.805e-03	1.832e-03
CP to Q	4.954e-03	4.631e-03	4.501e-03	4.525e-03
	C12T28SOI_LRP_-CNHLSX15_P0	C12T28SOI_LRP_-CNHLSX15_P4	C12T28SOI_LRP_-CNHLSX15_P10	C12T28SOI_LRP_-CNHLSX15_P16
CP (output stable)	3.747e-03	3.710e-03	3.781e-03	3.906e-03
E (output stable)	1.824e-03	1.717e-03	1.645e-03	1.644e-03
TE (output stable)	1.950e-03	1.870e-03	1.861e-03	1.897e-03
CP to Q	7.388e-03	6.874e-03	6.693e-03	6.705e-03
	C12T28SOI_LRP_-CNHLSX22_P0	C12T28SOI_LRP_-CNHLSX22_P4	C12T28SOI_LRP_-CNHLSX22_P10	C12T28SOI_LRP_-CNHLSX22_P16
CP (output stable)	4.169e-03	4.144e-03	4.231e-03	4.387e-03
E (output stable)	1.942e-03	1.838e-03	1.768e-03	1.769e-03
TE (output stable)	2.069e-03	1.991e-03	1.983e-03	2.022e-03
CP to Q	9.681e-03	8.958e-03	8.728e-03	8.743e-03
	C12T28SOI_LRP_-CNHLSX29_P0	C12T28SOI_LRP_-CNHLSX29_P4	C12T28SOI_LRP_-CNHLSX29_P10	C12T28SOI_LRP_-CNHLSX29_P16
CP (output stable)	4.346e-03	4.331e-03	4.468e-03	4.634e-03
E (output stable)	1.973e-03	1.866e-03	1.796e-03	1.796e-03
TE (output stable)	2.099e-03	2.020e-03	2.011e-03	2.049e-03
CP to Q	1.186e-02	1.104e-02	1.063e-02	1.076e-02
	C12T28SOI_LRP_-CNHLSX36_P0	C12T28SOI_LRP_-CNHLSX36_P4	C12T28SOI_LRP_-CNHLSX36_P10	C12T28SOI_LRP_-CNHLSX36_P16
CP (output stable)	4.634e-03	4.625e-03	4.777e-03	4.975e-03
E (output stable)	1.979e-03	1.872e-03	1.804e-03	1.806e-03
TE (output stable)	2.105e-03	2.026e-03	2.019e-03	2.059e-03
CP to Q	1.389e-02	1.292e-02	1.252e-02	1.264e-02
	C12T28SOI_LRP_-CNHLSX51_P0	C12T28SOI_LRP_-CNHLSX51_P4	C12T28SOI_LRP_-CNHLSX51_P10	C12T28SOI_LRP_-CNHLSX51_P16
CP (output stable)	5.068e-03	5.103e-03	5.308e-03	5.559e-03
E (output stable)	1.992e-03	1.893e-03	1.834e-03	1.845e-03
TE (output stable)	2.118e-03	2.047e-03	2.050e-03	2.098e-03
CP to Q	1.872e-02	1.761e-02	1.701e-02	1.714e-02
	C12T28SOI_LRP_-CNHLSX58_P0	C12T28SOI_LRP_-CNHLSX58_P4	C12T28SOI_LRP_-CNHLSX58_P10	C12T28SOI_LRP_-CNHLSX58_P16
CP (output stable)	6.424e-03	6.507e-03	6.834e-03	7.181e-03
E (output stable)	2.165e-03	2.072e-03	2.024e-03	2.044e-03
TE (output stable)	2.290e-03	2.224e-03	2.236e-03	2.294e-03
CP to Q	2.141e-02	1.983e-02	1.915e-02	1.930e-02
	C12T28SOI_LRP_-CNHLSX71_P0	C12T28SOI_LRP_-CNHLSX71_P4	C12T28SOI_LRP_-CNHLSX71_P10	C12T28SOI_LRP_-CNHLSX71_P16
CP (output stable)	7.216e-03	7.380e-03	7.747e-03	8.190e-03
E (output stable)	2.231e-03	2.145e-03	2.103e-03	2.131e-03
TE (output stable)	2.356e-03	2.297e-03	2.317e-03	2.381e-03
CP to Q	2.617e-02	2.457e-02	2.371e-02	2.381e-02
	C12T28SOI_LRP_-CNHLSX93_P0	C12T28SOI_LRP_-CNHLSX93_P4	C12T28SOI_LRP_-CNHLSX93_P10	C12T28SOI_LRP_-CNHLSX93_P16
CP (output stable)	8.153e-03	8.389e-03	8.872e-03	9.406e-03
E (output stable)	2.385e-03	2.304e-03	2.274e-03	2.311e-03
TE (output stable)	2.512e-03	2.459e-03	2.489e-03	2.564e-03
CP to Q	3.466e-02	3.235e-02	3.096e-02	3.120e-02

	C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP (output stable)	6.015e-03	6.077e-03	6.300e-03	6.553e-03
E (output stable)	1.889e-03	1.771e-03	1.691e-03	1.684e-03
TE (output stable)	2.018e-03	1.925e-03	1.905e-03	1.937e-03
CP to Q	1.413e-02	1.346e-02	1.313e-02	1.333e-02
	C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP (output stable)	6.276e-03	6.344e-03	6.605e-03	6.898e-03
E (output stable)	1.899e-03	1.783e-03	1.705e-03	1.700e-03
TE (output stable)	2.028e-03	1.936e-03	1.919e-03	1.953e-03
CP to Q	1.609e-02	1.532e-02	1.501e-02	1.516e-02
	C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP (output stable)	6.703e-03	6.829e-03	7.109e-03	7.449e-03
E (output stable)	1.959e-03	1.846e-03	1.775e-03	1.776e-03
TE (output stable)	2.089e-03	2.000e-03	1.989e-03	2.029e-03
CP to Q	1.871e-02	1.753e-02	1.698e-02	1.716e-02
	C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP (output stable)	6.752e-03	6.821e-03	7.125e-03	7.449e-03
E (output stable)	1.959e-03	1.846e-03	1.775e-03	1.776e-03
TE (output stable)	2.089e-03	2.001e-03	1.989e-03	2.029e-03
CP to Q	2.072e-02	1.950e-02	1.894e-02	1.912e-02
	C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP (output stable)	7.772e-03	7.898e-03	8.354e-03	8.750e-03
E (output stable)	2.045e-03	1.937e-03	1.874e-03	1.883e-03
TE (output stable)	2.175e-03	2.091e-03	2.088e-03	2.135e-03
CP to Q	2.274e-02	2.132e-02	2.066e-02	2.095e-02
	C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP (output stable)	8.652e-03	8.846e-03	9.303e-03	9.865e-03
E (output stable)	2.188e-03	2.082e-03	2.023e-03	2.038e-03
TE (output stable)	2.317e-03	2.236e-03	2.237e-03	2.291e-03
CP to Q	2.752e-02	2.582e-02	2.489e-02	2.539e-02
	C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP (output stable)	9.435e-03	9.620e-03	1.015e-02	1.079e-02
E (output stable)	2.229e-03	2.135e-03	2.086e-03	2.118e-03
TE (output stable)	2.359e-03	2.290e-03	2.300e-03	2.371e-03
CP to Q	3.172e-02	2.983e-02	2.902e-02	2.922e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	C12T28SOI_LRP_-CNHLSX7_P0	C12T28SOI_LRP_-CNHLSX7_P4	C12T28SOI_LRP_-CNHLSX7_P10	C12T28SOI_LRP_-CNHLSX7_P16
CP (output stable)	-3.648e-05	-3.378e-05	-2.666e-05	-2.373e-05
E (output stable)	8.471e-07	3.145e-06	1.186e-05	1.235e-05
TE (output stable)	1.008e-06	6.775e-07	2.049e-08	-9.109e-07
CP to Q	1.449e-05	1.701e-05	1.790e-05	1.734e-05
	C12T28SOI_LRP_-CNHLSX15_P0	C12T28SOI_LRP_-CNHLSX15_P4	C12T28SOI_LRP_-CNHLSX15_P10	C12T28SOI_LRP_-CNHLSX15_P16
CP (output stable)	-2.639e-05	-2.291e-05	-1.836e-05	-1.404e-05
E (output stable)	7.307e-07	3.141e-06	1.167e-05	1.237e-05
TE (output stable)	9.920e-07	5.294e-07	1.883e-08	-8.633e-07
CP to Q	5.249e-06	6.228e-06	7.252e-06	5.975e-06
	C12T28SOI_LRP_-CNHLSX22_P0	C12T28SOI_LRP_-CNHLSX22_P4	C12T28SOI_LRP_-CNHLSX22_P10	C12T28SOI_LRP_-CNHLSX22_P16
CP (output stable)	-1.176e-06	7.848e-07	5.176e-06	9.989e-06
E (output stable)	7.466e-07	3.080e-06	1.167e-05	1.233e-05
TE (output stable)	7.045e-07	5.518e-07	-1.844e-08	-8.659e-07
CP to Q	2.063e-05	2.490e-05	2.366e-05	2.381e-05
	C12T28SOI_LRP_-CNHLSX29_P0	C12T28SOI_LRP_-CNHLSX29_P4	C12T28SOI_LRP_-CNHLSX29_P10	C12T28SOI_LRP_-CNHLSX29_P16
CP (output stable)	-2.246e-05	-2.076e-05	-1.429e-05	-8.073e-06
E (output stable)	7.702e-07	3.088e-06	1.152e-05	1.229e-05
TE (output stable)	9.119e-07	5.236e-07	1.159e-08	-9.172e-07
CP to Q	1.208e-05	1.609e-05	1.615e-05	1.414e-05
	C12T28SOI_LRP_-CNHLSX36_P0	C12T28SOI_LRP_-CNHLSX36_P4	C12T28SOI_LRP_-CNHLSX36_P10	C12T28SOI_LRP_-CNHLSX36_P16
CP (output stable)	-8.640e-06	-6.439e-06	-6.989e-07	5.701e-06
E (output stable)	7.859e-07	3.140e-06	1.153e-05	1.230e-05
TE (output stable)	9.607e-07	5.582e-07	-3.622e-09	-8.359e-07
CP to Q	3.563e-05	3.914e-05	3.691e-05	3.460e-05
	C12T28SOI_LRP_-CNHLSX51_P0	C12T28SOI_LRP_-CNHLSX51_P4	C12T28SOI_LRP_-CNHLSX51_P10	C12T28SOI_LRP_-CNHLSX51_P16
CP (output stable)	-1.924e-05	-1.627e-05	-9.455e-06	-2.552e-06
E (output stable)	7.553e-07	3.129e-06	1.166e-05	1.238e-05
TE (output stable)	9.920e-07	5.294e-07	-1.396e-08	-8.663e-07
CP to Q	4.876e-05	4.921e-05	4.577e-05	3.964e-05
	C12T28SOI_LRP_-CNHLSX58_P0	C12T28SOI_LRP_-CNHLSX58_P4	C12T28SOI_LRP_-CNHLSX58_P10	C12T28SOI_LRP_-CNHLSX58_P16
CP (output stable)	-6.138e-05	-5.809e-05	-4.951e-05	-4.386e-05
E (output stable)	8.085e-07	3.155e-06	1.183e-05	1.222e-05
TE (output stable)	6.434e-07	6.353e-07	-3.175e-08	-9.232e-07
CP to Q	4.705e-05	5.002e-05	4.296e-05	4.188e-05
	C12T28SOI_LRP_-CNHLSX71_P0	C12T28SOI_LRP_-CNHLSX71_P4	C12T28SOI_LRP_-CNHLSX71_P10	C12T28SOI_LRP_-CNHLSX71_P16
CP (output stable)	-4.336e-05	-4.123e-05	-3.338e-05	-2.407e-05
E (output stable)	7.952e-07	3.131e-06	1.183e-05	1.222e-05
TE (output stable)	6.466e-07	4.739e-07	-3.380e-08	-9.196e-07
CP to Q	4.153e-05	4.562e-05	4.132e-05	3.255e-05
	C12T28SOI_LRP_-CNHLSX93_P0	C12T28SOI_LRP_-CNHLSX93_P4	C12T28SOI_LRP_-CNHLSX93_P10	C12T28SOI_LRP_-CNHLSX93_P16
CP (output stable)	-5.022e-05	-4.623e-05	-3.540e-05	-2.727e-05
E (output stable)	7.816e-07	3.139e-06	1.155e-05	1.231e-05
TE (output stable)	8.977e-07	5.121e-07	5.448e-08	-9.000e-07

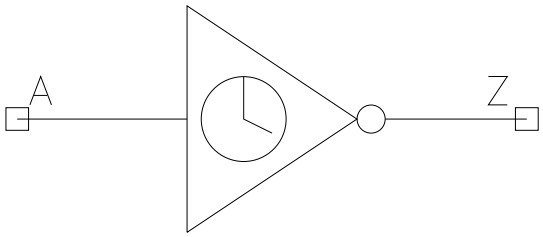
CP to Q	7.860e-05	7.896e-05	7.800e-05	6.386e-05
	C12T28SOI_-LRPHP_-CNHLSX29_P0	C12T28SOI_-LRPHP_-CNHLSX29_P4	C12T28SOI_-LRPHP_-CNHLSX29_P10	C12T28SOI_-LRPHP_-CNHLSX29_P16
CP (output stable)	-3.615e-05	-3.203e-05	-2.608e-05	-1.981e-05
E (output stable)	6.440e-07	2.794e-06	1.182e-05	1.285e-05
TE (output stable)	9.526e-07	7.959e-07	1.040e-07	-7.402e-07
CP to Q	2.182e-05	2.429e-05	2.004e-05	1.790e-05
	C12T28SOI_-LRPHP_-CNHLSX36_P0	C12T28SOI_-LRPHP_-CNHLSX36_P4	C12T28SOI_-LRPHP_-CNHLSX36_P10	C12T28SOI_-LRPHP_-CNHLSX36_P16
CP (output stable)	-2.379e-05	-1.984e-05	-1.341e-05	-3.574e-06
E (output stable)	6.253e-07	2.788e-06	1.182e-05	1.285e-05
TE (output stable)	9.437e-07	7.993e-07	1.271e-07	-7.415e-07
CP to Q	3.354e-05	3.409e-05	3.346e-05	2.834e-05
	C12T28SOI_-LRPHP_-CNHLSX44_P0	C12T28SOI_-LRPHP_-CNHLSX44_P4	C12T28SOI_-LRPHP_-CNHLSX44_P10	C12T28SOI_-LRPHP_-CNHLSX44_P16
CP (output stable)	-3.836e-05	-3.322e-05	-2.240e-05	-1.340e-05
E (output stable)	6.255e-07	2.796e-06	1.182e-05	1.285e-05
TE (output stable)	7.757e-07	7.951e-07	1.249e-07	-7.447e-07
CP to Q	3.350e-05	3.439e-05	3.032e-05	2.705e-05
	C12T28SOI_-LRPHP_-CNHLSX51_P0	C12T28SOI_-LRPHP_-CNHLSX51_P4	C12T28SOI_-LRPHP_-CNHLSX51_P10	C12T28SOI_-LRPHP_-CNHLSX51_P16
CP (output stable)	-3.690e-05	-3.299e-05	-2.213e-05	-1.509e-05
E (output stable)	6.199e-07	2.799e-06	1.182e-05	1.284e-05
TE (output stable)	7.758e-07	7.171e-07	1.219e-07	-7.297e-07
CP to Q	4.550e-05	4.704e-05	3.993e-05	3.974e-05
	C12T28SOI_-LRPHP_-CNHLSX58_P0	C12T28SOI_-LRPHP_-CNHLSX58_P4	C12T28SOI_-LRPHP_-CNHLSX58_P10	C12T28SOI_-LRPHP_-CNHLSX58_P16
CP (output stable)	-6.618e-05	-6.068e-05	-5.860e-05	-4.425e-05
E (output stable)	6.164e-07	2.802e-06	1.180e-05	1.282e-05
TE (output stable)	7.700e-07	7.924e-07	7.188e-08	-7.547e-07
CP to Q	5.079e-05	4.918e-05	4.190e-05	3.770e-05
	C12T28SOI_-LRPHP_-CNHLSX71_P0	C12T28SOI_-LRPHP_-CNHLSX71_P4	C12T28SOI_-LRPHP_-CNHLSX71_P10	C12T28SOI_-LRPHP_-CNHLSX71_P16
CP (output stable)	-5.507e-05	-4.503e-05	-4.770e-05	-2.683e-05
E (output stable)	5.198e-07	2.738e-06	1.177e-05	1.281e-05
TE (output stable)	9.091e-07	7.401e-07	7.367e-08	-7.702e-07
CP to Q	4.832e-05	4.878e-05	4.522e-05	3.665e-05
	C12T28SOI_-LRPHP_-CNHLSX86_P0	C12T28SOI_-LRPHP_-CNHLSX86_P4	C12T28SOI_-LRPHP_-CNHLSX86_P10	C12T28SOI_-LRPHP_-CNHLSX86_P16
CP (output stable)	-6.396e-05	-4.491e-05	-1.919e-05	-3.389e-05
E (output stable)	5.961e-07	2.768e-06	1.180e-05	1.282e-05
TE (output stable)	9.606e-07	7.592e-07	9.958e-08	-7.700e-07
CP to Q	5.762e-05	5.501e-05	3.700e-05	3.420e-05

CNIV

Cell Description

Inverter with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.272	0.3264
X5_P4	1.200	0.272	0.3264
X5_P10	1.200	0.272	0.3264
X5_P16	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X16_P0	1.200	0.408	0.4896
X16_P4	1.200	0.408	0.4896
X16_P10	1.200	0.408	0.4896
X16_P16	1.200	0.408	0.4896
X23_P0	1.200	0.544	0.6528
X23_P4	1.200	0.544	0.6528
X23_P10	1.200	0.544	0.6528
X23_P16	1.200	0.544	0.6528
X31_P0	1.200	0.680	0.8160
X31_P4	1.200	0.680	0.8160
X31_P10	1.200	0.680	0.8160
X31_P16	1.200	0.680	0.8160
X39_P0	1.200	0.816	0.9792
X39_P4	1.200	0.816	0.9792
X39_P10	1.200	0.816	0.9792
X39_P16	1.200	0.816	0.9792
X47_P0	1.200	0.952	1.1424
X47_P4	1.200	0.952	1.1424
X47_P10	1.200	0.952	1.1424
X47_P16	1.200	0.952	1.1424
X55_P0	1.200	1.088	1.3056
X55_P4	1.200	1.088	1.3056
X55_P10	1.200	1.088	1.3056
X55_P16	1.200	1.088	1.3056
X61_P0	1.200	1.224	1.4688

X61_P4	1.200	1.224	1.4688
X61_P10	1.200	1.224	1.4688
X61_P16	1.200	1.224	1.4688
X70_P0	1.200	1.360	1.6320
X70_P4	1.200	1.360	1.6320
X70_P10	1.200	1.360	1.6320
X70_P16	1.200	1.360	1.6320
X94_P0	1.200	1.768	2.1216
X94_P4	1.200	1.768	2.1216
X94_P10	1.200	1.768	2.1216
X94_P16	1.200	1.768	2.1216
X133_P0	1.200	2.448	2.9376
X133_P4	1.200	2.448	2.9376
X133_P10	1.200	2.448	2.9376
X133_P16	1.200	2.448	2.9376

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X5_P0	X5_P4	X5_P10	X5_P16
A	0.0006	0.0007	0.0007	0.0007
	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0009	0.0010	0.0010	0.0011
	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0018	0.0018	0.0019	0.0020
	X23_P0	X23_P4	X23_P10	X23_P16
A	0.0026	0.0027	0.0029	0.0031
	X31_P0	X31_P4	X31_P10	X31_P16
A	0.0035	0.0036	0.0038	0.0040
	X39_P0	X39_P4	X39_P10	X39_P16
A	0.0043	0.0045	0.0048	0.0050
	X47_P0	X47_P4	X47_P10	X47_P16
A	0.0054	0.0055	0.0058	0.0061
	X55_P0	X55_P4	X55_P10	X55_P16
A	0.0062	0.0063	0.0067	0.0070
	X61_P0	X61_P4	X61_P10	X61_P16
A	0.0068	0.0072	0.0075	0.0079
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0081	0.0084	0.0088	0.0093
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0111	0.0115	0.0123	0.0129
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0161	0.0168	0.0180	0.0189

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X5_P4	X5_P0	X5_P4
A to Z ↓	0.0036	0.0043	2.6941	2.8746

A to Z ↑	0.0098	0.0108	4.1019	4.5413
	X5_P10	**X5_P16**	**X5_P10**	**X5_P16**
A to Z ↓	0.0055	0.0065	3.1311	3.3625
A to Z ↑	0.0123	0.0136	5.2618	5.9624
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0035	0.0040	1.7417	1.8555
A to Z ↑	0.0081	0.0090	2.2680	2.5153
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0049	0.0057	2.0164	2.1645
A to Z ↑	0.0102	0.0112	2.9180	3.3005
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0026	0.0031	0.8588	0.9144
A to Z ↑	0.0072	0.0080	1.1337	1.2572
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0039	0.0046	0.9939	1.0653
A to Z ↑	0.0091	0.0100	1.4570	1.6470
	X23_P0	**X23_P4**	**X23_P0**	**X23_P4**
A to Z ↓	0.0030	0.0035	0.6104	0.6504
A to Z ↑	0.0072	0.0080	0.7703	0.8534
	X23_P10	**X23_P16**	**X23_P10**	**X23_P16**
A to Z ↓	0.0043	0.0051	0.7072	0.7585
A to Z ↑	0.0091	0.0101	0.9880	1.1154
	X31_P0	**X31_P4**	**X31_P0**	**X31_P4**
A to Z ↓	0.0028	0.0032	0.4424	0.4711
A to Z ↑	0.0070	0.0078	0.5766	0.6383
	X31_P10	**X31_P16**	**X31_P10**	**X31_P16**
A to Z ↓	0.0039	0.0047	0.5125	0.5493
A to Z ↑	0.0088	0.0098	0.7390	0.8342
	X39_P0	**X39_P4**	**X39_P0**	**X39_P4**
A to Z ↓	0.0032	0.0037	0.3575	0.3806
A to Z ↑	0.0073	0.0081	0.4644	0.5142
	X39_P10	**X39_P16**	**X39_P10**	**X39_P16**
A to Z ↓	0.0045	0.0052	0.4139	0.4442
A to Z ↑	0.0092	0.0102	0.5944	0.6716
	X47_P0	**X47_P4**	**X47_P0**	**X47_P4**
A to Z ↓	0.0031	0.0035	0.2971	0.3164
A to Z ↑	0.0072	0.0080	0.3866	0.4284
	X47_P10	**X47_P16**	**X47_P10**	**X47_P16**
A to Z ↓	0.0043	0.0051	0.3444	0.3696
A to Z ↑	0.0091	0.0100	0.4949	0.5593
	X55_P0	**X55_P4**	**X55_P0**	**X55_P4**
A to Z ↓	0.0035	0.0040	0.2562	0.2730
A to Z ↑	0.0075	0.0083	0.3320	0.3680
	X55_P10	**X55_P16**	**X55_P10**	**X55_P16**
A to Z ↓	0.0048	0.0056	0.2972	0.3188
A to Z ↑	0.0094	0.0104	0.4252	0.4806
	X61_P0	**X61_P4**	**X61_P0**	**X61_P4**
A to Z ↓	0.0036	0.0042	0.2301	0.2452
A to Z ↑	0.0076	0.0085	0.3001	0.3326
	X61_P10	**X61_P16**	**X61_P10**	**X61_P16**
A to Z ↓	0.0050	0.0058	0.2668	0.2864
A to Z ↑	0.0096	0.0106	0.3848	0.4347

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0041	0.0046	0.2024	0.2156
A to Z ↑	0.0080	0.0088	0.2615	0.2891
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0054	0.0062	0.2346	0.2513
A to Z ↑	0.0099	0.0110	0.3338	0.3766
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0054	0.0058	0.1557	0.1660
A to Z ↑	0.0092	0.0099	0.1992	0.2204
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0068	0.0077	0.1804	0.1934
A to Z ↑	0.0111	0.0122	0.2541	0.2866
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0073	0.0076	0.1154	0.1230
A to Z ↑	0.0108	0.0115	0.1447	0.1597
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0087	0.0098	0.1337	0.1432
A to Z ↑	0.0129	0.0142	0.1839	0.2071

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X5_P0	2.810e-05	8.135e-10
X5_P4	8.958e-06	8.135e-10
X5_P10	2.842e-06	8.135e-10
X5_P16	1.492e-06	8.135e-10
X8_P0	4.566e-05	8.135e-10
X8_P4	1.390e-05	8.135e-10
X8_P10	4.353e-06	8.135e-10
X8_P16	2.299e-06	8.135e-10
X16_P0	9.208e-05	9.792e-10
X16_P4	2.790e-05	9.792e-10
X16_P10	8.653e-06	9.792e-10
X16_P16	4.558e-06	9.792e-10
X23_P0	1.283e-04	1.145e-09
X23_P4	3.840e-05	1.145e-09
X23_P10	1.185e-05	1.145e-09
X23_P16	6.276e-06	1.145e-09
X31_P0	1.717e-04	1.310e-09
X31_P4	5.092e-05	1.310e-09
X31_P10	1.566e-05	1.310e-09
X31_P16	8.325e-06	1.310e-09
X39_P0	2.098e-04	1.476e-09
X39_P4	6.213e-05	1.476e-09
X39_P10	1.910e-05	1.476e-09
X39_P16	1.018e-05	1.476e-09
X47_P0	2.449e-04	1.642e-09
X47_P4	7.290e-05	1.642e-09
X47_P10	2.248e-05	1.642e-09
X47_P16	1.202e-05	1.642e-09
X55_P0	2.877e-04	1.807e-09
X55_P4	8.469e-05	1.807e-09
X55_P10	2.597e-05	1.807e-09

X55_P16	1.388e-05	1.807e-09
X61_P0	3.214e-04	1.973e-09
X61_P4	9.375e-05	1.973e-09
X61_P10	2.864e-05	1.973e-09
X61_P16	1.530e-05	1.973e-09
X70_P0	3.590e-04	2.139e-09
X70_P4	1.063e-04	2.139e-09
X70_P10	3.272e-05	2.139e-09
X70_P16	1.755e-05	2.139e-09
X94_P0	4.735e-04	2.635e-09
X94_P4	1.398e-04	2.635e-09
X94_P10	4.300e-05	2.635e-09
X94_P16	2.309e-05	2.635e-09
X133_P0	6.850e-04	3.464e-09
X133_P4	1.985e-04	3.464e-09
X133_P10	6.044e-05	3.464e-09
X133_P16	3.242e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	1.103e-03	8.968e-04	7.489e-04	6.790e-04
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	1.767e-03	1.401e-03	1.126e-03	9.946e-04
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	3.378e-03	2.632e-03	2.034e-03	1.739e-03
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	4.977e-03	3.917e-03	3.070e-03	2.653e-03
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	6.579e-03	5.110e-03	3.906e-03	3.357e-03
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	8.252e-03	6.481e-03	5.038e-03	4.321e-03
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	9.814e-03	7.695e-03	5.957e-03	5.100e-03
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	1.162e-02	9.110e-03	7.106e-03	6.109e-03
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	1.288e-02	1.005e-02	7.775e-03	6.654e-03
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	1.502e-02	1.176e-02	9.147e-03	7.877e-03
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	2.100e-02	1.632e-02	1.270e-02	1.090e-02
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	3.314e-02	2.573e-02	2.043e-02	1.768e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	2.545e-07	6.204e-07	6.306e-07	1.955e-06
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	-5.744e-07	8.134e-07	9.144e-07	1.159e-06
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	-2.800e-08	-1.006e-06	3.792e-07	-1.176e-07

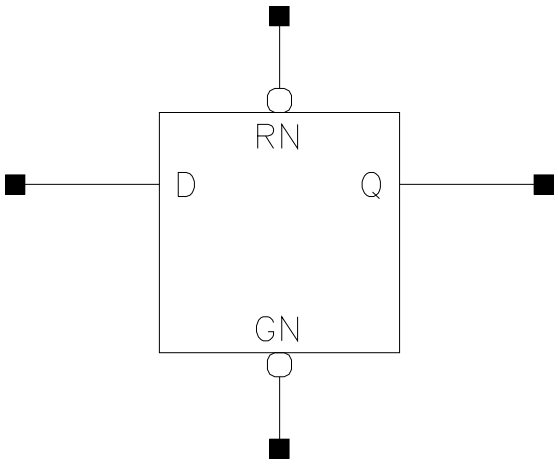
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	3.400e-08	-3.186e-06	-8.600e-08	2.210e-07
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	-1.080e-07	-3.278e-06	-6.100e-08	-6.179e-07
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	-2.550e-07	-5.232e-06	9.980e-07	1.121e-06
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	-2.170e-07	-6.436e-06	3.990e-07	-3.890e-07
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	4.390e-07	-1.463e-06	1.220e-06	-5.230e-07
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	-3.420e-07	-4.070e-06	1.926e-06	-9.050e-07
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	-1.350e-07	-4.136e-06	3.720e-07	-9.250e-07
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	-1.051e-06	2.530e-06	1.605e-06	1.351e-05
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	1.178e-05	-2.359e-06	-1.963e-06	4.532e-06

CNLDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
D	0.0013	0.0014	0.0015	0.0015
GN	0.0023	0.0024	0.0025	0.0026
RN	0.0007	0.0007	0.0007	0.0008

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	X33_P4	X33_P0	X33_P4

D to Q ↓	0.0370	0.0425	0.4096	0.4410
D to Q ↑	0.0367	0.0412	0.5860	0.6522
GN to Q ↓	0.0345	0.0394	0.4102	0.4414
GN to Q ↑	0.0416	0.0466	0.5856	0.6532
RN to Q ↓	0.0466	0.0527	0.4050	0.4375
RN to Q ↑	0.0415	0.0464	0.5863	0.6534
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D to Q ↓	0.0513	0.0601	0.4880	0.5315
D to Q ↑	0.0486	0.0561	0.7612	0.8659
GN to Q ↓	0.0467	0.0539	0.4884	0.5320
GN to Q ↑	0.0548	0.0630	0.7616	0.8664
RN to Q ↓	0.0624	0.0723	0.4849	0.5288
RN to Q ↑	0.0543	0.0621	0.7620	0.8664

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X33_P0	X33_P4	X33_P10	X33_P16
D ↓	hold_rising to GN	-0.0029	-0.0048	-0.0145	-0.0191
D ↑	hold_rising to GN	-0.0042	-0.0070	-0.0144	-0.0190
D ↓	setup_rising to GN	0.0395	0.0443	0.0566	0.0667
D ↑	setup_rising to GN	0.0385	0.0437	0.0539	0.0609
GN ↓	min_pulse_width to GN	0.0464	0.0522	0.0617	0.0723
RN ↓	min_pulse_width to RN	0.0615	0.0686	0.0806	0.0952
RN ↑	recovery_rising to GN	0.0463	0.0481	0.0578	0.0683
RN ↑	removal_rising to GN	-0.0261	-0.0310	-0.0384	-0.0430

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X33_P0	2.605e-04	3.464e-09
X33_P4	7.456e-05	3.464e-09
X33_P10	2.444e-05	3.464e-09
X33_P16	1.470e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	1.212e-04	1.657e-04	2.095e-04	2.115e-04
GN (output stable)	2.766e-03	2.549e-03	2.413e-03	2.378e-03
RN (output stable)	1.291e-04	1.168e-04	9.939e-05	8.184e-05
D to Q	2.037e-02	1.907e-02	1.830e-02	1.817e-02
GN to Q	2.471e-02	2.330e-02	2.248e-02	2.238e-02
RN to Q	1.596e-02	1.501e-02	1.445e-02	1.432e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	1.134e-07	-2.068e-07	-1.113e-06	-2.420e-06

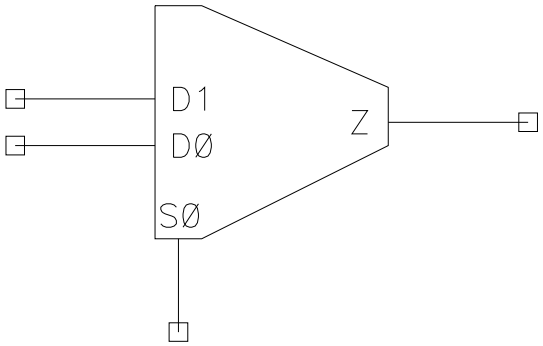
GN (output stable)	7.225e-07	3.608e-06	1.013e-05	9.819e-06
RN (output stable)	1.212e-07	1.582e-07	1.896e-07	2.870e-07
D to Q	-4.640e-08	-1.398e-07	-8.306e-07	-2.148e-06
GN to Q	8.497e-06	1.647e-05	2.560e-05	3.525e-05
RN to Q	-2.349e-06	-7.321e-06	-1.394e-05	-2.153e-05

CNMUX21

Cell Description

2:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320
X17_P4	1.200	1.360	1.6320
X17_P10	1.200	1.360	1.6320
X17_P16	1.200	1.360	1.6320
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0011	0.0011	0.0012	0.0013
D1	0.0011	0.0011	0.0012	0.0013
S0	0.0015	0.0015	0.0016	0.0017
	X33_P0	X33_P4	X33_P10	X33_P16
D0	0.0020	0.0021	0.0023	0.0024
D1	0.0020	0.0021	0.0023	0.0024
S0	0.0025	0.0026	0.0028	0.0030

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X17_P4	X17_P0	X17_P4

D0 to Z ↓	0.0251	0.0279	0.7667	0.8204
D0 to Z ↑	0.0198	0.0221	1.1224	1.2471
D1 to Z ↓	0.0246	0.0276	0.7656	0.8192
D1 to Z ↑	0.0188	0.0209	1.1217	1.2466
S0 to Z ↓	0.0232	0.0260	0.7625	0.8164
S0 to Z ↑	0.0230	0.0257	1.1213	1.2461
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0328	0.0374	0.9010	0.9740
D0 to Z ↑	0.0258	0.0294	1.4504	1.6423
D1 to Z ↓	0.0325	0.0372	0.8997	0.9735
D1 to Z ↑	0.0244	0.0278	1.4484	1.6409
S0 to Z ↓	0.0305	0.0349	0.8964	0.9693
S0 to Z ↑	0.0302	0.0344	1.4488	1.6429
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
D0 to Z ↓	0.0240	0.0270	0.3948	0.4231
D0 to Z ↑	0.0196	0.0220	0.5658	0.6287
D1 to Z ↓	0.0249	0.0280	0.3956	0.4239
D1 to Z ↑	0.0191	0.0214	0.5657	0.6286
S0 to Z ↓	0.0241	0.0271	0.3937	0.4220
S0 to Z ↑	0.0234	0.0263	0.5653	0.6281
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D0 to Z ↓	0.0317	0.0362	0.4647	0.5025
D0 to Z ↑	0.0257	0.0293	0.7306	0.8278
D1 to Z ↓	0.0328	0.0378	0.4659	0.5040
D1 to Z ↑	0.0248	0.0283	0.7304	0.8272
S0 to Z ↓	0.0316	0.0361	0.4639	0.5017
S0 to Z ↑	0.0308	0.0352	0.7303	0.8275

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P0	2.470e-04	2.139e-09
X17_P4	7.593e-05	2.139e-09
X17_P10	2.393e-05	2.139e-09
X17_P16	1.277e-05	2.139e-09
X33_P0	4.661e-04	3.464e-09
X33_P4	1.427e-04	3.464e-09
X33_P10	4.515e-05	3.464e-09
X33_P16	2.432e-05	3.464e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	2.375e-03	2.046e-03	1.805e-03	1.693e-03
D1 (output stable)	2.329e-03	1.984e-03	1.726e-03	1.607e-03
S0 (output stable)	1.972e-03	1.848e-03	1.797e-03	1.804e-03
D0 to Z	8.159e-03	7.606e-03	7.415e-03	7.437e-03
D1 to Z	7.980e-03	7.432e-03	7.238e-03	7.279e-03
S0 to Z	8.615e-03	8.057e-03	7.865e-03	7.905e-03
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	4.090e-03	3.393e-03	2.860e-03	2.602e-03
D1 (output stable)	4.157e-03	3.482e-03	2.965e-03	2.712e-03
S0 (output stable)	3.201e-03	2.999e-03	2.906e-03	2.927e-03

D0 to Z	1.586e-02	1.495e-02	1.455e-02	1.464e-02
D1 to Z	1.580e-02	1.488e-02	1.440e-02	1.456e-02
S0 to Z	1.698e-02	1.607e-02	1.569e-02	1.581e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

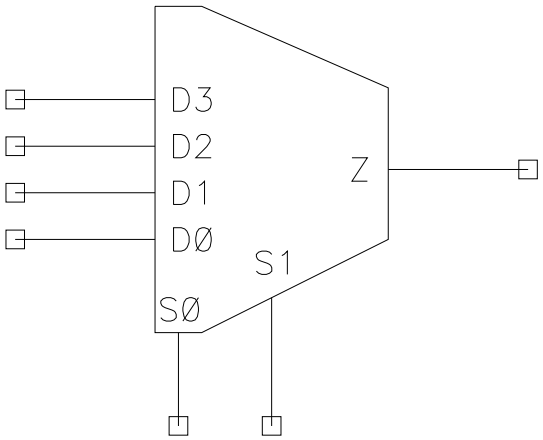
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	1.176e-06	1.778e-06	2.490e-06	1.585e-06
D1 (output stable)	1.037e-06	6.325e-07	2.687e-06	1.916e-06
S0 (output stable)	3.745e-07	3.345e-07	1.432e-07	-8.685e-08
D0 to Z	5.560e-07	2.490e-07	-7.000e-08	3.250e-08
D1 to Z	5.968e-07	3.835e-07	-1.255e-07	2.040e-07
S0 to Z	9.400e-09	4.349e-07	9.615e-08	-1.651e-07
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	-5.025e-07	4.205e-07	3.381e-07	1.602e-06
D1 (output stable)	-5.810e-07	3.310e-07	1.538e-06	3.935e-06
S0 (output stable)	4.310e-07	9.925e-08	5.250e-08	-4.145e-08
D0 to Z	6.730e-07	1.400e-08	-1.850e-07	-6.770e-07
D1 to Z	9.135e-07	1.700e-08	5.140e-07	-4.215e-07
S0 to Z	8.838e-07	8.304e-07	3.998e-08	-3.429e-07

CNMUX41

Cell Description

4:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	2.400	2.176	5.2224
X17_P4	2.400	2.176	5.2224
X17_P10	2.400	2.176	5.2224
X17_P16	2.400	2.176	5.2224
X27_P0	2.400	2.312	5.5488
X27_P4	2.400	2.312	5.5488
X27_P10	2.400	2.312	5.5488
X27_P16	2.400	2.312	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0017	0.0018	0.0019	0.0020
D1	0.0016	0.0017	0.0018	0.0019
D2	0.0017	0.0018	0.0019	0.0020
D3	0.0017	0.0018	0.0019	0.0020
S0	0.0042	0.0044	0.0048	0.0051
S1	0.0023	0.0024	0.0025	0.0027

	X27_P0	X27_P4	X27_P10	X27_P16
D0	0.0016	0.0017	0.0017	0.0018
D1	0.0015	0.0016	0.0017	0.0018
D2	0.0015	0.0016	0.0016	0.0017
D3	0.0015	0.0015	0.0016	0.0017
S0	0.0037	0.0039	0.0041	0.0044
S1	0.0020	0.0021	0.0023	0.0025

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
D0 to Z ↓	0.0383	0.0441	0.8012	0.8598
D0 to Z ↑	0.0283	0.0316	1.1427	1.2690
D1 to Z ↓	0.0379	0.0437	0.8014	0.8592
D1 to Z ↑	0.0279	0.0312	1.1414	1.2687
D2 to Z ↓	0.0388	0.0448	0.8016	0.8596
D2 to Z ↑	0.0277	0.0311	1.1403	1.2664
D3 to Z ↓	0.0385	0.0444	0.8015	0.8592
D3 to Z ↑	0.0276	0.0308	1.1399	1.2662
S0 to Z ↓	0.0447	0.0515	0.7998	0.8576
S0 to Z ↑	0.0380	0.0430	1.1423	1.2684
S1 to Z ↓	0.0303	0.0342	0.8005	0.8581
S1 to Z ↑	0.0293	0.0327	1.1416	1.2678
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0527	0.0613	0.9437	1.0234
D0 to Z ↑	0.0369	0.0424	1.4736	1.6714
D1 to Z ↓	0.0521	0.0606	0.9439	1.0226
D1 to Z ↑	0.0365	0.0419	1.4726	1.6714
D2 to Z ↓	0.0537	0.0625	0.9445	1.0234
D2 to Z ↑	0.0364	0.0417	1.4722	1.6688
D3 to Z ↓	0.0533	0.0621	0.9442	1.0227
D3 to Z ↑	0.0361	0.0414	1.4713	1.6687
S0 to Z ↓	0.0619	0.0722	0.9419	1.0213
S0 to Z ↑	0.0509	0.0589	1.4740	1.6716
S1 to Z ↓	0.0403	0.0464	0.9422	1.0215
S1 to Z ↑	0.0380	0.0430	1.4739	1.6716
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0433	0.0497	0.5095	0.5479
D0 to Z ↑	0.0362	0.0404	0.7690	0.8545
D1 to Z ↓	0.0391	0.0449	0.5022	0.5393
D1 to Z ↑	0.0351	0.0392	0.7684	0.8540
D2 to Z ↓	0.0450	0.0520	0.5109	0.5499
D2 to Z ↑	0.0356	0.0399	0.7680	0.8529
D3 to Z ↓	0.0446	0.0515	0.5106	0.5494
D3 to Z ↑	0.0352	0.0394	0.7676	0.8528
S0 to Z ↓	0.0495	0.0570	0.5067	0.5450
S0 to Z ↑	0.0444	0.0502	0.7694	0.8543
S1 to Z ↓	0.0328	0.0373	0.5078	0.5457
S1 to Z ↑	0.0407	0.0453	0.7683	0.8535
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.0597	0.0694	0.6048	0.6584
D0 to Z ↑	0.0475	0.0546	0.9928	1.1257

D1 to Z ↓	0.0538	0.0624	0.5944	0.6455
D1 to Z ↑	0.0462	0.0531	0.9926	1.1251
D2 to Z ↓	0.0626	0.0730	0.6074	0.6616
D2 to Z ↑	0.0468	0.0537	0.9913	1.1245
D3 to Z ↓	0.0621	0.0724	0.6075	0.6613
D3 to Z ↑	0.0463	0.0532	0.9909	1.1242
S0 to Z ↓	0.0685	0.0798	0.6016	0.6546
S0 to Z ↑	0.0596	0.0689	0.9929	1.1260
S1 to Z ↓	0.0445	0.0515	0.6025	0.6556
S1 to Z ↑	0.0529	0.0600	0.9918	1.1253

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P0	3.233e-04	4.247e-09
X17_P4	1.045e-04	4.247e-09
X17_P10	3.813e-05	4.247e-09
X17_P16	2.436e-05	4.247e-09
X27_P0	3.394e-04	4.452e-09
X27_P4	1.087e-04	4.452e-09
X27_P10	3.865e-05	4.452e-09
X27_P16	2.406e-05	4.452e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	1.850e-04	1.137e-04	8.741e-05	2.180e-04
D1 (output stable)	1.426e-04	1.054e-04	9.376e-05	1.902e-04
D2 (output stable)	1.889e-04	1.289e-04	9.639e-05	1.231e-04
D3 (output stable)	1.821e-04	1.431e-04	1.387e-04	2.234e-04
S0 (output stable)	5.248e-03	5.277e-03	5.551e-03	6.063e-03
S1 (output stable)	4.663e-03	4.249e-03	4.198e-03	4.217e-03
D0 to Z	1.199e-02	1.171e-02	1.175e-02	1.203e-02
D1 to Z	1.195e-02	1.168e-02	1.173e-02	1.202e-02
D2 to Z	1.227e-02	1.200e-02	1.211e-02	1.241e-02
D3 to Z	1.214e-02	1.187e-02	1.196e-02	1.228e-02
S0 to Z	1.777e-02	1.770e-02	1.820e-02	1.906e-02
S1 to Z	1.407e-02	1.288e-02	1.216e-02	1.216e-02
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	1.774e-04	1.012e-04	8.528e-05	2.144e-04
D1 (output stable)	1.403e-04	1.069e-04	1.024e-04	1.944e-04
D2 (output stable)	1.755e-04	1.140e-04	9.459e-05	1.224e-04
D3 (output stable)	1.690e-04	1.283e-04	1.384e-04	2.210e-04
S0 (output stable)	4.909e-03	4.898e-03	5.138e-03	5.595e-03
S1 (output stable)	4.115e-03	3.779e-03	3.756e-03	3.778e-03
D0 to Z	1.603e-02	1.519e-02	1.488e-02	1.500e-02
D1 to Z	1.554e-02	1.478e-02	1.452e-02	1.468e-02
D2 to Z	1.621e-02	1.543e-02	1.512e-02	1.526e-02
D3 to Z	1.606e-02	1.527e-02	1.497e-02	1.512e-02
S0 to Z	2.119e-02	2.056e-02	2.063e-02	2.127e-02
S1 to Z	1.754e-02	1.592e-02	1.493e-02	1.485e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

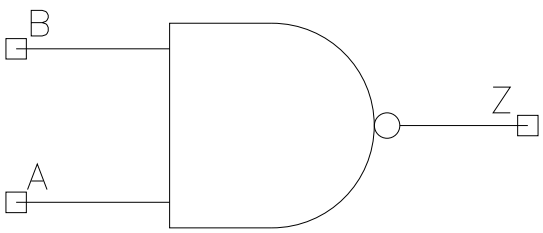
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	1.417e-06	1.877e-05	2.552e-05	1.929e-06
D1 (output stable)	1.261e-06	1.303e-05	1.841e-05	4.516e-06
D2 (output stable)	1.448e-06	1.895e-05	2.638e-05	1.730e-05
D3 (output stable)	1.535e-06	1.937e-05	2.586e-05	9.085e-06
S0 (output stable)	1.960e-06	2.154e-07	-1.762e-05	-5.577e-05
S1 (output stable)	2.778e-06	1.355e-04	1.875e-04	1.329e-04
D0 to Z	3.846e-07	4.971e-07	1.483e-06	-3.914e-06
D1 to Z	1.006e-06	1.692e-06	3.697e-06	-2.764e-06
D2 to Z	7.545e-07	1.396e-06	2.589e-06	-4.054e-06
D3 to Z	8.174e-07	2.286e-06	5.597e-06	-2.512e-06
S0 to Z	4.599e-06	3.852e-06	-8.967e-06	-4.435e-05
S1 to Z	4.221e-07	1.080e-04	1.892e-04	1.715e-04
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	1.608e-06	2.041e-05	2.265e-05	5.108e-07
D1 (output stable)	1.293e-06	1.252e-05	1.651e-05	3.269e-06
D2 (output stable)	1.764e-06	1.988e-05	2.259e-05	1.308e-05
D3 (output stable)	1.796e-06	2.070e-05	2.135e-05	3.790e-06
S0 (output stable)	1.942e-06	-5.185e-07	-2.182e-05	-5.999e-05
S1 (output stable)	6.683e-06	1.397e-04	1.779e-04	1.229e-04
D0 to Z	2.644e-07	8.519e-07	1.096e-06	-4.275e-06
D1 to Z	8.966e-07	1.799e-06	3.041e-06	-4.717e-06
D2 to Z	2.319e-07	1.714e-06	1.059e-06	-6.063e-06
D3 to Z	3.300e-07	3.479e-06	2.851e-06	-4.217e-06
S0 to Z	4.282e-06	3.278e-06	-1.221e-05	-4.726e-05
S1 to Z	5.777e-07	1.100e-04	1.858e-04	1.651e-04

CNNAND2

Cell Description

2 input NAND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X33_P0	1.200	1.224	1.4688
X33_P4	1.200	1.224	1.4688
X33_P10	1.200	1.224	1.4688
X33_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0022	0.0023	0.0024	0.0026
B	0.0021	0.0022	0.0023	0.0024
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0008	0.0009	0.0010	0.0010
B	0.0008	0.0008	0.0009	0.0010

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0041	0.0049	0.9850	1.0534
A to Z ↑	0.0116	0.0130	1.1668	1.2935
B to Z ↓	0.0044	0.0050	1.0019	1.0738
B to Z ↑	0.0092	0.0101	1.1764	1.3033
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0063	0.0075	1.1584	1.2555
A to Z ↑	0.0149	0.0168	1.4995	1.6959
B to Z ↓	0.0060	0.0069	1.1801	1.2799
B to Z ↑	0.0115	0.0127	1.5116	1.7084
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0253	0.0286	0.3865	0.4127
A to Z ↑	0.0314	0.0356	0.5629	0.6252
B to Z ↓	0.0267	0.0301	0.3864	0.4129
B to Z ↑	0.0304	0.0344	0.5636	0.6258
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0344	0.0402	0.4519	0.4874
A to Z ↑	0.0425	0.0493	0.7268	0.8237
B to Z ↓	0.0361	0.0420	0.4516	0.4874
B to Z ↑	0.0410	0.0475	0.7270	0.8231

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X15_P0	1.042e-04	1.642e-09
X15_P4	3.421e-05	1.642e-09
X15_P10	1.189e-05	1.642e-09
X15_P16	6.986e-06	1.642e-09
X33_P0	2.747e-04	1.973e-09
X33_P4	8.582e-05	1.973e-09
X33_P10	2.713e-05	1.973e-09
X33_P16	1.435e-05	1.973e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.636e-04	1.468e-04	1.326e-04	1.251e-04
B (output stable)	2.671e-04	2.762e-04	3.534e-04	4.385e-04
A to Z	4.610e-03	4.063e-03	3.725e-03	3.631e-03
B to Z	3.901e-03	3.192e-03	2.658e-03	2.404e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	2.736e-05	2.471e-05	2.273e-05	2.104e-05
B (output stable)	3.368e-05	3.419e-05	3.450e-05	4.309e-05
A to Z	1.281e-02	1.249e-02	1.276e-02	1.321e-02
B to Z	1.268e-02	1.233e-02	1.255e-02	1.296e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

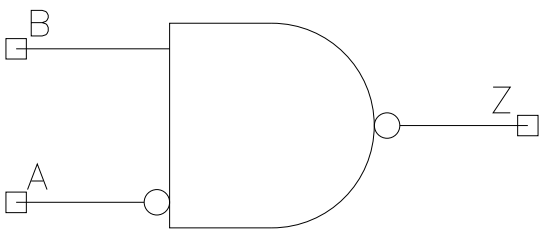
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	5.900e-08	1.870e-08	-5.460e-08	-9.120e-08
B (output stable)	3.910e-08	1.410e-08	-2.510e-08	-8.800e-08
A to Z	1.300e-06	-3.220e-07	-8.000e-08	2.410e-07
B to Z	2.070e-07	-4.400e-08	3.420e-07	2.531e-06
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	8.404e-08	7.840e-08	5.245e-08	2.725e-08
B (output stable)	9.870e-08	8.860e-08	7.570e-08	5.860e-08
A to Z	2.950e-07	6.000e-08	-1.600e-07	-4.048e-07
B to Z	5.900e-08	-5.000e-10	-1.395e-07	-3.267e-07

CNNAND2A

Cell Description

2 input NAND with A input inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0009	0.0009	0.0010	0.0011
B	0.0010	0.0010	0.0011	0.0012
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0013	0.0013	0.0015	0.0015
B	0.0009	0.0010	0.0011	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0225	0.0259	0.7550	0.8090
A to Z ↑	0.0188	0.0211	1.1206	1.2448
B to Z ↓	0.0240	0.0272	0.7534	0.8072
B to Z ↑	0.0251	0.0282	1.1185	1.2428
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**

A to Z ↓	0.0313	0.0362	0.8880	0.9601
A to Z ↑	0.0247	0.0278	1.4480	1.6409
B to Z ↓	0.0330	0.0382	0.8862	0.9586
B to Z ↑	0.0333	0.0378	1.4474	1.6402
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0247	0.0285	0.4519	0.4841
A to Z ↑	0.0215	0.0240	0.7252	0.8043
B to Z ↓	0.0256	0.0291	0.4504	0.4826
B to Z ↑	0.0279	0.0315	0.7231	0.8016
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0344	0.0399	0.5325	0.5774
A to Z ↑	0.0282	0.0319	0.9352	1.0604
B to Z ↓	0.0350	0.0409	0.5317	0.5765
B to Z ↑	0.0373	0.0429	0.9313	1.0581

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X17_P0	1.818e-04	1.642e-09
X17_P4	5.847e-05	1.642e-09
X17_P10	1.861e-05	1.642e-09
X17_P16	9.736e-06	1.642e-09
X27_P0	2.585e-04	2.304e-09
X27_P4	8.324e-05	2.304e-09
X27_P10	2.630e-05	2.304e-09
X27_P16	1.366e-05	2.304e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	5.956e-05	5.979e-05	5.927e-05	5.882e-05
B (output stable)	2.269e-03	1.977e-03	1.774e-03	1.701e-03
A to Z	6.500e-03	6.147e-03	6.113e-03	6.116e-03
B to Z	8.322e-03	7.947e-03	7.964e-03	8.009e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.703e-04	1.703e-04	1.660e-04	3.208e-04
B (output stable)	2.443e-03	2.191e-03	1.978e-03	1.974e-03
A to Z	1.081e-02	1.020e-02	1.012e-02	1.024e-02
B to Z	1.204e-02	1.159e-02	1.164e-02	1.188e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

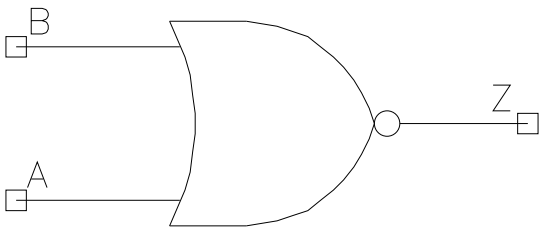
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	2.953e-07	2.444e-07	-3.404e-07	-1.432e-06
B (output stable)	3.420e-07	6.498e-06	2.474e-05	2.561e-05
A to Z	2.095e-07	2.203e-07	-3.290e-08	-4.347e-07
B to Z	7.315e-07	1.470e-06	3.607e-07	-2.057e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	7.308e-07	3.405e-07	-4.483e-06	-4.946e-05
B (output stable)	1.637e-06	5.644e-05	8.143e-05	8.449e-05
A to Z	1.870e-07	4.700e-07	-9.090e-07	-3.595e-06
B to Z	3.950e-07	-1.021e-06	-7.170e-07	-2.836e-07

CNNOR2

Cell Description

2 input NOR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	0.952	1.1424
X14_P4	1.200	0.952	1.1424
X14_P10	1.200	0.952	1.1424
X14_P16	1.200	0.952	1.1424
X33_P0	1.200	1.496	1.7952
X33_P4	1.200	1.496	1.7952
X33_P10	1.200	1.496	1.7952
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0024	0.0025	0.0027	0.0028
B	0.0023	0.0023	0.0024	0.0025
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0010	0.0010	0.0011	0.0011
B	0.0010	0.0010	0.0011	0.0011

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0070	0.0080	0.8675	0.9240
A to Z ↑	0.0095	0.0113	1.5022	1.6585
B to Z ↓	0.0045	0.0052	0.8792	0.9356
B to Z ↑	0.0093	0.0103	1.5174	1.6763
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**

A to Z ↓	0.0094	0.0108	1.0031	1.0748
A to Z ↑	0.0135	0.0158	1.9006	2.1320
B to Z ↓	0.0063	0.0072	1.0181	1.0909
B to Z ↑	0.0117	0.0129	1.9204	2.1548
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0293	0.0332	0.3819	0.4086
A to Z ↑	0.0283	0.0327	0.5622	0.6232
B to Z ↓	0.0275	0.0313	0.3817	0.4082
B to Z ↑	0.0295	0.0337	0.5615	0.6236
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0393	0.0458	0.4468	0.4824
A to Z ↑	0.0392	0.0460	0.7241	0.8210
B to Z ↓	0.0372	0.0436	0.4469	0.4825
B to Z ↑	0.0397	0.0462	0.7242	0.8212

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X14_P0	1.107e-04	1.642e-09
X14_P4	3.194e-05	1.642e-09
X14_P10	1.033e-05	1.642e-09
X14_P16	6.097e-06	1.642e-09
X33_P0	3.191e-04	2.304e-09
X33_P4	9.619e-05	2.304e-09
X33_P10	3.030e-05	2.304e-09
X33_P16	1.658e-05	2.304e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	2.455e-04	2.518e-04	2.518e-04	2.641e-04
B (output stable)	4.495e-04	3.666e-04	1.520e-04	1.108e-04
A to Z	5.081e-03	4.558e-03	4.268e-03	4.276e-03
B to Z	3.969e-03	3.252e-03	2.712e-03	2.453e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	6.077e-05	6.087e-05	6.141e-05	6.273e-05
B (output stable)	9.418e-05	8.400e-05	3.112e-05	1.581e-05
A to Z	1.426e-02	1.400e-02	1.408e-02	1.465e-02
B to Z	1.400e-02	1.368e-02	1.366e-02	1.418e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

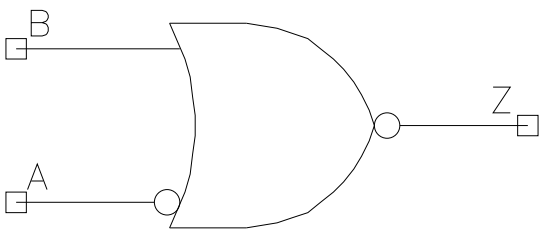
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	5.110e-07	5.220e-07	-2.512e-06	-6.074e-06
B (output stable)	1.456e-06	4.161e-05	8.575e-05	8.596e-05
A to Z	6.323e-06	4.779e-06	2.124e-06	-8.590e-07
B to Z	-2.240e-07	-5.800e-08	3.022e-06	1.650e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	3.081e-07	2.594e-07	-3.668e-07	-1.368e-06
B (output stable)	5.023e-07	4.934e-06	2.431e-05	2.613e-05
A to Z	-3.510e-07	-6.600e-08	-4.770e-07	-1.004e-06
B to Z	-3.910e-07	-4.250e-07	-5.830e-07	-3.350e-07

CNNOR2A

Cell Description

2 input NOR with A input Inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	1.224	1.4688
X15_P4	1.200	1.224	1.4688
X15_P10	1.200	1.224	1.4688
X15_P16	1.200	1.224	1.4688
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0014	0.0014	0.0015	0.0016
B	0.0009	0.0010	0.0011	0.0011
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0016	0.0017	0.0018	0.0020
B	0.0010	0.0010	0.0011	0.0012

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0245	0.0276	0.9281	0.9934
A to Z ↑	0.0150	0.0171	1.1236	1.2486
B to Z ↓	0.0225	0.0255	0.9216	0.9876
B to Z ↑	0.0237	0.0268	1.1206	1.2459
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0324	0.0371	1.0891	1.1786
A to Z ↑	0.0203	0.0234	1.4522	1.6481
B to Z ↓	0.0306	0.0357	1.0826	1.1711
B to Z ↑	0.0315	0.0360	1.4491	1.6454
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0211	0.0238	0.5204	0.5574
A to Z ↑	0.0170	0.0189	0.5977	0.6638
B to Z ↓	0.0229	0.0261	0.5203	0.5563
B to Z ↑	0.0260	0.0295	0.5973	0.6630
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0282	0.0322	0.6110	0.6606
A to Z ↑	0.0222	0.0253	0.7707	0.8744
B to Z ↓	0.0314	0.0367	0.6104	0.6597
B to Z ↑	0.0346	0.0398	0.7699	0.8726

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X15_P0	1.691e-04	1.973e-09
X15_P4	4.794e-05	1.973e-09
X15_P10	1.502e-05	1.973e-09
X15_P16	8.525e-06	1.973e-09
X27_P0	2.620e-04	2.304e-09
X27_P4	7.150e-05	2.304e-09
X27_P10	2.204e-05	2.304e-09
X27_P16	1.258e-05	2.304e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.024e-04	9.100e-05	8.122e-05	7.524e-05
B (output stable)	2.424e-03	2.155e-03	2.073e-03	2.068e-03
A to Z	6.577e-03	6.277e-03	6.211e-03	6.315e-03
B to Z	8.096e-03	7.818e-03	7.804e-03	7.976e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.399e-04	1.264e-04	1.141e-04	1.084e-04
B (output stable)	2.702e-03	2.471e-03	2.441e-03	2.505e-03
A to Z	1.096e-02	1.032e-02	1.021e-02	1.029e-02
B to Z	1.249e-02	1.209e-02	1.219e-02	1.248e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

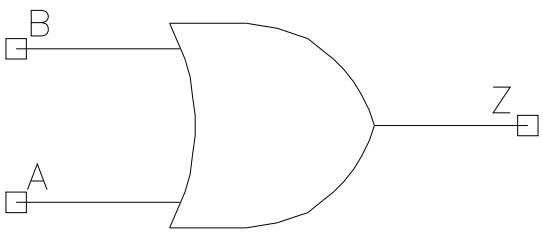
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.001e-07	9.480e-08	7.050e-08	5.660e-08
B (output stable)	1.275e-06	1.214e-06	-2.970e-07	-1.965e-06
A to Z	2.551e-06	1.327e-06	-7.180e-08	-1.623e-07
B to Z	8.039e-07	-4.009e-07	-4.110e-08	1.226e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	7.810e-08	6.330e-08	3.000e-09	-1.710e-08
B (output stable)	1.255e-06	5.595e-07	2.167e-07	2.606e-07
A to Z	-1.704e-07	2.488e-07	2.570e-08	-6.171e-07
B to Z	8.448e-07	8.005e-07	6.490e-08	-3.071e-07

CNOR2

Cell Description

2 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X20_P0	1.200	1.360	1.6320
X20_P4	1.200	1.360	1.6320
X20_P10	1.200	1.360	1.6320
X20_P16	1.200	1.360	1.6320
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320
X37_P0	1.200	1.632	1.9584
X37_P4	1.200	1.632	1.9584
X37_P10	1.200	1.632	1.9584
X37_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0017	0.0018	0.0019	0.0020
B	0.0016	0.0016	0.0018	0.0019
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0025	0.0027	0.0029	0.0031
B	0.0026	0.0028	0.0030	0.0032
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0018	0.0019	0.0020	0.0022

B	0.0018	0.0019	0.0020	0.0022
	X37_P0	X37_P4	X37_P10	X37_P16
A	0.0026	0.0027	0.0030	0.0031
B	0.0026	0.0028	0.0029	0.0032

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0185	0.0212	0.8492	0.9085
A to Z ↑	0.0142	0.0160	1.1696	1.3001
B to Z ↓	0.0188	0.0210	0.8483	0.9069
B to Z ↑	0.0126	0.0142	1.1695	1.2994
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0256	0.0296	0.9942	1.0736
A to Z ↑	0.0189	0.0214	1.5152	1.7196
B to Z ↓	0.0248	0.0281	0.9964	1.0757
B to Z ↑	0.0168	0.0190	1.5124	1.7187
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0173	0.0200	0.6584	0.7048
A to Z ↑	0.0148	0.0166	0.8127	0.9028
B to Z ↓	0.0175	0.0197	0.6586	0.7047
B to Z ↑	0.0127	0.0143	0.8120	0.9018
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0239	0.0277	0.7727	0.8346
A to Z ↑	0.0193	0.0219	1.0491	1.1892
B to Z ↓	0.0231	0.0263	0.7724	0.8341
B to Z ↑	0.0167	0.0189	1.0474	1.1876
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0228	0.0262	0.3858	0.4132
A to Z ↑	0.0179	0.0201	0.5524	0.6148
B to Z ↓	0.0231	0.0261	0.3856	0.4128
B to Z ↑	0.0160	0.0180	0.5513	0.6139
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0315	0.0366	0.4531	0.4897
A to Z ↑	0.0234	0.0265	0.7147	0.8118
B to Z ↓	0.0307	0.0351	0.4533	0.4900
B to Z ↑	0.0210	0.0238	0.7144	0.8109
	X37_P0	**X37_P4**	**X37_P0**	**X37_P4**
A to Z ↓	0.0206	0.0239	0.3697	0.3958
A to Z ↑	0.0171	0.0193	0.4514	0.5015
B to Z ↓	0.0211	0.0241	0.3693	0.3958
B to Z ↑	0.0152	0.0172	0.4509	0.5005
	X37_P10	**X37_P16**	**X37_P10**	**X37_P16**
A to Z ↓	0.0286	0.0332	0.4344	0.4696
A to Z ↑	0.0223	0.0252	0.5822	0.6605
B to Z ↓	0.0282	0.0323	0.4342	0.4698
B to Z ↑	0.0199	0.0225	0.5820	0.6594

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X15_P0	1.523e-04	1.642e-09

X15_P4	4.850e-05	1.642e-09
X15_P10	1.556e-05	1.642e-09
X15_P16	8.385e-06	1.642e-09
X20_P0	2.328e-04	2.139e-09
X20_P4	7.249e-05	2.139e-09
X20_P10	2.305e-05	2.139e-09
X20_P16	1.243e-05	2.139e-09
X33_P0	2.597e-04	2.139e-09
X33_P4	8.567e-05	2.139e-09
X33_P10	2.775e-05	2.139e-09
X33_P16	1.468e-05	2.139e-09
X37_P0	3.183e-04	2.470e-09
X37_P4	1.011e-04	2.470e-09
X37_P10	3.211e-05	2.470e-09
X37_P16	1.702e-05	2.470e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.409e-04	1.433e-04	1.459e-04	1.503e-04
B (output stable)	2.708e-04	2.126e-04	1.026e-04	7.679e-05
A to Z	6.806e-03	6.384e-03	6.365e-03	6.449e-03
B to Z	6.155e-03	5.609e-03	5.424e-03	5.374e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.503e-04	2.533e-04	2.532e-04	2.633e-04
B (output stable)	4.606e-04	3.697e-04	1.498e-04	1.114e-04
A to Z	1.031e-02	9.823e-03	9.667e-03	9.886e-03
B to Z	9.150e-03	8.468e-03	8.065e-03	8.050e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.870e-04	1.868e-04	1.897e-04	1.970e-04
B (output stable)	4.165e-04	3.094e-04	1.618e-04	1.305e-04
A to Z	1.284e-02	1.217e-02	1.197e-02	1.219e-02
B to Z	1.197e-02	1.115e-02	1.075e-02	1.080e-02
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	2.514e-04	2.541e-04	2.549e-04	2.616e-04
B (output stable)	4.645e-04	3.719e-04	1.576e-04	1.113e-04
A to Z	1.512e-02	1.451e-02	1.424e-02	1.448e-02
B to Z	1.398e-02	1.316e-02	1.265e-02	1.268e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	3.038e-07	2.686e-07	-1.680e-06	-3.772e-06
B (output stable)	9.650e-07	2.727e-05	5.321e-05	5.254e-05
A to Z	2.846e-06	1.509e-06	5.897e-07	-1.261e-06
B to Z	5.830e-08	-1.296e-07	4.554e-07	-1.563e-07
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	4.636e-07	4.567e-07	-2.569e-06	-6.202e-06
B (output stable)	1.558e-06	4.324e-05	8.559e-05	8.643e-05
A to Z	5.376e-06	1.988e-06	1.024e-06	-2.081e-06
B to Z	-1.289e-06	-4.482e-07	1.557e-06	-8.583e-07
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	8.047e-07	5.273e-07	-3.678e-06	-8.055e-06

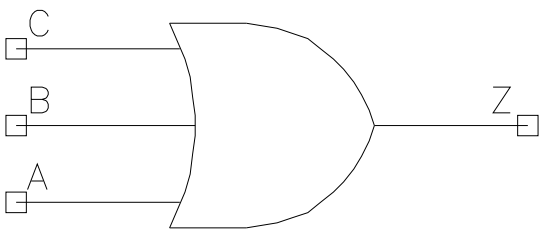
B (output stable)	1.615e-06	6.245e-05	1.083e-04	1.084e-04
A to Z	8.720e-07	4.290e-07	6.810e-07	-3.555e-06
B to Z	2.080e-06	6.693e-07	-4.097e-07	-8.209e-07
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	4.688e-07	4.588e-07	-2.747e-06	-6.172e-06
B (output stable)	1.558e-06	4.359e-05	8.633e-05	8.536e-05
A to Z	1.382e-06	4.640e-07	5.470e-07	-2.491e-06
B to Z	-5.783e-07	1.601e-06	-4.558e-07	-7.729e-07

CNOR3

Cell Description

3 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	1.360	1.6320
X14_P4	1.200	1.360	1.6320
X14_P10	1.200	1.360	1.6320
X14_P16	1.200	1.360	1.6320
X20_P0	1.200	1.632	1.9584
X20_P4	1.200	1.632	1.9584
X20_P10	1.200	1.632	1.9584
X20_P16	1.200	1.632	1.9584
X27_P0	1.200	2.040	2.4480
X27_P4	1.200	2.040	2.4480
X27_P10	1.200	2.040	2.4480
X27_P16	1.200	2.040	2.4480

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0010	0.0010	0.0011	0.0012
B	0.0009	0.0010	0.0011	0.0011
C	0.0009	0.0010	0.0011	0.0012
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0009	0.0010	0.0011	0.0011
B	0.0009	0.0010	0.0011	0.0011
C	0.0009	0.0010	0.0011	0.0011
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0013	0.0013	0.0014	0.0015
B	0.0013	0.0014	0.0015	0.0015

C	0.0010	0.0010	0.0011	0.0012

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0359	0.0408	0.9248	0.9904
A to Z ↑	0.0287	0.0328	1.1795	1.3094
B to Z ↓	0.0350	0.0403	0.9236	0.9895
B to Z ↑	0.0305	0.0347	1.1797	1.3091
C to Z ↓	0.0332	0.0376	0.9238	0.9888
C to Z ↑	0.0264	0.0300	1.1785	1.3071
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0485	0.0563	1.0865	1.1742
A to Z ↑	0.0390	0.0451	1.5204	1.7250
B to Z ↓	0.0486	0.0568	1.0871	1.1743
B to Z ↑	0.0412	0.0475	1.5218	1.7250
C to Z ↓	0.0446	0.0516	1.0855	1.1726
C to Z ↑	0.0357	0.0413	1.5191	1.7231
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0359	0.0406	0.6810	0.7288
A to Z ↑	0.0311	0.0353	0.8313	0.9229
B to Z ↓	0.0351	0.0401	0.6808	0.7286
B to Z ↑	0.0326	0.0371	0.8322	0.9221
C to Z ↓	0.0324	0.0365	0.6808	0.7284
C to Z ↑	0.0296	0.0334	0.8323	0.9225
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0485	0.0562	0.7990	0.8634
A to Z ↑	0.0426	0.0497	1.0707	1.2124
B to Z ↓	0.0485	0.0566	0.7992	0.8628
B to Z ↑	0.0445	0.0517	1.0707	1.2114
C to Z ↓	0.0435	0.0504	0.7990	0.8626
C to Z ↑	0.0401	0.0466	1.0705	1.2126
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0262	0.0303	0.5665	0.6088
A to Z ↑	0.0304	0.0341	0.6864	0.7627
B to Z ↓	0.0266	0.0304	0.5667	0.6091
B to Z ↑	0.0282	0.0315	0.6858	0.7617
C to Z ↓	0.0248	0.0281	0.5610	0.6033
C to Z ↑	0.0236	0.0264	0.5596	0.6230
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0364	0.0423	0.6732	0.7341
A to Z ↑	0.0399	0.0455	0.8865	1.0066
B to Z ↓	0.0361	0.0416	0.6731	0.7344
B to Z ↑	0.0367	0.0418	0.8850	1.0039
C to Z ↓	0.0330	0.0378	0.6663	0.7251
C to Z ↑	0.0305	0.0345	0.7249	0.8239

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X14_P0	2.210e-04	2.139e-09
X14_P4	7.079e-05	2.139e-09

X14_P10	2.289e-05	2.139e-09
X14_P16	1.231e-05	2.139e-09
X20_P0	2.672e-04	2.504e-09
X20_P4	8.670e-05	2.504e-09
X20_P10	2.794e-05	2.504e-09
X20_P16	1.482e-05	2.504e-09
X27_P0	2.297e-04	3.069e-09
X27_P4	7.574e-05	3.069e-09
X27_P10	2.587e-05	3.069e-09
X27_P16	1.460e-05	3.069e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	8.281e-04	7.695e-04	7.159e-04	7.143e-04
B (output stable)	9.039e-04	8.722e-04	8.811e-04	9.120e-04
C (output stable)	2.139e-03	1.910e-03	1.765e-03	1.734e-03
A to Z	9.125e-03	9.015e-03	9.136e-03	9.410e-03
B to Z	9.403e-03	9.348e-03	9.554e-03	9.886e-03
C to Z	9.068e-03	8.878e-03	8.932e-03	9.150e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	8.069e-04	7.475e-04	6.929e-04	6.893e-04
B (output stable)	8.810e-04	8.455e-04	8.490e-04	8.763e-04
C (output stable)	2.034e-03	1.792e-03	1.638e-03	1.598e-03
A to Z	1.113e-02	1.088e-02	1.107e-02	1.140e-02
B to Z	1.140e-02	1.121e-02	1.147e-02	1.186e-02
C to Z	1.101e-02	1.069e-02	1.081e-02	1.109e-02
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	2.066e-03	2.111e-03	2.230e-03	2.364e-03
B (output stable)	1.915e-03	1.909e-03	1.940e-03	2.035e-03
C (output stable)	4.595e-03	4.556e-03	4.756e-03	5.084e-03
A to Z	1.385e-02	1.358e-02	1.378e-02	1.419e-02
B to Z	1.326e-02	1.290e-02	1.300e-02	1.333e-02
C to Z	1.223e-02	1.161e-02	1.126e-02	1.133e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	3.960e-07	3.268e-06	1.611e-05	1.718e-05
B (output stable)	2.950e-07	2.128e-07	-1.638e-07	-9.334e-07
C (output stable)	8.530e-07	8.622e-07	5.584e-07	4.259e-07
A to Z	1.423e-06	9.762e-08	3.560e-07	-1.830e-07
B to Z	1.047e-06	5.183e-07	1.521e-07	-2.446e-07
C to Z	-3.077e-07	1.751e-06	7.787e-07	4.147e-07
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	3.345e-07	3.379e-06	1.553e-05	1.647e-05
B (output stable)	3.947e-07	2.562e-07	-1.831e-07	-9.295e-07
C (output stable)	7.620e-07	1.171e-06	9.515e-07	5.320e-07
A to Z	3.810e-08	8.711e-07	2.444e-07	4.150e-08
B to Z	1.153e-06	1.093e-07	5.190e-08	-2.597e-07
C to Z	3.810e-08	9.289e-07	4.534e-07	5.940e-08
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	2.756e-07	2.503e-07	-7.480e-07	-2.150e-06

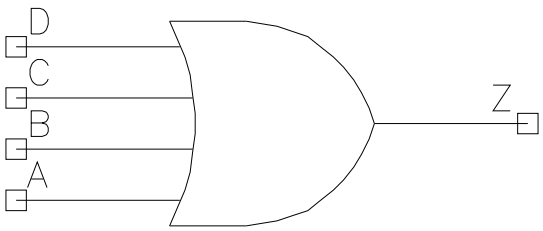
B (output stable)	4.321e-07	9.336e-06	2.648e-05	2.615e-05
C (output stable)	2.036e-07	2.542e-07	-7.070e-07	-2.124e-06
A to Z	-7.400e-08	6.500e-08	-2.843e-07	-1.092e-06
B to Z	-3.240e-07	-2.220e-07	-1.840e-07	-3.130e-07
C to Z	-1.290e-07	-3.000e-08	-1.510e-07	-2.690e-07

CNOR4

Cell Description

4 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X20_P4	1.200	2.176	2.6112
X20_P10	1.200	2.176	2.6112
X20_P16	1.200	2.176	2.6112
X27_P0	1.200	2.312	2.7744
X27_P4	1.200	2.312	2.7744
X27_P10	1.200	2.312	2.7744
X27_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0014	0.0014	0.0015	0.0016
B	0.0015	0.0016	0.0017	0.0018
C	0.0014	0.0015	0.0016	0.0017
D	0.0015	0.0016	0.0017	0.0018
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0014	0.0014	0.0015	0.0016
B	0.0015	0.0016	0.0017	0.0018
C	0.0014	0.0015	0.0016	0.0017
D	0.0016	0.0017	0.0018	0.0019

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0242	0.0280	0.6430	0.6914
A to Z ↑	0.0237	0.0268	0.9668	1.0729
B to Z ↓	0.0236	0.0270	0.6432	0.6915
B to Z ↑	0.0220	0.0248	0.9664	1.0726
C to Z ↓	0.0234	0.0268	0.6407	0.6890
C to Z ↑	0.0227	0.0254	0.9597	1.0661
D to Z ↓	0.0233	0.0264	0.6400	0.6887
D to Z ↑	0.0211	0.0234	0.9581	1.0644
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0334	0.0388	0.7642	0.8332
A to Z ↑	0.0314	0.0361	1.2477	1.4162
B to Z ↓	0.0319	0.0368	0.7642	0.8332
B to Z ↑	0.0289	0.0333	1.2471	1.4148
C to Z ↓	0.0322	0.0366	0.7624	0.8303
C to Z ↑	0.0297	0.0332	1.2407	1.4085
D to Z ↓	0.0313	0.0352	0.7620	0.8304
D to Z ↑	0.0274	0.0306	1.2392	1.4074
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0266	0.0305	0.5314	0.5711
A to Z ↑	0.0254	0.0285	0.7238	0.8033
B to Z ↓	0.0262	0.0298	0.5310	0.5714
B to Z ↑	0.0238	0.0266	0.7229	0.8021
C to Z ↓	0.0246	0.0283	0.5285	0.5682
C to Z ↑	0.0232	0.0261	0.7175	0.7975
D to Z ↓	0.0245	0.0280	0.5279	0.5679
D to Z ↑	0.0211	0.0238	0.7162	0.7964
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0365	0.0422	0.6314	0.6895
A to Z ↑	0.0335	0.0381	0.9332	1.0606
B to Z ↓	0.0353	0.0404	0.6319	0.6900
B to Z ↑	0.0313	0.0355	0.9336	1.0598
C to Z ↓	0.0337	0.0391	0.6279	0.6851
C to Z ↑	0.0303	0.0344	0.9281	1.0558
D to Z ↓	0.0329	0.0377	0.6279	0.6850
D to Z ↑	0.0275	0.0312	0.9265	1.0528

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X20_P0	2.117e-04	3.271e-09
X20_P4	7.096e-05	3.271e-09
X20_P10	2.495e-05	3.271e-09
X20_P16	1.451e-05	3.271e-09
X27_P0	2.336e-04	3.443e-09
X27_P4	7.919e-05	3.443e-09
X27_P10	2.811e-05	3.443e-09
X27_P16	1.642e-05	3.443e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.380e-03	2.414e-03	2.507e-03	2.658e-03

B (output stable)	2.188e-03	2.147e-03	2.135e-03	2.232e-03
C (output stable)	2.232e-03	2.201e-03	2.343e-03	2.461e-03
D (output stable)	2.032e-03	1.927e-03	1.956e-03	2.013e-03
A to Z	1.133e-02	1.126e-02	1.152e-02	1.201e-02
B to Z	1.084e-02	1.063e-02	1.074e-02	1.114e-02
C to Z	1.078e-02	1.038e-02	1.042e-02	1.045e-02
D to Z	1.028e-02	9.751e-03	9.638e-03	9.570e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	2.736e-03	2.779e-03	2.925e-03	3.087e-03
B (output stable)	2.542e-03	2.513e-03	2.558e-03	2.665e-03
C (output stable)	2.345e-03	2.342e-03	2.467e-03	2.626e-03
D (output stable)	2.149e-03	2.074e-03	2.084e-03	2.175e-03
A to Z	1.379e-02	1.352e-02	1.376e-02	1.422e-02
B to Z	1.329e-02	1.290e-02	1.299e-02	1.336e-02
C to Z	1.229e-02	1.189e-02	1.171e-02	1.201e-02
D to Z	1.180e-02	1.130e-02	1.097e-02	1.116e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

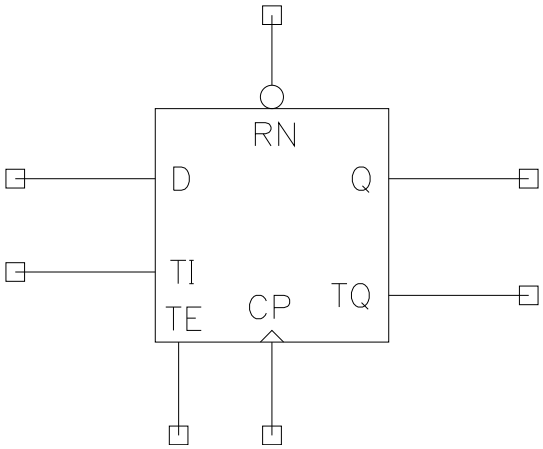
Pin Cycle (vdds)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.737e-07	4.055e-07	-7.590e-07	-2.294e-06
B (output stable)	3.069e-07	1.023e-05	2.457e-05	2.291e-05
C (output stable)	4.784e-07	4.315e-07	-8.740e-07	-3.538e-06
D (output stable)	5.168e-07	9.303e-06	2.502e-05	2.443e-05
A to Z	-1.208e-07	1.080e-07	-2.244e-07	-1.213e-06
B to Z	-2.900e-07	-3.450e-07	-3.760e-07	-4.570e-07
C to Z	-1.474e-07	2.311e-07	6.249e-07	-6.893e-07
D to Z	-6.700e-07	-2.140e-07	1.040e-07	-4.730e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	3.722e-07	3.410e-07	-7.277e-07	-2.287e-06
B (output stable)	4.196e-07	1.013e-05	2.448e-05	2.288e-05
C (output stable)	4.449e-07	4.099e-07	-7.321e-07	-3.458e-06
D (output stable)	5.281e-07	9.461e-06	2.536e-05	2.462e-05
A to Z	2.970e-07	2.957e-07	2.480e-08	-1.061e-06
B to Z	-3.510e-07	-1.550e-07	-2.140e-07	-2.630e-07
C to Z	1.730e-07	2.075e-07	-1.100e-07	-8.324e-07
D to Z	-3.900e-08	-2.480e-07	-4.790e-07	-4.410e-07

CNSDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.080	4.8960
X15_P4	1.200	4.080	4.8960
X15_P10	1.200	4.080	4.8960
X15_P16	1.200	4.080	4.8960

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0008	0.0009	0.0009	0.0010
D	0.0007	0.0007	0.0007	0.0008
RN	0.0009	0.0009	0.0010	0.0010

TE	0.0010	0.0011	0.0012	0.0012
TI	0.0003	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	X15_P4	X15_P0	X15_P4
CP to Q ↓	0.0529	0.0601	0.9334	0.9995
CP to Q ↑	0.0552	0.0623	1.1030	1.2276
CP to TQ ↓	0.0542	0.0618	4.2038	4.5060
CP to TQ ↑	0.0592	0.0669	9.8942	10.8661
RN to Q ↓	0.0586	0.0667	0.9340	0.9989
RN to TQ ↓	0.0599	0.0683	4.2058	4.5060
	X15_P10	X15_P16	X15_P10	X15_P16
CP to Q ↓	0.0718	0.0833	1.0949	1.1821
CP to Q ↑	0.0740	0.0854	1.4264	1.6201
CP to TQ ↓	0.0740	0.0860	4.9389	5.3269
CP to TQ ↑	0.0795	0.0919	12.5703	14.2625
RN to Q ↓	0.0798	0.0930	1.0939	1.1796
RN to TQ ↓	0.0820	0.0956	4.9391	5.3261

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.0544	0.0659	0.0833	0.0983
CP ↑	min_pulse_width to CP	0.0300	0.0311	0.0359	0.0406
D ↓	hold_rising to CP	-0.0020	-0.0069	-0.0143	-0.0189
D ↑	hold_rising to CP	-0.0046	-0.0043	-0.0095	-0.0144
D ↓	setup_rising to CP	0.0367	0.0415	0.0568	0.0663
D ↑	setup_rising to CP	0.0295	0.0344	0.0393	0.0466
RN ↓	min_pulse_width to RN	0.0496	0.0540	0.0637	0.0735
RN ↑	recovery_rising to CP	0.0134	0.0127	0.0149	0.0197
RN ↑	removal_rising to CP	-0.0031	-0.0028	-0.0053	-0.0074
TE ↓	hold_rising to CP	0.0002	-0.0047	-0.0121	-0.0170
TE ↑	hold_rising to CP	-0.0119	-0.0144	-0.0249	-0.0290
TE ↓	setup_rising to CP	0.0486	0.0534	0.0632	0.0758
TE ↑	setup_rising to CP	0.0694	0.0835	0.1083	0.1272
TI ↓	hold_rising to CP	-0.0326	-0.0436	-0.0596	-0.0743
TI ↑	hold_rising to CP	-0.0139	-0.0152	-0.0215	-0.0264
TI ↓	setup_rising to CP	0.0713	0.0831	0.1041	0.1235
TI ↑	setup_rising to CP	0.0401	0.0450	0.0512	0.0610

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X15_P0	3.591e-04	5.451e-09
X15_P4	1.123e-04	5.451e-09
X15_P10	3.721e-05	5.451e-09
X15_P16	2.129e-05	5.451e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

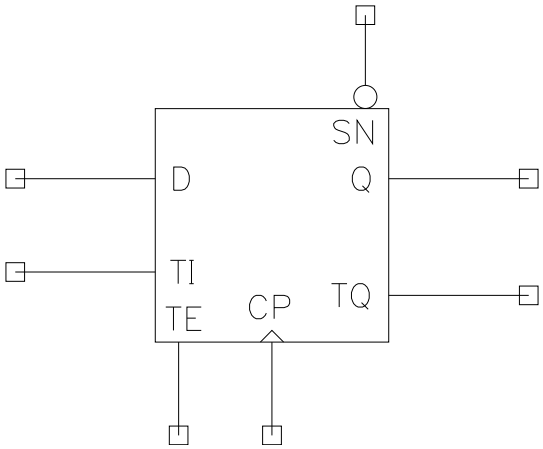
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	6.275e-03	6.219e-03	6.233e-03	6.283e-03
Clock 100Mhz Data 25Mhz	1.018e-02	1.011e-02	1.022e-02	1.040e-02
Clock 100Mhz Data 50Mhz	1.409e-02	1.400e-02	1.421e-02	1.452e-02
Clock = 0 Data 100Mhz	5.710e-03	5.733e-03	5.804e-03	5.895e-03
Clock = 1 Data 100Mhz	6.872e-05	6.614e-05	6.429e-05	6.329e-05

CNSDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.216	5.0592
X15_P4	1.200	4.216	5.0592
X15_P10	1.200	4.216	5.0592
X15_P16	1.200	4.216	5.0592

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0008	0.0009	0.0009	0.0010
D	0.0005	0.0005	0.0005	0.0005
SN	0.0016	0.0017	0.0017	0.0018

TE	0.0010	0.0011	0.0012	0.0012
TI	0.0004	0.0004	0.0005	0.0005

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	X15_P4	X15_P0	X15_P4
CP to Q ↓	0.0530	0.0602	0.9344	1.0003
CP to Q ↑	0.0555	0.0626	1.1054	1.2280
CP to TQ ↓	0.0544	0.0619	4.2143	4.5154
CP to TQ ↑	0.0596	0.0674	9.8916	10.8717
SN to Q ↑	0.0476	0.0539	1.1047	1.2260
SN to TQ ↑	0.0517	0.0586	9.9032	10.8653
	X15_P10	X15_P16	X15_P10	X15_P16
CP to Q ↓	0.0718	0.0833	1.0949	1.1817
CP to Q ↑	0.0743	0.0859	1.4265	1.6200
CP to TQ ↓	0.0741	0.0861	4.9485	5.3373
CP to TQ ↑	0.0799	0.0925	12.5744	14.2639
SN to Q ↑	0.0642	0.0743	1.4280	1.6190
SN to TQ ↑	0.0698	0.0809	12.5691	14.2654

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.0617	0.0732	0.0906	0.1074
CP ↑	min_pulse_width to CP	0.0300	0.0348	0.0358	0.0417
D ↓	hold_rising to CP	-0.0072	-0.0121	-0.0170	-0.0237
D ↑	hold_rising to CP	0.0006	-0.0046	-0.0064	-0.0117
D ↓	setup_rising to CP	0.0415	0.0464	0.0614	0.0736
D ↑	setup_rising to CP	0.0239	0.0295	0.0344	0.0393
SN ↓	min_pulse_width to SN	0.0376	0.0398	0.0474	0.0518
SN ↑	recovery_rising to CP	-0.0020	-0.0020	-0.0020	0.0005
SN ↑	removal_rising to CP	0.0236	0.0262	0.0311	0.0360
TE ↓	hold_rising to CP	-0.0047	-0.0069	-0.0173	-0.0219
TE ↑	hold_rising to CP	-0.0095	-0.0119	-0.0193	-0.0241
TE ↓	setup_rising to CP	0.0437	0.0485	0.0583	0.0711
TE ↑	setup_rising to CP	0.0761	0.0908	0.1125	0.1376
TI ↓	hold_rising to CP	-0.0428	-0.0526	-0.0686	-0.0845
TI ↑	hold_rising to CP	-0.0090	-0.0098	-0.0166	-0.0254
TI ↓	setup_rising to CP	0.0769	0.0921	0.1144	0.1334
TI ↑	setup_rising to CP	0.0347	0.0401	0.0463	0.0563

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X15_P0	3.670e-04	5.617e-09
X15_P4	1.171e-04	5.617e-09
X15_P10	3.901e-05	5.617e-09
X15_P16	2.223e-05	5.617e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

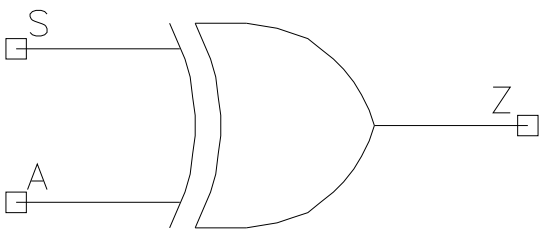
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	6.329e-03	6.275e-03	6.289e-03	6.340e-03
Clock 100Mhz Data 25Mhz	1.030e-02	1.024e-02	1.035e-02	1.053e-02
Clock 100Mhz Data 50Mhz	1.428e-02	1.420e-02	1.440e-02	1.471e-02
Clock = 0 Data 100Mhz	5.788e-03	5.801e-03	5.866e-03	5.953e-03
Clock = 1 Data 100Mhz	6.815e-05	6.599e-05	6.419e-05	6.327e-05

CNXOR2

Cell Description

2 input Exclusive OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X16_P0	1.200	1.360	1.6320
X16_P4	1.200	1.360	1.6320
X16_P10	1.200	1.360	1.6320
X16_P16	1.200	1.360	1.6320
X27_P0	1.200	2.040	2.4480
X27_P4	1.200	2.040	2.4480
X27_P10	1.200	2.040	2.4480
X27_P16	1.200	2.040	2.4480

Truth Table

A	S	Z
1	S	!S
0	S	S

Pin Capacitance

Pin	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0011	0.0012	0.0013	0.0013
S	0.0016	0.0017	0.0018	0.0020
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0017	0.0018	0.0019	0.0020
S	0.0023	0.0024	0.0025	0.0027

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0276	0.0311	0.7969	0.8536
A to Z ↑	0.0264	0.0295	1.1338	1.2601
S to Z ↓	0.0216	0.0242	0.7934	0.8495
S to Z ↑	0.0212	0.0238	1.1321	1.2589
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0369	0.0429	0.9372	1.0157

A to Z ↑	0.0345	0.0395	1.4679	1.6674
S to Z ↓	0.0284	0.0328	0.9333	1.0114
S to Z ↑	0.0278	0.0320	1.4671	1.6664
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0288	0.0326	0.5230	0.5619
A to Z ↑	0.0289	0.0325	0.6049	0.6716
S to Z ↓	0.0238	0.0269	0.5228	0.5614
S to Z ↑	0.0242	0.0271	0.6041	0.6718
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0385	0.0444	0.6184	0.6704
A to Z ↑	0.0381	0.0433	0.7804	0.8854
S to Z ↓	0.0316	0.0361	0.6180	0.6703
S to Z ↑	0.0317	0.0361	0.7808	0.8859

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X16_P0	2.972e-04	2.139e-09
X16_P4	9.013e-05	2.139e-09
X16_P10	2.773e-05	2.139e-09
X16_P16	1.436e-05	2.139e-09
X27_P0	4.431e-04	3.007e-09
X27_P4	1.283e-04	3.007e-09
X27_P10	3.846e-05	3.007e-09
X27_P16	1.992e-05	3.007e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	1.016e-02	9.615e-03	9.447e-03	9.620e-03
S to Z	8.831e-03	8.178e-03	7.884e-03	7.969e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	1.833e-02	1.734e-02	1.693e-02	1.697e-02
S to Z	1.430e-02	1.331e-02	1.277e-02	1.272e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

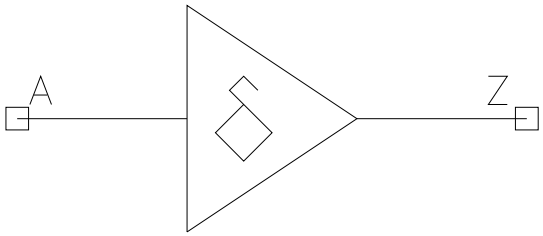
Pin Cycle (vdds)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	6.051e-07	5.061e-07	7.150e-09	9.835e-08
S to Z	1.004e-06	1.653e-06	6.087e-07	3.528e-07
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	-5.906e-07	-3.463e-07	4.498e-07	5.450e-09
S to Z	1.167e-07	6.042e-07	1.818e-07	-5.100e-09

DLYHF

Cell Description

Delay cell for Hold Time Fixing

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LR_-DLYHFM4X7_P0	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X7_P4	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X7_P10	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X7_P16	1.200	1.088	1.3056
C12T28SOI_LR_-DLYHFM4X15_P0	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM4X15_P4	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM4X15_P10	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM4X15_P16	1.200	1.224	1.4688
C12T28SOI_LR_-DLYHFM8X7_P0	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X7_P4	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X7_P10	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X7_P16	1.200	1.904	2.2848
C12T28SOI_LR_-DLYHFM8X15_P0	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X15_P4	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X15_P10	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X15_P16	1.200	2.040	2.4480
C12T28SOI_LR_-DLYHFM8X54_P0	1.200	4.216	5.0592

C12T28SOI_LR_-DLYHFM8X54_P4	1.200	4.216	5.0592
C12T28SOI_LR_-DLYHFM8X54_P10	1.200	4.216	5.0592
C12T28SOI_LR_-DLYHFM8X54_P16	1.200	4.216	5.0592

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C12T28SOI_LR_-DLYHFM4X7_P0	C12T28SOI_LR_-DLYHFM4X7_P4	C12T28SOI_LR_-DLYHFM4X7_P10	C12T28SOI_LR_-DLYHFM4X7_P16
A	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LR_-DLYHFM4X15_P0	C12T28SOI_LR_-DLYHFM4X15_P4	C12T28SOI_LR_-DLYHFM4X15_P10	C12T28SOI_LR_-DLYHFM4X15_P16
A	0.0009	0.0009	0.0009	0.0010
	C12T28SOI_LR_-DLYHFM8X7_P0	C12T28SOI_LR_-DLYHFM8X7_P4	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A	0.0008	0.0009	0.0009	0.0009
	C12T28SOI_LR_-DLYHFM8X15_P0	C12T28SOI_LR_-DLYHFM8X15_P4	C12T28SOI_LR_-DLYHFM8X15_P10	C12T28SOI_LR_-DLYHFM8X15_P16
A	0.0008	0.0008	0.0009	0.0009
	C12T28SOI_LR_-DLYHFM8X54_P0	C12T28SOI_LR_-DLYHFM8X54_P4	C12T28SOI_LR_-DLYHFM8X54_P10	C12T28SOI_LR_-DLYHFM8X54_P16
A	0.0008	0.0008	0.0009	0.0009

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LR_-DLYHFM4X7_P0	**C12T28SOI_LR_-DLYHFM4X7_P4**	**C12T28SOI_LR_-DLYHFM4X7_P0**	**C12T28SOI_LR_-DLYHFM4X7_P4**
A to Z ↓	0.0756	0.0867	1.8096	1.9464
A to Z ↑	0.0723	0.0829	2.5828	2.8728
	C12T28SOI_LR_-DLYHFM4X7_P10	**C12T28SOI_LR_-DLYHFM4X7_P16**	**C12T28SOI_LR_-DLYHFM4X7_P10**	**C12T28SOI_LR_-DLYHFM4X7_P16**
A to Z ↓	0.1046	0.1225	2.1488	2.3393
A to Z ↑	0.1003	0.1178	3.3448	3.8000
	C12T28SOI_LR_-DLYHFM4X15_P0	**C12T28SOI_LR_-DLYHFM4X15_P4**	**C12T28SOI_LR_-DLYHFM4X15_P0**	**C12T28SOI_LR_-DLYHFM4X15_P4**
A to Z ↓	0.0824	0.0949	0.8833	0.9536
A to Z ↑	0.0804	0.0924	1.1952	1.3312
	C12T28SOI_LR_-DLYHFM4X15_P10	**C12T28SOI_LR_-DLYHFM4X15_P16**	**C12T28SOI_LR_-DLYHFM4X15_P10**	**C12T28SOI_LR_-DLYHFM4X15_P16**
A to Z ↓	0.1149	0.1352	1.0577	1.1563
A to Z ↑	0.1120	0.1318	1.5529	1.7660
	C12T28SOI_LR_-DLYHFM8X7_P0	**C12T28SOI_LR_-DLYHFM8X7_P4**	**C12T28SOI_LR_-DLYHFM8X7_P0**	**C12T28SOI_LR_-DLYHFM8X7_P4**
A to Z ↓	0.1323	0.1524	1.8192	1.9616
A to Z ↑	0.1234	0.1420	2.3957	2.6639

	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A to Z ↓	0.1852	0.2181	2.1672	2.3595
A to Z ↑	0.1727	0.2034	3.1021	3.5234
	C12T28SOI_LR_-DLYHFM8X15_P0	**C12T28SOI_LR_-DLYHFM8X15_P4**	**C12T28SOI_LR_-DLYHFM8X15_P0**	**C12T28SOI_LR_-DLYHFM8X15_P4**
A to Z ↓	0.1381	0.1594	0.8838	0.9558
A to Z ↑	0.1313	0.1514	1.1961	1.3329
	C12T28SOI_LR_-DLYHFM8X15_P10	**C12T28SOI_LR_-DLYHFM8X15_P16**	**C12T28SOI_LR_-DLYHFM8X15_P10**	**C12T28SOI_LR_-DLYHFM8X15_P16**
A to Z ↓	0.1941	0.2293	1.0617	1.1617
A to Z ↑	0.1842	0.2172	1.5548	1.7686
	C12T28SOI_LR_-DLYHFM8X54_P0	**C12T28SOI_LR_-DLYHFM8X54_P4**	**C12T28SOI_LR_-DLYHFM8X54_P0**	**C12T28SOI_LR_-DLYHFM8X54_P4**
A to Z ↓	0.1824	0.2104	0.2353	0.2521
A to Z ↑	0.1661	0.1917	0.3443	0.3824
	C12T28SOI_LR_-DLYHFM8X54_P10	**C12T28SOI_LR_-DLYHFM8X54_P16**	**C12T28SOI_LR_-DLYHFM8X54_P10**	**C12T28SOI_LR_-DLYHFM8X54_P16**
A to Z ↓	0.2580	0.3045	0.2768	0.2995
A to Z ↑	0.2360	0.2795	0.4442	0.5035

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
C12T28SOI_LR_DLYHFM4X7_P0	4.994e-05	1.807e-09
C12T28SOI_LR_DLYHFM4X7_P4	1.696e-05	1.807e-09
C12T28SOI_LR_DLYHFM4X7_P10	6.588e-06	1.807e-09
C12T28SOI_LR_DLYHFM4X7_P16	4.386e-06	1.807e-09
C12T28SOI_LR_DLYHFM4X15_P0	9.497e-05	1.973e-09
C12T28SOI_LR_DLYHFM4X15_P4	3.026e-05	1.973e-09
C12T28SOI_LR_DLYHFM4X15_P10	1.070e-05	1.973e-09
C12T28SOI_LR_DLYHFM4X15_P16	6.586e-06	1.973e-09
C12T28SOI_LR_DLYHFM8X7_P0	5.456e-05	2.801e-09
C12T28SOI_LR_DLYHFM8X7_P4	1.942e-05	2.801e-09
C12T28SOI_LR_DLYHFM8X7_P10	8.224e-06	2.801e-09
C12T28SOI_LR_DLYHFM8X7_P16	5.864e-06	2.801e-09
C12T28SOI_LR_DLYHFM8X15_P0	1.006e-04	2.967e-09
C12T28SOI_LR_DLYHFM8X15_P4	3.312e-05	2.967e-09
C12T28SOI_LR_DLYHFM8X15_P10	1.243e-05	2.967e-09
C12T28SOI_LR_DLYHFM8X15_P16	8.088e-06	2.967e-09
C12T28SOI_LR_DLYHFM8X54_P0	3.324e-04	5.617e-09
C12T28SOI_LR_DLYHFM8X54_P4	1.084e-04	5.617e-09
C12T28SOI_LR_DLYHFM8X54_P10	4.123e-05	5.617e-09
C12T28SOI_LR_DLYHFM8X54_P16	2.755e-05	5.617e-09

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

Pin Cycle (vdd)	C12T28SOI_LR_-DLYHFM4X7_P0	C12T28SOI_LR_-DLYHFM4X7_P4	C12T28SOI_LR_-DLYHFM4X7_P10	C12T28SOI_LR_-DLYHFM4X7_P16
A to Z	6.128e-03	6.113e-03	6.258e-03	6.481e-03
	C12T28SOI_LR_-DLYHFM4X15_P0	C12T28SOI_LR_-DLYHFM4X15_P4	C12T28SOI_LR_-DLYHFM4X15_P10	C12T28SOI_LR_-DLYHFM4X15_P16
A to Z	9.958e-03	9.624e-03	9.543e-03	9.684e-03

	C12T28SOI_LR_-DLYHFM8X7_P0	C12T28SOI_LR_-DLYHFM8X7_P4	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A to Z	9.519e-03	9.564e-03	9.859e-03	1.021e-02
	C12T28SOI_LR_-DLYHFM8X15_P0	C12T28SOI_LR_-DLYHFM8X15_P4	C12T28SOI_LR_-DLYHFM8X15_P10	C12T28SOI_LR_-DLYHFM8X15_P16
A to Z	1.334e-02	1.306e-02	1.311e-02	1.339e-02
	C12T28SOI_LR_-DLYHFM8X54_P0	C12T28SOI_LR_-DLYHFM8X54_P4	C12T28SOI_LR_-DLYHFM8X54_P10	C12T28SOI_LR_-DLYHFM8X54_P16
A to Z	4.011e-02	3.997e-02	4.138e-02	4.294e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V, Best process

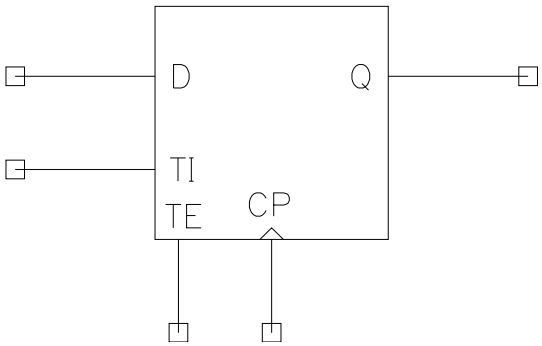
Pin Cycle (vdds)	C12T28SOI_LR_-DLYHFM4X7_P0	C12T28SOI_LR_-DLYHFM4X7_P4	C12T28SOI_LR_-DLYHFM4X7_P10	C12T28SOI_LR_-DLYHFM4X7_P16
A to Z	1.284e-07	4.660e-08	-1.050e-06	-2.071e-06
	C12T28SOI_LR_-DLYHFM4X15_P0	C12T28SOI_LR_-DLYHFM4X15_P4	C12T28SOI_LR_-DLYHFM4X15_P10	C12T28SOI_LR_-DLYHFM4X15_P16
A to Z	9.640e-08	8.600e-09	-9.771e-07	-2.096e-06
	C12T28SOI_LR_-DLYHFM8X7_P0	C12T28SOI_LR_-DLYHFM8X7_P4	C12T28SOI_LR_-DLYHFM8X7_P10	C12T28SOI_LR_-DLYHFM8X7_P16
A to Z	3.562e-07	2.107e-07	-1.673e-06	-3.161e-06
	C12T28SOI_LR_-DLYHFM8X15_P0	C12T28SOI_LR_-DLYHFM8X15_P4	C12T28SOI_LR_-DLYHFM8X15_P10	C12T28SOI_LR_-DLYHFM8X15_P16
A to Z	4.997e-07	2.685e-07	-1.485e-06	-3.195e-06
	C12T28SOI_LR_-DLYHFM8X54_P0	C12T28SOI_LR_-DLYHFM8X54_P4	C12T28SOI_LR_-DLYHFM8X54_P10	C12T28SOI_LR_-DLYHFM8X54_P16
A to Z	1.068e-06	1.072e-06	-3.774e-06	-1.235e-05

SDFSYNCPQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.400	8.1600
X8_P4	2.400	3.400	8.1600
X8_P10	2.400	3.400	8.1600
X8_P16	2.400	3.400	8.1600

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0009	0.0010	0.0011	0.0011
D	0.0007	0.0007	0.0008	0.0008
TE	0.0011	0.0011	0.0012	0.0012
TI	0.0003	0.0003	0.0003	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X8_P4	X8_P0	X8_P4
CP to Q ↓	0.0887	0.1016	1.4738	1.5777
CP to Q ↑	0.1026	0.1170	2.2163	2.4653

	X8_P10	X8_P16	X8_P10	X8_P16
CP to Q ↓	0.1230	0.1445	1.7309	1.8704
CP to Q ↑	0.1408	0.1650	2.8722	3.2568

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1301	0.1566	0.1914	0.2287
CP ↑	min_pulse_width to CP	0.0531	0.0579	0.0686	0.0820
D ↓	hold_rising to CP	-0.0343	-0.0441	-0.0582	-0.0729
D ↑	hold_rising to CP	-0.0089	-0.0144	-0.0193	-0.0264
D ↓	setup_rising to CP	0.0759	0.0909	0.1104	0.1300
D ↑	setup_rising to CP	0.0367	0.0389	0.0490	0.0539
TE ↓	hold_rising to CP	-0.0290	-0.0361	-0.0481	-0.0601
TE ↑	hold_rising to CP	-0.0332	-0.0437	-0.0534	-0.0632
TE ↓	setup_rising to CP	0.0714	0.0858	0.1054	0.1249
TE ↑	setup_rising to CP	0.1452	0.1714	0.2157	0.2545
TI ↓	hold_rising to CP	-0.0960	-0.1169	-0.1524	-0.1832
TI ↑	hold_rising to CP	-0.0356	-0.0444	-0.0556	-0.0667
TI ↓	setup_rising to CP	0.1404	0.1701	0.2107	0.2512
TI ↑	setup_rising to CP	0.0658	0.0702	0.0854	0.0966

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	4.531e-04	6.096e-09
X8_P4	1.465e-04	6.096e-09
X8_P10	5.122e-05	6.096e-09
X8_P16	3.099e-05	6.096e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

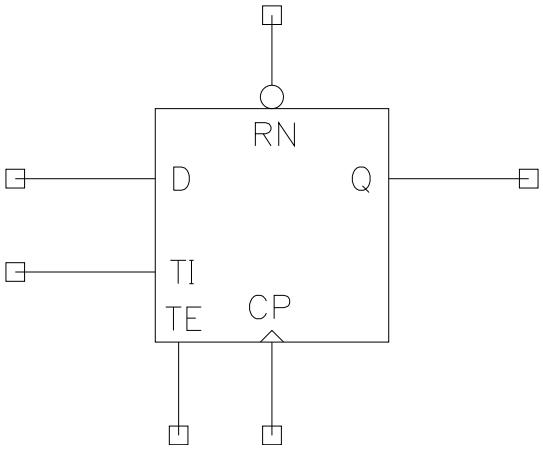
Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	1.221e-02	1.237e-02	1.266e-02	1.299e-02
Clock 100Mhz Data 25Mhz	1.953e-02	1.953e-02	1.994e-02	2.043e-02
Clock 100Mhz Data 50Mhz	2.686e-02	2.669e-02	2.722e-02	2.788e-02
Clock = 0 Data 100Mhz	1.407e-02	1.379e-02	1.365e-02	1.362e-02
Clock = 1 Data 100Mhz	5.694e-05	5.473e-05	5.334e-05	5.310e-05

SDFSYNCPRQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0009	0.0010	0.0010	0.0011
D	0.0007	0.0008	0.0008	0.0008
RN	0.0020	0.0021	0.0023	0.0024
TE	0.0011	0.0011	0.0012	0.0012
TI	0.0003	0.0003	0.0003	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
CP to Q ↓	0.0970	0.1110	1.4789	1.5842
CP to Q ↑	0.1037	0.1182	2.2044	2.4544
RN to Q ↓	0.1100	0.1255	1.4822	1.5864
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
CP to Q ↓	0.1342	0.1576	1.7398	1.8841
CP to Q ↑	0.1423	0.1670	2.8600	3.2483
RN to Q ↓	0.1517	0.1787	1.7428	1.8864

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1301	0.1523	0.1890	0.2282
CP ↑	min_pulse_width to CP	0.0542	0.0590	0.0734	0.0831
D ↓	hold_rising to CP	-0.0313	-0.0410	-0.0561	-0.0708
D ↑	hold_rising to CP	-0.0119	-0.0144	-0.0193	-0.0294
D ↓	setup_rising to CP	0.0738	0.0857	0.1055	0.1251
D ↑	setup_rising to CP	0.0392	0.0419	0.0490	0.0539
RN ↓	min_pulse_width to RN	0.0903	0.1023	0.1218	0.1414
RN ↑	recovery_rising to CP	0.0078	0.0100	0.0100	0.0129
RN ↑	removal_rising to CP	-0.0027	-0.0052	-0.0052	-0.0078
TE ↓	hold_rising to CP	-0.0297	-0.0362	-0.0481	-0.0601
TE ↑	hold_rising to CP	-0.0388	-0.0437	-0.0534	-0.0654
TE ↓	setup_rising to CP	0.0687	0.0837	0.1001	0.1200
TE ↑	setup_rising to CP	0.1396	0.1665	0.2109	0.2499
TI ↓	hold_rising to CP	-0.0911	-0.1174	-0.1475	-0.1822
TI ↑	hold_rising to CP	-0.0395	-0.0459	-0.0569	-0.0667
TI ↓	setup_rising to CP	0.1370	0.1668	0.2058	0.2422
TI ↑	setup_rising to CP	0.0653	0.0756	0.0854	0.0964

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	4.543e-04	6.909e-09
X8_P4	1.469e-04	6.909e-09
X8_P10	5.364e-05	6.909e-09
X8_P16	3.440e-05	6.909e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	1.268e-02	1.286e-02	1.317e-02	1.353e-02

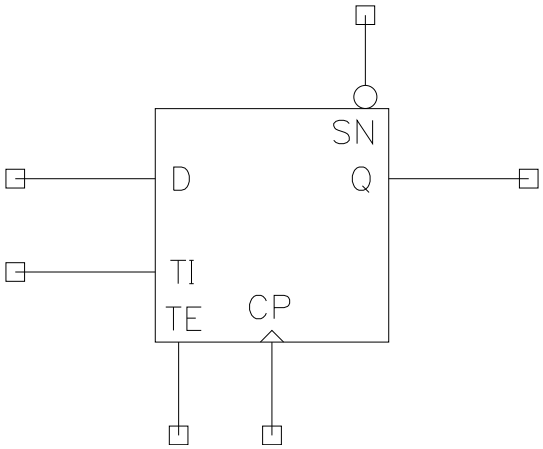
Clock 100Mhz Data 25Mhz	2.004e-02	2.007e-02	2.052e-02	2.110e-02
Clock 100Mhz Data 50Mhz	2.740e-02	2.729e-02	2.787e-02	2.867e-02
Clock = 0 Data 100Mhz	1.362e-02	1.341e-02	1.333e-02	1.335e-02
Clock = 1 Data 100Mhz	5.729e-05	5.501e-05	5.671e-05	6.758e-05

SDFSYNCPSQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0009	0.0010	0.0010	0.0011
D	0.0005	0.0005	0.0005	0.0005
SN	0.0019	0.0020	0.0021	0.0023
TE	0.0011	0.0011	0.0012	0.0012
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
CP to Q ↓	0.0749	0.0854	1.7637	1.9248
CP to Q ↑	0.0896	0.1019	2.3439	2.6157
SN to Q ↑	0.0914	0.1042	2.2747	2.5369
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
CP to Q ↓	0.1020	0.1186	2.1730	2.4083
CP to Q ↑	0.1225	0.1434	3.0558	3.4822
SN to Q ↑	0.1255	0.1474	2.9642	3.3705

Timing Constraints (ns) at 125C, 1.10V, Best process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1210	0.1450	0.1818	0.2179
CP ↑	min_pulse_width to CP	0.0542	0.0627	0.0734	0.0879
D ↓	hold_rising to CP	-0.0271	-0.0313	-0.0433	-0.0586
D ↑	hold_rising to CP	-0.0089	-0.0144	-0.0190	-0.0264
D ↓	setup_rising to CP	0.0658	0.0812	0.0976	0.1175
D ↑	setup_rising to CP	0.0392	0.0415	0.0494	0.0568
SN ↓	min_pulse_width to SN	0.1060	0.1206	0.1401	0.1646
SN ↑	recovery_rising to CP	-0.0091	-0.0066	-0.0038	-0.0066
SN ↑	removal_rising to CP	0.0379	0.0403	0.0449	0.0528
TE ↓	hold_rising to CP	-0.0193	-0.0294	-0.0414	-0.0512
TE ↑	hold_rising to CP	-0.0388	-0.0437	-0.0557	-0.0685
TE ↓	setup_rising to CP	0.0640	0.0760	0.0956	0.1124
TE ↑	setup_rising to CP	0.1324	0.1592	0.2004	0.2424
TI ↓	hold_rising to CP	-0.0863	-0.1071	-0.1377	-0.1684
TI ↑	hold_rising to CP	-0.0410	-0.0472	-0.0569	-0.0721
TI ↓	setup_rising to CP	0.1321	0.1563	0.1968	0.2364
TI ↑	setup_rising to CP	0.0707	0.0756	0.0867	0.1018

Average Leakage Power (mW) at 125C, 1.10V, Best process

	vdd	vdds
X8_P0	4.569e-04	7.082e-09
X8_P4	1.557e-04	7.081e-09
X8_P10	5.708e-05	7.082e-09
X8_P16	3.578e-05	7.082e-09

Internal Energy (uW/MHz) at 125C, 1.10V, Best process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	1.250e-02	1.268e-02	1.299e-02	1.335e-02

Clock 100Mhz Data 25Mhz	1.977e-02	1.972e-02	2.007e-02	2.055e-02
Clock 100Mhz Data 50Mhz	2.704e-02	2.676e-02	2.714e-02	2.776e-02
Clock = 0 Data 100Mhz	1.355e-02	1.339e-02	1.335e-02	1.341e-02
Clock = 1 Data 100Mhz	6.959e-05	6.742e-05	6.563e-05	6.453e-05

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