



cmos028fdsoi Technology

PDC vs MC Noise report for LVT models

DK1.2_RF_mmW

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Technology R&D Crolles Site – TDP/TDS/SPICE Modeling

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General information on PDC vs MC Noise report for LVT models

- Maximum supply voltage is - V.
- Validity domain is defined as follows:
 - ✓ Drawn gate length varies from 30nm to 10um.
 - ✓ Drawn transistor width varies from 80nm to 10um.
 - ✓ Device temperature varies from -40 °C to 125 °C.

Output parameters definitions

- Model(s): lvtmfet_acc, lvtpfet_acc

lvtnfet_acc

Electrical characteristics per geometry

lvtnfet_acc @ w=20e-6, l=2.0e-6, pre_layout_local=1, nf=4, sa=8.500e-08, sb=8.500e-08, sd=1.140e-07, pcpastrx_top=1.050e-07, pcpastrx_bot=1.050e-07, devtype=PCELLwoWPE, as=4.25e-13, ad=4.25e-13, ps=1.017e-05, pd=1.017e-05, vbs=0, vdd=1, temp=25

	TT_Noisedev=4	TT_Noisedev=0	TT_Noisedev=2	PRO_MC_PARAM_ TT_1_MC_AVG-3S	PRO_MC_PARAM_ TT_1_MC_AVG	PRO_MC_PARAM_ TT_1_MC_AVG+3S
logSi2@1Hz [log10(A ² /Hz)]	-18.11	-17.94	-17.78	-18.11	-17.94	-17.78
logSi2ovId2@1Hz [log10(1/Hz)]	-9.51	-9.34	-9.18	-9.51	-9.34	-9.18
logSv2@1Hz [log10(V ² /Hz)]	-11.65	-11.49	-11.33	-11.66	-11.49	-11.33

lvtpfet_acc

Electrical characteristics per geometry

lvtpfet_acc @ w=0.30e-6, l=0.030e-6, pre_layout_local=1, nf=1, sa=8.500e-08, sb=8.500e-08, sd=1.140e-07, pcpastrx_top=5.700e-08, pcpastrx_bot=8.000e-08, devtype=PCELLwoWPE, as=2.55e-14, ad=2.55e-14, ps=7.7e-07, pd=7.7e-07, vbs=1, vdd=1, temp=25

	TT_Noisedev=4	TT_Noisedev=0	TT_Noisedev=2	PRO_MC_PARAM_ TT_1_MC_AVG-3S	PRO_MC_PARAM_ TT_1_MC_AVG	PRO_MC_PARAM_ TT_1_MC_AVG+3S
logSi2@1Hz [log10(A ² /Hz)]	-16.67	-15.66	-14.65	-16.68	-15.66	-14.65
logSi2ovId2@1Hz [log10(1/Hz)]	-7.28	-6.26	-5.25	-7.28	-6.26	-5.25
logSv2@1Hz [log10(V ² /Hz)]	-8.89	-7.88	-6.87	-8.89	-7.88	-6.87

lvtpfet_acc @ w=20e-6, l=2.0e-6, pre_layout_local=1, nf=4, sa=8.500e-08, sb=8.500e-08, sd=1.140e-07, pcpastrx_top=1.050e-07, pcpastrx_bot=1.050e-07, devtype=PCELLwoWPE, as=4.25e-13, ad=4.25e-13, ps=1.017e-05, pd=1.017e-05, vbs=1, vdd=1, temp=25

	TT_Noisedev=4	TT_Noisedev=0	TT_Noisedev=2	PRO_MC_PARAM_ TT_1_MC_AVG-3S	PRO_MC_PARAM_ TT_1_MC_AVG	PRO_MC_PARAM_ TT_1_MC_AVG+3S
logSi2@1Hz [log10(A ² /Hz)]	-19.24	-19	-18.76	-19.24	-19	-18.76
logSi2ovId2@1Hz [log10(1/Hz)]	-9.84	-9.6	-9.36	-9.84	-9.6	-9.36
logSv2@1Hz [log10(V ² /Hz)]	-11.88	-11.65	-11.41	-11.89	-11.65	-11.41

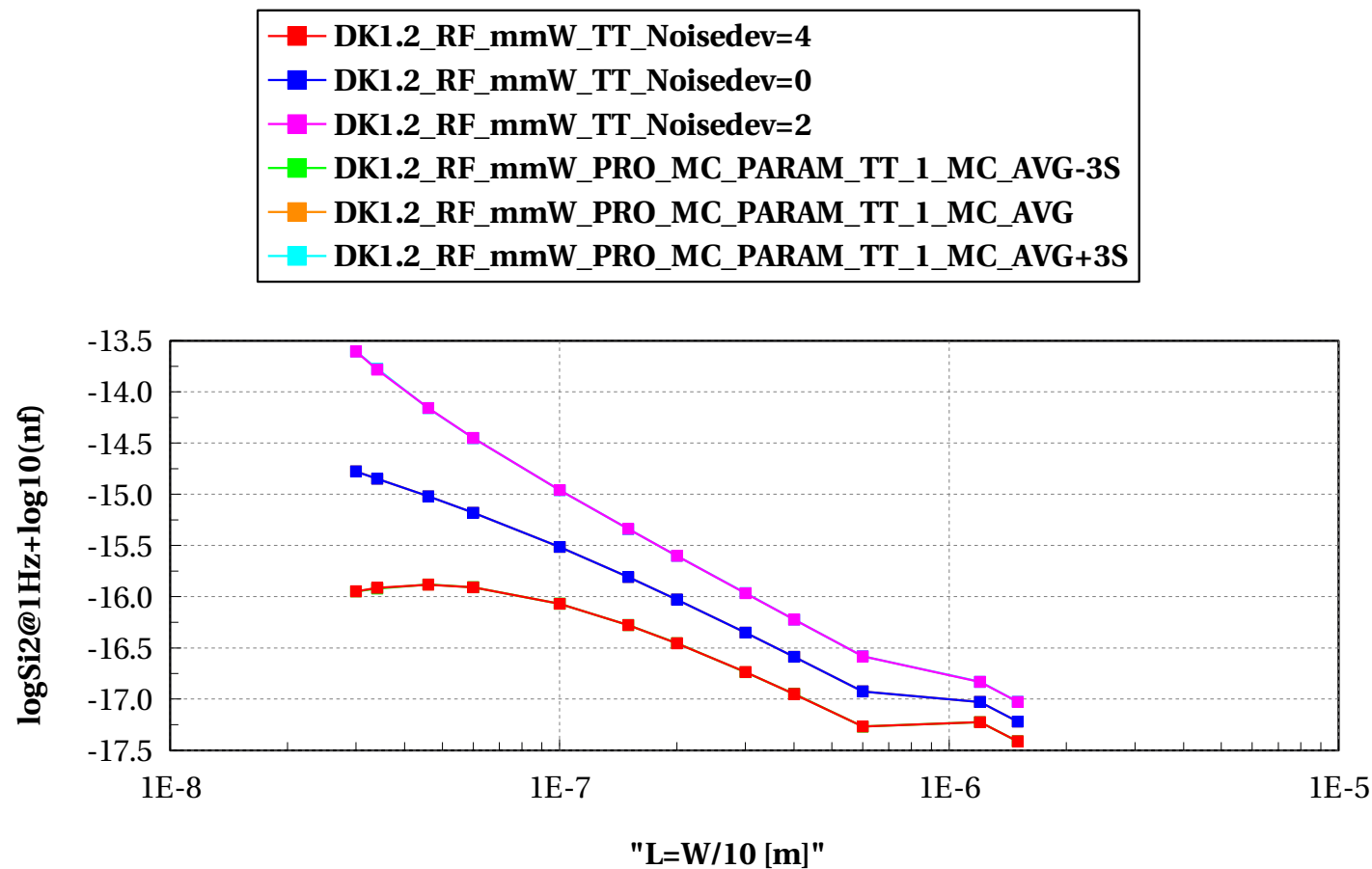
lvtnfet_acc

Electrical characteristics scaling

Scaling versus Length @ $W/L=10$ and $W/NF<5e-6$

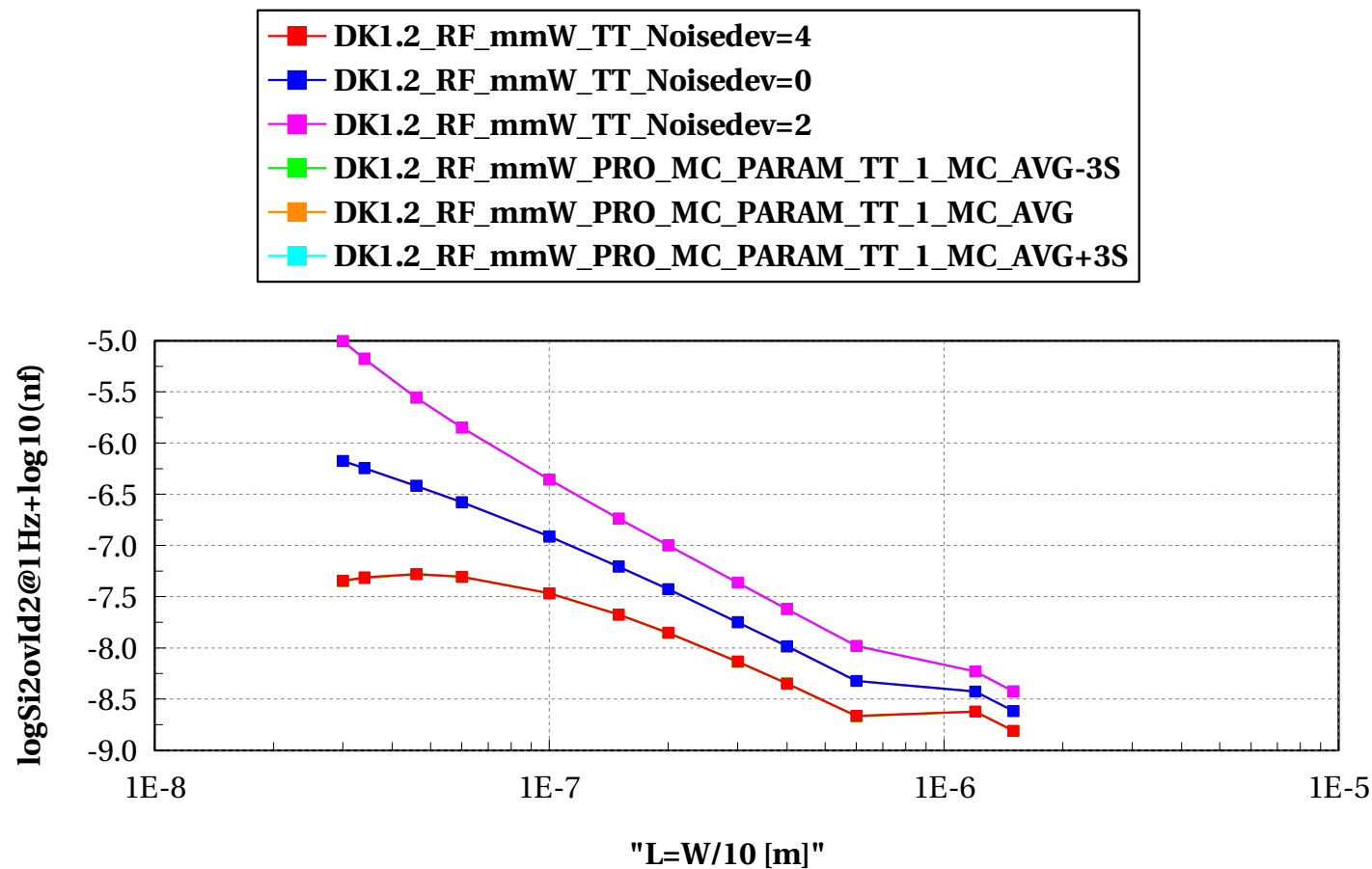
lvtnfet_acc, logSi2@1Hz+log10(nf) vs "L=W/10 [m]"

W/L==10 and Temp==25



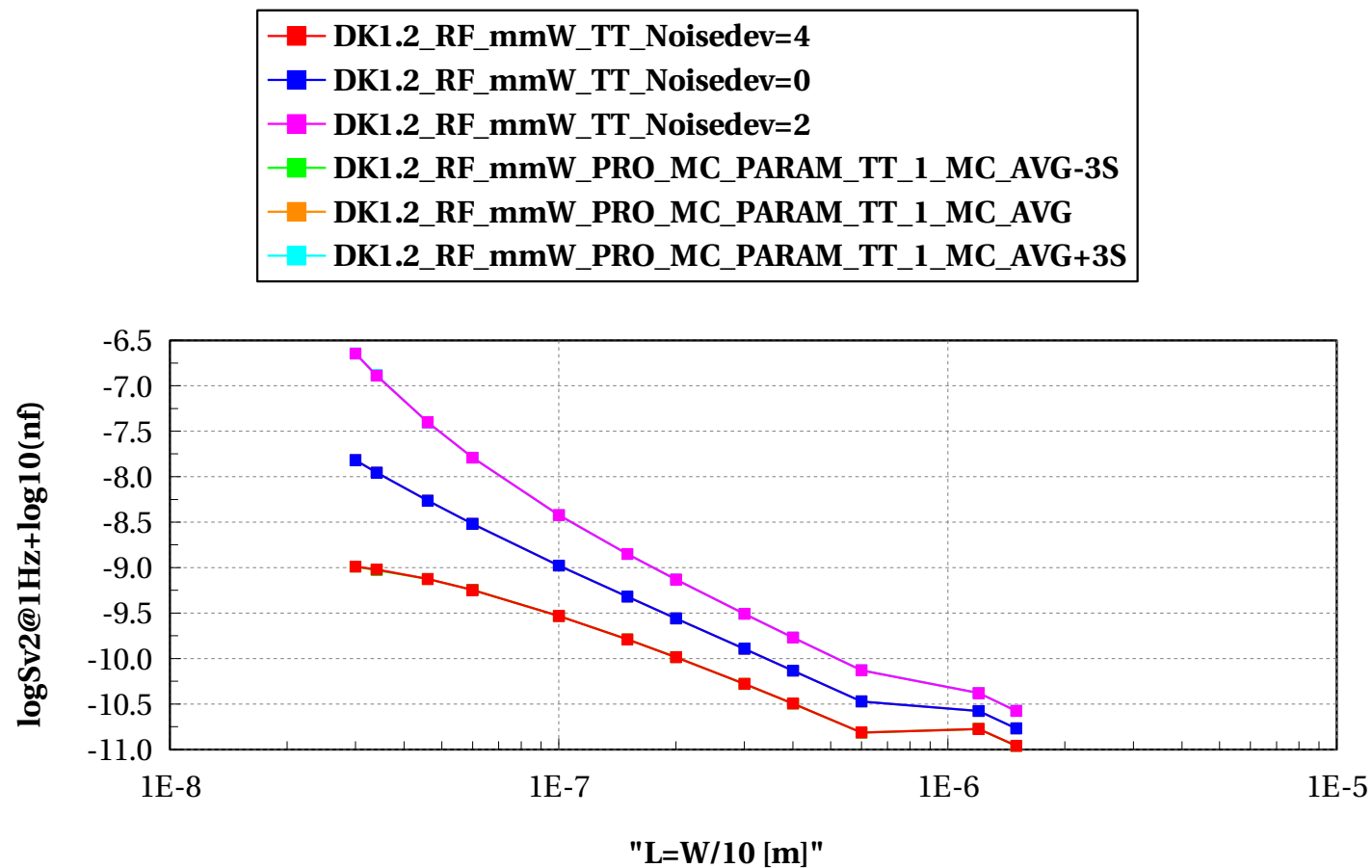
lvtnfet_acc, logSi2ovld2@1Hz+log10(nf) vs "L=W/10 [m]"

W/L==10 and Temp==25



lvtnfet_acc, logSv2@1Hz+log10(nf) vs "L=W/10 [m]"

W/L==10 and Temp==25



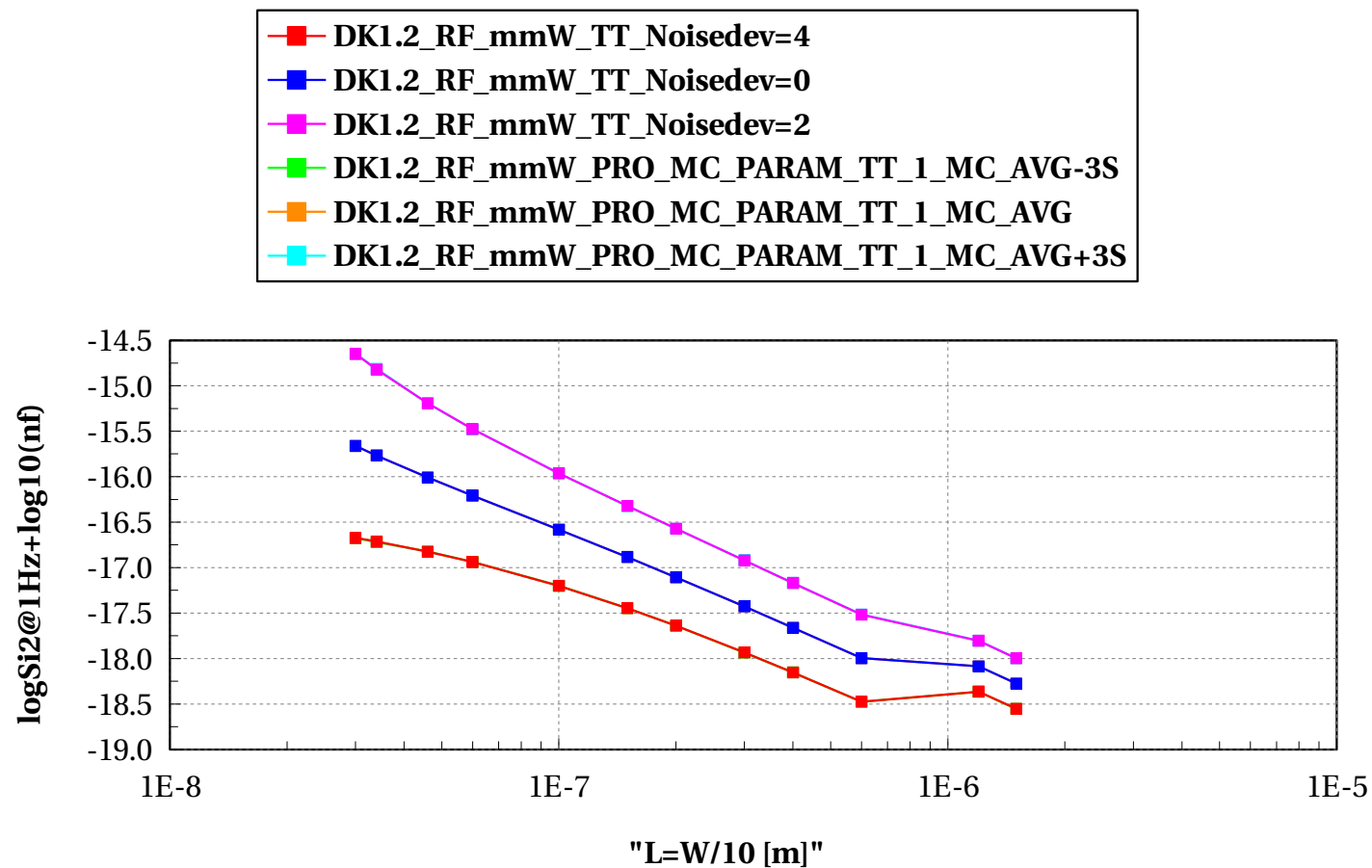
lvtpfet_acc

Electrical characteristics scaling

Scaling versus Length @ $W/L=10$ and $W/NF<5e-6$

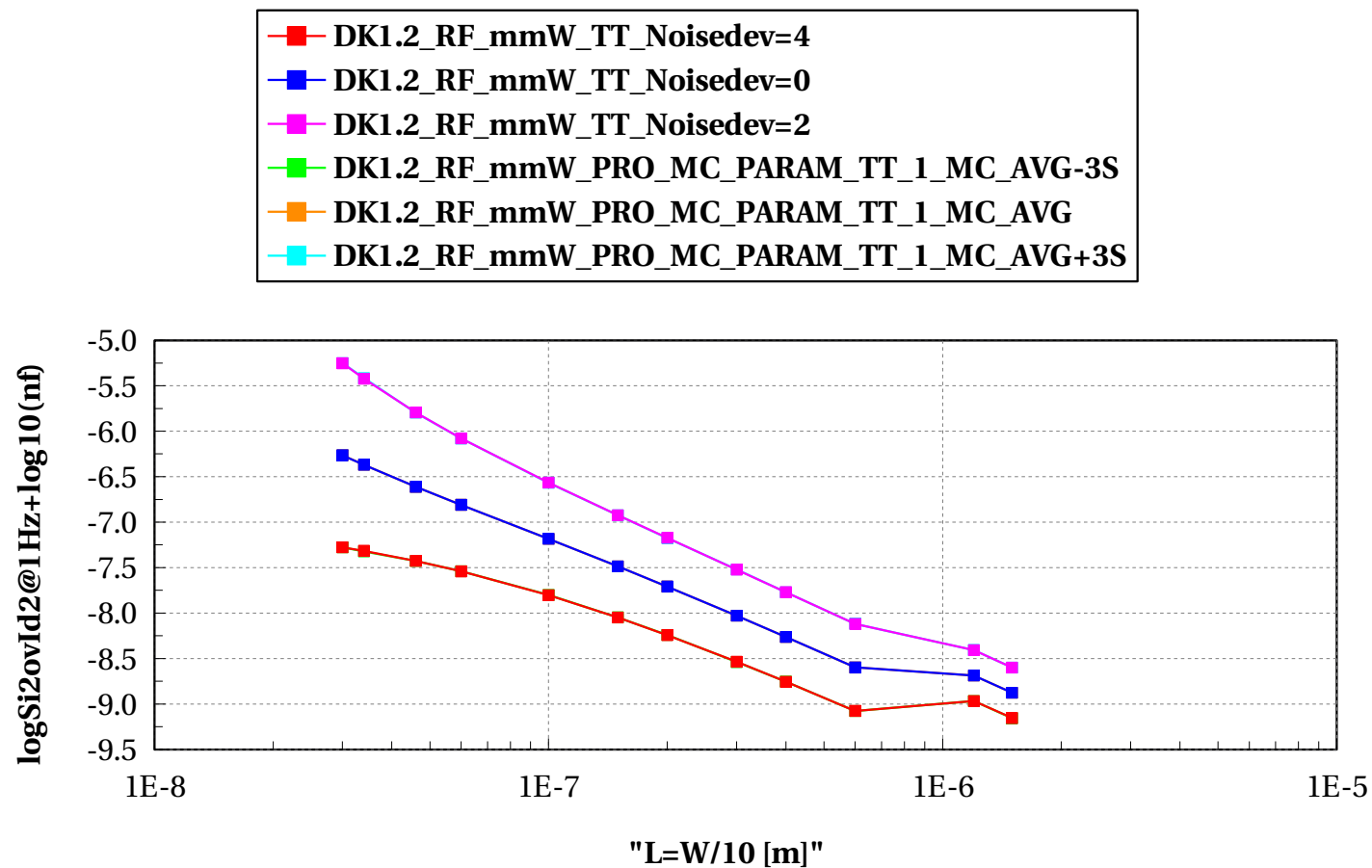
lvtpfet_acc, logSi2@1Hz+log10(nf) vs "L=W/10 [m]"

W/L==10 and Temp==25



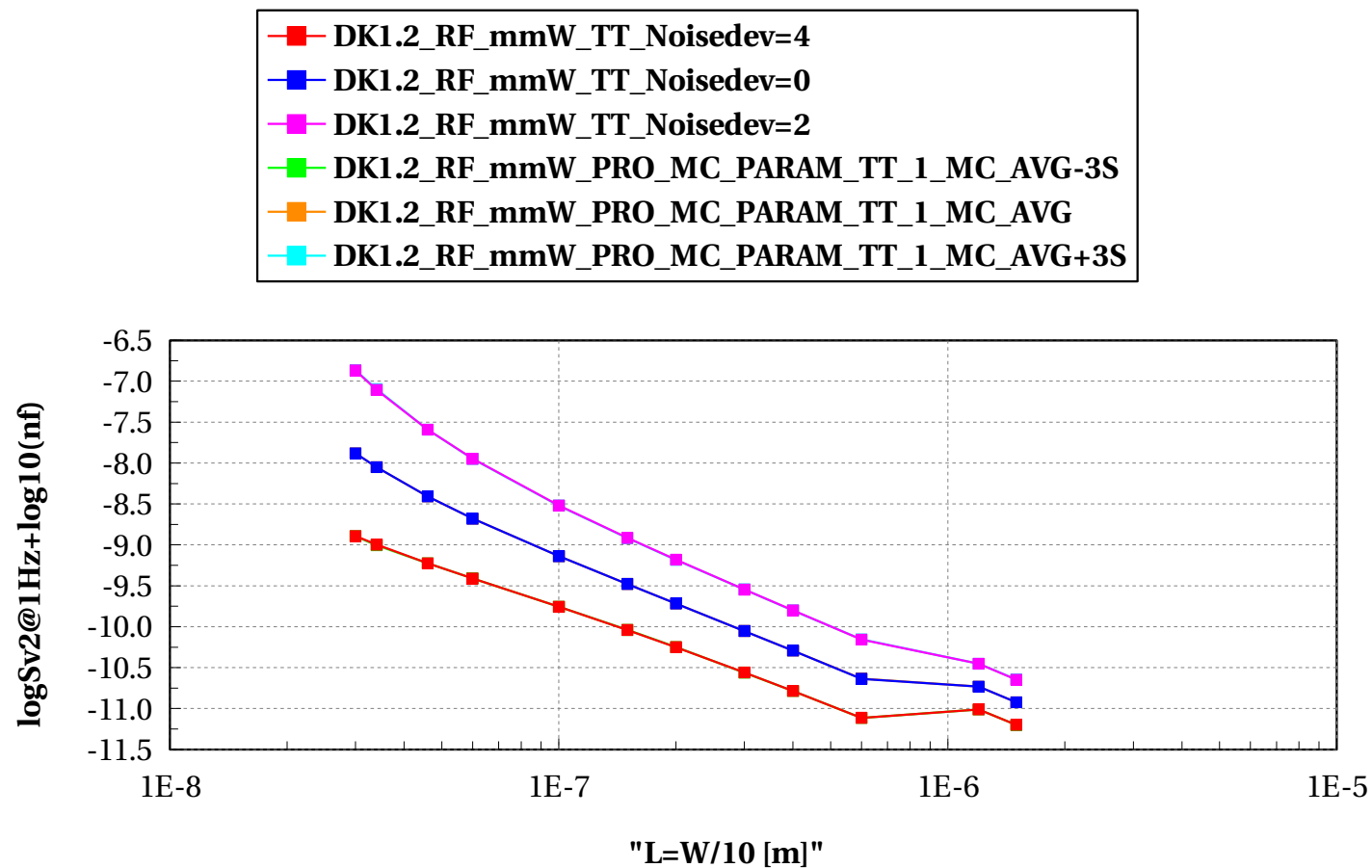
lvtpfet_acc, logSi2ovld2@1Hz+log10(nf) vs "L=W/10 [m]"

W/L==10 and Temp==25



lvtpfet_acc, logSv2@1Hz+log10(nf) vs "L=W/10 [m]"

W/L==10 and Temp==25



Annex

Conditions of simulations

The simulations were done with SBenchLSF Alpha using Eldo simulator 2018.3.

- Model lvtinfet_acc (DK1.2_RF_mmW)

- ✓ Input Parameters

- ✗ ams_release = 2018.3
- ✗ mc_runs = 500
- ✗ iana = 5e-6 A
- ✗ temp = 25 °C
- ✗ mc_sens = 0
- ✗ f_ext = 100k Hz
- ✗ sbenchlsf_release = Alpha
- ✗ vbs = 0 V
- ✗ model_version = 1.3.e
- ✗ vds_ana = Vdd/4 V
- ✗ mc_nsigma = 3
- ✗ vdd = 1 V

- ✓ Sweep Parameters

- ✓ Extra parameters

- ✗ lvt_dev = 0
- Model lvtpfet_acc (DK1.2_RF_mmW)
 - ✓ Input Parameters
 - ✗ ams_release = 2018.3
 - ✗ mc_runs = 500
 - ✗ iana = 2e-6 A
 - ✗ temp = 25 °C
 - ✗ mc_sens = 0
 - ✗ f_ext = 100k Hz
 - ✗ sbenchlsf_release = Alpha
 - ✗ vbs = 1 V
 - ✗ model_version = 1.3.e
 - ✗ vds_ana = Vdd/4 V
 - ✗ mc_nsigma = 3
 - ✗ vdd = 1 V
 - ✓ Sweep Parameters
 - ✓ Extra parameters
 - ✗ lvt_dev = 0