C28SOI_IO_EXT_ALLF_DIGNEG_LR_EG User's manual

Negative 1.8 V Dedicated supply IO library and ESD core clamp designed in 28 nm FDSOI technology

Overview

The C28SOI_IO_EXT_ALLF_DIGNEG_LR_EG library is designed in 28 nm FDSOI technology. It contains 4 cells for dedicated core supply and ESD core clamp for negative 1.8 V .

Features

- Contains negative 1.8V power cells
- Uses the standard process option and 28 Å gate oxide.
- Supports Compatible Standard Frame (CSF##) only
- Supports single row[1] configuration for IO ring
- FC (Flip-chip) and CL (Cluster) frames provided.

Product name contains ALLF due to legacy reasons although only CSF is supported

Information Snapshot

Process Options

- GO1: SVT
- GO2: 28 Å

[1]Single row configuration is also called linear configuration.

Packaging

- Flip-chip

Table 1 : Operating values

Symbol	Parameter	Min	Typ	Max	Unit
VDDCORENEG1V8	Negative power supply	-1.95	-1.8	0 (1)	V
vdd	Supply voltage for 1.0 V node	0.6	1.0	1.1	V
vdde	Supply voltage for 1.8 V IO ring	1.65	1.8	1.95	V
$T_{junction}$	Operating junction temperature	- 40	25	125	°C

Notes:

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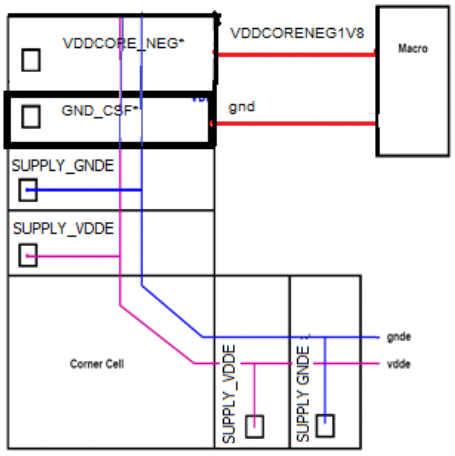
For more details about electrical specifications, please refer to *Section 3: Electrical Specifications*.

Figure 1 : Example of dedicated supplies usage



1. Quick References

	*The document uses the following convention to indicate logic levels:* *L indicates logic low.* *H indicates logic high.* *X indicates don't care state.* *Z indicates high impedance state.* *'-' (Hyphen) indicates 'No activity'.*

	** suffixed in library name indicates multiple metallization options.* *** suffixed in cell name indicates multiple packages / configurations.*

1.1 Metal Stacking Convention

The metallization option supported by this library can be referred from its product package. The following is the convention that can be used to decode the segment in the library name:

- 7 metal option (5U1X2T8XLB) known as 5002 refers as follows:
  - 5U1X refers to the first 5 levels with 1X pitch (thin) metal.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 8 metal option (6U1X2T8XLB) known as 6002 refers as follows:
  - 6U1X refers to the first 6 levels with 1X pitch (thin) metal in ultra-low-K.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 10 metal option (6U1X2U2X2T8XLB) known as 6202 refers as follows:
  - 6U1X refers to the first 6 levels with 1x pitch (thin) metal in ultra-low-K.
  - 2U2X refers to the next 2 levels with 2x pitch (thin) metal in ultra-low-K.
  - 2T8X refers to 2 levels with 8x (thick) metal in oxide.
  - LB is the Alucap.

1.2 Reference Documentation

For details on the following topics:

- Power Sequencing Recommendation in IOs
- Specifications and Analysis of Overshoots and Undershoots
- SSN Application Notes
- ESD qualification
- Latch-up qualification
- Maturity information
- RDL recommended rules
  - ST users, refer to the IO Reference catalog

    (http://ccds.st.com/cps/sections/library/io/io_reference_catalog/downloadFile/file/IO_Helpdesk_Solutions.pdf).
  - Non-ST users, contact Customer Support personnel

1.3 Reference Library

The C28SOI_IO_EXT_ALLF_DIGNEG_LR_EG library refers to some cells from 28 nm FDSOI libraries listed below. For a correct usage, these libraries are mandatory:

- C28SOI_IO_ALLF_FRAMEKIT_EG
- C28SOI_IO_ALLF_IOSUPPLYKIT_EG

1.4 Acronyms and Abbreviations Used

Table 2 : Acronyms and Abbreviation

Acronym/Abbreviation	Description
B2B	Back-to-Back
CDM	Charge Device Model
DC	Direct Current
DRM	Design Rule Manual
ESD	Electrostatic Discharge
HBM	Human Body Model
FC	Flip-chip
CL	Cluster
MM	Machine Model
RMS	Root Mean Square
SVT	Standard V_T
2ROWS	Two rows

2. Functional Specifications

The C28SOI_IO_EXT_ALLF_CORESUPPLY_EG library includes 65 cells.

Table 3 : Cell List

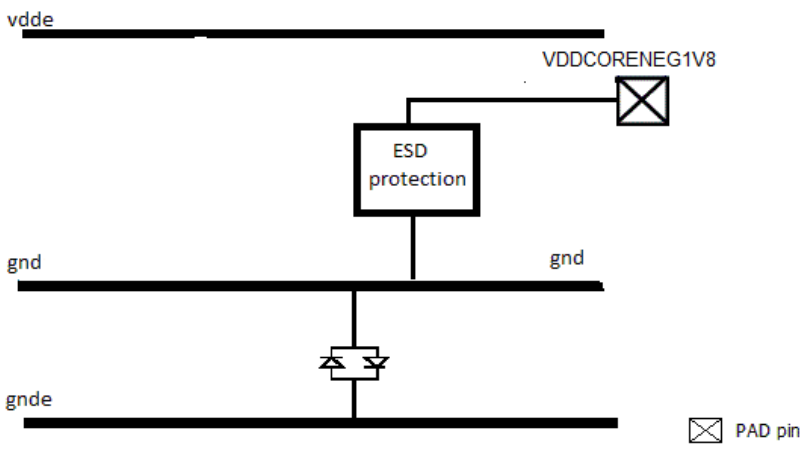
Cell Name	Width x Height (µm)	Cell Description
VDDCORE_NEG1V8_EXT_CSF_CL_LIN	40 x 106.3	Dedicated negative 1.0V power supply referring to gnd ground node
VDDCORE_NEG1V8_EXT_CSF_FC_LIN	40 x 90.8	
ESDCLAMP_NEG1V8_NOB2B_EXT	74.991 x 54.41	Core cell including negative 1.0 V ESD clamp
ESDCLAMP_NEG1V8_WITH_B2B_EXT	83.921 x 54.41	

The ALLCELLS cells are not considered part of the Deliverable. These cells are specifically for QA check and hence subject to change, without prior notice.

2.1 VDDCORE_NEG1V8 _EXT_CSF_FC_LIN /CL_LIN

2.1.1 Functional Diagram

Figure 2 : Block diagram



2.1.2 Interface Description

Table 4 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
VDDCORENEG1V8	Input / Output	VDDCORENEG1V8	Dedicated power node, pad side
Track and core pins			
VDDCORENEG1V8	Input / Output	VDDCORENEG1V8	Dedicated power node, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.1.3 Cell Information

Table 5 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (VDDCORENEG1V8 node)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C (VDDCORENEG1V8 node)	-	-	2.5	µA
I_{DC}	DC current Pad To Core [1]	110 °C (VDDCORENEG1V8 node)	-	-	110	mA
		125 °C (VDDCORENEG1V8 node)	-	-	40	
	DC current Pad To Core [2]	110 °C (VDDCORENEG1V8 node)	-	-	38	
		125 °C (VDDCORENEG1V8 node)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (VDDCORENEG1V8 node)	-	-	167	mA
	RMS current Pad To Core [2]	100 °C (VDDCORENEG1V8 node)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

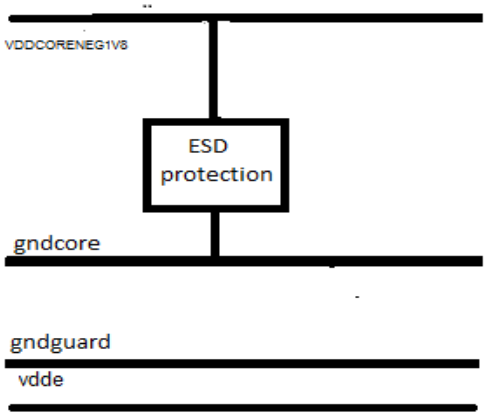
2.1.4 Functional Description

The VDDCORE_NEG1V8_EXT _** cell can be used dedicated core supply cell for core blocks requiring specific supply.

2.2 ESDCLAMP_NEG1V8_NOB2B_EXT

2.2.1 Functional Diagram

Figure 3 : Block diagram



2.2.2 Interface Description

Table 6 : Pin description

Pin	Type	Voltage Level (V)	Description
VDDCORENEG1V8	Input / Output	-1.8 Volts	Dedicated power node
vdde	Input/Output	vdde	Deep Nwell guard ring biasing (1.8/3.3 volts)
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.2.3 Cell Information

Table 7 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (VDDCORENEG1V8 node)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C (VDDCORENEG1V8 node)	-	-	2.5	µA

2.2.4 Functional Description

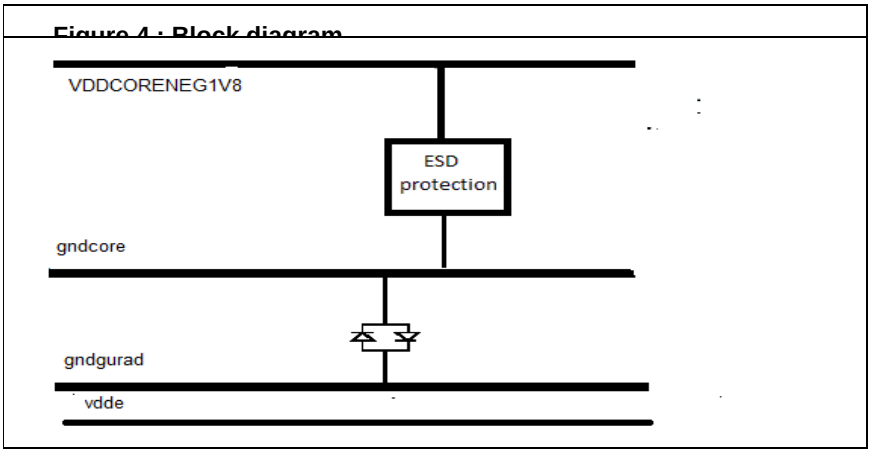
The cell is a core block that protects devices plugged between VDDCORENEG1V8 and gndcore. Pins are provided in metal 5.

As mentioned by cell name, there is no back to back diode between gndcore and gndguard . B2B diodes from C28SOI_IO_EXT_ALLF_CORESUPPLY_EG need to added at core side between gndcore and gndgurad

2.3 ESDCLAMP_NEG1V8_WITH_B2B_EXT

2.3.1 Functional Diagram

Figure 4 : Block diagram



2.3.2 Interface Description

Table 8 : Pin description

Pin	Type	Voltage Level (V)	Description
VDDCORENEG1V8	Input / Output	-1.8 Volts	Dedicated power node
vdde	Input/Output	vdde	Deep Nwell guard ring biasing (1.8/3.3 volts)
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.3.3 Cell Information

Table 9 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (VDDCORENEG1V8 node)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C (VDDCORENEG1V8 node)	-	-	2.5	µA

2.3.4 Functional Description

The cell is a core block that protects devices plugged between VDDCORENEG1V8 and gndcore with back to back diode between gndcore and gndguard Pins are provided in metal 5.

3. Electrical Specifications

3.1 ESD and Latch-up Characteristics

Table 10 : ESD and Latch-up Characteristics

Symbol	Parameter	Condition	Target	Unit
V_{ESD}	Electrostatic discharge voltage	Human Body Model (HBM) [1]	2000	V
		Machine Model (MM) [1]	100	V
		Charge Device Model (CDM)	500V JEDEC	V
	Over-voltage stress		1.5* VDDCORENEG1V8	V

[1] ESD qualification: According to electrostatic discharge sensitivity measurement
[2] Latch-up qualification: According to latch-up sensitivity measurement.

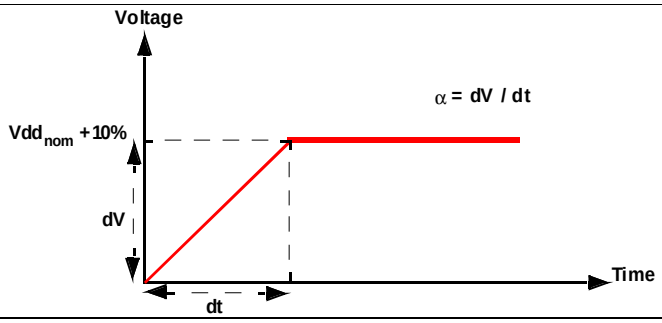
The level of CDM current seen at a given pre-charge voltage varies significantly with the chip size and package type. For instance, larger dies/packages generates higher CDM current.

However, this package size dependence has been considered during IO qualification, so that the above CDM commitment remains valid for any die/package size (even for large die/package sizes of hundreds of mm^2).

3.2 ESD Clamps Power-up Sensitivity

For correct power-up sequence without parasitic clamp switch-on, it is necessary to limit the power rise time as per next table.

Figure 5 : ESD Clamp Power-up Sensitivity



Power Ramp-Up should be equal or slower than 0.5V/us.

4. Usage Guidelines

4.1 Design Requirements

Libraries given by the table below are required to be used with this library.

Table 11 : Mandatory Libraries

Library Name	Description
C28SOI_IO_EXT_CSF_BASIC_EG*	Contains supply, corner and place and route cells needed for a CSF IO ring construction

Only supply cells from other BASICs libraries must be used with dedicated supplies to build an IO ring. The following table lists the mandatory cells required.

Table 12 : Mandatory Cells

Cell Name	Mandatory Nodes	Cell Type
VDDE_*	vdde/ vdde1v8 / vdde3v3	Supply cell
GNDE_*	gnde	Supply cell
GND_EXT_CSF*	gnd	Supply cell

4.2 Physical implementation

For information on IO ring construction and supplies management, See, design requirements section on the C28SOI_IO_EXT_ALLF_CORESUPPLY_EG * User Manual

- The VDDCORE_NEG1V8_EXT*/ ESDCLAMP_NEG1V8: cell requires a power-up sequence. vdde is powered first, followed by VDDCORENEG1V8 .
- Supplying GO1 devices through a VDDCORE_NEG1V8_EXT_**/ ESDCLAMP_NEG1V8* cell is forbidden. VDDCORE_NEG1V8_EXT_**/ ESDCLAMP_NEG1V8** cells must be used only with GO2 devices.
- VDDCORE_NEG1V8_EXT_** / ESDCLAMP_NEG1V8** cell does not protect GO1 device.

4.2.1 Guidelines for placement for VDDCORE_NEG1V8_EXT_CSF_** in IO ring

- GND_EXT_CSF_** cell from **C28SOI_IO_EXT_CSF_BASIC_EG** * library to be used with VDDCORE_NEG1V8_EXT_CSF_** cells

- GNDE_EXT_CSF_** cell from **C28SOI_IO_EXT_CSF_BASIC_EG** * and GNDCORE_EXT_CSF_FC* from C28SOI_**IO_EXT_ALLF_CORESUPPLY_EG library** are not allowed to be used with VDDCORE_NEG1V8_EXT_CSF_* cells.

- The maximum distance between VDDCORE_NEG1V8_EXT_CSF_* cell and GND_CSF* clamp is 400 um

4.2.2 Guidelines for placement for ESDCLAMP_NEG1V8* in core

- BUMP to ESDCLAMP_NEG1V8* core pin and LB routing should have resistance less than 0.5 and should be at least 3 µm wide.

- Back-to-Back diodes need to placed between common ground substrate and ground (GNDCORE) of the clamp cell ESDCLAMP_NEG1V8_NOB2B* cells

5. Contact Information

ST users, login to **HELPDESK**. (http://col2.cro.st.com/helpdesk) for submitting queries or support requests.

Non-ST users, contact Customer Support personnel.

Appendix A: Cell Naming Convention

Table 13 : Naming Convention for Core Supply Cells

Segment Name	Description
Cell type	Refers to the functionality of cell. It can have any of the following values: – GNDCORE (dedicated ground). – VDDCORE_1V0 (dedicated supply 1.0 V). – VDDCORE_1V8 (dedicated supply 1.8 V). – VDDCORE_3V3 (dedicated supply 3.3 V).
1st suffix	Refers to the cell offer. It can have either of the following values: – <none> – EXT: extended CDM specification offer
2nd suffix	Refers to the functionality of cell. It can have any of the following values: – CSF: refers to compatible standard frame. – 3V3SF: refers to 3.3 V standard frame.
3rd suffix	Refers to the layout view of cell. It can have any of the following values: – FC: represents flip-chip configuration. – CL: represents cluster configuration.
4th suffix	Refers to the layout view of cell. It can have any of the following values: – LIN: represents single row configuration.

Table 14 : Example Segments in Name of GNDCORE_EXT_CSF_FC_LIN Cell

Segment Name	Segment Value	Description
Cell type	GNDCORE	Dedicated ground supply.
1st suffix	EXT	Extended CDM specification
2nd suffix	CSF	Uses compatible standard frame.
3rd suffix	FC	Uses flip-chip configuration.
4th suffix	LIN	Uses single row configuration.

Appendix B: Document Revision History

Table 15 : Document Revision History

Date	Document Version	Comments
-January-2016	1.3	• Reference Library added • Table 2 “Acronyms and Abbreviations” added • ESDCLAMP_1V0_45U_130U_EXT added • Aligned to ESD and Latch-up guideline
03-July-2015	1.2	• “ Pin description” tables improved • “ Cell Information“ tables updated
07-Oct-2014	1.1	• Track pins description added • Typo fixed
24-Sept-2014	1.0	• First release

Please Read Carefully: