Layout Finishing and SoC Tiling:
FE density violations

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CMOS and derivative PDK

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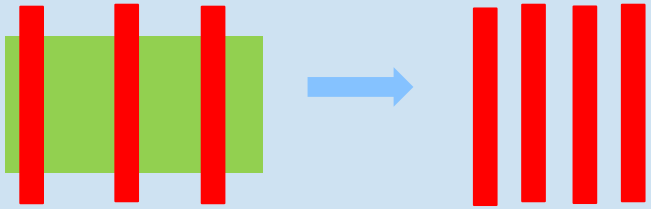
Program Management & Services / Process Design Kit

Blockage layer (exclude) : Cases

- In an exception mode, Tiling-result can be better controlled adding blockage/exclusion CAD marker-layers at top level:
  - For example when IPs are not compliant with sign-off IP-check density rules and some fine tuning is required.

DRC erros	layers	action
PC.DEN.1: min PC density	RX ; exclude	Tiler will replace RTA tiling (not dense regarding PC) by PC fingers.  To be used locally.
RX maximum density	RX ; exclude	Blocks RX tiling generation
PC max density	PC ; exclude	Blocks PC tiling generation

Max PC violation

- The tiler is adding as much as possible dummy transistors, with a single target : do not violate max RX.
- So in some rare occasion, it may add dummy transistors which increase PC density to the point that max PC density is violated.
- In such case, prevent the tiler from adding such dummy transistors by adding **PC; exclude** on related area, and run the tiler back.

We work on a workaround to this « single target » limitation.

Min PC violation

- The tiler is adding as much as possible dummy transistors.
- In some rare occasion, the min PC density may not be reached.
- In such case, prevent the tiler from adding such dummy transistors by adding **RX; exclude** on related area, and run the tiler back.
- PC;fill will be added instead in a denser way

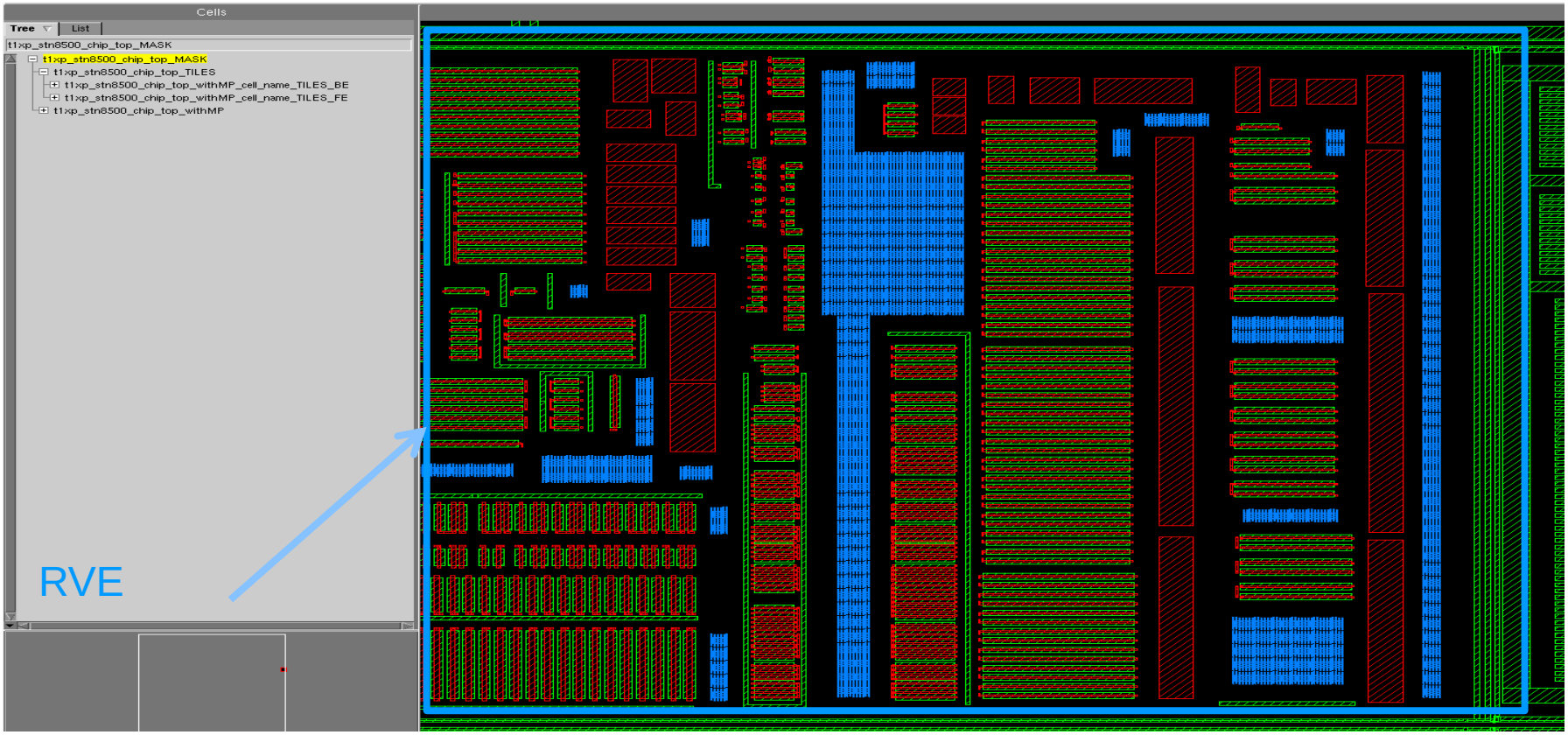
Be careful: you need technologs agreement,
as PC;fill leads to **lower yield** than dummy transistors.

Blockage layer addition: How to (1/5)

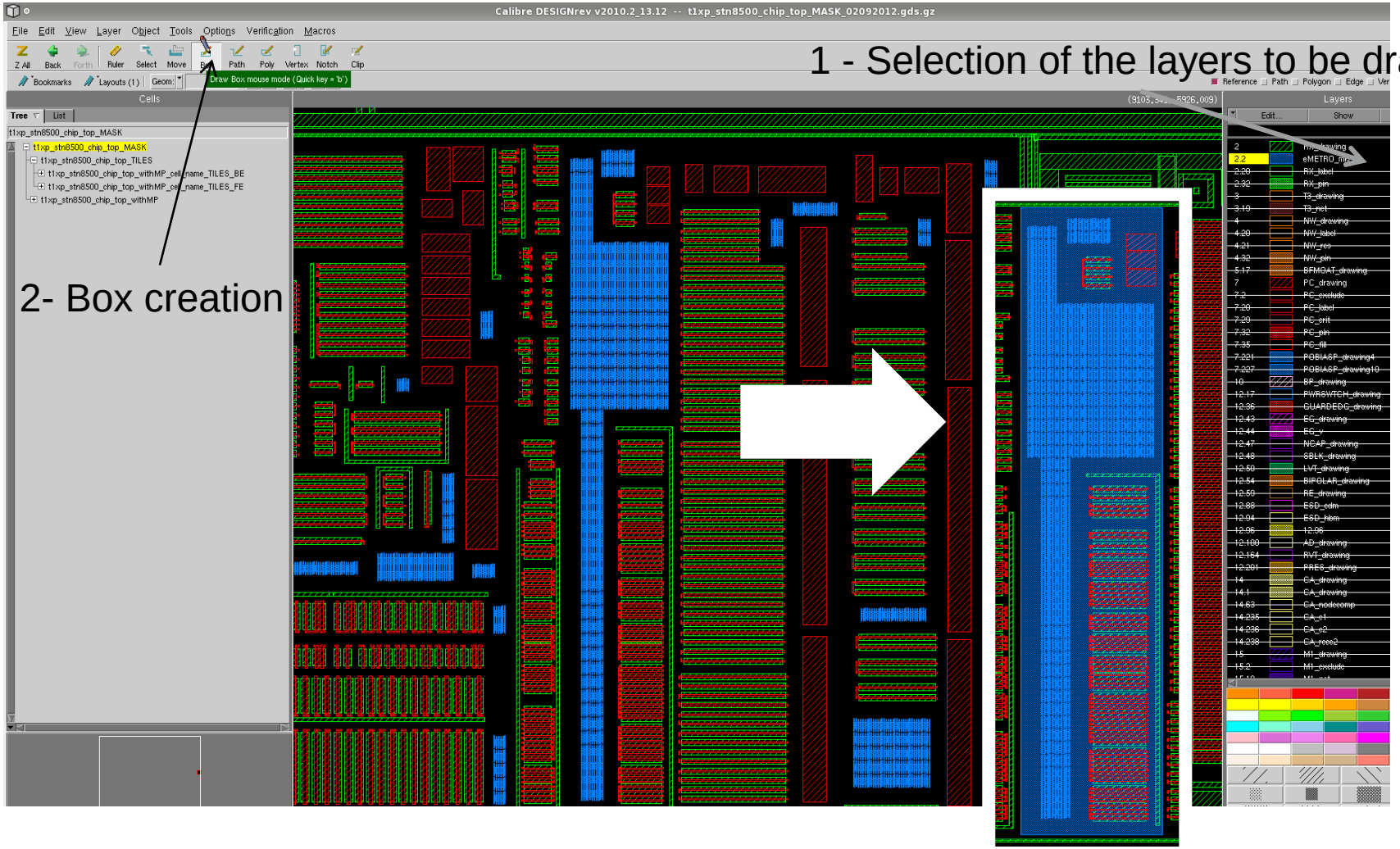
- Example of a Tiling-Methodology to be followed and customized accordingly:
  - Opening of tiled layout in calibredrv
  - Visualization of error in calibredrv
  - Drawing of the exclusion marker at top level of the tiled design.
  - Export of exclusion markers in a new gds
  - Merge this new GDS with the original top
  - Run Tiling back

Blockage layer addition: How to (2/5)

- ‘PC.DEN.1’ DRC error meaning not enough PC. So RX exclude layers must be added to complement PC (PC and RX density fill are linked each other -> refer to DRM tiling algorithm)



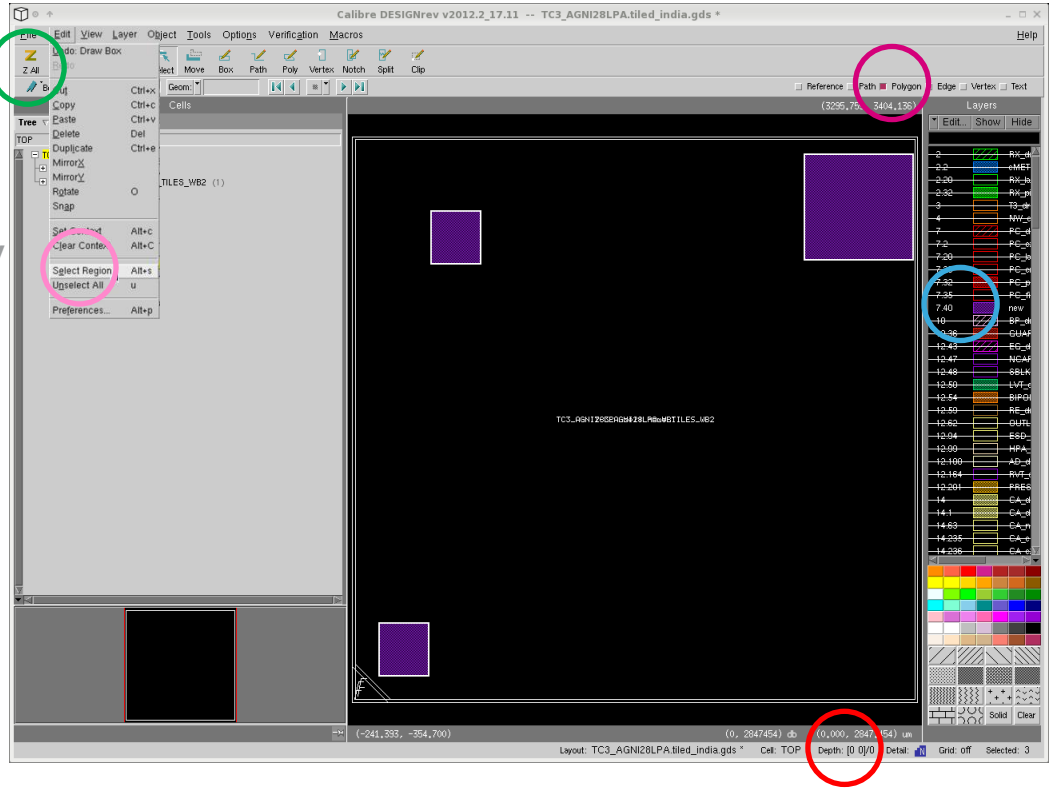
Blockage layer addition: How to (3/5)



Blockage layer addition: How to (4/5)

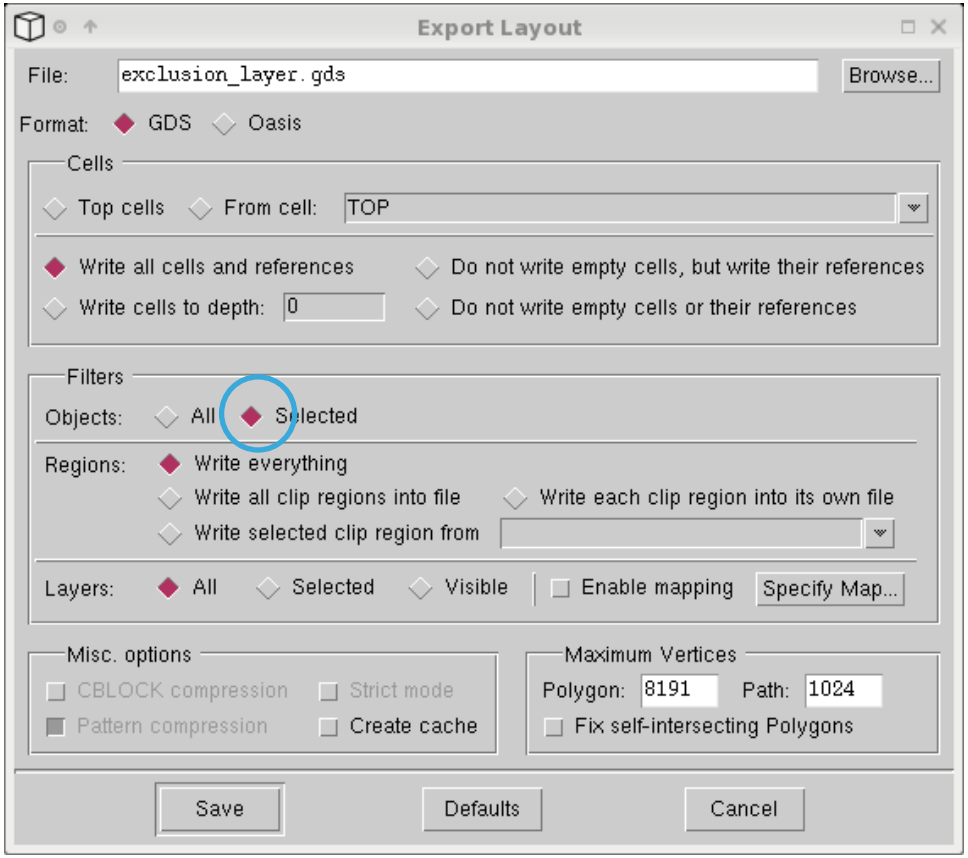
- Repeat again this action for all the areas from which such an extra marker layer is required.

- Then
  1. In Layers pane
     - LMB RX_exclude
     - RMB > Show selected only
  2. In footer bar
     - Depth 0 0
  3. In header bar
     - Tick Polygon only
  3. Zoom All
  4. Edit > Select Region



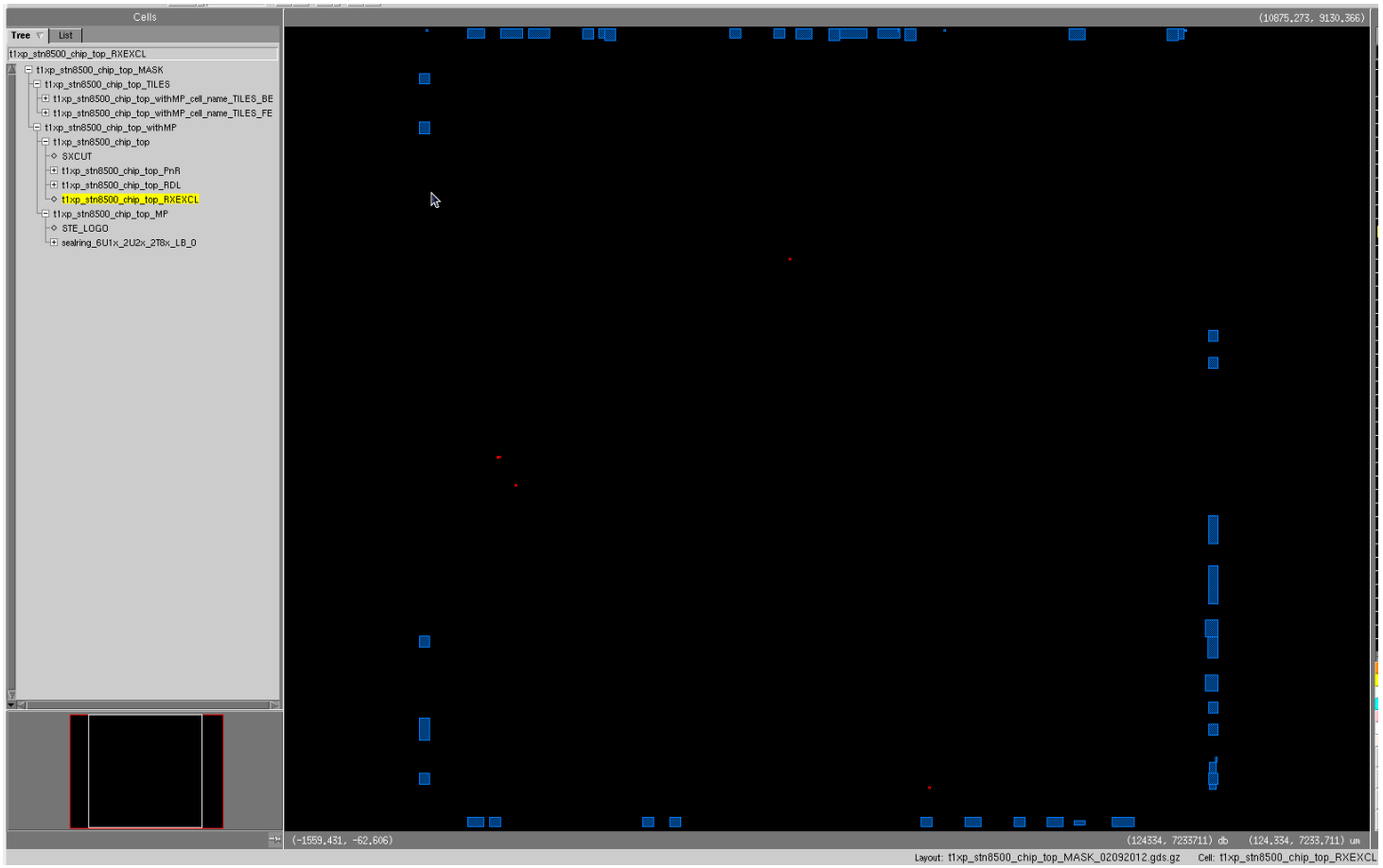
Blockage layer addition: How to (5/5)

- File > Export Layout
- Objects > Selected
- Set output filename
  - file.gds.gz supported
- Save



Blockage layer addition: Final Result

- GDS with exclude layers has been sent to Top designer to be merged with the top design.
- Highlighted in blue here: RX exclude layers



Tiler switch : to be use with caution

- The tiler provides a switch (in Expert Parameters) to run the following steps :
  - Run the tiler
  - Check density
  - If min poly is violated: remove dummy transistors under this error
  - Re-tile with PC;fill only in this area
- This feature should not be used (except with technologs agreement) as using PC;fill instead of dummy transitors lead to poor yield.
- Prefer the local approach described in previous slides for RX_EXCLUDE

THANK YOU !

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