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C28SOI_SC_8_COREPBP10_LL
Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 10 nm

Overview

- C28SOI_SC_8_COREPBP10_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

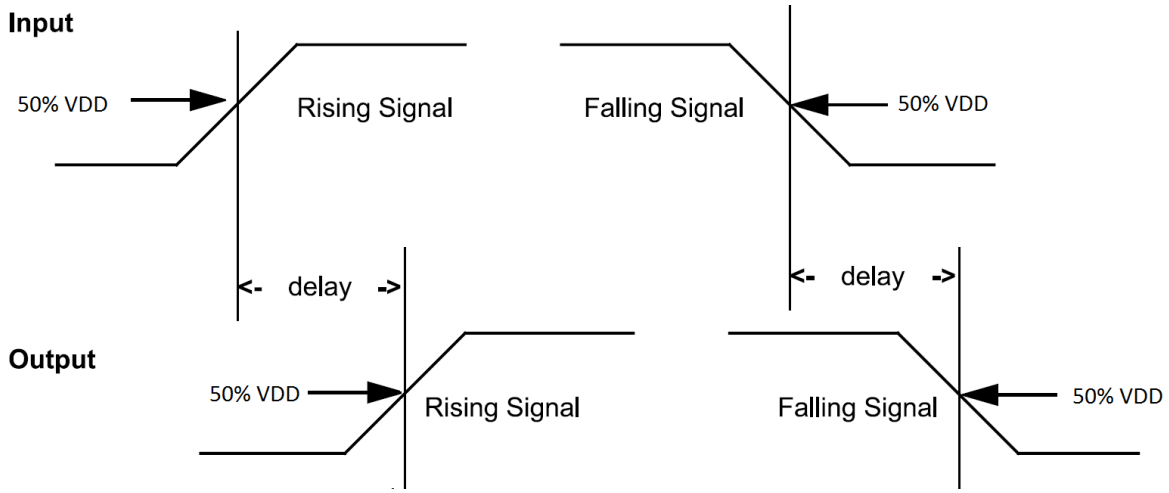


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

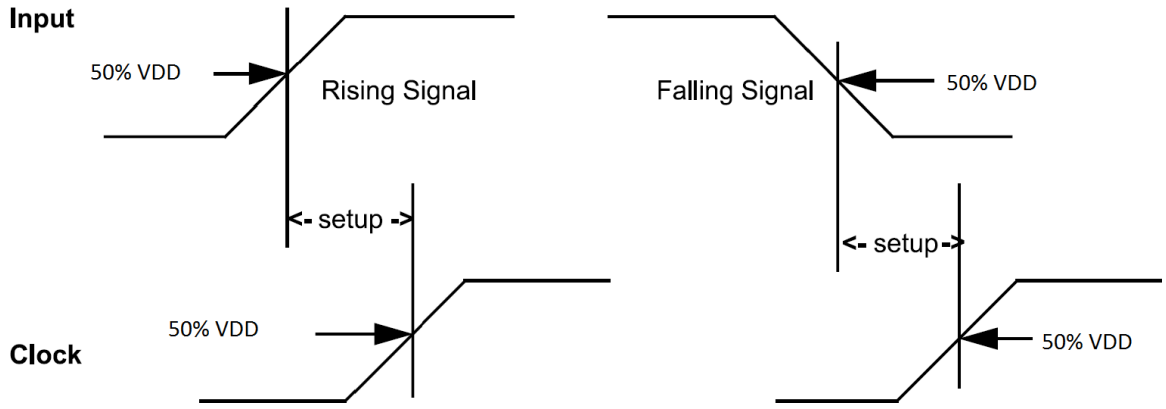


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

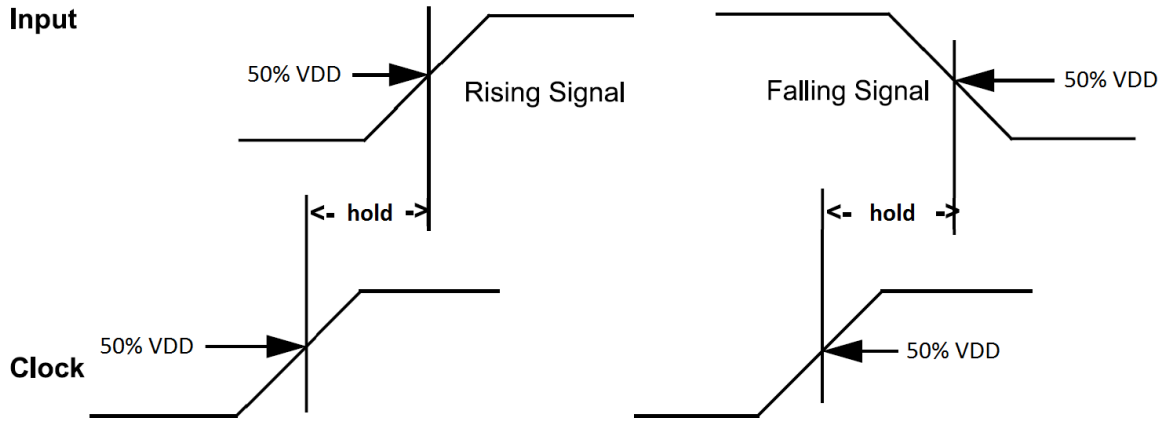


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

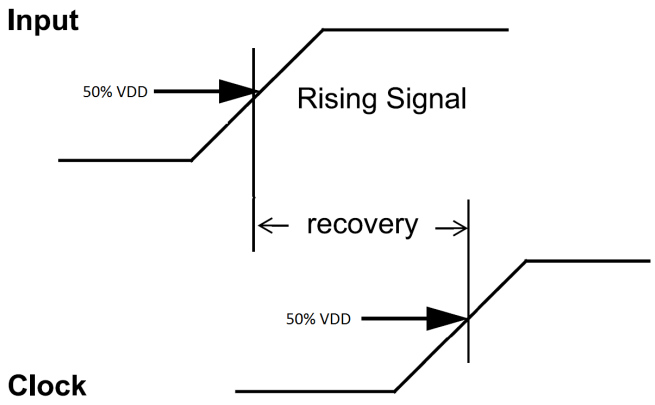


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

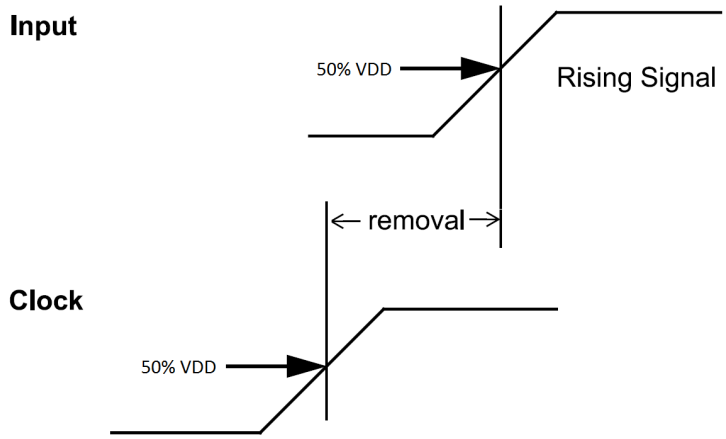


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

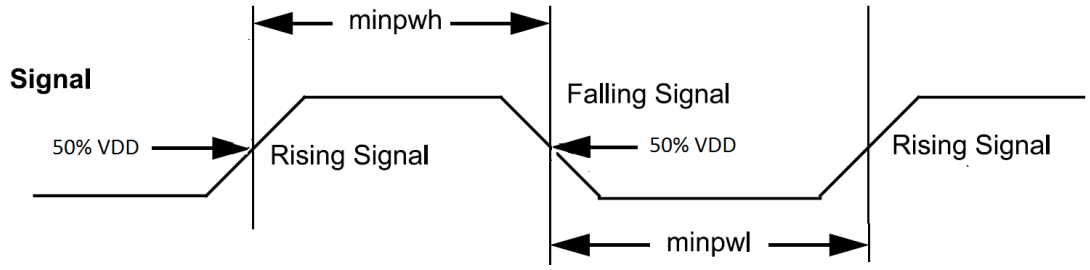


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

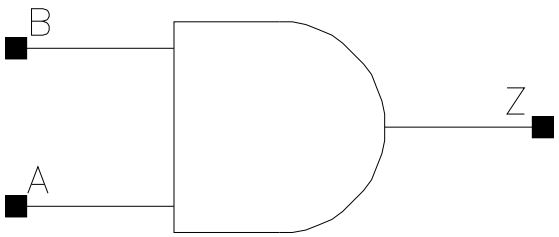
The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description	Logical Symbol
2 input AND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.544	0.4352
X10_P10	0.800	0.680	0.5440
X11_P10	1.600	0.544	0.8704
X19_P10	0.800	1.224	0.9792
X24_P10	0.800	1.360	1.0880
X29_P10	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X11_P10	X19_P10
A	0.0006	0.0008	0.0010	0.0016
B	0.0005	0.0008	0.0010	0.0014
	X24_P10	X29_P10		
A	0.0016	0.0016		
B	0.0014	0.0014		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0254	0.0213	2.9718	1.4197
A to Z ↑	0.0195	0.0190	4.1945	2.0182
B to Z ↓	0.0242	0.0198	2.9711	1.4180
B to Z ↑	0.0215	0.0207	4.1963	2.0178
	X11_P10	**X19_P10**	**X11_P10**	**X19_P10**

A to Z ↓	0.0233	0.0209	1.1381	0.7296
A to Z ↑	0.0173	0.0186	1.9386	1.0171
B to Z ↓	0.0215	0.0199	1.1372	0.7303
B to Z ↑	0.0190	0.0206	1.9397	1.0164
	X24_P10	**X29_P10**	**X24_P10**	**X29_P10**
A to Z ↓	0.0227	0.0242	0.5932	0.4943
A to Z ↑	0.0206	0.0221	0.8156	0.6776
B to Z ↓	0.0219	0.0235	0.5930	0.4943
B to Z ↑	0.0226	0.0243	0.8161	0.6780

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	1.970e-05	1.000e-20
X10_P10	4.412e-05	1.000e-20
X11_P10	4.839e-05	1.000e-20
X19_P10	8.500e-05	1.000e-20
X24_P10	9.906e-05	1.000e-20
X29_P10	1.131e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X11_P10	X19_P10
A (output stable)	8.395e-06	1.565e-05	2.127e-05	3.066e-05
B (output stable)	1.912e-05	3.497e-05	4.779e-05	7.060e-05
A to Z	2.318e-03	4.061e-03	4.745e-03	8.056e-03
B to Z	2.214e-03	3.895e-03	4.467e-03	7.696e-03
	X24_P10	X29_P10		
A (output stable)	3.083e-05	3.022e-05		
B (output stable)	7.115e-05	7.099e-05		
A to Z	9.861e-03	1.163e-02		
B to Z	9.525e-03	1.133e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

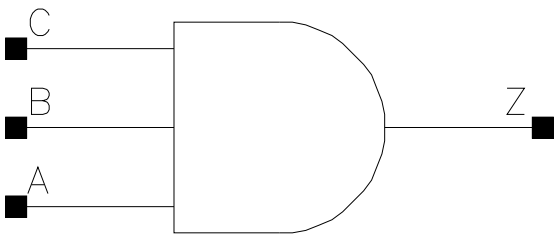
Pin Cycle (vdds)	X5_P10	X10_P10	X11_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P10	X29_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.680	0.5440
X10_P10	0.800	0.816	0.6528
X14_P10	0.800	1.360	1.0880
X19_P10	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0005	0.0008	0.0013	0.0016
B	0.0005	0.0007	0.0011	0.0015
C	0.0005	0.0008	0.0011	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0284	0.0237	3.0024	1.4273
A to Z ↑	0.0258	0.0247	4.2413	2.0431
B to Z ↓	0.0275	0.0225	3.0012	1.4280
B to Z ↑	0.0274	0.0259	4.2411	2.0441
C to Z ↓	0.0262	0.0212	3.0001	1.4261
C to Z ↑	0.0289	0.0271	4.2408	2.0445
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0237	0.0227	0.9859	0.7324

A to Z ↑	0.0233	0.0232	1.3885	1.0267
B to Z ↓	0.0225	0.0215	0.9848	0.7315
B to Z ↑	0.0247	0.0245	1.3880	1.0269
C to Z ↓	0.0213	0.0202	0.9843	0.7314
C to Z ↑	0.0261	0.0257	1.3878	1.0264

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	1.931e-05	1.000e-20
X10_P10	4.324e-05	1.000e-20
X14_P10	6.136e-05	1.000e-20
X19_P10	8.416e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.045e-05	2.037e-05	2.764e-05	3.707e-05
B (output stable)	1.653e-05	3.062e-05	4.357e-05	6.030e-05
C (output stable)	4.116e-05	7.736e-05	1.132e-04	1.626e-04
A to Z	2.690e-03	4.696e-03	6.857e-03	9.033e-03
B to Z	2.584e-03	4.509e-03	6.552e-03	8.628e-03
C to Z	2.488e-03	4.329e-03	6.284e-03	8.239e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

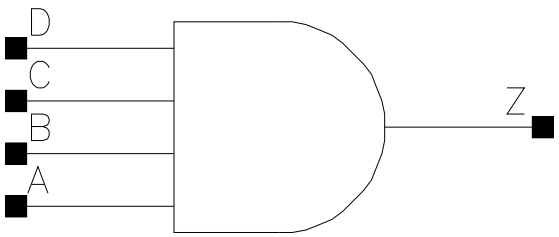
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.088	0.8704
X3_P10	0.800	1.088	0.8704
X10_P10	0.800	2.176	1.7408
X13_P10	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P10	X3_P10	X10_P10	X13_P10
A	0.0005	0.0006	0.0012	0.0014
B	0.0005	0.0005	0.0012	0.0014
C	0.0005	0.0005	0.0012	0.0014
D	0.0006	0.0006	0.0012	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	X3_P10	X2_P10	X3_P10
A to Z ↓	0.0224	0.0241	5.3210	3.5932
A to Z ↑	0.0219	0.0220	13.6898	7.5084
B to Z ↓	0.0208	0.0231	5.3147	3.5938
B to Z ↑	0.0235	0.0239	13.6963	7.5116
C to Z ↓	0.0227	0.0247	5.3168	3.5945
C to Z ↑	0.0218	0.0220	13.7113	7.5179

D to Z ↓	0.0214	0.0239	5.3180	3.5901
D to Z ↑	0.0238	0.0247	13.7144	7.5172
	X10_P10	**X13_P10**	**X10_P10**	**X13_P10**
A to Z ↓	0.0235	0.0233	1.2346	0.9201
A to Z ↑	0.0217	0.0234	2.5078	1.9234
B to Z ↓	0.0223	0.0212	1.2351	0.9186
B to Z ↑	0.0235	0.0245	2.5084	1.9234
C to Z ↓	0.0233	0.0223	1.2269	0.9218
C to Z ↑	0.0209	0.0207	2.5059	1.9193
D to Z ↓	0.0210	0.0203	1.2248	0.9192
D to Z ↑	0.0219	0.0219	2.5046	1.9180

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P10	1.628e-05	1.000e-20
X3_P10	2.185e-05	1.000e-20
X10_P10	6.619e-05	1.000e-20
X13_P10	9.049e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P10	X3_P10	X10_P10	X13_P10
A (output stable)	5.015e-04	5.901e-04	1.584e-03	2.075e-03
B (output stable)	4.639e-04	5.488e-04	1.470e-03	1.929e-03
C (output stable)	4.978e-04	5.454e-04	1.423e-03	1.807e-03
D (output stable)	4.584e-04	5.128e-04	1.296e-03	1.654e-03
A to Z	1.808e-03	2.393e-03	6.898e-03	9.109e-03
B to Z	1.707e-03	2.281e-03	6.597e-03	8.543e-03
C to Z	1.822e-03	2.345e-03	6.111e-03	7.705e-03
D to Z	1.719e-03	2.263e-03	5.633e-03	7.160e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

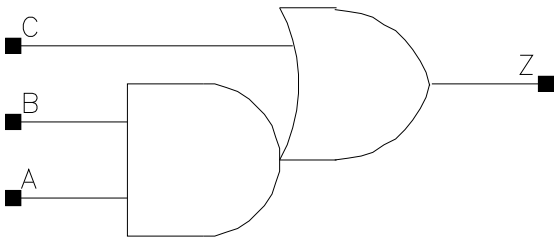
Pin Cycle (vdds)	X2_P10	X3_P10	X10_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	0.952	0.7616
X19_P10	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0005	0.0007	0.0014
B	0.0005	0.0007	0.0012
C	0.0005	0.0008	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0341	0.0309	2.8573	1.4313
A to Z ↑	0.0219	0.0206	3.9156	1.9948
B to Z ↓	0.0320	0.0287	2.8478	1.4258
B to Z ↑	0.0242	0.0228	3.9132	1.9937
C to Z ↓	0.0331	0.0288	2.8455	1.4258
C to Z ↑	0.0215	0.0200	3.8877	1.9804
	X19_P10		**X19_P10**	
A to Z ↓	0.0297		0.7446	
A to Z ↑	0.0227		1.0057	

B to Z ↓	0.0285		0.7444	
B to Z ↑	0.0250		1.0062	
C to Z ↓	0.0283		0.7429	
C to Z ↑	0.0217		0.9974	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	2.083e-05	1.000e-20
X10_P10	4.178e-05	1.000e-20
X19_P10	7.687e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	3.466e-05	4.887e-05	1.097e-04
B (output stable)	3.778e-05	5.831e-05	1.238e-04
C (output stable)	4.430e-05	5.912e-05	1.383e-04
A to Z	2.709e-03	4.670e-03	9.049e-03
B to Z	2.595e-03	4.469e-03	8.791e-03
C to Z	2.891e-03	4.854e-03	9.459e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

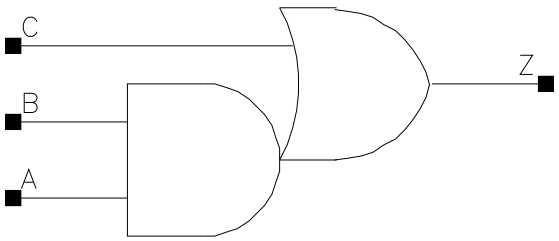
Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	0.952	0.7616
X14_P10	0.800	1.632	1.3056
X19_P10	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0005	0.0007	0.0014	0.0014
B	0.0005	0.0007	0.0015	0.0014
C	0.0006	0.0007	0.0015	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0342	0.0305	2.8495	1.4406
A to Z ↑	0.0241	0.0230	3.9947	2.0132
B to Z ↓	0.0326	0.0290	2.8410	1.4379
B to Z ↑	0.0270	0.0253	3.9923	2.0122
C to Z ↓	0.0311	0.0287	2.8321	1.4330
C to Z ↑	0.0185	0.0172	3.9477	1.9920
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0278	0.0300	0.9858	0.7399

A to Z ↑	0.0212	0.0227	1.3682	1.0210
B to Z ↓	0.0251	0.0274	0.9825	0.7372
B to Z ↑	0.0228	0.0245	1.3693	1.0196
C to Z ↓	0.0244	0.0267	0.9797	0.7349
C to Z ↑	0.0151	0.0164	1.3543	1.0079

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	2.092e-05	1.000e-20
X10_P10	3.990e-05	1.000e-20
X14_P10	7.197e-05	1.000e-20
X19_P10	8.256e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.180e-05	1.519e-05	4.988e-05	4.995e-05
B (output stable)	1.622e-05	2.097e-05	9.154e-05	9.159e-05
C (output stable)	1.628e-04	1.870e-04	5.420e-04	5.425e-04
A to Z	2.947e-03	4.799e-03	8.165e-03	9.948e-03
B to Z	2.838e-03	4.620e-03	7.561e-03	9.343e-03
C to Z	2.507e-03	4.167e-03	6.715e-03	8.318e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

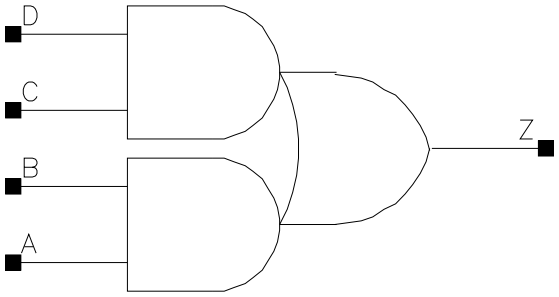
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.088	0.8704
X10_P10	0.800	1.088	0.8704
X14_P10	0.800	1.768	1.4144
X19_P10	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0006	0.0007	0.0015	0.0015
B	0.0006	0.0009	0.0013	0.0013
C	0.0005	0.0007	0.0015	0.0015
D	0.0006	0.0008	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0352	0.0307	2.8626	1.4433
A to Z ↑	0.0256	0.0245	4.0263	1.9978
B to Z ↓	0.0321	0.0281	2.8502	1.4368

B to Z ↑	0.0271	0.0263	4.0255	1.9972
C to Z ↓	0.0328	0.0293	2.8524	1.4370
C to Z ↑	0.0214	0.0203	4.0157	1.9915
D to Z ↓	0.0312	0.0277	2.8463	1.4348
D to Z ↑	0.0238	0.0225	4.0144	1.9910
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0275	0.0299	0.9852	0.7429
A to Z ↑	0.0216	0.0233	1.3734	1.0274
B to Z ↓	0.0256	0.0281	0.9839	0.7418
B to Z ↑	0.0237	0.0255	1.3729	1.0270
C to Z ↓	0.0264	0.0288	0.9825	0.7410
C to Z ↑	0.0182	0.0199	1.3681	1.0242
D to Z ↓	0.0247	0.0273	0.9814	0.7401
D to Z ↑	0.0199	0.0219	1.3673	1.0237

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	2.503e-05	1.000e-20
X10_P10	4.946e-05	1.000e-20
X14_P10	8.256e-05	1.000e-20
X19_P10	9.489e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	2.687e-05	3.536e-05	4.468e-05	4.494e-05
B (output stable)	1.202e-04	1.106e-04	6.587e-05	6.612e-05
C (output stable)	3.792e-05	4.844e-05	1.153e-04	1.156e-04
D (output stable)	4.313e-05	6.169e-05	1.407e-04	1.410e-04
A to Z	3.333e-03	5.401e-03	8.490e-03	1.042e-02
B to Z	3.046e-03	4.988e-03	8.045e-03	9.980e-03
C to Z	2.882e-03	4.721e-03	7.294e-03	9.171e-03
D to Z	2.753e-03	4.527e-03	6.889e-03	8.780e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

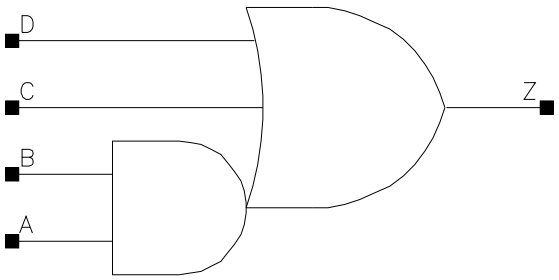
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	1.088	0.8704
X19_P10	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0005	0.0007	0.0013
B	0.0005	0.0007	0.0013
C	0.0006	0.0007	0.0014
D	0.0005	0.0007	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0419	0.0369	3.1525	1.4913
A to Z ↑	0.0227	0.0201	4.1650	2.0068
B to Z ↓	0.0401	0.0343	3.1469	1.4843
B to Z ↑	0.0250	0.0222	4.1600	2.0061
C to Z ↓	0.0417	0.0363	3.1435	1.4856
C to Z ↑	0.0219	0.0282	4.1318	2.0069

D to Z ↓	0.0423	0.0372	3.1456	1.4867
D to Z ↑	0.0217	0.0277	4.1312	2.0044
	X19_P10		**X19_P10**	
A to Z ↓	0.0365		0.7710	
A to Z ↑	0.0223		0.9988	
B to Z ↓	0.0333		0.7668	
B to Z ↑	0.0238		0.9983	
C to Z ↓	0.0354		0.7674	
C to Z ↑	0.0232		0.9918	
D to Z ↓	0.0356		0.7682	
D to Z ↑	0.0229		0.9907	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	1.670e-05	1.000e-20
X10_P10	3.588e-05	1.000e-20
X19_P10	6.703e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	4.067e-05	8.631e-05	1.519e-04
B (output stable)	4.076e-05	8.668e-05	1.722e-04
C (output stable)	2.134e-05	3.865e-05	8.174e-05
D (output stable)	2.972e-05	5.495e-05	1.040e-04
A to Z	2.870e-03	4.965e-03	9.813e-03
B to Z	2.762e-03	4.736e-03	9.199e-03
C to Z	3.149e-03	5.614e-03	1.070e-02
D to Z	3.012e-03	5.373e-03	1.017e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

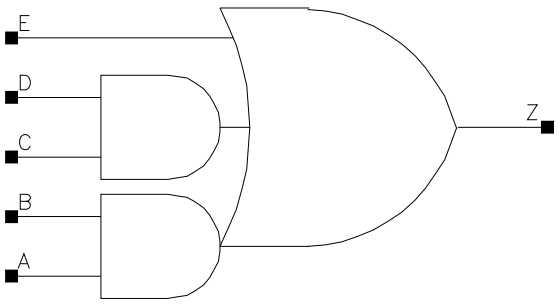
Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.088	0.8704
X10_P10	0.800	1.224	0.9792
X19_P10	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0005	0.0007	0.0014
B	0.0005	0.0007	0.0013
C	0.0005	0.0009	0.0014
D	0.0005	0.0007	0.0013
E	0.0005	0.0007	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0503	0.0409	2.9866	1.4860
A to Z ↑	0.0295	0.0258	4.0632	2.0183

B to Z ↓	0.0492	0.0389	2.9785	1.4831
B to Z ↑	0.0328	0.0282	4.0608	2.0154
C to Z ↓	0.0462	0.0383	2.9768	1.4820
C to Z ↑	0.0253	0.0215	4.0361	2.0035
D to Z ↓	0.0433	0.0349	2.9620	1.4741
D to Z ↑	0.0278	0.0233	4.0343	2.0034
E to Z ↓	0.0452	0.0367	2.9612	1.4761
E to Z ↑	0.0234	0.0204	3.9955	1.9886
	X19_P10		**X19_P10**	
A to Z ↓	0.0396		0.7647	
A to Z ↑	0.0267		1.0129	
B to Z ↓	0.0376		0.7632	
B to Z ↑	0.0294		1.0118	
C to Z ↓	0.0362		0.7619	
C to Z ↑	0.0218		1.0049	
D to Z ↓	0.0341		0.7595	
D to Z ↑	0.0240		1.0043	
E to Z ↓	0.0354		0.7601	
E to Z ↑	0.0257		1.0008	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	2.081e-05	1.000e-20
X10_P10	4.368e-05	1.000e-20
X19_P10	8.003e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	1.243e-05	2.120e-05	4.276e-05
B (output stable)	1.758e-05	2.452e-05	4.653e-05
C (output stable)	5.379e-05	7.383e-05	1.597e-04
D (output stable)	5.625e-05	8.761e-05	1.703e-04
E (output stable)	8.168e-05	1.191e-04	2.464e-04
A to Z	3.877e-03	6.184e-03	1.194e-02
B to Z	3.786e-03	5.961e-03	1.151e-02
C to Z	3.280e-03	5.188e-03	9.863e-03
D to Z	3.147e-03	4.922e-03	9.479e-03
E to Z	3.365e-03	5.359e-03	1.042e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

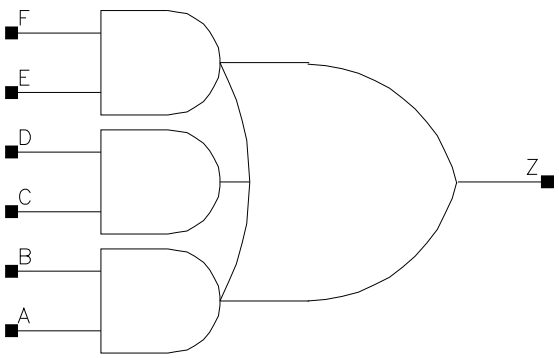
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.360	1.0880
X5_P10	0.800	1.360	1.0880
X10_P10	0.800	1.632	1.3056
X19_P10	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P10	X5_P10	X10_P10	X19_P10
A	0.0006	0.0006	0.0008	0.0014

B	0.0006	0.0006	0.0009	0.0013
C	0.0008	0.0008	0.0007	0.0013
D	0.0006	0.0006	0.0007	0.0013
E	0.0008	0.0008	0.0007	0.0014
F	0.0006	0.0006	0.0007	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X5_P10**	**X2_P10**	**X5_P10**
A to Z ↓	0.0390	0.0407	5.5241	3.0714
A to Z ↑	0.0291	0.0290	7.6772	4.2479
B to Z ↓	0.0369	0.0387	5.5020	3.0609
B to Z ↑	0.0320	0.0321	7.6704	4.2446
C to Z ↓	0.0366	0.0384	5.5196	3.0692
C to Z ↑	0.0267	0.0267	7.6067	4.2163
D to Z ↓	0.0334	0.0352	5.4981	3.0590
D to Z ↑	0.0287	0.0289	7.6005	4.2132
E to Z ↓	0.0317	0.0335	5.4913	3.0566
E to Z ↑	0.0217	0.0218	7.5597	4.1953
F to Z ↓	0.0291	0.0310	5.4727	3.0482
F to Z ↑	0.0234	0.0237	7.5595	4.1956
	X10_P10	**X19_P10**	**X10_P10**	**X19_P10**
A to Z ↓	0.0440	0.0414	1.4842	0.7628
A to Z ↑	0.0317	0.0290	2.0300	1.0177
B to Z ↓	0.0415	0.0397	1.4763	0.7617
B to Z ↑	0.0340	0.0317	2.0279	1.0172
C to Z ↓	0.0410	0.0388	1.4799	0.7621
C to Z ↑	0.0281	0.0265	2.0171	1.0112
D to Z ↓	0.0393	0.0374	1.4755	0.7608
D to Z ↑	0.0309	0.0291	2.0153	1.0110
E to Z ↓	0.0375	0.0365	1.4749	0.7596
E to Z ↑	0.0238	0.0228	2.0070	1.0072
F to Z ↓	0.0352	0.0343	1.4691	0.7576
F to Z ↑	0.0261	0.0251	2.0064	1.0065

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P10	2.389e-05	1.000e-20
X5_P10	3.011e-05	1.000e-20
X10_P10	4.969e-05	1.000e-20
X19_P10	9.518e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P10	X5_P10	X10_P10	X19_P10
A (output stable)	2.586e-05	2.586e-05	3.899e-05	5.860e-05
B (output stable)	2.891e-05	2.890e-05	8.032e-05	6.769e-05
C (output stable)	4.281e-05	4.287e-05	4.355e-05	9.082e-05
D (output stable)	5.008e-05	5.013e-05	5.126e-05	1.079e-04
E (output stable)	1.002e-04	1.003e-04	1.327e-04	2.166e-04
F (output stable)	1.093e-04	1.094e-04	1.353e-04	2.312e-04

A to Z	3.510e-03	4.173e-03	6.911e-03	1.283e-02
B to Z	3.355e-03	4.012e-03	6.528e-03	1.242e-02
C to Z	2.949e-03	3.595e-03	6.147e-03	1.147e-02
D to Z	2.775e-03	3.413e-03	5.964e-03	1.112e-02
E to Z	2.374e-03	2.984e-03	5.415e-03	1.028e-02
F to Z	2.230e-03	2.836e-03	5.217e-03	9.891e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

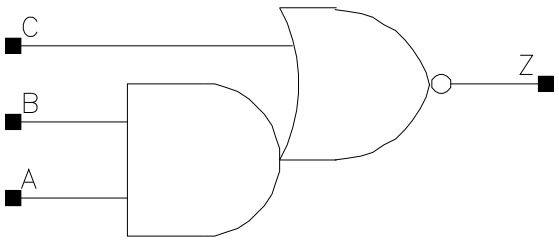
Pin Cycle (vdds)	X2_P10	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X10_P10	0.800	1.360	1.0880
X19_P10	0.800	2.584	2.0672
X25_P10	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P10	X10_P10	X19_P10	X25_P10
A	0.0007	0.0018	0.0035	0.0046
B	0.0006	0.0016	0.0032	0.0044
C	0.0007	0.0019	0.0035	0.0047

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X10_P10**	**X3_P10**	**X10_P10**
A to Z ↓	0.0069	0.0073	4.6148	1.6660
A to Z ↑	0.0147	0.0150	7.2417	2.4785
B to Z ↓	0.0079	0.0083	4.6830	1.6898
B to Z ↑	0.0120	0.0118	7.1192	2.4732
C to Z ↓	0.0082	0.0084	2.9635	1.0288
C to Z ↑	0.0134	0.0136	6.5912	2.2775
	X19_P10	**X25_P10**	**X19_P10**	**X25_P10**
A to Z ↓	0.0077	0.0078	0.8510	0.6494

A to Z ↑	0.0154	0.0152	1.2702	0.9455
B to Z ↓	0.0083	0.0083	0.8637	0.6594
B to Z ↑	0.0120	0.0119	1.2698	0.9577
C to Z ↓	0.0101	0.0102	0.6252	0.4779
C to Z ↑	0.0137	0.0136	1.1695	0.8757

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.804e-05	1.000e-20
X10_P10	4.952e-05	1.000e-20
X19_P10	9.509e-05	1.000e-20
X25_P10	1.258e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X10_P10	X19_P10	X25_P10
A (output stable)	4.833e-05	1.699e-04	3.313e-04	4.340e-04
B (output stable)	6.226e-05	2.186e-04	4.320e-04	5.595e-04
C (output stable)	6.211e-05	2.009e-04	3.900e-04	5.316e-04
A to Z	1.222e-03	3.724e-03	7.573e-03	9.964e-03
B to Z	1.049e-03	2.999e-03	6.068e-03	8.021e-03
C to Z	1.589e-03	4.715e-03	9.185e-03	1.221e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

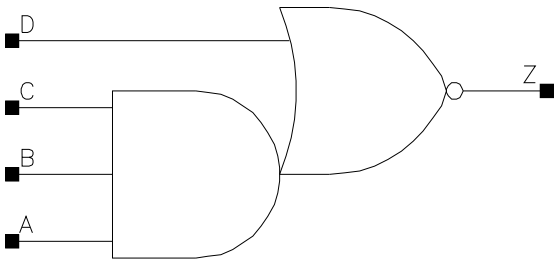
Pin Cycle (vdds)	X3_P10	X10_P10	X19_P10	X25_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X17_P10	0.800	3.536	2.8288
X22_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X17_P10	X22_P10
A	0.0006	0.0035	0.0048
B	0.0006	0.0033	0.0044
C	0.0007	0.0031	0.0043
D	0.0007	0.0036	0.0047

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X17_P10	X3_P10	X17_P10
A to Z ↓	0.0109	0.0116	6.3186	1.2099
A to Z ↑	0.0189	0.0183	7.2512	1.2227
B to Z ↓	0.0118	0.0121	6.3458	1.2159
B to Z ↑	0.0169	0.0162	7.2663	1.2434
C to Z ↓	0.0131	0.0121	6.3992	1.2238
C to Z ↑	0.0155	0.0131	7.2921	1.2522
D to Z ↓	0.0103	0.0121	2.9015	0.6155

D to Z ↑	0.0172	0.0160	6.2259	1.0606
	X22_P10		**X22_P10**	
A to Z ↓	0.0115		0.9196	
A to Z ↑	0.0180		0.9145	
B to Z ↓	0.0119		0.9247	
B to Z ↑	0.0159		0.9334	
C to Z ↓	0.0120		0.9311	
C to Z ↑	0.0130		0.9424	
D to Z ↓	0.0128		0.5097	
D to Z ↑	0.0154		0.7938	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.892e-05	1.000e-20
X17_P10	9.372e-05	1.000e-20
X22_P10	1.218e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X17_P10	X22_P10
A (output stable)	3.943e-05	2.431e-04	3.184e-04
B (output stable)	4.361e-05	3.091e-04	4.045e-04
C (output stable)	5.969e-05	5.653e-04	7.368e-04
D (output stable)	9.604e-05	5.790e-04	7.697e-04
A to Z	1.703e-03	9.747e-03	1.274e-02
B to Z	1.502e-03	8.227e-03	1.073e-02
C to Z	1.330e-03	6.777e-03	8.834e-03
D to Z	2.142e-03	1.156e-02	1.502e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

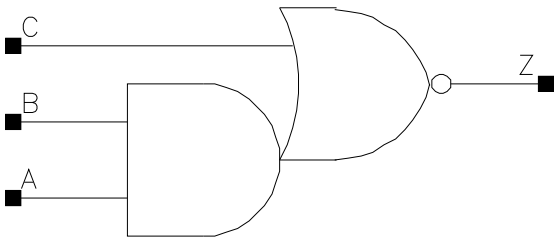
Pin Cycle (vdds)	X3_P10	X17_P10	X22_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X6_P10	0.800	1.088	0.8704
X9_P10	0.800	1.360	1.0880
X12_P10	0.800	1.904	1.5232
X25_P10	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X9_P10	X12_P10
A	0.0006	0.0013	0.0019	0.0026
B	0.0006	0.0012	0.0018	0.0024
C	0.0007	0.0011	0.0016	0.0022
	X25_P10			
A	0.0051			
B	0.0047			
C	0.0043			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0103	0.0100	5.9719	2.4296
A to Z ↑	0.0149	0.0159	8.2078	3.6829
B to Z ↓	0.0121	0.0108	6.0277	2.4600

B to Z ↑	0.0130	0.0128	8.0992	3.6993
C to Z ↓	0.0064	0.0057	3.8939	1.8548
C to Z ↑	0.0126	0.0118	7.5790	3.4281
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0095	0.0099	1.6657	1.2511
A to Z ↑	0.0148	0.0150	2.4679	1.8231
B to Z ↓	0.0108	0.0107	1.6881	1.2678
B to Z ↑	0.0118	0.0119	2.4713	1.8504
C to Z ↓	0.0057	0.0056	1.2624	0.9445
C to Z ↑	0.0112	0.0113	2.2981	1.7111
	X25_P10		**X25_P10**	
A to Z ↓	0.0098		0.6512	
A to Z ↑	0.0145		0.9265	
B to Z ↓	0.0108		0.6592	
B to Z ↑	0.0115		0.9318	
C to Z ↓	0.0055		0.4795	
C to Z ↑	0.0109		0.8664	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.455e-05	1.000e-20
X6_P10	3.470e-05	1.000e-20
X9_P10	4.899e-05	1.000e-20
X12_P10	6.600e-05	1.000e-20
X25_P10	1.284e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	1.513e-05	4.931e-05	6.394e-05	9.466e-05
B (output stable)	2.002e-05	9.072e-05	1.061e-04	1.688e-04
C (output stable)	1.986e-04	5.283e-04	6.433e-04	8.990e-04
A to Z	1.381e-03	3.345e-03	4.662e-03	6.393e-03
B to Z	1.232e-03	2.802e-03	3.869e-03	5.261e-03
C to Z	9.741e-04	2.162e-03	3.031e-03	4.162e-03
	X25_P10			
A (output stable)	1.800e-04			
B (output stable)	3.022e-04			
C (output stable)	1.696e-03			
A to Z	1.226e-02			
B to Z	1.018e-02			
C to Z	7.977e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

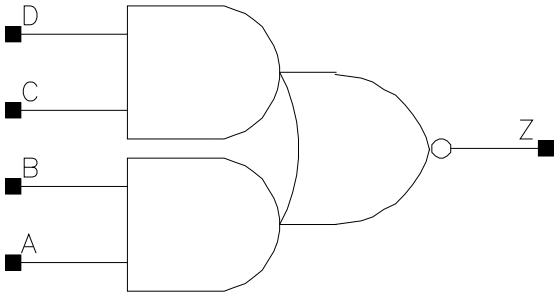
	X25_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.680	0.5440
X6_P10	0.800	1.224	0.9792
X9_P10	0.800	1.768	1.4144
X12_P10	0.800	2.448	1.9584
X24_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P10	X6_P10	X9_P10	X12_P10
A	0.0005	0.0013	0.0019	0.0026
B	0.0005	0.0012	0.0018	0.0025
C	0.0005	0.0013	0.0018	0.0024
D	0.0005	0.0011	0.0017	0.0023
	X24_P10			
A	0.0050			
B	0.0049			
C	0.0048			
D	0.0045			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X6_P10**	**X2_P10**	**X6_P10**
A to Z ↓	0.0103	0.0109	6.0766	2.3291
A to Z ↑	0.0192	0.0166	10.1419	3.3616
B to Z ↓	0.0120	0.0125	6.1550	2.3553
B to Z ↑	0.0168	0.0145	10.1223	3.4374
C to Z ↓	0.0069	0.0071	6.1045	2.3432
C to Z ↑	0.0165	0.0145	10.1732	3.3714
D to Z ↓	0.0080	0.0082	6.2062	2.3781
D to Z ↑	0.0139	0.0124	10.1468	3.4788
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0117	0.0122	1.6664	1.2559
A to Z ↑	0.0175	0.0178	2.2554	1.6955
B to Z ↓	0.0135	0.0135	1.6855	1.2700
B to Z ↑	0.0149	0.0150	2.2615	1.6766
C to Z ↓	0.0077	0.0082	1.6664	1.2607
C to Z ↑	0.0153	0.0157	2.2643	1.6894
D to Z ↓	0.0089	0.0087	1.6923	1.2801
D to Z ↑	0.0124	0.0125	2.2655	1.6975
	X24_P10		**X24_P10**	
A to Z ↓	0.0122		0.6476	
A to Z ↑	0.0175		0.8559	
B to Z ↓	0.0137		0.6549	
B to Z ↑	0.0148		0.8505	
C to Z ↓	0.0082		0.6350	
C to Z ↑	0.0157		0.8566	
D to Z ↓	0.0088		0.6453	
D to Z ↑	0.0126		0.8608	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P10	1.310e-05	1.000e-20
X6_P10	4.130e-05	1.000e-20
X9_P10	5.944e-05	1.000e-20
X12_P10	7.953e-05	1.000e-20
X24_P10	1.552e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P10	X6_P10	X9_P10	X12_P10
A (output stable)	1.764e-05	4.469e-05	8.538e-05	1.270e-04
B (output stable)	2.390e-05	6.603e-05	1.710e-04	2.702e-04
C (output stable)	5.044e-05	1.124e-04	1.985e-04	2.827e-04
D (output stable)	6.088e-05	1.412e-04	2.742e-04	4.099e-04
A to Z	1.414e-03	3.764e-03	5.866e-03	8.009e-03
B to Z	1.248e-03	3.326e-03	5.077e-03	6.932e-03
C to Z	9.520e-04	2.603e-03	4.076e-03	5.611e-03
D to Z	8.096e-04	2.226e-03	3.373e-03	4.596e-03
	X24_P10			
A (output stable)	2.352e-04			
B (output stable)	4.549e-04			
C (output stable)	5.412e-04			
D (output stable)	7.918e-04			

A to Z	1.557e-02			
B to Z	1.353e-02			
C to Z	1.101e-02			
D to Z	9.064e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

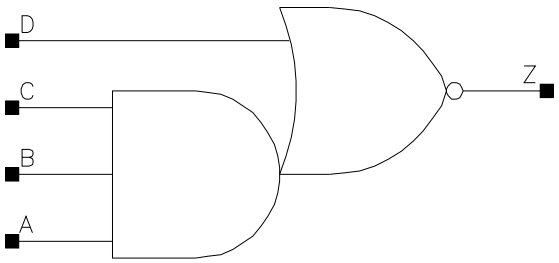
Pin Cycle (vdds)	X2_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X12_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X12_P10
A	0.0007	0.0025
B	0.0006	0.0024
C	0.0008	0.0023
D	0.0007	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X12_P10	X3_P10	X12_P10
A to Z ↓	0.0131	0.0137	6.3211	1.7942
A to Z ↑	0.0189	0.0181	7.0871	1.8527
B to Z ↓	0.0145	0.0142	6.3444	1.8002
B to Z ↑	0.0174	0.0159	7.1941	1.8540
C to Z ↓	0.0165	0.0146	6.3932	1.8096
C to Z ↑	0.0165	0.0130	7.2494	1.8684
D to Z ↓	0.0060	0.0051	2.9720	0.8022
D to Z ↑	0.0137	0.0120	6.2208	1.6071

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.928e-05	1.000e-20
X12_P10	6.717e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X12_P10
A (output stable)	1.371e-05	7.422e-05
B (output stable)	1.790e-05	1.213e-04
C (output stable)	4.059e-05	2.701e-04
D (output stable)	3.924e-04	1.316e-03
A to Z	2.092e-03	7.769e-03
B to Z	1.890e-03	6.650e-03
C to Z	1.731e-03	5.633e-03
D to Z	1.348e-03	4.624e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

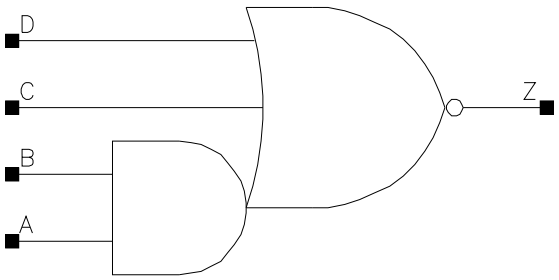
Pin Cycle (vdds)	X3_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X20_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P10	X20_P10
A	0.0006	0.0046
B	0.0006	0.0042
C	0.0007	0.0044
D	0.0007	0.0041

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X20_P10	X3_P10	X20_P10
A to Z ↓	0.0082	0.0092	4.5353	0.7351
A to Z ↑	0.0195	0.0182	10.1991	1.3270
B to Z ↓	0.0095	0.0101	4.6030	0.7471
B to Z ↑	0.0170	0.0146	10.3084	1.3287
C to Z ↓	0.0100	0.0146	2.9451	0.6096
C to Z ↑	0.0205	0.0191	9.7087	1.2540
D to Z ↓	0.0095	0.0132	2.9477	0.6092

D to Z ↑	0.0211	0.0182	9.7355	1.2591

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.636e-05	1.000e-20
X20_P10	1.041e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X20_P10
A (output stable)	8.633e-05	6.080e-04
B (output stable)	9.262e-05	6.566e-04
C (output stable)	3.884e-05	4.109e-04
D (output stable)	5.494e-05	6.082e-04
A to Z	1.457e-03	1.003e-02
B to Z	1.273e-03	8.256e-03
C to Z	2.113e-03	1.522e-02
D to Z	1.866e-03	1.244e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

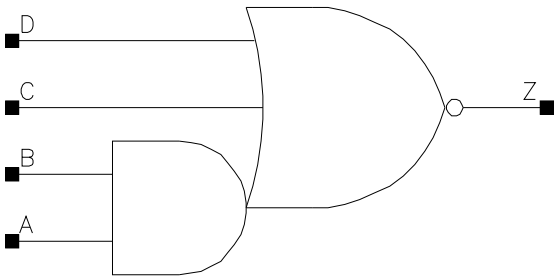
Pin Cycle (vdds)	X3_P10	X20_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.816	0.6528
X10_P10	0.800	2.448	1.9584
X19_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P10	X10_P10	X19_P10
A	0.0006	0.0024	0.0048
B	0.0006	0.0023	0.0046
C	0.0007	0.0021	0.0040
D	0.0005	0.0019	0.0037

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	X10_P10	X2_P10	X10_P10
A to Z ↓	0.0116	0.0120	5.3408	1.4223
A to Z ↑	0.0217	0.0201	10.8011	2.6518
B to Z ↓	0.0136	0.0132	5.4077	1.4379
B to Z ↑	0.0192	0.0167	10.8511	2.6626
C to Z ↓	0.0112	0.0104	4.8459	1.2158
C to Z ↑	0.0165	0.0148	10.2987	2.5249

D to Z ↓	0.0091	0.0075	4.8886	1.2301
D to Z ↑	0.0160	0.0135	10.3131	2.5312
	X19_P10		**X19_P10**	
A to Z ↓	0.0116		0.7296	
A to Z ↑	0.0195		1.3478	
B to Z ↓	0.0132		0.7386	
B to Z ↑	0.0161		1.3496	
C to Z ↓	0.0110		0.6585	
C to Z ↑	0.0141		1.2821	
D to Z ↓	0.0080		0.6665	
D to Z ↑	0.0128		1.2861	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P10	1.387e-05	1.000e-20
X10_P10	5.593e-05	1.000e-20
X19_P10	1.093e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P10	X10_P10	X19_P10
A (output stable)	1.832e-05	7.799e-05	1.528e-04
B (output stable)	1.909e-05	1.101e-04	2.097e-04
C (output stable)	5.410e-05	2.543e-04	4.936e-04
D (output stable)	1.302e-04	6.397e-04	1.198e-03
A to Z	1.979e-03	7.521e-03	1.443e-02
B to Z	1.787e-03	6.469e-03	1.247e-02
C to Z	1.313e-03	5.074e-03	9.581e-03
D to Z	1.100e-03	3.880e-03	7.254e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

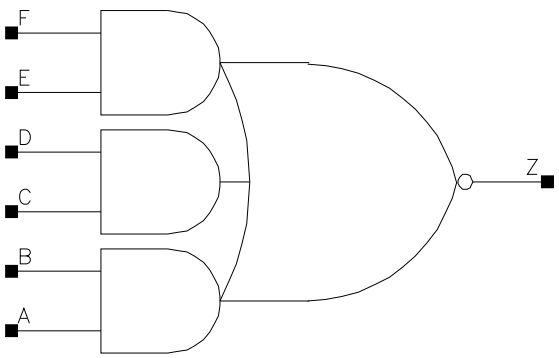
Pin Cycle (vdds)	X2_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.088	0.8704
X5_P10	0.800	2.040	1.6320
X7_P10	0.800	2.720	2.1760
X9_P10	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P10	X5_P10	X7_P10	X9_P10
A	0.0006	0.0011	0.0019	0.0024

B	0.0006	0.0013	0.0017	0.0022
C	0.0006	0.0011	0.0017	0.0025
D	0.0006	0.0012	0.0016	0.0022
E	0.0007	0.0012	0.0017	0.0022
F	0.0006	0.0010	0.0015	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X5_P10**	**X2_P10**	**X5_P10**
A to Z ↓	0.0130	0.0160	4.7839	2.7058
A to Z ↑	0.0284	0.0266	10.4621	4.7935
B to Z ↓	0.0151	0.0183	4.8433	2.7265
B to Z ↑	0.0257	0.0247	10.5170	4.7581
C to Z ↓	0.0118	0.0142	4.8074	2.6922
C to Z ↑	0.0252	0.0240	10.5393	4.8104
D to Z ↓	0.0137	0.0162	4.8828	2.7193
D to Z ↑	0.0225	0.0221	10.5331	4.7885
E to Z ↓	0.0086	0.0104	4.8464	2.6486
E to Z ↑	0.0213	0.0207	10.5330	4.7785
F to Z ↓	0.0097	0.0118	4.9382	2.6813
F to Z ↑	0.0179	0.0181	10.5045	4.8001
	X7_P10	**X9_P10**	**X7_P10**	**X9_P10**
A to Z ↓	0.0158	0.0163	1.8776	1.4291
A to Z ↑	0.0259	0.0265	3.1382	2.3651
B to Z ↓	0.0179	0.0181	1.8932	1.4406
B to Z ↑	0.0234	0.0236	3.2134	2.4062
C to Z ↓	0.0140	0.0148	1.8810	1.4202
C to Z ↑	0.0236	0.0247	3.2067	2.4078
D to Z ↓	0.0160	0.0158	1.9013	1.4353
D to Z ↑	0.0206	0.0209	3.1800	2.3892
E to Z ↓	0.0098	0.0099	1.8823	1.4254
E to Z ↑	0.0196	0.0197	3.1733	2.3962
F to Z ↓	0.0113	0.0108	1.9104	1.4473
F to Z ↑	0.0169	0.0164	3.2064	2.3946

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P10	2.263e-05	1.000e-20
X5_P10	4.762e-05	1.000e-20
X7_P10	6.941e-05	1.000e-20
X9_P10	9.002e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P10	X5_P10	X7_P10	X9_P10
A (output stable)	2.960e-05	5.616e-05	9.939e-05	1.382e-04
B (output stable)	3.461e-05	7.396e-05	1.432e-04	2.256e-04
C (output stable)	5.528e-05	1.043e-04	1.478e-04	2.145e-04
D (output stable)	6.309e-05	1.202e-04	2.017e-04	2.901e-04
E (output stable)	1.084e-04	2.384e-04	3.543e-04	5.088e-04
F (output stable)	1.282e-04	2.537e-04	4.021e-04	5.839e-04

A to Z	2.652e-03	5.433e-03	7.979e-03	1.083e-02
B to Z	2.431e-03	5.121e-03	7.235e-03	9.762e-03
C to Z	2.041e-03	4.280e-03	6.236e-03	8.442e-03
D to Z	1.839e-03	3.978e-03	5.567e-03	7.506e-03
E to Z	1.444e-03	3.220e-03	4.520e-03	5.975e-03
F to Z	1.262e-03	2.874e-03	3.900e-03	5.075e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

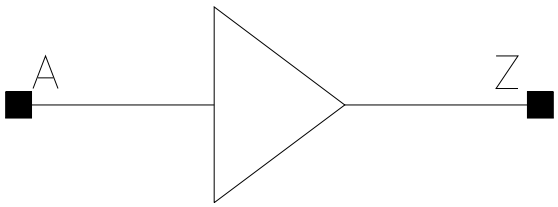
Pin Cycle (vdds)	X2_P10	X5_P10	X7_P10	X9_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.544	0.4352
X5_P10	0.800	0.544	0.4352
X9_P10	0.800	0.680	0.5440
X11_P10	1.600	0.408	0.6528
X13_P10	0.800	0.680	0.5440
X19_P10	0.800	0.952	0.7616
X23_P10	1.600	0.544	0.8704
X24_P10	0.800	1.088	0.8704
X29_P10	0.800	1.224	0.9792
X34_P10	1.600	0.680	1.0880
X38_P10	0.800	1.632	1.3056
X46_P10	1.600	0.952	1.5232
X57_P10	0.800	2.312	1.8496
X68_P10	1.600	1.224	1.9584
X91_P10	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P10	X5_P10	X9_P10	X11_P10
A	0.0006	0.0006	0.0006	0.0009
	X13_P10	X19_P10	X23_P10	X24_P10
A	0.0008	0.0011	0.0013	0.0013
	X29_P10	X34_P10	X38_P10	X46_P10
A	0.0015	0.0017	0.0022	0.0022
	X57_P10	X68_P10	X91_P10	
A	0.0030	0.0031	0.0041	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X5_P10**	**X2_P10**	**X5_P10**
A to Z ↓	0.0204	0.0213	5.2817	2.9380
A to Z ↑	0.0157	0.0161	7.4800	4.1134
	X9_P10	**X11_P10**	**X9_P10**	**X11_P10**
A to Z ↓	0.0260	0.0244	1.5035	1.1436
A to Z ↑	0.0199	0.0178	2.0502	1.9341
	X13_P10	**X19_P10**	**X13_P10**	**X19_P10**
A to Z ↓	0.0232	0.0232	1.0291	0.7277
A to Z ↑	0.0188	0.0175	1.4245	1.0014
	X23_P10	**X24_P10**	**X23_P10**	**X24_P10**
A to Z ↓	0.0234	0.0230	0.5531	0.5931
A to Z ↑	0.0174	0.0182	0.9749	0.8030
	X29_P10	**X34_P10**	**X29_P10**	**X34_P10**
A to Z ↓	0.0222	0.0233	0.4913	0.3796
A to Z ↑	0.0178	0.0176	0.6738	0.6659
	X38_P10	**X46_P10**	**X38_P10**	**X46_P10**
A to Z ↓	0.0217	0.0228	0.3717	0.2854
A to Z ↑	0.0176	0.0170	0.4969	0.5004
	X57_P10	**X68_P10**	**X57_P10**	**X68_P10**
A to Z ↓	0.0228	0.0225	0.2497	0.1933
A to Z ↑	0.0185	0.0171	0.3333	0.3350
	X91_P10		**X91_P10**	
A to Z ↓	0.0239		0.1491	
A to Z ↑	0.0180		0.2521	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P10	1.187e-05	1.000e-20
X5_P10	1.920e-05	1.000e-20
X9_P10	3.205e-05	1.000e-20
X11_P10	3.966e-05	1.000e-20
X13_P10	4.933e-05	1.000e-20
X19_P10	6.473e-05	1.000e-20
X23_P10	7.704e-05	1.000e-20
X24_P10	8.123e-05	1.000e-20
X29_P10	9.865e-05	1.000e-20
X34_P10	1.113e-04	1.000e-20
X38_P10	1.339e-04	1.000e-20
X46_P10	1.442e-04	1.000e-20
X57_P10	1.926e-04	1.000e-20
X68_P10	2.138e-04	1.000e-20
X91_P10	2.757e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P10	X5_P10	X9_P10	X11_P10
A to Z	1.614e-03	2.131e-03	3.631e-03	4.223e-03
	X13_P10	X19_P10	X23_P10	X24_P10
A to Z	5.213e-03	7.143e-03	7.896e-03	8.921e-03
	X29_P10	X34_P10	X38_P10	X46_P10

A to Z	1.043e-02	1.181e-02	1.427e-02	1.537e-02
	X57_P10	X68_P10	X91_P10	
A to Z	2.132e-02	2.258e-02	3.063e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

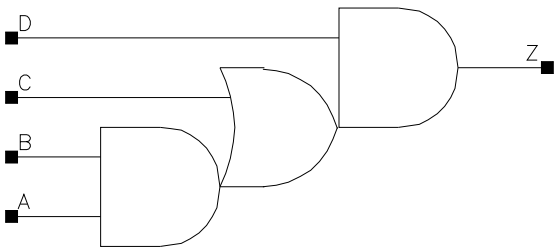
Pin Cycle (vdds)	X2_P10	X5_P10	X9_P10	X11_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P10	X19_P10	X23_P10	X24_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P10	X34_P10	X38_P10	X46_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P10	X68_P10	X91_P10	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.952	0.7616
X10_P10	0.800	1.632	1.3056
X14_P10	0.800	1.768	1.4144
X19_P10	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0007	0.0015	0.0015	0.0015
B	0.0007	0.0014	0.0014	0.0014
C	0.0007	0.0016	0.0016	0.0016
D	0.0011	0.0014	0.0015	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0267	0.0245	3.0002	1.4178
A to Z ↑	0.0263	0.0242	4.2249	2.0134
B to Z ↓	0.0246	0.0224	2.9915	1.4155
B to Z ↑	0.0275	0.0251	4.2206	2.0130
C to Z ↓	0.0239	0.0219	2.9864	1.4123
C to Z ↑	0.0199	0.0180	4.1847	1.9939

D to Z ↓	0.0237	0.0206	2.9631	1.4013
D to Z ↑	0.0221	0.0190	4.1910	1.9983
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0273	0.0297	0.9858	0.7403
A to Z ↑	0.0270	0.0294	1.3514	1.0150
B to Z ↓	0.0253	0.0279	0.9857	0.7389
B to Z ↑	0.0280	0.0305	1.3510	1.0138
C to Z ↓	0.0246	0.0272	0.9815	0.7365
C to Z ↑	0.0203	0.0223	1.3346	1.0010
D to Z ↓	0.0224	0.0240	0.9709	0.7264
D to Z ↑	0.0210	0.0228	1.3389	1.0034

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.145e-05	1.000e-20
X10_P10	6.352e-05	1.000e-20
X14_P10	7.697e-05	1.000e-20
X19_P10	9.044e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	4.791e-05	9.201e-05	9.378e-05	9.424e-05
B (output stable)	7.431e-05	1.419e-04	1.445e-04	1.444e-04
C (output stable)	2.176e-04	3.563e-04	3.586e-04	3.594e-04
D (output stable)	7.327e-05	1.152e-04	1.161e-04	1.164e-04
A to Z	3.418e-03	6.382e-03	8.290e-03	1.035e-02
B to Z	3.215e-03	5.919e-03	7.822e-03	9.873e-03
C to Z	2.817e-03	5.109e-03	6.821e-03	8.666e-03
D to Z	3.462e-03	6.315e-03	7.946e-03	9.632e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

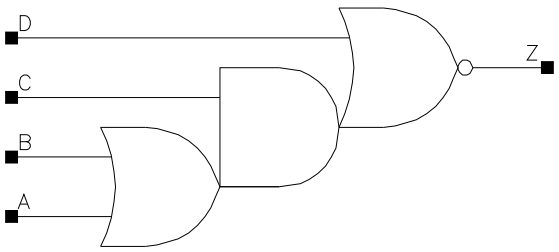
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X6_P10	0.800	1.496	1.1968
X9_P10	0.800	1.768	1.4144
X12_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X9_P10	X12_P10
A	0.0007	0.0013	0.0020	0.0025
B	0.0007	0.0012	0.0019	0.0024
C	0.0006	0.0012	0.0018	0.0024
D	0.0008	0.0012	0.0017	0.0024

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0119	0.0108	4.7121	2.4099
A to Z ↑	0.0223	0.0222	10.2275	5.4140
B to Z ↓	0.0111	0.0106	4.5734	2.4219
B to Z ↑	0.0227	0.0219	10.2431	5.4250
C to Z ↓	0.0113	0.0106	4.3863	2.2765
C to Z ↑	0.0143	0.0135	7.2567	3.7620

D to Z ↓	0.0059	0.0045	2.9936	1.5215
D to Z ↑	0.0150	0.0132	7.6606	3.9899
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0109	0.0114	1.6491	1.2861
A to Z ↑	0.0205	0.0218	3.4830	2.6871
B to Z ↓	0.0103	0.0106	1.6639	1.2859
B to Z ↑	0.0208	0.0213	3.4893	2.6927
C to Z ↓	0.0109	0.0111	1.5697	1.2125
C to Z ↑	0.0128	0.0131	2.4449	1.8604
D to Z ↓	0.0048	0.0047	1.0543	0.8070
D to Z ↑	0.0123	0.0122	2.5836	1.9746

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.938e-05	1.000e-20
X6_P10	3.738e-05	1.000e-20
X9_P10	5.269e-05	1.000e-20
X12_P10	6.972e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	1.518e-05	3.685e-05	4.561e-05	7.656e-05
B (output stable)	1.817e-05	4.371e-05	5.718e-05	1.032e-04
C (output stable)	6.026e-05	1.327e-04	1.797e-04	2.448e-04
D (output stable)	2.296e-04	5.925e-04	8.167e-04	1.235e-03
A to Z	2.135e-03	4.093e-03	5.757e-03	7.938e-03
B to Z	1.876e-03	3.433e-03	4.989e-03	6.680e-03
C to Z	1.608e-03	2.985e-03	4.306e-03	5.836e-03
D to Z	1.251e-03	2.215e-03	3.151e-03	4.137e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

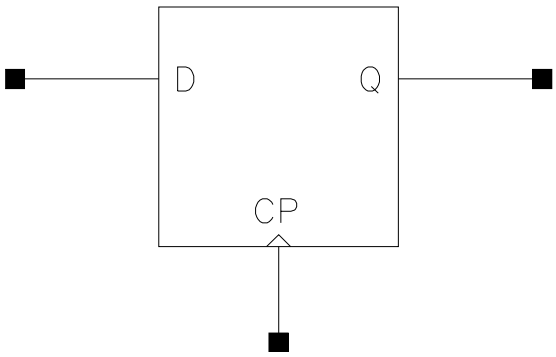
Pin Cycle (vdds)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	1.600	1.496	2.3936
X19_P10	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P10	X19_P10
CP	0.0009	0.0009
D	0.0008	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P10	X19_P10	X10_P10	X19_P10
CP to Q ↓	0.0421	0.0572	1.4668	0.7877
CP to Q ↑	0.0490	0.0570	1.9863	1.0191

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P10	X19_P10
CP ↓	min_pulse_width to CP	0.0398	0.0398
CP ↑	min_pulse_width to CP	0.0365	0.0505
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0170	0.0170
D ↑	setup_rising to CP	0.0146	0.0146

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P10	8.939e-05	1.000e-20
X19_P10	1.131e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

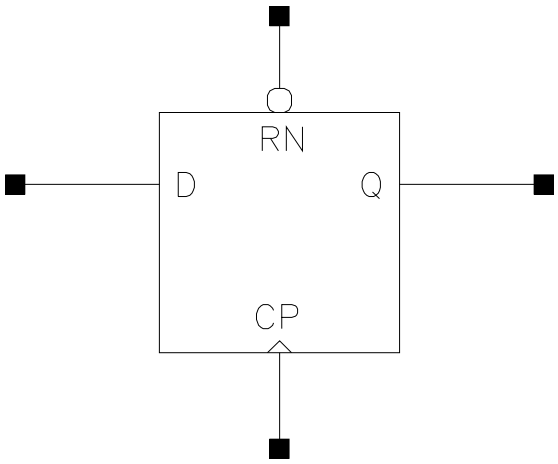
Pin Cycle	X10_P10	X19_P10
Clock 100Mhz Data 0Mhz	1.030e-02	1.031e-02
Clock 100Mhz Data 25Mhz	1.288e-02	1.622e-02
Clock 100Mhz Data 50Mhz	1.546e-02	2.213e-02
Clock = 0 Data 100Mhz	4.299e-03	4.299e-03
Clock = 1 Data 100Mhz	2.115e-05	2.118e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	1.600	1.768	2.8288
X19_P10	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P10	X19_P10
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0009	0.0009

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P10	X19_P10	X10_P10	X19_P10
CP to Q ↓	0.0454	0.0591	1.4876	0.7824
CP to Q ↑	0.0509	0.0587	1.9812	1.0127
RN to Q ↓	0.0440	0.0507	1.4199	0.7335

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P10	X19_P10
CP ↓	min_pulse_width to CP	0.0397	0.0397
CP ↑	min_pulse_width to CP	0.0364	0.0505
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0103	0.0103
D ↓	setup_rising to CP	0.0176	0.0176
D ↑	setup_rising to CP	0.0146	0.0146
RN ↓	min_pulse_width to RN	0.0566	0.0735
RN ↑	recovery_rising to CP	0.0081	0.0081
RN ↑	removal_rising to CP	-0.0033	-0.0033

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P10	1.039e-04	1.000e-20
X19_P10	1.336e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

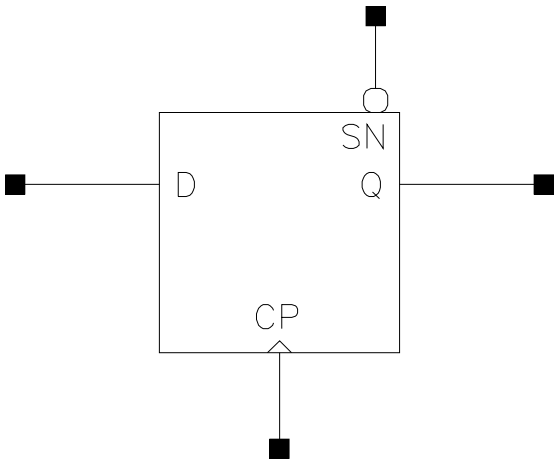
Pin Cycle	X10_P10	X19_P10
Clock 100Mhz Data 0Mhz	1.042e-02	1.042e-02
Clock 100Mhz Data 25Mhz	1.320e-02	1.653e-02
Clock 100Mhz Data 50Mhz	1.598e-02	2.263e-02
Clock = 0 Data 100Mhz	4.344e-03	4.344e-03
Clock = 1 Data 100Mhz	2.150e-05	2.162e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	1.600	1.768	2.8288
X19_P10	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P10	X19_P10
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0011	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P10	X19_P10	X10_P10	X19_P10
CP to Q ↓	0.0430	0.0577	1.4759	0.7767
CP to Q ↑	0.0504	0.0588	1.9799	1.0126
SN to Q ↑	0.0314	0.0338	1.9429	0.9827

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P10	X19_P10
CP ↓	min_pulse_width to CP	0.0398	0.0433
CP ↑	min_pulse_width to CP	0.0365	0.0505
D ↓	hold_rising to CP	0.0146	0.0146
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0198	0.0198
D ↑	setup_rising to CP	0.0146	0.0146
SN ↓	min_pulse_width to SN	0.0376	0.0376
SN ↑	recovery_rising to CP	-0.0017	-0.0022
SN ↑	removal_rising to CP	0.0232	0.0232

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P10	1.025e-04	1.000e-20
X19_P10	1.263e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

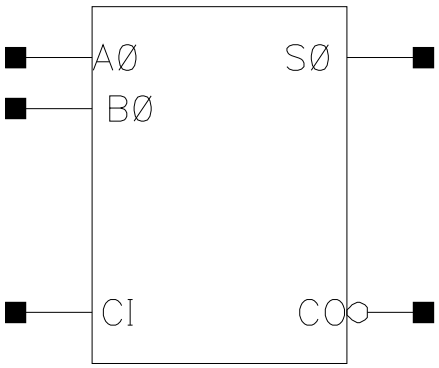
Pin Cycle	X10_P10	X19_P10
Clock 100Mhz Data 0Mhz	1.025e-02	1.026e-02
Clock 100Mhz Data 25Mhz	1.294e-02	1.636e-02
Clock 100Mhz Data 50Mhz	1.564e-02	2.247e-02
Clock = 0 Data 100Mhz	4.199e-03	4.200e-03
Clock = 1 Data 100Mhz	2.139e-05	2.157e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_-P10	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_-P10	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_-P10	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_-P10	1.600	2.720	4.3520
C8T28SOIDV_LLS1_-FA1X4_P10	1.600	2.040	3.2640
C8T28SOIDV_LLS1_-FA1X9_P10	1.600	3.128	5.0048
C8T28SOIDV_LLS1_-FA1X18_P10	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P10	C8T28SOIDV_LL_-FA1X9_P10	C8T28SOIDV_LL_-FA1X14_P10	C8T28SOIDV_LL_-FA1X19_P10
A0	0.0025	0.0027	0.0043	0.0046
B0	0.0022	0.0022	0.0039	0.0042
CI	0.0016	0.0016	0.0028	0.0031
	C8T28SOIDV_LLS1_-FA1X4_P10	C8T28SOIDV_LLS1_-FA1X9_P10	C8T28SOIDV_LLS1_-FA1X18_P10	
A0	0.0024	0.0033	0.0035	
B0	0.0023	0.0037	0.0041	
CI	0.0017	0.0025	0.0031	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P10	**C8T28SOIDV_LL_-FA1X9_P10**	**C8T28SOIDV_LL_-FA1X5_P10**	**C8T28SOIDV_LL_-FA1X9_P10**
A0 to CO ↓	0.0352	0.0382	3.0540	1.5617
A0 to CO ↑	0.0273	0.0298	3.9392	2.0138
A0 to S0 ↓	0.0386	0.0431	3.0016	1.5425
A0 to S0 ↑	0.0401	0.0441	3.9480	1.9786
B0 to CO ↓	0.0358	0.0391	3.0626	1.5677
B0 to CO ↑	0.0287	0.0312	3.9400	2.0160
B0 to S0 ↓	0.0394	0.0440	3.0026	1.5434
B0 to S0 ↑	0.0411	0.0453	3.9480	1.9793
CI to CO ↓	0.0349	0.0379	3.0631	1.5668
CI to CO ↑	0.0286	0.0312	3.9376	2.0126
CI to S0 ↓	0.0393	0.0440	3.0033	1.5435
CI to S0 ↑	0.0412	0.0454	3.9469	1.9789
	C8T28SOIDV_LL_-FA1X14_P10	**C8T28SOIDV_LL_-FA1X19_P10**	**C8T28SOIDV_LL_-FA1X14_P10**	**C8T28SOIDV_LL_-FA1X19_P10**
A0 to CO ↓	0.0362	0.0400	1.0194	0.7753
A0 to CO ↑	0.0282	0.0295	1.3831	1.0326
A0 to S0 ↓	0.0449	0.0459	1.0115	0.7518
A0 to S0 ↑	0.0464	0.0483	1.3345	0.9966
B0 to CO ↓	0.0362	0.0400	1.0227	0.7770
B0 to CO ↑	0.0290	0.0303	1.3826	1.0320
B0 to S0 ↓	0.0455	0.0465	1.0123	0.7521
B0 to S0 ↑	0.0471	0.0490	1.3354	0.9974
CI to CO ↓	0.0353	0.0390	1.0205	0.7749
CI to CO ↑	0.0289	0.0302	1.3816	1.0322
CI to S0 ↓	0.0452	0.0463	1.0123	0.7520
CI to S0 ↑	0.0468	0.0489	1.3348	0.9968
	C8T28SOIDV_-LLS1_FA1X4_P10	**C8T28SOIDV_-LLS1_FA1X9_P10**	**C8T28SOIDV_-LLS1_FA1X4_P10**	**C8T28SOIDV_-LLS1_FA1X9_P10**
A0 to CO ↓	0.0249	0.0222	5.4026	1.8444
A0 to CO ↑	0.0235	0.0214	3.9908	2.0096
A0 to S0 ↓	0.0519	0.0560	3.1964	1.1792
A0 to S0 ↑	0.0493	0.0481	4.1498	1.9685
B0 to CO ↓	0.0233	0.0235	5.3950	1.8471
B0 to CO ↑	0.0188	0.0198	3.9791	2.0081
B0 to S0 ↓	0.0518	0.0585	3.1956	1.1792
B0 to S0 ↑	0.0493	0.0506	4.1483	1.9681
CI to CO ↓	0.0242	0.0338	5.3919	1.8576
CI to CO ↑	0.0200	0.0185	3.9921	2.0238

CI to S0 ↓	0.0293	0.0354	3.1995	1.1816
CI to S0 ↑	0.0259	0.0268	4.1491	1.9680
	C8T28SOIDV_-LLS1_FA1X18_P10		**C8T28SOIDV_-LLS1_FA1X18_P10**	
A0 to CO ↓	0.0288		0.9736	
A0 to CO ↑	0.0223		0.9898	
A0 to S0 ↓	0.0603		0.6106	
A0 to S0 ↑	0.0493		0.9883	
B0 to CO ↓	0.0306		0.9748	
B0 to CO ↑	0.0208		0.9887	
B0 to S0 ↓	0.0619		0.6107	
B0 to S0 ↑	0.0510		0.9885	
CI to CO ↓	0.0427		0.9807	
CI to CO ↑	0.0227		0.9915	
CI to S0 ↓	0.0370		0.6114	
CI to S0 ↑	0.0251		0.9885	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P10	7.387e-05	1.000e-20
C8T28SOIDV_LL_FA1X9_P10	1.026e-04	1.000e-20
C8T28SOIDV_LL_FA1X14_P10	1.545e-04	1.000e-20
C8T28SOIDV_LL_FA1X19_P10	1.919e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P10	1.599e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P10	2.334e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P10	3.522e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P10	C8T28SOIDV_LL_-FA1X9_P10	C8T28SOIDV_LL_-FA1X14_P10	C8T28SOIDV_LL_-FA1X19_P10
A0 to CO	3.774e-03	5.665e-03	9.166e-03	1.151e-02
A0 to S0	3.832e-03	5.553e-03	9.351e-03	1.169e-02
B0 to CO	3.820e-03	5.756e-03	9.244e-03	1.164e-02
B0 to S0	3.800e-03	5.555e-03	9.311e-03	1.165e-02
CI to CO	3.853e-03	5.755e-03	9.385e-03	1.184e-02
CI to S0	3.782e-03	5.538e-03	9.290e-03	1.161e-02
	C8T28SOIDV_LLS1_-FA1X4_P10	C8T28SOIDV_LLS1_-FA1X9_P10	C8T28SOIDV_LLS1_-FA1X18_P10	
A0 to CO	5.701e-03	8.885e-03	1.447e-02	
A0 to S0	7.695e-03	1.144e-02	1.798e-02	
B0 to CO	6.013e-03	9.022e-03	1.461e-02	
B0 to S0	8.241e-03	1.174e-02	1.830e-02	
CI to CO	4.156e-03	7.477e-03	1.319e-02	
CI to S0	4.721e-03	8.345e-03	1.429e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P10	C8T28SOIDV_LL_-FA1X9_P10	C8T28SOIDV_LL_-FA1X14_P10	C8T28SOIDV_LL_-FA1X19_P10
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P10	C8T28SOIDV_LLS1_-FA1X9_P10	C8T28SOIDV_LLS1_-FA1X18_P10	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P10	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P10	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P10	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P10	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P10	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P10	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P10	C8T28SOI_LL_-HA1X9_P10	C8T28SOI_LLS1_-HA1X5_P10	C8T28SOIDV_LL_-HA1X14_P10
A0	0.0008	0.0012	0.0014	0.0018
B0	0.0007	0.0012	0.0013	0.0015
	C8T28SOIDV_LL_-HA1X19_P10	C8T28SOIDV_LLS1_-HA1X11_P10		
A0	0.0022	0.0021		
B0	0.0018	0.0021		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P10	**C8T28SOI_LL_-HA1X9_P10**	**C8T28SOI_LL_-HA1X5_P10**	**C8T28SOI_LL_-HA1X9_P10**
A0 to CO ↓	0.0287	0.0253	3.0173	1.4842
A0 to CO ↑	0.0259	0.0237	4.1857	2.0291
A0 to S0 ↓	0.0357	0.0336	2.8986	1.4677
A0 to S0 ↑	0.0346	0.0329	4.0737	2.0219
B0 to CO ↓	0.0280	0.0246	3.0175	1.4826
B0 to CO ↑	0.0285	0.0263	4.1872	2.0277
B0 to S0 ↓	0.0378	0.0353	2.8990	1.4681
B0 to S0 ↑	0.0340	0.0322	4.0719	2.0226
	C8T28SOI_LLS1_-HA1X5_P10	**C8T28SOIDV_LL_-HA1X14_P10**	**C8T28SOI_LLS1_-HA1X5_P10**	**C8T28SOIDV_LL_-HA1X14_P10**
A0 to CO ↓	0.0231	0.0263	2.9606	1.0171
A0 to CO ↑	0.0205	0.0233	4.1411	1.3625
A0 to S0 ↓	0.0304	0.0367	2.9551	1.0258
A0 to S0 ↑	0.0353	0.0360	4.1626	1.3401
B0 to CO ↓	0.0218	0.0243	2.9620	1.0135
B0 to CO ↑	0.0224	0.0247	4.1394	1.3624
B0 to S0 ↓	0.0325	0.0373	2.9544	1.0261
B0 to S0 ↑	0.0345	0.0343	4.1633	1.3415
	C8T28SOIDV_LL_-HA1X19_P10	**C8T28SOIDV_-LLS1_HA1X11_P10**	**C8T28SOIDV_LL_-HA1X19_P10**	**C8T28SOIDV_-LLS1_HA1X11_P10**
A0 to CO ↓	0.0246	0.0228	0.7517	1.0851
A0 to CO ↑	0.0227	0.0231	1.0326	1.9911
A0 to S0 ↓	0.0342	0.0285	0.7479	1.0990
A0 to S0 ↑	0.0336	0.0310	1.0070	2.0085
B0 to CO ↓	0.0228	0.0213	0.7496	1.0824
B0 to CO ↑	0.0242	0.0253	1.0326	1.9904
B0 to S0 ↓	0.0353	0.0293	0.7472	1.0984
B0 to S0 ↑	0.0321	0.0310	1.0070	2.0075

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_HA1X5_P10	4.331e-05	1.000e-20
C8T28SOI_LL_HA1X9_P10	9.435e-05	1.000e-20
C8T28SOI_LLS1_HA1X5_P10	5.346e-05	1.000e-20
C8T28SOIDV_LL_HA1X14_P10	1.350e-04	1.000e-20
C8T28SOIDV_LL_HA1X19_P10	1.860e-04	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P10	1.234e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

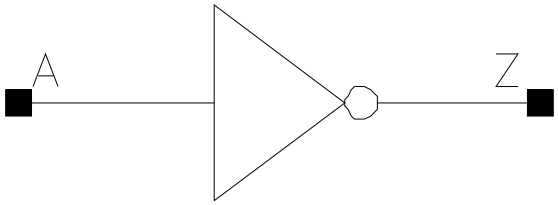
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P10	C8T28SOI_LL_-HA1X9_P10	C8T28SOI_LLS1_-HA1X5_P10	C8T28SOIDV_LL_-HA1X14_P10
A0 to CO	2.875e-03	4.842e-03	3.377e-03	7.692e-03
A0 to S0	2.649e-03	4.723e-03	3.048e-03	7.785e-03
B0 to CO	2.916e-03	5.016e-03	3.417e-03	7.744e-03
B0 to S0	2.615e-03	4.648e-03	2.970e-03	7.602e-03
	C8T28SOIDV_LL_-HA1X19_P10	C8T28SOIDV_LLS1_-HA1X11_P10		
A0 to CO	9.384e-03	6.651e-03		
A0 to S0	9.510e-03	6.073e-03		

B0 to CO	9.430e-03	6.142e-03		
B0 to S0	9.311e-03	6.183e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P10	C8T28SOI_LL_-HA1X9_P10	C8T28SOI_LLS1_-HA1X5_P10	C8T28SOIDV_LL_-HA1X14_P10
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P10	C8T28SOIDV_LLS1_-HA1X11_P10		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P10	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P10	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P10	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P10	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P10	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P10	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P10	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P10	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P10	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P10	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P10	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P10	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P10	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P10	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P10	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P10	C8T28SOI_LL_IVX3_-P10	C8T28SOI_LL_IVX5_-P10	C8T28SOI_LL_-IVX10_P10

A	0.0004	0.0005	0.0006	0.0012
	C8T28SOI_LL_-IVX14_P10	C8T28SOI_LL_-IVX19_P10	C8T28SOI_LL_-IVX29_P10	C8T28SOI_LL_-IVX34_P10
A	0.0019	0.0024	0.0036	0.0042
	C8T28SOI_LL_-IVX38_P10	C8T28SOIDV_LL_-IVX11_P10	C8T28SOIDV_LL_-IVX23_P10	C8T28SOIDV_LL_-IVX34_P10
A	0.0048	0.0013	0.0026	0.0039
	C8T28SOIDV_LL_-IVX46_P10	C8T28SOIDV_LL_-IVX68_P10	C8T28SOIDV_LL_-IVX91_P10	
A	0.0052	0.0079	0.0110	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P10	**C8T28SOI_LL_-IVX3_P10**	**C8T28SOI_LL_-IVX2_P10**	**C8T28SOI_LL_-IVX3_P10**
A to Z ↓	0.0054	0.0052	5.5238	4.3443
A to Z ↑	0.0108	0.0099	7.7165	5.9617
	C8T28SOI_LL_-IVX5_P10	**C8T28SOI_LL_-IVX10_P10**	**C8T28SOI_LL_-IVX5_P10**	**C8T28SOI_LL_-IVX10_P10**
A to Z ↓	0.0048	0.0037	3.0450	1.4641
A to Z ↑	0.0089	0.0075	4.2408	2.0226
	C8T28SOI_LL_-IVX14_P10	**C8T28SOI_LL_-IVX19_P10**	**C8T28SOI_LL_-IVX14_P10**	**C8T28SOI_LL_-IVX19_P10**
A to Z ↓	0.0040	0.0043	1.0150	0.7738
A to Z ↑	0.0074	0.0076	1.3594	1.0426
	C8T28SOI_LL_-IVX29_P10	**C8T28SOI_LL_-IVX34_P10**	**C8T28SOI_LL_-IVX29_P10**	**C8T28SOI_LL_-IVX34_P10**
A to Z ↓	0.0042	0.0040	0.5167	0.4403
A to Z ↑	0.0074	0.0071	0.6909	0.5900
	C8T28SOI_LL_-IVX38_P10	**C8T28SOIDV_LL_-IVX11_P10**	**C8T28SOI_LL_-IVX38_P10**	**C8T28SOIDV_LL_-IVX11_P10**
A to Z ↓	0.0042	0.0036	0.3908	1.1841
A to Z ↑	0.0073	0.0088	0.5228	2.0484
	C8T28SOIDV_LL_-IVX23_P10	**C8T28SOIDV_LL_-IVX34_P10**	**C8T28SOIDV_LL_-IVX23_P10**	**C8T28SOIDV_LL_-IVX34_P10**
A to Z ↓	0.0030	0.0033	0.5765	0.3945
A to Z ↑	0.0080	0.0081	0.9993	0.6706
	C8T28SOIDV_LL_-IVX46_P10	**C8T28SOIDV_LL_-IVX68_P10**	**C8T28SOIDV_LL_-IVX46_P10**	**C8T28SOIDV_LL_-IVX68_P10**
A to Z ↓	0.0032	0.0032	0.2969	0.2020
A to Z ↑	0.0078	0.0076	0.5031	0.3378
	C8T28SOIDV_LL_-IVX91_P10		**C8T28SOIDV_LL_-IVX91_P10**	
A to Z ↓	0.0037		0.1565	
A to Z ↑	0.0081		0.2568	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_IVX2_P10	6.184e-06	1.000e-20
C8T28SOI_LL_IVX3_P10	8.549e-06	1.000e-20
C8T28SOI_LL_IVX5_P10	1.286e-05	1.000e-20
C8T28SOI_LL_IVX10_P10	2.706e-05	1.000e-20

C8T28SOI_LL_IVX14_P10	3.897e-05	1.000e-20
C8T28SOI_LL_IVX19_P10	5.071e-05	1.000e-20
C8T28SOI_LL_IVX29_P10	7.416e-05	1.000e-20
C8T28SOI_LL_IVX34_P10	8.590e-05	1.000e-20
C8T28SOI_LL_IVX38_P10	9.764e-05	1.000e-20
C8T28SOIDV_LL_IVX11_P10	2.959e-05	1.000e-20
C8T28SOIDV_LL_IVX23_P10	5.955e-05	1.000e-20
C8T28SOIDV_LL_IVX34_P10	8.614e-05	1.000e-20
C8T28SOIDV_LL_IVX46_P10	1.122e-04	1.000e-20
C8T28SOIDV_LL_IVX68_P10	1.644e-04	1.000e-20
C8T28SOIDV_LL_IVX91_P10	2.166e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P10	C8T28SOI_LL_IVX3_-P10	C8T28SOI_LL_IVX5_-P10	C8T28SOI_LL_-IVX10_P10
A to Z	6.258e-04	7.823e-04	1.026e-03	2.005e-03
	C8T28SOI_LL_-IVX14_P10	C8T28SOI_LL_-IVX19_P10	C8T28SOI_LL_-IVX29_P10	C8T28SOI_LL_-IVX34_P10
A to Z	3.021e-03	4.033e-03	5.930e-03	6.813e-03
	C8T28SOI_LL_-IVX38_P10	C8T28SOIDV_LL_-IVX11_P10	C8T28SOIDV_LL_-IVX23_P10	C8T28SOIDV_LL_-IVX34_P10
A to Z	7.772e-03	2.267e-03	4.387e-03	6.579e-03
	C8T28SOIDV_LL_-IVX46_P10	C8T28SOIDV_LL_-IVX68_P10	C8T28SOIDV_LL_-IVX91_P10	
A to Z	8.497e-03	1.256e-02	1.691e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

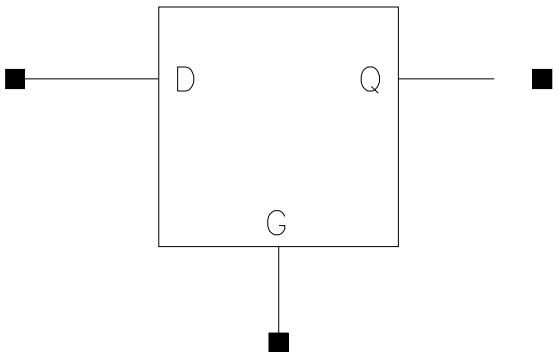
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P10	C8T28SOI_LL_IVX3_-P10	C8T28SOI_LL_IVX5_-P10	C8T28SOI_LL_-IVX10_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P10	C8T28SOI_LL_-IVX19_P10	C8T28SOI_LL_-IVX29_P10	C8T28SOI_LL_-IVX34_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P10	C8T28SOIDV_LL_-IVX11_P10	C8T28SOIDV_LL_-IVX23_P10	C8T28SOIDV_LL_-IVX34_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P10	C8T28SOIDV_LL_-IVX68_P10	C8T28SOIDV_LL_-IVX91_P10	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.360	1.0880
X9_P10	1.600	0.952	1.5232
X19_P10	1.600	1.224	1.9584
X28_P10	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10	X28_P10
D	0.0004	0.0007	0.0011	0.0018
G	0.0009	0.0009	0.0019	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D to Q ↓	0.0399	0.0388	3.0615	1.5765
D to Q ↑	0.0234	0.0280	4.0608	1.9864
G to Q ↓	0.0423	0.0413	3.0532	1.5734

G to Q ↑	0.0231	0.0265	4.0651	1.9859
	X19_P10	**X28_P10**	**X19_P10**	**X28_P10**
D to Q ↓	0.0316	0.0329	0.7557	0.5092
D to Q ↑	0.0250	0.0253	1.0009	0.6730
G to Q ↓	0.0356	0.0325	0.7541	0.5077
G to Q ↑	0.0228	0.0230	1.0014	0.6727

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P10	X9_P10	X19_P10	X28_P10
D ↓	hold_falling to G	-0.0023	-0.0017	0.0052	0.0058
D ↑	hold_falling to G	0.0088	0.0041	0.0068	0.0068
D ↓	setup_falling to G	0.0369	0.0370	0.0263	0.0295
D ↑	setup_falling to G	0.0264	0.0280	0.0280	0.0280
G ↑	min_pulse_width to G	0.0331	0.0366	0.0318	0.0318

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.372e-05	1.000e-20
X9_P10	5.392e-05	1.000e-20
X19_P10	9.177e-05	1.000e-20
X28_P10	1.247e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	1.104e-05	2.875e-05	3.388e-05	8.798e-05
G (output stable)	1.152e-03	1.394e-03	2.303e-03	2.272e-03
D to Q	4.578e-03	7.250e-03	1.113e-02	1.600e-02
G to Q	4.349e-03	6.905e-03	1.036e-02	1.421e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

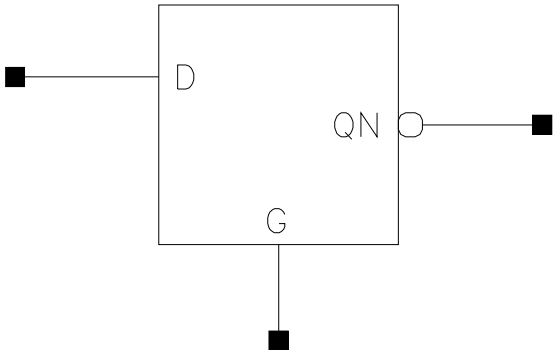
Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P10	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P10
D	0.0005
G	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P10	X10_P10
D to QN ↓	0.0359	1.4224
D to QN ↑	0.0475	1.9750
G to QN ↓	0.0352	1.4223
G to QN ↑	0.0498	1.9764

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P10
D ↓	hold_falling to G	-0.0094
D ↑	hold_falling to G	0.0014
D ↓	setup_falling to G	0.0370
D ↑	setup_falling to G	0.0232
G ↑	min_pulse_width to G	0.0330

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P10	5.082e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X10_P10
D (output stable)	1.092e-05
G (output stable)	1.307e-03
D to QN	5.875e-03
G to QN	5.665e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

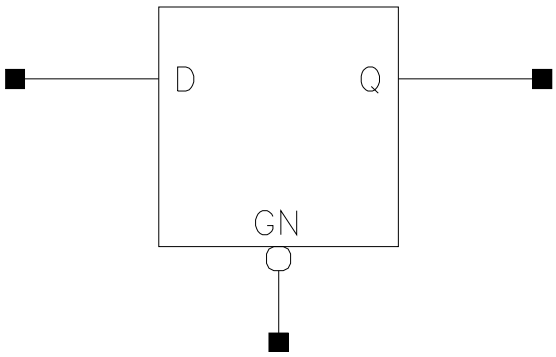
Pin Cycle (vdds)	X10_P10
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.360	1.0880
X9_P10	1.600	0.952	1.5232
X19_P10	1.600	1.224	1.9584
X28_P10	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10	X28_P10
D	0.0004	0.0008	0.0011	0.0016
GN	0.0009	0.0010	0.0014	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D to Q ↓	0.0403	0.0382	3.0645	1.5800
D to Q ↑	0.0235	0.0277	4.0593	1.9891
GN to Q ↓	0.0369	0.0369	3.0672	1.5813

GN to Q ↑	0.0405	0.0392	4.0567	1.9795
	X19_P10	**X28_P10**	**X19_P10**	**X28_P10**
D to Q ↓	0.0320	0.0318	0.7523	0.5083
D to Q ↑	0.0262	0.0259	0.9946	0.6653
GN to Q ↓	0.0287	0.0277	0.7530	0.5083
GN to Q ↑	0.0356	0.0355	0.9911	0.6647

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P10	X9_P10	X19_P10	X28_P10
D ↓	hold_rising to GN	-0.0046	-0.0030	0.0019	0.0019
D ↑	hold_rising to GN	0.0132	0.0074	0.0074	0.0106
D ↓	setup_rising to GN	0.0448	0.0401	0.0352	0.0352
D ↑	setup_rising to GN	0.0190	0.0239	0.0239	0.0243
GN ↓	min_pulse_width to GN	0.0505	0.0465	0.0393	0.0364

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.306e-05	1.000e-20
X9_P10	5.422e-05	1.000e-20
X19_P10	9.564e-05	1.000e-20
X28_P10	1.263e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	1.089e-05	1.740e-05	3.372e-05	7.607e-05
GN (output stable)	1.150e-03	1.382e-03	2.018e-03	2.168e-03
D to Q	4.587e-03	7.280e-03	1.146e-02	1.585e-02
GN to Q	6.596e-03	9.500e-03	1.423e-02	1.829e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

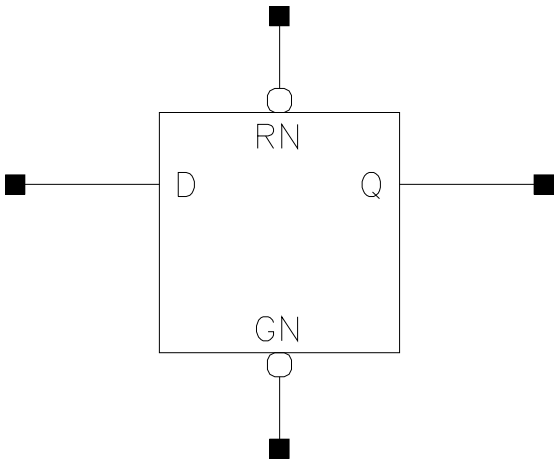
Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10	X28_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.632	1.3056
X9_P10	1.600	1.224	1.9584
X19_P10	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10
D	0.0004	0.0007	0.0013
GN	0.0011	0.0011	0.0016
RN	0.0005	0.0006	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D to Q ↓	0.0408	0.0396	3.0001	1.5327

D to Q ↑	0.0384	0.0424	4.1981	2.0535
GN to Q ↓	0.0383	0.0370	3.0032	1.5340
GN to Q ↑	0.0522	0.0497	4.1983	2.0548
RN to Q ↓	0.0343	0.0423	2.8454	1.4930
RN to Q ↑	0.0408	0.0447	4.1972	2.0569
	X19_P10		**X19_P10**	
D to Q ↓	0.0330		0.7580	
D to Q ↑	0.0461		1.0380	
GN to Q ↓	0.0300		0.7588	
GN to Q ↑	0.0482		1.0401	
RN to Q ↓	0.0525		0.7670	
RN to Q ↑	0.0508		1.0398	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P10	X9_P10	X19_P10
D ↓	hold_rising to GN	-0.0046	-0.0025	0.0025
D ↑	hold_rising to GN	0.0010	-0.0039	-0.0088
D ↓	setup_rising to GN	0.0445	0.0424	0.0354
D ↑	setup_rising to GN	0.0395	0.0443	0.0485
GN ↓	min_pulse_width to GN	0.0525	0.0495	0.0495
RN ↓	min_pulse_width to RN	0.0425	0.0518	0.0664
RN ↑	recovery_rising to GN	0.0422	0.0466	0.0563
RN ↑	removal_rising to GN	-0.0217	-0.0266	-0.0342

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.531e-05	1.000e-20
X9_P10	5.500e-05	1.000e-20
X19_P10	9.439e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10
D (output stable)	7.126e-05	6.430e-05	1.046e-04
GN (output stable)	1.277e-03	1.400e-03	1.815e-03
RN (output stable)	3.745e-05	4.898e-05	6.857e-05
D to Q	5.687e-03	8.253e-03	1.327e-02
GN to Q	7.861e-03	1.043e-02	1.583e-02
RN to Q	4.178e-03	6.184e-03	1.074e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

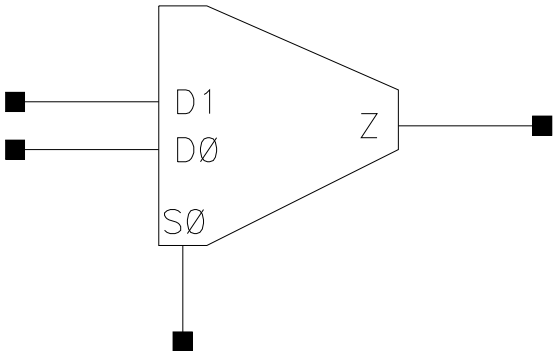
Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.360	1.0880
X9_P10	0.800	1.496	1.1968
X14_P10	0.800	2.176	1.7408
X19_P10	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P10	X9_P10	X14_P10	X19_P10
D0	0.0006	0.0008	0.0011	0.0014
D1	0.0005	0.0008	0.0011	0.0014
S0	0.0011	0.0011	0.0013	0.0017

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X9_P10	X5_P10	X9_P10
D0 to Z ↓	0.0300	0.0288	3.0390	1.5393
D0 to Z ↑	0.0242	0.0243	4.1524	2.1110
D1 to Z ↓	0.0304	0.0280	3.0329	1.5358
D1 to Z ↑	0.0240	0.0231	4.1552	2.1076
S0 to Z ↓	0.0283	0.0255	3.0273	1.5312
S0 to Z ↑	0.0272	0.0255	4.1533	2.1088

	X14_P10	X19_P10	X14_P10	X19_P10
D0 to Z ↓	0.0310	0.0276	1.0599	0.7657
D0 to Z ↑	0.0253	0.0237	1.4250	1.0355
D1 to Z ↓	0.0313	0.0283	1.0599	0.7662
D1 to Z ↑	0.0245	0.0232	1.4251	1.0346
S0 to Z ↓	0.0300	0.0280	1.0551	0.7642
S0 to Z ↑	0.0294	0.0272	1.4250	1.0344

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.982e-05	1.000e-20
X9_P10	6.755e-05	1.000e-20
X14_P10	9.069e-05	1.000e-20
X19_P10	1.328e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X9_P10	X14_P10	X19_P10
D0 (output stable)	9.099e-04	1.572e-03	1.894e-03	2.480e-03
D1 (output stable)	8.666e-04	1.385e-03	1.948e-03	2.577e-03
S0 (output stable)	1.229e-03	1.146e-03	1.729e-03	2.116e-03
D0 to Z	3.243e-03	5.316e-03	8.390e-03	1.048e-02
D1 to Z	3.186e-03	5.020e-03	8.205e-03	1.042e-02
S0 to Z	3.939e-03	5.266e-03	9.109e-03	1.119e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

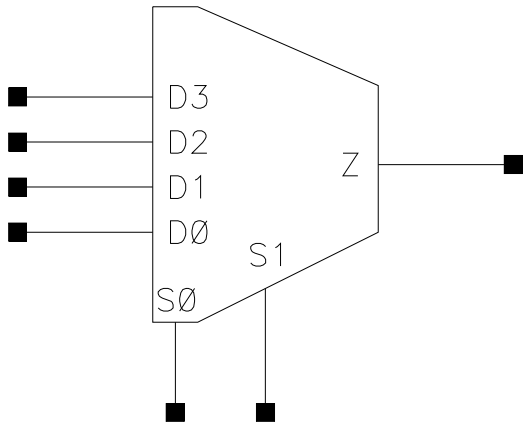
Pin Cycle (vdds)	X5_P10	X9_P10	X14_P10	X19_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.600	1.496	2.3936
X9_P10	1.600	1.768	2.8288
X13_P10	1.600	2.312	3.6992
X18_P10	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P10	X9_P10	X13_P10	X18_P10
D0	0.0005	0.0008	0.0011	0.0011
D1	0.0005	0.0006	0.0011	0.0011
D2	0.0004	0.0007	0.0011	0.0011
D3	0.0004	0.0006	0.0011	0.0011
S0	0.0014	0.0019	0.0026	0.0026
S1	0.0008	0.0009	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X9_P10	X4_P10	X9_P10
D0 to Z ↓	0.0628	0.0534	3.2995	1.6172
D0 to Z ↑	0.0410	0.0387	4.2677	2.1165
D1 to Z ↓	0.0620	0.0532	3.2940	1.6188
D1 to Z ↑	0.0409	0.0384	4.2576	2.1161
D2 to Z ↓	0.0573	0.0538	3.2506	1.6221
D2 to Z ↑	0.0394	0.0383	4.2432	2.1148
D3 to Z ↓	0.0579	0.0529	3.2578	1.6211
D3 to Z ↑	0.0401	0.0382	4.2417	2.1141
S0 to Z ↓	0.0656	0.0595	3.2757	1.6186
S0 to Z ↑	0.0488	0.0479	4.2628	2.1184
S1 to Z ↓	0.0431	0.0413	3.2698	1.6185
S1 to Z ↑	0.0378	0.0376	4.2546	2.1150
	X13_P10	X18_P10	X13_P10	X18_P10
D0 to Z ↓	0.0529	0.0578	1.1344	0.8489
D0 to Z ↑	0.0346	0.0377	1.4185	1.0723
D1 to Z ↓	0.0532	0.0581	1.1354	0.8497
D1 to Z ↑	0.0355	0.0386	1.4191	1.0721
D2 to Z ↓	0.0478	0.0521	1.1141	0.8337
D2 to Z ↑	0.0345	0.0375	1.4145	1.0700
D3 to Z ↓	0.0474	0.0517	1.1133	0.8328
D3 to Z ↑	0.0347	0.0377	1.4140	1.0695
S0 to Z ↓	0.0570	0.0616	1.1241	0.8414
S0 to Z ↑	0.0439	0.0470	1.4182	1.0724
S1 to Z ↓	0.0402	0.0448	1.1232	0.8408
S1 to Z ↑	0.0341	0.0372	1.4161	1.0710

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	3.969e-05	1.000e-20
X9_P10	6.317e-05	1.000e-20
X13_P10	1.068e-04	1.000e-20
X18_P10	1.196e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X9_P10	X13_P10	X18_P10
D0 (output stable)	5.032e-05	5.471e-05	1.110e-04	1.098e-04
D1 (output stable)	6.923e-05	7.164e-05	1.020e-04	1.016e-04
D2 (output stable)	6.795e-05	7.580e-05	1.023e-04	1.022e-04
D3 (output stable)	5.188e-05	7.233e-05	9.338e-05	9.308e-05
S0 (output stable)	1.561e-03	1.885e-03	3.125e-03	3.125e-03
S1 (output stable)	1.680e-03	1.952e-03	3.137e-03	3.139e-03
D0 to Z	4.241e-03	6.582e-03	1.042e-02	1.327e-02
D1 to Z	4.188e-03	6.564e-03	1.052e-02	1.338e-02
D2 to Z	3.974e-03	6.567e-03	9.890e-03	1.258e-02
D3 to Z	4.021e-03	6.561e-03	9.905e-03	1.257e-02
S0 to Z	5.927e-03	8.788e-03	1.382e-02	1.661e-02
S1 to Z	4.826e-03	7.302e-03	1.134e-02	1.408e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

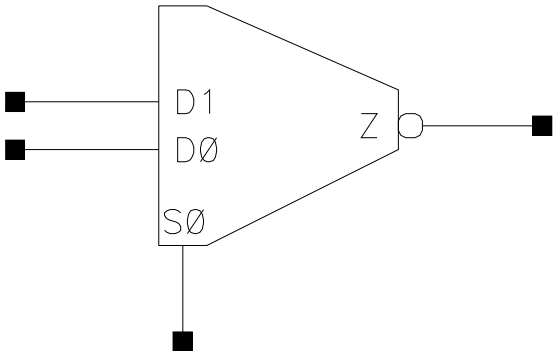
Pin Cycle (vdds)	X4_P10	X9_P10	X13_P10	X18_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P10	0.800	0.952	0.7616
X2_P10	0.800	0.952	0.7616
X6_P10	0.800	1.904	1.5232
X9_P10	0.800	2.448	1.9584
X12_P10	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P10	X2_P10	X6_P10	X9_P10
D0	0.0004	0.0006	0.0013	0.0019
D1	0.0004	0.0006	0.0012	0.0019
S0	0.0010	0.0014	0.0020	0.0029
	X12_P10			
D0	0.0025			
D1	0.0025			
S0	0.0033			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P10	X2_P10	X1_P10	X2_P10
D0 to Z ↓	0.0097	0.0094	7.8924	5.4536

D0 to Z ↑	0.0197	0.0155	15.6384	8.7138
D1 to Z ↓	0.0094	0.0090	7.8013	5.3305
D1 to Z ↑	0.0200	0.0158	15.6591	8.8744
S0 to Z ↓	0.0184	0.0134	7.8189	5.3908
S0 to Z ↑	0.0209	0.0144	15.5751	8.7670
	X6_P10	**X9_P10**	**X6_P10**	**X9_P10**
D0 to Z ↓	0.0108	0.0099	2.4713	1.6605
D0 to Z ↑	0.0161	0.0153	3.6718	2.5647
D1 to Z ↓	0.0103	0.0100	2.4217	1.6696
D1 to Z ↑	0.0171	0.0157	3.7932	2.5063
S0 to Z ↓	0.0161	0.0138	2.4420	1.6639
S0 to Z ↑	0.0169	0.0149	3.7229	2.5326
	X12_P10		**X12_P10**	
D0 to Z ↓	0.0103		1.2706	
D0 to Z ↑	0.0154		1.9347	
D1 to Z ↓	0.0099		1.2652	
D1 to Z ↑	0.0157		1.8883	
S0 to Z ↓	0.0149		1.2662	
S0 to Z ↑	0.0158		1.9098	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X1_P10	1.428e-05	1.000e-20
X2_P10	2.801e-05	1.000e-20
X6_P10	5.589e-05	1.000e-20
X9_P10	8.773e-05	1.000e-20
X12_P10	1.066e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X1_P10	X2_P10	X6_P10	X9_P10
D0 (output stable)	1.088e-05	2.354e-05	7.052e-05	1.016e-04
D1 (output stable)	1.053e-05	2.487e-05	7.672e-05	1.094e-04
S0 (output stable)	1.183e-03	1.472e-03	2.355e-03	3.813e-03
D0 to Z	1.013e-03	1.366e-03	3.496e-03	4.830e-03
D1 to Z	1.014e-03	1.351e-03	3.520e-03	4.898e-03
S0 to Z	2.010e-03	2.414e-03	4.845e-03	7.078e-03
	X12_P10			
D0 (output stable)	1.330e-04			
D1 (output stable)	1.373e-04			
S0 (output stable)	4.294e-03			
D0 to Z	6.504e-03			
D1 to Z	6.492e-03			
S0 to Z	8.740e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X1_P10	X2_P10	X6_P10	X9_P10
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

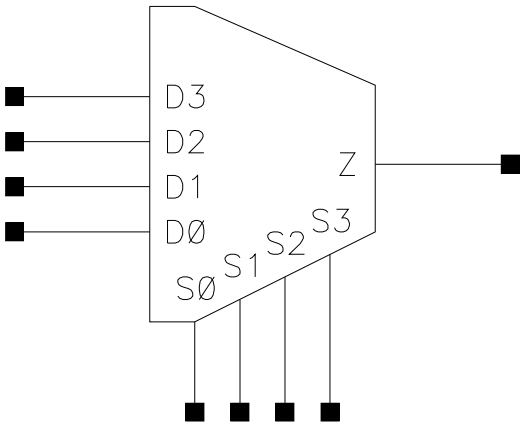
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P10			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.600	0.952	1.5232
X15_P10	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
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0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P10	X15_P10
D0	0.0006	0.0016
D1	0.0007	0.0013
D2	0.0007	0.0016
D3	0.0006	0.0014
S0	0.0006	0.0014
S1	0.0006	0.0016
S2	0.0007	0.0015
S3	0.0007	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X15_P10	X4_P10	X15_P10
D0 to Z ↓	0.0329	0.0356	4.6879	1.2351
D0 to Z ↑	0.0287	0.0282	3.9269	0.9959
D1 to Z ↓	0.0312	0.0333	4.6843	1.2340
D1 to Z ↑	0.0243	0.0242	3.9066	0.9901
D2 to Z ↓	0.0324	0.0350	4.6936	1.2360
D2 to Z ↑	0.0278	0.0267	3.9423	1.0005
D3 to Z ↓	0.0304	0.0329	4.6863	1.2335
D3 to Z ↑	0.0235	0.0231	3.9210	0.9951
S0 to Z ↓	0.0311	0.0324	4.6856	1.2336
S0 to Z ↑	0.0312	0.0294	3.9252	0.9953
S1 to Z ↓	0.0291	0.0306	4.6826	1.2326
S1 to Z ↑	0.0264	0.0255	3.9046	0.9895
S2 to Z ↓	0.0311	0.0320	4.6918	1.2340
S2 to Z ↑	0.0303	0.0282	3.9400	1.0004
S3 to Z ↓	0.0294	0.0302	4.6866	1.2320
S3 to Z ↑	0.0259	0.0243	3.9224	0.9944

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	4.899e-05	1.000e-20
X15_P10	1.426e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X15_P10
D0 (output stable)	5.385e-04	1.499e-03
D1 (output stable)	4.596e-04	1.268e-03
D2 (output stable)	5.228e-04	1.427e-03
D3 (output stable)	4.468e-04	1.201e-03
S0 (output stable)	5.112e-04	1.429e-03
S1 (output stable)	4.375e-04	1.235e-03
S2 (output stable)	5.047e-04	1.378e-03
S3 (output stable)	4.294e-04	1.179e-03
D0 to Z	4.105e-03	1.223e-02
D1 to Z	3.536e-03	1.067e-02
D2 to Z	3.807e-03	1.111e-02
D3 to Z	3.256e-03	9.591e-03
S0 to Z	3.946e-03	1.148e-02
S1 to Z	3.392e-03	1.005e-02
S2 to Z	3.678e-03	1.044e-02
S3 to Z	3.136e-03	8.933e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

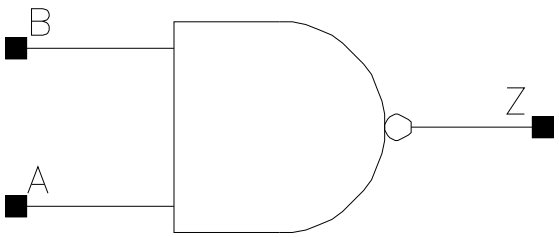
Pin Cycle (vdds)	X4_P10	X15_P10
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P10	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P10	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P10	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P10	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P10	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P10	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P10	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P10	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P10	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P10	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P10	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P10	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P10	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P10	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P10	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P10	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P10	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P10	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P10	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P10	C8T28SOI_LL_-NAND2X4_P10	C8T28SOI_LL_-NAND2X8_P10	C8T28SOI_LL_-NAND2X12_P10
A	0.0004	0.0006	0.0013	0.0019
B	0.0004	0.0006	0.0012	0.0017
	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X24_P10	C8T28SOI_-LLBR0P8_-NAND2X4_P10
A	0.0025	0.0031	0.0008	0.0007
B	0.0023	0.0028	0.0008	0.0006
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	C8T28SOI_-LLBR0P8_-NAND2X12_P10	C8T28SOI_-LLBR0P8_-NAND2X16_P10	C8T28SOI_LLS_-NAND2X8_P10
A	0.0013	0.0019	0.0025	0.0013
B	0.0011	0.0017	0.0022	0.0011
	C8T28SOI_LLS_-NAND2X15_P10	C8T28SOI_LLS_-NAND2X23_P10	C8T28SOI_LLS_-NAND2X31_P10	C8T28SOIDV_LL_-NAND2X9_P10
A	0.0025	0.0038	0.0050	0.0013
B	0.0023	0.0035	0.0047	0.0014
	C8T28SOIDV_LL_-NAND2X18_P10	C8T28SOIDV_LL_-NAND2X27_P10	C8T28SOIDV_LL_-NAND2X36_P10	
A	0.0026	0.0040	0.0053	
B	0.0025	0.0037	0.0050	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND2X2_P10	**C8T28SOI_LL_-NAND2X4_P10**	**C8T28SOI_LL_-NAND2X2_P10**	**C8T28SOI_LL_-NAND2X4_P10**
A to Z ↓	0.0074	0.0066	8.3974	4.7357
A to Z ↑	0.0125	0.0106	7.6616	4.2323
B to Z ↓	0.0090	0.0078	8.5003	4.7915
B to Z ↑	0.0112	0.0090	7.7154	4.2949
	C8T28SOI_LL_-NAND2X8_P10	**C8T28SOI_LL_-NAND2X12_P10**	**C8T28SOI_LL_-NAND2X8_P10**	**C8T28SOI_LL_-NAND2X12_P10**
A to Z ↓	0.0072	0.0069	2.4144	1.6509
A to Z ↑	0.0107	0.0104	2.0240	1.3808
B to Z ↓	0.0074	0.0079	2.4406	1.6704
B to Z ↑	0.0079	0.0081	2.0431	1.4017

	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10
A to Z ↓	0.0071	0.0070	1.2514	1.0105
A to Z ↑	0.0104	0.0104	1.0396	0.8414
B to Z ↓	0.0075	0.0079	1.2673	1.0237
B to Z ↑	0.0077	0.0080	1.0547	0.8548
	C8T28SOI_LL_-NAND2X24_P10	**C8T28SOI_-LLBR0P8_-NAND2X4_P10**	**C8T28SOI_LL_-NAND2X24_P10**	**C8T28SOI_-LLBR0P8_-NAND2X4_P10**
A to Z ↓	0.0303	0.0047	0.5936	3.4015
A to Z ↑	0.0316	0.0141	0.8209	5.2770
B to Z ↓	0.0320	0.0054	0.5938	3.4645
B to Z ↑	0.0300	0.0116	0.8215	5.3017
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	**C8T28SOI_-LLBR0P8_-NAND2X12_P10**	**C8T28SOI_-LLBR0P8_-NAND2X8_P10**	**C8T28SOI_-LLBR0P8_-NAND2X12_P10**
A to Z ↓	0.0052	0.0051	1.8717	1.2791
A to Z ↑	0.0141	0.0141	2.6578	1.8000
B to Z ↓	0.0047	0.0053	1.9077	1.3037
B to Z ↑	0.0102	0.0107	2.6810	1.8144
	C8T28SOI_-LLBR0P8_-NAND2X16_P10	**C8T28SOI_LLS_-NAND2X8_P10**	**C8T28SOI_-LLBR0P8_-NAND2X16_P10**	**C8T28SOI_LLS_-NAND2X8_P10**
A to Z ↓	0.0049	0.0072	0.9770	2.4062
A to Z ↑	0.0135	0.0108	1.3466	2.0502
B to Z ↓	0.0047	0.0074	0.9956	2.4334
B to Z ↑	0.0098	0.0080	1.3624	2.0807
	C8T28SOI_LLS_-NAND2X15_P10	**C8T28SOI_LLS_-NAND2X23_P10**	**C8T28SOI_LLS_-NAND2X15_P10**	**C8T28SOI_LLS_-NAND2X23_P10**
A to Z ↓	0.0071	0.0071	1.2484	0.8422
A to Z ↑	0.0104	0.0103	1.0232	0.6824
B to Z ↓	0.0076	0.0078	1.2641	0.8525
B to Z ↑	0.0077	0.0078	1.0334	0.6896
	C8T28SOI_LLS_-NAND2X31_P10	**C8T28SOIDV_LL_-NAND2X9_P10**	**C8T28SOI_LLS_-NAND2X31_P10**	**C8T28SOIDV_LL_-NAND2X9_P10**
A to Z ↓	0.0071	0.0061	0.6376	1.8846
A to Z ↑	0.0103	0.0113	0.5137	1.9762
B to Z ↓	0.0079	0.0070	0.6454	1.9098
B to Z ↑	0.0078	0.0093	0.5190	2.0141
	C8T28SOIDV_LL_-NAND2X18_P10	**C8T28SOIDV_LL_-NAND2X27_P10**	**C8T28SOIDV_LL_-NAND2X18_P10**	**C8T28SOIDV_LL_-NAND2X27_P10**
A to Z ↓	0.0065	0.0065	0.9601	0.6534
A to Z ↑	0.0116	0.0116	0.9942	0.6711
B to Z ↓	0.0065	0.0072	0.9728	0.6627
B to Z ↑	0.0086	0.0090	1.0016	0.6758
	C8T28SOIDV_LL_-NAND2X36_P10		**C8T28SOIDV_LL_-NAND2X36_P10**	
A to Z ↓	0.0065		0.4921	
A to Z ↑	0.0115		0.5026	
B to Z ↓	0.0067		0.4991	
B to Z ↑	0.0085		0.5067	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P10	6.358e-06	1.000e-20
C8T28SOI_LL_NAND2X4_P10	1.353e-05	1.000e-20
C8T28SOI_LL_NAND2X8_P10	2.726e-05	1.000e-20
C8T28SOI_LL_NAND2X12_P10	3.956e-05	1.000e-20
C8T28SOI_LL_NAND2X15_P10	5.190e-05	1.000e-20
C8T28SOI_LL_NAND2X19_P10	6.424e-05	1.000e-20
C8T28SOI_LL_NAND2X24_P10	9.344e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P10	1.331e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P10	2.433e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_-P10	3.497e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_-P10	4.565e-05	1.000e-20
C8T28SOI_LLS_NAND2X8_P10	2.726e-05	1.000e-20
C8T28SOI_LLS_NAND2X15_P10	5.190e-05	1.000e-20
C8T28SOI_LLS_NAND2X23_P10	7.658e-05	1.000e-20
C8T28SOI_LLS_NAND2X31_P10	1.013e-04	1.000e-20
C8T28SOIDV_LL_NAND2X9_P10	3.127e-05	1.000e-20
C8T28SOIDV_LL_NAND2X18_P10	6.012e-05	1.000e-20
C8T28SOIDV_LL_NAND2X27_P10	8.768e-05	1.000e-20
C8T28SOIDV_LL_NAND2X36_P10	1.153e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P10	C8T28SOI_LL_-NAND2X4_P10	C8T28SOI_LL_-NAND2X8_P10	C8T28SOI_LL_-NAND2X12_P10
A (output stable)	7.905e-06	1.416e-05	6.317e-05	7.932e-05
B (output stable)	1.684e-05	3.104e-05	2.027e-04	2.128e-04
A to Z	7.442e-04	1.206e-03	2.561e-03	3.731e-03
B to Z	6.479e-04	1.023e-03	2.020e-03	3.054e-03
	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X24_P10	C8T28SOI_-LLBR0P8_-NAND2X4_P10
A (output stable)	1.191e-04	1.298e-04	1.700e-05	1.963e-05
B (output stable)	3.513e-04	3.447e-04	3.501e-05	4.257e-05
A to Z	4.968e-03	6.153e-03	1.056e-02	1.303e-03
B to Z	3.954e-03	5.019e-03	1.039e-02	1.071e-03
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	C8T28SOI_-LLBR0P8_-NAND2X12_P10	C8T28SOI_-LLBR0P8_-NAND2X16_P10	C8T28SOI_LLS_-NAND2X8_P10
A (output stable)	7.601e-05	9.170e-05	1.425e-04	6.455e-05
B (output stable)	2.445e-04	2.533e-04	4.213e-04	2.123e-04
A to Z	2.606e-03	3.878e-03	4.954e-03	2.567e-03
B to Z	1.901e-03	2.975e-03	3.656e-03	2.024e-03
	C8T28SOI_LLS_-NAND2X15_P10	C8T28SOI_LLS_-NAND2X23_P10	C8T28SOI_LLS_-NAND2X31_P10	C8T28SOIDV_LL_-NAND2X9_P10
A (output stable)	1.225e-04	1.775e-04	2.273e-04	3.498e-05
B (output stable)	3.563e-04	4.986e-04	6.240e-04	7.761e-05
A to Z	5.010e-03	7.468e-03	9.906e-03	2.789e-03
B to Z	3.993e-03	5.996e-03	7.988e-03	2.351e-03
	C8T28SOIDV_LL_-NAND2X18_P10	C8T28SOIDV_LL_-NAND2X27_P10	C8T28SOIDV_LL_-NAND2X36_P10	
A (output stable)	1.349e-04	1.647e-04	2.749e-04	

B (output stable)	4.846e-04	4.180e-04	9.178e-04	
A to Z	5.665e-03	8.435e-03	1.114e-02	
B to Z	4.444e-03	6.904e-03	8.788e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

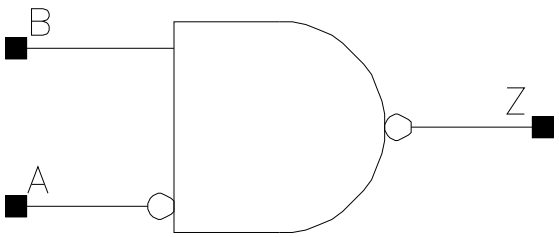
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P10	C8T28SOI_LL_-NAND2X4_P10	C8T28SOI_LL_-NAND2X8_P10	C8T28SOI_LL_-NAND2X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P10	C8T28SOI_LL_-NAND2X19_P10	C8T28SOI_LL_-NAND2X24_P10	C8T28SOI_-LLBR0P8_-NAND2X4_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P10	C8T28SOI_-LLBR0P8_-NAND2X12_P10	C8T28SOI_-LLBR0P8_-NAND2X16_P10	C8T28SOI_LLS_-NAND2X8_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P10	C8T28SOI_LLS_-NAND2X23_P10	C8T28SOI_LLS_-NAND2X31_P10	C8T28SOIDV_LL_-NAND2X9_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P10	C8T28SOIDV_LL_-NAND2X27_P10	C8T28SOIDV_LL_-NAND2X36_P10	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.544	0.4352
X4_P10	0.800	0.680	0.5440
X9_P10	1.600	0.544	0.8704
X13_P10	1.600	0.816	1.3056
X17_P10	1.600	0.816	1.3056
X23_P10	0.800	2.312	1.8496
X27_P10	1.600	1.088	1.7408
X31_P10	0.800	2.992	2.3936
X36_P10	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P10	X4_P10	X9_P10	X13_P10
A	0.0006	0.0006	0.0010	0.0010
B	0.0004	0.0006	0.0012	0.0020
	X17_P10	X23_P10	X27_P10	X31_P10
A	0.0010	0.0022	0.0017	0.0029
B	0.0024	0.0035	0.0038	0.0045
	X36_P10			
A	0.0017			
B	0.0049			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X4_P10**	**X2_P10**	**X4_P10**
A to Z ↓	0.0215	0.0225	8.3604	4.7609
A to Z ↑	0.0167	0.0173	7.4518	4.0902
B to Z ↓	0.0093	0.0079	8.5840	4.8840
B to Z ↑	0.0113	0.0089	7.7202	4.2921
	X9_P10	**X13_P10**	**X9_P10**	**X13_P10**
A to Z ↓	0.0229	0.0278	1.9164	1.2081
A to Z ↑	0.0172	0.0210	1.9399	1.2797
B to Z ↓	0.0072	0.0070	1.9750	1.2455
B to Z ↑	0.0093	0.0096	2.0263	1.3555
	X17_P10	**X23_P10**	**X17_P10**	**X23_P10**
A to Z ↓	0.0303	0.0219	0.9563	0.8345
A to Z ↑	0.0221	0.0178	0.9934	0.6787
B to Z ↓	0.0068	0.0076	0.9836	0.8577
B to Z ↑	0.0091	0.0078	1.0544	0.7088
	X27_P10	**X31_P10**	**X27_P10**	**X31_P10**
A to Z ↓	0.0255	0.0217	0.6458	0.6308
A to Z ↑	0.0198	0.0175	0.6608	0.4955
B to Z ↓	0.0068	0.0079	0.6658	0.6479
B to Z ↑	0.0087	0.0079	0.6790	0.5331
	X36_P10		**X36_P10**	
A to Z ↓	0.0295		0.4879	
A to Z ↑	0.0228		0.4962	
B to Z ↓	0.0067		0.5012	
B to Z ↑	0.0084		0.5098	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P10	1.167e-05	1.000e-20
X4_P10	1.960e-05	1.000e-20
X9_P10	4.600e-05	1.000e-20
X13_P10	5.625e-05	1.000e-20
X17_P10	7.208e-05	1.000e-20
X23_P10	1.149e-04	1.000e-20
X27_P10	1.156e-04	1.000e-20
X31_P10	1.513e-04	1.000e-20
X36_P10	1.438e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P10	X4_P10	X9_P10	X13_P10
A (output stable)	1.046e-03	1.291e-03	2.510e-03	3.474e-03
B (output stable)	1.691e-05	3.150e-05	8.080e-05	2.244e-04
A to Z	1.672e-03	2.270e-03	4.853e-03	7.574e-03
B to Z	6.463e-04	1.014e-03	2.357e-03	3.587e-03
	X17_P10	X23_P10	X27_P10	X31_P10
A (output stable)	3.870e-03	6.523e-03	6.234e-03	8.595e-03
B (output stable)	2.675e-04	4.467e-04	4.202e-04	5.853e-04
A to Z	9.175e-03	1.297e-02	1.344e-02	1.718e-02
B to Z	4.504e-03	5.983e-03	6.682e-03	7.952e-03
	X36_P10			
A (output stable)	7.919e-03			

B (output stable)	6.905e-04			
A to Z	1.807e-02			
B to Z	8.711e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

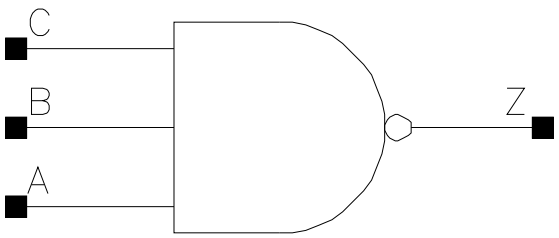
Pin Cycle (vdds)	X2_P10	X4_P10	X9_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P10	X23_P10	X27_P10	X31_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P10	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P10	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P10	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P10	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P10	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P10	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P10	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P10	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P10	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P10	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P10	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P10	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P10	C8T28SOI_LL_-NAND3X7_P10	C8T28SOI_LL_-NAND3X10_P10	C8T28SOI_LL_-NAND3X14_P10
A	0.0006	0.0012	0.0019	0.0025
B	0.0006	0.0012	0.0018	0.0023
C	0.0006	0.0011	0.0017	0.0023
	C8T28SOI_LL_-NAND3X20_P10	C8T28SOI_LL_-NAND3X27_P10	C8T28SOI_-LLBR0P6_-NAND3X3_P10	C8T28SOI_-LLBR0P6_-NAND3X7_P10
A	0.0037	0.0050	0.0008	0.0013
B	0.0035	0.0048	0.0006	0.0012
C	0.0033	0.0045	0.0006	0.0011
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	C8T28SOI_-LLBR0P6_-NAND3X14_P10	C8T28SOI_-LLBR0P6_-NAND3X20_P10	C8T28SOI_-LLBR0P6_-NAND3X27_P10
A	0.0019	0.0025	0.0037	0.0050
B	0.0017	0.0023	0.0034	0.0046
C	0.0017	0.0022	0.0033	0.0045

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-NAND3X3_P10	**C8T28SOI_LL_-NAND3X7_P10**	**C8T28SOI_LL_-NAND3X3_P10**	**C8T28SOI_LL_-NAND3X7_P10**
A to Z ↓	0.0101	0.0114	6.6874	3.4089
A to Z ↑	0.0131	0.0135	4.2831	2.1023
B to Z ↓	0.0111	0.0116	6.7171	3.4224
B to Z ↑	0.0118	0.0121	4.3085	2.1074
C to Z ↓	0.0119	0.0115	6.7608	3.4372
C to Z ↑	0.0103	0.0096	4.3518	2.0473
	C8T28SOI_LL_-NAND3X10_P10	**C8T28SOI_LL_-NAND3X14_P10**	**C8T28SOI_LL_-NAND3X10_P10**	**C8T28SOI_LL_-NAND3X14_P10**
A to Z ↓	0.0108	0.0111	2.3410	1.7742
A to Z ↑	0.0127	0.0130	1.3573	1.0605
B to Z ↓	0.0115	0.0114	2.3520	1.7813
B to Z ↑	0.0114	0.0115	1.4010	1.0601
C to Z ↓	0.0115	0.0114	2.3639	1.7905
C to Z ↑	0.0092	0.0092	1.4128	1.0532
	C8T28SOI_LL_-NAND3X20_P10	**C8T28SOI_LL_-NAND3X27_P10**	**C8T28SOI_LL_-NAND3X20_P10**	**C8T28SOI_LL_-NAND3X27_P10**
A to Z ↓	0.0107	0.0108	1.2053	0.9170
A to Z ↑	0.0125	0.0125	0.6843	0.5164
B to Z ↓	0.0115	0.0115	1.2107	0.9211
B to Z ↑	0.0112	0.0111	0.6844	0.5152
C to Z ↓	0.0115	0.0116	1.2169	0.9258
C to Z ↑	0.0089	0.0089	0.7047	0.5309
	C8T28SOI_-LLBR0P6_-NAND3X3_P10	**C8T28SOI_-LLBR0P6_-NAND3X7_P10**	**C8T28SOI_-LLBR0P6_-NAND3X3_P10**	**C8T28SOI_-LLBR0P6_-NAND3X7_P10**
A to Z ↓	0.0065	0.0084	4.2889	2.4258
A to Z ↑	0.0192	0.0204	6.1501	3.1392
B to Z ↓	0.0067	0.0080	4.3403	2.4476
B to Z ↑	0.0166	0.0175	6.1473	3.1500

C to Z ↓	0.0067	0.0069	4.4058	2.4772
C to Z ↑	0.0136	0.0133	6.2017	3.1231
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	**C8T28SOI_-LLBR0P6_-NAND3X14_P10**	**C8T28SOI_-LLBR0P6_-NAND3X10_P10**	**C8T28SOI_-LLBR0P6_-NAND3X14_P10**
A to Z ↓	0.0075	0.0081	1.6115	1.2287
A to Z ↑	0.0194	0.0198	2.0946	1.5880
B to Z ↓	0.0072	0.0073	1.6281	1.2408
B to Z ↑	0.0164	0.0168	2.1048	1.5915
C to Z ↓	0.0065	0.0063	1.6504	1.2577
C to Z ↑	0.0126	0.0124	2.1228	1.5906
	C8T28SOI_-LLBR0P6_-NAND3X20_P10	**C8T28SOI_-LLBR0P6_-NAND3X27_P10**	**C8T28SOI_-LLBR0P6_-NAND3X20_P10**	**C8T28SOI_-LLBR0P6_-NAND3X27_P10**
A to Z ↓	0.0076	0.0076	0.8292	0.6362
A to Z ↑	0.0194	0.0194	1.0569	0.7977
B to Z ↓	0.0073	0.0073	0.8378	0.6425
B to Z ↑	0.0165	0.0164	1.0585	0.7973
C to Z ↓	0.0063	0.0064	0.8493	0.6512
C to Z ↑	0.0121	0.0121	1.0671	0.8025

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P10	1.079e-05	1.000e-20
C8T28SOI_LL_NAND3X7_P10	2.254e-05	1.000e-20
C8T28SOI_LL_NAND3X10_P10	3.168e-05	1.000e-20
C8T28SOI_LL_NAND3X14_P10	4.257e-05	1.000e-20
C8T28SOI_LL_NAND3X20_P10	6.262e-05	1.000e-20
C8T28SOI_LL_NAND3X27_P10	8.262e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P10	1.055e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P10	2.046e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_-P10	2.783e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_-P10	3.775e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_-P10	5.507e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_-P10	7.231e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P10	C8T28SOI_LL_-NAND3X7_P10	C8T28SOI_LL_-NAND3X10_P10	C8T28SOI_LL_-NAND3X14_P10
A (output stable)	1.743e-05	6.753e-05	8.598e-05	1.275e-04
B (output stable)	2.685e-05	1.176e-04	1.615e-04	2.230e-04
C (output stable)	6.815e-05	3.474e-04	4.231e-04	6.401e-04
A to Z	1.540e-03	3.373e-03	4.772e-03	6.428e-03
B to Z	1.356e-03	2.857e-03	4.019e-03	5.419e-03
C to Z	1.185e-03	2.381e-03	3.372e-03	4.524e-03
	C8T28SOI_LL_-NAND3X20_P10	C8T28SOI_LL_-NAND3X27_P10	C8T28SOI_-LLBR0P6_-NAND3X3_P10	C8T28SOI_-LLBR0P6_-NAND3X7_P10

A (output stable)	1.739e-04	2.309e-04	2.744e-05	8.963e-05
B (output stable)	3.231e-04	4.337e-04	4.015e-05	1.477e-04
C (output stable)	9.466e-04	1.221e-03	1.074e-04	4.507e-04
A to Z	9.456e-03	1.252e-02	1.657e-03	3.650e-03
B to Z	7.970e-03	1.057e-02	1.369e-03	2.886e-03
C to Z	6.541e-03	8.705e-03	1.088e-03	2.155e-03
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	C8T28SOI_-LLBR0P6_-NAND3X14_P10	C8T28SOI_-LLBR0P6_-NAND3X20_P10	C8T28SOI_-LLBR0P6_-NAND3X27_P10
A (output stable)	1.153e-04	1.839e-04	2.379e-04	3.220e-04
B (output stable)	1.988e-04	3.094e-04	4.222e-04	5.628e-04
C (output stable)	5.557e-04	8.718e-04	1.241e-03	1.605e-03
A to Z	5.048e-03	6.941e-03	1.009e-02	1.333e-02
B to Z	3.915e-03	5.374e-03	7.815e-03	1.031e-02
C to Z	2.969e-03	3.936e-03	5.687e-03	7.543e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

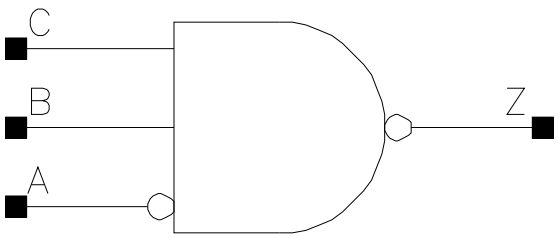
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P10	C8T28SOI_LL_-NAND3X7_P10	C8T28SOI_LL_-NAND3X10_P10	C8T28SOI_LL_-NAND3X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P10	C8T28SOI_LL_-NAND3X27_P10	C8T28SOI_-LLBR0P6_-NAND3X3_P10	C8T28SOI_-LLBR0P6_-NAND3X7_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P10	C8T28SOI_-LLBR0P6_-NAND3X14_P10	C8T28SOI_-LLBR0P6_-NAND3X20_P10	C8T28SOI_-LLBR0P6_-NAND3X27_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X7_P10	0.800	1.360	1.0880
X10_P10	0.800	1.632	1.3056
X14_P10	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X10_P10	X14_P10
A	0.0007	0.0010	0.0009	0.0009
B	0.0006	0.0012	0.0018	0.0024
C	0.0006	0.0011	0.0017	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0270	0.0268	6.6859	3.4151
A to Z ↑	0.0195	0.0205	4.0990	1.9861
B to Z ↓	0.0108	0.0114	6.7579	3.4480
B to Z ↑	0.0115	0.0116	4.3135	2.0524
C to Z ↓	0.0115	0.0111	6.8037	3.4619
C to Z ↑	0.0100	0.0091	4.3585	2.0518
	X10_P10	**X14_P10**	**X10_P10**	**X14_P10**
A to Z ↓	0.0297	0.0325	2.3302	1.7768

A to Z ↑	0.0230	0.0255	1.3584	1.0166
B to Z ↓	0.0114	0.0111	2.3501	1.7919
B to Z ↑	0.0113	0.0112	1.4026	1.0490
C to Z ↓	0.0114	0.0111	2.3612	1.8006
C to Z ↑	0.0092	0.0087	1.4156	1.0544

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.616e-05	1.000e-20
X7_P10	3.551e-05	1.000e-20
X10_P10	4.495e-05	1.000e-20
X14_P10	5.591e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	1.287e-03	2.408e-03	3.000e-03	3.615e-03
B (output stable)	2.765e-05	9.939e-05	1.696e-04	2.071e-04
C (output stable)	6.873e-05	3.566e-04	4.484e-04	6.156e-04
A to Z	2.615e-03	5.485e-03	7.635e-03	9.833e-03
B to Z	1.305e-03	2.760e-03	4.006e-03	5.271e-03
C to Z	1.133e-03	2.255e-03	3.356e-03	4.341e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

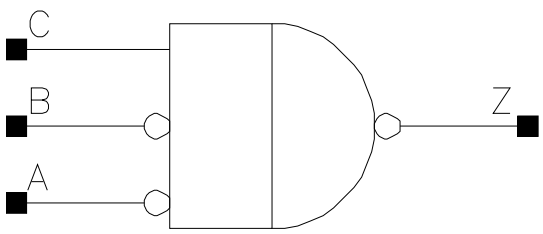
Pin Cycle (vdds)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	0.816	0.6528
X8_P10	0.800	1.088	0.8704
X12_P10	0.800	1.632	1.3056
X15_P10	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X12_P10	X15_P10
A	0.0007	0.0007	0.0014	0.0013
B	0.0008	0.0008	0.0014	0.0014
C	0.0006	0.0012	0.0017	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	**X8_P10**	**X4_P10**	**X8_P10**
A to Z ↓	0.0234	0.0290	4.4795	2.3896
A to Z ↑	0.0170	0.0200	3.9282	1.9629
B to Z ↓	0.0248	0.0306	4.4810	2.3891
B to Z ↑	0.0156	0.0188	3.9214	1.9612
C to Z ↓	0.0081	0.0075	4.5840	2.4354
C to Z ↑	0.0091	0.0081	3.9980	2.0613
	X12_P10	**X15_P10**	**X12_P10**	**X15_P10**
A to Z ↓	0.0263	0.0289	1.6300	1.2425
A to Z ↑	0.0183	0.0219	1.3105	0.9867
B to Z ↓	0.0264	0.0292	1.6296	1.2423

B to Z ↑	0.0162	0.0199	1.3078	0.9853
C to Z ↓	0.0082	0.0076	1.6647	1.2697
C to Z ↑	0.0085	0.0076	1.3995	1.0310

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	2.579e-05	1.000e-20
X8_P10	3.455e-05	1.000e-20
X12_P10	5.587e-05	1.000e-20
X15_P10	6.267e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	6.923e-04	9.152e-04	1.540e-03	1.733e-03
B (output stable)	6.336e-04	8.544e-04	1.417e-03	1.618e-03
C (output stable)	3.402e-05	2.041e-04	2.170e-04	3.377e-04
A to Z	3.131e-03	5.126e-03	7.995e-03	9.787e-03
B to Z	2.904e-03	4.901e-03	7.267e-03	9.101e-03
C to Z	1.124e-03	2.056e-03	3.199e-03	4.002e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

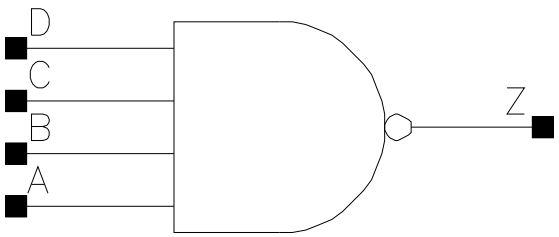
Pin Cycle (vdds)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.224	0.9792
X10_P10	0.800	1.360	1.0880
X14_P10	0.800	1.904	1.5232
X18_P10	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X18_P10
A	0.0005	0.0005	0.0006	0.0007
B	0.0006	0.0006	0.0006	0.0009
C	0.0005	0.0005	0.0006	0.0007
D	0.0005	0.0005	0.0006	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0377	0.0362	2.8531	1.4384
A to Z ↑	0.0326	0.0339	3.9619	2.0111
B to Z ↓	0.0397	0.0385	2.8533	1.4376
B to Z ↑	0.0313	0.0332	3.9615	2.0110
C to Z ↓	0.0391	0.0372	2.8541	1.4384
C to Z ↑	0.0338	0.0356	3.9596	2.0087

D to Z ↓	0.0417	0.0397	2.8521	1.4390
D to Z ↑	0.0331	0.0350	3.9545	2.0092
	X14_P10	**X18_P10**	**X14_P10**	**X18_P10**
A to Z ↓	0.0392	0.0371	0.9921	0.7987
A to Z ↑	0.0340	0.0337	1.3785	1.0827
B to Z ↓	0.0416	0.0391	0.9915	0.7981
B to Z ↑	0.0328	0.0327	1.3780	1.0830
C to Z ↓	0.0382	0.0345	0.9909	0.7972
C to Z ↑	0.0342	0.0330	1.3740	1.0803
D to Z ↓	0.0406	0.0364	0.9907	0.7972
D to Z ↑	0.0334	0.0316	1.3746	1.0810

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	2.682e-05	1.000e-20
X10_P10	4.161e-05	1.000e-20
X14_P10	5.910e-05	1.000e-20
X18_P10	7.804e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	5.111e-04	6.096e-04	8.908e-04	9.962e-04
B (output stable)	4.759e-04	5.708e-04	8.413e-04	9.433e-04
C (output stable)	5.371e-04	5.862e-04	8.757e-04	9.162e-04
D (output stable)	4.975e-04	5.482e-04	8.219e-04	8.537e-04
A to Z	3.740e-03	5.536e-03	8.481e-03	1.004e-02
B to Z	3.645e-03	5.438e-03	8.339e-03	9.900e-03
C to Z	3.906e-03	5.591e-03	8.083e-03	9.376e-03
D to Z	3.825e-03	5.502e-03	7.955e-03	9.212e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

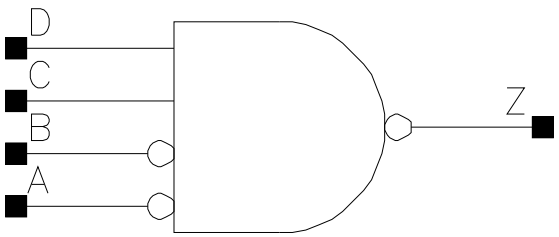
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.952	0.7616
X7_P10	0.800	1.360	1.0880
X10_P10	0.800	2.040	1.6320
X14_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P10	X7_P10	X10_P10	X14_P10
A	0.0008	0.0008	0.0015	0.0013
B	0.0008	0.0008	0.0015	0.0014
C	0.0008	0.0012	0.0018	0.0023
D	0.0006	0.0012	0.0017	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X7_P10	X3_P10	X7_P10
A to Z ↓	0.0269	0.0318	6.4525	3.4137
A to Z ↑	0.0185	0.0217	3.9755	1.9935
B to Z ↓	0.0280	0.0331	6.4542	3.4142
B to Z ↑	0.0170	0.0202	3.9742	1.9919
C to Z ↓	0.0112	0.0113	6.5235	3.4409
C to Z ↑	0.0119	0.0115	4.1392	2.0554

D to Z ↓	0.0115	0.0110	6.5550	3.4550
D to Z ↑	0.0100	0.0090	4.1357	2.0522
	X10_P10	**X14_P10**	**X10_P10**	**X14_P10**
A to Z ↓	0.0297	0.0325	2.3298	1.7830
A to Z ↑	0.0199	0.0251	1.3456	0.9954
B to Z ↓	0.0298	0.0329	2.3298	1.7824
B to Z ↑	0.0179	0.0232	1.3432	0.9938
C to Z ↓	0.0114	0.0112	2.3473	1.7947
C to Z ↑	0.0114	0.0112	1.4031	1.0507
D to Z ↓	0.0114	0.0112	2.3589	1.8034
D to Z ↑	0.0092	0.0088	1.4158	1.0564

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	2.302e-05	1.000e-20
X7_P10	2.972e-05	1.000e-20
X10_P10	4.955e-05	1.000e-20
X14_P10	5.377e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	8.589e-04	1.130e-03	1.986e-03	2.269e-03
B (output stable)	7.806e-04	1.052e-03	1.791e-03	2.083e-03
C (output stable)	5.550e-05	1.147e-04	1.799e-04	2.393e-04
D (output stable)	1.501e-04	4.094e-04	5.025e-04	7.176e-04
A to Z	3.556e-03	5.769e-03	9.071e-03	1.145e-02
B to Z	3.344e-03	5.563e-03	8.365e-03	1.078e-02
C to Z	1.397e-03	2.747e-03	3.984e-03	5.269e-03
D to Z	1.227e-03	2.245e-03	3.339e-03	4.356e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

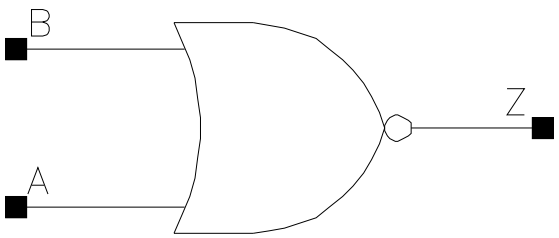
Pin Cycle (vdds)	X3_P10	X7_P10	X10_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.408	0.3264
X4_P10	0.800	0.408	0.3264
X8_P10	0.800	0.680	0.5440
X9_P10	1.600	0.408	0.6528
X12_P10	0.800	0.952	0.7616
X16_P10	0.800	1.224	0.9792
X19_P10	1.600	0.680	1.0880
X20_P10	0.800	1.496	1.1968
X23_P10	0.800	1.496	1.1968
X24_P10	0.800	1.768	1.4144
X27_P10	0.800	1.632	1.3056
X29_P10	1.600	0.952	1.5232
X31_P10	0.800	2.312	1.8496
X34_P10	0.800	2.040	1.6320
X38_P10	0.800	2.176	1.7408
X39_P10	1.600	1.224	1.9584
X46_P10	1.600	1.224	1.9584
X57_P10	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P10	X4_P10	X8_P10	X9_P10
A	0.0004	0.0006	0.0013	0.0013
B	0.0004	0.0006	0.0011	0.0013
	X12_P10	X16_P10	X19_P10	X20_P10

A	0.0019	0.0025	0.0027	0.0032
B	0.0017	0.0023	0.0025	0.0028
	X23_P10	X24_P10	X27_P10	X29_P10
A	0.0008	0.0037	0.0008	0.0040
B	0.0007	0.0034	0.0007	0.0038
	X31_P10	X34_P10	X38_P10	X39_P10
A	0.0050	0.0008	0.0008	0.0054
B	0.0047	0.0008	0.0008	0.0049
	X46_P10	X57_P10		
A	0.0008	0.0008		
B	0.0009	0.0009		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X4_P10**	**X2_P10**	**X4_P10**
A to Z ↓	0.0071	0.0069	5.5059	3.0782
A to Z ↑	0.0136	0.0123	13.7597	7.6928
B to Z ↓	0.0058	0.0053	5.5509	3.1060
B to Z ↑	0.0149	0.0132	13.8232	7.7236
	X8_P10	**X9_P10**	**X8_P10**	**X9_P10**
A to Z ↓	0.0064	0.0057	1.4840	1.1964
A to Z ↑	0.0113	0.0116	3.6737	3.4912
B to Z ↓	0.0038	0.0042	1.4890	1.2385
B to Z ↑	0.0107	0.0124	3.6882	3.5072
	X12_P10	**X16_P10**	**X12_P10**	**X16_P10**
A to Z ↓	0.0066	0.0066	1.0153	0.7555
A to Z ↑	0.0109	0.0112	2.4089	1.8429
B to Z ↓	0.0044	0.0042	1.0261	0.7641
B to Z ↑	0.0110	0.0108	2.4216	1.8513
	X19_P10	**X20_P10**	**X19_P10**	**X20_P10**
A to Z ↓	0.0062	0.0068	0.6017	0.6199
A to Z ↑	0.0126	0.0109	1.7913	1.4638
B to Z ↓	0.0043	0.0045	0.6085	0.6268
B to Z ↑	0.0124	0.0110	1.7971	1.4711
	X23_P10	**X24_P10**	**X23_P10**	**X24_P10**
A to Z ↓	0.0281	0.0066	0.6216	0.5135
A to Z ↑	0.0368	0.0110	0.8252	1.2346
B to Z ↓	0.0264	0.0042	0.6215	0.5197
B to Z ↑	0.0380	0.0107	0.8255	1.2407
	X27_P10	**X29_P10**	**X27_P10**	**X29_P10**
A to Z ↓	0.0295	0.0059	0.5184	0.3982
A to Z ↑	0.0381	0.0119	0.6892	1.2034
B to Z ↓	0.0278	0.0040	0.5183	0.4021
B to Z ↑	0.0393	0.0121	0.6894	1.2074
	X31_P10	**X34_P10**	**X31_P10**	**X34_P10**
A to Z ↓	0.0068	0.0312	0.3831	0.4252
A to Z ↑	0.0111	0.0431	0.9259	0.5671
B to Z ↓	0.0045	0.0295	0.3881	0.4253
B to Z ↑	0.0109	0.0446	0.9305	0.5672
	X38_P10	**X39_P10**	**X38_P10**	**X39_P10**
A to Z ↓	0.0318	0.0061	0.3705	0.3032
A to Z ↑	0.0436	0.0121	0.4969	0.9031

B to Z ↓	0.0301	0.0041	0.3703	0.3071
B to Z ↑	0.0450	0.0120	0.4974	0.9063
	X46_P10	**X57_P10**	**X46_P10**	**X57_P10**
A to Z ↓	0.0357	0.0387	0.2862	0.2340
A to Z ↑	0.0448	0.0472	0.4923	0.3968
B to Z ↓	0.0343	0.0373	0.2861	0.2341
B to Z ↑	0.0469	0.0493	0.4925	0.3967

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P10	6.374e-06	1.000e-20
X4_P10	1.337e-05	1.000e-20
X8_P10	2.820e-05	1.000e-20
X9_P10	3.186e-05	1.000e-20
X12_P10	4.105e-05	1.000e-20
X16_P10	5.392e-05	1.000e-20
X19_P10	6.151e-05	1.000e-20
X20_P10	6.680e-05	1.000e-20
X23_P10	1.035e-04	1.000e-20
X24_P10	7.968e-05	1.000e-20
X27_P10	1.175e-04	1.000e-20
X29_P10	8.997e-05	1.000e-20
X31_P10	1.054e-04	1.000e-20
X34_P10	1.466e-04	1.000e-20
X38_P10	1.607e-04	1.000e-20
X39_P10	1.185e-04	1.000e-20
X46_P10	1.653e-04	1.000e-20
X57_P10	1.954e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P10	X4_P10	X8_P10	X9_P10
A (output stable)	1.345e-05	2.293e-05	8.657e-05	5.023e-05
B (output stable)	2.462e-05	4.341e-05	2.409e-04	9.939e-05
A to Z	7.408e-04	1.250e-03	2.504e-03	2.675e-03
B to Z	6.273e-04	1.041e-03	1.875e-03	2.223e-03
	X12_P10	X16_P10	X19_P10	X20_P10
A (output stable)	1.208e-04	1.732e-04	1.844e-04	2.000e-04
B (output stable)	2.989e-04	4.466e-04	5.548e-04	4.613e-04
A to Z	3.730e-03	4.982e-03	5.600e-03	6.200e-03
B to Z	2.897e-03	3.776e-03	4.431e-03	4.803e-03
	X23_P10	X24_P10	X27_P10	X29_P10
A (output stable)	2.510e-05	2.523e-04	2.490e-05	2.340e-04
B (output stable)	4.804e-05	6.183e-04	4.824e-05	5.796e-04
A to Z	1.047e-02	7.379e-03	1.196e-02	8.019e-03
B to Z	1.027e-02	5.632e-03	1.176e-02	6.418e-03
	X31_P10	X34_P10	X38_P10	X39_P10
A (output stable)	3.388e-04	2.657e-05	2.675e-05	3.572e-04
B (output stable)	8.312e-04	5.144e-05	5.145e-05	9.542e-04
A to Z	9.874e-03	1.593e-02	1.732e-02	1.078e-02
B to Z	7.571e-03	1.569e-02	1.708e-02	8.492e-03
	X46_P10	X57_P10		

A (output stable)	2.719e-05	2.816e-05		
B (output stable)	5.295e-05	5.362e-05		
A to Z	1.914e-02	2.390e-02		
B to Z	1.894e-02	2.370e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

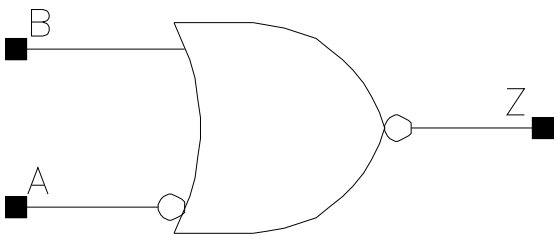
Pin Cycle (vdds)	X2_P10	X4_P10	X8_P10	X9_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P10	X16_P10	X19_P10	X20_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P10	X24_P10	X27_P10	X29_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P10	X34_P10	X38_P10	X39_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P10	X57_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	0.544	0.4352
X3_P10	0.800	0.544	0.4352
X4_P10	0.800	0.544	0.4352
X10_P10	1.600	0.544	0.8704
X14_P10	1.600	0.816	1.3056
X19_P10	1.600	0.816	1.3056
X29_P10	1.600	1.088	1.7408
X39_P10	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P10	X3_P10	X4_P10	X10_P10
A	0.0006	0.0006	0.0006	0.0010
B	0.0004	0.0005	0.0005	0.0013
	X14_P10	X19_P10	X29_P10	X39_P10
A	0.0010	0.0010	0.0017	0.0017
B	0.0020	0.0024	0.0037	0.0049

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X3_P10**	**X2_P10**	**X3_P10**
A to Z ↓	0.0208	0.0210	5.2790	4.0536
A to Z ↑	0.0186	0.0186	13.6713	11.6841
B to Z ↓	0.0056	0.0047	5.5842	4.2692

B to Z ↑	0.0143	0.0139	13.8169	11.7867
	X4_P10	**X10_P10**	**X4_P10**	**X10_P10**
A to Z ↓	0.0217	0.0223	3.1480	1.1557
A to Z ↑	0.0188	0.0187	8.6060	3.4416
B to Z ↓	0.0046	0.0043	3.3084	1.1815
B to Z ↑	0.0126	0.0127	8.6898	3.4734
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0269	0.0287	0.7288	0.5701
A to Z ↑	0.0218	0.0228	2.3120	1.7314
B to Z ↓	0.0039	0.0038	0.8131	0.6368
B to Z ↑	0.0120	0.0112	2.3368	1.7490
	X29_P10	**X39_P10**	**X29_P10**	**X39_P10**
A to Z ↓	0.0247	0.0286	0.3834	0.2879
A to Z ↑	0.0216	0.0236	1.2008	0.8830
B to Z ↓	0.0040	0.0037	0.4032	0.3150
B to Z ↑	0.0120	0.0111	1.2124	0.8916

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P10	1.187e-05	1.000e-20
X3_P10	1.376e-05	1.000e-20
X4_P10	1.775e-05	1.000e-20
X10_P10	4.740e-05	1.000e-20
X14_P10	5.715e-05	1.000e-20
X19_P10	7.648e-05	1.000e-20
X29_P10	1.180e-04	1.000e-20
X39_P10	1.481e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P10	X3_P10	X4_P10	X10_P10
A (output stable)	1.048e-03	1.126e-03	1.245e-03	2.564e-03
B (output stable)	2.459e-05	2.873e-05	3.943e-05	1.035e-04
A to Z	1.690e-03	1.854e-03	2.150e-03	4.908e-03
B to Z	5.995e-04	6.947e-04	8.726e-04	2.305e-03
	X14_P10	X19_P10	X29_P10	X39_P10
A (output stable)	3.597e-03	4.037e-03	6.293e-03	7.988e-03
B (output stable)	1.554e-04	2.074e-04	5.637e-04	3.940e-04
A to Z	7.204e-03	8.773e-03	1.360e-02	1.745e-02
B to Z	3.198e-03	4.061e-03	6.369e-03	7.999e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X2_P10	X3_P10	X4_P10	X10_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P10	X19_P10	X29_P10	X39_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

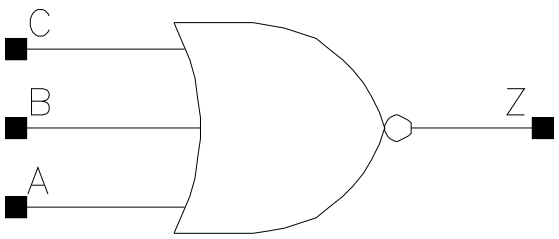
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.544	0.4352
X7_P10	0.800	0.952	0.7616
X11_P10	0.800	1.360	1.0880
X14_P10	0.800	1.768	1.4144
X21_P10	0.800	2.584	2.0672
X29_P10	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X11_P10	X14_P10
A	0.0006	0.0011	0.0019	0.0025
B	0.0006	0.0013	0.0018	0.0026
C	0.0006	0.0011	0.0017	0.0023
	X21_P10	X29_P10		
A	0.0039	0.0052		
B	0.0038	0.0051		
C	0.0034	0.0045		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0079	0.0081	3.1310	1.6326
A to Z ↑	0.0155	0.0158	10.5011	5.4355

B to Z ↓	0.0073	0.0071	3.1537	1.5762
B to Z ↑	0.0156	0.0160	10.5214	5.4486
C to Z ↓	0.0058	0.0047	3.1990	1.5966
C to Z ↑	0.0157	0.0136	10.5413	5.4448
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0080	0.0081	1.0273	0.7866
A to Z ↑	0.0162	0.0157	3.6030	2.6128
B to Z ↓	0.0073	0.0072	1.0355	0.7667
B to Z ↑	0.0155	0.0157	3.6096	2.6188
C to Z ↓	0.0052	0.0049	1.0369	0.7808
C to Z ↑	0.0148	0.0138	3.6115	2.6191
	X21_P10	**X29_P10**	**X21_P10**	**X29_P10**
A to Z ↓	0.0080	0.0082	0.5236	0.3932
A to Z ↑	0.0156	0.0157	1.7553	1.3206
B to Z ↓	0.0072	0.0073	0.5152	0.3893
B to Z ↑	0.0155	0.0155	1.7588	1.3231
C to Z ↓	0.0051	0.0052	0.5257	0.3968
C to Z ↑	0.0139	0.0140	1.7592	1.3237

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.163e-05	1.000e-20
X7_P10	2.278e-05	1.000e-20
X11_P10	3.481e-05	1.000e-20
X14_P10	4.702e-05	1.000e-20
X21_P10	6.947e-05	1.000e-20
X29_P10	9.219e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	2.799e-05	6.583e-05	1.180e-04	1.365e-04
B (output stable)	3.319e-05	9.519e-05	1.358e-04	1.895e-04
C (output stable)	9.071e-05	3.105e-04	3.820e-04	6.172e-04
A to Z	1.493e-03	2.982e-03	4.698e-03	6.173e-03
B to Z	1.270e-03	2.557e-03	3.784e-03	5.281e-03
C to Z	1.057e-03	1.883e-03	3.073e-03	3.949e-03
	X21_P10	X29_P10		
A (output stable)	2.031e-04	2.680e-04		
B (output stable)	2.778e-04	3.722e-04		
C (output stable)	8.802e-04	1.176e-03		
A to Z	9.173e-03	1.223e-02		
B to Z	7.790e-03	1.038e-02		
C to Z	5.894e-03	7.858e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

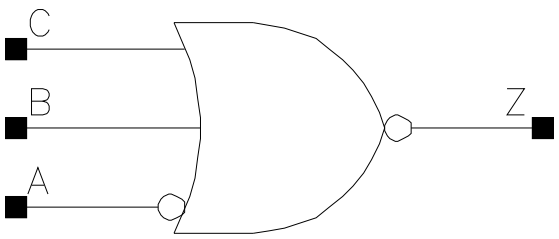
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P10	X29_P10		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X7_P10	0.800	1.360	1.0880
X11_P10	0.800	1.632	1.3056
X14_P10	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X11_P10	X14_P10
A	0.0007	0.0008	0.0010	0.0015
B	0.0006	0.0012	0.0018	0.0023
C	0.0006	0.0012	0.0017	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X7_P10**	**X3_P10**	**X7_P10**
A to Z ↓	0.0234	0.0218	2.9827	1.4103
A to Z ↑	0.0248	0.0254	10.5397	5.1775
B to Z ↓	0.0073	0.0072	3.1645	1.5006
B to Z ↑	0.0155	0.0160	10.5933	5.2041
C to Z ↓	0.0058	0.0049	3.2044	1.5131
C to Z ↑	0.0157	0.0142	10.6139	5.2031
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0264	0.0211	0.9903	0.7330

A to Z ↑	0.0286	0.0249	3.6070	2.6555
B to Z ↓	0.0072	0.0071	1.0366	0.7755
B to Z ↑	0.0153	0.0153	3.6237	2.6704
C to Z ↓	0.0050	0.0049	1.0388	0.7847
C to Z ↑	0.0145	0.0140	3.6252	2.6708

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.759e-05	1.000e-20
X7_P10	3.894e-05	1.000e-20
X11_P10	4.761e-05	1.000e-20
X14_P10	7.198e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	1.324e-03	2.364e-03	3.028e-03	4.401e-03
B (output stable)	3.459e-05	1.116e-04	1.428e-04	2.121e-04
C (output stable)	9.123e-05	3.434e-04	3.876e-04	6.079e-04
A to Z	2.720e-03	5.658e-03	7.628e-03	1.065e-02
B to Z	1.257e-03	2.688e-03	3.768e-03	5.100e-03
C to Z	1.048e-03	2.054e-03	3.021e-03	3.924e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

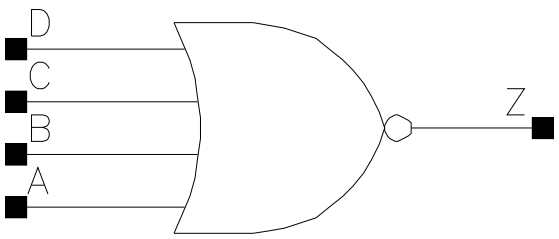
Pin Cycle (vdds)	X3_P10	X7_P10	X11_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	1.224	0.9792
X10_P10	0.800	1.632	1.3056
X14_P10	0.800	1.904	1.5232
X18_P10	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X18_P10
A	0.0005	0.0005	0.0006	0.0007
B	0.0006	0.0007	0.0007	0.0008
C	0.0005	0.0005	0.0006	0.0007
D	0.0006	0.0005	0.0006	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0254	0.0300	2.9565	1.4206
A to Z ↑	0.0401	0.0453	4.1579	2.0072
B to Z ↓	0.0244	0.0298	2.9576	1.4209
B to Z ↑	0.0419	0.0485	4.1578	2.0082
C to Z ↓	0.0259	0.0305	2.9556	1.4176
C to Z ↑	0.0428	0.0490	4.1568	2.0043

D to Z ↓	0.0254	0.0292	2.9512	1.4180
D to Z ↑	0.0451	0.0506	4.1480	2.0049
	X14_P10	**X18_P10**	**X14_P10**	**X18_P10**
A to Z ↓	0.0293	0.0310	0.9789	0.7733
A to Z ↑	0.0422	0.0414	1.3835	1.0363
B to Z ↓	0.0286	0.0297	0.9784	0.7728
B to Z ↑	0.0445	0.0429	1.3828	1.0353
C to Z ↓	0.0285	0.0309	0.9750	0.7698
C to Z ↑	0.0425	0.0422	1.3823	1.0349
D to Z ↓	0.0274	0.0294	0.9735	0.7706
D to Z ↑	0.0443	0.0436	1.3811	1.0353

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.425e-05	1.000e-20
X10_P10	5.272e-05	1.000e-20
X14_P10	7.877e-05	1.000e-20
X18_P10	1.035e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	5.425e-04	6.737e-04	8.627e-04	1.069e-03
B (output stable)	5.007e-04	6.392e-04	8.099e-04	9.904e-04
C (output stable)	5.632e-04	6.323e-04	8.412e-04	1.050e-03
D (output stable)	5.221e-04	5.912e-04	7.815e-04	9.688e-04
A to Z	3.658e-03	5.920e-03	8.371e-03	1.066e-02
B to Z	3.544e-03	5.817e-03	8.223e-03	1.047e-02
C to Z	3.751e-03	5.791e-03	7.881e-03	1.009e-02
D to Z	3.658e-03	5.684e-03	7.735e-03	9.877e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

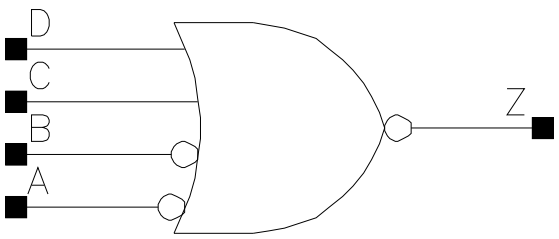
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	1.224	0.9792
X7_P10	0.800	1.496	1.1968
X11_P10	0.800	2.040	1.6320
X14_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P10	X7_P10	X11_P10	X14_P10
A	0.0008	0.0008	0.0015	0.0015
B	0.0008	0.0008	0.0015	0.0015
C	0.0006	0.0012	0.0017	0.0024
D	0.0006	0.0011	0.0017	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X7_P10	X4_P10	X7_P10
A to Z ↓	0.0237	0.0251	2.7766	1.4332
A to Z ↑	0.0302	0.0302	10.1539	5.2585
B to Z ↓	0.0217	0.0231	2.7730	1.4315
B to Z ↑	0.0312	0.0313	10.1596	5.2606
C to Z ↓	0.0075	0.0072	2.8999	1.5127
C to Z ↑	0.0165	0.0159	10.1843	5.2864

D to Z ↓	0.0060	0.0049	2.9226	1.5134
D to Z ↑	0.0165	0.0143	10.1951	5.2859
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0227	0.0250	0.9794	0.7364
A to Z ↑	0.0280	0.0306	3.5597	2.6462
B to Z ↓	0.0204	0.0230	0.9771	0.7350
B to Z ↑	0.0288	0.0320	3.5605	2.6458
C to Z ↓	0.0073	0.0073	1.0359	0.7732
C to Z ↑	0.0152	0.0154	3.5737	2.6567
D to Z ↓	0.0051	0.0050	1.0391	0.7775
D to Z ↑	0.0145	0.0141	3.5766	2.6573

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	2.543e-05	1.000e-20
X7_P10	3.469e-05	1.000e-20
X11_P10	5.610e-05	1.000e-20
X14_P10	6.520e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X7_P10	X11_P10	X14_P10
A (output stable)	1.035e-03	1.208e-03	1.995e-03	2.353e-03
B (output stable)	9.666e-04	1.140e-03	1.830e-03	2.213e-03
C (output stable)	7.355e-05	1.134e-04	1.661e-04	2.366e-04
D (output stable)	1.542e-04	3.535e-04	4.475e-04	6.874e-04
A to Z	4.320e-03	5.984e-03	9.244e-03	1.194e-02
B to Z	4.036e-03	5.705e-03	8.648e-03	1.137e-02
C to Z	1.402e-03	2.649e-03	3.788e-03	5.145e-03
D to Z	1.193e-03	2.041e-03	3.045e-03	3.993e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

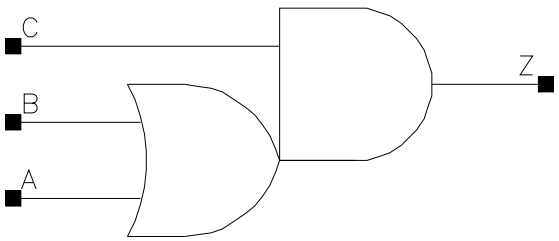
Pin Cycle (vdds)	X4_P10	X7_P10	X11_P10	X14_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.680	0.5440
X10_P10	0.800	0.952	0.7616
X19_P10	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10
A	0.0007	0.0007	0.0013
B	0.0007	0.0008	0.0016
C	0.0008	0.0009	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0219	0.0254	2.8535	1.4277
A to Z ↑	0.0194	0.0236	4.5470	2.0074
B to Z ↓	0.0233	0.0269	2.8558	1.4278
B to Z ↑	0.0175	0.0214	4.5417	2.0049
C to Z ↓	0.0214	0.0235	2.8217	1.4094
C to Z ↑	0.0177	0.0210	4.5450	2.0061
	X19_P10		**X19_P10**	
A to Z ↓	0.0264		0.7411	
A to Z ↑	0.0247		1.0265	

B to Z ↓	0.0279		0.7418	
B to Z ↑	0.0223		1.0240	
C to Z ↓	0.0237		0.7298	
C to Z ↑	0.0213		1.0241	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	2.741e-05	1.000e-20
X10_P10	4.658e-05	1.000e-20
X19_P10	8.885e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X19_P10
A (output stable)	4.931e-05	5.042e-05	1.065e-04
B (output stable)	5.814e-05	6.128e-05	1.222e-04
C (output stable)	4.384e-05	4.531e-05	8.801e-05
A to Z	2.614e-03	4.541e-03	9.199e-03
B to Z	2.416e-03	4.292e-03	8.712e-03
C to Z	2.863e-03	4.629e-03	9.214e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

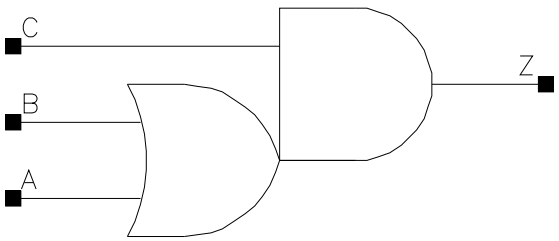
Pin Cycle (vdds)	X5_P10	X10_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X10_P10	0.800	1.360	1.0880
X14_P10	0.800	1.496	1.1968
X19_P10	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0007	0.0015	0.0015	0.0015
B	0.0007	0.0014	0.0014	0.0014
C	0.0008	0.0014	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0272	0.0228	2.8011	1.4168
A to Z ↑	0.0193	0.0178	3.9835	1.9556
B to Z ↓	0.0288	0.0240	2.8030	1.4178
B to Z ↑	0.0176	0.0161	3.9816	1.9520
C to Z ↓	0.0194	0.0160	2.7493	1.3973
C to Z ↑	0.0184	0.0167	3.9763	1.9505
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0256	0.0281	0.9862	0.7423

A to Z ↑	0.0199	0.0216	1.3245	0.9933
B to Z ↓	0.0270	0.0296	0.9862	0.7428
B to Z ↑	0.0183	0.0202	1.3233	0.9940
C to Z ↓	0.0182	0.0200	0.9673	0.7270
C to Z ↑	0.0191	0.0210	1.3205	0.9919

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	3.075e-05	1.000e-20
X10_P10	6.338e-05	1.000e-20
X14_P10	7.641e-05	1.000e-20
X19_P10	8.931e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.656e-05	3.513e-05	3.531e-05	3.518e-05
B (output stable)	2.242e-05	5.202e-05	5.213e-05	5.222e-05
C (output stable)	1.781e-04	3.572e-04	3.579e-04	3.592e-04
A to Z	3.264e-03	5.897e-03	7.705e-03	9.582e-03
B to Z	3.048e-03	5.378e-03	7.185e-03	9.078e-03
C to Z	2.730e-03	4.847e-03	6.474e-03	8.103e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

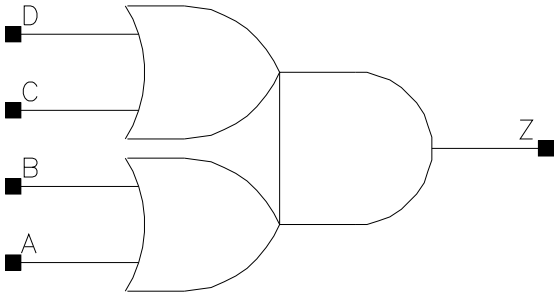
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.952	0.7616
X10_P10	0.800	1.088	0.8704
X14_P10	0.800	1.904	1.5232
X19_P10	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0005	0.0007	0.0014	0.0014
B	0.0005	0.0007	0.0014	0.0014
C	0.0005	0.0008	0.0014	0.0014
D	0.0005	0.0008	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0375	0.0312	2.8908	1.4404
A to Z ↑	0.0264	0.0237	3.9985	1.9975
B to Z ↓	0.0394	0.0329	2.8907	1.4404

B to Z ↑	0.0251	0.0221	3.9927	1.9943
C to Z ↓	0.0318	0.0275	2.8648	1.4317
C to Z ↑	0.0263	0.0245	3.9926	1.9945
D to Z ↓	0.0335	0.0288	2.8642	1.4318
D to Z ↑	0.0246	0.0225	3.9896	1.9918
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0297	0.0318	0.9984	0.7484
A to Z ↑	0.0224	0.0237	1.3287	0.9986
B to Z ↓	0.0303	0.0324	0.9987	0.7488
B to Z ↑	0.0203	0.0216	1.3256	0.9961
C to Z ↓	0.0250	0.0272	0.9921	0.7440
C to Z ↑	0.0225	0.0240	1.3266	0.9965
D to Z ↓	0.0253	0.0277	0.9920	0.7438
D to Z ↑	0.0200	0.0216	1.3239	0.9947

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	2.273e-05	1.000e-20
X10_P10	4.801e-05	1.000e-20
X14_P10	8.053e-05	1.000e-20
X19_P10	9.170e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.651e-05	2.530e-05	7.286e-05	7.267e-05
B (output stable)	2.259e-05	3.803e-05	1.761e-04	1.757e-04
C (output stable)	5.443e-05	6.355e-05	1.478e-04	1.480e-04
D (output stable)	6.206e-05	7.766e-05	2.413e-04	2.422e-04
A to Z	3.326e-03	5.412e-03	8.875e-03	1.060e-02
B to Z	3.192e-03	5.150e-03	8.180e-03	9.897e-03
C to Z	2.906e-03	4.873e-03	7.768e-03	9.463e-03
D to Z	2.780e-03	4.630e-03	7.081e-03	8.776e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

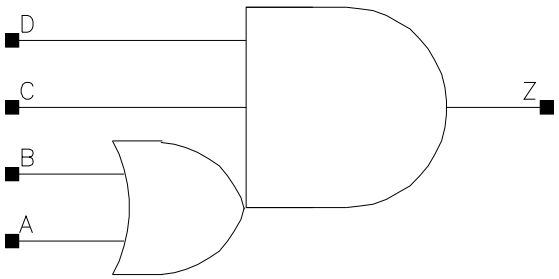
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	0.816	0.6528
X10_P10	0.800	1.088	0.8704
X14_P10	0.800	1.904	1.5232
X19_P10	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P10	X10_P10	X14_P10	X19_P10
A	0.0005	0.0010	0.0012	0.0014
B	0.0005	0.0008	0.0012	0.0015
C	0.0006	0.0008	0.0012	0.0014
D	0.0005	0.0007	0.0012	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X10_P10	X4_P10	X10_P10
A to Z ↓	0.0314	0.0308	3.1240	1.4617
A to Z ↑	0.0301	0.0324	4.2287	2.0322
B to Z ↓	0.0335	0.0305	3.1253	1.4620
B to Z ↑	0.0287	0.0284	4.2244	2.0264
C to Z ↓	0.0281	0.0257	3.0539	1.4348

C to Z ↑	0.0272	0.0275	4.2223	2.0275
D to Z ↓	0.0274	0.0247	3.0538	1.4341
D to Z ↑	0.0291	0.0290	4.2244	2.0282
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0303	0.0292	0.9973	0.7418
A to Z ↑	0.0312	0.0323	1.3535	1.0139
B to Z ↓	0.0306	0.0295	0.9975	0.7418
B to Z ↑	0.0282	0.0292	1.3492	1.0097
C to Z ↓	0.0268	0.0259	0.9795	0.7295
C to Z ↑	0.0274	0.0280	1.3498	1.0114
D to Z ↓	0.0253	0.0245	0.9775	0.7283
D to Z ↑	0.0282	0.0289	1.3501	1.0114

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	2.102e-05	1.000e-20
X10_P10	4.565e-05	1.000e-20
X14_P10	6.771e-05	1.000e-20
X19_P10	8.957e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X10_P10	X14_P10	X19_P10
A (output stable)	7.464e-05	1.086e-04	1.742e-04	1.912e-04
B (output stable)	7.129e-05	1.177e-04	1.988e-04	2.196e-04
C (output stable)	1.500e-05	2.799e-05	6.870e-05	7.701e-05
D (output stable)	2.690e-05	4.414e-05	1.499e-04	1.639e-04
A to Z	2.827e-03	5.322e-03	8.147e-03	1.038e-02
B to Z	2.714e-03	4.901e-03	7.538e-03	9.601e-03
C to Z	3.014e-03	5.361e-03	8.511e-03	1.069e-02
D to Z	2.894e-03	5.168e-03	8.007e-03	1.012e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

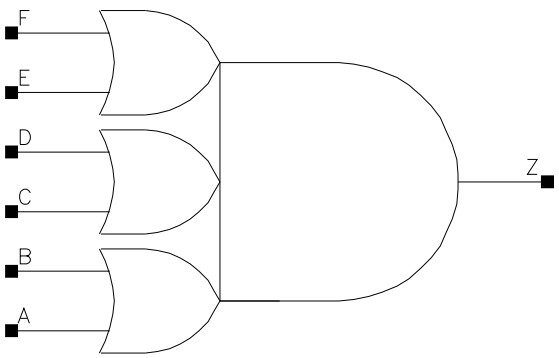
Pin Cycle (vdds)	X4_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	1.360	1.0880
X9_P10	0.800	1.496	1.1968
X19_P10	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P10	X9_P10	X19_P10
A	0.0006	0.0007	0.0012
B	0.0007	0.0009	0.0014
C	0.0005	0.0007	0.0013
D	0.0005	0.0007	0.0014
E	0.0005	0.0007	0.0013
F	0.0005	0.0007	0.0015

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X9_P10	X4_P10	X9_P10
A to Z ↓	0.0442	0.0378	3.1849	1.5728
A to Z ↑	0.0338	0.0331	4.3306	2.1314
B to Z ↓	0.0473	0.0404	3.1854	1.5730
B to Z ↑	0.0334	0.0318	4.3325	2.1294
C to Z ↓	0.0404	0.0343	3.1621	1.5631
C to Z ↑	0.0347	0.0330	4.3338	2.1312
D to Z ↓	0.0422	0.0359	3.1618	1.5634
D to Z ↑	0.0328	0.0309	4.3273	2.1278
E to Z ↓	0.0345	0.0302	3.1281	1.5523
E to Z ↑	0.0327	0.0321	4.3252	2.1280
F to Z ↓	0.0366	0.0321	3.1284	1.5527
F to Z ↑	0.0313	0.0304	4.3202	2.1258
	X19_P10		X19_P10	
A to Z ↓	0.0373		0.7562	
A to Z ↑	0.0322		1.0148	
B to Z ↓	0.0393		0.7562	
B to Z ↑	0.0297		1.0116	
C to Z ↓	0.0342		0.7511	
C to Z ↑	0.0324		1.0144	
D to Z ↓	0.0360		0.7512	
D to Z ↑	0.0303		1.0112	
E to Z ↓	0.0300		0.7460	
E to Z ↑	0.0318		1.0125	
F to Z ↓	0.0318		0.7464	
F to Z ↑	0.0295		1.0096	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	2.383e-05	1.000e-20
X9_P10	5.005e-05	1.000e-20
X19_P10	9.932e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X9_P10	X19_P10
A (output stable)	1.594e-05	2.554e-05	4.687e-05
B (output stable)	2.418e-05	3.676e-05	6.363e-05
C (output stable)	3.196e-05	4.261e-05	8.385e-05
D (output stable)	3.783e-05	5.104e-05	1.018e-04
E (output stable)	1.051e-04	1.293e-04	2.419e-04
F (output stable)	1.045e-04	1.379e-04	2.555e-04
A to Z	3.920e-03	6.435e-03	1.280e-02
B to Z	3.816e-03	6.217e-03	1.227e-02
C to Z	3.568e-03	5.917e-03	1.181e-02
D to Z	3.427e-03	5.658e-03	1.129e-02
E to Z	3.116e-03	5.355e-03	1.072e-02
F to Z	3.004e-03	5.133e-03	1.024e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

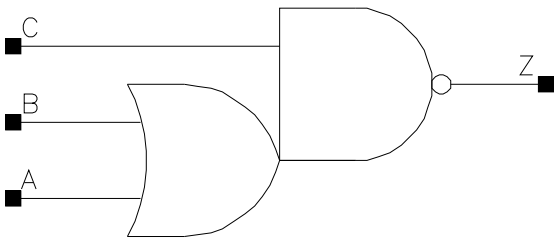
Pin Cycle (vdds)	X4_P10	X9_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.544	0.4352
X10_P10	0.800	1.360	1.0880
X20_P10	0.800	2.720	2.1760
X26_P10	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P10	X10_P10	X20_P10	X26_P10
A	0.0005	0.0018	0.0035	0.0046
B	0.0005	0.0016	0.0032	0.0044
C	0.0006	0.0019	0.0038	0.0052

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X10_P10**	**X3_P10**	**X10_P10**
A to Z ↓	0.0096	0.0109	5.3446	1.6855
A to Z ↑	0.0121	0.0120	8.6953	2.4475
B to Z ↓	0.0075	0.0083	5.2475	1.6949
B to Z ↑	0.0129	0.0119	8.7391	2.4624
C to Z ↓	0.0082	0.0088	4.8431	1.5428
C to Z ↑	0.0131	0.0122	4.9509	1.4008
	X20_P10	**X26_P10**	**X20_P10**	**X26_P10**
A to Z ↓	0.0114	0.0114	0.8615	0.6521

A to Z ↑	0.0125	0.0124	1.2552	0.9444
B to Z ↓	0.0087	0.0089	0.8714	0.6625
B to Z ↑	0.0124	0.0125	1.2620	0.9498
C to Z ↓	0.0093	0.0094	0.7909	0.5997
C to Z ↑	0.0124	0.0123	0.6897	0.5185

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.409e-05	1.000e-20
X10_P10	4.946e-05	1.000e-20
X20_P10	9.772e-05	1.000e-20
X26_P10	1.289e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X10_P10	X20_P10	X26_P10
A (output stable)	4.326e-05	1.608e-04	3.304e-04	4.261e-04
B (output stable)	5.203e-05	2.146e-04	4.544e-04	5.757e-04
C (output stable)	3.947e-05	1.354e-04	2.856e-04	3.750e-04
A to Z	1.067e-03	3.916e-03	7.999e-03	1.063e-02
B to Z	8.908e-04	3.024e-03	6.306e-03	8.393e-03
C to Z	1.335e-03	4.616e-03	9.524e-03	1.259e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

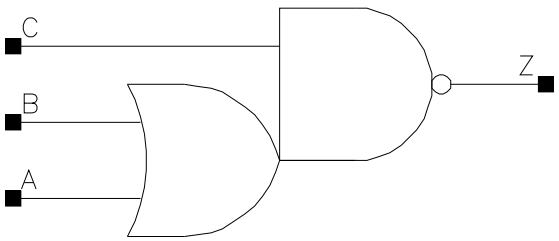
Pin Cycle (vdds)	X3_P10	X10_P10	X20_P10	X26_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X7_P10	0.800	0.952	0.7616
X10_P10	0.800	1.360	1.0880
X13_P10	0.800	1.904	1.5232
X26_P10	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P10	X7_P10	X10_P10	X13_P10
A	0.0007	0.0012	0.0020	0.0025
B	0.0006	0.0013	0.0018	0.0023
C	0.0008	0.0012	0.0017	0.0024
	X26_P10			
A	0.0050			
B	0.0045			
C	0.0047			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X7_P10	X3_P10	X7_P10
A to Z ↓	0.0109	0.0098	4.6936	2.4320
A to Z ↑	0.0166	0.0147	7.0237	3.6136
B to Z ↓	0.0092	0.0076	4.7149	2.3684

B to Z ↑	0.0177	0.0156	7.0551	3.6302
C to Z ↓	0.0098	0.0084	4.4727	2.2688
C to Z ↑	0.0106	0.0091	4.1376	2.1534
	X10_P10	**X13_P10**	**X10_P10**	**X13_P10**
A to Z ↓	0.0095	0.0101	1.6423	1.2569
A to Z ↑	0.0142	0.0153	2.3852	1.8388
B to Z ↓	0.0074	0.0076	1.6375	1.2611
B to Z ↑	0.0151	0.0153	2.3972	1.8464
C to Z ↓	0.0083	0.0085	1.5551	1.1871
C to Z ↑	0.0085	0.0086	1.4194	1.0747
	X26_P10		**X26_P10**	
A to Z ↓	0.0100		0.6480	
A to Z ↑	0.0150		0.9282	
B to Z ↓	0.0075		0.6471	
B to Z ↑	0.0150		0.9324	
C to Z ↓	0.0087		0.6107	
C to Z ↑	0.0085		0.5422	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.876e-05	1.000e-20
X7_P10	3.455e-05	1.000e-20
X10_P10	5.067e-05	1.000e-20
X13_P10	6.749e-05	1.000e-20
X26_P10	1.307e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X7_P10	X10_P10	X13_P10
A (output stable)	1.937e-05	3.550e-05	5.225e-05	9.351e-05
B (output stable)	2.560e-05	4.988e-05	7.339e-05	1.785e-04
C (output stable)	1.823e-04	3.548e-04	4.717e-04	6.817e-04
A to Z	1.839e-03	3.103e-03	4.548e-03	6.400e-03
B to Z	1.589e-03	2.645e-03	3.826e-03	5.120e-03
C to Z	1.343e-03	2.350e-03	3.393e-03	4.662e-03
	X26_P10			
A (output stable)	1.803e-04			
B (output stable)	3.207e-04			
C (output stable)	1.260e-03			
A to Z	1.245e-02			
B to Z	9.884e-03			
C to Z	9.064e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P10	X7_P10	X10_P10	X13_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

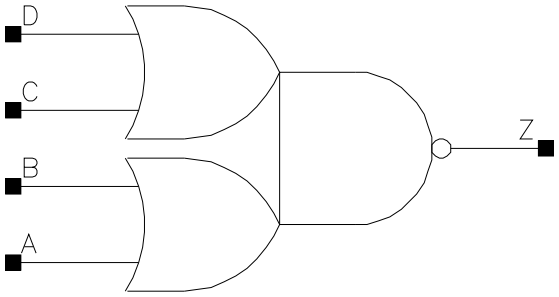
	X26_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X6_P10	0.800	1.360	1.0880
X8_P10	0.800	1.768	1.4144
X11_P10	0.800	2.448	1.9584
X24_P10	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X8_P10	X11_P10
A	0.0006	0.0013	0.0018	0.0024
B	0.0006	0.0011	0.0017	0.0022
C	0.0006	0.0012	0.0017	0.0023
D	0.0005	0.0010	0.0016	0.0021
	X24_P10			
A	0.0051			
B	0.0047			
C	0.0048			
D	0.0045			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	**X6_P10**	**X3_P10**	**X6_P10**
A to Z ↓	0.0102	0.0123	4.4033	2.3871
A to Z ↑	0.0187	0.0183	8.5904	3.8117
B to Z ↓	0.0088	0.0101	4.3708	2.3984
B to Z ↑	0.0200	0.0183	8.6129	3.8239
C to Z ↓	0.0092	0.0116	4.5127	2.4176
C to Z ↑	0.0128	0.0132	8.6264	3.8387
D to Z ↓	0.0074	0.0088	4.4769	2.4470
D to Z ↑	0.0137	0.0125	8.6634	3.8592
	X8_P10	**X11_P10**	**X8_P10**	**X11_P10**
A to Z ↓	0.0117	0.0120	1.6303	1.2363
A to Z ↑	0.0172	0.0173	2.5554	1.9173
B to Z ↓	0.0097	0.0097	1.6420	1.2410
B to Z ↑	0.0176	0.0176	2.5672	1.9265
C to Z ↓	0.0113	0.0116	1.6619	1.2590
C to Z ↑	0.0123	0.0126	2.5539	1.9346
D to Z ↓	0.0090	0.0089	1.6825	1.2666
D to Z ↑	0.0123	0.0124	2.5725	1.9470
	X24_P10		**X24_P10**	
A to Z ↓	0.0121		0.6081	
A to Z ↑	0.0173		0.9288	
B to Z ↓	0.0098		0.6048	
B to Z ↑	0.0178		0.9332	
C to Z ↓	0.0120		0.6193	
C to Z ↑	0.0126		0.9314	
D to Z ↓	0.0092		0.6181	
D to Z ↑	0.0125		0.9378	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.809e-05	1.000e-20
X6_P10	4.117e-05	1.000e-20
X8_P10	5.955e-05	1.000e-20
X11_P10	8.008e-05	1.000e-20
X24_P10	1.605e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X6_P10	X8_P10	X11_P10
A (output stable)	2.250e-05	7.499e-05	9.540e-05	1.339e-04
B (output stable)	3.287e-05	1.811e-04	1.913e-04	3.026e-04
C (output stable)	5.967e-05	1.480e-04	1.902e-04	2.627e-04
D (output stable)	7.304e-05	2.458e-04	2.872e-04	4.289e-04
A to Z	1.714e-03	3.903e-03	5.481e-03	7.384e-03
B to Z	1.505e-03	3.240e-03	4.548e-03	6.127e-03
C to Z	1.198e-03	2.936e-03	4.142e-03	5.664e-03
D to Z	1.018e-03	2.300e-03	3.290e-03	4.478e-03
	X24_P10			
A (output stable)	2.725e-04			
B (output stable)	5.727e-04			
C (output stable)	5.109e-04			
D (output stable)	7.924e-04			

A to Z	1.523e-02			
B to Z	1.266e-02			
C to Z	1.167e-02			
D to Z	9.274e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

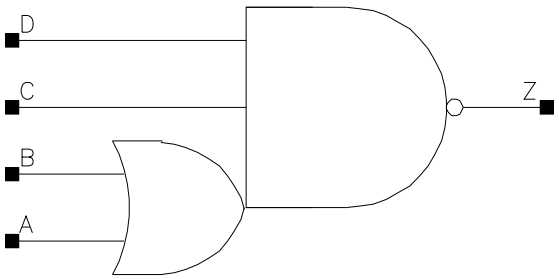
Pin Cycle (vdds)	X3_P10	X6_P10	X8_P10	X11_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P10			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.816	0.6528
X6_P10	0.800	1.360	1.0880
X12_P10	0.800	2.448	1.9584
X18_P10	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X12_P10	X18_P10
A	0.0008	0.0012	0.0023	0.0034
B	0.0006	0.0011	0.0021	0.0031
C	0.0006	0.0013	0.0025	0.0038
D	0.0006	0.0012	0.0024	0.0035

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0173	0.0151	6.4150	3.4605
A to Z ↑	0.0172	0.0141	7.3119	3.6776
B to Z ↓	0.0130	0.0118	6.4647	3.4800
B to Z ↑	0.0159	0.0137	7.3236	3.6978
C to Z ↓	0.0133	0.0133	6.0299	3.2563

C to Z ↑	0.0154	0.0147	3.9880	2.0554
D to Z ↓	0.0147	0.0136	6.0670	3.2731
D to Z ↑	0.0147	0.0133	4.0982	2.0618
	X12_P10	**X18_P10**	**X12_P10**	**X18_P10**
A to Z ↓	0.0154	0.0156	1.7995	1.2167
A to Z ↑	0.0139	0.0138	1.8446	1.2369
B to Z ↓	0.0120	0.0123	1.8116	1.2265
B to Z ↑	0.0135	0.0136	1.8562	1.2448
C to Z ↓	0.0131	0.0132	1.6939	1.1464
C to Z ↑	0.0145	0.0143	1.0474	0.6904
D to Z ↓	0.0137	0.0138	1.7032	1.1520
D to Z ↑	0.0130	0.0130	1.0451	0.6980

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.529e-05	1.000e-20
X6_P10	2.880e-05	1.000e-20
X12_P10	5.488e-05	1.000e-20
X18_P10	8.099e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X6_P10	X12_P10	X18_P10
A (output stable)	1.049e-04	2.168e-04	4.113e-04	5.759e-04
B (output stable)	1.146e-04	2.415e-04	4.372e-04	6.225e-04
C (output stable)	2.462e-05	7.444e-05	1.389e-04	2.179e-04
D (output stable)	4.247e-05	1.565e-04	2.789e-04	4.290e-04
A to Z	1.806e-03	3.017e-03	5.915e-03	8.822e-03
B to Z	1.420e-03	2.371e-03	4.611e-03	6.924e-03
C to Z	2.162e-03	4.016e-03	7.708e-03	1.153e-02
D to Z	1.972e-03	3.450e-03	6.650e-03	9.880e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

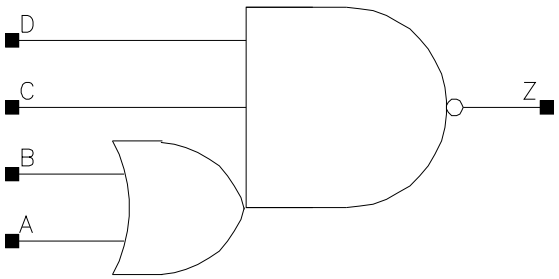
Pin Cycle (vdds)	X3_P10	X6_P10	X12_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P10	0.800	0.680	0.5440
X6_P10	0.800	1.360	1.0880
X9_P10	0.800	1.768	1.4144
X12_P10	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P10	X6_P10	X9_P10	X12_P10
A	0.0006	0.0013	0.0020	0.0025
B	0.0006	0.0012	0.0017	0.0025
C	0.0006	0.0012	0.0018	0.0024
D	0.0006	0.0011	0.0017	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P10	X6_P10	X3_P10	X6_P10
A to Z ↓	0.0135	0.0139	6.8848	3.4136
A to Z ↑	0.0176	0.0187	7.3606	3.6701
B to Z ↓	0.0114	0.0113	6.7564	3.4340
B to Z ↑	0.0187	0.0188	7.3896	3.6844
C to Z ↓	0.0113	0.0119	6.5080	3.2678

C to Z ↑	0.0117	0.0120	4.3076	2.1329
D to Z ↓	0.0121	0.0120	6.5549	3.2874
D to Z ↑	0.0102	0.0097	4.3518	2.1499
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0142	0.0142	2.3445	1.7832
A to Z ↑	0.0180	0.0185	2.4203	1.8889
B to Z ↓	0.0117	0.0115	2.3460	1.7895
B to Z ↑	0.0184	0.0191	2.4313	1.8984
C to Z ↓	0.0119	0.0120	2.2364	1.7025
C to Z ↑	0.0115	0.0117	1.4092	1.0678
D to Z ↓	0.0123	0.0122	2.2502	1.7132
D to Z ↑	0.0095	0.0093	1.4206	1.0806

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P10	1.399e-05	1.000e-20
X6_P10	2.944e-05	1.000e-20
X9_P10	4.186e-05	1.000e-20
X12_P10	5.600e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	1.437e-05	3.195e-05	5.065e-05	6.427e-05
B (output stable)	1.628e-05	5.183e-05	7.130e-05	9.694e-05
C (output stable)	4.569e-05	1.027e-04	1.535e-04	1.988e-04
D (output stable)	8.775e-05	3.082e-04	3.542e-04	5.608e-04
A to Z	1.879e-03	4.042e-03	5.916e-03	7.902e-03
B to Z	1.627e-03	3.342e-03	4.874e-03	6.510e-03
C to Z	1.396e-03	3.025e-03	4.349e-03	5.882e-03
D to Z	1.223e-03	2.553e-03	3.736e-03	4.932e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

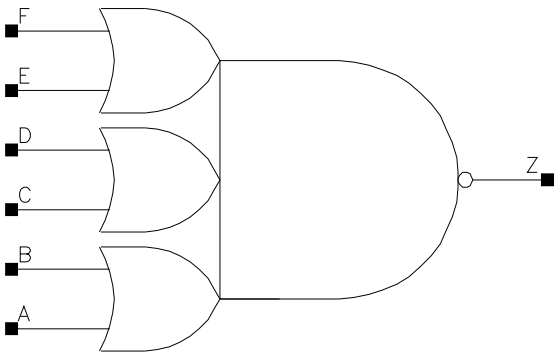
Pin Cycle (vdds)	X3_P10	X6_P10	X9_P10	X12_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.224	0.9792
X3_P10	0.800	1.224	0.9792
X5_P10	0.800	2.040	1.6320
X8_P10	0.800	2.720	2.1760
X10_P10	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P10	X3_P10	X5_P10	X8_P10
A	0.0005	0.0007	0.0013	0.0019
B	0.0005	0.0006	0.0012	0.0017
C	0.0005	0.0006	0.0012	0.0018
D	0.0006	0.0006	0.0011	0.0017

E	0.0005	0.0006	0.0012	0.0017
F	0.0005	0.0006	0.0011	0.0016
	X10_P10			
A	0.0025			
B	0.0023			
C	0.0024			
D	0.0022			
E	0.0023			
F	0.0021			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X3_P10**	**X2_P10**	**X3_P10**
A to Z ↓	0.0179	0.0174	7.4613	5.8749
A to Z ↑	0.0257	0.0225	9.8753	6.9450
B to Z ↓	0.0164	0.0158	7.4892	5.9149
B to Z ↑	0.0275	0.0242	9.8965	6.9672
C to Z ↓	0.0177	0.0176	7.5102	5.8998
C to Z ↑	0.0221	0.0198	9.8843	7.0649
D to Z ↓	0.0165	0.0155	7.5969	5.9849
D to Z ↑	0.0244	0.0210	9.9296	7.0871
E to Z ↓	0.0160	0.0160	7.5806	5.9450
E to Z ↑	0.0170	0.0152	9.9058	7.0880
F to Z ↓	0.0146	0.0141	7.6621	6.0397
F to Z ↑	0.0185	0.0163	9.9579	7.1245
	X5_P10	**X8_P10**	**X5_P10**	**X8_P10**
A to Z ↓	0.0186	0.0182	3.1444	2.1380
A to Z ↑	0.0234	0.0225	3.6671	2.4254
B to Z ↓	0.0161	0.0158	3.1652	2.1430
B to Z ↑	0.0237	0.0234	3.6771	2.4338
C to Z ↓	0.0174	0.0179	3.1675	2.1523
C to Z ↑	0.0195	0.0192	3.7073	2.4858
D to Z ↓	0.0149	0.0153	3.1810	2.1613
D to Z ↑	0.0199	0.0203	3.7231	2.4964
E to Z ↓	0.0170	0.0168	3.2047	2.1703
E to Z ↑	0.0153	0.0148	3.7168	2.4961
F to Z ↓	0.0141	0.0141	3.2228	2.1772
F to Z ↑	0.0151	0.0153	3.7372	2.5126
	X10_P10		**X10_P10**	
A to Z ↓	0.0187		1.6260	
A to Z ↑	0.0229		1.8444	
B to Z ↓	0.0161		1.6316	
B to Z ↑	0.0234		1.8507	
C to Z ↓	0.0177		1.6357	
C to Z ↑	0.0193		1.8824	
D to Z ↓	0.0152		1.6421	
D to Z ↑	0.0199		1.8909	
E to Z ↓	0.0171		1.6506	
E to Z ↑	0.0150		1.8803	
F to Z ↓	0.0146		1.6621	
F to Z ↑	0.0153		1.8919	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P10	1.706e-05	1.000e-20
X3_P10	2.602e-05	1.000e-20
X5_P10	4.940e-05	1.000e-20
X8_P10	7.105e-05	1.000e-20
X10_P10	9.444e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P10	X3_P10	X5_P10	X8_P10
A (output stable)	2.012e-05	2.515e-05	6.987e-05	9.415e-05
B (output stable)	2.616e-05	3.428e-05	1.354e-04	1.591e-04
C (output stable)	3.735e-05	4.596e-05	1.065e-04	1.466e-04
D (output stable)	4.405e-05	5.410e-05	1.676e-04	1.981e-04
E (output stable)	1.133e-04	1.393e-04	2.520e-04	3.782e-04
F (output stable)	1.216e-04	1.513e-04	3.145e-04	4.352e-04
A to Z	2.260e-03	2.775e-03	5.569e-03	8.047e-03
B to Z	2.077e-03	2.525e-03	4.837e-03	7.033e-03
C to Z	1.866e-03	2.322e-03	4.484e-03	6.582e-03
D to Z	1.708e-03	2.072e-03	3.873e-03	5.753e-03
E to Z	1.453e-03	1.830e-03	3.660e-03	5.244e-03
F to Z	1.300e-03	1.608e-03	3.050e-03	4.465e-03
	X10_P10			
A (output stable)	1.336e-04			
B (output stable)	2.465e-04			
C (output stable)	1.998e-04			
D (output stable)	3.080e-04			
E (output stable)	4.870e-04			
F (output stable)	5.843e-04			
A to Z	1.086e-02			
B to Z	9.430e-03			
C to Z	8.799e-03			
D to Z	7.605e-03			
E to Z	7.128e-03			
F to Z	6.006e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X2_P10	X3_P10	X5_P10	X8_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P10			

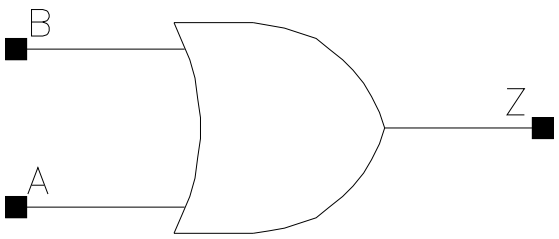
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.544	0.4352
X9_P10	0.800	0.680	0.5440
X19_P10	0.800	1.360	1.0880
X29_P10	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P10	X9_P10	X19_P10	X29_P10
A	0.0006	0.0007	0.0013	0.0013
B	0.0005	0.0007	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X9_P10**	**X5_P10**	**X9_P10**
A to Z ↓	0.0280	0.0252	3.0186	1.5199
A to Z ↑	0.0181	0.0198	4.1152	2.0749
B to Z ↓	0.0295	0.0263	3.0200	1.5196
B to Z ↑	0.0171	0.0183	4.1210	2.0763
	X19_P10	**X29_P10**	**X19_P10**	**X29_P10**
A to Z ↓	0.0255	0.0307	0.7305	0.4998
A to Z ↑	0.0198	0.0231	0.9884	0.6634
B to Z ↓	0.0256	0.0311	0.7305	0.4997
B to Z ↑	0.0177	0.0211	0.9867	0.6634

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	1.753e-05	1.000e-20
X9_P10	3.399e-05	1.000e-20
X19_P10	6.932e-05	1.000e-20
X29_P10	8.818e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X9_P10	X19_P10	X29_P10
A (output stable)	1.402e-05	2.561e-05	9.132e-05	9.155e-05
B (output stable)	2.855e-05	4.800e-05	2.709e-04	2.717e-04
A to Z	2.429e-03	4.083e-03	8.592e-03	1.267e-02
B to Z	2.308e-03	3.878e-03	7.895e-03	1.197e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

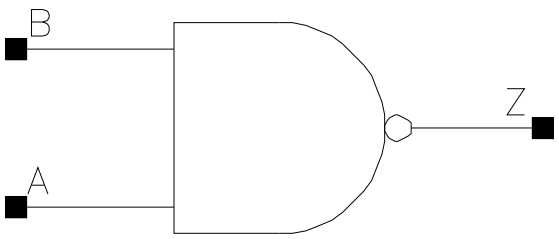
Pin Cycle (vdds)	X5_P10	X9_P10	X19_P10	X29_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.816	0.6528
X9_P10	0.800	0.952	0.7616
X14_P10	0.800	1.088	0.8704
X18_P10	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P10	X9_P10	X14_P10	X18_P10
A	0.0008	0.0007	0.0007	0.0007
B	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X9_P10**	**X5_P10**	**X9_P10**
A to Z ↓	0.0234	0.0270	2.7432	1.4932
A to Z ↑	0.0259	0.0287	3.9619	2.0842
B to Z ↓	0.0248	0.0289	2.7423	1.4934
B to Z ↑	0.0241	0.0274	3.9653	2.0837
	X14_P10	**X18_P10**	**X14_P10**	**X18_P10**
A to Z ↓	0.0302	0.0322	1.0315	0.7786
A to Z ↑	0.0309	0.0320	1.3787	1.0688
B to Z ↓	0.0321	0.0340	1.0316	0.7788
B to Z ↑	0.0296	0.0307	1.3789	1.0683

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	4.257e-05	1.000e-20
X9_P10	5.027e-05	1.000e-20
X14_P10	5.994e-05	1.000e-20
X18_P10	6.559e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X9_P10	X14_P10	X18_P10
A (output stable)	1.529e-05	1.441e-05	1.465e-05	1.503e-05
B (output stable)	3.480e-05	3.173e-05	3.195e-05	3.053e-05
A to Z	4.252e-03	5.523e-03	7.225e-03	8.354e-03
B to Z	4.074e-03	5.353e-03	7.056e-03	8.191e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

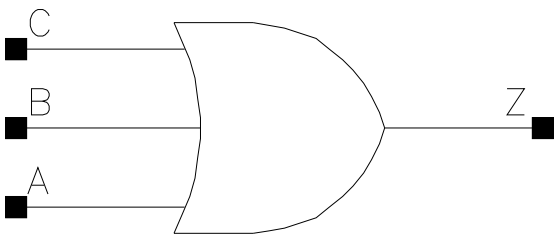
Pin Cycle (vdds)	X5_P10	X9_P10	X14_P10	X18_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.680	0.5440
X10_P10	0.800	0.952	0.7616
X14_P10	0.800	1.496	1.1968
X19_P10	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0005	0.0008	0.0013	0.0021
B	0.0005	0.0007	0.0015	0.0021
C	0.0006	0.0007	0.0014	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0362	0.0331	3.1139	1.4839
A to Z ↑	0.0213	0.0192	4.1397	1.9705
B to Z ↓	0.0365	0.0335	3.1121	1.4848
B to Z ↑	0.0207	0.0182	4.1343	1.9697
C to Z ↓	0.0374	0.0338	3.1137	1.4823
C to Z ↑	0.0196	0.0168	4.1393	1.9684
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**
A to Z ↓	0.0310	0.0298	0.9959	0.7609

A to Z ↑	0.0177	0.0174	1.3469	1.0316
B to Z ↓	0.0318	0.0296	0.9965	0.7613
B to Z ↑	0.0166	0.0166	1.3443	1.0306
C to Z ↓	0.0299	0.0292	0.9948	0.7611
C to Z ↑	0.0147	0.0147	1.3421	1.0290

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	1.569e-05	1.000e-20
X10_P10	3.186e-05	1.000e-20
X14_P10	5.354e-05	1.000e-20
X19_P10	7.354e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	1.747e-05	3.124e-05	6.593e-05	1.186e-04
B (output stable)	2.080e-05	3.604e-05	9.372e-05	1.360e-04
C (output stable)	5.448e-05	9.761e-05	3.201e-04	3.741e-04
A to Z	2.874e-03	4.943e-03	7.960e-03	1.113e-02
B to Z	2.731e-03	4.704e-03	7.530e-03	1.020e-02
C to Z	2.608e-03	4.475e-03	6.795e-03	9.373e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

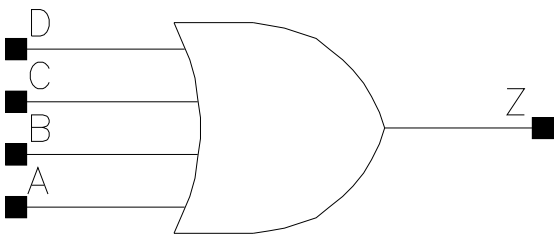
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	0.800	1.224	0.9792
X8_P10	0.800	1.496	1.1968
X12_P10	0.800	2.176	1.7408
X15_P10	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P10	X8_P10	X12_P10	X15_P10
A	0.0005	0.0007	0.0013	0.0014
B	0.0005	0.0008	0.0012	0.0014
C	0.0005	0.0007	0.0013	0.0014
D	0.0006	0.0008	0.0012	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X8_P10	X4_P10	X8_P10
A to Z ↓	0.0293	0.0283	4.5074	2.3899
A to Z ↑	0.0189	0.0199	3.8581	2.0615
B to Z ↓	0.0313	0.0300	4.5088	2.3898
B to Z ↑	0.0179	0.0186	3.8593	2.0605
C to Z ↓	0.0313	0.0280	4.5174	2.3846
C to Z ↑	0.0194	0.0193	3.9604	2.0678

D to Z ↓	0.0337	0.0298	4.5168	2.3850
D to Z ↑	0.0186	0.0182	3.9574	2.0654
	X12_P10	**X15_P10**	**X12_P10**	**X15_P10**
A to Z ↓	0.0285	0.0288	1.6502	1.2378
A to Z ↑	0.0201	0.0192	1.3202	1.0132
B to Z ↓	0.0293	0.0292	1.6499	1.2377
B to Z ↑	0.0188	0.0174	1.3191	1.0121
C to Z ↓	0.0280	0.0279	1.6481	1.2355
C to Z ↑	0.0192	0.0182	1.3159	1.0193
D to Z ↓	0.0289	0.0285	1.6475	1.2353
D to Z ↑	0.0178	0.0166	1.3139	1.0171

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	2.080e-05	1.000e-20
X8_P10	4.394e-05	1.000e-20
X12_P10	5.723e-05	1.000e-20
X15_P10	8.241e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	6.191e-04	1.104e-03	1.682e-03	2.268e-03
B (output stable)	5.793e-04	1.025e-03	1.541e-03	2.077e-03
C (output stable)	5.910e-04	1.020e-03	1.506e-03	2.026e-03
D (output stable)	5.511e-04	9.381e-04	1.361e-03	1.860e-03
A to Z	2.635e-03	5.157e-03	7.425e-03	9.823e-03
B to Z	2.530e-03	4.943e-03	6.988e-03	9.142e-03
C to Z	2.635e-03	4.642e-03	6.710e-03	8.585e-03
D to Z	2.535e-03	4.436e-03	6.272e-03	7.988e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

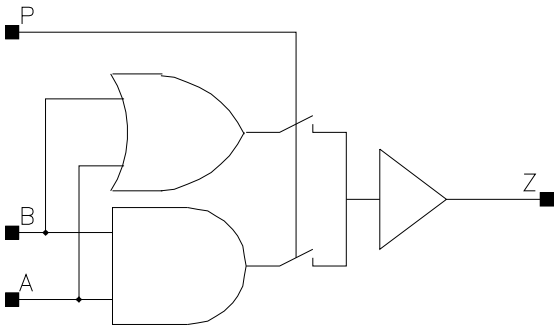
Pin Cycle (vdds)	X4_P10	X8_P10	X12_P10	X15_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	0.800	0.952	0.7616
X10_P10	1.600	0.816	1.3056
X14_P10	1.600	1.224	1.9584
X19_P10	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P10	X10_P10	X14_P10	X19_P10
A	0.0011	0.0013	0.0025	0.0025
B	0.0010	0.0014	0.0026	0.0027
P	0.0006	0.0008	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
A to Z ↓	0.0347	0.0321	3.0647	1.4305
A to Z ↑	0.0200	0.0243	4.1529	1.9875
B to Z ↓	0.0350	0.0332	3.0736	1.4364
B to Z ↑	0.0212	0.0259	4.1588	1.9892
P to Z ↓	0.0330	0.0322	3.0695	1.4358
P to Z ↑	0.0207	0.0257	4.1517	1.9871
	X14_P10	**X19_P10**	**X14_P10**	**X19_P10**

A to Z ↓	0.0296	0.0319	0.9864	0.7392
A to Z ↑	0.0235	0.0246	1.3620	1.0173
B to Z ↓	0.0287	0.0312	0.9955	0.7444
B to Z ↑	0.0236	0.0251	1.3641	1.0181
P to Z ↓	0.0289	0.0314	0.9955	0.7436
P to Z ↑	0.0242	0.0257	1.3629	1.0169

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	2.369e-05	1.000e-20
X10_P10	5.213e-05	1.000e-20
X14_P10	8.597e-05	1.000e-20
X19_P10	9.926e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	3.546e-05	5.242e-05	1.492e-04	1.399e-04
B (output stable)	5.050e-05	8.268e-05	3.442e-04	3.262e-04
P (output stable)	1.559e-04	2.429e-04	4.692e-04	4.274e-04
A to Z	2.887e-03	5.612e-03	8.899e-03	1.077e-02
B to Z	2.806e-03	5.551e-03	8.456e-03	1.036e-02
P to Z	2.609e-03	5.304e-03	8.392e-03	1.033e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

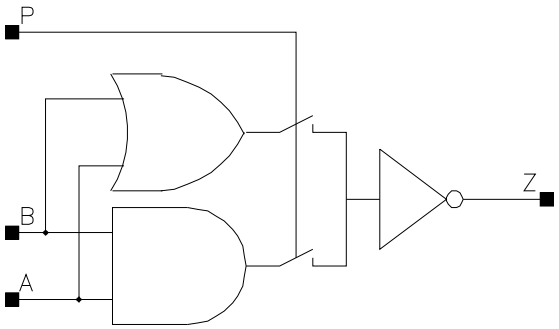
Pin Cycle (vdds)	X5_P10	X10_P10	X14_P10	X19_P10
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.600	0.544	0.8704
X10_P10	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P10	X10_P10
A	0.0012	0.0023
B	0.0011	0.0021
P	0.0008	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	X10_P10	X5_P10	X10_P10
A to Z ↓	0.0119	0.0112	4.5665	2.3865
A to Z ↑	0.0183	0.0170	7.0512	3.5840
B to Z ↓	0.0128	0.0110	4.5297	2.3992
B to Z ↑	0.0186	0.0157	7.0406	3.6373
P to Z ↓	0.0131	0.0112	4.6379	2.4173
P to Z ↑	0.0182	0.0152	7.1132	3.6074

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	2.437e-05	1.000e-20
X10_P10	4.581e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P10	X10_P10
A (output stable)	5.012e-05	1.497e-04
B (output stable)	7.555e-05	3.366e-04
P (output stable)	2.099e-04	4.779e-04
A to Z	2.046e-03	3.683e-03
B to Z	1.913e-03	3.167e-03
P to Z	1.684e-03	2.922e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

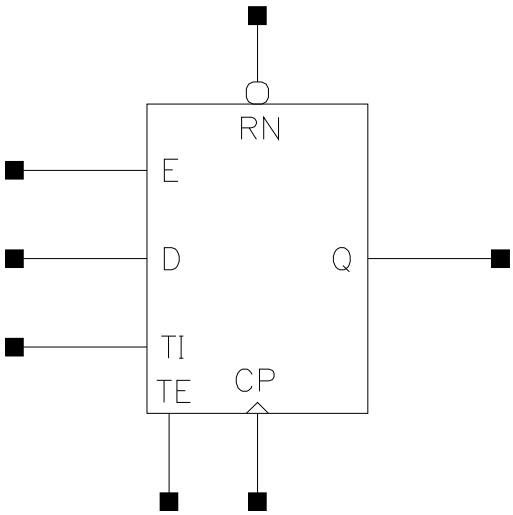
Pin Cycle (vdds)	X5_P10	X10_P10
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.600	2.992	4.7872
X10_P10	1.600	3.128	5.0048
X19_P10	1.600	3.264	5.2224
X23_P10	1.600	3.264	5.2224
X29_P10	1.600	3.536	5.6576
X34_P10	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10	X23_P10
CP	0.0006	0.0006	0.0006	0.0006
D	0.0006	0.0006	0.0006	0.0006
E	0.0013	0.0013	0.0013	0.0013

RN	0.0010	0.0009	0.0010	0.0010
TE	0.0010	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004	0.0004
	X29_P10	X34_P10		
CP	0.0006	0.0006		
D	0.0006	0.0006		
E	0.0013	0.0013		
RN	0.0009	0.0009		
TE	0.0010	0.0010		
TI	0.0004	0.0004		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
CP to Q ↓	0.0458	0.0733	2.8126	1.4065
CP to Q ↑	0.0615	0.0952	3.9169	1.9848
RN to Q ↓	0.0433	0.0659	2.7156	1.4057
	X19_P10	**X23_P10**	**X19_P10**	**X23_P10**
CP to Q ↓	0.0798	0.0804	0.7284	0.5573
CP to Q ↑	0.0998	0.0983	1.0008	0.9800
RN to Q ↓	0.0726	0.0732	0.7286	0.5571
	X29_P10	**X34_P10**	**X29_P10**	**X34_P10**
CP to Q ↓	0.0691	0.0686	0.4850	0.3833
CP to Q ↑	0.0824	0.0833	0.6644	0.6625
RN to Q ↓	0.0647	0.0642	0.4838	0.3826

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P10	X10_P10	X19_P10	X23_P10
CP ↓	min_pulse_width to CP	0.0548	0.0548	0.0548	0.0548
CP ↑	min_pulse_width to CP	0.0409	0.0395	0.0409	0.0409
D ↓	hold_rising to CP	-0.0294	-0.0294	-0.0294	-0.0294
D ↑	hold_rising to CP	-0.0067	-0.0067	-0.0067	-0.0067
D ↓	setup_rising to CP	0.0614	0.0614	0.0640	0.0640
D ↑	setup_rising to CP	0.0374	0.0374	0.0374	0.0374
E ↓	hold_rising to CP	-0.0311	-0.0311	-0.0311	-0.0311
E ↑	hold_rising to CP	-0.0099	-0.0099	-0.0099	-0.0099
E ↓	setup_rising to CP	0.0834	0.0834	0.0834	0.0834
E ↑	setup_rising to CP	0.0640	0.0640	0.0640	0.0640
RN ↓	min_pulse_width to RN	0.0544	0.0447	0.0496	0.0496
RN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
RN ↑	removal_rising to CP	0.0064	0.0064	0.0064	0.0064
TE ↓	hold_rising to CP	-0.0142	-0.0142	-0.0142	-0.0142

TE ↑	hold_rising to CP	-0.0045	-0.0045	-0.0045	-0.0045
TE ↓	setup_rising to CP	0.0483	0.0479	0.0479	0.0479
TE ↑	setup_rising to CP	0.0618	0.0618	0.0618	0.0618
TI ↓	hold_rising to CP	-0.0264	-0.0264	-0.0264	-0.0264
TI ↑	hold_rising to CP	-0.0030	-0.0030	-0.0030	-0.0030
TI ↓	setup_rising to CP	0.0570	0.0570	0.0570	0.0570
TI ↑	setup_rising to CP	0.0286	0.0293	0.0286	0.0286
		X29_P10	X34_P10		
CP ↓	min_pulse_width to CP	0.0548	0.0548		
CP ↑	min_pulse_width to CP	0.0408	0.0408		
D ↓	hold_rising to CP	-0.0294	-0.0294		
D ↑	hold_rising to CP	-0.0067	-0.0067		
D ↓	setup_rising to CP	0.0640	0.0640		
D ↑	setup_rising to CP	0.0374	0.0374		
E ↓	hold_rising to CP	-0.0315	-0.0315		
E ↑	hold_rising to CP	-0.0099	-0.0099		
E ↓	setup_rising to CP	0.0834	0.0834		
E ↑	setup_rising to CP	0.0640	0.0640		
RN ↓	min_pulse_width to RN	0.0518	0.0518		
RN ↑	recovery_rising to CP	-0.0017	-0.0017		
RN ↑	removal_rising to CP	0.0064	0.0064		
TE ↓	hold_rising to CP	-0.0142	-0.0142		
TE ↑	hold_rising to CP	-0.0013	-0.0013		
TE ↓	setup_rising to CP	0.0479	0.0479		
TE ↑	setup_rising to CP	0.0618	0.0618		
TI ↓	hold_rising to CP	-0.0264	-0.0264		
TI ↑	hold_rising to CP	-0.0030	-0.0030		
TI ↓	setup_rising to CP	0.0570	0.0570		
TI ↑	setup_rising to CP	0.0286	0.0286		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	9.450e-05	1.000e-20
X10_P10	1.162e-04	1.000e-20
X19_P10	1.532e-04	1.000e-20
X23_P10	1.575e-04	1.000e-20

X29_P10	2.020e-04	1.000e-20
X34_P10	2.098e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

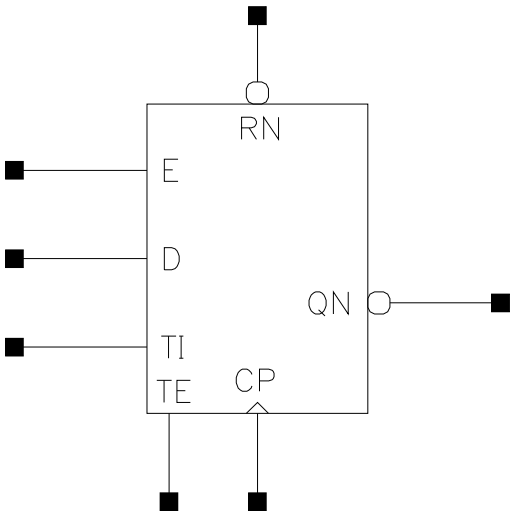
Pin Cycle	X5_P10	X10_P10	X19_P10	X23_P10
Clock 100Mhz Data 0Mhz	1.024e-02	1.023e-02	1.024e-02	1.025e-02
Clock 100Mhz Data 25Mhz	1.077e-02	1.142e-02	1.253e-02	1.265e-02
Clock 100Mhz Data 50Mhz	1.131e-02	1.261e-02	1.482e-02	1.505e-02
Clock = 0 Data 100Mhz	6.427e-03	6.425e-03	6.425e-03	6.425e-03
Clock = 1 Data 100Mhz	2.485e-03	2.485e-03	2.486e-03	2.486e-03
	X29_P10	X34_P10		
Clock 100Mhz Data 0Mhz	1.025e-02	1.025e-02		
Clock 100Mhz Data 25Mhz	1.353e-02	1.385e-02		
Clock 100Mhz Data 50Mhz	1.681e-02	1.745e-02		
Clock = 0 Data 100Mhz	6.424e-03	6.424e-03		
Clock = 1 Data 100Mhz	2.485e-03	2.485e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P10	1.600	2.992	4.7872
X10_P10	1.600	3.128	5.0048
X19_P10	1.600	3.264	5.2224
X23_P10	1.600	3.264	5.2224
X29_P10	1.600	3.536	5.6576
X34_P10	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P10	X10_P10	X19_P10	X23_P10
CP	0.0006	0.0006	0.0006	0.0006
D	0.0006	0.0006	0.0006	0.0006
E	0.0013	0.0014	0.0014	0.0014

RN	0.0009	0.0009	0.0009	0.0009
TE	0.0010	0.0010	0.0010	0.0010
TI	0.0004	0.0004	0.0004	0.0004
	X29_P10	X34_P10		
CP	0.0006	0.0006		
D	0.0006	0.0006		
E	0.0014	0.0013		
RN	0.0009	0.0010		
TE	0.0010	0.0010		
TI	0.0004	0.0004		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P10	**X10_P10**	**X5_P10**	**X10_P10**
CP to QN ↓	0.0832	0.0740	2.8063	1.4049
CP to QN ↑	0.0614	0.0581	3.9022	1.9836
RN to QN ↑	0.0538	0.0547	3.9019	1.9820
	X19_P10	**X23_P10**	**X19_P10**	**X23_P10**
CP to QN ↓	0.0785	0.0792	0.7212	0.5574
CP to QN ↑	0.0640	0.0619	1.0016	0.9789
RN to QN ↑	0.0586	0.0565	1.0002	0.9788
	X29_P10	**X34_P10**	**X29_P10**	**X34_P10**
CP to QN ↓	0.1054	0.1033	0.4853	0.3782
CP to QN ↑	0.0831	0.0823	0.6654	0.6628
RN to QN ↑	0.0756	0.0750	0.6647	0.6629

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P10	X10_P10	X19_P10	X23_P10
CP ↓	min_pulse_width to CP	0.0548	0.0548	0.0548	0.0548
CP ↑	min_pulse_width to CP	0.0394	0.0408	0.0408	0.0408
D ↓	hold_rising to CP	-0.0294	-0.0294	-0.0294	-0.0294
D ↑	hold_rising to CP	-0.0067	-0.0067	-0.0067	-0.0067
D ↓	setup_rising to CP	0.0640	0.0640	0.0640	0.0640
D ↑	setup_rising to CP	0.0374	0.0374	0.0374	0.0374
E ↓	hold_rising to CP	-0.0311	-0.0311	-0.0315	-0.0315
E ↑	hold_rising to CP	-0.0099	-0.0099	-0.0099	-0.0099
E ↓	setup_rising to CP	0.0834	0.0834	0.0834	0.0834
E ↑	setup_rising to CP	0.0640	0.0640	0.0640	0.0640
RN ↓	min_pulse_width to RN	0.0447	0.0496	0.0566	0.0566
RN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
RN ↑	removal_rising to CP	0.0064	0.0064	0.0064	0.0064
TE ↓	hold_rising to CP	-0.0142	-0.0142	-0.0142	-0.0142

TE ↑	hold_rising to CP	-0.0045	-0.0045	-0.0013	-0.0013
TE ↓	setup_rising to CP	0.0479	0.0479	0.0479	0.0479
TE ↑	setup_rising to CP	0.0618	0.0618	0.0618	0.0618
TI ↓	hold_rising to CP	-0.0264	-0.0264	-0.0264	-0.0264
TI ↑	hold_rising to CP	-0.0030	-0.0030	-0.0030	-0.0030
TI ↓	setup_rising to CP	0.0570	0.0570	0.0570	0.0570
TI ↑	setup_rising to CP	0.0286	0.0286	0.0286	0.0286
		X29_P10	X34_P10		
CP ↓	min_pulse_width to CP	0.0548	0.0548		
CP ↑	min_pulse_width to CP	0.0395	0.0395		
D ↓	hold_rising to CP	-0.0294	-0.0294		
D ↑	hold_rising to CP	-0.0067	-0.0067		
D ↓	setup_rising to CP	0.0614	0.0640		
D ↑	setup_rising to CP	0.0374	0.0374		
E ↓	hold_rising to CP	-0.0311	-0.0311		
E ↑	hold_rising to CP	-0.0099	-0.0099		
E ↓	setup_rising to CP	0.0834	0.0834		
E ↑	setup_rising to CP	0.0640	0.0640		
RN ↓	min_pulse_width to RN	0.0447	0.0447		
RN ↑	recovery_rising to CP	-0.0017	-0.0017		
RN ↑	removal_rising to CP	0.0064	0.0064		
TE ↓	hold_rising to CP	-0.0142	-0.0142		
TE ↑	hold_rising to CP	-0.0045	-0.0045		
TE ↓	setup_rising to CP	0.0479	0.0479		
TE ↑	setup_rising to CP	0.0618	0.0618		
TI ↓	hold_rising to CP	-0.0264	-0.0264		
TI ↑	hold_rising to CP	-0.0030	-0.0030		
TI ↓	setup_rising to CP	0.0570	0.0570		
TI ↑	setup_rising to CP	0.0293	0.0286		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P10	9.260e-05	1.000e-20
X10_P10	1.121e-04	1.000e-20
X19_P10	1.461e-04	1.000e-20
X23_P10	1.527e-04	1.000e-20

X29_P10	1.871e-04	1.000e-20
X34_P10	1.991e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

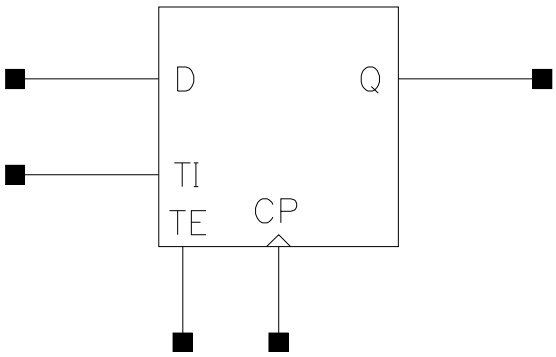
Pin Cycle	X5_P10	X10_P10	X19_P10	X23_P10
Clock 100Mhz Data 0Mhz	1.024e-02	1.025e-02	1.025e-02	1.025e-02
Clock 100Mhz Data 25Mhz	1.084e-02	1.139e-02	1.253e-02	1.264e-02
Clock 100Mhz Data 50Mhz	1.144e-02	1.252e-02	1.481e-02	1.502e-02
Clock = 0 Data 100Mhz	6.425e-03	6.425e-03	6.425e-03	6.425e-03
Clock = 1 Data 100Mhz	2.485e-03	2.486e-03	2.486e-03	2.486e-03
	X29_P10	X34_P10		
Clock 100Mhz Data 0Mhz	1.025e-02	1.025e-02		
Clock 100Mhz Data 25Mhz	1.361e-02	1.387e-02		
Clock 100Mhz Data 50Mhz	1.696e-02	1.749e-02		
Clock = 0 Data 100Mhz	6.424e-03	6.424e-03		
Clock = 1 Data 100Mhz	2.485e-03	2.485e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P10	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P10	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P10	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P10	C8T28SOI_LLHF_-SDFPQX3_P10	C8T28SOIDV_LL_-SDFPQX5_P10	C8T28SOIDV_LL_-SDFPQX10_P10
CP	0.0008	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P10	C8T28SOIDV_LL_-SDFPQX23_P10	C8T28SOIDV_LL_-SDFPQX29_P10	
CP	0.0006	0.0006	0.0006	
D	0.0006	0.0006	0.0006	
TE	0.0010	0.0010	0.0010	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P10	**C8T28SOI_LLHF_-SDFPQX3_P10**	**C8T28SOI_LL_-SDFPQX5_P10**	**C8T28SOI_LLHF_-SDFPQX3_P10**
CP to Q ↓	0.0470	0.0403	2.9438	4.4567
CP to Q ↑	0.0462	0.0518	3.9503	5.8801
	C8T28SOIDV_LL_-SDFPQX5_P10	**C8T28SOIDV_LL_-SDFPQX10_P10**	**C8T28SOIDV_LL_-SDFPQX5_P10**	**C8T28SOIDV_LL_-SDFPQX10_P10**
CP to Q ↓	0.0428	0.0603	2.8039	1.3664
CP to Q ↑	0.0531	0.0764	3.9093	1.9588
	C8T28SOIDV_LL_-SDFPQX19_P10	**C8T28SOIDV_LL_-SDFPQX23_P10**	**C8T28SOIDV_LL_-SDFPQX19_P10**	**C8T28SOIDV_LL_-SDFPQX23_P10**
CP to Q ↓	0.0660	0.0675	0.7088	0.5539
CP to Q ↑	0.0817	0.0835	0.9902	0.9815
	C8T28SOIDV_LL_-SDFPQX29_P10		**C8T28SOIDV_LL_-SDFPQX29_P10**	
CP to Q ↓	0.0648		0.4752	
CP to Q ↑	0.0782		0.6569	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P10	C8T28SOI_-LLHF_-SDFPQX3_P10	C8T28SOIDV_-LL_SDFPQX5_-P10	C8T28SOIDV_-LL_SDFPQX10_-P10
CP ↓	min_pulse_width to CP	0.0718	0.0715	0.0622	0.0604
CP ↑	min_pulse_width to CP	0.0375	0.0318	0.0362	0.0348
D ↓	hold_rising to CP	-0.0267	-0.0626	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0045	-0.0025	0.0058	0.0058
D ↓	setup_rising to CP	0.0587	0.0995	0.0369	0.0369
D ↑	setup_rising to CP	0.0288	0.0320	0.0223	0.0223
TE ↓	hold_rising to CP	-0.0159	-0.0181	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0018	0.0008	-0.0017	-0.0017
TE ↓	setup_rising to CP	0.0533	0.0774	0.0344	0.0344
TE ↑	setup_rising to CP	0.0716	0.0901	0.0689	0.0689

TI ↓	hold_rising to CP	-0.0413	-0.0605	-0.0313	-0.0329
TI ↑	hold_rising to CP	-0.0028	0.0027	-0.0043	-0.0043
TI ↓	setup_rising to CP	0.0711	0.0901	0.0675	0.0675
TI ↑	setup_rising to CP	0.0286	0.0264	0.0284	0.0284
		C8T28SOIDV_-LL_SDFPQX19_-P10	C8T28SOIDV_-LL_SDFPQX23_-P10	C8T28SOIDV_-LL_SDFPQX29_-P10	
CP ↓	min_pulse_width to CP	0.0604	0.0604	0.0628	
CP ↑	min_pulse_width to CP	0.0348	0.0348	0.0362	
D ↓	hold_rising to CP	-0.0023	-0.0023	-0.0023	
D ↑	hold_rising to CP	0.0058	0.0058	0.0058	
D ↓	setup_rising to CP	0.0369	0.0369	0.0396	
D ↑	setup_rising to CP	0.0223	0.0223	0.0223	
TE ↓	hold_rising to CP	-0.0001	-0.0001	-0.0001	
TE ↑	hold_rising to CP	-0.0017	-0.0017	-0.0023	
TE ↓	setup_rising to CP	0.0344	0.0344	0.0344	
TE ↑	setup_rising to CP	0.0689	0.0689	0.0715	
TI ↓	hold_rising to CP	-0.0313	-0.0313	-0.0329	
TI ↑	hold_rising to CP	-0.0043	-0.0043	-0.0043	
TI ↓	setup_rising to CP	0.0675	0.0675	0.0675	
TI ↑	setup_rising to CP	0.0284	0.0286	0.0286	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P10	7.732e-05	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P10	6.824e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P10	7.296e-05	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P10	1.002e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P10	1.246e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P10	1.309e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P10	1.641e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P10	C8T28SOI_LLHF_-SDFPQX3_P10	C8T28SOIDV_LL_-SDFPQX5_P10	C8T28SOIDV_LL_-SDFPQX10_P10
Clock 100Mhz Data 0Mhz	1.015e-02	9.718e-03	9.308e-03	9.099e-03
Clock 100Mhz Data 25Mhz	9.926e-03	9.484e-03	9.246e-03	9.681e-03
Clock 100Mhz Data 50Mhz	9.699e-03	9.250e-03	9.184e-03	1.026e-02

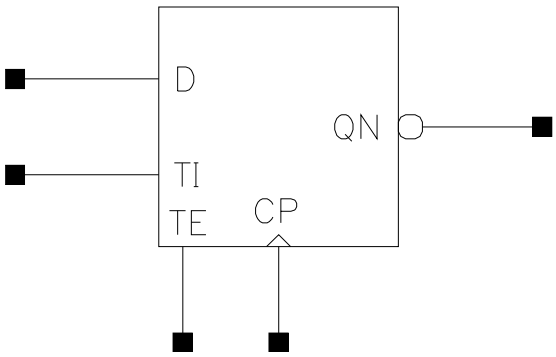
Clock = 0 Data 100Mhz	5.164e-03	5.396e-03	5.095e-03	4.941e-03
Clock = 1 Data 100Mhz	3.532e-05	6.409e-04	4.401e-04	3.397e-04
	C8T28SOIDV_LL_-SDFPQX19_P10	C8T28SOIDV_LL_-SDFPQX23_P10	C8T28SOIDV_LL_-SDFPQX29_P10	
Clock 100Mhz Data 0Mhz	8.977e-03	8.897e-03	8.840e-03	
Clock 100Mhz Data 25Mhz	1.051e-02	1.056e-02	1.131e-02	
Clock 100Mhz Data 50Mhz	1.205e-02	1.223e-02	1.379e-02	
Clock = 0 Data 100Mhz	4.847e-03	4.784e-03	4.742e-03	
Clock = 1 Data 100Mhz	2.795e-04	2.394e-04	2.108e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P10	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P10	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P10	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P10	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P10	C8T28SOI_LLHF_-SDFPQNX3_P10	C8T28SOIDV_LL_-SDFPQNX5_P10	C8T28SOIDV_LL_-SDFPQNX10_P10

CP	0.0008	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P10	C8T28SOIDV_LL_-SDFPQNX29_P10		
CP	0.0006	0.0006		
D	0.0006	0.0006		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P10	**C8T28SOI_LLHF_-SDFPQNX3_P10**	**C8T28SOI_LL_-SDFPQNX5_P10**	**C8T28SOI_LLHF_-SDFPQNX3_P10**
CP to QN ↓	0.0593	0.0625	2.8525	4.2168
CP to QN ↑	0.0516	0.0489	4.2458	5.7247
	C8T28SOIDV_LL_-SDFPQNX5_P10	**C8T28SOIDV_LL_-SDFPQNX10_P10**	**C8T28SOIDV_LL_-SDFPQNX5_P10**	**C8T28SOIDV_LL_-SDFPQNX10_P10**
CP to QN ↓	0.0653	0.0624	2.7592	1.3762
CP to QN ↑	0.0489	0.0530	3.8664	1.9594
	C8T28SOIDV_LL_-SDFPQNX19_P10	**C8T28SOIDV_LL_-SDFPQNX29_P10**	**C8T28SOIDV_LL_-SDFPQNX19_P10**	**C8T28SOIDV_LL_-SDFPQNX29_P10**
CP to QN ↓	0.0710	0.0823	0.7161	0.4897
CP to QN ↑	0.0630	0.0710	1.0065	0.6605

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P10	C8T28SOI_-LLHF_-SDFPQNX3_P10	C8T28SOIDV_-LL_SDFPQNX5_-P10	C8T28SOIDV_-LL_-SDFPQNX10_-P10
CP ↓	min_pulse_width to CP	0.0718	0.0680	0.0622	0.0622
CP ↑	min_pulse_width to CP	0.0315	0.0284	0.0348	0.0362
D ↓	hold_rising to CP	-0.0267	-0.0626	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0045	-0.0025	0.0058	0.0058
D ↓	setup_rising to CP	0.0587	0.0969	0.0364	0.0364
D ↑	setup_rising to CP	0.0288	0.0320	0.0223	0.0223
TE ↓	hold_rising to CP	-0.0186	-0.0181	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0018	0.0008	-0.0027	-0.0017
TE ↓	setup_rising to CP	0.0533	0.0780	0.0344	0.0344
TE ↑	setup_rising to CP	0.0716	0.0901	0.0689	0.0715
TI ↓	hold_rising to CP	-0.0413	-0.0605	-0.0329	-0.0329
TI ↑	hold_rising to CP	-0.0028	0.0027	-0.0031	-0.0043
TI ↓	setup_rising to CP	0.0711	0.0901	0.0675	0.0675

TI ↑	setup_rising to CP	0.0286	0.0264	0.0278	0.0284
		C8T28SOIDV_-LL_-SDFPQNX19_-P10	C8T28SOIDV_-LL_-SDFPQNX29_-P10		
CP ↓	min_pulse_width to CP	0.0622	0.0622		
CP ↑	min_pulse_width to CP	0.0394	0.0348		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0058	0.0058		
D ↓	setup_rising to CP	0.0364	0.0364		
D ↑	setup_rising to CP	0.0223	0.0223		
TE ↓	hold_rising to CP	-0.0001	-0.0001		
TE ↑	hold_rising to CP	-0.0023	-0.0017		
TE ↓	setup_rising to CP	0.0344	0.0344		
TE ↑	setup_rising to CP	0.0689	0.0683		
TI ↓	hold_rising to CP	-0.0313	-0.0329		
TI ↑	hold_rising to CP	-0.0043	-0.0043		
TI ↓	setup_rising to CP	0.0675	0.0675		
TI ↑	setup_rising to CP	0.0284	0.0284		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P10	7.640e-05	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P10	6.906e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P10	7.367e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P10	9.863e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P10	1.251e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P10	1.864e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P10	C8T28SOI_LLHF_-SDFPQNX3_P10	C8T28SOIDV_LL_-SDFPQNX5_P10	C8T28SOIDV_LL_-SDFPQNX10_P10
Clock 100Mhz Data 0Mhz	1.015e-02	9.822e-03	9.391e-03	9.158e-03
Clock 100Mhz Data 25Mhz	9.799e-03	9.558e-03	9.190e-03	9.683e-03
Clock 100Mhz Data 50Mhz	9.444e-03	9.294e-03	8.989e-03	1.021e-02
Clock = 0 Data 100Mhz	5.164e-03	5.416e-03	5.114e-03	4.956e-03
Clock = 1 Data 100Mhz	3.558e-05	6.440e-04	4.421e-04	3.412e-04

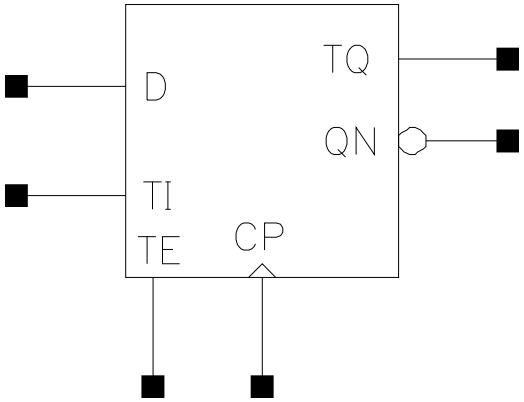
	C8T28SOIDV_LL_-SDFPQNX19_P10	C8T28SOIDV_LL_-SDFPQNX29_P10		
Clock 100Mhz Data 0Mhz	9.024e-03	8.931e-03		
Clock 100Mhz Data 25Mhz	1.078e-02	1.193e-02		
Clock 100Mhz Data 50Mhz	1.253e-02	1.492e-02		
Clock = 0 Data 100Mhz	4.857e-03	4.795e-03		
Clock = 1 Data 100Mhz	2.807e-04	2.404e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P10	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P10	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P10	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P10	C8T28SOI_LLHF_-SDFPQNTX3_P10	C8T28SOIDV_LL_-SDFPQNTX5_P10	C8T28SOIDV_LL_-SDFPQNTX10_P10
CP	0.0008	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P10	C8T28SOIDV_LL_-SDFPQNTX29_P10		
CP	0.0006	0.0006		
D	0.0006	0.0006		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNTX5_P10	**C8T28SOI_LLHF_-SDFPQNTX3_P10**	**C8T28SOI_LL_-SDFPQNTX5_P10**	**C8T28SOI_LLHF_-SDFPQNTX3_P10**
CP to QN ↓	0.0673	0.0684	2.9475	4.2793
CP to QN ↑	0.0654	0.0596	4.2479	5.7425
CP to TQ ↓	0.0527	0.0415	7.2237	4.9289
CP to TQ ↑	0.0568	0.0513	17.5355	9.7341
	C8T28SOIDV_LL_-SDFPQNTX5_P10	**C8T28SOIDV_LL_-SDFPQNTX10_P10**	**C8T28SOIDV_LL_-SDFPQNTX5_P10**	**C8T28SOIDV_LL_-SDFPQNTX10_P10**
CP to QN ↓	0.0702	0.0691	2.7147	1.3850
CP to QN ↑	0.0571	0.0578	3.8672	1.9655
CP to TQ ↓	0.0398	0.0413	4.9123	5.1116
CP to TQ ↑	0.0527	0.0539	7.8953	8.2097
	C8T28SOIDV_LL_-SDFPQNTX19_P10	**C8T28SOIDV_LL_-SDFPQNTX29_P10**	**C8T28SOIDV_LL_-SDFPQNTX19_P10**	**C8T28SOIDV_LL_-SDFPQNTX29_P10**
CP to QN ↓	0.0719	0.0846	0.7134	0.4916
CP to QN ↑	0.0633	0.0755	0.9981	0.6598
CP to TQ ↓	0.0430	0.0416	5.0231	5.1573
CP to TQ ↑	0.0557	0.0559	8.3878	10.3910

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_-P10	C8T28SOI_-LLHF_-SDFPQNTX3_-P10	C8T28SOIDV_-LL_-SDFPQNTX5_-P10	C8T28SOIDV_-LL_-SDFPQNTX10_-P10
CP ↓	min_pulse_width to CP	0.0718	0.0680	0.0622	0.0622
CP ↑	min_pulse_width to CP	0.0410	0.0365	0.0362	0.0362
D ↓	hold_rising to CP	-0.0267	-0.0630	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0040	-0.0025	0.0058	0.0058
D ↓	setup_rising to CP	0.0587	0.0974	0.0396	0.0369

D ↑	setup_rising to CP	0.0288	0.0320	0.0223	0.0223
TE ↓	hold_rising to CP	-0.0186	-0.0213	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0018	-0.0014	-0.0027	-0.0017
TE ↓	setup_rising to CP	0.0533	0.0780	0.0344	0.0344
TE ↑	setup_rising to CP	0.0716	0.0905	0.0683	0.0689
TI ↓	hold_rising to CP	-0.0370	-0.0589	-0.0329	-0.0313
TI ↑	hold_rising to CP	-0.0028	0.0027	-0.0031	-0.0043
TI ↓	setup_rising to CP	0.0711	0.0903	0.0675	0.0675
TI ↑	setup_rising to CP	0.0286	0.0280	0.0278	0.0284
		C8T28SOIDV_-LL_-SDFPQNTX19_-P10	C8T28SOIDV_-LL_-SDFPQNTX29_-P10		
CP ↓	min_pulse_width to CP	0.0622	0.0622		
CP ↑	min_pulse_width to CP	0.0408	0.0362		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0058	0.0058		
D ↓	setup_rising to CP	0.0364	0.0396		
D ↑	setup_rising to CP	0.0223	0.0223		
TE ↓	hold_rising to CP	-0.0001	-0.0001		
TE ↑	hold_rising to CP	-0.0017	-0.0017		
TE ↓	setup_rising to CP	0.0344	0.0344		
TE ↑	setup_rising to CP	0.0683	0.0683		
TI ↓	hold_rising to CP	-0.0313	-0.0329		
TI ↑	hold_rising to CP	-0.0043	-0.0043		
TI ↓	setup_rising to CP	0.0675	0.0675		
TI ↑	setup_rising to CP	0.0284	0.0284		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P10	7.712e-05	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P10	7.386e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P10	7.876e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P10	9.382e-05	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P10	1.241e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P10	1.885e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

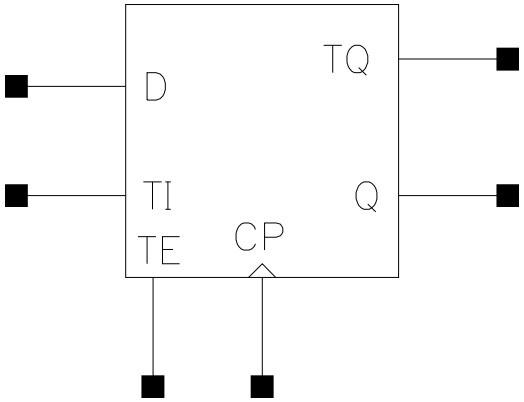
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P10	C8T28SOI_LLHF_-SDFPQNTX3_P10	C8T28SOIDV_LL_-SDFPQNTX5_P10	C8T28SOIDV_LL_-SDFPQNTX10_P10
Clock 100Mhz Data 0Mhz	1.016e-02	9.821e-03	9.383e-03	9.154e-03
Clock 100Mhz Data 25Mhz	1.022e-02	9.888e-03	9.497e-03	9.695e-03
Clock 100Mhz Data 50Mhz	1.029e-02	9.954e-03	9.610e-03	1.024e-02
Clock = 0 Data 100Mhz	5.169e-03	5.418e-03	5.119e-03	4.960e-03
Clock = 1 Data 100Mhz	3.563e-05	6.482e-04	4.450e-04	3.434e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P10	C8T28SOIDV_LL_-SDFPQNTX29_P10		
Clock 100Mhz Data 0Mhz	9.018e-03	8.921e-03		
Clock 100Mhz Data 25Mhz	1.064e-02	1.219e-02		
Clock 100Mhz Data 50Mhz	1.226e-02	1.547e-02		
Clock = 0 Data 100Mhz	4.864e-03	4.801e-03		
Clock = 1 Data 100Mhz	2.825e-04	2.419e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P10	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P10	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P10	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P10	C8T28SOI_LLHF_-SDFPQTX3_P10	C8T28SOIDV_LL_-SDFPQTX5_P10	C8T28SOIDV_LL_-SDFPQTX10_P10
CP	0.0008	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P10	C8T28SOIDV_LL_-SDFPQTX29_P10		
CP	0.0006	0.0006		
D	0.0006	0.0006		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQTX5_P10	**C8T28SOI_LLHF_-SDFPQTX3_P10**	**C8T28SOI_LL_-SDFPQTX5_P10**	**C8T28SOI_LLHF_-SDFPQTX3_P10**
CP to Q ↓	0.0562	0.0510	3.1045	4.6122
CP to Q ↑	0.0508	0.0529	3.9816	5.9742
CP to TQ ↓	0.0637	0.0491	7.8911	5.0878
CP to TQ ↑	0.0629	0.0557	17.7554	9.8985
	C8T28SOIDV_LL_-SDFPQTX5_P10	**C8T28SOIDV_LL_-SDFPQTX10_P10**	**C8T28SOIDV_LL_-SDFPQTX5_P10**	**C8T28SOIDV_LL_-SDFPQTX10_P10**
CP to Q ↓	0.0467	0.0619	2.8700	1.3716
CP to Q ↑	0.0552	0.0779	3.9653	1.9613
CP to TQ ↓	0.0457	0.0636	5.0618	5.1438
CP to TQ ↑	0.0568	0.0808	8.5973	8.4901
	C8T28SOIDV_LL_-SDFPQTX19_P10	**C8T28SOIDV_LL_-SDFPQTX29_P10**	**C8T28SOIDV_LL_-SDFPQTX19_P10**	**C8T28SOIDV_LL_-SDFPQTX29_P10**
CP to Q ↓	0.0675	0.0731	0.7117	0.4647
CP to Q ↑	0.0825	0.0822	0.9924	0.6555
CP to TQ ↓	0.0698	0.0436	5.1949	5.2964
CP to TQ ↑	0.0869	0.0570	8.5210	10.3952

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P10	C8T28SOI_-LLHF_-SDFPQTX3_P10	C8T28SOIDV_-LL_SDFPQTX5_-P10	C8T28SOIDV_-LL_-SDFPQTX10_-P10
CP ↓	min_pulse_width to CP	0.0718	0.0680	0.0622	0.0604
CP ↑	min_pulse_width to CP	0.0456	0.0412	0.0409	0.0348
D ↓	hold_rising to CP	-0.0267	-0.0626	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0049	-0.0025	0.0058	0.0058
D ↓	setup_rising to CP	0.0587	0.0969	0.0369	0.0369

D ↑	setup_rising to CP	0.0288	0.0320	0.0223	0.0223
TE ↓	hold_rising to CP	-0.0186	-0.0181	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0018	0.0008	-0.0017	-0.0017
TE ↓	setup_rising to CP	0.0533	0.0780	0.0344	0.0344
TE ↑	setup_rising to CP	0.0716	0.0905	0.0689	0.0689
TI ↓	hold_rising to CP	-0.0413	-0.0605	-0.0329	-0.0329
TI ↑	hold_rising to CP	-0.0028	0.0027	-0.0043	-0.0043
TI ↓	setup_rising to CP	0.0711	0.0903	0.0675	0.0675
TI ↑	setup_rising to CP	0.0286	0.0264	0.0284	0.0284
		C8T28SOIDV_-LL_-SDFPQTX19_-P10	C8T28SOIDV_-LL_-SDFPQTX29_-P10		
CP ↓	min_pulse_width to CP	0.0604	0.0622		
CP ↑	min_pulse_width to CP	0.0348	0.0408		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0058	0.0058		
D ↓	setup_rising to CP	0.0369	0.0396		
D ↑	setup_rising to CP	0.0223	0.0223		
TE ↓	hold_rising to CP	-0.0001	-0.0001		
TE ↑	hold_rising to CP	-0.0017	-0.0023		
TE ↓	setup_rising to CP	0.0344	0.0344		
TE ↑	setup_rising to CP	0.0689	0.0715		
TI ↓	hold_rising to CP	-0.0313	-0.0329		
TI ↑	hold_rising to CP	-0.0043	-0.0043		
TI ↓	setup_rising to CP	0.0675	0.0675		
TI ↑	setup_rising to CP	0.0284	0.0284		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P10	7.852e-05	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P10	7.386e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P10	7.834e-05	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P10	1.053e-04	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P10	1.310e-04	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P10	1.722e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

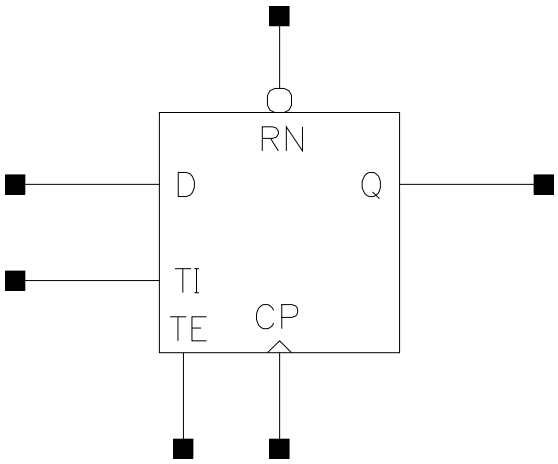
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P10	C8T28SOI_LLHF_-SDFPQTX3_P10	C8T28SOIDV_LL_-SDFPQTX5_P10	C8T28SOIDV_LL_-SDFPQTX10_P10
Clock 100Mhz Data 0Mhz	1.016e-02	9.830e-03	9.384e-03	9.156e-03
Clock 100Mhz Data 25Mhz	1.038e-02	9.965e-03	9.590e-03	9.958e-03
Clock 100Mhz Data 50Mhz	1.059e-02	1.010e-02	9.796e-03	1.076e-02
Clock = 0 Data 100Mhz	5.169e-03	5.421e-03	5.113e-03	4.954e-03
Clock = 1 Data 100Mhz	3.546e-05	6.452e-04	4.430e-04	3.419e-04
	C8T28SOIDV_LL_-SDFPQTX19_P10	C8T28SOIDV_LL_-SDFPQTX29_P10		
Clock 100Mhz Data 0Mhz	9.022e-03	8.937e-03		
Clock 100Mhz Data 25Mhz	1.085e-02	1.176e-02		
Clock 100Mhz Data 50Mhz	1.268e-02	1.459e-02		
Clock = 0 Data 100Mhz	4.857e-03	4.797e-03		
Clock = 1 Data 100Mhz	2.813e-04	2.409e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P10	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P10	C8T28SOI_LLHF_-SDFPRQX3_P10	C8T28SOIDV_LL_-SDFPRQX5_P10	C8T28SOIDV_LL_-SDFPRQX10_P10
CP	0.0008	0.0008	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0010	0.0010
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P10	C8T28SOIDV_LL_-SDFPRQX29_P10		
CP	0.0006	0.0006		
D	0.0006	0.0006		
RN	0.0010	0.0009		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P10	**C8T28SOI_LLHF_-SDFPRQX3_P10**	**C8T28SOI_LL_-SDFPRQX5_P10**	**C8T28SOI_LLHF_-SDFPRQX3_P10**
CP to Q ↓	0.0531	0.0480	2.9599	4.4880
CP to Q ↑	0.0481	0.0521	3.9580	5.8209
RN to Q ↓	0.0396	0.0368	2.8203	4.3259
	C8T28SOIDV_LL_-SDFPRQX5_P10	**C8T28SOIDV_LL_-SDFPRQX10_P10**	**C8T28SOIDV_LL_-SDFPRQX5_P10**	**C8T28SOIDV_LL_-SDFPRQX10_P10**
CP to Q ↓	0.0433	0.0616	2.8007	1.3799
CP to Q ↑	0.0554	0.0793	3.9095	1.9643
RN to Q ↓	0.0442	0.0583	2.7089	1.3795
	C8T28SOIDV_LL_-SDFPRQX19_P10	**C8T28SOIDV_LL_-SDFPRQX29_P10**	**C8T28SOIDV_LL_-SDFPRQX19_P10**	**C8T28SOIDV_LL_-SDFPRQX29_P10**
CP to Q ↓	0.0665	0.0678	0.7104	0.4843
CP to Q ↑	0.0839	0.0871	1.0058	0.6835
RN to Q ↓	0.0628	0.0644	0.7099	0.4841

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P10	C8T28SOI_-LLHF_-SDFPRQX3_P10	C8T28SOIDV_-LL_SDFPRQX5_-P10	C8T28SOIDV_-LL_-SDFPRQX10_-P10
CP ↓	min_pulse_width to CP	0.0725	0.0667	0.0635	0.0635
CP ↑	min_pulse_width to CP	0.0423	0.0365	0.0362	0.0362
D ↓	hold_rising to CP	-0.0267	-0.0572	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0040	-0.0041	0.0026	0.0026
D ↓	setup_rising to CP	0.0587	0.0974	0.0369	0.0364
D ↑	setup_rising to CP	0.0315	0.0341	0.0249	0.0249
RN ↓	min_pulse_width to RN	0.0496	0.0474	0.0469	0.0447
RN ↑	recovery_rising to CP	0.0032	0.0032	0.0032	0.0032

RN ↑	removal_rising to CP	0.0074	0.0074	0.0069	0.0042
TE ↓	hold_rising to CP	-0.0186	-0.0240	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0018	-0.0046	-0.0044	-0.0044
TE ↓	setup_rising to CP	0.0533	0.0725	0.0371	0.0371
TE ↑	setup_rising to CP	0.0716	0.0911	0.0662	0.0689
TI ↓	hold_rising to CP	-0.0377	-0.0596	-0.0313	-0.0315
TI ↑	hold_rising to CP	-0.0036	-0.0032	-0.0079	-0.0079
TI ↓	setup_rising to CP	0.0711	0.0895	0.0659	0.0659
TI ↑	setup_rising to CP	0.0326	0.0273	0.0342	0.0342
		C8T28SOIDV_-LL_-SDFPRQX19_-P10	C8T28SOIDV_-LL_-SDFPRQX29_-P10		
CP ↓	min_pulse_width to CP	0.0635	0.0635		
CP ↑	min_pulse_width to CP	0.0348	0.0363		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0026	0.0026		
D ↓	setup_rising to CP	0.0364	0.0396		
D ↑	setup_rising to CP	0.0249	0.0249		
RN ↓	min_pulse_width to RN	0.0425	0.0447		
RN ↑	recovery_rising to CP	0.0032	0.0032		
RN ↑	removal_rising to CP	0.0042	0.0069		
TE ↓	hold_rising to CP	-0.0001	-0.0001		
TE ↑	hold_rising to CP	-0.0044	-0.0044		
TE ↓	setup_rising to CP	0.0371	0.0366		
TE ↑	setup_rising to CP	0.0662	0.0689		
TI ↓	hold_rising to CP	-0.0315	-0.0313		
TI ↑	hold_rising to CP	-0.0079	-0.0079		
TI ↓	setup_rising to CP	0.0659	0.0659		
TI ↑	setup_rising to CP	0.0342	0.0342		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P10	8.312e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P10	7.513e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P10	7.962e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P10	1.052e-04	1.000e-20

C8T28SOIDV_LL_SDFPRQX19_P10	1.338e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P10	1.703e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

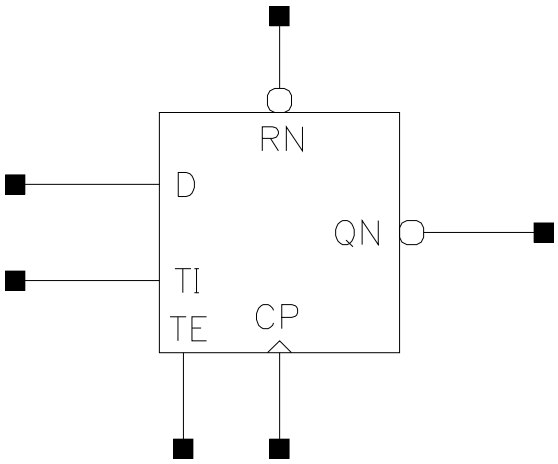
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P10	C8T28SOI_LLHF_-SDFPRQX3_P10	C8T28SOIDV_LL_-SDFPRQX5_P10	C8T28SOIDV_LL_-SDFPRQX10_P10
Clock 100Mhz Data 0Mhz	1.052e-02	1.009e-02	9.623e-03	9.391e-03
Clock 100Mhz Data 25Mhz	1.024e-02	9.844e-03	9.437e-03	9.916e-03
Clock 100Mhz Data 50Mhz	9.962e-03	9.600e-03	9.251e-03	1.044e-02
Clock = 0 Data 100Mhz	4.831e-03	5.131e-03	4.935e-03	4.839e-03
Clock = 1 Data 100Mhz	3.539e-05	6.483e-04	4.446e-04	3.428e-04
	C8T28SOIDV_LL_-SDFPRQX19_P10	C8T28SOIDV_LL_-SDFPRQX29_P10		
Clock 100Mhz Data 0Mhz	9.251e-03	9.160e-03		
Clock 100Mhz Data 25Mhz	1.072e-02	1.179e-02		
Clock 100Mhz Data 50Mhz	1.219e-02	1.442e-02		
Clock = 0 Data 100Mhz	4.780e-03	4.743e-03		
Clock = 1 Data 100Mhz	2.817e-04	2.412e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P10	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P10	C8T28SOI_LLHF_-SDFPRQNX3_P10	C8T28SOIDV_LL_-SDFPRQNX5_P10	C8T28SOIDV_LL_-SDFPRQNX10_P10
CP	0.0008	0.0007	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0010	0.0009
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P10	C8T28SOIDV_LL_-SDFPRQNX29_P10		
CP	0.0006	0.0006		
D	0.0006	0.0006		
RN	0.0008	0.0009		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNX5_P10	**C8T28SOI_LLHF_-SDFPRQNX3_P10**	**C8T28SOI_LL_-SDFPRQNX5_P10**	**C8T28SOI_LLHF_-SDFPRQNX3_P10**
CP to QN ↓	0.0624	0.0652	2.9196	4.2261
CP to QN ↑	0.0564	0.0529	4.0708	5.7197
RN to QN ↑	0.0461	0.0444	4.0661	5.7220
	C8T28SOIDV_LL_-SDFPRQNX5_P10	**C8T28SOIDV_LL_-SDFPRQNX10_P10**	**C8T28SOIDV_LL_-SDFPRQNX5_P10**	**C8T28SOIDV_LL_-SDFPRQNX10_P10**
CP to QN ↓	0.0702	0.0649	2.7080	1.3807
CP to QN ↑	0.0537	0.0535	3.8597	1.9659
RN to QN ↑	0.0501	0.0533	3.8613	1.9615
	C8T28SOIDV_LL_-SDFPRQNX19_P10	**C8T28SOIDV_LL_-SDFPRQNX29_P10**	**C8T28SOIDV_LL_-SDFPRQNX19_P10**	**C8T28SOIDV_LL_-SDFPRQNX29_P10**
CP to QN ↓	0.0726	0.0771	0.7248	0.4860
CP to QN ↑	0.0599	0.0667	1.0103	0.6803
RN to QN ↑	0.0569	0.0596	1.0087	0.6783

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P10	C8T28SOI_-LLHF_-SDFPRQNX3_-P10	C8T28SOIDV_-LL_-SDFPRQNX5_-P10	C8T28SOIDV_-LL_-SDFPRQNX10_-P10
CP ↓	min_pulse_width to CP	0.0718	0.0667	0.0635	0.0635
CP ↑	min_pulse_width to CP	0.0363	0.0318	0.0362	0.0362
D ↓	hold_rising to CP	-0.0267	-0.0572	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0040	-0.0041	0.0026	0.0026
D ↓	setup_rising to CP	0.0591	0.0942	0.0364	0.0396
D ↑	setup_rising to CP	0.0288	0.0341	0.0249	0.0249
RN ↓	min_pulse_width to RN	0.0474	0.0474	0.0447	0.0469
RN ↑	recovery_rising to CP	0.0032	0.0032	0.0032	0.0032

RN ↑	removal_rising to CP	0.0074	0.0074	0.0069	0.0048
TE ↓	hold_rising to CP	-0.0186	-0.0240	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0018	-0.0046	-0.0044	-0.0044
TE ↓	setup_rising to CP	0.0533	0.0725	0.0371	0.0371
TE ↑	setup_rising to CP	0.0716	0.0911	0.0689	0.0662
TI ↓	hold_rising to CP	-0.0370	-0.0599	-0.0313	-0.0313
TI ↑	hold_rising to CP	-0.0036	-0.0032	-0.0036	-0.0079
TI ↓	setup_rising to CP	0.0711	0.0895	0.0659	0.0659
TI ↑	setup_rising to CP	0.0326	0.0270	0.0342	0.0342
		C8T28SOIDV_-LL_-SDFPRQNX19_-P10	C8T28SOIDV_-LL_-SDFPRQNX29_-P10		
CP ↓	min_pulse_width to CP	0.0635	0.0635		
CP ↑	min_pulse_width to CP	0.0395	0.0455		
D ↓	hold_rising to CP	0.0004	0.0004		
D ↑	hold_rising to CP	0.0026	0.0026		
D ↓	setup_rising to CP	0.0396	0.0396		
D ↑	setup_rising to CP	0.0249	0.0249		
RN ↓	min_pulse_width to RN	0.0518	0.0615		
RN ↑	recovery_rising to CP	-0.0000	-0.0000		
RN ↑	removal_rising to CP	0.0069	0.0069		
TE ↓	hold_rising to CP	0.0026	0.0048		
TE ↑	hold_rising to CP	-0.0044	-0.0044		
TE ↓	setup_rising to CP	0.0371	0.0371		
TE ↑	setup_rising to CP	0.0689	0.0689		
TI ↓	hold_rising to CP	-0.0280	-0.0280		
TI ↑	hold_rising to CP	-0.0036	-0.0036		
TI ↓	setup_rising to CP	0.0659	0.0659		
TI ↑	setup_rising to CP	0.0342	0.0342		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P10	8.061e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P10	7.518e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P10	7.771e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P10	1.028e-04	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P10	1.231e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P10	1.587e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

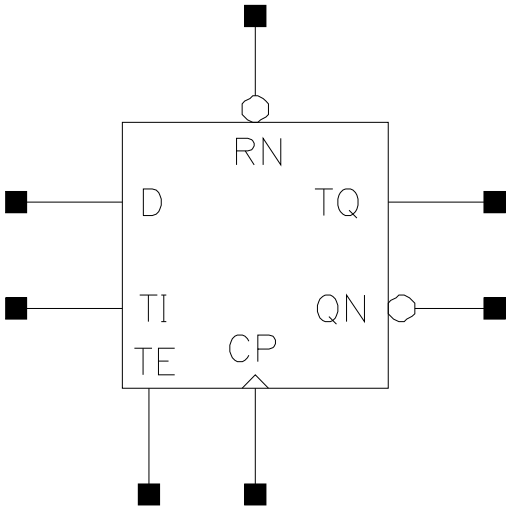
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P10	C8T28SOI_LLHF_-SDFPRQNX3_P10	C8T28SOIDV_LL_-SDFPRQNX5_P10	C8T28SOIDV_LL_-SDFPRQNX10_P10
Clock 100Mhz Data 0Mhz	1.051e-02	1.006e-02	9.611e-03	9.382e-03
Clock 100Mhz Data 25Mhz	1.009e-02	9.759e-03	9.443e-03	9.918e-03
Clock 100Mhz Data 50Mhz	9.660e-03	9.453e-03	9.276e-03	1.045e-02
Clock = 0 Data 100Mhz	4.825e-03	5.124e-03	4.936e-03	4.837e-03
Clock = 1 Data 100Mhz	3.539e-05	6.472e-04	4.439e-04	3.422e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P10	C8T28SOIDV_LL_-SDFPRQNX29_P10		
Clock 100Mhz Data 0Mhz	9.303e-03	9.279e-03		
Clock 100Mhz Data 25Mhz	1.084e-02	1.219e-02		
Clock 100Mhz Data 50Mhz	1.237e-02	1.510e-02		
Clock = 0 Data 100Mhz	4.777e-03	4.738e-03		
Clock = 1 Data 100Mhz	2.813e-04	2.407e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P10	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P10	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P10	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P10	C8T28SOI_LLHF_-SDFPRQNTX3_P10	C8T28SOIDV_LL_-SDFPRQNTX5_P10	C8T28SOIDV_LL_-SDFPRQNTX10_P10
CP	0.0008	0.0007	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0010	0.0010
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P10	C8T28SOIDV_LL_-SDFPRQNTX29_P10		
CP	0.0006	0.0006		
D	0.0006	0.0006		
RN	0.0009	0.0008		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNTX5_P10	**C8T28SOI_LLHF_-SDFPRQNTX3_P10**	**C8T28SOI_LL_-SDFPRQNTX5_P10**	**C8T28SOI_LLHF_-SDFPRQNTX3_P10**
CP to QN ↓	0.0695	0.0711	2.8661	4.2690
CP to QN ↑	0.0704	0.0639	4.2532	5.7466
CP to TQ ↓	0.0582	0.0456	7.5402	4.9639
CP to TQ ↑	0.0580	0.0536	17.5349	9.7565
RN to QN ↑	0.0563	0.0526	4.2484	5.7509
RN to TQ ↓	0.0447	0.0349	7.3628	4.8573
	C8T28SOIDV_LL_-SDFPRQNTX5_P10	**C8T28SOIDV_LL_-SDFPRQNTX10_P10**	**C8T28SOIDV_LL_-SDFPRQNTX5_P10**	**C8T28SOIDV_LL_-SDFPRQNTX10_P10**
CP to QN ↓	0.0741	0.0790	2.7406	1.4169
CP to QN ↑	0.0590	0.0629	3.8512	1.9562
CP to TQ ↓	0.0407	0.0411	4.9236	4.9573
CP to TQ ↑	0.0556	0.0556	7.9026	7.9074
RN to QN ↑	0.0583	0.0617	3.8632	1.9596
RN to TQ ↓	0.0430	0.0435	4.8206	4.8511
	C8T28SOIDV_LL_-SDFPRQNTX19_P10	**C8T28SOIDV_LL_-SDFPRQNTX29_P10**	**C8T28SOIDV_LL_-SDFPRQNTX19_P10**	**C8T28SOIDV_LL_-SDFPRQNTX29_P10**
CP to QN ↓	0.0759	0.0777	0.7138	0.4864
CP to QN ↑	0.0651	0.0723	0.9893	0.6740
CP to TQ ↓	0.0443	0.0538	4.9952	5.6431
CP to TQ ↑	0.0591	0.0662	7.9272	8.9758
RN to QN ↑	0.0604	0.0621	0.9923	0.6758
RN to TQ ↓	0.0435	0.0484	4.8763	5.4027

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P10	C8T28SOI_-LLHF_-SDFPRQNTX3_-P10	C8T28SOIDV_-LL_-SDFPRQNTX5_-P10	C8T28SOIDV_-LL_SDF-PRQNTX10_P10
CP ↓	min_pulse_width to CP	0.0718	0.0667	0.0635	0.0635
CP ↑	min_pulse_width to CP	0.0456	0.0377	0.0362	0.0362
D ↓	hold_rising to CP	-0.0267	-0.0572	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0040	-0.0041	0.0026	0.0026
D ↓	setup_rising to CP	0.0591	0.0974	0.0364	0.0396
D ↑	setup_rising to CP	0.0288	0.0341	0.0249	0.0249
RN ↓	min_pulse_width to RN	0.0518	0.0496	0.0518	0.0518
RN ↑	recovery_rising to CP	0.0032	0.0032	0.0032	0.0032
RN ↑	removal_rising to CP	0.0074	0.0074	0.0069	0.0048
TE ↓	hold_rising to CP	-0.0186	-0.0240	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0018	-0.0046	-0.0044	-0.0044
TE ↓	setup_rising to CP	0.0533	0.0725	0.0371	0.0371
TE ↑	setup_rising to CP	0.0716	0.0911	0.0689	0.0689
TI ↓	hold_rising to CP	-0.0362	-0.0596	-0.0313	-0.0315
TI ↑	hold_rising to CP	-0.0036	-0.0032	-0.0036	-0.0079
TI ↓	setup_rising to CP	0.0711	0.0895	0.0659	0.0659
TI ↑	setup_rising to CP	0.0284	0.0270	0.0342	0.0342
		C8T28SOIDV_-LL_SDF-PRQNTX19_P10	C8T28SOIDV_-LL_SDF-PRQNTX29_P10		
CP ↓	min_pulse_width to CP	0.0635	0.0635		
CP ↑	min_pulse_width to CP	0.0408	0.0468		
D ↓	hold_rising to CP	0.0004	0.0004		
D ↑	hold_rising to CP	0.0026	0.0026		
D ↓	setup_rising to CP	0.0396	0.0396		
D ↑	setup_rising to CP	0.0249	0.0249		
RN ↓	min_pulse_width to RN	0.0566	0.0637		
RN ↑	recovery_rising to CP	-0.0000	-0.0000		
RN ↑	removal_rising to CP	0.0069	0.0069		
TE ↓	hold_rising to CP	0.0021	0.0026		
TE ↑	hold_rising to CP	-0.0044	-0.0044		

TE ↓	setup_rising to CP	0.0371	0.0371		
TE ↑	setup_rising to CP	0.0689	0.0689		
TI ↓	hold_rising to CP	-0.0280	-0.0280		
TI ↑	hold_rising to CP	-0.0036	-0.0036		
TI ↓	setup_rising to CP	0.0659	0.0659		
TI ↑	setup_rising to CP	0.0342	0.0342		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P10	8.125e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P10	7.941e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P10	8.324e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_P10	9.378e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_P10	1.235e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_P10	1.632e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

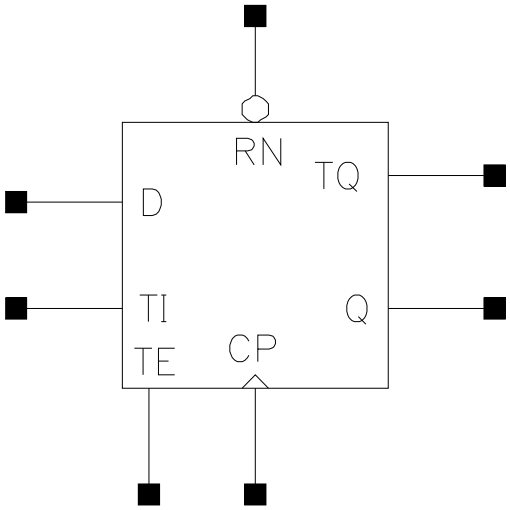
Pin Cycle	C8T28SOI_LL_SDFPRQNTX5_P10	C8T28SOI_LLHF_SDFPRQNTX3_P10	C8T28SOIDV_LL_SDFPRQNTX5_P10	C8T28SOIDV_LL_SDFPRQNTX10_P10
Clock 100Mhz Data 0Mhz	1.053e-02	1.007e-02	9.631e-03	9.398e-03
Clock 100Mhz Data 25Mhz	1.049e-02	1.010e-02	9.730e-03	1.002e-02
Clock 100Mhz Data 50Mhz	1.046e-02	1.012e-02	9.829e-03	1.065e-02
Clock = 0 Data 100Mhz	4.806e-03	5.121e-03	4.937e-03	4.839e-03
Clock = 1 Data 100Mhz	3.508e-05	6.500e-04	4.458e-04	3.437e-04
	C8T28SOIDV_LL_SDFPRQNTX19_P10	C8T28SOIDV_LL_SDFPRQNTX29_P10		
Clock 100Mhz Data 0Mhz	9.318e-03	9.255e-03		
Clock 100Mhz Data 25Mhz	1.090e-02	1.253e-02		
Clock 100Mhz Data 50Mhz	1.248e-02	1.580e-02		
Clock = 0 Data 100Mhz	4.780e-03	4.742e-03		
Clock = 1 Data 100Mhz	2.825e-04	2.418e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P10	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P10	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P10	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P10	C8T28SOI_LLHF_-SDFPRQTX3_P10	C8T28SOIDV_LL_-SDFPRQTX5_P10	C8T28SOIDV_LL_-SDFPRQTX10_P10
CP	0.0008	0.0007	0.0006	0.0006
D	0.0005	0.0006	0.0006	0.0006
RN	0.0009	0.0009	0.0010	0.0009
TE	0.0011	0.0010	0.0010	0.0010
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P10	C8T28SOIDV_LL_-SDFPRQTX29_P10		
CP	0.0006	0.0006		
D	0.0006	0.0006		
RN	0.0010	0.0009		
TE	0.0010	0.0010		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPRQTX5_P10	**C8T28SOI_LLHF_-SDFPRQTX3_P10**	**C8T28SOI_LL_-SDFPRQTX5_P10**	**C8T28SOI_LLHF_-SDFPRQTX3_P10**
CP to Q ↓	0.0630	0.0538	3.1487	4.6334
CP to Q ↑	0.0523	0.0547	3.9873	5.9760
CP to TQ ↓	0.0705	0.0516	7.9529	5.1124
CP to TQ ↑	0.0644	0.0573	17.5824	9.9045
RN to Q ↓	0.0466	0.0416	2.9560	4.4252
RN to TQ ↓	0.0542	0.0397	7.6591	4.9418
	C8T28SOIDV_LL_-SDFPRQTX5_P10	**C8T28SOIDV_LL_-SDFPRQTX10_P10**	**C8T28SOIDV_LL_-SDFPRQTX5_P10**	**C8T28SOIDV_LL_-SDFPRQTX10_P10**
CP to Q ↓	0.0471	0.0630	2.8895	1.4017
CP to Q ↑	0.0575	0.0804	3.9478	1.9623
CP to TQ ↓	0.0469	0.0649	5.0618	4.9411
CP to TQ ↑	0.0594	0.0834	8.0241	7.9612
RN to Q ↓	0.0460	0.0590	2.7791	1.4016
RN to TQ ↓	0.0462	0.0609	4.9330	4.9399
	C8T28SOIDV_LL_-SDFPRQTX19_P10	**C8T28SOIDV_LL_-SDFPRQTX29_P10**	**C8T28SOIDV_LL_-SDFPRQTX19_P10**	**C8T28SOIDV_LL_-SDFPRQTX29_P10**
CP to Q ↓	0.0705	0.0685	0.7350	0.4922
CP to Q ↑	0.0863	0.0875	0.9962	0.6796
CP to TQ ↓	0.0731	0.0698	4.9949	4.9074
CP to TQ ↑	0.0907	0.0914	7.9596	8.1505
RN to Q ↓	0.0675	0.0651	0.7352	0.4922
RN to TQ ↓	0.0701	0.0664	4.9941	4.9080

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_-P10	C8T28SOI_-LLHF_-SDFPRQTX3_-P10	C8T28SOIDV_-LL_-SDFPRQTX5_-P10	C8T28SOIDV_-LL_-SDFPRQTX10_-P10
CP ↓	min_pulse_width to CP	0.0718	0.0667	0.0635	0.0635
CP ↑	min_pulse_width to CP	0.0517	0.0424	0.0402	0.0348
D ↓	hold_rising to CP	-0.0267	-0.0572	-0.0023	-0.0023
D ↑	hold_rising to CP	-0.0040	-0.0041	0.0026	0.0026
D ↓	setup_rising to CP	0.0591	0.0974	0.0396	0.0364
D ↑	setup_rising to CP	0.0288	0.0341	0.0249	0.0249
RN ↓	min_pulse_width to RN	0.0566	0.0518	0.0518	0.0425
RN ↑	recovery_rising to CP	0.0032	0.0032	0.0032	0.0032
RN ↑	removal_rising to CP	0.0074	0.0047	0.0069	0.0069
TE ↓	hold_rising to CP	-0.0186	-0.0240	-0.0001	-0.0001
TE ↑	hold_rising to CP	-0.0018	-0.0046	-0.0044	-0.0044
TE ↓	setup_rising to CP	0.0533	0.0758	0.0371	0.0371
TE ↑	setup_rising to CP	0.0716	0.0911	0.0689	0.0662
TI ↓	hold_rising to CP	-0.0362	-0.0596	-0.0313	-0.0315
TI ↑	hold_rising to CP	-0.0036	-0.0032	-0.0079	-0.0079
TI ↓	setup_rising to CP	0.0711	0.0895	0.0659	0.0659
TI ↑	setup_rising to CP	0.0326	0.0270	0.0342	0.0342
		C8T28SOIDV_-LL_-SDFPRQTX19_-P10	C8T28SOIDV_-LL_-SDFPRQTX29_-P10		
CP ↓	min_pulse_width to CP	0.0635	0.0635		
CP ↑	min_pulse_width to CP	0.0362	0.0363		
D ↓	hold_rising to CP	-0.0023	-0.0023		
D ↑	hold_rising to CP	0.0026	0.0026		
D ↓	setup_rising to CP	0.0396	0.0396		
D ↑	setup_rising to CP	0.0249	0.0249		
RN ↓	min_pulse_width to RN	0.0447	0.0447		
RN ↑	recovery_rising to CP	0.0032	0.0032		
RN ↑	removal_rising to CP	0.0069	0.0069		
TE ↓	hold_rising to CP	-0.0001	-0.0001		
TE ↑	hold_rising to CP	-0.0044	-0.0044		

TE ↓	setup_rising to CP	0.0371	0.0371		
TE ↑	setup_rising to CP	0.0689	0.0689		
TI ↓	hold_rising to CP	-0.0315	-0.0313		
TI ↑	hold_rising to CP	-0.0079	-0.0079		
TI ↓	setup_rising to CP	0.0659	0.0659		
TI ↑	setup_rising to CP	0.0342	0.0342		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P10	8.452e-05	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P10	7.962e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P10	8.519e-05	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P10	1.106e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P10	1.373e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P10	1.757e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

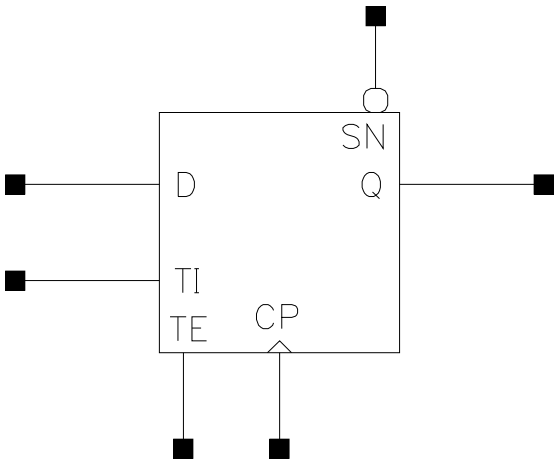
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P10	C8T28SOI_LLHF_-SDFPRQTX3_P10	C8T28SOIDV_LL_-SDFPRQTX5_P10	C8T28SOIDV_LL_-SDFPRQTX10_P10
Clock 100Mhz Data 0Mhz	1.053e-02	1.008e-02	9.621e-03	9.390e-03
Clock 100Mhz Data 25Mhz	1.069e-02	1.016e-02	9.733e-03	1.021e-02
Clock 100Mhz Data 50Mhz	1.086e-02	1.024e-02	9.845e-03	1.103e-02
Clock = 0 Data 100Mhz	4.814e-03	5.128e-03	4.935e-03	4.838e-03
Clock = 1 Data 100Mhz	3.538e-05	6.506e-04	4.461e-04	3.440e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P10	C8T28SOIDV_LL_-SDFPRQTX29_P10		
Clock 100Mhz Data 0Mhz	9.252e-03	9.160e-03		
Clock 100Mhz Data 25Mhz	1.108e-02	1.199e-02		
Clock 100Mhz Data 50Mhz	1.290e-02	1.483e-02		
Clock = 0 Data 100Mhz	4.781e-03	4.744e-03		
Clock = 1 Data 100Mhz	2.827e-04	2.420e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P10	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P10	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P10	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P10	C8T28SOI_LLHF_-SDFPSQX3_P10	C8T28SOIDV_LL_-SDFPSQX5_P10	C8T28SOIDV_LL_-SDFPSQX10_P10
CP	0.0008	0.0008	0.0006	0.0006
D	0.0003	0.0005	0.0004	0.0004
SN	0.0015	0.0014	0.0011	0.0011
TE	0.0011	0.0010	0.0011	0.0011
TI	0.0004	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQX14_P10	C8T28SOIDV_LL_-SDFPSQX19_P10	C8T28SOIDV_LL_-SDFPSQX29_P10	
CP	0.0006	0.0006	0.0006	
D	0.0004	0.0004	0.0004	
SN	0.0011	0.0011	0.0011	
TE	0.0011	0.0011	0.0011	
TI	0.0005	0.0005	0.0005	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P10	**C8T28SOI_LLHF_-SDFPSQX3_P10**	**C8T28SOI_LL_-SDFPSQX5_P10**	**C8T28SOI_LLHF_-SDFPSQX3_P10**
CP to Q ↓	0.0550	0.0485	3.0178	4.5481
CP to Q ↑	0.0493	0.0531	3.9801	5.8373
SN to Q ↑	0.0331	0.0310	3.9036	5.7496
	C8T28SOIDV_LL_-SDFPSQX5_P10	**C8T28SOIDV_LL_-SDFPSQX10_P10**	**C8T28SOIDV_LL_-SDFPSQX5_P10**	**C8T28SOIDV_LL_-SDFPSQX10_P10**
CP to Q ↓	0.0427	0.0619	2.7969	1.3530
CP to Q ↑	0.0528	0.0840	3.9023	1.9539
SN to Q ↑	0.0307	0.0591	3.8703	1.9537
	C8T28SOIDV_LL_-SDFPSQX14_P10	**C8T28SOIDV_LL_-SDFPSQX19_P10**	**C8T28SOIDV_LL_-SDFPSQX14_P10**	**C8T28SOIDV_LL_-SDFPSQX19_P10**
CP to Q ↓	0.0627	0.0669	0.9332	0.7225
CP to Q ↑	0.0843	0.0876	1.3122	0.9890
SN to Q ↑	0.0595	0.0629	1.3119	0.9886
	C8T28SOIDV_LL_-SDFPSQX29_P10		**C8T28SOIDV_LL_-SDFPSQX29_P10**	
CP to Q ↓	0.0668		0.4890	
CP to Q ↑	0.0914		0.6568	
SN to Q ↑	0.0664		0.6568	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P10	C8T28SOI_-LLHF_-SDFPSQX3_P10	C8T28SOIDV_-LL_SDFPSQX5_-P10	C8T28SOIDV_-LL_-SDFPSQX10_-P10
CP ↓	min_pulse_width to CP	0.0779	0.0775	0.0676	0.0677
CP ↑	min_pulse_width to CP	0.0456	0.0377	0.0362	0.0355
D ↓	hold_rising to CP	-0.0316	-0.0675	-0.0072	-0.0120
D ↑	hold_rising to CP	-0.0050	-0.0025	0.0026	0.0026
D ↓	setup_rising to CP	0.0662	0.1072	0.0467	0.0493
D ↑	setup_rising to CP	0.0293	0.0320	0.0249	0.0244

SN ↓	min_pulse_width to SN	0.0403	0.0354	0.0354	0.0354
SN ↑	recovery_rising to CP	0.0032	0.0032	-0.0043	-0.0039
SN ↑	removal_rising to CP	0.0189	0.0212	0.0286	0.0286
TE ↓	hold_rising to CP	-0.0159	-0.0181	-0.0050	-0.0098
TE ↑	hold_rising to CP	-0.0024	0.0008	0.0021	-0.0027
TE ↓	setup_rising to CP	0.0640	0.0877	0.0445	0.0441
TE ↑	setup_rising to CP	0.0755	0.1008	0.0715	0.0715
TI ↓	hold_rising to CP	-0.0462	-0.0654	-0.0329	-0.0315
TI ↑	hold_rising to CP	-0.0030	0.0027	0.0033	-0.0030
TI ↓	setup_rising to CP	0.0765	0.0992	0.0710	0.0659
TI ↑	setup_rising to CP	0.0278	0.0264	0.0231	0.0293
		C8T28SOIDV_-LL_-SDFPSQX14_-P10	C8T28SOIDV_-LL_-SDFPSQX19_-P10	C8T28SOIDV_-LL_-SDFPSQX29_-P10	
CP ↓	min_pulse_width to CP	0.0677	0.0677	0.0677	
CP ↑	min_pulse_width to CP	0.0349	0.0349	0.0363	
D ↓	hold_rising to CP	-0.0120	-0.0120	-0.0120	
D ↑	hold_rising to CP	0.0026	0.0026	0.0026	
D ↓	setup_rising to CP	0.0493	0.0493	0.0493	
D ↑	setup_rising to CP	0.0244	0.0244	0.0244	
SN ↓	min_pulse_width to SN	0.0354	0.0354	0.0354	
SN ↑	recovery_rising to CP	-0.0071	-0.0071	-0.0039	
SN ↑	removal_rising to CP	0.0286	0.0286	0.0286	
TE ↓	hold_rising to CP	-0.0098	-0.0098	-0.0098	
TE ↑	hold_rising to CP	-0.0027	-0.0027	-0.0027	
TE ↓	setup_rising to CP	0.0441	0.0441	0.0441	
TE ↑	setup_rising to CP	0.0715	0.0715	0.0715	
TI ↓	hold_rising to CP	-0.0315	-0.0315	-0.0315	
TI ↑	hold_rising to CP	-0.0030	-0.0030	-0.0030	
TI ↓	setup_rising to CP	0.0659	0.0659	0.0659	
TI ↑	setup_rising to CP	0.0293	0.0278	0.0293	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds

C8T28SOI_LL_SDFPSQX5_P10	8.316e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQX3_P10	7.722e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P10	8.017e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P10	1.075e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P10	1.197e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P10	1.334e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P10	1.657e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

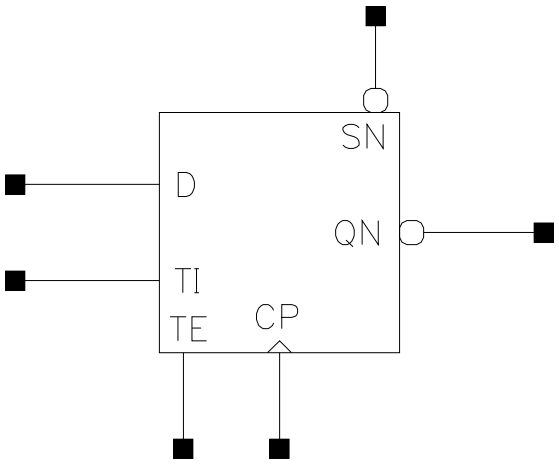
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P10	C8T28SOI_LLHF_-SDFPSQX3_P10	C8T28SOIDV_LL_-SDFPSQX5_P10	C8T28SOIDV_LL_-SDFPSQX10_P10
Clock 100Mhz Data 0Mhz	1.036e-02	9.826e-03	9.407e-03	9.190e-03
Clock 100Mhz Data 25Mhz	1.030e-02	9.728e-03	9.249e-03	9.873e-03
Clock 100Mhz Data 50Mhz	1.025e-02	9.630e-03	9.091e-03	1.056e-02
Clock = 0 Data 100Mhz	4.955e-03	5.270e-03	5.122e-03	5.079e-03
Clock = 1 Data 100Mhz	3.515e-05	6.444e-04	4.423e-04	3.415e-04
	C8T28SOIDV_LL_-SDFPSQX14_P10	C8T28SOIDV_LL_-SDFPSQX19_P10	C8T28SOIDV_LL_-SDFPSQX29_P10	
Clock 100Mhz Data 0Mhz	9.060e-03	8.973e-03	8.911e-03	
Clock 100Mhz Data 25Mhz	1.012e-02	1.068e-02	1.148e-02	
Clock 100Mhz Data 50Mhz	1.119e-02	1.240e-02	1.405e-02	
Clock = 0 Data 100Mhz	5.053e-03	5.036e-03	5.024e-03	
Clock = 1 Data 100Mhz	2.811e-04	2.408e-04	2.121e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P10	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P10	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P10	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P10	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P10	C8T28SOI_LLHF_-SDFPSQNX3_P10	C8T28SOIDV_LL_-SDFPSQNX5_P10	C8T28SOIDV_LL_-SDFPSQNX10_P10
CP	0.0008	0.0008	0.0006	0.0006
D	0.0003	0.0005	0.0004	0.0004
SN	0.0015	0.0014	0.0011	0.0012
TE	0.0011	0.0010	0.0011	0.0011
TI	0.0004	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQNX14_P10	C8T28SOIDV_LL_-SDFPSQNX19_P10	C8T28SOIDV_LL_-SDFPSQNX23_P10	C8T28SOIDV_LL_-SDFPSQNX29_P10
CP	0.0006	0.0006	0.0006	0.0006
D	0.0004	0.0004	0.0004	0.0004
SN	0.0012	0.0012	0.0012	0.0011
TE	0.0011	0.0011	0.0011	0.0011
TI	0.0005	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPSQNX5_P10	**C8T28SOI_LLHF_-SDFPSQNX3_P10**	**C8T28SOI_LL_-SDFPSQNX5_P10**	**C8T28SOI_LLHF_-SDFPSQNX3_P10**
CP to QN ↓	0.0653	0.0652	2.9944	4.2132
CP to QN ↑	0.0595	0.0550	4.1220	5.7251
SN to QN ↓	0.0493	0.0434	2.9964	4.2167
	C8T28SOIDV_LL_-SDFPSQNX5_P10	**C8T28SOIDV_LL_-SDFPSQNX10_P10**	**C8T28SOIDV_LL_-SDFPSQNX5_P10**	**C8T28SOIDV_LL_-SDFPSQNX10_P10**
CP to QN ↓	0.0699	0.0666	2.6954	1.3839
CP to QN ↑	0.0560	0.0578	3.8637	1.9352
SN to QN ↓	0.0467	0.0412	2.7003	1.3820
	C8T28SOIDV_LL_-SDFPSQNX14_P10	**C8T28SOIDV_LL_-SDFPSQNX19_P10**	**C8T28SOIDV_LL_-SDFPSQNX14_P10**	**C8T28SOIDV_LL_-SDFPSQNX19_P10**
CP to QN ↓	0.0695	0.0716	0.9160	0.6992
CP to QN ↑	0.0599	0.0623	1.3001	0.9776
SN to QN ↓	0.0431	0.0457	0.9143	0.6985
	C8T28SOIDV_LL_-SDFPSQNX23_P10	**C8T28SOIDV_LL_-SDFPSQNX29_P10**	**C8T28SOIDV_LL_-SDFPSQNX23_P10**	**C8T28SOIDV_LL_-SDFPSQNX29_P10**
CP to QN ↓	0.0726	0.0703	0.5612	0.4834
CP to QN ↑	0.0617	0.0630	0.9747	0.6557
SN to QN ↓	0.0464	0.0451	0.5603	0.4822

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P10	C8T28SOI_-LLHF_-SDFPSQNX3_-P10	C8T28SOIDV_-LL_-SDFPSQNX5_-P10	C8T28SOIDV_-LL_-SDFPSQNX10_-P10
CP ↓	min_pulse_width to CP	0.0779	0.0768	0.0676	0.0706
CP ↑	min_pulse_width to CP	0.0362	0.0318	0.0362	0.0362
D ↓	hold_rising to CP	-0.0316	-0.0675	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0050	-0.0025	0.0026	0.0026
D ↓	setup_rising to CP	0.0662	0.1072	0.0467	0.0467

D ↑	setup_rising to CP	0.0293	0.0320	0.0249	0.0249
SN ↓	min_pulse_width to SN	0.0376	0.0354	0.0354	0.0354
SN ↑	recovery_rising to CP	0.0032	0.0032	-0.0039	-0.0043
SN ↑	removal_rising to CP	0.0189	0.0212	0.0286	0.0286
TE ↓	hold_rising to CP	-0.0159	-0.0181	-0.0050	-0.0050
TE ↑	hold_rising to CP	-0.0024	0.0008	0.0021	0.0021
TE ↓	setup_rising to CP	0.0640	0.0882	0.0445	0.0445
TE ↑	setup_rising to CP	0.0764	0.1008	0.0715	0.0715
TI ↓	hold_rising to CP	-0.0462	-0.0654	-0.0329	-0.0329
TI ↑	hold_rising to CP	-0.0030	0.0027	0.0033	0.0033
TI ↓	setup_rising to CP	0.0765	0.0992	0.0710	0.0710
TI ↑	setup_rising to CP	0.0278	0.0264	0.0231	0.0231
		C8T28SOIDV_-LL_-SDFPSQNX14_-P10	C8T28SOIDV_-LL_-SDFPSQNX19_-P10	C8T28SOIDV_-LL_-SDFPSQNX23_-P10	C8T28SOIDV_-LL_-SDFPSQNX29_-P10
CP ↓	min_pulse_width to CP	0.0706	0.0706	0.0706	0.0676
CP ↑	min_pulse_width to CP	0.0395	0.0395	0.0408	0.0408
D ↓	hold_rising to CP	-0.0072	-0.0072	-0.0072	-0.0072
D ↑	hold_rising to CP	0.0026	0.0026	0.0026	0.0026
D ↓	setup_rising to CP	0.0467	0.0467	0.0467	0.0467
D ↑	setup_rising to CP	0.0249	0.0249	0.0249	0.0249
SN ↓	min_pulse_width to SN	0.0354	0.0354	0.0381	0.0403
SN ↑	recovery_rising to CP	-0.0039	-0.0043	-0.0043	-0.0043
SN ↑	removal_rising to CP	0.0286	0.0286	0.0286	0.0286
TE ↓	hold_rising to CP	-0.0050	-0.0050	-0.0050	-0.0050
TE ↑	hold_rising to CP	0.0021	0.0021	0.0021	0.0021
TE ↓	setup_rising to CP	0.0445	0.0445	0.0445	0.0445
TE ↑	setup_rising to CP	0.0715	0.0715	0.0715	0.0715
TI ↓	hold_rising to CP	-0.0313	-0.0313	-0.0329	-0.0329
TI ↑	hold_rising to CP	0.0033	0.0033	0.0033	0.0033
TI ↓	setup_rising to CP	0.0710	0.0710	0.0710	0.0710
TI ↑	setup_rising to CP	0.0231	0.0231	0.0231	0.0231

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P10	8.451e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P10	7.771e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P10	8.304e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P10	1.115e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P10	1.242e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P10	1.403e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P10	1.452e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P10	1.793e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

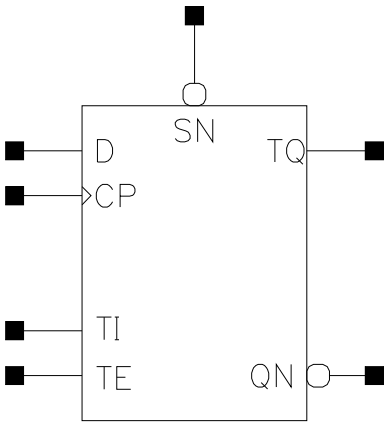
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P10	C8T28SOI_LLHF_-SDFPSQNX3_P10	C8T28SOIDV_LL_-SDFPSQNX5_P10	C8T28SOIDV_LL_-SDFPSQNX10_P10
Clock 100Mhz Data 0Mhz	1.034e-02	9.816e-03	9.396e-03	9.275e-03
Clock 100Mhz Data 25Mhz	1.009e-02	9.620e-03	9.349e-03	1.003e-02
Clock 100Mhz Data 50Mhz	9.844e-03	9.423e-03	9.302e-03	1.079e-02
Clock = 0 Data 100Mhz	4.953e-03	5.270e-03	5.122e-03	5.046e-03
Clock = 1 Data 100Mhz	3.525e-05	6.445e-04	4.424e-04	3.413e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P10	C8T28SOIDV_LL_-SDFPSQNX19_P10	C8T28SOIDV_LL_-SDFPSQNX23_P10	C8T28SOIDV_LL_-SDFPSQNX29_P10
Clock 100Mhz Data 0Mhz	9.200e-03	9.153e-03	9.118e-03	9.054e-03
Clock 100Mhz Data 25Mhz	1.038e-02	1.080e-02	1.094e-02	1.172e-02
Clock 100Mhz Data 50Mhz	1.155e-02	1.245e-02	1.276e-02	1.440e-02
Clock = 0 Data 100Mhz	5.000e-03	4.970e-03	4.948e-03	4.935e-03
Clock = 1 Data 100Mhz	2.808e-04	2.405e-04	2.116e-04	1.900e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P10	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P10	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P10	C8T28SOI_LLHF_-SDFPSQNTX3_P10	C8T28SOIDV_LL_-SDFPSQNTX5_P10	C8T28SOIDV_LL_-SDFPSQNTX10_P10
CP	0.0008	0.0008	0.0006	0.0006
D	0.0003	0.0005	0.0004	0.0004
SN	0.0015	0.0014	0.0011	0.0011
TE	0.0011	0.0010	0.0011	0.0011
TI	0.0004	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQNTX19_P10	C8T28SOIDV_LL_-SDFPSQNTX23_P10	C8T28SOIDV_LL_-SDFPSQNTX29_P10	
CP	0.0006	0.0006	0.0006	
D	0.0004	0.0004	0.0004	
SN	0.0011	0.0011	0.0011	
TE	0.0011	0.0011	0.0011	
TI	0.0005	0.0005	0.0005	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P10	**C8T28SOI_LLHF_-SDFPSQNTX3_P10**	**C8T28SOI_LL_-SDFPSQNTX5_P10**	**C8T28SOI_LLHF_-SDFPSQNTX3_P10**
CP to QN ↓	0.0718	0.0703	3.0365	4.2569
CP to QN ↑	0.0699	0.0647	4.0708	5.7583
CP to TQ ↓	0.0566	0.0459	7.4487	4.9959
CP to TQ ↑	0.0591	0.0547	17.5168	9.7590
SN to QN ↓	0.0519	0.0458	3.0458	4.2672
SN to TQ ↑	0.0411	0.0322	17.4633	9.7059
	C8T28SOIDV_LL_-SDFPSQNTX5_P10	**C8T28SOIDV_LL_-SDFPSQNTX10_P10**	**C8T28SOIDV_LL_-SDFPSQNTX5_P10**	**C8T28SOIDV_LL_-SDFPSQNTX10_P10**
CP to QN ↓	0.0706	0.0676	2.7482	1.3760
CP to QN ↑	0.0582	0.0619	3.8705	1.9448
CP to TQ ↓	0.0408	0.0472	4.9712	5.0410
CP to TQ ↑	0.0535	0.0564	8.4928	8.5579
SN to QN ↓	0.0462	0.0433	2.7575	1.3772
SN to TQ ↑	0.0307	0.0327	8.4564	8.4875
	C8T28SOIDV_LL_-SDFPSQNTX19_P10	**C8T28SOIDV_LL_-SDFPSQNTX23_P10**	**C8T28SOIDV_LL_-SDFPSQNTX19_P10**	**C8T28SOIDV_LL_-SDFPSQNTX23_P10**
CP to QN ↓	0.0725	0.0742	0.6937	0.5593
CP to QN ↑	0.0668	0.0657	0.9816	0.9756
CP to TQ ↓	0.0471	0.0479	5.0386	5.0789
CP to TQ ↑	0.0564	0.0571	8.5588	8.5670
SN to QN ↓	0.0477	0.0490	0.6941	0.5596
SN to TQ ↑	0.0328	0.0332	8.4872	8.4913
	C8T28SOIDV_LL_-SDFPSQNTX29_P10		**C8T28SOIDV_LL_-SDFPSQNTX29_P10**	
CP to QN ↓	0.0738		0.4842	
CP to QN ↑	0.0678		0.6557	

CP to TQ ↓	0.0499		5.1684	
CP to TQ ↑	0.0609		9.7274	
SN to QN ↓	0.0475		0.4842	
SN to TQ ↑	0.0353		9.6277	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P10	C8T28SOI_-LLHF_-SDFPSQNTX3_-P10	C8T28SOIDV_-LL_-SDFPSQNTX5_-P10	C8T28SOIDV_-LL_SDFP-SQNTX10_P10
CP ↓	min_pulse_width to CP	0.0796	0.0775	0.0676	0.0676
CP ↑	min_pulse_width to CP	0.0456	0.0377	0.0362	0.0408
D ↓	hold_rising to CP	-0.0316	-0.0675	-0.0072	-0.0072
D ↑	hold_rising to CP	-0.0050	-0.0025	0.0026	0.0026
D ↓	setup_rising to CP	0.0656	0.1072	0.0467	0.0467
D ↑	setup_rising to CP	0.0293	0.0320	0.0249	0.0249
SN ↓	min_pulse_width to SN	0.0425	0.0354	0.0354	0.0381
SN ↑	recovery_rising to CP	0.0031	0.0031	-0.0039	-0.0043
SN ↑	removal_rising to CP	0.0190	0.0212	0.0286	0.0286
TE ↓	hold_rising to CP	-0.0159	-0.0181	-0.0050	-0.0050
TE ↑	hold_rising to CP	-0.0024	0.0008	0.0021	0.0021
TE ↓	setup_rising to CP	0.0640	0.0877	0.0445	0.0445
TE ↑	setup_rising to CP	0.0813	0.1008	0.0715	0.0715
TI ↓	hold_rising to CP	-0.0462	-0.0654	-0.0329	-0.0329
TI ↑	hold_rising to CP	-0.0030	0.0027	0.0033	0.0033
TI ↓	setup_rising to CP	0.0808	0.0992	0.0710	0.0710
TI ↑	setup_rising to CP	0.0271	0.0264	0.0231	0.0231
		C8T28SOIDV_-LL_SDFP-SQNTX19_P10	C8T28SOIDV_-LL_SDFP-SQNTX23_P10	C8T28SOIDV_-LL_SDFP-SQNTX29_P10	
CP ↓	min_pulse_width to CP	0.0676	0.0676	0.0676	
CP ↑	min_pulse_width to CP	0.0408	0.0408	0.0455	
D ↓	hold_rising to CP	-0.0072	-0.0072	-0.0072	
D ↑	hold_rising to CP	0.0026	0.0026	0.0026	
D ↓	setup_rising to CP	0.0467	0.0467	0.0467	
D ↑	setup_rising to CP	0.0249	0.0249	0.0249	
SN ↓	min_pulse_width to SN	0.0381	0.0381	0.0430	

SN ↑	recovery_rising to CP	-0.0017	-0.0043	-0.0017	
SN ↑	removal_rising to CP	0.0286	0.0286	0.0286	
TE ↓	hold_rising to CP	-0.0050	-0.0050	-0.0050	
TE ↑	hold_rising to CP	0.0021	0.0021	0.0021	
TE ↓	setup_rising to CP	0.0445	0.0445	0.0445	
TE ↑	setup_rising to CP	0.0715	0.0715	0.0715	
TI ↓	hold_rising to CP	-0.0329	-0.0329	-0.0329	
TI ↑	hold_rising to CP	0.0033	0.0033	0.0033	
TI ↓	setup_rising to CP	0.0710	0.0710	0.0710	
TI ↑	setup_rising to CP	0.0231	0.0231	0.0231	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P10	8.476e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P10	8.306e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P10	8.929e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_-P10	1.172e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_-P10	1.466e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_-P10	1.520e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_-P10	1.845e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P10	C8T28SOI_LLHF_-SDFPSQNTX3_P10	C8T28SOIDV_LL_-SDFPSQNTX5_P10	C8T28SOIDV_LL_-SDFPSQNTX10_P10
Clock 100Mhz Data 0Mhz	1.006e-02	9.675e-03	9.307e-03	9.124e-03
Clock 100Mhz Data 25Mhz	1.024e-02	9.860e-03	9.458e-03	1.018e-02
Clock 100Mhz Data 50Mhz	1.043e-02	1.005e-02	9.608e-03	1.123e-02
Clock = 0 Data 100Mhz	4.947e-03	5.267e-03	5.120e-03	5.047e-03
Clock = 1 Data 100Mhz	3.547e-05	6.452e-04	4.430e-04	3.418e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P10	C8T28SOIDV_LL_-SDFPSQNTX23_P10	C8T28SOIDV_LL_-SDFPSQNTX29_P10	
Clock 100Mhz Data 0Mhz	9.014e-03	8.941e-03	8.890e-03	
Clock 100Mhz Data 25Mhz	1.098e-02	1.113e-02	1.196e-02	
Clock 100Mhz Data 50Mhz	1.295e-02	1.332e-02	1.503e-02	

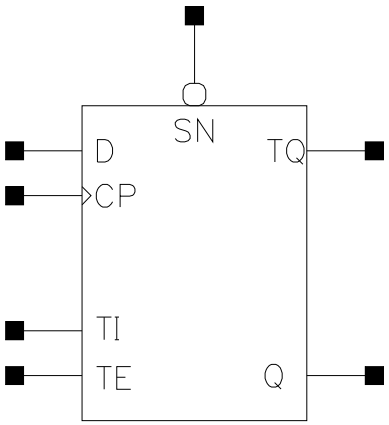
Clock = 0 Data 100Mhz	5.003e-03	4.974e-03	4.955e-03	
Clock = 1 Data 100Mhz	2.813e-04	2.408e-04	2.120e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P10	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P10	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P10	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P10	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P10	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P10	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P10	C8T28SOI_LLHF_-SDFPSQTX3_P10	C8T28SOIDV_LL_-SDFPSQTX5_P10	C8T28SOIDV_LL_-SDFPSQTX10_P10
CP	0.0008	0.0008	0.0006	0.0006
D	0.0003	0.0005	0.0004	0.0004
SN	0.0015	0.0014	0.0011	0.0011
TE	0.0011	0.0010	0.0011	0.0011
TI	0.0004	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQTX19_P10	C8T28SOIDV_LL_-SDFPSQTX29_P10		
CP	0.0006	0.0006		
D	0.0004	0.0004		
SN	0.0011	0.0011		
TE	0.0011	0.0011		
TI	0.0005	0.0005		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPSQTX5_P10	**C8T28SOI_LLHF_-SDFPSQTX3_P10**	**C8T28SOI_LL_-SDFPSQTX5_P10**	**C8T28SOI_LLHF_-SDFPSQTX3_P10**
CP to Q ↓	0.0608	0.0543	3.1654	4.6774
CP to Q ↑	0.0526	0.0557	3.9885	5.9834
CP to TQ ↓	0.0683	0.0520	7.8898	5.1474
CP to TQ ↑	0.0650	0.0584	17.5545	9.9139
SN to Q ↑	0.0343	0.0323	3.9094	5.8818
SN to TQ ↑	0.0438	0.0340	17.4885	9.8431
	C8T28SOIDV_LL_-SDFPSQTX5_P10	**C8T28SOIDV_LL_-SDFPSQTX10_P10**	**C8T28SOIDV_LL_-SDFPSQTX5_P10**	**C8T28SOIDV_LL_-SDFPSQTX10_P10**
CP to Q ↓	0.0475	0.0614	2.8787	1.3892
CP to Q ↑	0.0555	0.0833	3.9596	1.9709
CP to TQ ↓	0.0476	0.0631	5.0599	5.1221
CP to TQ ↑	0.0566	0.0865	8.6020	8.4730
SN to Q ↑	0.0324	0.0586	3.9190	1.9711
SN to TQ ↑	0.0328	0.0618	8.5432	8.4801
	C8T28SOIDV_LL_-SDFPSQTX19_P10	**C8T28SOIDV_LL_-SDFPSQTX29_P10**	**C8T28SOIDV_LL_-SDFPSQTX19_P10**	**C8T28SOIDV_LL_-SDFPSQTX29_P10**
CP to Q ↓	0.0674	0.0750	0.7198	0.4782
CP to Q ↑	0.0887	0.0960	1.0109	0.6694
CP to TQ ↓	0.0672	0.0410	4.4368	4.5646
CP to TQ ↑	0.0927	0.0583	9.6597	9.7385
SN to Q ↑	0.0639	0.0686	1.0110	0.6709
SN to TQ ↑	0.0679	0.0334	9.6598	9.6968

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_-P10	C8T28SOI_-LLHF_-SDFPSQTX3_-P10	C8T28SOIDV_-LL_-SDFPSQTX5_-P10	C8T28SOIDV_-LL_-SDFPSQTX10_-P10
CP ↓	min_pulse_width to CP	0.0796	0.0775	0.0676	0.0683
CP ↑	min_pulse_width to CP	0.0518	0.0424	0.0409	0.0349
D ↓	hold_rising to CP	-0.0316	-0.0675	-0.0072	-0.0120
D ↑	hold_rising to CP	-0.0050	-0.0025	0.0026	0.0026
D ↓	setup_rising to CP	0.0656	0.1072	0.0467	0.0493
D ↑	setup_rising to CP	0.0293	0.0320	0.0249	0.0244
SN ↓	min_pulse_width to SN	0.0452	0.0354	0.0381	0.0354
SN ↑	recovery_rising to CP	0.0031	0.0031	-0.0043	-0.0039
SN ↑	removal_rising to CP	0.0190	0.0212	0.0286	0.0286
TE ↓	hold_rising to CP	-0.0159	-0.0181	-0.0050	-0.0098
TE ↑	hold_rising to CP	-0.0024	0.0008	0.0021	-0.0027
TE ↓	setup_rising to CP	0.0640	0.0877	0.0445	0.0436
TE ↑	setup_rising to CP	0.0813	0.1008	0.0715	0.0715
TI ↓	hold_rising to CP	-0.0462	-0.0654	-0.0329	-0.0315
TI ↑	hold_rising to CP	-0.0030	0.0027	0.0033	-0.0030
TI ↓	setup_rising to CP	0.0808	0.0992	0.0710	0.0659
TI ↑	setup_rising to CP	0.0271	0.0264	0.0231	0.0293
		C8T28SOIDV_-LL_-SDFPSQTX19_-P10	C8T28SOIDV_-LL_-SDFPSQTX29_-P10		
CP ↓	min_pulse_width to CP	0.0677	0.0683		
CP ↑	min_pulse_width to CP	0.0349	0.0402		
D ↓	hold_rising to CP	-0.0120	-0.0120		
D ↑	hold_rising to CP	0.0026	0.0026		
D ↓	setup_rising to CP	0.0493	0.0493		
D ↑	setup_rising to CP	0.0244	0.0244		
SN ↓	min_pulse_width to SN	0.0354	0.0403		
SN ↑	recovery_rising to CP	-0.0071	-0.0039		
SN ↑	removal_rising to CP	0.0286	0.0286		
TE ↓	hold_rising to CP	-0.0098	-0.0098		
TE ↑	hold_rising to CP	-0.0027	-0.0027		

TE ↓	setup_rising to CP	0.0441	0.0436		
TE ↑	setup_rising to CP	0.0715	0.0715		
TI ↓	hold_rising to CP	-0.0315	-0.0315		
TI ↑	hold_rising to CP	-0.0030	-0.0030		
TI ↓	setup_rising to CP	0.0659	0.0659		
TI ↑	setup_rising to CP	0.0278	0.0278		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P10	8.362e-05	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P10	8.247e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P10	8.698e-05	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P10	1.131e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P10	1.367e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P10	1.744e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

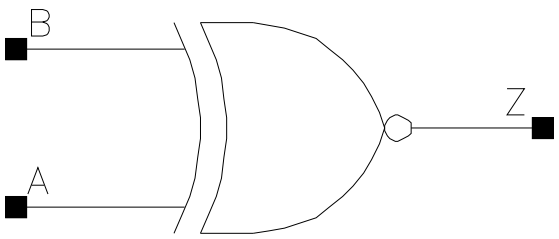
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P10	C8T28SOI_LLHF_-SDFPSQTX3_P10	C8T28SOIDV_LL_-SDFPSQTX5_P10	C8T28SOIDV_LL_-SDFPSQTX10_P10
Clock 100Mhz Data 0Mhz	1.007e-02	9.683e-03	9.316e-03	9.121e-03
Clock 100Mhz Data 25Mhz	1.041e-02	9.957e-03	9.539e-03	1.000e-02
Clock 100Mhz Data 50Mhz	1.076e-02	1.023e-02	9.763e-03	1.088e-02
Clock = 0 Data 100Mhz	4.947e-03	5.267e-03	5.120e-03	5.091e-03
Clock = 1 Data 100Mhz	3.535e-05	6.451e-04	4.428e-04	3.420e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P10	C8T28SOIDV_LL_-SDFPSQTX29_P10		
Clock 100Mhz Data 0Mhz	9.005e-03	8.928e-03		
Clock 100Mhz Data 25Mhz	1.092e-02	1.183e-02		
Clock 100Mhz Data 50Mhz	1.283e-02	1.474e-02		
Clock = 0 Data 100Mhz	5.062e-03	5.044e-03		
Clock = 1 Data 100Mhz	2.815e-04	2.412e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P10	1.600	0.544	0.8704
X5_P10	0.800	1.496	1.1968
X8_P10	1.600	1.088	1.7408
X9_P10	0.800	1.632	1.3056
X11_P10	1.600	1.360	2.1760
X14_P10	0.800	2.312	1.8496
X15_P10	1.600	1.904	3.0464
X19_P10	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P10	X5_P10	X8_P10	X9_P10
A	0.0011	0.0006	0.0019	0.0007
B	0.0010	0.0010	0.0015	0.0013
	X11_P10	X14_P10	X15_P10	X19_P10
A	0.0028	0.0011	0.0033	0.0013
B	0.0024	0.0018	0.0029	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P10	X5_P10	X4_P10	X5_P10
A to Z ↓	0.0147	0.0400	3.6899	2.9006
A to Z ↑	0.0164	0.0372	5.3867	4.1782
B to Z ↓	0.0136	0.0296	3.6898	2.8857
B to Z ↑	0.0178	0.0279	5.4005	4.1742

	X8_P10	X9_P10	X8_P10	X9_P10
A to Z ↓	0.0177	0.0383	1.9519	1.4912
A to Z ↑	0.0199	0.0362	2.8815	2.1334
B to Z ↓	0.0166	0.0289	1.9518	1.4880
B to Z ↑	0.0209	0.0279	2.8862	2.1316
	X11_P10	**X14_P10**	**X11_P10**	**X14_P10**
A to Z ↓	0.0164	0.0360	1.3653	1.0132
A to Z ↑	0.0180	0.0335	1.8774	1.3797
B to Z ↓	0.0148	0.0270	1.3650	1.0099
B to Z ↑	0.0186	0.0259	1.8822	1.3771
	X15_P10	**X19_P10**	**X15_P10**	**X19_P10**
A to Z ↓	0.0182	0.0339	1.0364	0.7551
A to Z ↑	0.0201	0.0325	1.4320	1.0270
B to Z ↓	0.0166	0.0262	1.0358	0.7523
B to Z ↑	0.0209	0.0255	1.4348	1.0262

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P10	4.108e-05	1.000e-20
X5_P10	4.445e-05	1.000e-20
X8_P10	6.565e-05	1.000e-20
X9_P10	7.267e-05	1.000e-20
X11_P10	1.007e-04	1.000e-20
X14_P10	1.124e-04	1.000e-20
X15_P10	1.268e-04	1.000e-20
X19_P10	1.559e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P10	X5_P10	X8_P10	X9_P10
A to Z	2.467e-03	5.043e-03	4.674e-03	7.437e-03
B to Z	2.423e-03	4.113e-03	4.648e-03	6.179e-03
	X11_P10	X14_P10	X15_P10	X19_P10
A to Z	6.733e-03	1.163e-02	9.075e-03	1.432e-02
B to Z	6.579e-03	9.452e-03	8.931e-03	1.190e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

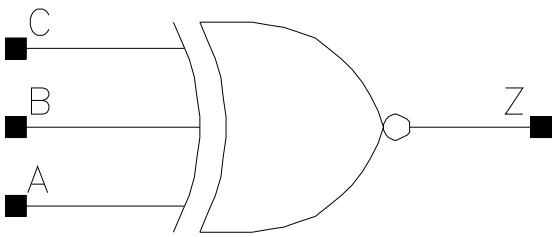
Pin Cycle (vdds)	X4_P10	X5_P10	X8_P10	X9_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P10	X14_P10	X15_P10	X19_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P10	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P10	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P10	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P10	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P10	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P10	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P10	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P10	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P10	C8T28SOIDV_LL_-XNOR3X4_P10	C8T28SOIDV_LL_-XNOR3X9_P10	C8T28SOIDV_LL_-XNOR3X13_P10
A	0.0017	0.0017	0.0022	0.0029
B	0.0017	0.0016	0.0021	0.0028
C	0.0007	0.0007	0.0007	0.0007
	C8T28SOIDV_LLS_-XNOR3X1_P10	C8T28SOIDV_LLS_-XNOR3X2_P10	C8T28SOIDV_LLS_-XNOR3X5_P10	C8T28SOIDV_LLS_-XNOR3X7_P10

A	0.0017	0.0019	0.0042	0.0064
B	0.0017	0.0020	0.0038	0.0060
C	0.0011	0.0014	0.0028	0.0040

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_XNOR3X2_P10	C8T28SOIDV_LL_XNOR3X4_P10	C8T28SOIDV_LL_XNOR3X2_P10	C8T28SOIDV_LL_XNOR3X4_P10
A to Z ↓	0.0401	0.0429	5.6753	3.1303
A to Z ↑	0.0386	0.0397	7.3845	4.2300
B to Z ↓	0.0409	0.0439	5.6768	3.1309
B to Z ↑	0.0396	0.0408	7.3851	4.2298
C to Z ↓	0.0559	0.0596	5.6720	3.1303
C to Z ↑	0.0545	0.0564	7.3792	4.2306
	C8T28SOIDV_LL_XNOR3X9_P10	C8T28SOIDV_LL_XNOR3X13_P10	C8T28SOIDV_LL_XNOR3X9_P10	C8T28SOIDV_LL_XNOR3X13_P10
A to Z ↓	0.0378	0.0430	1.5789	1.0815
A to Z ↑	0.0400	0.0459	2.0748	1.4434
B to Z ↓	0.0388	0.0440	1.5791	1.0814
B to Z ↑	0.0412	0.0473	2.0751	1.4437
C to Z ↓	0.0563	0.0671	1.5775	1.0810
C to Z ↑	0.0583	0.0705	2.0753	1.4435
	C8T28SOIDV_LLS_XNOR3X1_P10	C8T28SOIDV_LLS_XNOR3X2_P10	C8T28SOIDV_LLS_XNOR3X1_P10	C8T28SOIDV_LLS_XNOR3X2_P10
A to Z ↓	0.0245	0.0275	9.7450	5.5447
A to Z ↑	0.0256	0.0255	15.0388	8.1727
B to Z ↓	0.0255	0.0287	9.7640	5.5514
B to Z ↑	0.0265	0.0266	15.0334	8.1691
C to Z ↓	0.0250	0.0276	9.7904	5.5728
C to Z ↑	0.0261	0.0257	15.0404	8.1782
	C8T28SOIDV_LLS_XNOR3X5_P10	C8T28SOIDV_LLS_XNOR3X7_P10	C8T28SOIDV_LLS_XNOR3X5_P10	C8T28SOIDV_LLS_XNOR3X7_P10
A to Z ↓	0.0286	0.0248	2.6925	1.8599
A to Z ↑	0.0278	0.0241	4.0498	2.7118
B to Z ↓	0.0287	0.0245	2.6985	1.8658
B to Z ↑	0.0278	0.0239	4.0500	2.7129
C to Z ↓	0.0278	0.0240	2.7005	1.8687
C to Z ↑	0.0268	0.0231	4.0469	2.7128

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P10	3.326e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P10	3.906e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P10	6.702e-05	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P10	9.516e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P10	2.228e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P10	3.727e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P10	8.641e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P10	1.334e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P10	C8T28SOIDV_LL_-XNOR3X4_P10	C8T28SOIDV_LL_-XNOR3X9_P10	C8T28SOIDV_LL_-XNOR3X13_P10
A to Z	3.050e-03	3.753e-03	5.865e-03	9.670e-03
B to Z	3.036e-03	3.741e-03	5.904e-03	9.739e-03
C to Z	4.836e-03	5.594e-03	8.178e-03	1.317e-02
	C8T28SOIDV_LLS_-XNOR3X1_P10	C8T28SOIDV_LLS_-XNOR3X2_P10	C8T28SOIDV_LLS_-XNOR3X5_P10	C8T28SOIDV_LLS_-XNOR3X7_P10
A to Z	1.800e-03	2.650e-03	5.767e-03	8.015e-03
B to Z	1.794e-03	2.690e-03	5.874e-03	7.994e-03
C to Z	1.776e-03	2.669e-03	5.874e-03	7.989e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

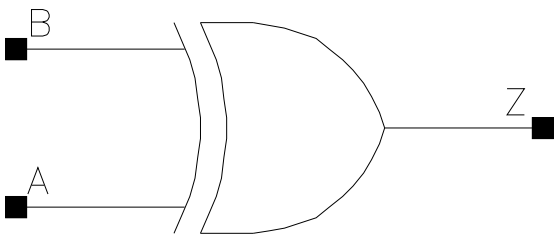
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P10	C8T28SOIDV_LL_-XNOR3X4_P10	C8T28SOIDV_LL_-XNOR3X9_P10	C8T28SOIDV_LL_-XNOR3X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P10	C8T28SOIDV_LLS_-XNOR3X2_P10	C8T28SOIDV_LLS_-XNOR3X5_P10	C8T28SOIDV_LLS_-XNOR3X7_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P10	0.800	1.360	1.0880
X4_P10	1.600	0.544	0.8704
X5_P10	0.800	1.360	1.0880
X8_P10	1.600	1.088	1.7408
X9_P10	0.800	1.496	1.1968
X12_P10	1.600	1.360	2.1760
X13_P10	0.800	2.176	1.7408
X15_P10	1.600	1.904	3.0464
X17_P10	0.800	2.312	1.8496
X18_P10	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P10	X4_P10	X5_P10	X8_P10
A	0.0006	0.0011	0.0007	0.0018
B	0.0011	0.0010	0.0012	0.0017
	X9_P10	X12_P10	X13_P10	X15_P10
A	0.0008	0.0029	0.0014	0.0034
B	0.0015	0.0022	0.0025	0.0027
	X17_P10	X18_P10		
A	0.0014	0.0018		
B	0.0025	0.0022		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P10	**X4_P10**	**X2_P10**	**X4_P10**
A to Z ↓	0.0341	0.0142	5.4438	2.8706
A to Z ↑	0.0335	0.0185	7.5790	6.9873
B to Z ↓	0.0264	0.0152	5.3981	2.8985
B to Z ↑	0.0269	0.0170	7.5714	6.9814
	X5_P10	**X8_P10**	**X5_P10**	**X8_P10**
A to Z ↓	0.0326	0.0185	3.0004	1.5605
A to Z ↑	0.0305	0.0221	4.0923	3.6755
B to Z ↓	0.0251	0.0202	2.9858	1.5778
B to Z ↑	0.0244	0.0208	4.0863	3.6736
	X9_P10	**X12_P10**	**X9_P10**	**X12_P10**
A to Z ↓	0.0324	0.0167	1.5680	1.0478
A to Z ↑	0.0313	0.0199	2.1291	2.4637
B to Z ↓	0.0251	0.0171	1.5622	1.0588
B to Z ↑	0.0247	0.0180	2.1280	2.4624
	X13_P10	**X15_P10**	**X13_P10**	**X15_P10**
A to Z ↓	0.0298	0.0180	1.0728	0.8168
A to Z ↑	0.0287	0.0229	1.4694	2.1823
B to Z ↓	0.0212	0.0183	1.0695	0.8260
B to Z ↑	0.0205	0.0208	1.4669	2.1802
	X17_P10	**X18_P10**	**X17_P10**	**X18_P10**
A to Z ↓	0.0317	0.0354	0.8112	0.8036
A to Z ↑	0.0302	0.0327	1.1000	1.0383
B to Z ↓	0.0230	0.0282	0.8096	0.8034
B to Z ↑	0.0221	0.0257	1.0983	1.0381

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P10	3.545e-05	1.000e-20
X4_P10	3.998e-05	1.000e-20
X5_P10	5.439e-05	1.000e-20
X8_P10	6.354e-05	1.000e-20
X9_P10	8.835e-05	1.000e-20
X12_P10	9.822e-05	1.000e-20
X13_P10	1.425e-04	1.000e-20
X15_P10	1.172e-04	1.000e-20
X17_P10	1.536e-04	1.000e-20
X18_P10	1.523e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P10	X4_P10	X5_P10	X8_P10
A to Z	3.678e-03	2.491e-03	4.754e-03	4.813e-03
B to Z	3.240e-03	2.416e-03	4.134e-03	4.786e-03
	X9_P10	X12_P10	X13_P10	X15_P10
A to Z	7.060e-03	6.854e-03	1.144e-02	8.767e-03
B to Z	6.272e-03	6.650e-03	8.304e-03	8.553e-03
	X17_P10	X18_P10		
A to Z	1.317e-02	1.468e-02		
B to Z	1.002e-02	1.194e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

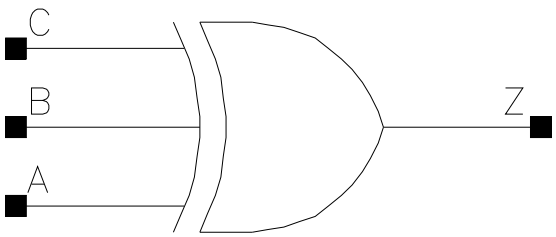
Pin Cycle (vdds)	X2_P10	X4_P10	X5_P10	X8_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P10	X12_P10	X13_P10	X15_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P10	X18_P10		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P10	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P10	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P10	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P10	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P10	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P10	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P10	C8T28SOIDV_LL_-XOR3X4_P10	C8T28SOIDV_LL_-XOR3X9_P10	C8T28SOIDV_LL_-XOR3X13_P10
A	0.0018	0.0017	0.0021	0.0029
B	0.0017	0.0018	0.0021	0.0028
C	0.0011	0.0011	0.0014	0.0023
	C8T28SOIDV_LLS_-XOR3X1_P10	C8T28SOIDV_LLS_-XOR3X2_P10	C8T28SOIDV_LLS_-XOR3X5_P10	C8T28SOIDV_LLS_-XOR3X7_P10

A	0.0018	0.0020	0.0034	0.0052
B	0.0019	0.0020	0.0032	0.0052
C	0.0006	0.0006	0.0006	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P10	**C8T28SOIDV_LL_-XOR3X4_P10**	**C8T28SOIDV_LL_-XOR3X2_P10**	**C8T28SOIDV_LL_-XOR3X4_P10**
A to Z ↓	0.0391	0.0432	5.6971	3.1406
A to Z ↑	0.0378	0.0408	7.5819	4.2322
B to Z ↓	0.0397	0.0443	5.6993	3.1418
B to Z ↑	0.0386	0.0421	7.5837	4.2347
C to Z ↓	0.0394	0.0439	5.7000	3.1430
C to Z ↑	0.0383	0.0416	7.5874	4.2344
	C8T28SOIDV_LL_-XOR3X9_P10	**C8T28SOIDV_LL_-XOR3X13_P10**	**C8T28SOIDV_LL_-XOR3X9_P10**	**C8T28SOIDV_LL_-XOR3X13_P10**
A to Z ↓	0.0403	0.0443	1.5676	1.0698
A to Z ↑	0.0408	0.0467	2.0890	1.4050
B to Z ↓	0.0414	0.0453	1.5681	1.0701
B to Z ↑	0.0422	0.0481	2.0884	1.4059
C to Z ↓	0.0407	0.0451	1.5686	1.0705
C to Z ↑	0.0413	0.0482	2.0883	1.4054
	C8T28SOIDV_LLS_-XOR3X1_P10	**C8T28SOIDV_LLS_-XOR3X2_P10**	**C8T28SOIDV_LLS_-XOR3X1_P10**	**C8T28SOIDV_LLS_-XOR3X2_P10**
A to Z ↓	0.0259	0.0285	7.0172	5.6556
A to Z ↑	0.0258	0.0254	10.9585	7.8255
B to Z ↓	0.0270	0.0294	7.0429	5.6627
B to Z ↑	0.0270	0.0263	10.9664	7.8256
C to Z ↓	0.0429	0.0462	7.0001	5.6323
C to Z ↑	0.0434	0.0436	10.9464	7.7909
	C8T28SOIDV_LLS_-XOR3X5_P10	**C8T28SOIDV_LLS_-XOR3X7_P10**	**C8T28SOIDV_LLS_-XOR3X5_P10**	**C8T28SOIDV_LLS_-XOR3X7_P10**
A to Z ↓	0.0381	0.0325	2.9420	2.0310
A to Z ↑	0.0323	0.0278	4.0846	2.7637
B to Z ↓	0.0369	0.0329	2.9509	2.0356
B to Z ↑	0.0320	0.0284	4.0872	2.7649
C to Z ↓	0.0645	0.0538	2.9473	2.0275
C to Z ↑	0.0596	0.0493	4.0735	2.7538

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P10	2.715e-05	1.000e-20
C8T28SOIDV_LL_XOR3X4_P10	3.375e-05	1.000e-20
C8T28SOIDV_LL_XOR3X9_P10	6.068e-05	1.000e-20
C8T28SOIDV_LL_XOR3X13_P10	8.860e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P10	3.764e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P10	4.444e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P10	7.542e-05	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P10	1.149e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P10	C8T28SOIDV_LL_-XOR3X4_P10	C8T28SOIDV_LL_-XOR3X9_P10	C8T28SOIDV_LL_-XOR3X13_P10
A to Z	2.910e-03	3.742e-03	5.908e-03	1.008e-02
B to Z	2.890e-03	3.743e-03	5.950e-03	1.013e-02
C to Z	2.875e-03	3.718e-03	5.933e-03	1.015e-02
	C8T28SOIDV_LLS_-XOR3X1_P10	C8T28SOIDV_LLS_-XOR3X2_P10	C8T28SOIDV_LLS_-XOR3X5_P10	C8T28SOIDV_LLS_-XOR3X7_P10
A to Z	2.241e-03	2.720e-03	5.507e-03	7.682e-03
B to Z	2.248e-03	2.762e-03	5.646e-03	7.866e-03
C to Z	4.283e-03	4.907e-03	9.284e-03	1.299e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P10	C8T28SOIDV_LL_-XOR3X4_P10	C8T28SOIDV_LL_-XOR3X9_P10	C8T28SOIDV_LL_-XOR3X13_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P10	C8T28SOIDV_LLS_-XOR3X2_P10	C8T28SOIDV_LLS_-XOR3X5_P10	C8T28SOIDV_LLS_-XOR3X7_P10
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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