# Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB

## 3.3

## Release Notes

## October 2018


**PDK & Foundation Design Flows**

**Technology R&D – T&DP – Design Platform**

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# Revision History

| Date | Product Version | Comments |
|---|---|---|
| 01/07/2016 | 2.8.b | First version (aligned with DK version) |
| 09/09/2016 | 2.8.c | Bug fix vc.bbview |
| 07/10/2016 | 2.9 | Alignment with DK 2.9 (HLVT inclusion) |
| 13/01/2017 | 3.0 | - technology.lef: updated routing directions for alignment with PG grid requirements & reintroduction of former vias definition<br>- Introduction of technology_COT.lef file with systematic orthogonal metal layers<br>- Alignment of PVS files with last DK 2.9<br>- Updated “overlap” strategy in dummy_layers.lef file for SignOff Extraction task => both “overlap” & “OVERLAP” layers are now defined |
| 07/02/2017 | 3.0.a | Update of QRC techfiles with latest EM effects |
| 28/03/2017 | 3.0.b | Added missing CORE12TEG site in sites.lef (bug fix for test chip team) |
| 31/03/2017 | 3.0.c | QRC_TECHFILE bbview key alignment with latest spec<br>Removal of former .csh env variables<br>Addition of .cdslib file (and its bbview key)<br>Addition of OA sites library (and its bbview key)<br>Removal of PVS decks as agreed with TPPM (already in DK)<br>Update of tech LEF regarding 553q1/q2 rules |
| 06/04/2017 | 3.0.d | Optimization of XA double vias definition in technology_COT.lef |
| 02/06/2017 | 3.1 | CAP_TABLE & QRC_TECHFILE regenerated for alignment with updated PEX 28NM_STARRCXT_FDSOI_PROTOTYPE 2.3-PRELIM-00 (using ext 16.10/innovus 16.14)<br>Renaming of technology_COT.lef in technology_alternative.lef |
| 20/10/2017 | 3.2 | Introduction of Via Large Array Spacing rules in tech LEF<br>Duplication of “overlap/OVERLAP” in tech LEF (i.e. Zuma request)<br>Aligned LPA strategy (new lpa.layer.map) with P28 FTK CDN strategy<br>Removal of obsolete CAP_TABLE files |
| 09/11/2017 | 3.2.a | [TRC #460908]: Addition of missing LEFOBS lines in Innovus map_out (required for LPA litho HS fixing)<br>[TRC #460914]: Addition of M6 in layer list of LPA conf file<br>[TRC #460904]: Removal of LPA MAP/ directory, transfer of LPA map file in TECH/ directory and removal of LPA map file bbview key |
| 13/07/2018 | 3.3 PRELIM | Introduction of bin.tcl file for LIMA team |
| 10/08/2018 | 3.3 INTERM | [TRC #498345]: "LEFOBS" missing in Innovus |

| | | |
|---|---|---|
| | | mapOut for layer above M3<br>[TRC #460908]: C28SOI: Missing lines in Innovus mapOut<br>[TRC #460904]: LPA mapFile : incorrect management<br>[TRC #460914]: C28SOI: Wrong line ine "LPA conf file"<br>[TRC #496960 & #496961]: Antenna rules not coded for VV & LB layers<br>EDI map_out: alignment with metal/via fillOPC purposes mappings for track-based fill |
| 07/10/2018 | 3.3 | Coding of new high-voltage FBB rules in tech LEF<br>Inclusion of new VH/VL custom layers in Innovus map_out<br>TRC #504081 Need new layers in the EDI/map_out file for SIP Wirebond flow |

# Table of Contents

# 1. Introduction

This document contains the Release Notes for Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB 3.3. The following sections describe the release in detail and provide other information that supplements the main documentation.

| Product Name | **Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB** |
|---|---|
| Release Number | 3.3 |
| Release Date | 07/10/2018 |
| Library Type | 8T, 12T |
| Technology | cmos028FDSOI_6U1x_2T8x_LB |
| DK version | DK_cmos28FDSOI_RF_mmW_6U1x_2T8x_LB@1.2 |
| CAD tool version | innovus 17.14<br>For SignOff tools versions (mvs/pvs/quantus/tempus/voltus), please refer to DDF&M team (Christophe Pouly - Sylvain Biard) |

# 2. History

This section provides a brief history of all the previous releases of this product. It includes the updates made in the corresponding releases.

## 2.1 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@3.3

- Coding of new high-voltage FBB rules in tech LEF
- Inclusion of new VH/VL custom layers in Innovus map_out
- TRC #504081 Need new layers in the EDI/map_out file for SIP Wirebond flow

## 2.2 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@3.3 INTERM

- [TRC #498345]: "LEFOBS" missing in Innovus mapOut for layer above M3
- [TRC #460908]: C28SOI: Missing lines in Innovus mapOut
- [TRC #460904]: LPA mapFile : incorrect management
- [TRC #460914]: C28SOI: Wrong line ine "LPA conf file"
- [TRC #496960 & #496961]: Antenna rules not coded for VV & LB layers
- EDI map_out: alignment with metal/via fillOPC purposes mappings for track-based fill

## 2.3 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@3.3 PRELIM

- Introduction of bin.tcl file for LIMA team

## 2.4 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@3.2.a

- [TRC #460908]: Addition of missing LEFOBS lines in Innovus map_out (required for LPA litho HS fixing)
- [TRC #460914]: Addition of M6 in layer list of LPA conf file
- [TRC #460904]: Removal of LPA MAP/ directory, transfer of LPA map file in TECH/ directory and removal of LPA map file bbview key

## 2.5 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@3.2

- Introduction of Via Large Array Spacing rules in tech LEF
- Duplication of “overlap/OVERLAP” in tech LEF (i.e. Zuma request)
- Aligned LPA strategy (new lpa.layer.map) with P28 FTK CDN strategy
- Removal of obsolete CAP_TABLE files

## 2.6 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@3.1

- CAP_TABLE & QRC_TECHFILE regenerated for alignment with updated PEX 28NM_STARRCXT_FDSOI_PROTOTYPE 2.3-PRELIM-00 (using ext 16.10/innovus 16.14)
- Renaming of technology_COT.lef in technology_alternative.lef

## 2.7 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@3.0.d

- Optimization of XA double vias definition in technology_COT.lef (to align with IA/IB routing directions).

## 2.8 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@3.0.c

- QRC_TECHFILE bbview key alignment with latest spec
- Removal of former .csh env variables
- Addition of .cdslib file (and its bbview key) for ARCAD team
- Addition of OA sites library (and its bbview key) for ARCAD team
- Removal of PVS decks as agreed with TPPM (already in DK)
- Update of tech LEF regarding 553q1/q2 rules for DDFM team

## 2.9 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@3.0.b

- Added missing CORE12TEG site in sites.lef (bug fix for test chip team)

## 2.10 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@3.0.a

- Update of QRC techfiles in order to include latest EM effects

## 2.11 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@3.0

- technology.lef: updated routing directions for alignment with PG grid requirements & reintroduction of former vias definition
- Introduction of technology_COT.lef file with systematic orthogonal metal layers
- Alignment of PVS files with last DK 2.9
- Updated “overlap” strategy in dummy_layers.lef file for SignOff Extraction task => both “overlap” & “OVERLAP” layers are now defined

## 2.12 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@2.9

- Addition of HLVT layer in tech LEF in order to be aligned with DK 2.9

## 2.13 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@2.8.c

- Bug fix in vc.bbview file

## 2.14 Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB@2.8.b

- Initial release
- Contains PNR and SignOff files

# 3. References

Please refer to the Foundation_Cadence_TechnoKit_cmos028FDSOI_6U1x_2T8x_LB user manual for details concerning the product content.

# 4. User Interface

Please contact **HELPDESK** for any problems or suggestions.