Smart Tiling Manual

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1 - PURPOSE

Smart Tiling allows putting tiles in your layout, but in a smarter manner than the classical tiling procedure.
It creates new GDS file(s) containing all tiles in specified layers in order to respect required minimum density, max density and density gradient.
It can also refer to user's customization through the Gui expert parameters, which can be enabled only with technologists and/or DK team's agreement: a gds, even DRC clean, may be refused otherwise.

2 - SETUP

The Smart Tiling feature is included in this Design Kit. You must setup the Calibre version to the qualified version, indicated in the release notes. Newer Calibre releases can be used, but have not been qualified.

Warning:
• Always read the release notes before using the related Smart Tiling feature.
• Always set the Calibre version to the qualified version. This may not be the same as the one used for the DRC/LVS check.

3 - SMART TILING RELATED FILES AND VARIABLES WITHIN THE DK

3.1 - Architecture & files

$DKITROOT/DATA/CALIBRE/calibre_smart_tiling: contains runset and customization files
$DKITROOT/doc: contains the documentation

3.2 - Variables

Variable	Usage
DKITROOT/DATA/CALIBRE/calibre_smart_tiling	Location of the Smart Tiling deck
MGC_CALIBRE_SMART_TILING_RUNSET_FILE	Calibre runset file
MGC_CALIBRE_SMART_TILING_CUSTOMIZATION_FILE	TVF customization (switches) file
U2DK_CALIBRE_SMART_TILING_DECK	TVF main file
U2DK_CALIBRE_TVF_PACK	Location of the tvf files
CTK_CALIBRE_SMART_TILING_GEN_TEMPLATE	Script used to generate template file

Note: TVF stands for TCL Verification language. It is a higher level language, which is used by Calibre to generate a SVRF technology file.

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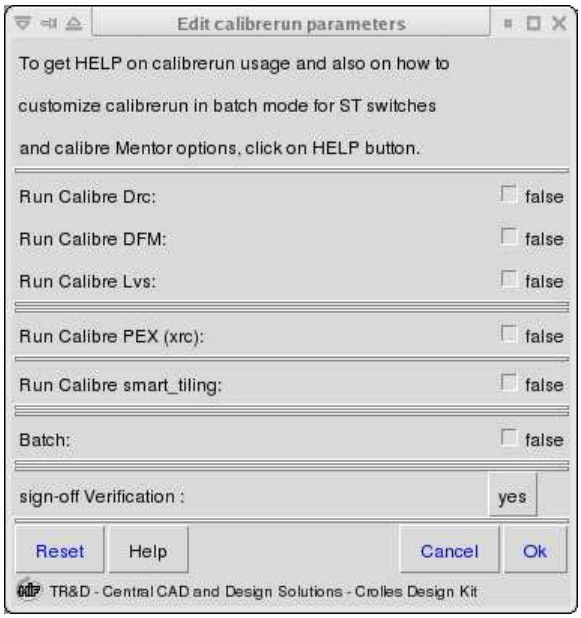
4 - RUN SMART TILING

Smart Tiling feature is only available from UNIX, in Gui or batch mode. The use of calibrerun tool for Smart Tiling is mandatory.

4.1 - Calibrerun interface (Gui/batch)

In a UNIX window with the Design Kit set, type: calibrerun -gui
Then the following interface appears: Select "*Run Calibre smart_tiling*" and click OK. Calibre will then open with default Smart Tiling settings.

To access batch mode, click on 'Batch' button: Fill the fields (layout name and path, primary cell name), and execute tiling with 'OK'.



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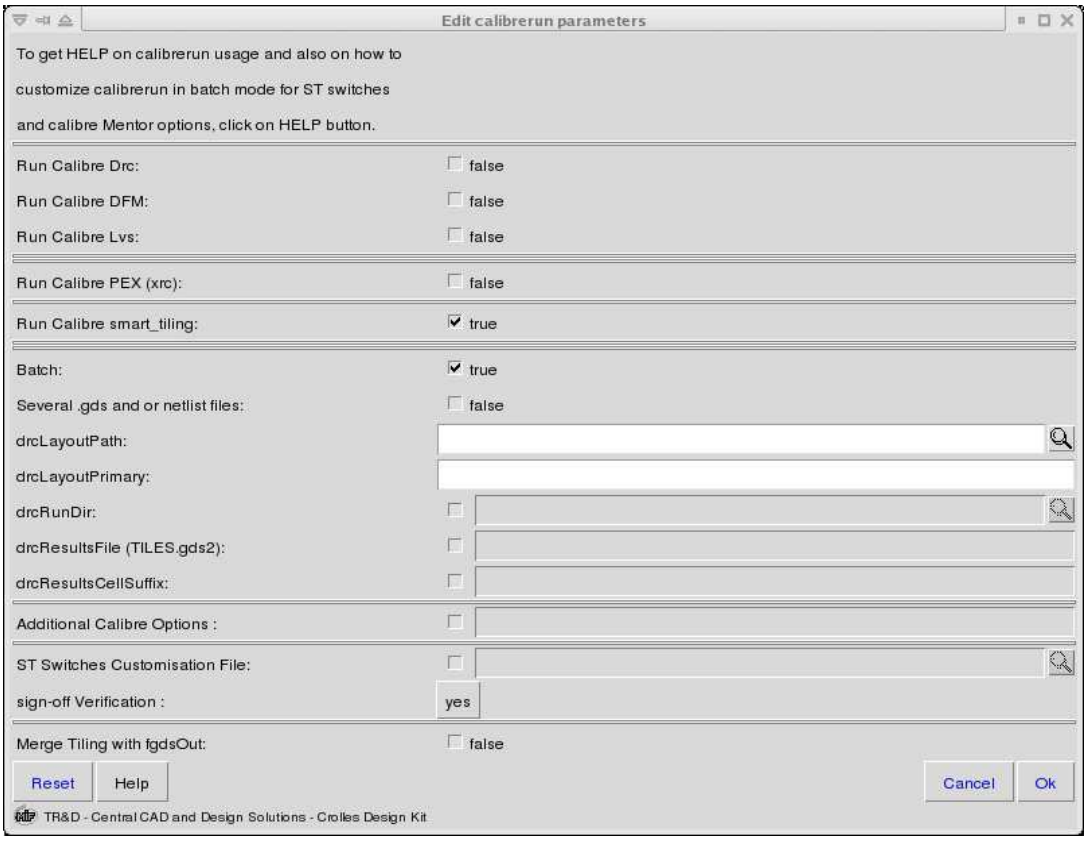

4.2 - Smart tiling flow

The flow of the smart tiling is made of two main steps:

1. Tiling with eMetro Structures:
The eMetro structures are aimed to monitor the technology process during the fabrication of the chips in fab. Tiling with eMetro is mandatory for technologies cmos032/cmos028 as it is very difficult to process a chip in these technologies without adjusting the process parameters (temperature, etching,etc.) all over the chip in real time.

Formerly, the tiler was in charge of instantiating eMetro. But it appeared that some of the designs were too dense for this. So it has been decided to handle eMetro instantiation at floorplan.
Before running the tiler, a DRC is run to check that enough eMetro have been used.
If one or several eMetro are not enough instantiated, related tiling pass can be enabled in the tiler GUI.

FE and BE eMetro are also generated in separated gds for archive.

2. Tiling with Front-End/Back-End tiles:
Tiling with Front-End and Back-End tiles allows to add tiles of layers PC/RX, metals, vias and MIM in order to achieve the density constraints over specific devices and the whole chip. FE/BE Tiles are added after eMetro.

In case of metal fix, there are two possibilities:

1.If you order first FE masks for a PG, and note during the following week that some metal mask modification are needed: the designer will restart the flow from the reference db (design gds + FE eMetro + FE tiles + BE eMetro) that he will tile with BE layers only, before ordering BE masks.
2. If after PG, you need a metal fix: you will try to modify a minimum number of masks.

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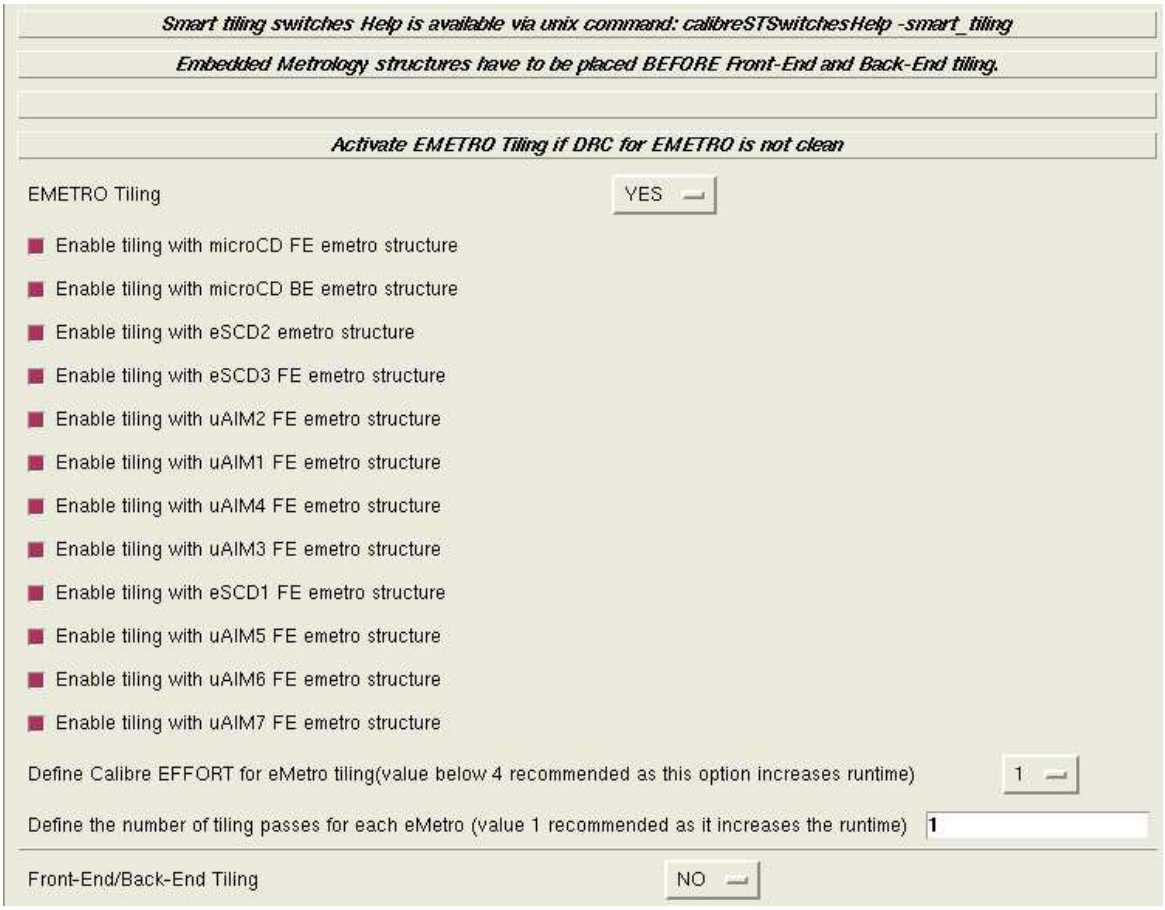
In processes with no via-tiling, it was easy to re-generate a single level of metal fill.
But doing so now would leave some dvia not enclosed by metal, and generate DRC errors.
A Calibre DRV macro (PROMOTE) is provided in the DK to help designers performing fast and simple metal fix, despite via-tiling: please, check available slide in DK doc directory.

4.3 - Customization window (GUI only)

In this window, one can choose to run the tiling flow of the eMetrology or the flow of Front-End/Back-End tiling.

* The eMetrology flow is generally ran first on the input GDS to generate eMetrology structures which should be placed on the initial GDS of the circuit before the Front-End/Back-End tiling step.
eMetro structures are tiled to monitor the process correctly, even in the middle of big chips (structures in sealring may be too far from chip center to monitor it).



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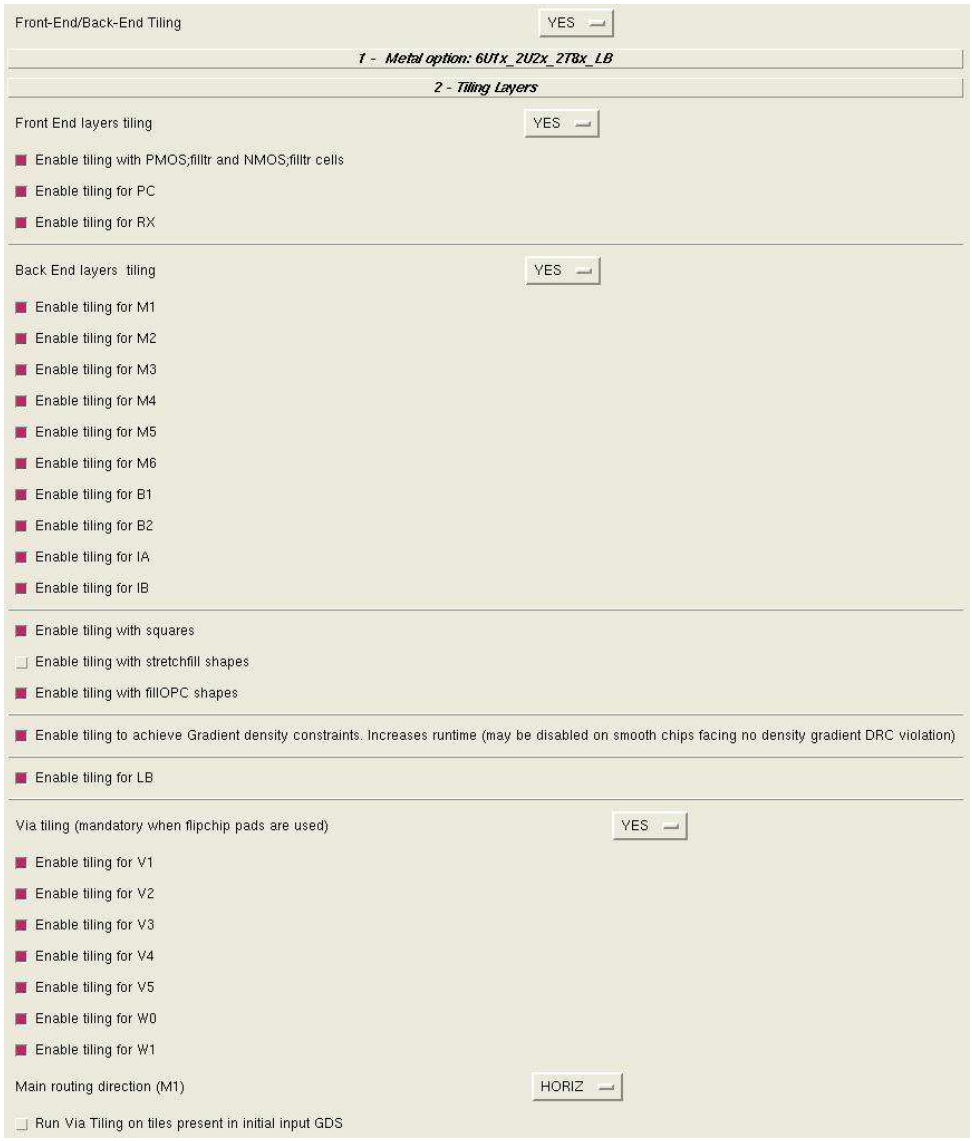
*The basic tiling flow (“FE/BE tiles”, as opposed to “eMetro”) allows to enable/disable all layers to be tiled.



Section1:
- The metal option cannot be modified: it is aligned on the loaded DK
- By default, the density targets are those intended for Top level tiling (45% for metals and LB, min DRC density target for PC/RX).

Section2:
Switches are available to select/unselect PC/RX tiling, metal tiling, via tiling, and the direction of M1 routing (following metals will be tiled alternatively in horizontal and vertical direction).
All layers are individually selectable. One can also select individually the type of the shapes to tile with (rectfill, stretchfill or fillOPC), but you need process engineer agreement for this.

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"Enable tiling to achieve Gradient density constraints. Increases runtime (may be disabled on smooth chips facing no density gradient DRC violation)":

To speed up dry-run, you can disable this switch. It remains interesting for the final sign-off tiling, as even if no gradient violation is witnessed, it helps to smooth the chip.

"Main routing direction (M1)":

It is easier for the tiler to fill the chip trying to instantiate metal stripes in routing direction. It is easier to identify this direction by looking at high metal level (each level is tiled in an orthogonal way).

"Run Via Tiling on tiles present in intial GDS":

Via tiling can be added on dummy metal present in the initial gds when possible.
Designers may want to prevent via tiling to impact pre-existing tiles (protecting symmetrical structures from device mismatch for example). This feature is thus turned off by default. Turn it on increases dummy via density.

Section3:
Some devices require specific tiling (ie: have specific density rules). But, there are no such devices in this process for now.

Section4:
Some "expert" options are available in this section.
They can be modified only with technologists and/or DK team's agreement: a gds, even DRC clean, may be refused otherwise.

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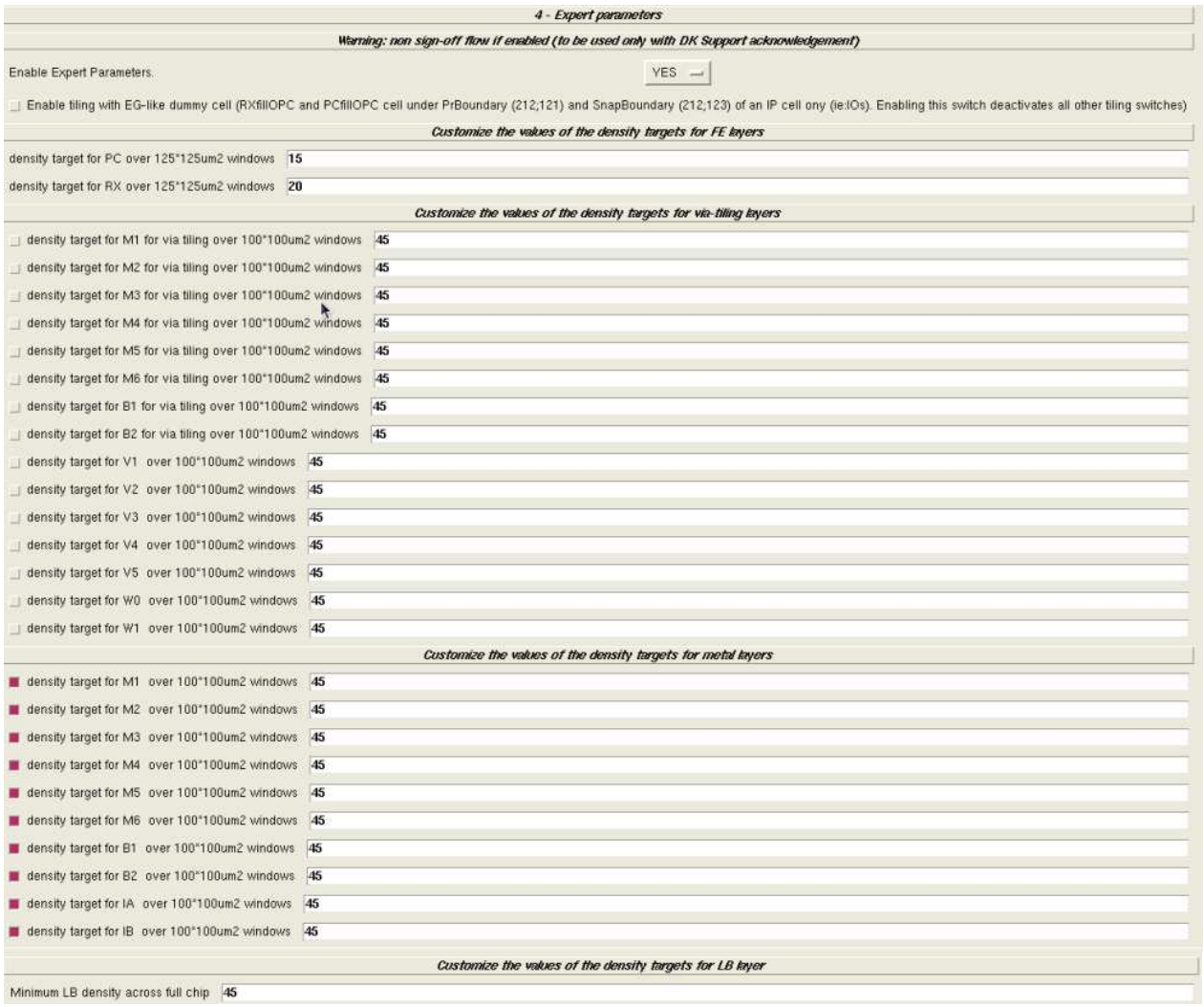

*EG-like dummy cell switch can be turned on to tile with RXfillOPC and PCfillOPC. This feature is aimed to be used only for tiling ST IOs with poly density errors. To enable this feature, PrBoundary (212;121) or SnapBoundary (212;123) need to be drawn over the region which needs to be tiled. Otherwise no tiles will be generated. Be aware that switching on this option will turn off all the others switches (e.g. tiling with RXfilltr dummy transistors)

*All targets can be fine-tuned here: for FE layers, for via-tiling process, and for BE layers.
* The tiler is computing density, based on a process window.
If your main goal is to avoid min density violation, set the last switch to “LOW_DENSITY”: the tiler will work with a big window, similar to the one used for min density rules in DRC.
If your main goal is to avoid max density violation, set the last switch to “HIGH_DENSITY”: the tiler will work with a small window, similar to the one used for max density rules in DRC. This is the default of the tiler.

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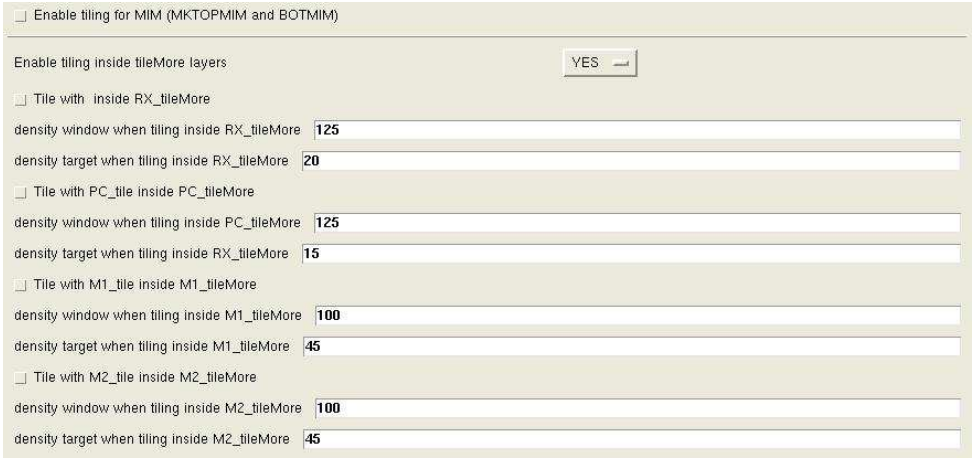
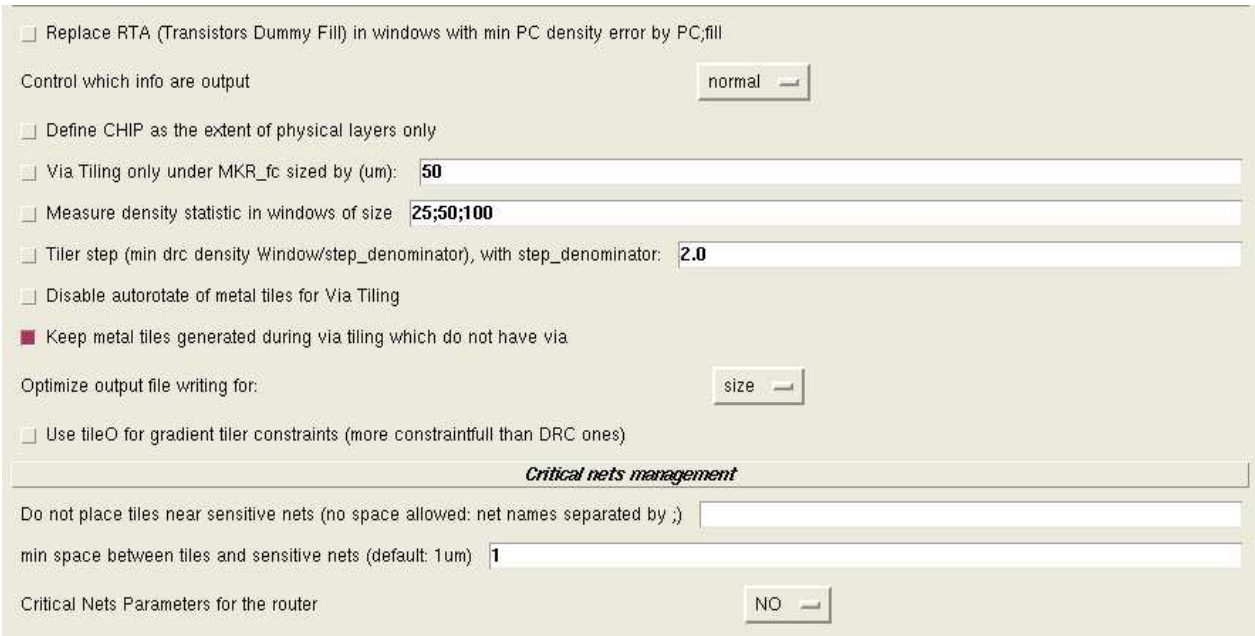


*MIM tiling is no more mandatory, but remains available (as other deprecated features) in expert parameters, to fast deployment in case of new recommendation from process engineer.

*<layer>_tileMore are available for all stacks, and provide a simple workaround to the designer when he faces a tiling problem in rush time, and cannot wait for a patch. The tiler will have an extra pass focusing on this layer, which can help to locally increase a layer density. If you need to use this feature, then you must also enter a ticket to DK team.



*”***Replace RTA (Transistors Dummy Fill) in windows with min PC density error by PC;fill”**
Dummy transistors (PC;filltr/RX;filltr) are used instead of simple PC;fill/RX;fill with a tremendous positive impact on yield for several identified reasons. You should not enable this feature without process engineer agreement, or you may have your gds blocked at PG level.

“Control which info are output”
Different types of info may be output for debug purpose:

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	Normal	Verbose	Debug
debugTiling	**0**	**1**	**1**
debugStepGds	**0**	**0**	**1**
debugStep	**0**	**0**	**1**

With
- debugTiling: generates in the run directory (names can be slightly different)
  - areaToFill_layerToFill_passi.oas, contains the area to be filled for each layer
  - outConstrainArea_layerToFill_passi.oas, contains the area not to fill for each layer and each pass (I.e all the exclusion area regarding all the constraints)
  - outConstrainArea_layerToFill_pass_i_layerConstrains.oas,contains the area not to fill for each layer and each pass, constrains by constrains.
  outConstrainArea_layerToFill_passi.oas = outConstrainArea_layerToFill_pass_i_layerConstrains1.oas OR outConstrainArea_layerToFill_pass_i_layerConstrains2.oas OR outConstrainArea_layerToFill_pass_i_layerConstrainsN.oas
- debugStepGds: generates in the run directory
  - A layout for each layer and each pass, name: TILE_layer_passi.oas, contains all the fill shapes generated during the regarded pass
- debugStep: generate in the run directory a RDB file for each pass DFMFILL_layer_stepi.rdb, this database contains density gradient number of fill shape before and after the pass (read Mentor documentation about it).

"Define the layer CHIP as the extent of all physical layers only"
That is to say: "CHIP=EXTENT ALL_PHYSICAL_LAYERS" (bbox of the physical layers) instead of "CHIP = EXTENT DRAWN ORIGINAL" (bbox of all polygons in the db) which is default.

"Via Tiling only under MKR_fc sized by (um)"
You can reduce via-tiling to the vicinity of bumping pads, with process engineer agreement only (not safe!).

"Measure density statistic in windows of size"
To output density statistic in rdb files, by setting your own process window size of interest.

"Tiler step (min drc density Window/step_denominator), with step_denominator:"
To modify the tiler step (increase the step_denominator will reduce the tiler step and increase the runtime).

When modifying the tiler step, you may meet 2 common errors:

* **Error DFM137** on line 6042 of SVRF generated from TVF - FILLSHAPE is too big relative to the WINDOW.

=> the max size of the fill shape must be smaller than the step (aka "atomic window").
Ex: fill shape max length is 4.5, window size is 50:
step = window_size / step_denominator = 50/8 = 6.25 (> 4.5): the fill shape can be added in an atomic window
step = window_size / step_denominator = 50/16 = 3.125 (< 4.5): the fill shape cannot be added in an atomic window (DFM137 error)

* **Error DFM193** on line 2228 of SVRF generated from TVF - The analysis/gradient window size is not a multiple of the step: step.

step = window_size / step_denominator = 50/12 = 1.666... : this is a non-decimal number leading to DFM193

"Disable autorotate of metal tiles for Via Tiling"
If you want to prevent metal fill added during via-tiling to be rotated once main direction has been tried.

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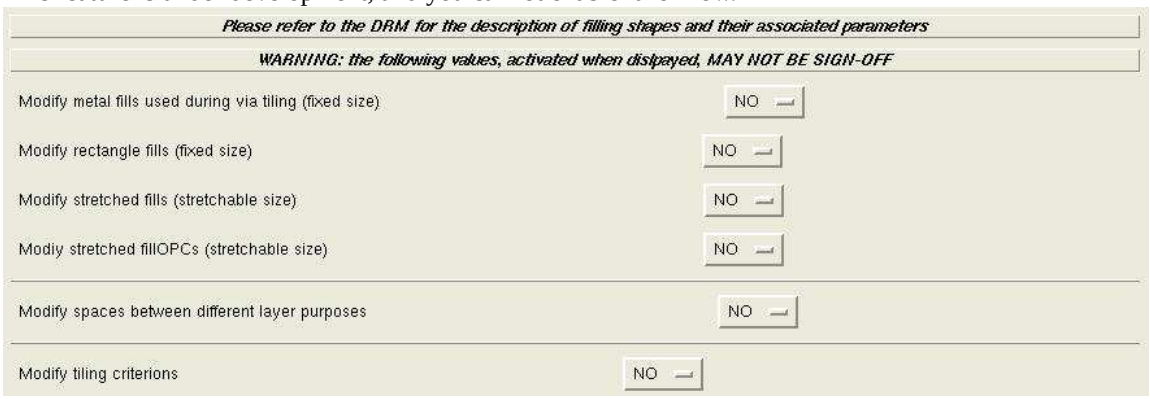
"Keep metal tiles generated during via tiling which do not have via"
Formerly, tiling target was not 45% for all tiler passes, to be able to later manage gradient more easily. That is why metal fill added during via tiling pass were not kept if not required by any dvia.
As all passes targets are now 45%, this metal fill with no dvia are kept.

"Optimize output file writing for"
size or runtime. This advanced feature is still under study: keep the default value (size).

"Use tileO for gradient tiler constraints (more constraintfull than DRC ones)"
tileO/fillOPC should not have an important impact on gradient, and requires some runtime. In case of gradient problem, you may try to enable this switch.

"Critical net management"
This feature is under development, and you cannot enable it for now.



Most of the parameters listed in the DRM (tiler section) can be customized here with process engineer agreement: Tiler passes and the size/step/offset of related fill shapes, and tiling criterion.

Global Expert Parameters do apply to both eMetro and basic tiles.
-Turbo Flex decrease runtime in MTFlex mode (LSF).
-4 GDS are now generated to ease archiving for future ECO. But you may prefer a single gds to fast a dry run.
- To encourage dry-runs, you also have the ability to automatically merge the files generated by the tiler with the initial design in a new global file.

4.4 - Outputs

In the Smart Tiling Run Directory, there are two output files:

- By default, FE/BE Tiles are enabled, two files <topcell>.tiles_FE.gds and <topcell>.tiles_BE.gds are generated.
- For a dry run with both eMetro and FE/BE Tiles selected, 4 gds files (<topcell>.eMetro_FE.gds, <topcell>.eMetro_BE.gds, <topcell>.tiles_FE.gds and <topcell>.tiles_BE.gds) are generated.
- When the global expert switch "Generate 4 Gds files…" is deselected, only one output gds file is generated with the name specified by the user in the gui of the tiler or via calirberun options when smart tiling is ran in batch.

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- In batch mode, an option “merge Tiling with fgdsout” is available from Calibrerun menu and enables one to get tiling and original GDS file merged in a new GDS file. **This should not be used as it does not work anymore. Merging has to be performed manually through “calibredrv -a layout filemerge …” command. Please note that before merging you ran run following command to get rid of small squares of 1nmx1nm generated during eMETRO insertion: calibredrv scriptPath/TCDcleanning.tcl <gds path>.**

4.5 - IP-check Flow:

The IPs should be delivered with no tiles, to ensure tiling uniformity at top level and ease gradient management during top-level tiling.

In specific cases, the designer may want to protect some sensitive areas (from tiles). It is recommended to use, as less as possible, Mi;tileNot (or Mi;Exclude, depending on the process) markers.

MKR;tileNot must be avoided: do not use it to protect only M1 sensitive area for example, it may generate later useless gradient problems. Please use instead M1_tileNot only in this case.

Whether the IP is delivered not tiled, or partially tiled, the IP/block provider (internal or external) must run the IP-checks.

The IP Check flow is the following:

- Tile the IP (tiler default settings)

- Add Mi;tileNot on sensitive areas: under this marker change Mi;fill/Mi;fillOPC into Mi;dg (for these shapes to be considered in next step)

- Perform the parasitical extraction (optimize the design until you get correct results)

- Run the DRC with IP-check switch activated (optimize the design until you get correct results). This step can be done now in the tiler by using the new feature “Run IP-Check DRC rules after tiling”.

- Remove Mi;fill from your IP (Mi;fill under Mi;tileNot, will remain on the IP)

- Deliver

The tiles generated at top level will be different than the one generated at IP level during the dry run (the considered bbox is different).

The IP-check DRC density rules are more stringent than the top level ones, and ensure that your IP instantiation at top level will generate no min/max density rule nor gradient violation (process windows offset problem):

- The step is much smaller (more process windows are checked, increasing the density violation detection number)

- Min density is slightly higher, max density slightly lower

- Extra density rules are added to check that the tiler will be able to manage the IP edges to ease gradient smoothing when the IP will be abutted to others (very low/high density process windows are forbidden on the edge of the IP)

If for some reason, your IP is delivered with tiles, IP-tiling rules must also be checked.

5 - FILLING GENERATION DETAILS

Description of each layer filling is provided in the DRM.

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