28FD MOSFET mismatch model description and usage

SPICE modeling team

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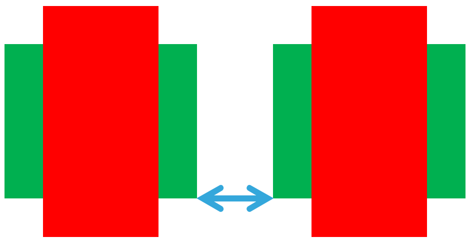
life.augmented

MOSFET mismatch model

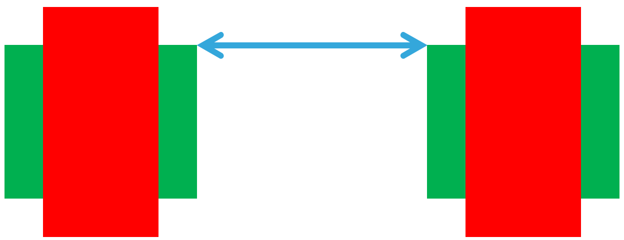
MOSFET matching in 28FDSOI

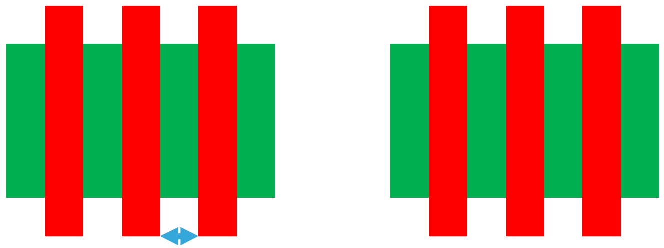
- In 28FDSOI technology, MOSFET local variability is not only device geometry dependent but also **distance dependent**

- Two illustrations:

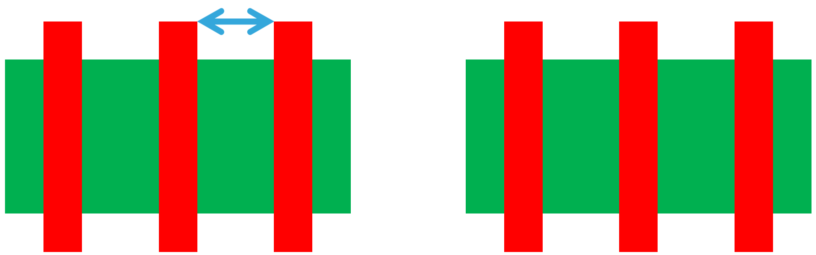


is different from



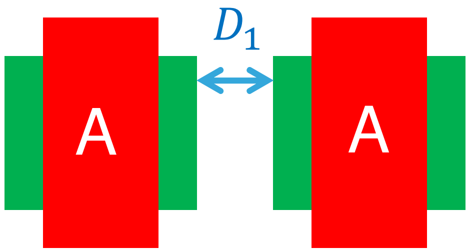


is different from

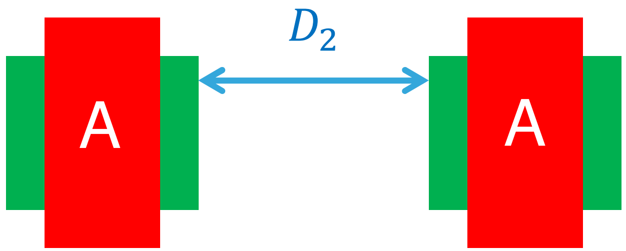


Consequences for a single device

- For a given device multiplicity (illustrated here with M=2), local variability σ is smaller for larger distance between device elements

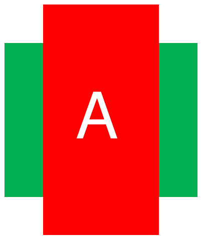


σ_{D_1}

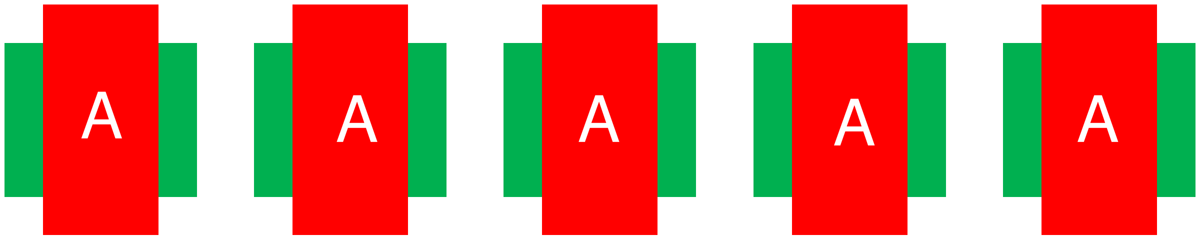


$\sigma_{D_2} < \sigma_{D_1}$ $for\ D_2 > D_1$

- Standard deviation of local variability is not proportional to the inverse square-root of device multiplicity (illustrated here from M=1 to M=5)



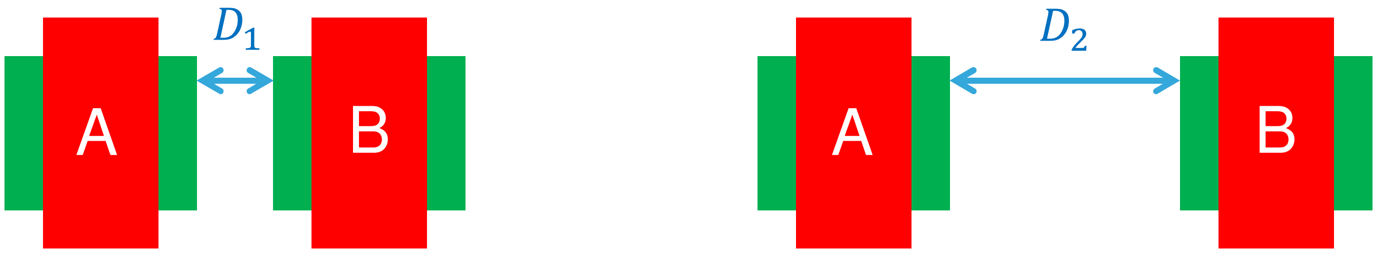
$\sigma_{M=1}$



$\sigma_{M=5} > \sigma_{M=1}/\sqrt{5}$

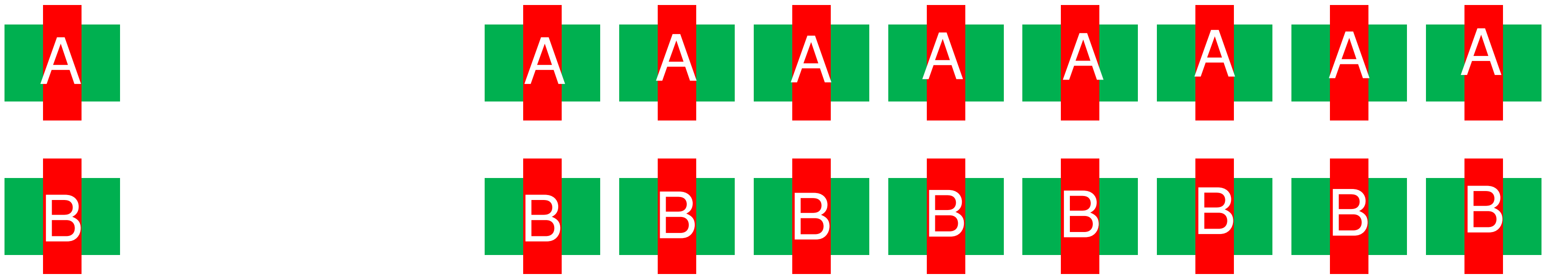
Consequences for a device pair

- Mismatch σ_Δ between two MOSFETs is larger for larger distance between them



σ_{Δ,D_1} $\qquad$ $\sigma_{\Delta,D_2} > \sigma_{\Delta,D_1}\ \ for\ D_2 > D_1$

- Standard deviation of mismatch is not proportional to the inverse square-root of device multiplicity

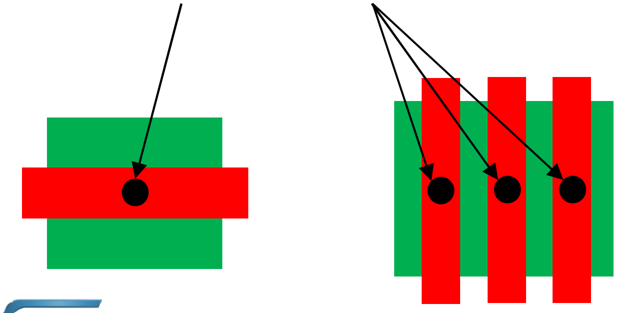


$\sigma_{\Delta,M=1}$ $\qquad$ $\sigma_{\Delta,M=8} > \sigma_{\Delta,M=1}/\sqrt{8}$

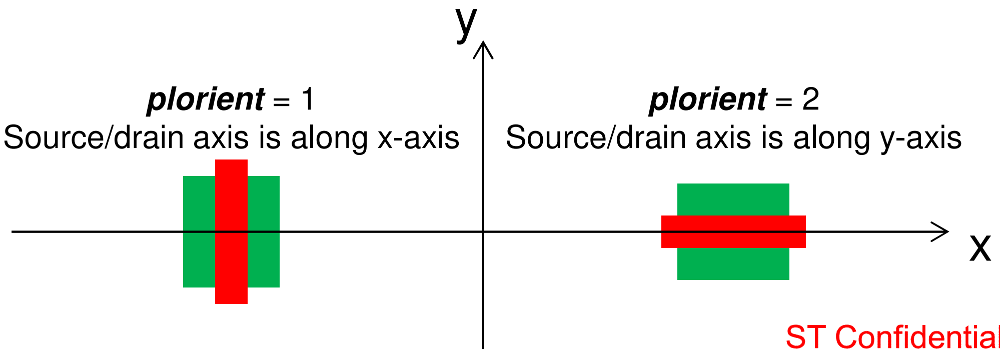
MOSFET mismatch model

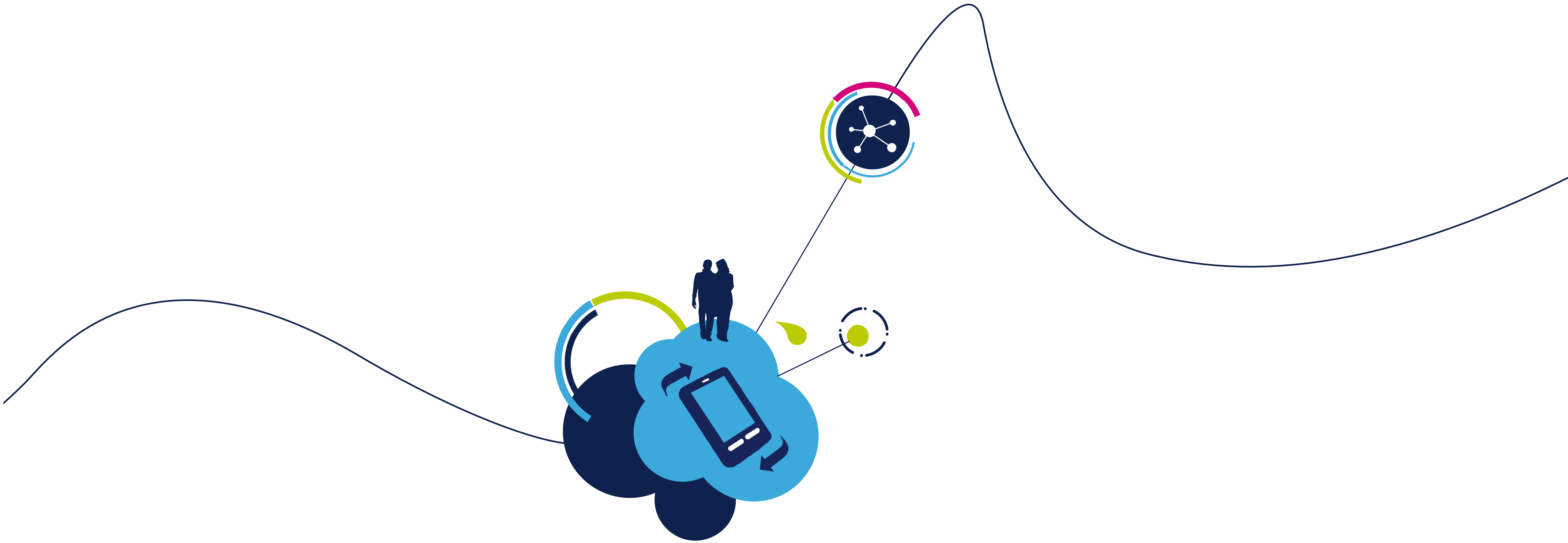
- This distance dependence of local variability is accounted for in 28FDSOI **Monte-Carlo simulations**
- To achieve this, both LOT and DEV random variables are used in the model. Therefore, any option restricting the activation of LOT or DEV variables has to be **prohibited** (see slides 26-29 for settings within ArtistKit)
- In post-layout simulations, such a feature is made possible through the extraction by LVS of transistor centroid position (***xpos***, ***ypos***) and orientation (***plorient***), as instance parameters

For each device instance,
centroid coordinates (***xpos***, ***ypos***) are extracted



For each device instance, orientation is extracted
according to the following convention





MOSFET matching simulations from schematics

Anticipating post-layout simulation

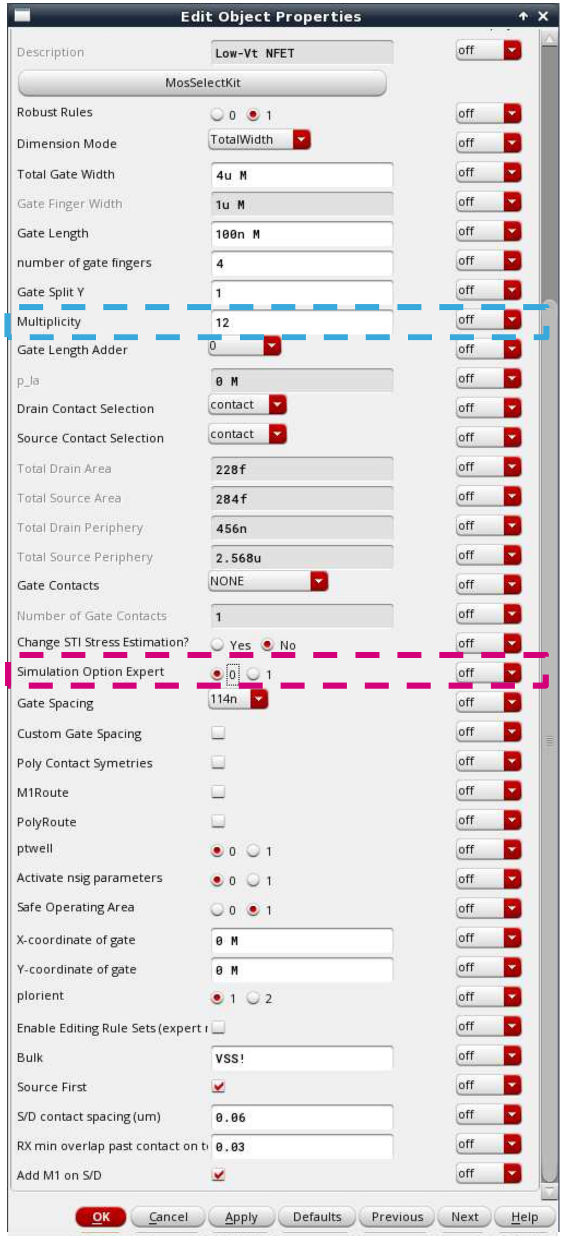
- In order to ease the optimization of matching, an option is offered in 28FDSOI models to correctly simulate these distance dependence effects from schematics, without the need for a layout

- In this “schematic mode”, MOSFET mismatch model enables the use of a single instantiation to simulate multiple devices featuring regular arrangement, as described in the following slides

- In addition to (***xpos***, ***ypos***) and ***plorient***, new instance parameters are required to describe the arrangement of devices: number of rows/columns and pitch between rows/columns

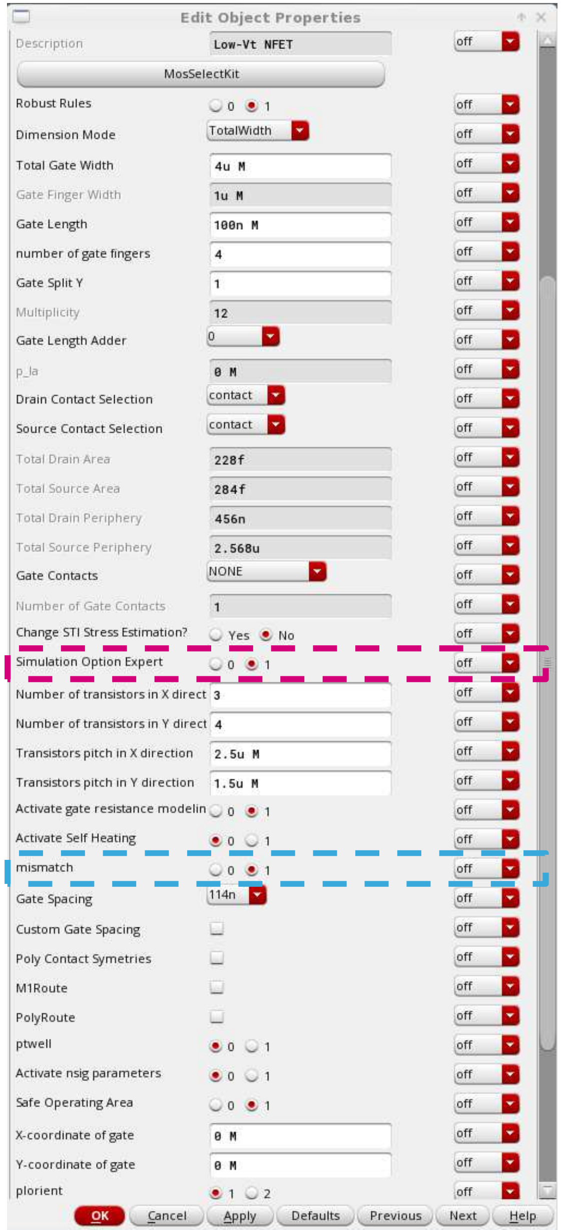
- These instance parameters are only relevant in schematic since, when layout is available, LVS extracts one instance per device

Introduction to expert mode



- By default, Simulation Option Expert flag is set to 0
- In this case, simulation of multiple devices is performed by specifying the number of devices in parallel, using Multiplicity parameter
- Since distances between devices are not known, their effect on matching cannot be accounted for and devices are thus assumed fully uncorrelated
- As a result, standard deviation is proportional to the inverse square-root of Multiplicity, which may lead to inaccurate estimation of matching

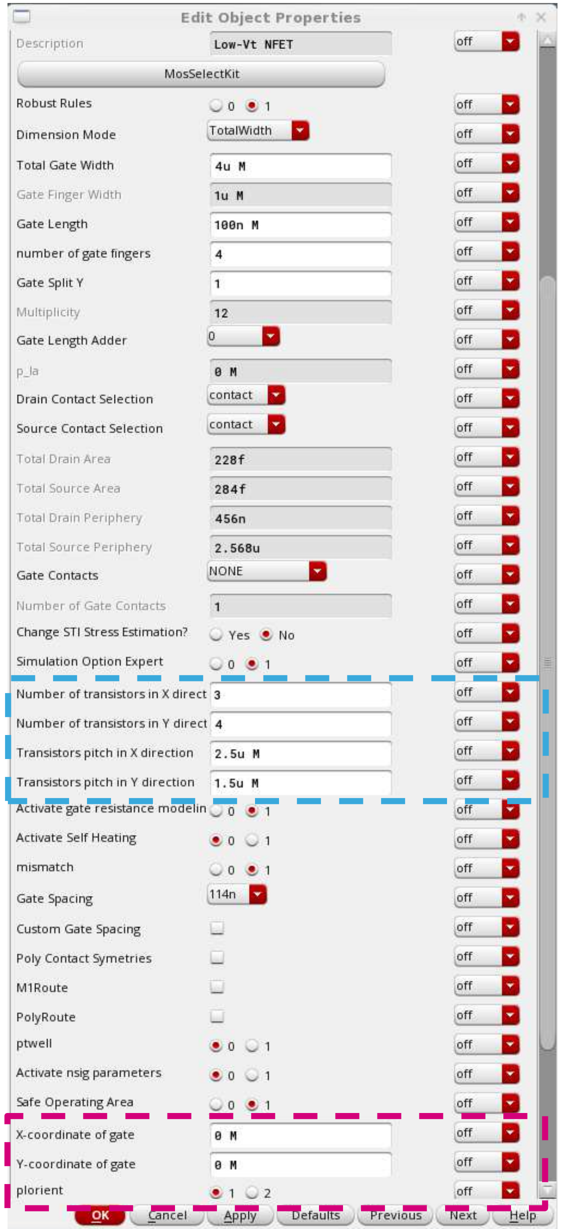
Activation of the mode and warning



- The mode in which mismatch between multiple devices can be accurately simulated from schematic is accessible in expert mode:
  - "Simulation Option Expert" has to be set to 1
  - Of course, "mismatch" has to be set to 1 (default)

- Important warning:
  - In this **schematic** mode, only the **standard deviations** can be exploited. The distribution tails provided by the Monte-Carlo simulations may be non-physical in some cases
  - In order to get exploitable **distribution tails** in all configurations, **post-layout** Monte-Carlo simulations have to be used

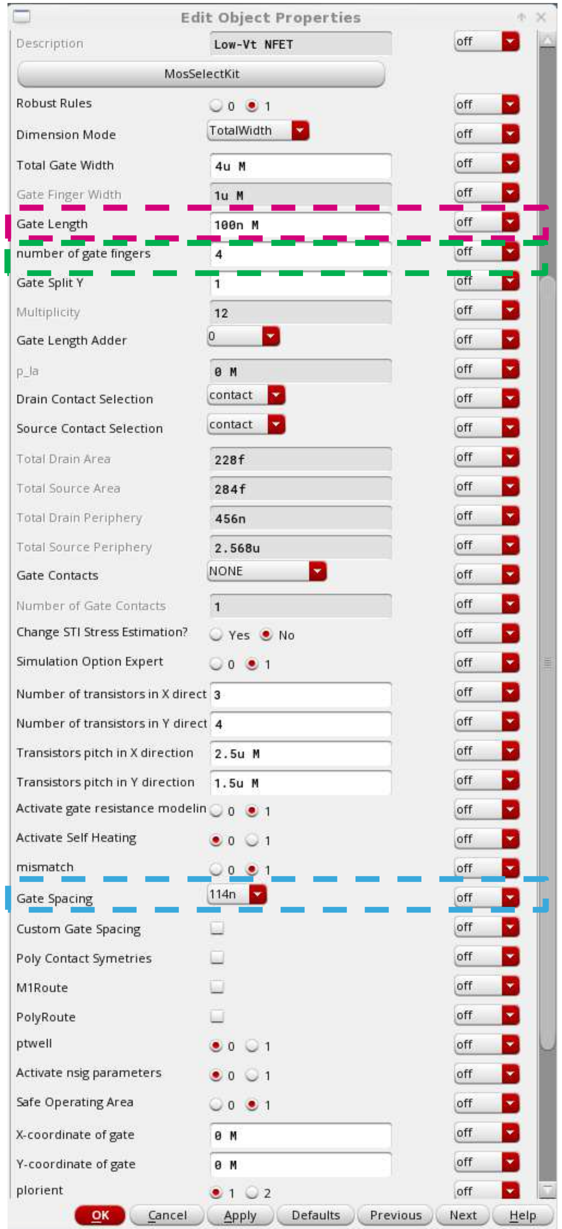
Definition of instance parameters



- Parameters normally extracted during post-layout simulations have to be entered in case of simulation from schematics
  - ***xpos*** X-coordinate of the bottom left device element centroid
  - ***ypos*** Y-coordinate of the bottom left device element centroid
  - ***plorient*** Orientation of the transistor

- In addition, specific instance parameters are used to describe the arrangement of multiple transistors
  - ***mx*** Number of transistors in X direction
  - ***my*** Number of transistors in Y direction
  - ***deltax*** Pitch between transistors in X direction
  - ***deltay*** Pitch between transistors in Y direction

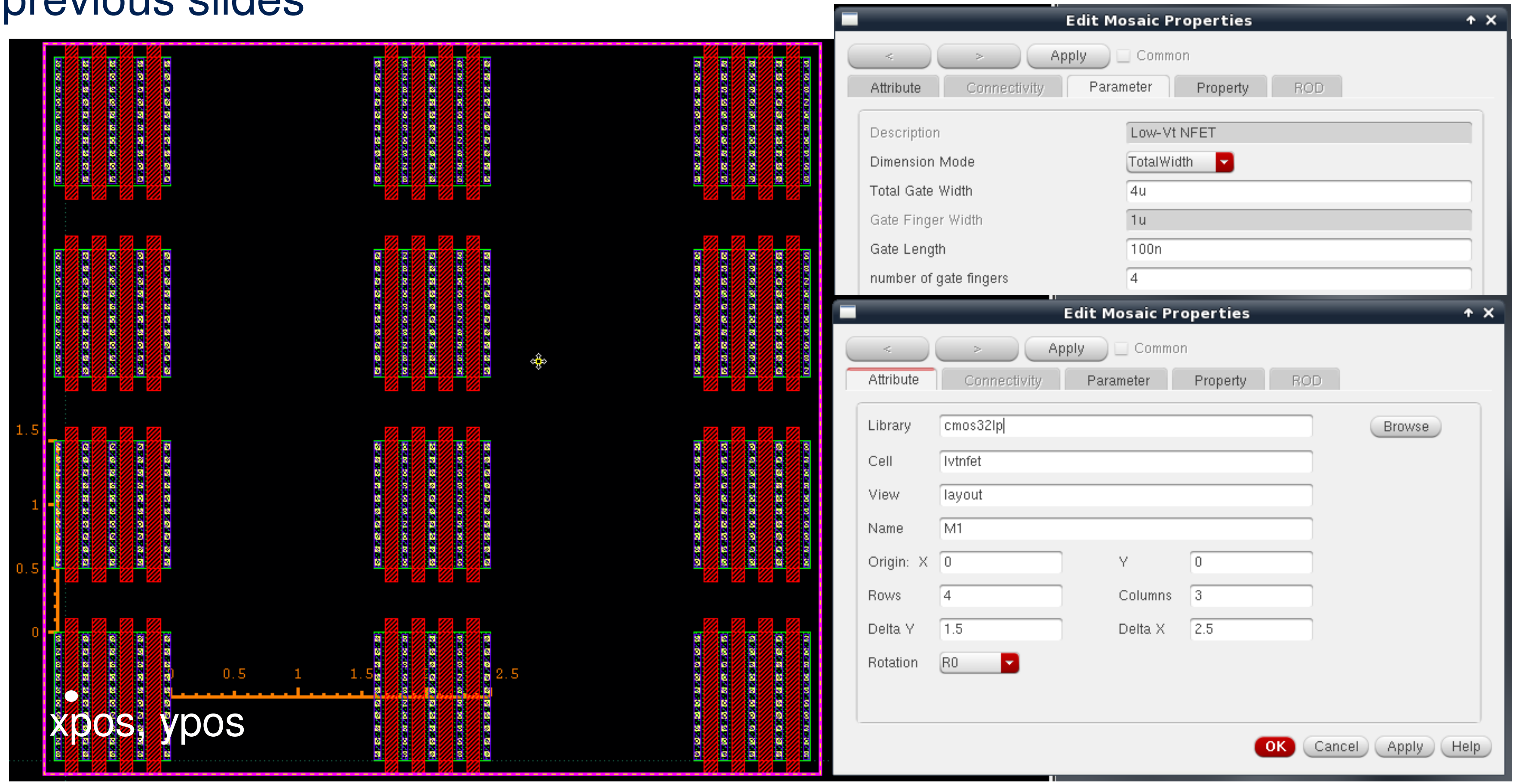
Definition of instance parameters



- Multiple multi-finger transistors can be instantiated by combining ***nf*** > 1 with the parameters described in previous slide
- In multi-finger transistors, the pitch between consecutive fingers is given by ***L***+***sd***

Illustration: Multiple devices in 2D array

- Layout view of the 2D array case corresponding to the snapshots of previous slides

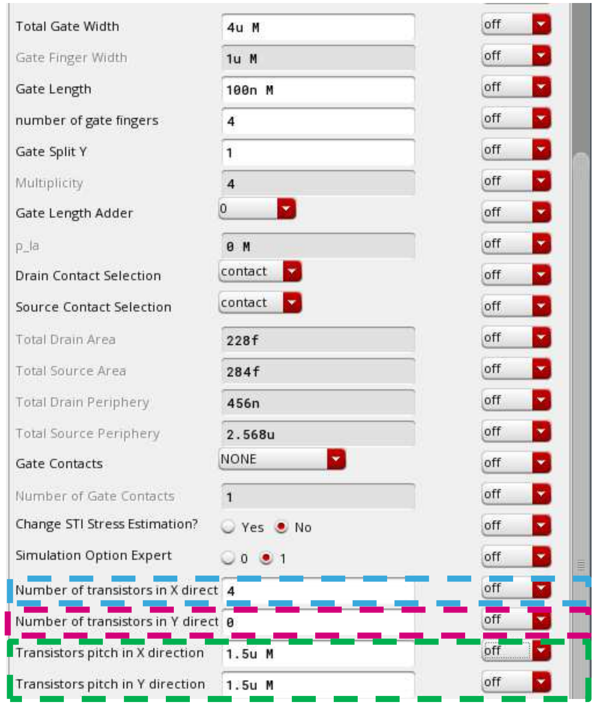


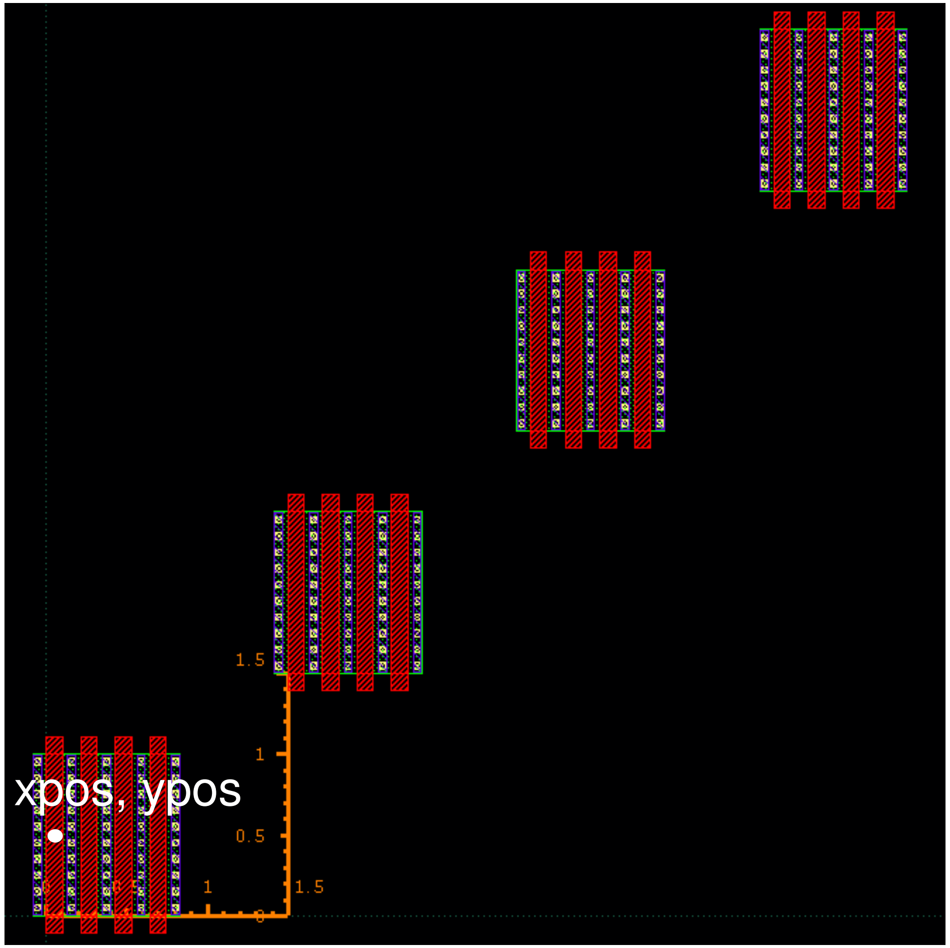
mx = 3
my = 4
nf = 4

deltax = 2.5µm
deltay = 1.5µm
sd+L = 214nm

Illustration: Multiple devices in 1D array

- The specific value ***my***=0 is used to describe a 1D array of ***mx*** transistor elements aligned with a pitch given by ***deltax*** and ***deltay*** in x and y direction, respectively



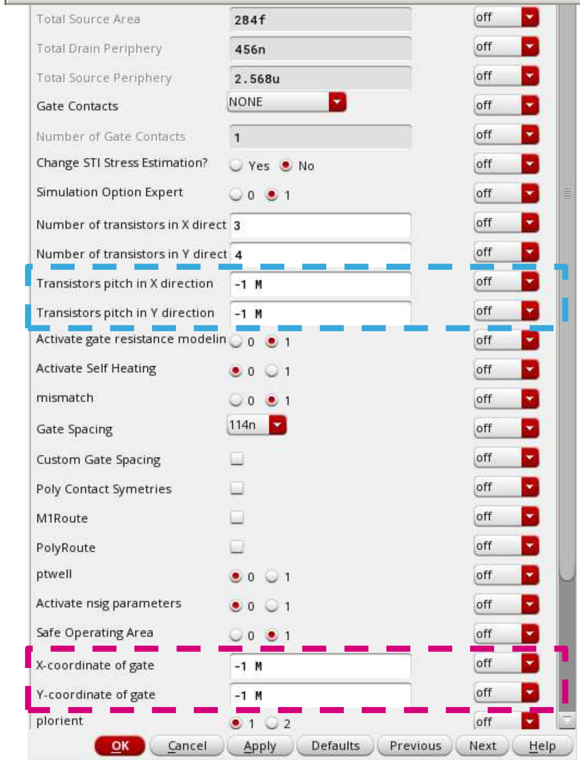


mx = 4
my = 0
nf = 4

deltax = 1.5µm
deltay = 1.5µm
sd+L = 214nm

Use of instance parameters

- When ***mx***>1 and/or ***my***>1 configuration is used, instance parameters describing the position of transistor elements (***xpos***, ***ypos***, ***deltax*** and ***deltay***) are required

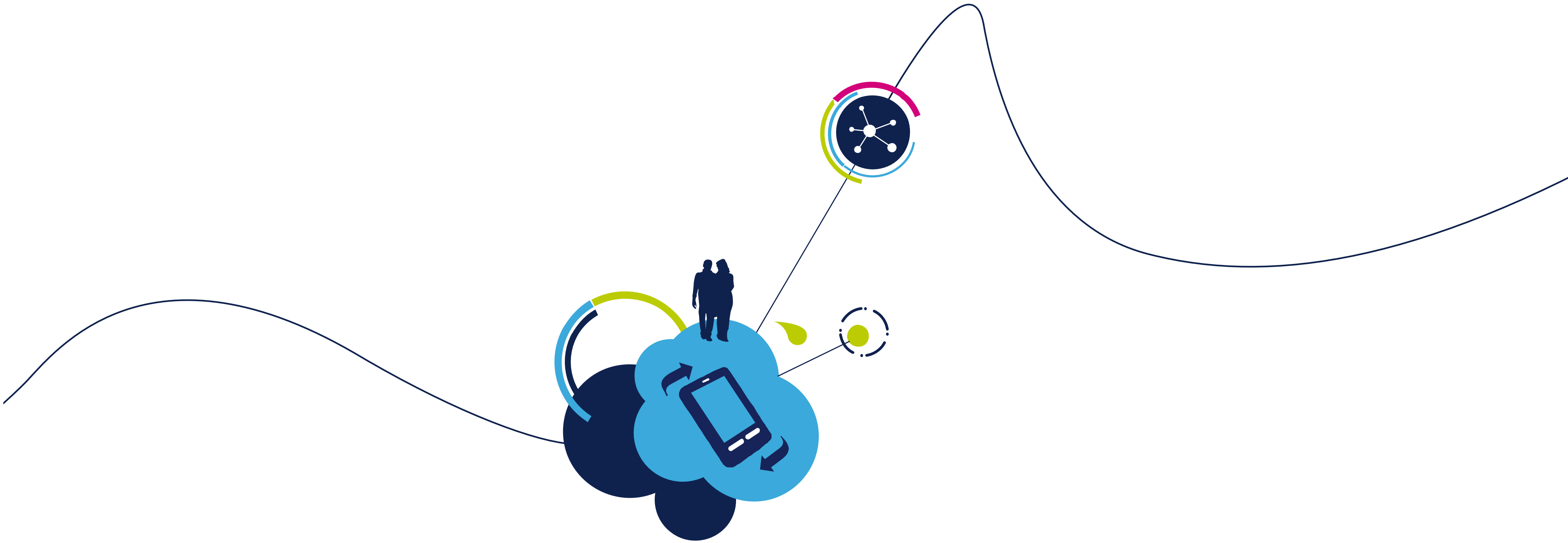


- Otherwise, a warning message pops-up, indicating that the simulation result could be meaningless

Default behavior of the model

- When ***xpos*** and/or ***ypos*** are not given or set to -1
  - Correlations between transistors and between parts of multiple transistors are ignored
  - This corresponds to the case where device elements are assumed very far one from the others
  - In that case, usual behavior is obtained (i.e. results follow Pelgrom's law). In particular, mismatch standard deviation is inversely proportional to transistor multiplicity

- Special case of multi-finger transistors
  - The correlation between fingers of a multi-finger transistors is **always** accounted for, even if ***xpos*** and/or ***ypos*** are not given or set to -1

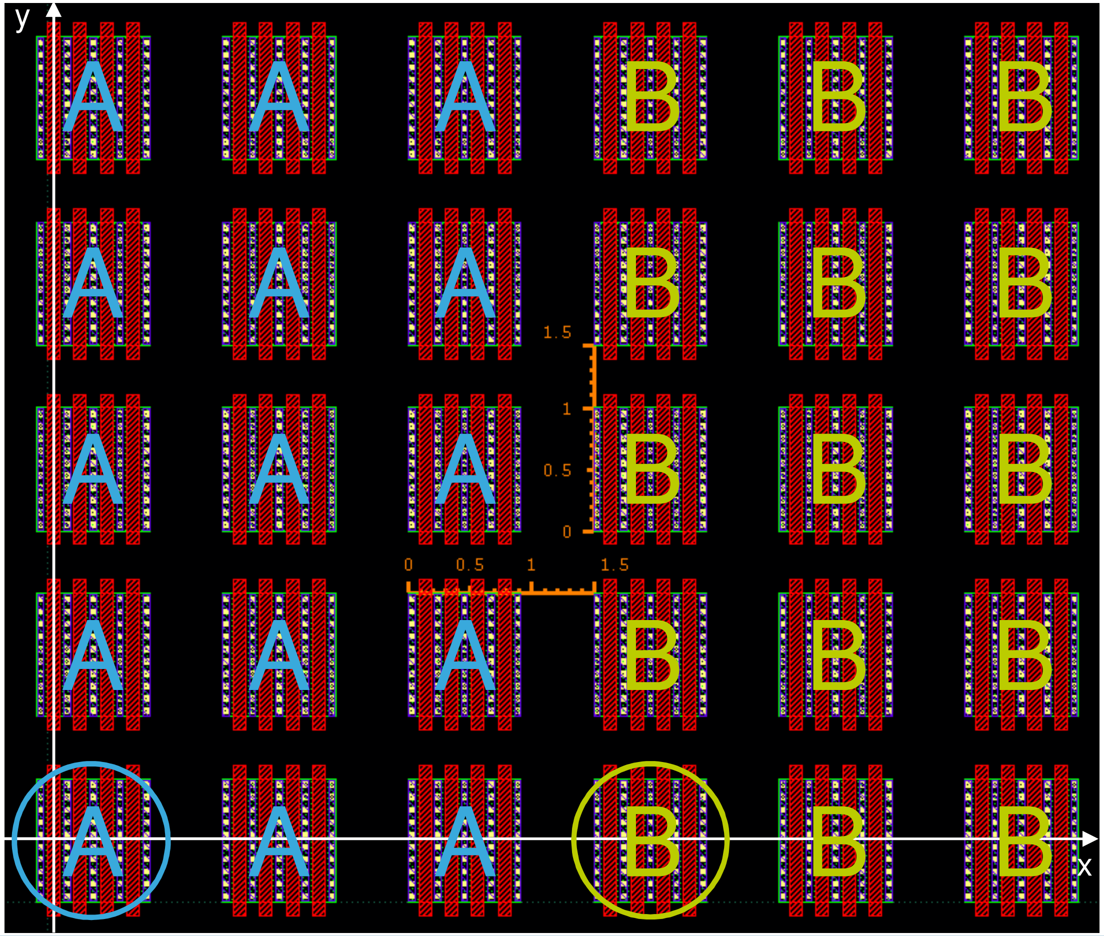


Examples

Description of test cases

- In the following slides, a few examples of multiple transistor instantiations are described
- Layout views are displayed to illustrate the actual configuration
- Multiple MOS transistors are named A, B, C…
- Below the layout view are given the corresponding transistor instantiations in schematics mode
- Notice that the transistor orientation ***plorient*** is set to 1 in all cases

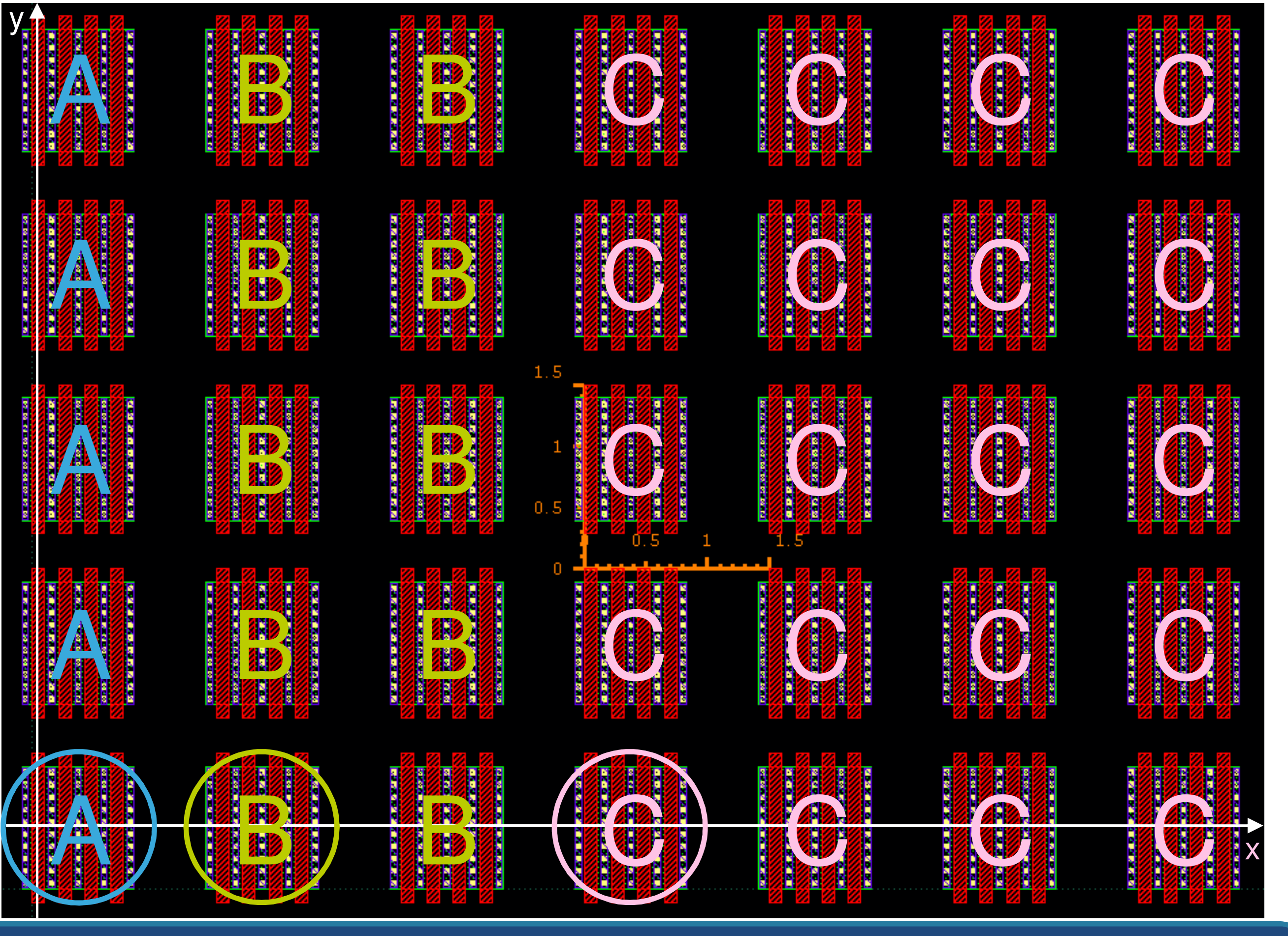
Ex. 1: Two MOS in simple 2D arrays
Only 1 instance per MOS needed



Device A: nf=4 xpos=0 ypos=0 mx=3 my=5 deltax=1.5u deltay=1.5u

Device B: nf=4 xpos=4.5u ypos=0 mx=3 my=5 deltax=1.5u deltay=1.5u

Ex. 2: Three MOS in simple 2D arrays Only 1 instance per MOS needed

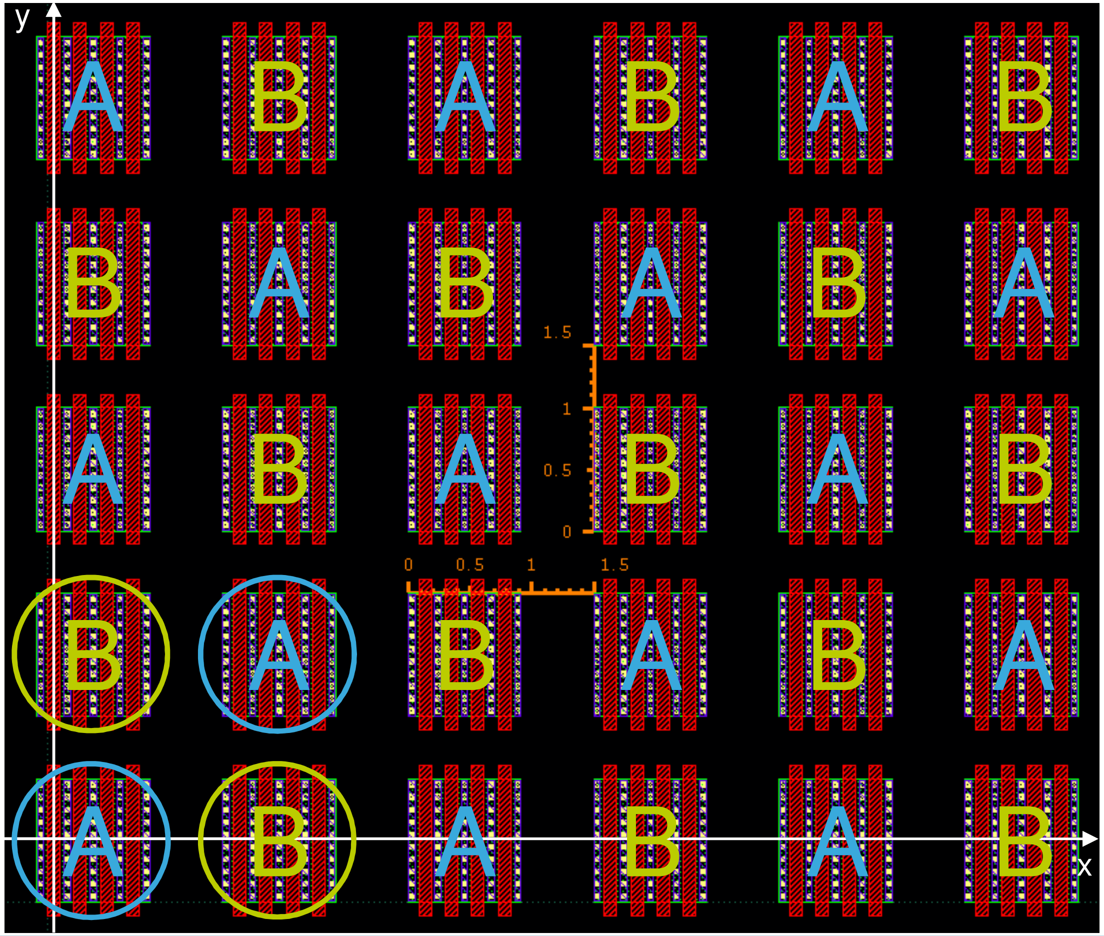


Device A: nf=4 xpos=0 ypos=0 mx=1 my=5 deltax=1.5u deltay=1.5u

Device B: nf=4 xpos=1.5u ypos=0 mx=2 my=5 deltax=1.5u deltay=1.5u

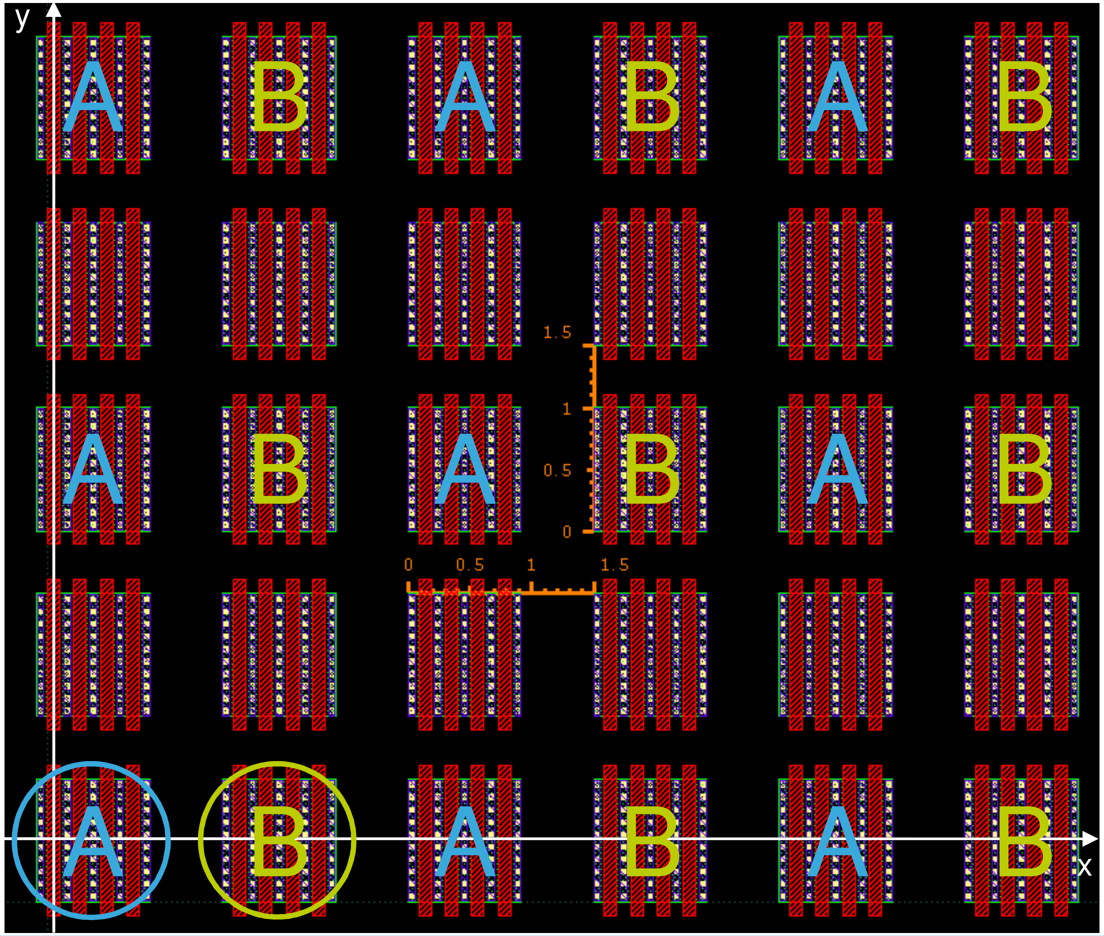
Device C: nf=4 xpos=4.5u ypos=0 mx=4 my=5 deltax=1.5u deltay=1.5u

Ex. 3: Two MOS in interleaved 2D arrays
2 instances per MOS needed (1/3)



Device A1:	nf=4	xpos=0	ypos=0	mx=3	my=3	deltax=3u	deltay=3u
Device A2:	nf=4	xpos=1.5u	ypos=1.5u	mx=3	my=2	deltax=3u	deltay=3u
Device B1:	nf=4	xpos=1.5u	ypos=0	mx=3	my=3	deltax=3u	deltay=3u
Device B2:	nf=4	xpos=0	ypos=1.5u	mx=3	my=2	deltax=3u	deltay=3u

Ex. 3: Two MOS in interleaved 2D arrays
First instance (2/3)



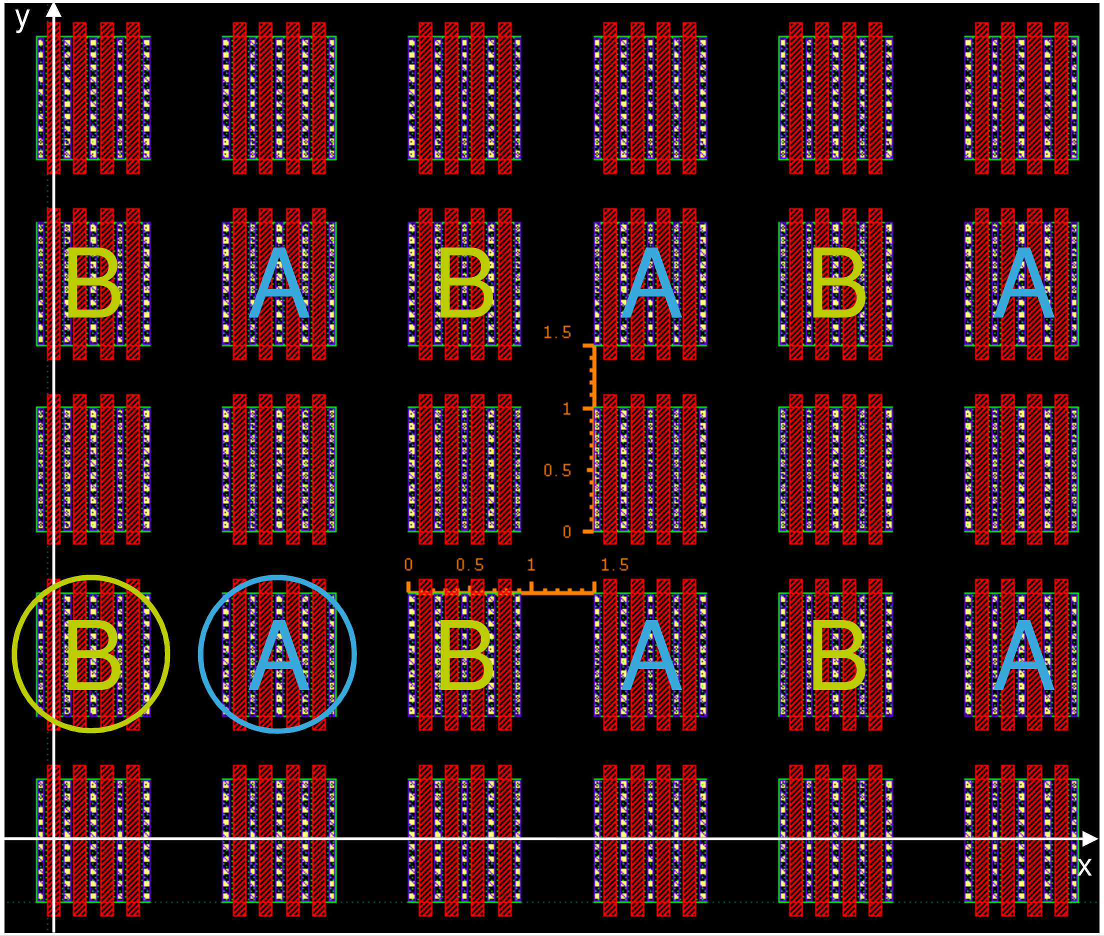
Device A1: nf=4 xpos=0 ypos=0 mx=3 my=3 deltax=3u deltay=3u

Device A2: nf=4 xpos=1.5u ypos=1.5u mx=3 my=2 deltax=3u deltay=3u

Device B1: nf=4 xpos=1.5u ypos=0 mx=3 my=3 deltax=3u deltay=3u

Device B2: nf=4 xpos=0 ypos=1.5u mx=3 my=2 deltax=3u deltay=3u

Ex. 3: Two MOS in interleaved 2D arrays
Second instance (3/3)



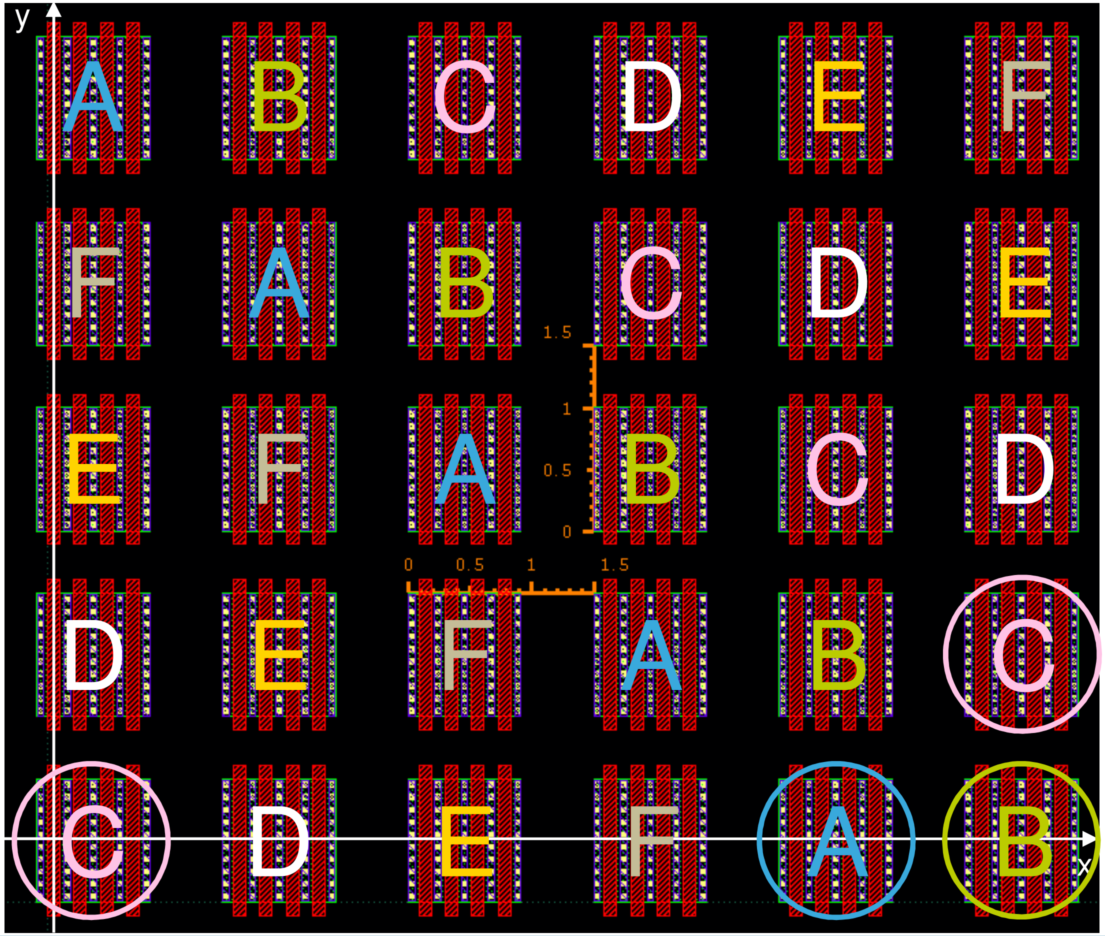
Device A1: nf=4 xpos=0 ypos=0 mx=3 my=3 deltax=3u deltay=3u

Device A2: nf=4 xpos=1.5u ypos=1.5u mx=3 my=2 deltax=3u deltay=3u

Device B1: nf=4 xpos=1.5u ypos=0 mx=3 my=3 deltax=3u deltay=3u

Device B2: nf=4 xpos=0 ypos=1.5u mx=3 my=2 deltax=3u deltay=3u

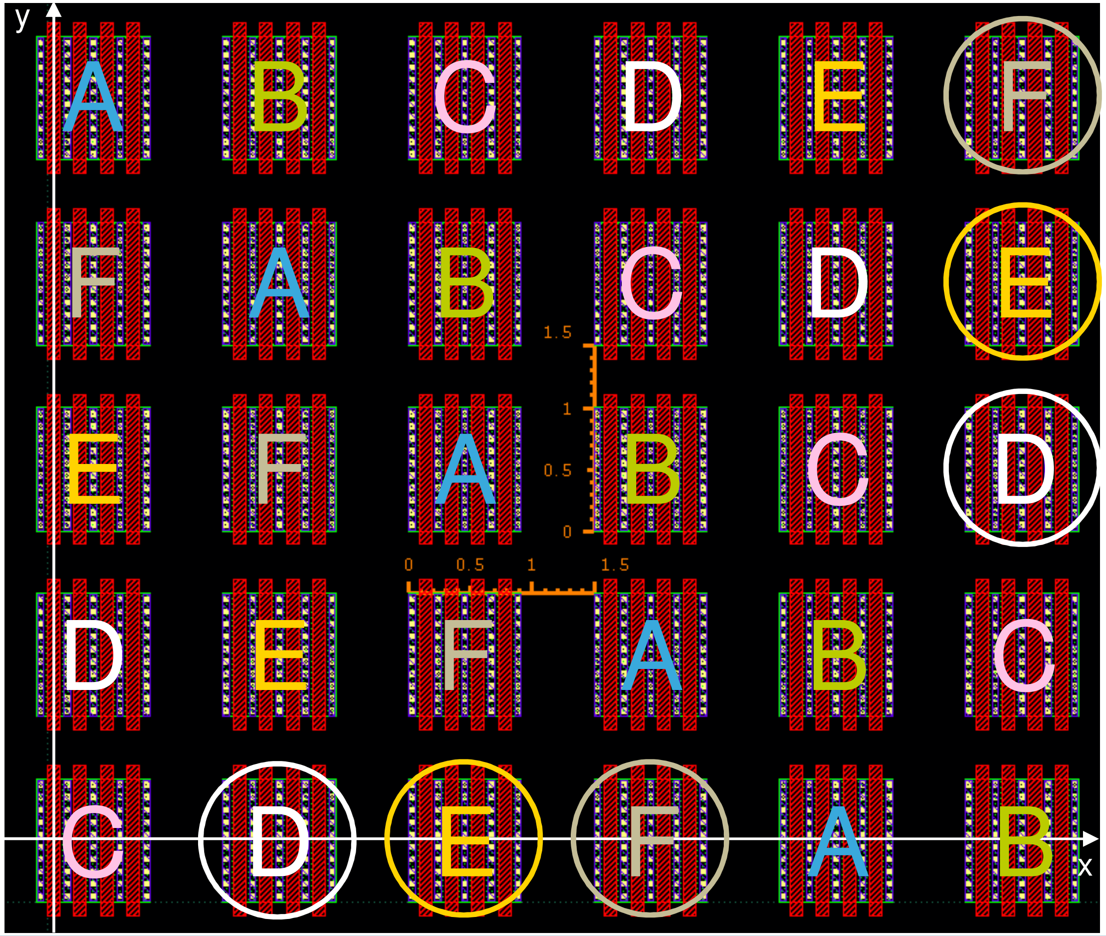
Ex. 4: Six MOS in interleaved 1D arrays
1 to several instances per MOS needed (1/2)



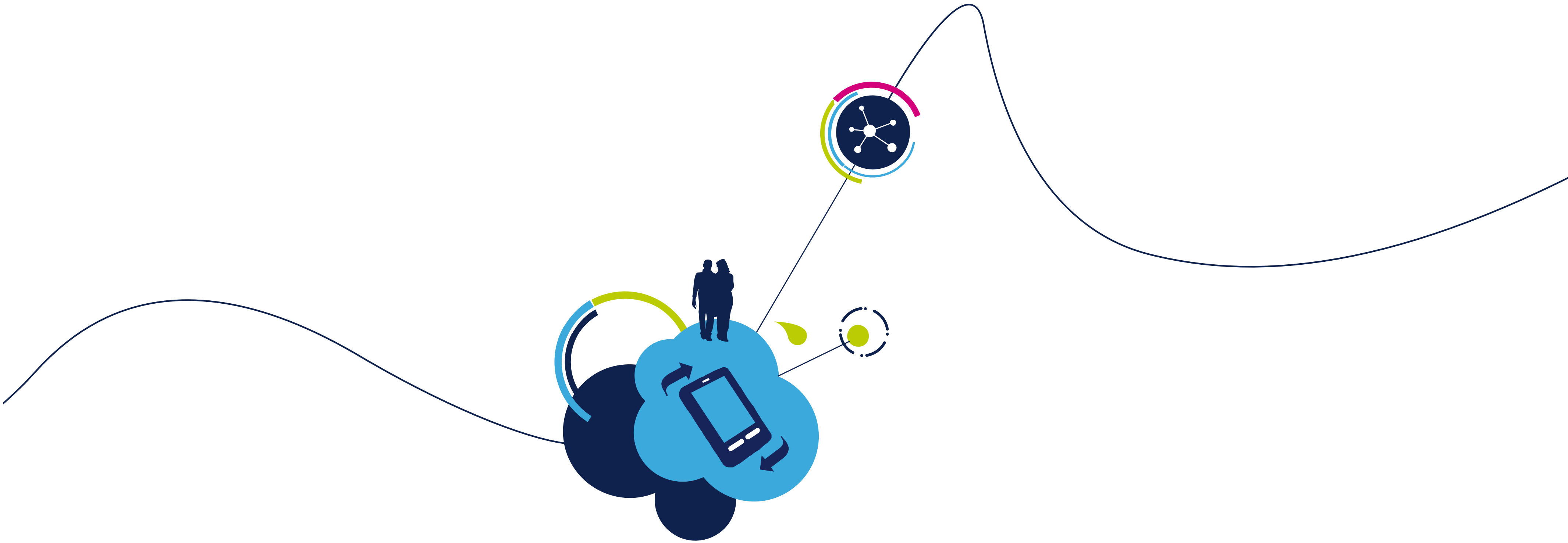
Device A: nf=4 xpos=6u ypos=0 mx=5 my=0 deltax=-1.5u deltay=1.5u
Device B: nf=4 xpos=7.5u ypos=0 mx=5 my=0 deltax=-1.5u deltay=1.5u
Device C1: nf=4 xpos=0 ypos=0
Device C2: nf=4 xpos=7.5u ypos=1.5u mx=4 my=0 deltax=-1.5u deltay=1.5u

… continued on next slide

Ex. 4: Six MOS in interleaved 1D arrays 1 to several instances per MOS needed (2/2)



Device D1:	nf=4	xpos=1.5u	ypos=0	mx=2	my=0	deltax=-1.5u	deltay=1.5u
Device D2:	nf=4	xpos=7.5u	ypos=3u	mx=3	my=0	deltax=-1.5u	deltay=1.5u
Device E1:	nf=4	xpos=3u	ypos=0	mx=3	my=0	deltax=-1.5u	deltay=1.5u
Device E2:	nf=4	xpos=7.5u	ypos=4.5u	mx=2	my=0	deltax=-1.5u	deltay=1.5u
Device F1:	nf=4	xpos=4.5u	ypos=0	mx=4	my=0	deltax=-1.5u	deltay=1.5u
Device F2:	nf=4	xpos=7.5u	ypos=6u				



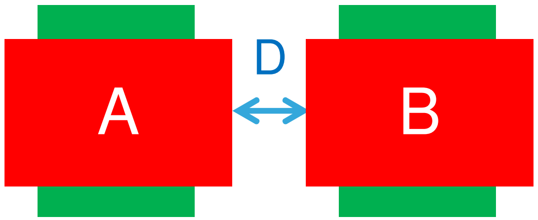
About sensitivity analysis

Introduction to sensitivity analysis

- Designers may want to perform a sensitivity analysis during Monte-Carlo matching simulations to identify main contributors among involved devices, and their associated input matching parameters

- Since the mismatch model is accounting for the distance between devices, sensitivity analysis results change when this distance varies

- To illustrate this point, consider two transistors A and B, spaced by a distance, D:



- Let DVT_AB be the difference between transistors' Vth, which will be used as an indicator of how transistors A and B are matched

Interpreting sensitivity analysis results 1/2

- In the mismatch model, the effect of distance is accounted for thanks to a large number of global (or LOT) statistical variables, GPOS*
- As a result, these global variables may appear in the sensitivity analysis results, with a cumulated level of contribution which depends on the relative position of transistors A and B
- Case 1: When distance D is large, position dependent contribution to mismatch is large, thus GPOS* cumulated contribution is significant:
  - 63.9% of mismatch is due to position dependent contribution (GPOS* variables)
  - 34.1% of mismatch is due to other sources of local variations

List of Important Variables :

Index(I) Value		%Pass	Histo S(I)	percent	/ cumulative	/ CI bootstrap [lower	upper]	Variable Name
159	[ ]	100.0%	|--------------------	16.3%	16.3%	15.3%	18.0%	PEM(LVTNFET_ACC.DVFBO_MCDEV,XA.M1)
153	[ ]	100.0%	|-------------------	15.9%	32.2%	14.7%	17.6%	PEM(LVTNFET_ACC.DVFBO_MCDEV,XB.M1)
160	[ ]	98.2%	|	1.0%	33.3%	0.7%	1.5%	PEM(LVTNFET_ACC.DUO_MCDEV,XA.M1)
154	[ ]	92.6%	|-	0.9%	34.1%	0.6%	1.4%	PEM(LVTNFET_ACC.DUO_MCDEV,XB.M1)
74	[+]	0.1%	|	0.1%	34.3%	0.1%	0.4%	P(GPOSX1_15)
62	[+]	0.1%	|	0.1%	34.3%	0.0%	0.4%	P(GPOSC1_13)
68	[+]	0.1%	|	0.1%	34.4%	0.1%	0.4%	P(GPOSS1_14)
17	[+]	0.1%		0.1%	34.4%	0.0%	0.4%	P(GPOSC1_4)

Other sources

GPOS* (not all shown)

Interpreting sensitivity analysis results 2/2

- Case 2: When distance D is small, position dependent contribution to mismatch is weak, thus GPOS* cumulated contribution is negligible:
  - Nearly 100% of mismatch is due to other sources of local variations

List of Important Variables :

Index(I) Value		%Pass	Histo S(I)	percent /	cumulative /	CI bootstrap [lower	upper]	Variable Name
153	[ ]	100.0%	|--------------------	48.7%	48.7%	47.2%	50.7%	PEM(LVTNFET_ACC.DVFB0_MCDEV,XB.M1)
159	[ ]	100.0%	|-------------------	46.8%	95.4%	45.3%	48.4%	PEM(LVTNFET_ACC.DVFB0_MCDEV,XA.M1)
160	[ ]	100.0%	|	2.4%	97.9%	2.0%	3.2%	PEM(LVTNFET_ACC.DUO_MCDEV,XA.M1)
154	[ ]	100.0%	|	2.2%	100.0%	1.8%	3.0%	PEM(LVTNFET_ACC.DUO_MCDEV,XB.M1)
51	[ ]	0.7%	|	0.2%	100.3%	0.1%	0.6%	P(GPOSP1_11)
46	[+]	0.1%	|	0.1%	100.4%	0.1%	0.5%	P(GPOSP1_10)
138	[+]	0.1%	|	0.1%	100.5%	0.0%	0.4%	P(GPOSS2_13)
124	[+]	0.1%	|	0.1%	100.5%	0.1%	0.4%	P(GPOSX2_10)

Other sources

GPOS*
(not all shown)

  - Here, mismatch of transistors A and B will be reduced compared to Case 1, thanks to a significant correlation level between the transistors

- Notes:
  - In some simulators, GPOS* contributions may be aggregated under a single one named "Process", due to the fact that these variables are global, like variables used to describe process variations
  - Sensitivity analysis results may be inaccurate, especially when dealing with complex circuits

Simulation settings within ArtistKit

Settings for Monte-Carlo simulations

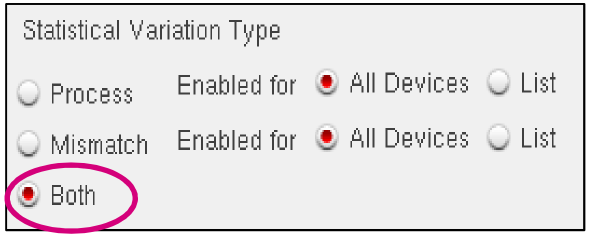
- SPICE implementation of new matching model relies on both local and global statistical variables
  - Global statistical variables are mandatory to capture correlation effects

- As a result, matching simulations now require that both Process-like (global) and matching-like (local) statistical variations are enabled

Spectre

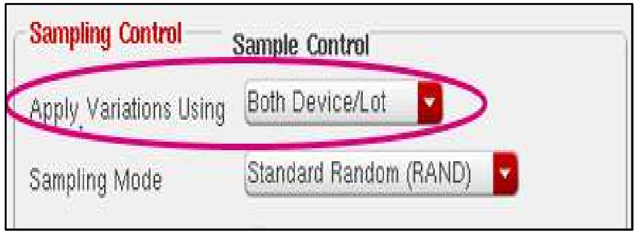
ADE-XL→ Monte-Carlo sampling

GoldenGate



ADE-L→ Choosing Analyses Form→ DC or AC or others→ Task→ Enable task→ Monte Carlo

Eldo



ADE-L→ Choosing Analyses → mc

- **<u>The choice “process and/or mismatch” is now only managed by Artiskit setup corners menu</u>**

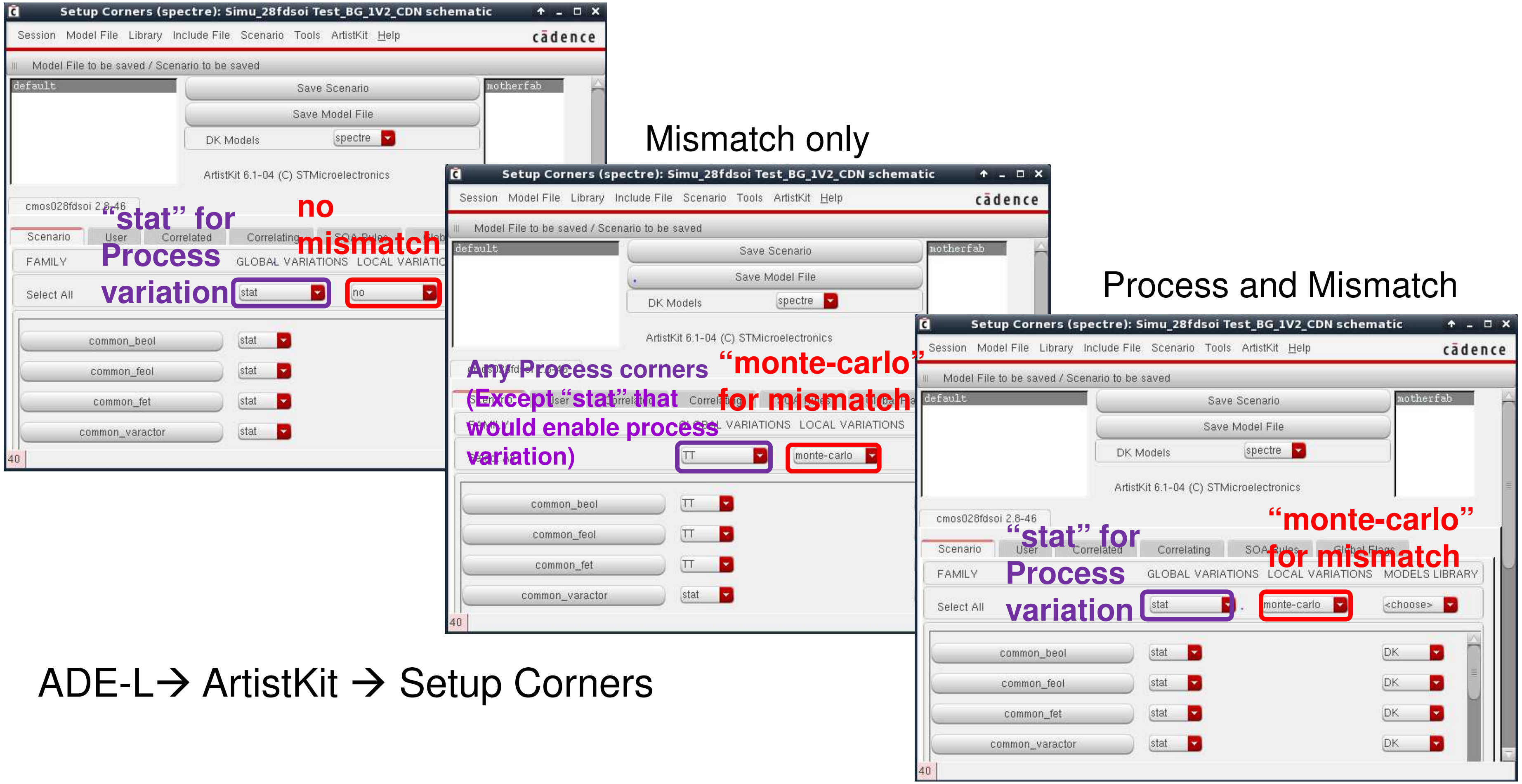
- **<u>=> ALWAYS LET “ALL/BOTH” STATISTICAL VARIATION SELECTION</u>**

Variability selection from ADE-L/ArtistKit for Monte-Carlo simulation

Process only

Mismatch only

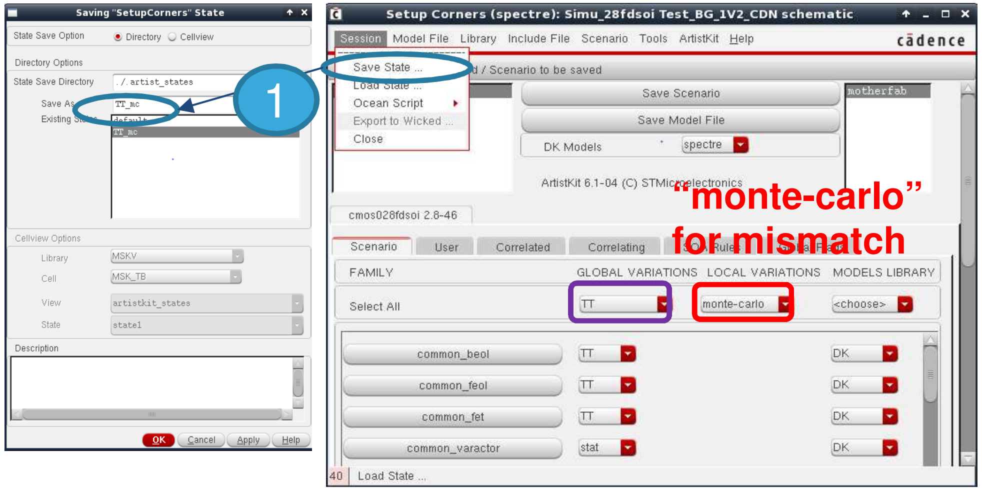
Process and Mismatch



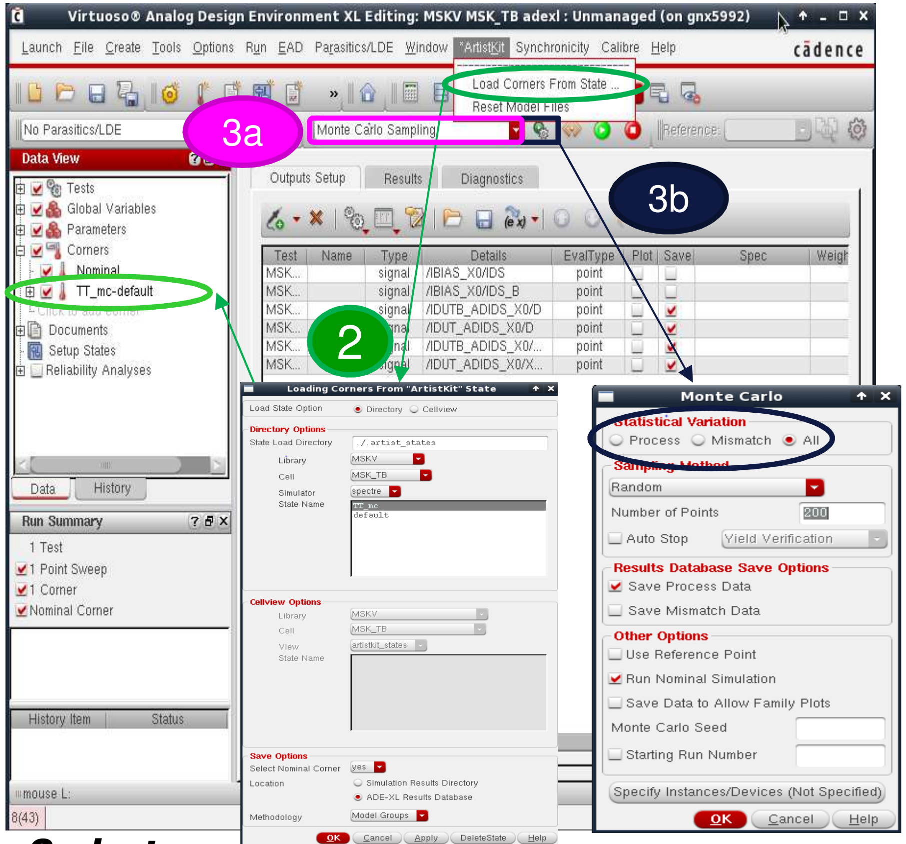
ADE-L→ ArtistKit → Setup Corners

Monte-carlo with ADE-XL : Mismatch only (spectre) in 3 steps

1st step: create & save the corners state
ADE-L→ArtistKit→ Set up corners menu



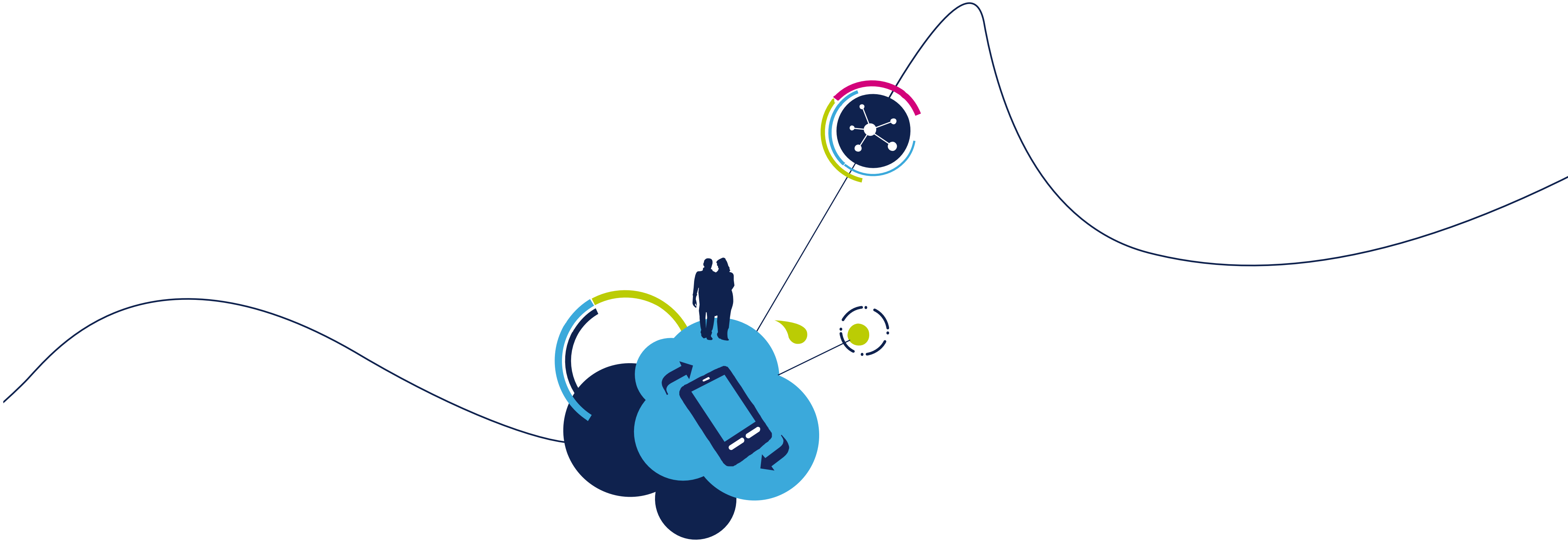
2nd step: load the corners state
ADE-XL→ArtistKit→Load Corners from state



3rd step:

- 3a: choose “Monte carlo sampling”
- 3b: Set “All” to statistical variation in the monte-carlo window

*Note: FDSOI models require **both** Process-like (global) and matching-like (local) statistical mechanism/engine to be enable*



Thank you!