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C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG

User manual

1.8 V IO compensation cell designed in 28 nm FDSOI technology

Overview

The C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG library contains a compensation cell designed in 28 nm FDSOI technology. The cell generates an 8-bit compensation code, which represents PVT variations as seen on the chip. These codes can be used by output buffers and other circuits for active correction of any PVT dependent circuit parameters.

Note: The compensation cell is mandatory for 1.8 V IOs to work if active slew rate compensated buffers are used.

Features

- Clocked architecture for low power consumption
- Fixed code, when core power supply is down
- Accurate mode for high performance using external resistor
- Support for on-chip resistor in Non-accurate mode
- Capability to freeze codes
- Low power and medium oxide process option
- Uses LVT# devices in GO1
- Metallization options supported as per product package
- Contains IO ring compensation cell and core macro compensation cell
- Core macro cell uses four metal levels
- Allows over the cell routing with metal5 and above, in the macro cell
- Wake-up time of 10 µs
- Built in Power on Reset (POR)
- Antenna diode protection for core side input pins
- Programmable control to switch-off internal reference currents for IDDQ testing
- Supports single row configuration(a)
- No power sequence required for core and IO supplies(b)

Product name contains LR due to legacy reasons although LVT devices are used.

a. Single row configuration is also called linear configuration.

b. Refer to *Section 2.4: Core-off and IO-off functionality* for details.

Information snapshot

- Process options
  - GO1: 16 Å
  - GO2: 28 Å
- Packaging
  - Flip-chip

Table 1. Operating conditions

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
$T_{Junction}$	Operating junction temperature	-40	25	125	°C
vdde1v8	Pad supply voltage	1.65	1.8	1.95	V
vdd	Core supply voltage	0.6	1.0	1.15	V

1 Quick references

Note: The document uses the following convention to indicate logic levels:

- L indicates logic low.

- H indicates logic high.

- X indicates don't care state.

- Z indicates high impedance state.

- '-' (Hyphen) indicates 'No activity'.

Note: The suffix '' in the library name indicates multiple metallization options.*

1.1 Metal stacking convention

The metallization options supported by the library can be inferred from its product package:

- 7 metal option (5U1X2T8XLB) signifies:
  - 5U1X refers to the first 5 levels with 1X pitch (thin metals).
  - 2T8X refers to 2 levels with 8X (thick metals) in oxide.
  - LB is the Alucap.
- 8 metal option (6U1X2T8XLB) signifies:
  - 6U1X refers to the first 6 levels with 1X pitch (thin metals) in ultra low K.
  - 2T8X refers to 2 levels with 8X (thick metals) in oxide.
  - LB is the Alucap.
- 10 metal option (6U1X2U2X2T8XLB) signifies:
  - 6U1X refers to the first 6 levels with 1X pitch (thin metals) in ultra low K.
  - 2U2X refers to the next 2 levels with 2X pitch (thin metals) in ultra low K.
  - 2T8X refers to 2 levels with 8X (thick metals) in oxide.
  - LB is the Alucap.

1.2 Reference documentation

The following documents can be used for further study:

- User manuals of the following libraries:
  - C28SOI_IO_EXT_CSF_BASIC_EG*
  - C28SOI_IO_EXT_ALLF_CORESUPPLY_EG*
  - C28SOI_IO_ALLF_IOSUPPLYKIT_EG*
  - C28SOI_IO_ALLF_FRAMEKIT_EG*
  - C28SOI_IO_ALLF_CDMKIT_EG*

For details in the following topics:

- Power Sequencing Recommendation in IOs
- Specifications and Analysis of Overshoots and Undershoots
- SSN Application Notes
- ESD qualification

- Latch-up qualification
- Maturity information

ST users, refer to the IO Reference catalog. (http://ccds.st.com/cps/sections/library/io/io_reference_catalog/downloadFile/file/IO_Helpdesk_Solutions.pdf).

Non-ST users, contact Customer Support personnel.

2 Functional specifications

Table 2. Cell list

Cell name	Width (µm)	Height (µm)	Description
IO ring compensation cell(1)			
COMPENSATION_EXT_CSF_1V8_FC_LIN	460	90.8	IO cell
Core macro compensation cell			
COMPENSATION_EXT_1V8	340	90.8	Macro cell

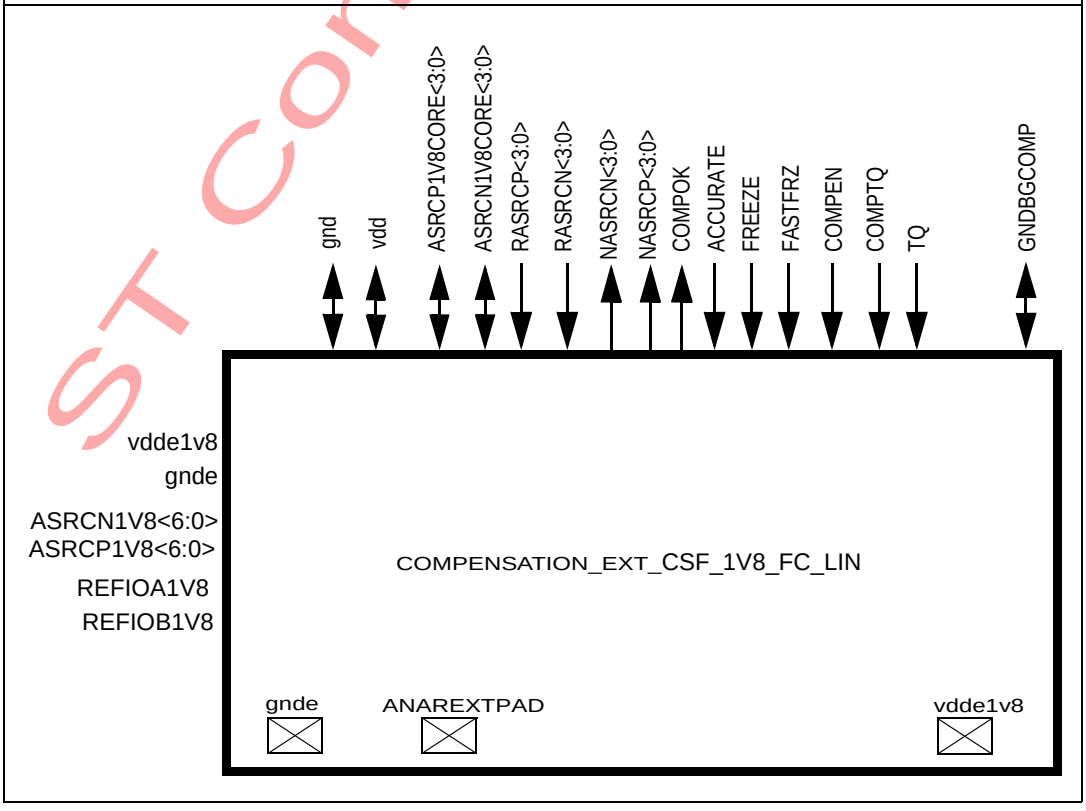
1. This cell is supported in single row configuration.

Caution: The ALLCELLS are not considered part of the deliverable. These cells are specifically for QA check and hence subject to change, without prior notice.

2.1 COMPENSATION_EXT_CSF_1V8_FC_LIN

2.1.1 Functional diagram

Figure 1. Block diagram of COMPENSATION_EXT_CSF_1V8_FC_LIN



1. It is recommended to use dedicated ground supply cell for GNDBGCOMP.

2.1.2 Pin description

Table 3. Logic pins(1)

Pin	Type	Voltage level	Description
FREEZE	Input	vdd	– When high, it freezes the compensation code at its running value. Freeze mode is activated on the signal rising edge. – Compensation cell delivers refreshed compensation code at a delay after signal falling edge. Refer *Table 17: Switching delay characteristics to normal mode* for the values of delay.
FASTFRZ	Input	vdd	– When high, it fast-freezes the compensation code at its running value. Fast Freeze mode is activated on signal rising edge. – Compensation cell delivers a refreshed compensation code, at a comparatively lesser delay after signal falling edge, than the delay of the FREEZE signal.
TQ	Input	vdd	When high, it puts all IOs and reference generators in IDDQ mode.
COMPEN	Input	vdd	Control the operating modes of the compensation cell.
COMPTQ	Input	vdd	
COMPOK	Output	vdd	– Can be high in the Normal mode and when a new measured code is available on the ASRC lines. – When the compensation cell changes from any other mode to Normal mode, delay constraints are applied to COMPOK signal.
ACCURATE (2)	Input	vdd	– When high, it sets the compensation cell to work with an external resistor for reference current generation to provide an accurate compensation code. – When low, it uses an internal resistor for compensation cell current reference.
ASRCN1V8CORE<3:0> (3)	Input/Output	vdde1v8	– Compensation code for NMOS. – Bits <3:0> used for standard NMOS compensation. – This pin is available at the core.
ASRCP1V8CORE<3:0> (3)	Input/Output	vdde1v8	– Compensation code for PMOS. – Bits <3:0> used for standard PMOS compensation. – This pin is available at the core.
NASRCN<3:0>	Output	vdd	Bits <3:0> are used for standard NMOS compensation with 1.0 V.

Table 3. Logic pins(1) (continued)

Pin	Type	Voltage level	Description
NASRCP<3:0>	Output	vdd	Bits <3:0> are used for standard PMOS compensation with 1.0 V.
RASRCN<3:0> (4)	Input	vdd	4-bit NMOS compensation codes from core.
RASRCP<3:0>(4)	Input	vdd	4-bit PMOS compensation codes from core.
ANAREXTPAD(5) (6)	Input/Output	vdde1v8	The external resistance of 10 kΩ that is connected to GNDBGCOMP in Accurate mode.

1. Logic pins are digital. Hence, ensure that all the input pins are either tied to ground or to their respective supply levels, depending upon the mode of operation of the IO cell. Floating input pins are not allowed.
2. If Accurate mode (refer *Section : Operating modes*) is intended for use, then ANAREXTPAD is directly connected through a 10 k Ω (+/-1%) external or internal resistor to ground potential.
3. ASRCN1V8CORE<3:0> and ASRCP1V8CORE<3:0> are the core pins and are available at core side. However, logically they are identical to ASRCN1V8<3:0> and ASRCP1V8<3:0> pins.
4. RASRCN<3:0> and RASRCP<3:0> pins must not be left floating. They can be used for enhanced testability, if no other use is intended. They should be connected either to ground or vdd if they are not used.
5. The maximum permissible value of all the capacitances (inclusive of pad capacitance, on-board routing capacitance, and external capacitance) seen at ANAREXTPAD node should not be more than 10 pF.
6. In Non-accurate mode, this pin can be left floating.

Table 4. Track pins

Pin	Type	Voltage level	Description
ASRCN1V8<3:0>(1)	Input/Output	vdde1v8	Bits <3:0> are used for standard NMOS compensation.
ASRCP1V8<3:0>(1)	Input/Output	vdde1v8	Bits <3:0> are used for standard PMOS compensation.
GNDBGCOMP	Input/Output	gnd	Dedicated ground for the reference cells. It should be connected to dedicated supply pad.
vdd	Input/Output	vdd	Core supply pin.
gnd	Input/Output	Ground	Ground.
gnde	Input/Output	Ground	Ground.
vdde1v8	Input/Output	vdde1v8	vdde supply pin.

1. ASRCN1V8<3:0> and ASRCP1V8<3:0> are rail pins and are available at the ring side.

Table 5. Unused track pins(1)

Pin	Type	Voltage level	Description
ASRCP1V8<6:4>	Input/Output	0/vdde1v8	Compensation bit track pins.
ASRCN1V8<6:4>	Input/Output	0/vdde1v8	
REFIOA1V8	Input/Output	0/vdde1v8	Reference signal track pin.
REFIOB1V8	Input/Output	0/vdde1v8	

1. These pins can be left unconnected, as they are unused pins.

2.1.3 Functional description

This compensation cell is located in the IO ring and provides the following:

- Compensation code at 1.8 V to be used in the IO ring (ASRCN1V8<3:0> and ASRCP1V8<3:0>) and compensation code at 1.8 V to be used in the core (ASRCN1V8CORE<3:0> and ASRCP1V8CORE<3:0>).
- Compensation code at vdd level (NASRCN<3:0> and NASRCP<3:0>).
- Compensation code status signal at vdd level (COMPOK).

For IO ring, the following components are integrated inside the compensation cell:

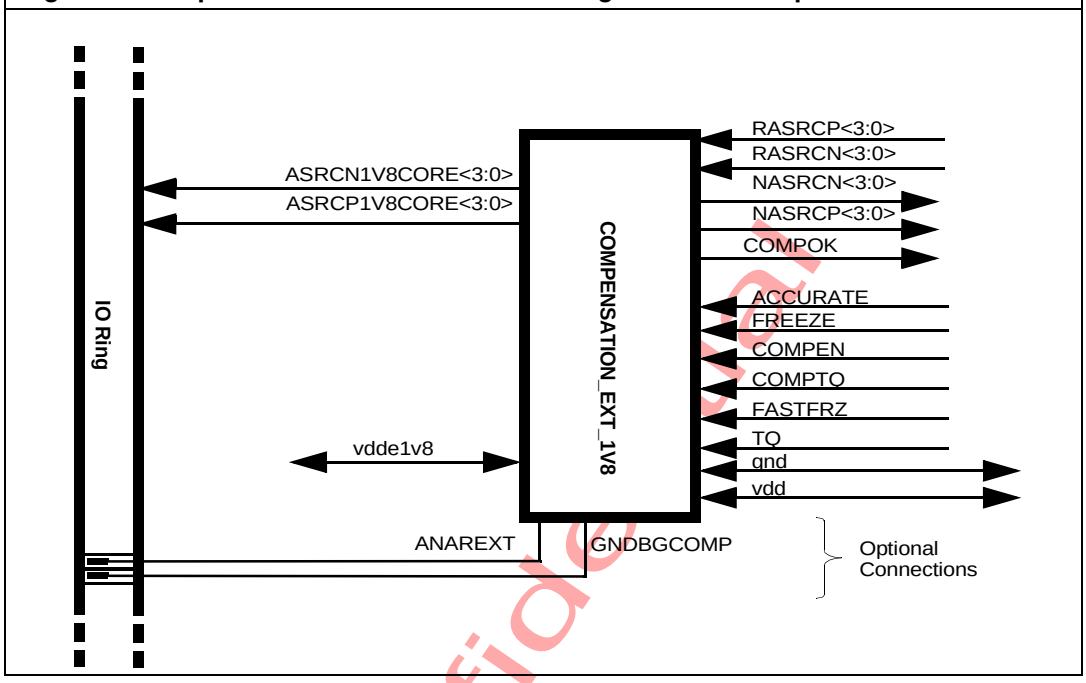
- Two supply cells providing supply (vdde1v8/gnde) to the IO ring and ESD protection clamp on both sides of the compensation cell.
- One ANAPAD (for pin ANAREXTPAD), which is used to connect the external resistor in the Accurate mode of compensation.

2.2 COMPENSATION_EXT_1V8

This contains core macro compensation cell.

2.2.1 Functional diagram

Figure 2. Compensation connections to IO ring and core compensation cell in core



2.2.2 Pin description

Table 6. Pin description

Pin	Type	Voltage level	Description
Logic pins(1)			
FREEZE	Input	vdd	– When high, it freezes the compensation code at its running value. Freeze mode is activated on signal rising edge. – Compensation cell delivers refreshed compensation code, at a delay after signal falling edge. Refer *Table 17: Switching delay characteristics to normal mode* for the values of delay.
FASTFRZ	Input	vdd	– When high, it fast-freezes the compensation code at its running value. Fast Freeze mode is activated on signal rising edge. – Compensation cell delivers refreshed compensation code, at a comparatively lesser delay after signal falling edge than the delay of the FREEZE signal.
TQ	Input	vdd	When high, it puts all IOs and reference generators in IDDQ mode.
COMPEN	Input	vdd	Control the operating modes of the compensation cell.
COMPTQ	Input	vdd	

Table 6. Pin description (continued)

Pin	Type	Voltage level	Description
COMPOK	Output	vdd	– Can be high in the Normal mode and when a new measured code is available on the ASRC lines. – When the compensation cell changes from any other mode to Normal mode, delay constraints are applied to COMPOK signal.
ACCURATE (2)	Input	vdd	– When high, it sets the compensation cell to work with an external resistor for reference current generation, to provide an accurate compensation code. – When low, it uses internal resistor for compensation cell current reference.
ASRCN1V8CORE <3:0> (3)	Input/Output	vdde1v8	– Compensation code for NMOS. – Bits <3:0> used for standard NMOS compensation. – This pin is available at the core.
ASRCP1V8CORE <3:0> (3)	Input/Output	vdde1v8	– Compensation code for PMOS. – Bits <3:0> used for standard PMOS compensation. – This pin is available at the core.
NASRCN<3:0>	Output	vdd	Bits <3:0> are used for standard NMOS compensation with 1.0 V.
NASRCP<3:0>	Output	vdd	Bits <3:0> are used for standard PMOS compensation with 1.0 V.
RASRCN<3:0>(4)	Input	vdd	4-bit NMOS compensation codes from core.
RASRCP<3:0> (4)	Input	vdd	4-bit PMOS compensation codes from core.
ANAREXT (5) (6) (7)	Input/Output	vdde1v8	It must be connected to an ANA pad, further connected through a resistor to ground potential (dedicated ground).

1. Logic pins are digital. Hence, ensure that all the input pins are either tied to ground or to their respective supply levels, depending upon the mode of operation of the IO cell. Floating input pins are not allowed.
2. If Accurate mode (refer *Section : Operating modes*) is to be used, then ANAREXT must be connected to an ANA pad, which is further connected through a 10 kΩ (+/-1%) resistor to ground potential.
3. ASRCN1V8CORE<3:0> and ASRCP1V8CORE<3:03:0> are the core pins and are available at core side.
4. RASRCN<3:0> and RASRCP<3:0> pins must not be left floating. They can be used for enhanced testability, if no other use is intended. They should be connected either to ground or vdd, if they are not used.
5. The maximum permissible value of all capacitances (inclusive of pad capacitance, on-board routing capacitance, and external capacitance) seen at ANA pad should not be more than 10 pF.
6. In Non-accurate mode, this pin can be left floating.
7. It is recommended that parasitic resistance between ANAREXT and the ANA pad be kept less than 10 Ω.

Table 7. Track pins

Pin	Type	Voltage level	Description
GNDBGCOMP	Input/Output	gnd	Dedicated ground for the reference cells. It should be connected to dedicated supply pad.
vdd	Input/Output	vdd	Core supply pin.
gnd	Input/Output	Ground	Ground.
vdde1v8	Input/Output	vdde1v8	vdde supply pin.

2.2.3 Functional description

This compensation cell is located in the core and must be connected to IO rails through the filler cell FILLCELL_REFASRC_EXT_CSF_FC_LIN, which is taken from the C28SOI_IO_EXT_CSF_BASIC_EG* library. This core cell provides the following:

- Compensation code at 1V8 (ASRCN1V8CORE<3:0> and ASRCP1V8CORE<3:0>).
- Compensation code at 1V0 (NASRCN<3:0> and NASRCP<3:0>).
- Compensation code status signal (COMPOK) at vdd level.

Logic behavior

The ACCURATE pin is used to select Accurate and Standard[c] modes.

Table 8. Accurate mode programming

Accurate mode	Programming mode
L	Standard mode (uses internal resistor)
H	Accurate mode (uses external resistor)

Table 9. Functional behavior

Operating modes	Input					Output
	TQ	COMPEN	COMPTQ	FREEZE	FASTFRZ	COMPOK
Normal mode	L	L	L	L	L	H
Freeze mode	L	L	L	↑ (1)	L	L
Fast Freeze mode	L	L	L	L	↑ (1)	L
Read mode	L	H	H	L	L	L
High Impedance mode	L	H	L	L	L	L

c. Standard mode was referred to as Non-accurate mode.

Table 9. Functional behavior

Operating modes	Input					Output
	TQ	COMPEN	COMPTQ	FREEZE	FASTFRZ	COMPOK
Fixed Code mode	L	L	H	L	L	L
IDDQ mode	H	-	-	L	L	L

1. ↑ indicates that compensation starts freezing the 4-bit codes on the rising edge.

2.3 Operating modes

Table 10. Status of digital code bus in different operating modes

Operating mode	Input	Output		Description
	RASRCP<3:0> and RASRCN<3:0>	**ASRCP1V8<3:0> and ASRCN1V <3:0>**	**NASRCP <3:0> and NASRCN <3:0>**	
Normal	-	f (PVT)	f(PVT)	4-bit code is internally generated for PMOS and NMOS separately, based on the PVT conditions on a chip.
Freeze	-	f (PVT) @ t_0		– 4-bit code is internally generated for PMOS and NMOS separately, based on the PVT conditions on a chip. – They are latched when FREEZE enters logic high from logic low at time = t_0.
Fast Freeze	-	f (PVT) @ t_0		– 4-bit code is internally generated for PMOS and NMOS separately, based on the PVT conditions on a chip. – They are latched when FASTFRZ enters logic high from logic low at time = t_0.
Read	RASRCP<3:0> and RASRCN<3:0>			Digital code is read from RASRCP<3:0> and RASRCN<3:0> buses and is transferred to the respective outputs with appropriate level shifting.
High Impedance	-	Z	X	– ASRCP1V8<3:0> and ASRCN1V8<3:0> buses are in high impedance state.(1) – NASRCP<3:0> and NASRCN<3:0> buses are in Indeterminate state.(1)
Fixed code	-	ASRCP1V8<3:0> - HLHL ASRCN1V8<3:0> - LHLH	NASRCP<3:0> - HLHL NASRCN<3:0> - LHLH	Fixed code is output on the ASRC bus.
IDDQ	-	ASRCP1V8<3:0> - HLHL ASRCN1V8<3:0> - LHLH	NASRCP<3:0> - HLHL NASRCN<3:0> - LHLH	

1. ASRCP1V8<3:0> and ASRCN1V8<3:0> floating buses can lead to internal power consumption from vdd supply, unless externally driven to a valid logic state.

Compensation cell behavior for different vdd supply operating conditions

Table 11. Behavior in different vdd supply operating conditions

Core vdd(1)	IO vdd(2)	Description
0.7 V - 1.15 V	0.7 V - 1.15 V	Compensation works in Normal mode, codes generated are f (PVT).
0	0	Compensation cell enters into Freeze mode. Refer *Section 2.4: Core-off and IO-off functionality* for details.

1. vdd supply used in the core.
2. vdd supply used in the IO ring.

Note: Both the compensation cells COMPENSATION_EXT_CSF_1V8_FC_LIN and COMPENSATION_EXT_1V8 should be driven by the vdd supply used in the IO ring.

Programming for Accurate or Standard mode

The compensation cell can be programmed to operate in Accurate or Standard mode by setting a valid logic level on the ACCURATE input pin (refer *Table 9: Functional behavior*).

Accurate mode

In this mode, the macro cell uses an off-chip resistor for reference current generation. The value of this resistance is subject to variations in process and temperature within +/-1%. As a result, the compensation cell generates accurate reference current and digital codes. This mode is recommended to be used for high performance applications. It requires more chip area, especially in pad-limited designs, as it needs an external resistor to be connected to the ANAREXT pin, through an additional analog and ground pad.

Standard mode

In this mode, the macro cell uses an on-chip resistor, which is included inside the macro cell, for reference current generation. The value of this resistance is subject to variations in process and temperature, usually within +/-20% that causes minor inaccuracy in generation of digital codes. This mode should be used when slew and impedance correction is not critical, as it saves off-chip area and most of an external component.

Operating modes

Once programmed, the compensation cell can function in various modes of operation based on logic values on the input pins. For more information on operating modes, refer to *Table 9: Functional behavior*.

Normal mode

In this mode, the macro cell constantly tracks the PVT condition of the chip and generates an 8-bit digital code. This 8-bit code is referred to as f (PVT) and it represents the current PVT state. The 8-bit code is available on ASRCN1V8<0.3> and ASRCP1V8<3:0> buses at 1V8 level, and on NASRCN<3:0> and NASRCP<3:0> buses at 1V0 level. In Normal mode, the internal reference current generators are active and power consumption is higher than that in all the other modes.

Freeze mode

The macro cell enters this mode on the rising edge (logic low-to-high transition) of the FREEZE pin. In this mode, the 8-bit code is latched at the time of rising edge of FREEZE signal and is available on ASRCN1V8<0.3> and ASRCP1V8<3:0> buses at 1V8 level, and on NASRCN<3:0> and NASRCP<3:0> buses at 1V0 level.

Freeze mode is used where the current consumption is to be kept low. In this mode, all the internal blocks are switched off to reduce the static power consumption. Internal latches keep the code, which is calculated before the cell enters the Freeze mode.

The time taken to switch from Freeze to Normal mode is in the order of microseconds, as all the internal blocks should be switched on.

Caution: To ensure that valid 8-bit codes are latched properly, Freeze mode should be entered only from Normal mode, when the COMPOK status pin is at logic high.

Fast Freeze mode

The compensation cell enters this mode on the rising edge (logic low-to-high transition) of the FASTFRZ pin. The 8-bit code is available on ASRCN1V8<0.3> and ASRCP1V8<3:0> buses at 1V8 level, and on NASRCN<3:0> and NASRCP<3:0> buses at 1V0 level. This mode is used to freeze the digital compensation codes, when the data is transferred from the compensated IOs on a chip to an external device, during Burst mode. This ensures signal integrity and eliminates the jitter caused due to modification in the IO driver strength.

After the data transfer operation is complete, the compensation cell can be brought back to Normal mode by putting a logic low on the FASTFRZ pin. The bandgap, measurement block, and other internal blocks are kept ON in this mode to enable the user to switch back to Normal mode quickly. The time taken for switching the compensation from Fast Freeze mode to Normal mode is considerably smaller than the delay incurred in switching from Freeze mode to Normal mode. In this mode, the current consumption is comparable to consumption in the Normal mode.

Caution: To ensure that valid 8-bit codes are latched properly, Fast Freeze mode should be entered only from Normal mode when the COMPOK status pin is at logic high.

Read mode

In this mode, it is possible to force the digital codes from the chip core logic. The digital logic at RASRCP<3:0> and RASRCN<3:0> inputs is presented on the ASRCP1V8<3:0> and ASRCN1V8<3:0> respectively for vdde level logic and on NASRCP<3:0> and NASRCN<3:0> buses, respectively, at the specified voltage level vdd (Core Logic Level).The bandgap, measurement block, and comparator blocks are switched off to reduce static power consumption to minimum value.

High Impedance mode

In this mode, the ASRCN1V8<3:0> and ASRCP1V8<3:0> buses are tri-stated. High Impedance mode is used when two or more compensation cells are sharing the same ASRC1V8 buses and another macro takes over the 8-bit code in the IO ring. The bandgap, measurement, and comparator blocks are switched off to reduce static power consumption to a minimum.

Fixed Code mode

The digital code is forced to a fixed value on the buses, ASRCN1V8<3:0>, ASRCP1V8<3:0>, NASRCN<3:0>, and NASRCP<3:0> at the specified voltage levels. The fixed value, same as the digital code, is obtained at typical PVT conditions and represents

typical bit patterns (ASRCN1V8<3:0>/NASRCN<3:0> -- LHLH and ASRCP1V8<3:0>/NASRCP<3:0> -- HLHL). The bandgap, measurement, and other blocks are switched off to reduce static power consumption to a minimum.

IDDQ mode

The IDDQ mode shuts down all internal blocks consuming static currents. In this mode, there is no static current consumption in the macro cell, except leakage. This mode is used during IDDQ testing. The digital code is forced to a fixed value, which is equal to typical bit patterns (ASRCN1V8<3:0>/NASRCN<3:0> -- LHLH and ASRCP1V8<3:0>/NASRCP<3:0> -- HLHL) on the ASRCN1V8<3:0>, ASRCP1V8<3:0>, NASRCN<3:0>, and NASRCP<3:0> buses, at the specified voltage levels. The bandgap, measurement, and comparator blocks are switched off to reduce static power consumption to a minimum.

2.3.1 COMPOK status signal

The logic value on this output pin informs the user the status of the 8-bit code available on the ASRCN1V8<3:0>/ASRCP1V8<3:0> and NASRCN<3:0>/NASRCP<3:0> buses.

Table 12. COMPOK status in different modes

COMPOK	Mode	Description
H	Normal	Valid 8-bit code signals are available on ASRCN1V8<0.3> and ASRCP1V8<3:0> buses at 1V8 level, and on NASRCN<3:0> and NASRCP<3:0> buses at 1V0 level, and the compensation cell is tracking f(PVT).
L	Normal	Occurs when the compensation cell enters the Normal mode from another mode and is in the process of generating the 8-bit code representing f (PVT).
	Fast Freeze	8-bit code signals are available on ASRCN1V8<0.3> and ASRCP1V8<3:0> buses at 1V8 level, and on NASRCN<3:0> and NASRCP<3:0> buses at 1V0 level. These signals are not generated by f (PVT). This also signals that the compensation cell is in a mode other than the Normal mode.
	Freeze	
	Read	
	High impedance	
	Fixed code	
	IDDQ	

The COMPOK pin indicates that the compensation cell has started generating valid codes, which are PVT dependent and the cell is stabilized. It is recommended to latch 8-bit codes when the COMPOK pin reaches logic high.

2.4 Core-off and IO-off functionality

The compensation cell supports Core-off mode, therefore, vdde1v8 supply can be switched on before vdd supply. The compensation cell also supports the IO-off mode, where vdd supply can be switched on before vdde1v8 supply. The compensation cell can be in different states, depending on the state of the power supplies vdde1v8 and vdd.

Table 13. State of cell

Power supply state	Programming mode	Condition
Power-not-OK	1.8 V supply mode	vdde1v8 < 1.5 V

It should be noted that the COMPOK pin is at logic low during Power-not-OK and Core-off states. The status of cell output in the power supply states is shown in the following table.

Table 14. Cell status output in power supply states

Power supply state	COMPOK	ASRCP1V8 <3:0>	ASRCN1V8 <3:0>	NASRCP1V8 <3:0>	NASRCN1V8 <3:0>
Power-not-OK (1)	L	(1)			
Core-off	L	HLHL	LHLH	-	-
IO-off	L	-	-	LLLL	LLLL

1. When vdde1v8 supply is less than the voltage required by the digital logic function, the logic at ASRCN1V8<3:0>, ASRCP1V8<3:0>, NASRCN<3:0>, and NASRCP<3:0> buses do not track the PVT conditions and continue to reflect the codes generated during last valid power supply conditions.

Caution: IO-off and Core-off features are guaranteed only when the available supply is in operating range. During transition or during voltage-ramp up, fixed logic state at output pins may not be ensured.Some glitch might occur at the Pad during the transition phase of supplies, that is, vdd/vdde1v8.

3 Electrical specifications

3.1 ESD and latch-up characteristics

Table 15. Library ESD targets

Symbol	Parameter	Condition	Target	Unit
V_{ESD}	Electrostatic discharge voltage	Human Body Model (HBM)	2000	V
		Machine Model (MM)	100	
		Charge Device Model (CDM)	500	
$P_{latch-up}$	Over-voltage stress	Maximum operating junction temperature 125 °C	1.5 * vdde1v8	V
	Latch-up current(1)	Across temperature range	100	mA

1. Specifications mentioned in above table are valid for negative injection current only in case of Fail-safe/Tolerant IOs.

Caution: The level of CDM current seen at a given pre-charge voltage varies significantly with the chip size and package type. For instance, larger dies/packages generate higher CDM current.
However, this package size dependence has been considered during IO qualification, so that the above CDM commitment remains valid even for large die/package size (even for large die/package sizes of hundreds of mm^2).

3.2 Noise profile

White noise of amplitude 40 mV, in the frequency band of 1 Hz to 150 MHz, is used for noise analysis. Its effect is then observed on the cell for a period of 8 ms.

The above noise source applied on IO supply and +1/-1 bit (decimal) shift is observed on the code.

Table 16. Input pin capacitance(1)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
IO pin capacitance	C_{IN}	-	-	2	pF	-

1. IO pin capacitance is visible at ANAREXTPAD, in IO cell.

3.3 Dynamic characteristics

The various specifications that are covered under dynamic (AC) characteristics are described in this section.

Table 17. Switching delay characteristics to normal mode

Mode change	Switching delay	Unit
From IDDQ mode	15	µs
From Freeze mode	15	µs
From Fast Freeze mode	10	ns
From Read mode	15	µs
From High Impedance mode	15	µs
From Fixed Code mode	15	µs

Table 18. Switching delay characteristics from normal mode

Mode change	Switching delay	Unit
To IDDQ mode	10	ns
To Freeze mode	10	ns
To Fast Freeze mode	10	ns
To Read mode	10	ns
To High Impedance mode	10	ns
To Fixed Code mode	10	ns

4 Usage guidelines

4.1 IO ring development guidelines

This section provides guidelines for constructing an IO ring using the cells of this library.

4.1.1 Mandatory library and cell list

The C28SOI_IO_EXT_CSF_COMPENSATION1V8_LR_EG library supports the construction of an IO ring in various configurations and for various applications. The mandatory libraries required for developing the IO ring using the IO cells from this library are listed in the following table.

Table 19. Mandatory libraries and cells

Library name	Cell type	Cell name	Description
C28SOI_IO_ALLF_ FRAMEKIT_EG*	-	-	Contains leaf cells used by all other libraries, specially rail templates and bondpads
C28SOI_IO_EXT_CSF_ BASIC_EG*	Supply cell	VDDE_EXT_CSF_ FC_LIN	Contains ESD protection cells, supply cells, corner, and place and route cells (for 1.8 V cells)
	Supply cell	VDD_EXT_CSF_FC_ LIN	
	Ground cell	GNDE_EXT_CSF_ FC_LIN	
	Ground cell	GND_EXT_CSF_FC_ LIN	
	Supply cell	VDDE_EXT_CSF_ FC_INNER	
	Ground cell	GNDE_EXT_CSF_ FC_INNER	
	Supply cell	VDDE_EXT_CSF_ FC_OUTER	
	Ground cell	GNDE_EXT_CSF_ FC_OUTER	
	Supply and Ground cell	GND_VDD_EXT_ CSF_FC_2ROWS	
	Filler cell	FILLCELL_ REFASRC_EXT_ CSF_FC_LIN	
	Filler cell	FILLCELL_VDDE _GNDE_EXT_CSF _FC_LIN	
	Analog input cell	WIRECELL_EXT_CSF_ FC_LIN	Analog input IO pad for IO ring.

Table 19. Mandatory libraries and cells (continued)

Library name	Cell type	Cell name	Description
C28SOI_IO_ALLF_ IOSUPPLYKIT_EG*	-	-	Reference library for BASIC; contains ESD Clamps
C28SOI_IO_EXT_ALLF_ CORESUPPLY_EG*	Supply cell	GNDCORE_EXT_CSF_ FC_LIN	Contains core supply cells.
C28SOI_IO_ALLF_CDMKIT_ EG*	-	-	Provide all ESD CDM protection leaf cells, can be used in the cells as well as in SoC

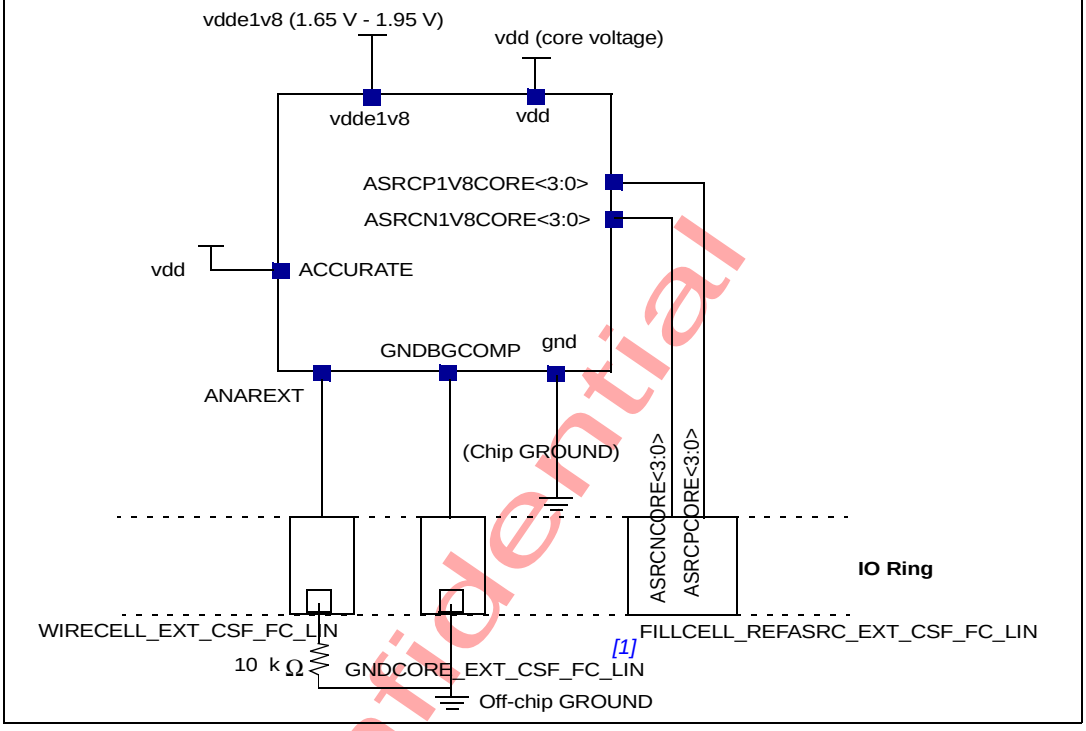
4.2 Design requirements

4.2.1 Using core compensation cell in Accurate mode

In Accurate mode, an external resistor must be connected to the ANAREXT pin, through the analog cell. The ANA cell, WIRECELL_EXT_CSF_FC_LIN, is used for connecting the external resistor to the ANA pad. The supply cell GNDCORE_EXT_CSF_FC_LIN cell is used as a dedicated ground supply (GNDBGCOMP).

The ASRCP1V8CORE<3:0> and ASRCN1V8CORE<3:0> bits of the compensation cell are connected to ASRCPCORE<3:0> and ASRCNCORE<3:0> of the filler cell, respectively.

Figure 3. Core compensation cell in Accurate mode



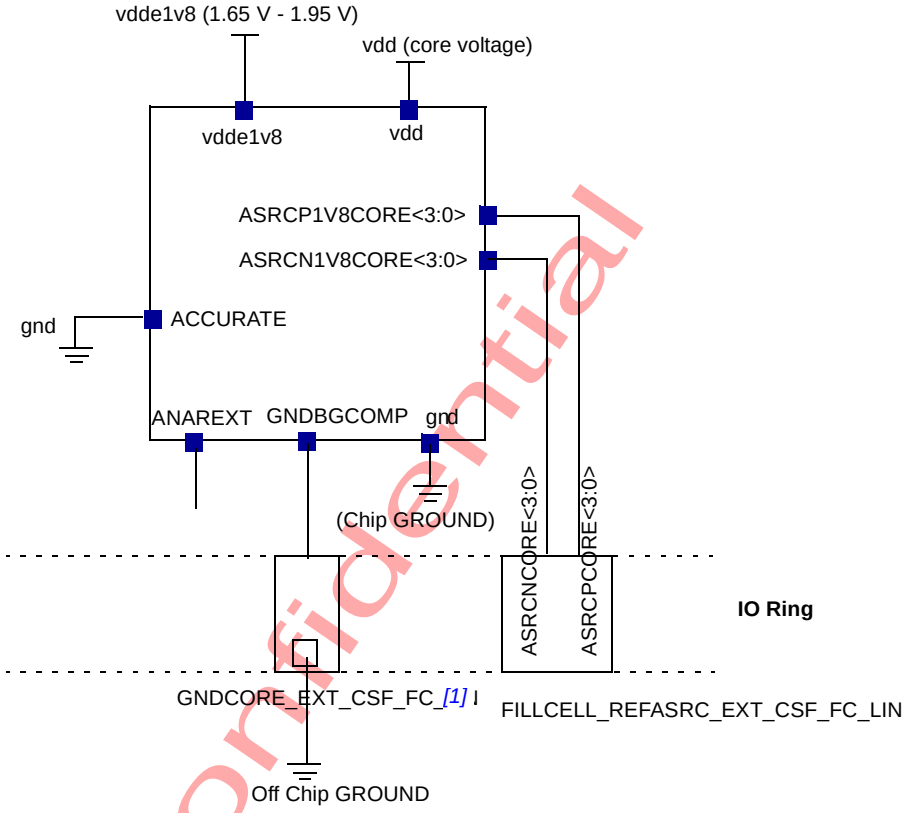
1. GNDCORE_EXT_CSF_FC_LIN cell is available in C28SOI_IO_ALLF_CORESUPPLY_EG* library. Instead of the coresupply cell, the GNDBGCOMP can also be connected to gnd rail.

4.2.2 Using core compensation cell in Standard mode

The supply cell, GNDCORE_EXT_CSF_FC_LIN, is used as a dedicated ground supply (GNDBGCOMP). Although, the ANAREXT pin can be connected to the chip GROUND via the ANA cell, WIRECELL_EXT_CSF_FC_LIN, it is recommended that the pin should remain disconnected.

The ASRCN1V8CORE<3:0> and ASRCP1V8CORE<3:0> bits of the compensation cell are connected to ASRCNCORE<3:0> and ASRCPCORE<3:0> of the filler cell, respectively.

Figure 4. Core compensation cell in Standard mode



1. GNDCORE_EXT_CSF_FC_LIN cell is available in C28SOI_IO_ALLF_CORESUPPLY_EG* library. Instead of the coresupply cell, the GNDBGCOMP should be connected to dedicated supply pad.
2. The ANAREXT pin should remain disconnected in the Standard mode.

4.2.3 Recommendations for using the compensation cell

Mode related

- The compensation cell should generally be used in Normal mode. The other modes of operation should be used to debug or when the chip is to be put in low power.
- Freeze mode should always be used in Normal mode and to latch the codes, FREEZE signal should go high only when COMPOK is high. There should be a delay of around 10 µs between COMPOK going high and transmission of FREEZE signal.
- High Impedance mode should be used only when another compensation cell is present to provide codes.
- The compensation cell should be used in Accurate mode to ensure high performance of the IO or high accuracy of the code.
- Accurate mode is applicable, when compensation cell is in Normal or Freeze mode.
- In Accurate mode, an ANA pad should be placed for external resistor and ground pad should be placed for GNDBGCOMP.
- Standard mode can be used for low performance when 2 bit/3 bit inaccuracy is acceptable.
- Never share same external resistor with two compensation cells. It can be used if one compensation cell is in Accurate mode while the other is in Standard mode.

Pins/Signals related

- GNDBGCOMP should be connected to dedicated ground in both Accurate and Standard modes.
- Codes are latched after the rising edge of FREEZE signal.
- Mutual coupling capacitance between ANAREXT node and other digital switching IO should not be more than 0.8 pF.
- If Accurate mode is intended for use, then ANAREXT must be connected to ANAPAD, which is further connected through a 10 kΩ (1%) resistor to ground potential. This ground potential must be provided to GNDBGCOMP through a separate core supply pad.
- The ANAREXT pin should be left unconnected if the compensation cell is in Standard mode. However, this pin can also be grounded in Standard mode.
- Pins, RASRCP<3:0> and RASRCN<3:0>, should never be left floating in any mode of operation.
- The input pins should be at some logic level, even if these are not used in a particular operating mode.

Capacitance/Resistance related

- The maximum permissible value of capacitance (inclusive of pad capacitance + on-board routing capacitance + external capacitance) seen at ANAREXT node, should not be more than 10 pF.
- It is recommended that parasitic resistance between ANAREXT node and the ANAPAD be kept as small as possible for core macro compensation cell.
- External resistor should have good accuracy (+/-1%).

Supply related

- vdde1v8 should always be supplied by the IO ring supply to take into consideration the variation in supply for code compensation.
- The supply level of the compensation cell should be same the vdde1v8 supply level of the IO ring on which the compensation cell provides codes.

4.3 IO placement guidelines

The following are the differences between compensation cell in IO ring (referred to as IO ring compensation cell) and compensation cell in core (referred to as core macro compensation cell).

- ANAREXTPAD, gnde, and vdde1v8 are included in the IO ring compensation cell whereas, the core macro compensation cell does not contain these pads.
- The core macro compensation cell has lesser width compared to IO ring compensation cell.
- ASRCP1V8<6:0> and ASRCN1V8<6:0> pins are available only in the IO ring compensation cell.
- Pins vdde1v8, vdd, gnd, GNDBGCOMP, ASRCP1V8<6:0>, and ASRCN1V8<6:0> are implicit pins.
- In the IO ring compensation cell, the external resistor of value 10 kΩ can be directly connected to the ANAREXTPAD (of the IO ring compensation cell), whereas in the core macro compensation cell, the resistor is connected to ANAPAD cell on the board, which in turn is connected to ANAREXT pin of the macro cell.

4.4 Layout compensation cell guidelines

The following are the recommended guidelines to layout the compensation cell in IO ring and core areas.

4.4.1 Compensation cell to be placed in IO ring

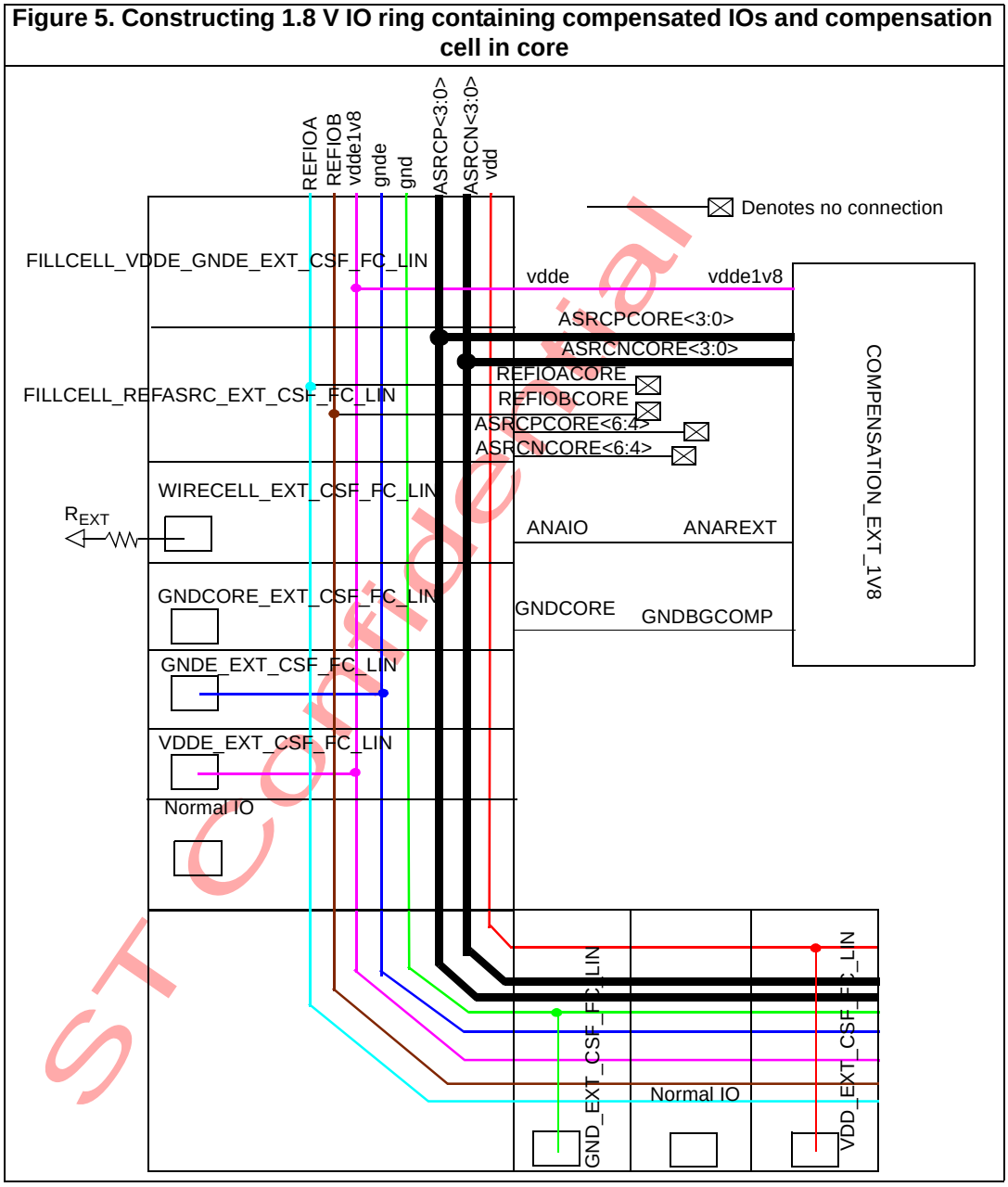
- The compensation cell, which is to be placed in IO ring contains inherited gnde, vdde1v8, and ANAREXTPAD pins. There is no need to manage the connection between compensation cell and ANAREXTPAD. Therefore, an on-board resistor of value 10 kΩ can directly be placed.
- The compensation cell can be flipped and placed in the ring.
- Any cell can be placed abutted to the compensation ring, as the supply cells are already integrated inside the compensation cell. GNDBGCOMP should be supplied with a dedicated ground. If this dedicated ground is used, then it is preferable to use it closer to the compensation cell.
- Since this IO compensation cell already integrates the ANAREXTPAD inside the cell, there is no constraint for the supply cells.
- Routing resistance of metal, connecting supply/ground to the compensation cell should not be more than 5 Ω.

4.4.2 Compensation cell to be placed in core

- The compensation cell, which is to be placed in the core, does not contain inherited gnde, vdde1v8, and ANAREXTPAD pins. Hence, there is a need to manage the connection between the compensation cell and ANAPAD used to connect resistor, of value 10 kΩ, to the ANAREXT pin of the cell and dedicated ground.
- It is recommended to put either supply cells or low frequency IO cells on both the sides of ANAPAD used for the resistor, only if compensation cell is put in core and ANAREXT pin is used to connect the resistor.
- Routing resistance of metal, connecting supply/ground to the compensation cell should not be more than 5 Ω.

4.5 Place and route requirements

Figure 5. Constructing 1.8 V IO ring containing compensated IOs and compensation cell in core



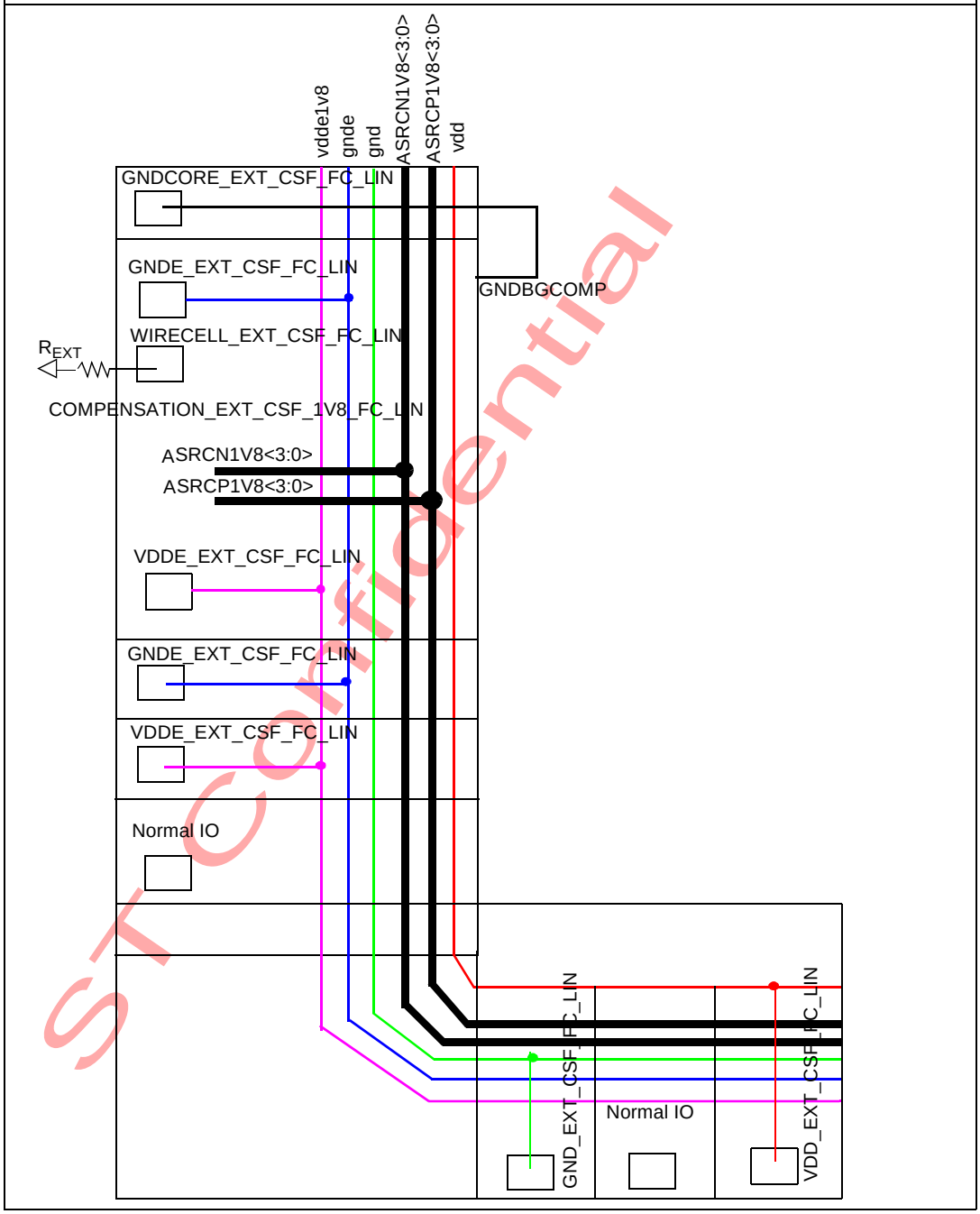
1. IO ring is for an IO operating at 1.8 V.
2. The signals apart from ASRCPCORE<3:0> and ASRCNCORE<3:0> can be left unconnected, applicable only for this compensation. However, if a different compensation macro is used, check for the respective User manual.

Table 20. Connectivity information of signals from compensation macro to IO ring

From		To	
Cell	**Pin**	**Cell**	**Pin**
COMPENSATION_EXT_1V8 (macro cell)	ANAREXT	ANAIO	WIRECELL_EXT_CSF_**
	vdde1v8	VDDE	FILLECELL_VDDE_GNDE_EXT_CSF_**
	GNDBGCOMP	GNDCORE	GNDCORE_EXT_CSF_**
	ASRCP1V8CORE<3:0>	ASRCPCORE<3:0>	FILLCELL_REFASRC_EXT_CSF_**
	ASRCN1V8CORE<3:0>	ASRCNCORE<3:0>	
Not Applicable	Can be left unconnected (1)	ASRCPCORE<6:4>	
		ASRCNCORE<6:4>	
		REFIOACORE	
		REFIOBCORE	

1. The signals apart from ASRCPCORE<3:0> and ASRCNCORE<3:0> can be left unconnected, applicable only for this compensation. However, if a different compensation macro is used, refer to the respective User manual.

Figure 6. Constructing 1.8 V IO ring containing compensated IOs using compensation cell in IO ring



5 Contact information

ST users, login to **HELPDESK** (http://col2.cro.st.com/helpdesk) for submitting queries or support requests.

Non-ST users, contact Customer Support personnel.

Appendix A Cell naming convention

Table 21. Naming convention for compensation cells

Segment name	Description
COMPENSATION	Refers to the type of the cell. The value of this segment is COMPENSATION, which indicates a macro cell.
1st suffix	Refers to the type of the cell frame. The value of this segment is EXT_CSF, which indicates compatible standard frame.
2nd suffix	Refers to the operating voltage. The value of this segment is 1V8, which indicates 1.8 V supply voltage.
3rd suffix	Refers to the type of package of the IO ring. The value of this segment is FC, which indicates flip-chip package.
4th suffix	Refers to the type of configuration of the IO ring. The value of this segment is LIN, which indicates single row configuration.

Table 22. Example: segments in name of COMPENSATION_EXT_CSF_1V8_FC_LIN cell

Segment name	Segment Value	Description
Cell type	COMPENSATION	Compensation cell
1st suffix	EXT_CSF	Compatible standard frame
2nd suffix	1V8	1.8 V operating voltage
3rd suffix	FC	Flip-chip package
4th suffix	LIN	Linear configuration

Appendix B Connectivity of compensation signals

Note: If application constraints do not allow the placement of the compensation cell, the restrictions and guidelines given in this appendix should be followed. However, is not recommended to avoid the compensation cell.

B.1 Indicative compensation codes at slow/typical/fast PVT conditions

Table 23. Compensation codes(1)

PVT	ASRCP1V8<3:0>	ASRCN1V8<3:0>
Slow	LLLL	HHHH
Typical	HLHL	LHLH
Fast	HHHH	LLLL

1. Codes mentioned are indicative. For accurate codes based on Spice, refer *Section 5: Contact information*.

B.2 Restrictions for compensation unavoidance

Even if it is desired to avoid compensation cell, the use of the compensation cell is mandatory when any of the following conditions is applicable for concerned compensated IO IP, as these signals cannot be hard-coded, while trying to avoid compensation:

- If there are some analog reference (non rail-to-rail) signals generated by the compensation cell, and also used in the concerned IO, such as REFE, REFA, REFB, REFC, REFD, and VBG (bandgap voltage) etc., it is mandatory to use the compensation cell along with the IO library, as these signals are analog in nature and hence, cannot be hard-coded.
- In case there are some rail-to-rail control signals (for example, signal sensing the core supply off, etc.) that are being generated by the compensation cell and no other possibility to generate these signals anywhere else, and also used in the concerned IO, then, it is mandatory to use the compensation cell.

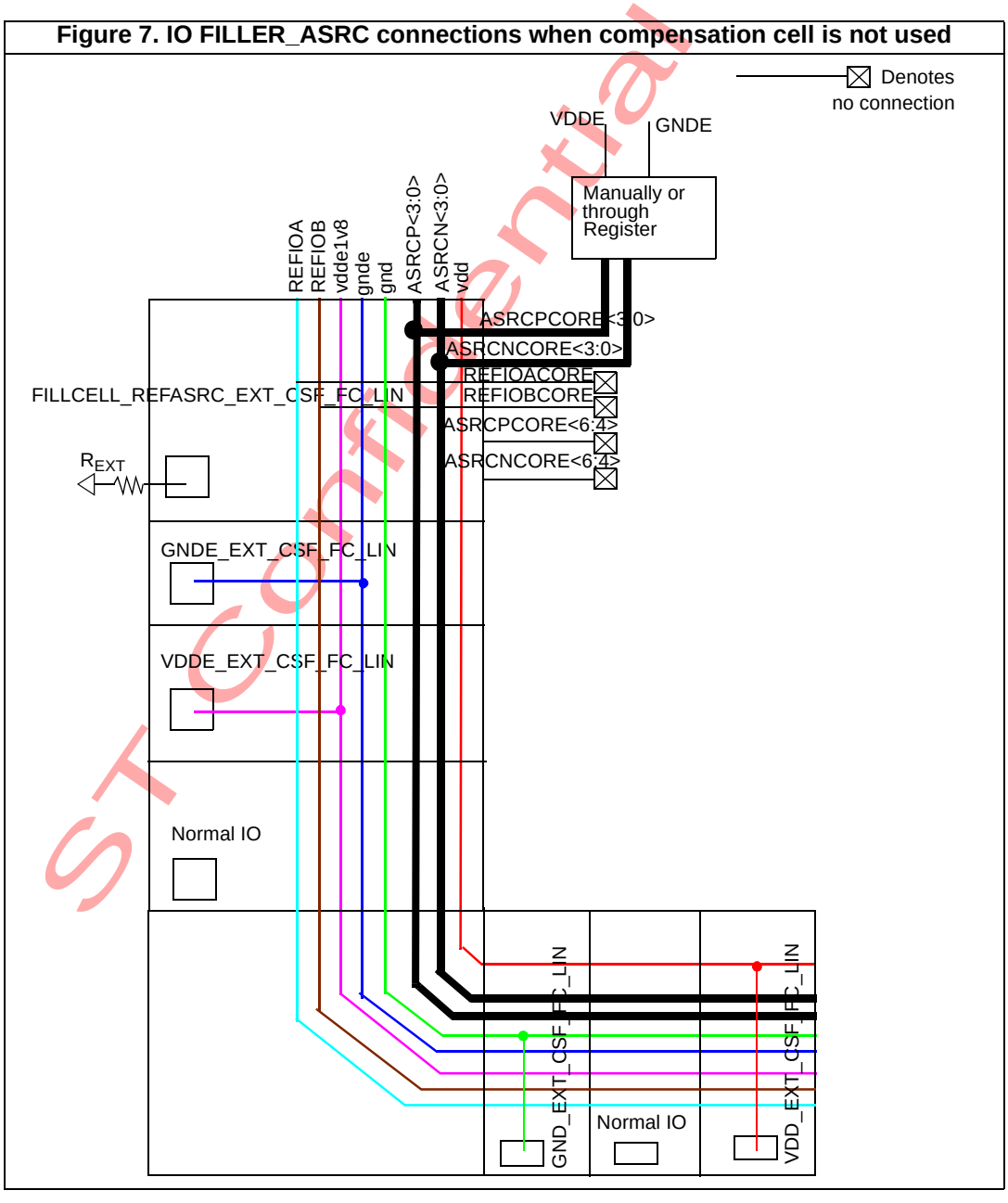
B.3 Guidelines when compensation cell is not used

None of the three conditions mentioned in *B.1: Indicative compensation codes at slow/typical/fast PVT conditions* are applicable for this compensated macro cell. So, in order to save chip area, the compensation cell usage can be avoided, while compromising on a few attributes related to the IO performance.

-)The usage of IOFILLER_REFARSRC_** cell is mandatory.
- The compensation codes should be either hard-coded or manually controlled through some registers, to valid full-swing logic levels.
  - In order to achieve the symmetric performance of IO across PVT conditions, the compensation codes can be hard-coded to typical PVT codes.

  - In order to achieve fast performance of the IO, the compensation codes can be hard-coded to the worst case codes, which might compromise with the SSN number, as the IOs would now become faster, even at best case PVT conditions.
  - In order to restrict the overshoots and undershoots, the compensation codes can be hard-coded to the best case codes, which might lead to the under-performance of IO on worst case PVT conditions.
- The logic signals (for example, Supply Selection mode pins, and so on) should be hard-coded to valid full swing logic levels.

Figure 7. IO FILLER_ASRC connections when compensation cell is not used



Appendix C Document revision history

Table 24. Document revision history

Date	Revision	Changes
09-Hun-16	1.2	Updated *Table 1: Operating conditions*, *Table 15: Library ESD targets*, *Table 17: Switching delay characteristics to normal mode*, *Table 18: Switching delay characteristics from normal mode*, and *Table 19: Mandatory libraries and cells*.
20-Jul-15	1.1	Updated *Table 1: Operating conditions*, *Table 15: Library ESD targets*, and *Table 16: Input pin capacitance*.
7-Nov-14	1.0	Initial release.