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C28SOI_SC_8_CLK_LL Databook

8 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

Overview

- C28SOI_SC_8_CLK_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 388 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

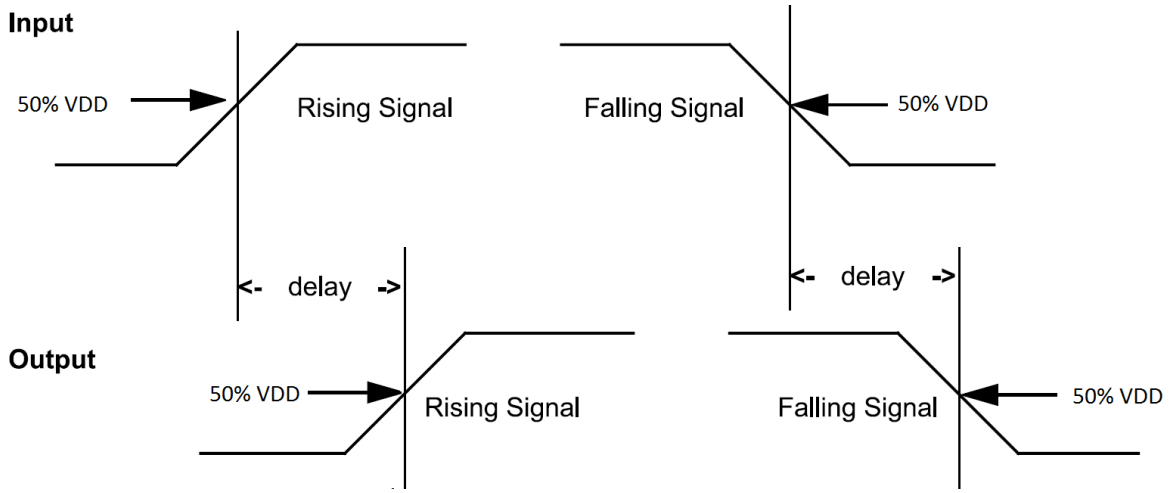


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

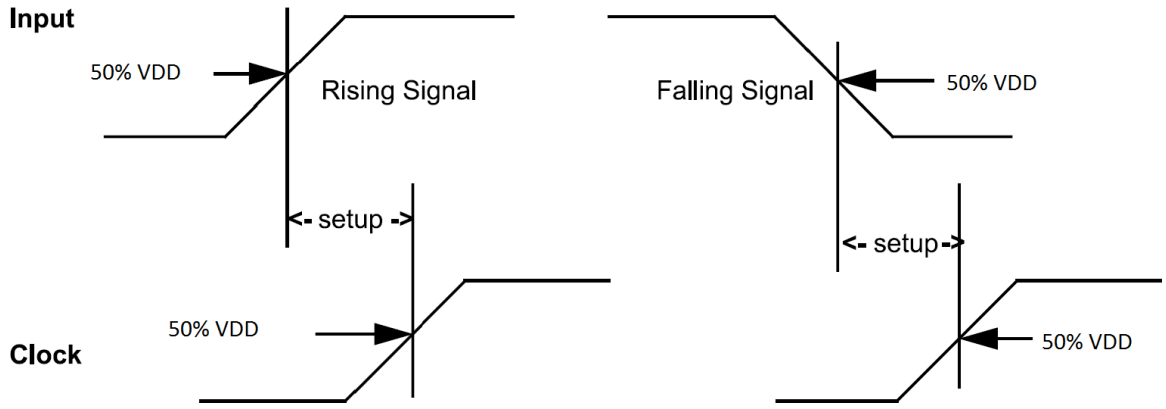


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

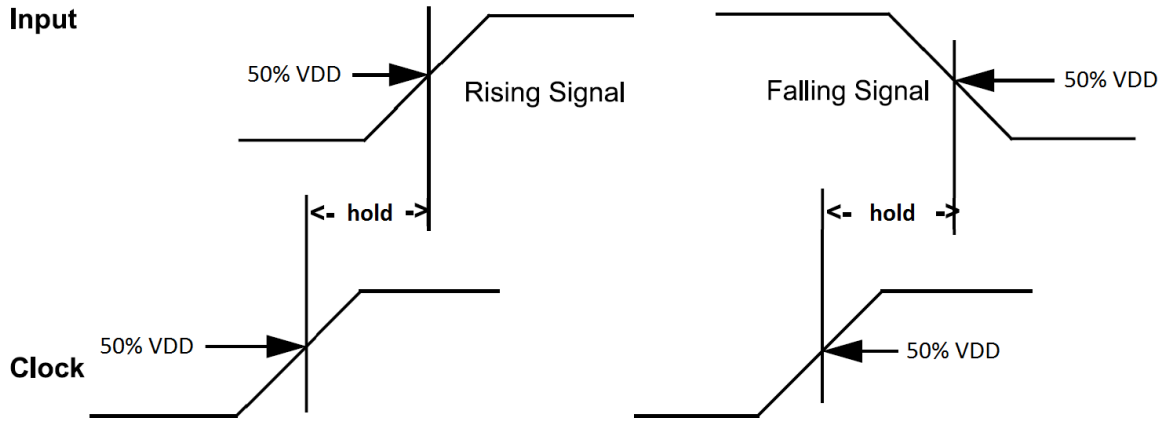


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

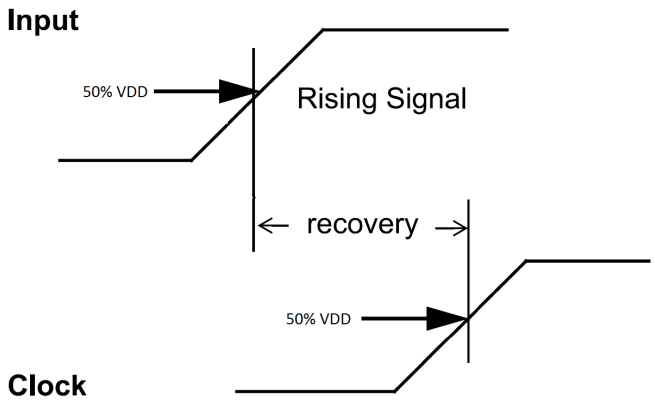


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

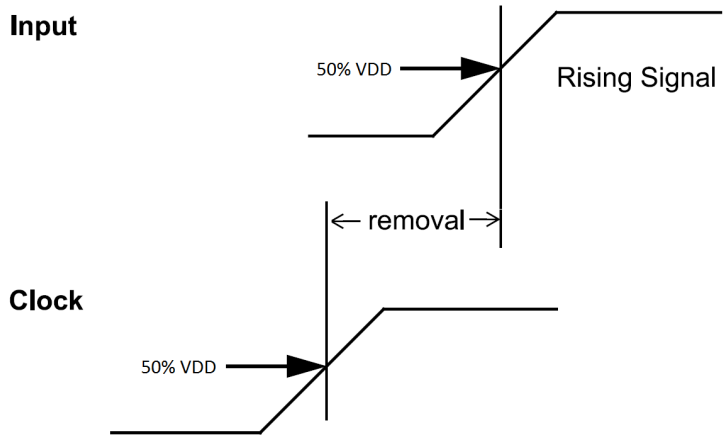


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

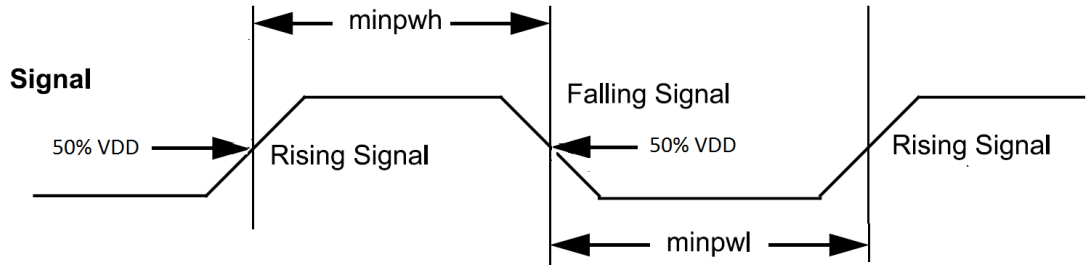


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

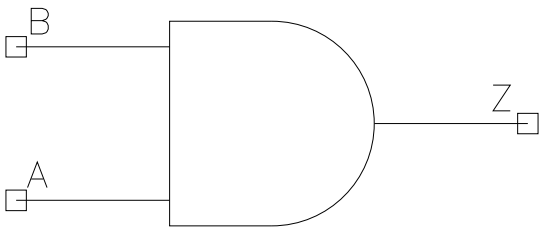
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

CNAND2

Cell Description

2 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	0.800	1.496	1.1968
X14_P4	0.800	1.496	1.1968
X14_P10	0.800	1.496	1.1968
X14_P16	0.800	1.496	1.1968
X19_P0	0.800	1.632	1.3056
X19_P4	0.800	1.632	1.3056
X19_P10	0.800	1.632	1.3056
X19_P16	0.800	1.632	1.3056
X27_P0	0.800	1.632	1.3056
X27_P4	0.800	1.632	1.3056
X27_P10	0.800	1.632	1.3056
X27_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0015	0.0016	0.0018	0.0019
B	0.0015	0.0016	0.0018	0.0019
	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0015	0.0016	0.0018	0.0019
B	0.0015	0.0016	0.0018	0.0019
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0013	0.0014	0.0015	0.0016
B	0.0012	0.0012	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0157	0.0180	0.8316	0.8881
A to Z ↑	0.0115	0.0132	0.9944	1.1232
B to Z ↓	0.0147	0.0168	0.8312	0.8882
B to Z ↑	0.0134	0.0150	0.9930	1.1221
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0215	0.0247	0.9701	1.0428
A to Z ↑	0.0158	0.0182	1.3235	1.5117
B to Z ↓	0.0199	0.0228	0.9687	1.0426
B to Z ↑	0.0176	0.0199	1.3223	1.5108
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0172	0.0196	0.6367	0.6809
A to Z ↑	0.0129	0.0148	0.7694	0.8673
B to Z ↓	0.0162	0.0185	0.6361	0.6803
B to Z ↑	0.0148	0.0167	0.7678	0.8669
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0234	0.0270	0.7429	0.8003
A to Z ↑	0.0176	0.0202	1.0192	1.1637
B to Z ↓	0.0220	0.0253	0.7435	0.7999
B to Z ↑	0.0196	0.0222	1.0191	1.1636
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0187	0.0219	0.5217	0.5591
A to Z ↑	0.0170	0.0192	0.4419	0.4991
B to Z ↓	0.0185	0.0216	0.5221	0.5596
B to Z ↑	0.0187	0.0211	0.4411	0.4991
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0261	0.0303	0.6119	0.6581
A to Z ↑	0.0221	0.0253	0.5879	0.6714
B to Z ↓	0.0256	0.0297	0.6120	0.6593
B to Z ↑	0.0242	0.0273	0.5879	0.6713

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X14_P0	1.237e-03	1.000e-20
X14_P4	3.189e-04	1.000e-20
X14_P10	7.450e-05	1.000e-20
X14_P16	3.014e-05	1.000e-20
X19_P0	1.486e-03	1.000e-20
X19_P4	3.815e-04	1.000e-20
X19_P10	8.855e-05	1.000e-20
X19_P16	3.561e-05	1.000e-20
X27_P0	2.183e-03	1.000e-20
X27_P4	5.472e-04	1.000e-20
X27_P10	1.223e-04	1.000e-20
X27_P16	4.727e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	8.645e-05	7.682e-05	6.989e-05	6.643e-05
B (output stable)	2.019e-04	2.070e-04	2.095e-04	2.296e-04
A to Z	9.014e-03	7.921e-03	7.331e-03	7.220e-03

B to Z	8.468e-03	7.356e-03	6.696e-03	6.509e-03
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	8.945e-05	7.700e-05	7.009e-05	6.666e-05
B (output stable)	2.057e-04	2.090e-04	2.097e-04	2.303e-04
A to Z	1.098e-02	9.744e-03	9.097e-03	8.979e-03
B to Z	1.051e-02	9.217e-03	8.481e-03	8.286e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	4.000e-05	3.441e-05	2.988e-05	2.787e-05
B (output stable)	6.818e-05	6.805e-05	6.712e-05	6.588e-05
A to Z	1.468e-02	1.312e-02	1.198e-02	1.181e-02
B to Z	1.459e-02	1.296e-02	1.173e-02	1.149e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

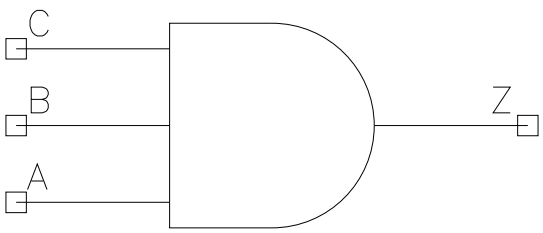
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAND3

Cell Description

3 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	0.800	0.816	0.6528
X10_P4	0.800	0.816	0.6528
X10_P10	0.800	0.816	0.6528
X10_P16	0.800	0.816	0.6528
X14_P0	0.800	1.360	1.0880
X14_P4	0.800	1.360	1.0880
X14_P10	0.800	1.360	1.0880
X14_P16	0.800	1.360	1.0880
X19_P0	0.800	1.496	1.1968
X19_P4	0.800	1.496	1.1968
X19_P10	0.800	1.496	1.1968
X19_P16	0.800	1.496	1.1968
X27_P0	0.800	2.312	1.8496
X27_P4	0.800	2.312	1.8496
X27_P10	0.800	2.312	1.8496
X27_P16	0.800	2.312	1.8496

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X10_P0	X10_P4	X10_P10	X10_P16
A	0.0007	0.0008	0.0008	0.0009
B	0.0006	0.0007	0.0007	0.0008
C	0.0007	0.0007	0.0008	0.0008
	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0012	0.0013	0.0013	0.0014
B	0.0010	0.0010	0.0011	0.0012

C	0.0009	0.0010	0.0011	0.0012
	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0014	0.0015	0.0016	0.0017
B	0.0013	0.0014	0.0015	0.0016
C	0.0012	0.0013	0.0014	0.0015
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0017	0.0018	0.0020	0.0021
B	0.0017	0.0018	0.0020	0.0021
C	0.0017	0.0018	0.0020	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	**X10_P4**	**X10_P0**	**X10_P4**
A to Z ↓	0.0165	0.0195	1.2211	1.3079
A to Z ↑	0.0187	0.0209	1.5431	1.7385
B to Z ↓	0.0157	0.0185	1.2216	1.3073
B to Z ↑	0.0202	0.0223	1.5434	1.7383
C to Z ↓	0.0148	0.0175	1.2197	1.3052
C to Z ↑	0.0213	0.0235	1.5429	1.7386
	X10_P10	**X10_P16**	**X10_P10**	**X10_P16**
A to Z ↓	0.0237	0.0276	1.4273	1.5380
A to Z ↑	0.0247	0.0284	2.0431	2.3338
B to Z ↓	0.0225	0.0261	1.4280	1.5364
B to Z ↑	0.0259	0.0294	2.0441	2.3308
C to Z ↓	0.0212	0.0246	1.4261	1.5343
C to Z ↑	0.0271	0.0305	2.0445	2.3327
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0169	0.0196	0.8425	0.9028
A to Z ↑	0.0178	0.0198	1.0486	1.1803
B to Z ↓	0.0159	0.0186	0.8427	0.9019
B to Z ↑	0.0194	0.0213	1.0477	1.1806
C to Z ↓	0.0151	0.0176	0.8414	0.9003
C to Z ↑	0.0207	0.0226	1.0470	1.1795
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0237	0.0277	0.9859	1.0625
A to Z ↑	0.0233	0.0272	1.3885	1.5840
B to Z ↓	0.0225	0.0262	0.9848	1.0614
B to Z ↑	0.0247	0.0283	1.3880	1.5827
C to Z ↓	0.0213	0.0248	0.9843	1.0599
C to Z ↑	0.0261	0.0296	1.3878	1.5832
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0160	0.0188	0.6264	0.6694
A to Z ↑	0.0178	0.0197	0.7744	0.8724
B to Z ↓	0.0151	0.0177	0.6257	0.6697
B to Z ↑	0.0194	0.0212	0.7729	0.8721
C to Z ↓	0.0142	0.0167	0.6257	0.6693
C to Z ↑	0.0206	0.0224	0.7734	0.8713
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0227	0.0265	0.7324	0.7886
A to Z ↑	0.0232	0.0269	1.0267	1.1724
B to Z ↓	0.0215	0.0250	0.7315	0.7876
B to Z ↑	0.0245	0.0280	1.0269	1.1725

C to Z ↓	0.0202	0.0235	0.7314	0.7870
C to Z ↑	0.0257	0.0291	1.0264	1.1721
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0197	0.0228	0.5225	0.5599
A to Z ↑	0.0178	0.0203	0.4455	0.5027
B to Z ↓	0.0188	0.0218	0.5228	0.5596
B to Z ↑	0.0196	0.0218	0.4454	0.5027
C to Z ↓	0.0183	0.0212	0.5222	0.5593
C to Z ↑	0.0204	0.0226	0.4448	0.5027
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0275	0.0319	0.6124	0.6585
A to Z ↑	0.0243	0.0281	0.5928	0.6769
B to Z ↓	0.0262	0.0304	0.6113	0.6584
B to Z ↑	0.0256	0.0291	0.5923	0.6771
C to Z ↓	0.0255	0.0294	0.6120	0.6586
C to Z ↑	0.0262	0.0296	0.5927	0.6768

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P0	7.771e-04	1.000e-20
X10_P4	1.933e-04	1.000e-20
X10_P10	4.324e-05	1.000e-20
X10_P16	1.707e-05	1.000e-20
X14_P0	1.094e-03	1.000e-20
X14_P4	2.724e-04	1.000e-20
X14_P10	6.136e-05	1.000e-20
X14_P16	2.440e-05	1.000e-20
X19_P0	1.493e-03	1.000e-20
X19_P4	3.739e-04	1.000e-20
X19_P10	8.416e-05	1.000e-20
X19_P16	3.333e-05	1.000e-20
X27_P0	2.524e-03	1.000e-20
X27_P4	6.208e-04	1.000e-20
X27_P10	1.364e-04	1.000e-20
X27_P16	5.268e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X10_P0	X10_P4	X10_P10	X10_P16
A (output stable)	2.442e-05	2.219e-05	2.037e-05	1.975e-05
B (output stable)	3.452e-05	3.131e-05	3.062e-05	4.649e-05
C (output stable)	6.464e-05	6.696e-05	7.736e-05	1.044e-04
A to Z	5.618e-03	5.009e-03	4.696e-03	4.644e-03
B to Z	5.466e-03	4.850e-03	4.509e-03	4.427e-03
C to Z	5.347e-03	4.704e-03	4.329e-03	4.218e-03
	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	3.350e-05	2.953e-05	2.764e-05	2.639e-05
B (output stable)	4.901e-05	4.462e-05	4.357e-05	6.431e-05
C (output stable)	9.353e-05	9.870e-05	1.132e-04	1.506e-04
A to Z	8.314e-03	7.348e-03	6.857e-03	6.831e-03
B to Z	8.028e-03	7.078e-03	6.552e-03	6.497e-03
C to Z	7.846e-03	6.861e-03	6.284e-03	6.190e-03

	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	4.464e-05	3.973e-05	3.707e-05	3.568e-05
B (output stable)	6.624e-05	6.068e-05	6.030e-05	9.051e-05
C (output stable)	1.343e-04	1.407e-04	1.626e-04	2.154e-04
A to Z	1.101e-02	9.714e-03	9.033e-03	8.977e-03
B to Z	1.064e-02	9.345e-03	8.628e-03	8.527e-03
C to Z	1.034e-02	9.017e-03	8.239e-03	8.087e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	9.909e-05	8.844e-05	8.234e-05	8.078e-05
B (output stable)	1.456e-04	1.347e-04	1.480e-04	2.082e-04
C (output stable)	3.095e-04	3.146e-04	4.122e-04	5.110e-04
A to Z	1.686e-02	1.513e-02	1.429e-02	1.418e-02
B to Z	1.635e-02	1.457e-02	1.364e-02	1.345e-02
C to Z	1.600e-02	1.412e-02	1.305e-02	1.275e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

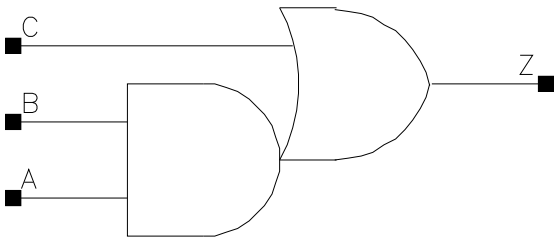
Pin Cycle (vdds)	X10_P0	X10_P4	X10_P10	X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	0.800	1.632	1.3056
X19_P4	0.800	1.632	1.3056
X19_P10	0.800	1.632	1.3056
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0013	0.0014	0.0015	0.0015
B	0.0011	0.0012	0.0013	0.0014
C	0.0012	0.0012	0.0013	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0218	0.0248	0.6340	0.6783
A to Z ↑	0.0159	0.0180	0.7548	0.8518
B to Z ↓	0.0209	0.0238	0.6335	0.6783
B to Z ↑	0.0178	0.0200	0.7545	0.8520
C to Z ↓	0.0198	0.0228	0.6324	0.6777
C to Z ↑	0.0167	0.0189	0.7483	0.8475
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0295	0.0341	0.7438	0.8027

A to Z ↑	0.0213	0.0243	1.0037	1.1474
B to Z ↓	0.0282	0.0324	0.7435	0.8022
B to Z ↑	0.0235	0.0266	1.0044	1.1461
C to Z ↓	0.0277	0.0324	0.7422	0.8007
C to Z ↑	0.0222	0.0252	0.9980	1.1390

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X19_P0	1.183e-03	1.000e-20
X19_P4	3.186e-04	1.000e-20
X19_P10	7.829e-05	1.000e-20
X19_P16	3.264e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	1.161e-04	1.170e-04	1.123e-04	9.077e-05
B (output stable)	1.287e-04	1.319e-04	1.279e-04	1.047e-04
C (output stable)	1.809e-04	1.525e-04	1.402e-04	1.395e-04
A to Z	1.092e-02	9.721e-03	9.040e-03	8.875e-03
B to Z	1.072e-02	9.467e-03	8.731e-03	8.510e-03
C to Z	1.126e-02	1.009e-02	9.517e-03	9.446e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

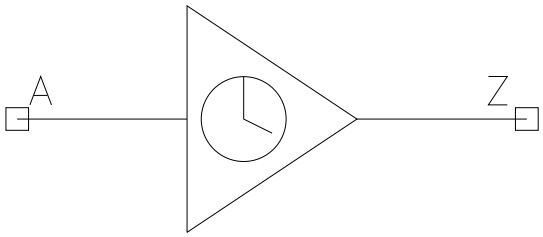
Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNBF

Cell Description

Buffer with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_CNBFX2_P0	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX2_P4	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX2_-P10	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX2_-P16	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_P0	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_P4	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_-P10	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_-P16	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX8_P0	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX8_P4	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX8_-P10	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX8_-P16	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX12_-P0	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX12_-P4	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX12_-P10	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX12_-P16	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX18_-P0	0.800	0.952	0.7616
C8T28SOI_LL_CNBFX18_-P4	0.800	0.952	0.7616
C8T28SOI_LL_CNBFX18_-P10	0.800	0.952	0.7616
C8T28SOI_LL_CNBFX18_-P16	0.800	0.952	0.7616

C8T28SOI_LL_CNBFX23_-P0	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX23_-P4	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX23_-P10	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX23_-P16	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX28_-P0	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX28_-P4	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX28_-P10	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX28_-P16	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX32_-P0	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX32_-P4	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX32_-P10	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX32_-P16	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX37_-P0	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX37_-P4	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX37_-P10	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX37_-P16	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX54_-P0	0.800	2.312	1.8496
C8T28SOI_LL_CNBFX54_-P4	0.800	2.312	1.8496
C8T28SOI_LL_CNBFX54_-P10	0.800	2.312	1.8496
C8T28SOI_LL_CNBFX54_-P16	0.800	2.312	1.8496
C8T28SOIDV_LL_-CNBFX18_P0	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX18_P4	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX18_P10	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX18_P16	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX28_P0	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNBFX28_P4	1.600	0.680	1.0880

C8T28SOIDV_LL_-CNBFX28_P10	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNBFX28_P16	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNBFX37_P0	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX37_P4	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX37_P10	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX37_P16	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX55_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX55_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX55_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX55_P16	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX74_P0	1.600	1.632	2.6112
C8T28SOIDV_LL_-CNBFX74_P4	1.600	1.632	2.6112
C8T28SOIDV_LL_-CNBFX74_P10	1.600	1.632	2.6112
C8T28SOIDV_LL_-CNBFX74_P16	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C8T28SOI_LL_-CNBFX2_P0	C8T28SOI_LL_-CNBFX2_P4	C8T28SOI_LL_-CNBFX2_P10	C8T28SOI_LL_-CNBFX2_P16
A	0.0005	0.0005	0.0006	0.0006
	C8T28SOI_LL_-CNBFX4_P0	C8T28SOI_LL_-CNBFX4_P4	C8T28SOI_LL_-CNBFX4_P10	C8T28SOI_LL_-CNBFX4_P16
A	0.0005	0.0006	0.0006	0.0006
	C8T28SOI_LL_-CNBFX8_P0	C8T28SOI_LL_-CNBFX8_P4	C8T28SOI_LL_-CNBFX8_P10	C8T28SOI_LL_-CNBFX8_P16
A	0.0006	0.0007	0.0007	0.0008
	C8T28SOI_LL_-CNBFX12_P0	C8T28SOI_LL_-CNBFX12_P4	C8T28SOI_LL_-CNBFX12_P10	C8T28SOI_LL_-CNBFX12_P16
A	0.0007	0.0007	0.0008	0.0008
	C8T28SOI_LL_-CNBFX18_P0	C8T28SOI_LL_-CNBFX18_P4	C8T28SOI_LL_-CNBFX18_P10	C8T28SOI_LL_-CNBFX18_P16
A	0.0010	0.0010	0.0011	0.0012
	C8T28SOI_LL_-CNBFX23_P0	C8T28SOI_LL_-CNBFX23_P4	C8T28SOI_LL_-CNBFX23_P10	C8T28SOI_LL_-CNBFX23_P16
A	0.0011	0.0012	0.0013	0.0014

	C8T28SOI_LL_-CNBFX28_P0	C8T28SOI_LL_-CNBFX28_P4	C8T28SOI_LL_-CNBFX28_P10	C8T28SOI_LL_-CNBFX28_P16
A	0.0013	0.0014	0.0015	0.0016
	C8T28SOI_LL_-CNBFX32_P0	C8T28SOI_LL_-CNBFX32_P4	C8T28SOI_LL_-CNBFX32_P10	C8T28SOI_LL_-CNBFX32_P16
A	0.0017	0.0018	0.0019	0.0020
	C8T28SOI_LL_-CNBFX37_P0	C8T28SOI_LL_-CNBFX37_P4	C8T28SOI_LL_-CNBFX37_P10	C8T28SOI_LL_-CNBFX37_P16
A	0.0018	0.0019	0.0020	0.0022
	C8T28SOI_LL_-CNBFX54_P0	C8T28SOI_LL_-CNBFX54_P4	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A	0.0024	0.0026	0.0028	0.0030
	C8T28SOIDV_LL_-CNBFX18_P0	C8T28SOIDV_LL_-CNBFX18_P4	C8T28SOIDV_LL_-CNBFX18_P10	C8T28SOIDV_LL_-CNBFX18_P16
A	0.0012	0.0013	0.0014	0.0015
	C8T28SOIDV_LL_-CNBFX28_P0	C8T28SOIDV_LL_-CNBFX28_P4	C8T28SOIDV_LL_-CNBFX28_P10	C8T28SOIDV_LL_-CNBFX28_P16
A	0.0013	0.0014	0.0015	0.0016
	C8T28SOIDV_LL_-CNBFX37_P0	C8T28SOIDV_LL_-CNBFX37_P4	C8T28SOIDV_LL_-CNBFX37_P10	C8T28SOIDV_LL_-CNBFX37_P16
A	0.0017	0.0019	0.0021	0.0022
	C8T28SOIDV_LL_-CNBFX55_P0	C8T28SOIDV_LL_-CNBFX55_P4	C8T28SOIDV_LL_-CNBFX55_P10	C8T28SOIDV_LL_-CNBFX55_P16
A	0.0024	0.0025	0.0028	0.0030
	C8T28SOIDV_LL_-CNBFX74_P0	C8T28SOIDV_LL_-CNBFX74_P4	C8T28SOIDV_LL_-CNBFX74_P10	C8T28SOIDV_LL_-CNBFX74_P16
A	0.0031	0.0033	0.0036	0.0038

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-CNBFX2_P0	**C8T28SOI_LL_-CNBFX2_P4**	**C8T28SOI_LL_-CNBFX2_P0**	**C8T28SOI_LL_-CNBFX2_P4**
A to Z ↓	0.0153	0.0175	4.8536	5.1812
A to Z ↑	0.0120	0.0136	5.7157	6.4703
	C8T28SOI_LL_-CNBFX2_P10	**C8T28SOI_LL_-CNBFX2_P16**	**C8T28SOI_LL_-CNBFX2_P10**	**C8T28SOI_LL_-CNBFX2_P16**
A to Z ↓	0.0207	0.0236	5.6466	6.0562
A to Z ↑	0.0162	0.0186	7.6656	8.8107
	C8T28SOI_LL_-CNBFX4_P0	**C8T28SOI_LL_-CNBFX4_P4**	**C8T28SOI_LL_-CNBFX4_P0**	**C8T28SOI_LL_-CNBFX4_P4**
A to Z ↓	0.0161	0.0184	2.9898	3.1980
A to Z ↑	0.0118	0.0134	3.1626	3.5757
	C8T28SOI_LL_-CNBFX4_P10	**C8T28SOI_LL_-CNBFX4_P16**	**C8T28SOI_LL_-CNBFX4_P10**	**C8T28SOI_LL_-CNBFX4_P16**
A to Z ↓	0.0218	0.0250	3.4914	3.7533
A to Z ↑	0.0160	0.0184	4.2175	4.8116
	C8T28SOI_LL_-CNBFX8_P0	**C8T28SOI_LL_-CNBFX8_P4**	**C8T28SOI_LL_-CNBFX8_P0**	**C8T28SOI_LL_-CNBFX8_P4**
A to Z ↓	0.0156	0.0179	1.4934	1.5989
A to Z ↑	0.0121	0.0139	1.5449	1.7488
	C8T28SOI_LL_-CNBFX8_P10	**C8T28SOI_LL_-CNBFX8_P16**	**C8T28SOI_LL_-CNBFX8_P10**	**C8T28SOI_LL_-CNBFX8_P16**
A to Z ↓	0.0213	0.0246	1.7471	1.8779

A to Z ↑	0.0165	0.0188	2.0608	2.3516
	C8T28SOI_LL_-CNBFX12_P0	**C8T28SOI_LL_-CNBFX12_P4**	**C8T28SOI_LL_-CNBFX12_P0**	**C8T28SOI_LL_-CNBFX12_P4**
A to Z ↓	0.0167	0.0194	1.0189	1.0919
A to Z ↑	0.0152	0.0171	1.0120	1.1491
	C8T28SOI_LL_-CNBFX12_P10	**C8T28SOI_LL_-CNBFX12_P16**	**C8T28SOI_LL_-CNBFX12_P10**	**C8T28SOI_LL_-CNBFX12_P16**
A to Z ↓	0.0233	0.0271	1.1940	1.2845
A to Z ↑	0.0201	0.0228	1.3552	1.5499
	C8T28SOI_LL_-CNBFX18_P0	**C8T28SOI_LL_-CNBFX18_P4**	**C8T28SOI_LL_-CNBFX18_P0**	**C8T28SOI_LL_-CNBFX18_P4**
A to Z ↓	0.0160	0.0185	0.6672	0.7155
A to Z ↑	0.0132	0.0151	0.7531	0.8546
	C8T28SOI_LL_-CNBFX18_P10	**C8T28SOI_LL_-CNBFX18_P16**	**C8T28SOI_LL_-CNBFX18_P10**	**C8T28SOI_LL_-CNBFX18_P16**
A to Z ↓	0.0221	0.0256	0.7831	0.8442
A to Z ↑	0.0178	0.0202	1.0070	1.1524
	C8T28SOI_LL_-CNBFX23_P0	**C8T28SOI_LL_-CNBFX23_P4**	**C8T28SOI_LL_-CNBFX23_P0**	**C8T28SOI_LL_-CNBFX23_P4**
A to Z ↓	0.0164	0.0188	0.5216	0.5590
A to Z ↑	0.0135	0.0153	0.6018	0.6831
	C8T28SOI_LL_-CNBFX23_P10	**C8T28SOI_LL_-CNBFX23_P16**	**C8T28SOI_LL_-CNBFX23_P10**	**C8T28SOI_LL_-CNBFX23_P16**
A to Z ↓	0.0227	0.0261	0.6110	0.6585
A to Z ↑	0.0182	0.0206	0.8065	0.9223
	C8T28SOI_LL_-CNBFX28_P0	**C8T28SOI_LL_-CNBFX28_P4**	**C8T28SOI_LL_-CNBFX28_P0**	**C8T28SOI_LL_-CNBFX28_P4**
A to Z ↓	0.0164	0.0189	0.4303	0.4615
A to Z ↑	0.0136	0.0155	0.5059	0.5719
	C8T28SOI_LL_-CNBFX28_P10	**C8T28SOI_LL_-CNBFX28_P16**	**C8T28SOI_LL_-CNBFX28_P10**	**C8T28SOI_LL_-CNBFX28_P16**
A to Z ↓	0.0225	0.0260	0.5054	0.5441
A to Z ↑	0.0182	0.0207	0.6757	0.7713
	C8T28SOI_LL_-CNBFX32_P0	**C8T28SOI_LL_-CNBFX32_P4**	**C8T28SOI_LL_-CNBFX32_P0**	**C8T28SOI_LL_-CNBFX32_P4**
A to Z ↓	0.0169	0.0195	0.3729	0.3994
A to Z ↑	0.0136	0.0155	0.4357	0.4931
	C8T28SOI_LL_-CNBFX32_P10	**C8T28SOI_LL_-CNBFX32_P16**	**C8T28SOI_LL_-CNBFX32_P10**	**C8T28SOI_LL_-CNBFX32_P16**
A to Z ↓	0.0232	0.0267	0.4369	0.4707
A to Z ↑	0.0182	0.0207	0.5813	0.6639
	C8T28SOI_LL_-CNBFX37_P0	**C8T28SOI_LL_-CNBFX37_P4**	**C8T28SOI_LL_-CNBFX37_P0**	**C8T28SOI_LL_-CNBFX37_P4**
A to Z ↓	0.0168	0.0192	0.3236	0.3465
A to Z ↑	0.0140	0.0158	0.3800	0.4306
	C8T28SOI_LL_-CNBFX37_P10	**C8T28SOI_LL_-CNBFX37_P16**	**C8T28SOI_LL_-CNBFX37_P10**	**C8T28SOI_LL_-CNBFX37_P16**
A to Z ↓	0.0230	0.0265	0.3793	0.4089
A to Z ↑	0.0186	0.0211	0.5074	0.5801
	C8T28SOI_LL_-CNBFX54_P0	**C8T28SOI_LL_-CNBFX54_P4**	**C8T28SOI_LL_-CNBFX54_P0**	**C8T28SOI_LL_-CNBFX54_P4**
A to Z ↓	0.0166	0.0190	0.2258	0.2419
A to Z ↑	0.0144	0.0162	0.2539	0.2881

	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A to Z ↓	0.0227	0.0263	0.2648	0.2857
A to Z ↑	0.0189	0.0216	0.3401	0.3885
	C8T28SOIDV_LL_-CNBFX18_P0	**C8T28SOIDV_LL_-CNBFX18_P4**	**C8T28SOIDV_LL_-CNBFX18_P0**	**C8T28SOIDV_LL_-CNBFX18_P4**
A to Z ↓	0.0144	0.0167	0.6390	0.6842
A to Z ↑	0.0139	0.0156	0.7459	0.8446
	C8T28SOIDV_LL_-CNBFX18_P10	**C8T28SOIDV_LL_-CNBFX18_P16**	**C8T28SOIDV_LL_-CNBFX18_P10**	**C8T28SOIDV_LL_-CNBFX18_P16**
A to Z ↓	0.0201	0.0234	0.7496	0.8084
A to Z ↑	0.0183	0.0208	0.9972	1.1408
	C8T28SOIDV_LL_-CNBFX28_P0	**C8T28SOIDV_LL_-CNBFX28_P4**	**C8T28SOIDV_LL_-CNBFX28_P0**	**C8T28SOIDV_LL_-CNBFX28_P4**
A to Z ↓	0.0164	0.0192	0.4315	0.4629
A to Z ↑	0.0145	0.0165	0.5095	0.5770
	C8T28SOIDV_LL_-CNBFX28_P10	**C8T28SOIDV_LL_-CNBFX28_P16**	**C8T28SOIDV_LL_-CNBFX28_P10**	**C8T28SOIDV_LL_-CNBFX28_P16**
A to Z ↓	0.0228	0.0268	0.5078	0.5475
A to Z ↑	0.0191	0.0220	0.6802	0.7772
	C8T28SOIDV_LL_-CNBFX37_P0	**C8T28SOIDV_LL_-CNBFX37_P4**	**C8T28SOIDV_LL_-CNBFX37_P0**	**C8T28SOIDV_LL_-CNBFX37_P4**
A to Z ↓	0.0160	0.0186	0.3247	0.3484
A to Z ↑	0.0136	0.0155	0.3827	0.4334
	C8T28SOIDV_LL_-CNBFX37_P10	**C8T28SOIDV_LL_-CNBFX37_P16**	**C8T28SOIDV_LL_-CNBFX37_P10**	**C8T28SOIDV_LL_-CNBFX37_P16**
A to Z ↓	0.0225	0.0260	0.3825	0.4121
A to Z ↑	0.0185	0.0209	0.5111	0.5831
	C8T28SOIDV_LL_-CNBFX55_P0	**C8T28SOIDV_LL_-CNBFX55_P4**	**C8T28SOIDV_LL_-CNBFX55_P0**	**C8T28SOIDV_LL_-CNBFX55_P4**
A to Z ↓	0.0159	0.0184	0.2197	0.2355
A to Z ↑	0.0141	0.0159	0.2546	0.2883
	C8T28SOIDV_LL_-CNBFX55_P10	**C8T28SOIDV_LL_-CNBFX55_P16**	**C8T28SOIDV_LL_-CNBFX55_P10**	**C8T28SOIDV_LL_-CNBFX55_P16**
A to Z ↓	0.0222	0.0259	0.2584	0.2787
A to Z ↑	0.0186	0.0213	0.3396	0.3885
	C8T28SOIDV_LL_-CNBFX74_P0	**C8T28SOIDV_LL_-CNBFX74_P4**	**C8T28SOIDV_LL_-CNBFX74_P0**	**C8T28SOIDV_LL_-CNBFX74_P4**
A to Z ↓	0.0167	0.0193	0.1664	0.1787
A to Z ↑	0.0155	0.0175	0.1926	0.2182
	C8T28SOIDV_LL_-CNBFX74_P10	**C8T28SOIDV_LL_-CNBFX74_P16**	**C8T28SOIDV_LL_-CNBFX74_P10**	**C8T28SOIDV_LL_-CNBFX74_P16**
A to Z ↓	0.0233	0.0271	0.1962	0.2121
A to Z ↑	0.0204	0.0232	0.2574	0.2937

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_CNBFX2_P0	1.790e-04	1.000e-20
C8T28SOI_LL_CNBFX2_P4	4.578e-05	1.000e-20
C8T28SOI_LL_CNBFX2_P10	1.130e-05	1.000e-20
C8T28SOI_LL_CNBFX2_P16	4.807e-06	1.000e-20
C8T28SOI_LL_CNBFX4_P0	2.849e-04	1.000e-20

C8T28SOI_LL_CNBFX4_P4	7.426e-05	1.000e-20
C8T28SOI_LL_CNBFX4_P10	1.795e-05	1.000e-20
C8T28SOI_LL_CNBFX4_P16	7.401e-06	1.000e-20
C8T28SOI_LL_CNBFX8_P0	5.755e-04	1.000e-20
C8T28SOI_LL_CNBFX8_P4	1.477e-04	1.000e-20
C8T28SOI_LL_CNBFX8_P10	3.448e-05	1.000e-20
C8T28SOI_LL_CNBFX8_P16	1.381e-05	1.000e-20
C8T28SOI_LL_CNBFX12_P0	8.282e-04	1.000e-20
C8T28SOI_LL_CNBFX12_P4	2.110e-04	1.000e-20
C8T28SOI_LL_CNBFX12_P10	4.850e-05	1.000e-20
C8T28SOI_LL_CNBFX12_P16	1.917e-05	1.000e-20
C8T28SOI_LL_CNBFX18_P0	1.047e-03	1.000e-20
C8T28SOI_LL_CNBFX18_P4	2.710e-04	1.000e-20
C8T28SOI_LL_CNBFX18_P10	6.389e-05	1.000e-20
C8T28SOI_LL_CNBFX18_P16	2.576e-05	1.000e-20
C8T28SOI_LL_CNBFX23_P0	1.375e-03	1.000e-20
C8T28SOI_LL_CNBFX23_P4	3.511e-04	1.000e-20
C8T28SOI_LL_CNBFX23_P10	8.150e-05	1.000e-20
C8T28SOI_LL_CNBFX23_P16	3.260e-05	1.000e-20
C8T28SOI_LL_CNBFX28_P0	1.592e-03	1.000e-20
C8T28SOI_LL_CNBFX28_P4	4.132e-04	1.000e-20
C8T28SOI_LL_CNBFX28_P10	9.693e-05	1.000e-20
C8T28SOI_LL_CNBFX28_P16	3.885e-05	1.000e-20
C8T28SOI_LL_CNBFX32_P0	1.842e-03	1.000e-20
C8T28SOI_LL_CNBFX32_P4	4.742e-04	1.000e-20
C8T28SOI_LL_CNBFX32_P10	1.111e-04	1.000e-20
C8T28SOI_LL_CNBFX32_P16	4.468e-05	1.000e-20
C8T28SOI_LL_CNBFX37_P0	2.155e-03	1.000e-20
C8T28SOI_LL_CNBFX37_P4	5.549e-04	1.000e-20
C8T28SOI_LL_CNBFX37_P10	1.294e-04	1.000e-20
C8T28SOI_LL_CNBFX37_P16	5.173e-05	1.000e-20
C8T28SOI_LL_CNBFX54_P0	3.286e-03	1.000e-20
C8T28SOI_LL_CNBFX54_P4	8.371e-04	1.000e-20
C8T28SOI_LL_CNBFX54_P10	1.924e-04	1.000e-20
C8T28SOI_LL_CNBFX54_P16	7.617e-05	1.000e-20
C8T28SOIDV_LL_CNBFX18_P0	1.208e-03	1.000e-20
C8T28SOIDV_LL_CNBFX18_P4	3.094e-04	1.000e-20
C8T28SOIDV_LL_CNBFX18_P10	7.172e-05	1.000e-20
C8T28SOIDV_LL_CNBFX18_P16	2.849e-05	1.000e-20
C8T28SOIDV_LL_CNBFX28_P0	1.672e-03	1.000e-20
C8T28SOIDV_LL_CNBFX28_P4	4.288e-04	1.000e-20
C8T28SOIDV_LL_CNBFX28_P10	9.911e-05	1.000e-20
C8T28SOIDV_LL_CNBFX28_P16	3.926e-05	1.000e-20
C8T28SOIDV_LL_CNBFX37_P0	2.210e-03	1.000e-20
C8T28SOIDV_LL_CNBFX37_P4	5.635e-04	1.000e-20
C8T28SOIDV_LL_CNBFX37_P10	1.298e-04	1.000e-20
C8T28SOIDV_LL_CNBFX37_P16	5.136e-05	1.000e-20
C8T28SOIDV_LL_CNBFX55_P0	3.271e-03	1.000e-20
C8T28SOIDV_LL_CNBFX55_P4	8.360e-04	1.000e-20
C8T28SOIDV_LL_CNBFX55_P10	1.922e-04	1.000e-20
C8T28SOIDV_LL_CNBFX55_P16	7.587e-05	1.000e-20
C8T28SOIDV_LL_CNBFX74_P0	4.201e-03	1.000e-20

C8T28SOIDV_LL_CNBFX74_P4	1.076e-03	1.000e-20
C8T28SOIDV_LL_CNBFX74_P10	2.477e-04	1.000e-20
C8T28SOIDV_LL_CNBFX74_P16	9.781e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_-CNBFX2_P0	C8T28SOI_LL_-CNBFX2_P4	C8T28SOI_LL_-CNBFX2_P10	C8T28SOI_LL_-CNBFX2_P16
A to Z	1.990e-03	1.726e-03	1.580e-03	1.543e-03
	C8T28SOI_LL_-CNBFX4_P0	C8T28SOI_LL_-CNBFX4_P4	C8T28SOI_LL_-CNBFX4_P10	C8T28SOI_LL_-CNBFX4_P16
A to Z	2.519e-03	2.197e-03	2.030e-03	1.995e-03
	C8T28SOI_LL_-CNBFX8_P0	C8T28SOI_LL_-CNBFX8_P4	C8T28SOI_LL_-CNBFX8_P10	C8T28SOI_LL_-CNBFX8_P16
A to Z	4.345e-03	3.769e-03	3.450e-03	3.377e-03
	C8T28SOI_LL_-CNBFX12_P0	C8T28SOI_LL_-CNBFX12_P4	C8T28SOI_LL_-CNBFX12_P10	C8T28SOI_LL_-CNBFX12_P16
A to Z	6.374e-03	5.603e-03	5.165e-03	5.065e-03
	C8T28SOI_LL_-CNBFX18_P0	C8T28SOI_LL_-CNBFX18_P4	C8T28SOI_LL_-CNBFX18_P10	C8T28SOI_LL_-CNBFX18_P16
A to Z	8.702e-03	7.621e-03	6.987e-03	6.801e-03
	C8T28SOI_LL_-CNBFX23_P0	C8T28SOI_LL_-CNBFX23_P4	C8T28SOI_LL_-CNBFX23_P10	C8T28SOI_LL_-CNBFX23_P16
A to Z	1.106e-02	9.632e-03	8.950e-03	8.722e-03
	C8T28SOI_LL_-CNBFX28_P0	C8T28SOI_LL_-CNBFX28_P4	C8T28SOI_LL_-CNBFX28_P10	C8T28SOI_LL_-CNBFX28_P16
A to Z	1.300e-02	1.141e-02	1.040e-02	1.013e-02
	C8T28SOI_LL_-CNBFX32_P0	C8T28SOI_LL_-CNBFX32_P4	C8T28SOI_LL_-CNBFX32_P10	C8T28SOI_LL_-CNBFX32_P16
A to Z	1.549e-02	1.362e-02	1.246e-02	1.216e-02
	C8T28SOI_LL_-CNBFX37_P0	C8T28SOI_LL_-CNBFX37_P4	C8T28SOI_LL_-CNBFX37_P10	C8T28SOI_LL_-CNBFX37_P16
A to Z	1.781e-02	1.554e-02	1.428e-02	1.392e-02
	C8T28SOI_LL_-CNBFX54_P0	C8T28SOI_LL_-CNBFX54_P4	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A to Z	2.619e-02	2.287e-02	2.087e-02	2.046e-02
	C8T28SOIDV_LL_-CNBFX18_P0	C8T28SOIDV_LL_-CNBFX18_P4	C8T28SOIDV_LL_-CNBFX18_P10	C8T28SOIDV_LL_-CNBFX18_P16
A to Z	8.847e-03	7.698e-03	7.061e-03	6.926e-03
	C8T28SOIDV_LL_-CNBFX28_P0	C8T28SOIDV_LL_-CNBFX28_P4	C8T28SOIDV_LL_-CNBFX28_P10	C8T28SOIDV_LL_-CNBFX28_P16
A to Z	1.293e-02	1.148e-02	1.045e-02	1.039e-02
	C8T28SOIDV_LL_-CNBFX37_P0	C8T28SOIDV_LL_-CNBFX37_P4	C8T28SOIDV_LL_-CNBFX37_P10	C8T28SOIDV_LL_-CNBFX37_P16
A to Z	1.687e-02	1.472e-02	1.369e-02	1.333e-02
	C8T28SOIDV_LL_-CNBFX55_P0	C8T28SOIDV_LL_-CNBFX55_P4	C8T28SOIDV_LL_-CNBFX55_P10	C8T28SOIDV_LL_-CNBFX55_P16
A to Z	2.497e-02	2.183e-02	2.015e-02	1.987e-02
	C8T28SOIDV_LL_-CNBFX74_P0	C8T28SOIDV_LL_-CNBFX74_P4	C8T28SOIDV_LL_-CNBFX74_P10	C8T28SOIDV_LL_-CNBFX74_P16
A to Z	3.360e-02	2.966e-02	2.716e-02	2.684e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

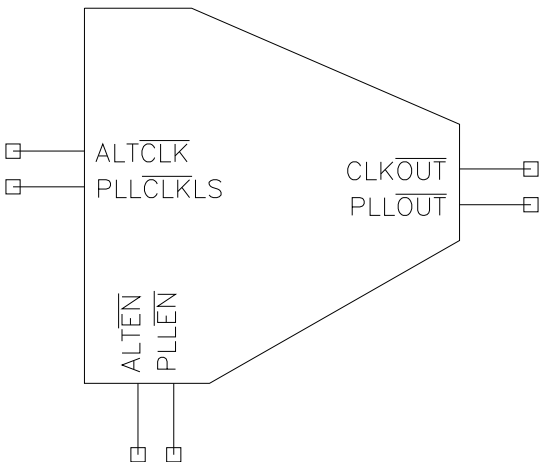
Pin Cycle (vdds)	C8T28SOI_LL_-CNBFX2_P0	C8T28SOI_LL_-CNBFX2_P4	C8T28SOI_LL_-CNBFX2_P10	C8T28SOI_LL_-CNBFX2_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX4_P0	C8T28SOI_LL_-CNBFX4_P4	C8T28SOI_LL_-CNBFX4_P10	C8T28SOI_LL_-CNBFX4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX8_P0	C8T28SOI_LL_-CNBFX8_P4	C8T28SOI_LL_-CNBFX8_P10	C8T28SOI_LL_-CNBFX8_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX12_P0	C8T28SOI_LL_-CNBFX12_P4	C8T28SOI_LL_-CNBFX12_P10	C8T28SOI_LL_-CNBFX12_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX18_P0	C8T28SOI_LL_-CNBFX18_P4	C8T28SOI_LL_-CNBFX18_P10	C8T28SOI_LL_-CNBFX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX23_P0	C8T28SOI_LL_-CNBFX23_P4	C8T28SOI_LL_-CNBFX23_P10	C8T28SOI_LL_-CNBFX23_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX28_P0	C8T28SOI_LL_-CNBFX28_P4	C8T28SOI_LL_-CNBFX28_P10	C8T28SOI_LL_-CNBFX28_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX32_P0	C8T28SOI_LL_-CNBFX32_P4	C8T28SOI_LL_-CNBFX32_P10	C8T28SOI_LL_-CNBFX32_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX37_P0	C8T28SOI_LL_-CNBFX37_P4	C8T28SOI_LL_-CNBFX37_P10	C8T28SOI_LL_-CNBFX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX54_P0	C8T28SOI_LL_-CNBFX54_P4	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX18_P0	C8T28SOIDV_LL_-CNBFX18_P4	C8T28SOIDV_LL_-CNBFX18_P10	C8T28SOIDV_LL_-CNBFX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX28_P0	C8T28SOIDV_LL_-CNBFX28_P4	C8T28SOIDV_LL_-CNBFX28_P10	C8T28SOIDV_LL_-CNBFX28_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX37_P0	C8T28SOIDV_LL_-CNBFX37_P4	C8T28SOIDV_LL_-CNBFX37_P10	C8T28SOIDV_LL_-CNBFX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX55_P0	C8T28SOIDV_LL_-CNBFX55_P4	C8T28SOIDV_LL_-CNBFX55_P10	C8T28SOIDV_LL_-CNBFX55_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX74_P0	C8T28SOIDV_LL_-CNBFX74_P4	C8T28SOIDV_LL_-CNBFX74_P10	C8T28SOIDV_LL_-CNBFX74_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNGFMUX21

Cell Description

2:1 Glitch-free MUX for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X30_P0	1.600	4.488	7.1808
X30_P4	1.600	4.488	7.1808
X30_P10	1.600	4.488	7.1808
X30_P16	1.600	4.488	7.1808

Truth Table

PLL_CLK_LS	ALT_CLK	IPLL_EN_LD	IALT_EN_LD	CLK_OUT
0	-	-	0	0
0	0	-	-	0
-	0	0	-	0
PLL_CLK_LS	1	-	1	1
1	ALT_CLK	1	-	1
1	1	0	0	0

PLL_CLK_LS	PLL_OUT
PLL_CLK_LS	PLL_CLK_LS
1	1

PLL_EN	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD
PLL_EN	0	-	PLL_EN
-	-	IPLL_EN_LD	IPLL_EN_LD
-	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

ALT_EN	ALT_CLK	IALT_EN_LD	IALT_EN_LD
ALT_EN	0	-	ALT_EN
-	-	IALT_EN_LD	IALT_EN_LD
-	ALT_CLK	IALT_EN_LD	IALT_EN_LD

Pin Capacitance

Pin	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK	0.0027	0.0029	0.0031	0.0032
ALT_EN	0.0005	0.0005	0.0006	0.0006
PLL_CLK_LS	0.0046	0.0048	0.0051	0.0054
PLL_EN	0.0005	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**
ALT_CLK to CLK_OUT ↓	0.0220	0.0252	0.4405	0.4741
ALT_CLK to CLK_OUT ↑	0.0200	0.0228	0.5501	0.6229
PLL_CLK_LS to CLK_OUT ↓	0.0214	0.0243	0.4438	0.4774
PLL_CLK_LS to CLK_OUT ↑	0.0222	0.0248	0.5519	0.6262
PLL_CLK_LS to PLL_OUT ↓	0.0139	0.0159	0.3673	0.3925
PLL_CLK_LS to PLL_OUT ↑	0.0149	0.0165	0.5028	0.5694
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
ALT_CLK to CLK_OUT ↓	0.0301	0.0349	0.5229	0.5676
ALT_CLK to CLK_OUT ↑	0.0274	0.0321	0.7331	0.8369
PLL_CLK_LS to CLK_OUT ↓	0.0290	0.0332	0.5263	0.5708
PLL_CLK_LS to CLK_OUT ↑	0.0291	0.0332	0.7367	0.8418
PLL_CLK_LS to PLL_OUT ↓	0.0192	0.0222	0.4289	0.4617
PLL_CLK_LS to PLL_OUT ↑	0.0192	0.0218	0.6713	0.7675

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0416	0.0461	0.0540	0.0598
ALT_EN ↓	hold_rising to ALT_CLK	-0.0101	-0.0149	-0.0252	-0.0296
ALT_EN ↑	hold_rising to ALT_CLK	0.0083	0.0025	0.0009	-0.0050
ALT_EN ↓	setup_rising to ALT_CLK	0.0379	0.0396	0.0498	0.0601

ALT_EN ↑	setup_rising to ALT_CLK	0.0221	0.0243	0.0288	0.0337
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0384	0.0415	0.0508	0.0553
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0084	-0.0101	-0.0208	-0.0247
PLL_EN ↑	hold_rising to PLL_CLK_LS	0.0079	0.0079	0.0025	0.0009
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0330	0.0347	0.0449	0.0494
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0168	0.0223	0.0298	0.0347

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X30_P0	5.931e-03	1.000e-20
X30_P4	1.524e-03	1.000e-20
X30_P10	3.637e-04	1.000e-20
X30_P16	1.516e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	5.522e-03	5.190e-03	5.105e-03	5.210e-03
ALT_EN (output stable)	3.235e-03	3.030e-03	2.960e-03	2.990e-03
PLL_CLK_LS (output stable)	9.343e-02	2.992e-02	1.848e-02	1.651e-02
PLL_EN (output stable)	2.871e-03	2.730e-03	2.724e-03	2.793e-03
ALT_CLK to CLK_OUT	1.945e-02	1.817e-02	1.781e-02	1.815e-02
PLL_CLK_LS to CLK_OUT	1.646e-02	1.320e-02	1.248e-02	1.238e-02
PLL_CLK_LS to PLL_OUT	1.310e-01	3.605e-02	1.914e-02	1.600e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_CLK to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00

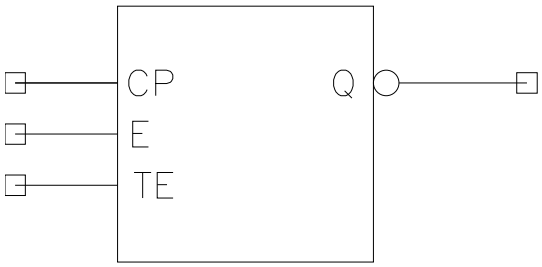
PLL_CLK_LS to PLL_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNHLS

Cell Description

Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LLP1_-CNHLSX10_P0	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX10_P4	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX10_P10	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX10_P16	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX14_P0	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX14_P4	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX14_P10	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX14_P16	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX19_P0	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX19_P4	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX19_P10	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX19_P16	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX24_P0	0.800	2.584	2.0672
C8T28SOI_LLP1_-CNHLSX24_P4	0.800	2.584	2.0672
C8T28SOI_LLP1_-CNHLSX24_P10	0.800	2.584	2.0672
C8T28SOI_LLP1_-CNHLSX24_P16	0.800	2.584	2.0672

C8T28SOI_LLP1_-CNHLSX29_P0	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX29_P4	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX29_P10	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX29_P16	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX34_P0	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX34_P4	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX34_P10	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX34_P16	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX38_P0	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX38_P4	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX38_P10	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX38_P16	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX57_P0	0.800	4.080	3.2640
C8T28SOI_LLP1_-CNHLSX57_P4	0.800	4.080	3.2640
C8T28SOI_LLP1_-CNHLSX57_P10	0.800	4.080	3.2640
C8T28SOI_LLP1_-CNHLSX57_P16	0.800	4.080	3.2640
C8T28SOI_LLP_-CNHLSX4_P0	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX4_P4	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX4_P10	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX4_P16	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX9_P0	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX9_P4	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX9_P10	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX9_P16	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX13_P0	0.800	2.312	1.8496
C8T28SOI_LLP_-CNHLSX13_P4	0.800	2.312	1.8496

C8T28SOI_LLP_-CNHLSX13_P10	0.800	2.312	1.8496
C8T28SOI_LLP_-CNHLSX13_P16	0.800	2.312	1.8496
C8T28SOI_LLP_-CNHLSX17_P0	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX17_P4	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX17_P10	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX17_P16	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX21_P0	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX21_P4	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX21_P10	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX21_P16	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX27_P0	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX27_P4	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX27_P10	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX27_P16	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX30_P0	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX30_P4	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX30_P10	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX30_P16	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX38_P0	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX38_P4	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX38_P10	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX38_P16	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX54_P0	0.800	5.304	4.2432
C8T28SOI_LLP_-CNHLSX54_P4	0.800	5.304	4.2432
C8T28SOI_LLP_-CNHLSX54_P10	0.800	5.304	4.2432
C8T28SOI_LLP_-CNHLSX54_P16	0.800	5.304	4.2432

Truth Table

CP	E	TE	OLDIE	Q
0	-	-	-	0
1	-	-	OLDIE	OLDIE

OLDIE	OLDIE
OLDIE	OLDIE

Pin Capacitance

Pin	C8T28SOI_LLP1_-CNHLSX10_P0	C8T28SOI_LLP1_-CNHLSX10_P4	C8T28SOI_LLP1_-CNHLSX10_P10	C8T28SOI_LLP1_-CNHLSX10_P16
CP	0.0012	0.0013	0.0014	0.0014
E	0.0004	0.0004	0.0004	0.0004
TE	0.0007	0.0007	0.0008	0.0008
	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P10	C8T28SOI_LLP1_-CNHLSX14_P16
CP	0.0012	0.0013	0.0013	0.0014
E	0.0004	0.0004	0.0004	0.0004
TE	0.0007	0.0007	0.0008	0.0008
	C8T28SOI_LLP1_-CNHLSX19_P0	C8T28SOI_LLP1_-CNHLSX19_P4	C8T28SOI_LLP1_-CNHLSX19_P10	C8T28SOI_LLP1_-CNHLSX19_P16
CP	0.0018	0.0019	0.0021	0.0022
E	0.0004	0.0004	0.0004	0.0004
TE	0.0007	0.0007	0.0008	0.0008
	C8T28SOI_LLP1_-CNHLSX24_P0	C8T28SOI_LLP1_-CNHLSX24_P4	C8T28SOI_LLP1_-CNHLSX24_P10	C8T28SOI_LLP1_-CNHLSX24_P16
CP	0.0018	0.0019	0.0021	0.0022
E	0.0004	0.0004	0.0004	0.0004
TE	0.0007	0.0007	0.0008	0.0008
	C8T28SOI_LLP1_-CNHLSX29_P0	C8T28SOI_LLP1_-CNHLSX29_P4	C8T28SOI_LLP1_-CNHLSX29_P10	C8T28SOI_LLP1_-CNHLSX29_P16
CP	0.0019	0.0020	0.0021	0.0023
E	0.0004	0.0004	0.0004	0.0004
TE	0.0007	0.0007	0.0008	0.0008
	C8T28SOI_LLP1_-CNHLSX34_P0	C8T28SOI_LLP1_-CNHLSX34_P4	C8T28SOI_LLP1_-CNHLSX34_P10	C8T28SOI_LLP1_-CNHLSX34_P16
CP	0.0019	0.0020	0.0021	0.0022
E	0.0004	0.0004	0.0004	0.0004
TE	0.0007	0.0007	0.0008	0.0008
	C8T28SOI_LLP1_-CNHLSX38_P0	C8T28SOI_LLP1_-CNHLSX38_P4	C8T28SOI_LLP1_-CNHLSX38_P10	C8T28SOI_LLP1_-CNHLSX38_P16
CP	0.0019	0.0020	0.0021	0.0022
E	0.0004	0.0004	0.0004	0.0004
TE	0.0007	0.0007	0.0008	0.0008
	C8T28SOI_LLP1_-CNHLSX57_P0	C8T28SOI_LLP1_-CNHLSX57_P4	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP	0.0030	0.0032	0.0034	0.0036
E	0.0004	0.0004	0.0004	0.0004
TE	0.0007	0.0007	0.0008	0.0008
	C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP	0.0017	0.0017	0.0018	0.0019
E	0.0003	0.0004	0.0004	0.0004

TE	0.0006	0.0007	0.0007	0.0008
	C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP	0.0020	0.0021	0.0022	0.0023
E	0.0003	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0008
	C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP	0.0021	0.0022	0.0023	0.0024
E	0.0003	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0008
	C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP	0.0021	0.0022	0.0023	0.0024
E	0.0003	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0008
	C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP	0.0021	0.0022	0.0023	0.0024
E	0.0003	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0008
	C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP	0.0029	0.0030	0.0031	0.0033
E	0.0003	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0008
	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP	0.0029	0.0030	0.0032	0.0033
E	0.0003	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0008
	C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP	0.0029	0.0030	0.0032	0.0034
E	0.0003	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0008
	C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP	0.0053	0.0055	0.0058	0.0062
E	0.0003	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LLP1_-CNHLSX10_P0	**C8T28SOI_LLP1_-CNHLSX10_P4**	**C8T28SOI_LLP1_-CNHLSX10_P0**	**C8T28SOI_LLP1_-CNHLSX10_P4**
CP to Q ↓	0.0203	0.0233	1.2511	1.3379
CP to Q ↑	0.0200	0.0224	1.4966	1.6951
	C8T28SOI_LLP1_-CNHLSX10_P10	**C8T28SOI_LLP1_-CNHLSX10_P16**	**C8T28SOI_LLP1_-CNHLSX10_P10**	**C8T28SOI_LLP1_-CNHLSX10_P16**
CP to Q ↓	0.0278	0.0321	1.4627	1.5749
CP to Q ↑	0.0260	0.0294	2.0014	2.2867

	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4
CP to Q ↓	0.0220	0.0254	0.8426	0.9020
CP to Q ↑	0.0220	0.0247	1.0069	1.1400
	C8T28SOI_LLP1_-CNHLSX14_P10	**C8T28SOI_LLP1_-CNHLSX14_P16**	**C8T28SOI_LLP1_-CNHLSX14_P10**	**C8T28SOI_LLP1_-CNHLSX14_P16**
CP to Q ↓	0.0306	0.0354	0.9883	1.0650
CP to Q ↑	0.0288	0.0325	1.3452	1.5379
	C8T28SOI_LLP1_-CNHLSX19_P0	**C8T28SOI_LLP1_-CNHLSX19_P4**	**C8T28SOI_LLP1_-CNHLSX19_P0**	**C8T28SOI_LLP1_-CNHLSX19_P4**
CP to Q ↓	0.0177	0.0203	0.6215	0.6648
CP to Q ↑	0.0177	0.0198	0.7511	0.8488
	C8T28SOI_LLP1_-CNHLSX19_P10	**C8T28SOI_LLP1_-CNHLSX19_P16**	**C8T28SOI_LLP1_-CNHLSX19_P10**	**C8T28SOI_LLP1_-CNHLSX19_P16**
CP to Q ↓	0.0243	0.0281	0.7260	0.7820
CP to Q ↑	0.0230	0.0260	1.0012	1.1435
	C8T28SOI_LLP1_-CNHLSX24_P0	**C8T28SOI_LLP1_-CNHLSX24_P4**	**C8T28SOI_LLP1_-CNHLSX24_P0**	**C8T28SOI_LLP1_-CNHLSX24_P4**
CP to Q ↓	0.0193	0.0222	0.5079	0.5433
CP to Q ↑	0.0193	0.0216	0.6059	0.6849
	C8T28SOI_LLP1_-CNHLSX24_P10	**C8T28SOI_LLP1_-CNHLSX24_P16**	**C8T28SOI_LLP1_-CNHLSX24_P10**	**C8T28SOI_LLP1_-CNHLSX24_P16**
CP to Q ↓	0.0266	0.0308	0.5942	0.6396
CP to Q ↑	0.0252	0.0285	0.8072	0.9228
	C8T28SOI_LLP1_-CNHLSX29_P0	**C8T28SOI_LLP1_-CNHLSX29_P4**	**C8T28SOI_LLP1_-CNHLSX29_P0**	**C8T28SOI_LLP1_-CNHLSX29_P4**
CP to Q ↓	0.0189	0.0218	0.4248	0.4550
CP to Q ↑	0.0197	0.0219	0.5073	0.5735
	C8T28SOI_LLP1_-CNHLSX29_P10	**C8T28SOI_LLP1_-CNHLSX29_P16**	**C8T28SOI_LLP1_-CNHLSX29_P10**	**C8T28SOI_LLP1_-CNHLSX29_P16**
CP to Q ↓	0.0262	0.0303	0.4980	0.5366
CP to Q ↑	0.0254	0.0287	0.6753	0.7704
	C8T28SOI_LLP1_-CNHLSX34_P0	**C8T28SOI_LLP1_-CNHLSX34_P4**	**C8T28SOI_LLP1_-CNHLSX34_P0**	**C8T28SOI_LLP1_-CNHLSX34_P4**
CP to Q ↓	0.0201	0.0233	0.3694	0.3954
CP to Q ↑	0.0210	0.0234	0.4380	0.4943
	C8T28SOI_LLP1_-CNHLSX34_P10	**C8T28SOI_LLP1_-CNHLSX34_P16**	**C8T28SOI_LLP1_-CNHLSX34_P10**	**C8T28SOI_LLP1_-CNHLSX34_P16**
CP to Q ↓	0.0282	0.0325	0.4329	0.4670
CP to Q ↑	0.0273	0.0307	0.5824	0.6642
	C8T28SOI_LLP1_-CNHLSX38_P0	**C8T28SOI_LLP1_-CNHLSX38_P4**	**C8T28SOI_LLP1_-CNHLSX38_P0**	**C8T28SOI_LLP1_-CNHLSX38_P4**
CP to Q ↓	0.0212	0.0246	0.3228	0.3462
CP to Q ↑	0.0221	0.0247	0.3833	0.4331
	C8T28SOI_LLP1_-CNHLSX38_P10	**C8T28SOI_LLP1_-CNHLSX38_P16**	**C8T28SOI_LLP1_-CNHLSX38_P10**	**C8T28SOI_LLP1_-CNHLSX38_P16**
CP to Q ↓	0.0297	0.0343	0.3792	0.4094
CP to Q ↑	0.0289	0.0325	0.5106	0.5828
	C8T28SOI_LLP1_-CNHLSX57_P0	**C8T28SOI_LLP1_-CNHLSX57_P4**	**C8T28SOI_LLP1_-CNHLSX57_P0**	**C8T28SOI_LLP1_-CNHLSX57_P4**
CP to Q ↓	0.0199	0.0229	0.2172	0.2323
CP to Q ↑	0.0205	0.0229	0.2664	0.3001

	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP to Q ↓	0.0276	0.0318	0.2543	0.2739
CP to Q ↑	0.0268	0.0302	0.3525	0.4011
	C8T28SOI_LLP_-CNHLSX4_P0	**C8T28SOI_LLP_-CNHLSX4_P4**	**C8T28SOI_LLP_-CNHLSX4_P0**	**C8T28SOI_LLP_-CNHLSX4_P4**
CP to Q ↓	0.0211	0.0243	3.0444	3.2607
CP to Q ↑	0.0152	0.0174	3.1380	3.5437
	C8T28SOI_LLP_-CNHLSX4_P10	**C8T28SOI_LLP_-CNHLSX4_P16**	**C8T28SOI_LLP_-CNHLSX4_P10**	**C8T28SOI_LLP_-CNHLSX4_P16**
CP to Q ↓	0.0290	0.0334	3.5657	3.8404
CP to Q ↑	0.0206	0.0235	4.1720	4.7627
	C8T28SOI_LLP_-CNHLSX9_P0	**C8T28SOI_LLP_-CNHLSX9_P4**	**C8T28SOI_LLP_-CNHLSX9_P0**	**C8T28SOI_LLP_-CNHLSX9_P4**
CP to Q ↓	0.0194	0.0222	1.3998	1.5012
CP to Q ↑	0.0141	0.0161	1.5433	1.7489
	C8T28SOI_LLP_-CNHLSX9_P10	**C8T28SOI_LLP_-CNHLSX9_P16**	**C8T28SOI_LLP_-CNHLSX9_P10**	**C8T28SOI_LLP_-CNHLSX9_P16**
CP to Q ↓	0.0264	0.0305	1.6413	1.7660
CP to Q ↑	0.0192	0.0220	2.0641	2.3588
	C8T28SOI_LLP_-CNHLSX13_P0	**C8T28SOI_LLP_-CNHLSX13_P4**	**C8T28SOI_LLP_-CNHLSX13_P0**	**C8T28SOI_LLP_-CNHLSX13_P4**
CP to Q ↓	0.0229	0.0265	0.9361	1.0037
CP to Q ↑	0.0172	0.0196	1.0377	1.1749
	C8T28SOI_LLP_-CNHLSX13_P10	**C8T28SOI_LLP_-CNHLSX13_P16**	**C8T28SOI_LLP_-CNHLSX13_P10**	**C8T28SOI_LLP_-CNHLSX13_P16**
CP to Q ↓	0.0319	0.0372	1.0993	1.1842
CP to Q ↑	0.0233	0.0267	1.3882	1.5864
	C8T28SOI_LLP_-CNHLSX17_P0	**C8T28SOI_LLP_-CNHLSX17_P4**	**C8T28SOI_LLP_-CNHLSX17_P0**	**C8T28SOI_LLP_-CNHLSX17_P4**
CP to Q ↓	0.0256	0.0296	0.7190	0.7700
CP to Q ↑	0.0197	0.0224	0.7765	0.8823
	C8T28SOI_LLP_-CNHLSX17_P10	**C8T28SOI_LLP_-CNHLSX17_P16**	**C8T28SOI_LLP_-CNHLSX17_P10**	**C8T28SOI_LLP_-CNHLSX17_P16**
CP to Q ↓	0.0362	0.0419	0.8429	0.9078
CP to Q ↑	0.0268	0.0303	1.0428	1.1933
	C8T28SOI_LLP_-CNHLSX21_P0	**C8T28SOI_LLP_-CNHLSX21_P4**	**C8T28SOI_LLP_-CNHLSX21_P0**	**C8T28SOI_LLP_-CNHLSX21_P4**
CP to Q ↓	0.0281	0.0324	0.5824	0.6249
CP to Q ↑	0.0226	0.0256	0.6337	0.7176
	C8T28SOI_LLP_-CNHLSX21_P10	**C8T28SOI_LLP_-CNHLSX21_P16**	**C8T28SOI_LLP_-CNHLSX21_P10**	**C8T28SOI_LLP_-CNHLSX21_P16**
CP to Q ↓	0.0391	0.0456	0.6849	0.7382
CP to Q ↑	0.0302	0.0344	0.8470	0.9687
	C8T28SOI_LLP_-CNHLSX27_P0	**C8T28SOI_LLP_-CNHLSX27_P4**	**C8T28SOI_LLP_-CNHLSX27_P0**	**C8T28SOI_LLP_-CNHLSX27_P4**
CP to Q ↓	0.0185	0.0211	0.4799	0.5145
CP to Q ↑	0.0153	0.0173	0.4731	0.5357
	C8T28SOI_LLP_-CNHLSX27_P10	**C8T28SOI_LLP_-CNHLSX27_P16**	**C8T28SOI_LLP_-CNHLSX27_P10**	**C8T28SOI_LLP_-CNHLSX27_P16**
CP to Q ↓	0.0254	0.0292	0.5621	0.6053
CP to Q ↑	0.0204	0.0232	0.6322	0.7225

	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4
CP to Q ↓	0.0197	0.0225	0.4241	0.4546
CP to Q ↑	0.0164	0.0186	0.4198	0.4753
	C8T28SOI_LLP_-CNHLSX30_P10	**C8T28SOI_LLP_-CNHLSX30_P16**	**C8T28SOI_LLP_-CNHLSX30_P10**	**C8T28SOI_LLP_-CNHLSX30_P16**
CP to Q ↓	0.0270	0.0312	0.4977	0.5363
CP to Q ↑	0.0220	0.0249	0.5600	0.6395
	C8T28SOI_LLP_-CNHLSX38_P0	**C8T28SOI_LLP_-CNHLSX38_P4**	**C8T28SOI_LLP_-CNHLSX38_P0**	**C8T28SOI_LLP_-CNHLSX38_P4**
CP to Q ↓	0.0220	0.0250	0.3395	0.3642
CP to Q ↑	0.0185	0.0207	0.3385	0.3834
	C8T28SOI_LLP_-CNHLSX38_P10	**C8T28SOI_LLP_-CNHLSX38_P16**	**C8T28SOI_LLP_-CNHLSX38_P10**	**C8T28SOI_LLP_-CNHLSX38_P16**
CP to Q ↓	0.0300	0.0347	0.3990	0.4304
CP to Q ↑	0.0244	0.0276	0.4516	0.5158
	C8T28SOI_LLP_-CNHLSX54_P0	**C8T28SOI_LLP_-CNHLSX54_P4**	**C8T28SOI_LLP_-CNHLSX54_P0**	**C8T28SOI_LLP_-CNHLSX54_P4**
CP to Q ↓	0.0166	0.0189	0.2406	0.2576
CP to Q ↑	0.0155	0.0173	0.2459	0.2780
	C8T28SOI_LLP_-CNHLSX54_P10	**C8T28SOI_LLP_-CNHLSX54_P16**	**C8T28SOI_LLP_-CNHLSX54_P10**	**C8T28SOI_LLP_-CNHLSX54_P16**
CP to Q ↓	0.0227	0.0261	0.2818	0.3033
CP to Q ↑	0.0203	0.0229	0.3270	0.3723

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_-LLP1_-CNHLSX10_P0	C8T28SOI_-LLP1_-CNHLSX10_P4	C8T28SOI_-LLP1_-CNHLSX10_P10	C8T28SOI_-LLP1_-CNHLSX10_P16
CP ↓	min_pulse_width to CP	0.0340	0.0419	0.0511	0.0555
E ↓	hold_rising to CP	0.0081	0.0053	0.0036	-0.0023
E ↑	hold_rising to CP	0.0007	-0.0009	-0.0053	-0.0128
E ↓	setup_rising to CP	0.0197	0.0224	0.0214	0.0268
E ↑	setup_rising to CP	0.0260	0.0304	0.0406	0.0450
TE ↓	hold_rising to CP	0.0107	0.0048	-0.0000	0.0004
TE ↑	hold_rising to CP	0.0018	-0.0004	-0.0111	-0.0154
TE ↓	setup_rising to CP	0.0172	0.0193	0.0247	0.0268
TE ↑	setup_rising to CP	0.0288	0.0304	0.0402	0.0472
		C8T28SOI_-LLP1_-CNHLSX14_P0	C8T28SOI_-LLP1_-CNHLSX14_P4	C8T28SOI_-LLP1_-CNHLSX14_P10	C8T28SOI_-LLP1_-CNHLSX14_P16
CP ↓	min_pulse_width to CP	0.0342	0.0419	0.0511	0.0557
E ↓	hold_rising to CP	0.0101	0.0080	0.0026	0.0030
E ↑	hold_rising to CP	0.0013	-0.0009	-0.0053	-0.0128
E ↓	setup_rising to CP	0.0165	0.0197	0.0224	0.0272

E ↑	setup_rising to CP	0.0292	0.0304	0.0406	0.0477
TE ↓	hold_rising to CP	0.0103	0.0107	0.0048	-0.0001
TE ↑	hold_rising to CP	0.0018	-0.0004	-0.0111	-0.0154
TE ↓	setup_rising to CP	0.0144	0.0199	0.0193	0.0247
TE ↑	setup_rising to CP	0.0288	0.0363	0.0402	0.0472
		C8T28SOI_-LLP1_-CNHLSX19_P0	C8T28SOI_-LLP1_-CNHLSX19_P4	C8T28SOI_-LLP1_-CNHLSX19_P10	C8T28SOI_-LLP1_-CNHLSX19_P16
CP ↓	min_pulse_width to CP	0.0419	0.0477	0.0589	0.0681
E ↓	hold_rising to CP	0.0032	0.0004	-0.0013	-0.0071
E ↑	hold_rising to CP	0.0017	-0.0032	-0.0107	-0.0177
E ↓	setup_rising to CP	0.0214	0.0246	0.0263	0.0317
E ↑	setup_rising to CP	0.0282	0.0357	0.0460	0.0525
TE ↓	hold_rising to CP	0.0058	-0.0000	-0.0049	-0.0040
TE ↑	hold_rising to CP	-0.0008	-0.0057	-0.0128	-0.0208
TE ↓	setup_rising to CP	0.0225	0.0247	0.0296	0.0349
TE ↑	setup_rising to CP	0.0308	0.0353	0.0450	0.0521
		C8T28SOI_-LLP1_-CNHLSX24_P0	C8T28SOI_-LLP1_-CNHLSX24_P4	C8T28SOI_-LLP1_-CNHLSX24_P10	C8T28SOI_-LLP1_-CNHLSX24_P16
CP ↓	min_pulse_width to CP	0.0433	0.0477	0.0589	0.0681
E ↓	hold_rising to CP	0.0053	0.0036	-0.0023	-0.0071
E ↑	hold_rising to CP	0.0017	-0.0058	-0.0107	-0.0177
E ↓	setup_rising to CP	0.0214	0.0246	0.0263	0.0317
E ↑	setup_rising to CP	0.0282	0.0357	0.0455	0.0525
TE ↓	hold_rising to CP	0.0054	0.0026	0.0009	-0.0045
TE ↑	hold_rising to CP	-0.0008	-0.0057	-0.0128	-0.0203
TE ↓	setup_rising to CP	0.0193	0.0247	0.0300	0.0290
TE ↑	setup_rising to CP	0.0308	0.0353	0.0450	0.0553
		C8T28SOI_-LLP1_-CNHLSX29_P0	C8T28SOI_-LLP1_-CNHLSX29_P4	C8T28SOI_-LLP1_-CNHLSX29_P10	C8T28SOI_-LLP1_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0478	0.0556	0.0681	0.0772
E ↓	hold_rising to CP	0.0032	0.0004	-0.0013	-0.0067
E ↑	hold_rising to CP	-0.0036	-0.0081	-0.0151	-0.0253
E ↓	setup_rising to CP	0.0214	0.0272	0.0321	0.0338
E ↑	setup_rising to CP	0.0331	0.0406	0.0499	0.0623

TE ↓	hold_rising to CP	0.0058	-0.0001	-0.0049	-0.0066
TE ↑	hold_rising to CP	-0.0057	-0.0106	-0.0209	-0.0274
TE ↓	setup_rising to CP	0.0225	0.0247	0.0296	0.0344
TE ↑	setup_rising to CP	0.0357	0.0401	0.0525	0.0618
		C8T28SOI_-LLP1_-CNHLSX34_P0	C8T28SOI_-LLP1_-CNHLSX34_P4	C8T28SOI_-LLP1_-CNHLSX34_P10	C8T28SOI_-LLP1_-CNHLSX34_P16
CP ↓	min_pulse_width to CP	0.0478	0.0556	0.0681	0.0772
E ↓	hold_rising to CP	0.0053	0.0036	-0.0023	-0.0072
E ↑	hold_rising to CP	-0.0036	-0.0081	-0.0151	-0.0253
E ↓	setup_rising to CP	0.0214	0.0246	0.0263	0.0317
E ↑	setup_rising to CP	0.0331	0.0406	0.0499	0.0623
TE ↓	hold_rising to CP	0.0054	-0.0001	-0.0017	-0.0045
TE ↑	hold_rising to CP	-0.0057	-0.0106	-0.0176	-0.0274
TE ↓	setup_rising to CP	0.0193	0.0247	0.0296	0.0349
TE ↑	setup_rising to CP	0.0357	0.0401	0.0521	0.0618
		C8T28SOI_-LLP1_-CNHLSX38_P0	C8T28SOI_-LLP1_-CNHLSX38_P4	C8T28SOI_-LLP1_-CNHLSX38_P10	C8T28SOI_-LLP1_-CNHLSX38_P16
CP ↓	min_pulse_width to CP	0.0478	0.0556	0.0681	0.0772
E ↓	hold_rising to CP	0.0052	0.0032	-0.0023	-0.0072
E ↑	hold_rising to CP	-0.0036	-0.0081	-0.0151	-0.0253
E ↓	setup_rising to CP	0.0218	0.0246	0.0263	0.0317
E ↑	setup_rising to CP	0.0331	0.0402	0.0499	0.0623
TE ↓	hold_rising to CP	0.0048	0.0026	0.0009	-0.0045
TE ↑	hold_rising to CP	-0.0057	-0.0106	-0.0176	-0.0274
TE ↓	setup_rising to CP	0.0193	0.0247	0.0300	0.0317
TE ↑	setup_rising to CP	0.0353	0.0428	0.0553	0.0645
		C8T28SOI_-LLP1_-CNHLSX57_P0	C8T28SOI_-LLP1_-CNHLSX57_P4	C8T28SOI_-LLP1_-CNHLSX57_P10	C8T28SOI_-LLP1_-CNHLSX57_P16
CP ↓	min_pulse_width to CP	0.0524	0.0602	0.0740	0.0865
E ↓	hold_rising to CP	0.0036	-0.0023	-0.0071	-0.0062
E ↑	hold_rising to CP	-0.0032	-0.0107	-0.0204	-0.0307
E ↓	setup_rising to CP	0.0246	0.0263	0.0317	0.0370
E ↑	setup_rising to CP	0.0380	0.0454	0.0548	0.0694
TE ↓	hold_rising to CP	0.0026	0.0009	-0.0049	-0.0098
TE ↑	hold_rising to CP	-0.0057	-0.0106	-0.0203	-0.0301

TE ↓	setup_rising to CP	0.0247	0.0242	0.0290	0.0339
TE ↑	setup_rising to CP	0.0380	0.0450	0.0602	0.0720
		C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP ↓	min_pulse_width to CP	0.0255	0.0286	0.0332	0.0360
E ↓	hold_rising to CP	-0.0035	-0.0052	-0.0101	-0.0155
E ↑	hold_rising to CP	0.0084	0.0058	0.0009	-0.0017
E ↓	setup_rising to CP	0.0309	0.0300	0.0375	0.0424
E ↑	setup_rising to CP	0.0190	0.0249	0.0265	0.0314
TE ↓	hold_rising to CP	-0.0035	-0.0030	-0.0105	-0.0154
TE ↑	hold_rising to CP	0.0058	0.0058	0.0010	-0.0013
TE ↓	setup_rising to CP	0.0284	0.0305	0.0350	0.0398
TE ↑	setup_rising to CP	0.0190	0.0239	0.0293	0.0313
		C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP ↓	min_pulse_width to CP	0.0232	0.0254	0.0299	0.0337
E ↓	hold_rising to CP	-0.0003	-0.0061	-0.0106	-0.0155
E ↑	hold_rising to CP	0.0079	0.0058	0.0058	0.0010
E ↓	setup_rising to CP	0.0251	0.0304	0.0354	0.0403
E ↑	setup_rising to CP	0.0168	0.0190	0.0239	0.0293
TE ↓	hold_rising to CP	-0.0039	-0.0030	-0.0078	-0.0133
TE ↑	hold_rising to CP	0.0058	0.0058	0.0036	-0.0017
TE ↓	setup_rising to CP	0.0288	0.0279	0.0354	0.0403
TE ↑	setup_rising to CP	0.0190	0.0217	0.0265	0.0314
		C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP ↓	min_pulse_width to CP	0.0238	0.0253	0.0315	0.0355
E ↓	hold_rising to CP	-0.0003	-0.0061	-0.0106	-0.0155
E ↑	hold_rising to CP	0.0079	0.0058	0.0032	0.0010
E ↓	setup_rising to CP	0.0251	0.0304	0.0354	0.0403
E ↑	setup_rising to CP	0.0168	0.0190	0.0239	0.0293
TE ↓	hold_rising to CP	-0.0007	-0.0030	-0.0078	-0.0133
TE ↑	hold_rising to CP	0.0058	0.0058	0.0036	-0.0017
TE ↓	setup_rising to CP	0.0288	0.0279	0.0354	0.0403
TE ↑	setup_rising to CP	0.0190	0.0217	0.0265	0.0314

		C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP ↓	min_pulse_width to CP	0.0255	0.0253	0.0322	0.0361
E ↓	hold_rising to CP	-0.0003	-0.0061	-0.0106	-0.0155
E ↑	hold_rising to CP	0.0079	0.0058	0.0058	0.0010
E ↓	setup_rising to CP	0.0251	0.0304	0.0354	0.0403
E ↑	setup_rising to CP	0.0168	0.0190	0.0239	0.0293
TE ↓	hold_rising to CP	-0.0039	-0.0030	-0.0078	-0.0133
TE ↑	hold_rising to CP	0.0058	0.0058	0.0036	-0.0017
TE ↓	setup_rising to CP	0.0288	0.0279	0.0354	0.0403
TE ↑	setup_rising to CP	0.0190	0.0217	0.0265	0.0314
		C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP ↓	min_pulse_width to CP	0.0255	0.0277	0.0322	0.0361
E ↓	hold_rising to CP	-0.0003	-0.0057	-0.0106	-0.0155
E ↑	hold_rising to CP	0.0079	0.0058	0.0058	0.0010
E ↓	setup_rising to CP	0.0251	0.0304	0.0354	0.0403
E ↑	setup_rising to CP	0.0168	0.0190	0.0239	0.0293
TE ↓	hold_rising to CP	-0.0007	-0.0030	-0.0078	-0.0133
TE ↑	hold_rising to CP	0.0058	0.0058	0.0036	-0.0017
TE ↓	setup_rising to CP	0.0288	0.0279	0.0354	0.0403
TE ↑	setup_rising to CP	0.0190	0.0217	0.0265	0.0314
		C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP ↓	min_pulse_width to CP	0.0255	0.0294	0.0340	0.0385
E ↓	hold_rising to CP	-0.0052	-0.0110	-0.0155	-0.0204
E ↑	hold_rising to CP	0.0057	0.0058	0.0009	-0.0017
E ↓	setup_rising to CP	0.0304	0.0358	0.0403	0.0478
E ↑	setup_rising to CP	0.0190	0.0239	0.0293	0.0342
TE ↓	hold_rising to CP	-0.0030	-0.0084	-0.0133	-0.0208
TE ↑	hold_rising to CP	0.0058	0.0058	0.0010	-0.0013
TE ↓	setup_rising to CP	0.0305	0.0328	0.0403	0.0451
TE ↑	setup_rising to CP	0.0190	0.0239	0.0314	0.0363
		C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP ↓	min_pulse_width to CP	0.0256	0.0294	0.0340	0.0385
E ↓	hold_rising to CP	-0.0052	-0.0110	-0.0155	-0.0204

E ↑	hold_rising to CP	0.0057	0.0058	0.0009	-0.0017
E ↓	setup_rising to CP	0.0304	0.0358	0.0403	0.0478
E ↑	setup_rising to CP	0.0190	0.0239	0.0293	0.0342
TE ↓	hold_rising to CP	-0.0030	-0.0084	-0.0133	-0.0208
TE ↑	hold_rising to CP	0.0058	0.0032	0.0010	-0.0013
TE ↓	setup_rising to CP	0.0305	0.0333	0.0403	0.0451
TE ↑	setup_rising to CP	0.0190	0.0239	0.0314	0.0363
		C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP ↓	min_pulse_width to CP	0.0255	0.0294	0.0339	0.0384
E ↓	hold_rising to CP	-0.0052	-0.0110	-0.0155	-0.0204
E ↑	hold_rising to CP	0.0057	0.0058	0.0009	-0.0017
E ↓	setup_rising to CP	0.0304	0.0358	0.0403	0.0478
E ↑	setup_rising to CP	0.0190	0.0239	0.0293	0.0342
TE ↓	hold_rising to CP	-0.0030	-0.0084	-0.0133	-0.0181
TE ↑	hold_rising to CP	0.0058	0.0032	0.0010	-0.0013
TE ↓	setup_rising to CP	0.0305	0.0328	0.0403	0.0451
TE ↑	setup_rising to CP	0.0223	0.0239	0.0314	0.0363
		C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP ↓	min_pulse_width to CP	0.0256	0.0295	0.0347	0.0393
E ↓	hold_rising to CP	-0.0052	-0.0106	-0.0155	-0.0230
E ↑	hold_rising to CP	0.0084	0.0058	0.0036	0.0010
E ↓	setup_rising to CP	0.0300	0.0354	0.0424	0.0473
E ↑	setup_rising to CP	0.0190	0.0244	0.0288	0.0363
TE ↓	hold_rising to CP	-0.0056	-0.0078	-0.0154	-0.0202
TE ↑	hold_rising to CP	0.0058	0.0058	0.0010	-0.0013
TE ↓	setup_rising to CP	0.0337	0.0354	0.0435	0.0479
TE ↑	setup_rising to CP	0.0190	0.0239	0.0314	0.0363

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LLP1_CNHLSX10_P0	1.152e-03	1.000e-20
C8T28SOI_LLP1_CNHLSX10_P4	2.996e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX10_P10	7.195e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX10_P16	2.995e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX14_P0	1.392e-03	1.000e-20
C8T28SOI_LLP1_CNHLSX14_P4	3.600e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX14_P10	8.560e-05	1.000e-20

C8T28SOI_LLP1_CNHLSX14_P16	3.531e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P0	1.818e-03	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P4	4.711e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P10	1.119e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P16	4.601e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P0	2.047e-03	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P4	5.293e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P10	1.252e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P16	5.123e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P0	2.490e-03	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P4	6.402e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P10	1.497e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P16	6.068e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P0	2.719e-03	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P4	6.985e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P10	1.630e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P16	6.591e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P0	2.949e-03	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P4	7.568e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P10	1.763e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P16	7.114e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P0	4.044e-03	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P4	1.042e-03	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P10	2.439e-04	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P16	9.865e-05	1.000e-20
C8T28SOI_LLP_CNHLSX4_P0	9.482e-04	1.000e-20
C8T28SOI_LLP_CNHLSX4_P4	2.444e-04	1.000e-20
C8T28SOI_LLP_CNHLSX4_P10	5.870e-05	1.000e-20
C8T28SOI_LLP_CNHLSX4_P16	2.441e-05	1.000e-20
C8T28SOI_LLP_CNHLSX9_P0	1.310e-03	1.000e-20
C8T28SOI_LLP_CNHLSX9_P4	3.340e-04	1.000e-20
C8T28SOI_LLP_CNHLSX9_P10	7.865e-05	1.000e-20
C8T28SOI_LLP_CNHLSX9_P16	3.219e-05	1.000e-20
C8T28SOI_LLP_CNHLSX13_P0	1.520e-03	1.000e-20
C8T28SOI_LLP_CNHLSX13_P4	3.876e-04	1.000e-20
C8T28SOI_LLP_CNHLSX13_P10	9.088e-05	1.000e-20
C8T28SOI_LLP_CNHLSX13_P16	3.698e-05	1.000e-20
C8T28SOI_LLP_CNHLSX17_P0	1.771e-03	1.000e-20
C8T28SOI_LLP_CNHLSX17_P4	4.481e-04	1.000e-20
C8T28SOI_LLP_CNHLSX17_P10	1.039e-04	1.000e-20
C8T28SOI_LLP_CNHLSX17_P16	4.196e-05	1.000e-20
C8T28SOI_LLP_CNHLSX21_P0	1.916e-03	1.000e-20
C8T28SOI_LLP_CNHLSX21_P4	4.902e-04	1.000e-20
C8T28SOI_LLP_CNHLSX21_P10	1.147e-04	1.000e-20
C8T28SOI_LLP_CNHLSX21_P16	4.642e-05	1.000e-20
C8T28SOI_LLP_CNHLSX27_P0	2.701e-03	1.000e-20
C8T28SOI_LLP_CNHLSX27_P4	6.783e-04	1.000e-20
C8T28SOI_LLP_CNHLSX27_P10	1.556e-04	1.000e-20
C8T28SOI_LLP_CNHLSX27_P16	6.240e-05	1.000e-20
C8T28SOI_LLP_CNHLSX30_P0	2.944e-03	1.000e-20
C8T28SOI_LLP_CNHLSX30_P4	7.389e-04	1.000e-20
C8T28SOI_LLP_CNHLSX30_P10	1.694e-04	1.000e-20

C8T28SOI_LLP_CNHLSX30_P16	6.779e-05	1.000e-20
C8T28SOI_LLP_CNHLSX38_P0	3.397e-03	1.000e-20
C8T28SOI_LLP_CNHLSX38_P4	8.487e-04	1.000e-20
C8T28SOI_LLP_CNHLSX38_P10	1.933e-04	1.000e-20
C8T28SOI_LLP_CNHLSX38_P16	7.694e-05	1.000e-20
C8T28SOI_LLP_CNHLSX54_P0	4.948e-03	1.000e-20
C8T28SOI_LLP_CNHLSX54_P4	1.239e-03	1.000e-20
C8T28SOI_LLP_CNHLSX54_P10	2.818e-04	1.000e-20
C8T28SOI_LLP_CNHLSX54_P16	1.120e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LLP1_-CNHLSX10_P0	C8T28SOI_LLP1_-CNHLSX10_P4	C8T28SOI_LLP1_-CNHLSX10_P10	C8T28SOI_LLP1_-CNHLSX10_P16
CP (output stable)	1.931e-03	1.878e-03	1.895e-03	1.947e-03
E (output stable)	1.620e-03	1.485e-03	1.422e-03	1.421e-03
TE (output stable)	1.695e-03	1.558e-03	1.510e-03	1.525e-03
CP to Q	6.083e-03	5.552e-03	5.280e-03	5.256e-03
	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P10	C8T28SOI_LLP1_-CNHLSX14_P16
CP (output stable)	1.934e-03	1.880e-03	1.900e-03	1.951e-03
E (output stable)	1.622e-03	1.485e-03	1.422e-03	1.421e-03
TE (output stable)	1.697e-03	1.559e-03	1.510e-03	1.524e-03
CP to Q	8.086e-03	7.322e-03	6.896e-03	6.820e-03
	C8T28SOI_LLP1_-CNHLSX19_P0	C8T28SOI_LLP1_-CNHLSX19_P4	C8T28SOI_LLP1_-CNHLSX19_P10	C8T28SOI_LLP1_-CNHLSX19_P16
CP (output stable)	2.654e-03	2.637e-03	2.703e-03	2.808e-03
E (output stable)	1.740e-03	1.609e-03	1.553e-03	1.560e-03
TE (output stable)	1.814e-03	1.682e-03	1.641e-03	1.664e-03
CP to Q	1.019e-02	9.139e-03	8.575e-03	8.461e-03
	C8T28SOI_LLP1_-CNHLSX24_P0	C8T28SOI_LLP1_-CNHLSX24_P4	C8T28SOI_LLP1_-CNHLSX24_P10	C8T28SOI_LLP1_-CNHLSX24_P16
CP (output stable)	2.676e-03	2.657e-03	2.721e-03	2.829e-03
E (output stable)	1.740e-03	1.610e-03	1.554e-03	1.562e-03
TE (output stable)	1.816e-03	1.684e-03	1.642e-03	1.665e-03
CP to Q	1.230e-02	1.107e-02	1.039e-02	1.026e-02
	C8T28SOI_LLP1_-CNHLSX29_P0	C8T28SOI_LLP1_-CNHLSX29_P4	C8T28SOI_LLP1_-CNHLSX29_P10	C8T28SOI_LLP1_-CNHLSX29_P16
CP (output stable)	2.949e-03	2.939e-03	3.033e-03	3.163e-03
E (output stable)	1.850e-03	1.720e-03	1.674e-03	1.691e-03
TE (output stable)	1.922e-03	1.793e-03	1.761e-03	1.794e-03
CP to Q	1.429e-02	1.282e-02	1.201e-02	1.185e-02
	C8T28SOI_LLP1_-CNHLSX34_P0	C8T28SOI_LLP1_-CNHLSX34_P4	C8T28SOI_LLP1_-CNHLSX34_P10	C8T28SOI_LLP1_-CNHLSX34_P16
CP (output stable)	2.953e-03	2.943e-03	3.007e-03	3.163e-03
E (output stable)	1.851e-03	1.720e-03	1.674e-03	1.691e-03
TE (output stable)	1.924e-03	1.793e-03	1.761e-03	1.794e-03
CP to Q	1.646e-02	1.479e-02	1.401e-02	1.367e-02
	C8T28SOI_LLP1_-CNHLSX38_P0	C8T28SOI_LLP1_-CNHLSX38_P4	C8T28SOI_LLP1_-CNHLSX38_P10	C8T28SOI_LLP1_-CNHLSX38_P16
CP (output stable)	2.953e-03	2.943e-03	3.018e-03	3.167e-03
E (output stable)	1.852e-03	1.721e-03	1.675e-03	1.692e-03
TE (output stable)	1.925e-03	1.794e-03	1.762e-03	1.795e-03

CP to Q	1.877e-02	1.685e-02	1.591e-02	1.546e-02
	C8T28SOI_LLP1_-CNHLSX57_P0	C8T28SOI_LLP1_-CNHLSX57_P4	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP (output stable)	3.752e-03	3.783e-03	3.912e-03	4.134e-03
E (output stable)	1.954e-03	1.824e-03	1.783e-03	1.806e-03
TE (output stable)	2.024e-03	1.898e-03	1.872e-03	1.910e-03
CP to Q	2.717e-02	2.433e-02	2.283e-02	2.232e-02
	C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP (output stable)	2.848e-03	2.653e-03	2.593e-03	2.625e-03
E (output stable)	1.612e-03	1.462e-03	1.371e-03	1.346e-03
TE (output stable)	1.695e-03	1.544e-03	1.464e-03	1.453e-03
CP to Q	4.342e-03	3.853e-03	3.586e-03	3.517e-03
	C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP (output stable)	2.955e-03	2.770e-03	2.729e-03	2.771e-03
E (output stable)	1.562e-03	1.419e-03	1.334e-03	1.312e-03
TE (output stable)	1.647e-03	1.502e-03	1.427e-03	1.421e-03
CP to Q	6.119e-03	5.397e-03	4.995e-03	4.889e-03
	C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP (output stable)	3.000e-03	2.821e-03	2.779e-03	2.826e-03
E (output stable)	1.568e-03	1.426e-03	1.343e-03	1.322e-03
TE (output stable)	1.653e-03	1.509e-03	1.437e-03	1.432e-03
CP to Q	8.172e-03	7.266e-03	6.764e-03	6.644e-03
	C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP (output stable)	3.004e-03	2.823e-03	2.778e-03	2.830e-03
E (output stable)	1.567e-03	1.426e-03	1.343e-03	1.322e-03
TE (output stable)	1.653e-03	1.509e-03	1.437e-03	1.432e-03
CP to Q	1.044e-02	9.281e-03	8.684e-03	8.406e-03
	C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP (output stable)	3.002e-03	2.820e-03	2.782e-03	2.825e-03
E (output stable)	1.568e-03	1.427e-03	1.343e-03	1.322e-03
TE (output stable)	1.652e-03	1.510e-03	1.437e-03	1.432e-03
CP to Q	1.316e-02	1.168e-02	1.081e-02	1.053e-02
	C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP (output stable)	3.928e-03	3.785e-03	3.804e-03	3.949e-03
E (output stable)	1.719e-03	1.580e-03	1.506e-03	1.493e-03
TE (output stable)	1.805e-03	1.663e-03	1.600e-03	1.603e-03
CP to Q	1.478e-02	1.302e-02	1.210e-02	1.178e-02
	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP (output stable)	3.916e-03	3.775e-03	3.809e-03	3.940e-03
E (output stable)	1.720e-03	1.579e-03	1.505e-03	1.492e-03
TE (output stable)	1.803e-03	1.662e-03	1.599e-03	1.602e-03
CP to Q	1.667e-02	1.473e-02	1.375e-02	1.336e-02
	C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP (output stable)	3.924e-03	3.780e-03	3.824e-03	3.942e-03
E (output stable)	1.717e-03	1.578e-03	1.504e-03	1.491e-03

TE (output stable)	1.804e-03	1.661e-03	1.598e-03	1.601e-03
CP to Q	2.084e-02	1.819e-02	1.699e-02	1.650e-02
	C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP (output stable)	5.624e-03	5.568e-03	5.714e-03	6.005e-03
E (output stable)	1.820e-03	1.698e-03	1.645e-03	1.650e-03
TE (output stable)	1.907e-03	1.781e-03	1.739e-03	1.760e-03
CP to Q	2.778e-02	2.419e-02	2.246e-02	2.169e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOI_LLP1_-CNHLSX10_P0	C8T28SOI_LLP1_-CNHLSX10_P4	C8T28SOI_LLP1_-CNHLSX10_P10	C8T28SOI_LLP1_-CNHLSX10_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P10	C8T28SOI_LLP1_-CNHLSX14_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX19_P0	C8T28SOI_LLP1_-CNHLSX19_P4	C8T28SOI_LLP1_-CNHLSX19_P10	C8T28SOI_LLP1_-CNHLSX19_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX24_P0	C8T28SOI_LLP1_-CNHLSX24_P4	C8T28SOI_LLP1_-CNHLSX24_P10	C8T28SOI_LLP1_-CNHLSX24_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX29_P0	C8T28SOI_LLP1_-CNHLSX29_P4	C8T28SOI_LLP1_-CNHLSX29_P10	C8T28SOI_LLP1_-CNHLSX29_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX34_P0	C8T28SOI_LLP1_-CNHLSX34_P4	C8T28SOI_LLP1_-CNHLSX34_P10	C8T28SOI_LLP1_-CNHLSX34_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX38_P0	C8T28SOI_LLP1_-CNHLSX38_P4	C8T28SOI_LLP1_-CNHLSX38_P10	C8T28SOI_LLP1_-CNHLSX38_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

	C8T28SOI_LLP1_-CNHLSX57_P0	C8T28SOI_LLP1_-CNHLSX57_P4	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

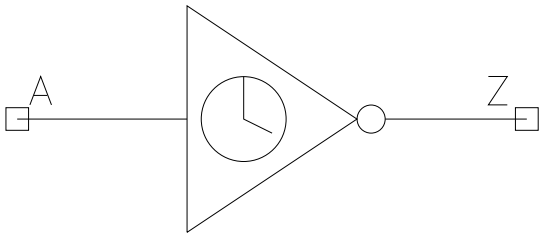
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNIV

Cell Description

Inverter with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_CNIVX2_P0	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX2_P4	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX2_-P10	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX2_-P16	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_P0	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_P4	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_-P10	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_-P16	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX9_P0	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX9_P4	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX9_-P10	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX9_-P16	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX14_-P0	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX14_-P4	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX14_-P10	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX14_-P16	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX18_-P0	0.800	0.680	0.5440
C8T28SOI_LL_CNIVX18_-P4	0.800	0.680	0.5440
C8T28SOI_LL_CNIVX18_-P10	0.800	0.680	0.5440
C8T28SOI_LL_CNIVX18_-P16	0.800	0.680	0.5440

C8T28SOI_LL_CNIVX22_P0	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX22_P4	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX22_P10	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX22_P16	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX27_P0	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX27_P4	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX27_P10	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX27_P16	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX32_P0	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX32_P4	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX32_P10	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX32_P16	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX37_P0	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX37_P4	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX37_P10	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX37_P16	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX74_P0	0.800	2.312	1.8496
C8T28SOI_LL_CNIVX74_P4	0.800	2.312	1.8496
C8T28SOI_LL_CNIVX74_P10	0.800	2.312	1.8496
C8T28SOI_LL_CNIVX74_P16	0.800	2.312	1.8496
C8T28SOIDV_LL_CNIVX18_P0	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX18_P4	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX18_P10	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX18_P16	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX28_P0	1.600	0.544	0.8704
C8T28SOIDV_LL_CNIVX28_P4	1.600	0.544	0.8704

C8T28SOIDV_LL_-CNIVX28_P10	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNIVX28_P16	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNIVX37_P0	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX37_P4	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX37_P10	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX37_P16	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX55_P0	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX55_P4	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX55_P10	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX55_P16	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX74_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNIVX74_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNIVX74_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNIVX74_P16	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_-CNIVX2_P0	C8T28SOI_LL_-CNIVX2_P4	C8T28SOI_LL_-CNIVX2_P10	C8T28SOI_LL_-CNIVX2_P16
A	0.0004	0.0004	0.0004	0.0005
	C8T28SOI_LL_-CNIVX4_P0	C8T28SOI_LL_-CNIVX4_P4	C8T28SOI_LL_-CNIVX4_P10	C8T28SOI_LL_-CNIVX4_P16
A	0.0006	0.0006	0.0006	0.0007
	C8T28SOI_LL_-CNIVX9_P0	C8T28SOI_LL_-CNIVX9_P4	C8T28SOI_LL_-CNIVX9_P10	C8T28SOI_LL_-CNIVX9_P16
A	0.0011	0.0011	0.0012	0.0013
	C8T28SOI_LL_-CNIVX14_P0	C8T28SOI_LL_-CNIVX14_P4	C8T28SOI_LL_-CNIVX14_P10	C8T28SOI_LL_-CNIVX14_P16
A	0.0016	0.0017	0.0018	0.0019
	C8T28SOI_LL_-CNIVX18_P0	C8T28SOI_LL_-CNIVX18_P4	C8T28SOI_LL_-CNIVX18_P10	C8T28SOI_LL_-CNIVX18_P16
A	0.0021	0.0022	0.0023	0.0025
	C8T28SOI_LL_-CNIVX22_P0	C8T28SOI_LL_-CNIVX22_P4	C8T28SOI_LL_-CNIVX22_P10	C8T28SOI_LL_-CNIVX22_P16
A	0.0027	0.0027	0.0029	0.0031

	C8T28SOI_LL_-CNIVX27_P0	C8T28SOI_LL_-CNIVX27_P4	C8T28SOI_LL_-CNIVX27_P10	C8T28SOI_LL_-CNIVX27_P16
A	0.0032	0.0033	0.0035	0.0037
	C8T28SOI_LL_-CNIVX32_P0	C8T28SOI_LL_-CNIVX32_P4	C8T28SOI_LL_-CNIVX32_P10	C8T28SOI_LL_-CNIVX32_P16
A	0.0038	0.0039	0.0041	0.0044
	C8T28SOI_LL_-CNIVX37_P0	C8T28SOI_LL_-CNIVX37_P4	C8T28SOI_LL_-CNIVX37_P10	C8T28SOI_LL_-CNIVX37_P16
A	0.0043	0.0044	0.0047	0.0049
	C8T28SOI_LL_-CNIVX74_P0	C8T28SOI_LL_-CNIVX74_P4	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A	0.0088	0.0092	0.0096	0.0103
	C8T28SOIDV_LL_-CNIVX18_P0	C8T28SOIDV_LL_-CNIVX18_P4	C8T28SOIDV_LL_-CNIVX18_P10	C8T28SOIDV_LL_-CNIVX18_P16
A	0.0021	0.0022	0.0023	0.0024
	C8T28SOIDV_LL_-CNIVX28_P0	C8T28SOIDV_LL_-CNIVX28_P4	C8T28SOIDV_LL_-CNIVX28_P10	C8T28SOIDV_LL_-CNIVX28_P16
A	0.0031	0.0032	0.0035	0.0037
	C8T28SOIDV_LL_-CNIVX37_P0	C8T28SOIDV_LL_-CNIVX37_P4	C8T28SOIDV_LL_-CNIVX37_P10	C8T28SOIDV_LL_-CNIVX37_P16
A	0.0041	0.0043	0.0045	0.0048
	C8T28SOIDV_LL_-CNIVX55_P0	C8T28SOIDV_LL_-CNIVX55_P4	C8T28SOIDV_LL_-CNIVX55_P10	C8T28SOIDV_LL_-CNIVX55_P16
A	0.0063	0.0065	0.0069	0.0074
	C8T28SOIDV_LL_-CNIVX74_P0	C8T28SOIDV_LL_-CNIVX74_P4	C8T28SOIDV_LL_-CNIVX74_P10	C8T28SOIDV_LL_-CNIVX74_P16
A	0.0087	0.0090	0.0095	0.0101

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-CNIVX2_P0	**C8T28SOI_LL_-CNIVX2_P4**	**C8T28SOI_LL_-CNIVX2_P0**	**C8T28SOI_LL_-CNIVX2_P4**
A to Z ↓	0.0043	0.0049	5.0731	5.4129
A to Z ↑	0.0076	0.0087	5.3479	6.0306
	C8T28SOI_LL_-CNIVX2_P10	**C8T28SOI_LL_-CNIVX2_P16**	**C8T28SOI_LL_-CNIVX2_P10**	**C8T28SOI_LL_-CNIVX2_P16**
A to Z ↓	0.0060	0.0068	5.8665	6.2714
A to Z ↑	0.0101	0.0113	7.0807	8.0928
	C8T28SOI_LL_-CNIVX4_P0	**C8T28SOI_LL_-CNIVX4_P4**	**C8T28SOI_LL_-CNIVX4_P0**	**C8T28SOI_LL_-CNIVX4_P4**
A to Z ↓	0.0030	0.0037	2.7354	2.9154
A to Z ↑	0.0068	0.0077	3.3954	3.8375
	C8T28SOI_LL_-CNIVX4_P10	**C8T28SOI_LL_-CNIVX4_P16**	**C8T28SOI_LL_-CNIVX4_P10**	**C8T28SOI_LL_-CNIVX4_P16**
A to Z ↓	0.0046	0.0053	3.1650	3.3849
A to Z ↑	0.0089	0.0099	4.5032	5.1272
	C8T28SOI_LL_-CNIVX9_P0	**C8T28SOI_LL_-CNIVX9_P4**	**C8T28SOI_LL_-CNIVX9_P0**	**C8T28SOI_LL_-CNIVX9_P4**
A to Z ↓	0.0024	0.0030	1.3186	1.4057
A to Z ↑	0.0056	0.0064	1.5666	1.7689
	C8T28SOI_LL_-CNIVX9_P10	**C8T28SOI_LL_-CNIVX9_P16**	**C8T28SOI_LL_-CNIVX9_P10**	**C8T28SOI_LL_-CNIVX9_P16**
A to Z ↓	0.0037	0.0044	1.5279	1.6335

A to Z ↑	0.0074	0.0083	2.0738	2.3609
	C8T28SOI_LL_-CNIVX14_P0	**C8T28SOI_LL_-CNIVX14_P4**	**C8T28SOI_LL_-CNIVX14_P0**	**C8T28SOI_LL_-CNIVX14_P4**
A to Z ↓	0.0027	0.0033	0.8905	0.9493
A to Z ↑	0.0057	0.0065	1.0676	1.2052
	C8T28SOI_LL_-CNIVX14_P10	**C8T28SOI_LL_-CNIVX14_P16**	**C8T28SOI_LL_-CNIVX14_P10**	**C8T28SOI_LL_-CNIVX14_P16**
A to Z ↓	0.0040	0.0047	1.0317	1.1031
A to Z ↑	0.0076	0.0085	1.4098	1.6043
	C8T28SOI_LL_-CNIVX18_P0	**C8T28SOI_LL_-CNIVX18_P4**	**C8T28SOI_LL_-CNIVX18_P0**	**C8T28SOI_LL_-CNIVX18_P4**
A to Z ↓	0.0031	0.0036	0.6998	0.7478
A to Z ↑	0.0058	0.0066	0.8103	0.9129
	C8T28SOI_LL_-CNIVX18_P10	**C8T28SOI_LL_-CNIVX18_P16**	**C8T28SOI_LL_-CNIVX18_P10**	**C8T28SOI_LL_-CNIVX18_P16**
A to Z ↓	0.0045	0.0052	0.8132	0.8715
A to Z ↑	0.0077	0.0086	1.0684	1.2139
	C8T28SOI_LL_-CNIVX22_P0	**C8T28SOI_LL_-CNIVX22_P4**	**C8T28SOI_LL_-CNIVX22_P0**	**C8T28SOI_LL_-CNIVX22_P4**
A to Z ↓	0.0028	0.0034	0.5618	0.6002
A to Z ↑	0.0055	0.0062	0.6462	0.7285
	C8T28SOI_LL_-CNIVX22_P10	**C8T28SOI_LL_-CNIVX22_P16**	**C8T28SOI_LL_-CNIVX22_P10**	**C8T28SOI_LL_-CNIVX22_P16**
A to Z ↓	0.0042	0.0048	0.6532	0.6991
A to Z ↑	0.0072	0.0081	0.8517	0.9680
	C8T28SOI_LL_-CNIVX27_P0	**C8T28SOI_LL_-CNIVX27_P4**	**C8T28SOI_LL_-CNIVX27_P0**	**C8T28SOI_LL_-CNIVX27_P4**
A to Z ↓	0.0032	0.0038	0.4674	0.4996
A to Z ↑	0.0058	0.0066	0.5369	0.6053
	C8T28SOI_LL_-CNIVX27_P10	**C8T28SOI_LL_-CNIVX27_P16**	**C8T28SOI_LL_-CNIVX27_P10**	**C8T28SOI_LL_-CNIVX27_P16**
A to Z ↓	0.0047	0.0054	0.5433	0.5822
A to Z ↑	0.0077	0.0086	0.7084	0.8039
	C8T28SOI_LL_-CNIVX32_P0	**C8T28SOI_LL_-CNIVX32_P4**	**C8T28SOI_LL_-CNIVX32_P0**	**C8T28SOI_LL_-CNIVX32_P4**
A to Z ↓	0.0032	0.0038	0.3865	0.4127
A to Z ↑	0.0060	0.0068	0.4583	0.5164
	C8T28SOI_LL_-CNIVX32_P10	**C8T28SOI_LL_-CNIVX32_P16**	**C8T28SOI_LL_-CNIVX32_P10**	**C8T28SOI_LL_-CNIVX32_P16**
A to Z ↓	0.0046	0.0053	0.4485	0.4807
A to Z ↑	0.0078	0.0087	0.6048	0.6865
	C8T28SOI_LL_-CNIVX37_P0	**C8T28SOI_LL_-CNIVX37_P4**	**C8T28SOI_LL_-CNIVX37_P0**	**C8T28SOI_LL_-CNIVX37_P4**
A to Z ↓	0.0032	0.0039	0.3419	0.3650
A to Z ↑	0.0059	0.0068	0.4047	0.4554
	C8T28SOI_LL_-CNIVX37_P10	**C8T28SOI_LL_-CNIVX37_P16**	**C8T28SOI_LL_-CNIVX37_P10**	**C8T28SOI_LL_-CNIVX37_P16**
A to Z ↓	0.0047	0.0054	0.3969	0.4254
A to Z ↑	0.0078	0.0087	0.5331	0.6049
	C8T28SOI_LL_-CNIVX74_P0	**C8T28SOI_LL_-CNIVX74_P4**	**C8T28SOI_LL_-CNIVX74_P0**	**C8T28SOI_LL_-CNIVX74_P4**
A to Z ↓	0.0057	0.0067	0.1728	0.1847
A to Z ↑	0.0083	0.0094	0.2044	0.2298

	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A to Z ↓	0.0077	0.0085	0.2011	0.2154
A to Z ↑	0.0106	0.0117	0.2690	0.3051
	C8T28SOIDV_LL_-CNIVX18_P0	**C8T28SOIDV_LL_-CNIVX18_P4**	**C8T28SOIDV_LL_-CNIVX18_P0**	**C8T28SOIDV_LL_-CNIVX18_P4**
A to Z ↓	0.0030	0.0035	0.6649	0.7116
A to Z ↑	0.0053	0.0061	0.7767	0.8793
	C8T28SOIDV_LL_-CNIVX18_P10	**C8T28SOIDV_LL_-CNIVX18_P16**	**C8T28SOIDV_LL_-CNIVX18_P10**	**C8T28SOIDV_LL_-CNIVX18_P16**
A to Z ↓	0.0044	0.0050	0.7746	0.8301
A to Z ↑	0.0073	0.0081	1.0318	1.1752
	C8T28SOIDV_LL_-CNIVX28_P0	**C8T28SOIDV_LL_-CNIVX28_P4**	**C8T28SOIDV_LL_-CNIVX28_P0**	**C8T28SOIDV_LL_-CNIVX28_P4**
A to Z ↓	0.0033	0.0038	0.4523	0.4839
A to Z ↑	0.0053	0.0061	0.5189	0.5875
	C8T28SOIDV_LL_-CNIVX28_P10	**C8T28SOIDV_LL_-CNIVX28_P16**	**C8T28SOIDV_LL_-CNIVX28_P10**	**C8T28SOIDV_LL_-CNIVX28_P16**
A to Z ↓	0.0046	0.0052	0.5268	0.5649
A to Z ↑	0.0072	0.0081	0.6892	0.7848
	C8T28SOIDV_LL_-CNIVX37_P0	**C8T28SOIDV_LL_-CNIVX37_P4**	**C8T28SOIDV_LL_-CNIVX37_P0**	**C8T28SOIDV_LL_-CNIVX37_P4**
A to Z ↓	0.0032	0.0037	0.3401	0.3639
A to Z ↑	0.0050	0.0059	0.3890	0.4404
	C8T28SOIDV_LL_-CNIVX37_P10	**C8T28SOIDV_LL_-CNIVX37_P16**	**C8T28SOIDV_LL_-CNIVX37_P10**	**C8T28SOIDV_LL_-CNIVX37_P16**
A to Z ↓	0.0045	0.0050	0.3961	0.4251
A to Z ↑	0.0070	0.0078	0.5169	0.5884
	C8T28SOIDV_LL_-CNIVX55_P0	**C8T28SOIDV_LL_-CNIVX55_P4**	**C8T28SOIDV_LL_-CNIVX55_P0**	**C8T28SOIDV_LL_-CNIVX55_P4**
A to Z ↓	0.0032	0.0037	0.2288	0.2449
A to Z ↑	0.0049	0.0058	0.2605	0.2950
	C8T28SOIDV_LL_-CNIVX55_P10	**C8T28SOIDV_LL_-CNIVX55_P16**	**C8T28SOIDV_LL_-CNIVX55_P10**	**C8T28SOIDV_LL_-CNIVX55_P16**
A to Z ↓	0.0044	0.0051	0.2668	0.2862
A to Z ↑	0.0068	0.0077	0.3460	0.3937
	C8T28SOIDV_LL_-CNIVX74_P0	**C8T28SOIDV_LL_-CNIVX74_P4**	**C8T28SOIDV_LL_-CNIVX74_P0**	**C8T28SOIDV_LL_-CNIVX74_P4**
A to Z ↓	0.0038	0.0043	0.1746	0.1867
A to Z ↑	0.0053	0.0062	0.1970	0.2225
	C8T28SOIDV_LL_-CNIVX74_P10	**C8T28SOIDV_LL_-CNIVX74_P16**	**C8T28SOIDV_LL_-CNIVX74_P10**	**C8T28SOIDV_LL_-CNIVX74_P16**
A to Z ↓	0.0050	0.0057	0.2037	0.2182
A to Z ↑	0.0072	0.0081	0.2611	0.2966

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_CNIVX2_P0	1.041e-04	1.000e-20
C8T28SOI_LL_CNIVX2_P4	2.667e-05	1.000e-20
C8T28SOI_LL_CNIVX2_P10	6.513e-06	1.000e-20
C8T28SOI_LL_CNIVX2_P16	2.734e-06	1.000e-20
C8T28SOI_LL_CNIVX4_P0	1.952e-04	1.000e-20

C8T28SOI_LL_CNIVX4_P4	5.110e-05	1.000e-20
C8T28SOI_LL_CNIVX4_P10	1.228e-05	1.000e-20
C8T28SOI_LL_CNIVX4_P16	5.027e-06	1.000e-20
C8T28SOI_LL_CNIVX9_P0	4.149e-04	1.000e-20
C8T28SOI_LL_CNIVX9_P4	1.093e-04	1.000e-20
C8T28SOI_LL_CNIVX9_P10	2.611e-05	1.000e-20
C8T28SOI_LL_CNIVX9_P16	1.059e-05	1.000e-20
C8T28SOI_LL_CNIVX14_P0	6.230e-04	1.000e-20
C8T28SOI_LL_CNIVX14_P4	1.623e-04	1.000e-20
C8T28SOI_LL_CNIVX14_P10	3.836e-05	1.000e-20
C8T28SOI_LL_CNIVX14_P16	1.549e-05	1.000e-20
C8T28SOI_LL_CNIVX18_P0	7.848e-04	1.000e-20
C8T28SOI_LL_CNIVX18_P4	2.061e-04	1.000e-20
C8T28SOI_LL_CNIVX18_P10	4.889e-05	1.000e-20
C8T28SOI_LL_CNIVX18_P16	1.969e-05	1.000e-20
C8T28SOI_LL_CNIVX22_P0	9.688e-04	1.000e-20
C8T28SOI_LL_CNIVX22_P4	2.543e-04	1.000e-20
C8T28SOI_LL_CNIVX22_P10	6.025e-05	1.000e-20
C8T28SOI_LL_CNIVX22_P16	2.425e-05	1.000e-20
C8T28SOI_LL_CNIVX27_P0	1.153e-03	1.000e-20
C8T28SOI_LL_CNIVX27_P4	3.026e-04	1.000e-20
C8T28SOI_LL_CNIVX27_P10	7.163e-05	1.000e-20
C8T28SOI_LL_CNIVX27_P16	2.881e-05	1.000e-20
C8T28SOI_LL_CNIVX32_P0	1.345e-03	1.000e-20
C8T28SOI_LL_CNIVX32_P4	3.538e-04	1.000e-20
C8T28SOI_LL_CNIVX32_P10	8.400e-05	1.000e-20
C8T28SOI_LL_CNIVX32_P16	3.387e-05	1.000e-20
C8T28SOI_LL_CNIVX37_P0	1.530e-03	1.000e-20
C8T28SOI_LL_CNIVX37_P4	4.024e-04	1.000e-20
C8T28SOI_LL_CNIVX37_P10	9.550e-05	1.000e-20
C8T28SOI_LL_CNIVX37_P16	3.850e-05	1.000e-20
C8T28SOI_LL_CNIVX74_P0	3.009e-03	1.000e-20
C8T28SOI_LL_CNIVX74_P4	7.912e-04	1.000e-20
C8T28SOI_LL_CNIVX74_P10	1.876e-04	1.000e-20
C8T28SOI_LL_CNIVX74_P16	7.552e-05	1.000e-20
C8T28SOIDV_LL_CNIVX18_P0	8.504e-04	1.000e-20
C8T28SOIDV_LL_CNIVX18_P4	2.204e-04	1.000e-20
C8T28SOIDV_LL_CNIVX18_P10	5.158e-05	1.000e-20
C8T28SOIDV_LL_CNIVX18_P16	2.059e-05	1.000e-20
C8T28SOIDV_LL_CNIVX28_P0	1.300e-03	1.000e-20
C8T28SOIDV_LL_CNIVX28_P4	3.321e-04	1.000e-20
C8T28SOIDV_LL_CNIVX28_P10	7.649e-05	1.000e-20
C8T28SOIDV_LL_CNIVX28_P16	3.025e-05	1.000e-20
C8T28SOIDV_LL_CNIVX37_P0	1.719e-03	1.000e-20
C8T28SOIDV_LL_CNIVX37_P4	4.376e-04	1.000e-20
C8T28SOIDV_LL_CNIVX37_P10	1.003e-04	1.000e-20
C8T28SOIDV_LL_CNIVX37_P16	3.954e-05	1.000e-20
C8T28SOIDV_LL_CNIVX55_P0	2.554e-03	1.000e-20
C8T28SOIDV_LL_CNIVX55_P4	6.480e-04	1.000e-20
C8T28SOIDV_LL_CNIVX55_P10	1.478e-04	1.000e-20
C8T28SOIDV_LL_CNIVX55_P16	5.809e-05	1.000e-20
C8T28SOIDV_LL_CNIVX74_P0	3.406e-03	1.000e-20

C8T28SOIDV_LL_CNIVX74_P4	8.624e-04	1.000e-20
C8T28SOIDV_LL_CNIVX74_P10	1.961e-04	1.000e-20
C8T28SOIDV_LL_CNIVX74_P16	7.692e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_-CNIVX2_P0	C8T28SOI_LL_-CNIVX2_P4	C8T28SOI_LL_-CNIVX2_P10	C8T28SOI_LL_-CNIVX2_P16
A to Z	1.093e-03	8.291e-04	6.445e-04	5.581e-04
	C8T28SOI_LL_-CNIVX4_P0	C8T28SOI_LL_-CNIVX4_P4	C8T28SOI_LL_-CNIVX4_P10	C8T28SOI_LL_-CNIVX4_P16
A to Z	1.732e-03	1.293e-03	9.794e-04	8.274e-04
	C8T28SOI_LL_-CNIVX9_P0	C8T28SOI_LL_-CNIVX9_P4	C8T28SOI_LL_-CNIVX9_P10	C8T28SOI_LL_-CNIVX9_P16
A to Z	3.601e-03	2.664e-03	1.950e-03	1.616e-03
	C8T28SOI_LL_-CNIVX14_P0	C8T28SOI_LL_-CNIVX14_P4	C8T28SOI_LL_-CNIVX14_P10	C8T28SOI_LL_-CNIVX14_P16
A to Z	5.374e-03	4.007e-03	2.963e-03	2.477e-03
	C8T28SOI_LL_-CNIVX18_P0	C8T28SOI_LL_-CNIVX18_P4	C8T28SOI_LL_-CNIVX18_P10	C8T28SOI_LL_-CNIVX18_P16
A to Z	7.017e-03	5.257e-03	3.918e-03	3.298e-03
	C8T28SOI_LL_-CNIVX22_P0	C8T28SOI_LL_-CNIVX22_P4	C8T28SOI_LL_-CNIVX22_P10	C8T28SOI_LL_-CNIVX22_P16
A to Z	8.669e-03	6.444e-03	4.776e-03	3.953e-03
	C8T28SOI_LL_-CNIVX27_P0	C8T28SOI_LL_-CNIVX27_P4	C8T28SOI_LL_-CNIVX27_P10	C8T28SOI_LL_-CNIVX27_P16
A to Z	1.047e-02	7.840e-03	5.825e-03	4.870e-03
	C8T28SOI_LL_-CNIVX32_P0	C8T28SOI_LL_-CNIVX32_P4	C8T28SOI_LL_-CNIVX32_P10	C8T28SOI_LL_-CNIVX32_P16
A to Z	1.236e-02	9.241e-03	6.826e-03	5.695e-03
	C8T28SOI_LL_-CNIVX37_P0	C8T28SOI_LL_-CNIVX37_P4	C8T28SOI_LL_-CNIVX37_P10	C8T28SOI_LL_-CNIVX37_P16
A to Z	1.403e-02	1.052e-02	7.803e-03	6.517e-03
	C8T28SOI_LL_-CNIVX74_P0	C8T28SOI_LL_-CNIVX74_P4	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A to Z	2.996e-02	2.297e-02	1.732e-02	1.446e-02
	C8T28SOIDV_LL_-CNIVX18_P0	C8T28SOIDV_LL_-CNIVX18_P4	C8T28SOIDV_LL_-CNIVX18_P10	C8T28SOIDV_LL_-CNIVX18_P16
A to Z	7.044e-03	5.205e-03	3.833e-03	3.180e-03
	C8T28SOIDV_LL_-CNIVX28_P0	C8T28SOIDV_LL_-CNIVX28_P4	C8T28SOIDV_LL_-CNIVX28_P10	C8T28SOIDV_LL_-CNIVX28_P16
A to Z	1.056e-02	7.832e-03	5.831e-03	4.844e-03
	C8T28SOIDV_LL_-CNIVX37_P0	C8T28SOIDV_LL_-CNIVX37_P4	C8T28SOIDV_LL_-CNIVX37_P10	C8T28SOIDV_LL_-CNIVX37_P16
A to Z	1.383e-02	1.018e-02	7.556e-03	6.149e-03
	C8T28SOIDV_LL_-CNIVX55_P0	C8T28SOIDV_LL_-CNIVX55_P4	C8T28SOIDV_LL_-CNIVX55_P10	C8T28SOIDV_LL_-CNIVX55_P16
A to Z	2.055e-02	1.516e-02	1.115e-02	9.173e-03
	C8T28SOIDV_LL_-CNIVX74_P0	C8T28SOIDV_LL_-CNIVX74_P4	C8T28SOIDV_LL_-CNIVX74_P10	C8T28SOIDV_LL_-CNIVX74_P16
A to Z	2.760e-02	2.048e-02	1.509e-02	1.240e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

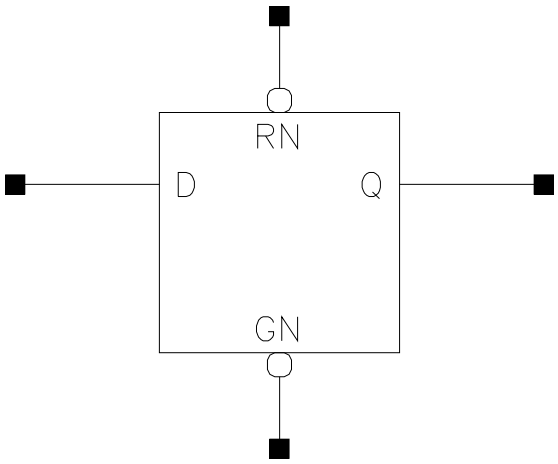
Pin Cycle (vdds)	C8T28SOI_LL_-CNIVX2_P0	C8T28SOI_LL_-CNIVX2_P4	C8T28SOI_LL_-CNIVX2_P10	C8T28SOI_LL_-CNIVX2_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX4_P0	C8T28SOI_LL_-CNIVX4_P4	C8T28SOI_LL_-CNIVX4_P10	C8T28SOI_LL_-CNIVX4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX9_P0	C8T28SOI_LL_-CNIVX9_P4	C8T28SOI_LL_-CNIVX9_P10	C8T28SOI_LL_-CNIVX9_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX14_P0	C8T28SOI_LL_-CNIVX14_P4	C8T28SOI_LL_-CNIVX14_P10	C8T28SOI_LL_-CNIVX14_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX18_P0	C8T28SOI_LL_-CNIVX18_P4	C8T28SOI_LL_-CNIVX18_P10	C8T28SOI_LL_-CNIVX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX22_P0	C8T28SOI_LL_-CNIVX22_P4	C8T28SOI_LL_-CNIVX22_P10	C8T28SOI_LL_-CNIVX22_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX27_P0	C8T28SOI_LL_-CNIVX27_P4	C8T28SOI_LL_-CNIVX27_P10	C8T28SOI_LL_-CNIVX27_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX32_P0	C8T28SOI_LL_-CNIVX32_P4	C8T28SOI_LL_-CNIVX32_P10	C8T28SOI_LL_-CNIVX32_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX37_P0	C8T28SOI_LL_-CNIVX37_P4	C8T28SOI_LL_-CNIVX37_P10	C8T28SOI_LL_-CNIVX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX74_P0	C8T28SOI_LL_-CNIVX74_P4	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX18_P0	C8T28SOIDV_LL_-CNIVX18_P4	C8T28SOIDV_LL_-CNIVX18_P10	C8T28SOIDV_LL_-CNIVX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX28_P0	C8T28SOIDV_LL_-CNIVX28_P4	C8T28SOIDV_LL_-CNIVX28_P10	C8T28SOIDV_LL_-CNIVX28_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX37_P0	C8T28SOIDV_LL_-CNIVX37_P4	C8T28SOIDV_LL_-CNIVX37_P10	C8T28SOIDV_LL_-CNIVX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX55_P0	C8T28SOIDV_LL_-CNIVX55_P4	C8T28SOIDV_LL_-CNIVX55_P10	C8T28SOIDV_LL_-CNIVX55_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX74_P0	C8T28SOIDV_LL_-CNIVX74_P4	C8T28SOIDV_LL_-CNIVX74_P10	C8T28SOIDV_LL_-CNIVX74_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNLDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	1.600	1.360	2.1760
X19_P4	1.600	1.360	2.1760
X19_P10	1.600	1.360	2.1760
X19_P16	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
D	0.0011	0.0012	0.0012	0.0013
GN	0.0013	0.0014	0.0015	0.0016
RN	0.0005	0.0005	0.0005	0.0006

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	X19_P4	X19_P0	X19_P4

D to Q ↓	0.0285	0.0333	0.6486	0.6992
D to Q ↑	0.0313	0.0353	0.7629	0.8699
GN to Q ↓	0.0254	0.0299	0.6491	0.6996
GN to Q ↑	0.0340	0.0386	0.7645	0.8713
RN to Q ↓	0.0375	0.0437	0.6411	0.6929
RN to Q ↑	0.0353	0.0400	0.7648	0.8715
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
D to Q ↓	0.0407	0.0480	0.7729	0.8394
D to Q ↑	0.0418	0.0482	1.0304	1.1829
GN to Q ↓	0.0363	0.0424	0.7732	0.8404
GN to Q ↑	0.0459	0.0528	1.0334	1.1846
RN to Q ↓	0.0531	0.0622	0.7666	0.8351
RN to Q ↑	0.0471	0.0539	1.0339	1.1855

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X19_P0	X19_P4	X19_P10	X19_P16
D ↓	hold_rising to GN	0.0041	0.0025	-0.0046	-0.0095
D ↑	hold_rising to GN	0.0032	0.0010	-0.0039	-0.0088
D ↓	setup_rising to GN	0.0331	0.0385	0.0450	0.0553
D ↑	setup_rising to GN	0.0340	0.0389	0.0433	0.0541
GN ↓	min_pulse_width to GN	0.0366	0.0408	0.0483	0.0575
RN ↓	min_pulse_width to RN	0.0474	0.0544	0.0664	0.0784
RN ↑	recovery_rising to GN	0.0390	0.0407	0.0514	0.0579
RN ↑	removal_rising to GN	-0.0191	-0.0239	-0.0314	-0.0359

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X19_P0	1.639e-03	1.000e-20
X19_P4	4.083e-04	1.000e-20
X19_P10	9.297e-05	1.000e-20
X19_P16	3.716e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
D (output stable)	7.148e-05	7.088e-05	1.108e-04	1.374e-04
GN (output stable)	2.370e-03	2.017e-03	1.843e-03	1.779e-03
RN (output stable)	8.606e-05	8.033e-05	7.423e-05	6.664e-05
D to Q	1.621e-02	1.448e-02	1.349e-02	1.328e-02
GN to Q	1.894e-02	1.712e-02	1.608e-02	1.586e-02
RN to Q	1.230e-02	1.125e-02	1.069e-02	1.062e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

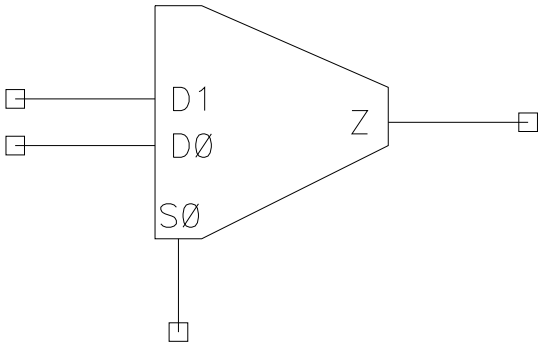
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX21

Cell Description

2:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	1.632	1.3056
X9_P4	0.800	1.632	1.3056
X9_P10	0.800	1.632	1.3056
X9_P16	0.800	1.632	1.3056
X15_P0	0.800	2.312	1.8496
X15_P4	0.800	2.312	1.8496
X15_P10	0.800	2.312	1.8496
X15_P16	0.800	2.312	1.8496
X27_P0	0.800	2.584	2.0672
X27_P4	0.800	2.584	2.0672
X27_P10	0.800	2.584	2.0672
X27_P16	0.800	2.584	2.0672

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
D0	0.0007	0.0007	0.0008	0.0008
D1	0.0007	0.0007	0.0008	0.0008
S0	0.0012	0.0013	0.0014	0.0014
	X15_P0	X15_P4	X15_P10	X15_P16
D0	0.0011	0.0011	0.0012	0.0013
D1	0.0011	0.0012	0.0012	0.0013
S0	0.0012	0.0013	0.0013	0.0014
	X27_P0	X27_P4	X27_P10	X27_P16

D0	0.0012	0.0012	0.0013	0.0014
D1	0.0011	0.0012	0.0013	0.0014
S0	0.0014	0.0015	0.0016	0.0017

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
D0 to Z ↓	0.0213	0.0244	1.2790	1.3708
D0 to Z ↑	0.0182	0.0205	1.6201	1.8321
D1 to Z ↓	0.0211	0.0242	1.2778	1.3683
D1 to Z ↑	0.0177	0.0200	1.6166	1.8290
S0 to Z ↓	0.0185	0.0210	1.2734	1.3637
S0 to Z ↑	0.0176	0.0201	1.6189	1.8287
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
D0 to Z ↓	0.0291	0.0336	1.5021	1.6216
D0 to Z ↑	0.0240	0.0274	2.1579	2.4622
D1 to Z ↓	0.0289	0.0334	1.5005	1.6201
D1 to Z ↑	0.0234	0.0266	2.1529	2.4601
S0 to Z ↓	0.0248	0.0283	1.4951	1.6139
S0 to Z ↑	0.0239	0.0274	2.1523	2.4592
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
D0 to Z ↓	0.0197	0.0227	0.8472	0.9092
D0 to Z ↑	0.0207	0.0231	0.8664	0.9793
D1 to Z ↓	0.0209	0.0240	0.8486	0.9094
D1 to Z ↑	0.0198	0.0221	0.8648	0.9791
S0 to Z ↓	0.0224	0.0255	0.8456	0.9065
S0 to Z ↑	0.0220	0.0251	0.8642	0.9787
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
D0 to Z ↓	0.0271	0.0313	0.9965	1.0752
D0 to Z ↑	0.0268	0.0304	1.1553	1.3195
D1 to Z ↓	0.0288	0.0333	0.9985	1.0775
D1 to Z ↑	0.0257	0.0291	1.1538	1.3175
S0 to Z ↓	0.0301	0.0344	0.9944	1.0744
S0 to Z ↑	0.0298	0.0341	1.1531	1.3176
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0225	0.0258	0.4726	0.5081
D0 to Z ↑	0.0224	0.0250	0.5157	0.5834
D1 to Z ↓	0.0235	0.0270	0.4738	0.5094
D1 to Z ↑	0.0228	0.0254	0.5159	0.5836
S0 to Z ↓	0.0245	0.0277	0.4730	0.5078
S0 to Z ↑	0.0228	0.0260	0.5155	0.5829
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.0310	0.0359	0.5584	0.6046
D0 to Z ↑	0.0292	0.0332	0.6863	0.7838
D1 to Z ↓	0.0324	0.0377	0.5600	0.6065
D1 to Z ↑	0.0296	0.0335	0.6876	0.7849
S0 to Z ↓	0.0327	0.0374	0.5586	0.6046
S0 to Z ↑	0.0309	0.0354	0.6864	0.7843

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds

X9_P0	1.228e-03	1.000e-20
X9_P4	3.191e-04	1.000e-20
X9_P10	7.566e-05	1.000e-20
X9_P16	3.070e-05	1.000e-20
X15_P0	1.802e-03	1.000e-20
X15_P4	4.586e-04	1.000e-20
X15_P10	1.071e-04	1.000e-20
X15_P16	4.314e-05	1.000e-20
X27_P0	2.489e-03	1.000e-20
X27_P4	6.473e-04	1.000e-20
X27_P10	1.523e-04	1.000e-20
X27_P16	6.113e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	2.253e-03	1.849e-03	1.556e-03	1.423e-03
D1 (output stable)	2.216e-03	1.815e-03	1.525e-03	1.389e-03
S0 (output stable)	2.385e-03	2.030e-03	1.796e-03	1.713e-03
D0 to Z	6.438e-03	5.772e-03	5.407e-03	5.338e-03
D1 to Z	6.277e-03	5.623e-03	5.272e-03	5.209e-03
S0 to Z	7.356e-03	6.515e-03	6.025e-03	5.899e-03
	X15_P0	X15_P4	X15_P10	X15_P16
D0 (output stable)	3.434e-03	2.711e-03	2.175e-03	1.921e-03
D1 (output stable)	3.420e-03	2.753e-03	2.254e-03	2.023e-03
S0 (output stable)	2.065e-03	1.854e-03	1.739e-03	1.719e-03
D0 to Z	1.125e-02	1.000e-02	9.307e-03	9.135e-03
D1 to Z	1.109e-02	9.876e-03	9.201e-03	9.035e-03
S0 to Z	1.168e-02	1.052e-02	9.894e-03	9.762e-03
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	3.809e-03	2.999e-03	2.408e-03	2.122e-03
D1 (output stable)	3.695e-03	2.953e-03	2.409e-03	2.152e-03
S0 (output stable)	2.497e-03	2.216e-03	2.050e-03	2.010e-03
D0 to Z	1.763e-02	1.571e-02	1.459e-02	1.430e-02
D1 to Z	1.769e-02	1.577e-02	1.464e-02	1.433e-02
S0 to Z	1.830e-02	1.643e-02	1.535e-02	1.509e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

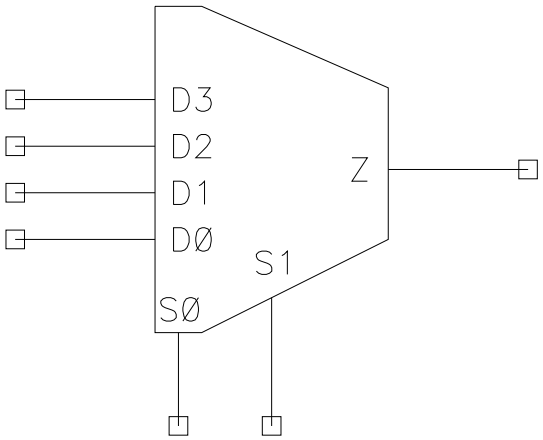
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX41

Cell Description

4:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	1.600	1.768	2.8288
X9_P4	1.600	1.768	2.8288
X9_P10	1.600	1.768	2.8288
X9_P16	1.600	1.768	2.8288
X27_P0	1.600	2.584	4.1344
X27_P4	1.600	2.584	4.1344
X27_P10	1.600	2.584	4.1344
X27_P16	1.600	2.584	4.1344

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
D0	0.0007	0.0007	0.0007	0.0008
D1	0.0005	0.0006	0.0006	0.0006
D2	0.0007	0.0007	0.0007	0.0008
D3	0.0006	0.0006	0.0006	0.0006
S0	0.0016	0.0017	0.0019	0.0020
S1	0.0009	0.0009	0.0010	0.0011

	X27_P0	X27_P4	X27_P10	X27_P16
D0	0.0010	0.0010	0.0011	0.0011
D1	0.0009	0.0009	0.0010	0.0010
D2	0.0010	0.0011	0.0011	0.0012
D3	0.0010	0.0010	0.0011	0.0011
S0	0.0025	0.0026	0.0028	0.0030
S1	0.0017	0.0018	0.0020	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
D0 to Z ↓	0.0355	0.0415	1.3266	1.4289
D0 to Z ↑	0.0335	0.0379	1.6304	1.8489
D1 to Z ↓	0.0353	0.0414	1.3277	1.4298
D1 to Z ↑	0.0333	0.0376	1.6297	1.8474
D2 to Z ↓	0.0360	0.0420	1.3307	1.4329
D2 to Z ↑	0.0319	0.0362	1.6229	1.8435
D3 to Z ↓	0.0350	0.0409	1.3292	1.4320
D3 to Z ↑	0.0316	0.0359	1.6239	1.8405
S0 to Z ↓	0.0385	0.0455	1.3263	1.4288
S0 to Z ↑	0.0389	0.0447	1.6304	1.8483
S1 to Z ↓	0.0283	0.0325	1.3267	1.4289
S1 to Z ↑	0.0318	0.0359	1.6270	1.8457
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
D0 to Z ↓	0.0506	0.0593	1.5765	1.7126
D0 to Z ↑	0.0447	0.0513	2.1850	2.5016
D1 to Z ↓	0.0505	0.0592	1.5778	1.7140
D1 to Z ↑	0.0445	0.0510	2.1835	2.4994
D2 to Z ↓	0.0511	0.0599	1.5824	1.7193
D2 to Z ↑	0.0428	0.0492	2.1779	2.4939
D3 to Z ↓	0.0499	0.0586	1.5805	1.7170
D3 to Z ↑	0.0425	0.0488	2.1771	2.4923
S0 to Z ↓	0.0559	0.0660	1.5773	1.7134
S0 to Z ↑	0.0536	0.0622	2.1842	2.5005
S1 to Z ↓	0.0391	0.0454	1.5776	1.7142
S1 to Z ↑	0.0421	0.0482	2.1799	2.4964
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0383	0.0446	0.4446	0.4804
D0 to Z ↑	0.0390	0.0441	0.5956	0.6734
D1 to Z ↓	0.0411	0.0480	0.4478	0.4846
D1 to Z ↑	0.0386	0.0438	0.5950	0.6732
D2 to Z ↓	0.0406	0.0474	0.4475	0.4839
D2 to Z ↑	0.0393	0.0444	0.5957	0.6740
D3 to Z ↓	0.0391	0.0457	0.4460	0.4819
D3 to Z ↑	0.0389	0.0440	0.5957	0.6740
S0 to Z ↓	0.0459	0.0538	0.4456	0.4815
S0 to Z ↑	0.0462	0.0530	0.5964	0.6745
S1 to Z ↓	0.0332	0.0382	0.4467	0.4825
S1 to Z ↑	0.0394	0.0443	0.5958	0.6734
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.0544	0.0639	0.5326	0.5807
D0 to Z ↑	0.0523	0.0602	0.7937	0.9073

D1 to Z ↓	0.0585	0.0687	0.5380	0.5872
D1 to Z ↑	0.0520	0.0600	0.7935	0.9069
D2 to Z ↓	0.0579	0.0680	0.5369	0.5857
D2 to Z ↑	0.0526	0.0606	0.7945	0.9079
D3 to Z ↓	0.0558	0.0656	0.5344	0.5826
D3 to Z ↑	0.0521	0.0600	0.7941	0.9078
S0 to Z ↓	0.0657	0.0772	0.5341	0.5825
S0 to Z ↑	0.0637	0.0741	0.7945	0.9079
S1 to Z ↓	0.0460	0.0537	0.5352	0.5838
S1 to Z ↑	0.0521	0.0598	0.7938	0.9074

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X9_P0	9.501e-04	1.000e-20
X9_P4	2.495e-04	1.000e-20
X9_P10	6.174e-05	1.000e-20
X9_P16	2.660e-05	1.000e-20
X27_P0	2.228e-03	1.000e-20
X27_P4	5.815e-04	1.000e-20
X27_P10	1.413e-04	1.000e-20
X27_P16	5.978e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	6.229e-05	5.771e-05	5.508e-05	5.010e-05
D1 (output stable)	7.867e-05	7.529e-05	7.356e-05	7.183e-05
D2 (output stable)	8.020e-05	7.483e-05	7.577e-05	7.234e-05
D3 (output stable)	8.038e-05	7.623e-05	7.317e-05	7.112e-05
S0 (output stable)	2.017e-03	1.885e-03	1.864e-03	1.918e-03
S1 (output stable)	2.357e-03	2.140e-03	2.020e-03	1.854e-03
D0 to Z	7.898e-03	7.147e-03	6.735e-03	6.671e-03
D1 to Z	7.873e-03	7.124e-03	6.724e-03	6.658e-03
D2 to Z	7.779e-03	7.027e-03	6.626e-03	6.557e-03
D3 to Z	7.741e-03	6.990e-03	6.592e-03	6.523e-03
S0 to Z	9.930e-03	9.188e-03	8.861e-03	8.899e-03
S1 to Z	8.936e-03	8.013e-03	7.455e-03	7.080e-03
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	1.256e-04	1.141e-04	1.077e-04	1.004e-04
D1 (output stable)	8.795e-05	7.990e-05	7.395e-05	7.500e-05
D2 (output stable)	1.283e-04	1.165e-04	1.081e-04	1.024e-04
D3 (output stable)	1.222e-04	1.129e-04	1.071e-04	1.115e-04
S0 (output stable)	3.501e-03	3.372e-03	3.413e-03	3.537e-03
S1 (output stable)	3.715e-03	3.346e-03	3.218e-03	3.110e-03
D0 to Z	2.358e-02	2.099e-02	1.944e-02	1.904e-02
D1 to Z	2.407e-02	2.145e-02	1.988e-02	1.947e-02
D2 to Z	2.417e-02	2.152e-02	1.995e-02	1.953e-02
D3 to Z	2.383e-02	2.121e-02	1.965e-02	1.925e-02
S0 to Z	2.734e-02	2.488e-02	2.356e-02	2.337e-02
S1 to Z	2.552e-02	2.265e-02	2.087e-02	2.012e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

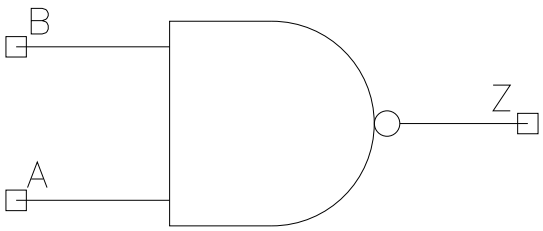
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2

Cell Description

2 input NAND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	0.800	0.952	0.7616
X8_P4	0.800	0.952	0.7616
X8_P10	0.800	0.952	0.7616
X8_P16	0.800	0.952	0.7616
X15_P0	0.800	1.224	0.9792
X15_P4	0.800	1.224	0.9792
X15_P10	0.800	1.224	0.9792
X15_P16	0.800	1.224	0.9792
X27_P0	0.800	1.632	1.3056
X27_P4	0.800	1.632	1.3056
X27_P10	0.800	1.632	1.3056
X27_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0013	0.0013	0.0014	0.0015
B	0.0012	0.0012	0.0013	0.0014
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0005	0.0006	0.0006	0.0007
B	0.0005	0.0005	0.0006	0.0006
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0006	0.0006	0.0007	0.0007
B	0.0007	0.0007	0.0008	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0032	0.0040	1.5956	1.7141
A to Z ↑	0.0100	0.0113	1.7581	1.9918
B to Z ↓	0.0043	0.0050	1.6222	1.7443
B to Z ↑	0.0077	0.0088	1.7727	2.0108
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0054	0.0065	1.8822	2.0329
A to Z ↑	0.0132	0.0149	2.3434	2.6747
B to Z ↓	0.0059	0.0068	1.9172	2.0713
B to Z ↑	0.0102	0.0114	2.3617	2.6968
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0228	0.0262	0.8302	0.8885
A to Z ↑	0.0243	0.0281	0.8376	0.9479
B to Z ↓	0.0247	0.0282	0.8297	0.8880
B to Z ↑	0.0245	0.0283	0.8379	0.9494
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0315	0.0369	0.9712	1.0450
A to Z ↑	0.0338	0.0393	1.1183	1.2772
B to Z ↓	0.0337	0.0391	0.9707	1.0444
B to Z ↑	0.0340	0.0394	1.1180	1.2770
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0239	0.0272	0.4367	0.4684
A to Z ↑	0.0245	0.0283	0.5030	0.5679
B to Z ↓	0.0248	0.0282	0.4365	0.4682
B to Z ↑	0.0237	0.0274	0.5032	0.5685
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0325	0.0378	0.5122	0.5525
A to Z ↑	0.0340	0.0396	0.6698	0.7650
B to Z ↓	0.0336	0.0390	0.5123	0.5522
B to Z ↑	0.0329	0.0382	0.6695	0.7649

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	3.945e-04	1.000e-20
X8_P4	1.058e-04	1.000e-20
X8_P10	2.663e-05	1.000e-20
X8_P16	1.155e-05	1.000e-20
X15_P0	9.648e-04	1.000e-20
X15_P4	2.492e-04	1.000e-20
X15_P10	5.983e-05	1.000e-20
X15_P16	2.467e-05	1.000e-20
X27_P0	1.607e-03	1.000e-20
X27_P4	4.276e-04	1.000e-20
X27_P10	1.033e-04	1.000e-20
X27_P16	4.212e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	8.659e-05	7.585e-05	6.907e-05	6.559e-05
B (output stable)	2.002e-04	2.055e-04	2.082e-04	2.280e-04
A to Z	4.062e-03	3.293e-03	2.786e-03	2.584e-03

B to Z	3.568e-03	2.760e-03	2.180e-03	1.896e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.568e-05	1.330e-05	1.144e-05	1.074e-05
B (output stable)	2.568e-05	2.596e-05	2.618e-05	2.555e-05
A to Z	8.587e-03	8.025e-03	7.771e-03	7.871e-03
B to Z	8.497e-03	7.923e-03	7.651e-03	7.733e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	2.336e-05	1.886e-05	1.597e-05	1.490e-05
B (output stable)	3.318e-05	3.118e-05	3.068e-05	3.039e-05
A to Z	1.361e-02	1.265e-02	1.221e-02	1.226e-02
B to Z	1.352e-02	1.253e-02	1.207e-02	1.209e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

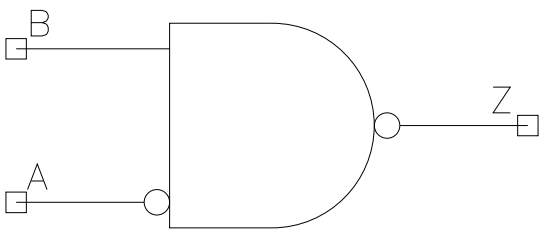
Pin Cycle (vdds)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2A

Cell Description

2 input NAND with A input inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	0.952	0.7616
X9_P4	0.800	0.952	0.7616
X9_P10	0.800	0.952	0.7616
X9_P16	0.800	0.952	0.7616
X15_P0	0.800	1.360	1.0880
X15_P4	0.800	1.360	1.0880
X15_P10	0.800	1.360	1.0880
X15_P16	0.800	1.360	1.0880
X27_P0	0.800	2.856	2.2848
X27_P4	0.800	2.856	2.2848
X27_P10	0.800	2.856	2.2848
X27_P16	0.800	2.856	2.2848

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
A	0.0006	0.0006	0.0007	0.0007
B	0.0006	0.0006	0.0007	0.0008
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0005	0.0006	0.0006	0.0007
B	0.0006	0.0006	0.0006	0.0007
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0018	0.0019	0.0020	0.0022
B	0.0041	0.0042	0.0043	0.0046

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
A to Z ↓	0.0176	0.0202	1.2612	1.3521
A to Z ↑	0.0154	0.0175	1.5392	1.7357
B to Z ↓	0.0193	0.0223	1.2594	1.3485
B to Z ↑	0.0208	0.0236	1.5350	1.7350
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
A to Z ↓	0.0243	0.0285	1.4807	1.5971
A to Z ↑	0.0205	0.0233	2.0427	2.3287
B to Z ↓	0.0269	0.0316	1.4773	1.5932
B to Z ↑	0.0279	0.0320	2.0402	2.3261
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0302	0.0351	0.8797	0.9401
A to Z ↑	0.0269	0.0310	0.8355	0.9427
B to Z ↓	0.0237	0.0271	0.8800	0.9406
B to Z ↑	0.0238	0.0274	0.8359	0.9426
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0425	0.0500	1.0271	1.1069
A to Z ↑	0.0375	0.0441	1.1081	1.2610
B to Z ↓	0.0326	0.0382	1.0274	1.1062
B to Z ↑	0.0328	0.0382	1.1075	1.2615
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0159	0.0184	0.5485	0.5893
A to Z ↑	0.0166	0.0188	0.4904	0.5553
B to Z ↓	0.0064	0.0069	0.5653	0.6078
B to Z ↑	0.0052	0.0064	0.4252	0.4793
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0221	0.0254	0.6485	0.7028
A to Z ↑	0.0223	0.0255	0.6541	0.7472
B to Z ↓	0.0076	0.0082	0.6683	0.7225
B to Z ↑	0.0078	0.0090	0.5593	0.6336

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X9_P0	7.310e-04	1.000e-20
X9_P4	1.968e-04	1.000e-20
X9_P10	4.840e-05	1.000e-20
X9_P16	2.005e-05	1.000e-20
X15_P0	9.767e-04	1.000e-20
X15_P4	2.557e-04	1.000e-20
X15_P10	6.269e-05	1.000e-20
X15_P16	2.626e-05	1.000e-20
X27_P0	2.022e-03	1.000e-20
X27_P4	5.250e-04	1.000e-20
X27_P10	1.257e-04	1.000e-20
X27_P16	5.220e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	3.632e-05	2.774e-05	2.534e-05	2.458e-05
B (output stable)	2.120e-03	1.709e-03	1.428e-03	1.306e-03
A to Z	5.147e-03	4.533e-03	4.192e-03	4.133e-03

B to Z	6.278e-03	5.697e-03	5.398e-03	5.378e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.531e-03	1.311e-03	1.185e-03	1.154e-03
B (output stable)	2.336e-05	2.400e-05	2.454e-05	2.429e-05
A to Z	9.067e-03	8.642e-03	8.564e-03	8.773e-03
B to Z	8.130e-03	7.571e-03	7.379e-03	7.505e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	8.011e-03	7.257e-03	6.969e-03	7.033e-03
B (output stable)	5.494e-04	5.665e-04	5.828e-04	6.498e-04
A to Z	1.664e-02	1.526e-02	1.474e-02	1.477e-02
B to Z	1.254e-02	9.678e-03	7.469e-03	6.430e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

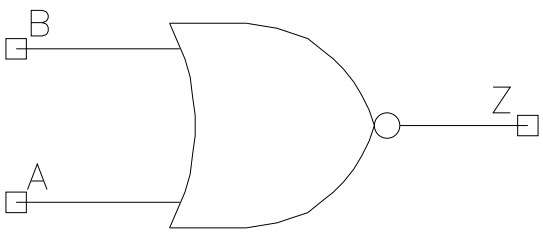
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2

Cell Description

2 input NOR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	0.800	0.952	0.7616
X8_P4	0.800	0.952	0.7616
X8_P10	0.800	0.952	0.7616
X8_P16	0.800	0.952	0.7616
X15_P0	0.800	1.360	1.0880
X15_P4	0.800	1.360	1.0880
X15_P10	0.800	1.360	1.0880
X15_P16	0.800	1.360	1.0880
X27_P0	0.800	1.632	1.3056
X27_P4	0.800	1.632	1.3056
X27_P10	0.800	1.632	1.3056
X27_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0014	0.0015	0.0016	0.0017
B	0.0013	0.0013	0.0014	0.0015
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0005	0.0005	0.0006	0.0006
B	0.0006	0.0006	0.0007	0.0007
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0006	0.0006	0.0007	0.0007
B	0.0007	0.0007	0.0007	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0068	0.0077	1.4393	1.5365
A to Z ↑	0.0069	0.0081	2.0773	2.3177
B to Z ↓	0.0043	0.0051	1.4475	1.5433
B to Z ↑	0.0076	0.0085	2.0959	2.3365
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0091	0.0104	1.6701	1.7858
A to Z ↑	0.0100	0.0118	2.6677	2.9970
B to Z ↓	0.0062	0.0071	1.6789	1.7961
B to Z ↑	0.0097	0.0108	2.6902	3.0232
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0230	0.0266	0.8259	0.8834
A to Z ↑	0.0235	0.0269	0.8280	0.9382
B to Z ↓	0.0219	0.0253	0.8261	0.8836
B to Z ↑	0.0251	0.0287	0.8283	0.9388
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0321	0.0374	0.9646	1.0386
A to Z ↑	0.0325	0.0381	1.1084	1.2679
B to Z ↓	0.0307	0.0358	0.9644	1.0377
B to Z ↑	0.0342	0.0396	1.1087	1.2681
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0246	0.0286	0.4646	0.4980
A to Z ↑	0.0241	0.0279	0.4931	0.5589
B to Z ↓	0.0246	0.0286	0.4646	0.4976
B to Z ↑	0.0255	0.0293	0.4922	0.5590
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0346	0.0407	0.5457	0.5890
A to Z ↑	0.0335	0.0393	0.6599	0.7541
B to Z ↓	0.0344	0.0404	0.5451	0.5887
B to Z ↑	0.0350	0.0406	0.6599	0.7543

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X8_P0	5.614e-04	1.000e-20
X8_P4	1.454e-04	1.000e-20
X8_P10	3.423e-05	1.000e-20
X8_P16	1.392e-05	1.000e-20
X15_P0	1.326e-03	1.000e-20
X15_P4	3.335e-04	1.000e-20
X15_P10	7.673e-05	1.000e-20
X15_P16	3.066e-05	1.000e-20
X27_P0	2.177e-03	1.000e-20
X27_P4	5.438e-04	1.000e-20
X27_P10	1.221e-04	1.000e-20
X27_P16	4.763e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	1.404e-04	1.197e-04	1.101e-04	1.090e-04
B (output stable)	2.704e-04	2.887e-04	2.892e-04	2.764e-04
A to Z	4.407e-03	3.620e-03	3.103e-03	2.934e-03

B to Z	3.768e-03	2.920e-03	2.296e-03	2.003e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	3.082e-05	2.323e-05	2.185e-05	2.113e-05
B (output stable)	3.355e-05	4.050e-05	3.949e-05	3.765e-05
A to Z	8.741e-03	8.126e-03	7.938e-03	8.028e-03
B to Z	8.603e-03	7.979e-03	7.765e-03	7.829e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	4.000e-05	2.873e-05	2.627e-05	2.560e-05
B (output stable)	4.182e-05	4.968e-05	4.904e-05	4.692e-05
A to Z	1.345e-02	1.260e-02	1.210e-02	1.227e-02
B to Z	1.326e-02	1.241e-02	1.189e-02	1.202e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

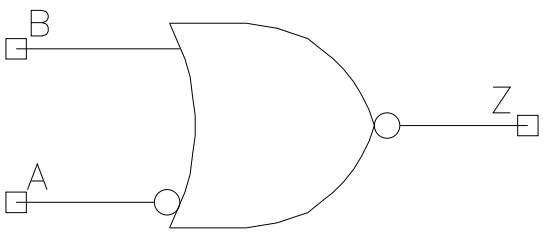
Pin Cycle (vdds)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2A

Cell Description

2 input NOR with A input Inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	1.360	1.0880
X9_P4	0.800	1.360	1.0880
X9_P10	0.800	1.360	1.0880
X9_P16	0.800	1.360	1.0880
X15_P0	0.800	1.496	1.1968
X15_P4	0.800	1.496	1.1968
X15_P10	0.800	1.496	1.1968
X15_P16	0.800	1.496	1.1968
X27_P0	0.800	1.768	1.4144
X27_P4	0.800	1.768	1.4144
X27_P10	0.800	1.768	1.4144
X27_P16	0.800	1.768	1.4144

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
A	0.0010	0.0011	0.0011	0.0012
B	0.0008	0.0008	0.0009	0.0010
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0006	0.0007	0.0007	0.0008
B	0.0007	0.0007	0.0008	0.0008
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0007	0.0007	0.0008	0.0008
B	0.0006	0.0007	0.0007	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
A to Z ↓	0.0193	0.0220	1.2450	1.3331
A to Z ↑	0.0107	0.0126	1.6125	1.8219
B to Z ↓	0.0172	0.0201	1.2397	1.3259
B to Z ↑	0.0206	0.0231	1.6098	1.8183
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
A to Z ↓	0.0261	0.0299	1.4570	1.5675
A to Z ↑	0.0155	0.0180	2.1438	2.4463
B to Z ↓	0.0246	0.0289	1.4500	1.5610
B to Z ↑	0.0273	0.0312	2.1402	2.4428
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0298	0.0344	0.8253	0.8830
A to Z ↑	0.0269	0.0314	0.8302	0.9407
B to Z ↓	0.0219	0.0255	0.8265	0.8840
B to Z ↑	0.0258	0.0295	0.8304	0.9405
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0416	0.0487	0.9653	1.0398
A to Z ↑	0.0383	0.0451	1.1089	1.2689
B to Z ↓	0.0308	0.0360	0.9651	1.0390
B to Z ↑	0.0352	0.0407	1.1102	1.2682
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0298	0.0348	0.4455	0.4782
A to Z ↑	0.0289	0.0333	0.4984	0.5635
B to Z ↓	0.0250	0.0289	0.4458	0.4776
B to Z ↑	0.0261	0.0297	0.4986	0.5631
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0426	0.0506	0.5246	0.5663
A to Z ↑	0.0403	0.0473	0.6643	0.7577
B to Z ↓	0.0350	0.0413	0.5241	0.5668
B to Z ↑	0.0355	0.0413	0.6640	0.7585

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X9_P0	9.577e-04	1.000e-20
X9_P4	2.470e-04	1.000e-20
X9_P10	5.844e-05	1.000e-20
X9_P16	2.397e-05	1.000e-20
X15_P0	1.498e-03	1.000e-20
X15_P4	3.780e-04	1.000e-20
X15_P10	8.732e-05	1.000e-20
X15_P16	3.498e-05	1.000e-20
X27_P0	2.219e-03	1.000e-20
X27_P4	5.665e-04	1.000e-20
X27_P10	1.301e-04	1.000e-20
X27_P16	5.146e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	7.545e-05	6.464e-05	5.817e-05	5.504e-05
B (output stable)	2.590e-03	2.148e-03	1.847e-03	1.771e-03
A to Z	5.719e-03	5.089e-03	4.771e-03	4.722e-03

B to Z	6.759e-03	6.169e-03	5.909e-03	5.903e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.993e-03	1.688e-03	1.503e-03	1.446e-03
B (output stable)	4.036e-05	4.268e-05	4.200e-05	3.987e-05
A to Z	1.008e-02	9.576e-03	9.407e-03	9.577e-03
B to Z	8.728e-03	8.141e-03	7.881e-03	7.974e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	2.134e-03	1.789e-03	1.579e-03	1.509e-03
B (output stable)	5.000e-05	5.118e-05	4.997e-05	4.742e-05
A to Z	1.502e-02	1.411e-02	1.383e-02	1.413e-02
B to Z	1.370e-02	1.265e-02	1.222e-02	1.243e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

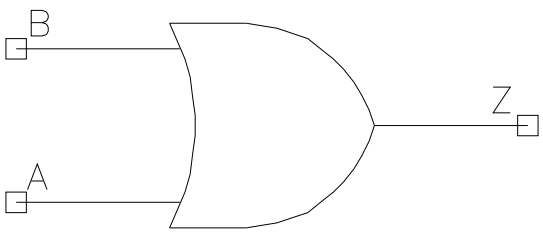
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR2

Cell Description

2 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	0.800	1.632	1.3056
X19_P4	0.800	1.632	1.3056
X19_P10	0.800	1.632	1.3056
X19_P16	0.800	1.632	1.3056
X37_P0	0.800	2.176	1.7408
X37_P4	0.800	2.176	1.7408
X37_P10	0.800	2.176	1.7408
X37_P16	0.800	2.176	1.7408

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0016	0.0017	0.0018	0.0019
B	0.0016	0.0016	0.0018	0.0019
	X37_P0	X37_P4	X37_P10	X37_P16
A	0.0016	0.0017	0.0018	0.0020
B	0.0015	0.0016	0.0017	0.0018

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0158	0.0182	0.6413	0.6859
A to Z ↑	0.0155	0.0174	0.7884	0.8879
B to Z ↓	0.0172	0.0193	0.6406	0.6853
B to Z ↑	0.0136	0.0153	0.7879	0.8861
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**

A to Z ↓	0.0220	0.0259	0.7488	0.8074
A to Z ↑	0.0203	0.0232	1.0412	1.1851
B to Z ↓	0.0228	0.0262	0.7491	0.8078
B to Z ↑	0.0179	0.0204	1.0396	1.1833
	X37_P0	**X37_P4**	**X37_P0**	**X37_P4**
A to Z ↓	0.0200	0.0231	0.3271	0.3505
A to Z ↑	0.0199	0.0222	0.4071	0.4605
B to Z ↓	0.0220	0.0251	0.3269	0.3504
B to Z ↑	0.0180	0.0203	0.4062	0.4599
	X37_P10	**X37_P16**	**X37_P10**	**X37_P16**
A to Z ↓	0.0280	0.0333	0.3848	0.4160
A to Z ↑	0.0258	0.0294	0.5425	0.6198
B to Z ↓	0.0297	0.0346	0.3846	0.4158
B to Z ↑	0.0236	0.0269	0.5415	0.6195

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X19_P0	1.136e-03	1.000e-20
X19_P4	3.089e-04	1.000e-20
X19_P10	7.697e-05	1.000e-20
X19_P16	3.218e-05	1.000e-20
X37_P0	1.667e-03	1.000e-20
X37_P4	4.543e-04	1.000e-20
X37_P10	1.139e-04	1.000e-20
X37_P16	4.780e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	1.366e-04	1.162e-04	1.078e-04	1.077e-04
B (output stable)	2.633e-04	2.815e-04	2.811e-04	2.711e-04
A to Z	1.107e-02	9.725e-03	9.066e-03	9.005e-03
B to Z	1.035e-02	8.976e-03	8.232e-03	8.039e-03
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	1.404e-04	1.155e-04	1.071e-04	1.049e-04
B (output stable)	2.667e-04	2.899e-04	2.920e-04	2.864e-04
A to Z	2.017e-02	1.784e-02	1.648e-02	1.642e-02
B to Z	1.942e-02	1.710e-02	1.561e-02	1.542e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

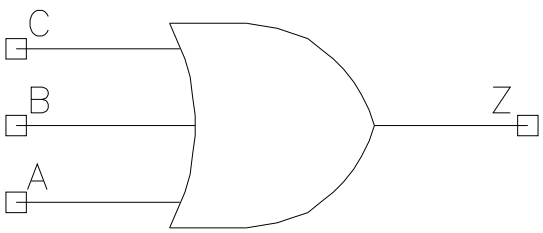
Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR3

Cell Description

3 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	0.800	2.312	1.8496
X14_P4	0.800	2.312	1.8496
X14_P10	0.800	2.312	1.8496
X14_P16	0.800	2.312	1.8496
X19_P0	0.800	2.448	1.9584
X19_P4	0.800	2.448	1.9584
X19_P10	0.800	2.448	1.9584
X19_P16	0.800	2.448	1.9584
X27_P0	1.600	2.312	3.6992
X27_P4	1.600	2.312	3.6992
X27_P10	1.600	2.312	3.6992
X27_P16	1.600	2.312	3.6992

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0005	0.0005	0.0005	0.0006
B	0.0005	0.0005	0.0006	0.0006
C	0.0005	0.0005	0.0006	0.0006
	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0005	0.0005	0.0005	0.0006
B	0.0005	0.0005	0.0006	0.0006
C	0.0005	0.0005	0.0006	0.0006
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0021	0.0022	0.0024	0.0026
B	0.0022	0.0023	0.0025	0.0027

C	0.0019	0.0020	0.0022	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0346	0.0397	0.8341	0.8921
A to Z ↑	0.0344	0.0392	1.0241	1.1567
B to Z ↓	0.0364	0.0416	0.8343	0.8922
B to Z ↑	0.0334	0.0382	1.0237	1.1569
C to Z ↓	0.0309	0.0353	0.8335	0.8918
C to Z ↑	0.0298	0.0339	1.0247	1.1572
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0484	0.0568	0.9758	1.0510
A to Z ↑	0.0473	0.0548	1.3615	1.5526
B to Z ↓	0.0503	0.0585	0.9752	1.0507
B to Z ↑	0.0461	0.0535	1.3614	1.5524
C to Z ↓	0.0427	0.0497	0.9755	1.0502
C to Z ↑	0.0407	0.0470	1.3598	1.5507
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0364	0.0420	0.6290	0.6728
A to Z ↑	0.0359	0.0411	0.7673	0.8667
B to Z ↓	0.0382	0.0439	0.6290	0.6731
B to Z ↑	0.0349	0.0400	0.7677	0.8671
C to Z ↓	0.0326	0.0376	0.6289	0.6729
C to Z ↑	0.0313	0.0357	0.7668	0.8676
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0512	0.0601	0.7359	0.7940
A to Z ↑	0.0494	0.0571	1.0202	1.1631
B to Z ↓	0.0531	0.0618	0.7368	0.7940
B to Z ↑	0.0482	0.0557	1.0206	1.1622
C to Z ↓	0.0455	0.0529	0.7364	0.7934
C to Z ↑	0.0427	0.0492	1.0191	1.1640
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0192	0.0221	0.5164	0.5559
A to Z ↑	0.0206	0.0233	0.4868	0.5503
B to Z ↓	0.0201	0.0229	0.5163	0.5560
B to Z ↑	0.0192	0.0217	0.4854	0.5493
C to Z ↓	0.0159	0.0182	0.5125	0.5515
C to Z ↑	0.0156	0.0176	0.4883	0.5522
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0269	0.0315	0.6139	0.6665
A to Z ↑	0.0274	0.0313	0.6472	0.7390
B to Z ↓	0.0272	0.0313	0.6138	0.6664
B to Z ↑	0.0255	0.0290	0.6463	0.7388
C to Z ↓	0.0217	0.0248	0.6080	0.6595
C to Z ↑	0.0205	0.0231	0.6489	0.7410

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X14_P0	1.107e-03	1.000e-20
X14_P4	3.061e-04	1.000e-20

X14_P10	7.854e-05	1.000e-20
X14_P16	3.362e-05	1.000e-20
X19_P0	1.206e-03	1.000e-20
X19_P4	3.360e-04	1.000e-20
X19_P10	8.684e-05	1.000e-20
X19_P16	3.728e-05	1.000e-20
X27_P0	2.205e-03	1.000e-20
X27_P4	5.968e-04	1.000e-20
X27_P10	1.488e-04	1.000e-20
X27_P16	6.281e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	7.540e-04	7.110e-04	7.073e-04	7.262e-04
B (output stable)	7.171e-04	6.781e-04	6.684e-04	6.799e-04
C (output stable)	2.105e-03	1.845e-03	1.692e-03	1.641e-03
A to Z	1.078e-02	1.022e-02	1.024e-02	1.042e-02
B to Z	1.066e-02	1.009e-02	1.009e-02	1.025e-02
C to Z	1.045e-02	9.814e-03	9.745e-03	9.862e-03
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	7.539e-04	7.113e-04	7.075e-04	7.270e-04
B (output stable)	7.166e-04	6.780e-04	6.686e-04	6.802e-04
C (output stable)	2.104e-03	1.844e-03	1.693e-03	1.642e-03
A to Z	1.280e-02	1.218e-02	1.206e-02	1.218e-02
B to Z	1.268e-02	1.205e-02	1.192e-02	1.201e-02
C to Z	1.246e-02	1.177e-02	1.157e-02	1.162e-02
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	3.424e-03	3.227e-03	3.233e-03	3.352e-03
B (output stable)	3.203e-03	3.018e-03	2.967e-03	3.009e-03
C (output stable)	7.494e-03	6.622e-03	6.150e-03	6.152e-03
A to Z	2.047e-02	1.888e-02	1.843e-02	1.871e-02
B to Z	1.935e-02	1.773e-02	1.710e-02	1.720e-02
C to Z	1.590e-02	1.413e-02	1.320e-02	1.295e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

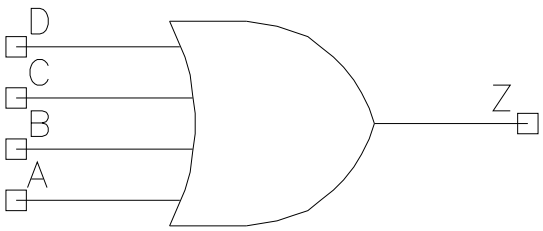
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR4

Cell Description

4 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	0.800	2.448	1.9584
X19_P4	0.800	2.448	1.9584
X19_P10	0.800	2.448	1.9584
X19_P16	0.800	2.448	1.9584
X27_P0	1.600	2.584	4.1344
X27_P4	1.600	2.584	4.1344
X27_P10	1.600	2.584	4.1344
X27_P16	1.600	2.584	4.1344

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0005	0.0005	0.0005	0.0006
B	0.0005	0.0005	0.0006	0.0006
C	0.0006	0.0006	0.0006	0.0007
D	0.0005	0.0005	0.0005	0.0006
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0022	0.0023	0.0026	0.0027
B	0.0020	0.0022	0.0023	0.0025
C	0.0022	0.0023	0.0025	0.0026
D	0.0021	0.0022	0.0024	0.0026

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0371	0.0427	0.6289	0.6731
A to Z ↑	0.0321	0.0368	0.7673	0.8657
B to Z ↓	0.0389	0.0446	0.6288	0.6733
B to Z ↑	0.0311	0.0358	0.7667	0.8664
C to Z ↓	0.0364	0.0417	0.6291	0.6728
C to Z ↑	0.0292	0.0337	0.7670	0.8652
D to Z ↓	0.0379	0.0433	0.6287	0.6735
D to Z ↑	0.0282	0.0325	0.7664	0.8654
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0518	0.0609	0.7370	0.7944
A to Z ↑	0.0442	0.0512	1.0177	1.1617
B to Z ↓	0.0537	0.0626	0.7365	0.7945
B to Z ↑	0.0429	0.0498	1.0186	1.1612
C to Z ↓	0.0504	0.0591	0.7368	0.7944
C to Z ↑	0.0404	0.0468	1.0188	1.1617
D to Z ↓	0.0520	0.0605	0.7364	0.7940
D to Z ↑	0.0391	0.0454	1.0183	1.1615
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0177	0.0206	0.5203	0.5603
A to Z ↑	0.0209	0.0235	0.4915	0.5555
B to Z ↓	0.0198	0.0226	0.5200	0.5603
B to Z ↑	0.0186	0.0210	0.4912	0.5546
C to Z ↓	0.0178	0.0203	0.5193	0.5592
C to Z ↑	0.0192	0.0215	0.4929	0.5569
D to Z ↓	0.0187	0.0211	0.5187	0.5586
D to Z ↑	0.0175	0.0195	0.4924	0.5560
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0251	0.0295	0.6185	0.6719
A to Z ↑	0.0275	0.0313	0.6527	0.7442
B to Z ↓	0.0268	0.0309	0.6185	0.6720
B to Z ↑	0.0247	0.0282	0.6511	0.7440
C to Z ↓	0.0246	0.0288	0.6173	0.6706
C to Z ↑	0.0251	0.0285	0.6544	0.7474
D to Z ↓	0.0249	0.0286	0.6170	0.6702
D to Z ↑	0.0226	0.0256	0.6532	0.7451

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X19_P0	1.097e-03	1.000e-20
X19_P4	3.062e-04	1.000e-20
X19_P10	7.950e-05	1.000e-20
X19_P16	3.438e-05	1.000e-20
X27_P0	2.064e-03	1.000e-20
X27_P4	5.657e-04	1.000e-20
X27_P10	1.433e-04	1.000e-20
X27_P16	6.147e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	9.265e-04	8.660e-04	8.521e-04	8.685e-04

B (output stable)	8.784e-04	8.192e-04	7.972e-04	8.039e-04
C (output stable)	7.955e-04	7.188e-04	6.836e-04	6.800e-04
D (output stable)	7.479e-04	6.708e-04	6.258e-04	6.133e-04
A to Z	1.192e-02	1.138e-02	1.122e-02	1.140e-02
B to Z	1.179e-02	1.125e-02	1.108e-02	1.123e-02
C to Z	1.147e-02	1.092e-02	1.074e-02	1.089e-02
D to Z	1.139e-02	1.083e-02	1.063e-02	1.076e-02
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	4.281e-03	4.022e-03	4.003e-03	4.132e-03
B (output stable)	3.869e-03	3.638e-03	3.579e-03	3.648e-03
C (output stable)	3.854e-03	3.542e-03	3.446e-03	3.542e-03
D (output stable)	3.534e-03	3.216e-03	3.037e-03	3.054e-03
A to Z	2.010e-02	1.846e-02	1.793e-02	1.813e-02
B to Z	1.874e-02	1.718e-02	1.656e-02	1.663e-02
C to Z	1.792e-02	1.603e-02	1.517e-02	1.511e-02
D to Z	1.677e-02	1.487e-02	1.384e-02	1.361e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

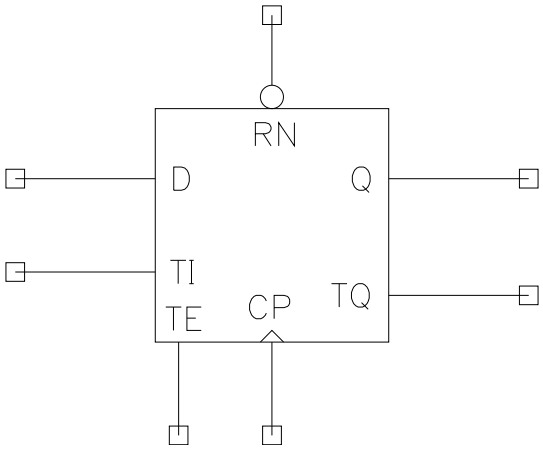
Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNSDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	1.600	2.176	3.4816
X9_P4	1.600	2.176	3.4816
X9_P10	1.600	2.176	3.4816
X9_P16	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
CP	0.0005	0.0006	0.0006	0.0006
D	0.0005	0.0005	0.0006	0.0006
RN	0.0008	0.0008	0.0009	0.0010

TE	0.0008	0.0009	0.0010	0.0010
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	X9_P4	X9_P0	X9_P4
CP to Q ↓	0.0509	0.0580	1.2966	1.3883
CP to Q ↑	0.0527	0.0604	1.4540	1.6474
CP to TQ ↓	0.0517	0.0591	4.4114	4.7050
CP to TQ ↑	0.0551	0.0632	7.2799	8.2292
RN to Q ↓	0.0487	0.0559	1.2961	1.3886
RN to TQ ↓	0.0495	0.0570	4.4117	4.7061
	X9_P10	X9_P16	X9_P10	X9_P16
CP to Q ↓	0.0695	0.0807	1.5185	1.6364
CP to Q ↑	0.0726	0.0843	1.9479	2.2259
CP to TQ ↓	0.0708	0.0823	5.1211	5.4911
CP to TQ ↑	0.0759	0.0881	9.6941	11.0962
RN to Q ↓	0.0673	0.0785	1.5180	1.6355
RN to TQ ↓	0.0687	0.0802	5.1203	5.4905

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X9_P0	X9_P4	X9_P10	X9_P16
CP ↓	min_pulse_width to CP	0.0374	0.0443	0.0583	0.0700
CP ↑	min_pulse_width to CP	0.0315	0.0314	0.0360	0.0406
D ↓	hold_rising to CP	0.0080	0.0052	0.0003	-0.0055
D ↑	hold_rising to CP	0.0080	0.0058	0.0005	-0.0049
D ↓	setup_rising to CP	0.0218	0.0267	0.0343	0.0445
D ↑	setup_rising to CP	0.0195	0.0223	0.0239	0.0298
RN ↓	min_pulse_width to RN	0.0327	0.0398	0.0447	0.0518
RN ↑	recovery_rising to CP	0.0026	0.0054	0.0081	0.0103
RN ↑	removal_rising to CP	0.0021	0.0025	-0.0001	-0.0033
TE ↓	hold_rising to CP	0.0123	0.0070	0.0048	-0.0001
TE ↑	hold_rising to CP	-0.0027	-0.0017	-0.0076	-0.0125
TE ↓	setup_rising to CP	0.0296	0.0313	0.0361	0.0415
TE ↑	setup_rising to CP	0.0401	0.0462	0.0640	0.0786
TI ↓	hold_rising to CP	-0.0104	-0.0166	-0.0280	-0.0377
TI ↑	hold_rising to CP	-0.0031	-0.0037	-0.0092	-0.0141
TI ↓	setup_rising to CP	0.0403	0.0516	0.0626	0.0772
TI ↑	setup_rising to CP	0.0280	0.0286	0.0332	0.0397

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X9_P0	1.806e-03	1.000e-20
X9_P4	4.707e-04	1.000e-20
X9_P10	1.158e-04	1.000e-20
X9_P16	4.939e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

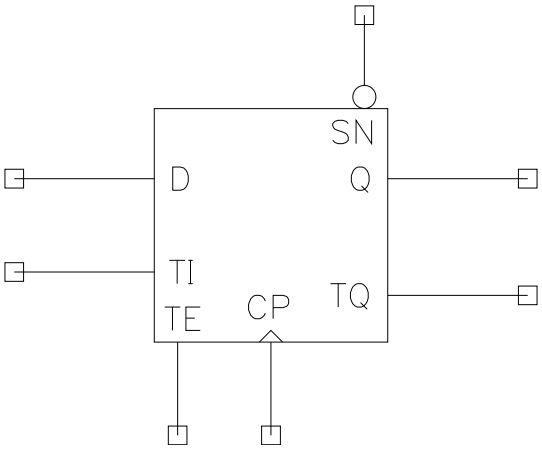
Pin Cycle	X9_P0	X9_P4	X9_P10	X9_P16
Clock 100Mhz Data 0Mhz	9.627e-03	9.411e-03	9.319e-03	9.323e-03
Clock 100Mhz Data 25Mhz	1.030e-02	1.004e-02	1.000e-02	1.010e-02
Clock 100Mhz Data 50Mhz	1.096e-02	1.068e-02	1.069e-02	1.087e-02
Clock = 0 Data 100Mhz	4.116e-03	4.079e-03	4.101e-03	4.156e-03
Clock = 1 Data 100Mhz	4.700e-05	4.417e-05	4.174e-05	4.012e-05

CNSDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	1.600	2.176	3.4816
X9_P4	1.600	2.176	3.4816
X9_P10	1.600	2.176	3.4816
X9_P16	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
CP	0.0005	0.0006	0.0006	0.0006
D	0.0003	0.0003	0.0004	0.0004
SN	0.0008	0.0009	0.0010	0.0010

TE	0.0009	0.0009	0.0010	0.0011
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	X9_P4	X9_P0	X9_P4
CP to Q ↓	0.0505	0.0577	1.2982	1.3875
CP to Q ↑	0.0513	0.0589	1.4573	1.6510
CP to TQ ↓	0.0513	0.0586	4.4182	4.7113
CP to TQ ↑	0.0535	0.0615	7.2650	8.2114
SN to Q ↑	0.0401	0.0461	1.4572	1.6519
SN to TQ ↑	0.0423	0.0487	7.2614	8.2117
	X9_P10	X9_P16	X9_P10	X9_P16
CP to Q ↓	0.0691	0.0803	1.5156	1.6305
CP to Q ↑	0.0709	0.0827	1.9492	2.2283
CP to TQ ↓	0.0703	0.0818	5.1269	5.4964
CP to TQ ↑	0.0741	0.0864	9.6730	11.0746
SN to Q ↑	0.0554	0.0646	1.9505	2.2308
SN to TQ ↑	0.0586	0.0683	9.6704	11.0691

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X9_P0	X9_P4	X9_P10	X9_P16
CP ↓	min_pulse_width to CP	0.0404	0.0497	0.0638	0.0755
CP ↑	min_pulse_width to CP	0.0314	0.0315	0.0361	0.0407
D ↓	hold_rising to CP	0.0053	-0.0001	-0.0050	-0.0072
D ↑	hold_rising to CP	0.0058	0.0026	-0.0023	-0.0045
D ↓	setup_rising to CP	0.0246	0.0321	0.0392	0.0494
D ↑	setup_rising to CP	0.0223	0.0244	0.0298	0.0347
SN ↓	min_pulse_width to SN	0.0327	0.0376	0.0398	0.0469
SN ↑	recovery_rising to CP	-0.0097	-0.0071	-0.0071	-0.0039
SN ↑	removal_rising to CP	0.0209	0.0236	0.0290	0.0284
TE ↓	hold_rising to CP	0.0075	0.0054	-0.0001	-0.0050
TE ↑	hold_rising to CP	0.0027	0.0032	-0.0017	-0.0076
TE ↓	setup_rising to CP	0.0270	0.0287	0.0394	0.0441
TE ↑	setup_rising to CP	0.0471	0.0569	0.0715	0.0835
TI ↓	hold_rising to CP	-0.0166	-0.0224	-0.0329	-0.0426
TI ↑	hold_rising to CP	0.0040	0.0027	-0.0037	-0.0092
TI ↓	setup_rising to CP	0.0466	0.0564	0.0710	0.0821
TI ↑	setup_rising to CP	0.0208	0.0280	0.0329	0.0332

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X9_P0	1.645e-03	1.000e-20
X9_P4	4.362e-04	1.000e-20
X9_P10	1.100e-04	1.000e-20
X9_P16	4.784e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

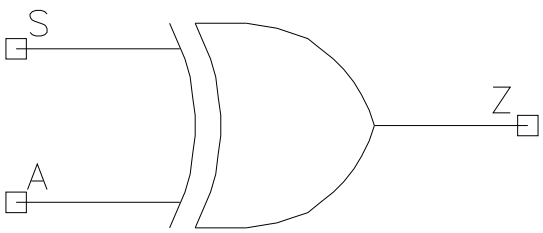
Pin Cycle	X9_P0	X9_P4	X9_P10	X9_P16
Clock 100Mhz Data 0Mhz	9.479e-03	9.266e-03	9.176e-03	9.181e-03
Clock 100Mhz Data 25Mhz	1.021e-02	9.968e-03	9.934e-03	1.003e-02
Clock 100Mhz Data 50Mhz	1.095e-02	1.067e-02	1.069e-02	1.089e-02
Clock = 0 Data 100Mhz	4.349e-03	4.301e-03	4.310e-03	4.353e-03
Clock = 1 Data 100Mhz	4.632e-05	4.324e-05	4.060e-05	3.895e-05

CNXOR2

Cell Description

2 input Exclusive OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	1.496	1.1968
X9_P4	0.800	1.496	1.1968
X9_P10	0.800	1.496	1.1968
X9_P16	0.800	1.496	1.1968
X15_P0	0.800	2.312	1.8496
X15_P4	0.800	2.312	1.8496
X15_P10	0.800	2.312	1.8496
X15_P16	0.800	2.312	1.8496
X27_P0	0.800	2.584	2.0672
X27_P4	0.800	2.584	2.0672
X27_P10	0.800	2.584	2.0672
X27_P16	0.800	2.584	2.0672

Truth Table

A	S	Z
1	S	!S
0	S	S

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
A	0.0007	0.0007	0.0008	0.0008
S	0.0014	0.0014	0.0015	0.0016
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0013	0.0013	0.0014	0.0015
S	0.0021	0.0022	0.0024	0.0025
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0011	0.0012	0.0013	0.0014
S	0.0021	0.0022	0.0024	0.0025

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
A to Z ↓	0.0238	0.0273	1.3493	1.4450
A to Z ↑	0.0239	0.0270	1.6302	1.8375
S to Z ↓	0.0189	0.0215	1.3435	1.4392
S to Z ↑	0.0185	0.0211	1.6290	1.8361
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
A to Z ↓	0.0328	0.0381	1.5864	1.7133
A to Z ↑	0.0317	0.0363	2.1614	2.4667
S to Z ↓	0.0253	0.0290	1.5789	1.7065
S to Z ↑	0.0250	0.0286	2.1605	2.4655
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0224	0.0257	0.8456	0.9054
A to Z ↑	0.0220	0.0250	0.8572	0.9706
S to Z ↓	0.0168	0.0192	0.8445	0.9035
S to Z ↑	0.0160	0.0183	0.8562	0.9692
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0309	0.0358	0.9926	1.0709
A to Z ↑	0.0297	0.0340	1.1450	1.3085
S to Z ↓	0.0228	0.0261	0.9901	1.0686
S to Z ↑	0.0217	0.0249	1.1435	1.3066
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0270	0.0309	0.4852	0.5202
A to Z ↑	0.0275	0.0310	0.5183	0.5869
S to Z ↓	0.0211	0.0240	0.4847	0.5198
S to Z ↑	0.0207	0.0235	0.5182	0.5868
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0371	0.0431	0.5718	0.6190
A to Z ↑	0.0368	0.0422	0.6926	0.7910
S to Z ↓	0.0286	0.0330	0.5711	0.6183
S to Z ↑	0.0279	0.0320	0.6919	0.7907

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X9_P0	1.409e-03	1.000e-20
X9_P4	3.645e-04	1.000e-20
X9_P10	8.572e-05	1.000e-20
X9_P16	3.436e-05	1.000e-20
X15_P0	2.538e-03	1.000e-20
X15_P4	6.483e-04	1.000e-20
X15_P10	1.502e-04	1.000e-20
X15_P16	5.962e-05	1.000e-20
X27_P0	3.095e-03	1.000e-20
X27_P4	7.819e-04	1.000e-20
X27_P10	1.789e-04	1.000e-20
X27_P16	7.048e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
A to Z	8.132e-03	7.422e-03	7.046e-03	7.006e-03
S to Z	7.603e-03	6.726e-03	6.206e-03	6.076e-03
	X15_P0	X15_P4	X15_P10	X15_P16

A to Z	1.469e-02	1.334e-02	1.262e-02	1.247e-02
S to Z	1.209e-02	1.037e-02	9.276e-03	8.879e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	2.125e-02	1.909e-02	1.791e-02	1.761e-02
S to Z	1.920e-02	1.661e-02	1.502e-02	1.447e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

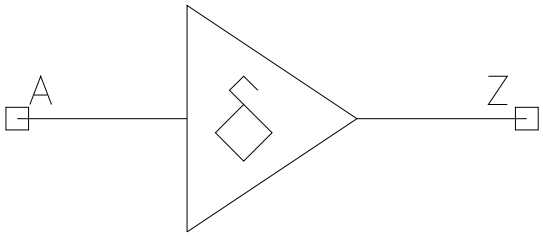
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DLYHF

Cell Description

Delay cell for Hold Time Fixing

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-DLYHFM4X4_P0	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X4_P4	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X4_P10	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X4_P16	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X12_P0	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM4X12_P4	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM4X12_P10	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM4X12_P16	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM8X4_P0	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X4_P4	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X4_P10	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X4_P16	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X12_P0	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X12_P4	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X12_P10	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X12_P16	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X30_P0	0.800	5.848	4.6784

C8T28SOI_LL_-DLYHFM8X30_P4	0.800	5.848	4.6784
C8T28SOI_LL_-DLYHFM8X30_P10	0.800	5.848	4.6784
C8T28SOI_LL_-DLYHFM8X30_P16	0.800	5.848	4.6784

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C8T28SOI_LL_-DLYHFM4X4_P0	C8T28SOI_LL_-DLYHFM4X4_P4	C8T28SOI_LL_-DLYHFM4X4_P10	C8T28SOI_LL_-DLYHFM4X4_P16
A	0.0009	0.0009	0.0009	0.0010
	C8T28SOI_LL_-DLYHFM4X12_P0	C8T28SOI_LL_-DLYHFM4X12_P4	C8T28SOI_LL_-DLYHFM4X12_P10	C8T28SOI_LL_-DLYHFM4X12_P16
A	0.0008	0.0009	0.0009	0.0010
	C8T28SOI_LL_-DLYHFM8X4_P0	C8T28SOI_LL_-DLYHFM8X4_P4	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A	0.0008	0.0008	0.0008	0.0009
	C8T28SOI_LL_-DLYHFM8X12_P0	C8T28SOI_LL_-DLYHFM8X12_P4	C8T28SOI_LL_-DLYHFM8X12_P10	C8T28SOI_LL_-DLYHFM8X12_P16
A	0.0007	0.0008	0.0008	0.0008
	C8T28SOI_LL_-DLYHFM8X30_P0	C8T28SOI_LL_-DLYHFM8X30_P4	C8T28SOI_LL_-DLYHFM8X30_P10	C8T28SOI_LL_-DLYHFM8X30_P16
A	0.0007	0.0008	0.0008	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-DLYHFM4X4_P0	**C8T28SOI_LL_-DLYHFM4X4_P4**	**C8T28SOI_LL_-DLYHFM4X4_P0**	**C8T28SOI_LL_-DLYHFM4X4_P4**
A to Z ↓	0.0528	0.0606	2.9980	3.2144
A to Z ↑	0.0504	0.0579	3.0373	3.4515
	C8T28SOI_LL_-DLYHFM4X4_P10	**C8T28SOI_LL_-DLYHFM4X4_P16**	**C8T28SOI_LL_-DLYHFM4X4_P10**	**C8T28SOI_LL_-DLYHFM4X4_P16**
A to Z ↓	0.0730	0.0853	3.5205	3.7922
A to Z ↑	0.0699	0.0818	4.0756	4.6686
	C8T28SOI_LL_-DLYHFM4X12_P0	**C8T28SOI_LL_-DLYHFM4X12_P4**	**C8T28SOI_LL_-DLYHFM4X12_P0**	**C8T28SOI_LL_-DLYHFM4X12_P4**
A to Z ↓	0.0600	0.0693	1.0504	1.1300
A to Z ↑	0.0571	0.0658	1.1467	1.3016
	C8T28SOI_LL_-DLYHFM4X12_P10	**C8T28SOI_LL_-DLYHFM4X12_P16**	**C8T28SOI_LL_-DLYHFM4X12_P10**	**C8T28SOI_LL_-DLYHFM4X12_P16**
A to Z ↓	0.0840	0.0989	1.2456	1.3504
A to Z ↑	0.0795	0.0931	1.5406	1.7641
	C8T28SOI_LL_-DLYHFM8X4_P0	**C8T28SOI_LL_-DLYHFM8X4_P4**	**C8T28SOI_LL_-DLYHFM8X4_P0**	**C8T28SOI_LL_-DLYHFM8X4_P4**
A to Z ↓	0.1006	0.1166	2.9937	3.2098
A to Z ↑	0.0960	0.1097	2.9909	3.3850

	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A to Z ↓	0.1429	0.1697	3.5111	3.7857
A to Z ↑	0.1316	0.1534	4.0054	4.5809
	C8T28SOI_LL_-DLYHFM8X12_P0	**C8T28SOI_LL_-DLYHFM8X12_P4**	**C8T28SOI_LL_-DLYHFM8X12_P0**	**C8T28SOI_LL_-DLYHFM8X12_P4**
A to Z ↓	0.1081	0.1254	1.0428	1.1218
A to Z ↑	0.1031	0.1179	1.1432	1.2991
	C8T28SOI_LL_-DLYHFM8X12_P10	**C8T28SOI_LL_-DLYHFM8X12_P16**	**C8T28SOI_LL_-DLYHFM8X12_P10**	**C8T28SOI_LL_-DLYHFM8X12_P16**
A to Z ↓	0.1541	0.1834	1.2360	1.3385
A to Z ↑	0.1417	0.1654	1.5355	1.7583
	C8T28SOI_LL_-DLYHFM8X30_P0	**C8T28SOI_LL_-DLYHFM8X30_P4**	**C8T28SOI_LL_-DLYHFM8X30_P0**	**C8T28SOI_LL_-DLYHFM8X30_P4**
A to Z ↓	0.1389	0.1612	0.4056	0.4347
A to Z ↑	0.1415	0.1635	0.4609	0.5225
	C8T28SOI_LL_-DLYHFM8X30_P10	**C8T28SOI_LL_-DLYHFM8X30_P16**	**C8T28SOI_LL_-DLYHFM8X30_P10**	**C8T28SOI_LL_-DLYHFM8X30_P16**
A to Z ↓	0.1976	0.2348	0.4767	0.5146
A to Z ↑	0.1991	0.2351	0.6162	0.7052

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_DLYHFM4X4_P0	2.545e-04	1.000e-20
C8T28SOI_LL_DLYHFM4X4_P4	6.947e-05	1.000e-20
C8T28SOI_LL_DLYHFM4X4_P10	1.834e-05	1.000e-20
C8T28SOI_LL_DLYHFM4X4_P16	8.546e-06	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P0	5.994e-04	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P4	1.561e-04	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P10	3.828e-05	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P16	1.651e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P0	3.860e-04	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P4	1.134e-04	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P10	3.420e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P16	1.822e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P0	7.098e-04	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P4	1.939e-04	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P10	5.253e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P16	2.549e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P0	1.708e-03	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P4	4.590e-04	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P10	1.191e-04	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P16	5.496e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_-DLYHFM4X4_P0	C8T28SOI_LL_-DLYHFM4X4_P4	C8T28SOI_LL_-DLYHFM4X4_P10	C8T28SOI_LL_-DLYHFM4X4_P16
A to Z	5.314e-03	5.265e-03	5.390e-03	5.601e-03
	C8T28SOI_LL_-DLYHFM4X12_P0	C8T28SOI_LL_-DLYHFM4X12_P4	C8T28SOI_LL_-DLYHFM4X12_P10	C8T28SOI_LL_-DLYHFM4X12_P16
A to Z	9.947e-03	9.439e-03	9.273e-03	9.405e-03

	C8T28SOI_LL_-DLYHFM8X4_P0	C8T28SOI_LL_-DLYHFM8X4_P4	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A to Z	1.631e-02	1.621e-02	1.671e-02	1.742e-02
	C8T28SOI_LL_-DLYHFM8X12_P0	C8T28SOI_LL_-DLYHFM8X12_P4	C8T28SOI_LL_-DLYHFM8X12_P10	C8T28SOI_LL_-DLYHFM8X12_P16
A to Z	2.014e-02	1.962e-02	1.985e-02	2.047e-02
	C8T28SOI_LL_-DLYHFM8X30_P0	C8T28SOI_LL_-DLYHFM8X30_P4	C8T28SOI_LL_-DLYHFM8X30_P10	C8T28SOI_LL_-DLYHFM8X30_P16
A to Z	3.679e-02	3.597e-02	3.644e-02	3.766e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

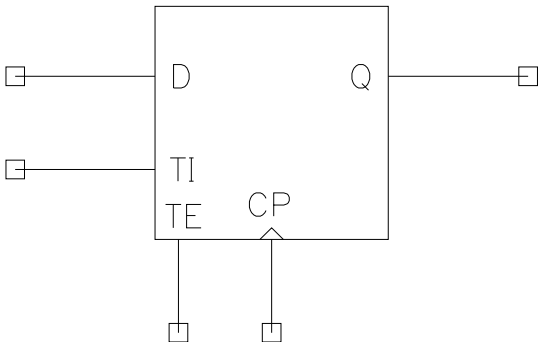
Pin Cycle (vdds)	C8T28SOI_LL_-DLYHFM4X4_P0	C8T28SOI_LL_-DLYHFM4X4_P4	C8T28SOI_LL_-DLYHFM4X4_P10	C8T28SOI_LL_-DLYHFM4X4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM4X12_P0	C8T28SOI_LL_-DLYHFM4X12_P4	C8T28SOI_LL_-DLYHFM4X12_P10	C8T28SOI_LL_-DLYHFM4X12_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM8X4_P0	C8T28SOI_LL_-DLYHFM8X4_P4	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM8X12_P0	C8T28SOI_LL_-DLYHFM8X12_P4	C8T28SOI_LL_-DLYHFM8X12_P10	C8T28SOI_LL_-DLYHFM8X12_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM8X30_P0	C8T28SOI_LL_-DLYHFM8X30_P4	C8T28SOI_LL_-DLYHFM8X30_P10	C8T28SOI_LL_-DLYHFM8X30_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFSYNCPQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	1.600	3.264	5.2224
C8T28SOIDV_LL1_-SDFSYNCPQX5_P4	1.600	3.264	5.2224
C8T28SOIDV_LL1_-SDFSYNCPQX5_P10	1.600	3.264	5.2224
C8T28SOIDV_LL1_-SDFSYNCPQX5_P16	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P0	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P4	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P10	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P16	1.600	3.264	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	C8T28SOIDV_LL1_-SDFSYNCPQX5_P4	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16
CP	0.0007	0.0007	0.0008	0.0008
D	0.0010	0.0010	0.0011	0.0012
TE	0.0009	0.0009	0.0010	0.0011
TI	0.0004	0.0004	0.0004	0.0005
	C8T28SOIDV_LL_-SDFSYNCPQX5_P0	C8T28SOIDV_LL_-SDFSYNCPQX5_P4	C8T28SOIDV_LL_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPQX5_-P16
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0006
TE	0.0008	0.0009	0.0010	0.0010
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	**C8T28SOIDV_LL1_-SDFSYNCPQX5_P4**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_P0**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_P4**
CP to Q ↓	0.0537	0.0618	2.6529	2.8934
CP to Q ↑	0.0662	0.0756	3.0263	3.4522
	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10	**C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16**
CP to Q ↓	0.0746	0.0869	3.2505	3.5871
CP to Q ↑	0.0910	0.1063	4.0986	4.7053
	C8T28SOIDV_LL_-SDFSYNCPQX5_P0	**C8T28SOIDV_LL_-SDFSYNCPQX5_P4**	**C8T28SOIDV_LL_-SDFSYNCPQX5_P0**	**C8T28SOIDV_LL_-SDFSYNCPQX5_P4**
CP to Q ↓	0.0777	0.0905	2.7837	3.0743
CP to Q ↑	0.1018	0.1165	3.0580	3.4891
	C8T28SOIDV_LL_-SDFSYNCPQX5_-P10	**C8T28SOIDV_LL_-SDFSYNCPQX5_-P16**	**C8T28SOIDV_LL_-SDFSYNCPQX5_-P10**	**C8T28SOIDV_LL_-SDFSYNCPQX5_-P16**
CP to Q ↓	0.1098	0.1284	3.4919	3.8900
CP to Q ↑	0.1412	0.1662	4.1470	4.7641

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P0	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P4	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P10	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P16
CP ↓	min_pulse_width to CP	0.0679	0.0819	0.1030	0.1259
CP ↑	min_pulse_width to CP	0.0455	0.0501	0.0594	0.0687
D ↓	hold_rising to CP	-0.0072	-0.0098	-0.0196	-0.0245
D ↑	hold_rising to CP	0.0005	-0.0023	-0.0039	-0.0098
D ↓	setup_rising to CP	0.0338	0.0445	0.0543	0.0689
D ↑	setup_rising to CP	0.0244	0.0272	0.0320	0.0341
TE ↓	hold_rising to CP	-0.0045	-0.0121	-0.0170	-0.0273
TE ↑	hold_rising to CP	-0.0141	-0.0190	-0.0239	-0.0342

TE ↓	setup_rising to CP	0.0386	0.0467	0.0564	0.0685
TE ↑	setup_rising to CP	0.0836	0.1031	0.1350	0.1616
TI ↓	hold_rising to CP	-0.0608	-0.0768	-0.0977	-0.1221
TI ↑	hold_rising to CP	-0.0147	-0.0195	-0.0257	-0.0321
TI ↓	setup_rising to CP	0.0906	0.1065	0.1358	0.1615
TI ↑	setup_rising to CP	0.0394	0.0443	0.0548	0.0626
		C8T28SOIDV_-LL_SDF-SYNCPQX5_P0	C8T28SOIDV_-LL_SDF-SYNCPQX5_P4	C8T28SOIDV_-LL_SDF-SYNCPQX5_P10	C8T28SOIDV_-LL_SDF-SYNCPQX5_P16
CP ↓	min_pulse_width to CP	0.1124	0.1424	0.1823	0.2210
CP ↑	min_pulse_width to CP	0.0688	0.0782	0.0922	0.1061
D ↓	hold_rising to CP	-0.0196	-0.0294	-0.0414	-0.0512
D ↑	hold_rising to CP	-0.0288	-0.0342	-0.0381	-0.0488
D ↓	setup_rising to CP	0.0591	0.0737	0.0959	0.1154
D ↑	setup_rising to CP	0.0568	0.0585	0.0688	0.0785
TE ↓	hold_rising to CP	-0.0121	-0.0219	-0.0375	-0.0490
TE ↑	hold_rising to CP	-0.0457	-0.0505	-0.0629	-0.0759
TE ↓	setup_rising to CP	0.0637	0.0745	0.0934	0.1134
TE ↑	setup_rising to CP	0.0986	0.1253	0.1621	0.1962
TI ↓	hold_rising to CP	-0.0560	-0.0755	-0.1012	-0.1257
TI ↑	hold_rising to CP	-0.0474	-0.0539	-0.0650	-0.0790
TI ↓	setup_rising to CP	0.0990	0.1247	0.1604	0.1894
TI ↑	setup_rising to CP	0.0772	0.0844	0.0947	0.1087

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL1_SDFSYNCPQX5_-P0	2.543e-03	1.000e-20
C8T28SOIDV_LL1_SDFSYNCPQX5_-P4	6.702e-04	1.000e-20
C8T28SOIDV_LL1_SDFSYNCPQX5_-P10	1.656e-04	1.000e-20
C8T28SOIDV_LL1_SDFSYNCPQX5_-P16	7.109e-05	1.000e-20
C8T28SOIDV_LL_SDFSYNCPQX5_-P0	2.624e-03	1.000e-20
C8T28SOIDV_LL_SDFSYNCPQX5_-P4	6.847e-04	1.000e-20
C8T28SOIDV_LL_SDFSYNCPQX5_-P10	1.669e-04	1.000e-20

C8T28SOIDV_LL_SDFSYNCPQX5_-P16	7.089e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

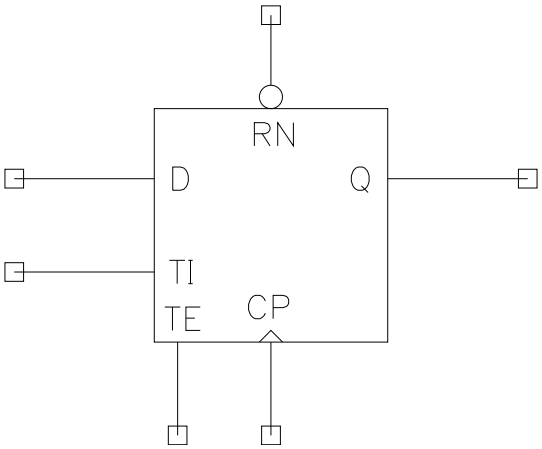
Pin Cycle	C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	C8T28SOIDV_LL1_-SDFSYNCPQX5_P4	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16
Clock 100Mhz Data 0Mhz	1.995e-02	1.986e-02	2.006e-02	2.044e-02
Clock 100Mhz Data 25Mhz	2.164e-02	2.122e-02	2.122e-02	2.161e-02
Clock 100Mhz Data 50Mhz	2.334e-02	2.258e-02	2.237e-02	2.278e-02
Clock = 0 Data 100Mhz	1.277e-02	1.241e-02	1.225e-02	1.222e-02
Clock = 1 Data 100Mhz	1.027e-04	9.311e-05	8.748e-05	8.395e-05
	C8T28SOIDV_LL_-SDFSYNCPQX5_P0	C8T28SOIDV_LL_-SDFSYNCPQX5_P4	C8T28SOIDV_LL_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPQX5_-P16
Clock 100Mhz Data 0Mhz	2.027e-02	2.021e-02	2.034e-02	2.060e-02
Clock 100Mhz Data 25Mhz	2.341e-02	2.325e-02	2.336e-02	2.372e-02
Clock 100Mhz Data 50Mhz	2.655e-02	2.628e-02	2.637e-02	2.683e-02
Clock = 0 Data 100Mhz	1.432e-02	1.535e-02	1.589e-02	1.625e-02
Clock = 1 Data 100Mhz	7.470e-05	6.802e-05	6.266e-05	5.852e-05

SDFSYNCPRQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P0	1.600	3.944	6.3104
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P4	1.600	3.944	6.3104
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P10	1.600	3.944	6.3104
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P16	1.600	3.944	6.3104
C8T28SOIDV_LL_-SDFSYNCPRQX5_P0	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPRQX5_P4	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPRQX5_P10	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPRQX5_P16	1.600	4.080	6.5280

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI

-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16
CP	0.0007	0.0008	0.0008	0.0009
D	0.0010	0.0011	0.0011	0.0012
RN	0.0014	0.0014	0.0015	0.0016
TE	0.0009	0.0009	0.0010	0.0011
TI	0.0003	0.0003	0.0003	0.0004
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16
CP	0.0005	0.0005	0.0005	0.0005
D	0.0005	0.0005	0.0005	0.0006
RN	0.0020	0.0021	0.0023	0.0025
TE	0.0008	0.0009	0.0010	0.0010
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4**
CP to Q ↓	0.0602	0.0693	2.6505	2.8895
CP to Q ↑	0.0684	0.0781	3.0202	3.4441
RN to Q ↓	0.0462	0.0534	2.4372	2.6366
	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16**
CP to Q ↓	0.0834	0.0973	3.2460	3.5815
CP to Q ↑	0.0939	0.1095	4.0874	4.6905
RN to Q ↓	0.0646	0.0756	2.9233	3.1912
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4**
CP to Q ↓	0.0864	0.0997	2.7836	3.0687
CP to Q ↑	0.1073	0.1227	3.0628	3.4983
RN to Q ↓	0.0534	0.0617	2.4726	2.6817
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16**
CP to Q ↓	0.1200	0.1397	3.4868	3.8779
CP to Q ↑	0.1485	0.1745	4.1575	4.7689
RN to Q ↓	0.0751	0.0881	2.9868	3.2688

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P0	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P4	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P10	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P16
CP ↓	min_pulse_width to CP	0.0687	0.0827	0.1079	0.1330
CP ↑	min_pulse_width to CP	0.0531	0.0592	0.0686	0.0814
D ↓	hold_rising to CP	-0.0098	-0.0147	-0.0196	-0.0300
D ↑	hold_rising to CP	-0.0044	-0.0071	-0.0120	-0.0141
D ↓	setup_rising to CP	0.0370	0.0445	0.0591	0.0689
D ↑	setup_rising to CP	0.0292	0.0320	0.0395	0.0444
RN ↓	min_pulse_width to RN	0.0686	0.0784	0.0952	0.1099
RN ↑	recovery_rising to CP	0.0032	-0.0000	0.0005	0.0005
RN ↑	removal_rising to CP	0.0016	0.0048	0.0043	0.0043
TE ↓	hold_rising to CP	-0.0072	-0.0121	-0.0218	-0.0267
TE ↑	hold_rising to CP	-0.0218	-0.0271	-0.0342	-0.0391
TE ↓	setup_rising to CP	0.0409	0.0463	0.0565	0.0712
TE ↑	setup_rising to CP	0.0862	0.1057	0.1350	0.1665
TI ↓	hold_rising to CP	-0.0566	-0.0768	-0.0977	-0.1221
TI ↑	hold_rising to CP	-0.0238	-0.0259	-0.0364	-0.0410
TI ↓	setup_rising to CP	0.0863	0.1065	0.1358	0.1658
TI ↑	setup_rising to CP	0.0486	0.0551	0.0605	0.0710
		C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P0	C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P4	C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P10	C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P16
CP ↓	min_pulse_width to CP	0.1057	0.1311	0.1681	0.2027
CP ↑	min_pulse_width to CP	0.0734	0.0815	0.0967	0.1106
D ↓	hold_rising to CP	-0.0098	-0.0170	-0.0268	-0.0371
D ↑	hold_rising to CP	-0.0244	-0.0235	-0.0342	-0.0413
D ↓	setup_rising to CP	0.0461	0.0613	0.0791	0.0964
D ↑	setup_rising to CP	0.0487	0.0542	0.0616	0.0687
RN ↓	min_pulse_width to RN	0.0708	0.0806	0.1001	0.1147
RN ↑	recovery_rising to CP	0.0048	0.0028	0.0031	0.0005
RN ↑	removal_rising to CP	-0.0001	0.0020	0.0021	0.0047
TE ↓	hold_rising to CP	-0.0023	-0.0131	-0.0197	-0.0294
TE ↑	hold_rising to CP	-0.0409	-0.0466	-0.0560	-0.0684

TE ↓	setup_rising to CP	0.0556	0.0605	0.0735	0.0885
TE ↑	setup_rising to CP	0.0862	0.1106	0.1425	0.1714
TI ↓	hold_rising to CP	-0.0462	-0.0622	-0.0830	-0.1069
TI ↑	hold_rising to CP	-0.0448	-0.0497	-0.0592	-0.0706
TI ↓	setup_rising to CP	0.0857	0.1065	0.1414	0.1709
TI ↑	setup_rising to CP	0.0730	0.0795	0.0892	0.1005

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P0	2.811e-03	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P4	7.388e-04	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P10	1.829e-04	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P16	7.929e-05	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P0	2.784e-03	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P4	7.319e-04	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P10	1.808e-04	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P16	7.848e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16
Clock 100Mhz Data 0Mhz	2.150e-02	2.144e-02	2.169e-02	2.212e-02
Clock 100Mhz Data 25Mhz	2.361e-02	2.315e-02	2.318e-02	2.355e-02
Clock 100Mhz Data 50Mhz	2.572e-02	2.485e-02	2.466e-02	2.498e-02
Clock = 0 Data 100Mhz	1.527e-02	1.483e-02	1.459e-02	1.453e-02
Clock = 1 Data 100Mhz	9.432e-05	8.674e-05	8.189e-05	7.897e-05
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16
Clock 100Mhz Data 0Mhz	2.190e-02	2.182e-02	2.196e-02	2.225e-02
Clock 100Mhz Data 25Mhz	2.514e-02	2.480e-02	2.483e-02	2.513e-02

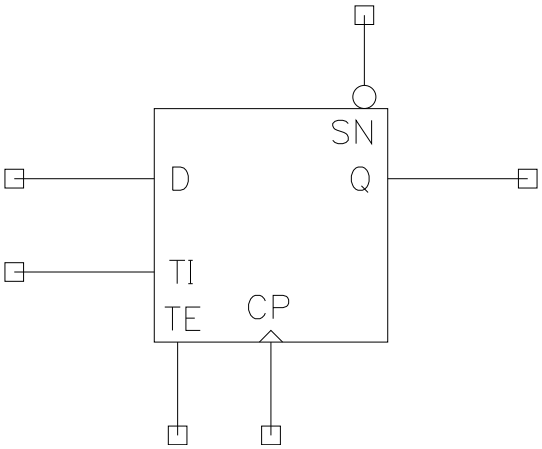
Clock 100Mhz Data 50Mhz	2.839e-02	2.779e-02	2.770e-02	2.802e-02
Clock = 0 Data 100Mhz	1.564e-02	1.610e-02	1.630e-02	1.644e-02
Clock = 1 Data 100Mhz	7.304e-05	6.818e-05	6.409e-05	6.084e-05

SDFSYNCPSQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P0	1.600	4.080	6.5280
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P4	1.600	4.080	6.5280
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P10	1.600	4.080	6.5280
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P16	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P0	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P4	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P10	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P16	1.600	4.080	6.5280

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI

-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16
CP	0.0006	0.0006	0.0007	0.0007
D	0.0007	0.0007	0.0008	0.0008
SN	0.0017	0.0018	0.0019	0.0020
TE	0.0009	0.0010	0.0011	0.0012
TI	0.0004	0.0004	0.0004	0.0004
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16
CP	0.0005	0.0005	0.0005	0.0005
D	0.0003	0.0004	0.0004	0.0004
SN	0.0015	0.0016	0.0017	0.0019
TE	0.0008	0.0009	0.0010	0.0010
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4**
CP to Q ↓	0.0655	0.0752	2.7862	3.0428
CP to Q ↑	0.0700	0.0801	3.0381	3.4662
SN to Q ↑	0.0591	0.0680	2.9250	3.3352
	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16**
CP to Q ↓	0.0898	0.1043	3.4151	3.7693
CP to Q ↑	0.0963	0.1119	4.1135	4.7192
SN to Q ↑	0.0821	0.0962	3.9569	4.5356
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4**
CP to Q ↓	0.0902	0.1040	2.8619	3.1590
CP to Q ↑	0.1098	0.1258	3.0836	3.5202
SN to Q ↑	0.0670	0.0763	2.8882	3.2994
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16**
CP to Q ↓	0.1249	0.1451	3.5844	3.9850
CP to Q ↑	0.1518	0.1780	4.1830	4.8008
SN to Q ↑	0.0911	0.0914	3.9256	4.5954

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P0	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P4	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P10	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P16
CP ↓	min_pulse_width to CP	0.0673	0.0814	0.1045	0.1250
CP ↑	min_pulse_width to CP	0.0547	0.0642	0.0735	0.0862
D ↓	hold_rising to CP	-0.0049	-0.0098	-0.0147	-0.0245
D ↑	hold_rising to CP	-0.0043	-0.0071	-0.0120	-0.0196
D ↓	setup_rising to CP	0.0348	0.0419	0.0543	0.0640
D ↑	setup_rising to CP	0.0292	0.0320	0.0395	0.0444
SN ↓	min_pulse_width to SN	0.0745	0.0842	0.0989	0.1135
SN ↑	recovery_rising to CP	-0.0110	-0.0110	-0.0115	-0.0115
SN ↑	removal_rising to CP	0.0279	0.0302	0.0352	0.0401
TE ↓	hold_rising to CP	-0.0049	-0.0098	-0.0170	-0.0241
TE ↑	hold_rising to CP	-0.0218	-0.0267	-0.0342	-0.0440
TE ↓	setup_rising to CP	0.0393	0.0468	0.0545	0.0663
TE ↑	setup_rising to CP	0.0862	0.1030	0.1323	0.1568
TI ↓	hold_rising to CP	-0.0559	-0.0719	-0.0928	-0.1121
TI ↑	hold_rising to CP	-0.0238	-0.0302	-0.0364	-0.0419
TI ↓	setup_rising to CP	0.0857	0.1016	0.1273	0.1569
TI ↑	setup_rising to CP	0.0502	0.0551	0.0605	0.0723
		C8T28SOIDV_-LL_SDFSYNCP-SQX5_P0	C8T28SOIDV_-LL_SDFSYNCP-SQX5_P4	C8T28SOIDV_-LL_SDFSYNCP-SQX5_P10	C8T28SOIDV_-LL_SDFSYNCP-SQX5_P16
CP ↓	min_pulse_width to CP	0.1117	0.1359	0.1745	0.2115
CP ↑	min_pulse_width to CP	0.0766	0.0859	0.1013	0.1188
D ↓	hold_rising to CP	-0.0115	-0.0192	-0.0290	-0.0361
D ↑	hold_rising to CP	-0.0244	-0.0235	-0.0338	-0.0407
D ↓	setup_rising to CP	0.0542	0.0661	0.0866	0.1003
D ↑	setup_rising to CP	0.0492	0.0542	0.0612	0.0714
SN ↓	min_pulse_width to SN	0.0757	0.0854	0.1050	0.1196
SN ↑	recovery_rising to CP	-0.0234	-0.0234	-0.0283	-0.0306
SN ↑	removal_rising to CP	0.0528	0.0572	0.0697	0.0795
TE ↓	hold_rising to CP	-0.0072	-0.0148	-0.0245	-0.0343
TE ↑	hold_rising to CP	-0.0413	-0.0462	-0.0586	-0.0684

TE ↓	setup_rising to CP	0.0560	0.0637	0.0787	0.0988
TE ↑	setup_rising to CP	0.0938	0.1213	0.1497	0.1812
TI ↓	hold_rising to CP	-0.0511	-0.0671	-0.0915	-0.1123
TI ↑	hold_rising to CP	-0.0448	-0.0497	-0.0608	-0.0703
TI ↓	setup_rising to CP	0.0955	0.1163	0.1514	0.1764
TI ↑	setup_rising to CP	0.0730	0.0795	0.0908	0.1002

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P0	2.590e-03	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P4	7.001e-04	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P10	1.790e-04	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P16	7.933e-05	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P0	2.606e-03	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P4	6.977e-04	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P10	1.763e-04	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P16	7.742e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16
Clock 100Mhz Data 0Mhz	2.021e-02	2.017e-02	2.041e-02	2.079e-02
Clock 100Mhz Data 25Mhz	2.305e-02	2.253e-02	2.248e-02	2.277e-02
Clock 100Mhz Data 50Mhz	2.590e-02	2.490e-02	2.456e-02	2.475e-02
Clock = 0 Data 100Mhz	1.453e-02	1.410e-02	1.387e-02	1.380e-02
Clock = 1 Data 100Mhz	9.773e-05	9.074e-05	8.551e-05	8.236e-05
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16
Clock 100Mhz Data 0Mhz	2.084e-02	2.095e-02	2.121e-02	2.159e-02
Clock 100Mhz Data 25Mhz	2.483e-02	2.464e-02	2.474e-02	2.512e-02

Clock 100Mhz Data 50Mhz	2.881e-02	2.833e-02	2.828e-02	2.866e-02
Clock = 0 Data 100Mhz	1.553e-02	1.636e-02	1.678e-02	1.706e-02
Clock = 1 Data 100Mhz	7.607e-05	7.075e-05	6.637e-05	6.283e-05

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