QRC user guide

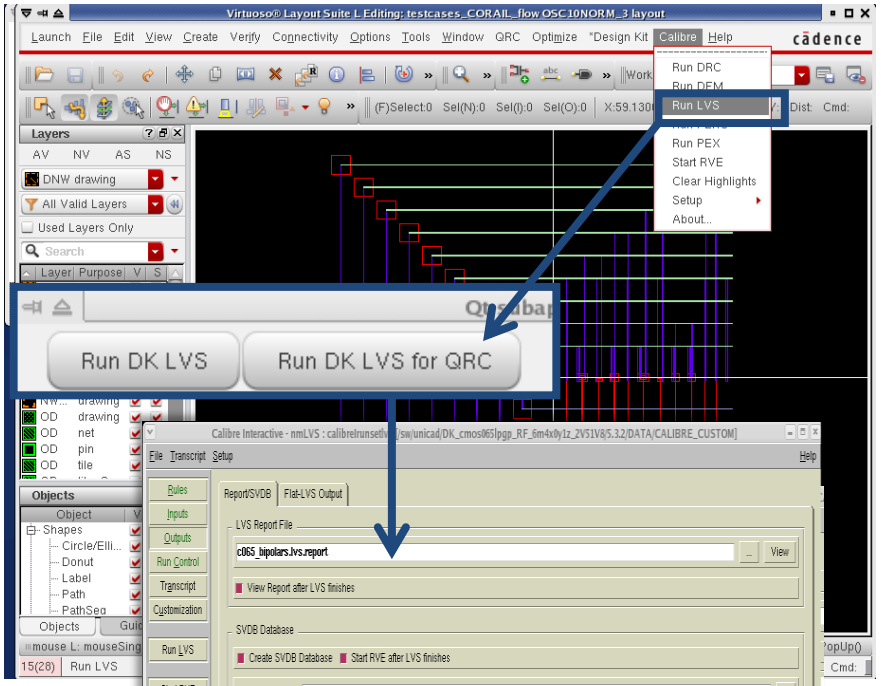
PDK 28FDSOI solution

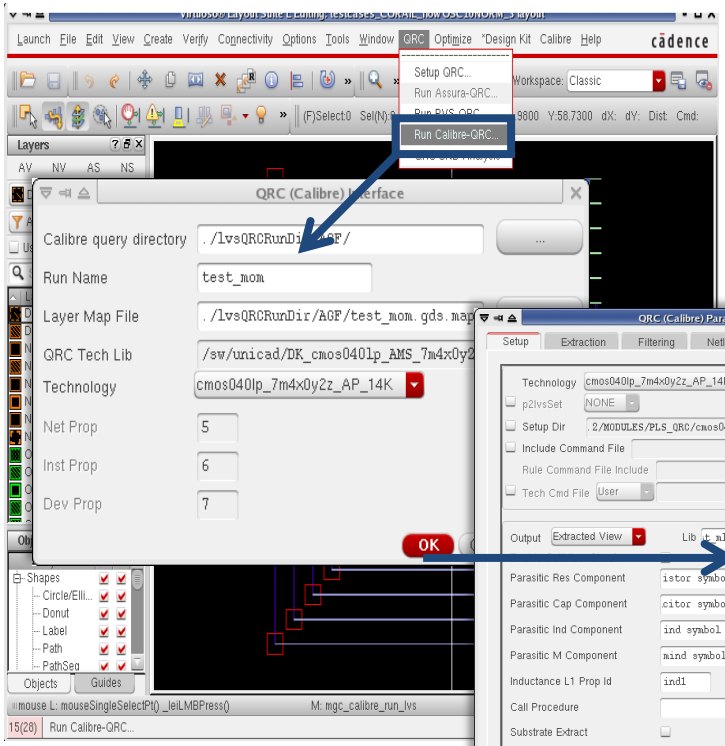
Crolles PDK

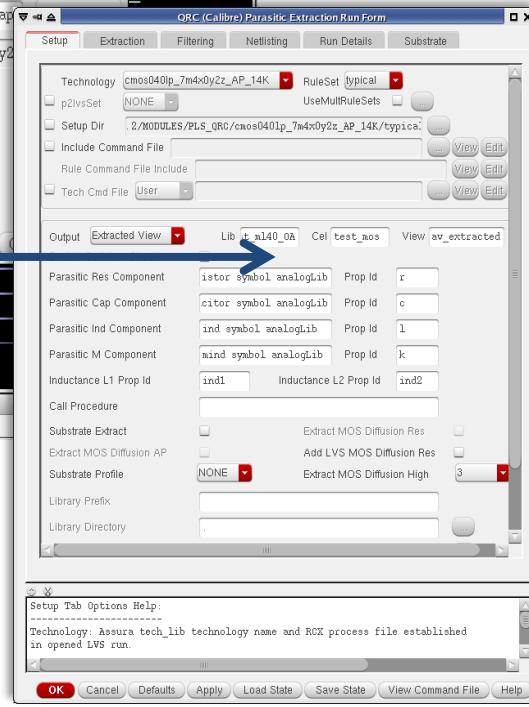
life.augmented

Virtuoso framework usage

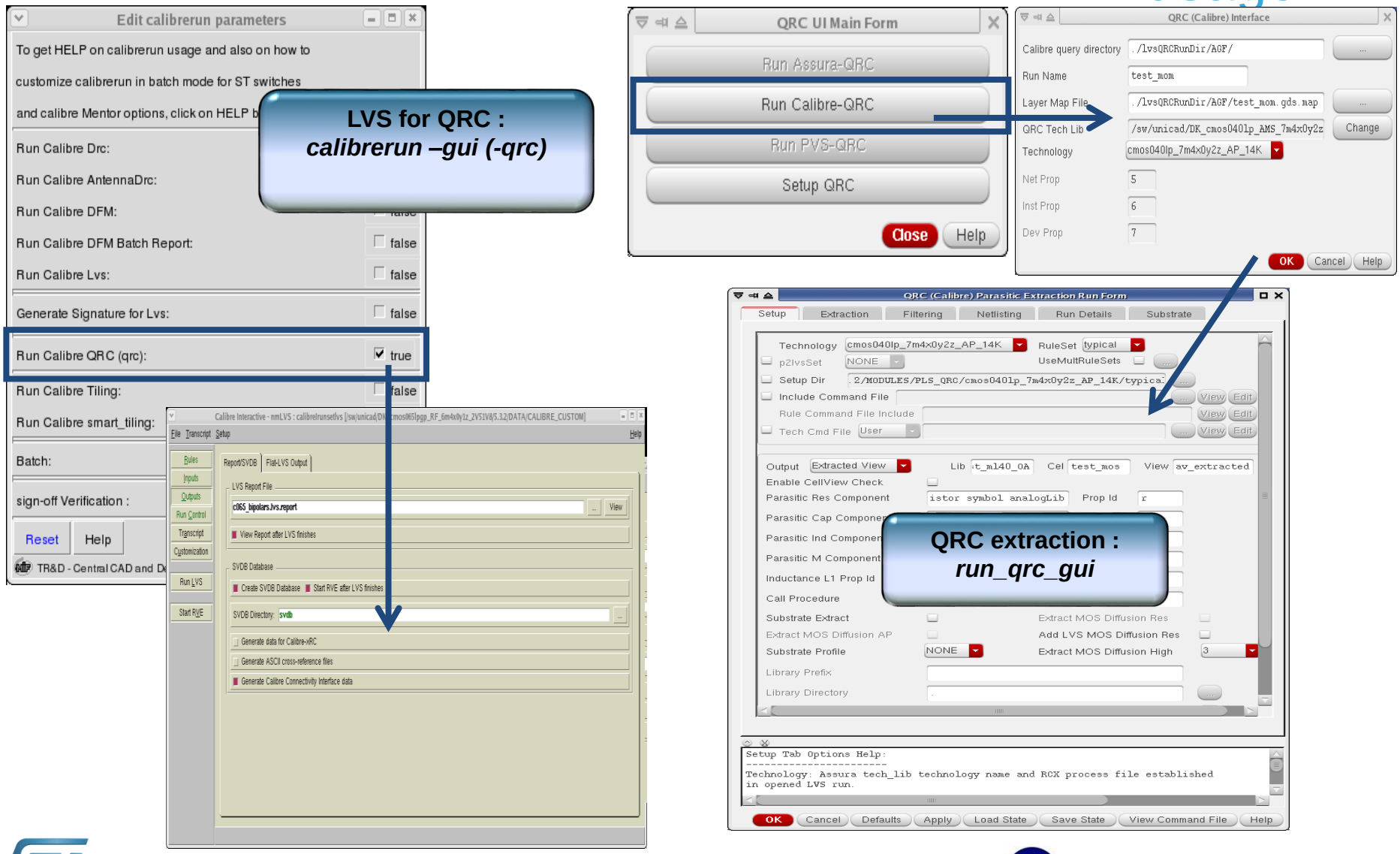
- QRC : Calibre LVS -> QRC : Managed by Calibrerun + QRC GUI





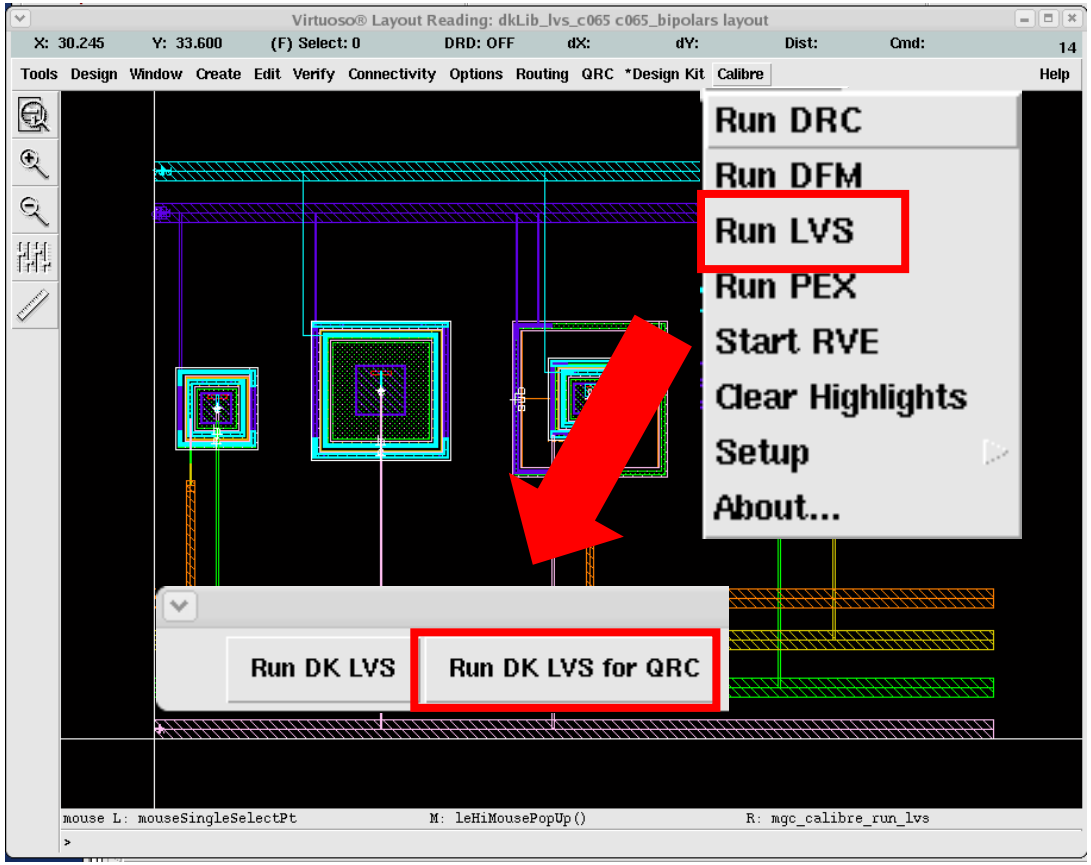


Main differences versus PLS flow : standalone usage



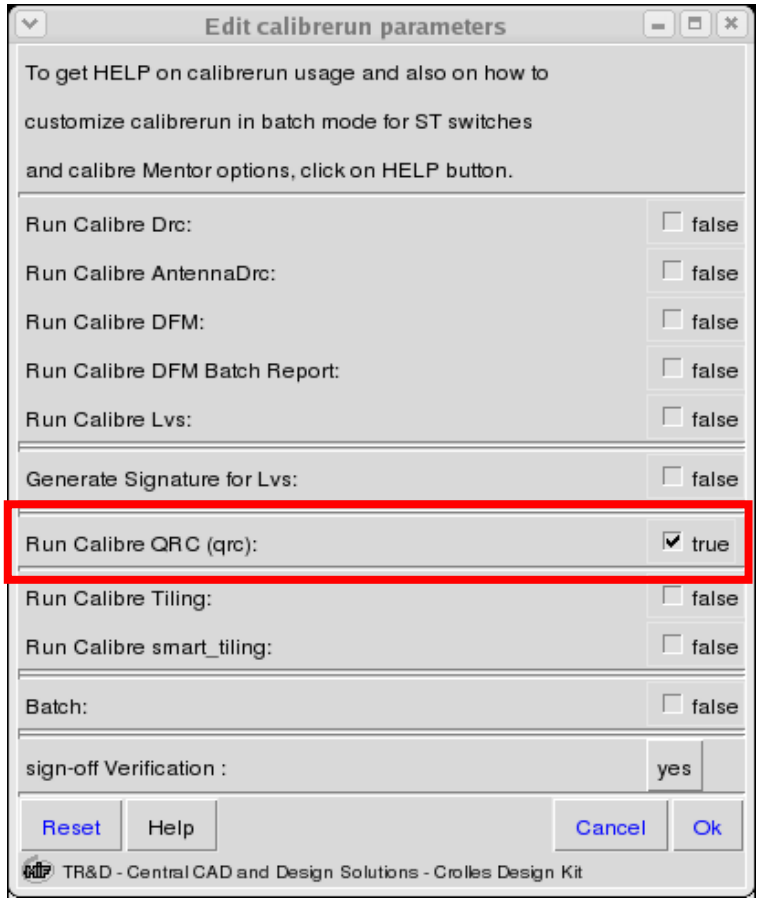
Calibre LVS for QRC (1/3)

- From Virtuoso :
  - Select LVS from Calibre menu
  - Select LVS for QRC in pop-up window



Calibre LVS for QRC (2/3)

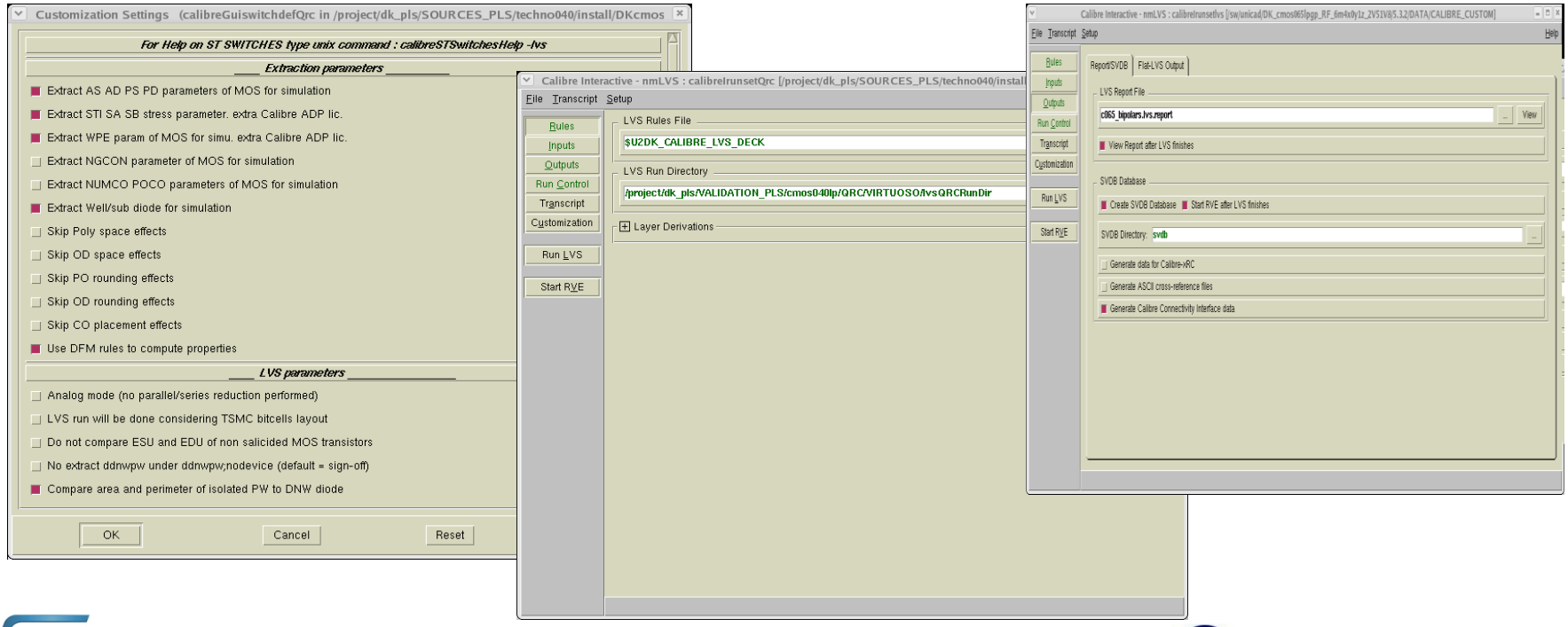
- From Calibrerun -gui:
  - Select LVS for QRC :



  - Or only run “Calibrerun –gui –qrc” to directly open Calibre LVS GUI for QRC

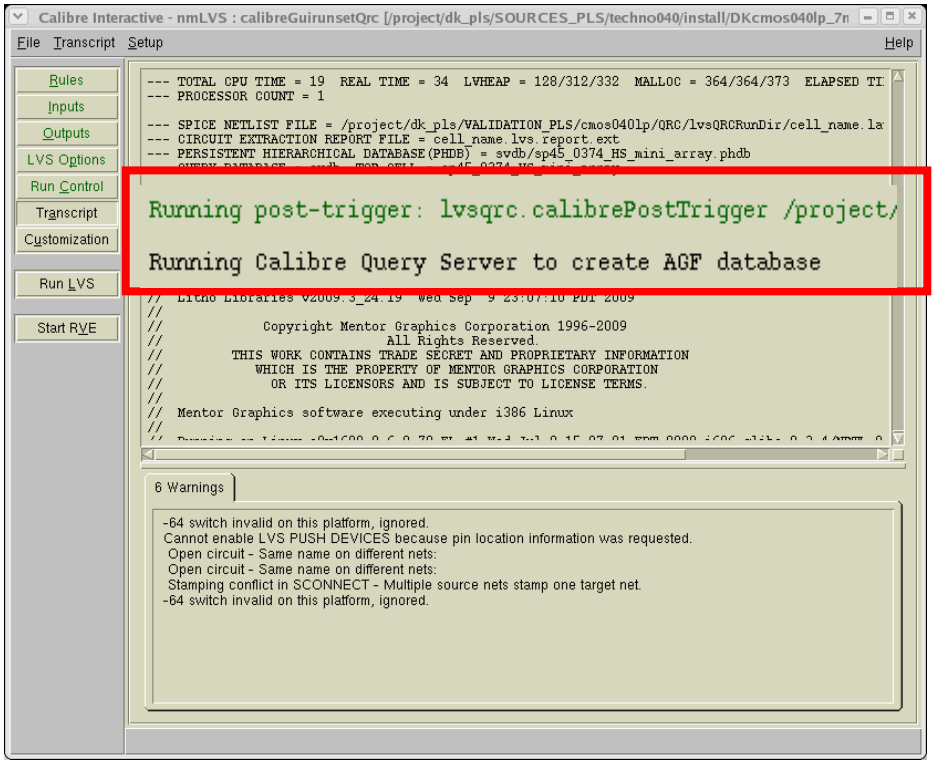
Calibre LVS for QRC (3/3)

- Switches for DFM/LPE LVS are displayed in customization window
- Pre-defined run directory is “lvsQRCRunDir”
- Calibre CI is output by default as it is mandatory for Query step



Calibre Query for QRC

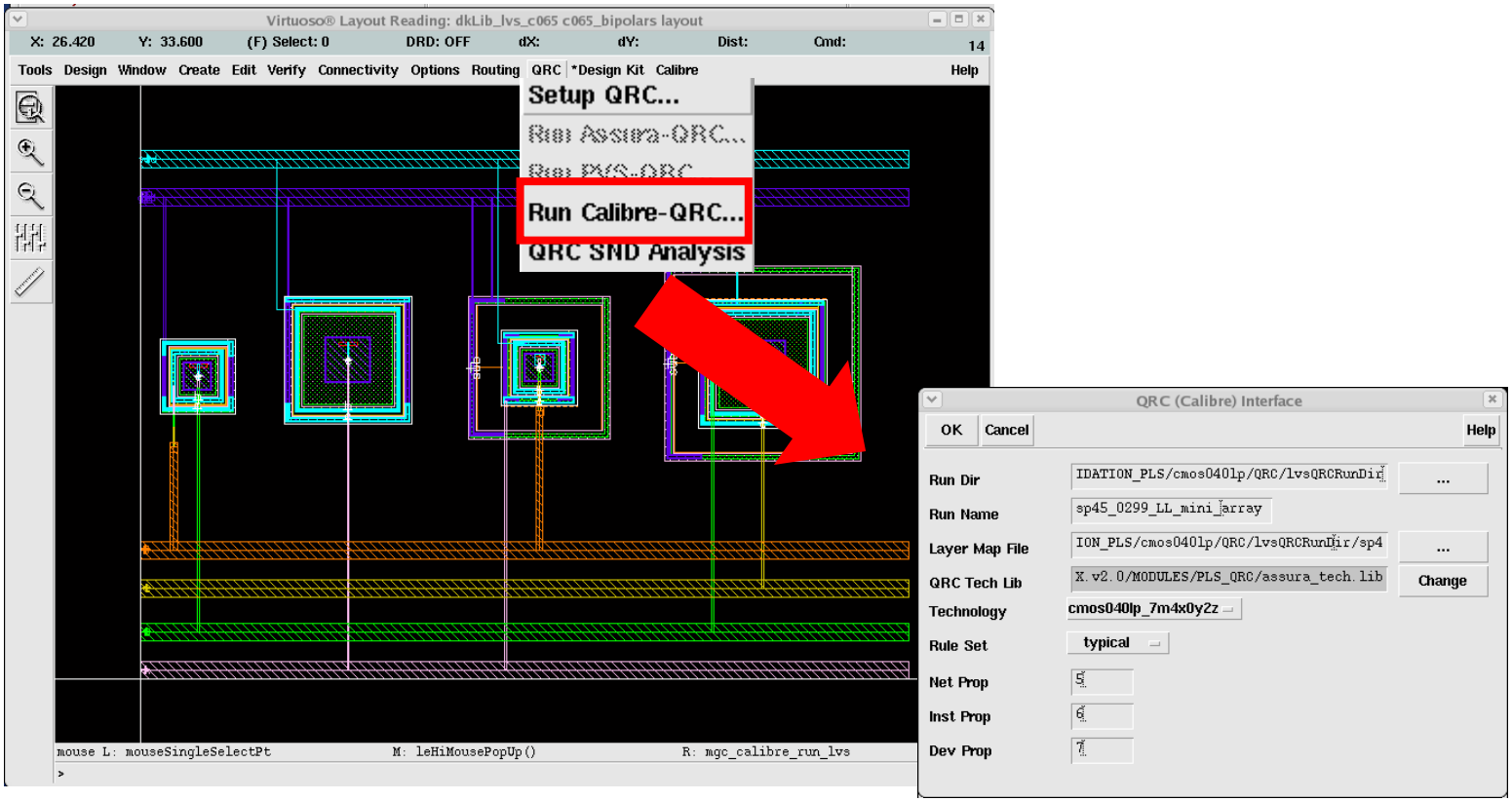
- Calibre Query Server is automatically run after LVS step thanks to a post-trigger :



- AGF database is created in run directory with all required information for QRC

Run QRC

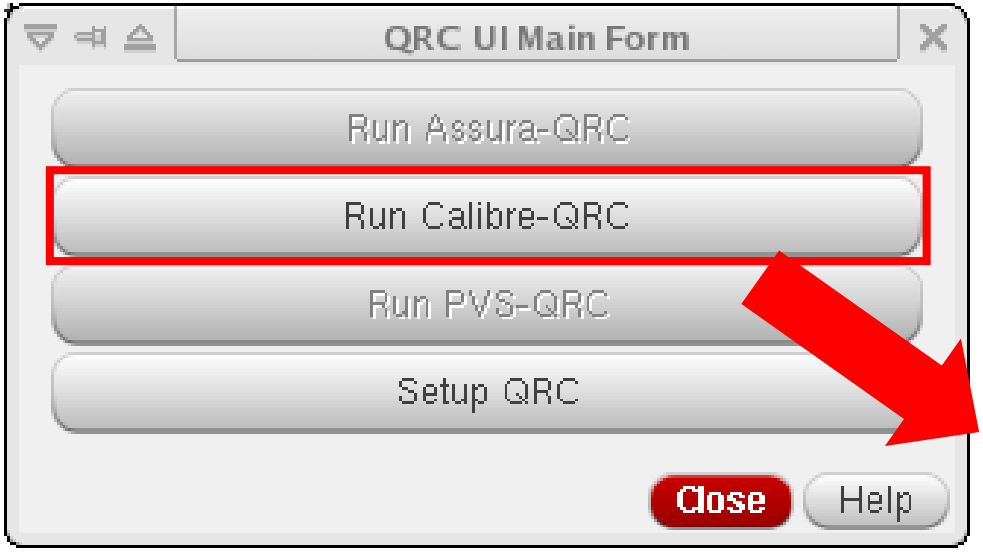
- From Virtuoso :
  - Select “Run Calibre-QRC” from QRC menu :

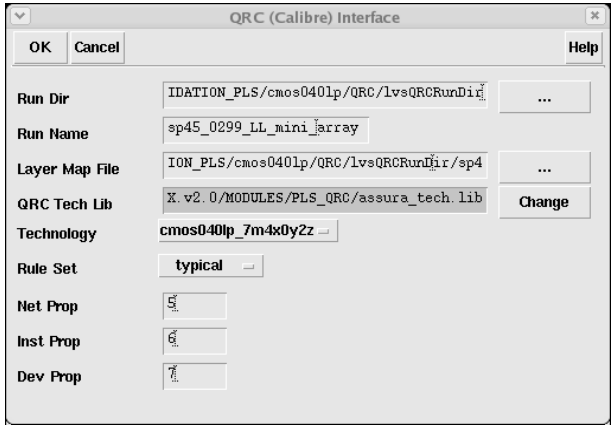


  - Setup QRC on pop-up window (see next slide)

Run QRC (standalone GUI)

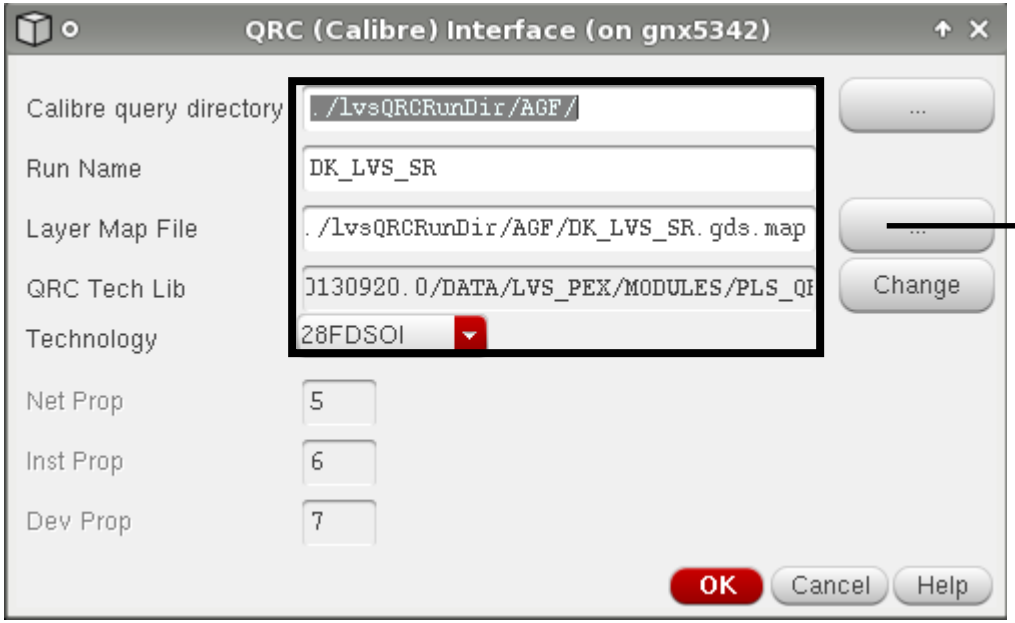
- From Unix terminal
  - Launch “run_qrc_gui” executable





  - Setup QRC on pop-up window (see next slide)

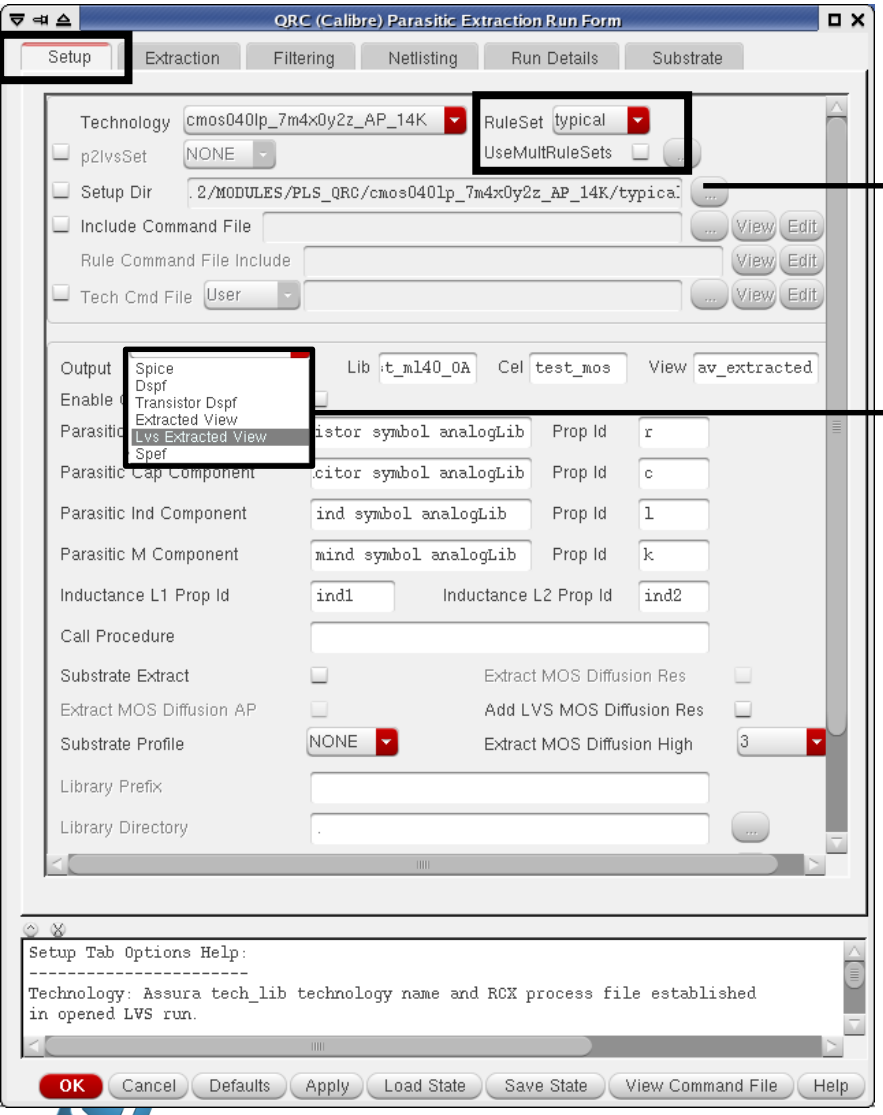
Setup Calibre - QRC



- **Run dir** is pre-defined to default AGF database coming from LVS
- **Topcell name** is automatically filled with cell name when QRC was launched from Virtuoso
- **Layer map** file is automatically filled according to both previous fields
- **QRC tech file** is pre-defined to Design Kit setup

QRC Graphical User Interface

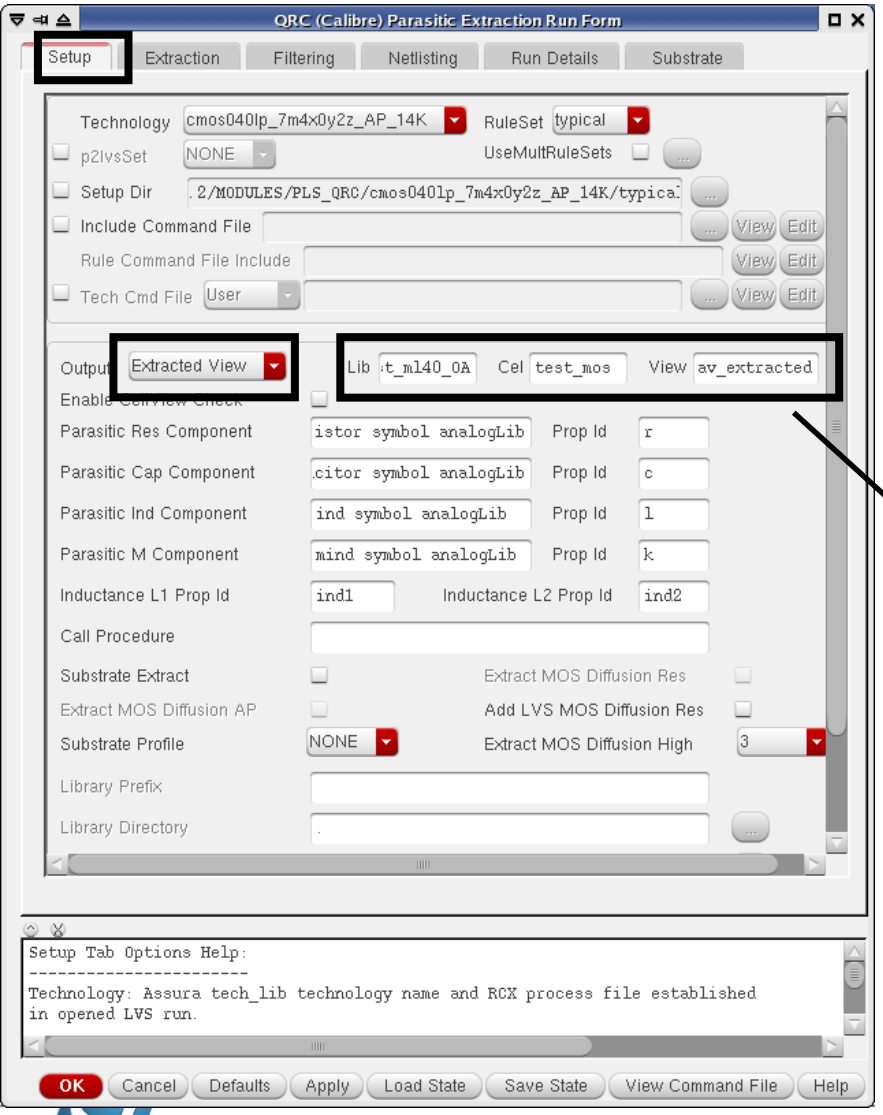
- Setup tab : general options

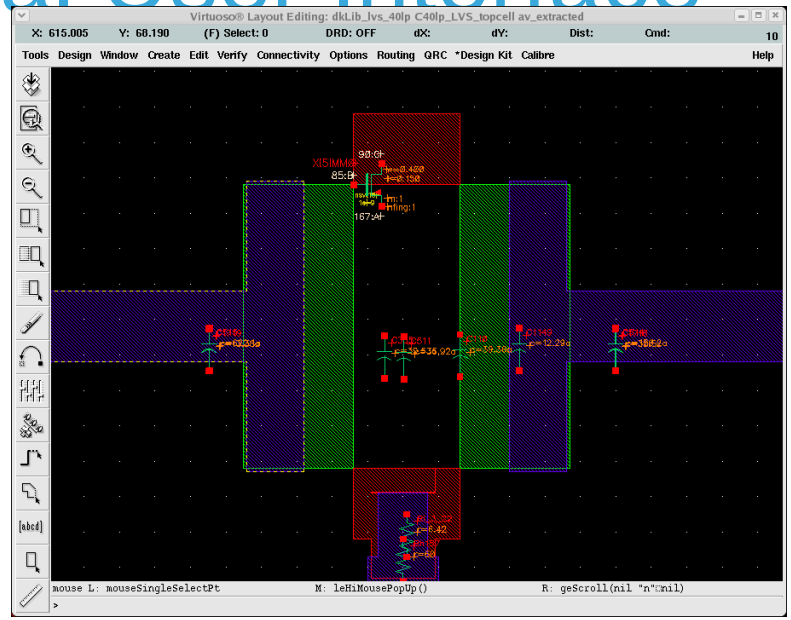


- **Corner selection** : typical, cbest, cworst, rcbest, rcworst
- Multiple Corner extraction
- **Supported output formats :**
  - Transistor level :
    - Extracted View (default)
    - LVS Extracted View
    - Transistor DSPF
    - Spice
  - Cell level :
    - DSPF/SPEF

QRC Graphical User Interface

- Setup tab : Extracted view

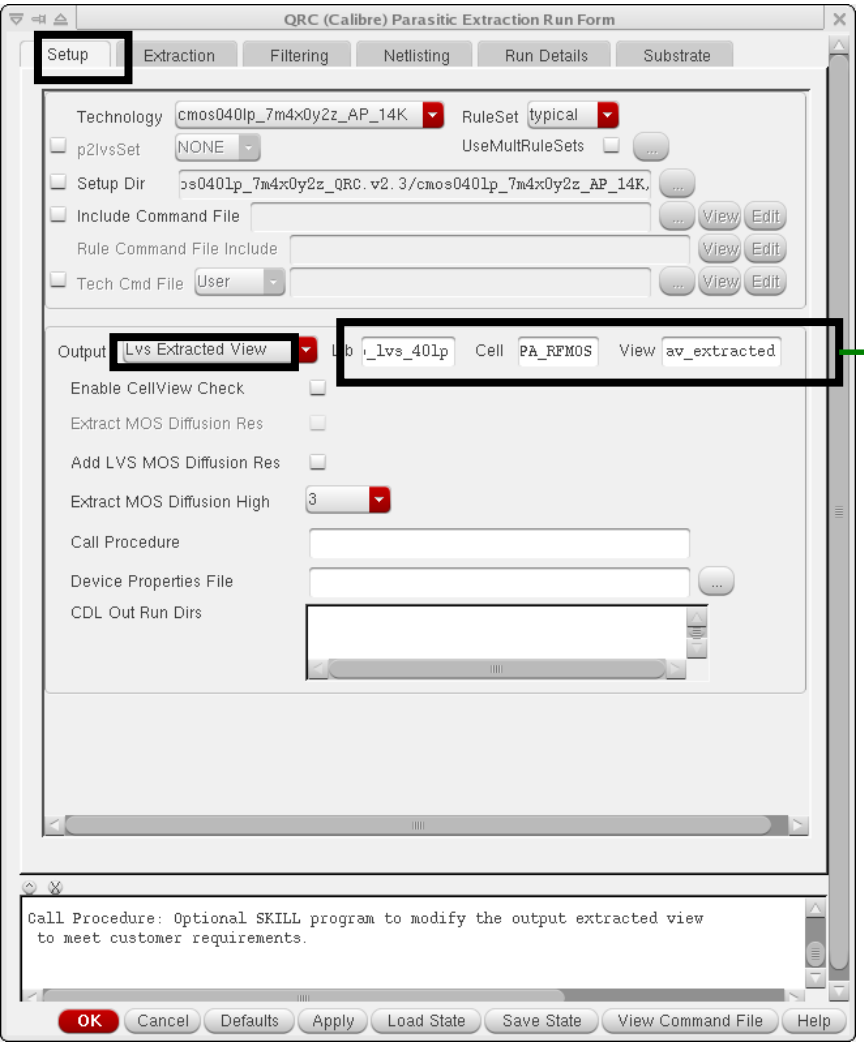




- **Name and library of the extracted view in virtuoso**

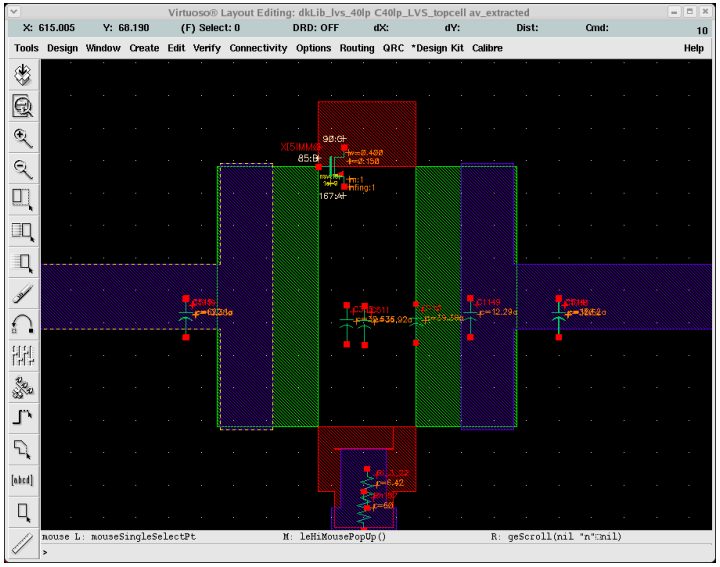
QRC Graphical User Interface

- Setup tab : LVS Extracted view



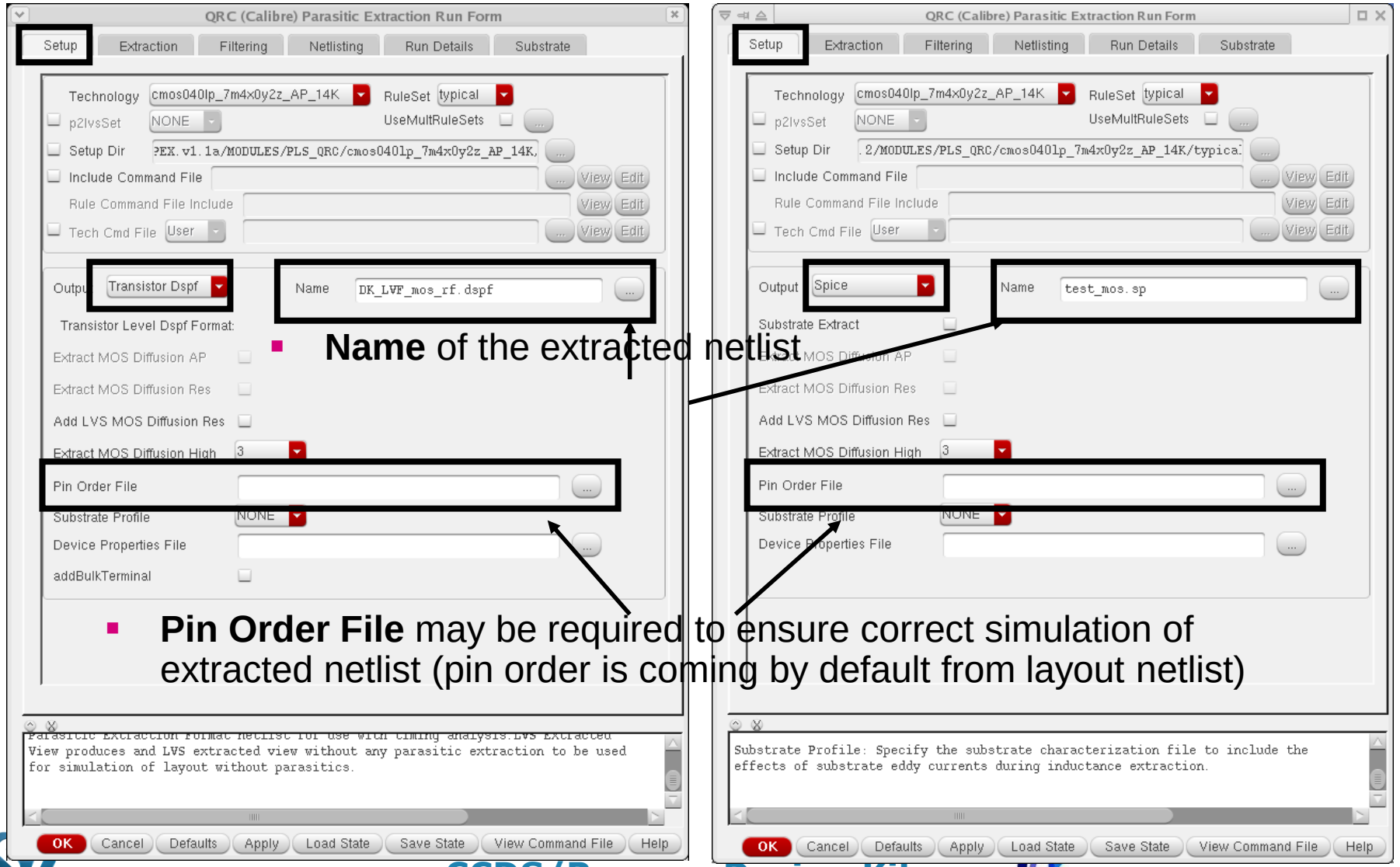
- Creates an extracted view **without parasitics**, which includes only devices and allows to take into account **layout effects** for simulation

- **Name and library of the extracted view in virtuoso**



QRC Graphical User Interface

- Setup tab : Transistor DSPF and Spice

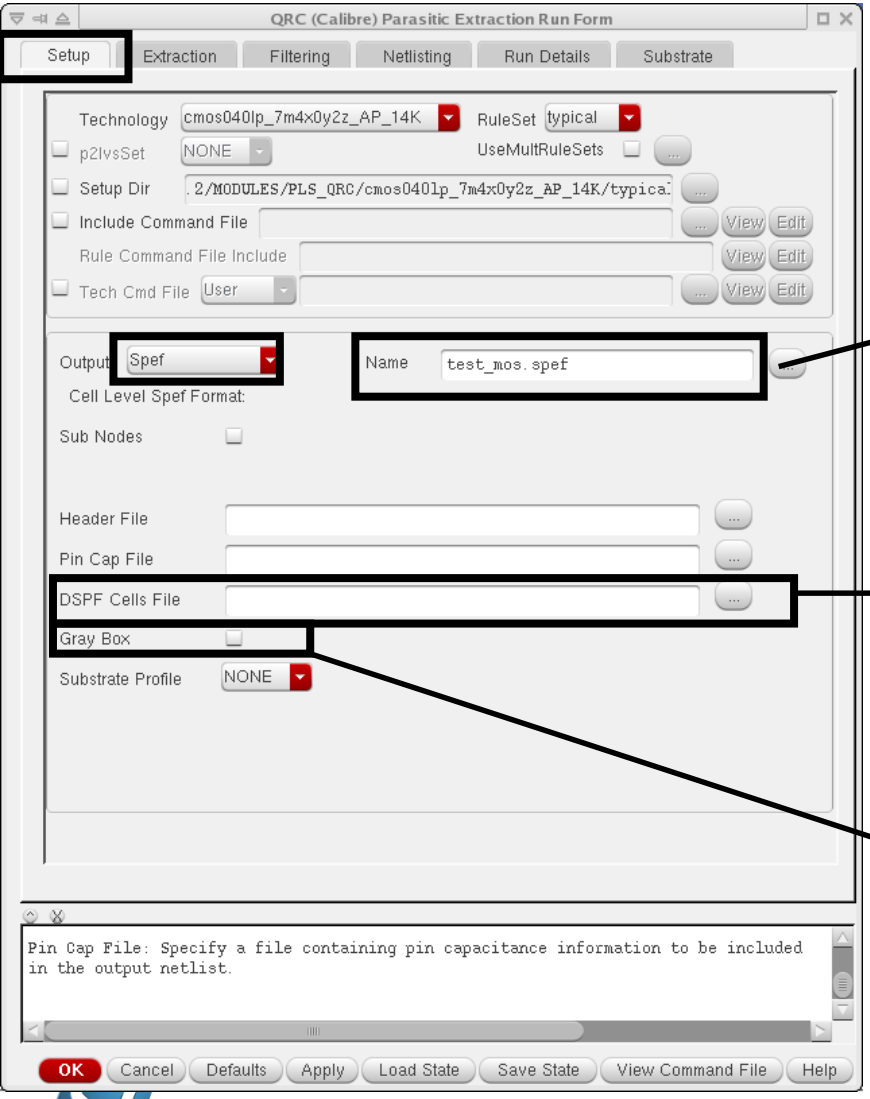


- **Name** of the extracted netlist

- **Pin Order File** may be required to ensure correct simulation of extracted netlist (pin order is coming by default from layout netlist)

QRC Graphical User Interface

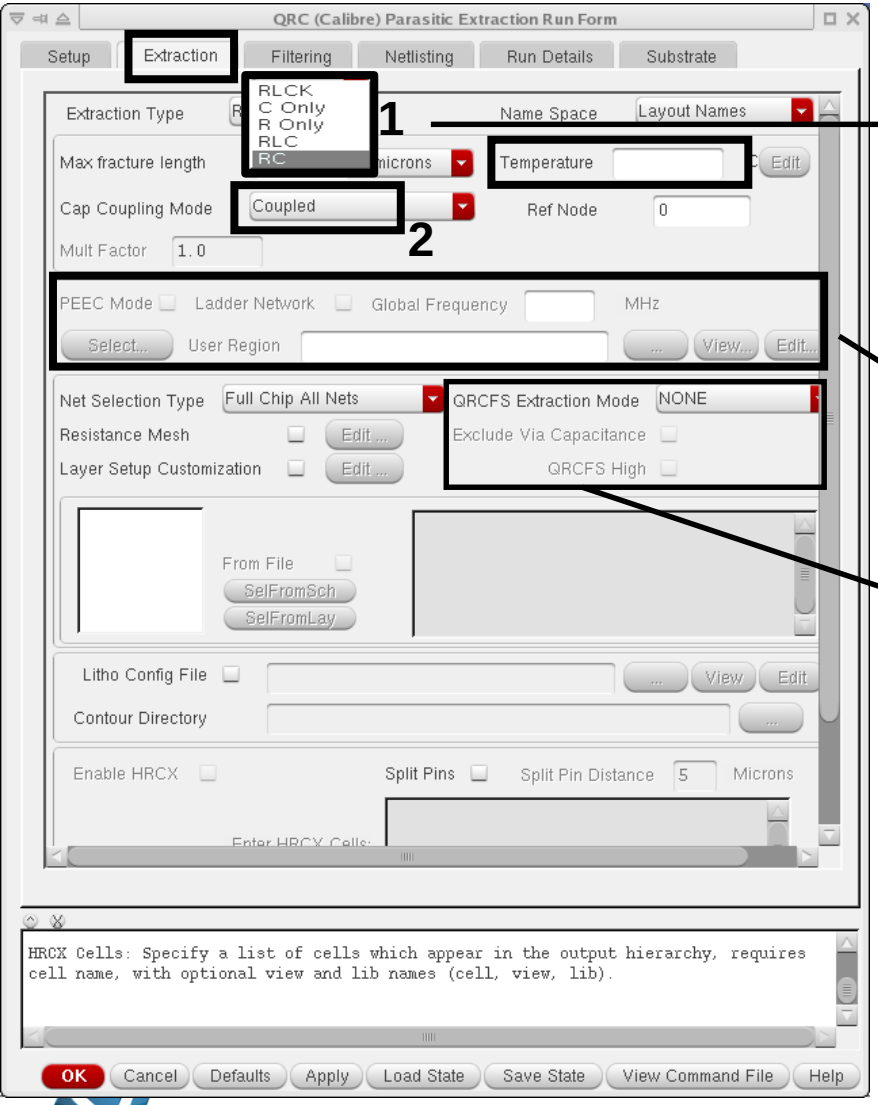
- Setup tab : DSPF & SPEF for Cell Level



- **Name of the extracted netlist**
- **DSPF Cell File** is required and similar to hcell file used during Calibre LVS
- **Gray box** option is recommended for accurate capacitance extraction between cells

QRC Graphical User Interface

- Extraction tab :



- 1) **Extraction mode** selection :
  - R, C, RC, RLC, RLCK
- 2) Capacitances :
  - Coupled
  - Decoupled (to ground)
  - Decoupled_to_substrate
- 3) **Temperature** for R extraction

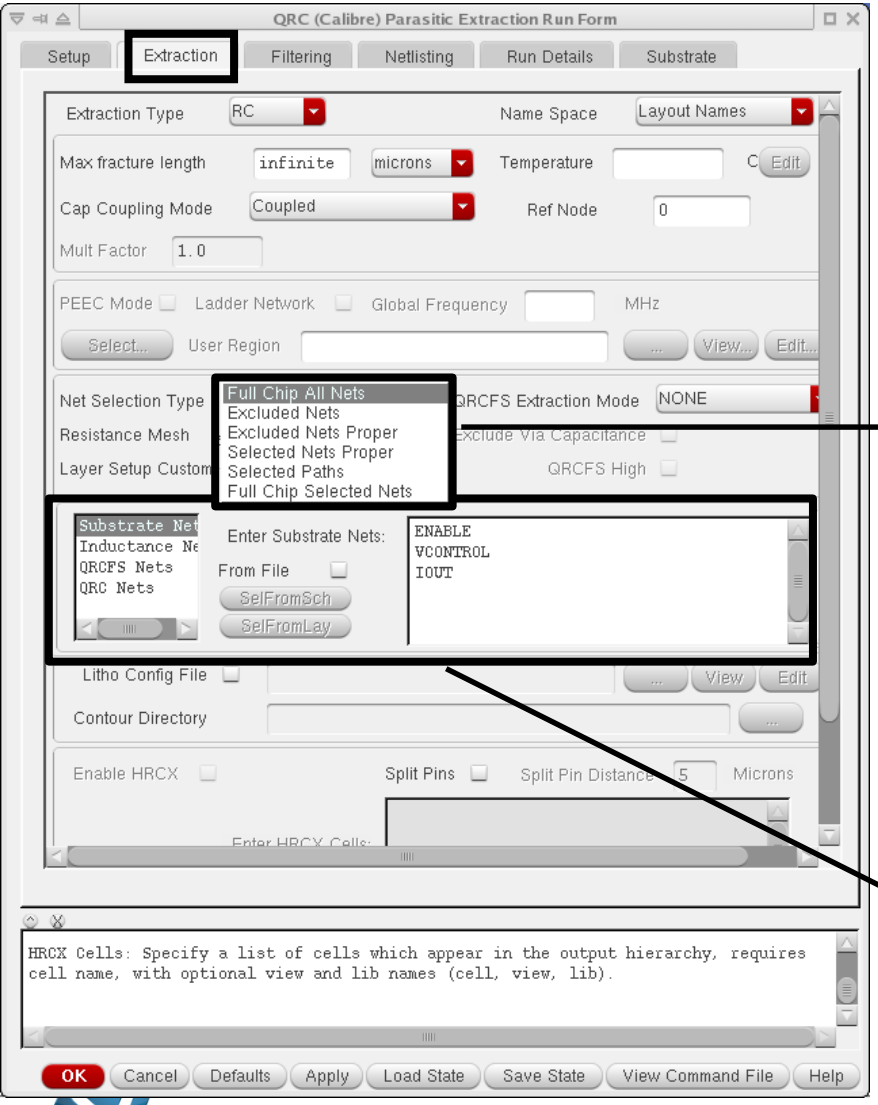
- **Inductance extraction setup :**
  - See slide 18 for more details about usage

- **Field-Solver extraction : QRCFS**

Note from Cadence *: "QRCFS is fast BEM solver. (BEM = Boudary Element Method) For each conductor (aggressor), FS computes C value up to some checking distance. Then, FS would evaluate the quality of the solution. If the solution is good, that is the end. Otherwise, FS would double the checking distance and repeat the process."*
High_accuracy *has finer mesh.*

QRC Graphical User Interface

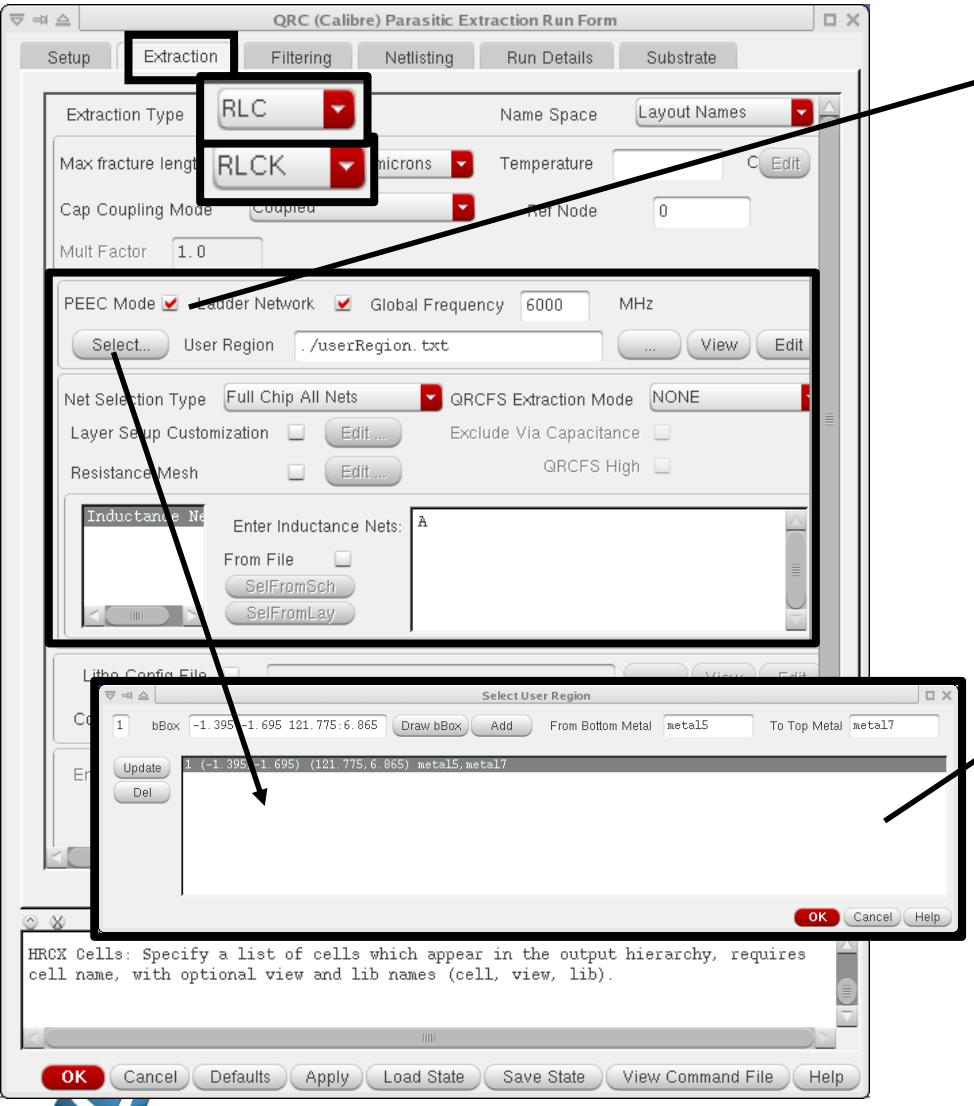
- Extraction tab :



- **Net selection (depends on extraction mode)**
  - **Full Chip All Nets** (default) :
    - All nets are selected for RLCK extraction (if no specified inductance nets)
  - **Full Chip Selected Nets** :
    - Listed Nets only are selected for R extraction
    - All nets are selected for C extraction
    - L&K extraction not supported
  - **Selected Nets Proper** :
    - Listed Nets only are selected for RLCK extraction
  - **Selected Paths** :
    - Paths derived from listed nets are selected for RC extraction
    - L&K extraction not supported
  - **Excuded Nets proper :**
    - All nets except specified excluded nets are selected for RLCK extraction
  - **Excluded Nets :**
    - All nets except specified excluded nets are selected for R extraction
    - All nets including excluded nets are selected for C extraction
    - All nets except specified excluded nets are selected for L&K extraction (if no specified inductance nets)
  - **Required** for inductance extraction
  - **Optional** for QRC, QRCFS and Substrate extraction
  - Net names can be directly specified in GUI or through a netfile
  - Wildcards are supported

QRC Graphical User Interface

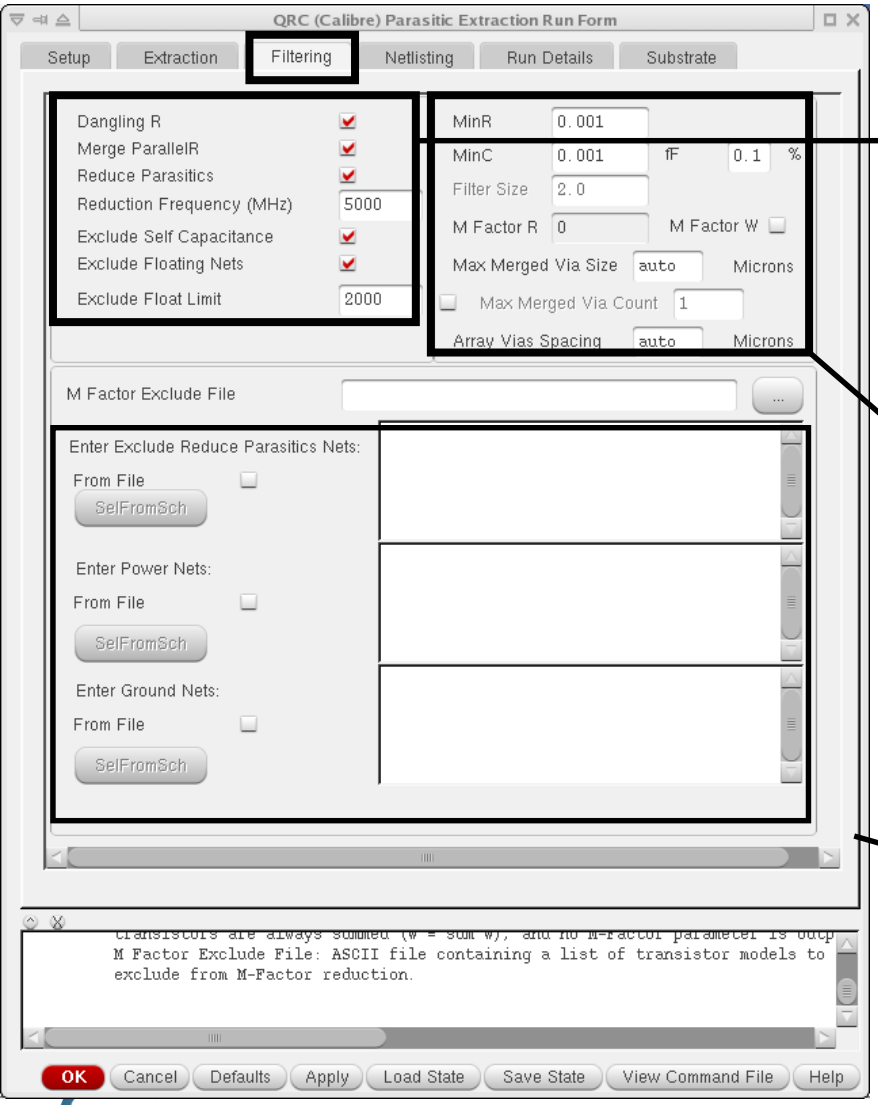
- Inductance setup :



- **PEEC** (Partial Element Equivalent Circuit)
  - Recommended mode for analog/RF designs
  - Computes partial mutual inductances between nets inside the same interaction region
- **User-region file** can be defined thanks to pop-up windows :
  - Avoid LK extraction where current direction is not well defined (ex : large metal plates)
  - Encompass local power/ground structures
  - Cut “across” critical nets
  - 200um max
- Use **net selection** to define nets to be taken into account for inductance extraction Nets must be located in user regions
  - If no Inductance nets are provided, all nets in user region will have inductance extracted (not recommended, because of netlist size)
  - If mutual couplings are expected between 2 nets, both of them must be specified
- **Ladder network** (broadband interconnect model)
  - Models skin and proximity effects.
  - Adds additional R, L, and K values (and other components such as CCVS) to the parasitic netlist compared with the Low Frequency interconnect modeling
  - Valid for all frequencies (global frequency field is useless in this mode)
  - To be used with caution because of the runtime and netlist size increase, and potential simulation convergence issues
- **Global Frequency** is useless with ladder network option. It is otherwise used to filter small Ls.
- **Exclude Self Capacitance** must not be enabled for RLKC

QRC Graphical User Interface

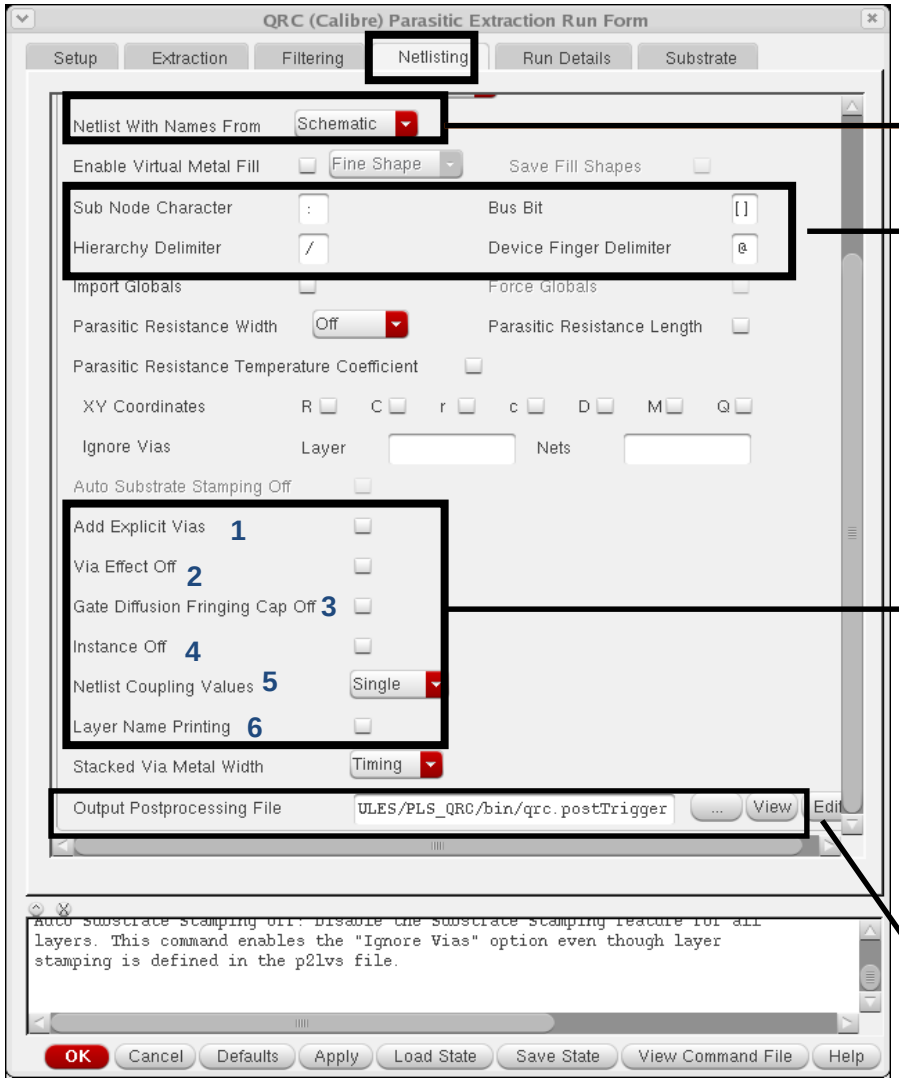
- Filtering tab :



- **Reduction options :**
  - **Pre-defined by PDK :**
    - Remove dangling resistors
    - Merge parallel resistors
    - RC Reduction
      - Some nets may be excluded from reduction
    - Exclude self capacitance
    - Exclude floating nets
- **Filtering options :**
  - Capacitive and resistive thresholds
  - Merge vias
- Define nets to be excluded from parasitic reduction
- Define power and ground nets to be excluded from R extraction

QRC Graphical User Interface

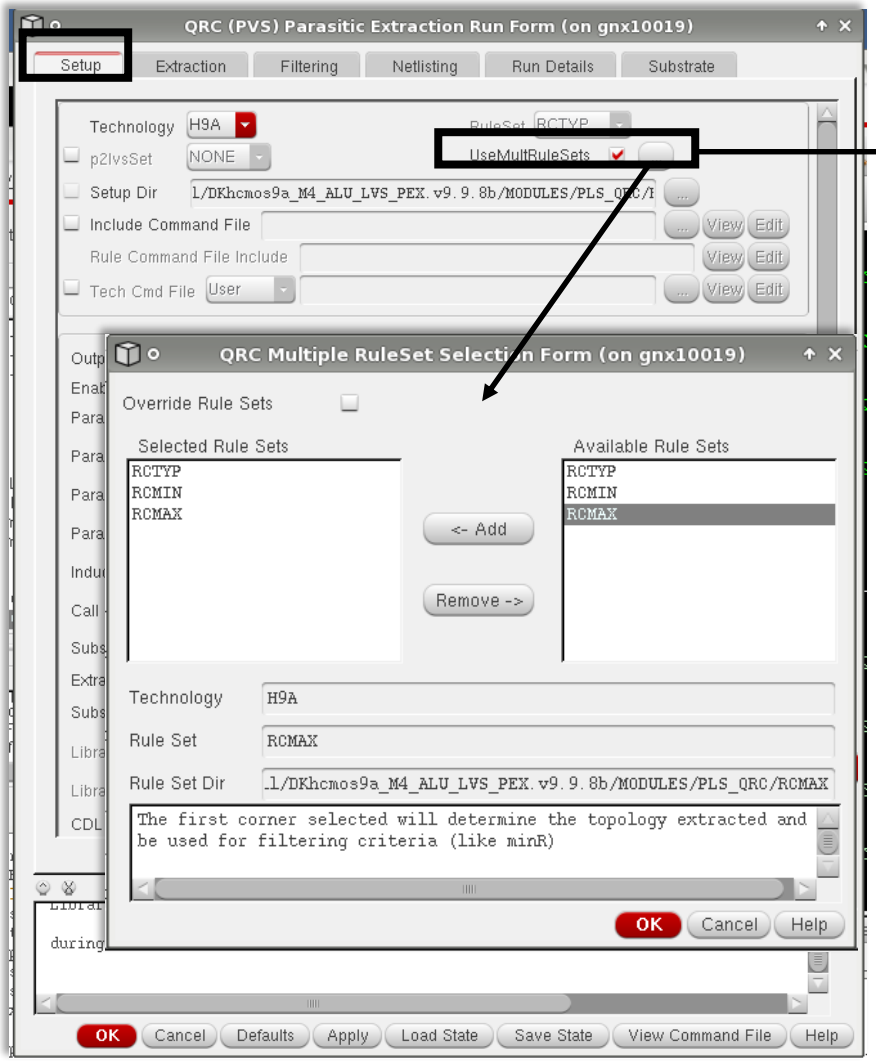
- Netlisting tab :



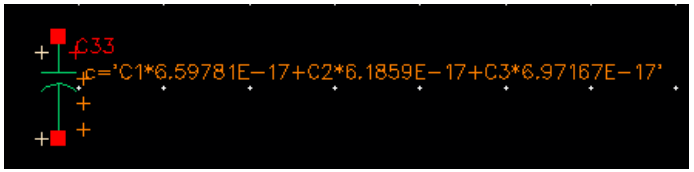
- Use schematic or layout names (layout names are mandatory in case of layout-only extractions
- Netlist syntax controls
- 1) Explicitly displays computed resistances of vias/contacts
- 2) Disable via/contact capacitance during parasitic extraction
- 3) Disable gate-to-diffusion fringing capacitance of MOS
- 4) Disable instance display in output netlist
- 5) Allows double coupling capacitance display
- 6) Display metal layer for each extracted parasitic resistors
- netlist post-processing

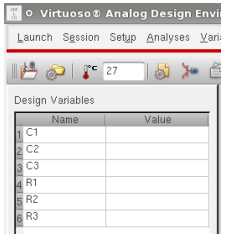
QRC Graphical User Interface

- Multi-corner extraction:



- Allows to run several corners in a single extraction
- When "**UseMultRuleSets**" option is enabled, corners of interest can be selected in the pop-up window
- The values of R&C parasitics in output (extracted view or netlist) will be based on coefficients
  - Those coefficients can be defined during simulation to reflect the corner

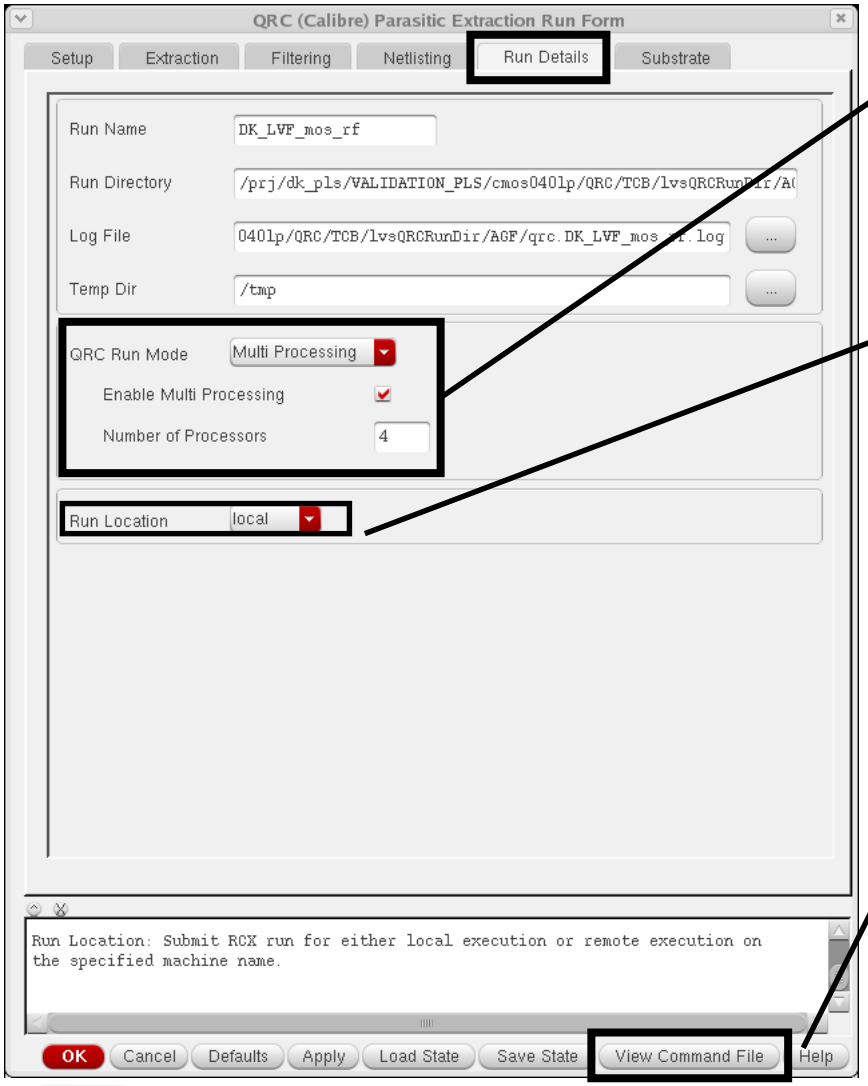




- Limitations :
  - Field-solver, Inductance and reduction are not supported in this mode

QRC Graphical User Interface

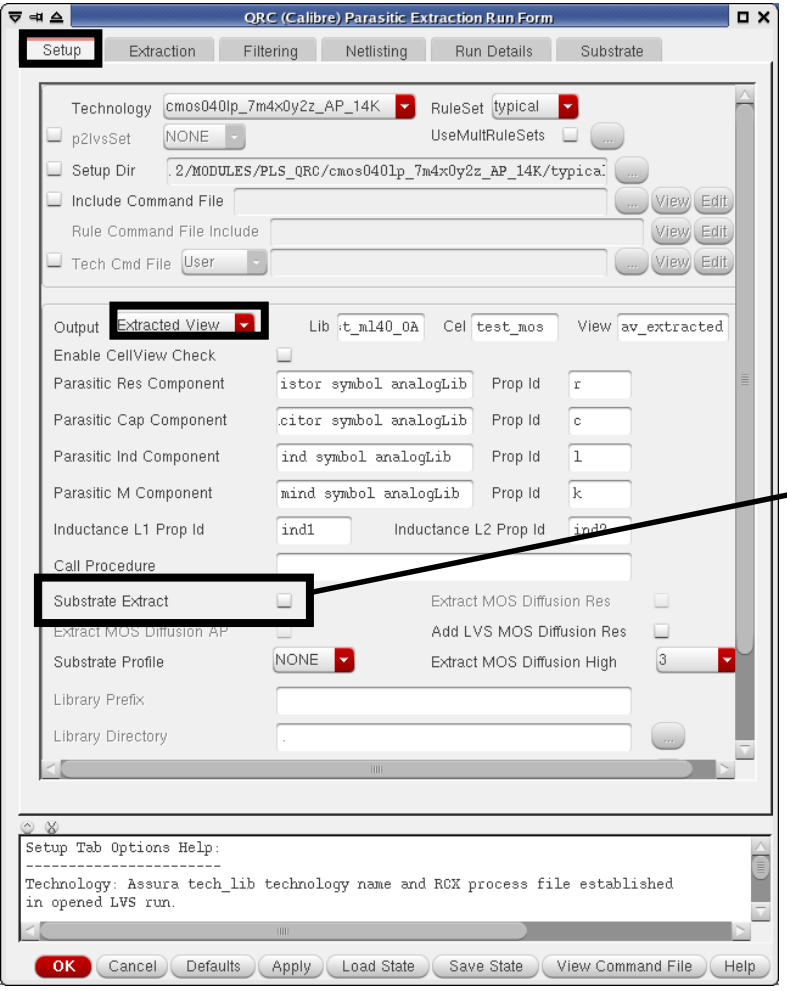
- Run Details tab :



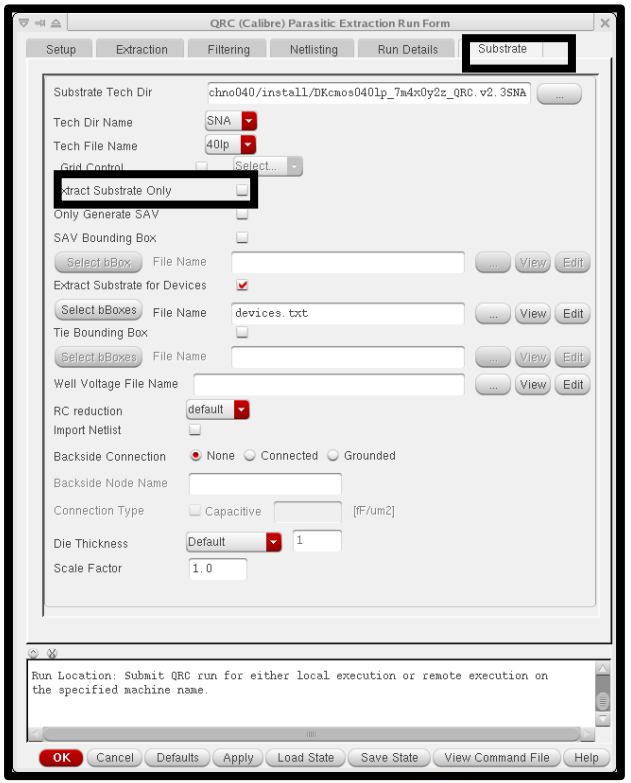
- Allows to run QRC in Distributed Processing mode
  - Number of CPUs is required
- Allows to run QRC on local host or through LSF compute farm
- **To display (and save) QRC command file according to the settings defined in GUI :**
  - Allows to run qrc –cmd cmd_file.ccl

QRC Graphical User Interface

- Substrate tab :



- Substrate extraction is for :
  - spice and extracted view outputs
  - R, RC, RLC, RLCK,
  - NoRC is available with substrate only option in substrate tab



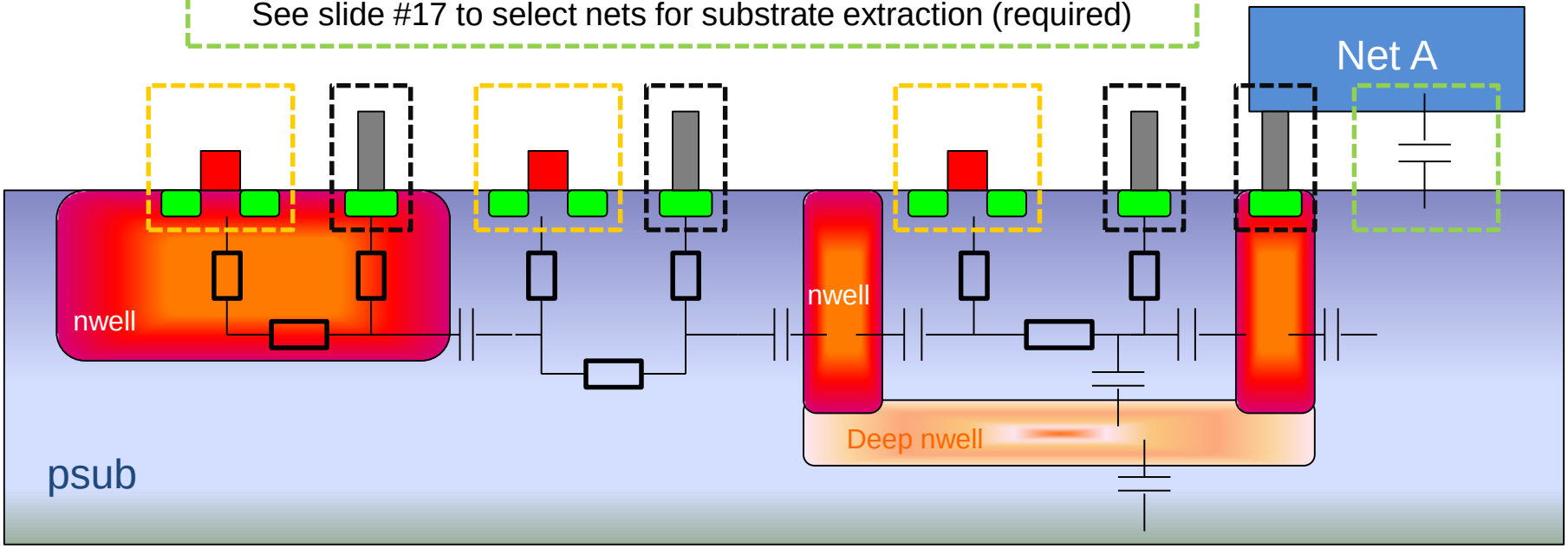
Substrate extraction

- SNA allows to extract parasitics elements in substrate based on doping profiles for each region (psub, nwell, deep nwell)
- Capacitors are computed for each junctions, replacing intentional diodes. Therefore it is mandatory to enable the switch *NO_DIODES_FOR_SNA* during LVS prior to QRC/SNA extraction
- The substrate network could have several interfaces with external circuit :

Connection through taps only.
This is the default behavior.
See next slide to select a region (optional)

Connection through bulk terminal of devices
See next slide to select a region (required)

Connection through substrate capacitance of interconnect
See slide #17 to select nets for substrate extraction (required)

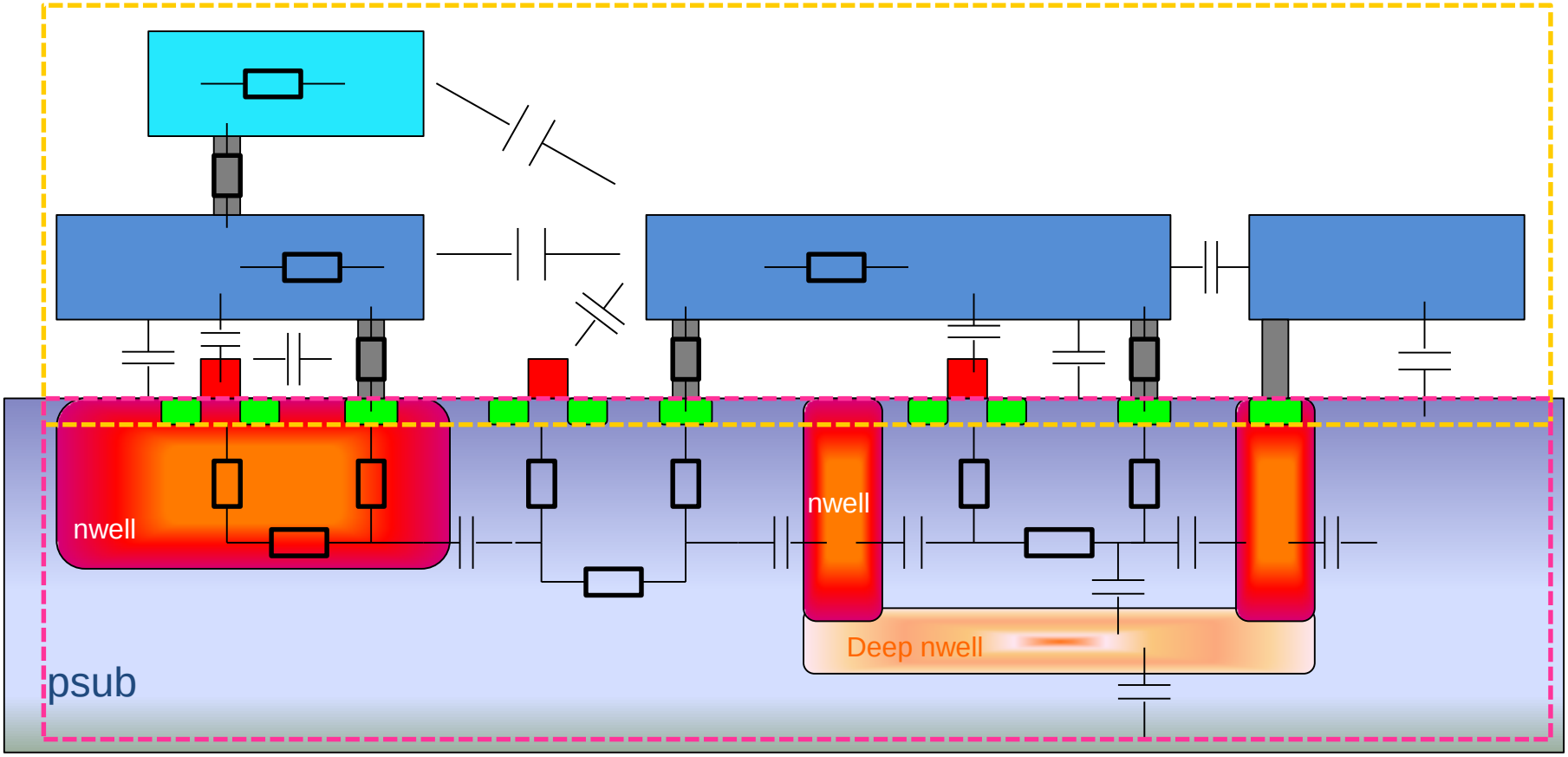


Substrate extraction

- Substrate parasitics can be extracted in standalone or in addition to interconnect parasitics

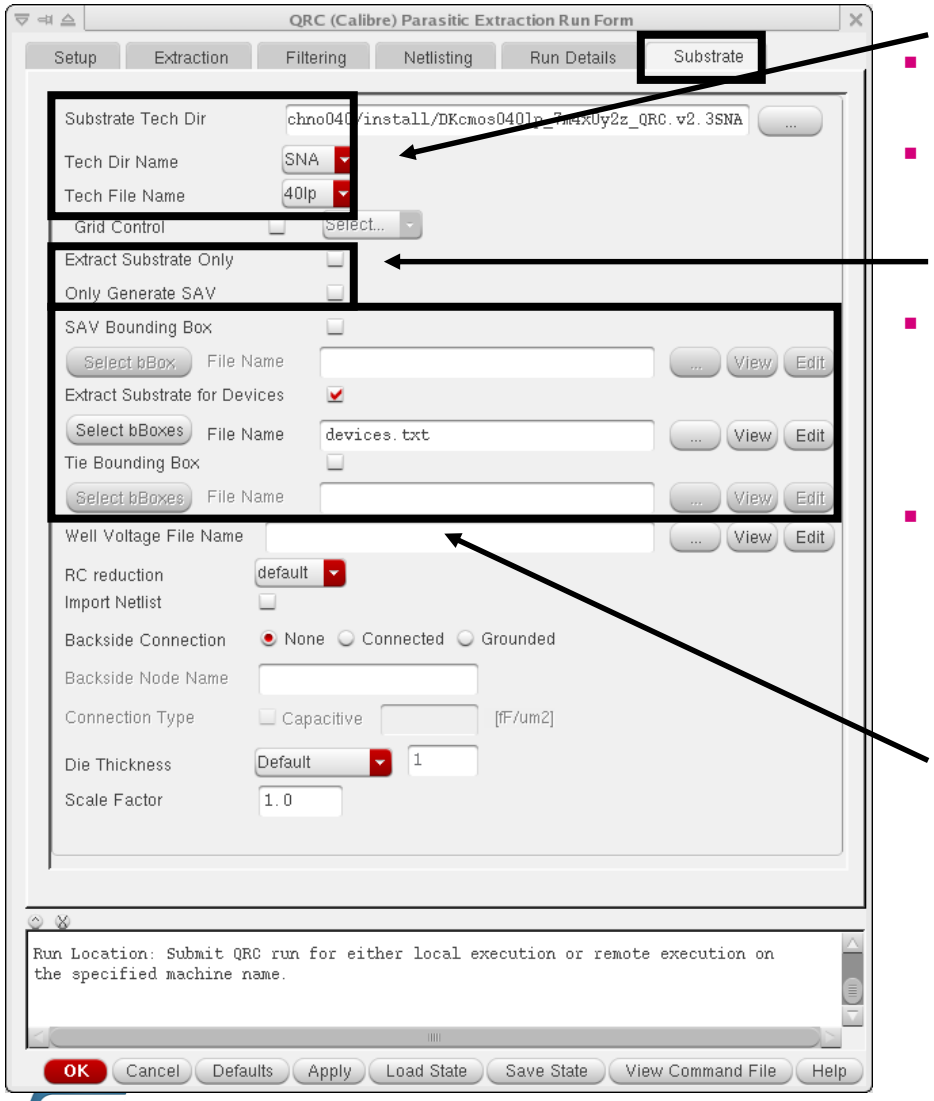
QRC perimeter

SNA perimeter



QRC Graphical User Interface

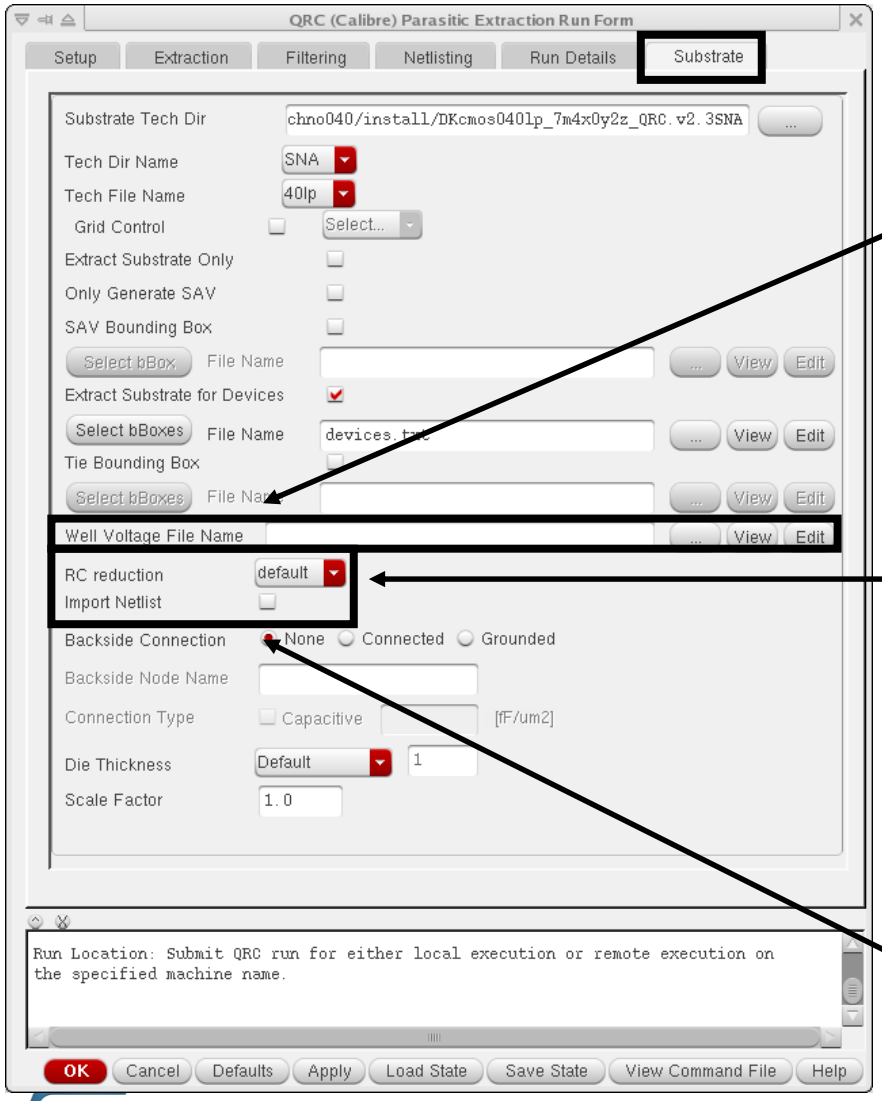
- Substrate tab :



- **SNA technology data** is pre-defined and refers to Design Kit location
- Allows to **compute only parasitic substrate network** (interconnects are ignored). It is useful to run Post-Layout Simulation taking into account only substrate effects.
- Allows to **generate only Substrate Abstract View**. It creates an “empty” extracted view which allows to save runtime. This option is highly recommended for SND usage on top of chips.
- **Bounding boxes :**
  - The “**SAV bounding box**” allows to increase the size of area on which SAV is computed. If not specified, the default area is set to 10 microns outside the bounding box of the layout.
  - The “**Extract Substrate for Device**” commands allows to select regions where bulk terminal of device is connected to substrate network.
  - The “**tie bounding box**” allows to define specific regions where taps are connected to substrate network. If not specified, all taps are connected.

QRC Graphical User Interface

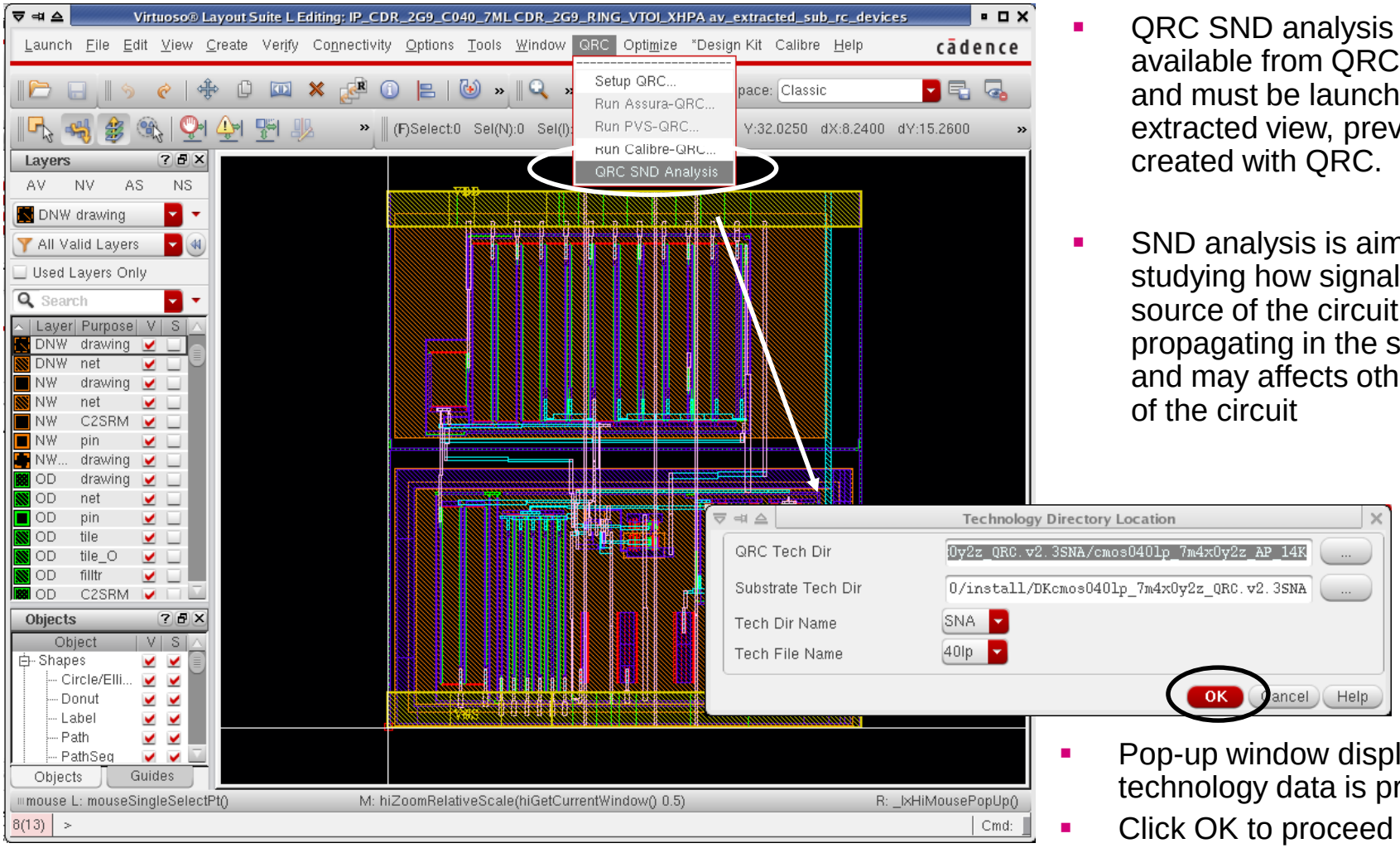
- Substrate tab :



- The **Well Voltage File Name** allows to define different voltages for the multiple nwell. If not specified, the same voltage is applied for all nwells.
- **RC reduction** is enabled by **default** to reduce the number of parasitic components in the substrate network. It is impacted by the global frequency if it has specified in “Extraction” tab (default is 5Ghz). The reduction can be **disabled** (very large network -> not recommended) or set to “**fast**” (save memory and runtime)
- **Import Netlist** is only available with extracted view output. It allows to include the substrate parasitics directly in the extracted view. It can increase its generation runtime. When disabled, the substrate network is included with a symbol from the substrateLib library (available in the Design Kit or in IC installation)

QRC Graphical User Interface

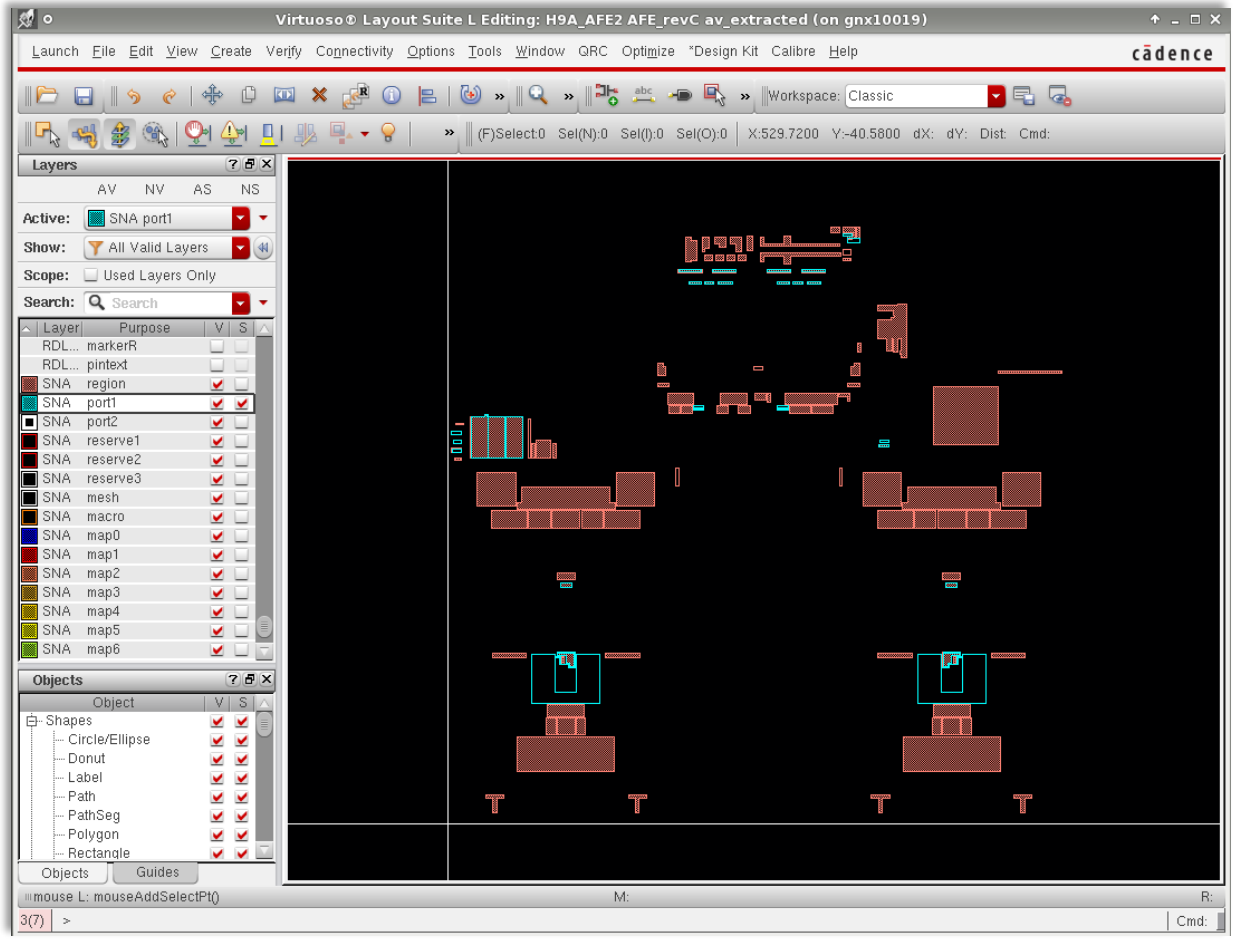
- Surface Noise Distribution (SND) :



- QRC SND analysis is available from QRC menu and must be launched from extracted view, previously created with QRC.
- SND analysis is aimed at studying how signals from a source of the circuit are propagating in the substrate and may affects other parts of the circuit
- Pop-up window displaying technology data is pre-defined.
- Click OK to proceed with SND

QRC Graphical User Interface

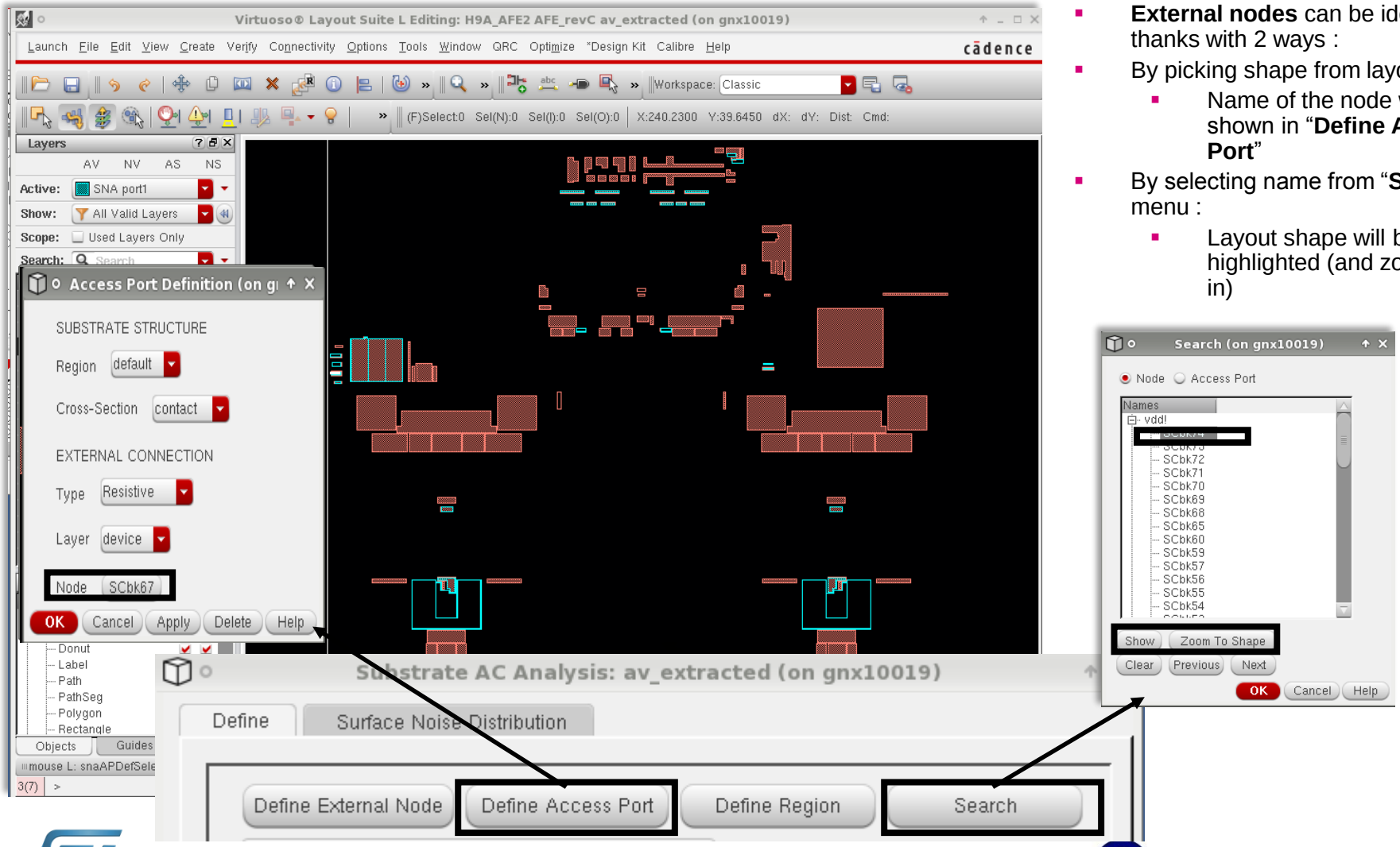
- Surface Noise Distribution (SND) :



- When SND is running, layout colors are updated to display the substrate regions and nodes
- **Regions** are wells (nwells, deep-nwells, isolated pwells)
  - Drawn with SNA-region layer (orange)
- **External Nodes** are connections to these regions (taps, bulk terminals of devices). They are the interfaces to the substrate network.
  - Drawn with SNA-port1 layer (blue)

QRC Graphical User Interface

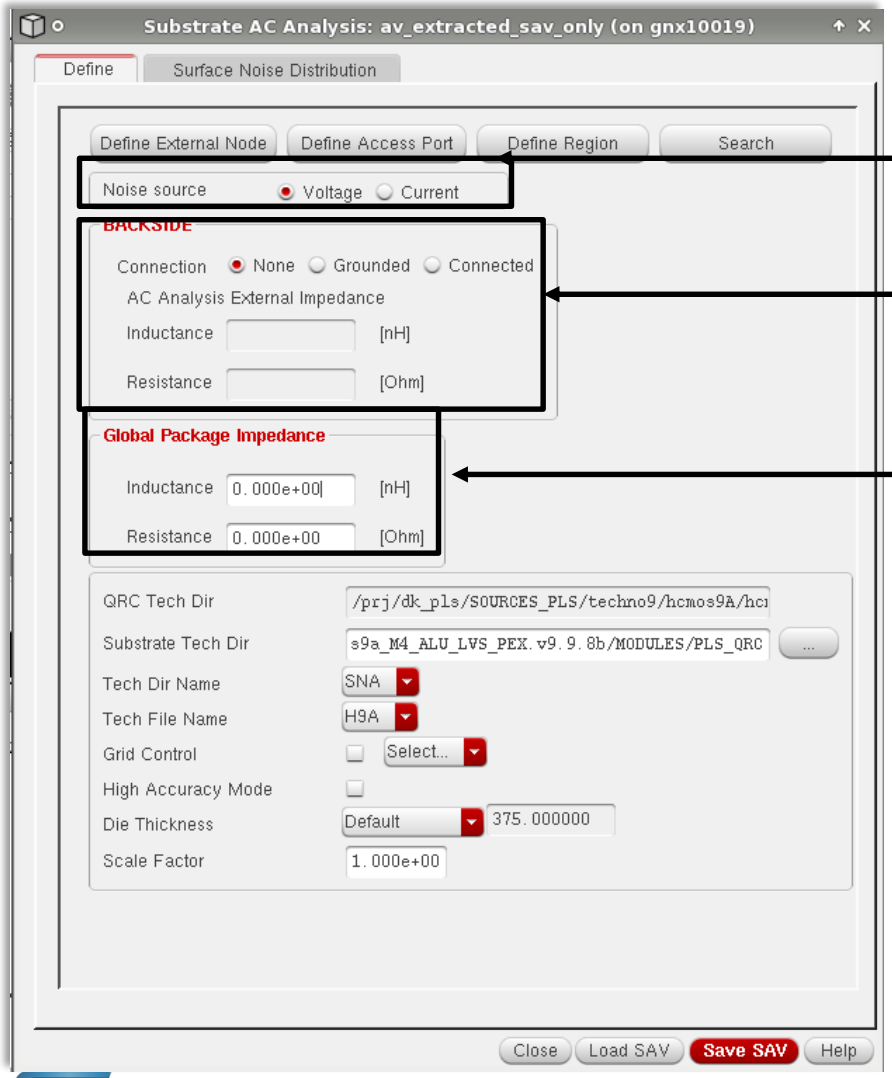
- Surface Noise Distribution (SND) :



- **External nodes** can be identified thanks with 2 ways :
- By picking shape from layout
  - Name of the node will be shown in "**Define Access Port**"
- By selecting name from "**Search**" menu :
  - Layout shape will be highlighted (and zoomed in)

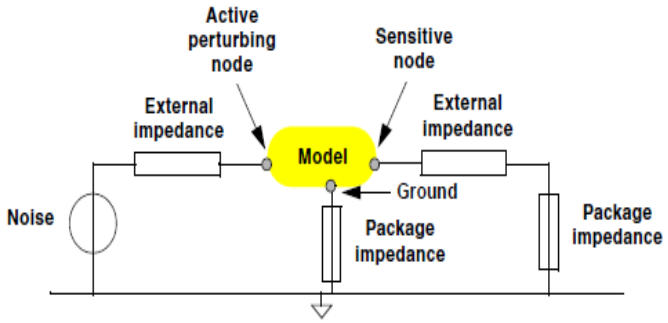
QRC Graphical User Interface

- Surface Noise Distribution (SND) :



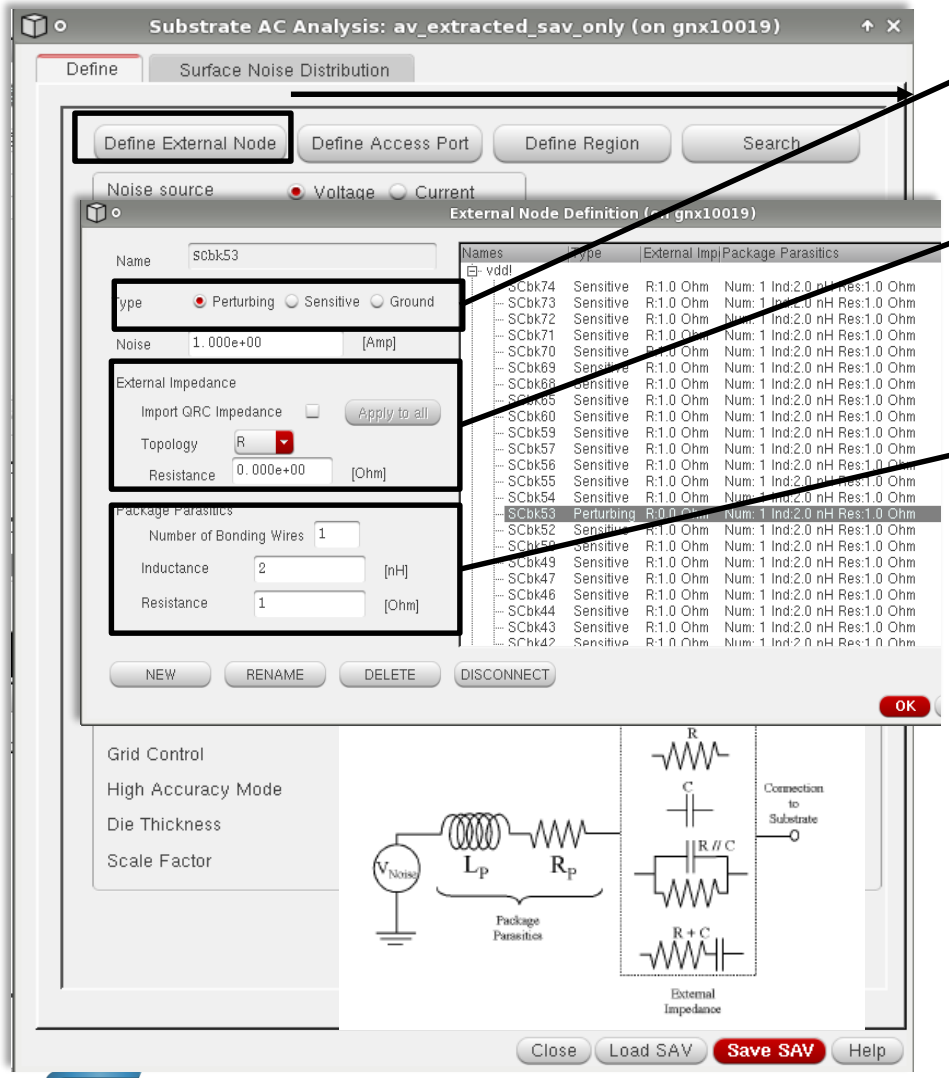
- The **external nodes** are the ports of the substrate parasitic network.
- The **noise source** will be selected among these ports.
- User can select either **Voltage** or **Current** noise, as perturbing source
- Specifies the type of backside connection (if any)
- Global Package Impedance can be defined to reflect the parasitics of bonding wires connected to **grounded** and **sensitive** nets

Figure 5-13 Setting Node Characteristics



QRC Graphical User Interface

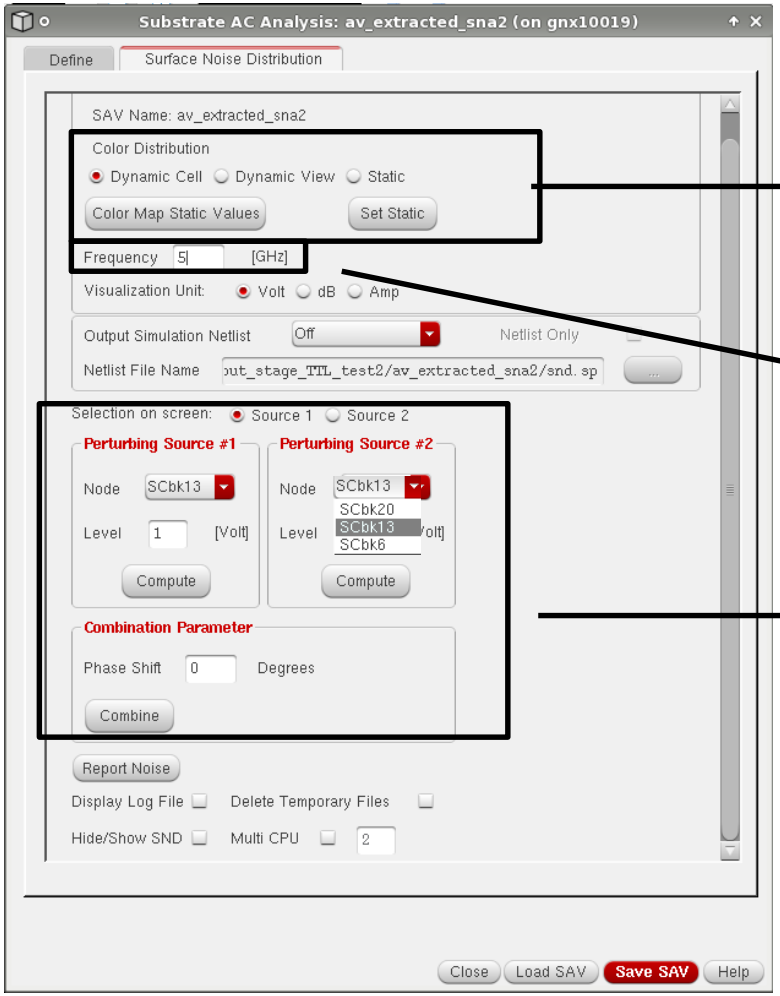
- Surface Noise Distribution (SND) :



- **"Define External node** " allows to define the type and the characteristics of each substrate nodes :
- By default, all substrate nodes are defined as "**sensitive**" (i.e. null noise level)
  - **External impedance** should be defined to estimate the parasitics of interconnects
    - It can be manually specified thanks to the equivalent RC network
    - It can be directly imported from a previous QRC extraction
  - **Bonding wires** could also be defined
    - If already defined, impedance defined on main SND interface will be automatically pre-filled
    - It can be manually defined to overwrite the global package definition
  - Those nodes will be used to study the propagation of the noise source
- Nodes intended to **shield** some region of the chips should be defined as **grounded**
  - **External impedance** is useless (always zero)
  - **Bonding wires** could also be defined (same methodology as sensitive nodes)
- **One or several perturbing** node should be defined as locations for noise injection in the substrate.
  - **Noise voltage** is useless. It will be defined later.
  - **External impedance** should be defined to represent the parasitics of interconnects (same methodology as sensitive nodes)
  - Number of **bonding wires** is useless

QRC Graphical User Interface

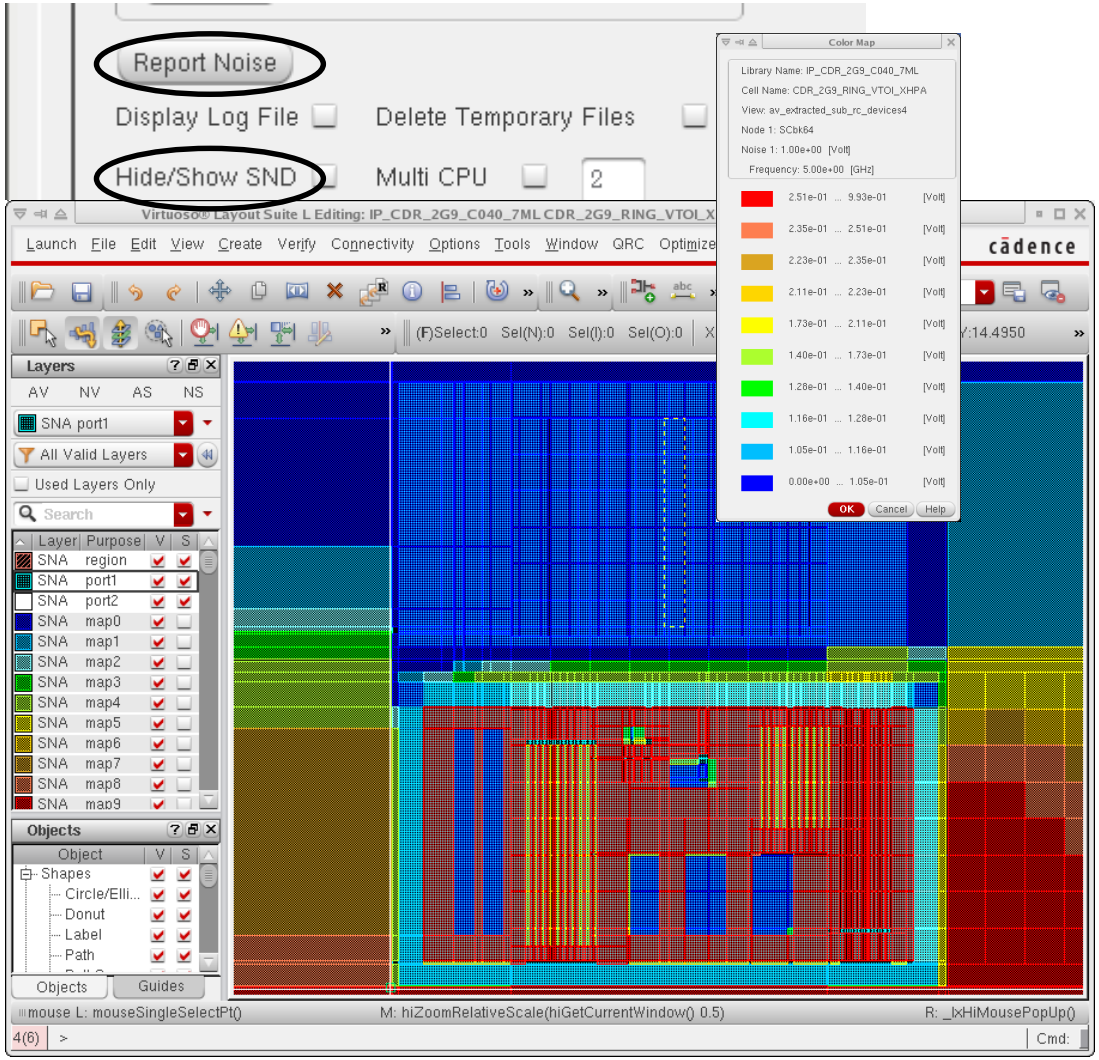
- Surface Noise Distribution (SND) :



- Once the perturbing node(s) have been defined, SND analysis can be run.
- The potential distribution along the substrate will be displayed thanks to **a color map**. This color map can be :
  - **dynamic** (the tool automatically sets the scale to give the best visual effect)
  - **static** (the color map is kept constant to facilitate the comparison among successive runs). The values have to be defined by the user.
- **Frequency** of SND analysis has to be defined
- **Perturbing nodes selections** :
  - If several perturbing nodes have been defined in the previous tab, the SND analysis can be run with **1 or 2 noise sources**
  - **Independent analysis** :
    - Select the noise source #1 **or** #2 and click on **compute**
  - **Combined analysis** :
    - Select the noise sources #1 **and** #2, define the phase shift between the 2 voltages and click on **Combine**

QRC Graphical User Interface

- Surface Noise Distribution (SND) :

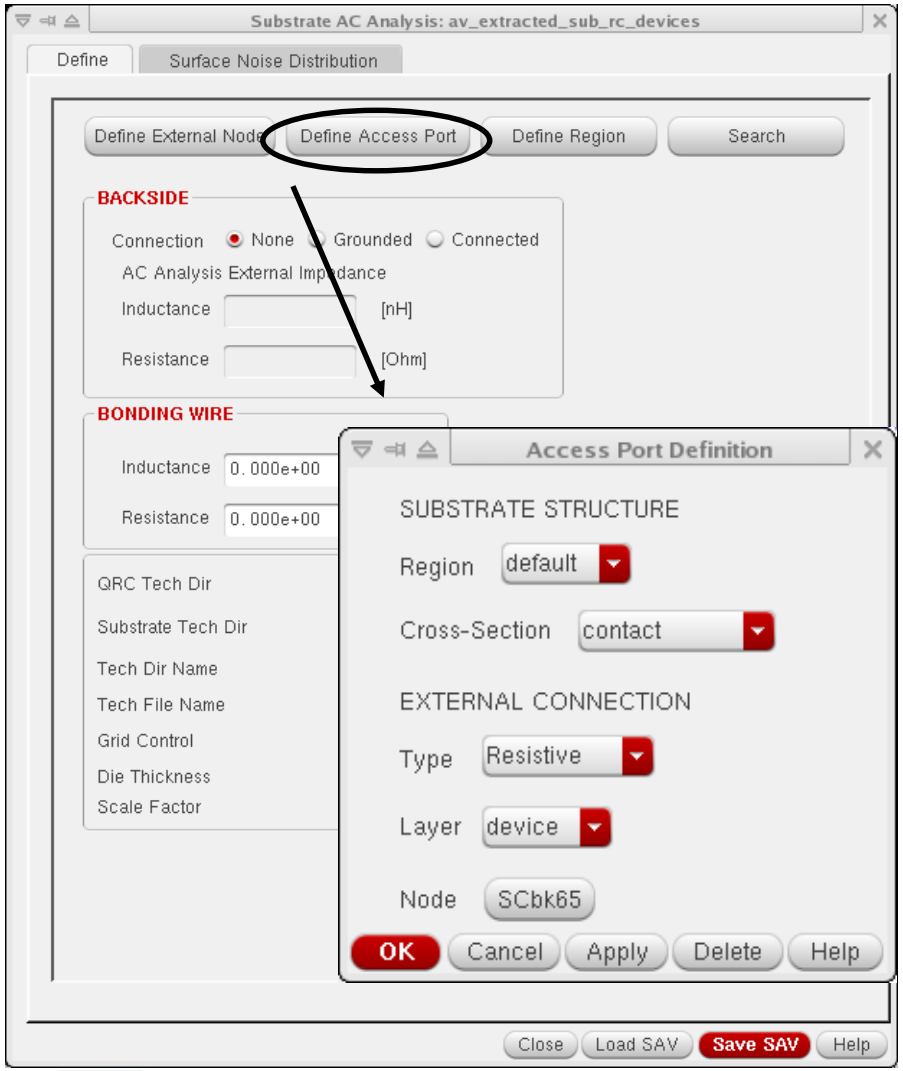


- After SND Analysis, the previously defined **color map** shows the voltage distribution overlaid on the layout.
- It can be easily switch on or off with the **Hide/Show** button
- The scale can be translated from **Volt/Amp** to **dB**.
- **Potentials** of all sensitive nodes can be dumped into a txt file in the current working directory
- User can **probe** noise of specific areas directly by **clicking on the layout**. The data will be added to the txt file

```
52 Net Name: "SCbk42" Potential: 1.328e-05 [Volt] -9.754e+01 [dB]
53 Net Name: "SCbk43" Potential: 1.333e-05 [Volt] -9.750e+01 [dB]
54 Net Name: "SCbk44" Potential: 7.656e-06 [Volt] -1.023e+02 [dB]
55 Net Name: "SCbk45" Potential: 9.587e-06 [Volt] -1.004e+02 [dB]
56 Net Name: "SCbk46" Potential: 1.155e-05 [Volt] -9.875e+01 [dB]
57 Net Name: "SCbk47" Potential: 1.141e-05 [Volt] -9.886e+01 [dB]
58 Net Name: "SCbk48" Potential: 1.135e-05 [Volt] -9.890e+01 [dB]
59 Net Name: "SCbk49" Potential: 1.051e-05 [Volt] -9.957e+01 [dB]
60 Net Name: "SCbk50" Potential: 1.049e-05 [Volt] -9.959e+01 [dB]
61 Net Name: "SCbk51" Potential: 1.045e-05 [Volt] -9.962e+01 [dB]
62 Net Name: "SCbk52" Potential: 1.143e-05 [Volt] -9.884e+01 [dB]
63 Net Name: "SCbk53" Potential: 1.146e-05 [Volt] -9.882e+01 [dB]
64 Net Name: "SCbk54" Potential: 9.683e-06 [Volt] -1.003e+02 [dB]
65 Net Name: "SCbk55" Potential: 8.954e-06 [Volt] -1.010e+02 [dB]
66 Net Name: "SCbk56" Potential: 8.799e-06 [Volt] -1.011e+02 [dB]
67 Net Name: "SCbk57" Potential: 3.364e-05 [Volt] -8.946e+01 [dB]
68 Net Name: "SCbk58" Potential: 5.289e-04 [Volt] -6.553e+01 [dB]
69 Net Name: "SCbk59" Potential: 9.765e-05 [Volt] -8.021e+01 [dB]
70
71 USER SELECTION SECTION
72 Location: 10.71 3.8345 Potential: 2.002e-02 [Volt] -3.397e+01 [dB]
73 Location: 8.625 5.5915 Potential: 1.856e-03 [Volt] -5.463e+01 [dB]
```

QRC Graphical User Interface

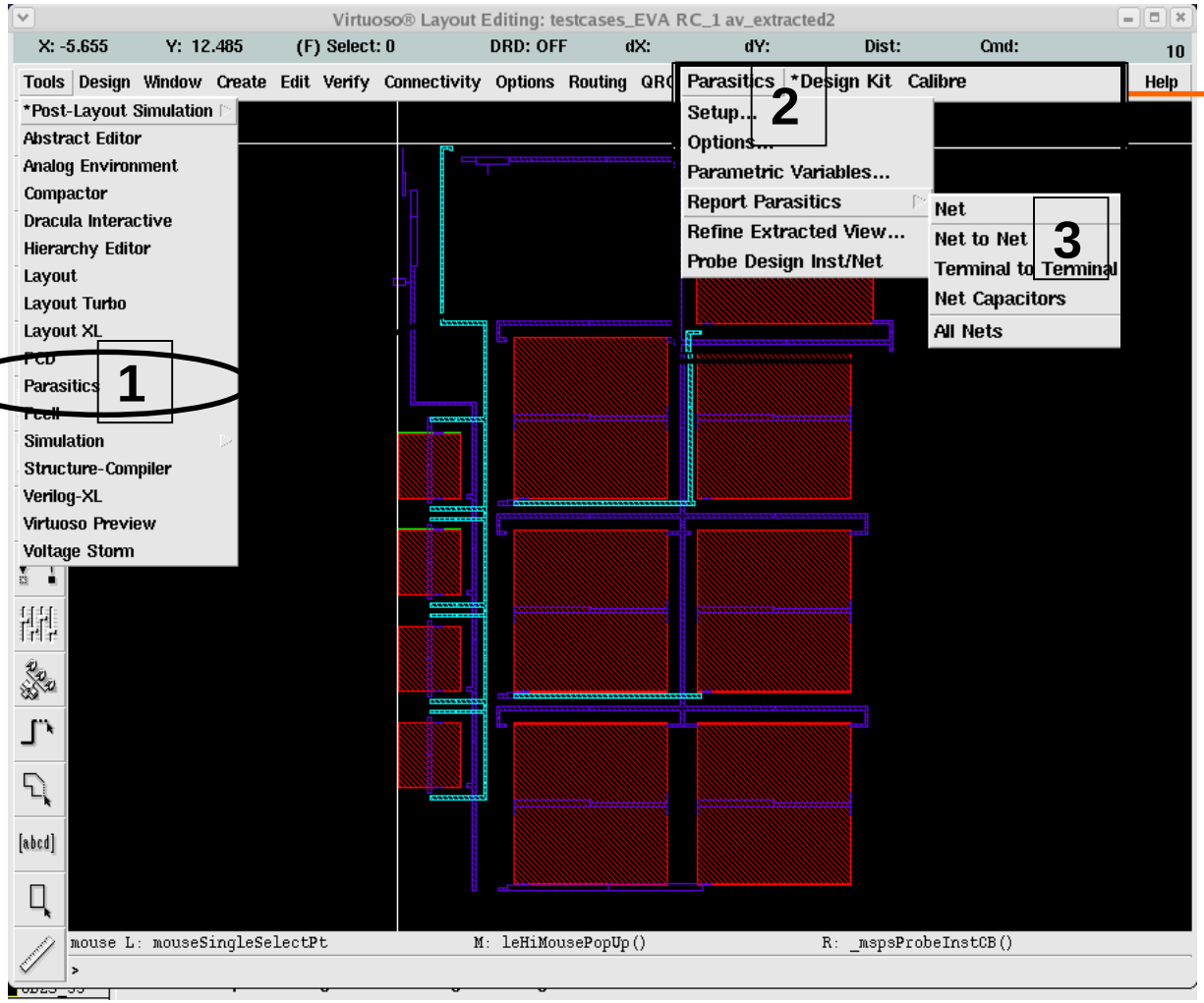
- Surface Noise Distribution (SND) :



- New **access port** can be defined to perform "What if" analysis. It allows to anticipate the effects of layout modifications such as adding a **new device** or adding a **guarding.**
- New **access port** can be drawn on extracted view layout with the LSW layer "**SNA port1**"
- While the new port is highlighted on layout, click on "**Define Access Port**" to specify the parameters :
  - **Region** (default, nwell, deep-nwell)
  - **Cross-Section** (default, channel, contact, source_drain)
  - **Type** (resistive, capacitive)
  - **Layer**
  - **Node** (attach to an existing node or create a new one)
- **Re-run SND Analysis** and compare new results versus the previous ones.

QRC Extracted view's probing capabilities

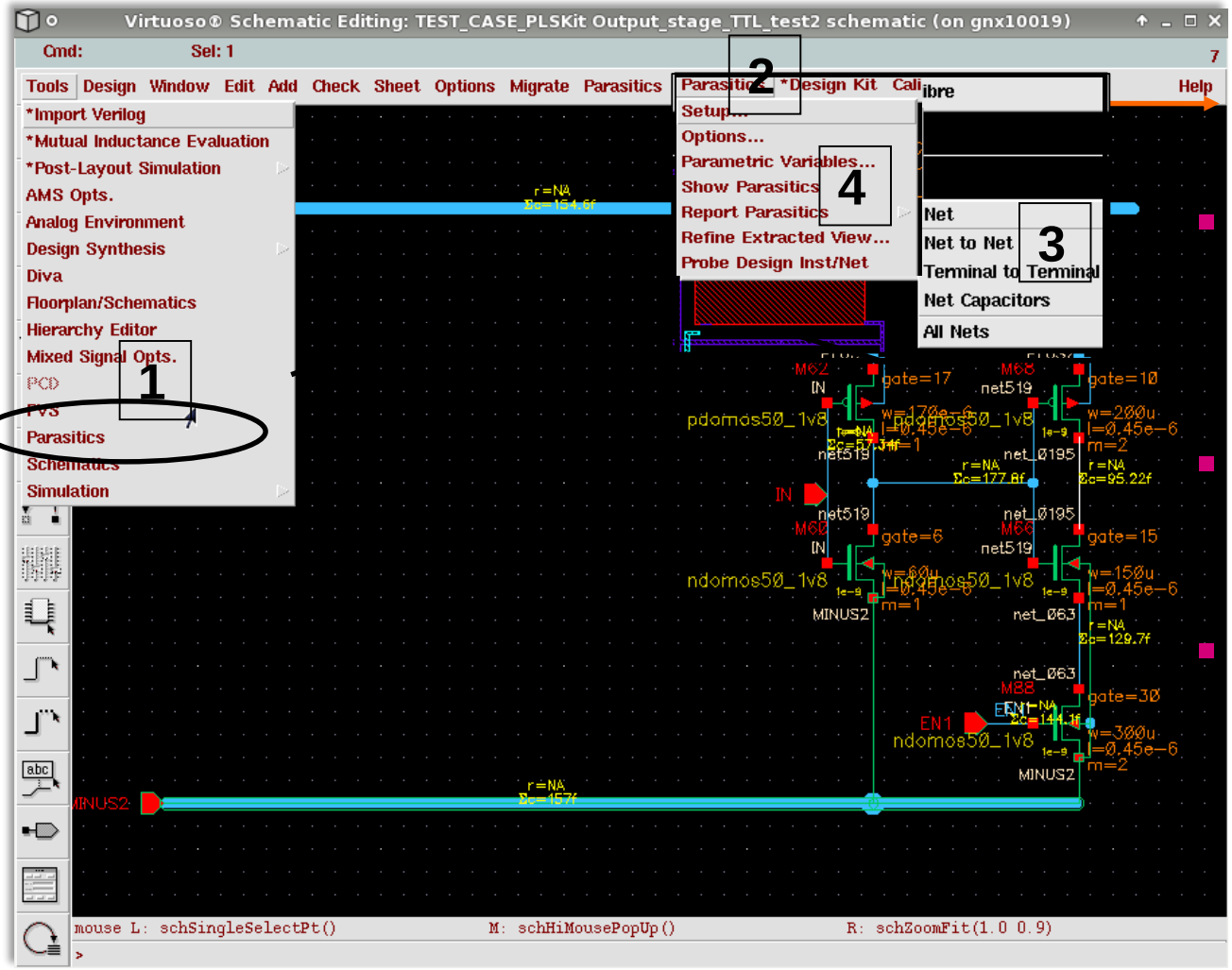
- From extracted view :



- 1. Enable **Parasitics menu** from **Tools -> Parasitics**
- 2. Open **Parasitics menu** to select **Setup** and click **OK**
- 3. Open **Parasitics menu** to select **Report Parasitics.** Several options are available :
  - **Net**
  - **Net to Net**
  - **Terminal to Terminal**
  - **Net Capacitors**
  - **All Nets**

QRC Extracted view's probing capabilities

- From schematic view :



1. Enable **Parasitics menu** from **Tools -> Parasitics**

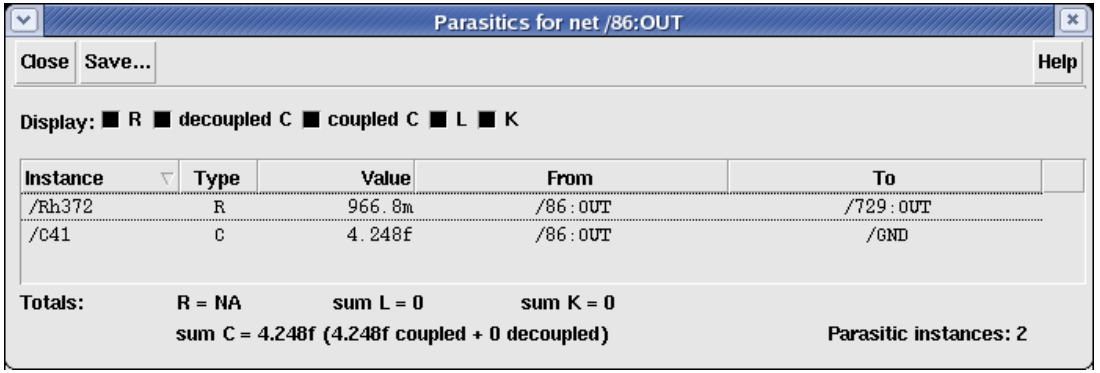
2. Open **Parasitics menu** to select **Setup** and click **OK**

3. Same functionalities as from extracted view

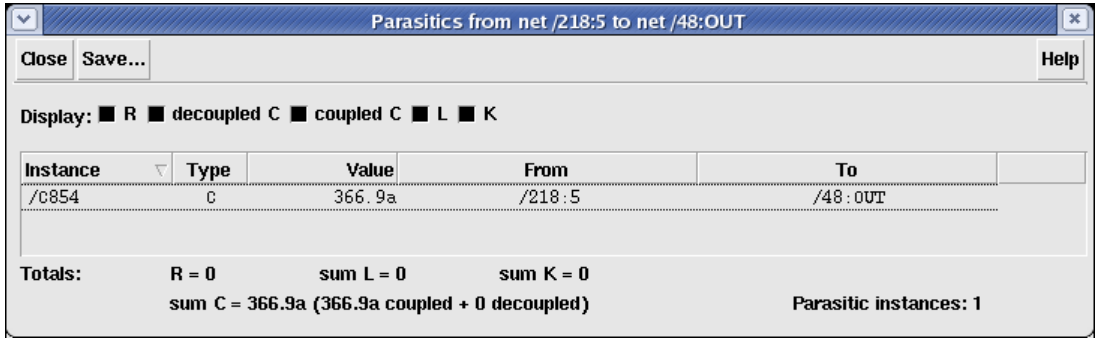
4. Parasitics can be **back-annotated** on schematic nets

QRC Extracted view's probing capabilities

- **Report Parasitics -> Net** displays **all parasitics** related to the selected net on extracted view :



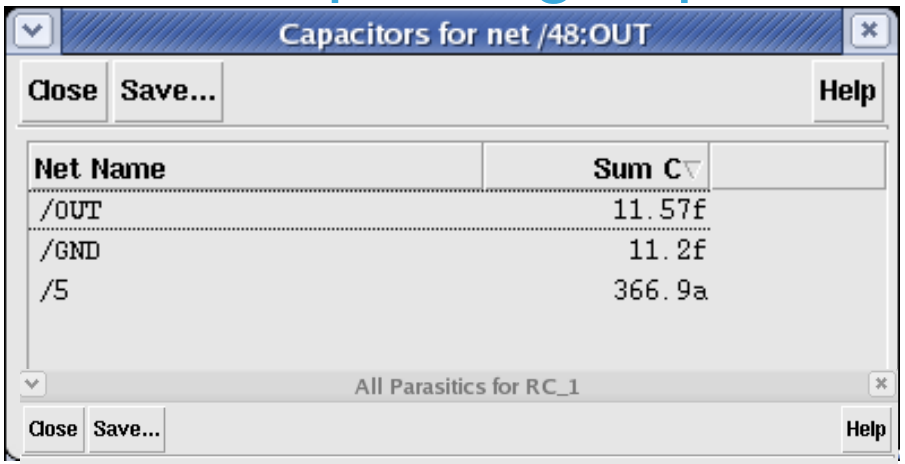
- **Report Parasitics -> Net to Net** displays parasitic capacitors between the 2 selected nets on extracted view :



- **Report Parasitics -> Terminal to Terminal** displays parasitic resistors between the 2 selected terminals on extracted view :

QRC Extracted view's probing capabilities

- **Report Parasitics -> Net Capacitors** displays all parasitic capacitors related to the selected net on extracted view :



- **Report Parasitics -> All Nets** displays all parasitics for all nets of the design :

What's new in PDK 28FDSOI 2.3 ?

- QRC version : PVE 12.1.1 (12.11.076)
  - First release

- Know limitations :

CCR number	Description
1003714	Global Frequency should be in Substrate tab
1132535	QRC vs QRCFS large diff on 40nm
1098418	Improve GUI usage model for: Import QRC Impedance Apply to all
1067254	Figure 5-12 doesn't apply to sensitive nodes - DOC needs to be corrected
994139	Have snarcr to run multi-cpu
1102685	qrcToDfII fails if thumbnail is present
1121626	QRC fails with Conly+extracted_view+selected_nets_proper+parasiticblocking_device_cells_file
1054394	substrateStormPP in QRC-SNA
1110678	extview.trp to transfert model even if different from spice model
1116057	Please, remove Return Limited mode from GUI
1125887	Terminal to Terminal probing doesn't work for MOS devices in QCI flow
1084623	QRC setup should have peecMode t as default and new peecModeReadOnly
1133845	DSPF output does not honor -exclude_self_cap false
1135305	Parasitics Probing Report has wrong sumC calculation in case of exclude_self_cap=false
1119329	QRC UI generates incorrect CCL file for default resistance mesh setting