C28SOI_SC_12_COREPBP16_LL Databook

12 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 16 nm

Overview

- C28SOI_SC_12_COREPBP16_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 383 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

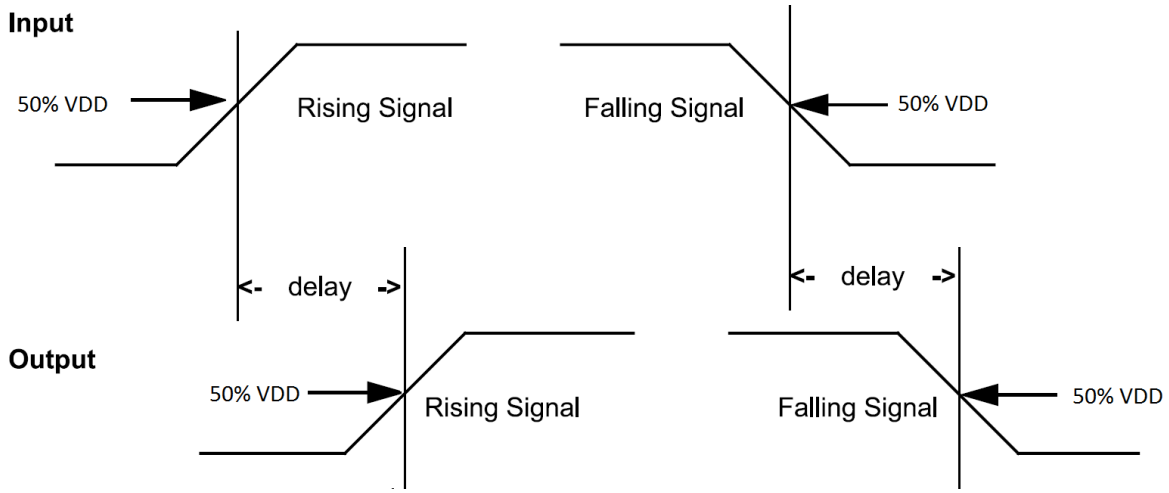


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

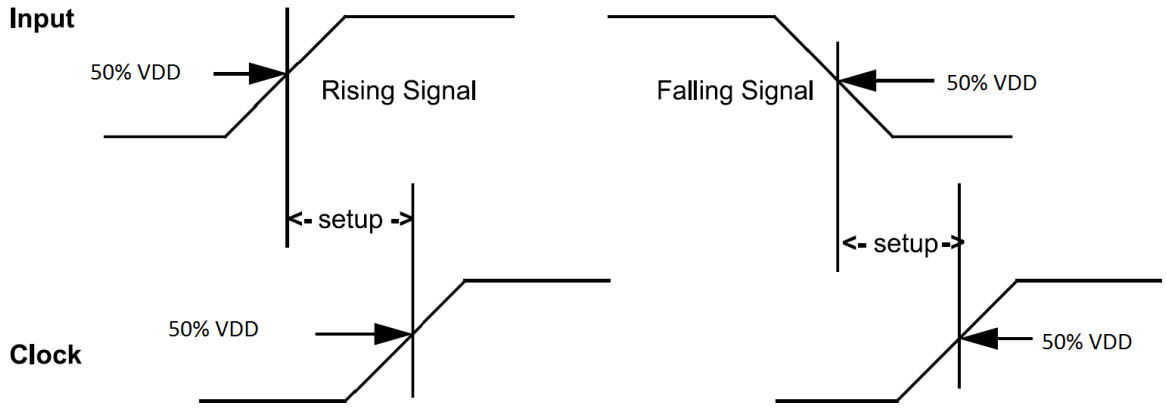


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

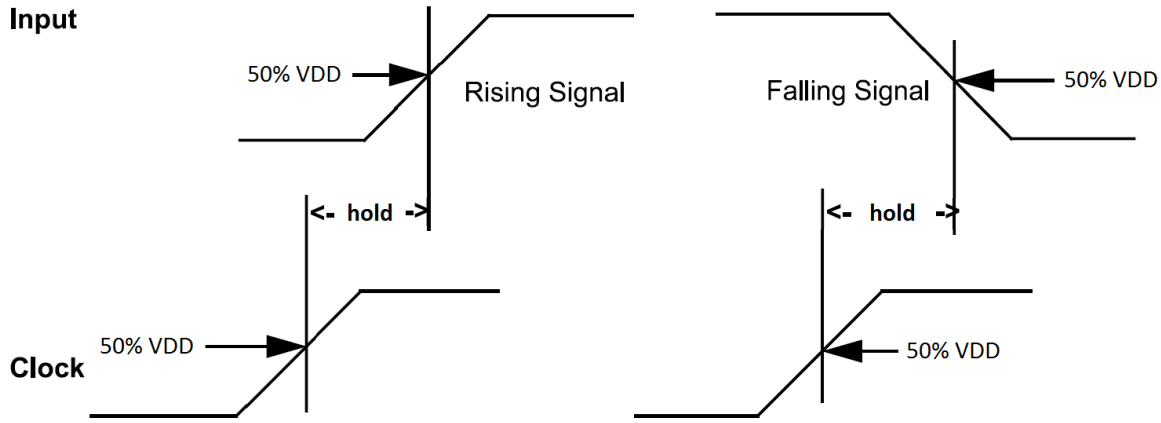


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

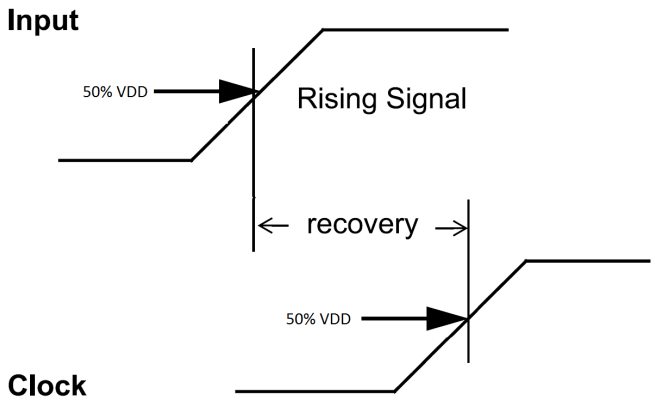


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

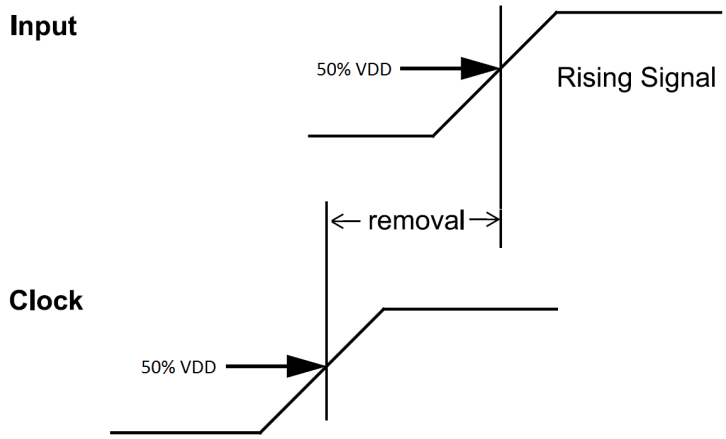


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

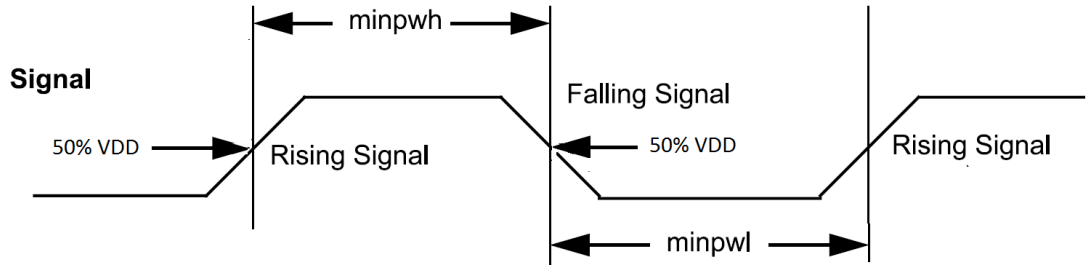


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

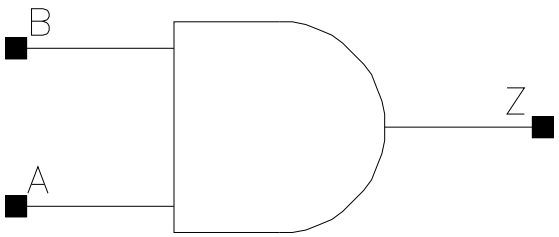
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X25_P16	1.200	1.088	1.3056
X33_P16	1.200	1.360	1.6320
X42_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0008	0.0012	0.0017	0.0022
B	0.0007	0.0011	0.0017	0.0022
	X42_P16			
A	0.0021			
B	0.0022			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0424	0.0343	2.6737	1.3566
A to Z ↑	0.0344	0.0315	4.5487	2.2295
B to Z ↓	0.0403	0.0322	2.6769	1.3575
B to Z ↑	0.0360	0.0327	4.5543	2.2294
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0355	0.0341	0.8964	0.6665

A to Z ↑	0.0311	0.0317	1.4646	1.1032
B to Z ↓	0.0335	0.0310	0.8967	0.6653
B to Z ↑	0.0325	0.0318	1.4631	1.1030
	X42_P16		**X42_P16**	
A to Z ↓	0.0369		0.5411	
A to Z ↑	0.0347		0.8839	
B to Z ↓	0.0340		0.5401	
B to Z ↑	0.0350		0.8832	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	4.466e-06	1.000e-20
X16_P16	9.260e-06	1.000e-20
X25_P16	1.363e-05	1.000e-20
X33_P16	1.889e-05	1.000e-20
X42_P16	2.186e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	8.173e-06	1.615e-05	2.508e-05	6.616e-05
B (output stable)	1.876e-05	3.376e-05	5.278e-05	2.811e-04
A to Z	2.049e-03	3.362e-03	5.213e-03	6.859e-03
B to Z	1.939e-03	3.159e-03	4.906e-03	6.176e-03
	X42_P16			
A (output stable)	6.716e-05			
B (output stable)	2.781e-04			
A to Z	8.272e-03			
B to Z	7.590e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

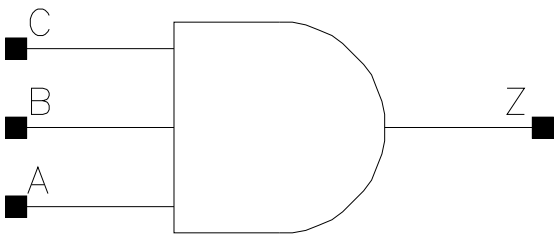
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X25_P16	1.200	1.360	1.6320
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0007	0.0011	0.0018	0.0022
B	0.0006	0.0011	0.0016	0.0021
C	0.0006	0.0011	0.0015	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0458	0.0377	2.7070	1.3213
A to Z ↑	0.0451	0.0412	4.5983	2.2021
B to Z ↓	0.0442	0.0359	2.7052	1.3200
B to Z ↑	0.0453	0.0414	4.5942	2.2033
C to Z ↓	0.0423	0.0339	2.7022	1.3193
C to Z ↑	0.0464	0.0416	4.5979	2.2021
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0380	0.0359	0.9050	0.6767

A to Z ↑	0.0406	0.0390	1.4937	1.1185
B to Z ↓	0.0364	0.0342	0.9040	0.6764
B to Z ↑	0.0410	0.0393	1.4923	1.1199
C to Z ↓	0.0343	0.0323	0.9034	0.6760
C to Z ↑	0.0413	0.0396	1.4938	1.1194

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	4.205e-06	1.000e-20
X17_P16	9.032e-06	1.000e-20
X25_P16	1.291e-05	1.000e-20
X33_P16	1.766e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	1.003e-05	2.120e-05	2.767e-05	3.873e-05
B (output stable)	1.986e-05	4.304e-05	5.967e-05	8.372e-05
C (output stable)	5.074e-05	1.032e-04	1.504e-04	2.114e-04
A to Z	2.267e-03	3.933e-03	5.736e-03	7.374e-03
B to Z	2.153e-03	3.719e-03	5.418e-03	6.943e-03
C to Z	2.059e-03	3.511e-03	5.108e-03	6.518e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

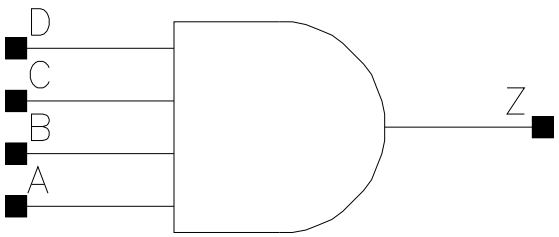
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X6_P16	1.200	1.088	1.3056
X20_P16	1.200	2.312	2.7744
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X4_P16	X6_P16	X20_P16	X27_P16
A	0.0005	0.0008	0.0019	0.0021
B	0.0005	0.0008	0.0019	0.0022
C	0.0005	0.0008	0.0019	0.0022
D	0.0005	0.0008	0.0019	0.0022

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X6_P16	X4_P16	X6_P16
A to Z ↓	0.0485	0.0413	5.0994	3.3063
A to Z ↑	0.0466	0.0359	15.4420	8.1472
B to Z ↓	0.0472	0.0388	5.1065	3.3029
B to Z ↑	0.0484	0.0370	15.4481	8.1460
C to Z ↓	0.0502	0.0440	5.0812	3.3252
C to Z ↑	0.0461	0.0350	15.4463	8.1686

D to Z ↓	0.0487	0.0408	5.0792	3.3198
D to Z ↑	0.0489	0.0362	15.4733	8.1685
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0400	0.0368	0.9569	0.6752
A to Z ↑	0.0373	0.0413	2.7035	2.0457
B to Z ↓	0.0363	0.0338	0.9547	0.6738
B to Z ↑	0.0373	0.0416	2.7031	2.0460
C to Z ↓	0.0387	0.0354	0.9633	0.6783
C to Z ↑	0.0325	0.0354	2.7016	2.0448
D to Z ↓	0.0348	0.0325	0.9609	0.6763
D to Z ↑	0.0324	0.0358	2.7037	2.0444

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	2.325e-06	1.000e-20
X6_P16	5.710e-06	1.000e-20
X20_P16	1.710e-05	1.000e-20
X27_P16	2.163e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	3.582e-04	5.639e-04	1.682e-03	2.046e-03
B (output stable)	3.343e-04	5.090e-04	1.527e-03	1.885e-03
C (output stable)	3.393e-04	5.611e-04	1.441e-03	1.784e-03
D (output stable)	3.204e-04	5.027e-04	1.273e-03	1.615e-03
A to Z	1.471e-03	2.303e-03	7.040e-03	9.049e-03
B to Z	1.405e-03	2.160e-03	6.402e-03	8.398e-03
C to Z	1.438e-03	2.302e-03	5.903e-03	7.368e-03
D to Z	1.373e-03	2.149e-03	5.253e-03	6.724e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

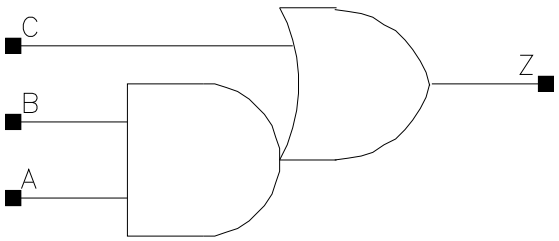
Pin Cycle (vdds)	X4_P16	X6_P16	X20_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0010	0.0021
B	0.0007	0.0011	0.0020
C	0.0008	0.0012	0.0021

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0531	0.0466	2.7565	1.3485
A to Z ↑	0.0355	0.0315	4.4729	2.1837
B to Z ↓	0.0493	0.0431	2.7479	1.3427
B to Z ↑	0.0374	0.0334	4.4736	2.1802
C to Z ↓	0.0532	0.0468	2.7422	1.3424
C to Z ↑	0.0319	0.0297	4.4428	2.1702
	X33_P16		**X33_P16**	
A to Z ↓	0.0468		0.6827	
A to Z ↑	0.0322		1.0987	

B to Z ↓	0.0431		0.6811	
B to Z ↑	0.0332		1.0970	
C to Z ↓	0.0468		0.6800	
C to Z ↑	0.0292		1.0926	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	4.734e-06	1.000e-20
X17_P16	9.767e-06	1.000e-20
X33_P16	1.955e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.810e-05	3.313e-05	8.109e-05
B (output stable)	2.181e-05	4.040e-05	1.205e-04
C (output stable)	4.209e-05	7.148e-05	1.683e-04
A to Z	2.104e-03	3.619e-03	7.244e-03
B to Z	1.991e-03	3.402e-03	6.692e-03
C to Z	2.326e-03	4.009e-03	7.977e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

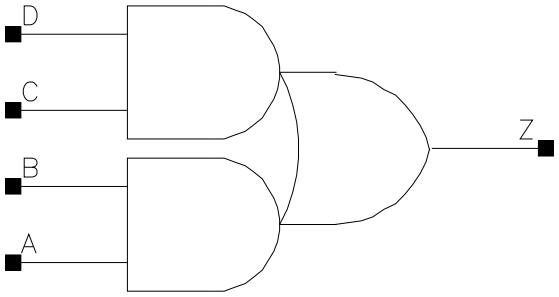
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0006	0.0010	0.0021
B	0.0007	0.0011	0.0019
C	0.0006	0.0010	0.0021
D	0.0007	0.0011	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0619	0.0529	2.6528	1.3342
A to Z ↑	0.0454	0.0405	4.3993	2.1890
B to Z ↓	0.0576	0.0491	2.6392	1.3296
B to Z ↑	0.0461	0.0416	4.3983	2.1879

C to Z ↓	0.0547	0.0476	2.6422	1.3299
C to Z ↑	0.0382	0.0342	4.3888	2.1807
D to Z ↓	0.0523	0.0451	2.6358	1.3270
D to Z ↑	0.0406	0.0361	4.3869	2.1822
	X33_P16		**X33_P16**	
A to Z ↓	0.0506		0.6829	
A to Z ↑	0.0374		1.1035	
B to Z ↓	0.0478		0.6821	
B to Z ↑	0.0393		1.1036	
C to Z ↓	0.0453		0.6815	
C to Z ↑	0.0321		1.0991	
D to Z ↓	0.0425		0.6801	
D to Z ↑	0.0338		1.0985	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	5.509e-06	1.000e-20
X17_P16	1.141e-05	1.000e-20
X33_P16	2.166e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	2.361e-05	3.398e-05	4.918e-05
B (output stable)	1.134e-04	1.404e-04	6.893e-05
C (output stable)	2.199e-05	4.287e-05	9.266e-05
D (output stable)	2.722e-05	5.402e-05	1.178e-04
A to Z	2.813e-03	4.689e-03	8.749e-03
B to Z	2.587e-03	4.338e-03	8.286e-03
C to Z	2.352e-03	3.944e-03	7.277e-03
D to Z	2.254e-03	3.744e-03	6.854e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

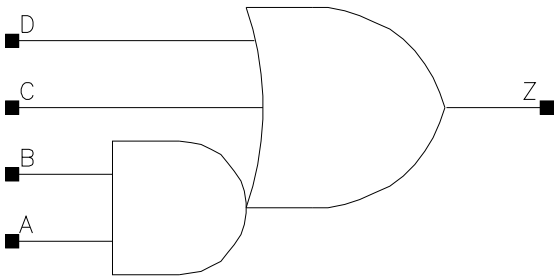
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	0.952	1.1424
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0006	0.0010	0.0019
B	0.0006	0.0010	0.0019
C	0.0007	0.0010	0.0020
D	0.0007	0.0010	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0700	0.0598	2.8920	1.4191
A to Z ↑	0.0382	0.0340	4.4658	2.2390
B to Z ↓	0.0669	0.0557	2.8844	1.4138
B to Z ↑	0.0405	0.0354	4.4654	2.2400
C to Z ↓	0.0751	0.0639	2.8792	1.4142
C to Z ↑	0.0344	0.0315	4.4359	2.2265

D to Z ↓	0.0733	0.0632	2.8808	1.4146
D to Z ↑	0.0339	0.0313	4.4303	2.2267
	X33_P16		**X33_P16**	
A to Z ↓	0.0608		0.7106	
A to Z ↑	0.0342		1.0996	
B to Z ↓	0.0543		0.7063	
B to Z ↑	0.0346		1.0991	
C to Z ↓	0.0660		0.7077	
C to Z ↑	0.0310		1.0955	
D to Z ↓	0.0634		0.7076	
D to Z ↑	0.0300		1.0922	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	4.306e-06	1.000e-20
X17_P16	8.966e-06	1.000e-20
X33_P16	1.824e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.565e-05	3.227e-05	8.665e-05
B (output stable)	1.671e-05	3.381e-05	1.181e-04
C (output stable)	2.160e-05	4.180e-05	1.244e-04
D (output stable)	1.935e-05	3.946e-05	1.190e-04
A to Z	2.349e-03	3.947e-03	7.945e-03
B to Z	2.252e-03	3.721e-03	7.231e-03
C to Z	2.700e-03	4.560e-03	9.354e-03
D to Z	2.546e-03	4.292e-03	8.570e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

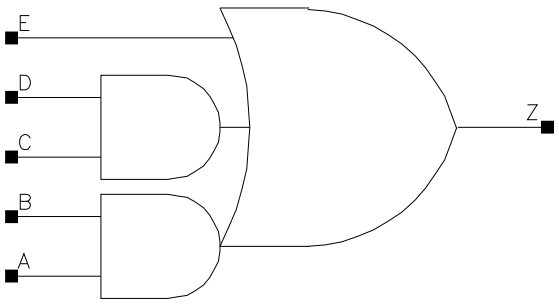
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.088	1.3056
X17_P16	1.200	1.224	1.4688
X33_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0006	0.0010	0.0020
B	0.0007	0.0010	0.0018
C	0.0008	0.0012	0.0020
D	0.0007	0.0010	0.0019
E	0.0007	0.0010	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0878	0.0730	2.7599	1.3789
A to Z ↑	0.0478	0.0409	4.3859	2.1992

B to Z ↓	0.0849	0.0695	2.7506	1.3747
B to Z ↑	0.0506	0.0431	4.3853	2.1980
C to Z ↓	0.0729	0.0621	2.7463	1.3731
C to Z ↑	0.0405	0.0344	4.3476	2.1824
D to Z ↓	0.0680	0.0567	2.7343	1.3673
D to Z ↑	0.0425	0.0360	4.3479	2.1848
E to Z ↓	0.0767	0.0638	2.7318	1.3673
E to Z ↑	0.0359	0.0312	4.3142	2.1707
	X33_P16		**X33_P16**	
A to Z ↓	0.0725		0.7103	
A to Z ↑	0.0424		1.1092	
B to Z ↓	0.0677		0.7081	
B to Z ↑	0.0439		1.1085	
C to Z ↓	0.0600		0.7070	
C to Z ↑	0.0345		1.0999	
D to Z ↓	0.0551		0.7041	
D to Z ↑	0.0359		1.1003	
E to Z ↓	0.0624		0.7044	
E to Z ↑	0.0311		1.0927	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	5.283e-06	1.000e-20
X17_P16	1.079e-05	1.000e-20
X33_P16	2.020e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.349e-05	2.207e-05	5.201e-05
B (output stable)	1.811e-05	2.590e-05	7.192e-05
C (output stable)	2.819e-05	4.246e-05	1.024e-04
D (output stable)	3.219e-05	5.092e-05	1.259e-04
E (output stable)	5.767e-05	1.004e-04	2.227e-04
A to Z	3.259e-03	5.233e-03	1.036e-02
B to Z	3.164e-03	5.003e-03	9.749e-03
C to Z	2.553e-03	4.147e-03	8.019e-03
D to Z	2.432e-03	3.898e-03	7.463e-03
E to Z	2.802e-03	4.496e-03	8.719e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

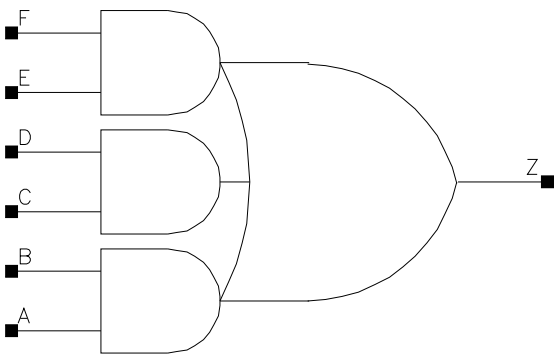
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.360	1.6320
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
A	0.0006	0.0007	0.0010	0.0020

B	0.0006	0.0008	0.0013	0.0018
C	0.0006	0.0007	0.0010	0.0019
D	0.0006	0.0007	0.0009	0.0018
E	0.0007	0.0008	0.0010	0.0020
F	0.0007	0.0008	0.0010	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0874	0.0823	5.3510	2.7443
A to Z ↑	0.0508	0.0484	8.7998	4.4387
B to Z ↓	0.0802	0.0761	5.3143	2.7263
B to Z ↑	0.0511	0.0491	8.7958	4.4378
C to Z ↓	0.0785	0.0746	5.3293	2.7345
C to Z ↑	0.0458	0.0435	8.7481	4.4130
D to Z ↓	0.0750	0.0713	5.3132	2.7252
D to Z ↑	0.0483	0.0460	8.7410	4.4128
E to Z ↓	0.0644	0.0629	5.3044	2.7223
E to Z ↑	0.0387	0.0371	8.6963	4.3917
F to Z ↓	0.0601	0.0587	5.2867	2.7128
F to Z ↑	0.0406	0.0389	8.6972	4.3905
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
A to Z ↓	0.0782	0.0753	1.3838	0.7089
A to Z ↑	0.0451	0.0454	2.2066	1.1135
B to Z ↓	0.0738	0.0710	1.3752	0.7073
B to Z ↑	0.0469	0.0470	2.2047	1.1129
C to Z ↓	0.0720	0.0694	1.3797	0.7080
C to Z ↑	0.0408	0.0419	2.1943	1.1059
D to Z ↓	0.0680	0.0655	1.3740	0.7063
D to Z ↑	0.0430	0.0436	2.1940	1.1060
E to Z ↓	0.0604	0.0614	1.3735	0.7060
E to Z ↑	0.0344	0.0364	2.1854	1.1027
F to Z ↓	0.0564	0.0568	1.3688	0.7033
F to Z ↑	0.0362	0.0380	2.1857	1.1028

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	4.135e-06	1.000e-20
X8_P16	6.960e-06	1.000e-20
X17_P16	1.234e-05	1.000e-20
X33_P16	2.283e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	2.538e-05	2.964e-05	3.781e-05	7.268e-05
B (output stable)	8.651e-05	9.489e-05	9.843e-05	1.107e-04
C (output stable)	2.058e-05	2.585e-05	3.640e-05	7.408e-05
D (output stable)	2.506e-05	3.166e-05	4.403e-05	1.183e-04
E (output stable)	4.497e-05	5.435e-05	7.338e-05	1.232e-04
F (output stable)	4.821e-05	5.779e-05	8.109e-05	1.554e-04

A to Z	2.913e-03	3.884e-03	5.883e-03	1.123e-02
B to Z	2.669e-03	3.596e-03	5.511e-03	1.063e-02
C to Z	2.445e-03	3.325e-03	5.141e-03	9.826e-03
D to Z	2.344e-03	3.191e-03	4.917e-03	9.294e-03
E to Z	1.948e-03	2.758e-03	4.294e-03	8.520e-03
F to Z	1.841e-03	2.614e-03	4.066e-03	7.992e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

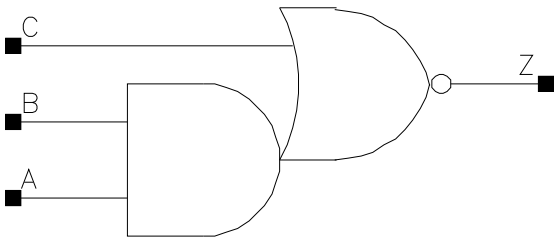
Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008
X44_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X33_P16	X44_P16
A	0.0008	0.0025	0.0049	0.0066
B	0.0008	0.0023	0.0045	0.0059
C	0.0009	0.0026	0.0051	0.0067

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0132	0.0140	4.8949	1.6540
A to Z ↑	0.0225	0.0231	8.2629	2.7399
B to Z ↓	0.0134	0.0137	4.9255	1.6679
B to Z ↑	0.0183	0.0182	8.1847	2.7420
C to Z ↓	0.0137	0.0139	2.7084	0.9216
C to Z ↑	0.0241	0.0241	7.5521	2.5186
	X33_P16	**X44_P16**	**X33_P16**	**X44_P16**
A to Z ↓	0.0144	0.0143	0.8372	0.6343

A to Z ↑	0.0231	0.0231	1.3706	1.0365
B to Z ↓	0.0136	0.0135	0.8450	0.6403
B to Z ↑	0.0180	0.0179	1.3701	1.0340
C to Z ↓	0.0156	0.0159	0.5494	0.4283
C to Z ↑	0.0245	0.0243	1.2582	0.9504

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P16	4.019e-06	1.000e-20
X17_P16	1.155e-05	1.000e-20
X33_P16	2.214e-05	1.000e-20
X44_P16	2.913e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	3.397e-05	1.073e-04	2.347e-04	3.085e-04
B (output stable)	4.035e-05	1.728e-04	3.833e-04	5.034e-04
C (output stable)	7.130e-05	2.219e-04	4.868e-04	6.346e-04
A to Z	9.339e-04	3.003e-03	6.079e-03	8.028e-03
B to Z	7.358e-04	2.170e-03	4.320e-03	5.692e-03
C to Z	1.362e-03	4.089e-03	8.335e-03	1.095e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

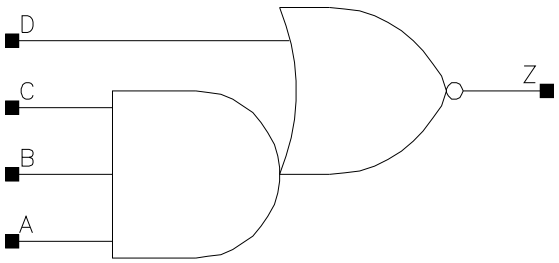
Pin Cycle (vdds)	X6_P16	X17_P16	X33_P16	X44_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X29_P16	1.200	3.536	4.2432
X38_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X29_P16	X38_P16
A	0.0009	0.0050	0.0065
B	0.0008	0.0048	0.0063
C	0.0008	0.0045	0.0060
D	0.0009	0.0051	0.0064

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X29_P16	X5_P16	X29_P16
A to Z ↓	0.0200	0.0214	7.1190	1.2148
A to Z ↑	0.0293	0.0291	8.2607	1.3615
B to Z ↓	0.0198	0.0203	7.1265	1.2182
B to Z ↑	0.0260	0.0256	8.2575	1.3679
C to Z ↓	0.0193	0.0186	7.1405	1.2218
C to Z ↑	0.0221	0.0210	8.1856	1.3754
D to Z ↓	0.0163	0.0184	2.7512	0.5543

D to Z ↑	0.0279	0.0283	7.0293	1.1671
	X38_P16		**X38_P16**	
A to Z ↓	0.0209		0.9319	
A to Z ↑	0.0285		1.0247	
B to Z ↓	0.0200		0.9344	
B to Z ↑	0.0251		1.0313	
C to Z ↓	0.0183		0.9376	
C to Z ↑	0.0205		1.0399	
D to Z ↓	0.0193		0.4604	
D to Z ↑	0.0277		0.8791	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	3.972e-06	1.000e-20
X29_P16	2.172e-05	1.000e-20
X38_P16	2.806e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X29_P16	X38_P16
A (output stable)	1.916e-05	1.648e-04	2.075e-04
B (output stable)	2.780e-05	2.786e-04	3.543e-04
C (output stable)	5.350e-05	5.860e-04	7.492e-04
D (output stable)	9.027e-05	6.839e-04	8.853e-04
A to Z	1.419e-03	9.043e-03	1.150e-02
B to Z	1.211e-03	7.272e-03	9.311e-03
C to Z	1.007e-03	5.500e-03	6.986e-03
D to Z	1.782e-03	1.094e-02	1.407e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

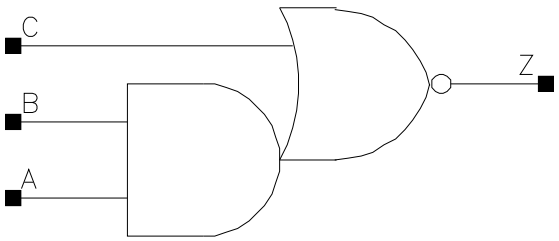
Pin Cycle (vdds)	X5_P16	X29_P16	X38_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X11_P16	1.200	1.088	1.3056
X16_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X6_P16	X11_P16	X16_P16	X23_P16
A	0.0009	0.0019	0.0027	0.0036
B	0.0009	0.0017	0.0025	0.0033
C	0.0009	0.0016	0.0023	0.0032
	X46_P16			
A	0.0069			
B	0.0065			
C	0.0063			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X11_P16	X6_P16	X11_P16
A to Z ↓	0.0160	0.0174	4.7727	2.4004
A to Z ↑	0.0264	0.0278	8.2375	4.0248
B to Z ↓	0.0170	0.0171	4.7982	2.4151

B to Z ↑	0.0230	0.0235	8.1752	4.0344
C to Z ↓	0.0100	0.0105	2.7700	1.6365
C to Z ↑	0.0184	0.0179	7.6054	3.7307
	X16_P16	**X23_P16**	**X16_P16**	**X23_P16**
A to Z ↓	0.0166	0.0170	1.6533	1.2407
A to Z ↑	0.0261	0.0265	2.7010	2.0397
B to Z ↓	0.0169	0.0167	1.6650	1.2486
B to Z ↑	0.0217	0.0220	2.7015	2.0458
C to Z ↓	0.0106	0.0093	1.1429	0.7046
C to Z ↑	0.0170	0.0175	2.5027	1.8930
	X46_P16		**X46_P16**	
A to Z ↓	0.0165		0.6344	
A to Z ↑	0.0254		1.0472	
B to Z ↓	0.0164		0.6390	
B to Z ↑	0.0209		1.0453	
C to Z ↓	0.0096		0.3605	
C to Z ↑	0.0175		0.9695	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P16	4.029e-06	1.000e-20
X11_P16	8.041e-06	1.000e-20
X16_P16	1.116e-05	1.000e-20
X23_P16	1.585e-05	1.000e-20
X46_P16	3.061e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	1.791e-05	5.202e-05	6.604e-05	9.515e-05
B (output stable)	2.500e-05	1.189e-04	1.220e-04	1.975e-04
C (output stable)	1.752e-04	3.999e-04	5.357e-04	7.299e-04
A to Z	1.409e-03	3.115e-03	4.246e-03	5.799e-03
B to Z	1.194e-03	2.493e-03	3.357e-03	4.518e-03
C to Z	7.367e-04	1.498e-03	2.041e-03	2.858e-03
	X46_P16			
A (output stable)	1.707e-04			
B (output stable)	3.395e-04			
C (output stable)	1.289e-03			
A to Z	1.069e-02			
B to Z	8.302e-03			
C to Z	5.396e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X6_P16	X11_P16	X16_P16	X23_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

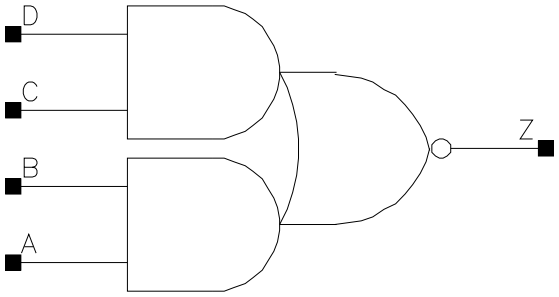
	X46_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X4_P16	X10_P16	X16_P16	X21_P16
A	0.0007	0.0019	0.0027	0.0035
B	0.0007	0.0016	0.0025	0.0033
C	0.0007	0.0018	0.0025	0.0033
D	0.0007	0.0015	0.0023	0.0030
	X42_P16			
A	0.0070			
B	0.0065			
C	0.0065			
D	0.0061			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X10_P16**	**X4_P16**	**X10_P16**
A to Z ↓	0.0180	0.0178	5.9716	2.3331
A to Z ↑	0.0346	0.0289	11.4087	3.7011
B to Z ↓	0.0193	0.0191	6.0016	2.3469
B to Z ↑	0.0309	0.0261	11.3969	3.7682
C to Z ↓	0.0136	0.0129	6.0569	2.3403
C to Z ↑	0.0264	0.0227	11.4415	3.7286
D to Z ↓	0.0141	0.0134	6.1086	2.3603
D to Z ↑	0.0224	0.0192	11.4266	3.7701
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0194	0.0194	1.6615	1.2446
A to Z ↑	0.0302	0.0302	2.4900	1.9084
B to Z ↓	0.0201	0.0196	1.6706	1.2517
B to Z ↑	0.0264	0.0261	2.4908	1.9109
C to Z ↓	0.0142	0.0146	1.6586	1.2438
C to Z ↑	0.0235	0.0242	2.4977	1.9136
D to Z ↓	0.0139	0.0136	1.6728	1.2550
D to Z ↑	0.0192	0.0194	2.5020	1.9175
	X42_P16		**X42_P16**	
A to Z ↓	0.0201		0.6417	
A to Z ↑	0.0304		0.9557	
B to Z ↓	0.0201		0.6454	
B to Z ↑	0.0262		0.9533	
C to Z ↓	0.0150		0.6368	
C to Z ↑	0.0242		0.9592	
D to Z ↓	0.0143		0.6427	
D to Z ↑	0.0197		0.9579	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	3.286e-06	1.000e-20
X10_P16	1.001e-05	1.000e-20
X16_P16	1.401e-05	1.000e-20
X21_P16	1.890e-05	1.000e-20
X42_P16	3.685e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	1.979e-05	4.661e-05	9.363e-05	1.282e-04
B (output stable)	2.826e-05	6.931e-05	2.081e-04	3.313e-04
C (output stable)	3.241e-05	9.033e-05	1.566e-04	2.141e-04
D (output stable)	4.195e-05	1.156e-04	2.740e-04	4.142e-04
A to Z	1.443e-03	3.507e-03	5.561e-03	7.297e-03
B to Z	1.260e-03	3.056e-03	4.663e-03	6.078e-03
C to Z	8.322e-04	2.072e-03	3.316e-03	4.537e-03
D to Z	6.719e-04	1.667e-03	2.478e-03	3.318e-03
	X42_P16			
A (output stable)	2.454e-04			
B (output stable)	5.619e-04			
C (output stable)	4.138e-04			
D (output stable)	7.465e-04			

A to Z	1.436e-02			
B to Z	1.202e-02			
C to Z	8.844e-03			
D to Z	6.605e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

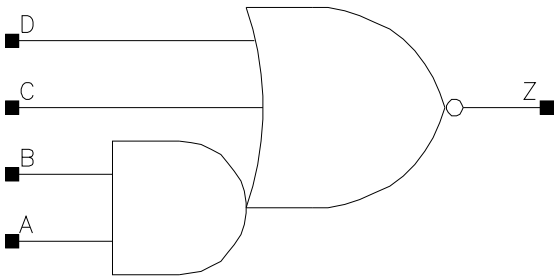
Pin Cycle (vdds)	X4_P16	X10_P16	X16_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X35_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X5_P16	X35_P16
A	0.0008	0.0063
B	0.0008	0.0058
C	0.0009	0.0061
D	0.0009	0.0058

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X35_P16	X5_P16	X35_P16
A to Z ↓	0.0155	0.0161	4.9448	0.7191
A to Z ↑	0.0300	0.0279	11.9940	1.5131
B to Z ↓	0.0161	0.0159	4.9802	0.7252
B to Z ↑	0.0249	0.0221	11.9422	1.5133
C to Z ↓	0.0164	0.0209	2.8552	0.5507
C to Z ↑	0.0356	0.0348	11.3183	1.4283
D to Z ↓	0.0159	0.0194	2.8748	0.5492

D to Z ↑	0.0343	0.0319	11.3246	1.4307

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	3.368e-06	1.000e-20
X35_P16	2.369e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X35_P16
A (output stable)	3.151e-05	2.874e-04
B (output stable)	3.414e-05	3.537e-04
C (output stable)	4.041e-05	4.631e-04
D (output stable)	3.813e-05	4.073e-04
A to Z	1.148e-03	8.302e-03
B to Z	9.456e-04	6.261e-03
C to Z	1.855e-03	1.445e-02
D to Z	1.576e-03	1.143e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

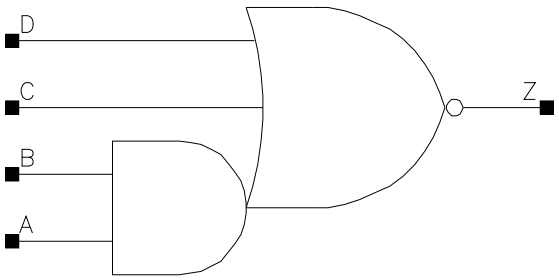
Pin Cycle (vdds)	X5_P16	X35_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.680	0.8160
X17_P16	1.200	2.448	2.9376
X34_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X4_P16	X17_P16	X34_P16
A	0.0009	0.0035	0.0071
B	0.0009	0.0033	0.0066
C	0.0008	0.0030	0.0058
D	0.0007	0.0027	0.0053

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X17_P16	X4_P16	X17_P16
A to Z ↓	0.0187	0.0204	5.4044	1.4122
A to Z ↑	0.0356	0.0375	12.0360	2.9571
B to Z ↓	0.0202	0.0206	5.4312	1.4199
B to Z ↑	0.0313	0.0319	11.9654	2.9616
C to Z ↓	0.0171	0.0170	4.6317	1.1331
C to Z ↑	0.0255	0.0274	11.3754	2.8024

D to Z ↓	0.0144	0.0130	4.7497	1.1378
D to Z ↑	0.0223	0.0204	11.4094	2.8123
	X34_P16		**X34_P16**	
A to Z ↓	0.0201		0.7207	
A to Z ↑	0.0368		1.4985	
B to Z ↓	0.0206		0.7247	
B to Z ↑	0.0313		1.4955	
C to Z ↓	0.0173		0.5973	
C to Z ↑	0.0265		1.4182	
D to Z ↓	0.0134		0.6019	
D to Z ↑	0.0200		1.4234	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	3.004e-06	1.000e-20
X17_P16	1.195e-05	1.000e-20
X34_P16	2.333e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X17_P16	X34_P16
A (output stable)	1.773e-05	8.637e-05	1.740e-04
B (output stable)	1.995e-05	1.355e-04	2.513e-04
C (output stable)	4.074e-05	2.215e-04	4.222e-04
D (output stable)	7.223e-05	4.391e-04	8.332e-04
A to Z	1.742e-03	7.627e-03	1.473e-02
B to Z	1.543e-03	6.404e-03	1.241e-02
C to Z	1.052e-03	4.654e-03	8.835e-03
D to Z	7.521e-04	2.843e-03	5.407e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

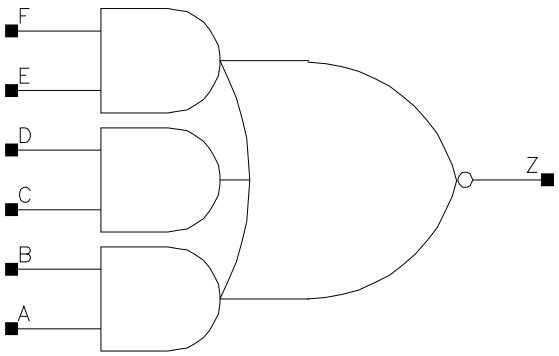
Pin Cycle (vdds)	X4_P16	X17_P16	X34_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.088	1.3056
X8_P16	1.200	2.176	2.6112
X13_P16	1.200	2.720	3.2640
X17_P16	1.200	3.672	4.4064

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X4_P16	X8_P16	X13_P16	X17_P16
A	0.0009	0.0018	0.0027	0.0035

B	0.0009	0.0016	0.0025	0.0032
C	0.0009	0.0017	0.0025	0.0032
D	0.0008	0.0016	0.0023	0.0030
E	0.0010	0.0016	0.0024	0.0031
F	0.0008	0.0015	0.0022	0.0029

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0219	0.0264	4.7857	2.7536
A to Z ↑	0.0514	0.0501	11.5608	5.3131
B to Z ↓	0.0238	0.0271	4.8043	2.7620
B to Z ↑	0.0470	0.0453	11.5624	5.3236
C to Z ↓	0.0200	0.0238	4.7386	2.7530
C to Z ↑	0.0444	0.0446	11.6085	5.3294
D to Z ↓	0.0215	0.0246	4.7666	2.7657
D to Z ↑	0.0400	0.0396	11.5751	5.3296
E to Z ↓	0.0151	0.0181	4.6493	2.7522
E to Z ↑	0.0332	0.0332	11.5551	5.3156
F to Z ↓	0.0159	0.0179	4.6911	2.7744
F to Z ↑	0.0287	0.0279	11.6189	5.3218
	X13_P16	**X17_P16**	**X13_P16**	**X17_P16**
A to Z ↓	0.0253	0.0254	1.8675	1.4199
A to Z ↑	0.0467	0.0468	3.5175	2.6782
B to Z ↓	0.0265	0.0261	1.8729	1.4245
B to Z ↑	0.0424	0.0417	3.5278	2.6799
C to Z ↓	0.0228	0.0228	1.8790	1.4060
C to Z ↑	0.0410	0.0412	3.5322	2.6916
D to Z ↓	0.0240	0.0232	1.8873	1.4128
D to Z ↑	0.0366	0.0363	3.5370	2.6886
E to Z ↓	0.0172	0.0171	1.8733	1.4069
E to Z ↑	0.0308	0.0309	3.5286	2.6808
F to Z ↓	0.0175	0.0166	1.8868	1.4180
F to Z ↑	0.0262	0.0258	3.5348	2.6896

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	5.525e-06	1.000e-20
X8_P16	1.118e-05	1.000e-20
X13_P16	1.565e-05	1.000e-20
X17_P16	2.093e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

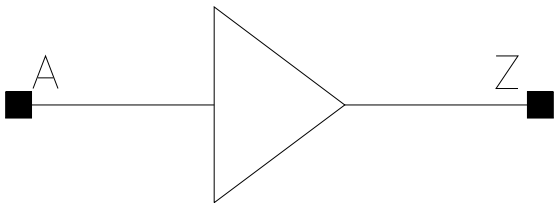
Pin Cycle (vdd)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	3.290e-05	7.791e-05	1.096e-04	1.473e-04
B (output stable)	3.835e-05	1.573e-04	1.716e-04	2.794e-04
C (output stable)	3.563e-05	8.394e-05	1.161e-04	1.615e-04
D (output stable)	4.285e-05	1.698e-04	1.814e-04	2.927e-04
E (output stable)	5.667e-05	1.399e-04	1.982e-04	2.698e-04
F (output stable)	6.661e-05	2.189e-04	2.669e-04	4.007e-04

A to Z	2.784e-03	5.879e-03	8.147e-03	1.078e-02
B to Z	2.552e-03	5.288e-03	7.359e-03	9.567e-03
C to Z	2.079e-03	4.589e-03	6.166e-03	8.206e-03
D to Z	1.870e-03	4.028e-03	5.437e-03	7.105e-03
E to Z	1.330e-03	3.042e-03	4.021e-03	5.352e-03
F to Z	1.132e-03	2.467e-03	3.294e-03	4.253e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X4_P16	X8_P16	X13_P16	X17_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description	Logical Symbol
Buffer	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.408	0.4896
X6_P16	1.200	0.408	0.4896
X8_P16	1.200	0.408	0.4896
X13_P16	1.200	0.544	0.6528
X16_P16	1.200	0.544	0.6528
X21_P16	1.200	0.680	0.8160
X25_P16	1.200	0.680	0.8160
X29_P16	1.200	0.952	1.1424
X33_P16	1.200	0.952	1.1424
X42_P16	1.200	1.088	1.3056
X50_P16	1.200	1.224	1.4688
X58_P16	1.200	1.496	1.7952
X67_P16	1.200	1.632	1.9584
X75_P16	1.200	1.768	2.1216
X84_P16	1.200	1.904	2.2848
X100_P16	1.200	2.312	2.7744
X134_P16	1.200	2.992	3.5904

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0008	0.0008	0.0008	0.0008
	X16_P16	X21_P16	X25_P16	X29_P16
A	0.0008	0.0012	0.0012	0.0016
	X33_P16	X42_P16	X50_P16	X58_P16
A	0.0016	0.0018	0.0022	0.0032

	X67_P16	X75_P16	X84_P16	X100_P16
A	0.0032	0.0032	0.0032	0.0042
	X134_P16			
A	0.0052			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0330	0.0333	5.0152	3.6001
A to Z ↑	0.0265	0.0262	8.6179	6.2725
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0349	0.0396	2.6414	1.7240
A to Z ↑	0.0272	0.0305	4.4492	2.9213
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0431	0.0354	1.3605	1.0543
A to Z ↑	0.0324	0.0281	2.2289	1.7483
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0370	0.0355	0.8982	0.7632
A to Z ↑	0.0289	0.0268	1.4580	1.2499
	X33_P16	**X42_P16**	**X33_P16**	**X42_P16**
A to Z ↓	0.0370	0.0359	0.6749	0.5462
A to Z ↑	0.0277	0.0280	1.0927	0.8770
	X50_P16	**X58_P16**	**X50_P16**	**X58_P16**
A to Z ↓	0.0352	0.0325	0.4547	0.3911
A to Z ↑	0.0276	0.0260	0.7294	0.6264
	X67_P16	**X75_P16**	**X67_P16**	**X75_P16**
A to Z ↓	0.0341	0.0360	0.3437	0.3097
A to Z ↑	0.0270	0.0284	0.5490	0.4902
	X84_P16	**X100_P16**	**X84_P16**	**X100_P16**
A to Z ↓	0.0378	0.0352	0.2805	0.2352
A to Z ↑	0.0296	0.0278	0.4428	0.3705
	X134_P16		**X134_P16**	
A to Z ↓	0.0370		0.1821	
A to Z ↑	0.0294		0.2824	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	2.829e-06	1.000e-20
X6_P16	3.578e-06	1.000e-20
X8_P16	4.627e-06	1.000e-20
X13_P16	5.842e-06	1.000e-20
X16_P16	7.539e-06	1.000e-20
X21_P16	1.037e-05	1.000e-20
X25_P16	1.199e-05	1.000e-20
X29_P16	1.343e-05	1.000e-20
X33_P16	1.500e-05	1.000e-20
X42_P16	1.886e-05	1.000e-20
X50_P16	2.287e-05	1.000e-20
X58_P16	2.831e-05	1.000e-20
X67_P16	3.103e-05	1.000e-20
X75_P16	3.376e-05	1.000e-20

X84_P16	3.648e-05	1.000e-20
X100_P16	4.464e-05	1.000e-20
X134_P16	5.826e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	1.374e-03	1.546e-03	1.851e-03	2.474e-03
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	3.013e-03	4.035e-03	4.535e-03	5.093e-03
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	5.615e-03	7.047e-03	8.330e-03	1.014e-02
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	1.129e-02	1.266e-02	1.396e-02	1.642e-02
	X134_P16			
A to Z	2.250e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

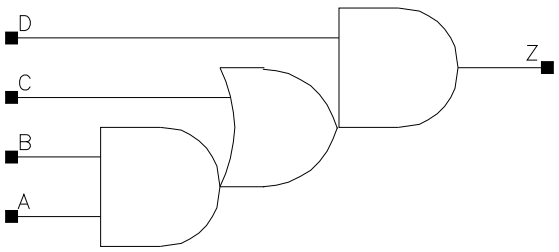
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P16	X21_P16	X25_P16	X29_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P16	X42_P16	X50_P16	X58_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X67_P16	X75_P16	X84_P16	X100_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X134_P16			
A to Z	0.000e+00			

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.632	1.9584
X25_P16	1.200	1.768	2.1216
X33_P16	1.200	1.904	2.2848

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0010	0.0022	0.0021	0.0021
B	0.0010	0.0019	0.0019	0.0018
C	0.0011	0.0024	0.0023	0.0023
D	0.0016	0.0021	0.0021	0.0021

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0459	0.0433	2.7003	1.3369
A to Z ↑	0.0423	0.0397	4.5123	2.1954
B to Z ↓	0.0423	0.0390	2.6917	1.3354
B to Z ↑	0.0424	0.0388	4.5150	2.1928
C to Z ↓	0.0380	0.0347	2.6864	1.3328
C to Z ↑	0.0311	0.0280	4.4713	2.1724

D to Z ↓	0.0375	0.0327	2.6634	1.3221
D to Z ↑	0.0368	0.0318	4.4739	2.1757
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0477	0.0509	0.9094	0.6878
A to Z ↑	0.0438	0.0464	1.4810	1.1149
B to Z ↓	0.0436	0.0476	0.9083	0.6861
B to Z ↑	0.0430	0.0464	1.4805	1.1129
C to Z ↓	0.0393	0.0431	0.9057	0.6841
C to Z ↑	0.0314	0.0340	1.4639	1.1002
D to Z ↓	0.0357	0.0379	0.8958	0.6738
D to Z ↑	0.0349	0.0371	1.4673	1.1024

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	7.386e-06	1.000e-20
X17_P16	1.432e-05	1.000e-20
X25_P16	1.722e-05	1.000e-20
X33_P16	2.012e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	6.798e-05	1.411e-04	1.428e-04	1.261e-04
B (output stable)	8.877e-05	1.901e-04	1.920e-04	1.625e-04
C (output stable)	2.602e-04	4.345e-04	4.382e-04	4.194e-04
D (output stable)	8.119e-05	1.158e-04	1.169e-04	1.156e-04
A to Z	3.143e-03	5.753e-03	7.222e-03	8.481e-03
B to Z	2.909e-03	5.153e-03	6.614e-03	7.974e-03
C to Z	2.420e-03	4.162e-03	5.569e-03	6.840e-03
D to Z	3.211e-03	5.520e-03	6.897e-03	8.070e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

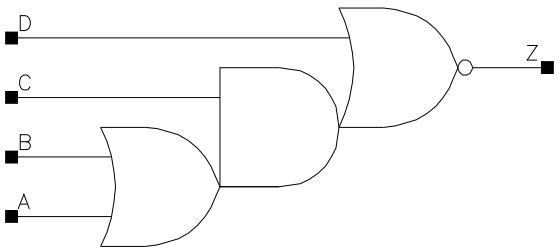
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.952	1.1424
X11_P16	1.200	1.496	1.7952
X16_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X16_P16	X21_P16
A	0.0010	0.0018	0.0027	0.0035
B	0.0009	0.0017	0.0027	0.0034
C	0.0009	0.0017	0.0025	0.0034
D	0.0011	0.0017	0.0024	0.0032

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0199	0.0189	4.6522	2.4320
A to Z ↑	0.0431	0.0397	11.7687	6.0749
B to Z ↓	0.0191	0.0184	4.5675	2.4031
B to Z ↑	0.0402	0.0376	11.7804	6.0792
C to Z ↓	0.0178	0.0169	4.2804	2.2426
C to Z ↑	0.0261	0.0240	8.0723	4.1177

D to Z ↓	0.0112	0.0096	2.6492	1.3428
D to Z ↑	0.0225	0.0194	8.6001	4.3969
	X16_P16	**X21_P16**	**X16_P16**	**X21_P16**
A to Z ↓	0.0188	0.0191	1.6532	1.2611
A to Z ↑	0.0369	0.0390	3.9368	3.0156
B to Z ↓	0.0179	0.0183	1.6568	1.2608
B to Z ↑	0.0360	0.0367	3.9392	3.0183
C to Z ↓	0.0170	0.0170	1.5422	1.1718
C to Z ↑	0.0232	0.0234	2.7292	2.0464
D to Z ↓	0.0095	0.0095	0.9365	0.7128
D to Z ↑	0.0181	0.0181	2.8958	2.1851

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	4.587e-06	1.000e-20
X11_P16	8.682e-06	1.000e-20
X16_P16	1.197e-05	1.000e-20
X21_P16	1.602e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	2.121e-05	3.787e-05	4.886e-05	8.212e-05
B (output stable)	1.158e-05	2.214e-05	2.676e-05	4.360e-05
C (output stable)	6.832e-05	1.405e-04	1.893e-04	2.680e-04
D (output stable)	1.765e-04	3.620e-04	5.259e-04	7.239e-04
A to Z	2.253e-03	3.946e-03	5.501e-03	7.738e-03
B to Z	1.833e-03	3.247e-03	4.669e-03	6.314e-03
C to Z	1.527e-03	2.639e-03	3.760e-03	5.145e-03
D to Z	9.134e-04	1.539e-03	2.079e-03	2.774e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

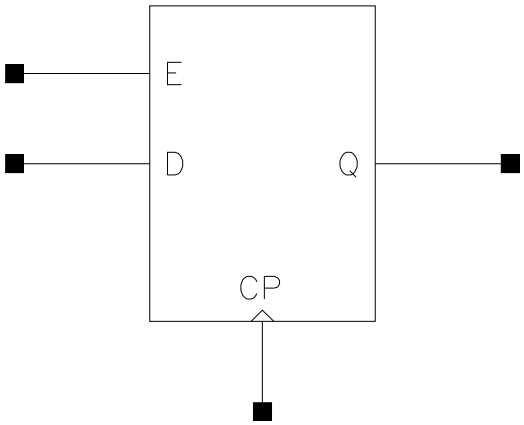
Pin Cycle (vdds)	X5_P16	X11_P16	X16_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPHQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.128	3.7536
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	Q
IQ	IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0012	0.0012	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0553	0.0640	2.6853	1.3892
CP to Q ↑	0.0690	0.0738	4.4862	2.2497
	X33_P16		**X33_P16**	
CP to Q ↓	0.0976		0.6838	
CP to Q ↑	0.1203		1.1110	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0759	0.0759	0.0759
CP ↑	min_pulse_width to CP	0.0454	0.0547	0.0393
D ↓	hold_rising to CP	-0.0289	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0137	-0.0110	-0.0169
D ↓	setup_rising to CP	0.0782	0.0782	0.0782
D ↑	setup_rising to CP	0.0433	0.0465	0.0437
E ↓	hold_rising to CP	-0.0214	-0.0214	-0.0214
E ↑	hold_rising to CP	-0.0142	-0.0142	-0.0142
E ↓	setup_rising to CP	0.0803	0.0803	0.0803
E ↑	setup_rising to CP	0.0857	0.0857	0.0857

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	1.753e-05	1.000e-20
X17_P16	2.042e-05	1.000e-20
X33_P16	2.952e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

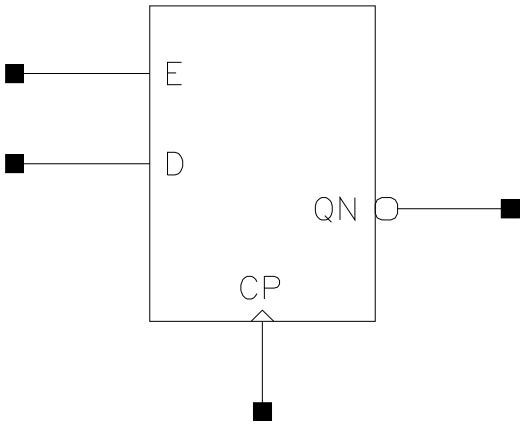
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	6.545e-03	6.547e-03	6.556e-03
Clock 100Mhz Data 25Mhz	8.660e-03	9.315e-03	1.158e-02
Clock 100Mhz Data 50Mhz	1.078e-02	1.208e-02	1.661e-02
Clock = 0 Data 100Mhz	4.237e-03	4.237e-03	4.237e-03
Clock = 1 Data 100Mhz	1.139e-03	1.139e-03	1.140e-03

DFPHQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.992	3.5904
X17_P16	1.200	3.264	3.9168
X33_P16	1.200	3.672	4.4064

Truth Table

IQ	QN
IQ	!IQ

CP	E	D	IQ	IQ
/	0	-	IQ	IQ
/	1	D	-	D
-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0009	0.0009	0.0009
D	0.0007	0.0007	0.0007
E	0.0010	0.0010	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.0991	0.0925	2.7597	1.3219
CP to QN ↑	0.0743	0.0764	4.5468	2.1893
	X33_P16		**X33_P16**	
CP to QN ↓	0.0993		0.6857	
CP to QN ↑	0.0846		1.1142	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0759	0.0759	0.0759
CP ↑	min_pulse_width to CP	0.0393	0.0406	0.0486
D ↓	hold_rising to CP	-0.0289	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0169	-0.0137	-0.0110
D ↓	setup_rising to CP	0.0782	0.0782	0.0782
D ↑	setup_rising to CP	0.0465	0.0465	0.0465
E ↓	hold_rising to CP	-0.0214	-0.0214	-0.0214
E ↑	hold_rising to CP	-0.0142	-0.0142	-0.0142
E ↓	setup_rising to CP	0.0803	0.0803	0.0803
E ↑	setup_rising to CP	0.0857	0.0857	0.0857

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	1.736e-05	1.000e-20
X17_P16	2.219e-05	1.000e-20
X33_P16	2.880e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

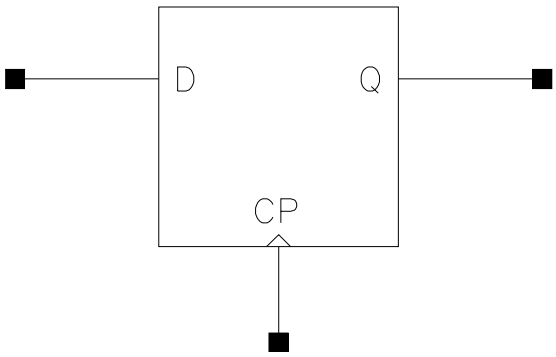
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	6.539e-03	6.542e-03	6.545e-03
Clock 100Mhz Data 25Mhz	8.701e-03	9.720e-03	1.145e-02
Clock 100Mhz Data 50Mhz	1.086e-02	1.290e-02	1.636e-02
Clock = 0 Data 100Mhz	4.237e-03	4.236e-03	4.237e-03
Clock = 1 Data 100Mhz	1.139e-03	1.139e-03	1.139e-03

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.176	2.6112
X17_P16	1.200	2.448	2.9376
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.720	3.2640

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0578	0.0639	2.6758	1.3775
CP to Q ↑	0.0702	0.0781	4.3803	2.2231
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to Q ↓	0.0815	0.0848	0.8196	0.7425
CP to Q ↑	0.0886	0.0905	1.2524	1.1361

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0711	0.0711	0.0711	0.0711
CP ↑	min_pulse_width to CP	0.0439	0.0500	0.0689	0.0737
D ↓	hold_rising to CP	0.0075	0.0053	0.0079	0.0079
D ↑	hold_rising to CP	0.0049	0.0049	0.0049	0.0049
D ↓	setup_rising to CP	0.0391	0.0440	0.0445	0.0440
D ↑	setup_rising to CP	0.0222	0.0222	0.0222	0.0222

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	1.388e-05	1.000e-20
X17_P16	1.702e-05	1.000e-20
X30_P16	2.135e-05	1.000e-20
X33_P16	2.253e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

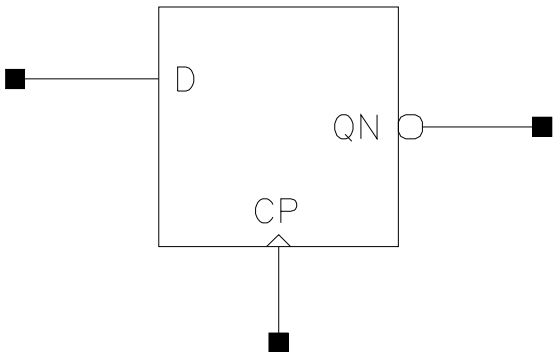
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	6.896e-03	6.940e-03	6.956e-03	6.964e-03
Clock 100Mhz Data 25Mhz	7.947e-03	8.903e-03	1.041e-02	1.077e-02
Clock 100Mhz Data 50Mhz	8.999e-03	1.087e-02	1.386e-02	1.457e-02
Clock = 0 Data 100Mhz	2.840e-03	2.932e-03	2.960e-03	2.974e-03
Clock = 1 Data 100Mhz	1.606e-05	1.609e-05	1.615e-05	1.618e-05

DFPQN

Cell Description

Positive edge triggered Non-scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X30_P16	1.200	2.720	3.2640
X33_P16	1.200	2.856	3.4272

Truth Table

IQ	QN
IQ	!IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X30_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0008	0.0008	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.0562	0.0669	2.7424	1.4204
CP to QN ↑	0.0604	0.0643	4.3661	2.2172
	X30_P16	**X33_P16**	**X30_P16**	**X33_P16**

CP to QN ↓	0.0998	0.1000	0.7575	0.6839
CP to QN ↑	0.0784	0.0908	1.2108	1.1136

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P16	X17_P16	X30_P16	X33_P16
CP ↓	min_pulse_width to CP	0.0567	0.0602	0.0711	0.0711
CP ↑	min_pulse_width to CP	0.0405	0.0500	0.0439	0.0534
D ↓	hold_rising to CP	0.0123	0.0172	0.0053	0.0075
D ↑	hold_rising to CP	0.0102	0.0097	0.0049	0.0049
D ↓	setup_rising to CP	0.0245	0.0277	0.0440	0.0424
D ↑	setup_rising to CP	0.0271	0.0271	0.0222	0.0222

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	1.294e-05	1.000e-20
X17_P16	1.587e-05	1.000e-20
X30_P16	2.364e-05	1.000e-20
X33_P16	2.519e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

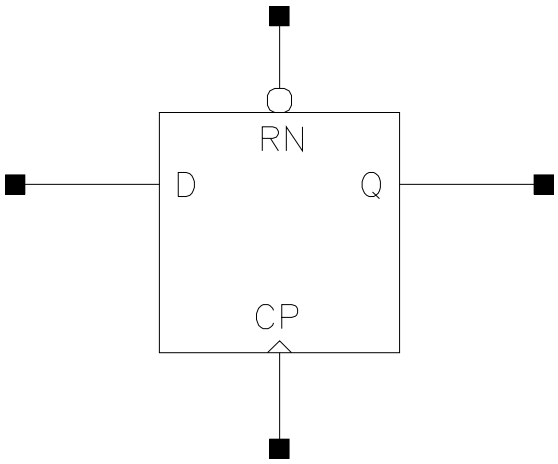
Pin Cycle	X8_P16	X17_P16	X30_P16	X33_P16
Clock 100Mhz Data 0Mhz	6.659e-03	6.662e-03	6.764e-03	6.806e-03
Clock 100Mhz Data 25Mhz	7.582e-03	8.299e-03	1.022e-02	1.070e-02
Clock 100Mhz Data 50Mhz	8.504e-03	9.936e-03	1.368e-02	1.460e-02
Clock = 0 Data 100Mhz	2.475e-03	2.475e-03	2.657e-03	2.703e-03
Clock = 1 Data 100Mhz	1.582e-05	1.589e-05	1.602e-05	1.611e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0008	0.0008
RN	0.0010	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0666	0.0841	1.3898	0.8308
CP to Q ↑	0.0806	0.0908	2.2280	1.2571
RN to Q ↓	0.1141	0.1544	1.4781	0.8856

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0758	0.0758
CP ↑	min_pulse_width to CP	0.0546	0.0689
D ↓	hold_rising to CP	0.0053	0.0053
D ↑	hold_rising to CP	0.0053	0.0053
D ↓	setup_rising to CP	0.0472	0.0472
D ↑	setup_rising to CP	0.0271	0.0271
RN ↓	min_pulse_width to RN	0.1365	0.1755
RN ↑	recovery_rising to CP	0.0248	0.0276
RN ↑	removal_rising to CP	-0.0077	-0.0077

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P16	1.862e-05	1.000e-20
X30_P16	2.311e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

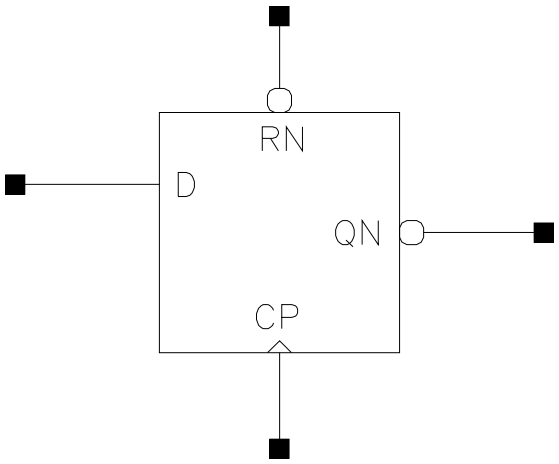
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	7.392e-03	7.390e-03
Clock 100Mhz Data 25Mhz	9.492e-03	1.097e-02
Clock 100Mhz Data 50Mhz	1.159e-02	1.455e-02
Clock = 0 Data 100Mhz	3.472e-03	3.474e-03
Clock = 1 Data 100Mhz	1.616e-05	1.631e-05

DFPRQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0008	0.0008
RN	0.0010	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.0953	0.1033	1.3107	0.7583
CP to QN ↑	0.0760	0.0819	2.1765	1.2140
RN to QN ↑	0.1162	0.1238	2.1849	1.2176

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0758	0.0758
CP ↑	min_pulse_width to CP	0.0438	0.0453
D ↓	hold_rising to CP	0.0053	0.0053
D ↑	hold_rising to CP	0.0027	0.0027
D ↓	setup_rising to CP	0.0472	0.0472
D ↑	setup_rising to CP	0.0271	0.0271
RN ↓	min_pulse_width to RN	0.1067	0.1143
RN ↑	recovery_rising to CP	0.0248	0.0222
RN ↑	removal_rising to CP	-0.0077	-0.0077

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P16	2.099e-05	1.000e-20
X30_P16	2.509e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

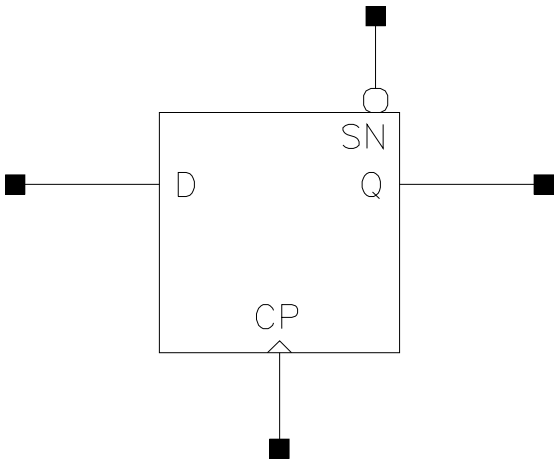
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	7.388e-03	7.387e-03
Clock 100Mhz Data 25Mhz	9.864e-03	1.100e-02
Clock 100Mhz Data 50Mhz	1.234e-02	1.461e-02
Clock = 0 Data 100Mhz	3.517e-03	3.503e-03
Clock = 1 Data 100Mhz	1.609e-05	1.620e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0008	0.0008
SN	0.0013	0.0013

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to Q ↓	0.0667	0.0850	1.3918	0.8282
CP to Q ↑	0.0799	0.0906	2.2287	1.2567
SN to Q ↑	0.0789	0.0927	2.2355	1.2598

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0818	0.0819
CP ↑	min_pulse_width to CP	0.0546	0.0688
D ↓	hold_rising to CP	0.0053	0.0053
D ↑	hold_rising to CP	0.0053	0.0049
D ↓	setup_rising to CP	0.0521	0.0521
D ↑	setup_rising to CP	0.0249	0.0249
SN ↓	min_pulse_width to SN	0.0745	0.0918
SN ↑	recovery_rising to CP	0.0129	0.0129
SN ↑	removal_rising to CP	0.0384	0.0384

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P16	1.843e-05	1.000e-20
X30_P16	2.254e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

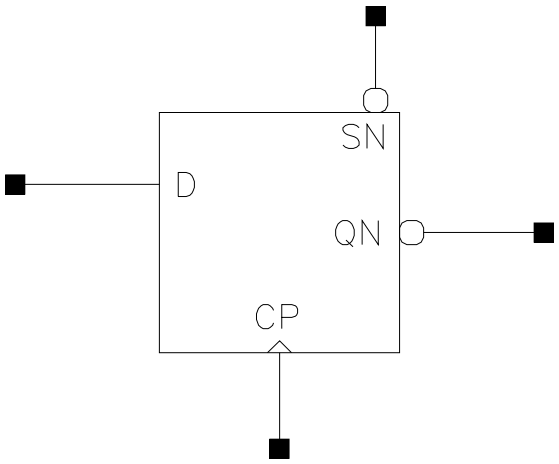
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	7.456e-03	7.445e-03
Clock 100Mhz Data 25Mhz	9.551e-03	1.103e-02
Clock 100Mhz Data 50Mhz	1.165e-02	1.462e-02
Clock = 0 Data 100Mhz	3.443e-03	3.442e-03
Clock = 1 Data 100Mhz	1.631e-05	1.637e-05

DFPSQN

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	3.128	3.7536
X30_P16	1.200	3.400	4.0800

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X17_P16	X30_P16
CP	0.0010	0.0010
D	0.0008	0.0008
SN	0.0012	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P16	X30_P16	X17_P16	X30_P16
CP to QN ↓	0.0946	0.1027	1.3133	0.7607
CP to QN ↑	0.0764	0.0824	2.1743	1.2122
SN to QN ↓	0.0925	0.1009	1.3132	0.7597

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P16	X30_P16
CP ↓	min_pulse_width to CP	0.0818	0.0818
CP ↑	min_pulse_width to CP	0.0438	0.0452
D ↓	hold_rising to CP	0.0053	0.0053
D ↑	hold_rising to CP	0.0053	0.0053
D ↓	setup_rising to CP	0.0521	0.0521
D ↑	setup_rising to CP	0.0249	0.0249
SN ↓	min_pulse_width to SN	0.0642	0.0669
SN ↑	recovery_rising to CP	0.0102	0.0129
SN ↑	removal_rising to CP	0.0384	0.0384

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P16	2.071e-05	1.000e-20
X30_P16	2.515e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

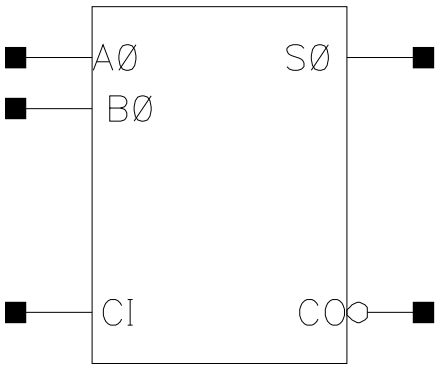
Pin Cycle	X17_P16	X30_P16
Clock 100Mhz Data 0Mhz	7.452e-03	7.451e-03
Clock 100Mhz Data 25Mhz	9.901e-03	1.104e-02
Clock 100Mhz Data 50Mhz	1.235e-02	1.463e-02
Clock = 0 Data 100Mhz	3.443e-03	3.444e-03
Clock = 1 Data 100Mhz	1.629e-05	1.638e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_FA1X8_P16	1.200	2.176	2.6112
C12T28SOI_LL_FA1X33_P16	1.200	4.896	5.8752
C12T28SOI_LLS1_FA1X8_P16	1.200	3.672	4.4064
C12T28SOI_LLS1_FA1X33_P16	1.200	8.024	9.6288

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C12T28SOI_LL_FA1X8_P16	C12T28SOI_LL_FA1X33_P16	C12T28SOI_LLS1_FA1X8_P16	C12T28SOI_LLS1_FA1X33_P16
A0	0.0035	0.0070	0.0031	0.0060
B0	0.0032	0.0067	0.0033	0.0058
CI	0.0024	0.0052	0.0023	0.0041

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16
A0 to CO ↓	0.0616	0.0669	2.7878	0.7330
A0 to CO ↑	0.0457	0.0470	4.5171	1.1542
A0 to S0 ↓	0.0647	0.0812	2.7567	0.7174
A0 to S0 ↑	0.0664	0.0809	4.4648	1.1366
B0 to CO ↓	0.0605	0.0672	2.7978	0.7376
B0 to CO ↑	0.0468	0.0488	4.5199	1.1516
B0 to S0 ↓	0.0649	0.0823	2.7579	0.7176
B0 to S0 ↑	0.0664	0.0818	4.4677	1.1371
CI to CO ↓	0.0577	0.0647	2.8010	0.7364
CI to CO ↑	0.0457	0.0468	4.5165	1.1541
CI to S0 ↓	0.0639	0.0811	2.7578	0.7174
CI to S0 ↑	0.0659	0.0816	4.4663	1.1368
	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16
A0 to CO ↓	0.0389	0.0484	5.5988	0.9694
A0 to CO ↑	0.0336	0.0389	4.5327	1.1406
A0 to S0 ↓	0.0853	0.1058	2.9507	0.7438
A0 to S0 ↑	0.0779	0.0843	4.6510	1.1498
B0 to CO ↓	0.0396	0.0496	5.5983	0.9704
B0 to CO ↑	0.0315	0.0374	4.5290	1.1402
B0 to S0 ↓	0.0858	0.1082	2.9493	0.7437
B0 to S0 ↑	0.0784	0.0866	4.6503	1.1505
CI to CO ↓	0.0394	0.0707	5.5914	0.9828
CI to CO ↑	0.0350	0.0423	4.6158	1.1487
CI to S0 ↓	0.0475	0.0628	2.9499	0.7439
CI to S0 ↑	0.0410	0.0410	4.6512	1.1506

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_FA1X8_P16	1.624e-05	1.000e-20
C12T28SOI_LL_FA1X33_P16	4.316e-05	1.000e-20
C12T28SOI_LLS1_FA1X8_P16	3.522e-05	1.000e-20
C12T28SOI_LLS1_FA1X33_P16	7.277e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16
A0 to CO	3.273e-03	9.352e-03	4.922e-03	1.237e-02
A0 to S0	3.297e-03	9.724e-03	6.610e-03	1.539e-02
B0 to CO	3.325e-03	9.552e-03	4.955e-03	1.254e-02
B0 to S0	3.239e-03	9.675e-03	6.719e-03	1.574e-02
CI to CO	3.339e-03	9.608e-03	3.485e-03	1.112e-02
CI to S0	3.218e-03	9.633e-03	3.957e-03	1.197e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_-FA1X8_P16	C12T28SOI_LL_-FA1X33_P16	C12T28SOI_LLS1_-FA1X8_P16	C12T28SOI_LLS1_-FA1X33_P16
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X33_P16	1.200	2.992	3.5904

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X8_P16	X33_P16
A0	0.0012	0.0035
B0	0.0011	0.0032

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
A0 to CO ↓	0.0462	0.0413	2.7549	0.6801
A0 to CO ↑	0.0426	0.0377	4.4945	1.1431
A0 to S0 ↓	0.0621	0.0574	2.6984	0.6796
A0 to S0 ↑	0.0576	0.0630	4.4349	1.1320
B0 to CO ↓	0.0449	0.0382	2.7549	0.6759
B0 to CO ↑	0.0449	0.0386	4.4945	1.1433
B0 to S0 ↓	0.0633	0.0562	2.6987	0.6801
B0 to S0 ↑	0.0570	0.0606	4.4347	1.1321

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	9.836e-06	1.000e-20
X33_P16	4.019e-05	1.000e-20

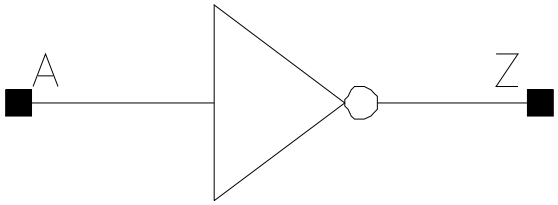
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X33_P16
A0 to CO	2.539e-03	8.315e-03
A0 to S0	2.330e-03	8.061e-03
B0 to CO	2.583e-03	8.476e-03
B0 to S0	2.288e-03	7.759e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X8_P16	X33_P16
A0 to CO	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.272	0.3264
X6_P16	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X13_P16	1.200	0.408	0.4896
X17_P16	1.200	0.408	0.4896
X21_P16	1.200	0.544	0.6528
X25_P16	1.200	0.544	0.6528
X29_P16	1.200	0.680	0.8160
X33_P16	1.200	0.680	0.8160
X50_P16	1.200	0.952	1.1424
X58_P16	1.200	1.088	1.3056
X67_P16	1.200	1.224	1.4688
X75_P16	1.200	1.360	1.6320
X84_P16	1.200	1.496	1.7952
X100_P16	1.200	1.768	2.1216
X134_P16	1.200	2.312	2.7744

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X13_P16
A	0.0006	0.0007	0.0009	0.0013
	X17_P16	X21_P16	X25_P16	X29_P16
A	0.0017	0.0022	0.0025	0.0030
	X33_P16	X50_P16	X58_P16	X67_P16
A	0.0033	0.0050	0.0058	0.0066
	X75_P16	X84_P16	X100_P16	X134_P16

A	0.0075	0.0085	0.0103	0.0142

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0101	0.0096	5.1467	3.9360
A to Z ↑	0.0159	0.0145	8.7291	6.5398
	X8_P16	**X13_P16**	**X8_P16**	**X13_P16**
A to Z ↓	0.0086	0.0075	2.6650	1.7379
A to Z ↑	0.0130	0.0119	4.4910	2.9652
	X17_P16	**X21_P16**	**X17_P16**	**X21_P16**
A to Z ↓	0.0073	0.0079	1.3204	1.0700
A to Z ↑	0.0111	0.0120	2.2008	1.7778
	X25_P16	**X29_P16**	**X25_P16**	**X29_P16**
A to Z ↓	0.0078	0.0074	0.9033	0.7707
A to Z ↑	0.0115	0.0111	1.4770	1.2666
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0074	0.0076	0.6804	0.4597
A to Z ↑	0.0108	0.0108	1.1063	0.7396
	X58_P16	**X67_P16**	**X58_P16**	**X67_P16**
A to Z ↓	0.0078	0.0078	0.3981	0.3494
A to Z ↑	0.0110	0.0109	0.6368	0.5577
	X75_P16	**X84_P16**	**X75_P16**	**X84_P16**
A to Z ↓	0.0082	0.0083	0.3143	0.2839
A to Z ↑	0.0113	0.0114	0.4988	0.4507
	X100_P16	**X134_P16**	**X100_P16**	**X134_P16**
A to Z ↓	0.0090	0.0098	0.2407	0.1861
A to Z ↑	0.0120	0.0127	0.3785	0.2891

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.487e-06	1.000e-20
X6_P16	2.048e-06	1.000e-20
X8_P16	3.199e-06	1.000e-20
X13_P16	4.559e-06	1.000e-20
X17_P16	6.394e-06	1.000e-20
X21_P16	7.460e-06	1.000e-20
X25_P16	9.181e-06	1.000e-20
X29_P16	1.030e-05	1.000e-20
X33_P16	1.190e-05	1.000e-20
X50_P16	1.734e-05	1.000e-20
X58_P16	2.006e-05	1.000e-20
X67_P16	2.278e-05	1.000e-20
X75_P16	2.550e-05	1.000e-20
X84_P16	2.823e-05	1.000e-20
X100_P16	3.367e-05	1.000e-20
X134_P16	4.456e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X13_P16

A to Z	3.761e-04	4.548e-04	5.770e-04	7.729e-04
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	9.755e-04	1.353e-03	1.550e-03	1.688e-03
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	1.876e-03	2.809e-03	3.388e-03	3.735e-03
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	4.290e-03	4.680e-03	5.692e-03	7.771e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

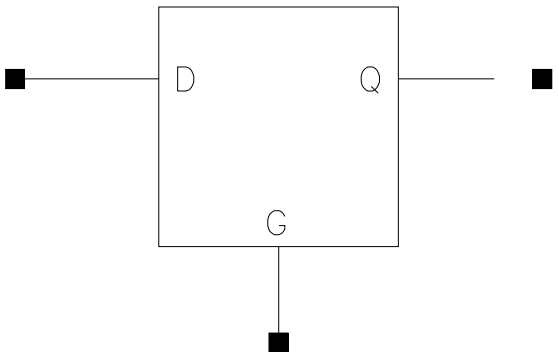
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X13_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P16	X21_P16	X25_P16	X29_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P16	X50_P16	X58_P16	X67_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X75_P16	X84_P16	X100_P16	X134_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X23_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X8_P16	X23_P16
D	0.0006	0.0014
G	0.0013	0.0021

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X23_P16	X8_P16	X23_P16
D to Q ↓	0.0704	0.0543	2.8087	1.3438
D to Q ↑	0.0452	0.0445	4.4225	1.1677
G to Q ↓	0.0760	0.0576	2.8057	1.3451
G to Q ↑	0.0433	0.0385	4.4215	1.1697

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P16	X23_P16
D ↓	hold_falling to G	-0.0240	-0.0088
D ↑	hold_falling to G	-0.0042	-0.0074
D ↓	setup_falling to G	0.0683	0.0431
D ↑	setup_falling to G	0.0502	0.0550
G ↑	min_pulse_width to G	0.0658	0.0565

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	7.664e-06	1.000e-20
X23_P16	1.744e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X23_P16
D (output stable)	1.094e-05	4.967e-05
G (output stable)	8.118e-04	1.606e-03
D to Q	3.996e-03	7.711e-03
G to Q	3.664e-03	6.766e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

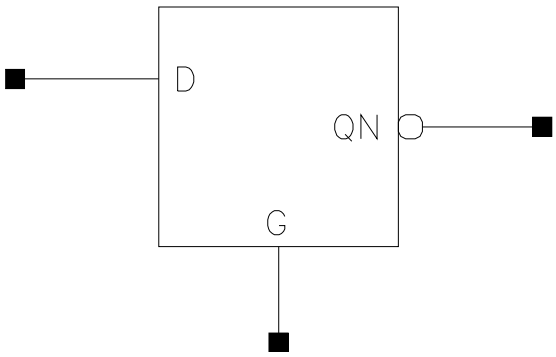
Pin Cycle (vdds)	X8_P16	X23_P16
D (output stable)	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P16	1.200	1.360	1.6320

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X17_P16
D	0.0006
G	0.0015

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X17_P16	X17_P16
D to QN ↓	0.0621	1.3166
D to QN ↑	0.0780	2.1686
G to QN ↓	0.0597	1.3171
G to QN ↑	0.0807	2.1688

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X17_P16
D ↓	hold_falling to G	-0.0289
D ↑	hold_falling to G	-0.0159
D ↓	setup_falling to G	0.0538
D ↑	setup_falling to G	0.0400
G ↑	min_pulse_width to G	0.0517

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X17_P16	1.210e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X17_P16
D (output stable)	1.131e-05
G (output stable)	9.048e-04
D to QN	5.019e-03
G to QN	4.571e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

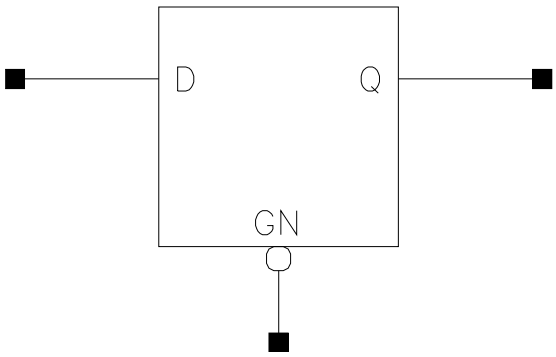
Pin Cycle (vdds)	X17_P16
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X33_P16	1.200	2.040	2.4480

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
D	0.0006	0.0008	0.0019
GN	0.0012	0.0016	0.0021

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D to Q ↓	0.0711	0.0603	2.8193	1.3837
D to Q ↑	0.0461	0.0429	4.4265	2.2633
GN to Q ↓	0.0632	0.0526	2.8199	1.3841
GN to Q ↑	0.0681	0.0640	4.4253	2.2621

	X33_P16		X33_P16	
D to Q ↓	0.0584		0.7053	
D to Q ↑	0.0366		1.1321	
GN to Q ↓	0.0493		0.7058	
GN to Q ↑	0.0490		1.1305	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P16	X17_P16	X33_P16
D ↓	hold_rising to GN	-0.0259	-0.0194	-0.0194
D ↑	hold_rising to GN	-0.0013	-0.0017	0.0036
D ↓	setup_rising to GN	0.0786	0.0663	0.0646
D ↑	setup_rising to GN	0.0416	0.0416	0.0314
GN ↓	min_pulse_width to GN	0.0818	0.0696	0.0638

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	7.427e-06	1.000e-20
X17_P16	1.210e-05	1.000e-20
X33_P16	2.076e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
D (output stable)	1.087e-05	1.835e-05	5.247e-05
GN (output stable)	8.088e-04	1.115e-03	1.388e-03
D to Q	4.014e-03	5.676e-03	9.238e-03
GN to Q	5.640e-03	7.724e-03	1.144e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

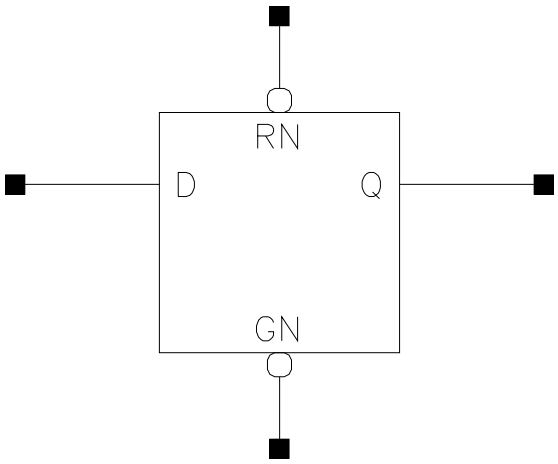
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.496	1.7952
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X8_P16	X33_P16
D	0.0006	0.0014
GN	0.0014	0.0026
RN	0.0006	0.0006

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X33_P16	X8_P16	X33_P16
D to Q ↓	0.0663	0.0587	2.7485	0.7086
D to Q ↑	0.0601	0.0772	4.5136	1.1685

GN to Q ↓	0.0593	0.0532	2.7476	0.7094
GN to Q ↑	0.0786	0.0809	4.5132	1.1685
RN to Q ↓	0.0529	0.1030	2.6538	0.7728
RN to Q ↑	0.0645	0.0837	4.5077	1.1692

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P16	X33_P16
D ↓	hold_rising to GN	-0.0243	-0.0166
D ↑	hold_rising to GN	-0.0169	-0.0364
D ↓	setup_rising to GN	0.0721	0.0615
D ↑	setup_rising to GN	0.0588	0.0854
GN ↓	min_pulse_width to GN	0.0739	0.0858
RN ↓	min_pulse_width to RN	0.0610	0.1147
RN ↑	recovery_rising to GN	0.0638	0.0924
RN ↑	removal_rising to GN	-0.0418	-0.0631

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	7.881e-06	1.000e-20
X33_P16	1.999e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X33_P16
D (output stable)	6.670e-05	1.209e-04
GN (output stable)	9.363e-04	1.436e-03
RN (output stable)	3.199e-05	6.154e-05
D to Q	4.019e-03	1.053e-02
GN to Q	5.767e-03	1.316e-02
RN to Q	3.134e-03	8.456e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

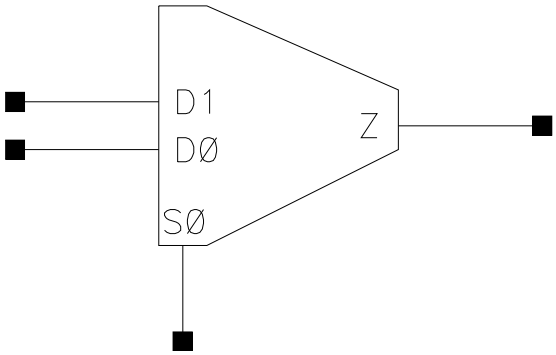
Pin Cycle (vdds)	X8_P16	X33_P16
D (output stable)	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
D0	0.0008	0.0012	0.0015	0.0021
D1	0.0008	0.0011	0.0015	0.0021
S0	0.0014	0.0016	0.0018	0.0027

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
D0 to Z ↓	0.0530	0.0463	2.7451	1.3444
D0 to Z ↑	0.0420	0.0380	4.5132	2.1998
D1 to Z ↓	0.0503	0.0457	2.7403	1.3428
D1 to Z ↑	0.0382	0.0356	4.5045	2.1980
S0 to Z ↓	0.0451	0.0431	2.7359	1.3410
S0 to Z ↑	0.0429	0.0425	4.5073	2.1963

	X25_P16	X33_P16	X25_P16	X33_P16
D0 to Z ↓	0.0502	0.0447	0.9238	0.6928
D0 to Z ↑	0.0411	0.0376	1.4783	1.1067
D1 to Z ↓	0.0535	0.0465	0.9269	0.6936
D1 to Z ↑	0.0393	0.0360	1.4763	1.1064
S0 to Z ↓	0.0496	0.0450	0.9241	0.6917
S0 to Z ↑	0.0475	0.0430	1.4769	1.1062

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	8.847e-06	1.000e-20
X17_P16	1.644e-05	1.000e-20
X25_P16	2.181e-05	1.000e-20
X33_P16	3.214e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	7.088e-04	1.045e-03	1.126e-03	1.535e-03
D1 (output stable)	5.751e-04	9.643e-04	1.263e-03	1.613e-03
S0 (output stable)	9.637e-04	1.104e-03	1.437e-03	1.776e-03
D0 to Z	2.706e-03	4.418e-03	6.918e-03	8.655e-03
D1 to Z	2.495e-03	4.280e-03	6.978e-03	8.576e-03
S0 to Z	3.083e-03	4.712e-03	7.728e-03	9.436e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

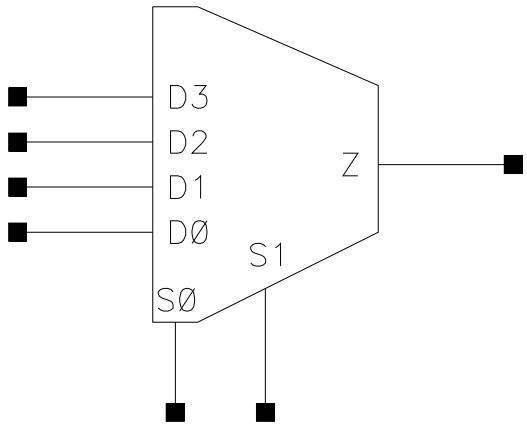
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	2.312	2.7744
X31_P16	1.200	4.624	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X8_P16	X31_P16
D0	0.0006	0.0015
D1	0.0006	0.0015
D2	0.0006	0.0015
D3	0.0006	0.0015
S0	0.0020	0.0040
S1	0.0013	0.0026

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X31_P16	X8_P16	X31_P16

D0 to Z ↓	0.0927	0.0931	2.8952	0.7985
D0 to Z ↑	0.0617	0.0636	4.5648	1.2206
D1 to Z ↓	0.0920	0.0933	2.8938	0.7989
D1 to Z ↑	0.0620	0.0635	4.5665	1.2211
D2 to Z ↓	0.0999	0.0879	2.9151	0.7919
D2 to Z ↑	0.0653	0.0591	4.5806	1.2144
D3 to Z ↓	0.0996	0.0872	2.9151	0.7903
D3 to Z ↑	0.0646	0.0604	4.5797	1.2179
S0 to Z ↓	0.1035	0.1029	2.9009	0.7941
S0 to Z ↑	0.0772	0.0802	4.5785	1.2198
S1 to Z ↓	0.0743	0.0711	2.9043	0.7947
S1 to Z ↑	0.0592	0.0604	4.5741	1.2188

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	8.717e-06	1.000e-20
X31_P16	2.684e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X31_P16
D0 (output stable)	1.087e-05	7.254e-05
D1 (output stable)	1.191e-05	8.532e-05
D2 (output stable)	1.560e-05	7.476e-05
D3 (output stable)	1.600e-05	9.567e-05
S0 (output stable)	1.448e-03	3.373e-03
S1 (output stable)	1.107e-03	2.456e-03
D0 to Z	3.020e-03	1.034e-02
D1 to Z	3.010e-03	1.039e-02
D2 to Z	3.249e-03	9.726e-03
D3 to Z	3.240e-03	9.719e-03
S0 to Z	4.651e-03	1.386e-02
S1 to Z	3.479e-03	1.018e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

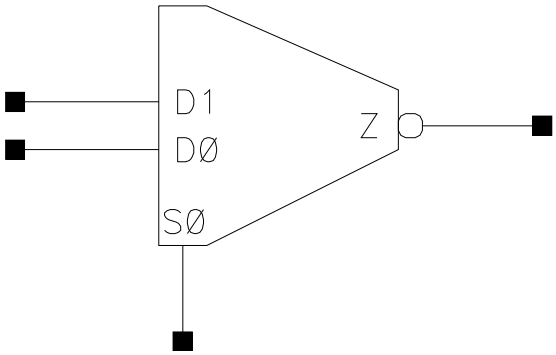
Pin Cycle (vdds)	X8_P16	X31_P16
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.816	0.9792
X5_P16	1.200	0.952	1.1424
X10_P16	1.200	1.768	2.1216
X16_P16	1.200	2.448	2.9376
X21_P16	1.200	3.128	3.7536

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X3_P16	X5_P16	X10_P16	X16_P16
D0	0.0006	0.0009	0.0018	0.0027
D1	0.0006	0.0009	0.0017	0.0026
S0	0.0012	0.0022	0.0029	0.0043
	X21_P16			
D0	0.0036			
D1	0.0035			
S0	0.0050			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X5_P16**	**X3_P16**	**X5_P16**
D0 to Z ↓	0.0177	0.0179	9.1429	5.4366

D0 to Z ↑	0.0298	0.0263	17.9291	8.9930
D1 to Z ↓	0.0174	0.0169	9.0591	5.2354
D1 to Z ↑	0.0310	0.0278	17.9439	9.2280
S0 to Z ↓	0.0275	0.0225	9.0752	5.3308
S0 to Z ↑	0.0296	0.0239	17.9142	9.0944
	X10_P16	**X16_P16**	**X10_P16**	**X16_P16**
D0 to Z ↓	0.0202	0.0187	2.5423	1.6588
D0 to Z ↑	0.0289	0.0275	4.1545	2.7249
D1 to Z ↓	0.0180	0.0178	2.4781	1.6367
D1 to Z ↑	0.0292	0.0282	4.1991	2.7452
S0 to Z ↓	0.0276	0.0237	2.5021	1.6444
S0 to Z ↑	0.0286	0.0246	4.1723	2.7328
	X21_P16		**X21_P16**	
D0 to Z ↓	0.0186		1.2616	
D0 to Z ↑	0.0269		2.0594	
D1 to Z ↓	0.0176		1.2390	
D1 to Z ↑	0.0283		2.0521	
S0 to Z ↓	0.0249		1.2468	
S0 to Z ↑	0.0253		2.0524	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	3.207e-06	1.000e-20
X5_P16	7.348e-06	1.000e-20
X10_P16	1.317e-05	1.000e-20
X16_P16	2.089e-05	1.000e-20
X21_P16	2.566e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	1.083e-05	2.540e-05	7.780e-05	1.234e-04
D1 (output stable)	1.085e-05	2.722e-05	6.701e-05	1.150e-04
S0 (output stable)	8.101e-04	1.198e-03	2.114e-03	3.282e-03
D0 to Z	7.910e-04	1.340e-03	3.360e-03	4.722e-03
D1 to Z	7.913e-04	1.330e-03	3.173e-03	4.652e-03
S0 to Z	1.425e-03	2.110e-03	4.422e-03	6.270e-03
	X21_P16			
D0 (output stable)	1.578e-04			
D1 (output stable)	1.568e-04			
S0 (output stable)	3.678e-03			
D0 to Z	6.070e-03			
D1 to Z	6.135e-03			
S0 to Z	7.689e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P16	X5_P16	X10_P16	X16_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

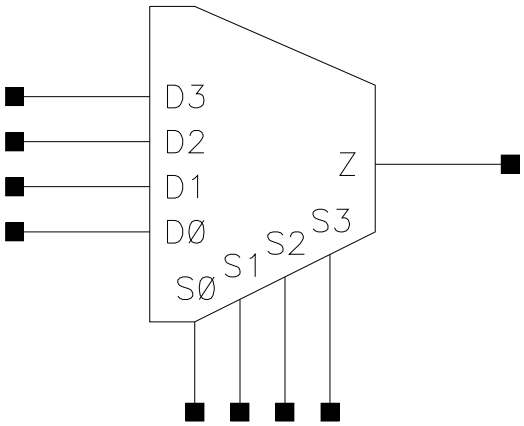
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P16			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	1.768	2.1216
X27_P16	1.200	3.672	4.4064

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X7_P16	X27_P16
D0	0.0007	0.0021
D1	0.0007	0.0021
D2	0.0007	0.0021
D3	0.0007	0.0021
S0	0.0007	0.0019
S1	0.0007	0.0020
S2	0.0007	0.0020
S3	0.0007	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	X27_P16	X7_P16	X27_P16
D0 to Z ↓	0.0701	0.0583	4.6303	1.2511
D0 to Z ↑	0.0513	0.0432	4.4513	1.1029
D1 to Z ↓	0.0633	0.0526	4.6260	1.2501
D1 to Z ↑	0.0459	0.0377	4.4315	1.0983
D2 to Z ↓	0.0714	0.0557	4.6388	1.2517
D2 to Z ↑	0.0501	0.0402	4.4706	1.1071
D3 to Z ↓	0.0646	0.0502	4.6324	1.2497
D3 to Z ↑	0.0448	0.0347	4.4498	1.1023
S0 to Z ↓	0.0679	0.0548	4.6277	1.2509
S0 to Z ↑	0.0540	0.0447	4.4509	1.1027
S1 to Z ↓	0.0614	0.0491	4.6233	1.2501
S1 to Z ↑	0.0485	0.0388	4.4325	1.0984
S2 to Z ↓	0.0690	0.0521	4.6366	1.2505
S2 to Z ↑	0.0528	0.0416	4.4714	1.1074
S3 to Z ↓	0.0626	0.0465	4.6308	1.2485
S3 to Z ↑	0.0473	0.0358	4.4522	1.1028

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X7_P16	8.139e-06	1.000e-20
X27_P16	3.291e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X7_P16	X27_P16
D0 (output stable)	4.423e-04	1.409e-03
D1 (output stable)	3.662e-04	1.136e-03
D2 (output stable)	4.088e-04	1.316e-03
D3 (output stable)	3.331e-04	1.044e-03
S0 (output stable)	4.300e-04	1.342e-03
S1 (output stable)	3.525e-04	1.078e-03
S2 (output stable)	3.960e-04	1.250e-03
S3 (output stable)	3.186e-04	9.867e-04
D0 to Z	3.435e-03	1.078e-02
D1 to Z	3.012e-03	9.263e-03
D2 to Z	3.321e-03	9.436e-03
D3 to Z	2.903e-03	7.929e-03
S0 to Z	3.346e-03	1.022e-02
S1 to Z	2.924e-03	8.732e-03
S2 to Z	3.227e-03	8.850e-03
S3 to Z	2.811e-03	7.393e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

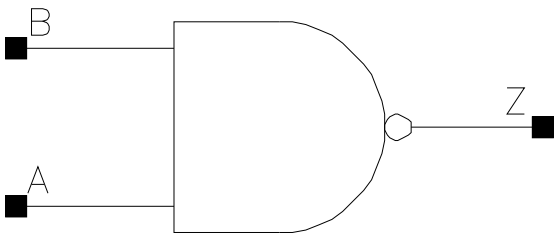
Pin Cycle (vdds)	X7_P16	X27_P16
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description

2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND2X3_P16	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X5_P16	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X7_P16	1.200	0.408	0.4896
C12T28SOI_LL_-NAND2X10_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X13_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND2X17_P16	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X20_P16	1.200	0.952	1.1424
C12T28SOI_LL_-NAND2X24_P16	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X27_P16	1.200	1.224	1.4688
C12T28SOI_LL_-NAND2X42_P16	1.200	1.360	1.6320
C12T28SOI_LL_-NAND2X47_P16	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X50_P16	1.200	1.496	1.7952
C12T28SOI_LL_-NAND2X58_P16	1.200	1.632	1.9584
C12T28SOI_LL_-NAND2X67_P16	1.200	1.768	2.1216
C12T28SOI_LLBR0D8_-NAND2X7_P16	1.200	0.952	1.1424
C12T28SOI_LLBR0D8_-NAND2X14_P16	1.200	1.224	1.4688

C12T28SOI_LLS_-NAND2X40_P16	1.200	1.768	2.1216
C12T28SOI_LLS_-NAND2X54_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND2X3_P16	C12T28SOI_LL_-NAND2X5_P16	C12T28SOI_LL_-NAND2X7_P16	C12T28SOI_LL_-NAND2X10_P16
A	0.0006	0.0007	0.0009	0.0014
B	0.0006	0.0007	0.0009	0.0013
	C12T28SOI_LL_-NAND2X13_P16	C12T28SOI_LL_-NAND2X17_P16	C12T28SOI_LL_-NAND2X20_P16	C12T28SOI_LL_-NAND2X24_P16
A	0.0018	0.0022	0.0026	0.0031
B	0.0016	0.0021	0.0024	0.0029
	C12T28SOI_LL_-NAND2X27_P16	C12T28SOI_LL_-NAND2X42_P16	C12T28SOI_LL_-NAND2X47_P16	C12T28SOI_LL_-NAND2X50_P16
A	0.0034	0.0011	0.0011	0.0011
B	0.0032	0.0011	0.0011	0.0011
	C12T28SOI_LL_-NAND2X58_P16	C12T28SOI_LL_-NAND2X67_P16	C12T28SOI_-LLBR0D8_-NAND2X7_P16	C12T28SOI_-LLBR0D8_-NAND2X14_P16
A	0.0011	0.0011	0.0009	0.0018
B	0.0011	0.0011	0.0009	0.0016
	C12T28SOI_LLS_-NAND2X40_P16	C12T28SOI_LLS_-NAND2X54_P16		
A	0.0051	0.0069		
B	0.0047	0.0063		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND2X3_P16	**C12T28SOI_LL_-NAND2X5_P16**	**C12T28SOI_LL_-NAND2X3_P16**	**C12T28SOI_LL_-NAND2X5_P16**
A to Z ↓	0.0132	0.0121	8.8741	5.6552
A to Z ↑	0.0191	0.0172	8.7313	5.5303
B to Z ↓	0.0145	0.0127	8.9408	5.7027
B to Z ↑	0.0172	0.0149	8.7798	5.5616
	C12T28SOI_LL_-NAND2X7_P16	**C12T28SOI_LL_-NAND2X10_P16**	**C12T28SOI_LL_-NAND2X7_P16**	**C12T28SOI_LL_-NAND2X10_P16**
A to Z ↓	0.0120	0.0141	4.7266	3.1360
A to Z ↑	0.0167	0.0181	4.4665	2.9408
B to Z ↓	0.0125	0.0124	4.7570	3.1625
B to Z ↑	0.0143	0.0142	4.5020	2.9600
	C12T28SOI_LL_-NAND2X13_P16	**C12T28SOI_LL_-NAND2X17_P16**	**C12T28SOI_LL_-NAND2X13_P16**	**C12T28SOI_LL_-NAND2X17_P16**
A to Z ↓	0.0135	0.0133	2.3960	1.9173

A to Z ↑	0.0170	0.0172	2.1872	1.7699
B to Z ↓	0.0119	0.0126	2.4168	1.9328
B to Z ↑	0.0131	0.0140	2.2025	1.7783
	C12T28SOI_LL_-NAND2X20_P16	**C12T28SOI_LL_-NAND2X24_P16**	**C12T28SOI_LL_-NAND2X20_P16**	**C12T28SOI_LL_-NAND2X24_P16**
A to Z ↓	0.0130	0.0136	1.6350	1.3938
A to Z ↑	0.0166	0.0171	1.4687	1.2597
B to Z ↓	0.0124	0.0121	1.6481	1.4058
B to Z ↑	0.0134	0.0133	1.4795	1.2677
	C12T28SOI_LL_-NAND2X27_P16	**C12T28SOI_LL_-NAND2X42_P16**	**C12T28SOI_LL_-NAND2X27_P16**	**C12T28SOI_LL_-NAND2X42_P16**
A to Z ↓	0.0133	0.0511	1.2385	0.5498
A to Z ↑	0.0166	0.0507	1.1014	0.8762
B to Z ↓	0.0119	0.0524	1.2492	0.5497
B to Z ↑	0.0129	0.0486	1.1088	0.8759
	C12T28SOI_LL_-NAND2X47_P16	**C12T28SOI_LL_-NAND2X50_P16**	**C12T28SOI_LL_-NAND2X47_P16**	**C12T28SOI_LL_-NAND2X50_P16**
A to Z ↓	0.0527	0.0534	0.4897	0.4591
A to Z ↑	0.0515	0.0521	0.7643	0.7316
B to Z ↓	0.0541	0.0547	0.4898	0.4593
B to Z ↑	0.0495	0.0500	0.7645	0.7317
	C12T28SOI_LL_-NAND2X58_P16	**C12T28SOI_LL_-NAND2X67_P16**	**C12T28SOI_LL_-NAND2X58_P16**	**C12T28SOI_LL_-NAND2X67_P16**
A to Z ↓	0.0561	0.0582	0.3977	0.3497
A to Z ↑	0.0540	0.0553	0.6288	0.5521
B to Z ↓	0.0574	0.0595	0.3977	0.3497
B to Z ↑	0.0519	0.0532	0.6292	0.5525
	C12T28SOI_-LLBR0D8_-NAND2X7_P16	**C12T28SOI_-LLBR0D8_-NAND2X14_P16**	**C12T28SOI_-LLBR0D8_-NAND2X7_P16**	**C12T28SOI_-LLBR0D8_-NAND2X14_P16**
A to Z ↓	0.0100	0.0116	3.5368	1.8406
A to Z ↑	0.0206	0.0210	5.9595	2.8989
B to Z ↓	0.0099	0.0090	3.5770	1.8654
B to Z ↑	0.0168	0.0150	6.1076	2.9463
	C12T28SOI_LLS_-NAND2X40_P16	**C12T28SOI_LLS_-NAND2X54_P16**	**C12T28SOI_LLS_-NAND2X40_P16**	**C12T28SOI_LLS_-NAND2X54_P16**
A to Z ↓	0.0132	0.0132	0.8373	0.6328
A to Z ↑	0.0165	0.0165	0.7369	0.5542
B to Z ↓	0.0120	0.0122	0.8447	0.6385
B to Z ↑	0.0129	0.0129	0.7422	0.5590

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_NAND2X3_P16	1.557e-06	1.000e-20
C12T28SOI_LL_NAND2X5_P16	2.685e-06	1.000e-20
C12T28SOI_LL_NAND2X7_P16	3.365e-06	1.000e-20
C12T28SOI_LL_NAND2X10_P16	4.614e-06	1.000e-20
C12T28SOI_LL_NAND2X13_P16	6.477e-06	1.000e-20
C12T28SOI_LL_NAND2X17_P16	7.640e-06	1.000e-20
C12T28SOI_LL_NAND2X20_P16	9.389e-06	1.000e-20
C12T28SOI_LL_NAND2X24_P16	1.065e-05	1.000e-20
C12T28SOI_LL_NAND2X27_P16	1.231e-05	1.000e-20

C12T28SOI_LL_NAND2X42_P16	2.246e-05	1.000e-20
C12T28SOI_LL_NAND2X47_P16	2.424e-05	1.000e-20
C12T28SOI_LL_NAND2X50_P16	2.494e-05	1.000e-20
C12T28SOI_LL_NAND2X58_P16	2.742e-05	1.000e-20
C12T28SOI_LL_NAND2X67_P16	2.990e-05	1.000e-20
C12T28SOI_LLBR0D8_NAND2X7_-P16	3.424e-06	1.000e-20
C12T28SOI_LLBR0D8_NAND2X14_-P16	6.439e-06	1.000e-20
C12T28SOI_LLS_NAND2X40_P16	1.815e-05	1.000e-20
C12T28SOI_LLS_NAND2X54_P16	2.399e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND2X3_P16	C12T28SOI_LL_-NAND2X5_P16	C12T28SOI_LL_-NAND2X7_P16	C12T28SOI_LL_-NAND2X10_P16
A (output stable)	8.333e-06	1.271e-05	1.556e-05	5.445e-05
B (output stable)	1.690e-05	2.652e-05	3.254e-05	2.387e-04
A to Z	5.462e-04	7.374e-04	8.832e-04	1.565e-03
B to Z	4.483e-04	5.777e-04	6.867e-04	1.029e-03
	C12T28SOI_LL_-NAND2X13_P16	C12T28SOI_LL_-NAND2X17_P16	C12T28SOI_LL_-NAND2X20_P16	C12T28SOI_LL_-NAND2X24_P16
A (output stable)	6.602e-05	7.748e-05	8.616e-05	1.206e-04
B (output stable)	2.710e-04	2.474e-04	2.662e-04	4.514e-04
A to Z	1.925e-03	2.390e-03	2.729e-03	3.350e-03
B to Z	1.259e-03	1.678e-03	1.919e-03	2.208e-03
	C12T28SOI_LL_-NAND2X27_P16	C12T28SOI_LL_-NAND2X42_P16	C12T28SOI_LL_-NAND2X47_P16	C12T28SOI_LL_-NAND2X50_P16
A (output stable)	1.279e-04	1.734e-05	1.742e-05	1.742e-05
B (output stable)	4.838e-04	3.437e-05	3.435e-05	3.445e-05
A to Z	3.684e-03	9.620e-03	1.038e-02	1.077e-02
B to Z	2.436e-03	9.417e-03	1.019e-02	1.057e-02
	C12T28SOI_LL_-NAND2X58_P16	C12T28SOI_LL_-NAND2X67_P16	C12T28SOI_-LLBR0D8_-NAND2X7_P16	C12T28SOI_-LLBR0D8_-NAND2X14_P16
A (output stable)	1.751e-05	1.757e-05	2.019e-05	8.154e-05
B (output stable)	3.457e-05	3.456e-05	4.274e-05	3.323e-04
A to Z	1.228e-02	1.351e-02	9.221e-04	2.019e-03
B to Z	1.208e-02	1.331e-02	6.474e-04	1.144e-03
	C12T28SOI_LLS_-NAND2X40_P16	C12T28SOI_LLS_-NAND2X54_P16		
A (output stable)	1.835e-04	2.428e-04		
B (output stable)	6.456e-04	8.165e-04		
A to Z	5.436e-03	7.179e-03		
B to Z	3.656e-03	4.862e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND2X3_P16	C12T28SOI_LL_-NAND2X5_P16	C12T28SOI_LL_-NAND2X7_P16	C12T28SOI_LL_-NAND2X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

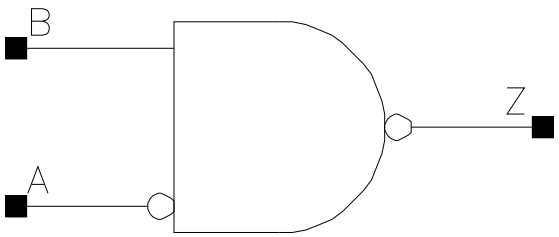
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X13_P16	C12T28SOI_LL_-NAND2X17_P16	C12T28SOI_LL_-NAND2X20_P16	C12T28SOI_LL_-NAND2X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X27_P16	C12T28SOI_LL_-NAND2X42_P16	C12T28SOI_LL_-NAND2X47_P16	C12T28SOI_LL_-NAND2X50_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND2X58_P16	C12T28SOI_LL_-NAND2X67_P16	C12T28SOI_-LLBR0D8_-NAND2X7_P16	C12T28SOI_-LLBR0D8_-NAND2X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLS_-NAND2X40_P16	C12T28SOI_LLS_-NAND2X54_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X7_P16	1.200	0.544	0.6528
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X40_P16	1.200	2.312	2.7744
X54_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X3_P16	X7_P16	X13_P16	X27_P16
A	0.0009	0.0009	0.0012	0.0022
B	0.0006	0.0008	0.0016	0.0032
	X40_P16	X54_P16		
A	0.0033	0.0043		
B	0.0047	0.0063		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X7_P16**	**X3_P16**	**X7_P16**
A to Z ↓	0.0359	0.0383	8.9046	4.7348
A to Z ↑	0.0288	0.0300	8.5960	4.4340
B to Z ↓	0.0149	0.0125	9.0409	4.7939
B to Z ↑	0.0174	0.0142	8.7825	4.5292
	X13_P16	**X27_P16**	**X13_P16**	**X27_P16**

A to Z ↓	0.0351	0.0339	2.4945	1.2379
A to Z ↑	0.0283	0.0274	2.2593	1.0973
B to Z ↓	0.0116	0.0116	2.5314	1.2578
B to Z ↑	0.0130	0.0127	2.2572	1.1100
	X40_P16	**X54_P16**	**X40_P16**	**X54_P16**
A to Z ↓	0.0345	0.0343	0.8292	0.6281
A to Z ↑	0.0280	0.0278	0.7308	0.5505
B to Z ↓	0.0116	0.0117	0.8420	0.6377
B to Z ↑	0.0125	0.0125	0.7450	0.5613

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	2.829e-06	1.000e-20
X7_P16	4.654e-06	1.000e-20
X13_P16	9.649e-06	1.000e-20
X27_P16	1.855e-05	1.000e-20
X40_P16	2.712e-05	1.000e-20
X54_P16	3.569e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	8.762e-04	1.136e-03	1.855e-03	3.568e-03
B (output stable)	1.729e-05	3.265e-05	2.380e-04	4.018e-04
A to Z	1.491e-03	2.103e-03	3.852e-03	7.530e-03
B to Z	4.553e-04	6.799e-04	1.228e-03	2.437e-03
	X40_P16	X54_P16		
A (output stable)	5.520e-03	7.235e-03		
B (output stable)	5.762e-04	7.662e-04		
A to Z	1.135e-02	1.492e-02		
B to Z	3.531e-03	4.656e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

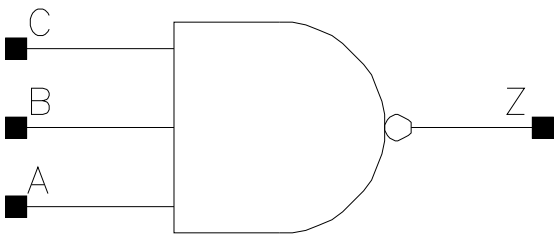
Pin Cycle (vdds)	X3_P16	X7_P16	X13_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X40_P16	X54_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-NAND3X4_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X6_P16	1.200	0.680	0.8160
C12T28SOI_LL_-NAND3X9_P16	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X12_P16	1.200	1.088	1.3056
C12T28SOI_LL_-NAND3X15_P16	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X18_P16	1.200	1.360	1.6320
C12T28SOI_LL_-NAND3X21_P16	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X24_P16	1.200	1.904	2.2848
C12T28SOI_LL_-NAND3X35_P16	1.200	2.720	3.2640
C12T28SOI_LL_-NAND3X47_P16	1.200	3.536	4.2432
C12T28SOI_LLBR0P6_-NAND3X6_P16	1.200	1.224	1.4688
C12T28SOI_LLBR0P6_-NAND3X12_P16	1.200	1.632	1.9584
C12T28SOI_LLBR0P6_-NAND3X18_P16	1.200	1.904	2.2848
C12T28SOI_LLBR0P6_-NAND3X24_P16	1.200	2.448	2.9376
C12T28SOI_LLBR0P6_-NAND3X35_P16	1.200	3.264	3.9168
C12T28SOI_LLBR0P6_-NAND3X47_P16	1.200	4.080	4.8960

C12T28SOIDV_LLBR0P6_-NAND3X18_P16	2.400	1.088	2.6112

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A	0.0007	0.0009	0.0014	0.0018
B	0.0007	0.0009	0.0014	0.0017
C	0.0007	0.0008	0.0013	0.0016
	C12T28SOI_LL_-NAND3X15_P16	C12T28SOI_LL_-NAND3X18_P16	C12T28SOI_LL_-NAND3X21_P16	C12T28SOI_LL_-NAND3X24_P16
A	0.0022	0.0026	0.0031	0.0034
B	0.0022	0.0025	0.0029	0.0033
C	0.0020	0.0023	0.0028	0.0031
	C12T28SOI_LL_-NAND3X35_P16	C12T28SOI_LL_-NAND3X47_P16	C12T28SOI_-LLBR0P6_-NAND3X6_P16	C12T28SOI_-LLBR0P6_-NAND3X12_P16
A	0.0052	0.0069	0.0009	0.0018
B	0.0050	0.0066	0.0009	0.0017
C	0.0047	0.0063	0.0008	0.0016
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	C12T28SOI_-LLBR0P6_-NAND3X24_P16	C12T28SOI_-LLBR0P6_-NAND3X35_P16	C12T28SOI_-LLBR0P6_-NAND3X47_P16
A	0.0026	0.0035	0.0052	0.0069
B	0.0025	0.0033	0.0049	0.0065
C	0.0023	0.0030	0.0045	0.0060
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16			
A	0.0027			
B	0.0026			
C	0.0024			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16
A to Z ↓	0.0221	0.0200	9.3172	6.6190
A to Z ↑	0.0244	0.0220	6.3253	4.3367
B to Z ↓	0.0232	0.0206	9.3331	6.6302
B to Z ↑	0.0234	0.0207	6.3373	4.3448
C to Z ↓	0.0202	0.0181	9.3582	6.6496
C to Z ↑	0.0200	0.0175	6.3445	4.3671

	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A to Z ↓	0.0221	0.0206	4.5077	3.4706
A to Z ↑	0.0231	0.0214	2.9546	2.2051
B to Z ↓	0.0206	0.0193	4.5168	3.4775
B to Z ↑	0.0209	0.0194	2.9584	2.2083
C to Z ↓	0.0180	0.0169	4.5308	3.4887
C to Z ↑	0.0175	0.0160	2.9541	2.1978
	C12T28SOI_LL_-NAND3X15_P16	**C12T28SOI_LL_-NAND3X18_P16**	**C12T28SOI_LL_-NAND3X15_P16**	**C12T28SOI_LL_-NAND3X18_P16**
A to Z ↓	0.0198	0.0193	2.8231	2.3985
A to Z ↑	0.0211	0.0204	1.7676	1.4666
B to Z ↓	0.0192	0.0187	2.8287	2.4039
B to Z ↑	0.0191	0.0184	1.7714	1.4699
C to Z ↓	0.0172	0.0166	2.8382	2.4112
C to Z ↑	0.0160	0.0153	1.7818	1.4785
	C12T28SOI_LL_-NAND3X21_P16	**C12T28SOI_LL_-NAND3X24_P16**	**C12T28SOI_LL_-NAND3X21_P16**	**C12T28SOI_LL_-NAND3X24_P16**
A to Z ↓	0.0204	0.0199	2.0270	1.8044
A to Z ↑	0.0212	0.0206	1.2652	1.1071
B to Z ↓	0.0192	0.0189	2.0308	1.8083
B to Z ↑	0.0192	0.0187	1.2670	1.1087
C to Z ↓	0.0170	0.0167	2.0375	1.8139
C to Z ↑	0.0159	0.0154	1.2690	1.1098
	C12T28SOI_LL_-NAND3X35_P16	**C12T28SOI_LL_-NAND3X47_P16**	**C12T28SOI_LL_-NAND3X35_P16**	**C12T28SOI_LL_-NAND3X47_P16**
A to Z ↓	0.0193	0.0195	1.2273	0.9314
A to Z ↑	0.0202	0.0203	0.7401	0.5577
B to Z ↓	0.0186	0.0186	1.2299	0.9334
B to Z ↑	0.0182	0.0182	0.7405	0.5569
C to Z ↓	0.0166	0.0167	1.2344	0.9366
C to Z ↑	0.0149	0.0149	0.7445	0.5596
	C12T28SOI_-LLBR0P6_-NAND3X6_P16	**C12T28SOI_-LLBR0P6_-NAND3X12_P16**	**C12T28SOI_-LLBR0P6_-NAND3X6_P16**	**C12T28SOI_-LLBR0P6_-NAND3X12_P16**
A to Z ↓	0.0159	0.0167	4.4408	2.3324
A to Z ↑	0.0316	0.0313	6.8860	3.4961
B to Z ↓	0.0159	0.0148	4.4602	2.3441
B to Z ↑	0.0284	0.0266	6.9005	3.4990
C to Z ↓	0.0125	0.0112	4.4915	2.3624
C to Z ↑	0.0216	0.0194	6.9343	3.5091
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	**C12T28SOI_-LLBR0P6_-NAND3X24_P16**	**C12T28SOI_-LLBR0P6_-NAND3X18_P16**	**C12T28SOI_-LLBR0P6_-NAND3X24_P16**
A to Z ↓	0.0155	0.0161	1.6154	1.2164
A to Z ↑	0.0296	0.0301	2.3269	1.7539
B to Z ↓	0.0143	0.0144	1.6232	1.2221
B to Z ↑	0.0250	0.0255	2.3306	1.7558
C to Z ↓	0.0112	0.0110	1.6354	1.2320
C to Z ↑	0.0186	0.0186	2.3451	1.7597
	C12T28SOI_-LLBR0P6_-NAND3X35_P16	**C12T28SOI_-LLBR0P6_-NAND3X47_P16**	**C12T28SOI_-LLBR0P6_-NAND3X35_P16**	**C12T28SOI_-LLBR0P6_-NAND3X47_P16**

A to Z ↓	0.0156	0.0157	0.8300	0.6321
A to Z ↑	0.0299	0.0299	1.1944	0.9012
B to Z ↓	0.0143	0.0144	0.8346	0.6354
B to Z ↑	0.0252	0.0252	1.1950	0.9014
C to Z ↓	0.0110	0.0113	0.8414	0.6402
C to Z ↑	0.0183	0.0185	1.2062	0.9044
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16		**C12T28SOIDV_-LLBR0P6_-NAND3X18_P16**	
A to Z ↓	0.0166		1.5525	
A to Z ↑	0.0298		2.1874	
B to Z ↓	0.0146		1.5602	
B to Z ↑	0.0253		2.1893	
C to Z ↓	0.0109		1.5724	
C to Z ↑	0.0182		2.1808	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
C12T28SOI_LL_NAND3X4_P16	1.966e-06	1.000e-20
C12T28SOI_LL_NAND3X6_P16	2.999e-06	1.000e-20
C12T28SOI_LL_NAND3X9_P16	3.976e-06	1.000e-20
C12T28SOI_LL_NAND3X12_P16	5.527e-06	1.000e-20
C12T28SOI_LL_NAND3X15_P16	6.228e-06	1.000e-20
C12T28SOI_LL_NAND3X18_P16	7.632e-06	1.000e-20
C12T28SOI_LL_NAND3X21_P16	9.005e-06	1.000e-20
C12T28SOI_LL_NAND3X24_P16	1.037e-05	1.000e-20
C12T28SOI_LL_NAND3X35_P16	1.521e-05	1.000e-20
C12T28SOI_LL_NAND3X47_P16	2.003e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X6_-P16	3.237e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X12_-P16	5.824e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X18_-P16	7.777e-06	1.000e-20
C12T28SOI_LLBR0P6_NAND3X24_-P16	1.067e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X35_-P16	1.551e-05	1.000e-20
C12T28SOI_LLBR0P6_NAND3X47_-P16	2.033e-05	1.000e-20
C12T28SOIDV_LLBR0P6_-NAND3X18_P16	9.640e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A (output stable)	1.703e-05	2.349e-05	6.005e-05	7.112e-05
B (output stable)	4.304e-05	5.483e-05	1.482e-04	1.712e-04
C (output stable)	2.003e-04	2.389e-04	3.923e-04	4.502e-04
A to Z	1.267e-03	1.568e-03	2.535e-03	3.014e-03
B to Z	1.133e-03	1.365e-03	2.028e-03	2.416e-03
C to Z	8.638e-04	1.037e-03	1.497e-03	1.775e-03

	C12T28SOI_LL_-NAND3X15_P16	C12T28SOI_LL_-NAND3X18_P16	C12T28SOI_LL_-NAND3X21_P16	C12T28SOI_LL_-NAND3X24_P16
A (output stable)	7.687e-05	8.731e-05	1.207e-04	1.309e-04
B (output stable)	1.892e-04	2.158e-04	2.904e-04	3.168e-04
C (output stable)	4.691e-04	5.373e-04	7.447e-04	7.992e-04
A to Z	3.580e-03	4.075e-03	5.130e-03	5.621e-03
B to Z	2.874e-03	3.260e-03	4.096e-03	4.480e-03
C to Z	2.165e-03	2.419e-03	3.025e-03	3.299e-03
	C12T28SOI_LL_-NAND3X35_P16	C12T28SOI_LL_-NAND3X47_P16	C12T28SOI_-LLBR0P6_-NAND3X6_P16	C12T28SOI_-LLBR0P6_-NAND3X12_P16
A (output stable)	1.747e-04	2.336e-04	3.389e-05	1.010e-04
B (output stable)	4.313e-04	5.663e-04	7.906e-05	2.510e-04
C (output stable)	1.142e-03	1.471e-03	3.228e-04	6.473e-04
A to Z	8.090e-03	1.069e-02	1.719e-03	3.387e-03
B to Z	6.441e-03	8.489e-03	1.401e-03	2.479e-03
C to Z	4.664e-03	6.212e-03	9.041e-04	1.470e-03
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	C12T28SOI_-LLBR0P6_-NAND3X24_P16	C12T28SOI_-LLBR0P6_-NAND3X35_P16	C12T28SOI_-LLBR0P6_-NAND3X47_P16
A (output stable)	1.226e-04	1.870e-04	2.487e-04	3.228e-04
B (output stable)	3.078e-04	4.603e-04	6.273e-04	7.993e-04
C (output stable)	7.479e-04	1.165e-03	1.694e-03	2.158e-03
A to Z	4.545e-03	6.285e-03	9.076e-03	1.190e-02
B to Z	3.304e-03	4.582e-03	6.601e-03	8.727e-03
C to Z	2.044e-03	2.727e-03	3.854e-03	5.134e-03
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16			
A (output stable)	1.470e-04			
B (output stable)	3.735e-04			
C (output stable)	9.360e-04			
A to Z	5.015e-03			
B to Z	3.670e-03			
C to Z	2.155e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	C12T28SOI_LL_-NAND3X4_P16	C12T28SOI_LL_-NAND3X6_P16	C12T28SOI_LL_-NAND3X9_P16	C12T28SOI_LL_-NAND3X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X15_P16	C12T28SOI_LL_-NAND3X18_P16	C12T28SOI_LL_-NAND3X21_P16	C12T28SOI_LL_-NAND3X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

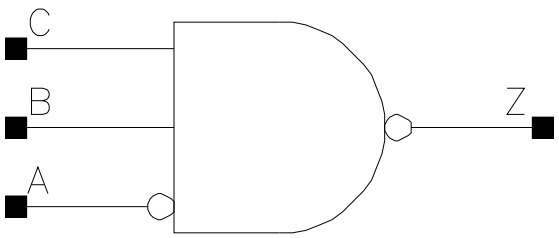
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-NAND3X35_P16	C12T28SOI_LL_-NAND3X47_P16	C12T28SOI_-LLBR0P6_-NAND3X6_P16	C12T28SOI_-LLBR0P6_-NAND3X12_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_-LLBR0P6_-NAND3X18_P16	C12T28SOI_-LLBR0P6_-NAND3X24_P16	C12T28SOI_-LLBR0P6_-NAND3X35_P16	C12T28SOI_-LLBR0P6_-NAND3X47_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOIDV_-LLBR0P6_-NAND3X18_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.816	0.9792
X12_P16	1.200	1.224	1.4688
X18_P16	1.200	1.496	1.7952
X24_P16	1.200	2.312	2.7744

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0008	0.0012	0.0012	0.0021
B	0.0009	0.0017	0.0025	0.0033
C	0.0008	0.0016	0.0023	0.0031

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X12_P16**	**X6_P16**	**X12_P16**
A to Z ↓	0.0438	0.0418	6.6863	3.5066
A to Z ↑	0.0324	0.0313	4.3102	2.1613
B to Z ↓	0.0175	0.0184	6.7153	3.5225
B to Z ↑	0.0185	0.0185	4.3548	2.1882
C to Z ↓	0.0174	0.0158	6.7368	3.5340
C to Z ↑	0.0163	0.0149	4.3776	2.2020
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0481	0.0403	2.4025	1.8105

A to Z ↑	0.0360	0.0297	1.4537	1.0885
B to Z ↓	0.0187	0.0181	2.4108	1.8187
B to Z ↑	0.0183	0.0179	1.4703	1.1044
C to Z ↓	0.0168	0.0156	2.4175	1.8251
C to Z ↑	0.0154	0.0143	1.4773	1.1112

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P16	4.105e-06	1.000e-20
X12_P16	8.577e-06	1.000e-20
X18_P16	1.060e-05	1.000e-20
X24_P16	1.678e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	1.117e-03	1.982e-03	2.711e-03	3.685e-03
B (output stable)	4.032e-05	1.407e-04	2.317e-04	3.225e-04
C (output stable)	1.005e-04	4.500e-04	5.407e-04	8.292e-04
A to Z	2.536e-03	5.026e-03	7.216e-03	9.577e-03
B to Z	1.105e-03	2.229e-03	3.263e-03	4.181e-03
C to Z	9.009e-04	1.563e-03	2.430e-03	2.917e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

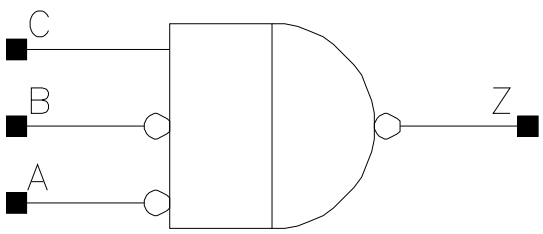
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X7_P16	1.200	0.816	0.9792
X13_P16	1.200	1.088	1.3056
X20_P16	1.200	1.632	1.9584
X27_P16	1.200	1.904	2.2848

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X7_P16	X13_P16	X20_P16	X27_P16
A	0.0011	0.0010	0.0021	0.0019
B	0.0012	0.0011	0.0021	0.0020
C	0.0009	0.0016	0.0024	0.0031

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X7_P16	**X13_P16**	**X7_P16**	**X13_P16**
A to Z ↓	0.0404	0.0499	4.5426	2.4025
A to Z ↑	0.0275	0.0316	4.2833	2.1542
B to Z ↓	0.0401	0.0498	4.5454	2.4031
B to Z ↑	0.0259	0.0301	4.2831	2.1541
C to Z ↓	0.0124	0.0116	4.5943	2.4196
C to Z ↑	0.0142	0.0129	4.3666	2.2011
	X20_P16	**X27_P16**	**X20_P16**	**X27_P16**
A to Z ↓	0.0454	0.0501	1.6304	1.2351
A to Z ↑	0.0294	0.0352	1.4481	1.0885
B to Z ↓	0.0421	0.0478	1.6306	1.2357

B to Z ↑	0.0269	0.0332	1.4456	1.0868
C to Z ↓	0.0128	0.0122	1.6479	1.2456
C to Z ↑	0.0138	0.0133	1.4790	1.1099

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X7_P16	6.314e-06	1.000e-20
X13_P16	8.590e-06	1.000e-20
X20_P16	1.383e-05	1.000e-20
X27_P16	1.548e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	6.276e-04	8.522e-04	1.452e-03	1.704e-03
B (output stable)	5.466e-04	7.718e-04	1.200e-03	1.492e-03
C (output stable)	3.454e-05	2.863e-04	2.465e-04	3.370e-04
A to Z	2.815e-03	4.651e-03	7.357e-03	9.159e-03
B to Z	2.538e-03	4.379e-03	6.420e-03	8.362e-03
C to Z	7.069e-04	1.229e-03	2.029e-03	2.641e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

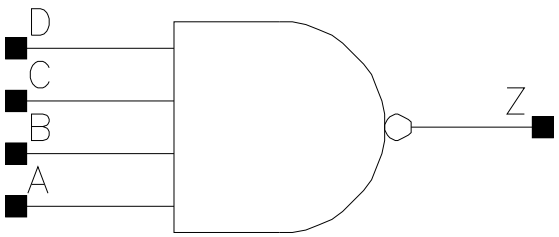
Pin Cycle (vdds)	X7_P16	X13_P16	X20_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0007	0.0007	0.0009	0.0011
B	0.0008	0.0007	0.0009	0.0012
C	0.0007	0.0007	0.0009	0.0011
D	0.0007	0.0007	0.0009	0.0012

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0679	0.0661	2.6772	1.3390
A to Z ↑	0.0528	0.0569	4.3570	2.1691
B to Z ↓	0.0696	0.0689	2.6742	1.3388
B to Z ↑	0.0508	0.0562	4.3556	2.1702
C to Z ↓	0.0682	0.0658	2.6761	1.3394
C to Z ↑	0.0539	0.0593	4.3511	2.1675

D to Z ↓	0.0703	0.0674	2.6761	1.3380
D to Z ↑	0.0527	0.0570	4.3513	2.1645
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0702	0.0646	0.9202	0.6904
A to Z ↑	0.0549	0.0538	1.4569	1.0953
B to Z ↓	0.0721	0.0662	0.9208	0.6903
B to Z ↑	0.0534	0.0521	1.4567	1.0949
C to Z ↓	0.0648	0.0595	0.9200	0.6904
C to Z ↑	0.0556	0.0540	1.4558	1.0919
D to Z ↓	0.0664	0.0611	0.9209	0.6905
D to Z ↑	0.0534	0.0520	1.4555	1.0919

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	6.926e-06	1.000e-20
X17_P16	1.098e-05	1.000e-20
X25_P16	1.564e-05	1.000e-20
X33_P16	2.126e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	4.415e-04	5.544e-04	8.127e-04	9.667e-04
B (output stable)	4.042e-04	5.241e-04	7.597e-04	8.949e-04
C (output stable)	4.343e-04	5.289e-04	8.137e-04	9.246e-04
D (output stable)	3.977e-04	4.878e-04	7.509e-04	8.475e-04
A to Z	3.332e-03	5.084e-03	7.904e-03	9.734e-03
B to Z	3.229e-03	4.993e-03	7.752e-03	9.534e-03
C to Z	3.403e-03	4.994e-03	7.376e-03	9.005e-03
D to Z	3.310e-03	4.886e-03	7.216e-03	8.806e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

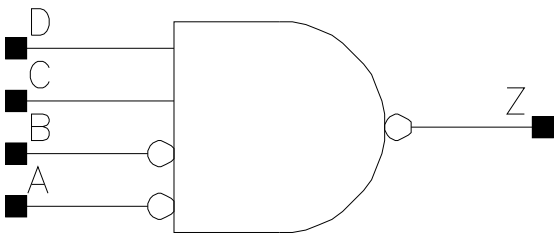
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X12_P16	1.200	1.496	1.7952
X18_P16	1.200	2.040	2.4480
X24_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X6_P16	X12_P16	X18_P16	X24_P16
A	0.0011	0.0011	0.0021	0.0019
B	0.0011	0.0015	0.0021	0.0019
C	0.0009	0.0017	0.0024	0.0033
D	0.0008	0.0016	0.0023	0.0032

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X12_P16	X6_P16	X12_P16
A to Z ↓	0.0433	0.0591	6.8579	3.5146
A to Z ↑	0.0292	0.0357	4.2834	2.1585
B to Z ↓	0.0422	0.0575	6.8606	3.5160
B to Z ↑	0.0266	0.0338	4.2832	2.1547
C to Z ↓	0.0175	0.0183	6.8865	3.5208
C to Z ↑	0.0185	0.0184	4.5475	2.1881

D to Z ↓	0.0171	0.0158	6.9063	3.5321
D to Z ↑	0.0162	0.0148	4.5696	2.2023
	X18_P16	**X24_P16**	**X18_P16**	**X24_P16**
A to Z ↓	0.0507	0.0568	2.3968	1.8162
A to Z ↑	0.0314	0.0400	1.4491	1.0901
B to Z ↓	0.0475	0.0542	2.3972	1.8165
B to Z ↑	0.0290	0.0375	1.4467	1.0884
C to Z ↓	0.0183	0.0188	2.4036	1.8187
C to Z ↑	0.0181	0.0184	1.4743	1.1030
D to Z ↓	0.0165	0.0166	2.4114	1.8249
D to Z ↑	0.0151	0.0151	1.4973	1.1108

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P16	5.246e-06	1.000e-20
X12_P16	7.619e-06	1.000e-20
X18_P16	1.220e-05	1.000e-20
X24_P16	1.319e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	7.117e-04	1.219e-03	1.829e-03	2.205e-03
B (output stable)	5.996e-04	1.057e-03	1.497e-03	1.888e-03
C (output stable)	5.045e-05	1.616e-04	2.419e-04	3.456e-04
D (output stable)	1.226e-04	4.897e-04	5.847e-04	9.224e-04
A to Z	2.994e-03	5.763e-03	8.463e-03	1.110e-02
B to Z	2.715e-03	5.350e-03	7.588e-03	1.025e-02
C to Z	1.070e-03	2.215e-03	3.176e-03	4.430e-03
D to Z	8.634e-04	1.553e-03	2.383e-03	3.206e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

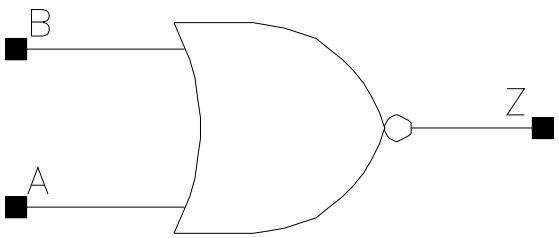
Pin Cycle (vdds)	X6_P16	X12_P16	X18_P16	X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.408	0.4896
X5_P16	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X10_P16	1.200	0.680	0.8160
X14_P16	1.200	0.680	0.8160
X17_P16	1.200	0.952	1.1424
X21_P16	1.200	0.952	1.1424
X24_P16	1.200	1.224	1.4688
X27_P16	1.200	1.224	1.4688
X34_P16	1.200	1.496	1.7952
X40_P16	1.200	1.360	1.6320
X41_P16	1.200	1.768	2.1216
X49_P16	1.200	1.496	1.7952
X53_P16	1.200	1.904	2.2848
X55_P16	1.200	2.312	2.7744
X57_P16	1.200	1.904	2.2848
X65_P16	1.200	2.040	2.4480
X84_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X3_P16	X5_P16	X7_P16	X10_P16
A	0.0006	0.0007	0.0009	0.0014
B	0.0006	0.0007	0.0009	0.0013
	X14_P16	X17_P16	X21_P16	X24_P16

A	0.0018	0.0023	0.0027	0.0031
B	0.0016	0.0021	0.0024	0.0029
	X27_P16	X34_P16	X40_P16	X41_P16
A	0.0034	0.0043	0.0010	0.0053
B	0.0032	0.0039	0.0011	0.0048
	X49_P16	X53_P16	X55_P16	X57_P16
A	0.0010	0.0011	0.0070	0.0011
B	0.0011	0.0010	0.0063	0.0010
	X65_P16	X84_P16		
A	0.0011	0.0012		
B	0.0010	0.0010		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	**X5_P16**	**X3_P16**	**X5_P16**
A to Z ↓	0.0125	0.0119	5.1588	3.6982
A to Z ↑	0.0222	0.0203	16.1241	11.6229
B to Z ↓	0.0111	0.0101	5.2488	3.7245
B to Z ↑	0.0215	0.0192	16.1952	11.6737
	X7_P16	**X10_P16**	**X7_P16**	**X10_P16**
A to Z ↓	0.0116	0.0121	2.6990	1.7637
A to Z ↑	0.0190	0.0222	8.1416	5.4479
B to Z ↓	0.0098	0.0090	2.7279	1.7805
B to Z ↑	0.0177	0.0165	8.1770	5.4765
	X14_P16	**X17_P16**	**X14_P16**	**X17_P16**
A to Z ↓	0.0118	0.0120	1.3339	1.0770
A to Z ↑	0.0205	0.0207	4.0101	3.2533
B to Z ↓	0.0087	0.0096	1.3469	1.0853
B to Z ↑	0.0155	0.0170	4.0323	3.2684
	X21_P16	**X24_P16**	**X21_P16**	**X24_P16**
A to Z ↓	0.0119	0.0118	0.9099	0.7778
A to Z ↑	0.0199	0.0203	2.6912	2.3485
B to Z ↓	0.0094	0.0090	0.9169	0.7849
B to Z ↑	0.0163	0.0160	2.7037	2.3606
	X27_P16	**X34_P16**	**X27_P16**	**X34_P16**
A to Z ↓	0.0117	0.0121	0.6879	0.5552
A to Z ↑	0.0196	0.0198	2.0554	1.6381
B to Z ↓	0.0089	0.0093	0.6946	0.5598
B to Z ↑	0.0156	0.0162	2.0650	1.6454
	X40_P16	**X41_P16**	**X40_P16**	**X41_P16**
A to Z ↓	0.0450	0.0119	0.5623	0.4626
A to Z ↑	0.0618	0.0197	0.8961	1.3580
B to Z ↓	0.0433	0.0090	0.5629	0.4670
B to Z ↑	0.0619	0.0156	0.8969	1.3649
	X49_P16	**X53_P16**	**X49_P16**	**X53_P16**
A to Z ↓	0.0475	0.0489	0.4692	0.4297
A to Z ↑	0.0639	0.0732	0.7462	0.6894
B to Z ↓	0.0457	0.0472	0.4689	0.4298
B to Z ↑	0.0639	0.0726	0.7468	0.6897
	X55_P16	**X57_P16**	**X55_P16**	**X57_P16**
A to Z ↓	0.0120	0.0493	0.3496	0.4035
A to Z ↑	0.0197	0.0734	1.0227	0.6406

B to Z ↓	0.0091	0.0476	0.3531	0.4027
B to Z ↑	0.0155	0.0728	1.0273	0.6409
	X65_P16	**X84_P16**	**X65_P16**	**X84_P16**
A to Z ↓	0.0507	0.0530	0.3541	0.2804
A to Z ↑	0.0743	0.0752	0.5615	0.4438
B to Z ↓	0.0489	0.0513	0.3541	0.2808
B to Z ↑	0.0738	0.0748	0.5618	0.4437

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	1.512e-06	1.000e-20
X5_P16	2.248e-06	1.000e-20
X7_P16	3.362e-06	1.000e-20
X10_P16	4.607e-06	1.000e-20
X14_P16	6.542e-06	1.000e-20
X17_P16	7.692e-06	1.000e-20
X21_P16	9.527e-06	1.000e-20
X24_P16	1.077e-05	1.000e-20
X27_P16	1.252e-05	1.000e-20
X34_P16	1.551e-05	1.000e-20
X40_P16	2.303e-05	1.000e-20
X41_P16	1.850e-05	1.000e-20
X49_P16	2.596e-05	1.000e-20
X53_P16	3.038e-05	1.000e-20
X55_P16	2.449e-05	1.000e-20
X57_P16	3.219e-05	1.000e-20
X65_P16	3.512e-05	1.000e-20
X84_P16	4.166e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	1.429e-05	1.958e-05	2.780e-05	8.795e-05
B (output stable)	2.163e-05	3.119e-05	4.506e-05	1.316e-04
A to Z	5.711e-04	7.040e-04	9.348e-04	1.658e-03
B to Z	4.292e-04	5.099e-04	6.621e-04	9.054e-04
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	1.031e-04	1.238e-04	1.382e-04	1.700e-04
B (output stable)	1.766e-04	1.929e-04	2.282e-04	2.694e-04
A to Z	2.054e-03	2.564e-03	2.954e-03	3.482e-03
B to Z	1.142e-03	1.579e-03	1.816e-03	2.039e-03
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	1.816e-04	2.207e-04	2.830e-05	2.851e-04
B (output stable)	3.070e-04	3.428e-04	4.520e-05	4.630e-04
A to Z	3.852e-03	4.847e-03	9.392e-03	5.821e-03
B to Z	2.259e-03	2.999e-03	9.127e-03	3.386e-03
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	2.827e-05	2.872e-05	3.715e-04	2.872e-05
B (output stable)	4.515e-05	4.782e-05	6.109e-04	4.782e-05
A to Z	1.068e-02	1.313e-02	7.700e-03	1.352e-02
B to Z	1.041e-02	1.284e-02	4.499e-03	1.323e-02
	X65_P16	X84_P16		

A (output stable)	2.879e-05	2.979e-05		
B (output stable)	4.782e-05	4.900e-05		
A to Z	1.466e-02	1.745e-02		
B to Z	1.437e-02	1.711e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

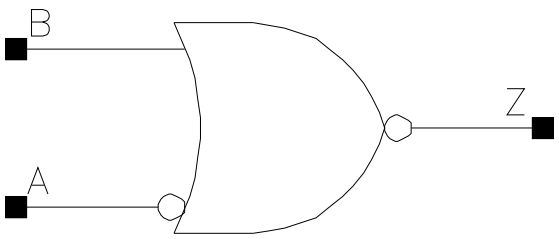
Pin Cycle (vdds)	X3_P16	X5_P16	X7_P16	X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P16	X17_P16	X21_P16	X24_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P16	X34_P16	X40_P16	X41_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X49_P16	X53_P16	X55_P16	X57_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X65_P16	X84_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X7_P16	1.200	0.680	0.8160
X13_P16	1.200	0.952	1.1424
X27_P16	1.200	1.632	1.9584
X41_P16	1.200	2.312	2.7744
X55_P16	1.200	2.992	3.5904

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X3_P16	X6_P16	X7_P16	X13_P16
A	0.0008	0.0008	0.0008	0.0012
B	0.0006	0.0009	0.0009	0.0016
	X27_P16	X41_P16	X55_P16	
A	0.0022	0.0033	0.0042	
B	0.0032	0.0048	0.0063	

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X6_P16	X3_P16	X6_P16
A to Z ↓	0.0339	0.0379	5.0512	3.2504
A to Z ↑	0.0328	0.0327	16.0170	8.1039
B to Z ↓	0.0114	0.0112	5.2386	3.3976
B to Z ↑	0.0217	0.0177	16.1731	8.1884

	X7_P16	X13_P16	X7_P16	X13_P16
A to Z ↓	0.0384	0.0339	2.5606	1.3884
A to Z ↑	0.0358	0.0333	7.9850	4.2096
B to Z ↓	0.0104	0.0093	2.6028	1.4040
B to Z ↑	0.0193	0.0170	8.0400	4.2456
	X27_P16	**X41_P16**	**X27_P16**	**X41_P16**
A to Z ↓	0.0327	0.0333	0.6684	0.4518
A to Z ↑	0.0320	0.0323	2.0228	1.3540
B to Z ↓	0.0091	0.0091	0.6948	0.4682
B to Z ↑	0.0161	0.0158	2.0406	1.3661
	X55_P16		**X55_P16**	
A to Z ↓	0.0329		0.3414	
A to Z ↑	0.0320		1.0202	
B to Z ↓	0.0091		0.3545	
B to Z ↑	0.0157		1.0292	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	2.796e-06	1.000e-20
X6_P16	4.432e-06	1.000e-20
X7_P16	5.089e-06	1.000e-20
X13_P16	9.612e-06	1.000e-20
X27_P16	1.872e-05	1.000e-20
X41_P16	2.744e-05	1.000e-20
X55_P16	3.615e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	8.643e-04	1.101e-03	1.179e-03	1.896e-03
B (output stable)	2.455e-05	4.543e-05	1.122e-04	2.068e-04
A to Z	1.497e-03	2.098e-03	2.455e-03	4.087e-03
B to Z	4.387e-04	6.462e-04	8.013e-04	1.257e-03
	X27_P16	X41_P16	X55_P16	
A (output stable)	3.710e-03	5.635e-03	7.382e-03	
B (output stable)	4.195e-04	6.010e-04	7.911e-04	
A to Z	8.106e-03	1.208e-02	1.593e-02	
B to Z	2.419e-03	3.530e-03	4.644e-03	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

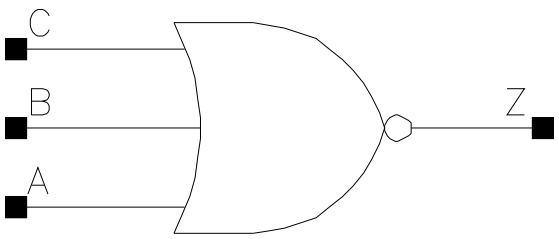
Pin Cycle (vdds)	X3_P16	X6_P16	X7_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P16	X41_P16	X55_P16	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	0.544	0.6528
X6_P16	1.200	0.544	0.6528
X9_P16	1.200	0.952	1.1424
X13_P16	1.200	0.952	1.1424
X16_P16	1.200	1.360	1.6320
X19_P16	1.200	1.496	1.7952
X22_P16	1.200	1.768	2.1216
X25_P16	1.200	1.904	2.2848
X37_P16	1.200	2.584	3.1008
X49_P16	1.200	3.400	4.0800

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X4_P16	X6_P16	X9_P16	X13_P16
A	0.0007	0.0009	0.0014	0.0017
B	0.0007	0.0009	0.0015	0.0018
C	0.0007	0.0009	0.0013	0.0016
	X16_P16	X19_P16	X22_P16	X25_P16
A	0.0023	0.0026	0.0031	0.0035
B	0.0023	0.0030	0.0032	0.0040
C	0.0020	0.0023	0.0028	0.0031
	X37_P16	X49_P16		
A	0.0052	0.0070		
B	0.0053	0.0071		

C	0.0046	0.0063		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0143	0.0137	3.7451	2.7367
A to Z ↑	0.0313	0.0285	16.9928	11.8843
B to Z ↓	0.0135	0.0129	3.7461	2.7379
B to Z ↑	0.0290	0.0261	17.0019	11.8930
C to Z ↓	0.0120	0.0111	3.7692	2.7629
C to Z ↑	0.0263	0.0230	17.0423	11.9180
	X9_P16	**X13_P16**	**X9_P16**	**X13_P16**
A to Z ↓	0.0140	0.0138	1.8146	1.3834
A to Z ↑	0.0316	0.0294	7.9440	5.8626
B to Z ↓	0.0134	0.0129	1.7750	1.3345
B to Z ↑	0.0310	0.0281	7.9491	5.8675
C to Z ↓	0.0104	0.0100	1.7846	1.3522
C to Z ↑	0.0213	0.0198	7.9595	5.8752
	X16_P16	**X19_P16**	**X16_P16**	**X19_P16**
A to Z ↓	0.0140	0.0137	1.0847	0.9078
A to Z ↑	0.0301	0.0295	4.7627	3.9207
B to Z ↓	0.0134	0.0133	1.0873	0.8914
B to Z ↑	0.0288	0.0290	4.7661	3.9241
C to Z ↓	0.0108	0.0105	1.0895	0.9230
C to Z ↑	0.0223	0.0209	4.7739	3.9299
	X22_P16	**X25_P16**	**X22_P16**	**X25_P16**
A to Z ↓	0.0138	0.0137	0.7915	0.6909
A to Z ↑	0.0297	0.0295	3.3937	2.9456
B to Z ↓	0.0132	0.0131	0.7798	0.6689
B to Z ↑	0.0285	0.0290	3.3967	2.9475
C to Z ↓	0.0102	0.0102	0.7854	0.6921
C to Z ↑	0.0206	0.0199	3.4026	2.9521
	X37_P16	**X49_P16**	**X37_P16**	**X49_P16**
A to Z ↓	0.0138	0.0139	0.4765	0.3600
A to Z ↑	0.0286	0.0287	1.9711	1.4829
B to Z ↓	0.0131	0.0132	0.4718	0.3568
B to Z ↑	0.0271	0.0270	1.9728	1.4841
C to Z ↓	0.0105	0.0107	0.4760	0.3601
C to Z ↑	0.0199	0.0203	1.9763	1.4871

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.800e-06	1.000e-20
X6_P16	2.739e-06	1.000e-20
X9_P16	3.760e-06	1.000e-20
X13_P16	5.429e-06	1.000e-20
X16_P16	6.366e-06	1.000e-20
X19_P16	8.219e-06	1.000e-20
X22_P16	8.973e-06	1.000e-20
X25_P16	1.081e-05	1.000e-20
X37_P16	1.567e-05	1.000e-20

X49_P16	2.081e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	2.359e-05	3.298e-05	5.948e-05	7.755e-05
B (output stable)	2.245e-06	5.885e-06	2.636e-05	3.318e-05
C (output stable)	3.057e-05	4.796e-05	1.090e-04	1.469e-04
A to Z	1.057e-03	1.357e-03	2.290e-03	2.850e-03
B to Z	8.535e-04	1.071e-03	1.918e-03	2.328e-03
C to Z	6.532e-04	7.857e-04	1.110e-03	1.367e-03
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	9.222e-05	1.118e-04	1.331e-04	1.541e-04
B (output stable)	2.938e-05	3.876e-05	4.975e-05	5.986e-05
C (output stable)	1.578e-04	2.077e-04	2.379e-04	2.881e-04
A to Z	3.606e-03	4.289e-03	4.983e-03	5.710e-03
B to Z	2.942e-03	3.548e-03	4.072e-03	4.736e-03
C to Z	1.934e-03	2.177e-03	2.473e-03	2.749e-03
	X37_P16	X49_P16		
A (output stable)	2.267e-04	2.992e-04		
B (output stable)	8.204e-05	1.057e-04		
C (output stable)	4.140e-04	5.435e-04		
A to Z	8.224e-03	1.095e-02		
B to Z	6.636e-03	8.809e-03		
C to Z	4.008e-03	5.424e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

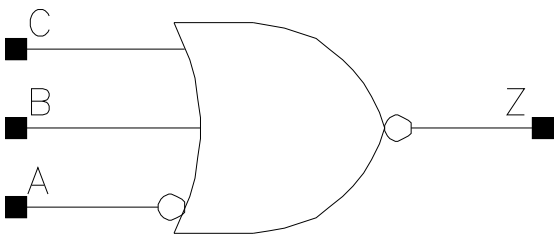
Pin Cycle (vdds)	X4_P16	X6_P16	X9_P16	X13_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P16	X19_P16	X22_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P16	X49_P16		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.680	0.8160
X13_P16	1.200	1.224	1.4688
X19_P16	1.200	1.496	1.7952
X25_P16	1.200	2.176	2.6112

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0009	0.0012	0.0012	0.0022
B	0.0009	0.0018	0.0026	0.0035
C	0.0009	0.0016	0.0023	0.0031

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X13_P16**	**X6_P16**	**X13_P16**
A to Z ↓	0.0382	0.0359	2.6837	1.4611
A to Z ↑	0.0429	0.0421	12.0069	5.8570
B to Z ↓	0.0131	0.0129	2.7527	1.3405
B to Z ↑	0.0264	0.0281	12.0357	5.8674
C to Z ↓	0.0113	0.0100	2.7670	1.3531
C to Z ↑	0.0236	0.0198	12.0612	5.8754
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0414	0.0356	0.9067	0.6860

A to Z ↑	0.0455	0.0417	3.9328	2.9495
B to Z ↓	0.0133	0.0130	0.9278	0.6920
B to Z ↑	0.0269	0.0271	3.9425	2.9557
C to Z ↓	0.0105	0.0101	0.9243	0.6956
C to Z ↑	0.0210	0.0199	3.9485	2.9610

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P16	4.075e-06	1.000e-20
X13_P16	8.811e-06	1.000e-20
X19_P16	1.100e-05	1.000e-20
X25_P16	1.697e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	1.141e-03	2.024e-03	2.697e-03	3.973e-03
B (output stable)	1.270e-05	5.056e-05	5.957e-05	9.063e-05
C (output stable)	5.596e-05	1.863e-04	2.277e-04	3.388e-04
A to Z	2.589e-03	5.151e-03	7.094e-03	9.919e-03
B to Z	1.082e-03	2.334e-03	3.304e-03	4.444e-03
C to Z	8.011e-04	1.369e-03	2.162e-03	2.709e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

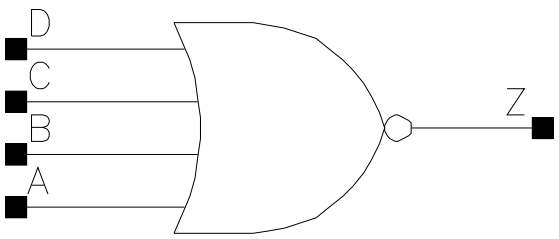
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X25_P16	1.200	1.904	2.2848
X32_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X32_P16
A	0.0007	0.0007	0.0008	0.0010
B	0.0007	0.0007	0.0009	0.0012
C	0.0007	0.0006	0.0008	0.0010
D	0.0007	0.0006	0.0009	0.0010

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0476	0.0464	2.6408	1.2972
A to Z ↑	0.0689	0.0736	4.4680	2.1902
B to Z ↓	0.0458	0.0452	2.6442	1.2972
B to Z ↑	0.0683	0.0733	4.4632	2.1897
C to Z ↓	0.0466	0.0462	2.6380	1.2951
C to Z ↑	0.0697	0.0754	4.4645	2.1900

D to Z ↓	0.0458	0.0455	2.6380	1.2931
D to Z ↑	0.0698	0.0758	4.4601	2.1902
	X25_P16	**X32_P16**	**X25_P16**	**X32_P16**
A to Z ↓	0.0478	0.0499	0.8968	0.7079
A to Z ↑	0.0719	0.0693	1.4886	1.1334
B to Z ↓	0.0465	0.0484	0.8976	0.7082
B to Z ↑	0.0720	0.0690	1.4887	1.1337
C to Z ↓	0.0462	0.0492	0.8942	0.7059
C to Z ↑	0.0717	0.0699	1.4877	1.1323
D to Z ↓	0.0447	0.0468	0.8942	0.7060
D to Z ↑	0.0715	0.0694	1.4874	1.1330

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	6.970e-06	1.000e-20
X17_P16	1.127e-05	1.000e-20
X25_P16	1.722e-05	1.000e-20
X32_P16	2.226e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	4.481e-04	5.599e-04	7.735e-04	9.801e-04
B (output stable)	3.895e-04	5.026e-04	6.972e-04	8.732e-04
C (output stable)	4.132e-04	5.016e-04	7.899e-04	1.013e-03
D (output stable)	3.566e-04	4.487e-04	7.093e-04	9.030e-04
A to Z	3.181e-03	4.847e-03	7.440e-03	9.312e-03
B to Z	3.033e-03	4.709e-03	7.232e-03	9.065e-03
C to Z	3.212e-03	4.826e-03	7.023e-03	8.828e-03
D to Z	3.060e-03	4.690e-03	6.830e-03	8.556e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

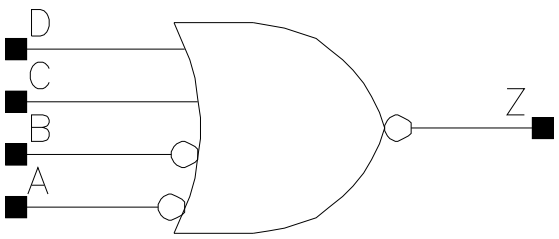
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X32_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X13_P16	1.200	1.496	1.7952
X19_P16	1.200	2.040	2.4480
X25_P16	1.200	2.448	2.9376

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X6_P16	X13_P16	X19_P16	X25_P16
A	0.0011	0.0011	0.0022	0.0021
B	0.0011	0.0016	0.0022	0.0022
C	0.0009	0.0017	0.0025	0.0034
D	0.0008	0.0016	0.0024	0.0031

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	X13_P16	X6_P16	X13_P16
A to Z ↓	0.0324	0.0411	2.6194	1.3065
A to Z ↑	0.0427	0.0534	11.5559	5.9258
B to Z ↓	0.0300	0.0392	2.6161	1.3048
B to Z ↑	0.0433	0.0545	11.5584	5.9283
C to Z ↓	0.0135	0.0129	2.7765	1.3370
C to Z ↑	0.0266	0.0280	11.5891	5.9391

D to Z ↓	0.0114	0.0101	2.7719	1.3487
D to Z ↑	0.0232	0.0203	11.6093	5.9466
	X19_P16	**X25_P16**	**X19_P16**	**X25_P16**
A to Z ↓	0.0358	0.0396	0.8942	0.6750
A to Z ↑	0.0478	0.0522	3.9334	2.9668
B to Z ↓	0.0327	0.0369	0.8931	0.6738
B to Z ↑	0.0477	0.0527	3.9346	2.9678
C to Z ↓	0.0133	0.0132	0.9285	0.6956
C to Z ↑	0.0268	0.0271	3.9424	2.9718
D to Z ↓	0.0105	0.0102	0.9246	0.6948
D to Z ↑	0.0210	0.0199	3.9481	2.9765

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P16	5.423e-06	1.000e-20
X13_P16	7.845e-06	1.000e-20
X19_P16	1.279e-05	1.000e-20
X25_P16	1.482e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	6.849e-04	1.182e-03	1.778e-03	2.167e-03
B (output stable)	6.063e-04	1.112e-03	1.617e-03	2.032e-03
C (output stable)	8.883e-06	4.894e-05	6.459e-05	1.068e-04
D (output stable)	6.322e-05	1.977e-04	2.540e-04	4.019e-04
A to Z	3.082e-03	5.907e-03	8.747e-03	1.136e-02
B to Z	2.879e-03	5.591e-03	8.095e-03	1.077e-02
C to Z	1.126e-03	2.314e-03	3.292e-03	4.423e-03
D to Z	8.300e-04	1.400e-03	2.162e-03	2.710e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

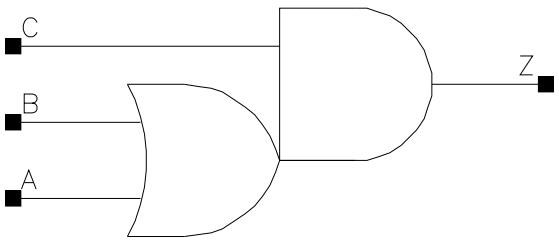
Pin Cycle (vdds)	X6_P16	X13_P16	X19_P16	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.680	0.8160
X17_P16	1.200	0.816	0.9792
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0010	0.0010	0.0019
B	0.0011	0.0011	0.0021
C	0.0011	0.0011	0.0021

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
A to Z ↓	0.0362	0.0423	2.7125	1.3495
A to Z ↑	0.0315	0.0349	4.4702	2.1935
B to Z ↓	0.0357	0.0421	2.7165	1.3508
B to Z ↑	0.0286	0.0322	4.4640	2.1894
C to Z ↓	0.0323	0.0358	2.6870	1.3273
C to Z ↑	0.0300	0.0330	4.4644	2.1893
	X33_P16		**X33_P16**	
A to Z ↓	0.0442		0.6852	
A to Z ↑	0.0373		1.1015	

B to Z ↓	0.0441		0.6853	
B to Z ↑	0.0342		1.0997	
C to Z ↓	0.0366		0.6713	
C to Z ↑	0.0341		1.0994	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	6.865e-06	1.000e-20
X17_P16	1.004e-05	1.000e-20
X33_P16	2.006e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	7.419e-05	7.565e-05	1.538e-04
B (output stable)	8.445e-05	8.544e-05	1.643e-04
C (output stable)	4.886e-05	5.079e-05	9.502e-05
A to Z	2.369e-03	3.514e-03	7.420e-03
B to Z	2.087e-03	3.223e-03	6.855e-03
C to Z	2.600e-03	3.678e-03	7.624e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

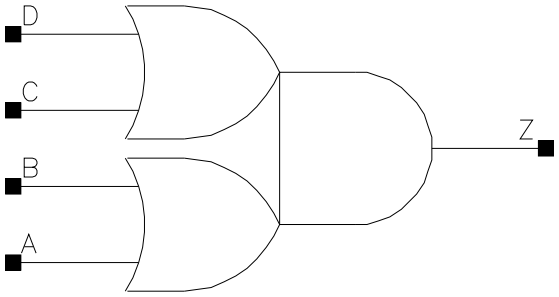
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X17_P16	1.200	1.088	1.3056
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0006	0.0010	0.0020
B	0.0007	0.0011	0.0020
C	0.0007	0.0011	0.0020
D	0.0007	0.0010	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0636	0.0529	2.6539	1.3409
A to Z ↑	0.0439	0.0380	4.3838	2.1899
B to Z ↓	0.0639	0.0527	2.6536	1.3411
B to Z ↑	0.0421	0.0358	4.3775	2.1874

C to Z ↓	0.0551	0.0461	2.6320	1.3335
C to Z ↑	0.0420	0.0374	4.3809	2.1888
D to Z ↓	0.0543	0.0454	2.6321	1.3335
D to Z ↑	0.0395	0.0344	4.3775	2.1859
	X33_P16		**X33_P16**	
A to Z ↓	0.0539		0.6908	
A to Z ↑	0.0382		1.0997	
B to Z ↓	0.0515		0.6909	
B to Z ↑	0.0353		1.0969	
C to Z ↓	0.0466		0.6860	
C to Z ↑	0.0370		1.0989	
D to Z ↓	0.0436		0.6867	
D to Z ↑	0.0336		1.0967	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	5.499e-06	1.000e-20
X17_P16	1.141e-05	1.000e-20
X33_P16	2.179e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.653e-05	2.759e-05	8.375e-05
B (output stable)	1.981e-05	3.698e-05	1.335e-04
C (output stable)	6.299e-05	8.089e-05	1.864e-04
D (output stable)	6.657e-05	8.986e-05	2.413e-04
A to Z	2.832e-03	4.564e-03	9.111e-03
B to Z	2.685e-03	4.258e-03	8.261e-03
C to Z	2.440e-03	3.984e-03	7.963e-03
D to Z	2.286e-03	3.688e-03	7.067e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

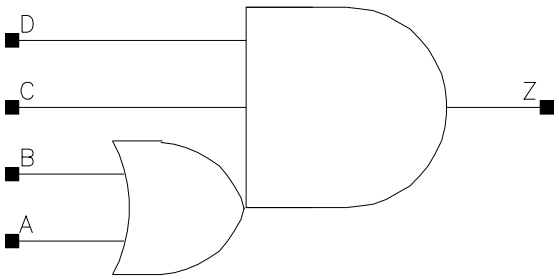
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X17_P16	1.200	1.088	1.3056
X25_P16	1.200	1.904	2.2848
X33_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X8_P16	X17_P16	X25_P16	X33_P16
A	0.0006	0.0010	0.0016	0.0019
B	0.0006	0.0010	0.0016	0.0020
C	0.0007	0.0011	0.0017	0.0021
D	0.0007	0.0011	0.0017	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0535	0.0503	2.7831	1.3565
A to Z ↑	0.0515	0.0483	4.5512	2.2067
B to Z ↓	0.0536	0.0485	2.7823	1.3576
B to Z ↑	0.0484	0.0437	4.5445	2.2009
C to Z ↓	0.0439	0.0407	2.7137	1.3295

C to Z ↑	0.0493	0.0457	4.5396	2.2004
D to Z ↓	0.0426	0.0393	2.7124	1.3276
D to Z ↑	0.0504	0.0466	4.5400	2.1994
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**
A to Z ↓	0.0521	0.0496	0.9166	0.6884
A to Z ↑	0.0485	0.0488	1.4896	1.1166
B to Z ↓	0.0498	0.0476	0.9175	0.6886
B to Z ↑	0.0443	0.0444	1.4854	1.1133
C to Z ↓	0.0425	0.0403	0.8994	0.6744
C to Z ↑	0.0465	0.0459	1.4849	1.1132
D to Z ↓	0.0403	0.0385	0.8971	0.6728
D to Z ↑	0.0460	0.0458	1.4841	1.1131

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	4.562e-06	1.000e-20
X17_P16	9.732e-06	1.000e-20
X25_P16	1.477e-05	1.000e-20
X33_P16	1.942e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	6.765e-05	1.313e-04	2.185e-04	2.362e-04
B (output stable)	6.887e-05	1.366e-04	2.306e-04	2.490e-04
C (output stable)	1.254e-05	2.679e-05	6.892e-05	7.614e-05
D (output stable)	2.830e-05	5.849e-05	2.055e-04	2.165e-04
A to Z	2.354e-03	4.281e-03	6.800e-03	8.429e-03
B to Z	2.211e-03	3.887e-03	6.152e-03	7.615e-03
C to Z	2.526e-03	4.533e-03	7.362e-03	8.914e-03
D to Z	2.418e-03	4.325e-03	6.827e-03	8.368e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

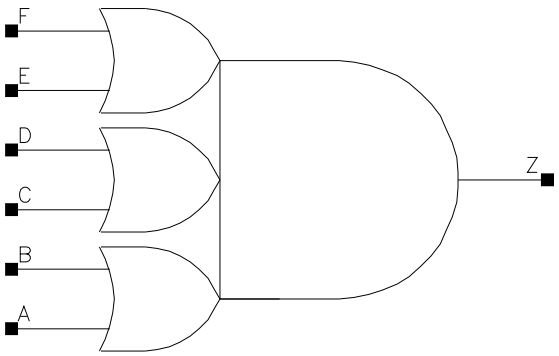
Pin Cycle (vdds)	X8_P16	X17_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	1.224	1.4688
X17_P16	1.200	1.360	1.6320
X33_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
A	0.0007	0.0010	0.0018
B	0.0006	0.0010	0.0019
C	0.0007	0.0010	0.0018
D	0.0006	0.0010	0.0019
E	0.0007	0.0010	0.0018
F	0.0006	0.0010	0.0019

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	X17_P16	X8_P16	X17_P16
A to Z ↓	0.0727	0.0618	2.8453	1.3817
A to Z ↑	0.0573	0.0522	4.5272	2.2160
B to Z ↓	0.0724	0.0619	2.8463	1.3819
B to Z ↑	0.0549	0.0499	4.5263	2.2144
C to Z ↓	0.0667	0.0579	2.8280	1.3777
C to Z ↑	0.0569	0.0512	4.5313	2.2161
D to Z ↓	0.0669	0.0579	2.8274	1.3780
D to Z ↑	0.0542	0.0485	4.5256	2.2132
E to Z ↓	0.0577	0.0507	2.8043	1.3701
E to Z ↑	0.0523	0.0480	4.5267	2.2144
F to Z ↓	0.0582	0.0505	2.8052	1.3698
F to Z ↑	0.0498	0.0451	4.5200	2.2115
	X33_P16		X33_P16	
A to Z ↓	0.0621		0.7040	
A to Z ↑	0.0533		1.1174	
B to Z ↓	0.0625		0.7041	
B to Z ↑	0.0500		1.1144	
C to Z ↓	0.0570		0.6993	
C to Z ↑	0.0522		1.1166	
D to Z ↓	0.0572		0.6997	
D to Z ↑	0.0490		1.1134	
E to Z ↓	0.0500		0.6956	
E to Z ↑	0.0490		1.1154	
F to Z ↓	0.0501		0.6956	
F to Z ↑	0.0456		1.1126	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	5.652e-06	1.000e-20
X17_P16	1.195e-05	1.000e-20
X33_P16	2.280e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X17_P16	X33_P16
A (output stable)	1.447e-05	2.588e-05	4.855e-05
B (output stable)	1.686e-05	3.514e-05	6.271e-05
C (output stable)	3.264e-05	5.264e-05	1.076e-04
D (output stable)	3.621e-05	6.012e-05	1.216e-04
E (output stable)	1.101e-04	1.602e-04	3.055e-04
F (output stable)	1.097e-04	1.636e-04	3.174e-04
A to Z	3.262e-03	5.483e-03	1.073e-02
B to Z	3.104e-03	5.196e-03	1.018e-02
C to Z	2.967e-03	5.035e-03	9.789e-03
D to Z	2.820e-03	4.744e-03	9.233e-03
E to Z	2.590e-03	4.465e-03	8.685e-03
F to Z	2.455e-03	4.187e-03	8.155e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

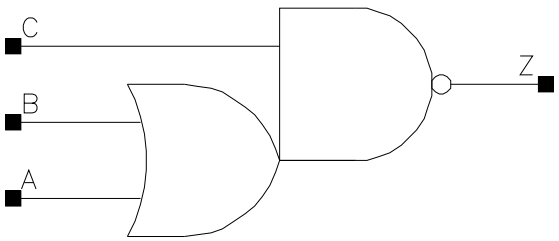
Pin Cycle (vdds)	X8_P16	X17_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.544	0.6528
X17_P16	1.200	1.360	1.6320
X34_P16	1.200	2.720	3.2640
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X6_P16	X17_P16	X34_P16	X46_P16
A	0.0008	0.0025	0.0051	0.0066
B	0.0008	0.0023	0.0045	0.0060
C	0.0009	0.0026	0.0053	0.0069

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X17_P16**	**X6_P16**	**X17_P16**
A to Z ↓	0.0164	0.0172	5.0710	1.6602
A to Z ↑	0.0200	0.0217	8.1406	2.7275
B to Z ↓	0.0134	0.0139	5.0078	1.6750
B to Z ↑	0.0187	0.0187	8.1723	2.7407
C to Z ↓	0.0158	0.0160	4.6268	1.5272
C to Z ↑	0.0193	0.0191	4.4782	1.4755
	X34_P16	**X46_P16**	**X34_P16**	**X46_P16**
A to Z ↓	0.0178	0.0177	0.8439	0.6420

A to Z ↑	0.0225	0.0220	1.3610	1.0379
B to Z ↓	0.0142	0.0142	0.8529	0.6504
B to Z ↑	0.0190	0.0190	1.3672	1.0437
C to Z ↓	0.0165	0.0163	0.7772	0.5917
C to Z ↑	0.0195	0.0193	0.7374	0.5599

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P16	3.991e-06	1.000e-20
X17_P16	1.155e-05	1.000e-20
X34_P16	2.300e-05	1.000e-20
X46_P16	3.030e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	6.381e-05	2.222e-04	4.747e-04	5.773e-04
B (output stable)	7.441e-05	2.438e-04	5.474e-04	6.595e-04
C (output stable)	4.384e-05	1.486e-04	3.095e-04	3.916e-04
A to Z	1.012e-03	3.334e-03	6.996e-03	8.955e-03
B to Z	7.343e-04	2.233e-03	4.624e-03	6.011e-03
C to Z	1.244e-03	3.830e-03	7.965e-03	1.026e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

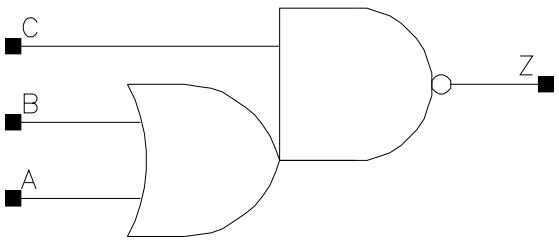
Pin Cycle (vdds)	X6_P16	X17_P16	X34_P16	X46_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.544	0.6528
X11_P16	1.200	0.952	1.1424
X17_P16	1.200	1.360	1.6320
X23_P16	1.200	1.904	2.2848
X46_P16	1.200	3.536	4.2432

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X5_P16	X11_P16	X17_P16	X23_P16
A	0.0009	0.0017	0.0027	0.0036
B	0.0008	0.0018	0.0025	0.0033
C	0.0008	0.0016	0.0024	0.0032
	X46_P16			
A	0.0072			
B	0.0065			
C	0.0065			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X11_P16	X5_P16	X11_P16
A to Z ↓	0.0176	0.0177	5.1779	2.4196
A to Z ↑	0.0257	0.0256	8.5688	4.0208
B to Z ↓	0.0150	0.0151	5.1172	2.3703

B to Z ↑	0.0247	0.0246	8.5948	4.0351
C to Z ↓	0.0136	0.0136	4.8086	2.2355
C to Z ↑	0.0145	0.0144	4.7680	2.2320
	X17_P16	**X23_P16**	**X17_P16**	**X23_P16**
A to Z ↓	0.0170	0.0180	1.6675	1.2347
A to Z ↑	0.0243	0.0270	2.6696	2.0254
B to Z ↓	0.0143	0.0149	1.6644	1.2344
B to Z ↑	0.0230	0.0239	2.6779	2.0332
C to Z ↓	0.0131	0.0134	1.5561	1.1499
C to Z ↑	0.0133	0.0138	1.4856	1.1259
	X46_P16		**X46_P16**	
A to Z ↓	0.0178		0.6391	
A to Z ↑	0.0264		1.0199	
B to Z ↓	0.0146		0.6346	
B to Z ↑	0.0234		1.0244	
C to Z ↓	0.0134		0.5942	
C to Z ↑	0.0134		0.5672	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	3.835e-06	1.000e-20
X11_P16	7.969e-06	1.000e-20
X17_P16	1.169e-05	1.000e-20
X23_P16	1.585e-05	1.000e-20
X46_P16	3.056e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	1.755e-05	3.804e-05	5.522e-05	1.054e-04
B (output stable)	2.150e-05	5.018e-05	7.102e-05	1.433e-04
C (output stable)	1.823e-04	4.525e-04	5.167e-04	8.637e-04
A to Z	1.343e-03	2.858e-03	3.966e-03	6.011e-03
B to Z	1.046e-03	2.248e-03	3.004e-03	4.309e-03
C to Z	7.567e-04	1.654e-03	2.234e-03	3.259e-03
	X46_P16			
A (output stable)	2.003e-04			
B (output stable)	2.710e-04			
C (output stable)	1.534e-03			
A to Z	1.155e-02			
B to Z	8.181e-03			
C to Z	6.227e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X5_P16	X11_P16	X17_P16	X23_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

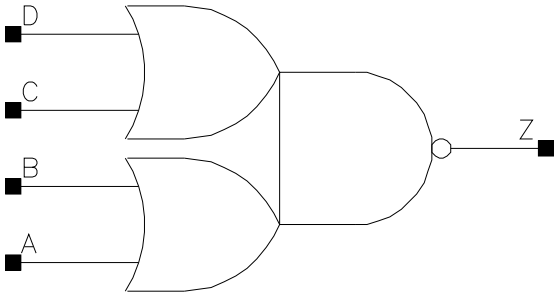
	X46_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.680	0.8160
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.448	2.9376
X42_P16	1.200	4.624	5.5488

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0009	0.0018	0.0026	0.0036
B	0.0009	0.0016	0.0023	0.0032
C	0.0008	0.0017	0.0025	0.0034
D	0.0008	0.0015	0.0022	0.0031
	X42_P16			
A	0.0073			
B	0.0065			
C	0.0068			
D	0.0061			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	**X10_P16**	**X5_P16**	**X10_P16**
A to Z ↓	0.0192	0.0206	4.6971	2.3578
A to Z ↑	0.0299	0.0304	8.9627	4.1181
B to Z ↓	0.0169	0.0177	4.6293	2.3614
B to Z ↑	0.0286	0.0271	8.9786	4.1337
C to Z ↓	0.0168	0.0184	4.7481	2.3713
C to Z ↑	0.0213	0.0234	8.8134	4.1277
D to Z ↓	0.0141	0.0147	4.6676	2.3814
D to Z ↑	0.0198	0.0187	8.8410	4.1503
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0197	0.0200	1.6121	1.1558
A to Z ↑	0.0286	0.0295	2.7647	2.0311
B to Z ↓	0.0172	0.0171	1.6196	1.1547
B to Z ↑	0.0261	0.0266	2.7738	2.0376
C to Z ↓	0.0179	0.0180	1.6206	1.1626
C to Z ↑	0.0218	0.0223	2.7717	2.0326
D to Z ↓	0.0147	0.0145	1.6406	1.1663
D to Z ↑	0.0183	0.0184	2.7856	2.0439
	X42_P16		**X42_P16**	
A to Z ↓	0.0203		0.6000	
A to Z ↑	0.0295		1.0289	
B to Z ↓	0.0173		0.5954	
B to Z ↑	0.0267		1.0323	
C to Z ↓	0.0186		0.6055	
C to Z ↑	0.0225		1.0256	
D to Z ↓	0.0149		0.6019	
D to Z ↑	0.0187		1.0309	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	4.612e-06	1.000e-20
X10_P16	9.691e-06	1.000e-20
X15_P16	1.382e-05	1.000e-20
X21_P16	1.914e-05	1.000e-20
X42_P16	3.742e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	2.415e-05	8.155e-05	1.053e-04	1.541e-04
B (output stable)	3.394e-05	1.289e-04	1.566e-04	2.287e-04
C (output stable)	6.523e-05	1.760e-04	2.231e-04	3.212e-04
D (output stable)	7.702e-05	2.247e-04	2.729e-04	3.945e-04
A to Z	1.627e-03	3.716e-03	5.115e-03	7.220e-03
B to Z	1.341e-03	2.842e-03	3.924e-03	5.543e-03
C to Z	1.096e-03	2.684e-03	3.628e-03	5.114e-03
D to Z	8.354e-04	1.787e-03	2.487e-03	3.472e-03
	X42_P16			
A (output stable)	3.013e-04			
B (output stable)	4.483e-04			
C (output stable)	6.270e-04			
D (output stable)	7.827e-04			

A to Z	1.430e-02			
B to Z	1.095e-02			
C to Z	1.020e-02			
D to Z	6.972e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

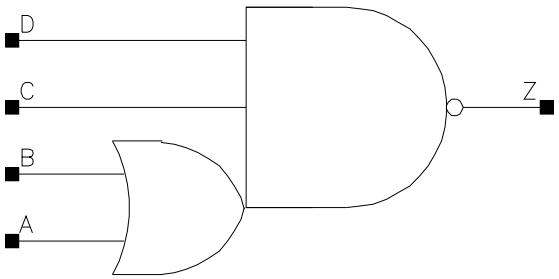
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X42_P16			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X21_P16	1.200	2.448	2.9376
X31_P16	1.200	3.536	4.2432

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X21_P16	X31_P16
A	0.0009	0.0016	0.0033	0.0049
B	0.0010	0.0015	0.0029	0.0044
C	0.0009	0.0018	0.0035	0.0052
D	0.0009	0.0017	0.0033	0.0049

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0241	0.0228	6.6960	3.5246
A to Z ↑	0.0275	0.0252	8.0600	4.0568
B to Z ↓	0.0208	0.0181	6.7214	3.5372
B to Z ↑	0.0257	0.0216	8.1154	4.0772
C to Z ↓	0.0225	0.0232	6.3211	3.3300

C to Z ↑	0.0236	0.0231	4.3533	2.1899
D to Z ↓	0.0233	0.0222	6.3369	3.3390
D to Z ↑	0.0224	0.0209	4.3885	2.1917
	X21_P16	**X31_P16**	**X21_P16**	**X31_P16**
A to Z ↓	0.0231	0.0233	1.8268	1.2363
A to Z ↑	0.0247	0.0246	2.0289	1.3586
B to Z ↓	0.0182	0.0184	1.8350	1.2447
B to Z ↑	0.0211	0.0212	2.0379	1.3658
C to Z ↓	0.0230	0.0230	1.7274	1.1701
C to Z ↑	0.0226	0.0226	1.1052	0.7425
D to Z ↓	0.0222	0.0224	1.7318	1.1730
D to Z ↑	0.0206	0.0206	1.1059	0.7419

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	3.619e-06	1.000e-20
X10_P16	6.877e-06	1.000e-20
X21_P16	1.306e-05	1.000e-20
X31_P16	1.926e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	1.256e-04	2.695e-04	4.996e-04	7.316e-04
B (output stable)	1.284e-04	2.806e-04	5.171e-04	7.614e-04
C (output stable)	2.550e-05	7.785e-05	1.489e-04	2.209e-04
D (output stable)	5.365e-05	2.228e-04	4.000e-04	5.831e-04
A to Z	1.584e-03	2.762e-03	5.354e-03	7.959e-03
B to Z	1.164e-03	1.895e-03	3.645e-03	5.472e-03
C to Z	1.897e-03	3.677e-03	7.030e-03	1.042e-02
D to Z	1.700e-03	3.035e-03	5.837e-03	8.686e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

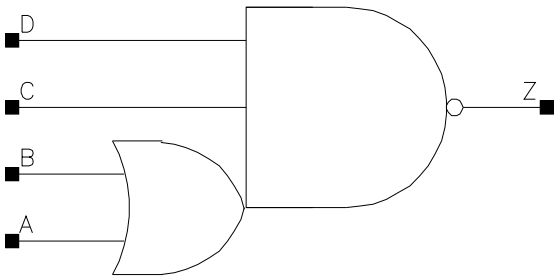
Pin Cycle (vdds)	X5_P16	X10_P16	X21_P16	X31_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P16	1.200	0.816	0.9792
X10_P16	1.200	1.360	1.6320
X15_P16	1.200	1.768	2.1216
X21_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P16	X10_P16	X15_P16	X21_P16
A	0.0010	0.0019	0.0028	0.0037
B	0.0009	0.0017	0.0024	0.0033
C	0.0009	0.0017	0.0025	0.0033
D	0.0008	0.0016	0.0024	0.0032

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P16	X10_P16	X5_P16	X10_P16
A to Z ↓	0.0235	0.0254	6.8139	3.5176
A to Z ↑	0.0298	0.0327	7.9166	4.0123
B to Z ↓	0.0203	0.0213	6.7417	3.5209
B to Z ↑	0.0290	0.0298	7.9374	4.0263
C to Z ↓	0.0180	0.0204	6.4376	3.3402

C to Z ↑	0.0183	0.0194	4.4020	2.2232
D to Z ↓	0.0178	0.0187	6.4615	3.3527
D to Z ↑	0.0160	0.0163	4.4262	2.2366
	X15_P16	**X21_P16**	**X15_P16**	**X21_P16**
A to Z ↓	0.0249	0.0252	2.4139	1.8153
A to Z ↑	0.0313	0.0321	2.6964	2.0390
B to Z ↓	0.0211	0.0211	2.4119	1.8135
B to Z ↑	0.0290	0.0296	2.7053	2.0440
C to Z ↓	0.0198	0.0202	2.2887	1.7211
C to Z ↑	0.0186	0.0190	1.4814	1.1143
D to Z ↓	0.0183	0.0188	2.2974	1.7274
D to Z ↑	0.0156	0.0160	1.4905	1.1211

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X5_P16	3.531e-06	1.000e-20
X10_P16	6.961e-06	1.000e-20
X15_P16	9.780e-06	1.000e-20
X21_P16	1.336e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	1.570e-05	3.494e-05	5.165e-05	6.662e-05
B (output stable)	1.673e-05	4.541e-05	6.187e-05	8.304e-05
C (output stable)	5.662e-05	1.234e-04	1.921e-04	2.449e-04
D (output stable)	1.099e-04	4.048e-04	4.701e-04	7.143e-04
A to Z	1.840e-03	4.054e-03	5.730e-03	7.838e-03
B to Z	1.513e-03	3.145e-03	4.455e-03	6.075e-03
C to Z	1.169e-03	2.670e-03	3.693e-03	5.135e-03
D to Z	9.613e-04	2.068e-03	2.879e-03	3.984e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

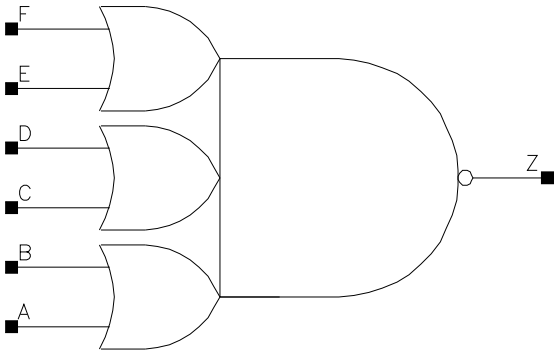
Pin Cycle (vdds)	X5_P16	X10_P16	X15_P16	X21_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P16	1.200	1.088	1.3056
X9_P16	1.200	2.040	2.4480

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X3_P16	X9_P16
A	0.0008	0.0019
B	0.0007	0.0017
C	0.0007	0.0018
D	0.0007	0.0016
E	0.0007	0.0017
F	0.0007	0.0015

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P16	X9_P16	X3_P16	X9_P16
A to Z ↓	0.0297	0.0314	7.8679	3.1760
A to Z ↑	0.0408	0.0390	11.2318	4.0380
B to Z ↓	0.0276	0.0277	7.9146	3.1795
B to Z ↑	0.0409	0.0363	11.2523	4.0468
C to Z ↓	0.0281	0.0292	7.9133	3.1861
C to Z ↑	0.0351	0.0335	11.2403	4.0284
D to Z ↓	0.0257	0.0254	7.9519	3.1924
D to Z ↑	0.0350	0.0307	11.2666	4.0395
E to Z ↓	0.0237	0.0251	7.9441	3.1876
E to Z ↑	0.0269	0.0262	11.2690	4.0328
F to Z ↓	0.0214	0.0208	7.9822	3.1933
F to Z ↑	0.0266	0.0223	11.3100	4.0500

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X3_P16	4.091e-06	1.000e-20
X9_P16	1.156e-05	1.000e-20

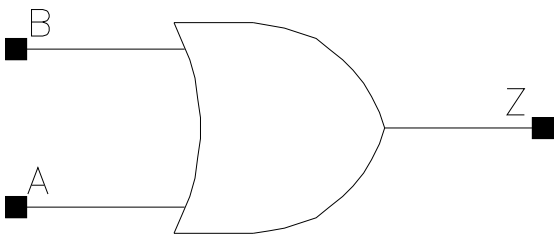
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X3_P16	X9_P16
A (output stable)	2.015e-05	7.512e-05
B (output stable)	2.436e-05	1.059e-04
C (output stable)	4.684e-05	1.379e-04
D (output stable)	5.038e-05	1.706e-04
E (output stable)	1.427e-04	3.529e-04
F (output stable)	1.485e-04	3.794e-04
A to Z	2.125e-03	5.645e-03
B to Z	1.913e-03	4.761e-03
C to Z	1.721e-03	4.561e-03
D to Z	1.516e-03	3.747e-03
E to Z	1.239e-03	3.452e-03
F to Z	1.048e-03	2.587e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X3_P16	X9_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00

OR2

Cell Description	Logical Symbol
2 input OR	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.544	0.6528
X16_P16	1.200	0.680	0.8160
X33_P16	1.200	1.360	1.6320
X50_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X8_P16	X16_P16	X33_P16	X50_P16
A	0.0008	0.0010	0.0020	0.0020
B	0.0007	0.0010	0.0020	0.0020

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0489	0.0427	2.7256	1.3759
A to Z ↑	0.0299	0.0309	4.4330	2.2282
B to Z ↓	0.0479	0.0419	2.7253	1.3751
B to Z ↑	0.0283	0.0288	4.4312	2.2247
	X33_P16	**X50_P16**	**X33_P16**	**X50_P16**
A to Z ↓	0.0442	0.0516	0.6785	0.4656
A to Z ↑	0.0308	0.0303	1.0869	0.7306
B to Z ↓	0.0414	0.0492	0.6779	0.4659
B to Z ↑	0.0281	0.0282	1.0845	0.7297

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	4.536e-06	1.000e-20
X16_P16	8.600e-06	1.000e-20
X33_P16	1.739e-05	1.000e-20
X50_P16	2.288e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	1.505e-05	2.861e-05	1.049e-04	9.542e-05
B (output stable)	2.382e-05	4.688e-05	1.879e-04	1.775e-04
A to Z	2.125e-03	3.463e-03	7.278e-03	9.842e-03
B to Z	1.968e-03	3.176e-03	6.399e-03	9.005e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

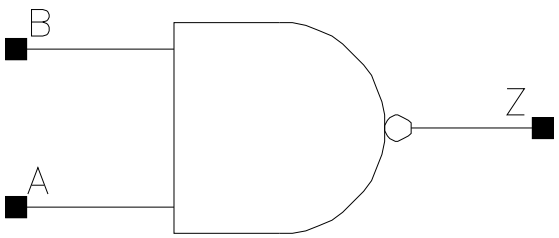
Pin Cycle (vdds)	X8_P16	X16_P16	X33_P16	X50_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.816	0.9792
X16_P16	1.200	0.952	1.1424
X24_P16	1.200	1.088	1.3056
X32_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P16	X16_P16	X24_P16	X32_P16
A	0.0010	0.0011	0.0011	0.0010
B	0.0011	0.0012	0.0012	0.0011

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0415	0.0437	2.6406	1.3698
A to Z ↑	0.0432	0.0444	4.4521	2.2606
B to Z ↓	0.0429	0.0452	2.6417	1.3694
B to Z ↑	0.0411	0.0419	4.4495	2.2570
	X24_P16	**X32_P16**	**X24_P16**	**X32_P16**
A to Z ↓	0.0487	0.0495	0.9278	0.6990
A to Z ↑	0.0479	0.0493	1.5097	1.1278
B to Z ↓	0.0502	0.0512	0.9271	0.6994
B to Z ↑	0.0453	0.0474	1.5075	1.1288

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	9.530e-06	1.000e-20
X16_P16	1.221e-05	1.000e-20
X24_P16	1.472e-05	1.000e-20
X32_P16	1.916e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	1.583e-05	1.592e-05	1.606e-05	1.698e-05
B (output stable)	3.182e-05	3.199e-05	3.213e-05	3.104e-05
A to Z	4.026e-03	4.736e-03	6.023e-03	7.972e-03
B to Z	3.838e-03	4.560e-03	5.856e-03	7.793e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

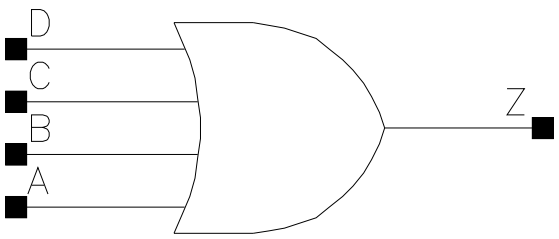
Pin Cycle (vdds)	X8_P16	X16_P16	X24_P16	X32_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P16	1.200	2.176	2.6112
X27_P16	1.200	2.584	3.1008

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P16	X27_P16
A	0.0018	0.0021
B	0.0016	0.0020
C	0.0018	0.0021
D	0.0016	0.0021

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P16	X27_P16	X20_P16	X27_P16
A to Z ↓	0.0492	0.0514	1.6557	1.2381
A to Z ↑	0.0321	0.0312	1.4523	1.0850
B to Z ↓	0.0469	0.0483	1.6563	1.2388
B to Z ↑	0.0301	0.0288	1.4509	1.0840
C to Z ↓	0.0476	0.0498	1.6517	1.2365
C to Z ↑	0.0305	0.0301	1.4548	1.0871
D to Z ↓	0.0452	0.0473	1.6523	1.2368
D to Z ↑	0.0284	0.0280	1.4528	1.0872

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X20_P16	1.405e-05	1.000e-20
X27_P16	2.047e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X20_P16	X27_P16
A (output stable)	1.575e-03	2.203e-03
B (output stable)	1.340e-03	1.858e-03
C (output stable)	1.419e-03	2.068e-03
D (output stable)	1.178e-03	1.761e-03
A to Z	6.638e-03	9.363e-03
B to Z	6.036e-03	8.430e-03
C to Z	5.839e-03	8.150e-03
D to Z	5.232e-03	7.332e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

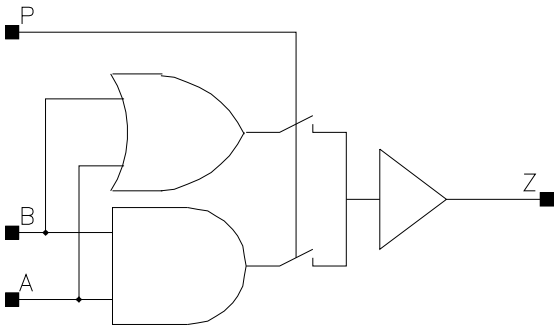
Pin Cycle (vdds)	X20_P16	X27_P16
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	0.952	1.1424
X16_P16	1.200	1.224	1.4688
X25_P16	1.200	2.040	2.4480
X33_P16	1.200	2.176	2.6112

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X8_P16	X16_P16	X25_P16	X33_P16
A	0.0013	0.0019	0.0034	0.0034
B	0.0012	0.0018	0.0037	0.0037
P	0.0007	0.0010	0.0019	0.0018

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0599	0.0533	2.7855	1.3588
A to Z ↑	0.0411	0.0380	4.4897	2.2436
B to Z ↓	0.0594	0.0530	2.7986	1.3672
B to Z ↑	0.0423	0.0391	4.4916	2.2479
P to Z ↓	0.0535	0.0482	2.7985	1.3665
P to Z ↑	0.0402	0.0373	4.4891	2.2434
	X25_P16	**X33_P16**	**X25_P16**	**X33_P16**

A to Z ↓	0.0508	0.0548	0.9217	0.6992
A to Z ↑	0.0375	0.0398	1.5054	1.1287
B to Z ↓	0.0502	0.0538	0.9266	0.7024
B to Z ↑	0.0388	0.0408	1.5047	1.1297
P to Z ↓	0.0467	0.0504	0.9274	0.7024
P to Z ↑	0.0367	0.0389	1.5030	1.1278

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	5.133e-06	1.000e-20
X16_P16	1.100e-05	1.000e-20
X25_P16	1.834e-05	1.000e-20
X33_P16	2.113e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	3.183e-05	5.237e-05	1.179e-04	1.177e-04
B (output stable)	4.036e-05	7.583e-05	2.070e-04	2.091e-04
P (output stable)	1.199e-04	2.197e-04	3.656e-04	3.755e-04
A to Z	2.477e-03	4.223e-03	7.263e-03	8.560e-03
B to Z	2.410e-03	4.112e-03	6.973e-03	8.285e-03
P to Z	2.171e-03	3.761e-03	6.491e-03	7.781e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

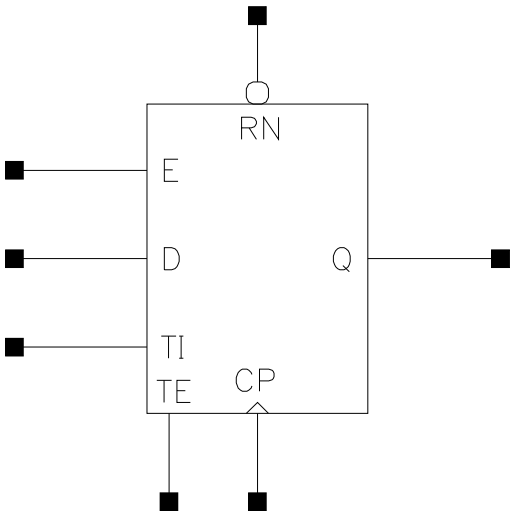
Pin Cycle (vdds)	X8_P16	X16_P16	X25_P16	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.488	5.3856
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0007	0.0007	0.0007
E	0.0009	0.0011	0.0011	0.0011
RN	0.0008	0.0007	0.0007	0.0008
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to Q ↓	0.1190	0.0592	6.1489	2.6997
CP to Q ↑	0.0938	0.0788	9.2290	4.4296
RN to Q ↓	0.0966	0.0833	5.2811	2.8591
	X17_P16	X33_P16	X17_P16	X33_P16
CP to Q ↓	0.1045	0.1106	1.3124	0.6878
CP to Q ↑	0.1301	0.1369	2.1733	1.1040
RN to Q ↓	0.1404	0.1462	1.3112	0.6855

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1618	0.1084	0.1084	0.1084
CP ↑	min_pulse_width to CP	0.1115	0.0486	0.0439	0.0439
D ↓	hold_rising to CP	-0.1700	-0.0853	-0.0849	-0.0875
D ↑	hold_rising to CP	-0.1043	-0.0387	-0.0413	-0.0413
D ↓	setup_rising to CP	0.2292	0.1443	0.1443	0.1443
D ↑	setup_rising to CP	0.1438	0.0791	0.0758	0.0763
E ↓	hold_rising to CP	-0.1190	-0.1212	-0.1206	-0.1206
E ↑	hold_rising to CP	-0.1021	-0.0413	-0.0413	-0.0413
E ↓	setup_rising to CP	0.2049	0.2004	0.2004	0.1999
E ↑	setup_rising to CP	0.2234	0.1518	0.1546	0.1550
RN ↓	min_pulse_width to RN	0.0974	0.1121	0.0952	0.0952
RN ↑	recovery_rising to CP	0.0276	0.0271	0.0249	0.0222
RN ↑	removal_rising to CP	-0.0196	-0.0077	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0844	-0.0555	-0.0550	-0.0550
TE ↑	hold_rising to CP	-0.0701	-0.0457	-0.0457	-0.0452
TE ↓	setup_rising to CP	0.1469	0.1197	0.1197	0.1176
TE ↑	setup_rising to CP	0.2934	0.2078	0.2078	0.2078
TI ↓	hold_rising to CP	-0.2272	-0.1234	-0.1267	-0.1267
TI ↑	hold_rising to CP	-0.0787	-0.0462	-0.0475	-0.0468
TI ↓	setup_rising to CP	0.2863	0.1875	0.1875	0.1875
TI ↑	setup_rising to CP	0.1189	0.0856	0.0856	0.0856

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.587e-05	1.000e-20
X8_P16	1.808e-05	1.000e-20
X17_P16	2.298e-05	1.000e-20
X33_P16	2.974e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

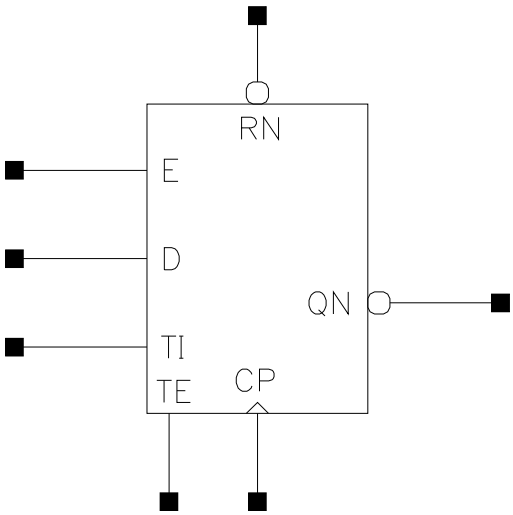
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	7.362e-03	7.423e-03	7.439e-03	7.446e-03
Clock 100Mhz Data 25Mhz	7.956e-03	8.068e-03	8.679e-03	9.442e-03
Clock 100Mhz Data 50Mhz	8.549e-03	8.714e-03	9.919e-03	1.144e-02
Clock = 0 Data 100Mhz	5.547e-03	5.342e-03	5.277e-03	5.244e-03
Clock = 1 Data 100Mhz	2.012e-03	2.060e-03	2.079e-03	2.088e-03

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.760	5.7120
X8_P16	1.200	4.624	5.5488
X17_P16	1.200	4.760	5.7120
X33_P16	1.200	5.032	6.0384

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0007	0.0007	0.0007
E	0.0009	0.0011	0.0011	0.0011
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0010	0.0010	0.0010	0.0010

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to QN ↓	0.1173	0.1095	5.1487	2.6189
CP to QN ↑	0.1311	0.0789	9.0345	4.3334
RN to QN ↑	0.1179	0.1171	9.0107	4.3263
	X17_P16	X33_P16	X17_P16	X33_P16
CP to QN ↓	0.1035	0.1097	1.3150	0.6876
CP to QN ↑	0.0822	0.0900	2.1753	1.1048
RN to QN ↑	0.1163	0.1295	2.1831	1.1088

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1602	0.1084	0.1084	0.1084
CP ↑	min_pulse_width to CP	0.0785	0.0439	0.0485	0.0533
D ↓	hold_rising to CP	-0.1723	-0.0849	-0.0853	-0.0853
D ↑	hold_rising to CP	-0.1043	-0.0413	-0.0387	-0.0387
D ↓	setup_rising to CP	0.2324	0.1443	0.1443	0.1443
D ↑	setup_rising to CP	0.1438	0.0791	0.0785	0.0785
E ↓	hold_rising to CP	-0.1185	-0.1206	-0.1212	-0.1212
E ↑	hold_rising to CP	-0.1021	-0.0413	-0.0413	-0.0413
E ↓	setup_rising to CP	0.2075	0.2004	0.2004	0.1999
E ↑	setup_rising to CP	0.2224	0.1546	0.1546	0.1546
RN ↓	min_pulse_width to RN	0.0947	0.0952	0.1094	0.1191
RN ↑	recovery_rising to CP	0.0276	0.0271	0.0271	0.0276
RN ↑	removal_rising to CP	-0.0196	-0.0131	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0865	-0.0555	-0.0555	-0.0555
TE ↑	hold_rising to CP	-0.0701	-0.0457	-0.0457	-0.0457
TE ↓	setup_rising to CP	0.1469	0.1197	0.1193	0.1197
TE ↑	setup_rising to CP	0.2908	0.2078	0.2078	0.2078
TI ↓	hold_rising to CP	-0.2270	-0.1227	-0.1234	-0.1234
TI ↑	hold_rising to CP	-0.0827	-0.0475	-0.0462	-0.0462
TI ↓	setup_rising to CP	0.2870	0.1875	0.1872	0.1872
TI ↑	setup_rising to CP	0.1189	0.0856	0.0856	0.0856

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.615e-05	1.000e-20
X8_P16	1.810e-05	1.000e-20
X17_P16	2.276e-05	1.000e-20
X33_P16	2.908e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

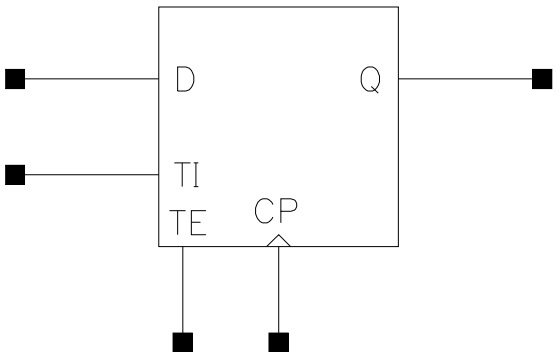
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	7.359e-03	7.420e-03	7.431e-03	7.437e-03
Clock 100Mhz Data 25Mhz	7.901e-03	8.110e-03	8.640e-03	9.385e-03
Clock 100Mhz Data 50Mhz	8.443e-03	8.799e-03	9.849e-03	1.133e-02
Clock = 0 Data 100Mhz	5.551e-03	5.348e-03	5.280e-03	5.246e-03
Clock = 1 Data 100Mhz	2.011e-03	2.063e-03	2.081e-03	2.090e-03

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.400	4.0800
X8_P16	1.200	3.128	3.7536
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0010	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.0962	0.0550	5.7376	2.6897
CP to Q ↑	0.0837	0.0714	9.2582	4.3843
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0853	0.0943	1.2904	0.6774
CP to Q ↑	0.1289	0.1365	2.1695	1.1021

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1437	0.1510	0.1510	0.1510
CP ↑	min_pulse_width to CP	0.0751	0.0405	0.0406	0.0407
D ↓	hold_rising to CP	-0.1039	-0.0436	-0.0468	-0.0468
D ↑	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1485	0.1008	0.1008	0.1008
D ↑	setup_rising to CP	0.0750	0.0417	0.0417	0.0417
TE ↓	hold_rising to CP	-0.0723	-0.0419	-0.0436	-0.0436
TE ↑	hold_rising to CP	-0.0581	-0.0364	-0.0386	-0.0386
TE ↓	setup_rising to CP	0.1242	0.0978	0.0978	0.0978
TE ↑	setup_rising to CP	0.2566	0.2078	0.2078	0.2078
TI ↓	hold_rising to CP	-0.2139	-0.1345	-0.1345	-0.1345
TI ↑	hold_rising to CP	-0.0648	-0.0374	-0.0390	-0.0390
TI ↓	setup_rising to CP	0.2616	0.1985	0.1985	0.1985
TI ↑	setup_rising to CP	0.0994	0.0723	0.0723	0.0723

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.297e-05	1.000e-20
X8_P16	1.519e-05	1.000e-20
X17_P16	2.167e-05	1.000e-20
X33_P16	2.718e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

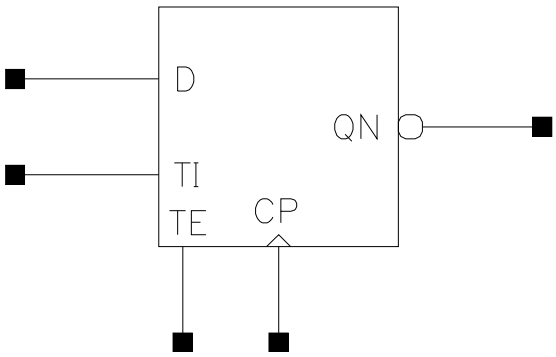
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	6.632e-03	6.709e-03	6.730e-03	6.740e-03
Clock 100Mhz Data 25Mhz	6.678e-03	6.777e-03	7.397e-03	8.027e-03
Clock 100Mhz Data 50Mhz	6.723e-03	6.844e-03	8.065e-03	9.313e-03
Clock = 0 Data 100Mhz	4.365e-03	4.107e-03	4.020e-03	3.977e-03
Clock = 1 Data 100Mhz	1.142e-03	5.870e-04	4.022e-04	3.098e-04

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.536	4.2432
X8_P16	1.200	3.264	3.9168
X17_P16	1.200	3.536	4.2432
X33_P16	1.200	3.808	4.5696

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1097	0.1184	5.8578	2.7126
CP to QN ↑	0.1033	0.0725	9.2056	4.3418
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0878	0.0976	1.2902	0.6775
CP to QN ↑	0.0720	0.0798	2.1676	1.1006

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1431	0.1510	0.1510	0.1510
CP ↑	min_pulse_width to CP	0.0595	0.0406	0.0405	0.0452
D ↓	hold_rising to CP	-0.1039	-0.0468	-0.0436	-0.0436
D ↑	hold_rising to CP	-0.0457	-0.0120	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1485	0.1008	0.1008	0.1008
D ↑	setup_rising to CP	0.0783	0.0417	0.0417	0.0417
TE ↓	hold_rising to CP	-0.0718	-0.0414	-0.0419	-0.0419
TE ↑	hold_rising to CP	-0.0577	-0.0386	-0.0364	-0.0364
TE ↓	setup_rising to CP	0.1242	0.0978	0.0978	0.0978
TE ↑	setup_rising to CP	0.2566	0.2078	0.2078	0.2078
TI ↓	hold_rising to CP	-0.2139	-0.1345	-0.1329	-0.1329
TI ↑	hold_rising to CP	-0.0648	-0.0390	-0.0374	-0.0374
TI ↓	setup_rising to CP	0.2583	0.1985	0.1985	0.1985
TI ↑	setup_rising to CP	0.0994	0.0723	0.0723	0.0723

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.306e-05	1.000e-20
X8_P16	1.526e-05	1.000e-20
X17_P16	2.158e-05	1.000e-20
X33_P16	2.709e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

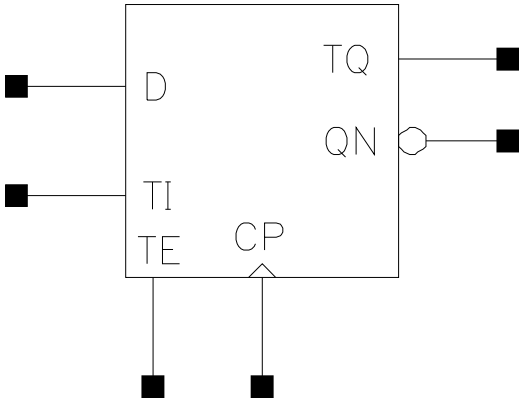
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	6.563e-03	6.672e-03	6.707e-03	6.724e-03
Clock 100Mhz Data 25Mhz	6.641e-03	6.853e-03	7.335e-03	7.982e-03
Clock 100Mhz Data 50Mhz	6.719e-03	7.034e-03	7.963e-03	9.240e-03
Clock = 0 Data 100Mhz	4.381e-03	4.113e-03	4.024e-03	3.980e-03
Clock = 1 Data 100Mhz	1.134e-03	5.833e-04	3.998e-04	3.080e-04

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.536	4.2432
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0013	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
TE	0.0009	0.0011	0.0011	0.0011

TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1223	0.1043	5.2905	2.6277
CP to QN ↑	0.1264	0.0756	8.9742	4.3346
CP to TQ ↓	0.0874	0.0500	7.3751	5.0090
CP to TQ ↑	0.0864	0.0713	17.5816	12.3691
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.0975	0.1053	1.3191	0.6911
CP to QN ↑	0.0778	0.0835	2.1879	1.1164
CP to TQ ↓	0.0520	0.0543	6.7404	6.7495
CP to TQ ↑	0.0726	0.0747	16.0561	16.9339

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1437	0.1510	0.1510	0.1510
CP ↑	min_pulse_width to CP	0.0785	0.0405	0.0439	0.0452
D ↓	hold_rising to CP	-0.1044	-0.0436	-0.0436	-0.0436
D ↑	hold_rising to CP	-0.0431	-0.0120	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1485	0.1008	0.1008	0.1008
D ↑	setup_rising to CP	0.0756	0.0417	0.0417	0.0417
TE ↓	hold_rising to CP	-0.0723	-0.0419	-0.0419	-0.0419
TE ↑	hold_rising to CP	-0.0582	-0.0359	-0.0359	-0.0359
TE ↓	setup_rising to CP	0.1246	0.0956	0.0952	0.0952
TE ↑	setup_rising to CP	0.2566	0.2078	0.2078	0.2078
TI ↓	hold_rising to CP	-0.2123	-0.1336	-0.1339	-0.1296
TI ↑	hold_rising to CP	-0.0648	-0.0374	-0.0374	-0.0374
TI ↓	setup_rising to CP	0.2583	0.1985	0.1985	0.1985
TI ↑	setup_rising to CP	0.0994	0.0723	0.0723	0.0723

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.387e-05	1.000e-20
X8_P16	1.698e-05	1.000e-20
X17_P16	2.051e-05	1.000e-20
X33_P16	2.702e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16

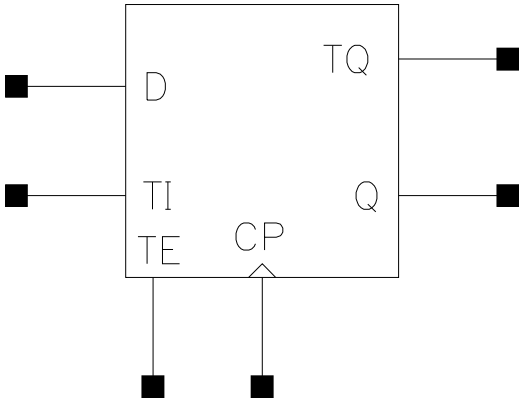
Clock 100Mhz Data 0Mhz	6.753e-03	6.769e-03	6.774e-03	6.778e-03
Clock 100Mhz Data 25Mhz	6.950e-03	7.122e-03	7.391e-03	8.117e-03
Clock 100Mhz Data 50Mhz	7.147e-03	7.476e-03	8.007e-03	9.456e-03
Clock = 0 Data 100Mhz	4.377e-03	4.116e-03	4.030e-03	3.988e-03
Clock = 1 Data 100Mhz	1.142e-03	5.873e-04	4.024e-04	3.100e-04

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.672	4.4064
X8_P16	1.200	3.400	4.0800
X17_P16	1.200	3.672	4.4064
X33_P16	1.200	3.944	4.7328

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ
/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0009	0.0009	0.0009
D	0.0009	0.0007	0.0007	0.0007

TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1283	0.0616	6.1112	2.6898
CP to Q ↑	0.0963	0.0758	9.3464	4.4101
CP to TQ ↓	0.1223	0.0634	6.1031	6.8673
CP to TQ ↑	0.0990	0.0841	12.3720	17.1516
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0876	0.0967	1.3231	0.6889
CP to Q ↑	0.1312	0.1386	2.2032	1.1062
CP to TQ ↓	0.0909	0.1015	6.6286	6.7297
CP to TQ ↑	0.1395	0.1501	16.7122	16.8398

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1431	0.1510	0.1510	0.1510
CP ↑	min_pulse_width to CP	0.1115	0.0453	0.0407	0.0407
D ↓	hold_rising to CP	-0.1039	-0.0436	-0.0468	-0.0468
D ↑	hold_rising to CP	-0.0457	-0.0120	-0.0120	-0.0120
D ↓	setup_rising to CP	0.1489	0.1008	0.1008	0.1008
D ↑	setup_rising to CP	0.0751	0.0417	0.0417	0.0417
TE ↓	hold_rising to CP	-0.0718	-0.0387	-0.0436	-0.0436
TE ↑	hold_rising to CP	-0.0577	-0.0364	-0.0386	-0.0386
TE ↓	setup_rising to CP	0.1246	0.0952	0.0978	0.0978
TE ↑	setup_rising to CP	0.2566	0.2078	0.2078	0.2078
TI ↓	hold_rising to CP	-0.2123	-0.1296	-0.1345	-0.1345
TI ↑	hold_rising to CP	-0.0640	-0.0374	-0.0390	-0.0390
TI ↓	setup_rising to CP	0.2583	0.1985	0.1985	0.1985
TI ↑	setup_rising to CP	0.0994	0.0723	0.0723	0.0723

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.422e-05	1.000e-20
X8_P16	1.604e-05	1.000e-20
X17_P16	2.235e-05	1.000e-20
X33_P16	2.782e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

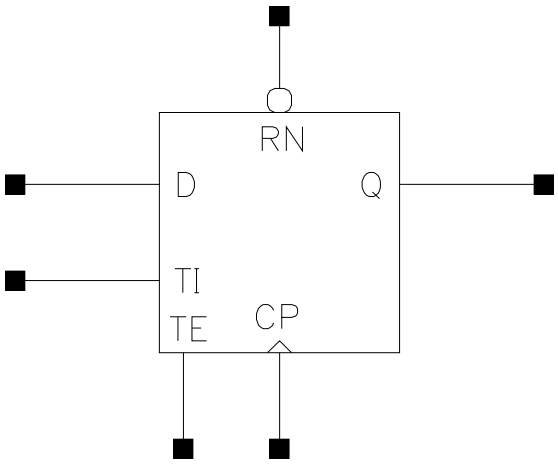
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	6.607e-03	6.694e-03	6.720e-03	6.733e-03
Clock 100Mhz Data 25Mhz	6.996e-03	6.967e-03	7.557e-03	8.233e-03
Clock 100Mhz Data 50Mhz	7.385e-03	7.239e-03	8.394e-03	9.733e-03
Clock = 0 Data 100Mhz	4.356e-03	4.100e-03	4.016e-03	3.974e-03
Clock = 1 Data 100Mhz	1.132e-03	5.824e-04	3.991e-04	3.075e-04

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.672	4.4064
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
RN	0.0008	0.0007	0.0007	0.0007
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1166	0.0590	6.2560	2.7051
CP to Q ↑	0.0923	0.0772	9.2626	4.4285
RN to Q ↓	0.0954	0.0845	5.3581	2.8350
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0896	0.0991	1.3038	0.6868
CP to Q ↑	0.1155	0.1223	2.1680	1.1019
RN to Q ↓	0.1261	0.1355	1.3019	0.6846

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1602	0.1557	0.1605	0.1605
CP ↑	min_pulse_width to CP	0.1021	0.0453	0.0406	0.0407
D ↓	hold_rising to CP	-0.0946	-0.0321	-0.0316	-0.0312
D ↑	hold_rising to CP	-0.0533	-0.0169	-0.0169	-0.0169
D ↓	setup_rising to CP	0.1485	0.0986	0.0981	0.0981
D ↑	setup_rising to CP	0.0880	0.0515	0.0514	0.0515
RN ↓	min_pulse_width to RN	0.0947	0.1023	0.0957	0.0957
RN ↑	recovery_rising to CP	0.0271	0.0271	0.0271	0.0276
RN ↑	removal_rising to CP	-0.0196	-0.0126	-0.0131	-0.0131
TE ↓	hold_rising to CP	-0.0702	-0.0267	-0.0289	-0.0289
TE ↑	hold_rising to CP	-0.0675	-0.0462	-0.0511	-0.0511
TE ↓	setup_rising to CP	0.1246	0.0927	0.0927	0.0927
TE ↑	setup_rising to CP	0.2576	0.1980	0.2006	0.2006
TI ↓	hold_rising to CP	-0.1936	-0.1101	-0.1101	-0.1101
TI ↑	hold_rising to CP	-0.0738	-0.0472	-0.0488	-0.0488
TI ↓	setup_rising to CP	0.2583	0.1888	0.1885	0.1885
TI ↑	setup_rising to CP	0.1140	0.0869	0.0885	0.0885

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.444e-05	1.000e-20
X8_P16	1.630e-05	1.000e-20
X17_P16	2.238e-05	1.000e-20
X33_P16	2.810e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	7.373e-03	7.425e-03	7.474e-03	7.500e-03

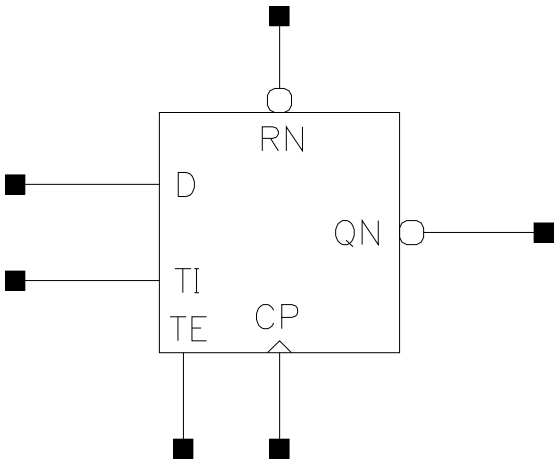
Clock 100Mhz Data 25Mhz	7.491e-03	7.458e-03	8.168e-03	8.844e-03
Clock 100Mhz Data 50Mhz	7.610e-03	7.490e-03	8.861e-03	1.019e-02
Clock = 0 Data 100Mhz	4.456e-03	4.124e-03	4.013e-03	3.958e-03
Clock = 1 Data 100Mhz	1.162e-03	5.983e-04	4.106e-04	3.168e-04

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	3.944	4.7328
X33_P16	1.200	4.216	5.0592

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007
RN	0.0008	0.0008	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	X8_P16	X4_P16	X8_P16
CP to QN ↓	0.1050	0.0973	5.0297	2.5534
CP to QN ↑	0.1191	0.0709	9.0035	4.3080
RN to QN ↑	0.1089	0.1099	8.9809	4.3030
	X17_P16	X33_P16	X17_P16	X33_P16
CP to QN ↓	0.0956	0.1058	1.3059	0.6862
CP to QN ↑	0.0790	0.0875	2.1784	1.1122
RN to QN ↑	0.1151	0.1267	2.1854	1.1137

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1602	0.1557	0.1557	0.1558
CP ↑	min_pulse_width to CP	0.0737	0.0406	0.0453	0.0499
D ↓	hold_rising to CP	-0.0946	-0.0321	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0533	-0.0169	-0.0169	-0.0169
D ↓	setup_rising to CP	0.1485	0.0960	0.0981	0.0981
D ↑	setup_rising to CP	0.0880	0.0515	0.0515	0.0515
RN ↓	min_pulse_width to RN	0.0947	0.0930	0.1094	0.1143
RN ↑	recovery_rising to CP	0.0271	0.0293	0.0271	0.0271
RN ↑	removal_rising to CP	-0.0196	-0.0121	-0.0126	-0.0126
TE ↓	hold_rising to CP	-0.0702	-0.0289	-0.0267	-0.0267
TE ↑	hold_rising to CP	-0.0701	-0.0462	-0.0462	-0.0462
TE ↓	setup_rising to CP	0.1246	0.0927	0.0927	0.0927
TE ↑	setup_rising to CP	0.2576	0.1980	0.2006	0.2006
TI ↓	hold_rising to CP	-0.1977	-0.1101	-0.1085	-0.1085
TI ↑	hold_rising to CP	-0.0781	-0.0488	-0.0472	-0.0472
TI ↓	setup_rising to CP	0.2583	0.1888	0.1885	0.1885
TI ↑	setup_rising to CP	0.1140	0.0869	0.0885	0.0885

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.486e-05	1.000e-20
X8_P16	1.632e-05	1.000e-20
X17_P16	2.213e-05	1.000e-20
X33_P16	2.728e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	7.307e-03	7.388e-03	7.415e-03	7.429e-03

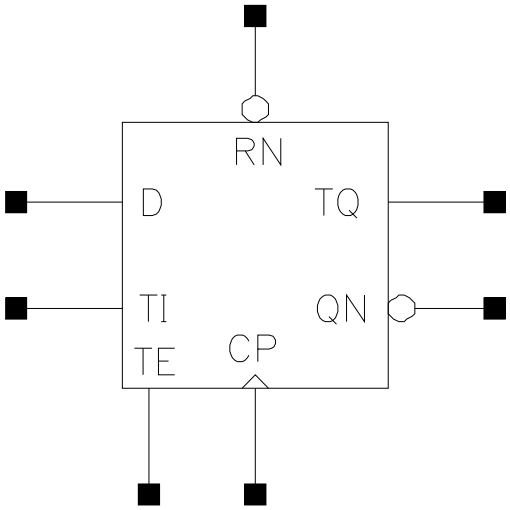
Clock 100Mhz Data 25Mhz	7.355e-03	7.455e-03	8.029e-03	8.680e-03
Clock 100Mhz Data 50Mhz	7.403e-03	7.521e-03	8.643e-03	9.931e-03
Clock = 0 Data 100Mhz	4.452e-03	4.120e-03	4.014e-03	3.961e-03
Clock = 1 Data 100Mhz	1.160e-03	5.975e-04	4.101e-04	3.164e-04

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007

RN	0.0010	0.0007	0.0008	0.0008
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1176	0.1009	5.0427	2.6792
CP to QN ↑	0.1559	0.0798	8.0336	4.4531
CP to TQ ↓	0.1101	0.0535	6.5938	5.2707
CP to TQ ↑	0.0959	0.0782	13.9689	12.9403
RN to QN ↑	0.1078	0.1081	8.1049	4.4411
RN to TQ ↓	0.0735	0.0725	5.8839	5.5486
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.1041	0.1120	1.3274	0.6971
CP to QN ↑	0.0808	0.0853	2.2087	1.1110
CP to TQ ↓	0.0557	0.0580	6.5549	6.4081
CP to TQ ↑	0.0783	0.0803	12.0933	12.2228
RN to QN ↑	0.1123	0.1203	2.2050	1.1087
RN to TQ ↓	0.0780	0.0821	6.8251	6.7198

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1602	0.1557	0.1587	0.1587
CP ↑	min_pulse_width to CP	0.1068	0.0439	0.0453	0.0453
D ↓	hold_rising to CP	-0.0946	-0.0289	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0533	-0.0169	-0.0169	-0.0169
D ↓	setup_rising to CP	0.1485	0.0960	0.0981	0.0981
D ↑	setup_rising to CP	0.0876	0.0515	0.0514	0.0514
RN ↓	min_pulse_width to RN	0.0996	0.0996	0.1045	0.1094
RN ↑	recovery_rising to CP	0.0296	0.0271	0.0271	0.0271
RN ↑	removal_rising to CP	-0.0228	-0.0126	-0.0131	-0.0131
TE ↓	hold_rising to CP	-0.0702	-0.0267	-0.0267	-0.0267
TE ↑	hold_rising to CP	-0.0675	-0.0462	-0.0462	-0.0462
TE ↓	setup_rising to CP	0.1242	0.0927	0.0927	0.0927
TE ↑	setup_rising to CP	0.2570	0.1980	0.1980	0.1980
TI ↓	hold_rising to CP	-0.1936	-0.1101	-0.1085	-0.1085
TI ↑	hold_rising to CP	-0.0745	-0.0472	-0.0488	-0.0488
TI ↓	setup_rising to CP	0.2583	0.1888	0.1885	0.1885
TI ↑	setup_rising to CP	0.1140	0.0869	0.0885	0.0885

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.614e-05	1.000e-20
X8_P16	1.718e-05	1.000e-20
X17_P16	2.093e-05	1.000e-20
X33_P16	2.711e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

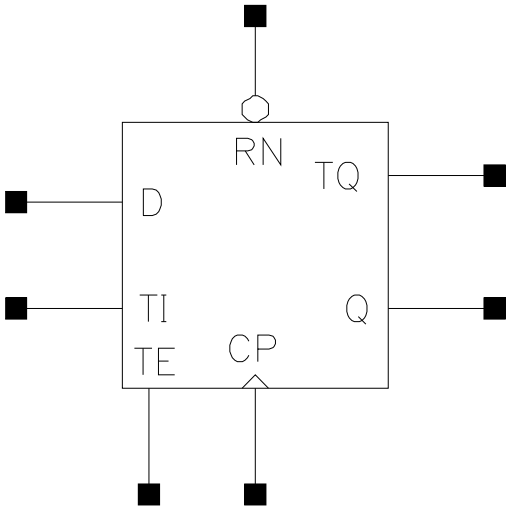
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	7.308e-03	7.384e-03	7.445e-03	7.476e-03
Clock 100Mhz Data 25Mhz	7.582e-03	7.596e-03	7.956e-03	8.706e-03
Clock 100Mhz Data 50Mhz	7.855e-03	7.809e-03	8.468e-03	9.935e-03
Clock = 0 Data 100Mhz	4.449e-03	4.120e-03	4.007e-03	3.951e-03
Clock = 1 Data 100Mhz	1.160e-03	5.977e-04	4.101e-04	3.164e-04

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0009	0.0007	0.0007	0.0007

RN	0.0008	0.0008	0.0007	0.0007
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0003	0.0003	0.0003

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1320	0.0641	6.5367	2.7693
CP to Q ↑	0.0988	0.0805	9.5190	4.5474
CP to TQ ↓	0.1244	0.0639	8.1493	6.9212
CP to TQ ↑	0.1030	0.0858	18.8344	17.0723
RN to Q ↓	0.0989	0.0966	5.5562	2.9127
RN to TQ ↓	0.0967	0.0938	7.0515	7.2484
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0924	0.1024	1.3209	0.6953
CP to Q ↑	0.1161	0.1233	2.1746	1.1045
CP to TQ ↓	0.0958	0.1082	6.6636	6.7591
CP to TQ ↑	0.1238	0.1352	16.8454	16.9072
RN to Q ↓	0.1290	0.1389	1.3193	0.6939
RN to TQ ↓	0.1323	0.1448	6.6620	6.7574

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1603	0.1557	0.1558	0.1558
CP ↑	min_pulse_width to CP	0.1162	0.0500	0.0406	0.0406
D ↓	hold_rising to CP	-0.0946	-0.0289	-0.0321	-0.0321
D ↑	hold_rising to CP	-0.0533	-0.0169	-0.0169	-0.0169
D ↓	setup_rising to CP	0.1489	0.0960	0.0986	0.0986
D ↑	setup_rising to CP	0.0880	0.0515	0.0515	0.0515
RN ↓	min_pulse_width to RN	0.0996	0.1143	0.0930	0.0930
RN ↑	recovery_rising to CP	0.0276	0.0293	0.0271	0.0271
RN ↑	removal_rising to CP	-0.0174	-0.0125	-0.0126	-0.0126
TE ↓	hold_rising to CP	-0.0702	-0.0273	-0.0289	-0.0289
TE ↑	hold_rising to CP	-0.0701	-0.0462	-0.0462	-0.0462
TE ↓	setup_rising to CP	0.1246	0.0927	0.0927	0.0927
TE ↑	setup_rising to CP	0.2517	0.1980	0.1980	0.1980
TI ↓	hold_rising to CP	-0.1944	-0.1095	-0.1101	-0.1101
TI ↑	hold_rising to CP	-0.0781	-0.0475	-0.0488	-0.0488
TI ↓	setup_rising to CP	0.2570	0.1888	0.1888	0.1888
TI ↑	setup_rising to CP	0.1140	0.0869	0.0869	0.0876

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.512e-05	1.000e-20
X8_P16	1.693e-05	1.000e-20
X17_P16	2.277e-05	1.000e-20
X33_P16	2.851e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

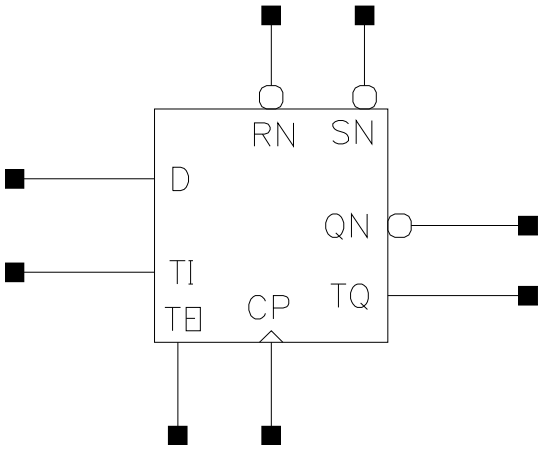
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	7.360e-03	7.415e-03	7.431e-03	7.440e-03
Clock 100Mhz Data 25Mhz	7.652e-03	7.593e-03	8.271e-03	8.972e-03
Clock 100Mhz Data 50Mhz	7.943e-03	7.770e-03	9.111e-03	1.050e-02
Clock = 0 Data 100Mhz	4.454e-03	4.123e-03	4.013e-03	3.958e-03
Clock = 1 Data 100Mhz	1.162e-03	5.985e-04	4.107e-04	3.169e-04

SDFPRSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.352	5.2224
X17_P16	1.200	4.488	5.3856
X33_P16	1.200	4.760	5.7120

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010
D	0.0006	0.0006	0.0006
RN	0.0008	0.0008	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to QN ↓	0.1110	0.1186	2.5957	1.3390
CP to QN ↑	0.0823	0.0864	4.3253	2.1837
CP to TQ ↓	0.0621	0.0620	8.4992	8.4975
CP to TQ ↑	0.0914	0.0913	22.7552	22.7594
RN to QN ↓	0.1212	0.1287	2.5966	1.3412
RN to QN ↑	0.1213	0.1277	4.3273	2.1858
RN to TQ ↓	0.0917	0.0912	9.1357	9.1368
RN to TQ ↑	0.1022	0.1022	22.7107	22.7283
SN to QN ↓	0.1282	0.1374	2.6072	1.3442
SN to TQ ↑	0.1064	0.1062	22.9916	23.0055
	X33_P16		**X33_P16**	
CP to QN ↓	0.1372		0.7146	
CP to QN ↑	0.0967		1.1138	
CP to TQ ↓	0.0622		8.5071	
CP to TQ ↑	0.0918		22.7791	
RN to QN ↓	0.1469		0.7151	
RN to QN ↑	0.1416		1.1136	
RN to TQ ↓	0.0912		9.1397	
RN to TQ ↑	0.1026		22.7443	
SN to QN ↓	0.1581		0.7147	
SN to TQ ↑	0.1065		23.0509	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1651	0.1651	0.1651
CP ↑	min_pulse_width to CP	0.0452	0.0500	0.0513
D ↓	hold_rising to CP	-0.0321	-0.0321	-0.0321
D ↑	hold_rising to CP	-0.0169	-0.0169	-0.0169
D ↓	setup_rising to CP	0.1025	0.1025	0.1025
D ↑	setup_rising to CP	0.0573	0.0573	0.0573
RN ↓	min_pulse_width to RN	0.1094	0.1143	0.1218
RN ↑	non_seq_hold_rising to SN	-0.0457	-0.0458	-0.0458
RN ↑	non_seq_setup_rising to SN	0.0986	0.0986	0.0986
RN ↑	recovery_rising to CP	0.0442	0.0442	0.0442
RN ↑	removal_rising to CP	-0.0245	-0.0245	-0.0245
SN ↓	min_pulse_width to SN	0.0891	0.0918	0.1016
SN ↑	recovery_rising to CP	0.0151	0.0151	0.0151
SN ↑	removal_rising to CP	0.0455	0.0455	0.0455

TE ↓	hold_rising to CP	-0.0289	-0.0289	-0.0289
TE ↑	hold_rising to CP	-0.0462	-0.0462	-0.0462
TE ↓	setup_rising to CP	0.1010	0.1010	0.1010
TE ↑	setup_rising to CP	0.2078	0.2078	0.2078
TI ↓	hold_rising to CP	-0.1101	-0.1101	-0.1101
TI ↑	hold_rising to CP	-0.0475	-0.0475	-0.0475
TI ↓	setup_rising to CP	0.1985	0.1985	0.1985
TI ↑	setup_rising to CP	0.0925	0.0925	0.0925

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	1.900e-05	1.000e-20
X17_P16	2.198e-05	1.000e-20
X33_P16	2.731e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

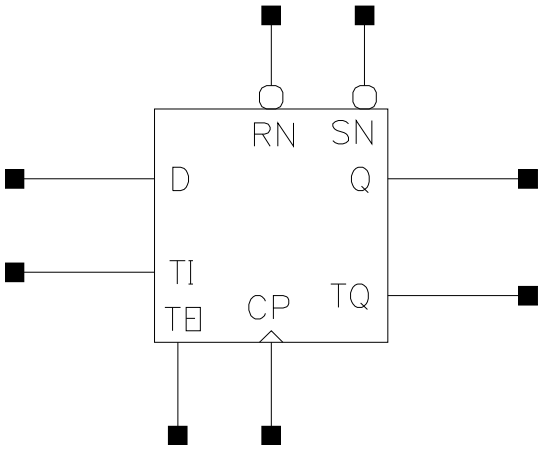
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	7.853e-03	7.853e-03	7.854e-03
Clock 100Mhz Data 25Mhz	7.978e-03	8.287e-03	9.116e-03
Clock 100Mhz Data 50Mhz	8.103e-03	8.721e-03	1.038e-02
Clock = 0 Data 100Mhz	3.929e-03	3.928e-03	3.928e-03
Clock = 1 Data 100Mhz	3.530e-05	3.537e-05	3.543e-05

SDFPRSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P16	1.200	4.216	5.0592
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	SN	TI	TE	IQ	IQ
-	-	1	0	-	-	-	1
-	-	0	-	-	-	-	0
-	/	1	1	TI	1	-	TI
D	/	1	1	-	0	-	D
-	-	1	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010
D	0.0006	0.0006	0.0006
RN	0.0008	0.0009	0.0008

SN	0.0013	0.0013	0.0013
TE	0.0011	0.0011	0.0011
TI	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P16	**X17_P16**	**X8_P16**	**X17_P16**
CP to Q ↓	0.0699	0.0786	2.7062	1.4063
CP to Q ↑	0.0879	0.0928	4.4279	2.2498
CP to TQ ↓	0.0716	0.0821	8.6184	8.7279
CP to TQ ↑	0.0983	0.1088	21.8175	21.9327
RN to Q ↓	0.1109	0.1303	3.0992	1.6218
RN to Q ↑	0.0789	0.0900	4.5929	2.3428
RN to TQ ↓	0.1101	0.1298	9.4029	9.6501
RN to TQ ↑	0.0959	0.1162	22.0388	22.1623
SN to Q ↑	0.1054	0.1164	4.5889	2.3416
SN to TQ ↑	0.1223	0.1426	22.0460	22.1653
	X33_P16		**X33_P16**	
CP to Q ↓	0.1008		0.7583	
CP to Q ↑	0.1065		1.1605	
CP to TQ ↓	0.1005		9.0333	
CP to TQ ↑	0.1285		22.1423	
RN to Q ↓	0.1770		0.8930	
RN to Q ↑	0.1176		1.2218	
RN to TQ ↓	0.1654		10.2873	
RN to TQ ↑	0.1563		22.3968	
SN to Q ↑	0.1438		1.2223	
SN to TQ ↑	0.1824		22.3990	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1651	0.1651	0.1652
CP ↑	min_pulse_width to CP	0.0546	0.0641	0.0879
D ↓	hold_rising to CP	-0.0289	-0.0289	-0.0289
D ↑	hold_rising to CP	-0.0169	-0.0169	-0.0169
D ↓	setup_rising to CP	0.1025	0.1025	0.1025
D ↑	setup_rising to CP	0.0573	0.0573	0.0573
RN ↓	min_pulse_width to RN	0.1289	0.1533	0.2021
RN ↑	non_seq_hold_rising to SN	-0.0505	-0.0604	-0.0798
RN ↑	non_seq_setup_rising to SN	0.0938	0.0938	0.1311
RN ↑	recovery_rising to CP	0.0368	0.0368	0.0368
RN ↑	removal_rising to CP	-0.0196	-0.0196	-0.0196
SN ↓	min_pulse_width to SN	0.1016	0.1184	0.1553
SN ↑	recovery_rising to CP	0.0151	0.0151	0.0151
SN ↑	removal_rising to CP	0.0455	0.0455	0.0455

TE ↓	hold_rising to CP	-0.0267	-0.0267	-0.0273
TE ↑	hold_rising to CP	-0.0462	-0.0462	-0.0462
TE ↓	setup_rising to CP	0.1008	0.1010	0.1008
TE ↑	setup_rising to CP	0.2078	0.2078	0.2078
TI ↓	hold_rising to CP	-0.1085	-0.1085	-0.1052
TI ↑	hold_rising to CP	-0.0475	-0.0475	-0.0475
TI ↓	setup_rising to CP	0.1985	0.1985	0.1985
TI ↑	setup_rising to CP	0.0925	0.0925	0.0925

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X8_P16	1.889e-05	1.000e-20
X17_P16	2.195e-05	1.000e-20
X33_P16	2.764e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

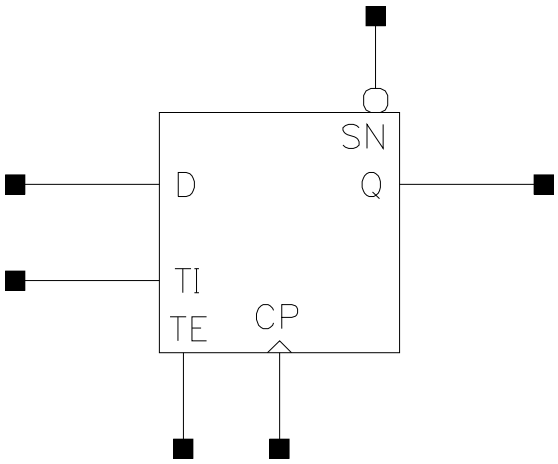
Pin Cycle	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	7.839e-03	7.841e-03	7.842e-03
Clock 100Mhz Data 25Mhz	7.906e-03	8.296e-03	9.350e-03
Clock 100Mhz Data 50Mhz	7.973e-03	8.750e-03	1.086e-02
Clock = 0 Data 100Mhz	3.928e-03	3.928e-03	3.929e-03
Clock = 1 Data 100Mhz	3.515e-05	3.520e-05	3.530e-05

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0005	0.0005	0.0005
SN	0.0014	0.0014	0.0015	0.0015
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004
	X33_P16			

CP	0.0010			
D	0.0005			
SN	0.0015			
TE	0.0011			
TI	0.0004			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1174	0.0613	6.2704	2.6899
CP to Q ↑	0.0968	0.0807	9.3383	4.4120
SN to Q ↑	0.0712	0.0808	9.0915	4.4095
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to Q ↓	0.0882	0.0937	1.3054	0.9021
CP to Q ↑	0.1158	0.1198	2.1673	1.4647
SN to Q ↑	0.1150	0.1190	2.1685	1.4657
	X33_P16		**X33_P16**	
CP to Q ↓	0.0976		0.6869	
CP to Q ↑	0.1223		1.1026	
SN to Q ↑	0.1216		1.1022	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.1650	0.1674	0.1668	0.1675
CP ↑	min_pulse_width to CP	0.1021	0.0453	0.0407	0.0407
D ↓	hold_rising to CP	-0.0942	-0.0370	-0.0387	-0.0387
D ↑	hold_rising to CP	-0.0506	-0.0116	-0.0137	-0.0137
D ↓	setup_rising to CP	0.1534	0.1057	0.1057	0.1057
D ↑	setup_rising to CP	0.0853	0.0434	0.0434	0.0434
SN ↓	min_pulse_width to SN	0.0620	0.0718	0.0691	0.0691
SN ↑	recovery_rising to CP	0.0155	0.0151	0.0151	0.0151
SN ↑	removal_rising to CP	0.0336	0.0460	0.0456	0.0456
TE ↓	hold_rising to CP	-0.0702	-0.0338	-0.0338	-0.0338
TE ↑	hold_rising to CP	-0.0652	-0.0413	-0.0413	-0.0413
TE ↓	setup_rising to CP	0.1295	0.1027	0.1027	0.1027
TE ↑	setup_rising to CP	0.2625	0.2127	0.2127	0.2127
TI ↓	hold_rising to CP	-0.1977	-0.1183	-0.1198	-0.1198
TI ↑	hold_rising to CP	-0.0729	-0.0423	-0.0439	-0.0439
TI ↓	setup_rising to CP	0.2632	0.2034	0.2034	0.2034
TI ↑	setup_rising to CP	0.1091	0.0787	0.0787	0.0787
		X33_P16			

CP ↓	min_pulse_width to CP	0.1675			
CP ↑	min_pulse_width to CP	0.0407			
D ↓	hold_rising to CP	-0.0387			
D ↑	hold_rising to CP	-0.0137			
D ↓	setup_rising to CP	0.1057			
D ↑	setup_rising to CP	0.0439			
SN ↓	min_pulse_width to SN	0.0691			
SN ↑	recovery_rising to CP	0.0151			
SN ↑	removal_rising to CP	0.0456			
TE ↓	hold_rising to CP	-0.0338			
TE ↑	hold_rising to CP	-0.0413			
TE ↓	setup_rising to CP	0.1027			
TE ↑	setup_rising to CP	0.2127			
TI ↓	hold_rising to CP	-0.1198			
TI ↑	hold_rising to CP	-0.0439			
TI ↓	setup_rising to CP	0.2034			
TI ↑	setup_rising to CP	0.0787			

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.448e-05	1.000e-20
X8_P16	1.668e-05	1.000e-20
X17_P16	2.249e-05	1.000e-20
X25_P16	2.507e-05	1.000e-20
X33_P16	2.763e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	7.156e-03	7.343e-03	7.404e-03	7.435e-03
Clock 100Mhz Data 25Mhz	7.311e-03	7.448e-03	8.101e-03	8.473e-03
Clock 100Mhz Data 50Mhz	7.466e-03	7.553e-03	8.799e-03	9.512e-03
Clock = 0 Data 100Mhz	4.276e-03	4.046e-03	3.970e-03	3.932e-03
Clock = 1 Data 100Mhz	1.161e-03	5.981e-04	4.105e-04	3.166e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	7.454e-03			

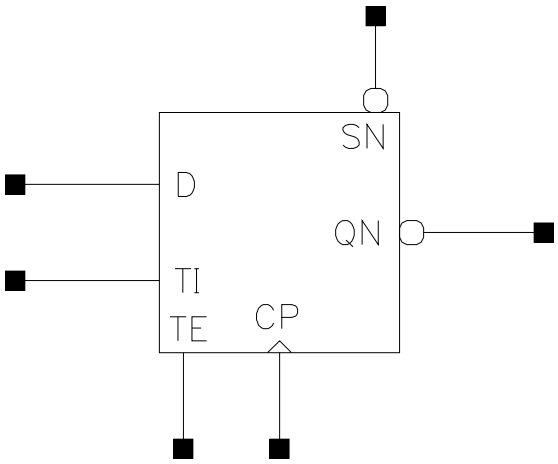
Clock 100Mhz Data 25Mhz	8.775e-03			
Clock 100Mhz Data 50Mhz	1.010e-02			
Clock = 0 Data 100Mhz	3.909e-03			
Clock = 1 Data 100Mhz	2.604e-04			

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	3.944	4.7328
X8_P16	1.200	3.808	4.5696
X17_P16	1.200	4.080	4.8960
X25_P16	1.200	4.216	5.0592
X33_P16	1.200	4.352	5.2224

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X25_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0005	0.0005	0.0005
SN	0.0015	0.0014	0.0015	0.0015
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004
	X33_P16			

CP	0.0010			
D	0.0005			
SN	0.0014			
TE	0.0011			
TI	0.0004			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1098	0.0981	5.0274	2.5565
CP to QN ↑	0.1204	0.0706	8.9873	4.3176
SN to QN ↓	0.0860	0.0970	5.0155	2.5550
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
CP to QN ↓	0.1014	0.1078	1.3109	0.9058
CP to QN ↑	0.0836	0.0890	2.1721	1.4654
SN to QN ↓	0.1027	0.1092	1.3105	0.9054
	X33_P16		**X33_P16**	
CP to QN ↓	0.1128		0.6888	
CP to QN ↑	0.0928		1.1046	
SN to QN ↓	0.1141		0.6888	

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X25_P16
CP ↓	min_pulse_width to CP	0.1650	0.1674	0.1674	0.1674
CP ↑	min_pulse_width to CP	0.0737	0.0406	0.0500	0.0500
D ↓	hold_rising to CP	-0.0968	-0.0387	-0.0338	-0.0338
D ↑	hold_rising to CP	-0.0506	-0.0110	-0.0116	-0.0116
D ↓	setup_rising to CP	0.1538	0.1057	0.1057	0.1057
D ↑	setup_rising to CP	0.0853	0.0434	0.0466	0.0466
SN ↓	min_pulse_width to SN	0.0593	0.0691	0.0767	0.0767
SN ↑	recovery_rising to CP	0.0161	0.0151	0.0151	0.0151
SN ↑	removal_rising to CP	0.0336	0.0460	0.0456	0.0456
TE ↓	hold_rising to CP	-0.0692	-0.0338	-0.0316	-0.0312
TE ↑	hold_rising to CP	-0.0652	-0.0413	-0.0413	-0.0413
TE ↓	setup_rising to CP	0.1295	0.1027	0.1027	0.1027
TE ↑	setup_rising to CP	0.2598	0.2127	0.2127	0.2127
TI ↓	hold_rising to CP	-0.1993	-0.1198	-0.1183	-0.1183
TI ↑	hold_rising to CP	-0.0729	-0.0423	-0.0423	-0.0423
TI ↓	setup_rising to CP	0.2619	0.2034	0.2034	0.2034
TI ↑	setup_rising to CP	0.1091	0.0787	0.0787	0.0787
		X33_P16			

CP ↓	min_pulse_width to CP	0.1675			
CP ↑	min_pulse_width to CP	0.0517			
D ↓	hold_rising to CP	-0.0370			
D ↑	hold_rising to CP	-0.0116			
D ↓	setup_rising to CP	0.1057			
D ↑	setup_rising to CP	0.0434			
SN ↓	min_pulse_width to SN	0.0767			
SN ↑	recovery_rising to CP	0.0151			
SN ↑	removal_rising to CP	0.0460			
TE ↓	hold_rising to CP	-0.0312			
TE ↑	hold_rising to CP	-0.0413			
TE ↓	setup_rising to CP	0.1027			
TE ↑	setup_rising to CP	0.2127			
TI ↓	hold_rising to CP	-0.1183			
TI ↑	hold_rising to CP	-0.0423			
TI ↓	setup_rising to CP	0.2034			
TI ↑	setup_rising to CP	0.0787			

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.424e-05	1.000e-20
X8_P16	1.663e-05	1.000e-20
X17_P16	2.261e-05	1.000e-20
X25_P16	2.546e-05	1.000e-20
X33_P16	2.834e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle	X4_P16	X8_P16	X17_P16	X25_P16
Clock 100Mhz Data 0Mhz	7.156e-03	7.354e-03	7.413e-03	7.442e-03
Clock 100Mhz Data 25Mhz	7.200e-03	7.414e-03	8.114e-03	8.485e-03
Clock 100Mhz Data 50Mhz	7.244e-03	7.475e-03	8.815e-03	9.527e-03
Clock = 0 Data 100Mhz	4.277e-03	4.050e-03	3.972e-03	3.933e-03
Clock = 1 Data 100Mhz	1.161e-03	5.981e-04	4.104e-04	3.166e-04
	X33_P16			
Clock 100Mhz Data 0Mhz	7.460e-03			

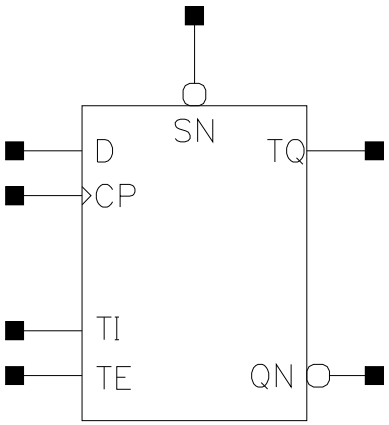
Clock 100Mhz Data 25Mhz	8.821e-03			
Clock 100Mhz Data 50Mhz	1.018e-02			
Clock = 0 Data 100Mhz	3.910e-03			
Clock = 1 Data 100Mhz	2.603e-04			

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.216	5.0592
X8_P16	1.200	4.080	4.8960
X17_P16	1.200	4.352	5.2224
X33_P16	1.200	4.624	5.5488

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0005	0.0005	0.0005

SN	0.0016	0.0017	0.0016	0.0016
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to QN ↓	0.1269	0.1035	5.0226	2.5635
CP to QN ↑	0.1572	0.0802	8.8465	4.3670
CP to TQ ↓	0.1126	0.0544	7.4451	6.1341
CP to TQ ↑	0.0967	0.0769	12.3521	12.0331
SN to QN ↓	0.0825	0.0784	5.0193	2.5647
SN to TQ ↑	0.0564	0.0540	12.1292	11.9939
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to QN ↓	0.1026	0.1138	1.3374	0.6818
CP to QN ↑	0.0904	0.0999	2.1739	1.1040
CP to TQ ↓	0.0677	0.0677	6.3787	6.3827
CP to TQ ↑	0.0867	0.0867	12.1618	12.1799
SN to QN ↓	0.0873	0.0983	1.3346	0.6817
SN to TQ ↑	0.0709	0.0709	12.1480	12.1714

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1650	0.1674	0.1674	0.1674
CP ↑	min_pulse_width to CP	0.1068	0.0440	0.0547	0.0595
D ↓	hold_rising to CP	-0.0942	-0.0370	-0.0338	-0.0338
D ↑	hold_rising to CP	-0.0506	-0.0116	-0.0116	-0.0116
D ↓	setup_rising to CP	0.1534	0.1057	0.1057	0.1057
D ↑	setup_rising to CP	0.0853	0.0434	0.0434	0.0434
SN ↓	min_pulse_width to SN	0.0571	0.0593	0.0620	0.0647
SN ↑	recovery_rising to CP	0.0155	0.0156	0.0156	0.0156
SN ↑	removal_rising to CP	0.0336	0.0434	0.0434	0.0434
TE ↓	hold_rising to CP	-0.0702	-0.0338	-0.0316	-0.0316
TE ↑	hold_rising to CP	-0.0652	-0.0413	-0.0413	-0.0413
TE ↓	setup_rising to CP	0.1291	0.1027	0.1027	0.1027
TE ↑	setup_rising to CP	0.2625	0.2127	0.2127	0.2127
TI ↓	hold_rising to CP	-0.1977	-0.1198	-0.1183	-0.1183
TI ↑	hold_rising to CP	-0.0729	-0.0423	-0.0426	-0.0426
TI ↓	setup_rising to CP	0.2632	0.2034	0.2034	0.2034
TI ↑	setup_rising to CP	0.1091	0.0787	0.0787	0.0787

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.608e-05	1.000e-20
X8_P16	1.842e-05	1.000e-20
X17_P16	2.440e-05	1.000e-20
X33_P16	3.013e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

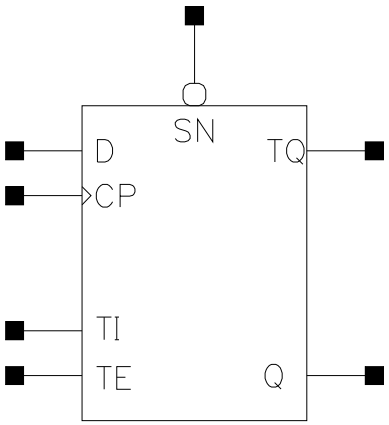
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	7.167e-03	7.353e-03	7.416e-03	7.448e-03
Clock 100Mhz Data 25Mhz	7.508e-03	7.624e-03	8.272e-03	8.954e-03
Clock 100Mhz Data 50Mhz	7.849e-03	7.894e-03	9.127e-03	1.046e-02
Clock = 0 Data 100Mhz	4.286e-03	4.055e-03	3.979e-03	3.940e-03
Clock = 1 Data 100Mhz	1.162e-03	5.982e-04	4.105e-04	3.167e-04

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	4.080	4.8960
X8_P16	1.200	3.944	4.7328
X17_P16	1.200	4.216	5.0592
X33_P16	1.200	4.488	5.3856

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X33_P16
CP	0.0010	0.0010	0.0010	0.0010
D	0.0008	0.0005	0.0005	0.0005

SN	0.0016	0.0015	0.0014	0.0015
TE	0.0009	0.0011	0.0011	0.0011
TI	0.0006	0.0004	0.0004	0.0004

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
CP to Q ↓	0.1354	0.0660	6.4447	2.7428
CP to Q ↑	0.1035	0.0837	9.3861	4.4564
CP to TQ ↓	0.1346	0.0677	9.3903	6.9536
CP to TQ ↑	0.1021	0.0930	12.4398	17.2202
SN to Q ↑	0.0605	0.0845	9.1127	4.4569
SN to TQ ↑	0.0594	0.0953	12.1531	17.1860
	X17_P16	**X33_P16**	**X17_P16**	**X33_P16**
CP to Q ↓	0.0904	0.0998	1.3356	0.6975
CP to Q ↑	0.1175	0.1240	2.1756	1.1065
CP to TQ ↓	0.0938	0.1057	6.6619	6.7494
CP to TQ ↑	0.1254	0.1361	16.8537	16.9311
SN to Q ↑	0.1166	0.1230	2.1754	1.1072
SN to TQ ↑	0.1244	0.1351	16.8530	16.9255

Timing Constraints (ns) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin	Constraint	X4_P16	X8_P16	X17_P16	X33_P16
CP ↓	min_pulse_width to CP	0.1643	0.1674	0.1668	0.1651
CP ↑	min_pulse_width to CP	0.1209	0.0500	0.0407	0.0407
D ↓	hold_rising to CP	-0.0942	-0.0338	-0.0387	-0.0387
D ↑	hold_rising to CP	-0.0500	-0.0116	-0.0137	-0.0110
D ↓	setup_rising to CP	0.1544	0.1057	0.1057	0.1057
D ↑	setup_rising to CP	0.0853	0.0466	0.0434	0.0439
SN ↓	min_pulse_width to SN	0.0544	0.0815	0.0691	0.0691
SN ↑	recovery_rising to CP	0.0161	0.0151	0.0151	0.0151
SN ↑	removal_rising to CP	0.0336	0.0460	0.0456	0.0456
TE ↓	hold_rising to CP	-0.0702	-0.0316	-0.0338	-0.0338
TE ↑	hold_rising to CP	-0.0647	-0.0413	-0.0413	-0.0413
TE ↓	setup_rising to CP	0.1295	0.1027	0.1027	0.1027
TE ↑	setup_rising to CP	0.2566	0.2127	0.2127	0.2127
TI ↓	hold_rising to CP	-0.1977	-0.1192	-0.1198	-0.1198
TI ↑	hold_rising to CP	-0.0745	-0.0423	-0.0439	-0.0439
TI ↓	setup_rising to CP	0.2626	0.2034	0.2034	0.2034
TI ↑	setup_rising to CP	0.1091	0.0787	0.0787	0.0787

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	1.585e-05	1.000e-20
X8_P16	1.758e-05	1.000e-20
X17_P16	2.325e-05	1.000e-20
X33_P16	2.838e-05	1.000e-20

Internal Energy (uW/MHz) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

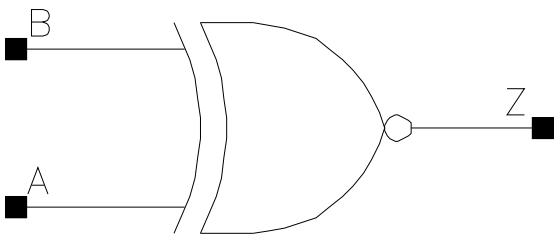
Pin Cycle	X4_P16	X8_P16	X17_P16	X33_P16
Clock 100Mhz Data 0Mhz	7.159e-03	7.344e-03	7.406e-03	7.437e-03
Clock 100Mhz Data 25Mhz	7.521e-03	7.611e-03	8.271e-03	8.977e-03
Clock 100Mhz Data 50Mhz	7.884e-03	7.877e-03	9.136e-03	1.052e-02
Clock = 0 Data 100Mhz	4.287e-03	4.052e-03	3.974e-03	3.934e-03
Clock = 1 Data 100Mhz	1.161e-03	5.982e-04	4.105e-04	3.167e-04

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.360	1.6320
X17_P16	1.200	1.496	1.7952
X25_P16	1.200	2.312	2.7744
X33_P16	1.200	2.448	2.9376

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X6_P16	X8_P16	X17_P16	X25_P16
A	0.0018	0.0007	0.0010	0.0015
B	0.0017	0.0015	0.0020	0.0026
	X33_P16			
A	0.0017			
B	0.0031			

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X6_P16	**X8_P16**	**X6_P16**	**X8_P16**
A to Z ↓	0.0277	0.0653	4.8526	2.7686
A to Z ↑	0.0294	0.0579	6.4926	4.5561
B to Z ↓	0.0261	0.0437	4.8467	2.7478
B to Z ↑	0.0294	0.0414	6.5062	4.5421
	X17_P16	**X25_P16**	**X17_P16**	**X25_P16**
A to Z ↓	0.0616	0.0619	1.3623	0.9348
A to Z ↑	0.0526	0.0531	2.2224	1.4773

B to Z ↓	0.0449	0.0437	1.3577	0.9334
B to Z ↑	0.0408	0.0397	2.2190	1.4749
	X33_P16		**X33_P16**	
A to Z ↓	0.0583		0.7024	
A to Z ↑	0.0513		1.1100	
B to Z ↓	0.0417		0.7013	
B to Z ↑	0.0389		1.1084	

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X6_P16	8.604e-06	1.000e-20
X8_P16	1.039e-05	1.000e-20
X17_P16	1.732e-05	1.000e-20
X25_P16	2.688e-05	1.000e-20
X33_P16	3.665e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	2.272e-03	4.233e-03	6.079e-03	9.736e-03
B to Z	2.195e-03	2.931e-03	4.593e-03	7.204e-03
	X33_P16			
A to Z	1.192e-02			
B to Z	9.085e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

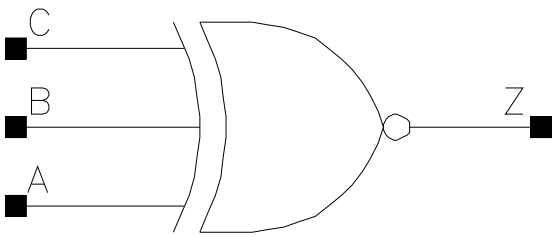
Pin Cycle (vdds)	X6_P16	X8_P16	X17_P16	X25_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P16			
A to Z	0.000e+00			
B to Z	0.000e+00			

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	2.176	2.6112
X16_P16	1.200	2.720	3.2640
X25_P16	1.200	3.944	4.7328

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X16_P16	X25_P16
A	0.0030	0.0025	0.0031	0.0046
B	0.0033	0.0023	0.0031	0.0042
C	0.0021	0.0007	0.0007	0.0008

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0454	0.0775	5.7868	2.9215
A to Z ↑	0.0425	0.0708	9.0532	4.5157
B to Z ↓	0.0464	0.0773	5.7853	2.9220
B to Z ↑	0.0428	0.0709	9.0393	4.5196
C to Z ↓	0.0451	0.1027	5.7872	2.9214
C to Z ↑	0.0410	0.0956	9.0451	4.5194
	X16_P16	**X25_P16**	**X16_P16**	**X25_P16**
A to Z ↓	0.0770	0.0767	1.5045	0.9574
A to Z ↑	0.0758	0.0747	2.3698	1.4838
B to Z ↓	0.0773	0.0781	1.5041	0.9570

B to Z ↑	0.0760	0.0763	2.3694	1.4848
C to Z ↓	0.1080	0.1145	1.5040	0.9568
C to Z ↑	0.1058	0.1121	2.3705	1.4853

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	8.754e-06	1.000e-20
X8_P16	9.173e-06	1.000e-20
X16_P16	1.550e-05	1.000e-20
X25_P16	2.238e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	2.445e-03	3.369e-03	5.515e-03	8.290e-03
B to Z	2.454e-03	3.325e-03	5.498e-03	8.325e-03
C to Z	2.377e-03	5.060e-03	7.619e-03	1.143e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

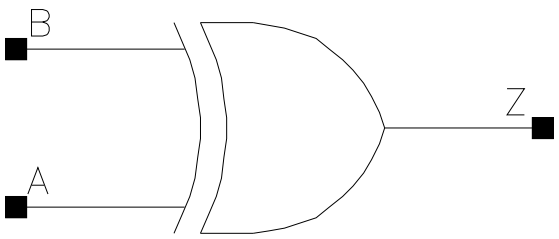
Pin Cycle (vdds)	X4_P16	X8_P16	X16_P16	X25_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	1.224	1.4688
X6_P16	1.200	0.952	1.1424
X8_P16	1.200	1.224	1.4688
X16_P16	1.200	1.360	1.6320
X25_P16	1.200	2.176	2.6112
X31_P16	1.200	2.312	2.7744

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X4_P16	X6_P16	X8_P16	X16_P16
A	0.0008	0.0017	0.0010	0.0012
B	0.0013	0.0016	0.0016	0.0018
	X25_P16	X31_P16		
A	0.0015	0.0020		
B	0.0027	0.0035		

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X6_P16**	**X4_P16**	**X6_P16**
A to Z ↓	0.0578	0.0284	5.1022	3.7290
A to Z ↑	0.0540	0.0299	8.7507	8.1566
B to Z ↓	0.0402	0.0284	5.0774	3.7440
B to Z ↑	0.0408	0.0281	8.7476	8.1504
	X8_P16	**X16_P16**	**X8_P16**	**X16_P16**
A to Z ↓	0.0521	0.0542	2.7022	1.3982

A to Z ↑	0.0464	0.0488	4.4480	2.2391
B to Z ↓	0.0391	0.0405	2.6948	1.3946
B to Z ↑	0.0372	0.0391	4.4479	2.2374
	X25_P16	**X31_P16**	**X25_P16**	**X31_P16**
A to Z ↓	0.0576	0.0539	0.9267	0.7469
A to Z ↑	0.0515	0.0486	1.4763	1.1907
B to Z ↓	0.0420	0.0394	0.9265	0.7468
B to Z ↑	0.0384	0.0364	1.4759	1.1905

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	8.360e-06	1.000e-20
X6_P16	8.417e-06	1.000e-20
X8_P16	1.321e-05	1.000e-20
X16_P16	1.960e-05	1.000e-20
X25_P16	2.654e-05	1.000e-20
X31_P16	3.592e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	3.151e-03	2.270e-03	3.873e-03	5.676e-03
B to Z	2.420e-03	2.146e-03	3.178e-03	4.709e-03
	X25_P16	X31_P16		
A to Z	8.871e-03	1.087e-02		
B to Z	6.355e-03	7.753e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

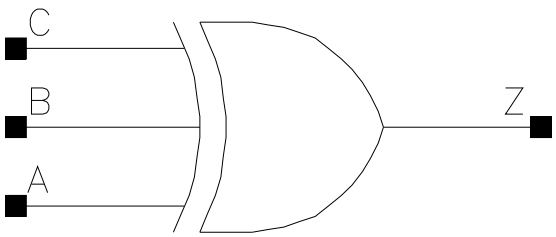
Pin Cycle (vdds)	X4_P16	X6_P16	X8_P16	X16_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P16	X31_P16		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P16	1.200	2.040	2.4480
X8_P16	1.200	1.904	2.2848
X17_P16	1.200	2.040	2.4480
X24_P16	1.200	3.808	4.5696

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	X4_P16	X8_P16	X17_P16	X24_P16
A	0.0025	0.0025	0.0031	0.0056
B	0.0026	0.0023	0.0029	0.0047
C	0.0008	0.0017	0.0024	0.0038

Propagation Delay at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P16	**X8_P16**	**X4_P16**	**X8_P16**
A to Z ↓	0.0456	0.0774	6.0390	2.9203
A to Z ↑	0.0428	0.0707	9.8910	4.5138
B to Z ↓	0.0459	0.0774	6.0387	2.9217
B to Z ↑	0.0431	0.0709	9.8783	4.5148
C to Z ↓	0.0797	0.0753	6.0312	2.9209
C to Z ↑	0.0766	0.0684	9.8620	4.5129
	X17_P16	**X24_P16**	**X17_P16**	**X24_P16**
A to Z ↓	0.0700	0.0822	1.3950	1.0073
A to Z ↑	0.0694	0.0615	2.1959	1.4853
B to Z ↓	0.0699	0.0825	1.3950	1.0068

B to Z ↑	0.0694	0.0616	2.1953	1.4860
C to Z ↓	0.0687	0.0796	1.3949	1.0064
C to Z ↑	0.0680	0.0603	2.1960	1.4863

Average Leakage Power (mW) at 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

	vdd	vdds
X4_P16	9.663e-06	1.000e-20
X8_P16	7.713e-06	1.000e-20
X17_P16	1.448e-05	1.000e-20
X24_P16	2.351e-05	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdd)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	2.287e-03	3.372e-03	5.273e-03	9.011e-03
B to Z	2.306e-03	3.327e-03	5.242e-03	8.941e-03
C to Z	4.661e-03	3.243e-03	5.208e-03	8.813e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 0.90V_0.00V_0.00V_0.00V, Worst process

Pin Cycle (vdds)	X4_P16	X8_P16	X17_P16	X24_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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