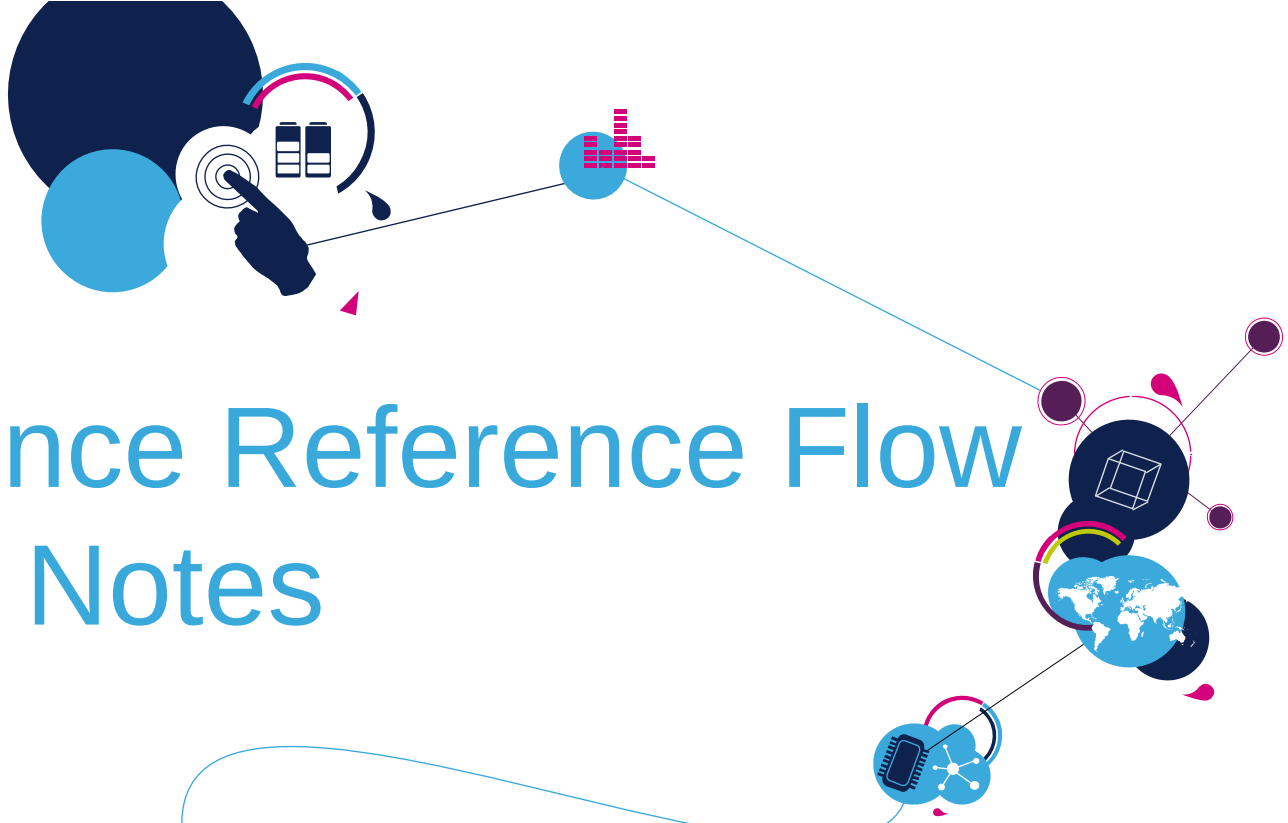

28nm FD-SOI Cadence Reference Flow Sign-Off Application Notes

Version 3.0

Digital Design Flows & Methodologies

October 2018

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Revisions

Version	Date	Comment
3.0	October 2018	• No change. Alignment with PnR 3.0
2.0	March 2018	• Updated EDA tools versions • Vdd range is 0.8V to 1.2V • OCV derate factors have to be applied on both gate delays and wire delays • Updated hold data derates for PB0 & PB4 clock tree • Updated Tempus settings
1.0	June 2017	Initial Version

Prerequisites : Documentation

- Please refer to the **Foundation_Cadence_TechnoKit_cmos028FDSOI** User Manual for the description of the technology files

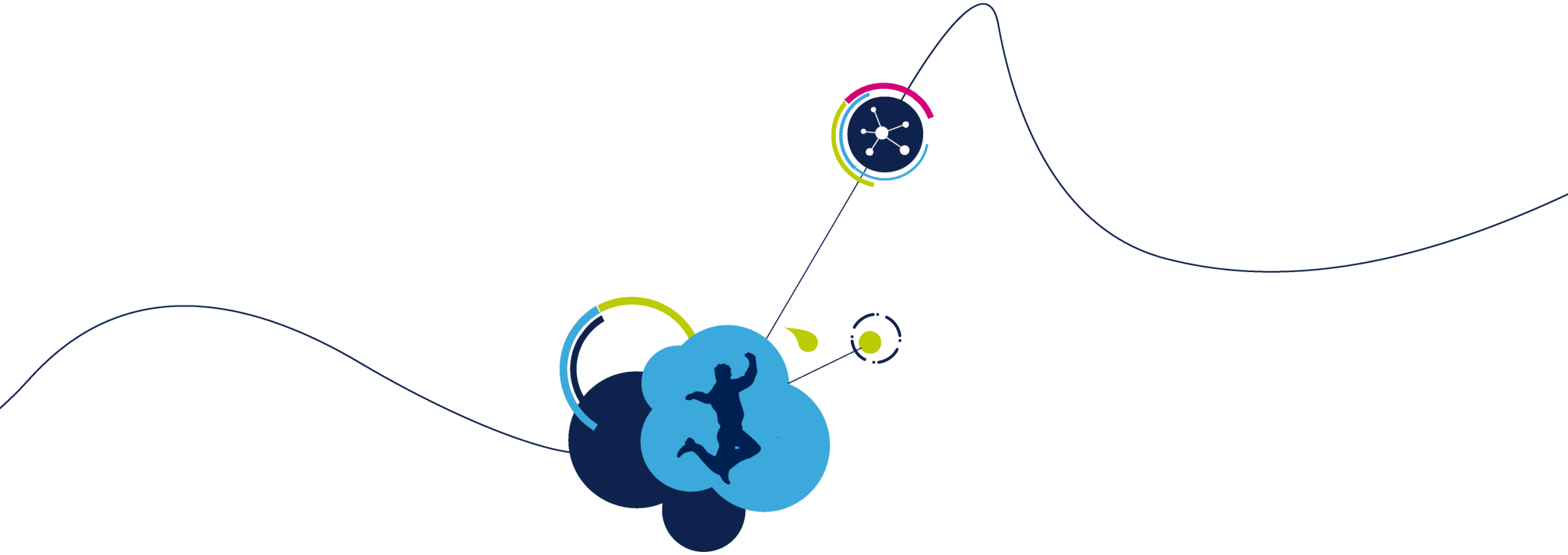
- Please refer to the **28nm FD-SOI Cadence Reference Flow PnR Application Notes** for information regarding Place-and-Route flow

EDA Tools Versions

- The 28nm FD-SOI Cadence Reference Flow has been qualified with the following EDA tools

Sign-Off Step	EDA Tool & Version
Gate-Level RC Extraction	Cadence Quantus 17.11
Static Timing Analysis	Cadence Tempus 15.22
Power Integrity	Cadence Voltus 17.11

- EDA tools versions used for flow execution are left up to user discretion

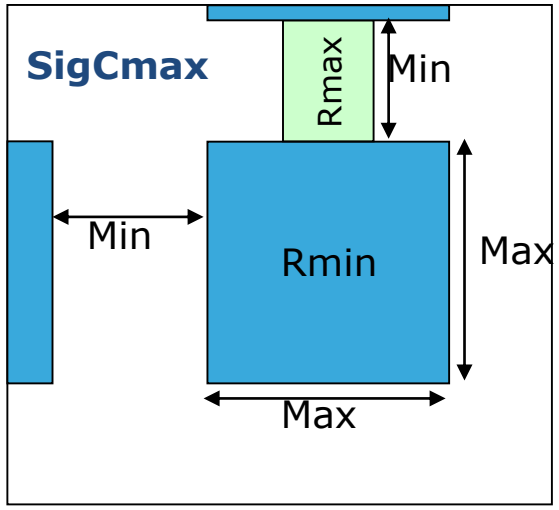


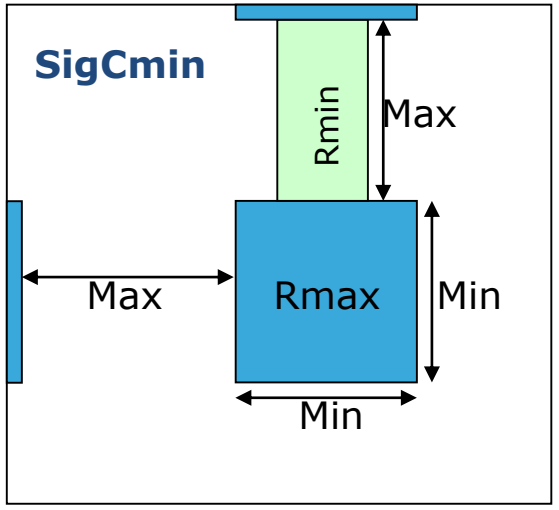
Gate-Level RC Extraction

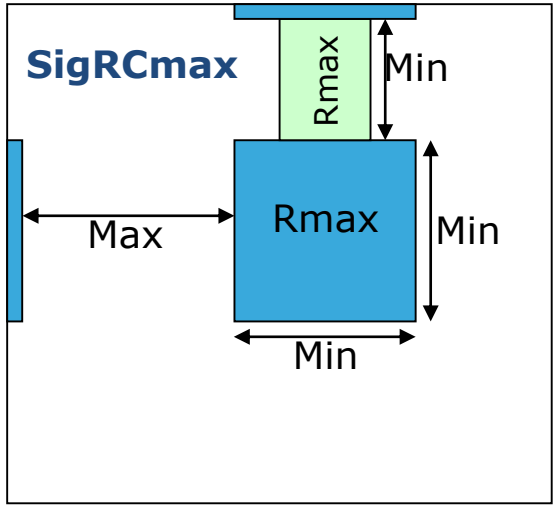
8 Sign-Off Extraction Scenarios

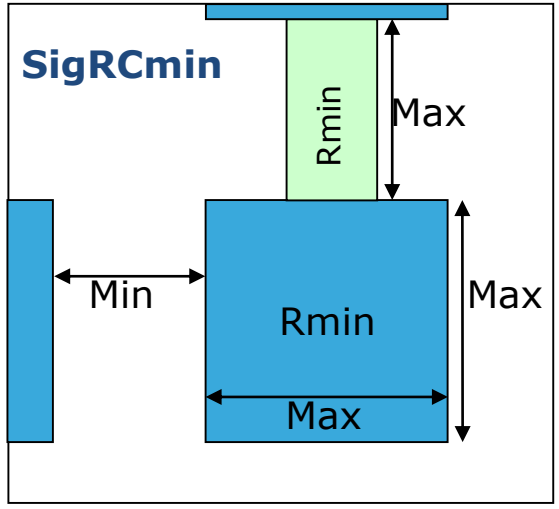
#	RC	T
1	SigCmin	max T
2	SigCmin	min T
3	SigCmax	max T
4	SigCmax	min T
5	SigRCmin	max T
6	SigRCmin	min T
7	SigRCmax	max T
8	SigRCmax	min T

28nm FD-SOI RC Corners Description



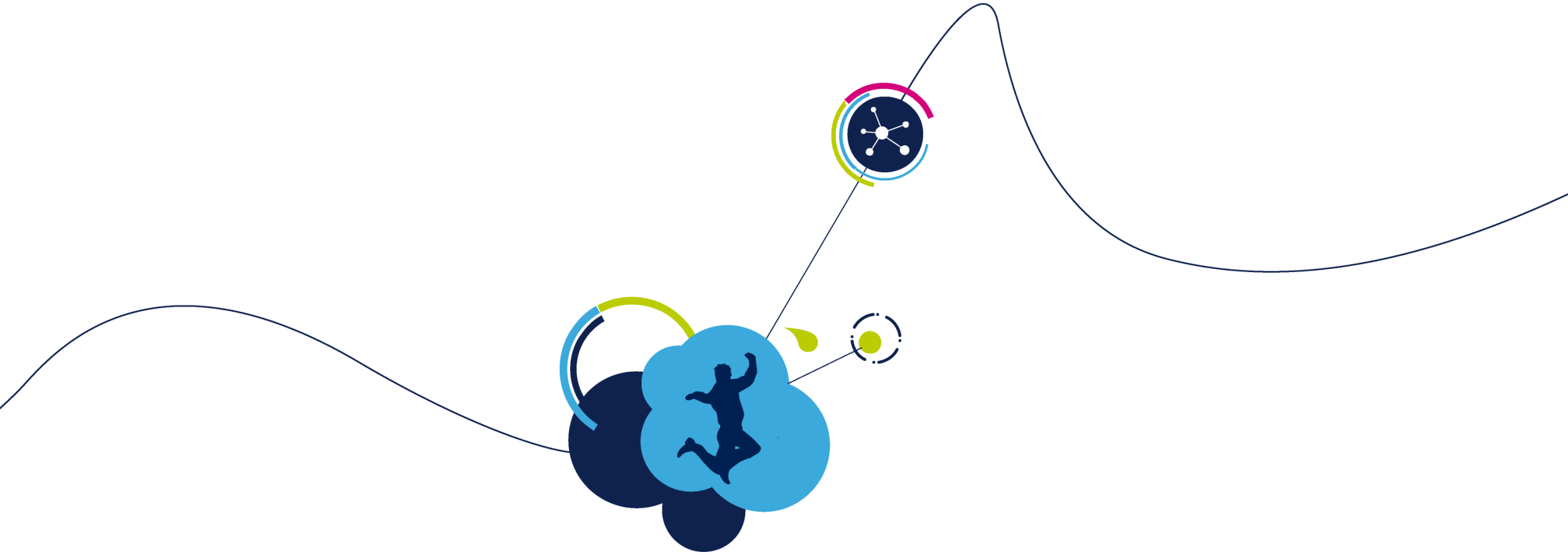






28nm FD-SOI RC Corners Summary

Name	Description	
	Capacitance	Resistance
SigCmin	Clateral MIN Cvertical MIN	Rwire MAX Rvia MIN
SigCmax	Clateral MAX Cvertical MAX	Rwire MIN Rvia MAX
SigRCmin	Clateral MAX Cvertical MIN	Rwire MIN Rvia MIN
SigRCmax	Clateral MIN Cvertical MAX	Rwire MAX Rvia MAX



Static Timing Analysis

16 Sign-Off STA Scenarios per timing mode

#	P	V	T	RC
1	ff28	max V	max T	SigCmin
2	ff28	max V	min T	SigCmin
3	ff28	max V	max T	SigCmax
4	ff28	max V	min T	SigCmax
5	ff28	max V	max T	SigRCmin
6	ff28	max V	min T	SigRCmin
7	ff28	max V	max T	SigRCmax
8	ff28	max V	min T	SigRCmax
9	ss28	min V	max T	SigCmin
10	ss28	min V	min T	SigCmin
11	ss28	min V	max T	SigCmax
12	ss28	min V	min T	SigCmax
13	ss28	min V	max T	SigRCmin
14	ss28	min V	min T	SigRCmin
15	ss28	min V	max T	SigRCmax
16	ss28	min V	min T	SigRCmax

Max. transition Constraint on Clock

- The maximum transition check on clock depends on the operating voltage
- In case of multiple operating voltages, it is required to check the max. transition on clock **only at the lowest voltage**

Voltage	Clock Max. Transition Constraint
0.95 V	150 ps
0.90 V	160 ps
0.85 V	170 ps
0.80 V	200 ps

Clock Tree Implementation Rules

Criteria	Value
Maximum clock transition	See previous slides
Clock tree cells	Only balanced clock cells (*CN* cells)
CTS	Only inverters
Vth	No Vth mix
	Use fastest Vth*
Poly Biasing	No Poly Biasing mix
	Use fastest PB*
Minimum drive strength allowed	X9
Maximum drive strength allowed (EMG constraints)	X70

* *Recommended*

28nm FD-SOI OCV Derating Factors

PB0 Clock Tree

	Clock	Data Derate for Hold Checks	Technology Uncertainty	
			Setup	Hold
1.20 V	+/- 5 %	- 23 %	0 ps	20 ps
1.10 V				
1.00 V				
0.90 V				
0.85 V				
0.80 V				

- To be applied on both gate delays and wire delays
- Valid under compliance with “Clock Tree Implementation Rules”

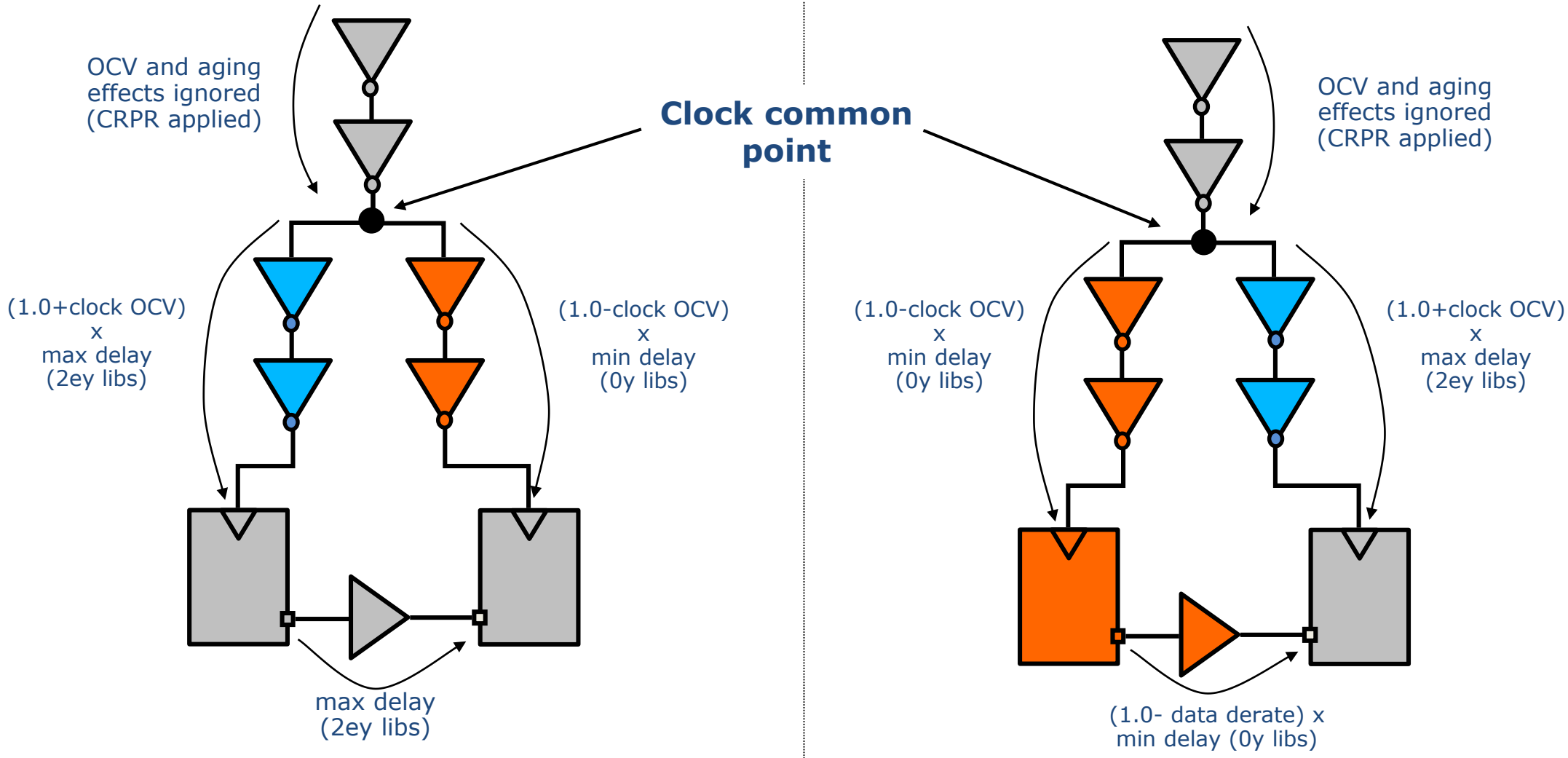
28nm FD-SOI OCV Derating Factors

PB4 Clock Tree

	Clock	Data Derate for Hold Checks	Technology Uncertainty	
			Setup	Hold
1.20 V	+/- 5 %	-18 %	0 ps	20 ps
1.10 V				
1.00 V				
0.90 V				
0.85 V				
0.80 V				

- To be applied on both gate delays and wire delays
- Valid under compliance with “Clock Tree Implementation Rules”

OCV & CRPR Strategy



Setup Checks

Hold Checks

Required Settings for Tempus 1/2

- The following variables have to be set in Tempus for static timing analysis in 28nm FD-SOI:
  - set_design_mode -process 28
  - set_analysis_mode -analysisType onChipVariation
  - set_global timing_cppr_transition_sense same_transition_expanded
  - set_global timing_use_latch_early_launch_edge false
  - set_global timing_enable_early_late_data_slews_for_setuphold_mode_checks true
  - set_global timing_allow_input_delay_on_clock_source true
  - set_global timing_enable_pessimistic_cppr_for_reconvergent_clock_paths true
  - set_global timing_enable_power_ground_constants true
  - set_global timing_enable_timing_window_pessimism_removal true
  - set_global timing_path_based_enable_exhaustive_depth_bounded_by_gba true

Required Settings for Tempus 2/2

- Usage of CCS libraries is mandatory (timing & noise)

- No derate is applied on the dynamic portion of net delays
  - set_timing_derate -net_delay -dynamic -clock –early 1.0
  - set_timing_derate -net_delay -dynamic -clock –late 1.0
  - set_timing_derate -net_delay -dynamic -data –early 1.0
  - set_timing_derate -net_delay -dynamic -data –late 1.0

Setting STA 0y/2ey in Tempus

- The following lines describe how to mix fresh (0y) and aged (2ey) libraries during Static Timing Analysis in Cadence Tempus

```
set init_view_name func_ss28_0.80V_0C_Cmax
read_view_definition view_definitions.tcl
read_verilog
```

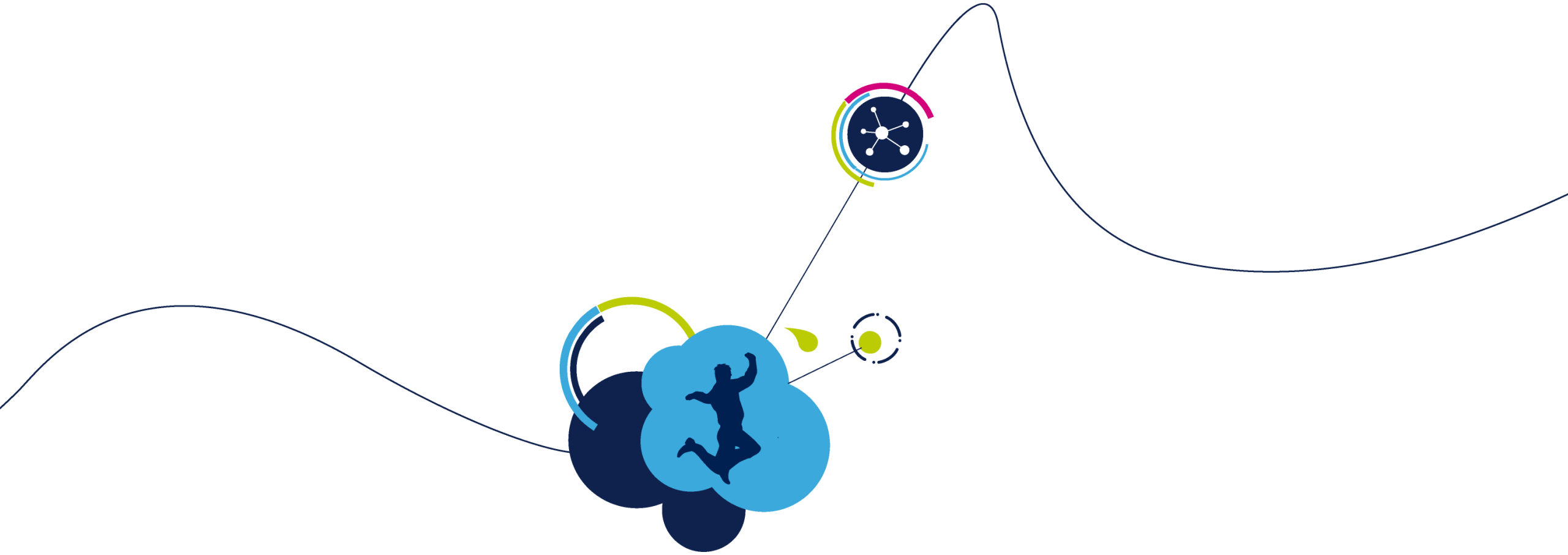
- In file: view_definitions.tcl (example for 2 libraries)

```
create_library_set -name ss28_0.80V_0C_2ey -timing [list \
        $my_working_path/LIBRARIES/C28SOI_SC_12_CLK_LL/ccs/C28SOI_SC_12_CLK_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C_2ey.lib.gz \
        $my_working_path/LIBRARIES/C28SOI_SC_12_CORE_LL/ccs/C28SOI_SC_12_CORE_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C_2ey.lib.gz ]
create_library_set -name ss28_0.80V_0C -timing [list \
        $my_working_path/LIBRARIES/C28SOI_SC_12_CLK_LL/ccs/C28SOI_SC_12_CLK_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C.lib.gz \
        $my_working_path/LIBRARIES/C28SOI_SC_12_CORE_LL/ccs/C28SOI_SC_12_CORE_LL_ss28_0.80V_0.00V_0.00V_0.00V_0C.lib.gz ]
create_delay_corner -name ss28_0.80V_0C_Cmax \
        -early_library_set ss28_0.80V_0C \
        -late_library_set ss28_0.80V_0C_2ey \
        -rc_corner Cmax
set_analysis_view -setup ${init_view_name} -hold ${init_view_name}
```

SDF Generation

SDF Generation Methodology

- SDF can be generated in Tempus for back-annotated simulation purpose
- Using native SDF 3.0 flow, ST standards cells have empty mapping files : it is not required to use them in the Tempus *write_sdf* command
- Some memories and macros may have non empty mapping files
  - In that case those mapping files are compliant with SDF 3.0
  - They have to be loaded in the *write_sdf* command
- Tempus ***write_sdf*** command
  - write_sdf <*design*>*.verilog.sdf.gz* -view <*view*> -precision 4 -version 3.0 –recrem merge_when_paired -setuphold merge_when_paired -map_file “" -recompute_parallel_arcs



Power Analysis & Power Integrity

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Sign-Off Power Analysis Scenarios Description

- The two following corners are typically used for power consumption measurements. However, power analysis scenarios may vary depending on chip specifications and power targets

#	Intent	P	V	T	RC
1	Typical Power Measurement	tt28	Nom. V	25°C	nominal
2	Maximum Power Measurement	ff28	Max. V	Max T	SigCmax

Sign-Off Power Integrity scenarios description

- The two following corners are typically used for static and dynamic IR-Drop analysis. However, IR-Drop scenarios may vary depending on chip specifications and power targets

#	Intent	P	V	T	RC (Signals)	RC (Power Grid)
1	Typical IR-Drop	tt28	Nom. V	25°C	nominal	nominal
2	Maximum IR-Drop	ff28	Max. V	Max T	SigCmax	SigRCmax

- The following corner has to be used for electro-migration checks

#	Intent	P	V	T	RC (Signals)	RC (Power Grid)
1	EM checks (Average & RMS)	ff28	Max. V	Max T	SigCmax	SigRCmax

- The following corner has to be used for ESD Bump-to-clamp checks*

#	Intent	P	V	T	RC (Signals)	RC (Power Grid)
1	ESD B2C Checks	any	any	25°C	NA	SigRCmax

* Please note the ESD Bump-to-clamp check is the only ESD check which is performed with Cadence Voltus, it does not reflect all the ESD checks to be performed on the IO/bumps.

Required Settings for Voltus

- The following variables have to be set in Voltus for tech PGV generation:
  - set_advanced_pg_library_mode -followpins_tap_layer highest_lef_pin_layer \
    -followpins_interface_node_layer highest_lef_pin_layer
- The following variables have to be set in Voltus for all power integrity analyses:
  - set_rail_analysis_mode -enable_manufacturing_effects true
  - set_rail_analysis_mode -process_techgen_em_rules true
  - set_rail_analysis_mode -em_rules_use_layout_dimension true
  - set_rail_analysis_mode –em_stack_via_check true
  - set_rail_analysis_mode -extractor_include extraction.inc
    with extraction.inc content: use_unoptimized_pgv all
    setvar enable_pin_inst_geo_conn_check true
- The following variables have to be set in Voltus for dynamic IR-drop analyses:
  - set_power_include_file power.inc
    (with power.inc content: ChipPwr rAlwaysUseDynamicCurrentModel 1)
  - set_power_analysis_mode -use_ccs_pgpin_cap true
  - set_power_analysis_mode -enable_reduce_lib_model true

Required Settings for Voltus

- CCS-power libraries are mandatory for dynamic IR-drop analyses in 28nm FD-SOI for standard cells and memory libraries

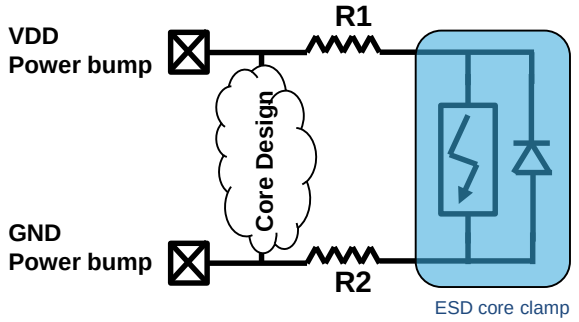
- PGV (Power Grid Views) are mandatory for all power integrity analysis for all libraries that transport current (ex : IOs, …). The corresponding PGV cell list must be defined when setting the rail analysis for both static and dynamic analyses through the following variable :

  - set_rail_analysis_mode –use_ir_view_list pgv_cell_list

Required Settings for Voltus ESD Check

- ESD cell protection have to be tagged during PGV generation:
  - set_advanced_pg_library_mode -common_supply_pins {IO GND VDD} -esd_cells {cell_clamp_list}
- The following command has to be used to perform ESD Bump-to-clamp check :
  - analyze_esd -gnd_net {ground_net_list} -pwr_net {power_net_list} \

    -method bump_to_esd_resistance -use_power_pad true
- User must check for each bump that at least one Bump-to-clamp resistance is ≤ 0.5 ohms.

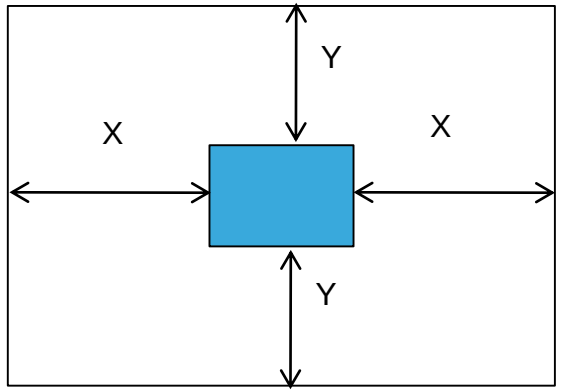


Core clamp placement criteria

R1 < x Ω
R2 < x Ω

EM/IR-Drop Prevention : CTS Halos

- It is recommended to define CTS halos to prevent EM & IR-Drops issues
- CTS halo defines an exclusion area around a clock tree cell (where no other clock tree cells are allowed)
- CTS Halo values depend on design mission profile
  - 28nm FD-SOI example
    - Design mission profile
      - Frequency **800MHz**
      - Voltage **1.15V**
      - grid M3 vertical pitch 16um
      - EM target: **10 years at 115C**
    - CTS Halo guidelines (assuming no halo overlap)
      - Y Halo = 0.1 um
      - X Halo = 8um for drives > X55
      - X Halo = 4um for drives < X55



- Please refer to PnR Application Notes for CTS halos implementation