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C28SOI_SC_12_CLK_LL Databook

12 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

Overview

- C28SOI_SC_12_CLK_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 328 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

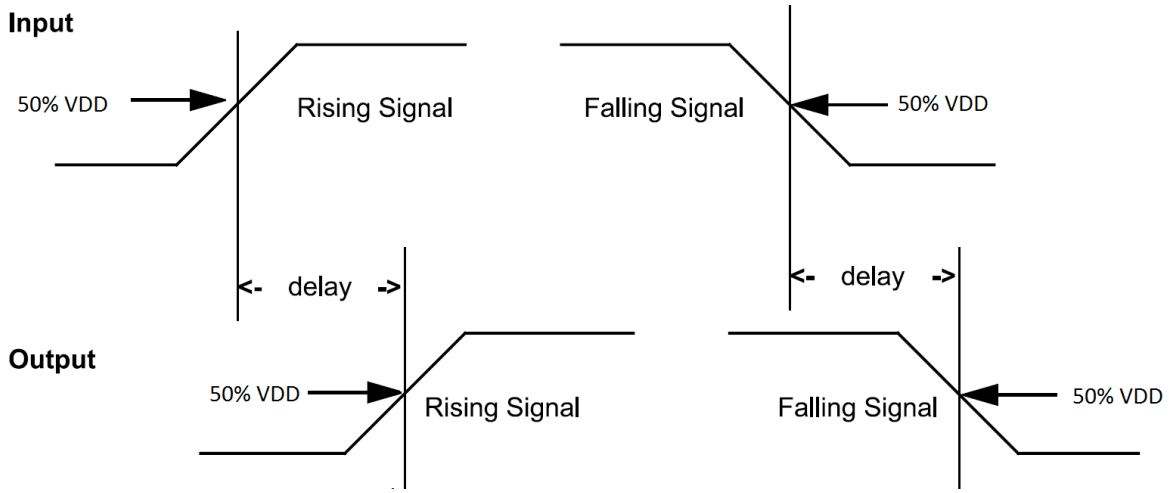


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

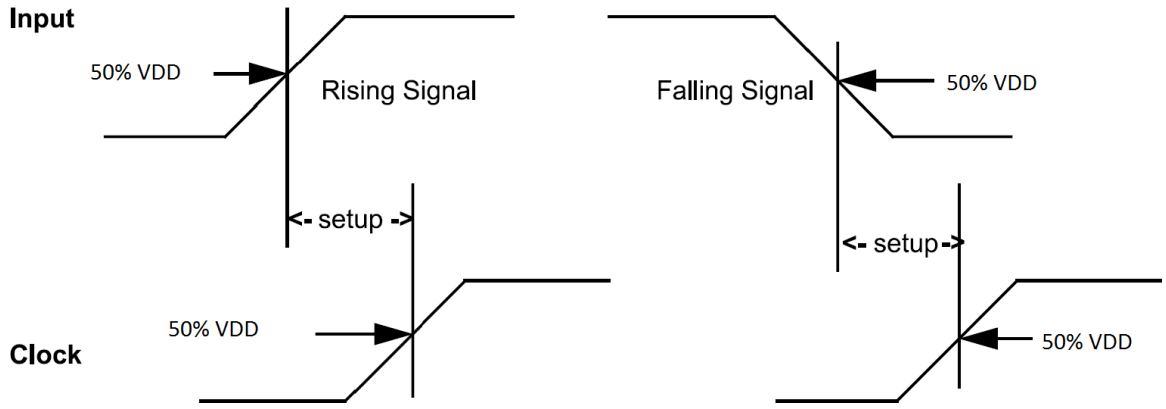


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

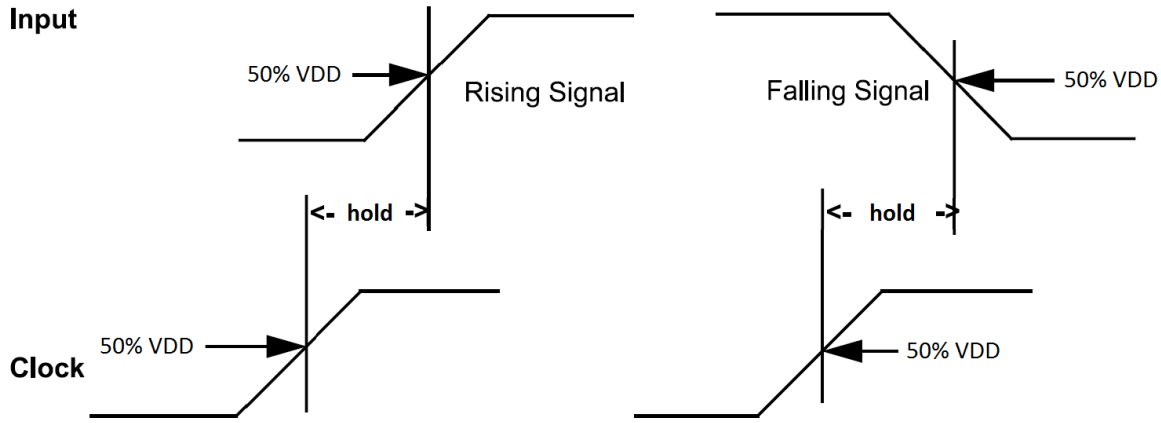


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

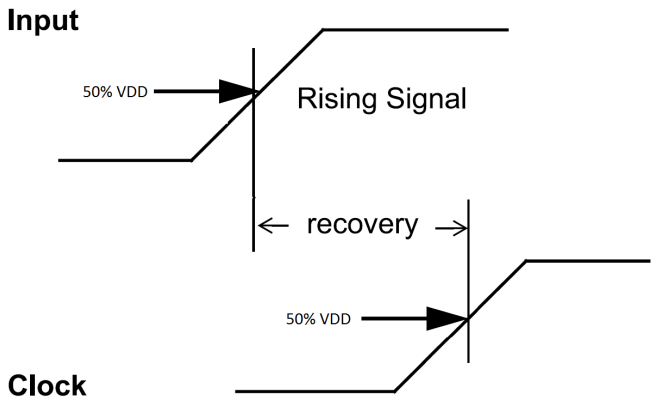


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

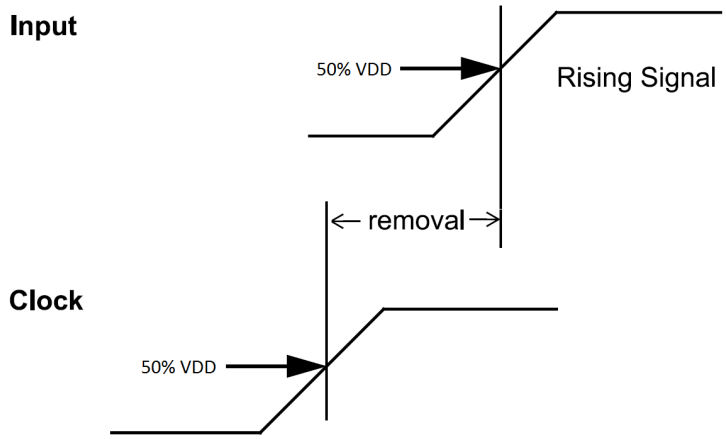


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

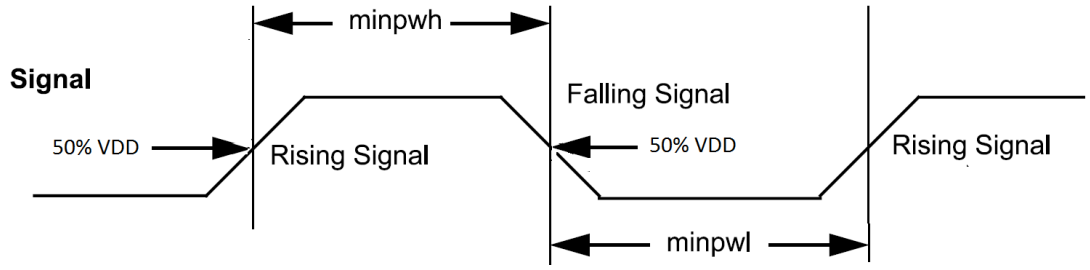


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

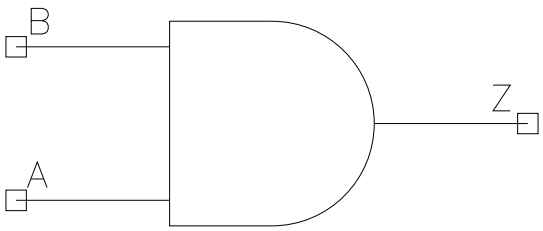
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

CNAND2

Cell Description

2 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.680	0.8160
X15_P4	1.200	0.680	0.8160
X15_P10	1.200	0.680	0.8160
X15_P16	1.200	0.680	0.8160
X20_P0	1.200	0.816	0.9792
X20_P4	1.200	0.816	0.9792
X20_P10	1.200	0.816	0.9792
X20_P16	1.200	0.816	0.9792
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0009	0.0009	0.0010	0.0011
B	0.0009	0.0009	0.0010	0.0010
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0009	0.0009	0.0010	0.0011
B	0.0008	0.0009	0.0009	0.0010
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0015	0.0016	0.0017	0.0018
B	0.0015	0.0015	0.0017	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0219	0.0244	0.9372	0.9969
A to Z ↑	0.0184	0.0201	1.0809	1.1714
B to Z ↓	0.0209	0.0232	0.9371	0.9976
B to Z ↑	0.0195	0.0214	1.0810	1.1716
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0286	0.0322	1.0849	1.1613
A to Z ↑	0.0236	0.0265	1.3088	1.4329
B to Z ↓	0.0272	0.0306	1.0838	1.1615
B to Z ↑	0.0250	0.0280	1.3085	1.4344
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0242	0.0277	0.6908	0.7372
A to Z ↑	0.0206	0.0234	0.8010	0.8722
B to Z ↓	0.0233	0.0266	0.6906	0.7368
B to Z ↑	0.0219	0.0248	0.8013	0.8716
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0324	0.0364	0.8019	0.8586
A to Z ↑	0.0273	0.0306	0.9742	1.0681
B to Z ↓	0.0311	0.0350	0.8012	0.8584
B to Z ↑	0.0289	0.0324	0.9743	1.0685
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0241	0.0271	0.3950	0.4210
A to Z ↑	0.0181	0.0205	0.5476	0.5938
B to Z ↓	0.0220	0.0248	0.3943	0.4200
B to Z ↑	0.0186	0.0210	0.5471	0.5935
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0316	0.0359	0.4569	0.4895
A to Z ↑	0.0239	0.0271	0.6616	0.7249
B to Z ↓	0.0288	0.0327	0.4564	0.4888
B to Z ↑	0.0244	0.0276	0.6615	0.7253

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X15_P0	3.798e-05	1.000e-20
X15_P4	6.398e-06	1.000e-20
X15_P10	1.029e-06	1.000e-20
X15_P16	3.914e-07	1.000e-20
X20_P0	4.765e-05	1.000e-20
X20_P4	7.954e-06	1.000e-20
X20_P10	1.268e-06	1.000e-20
X20_P16	4.807e-07	1.000e-20
X33_P0	7.065e-05	1.000e-20
X33_P4	1.218e-05	1.000e-20
X33_P10	2.033e-06	1.000e-20
X33_P16	8.050e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	2.718e-05	2.416e-05	2.003e-05	1.730e-05
B (output stable)	5.252e-05	6.491e-05	6.984e-05	6.513e-05
A to Z	4.237e-03	3.949e-03	3.979e-03	4.043e-03

B to Z	4.114e-03	3.790e-03	3.769e-03	3.816e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.706e-05	2.444e-05	2.063e-05	1.748e-05
B (output stable)	5.297e-05	6.512e-05	6.922e-05	6.554e-05
A to Z	5.570e-03	5.374e-03	5.374e-03	5.430e-03
B to Z	5.466e-03	5.220e-03	5.169e-03	5.203e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.037e-04	8.512e-05	6.524e-05	5.324e-05
B (output stable)	3.498e-04	3.743e-04	3.800e-04	3.779e-04
A to Z	8.662e-03	8.235e-03	8.172e-03	8.439e-03
B to Z	8.116e-03	7.596e-03	7.441e-03	7.623e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

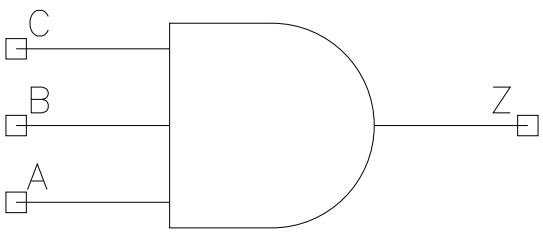
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAND3

Cell Description

3 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X25_P0	1.200	1.360	1.6320
X25_P4	1.200	1.360	1.6320
X25_P10	1.200	1.360	1.6320
X25_P16	1.200	1.360	1.6320
X33_P0	1.200	1.768	2.1216
X33_P4	1.200	1.768	2.1216
X33_P10	1.200	1.768	2.1216
X33_P16	1.200	1.768	2.1216

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0009	0.0009	0.0009	0.0010
B	0.0008	0.0009	0.0009	0.0009
C	0.0008	0.0009	0.0009	0.0010
	X25_P0	X25_P4	X25_P10	X25_P16
A	0.0017	0.0018	0.0019	0.0021
B	0.0015	0.0016	0.0017	0.0019
C	0.0015	0.0016	0.0017	0.0018
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0020	0.0021	0.0022	0.0024
B	0.0019	0.0020	0.0021	0.0023

C	0.0018	0.0019	0.0021	0.0022

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0283	0.0318	0.7769	0.8275
A to Z ↑	0.0258	0.0290	0.7838	0.8523
B to Z ↓	0.0275	0.0308	0.7766	0.8270
B to Z ↑	0.0271	0.0301	0.7835	0.8520
C to Z ↓	0.0265	0.0297	0.7756	0.8268
C to Z ↑	0.0277	0.0308	0.7837	0.8521
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
A to Z ↓	0.0369	0.0419	0.8989	0.9631
A to Z ↑	0.0338	0.0387	0.9515	1.0465
B to Z ↓	0.0359	0.0406	0.8986	0.9633
B to Z ↑	0.0347	0.0393	0.9520	1.0462
C to Z ↓	0.0344	0.0389	0.8981	0.9625
C to Z ↑	0.0354	0.0401	0.9522	1.0474
	X25_P0	**X25_P4**	**X25_P0**	**X25_P4**
A to Z ↓	0.0212	0.0240	0.5320	0.5660
A to Z ↑	0.0201	0.0227	0.7406	0.8039
B to Z ↓	0.0203	0.0229	0.5319	0.5659
B to Z ↑	0.0213	0.0237	0.7415	0.8029
C to Z ↓	0.0191	0.0216	0.5312	0.5656
C to Z ↑	0.0219	0.0243	0.7416	0.8031
	X25_P10	**X25_P16**	**X25_P10**	**X25_P16**
A to Z ↓	0.0280	0.0316	0.6140	0.6572
A to Z ↑	0.0266	0.0302	0.8948	0.9792
B to Z ↓	0.0268	0.0301	0.6130	0.6565
B to Z ↑	0.0274	0.0308	0.8958	0.9812
C to Z ↓	0.0251	0.0282	0.6133	0.6558
C to Z ↑	0.0281	0.0314	0.8941	0.9810
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0222	0.0253	0.3842	0.4095
A to Z ↑	0.0223	0.0252	0.3836	0.4158
B to Z ↓	0.0214	0.0243	0.3846	0.4097
B to Z ↑	0.0236	0.0264	0.3837	0.4166
C to Z ↓	0.0205	0.0233	0.3843	0.4097
C to Z ↑	0.0244	0.0272	0.3834	0.4166
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0295	0.0334	0.4457	0.4767
A to Z ↑	0.0294	0.0334	0.4643	0.5092
B to Z ↓	0.0283	0.0320	0.4452	0.4768
B to Z ↑	0.0304	0.0342	0.4646	0.5099
C to Z ↓	0.0271	0.0306	0.4452	0.4761
C to Z ↑	0.0312	0.0349	0.4644	0.5092

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P0	5.515e-05	1.000e-20
X17_P4	8.999e-06	1.000e-20

X17_P10	1.384e-06	1.000e-20
X17_P16	5.121e-07	1.000e-20
X25_P0	6.145e-05	1.000e-20
X25_P4	1.036e-05	1.000e-20
X25_P10	1.707e-06	1.000e-20
X25_P16	6.948e-07	1.000e-20
X33_P0	1.167e-04	1.000e-20
X33_P4	1.941e-05	1.000e-20
X33_P10	3.031e-06	1.000e-20
X33_P16	1.128e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	2.956e-05	2.273e-05	1.537e-05	1.135e-05
B (output stable)	6.517e-05	6.998e-05	6.924e-05	6.408e-05
C (output stable)	1.187e-04	1.299e-04	8.001e-05	4.697e-05
A to Z	6.281e-03	5.906e-03	5.841e-03	5.949e-03
B to Z	6.138e-03	5.728e-03	5.628e-03	5.709e-03
C to Z	6.014e-03	5.561e-03	5.418e-03	5.476e-03
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	5.487e-05	4.167e-05	2.722e-05	1.936e-05
B (output stable)	1.262e-04	1.365e-04	1.325e-04	1.220e-04
C (output stable)	2.398e-04	2.634e-04	1.645e-04	9.452e-05
A to Z	7.506e-03	7.217e-03	7.242e-03	7.432e-03
B to Z	7.169e-03	6.827e-03	6.804e-03	6.947e-03
C to Z	6.877e-03	6.471e-03	6.364e-03	6.454e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	6.628e-05	5.037e-05	3.436e-05	2.488e-05
B (output stable)	1.538e-04	1.673e-04	1.626e-04	1.506e-04
C (output stable)	2.971e-04	3.249e-04	2.018e-04	1.156e-04
A to Z	1.199e-02	1.149e-02	1.137e-02	1.161e-02
B to Z	1.161e-02	1.104e-02	1.084e-02	1.103e-02
C to Z	1.130e-02	1.063e-02	1.033e-02	1.045e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X25_P0	X25_P4	X25_P10	X25_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

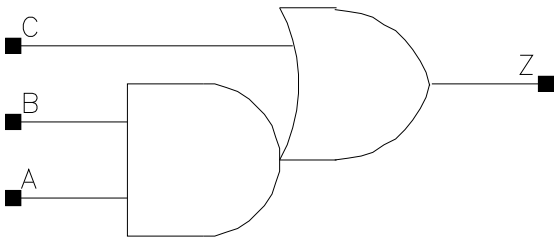
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	1.632	1.9584
X33_P4	1.200	1.632	1.9584
X33_P10	1.200	1.632	1.9584
X33_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0018	0.0019	0.0020	0.0022
B	0.0016	0.0017	0.0018	0.0019
C	0.0016	0.0016	0.0018	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0240	0.0272	0.3969	0.4234
A to Z ↑	0.0219	0.0245	0.5460	0.5926
B to Z ↓	0.0229	0.0260	0.3972	0.4229
B to Z ↑	0.0233	0.0260	0.5458	0.5930
C to Z ↓	0.0237	0.0271	0.3962	0.4222
C to Z ↑	0.0240	0.0267	0.5446	0.5904
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0319	0.0363	0.4600	0.4938

A to Z ↑	0.0283	0.0319	0.6610	0.7243
B to Z ↓	0.0303	0.0343	0.4602	0.4938
B to Z ↑	0.0298	0.0334	0.6602	0.7237
C to Z ↓	0.0319	0.0363	0.4592	0.4925
C to Z ↑	0.0307	0.0342	0.6577	0.7205

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X33_P0	6.223e-05	1.000e-20
X33_P4	1.134e-05	1.000e-20
X33_P10	2.021e-06	1.000e-20
X33_P16	8.227e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.914e-04	1.016e-04	5.074e-05	2.491e-05
B (output stable)	2.440e-04	1.608e-04	1.281e-04	1.198e-04
C (output stable)	2.459e-04	2.352e-04	2.296e-04	2.322e-04
A to Z	9.266e-03	8.716e-03	8.572e-03	8.694e-03
B to Z	8.994e-03	8.365e-03	8.132e-03	8.199e-03
C to Z	1.007e-02	9.654e-03	9.669e-03	9.884e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

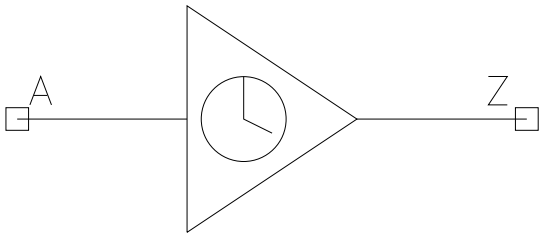
Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNBF

Cell Description

Buffer with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P0	1.200	0.408	0.4896
X4_P4	1.200	0.408	0.4896
X4_P10	1.200	0.408	0.4896
X4_P16	1.200	0.408	0.4896
X7_P0	1.200	0.408	0.4896
X7_P4	1.200	0.408	0.4896
X7_P10	1.200	0.408	0.4896
X7_P16	1.200	0.408	0.4896
X15_P0	1.200	0.544	0.6528
X15_P4	1.200	0.544	0.6528
X15_P10	1.200	0.544	0.6528
X15_P16	1.200	0.544	0.6528
X22_P0	1.200	0.680	0.8160
X22_P4	1.200	0.680	0.8160
X22_P10	1.200	0.680	0.8160
X22_P16	1.200	0.680	0.8160
X30_P0	1.200	0.952	1.1424
X30_P4	1.200	0.952	1.1424
X30_P10	1.200	0.952	1.1424
X30_P16	1.200	0.952	1.1424
X38_P0	1.200	1.088	1.3056
X38_P4	1.200	1.088	1.3056
X38_P10	1.200	1.088	1.3056
X38_P16	1.200	1.088	1.3056
X44_P0	1.200	1.224	1.4688
X44_P4	1.200	1.224	1.4688
X44_P10	1.200	1.224	1.4688
X44_P16	1.200	1.224	1.4688
X52_P0	1.200	1.496	1.7952
X52_P4	1.200	1.496	1.7952
X52_P10	1.200	1.496	1.7952
X52_P16	1.200	1.496	1.7952
X59_P0	1.200	1.632	1.9584

X59_P4	1.200	1.632	1.9584
X59_P10	1.200	1.632	1.9584
X59_P16	1.200	1.632	1.9584
X70_P0	1.200	1.768	2.1216
X70_P4	1.200	1.768	2.1216
X70_P10	1.200	1.768	2.1216
X70_P16	1.200	1.768	2.1216
X94_P0	1.200	2.312	2.7744
X94_P4	1.200	2.312	2.7744
X94_P10	1.200	2.312	2.7744
X94_P16	1.200	2.312	2.7744
X133_P0	1.200	3.264	3.9168
X133_P4	1.200	3.264	3.9168
X133_P10	1.200	3.264	3.9168
X133_P16	1.200	3.264	3.9168

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X4_P0	X4_P4	X4_P10	X4_P16
A	0.0007	0.0007	0.0007	0.0008
	X7_P0	X7_P4	X7_P10	X7_P16
A	0.0007	0.0007	0.0007	0.0008
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0009	0.0009	0.0010	0.0011
	X22_P0	X22_P4	X22_P10	X22_P16
A	0.0010	0.0011	0.0012	0.0012
	X30_P0	X30_P4	X30_P10	X30_P16
A	0.0015	0.0015	0.0016	0.0017
	X38_P0	X38_P4	X38_P10	X38_P16
A	0.0017	0.0018	0.0020	0.0021
	X44_P0	X44_P4	X44_P10	X44_P16
A	0.0018	0.0019	0.0020	0.0022
	X52_P0	X52_P4	X52_P10	X52_P16
A	0.0023	0.0025	0.0027	0.0029
	X59_P0	X59_P4	X59_P10	X59_P16
A	0.0027	0.0028	0.0030	0.0032
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0028	0.0029	0.0031	0.0033
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0036	0.0038	0.0041	0.0044
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0054	0.0057	0.0061	0.0066

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P0	X4_P4	X4_P0	X4_P4
A to Z ↓	0.0210	0.0238	3.3522	3.5677

A to Z ↑	0.0161	0.0182	3.9817	4.3473
	X4_P10	**X4_P16**	**X4_P10**	**X4_P16**
A to Z ↓	0.0276	0.0308	3.8586	4.1200
A to Z ↑	0.0211	0.0235	4.8764	5.3572
	X7_P0	**X7_P4**	**X7_P0**	**X7_P4**
A to Z ↓	0.0210	0.0237	1.8196	1.9393
A to Z ↑	0.0157	0.0179	2.3144	2.5131
	X7_P10	**X7_P16**	**X7_P10**	**X7_P16**
A to Z ↓	0.0276	0.0311	2.0994	2.2474
A to Z ↑	0.0208	0.0233	2.8038	3.0770
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0199	0.0225	0.9513	1.0136
A to Z ↑	0.0167	0.0189	1.0721	1.1651
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0262	0.0298	1.1003	1.1783
A to Z ↑	0.0218	0.0246	1.3004	1.4249
	X22_P0	**X22_P4**	**X22_P0**	**X22_P4**
A to Z ↓	0.0200	0.0228	0.6508	0.6938
A to Z ↑	0.0177	0.0200	0.7238	0.7857
	X22_P10	**X22_P16**	**X22_P10**	**X22_P16**
A to Z ↓	0.0267	0.0302	0.7539	0.8068
A to Z ↑	0.0232	0.0259	0.8758	0.9604
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**
A to Z ↓	0.0191	0.0218	0.4557	0.4861
A to Z ↑	0.0157	0.0179	0.5411	0.5867
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
A to Z ↓	0.0252	0.0286	0.5280	0.5661
A to Z ↑	0.0206	0.0232	0.6538	0.7164
	X38_P0	**X38_P4**	**X38_P0**	**X38_P4**
A to Z ↓	0.0190	0.0216	0.3670	0.3911
A to Z ↑	0.0162	0.0183	0.4343	0.4715
	X38_P10	**X38_P16**	**X38_P10**	**X38_P16**
A to Z ↓	0.0252	0.0285	0.4255	0.4560
A to Z ↑	0.0212	0.0238	0.5245	0.5750
	X44_P0	**X44_P4**	**X44_P0**	**X44_P4**
A to Z ↓	0.0194	0.0220	0.3167	0.3379
A to Z ↑	0.0167	0.0188	0.3823	0.4152
	X44_P10	**X44_P16**	**X44_P10**	**X44_P16**
A to Z ↓	0.0257	0.0292	0.3672	0.3932
A to Z ↑	0.0218	0.0244	0.4627	0.5076
	X52_P0	**X52_P4**	**X52_P0**	**X52_P4**
A to Z ↓	0.0191	0.0217	0.2732	0.2915
A to Z ↑	0.0174	0.0196	0.3192	0.3463
	X52_P10	**X52_P16**	**X52_P10**	**X52_P16**
A to Z ↓	0.0254	0.0287	0.3166	0.3393
A to Z ↑	0.0227	0.0254	0.3858	0.4227
	X59_P0	**X59_P4**	**X59_P0**	**X59_P4**
A to Z ↓	0.0190	0.0216	0.2391	0.2552
A to Z ↑	0.0165	0.0186	0.2828	0.3070
	X59_P10	**X59_P16**	**X59_P10**	**X59_P16**
A to Z ↓	0.0251	0.0286	0.2773	0.2972
A to Z ↑	0.0215	0.0242	0.3421	0.3750

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0202	0.0227	0.1997	0.2128
A to Z ↑	0.0173	0.0193	0.2453	0.2651
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0266	0.0300	0.2314	0.2483
A to Z ↑	0.0223	0.0250	0.2958	0.3239
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0199	0.0224	0.1522	0.1624
A to Z ↑	0.0172	0.0191	0.1866	0.2022
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0261	0.0295	0.1770	0.1899
A to Z ↑	0.0221	0.0247	0.2256	0.2469
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0202	0.0227	0.1126	0.1208
A to Z ↑	0.0176	0.0197	0.1357	0.1480
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0264	0.0298	0.1318	0.1415
A to Z ↑	0.0226	0.0253	0.1649	0.1807

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X4_P0	6.414e-06	1.000e-20
X4_P4	1.210e-06	1.000e-20
X4_P10	2.344e-07	1.000e-20
X4_P16	1.019e-07	1.000e-20
X7_P0	1.386e-05	1.000e-20
X7_P4	2.497e-06	1.000e-20
X7_P10	4.406e-07	1.000e-20
X7_P16	1.747e-07	1.000e-20
X15_P0	3.015e-05	1.000e-20
X15_P4	5.235e-06	1.000e-20
X15_P10	8.700e-07	1.000e-20
X15_P16	3.281e-07	1.000e-20
X22_P0	4.606e-05	1.000e-20
X22_P4	7.887e-06	1.000e-20
X22_P10	1.280e-06	1.000e-20
X22_P16	4.739e-07	1.000e-20
X30_P0	5.693e-05	1.000e-20
X30_P4	9.962e-06	1.000e-20
X30_P10	1.668e-06	1.000e-20
X30_P16	6.363e-07	1.000e-20
X38_P0	7.365e-05	1.000e-20
X38_P4	1.281e-05	1.000e-20
X38_P10	2.121e-06	1.000e-20
X38_P16	8.000e-07	1.000e-20
X44_P0	8.452e-05	1.000e-20
X44_P4	1.452e-05	1.000e-20
X44_P10	2.379e-06	1.000e-20
X44_P16	8.954e-07	1.000e-20
X52_P0	9.808e-05	1.000e-20
X52_P4	1.708e-05	1.000e-20
X52_P10	2.830e-06	1.000e-20

X52_P16	1.070e-06	1.000e-20
X59_P0	1.172e-04	1.000e-20
X59_P4	2.015e-05	1.000e-20
X59_P10	3.296e-06	1.000e-20
X59_P16	1.237e-06	1.000e-20
X70_P0	1.305e-04	1.000e-20
X70_P4	2.278e-05	1.000e-20
X70_P10	3.779e-06	1.000e-20
X70_P16	1.430e-06	1.000e-20
X94_P0	1.730e-04	1.000e-20
X94_P4	3.019e-05	1.000e-20
X94_P10	5.006e-06	1.000e-20
X94_P16	1.894e-06	1.000e-20
X133_P0	2.440e-04	1.000e-20
X133_P4	4.282e-05	1.000e-20
X133_P10	7.132e-06	1.000e-20
X133_P16	2.707e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	1.636e-03	1.584e-03	1.590e-03	1.622e-03
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	2.196e-03	2.108e-03	2.106e-03	2.157e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	3.820e-03	3.614e-03	3.581e-03	3.670e-03
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	5.662e-03	5.367e-03	5.317e-03	5.445e-03
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	7.318e-03	6.939e-03	6.729e-03	6.944e-03
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	9.269e-03	8.777e-03	8.647e-03	8.814e-03
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	1.045e-02	9.857e-03	9.616e-03	9.838e-03
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	1.282e-02	1.205e-02	1.197e-02	1.218e-02
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	1.434e-02	1.359e-02	1.327e-02	1.369e-02
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	1.709e-02	1.599e-02	1.575e-02	1.603e-02
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	2.250e-02	2.095e-02	2.057e-02	2.091e-02
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	3.441e-02	3.261e-02	3.175e-02	3.190e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X4_P0	X4_P4	X4_P10	X4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X7_P0	X7_P4	X7_P10	X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

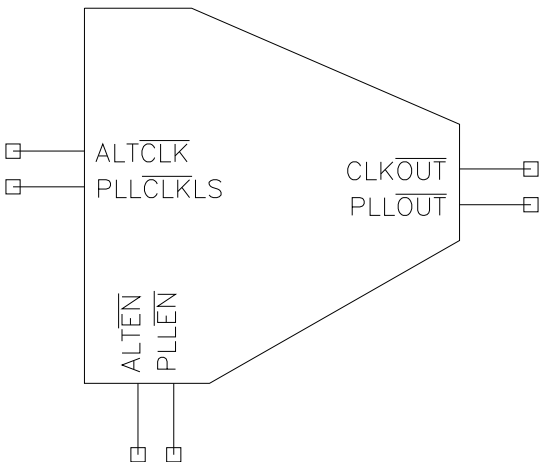
	X22_P0	X22_P4	X22_P10	X22_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X30_P0	X30_P4	X30_P10	X30_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X38_P0	X38_P4	X38_P10	X38_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X44_P0	X44_P4	X44_P10	X44_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X52_P0	X52_P4	X52_P10	X52_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X59_P0	X59_P4	X59_P10	X59_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNGFMUX21

Cell Description

2:1 Glitch-free MUX for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	2.400	2.856	6.8544
X15_P4	2.400	2.856	6.8544
X15_P10	2.400	2.856	6.8544
X15_P16	2.400	2.856	6.8544
X30_P0	2.400	3.944	9.4656
X30_P4	2.400	3.944	9.4656
X30_P10	2.400	3.944	9.4656
X30_P16	2.400	3.944	9.4656

Truth Table

PLL_CLK_LS	ALT_CLK	IPLL_EN_LD	IALT_EN_LD	CLK_OUT
0	-	-	0	0
0	0	-	-	0
-	0	0	-	0
PLL_CLK_LS	1	-	1	1
1	ALT_CLK	1	-	1
1	1	0	0	0

PLL_CLK_LS	PLL_OUT
PLL_CLK_LS	PLL_CLK_LS
1	1

PLL_EN	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

PLL_EN	0	-	PLL_EN
-	-	IPLL_EN_LD	IPLL_EN_LD
-	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

ALT_EN	ALT_CLK	IALT_EN_LD	IALT_EN_LD
ALT_EN	0	-	ALT_EN
-	-	IALT_EN_LD	IALT_EN_LD
-	ALT_CLK	IALT_EN_LD	IALT_EN_LD

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK	0.0024	0.0025	0.0027	0.0029
ALT_EN	0.0006	0.0006	0.0006	0.0006
PLL_CLK_LS	0.0031	0.0032	0.0035	0.0037
PLL_EN	0.0005	0.0005	0.0006	0.0006
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK	0.0037	0.0039	0.0042	0.0044
ALT_EN	0.0006	0.0006	0.0006	0.0006
PLL_CLK_LS	0.0051	0.0054	0.0058	0.0061
PLL_EN	0.0005	0.0005	0.0006	0.0006

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
ALT_CLK to CLK_OUT ↓	0.0268	0.0301	0.9626	1.0288
ALT_CLK to CLK_OUT ↑	0.0198	0.0225	1.2631	1.3726
PLL_CLK_LS to CLK_OUT ↓	0.0242	0.0271	0.9672	1.0347
PLL_CLK_LS to CLK_OUT ↑	0.0193	0.0218	1.2630	1.3741
PLL_CLK_LS to PLL_OUT ↓	0.0202	0.0230	0.9060	0.9643
PLL_CLK_LS to PLL_OUT ↑	0.0170	0.0193	1.0773	1.1683
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
ALT_CLK to CLK_OUT ↓	0.0349	0.0394	1.1251	1.2120
ALT_CLK to CLK_OUT ↑	0.0265	0.0301	1.5327	1.6806
PLL_CLK_LS to CLK_OUT ↓	0.0312	0.0349	1.1314	1.2183
PLL_CLK_LS to CLK_OUT ↑	0.0253	0.0285	1.5352	1.6849
PLL_CLK_LS to PLL_OUT ↓	0.0267	0.0303	1.0468	1.1206
PLL_CLK_LS to PLL_OUT ↑	0.0223	0.0250	1.3022	1.4283
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**

ALT_CLK to CLK_OUT ↓	0.0258	0.0291	0.4992	0.5331
ALT_CLK to CLK_OUT ↑	0.0198	0.0226	0.5670	0.6151
PLL_CLK_LS to CLK_OUT ↓	0.0238	0.0265	0.5044	0.5390
PLL_CLK_LS to CLK_OUT ↑	0.0200	0.0225	0.5701	0.6190
PLL_CLK_LS to PLL_OUT ↓	0.0173	0.0197	0.4629	0.4934
PLL_CLK_LS to PLL_OUT ↑	0.0149	0.0169	0.5409	0.5871
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
ALT_CLK to CLK_OUT ↓	0.0339	0.0380	0.5824	0.6269
ALT_CLK to CLK_OUT ↑	0.0267	0.0302	0.6856	0.7511
PLL_CLK_LS to CLK_OUT ↓	0.0305	0.0340	0.5884	0.6329
PLL_CLK_LS to CLK_OUT ↑	0.0260	0.0291	0.6898	0.7560
PLL_CLK_LS to PLL_OUT ↓	0.0232	0.0262	0.5357	0.5731
PLL_CLK_LS to PLL_OUT ↑	0.0196	0.0220	0.6546	0.7169

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0465	0.0510	0.0554	0.0633
ALT_EN ↓	hold_rising to ALT_CLK	-0.0123	-0.0171	-0.0220	-0.0265
ALT_EN ↑	hold_rising to ALT_CLK	0.0032	-0.0022	-0.0071	-0.0067
ALT_EN ↓	setup_rising to ALT_CLK	0.0397	0.0446	0.0517	0.0592
ALT_EN ↑	setup_rising to ALT_CLK	0.0245	0.0265	0.0319	0.0367
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0465	0.0510	0.0554	0.0634
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0149	-0.0171	-0.0247	-0.0318
PLL_EN ↑	hold_rising to PLL_CLK_LS	0.0032	-0.0022	-0.0045	-0.0067
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0397	0.0446	0.0521	0.0592
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0245	0.0265	0.0319	0.0367
		X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0431	0.0510	0.0554	0.0634
ALT_EN ↓	hold_rising to ALT_CLK	-0.0127	-0.0171	-0.0220	-0.0269

ALT_EN ↑	hold_rising to ALT_CLK	0.0032	-0.0022	-0.0071	-0.0067
ALT_EN ↓	setup_rising to ALT_CLK	0.0397	0.0446	0.0521	0.0592
ALT_EN ↑	setup_rising to ALT_CLK	0.0266	0.0293	0.0368	0.0416
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0431	0.0510	0.0554	0.0634
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0149	-0.0204	-0.0269	-0.0318
PLL_EN ↑	hold_rising to PLL_CLK_LS	-0.0000	-0.0022	-0.0071	-0.0067
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0397	0.0452	0.0521	0.0592
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0266	0.0320	0.0368	0.0443

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X15_P0	1.294e-04	1.000e-20
X15_P4	2.347e-05	1.000e-20
X15_P10	4.331e-06	1.000e-20
X15_P16	1.890e-06	1.000e-20
X30_P0	2.382e-04	1.000e-20
X30_P4	4.221e-05	1.000e-20
X30_P10	7.504e-06	1.000e-20
X30_P16	3.185e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	3.750e-03	3.703e-03	3.759e-03	3.881e-03
ALT_EN (output stable)	2.538e-03	2.493e-03	2.507e-03	2.558e-03
PLL_CLK_LS (output stable)	8.520e-03	7.353e-03	7.237e-03	7.313e-03
PLL_EN (output stable)	2.545e-03	2.492e-03	2.536e-03	2.638e-03
ALT_CLK to CLK_OUT	7.912e-03	7.791e-03	7.958e-03	8.269e-03
PLL_CLK_LS to CLK_OUT	5.077e-03	4.872e-03	6.548e-03	6.709e-03
PLL_CLK_LS to PLL_OUT	7.595e-03	5.849e-03	7.359e-03	7.449e-03
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	4.723e-03	4.689e-03	4.813e-03	5.002e-03
ALT_EN (output stable)	2.806e-03	2.792e-03	2.845e-03	2.911e-03
PLL_CLK_LS (output stable)	1.344e-02	1.139e-02	1.112e-02	1.130e-02

PLL_EN (output stable)	2.907e-03	2.894e-03	2.991e-03	3.126e-03
ALT_CLK to CLK_OUT	1.402e-02	1.395e-02	1.441e-02	1.483e-02
PLL_CLK_LS to CLK_OUT	9.072e-03	8.704e-03	8.706e-03	8.874e-03
PLL_CLK_LS to PLL_OUT	1.356e-02	1.032e-02	9.696e-03	9.683e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

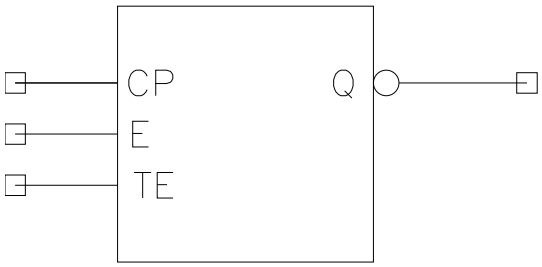
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
ALT_CLK (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_CLK to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to PLL_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_CLK to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to PLL_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNHLS

Cell Description

Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LLP_-CNHLSX7_P0	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX7_P4	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX7_P10	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX7_P16	1.200	1.768	2.1216
C12T28SOI_LLP_-CNHLSX15_P0	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX15_P4	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX15_P10	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX15_P16	1.200	1.904	2.2848
C12T28SOI_LLP_-CNHLSX22_P0	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX22_P4	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX22_P10	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX22_P16	1.200	2.312	2.7744
C12T28SOI_LLP_-CNHLSX29_P0	1.200	2.448	2.9376
C12T28SOI_LLP_-CNHLSX29_P4	1.200	2.448	2.9376
C12T28SOI_LLP_-CNHLSX29_P10	1.200	2.448	2.9376
C12T28SOI_LLP_-CNHLSX29_P16	1.200	2.448	2.9376

C12T28SOI_LLP_-CNHLSX36_P0	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX36_P4	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX36_P10	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX36_P16	1.200	2.584	3.1008
C12T28SOI_LLP_-CNHLSX51_P0	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX51_P4	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX51_P10	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX51_P16	1.200	3.128	3.7536
C12T28SOI_LLP_-CNHLSX58_P0	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX58_P4	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX58_P10	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX58_P16	1.200	3.808	4.5696
C12T28SOI_LLP_-CNHLSX71_P0	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX71_P4	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX71_P10	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX71_P16	1.200	4.352	5.2224
C12T28SOI_LLP_-CNHLSX93_P0	1.200	4.896	5.8752
C12T28SOI_LLP_-CNHLSX93_P4	1.200	4.896	5.8752
C12T28SOI_LLP_-CNHLSX93_P10	1.200	4.896	5.8752
C12T28SOI_LLP_-CNHLSX93_P16	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX29_P0	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX29_P4	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX29_P10	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX29_P16	1.200	2.992	3.5904
C12T28SOI_LLPHP_-CNHLSX36_P0	1.200	3.128	3.7536
C12T28SOI_LLPHP_-CNHLSX36_P4	1.200	3.128	3.7536

C12T28SOI_LLPHP_-CNHLSX36_P10	1.200	3.128	3.7536
C12T28SOI_LLPHP_-CNHLSX36_P16	1.200	3.128	3.7536
C12T28SOI_LLPHP_-CNHLSX44_P0	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX44_P4	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX44_P10	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX44_P16	1.200	3.536	4.2432
C12T28SOI_LLPHP_-CNHLSX51_P0	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX51_P4	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX51_P10	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX51_P16	1.200	3.672	4.4064
C12T28SOI_LLPHP_-CNHLSX58_P0	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX58_P4	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX58_P10	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX58_P16	1.200	4.352	5.2224
C12T28SOI_LLPHP_-CNHLSX71_P0	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX71_P4	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX71_P10	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX71_P16	1.200	4.896	5.8752
C12T28SOI_LLPHP_-CNHLSX86_P0	1.200	5.304	6.3648
C12T28SOI_LLPHP_-CNHLSX86_P4	1.200	5.304	6.3648
C12T28SOI_LLPHP_-CNHLSX86_P10	1.200	5.304	6.3648
C12T28SOI_LLPHP_-CNHLSX86_P16	1.200	5.304	6.3648

Truth Table

CP	E	TE	OLDIE	Q
0	-	-	-	0
1	-	-	OLDIE	OLDIE

OLDIE	OLDIE
OLDIE	OLDIE

Pin Capacitance

Pin	C12T28SOI_LLP_-CNHLSX7_P0	C12T28SOI_LLP_-CNHLSX7_P4	C12T28SOI_LLP_-CNHLSX7_P10	C12T28SOI_LLP_-CNHLSX7_P16
CP	0.0020	0.0021	0.0022	0.0023
E	0.0005	0.0005	0.0006	0.0006
TE	0.0010	0.0010	0.0011	0.0011
	C12T28SOI_LLP_-CNHLSX15_P0	C12T28SOI_LLP_-CNHLSX15_P4	C12T28SOI_LLP_-CNHLSX15_P10	C12T28SOI_LLP_-CNHLSX15_P16
CP	0.0026	0.0027	0.0029	0.0030
E	0.0005	0.0005	0.0006	0.0006
TE	0.0010	0.0010	0.0011	0.0011
	C12T28SOI_LLP_-CNHLSX22_P0	C12T28SOI_LLP_-CNHLSX22_P4	C12T28SOI_LLP_-CNHLSX22_P10	C12T28SOI_LLP_-CNHLSX22_P16
CP	0.0028	0.0029	0.0030	0.0032
E	0.0005	0.0005	0.0006	0.0006
TE	0.0010	0.0010	0.0011	0.0011
	C12T28SOI_LLP_-CNHLSX29_P0	C12T28SOI_LLP_-CNHLSX29_P4	C12T28SOI_LLP_-CNHLSX29_P10	C12T28SOI_LLP_-CNHLSX29_P16
CP	0.0030	0.0031	0.0033	0.0036
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0010	0.0011	0.0011
	C12T28SOI_LLP_-CNHLSX36_P0	C12T28SOI_LLP_-CNHLSX36_P4	C12T28SOI_LLP_-CNHLSX36_P10	C12T28SOI_LLP_-CNHLSX36_P16
CP	0.0033	0.0034	0.0037	0.0039
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0010	0.0011	0.0011
	C12T28SOI_LLP_-CNHLSX51_P0	C12T28SOI_LLP_-CNHLSX51_P4	C12T28SOI_LLP_-CNHLSX51_P10	C12T28SOI_LLP_-CNHLSX51_P16
CP	0.0039	0.0041	0.0043	0.0046
E	0.0005	0.0005	0.0006	0.0006
TE	0.0010	0.0010	0.0011	0.0011
	C12T28SOI_LLP_-CNHLSX58_P0	C12T28SOI_LLP_-CNHLSX58_P4	C12T28SOI_LLP_-CNHLSX58_P10	C12T28SOI_LLP_-CNHLSX58_P16
CP	0.0054	0.0056	0.0059	0.0064
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0010	0.0010	0.0011
	C12T28SOI_LLP_-CNHLSX71_P0	C12T28SOI_LLP_-CNHLSX71_P4	C12T28SOI_LLP_-CNHLSX71_P10	C12T28SOI_LLP_-CNHLSX71_P16
CP	0.0061	0.0064	0.0069	0.0074
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0010	0.0010	0.0011
	C12T28SOI_LLP_-CNHLSX93_P0	C12T28SOI_LLP_-CNHLSX93_P4	C12T28SOI_LLP_-CNHLSX93_P10	C12T28SOI_LLP_-CNHLSX93_P16
CP	0.0072	0.0075	0.0082	0.0087
E	0.0005	0.0005	0.0006	0.0006
TE	0.0009	0.0010	0.0011	0.0011
	C12T28SOI_LLPHP_-CNHLSX29_P0	C12T28SOI_LLPHP_-CNHLSX29_P4	C12T28SOI_LLPHP_-CNHLSX29_P10	C12T28SOI_LLPHP_-CNHLSX29_P16
CP	0.0023	0.0024	0.0027	0.0029
E	0.0006	0.0006	0.0007	0.0007
TE	0.0009	0.0009	0.0010	0.0011
	C12T28SOI_LLPHP_-CNHLSX36_P0	C12T28SOI_LLPHP_-CNHLSX36_P4	C12T28SOI_LLPHP_-CNHLSX36_P10	C12T28SOI_LLPHP_-CNHLSX36_P16

CP	0.0026	0.0028	0.0030	0.0032
E	0.0006	0.0006	0.0007	0.0007
TE	0.0009	0.0009	0.0010	0.0011
	C12T28SOI_LLPHP_-CNHLSX44_P0	C12T28SOI_LLPHP_-CNHLSX44_P4	C12T28SOI_LLPHP_-CNHLSX44_P10	C12T28SOI_LLPHP_-CNHLSX44_P16
CP	0.0032	0.0033	0.0035	0.0037
E	0.0006	0.0006	0.0007	0.0007
TE	0.0009	0.0009	0.0010	0.0011
	C12T28SOI_LLPHP_-CNHLSX51_P0	C12T28SOI_LLPHP_-CNHLSX51_P4	C12T28SOI_LLPHP_-CNHLSX51_P10	C12T28SOI_LLPHP_-CNHLSX51_P16
CP	0.0032	0.0033	0.0035	0.0037
E	0.0006	0.0006	0.0007	0.0007
TE	0.0009	0.0009	0.0010	0.0011
	C12T28SOI_LLPHP_-CNHLSX58_P0	C12T28SOI_LLPHP_-CNHLSX58_P4	C12T28SOI_LLPHP_-CNHLSX58_P10	C12T28SOI_LLPHP_-CNHLSX58_P16
CP	0.0043	0.0045	0.0049	0.0052
E	0.0006	0.0006	0.0007	0.0007
TE	0.0009	0.0009	0.0010	0.0011
	C12T28SOI_LLPHP_-CNHLSX71_P0	C12T28SOI_LLPHP_-CNHLSX71_P4	C12T28SOI_LLPHP_-CNHLSX71_P10	C12T28SOI_LLPHP_-CNHLSX71_P16
CP	0.0053	0.0056	0.0059	0.0064
E	0.0006	0.0006	0.0007	0.0007
TE	0.0009	0.0009	0.0010	0.0011
	C12T28SOI_LLPHP_-CNHLSX86_P0	C12T28SOI_LLPHP_-CNHLSX86_P4	C12T28SOI_LLPHP_-CNHLSX86_P10	C12T28SOI_LLPHP_-CNHLSX86_P16
CP	0.0063	0.0067	0.0072	0.0077
E	0.0006	0.0006	0.0007	0.0007
TE	0.0009	0.0009	0.0010	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LLP_-CNHLSX7_P0	**C12T28SOI_LLP_-CNHLSX7_P4**	**C12T28SOI_LLP_-CNHLSX7_P0**	**C12T28SOI_LLP_-CNHLSX7_P4**
CP to Q ↓	0.0245	0.0277	1.8949	2.0197
CP to Q ↑	0.0184	0.0209	2.1573	2.3418
	C12T28SOI_LLP_-CNHLSX7_P10	**C12T28SOI_LLP_-CNHLSX7_P16**	**C12T28SOI_LLP_-CNHLSX7_P10**	**C12T28SOI_LLP_-CNHLSX7_P16**
CP to Q ↓	0.0323	0.0364	2.1944	2.3521
CP to Q ↑	0.0244	0.0274	2.6122	2.8647
	C12T28SOI_LLP_-CNHLSX15_P0	**C12T28SOI_LLP_-CNHLSX15_P4**	**C12T28SOI_LLP_-CNHLSX15_P0**	**C12T28SOI_LLP_-CNHLSX15_P4**
CP to Q ↓	0.0208	0.0234	0.9517	1.0122
CP to Q ↑	0.0175	0.0197	1.0868	1.1779
	C12T28SOI_LLP_-CNHLSX15_P10	**C12T28SOI_LLP_-CNHLSX15_P16**	**C12T28SOI_LLP_-CNHLSX15_P10**	**C12T28SOI_LLP_-CNHLSX15_P16**
CP to Q ↓	0.0273	0.0306	1.0992	1.1768
CP to Q ↑	0.0230	0.0257	1.3139	1.4413
	C12T28SOI_LLP_-CNHLSX22_P0	**C12T28SOI_LLP_-CNHLSX22_P4**	**C12T28SOI_LLP_-CNHLSX22_P0**	**C12T28SOI_LLP_-CNHLSX22_P4**
CP to Q ↓	0.0209	0.0236	0.6591	0.7022
CP to Q ↑	0.0188	0.0211	0.7328	0.7955
	C12T28SOI_LLP_-CNHLSX22_P10	**C12T28SOI_LLP_-CNHLSX22_P16**	**C12T28SOI_LLP_-CNHLSX22_P10**	**C12T28SOI_LLP_-CNHLSX22_P16**

CP to Q ↓	0.0273	0.0311	0.7635	0.8179
CP to Q ↑	0.0244	0.0276	0.8873	0.9729
	C12T28SOI_LLP_-CNHLSX29_P0	**C12T28SOI_LLP_-CNHLSX29_P4**	**C12T28SOI_LLP_-CNHLSX29_P0**	**C12T28SOI_LLP_-CNHLSX29_P4**
CP to Q ↓	0.0209	0.0236	0.4930	0.5259
CP to Q ↑	0.0186	0.0210	0.5494	0.5972
	C12T28SOI_LLP_-CNHLSX29_P10	**C12T28SOI_LLP_-CNHLSX29_P16**	**C12T28SOI_LLP_-CNHLSX29_P10**	**C12T28SOI_LLP_-CNHLSX29_P16**
CP to Q ↓	0.0273	0.0310	0.5722	0.6127
CP to Q ↑	0.0241	0.0274	0.6654	0.7298
	C12T28SOI_LLP_-CNHLSX36_P0	**C12T28SOI_LLP_-CNHLSX36_P4**	**C12T28SOI_LLP_-CNHLSX36_P0**	**C12T28SOI_LLP_-CNHLSX36_P4**
CP to Q ↓	0.0207	0.0234	0.3943	0.4203
CP to Q ↑	0.0184	0.0207	0.4403	0.4782
	C12T28SOI_LLP_-CNHLSX36_P10	**C12T28SOI_LLP_-CNHLSX36_P16**	**C12T28SOI_LLP_-CNHLSX36_P10**	**C12T28SOI_LLP_-CNHLSX36_P16**
CP to Q ↓	0.0273	0.0310	0.4569	0.4896
CP to Q ↑	0.0241	0.0273	0.5333	0.5847
	C12T28SOI_LLP_-CNHLSX51_P0	**C12T28SOI_LLP_-CNHLSX51_P4**	**C12T28SOI_LLP_-CNHLSX51_P0**	**C12T28SOI_LLP_-CNHLSX51_P4**
CP to Q ↓	0.0226	0.0255	0.2869	0.3062
CP to Q ↑	0.0191	0.0216	0.3163	0.3436
	C12T28SOI_LLP_-CNHLSX51_P10	**C12T28SOI_LLP_-CNHLSX51_P16**	**C12T28SOI_LLP_-CNHLSX51_P10**	**C12T28SOI_LLP_-CNHLSX51_P16**
CP to Q ↓	0.0297	0.0335	0.3330	0.3569
CP to Q ↑	0.0251	0.0282	0.3830	0.4199
	C12T28SOI_LLP_-CNHLSX58_P0	**C12T28SOI_LLP_-CNHLSX58_P4**	**C12T28SOI_LLP_-CNHLSX58_P0**	**C12T28SOI_LLP_-CNHLSX58_P4**
CP to Q ↓	0.0197	0.0223	0.2532	0.2699
CP to Q ↑	0.0167	0.0188	0.2779	0.3019
	C12T28SOI_LLP_-CNHLSX58_P10	**C12T28SOI_LLP_-CNHLSX58_P16**	**C12T28SOI_LLP_-CNHLSX58_P10**	**C12T28SOI_LLP_-CNHLSX58_P16**
CP to Q ↓	0.0259	0.0292	0.2931	0.3139
CP to Q ↑	0.0217	0.0244	0.3362	0.3684
	C12T28SOI_LLP_-CNHLSX71_P0	**C12T28SOI_LLP_-CNHLSX71_P4**	**C12T28SOI_LLP_-CNHLSX71_P0**	**C12T28SOI_LLP_-CNHLSX71_P4**
CP to Q ↓	0.0192	0.0218	0.2097	0.2233
CP to Q ↑	0.0170	0.0192	0.2267	0.2462
	C12T28SOI_LLP_-CNHLSX71_P10	**C12T28SOI_LLP_-CNHLSX71_P16**	**C12T28SOI_LLP_-CNHLSX71_P10**	**C12T28SOI_LLP_-CNHLSX71_P16**
CP to Q ↓	0.0255	0.0286	0.2429	0.2600
CP to Q ↑	0.0223	0.0249	0.2744	0.3008
	C12T28SOI_LLP_-CNHLSX93_P0	**C12T28SOI_LLP_-CNHLSX93_P4**	**C12T28SOI_LLP_-CNHLSX93_P0**	**C12T28SOI_LLP_-CNHLSX93_P4**
CP to Q ↓	0.0205	0.0229	0.1658	0.1767
CP to Q ↑	0.0184	0.0204	0.1797	0.1953
	C12T28SOI_LLP_-CNHLSX93_P10	**C12T28SOI_LLP_-CNHLSX93_P16**	**C12T28SOI_LLP_-CNHLSX93_P10**	**C12T28SOI_LLP_-CNHLSX93_P16**
CP to Q ↓	0.0267	0.0301	0.1923	0.2062
CP to Q ↑	0.0237	0.0266	0.2174	0.2388
	C12T28SOI_-LLPHP_-CNHLSX29_P0	**C12T28SOI_-LLPHP_-CNHLSX29_P4**	**C12T28SOI_-LLPHP_-CNHLSX29_P0**	**C12T28SOI_-LLPHP_-CNHLSX29_P4**

CP to Q ↓	0.0199	0.0225	0.5017	0.5341
CP to Q ↑	0.0178	0.0200	0.5596	0.6057
	C12T28SOI_-LLPHP_-CNHLSX29_P10	**C12T28SOI_-LLPHP_-CNHLSX29_P16**	**C12T28SOI_-LLPHP_-CNHLSX29_P10**	**C12T28SOI_-LLPHP_-CNHLSX29_P16**
CP to Q ↓	0.0261	0.0295	0.5804	0.6215
CP to Q ↑	0.0231	0.0260	0.6734	0.7365
	C12T28SOI_-LLPHP_-CNHLSX36_P0	**C12T28SOI_-LLPHP_-CNHLSX36_P4**	**C12T28SOI_-LLPHP_-CNHLSX36_P0**	**C12T28SOI_-LLPHP_-CNHLSX36_P4**
CP to Q ↓	0.0197	0.0223	0.4006	0.4261
CP to Q ↑	0.0176	0.0199	0.4505	0.4879
	C12T28SOI_-LLPHP_-CNHLSX36_P10	**C12T28SOI_-LLPHP_-CNHLSX36_P16**	**C12T28SOI_-LLPHP_-CNHLSX36_P10**	**C12T28SOI_-LLPHP_-CNHLSX36_P16**
CP to Q ↓	0.0260	0.0294	0.4630	0.4958
CP to Q ↑	0.0231	0.0260	0.5426	0.5936
	C12T28SOI_-LLPHP_-CNHLSX44_P0	**C12T28SOI_-LLPHP_-CNHLSX44_P4**	**C12T28SOI_-LLPHP_-CNHLSX44_P0**	**C12T28SOI_-LLPHP_-CNHLSX44_P4**
CP to Q ↓	0.0199	0.0223	0.3347	0.3564
CP to Q ↑	0.0172	0.0192	0.3763	0.4070
	C12T28SOI_-LLPHP_-CNHLSX44_P10	**C12T28SOI_-LLPHP_-CNHLSX44_P16**	**C12T28SOI_-LLPHP_-CNHLSX44_P10**	**C12T28SOI_-LLPHP_-CNHLSX44_P16**
CP to Q ↓	0.0260	0.0291	0.3867	0.4138
CP to Q ↑	0.0223	0.0248	0.4524	0.4943
	C12T28SOI_-LLPHP_-CNHLSX51_P0	**C12T28SOI_-LLPHP_-CNHLSX51_P4**	**C12T28SOI_-LLPHP_-CNHLSX51_P0**	**C12T28SOI_-LLPHP_-CNHLSX51_P4**
CP to Q ↓	0.0213	0.0240	0.2898	0.3088
CP to Q ↑	0.0185	0.0207	0.3246	0.3513
	C12T28SOI_-LLPHP_-CNHLSX51_P10	**C12T28SOI_-LLPHP_-CNHLSX51_P16**	**C12T28SOI_-LLPHP_-CNHLSX51_P10**	**C12T28SOI_-LLPHP_-CNHLSX51_P16**
CP to Q ↓	0.0276	0.0313	0.3351	0.3587
CP to Q ↑	0.0237	0.0267	0.3904	0.4269
	C12T28SOI_-LLPHP_-CNHLSX58_P0	**C12T28SOI_-LLPHP_-CNHLSX58_P4**	**C12T28SOI_-LLPHP_-CNHLSX58_P0**	**C12T28SOI_-LLPHP_-CNHLSX58_P4**
CP to Q ↓	0.0185	0.0208	0.2532	0.2694
CP to Q ↑	0.0158	0.0178	0.2859	0.3093
	C12T28SOI_-LLPHP_-CNHLSX58_P10	**C12T28SOI_-LLPHP_-CNHLSX58_P16**	**C12T28SOI_-LLPHP_-CNHLSX58_P10**	**C12T28SOI_-LLPHP_-CNHLSX58_P16**
CP to Q ↓	0.0241	0.0275	0.2921	0.3126
CP to Q ↑	0.0205	0.0233	0.3434	0.3754
	C12T28SOI_-LLPHP_-CNHLSX71_P0	**C12T28SOI_-LLPHP_-CNHLSX71_P4**	**C12T28SOI_-LLPHP_-CNHLSX71_P0**	**C12T28SOI_-LLPHP_-CNHLSX71_P4**
CP to Q ↓	0.0183	0.0209	0.2108	0.2244
CP to Q ↑	0.0164	0.0186	0.2328	0.2520

	C12T28SOI_-LLPHP_-CNHLSX71_P10	C12T28SOI_-LLPHP_-CNHLSX71_P16	C12T28SOI_-LLPHP_-CNHLSX71_P10	C12T28SOI_-LLPHP_-CNHLSX71_P16
CP to Q ↓	0.0241	0.0274	0.2434	0.2605
CP to Q ↑	0.0213	0.0241	0.2797	0.3060
	C12T28SOI_-LLPHP_-CNHLSX86_P0	**C12T28SOI_-LLPHP_-CNHLSX86_P4**	**C12T28SOI_-LLPHP_-CNHLSX86_P0**	**C12T28SOI_-LLPHP_-CNHLSX86_P4**
CP to Q ↓	0.0180	0.0204	0.1785	0.1898
CP to Q ↑	0.0165	0.0185	0.1969	0.2130
	C12T28SOI_-LLPHP_-CNHLSX86_P10	**C12T28SOI_-LLPHP_-CNHLSX86_P16**	**C12T28SOI_-LLPHP_-CNHLSX86_P10**	**C12T28SOI_-LLPHP_-CNHLSX86_P16**
CP to Q ↓	0.0237	0.0268	0.2059	0.2204
CP to Q ↑	0.0214	0.0240	0.2365	0.2587

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C12T28SOI_-LLP_CNHLSX7_-P0	C12T28SOI_-LLP_CNHLSX7_-P4	C12T28SOI_-LLP_CNHLSX7_-P10	C12T28SOI_-LLP_CNHLSX7_-P16
CP ↓	min_pulse_width to CP	0.0256	0.0295	0.0357	0.0378
E ↓	hold_rising to CP	-0.0061	-0.0052	-0.0132	-0.0181
E ↑	hold_rising to CP	0.0107	0.0085	0.0032	0.0036
E ↓	setup_rising to CP	0.0311	0.0328	0.0372	0.0421
E ↑	setup_rising to CP	0.0190	0.0216	0.0270	0.0287
TE ↓	hold_rising to CP	-0.0035	-0.0052	-0.0101	-0.0149
TE ↑	hold_rising to CP	0.0085	0.0058	0.0036	0.0010
TE ↓	setup_rising to CP	0.0280	0.0334	0.0350	0.0421
TE ↑	setup_rising to CP	0.0190	0.0216	0.0270	0.0318
		C12T28SOI_-LLP_-CNHLSX15_P0	C12T28SOI_-LLP_-CNHLSX15_P4	C12T28SOI_-LLP_-CNHLSX15_P10	C12T28SOI_-LLP_-CNHLSX15_P16
CP ↓	min_pulse_width to CP	0.0256	0.0295	0.0333	0.0361
E ↓	hold_rising to CP	-0.0061	-0.0052	-0.0132	-0.0181
E ↑	hold_rising to CP	0.0107	0.0085	0.0032	0.0036
E ↓	setup_rising to CP	0.0311	0.0328	0.0372	0.0421
E ↑	setup_rising to CP	0.0191	0.0217	0.0270	0.0319
TE ↓	hold_rising to CP	-0.0035	-0.0052	-0.0101	-0.0149
TE ↑	hold_rising to CP	0.0085	0.0058	0.0036	0.0014
TE ↓	setup_rising to CP	0.0280	0.0334	0.0377	0.0421
TE ↑	setup_rising to CP	0.0190	0.0212	0.0265	0.0318

		C12T28SOI_-LLP_-CNHLSX22_P0	C12T28SOI_-LLP_-CNHLSX22_P4	C12T28SOI_-LLP_-CNHLSX22_P10	C12T28SOI_-LLP_-CNHLSX22_P16
CP ↓	min_pulse_width to CP	0.0263	0.0301	0.0357	0.0402
E ↓	hold_rising to CP	-0.0052	-0.0106	-0.0123	-0.0198
E ↑	hold_rising to CP	0.0085	0.0058	0.0036	0.0010
E ↓	setup_rising to CP	0.0327	0.0350	0.0426	0.0475
E ↑	setup_rising to CP	0.0190	0.0244	0.0261	0.0345
TE ↓	hold_rising to CP	-0.0056	-0.0105	-0.0155	-0.0204
TE ↑	hold_rising to CP	0.0058	0.0036	0.0036	-0.0018
TE ↓	setup_rising to CP	0.0334	0.0350	0.0399	0.0474
TE ↑	setup_rising to CP	0.0216	0.0270	0.0319	0.0335
		C12T28SOI_-LLP_-CNHLSX29_P0	C12T28SOI_-LLP_-CNHLSX29_P4	C12T28SOI_-LLP_-CNHLSX29_P10	C12T28SOI_-LLP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0297	0.0318	0.0357	0.0402
E ↓	hold_rising to CP	-0.0052	-0.0106	-0.0181	-0.0194
E ↑	hold_rising to CP	0.0085	0.0058	0.0036	0.0010
E ↓	setup_rising to CP	0.0359	0.0376	0.0420	0.0469
E ↑	setup_rising to CP	0.0190	0.0244	0.0293	0.0341
TE ↓	hold_rising to CP	-0.0052	-0.0101	-0.0149	-0.0198
TE ↑	hold_rising to CP	0.0058	0.0036	0.0036	-0.0018
TE ↓	setup_rising to CP	0.0334	0.0350	0.0421	0.0469
TE ↑	setup_rising to CP	0.0216	0.0270	0.0319	0.0367
		C12T28SOI_-LLP_-CNHLSX36_P0	C12T28SOI_-LLP_-CNHLSX36_P4	C12T28SOI_-LLP_-CNHLSX36_P10	C12T28SOI_-LLP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0297	0.0318	0.0357	0.0402
E ↓	hold_rising to CP	-0.0052	-0.0101	-0.0181	-0.0226
E ↑	hold_rising to CP	0.0085	0.0058	0.0036	0.0010
E ↓	setup_rising to CP	0.0359	0.0376	0.0420	0.0469
E ↑	setup_rising to CP	0.0190	0.0244	0.0261	0.0341
TE ↓	hold_rising to CP	-0.0084	-0.0101	-0.0149	-0.0198
TE ↑	hold_rising to CP	0.0058	0.0036	0.0036	-0.0018
TE ↓	setup_rising to CP	0.0334	0.0350	0.0421	0.0469
TE ↑	setup_rising to CP	0.0216	0.0270	0.0319	0.0367

		C12T28SOI_-LLP_-CNHLSX51_P0	C12T28SOI_-LLP_-CNHLSX51_P4	C12T28SOI_-LLP_-CNHLSX51_P10	C12T28SOI_-LLP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0273	0.0301	0.0356	0.0401
E ↓	hold_rising to CP	-0.0057	-0.0078	-0.0123	-0.0171
E ↑	hold_rising to CP	0.0085	0.0058	0.0036	0.0036
E ↓	setup_rising to CP	0.0301	0.0355	0.0430	0.0475
E ↑	setup_rising to CP	0.0190	0.0244	0.0293	0.0336
TE ↓	hold_rising to CP	-0.0056	-0.0084	-0.0159	-0.0204
TE ↑	hold_rising to CP	0.0058	0.0032	0.0036	0.0014
TE ↓	setup_rising to CP	0.0302	0.0351	0.0399	0.0448
TE ↑	setup_rising to CP	0.0216	0.0270	0.0319	0.0367
		C12T28SOI_-LLP_-CNHLSX58_P0	C12T28SOI_-LLP_-CNHLSX58_P4	C12T28SOI_-LLP_-CNHLSX58_P10	C12T28SOI_-LLP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0297	0.0342	0.0388	0.0433
E ↓	hold_rising to CP	-0.0110	-0.0127	-0.0171	-0.0247
E ↑	hold_rising to CP	0.0058	0.0058	0.0036	0.0014
E ↓	setup_rising to CP	0.0355	0.0372	0.0420	0.0528
E ↑	setup_rising to CP	0.0217	0.0265	0.0319	0.0368
TE ↓	hold_rising to CP	-0.0084	-0.0133	-0.0208	-0.0252
TE ↑	hold_rising to CP	0.0058	0.0036	0.0010	-0.0018
TE ↓	setup_rising to CP	0.0355	0.0409	0.0453	0.0502
TE ↑	setup_rising to CP	0.0244	0.0265	0.0319	0.0389
		C12T28SOI_-LLP_-CNHLSX71_P0	C12T28SOI_-LLP_-CNHLSX71_P4	C12T28SOI_-LLP_-CNHLSX71_P10	C12T28SOI_-LLP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0297	0.0325	0.0388	0.0433
E ↓	hold_rising to CP	-0.0110	-0.0127	-0.0171	-0.0247
E ↑	hold_rising to CP	0.0058	0.0058	0.0036	0.0014
E ↓	setup_rising to CP	0.0355	0.0404	0.0479	0.0523
E ↑	setup_rising to CP	0.0217	0.0265	0.0319	0.0368
TE ↓	hold_rising to CP	-0.0084	-0.0133	-0.0208	-0.0252
TE ↑	hold_rising to CP	0.0058	0.0036	0.0010	-0.0013
TE ↓	setup_rising to CP	0.0355	0.0409	0.0453	0.0528
TE ↑	setup_rising to CP	0.0244	0.0265	0.0335	0.0384

		C12T28SOI_-LLP_-CNHLSX93_P0	C12T28SOI_-LLP_-CNHLSX93_P4	C12T28SOI_-LLP_-CNHLSX93_P10	C12T28SOI_-LLP_-CNHLSX93_P16
CP ↓	min_pulse_width to CP	0.0303	0.0342	0.0394	0.0474
E ↓	hold_rising to CP	-0.0106	-0.0155	-0.0230	-0.0279
E ↑	hold_rising to CP	0.0058	0.0058	0.0036	0.0014
E ↓	setup_rising to CP	0.0350	0.0404	0.0479	0.0523
E ↑	setup_rising to CP	0.0245	0.0265	0.0368	0.0417
TE ↓	hold_rising to CP	-0.0105	-0.0159	-0.0204	-0.0279
TE ↑	hold_rising to CP	0.0058	0.0036	0.0010	-0.0013
TE ↓	setup_rising to CP	0.0350	0.0399	0.0448	0.0523
TE ↑	setup_rising to CP	0.0239	0.0293	0.0368	0.0416
		C12T28SOI_-LLPHP_-CNHLSX29_P0	C12T28SOI_-LLPHP_-CNHLSX29_P4	C12T28SOI_-LLPHP_-CNHLSX29_P10	C12T28SOI_-LLPHP_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0325	0.0371	0.0441	0.0493
E ↓	hold_rising to CP	0.0085	0.0026	0.0004	-0.0018
E ↑	hold_rising to CP	0.0243	0.0243	0.0276	0.0270
E ↓	setup_rising to CP	0.0268	0.0289	0.0343	0.0392
E ↑	setup_rising to CP	0.0151	0.0200	0.0222	0.0271
TE ↓	hold_rising to CP	0.0048	0.0026	0.0030	-0.0023
TE ↑	hold_rising to CP	0.0248	0.0248	0.0248	0.0270
TE ↓	setup_rising to CP	0.0273	0.0296	0.0317	0.0392
TE ↑	setup_rising to CP	0.0142	0.0200	0.0216	0.0270
		C12T28SOI_-LLPHP_-CNHLSX36_P0	C12T28SOI_-LLPHP_-CNHLSX36_P4	C12T28SOI_-LLPHP_-CNHLSX36_P10	C12T28SOI_-LLPHP_-CNHLSX36_P16
CP ↓	min_pulse_width to CP	0.0325	0.0371	0.0441	0.0493
E ↓	hold_rising to CP	0.0085	0.0026	0.0004	-0.0018
E ↑	hold_rising to CP	0.0243	0.0243	0.0276	0.0270
E ↓	setup_rising to CP	0.0268	0.0289	0.0343	0.0392
E ↑	setup_rising to CP	0.0151	0.0200	0.0222	0.0271
TE ↓	hold_rising to CP	0.0048	0.0026	0.0030	-0.0023
TE ↑	hold_rising to CP	0.0248	0.0248	0.0248	0.0270
TE ↓	setup_rising to CP	0.0273	0.0296	0.0344	0.0392
TE ↑	setup_rising to CP	0.0142	0.0200	0.0216	0.0270

		C12T28SOI_-LLPHP_-CNHLSX44_P0	C12T28SOI_-LLPHP_-CNHLSX44_P4	C12T28SOI_-LLPHP_-CNHLSX44_P10	C12T28SOI_-LLPHP_-CNHLSX44_P16
CP ↓	min_pulse_width to CP	0.0325	0.0371	0.0448	0.0527
E ↓	hold_rising to CP	0.0085	0.0026	0.0004	-0.0045
E ↑	hold_rising to CP	0.0243	0.0243	0.0276	0.0270
E ↓	setup_rising to CP	0.0268	0.0317	0.0339	0.0387
E ↑	setup_rising to CP	0.0146	0.0200	0.0249	0.0271
TE ↓	hold_rising to CP	0.0053	0.0026	0.0009	-0.0023
TE ↑	hold_rising to CP	0.0248	0.0248	0.0248	0.0270
TE ↓	setup_rising to CP	0.0264	0.0322	0.0371	0.0419
TE ↑	setup_rising to CP	0.0142	0.0200	0.0244	0.0319
		C12T28SOI_-LLPHP_-CNHLSX51_P0	C12T28SOI_-LLPHP_-CNHLSX51_P4	C12T28SOI_-LLPHP_-CNHLSX51_P10	C12T28SOI_-LLPHP_-CNHLSX51_P16
CP ↓	min_pulse_width to CP	0.0324	0.0370	0.0448	0.0510
E ↓	hold_rising to CP	0.0059	0.0026	0.0004	-0.0045
E ↑	hold_rising to CP	0.0243	0.0243	0.0276	0.0270
E ↓	setup_rising to CP	0.0268	0.0289	0.0343	0.0392
E ↑	setup_rising to CP	0.0146	0.0200	0.0249	0.0271
TE ↓	hold_rising to CP	0.0053	0.0026	0.0036	-0.0019
TE ↑	hold_rising to CP	0.0248	0.0248	0.0248	0.0270
TE ↓	setup_rising to CP	0.0273	0.0296	0.0338	0.0392
TE ↑	setup_rising to CP	0.0142	0.0200	0.0271	0.0319
		C12T28SOI_-LLPHP_-CNHLSX58_P0	C12T28SOI_-LLPHP_-CNHLSX58_P4	C12T28SOI_-LLPHP_-CNHLSX58_P10	C12T28SOI_-LLPHP_-CNHLSX58_P16
CP ↓	min_pulse_width to CP	0.0332	0.0371	0.0448	0.0534
E ↓	hold_rising to CP	0.0026	0.0031	0.0004	-0.0045
E ↑	hold_rising to CP	0.0243	0.0243	0.0276	0.0270
E ↓	setup_rising to CP	0.0321	0.0343	0.0392	0.0440
E ↑	setup_rising to CP	0.0146	0.0200	0.0249	0.0265
TE ↓	hold_rising to CP	0.0053	0.0026	-0.0023	-0.0045
TE ↑	hold_rising to CP	0.0248	0.0248	0.0248	0.0270
TE ↓	setup_rising to CP	0.0296	0.0312	0.0366	0.0441
TE ↑	setup_rising to CP	0.0142	0.0196	0.0271	0.0319

		C12T28SOI_-LLPHP_-CNHLSX71_P0	C12T28SOI_-LLPHP_-CNHLSX71_P4	C12T28SOI_-LLPHP_-CNHLSX71_P10	C12T28SOI_-LLPHP_-CNHLSX71_P16
CP ↓	min_pulse_width to CP	0.0356	0.0402	0.0489	0.0558
E ↓	hold_rising to CP	0.0031	0.0010	-0.0045	-0.0067
E ↑	hold_rising to CP	0.0248	0.0248	0.0243	0.0270
E ↓	setup_rising to CP	0.0317	0.0366	0.0441	0.0489
E ↑	setup_rising to CP	0.0200	0.0217	0.0271	0.0319
TE ↓	hold_rising to CP	0.0032	0.0004	-0.0018	-0.0072
TE ↑	hold_rising to CP	0.0253	0.0222	0.0221	0.0248
TE ↓	setup_rising to CP	0.0312	0.0371	0.0415	0.0463
TE ↑	setup_rising to CP	0.0200	0.0217	0.0265	0.0319
		C12T28SOI_-LLPHP_-CNHLSX86_P0	C12T28SOI_-LLPHP_-CNHLSX86_P4	C12T28SOI_-LLPHP_-CNHLSX86_P10	C12T28SOI_-LLPHP_-CNHLSX86_P16
CP ↓	min_pulse_width to CP	0.0356	0.0402	0.0495	0.0582
E ↓	hold_rising to CP	0.0026	0.0004	-0.0045	-0.0041
E ↑	hold_rising to CP	0.0243	0.0244	0.0243	0.0270
E ↓	setup_rising to CP	0.0317	0.0334	0.0382	0.0462
E ↑	setup_rising to CP	0.0200	0.0191	0.0271	0.0319
TE ↓	hold_rising to CP	0.0026	0.0032	-0.0023	-0.0045
TE ↑	hold_rising to CP	0.0248	0.0248	0.0248	0.0274
TE ↓	setup_rising to CP	0.0322	0.0344	0.0419	0.0463
TE ↑	setup_rising to CP	0.0200	0.0217	0.0265	0.0345

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LLP_CNHLSX7_P0	4.792e-05	1.000e-20
C12T28SOI_LLP_CNHLSX7_P4	8.582e-06	1.000e-20
C12T28SOI_LLP_CNHLSX7_P10	1.523e-06	1.000e-20
C12T28SOI_LLP_CNHLSX7_P16	6.295e-07	1.000e-20
C12T28SOI_LLP_CNHLSX15_P0	6.929e-05	1.000e-20
C12T28SOI_LLP_CNHLSX15_P4	1.220e-05	1.000e-20
C12T28SOI_LLP_CNHLSX15_P10	2.102e-06	1.000e-20
C12T28SOI_LLP_CNHLSX15_P16	8.452e-07	1.000e-20
C12T28SOI_LLP_CNHLSX22_P0	8.925e-05	1.000e-20
C12T28SOI_LLP_CNHLSX22_P4	1.535e-05	1.000e-20
C12T28SOI_LLP_CNHLSX22_P10	2.560e-06	1.000e-20
C12T28SOI_LLP_CNHLSX22_P16	1.006e-06	1.000e-20
C12T28SOI_LLP_CNHLSX29_P0	9.965e-05	1.000e-20
C12T28SOI_LLP_CNHLSX29_P4	1.719e-05	1.000e-20
C12T28SOI_LLP_CNHLSX29_P10	2.884e-06	1.000e-20
C12T28SOI_LLP_CNHLSX29_P16	1.141e-06	1.000e-20

C12T28SOI_LLP_CNHLSX36_P0	1.145e-04	1.000e-20
C12T28SOI_LLP_CNHLSX36_P4	1.970e-05	1.000e-20
C12T28SOI_LLP_CNHLSX36_P10	3.297e-06	1.000e-20
C12T28SOI_LLP_CNHLSX36_P16	1.303e-06	1.000e-20
C12T28SOI_LLP_CNHLSX51_P0	1.429e-04	1.000e-20
C12T28SOI_LLP_CNHLSX51_P4	2.476e-05	1.000e-20
C12T28SOI_LLP_CNHLSX51_P10	4.153e-06	1.000e-20
C12T28SOI_LLP_CNHLSX51_P16	1.638e-06	1.000e-20
C12T28SOI_LLP_CNHLSX58_P0	1.756e-04	1.000e-20
C12T28SOI_LLP_CNHLSX58_P4	3.037e-05	1.000e-20
C12T28SOI_LLP_CNHLSX58_P10	5.093e-06	1.000e-20
C12T28SOI_LLP_CNHLSX58_P16	2.005e-06	1.000e-20
C12T28SOI_LLP_CNHLSX71_P0	2.074e-04	1.000e-20
C12T28SOI_LLP_CNHLSX71_P4	3.587e-05	1.000e-20
C12T28SOI_LLP_CNHLSX71_P10	6.002e-06	1.000e-20
C12T28SOI_LLP_CNHLSX71_P16	2.358e-06	1.000e-20
C12T28SOI_LLP_CNHLSX93_P0	2.549e-04	1.000e-20
C12T28SOI_LLP_CNHLSX93_P4	4.407e-05	1.000e-20
C12T28SOI_LLP_CNHLSX93_P10	7.352e-06	1.000e-20
C12T28SOI_LLP_CNHLSX93_P16	2.878e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P0	1.107e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P4	1.928e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P10	3.280e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX29_P16	1.307e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P0	1.253e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P4	2.176e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P10	3.691e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX36_P16	1.468e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P0	1.434e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P4	2.501e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P10	4.244e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX44_P16	1.686e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P0	1.568e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P4	2.724e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P10	4.588e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX51_P16	1.810e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P0	1.865e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P4	3.243e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P10	5.480e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX58_P16	2.165e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P0	2.211e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P4	3.822e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P10	6.417e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX71_P16	2.527e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P0	2.532e-04	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P4	4.397e-05	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P10	7.396e-06	1.000e-20
C12T28SOI_LLPHP_CNHLSX86_P16	2.913e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LLP_-CNHLSX7_P0	C12T28SOI_LLP_-CNHLSX7_P4	C12T28SOI_LLP_-CNHLSX7_P10	C12T28SOI_LLP_-CNHLSX7_P16

CP (output stable)	2.487e-03	2.468e-03	2.527e-03	2.614e-03
E (output stable)	1.328e-03	1.251e-03	1.211e-03	1.217e-03
TE (output stable)	1.420e-03	1.378e-03	1.388e-03	1.431e-03
CP to Q	3.591e-03	3.419e-03	3.384e-03	3.441e-03
	C12T28SOI_LLP_-CNHLSX15_P0	C12T28SOI_LLP_-CNHLSX15_P4	C12T28SOI_LLP_-CNHLSX15_P10	C12T28SOI_LLP_-CNHLSX15_P16
CP (output stable)	2.878e-03	2.872e-03	2.960e-03	3.070e-03
E (output stable)	1.361e-03	1.289e-03	1.255e-03	1.268e-03
TE (output stable)	1.453e-03	1.416e-03	1.431e-03	1.481e-03
CP to Q	5.347e-03	5.034e-03	5.007e-03	5.064e-03
	C12T28SOI_LLP_-CNHLSX22_P0	C12T28SOI_LLP_-CNHLSX22_P4	C12T28SOI_LLP_-CNHLSX22_P10	C12T28SOI_LLP_-CNHLSX22_P16
CP (output stable)	3.212e-03	3.216e-03	3.318e-03	3.444e-03
E (output stable)	1.456e-03	1.385e-03	1.352e-03	1.367e-03
TE (output stable)	1.547e-03	1.511e-03	1.528e-03	1.580e-03
CP to Q	6.939e-03	6.542e-03	6.438e-03	6.586e-03
	C12T28SOI_LLP_-CNHLSX29_P0	C12T28SOI_LLP_-CNHLSX29_P4	C12T28SOI_LLP_-CNHLSX29_P10	C12T28SOI_LLP_-CNHLSX29_P16
CP (output stable)	3.343e-03	3.366e-03	3.483e-03	3.643e-03
E (output stable)	1.482e-03	1.410e-03	1.376e-03	1.390e-03
TE (output stable)	1.574e-03	1.536e-03	1.552e-03	1.603e-03
CP to Q	8.500e-03	8.018e-03	7.801e-03	8.007e-03
	C12T28SOI_LLP_-CNHLSX36_P0	C12T28SOI_LLP_-CNHLSX36_P4	C12T28SOI_LLP_-CNHLSX36_P10	C12T28SOI_LLP_-CNHLSX36_P16
CP (output stable)	3.574e-03	3.592e-03	3.741e-03	3.903e-03
E (output stable)	1.486e-03	1.414e-03	1.382e-03	1.397e-03
TE (output stable)	1.578e-03	1.540e-03	1.557e-03	1.611e-03
CP to Q	9.912e-03	9.304e-03	9.202e-03	9.423e-03
	C12T28SOI_LLP_-CNHLSX51_P0	C12T28SOI_LLP_-CNHLSX51_P4	C12T28SOI_LLP_-CNHLSX51_P10	C12T28SOI_LLP_-CNHLSX51_P16
CP (output stable)	3.935e-03	3.989e-03	4.167e-03	4.331e-03
E (output stable)	1.494e-03	1.429e-03	1.403e-03	1.423e-03
TE (output stable)	1.586e-03	1.555e-03	1.579e-03	1.637e-03
CP to Q	1.346e-02	1.270e-02	1.251e-02	1.272e-02
	C12T28SOI_LLP_-CNHLSX58_P0	C12T28SOI_LLP_-CNHLSX58_P4	C12T28SOI_LLP_-CNHLSX58_P10	C12T28SOI_LLP_-CNHLSX58_P16
CP (output stable)	5.075e-03	5.188e-03	5.411e-03	5.637e-03
E (output stable)	1.639e-03	1.577e-03	1.556e-03	1.582e-03
TE (output stable)	1.730e-03	1.702e-03	1.730e-03	1.793e-03
CP to Q	1.541e-02	1.449e-02	1.417e-02	1.438e-02
	C12T28SOI_LLP_-CNHLSX71_P0	C12T28SOI_LLP_-CNHLSX71_P4	C12T28SOI_LLP_-CNHLSX71_P10	C12T28SOI_LLP_-CNHLSX71_P16
CP (output stable)	5.695e-03	5.854e-03	6.154e-03	6.382e-03
E (output stable)	1.693e-03	1.633e-03	1.617e-03	1.649e-03
TE (output stable)	1.784e-03	1.758e-03	1.791e-03	1.860e-03
CP to Q	1.888e-02	1.783e-02	1.763e-02	1.776e-02
	C12T28SOI_LLP_-CNHLSX93_P0	C12T28SOI_LLP_-CNHLSX93_P4	C12T28SOI_LLP_-CNHLSX93_P10	C12T28SOI_LLP_-CNHLSX93_P16
CP (output stable)	6.482e-03	6.654e-03	7.063e-03	7.343e-03
E (output stable)	1.814e-03	1.757e-03	1.748e-03	1.789e-03
TE (output stable)	1.905e-03	1.884e-03	1.925e-03	2.002e-03
CP to Q	2.497e-02	2.313e-02	2.280e-02	2.313e-02

	C12T28SOI_LLPHP_-CNHLSX29_P0	C12T28SOI_LLPHP_-CNHLSX29_P4	C12T28SOI_LLPHP_-CNHLSX29_P10	C12T28SOI_LLPHP_-CNHLSX29_P16
CP (output stable)	4.656e-03	4.743e-03	4.925e-03	5.123e-03
E (output stable)	1.408e-03	1.327e-03	1.282e-03	1.289e-03
TE (output stable)	1.498e-03	1.451e-03	1.459e-03	1.506e-03
CP to Q	1.031e-02	9.857e-03	9.780e-03	1.002e-02
	C12T28SOI_LLPHP_-CNHLSX36_P0	C12T28SOI_LLPHP_-CNHLSX36_P4	C12T28SOI_LLPHP_-CNHLSX36_P10	C12T28SOI_LLPHP_-CNHLSX36_P16
CP (output stable)	4.860e-03	4.954e-03	5.157e-03	5.376e-03
E (output stable)	1.416e-03	1.336e-03	1.293e-03	1.302e-03
TE (output stable)	1.506e-03	1.460e-03	1.470e-03	1.517e-03
CP to Q	1.169e-02	1.118e-02	1.111e-02	1.138e-02
	C12T28SOI_LLPHP_-CNHLSX44_P0	C12T28SOI_LLPHP_-CNHLSX44_P4	C12T28SOI_LLPHP_-CNHLSX44_P10	C12T28SOI_LLPHP_-CNHLSX44_P16
CP (output stable)	5.231e-03	5.348e-03	5.585e-03	5.774e-03
E (output stable)	1.462e-03	1.385e-03	1.347e-03	1.359e-03
TE (output stable)	1.552e-03	1.509e-03	1.523e-03	1.575e-03
CP to Q	1.355e-02	1.279e-02	1.272e-02	1.287e-02
	C12T28SOI_LLPHP_-CNHLSX51_P0	C12T28SOI_LLPHP_-CNHLSX51_P4	C12T28SOI_LLPHP_-CNHLSX51_P10	C12T28SOI_LLPHP_-CNHLSX51_P16
CP (output stable)	5.260e-03	5.337e-03	5.578e-03	5.798e-03
E (output stable)	1.462e-03	1.385e-03	1.347e-03	1.359e-03
TE (output stable)	1.553e-03	1.510e-03	1.523e-03	1.575e-03
CP to Q	1.510e-02	1.428e-02	1.394e-02	1.429e-02
	C12T28SOI_LLPHP_-CNHLSX58_P0	C12T28SOI_LLPHP_-CNHLSX58_P4	C12T28SOI_LLPHP_-CNHLSX58_P10	C12T28SOI_LLPHP_-CNHLSX58_P16
CP (output stable)	6.092e-03	6.250e-03	6.579e-03	6.843e-03
E (output stable)	1.533e-03	1.458e-03	1.425e-03	1.444e-03
TE (output stable)	1.623e-03	1.583e-03	1.602e-03	1.659e-03
CP to Q	1.649e-02	1.553e-02	1.524e-02	1.571e-02
	C12T28SOI_LLPHP_-CNHLSX71_P0	C12T28SOI_LLPHP_-CNHLSX71_P4	C12T28SOI_LLPHP_-CNHLSX71_P10	C12T28SOI_LLPHP_-CNHLSX71_P16
CP (output stable)	6.800e-03	6.997e-03	7.359e-03	7.691e-03
E (output stable)	1.646e-03	1.573e-03	1.543e-03	1.565e-03
TE (output stable)	1.736e-03	1.698e-03	1.720e-03	1.780e-03
CP to Q	1.974e-02	1.889e-02	1.841e-02	1.889e-02
	C12T28SOI_LLPHP_-CNHLSX86_P0	C12T28SOI_LLPHP_-CNHLSX86_P4	C12T28SOI_LLPHP_-CNHLSX86_P10	C12T28SOI_LLPHP_-CNHLSX86_P16
CP (output stable)	7.394e-03	7.612e-03	8.026e-03	8.407e-03
E (output stable)	1.678e-03	1.612e-03	1.594e-03	1.624e-03
TE (output stable)	1.768e-03	1.736e-03	1.770e-03	1.839e-03
CP to Q	2.291e-02	2.173e-02	2.136e-02	2.182e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C12T28SOI_LLP_-CNHLSX7_P0	C12T28SOI_LLP_-CNHLSX7_P4	C12T28SOI_LLP_-CNHLSX7_P10	C12T28SOI_LLP_-CNHLSX7_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX15_P0	C12T28SOI_LLP_-CNHLSX15_P4	C12T28SOI_LLP_-CNHLSX15_P10	C12T28SOI_LLP_-CNHLSX15_P16

CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX22_P0	C12T28SOI_LLP_-CNHLSX22_P4	C12T28SOI_LLP_-CNHLSX22_P10	C12T28SOI_LLP_-CNHLSX22_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX29_P0	C12T28SOI_LLP_-CNHLSX29_P4	C12T28SOI_LLP_-CNHLSX29_P10	C12T28SOI_LLP_-CNHLSX29_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX36_P0	C12T28SOI_LLP_-CNHLSX36_P4	C12T28SOI_LLP_-CNHLSX36_P10	C12T28SOI_LLP_-CNHLSX36_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX51_P0	C12T28SOI_LLP_-CNHLSX51_P4	C12T28SOI_LLP_-CNHLSX51_P10	C12T28SOI_LLP_-CNHLSX51_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX58_P0	C12T28SOI_LLP_-CNHLSX58_P4	C12T28SOI_LLP_-CNHLSX58_P10	C12T28SOI_LLP_-CNHLSX58_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX71_P0	C12T28SOI_LLP_-CNHLSX71_P4	C12T28SOI_LLP_-CNHLSX71_P10	C12T28SOI_LLP_-CNHLSX71_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLP_-CNHLSX93_P0	C12T28SOI_LLP_-CNHLSX93_P4	C12T28SOI_LLP_-CNHLSX93_P10	C12T28SOI_LLP_-CNHLSX93_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX29_P0	C12T28SOI_LLPHP_-CNHLSX29_P4	C12T28SOI_LLPHP_-CNHLSX29_P10	C12T28SOI_LLPHP_-CNHLSX29_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

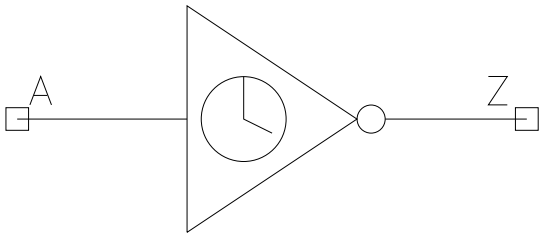
	C12T28SOI_LLPHP_-CNHLSX36_P0	C12T28SOI_LLPHP_-CNHLSX36_P4	C12T28SOI_LLPHP_-CNHLSX36_P10	C12T28SOI_LLPHP_-CNHLSX36_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX44_P0	C12T28SOI_LLPHP_-CNHLSX44_P4	C12T28SOI_LLPHP_-CNHLSX44_P10	C12T28SOI_LLPHP_-CNHLSX44_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX51_P0	C12T28SOI_LLPHP_-CNHLSX51_P4	C12T28SOI_LLPHP_-CNHLSX51_P10	C12T28SOI_LLPHP_-CNHLSX51_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX58_P0	C12T28SOI_LLPHP_-CNHLSX58_P4	C12T28SOI_LLPHP_-CNHLSX58_P10	C12T28SOI_LLPHP_-CNHLSX58_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX71_P0	C12T28SOI_LLPHP_-CNHLSX71_P4	C12T28SOI_LLPHP_-CNHLSX71_P10	C12T28SOI_LLPHP_-CNHLSX71_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LLPHP_-CNHLSX86_P0	C12T28SOI_LLPHP_-CNHLSX86_P4	C12T28SOI_LLPHP_-CNHLSX86_P10	C12T28SOI_LLPHP_-CNHLSX86_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNIV

Cell Description

Inverter with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P0	1.200	0.272	0.3264
X5_P4	1.200	0.272	0.3264
X5_P10	1.200	0.272	0.3264
X5_P16	1.200	0.272	0.3264
X8_P0	1.200	0.272	0.3264
X8_P4	1.200	0.272	0.3264
X8_P10	1.200	0.272	0.3264
X8_P16	1.200	0.272	0.3264
X16_P0	1.200	0.408	0.4896
X16_P4	1.200	0.408	0.4896
X16_P10	1.200	0.408	0.4896
X16_P16	1.200	0.408	0.4896
X23_P0	1.200	0.544	0.6528
X23_P4	1.200	0.544	0.6528
X23_P10	1.200	0.544	0.6528
X23_P16	1.200	0.544	0.6528
X31_P0	1.200	0.680	0.8160
X31_P4	1.200	0.680	0.8160
X31_P10	1.200	0.680	0.8160
X31_P16	1.200	0.680	0.8160
X39_P0	1.200	0.816	0.9792
X39_P4	1.200	0.816	0.9792
X39_P10	1.200	0.816	0.9792
X39_P16	1.200	0.816	0.9792
X47_P0	1.200	0.952	1.1424
X47_P4	1.200	0.952	1.1424
X47_P10	1.200	0.952	1.1424
X47_P16	1.200	0.952	1.1424
X55_P0	1.200	1.088	1.3056
X55_P4	1.200	1.088	1.3056
X55_P10	1.200	1.088	1.3056
X55_P16	1.200	1.088	1.3056
X61_P0	1.200	1.224	1.4688

X61_P4	1.200	1.224	1.4688
X61_P10	1.200	1.224	1.4688
X61_P16	1.200	1.224	1.4688
X70_P0	1.200	1.360	1.6320
X70_P4	1.200	1.360	1.6320
X70_P10	1.200	1.360	1.6320
X70_P16	1.200	1.360	1.6320
X94_P0	1.200	1.768	2.1216
X94_P4	1.200	1.768	2.1216
X94_P10	1.200	1.768	2.1216
X94_P16	1.200	1.768	2.1216
X133_P0	1.200	2.448	2.9376
X133_P4	1.200	2.448	2.9376
X133_P10	1.200	2.448	2.9376
X133_P16	1.200	2.448	2.9376

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	X5_P0	X5_P4	X5_P10	X5_P16
A	0.0006	0.0006	0.0006	0.0007
	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0008	0.0009	0.0009	0.0010
	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0015	0.0016	0.0017	0.0018
	X23_P0	X23_P4	X23_P10	X23_P16
A	0.0023	0.0024	0.0026	0.0027
	X31_P0	X31_P4	X31_P10	X31_P16
A	0.0031	0.0032	0.0034	0.0036
	X39_P0	X39_P4	X39_P10	X39_P16
A	0.0038	0.0039	0.0042	0.0044
	X47_P0	X47_P4	X47_P10	X47_P16
A	0.0047	0.0048	0.0051	0.0054
	X55_P0	X55_P4	X55_P10	X55_P16
A	0.0054	0.0056	0.0059	0.0062
	X61_P0	X61_P4	X61_P10	X61_P16
A	0.0060	0.0062	0.0066	0.0070
	X70_P0	X70_P4	X70_P10	X70_P16
A	0.0072	0.0074	0.0077	0.0082
	X94_P0	X94_P4	X94_P10	X94_P16
A	0.0098	0.0102	0.0108	0.0113
	X133_P0	X133_P4	X133_P10	X133_P16
A	0.0145	0.0150	0.0159	0.0165

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P0	X5_P4	X5_P0	X5_P4
A to Z ↓	0.0051	0.0061	2.8038	2.9754

A to Z ↑	0.0094	0.0106	4.0925	4.4573
	X5_P10	**X5_P16**	**X5_P10**	**X5_P16**
A to Z ↓	0.0074	0.0083	3.2074	3.4098
A to Z ↑	0.0121	0.0134	4.9757	5.4587
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0050	0.0058	1.7893	1.8991
A to Z ↑	0.0072	0.0082	2.2050	2.3907
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0068	0.0077	2.0485	2.1811
A to Z ↑	0.0096	0.0107	2.6552	2.8991
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0041	0.0048	0.8840	0.9386
A to Z ↑	0.0062	0.0071	1.1033	1.1957
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0058	0.0065	1.0123	1.0765
A to Z ↑	0.0083	0.0094	1.3273	1.4494
	X23_P0	**X23_P4**	**X23_P0**	**X23_P4**
A to Z ↓	0.0045	0.0053	0.6299	0.6691
A to Z ↑	0.0063	0.0072	0.7503	0.8126
	X23_P10	**X23_P16**	**X23_P10**	**X23_P16**
A to Z ↓	0.0062	0.0071	0.7219	0.7682
A to Z ↑	0.0085	0.0096	0.9019	0.9839
	X31_P0	**X31_P4**	**X31_P0**	**X31_P4**
A to Z ↓	0.0043	0.0049	0.4565	0.4849
A to Z ↑	0.0061	0.0069	0.5618	0.6085
	X31_P10	**X31_P16**	**X31_P10**	**X31_P16**
A to Z ↓	0.0058	0.0067	0.5231	0.5572
A to Z ↑	0.0080	0.0092	0.6753	0.7370
	X39_P0	**X39_P4**	**X39_P0**	**X39_P4**
A to Z ↓	0.0046	0.0053	0.3695	0.3923
A to Z ↑	0.0063	0.0072	0.4527	0.4904
	X39_P10	**X39_P16**	**X39_P10**	**X39_P16**
A to Z ↓	0.0063	0.0072	0.4233	0.4510
A to Z ↑	0.0085	0.0096	0.5437	0.5933
	X47_P0	**X47_P4**	**X47_P0**	**X47_P4**
A to Z ↓	0.0045	0.0053	0.3071	0.3259
A to Z ↑	0.0062	0.0072	0.3769	0.4080
	X47_P10	**X47_P16**	**X47_P10**	**X47_P16**
A to Z ↓	0.0062	0.0071	0.3520	0.3751
A to Z ↑	0.0083	0.0095	0.4524	0.4935
	X55_P0	**X55_P4**	**X55_P0**	**X55_P4**
A to Z ↓	0.0049	0.0057	0.2651	0.2813
A to Z ↑	0.0065	0.0075	0.3242	0.3508
	X55_P10	**X55_P16**	**X55_P10**	**X55_P16**
A to Z ↓	0.0067	0.0075	0.3040	0.3239
A to Z ↑	0.0087	0.0098	0.3889	0.4245
	X61_P0	**X61_P4**	**X61_P0**	**X61_P4**
A to Z ↓	0.0051	0.0058	0.2380	0.2526
A to Z ↑	0.0067	0.0076	0.2935	0.3179
	X61_P10	**X61_P16**	**X61_P10**	**X61_P16**
A to Z ↓	0.0068	0.0077	0.2731	0.2907
A to Z ↑	0.0088	0.0100	0.3524	0.3849

	X70_P0	X70_P4	X70_P0	X70_P4
A to Z ↓	0.0055	0.0062	0.2092	0.2224
A to Z ↑	0.0070	0.0079	0.2553	0.2762
	X70_P10	**X70_P16**	**X70_P10**	**X70_P16**
A to Z ↓	0.0072	0.0081	0.2400	0.2557
A to Z ↑	0.0091	0.0103	0.3060	0.3331
	X94_P0	**X94_P4**	**X94_P0**	**X94_P4**
A to Z ↓	0.0068	0.0074	0.1613	0.1712
A to Z ↑	0.0082	0.0090	0.1952	0.2110
	X94_P10	**X94_P16**	**X94_P10**	**X94_P16**
A to Z ↓	0.0085	0.0094	0.1849	0.1966
A to Z ↑	0.0102	0.0114	0.2337	0.2545
	X133_P0	**X133_P4**	**X133_P0**	**X133_P4**
A to Z ↓	0.0085	0.0090	0.1197	0.1272
A to Z ↑	0.0097	0.0105	0.1423	0.1539
	X133_P10	**X133_P16**	**X133_P10**	**X133_P16**
A to Z ↓	0.0103	0.0113	0.1373	0.1461
A to Z ↑	0.0119	0.0131	0.1704	0.1854

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X5_P0	4.460e-06	1.000e-20
X5_P4	8.517e-07	1.000e-20
X5_P10	1.641e-07	1.000e-20
X5_P16	6.971e-08	1.000e-20
X8_P0	1.193e-05	1.000e-20
X8_P4	2.096e-06	1.000e-20
X8_P10	3.530e-07	1.000e-20
X8_P16	1.332e-07	1.000e-20
X16_P0	2.394e-05	1.000e-20
X16_P4	4.207e-06	1.000e-20
X16_P10	7.060e-07	1.000e-20
X16_P16	2.661e-07	1.000e-20
X23_P0	3.399e-05	1.000e-20
X23_P4	5.955e-06	1.000e-20
X23_P10	9.938e-07	1.000e-20
X23_P16	3.744e-07	1.000e-20
X31_P0	4.651e-05	1.000e-20
X31_P4	8.077e-06	1.000e-20
X31_P10	1.336e-06	1.000e-20
X31_P16	5.024e-07	1.000e-20
X39_P0	5.698e-05	1.000e-20
X39_P4	9.911e-06	1.000e-20
X39_P10	1.641e-06	1.000e-20
X39_P16	6.180e-07	1.000e-20
X47_P0	6.583e-05	1.000e-20
X47_P4	1.155e-05	1.000e-20
X47_P10	1.928e-06	1.000e-20
X47_P16	7.306e-07	1.000e-20
X55_P0	7.909e-05	1.000e-20
X55_P4	1.372e-05	1.000e-20
X55_P10	2.263e-06	1.000e-20

X55_P16	8.520e-07	1.000e-20
X61_P0	8.784e-05	1.000e-20
X61_P4	1.511e-05	1.000e-20
X61_P10	2.479e-06	1.000e-20
X61_P16	9.340e-07	1.000e-20
X70_P0	9.769e-05	1.000e-20
X70_P4	1.711e-05	1.000e-20
X70_P10	2.849e-06	1.000e-20
X70_P16	1.079e-06	1.000e-20
X94_P0	1.296e-04	1.000e-20
X94_P4	2.267e-05	1.000e-20
X94_P10	3.769e-06	1.000e-20
X94_P16	1.428e-06	1.000e-20
X133_P0	1.949e-04	1.000e-20
X133_P4	3.344e-05	1.000e-20
X133_P10	5.444e-06	1.000e-20
X133_P16	2.037e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	7.150e-04	6.004e-04	5.244e-04	4.935e-04
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	1.152e-03	9.229e-04	7.693e-04	6.988e-04
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	2.175e-03	1.680e-03	1.326e-03	1.168e-03
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	3.228e-03	2.535e-03	2.036e-03	1.817e-03
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	4.230e-03	3.244e-03	2.526e-03	2.243e-03
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	5.332e-03	4.142e-03	3.298e-03	2.941e-03
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	6.318e-03	4.929e-03	3.882e-03	3.451e-03
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	7.503e-03	5.845e-03	4.651e-03	4.132e-03
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	8.279e-03	6.391e-03	5.050e-03	4.467e-03
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	9.713e-03	7.535e-03	5.976e-03	5.305e-03
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	1.358e-02	1.039e-02	8.168e-03	7.182e-03
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	2.142e-02	1.637e-02	1.301e-02	1.140e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X5_P0	X5_P4	X5_P10	X5_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X8_P0	X8_P4	X8_P10	X8_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

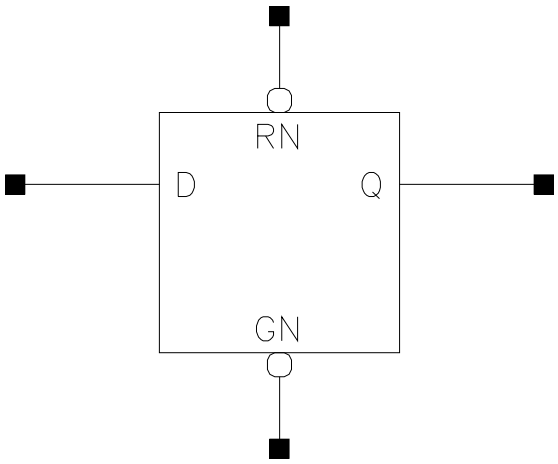
	X23_P0	X23_P4	X23_P10	X23_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P0	X31_P4	X31_P10	X31_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X39_P0	X39_P4	X39_P10	X39_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X47_P0	X47_P4	X47_P10	X47_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X55_P0	X55_P4	X55_P10	X55_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X61_P0	X61_P4	X61_P10	X61_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X70_P0	X70_P4	X70_P10	X70_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X94_P0	X94_P4	X94_P10	X94_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X133_P0	X133_P4	X133_P10	X133_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNLDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X33_P0	X33_P4	X33_P10	X33_P16
D	0.0012	0.0012	0.0013	0.0014
GN	0.0022	0.0023	0.0024	0.0025
RN	0.0006	0.0006	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X33_P0	X33_P4	X33_P0	X33_P4

D to Q ↓	0.0377	0.0425	0.4190	0.4486
D to Q ↑	0.0394	0.0439	0.5726	0.6246
GN to Q ↓	0.0349	0.0394	0.4197	0.4488
GN to Q ↑	0.0421	0.0471	0.5729	0.6243
RN to Q ↓	0.0514	0.0579	0.4333	0.4658
RN to Q ↑	0.0439	0.0488	0.5731	0.6238
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D to Q ↓	0.0498	0.0571	0.4906	0.5290
D to Q ↑	0.0509	0.0578	0.6996	0.7701
GN to Q ↓	0.0459	0.0521	0.4911	0.5292
GN to Q ↑	0.0548	0.0621	0.6995	0.7702
RN to Q ↓	0.0677	0.0771	0.5126	0.5550
RN to Q ↑	0.0562	0.0634	0.6995	0.7697

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X33_P0	X33_P4	X33_P10	X33_P16
D ↓	hold_rising to GN	-0.0030	-0.0042	-0.0117	-0.0162
D ↑	hold_rising to GN	-0.0039	-0.0093	-0.0169	-0.0218
D ↓	setup_rising to GN	0.0397	0.0446	0.0549	0.0614
D ↑	setup_rising to GN	0.0443	0.0492	0.0562	0.0632
GN ↓	min_pulse_width to GN	0.0471	0.0514	0.0604	0.0682
RN ↓	min_pulse_width to RN	0.0615	0.0686	0.0806	0.0903
RN ↑	recovery_rising to GN	0.0481	0.0535	0.0632	0.0707
RN ↑	removal_rising to GN	-0.0316	-0.0332	-0.0381	-0.0456

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X33_P0	7.955e-05	1.000e-20
X33_P4	1.387e-05	1.000e-20
X33_P10	2.368e-06	1.000e-20
X33_P16	9.632e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	1.535e-04	8.645e-05	8.284e-05	1.030e-04
GN (output stable)	2.079e-03	1.914e-03	1.827e-03	1.819e-03
RN (output stable)	7.187e-05	5.182e-05	4.701e-05	4.292e-05
D to Q	1.433e-02	1.325e-02	1.272e-02	1.274e-02
GN to Q	1.774e-02	1.658e-02	1.604e-02	1.612e-02
RN to Q	1.122e-02	1.038e-02	9.899e-03	9.821e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X33_P0	X33_P4	X33_P10	X33_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

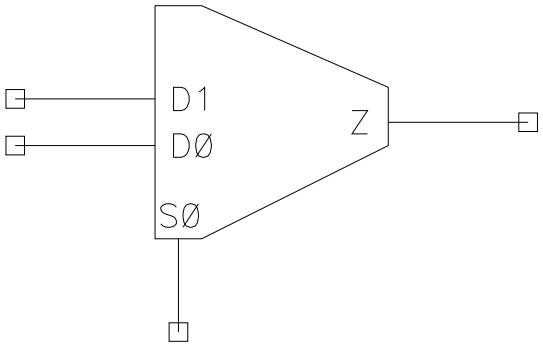
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX21

Cell Description

2:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	1.360	1.6320
X17_P4	1.200	1.360	1.6320
X17_P10	1.200	1.360	1.6320
X17_P16	1.200	1.360	1.6320
X33_P0	1.200	2.448	2.9376
X33_P4	1.200	2.448	2.9376
X33_P10	1.200	2.448	2.9376
X33_P16	1.200	2.448	2.9376

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0010	0.0011	0.0012	0.0012
D1	0.0010	0.0011	0.0012	0.0012
S0	0.0014	0.0015	0.0016	0.0017
	X33_P0	X33_P4	X33_P10	X33_P16
D0	0.0019	0.0020	0.0022	0.0023
D1	0.0019	0.0020	0.0021	0.0023
S0	0.0024	0.0025	0.0026	0.0028

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	X17_P4	X17_P0	X17_P4

D0 to Z ↓	0.0253	0.0284	0.7838	0.8352
D0 to Z ↑	0.0212	0.0237	1.0876	1.1803
D1 to Z ↓	0.0250	0.0280	0.7831	0.8338
D1 to Z ↑	0.0201	0.0225	1.0857	1.1801
S0 to Z ↓	0.0240	0.0270	0.7805	0.8310
S0 to Z ↑	0.0236	0.0265	1.0876	1.1782
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0330	0.0373	0.9079	0.9740
D0 to Z ↑	0.0274	0.0309	1.3150	1.4412
D1 to Z ↓	0.0327	0.0371	0.9063	0.9725
D1 to Z ↑	0.0260	0.0292	1.3130	1.4377
S0 to Z ↓	0.0313	0.0354	0.9041	0.9709
S0 to Z ↑	0.0307	0.0346	1.3138	1.4386
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
D0 to Z ↓	0.0244	0.0275	0.4043	0.4312
D0 to Z ↑	0.0210	0.0235	0.5487	0.5951
D1 to Z ↓	0.0253	0.0286	0.4053	0.4319
D1 to Z ↑	0.0204	0.0228	0.5488	0.5950
S0 to Z ↓	0.0253	0.0284	0.4039	0.4305
S0 to Z ↑	0.0239	0.0269	0.5479	0.5945
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
D0 to Z ↓	0.0322	0.0362	0.4699	0.5036
D0 to Z ↑	0.0274	0.0307	0.6626	0.7252
D1 to Z ↓	0.0334	0.0379	0.4706	0.5046
D1 to Z ↑	0.0264	0.0296	0.6629	0.7253
S0 to Z ↓	0.0330	0.0372	0.4690	0.5030
S0 to Z ↑	0.0313	0.0352	0.6627	0.7254

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P0	5.995e-05	1.000e-20
X17_P4	1.070e-05	1.000e-20
X17_P10	1.850e-06	1.000e-20
X17_P16	7.204e-07	1.000e-20
X33_P0	1.188e-04	1.000e-20
X33_P4	2.115e-05	1.000e-20
X33_P10	3.633e-06	1.000e-20
X33_P16	1.411e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	1.677e-03	1.471e-03	1.338e-03	1.281e-03
D1 (output stable)	1.632e-03	1.409e-03	1.262e-03	1.201e-03
S0 (output stable)	1.442e-03	1.386e-03	1.380e-03	1.406e-03
D0 to Z	5.896e-03	5.544e-03	5.458e-03	5.552e-03
D1 to Z	5.768e-03	5.398e-03	5.314e-03	5.403e-03
S0 to Z	6.249e-03	5.907e-03	5.842e-03	5.945e-03
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	2.790e-03	2.339e-03	2.039e-03	1.909e-03
D1 (output stable)	2.865e-03	2.423e-03	2.129e-03	2.002e-03
S0 (output stable)	2.356e-03	2.245e-03	2.218e-03	2.264e-03

D0 to Z	1.150e-02	1.088e-02	1.081e-02	1.089e-02
D1 to Z	1.142e-02	1.079e-02	1.064e-02	1.079e-02
S0 to Z	1.241e-02	1.181e-02	1.174e-02	1.187e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

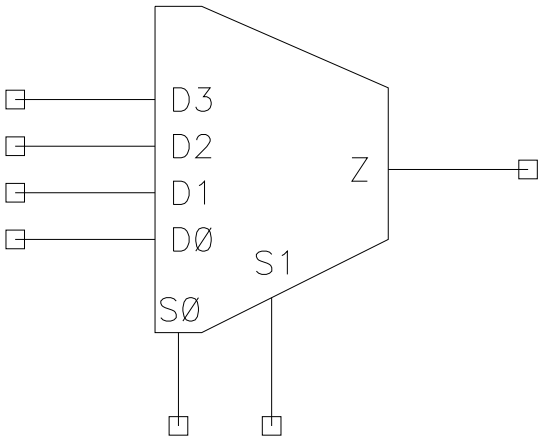
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX41

Cell Description

4:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	2.400	2.176	5.2224
X17_P4	2.400	2.176	5.2224
X17_P10	2.400	2.176	5.2224
X17_P16	2.400	2.176	5.2224
X27_P0	2.400	2.312	5.5488
X27_P4	2.400	2.312	5.5488
X27_P10	2.400	2.312	5.5488
X27_P16	2.400	2.312	5.5488

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
D0	0.0016	0.0017	0.0017	0.0018
D1	0.0015	0.0016	0.0017	0.0017
D2	0.0016	0.0016	0.0017	0.0018
D3	0.0016	0.0016	0.0017	0.0018
S0	0.0039	0.0041	0.0044	0.0047
S1	0.0022	0.0023	0.0025	0.0026

	X27_P0	X27_P4	X27_P10	X27_P16
D0	0.0014	0.0015	0.0016	0.0016
D1	0.0014	0.0014	0.0015	0.0016
D2	0.0014	0.0014	0.0015	0.0016
D3	0.0014	0.0014	0.0015	0.0015
S0	0.0034	0.0036	0.0039	0.0041
S1	0.0020	0.0021	0.0023	0.0024

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
D0 to Z ↓	0.0380	0.0434	0.8181	0.8719
D0 to Z ↑	0.0304	0.0342	1.1080	1.2022
D1 to Z ↓	0.0375	0.0428	0.8178	0.8717
D1 to Z ↑	0.0301	0.0338	1.1073	1.2022
D2 to Z ↓	0.0386	0.0441	0.8175	0.8715
D2 to Z ↑	0.0301	0.0338	1.1066	1.2013
D3 to Z ↓	0.0383	0.0436	0.8174	0.8717
D3 to Z ↑	0.0298	0.0334	1.1063	1.2004
S0 to Z ↓	0.0454	0.0516	0.8159	0.8697
S0 to Z ↑	0.0396	0.0448	1.1082	1.2023
S1 to Z ↓	0.0309	0.0348	0.8171	0.8718
S1 to Z ↑	0.0300	0.0336	1.1074	1.2018
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**
D0 to Z ↓	0.0507	0.0581	0.9482	1.0187
D0 to Z ↑	0.0394	0.0445	1.3392	1.4697
D1 to Z ↓	0.0501	0.0575	0.9476	1.0182
D1 to Z ↑	0.0389	0.0441	1.3390	1.4688
D2 to Z ↓	0.0519	0.0594	0.9479	1.0182
D2 to Z ↑	0.0390	0.0440	1.3380	1.4670
D3 to Z ↓	0.0514	0.0589	0.9481	1.0179
D3 to Z ↑	0.0387	0.0437	1.3382	1.4662
S0 to Z ↓	0.0607	0.0696	0.9457	1.0157
S0 to Z ↑	0.0523	0.0595	1.3398	1.4693
S1 to Z ↓	0.0403	0.0454	0.9481	1.0181
S1 to Z ↑	0.0385	0.0428	1.3393	1.4683
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0428	0.0486	0.5194	0.5551
D0 to Z ↑	0.0380	0.0425	0.7471	0.8118
D1 to Z ↓	0.0387	0.0439	0.5128	0.5477
D1 to Z ↑	0.0369	0.0413	0.7470	0.8111
D2 to Z ↓	0.0446	0.0508	0.5207	0.5565
D2 to Z ↑	0.0375	0.0420	0.7475	0.8114
D3 to Z ↓	0.0441	0.0503	0.5206	0.5566
D3 to Z ↑	0.0370	0.0414	0.7462	0.8108
S0 to Z ↓	0.0504	0.0571	0.5167	0.5522
S0 to Z ↑	0.0456	0.0515	0.7478	0.8119
S1 to Z ↓	0.0333	0.0377	0.5186	0.5542
S1 to Z ↑	0.0411	0.0458	0.7469	0.8110
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.0573	0.0654	0.6065	0.6535
D0 to Z ↑	0.0494	0.0556	0.9053	0.9931

D1 to Z ↓	0.0518	0.0590	0.5973	0.6425
D1 to Z ↑	0.0481	0.0543	0.9051	0.9925
D2 to Z ↓	0.0602	0.0686	0.6086	0.6555
D2 to Z ↑	0.0489	0.0549	0.9054	0.9919
D3 to Z ↓	0.0596	0.0679	0.6084	0.6553
D3 to Z ↑	0.0482	0.0542	0.9049	0.9918
S0 to Z ↓	0.0673	0.0766	0.6032	0.6494
S0 to Z ↑	0.0604	0.0686	0.9063	0.9938
S1 to Z ↓	0.0445	0.0498	0.6058	0.6523
S1 to Z ↑	0.0530	0.0586	0.9049	0.9921

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P0	7.606e-05	1.000e-20
X17_P4	1.420e-05	1.000e-20
X17_P10	2.800e-06	1.000e-20
X17_P16	1.349e-06	1.000e-20
X27_P0	7.913e-05	1.000e-20
X27_P4	1.468e-05	1.000e-20
X27_P10	2.838e-06	1.000e-20
X27_P16	1.328e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	1.847e-04	1.045e-04	1.330e-04	1.835e-04
D1 (output stable)	1.428e-04	1.013e-04	1.201e-04	1.658e-04
D2 (output stable)	1.863e-04	1.140e-04	6.336e-05	7.395e-05
D3 (output stable)	1.867e-04	1.383e-04	1.447e-04	2.064e-04
S0 (output stable)	3.997e-03	4.030e-03	4.344e-03	4.837e-03
S1 (output stable)	3.844e-03	3.464e-03	3.135e-03	2.978e-03
D0 to Z	8.856e-03	8.743e-03	8.832e-03	9.121e-03
D1 to Z	8.837e-03	8.730e-03	8.823e-03	9.130e-03
D2 to Z	9.129e-03	9.037e-03	9.182e-03	9.453e-03
D3 to Z	9.010e-03	8.910e-03	9.061e-03	9.334e-03
S0 to Z	1.333e-02	1.340e-02	1.393e-02	1.467e-02
S1 to Z	1.033e-02	9.425e-03	8.975e-03	8.943e-03
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	1.659e-04	9.290e-05	1.335e-04	1.847e-04
D1 (output stable)	1.396e-04	9.939e-05	1.251e-04	1.688e-04
D2 (output stable)	1.620e-04	1.015e-04	6.136e-05	7.620e-05
D3 (output stable)	1.675e-04	1.230e-04	1.440e-04	2.000e-04
S0 (output stable)	3.736e-03	3.744e-03	4.043e-03	4.481e-03
S1 (output stable)	3.379e-03	3.067e-03	2.801e-03	2.680e-03
D0 to Z	1.141e-02	1.086e-02	1.078e-02	1.088e-02
D1 to Z	1.112e-02	1.064e-02	1.060e-02	1.074e-02
D2 to Z	1.159e-02	1.106e-02	1.099e-02	1.105e-02
D3 to Z	1.145e-02	1.092e-02	1.087e-02	1.093e-02
S0 to Z	1.541e-02	1.503e-02	1.535e-02	1.582e-02
S1 to Z	1.249e-02	1.126e-02	1.068e-02	1.052e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

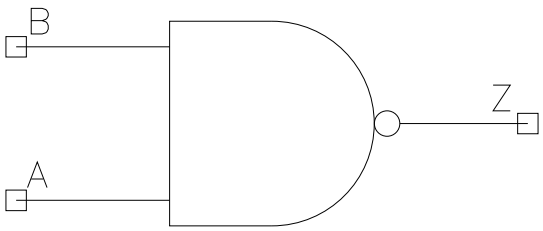
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2

Cell Description

2 input NAND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X33_P0	1.200	1.224	1.4688
X33_P4	1.200	1.224	1.4688
X33_P10	1.200	1.224	1.4688
X33_P16	1.200	1.224	1.4688

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0020	0.0021	0.0022	0.0024
B	0.0019	0.0019	0.0020	0.0021
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0008	0.0008	0.0009	0.0009
B	0.0008	0.0008	0.0009	0.0009

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0061	0.0073	1.0673	1.1376
A to Z ↑	0.0108	0.0122	1.1368	1.2317
B to Z ↓	0.0061	0.0070	1.0843	1.1572
B to Z ↑	0.0084	0.0095	1.1453	1.2418
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0089	0.0101	1.2365	1.3253
A to Z ↑	0.0142	0.0160	1.3670	1.4911
B to Z ↓	0.0081	0.0090	1.2598	1.3515
B to Z ↑	0.0110	0.0122	1.3794	1.5056
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0272	0.0305	0.3978	0.4236
A to Z ↑	0.0311	0.0350	0.5453	0.5911
B to Z ↓	0.0285	0.0320	0.3975	0.4237
B to Z ↑	0.0301	0.0340	0.5461	0.5910
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0364	0.0415	0.4601	0.4927
A to Z ↑	0.0416	0.0472	0.6586	0.7211
B to Z ↓	0.0380	0.0431	0.4604	0.4929
B to Z ↑	0.0403	0.0456	0.6587	0.7219

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X15_P0	2.360e-05	1.000e-20
X15_P4	4.301e-06	1.000e-20
X15_P10	8.073e-07	1.000e-20
X15_P16	3.612e-07	1.000e-20
X33_P0	6.422e-05	1.000e-20
X33_P4	1.156e-05	1.000e-20
X33_P10	2.010e-06	1.000e-20
X33_P16	7.857e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.386e-04	1.201e-04	9.633e-05	8.098e-05
B (output stable)	3.653e-04	4.099e-04	4.268e-04	4.168e-04
A to Z	3.253e-03	2.924e-03	2.775e-03	2.764e-03
B to Z	2.628e-03	2.177e-03	1.880e-03	1.750e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	2.336e-05	2.087e-05	1.771e-05	1.508e-05
B (output stable)	4.445e-05	5.392e-05	5.683e-05	5.515e-05
A to Z	9.478e-03	9.304e-03	9.705e-03	1.009e-02
B to Z	9.373e-03	9.170e-03	9.531e-03	9.894e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

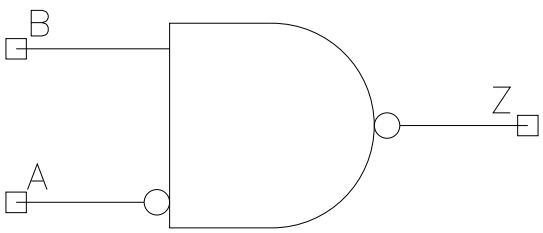
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2A

Cell Description

2 input NAND with A input inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X17_P0	1.200	0.952	1.1424
X17_P4	1.200	0.952	1.1424
X17_P10	1.200	0.952	1.1424
X17_P16	1.200	0.952	1.1424
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X17_P0	X17_P4	X17_P10	X17_P16
A	0.0008	0.0009	0.0009	0.0010
B	0.0009	0.0010	0.0011	0.0011
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0012	0.0013	0.0013	0.0014
B	0.0009	0.0009	0.0010	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X17_P0	**X17_P4**	**X17_P0**	**X17_P4**
A to Z ↓	0.0225	0.0255	0.7731	0.8237
A to Z ↑	0.0199	0.0222	1.0857	1.1779
B to Z ↓	0.0252	0.0283	0.7712	0.8223
B to Z ↑	0.0244	0.0275	1.0826	1.1745
	X17_P10	**X17_P16**	**X17_P10**	**X17_P16**

A to Z ↓	0.0305	0.0345	0.8973	0.9620
A to Z ↑	0.0259	0.0288	1.3113	1.4351
B to Z ↓	0.0338	0.0382	0.8950	0.9604
B to Z ↑	0.0324	0.0363	1.3101	1.4335
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0252	0.0287	0.4640	0.4955
A to Z ↑	0.0226	0.0252	0.7118	0.7739
B to Z ↓	0.0269	0.0303	0.4628	0.4938
B to Z ↑	0.0272	0.0308	0.7095	0.7709
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0337	0.0385	0.5390	0.5796
A to Z ↑	0.0291	0.0327	0.8630	0.9463
B to Z ↓	0.0356	0.0408	0.5377	0.5785
B to Z ↑	0.0360	0.0411	0.8590	0.9423

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X17_P0	3.834e-05	1.000e-20
X17_P4	7.076e-06	1.000e-20
X17_P10	1.269e-06	1.000e-20
X17_P16	5.035e-07	1.000e-20
X27_P0	4.691e-05	1.000e-20
X27_P4	8.762e-06	1.000e-20
X27_P10	1.612e-06	1.000e-20
X27_P16	6.589e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	4.908e-05	4.650e-05	4.399e-05	7.662e-05
B (output stable)	1.600e-03	1.413e-03	1.300e-03	1.272e-03
A to Z	4.709e-03	4.451e-03	4.504e-03	4.552e-03
B to Z	6.134e-03	5.864e-03	5.962e-03	6.048e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.497e-04	1.409e-04	2.362e-04	3.574e-04
B (output stable)	1.775e-03	1.578e-03	1.471e-03	1.491e-03
A to Z	7.747e-03	7.392e-03	7.369e-03	7.576e-03
B to Z	8.789e-03	8.512e-03	8.602e-03	8.887e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

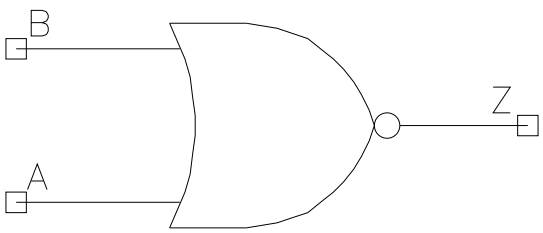
Pin Cycle (vdds)	X17_P0	X17_P4	X17_P10	X17_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2

Cell Description

2 input NOR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	0.952	1.1424
X14_P4	1.200	0.952	1.1424
X14_P10	1.200	0.952	1.1424
X14_P16	1.200	0.952	1.1424
X33_P0	1.200	1.496	1.7952
X33_P4	1.200	1.496	1.7952
X33_P10	1.200	1.496	1.7952
X33_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0022	0.0023	0.0024	0.0026
B	0.0020	0.0021	0.0022	0.0023
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0009	0.0009	0.0010	0.0011
B	0.0009	0.0010	0.0010	0.0010

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0084	0.0096	0.8950	0.9475
A to Z ↑	0.0090	0.0108	1.4741	1.5880
B to Z ↓	0.0061	0.0070	0.9056	0.9600
B to Z ↑	0.0084	0.0095	1.4880	1.6055
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**

A to Z ↓	0.0112	0.0125	1.0220	1.0867
A to Z ↑	0.0132	0.0151	1.7589	1.9247
B to Z ↓	0.0081	0.0091	1.0349	1.1027
B to Z ↑	0.0109	0.0122	1.7817	1.9498
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0309	0.0349	0.3922	0.4178
A to Z ↑	0.0283	0.0324	0.5437	0.5895
B to Z ↓	0.0293	0.0331	0.3919	0.4179
B to Z ↑	0.0290	0.0330	0.5436	0.5894
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0404	0.0464	0.4539	0.4862
A to Z ↑	0.0380	0.0441	0.6564	0.7186
B to Z ↓	0.0384	0.0443	0.4540	0.4864
B to Z ↑	0.0382	0.0443	0.6562	0.7187

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X14_P0	3.234e-05	1.000e-20
X14_P4	5.744e-06	1.000e-20
X14_P10	9.925e-07	1.000e-20
X14_P16	4.027e-07	1.000e-20
X33_P0	8.262e-05	1.000e-20
X33_P4	1.470e-05	1.000e-20
X33_P10	2.518e-06	1.000e-20
X33_P16	9.838e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	2.051e-04	1.987e-04	1.935e-04	2.011e-04
B (output stable)	3.860e-04	2.351e-04	9.655e-05	7.365e-05
A to Z	3.547e-03	3.283e-03	3.193e-03	3.218e-03
B to Z	2.702e-03	2.234e-03	1.914e-03	1.771e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	4.968e-05	4.672e-05	4.656e-05	4.736e-05
B (output stable)	7.800e-05	5.576e-05	1.688e-05	9.194e-06
A to Z	1.060e-02	1.049e-02	1.058e-02	1.115e-02
B to Z	1.040e-02	1.023e-02	1.023e-02	1.078e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

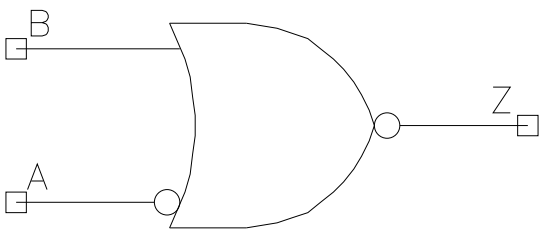
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2A

Cell Description

2 input NOR with A input Inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	1.224	1.4688
X15_P4	1.200	1.224	1.4688
X15_P10	1.200	1.224	1.4688
X15_P16	1.200	1.224	1.4688
X27_P0	1.200	1.496	1.7952
X27_P4	1.200	1.496	1.7952
X27_P10	1.200	1.496	1.7952
X27_P16	1.200	1.496	1.7952

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0013	0.0013	0.0014	0.0015
B	0.0009	0.0009	0.0010	0.0011
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0015	0.0016	0.0017	0.0018
B	0.0009	0.0010	0.0010	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0244	0.0274	0.9604	1.0227
A to Z ↑	0.0168	0.0192	1.0882	1.1813
B to Z ↓	0.0239	0.0269	0.9545	1.0163
B to Z ↑	0.0233	0.0264	1.0860	1.1791
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**

A to Z ↓	0.0318	0.0358	1.1096	1.1876
A to Z ↑	0.0225	0.0254	1.3169	1.4414
B to Z ↓	0.0316	0.0360	1.1038	1.1836
B to Z ↑	0.0309	0.0350	1.3140	1.4387
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0209	0.0236	0.5403	0.5756
A to Z ↑	0.0186	0.0209	0.5824	0.6317
B to Z ↓	0.0243	0.0275	0.5394	0.5746
B to Z ↑	0.0256	0.0290	0.5809	0.6299
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0278	0.0312	0.6249	0.6691
A to Z ↑	0.0244	0.0273	0.7041	0.7713
B to Z ↓	0.0325	0.0368	0.6254	0.6690
B to Z ↑	0.0342	0.0385	0.7032	0.7705

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X15_P0	5.171e-05	1.000e-20
X15_P4	8.777e-06	1.000e-20
X15_P10	1.433e-06	1.000e-20
X15_P16	5.502e-07	1.000e-20
X27_P0	8.448e-05	1.000e-20
X27_P4	1.423e-05	1.000e-20
X27_P10	2.289e-06	1.000e-20
X27_P16	8.664e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	8.396e-05	6.733e-05	5.015e-05	4.046e-05
B (output stable)	1.831e-03	1.685e-03	1.499e-03	1.431e-03
A to Z	4.815e-03	4.648e-03	4.665e-03	4.783e-03
B to Z	6.014e-03	5.849e-03	5.928e-03	6.112e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.169e-04	9.617e-05	7.454e-05	6.046e-05
B (output stable)	2.075e-03	1.943e-03	1.811e-03	1.749e-03
A to Z	7.881e-03	7.527e-03	7.607e-03	7.739e-03
B to Z	9.205e-03	8.971e-03	9.239e-03	9.449e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

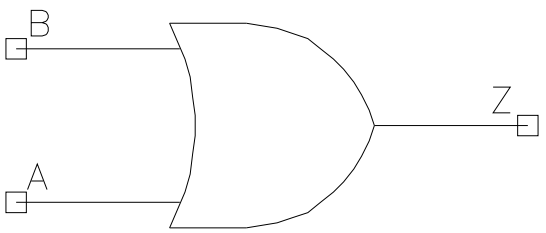
Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR2

Cell Description

2 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	0.952	1.1424
X15_P4	1.200	0.952	1.1424
X15_P10	1.200	0.952	1.1424
X15_P16	1.200	0.952	1.1424
X20_P0	1.200	1.360	1.6320
X20_P4	1.200	1.360	1.6320
X20_P10	1.200	1.360	1.6320
X20_P16	1.200	1.360	1.6320
X33_P0	1.200	1.360	1.6320
X33_P4	1.200	1.360	1.6320
X33_P10	1.200	1.360	1.6320
X33_P16	1.200	1.360	1.6320
X37_P0	1.200	1.632	1.9584
X37_P4	1.200	1.632	1.9584
X37_P10	1.200	1.632	1.9584
X37_P16	1.200	1.632	1.9584

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0016	0.0017	0.0018	0.0019
B	0.0014	0.0015	0.0017	0.0018
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0024	0.0025	0.0028	0.0029
B	0.0025	0.0026	0.0028	0.0030
	X33_P0	X33_P4	X33_P10	X33_P16
A	0.0017	0.0017	0.0019	0.0020

B	0.0017	0.0018	0.0019	0.0020
	X37_P0	X37_P4	X37_P10	X37_P16
A	0.0024	0.0025	0.0027	0.0029
B	0.0025	0.0026	0.0028	0.0030

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0184	0.0212	0.8726	0.9285
A to Z ↑	0.0154	0.0174	1.1355	1.2338
B to Z ↓	0.0181	0.0205	0.8723	0.9288
B to Z ↑	0.0137	0.0157	1.1349	1.2310
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0251	0.0286	1.0091	1.0807
A to Z ↑	0.0202	0.0226	1.3758	1.5075
B to Z ↓	0.0239	0.0271	1.0104	1.0812
B to Z ↑	0.0181	0.0203	1.3732	1.5061
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0170	0.0198	0.6834	0.7270
A to Z ↑	0.0160	0.0180	0.7915	0.8587
B to Z ↓	0.0168	0.0191	0.6834	0.7284
B to Z ↑	0.0139	0.0159	0.7910	0.8568
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0235	0.0270	0.7897	0.8453
A to Z ↑	0.0208	0.0233	0.9564	1.0484
B to Z ↓	0.0224	0.0255	0.7902	0.8464
B to Z ↑	0.0183	0.0205	0.9548	1.0464
	X33_P0	**X33_P4**	**X33_P0**	**X33_P4**
A to Z ↓	0.0226	0.0258	0.3957	0.4214
A to Z ↑	0.0190	0.0213	0.5342	0.5797
B to Z ↓	0.0222	0.0251	0.3959	0.4217
B to Z ↑	0.0171	0.0193	0.5331	0.5783
	X33_P10	**X33_P16**	**X33_P10**	**X33_P16**
A to Z ↓	0.0306	0.0349	0.4591	0.4917
A to Z ↑	0.0247	0.0276	0.6463	0.7084
B to Z ↓	0.0295	0.0333	0.4592	0.4926
B to Z ↑	0.0224	0.0249	0.6447	0.7070
	X37_P0	**X37_P4**	**X37_P0**	**X37_P4**
A to Z ↓	0.0203	0.0235	0.3829	0.4085
A to Z ↑	0.0182	0.0205	0.4374	0.4744
B to Z ↓	0.0204	0.0233	0.3833	0.4086
B to Z ↑	0.0165	0.0186	0.4365	0.4735
	X37_P10	**X37_P16**	**X37_P10**	**X37_P16**
A to Z ↓	0.0279	0.0316	0.4441	0.4758
A to Z ↑	0.0237	0.0263	0.5279	0.5783
B to Z ↓	0.0273	0.0308	0.4441	0.4762
B to Z ↑	0.0214	0.0238	0.5275	0.5775

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X15_P0	2.987e-05	1.000e-20

X15_P4	5.554e-06	1.000e-20
X15_P10	1.024e-06	1.000e-20
X15_P16	4.281e-07	1.000e-20
X20_P0	5.307e-05	1.000e-20
X20_P4	9.655e-06	1.000e-20
X20_P10	1.712e-06	1.000e-20
X20_P16	6.895e-07	1.000e-20
X33_P0	5.064e-05	1.000e-20
X33_P4	9.632e-06	1.000e-20
X33_P10	1.793e-06	1.000e-20
X33_P16	7.355e-07	1.000e-20
X37_P0	6.820e-05	1.000e-20
X37_P4	1.255e-05	1.000e-20
X37_P10	2.248e-06	1.000e-20
X37_P16	9.045e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.190e-04	1.144e-04	1.125e-04	1.150e-04
B (output stable)	2.283e-04	1.341e-04	7.056e-05	5.724e-05
A to Z	4.890e-03	4.715e-03	4.755e-03	4.904e-03
B to Z	4.354e-03	4.075e-03	3.989e-03	4.030e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	2.094e-04	2.011e-04	1.965e-04	1.986e-04
B (output stable)	3.880e-04	2.386e-04	9.798e-05	7.495e-05
A to Z	7.484e-03	7.265e-03	7.329e-03	7.617e-03
B to Z	6.584e-03	6.186e-03	6.041e-03	6.155e-03
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	1.602e-04	1.522e-04	1.493e-04	1.519e-04
B (output stable)	3.621e-04	2.036e-04	1.120e-04	9.335e-05
A to Z	9.251e-03	8.843e-03	8.872e-03	9.086e-03
B to Z	8.537e-03	7.974e-03	7.851e-03	7.939e-03
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	2.097e-04	2.003e-04	1.979e-04	2.023e-04
B (output stable)	3.916e-04	2.401e-04	1.031e-04	7.237e-05
A to Z	1.094e-02	1.058e-02	1.068e-02	1.088e-02
B to Z	1.006e-02	9.516e-03	9.377e-03	9.430e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X33_P0	X33_P4	X33_P10	X33_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

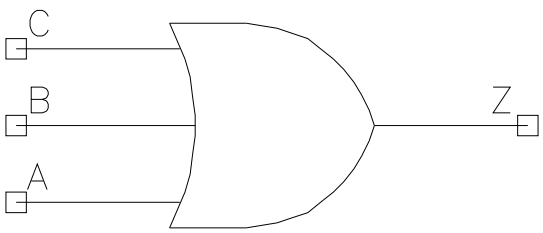
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR3

Cell Description

3 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	1.200	1.360	1.6320
X14_P4	1.200	1.360	1.6320
X14_P10	1.200	1.360	1.6320
X14_P16	1.200	1.360	1.6320
X20_P0	1.200	1.632	1.9584
X20_P4	1.200	1.632	1.9584
X20_P10	1.200	1.632	1.9584
X20_P16	1.200	1.632	1.9584

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0009	0.0010	0.0010	0.0011
B	0.0009	0.0009	0.0010	0.0011
C	0.0009	0.0009	0.0010	0.0011
	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0009	0.0009	0.0010	0.0011
B	0.0009	0.0009	0.0010	0.0011
C	0.0009	0.0009	0.0010	0.0011

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	X14_P4	X14_P0	X14_P4
A to Z ↓	0.0357	0.0404	0.9577	1.0207
A to Z ↑	0.0301	0.0340	1.1460	1.2424

B to Z ↓	0.0354	0.0404	0.9583	1.0209
B to Z ↑	0.0318	0.0359	1.1461	1.2422
C to Z ↓	0.0331	0.0373	0.9582	1.0198
C to Z ↑	0.0279	0.0314	1.1446	1.2410
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0475	0.0544	1.1090	1.1882
A to Z ↑	0.0396	0.0450	1.3832	1.5156
B to Z ↓	0.0478	0.0550	1.1087	1.1887
B to Z ↑	0.0417	0.0474	1.3840	1.5163
C to Z ↓	0.0436	0.0498	1.1080	1.1873
C to Z ↑	0.0366	0.0416	1.3814	1.5143
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0355	0.0403	0.7074	0.7535
A to Z ↑	0.0324	0.0368	0.8101	0.8785
B to Z ↓	0.0351	0.0402	0.7080	0.7540
B to Z ↑	0.0339	0.0385	0.8111	0.8795
C to Z ↓	0.0321	0.0363	0.7075	0.7528
C to Z ↑	0.0308	0.0349	0.8108	0.8792
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0475	0.0542	0.8194	0.8773
A to Z ↑	0.0434	0.0494	0.9788	1.0721
B to Z ↓	0.0477	0.0547	0.8194	0.8773
B to Z ↑	0.0452	0.0514	0.9790	1.0717
C to Z ↓	0.0427	0.0485	0.8187	0.8776
C to Z ↑	0.0411	0.0468	0.9788	1.0717

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X14_P0	4.465e-05	1.000e-20
X14_P4	8.246e-06	1.000e-20
X14_P10	1.512e-06	1.000e-20
X14_P16	6.268e-07	1.000e-20
X20_P0	5.229e-05	1.000e-20
X20_P4	9.740e-06	1.000e-20
X20_P10	1.792e-06	1.000e-20
X20_P16	7.374e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	6.112e-04	5.670e-04	5.365e-04	5.465e-04
B (output stable)	6.661e-04	6.537e-04	6.720e-04	7.067e-04
C (output stable)	1.522e-03	1.400e-03	1.340e-03	1.331e-03
A to Z	6.927e-03	6.858e-03	7.001e-03	7.290e-03
B to Z	7.139e-03	7.124e-03	7.336e-03	7.675e-03
C to Z	6.834e-03	6.714e-03	6.824e-03	7.084e-03
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	5.956e-04	5.492e-04	5.188e-04	5.274e-04
B (output stable)	6.481e-04	6.329e-04	6.475e-04	6.790e-04
C (output stable)	1.438e-03	1.316e-03	1.249e-03	1.231e-03
A to Z	8.306e-03	8.262e-03	8.480e-03	8.802e-03
B to Z	8.516e-03	8.525e-03	8.802e-03	9.171e-03

C to Z	8.171e-03	8.087e-03	8.270e-03	8.560e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

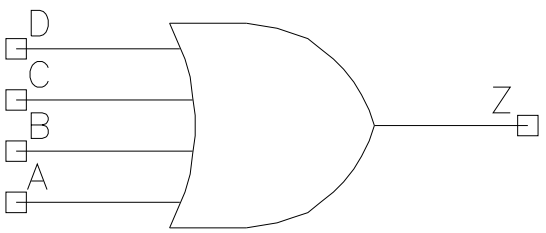
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR4

Cell Description

4 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X20_P0	1.200	2.176	2.6112
X20_P4	1.200	2.176	2.6112
X20_P10	1.200	2.176	2.6112
X20_P16	1.200	2.176	2.6112
X27_P0	1.200	2.312	2.7744
X27_P4	1.200	2.312	2.7744
X27_P10	1.200	2.312	2.7744
X27_P16	1.200	2.312	2.7744

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X20_P0	X20_P4	X20_P10	X20_P16
A	0.0013	0.0013	0.0014	0.0015
B	0.0014	0.0015	0.0016	0.0017
C	0.0013	0.0014	0.0015	0.0016
D	0.0014	0.0015	0.0016	0.0017
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0013	0.0014	0.0014	0.0015
B	0.0014	0.0015	0.0016	0.0016
C	0.0013	0.0014	0.0015	0.0016
D	0.0015	0.0016	0.0017	0.0018

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X20_P0	**X20_P4**	**X20_P0**	**X20_P4**
A to Z ↓	0.0252	0.0288	0.7002	0.7489
A to Z ↑	0.0249	0.0280	0.9445	1.0276
B to Z ↓	0.0237	0.0272	0.7003	0.7490
B to Z ↑	0.0232	0.0261	0.9439	1.0267
C to Z ↓	0.0240	0.0272	0.6976	0.7467
C to Z ↑	0.0238	0.0266	0.9354	1.0187
D to Z ↓	0.0230	0.0261	0.6970	0.7463
D to Z ↑	0.0223	0.0248	0.9360	1.0181
	X20_P10	**X20_P16**	**X20_P10**	**X20_P16**
A to Z ↓	0.0337	0.0385	0.8187	0.8826
A to Z ↑	0.0322	0.0366	1.1475	1.2585
B to Z ↓	0.0317	0.0364	0.8190	0.8833
B to Z ↑	0.0299	0.0340	1.1456	1.2561
C to Z ↓	0.0320	0.0358	0.8169	0.8798
C to Z ↑	0.0308	0.0340	1.1383	1.2502
D to Z ↓	0.0306	0.0342	0.8170	0.8795
D to Z ↑	0.0286	0.0315	1.1379	1.2487
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0275	0.0314	0.5766	0.6171
A to Z ↑	0.0264	0.0298	0.7075	0.7696
B to Z ↓	0.0262	0.0299	0.5769	0.6177
B to Z ↑	0.0249	0.0280	0.7069	0.7688
C to Z ↓	0.0251	0.0284	0.5736	0.6136
C to Z ↑	0.0243	0.0272	0.7007	0.7638
D to Z ↓	0.0241	0.0274	0.5734	0.6138
D to Z ↑	0.0223	0.0249	0.7004	0.7615
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0369	0.0418	0.6756	0.7290
A to Z ↑	0.0345	0.0388	0.8591	0.9428
B to Z ↓	0.0351	0.0399	0.6759	0.7292
B to Z ↑	0.0325	0.0364	0.8584	0.9418
C to Z ↓	0.0334	0.0379	0.6720	0.7247
C to Z ↑	0.0315	0.0353	0.8524	0.9363
D to Z ↓	0.0321	0.0364	0.6718	0.7247
D to Z ↑	0.0288	0.0322	0.8505	0.9340

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X20_P0	4.190e-05	1.000e-20
X20_P4	8.023e-06	1.000e-20
X20_P10	1.594e-06	1.000e-20
X20_P16	7.300e-07	1.000e-20
X27_P0	4.516e-05	1.000e-20
X27_P4	8.675e-06	1.000e-20
X27_P10	1.746e-06	1.000e-20
X27_P16	8.121e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	1.783e-03	1.816e-03	1.879e-03	2.013e-03

B (output stable)	1.633e-03	1.592e-03	1.578e-03	1.686e-03
C (output stable)	1.792e-03	1.822e-03	1.897e-03	1.950e-03
D (output stable)	1.639e-03	1.592e-03	1.581e-03	1.576e-03
A to Z	8.535e-03	8.577e-03	8.815e-03	9.284e-03
B to Z	8.140e-03	8.079e-03	8.199e-03	8.598e-03
C to Z	7.921e-03	7.725e-03	7.864e-03	7.962e-03
D to Z	7.527e-03	7.224e-03	7.232e-03	7.260e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	2.051e-03	2.109e-03	2.226e-03	2.358e-03
B (output stable)	1.899e-03	1.880e-03	1.927e-03	2.035e-03
C (output stable)	1.884e-03	1.920e-03	2.011e-03	2.092e-03
D (output stable)	1.735e-03	1.688e-03	1.699e-03	1.714e-03
A to Z	1.023e-02	1.021e-02	1.048e-02	1.092e-02
B to Z	9.831e-03	9.703e-03	9.872e-03	1.025e-02
C to Z	8.980e-03	8.699e-03	8.776e-03	9.054e-03
D to Z	8.604e-03	8.215e-03	8.181e-03	8.373e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

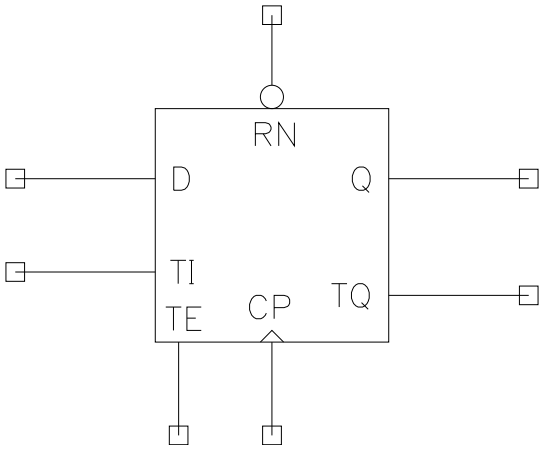
Pin Cycle (vdds)	X20_P0	X20_P4	X20_P10	X20_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNSDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.080	4.8960
X15_P4	1.200	4.080	4.8960
X15_P10	1.200	4.080	4.8960
X15_P16	1.200	4.080	4.8960

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0008	0.0008	0.0009	0.0009
D	0.0006	0.0007	0.0007	0.0007
RN	0.0008	0.0009	0.0009	0.0009

TE	0.0010	0.0010	0.0011	0.0011
TI	0.0003	0.0003	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	X15_P4	X15_P0	X15_P4
CP to Q ↓	0.0545	0.0613	0.9684	1.0299
CP to Q ↑	0.0573	0.0644	1.0689	1.1594
CP to TQ ↓	0.0559	0.0630	4.5477	4.8180
CP to TQ ↑	0.0616	0.0693	9.9487	11.1004
RN to Q ↓	0.0649	0.0739	0.9659	1.0292
RN to TQ ↓	0.0663	0.0756	4.5450	4.8144
	X15_P10	X15_P16	X15_P10	X15_P16
CP to Q ↓	0.0717	0.0816	1.1188	1.1967
CP to Q ↑	0.0750	0.0849	1.2911	1.4146
CP to TQ ↓	0.0738	0.0840	5.1887	5.5086
CP to TQ ↑	0.0807	0.0914	12.6636	14.0194
RN to Q ↓	0.0873	0.1000	1.1176	1.1946
RN to TQ ↓	0.0894	0.1023	5.1863	5.5063

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.0555	0.0649	0.0806	0.0940
CP ↑	min_pulse_width to CP	0.0311	0.0344	0.0389	0.0434
D ↓	hold_rising to CP	-0.0023	-0.0077	-0.0094	-0.0143
D ↑	hold_rising to CP	-0.0071	-0.0062	-0.0120	-0.0169
D ↓	setup_rising to CP	0.0370	0.0419	0.0542	0.0645
D ↑	setup_rising to CP	0.0346	0.0368	0.0416	0.0491
RN ↓	min_pulse_width to RN	0.0496	0.0566	0.0637	0.0708
RN ↑	recovery_rising to CP	0.0103	0.0151	0.0173	0.0228
RN ↑	removal_rising to CP	-0.0029	-0.0055	-0.0077	-0.0077
TE ↓	hold_rising to CP	-0.0001	-0.0023	-0.0072	-0.0147
TE ↑	hold_rising to CP	-0.0147	-0.0196	-0.0245	-0.0299
TE ↓	setup_rising to CP	0.0489	0.0533	0.0657	0.0732
TE ↑	setup_rising to CP	0.0715	0.0867	0.1052	0.1248
TI ↓	hold_rising to CP	-0.0342	-0.0440	-0.0550	-0.0704
TI ↑	hold_rising to CP	-0.0153	-0.0159	-0.0231	-0.0280
TI ↓	setup_rising to CP	0.0722	0.0832	0.1050	0.1202
TI ↑	setup_rising to CP	0.0410	0.0466	0.0528	0.0625

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X15_P0	7.672e-05	1.000e-20
X15_P4	1.390e-05	1.000e-20
X15_P10	2.566e-06	1.000e-20
X15_P16	1.117e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

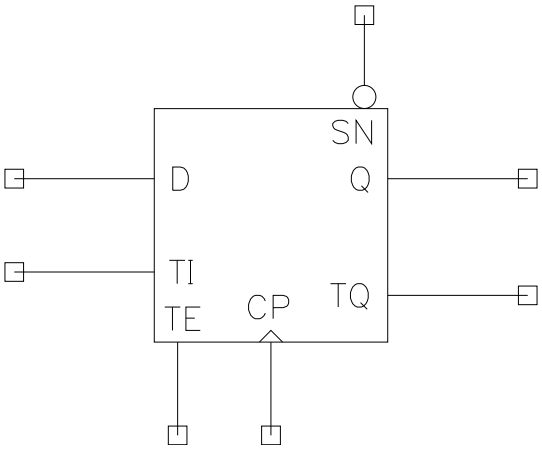
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	9.742e-03	9.698e-03	9.738e-03	9.821e-03
Clock 100Mhz Data 25Mhz	1.030e-02	1.027e-02	1.039e-02	1.056e-02
Clock 100Mhz Data 50Mhz	1.086e-02	1.084e-02	1.104e-02	1.131e-02
Clock = 0 Data 100Mhz	4.381e-03	4.412e-03	4.475e-03	4.551e-03
Clock = 1 Data 100Mhz	5.588e-05	5.191e-05	4.879e-05	4.666e-05

CNSDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X15_P0	1.200	4.216	5.0592
X15_P4	1.200	4.216	5.0592
X15_P10	1.200	4.216	5.0592
X15_P16	1.200	4.216	5.0592

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X15_P0	X15_P4	X15_P10	X15_P16
CP	0.0008	0.0008	0.0009	0.0009
D	0.0004	0.0004	0.0005	0.0005
SN	0.0016	0.0016	0.0016	0.0018

TE	0.0010	0.0010	0.0011	0.0011
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X15_P0	X15_P4	X15_P0	X15_P4
CP to Q ↓	0.0547	0.0616	0.9690	1.0312
CP to Q ↑	0.0577	0.0648	1.0685	1.1594
CP to TQ ↓	0.0561	0.0633	4.5572	4.8284
CP to TQ ↑	0.0620	0.0698	9.9482	11.1071
SN to Q ↑	0.0546	0.0617	1.0688	1.1598
SN to TQ ↑	0.0590	0.0667	9.9504	11.1101
	X15_P10	X15_P16	X15_P10	X15_P16
CP to Q ↓	0.0719	0.0817	1.1184	1.1966
CP to Q ↑	0.0754	0.0853	1.2915	1.4157
CP to TQ ↓	0.0741	0.0842	5.2004	5.5217
CP to TQ ↑	0.0813	0.0921	12.6715	14.0270
SN to Q ↑	0.0720	0.0816	1.2900	1.4137
SN to TQ ↑	0.0779	0.0884	12.6744	14.0282

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X15_P0	X15_P4	X15_P10	X15_P16
CP ↓	min_pulse_width to CP	0.0620	0.0737	0.0877	0.1028
CP ↑	min_pulse_width to CP	0.0345	0.0344	0.0389	0.0434
D ↓	hold_rising to CP	-0.0072	-0.0068	-0.0143	-0.0192
D ↑	hold_rising to CP	-0.0049	-0.0071	-0.0120	-0.0142
D ↓	setup_rising to CP	0.0419	0.0463	0.0587	0.0684
D ↑	setup_rising to CP	0.0293	0.0314	0.0367	0.0416
SN ↓	min_pulse_width to SN	0.0354	0.0376	0.0447	0.0496
SN ↑	recovery_rising to CP	-0.0017	0.0005	0.0005	0.0031
SN ↑	removal_rising to CP	0.0237	0.0260	0.0287	0.0303
TE ↓	hold_rising to CP	-0.0023	-0.0072	-0.0121	-0.0175
TE ↑	hold_rising to CP	-0.0088	-0.0143	-0.0218	-0.0267
TE ↓	setup_rising to CP	0.0431	0.0506	0.0608	0.0689
TE ↑	setup_rising to CP	0.0786	0.0933	0.1128	0.1355
TI ↓	hold_rising to CP	-0.0391	-0.0488	-0.0655	-0.0759
TI ↑	hold_rising to CP	-0.0097	-0.0169	-0.0218	-0.0244
TI ↓	setup_rising to CP	0.0786	0.0940	0.1092	0.1310
TI ↑	setup_rising to CP	0.0404	0.0410	0.0479	0.0586

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X15_P0	7.113e-05	1.000e-20
X15_P4	1.315e-05	1.000e-20
X15_P10	2.500e-06	1.000e-20
X15_P16	1.116e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

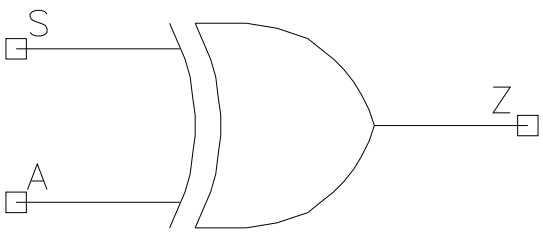
Pin Cycle	X15_P0	X15_P4	X15_P10	X15_P16
Clock 100Mhz Data 0Mhz	9.826e-03	9.780e-03	9.816e-03	9.894e-03
Clock 100Mhz Data 25Mhz	1.042e-02	1.038e-02	1.050e-02	1.067e-02
Clock 100Mhz Data 50Mhz	1.101e-02	1.099e-02	1.119e-02	1.145e-02
Clock = 0 Data 100Mhz	4.422e-03	4.448e-03	4.511e-03	4.588e-03
Clock = 1 Data 100Mhz	5.576e-05	5.211e-05	5.129e-05	5.098e-05

CNXOR2

Cell Description

2 input Exclusive OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X16_P0	1.200	1.360	1.6320
X16_P4	1.200	1.360	1.6320
X16_P10	1.200	1.360	1.6320
X16_P16	1.200	1.360	1.6320
X27_P0	1.200	2.040	2.4480
X27_P4	1.200	2.040	2.4480
X27_P10	1.200	2.040	2.4480
X27_P16	1.200	2.040	2.4480

Truth Table

A	S	Z
1	S	!S
0	S	S

Pin Capacitance

Pin	X16_P0	X16_P4	X16_P10	X16_P16
A	0.0011	0.0011	0.0012	0.0013
S	0.0015	0.0016	0.0018	0.0019
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0016	0.0016	0.0018	0.0019
S	0.0022	0.0023	0.0024	0.0025

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X16_P0	**X16_P4**	**X16_P0**	**X16_P4**
A to Z ↓	0.0289	0.0327	0.8143	0.8677
A to Z ↑	0.0270	0.0303	1.0989	1.1939
S to Z ↓	0.0225	0.0254	0.8121	0.8656
S to Z ↑	0.0217	0.0245	1.0970	1.1923
	X16_P10	**X16_P16**	**X16_P10**	**X16_P16**
A to Z ↓	0.0379	0.0433	0.9436	1.0124

A to Z ↑	0.0348	0.0394	1.3317	1.4613
S to Z ↓	0.0293	0.0334	0.9410	1.0109
S to Z ↑	0.0283	0.0321	1.3301	1.4603
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0298	0.0336	0.5422	0.5782
A to Z ↑	0.0292	0.0328	0.5890	0.6404
S to Z ↓	0.0248	0.0280	0.5414	0.5779
S to Z ↑	0.0245	0.0275	0.5894	0.6402
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0394	0.0445	0.6299	0.6757
A to Z ↑	0.0383	0.0431	0.7147	0.7839
S to Z ↓	0.0326	0.0369	0.6290	0.6757
S to Z ↑	0.0320	0.0361	0.7141	0.7833

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X16_P0	7.369e-05	1.000e-20
X16_P4	1.301e-05	1.000e-20
X16_P10	2.192e-06	1.000e-20
X16_P16	8.206e-07	1.000e-20
X27_P0	1.207e-04	1.000e-20
X27_P4	2.080e-05	1.000e-20
X27_P10	3.383e-06	1.000e-20
X27_P16	1.233e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	7.429e-03	7.110e-03	6.989e-03	7.174e-03
S to Z	6.382e-03	6.004e-03	5.813e-03	5.935e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	1.325e-02	1.258e-02	1.248e-02	1.260e-02
S to Z	1.018e-02	9.513e-03	9.265e-03	9.342e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

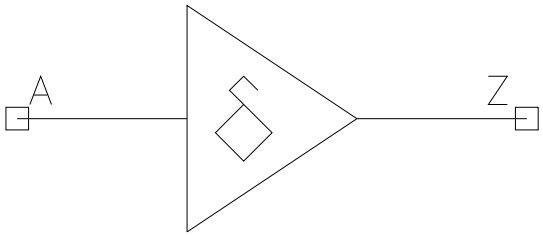
Pin Cycle (vdds)	X16_P0	X16_P4	X16_P10	X16_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DLYHF

Cell Description

Delay cell for Hold Time Fixing

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C12T28SOI_LL_-DLYHFM4X7_P0	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X7_P4	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X7_P10	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X7_P16	1.200	1.088	1.3056
C12T28SOI_LL_-DLYHFM4X15_P0	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM4X15_P4	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM4X15_P10	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM4X15_P16	1.200	1.224	1.4688
C12T28SOI_LL_-DLYHFM8X7_P0	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X7_P4	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X7_P10	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X7_P16	1.200	1.904	2.2848
C12T28SOI_LL_-DLYHFM8X15_P0	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X15_P4	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X15_P10	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X15_P16	1.200	2.040	2.4480
C12T28SOI_LL_-DLYHFM8X54_P0	1.200	4.216	5.0592

C12T28SOI_LL_-DLYHFM8X54_P4	1.200	4.216	5.0592
C12T28SOI_LL_-DLYHFM8X54_P10	1.200	4.216	5.0592
C12T28SOI_LL_-DLYHFM8X54_P16	1.200	4.216	5.0592

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C12T28SOI_LL_-DLYHFM4X7_P0	C12T28SOI_LL_-DLYHFM4X7_P4	C12T28SOI_LL_-DLYHFM4X7_P10	C12T28SOI_LL_-DLYHFM4X7_P16
A	0.0008	0.0008	0.0008	0.0009
	C12T28SOI_LL_-DLYHFM4X15_P0	C12T28SOI_LL_-DLYHFM4X15_P4	C12T28SOI_LL_-DLYHFM4X15_P10	C12T28SOI_LL_-DLYHFM4X15_P16
A	0.0008	0.0008	0.0008	0.0009
	C12T28SOI_LL_-DLYHFM8X7_P0	C12T28SOI_LL_-DLYHFM8X7_P4	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A	0.0008	0.0008	0.0008	0.0008
	C12T28SOI_LL_-DLYHFM8X15_P0	C12T28SOI_LL_-DLYHFM8X15_P4	C12T28SOI_LL_-DLYHFM8X15_P10	C12T28SOI_LL_-DLYHFM8X15_P16
A	0.0007	0.0008	0.0008	0.0008
	C12T28SOI_LL_-DLYHFM8X54_P0	C12T28SOI_LL_-DLYHFM8X54_P4	C12T28SOI_LL_-DLYHFM8X54_P10	C12T28SOI_LL_-DLYHFM8X54_P16
A	0.0007	0.0008	0.0008	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C12T28SOI_LL_-DLYHFM4X7_P0	**C12T28SOI_LL_-DLYHFM4X7_P4**	**C12T28SOI_LL_-DLYHFM4X7_P0**	**C12T28SOI_LL_-DLYHFM4X7_P4**
A to Z ↓	0.0767	0.0865	1.8648	1.9912
A to Z ↑	0.0738	0.0835	2.5242	2.7449
	C12T28SOI_LL_-DLYHFM4X7_P10	**C12T28SOI_LL_-DLYHFM4X7_P16**	**C12T28SOI_LL_-DLYHFM4X7_P10**	**C12T28SOI_LL_-DLYHFM4X7_P16**
A to Z ↓	0.1016	0.1164	2.1759	2.3433
A to Z ↑	0.0984	0.1129	3.0674	3.3662
	C12T28SOI_LL_-DLYHFM4X15_P0	**C12T28SOI_LL_-DLYHFM4X15_P4**	**C12T28SOI_LL_-DLYHFM4X15_P0**	**C12T28SOI_LL_-DLYHFM4X15_P4**
A to Z ↓	0.0830	0.0937	0.9040	0.9695
A to Z ↑	0.0814	0.0921	1.1659	1.2704
	C12T28SOI_LL_-DLYHFM4X15_P10	**C12T28SOI_LL_-DLYHFM4X15_P16**	**C12T28SOI_LL_-DLYHFM4X15_P10**	**C12T28SOI_LL_-DLYHFM4X15_P16**
A to Z ↓	0.1104	0.1271	1.0627	1.1494
A to Z ↑	0.1089	0.1253	1.4215	1.5639
	C12T28SOI_LL_-DLYHFM8X7_P0	**C12T28SOI_LL_-DLYHFM8X7_P4**	**C12T28SOI_LL_-DLYHFM8X7_P0**	**C12T28SOI_LL_-DLYHFM8X7_P4**
A to Z ↓	0.1348	0.1525	1.8717	2.0033
A to Z ↑	0.1258	0.1425	2.3335	2.5361

	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A to Z ↓	0.1802	0.2075	2.1911	2.3598
A to Z ↑	0.1684	0.1936	2.8327	3.1113
	C12T28SOI_LL_-DLYHFM8X15_P0	**C12T28SOI_LL_-DLYHFM8X15_P4**	**C12T28SOI_LL_-DLYHFM8X15_P0**	**C12T28SOI_LL_-DLYHFM8X15_P4**
A to Z ↓	0.1401	0.1588	0.9040	0.9700
A to Z ↑	0.1335	0.1513	1.1678	1.2729
	C12T28SOI_LL_-DLYHFM8X15_P10	**C12T28SOI_LL_-DLYHFM8X15_P16**	**C12T28SOI_LL_-DLYHFM8X15_P10**	**C12T28SOI_LL_-DLYHFM8X15_P16**
A to Z ↓	0.1880	0.2168	1.0660	1.1535
A to Z ↑	0.1790	0.2062	1.4236	1.5661
	C12T28SOI_LL_-DLYHFM8X54_P0	**C12T28SOI_LL_-DLYHFM8X54_P4**	**C12T28SOI_LL_-DLYHFM8X54_P0**	**C12T28SOI_LL_-DLYHFM8X54_P4**
A to Z ↓	0.1838	0.2092	0.2428	0.2591
A to Z ↑	0.1669	0.1900	0.3350	0.3633
	C12T28SOI_LL_-DLYHFM8X54_P10	**C12T28SOI_LL_-DLYHFM8X54_P16**	**C12T28SOI_LL_-DLYHFM8X54_P10**	**C12T28SOI_LL_-DLYHFM8X54_P16**
A to Z ↓	0.2481	0.2879	0.2821	0.3027
A to Z ↑	0.2256	0.2624	0.4048	0.4435

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C12T28SOI_LL_DLYHFM4X7_P0	1.041e-05	1.000e-20
C12T28SOI_LL_DLYHFM4X7_P4	1.968e-06	1.000e-20
C12T28SOI_LL_DLYHFM4X7_P10	4.196e-07	1.000e-20
C12T28SOI_LL_DLYHFM4X7_P16	2.214e-07	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P0	2.293e-05	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P4	4.134e-06	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P10	7.768e-07	1.000e-20
C12T28SOI_LL_DLYHFM4X15_P16	3.560e-07	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P0	1.155e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P4	2.232e-06	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P10	5.115e-07	1.000e-20
C12T28SOI_LL_DLYHFM8X7_P16	2.931e-07	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P0	2.326e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P4	4.263e-06	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P10	8.497e-07	1.000e-20
C12T28SOI_LL_DLYHFM8X15_P16	4.219e-07	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P0	8.040e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P4	1.518e-05	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P10	3.095e-06	1.000e-20
C12T28SOI_LL_DLYHFM8X54_P16	1.556e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C12T28SOI_LL_-DLYHFM4X7_P0	C12T28SOI_LL_-DLYHFM4X7_P4	C12T28SOI_LL_-DLYHFM4X7_P10	C12T28SOI_LL_-DLYHFM4X7_P16
A to Z	4.605e-03	4.598e-03	4.725e-03	4.907e-03
	C12T28SOI_LL_-DLYHFM4X15_P0	C12T28SOI_LL_-DLYHFM4X15_P4	C12T28SOI_LL_-DLYHFM4X15_P10	C12T28SOI_LL_-DLYHFM4X15_P16
A to Z	7.143e-03	6.829e-03	6.770e-03	6.895e-03

	C12T28SOI_LL_-DLYHFM8X7_P0	C12T28SOI_LL_-DLYHFM8X7_P4	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A to Z	7.222e-03	7.259e-03	7.490e-03	7.776e-03
	C12T28SOI_LL_-DLYHFM8X15_P0	C12T28SOI_LL_-DLYHFM8X15_P4	C12T28SOI_LL_-DLYHFM8X15_P10	C12T28SOI_LL_-DLYHFM8X15_P16
A to Z	9.738e-03	9.480e-03	9.509e-03	9.739e-03
	C12T28SOI_LL_-DLYHFM8X54_P0	C12T28SOI_LL_-DLYHFM8X54_P4	C12T28SOI_LL_-DLYHFM8X54_P10	C12T28SOI_LL_-DLYHFM8X54_P16
A to Z	2.980e-02	2.991e-02	3.077e-02	3.230e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

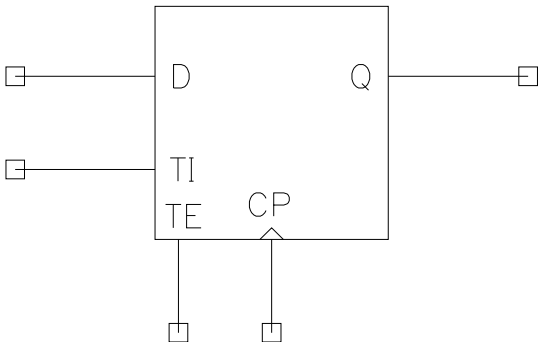
Pin Cycle (vdds)	C12T28SOI_LL_-DLYHFM4X7_P0	C12T28SOI_LL_-DLYHFM4X7_P4	C12T28SOI_LL_-DLYHFM4X7_P10	C12T28SOI_LL_-DLYHFM4X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM4X15_P0	C12T28SOI_LL_-DLYHFM4X15_P4	C12T28SOI_LL_-DLYHFM4X15_P10	C12T28SOI_LL_-DLYHFM4X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM8X7_P0	C12T28SOI_LL_-DLYHFM8X7_P4	C12T28SOI_LL_-DLYHFM8X7_P10	C12T28SOI_LL_-DLYHFM8X7_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM8X15_P0	C12T28SOI_LL_-DLYHFM8X15_P4	C12T28SOI_LL_-DLYHFM8X15_P10	C12T28SOI_LL_-DLYHFM8X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C12T28SOI_LL_-DLYHFM8X54_P0	C12T28SOI_LL_-DLYHFM8X54_P4	C12T28SOI_LL_-DLYHFM8X54_P10	C12T28SOI_LL_-DLYHFM8X54_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFSYNCPQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.400	8.1600
X8_P4	2.400	3.400	8.1600
X8_P10	2.400	3.400	8.1600
X8_P16	2.400	3.400	8.1600

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0009	0.0009	0.0010	0.0010
D	0.0006	0.0007	0.0007	0.0008
TE	0.0010	0.0010	0.0011	0.0011
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X8_P4	X8_P0	X8_P4
CP to Q ↓	0.0906	0.1029	1.5100	1.6127
CP to Q ↑	0.1051	0.1190	2.1435	2.3272

	X8_P10	X8_P16	X8_P10	X8_P16
CP to Q ↓	0.1221	0.1405	1.7512	1.8777
CP to Q ↑	0.1404	0.1617	2.5940	2.8465

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1313	0.1535	0.1840	0.2155
CP ↑	min_pulse_width to CP	0.0549	0.0594	0.0686	0.0792
D ↓	hold_rising to CP	-0.0316	-0.0414	-0.0538	-0.0632
D ↑	hold_rising to CP	-0.0147	-0.0163	-0.0218	-0.0289
D ↓	setup_rising to CP	0.0759	0.0883	0.1057	0.1230
D ↑	setup_rising to CP	0.0417	0.0466	0.0514	0.0562
TE ↓	hold_rising to CP	-0.0294	-0.0365	-0.0485	-0.0583
TE ↑	hold_rising to CP	-0.0387	-0.0462	-0.0559	-0.0657
TE ↓	setup_rising to CP	0.0745	0.0859	0.1005	0.1177
TE ↑	setup_rising to CP	0.1470	0.1714	0.2082	0.2425
TI ↓	hold_rising to CP	-0.0961	-0.1136	-0.1437	-0.1694
TI ↑	hold_rising to CP	-0.0410	-0.0475	-0.0586	-0.0683
TI ↓	setup_rising to CP	0.1456	0.1680	0.2028	0.2370
TI ↑	setup_rising to CP	0.0710	0.0771	0.0884	0.0981

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	9.003e-05	1.000e-20
X8_P4	1.692e-05	1.000e-20
X8_P10	3.371e-06	1.000e-20
X8_P16	1.608e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

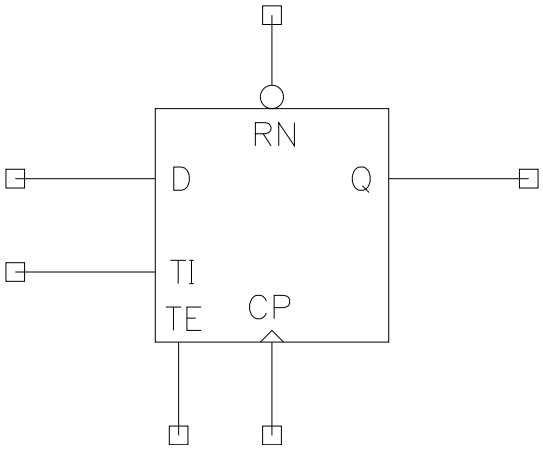
Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	1.892e-02	1.917e-02	1.960e-02	2.009e-02
Clock 100Mhz Data 25Mhz	1.946e-02	1.958e-02	2.003e-02	2.061e-02
Clock 100Mhz Data 50Mhz	2.000e-02	2.000e-02	2.047e-02	2.113e-02
Clock = 0 Data 100Mhz	1.006e-02	9.884e-03	9.798e-03	9.832e-03
Clock = 1 Data 100Mhz	4.767e-05	4.415e-05	4.525e-05	5.488e-05

SDFSYNCPRQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0009	0.0009	0.0010	0.0010
D	0.0007	0.0007	0.0007	0.0008
RN	0.0019	0.0020	0.0021	0.0023
TE	0.0010	0.0010	0.0011	0.0011
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	X8_P4	X8_P0	X8_P4
CP to Q ↓	0.0992	0.1128	1.5172	1.6191
CP to Q ↑	0.1060	0.1202	2.1325	2.3158
RN to Q ↓	0.1027	0.1184	1.5182	1.6177
	X8_P10	X8_P16	X8_P10	X8_P16
CP to Q ↓	0.1335	0.1537	1.7636	1.8913
CP to Q ↑	0.1419	0.1639	2.5806	2.8340
RN to Q ↓	0.1418	0.1643	1.7620	1.8907

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1307	0.1517	0.1840	0.2138
CP ↑	min_pulse_width to CP	0.0548	0.0627	0.0732	0.0825
D ↓	hold_rising to CP	-0.0316	-0.0365	-0.0485	-0.0583
D ↑	hold_rising to CP	-0.0142	-0.0163	-0.0234	-0.0316
D ↓	setup_rising to CP	0.0764	0.0862	0.1035	0.1175
D ↑	setup_rising to CP	0.0412	0.0466	0.0514	0.0562
RN ↓	min_pulse_width to RN	0.0903	0.1023	0.1218	0.1387
RN ↑	recovery_rising to CP	0.0103	0.0103	0.0125	0.0130
RN ↑	removal_rising to CP	-0.0055	-0.0051	-0.0077	-0.0082
TE ↓	hold_rising to CP	-0.0267	-0.0365	-0.0468	-0.0566
TE ↑	hold_rising to CP	-0.0413	-0.0462	-0.0560	-0.0657
TE ↓	setup_rising to CP	0.0713	0.0810	0.0982	0.1156
TE ↑	setup_rising to CP	0.1448	0.1691	0.2029	0.2376
TI ↓	hold_rising to CP	-0.0971	-0.1123	-0.1378	-0.1645
TI ↑	hold_rising to CP	-0.0426	-0.0465	-0.0586	-0.0683
TI ↓	setup_rising to CP	0.1420	0.1671	0.1970	0.2321
TI ↑	setup_rising to CP	0.0723	0.0771	0.0884	0.0981

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	9.194e-05	1.000e-20
X8_P4	1.736e-05	1.000e-20
X8_P10	3.587e-06	1.000e-20
X8_P16	1.817e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	1.967e-02	1.993e-02	2.041e-02	2.100e-02

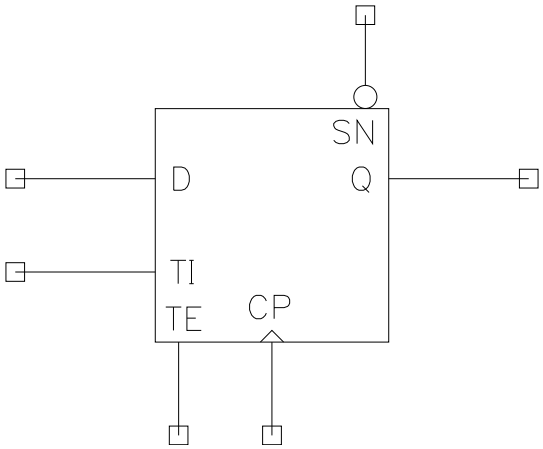
Clock 100Mhz Data 25Mhz	2.012e-02	2.027e-02	2.077e-02	2.147e-02
Clock 100Mhz Data 50Mhz	2.058e-02	2.060e-02	2.112e-02	2.195e-02
Clock = 0 Data 100Mhz	9.924e-03	9.790e-03	9.738e-03	9.772e-03
Clock = 1 Data 100Mhz	4.780e-05	4.434e-05	5.985e-05	8.192e-05

SDFSYNCPSQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	2.400	3.944	9.4656
X8_P4	2.400	3.944	9.4656
X8_P10	2.400	3.944	9.4656
X8_P16	2.400	3.944	9.4656

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
CP	0.0009	0.0009	0.0010	0.0010
D	0.0004	0.0005	0.0005	0.0005
SN	0.0017	0.0018	0.0019	0.0020
TE	0.0010	0.0010	0.0011	0.0011
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
CP to Q ↓	0.0770	0.0866	1.7924	1.9388
CP to Q ↑	0.0911	0.1029	2.2869	2.4979
SN to Q ↑	0.1086	0.1233	2.1880	2.3867
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
CP to Q ↓	0.1012	0.1152	2.1574	2.3619
CP to Q ↑	0.1214	0.1396	2.8025	3.0880
SN to Q ↑	0.1460	0.1679	2.6741	2.9404

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X8_P0	X8_P4	X8_P10	X8_P16
CP ↓	min_pulse_width to CP	0.1235	0.1447	0.1769	0.2061
CP ↑	min_pulse_width to CP	0.0562	0.0642	0.0733	0.0859
D ↓	hold_rising to CP	-0.0240	-0.0321	-0.0387	-0.0485
D ↑	hold_rising to CP	-0.0142	-0.0165	-0.0240	-0.0289
D ↓	setup_rising to CP	0.0684	0.0781	0.0986	0.1132
D ↑	setup_rising to CP	0.0417	0.0465	0.0514	0.0588
SN ↓	min_pulse_width to SN	0.1060	0.1179	0.1401	0.1597
SN ↑	recovery_rising to CP	-0.0039	-0.0013	-0.0017	-0.0012
SN ↑	removal_rising to CP	0.0356	0.0379	0.0423	0.0505
TE ↓	hold_rising to CP	-0.0218	-0.0267	-0.0371	-0.0436
TE ↑	hold_rising to CP	-0.0407	-0.0488	-0.0559	-0.0679
TE ↓	setup_rising to CP	0.0662	0.0761	0.0933	0.1079
TE ↑	setup_rising to CP	0.1399	0.1643	0.1980	0.2348
TI ↓	hold_rising to CP	-0.0879	-0.1039	-0.1339	-0.1596
TI ↑	hold_rising to CP	-0.0459	-0.0524	-0.0583	-0.0697
TI ↓	setup_rising to CP	0.1371	0.1579	0.1936	0.2285
TI ↑	setup_rising to CP	0.0715	0.0820	0.0932	0.1029

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	7.854e-05	1.000e-20
X8_P4	1.554e-05	1.000e-20
X8_P10	3.389e-06	1.000e-20
X8_P16	1.762e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	X8_P0	X8_P4	X8_P10	X8_P16
Clock 100Mhz Data 0Mhz	1.938e-02	1.965e-02	2.009e-02	2.063e-02

Clock 100Mhz Data 25Mhz	1.971e-02	1.979e-02	2.020e-02	2.078e-02
Clock 100Mhz Data 50Mhz	2.005e-02	1.992e-02	2.030e-02	2.092e-02
Clock = 0 Data 100Mhz	9.864e-03	9.787e-03	9.788e-03	9.860e-03
Clock = 1 Data 100Mhz	5.839e-05	5.427e-05	5.103e-05	5.918e-05

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