C28SOI_SC_12_CORE_LR

User Manual

12 track Standard Cell Library comprising commonly used booleans and sequential cells

Overview

Features

- The C28SOI_SC_12_CORE_LR Standard Cell library contains 383 cells.

Application

- Design needs in CMOS28FDSOI platform IPs.

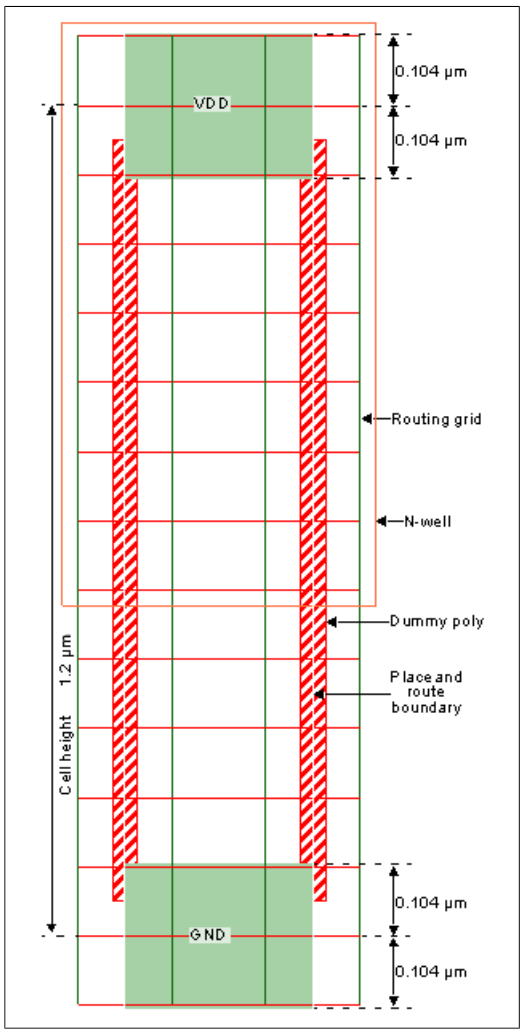
Library Architecture

This section illustrates the architecture used for C28SOI_SC_12_CORE_LR Standard Cell library.

Following table shows the Physical Specifications for this library.

Parameter	Value	Unit
Drawn Gate Length	0.030	µm
Layout Grid	0.001	µm
Vertical Pin Grid	0.1	µm
Horizontal Pin Grid	0.136	µm
Cell Power and Ground Rail Width	0.206	µm

Figure 1: Cell Architecture



1. Quick References

	Refer to the Naming Convention Document available in Design Package for more details regarding cell names.

	Refer to the Standard Cells Reference Manual available in Design Package for more details on library specific information.

2. Functional Specifications

2.1. Cell List

2.1.1. LR(LP Regular Vt)

2.1.1.1. Poly Bias With 0 nm

Table 2: Cell List

Cell Name	Drive Strength	Description
C12T28SOIDV_LRBR0P6_NAND3	X18	Beta ratio optimization 0.6, 3 input NAND, Vdd rail at the bottom of the cell
C12T28SOI_LRBR0D8_NAND2	X7, X14	Beta ratio optimization 0.8, 2 input NAND
C12T28SOI_LRBR0P6_NAND3	X6, X12, X18, X24, X35, X47	Beta ratio optimization 0.6, 3 input NAND
C12T28SOI_LRHF_SDFPHRQ	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LRHF_SDFPHRQN	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only
C12T28SOI_LRHF_SDFPQ	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having non-inverted output Q only
C12T28SOI_LRHF_SDFPQN	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having inverted output QN only
C12T28SOI_LRHF_SDFPQNT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ
C12T28SOI_LRHF_SDFPQT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LRHF_SDFPRQ	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LRHF_SDFPRQN	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only
C12T28SOI_LRHF_SDFPRQNT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ
C12T28SOI_LRHF_SDFPRQT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low

Cell Name	Drive Strength	Description
		asynchronous Reset; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LRHF_SDFPSQ	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only
C12T28SOI_LRHF_SDFPSQN	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only
C12T28SOI_LRHF_SDFPSQNT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ
C12T28SOI_LRHF_SDFPSQT	X4	Design optimized for hold fix, Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LRS1_FA1	X8, X33	Design optimized for speed, Full-adder having 1 bit input operand
C12T28SOI_LRS_NAND2	X40, X54	Design optimized for speed, 2 input NAND
C12T28SOI_LRS_NOR2	X34, X41, X55	Design optimized for speed, 2 input NOR
C12T28SOI_LRS_XNOR2	X6	Design optimized for speed, 2 input Exclusive NOR
C12T28SOI_LRS_XNOR3	X4	Design optimized for speed, 3 input Exclusive NOR
C12T28SOI_LRS_XOR2	X6	Design optimized for speed, 2 input Exclusive OR
C12T28SOI_LRS_XOR3	X4	Design optimized for speed, 3 input Exclusive OR
C12T28SOI_LR_AND2	X8, X16, X25, X33, X42	2 input AND
C12T28SOI_LR_AND3	X8, X17, X25, X33	3 input AND
C12T28SOI_LR_AND4	X4, X6, X20, X27	4 input AND
C12T28SOI_LR_AO112	X8, X17, X33	2 input AND into 3 input OR
C12T28SOI_LR_AO12	X8, X17, X33	2 input AND into 2 input OR
C12T28SOI_LR_AO212	X8, X17, X33	Double 2 input AND into 3 input OR
C12T28SOI_LR_AO22	X8, X17, X33	Double 2 input AND into 2 input OR
C12T28SOI_LR_AO222	X4, X8, X17, X33	Triple 2 input AND into 3 input OR
C12T28SOI_LR_AOI112	X5, X35	2 input AND into 3 input NOR
C12T28SOI_LR_AOI12	X6, X17, X33, X44	2 input AND into 2 input NOR
C12T28SOI_LR_AOI13	X5, X29, X38	3 input AND into 2 input NOR
C12T28SOI_LR_AOI21	X6, X11, X16, X23, X46	2 input AND into 2 input NOR
C12T28SOI_LR_AOI211	X4, X17, X34	2 input AND into 3 input NOR
C12T28SOI_LR_AOI22	X10, X16, X21, X42	Double 2 input AND into 2 input NOR
C12T28SOI_LR_AOI222	X4, X8, X13, X17	Triple 2 input AND into 3 input NOR

Cell Name	Drive Strength	Description
C12T28SOI_LR_BF	X16, X21, X25, X29, X33, X42, X50, X58, X67, X75, X84, X100, X134	Buffer
C12T28SOI_LR_CB4I1	X8, X17, X25, X33	4 input multi stage compound Boolean with non-inverting last stage
C12T28SOI_LR_CBI4I6	X5, X11, X16, X21	4 input multi stage compound Boolean with inverting last stage
C12T28SOI_LR_DFPHQ	X8, X17, X33	Positive edge triggered Non-scan D flip-flop; with active high data enable; having non-inverted output Q only
C12T28SOI_LR_DFPHQN	X8, X17, X33	Positive edge triggered Non-scan D flip-flop; with active high data enable; having inverted output QN only
C12T28SOI_LR_DFPQ	X8, X17, X30, X33	Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only
C12T28SOI_LR_DFPQN	X8, X17, X30, X33	Positive edge triggered Non-scan D flip-flop; having inverted output QN only
C12T28SOI_LR_DFPRQ	X17, X30	Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LR_DFPRQN	X17, X30	Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having inverted output QN only
C12T28SOI_LR_DFPSQ	X17, X30	Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only
C12T28SOI_LR_DFPSQN	X17, X30	Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having inverted output QN only
C12T28SOI_LR_FA1	X8, X33	Full-adder having 1 bit input operand
C12T28SOI_LR_HA1	X8, X33	Half-adder having 1 bit input operand
C12T28SOI_LR_IV	X4, X17, X21, X25, X29, X33, X50, X58, X67, X75, X84, X100, X134	Inverter
C12T28SOI_LR_LDHQ	X8, X23	Active High transparent Latch; having non-inverted output Q only
C12T28SOI_LR_LDHQN	X17	Active High transparent Latch; having inverted output QN only
C12T28SOI_LR_LDLQ	X8, X17, X33	Active Low transparent Latch; having non-inverted output Q only
C12T28SOI_LR_LDLRQ	X8, X33	Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LR_MUX21	X8, X17, X25, X33	2:1 non-inverting Multiplexer with coded selects
C12T28SOI_LR_MUX41	X8, X31	4:1 non-inverting Multiplexer with coded selects
C12T28SOI_LR_MUXI21	X3, X5, X10, X16, X21	2:1 inverting Multiplexer with coded selects

Cell Name	Drive Strength	Description
C12T28SOI_LR_MX41	X7, X27	4:1 non-inverting Multiplexer with individual selects
C12T28SOI_LR_NAND2	X3, X7, X10, X13, X17, X20, X24, X27, X42, X47, X50, X58, X67	2 input NAND
C12T28SOI_LR_NAND2A	X3, X7, X13, X27, X40, X54	2 input NAND with A input inverted
C12T28SOI_LR_NAND3	X6, X9, X12, X15, X18, X21, X24, X35, X47	3 input NAND
C12T28SOI_LR_NAND3A	X6, X12, X18, X24	3 input NAND with A input inverted
C12T28SOI_LR_NAND3AB	X7, X13, X20, X27	3 input NAND with A and B inputs inverted
C12T28SOI_LR_NAND4	X8, X17, X25, X33	4 input NAND
C12T28SOI_LR_NAND4AB	X6, X12, X18, X24	4 input NAND with A and B inputs inverted
C12T28SOI_LR_NOR2	X3, X7, X10, X14, X17, X21, X24, X27, X40, X49, X53, X57, X65, X84	2 input NOR
C12T28SOI_LR_NOR2A	X3, X6, X7, X13, X27, X41, X55	2 input NOR with A input inverted
C12T28SOI_LR_NOR3	X6, X9, X13, X16, X19, X22, X25, X37, X49	3 input NOR
C12T28SOI_LR_NOR3A	X6, X13, X19, X25	3 input NOR with A input inverted
C12T28SOI_LR_NOR4	X8, X17, X25, X32	4 input NOR
C12T28SOI_LR_NOR4AB	X6, X13, X19, X25	4 input NOR with A and B inputs inverted
C12T28SOI_LR_OA112	X8, X17, X25, X33	2 input OR into 3 input AND
C12T28SOI_LR_OA12	X8, X17, X33	2 input OR into 2 input AND
C12T28SOI_LR_OA22	X8, X17, X33	Double 2 input OR into 2 input AND
C12T28SOI_LR_OA222	X8, X17, X33	Triple 2 input OR into 3 input AND
C12T28SOI_LR_OAI112	X5, X10, X21, X31	2 input OR into 3 input NAND
C12T28SOI_LR_OAI12	X6, X17, X34, X46	2 input OR into 2 input NAND
C12T28SOI_LR_OAI21	X5, X11, X17, X23, X46	2 input OR into 2 input NAND
C12T28SOI_LR_OAI211	X5, X10, X15, X21	2 input OR into 3 input NAND
C12T28SOI_LR_OAI22	X5, X10, X15, X21, X42	Double 2 input OR into 2 input NAND
C12T28SOI_LR_OAI222	X3, X9	Triple 2 input OR into 3 input NAND
C12T28SOI_LR_OR2	X8, X16, X33, X50	2 input OR
C12T28SOI_LR_OR2AB	X8, X16, X24, X32	2 input OR with A and B inputs inverted
C12T28SOI_LR_OR4	X20, X27	4 input OR
C12T28SOI_LR_PAO2	X8, X16, X25, X33	2 bit programmable AND/OR logic
C12T28SOI_LR_SDFPHRQ	X8, X17, X33	Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LR_SDFPHRQN	X8, X17, X33	Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Cell Name	Drive Strength	Description
C12T28SOI_LR_SDFPQ	X8, X17, X33	Positive edge triggered Scan D flip-flop; having non-inverted output Q only
C12T28SOI_LR_SDFPQN	X8, X17, X33	Positive edge triggered Scan D flip-flop; having inverted output QN only
C12T28SOI_LR_SDFPQNT	X8, X17, X33	Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ
C12T28SOI_LR_SDFPQT	X8, X17, X33	Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LR_SDFPRQ	X8, X17, X33	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only
C12T28SOI_LR_SDFPRQN	X8, X17, X33	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only
C12T28SOI_LR_SDFPRQNT	X8, X17, X33	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ
C12T28SOI_LR_SDFPRQT	X8, X17, X33	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LR_SDFPRSQNT	X8, X17, X33	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having inverted output QN and non-inverted test output TQ
C12T28SOI_LR_SDFPRSQT	X8, X17, X33	Positive edge triggered Scan D flip-flop; with active low asynchronous Reset over active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LR_SDFPSQ	X8, X17, X25, X33	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only
C12T28SOI_LR_SDFPSQN	X8, X17, X25, X33	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only
C12T28SOI_LR_SDFPSQNT	X8, X17, X33	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ
C12T28SOI_LR_SDFPSQT	X8, X17, X33	Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ
C12T28SOI_LR_XNOR2	X8, X17, X25, X33	2 input Exclusive NOR
C12T28SOI_LR_XNOR3	X8, X16, X25	3 input Exclusive NOR
C12T28SOI_LR_XOR2	X4, X8, X16, X25, X31	2 input Exclusive OR
C12T28SOI_LR_XOR3	X8, X17, X24	3 input Exclusive OR

3. Contact Information

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