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C28SOI_SC_8_COREPBP4_LL Databook

8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 4 nm

Overview

- C28SOI_SC_8_COREPBP4_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 437 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

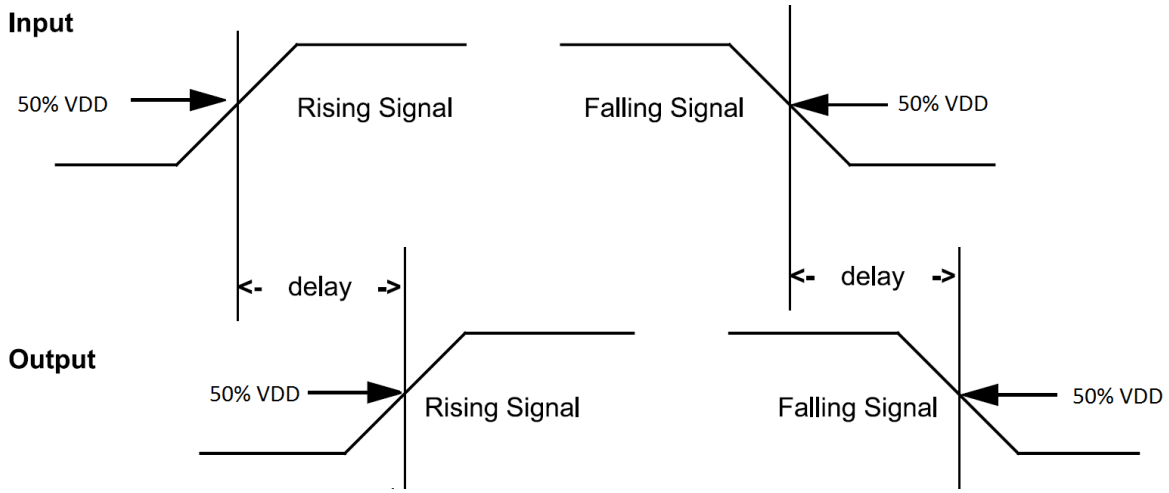


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

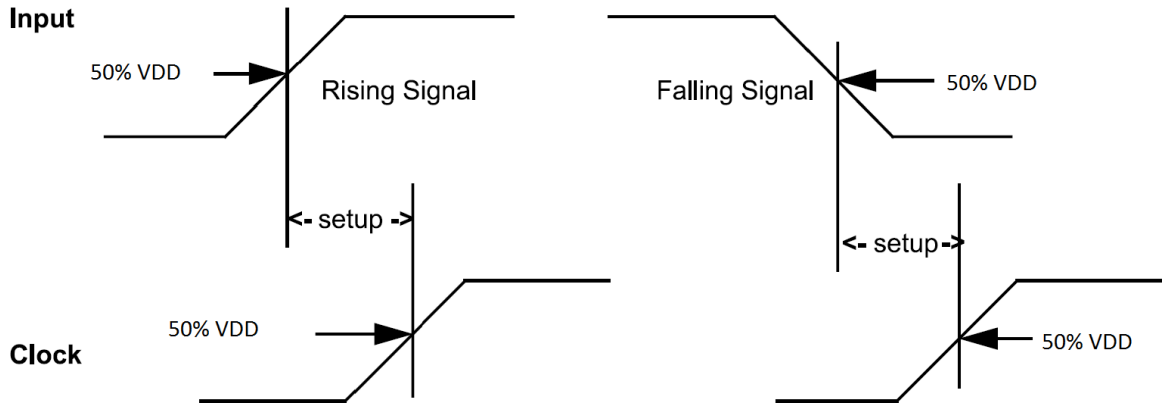


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

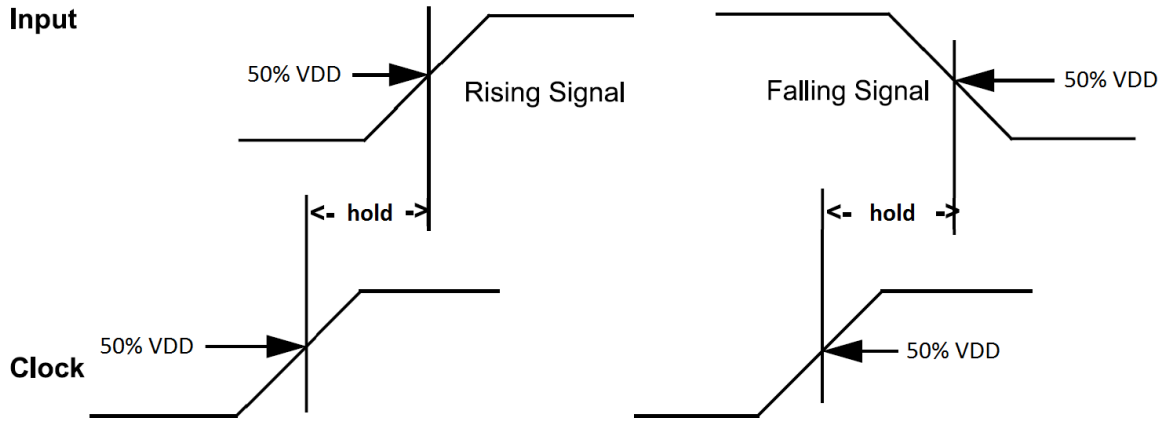


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

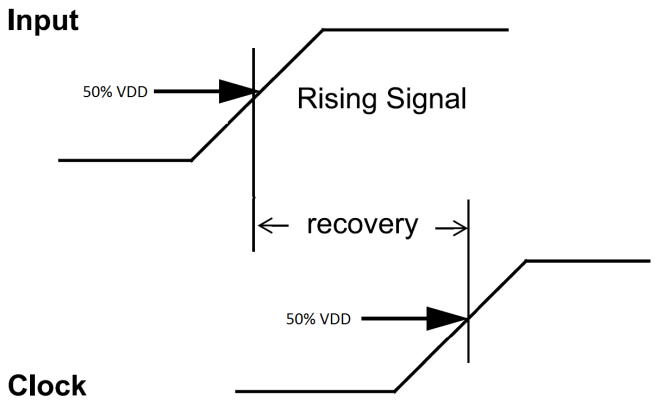


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

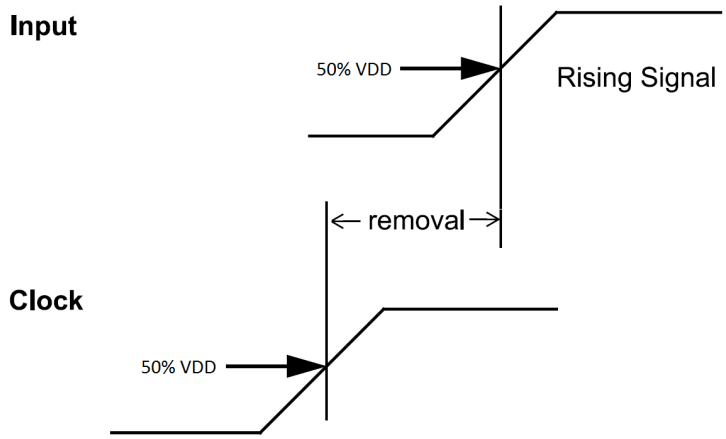


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

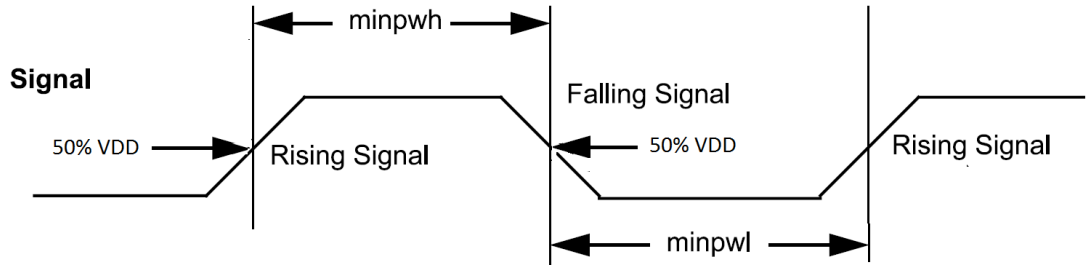


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

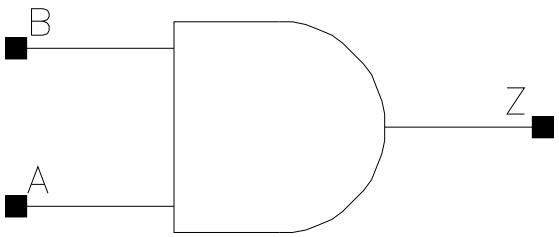
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

AND2

Cell Description

2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.544	0.4352
X10_P4	0.800	0.680	0.5440
X11_P4	1.600	0.544	0.8704
X19_P4	0.800	1.224	0.9792
X24_P4	0.800	1.360	1.0880
X29_P4	0.800	1.496	1.1968

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X11_P4	X19_P4
A	0.0005	0.0007	0.0009	0.0015
B	0.0005	0.0007	0.0009	0.0013
	X24_P4	X29_P4		
A	0.0014	0.0014		
B	0.0013	0.0013		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0212	0.0176	2.7204	1.3014
A to Z ↑	0.0164	0.0162	3.5677	1.7186
B to Z ↓	0.0202	0.0164	2.7174	1.2994
B to Z ↑	0.0183	0.0178	3.5644	1.7163
	X11_P4	**X19_P4**	**X11_P4**	**X19_P4**

A to Z ↓	0.0195	0.0174	1.0407	0.6676
A to Z ↑	0.0146	0.0160	1.6411	0.8645
B to Z ↓	0.0182	0.0166	1.0381	0.6682
B to Z ↑	0.0163	0.0178	1.6366	0.8635
	X24_P4	**X29_P4**	**X24_P4**	**X29_P4**
A to Z ↓	0.0188	0.0201	0.5421	0.4517
A to Z ↑	0.0176	0.0190	0.6937	0.5757
B to Z ↓	0.0182	0.0197	0.5427	0.4523
B to Z ↑	0.0195	0.0211	0.6936	0.5752

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	8.388e-05	1.000e-20
X10_P4	1.945e-04	1.000e-20
X11_P4	2.100e-04	1.000e-20
X19_P4	3.729e-04	1.000e-20
X24_P4	4.355e-04	1.000e-20
X29_P4	4.981e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X11_P4	X19_P4
A (output stable)	9.536e-06	1.796e-05	2.463e-05	3.459e-05
B (output stable)	1.893e-05	3.506e-05	4.937e-05	7.036e-05
A to Z	2.455e-03	4.391e-03	5.114e-03	8.753e-03
B to Z	2.371e-03	4.261e-03	4.893e-03	8.440e-03
	X24_P4	X29_P4		
A (output stable)	3.491e-05	3.409e-05		
B (output stable)	7.086e-05	7.136e-05		
A to Z	1.064e-02	1.266e-02		
B to Z	1.037e-02	1.243e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

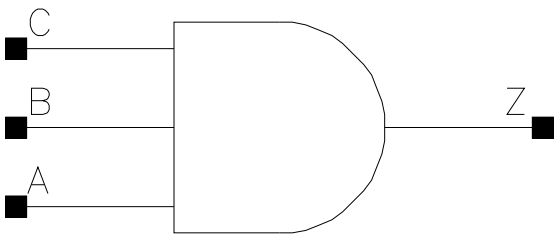
Pin Cycle (vdds)	X5_P4	X10_P4	X11_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P4	X29_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

AND3

Cell Description

3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.680	0.5440
X10_P4	0.800	0.816	0.6528
X14_P4	0.800	1.360	1.0880
X19_P4	0.800	1.496	1.1968

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0005	0.0008	0.0013	0.0015
B	0.0005	0.0007	0.0010	0.0014
C	0.0005	0.0007	0.0010	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0236	0.0195	2.7461	1.3079
A to Z ↑	0.0217	0.0209	3.6067	1.7385
B to Z ↓	0.0228	0.0185	2.7462	1.3073
B to Z ↑	0.0234	0.0223	3.6096	1.7383
C to Z ↓	0.0219	0.0175	2.7430	1.3052
C to Z ↑	0.0249	0.0235	3.6076	1.7386
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0196	0.0188	0.9028	0.6694

A to Z ↑	0.0198	0.0197	1.1803	0.8724
B to Z ↓	0.0186	0.0177	0.9019	0.6697
B to Z ↑	0.0213	0.0212	1.1806	0.8721
C to Z ↓	0.0176	0.0167	0.9003	0.6693
C to Z ↑	0.0226	0.0224	1.1795	0.8713

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	8.393e-05	1.000e-20
X10_P4	1.933e-04	1.000e-20
X14_P4	2.724e-04	1.000e-20
X19_P4	3.739e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.132e-05	2.219e-05	2.953e-05	3.973e-05
B (output stable)	1.741e-05	3.131e-05	4.462e-05	6.068e-05
C (output stable)	3.726e-05	6.696e-05	9.870e-05	1.407e-04
A to Z	2.827e-03	5.009e-03	7.348e-03	9.714e-03
B to Z	2.734e-03	4.850e-03	7.078e-03	9.345e-03
C to Z	2.657e-03	4.704e-03	6.861e-03	9.017e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

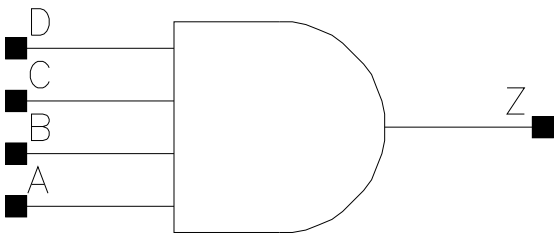
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AND4

Cell Description

4 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.088	0.8704
X3_P4	0.800	1.088	0.8704
X10_P4	0.800	2.176	1.7408
X13_P4	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
-	0	-	-	0
-	-	0	-	0
-	-	-	0	0
0	-	-	-	0
1	1	1	1	1

Pin Capacitance

Pin	X2_P4	X3_P4	X10_P4	X13_P4
A	0.0005	0.0005	0.0011	0.0013
B	0.0005	0.0005	0.0011	0.0013
C	0.0005	0.0005	0.0011	0.0013
D	0.0005	0.0005	0.0011	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	X3_P4	X2_P4	X3_P4
A to Z ↓	0.0186	0.0201	4.8823	3.2922
A to Z ↑	0.0183	0.0185	11.7997	6.5019
B to Z ↓	0.0173	0.0192	4.8780	3.2931
B to Z ↑	0.0199	0.0203	11.8015	6.5020
C to Z ↓	0.0190	0.0207	4.8804	3.2853
C to Z ↑	0.0186	0.0188	11.8094	6.5059

D to Z ↓	0.0179	0.0200	4.8776	3.2838
D to Z ↑	0.0205	0.0213	11.8104	6.5058
	X10_P4	**X13_P4**	**X10_P4**	**X13_P4**
A to Z ↓	0.0193	0.0194	1.1276	0.8415
A to Z ↑	0.0179	0.0198	2.1802	1.6723
B to Z ↓	0.0183	0.0176	1.1282	0.8403
B to Z ↑	0.0195	0.0210	2.1784	1.6719
C to Z ↓	0.0192	0.0186	1.1226	0.8427
C to Z ↑	0.0177	0.0178	2.1759	1.6678
D to Z ↓	0.0174	0.0168	1.1199	0.8415
D to Z ↑	0.0188	0.0190	2.1748	1.6667

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P4	6.413e-05	1.000e-20
X3_P4	8.829e-05	1.000e-20
X10_P4	2.750e-04	1.000e-20
X13_P4	3.783e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P4	X3_P4	X10_P4	X13_P4
A (output stable)	5.371e-04	6.156e-04	1.635e-03	2.166e-03
B (output stable)	5.026e-04	5.756e-04	1.531e-03	2.035e-03
C (output stable)	5.417e-04	5.847e-04	1.522e-03	1.937e-03
D (output stable)	5.050e-04	5.540e-04	1.420e-03	1.806e-03
A to Z	1.889e-03	2.462e-03	6.978e-03	9.381e-03
B to Z	1.798e-03	2.365e-03	6.704e-03	8.883e-03
C to Z	1.929e-03	2.474e-03	6.415e-03	8.211e-03
D to Z	1.835e-03	2.400e-03	6.002e-03	7.717e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

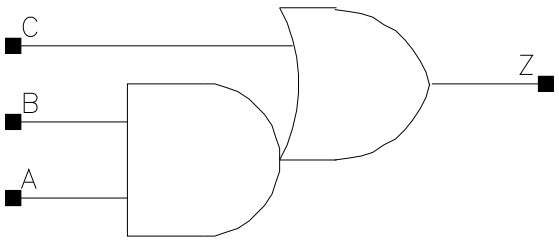
Pin Cycle (vdds)	X2_P4	X3_P4	X10_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	0.952	0.7616
X19_P4	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0005	0.0006	0.0013
B	0.0005	0.0007	0.0012
C	0.0005	0.0007	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0287	0.0260	2.6053	1.3066
A to Z ↑	0.0184	0.0174	3.3135	1.6906
B to Z ↓	0.0269	0.0242	2.5985	1.3021
B to Z ↑	0.0206	0.0195	3.3088	1.6891
C to Z ↓	0.0273	0.0239	2.5962	1.3021
C to Z ↑	0.0181	0.0169	3.2890	1.6789
	X19_P4		**X19_P4**	
A to Z ↓	0.0249		0.6793	
A to Z ↑	0.0193		0.8540	

B to Z ↓	0.0240		0.6790	
B to Z ↑	0.0214		0.8531	
C to Z ↓	0.0233		0.6780	
C to Z ↑	0.0184		0.8465	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	8.213e-05	1.000e-20
X10_P4	1.681e-04	1.000e-20
X19_P4	3.132e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	3.944e-05	5.138e-05	1.154e-04
B (output stable)	4.191e-05	6.044e-05	1.281e-04
C (output stable)	4.734e-05	6.480e-05	1.495e-04
A to Z	2.881e-03	5.027e-03	9.738e-03
B to Z	2.781e-03	4.850e-03	9.538e-03
C to Z	3.025e-03	5.159e-03	1.004e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

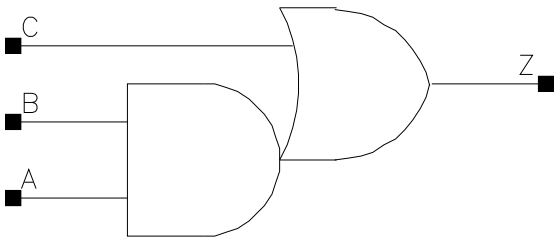
Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

AO21

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	0.952	0.7616
X14_P4	0.800	1.632	1.3056
X19_P4	0.800	1.768	1.4144

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0004	0.0007	0.0013	0.0013
B	0.0005	0.0006	0.0013	0.0013
C	0.0005	0.0007	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0281	0.0250	2.5985	1.3128
A to Z ↑	0.0204	0.0194	3.3862	1.7106
B to Z ↓	0.0268	0.0238	2.5934	1.3118
B to Z ↑	0.0230	0.0215	3.3849	1.7096
C to Z ↓	0.0263	0.0243	2.5850	1.3072
C to Z ↑	0.0155	0.0144	3.3444	1.6925
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0227	0.0247	0.9015	0.6752

A to Z ↑	0.0178	0.0192	1.1639	0.8668
B to Z ↓	0.0205	0.0226	0.8973	0.6734
B to Z ↑	0.0193	0.0210	1.1623	0.8659
C to Z ↓	0.0207	0.0227	0.8958	0.6712
C to Z ↑	0.0124	0.0138	1.1514	0.8560

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	8.257e-05	1.000e-20
X10_P4	1.621e-04	1.000e-20
X14_P4	2.897e-04	1.000e-20
X19_P4	3.328e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.300e-05	1.706e-05	5.561e-05	5.527e-05
B (output stable)	1.713e-05	2.219e-05	9.461e-05	9.451e-05
C (output stable)	1.593e-04	1.811e-04	5.259e-04	5.268e-04
A to Z	3.080e-03	5.076e-03	8.475e-03	1.046e-02
B to Z	2.984e-03	4.934e-03	7.948e-03	9.944e-03
C to Z	2.683e-03	4.512e-03	7.246e-03	9.014e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

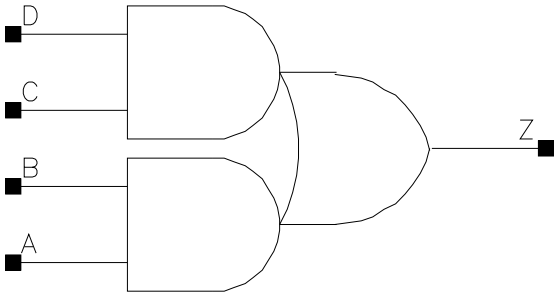
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO22

Cell Description

Double 2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.088	0.8704
X10_P4	0.800	1.088	0.8704
X14_P4	0.800	1.768	1.4144
X19_P4	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	-	0	0
0	-	-	0	0
0	-	0	-	0
-	0	0	-	0
-	-	1	1	1
1	1	-	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0005	0.0007	0.0014	0.0014
B	0.0005	0.0009	0.0012	0.0012
C	0.0005	0.0007	0.0014	0.0014
D	0.0005	0.0007	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0289	0.0251	2.6155	1.3173
A to Z ↑	0.0215	0.0205	3.4163	1.6937
B to Z ↓	0.0265	0.0230	2.6028	1.3128

B to Z ↑	0.0231	0.0223	3.4132	1.6929
C to Z ↓	0.0276	0.0244	2.6042	1.3127
C to Z ↑	0.0181	0.0171	3.4043	1.6868
D to Z ↓	0.0263	0.0231	2.6001	1.3110
D to Z ↑	0.0203	0.0191	3.4039	1.6862
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0226	0.0245	0.9007	0.6782
A to Z ↑	0.0183	0.0197	1.1692	0.8740
B to Z ↓	0.0211	0.0231	0.8998	0.6778
B to Z ↑	0.0202	0.0218	1.1677	0.8734
C to Z ↓	0.0222	0.0242	0.8984	0.6765
C to Z ↑	0.0154	0.0169	1.1646	0.8706
D to Z ↓	0.0209	0.0230	0.8973	0.6756
D to Z ↑	0.0170	0.0186	1.1632	0.8699

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.021e-04	1.000e-20
X10_P4	2.068e-04	1.000e-20
X14_P4	3.459e-04	1.000e-20
X19_P4	3.988e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	3.032e-05	3.939e-05	5.034e-05	5.034e-05
B (output stable)	1.055e-04	1.082e-04	6.869e-05	6.882e-05
C (output stable)	3.932e-05	4.987e-05	1.179e-04	1.182e-04
D (output stable)	4.339e-05	6.205e-05	1.412e-04	1.420e-04
A to Z	3.442e-03	5.600e-03	8.864e-03	1.091e-02
B to Z	3.186e-03	5.229e-03	8.493e-03	1.056e-02
C to Z	3.054e-03	5.007e-03	7.813e-03	9.811e-03
D to Z	2.945e-03	4.851e-03	7.479e-03	9.488e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

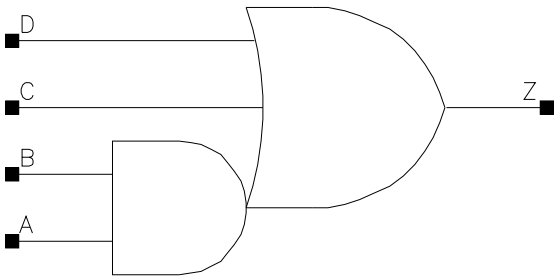
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AO112

Cell Description

2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	1.088	0.8704
X19_P4	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	0	0
0	-	0	0	0
1	1	-	-	1
-	-	-	1	1
-	-	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0005	0.0007	0.0012
B	0.0005	0.0007	0.0012
C	0.0005	0.0006	0.0013
D	0.0005	0.0006	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0354	0.0312	2.8657	1.3558
A to Z ↑	0.0190	0.0168	3.5317	1.7022
B to Z ↓	0.0340	0.0292	2.8612	1.3508
B to Z ↑	0.0212	0.0187	3.5296	1.7015
C to Z ↓	0.0342	0.0294	2.8580	1.3516
C to Z ↑	0.0184	0.0242	3.5017	1.7020

D to Z ↓	0.0351	0.0306	2.8591	1.3525
D to Z ↑	0.0182	0.0237	3.5036	1.7012
	X19_P4		**X19_P4**	
A to Z ↓	0.0309		0.7004	
A to Z ↑	0.0188		0.8464	
B to Z ↓	0.0283		0.6970	
B to Z ↑	0.0202		0.8464	
C to Z ↓	0.0288		0.6980	
C to Z ↑	0.0197		0.8401	
D to Z ↓	0.0295		0.6980	
D to Z ↑	0.0194		0.8398	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	6.234e-05	1.000e-20
X10_P4	1.390e-04	1.000e-20
X19_P4	2.604e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	5.152e-05	9.739e-05	1.623e-04
B (output stable)	5.046e-05	9.672e-05	1.823e-04
C (output stable)	2.318e-05	4.145e-05	8.744e-05
D (output stable)	3.207e-05	5.844e-05	1.103e-04
A to Z	3.046e-03	5.341e-03	1.057e-02
B to Z	2.956e-03	5.140e-03	1.002e-02
C to Z	3.266e-03	5.898e-03	1.128e-02
D to Z	3.150e-03	5.696e-03	1.083e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

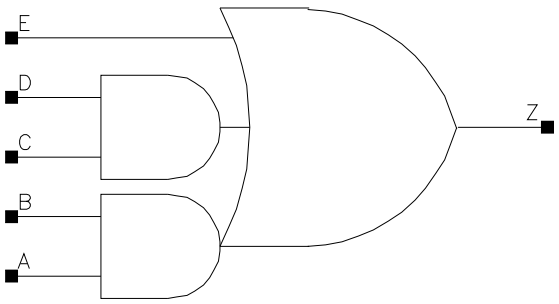
Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AO212

Cell Description

Double 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.088	0.8704
X10_P4	0.800	1.224	0.9792
X19_P4	0.800	2.312	1.8496

Truth Table

A	B	C	D	E	Z
-	0	0	-	0	0
-	0	-	0	0	0
0	-	-	0	0	0
0	-	0	-	0	0
1	1	-	-	-	1
-	-	-	-	1	1
-	-	1	1	-	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0004	0.0007	0.0013
B	0.0005	0.0007	0.0012
C	0.0005	0.0009	0.0013
D	0.0005	0.0007	0.0012
E	0.0005	0.0007	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0408	0.0331	2.7083	1.3513
A to Z ↑	0.0249	0.0217	3.4455	1.7111

B to Z ↓	0.0401	0.0316	2.7005	1.3494
B to Z ↑	0.0280	0.0239	3.4429	1.7091
C to Z ↓	0.0388	0.0323	2.7007	1.3487
C to Z ↑	0.0213	0.0181	3.4212	1.7004
D to Z ↓	0.0366	0.0295	2.6897	1.3421
D to Z ↑	0.0237	0.0198	3.4205	1.6981
E to Z ↓	0.0374	0.0305	2.6884	1.3440
E to Z ↑	0.0198	0.0171	3.3901	1.6877
	X19_P4		**X19_P4**	
A to Z ↓	0.0321		0.6953	
A to Z ↑	0.0225		0.8594	
B to Z ↓	0.0306		0.6944	
B to Z ↑	0.0250		0.8580	
C to Z ↓	0.0305		0.6927	
C to Z ↑	0.0184		0.8528	
D to Z ↓	0.0290		0.6912	
D to Z ↑	0.0205		0.8524	
E to Z ↓	0.0293		0.6916	
E to Z ↑	0.0220		0.8490	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	7.934e-05	1.000e-20
X10_P4	1.717e-04	1.000e-20
X19_P4	3.171e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	1.357e-05	2.307e-05	4.585e-05
B (output stable)	1.862e-05	2.618e-05	4.930e-05
C (output stable)	6.150e-05	7.478e-05	1.616e-04
D (output stable)	6.385e-05	8.877e-05	1.719e-04
E (output stable)	8.157e-05	1.199e-04	2.486e-04
A to Z	4.011e-03	6.435e-03	1.251e-02
B to Z	3.942e-03	6.257e-03	1.216e-02
C to Z	3.483e-03	5.560e-03	1.064e-02
D to Z	3.364e-03	5.326e-03	1.034e-02
E to Z	3.523e-03	5.671e-03	1.111e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

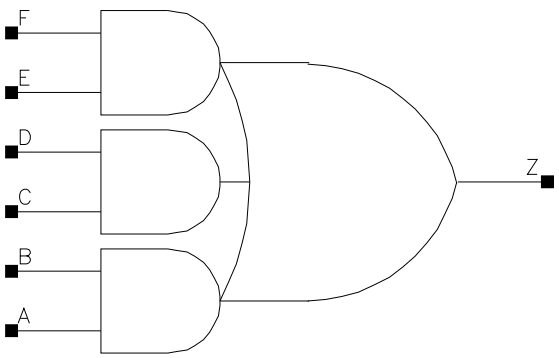
E to Z	0.000e+00	0.000e+00	0.000e+00

AO222

Cell Description

Triple 2 input AND into 3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.360	1.0880
X5_P4	0.800	1.360	1.0880
X10_P4	0.800	1.632	1.3056
X19_P4	0.800	2.584	2.0672

Truth Table

A	B	C	D	E	F	Z
-	0	0	-	-	0	0
0	-	0	-	-	0	0
0	-	-	0	0	-	0
0	-	0	-	0	-	0
-	0	-	0	0	-	0
0	-	-	0	-	0	0
-	0	0	-	0	-	0
-	0	-	0	-	0	0
1	-	-	-	1	1	1
-	-	0	-	1	1	1
-	-	1	1	-	0	1
-	-	-	0	1	1	1
1	1	-	-	-	-	1
0	-	1	1	-	-	1
-	-	1	1	0	-	1

Pin Capacitance

Pin	X2_P4	X5_P4	X10_P4	X19_P4
A	0.0005	0.0005	0.0008	0.0013

B	0.0006	0.0006	0.0008	0.0012
C	0.0007	0.0007	0.0006	0.0012
D	0.0005	0.0005	0.0006	0.0012
E	0.0007	0.0007	0.0007	0.0013
F	0.0006	0.0006	0.0007	0.0012

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	X5_P4	X2_P4	X5_P4
A to Z ↓	0.0316	0.0329	5.0431	2.8020
A to Z ↑	0.0246	0.0246	6.4963	3.6087
B to Z ↓	0.0300	0.0314	5.0265	2.7941
B to Z ↑	0.0274	0.0275	6.4873	3.6044
C to Z ↓	0.0302	0.0316	5.0416	2.8009
C to Z ↑	0.0226	0.0226	6.4372	3.5824
D to Z ↓	0.0276	0.0290	5.0234	2.7924
D to Z ↑	0.0245	0.0247	6.4288	3.5785
E to Z ↓	0.0270	0.0283	5.0162	2.7904
E to Z ↑	0.0183	0.0184	6.3964	3.5642
F to Z ↓	0.0249	0.0264	5.0009	2.7836
F to Z ↑	0.0200	0.0203	6.3943	3.5632
	X10_P4	X19_P4	X10_P4	X19_P4
A to Z ↓	0.0357	0.0334	1.3503	0.6932
A to Z ↑	0.0268	0.0244	1.7215	0.8631
B to Z ↓	0.0337	0.0322	1.3434	0.6923
B to Z ↑	0.0290	0.0270	1.7197	0.8620
C to Z ↓	0.0337	0.0320	1.3466	0.6926
C to Z ↑	0.0238	0.0223	1.7102	0.8577
D to Z ↓	0.0324	0.0309	1.3430	0.6916
D to Z ↑	0.0264	0.0248	1.7095	0.8570
E to Z ↓	0.0315	0.0307	1.3426	0.6906
E to Z ↑	0.0202	0.0193	1.7020	0.8542
F to Z ↓	0.0297	0.0289	1.3377	0.6889
F to Z ↑	0.0223	0.0214	1.7012	0.8539

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P4	9.408e-05	1.000e-20
X5_P4	1.198e-04	1.000e-20
X10_P4	2.001e-04	1.000e-20
X19_P4	3.878e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P4	X5_P4	X10_P4	X19_P4
A (output stable)	2.805e-05	2.814e-05	4.304e-05	6.453e-05
B (output stable)	3.067e-05	3.078e-05	8.024e-05	7.211e-05
C (output stable)	4.510e-05	4.529e-05	4.595e-05	9.543e-05
D (output stable)	5.115e-05	5.135e-05	5.329e-05	1.113e-04
E (output stable)	1.057e-04	1.061e-04	1.345e-04	2.157e-04
F (output stable)	1.152e-04	1.156e-04	1.361e-04	2.291e-04

A to Z	3.492e-03	4.223e-03	7.159e-03	1.331e-02
B to Z	3.355e-03	4.081e-03	6.815e-03	1.297e-02
C to Z	2.991e-03	3.699e-03	6.465e-03	1.208e-02
D to Z	2.841e-03	3.543e-03	6.313e-03	1.181e-02
E to Z	2.500e-03	3.164e-03	5.803e-03	1.104e-02
F to Z	2.371e-03	3.033e-03	5.635e-03	1.070e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

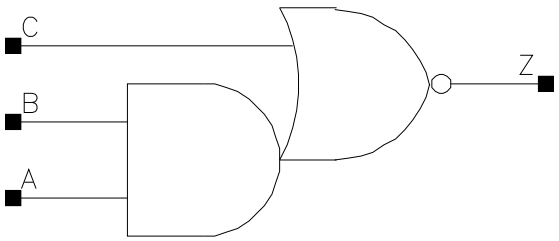
Pin Cycle (vdds)	X2_P4	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI12

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X10_P4	0.800	1.360	1.0880
X19_P4	0.800	2.584	2.0672
X25_P4	0.800	3.400	2.7200

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P4	X10_P4	X19_P4	X25_P4
A	0.0006	0.0016	0.0033	0.0044
B	0.0006	0.0015	0.0030	0.0042
C	0.0006	0.0017	0.0033	0.0044

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X10_P4**	**X3_P4**	**X10_P4**
A to Z ↓	0.0056	0.0059	4.1976	1.5162
A to Z ↑	0.0129	0.0130	6.2859	2.1572
B to Z ↓	0.0066	0.0071	4.2589	1.5383
B to Z ↑	0.0106	0.0103	6.1567	2.1511
C to Z ↓	0.0066	0.0069	2.7368	0.9492
C to Z ↑	0.0113	0.0114	5.7170	1.9835
	X19_P4	**X25_P4**	**X19_P4**	**X25_P4**
A to Z ↓	0.0063	0.0064	0.7757	0.5924

A to Z ↑	0.0134	0.0132	1.1084	0.8245
B to Z ↓	0.0071	0.0072	0.7876	0.6014
B to Z ↑	0.0105	0.0105	1.1072	0.8363
C to Z ↓	0.0086	0.0086	0.5760	0.4398
C to Z ↑	0.0115	0.0113	1.0216	0.7654

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	7.387e-05	1.000e-20
X10_P4	2.003e-04	1.000e-20
X19_P4	3.851e-04	1.000e-20
X25_P4	5.108e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X10_P4	X19_P4	X25_P4
A (output stable)	5.051e-05	1.782e-04	3.573e-04	4.717e-04
B (output stable)	6.405e-05	2.227e-04	4.516e-04	5.848e-04
C (output stable)	6.811e-05	2.155e-04	4.297e-04	5.839e-04
A to Z	1.420e-03	4.269e-03	8.588e-03	1.132e-02
B to Z	1.279e-03	3.630e-03	7.287e-03	9.628e-03
C to Z	1.782e-03	5.226e-03	1.012e-02	1.343e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

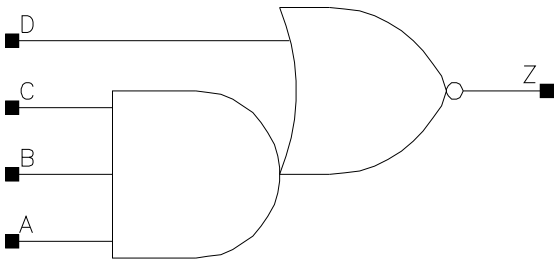
Pin Cycle (vdds)	X3_P4	X10_P4	X19_P4	X25_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

AOI13

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X17_P4	0.800	3.536	2.8288
X22_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X17_P4	X22_P4
A	0.0006	0.0033	0.0045
B	0.0005	0.0031	0.0042
C	0.0007	0.0029	0.0040
D	0.0007	0.0034	0.0044

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X17_P4	X3_P4	X17_P4
A to Z ↓	0.0091	0.0097	5.6960	1.0964
A to Z ↑	0.0162	0.0156	6.2957	1.0642
B to Z ↓	0.0103	0.0107	5.7252	1.1024
B to Z ↑	0.0146	0.0139	6.3098	1.0838
C to Z ↓	0.0116	0.0109	5.7739	1.1092
C to Z ↑	0.0135	0.0113	6.3322	1.0912
D to Z ↓	0.0086	0.0104	2.6796	0.5673

D to Z ↑	0.0144	0.0131	5.4208	0.9268
	X22_P4		**X22_P4**	
A to Z ↓	0.0096		0.8336	
A to Z ↑	0.0153		0.7956	
B to Z ↓	0.0105		0.8386	
B to Z ↑	0.0136		0.8135	
C to Z ↓	0.0109		0.8443	
C to Z ↑	0.0112		0.8219	
D to Z ↓	0.0110		0.4697	
D to Z ↑	0.0126		0.6945	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	7.582e-05	1.000e-20
X17_P4	3.743e-04	1.000e-20
X22_P4	4.880e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X17_P4	X22_P4
A (output stable)	4.182e-05	2.590e-04	3.412e-04
B (output stable)	4.603e-05	2.980e-04	3.904e-04
C (output stable)	5.805e-05	4.680e-04	6.126e-04
D (output stable)	1.047e-04	6.284e-04	8.214e-04
A to Z	1.836e-03	1.038e-02	1.360e-02
B to Z	1.655e-03	9.020e-03	1.179e-02
C to Z	1.507e-03	7.788e-03	1.019e-02
D to Z	2.282e-03	1.213e-02	1.570e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

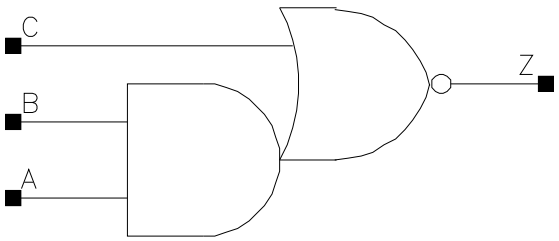
Pin Cycle (vdds)	X3_P4	X17_P4	X22_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI21

Cell Description

2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X6_P4	0.800	1.088	0.8704
X9_P4	0.800	1.360	1.0880
X12_P4	0.800	1.904	1.5232
X25_P4	0.800	3.536	2.8288

Truth Table

A	B	C	Z
-	-	1	0
1	1	-	0
0	-	0	1
-	0	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X9_P4	X12_P4
A	0.0005	0.0012	0.0018	0.0024
B	0.0005	0.0011	0.0017	0.0023
C	0.0006	0.0011	0.0015	0.0021
	X25_P4			
A	0.0048			
B	0.0045			
C	0.0041			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0087	0.0083	5.4230	2.2126
A to Z ↑	0.0122	0.0130	7.1248	3.2058
B to Z ↓	0.0105	0.0093	5.4736	2.2388

B to Z ↑	0.0107	0.0104	7.0127	3.2199
C to Z ↓	0.0052	0.0046	3.5873	1.7083
C to Z ↑	0.0111	0.0104	6.5567	2.9779
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0079	0.0082	1.5168	1.1404
A to Z ↑	0.0122	0.0123	2.1473	1.5865
B to Z ↓	0.0093	0.0092	1.5371	1.1553
B to Z ↑	0.0096	0.0097	2.1501	1.6109
C to Z ↓	0.0046	0.0045	1.1634	0.8697
C to Z ↑	0.0098	0.0099	1.9964	1.4867
	X25_P4		**X25_P4**	
A to Z ↓	0.0081		0.5933	
A to Z ↑	0.0119		0.8073	
B to Z ↓	0.0093		0.6007	
B to Z ↑	0.0093		0.8119	
C to Z ↓	0.0045		0.4415	
C to Z ↑	0.0096		0.7540	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	5.997e-05	1.000e-20
X6_P4	1.412e-04	1.000e-20
X9_P4	2.006e-04	1.000e-20
X12_P4	2.684e-04	1.000e-20
X25_P4	5.233e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.674e-05	5.439e-05	7.116e-05	1.036e-04
B (output stable)	2.115e-05	9.259e-05	1.087e-04	1.718e-04
C (output stable)	1.936e-04	5.111e-04	6.248e-04	8.733e-04
A to Z	1.491e-03	3.561e-03	5.038e-03	6.862e-03
B to Z	1.363e-03	3.105e-03	4.346e-03	5.889e-03
C to Z	1.192e-03	2.649e-03	3.750e-03	5.132e-03
	X25_P4			
A (output stable)	1.982e-04			
B (output stable)	3.044e-04			
C (output stable)	1.622e-03			
A to Z	1.323e-02			
B to Z	1.144e-02			
C to Z	9.876e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

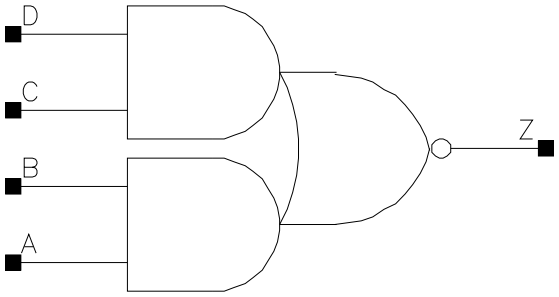
	X25_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

AOI22

Cell Description

Double 2 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.680	0.5440
X6_P4	0.800	1.224	0.9792
X9_P4	0.800	1.768	1.4144
X12_P4	0.800	2.448	1.9584
X24_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
-	-	1	1	0
1	1	-	-	0
-	0	-	0	1
0	-	0	-	1
-	0	0	-	1
0	-	-	0	1

Pin Capacitance

Pin	X2_P4	X6_P4	X9_P4	X12_P4
A	0.0005	0.0012	0.0018	0.0024
B	0.0005	0.0011	0.0017	0.0024
C	0.0005	0.0013	0.0017	0.0022
D	0.0004	0.0010	0.0016	0.0021
	X24_P4			
A	0.0047			
B	0.0046			
C	0.0045			
D	0.0043			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X6_P4**	**X2_P4**	**X6_P4**
A to Z ↓	0.0085	0.0092	5.5250	2.1161
A to Z ↑	0.0157	0.0135	8.7996	2.9249
B to Z ↓	0.0102	0.0108	5.5966	2.1402
B to Z ↑	0.0138	0.0118	8.7743	2.9964
C to Z ↓	0.0055	0.0058	5.5536	2.1297
C to Z ↑	0.0143	0.0125	8.7951	2.9233
D to Z ↓	0.0067	0.0070	5.6447	2.1613
D to Z ↑	0.0122	0.0109	8.7604	3.0244
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0099	0.0103	1.5156	1.1435
A to Z ↑	0.0142	0.0145	1.9659	1.4784
B to Z ↓	0.0117	0.0118	1.5336	1.1564
B to Z ↑	0.0121	0.0122	1.9700	1.4608
C to Z ↓	0.0064	0.0068	1.5158	1.1482
C to Z ↑	0.0131	0.0134	1.9670	1.4677
D to Z ↓	0.0077	0.0077	1.5390	1.1652
D to Z ↑	0.0107	0.0108	1.9668	1.4744
	X24_P4		**X24_P4**	
A to Z ↓	0.0104		0.5903	
A to Z ↑	0.0143		0.7478	
B to Z ↓	0.0120		0.5972	
B to Z ↑	0.0120		0.7420	
C to Z ↓	0.0069		0.5784	
C to Z ↑	0.0135		0.7455	
D to Z ↓	0.0078		0.5878	
D to Z ↑	0.0109		0.7490	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P4	5.098e-05	1.000e-20
X6_P4	1.679e-04	1.000e-20
X9_P4	2.381e-04	1.000e-20
X12_P4	3.168e-04	1.000e-20
X24_P4	6.174e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.958e-05	4.962e-05	9.444e-05	1.391e-04
B (output stable)	2.465e-05	6.852e-05	1.721e-04	2.717e-04
C (output stable)	5.156e-05	1.143e-04	2.027e-04	2.905e-04
D (output stable)	6.082e-05	1.409e-04	2.719e-04	4.034e-04
A to Z	1.462e-03	3.964e-03	6.081e-03	8.252e-03
B to Z	1.319e-03	3.575e-03	5.392e-03	7.357e-03
C to Z	1.081e-03	3.008e-03	4.613e-03	6.292e-03
D to Z	9.571e-04	2.652e-03	3.986e-03	5.417e-03
	X24_P4			
A (output stable)	2.593e-04			
B (output stable)	4.585e-04			
C (output stable)	5.503e-04			
D (output stable)	7.924e-04			

A to Z	1.612e-02			
B to Z	1.437e-02			
C to Z	1.237e-02			
D to Z	1.067e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

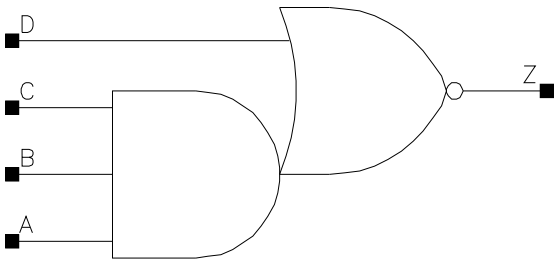
Pin Cycle (vdds)	X2_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

AOI31

Cell Description

3 input AND into 2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X12_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
1	1	1	-	0
-	-	-	1	0
0	-	-	0	1
-	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X12_P4
A	0.0006	0.0023
B	0.0006	0.0022
C	0.0008	0.0021
D	0.0006	0.0023

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X12_P4	X3_P4	X12_P4
A to Z ↓	0.0111	0.0114	5.6976	1.6247
A to Z ↑	0.0154	0.0146	6.1430	1.6141
B to Z ↓	0.0126	0.0123	5.7222	1.6310
B to Z ↑	0.0142	0.0128	6.2416	1.6151
C to Z ↓	0.0145	0.0130	5.7672	1.6392
C to Z ↑	0.0134	0.0104	6.2938	1.6280
D to Z ↓	0.0047	0.0040	2.7428	0.7402
D to Z ↑	0.0121	0.0105	5.3758	1.3948

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	7.776e-05	1.000e-20
X12_P4	2.682e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X12_P4
A (output stable)	1.494e-05	8.102e-05
B (output stable)	1.930e-05	1.121e-04
C (output stable)	3.805e-05	2.094e-04
D (output stable)	3.750e-04	1.262e-03
A to Z	2.149e-03	7.903e-03
B to Z	1.970e-03	6.941e-03
C to Z	1.828e-03	6.095e-03
D to Z	1.610e-03	5.623e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

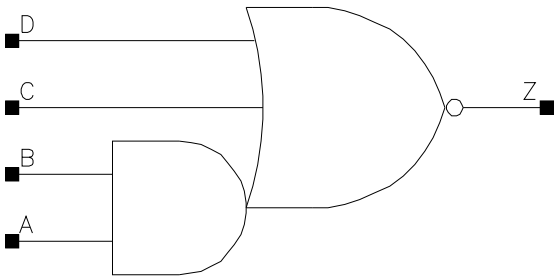
Pin Cycle (vdds)	X3_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI112

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X20_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X3_P4	X20_P4
A	0.0005	0.0043
B	0.0005	0.0040
C	0.0006	0.0042
D	0.0006	0.0039

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X20_P4	X3_P4	X20_P4
A to Z ↓	0.0066	0.0076	4.1272	0.6706
A to Z ↑	0.0173	0.0160	8.9008	1.1637
B to Z ↓	0.0079	0.0087	4.1905	0.6817
B to Z ↑	0.0153	0.0130	8.9972	1.1648
C to Z ↓	0.0081	0.0126	2.7199	0.5615
C to Z ↑	0.0169	0.0153	8.4884	1.1023
D to Z ↓	0.0076	0.0113	2.7251	0.5616

D to Z ↑	0.0179	0.0151	8.5158	1.1068

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	6.502e-05	1.000e-20
X20_P4	4.149e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X20_P4
A (output stable)	9.623e-05	6.607e-04
B (output stable)	1.035e-04	7.058e-04
C (output stable)	4.178e-05	4.287e-04
D (output stable)	5.822e-05	6.334e-04
A to Z	1.607e-03	1.109e-02
B to Z	1.449e-03	9.514e-03
C to Z	2.185e-03	1.533e-02
D to Z	1.970e-03	1.294e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

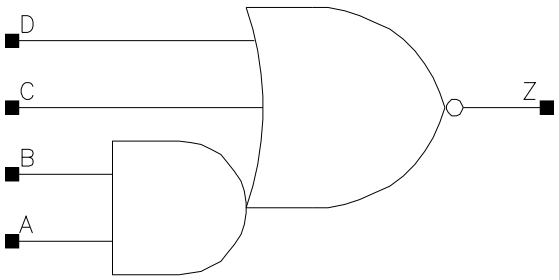
Pin Cycle (vdds)	X3_P4	X20_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00

AOI211

Cell Description

2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.816	0.6528
X10_P4	0.800	2.448	1.9584
X19_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	1	-	-	0
-	-	-	1	0
-	-	1	-	0
-	0	0	0	1
0	-	0	0	1

Pin Capacitance

Pin	X2_P4	X10_P4	X19_P4
A	0.0006	0.0022	0.0045
B	0.0006	0.0021	0.0043
C	0.0007	0.0019	0.0038
D	0.0005	0.0018	0.0035

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	X10_P4	X2_P4	X10_P4
A to Z ↓	0.0097	0.0099	4.8569	1.2933
A to Z ↑	0.0176	0.0161	9.4375	2.3233
B to Z ↓	0.0115	0.0112	4.9173	1.3080
B to Z ↑	0.0156	0.0133	9.4776	2.3319
C to Z ↓	0.0094	0.0087	4.4696	1.1196
C to Z ↑	0.0142	0.0124	8.9886	2.2099

D to Z ↓	0.0076	0.0062	4.5107	1.1328
D to Z ↑	0.0141	0.0119	9.0006	2.2155
	X19_P4		**X19_P4**	
A to Z ↓	0.0096		0.6642	
A to Z ↑	0.0156		1.1827	
B to Z ↓	0.0112		0.6723	
B to Z ↑	0.0129		1.1831	
C to Z ↓	0.0093		0.6056	
C to Z ↑	0.0118		1.1244	
D to Z ↓	0.0067		0.6129	
D to Z ↑	0.0113		1.1277	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P4	5.590e-05	1.000e-20
X10_P4	2.301e-04	1.000e-20
X19_P4	4.523e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P4	X10_P4	X19_P4
A (output stable)	1.973e-05	8.347e-05	1.640e-04
B (output stable)	2.026e-05	1.140e-04	2.121e-04
C (output stable)	5.629e-05	2.609e-04	5.199e-04
D (output stable)	1.248e-04	6.196e-04	1.182e-03
A to Z	1.996e-03	7.565e-03	1.465e-02
B to Z	1.832e-03	6.666e-03	1.296e-02
C to Z	1.436e-03	5.559e-03	1.052e-02
D to Z	1.263e-03	4.583e-03	8.590e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

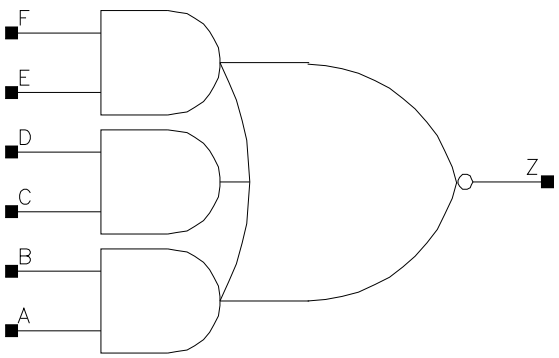
Pin Cycle (vdds)	X2_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00

AOI222

Cell Description

Triple 2 input AND into 3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.088	0.8704
X5_P4	0.800	2.040	1.6320
X7_P4	0.800	2.720	2.1760
X9_P4	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	-	0	-	1	1	0
1	-	-	-	1	1	0
-	-	-	0	1	1	0
0	-	1	1	-	-	0
-	-	1	1	-	0	0
1	1	-	-	-	-	0
-	-	1	1	0	-	0
0	-	0	-	0	-	1
0	-	0	-	-	0	1
0	-	-	0	0	-	1
0	-	-	0	-	0	1
-	0	0	-	0	-	1
-	0	-	0	0	-	1
-	0	0	-	-	0	1
-	0	-	0	-	0	1

Pin Capacitance

Pin	X2_P4	X5_P4	X7_P4	X9_P4
A	0.0006	0.0010	0.0017	0.0023

B	0.0006	0.0012	0.0015	0.0021
C	0.0006	0.0010	0.0016	0.0024
D	0.0005	0.0011	0.0015	0.0020
E	0.0007	0.0011	0.0015	0.0020
F	0.0005	0.0009	0.0014	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X5_P4**	**X2_P4**	**X5_P4**
A to Z ↓	0.0109	0.0137	4.3503	2.4553
A to Z ↑	0.0229	0.0215	9.1618	4.2086
B to Z ↓	0.0128	0.0158	4.4082	2.4752
B to Z ↑	0.0208	0.0199	9.2054	4.1721
C to Z ↓	0.0098	0.0121	4.3734	2.4453
C to Z ↑	0.0209	0.0200	9.2288	4.2209
D to Z ↓	0.0116	0.0140	4.4459	2.4711
D to Z ↑	0.0188	0.0185	9.2140	4.1982
E to Z ↓	0.0071	0.0088	4.4096	2.4058
E to Z ↑	0.0185	0.0180	9.1930	4.1791
F to Z ↓	0.0082	0.0102	4.4954	2.4364
F to Z ↑	0.0158	0.0159	9.1565	4.2005
	X7_P4	**X9_P4**	**X7_P4**	**X9_P4**
A to Z ↓	0.0134	0.0139	1.7047	1.2986
A to Z ↑	0.0207	0.0212	2.7522	2.0772
B to Z ↓	0.0155	0.0157	1.7201	1.3095
B to Z ↑	0.0188	0.0190	2.8210	2.1140
C to Z ↓	0.0119	0.0126	1.7078	1.2911
C to Z ↑	0.0195	0.0204	2.8139	2.1162
D to Z ↓	0.0138	0.0137	1.7280	1.3050
D to Z ↑	0.0171	0.0173	2.7879	2.0969
E to Z ↓	0.0083	0.0083	1.7095	1.2961
E to Z ↑	0.0170	0.0171	2.7752	2.0986
F to Z ↓	0.0098	0.0094	1.7358	1.3158
F to Z ↑	0.0147	0.0144	2.8041	2.0950

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P4	8.821e-05	1.000e-20
X5_P4	1.912e-04	1.000e-20
X7_P4	2.808e-04	1.000e-20
X9_P4	3.560e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P4	X5_P4	X7_P4	X9_P4
A (output stable)	3.260e-05	6.209e-05	1.070e-04	1.489e-04
B (output stable)	3.657e-05	7.799e-05	1.464e-04	2.314e-04
C (output stable)	5.748e-05	1.088e-04	1.576e-04	2.249e-04
D (output stable)	6.437e-05	1.238e-04	2.066e-04	2.942e-04
E (output stable)	1.102e-04	2.380e-04	3.531e-04	5.139e-04
F (output stable)	1.327e-04	2.520e-04	3.967e-04	5.880e-04

A to Z	2.593e-03	5.326e-03	7.767e-03	1.052e-02
B to Z	2.404e-03	5.064e-03	7.131e-03	9.606e-03
C to Z	2.062e-03	4.338e-03	6.298e-03	8.475e-03
D to Z	1.887e-03	4.086e-03	5.717e-03	7.683e-03
E to Z	1.570e-03	3.475e-03	4.893e-03	6.457e-03
F to Z	1.411e-03	3.168e-03	4.335e-03	5.672e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

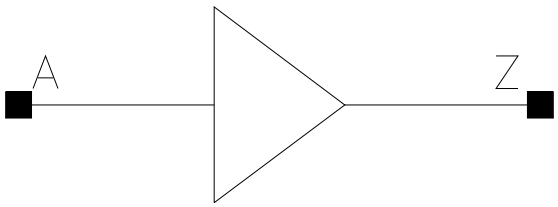
Pin Cycle (vdds)	X2_P4	X5_P4	X7_P4	X9_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

BF

Cell Description

Buffer

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.544	0.4352
X5_P4	0.800	0.544	0.4352
X9_P4	0.800	0.680	0.5440
X11_P4	1.600	0.408	0.6528
X13_P4	0.800	0.680	0.5440
X19_P4	0.800	0.952	0.7616
X23_P4	1.600	0.544	0.8704
X24_P4	0.800	1.088	0.8704
X29_P4	0.800	1.224	0.9792
X34_P4	1.600	0.680	1.0880
X38_P4	0.800	1.632	1.3056
X46_P4	1.600	0.952	1.5232
X57_P4	0.800	2.312	1.8496
X68_P4	1.600	1.224	1.9584
X91_P4	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	X2_P4	X5_P4	X9_P4	X11_P4
A	0.0006	0.0006	0.0006	0.0008
	X13_P4	X19_P4	X23_P4	X24_P4
A	0.0008	0.0010	0.0012	0.0012
	X29_P4	X34_P4	X38_P4	X46_P4
A	0.0014	0.0016	0.0021	0.0020
	X57_P4	X68_P4	X91_P4	
A	0.0027	0.0028	0.0038	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X5_P4**	**X2_P4**	**X5_P4**
A to Z ↓	0.0173	0.0180	4.8414	2.6920
A to Z ↑	0.0132	0.0135	6.3306	3.4888
	X9_P4	**X11_P4**	**X9_P4**	**X11_P4**
A to Z ↓	0.0216	0.0205	1.3729	1.0450
A to Z ↑	0.0168	0.0148	1.7358	1.6346
	X13_P4	**X19_P4**	**X13_P4**	**X19_P4**
A to Z ↓	0.0194	0.0193	0.9408	0.6650
A to Z ↑	0.0161	0.0147	1.2120	0.8499
	X23_P4	**X24_P4**	**X23_P4**	**X24_P4**
A to Z ↓	0.0196	0.0192	0.5046	0.5424
A to Z ↑	0.0146	0.0154	0.8260	0.6813
	X29_P4	**X34_P4**	**X29_P4**	**X34_P4**
A to Z ↓	0.0186	0.0196	0.4490	0.3466
A to Z ↑	0.0152	0.0149	0.5730	0.5659
	X38_P4	**X46_P4**	**X38_P4**	**X46_P4**
A to Z ↓	0.0182	0.0190	0.3397	0.2602
A to Z ↑	0.0150	0.0142	0.4216	0.4249
	X57_P4	**X68_P4**	**X57_P4**	**X68_P4**
A to Z ↓	0.0191	0.0188	0.2284	0.1762
A to Z ↑	0.0158	0.0144	0.2828	0.2843
	X91_P4		**X91_P4**	
A to Z ↓	0.0199		0.1357	
A to Z ↑	0.0151		0.2139	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P4	4.803e-05	1.000e-20
X5_P4	7.881e-05	1.000e-20
X9_P4	1.357e-04	1.000e-20
X11_P4	1.645e-04	1.000e-20
X13_P4	2.109e-04	1.000e-20
X19_P4	2.723e-04	1.000e-20
X23_P4	3.234e-04	1.000e-20
X24_P4	3.435e-04	1.000e-20
X29_P4	4.169e-04	1.000e-20
X34_P4	4.664e-04	1.000e-20
X38_P4	5.652e-04	1.000e-20
X46_P4	6.043e-04	1.000e-20
X57_P4	8.126e-04	1.000e-20
X68_P4	8.990e-04	1.000e-20
X91_P4	1.154e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P4	X5_P4	X9_P4	X11_P4
A to Z	1.768e-03	2.311e-03	3.923e-03	4.540e-03
	X13_P4	X19_P4	X23_P4	X24_P4
A to Z	5.696e-03	7.805e-03	8.641e-03	9.689e-03
	X29_P4	X34_P4	X38_P4	X46_P4

A to Z	1.142e-02	1.283e-02	1.556e-02	1.662e-02
	X57_P4	X68_P4	X91_P4	
A to Z	2.326e-02	2.450e-02	3.285e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

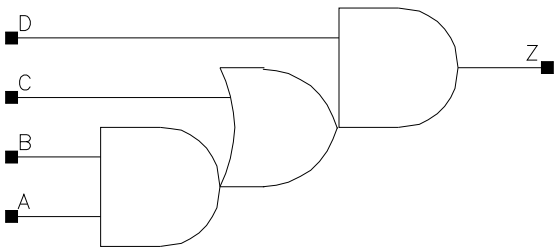
Pin Cycle (vdds)	X2_P4	X5_P4	X9_P4	X11_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X13_P4	X19_P4	X23_P4	X24_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X29_P4	X34_P4	X38_P4	X46_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X57_P4	X68_P4	X91_P4	
A to Z	0.000e+00	0.000e+00	0.000e+00	

CB4I1

Cell Description

4 input multi stage compound Boolean with non-inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.952	0.7616
X10_P4	0.800	1.632	1.3056
X14_P4	0.800	1.768	1.4144
X19_P4	0.800	1.904	1.5232

Truth Table

A	B	C	D	Z
-	0	0	-	0
0	-	0	-	0
-	-	-	0	0
1	1	-	1	1
-	-	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0006	0.0014	0.0014	0.0014
B	0.0007	0.0013	0.0013	0.0013
C	0.0007	0.0015	0.0015	0.0015
D	0.0010	0.0013	0.0014	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0219	0.0199	2.7452	1.2953
A to Z ↑	0.0225	0.0207	3.5865	1.7098
B to Z ↓	0.0203	0.0184	2.7383	1.2944
B to Z ↑	0.0238	0.0217	3.5826	1.7082
C to Z ↓	0.0203	0.0185	2.7317	1.2921
C to Z ↑	0.0171	0.0155	3.5460	1.6920

D to Z ↓	0.0197	0.0171	2.7143	1.2830
D to Z ↑	0.0187	0.0160	3.5582	1.6965
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0224	0.0244	0.9016	0.6753
A to Z ↑	0.0232	0.0252	1.1467	0.8614
B to Z ↓	0.0210	0.0230	0.8999	0.6750
B to Z ↑	0.0243	0.0264	1.1463	0.8591
C to Z ↓	0.0209	0.0230	0.8977	0.6719
C to Z ↑	0.0175	0.0192	1.1327	0.8487
D to Z ↓	0.0187	0.0199	0.8884	0.6644
D to Z ↑	0.0179	0.0194	1.1359	0.8512

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.322e-04	1.000e-20
X10_P4	2.684e-04	1.000e-20
X14_P4	3.277e-04	1.000e-20
X19_P4	3.871e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	4.434e-05	8.408e-05	8.493e-05	8.546e-05
B (output stable)	5.659e-05	1.058e-04	1.073e-04	1.078e-04
C (output stable)	1.795e-04	2.953e-04	2.969e-04	2.980e-04
D (output stable)	7.981e-05	1.254e-04	1.273e-04	1.275e-04
A to Z	3.561e-03	6.668e-03	8.783e-03	1.102e-02
B to Z	3.388e-03	6.274e-03	8.388e-03	1.063e-02
C to Z	3.046e-03	5.574e-03	7.463e-03	9.451e-03
D to Z	3.625e-03	6.681e-03	8.452e-03	1.027e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

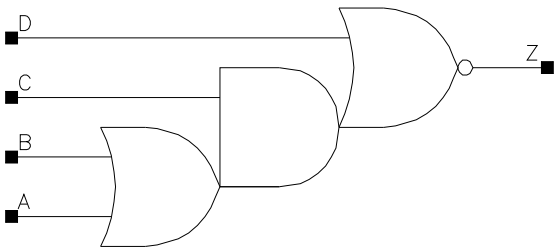
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CBI4I6

Cell Description

4 input multi stage compound Boolean with inverting last stage

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X6_P4	0.800	1.496	1.1968
X9_P4	0.800	1.768	1.4144
X12_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	-	1	0
1	-	1	-	0
-	1	1	-	0
0	0	-	0	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X9_P4	X12_P4
A	0.0006	0.0012	0.0018	0.0023
B	0.0006	0.0011	0.0017	0.0023
C	0.0006	0.0011	0.0017	0.0022
D	0.0008	0.0011	0.0016	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0098	0.0087	4.2865	2.1963
A to Z ↑	0.0183	0.0180	8.9288	4.7504
B to Z ↓	0.0091	0.0086	4.1601	2.2074
B to Z ↑	0.0191	0.0184	8.9466	4.7610
C to Z ↓	0.0097	0.0091	3.9914	2.0751
C to Z ↑	0.0119	0.0111	6.3024	3.2758

D to Z ↓	0.0046	0.0033	2.7670	1.4084
D to Z ↑	0.0134	0.0119	6.6549	3.4777
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0089	0.0094	1.5002	1.1718
A to Z ↑	0.0166	0.0175	3.0475	2.3580
B to Z ↓	0.0083	0.0086	1.5155	1.1726
B to Z ↑	0.0173	0.0178	3.0536	2.3629
C to Z ↓	0.0093	0.0095	1.4295	1.1061
C to Z ↑	0.0105	0.0107	2.1270	1.6200
D to Z ↓	0.0036	0.0036	0.9744	0.7458
D to Z ↑	0.0110	0.0109	2.2481	1.7204

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	7.743e-05	1.000e-20
X6_P4	1.483e-04	1.000e-20
X9_P4	2.116e-04	1.000e-20
X12_P4	2.773e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.657e-05	3.996e-05	4.959e-05	8.265e-05
B (output stable)	2.100e-05	4.923e-05	6.610e-05	1.145e-04
C (output stable)	6.103e-05	1.355e-04	1.836e-04	2.512e-04
D (output stable)	2.165e-04	5.651e-04	7.791e-04	1.179e-03
A to Z	2.163e-03	4.129e-03	5.842e-03	7.958e-03
B to Z	1.943e-03	3.554e-03	5.192e-03	6.896e-03
C to Z	1.760e-03	3.278e-03	4.724e-03	6.381e-03
D to Z	1.491e-03	2.702e-03	3.883e-03	5.096e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

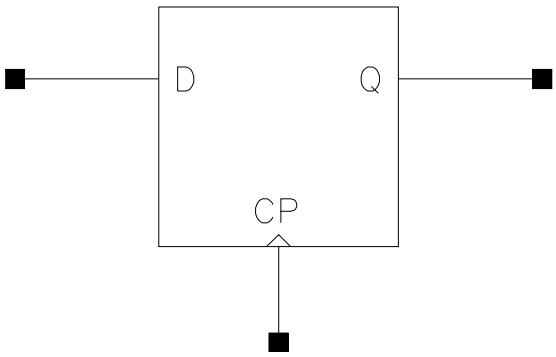
Pin Cycle (vdds)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DFPQ

Cell Description

Positive edge triggered Non-scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	1.600	1.496	2.3936
X19_P4	1.600	1.768	2.8288

Truth Table

IQ	Q
IQ	IQ

D	CP	IQ	IQ
D	/	-	D
-	-	IQ	IQ

Pin Capacitance

Pin	X10_P4	X19_P4
CP	0.0009	0.0009
D	0.0007	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P4	X19_P4	X10_P4	X19_P4
CP to Q ↓	0.0348	0.0469	1.3299	0.7085
CP to Q ↑	0.0409	0.0476	1.6803	0.8607

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P4	X19_P4
CP ↓	min_pulse_width to CP	0.0340	0.0340
CP ↑	min_pulse_width to CP	0.0284	0.0412
D ↓	hold_rising to CP	0.0173	0.0173
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0154	0.0150
D ↑	setup_rising to CP	0.0119	0.0119

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P4	3.608e-04	1.000e-20
X19_P4	4.607e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

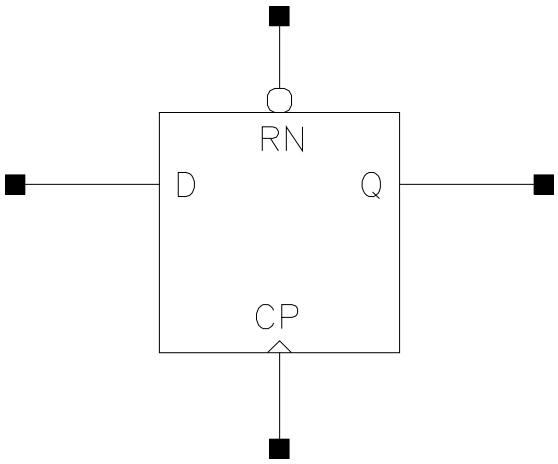
Pin Cycle	X10_P4	X19_P4
Clock 100Mhz Data 0Mhz	1.053e-02	1.053e-02
Clock 100Mhz Data 25Mhz	1.321e-02	1.688e-02
Clock 100Mhz Data 50Mhz	1.588e-02	2.323e-02
Clock = 0 Data 100Mhz	4.371e-03	4.371e-03
Clock = 1 Data 100Mhz	2.289e-05	2.343e-05

DFPRQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	1.600	1.768	2.8288
X19_P4	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	IQ	IQ
-	-	0	-	0
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P4	X19_P4
CP	0.0009	0.0009
D	0.0007	0.0007
RN	0.0009	0.0008

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P4	X19_P4	X10_P4	X19_P4
CP to Q ↓	0.0375	0.0482	1.3474	0.7031
CP to Q ↑	0.0426	0.0490	1.6756	0.8538
RN to Q ↓	0.0367	0.0419	1.2949	0.6654

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P4	X19_P4
CP ↓	min_pulse_width to CP	0.0339	0.0339
CP ↑	min_pulse_width to CP	0.0318	0.0412
D ↓	hold_rising to CP	0.0200	0.0200
D ↑	hold_rising to CP	0.0129	0.0129
D ↓	setup_rising to CP	0.0095	0.0095
D ↑	setup_rising to CP	0.0146	0.0146
RN ↓	min_pulse_width to RN	0.0469	0.0615
RN ↑	recovery_rising to CP	0.0054	0.0081
RN ↑	removal_rising to CP	-0.0007	-0.0007

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P4	4.296e-04	1.000e-20
X19_P4	5.644e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

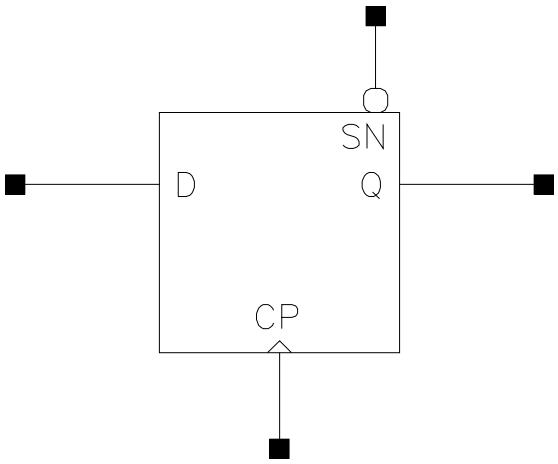
Pin Cycle	X10_P4	X19_P4
Clock 100Mhz Data 0Mhz	1.065e-02	1.065e-02
Clock 100Mhz Data 25Mhz	1.354e-02	1.718e-02
Clock 100Mhz Data 50Mhz	1.643e-02	2.370e-02
Clock = 0 Data 100Mhz	4.386e-03	4.387e-03
Clock = 1 Data 100Mhz	2.389e-05	2.380e-05

DFPSQ

Cell Description

Positive edge triggered Non-scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	1.600	1.768	2.8288
X19_P4	1.600	1.904	3.0464

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	IQ	IQ
-	-	0	-	1
D	/	1	-	D
-	-	1	IQ	IQ

Pin Capacitance

Pin	X10_P4	X19_P4
CP	0.0009	0.0009
D	0.0007	0.0007
SN	0.0011	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P4	X19_P4	X10_P4	X19_P4
CP to Q ↓	0.0355	0.0472	1.3371	0.6978
CP to Q ↑	0.0421	0.0490	1.6714	0.8559
SN to Q ↑	0.0265	0.0285	1.6399	0.8314

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P4	X19_P4
CP ↓	min_pulse_width to CP	0.0340	0.0340
CP ↑	min_pulse_width to CP	0.0318	0.0412
D ↓	hold_rising to CP	0.0173	0.0173
D ↑	hold_rising to CP	0.0124	0.0124
D ↓	setup_rising to CP	0.0150	0.0150
D ↑	setup_rising to CP	0.0119	0.0119
SN ↓	min_pulse_width to SN	0.0305	0.0332
SN ↑	recovery_rising to CP	-0.0043	-0.0017
SN ↑	removal_rising to CP	0.0242	0.0242

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P4	4.108e-04	1.000e-20
X19_P4	5.074e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

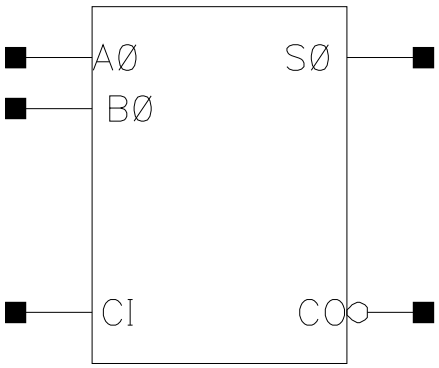
Pin Cycle	X10_P4	X19_P4
Clock 100Mhz Data 0Mhz	1.048e-02	1.049e-02
Clock 100Mhz Data 25Mhz	1.329e-02	1.703e-02
Clock 100Mhz Data 50Mhz	1.609e-02	2.357e-02
Clock = 0 Data 100Mhz	4.248e-03	4.248e-03
Clock = 1 Data 100Mhz	2.339e-05	2.359e-05

FA1

Cell Description

Full-adder having 1 bit input operand

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_FA1X5_-P4	1.600	1.360	2.1760
C8T28SOIDV_LL_FA1X9_-P4	1.600	1.496	2.3936
C8T28SOIDV_LL_FA1X14_-P4	1.600	2.584	4.1344
C8T28SOIDV_LL_FA1X19_-P4	1.600	2.720	4.3520
C8T28SOIDV_LLS1_-FA1X4_P4	1.600	2.040	3.2640
C8T28SOIDV_LLS1_-FA1X9_P4	1.600	3.128	5.0048
C8T28SOIDV_LLS1_-FA1X18_P4	1.600	4.352	6.9632

Truth Table

A0	B0	CI	S0
A0	!A0	CI	!CI
A0	A0	CI	CI

A0	B0	CI	CO
A0	-	A0	A0
A0	A0	-	A0
-	B0	B0	B0

Pin Capacitance

Pin	C8T28SOIDV_LL_-FA1X5_P4	C8T28SOIDV_LL_-FA1X9_P4	C8T28SOIDV_LL_-FA1X14_P4	C8T28SOIDV_LL_-FA1X19_P4
A0	0.0023	0.0025	0.0039	0.0042
B0	0.0020	0.0021	0.0036	0.0039
CI	0.0014	0.0015	0.0026	0.0028
	C8T28SOIDV_LLS1_-FA1X4_P4	C8T28SOIDV_LLS1_-FA1X9_P4	C8T28SOIDV_LLS1_-FA1X18_P4	
A0	0.0022	0.0030	0.0032	
B0	0.0021	0.0034	0.0038	
CI	0.0016	0.0024	0.0029	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-FA1X5_P4	**C8T28SOIDV_LL_-FA1X9_P4**	**C8T28SOIDV_LL_-FA1X5_P4**	**C8T28SOIDV_LL_-FA1X9_P4**
A0 to CO ↓	0.0290	0.0315	2.7812	1.4189
A0 to CO ↑	0.0230	0.0253	3.3295	1.7046
A0 to S0 ↓	0.0320	0.0355	2.7410	1.4076
A0 to S0 ↑	0.0332	0.0365	3.3463	1.6771
B0 to CO ↓	0.0296	0.0323	2.7888	1.4236
B0 to CO ↑	0.0242	0.0265	3.3309	1.7065
B0 to S0 ↓	0.0328	0.0365	2.7419	1.4075
B0 to S0 ↑	0.0342	0.0376	3.3469	1.6770
CI to CO ↓	0.0292	0.0318	2.7866	1.4212
CI to CO ↑	0.0243	0.0267	3.3268	1.7031
CI to S0 ↓	0.0328	0.0367	2.7428	1.4084
CI to S0 ↑	0.0345	0.0379	3.3474	1.6766
	C8T28SOIDV_LL_-FA1X14_P4	**C8T28SOIDV_LL_-FA1X19_P4**	**C8T28SOIDV_LL_-FA1X14_P4**	**C8T28SOIDV_LL_-FA1X19_P4**
A0 to CO ↓	0.0298	0.0328	0.9275	0.7041
A0 to CO ↑	0.0239	0.0250	1.1752	0.8767
A0 to S0 ↓	0.0370	0.0378	0.9210	0.6845
A0 to S0 ↑	0.0385	0.0400	1.1315	0.8454
B0 to CO ↓	0.0299	0.0330	0.9297	0.7047
B0 to CO ↑	0.0246	0.0257	1.1745	0.8758
B0 to S0 ↓	0.0377	0.0385	0.9219	0.6846
B0 to S0 ↑	0.0393	0.0407	1.1328	0.8458
CI to CO ↓	0.0295	0.0324	0.9276	0.7034
CI to CO ↑	0.0246	0.0257	1.1742	0.8758
CI to S0 ↓	0.0376	0.0384	0.9216	0.6850
CI to S0 ↑	0.0392	0.0407	1.1320	0.8456
	C8T28SOIDV_-LLS1_FA1X4_P4	**C8T28SOIDV_-LLS1_FA1X9_P4**	**C8T28SOIDV_-LLS1_FA1X4_P4**	**C8T28SOIDV_-LLS1_FA1X9_P4**
A0 to CO ↓	0.0212	0.0187	4.8931	1.6660
A0 to CO ↑	0.0203	0.0183	3.3875	1.7020
A0 to S0 ↓	0.0439	0.0469	2.9167	1.0679
A0 to S0 ↑	0.0417	0.0404	3.5134	1.6665
B0 to CO ↓	0.0197	0.0199	4.8869	1.6679
B0 to CO ↑	0.0159	0.0167	3.3785	1.7012
B0 to S0 ↓	0.0436	0.0490	2.9149	1.0682
B0 to S0 ↑	0.0416	0.0425	3.5106	1.6666
CI to CO ↓	0.0205	0.0287	4.8860	1.6754
CI to CO ↑	0.0168	0.0151	3.3915	1.7153

CI to S0 ↓	0.0250	0.0299	2.9202	1.0703
CI to S0 ↑	0.0219	0.0225	3.5151	1.6660
	C8T28SOIDV_-LLS1_FA1X18_P4		**C8T28SOIDV_-LLS1_FA1X18_P4**	
A0 to CO ↓	0.0242		0.8808	
A0 to CO ↑	0.0186		0.8377	
A0 to S0 ↓	0.0503		0.5521	
A0 to S0 ↑	0.0413		0.8375	
B0 to CO ↓	0.0259		0.8820	
B0 to CO ↑	0.0172		0.8372	
B0 to S0 ↓	0.0517		0.5522	
B0 to S0 ↑	0.0428		0.8375	
CI to CO ↓	0.0357		0.8856	
CI to CO ↑	0.0188		0.8391	
CI to S0 ↓	0.0310		0.5529	
CI to S0 ↑	0.0211		0.8376	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_FA1X5_P4	3.083e-04	1.000e-20
C8T28SOIDV_LL_FA1X9_P4	4.258e-04	1.000e-20
C8T28SOIDV_LL_FA1X14_P4	6.388e-04	1.000e-20
C8T28SOIDV_LL_FA1X19_P4	7.961e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X4_P4	6.881e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X9_P4	9.835e-04	1.000e-20
C8T28SOIDV_LLS1_FA1X18_P4	1.487e-03	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-FA1X5_P4	C8T28SOIDV_LL_-FA1X9_P4	C8T28SOIDV_LL_-FA1X14_P4	C8T28SOIDV_LL_-FA1X19_P4
A0 to CO	3.869e-03	5.945e-03	9.523e-03	1.205e-02
A0 to S0	3.936e-03	5.848e-03	9.739e-03	1.227e-02
B0 to CO	3.911e-03	6.036e-03	9.610e-03	1.220e-02
B0 to S0	3.914e-03	5.859e-03	9.723e-03	1.225e-02
CI to CO	3.941e-03	6.040e-03	9.746e-03	1.238e-02
CI to S0	3.901e-03	5.858e-03	9.715e-03	1.223e-02
	C8T28SOIDV_LLS1_-FA1X4_P4	C8T28SOIDV_LLS1_-FA1X9_P4	C8T28SOIDV_LLS1_-FA1X18_P4	
A0 to CO	5.882e-03	9.200e-03	1.492e-02	
A0 to S0	7.912e-03	1.181e-02	1.846e-02	
B0 to CO	6.182e-03	9.311e-03	1.503e-02	
B0 to S0	8.438e-03	1.206e-02	1.871e-02	
CI to CO	4.360e-03	7.754e-03	1.378e-02	
CI to S0	4.974e-03	8.675e-03	1.497e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOIDV_LL_-FA1X5_P4	C8T28SOIDV_LL_-FA1X9_P4	C8T28SOIDV_LL_-FA1X14_P4	C8T28SOIDV_LL_-FA1X19_P4
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00

B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CI to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS1_-FA1X4_P4	C8T28SOIDV_LLS1_-FA1X9_P4	C8T28SOIDV_LLS1_-FA1X18_P4	
A0 to CO	0.000e+00	0.000e+00	0.000e+00	
A0 to S0	0.000e+00	0.000e+00	0.000e+00	
B0 to CO	0.000e+00	0.000e+00	0.000e+00	
B0 to S0	0.000e+00	0.000e+00	0.000e+00	
CI to CO	0.000e+00	0.000e+00	0.000e+00	
CI to S0	0.000e+00	0.000e+00	0.000e+00	

HA1

Cell Description

Half-adder having 1 bit input operand

Logical Symbol

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_HA1X5_P4	0.800	1.360	1.0880
C8T28SOI_LL_HA1X9_P4	0.800	1.632	1.3056
C8T28SOI_LLS1_HA1X5_-P4	0.800	1.904	1.5232
C8T28SOIDV_LL_-HA1X14_P4	1.600	1.496	2.3936
C8T28SOIDV_LL_-HA1X19_P4	1.600	1.496	2.3936
C8T28SOIDV_LLS1_-HA1X11_P4	1.600	1.904	3.0464

Truth Table

A0	B0	S0
1	B0	!B0
0	B0	B0

A0	B0	CO
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	C8T28SOI_LL_-HA1X5_P4	C8T28SOI_LL_-HA1X9_P4	C8T28SOI_LLS1_-HA1X5_P4	C8T28SOIDV_LL_-HA1X14_P4
A0	0.0008	0.0011	0.0013	0.0016
B0	0.0007	0.0011	0.0012	0.0014
	C8T28SOIDV_LL_-HA1X19_P4	C8T28SOIDV_LLS1_-HA1X11_P4		
A0	0.0020	0.0019		
B0	0.0017	0.0019		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-HA1X5_P4	**C8T28SOI_LL_-HA1X9_P4**	**C8T28SOI_LL_-HA1X5_P4**	**C8T28SOI_LL_-HA1X9_P4**
A0 to CO ↓	0.0239	0.0209	2.7549	1.3549
A0 to CO ↑	0.0221	0.0201	3.5507	1.7195
A0 to S0 ↓	0.0296	0.0278	2.6524	1.3411
A0 to S0 ↑	0.0290	0.0276	3.4461	1.7192
B0 to CO ↓	0.0233	0.0204	2.7588	1.3554
B0 to CO ↑	0.0245	0.0226	3.5495	1.7198
B0 to S0 ↓	0.0317	0.0296	2.6498	1.3408
B0 to S0 ↑	0.0284	0.0270	3.4441	1.7192
	C8T28SOI_LLS1_-HA1X5_P4	**C8T28SOIDV_LL_-HA1X14_P4**	**C8T28SOI_LLS1_-HA1X5_P4**	**C8T28SOIDV_LL_-HA1X14_P4**
A0 to CO ↓	0.0192	0.0217	2.7105	0.9260
A0 to CO ↑	0.0175	0.0195	3.5119	1.1572
A0 to S0 ↓	0.0253	0.0303	2.7074	0.9367
A0 to S0 ↑	0.0300	0.0302	3.5305	1.1360
B0 to CO ↓	0.0181	0.0199	2.7088	0.9228
B0 to CO ↑	0.0193	0.0210	3.5099	1.1559
B0 to S0 ↓	0.0274	0.0312	2.7075	0.9365
B0 to S0 ↑	0.0293	0.0287	3.5297	1.1365
	C8T28SOIDV_LL_-HA1X19_P4	**C8T28SOIDV_-LLS1_HA1X11_P4**	**C8T28SOIDV_LL_-HA1X19_P4**	**C8T28SOIDV_-LLS1_HA1X11_P4**
A0 to CO ↓	0.0206	0.0188	0.6845	0.9894
A0 to CO ↑	0.0194	0.0198	0.8786	1.6877
A0 to S0 ↓	0.0284	0.0238	0.6822	1.0023
A0 to S0 ↑	0.0283	0.0263	0.8530	1.7057
B0 to CO ↓	0.0190	0.0176	0.6831	0.9886
B0 to CO ↑	0.0210	0.0218	0.8780	1.6873
B0 to S0 ↓	0.0296	0.0243	0.6814	1.0017
B0 to S0 ↑	0.0270	0.0263	0.8532	1.7050

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_HA1X5_P4	1.818e-04	1.000e-20
C8T28SOI_LL_HA1X9_P4	4.104e-04	1.000e-20
C8T28SOI_LLS1_HA1X5_P4	2.250e-04	1.000e-20
C8T28SOIDV_LL_HA1X14_P4	5.936e-04	1.000e-20
C8T28SOIDV_LL_HA1X19_P4	8.175e-04	1.000e-20
C8T28SOIDV_LLS1_HA1X11_P4	5.251e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

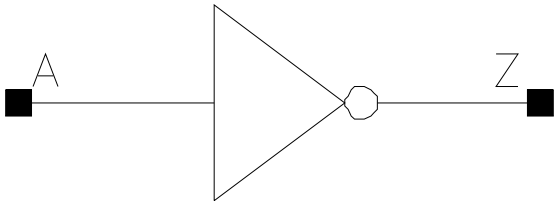
Pin Cycle (vdd)	C8T28SOI_LL_-HA1X5_P4	C8T28SOI_LL_-HA1X9_P4	C8T28SOI_LLS1_-HA1X5_P4	C8T28SOIDV_LL_-HA1X14_P4
A0 to CO	2.959e-03	5.017e-03	3.487e-03	7.921e-03
A0 to S0	2.770e-03	4.987e-03	3.188e-03	8.157e-03
B0 to CO	3.001e-03	5.196e-03	3.526e-03	7.980e-03
B0 to S0	2.744e-03	4.925e-03	3.121e-03	8.015e-03
	C8T28SOIDV_LL_-HA1X19_P4	C8T28SOIDV_LLS1_-HA1X11_P4		
A0 to CO	9.816e-03	6.889e-03		
A0 to S0	1.007e-02	6.407e-03		

B0 to CO	9.865e-03	6.421e-03		
B0 to S0	9.909e-03	6.498e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOI_LL_-HA1X5_P4	C8T28SOI_LL_-HA1X9_P4	C8T28SOI_LLS1_-HA1X5_P4	C8T28SOIDV_LL_-HA1X14_P4
A0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to CO	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B0 to S0	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-HA1X19_P4	C8T28SOIDV_LLS1_-HA1X11_P4		
A0 to CO	0.000e+00	0.000e+00		
A0 to S0	0.000e+00	0.000e+00		
B0 to CO	0.000e+00	0.000e+00		
B0 to S0	0.000e+00	0.000e+00		

IV

Cell Description	Logical Symbol
Inverter	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_IVX2_P4	0.800	0.272	0.2176
C8T28SOI_LL_IVX3_P4	0.800	0.272	0.2176
C8T28SOI_LL_IVX5_P4	0.800	0.272	0.2176
C8T28SOI_LL_IVX10_P4	0.800	0.408	0.3264
C8T28SOI_LL_IVX14_P4	0.800	0.544	0.4352
C8T28SOI_LL_IVX19_P4	0.800	0.680	0.5440
C8T28SOI_LL_IVX29_P4	0.800	0.952	0.7616
C8T28SOI_LL_IVX34_P4	0.800	1.088	0.8704
C8T28SOI_LL_IVX38_P4	0.800	1.224	0.9792
C8T28SOIDV_LL_IVX11_-P4	1.600	0.272	0.4352
C8T28SOIDV_LL_IVX23_-P4	1.600	0.408	0.6528
C8T28SOIDV_LL_IVX34_-P4	1.600	0.544	0.8704
C8T28SOIDV_LL_IVX46_-P4	1.600	0.680	1.0880
C8T28SOIDV_LL_IVX68_-P4	1.600	0.952	1.5232
C8T28SOIDV_LL_IVX91_-P4	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_IVX2_-P4	C8T28SOI_LL_IVX3_-P4	C8T28SOI_LL_IVX5_-P4	C8T28SOI_LL_-IVX10_P4

A	0.0004	0.0005	0.0006	0.0011
	C8T28SOI_LL_-IVX14_P4	C8T28SOI_LL_-IVX19_P4	C8T28SOI_LL_-IVX29_P4	C8T28SOI_LL_-IVX34_P4
A	0.0018	0.0023	0.0034	0.0040
	C8T28SOI_LL_-IVX38_P4	C8T28SOIDV_LL_-IVX11_P4	C8T28SOIDV_LL_-IVX23_P4	C8T28SOIDV_LL_-IVX34_P4
A	0.0046	0.0012	0.0025	0.0036
	C8T28SOIDV_LL_-IVX46_P4	C8T28SOIDV_LL_-IVX68_P4	C8T28SOIDV_LL_-IVX91_P4	
A	0.0049	0.0074	0.0103	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-IVX2_P4	**C8T28SOI_LL_-IVX3_P4**	**C8T28SOI_LL_-IVX2_P4**	**C8T28SOI_LL_-IVX3_P4**
A to Z ↓	0.0043	0.0042	5.0949	4.0002
A to Z ↑	0.0094	0.0086	6.5529	5.0734
	C8T28SOI_LL_-IVX5_P4	**C8T28SOI_LL_-IVX10_P4**	**C8T28SOI_LL_-IVX5_P4**	**C8T28SOI_LL_-IVX10_P4**
A to Z ↓	0.0039	0.0029	2.8063	1.3485
A to Z ↑	0.0077	0.0064	3.6125	1.7226
	C8T28SOI_LL_-IVX14_P4	**C8T28SOI_LL_-IVX19_P4**	**C8T28SOI_LL_-IVX14_P4**	**C8T28SOI_LL_-IVX19_P4**
A to Z ↓	0.0032	0.0035	0.9337	0.7121
A to Z ↑	0.0063	0.0066	1.1598	0.8917
	C8T28SOI_LL_-IVX29_P4	**C8T28SOI_LL_-IVX34_P4**	**C8T28SOI_LL_-IVX29_P4**	**C8T28SOI_LL_-IVX34_P4**
A to Z ↓	0.0035	0.0032	0.4758	0.4055
A to Z ↑	0.0064	0.0061	0.5900	0.5035
	C8T28SOI_LL_-IVX38_P4	**C8T28SOIDV_LL_-IVX11_P4**	**C8T28SOI_LL_-IVX38_P4**	**C8T28SOIDV_LL_-IVX11_P4**
A to Z ↓	0.0034	0.0027	0.3597	1.0888
A to Z ↑	0.0062	0.0078	0.4472	1.7400
	C8T28SOIDV_LL_-IVX23_P4	**C8T28SOIDV_LL_-IVX34_P4**	**C8T28SOIDV_LL_-IVX23_P4**	**C8T28SOIDV_LL_-IVX34_P4**
A to Z ↓	0.0022	0.0025	0.5304	0.3628
A to Z ↑	0.0071	0.0071	0.8488	0.5703
	C8T28SOIDV_LL_-IVX46_P4	**C8T28SOIDV_LL_-IVX68_P4**	**C8T28SOIDV_LL_-IVX46_P4**	**C8T28SOIDV_LL_-IVX68_P4**
A to Z ↓	0.0025	0.0025	0.2729	0.1858
A to Z ↑	0.0070	0.0068	0.4278	0.2876
	C8T28SOIDV_LL_-IVX91_P4		**C8T28SOIDV_LL_-IVX91_P4**	
A to Z ↓	0.0030		0.1441	
A to Z ↑	0.0072		0.2188	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_IVX2_P4	2.480e-05	1.000e-20
C8T28SOI_LL_IVX3_P4	3.523e-05	1.000e-20
C8T28SOI_LL_IVX5_P4	5.291e-05	1.000e-20
C8T28SOI_LL_IVX10_P4	1.132e-04	1.000e-20

C8T28SOI_LL_IVX14_P4	1.631e-04	1.000e-20
C8T28SOI_LL_IVX19_P4	2.125e-04	1.000e-20
C8T28SOI_LL_IVX29_P4	3.113e-04	1.000e-20
C8T28SOI_LL_IVX34_P4	3.607e-04	1.000e-20
C8T28SOI_LL_IVX38_P4	4.101e-04	1.000e-20
C8T28SOIDV_LL_IVX11_P4	1.226e-04	1.000e-20
C8T28SOIDV_LL_IVX23_P4	2.487e-04	1.000e-20
C8T28SOIDV_LL_IVX34_P4	3.613e-04	1.000e-20
C8T28SOIDV_LL_IVX46_P4	4.725e-04	1.000e-20
C8T28SOIDV_LL_IVX68_P4	6.946e-04	1.000e-20
C8T28SOIDV_LL_IVX91_P4	9.168e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_IVX2_-P4	C8T28SOI_LL_IVX3_-P4	C8T28SOI_LL_IVX5_-P4	C8T28SOI_LL_-IVX10_P4
A to Z	8.053e-04	1.016e-03	1.349e-03	2.737e-03
	C8T28SOI_LL_-IVX14_P4	C8T28SOI_LL_-IVX19_P4	C8T28SOI_LL_-IVX29_P4	C8T28SOI_LL_-IVX34_P4
A to Z	4.084e-03	5.403e-03	7.978e-03	9.160e-03
	C8T28SOI_LL_-IVX38_P4	C8T28SOIDV_LL_-IVX11_P4	C8T28SOIDV_LL_-IVX23_P4	C8T28SOIDV_LL_-IVX34_P4
A to Z	1.045e-02	3.021e-03	5.952e-03	8.842e-03
	C8T28SOIDV_LL_-IVX46_P4	C8T28SOIDV_LL_-IVX68_P4	C8T28SOIDV_LL_-IVX91_P4	
A to Z	1.165e-02	1.718e-02	2.308e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

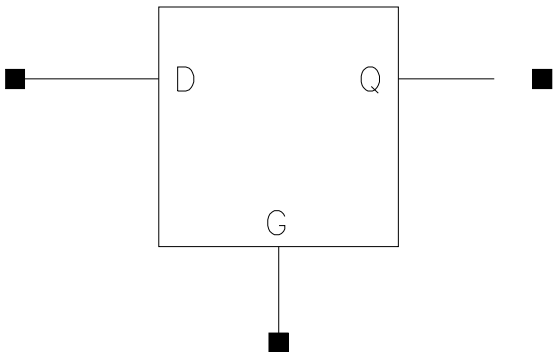
Pin Cycle (vdds)	C8T28SOI_LL_IVX2_-P4	C8T28SOI_LL_IVX3_-P4	C8T28SOI_LL_IVX5_-P4	C8T28SOI_LL_-IVX10_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX14_P4	C8T28SOI_LL_-IVX19_P4	C8T28SOI_LL_-IVX29_P4	C8T28SOI_LL_-IVX34_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-IVX38_P4	C8T28SOIDV_LL_-IVX11_P4	C8T28SOIDV_LL_-IVX23_P4	C8T28SOIDV_LL_-IVX34_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-IVX46_P4	C8T28SOIDV_LL_-IVX68_P4	C8T28SOIDV_LL_-IVX91_P4	
A to Z	0.000e+00	0.000e+00	0.000e+00	

LDHQ

Cell Description

Active High transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.360	1.0880
X9_P4	1.600	0.952	1.5232
X19_P4	1.600	1.224	1.9584
X28_P4	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4	X28_P4
D	0.0004	0.0007	0.0010	0.0017
G	0.0009	0.0009	0.0017	0.0017

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D to Q ↓	0.0329	0.0323	2.7714	1.4305
D to Q ↑	0.0195	0.0235	3.4514	1.6775
G to Q ↓	0.0344	0.0343	2.7655	1.4277

G to Q ↑	0.0194	0.0223	3.4532	1.6769
	X19_P4	**X28_P4**	**X19_P4**	**X28_P4**
D to Q ↓	0.0261	0.0269	0.6864	0.4629
D to Q ↑	0.0212	0.0214	0.8466	0.5701
G to Q ↓	0.0295	0.0268	0.6846	0.4615
G to Q ↑	0.0190	0.0190	0.8474	0.5701

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P4	X9_P4	X19_P4	X28_P4
D ↓	hold_falling to G	0.0031	0.0058	0.0102	0.0074
D ↑	hold_falling to G	0.0114	0.0089	0.0090	0.0090
D ↓	setup_falling to G	0.0320	0.0295	0.0215	0.0247
D ↑	setup_falling to G	0.0210	0.0263	0.0231	0.0231
G ↑	min_pulse_width to G	0.0284	0.0284	0.0271	0.0271

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.336e-04	1.000e-20
X9_P4	2.219e-04	1.000e-20
X19_P4	3.791e-04	1.000e-20
X28_P4	5.202e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	1.233e-05	3.237e-05	3.691e-05	9.555e-05
G (output stable)	1.277e-03	1.558e-03	2.576e-03	2.542e-03
D to Q	4.780e-03	7.657e-03	1.182e-02	1.684e-02
G to Q	4.682e-03	7.466e-03	1.120e-02	1.521e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

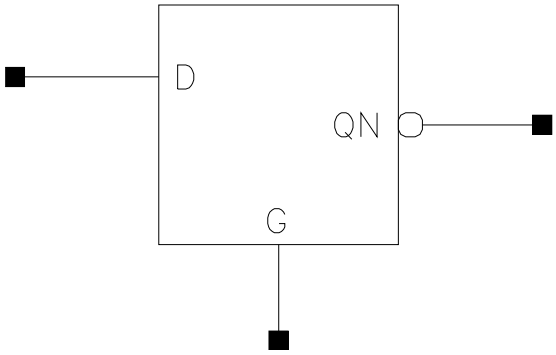
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
G to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDHQN

Cell Description

Active High transparent Latch; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P4	0.800	1.496	1.1968

Truth Table

IQ	QN
IQ	!IQ

D	G	IQ	IQ
D	1	-	D
-	0	IQ	IQ

Pin Capacitance

Pin	X10_P4
D	0.0004
G	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)	Kload (ns/pf)
	X10_P4	X10_P4
D to QN ↓	0.0294	1.3004
D to QN ↑	0.0394	1.6744
G to QN ↓	0.0289	1.3012
G to QN ↑	0.0411	1.6736

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X10_P4
D ↓	hold_falling to G	-0.0013
D ↑	hold_falling to G	0.0030
D ↓	setup_falling to G	0.0295
D ↑	setup_falling to G	0.0215
G ↑	min_pulse_width to G	0.0283

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X10_P4	2.074e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X10_P4
D (output stable)	1.191e-05
G (output stable)	1.505e-03
D to QN	5.980e-03
G to QN	5.996e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

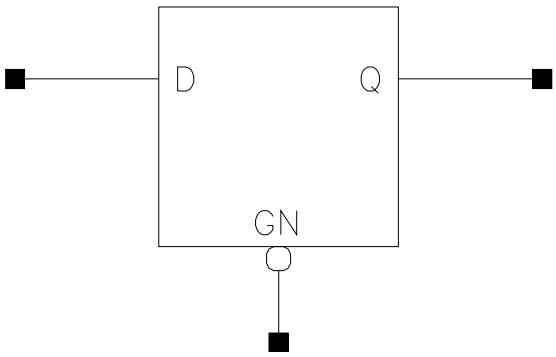
Pin Cycle (vdds)	X10_P4
D (output stable)	0.000e+00
G (output stable)	0.000e+00
D to QN	0.000e+00
G to QN	0.000e+00

LDLQ

Cell Description

Active Low transparent Latch; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.360	1.0880
X9_P4	1.600	0.952	1.5232
X19_P4	1.600	1.224	1.9584
X28_P4	1.600	1.496	2.3936

Truth Table

IQ	Q
IQ	IQ

D	GN	IQ	IQ
D	0	-	D
-	1	IQ	IQ

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4	X28_P4
D	0.0004	0.0007	0.0010	0.0015
GN	0.0009	0.0009	0.0013	0.0018

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D to Q ↓	0.0332	0.0319	2.7780	1.4330
D to Q ↑	0.0196	0.0234	3.4464	1.6789
GN to Q ↓	0.0309	0.0310	2.7800	1.4338

GN to Q ↑	0.0342	0.0330	3.4439	1.6731
	X19_P4	**X28_P4**	**X19_P4**	**X28_P4**
D to Q ↓	0.0265	0.0260	0.6829	0.4616
D to Q ↑	0.0221	0.0218	0.8393	0.5636
GN to Q ↓	0.0235	0.0225	0.6828	0.4614
GN to Q ↑	0.0301	0.0298	0.8385	0.5626

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P4	X9_P4	X19_P4	X28_P4
D ↓	hold_rising to GN	-0.0003	0.0019	0.0068	0.0068
D ↑	hold_rising to GN	0.0127	0.0128	0.0128	0.0128
D ↓	setup_rising to GN	0.0399	0.0325	0.0303	0.0277
D ↑	setup_rising to GN	0.0168	0.0223	0.0190	0.0191
GN ↓	min_pulse_width to GN	0.0426	0.0388	0.0318	0.0309

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.332e-04	1.000e-20
X9_P4	2.272e-04	1.000e-20
X19_P4	4.078e-04	1.000e-20
X28_P4	5.419e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	1.233e-05	1.967e-05	3.791e-05	8.259e-05
GN (output stable)	1.272e-03	1.544e-03	2.292e-03	2.401e-03
D to Q	4.789e-03	7.704e-03	1.217e-02	1.667e-02
GN to Q	6.819e-03	9.914e-03	1.488e-02	1.897e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

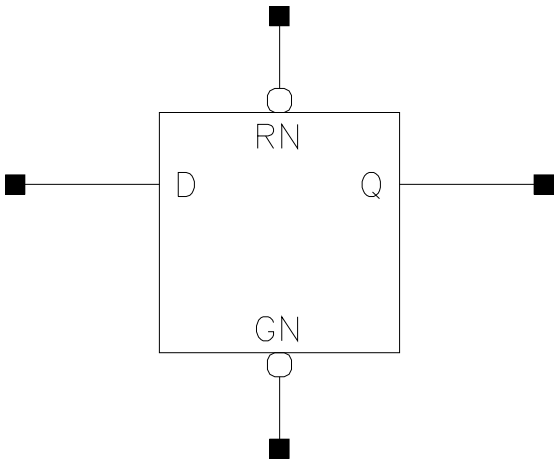
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4	X28_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

LDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.632	1.3056
X9_P4	1.600	1.224	1.9584
X19_P4	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4
D	0.0004	0.0006	0.0012
GN	0.0010	0.0010	0.0015
RN	0.0004	0.0005	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D to Q ↓	0.0337	0.0327	2.7189	1.3872

D to Q ↑	0.0327	0.0361	3.5553	1.7310
GN to Q ↓	0.0320	0.0308	2.7219	1.3894
GN to Q ↑	0.0442	0.0420	3.5522	1.7336
RN to Q ↓	0.0286	0.0351	2.5918	1.3529
RN to Q ↑	0.0342	0.0376	3.5556	1.7340
	X19_P4		**X19_P4**	
D to Q ↓	0.0270		0.6882	
D to Q ↑	0.0391		0.8747	
GN to Q ↓	0.0245		0.6889	
GN to Q ↑	0.0407		0.8771	
RN to Q ↓	0.0432		0.6932	
RN to Q ↑	0.0431		0.8771	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P4	X9_P4	X19_P4
D ↓	hold_rising to GN	0.0023	0.0019	0.0041
D ↑	hold_rising to GN	0.0032	0.0010	-0.0039
D ↓	setup_rising to GN	0.0401	0.0385	0.0279
D ↑	setup_rising to GN	0.0340	0.0394	0.0436
GN ↓	min_pulse_width to GN	0.0465	0.0434	0.0449
RN ↓	min_pulse_width to RN	0.0354	0.0425	0.0544
RN ↑	recovery_rising to GN	0.0373	0.0389	0.0460
RN ↑	removal_rising to GN	-0.0169	-0.0217	-0.0294

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.491e-04	1.000e-20
X9_P4	2.396e-04	1.000e-20
X19_P4	4.161e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4
D (output stable)	5.567e-05	4.414e-05	6.920e-05
GN (output stable)	1.376e-03	1.525e-03	1.993e-03
RN (output stable)	4.247e-05	5.295e-05	7.439e-05
D to Q	6.023e-03	8.791e-03	1.425e-02
GN to Q	8.236e-03	1.102e-02	1.683e-02
RN to Q	4.277e-03	6.407e-03	1.134e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

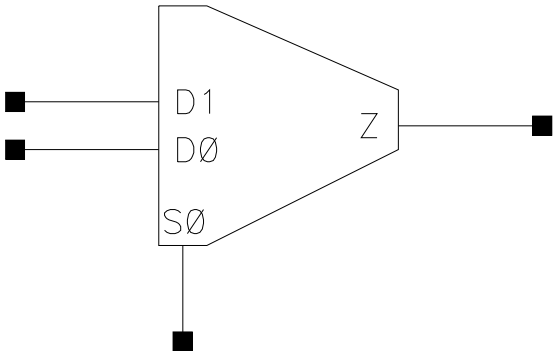
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4
D (output stable)	0.000e+00	0.000e+00	0.000e+00
GN (output stable)	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00

MUX21

Cell Description

2:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.360	1.0880
X9_P4	0.800	1.496	1.1968
X14_P4	0.800	2.176	1.7408
X19_P4	0.800	2.312	1.8496

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X5_P4	X9_P4	X14_P4	X19_P4
D0	0.0006	0.0007	0.0010	0.0013
D1	0.0005	0.0007	0.0010	0.0013
S0	0.0010	0.0010	0.0013	0.0016

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X9_P4	X5_P4	X9_P4
D0 to Z ↓	0.0253	0.0242	2.7770	1.4046
D0 to Z ↑	0.0207	0.0207	3.5239	1.7920
D1 to Z ↓	0.0255	0.0234	2.7745	1.4019
D1 to Z ↑	0.0204	0.0197	3.5280	1.7914
S0 to Z ↓	0.0240	0.0215	2.7662	1.3975
S0 to Z ↑	0.0230	0.0215	3.5239	1.7917

	X14_P4	X19_P4	X14_P4	X19_P4
D0 to Z ↓	0.0261	0.0233	0.9652	0.6979
D0 to Z ↑	0.0215	0.0202	1.2113	0.8792
D1 to Z ↓	0.0263	0.0238	0.9648	0.6990
D1 to Z ↑	0.0209	0.0198	1.2108	0.8778
S0 to Z ↓	0.0255	0.0237	0.9615	0.6966
S0 to Z ↑	0.0248	0.0230	1.2089	0.8774

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.613e-04	1.000e-20
X9_P4	2.847e-04	1.000e-20
X14_P4	3.805e-04	1.000e-20
X19_P4	5.591e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X9_P4	X14_P4	X19_P4
D0 (output stable)	1.112e-03	1.869e-03	2.313e-03	3.110e-03
D1 (output stable)	1.060e-03	1.676e-03	2.357e-03	3.179e-03
S0 (output stable)	1.357e-03	1.279e-03	1.841e-03	2.306e-03
D0 to Z	3.432e-03	5.699e-03	8.952e-03	1.126e-02
D1 to Z	3.375e-03	5.377e-03	8.772e-03	1.119e-02
S0 to Z	4.193e-03	5.649e-03	9.672e-03	1.194e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

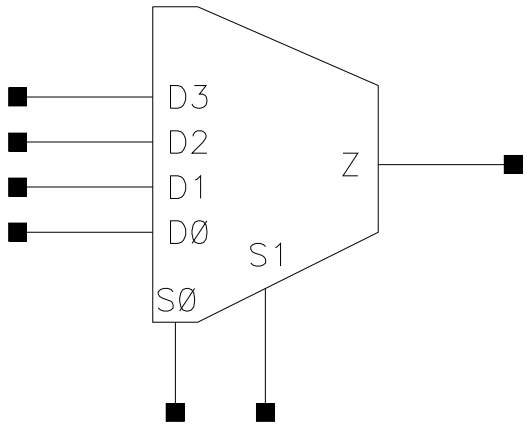
Pin Cycle (vdds)	X5_P4	X9_P4	X14_P4	X19_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUX41

Cell Description

4:1 non-inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.600	1.496	2.3936
X9_P4	1.600	1.768	2.8288
X13_P4	1.600	2.312	3.6992
X18_P4	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X4_P4	X9_P4	X13_P4	X18_P4
D0	0.0005	0.0007	0.0010	0.0010
D1	0.0004	0.0006	0.0011	0.0011
D2	0.0004	0.0007	0.0011	0.0011
D3	0.0004	0.0006	0.0011	0.0010
S0	0.0013	0.0017	0.0023	0.0024
S1	0.0008	0.0009	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X9_P4**	**X4_P4**	**X9_P4**
D0 to Z ↓	0.0517	0.0438	2.9803	1.4643
D0 to Z ↑	0.0348	0.0326	3.6095	1.7909
D1 to Z ↓	0.0510	0.0435	2.9779	1.4651
D1 to Z ↑	0.0346	0.0323	3.6051	1.7897
D2 to Z ↓	0.0470	0.0441	2.9389	1.4683
D2 to Z ↑	0.0333	0.0322	3.5875	1.7892
D3 to Z ↓	0.0475	0.0433	2.9448	1.4675
D3 to Z ↑	0.0339	0.0322	3.5881	1.7881
S0 to Z ↓	0.0536	0.0484	2.9610	1.4654
S0 to Z ↑	0.0408	0.0398	3.6074	1.7928
S1 to Z ↓	0.0360	0.0344	2.9567	1.4645
S1 to Z ↑	0.0322	0.0319	3.6006	1.7892
	X13_P4	**X18_P4**	**X13_P4**	**X18_P4**
D0 to Z ↓	0.0438	0.0478	1.0296	0.7696
D0 to Z ↑	0.0291	0.0317	1.2022	0.9077
D1 to Z ↓	0.0441	0.0480	1.0307	0.7702
D1 to Z ↑	0.0299	0.0325	1.2016	0.9083
D2 to Z ↓	0.0393	0.0428	1.0130	0.7563
D2 to Z ↑	0.0291	0.0317	1.1981	0.9054
D3 to Z ↓	0.0390	0.0425	1.0117	0.7558
D3 to Z ↑	0.0293	0.0319	1.1974	0.9055
S0 to Z ↓	0.0467	0.0504	1.0211	0.7630
S0 to Z ↑	0.0363	0.0388	1.2014	0.9078
S1 to Z ↓	0.0340	0.0378	1.0205	0.7627
S1 to Z ↑	0.0289	0.0314	1.1998	0.9066

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	1.575e-04	1.000e-20
X9_P4	2.561e-04	1.000e-20
X13_P4	4.356e-04	1.000e-20
X18_P4	4.896e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X9_P4	X13_P4	X18_P4
D0 (output stable)	5.128e-05	5.860e-05	1.165e-04	1.159e-04
D1 (output stable)	7.346e-05	7.520e-05	1.092e-04	1.088e-04
D2 (output stable)	6.579e-05	7.596e-05	1.079e-04	1.082e-04
D3 (output stable)	5.494e-05	7.613e-05	1.001e-04	1.002e-04
S0 (output stable)	1.634e-03	1.909e-03	3.109e-03	3.111e-03
S1 (output stable)	1.900e-03	2.082e-03	3.317e-03	3.324e-03
D0 to Z	4.436e-03	6.960e-03	1.095e-02	1.415e-02
D1 to Z	4.377e-03	6.940e-03	1.106e-02	1.427e-02
D2 to Z	4.150e-03	6.944e-03	1.035e-02	1.332e-02
D3 to Z	4.198e-03	6.938e-03	1.035e-02	1.331e-02
S0 to Z	6.124e-03	9.088e-03	1.414e-02	1.725e-02
S1 to Z	5.295e-03	7.836e-03	1.209e-02	1.514e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

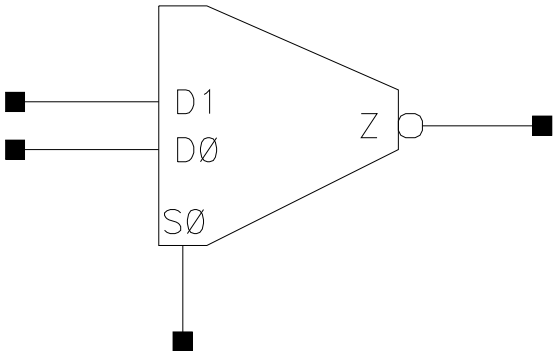
Pin Cycle (vdds)	X4_P4	X9_P4	X13_P4	X18_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

MUXI21

Cell Description

2:1 inverting Multiplexer with coded selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X1_P4	0.800	0.952	0.7616
X2_P4	0.800	0.952	0.7616
X6_P4	0.800	1.904	1.5232
X9_P4	0.800	2.448	1.9584
X12_P4	0.800	2.992	2.3936

Truth Table

D0	D1	S0	Z
D0	-	0	!D0
-	D1	1	!D1

Pin Capacitance

Pin	X1_P4	X2_P4	X6_P4	X9_P4
D0	0.0004	0.0005	0.0012	0.0018
D1	0.0004	0.0005	0.0011	0.0017
S0	0.0010	0.0013	0.0018	0.0026
	X12_P4			
D0	0.0024			
D1	0.0023			
S0	0.0030			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X1_P4	X2_P4	X1_P4	X2_P4
D0 to Z ↓	0.0080	0.0076	7.1970	4.9679

D0 to Z ↑	0.0169	0.0133	13.4266	7.5328
D1 to Z ↓	0.0077	0.0074	7.1222	4.8497
D1 to Z ↑	0.0171	0.0132	13.4519	7.6989
S0 to Z ↓	0.0156	0.0115	7.1257	4.8937
S0 to Z ↑	0.0179	0.0125	13.3994	7.5976
	X6_P4	**X9_P4**	**X6_P4**	**X9_P4**
D0 to Z ↓	0.0090	0.0082	2.2525	1.5148
D0 to Z ↑	0.0136	0.0129	3.1928	2.2340
D1 to Z ↓	0.0086	0.0084	2.2095	1.5218
D1 to Z ↑	0.0143	0.0131	3.3023	2.1830
S0 to Z ↓	0.0136	0.0117	2.2255	1.5159
S0 to Z ↑	0.0145	0.0128	3.2405	2.2078
	X12_P4		**X12_P4**	
D0 to Z ↓	0.0085		1.1590	
D0 to Z ↑	0.0130		1.6861	
D1 to Z ↓	0.0083		1.1532	
D1 to Z ↑	0.0131		1.6469	
S0 to Z ↓	0.0127		1.1540	
S0 to Z ↑	0.0137		1.6655	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X1_P4	5.428e-05	1.000e-20
X2_P4	1.139e-04	1.000e-20
X6_P4	2.262e-04	1.000e-20
X9_P4	3.556e-04	1.000e-20
X12_P4	4.310e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X1_P4	X2_P4	X6_P4	X9_P4
D0 (output stable)	1.188e-05	2.639e-05	7.755e-05	1.111e-04
D1 (output stable)	1.145e-05	2.716e-05	8.335e-05	1.196e-04
S0 (output stable)	1.302e-03	1.711e-03	2.568e-03	4.313e-03
D0 to Z	1.082e-03	1.496e-03	3.761e-03	5.240e-03
D1 to Z	1.084e-03	1.471e-03	3.756e-03	5.279e-03
S0 to Z	2.172e-03	2.731e-03	5.238e-03	7.873e-03
	X12_P4			
D0 (output stable)	1.454e-04			
D1 (output stable)	1.493e-04			
S0 (output stable)	4.785e-03			
D0 to Z	7.037e-03			
D1 to Z	7.014e-03			
S0 to Z	9.619e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X1_P4	X2_P4	X6_P4	X9_P4
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

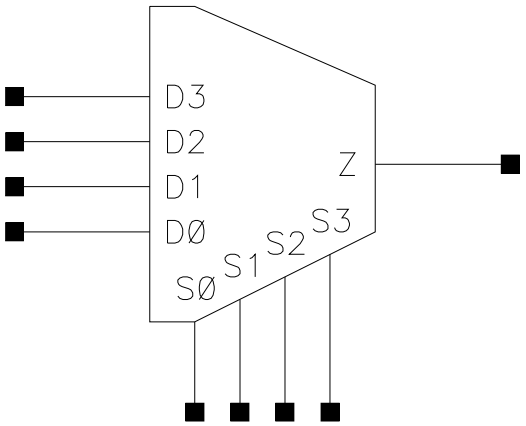
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P4			
D0 (output stable)	0.000e+00			
D1 (output stable)	0.000e+00			
S0 (output stable)	0.000e+00			
D0 to Z	0.000e+00			
D1 to Z	0.000e+00			
S0 to Z	0.000e+00			

MX41

Cell Description

4:1 non-inverting Multiplexer with individual selects

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.600	0.952	1.5232
X15_P4	1.600	2.312	3.6992

Truth Table

D0	D1	D2	D3	S0	S1	S2	S3	Z
0	0	0	0	-	-	-	-	0
0	0	0	-	-	-	-	0	0
-	0	0	0	0	-	-	-	0
0	0	-	-	-	-	0	0	0
0	-	0	-	-	0	-	0	0
-	0	0	-	0	-	-	0	0
-	0	-	0	0	-	0	-	0
0	-	0	0	-	0	-	-	0
0	-	-	0	-	0	0	-	0
0	-	-	-	-	0	0	0	0
-	-	-	0	0	0	0	-	0
-	0	-	-	0	-	0	0	0
0	0	-	0	-	-	0	-	0
-	-	-	-	0	0	0	0	0
-	-	0	-	0	0	-	0	0
-	-	0	0	0	0	-	-	0
0	0	-	1	-	-	-	1	1
-	0	-	1	-	-	0	1	1
-	1	0	-	-	1	-	-	1
1	-	-	-	1	1	1	-	1

-	-	0	1	-	0	-	1	1
-	1	-	-	-	1	0	-	1
1	-	-	-	1	-	-	0	1
1	D1	-	D1	1	-	-	-	1
-	-	1	-	-	-	1	0	1
0	-	1	-	-	-	1	-	1
-	-	1	0	0	-	1	-	1
-	1	1	-	0	-	1	-	1
-	0	-	1	0	-	-	1	1
-	0	-	1	-	0	-	1	1
-	-	1	1	-	-	0	1	1
-	1	-	-	-	1	-	0	1

Pin Capacitance

Pin	X4_P4	X15_P4
D0	0.0006	0.0015
D1	0.0006	0.0012
D2	0.0006	0.0015
D3	0.0006	0.0013
S0	0.0006	0.0013
S1	0.0006	0.0015
S2	0.0006	0.0013
S3	0.0006	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X15_P4	X4_P4	X15_P4
D0 to Z ↓	0.0272	0.0292	4.2558	1.1202
D0 to Z ↑	0.0242	0.0235	3.3217	0.8430
D1 to Z ↓	0.0264	0.0280	4.2526	1.1192
D1 to Z ↑	0.0205	0.0202	3.3040	0.8381
D2 to Z ↓	0.0269	0.0289	4.2572	1.1203
D2 to Z ↑	0.0236	0.0225	3.3342	0.8467
D3 to Z ↓	0.0258	0.0278	4.2514	1.1183
D3 to Z ↑	0.0200	0.0193	3.3170	0.8415
S0 to Z ↓	0.0257	0.0266	4.2539	1.1191
S0 to Z ↑	0.0265	0.0249	3.3189	0.8420
S1 to Z ↓	0.0246	0.0258	4.2510	1.1178
S1 to Z ↑	0.0225	0.0215	3.3013	0.8372
S2 to Z ↓	0.0258	0.0265	4.2565	1.1186
S2 to Z ↑	0.0259	0.0240	3.3341	0.8463
S3 to Z ↓	0.0250	0.0254	4.2513	1.1168
S3 to Z ↑	0.0222	0.0205	3.3172	0.8407

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	2.024e-04	1.000e-20
X15_P4	5.863e-04	1.000e-20

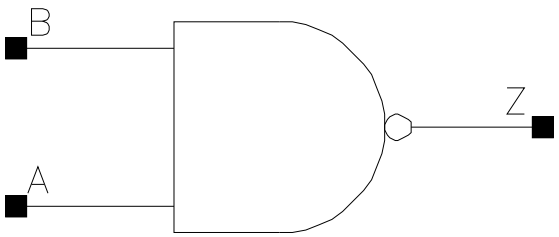
Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X15_P4
D0 (output stable)	5.350e-04	1.459e-03
D1 (output stable)	4.725e-04	1.267e-03
D2 (output stable)	5.237e-04	1.408e-03
D3 (output stable)	4.638e-04	1.220e-03
S0 (output stable)	5.105e-04	1.405e-03
S1 (output stable)	4.524e-04	1.243e-03
S2 (output stable)	5.079e-04	1.370e-03
S3 (output stable)	4.485e-04	1.205e-03
D0 to Z	4.129e-03	1.233e-02
D1 to Z	3.627e-03	1.094e-02
D2 to Z	3.878e-03	1.139e-02
D3 to Z	3.398e-03	1.004e-02
S0 to Z	3.991e-03	1.170e-02
S1 to Z	3.499e-03	1.040e-02
S2 to Z	3.769e-03	1.082e-02
S3 to Z	3.296e-03	9.460e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X4_P4	X15_P4
D0 (output stable)	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00
S2 (output stable)	0.000e+00	0.000e+00
S3 (output stable)	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00
S2 to Z	0.000e+00	0.000e+00
S3 to Z	0.000e+00	0.000e+00

NAND2

Cell Description	Logical Symbol
2 input NAND	

Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND2X2_P4	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X4_P4	0.800	0.408	0.3264
C8T28SOI_LL_NAND2X8_P4	0.800	0.680	0.5440
C8T28SOI_LL_NAND2X12_P4	0.800	0.952	0.7616
C8T28SOI_LL_NAND2X15_P4	0.800	1.224	0.9792
C8T28SOI_LL_NAND2X19_P4	0.800	1.496	1.1968
C8T28SOI_LL_NAND2X24_P4	0.800	1.360	1.0880
C8T28SOI_LLBR0P8_NAND2X4_P4	0.800	0.952	0.7616
C8T28SOI_LLBR0P8_NAND2X8_P4	0.800	1.224	0.9792
C8T28SOI_LLBR0P8_NAND2X12_P4	0.800	1.496	1.1968
C8T28SOI_LLBR0P8_NAND2X16_P4	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X8_P4	0.800	0.680	0.5440
C8T28SOI_LLS_NAND2X15_P4	0.800	1.224	0.9792
C8T28SOI_LLS_NAND2X23_P4	0.800	1.768	1.4144
C8T28SOI_LLS_NAND2X31_P4	0.800	2.312	1.8496
C8T28SOIDV_LL_NAND2X9_P4	1.600	0.408	0.6528

C8T28SOIDV_LL_-NAND2X18_P4	1.600	0.680	1.0880
C8T28SOIDV_LL_-NAND2X27_P4	1.600	0.952	1.5232
C8T28SOIDV_LL_-NAND2X36_P4	1.600	1.224	1.9584

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND2X2_P4	C8T28SOI_LL_-NAND2X4_P4	C8T28SOI_LL_-NAND2X8_P4	C8T28SOI_LL_-NAND2X12_P4
A	0.0004	0.0006	0.0012	0.0017
B	0.0004	0.0006	0.0011	0.0016
	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X24_P4	C8T28SOI_-LLBR0P8_-NAND2X4_P4
A	0.0023	0.0029	0.0007	0.0007
B	0.0022	0.0027	0.0007	0.0006
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	C8T28SOI_-LLBR0P8_-NAND2X12_P4	C8T28SOI_-LLBR0P8_-NAND2X16_P4	C8T28SOI_LLS_-NAND2X8_P4
A	0.0012	0.0018	0.0024	0.0012
B	0.0011	0.0016	0.0021	0.0011
	C8T28SOI_LLS_-NAND2X15_P4	C8T28SOI_LLS_-NAND2X23_P4	C8T28SOI_LLS_-NAND2X31_P4	C8T28SOIDV_LL_-NAND2X9_P4
A	0.0024	0.0036	0.0048	0.0012
B	0.0022	0.0034	0.0045	0.0013
	C8T28SOIDV_LL_-NAND2X18_P4	C8T28SOIDV_LL_-NAND2X27_P4	C8T28SOIDV_LL_-NAND2X36_P4	
A	0.0024	0.0037	0.0049	
B	0.0023	0.0035	0.0047	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-NAND2X2_P4	**C8T28SOI_LL_-NAND2X4_P4**	**C8T28SOI_LL_-NAND2X2_P4**	**C8T28SOI_LL_-NAND2X4_P4**
A to Z ↓	0.0063	0.0056	7.6432	4.3023
A to Z ↑	0.0106	0.0089	6.5231	3.6075
B to Z ↓	0.0079	0.0070	7.7357	4.3513
B to Z ↑	0.0095	0.0075	6.5605	3.6695
	C8T28SOI_LL_-NAND2X8_P4	**C8T28SOI_LL_-NAND2X12_P4**	**C8T28SOI_LL_-NAND2X8_P4**	**C8T28SOI_LL_-NAND2X12_P4**
A to Z ↓	0.0062	0.0059	2.1941	1.5012
A to Z ↑	0.0089	0.0087	1.7273	1.1805
B to Z ↓	0.0067	0.0071	2.2172	1.5188
B to Z ↑	0.0064	0.0067	1.7444	1.1995

	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4
A to Z ↓	0.0060	0.0060	1.1388	0.9194
A to Z ↑	0.0086	0.0087	0.8904	0.7218
B to Z ↓	0.0068	0.0071	1.1523	0.9311
B to Z ↑	0.0063	0.0066	0.9032	0.7335
	C8T28SOI_LL_-NAND2X24_P4	**C8T28SOI_-LLBR0P8_-NAND2X4_P4**	**C8T28SOI_LL_-NAND2X24_P4**	**C8T28SOI_-LLBR0P8_-NAND2X4_P4**
A to Z ↓	0.0252	0.0035	0.5433	3.0946
A to Z ↑	0.0261	0.0122	0.6993	4.4813
B to Z ↓	0.0267	0.0042	0.5432	3.1512
B to Z ↑	0.0248	0.0102	0.7002	4.5010
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	**C8T28SOI_-LLBR0P8_-NAND2X12_P4**	**C8T28SOI_-LLBR0P8_-NAND2X8_P4**	**C8T28SOI_-LLBR0P8_-NAND2X12_P4**
A to Z ↓	0.0038	0.0038	1.7087	1.1669
A to Z ↑	0.0121	0.0122	2.2624	1.5366
B to Z ↓	0.0038	0.0043	1.7390	1.1889
B to Z ↑	0.0089	0.0093	2.2817	1.5465
	C8T28SOI_-LLBR0P8_-NAND2X16_P4	**C8T28SOI_LLS_-NAND2X8_P4**	**C8T28SOI_-LLBR0P8_-NAND2X16_P4**	**C8T28SOI_LLS_-NAND2X8_P4**
A to Z ↓	0.0036	0.0062	0.8918	2.1890
A to Z ↑	0.0117	0.0090	1.1498	1.7505
B to Z ↓	0.0038	0.0067	0.9084	2.2120
B to Z ↑	0.0086	0.0066	1.1623	1.7816
	C8T28SOI_LLS_-NAND2X15_P4	**C8T28SOI_LLS_-NAND2X23_P4**	**C8T28SOI_LLS_-NAND2X15_P4**	**C8T28SOI_LLS_-NAND2X23_P4**
A to Z ↓	0.0061	0.0061	1.1361	0.7666
A to Z ↑	0.0086	0.0085	0.8751	0.5841
B to Z ↓	0.0069	0.0071	1.1494	0.7757
B to Z ↑	0.0063	0.0063	0.8837	0.5898
	C8T28SOI_LLS_-NAND2X31_P4	**C8T28SOIDV_LL_-NAND2X9_P4**	**C8T28SOI_LLS_-NAND2X31_P4**	**C8T28SOIDV_LL_-NAND2X9_P4**
A to Z ↓	0.0061	0.0051	0.5805	1.7094
A to Z ↑	0.0085	0.0096	0.4399	1.6783
B to Z ↓	0.0072	0.0061	0.5874	1.7323
B to Z ↑	0.0064	0.0079	0.4441	1.7145
	C8T28SOIDV_LL_-NAND2X18_P4	**C8T28SOIDV_LL_-NAND2X27_P4**	**C8T28SOIDV_LL_-NAND2X18_P4**	**C8T28SOIDV_LL_-NAND2X27_P4**
A to Z ↓	0.0053	0.0054	0.8730	0.5938
A to Z ↑	0.0098	0.0098	0.8452	0.5715
B to Z ↓	0.0057	0.0063	0.8835	0.6020
B to Z ↑	0.0073	0.0076	0.8530	0.5766
	C8T28SOIDV_LL_-NAND2X36_P4		**C8T28SOIDV_LL_-NAND2X36_P4**	
A to Z ↓	0.0053		0.4475	
A to Z ↑	0.0097		0.4280	
B to Z ↓	0.0059		0.4535	
B to Z ↑	0.0071		0.4323	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_NAND2X2_P4	2.468e-05	1.000e-20
C8T28SOI_LL_NAND2X4_P4	5.498e-05	1.000e-20
C8T28SOI_LL_NAND2X8_P4	1.118e-04	1.000e-20
C8T28SOI_LL_NAND2X12_P4	1.621e-04	1.000e-20
C8T28SOI_LL_NAND2X15_P4	2.125e-04	1.000e-20
C8T28SOI_LL_NAND2X19_P4	2.630e-04	1.000e-20
C8T28SOI_LL_NAND2X24_P4	3.855e-04	1.000e-20
C8T28SOI_LLBR0P8_NAND2X4_P4	5.039e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X8_P4	9.220e-05	1.000e-20
C8T28SOI_LLBR0P8_NAND2X12_P4	1.323e-04	1.000e-20
C8T28SOI_LLBR0P8_NAND2X16_P4	1.726e-04	1.000e-20
C8T28SOI_LLS_NAND2X8_P4	1.118e-04	1.000e-20
C8T28SOI_LLS_NAND2X15_P4	2.126e-04	1.000e-20
C8T28SOI_LLS_NAND2X23_P4	3.134e-04	1.000e-20
C8T28SOI_LLS_NAND2X31_P4	4.143e-04	1.000e-20
C8T28SOIDV_LL_NAND2X9_P4	1.272e-04	1.000e-20
C8T28SOIDV_LL_NAND2X18_P4	2.458e-04	1.000e-20
C8T28SOIDV_LL_NAND2X27_P4	3.595e-04	1.000e-20
C8T28SOIDV_LL_NAND2X36_P4	4.734e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND2X2_P4	C8T28SOI_LL_-NAND2X4_P4	C8T28SOI_LL_-NAND2X8_P4	C8T28SOI_LL_-NAND2X12_P4
A (output stable)	9.031e-06	1.536e-05	7.028e-05	8.539e-05
B (output stable)	1.659e-05	3.041e-05	2.013e-04	2.095e-04
A to Z	8.790e-04	1.472e-03	3.065e-03	4.501e-03
B to Z	7.891e-04	1.292e-03	2.601e-03	3.887e-03
	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X24_P4	C8T28SOI_-LLBR0P8_-NAND2X4_P4
A (output stable)	1.305e-04	1.410e-04	1.905e-05	2.278e-05
B (output stable)	3.480e-04	3.288e-04	3.550e-05	4.203e-05
A to Z	5.973e-03	7.412e-03	1.083e-02	1.540e-03
B to Z	5.070e-03	6.373e-03	1.069e-02	1.350e-03
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	C8T28SOI_-LLBR0P8_-NAND2X12_P4	C8T28SOI_-LLBR0P8_-NAND2X16_P4	C8T28SOI_LLS_-NAND2X8_P4
A (output stable)	8.429e-05	1.012e-04	1.600e-04	7.120e-05
B (output stable)	2.421e-04	2.497e-04	4.169e-04	2.097e-04
A to Z	3.037e-03	4.519e-03	5.815e-03	3.071e-03
B to Z	2.449e-03	3.754e-03	4.714e-03	2.602e-03
	C8T28SOI_LLS_-NAND2X15_P4	C8T28SOI_LLS_-NAND2X23_P4	C8T28SOI_LLS_-NAND2X31_P4	C8T28SOIDV_LL_-NAND2X9_P4
A (output stable)	1.353e-04	1.969e-04	2.552e-04	4.060e-05
B (output stable)	3.605e-04	4.857e-04	6.178e-04	7.637e-05
A to Z	6.020e-03	8.979e-03	1.191e-02	3.385e-03
B to Z	5.114e-03	7.638e-03	1.016e-02	2.992e-03
	C8T28SOIDV_LL_-NAND2X18_P4	C8T28SOIDV_LL_-NAND2X27_P4	C8T28SOIDV_LL_-NAND2X36_P4	
A (output stable)	1.509e-04	1.823e-04	3.051e-04	
B (output stable)	4.808e-04	4.138e-04	9.056e-04	
A to Z	6.776e-03	1.008e-02	1.332e-02	

B to Z	5.732e-03	8.756e-03	1.130e-02	

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

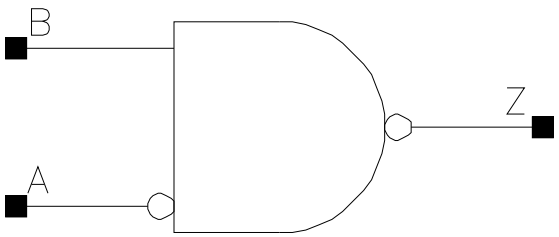
Pin Cycle (vdds)	C8T28SOI_LL_-NAND2X2_P4	C8T28SOI_LL_-NAND2X4_P4	C8T28SOI_LL_-NAND2X8_P4	C8T28SOI_LL_-NAND2X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND2X15_P4	C8T28SOI_LL_-NAND2X19_P4	C8T28SOI_LL_-NAND2X24_P4	C8T28SOI_-LLBR0P8_-NAND2X4_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P8_-NAND2X8_P4	C8T28SOI_-LLBR0P8_-NAND2X12_P4	C8T28SOI_-LLBR0P8_-NAND2X16_P4	C8T28SOI_LLS_-NAND2X8_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLS_-NAND2X15_P4	C8T28SOI_LLS_-NAND2X23_P4	C8T28SOI_LLS_-NAND2X31_P4	C8T28SOIDV_LL_-NAND2X9_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-NAND2X18_P4	C8T28SOIDV_LL_-NAND2X27_P4	C8T28SOIDV_LL_-NAND2X36_P4	
A (output stable)	0.000e+00	0.000e+00	0.000e+00	
B (output stable)	0.000e+00	0.000e+00	0.000e+00	
A to Z	0.000e+00	0.000e+00	0.000e+00	
B to Z	0.000e+00	0.000e+00	0.000e+00	

NAND2A

Cell Description

2 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.544	0.4352
X4_P4	0.800	0.680	0.5440
X9_P4	1.600	0.544	0.8704
X13_P4	1.600	0.816	1.3056
X17_P4	1.600	0.816	1.3056
X23_P4	0.800	2.312	1.8496
X27_P4	1.600	1.088	1.7408
X31_P4	0.800	2.992	2.3936
X36_P4	1.600	1.360	2.1760

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X2_P4	X4_P4	X9_P4	X13_P4
A	0.0006	0.0006	0.0010	0.0009
B	0.0004	0.0006	0.0012	0.0019
	X17_P4	X23_P4	X27_P4	X31_P4
A	0.0009	0.0020	0.0016	0.0027
B	0.0023	0.0033	0.0035	0.0043
	X36_P4			
A	0.0015			
B	0.0047			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X4_P4**	**X2_P4**	**X4_P4**
A to Z ↓	0.0183	0.0190	7.6006	4.3197
A to Z ↑	0.0139	0.0143	6.2976	3.4676
B to Z ↓	0.0081	0.0071	7.8127	4.4358
B to Z ↑	0.0095	0.0074	6.5656	3.6676
	X9_P4	**X13_P4**	**X9_P4**	**X13_P4**
A to Z ↓	0.0194	0.0233	1.7320	1.0925
A to Z ↑	0.0141	0.0174	1.6412	1.0844
B to Z ↓	0.0063	0.0061	1.7893	1.1308
B to Z ↑	0.0079	0.0082	1.7255	1.1570
	X17_P4	**X23_P4**	**X17_P4**	**X23_P4**
A to Z ↓	0.0255	0.0184	0.8629	0.7589
A to Z ↑	0.0183	0.0149	0.8393	0.5776
B to Z ↓	0.0060	0.0069	0.8912	0.7805
B to Z ↑	0.0077	0.0063	0.9003	0.6077
	X27_P4	**X31_P4**	**X27_P4**	**X31_P4**
A to Z ↓	0.0215	0.0184	0.5850	0.5739
A to Z ↑	0.0165	0.0148	0.5612	0.4208
B to Z ↓	0.0060	0.0072	0.6048	0.5898
B to Z ↑	0.0073	0.0065	0.5796	0.4569
	X36_P4		**X36_P4**	
A to Z ↓	0.0245		0.4413	
A to Z ↑	0.0189		0.4204	
B to Z ↓	0.0059		0.4551	
B to Z ↑	0.0071		0.4352	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P4	4.658e-05	1.000e-20
X4_P4	8.006e-05	1.000e-20
X9_P4	1.908e-04	1.000e-20
X13_P4	2.307e-04	1.000e-20
X17_P4	2.967e-04	1.000e-20
X23_P4	4.746e-04	1.000e-20
X27_P4	4.803e-04	1.000e-20
X31_P4	6.250e-04	1.000e-20
X36_P4	5.975e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P4	X4_P4	X9_P4	X13_P4
A (output stable)	1.167e-03	1.386e-03	2.686e-03	3.531e-03
B (output stable)	1.651e-05	3.085e-05	8.025e-05	2.221e-04
A to Z	1.793e-03	2.394e-03	5.067e-03	7.789e-03
B to Z	7.851e-04	1.284e-03	2.990e-03	4.519e-03
	X17_P4	X23_P4	X27_P4	X31_P4
A (output stable)	3.871e-03	6.973e-03	6.433e-03	9.314e-03
B (output stable)	2.655e-04	4.410e-04	4.151e-04	5.877e-04
A to Z	9.513e-03	1.357e-02	1.390e-02	1.823e-02
B to Z	5.749e-03	7.627e-03	8.545e-03	1.014e-02
	X36_P4			
A (output stable)	7.826e-03			

B (output stable)	6.820e-04			
A to Z	1.856e-02			
B to Z	1.120e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

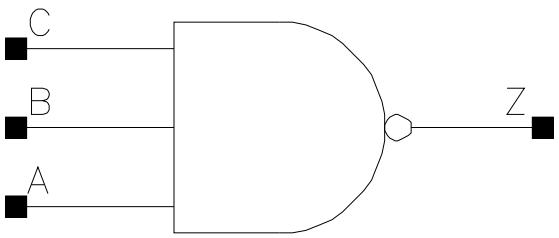
Pin Cycle (vdds)	X2_P4	X4_P4	X9_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P4	X23_P4	X27_P4	X31_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X36_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			

NAND3

Cell Description

3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_NAND3X3_P4	0.800	0.544	0.4352
C8T28SOI_LL_NAND3X7_P4	0.800	1.088	0.8704
C8T28SOI_LL_NAND3X10_P4	0.800	1.360	1.0880
C8T28SOI_LL_NAND3X14_P4	0.800	1.904	1.5232
C8T28SOI_LL_NAND3X20_P4	0.800	2.720	2.1760
C8T28SOI_LL_NAND3X27_P4	0.800	3.536	2.8288
C8T28SOI_LLBR0P6_NAND3X3_P4	0.800	1.088	0.8704
C8T28SOI_LLBR0P6_NAND3X7_P4	0.800	1.632	1.3056
C8T28SOI_LLBR0P6_NAND3X10_P4	0.800	1.904	1.5232
C8T28SOI_LLBR0P6_NAND3X14_P4	0.800	2.448	1.9584
C8T28SOI_LLBR0P6_NAND3X20_P4	0.800	3.264	2.6112
C8T28SOI_LLBR0P6_NAND3X27_P4	0.800	4.080	3.2640

Truth Table

A	B	C	Z
1	1	1	0
-	0	-	1
-	-	0	1
0	-	-	1

Pin Capacitance

Pin	C8T28SOI_LL_-NAND3X3_P4	C8T28SOI_LL_-NAND3X7_P4	C8T28SOI_LL_-NAND3X10_P4	C8T28SOI_LL_-NAND3X14_P4
A	0.0006	0.0012	0.0018	0.0023
B	0.0006	0.0011	0.0017	0.0022
C	0.0006	0.0011	0.0016	0.0021
	C8T28SOI_LL_-NAND3X20_P4	C8T28SOI_LL_-NAND3X27_P4	C8T28SOI_-LLBR0P6_-NAND3X3_P4	C8T28SOI_-LLBR0P6_-NAND3X7_P4
A	0.0034	0.0047	0.0007	0.0012
B	0.0033	0.0045	0.0006	0.0011
C	0.0031	0.0043	0.0006	0.0010
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	C8T28SOI_-LLBR0P6_-NAND3X14_P4	C8T28SOI_-LLBR0P6_-NAND3X20_P4	C8T28SOI_-LLBR0P6_-NAND3X27_P4
A	0.0017	0.0024	0.0035	0.0047
B	0.0016	0.0021	0.0032	0.0043
C	0.0016	0.0021	0.0032	0.0042

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-NAND3X3_P4	**C8T28SOI_LL_-NAND3X7_P4**	**C8T28SOI_LL_-NAND3X3_P4**	**C8T28SOI_LL_-NAND3X7_P4**
A to Z ↓	0.0088	0.0097	6.0258	3.0832
A to Z ↑	0.0108	0.0112	3.6543	1.7998
B to Z ↓	0.0100	0.0104	6.0559	3.0958
B to Z ↑	0.0098	0.0099	3.6809	1.8055
C to Z ↓	0.0109	0.0107	6.0956	3.1085
C to Z ↑	0.0085	0.0077	3.7254	1.7499
	C8T28SOI_LL_-NAND3X10_P4	**C8T28SOI_LL_-NAND3X14_P4**	**C8T28SOI_LL_-NAND3X10_P4**	**C8T28SOI_LL_-NAND3X14_P4**
A to Z ↓	0.0092	0.0094	2.1159	1.6061
A to Z ↑	0.0104	0.0107	1.1593	0.9091
B to Z ↓	0.0103	0.0103	2.1271	1.6129
B to Z ↑	0.0092	0.0094	1.2007	0.9100
C to Z ↓	0.0106	0.0106	2.1368	1.6207
C to Z ↑	0.0074	0.0073	1.2113	0.9031
	C8T28SOI_LL_-NAND3X20_P4	**C8T28SOI_LL_-NAND3X27_P4**	**C8T28SOI_LL_-NAND3X20_P4**	**C8T28SOI_LL_-NAND3X27_P4**
A to Z ↓	0.0091	0.0093	1.0916	0.8309
A to Z ↑	0.0103	0.0103	0.5856	0.4425
B to Z ↓	0.0104	0.0104	1.0971	0.8348
B to Z ↑	0.0090	0.0090	0.5864	0.4417
C to Z ↓	0.0107	0.0108	1.1025	0.8392
C to Z ↑	0.0071	0.0071	0.6049	0.4559
	C8T28SOI_-LLBR0P6_-NAND3X3_P4	**C8T28SOI_-LLBR0P6_-NAND3X7_P4**	**C8T28SOI_-LLBR0P6_-NAND3X3_P4**	**C8T28SOI_-LLBR0P6_-NAND3X7_P4**
A to Z ↓	0.0048	0.0064	3.8734	2.2025
A to Z ↑	0.0163	0.0173	5.2200	2.6689
B to Z ↓	0.0053	0.0064	3.9224	2.2240
B to Z ↑	0.0143	0.0150	5.2142	2.6778

C to Z ↓	0.0055	0.0059	3.9803	2.2492
C to Z ↑	0.0119	0.0117	5.2630	2.6509
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	**C8T28SOI_-LLBR0P6_-NAND3X14_P4**	**C8T28SOI_-LLBR0P6_-NAND3X10_P4**	**C8T28SOI_-LLBR0P6_-NAND3X14_P4**
A to Z ↓	0.0055	0.0060	1.4605	1.1158
A to Z ↑	0.0164	0.0168	1.7820	1.3529
B to Z ↓	0.0057	0.0058	1.4766	1.1272
B to Z ↑	0.0140	0.0144	1.7902	1.3552
C to Z ↓	0.0055	0.0053	1.4957	1.1419
C to Z ↑	0.0110	0.0109	1.8043	1.3528
	C8T28SOI_-LLBR0P6_-NAND3X20_P4	**C8T28SOI_-LLBR0P6_-NAND3X27_P4**	**C8T28SOI_-LLBR0P6_-NAND3X20_P4**	**C8T28SOI_-LLBR0P6_-NAND3X27_P4**
A to Z ↓	0.0056	0.0057	0.7531	0.5782
A to Z ↑	0.0164	0.0164	0.9011	0.6809
B to Z ↓	0.0058	0.0058	0.7614	0.5844
B to Z ↑	0.0142	0.0140	0.9017	0.6795
C to Z ↓	0.0053	0.0054	0.7713	0.5919
C to Z ↑	0.0106	0.0106	0.9083	0.6839

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_NAND3X3_P4	4.252e-05	1.000e-20
C8T28SOI_LL_NAND3X7_P4	8.826e-05	1.000e-20
C8T28SOI_LL_NAND3X10_P4	1.250e-04	1.000e-20
C8T28SOI_LL_NAND3X14_P4	1.667e-04	1.000e-20
C8T28SOI_LL_NAND3X20_P4	2.452e-04	1.000e-20
C8T28SOI_LL_NAND3X27_P4	3.236e-04	1.000e-20
C8T28SOI_LLBR0P6_NAND3X3_P4	3.680e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X7_P4	7.022e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X10_P4	9.597e-05	1.000e-20
C8T28SOI_LLBR0P6_NAND3X14_P4	1.292e-04	1.000e-20
C8T28SOI_LLBR0P6_NAND3X20_P4	1.881e-04	1.000e-20
C8T28SOI_LLBR0P6_NAND3X27_P4	2.470e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOI_LL_-NAND3X3_P4	C8T28SOI_LL_-NAND3X7_P4	C8T28SOI_LL_-NAND3X10_P4	C8T28SOI_LL_-NAND3X14_P4
A (output stable)	1.853e-05	7.227e-05	9.254e-05	1.355e-04
B (output stable)	2.822e-05	1.079e-04	1.435e-04	1.955e-04
C (output stable)	6.063e-05	2.586e-04	3.184e-04	4.691e-04
A to Z	1.727e-03	3.688e-03	5.277e-03	7.055e-03
B to Z	1.556e-03	3.232e-03	4.576e-03	6.171e-03
C to Z	1.400e-03	2.838e-03	4.030e-03	5.417e-03
	C8T28SOI_LL_-NAND3X20_P4	C8T28SOI_LL_-NAND3X27_P4	C8T28SOI_-LLBR0P6_-NAND3X3_P4	C8T28SOI_-LLBR0P6_-NAND3X7_P4
A (output stable)	1.842e-04	2.483e-04	2.996e-05	9.624e-05
B (output stable)	2.841e-04	3.712e-04	4.228e-05	1.387e-04
C (output stable)	6.962e-04	9.009e-04	9.452e-05	3.442e-04

A to Z	1.044e-02	1.384e-02	1.783e-03	3.830e-03
B to Z	9.104e-03	1.206e-02	1.547e-03	3.181e-03
C to Z	7.866e-03	1.045e-02	1.319e-03	2.585e-03
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	C8T28SOI_-LLBR0P6_-NAND3X14_P4	C8T28SOI_-LLBR0P6_-NAND3X20_P4	C8T28SOI_-LLBR0P6_-NAND3X27_P4
A (output stable)	1.233e-04	1.964e-04	2.565e-04	3.460e-04
B (output stable)	1.815e-04	2.769e-04	3.797e-04	4.984e-04
C (output stable)	4.318e-04	6.484e-04	9.436e-04	1.218e-03
A to Z	5.348e-03	7.288e-03	1.068e-02	1.410e-02
B to Z	4.375e-03	5.962e-03	8.720e-03	1.150e-02
C to Z	3.612e-03	4.793e-03	6.964e-03	9.221e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

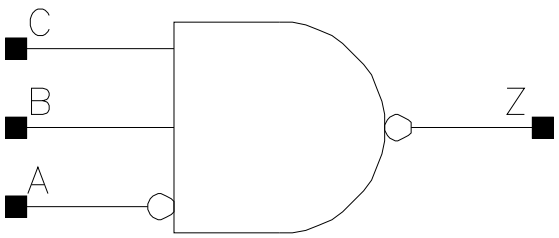
Pin Cycle (vdds)	C8T28SOI_LL_-NAND3X3_P4	C8T28SOI_LL_-NAND3X7_P4	C8T28SOI_LL_-NAND3X10_P4	C8T28SOI_LL_-NAND3X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-NAND3X20_P4	C8T28SOI_LL_-NAND3X27_P4	C8T28SOI_-LLBR0P6_-NAND3X3_P4	C8T28SOI_-LLBR0P6_-NAND3X7_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_-LLBR0P6_-NAND3X10_P4	C8T28SOI_-LLBR0P6_-NAND3X14_P4	C8T28SOI_-LLBR0P6_-NAND3X20_P4	C8T28SOI_-LLBR0P6_-NAND3X27_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3A

Cell Description

3 input NAND with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X7_P4	0.800	1.360	1.0880
X10_P4	0.800	1.632	1.3056
X14_P4	0.800	2.176	1.7408

Truth Table

A	B	C	Z
0	1	1	0
-	0	-	1
1	-	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X10_P4	X14_P4
A	0.0007	0.0010	0.0008	0.0008
B	0.0006	0.0011	0.0017	0.0022
C	0.0006	0.0011	0.0016	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0227	0.0225	6.0279	3.0902
A to Z ↑	0.0161	0.0170	3.4722	1.6821
B to Z ↓	0.0098	0.0103	6.0916	3.1200
B to Z ↑	0.0095	0.0094	3.6867	1.7543
C to Z ↓	0.0105	0.0103	6.1322	3.1318
C to Z ↑	0.0081	0.0072	3.7292	1.7538
	X10_P4	**X14_P4**	**X10_P4**	**X14_P4**
A to Z ↓	0.0250	0.0271	2.1060	1.6078

A to Z ↑	0.0192	0.0212	1.1523	0.8630
B to Z ↓	0.0103	0.0101	2.1255	1.6223
B to Z ↑	0.0092	0.0090	1.2022	0.8994
C to Z ↓	0.0106	0.0103	2.1345	1.6297
C to Z ↑	0.0074	0.0069	1.2142	0.9041

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	6.443e-05	1.000e-20
X7_P4	1.432e-04	1.000e-20
X10_P4	1.827e-04	1.000e-20
X14_P4	2.246e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	1.360e-03	2.547e-03	3.074e-03	3.603e-03
B (output stable)	2.875e-05	9.162e-05	1.463e-04	1.799e-04
C (output stable)	6.076e-05	2.703e-04	3.283e-04	4.601e-04
A to Z	2.680e-03	5.553e-03	7.661e-03	9.843e-03
B to Z	1.505e-03	3.150e-03	4.570e-03	6.029e-03
C to Z	1.351e-03	2.716e-03	4.024e-03	5.245e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

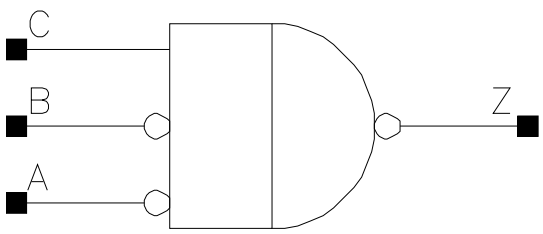
Pin Cycle (vdds)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND3AB

Cell Description

3 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	0.816	0.6528
X8_P4	0.800	1.088	0.8704
X12_P4	0.800	1.632	1.3056
X15_P4	0.800	1.904	1.5232

Truth Table

A	B	C	Z
0	0	1	0
-	-	0	1
1	-	-	1
-	1	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X12_P4	X15_P4
A	0.0007	0.0007	0.0013	0.0012
B	0.0008	0.0007	0.0013	0.0013
C	0.0006	0.0011	0.0016	0.0022

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	**X8_P4**	**X4_P4**	**X8_P4**
A to Z ↓	0.0200	0.0244	4.0635	2.1671
A to Z ↑	0.0139	0.0165	3.3258	1.6616
B to Z ↓	0.0214	0.0261	4.0625	2.1674
B to Z ↑	0.0128	0.0155	3.3238	1.6622
C to Z ↓	0.0072	0.0068	4.1613	2.2141
C to Z ↑	0.0075	0.0066	3.3990	1.7612
	X12_P4	**X15_P4**	**X12_P4**	**X15_P4**
A to Z ↓	0.0222	0.0242	1.4802	1.1277
A to Z ↑	0.0151	0.0184	1.1090	0.8364
B to Z ↓	0.0229	0.0250	1.4797	1.1270

B to Z ↑	0.0134	0.0166	1.1086	0.8353
C to Z ↓	0.0074	0.0069	1.5140	1.1548
C to Z ↑	0.0070	0.0062	1.1968	0.8817

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	1.028e-04	1.000e-20
X8_P4	1.363e-04	1.000e-20
X12_P4	2.203e-04	1.000e-20
X15_P4	2.491e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	7.448e-04	9.369e-04	1.604e-03	1.760e-03
B (output stable)	6.924e-04	8.836e-04	1.518e-03	1.669e-03
C (output stable)	3.359e-05	2.016e-04	2.153e-04	3.361e-04
A to Z	3.312e-03	5.291e-03	8.309e-03	1.016e-02
B to Z	3.119e-03	5.099e-03	7.703e-03	9.532e-03
C to Z	1.416e-03	2.629e-03	4.021e-03	5.129e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

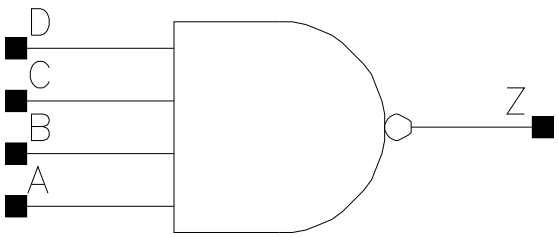
Pin Cycle (vdds)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4

Cell Description

4 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.224	0.9792
X10_P4	0.800	1.360	1.0880
X14_P4	0.800	1.904	1.5232
X18_P4	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
1	1	1	1	0
-	-	0	-	1
-	0	-	-	1
0	-	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X18_P4
A	0.0005	0.0005	0.0006	0.0006
B	0.0005	0.0005	0.0006	0.0008
C	0.0004	0.0004	0.0006	0.0007
D	0.0005	0.0005	0.0006	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0312	0.0298	2.6019	1.3137
A to Z ↑	0.0272	0.0282	3.3620	1.7129
B to Z ↓	0.0331	0.0320	2.6032	1.3137
B to Z ↑	0.0262	0.0275	3.3604	1.7125
C to Z ↓	0.0328	0.0311	2.6042	1.3124
C to Z ↑	0.0284	0.0297	3.3576	1.7099

D to Z ↓	0.0351	0.0334	2.6016	1.3131
D to Z ↑	0.0278	0.0292	3.3610	1.7112
	X14_P4	**X18_P4**	**X14_P4**	**X18_P4**
A to Z ↓	0.0323	0.0306	0.9042	0.7281
A to Z ↑	0.0283	0.0279	1.1746	0.9215
B to Z ↓	0.0344	0.0324	0.9038	0.7279
B to Z ↑	0.0273	0.0271	1.1758	0.9207
C to Z ↓	0.0320	0.0286	0.9030	0.7278
C to Z ↑	0.0284	0.0273	1.1712	0.9193
D to Z ↓	0.0342	0.0305	0.9031	0.7277
D to Z ↑	0.0277	0.0262	1.1720	0.9190

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.006e-04	1.000e-20
X10_P4	1.571e-04	1.000e-20
X14_P4	2.234e-04	1.000e-20
X18_P4	3.054e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	5.452e-04	6.349e-04	9.149e-04	1.035e-03
B (output stable)	5.137e-04	5.982e-04	8.674e-04	9.884e-04
C (output stable)	5.793e-04	6.229e-04	9.172e-04	9.852e-04
D (output stable)	5.414e-04	5.858e-04	8.655e-04	9.276e-04
A to Z	3.842e-03	5.652e-03	8.640e-03	1.025e-02
B to Z	3.760e-03	5.566e-03	8.503e-03	1.012e-02
C to Z	4.032e-03	5.746e-03	8.283e-03	9.647e-03
D to Z	3.956e-03	5.667e-03	8.170e-03	9.498e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

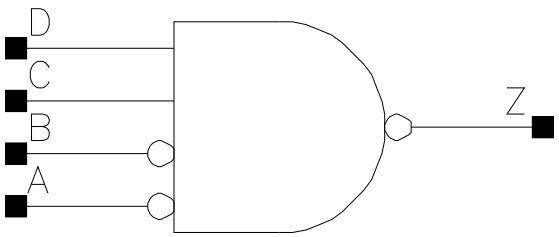
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NAND4AB

Cell Description

4 input NAND with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.952	0.7616
X7_P4	0.800	1.360	1.0880
X10_P4	0.800	2.040	1.6320
X14_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
0	0	1	1	0
1	-	-	-	1
-	-	-	0	1
-	-	0	-	1
-	1	-	-	1

Pin Capacitance

Pin	X3_P4	X7_P4	X10_P4	X14_P4
A	0.0007	0.0007	0.0013	0.0012
B	0.0007	0.0007	0.0014	0.0013
C	0.0007	0.0011	0.0017	0.0022
D	0.0006	0.0011	0.0016	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X7_P4	X3_P4	X7_P4
A to Z ↓	0.0229	0.0267	5.8250	3.0865
A to Z ↑	0.0152	0.0178	3.3642	1.6905
B to Z ↓	0.0240	0.0282	5.8249	3.0866
B to Z ↑	0.0138	0.0166	3.3666	1.6873
C to Z ↓	0.0102	0.0102	5.8886	3.1133
C to Z ↑	0.0098	0.0094	3.5440	1.7568

D to Z ↓	0.0106	0.0102	5.9149	3.1252
D to Z ↑	0.0081	0.0072	3.5404	1.7540
	X10_P4	**X14_P4**	**X10_P4**	**X14_P4**
A to Z ↓	0.0251	0.0270	2.1069	1.6127
A to Z ↑	0.0164	0.0209	1.1421	0.8436
B to Z ↓	0.0257	0.0279	2.1068	1.6123
B to Z ↑	0.0147	0.0193	1.1407	0.8416
C to Z ↓	0.0103	0.0101	2.1231	1.6246
C to Z ↑	0.0093	0.0091	1.2033	0.9010
D to Z ↓	0.0105	0.0104	2.1327	1.6324
D to Z ↑	0.0074	0.0070	1.2146	0.9058

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	9.166e-05	1.000e-20
X7_P4	1.160e-04	1.000e-20
X10_P4	1.933e-04	1.000e-20
X14_P4	2.098e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	9.243e-04	1.154e-03	2.061e-03	2.266e-03
B (output stable)	8.544e-04	1.088e-03	1.909e-03	2.118e-03
C (output stable)	4.893e-05	9.956e-05	1.523e-04	1.961e-04
D (output stable)	1.165e-04	2.902e-04	3.623e-04	5.051e-04
A to Z	3.663e-03	5.794e-03	9.191e-03	1.145e-02
B to Z	3.482e-03	5.632e-03	8.601e-03	1.085e-02
C to Z	1.603e-03	3.141e-03	4.554e-03	6.028e-03
D to Z	1.467e-03	2.707e-03	4.016e-03	5.257e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

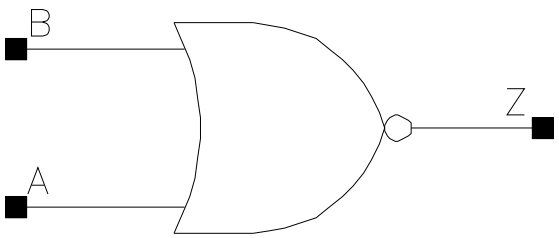
Pin Cycle (vdds)	X3_P4	X7_P4	X10_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR2

Cell Description

2 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.408	0.3264
X4_P4	0.800	0.408	0.3264
X8_P4	0.800	0.680	0.5440
X9_P4	1.600	0.408	0.6528
X12_P4	0.800	0.952	0.7616
X16_P4	0.800	1.224	0.9792
X19_P4	1.600	0.680	1.0880
X20_P4	0.800	1.496	1.1968
X23_P4	0.800	1.496	1.1968
X24_P4	0.800	1.768	1.4144
X27_P4	0.800	1.632	1.3056
X29_P4	1.600	0.952	1.5232
X31_P4	0.800	2.312	1.8496
X34_P4	0.800	2.040	1.6320
X38_P4	0.800	2.176	1.7408
X39_P4	1.600	1.224	1.9584
X46_P4	1.600	1.224	1.9584
X57_P4	1.600	1.360	2.1760

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X2_P4	X4_P4	X8_P4	X9_P4
A	0.0004	0.0006	0.0012	0.0012
B	0.0004	0.0006	0.0011	0.0012
	X12_P4	X16_P4	X19_P4	X20_P4

A	0.0018	0.0023	0.0025	0.0030
B	0.0016	0.0022	0.0023	0.0026
	X23_P4	X24_P4	X27_P4	X29_P4
A	0.0008	0.0035	0.0008	0.0037
B	0.0007	0.0033	0.0007	0.0035
	X31_P4	X34_P4	X38_P4	X39_P4
A	0.0046	0.0008	0.0008	0.0050
B	0.0043	0.0007	0.0007	0.0046
	X46_P4	X57_P4		
A	0.0007	0.0007		
B	0.0008	0.0008		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X4_P4**	**X2_P4**	**X4_P4**
A to Z ↓	0.0055	0.0054	5.0884	2.8377
A to Z ↑	0.0119	0.0108	11.8434	6.6590
B to Z ↓	0.0044	0.0040	5.1291	2.8656
B to Z ↑	0.0133	0.0119	11.9018	6.6935
	X8_P4	**X9_P4**	**X8_P4**	**X9_P4**
A to Z ↓	0.0049	0.0042	1.3710	1.1033
A to Z ↑	0.0097	0.0103	3.1933	3.0187
B to Z ↓	0.0027	0.0030	1.3750	1.1425
B to Z ↑	0.0097	0.0113	3.2066	3.0355
	X12_P4	**X16_P4**	**X12_P4**	**X16_P4**
A to Z ↓	0.0052	0.0051	0.9373	0.6975
A to Z ↑	0.0093	0.0095	2.0923	1.6027
B to Z ↓	0.0032	0.0030	0.9475	0.7056
B to Z ↑	0.0099	0.0098	2.1027	1.6102
	X19_P4	**X20_P4**	**X19_P4**	**X20_P4**
A to Z ↓	0.0047	0.0054	0.5555	0.5721
A to Z ↑	0.0109	0.0094	1.5537	1.2731
B to Z ↓	0.0031	0.0034	0.5615	0.5785
B to Z ↑	0.0113	0.0099	1.5585	1.2797
	X23_P4	**X24_P4**	**X23_P4**	**X24_P4**
A to Z ↓	0.0232	0.0052	0.5689	0.4740
A to Z ↑	0.0306	0.0094	0.6989	1.0749
B to Z ↓	0.0217	0.0031	0.5689	0.4798
B to Z ↑	0.0320	0.0097	0.6996	1.0801
	X27_P4	**X29_P4**	**X27_P4**	**X29_P4**
A to Z ↓	0.0243	0.0044	0.4740	0.3675
A to Z ↑	0.0318	0.0104	0.5839	1.0441
B to Z ↓	0.0229	0.0028	0.4734	0.3713
B to Z ↑	0.0331	0.0111	0.5843	1.0481
	X31_P4	**X34_P4**	**X31_P4**	**X34_P4**
A to Z ↓	0.0053	0.0257	0.3538	0.3895
A to Z ↑	0.0095	0.0357	0.8061	0.4805
B to Z ↓	0.0033	0.0243	0.3583	0.3894
B to Z ↑	0.0099	0.0373	0.8103	0.4815
	X38_P4	**X39_P4**	**X38_P4**	**X39_P4**
A to Z ↓	0.0263	0.0046	0.3391	0.2798
A to Z ↑	0.0362	0.0105	0.4216	0.7841

B to Z ↓	0.0249	0.0028	0.3392	0.2835
B to Z ↑	0.0378	0.0109	0.4220	0.7870
	X46_P4	**X57_P4**	**X46_P4**	**X57_P4**
A to Z ↓	0.0295	0.0318	0.2605	0.2128
A to Z ↑	0.0375	0.0395	0.4177	0.3362
B to Z ↓	0.0282	0.0305	0.2605	0.2127
B to Z ↑	0.0395	0.0415	0.4167	0.3363

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P4	2.493e-05	1.000e-20
X4_P4	5.401e-05	1.000e-20
X8_P4	1.154e-04	1.000e-20
X9_P4	1.300e-04	1.000e-20
X12_P4	1.677e-04	1.000e-20
X16_P4	2.199e-04	1.000e-20
X19_P4	2.518e-04	1.000e-20
X20_P4	2.723e-04	1.000e-20
X23_P4	4.587e-04	1.000e-20
X24_P4	3.246e-04	1.000e-20
X27_P4	5.231e-04	1.000e-20
X29_P4	3.688e-04	1.000e-20
X31_P4	4.292e-04	1.000e-20
X34_P4	6.316e-04	1.000e-20
X38_P4	6.941e-04	1.000e-20
X39_P4	4.859e-04	1.000e-20
X46_P4	7.230e-04	1.000e-20
X57_P4	8.590e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P4	X4_P4	X8_P4	X9_P4
A (output stable)	1.449e-05	2.481e-05	9.271e-05	5.449e-05
B (output stable)	2.533e-05	4.421e-05	2.420e-04	1.009e-04
A to Z	8.608e-04	1.474e-03	2.955e-03	3.221e-03
B to Z	7.585e-04	1.273e-03	2.408e-03	2.786e-03
	X12_P4	X16_P4	X19_P4	X20_P4
A (output stable)	1.292e-04	1.831e-04	1.951e-04	2.171e-04
B (output stable)	2.993e-04	4.553e-04	5.549e-04	4.750e-04
A to Z	4.413e-03	5.853e-03	6.560e-03	7.325e-03
B to Z	3.674e-03	4.810e-03	5.544e-03	6.072e-03
	X23_P4	X24_P4	X27_P4	X29_P4
A (output stable)	2.741e-05	2.671e-04	2.741e-05	2.539e-04
B (output stable)	4.918e-05	6.167e-04	5.000e-05	5.701e-04
A to Z	1.083e-02	8.686e-03	1.240e-02	9.516e-03
B to Z	1.066e-02	7.154e-03	1.224e-02	8.072e-03
	X31_P4	X34_P4	X38_P4	X39_P4
A (output stable)	3.613e-04	2.973e-05	2.941e-05	3.796e-04
B (output stable)	8.267e-04	5.218e-05	5.300e-05	9.278e-04
A to Z	1.161e-02	1.633e-02	1.793e-02	1.269e-02
B to Z	9.599e-03	1.614e-02	1.772e-02	1.067e-02
	X46_P4	X57_P4		

A (output stable)	2.955e-05	3.005e-05		
B (output stable)	5.386e-05	5.418e-05		
A to Z	1.982e-02	2.475e-02		
B to Z	1.965e-02	2.458e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

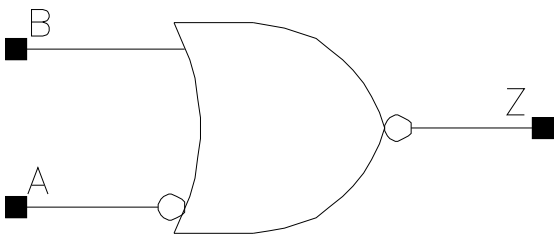
Pin Cycle (vdds)	X2_P4	X4_P4	X8_P4	X9_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X12_P4	X16_P4	X19_P4	X20_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X23_P4	X24_P4	X27_P4	X29_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X31_P4	X34_P4	X38_P4	X39_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X46_P4	X57_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

NOR2A

Cell Description

2 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	0.544	0.4352
X3_P4	0.800	0.544	0.4352
X4_P4	0.800	0.544	0.4352
X10_P4	1.600	0.544	0.8704
X14_P4	1.600	0.816	1.3056
X19_P4	1.600	0.816	1.3056
X29_P4	1.600	1.088	1.7408
X39_P4	1.600	1.360	2.1760

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X2_P4	X3_P4	X4_P4	X10_P4
A	0.0006	0.0006	0.0006	0.0010
B	0.0004	0.0004	0.0005	0.0012
	X14_P4	X19_P4	X29_P4	X39_P4
A	0.0010	0.0010	0.0015	0.0015
B	0.0019	0.0022	0.0035	0.0045

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	X3_P4	X2_P4	X3_P4
A to Z ↓	0.0175	0.0176	4.8433	3.7167
A to Z ↑	0.0154	0.0154	11.7763	10.0757
B to Z ↓	0.0042	0.0033	5.1575	3.9405

B to Z ↑	0.0128	0.0124	11.8943	10.1643
	X4_P4	**X10_P4**	**X4_P4**	**X10_P4**
A to Z ↓	0.0181	0.0187	2.8818	1.0557
A to Z ↑	0.0155	0.0154	7.4531	2.9757
B to Z ↓	0.0033	0.0030	3.0479	1.0902
B to Z ↑	0.0114	0.0115	7.5224	3.0026
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0223	0.0235	0.6639	0.5197
A to Z ↑	0.0182	0.0190	1.9985	1.4975
B to Z ↓	0.0027	0.0027	0.7492	0.5872
B to Z ↑	0.0109	0.0103	2.0211	1.5132
	X29_P4	**X39_P4**	**X29_P4**	**X39_P4**
A to Z ↓	0.0205	0.0234	0.3499	0.2625
A to Z ↑	0.0179	0.0197	1.0429	0.7651
B to Z ↓	0.0027	0.0025	0.3721	0.2903
B to Z ↑	0.0110	0.0102	1.0529	0.7728

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P4	4.764e-05	1.000e-20
X3_P4	5.514e-05	1.000e-20
X4_P4	7.219e-05	1.000e-20
X10_P4	1.962e-04	1.000e-20
X14_P4	2.350e-04	1.000e-20
X19_P4	3.169e-04	1.000e-20
X29_P4	4.898e-04	1.000e-20
X39_P4	6.169e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P4	X3_P4	X4_P4	X10_P4
A (output stable)	1.170e-03	1.238e-03	1.345e-03	2.741e-03
B (output stable)	2.547e-05	2.964e-05	4.111e-05	1.069e-04
A to Z	1.803e-03	1.961e-03	2.252e-03	5.109e-03
B to Z	7.311e-04	8.564e-04	1.091e-03	2.878e-03
	X14_P4	X19_P4	X29_P4	X39_P4
A (output stable)	3.650e-03	3.996e-03	6.481e-03	7.867e-03
B (output stable)	1.603e-04	2.137e-04	5.593e-04	4.103e-04
A to Z	7.409e-03	8.969e-03	1.389e-02	1.786e-02
B to Z	4.060e-03	5.241e-03	8.028e-03	1.029e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X2_P4	X3_P4	X4_P4	X10_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P4	X19_P4	X29_P4	X39_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

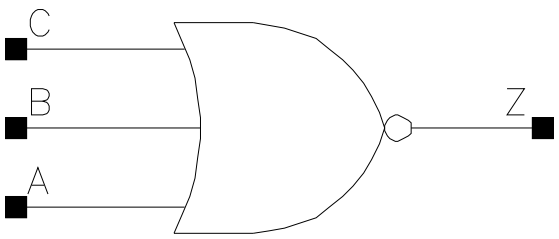
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR3

Cell Description

3 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.544	0.4352
X7_P4	0.800	0.952	0.7616
X11_P4	0.800	1.360	1.0880
X14_P4	0.800	1.768	1.4144
X21_P4	0.800	2.584	2.0672
X29_P4	0.800	3.400	2.7200

Truth Table

A	B	C	Z
1	-	-	0
-	1	-	0
-	-	1	0
0	0	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X11_P4	X14_P4
A	0.0006	0.0010	0.0017	0.0024
B	0.0006	0.0012	0.0016	0.0025
C	0.0006	0.0010	0.0016	0.0021
	X21_P4	X29_P4		
A	0.0037	0.0049		
B	0.0036	0.0048		
C	0.0032	0.0043		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X7_P4	X3_P4	X7_P4
A to Z ↓	0.0062	0.0063	2.8948	1.5055
A to Z ↑	0.0131	0.0131	9.1515	4.7503

B to Z ↓	0.0055	0.0054	2.9181	1.4549
B to Z ↑	0.0139	0.0138	9.1670	4.7638
C to Z ↓	0.0043	0.0032	2.9592	1.4739
C to Z ↑	0.0142	0.0126	9.1906	4.7555
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0062	0.0064	0.9487	0.7261
A to Z ↑	0.0135	0.0129	3.1606	2.2853
B to Z ↓	0.0056	0.0054	0.9567	0.7077
B to Z ↑	0.0136	0.0135	3.1658	2.2906
C to Z ↓	0.0037	0.0035	0.9580	0.7217
C to Z ↑	0.0135	0.0126	3.1670	2.2891
	X21_P4	**X29_P4**	**X21_P4**	**X29_P4**
A to Z ↓	0.0063	0.0064	0.4831	0.3626
A to Z ↑	0.0128	0.0130	1.5365	1.1564
B to Z ↓	0.0055	0.0056	0.4758	0.3597
B to Z ↑	0.0134	0.0134	1.5395	1.1587
C to Z ↓	0.0037	0.0038	0.4861	0.3671
C to Z ↑	0.0128	0.0129	1.5395	1.1590

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	4.607e-05	1.000e-20
X7_P4	9.155e-05	1.000e-20
X11_P4	1.371e-04	1.000e-20
X14_P4	1.875e-04	1.000e-20
X21_P4	2.756e-04	1.000e-20
X29_P4	3.655e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	2.898e-05	6.901e-05	1.218e-04	1.414e-04
B (output stable)	3.773e-05	1.064e-04	1.509e-04	2.117e-04
C (output stable)	8.722e-05	3.126e-04	3.740e-04	6.143e-04
A to Z	1.631e-03	3.200e-03	5.034e-03	6.621e-03
B to Z	1.439e-03	2.844e-03	4.251e-03	5.885e-03
C to Z	1.253e-03	2.301e-03	3.660e-03	4.771e-03
	X21_P4	X29_P4		
A (output stable)	2.085e-04	2.774e-04		
B (output stable)	3.105e-04	4.178e-04		
C (output stable)	8.654e-04	1.156e-03		
A to Z	9.857e-03	1.315e-02		
B to Z	8.696e-03	1.158e-02		
C to Z	7.127e-03	9.487e-03		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

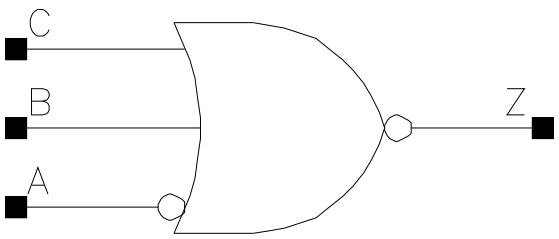
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X21_P4	X29_P4		
A (output stable)	0.000e+00	0.000e+00		
B (output stable)	0.000e+00	0.000e+00		
C (output stable)	0.000e+00	0.000e+00		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		
C to Z	0.000e+00	0.000e+00		

NOR3A

Cell Description

3 input NOR with A input inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X7_P4	0.800	1.360	1.0880
X11_P4	0.800	1.632	1.3056
X14_P4	0.800	2.176	1.7408

Truth Table

A	B	C	Z
-	-	1	0
0	-	-	0
-	1	-	0
1	0	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X11_P4	X14_P4
A	0.0007	0.0007	0.0010	0.0014
B	0.0006	0.0011	0.0016	0.0022
C	0.0006	0.0011	0.0016	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X7_P4**	**X3_P4**	**X7_P4**
A to Z ↓	0.0195	0.0181	2.7303	1.2932
A to Z ↑	0.0204	0.0209	9.2102	4.5341
B to Z ↓	0.0056	0.0055	2.9275	1.3871
B to Z ↑	0.0138	0.0139	9.2396	4.5527
C to Z ↓	0.0043	0.0035	2.9642	1.3989
C to Z ↑	0.0142	0.0131	9.2625	4.5489
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0217	0.0175	0.9068	0.6717

A to Z ↑	0.0237	0.0205	3.1673	2.3316
B to Z ↓	0.0055	0.0054	0.9578	0.7170
B to Z ↑	0.0135	0.0134	3.1774	2.3406
C to Z ↓	0.0036	0.0035	0.9595	0.7255
C to Z ↑	0.0134	0.0128	3.1788	2.3410

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	7.076e-05	1.000e-20
X7_P4	1.576e-04	1.000e-20
X11_P4	1.915e-04	1.000e-20
X14_P4	2.906e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	1.412e-03	2.541e-03	3.089e-03	4.743e-03
B (output stable)	3.887e-05	1.215e-04	1.571e-04	2.307e-04
C (output stable)	8.770e-05	3.433e-04	3.764e-04	5.992e-04
A to Z	2.754e-03	5.679e-03	7.522e-03	1.070e-02
B to Z	1.425e-03	2.990e-03	4.234e-03	5.718e-03
C to Z	1.243e-03	2.471e-03	3.613e-03	4.738e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

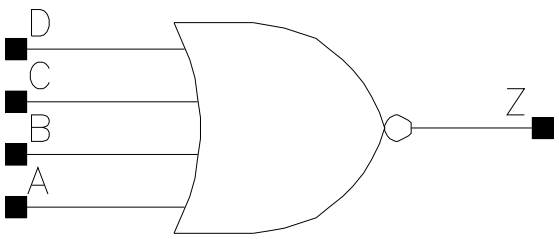
Pin Cycle (vdds)	X3_P4	X7_P4	X11_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4

Cell Description

4 input NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	1.224	0.9792
X10_P4	0.800	1.632	1.3056
X14_P4	0.800	1.904	1.5232
X18_P4	0.800	2.176	1.7408

Truth Table

A	B	C	D	Z
1	-	-	-	0
-	-	-	1	0
-	-	1	-	0
-	1	-	-	0
0	0	0	0	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X18_P4
A	0.0005	0.0004	0.0005	0.0006
B	0.0006	0.0006	0.0007	0.0008
C	0.0005	0.0005	0.0006	0.0007
D	0.0006	0.0005	0.0006	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0205	0.0247	2.7058	1.2998
A to Z ↑	0.0340	0.0380	3.5295	1.7072
B to Z ↓	0.0195	0.0245	2.7055	1.3003
B to Z ↑	0.0357	0.0409	3.5286	1.7055
C to Z ↓	0.0212	0.0252	2.7039	1.2990
C to Z ↑	0.0364	0.0411	3.5225	1.7037

D to Z ↓	0.0208	0.0241	2.7029	1.2969
D to Z ↑	0.0386	0.0428	3.5199	1.7052
	X14_P4	**X18_P4**	**X14_P4**	**X18_P4**
A to Z ↓	0.0240	0.0257	0.8946	0.7073
A to Z ↑	0.0351	0.0344	1.1768	0.8771
B to Z ↓	0.0234	0.0245	0.8948	0.7073
B to Z ↑	0.0374	0.0360	1.1785	0.8781
C to Z ↓	0.0235	0.0258	0.8922	0.7049
C to Z ↑	0.0355	0.0352	1.1755	0.8775
D to Z ↓	0.0225	0.0245	0.8921	0.7055
D to Z ↑	0.0373	0.0367	1.1772	0.8773

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.443e-04	1.000e-20
X10_P4	2.279e-04	1.000e-20
X14_P4	3.414e-04	1.000e-20
X18_P4	4.589e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	5.781e-04	6.853e-04	8.774e-04	1.088e-03
B (output stable)	5.401e-04	6.550e-04	8.307e-04	1.018e-03
C (output stable)	6.063e-04	6.552e-04	8.742e-04	1.087e-03
D (output stable)	5.695e-04	6.191e-04	8.230e-04	1.018e-03
A to Z	3.753e-03	6.053e-03	8.495e-03	1.085e-02
B to Z	3.652e-03	5.966e-03	8.363e-03	1.067e-02
C to Z	3.869e-03	5.961e-03	8.068e-03	1.036e-02
D to Z	3.784e-03	5.865e-03	7.939e-03	1.017e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

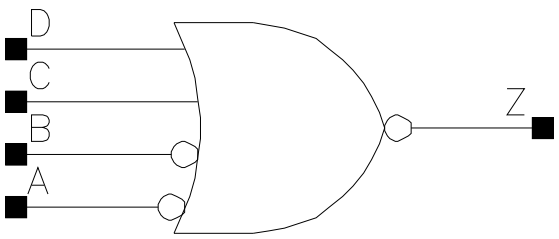
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

NOR4AB

Cell Description

4 input NOR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	1.224	0.9792
X7_P4	0.800	1.496	1.1968
X11_P4	0.800	2.040	1.6320
X14_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	-	1	-	0
-	0	-	-	0
-	-	-	1	0
0	-	-	-	0
1	1	0	0	1

Pin Capacitance

Pin	X4_P4	X7_P4	X11_P4	X14_P4
A	0.0007	0.0007	0.0014	0.0013
B	0.0008	0.0008	0.0014	0.0014
C	0.0006	0.0011	0.0016	0.0022
D	0.0006	0.0011	0.0016	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X7_P4	X4_P4	X7_P4
A to Z ↓	0.0197	0.0206	2.5451	1.3129
A to Z ↑	0.0253	0.0252	8.8771	4.6111
B to Z ↓	0.0182	0.0189	2.5433	1.3119
B to Z ↑	0.0265	0.0263	8.8810	4.6120
C to Z ↓	0.0057	0.0054	2.6799	1.3980
C to Z ↑	0.0147	0.0139	8.8912	4.6300

D to Z ↓	0.0045	0.0034	2.6991	1.3989
D to Z ↑	0.0150	0.0132	8.8985	4.6255
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0187	0.0205	0.8970	0.6750
A to Z ↑	0.0232	0.0253	3.1245	2.3216
B to Z ↓	0.0167	0.0188	0.8957	0.6736
B to Z ↑	0.0243	0.0267	3.1245	2.3213
C to Z ↓	0.0056	0.0056	0.9570	0.7147
C to Z ↑	0.0134	0.0134	3.1315	2.3282
D to Z ↓	0.0036	0.0035	0.9599	0.7192
D to Z ↑	0.0134	0.0129	3.1330	2.3273

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	1.030e-04	1.000e-20
X7_P4	1.394e-04	1.000e-20
X11_P4	2.248e-04	1.000e-20
X14_P4	2.596e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X7_P4	X11_P4	X14_P4
A (output stable)	1.100e-03	1.235e-03	2.082e-03	2.393e-03
B (output stable)	1.044e-03	1.182e-03	1.946e-03	2.270e-03
C (output stable)	7.763e-05	1.236e-04	1.811e-04	2.566e-04
D (output stable)	1.494e-04	3.503e-04	4.330e-04	6.783e-04
A to Z	4.391e-03	5.939e-03	9.242e-03	1.175e-02
B to Z	4.138e-03	5.689e-03	8.731e-03	1.123e-02
C to Z	1.576e-03	2.954e-03	4.259e-03	5.742e-03
D to Z	1.403e-03	2.454e-03	3.641e-03	4.805e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

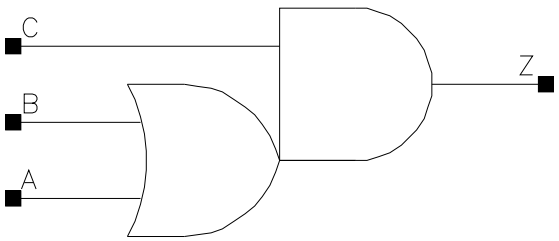
Pin Cycle (vdds)	X4_P4	X7_P4	X11_P4	X14_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA12

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.680	0.5440
X10_P4	0.800	0.952	0.7616
X19_P4	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4
A	0.0006	0.0007	0.0012
B	0.0007	0.0007	0.0014
C	0.0008	0.0009	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0184	0.0211	2.6071	1.3072
A to Z ↑	0.0165	0.0202	3.8583	1.7023
B to Z ↓	0.0199	0.0228	2.6094	1.3069
B to Z ↑	0.0147	0.0184	3.8564	1.7022
C to Z ↓	0.0179	0.0196	2.5827	1.2904
C to Z ↑	0.0148	0.0179	3.8561	1.7016
	X19_P4		**X19_P4**	
A to Z ↓	0.0220		0.6779	
A to Z ↑	0.0213		0.8725	

B to Z ↓	0.0237		0.6776	
B to Z ↑	0.0192		0.8710	
C to Z ↓	0.0198		0.6680	
C to Z ↑	0.0182		0.8704	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.152e-04	1.000e-20
X10_P4	1.983e-04	1.000e-20
X19_P4	3.786e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X19_P4
A (output stable)	5.076e-05	5.198e-05	1.085e-04
B (output stable)	5.926e-05	6.261e-05	1.237e-04
C (output stable)	4.850e-05	5.046e-05	9.914e-05
A to Z	2.810e-03	4.915e-03	9.920e-03
B to Z	2.629e-03	4.700e-03	9.524e-03
C to Z	3.040e-03	4.940e-03	9.858e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

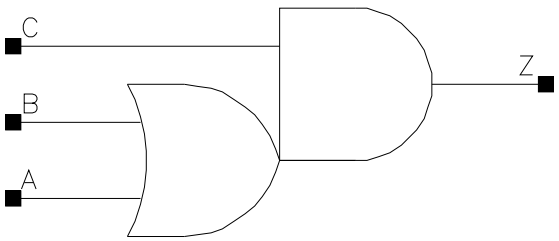
Pin Cycle (vdds)	X5_P4	X10_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00

OA21

Cell Description

2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X10_P4	0.800	1.360	1.0880
X14_P4	0.800	1.496	1.1968
X19_P4	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	0	-	0
-	-	0	0
1	-	1	1
-	1	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0006	0.0014	0.0014	0.0014
B	0.0007	0.0013	0.0013	0.0013
C	0.0007	0.0013	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0228	0.0191	2.5625	1.2983
A to Z ↑	0.0160	0.0149	3.3804	1.6570
B to Z ↓	0.0245	0.0204	2.5625	1.2996
B to Z ↑	0.0146	0.0135	3.3771	1.6554
C to Z ↓	0.0163	0.0134	2.5202	1.2821
C to Z ↑	0.0157	0.0146	3.3725	1.6524
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0213	0.0232	0.9010	0.6783

A to Z ↑	0.0166	0.0181	1.1224	0.8422
B to Z ↓	0.0227	0.0248	0.9009	0.6782
B to Z ↑	0.0153	0.0170	1.1212	0.8427
C to Z ↓	0.0151	0.0167	0.8854	0.6655
C to Z ↑	0.0163	0.0180	1.1196	0.8398

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.283e-04	1.000e-20
X10_P4	2.670e-04	1.000e-20
X14_P4	3.235e-04	1.000e-20
X19_P4	3.795e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.873e-05	3.920e-05	3.877e-05	3.955e-05
B (output stable)	2.414e-05	5.558e-05	5.611e-05	5.671e-05
C (output stable)	1.721e-04	3.473e-04	3.482e-04	3.507e-04
A to Z	3.427e-03	6.313e-03	8.132e-03	1.016e-02
B to Z	3.235e-03	5.842e-03	7.670e-03	9.722e-03
C to Z	2.982e-03	5.449e-03	7.055e-03	8.820e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

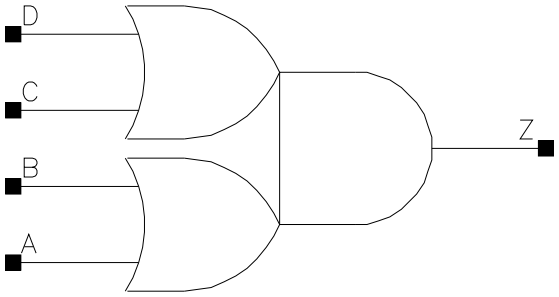
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA22

Cell Description

Double 2 input OR into 2 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.952	0.7616
X10_P4	0.800	1.088	0.8704
X14_P4	0.800	1.904	1.5232
X19_P4	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
0	0	-	-	0
-	-	0	0	0
-	1	1	-	1
1	-	1	-	1
1	-	-	1	1
-	1	-	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0004	0.0007	0.0013	0.0013
B	0.0005	0.0007	0.0013	0.0013
C	0.0005	0.0007	0.0013	0.0013
D	0.0005	0.0007	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0312	0.0258	2.6352	1.3144
A to Z ↑	0.0222	0.0199	3.3903	1.6941
B to Z ↓	0.0332	0.0276	2.6351	1.3145

B to Z ↑	0.0211	0.0187	3.3874	1.6905
C to Z ↓	0.0266	0.0229	2.6126	1.3075
C to Z ↑	0.0224	0.0208	3.3875	1.6913
D to Z ↓	0.0284	0.0243	2.6120	1.3073
D to Z ↑	0.0209	0.0192	3.3828	1.6901
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0246	0.0262	0.9116	0.6827
A to Z ↑	0.0189	0.0200	1.1268	0.8467
B to Z ↓	0.0257	0.0273	0.9118	0.6825
B to Z ↑	0.0171	0.0182	1.1234	0.8447
C to Z ↓	0.0209	0.0226	0.9058	0.6785
C to Z ↑	0.0192	0.0204	1.1243	0.8446
D to Z ↓	0.0217	0.0234	0.9060	0.6782
D to Z ↑	0.0171	0.0184	1.1216	0.8429

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	9.084e-05	1.000e-20
X10_P4	1.965e-04	1.000e-20
X14_P4	3.278e-04	1.000e-20
X19_P4	3.742e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.839e-05	2.839e-05	7.880e-05	7.836e-05
B (output stable)	2.458e-05	4.000e-05	1.803e-04	1.803e-04
C (output stable)	5.229e-05	6.569e-05	1.511e-04	1.512e-04
D (output stable)	6.041e-05	7.916e-05	2.423e-04	2.436e-04
A to Z	3.473e-03	5.701e-03	9.272e-03	1.107e-02
B to Z	3.358e-03	5.473e-03	8.688e-03	1.048e-02
C to Z	3.087e-03	5.220e-03	8.303e-03	1.005e-02
D to Z	2.977e-03	5.006e-03	7.711e-03	9.452e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

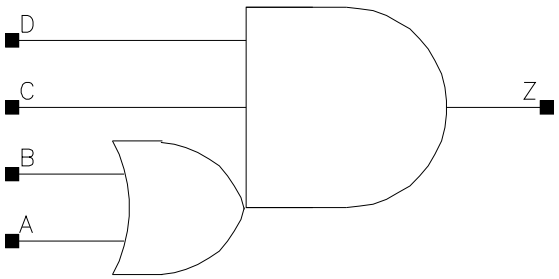
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA112

Cell Description

2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	0.816	0.6528
X10_P4	0.800	1.088	0.8704
X14_P4	0.800	1.904	1.5232
X19_P4	0.800	2.040	1.6320

Truth Table

A	B	C	D	Z
-	-	0	-	0
0	0	-	-	0
-	-	-	0	0
1	-	1	1	1
-	1	1	1	1

Pin Capacitance

Pin	X4_P4	X10_P4	X14_P4	X19_P4
A	0.0005	0.0010	0.0011	0.0013
B	0.0005	0.0007	0.0011	0.0014
C	0.0005	0.0007	0.0011	0.0013
D	0.0005	0.0007	0.0011	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X10_P4	X4_P4	X10_P4
A to Z ↓	0.0261	0.0254	2.8449	1.3345
A to Z ↑	0.0258	0.0278	3.5822	1.7245
B to Z ↓	0.0282	0.0257	2.8451	1.3335
B to Z ↑	0.0247	0.0245	3.5807	1.7208
C to Z ↓	0.0233	0.0212	2.7874	1.3122

C to Z ↑	0.0228	0.0232	3.5801	1.7199
D to Z ↓	0.0227	0.0204	2.7897	1.3114
D to Z ↑	0.0248	0.0248	3.5807	1.7191
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0250	0.0240	0.9096	0.6765
A to Z ↑	0.0268	0.0279	1.1476	0.8600
B to Z ↓	0.0257	0.0247	0.9102	0.6767
B to Z ↑	0.0243	0.0253	1.1444	0.8574
C to Z ↓	0.0222	0.0214	0.8959	0.6676
C to Z ↑	0.0230	0.0236	1.1449	0.8575
D to Z ↓	0.0210	0.0203	0.8940	0.6664
D to Z ↑	0.0241	0.0248	1.1440	0.8571

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	9.039e-05	1.000e-20
X10_P4	2.013e-04	1.000e-20
X14_P4	2.941e-04	1.000e-20
X19_P4	3.895e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X10_P4	X14_P4	X19_P4
A (output stable)	5.442e-05	7.978e-05	1.265e-04	1.398e-04
B (output stable)	5.206e-05	8.888e-05	1.504e-04	1.680e-04
C (output stable)	1.656e-05	3.051e-05	7.437e-05	8.267e-05
D (output stable)	2.553e-05	4.131e-05	1.424e-04	1.548e-04
A to Z	2.994e-03	5.677e-03	8.670e-03	1.108e-02
B to Z	2.900e-03	5.317e-03	8.143e-03	1.040e-02
C to Z	3.131e-03	5.642e-03	8.909e-03	1.125e-02
D to Z	3.023e-03	5.481e-03	8.471e-03	1.075e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

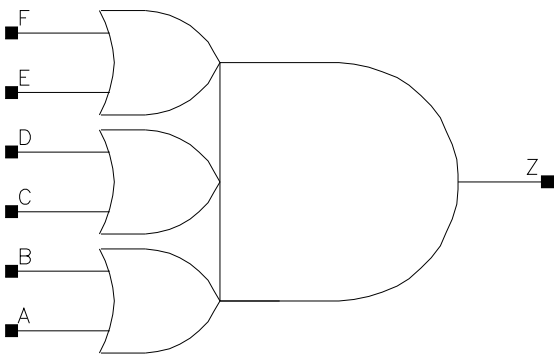
Pin Cycle (vdds)	X4_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OA222

Cell Description

Triple 2 input OR into 3 input AND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	1.360	1.0880
X9_P4	0.800	1.496	1.1968
X19_P4	0.800	2.720	2.1760

Truth Table

A	B	C	D	E	F	Z
0	0	-	-	-	-	0
-	-	0	0	-	-	0
-	-	-	-	0	0	0
1	-	-	1	-	1	1
-	1	-	1	-	1	1
1	-	1	-	-	1	1
-	1	1	-	-	1	1
1	-	-	1	1	-	1
-	1	-	1	1	-	1
-	1	1	-	1	-	1
1	-	1	-	1	-	1

Pin Capacitance

Pin	X4_P4	X9_P4	X19_P4
A	0.0005	0.0007	0.0011
B	0.0007	0.0009	0.0013
C	0.0005	0.0006	0.0012
D	0.0005	0.0006	0.0014
E	0.0005	0.0007	0.0012
F	0.0005	0.0007	0.0014

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X9_P4	X4_P4	X9_P4
A to Z ↓	0.0365	0.0310	2.8941	1.4310
A to Z ↑	0.0282	0.0276	3.6732	1.8070
B to Z ↓	0.0395	0.0336	2.8935	1.4307
B to Z ↑	0.0278	0.0266	3.6747	1.8056
C to Z ↓	0.0335	0.0283	2.8736	1.4229
C to Z ↑	0.0294	0.0280	3.6740	1.8062
D to Z ↓	0.0353	0.0300	2.8738	1.4228
D to Z ↑	0.0279	0.0263	3.6698	1.8040
E to Z ↓	0.0287	0.0250	2.8454	1.4139
E to Z ↑	0.0280	0.0275	3.6679	1.8036
F to Z ↓	0.0309	0.0269	2.8447	1.4140
F to Z ↑	0.0269	0.0261	3.6641	1.8015
	X19_P4		X19_P4	
A to Z ↓	0.0307		0.6882	
A to Z ↑	0.0268		0.8602	
B to Z ↓	0.0328		0.6881	
B to Z ↑	0.0247		0.8575	
C to Z ↓	0.0282		0.6839	
C to Z ↑	0.0274		0.8595	
D to Z ↓	0.0301		0.6838	
D to Z ↑	0.0257		0.8571	
E to Z ↓	0.0249		0.6798	
E to Z ↑	0.0272		0.8581	
F to Z ↓	0.0267		0.6798	
F to Z ↑	0.0253		0.8553	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	9.648e-05	1.000e-20
X9_P4	2.118e-04	1.000e-20
X19_P4	4.145e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X9_P4	X19_P4
A (output stable)	1.797e-05	2.864e-05	5.207e-05
B (output stable)	2.653e-05	4.005e-05	6.901e-05
C (output stable)	3.266e-05	4.408e-05	8.658e-05
D (output stable)	3.876e-05	5.243e-05	1.044e-04
E (output stable)	8.655e-05	1.084e-04	2.047e-04
F (output stable)	8.723e-05	1.171e-04	2.193e-04
A to Z	4.026e-03	6.682e-03	1.333e-02
B to Z	3.940e-03	6.505e-03	1.287e-02
C to Z	3.702e-03	6.213e-03	1.242e-02
D to Z	3.583e-03	5.994e-03	1.197e-02
E to Z	3.285e-03	5.706e-03	1.144e-02
F to Z	3.190e-03	5.519e-03	1.102e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

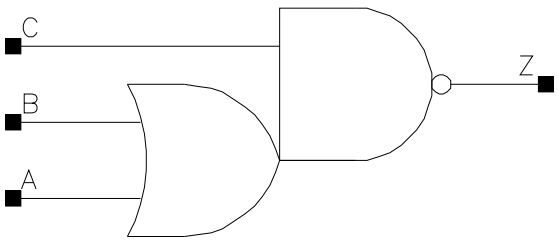
Pin Cycle (vdds)	X4_P4	X9_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00

OAI12

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.544	0.4352
X10_P4	0.800	1.360	1.0880
X20_P4	0.800	2.720	2.1760
X26_P4	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P4	X10_P4	X20_P4	X26_P4
A	0.0005	0.0017	0.0033	0.0044
B	0.0005	0.0015	0.0030	0.0042
C	0.0005	0.0017	0.0036	0.0049

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X10_P4**	**X3_P4**	**X10_P4**
A to Z ↓	0.0081	0.0094	4.8619	1.5361
A to Z ↑	0.0104	0.0100	7.5184	2.1271
B to Z ↓	0.0062	0.0072	4.7680	1.5433
B to Z ↑	0.0114	0.0104	7.5596	2.1402
C to Z ↓	0.0068	0.0075	4.4102	1.4057
C to Z ↑	0.0111	0.0102	4.2228	1.1997
	X20_P4	**X26_P4**	**X20_P4**	**X26_P4**
A to Z ↓	0.0099	0.0100	0.7851	0.5946

A to Z ↑	0.0104	0.0104	1.0937	0.8232
B to Z ↓	0.0076	0.0077	0.7945	0.6044
B to Z ↑	0.0109	0.0109	1.0997	0.8279
C to Z ↓	0.0080	0.0080	0.7213	0.5472
C to Z ↑	0.0104	0.0103	0.5910	0.4446

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	5.727e-05	1.000e-20
X10_P4	2.025e-04	1.000e-20
X20_P4	3.973e-04	1.000e-20
X26_P4	5.243e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X10_P4	X20_P4	X26_P4
A (output stable)	4.470e-05	1.638e-04	3.334e-04	4.312e-04
B (output stable)	5.324e-05	2.156e-04	4.439e-04	5.739e-04
C (output stable)	4.397e-05	1.491e-04	3.149e-04	4.123e-04
A to Z	1.236e-03	4.427e-03	8.963e-03	1.190e-02
B to Z	1.081e-03	3.657e-03	7.516e-03	9.985e-03
C to Z	1.522e-03	5.234e-03	1.072e-02	1.418e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

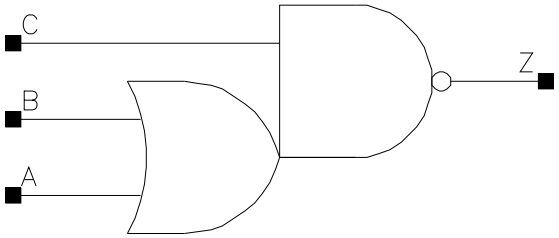
Pin Cycle (vdds)	X3_P4	X10_P4	X20_P4	X26_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI21

Cell Description

2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X7_P4	0.800	0.952	0.7616
X10_P4	0.800	1.360	1.0880
X13_P4	0.800	1.904	1.5232
X26_P4	0.800	3.536	2.8288

Truth Table

A	B	C	Z
1	-	1	0
-	1	1	0
0	0	-	1
-	-	0	1

Pin Capacitance

Pin	X3_P4	X7_P4	X10_P4	X13_P4
A	0.0006	0.0011	0.0018	0.0023
B	0.0006	0.0012	0.0017	0.0021
C	0.0008	0.0011	0.0016	0.0022
	X26_P4			
A	0.0047			
B	0.0043			
C	0.0044			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X7_P4	X3_P4	X7_P4
A to Z ↓	0.0091	0.0080	4.2761	2.2156
A to Z ↑	0.0141	0.0125	6.0776	3.1334
B to Z ↓	0.0075	0.0061	4.2954	2.1554

B to Z ↑	0.0154	0.0136	6.1074	3.1483
C to Z ↓	0.0087	0.0074	4.0735	2.0651
C to Z ↑	0.0090	0.0076	3.5352	1.8456
	X10_P4	**X13_P4**	**X10_P4**	**X13_P4**
A to Z ↓	0.0077	0.0084	1.4954	1.1459
A to Z ↑	0.0121	0.0128	2.0684	1.6009
B to Z ↓	0.0060	0.0062	1.4902	1.1502
B to Z ↑	0.0130	0.0132	2.0795	1.6075
C to Z ↓	0.0073	0.0075	1.4156	1.0816
C to Z ↑	0.0071	0.0072	1.2173	0.9230
	X26_P4		**X26_P4**	
A to Z ↓	0.0083		0.5910	
A to Z ↑	0.0125		0.8093	
B to Z ↓	0.0060		0.5901	
B to Z ↑	0.0131		0.8127	
C to Z ↓	0.0078		0.5566	
C to Z ↑	0.0071		0.4660	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	7.579e-05	1.000e-20
X7_P4	1.418e-04	1.000e-20
X10_P4	2.074e-04	1.000e-20
X13_P4	2.726e-04	1.000e-20
X26_P4	5.283e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X7_P4	X10_P4	X13_P4
A (output stable)	2.176e-05	3.984e-05	5.753e-05	1.021e-04
B (output stable)	2.740e-05	5.312e-05	7.874e-05	1.831e-04
C (output stable)	1.728e-04	3.426e-04	4.550e-04	6.624e-04
A to Z	1.975e-03	3.396e-03	5.012e-03	6.887e-03
B to Z	1.761e-03	3.021e-03	4.378e-03	5.811e-03
C to Z	1.606e-03	2.887e-03	4.185e-03	5.716e-03
	X26_P4			
A (output stable)	1.997e-04			
B (output stable)	3.340e-04			
C (output stable)	1.196e-03			
A to Z	1.344e-02			
B to Z	1.130e-02			
C to Z	1.112e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X3_P4	X7_P4	X10_P4	X13_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

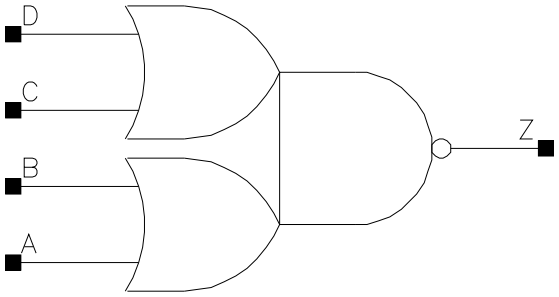
	X26_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			

OAI22

Cell Description

Double 2 input OR into 2 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X6_P4	0.800	1.360	1.0880
X8_P4	0.800	1.768	1.4144
X11_P4	0.800	2.448	1.9584
X24_P4	0.800	4.624	3.6992

Truth Table

A	B	C	D	Z
1	-	1	-	0
-	1	1	-	0
-	1	-	1	0
1	-	-	1	0
0	0	-	-	1
-	-	0	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X8_P4	X11_P4
A	0.0006	0.0012	0.0017	0.0022
B	0.0005	0.0011	0.0015	0.0021
C	0.0005	0.0011	0.0016	0.0022
D	0.0005	0.0010	0.0015	0.0020
	X24_P4			
A	0.0048			
B	0.0045			
C	0.0046			
D	0.0042			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	**X6_P4**	**X3_P4**	**X6_P4**
A to Z ↓	0.0081	0.0103	4.0184	2.1763
A to Z ↑	0.0159	0.0153	7.4175	3.3099
B to Z ↓	0.0069	0.0082	3.9878	2.1872
B to Z ↑	0.0173	0.0159	7.4429	3.3200
C to Z ↓	0.0076	0.0098	4.1142	2.2017
C to Z ↑	0.0112	0.0111	7.4463	3.3358
D to Z ↓	0.0060	0.0074	4.0792	2.2287
D to Z ↑	0.0122	0.0111	7.4837	3.3525
	X8_P4	**X11_P4**	**X8_P4**	**X11_P4**
A to Z ↓	0.0097	0.0099	1.4864	1.1273
A to Z ↑	0.0144	0.0144	2.2184	1.6661
B to Z ↓	0.0080	0.0079	1.4964	1.1318
B to Z ↑	0.0152	0.0152	2.2295	1.6743
C to Z ↓	0.0096	0.0099	1.5137	1.1470
C to Z ↑	0.0104	0.0106	2.2169	1.6814
D to Z ↓	0.0076	0.0076	1.5313	1.1539
D to Z ↑	0.0109	0.0110	2.2326	1.6918
	X24_P4		**X24_P4**	
A to Z ↓	0.0101		0.5560	
A to Z ↑	0.0144		0.8093	
B to Z ↓	0.0081		0.5530	
B to Z ↑	0.0154		0.8131	
C to Z ↓	0.0104		0.5661	
C to Z ↑	0.0106		0.8107	
D to Z ↓	0.0079		0.5648	
D to Z ↑	0.0110		0.8163	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	7.207e-05	1.000e-20
X6_P4	1.688e-04	1.000e-20
X8_P4	2.463e-04	1.000e-20
X11_P4	3.303e-04	1.000e-20
X24_P4	6.438e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X6_P4	X8_P4	X11_P4
A (output stable)	2.511e-05	8.111e-05	1.042e-04	1.453e-04
B (output stable)	3.475e-05	1.835e-04	1.955e-04	3.064e-04
C (output stable)	6.047e-05	1.510e-04	1.941e-04	2.685e-04
D (output stable)	7.346e-05	2.449e-04	2.870e-04	4.283e-04
A to Z	1.807e-03	4.048e-03	5.739e-03	7.702e-03
B to Z	1.624e-03	3.499e-03	4.947e-03	6.655e-03
C to Z	1.369e-03	3.233e-03	4.610e-03	6.257e-03
D to Z	1.206e-03	2.694e-03	3.868e-03	5.254e-03
	X24_P4			
A (output stable)	2.957e-04			
B (output stable)	5.750e-04			
C (output stable)	5.211e-04			
D (output stable)	7.918e-04			

A to Z	1.585e-02			
B to Z	1.370e-02			
C to Z	1.285e-02			
D to Z	1.080e-02			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

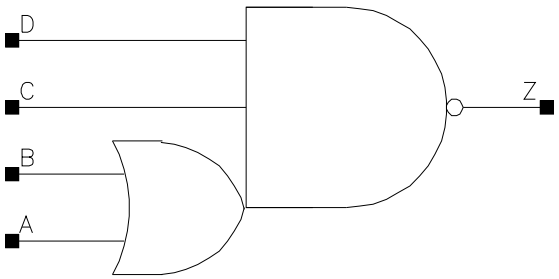
Pin Cycle (vdds)	X3_P4	X6_P4	X8_P4	X11_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X24_P4			
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			

OAI112

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.816	0.6528
X6_P4	0.800	1.360	1.0880
X12_P4	0.800	2.448	1.9584
X18_P4	0.800	3.536	2.8288

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X12_P4	X18_P4
A	0.0008	0.0011	0.0021	0.0031
B	0.0005	0.0010	0.0020	0.0030
C	0.0006	0.0012	0.0023	0.0036
D	0.0006	0.0011	0.0022	0.0033

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0153	0.0134	5.7856	3.1304
A to Z ↑	0.0143	0.0117	6.3415	3.1918
B to Z ↓	0.0116	0.0106	5.8387	3.1476
B to Z ↑	0.0138	0.0118	6.3512	3.2100
C to Z ↓	0.0114	0.0113	5.4400	2.9452

C to Z ↑	0.0127	0.0122	3.3959	1.7573
D to Z ↓	0.0130	0.0120	5.4780	2.9613
D to Z ↑	0.0122	0.0109	3.4971	1.7641
	X12_P4	**X18_P4**	**X12_P4**	**X18_P4**
A to Z ↓	0.0138	0.0140	1.6297	1.1028
A to Z ↑	0.0114	0.0114	1.6029	1.0760
B to Z ↓	0.0108	0.0111	1.6406	1.1119
B to Z ↑	0.0115	0.0117	1.6138	1.0835
C to Z ↓	0.0112	0.0113	1.5341	1.0394
C to Z ↑	0.0120	0.0118	0.8987	0.5923
D to Z ↓	0.0121	0.0123	1.5428	1.0447
D to Z ↑	0.0107	0.0107	0.8960	0.5993

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	6.155e-05	1.000e-20
X6_P4	1.145e-04	1.000e-20
X12_P4	2.178e-04	1.000e-20
X18_P4	3.212e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X6_P4	X12_P4	X18_P4
A (output stable)	7.828e-05	1.540e-04	2.871e-04	4.049e-04
B (output stable)	8.803e-05	1.768e-04	3.221e-04	4.448e-04
C (output stable)	2.730e-05	8.026e-05	1.492e-04	2.344e-04
D (output stable)	4.125e-05	1.465e-04	2.515e-04	3.884e-04
A to Z	1.919e-03	3.275e-03	6.405e-03	9.556e-03
B to Z	1.597e-03	2.728e-03	5.304e-03	7.945e-03
C to Z	2.293e-03	4.252e-03	8.172e-03	1.222e-02
D to Z	2.113e-03	3.748e-03	7.227e-03	1.075e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

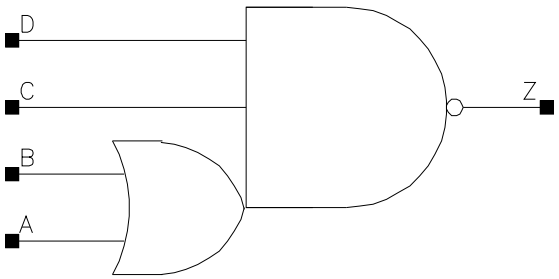
Pin Cycle (vdds)	X3_P4	X6_P4	X12_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI211

Cell Description

2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X3_P4	0.800	0.680	0.5440
X6_P4	0.800	1.360	1.0880
X9_P4	0.800	1.768	1.4144
X12_P4	0.800	2.448	1.9584

Truth Table

A	B	C	D	Z
-	1	1	1	0
1	-	1	1	0
-	-	0	-	1
0	0	-	-	1
-	-	-	0	1

Pin Capacitance

Pin	X3_P4	X6_P4	X9_P4	X12_P4
A	0.0006	0.0012	0.0018	0.0023
B	0.0006	0.0011	0.0016	0.0024
C	0.0006	0.0011	0.0017	0.0022
D	0.0006	0.0011	0.0016	0.0021

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X3_P4	X6_P4	X3_P4	X6_P4
A to Z ↓	0.0112	0.0116	6.2166	3.0897
A to Z ↑	0.0147	0.0154	6.3645	3.1895
B to Z ↓	0.0095	0.0093	6.0914	3.1080
B to Z ↑	0.0160	0.0161	6.3945	3.2018
C to Z ↓	0.0101	0.0106	5.8731	2.9583

C to Z ↑	0.0097	0.0099	3.6836	1.8300
D to Z ↓	0.0110	0.0110	5.9149	2.9750
D to Z ↑	0.0084	0.0079	3.7219	1.8451
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0118	0.0118	2.1221	1.6156
A to Z ↑	0.0148	0.0152	2.1009	1.6453
B to Z ↓	0.0097	0.0095	2.1223	1.6212
B to Z ↑	0.0157	0.0163	2.1120	1.6542
C to Z ↓	0.0106	0.0107	2.0234	1.5426
C to Z ↑	0.0094	0.0096	1.2091	0.9178
D to Z ↓	0.0113	0.0112	2.0356	1.5517
D to Z ↑	0.0078	0.0076	1.2190	0.9286

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X3_P4	5.539e-05	1.000e-20
X6_P4	1.157e-04	1.000e-20
X9_P4	1.653e-04	1.000e-20
X12_P4	2.195e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	1.577e-05	3.553e-05	5.580e-05	7.066e-05
B (output stable)	1.760e-05	5.422e-05	7.550e-05	1.022e-04
C (output stable)	4.546e-05	1.038e-04	1.536e-04	2.004e-04
D (output stable)	8.087e-05	2.821e-04	3.225e-04	5.060e-04
A to Z	1.951e-03	4.144e-03	6.067e-03	8.083e-03
B to Z	1.740e-03	3.565e-03	5.188e-03	6.912e-03
C to Z	1.587e-03	3.385e-03	4.887e-03	6.586e-03
D to Z	1.431e-03	2.979e-03	4.369e-03	5.764e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

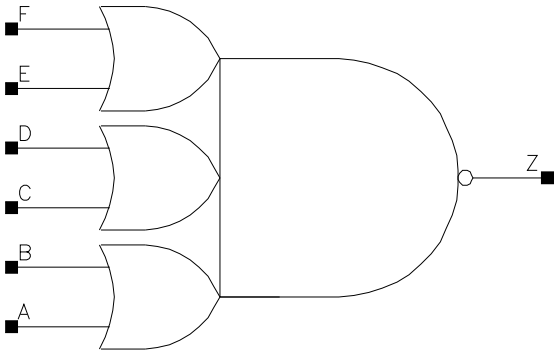
Pin Cycle (vdds)	X3_P4	X6_P4	X9_P4	X12_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OAI222

Cell Description

Triple 2 input OR into 3 input NAND

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.224	0.9792
X3_P4	0.800	1.224	0.9792
X5_P4	0.800	2.040	1.6320
X8_P4	0.800	2.720	2.1760
X10_P4	0.800	3.672	2.9376

Truth Table

A	B	C	D	E	F	Z
-	1	-	1	1	-	0
-	1	1	-	1	-	0
-	1	-	1	-	1	0
1	-	1	-	1	-	0
-	1	1	-	-	1	0
1	-	-	1	-	1	0
1	-	-	1	1	-	0
1	-	1	-	-	1	0
0	0	-	-	-	-	1
-	-	0	0	-	-	1
-	-	-	-	0	0	1

Pin Capacitance

Pin	X2_P4	X3_P4	X5_P4	X8_P4
A	0.0005	0.0006	0.0012	0.0018
B	0.0005	0.0006	0.0011	0.0016
C	0.0005	0.0006	0.0011	0.0017
D	0.0005	0.0005	0.0011	0.0016

E	0.0004	0.0006	0.0011	0.0016
F	0.0004	0.0005	0.0010	0.0015
	X10_P4			
A	0.0023			
B	0.0022			
C	0.0022			
D	0.0021			
E	0.0021			
F	0.0020			

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X3_P4**	**X2_P4**	**X3_P4**
A to Z ↓	0.0148	0.0144	6.7511	5.3160
A to Z ↑	0.0215	0.0188	8.5301	6.0008
B to Z ↓	0.0136	0.0131	6.7753	5.3514
B to Z ↑	0.0234	0.0206	8.5550	6.0222
C to Z ↓	0.0151	0.0150	6.8022	5.3438
C to Z ↑	0.0186	0.0167	8.5410	6.1099
D to Z ↓	0.0141	0.0133	6.8829	5.4219
D to Z ↑	0.0209	0.0180	8.5865	6.1324
E to Z ↓	0.0140	0.0140	6.8582	5.3778
E to Z ↑	0.0146	0.0129	8.5568	6.1279
F to Z ↓	0.0127	0.0124	6.9366	5.4672
F to Z ↑	0.0162	0.0142	8.6072	6.1623
	X5_P4	**X8_P4**	**X5_P4**	**X8_P4**
A to Z ↓	0.0156	0.0152	2.8499	1.9385
A to Z ↑	0.0194	0.0186	3.1851	2.1053
B to Z ↓	0.0135	0.0132	2.8687	1.9424
B to Z ↑	0.0202	0.0199	3.1938	2.1129
C to Z ↓	0.0150	0.0154	2.8733	1.9533
C to Z ↑	0.0163	0.0160	3.2204	2.1611
D to Z ↓	0.0129	0.0132	2.8846	1.9616
D to Z ↑	0.0171	0.0174	3.2349	2.1709
E to Z ↓	0.0149	0.0148	2.9059	1.9676
E to Z ↑	0.0129	0.0125	3.2288	2.1693
F to Z ↓	0.0125	0.0125	2.9223	1.9755
F to Z ↑	0.0133	0.0134	3.2475	2.1837
	X10_P4		**X10_P4**	
A to Z ↓	0.0157		1.4755	
A to Z ↑	0.0189		1.6031	
B to Z ↓	0.0135		1.4802	
B to Z ↑	0.0200		1.6086	
C to Z ↓	0.0153		1.4857	
C to Z ↑	0.0161		1.6372	
D to Z ↓	0.0131		1.4910	
D to Z ↑	0.0171		1.6452	
E to Z ↓	0.0151		1.4985	
E to Z ↑	0.0127		1.6349	
F to Z ↓	0.0128		1.5089	
F to Z ↑	0.0134		1.6458	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P4	6.645e-05	1.000e-20
X3_P4	1.051e-04	1.000e-20
X5_P4	1.960e-04	1.000e-20
X8_P4	2.822e-04	1.000e-20
X10_P4	3.735e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P4	X3_P4	X5_P4	X8_P4
A (output stable)	2.257e-05	2.831e-05	7.620e-05	1.036e-04
B (output stable)	2.840e-05	3.694e-05	1.398e-04	1.652e-04
C (output stable)	3.800e-05	4.739e-05	1.092e-04	1.494e-04
D (output stable)	4.480e-05	5.509e-05	1.682e-04	1.994e-04
E (output stable)	9.464e-05	1.183e-04	2.117e-04	3.128e-04
F (output stable)	1.024e-04	1.291e-04	2.710e-04	3.676e-04
A to Z	2.241e-03	2.772e-03	5.491e-03	7.960e-03
B to Z	2.086e-03	2.560e-03	4.885e-03	7.115e-03
C to Z	1.889e-03	2.368e-03	4.558e-03	6.669e-03
D to Z	1.757e-03	2.158e-03	4.049e-03	5.988e-03
E to Z	1.537e-03	1.953e-03	3.859e-03	5.545e-03
F to Z	1.405e-03	1.763e-03	3.340e-03	4.889e-03
	X10_P4			
A (output stable)	1.452e-04			
B (output stable)	2.546e-04			
C (output stable)	2.034e-04			
D (output stable)	3.095e-04			
E (output stable)	4.015e-04			
F (output stable)	4.998e-04			
A to Z	1.070e-02			
B to Z	9.518e-03			
C to Z	8.920e-03			
D to Z	7.924e-03			
E to Z	7.517e-03			
F to Z	6.555e-03			

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	X2_P4	X3_P4	X5_P4	X8_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
F to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X10_P4			

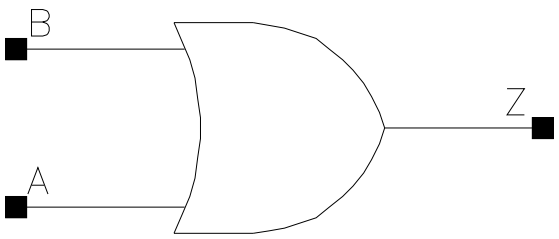
A (output stable)	0.000e+00			
B (output stable)	0.000e+00			
C (output stable)	0.000e+00			
D (output stable)	0.000e+00			
E (output stable)	0.000e+00			
F (output stable)	0.000e+00			
A to Z	0.000e+00			
B to Z	0.000e+00			
C to Z	0.000e+00			
D to Z	0.000e+00			
E to Z	0.000e+00			
F to Z	0.000e+00			

OR2

Cell Description

2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.544	0.4352
X9_P4	0.800	0.680	0.5440
X19_P4	0.800	1.360	1.0880
X29_P4	0.800	1.632	1.3056

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X5_P4	X9_P4	X19_P4	X29_P4
A	0.0006	0.0007	0.0012	0.0012
B	0.0005	0.0006	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X9_P4**	**X5_P4**	**X9_P4**
A to Z ↓	0.0236	0.0209	2.7594	1.3886
A to Z ↑	0.0152	0.0168	3.4942	1.7592
B to Z ↓	0.0251	0.0222	2.7560	1.3871
B to Z ↑	0.0141	0.0155	3.4939	1.7598
	X19_P4	**X29_P4**	**X19_P4**	**X29_P4**
A to Z ↓	0.0212	0.0253	0.6675	0.4553
A to Z ↑	0.0168	0.0196	0.8384	0.5631
B to Z ↓	0.0219	0.0262	0.6671	0.4550
B to Z ↑	0.0150	0.0178	0.8366	0.5619

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	6.740e-05	1.000e-20
X9_P4	1.364e-04	1.000e-20
X19_P4	2.745e-04	1.000e-20
X29_P4	3.474e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X9_P4	X19_P4	X29_P4
A (output stable)	1.541e-05	2.819e-05	9.814e-05	9.834e-05
B (output stable)	2.954e-05	4.955e-05	2.707e-04	2.722e-04
A to Z	2.587e-03	4.381e-03	9.253e-03	1.361e-02
B to Z	2.475e-03	4.213e-03	8.652e-03	1.299e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

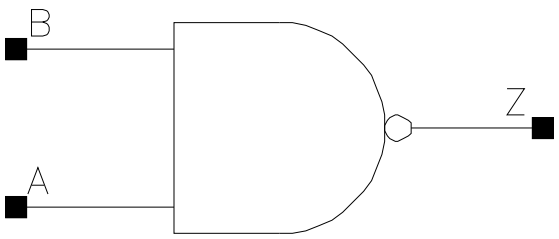
Pin Cycle (vdds)	X5_P4	X9_P4	X19_P4	X29_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR2AB

Cell Description

2 input OR with A and B inputs inverted

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.816	0.6528
X9_P4	0.800	0.952	0.7616
X14_P4	0.800	1.088	0.8704
X18_P4	0.800	1.088	0.8704

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X5_P4	X9_P4	X14_P4	X18_P4
A	0.0007	0.0007	0.0007	0.0006
B	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X9_P4**	**X5_P4**	**X9_P4**
A to Z ↓	0.0197	0.0227	2.5140	1.3663
A to Z ↑	0.0216	0.0240	3.3629	1.7703
B to Z ↓	0.0210	0.0245	2.5148	1.3675
B to Z ↑	0.0201	0.0229	3.3578	1.7688
	X14_P4	**X18_P4**	**X14_P4**	**X18_P4**
A to Z ↓	0.0251	0.0269	0.9428	0.7109
A to Z ↑	0.0259	0.0269	1.1676	0.9083
B to Z ↓	0.0268	0.0286	0.9424	0.7114
B to Z ↑	0.0247	0.0258	1.1680	0.9085

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	1.793e-04	1.000e-20
X9_P4	2.088e-04	1.000e-20
X14_P4	2.473e-04	1.000e-20
X18_P4	2.693e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X9_P4	X14_P4	X18_P4
A (output stable)	1.777e-05	1.658e-05	1.648e-05	1.746e-05
B (output stable)	3.488e-05	3.176e-05	3.156e-05	3.065e-05
A to Z	4.438e-03	5.724e-03	7.437e-03	8.736e-03
B to Z	4.284e-03	5.570e-03	7.284e-03	8.583e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

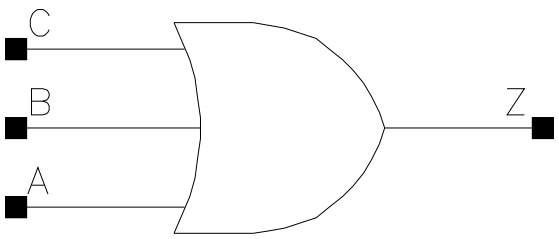
Pin Cycle (vdds)	X5_P4	X9_P4	X14_P4	X18_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR3

Cell Description

3 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.680	0.5440
X10_P4	0.800	0.952	0.7616
X14_P4	0.800	1.496	1.1968
X19_P4	0.800	2.040	1.6320

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0005	0.0007	0.0012	0.0019
B	0.0005	0.0007	0.0014	0.0019
C	0.0005	0.0007	0.0013	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0298	0.0272	2.8344	1.3499
A to Z ↑	0.0179	0.0160	3.5107	1.6694
B to Z ↓	0.0307	0.0282	2.8371	1.3497
B to Z ↑	0.0174	0.0151	3.5100	1.6696
C to Z ↓	0.0319	0.0289	2.8367	1.3501
C to Z ↑	0.0164	0.0140	3.5132	1.6679
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**
A to Z ↓	0.0256	0.0247	0.9075	0.6952

A to Z ↑	0.0148	0.0144	1.1442	0.8801
B to Z ↓	0.0267	0.0253	0.9076	0.6955
B to Z ↑	0.0136	0.0138	1.1409	0.8791
C to Z ↓	0.0259	0.0255	0.9073	0.6946
C to Z ↑	0.0121	0.0121	1.1409	0.8774

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	5.783e-05	1.000e-20
X10_P4	1.207e-04	1.000e-20
X14_P4	2.012e-04	1.000e-20
X19_P4	2.760e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	1.824e-05	3.249e-05	6.907e-05	1.223e-04
B (output stable)	2.386e-05	4.098e-05	1.049e-04	1.515e-04
C (output stable)	5.348e-05	9.402e-05	3.212e-04	3.652e-04
A to Z	3.014e-03	5.242e-03	8.443e-03	1.179e-02
B to Z	2.896e-03	5.046e-03	8.062e-03	1.097e-02
C to Z	2.794e-03	4.859e-03	7.456e-03	1.030e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

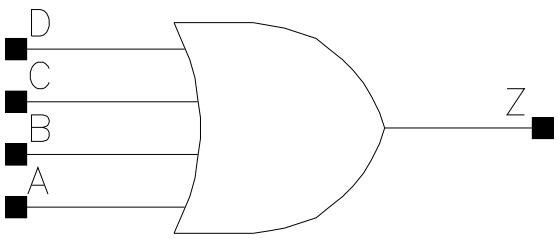
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

OR4

Cell Description

4 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	0.800	1.224	0.9792
X8_P4	0.800	1.496	1.1968
X12_P4	0.800	2.176	1.7408
X15_P4	0.800	2.584	2.0672

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X4_P4	X8_P4	X12_P4	X15_P4
A	0.0004	0.0006	0.0012	0.0013
B	0.0005	0.0007	0.0011	0.0013
C	0.0004	0.0006	0.0011	0.0013
D	0.0005	0.0007	0.0011	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X8_P4	X4_P4	X8_P4
A to Z ↓	0.0247	0.0238	4.0813	2.1670
A to Z ↑	0.0156	0.0165	3.2590	1.7533
B to Z ↓	0.0267	0.0256	4.0803	2.1661
B to Z ↑	0.0146	0.0155	3.2583	1.7512
C to Z ↓	0.0265	0.0236	4.0859	2.1619
C to Z ↑	0.0162	0.0162	3.3503	1.7598

D to Z ↓	0.0288	0.0255	4.0849	2.1613
D to Z ↑	0.0155	0.0152	3.3487	1.7565
	X12_P4	**X15_P4**	**X12_P4**	**X15_P4**
A to Z ↓	0.0237	0.0243	1.4947	1.1224
A to Z ↑	0.0166	0.0160	1.1189	0.8621
B to Z ↓	0.0248	0.0252	1.4944	1.1219
B to Z ↑	0.0155	0.0145	1.1183	0.8605
C to Z ↓	0.0234	0.0237	1.4933	1.1205
C to Z ↑	0.0158	0.0154	1.1136	0.8664
D to Z ↓	0.0245	0.0247	1.4923	1.1197
D to Z ↑	0.0148	0.0140	1.1126	0.8665

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	7.819e-05	1.000e-20
X8_P4	1.731e-04	1.000e-20
X12_P4	2.251e-04	1.000e-20
X15_P4	3.214e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	6.338e-04	1.134e-03	1.700e-03	2.306e-03
B (output stable)	5.984e-04	1.064e-03	1.585e-03	2.155e-03
C (output stable)	6.163e-04	1.069e-03	1.565e-03	2.105e-03
D (output stable)	5.819e-04	9.983e-04	1.450e-03	1.983e-03
A to Z	2.743e-03	5.340e-03	7.615e-03	1.022e-02
B to Z	2.639e-03	5.153e-03	7.233e-03	9.627e-03
C to Z	2.776e-03	4.906e-03	7.004e-03	9.181e-03
D to Z	2.690e-03	4.729e-03	6.639e-03	8.669e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

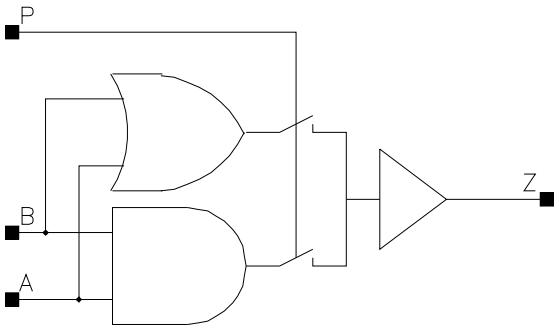
Pin Cycle (vdds)	X4_P4	X8_P4	X12_P4	X15_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAO2

Cell Description

2 bit programmable AND/OR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	0.800	0.952	0.7616
X10_P4	1.600	0.816	1.3056
X14_P4	1.600	1.224	1.9584
X19_P4	1.600	1.224	1.9584

Truth Table

A	B	P	Z
A	-	A	A
A	A	-	A
-	B	B	B

Pin Capacitance

Pin	X5_P4	X10_P4	X14_P4	X19_P4
A	0.0010	0.0012	0.0023	0.0022
B	0.0010	0.0013	0.0024	0.0024
P	0.0005	0.0008	0.0013	0.0013

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
A to Z ↓	0.0287	0.0265	2.7951	1.3047
A to Z ↑	0.0166	0.0206	3.5237	1.6844
B to Z ↓	0.0292	0.0276	2.8038	1.3104
B to Z ↑	0.0177	0.0220	3.5286	1.6859
P to Z ↓	0.0278	0.0271	2.7973	1.3086
P to Z ↑	0.0173	0.0219	3.5224	1.6844
	X14_P4	**X19_P4**	**X14_P4**	**X19_P4**

A to Z ↓	0.0244	0.0263	0.9005	0.6739
A to Z ↑	0.0200	0.0208	1.1584	0.8633
B to Z ↓	0.0240	0.0258	0.9080	0.6779
B to Z ↑	0.0202	0.0212	1.1593	0.8644
P to Z ↓	0.0246	0.0265	0.9069	0.6771
P to Z ↑	0.0208	0.0219	1.1574	0.8629

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	9.390e-05	1.000e-20
X10_P4	2.132e-04	1.000e-20
X14_P4	3.496e-04	1.000e-20
X19_P4	4.098e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	4.004e-05	6.030e-05	1.626e-04	1.553e-04
B (output stable)	5.448e-05	8.845e-05	3.541e-04	3.411e-04
P (output stable)	1.511e-04	2.366e-04	4.568e-04	4.171e-04
A to Z	3.005e-03	5.918e-03	9.333e-03	1.136e-02
B to Z	2.935e-03	5.876e-03	8.971e-03	1.098e-02
P to Z	2.769e-03	5.680e-03	8.995e-03	1.107e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

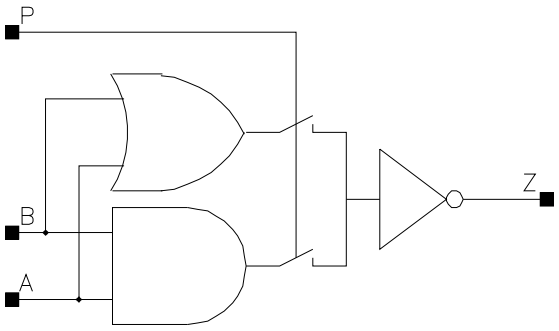
Pin Cycle (vdds)	X5_P4	X10_P4	X14_P4	X19_P4
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

PAOI2

Cell Description

2 bit programmable NAND/NOR logic

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.600	0.544	0.8704
X10_P4	1.600	0.952	1.5232

Truth Table

A	B	P	Z
A	-	A	!A
A	A	-	!A
-	B	B	!B

Pin Capacitance

Pin	X5_P4	X10_P4
A	0.0011	0.0021
B	0.0010	0.0019
P	0.0007	0.0011

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	X10_P4	X5_P4	X10_P4
A to Z ↓	0.0102	0.0093	4.1478	2.1707
A to Z ↑	0.0154	0.0141	6.1041	3.1121
B to Z ↓	0.0110	0.0092	4.1118	2.1815
B to Z ↑	0.0158	0.0133	6.0900	3.1599
P to Z ↓	0.0114	0.0098	4.2094	2.1975
P to Z ↑	0.0158	0.0134	6.1555	3.1312

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	9.736e-05	1.000e-20
X10_P4	1.823e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X5_P4	X10_P4
A (output stable)	5.685e-05	1.622e-04
B (output stable)	8.019e-05	3.447e-04
P (output stable)	2.037e-04	4.639e-04
A to Z	2.165e-03	3.904e-03
B to Z	2.049e-03	3.461e-03
P to Z	1.846e-03	3.271e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

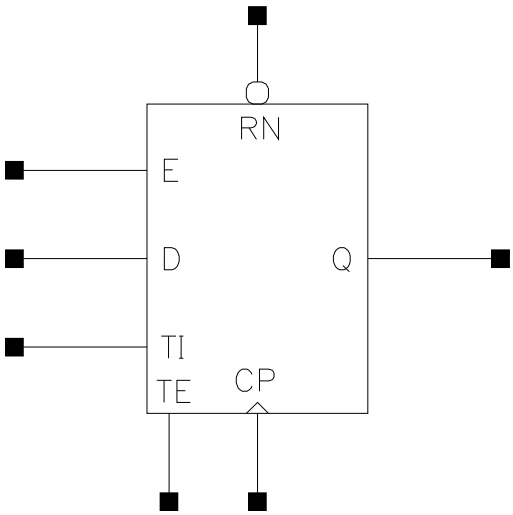
Pin Cycle (vdds)	X5_P4	X10_P4
A (output stable)	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00
P (output stable)	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00
P to Z	0.000e+00	0.000e+00

SDFPHRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.600	2.992	4.7872
X10_P4	1.600	3.128	5.0048
X19_P4	1.600	3.264	5.2224
X23_P4	1.600	3.264	5.2224
X29_P4	1.600	3.536	5.6576
X34_P4	1.600	3.536	5.6576

Truth Table

IQ	Q
IQ	IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4	X23_P4
CP	0.0006	0.0006	0.0006	0.0006
D	0.0006	0.0006	0.0006	0.0006
E	0.0012	0.0012	0.0012	0.0012

RN	0.0009	0.0009	0.0009	0.0009
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P4	X34_P4		
CP	0.0006	0.0006		
D	0.0006	0.0006		
E	0.0012	0.0012		
RN	0.0009	0.0009		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
CP to Q ↓	0.0386	0.0617	2.5590	1.2878
CP to Q ↑	0.0517	0.0791	3.3077	1.6860
RN to Q ↓	0.0361	0.0547	2.4783	1.2876
	X19_P4	**X23_P4**	**X19_P4**	**X23_P4**
CP to Q ↓	0.0667	0.0673	0.6645	0.5072
CP to Q ↑	0.0827	0.0815	0.8491	0.8294
RN to Q ↓	0.0599	0.0606	0.6653	0.5075
	X29_P4	**X34_P4**	**X29_P4**	**X34_P4**
CP to Q ↓	0.0573	0.0568	0.4426	0.3501
CP to Q ↑	0.0686	0.0693	0.5640	0.5626
RN to Q ↓	0.0532	0.0528	0.4425	0.3494

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P4	X10_P4	X19_P4	X23_P4
CP ↓	min_pulse_width to CP	0.0456	0.0456	0.0456	0.0456
CP ↑	min_pulse_width to CP	0.0364	0.0349	0.0363	0.0363
D ↓	hold_rising to CP	-0.0196	-0.0196	-0.0196	-0.0196
D ↑	hold_rising to CP	-0.0018	-0.0018	-0.0018	-0.0018
D ↓	setup_rising to CP	0.0494	0.0494	0.0494	0.0494
D ↑	setup_rising to CP	0.0299	0.0299	0.0299	0.0299
E ↓	hold_rising to CP	-0.0240	-0.0240	-0.0240	-0.0240
E ↑	hold_rising to CP	-0.0045	-0.0045	-0.0045	-0.0045
E ↓	setup_rising to CP	0.0661	0.0661	0.0661	0.0661
E ↑	setup_rising to CP	0.0488	0.0488	0.0488	0.0488
RN ↓	min_pulse_width to RN	0.0425	0.0376	0.0425	0.0425
RN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
RN ↑	removal_rising to CP	0.0090	0.0090	0.0090	0.0090
TE ↓	hold_rising to CP	-0.0094	-0.0094	-0.0094	-0.0094

TE ↑	hold_rising to CP	0.0004	0.0004	0.0004	0.0004
TE ↓	setup_rising to CP	0.0386	0.0386	0.0386	0.0386
TE ↑	setup_rising to CP	0.0471	0.0471	0.0471	0.0467
TI ↓	hold_rising to CP	-0.0169	-0.0166	-0.0169	-0.0169
TI ↑	hold_rising to CP	0.0025	0.0025	0.0025	0.0025
TI ↓	setup_rising to CP	0.0464	0.0464	0.0464	0.0464
TI ↑	setup_rising to CP	0.0222	0.0265	0.0222	0.0222
		X29_P4	X34_P4		
CP ↓	min_pulse_width to CP	0.0456	0.0456		
CP ↑	min_pulse_width to CP	0.0363	0.0363		
D ↓	hold_rising to CP	-0.0196	-0.0196		
D ↑	hold_rising to CP	-0.0018	-0.0018		
D ↓	setup_rising to CP	0.0494	0.0494		
D ↑	setup_rising to CP	0.0299	0.0299		
E ↓	hold_rising to CP	-0.0240	-0.0240		
E ↑	hold_rising to CP	-0.0045	-0.0045		
E ↓	setup_rising to CP	0.0661	0.0661		
E ↑	setup_rising to CP	0.0488	0.0488		
RN ↓	min_pulse_width to RN	0.0447	0.0447		
RN ↑	recovery_rising to CP	-0.0017	-0.0017		
RN ↑	removal_rising to CP	0.0090	0.0090		
TE ↓	hold_rising to CP	-0.0094	-0.0094		
TE ↑	hold_rising to CP	0.0004	0.0004		
TE ↓	setup_rising to CP	0.0386	0.0386		
TE ↑	setup_rising to CP	0.0467	0.0467		
TI ↓	hold_rising to CP	-0.0169	-0.0169		
TI ↑	hold_rising to CP	0.0025	0.0025		
TI ↓	setup_rising to CP	0.0464	0.0464		
TI ↑	setup_rising to CP	0.0265	0.0222		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	3.767e-04	1.000e-20
X10_P4	4.679e-04	1.000e-20
X19_P4	6.306e-04	1.000e-20
X23_P4	6.453e-04	1.000e-20

X29_P4	8.509e-04	1.000e-20
X34_P4	8.764e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

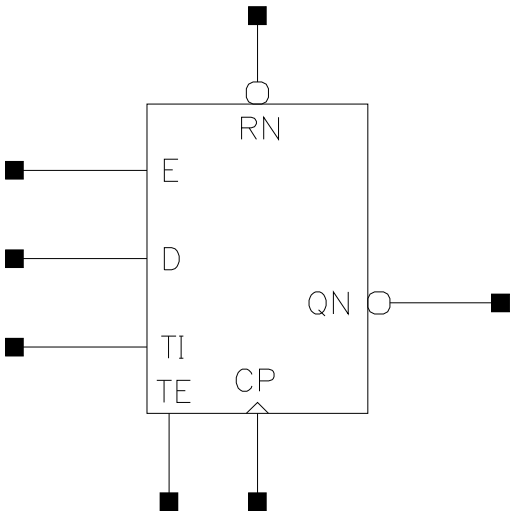
Pin Cycle	X5_P4	X10_P4	X19_P4	X23_P4
Clock 100Mhz Data 0Mhz	1.026e-02	1.025e-02	1.026e-02	1.026e-02
Clock 100Mhz Data 25Mhz	1.077e-02	1.141e-02	1.252e-02	1.264e-02
Clock 100Mhz Data 50Mhz	1.128e-02	1.257e-02	1.477e-02	1.502e-02
Clock = 0 Data 100Mhz	6.340e-03	6.340e-03	6.339e-03	6.338e-03
Clock = 1 Data 100Mhz	2.406e-03	2.405e-03	2.405e-03	2.405e-03
	X29_P4	X34_P4		
Clock 100Mhz Data 0Mhz	1.026e-02	1.026e-02		
Clock 100Mhz Data 25Mhz	1.350e-02	1.382e-02		
Clock 100Mhz Data 50Mhz	1.674e-02	1.739e-02		
Clock = 0 Data 100Mhz	6.339e-03	6.340e-03		
Clock = 1 Data 100Mhz	2.406e-03	2.407e-03		

SDFPHRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active high data enable and active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X5_P4	1.600	2.992	4.7872
X10_P4	1.600	3.128	5.0048
X19_P4	1.600	3.264	5.2224
X23_P4	1.600	3.264	5.2224
X29_P4	1.600	3.536	5.6576
X34_P4	1.600	3.536	5.6576

Truth Table

IQ	QN
IQ	!IQ

CP	RN	TE	TI	E	D	IQ	IQ
-	0	-	-	-	-	-	0
/	1	0	-	1	D	-	D
/	1	0	-	0	-	IQ	IQ
/	1	1	TI	-	-	-	TI
-	1	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	X5_P4	X10_P4	X19_P4	X23_P4
CP	0.0006	0.0006	0.0006	0.0006
D	0.0006	0.0006	0.0006	0.0006
E	0.0012	0.0013	0.0013	0.0013

RN	0.0009	0.0009	0.0008	0.0008
TE	0.0009	0.0009	0.0009	0.0009
TI	0.0003	0.0003	0.0003	0.0003
	X29_P4	X34_P4		
CP	0.0006	0.0006		
D	0.0006	0.0006		
E	0.0013	0.0012		
RN	0.0009	0.0009		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X5_P4	**X10_P4**	**X5_P4**	**X10_P4**
CP to QN ↓	0.0693	0.0616	2.5509	1.2857
CP to QN ↑	0.0524	0.0487	3.2958	1.6861
RN to QN ↑	0.0453	0.0454	3.2937	1.6827
	X19_P4	**X23_P4**	**X19_P4**	**X23_P4**
CP to QN ↓	0.0653	0.0658	0.6598	0.5076
CP to QN ↑	0.0535	0.0516	0.8484	0.8295
RN to QN ↑	0.0487	0.0468	0.8479	0.8291
	X29_P4	**X34_P4**	**X29_P4**	**X34_P4**
CP to QN ↓	0.0871	0.0852	0.4430	0.3452
CP to QN ↑	0.0698	0.0689	0.5641	0.5625
RN to QN ↑	0.0627	0.0621	0.5645	0.5629

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	X5_P4	X10_P4	X19_P4	X23_P4
CP ↓	min_pulse_width to CP	0.0456	0.0456	0.0456	0.0456
CP ↑	min_pulse_width to CP	0.0349	0.0363	0.0363	0.0363
D ↓	hold_rising to CP	-0.0196	-0.0196	-0.0196	-0.0196
D ↑	hold_rising to CP	-0.0018	-0.0018	-0.0018	-0.0018
D ↓	setup_rising to CP	0.0494	0.0494	0.0494	0.0494
D ↑	setup_rising to CP	0.0299	0.0299	0.0299	0.0299
E ↓	hold_rising to CP	-0.0240	-0.0240	-0.0240	-0.0240
E ↑	hold_rising to CP	-0.0045	-0.0045	-0.0045	-0.0045
E ↓	setup_rising to CP	0.0661	0.0688	0.0688	0.0688
E ↑	setup_rising to CP	0.0488	0.0488	0.0488	0.0488
RN ↓	min_pulse_width to RN	0.0376	0.0425	0.0447	0.0447
RN ↑	recovery_rising to CP	-0.0017	-0.0017	-0.0017	-0.0017
RN ↑	removal_rising to CP	0.0090	0.0090	0.0090	0.0090
TE ↓	hold_rising to CP	-0.0094	-0.0094	-0.0094	-0.0094

TE ↑	hold_rising to CP	0.0004	0.0004	0.0004	0.0004
TE ↓	setup_rising to CP	0.0386	0.0386	0.0386	0.0386
TE ↑	setup_rising to CP	0.0471	0.0467	0.0467	0.0467
TI ↓	hold_rising to CP	-0.0166	-0.0169	-0.0169	-0.0169
TI ↑	hold_rising to CP	0.0025	0.0025	0.0025	0.0025
TI ↓	setup_rising to CP	0.0464	0.0464	0.0464	0.0464
TI ↑	setup_rising to CP	0.0265	0.0265	0.0222	0.0265
		X29_P4	X34_P4		
CP ↓	min_pulse_width to CP	0.0456	0.0456		
CP ↑	min_pulse_width to CP	0.0363	0.0349		
D ↓	hold_rising to CP	-0.0196	-0.0196		
D ↑	hold_rising to CP	-0.0018	-0.0018		
D ↓	setup_rising to CP	0.0494	0.0494		
D ↑	setup_rising to CP	0.0299	0.0299		
E ↓	hold_rising to CP	-0.0240	-0.0240		
E ↑	hold_rising to CP	-0.0045	-0.0045		
E ↓	setup_rising to CP	0.0688	0.0661		
E ↑	setup_rising to CP	0.0488	0.0488		
RN ↓	min_pulse_width to RN	0.0398	0.0376		
RN ↑	recovery_rising to CP	-0.0017	-0.0017		
RN ↑	removal_rising to CP	0.0090	0.0090		
TE ↓	hold_rising to CP	-0.0094	-0.0094		
TE ↑	hold_rising to CP	0.0004	0.0004		
TE ↓	setup_rising to CP	0.0386	0.0386		
TE ↑	setup_rising to CP	0.0471	0.0471		
TI ↓	hold_rising to CP	-0.0169	-0.0166		
TI ↑	hold_rising to CP	0.0025	0.0025		
TI ↓	setup_rising to CP	0.0464	0.0464		
TI ↑	setup_rising to CP	0.0265	0.0222		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X5_P4	3.619e-04	1.000e-20
X10_P4	4.427e-04	1.000e-20
X19_P4	5.827e-04	1.000e-20
X23_P4	6.059e-04	1.000e-20

X29_P4	7.596e-04	1.000e-20
X34_P4	8.005e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

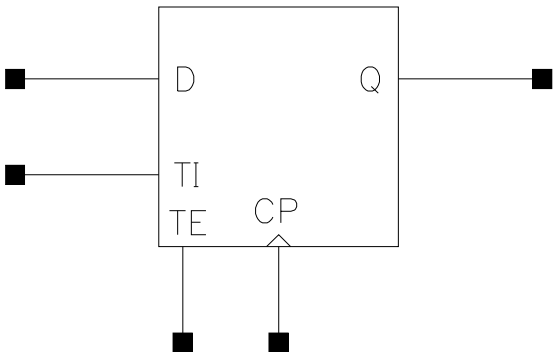
Pin Cycle	X5_P4	X10_P4	X19_P4	X23_P4
Clock 100Mhz Data 0Mhz	1.025e-02	1.026e-02	1.026e-02	1.027e-02
Clock 100Mhz Data 25Mhz	1.082e-02	1.137e-02	1.256e-02	1.267e-02
Clock 100Mhz Data 50Mhz	1.139e-02	1.247e-02	1.486e-02	1.508e-02
Clock = 0 Data 100Mhz	6.339e-03	6.340e-03	6.339e-03	6.340e-03
Clock = 1 Data 100Mhz	2.406e-03	2.405e-03	2.405e-03	2.406e-03
	X29_P4	X34_P4		
Clock 100Mhz Data 0Mhz	1.027e-02	1.027e-02		
Clock 100Mhz Data 25Mhz	1.355e-02	1.380e-02		
Clock 100Mhz Data 50Mhz	1.684e-02	1.734e-02		
Clock = 0 Data 100Mhz	6.341e-03	6.340e-03		
Clock = 1 Data 100Mhz	2.407e-03	2.407e-03		

SDFPQ

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_SDFPQX5_P4	0.800	3.264	2.6112
C8T28SOI_LLHF_SDFPQX3_P4	0.800	3.264	2.6112
C8T28SOIDV_LL_SDFPQX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_SDFPQX10_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_SDFPQX19_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX23_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_SDFPQX29_P4	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQX5_P4	C8T28SOI_LLHF_-SDFPQX3_P4	C8T28SOIDV_LL_-SDFPQX5_P4	C8T28SOIDV_LL_-SDFPQX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0006	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQX19_P4	C8T28SOIDV_LL_-SDFPQX23_P4	C8T28SOIDV_LL_-SDFPQX29_P4	
CP	0.0005	0.0005	0.0005	
D	0.0005	0.0005	0.0005	
TE	0.0009	0.0009	0.0009	
TI	0.0003	0.0003	0.0003	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQX5_P4	**C8T28SOI_LLHF_-SDFPQX3_P4**	**C8T28SOI_LL_-SDFPQX5_P4**	**C8T28SOI_LLHF_-SDFPQX3_P4**
CP to Q ↓	0.0393	0.0334	2.6673	4.0462
CP to Q ↑	0.0388	0.0432	3.3425	4.9819
	C8T28SOIDV_LL_-SDFPQX5_P4	**C8T28SOIDV_LL_-SDFPQX10_P4**	**C8T28SOIDV_LL_-SDFPQX5_P4**	**C8T28SOIDV_LL_-SDFPQX10_P4**
CP to Q ↓	0.0359	0.0504	2.5472	1.2511
CP to Q ↑	0.0444	0.0630	3.3042	1.6614
	C8T28SOIDV_LL_-SDFPQX19_P4	**C8T28SOIDV_LL_-SDFPQX23_P4**	**C8T28SOIDV_LL_-SDFPQX19_P4**	**C8T28SOIDV_LL_-SDFPQX23_P4**
CP to Q ↓	0.0548	0.0562	0.6477	0.5044
CP to Q ↑	0.0673	0.0690	0.8373	0.8318
	C8T28SOIDV_LL_-SDFPQX29_P4		**C8T28SOIDV_LL_-SDFPQX29_P4**	
CP to Q ↓	0.0540		0.4346	
CP to Q ↑	0.0647		0.5571	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQX5_P4	C8T28SOI_-LLHF_-SDFPQX3_P4	C8T28SOIDV_-LL_SDFPQX5_-P4	C8T28SOIDV_-LL_SDFPQX10_-P4
CP ↓	min_pulse_width to CP	0.0584	0.0573	0.0470	0.0470
CP ↑	min_pulse_width to CP	0.0329	0.0271	0.0317	0.0303
D ↓	hold_rising to CP	-0.0196	-0.0474	0.0032	0.0032
D ↑	hold_rising to CP	0.0009	0.0033	0.0080	0.0080
D ↓	setup_rising to CP	0.0461	0.0828	0.0299	0.0299
D ↑	setup_rising to CP	0.0239	0.0266	0.0169	0.0169
TE ↓	hold_rising to CP	-0.0115	-0.0132	0.0048	0.0048
TE ↑	hold_rising to CP	0.0030	0.0028	0.0032	0.0032
TE ↓	setup_rising to CP	0.0445	0.0660	0.0296	0.0296
TE ↑	setup_rising to CP	0.0569	0.0733	0.0510	0.0510

TI ↓	hold_rising to CP	-0.0257	-0.0501	-0.0215	-0.0215
TI ↑	hold_rising to CP	0.0028	0.0039	0.0028	0.0028
TI ↓	setup_rising to CP	0.0555	0.0741	0.0513	0.0513
TI ↑	setup_rising to CP	0.0222	0.0208	0.0280	0.0237
		C8T28SOIDV_-LL_SDFPQX19_-P4	C8T28SOIDV_-LL_SDFPQX23_-P4	C8T28SOIDV_-LL_SDFPQX29_-P4	
CP ↓	min_pulse_width to CP	0.0470	0.0470	0.0488	
CP ↑	min_pulse_width to CP	0.0303	0.0317	0.0317	
D ↓	hold_rising to CP	0.0032	0.0032	0.0032	
D ↑	hold_rising to CP	0.0080	0.0080	0.0080	
D ↓	setup_rising to CP	0.0299	0.0299	0.0294	
D ↑	setup_rising to CP	0.0169	0.0169	0.0169	
TE ↓	hold_rising to CP	0.0048	0.0048	0.0048	
TE ↑	hold_rising to CP	0.0032	0.0032	0.0032	
TE ↓	setup_rising to CP	0.0296	0.0296	0.0296	
TE ↑	setup_rising to CP	0.0510	0.0510	0.0569	
TI ↓	hold_rising to CP	-0.0215	-0.0215	-0.0215	
TI ↑	hold_rising to CP	0.0028	0.0028	0.0028	
TI ↓	setup_rising to CP	0.0513	0.0513	0.0521	
TI ↑	setup_rising to CP	0.0237	0.0237	0.0237	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQX5_P4	3.059e-04	1.000e-20
C8T28SOI_LLHF_SDFPQX3_P4	2.657e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX5_P4	2.899e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX10_P4	4.037e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX19_P4	5.085e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX23_P4	5.310e-04	1.000e-20
C8T28SOIDV_LL_SDFPQX29_P4	6.823e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOI_LL_-SDFPQX5_P4	C8T28SOI_LLHF_-SDFPQX3_P4	C8T28SOIDV_LL_-SDFPQX5_P4	C8T28SOIDV_LL_-SDFPQX10_P4
Clock 100Mhz Data 0Mhz	1.040e-02	9.934e-03	9.464e-03	9.224e-03
Clock 100Mhz Data 25Mhz	1.016e-02	9.674e-03	9.378e-03	9.754e-03
Clock 100Mhz Data 50Mhz	9.913e-03	9.415e-03	9.292e-03	1.028e-02

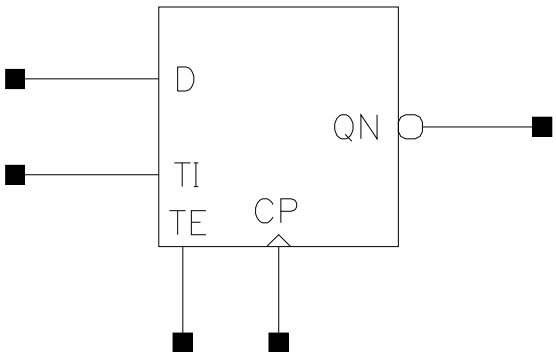
Clock = 0 Data 100Mhz	5.249e-03	5.510e-03	5.170e-03	4.996e-03
Clock = 1 Data 100Mhz	3.975e-05	6.393e-04	4.406e-04	3.412e-04
	C8T28SOIDV_LL_-SDFPQX19_P4	C8T28SOIDV_LL_-SDFPQX23_P4	C8T28SOIDV_LL_-SDFPQX29_P4	
Clock 100Mhz Data 0Mhz	9.084e-03	8.991e-03	8.925e-03	
Clock 100Mhz Data 25Mhz	1.059e-02	1.066e-02	1.141e-02	
Clock 100Mhz Data 50Mhz	1.210e-02	1.234e-02	1.390e-02	
Clock = 0 Data 100Mhz	4.890e-03	4.818e-03	4.770e-03	
Clock = 1 Data 100Mhz	2.817e-04	2.420e-04	2.136e-04	

SDFPQN

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNX5_P4	0.800	3.264	2.6112
C8T28SOI_LLHF_-SDFPQNX3_P4	0.800	3.400	2.7200
C8T28SOIDV_LL_-SDFPQNX5_P4	1.600	1.768	2.8288
C8T28SOIDV_LL_-SDFPQNX10_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNX19_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPQNX29_P4	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNX5_P4	C8T28SOI_LLHF_-SDFPQNX3_P4	C8T28SOIDV_LL_-SDFPQNX5_P4	C8T28SOIDV_LL_-SDFPQNX10_P4

CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0006	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNX19_P4	C8T28SOIDV_LL_-SDFPQNX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNX5_P4	**C8T28SOI_LLHF_-SDFPQNX3_P4**	**C8T28SOI_LL_-SDFPQNX5_P4**	**C8T28SOI_LLHF_-SDFPQNX3_P4**
CP to QN ↓	0.0490	0.0514	2.5996	3.8563
CP to QN ↑	0.0434	0.0408	3.5914	4.8369
	C8T28SOIDV_LL_-SDFPQNX5_P4	**C8T28SOIDV_LL_-SDFPQNX10_P4**	**C8T28SOIDV_LL_-SDFPQNX5_P4**	**C8T28SOIDV_LL_-SDFPQNX10_P4**
CP to QN ↓	0.0539	0.0517	2.5234	1.2608
CP to QN ↑	0.0412	0.0441	3.2680	1.6623
	C8T28SOIDV_LL_-SDFPQNX19_P4	**C8T28SOIDV_LL_-SDFPQNX29_P4**	**C8T28SOIDV_LL_-SDFPQNX19_P4**	**C8T28SOIDV_LL_-SDFPQNX29_P4**
CP to QN ↓	0.0581	0.0679	0.6533	0.4470
CP to QN ↑	0.0520	0.0589	0.8528	0.5605

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQNX5_P4	C8T28SOI_-LLHF_-SDFPQNX3_P4	C8T28SOIDV_-LL_SDFPQNX5_-P4	C8T28SOIDV_-LL_-SDFPQNX10_P4
CP ↓	min_pulse_width to CP	0.0584	0.0573	0.0470	0.0470
CP ↑	min_pulse_width to CP	0.0269	0.0271	0.0303	0.0317
D ↓	hold_rising to CP	-0.0196	-0.0474	0.0032	0.0032
D ↑	hold_rising to CP	0.0009	0.0033	0.0080	0.0080
D ↓	setup_rising to CP	0.0461	0.0828	0.0294	0.0299
D ↑	setup_rising to CP	0.0239	0.0266	0.0169	0.0169
TE ↓	hold_rising to CP	-0.0115	-0.0132	0.0048	0.0048
TE ↑	hold_rising to CP	0.0030	0.0028	0.0031	0.0032
TE ↓	setup_rising to CP	0.0445	0.0628	0.0296	0.0296
TE ↑	setup_rising to CP	0.0569	0.0738	0.0569	0.0510
TI ↓	hold_rising to CP	-0.0300	-0.0501	-0.0215	-0.0215
TI ↑	hold_rising to CP	0.0028	0.0039	0.0025	0.0028
TI ↓	setup_rising to CP	0.0555	0.0741	0.0528	0.0513
TI ↑	setup_rising to CP	0.0222	0.0208	0.0224	0.0280

		C8T28SOIDV_-LL_-SDFPQNX19_P4	C8T28SOIDV_-LL_-SDFPQNX29_P4		
CP ↓	min_pulse_width to CP	0.0470	0.0470		
CP ↑	min_pulse_width to CP	0.0317	0.0317		
D ↓	hold_rising to CP	0.0032	0.0032		
D ↑	hold_rising to CP	0.0080	0.0080		
D ↓	setup_rising to CP	0.0299	0.0299		
D ↑	setup_rising to CP	0.0169	0.0169		
TE ↓	hold_rising to CP	0.0048	0.0048		
TE ↑	hold_rising to CP	0.0032	0.0032		
TE ↓	setup_rising to CP	0.0296	0.0296		
TE ↑	setup_rising to CP	0.0510	0.0537		
TI ↓	hold_rising to CP	-0.0215	-0.0215		
TI ↑	hold_rising to CP	0.0028	0.0028		
TI ↓	setup_rising to CP	0.0513	0.0513		
TI ↑	setup_rising to CP	0.0237	0.0280		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQNX5_P4	3.023e-04	1.000e-20
C8T28SOI_LLHF_SDFPQNX3_P4	2.684e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNX5_P4	2.928e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNX10_P4	3.989e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNX19_P4	5.110e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNX29_P4	7.863e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle	C8T28SOI_LL_-SDFPQNX5_P4	C8T28SOI_LLHF_-SDFPQNX3_P4	C8T28SOIDV_LL_-SDFPQNX5_P4	C8T28SOIDV_LL_-SDFPQNX10_P4
Clock 100Mhz Data 0Mhz	1.040e-02	1.004e-02	9.542e-03	9.281e-03
Clock 100Mhz Data 25Mhz	9.993e-03	9.726e-03	9.288e-03	9.780e-03
Clock 100Mhz Data 50Mhz	9.588e-03	9.412e-03	9.033e-03	1.028e-02
Clock = 0 Data 100Mhz	5.248e-03	5.532e-03	5.191e-03	5.013e-03
Clock = 1 Data 100Mhz	3.943e-05	6.431e-04	4.429e-04	3.430e-04
	C8T28SOIDV_LL_-SDFPQNX19_P4	C8T28SOIDV_LL_-SDFPQNX29_P4		
Clock 100Mhz Data 0Mhz	9.129e-03	9.025e-03		

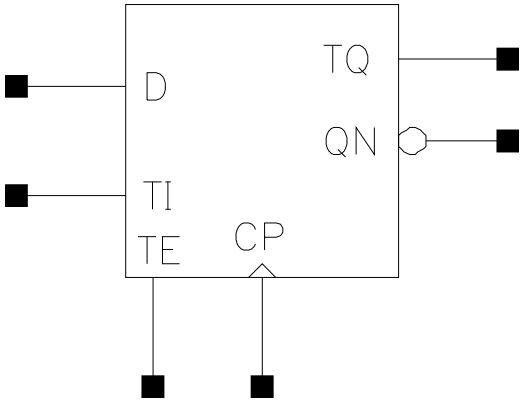
Clock 100Mhz Data 25Mhz	1.084e-02	1.196e-02		
Clock 100Mhz Data 50Mhz	1.256e-02	1.490e-02		
Clock = 0 Data 100Mhz	4.902e-03	4.832e-03		
Clock = 1 Data 100Mhz	2.831e-04	2.431e-04		

SDFPQNT

Cell Description

Positive edge triggered Scan D flip-flop; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQNTX5_P4	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQNTX3_P4	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQNTX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX10_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQNTX19_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQNTX29_P4	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI

-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQNTX5_P4	C8T28SOI_LLHF_-SDFPQNTX3_P4	C8T28SOIDV_LL_-SDFPQNTX5_P4	C8T28SOIDV_LL_-SDFPQNTX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0006	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQNTX19_P4	C8T28SOIDV_LL_-SDFPQNTX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPQNTX5_P4	**C8T28SOI_LLHF_-SDFPQNTX3_P4**	**C8T28SOI_LL_-SDFPQNTX5_P4**	**C8T28SOI_LLHF_-SDFPQNTX3_P4**
CP to QN ↓	0.0557	0.0563	2.6931	3.9081
CP to QN ↑	0.0543	0.0492	3.5970	4.8655
CP to TQ ↓	0.0440	0.0345	6.5583	4.5007
CP to TQ ↑	0.0477	0.0427	15.0568	8.2603
	C8T28SOIDV_LL_-SDFPQNTX5_P4	**C8T28SOIDV_LL_-SDFPQNTX10_P4**	**C8T28SOIDV_LL_-SDFPQNTX5_P4**	**C8T28SOIDV_LL_-SDFPQNTX10_P4**
CP to QN ↓	0.0580	0.0571	2.4803	1.2651
CP to QN ↑	0.0477	0.0482	3.2701	1.6657
CP to TQ ↓	0.0334	0.0346	4.5120	4.6753
CP to TQ ↑	0.0440	0.0450	6.6959	6.9369
	C8T28SOIDV_LL_-SDFPQNTX19_P4	**C8T28SOIDV_LL_-SDFPQNTX29_P4**	**C8T28SOIDV_LL_-SDFPQNTX19_P4**	**C8T28SOIDV_LL_-SDFPQNTX29_P4**
CP to QN ↓	0.0592	0.0697	0.6509	0.4493
CP to QN ↑	0.0526	0.0625	0.8469	0.5598
CP to TQ ↓	0.0359	0.0348	4.6140	4.7188
CP to TQ ↑	0.0464	0.0467	7.1247	8.7713

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQNTX5_P4	C8T28SOI_-LLHF_-SDFPQNTX3_P4	C8T28SOIDV_-LL_-SDFPQNTX5_P4	C8T28SOIDV_-LL_-SDFPQNTX10_-P4
CP ↓	min_pulse_width to CP	0.0584	0.0573	0.0470	0.0470
CP ↑	min_pulse_width to CP	0.0364	0.0318	0.0317	0.0317
D ↓	hold_rising to CP	-0.0196	-0.0480	0.0032	0.0032
D ↑	hold_rising to CP	0.0009	0.0033	0.0080	0.0080
D ↓	setup_rising to CP	0.0461	0.0828	0.0294	0.0299

D ↑	setup_rising to CP	0.0239	0.0266	0.0169	0.0169
TE ↓	hold_rising to CP	-0.0115	-0.0132	0.0048	0.0048
TE ↑	hold_rising to CP	0.0030	0.0028	0.0031	0.0032
TE ↓	setup_rising to CP	0.0445	0.0628	0.0296	0.0296
TE ↑	setup_rising to CP	0.0569	0.0738	0.0569	0.0510
TI ↓	hold_rising to CP	-0.0257	-0.0485	-0.0215	-0.0215
TI ↑	hold_rising to CP	0.0028	0.0039	0.0025	0.0028
TI ↓	setup_rising to CP	0.0555	0.0741	0.0528	0.0513
TI ↑	setup_rising to CP	0.0222	0.0208	0.0222	0.0280
		C8T28SOIDV_-LL_-SDFPQNTX19_-P4	C8T28SOIDV_-LL_-SDFPQNTX29_-P4		
CP ↓	min_pulse_width to CP	0.0470	0.0470		
CP ↑	min_pulse_width to CP	0.0363	0.0317		
D ↓	hold_rising to CP	0.0032	0.0032		
D ↑	hold_rising to CP	0.0080	0.0080		
D ↓	setup_rising to CP	0.0299	0.0299		
D ↑	setup_rising to CP	0.0169	0.0169		
TE ↓	hold_rising to CP	0.0048	0.0048		
TE ↑	hold_rising to CP	0.0032	0.0032		
TE ↓	setup_rising to CP	0.0296	0.0296		
TE ↑	setup_rising to CP	0.0510	0.0569		
TI ↓	hold_rising to CP	-0.0215	-0.0215		
TI ↑	hold_rising to CP	0.0028	0.0028		
TI ↓	setup_rising to CP	0.0513	0.0513		
TI ↑	setup_rising to CP	0.0237	0.0280		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQNTX5_P4	3.022e-04	1.000e-20
C8T28SOI_LLHF_SDFPQNTX3_P4	2.868e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNTX5_P4	3.128e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNTX10_P4	3.765e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNTX19_P4	5.057e-04	1.000e-20
C8T28SOIDV_LL_SDFPQNTX29_P4	7.871e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

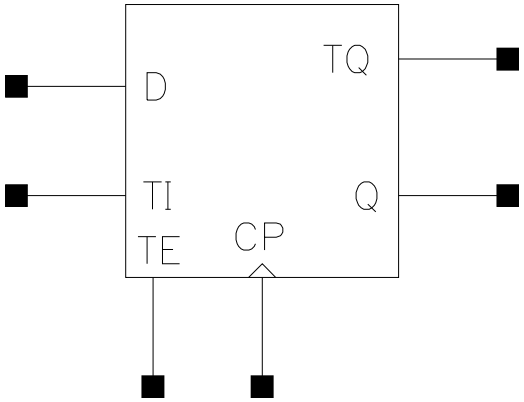
Pin Cycle	C8T28SOI_LL_-SDFPQNTX5_P4	C8T28SOI_LLHF_-SDFPQNTX3_P4	C8T28SOIDV_LL_-SDFPQNTX5_P4	C8T28SOIDV_LL_-SDFPQNTX10_P4
Clock 100Mhz Data 0Mhz	1.040e-02	1.004e-02	9.540e-03	9.279e-03
Clock 100Mhz Data 25Mhz	1.042e-02	1.007e-02	9.609e-03	9.798e-03
Clock 100Mhz Data 50Mhz	1.044e-02	1.010e-02	9.679e-03	1.032e-02
Clock = 0 Data 100Mhz	5.250e-03	5.531e-03	5.193e-03	5.014e-03
Clock = 1 Data 100Mhz	3.984e-05	6.459e-04	4.451e-04	3.446e-04
	C8T28SOIDV_LL_-SDFPQNTX19_P4	C8T28SOIDV_LL_-SDFPQNTX29_P4		
Clock 100Mhz Data 0Mhz	9.125e-03	9.017e-03		
Clock 100Mhz Data 25Mhz	1.076e-02	1.221e-02		
Clock 100Mhz Data 50Mhz	1.240e-02	1.540e-02		
Clock = 0 Data 100Mhz	4.906e-03	4.835e-03		
Clock = 1 Data 100Mhz	2.843e-04	2.442e-04		

SDFPQT

Cell Description

Positive edge triggered Scan D flip-flop; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPQTX5_P4	0.800	3.536	2.8288
C8T28SOI_LLHF_-SDFPQTX3_P4	0.800	3.536	2.8288
C8T28SOIDV_LL_-SDFPQTX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPQTX10_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPQTX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPQTX29_P4	1.600	2.312	3.6992

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

CP	TE	TI	E	D	IQ	IQ
/	0	-	1	D	-	D
/	0	-	0	-	IQ	IQ

/	1	TI	-	-	-	TI
-	-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPQTX5_P4	C8T28SOI_LLHF_-SDFPQTX3_P4	C8T28SOIDV_LL_-SDFPQTX5_P4	C8T28SOIDV_LL_-SDFPQTX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0006	0.0005	0.0005
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0004	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPQTX19_P4	C8T28SOIDV_LL_-SDFPQTX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPQTX5_P4	**C8T28SOI_LLHF_-SDFPQTX3_P4**	**C8T28SOI_LL_-SDFPQTX5_P4**	**C8T28SOI_LLHF_-SDFPQTX3_P4**
CP to Q ↓	0.0467	0.0424	2.8056	4.1737
CP to Q ↑	0.0426	0.0440	3.3664	5.0666
CP to TQ ↓	0.0528	0.0405	7.1683	4.6400
CP to TQ ↑	0.0527	0.0464	15.2839	8.4081
	C8T28SOIDV_LL_-SDFPQTX5_P4	**C8T28SOIDV_LL_-SDFPQTX10_P4**	**C8T28SOIDV_LL_-SDFPQTX5_P4**	**C8T28SOIDV_LL_-SDFPQTX10_P4**
CP to Q ↓	0.0390	0.0517	2.6048	1.2568
CP to Q ↑	0.0461	0.0643	3.3550	1.6634
CP to TQ ↓	0.0381	0.0530	4.6379	4.7244
CP to TQ ↑	0.0474	0.0667	7.2993	7.1810
	C8T28SOIDV_LL_-SDFPQTX19_P4	**C8T28SOIDV_LL_-SDFPQTX29_P4**	**C8T28SOIDV_LL_-SDFPQTX19_P4**	**C8T28SOIDV_LL_-SDFPQTX29_P4**
CP to Q ↓	0.0561	0.0603	0.6493	0.4251
CP to Q ↑	0.0680	0.0677	0.8407	0.5552
CP to TQ ↓	0.0579	0.0366	4.7655	4.8488
CP to TQ ↑	0.0717	0.0477	7.2033	8.7772

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPQTX5_P4	C8T28SOI_-LLHF_-SDFPQTX3_P4	C8T28SOIDV_-LL_SDFPQTX5_-P4	C8T28SOIDV_-LL_-SDFPQTX10_P4
CP ↓	min_pulse_width to CP	0.0584	0.0573	0.0470	0.0470
CP ↑	min_pulse_width to CP	0.0376	0.0330	0.0364	0.0303
D ↓	hold_rising to CP	-0.0196	-0.0474	0.0032	0.0032
D ↑	hold_rising to CP	0.0009	0.0033	0.0080	0.0080
D ↓	setup_rising to CP	0.0493	0.0828	0.0299	0.0299

D ↑	setup_rising to CP	0.0239	0.0266	0.0169	0.0169
TE ↓	hold_rising to CP	-0.0115	-0.0132	0.0048	0.0048
TE ↑	hold_rising to CP	0.0030	0.0028	0.0032	0.0032
TE ↓	setup_rising to CP	0.0445	0.0628	0.0296	0.0296
TE ↑	setup_rising to CP	0.0569	0.0738	0.0510	0.0510
TI ↓	hold_rising to CP	-0.0300	-0.0485	-0.0215	-0.0215
TI ↑	hold_rising to CP	0.0028	0.0039	0.0028	0.0028
TI ↓	setup_rising to CP	0.0555	0.0741	0.0513	0.0513
TI ↑	setup_rising to CP	0.0222	0.0208	0.0280	0.0237
		C8T28SOIDV_-LL_-SDFPQTX19_P4	C8T28SOIDV_-LL_-SDFPQTX29_P4		
CP ↓	min_pulse_width to CP	0.0470	0.0488		
CP ↑	min_pulse_width to CP	0.0303	0.0363		
D ↓	hold_rising to CP	0.0032	0.0032		
D ↑	hold_rising to CP	0.0080	0.0080		
D ↓	setup_rising to CP	0.0299	0.0294		
D ↑	setup_rising to CP	0.0169	0.0169		
TE ↓	hold_rising to CP	0.0048	0.0048		
TE ↑	hold_rising to CP	0.0032	0.0032		
TE ↓	setup_rising to CP	0.0296	0.0296		
TE ↑	setup_rising to CP	0.0510	0.0569		
TI ↓	hold_rising to CP	-0.0215	-0.0215		
TI ↑	hold_rising to CP	0.0028	0.0028		
TI ↓	setup_rising to CP	0.0513	0.0521		
TI ↑	setup_rising to CP	0.0280	0.0280		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPQTX5_P4	3.089e-04	1.000e-20
C8T28SOI_LLHF_SDFPQTX3_P4	2.868e-04	1.000e-20
C8T28SOIDV_LL_SDFPQTX5_P4	3.111e-04	1.000e-20
C8T28SOIDV_LL_SDFPQTX10_P4	4.240e-04	1.000e-20
C8T28SOIDV_LL_SDFPQTX19_P4	5.310e-04	1.000e-20
C8T28SOIDV_LL_SDFPQTX29_P4	7.110e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

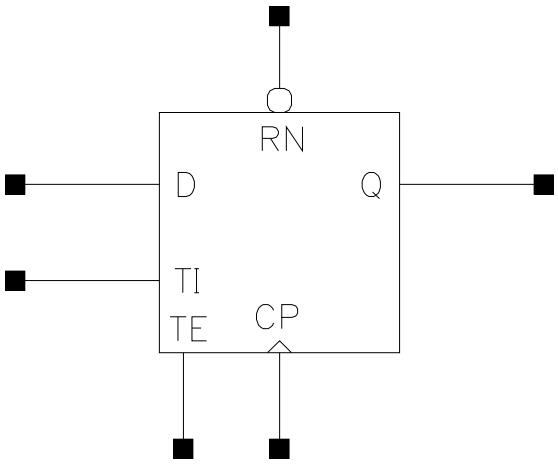
Pin Cycle	C8T28SOI_LL_-SDFPQTX5_P4	C8T28SOI_LLHF_-SDFPQTX3_P4	C8T28SOIDV_LL_-SDFPQTX5_P4	C8T28SOIDV_LL_-SDFPQTX10_P4
Clock 100Mhz Data 0Mhz	1.040e-02	1.005e-02	9.540e-03	9.280e-03
Clock 100Mhz Data 25Mhz	1.062e-02	1.018e-02	9.738e-03	1.003e-02
Clock 100Mhz Data 50Mhz	1.083e-02	1.032e-02	9.937e-03	1.078e-02
Clock = 0 Data 100Mhz	5.259e-03	5.539e-03	5.190e-03	5.011e-03
Clock = 1 Data 100Mhz	4.000e-05	6.449e-04	4.443e-04	3.441e-04
	C8T28SOIDV_LL_-SDFPQTX19_P4	C8T28SOIDV_LL_-SDFPQTX29_P4		
Clock 100Mhz Data 0Mhz	9.129e-03	9.032e-03		
Clock 100Mhz Data 25Mhz	1.095e-02	1.182e-02		
Clock 100Mhz Data 50Mhz	1.276e-02	1.461e-02		
Clock = 0 Data 100Mhz	4.902e-03	4.834e-03		
Clock = 1 Data 100Mhz	2.839e-04	2.439e-04		

SDFPRQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQX29_P4	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQX5_P4	C8T28SOI_LLHF_-SDFPRQX3_P4	C8T28SOIDV_LL_-SDFPRQX5_P4	C8T28SOIDV_LL_-SDFPRQX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0006	0.0005	0.0005
RN	0.0009	0.0008	0.0009	0.0010
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQX19_P4	C8T28SOIDV_LL_-SDFPRQX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0010	0.0009		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQX5_P4	**C8T28SOI_LLHF_-SDFPRQX3_P4**	**C8T28SOI_LL_-SDFPRQX5_P4**	**C8T28SOI_LLHF_-SDFPRQX3_P4**
CP to Q ↓	0.0443	0.0400	2.6786	4.0699
CP to Q ↑	0.0404	0.0434	3.3436	4.9255
RN to Q ↓	0.0329	0.0307	2.5622	3.9309
	C8T28SOIDV_LL_-SDFPRQX5_P4	**C8T28SOIDV_LL_-SDFPRQX10_P4**	**C8T28SOIDV_LL_-SDFPRQX5_P4**	**C8T28SOIDV_LL_-SDFPRQX10_P4**
CP to Q ↓	0.0363	0.0514	2.5491	1.2632
CP to Q ↑	0.0464	0.0656	3.3015	1.6651
RN to Q ↓	0.0369	0.0482	2.4739	1.2641
	C8T28SOIDV_LL_-SDFPRQX19_P4	**C8T28SOIDV_LL_-SDFPRQX29_P4**	**C8T28SOIDV_LL_-SDFPRQX19_P4**	**C8T28SOIDV_LL_-SDFPRQX29_P4**
CP to Q ↓	0.0552	0.0563	0.6489	0.4431
CP to Q ↑	0.0693	0.0717	0.8529	0.5811
RN to Q ↓	0.0517	0.0530	0.6489	0.4430

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQX5_P4	C8T28SOI_-LLHF_-SDFPRQX3_P4	C8T28SOIDV_-LL_SDFPRQX5_-P4	C8T28SOIDV_-LL_-SDFPRQX10_P4
CP ↓	min_pulse_width to CP	0.0584	0.0556	0.0488	0.0505
CP ↑	min_pulse_width to CP	0.0364	0.0318	0.0317	0.0317
D ↓	hold_rising to CP	-0.0164	-0.0425	0.0026	0.0026
D ↑	hold_rising to CP	-0.0023	-0.0026	0.0053	0.0053
D ↓	setup_rising to CP	0.0461	0.0774	0.0299	0.0294
D ↑	setup_rising to CP	0.0271	0.0266	0.0195	0.0195
RN ↓	min_pulse_width to RN	0.0425	0.0403	0.0398	0.0376
RN ↑	recovery_rising to CP	0.0006	0.0006	0.0006	0.0006
RN ↑	removal_rising to CP	0.0073	0.0074	0.0074	0.0074

TE ↓	hold_rising to CP	-0.0115	-0.0165	0.0048	0.0048
TE ↑	hold_rising to CP	-0.0002	0.0007	-0.0027	-0.0027
TE ↓	setup_rising to CP	0.0445	0.0633	0.0296	0.0296
TE ↑	setup_rising to CP	0.0569	0.0710	0.0520	0.0520
TI ↓	hold_rising to CP	-0.0266	-0.0442	-0.0218	-0.0218
TI ↑	hold_rising to CP	0.0028	0.0039	-0.0030	-0.0030
TI ↓	setup_rising to CP	0.0562	0.0748	0.0513	0.0513
TI ↑	setup_rising to CP	0.0280	0.0267	0.0278	0.0278
		C8T28SOIDV_-LL_-SDFPRQX19_P4	C8T28SOIDV_-LL_-SDFPRQX29_P4		
CP ↓	min_pulse_width to CP	0.0505	0.0505		
CP ↑	min_pulse_width to CP	0.0317	0.0317		
D ↓	hold_rising to CP	0.0026	0.0026		
D ↑	hold_rising to CP	0.0053	0.0053		
D ↓	setup_rising to CP	0.0294	0.0294		
D ↑	setup_rising to CP	0.0195	0.0195		
RN ↓	min_pulse_width to RN	0.0376	0.0376		
RN ↑	recovery_rising to CP	0.0006	0.0006		
RN ↑	removal_rising to CP	0.0074	0.0074		
TE ↓	hold_rising to CP	0.0048	0.0048		
TE ↑	hold_rising to CP	-0.0027	-0.0027		
TE ↓	setup_rising to CP	0.0296	0.0296		
TE ↑	setup_rising to CP	0.0520	0.0520		
TI ↓	hold_rising to CP	-0.0218	-0.0218		
TI ↑	hold_rising to CP	-0.0030	-0.0030		
TI ↓	setup_rising to CP	0.0513	0.0513		
TI ↑	setup_rising to CP	0.0278	0.0278		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQX5_P4	3.302e-04	1.000e-20
C8T28SOI_LLHF_SDFPRQX3_P4	2.927e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQX5_P4	3.198e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQX10_P4	4.275e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQX19_P4	5.534e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQX29_P4	7.096e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

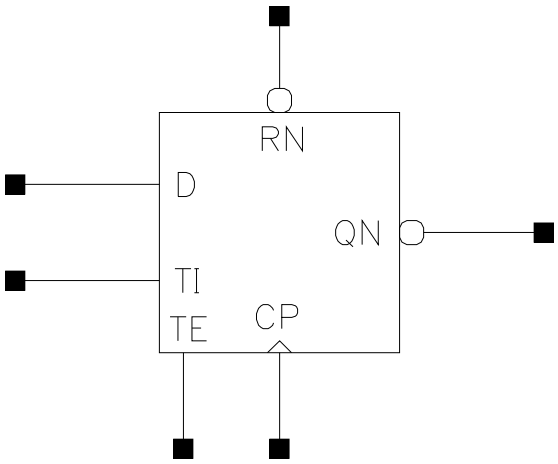
Pin Cycle	C8T28SOI_LL_-SDFPRQX5_P4	C8T28SOI_LLHF_-SDFPRQX3_P4	C8T28SOIDV_LL_-SDFPRQX5_P4	C8T28SOIDV_LL_-SDFPRQX10_P4
Clock 100Mhz Data 0Mhz	1.077e-02	1.030e-02	9.780e-03	9.519e-03
Clock 100Mhz Data 25Mhz	1.045e-02	1.001e-02	9.549e-03	9.970e-03
Clock 100Mhz Data 50Mhz	1.014e-02	9.726e-03	9.318e-03	1.042e-02
Clock = 0 Data 100Mhz	4.823e-03	5.154e-03	4.930e-03	4.819e-03
Clock = 1 Data 100Mhz	3.927e-05	6.479e-04	4.458e-04	3.449e-04
	C8T28SOIDV_LL_-SDFPRQX19_P4	C8T28SOIDV_LL_-SDFPRQX29_P4		
Clock 100Mhz Data 0Mhz	9.362e-03	9.258e-03		
Clock 100Mhz Data 25Mhz	1.079e-02	1.185e-02		
Clock 100Mhz Data 50Mhz	1.222e-02	1.444e-02		
Clock = 0 Data 100Mhz	4.752e-03	4.710e-03		
Clock = 1 Data 100Mhz	2.844e-04	2.442e-04		

SDFPRQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPRQNX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPRQNX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNX29_P4	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNX5_P4	C8T28SOI_LLHF_-SDFPRQNX3_P4	C8T28SOIDV_LL_-SDFPRQNX5_P4	C8T28SOIDV_LL_-SDFPRQNX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0006	0.0005	0.0005
RN	0.0009	0.0008	0.0009	0.0009
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNX19_P4	C8T28SOIDV_LL_-SDFPRQNX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNX5_P4	**C8T28SOI_LLHF_-SDFPRQNX3_P4**	**C8T28SOI_LL_-SDFPRQNX5_P4**	**C8T28SOI_LLHF_-SDFPRQNX3_P4**
CP to QN ↓	0.0517	0.0538	2.6633	3.8650
CP to QN ↑	0.0473	0.0441	3.4388	4.8401
RN to QN ↑	0.0383	0.0369	3.4415	4.8309
	C8T28SOIDV_LL_-SDFPRQNX5_P4	**C8T28SOIDV_LL_-SDFPRQNX10_P4**	**C8T28SOIDV_LL_-SDFPRQNX5_P4**	**C8T28SOIDV_LL_-SDFPRQNX10_P4**
CP to QN ↓	0.0583	0.0539	2.4713	1.2651
CP to QN ↑	0.0452	0.0446	3.2618	1.6653
RN to QN ↑	0.0417	0.0442	3.2642	1.6628
	C8T28SOIDV_LL_-SDFPRQNX19_P4	**C8T28SOIDV_LL_-SDFPRQNX29_P4**	**C8T28SOIDV_LL_-SDFPRQNX19_P4**	**C8T28SOIDV_LL_-SDFPRQNX29_P4**
CP to QN ↓	0.0600	0.0641	0.6626	0.4450
CP to QN ↑	0.0498	0.0553	0.8575	0.5783
RN to QN ↑	0.0471	0.0494	0.8568	0.5772

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNX5_-P4	C8T28SOI_-LLHF_-SDFPRQNX3_-P4	C8T28SOIDV_-LL_-SDFPRQNX5_-P4	C8T28SOIDV_-LL_-SDFPRQNX10_-P4
CP ↓	min_pulse_width to CP	0.0584	0.0573	0.0505	0.0505
CP ↑	min_pulse_width to CP	0.0317	0.0271	0.0317	0.0316
D ↓	hold_rising to CP	-0.0164	-0.0425	0.0026	0.0026
D ↑	hold_rising to CP	0.0009	-0.0026	0.0053	0.0053
D ↓	setup_rising to CP	0.0461	0.0774	0.0299	0.0294
D ↑	setup_rising to CP	0.0271	0.0266	0.0195	0.0195
RN ↓	min_pulse_width to RN	0.0403	0.0403	0.0376	0.0398
RN ↑	recovery_rising to CP	0.0006	0.0006	0.0006	0.0006

RN ↑	removal_rising to CP	0.0073	0.0074	0.0074	0.0074
TE ↓	hold_rising to CP	-0.0115	-0.0165	0.0048	0.0048
TE ↑	hold_rising to CP	-0.0002	0.0007	-0.0027	-0.0027
TE ↓	setup_rising to CP	0.0445	0.0633	0.0296	0.0296
TE ↑	setup_rising to CP	0.0543	0.0710	0.0520	0.0520
TI ↓	hold_rising to CP	-0.0264	-0.0452	-0.0218	-0.0218
TI ↑	hold_rising to CP	0.0028	0.0039	-0.0030	-0.0030
TI ↓	setup_rising to CP	0.0562	0.0748	0.0513	0.0513
TI ↑	setup_rising to CP	0.0280	0.0267	0.0278	0.0278
		C8T28SOIDV_-LL_-SDFPRQNX19_-P4	C8T28SOIDV_-LL_-SDFPRQNX29_-P4		
CP ↓	min_pulse_width to CP	0.0518	0.0518		
CP ↑	min_pulse_width to CP	0.0316	0.0363		
D ↓	hold_rising to CP	0.0053	0.0053		
D ↑	hold_rising to CP	0.0053	0.0053		
D ↓	setup_rising to CP	0.0299	0.0294		
D ↑	setup_rising to CP	0.0195	0.0195		
RN ↓	min_pulse_width to RN	0.0398	0.0518		
RN ↑	recovery_rising to CP	-0.0027	-0.0027		
RN ↑	removal_rising to CP	0.0069	0.0069		
TE ↓	hold_rising to CP	0.0070	0.0070		
TE ↑	hold_rising to CP	-0.0027	-0.0027		
TE ↓	setup_rising to CP	0.0296	0.0296		
TE ↑	setup_rising to CP	0.0520	0.0520		
TI ↓	hold_rising to CP	-0.0175	-0.0166		
TI ↑	hold_rising to CP	-0.0030	-0.0030		
TI ↓	setup_rising to CP	0.0513	0.0513		
TI ↑	setup_rising to CP	0.0278	0.0278		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQNX5_P4	3.138e-04	1.000e-20
C8T28SOI_LLHF_SDFPRQNX3_P4	2.888e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNX5_P4	3.046e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNX10_P4	4.125e-04	1.000e-20

C8T28SOIDV_LL_SDFPRQNX19_P4	4.945e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNX29_P4	6.422e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

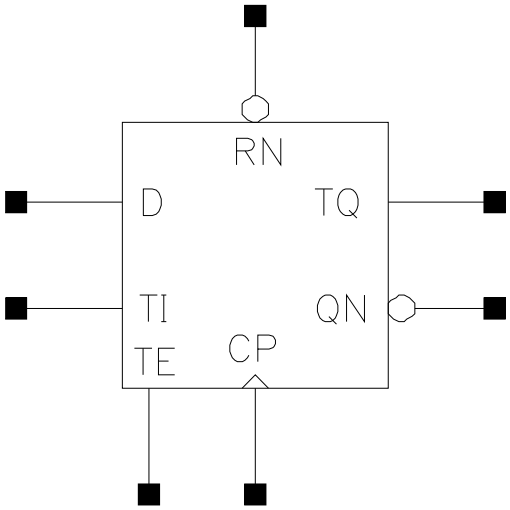
Pin Cycle	C8T28SOI_LL_-SDFPRQNX5_P4	C8T28SOI_LLHF_-SDFPRQNX3_P4	C8T28SOIDV_LL_-SDFPRQNX5_P4	C8T28SOIDV_LL_-SDFPRQNX10_P4
Clock 100Mhz Data 0Mhz	1.076e-02	1.028e-02	9.767e-03	9.510e-03
Clock 100Mhz Data 25Mhz	1.026e-02	9.903e-03	9.532e-03	1.000e-02
Clock 100Mhz Data 50Mhz	9.760e-03	9.527e-03	9.298e-03	1.049e-02
Clock = 0 Data 100Mhz	4.818e-03	5.148e-03	4.930e-03	4.819e-03
Clock = 1 Data 100Mhz	3.902e-05	6.477e-04	4.457e-04	3.448e-04
	C8T28SOIDV_LL_-SDFPRQNX19_P4	C8T28SOIDV_LL_-SDFPRQNX29_P4		
Clock 100Mhz Data 0Mhz	9.414e-03	9.377e-03		
Clock 100Mhz Data 25Mhz	1.093e-02	1.237e-02		
Clock 100Mhz Data 50Mhz	1.245e-02	1.536e-02		
Clock = 0 Data 100Mhz	4.750e-03	4.704e-03		
Clock = 1 Data 100Mhz	2.843e-04	2.440e-04		

SDFPRQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQNTX5_P4	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQNTX3_P4	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQNTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQNTX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQNTX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPRQNTX29_P4	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQNTX5_P4	C8T28SOI_LLHF_-SDFPRQNTX3_P4	C8T28SOIDV_LL_-SDFPRQNTX5_P4	C8T28SOIDV_LL_-SDFPRQNTX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0006	0.0005	0.0005
RN	0.0009	0.0008	0.0009	0.0010
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQNTX19_P4	C8T28SOIDV_LL_-SDFPRQNTX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0008	0.0008		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQNTX5_P4	**C8T28SOI_LLHF_-SDFPRQNTX3_P4**	**C8T28SOI_LL_-SDFPRQNTX5_P4**	**C8T28SOI_LLHF_-SDFPRQNTX3_P4**
CP to QN ↓	0.0576	0.0587	2.6210	3.9005
CP to QN ↑	0.0582	0.0529	3.5983	4.8665
CP to TQ ↓	0.0484	0.0379	6.8306	4.5361
CP to TQ ↑	0.0487	0.0448	15.0582	8.2814
RN to QN ↑	0.0464	0.0435	3.5978	4.8687
RN to TQ ↓	0.0372	0.0290	6.6813	4.4416
	C8T28SOIDV_LL_-SDFPRQNTX5_P4	**C8T28SOIDV_LL_-SDFPRQNTX10_P4**	**C8T28SOIDV_LL_-SDFPRQNTX5_P4**	**C8T28SOIDV_LL_-SDFPRQNTX10_P4**
CP to QN ↓	0.0614	0.0652	2.4997	1.2900
CP to QN ↑	0.0495	0.0527	3.2541	1.6529
CP to TQ ↓	0.0342	0.0346	4.5223	4.5458
CP to TQ ↑	0.0466	0.0466	6.7009	6.7067
RN to QN ↑	0.0463	0.0498	3.2553	1.6525
RN to TQ ↓	0.0360	0.0363	4.4362	4.4621
	C8T28SOIDV_LL_-SDFPRQNTX19_P4	**C8T28SOIDV_LL_-SDFPRQNTX29_P4**	**C8T28SOIDV_LL_-SDFPRQNTX19_P4**	**C8T28SOIDV_LL_-SDFPRQNTX29_P4**
CP to QN ↓	0.0627	0.0646	0.6517	0.4452
CP to QN ↑	0.0543	0.0599	0.8393	0.5731
CP to TQ ↓	0.0371	0.0448	4.5820	5.1314
CP to TQ ↑	0.0495	0.0555	6.7234	7.5794
RN to QN ↑	0.0503	0.0515	0.8401	0.5740
RN to TQ ↓	0.0362	0.0402	4.4826	4.9388

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQNTX5_-P4	C8T28SOI_-LLHF_-SDFPRQNTX3_-P4	C8T28SOIDV_-LL_-SDFPRQNTX5_-P4	C8T28SOIDV_-LL_SDF-PRQNTX10_P4
CP ↓	min_pulse_width to CP	0.0584	0.0573	0.0505	0.0505
CP ↑	min_pulse_width to CP	0.0376	0.0330	0.0316	0.0316
D ↓	hold_rising to CP	-0.0164	-0.0425	0.0026	0.0026
D ↑	hold_rising to CP	0.0009	-0.0026	0.0053	0.0053
D ↓	setup_rising to CP	0.0461	0.0774	0.0299	0.0294
D ↑	setup_rising to CP	0.0271	0.0266	0.0195	0.0195
RN ↓	min_pulse_width to RN	0.0447	0.0425	0.0425	0.0447
RN ↑	recovery_rising to CP	0.0006	0.0006	0.0006	0.0006
RN ↑	removal_rising to CP	0.0073	0.0074	0.0074	0.0074
TE ↓	hold_rising to CP	-0.0115	-0.0165	0.0048	0.0048
TE ↑	hold_rising to CP	-0.0002	0.0007	-0.0027	-0.0027
TE ↓	setup_rising to CP	0.0445	0.0607	0.0296	0.0296
TE ↑	setup_rising to CP	0.0543	0.0710	0.0520	0.0520
TI ↓	hold_rising to CP	-0.0266	-0.0452	-0.0218	-0.0218
TI ↑	hold_rising to CP	0.0028	0.0039	-0.0030	-0.0030
TI ↓	setup_rising to CP	0.0562	0.0748	0.0513	0.0513
TI ↑	setup_rising to CP	0.0280	0.0267	0.0278	0.0278
		C8T28SOIDV_-LL_SDF-PRQNTX19_P4	C8T28SOIDV_-LL_SDF-PRQNTX29_P4		
CP ↓	min_pulse_width to CP	0.0518	0.0518		
CP ↑	min_pulse_width to CP	0.0363	0.0409		
D ↓	hold_rising to CP	0.0053	0.0026		
D ↑	hold_rising to CP	0.0053	0.0053		
D ↓	setup_rising to CP	0.0299	0.0294		
D ↑	setup_rising to CP	0.0195	0.0195		
RN ↓	min_pulse_width to RN	0.0447	0.0544		
RN ↑	recovery_rising to CP	-0.0027	-0.0027		
RN ↑	removal_rising to CP	0.0069	0.0069		
TE ↓	hold_rising to CP	0.0070	0.0075		
TE ↑	hold_rising to CP	-0.0027	-0.0027		

TE ↓	setup_rising to CP	0.0296	0.0296		
TE ↑	setup_rising to CP	0.0520	0.0520		
TI ↓	hold_rising to CP	-0.0175	-0.0218		
TI ↑	hold_rising to CP	-0.0030	-0.0030		
TI ↓	setup_rising to CP	0.0513	0.0513		
TI ↑	setup_rising to CP	0.0278	0.0278		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQNTX5_P4	3.136e-04	1.000e-20
C8T28SOI_LLHF_SDFPRQNTX3_P4	3.060e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX5_P4	3.281e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX10_-P4	3.695e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX19_-P4	4.941e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQNTX29_-P4	6.612e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

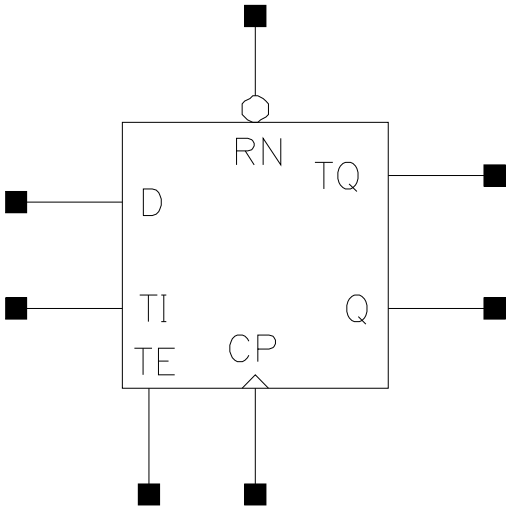
Pin Cycle	C8T28SOI_LL_-SDFPRQNTX5_P4	C8T28SOI_LLHF_-SDFPRQNTX3_P4	C8T28SOIDV_LL_-SDFPRQNTX5_P4	C8T28SOIDV_LL_-SDFPRQNTX10_P4
Clock 100Mhz Data 0Mhz	1.076e-02	1.028e-02	9.784e-03	9.522e-03
Clock 100Mhz Data 25Mhz	1.066e-02	1.026e-02	9.826e-03	1.013e-02
Clock 100Mhz Data 50Mhz	1.056e-02	1.023e-02	9.868e-03	1.074e-02
Clock = 0 Data 100Mhz	4.801e-03	5.145e-03	4.932e-03	4.821e-03
Clock = 1 Data 100Mhz	3.959e-05	6.500e-04	4.473e-04	3.461e-04
	C8T28SOIDV_LL_-SDFPRQNTX19_P4	C8T28SOIDV_LL_-SDFPRQNTX29_P4		
Clock 100Mhz Data 0Mhz	9.426e-03	9.352e-03		
Clock 100Mhz Data 25Mhz	1.102e-02	1.278e-02		
Clock 100Mhz Data 50Mhz	1.261e-02	1.621e-02		
Clock = 0 Data 100Mhz	4.753e-03	4.709e-03		
Clock = 1 Data 100Mhz	2.853e-04	2.448e-04		

SDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPRQTX5_P4	0.800	4.080	3.2640
C8T28SOI_LLHF_-SDFPRQTX3_P4	0.800	4.080	3.2640
C8T28SOIDV_LL_-SDFPRQTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPRQTX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPRQTX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPRQTX29_P4	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPRQTX5_P4	C8T28SOI_LLHF_-SDFPRQTX3_P4	C8T28SOIDV_LL_-SDFPRQTX5_P4	C8T28SOIDV_LL_-SDFPRQTX10_P4
CP	0.0007	0.0007	0.0005	0.0005
D	0.0005	0.0006	0.0005	0.0005
RN	0.0009	0.0008	0.0010	0.0009
TE	0.0010	0.0009	0.0009	0.0009
TI	0.0003	0.0005	0.0003	0.0003
	C8T28SOIDV_LL_-SDFPRQTX19_P4	C8T28SOIDV_LL_-SDFPRQTX29_P4		
CP	0.0005	0.0005		
D	0.0005	0.0005		
RN	0.0009	0.0009		
TE	0.0009	0.0009		
TI	0.0003	0.0003		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPRQTX5_P4	**C8T28SOI_LLHF_-SDFPRQTX3_P4**	**C8T28SOI_LL_-SDFPRQTX5_P4**	**C8T28SOI_LLHF_-SDFPRQTX3_P4**
CP to Q ↓	0.0522	0.0447	2.8349	4.1926
CP to Q ↑	0.0439	0.0456	3.3711	5.0707
CP to TQ ↓	0.0582	0.0426	7.2163	4.6618
CP to TQ ↑	0.0540	0.0479	15.1067	8.4200
RN to Q ↓	0.0386	0.0346	2.6775	4.0192
RN to TQ ↓	0.0446	0.0328	6.9725	4.5195
	C8T28SOIDV_LL_-SDFPRQTX5_P4	**C8T28SOIDV_LL_-SDFPRQTX10_P4**	**C8T28SOIDV_LL_-SDFPRQTX5_P4**	**C8T28SOIDV_LL_-SDFPRQTX10_P4**
CP to Q ↓	0.0394	0.0525	2.6228	1.2836
CP to Q ↑	0.0482	0.0666	3.3352	1.6610
CP to TQ ↓	0.0390	0.0542	4.6445	4.5614
CP to TQ ↑	0.0496	0.0691	6.8192	6.7672
RN to Q ↓	0.0384	0.0488	2.5369	1.2838
RN to TQ ↓	0.0384	0.0504	4.5396	4.5612
	C8T28SOIDV_LL_-SDFPRQTX19_P4	**C8T28SOIDV_LL_-SDFPRQTX29_P4**	**C8T28SOIDV_LL_-SDFPRQTX19_P4**	**C8T28SOIDV_LL_-SDFPRQTX29_P4**
CP to Q ↓	0.0587	0.0568	0.6712	0.4508
CP to Q ↑	0.0715	0.0719	0.8449	0.5778
CP to TQ ↓	0.0607	0.0578	4.6053	4.5052
CP to TQ ↑	0.0751	0.0751	6.7607	6.8895
RN to Q ↓	0.0556	0.0534	0.6710	0.4508
RN to TQ ↓	0.0576	0.0544	4.6058	4.5052

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPRQTX5_P4	C8T28SOI_-LLHF_-SDFPRQTX3_P4	C8T28SOIDV_-LL_-SDFPRQTX5_P4	C8T28SOIDV_-LL_-SDFPRQTX10_-P4
CP ↓	min_pulse_width to CP	0.0584	0.0573	0.0505	0.0505
CP ↑	min_pulse_width to CP	0.0423	0.0365	0.0316	0.0317
D ↓	hold_rising to CP	-0.0169	-0.0425	0.0026	0.0026
D ↑	hold_rising to CP	0.0009	-0.0026	0.0053	0.0053
D ↓	setup_rising to CP	0.0461	0.0774	0.0294	0.0294
D ↑	setup_rising to CP	0.0271	0.0266	0.0195	0.0195
RN ↓	min_pulse_width to RN	0.0469	0.0447	0.0447	0.0376
RN ↑	recovery_rising to CP	0.0006	0.0006	0.0006	0.0006
RN ↑	removal_rising to CP	0.0073	0.0074	0.0074	0.0074
TE ↓	hold_rising to CP	-0.0115	-0.0165	0.0048	0.0048
TE ↑	hold_rising to CP	-0.0002	0.0007	-0.0027	-0.0027
TE ↓	setup_rising to CP	0.0445	0.0633	0.0296	0.0296
TE ↑	setup_rising to CP	0.0543	0.0710	0.0520	0.0520
TI ↓	hold_rising to CP	-0.0266	-0.0452	-0.0218	-0.0218
TI ↑	hold_rising to CP	0.0028	0.0039	-0.0030	-0.0030
TI ↓	setup_rising to CP	0.0562	0.0748	0.0513	0.0513
TI ↑	setup_rising to CP	0.0280	0.0267	0.0278	0.0278
		C8T28SOIDV_-LL_-SDFPRQTX19_-P4	C8T28SOIDV_-LL_-SDFPRQTX29_-P4		
CP ↓	min_pulse_width to CP	0.0505	0.0505		
CP ↑	min_pulse_width to CP	0.0317	0.0317		
D ↓	hold_rising to CP	0.0026	0.0026		
D ↑	hold_rising to CP	0.0053	0.0053		
D ↓	setup_rising to CP	0.0294	0.0294		
D ↑	setup_rising to CP	0.0195	0.0195		
RN ↓	min_pulse_width to RN	0.0376	0.0376		
RN ↑	recovery_rising to CP	0.0006	0.0006		
RN ↑	removal_rising to CP	0.0074	0.0074		
TE ↓	hold_rising to CP	0.0048	0.0048		
TE ↑	hold_rising to CP	-0.0027	-0.0027		

TE ↓	setup_rising to CP	0.0296	0.0296		
TE ↑	setup_rising to CP	0.0520	0.0520		
TI ↓	hold_rising to CP	-0.0218	-0.0218		
TI ↑	hold_rising to CP	-0.0030	-0.0030		
TI ↓	setup_rising to CP	0.0513	0.0513		
TI ↑	setup_rising to CP	0.0278	0.0271		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPRQTX5_P4	3.341e-04	1.000e-20
C8T28SOI_LLHF_SDFPRQTX3_P4	3.110e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQTX5_P4	3.434e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQTX10_P4	4.465e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQTX19_P4	5.632e-04	1.000e-20
C8T28SOIDV_LL_SDFPRQTX29_P4	7.278e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

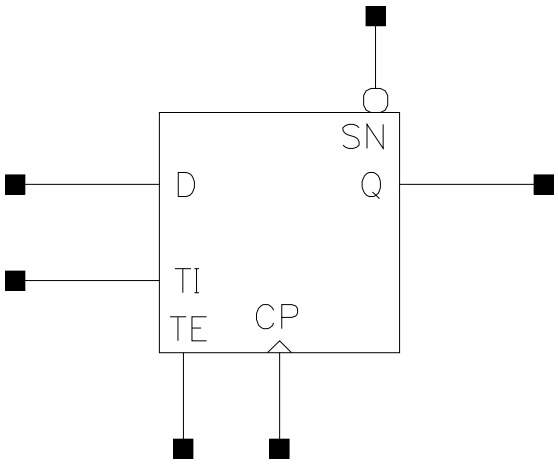
Pin Cycle	C8T28SOI_LL_-SDFPRQTX5_P4	C8T28SOI_LLHF_-SDFPRQTX3_P4	C8T28SOIDV_LL_-SDFPRQTX5_P4	C8T28SOIDV_LL_-SDFPRQTX10_P4
Clock 100Mhz Data 0Mhz	1.077e-02	1.029e-02	9.774e-03	9.515e-03
Clock 100Mhz Data 25Mhz	1.092e-02	1.035e-02	9.861e-03	1.026e-02
Clock 100Mhz Data 50Mhz	1.106e-02	1.041e-02	9.948e-03	1.101e-02
Clock = 0 Data 100Mhz	4.805e-03	5.148e-03	4.928e-03	4.818e-03
Clock = 1 Data 100Mhz	3.911e-05	6.502e-04	4.473e-04	3.459e-04
	C8T28SOIDV_LL_-SDFPRQTX19_P4	C8T28SOIDV_LL_-SDFPRQTX29_P4		
Clock 100Mhz Data 0Mhz	9.360e-03	9.256e-03		
Clock 100Mhz Data 25Mhz	1.117e-02	1.205e-02		
Clock 100Mhz Data 50Mhz	1.297e-02	1.484e-02		
Clock = 0 Data 100Mhz	4.752e-03	4.710e-03		
Clock = 1 Data 100Mhz	2.853e-04	2.449e-04		

SDFPSQ

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQX3_P4	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQX5_P4	1.600	1.904	3.0464
C8T28SOIDV_LL_-SDFPSQX10_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX14_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQX29_P4	1.600	2.584	4.1344

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQX5_P4	C8T28SOI_LLHF_-SDFPSQX3_P4	C8T28SOIDV_LL_-SDFPSQX5_P4	C8T28SOIDV_LL_-SDFPSQX10_P4
CP	0.0008	0.0007	0.0005	0.0006
D	0.0003	0.0005	0.0004	0.0004
SN	0.0014	0.0014	0.0010	0.0011
TE	0.0010	0.0009	0.0010	0.0010
TI	0.0004	0.0006	0.0005	0.0004
	C8T28SOIDV_LL_-SDFPSQX14_P4	C8T28SOIDV_LL_-SDFPSQX19_P4	C8T28SOIDV_LL_-SDFPSQX29_P4	
CP	0.0006	0.0006	0.0006	
D	0.0004	0.0004	0.0004	
SN	0.0010	0.0010	0.0011	
TE	0.0010	0.0010	0.0010	
TI	0.0004	0.0004	0.0004	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQX5_P4	**C8T28SOI_LLHF_-SDFPSQX3_P4**	**C8T28SOI_LL_-SDFPSQX5_P4**	**C8T28SOI_LLHF_-SDFPSQX3_P4**
CP to Q ↓	0.0460	0.0405	2.7232	4.1180
CP to Q ↑	0.0415	0.0443	3.3661	4.9328
SN to Q ↑	0.0278	0.0260	3.3024	4.8597
	C8T28SOIDV_LL_-SDFPSQX5_P4	**C8T28SOIDV_LL_-SDFPSQX10_P4**	**C8T28SOIDV_LL_-SDFPSQX5_P4**	**C8T28SOIDV_LL_-SDFPSQX10_P4**
CP to Q ↓	0.0358	0.0517	2.5405	1.2371
CP to Q ↑	0.0442	0.0694	3.2997	1.6549
SN to Q ↑	0.0257	0.0487	3.2701	1.6535
	C8T28SOIDV_LL_-SDFPSQX14_P4	**C8T28SOIDV_LL_-SDFPSQX19_P4**	**C8T28SOIDV_LL_-SDFPSQX14_P4**	**C8T28SOIDV_LL_-SDFPSQX19_P4**
CP to Q ↓	0.0522	0.0556	0.8537	0.6584
CP to Q ↑	0.0696	0.0724	1.1125	0.8361
SN to Q ↑	0.0489	0.0517	1.1115	0.8365
	C8T28SOIDV_LL_-SDFPSQX29_P4		**C8T28SOIDV_LL_-SDFPSQX29_P4**	
CP to Q ↓	0.0557		0.4461	
CP to Q ↑	0.0750		0.5561	
SN to Q ↑	0.0541		0.5564	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQX5_P4	C8T28SOI_-LLHF_-SDFPSQX3_P4	C8T28SOIDV_-LL_SDFPSQX5_-P4	C8T28SOIDV_-LL_-SDFPSQX10_P4
CP ↓	min_pulse_width to CP	0.0638	0.0669	0.0542	0.0543
CP ↑	min_pulse_width to CP	0.0411	0.0318	0.0317	0.0317
D ↓	hold_rising to CP	-0.0212	-0.0523	-0.0017	-0.0071
D ↑	hold_rising to CP	0.0004	0.0028	0.0080	0.0053
D ↓	setup_rising to CP	0.0542	0.0897	0.0369	0.0396
D ↑	setup_rising to CP	0.0244	0.0276	0.0195	0.0195

SN ↓	min_pulse_width to SN	0.0354	0.0305	0.0305	0.0305
SN ↑	recovery_rising to CP	-0.0027	0.0031	-0.0039	-0.0071
SN ↑	removal_rising to CP	0.0169	0.0190	0.0237	0.0237
TE ↓	hold_rising to CP	-0.0110	-0.0137	-0.0001	-0.0023
TE ↑	hold_rising to CP	0.0030	0.0028	0.0079	0.0031
TE ↓	setup_rising to CP	0.0484	0.0731	0.0347	0.0338
TE ↑	setup_rising to CP	0.0612	0.0840	0.0569	0.0569
TI ↓	hold_rising to CP	-0.0305	-0.0550	-0.0231	-0.0218
TI ↑	hold_rising to CP	0.0025	0.0055	0.0089	0.0025
TI ↓	setup_rising to CP	0.0662	0.0846	0.0563	0.0549
TI ↑	setup_rising to CP	0.0222	0.0211	0.0160	0.0222
		C8T28SOIDV_-LL_-SDFPSQX14_P4	C8T28SOIDV_-LL_-SDFPSQX19_P4	C8T28SOIDV_-LL_-SDFPSQX29_P4	
CP ↓	min_pulse_width to CP	0.0543	0.0543	0.0543	
CP ↑	min_pulse_width to CP	0.0317	0.0317	0.0317	
D ↓	hold_rising to CP	-0.0071	-0.0071	-0.0071	
D ↑	hold_rising to CP	0.0053	0.0053	0.0053	
D ↓	setup_rising to CP	0.0396	0.0396	0.0396	
D ↑	setup_rising to CP	0.0195	0.0195	0.0195	
SN ↓	min_pulse_width to SN	0.0305	0.0305	0.0305	
SN ↑	recovery_rising to CP	-0.0071	-0.0071	-0.0071	
SN ↑	removal_rising to CP	0.0237	0.0237	0.0237	
TE ↓	hold_rising to CP	-0.0023	-0.0023	-0.0023	
TE ↑	hold_rising to CP	0.0031	0.0031	0.0031	
TE ↓	setup_rising to CP	0.0338	0.0338	0.0338	
TE ↑	setup_rising to CP	0.0569	0.0569	0.0569	
TI ↓	hold_rising to CP	-0.0218	-0.0218	-0.0218	
TI ↑	hold_rising to CP	0.0025	0.0025	0.0025	
TI ↓	setup_rising to CP	0.0549	0.0549	0.0549	
TI ↑	setup_rising to CP	0.0222	0.0222	0.0222	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQX5_P4	3.262e-04	1.000e-20

C8T28SOI_LLHF_SDFPSQX3_P4	2.996e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX5_P4	3.149e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX10_P4	4.280e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX14_P4	4.813e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX19_P4	5.384e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQX29_P4	6.771e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

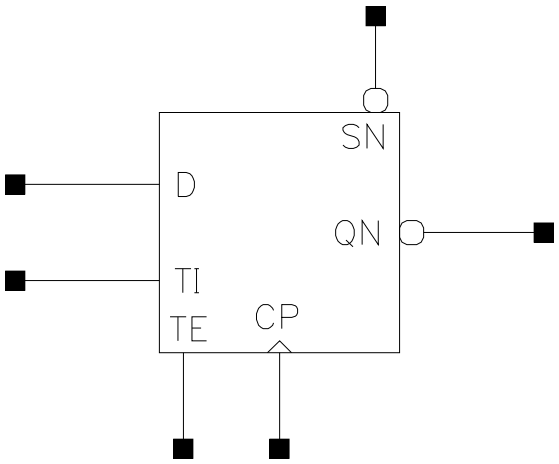
Pin Cycle	C8T28SOI_LL_-SDFPSQX5_P4	C8T28SOI_LLHF_-SDFPSQX3_P4	C8T28SOIDV_LL_-SDFPSQX5_P4	C8T28SOIDV_LL_-SDFPSQX10_P4
Clock 100Mhz Data 0Mhz	1.058e-02	1.003e-02	9.548e-03	9.305e-03
Clock 100Mhz Data 25Mhz	1.052e-02	9.907e-03	9.355e-03	9.934e-03
Clock 100Mhz Data 50Mhz	1.046e-02	9.785e-03	9.162e-03	1.056e-02
Clock = 0 Data 100Mhz	4.963e-03	5.315e-03	5.139e-03	5.086e-03
Clock = 1 Data 100Mhz	3.927e-05	6.442e-04	4.435e-04	3.437e-04
	C8T28SOIDV_LL_-SDFPSQX14_P4	C8T28SOIDV_LL_-SDFPSQX19_P4	C8T28SOIDV_LL_-SDFPSQX29_P4	
Clock 100Mhz Data 0Mhz	9.159e-03	9.062e-03	8.994e-03	
Clock 100Mhz Data 25Mhz	1.018e-02	1.076e-02	1.158e-02	
Clock 100Mhz Data 50Mhz	1.120e-02	1.245e-02	1.417e-02	
Clock = 0 Data 100Mhz	5.054e-03	5.033e-03	5.018e-03	
Clock = 1 Data 100Mhz	2.837e-04	2.438e-04	2.153e-04	

SDFPSQN

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNX5_P4	0.800	3.808	3.0464
C8T28SOI_LLHF_-SDFPSQNX3_P4	0.800	3.808	3.0464
C8T28SOIDV_LL_-SDFPSQNX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNX10_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX14_P4	1.600	2.176	3.4816
C8T28SOIDV_LL_-SDFPSQNX19_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX23_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNX29_P4	1.600	2.448	3.9168

Truth Table

IQ	QN
IQ	!IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNX5_P4	C8T28SOI_LLHF_-SDFPSQNX3_P4	C8T28SOIDV_LL_-SDFPSQNX5_P4	C8T28SOIDV_LL_-SDFPSQNX10_P4
CP	0.0008	0.0007	0.0005	0.0005
D	0.0003	0.0005	0.0004	0.0003
SN	0.0014	0.0014	0.0010	0.0011
TE	0.0010	0.0009	0.0010	0.0010
TI	0.0004	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQNX14_P4	C8T28SOIDV_LL_-SDFPSQNX19_P4	C8T28SOIDV_LL_-SDFPSQNX23_P4	C8T28SOIDV_LL_-SDFPSQNX29_P4
CP	0.0005	0.0005	0.0005	0.0005
D	0.0004	0.0004	0.0004	0.0004
SN	0.0011	0.0011	0.0011	0.0010
TE	0.0010	0.0010	0.0010	0.0010
TI	0.0005	0.0005	0.0005	0.0005

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNX5_P4	**C8T28SOI_LLHF_-SDFPSQNX3_P4**	**C8T28SOI_LL_-SDFPSQNX5_P4**	**C8T28SOI_LLHF_-SDFPSQNX3_P4**
CP to QN ↓	0.0542	0.0539	2.7350	3.8552
CP to QN ↑	0.0500	0.0459	3.4942	4.8399
SN to QN ↓	0.0407	0.0360	2.7345	3.8531
	C8T28SOIDV_LL_-SDFPSQNX5_P4	**C8T28SOIDV_LL_-SDFPSQNX10_P4**	**C8T28SOIDV_LL_-SDFPSQNX5_P4**	**C8T28SOIDV_LL_-SDFPSQNX10_P4**
CP to QN ↓	0.0580	0.0553	2.4608	1.2635
CP to QN ↑	0.0473	0.0482	3.2631	1.6363
SN to QN ↓	0.0387	0.0342	2.4590	1.2624
	C8T28SOIDV_LL_-SDFPSQNX14_P4	**C8T28SOIDV_LL_-SDFPSQNX19_P4**	**C8T28SOIDV_LL_-SDFPSQNX14_P4**	**C8T28SOIDV_LL_-SDFPSQNX19_P4**
CP to QN ↓	0.0573	0.0591	0.8368	0.6383
CP to QN ↑	0.0498	0.0518	1.0998	0.8273
SN to QN ↓	0.0355	0.0376	0.8362	0.6368
	C8T28SOIDV_LL_-SDFPSQNX23_P4	**C8T28SOIDV_LL_-SDFPSQNX29_P4**	**C8T28SOIDV_LL_-SDFPSQNX23_P4**	**C8T28SOIDV_LL_-SDFPSQNX29_P4**
CP to QN ↓	0.0601	0.0580	0.5116	0.4412
CP to QN ↑	0.0516	0.0523	0.8245	0.5554
SN to QN ↓	0.0383	0.0373	0.5109	0.4405

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNX5_-P4	C8T28SOI_-LLHF_-SDFPSQNX3_-P4	C8T28SOIDV_-LL_-SDFPSQNX5_-P4	C8T28SOIDV_-LL_-SDFPSQNX10_-P4
CP ↓	min_pulse_width to CP	0.0638	0.0669	0.0542	0.0559
CP ↑	min_pulse_width to CP	0.0316	0.0271	0.0317	0.0317
D ↓	hold_rising to CP	-0.0212	-0.0523	-0.0017	-0.0023
D ↑	hold_rising to CP	0.0004	0.0028	0.0079	0.0080
D ↓	setup_rising to CP	0.0542	0.0897	0.0369	0.0369

D ↑	setup_rising to CP	0.0244	0.0276	0.0195	0.0195
SN ↓	min_pulse_width to SN	0.0327	0.0305	0.0305	0.0305
SN ↑	recovery_rising to CP	-0.0027	0.0032	-0.0071	-0.0039
SN ↑	removal_rising to CP	0.0169	0.0190	0.0237	0.0237
TE ↓	hold_rising to CP	-0.0110	-0.0137	-0.0001	-0.0001
TE ↑	hold_rising to CP	0.0030	0.0028	0.0079	0.0079
TE ↓	setup_rising to CP	0.0484	0.0731	0.0347	0.0347
TE ↑	setup_rising to CP	0.0612	0.0840	0.0569	0.0569
TI ↓	hold_rising to CP	-0.0305	-0.0550	-0.0231	-0.0231
TI ↑	hold_rising to CP	0.0025	0.0039	0.0089	0.0089
TI ↓	setup_rising to CP	0.0662	0.0846	0.0563	0.0563
TI ↑	setup_rising to CP	0.0222	0.0211	0.0160	0.0160
		C8T28SOIDV_-LL_-SDFPSQNX14_-P4	C8T28SOIDV_-LL_-SDFPSQNX19_-P4	C8T28SOIDV_-LL_-SDFPSQNX23_-P4	C8T28SOIDV_-LL_-SDFPSQNX29_-P4
CP ↓	min_pulse_width to CP	0.0559	0.0559	0.0559	0.0542
CP ↑	min_pulse_width to CP	0.0317	0.0317	0.0349	0.0363
D ↓	hold_rising to CP	-0.0023	-0.0023	-0.0023	-0.0017
D ↑	hold_rising to CP	0.0080	0.0080	0.0080	0.0079
D ↓	setup_rising to CP	0.0369	0.0369	0.0369	0.0369
D ↑	setup_rising to CP	0.0195	0.0195	0.0195	0.0195
SN ↓	min_pulse_width to SN	0.0305	0.0305	0.0332	0.0332
SN ↑	recovery_rising to CP	-0.0071	-0.0039	-0.0039	-0.0039
SN ↑	removal_rising to CP	0.0237	0.0237	0.0237	0.0237
TE ↓	hold_rising to CP	-0.0001	-0.0001	-0.0001	-0.0001
TE ↑	hold_rising to CP	0.0079	0.0079	0.0079	0.0079
TE ↓	setup_rising to CP	0.0347	0.0347	0.0348	0.0347
TE ↑	setup_rising to CP	0.0569	0.0569	0.0569	0.0569
TI ↓	hold_rising to CP	-0.0231	-0.0231	-0.0231	-0.0231
TI ↑	hold_rising to CP	0.0089	0.0089	0.0089	0.0089
TI ↓	setup_rising to CP	0.0563	0.0563	0.0563	0.0563
TI ↑	setup_rising to CP	0.0160	0.0160	0.0160	0.0160

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQNX5_P4	3.389e-04	1.000e-20
C8T28SOI_LLHF_SDFPSQNX3_P4	3.057e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX5_P4	3.328e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX10_P4	4.544e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX14_P4	5.113e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX19_P4	5.807e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX23_P4	5.975e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNX29_P4	7.616e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

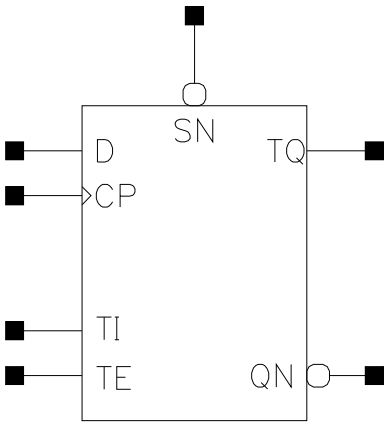
Pin Cycle	C8T28SOI_LL_-SDFPSQNX5_P4	C8T28SOI_LLHF_-SDFPSQNX3_P4	C8T28SOIDV_LL_-SDFPSQNX5_P4	C8T28SOIDV_LL_-SDFPSQNX10_P4
Clock 100Mhz Data 0Mhz	1.057e-02	1.002e-02	9.539e-03	9.385e-03
Clock 100Mhz Data 25Mhz	1.026e-02	9.767e-03	9.435e-03	1.012e-02
Clock 100Mhz Data 50Mhz	9.960e-03	9.517e-03	9.332e-03	1.086e-02
Clock = 0 Data 100Mhz	4.960e-03	5.314e-03	5.139e-03	5.051e-03
Clock = 1 Data 100Mhz	3.968e-05	6.452e-04	4.442e-04	3.437e-04
	C8T28SOIDV_LL_-SDFPSQNX14_P4	C8T28SOIDV_LL_-SDFPSQNX19_P4	C8T28SOIDV_LL_-SDFPSQNX23_P4	C8T28SOIDV_LL_-SDFPSQNX29_P4
Clock 100Mhz Data 0Mhz	9.292e-03	9.230e-03	9.187e-03	9.116e-03
Clock 100Mhz Data 25Mhz	1.045e-02	1.091e-02	1.107e-02	1.186e-02
Clock 100Mhz Data 50Mhz	1.160e-02	1.258e-02	1.295e-02	1.461e-02
Clock = 0 Data 100Mhz	4.997e-03	4.962e-03	4.937e-03	4.920e-03
Clock = 1 Data 100Mhz	2.836e-04	2.434e-04	2.148e-04	1.934e-04

SDFPSQNT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having inverted output QN and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQNTX5_P4	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQNTX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQNTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQNTX10_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQNTX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX23_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQNTX29_P4	1.600	2.584	4.1344

Truth Table

IQ	QN
IQ	!IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQNTX5_P4	C8T28SOI_LLHF_-SDFPSQNTX3_P4	C8T28SOIDV_LL_-SDFPSQNTX5_P4	C8T28SOIDV_LL_-SDFPSQNTX10_P4
CP	0.0008	0.0007	0.0005	0.0005
D	0.0003	0.0005	0.0004	0.0004
SN	0.0014	0.0014	0.0010	0.0010
TE	0.0010	0.0009	0.0010	0.0010
TI	0.0004	0.0006	0.0005	0.0005
	C8T28SOIDV_LL_-SDFPSQNTX19_P4	C8T28SOIDV_LL_-SDFPSQNTX23_P4	C8T28SOIDV_LL_-SDFPSQNTX29_P4	
CP	0.0005	0.0005	0.0005	
D	0.0004	0.0004	0.0003	
SN	0.0010	0.0010	0.0010	
TE	0.0010	0.0010	0.0010	
TI	0.0005	0.0005	0.0005	

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-SDFPSQNTX5_P4	**C8T28SOI_LLHF_-SDFPSQNTX3_P4**	**C8T28SOI_LL_-SDFPSQNTX5_P4**	**C8T28SOI_LLHF_-SDFPSQNTX3_P4**
CP to QN ↓	0.0594	0.0580	2.7751	3.8905
CP to QN ↑	0.0578	0.0536	3.4441	4.8776
CP to TQ ↓	0.0471	0.0382	6.7422	4.5606
CP to TQ ↑	0.0495	0.0457	15.0528	8.2825
SN to QN ↓	0.0429	0.0380	2.7765	3.9000
SN to TQ ↑	0.0344	0.0271	15.0084	8.2401
	C8T28SOIDV_LL_-SDFPSQNTX5_P4	**C8T28SOIDV_LL_-SDFPSQNTX10_P4**	**C8T28SOIDV_LL_-SDFPSQNTX5_P4**	**C8T28SOIDV_LL_-SDFPSQNTX10_P4**
CP to QN ↓	0.0584	0.0561	2.5116	1.2584
CP to QN ↑	0.0488	0.0514	3.2711	1.6434
CP to TQ ↓	0.0344	0.0394	4.5621	4.6129
CP to TQ ↑	0.0447	0.0470	7.2003	7.2549
SN to QN ↓	0.0382	0.0361	2.5211	1.2582
SN to TQ ↑	0.0258	0.0274	7.1702	7.1971
	C8T28SOIDV_LL_-SDFPSQNTX19_P4	**C8T28SOIDV_LL_-SDFPSQNTX23_P4**	**C8T28SOIDV_LL_-SDFPSQNTX19_P4**	**C8T28SOIDV_LL_-SDFPSQNTX23_P4**
CP to QN ↓	0.0598	0.0614	0.6344	0.5103
CP to QN ↑	0.0554	0.0544	0.8301	0.8256
CP to TQ ↓	0.0393	0.0399	4.6098	4.6396
CP to TQ ↑	0.0470	0.0476	7.2556	7.2639
SN to QN ↓	0.0394	0.0406	0.6347	0.5105
SN to TQ ↑	0.0274	0.0277	7.2027	7.2083
	C8T28SOIDV_LL_-SDFPSQNTX29_P4		**C8T28SOIDV_LL_-SDFPSQNTX29_P4**	
CP to QN ↓	0.0612		0.4423	
CP to QN ↑	0.0562		0.5555	

CP to TQ ↓	0.0415		4.7186	
CP to TQ ↑	0.0507		8.2513	
SN to QN ↓	0.0395		0.4418	
SN to TQ ↑	0.0295		8.1696	

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQNTX5_-P4	C8T28SOI_-LLHF_-SDFPSQNTX3_-P4	C8T28SOIDV_-LL_-SDFPSQNTX5_-P4	C8T28SOIDV_-LL_SDFP-SQNTX10_P4
CP ↓	min_pulse_width to CP	0.0638	0.0669	0.0535	0.0542
CP ↑	min_pulse_width to CP	0.0376	0.0330	0.0317	0.0363
D ↓	hold_rising to CP	-0.0212	-0.0523	-0.0017	-0.0017
D ↑	hold_rising to CP	0.0004	0.0028	0.0079	0.0079
D ↓	setup_rising to CP	0.0538	0.0897	0.0369	0.0369
D ↑	setup_rising to CP	0.0244	0.0276	0.0195	0.0195
SN ↓	min_pulse_width to SN	0.0354	0.0305	0.0305	0.0332
SN ↑	recovery_rising to CP	0.0031	0.0031	-0.0071	-0.0043
SN ↑	removal_rising to CP	0.0169	0.0190	0.0237	0.0237
TE ↓	hold_rising to CP	-0.0110	-0.0137	-0.0001	-0.0001
TE ↑	hold_rising to CP	0.0030	0.0028	0.0079	0.0079
TE ↓	setup_rising to CP	0.0516	0.0731	0.0347	0.0347
TE ↑	setup_rising to CP	0.0640	0.0840	0.0569	0.0569
TI ↓	hold_rising to CP	-0.0305	-0.0550	-0.0231	-0.0231
TI ↑	hold_rising to CP	0.0025	0.0055	0.0089	0.0089
TI ↓	setup_rising to CP	0.0662	0.0846	0.0563	0.0563
TI ↑	setup_rising to CP	0.0222	0.0211	0.0160	0.0160
		C8T28SOIDV_-LL_SDFP-SQNTX19_P4	C8T28SOIDV_-LL_SDFP-SQNTX23_P4	C8T28SOIDV_-LL_SDFP-SQNTX29_P4	
CP ↓	min_pulse_width to CP	0.0542	0.0542	0.0542	
CP ↑	min_pulse_width to CP	0.0362	0.0363	0.0362	
D ↓	hold_rising to CP	-0.0017	-0.0017	-0.0017	
D ↑	hold_rising to CP	0.0079	0.0079	0.0079	
D ↓	setup_rising to CP	0.0369	0.0369	0.0369	
D ↑	setup_rising to CP	0.0195	0.0195	0.0195	
SN ↓	min_pulse_width to SN	0.0332	0.0332	0.0381	

SN ↑	recovery_rising to CP	-0.0039	-0.0039	-0.0039	
SN ↑	removal_rising to CP	0.0237	0.0237	0.0237	
TE ↓	hold_rising to CP	-0.0001	-0.0001	-0.0001	
TE ↑	hold_rising to CP	0.0079	0.0079	0.0079	
TE ↓	setup_rising to CP	0.0347	0.0347	0.0347	
TE ↑	setup_rising to CP	0.0569	0.0569	0.0569	
TI ↓	hold_rising to CP	-0.0231	-0.0231	-0.0231	
TI ↑	hold_rising to CP	0.0089	0.0089	0.0089	
TI ↓	setup_rising to CP	0.0563	0.0563	0.0563	
TI ↑	setup_rising to CP	0.0160	0.0160	0.0160	

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQNTX5_P4	3.364e-04	1.000e-20
C8T28SOI_LLHF_SDFPSQNTX3_P4	3.252e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX5_P4	3.568e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX10_P4	4.749e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX19_P4	6.037e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX23_P4	6.224e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQNTX29_P4	7.809e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

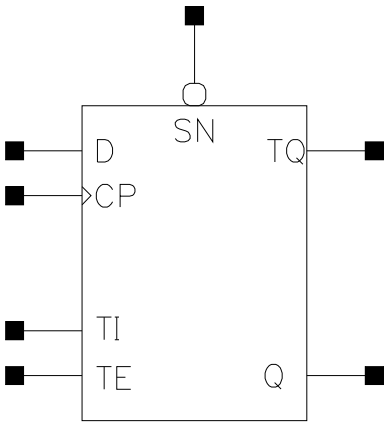
Pin Cycle	C8T28SOI_LL_-SDFPSQNTX5_P4	C8T28SOI_LLHF_-SDFPSQNTX3_P4	C8T28SOIDV_LL_-SDFPSQNTX5_P4	C8T28SOIDV_LL_-SDFPSQNTX10_P4
Clock 100Mhz Data 0Mhz	1.030e-02	9.882e-03	9.454e-03	9.239e-03
Clock 100Mhz Data 25Mhz	1.042e-02	1.003e-02	9.554e-03	1.029e-02
Clock 100Mhz Data 50Mhz	1.054e-02	1.018e-02	9.654e-03	1.133e-02
Clock = 0 Data 100Mhz	4.955e-03	5.312e-03	5.137e-03	5.050e-03
Clock = 1 Data 100Mhz	3.943e-05	6.435e-04	4.432e-04	3.430e-04
	C8T28SOIDV_LL_-SDFPSQNTX19_P4	C8T28SOIDV_LL_-SDFPSQNTX23_P4	C8T28SOIDV_LL_-SDFPSQNTX29_P4	
Clock 100Mhz Data 0Mhz	9.110e-03	9.024e-03	8.964e-03	
Clock 100Mhz Data 25Mhz	1.114e-02	1.129e-02	1.217e-02	
Clock 100Mhz Data 50Mhz	1.316e-02	1.356e-02	1.538e-02	
Clock = 0 Data 100Mhz	4.998e-03	4.963e-03	4.941e-03	
Clock = 1 Data 100Mhz	2.830e-04	2.431e-04	2.146e-04	

SDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-SDFPSQTX5_P4	0.800	3.944	3.1552
C8T28SOI_LLHF_-SDFPSQTX3_P4	0.800	3.944	3.1552
C8T28SOIDV_LL_-SDFPSQTX5_P4	1.600	2.040	3.2640
C8T28SOIDV_LL_-SDFPSQTX10_P4	1.600	2.312	3.6992
C8T28SOIDV_LL_-SDFPSQTX19_P4	1.600	2.448	3.9168
C8T28SOIDV_LL_-SDFPSQTX29_P4	1.600	2.720	4.3520

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D

-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOI_LL_-SDFPSQTX5_P4	C8T28SOI_LLHF_-SDFPSQTX3_P4	C8T28SOIDV_LL_-SDFPSQTX5_P4	C8T28SOIDV_LL_-SDFPSQTX10_P4
CP	0.0008	0.0007	0.0005	0.0006
D	0.0003	0.0005	0.0003	0.0004
SN	0.0014	0.0014	0.0010	0.0010
TE	0.0010	0.0009	0.0010	0.0010
TI	0.0004	0.0006	0.0005	0.0004
	C8T28SOIDV_LL_-SDFPSQTX19_P4	C8T28SOIDV_LL_-SDFPSQTX29_P4		
CP	0.0006	0.0006		
D	0.0004	0.0004		
SN	0.0010	0.0011		
TE	0.0010	0.0010		
TI	0.0004	0.0004		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOI_LL_-SDFPSQTX5_P4	**C8T28SOI_LLHF_-SDFPSQTX3_P4**	**C8T28SOI_LL_-SDFPSQTX5_P4**	**C8T28SOI_LLHF_-SDFPSQTX3_P4**
CP to Q ↓	0.0503	0.0452	2.8515	4.2325
CP to Q ↑	0.0441	0.0464	3.3683	5.0757
CP to TQ ↓	0.0562	0.0430	7.1440	4.6918
CP to TQ ↑	0.0544	0.0487	15.0834	8.4243
SN to Q ↑	0.0287	0.0271	3.3036	4.9924
SN to TQ ↑	0.0367	0.0285	15.0185	8.3682
	C8T28SOIDV_LL_-SDFPSQTX5_P4	**C8T28SOIDV_LL_-SDFPSQTX10_P4**	**C8T28SOIDV_LL_-SDFPSQTX5_P4**	**C8T28SOIDV_LL_-SDFPSQTX10_P4**
CP to Q ↓	0.0398	0.0512	2.6118	1.2714
CP to Q ↑	0.0465	0.0687	3.3481	1.6707
CP to TQ ↓	0.0396	0.0525	4.6409	4.7061
CP to TQ ↑	0.0472	0.0714	7.3008	7.1683
SN to Q ↑	0.0273	0.0481	3.3177	1.6704
SN to TQ ↑	0.0274	0.0507	7.2509	7.1623
	C8T28SOIDV_LL_-SDFPSQTX19_P4	**C8T28SOIDV_LL_-SDFPSQTX29_P4**	**C8T28SOIDV_LL_-SDFPSQTX19_P4**	**C8T28SOIDV_LL_-SDFPSQTX29_P4**
CP to Q ↓	0.0555	0.0622	0.6561	0.4372
CP to Q ↑	0.0728	0.0789	0.8579	0.5686
CP to TQ ↓	0.0552	0.0345	4.0769	4.1895
CP to TQ ↑	0.0761	0.0489	8.1957	8.2753
SN to Q ↑	0.0522	0.0561	0.8579	0.5697
SN to TQ ↑	0.0553	0.0281	8.1976	8.2484

Timing Constraints (ns) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin	Constraint	C8T28SOI_LL_-SDFPSQTX5_P4	C8T28SOI_-LLHF_-SDFPSQTX3_P4	C8T28SOIDV_-LL_-SDFPSQTX5_P4	C8T28SOIDV_-LL_-SDFPSQTX10_-P4
CP ↓	min_pulse_width to CP	0.0655	0.0669	0.0542	0.0543
CP ↑	min_pulse_width to CP	0.0424	0.0365	0.0364	0.0317
D ↓	hold_rising to CP	-0.0212	-0.0523	-0.0017	-0.0071
D ↑	hold_rising to CP	0.0004	0.0028	0.0080	0.0053
D ↓	setup_rising to CP	0.0538	0.0897	0.0369	0.0392
D ↑	setup_rising to CP	0.0244	0.0217	0.0195	0.0195
SN ↓	min_pulse_width to SN	0.0403	0.0332	0.0332	0.0305
SN ↑	recovery_rising to CP	0.0031	0.0031	-0.0039	-0.0071
SN ↑	removal_rising to CP	0.0169	0.0190	0.0237	0.0237
TE ↓	hold_rising to CP	-0.0110	-0.0137	-0.0001	-0.0023
TE ↑	hold_rising to CP	0.0030	0.0028	0.0079	0.0031
TE ↓	setup_rising to CP	0.0516	0.0731	0.0347	0.0371
TE ↑	setup_rising to CP	0.0640	0.0840	0.0569	0.0569
TI ↓	hold_rising to CP	-0.0305	-0.0550	-0.0231	-0.0218
TI ↑	hold_rising to CP	0.0025	0.0055	0.0089	0.0025
TI ↓	setup_rising to CP	0.0662	0.0846	0.0563	0.0565
TI ↑	setup_rising to CP	0.0222	0.0211	0.0160	0.0222
		C8T28SOIDV_-LL_-SDFPSQTX19_-P4	C8T28SOIDV_-LL_-SDFPSQTX29_-P4		
CP ↓	min_pulse_width to CP	0.0543	0.0543		
CP ↑	min_pulse_width to CP	0.0317	0.0317		
D ↓	hold_rising to CP	-0.0071	-0.0071		
D ↑	hold_rising to CP	0.0053	0.0079		
D ↓	setup_rising to CP	0.0396	0.0392		
D ↑	setup_rising to CP	0.0195	0.0195		
SN ↓	min_pulse_width to SN	0.0305	0.0332		
SN ↑	recovery_rising to CP	-0.0071	-0.0071		
SN ↑	removal_rising to CP	0.0237	0.0237		
TE ↓	hold_rising to CP	-0.0023	-0.0023		
TE ↑	hold_rising to CP	0.0031	0.0031		

TE ↓	setup_rising to CP	0.0338	0.0371		
TE ↑	setup_rising to CP	0.0569	0.0569		
TI ↓	hold_rising to CP	-0.0218	-0.0218		
TI ↑	hold_rising to CP	0.0025	0.0025		
TI ↓	setup_rising to CP	0.0549	0.0565		
TI ↑	setup_rising to CP	0.0222	0.0222		

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOI_LL_SDFPSQTX5_P4	3.267e-04	1.000e-20
C8T28SOI_LLHF_SDFPSQTX3_P4	3.188e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQTX5_P4	3.407e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQTX10_P4	4.523e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQTX19_P4	5.462e-04	1.000e-20
C8T28SOIDV_LL_SDFPSQTX29_P4	7.096e-04	1.000e-20

Internal Energy (uW/MHz) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

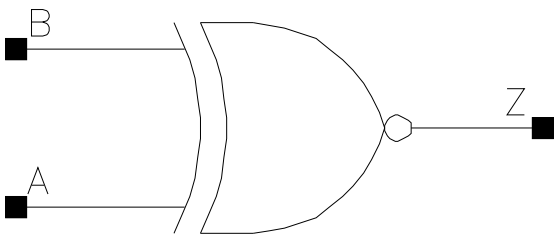
Pin Cycle	C8T28SOI_LL_-SDFPSQTX5_P4	C8T28SOI_LLHF_-SDFPSQTX3_P4	C8T28SOIDV_LL_-SDFPSQTX5_P4	C8T28SOIDV_LL_-SDFPSQTX10_P4
Clock 100Mhz Data 0Mhz	1.031e-02	9.891e-03	9.461e-03	9.240e-03
Clock 100Mhz Data 25Mhz	1.064e-02	1.017e-02	9.672e-03	1.006e-02
Clock 100Mhz Data 50Mhz	1.098e-02	1.044e-02	9.883e-03	1.088e-02
Clock = 0 Data 100Mhz	4.954e-03	5.310e-03	5.135e-03	5.096e-03
Clock = 1 Data 100Mhz	3.975e-05	6.441e-04	4.437e-04	3.438e-04
	C8T28SOIDV_LL_-SDFPSQTX19_P4	C8T28SOIDV_LL_-SDFPSQTX29_P4		
Clock 100Mhz Data 0Mhz	9.107e-03	9.020e-03		
Clock 100Mhz Data 25Mhz	1.095e-02	1.196e-02		
Clock 100Mhz Data 50Mhz	1.279e-02	1.490e-02		
Clock = 0 Data 100Mhz	5.063e-03	5.040e-03		
Clock = 1 Data 100Mhz	2.839e-04	2.440e-04		

XNOR2

Cell Description

2 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X4_P4	1.600	0.544	0.8704
X5_P4	0.800	1.496	1.1968
X8_P4	1.600	1.088	1.7408
X9_P4	0.800	1.632	1.3056
X11_P4	1.600	1.360	2.1760
X14_P4	0.800	2.312	1.8496
X15_P4	1.600	1.904	3.0464
X19_P4	0.800	2.448	1.9584

Truth Table

A	B	Z
0	B	!B
1	B	B

Pin Capacitance

Pin	X4_P4	X5_P4	X8_P4	X9_P4
A	0.0010	0.0006	0.0017	0.0007
B	0.0009	0.0010	0.0014	0.0012
	X11_P4	X14_P4	X15_P4	X19_P4
A	0.0025	0.0010	0.0030	0.0012
B	0.0022	0.0016	0.0026	0.0019

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X4_P4	X5_P4	X4_P4	X5_P4
A to Z ↓	0.0122	0.0334	3.3462	2.6374
A to Z ↑	0.0139	0.0317	4.6150	3.5363
B to Z ↓	0.0112	0.0250	3.3502	2.6285
B to Z ↑	0.0154	0.0236	4.6293	3.5339

	X8_P4	X9_P4	X8_P4	X9_P4
A to Z ↓	0.0147	0.0320	1.7757	1.3552
A to Z ↑	0.0167	0.0310	2.4866	1.8076
B to Z ↓	0.0138	0.0244	1.7772	1.3531
B to Z ↑	0.0179	0.0236	2.4918	1.8075
	X11_P4	**X14_P4**	**X11_P4**	**X14_P4**
A to Z ↓	0.0139	0.0300	1.2422	0.9225
A to Z ↑	0.0153	0.0285	1.6179	1.1723
B to Z ↓	0.0125	0.0228	1.2432	0.9194
B to Z ↑	0.0163	0.0219	1.6224	1.1706
	X15_P4	**X19_P4**	**X15_P4**	**X19_P4**
A to Z ↓	0.0154	0.0282	0.9442	0.6878
A to Z ↑	0.0170	0.0276	1.2367	0.8731
B to Z ↓	0.0140	0.0222	0.9443	0.6860
B to Z ↑	0.0181	0.0216	1.2392	0.8714

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X4_P4	1.737e-04	1.000e-20
X5_P4	1.796e-04	1.000e-20
X8_P4	2.734e-04	1.000e-20
X9_P4	3.008e-04	1.000e-20
X11_P4	4.230e-04	1.000e-20
X14_P4	4.705e-04	1.000e-20
X15_P4	5.283e-04	1.000e-20
X19_P4	6.615e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X4_P4	X5_P4	X8_P4	X9_P4
A to Z	2.658e-03	5.252e-03	4.894e-03	7.877e-03
B to Z	2.610e-03	4.406e-03	4.868e-03	6.721e-03
	X11_P4	X14_P4	X15_P4	X19_P4
A to Z	7.215e-03	1.224e-02	9.590e-03	1.512e-02
B to Z	7.081e-03	1.024e-02	9.478e-03	1.292e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

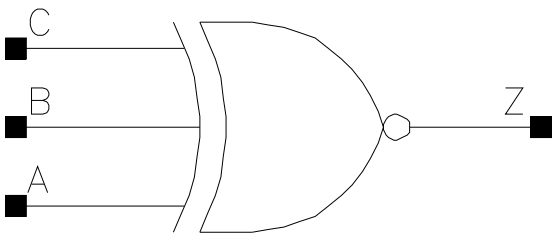
Pin Cycle (vdds)	X4_P4	X5_P4	X8_P4	X9_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X11_P4	X14_P4	X15_P4	X19_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XNOR3

Cell Description

3 input Exclusive NOR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XNOR3X2_P4	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X4_P4	1.600	1.360	2.1760
C8T28SOIDV_LL_-XNOR3X9_P4	1.600	1.496	2.3936
C8T28SOIDV_LL_-XNOR3X13_P4	1.600	2.040	3.2640
C8T28SOIDV_LLS_-XNOR3X1_P4	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X2_P4	1.600	1.088	1.7408
C8T28SOIDV_LLS_-XNOR3X5_P4	1.600	2.448	3.9168
C8T28SOIDV_LLS_-XNOR3X7_P4	1.600	2.992	4.7872

Truth Table

A	B	C	Z
A	A	C	!C
A	!A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XNOR3X2_P4	C8T28SOIDV_LL_-XNOR3X4_P4	C8T28SOIDV_LL_-XNOR3X9_P4	C8T28SOIDV_LL_-XNOR3X13_P4
A	0.0016	0.0016	0.0020	0.0027
B	0.0016	0.0015	0.0019	0.0026
C	0.0007	0.0007	0.0007	0.0007
	C8T28SOIDV_LLS_-XNOR3X1_P4	C8T28SOIDV_LLS_-XNOR3X2_P4	C8T28SOIDV_LLS_-XNOR3X5_P4	C8T28SOIDV_LLS_-XNOR3X7_P4

A	0.0016	0.0018	0.0039	0.0058
B	0.0016	0.0018	0.0035	0.0054
C	0.0011	0.0013	0.0025	0.0037

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XNOR3X2_P4	**C8T28SOIDV_LL_-XNOR3X4_P4**	**C8T28SOIDV_LL_-XNOR3X2_P4**	**C8T28SOIDV_LL_-XNOR3X4_P4**
A to Z ↓	0.0330	0.0351	5.1780	2.8418
A to Z ↑	0.0321	0.0330	6.2332	3.5775
B to Z ↓	0.0339	0.0361	5.1801	2.8420
B to Z ↑	0.0330	0.0340	6.2430	3.5794
C to Z ↓	0.0462	0.0491	5.1764	2.8402
C to Z ↑	0.0454	0.0469	6.2402	3.5767
	C8T28SOIDV_LL_-XNOR3X9_P4	**C8T28SOIDV_LL_-XNOR3X13_P4**	**C8T28SOIDV_LL_-XNOR3X9_P4**	**C8T28SOIDV_LL_-XNOR3X13_P4**
A to Z ↓	0.0308	0.0354	1.4367	0.9841
A to Z ↑	0.0331	0.0384	1.7562	1.2274
B to Z ↓	0.0318	0.0365	1.4375	0.9844
B to Z ↑	0.0342	0.0397	1.7570	1.2273
C to Z ↓	0.0462	0.0555	1.4361	0.9842
C to Z ↑	0.0480	0.0587	1.7566	1.2269
	C8T28SOIDV_LLS_-XNOR3X1_P4	**C8T28SOIDV_LLS_-XNOR3X2_P4**	**C8T28SOIDV_LLS_-XNOR3X1_P4**	**C8T28SOIDV_LLS_-XNOR3X2_P4**
A to Z ↓	0.0204	0.0229	8.8200	4.9995
A to Z ↑	0.0213	0.0213	12.9700	7.0770
B to Z ↓	0.0213	0.0240	8.8434	5.0078
B to Z ↑	0.0222	0.0224	12.9726	7.0801
C to Z ↓	0.0211	0.0232	8.8697	5.0292
C to Z ↑	0.0219	0.0217	12.9840	7.0898
	C8T28SOIDV_LLS_-XNOR3X5_P4	**C8T28SOIDV_LLS_-XNOR3X7_P4**	**C8T28SOIDV_LLS_-XNOR3X5_P4**	**C8T28SOIDV_LLS_-XNOR3X7_P4**
A to Z ↓	0.0239	0.0206	2.4391	1.6834
A to Z ↑	0.0233	0.0200	3.5224	2.3589
B to Z ↓	0.0241	0.0205	2.4456	1.6894
B to Z ↑	0.0235	0.0200	3.5236	2.3611
C to Z ↓	0.0235	0.0203	2.4485	1.6929
C to Z ↑	0.0228	0.0194	3.5231	2.3618

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_XNOR3X2_P4	1.317e-04	1.000e-20
C8T28SOIDV_LL_XNOR3X4_P4	1.568e-04	1.000e-20
C8T28SOIDV_LL_XNOR3X9_P4	2.742e-04	1.000e-20
C8T28SOIDV_LL_XNOR3X13_P4	3.923e-04	1.000e-20
C8T28SOIDV_LLS_XNOR3X1_P4	8.614e-05	1.000e-20
C8T28SOIDV_LLS_XNOR3X2_P4	1.502e-04	1.000e-20
C8T28SOIDV_LLS_XNOR3X5_P4	3.467e-04	1.000e-20
C8T28SOIDV_LLS_XNOR3X7_P4	5.422e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XNOR3X2_P4	C8T28SOIDV_LL_-XNOR3X4_P4	C8T28SOIDV_LL_-XNOR3X9_P4	C8T28SOIDV_LL_-XNOR3X13_P4
A to Z	3.078e-03	3.839e-03	6.053e-03	1.005e-02
B to Z	3.071e-03	3.836e-03	6.102e-03	1.014e-02
C to Z	4.829e-03	5.637e-03	8.242e-03	1.337e-02
	C8T28SOIDV_LLS_-XNOR3X1_P4	C8T28SOIDV_LLS_-XNOR3X2_P4	C8T28SOIDV_LLS_-XNOR3X5_P4	C8T28SOIDV_LLS_-XNOR3X7_P4
A to Z	1.818e-03	2.693e-03	5.840e-03	8.119e-03
B to Z	1.815e-03	2.734e-03	5.968e-03	8.121e-03
C to Z	1.800e-03	2.711e-03	5.982e-03	8.150e-03

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

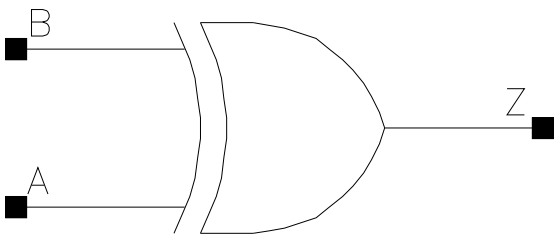
Pin Cycle (vdds)	C8T28SOIDV_LL_-XNOR3X2_P4	C8T28SOIDV_LL_-XNOR3X4_P4	C8T28SOIDV_LL_-XNOR3X9_P4	C8T28SOIDV_LL_-XNOR3X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XNOR3X1_P4	C8T28SOIDV_LLS_-XNOR3X2_P4	C8T28SOIDV_LLS_-XNOR3X5_P4	C8T28SOIDV_LLS_-XNOR3X7_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

XOR2

Cell Description

2 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X2_P4	0.800	1.360	1.0880
X4_P4	1.600	0.544	0.8704
X5_P4	0.800	1.360	1.0880
X8_P4	1.600	1.088	1.7408
X9_P4	0.800	1.496	1.1968
X12_P4	1.600	1.360	2.1760
X13_P4	0.800	2.176	1.7408
X15_P4	1.600	1.904	3.0464
X17_P4	0.800	2.312	1.8496
X18_P4	1.600	1.496	2.3936

Truth Table

A	B	Z
1	B	!B
0	B	B

Pin Capacitance

Pin	X2_P4	X4_P4	X5_P4	X8_P4
A	0.0005	0.0010	0.0007	0.0016
B	0.0010	0.0009	0.0011	0.0015
	X9_P4	X12_P4	X13_P4	X15_P4
A	0.0007	0.0026	0.0013	0.0031
B	0.0014	0.0020	0.0023	0.0024
	X17_P4	X18_P4		
A	0.0013	0.0017		
B	0.0023	0.0020		

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X2_P4	**X4_P4**	**X2_P4**	**X4_P4**
A to Z ↓	0.0284	0.0116	4.9744	2.6157
A to Z ↑	0.0284	0.0157	6.4090	6.0474
B to Z ↓	0.0225	0.0127	4.9385	2.6400
B to Z ↑	0.0227	0.0144	6.4042	6.0476
	X5_P4	**X8_P4**	**X5_P4**	**X8_P4**
A to Z ↓	0.0272	0.0151	2.7438	1.4228
A to Z ↑	0.0259	0.0189	3.4633	3.1982
B to Z ↓	0.0213	0.0169	2.7322	1.4394
B to Z ↑	0.0206	0.0177	3.4591	3.1977
	X9_P4	**X12_P4**	**X9_P4**	**X12_P4**
A to Z ↓	0.0270	0.0136	1.4290	0.9548
A to Z ↑	0.0266	0.0171	1.8098	2.1441
B to Z ↓	0.0213	0.0144	1.4237	0.9650
B to Z ↑	0.0209	0.0154	1.8072	2.1439
	X13_P4	**X15_P4**	**X13_P4**	**X15_P4**
A to Z ↓	0.0248	0.0147	0.9788	0.7459
A to Z ↑	0.0243	0.0197	1.2471	1.9057
B to Z ↓	0.0179	0.0153	0.9752	0.7542
B to Z ↑	0.0174	0.0177	1.2445	1.9045
	X17_P4	**X18_P4**	**X17_P4**	**X18_P4**
A to Z ↓	0.0263	0.0296	0.7389	0.7326
A to Z ↑	0.0255	0.0278	0.9331	0.8800
B to Z ↓	0.0194	0.0242	0.7370	0.7320
B to Z ↑	0.0187	0.0219	0.9318	0.8790

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
X2_P4	1.436e-04	1.000e-20
X4_P4	1.641e-04	1.000e-20
X5_P4	2.249e-04	1.000e-20
X8_P4	2.560e-04	1.000e-20
X9_P4	3.772e-04	1.000e-20
X12_P4	4.009e-04	1.000e-20
X13_P4	6.102e-04	1.000e-20
X15_P4	4.720e-04	1.000e-20
X17_P4	6.592e-04	1.000e-20
X18_P4	6.462e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	X2_P4	X4_P4	X5_P4	X8_P4
A to Z	3.813e-03	2.650e-03	4.958e-03	5.013e-03
B to Z	3.450e-03	2.588e-03	4.447e-03	4.988e-03
	X9_P4	X12_P4	X13_P4	X15_P4
A to Z	7.429e-03	7.203e-03	1.206e-02	9.100e-03
B to Z	6.794e-03	7.041e-03	9.352e-03	8.936e-03
	X17_P4	X18_P4		
A to Z	1.393e-02	1.559e-02		
B to Z	1.120e-02	1.323e-02		

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

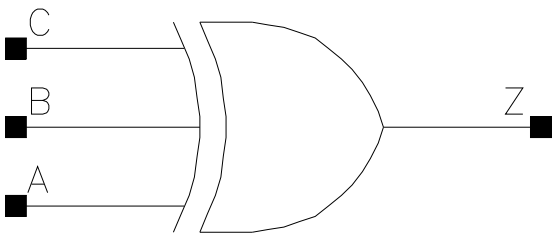
Pin Cycle (vdds)	X2_P4	X4_P4	X5_P4	X8_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X9_P4	X12_P4	X13_P4	X15_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X17_P4	X18_P4		
A to Z	0.000e+00	0.000e+00		
B to Z	0.000e+00	0.000e+00		

XOR3

Cell Description

3 input Exclusive OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL_-XOR3X2_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X4_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-XOR3X9_P4	1.600	1.360	2.1760
C8T28SOIDV_LL_-XOR3X13_P4	1.600	1.904	3.0464
C8T28SOIDV_LLS_-XOR3X1_P4	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X2_P4	1.600	1.224	1.9584
C8T28SOIDV_LLS_-XOR3X5_P4	1.600	2.584	4.1344
C8T28SOIDV_LLS_-XOR3X7_P4	1.600	3.264	5.2224

Truth Table

A	B	C	Z
A	!A	C	!C
A	A	C	C

Pin Capacitance

Pin	C8T28SOIDV_LL_-XOR3X2_P4	C8T28SOIDV_LL_-XOR3X4_P4	C8T28SOIDV_LL_-XOR3X9_P4	C8T28SOIDV_LL_-XOR3X13_P4
A	0.0017	0.0016	0.0019	0.0027
B	0.0016	0.0017	0.0019	0.0026
C	0.0010	0.0010	0.0013	0.0021
	C8T28SOIDV_LLS_-XOR3X1_P4	C8T28SOIDV_LLS_-XOR3X2_P4	C8T28SOIDV_LLS_-XOR3X5_P4	C8T28SOIDV_LLS_-XOR3X7_P4

A	0.0017	0.0018	0.0031	0.0048
B	0.0018	0.0018	0.0030	0.0049
C	0.0006	0.0006	0.0006	0.0010

Propagation Delay at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL_-XOR3X2_P4	**C8T28SOIDV_LL_-XOR3X4_P4**	**C8T28SOIDV_LL_-XOR3X2_P4**	**C8T28SOIDV_LL_-XOR3X4_P4**
A to Z ↓	0.0321	0.0354	5.2022	2.8516
A to Z ↑	0.0314	0.0339	6.4136	3.5818
B to Z ↓	0.0329	0.0366	5.2031	2.8532
B to Z ↑	0.0322	0.0352	6.4149	3.5829
C to Z ↓	0.0327	0.0363	5.2058	2.8534
C to Z ↑	0.0321	0.0349	6.4148	3.5842
	C8T28SOIDV_LL_-XOR3X9_P4	**C8T28SOIDV_LL_-XOR3X13_P4**	**C8T28SOIDV_LL_-XOR3X9_P4**	**C8T28SOIDV_LL_-XOR3X13_P4**
A to Z ↓	0.0330	0.0365	1.4259	0.9730
A to Z ↑	0.0338	0.0390	1.7687	1.1906
B to Z ↓	0.0342	0.0375	1.4262	0.9734
B to Z ↑	0.0350	0.0403	1.7702	1.1913
C to Z ↓	0.0336	0.0375	1.4267	0.9736
C to Z ↑	0.0344	0.0405	1.7701	1.1911
	C8T28SOIDV_LLS_-XOR3X1_P4	**C8T28SOIDV_LLS_-XOR3X2_P4**	**C8T28SOIDV_LLS_-XOR3X1_P4**	**C8T28SOIDV_LLS_-XOR3X2_P4**
A to Z ↓	0.0215	0.0238	6.3252	5.0971
A to Z ↑	0.0215	0.0212	9.4689	6.7773
B to Z ↓	0.0226	0.0247	6.3531	5.1051
B to Z ↑	0.0226	0.0221	9.4751	6.7782
C to Z ↓	0.0356	0.0383	6.2945	5.0674
C to Z ↑	0.0361	0.0362	9.4503	6.7473
	C8T28SOIDV_LLS_-XOR3X5_P4	**C8T28SOIDV_LLS_-XOR3X7_P4**	**C8T28SOIDV_LLS_-XOR3X5_P4**	**C8T28SOIDV_LLS_-XOR3X7_P4**
A to Z ↓	0.0317	0.0271	2.6561	1.8341
A to Z ↑	0.0272	0.0232	3.5505	2.4056
B to Z ↓	0.0308	0.0275	2.6649	1.8386
B to Z ↑	0.0271	0.0239	3.5552	2.4079
C to Z ↓	0.0535	0.0446	2.6555	1.8280
C to Z ↑	0.0498	0.0411	3.5405	2.3971

Average Leakage Power (mW) at 125C, 1.10V_0.00V_0.00V_0.00V, Best process

	vdd	vdds
C8T28SOIDV_LL_XOR3X2_P4	1.062e-04	1.000e-20
C8T28SOIDV_LL_XOR3X4_P4	1.353e-04	1.000e-20
C8T28SOIDV_LL_XOR3X9_P4	2.507e-04	1.000e-20
C8T28SOIDV_LL_XOR3X13_P4	3.662e-04	1.000e-20
C8T28SOIDV_LLS_XOR3X1_P4	1.513e-04	1.000e-20
C8T28SOIDV_LLS_XOR3X2_P4	1.811e-04	1.000e-20
C8T28SOIDV_LLS_XOR3X5_P4	3.035e-04	1.000e-20
C8T28SOIDV_LLS_XOR3X7_P4	4.638e-04	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdd)	C8T28SOIDV_LL_-XOR3X2_P4	C8T28SOIDV_LL_-XOR3X4_P4	C8T28SOIDV_LL_-XOR3X9_P4	C8T28SOIDV_LL_-XOR3X13_P4
A to Z	2.937e-03	3.831e-03	6.099e-03	1.044e-02
B to Z	2.925e-03	3.839e-03	6.151e-03	1.051e-02
C to Z	2.911e-03	3.817e-03	6.132e-03	1.053e-02
	C8T28SOIDV_LLS_-XOR3X1_P4	C8T28SOIDV_LLS_-XOR3X2_P4	C8T28SOIDV_LLS_-XOR3X5_P4	C8T28SOIDV_LLS_-XOR3X7_P4
A to Z	2.281e-03	2.771e-03	5.626e-03	7.848e-03
B to Z	2.286e-03	2.811e-03	5.778e-03	8.041e-03
C to Z	4.243e-03	4.837e-03	9.195e-03	1.281e-02

Internal Energy (uW/MHz) at Minimum Output Load, 125C, 1.10V_0.00V_0.00V_0.00V, Best process

Pin Cycle (vdds)	C8T28SOIDV_LL_-XOR3X2_P4	C8T28SOIDV_LL_-XOR3X4_P4	C8T28SOIDV_LL_-XOR3X9_P4	C8T28SOIDV_LL_-XOR3X13_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LLS_-XOR3X1_P4	C8T28SOIDV_LLS_-XOR3X2_P4	C8T28SOIDV_LLS_-XOR3X5_P4	C8T28SOIDV_LLS_-XOR3X7_P4
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

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