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C28SOI_SC_8_CLK_LL Databook

8 track Standard Cell Library comprising of cells for clock network (Balanced cells, Clock-gating cells) and Metastable tolerant Flip-flop

Overview

- C28SOI_SC_8_CLK_LL is a Standard Cell Library for CMOS028_FDSOI VLSI digital design platform.
- A portfolio of 388 cells.

Reading Standard Cell Datasheet

This chapter describes the components of the Datasheet for the cell.

2.1 Cell Category

The cell category field specifies the type of cell.The datasheets are presented alphabetically by the cell category.

2.2 Base Cell Name

The cell name field contains the cell name. The cell name presented here is the base cell name. The Cell Size table displays specific cell names for the different drives.

2.3 Cell Description

Functionality of the cell as well as cell specific attributes, characteristics and output pin equations, wherever applicable, are provided.

2.4 Functions

The function table gives all possible combinations of input and output signals for the cell. Table 2.1, ”Functions Key”, on page 2 defines the symbols used in datasheet function tables.

Symbol	Description
0	Logic Low
1	Logic High
/	Rising Edge
\	Falling Edge
-	No Change
↓	High to Low Transition
↑	Low to High Transition
x	Don't Care
IL	Illegal/Undefined
Z	High Impedance

Table 2.1: Functions Key

2.5 Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

2.6 Cell Size

The cell size table gives the height and width (μm) for each drive strength of the cell.

2.7 Functional Schematic

The functional schematic provides a functional representation of the cell.

2.8 Drive Strength

The drive strength of each cell is indicated by an X followed by the unit strength.

2.9 Pin Capacitance

The pin capacitance table shows the typical loading (pF) at the input pins of the cell for each drive strength of the cell.

2.10 Propagation Delay

The Propagation Delay through a cell is the sum of the intrinsic delay, the load dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal and the output stimulus crossing the threshold of 50% of V_{dd} for the rising signal and 50% of V_{dd} for the falling signal.

The propagation delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF).

Factors that affect propagation delay include: temperature, supply voltage, process variations, load, input transition time and input signal polarity. The timing models provided with this library include the effects of all these factors for three different combinations of supply voltage, process and temperature.

Figure 2.1 on page 3 illustrates the Propagation Delay Measurements.

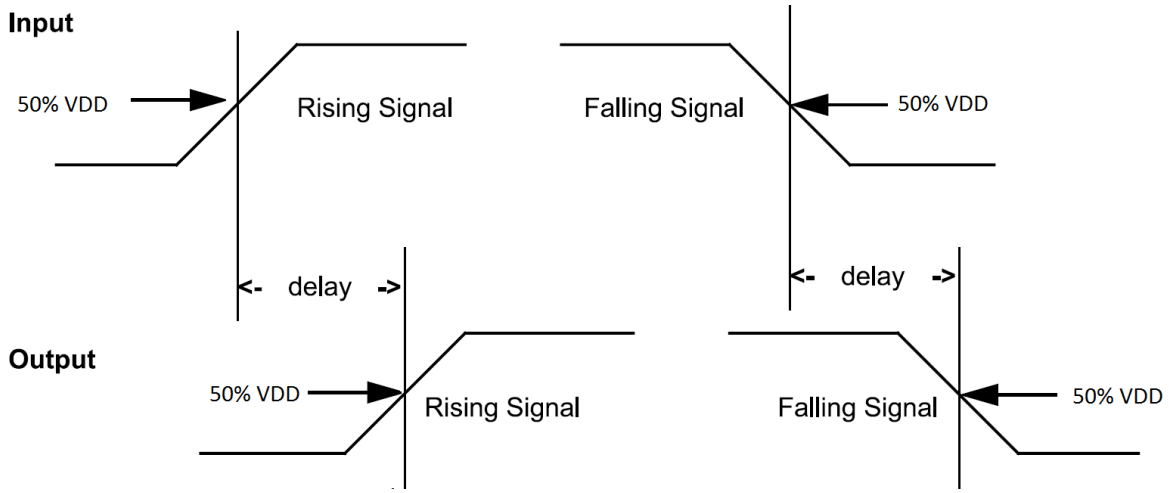


Figure 2.1: Thresholds for Propagation Delay Measurements

The intrinsic delays and load multiplier for each drive strength of the cell are calculated as a function of C(load in pF) and Transition time **0.020ns**.

2.11 Timing Constraints

Timing Constraints define the minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing Constraints include: setup time, hold time, recovery time, removal time and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time, data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for data slew and clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process variations.

Timing Constraints can affect propagation delays. The propagation delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, removal times and pulse widths). The use of shorter timing constraint intervals may increase the delay.

The timing constraints table in the datasheet shows the timing conditions (ns) required to maintain proper functionality. The Timing Constraints for each drive strength of the cell is measured as a function of input transition time(ns).

Timing Constraint values are measured for **0.020ns** data slew and **0.020ns** clock slew.

NOTE: All the Timing Constraints explained below are for flops triggered by rising clock edge. For falling edge triggered flops, the measurements are done with respect to the falling edge of clock crossing 50% of V_{dd}.

2.11.1 Setup Time

The Setup Time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as:

- The interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.
- The interval between the data signal crossing 50% of V_{dd} for the falling transition and the clock signal crossing 50% of V_{dd}.

For the measurement of setup time, the data-input signal is kept stable after the active clock edge for an infinite hold time.

Figure 2.2 on page 4 illustrates Setup Time for a sequential cell.

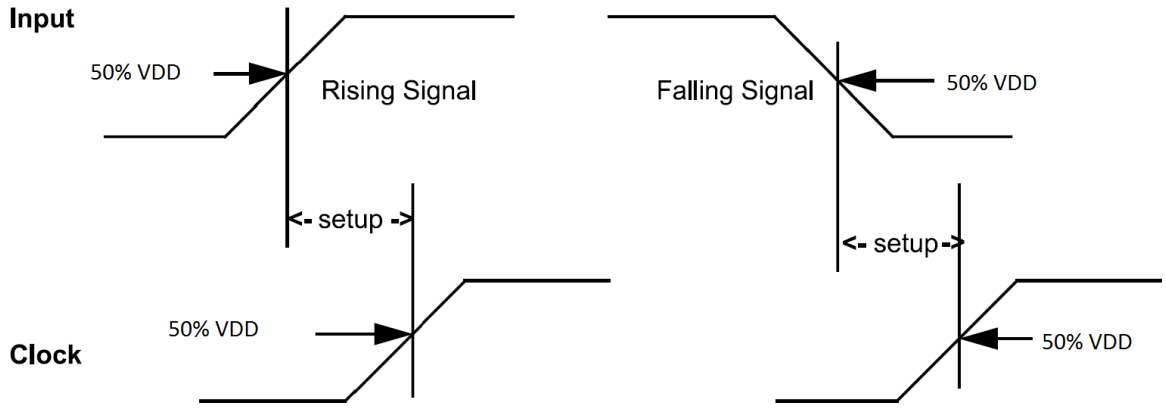


Figure 2.2: Setup Time

2.11.2 Hold Time

The Hold Time for a sequential cell is the minimum length of time the input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold constraint values are measured as:

- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.
- The interval between clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the falling transition.

For the measurement of Hold Time, the data-input signal is held stable before the active clock edge for an infinite Setup Time.

Figure 2.3 on page 5 illustrates Hold Time for a sequential cell.

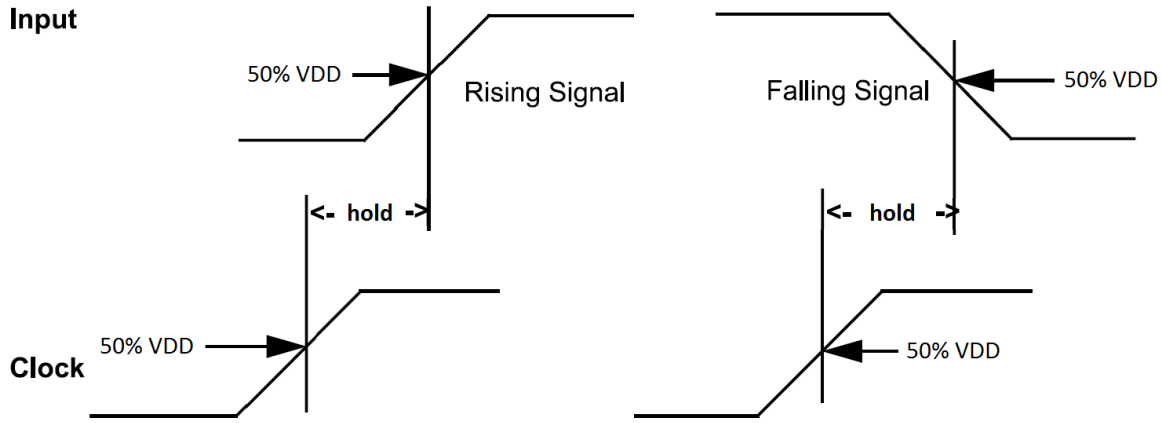


Figure 2.3: Hold Time

2.11.3 Recovery Time

Recovery Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for the rising transition and the clock signal crossing 50% of V_{dd}.

For the measurement of Recovery Time, the set or reset signal is held stable after the active clock edge for an infinite time.

Figure 2.4 on page 6 illustrates Recovery Time.

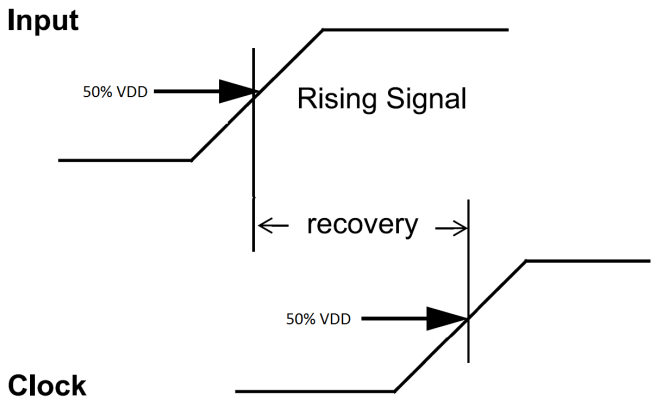


Figure 2.4: Recovery Time

2.11.4 Removal Time

Removal Time for a sequential cell is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Removal constraint values are measured as the interval between the clock signal crossing 50% of V_{dd} and the data signal crossing 50% of V_{dd} for the rising transition.

For the measurement of Removal Time, the set or reset signal is held stable before the active clock edge for an infinite time.

Figure 2.5 on page 7 illustrates Removal Time.

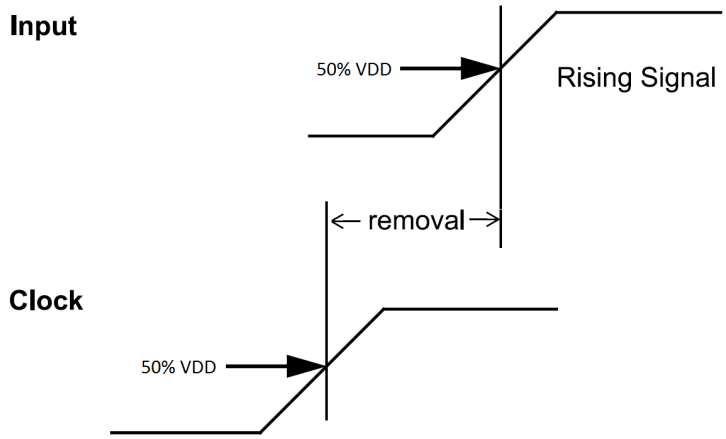


Figure 2.5: Removal Time

2.11.5 Minimum Pulse Width

Minimum Pulse Width is the minimum length of time between the leading and trailing edges of a pulse waveform (usually the clock signal) required to ensure the correct functioning of the cell. Minimum Pulse Width High (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of V_{dd} and the falling edge of the signal crossing 50% of V_{dd}. Minimum Pulse Width Low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of V_{dd} and the rising edge of the signal crossing 50% of V_{dd}.

Figure 2.6 on page 8 illustrates Minimum Pulse Width.

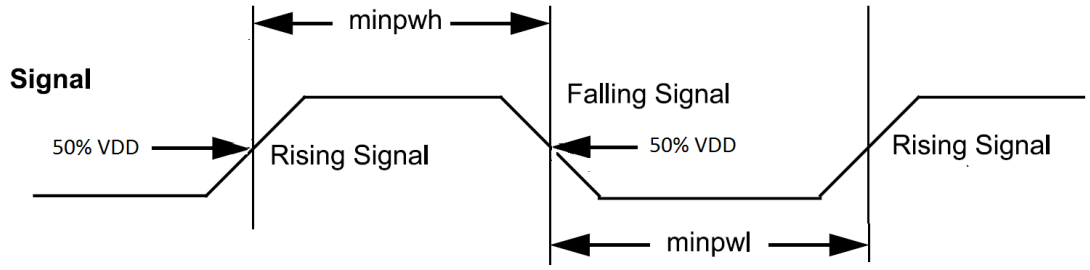


Figure 2.6: Minimum Pulse Width

2.12 Internal Energy at Minimum Output Load

The Power Dissipation internal to a cell, when a given input switches, is primarily dependent upon the cell design itself. The Power Dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The internal energy table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state.

The energy data for each drive strength of the cell in the datasheet is calculated as a function of Transition time (ns) **0.020ns** and no external load at the output pins.

2.13 Leakage Power

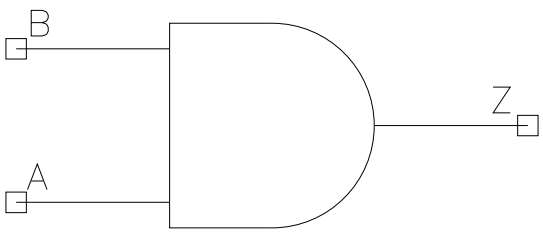
The leakage power depicts the average power consumed by the cell in the stand-by mode (i.e. when the inputs are constant).

CNAND2

Cell Description

2 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	0.800	1.496	1.1968
X14_P4	0.800	1.496	1.1968
X14_P10	0.800	1.496	1.1968
X14_P16	0.800	1.496	1.1968
X19_P0	0.800	1.632	1.3056
X19_P4	0.800	1.632	1.3056
X19_P10	0.800	1.632	1.3056
X19_P16	0.800	1.632	1.3056
X27_P0	0.800	1.632	1.3056
X27_P4	0.800	1.632	1.3056
X27_P10	0.800	1.632	1.3056
X27_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
0	-	0
-	0	0
1	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0014	0.0015	0.0016	0.0017
B	0.0015	0.0015	0.0016	0.0017
	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0014	0.0015	0.0016	0.0017
B	0.0014	0.0015	0.0016	0.0017
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0012	0.0013	0.0014	0.0014
B	0.0011	0.0011	0.0012	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0198	0.0224	0.9232	0.9809
A to Z ↑	0.0153	0.0174	1.2640	1.3766
B to Z ↓	0.0186	0.0210	0.9233	0.9811
B to Z ↑	0.0165	0.0186	1.2624	1.3778
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0261	0.0293	1.0618	1.1364
A to Z ↑	0.0204	0.0230	1.5387	1.6913
B to Z ↓	0.0243	0.0273	1.0625	1.1351
B to Z ↑	0.0216	0.0242	1.5405	1.6914
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0215	0.0243	0.7089	0.7539
A to Z ↑	0.0169	0.0191	0.9764	1.0634
B to Z ↓	0.0205	0.0231	0.7098	0.7543
B to Z ↑	0.0182	0.0205	0.9762	1.0638
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0283	0.0318	0.8171	0.8743
A to Z ↑	0.0224	0.0252	1.1887	1.3046
B to Z ↓	0.0267	0.0300	0.8176	0.8751
B to Z ↑	0.0238	0.0266	1.1877	1.3040
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0236	0.0270	0.5857	0.6242
A to Z ↑	0.0209	0.0235	0.5615	0.6128
B to Z ↓	0.0234	0.0266	0.5866	0.6244
B to Z ↑	0.0223	0.0251	0.5615	0.6116
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0311	0.0352	0.6772	0.7252
A to Z ↑	0.0268	0.0302	0.6843	0.7531
B to Z ↓	0.0306	0.0346	0.6780	0.7263
B to Z ↑	0.0285	0.0320	0.6848	0.7530

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X14_P0	2.555e-05	1.000e-20
X14_P4	4.705e-06	1.000e-20
X14_P10	8.984e-07	1.000e-20
X14_P16	4.090e-07	1.000e-20
X19_P0	3.059e-05	1.000e-20
X19_P4	5.599e-06	1.000e-20
X19_P10	1.057e-06	1.000e-20
X19_P16	4.765e-07	1.000e-20
X27_P0	4.481e-05	1.000e-20
X27_P4	7.881e-06	1.000e-20
X27_P10	1.373e-06	1.000e-20
X27_P16	5.673e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	8.443e-05	7.208e-05	5.797e-05	4.898e-05
B (output stable)	2.494e-04	2.693e-04	2.750e-04	2.709e-04
A to Z	4.863e-03	4.721e-03	4.758e-03	4.883e-03

B to Z	4.485e-03	4.267e-03	4.229e-03	4.304e-03
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	8.456e-05	7.238e-05	5.831e-05	4.905e-05
B (output stable)	2.500e-04	2.701e-04	2.756e-04	2.717e-04
A to Z	6.014e-03	5.832e-03	5.878e-03	6.026e-03
B to Z	5.647e-03	5.389e-03	5.358e-03	5.460e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	3.688e-05	3.248e-05	2.684e-05	2.322e-05
B (output stable)	7.763e-05	9.479e-05	9.858e-05	9.446e-05
A to Z	7.666e-03	7.363e-03	7.174e-03	7.347e-03
B to Z	7.541e-03	7.167e-03	6.911e-03	7.037e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

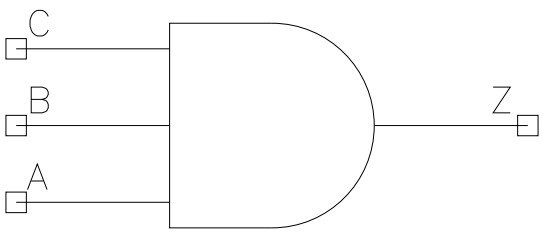
Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAND3

Cell Description

3 input AND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X10_P0	0.800	0.816	0.6528
X10_P4	0.800	0.816	0.6528
X10_P10	0.800	0.816	0.6528
X10_P16	0.800	0.816	0.6528
X14_P0	0.800	1.360	1.0880
X14_P4	0.800	1.360	1.0880
X14_P10	0.800	1.360	1.0880
X14_P16	0.800	1.360	1.0880
X19_P0	0.800	1.496	1.1968
X19_P4	0.800	1.496	1.1968
X19_P10	0.800	1.496	1.1968
X19_P16	0.800	1.496	1.1968
X27_P0	0.800	2.312	1.8496
X27_P4	0.800	2.312	1.8496
X27_P10	0.800	2.312	1.8496
X27_P16	0.800	2.312	1.8496

Truth Table

A	B	C	Z
-	0	-	0
0	-	-	0
-	-	0	0
1	1	1	1

Pin Capacitance

Pin	X10_P0	X10_P4	X10_P10	X10_P16
A	0.0007	0.0007	0.0008	0.0008
B	0.0006	0.0006	0.0007	0.0007
C	0.0006	0.0007	0.0007	0.0008
	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0011	0.0012	0.0012	0.0013
B	0.0009	0.0010	0.0010	0.0011

C	0.0009	0.0009	0.0010	0.0010
	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0013	0.0014	0.0015	0.0016
B	0.0012	0.0013	0.0014	0.0014
C	0.0011	0.0012	0.0013	0.0013
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0016	0.0017	0.0018	0.0019
B	0.0016	0.0017	0.0018	0.0019
C	0.0016	0.0017	0.0018	0.0019

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X10_P0	**X10_P4**	**X10_P0**	**X10_P4**
A to Z ↓	0.0219	0.0249	1.3576	1.4439
A to Z ↑	0.0232	0.0261	1.9531	2.1319
B to Z ↓	0.0209	0.0238	1.3582	1.4435
B to Z ↑	0.0243	0.0271	1.9565	2.1318
C to Z ↓	0.0200	0.0227	1.3564	1.4420
C to Z ↑	0.0249	0.0278	1.9537	2.1298
	X10_P10	**X10_P16**	**X10_P10**	**X10_P16**
A to Z ↓	0.0291	0.0329	1.5654	1.6754
A to Z ↑	0.0305	0.0346	2.3815	2.6147
B to Z ↓	0.0278	0.0313	1.5639	1.6736
B to Z ↑	0.0313	0.0350	2.3828	2.6185
C to Z ↓	0.0264	0.0297	1.5638	1.6719
C to Z ↑	0.0320	0.0357	2.3817	2.6166
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0222	0.0251	0.9403	0.9995
A to Z ↑	0.0224	0.0250	1.3295	1.4495
B to Z ↓	0.0212	0.0240	0.9402	0.9995
B to Z ↑	0.0236	0.0261	1.3294	1.4475
C to Z ↓	0.0202	0.0229	0.9395	0.9989
C to Z ↑	0.0245	0.0271	1.3292	1.4482
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0293	0.0332	1.0844	1.1610
A to Z ↑	0.0292	0.0335	1.6192	1.7801
B to Z ↓	0.0279	0.0317	1.0830	1.1607
B to Z ↑	0.0301	0.0341	1.6211	1.7817
C to Z ↓	0.0266	0.0301	1.0834	1.1601
C to Z ↑	0.0311	0.0350	1.6212	1.7820
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0211	0.0239	0.6975	0.7411
A to Z ↑	0.0219	0.0246	0.9814	1.0694
B to Z ↓	0.0201	0.0227	0.6973	0.7408
B to Z ↑	0.0232	0.0256	0.9806	1.0699
C to Z ↓	0.0191	0.0216	0.6973	0.7410
C to Z ↑	0.0239	0.0264	0.9804	1.0690
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0278	0.0315	0.8041	0.8610
A to Z ↑	0.0286	0.0326	1.1953	1.3165
B to Z ↓	0.0265	0.0299	0.8029	0.8597
B to Z ↑	0.0295	0.0333	1.1977	1.3166

C to Z ↓	0.0250	0.0282	0.8036	0.8606
C to Z ↑	0.0302	0.0339	1.1963	1.3156
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0250	0.0283	0.5869	0.6243
A to Z ↑	0.0229	0.0259	0.5653	0.6164
B to Z ↓	0.0240	0.0272	0.5865	0.6243
B to Z ↑	0.0242	0.0270	0.5660	0.6170
C to Z ↓	0.0235	0.0266	0.5870	0.6250
C to Z ↑	0.0243	0.0271	0.5657	0.6171
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0330	0.0372	0.6779	0.7256
A to Z ↑	0.0305	0.0346	0.6908	0.7600
B to Z ↓	0.0317	0.0357	0.6775	0.7249
B to Z ↑	0.0313	0.0352	0.6917	0.7606
C to Z ↓	0.0309	0.0348	0.6780	0.7250
C to Z ↑	0.0313	0.0350	0.6910	0.7603

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X10_P0	1.625e-05	1.000e-20
X10_P4	2.838e-06	1.000e-20
X10_P10	5.156e-07	1.000e-20
X10_P16	2.351e-07	1.000e-20
X14_P0	2.219e-05	1.000e-20
X14_P4	3.908e-06	1.000e-20
X14_P10	7.234e-07	1.000e-20
X14_P16	3.373e-07	1.000e-20
X19_P0	3.088e-05	1.000e-20
X19_P4	5.441e-06	1.000e-20
X19_P10	9.991e-07	1.000e-20
X19_P16	4.600e-07	1.000e-20
X27_P0	5.237e-05	1.000e-20
X27_P4	8.974e-06	1.000e-20
X27_P10	1.555e-06	1.000e-20
X27_P16	6.671e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X10_P0	X10_P4	X10_P10	X10_P16
A (output stable)	2.095e-05	1.607e-05	1.187e-05	9.458e-06
B (output stable)	4.586e-05	4.879e-05	4.757e-05	4.401e-05
C (output stable)	8.457e-05	9.159e-05	5.620e-05	3.315e-05
A to Z	3.051e-03	2.957e-03	2.979e-03	3.050e-03
B to Z	2.942e-03	2.828e-03	2.826e-03	2.881e-03
C to Z	2.846e-03	2.708e-03	2.678e-03	2.715e-03
	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	2.823e-05	2.119e-05	1.419e-05	1.163e-05
B (output stable)	6.550e-05	6.790e-05	6.733e-05	6.016e-05
C (output stable)	1.222e-04	1.295e-04	8.073e-05	4.653e-05
A to Z	4.500e-03	4.312e-03	4.320e-03	4.457e-03
B to Z	4.314e-03	4.107e-03	4.081e-03	4.203e-03
C to Z	4.173e-03	3.934e-03	3.864e-03	3.964e-03

	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	3.825e-05	2.845e-05	1.972e-05	1.517e-05
B (output stable)	9.084e-05	9.699e-05	9.417e-05	8.624e-05
C (output stable)	1.752e-04	1.875e-04	1.148e-04	6.575e-05
A to Z	5.887e-03	5.636e-03	5.632e-03	5.799e-03
B to Z	5.647e-03	5.355e-03	5.311e-03	5.457e-03
C to Z	5.432e-03	5.092e-03	4.997e-03	5.107e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	8.075e-05	5.894e-05	4.847e-05	4.525e-05
B (output stable)	1.871e-04	1.881e-04	1.827e-04	1.671e-04
C (output stable)	3.985e-04	3.680e-04	1.958e-04	1.186e-04
A to Z	9.181e-03	8.873e-03	8.937e-03	9.143e-03
B to Z	8.796e-03	8.431e-03	8.429e-03	8.592e-03
C to Z	8.469e-03	8.009e-03	7.904e-03	8.015e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

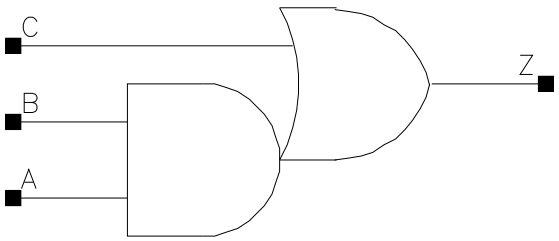
Pin Cycle (vdds)	X10_P0	X10_P4	X10_P10	X10_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNAO12

Cell Description

2 input AND into 2 input OR

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	0.800	1.632	1.3056
X19_P4	0.800	1.632	1.3056
X19_P10	0.800	1.632	1.3056
X19_P16	0.800	1.632	1.3056

Truth Table

A	B	C	Z
0	-	0	0
-	0	0	0
-	-	1	1
1	1	-	1

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0012	0.0013	0.0013	0.0014
B	0.0011	0.0011	0.0012	0.0012
C	0.0011	0.0011	0.0012	0.0013

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0275	0.0311	0.7066	0.7533
A to Z ↑	0.0200	0.0225	0.9585	1.0455
B to Z ↓	0.0265	0.0298	0.7072	0.7535
B to Z ↑	0.0216	0.0242	0.9581	1.0461
C to Z ↓	0.0267	0.0303	0.7056	0.7508
C to Z ↑	0.0201	0.0226	0.9541	1.0393
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0363	0.0411	0.8190	0.8782

A to Z ↑	0.0260	0.0292	1.1694	1.2846
B to Z ↓	0.0347	0.0392	0.8192	0.8788
B to Z ↑	0.0280	0.0313	1.1701	1.2850
C to Z ↓	0.0356	0.0405	0.8159	0.8756
C to Z ↑	0.0261	0.0291	1.1616	1.2747

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X19_P0	2.421e-05	1.000e-20
X19_P4	4.765e-06	1.000e-20
X19_P10	9.751e-07	1.000e-20
X19_P16	4.528e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	9.520e-05	4.725e-05	2.110e-05	1.176e-05
B (output stable)	1.097e-04	6.497e-05	5.139e-05	4.611e-05
C (output stable)	1.498e-04	1.424e-04	1.404e-04	1.433e-04
A to Z	5.817e-03	5.541e-03	5.497e-03	5.585e-03
B to Z	5.659e-03	5.340e-03	5.249e-03	5.306e-03
C to Z	6.195e-03	6.009e-03	6.056e-03	6.211e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

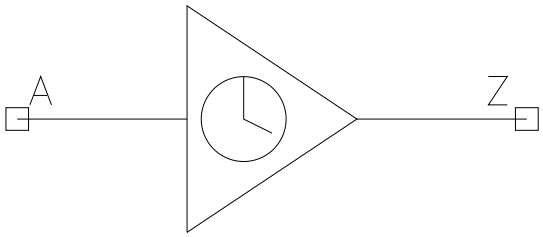
Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNBF

Cell Description

Buffer with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_CNBFX2_P0	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX2_P4	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX2_-P10	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX2_-P16	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_P0	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_P4	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_-P10	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX4_-P16	0.800	0.408	0.3264
C8T28SOI_LL_CNBFX8_P0	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX8_P4	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX8_-P10	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX8_-P16	0.800	0.544	0.4352
C8T28SOI_LL_CNBFX12_-P0	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX12_-P4	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX12_-P10	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX12_-P16	0.800	0.680	0.5440
C8T28SOI_LL_CNBFX18_-P0	0.800	0.952	0.7616
C8T28SOI_LL_CNBFX18_-P4	0.800	0.952	0.7616
C8T28SOI_LL_CNBFX18_-P10	0.800	0.952	0.7616
C8T28SOI_LL_CNBFX18_-P16	0.800	0.952	0.7616

C8T28SOI_LL_CNBFX23_-P0	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX23_-P4	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX23_-P10	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX23_-P16	0.800	1.088	0.8704
C8T28SOI_LL_CNBFX28_-P0	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX28_-P4	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX28_-P10	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX28_-P16	0.800	1.224	0.9792
C8T28SOI_LL_CNBFX32_-P0	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX32_-P4	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX32_-P10	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX32_-P16	0.800	1.496	1.1968
C8T28SOI_LL_CNBFX37_-P0	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX37_-P4	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX37_-P10	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX37_-P16	0.800	1.632	1.3056
C8T28SOI_LL_CNBFX54_-P0	0.800	2.312	1.8496
C8T28SOI_LL_CNBFX54_-P4	0.800	2.312	1.8496
C8T28SOI_LL_CNBFX54_-P10	0.800	2.312	1.8496
C8T28SOI_LL_CNBFX54_-P16	0.800	2.312	1.8496
C8T28SOIDV_LL_-CNBFX18_P0	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX18_P4	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX18_P10	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX18_P16	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNBFX28_P0	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNBFX28_P4	1.600	0.680	1.0880

C8T28SOIDV_LL_-CNBFX28_P10	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNBFX28_P16	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNBFX37_P0	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX37_P4	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX37_P10	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX37_P16	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNBFX55_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX55_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX55_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX55_P16	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNBFX74_P0	1.600	1.632	2.6112
C8T28SOIDV_LL_-CNBFX74_P4	1.600	1.632	2.6112
C8T28SOIDV_LL_-CNBFX74_P10	1.600	1.632	2.6112
C8T28SOIDV_LL_-CNBFX74_P16	1.600	1.632	2.6112

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C8T28SOI_LL_-CNBFX2_P0	C8T28SOI_LL_-CNBFX2_P4	C8T28SOI_LL_-CNBFX2_P10	C8T28SOI_LL_-CNBFX2_P16
A	0.0005	0.0005	0.0005	0.0006
	C8T28SOI_LL_-CNBFX4_P0	C8T28SOI_LL_-CNBFX4_P4	C8T28SOI_LL_-CNBFX4_P10	C8T28SOI_LL_-CNBFX4_P16
A	0.0005	0.0005	0.0006	0.0006
	C8T28SOI_LL_-CNBFX8_P0	C8T28SOI_LL_-CNBFX8_P4	C8T28SOI_LL_-CNBFX8_P10	C8T28SOI_LL_-CNBFX8_P16
A	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LL_-CNBFX12_P0	C8T28SOI_LL_-CNBFX12_P4	C8T28SOI_LL_-CNBFX12_P10	C8T28SOI_LL_-CNBFX12_P16
A	0.0006	0.0007	0.0007	0.0008
	C8T28SOI_LL_-CNBFX18_P0	C8T28SOI_LL_-CNBFX18_P4	C8T28SOI_LL_-CNBFX18_P10	C8T28SOI_LL_-CNBFX18_P16
A	0.0009	0.0010	0.0010	0.0011
	C8T28SOI_LL_-CNBFX23_P0	C8T28SOI_LL_-CNBFX23_P4	C8T28SOI_LL_-CNBFX23_P10	C8T28SOI_LL_-CNBFX23_P16
A	0.0010	0.0011	0.0012	0.0012

	C8T28SOI_LL_-CNBFX28_P0	C8T28SOI_LL_-CNBFX28_P4	C8T28SOI_LL_-CNBFX28_P10	C8T28SOI_LL_-CNBFX28_P16
A	0.0012	0.0013	0.0014	0.0014
	C8T28SOI_LL_-CNBFX32_P0	C8T28SOI_LL_-CNBFX32_P4	C8T28SOI_LL_-CNBFX32_P10	C8T28SOI_LL_-CNBFX32_P16
A	0.0016	0.0016	0.0017	0.0018
	C8T28SOI_LL_-CNBFX37_P0	C8T28SOI_LL_-CNBFX37_P4	C8T28SOI_LL_-CNBFX37_P10	C8T28SOI_LL_-CNBFX37_P16
A	0.0017	0.0017	0.0019	0.0020
	C8T28SOI_LL_-CNBFX54_P0	C8T28SOI_LL_-CNBFX54_P4	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A	0.0022	0.0024	0.0026	0.0027
	C8T28SOIDV_LL_-CNBFX18_P0	C8T28SOIDV_LL_-CNBFX18_P4	C8T28SOIDV_LL_-CNBFX18_P10	C8T28SOIDV_LL_-CNBFX18_P16
A	0.0011	0.0012	0.0013	0.0014
	C8T28SOIDV_LL_-CNBFX28_P0	C8T28SOIDV_LL_-CNBFX28_P4	C8T28SOIDV_LL_-CNBFX28_P10	C8T28SOIDV_LL_-CNBFX28_P16
A	0.0012	0.0013	0.0014	0.0015
	C8T28SOIDV_LL_-CNBFX37_P0	C8T28SOIDV_LL_-CNBFX37_P4	C8T28SOIDV_LL_-CNBFX37_P10	C8T28SOIDV_LL_-CNBFX37_P16
A	0.0016	0.0017	0.0019	0.0020
	C8T28SOIDV_LL_-CNBFX55_P0	C8T28SOIDV_LL_-CNBFX55_P4	C8T28SOIDV_LL_-CNBFX55_P10	C8T28SOIDV_LL_-CNBFX55_P16
A	0.0022	0.0024	0.0026	0.0028
	C8T28SOIDV_LL_-CNBFX74_P0	C8T28SOIDV_LL_-CNBFX74_P4	C8T28SOIDV_LL_-CNBFX74_P10	C8T28SOIDV_LL_-CNBFX74_P16
A	0.0029	0.0031	0.0033	0.0035

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-CNBFX2_P0	**C8T28SOI_LL_-CNBFX2_P4**	**C8T28SOI_LL_-CNBFX2_P0**	**C8T28SOI_LL_-CNBFX2_P4**
A to Z ↓	0.0200	0.0227	5.4923	5.8368
A to Z ↑	0.0157	0.0178	7.5943	8.4215
	C8T28SOI_LL_-CNBFX2_P10	**C8T28SOI_LL_-CNBFX2_P16**	**C8T28SOI_LL_-CNBFX2_P10**	**C8T28SOI_LL_-CNBFX2_P16**
A to Z ↓	0.0263	0.0296	6.3087	6.7196
A to Z ↑	0.0208	0.0233	9.5993	10.6481
	C8T28SOI_LL_-CNBFX4_P0	**C8T28SOI_LL_-CNBFX4_P4**	**C8T28SOI_LL_-CNBFX4_P0**	**C8T28SOI_LL_-CNBFX4_P4**
A to Z ↓	0.0206	0.0234	3.3239	3.5383
A to Z ↑	0.0152	0.0174	4.0509	4.4139
	C8T28SOI_LL_-CNBFX4_P10	**C8T28SOI_LL_-CNBFX4_P16**	**C8T28SOI_LL_-CNBFX4_P10**	**C8T28SOI_LL_-CNBFX4_P16**
A to Z ↓	0.0274	0.0308	3.8354	4.0972
A to Z ↑	0.0202	0.0227	4.9347	5.4257
	C8T28SOI_LL_-CNBFX8_P0	**C8T28SOI_LL_-CNBFX8_P4**	**C8T28SOI_LL_-CNBFX8_P0**	**C8T28SOI_LL_-CNBFX8_P4**
A to Z ↓	0.0197	0.0224	1.6660	1.7726
A to Z ↑	0.0152	0.0173	1.9760	2.1549
	C8T28SOI_LL_-CNBFX8_P10	**C8T28SOI_LL_-CNBFX8_P16**	**C8T28SOI_LL_-CNBFX8_P10**	**C8T28SOI_LL_-CNBFX8_P16**
A to Z ↓	0.0261	0.0295	1.9235	2.0552

A to Z ↑	0.0202	0.0227	2.4090	2.6475
	C8T28SOI_LL_-CNBFX12_P0	**C8T28SOI_LL_-CNBFX12_P4**	**C8T28SOI_LL_-CNBFX12_P0**	**C8T28SOI_LL_-CNBFX12_P4**
A to Z ↓	0.0213	0.0242	1.1406	1.2149
A to Z ↑	0.0182	0.0206	1.2980	1.4143
	C8T28SOI_LL_-CNBFX12_P10	**C8T28SOI_LL_-CNBFX12_P16**	**C8T28SOI_LL_-CNBFX12_P10**	**C8T28SOI_LL_-CNBFX12_P16**
A to Z ↓	0.0283	0.0320	1.3187	1.4116
A to Z ↑	0.0239	0.0268	1.5856	1.7397
	C8T28SOI_LL_-CNBFX18_P0	**C8T28SOI_LL_-CNBFX18_P4**	**C8T28SOI_LL_-CNBFX18_P0**	**C8T28SOI_LL_-CNBFX18_P4**
A to Z ↓	0.0203	0.0232	0.7448	0.7948
A to Z ↑	0.0162	0.0185	0.9634	1.0502
	C8T28SOI_LL_-CNBFX18_P10	**C8T28SOI_LL_-CNBFX18_P16**	**C8T28SOI_LL_-CNBFX18_P10**	**C8T28SOI_LL_-CNBFX18_P16**
A to Z ↓	0.0271	0.0306	0.8625	0.9245
A to Z ↑	0.0215	0.0240	1.1759	1.2912
	C8T28SOI_LL_-CNBFX23_P0	**C8T28SOI_LL_-CNBFX23_P4**	**C8T28SOI_LL_-CNBFX23_P0**	**C8T28SOI_LL_-CNBFX23_P4**
A to Z ↓	0.0207	0.0234	0.5821	0.6200
A to Z ↑	0.0164	0.0186	0.7713	0.8413
	C8T28SOI_LL_-CNBFX23_P10	**C8T28SOI_LL_-CNBFX23_P16**	**C8T28SOI_LL_-CNBFX23_P10**	**C8T28SOI_LL_-CNBFX23_P16**
A to Z ↓	0.0275	0.0309	0.6734	0.7209
A to Z ↑	0.0218	0.0243	0.9421	1.0353
	C8T28SOI_LL_-CNBFX28_P0	**C8T28SOI_LL_-CNBFX28_P4**	**C8T28SOI_LL_-CNBFX28_P0**	**C8T28SOI_LL_-CNBFX28_P4**
A to Z ↓	0.0205	0.0234	0.4809	0.5122
A to Z ↑	0.0164	0.0187	0.6454	0.7048
	C8T28SOI_LL_-CNBFX28_P10	**C8T28SOI_LL_-CNBFX28_P16**	**C8T28SOI_LL_-CNBFX28_P10**	**C8T28SOI_LL_-CNBFX28_P16**
A to Z ↓	0.0271	0.0305	0.5559	0.5960
A to Z ↑	0.0217	0.0243	0.7886	0.8657
	C8T28SOI_LL_-CNBFX32_P0	**C8T28SOI_LL_-CNBFX32_P4**	**C8T28SOI_LL_-CNBFX32_P0**	**C8T28SOI_LL_-CNBFX32_P4**
A to Z ↓	0.0213	0.0242	0.4163	0.4431
A to Z ↑	0.0166	0.0189	0.5559	0.6066
	C8T28SOI_LL_-CNBFX32_P10	**C8T28SOI_LL_-CNBFX32_P16**	**C8T28SOI_LL_-CNBFX32_P10**	**C8T28SOI_LL_-CNBFX32_P16**
A to Z ↓	0.0281	0.0317	0.4814	0.5152
A to Z ↑	0.0219	0.0246	0.6789	0.7451
	C8T28SOI_LL_-CNBFX37_P0	**C8T28SOI_LL_-CNBFX37_P4**	**C8T28SOI_LL_-CNBFX37_P0**	**C8T28SOI_LL_-CNBFX37_P4**
A to Z ↓	0.0210	0.0237	0.3613	0.3843
A to Z ↑	0.0168	0.0190	0.4858	0.5292
	C8T28SOI_LL_-CNBFX37_P10	**C8T28SOI_LL_-CNBFX37_P16**	**C8T28SOI_LL_-CNBFX37_P10**	**C8T28SOI_LL_-CNBFX37_P16**
A to Z ↓	0.0277	0.0312	0.4179	0.4476
A to Z ↑	0.0221	0.0248	0.5921	0.6509
	C8T28SOI_LL_-CNBFX54_P0	**C8T28SOI_LL_-CNBFX54_P4**	**C8T28SOI_LL_-CNBFX54_P0**	**C8T28SOI_LL_-CNBFX54_P4**
A to Z ↓	0.0206	0.0234	0.2524	0.2693
A to Z ↑	0.0171	0.0193	0.3257	0.3550

	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A to Z ↓	0.0272	0.0308	0.2926	0.3136
A to Z ↑	0.0224	0.0251	0.3972	0.4364
	C8T28SOIDV_LL_-CNBFX18_P0	**C8T28SOIDV_LL_-CNBFX18_P4**	**C8T28SOIDV_LL_-CNBFX18_P0**	**C8T28SOIDV_LL_-CNBFX18_P4**
A to Z ↓	0.0186	0.0212	0.7023	0.7482
A to Z ↑	0.0166	0.0187	0.9530	1.0404
	C8T28SOIDV_LL_-CNBFX18_P10	**C8T28SOIDV_LL_-CNBFX18_P16**	**C8T28SOIDV_LL_-CNBFX18_P10**	**C8T28SOIDV_LL_-CNBFX18_P16**
A to Z ↓	0.0249	0.0281	0.8133	0.8701
A to Z ↑	0.0217	0.0243	1.1640	1.2788
	C8T28SOIDV_LL_-CNBFX28_P0	**C8T28SOIDV_LL_-CNBFX28_P4**	**C8T28SOIDV_LL_-CNBFX28_P0**	**C8T28SOIDV_LL_-CNBFX28_P4**
A to Z ↓	0.0209	0.0239	0.4762	0.5083
A to Z ↑	0.0174	0.0198	0.6511	0.7096
	C8T28SOIDV_LL_-CNBFX28_P10	**C8T28SOIDV_LL_-CNBFX28_P16**	**C8T28SOIDV_LL_-CNBFX28_P10**	**C8T28SOIDV_LL_-CNBFX28_P16**
A to Z ↓	0.0276	0.0316	0.5521	0.5917
A to Z ↑	0.0226	0.0257	0.7936	0.8719
	C8T28SOIDV_LL_-CNBFX37_P0	**C8T28SOIDV_LL_-CNBFX37_P4**	**C8T28SOIDV_LL_-CNBFX37_P0**	**C8T28SOIDV_LL_-CNBFX37_P4**
A to Z ↓	0.0203	0.0231	0.3582	0.3826
A to Z ↑	0.0164	0.0187	0.4888	0.5336
	C8T28SOIDV_LL_-CNBFX37_P10	**C8T28SOIDV_LL_-CNBFX37_P16**	**C8T28SOIDV_LL_-CNBFX37_P10**	**C8T28SOIDV_LL_-CNBFX37_P16**
A to Z ↓	0.0273	0.0307	0.4163	0.4460
A to Z ↑	0.0220	0.0245	0.5972	0.6556
	C8T28SOIDV_LL_-CNBFX55_P0	**C8T28SOIDV_LL_-CNBFX55_P4**	**C8T28SOIDV_LL_-CNBFX55_P0**	**C8T28SOIDV_LL_-CNBFX55_P4**
A to Z ↓	0.0201	0.0228	0.2428	0.2590
A to Z ↑	0.0167	0.0189	0.3251	0.3545
	C8T28SOIDV_LL_-CNBFX55_P10	**C8T28SOIDV_LL_-CNBFX55_P16**	**C8T28SOIDV_LL_-CNBFX55_P10**	**C8T28SOIDV_LL_-CNBFX55_P16**
A to Z ↓	0.0268	0.0305	0.2818	0.3023
A to Z ↑	0.0220	0.0248	0.3967	0.4360
	C8T28SOIDV_LL_-CNBFX74_P0	**C8T28SOIDV_LL_-CNBFX74_P4**	**C8T28SOIDV_LL_-CNBFX74_P0**	**C8T28SOIDV_LL_-CNBFX74_P4**
A to Z ↓	0.0211	0.0240	0.1846	0.1971
A to Z ↑	0.0183	0.0207	0.2462	0.2685
	C8T28SOIDV_LL_-CNBFX74_P10	**C8T28SOIDV_LL_-CNBFX74_P16**	**C8T28SOIDV_LL_-CNBFX74_P10**	**C8T28SOIDV_LL_-CNBFX74_P16**
A to Z ↓	0.0280	0.0318	0.2145	0.2302
A to Z ↑	0.0239	0.0269	0.3003	0.3302

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_CNBFX2_P0	2.963e-06	1.000e-20
C8T28SOI_LL_CNBFX2_P4	5.927e-07	1.000e-20
C8T28SOI_LL_CNBFX2_P10	1.284e-07	1.000e-20
C8T28SOI_LL_CNBFX2_P16	6.180e-08	1.000e-20
C8T28SOI_LL_CNBFX4_P0	5.478e-06	1.000e-20

C8T28SOI_LL_CNBFX4_P4	1.064e-06	1.000e-20
C8T28SOI_LL_CNBFX4_P10	2.123e-07	1.000e-20
C8T28SOI_LL_CNBFX4_P16	9.400e-08	1.000e-20
C8T28SOI_LL_CNBFX8_P0	1.179e-05	1.000e-20
C8T28SOI_LL_CNBFX8_P4	2.181e-06	1.000e-20
C8T28SOI_LL_CNBFX8_P10	4.071e-07	1.000e-20
C8T28SOI_LL_CNBFX8_P16	1.722e-07	1.000e-20
C8T28SOI_LL_CNBFX12_P0	1.726e-05	1.000e-20
C8T28SOI_LL_CNBFX12_P4	3.127e-06	1.000e-20
C8T28SOI_LL_CNBFX12_P10	5.666e-07	1.000e-20
C8T28SOI_LL_CNBFX12_P16	2.349e-07	1.000e-20
C8T28SOI_LL_CNBFX18_P0	2.092e-05	1.000e-20
C8T28SOI_LL_CNBFX18_P4	3.935e-06	1.000e-20
C8T28SOI_LL_CNBFX18_P10	7.495e-07	1.000e-20
C8T28SOI_LL_CNBFX18_P16	3.243e-07	1.000e-20
C8T28SOI_LL_CNBFX23_P0	2.834e-05	1.000e-20
C8T28SOI_LL_CNBFX23_P4	5.176e-06	1.000e-20
C8T28SOI_LL_CNBFX23_P10	9.612e-07	1.000e-20
C8T28SOI_LL_CNBFX23_P16	4.116e-07	1.000e-20
C8T28SOI_LL_CNBFX28_P0	3.278e-05	1.000e-20
C8T28SOI_LL_CNBFX28_P4	6.117e-06	1.000e-20
C8T28SOI_LL_CNBFX28_P10	1.148e-06	1.000e-20
C8T28SOI_LL_CNBFX28_P16	4.911e-07	1.000e-20
C8T28SOI_LL_CNBFX32_P0	3.728e-05	1.000e-20
C8T28SOI_LL_CNBFX32_P4	6.911e-06	1.000e-20
C8T28SOI_LL_CNBFX32_P10	1.304e-06	1.000e-20
C8T28SOI_LL_CNBFX32_P16	5.658e-07	1.000e-20
C8T28SOI_LL_CNBFX37_P0	4.419e-05	1.000e-20
C8T28SOI_LL_CNBFX37_P4	8.168e-06	1.000e-20
C8T28SOI_LL_CNBFX37_P10	1.524e-06	1.000e-20
C8T28SOI_LL_CNBFX37_P16	6.527e-07	1.000e-20
C8T28SOI_LL_CNBFX54_P0	6.828e-05	1.000e-20
C8T28SOI_LL_CNBFX54_P4	1.237e-05	1.000e-20
C8T28SOI_LL_CNBFX54_P10	2.252e-06	1.000e-20
C8T28SOI_LL_CNBFX54_P16	9.489e-07	1.000e-20
C8T28SOIDV_LL_CNBFX18_P0	2.577e-05	1.000e-20
C8T28SOIDV_LL_CNBFX18_P4	4.784e-06	1.000e-20
C8T28SOIDV_LL_CNBFX18_P10	8.854e-07	1.000e-20
C8T28SOIDV_LL_CNBFX18_P16	3.675e-07	1.000e-20
C8T28SOIDV_LL_CNBFX28_P0	3.586e-05	1.000e-20
C8T28SOIDV_LL_CNBFX28_P4	6.630e-06	1.000e-20
C8T28SOIDV_LL_CNBFX28_P10	1.220e-06	1.000e-20
C8T28SOIDV_LL_CNBFX28_P16	5.062e-07	1.000e-20
C8T28SOIDV_LL_CNBFX37_P0	4.679e-05	1.000e-20
C8T28SOIDV_LL_CNBFX37_P4	8.594e-06	1.000e-20
C8T28SOIDV_LL_CNBFX37_P10	1.577e-06	1.000e-20
C8T28SOIDV_LL_CNBFX37_P16	6.585e-07	1.000e-20
C8T28SOIDV_LL_CNBFX55_P0	6.956e-05	1.000e-20
C8T28SOIDV_LL_CNBFX55_P4	1.277e-05	1.000e-20
C8T28SOIDV_LL_CNBFX55_P10	2.333e-06	1.000e-20
C8T28SOIDV_LL_CNBFX55_P16	9.707e-07	1.000e-20
C8T28SOIDV_LL_CNBFX74_P0	8.866e-05	1.000e-20

C8T28SOIDV_LL_CNBFX74_P4	1.631e-05	1.000e-20
C8T28SOIDV_LL_CNBFX74_P10	2.984e-06	1.000e-20
C8T28SOIDV_LL_CNBFX74_P16	1.245e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_-CNBFX2_P0	C8T28SOI_LL_-CNBFX2_P4	C8T28SOI_LL_-CNBFX2_P10	C8T28SOI_LL_-CNBFX2_P16
A to Z	1.107e-03	1.070e-03	1.070e-03	1.092e-03
	C8T28SOI_LL_-CNBFX4_P0	C8T28SOI_LL_-CNBFX4_P4	C8T28SOI_LL_-CNBFX4_P10	C8T28SOI_LL_-CNBFX4_P16
A to Z	1.381e-03	1.337e-03	1.346e-03	1.379e-03
	C8T28SOI_LL_-CNBFX8_P0	C8T28SOI_LL_-CNBFX8_P4	C8T28SOI_LL_-CNBFX8_P10	C8T28SOI_LL_-CNBFX8_P16
A to Z	2.275e-03	2.173e-03	2.168e-03	2.220e-03
	C8T28SOI_LL_-CNBFX12_P0	C8T28SOI_LL_-CNBFX12_P4	C8T28SOI_LL_-CNBFX12_P10	C8T28SOI_LL_-CNBFX12_P16
A to Z	3.359e-03	3.205e-03	3.192e-03	3.270e-03
	C8T28SOI_LL_-CNBFX18_P0	C8T28SOI_LL_-CNBFX18_P4	C8T28SOI_LL_-CNBFX18_P10	C8T28SOI_LL_-CNBFX18_P16
A to Z	4.500e-03	4.303e-03	4.274e-03	4.347e-03
	C8T28SOI_LL_-CNBFX23_P0	C8T28SOI_LL_-CNBFX23_P4	C8T28SOI_LL_-CNBFX23_P10	C8T28SOI_LL_-CNBFX23_P16
A to Z	5.763e-03	5.444e-03	5.477e-03	5.568e-03
	C8T28SOI_LL_-CNBFX28_P0	C8T28SOI_LL_-CNBFX28_P4	C8T28SOI_LL_-CNBFX28_P10	C8T28SOI_LL_-CNBFX28_P16
A to Z	6.685e-03	6.372e-03	6.263e-03	6.373e-03
	C8T28SOI_LL_-CNBFX32_P0	C8T28SOI_LL_-CNBFX32_P4	C8T28SOI_LL_-CNBFX32_P10	C8T28SOI_LL_-CNBFX32_P16
A to Z	8.073e-03	7.703e-03	7.612e-03	7.757e-03
	C8T28SOI_LL_-CNBFX37_P0	C8T28SOI_LL_-CNBFX37_P4	C8T28SOI_LL_-CNBFX37_P10	C8T28SOI_LL_-CNBFX37_P16
A to Z	9.198e-03	8.697e-03	8.645e-03	8.795e-03
	C8T28SOI_LL_-CNBFX54_P0	C8T28SOI_LL_-CNBFX54_P4	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A to Z	1.336e-02	1.264e-02	1.244e-02	1.275e-02
	C8T28SOIDV_LL_-CNBFX18_P0	C8T28SOIDV_LL_-CNBFX18_P4	C8T28SOIDV_LL_-CNBFX18_P10	C8T28SOIDV_LL_-CNBFX18_P16
A to Z	4.641e-03	4.423e-03	4.415e-03	4.532e-03
	C8T28SOIDV_LL_-CNBFX28_P0	C8T28SOIDV_LL_-CNBFX28_P4	C8T28SOIDV_LL_-CNBFX28_P10	C8T28SOIDV_LL_-CNBFX28_P16
A to Z	6.877e-03	6.620e-03	6.490e-03	6.742e-03
	C8T28SOIDV_LL_-CNBFX37_P0	C8T28SOIDV_LL_-CNBFX37_P4	C8T28SOIDV_LL_-CNBFX37_P10	C8T28SOIDV_LL_-CNBFX37_P16
A to Z	8.776e-03	8.340e-03	8.396e-03	8.534e-03
	C8T28SOIDV_LL_-CNBFX55_P0	C8T28SOIDV_LL_-CNBFX55_P4	C8T28SOIDV_LL_-CNBFX55_P10	C8T28SOIDV_LL_-CNBFX55_P16
A to Z	1.297e-02	1.231e-02	1.229e-02	1.266e-02
	C8T28SOIDV_LL_-CNBFX74_P0	C8T28SOIDV_LL_-CNBFX74_P4	C8T28SOIDV_LL_-CNBFX74_P10	C8T28SOIDV_LL_-CNBFX74_P16
A to Z	1.746e-02	1.665e-02	1.644e-02	1.693e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

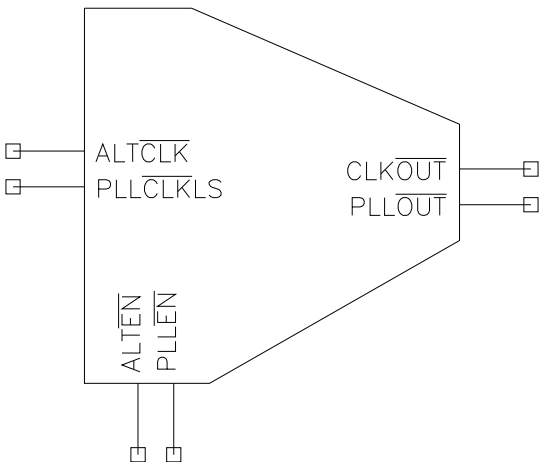
Pin Cycle (vdds)	C8T28SOI_LL_-CNBFX2_P0	C8T28SOI_LL_-CNBFX2_P4	C8T28SOI_LL_-CNBFX2_P10	C8T28SOI_LL_-CNBFX2_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX4_P0	C8T28SOI_LL_-CNBFX4_P4	C8T28SOI_LL_-CNBFX4_P10	C8T28SOI_LL_-CNBFX4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX8_P0	C8T28SOI_LL_-CNBFX8_P4	C8T28SOI_LL_-CNBFX8_P10	C8T28SOI_LL_-CNBFX8_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX12_P0	C8T28SOI_LL_-CNBFX12_P4	C8T28SOI_LL_-CNBFX12_P10	C8T28SOI_LL_-CNBFX12_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX18_P0	C8T28SOI_LL_-CNBFX18_P4	C8T28SOI_LL_-CNBFX18_P10	C8T28SOI_LL_-CNBFX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX23_P0	C8T28SOI_LL_-CNBFX23_P4	C8T28SOI_LL_-CNBFX23_P10	C8T28SOI_LL_-CNBFX23_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX28_P0	C8T28SOI_LL_-CNBFX28_P4	C8T28SOI_LL_-CNBFX28_P10	C8T28SOI_LL_-CNBFX28_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX32_P0	C8T28SOI_LL_-CNBFX32_P4	C8T28SOI_LL_-CNBFX32_P10	C8T28SOI_LL_-CNBFX32_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX37_P0	C8T28SOI_LL_-CNBFX37_P4	C8T28SOI_LL_-CNBFX37_P10	C8T28SOI_LL_-CNBFX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNBFX54_P0	C8T28SOI_LL_-CNBFX54_P4	C8T28SOI_LL_-CNBFX54_P10	C8T28SOI_LL_-CNBFX54_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX18_P0	C8T28SOIDV_LL_-CNBFX18_P4	C8T28SOIDV_LL_-CNBFX18_P10	C8T28SOIDV_LL_-CNBFX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX28_P0	C8T28SOIDV_LL_-CNBFX28_P4	C8T28SOIDV_LL_-CNBFX28_P10	C8T28SOIDV_LL_-CNBFX28_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX37_P0	C8T28SOIDV_LL_-CNBFX37_P4	C8T28SOIDV_LL_-CNBFX37_P10	C8T28SOIDV_LL_-CNBFX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX55_P0	C8T28SOIDV_LL_-CNBFX55_P4	C8T28SOIDV_LL_-CNBFX55_P10	C8T28SOIDV_LL_-CNBFX55_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNBFX74_P0	C8T28SOIDV_LL_-CNBFX74_P4	C8T28SOIDV_LL_-CNBFX74_P10	C8T28SOIDV_LL_-CNBFX74_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNGFMUX21

Cell Description

2:1 Glitch-free MUX for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X30_P0	1.600	4.488	7.1808
X30_P4	1.600	4.488	7.1808
X30_P10	1.600	4.488	7.1808
X30_P16	1.600	4.488	7.1808

Truth Table

PLL_CLK_LS	ALT_CLK	IPLL_EN_LD	IALT_EN_LD	CLK_OUT
0	-	-	0	0
0	0	-	-	0
-	0	0	-	0
PLL_CLK_LS	1	-	1	1
1	ALT_CLK	1	-	1
1	1	0	0	0

PLL_CLK_LS	PLL_OUT
PLL_CLK_LS	PLL_CLK_LS
1	1

PLL_EN	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD
PLL_EN	0	-	PLL_EN
-	-	IPLL_EN_LD	IPLL_EN_LD
-	PLL_CLK_LS	IPLL_EN_LD	IPLL_EN_LD

ALT_EN	ALT_CLK	IALT_EN_LD	IALT_EN_LD
ALT_EN	0	-	ALT_EN
-	-	IALT_EN_LD	IALT_EN_LD
-	ALT_CLK	IALT_EN_LD	IALT_EN_LD

Pin Capacitance

Pin	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK	0.0026	0.0027	0.0029	0.0030
ALT_EN	0.0005	0.0005	0.0005	0.0005
PLL_CLK_LS	0.0044	0.0045	0.0048	0.0050
PLL_EN	0.0004	0.0005	0.0005	0.0005

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X30_P0	**X30_P4**	**X30_P0**	**X30_P4**
ALT_CLK to CLK_OUT ↓	0.0283	0.0319	0.5165	0.5515
ALT_CLK to CLK_OUT ↑	0.0254	0.0287	0.7112	0.7775
PLL_CLK_LS to CLK_OUT ↓	0.0270	0.0301	0.5216	0.5570
PLL_CLK_LS to CLK_OUT ↑	0.0265	0.0297	0.7148	0.7827
PLL_CLK_LS to PLL_OUT ↓	0.0180	0.0202	0.4142	0.4402
PLL_CLK_LS to PLL_OUT ↑	0.0175	0.0196	0.6497	0.7102
	X30_P10	**X30_P16**	**X30_P10**	**X30_P16**
ALT_CLK to CLK_OUT ↓	0.0370	0.0418	0.6019	0.6479
ALT_CLK to CLK_OUT ↑	0.0337	0.0385	0.8728	0.9604
PLL_CLK_LS to CLK_OUT ↓	0.0348	0.0389	0.6077	0.6536
PLL_CLK_LS to CLK_OUT ↑	0.0344	0.0385	0.8785	0.9664
PLL_CLK_LS to PLL_OUT ↓	0.0237	0.0267	0.4772	0.5102
PLL_CLK_LS to PLL_OUT ↑	0.0227	0.0254	0.7956	0.8744

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK ↓	min_pulse_width to ALT_CLK	0.0508	0.0553	0.0645	0.0724
ALT_EN ↓	hold_rising to ALT_CLK	-0.0198	-0.0269	-0.0318	-0.0389
ALT_EN ↑	hold_rising to ALT_CLK	0.0004	-0.0017	-0.0071	-0.0061
ALT_EN ↓	setup_rising to ALT_CLK	0.0472	0.0548	0.0614	0.0711

ALT_EN ↑	setup_rising to ALT_CLK	0.0298	0.0315	0.0391	0.0465
PLL_CLK_LS ↓	min_pulse_width to PLL_CLK_LS	0.0462	0.0508	0.0600	0.0679
PLL_EN ↓	hold_rising to PLL_CLK_LS	-0.0149	-0.0225	-0.0269	-0.0367
PLL_EN ↑	hold_rising to PLL_CLK_LS	0.0058	0.0032	-0.0022	-0.0071
PLL_EN ↓	setup_rising to PLL_CLK_LS	0.0397	0.0472	0.0575	0.0614
PLL_EN ↑	setup_rising to PLL_CLK_LS	0.0245	0.0294	0.0368	0.0417

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X30_P0	1.169e-04	1.000e-20
X30_P4	2.212e-05	1.000e-20
X30_P10	4.522e-06	1.000e-20
X30_P16	2.208e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	3.565e-03	3.558e-03	3.653e-03	3.825e-03
ALT_EN (output stable)	2.072e-03	2.049e-03	2.071e-03	2.107e-03
PLL_CLK_LS (output stable)	1.156e-02	1.032e-02	1.022e-02	1.040e-02
PLL_EN (output stable)	1.841e-03	1.838e-03	1.902e-03	1.986e-03
ALT_CLK to CLK_OUT	1.186e-02	1.180e-02	1.214e-02	1.265e-02
PLL_CLK_LS to CLK_OUT	8.335e-03	7.987e-03	8.031e-03	8.230e-03
PLL_CLK_LS to PLL_OUT	1.116e-02	9.392e-03	9.079e-03	9.158e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X30_P0	X30_P4	X30_P10	X30_P16
ALT_CLK (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_EN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
ALT_CLK to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00
PLL_CLK_LS to CLK_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00

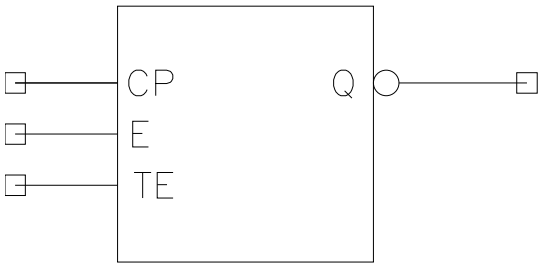
PLL_CLK_LS to PLL_OUT	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNHLS

Cell Description

Latch-based clock gating integrated cell; having active high enable clock transparent and active low enable clock hold low; with scan functionality for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LLP1_-CNHLSX10_P0	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX10_P4	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX10_P10	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX10_P16	0.800	1.904	1.5232
C8T28SOI_LLP1_-CNHLSX14_P0	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX14_P4	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX14_P10	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX14_P16	0.800	2.040	1.6320
C8T28SOI_LLP1_-CNHLSX19_P0	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX19_P4	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX19_P10	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX19_P16	0.800	2.448	1.9584
C8T28SOI_LLP1_-CNHLSX24_P0	0.800	2.584	2.0672
C8T28SOI_LLP1_-CNHLSX24_P4	0.800	2.584	2.0672
C8T28SOI_LLP1_-CNHLSX24_P10	0.800	2.584	2.0672
C8T28SOI_LLP1_-CNHLSX24_P16	0.800	2.584	2.0672

C8T28SOI_LLP1_-CNHLSX29_P0	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX29_P4	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX29_P10	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX29_P16	0.800	2.720	2.1760
C8T28SOI_LLP1_-CNHLSX34_P0	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX34_P4	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX34_P10	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX34_P16	0.800	2.856	2.2848
C8T28SOI_LLP1_-CNHLSX38_P0	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX38_P4	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX38_P10	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX38_P16	0.800	2.992	2.3936
C8T28SOI_LLP1_-CNHLSX57_P0	0.800	4.080	3.2640
C8T28SOI_LLP1_-CNHLSX57_P4	0.800	4.080	3.2640
C8T28SOI_LLP1_-CNHLSX57_P10	0.800	4.080	3.2640
C8T28SOI_LLP1_-CNHLSX57_P16	0.800	4.080	3.2640
C8T28SOI_LLP_-CNHLSX4_P0	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX4_P4	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX4_P10	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX4_P16	0.800	2.040	1.6320
C8T28SOI_LLP_-CNHLSX9_P0	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX9_P4	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX9_P10	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX9_P16	0.800	2.176	1.7408
C8T28SOI_LLP_-CNHLSX13_P0	0.800	2.312	1.8496
C8T28SOI_LLP_-CNHLSX13_P4	0.800	2.312	1.8496

C8T28SOI_LLP_-CNHLSX13_P10	0.800	2.312	1.8496
C8T28SOI_LLP_-CNHLSX13_P16	0.800	2.312	1.8496
C8T28SOI_LLP_-CNHLSX17_P0	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX17_P4	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX17_P10	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX17_P16	0.800	2.448	1.9584
C8T28SOI_LLP_-CNHLSX21_P0	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX21_P4	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX21_P10	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX21_P16	0.800	2.584	2.0672
C8T28SOI_LLP_-CNHLSX27_P0	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX27_P4	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX27_P10	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX27_P16	0.800	3.400	2.7200
C8T28SOI_LLP_-CNHLSX30_P0	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX30_P4	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX30_P10	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX30_P16	0.800	3.672	2.9376
C8T28SOI_LLP_-CNHLSX38_P0	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX38_P4	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX38_P10	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX38_P16	0.800	3.944	3.1552
C8T28SOI_LLP_-CNHLSX54_P0	0.800	5.304	4.2432
C8T28SOI_LLP_-CNHLSX54_P4	0.800	5.304	4.2432
C8T28SOI_LLP_-CNHLSX54_P10	0.800	5.304	4.2432
C8T28SOI_LLP_-CNHLSX54_P16	0.800	5.304	4.2432

Truth Table

CP	E	TE	OLDIE	Q
0	-	-	-	0
1	-	-	OLDIE	OLDIE

OLDIE	OLDIE
OLDIE	OLDIE

Pin Capacitance

Pin	C8T28SOI_LLP1_-CNHLSX10_P0	C8T28SOI_LLP1_-CNHLSX10_P4	C8T28SOI_LLP1_-CNHLSX10_P10	C8T28SOI_LLP1_-CNHLSX10_P16
CP	0.0010	0.0011	0.0011	0.0012
E	0.0004	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0007
	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P10	C8T28SOI_LLP1_-CNHLSX14_P16
CP	0.0010	0.0011	0.0012	0.0013
E	0.0004	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0007
	C8T28SOI_LLP1_-CNHLSX19_P0	C8T28SOI_LLP1_-CNHLSX19_P4	C8T28SOI_LLP1_-CNHLSX19_P10	C8T28SOI_LLP1_-CNHLSX19_P16
CP	0.0015	0.0016	0.0018	0.0019
E	0.0004	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0007
	C8T28SOI_LLP1_-CNHLSX24_P0	C8T28SOI_LLP1_-CNHLSX24_P4	C8T28SOI_LLP1_-CNHLSX24_P10	C8T28SOI_LLP1_-CNHLSX24_P16
CP	0.0016	0.0016	0.0018	0.0019
E	0.0004	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0007
	C8T28SOI_LLP1_-CNHLSX29_P0	C8T28SOI_LLP1_-CNHLSX29_P4	C8T28SOI_LLP1_-CNHLSX29_P10	C8T28SOI_LLP1_-CNHLSX29_P16
CP	0.0016	0.0017	0.0019	0.0020
E	0.0004	0.0004	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP1_-CNHLSX34_P0	C8T28SOI_LLP1_-CNHLSX34_P4	C8T28SOI_LLP1_-CNHLSX34_P10	C8T28SOI_LLP1_-CNHLSX34_P16
CP	0.0016	0.0017	0.0019	0.0020
E	0.0004	0.0004	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP1_-CNHLSX38_P0	C8T28SOI_LLP1_-CNHLSX38_P4	C8T28SOI_LLP1_-CNHLSX38_P10	C8T28SOI_LLP1_-CNHLSX38_P16
CP	0.0016	0.0017	0.0019	0.0020
E	0.0004	0.0004	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP1_-CNHLSX57_P0	C8T28SOI_LLP1_-CNHLSX57_P4	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP	0.0027	0.0028	0.0031	0.0032
E	0.0003	0.0004	0.0004	0.0004
TE	0.0006	0.0007	0.0007	0.0007
	C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP	0.0015	0.0015	0.0016	0.0017
E	0.0003	0.0003	0.0004	0.0004

TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP	0.0019	0.0020	0.0021	0.0022
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP	0.0020	0.0020	0.0021	0.0022
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP	0.0020	0.0020	0.0021	0.0022
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP	0.0020	0.0020	0.0021	0.0022
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP	0.0027	0.0028	0.0030	0.0031
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP	0.0027	0.0028	0.0030	0.0031
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP	0.0027	0.0028	0.0029	0.0031
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007
	C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP	0.0050	0.0052	0.0055	0.0058
E	0.0003	0.0003	0.0004	0.0004
TE	0.0006	0.0006	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LLP1_-CNHLSX10_P0	**C8T28SOI_LLP1_-CNHLSX10_P4**	**C8T28SOI_LLP1_-CNHLSX10_P0**	**C8T28SOI_LLP1_-CNHLSX10_P4**
CP to Q ↓	0.0265	0.0298	1.4130	1.5036
CP to Q ↑	0.0243	0.0272	1.9107	2.0852
	C8T28SOI_LLP1_-CNHLSX10_P10	**C8T28SOI_LLP1_-CNHLSX10_P16**	**C8T28SOI_LLP1_-CNHLSX10_P10**	**C8T28SOI_LLP1_-CNHLSX10_P16**
CP to Q ↓	0.0344	0.0386	1.6362	1.7553
CP to Q ↑	0.0312	0.0348	2.3330	2.5633

	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4
CP to Q ↓	0.0285	0.0321	0.9554	1.0189
CP to Q ↑	0.0263	0.0294	1.2858	1.4029
	C8T28SOI_LLP1_-CNHLSX14_P10	**C8T28SOI_LLP1_-CNHLSX14_P16**	**C8T28SOI_LLP1_-CNHLSX14_P10**	**C8T28SOI_LLP1_-CNHLSX14_P16**
CP to Q ↓	0.0373	0.0420	1.1095	1.1905
CP to Q ↑	0.0338	0.0378	1.5713	1.7262
	C8T28SOI_LLP1_-CNHLSX19_P0	**C8T28SOI_LLP1_-CNHLSX19_P4**	**C8T28SOI_LLP1_-CNHLSX19_P0**	**C8T28SOI_LLP1_-CNHLSX19_P4**
CP to Q ↓	0.0229	0.0258	0.6990	0.7439
CP to Q ↑	0.0213	0.0238	0.9568	1.0430
	C8T28SOI_LLP1_-CNHLSX19_P10	**C8T28SOI_LLP1_-CNHLSX19_P16**	**C8T28SOI_LLP1_-CNHLSX19_P10**	**C8T28SOI_LLP1_-CNHLSX19_P16**
CP to Q ↓	0.0300	0.0337	0.8082	0.8647
CP to Q ↑	0.0274	0.0306	1.1666	1.2806
	C8T28SOI_LLP1_-CNHLSX24_P0	**C8T28SOI_LLP1_-CNHLSX24_P4**	**C8T28SOI_LLP1_-CNHLSX24_P0**	**C8T28SOI_LLP1_-CNHLSX24_P4**
CP to Q ↓	0.0249	0.0280	0.5717	0.6093
CP to Q ↑	0.0231	0.0258	0.7724	0.8410
	C8T28SOI_LLP1_-CNHLSX24_P10	**C8T28SOI_LLP1_-CNHLSX24_P16**	**C8T28SOI_LLP1_-CNHLSX24_P10**	**C8T28SOI_LLP1_-CNHLSX24_P16**
CP to Q ↓	0.0325	0.0366	0.6618	0.7092
CP to Q ↑	0.0298	0.0333	0.9405	1.0333
	C8T28SOI_LLP1_-CNHLSX29_P0	**C8T28SOI_LLP1_-CNHLSX29_P4**	**C8T28SOI_LLP1_-CNHLSX29_P0**	**C8T28SOI_LLP1_-CNHLSX29_P4**
CP to Q ↓	0.0243	0.0274	0.4784	0.5095
CP to Q ↑	0.0232	0.0259	0.6455	0.7038
	C8T28SOI_LLP1_-CNHLSX29_P10	**C8T28SOI_LLP1_-CNHLSX29_P16**	**C8T28SOI_LLP1_-CNHLSX29_P10**	**C8T28SOI_LLP1_-CNHLSX29_P16**
CP to Q ↓	0.0318	0.0359	0.5540	0.5944
CP to Q ↑	0.0297	0.0332	0.7869	0.8638
	C8T28SOI_LLP1_-CNHLSX34_P0	**C8T28SOI_LLP1_-CNHLSX34_P4**	**C8T28SOI_LLP1_-CNHLSX34_P0**	**C8T28SOI_LLP1_-CNHLSX34_P4**
CP to Q ↓	0.0258	0.0291	0.4159	0.4434
CP to Q ↑	0.0247	0.0275	0.5575	0.6064
	C8T28SOI_LLP1_-CNHLSX34_P10	**C8T28SOI_LLP1_-CNHLSX34_P16**	**C8T28SOI_LLP1_-CNHLSX34_P10**	**C8T28SOI_LLP1_-CNHLSX34_P16**
CP to Q ↓	0.0340	0.0382	0.4825	0.5174
CP to Q ↑	0.0318	0.0354	0.6789	0.7449
	C8T28SOI_LLP1_-CNHLSX38_P0	**C8T28SOI_LLP1_-CNHLSX38_P4**	**C8T28SOI_LLP1_-CNHLSX38_P0**	**C8T28SOI_LLP1_-CNHLSX38_P4**
CP to Q ↓	0.0270	0.0305	0.3639	0.3883
CP to Q ↑	0.0259	0.0288	0.4883	0.5316
	C8T28SOI_LLP1_-CNHLSX38_P10	**C8T28SOI_LLP1_-CNHLSX38_P16**	**C8T28SOI_LLP1_-CNHLSX38_P10**	**C8T28SOI_LLP1_-CNHLSX38_P16**
CP to Q ↓	0.0356	0.0400	0.4223	0.4533
CP to Q ↑	0.0333	0.0371	0.5953	0.6537
	C8T28SOI_LLP1_-CNHLSX57_P0	**C8T28SOI_LLP1_-CNHLSX57_P4**	**C8T28SOI_LLP1_-CNHLSX57_P0**	**C8T28SOI_LLP1_-CNHLSX57_P4**
CP to Q ↓	0.0254	0.0286	0.2441	0.2602
CP to Q ↑	0.0242	0.0270	0.3381	0.3685

	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP to Q ↓	0.0333	0.0373	0.2826	0.3030
CP to Q ↑	0.0312	0.0348	0.4116	0.4513
	C8T28SOI_LLP_-CNHLSX4_P0	**C8T28SOI_LLP_-CNHLSX4_P4**	**C8T28SOI_LLP_-CNHLSX4_P0**	**C8T28SOI_LLP_-CNHLSX4_P4**
CP to Q ↓	0.0268	0.0308	3.4194	3.6400
CP to Q ↑	0.0199	0.0225	4.0049	4.3674
	C8T28SOI_LLP_-CNHLSX4_P10	**C8T28SOI_LLP_-CNHLSX4_P16**	**C8T28SOI_LLP_-CNHLSX4_P10**	**C8T28SOI_LLP_-CNHLSX4_P16**
CP to Q ↓	0.0362	0.0411	3.9515	4.2291
CP to Q ↑	0.0262	0.0293	4.8828	5.3600
	C8T28SOI_LLP_-CNHLSX9_P0	**C8T28SOI_LLP_-CNHLSX9_P4**	**C8T28SOI_LLP_-CNHLSX9_P0**	**C8T28SOI_LLP_-CNHLSX9_P4**
CP to Q ↓	0.0240	0.0272	1.5732	1.6739
CP to Q ↑	0.0178	0.0202	1.9791	2.1582
	C8T28SOI_LLP_-CNHLSX9_P10	**C8T28SOI_LLP_-CNHLSX9_P16**	**C8T28SOI_LLP_-CNHLSX9_P10**	**C8T28SOI_LLP_-CNHLSX9_P16**
CP to Q ↓	0.0318	0.0360	1.8162	1.9439
CP to Q ↑	0.0236	0.0265	2.4161	2.6525
	C8T28SOI_LLP_-CNHLSX13_P0	**C8T28SOI_LLP_-CNHLSX13_P4**	**C8T28SOI_LLP_-CNHLSX13_P0**	**C8T28SOI_LLP_-CNHLSX13_P4**
CP to Q ↓	0.0283	0.0322	1.0616	1.1332
CP to Q ↑	0.0212	0.0240	1.3273	1.4496
	C8T28SOI_LLP_-CNHLSX13_P10	**C8T28SOI_LLP_-CNHLSX13_P16**	**C8T28SOI_LLP_-CNHLSX13_P10**	**C8T28SOI_LLP_-CNHLSX13_P16**
CP to Q ↓	0.0377	0.0429	1.2325	1.3223
CP to Q ↑	0.0280	0.0316	1.6244	1.7838
	C8T28SOI_LLP_-CNHLSX17_P0	**C8T28SOI_LLP_-CNHLSX17_P4**	**C8T28SOI_LLP_-CNHLSX17_P0**	**C8T28SOI_LLP_-CNHLSX17_P4**
CP to Q ↓	0.0321	0.0364	0.8227	0.8784
CP to Q ↑	0.0239	0.0270	0.9976	1.0901
	C8T28SOI_LLP_-CNHLSX17_P10	**C8T28SOI_LLP_-CNHLSX17_P16**	**C8T28SOI_LLP_-CNHLSX17_P10**	**C8T28SOI_LLP_-CNHLSX17_P16**
CP to Q ↓	0.0431	0.0485	0.9577	1.0270
CP to Q ↑	0.0317	0.0353	1.2225	1.3443
	C8T28SOI_LLP_-CNHLSX21_P0	**C8T28SOI_LLP_-CNHLSX21_P4**	**C8T28SOI_LLP_-CNHLSX21_P0**	**C8T28SOI_LLP_-CNHLSX21_P4**
CP to Q ↓	0.0363	0.0411	0.6718	0.7174
CP to Q ↑	0.0272	0.0304	0.8102	0.8851
	C8T28SOI_LLP_-CNHLSX21_P10	**C8T28SOI_LLP_-CNHLSX21_P16**	**C8T28SOI_LLP_-CNHLSX21_P10**	**C8T28SOI_LLP_-CNHLSX21_P16**
CP to Q ↓	0.0481	0.0547	0.7838	0.8425
CP to Q ↑	0.0352	0.0395	0.9922	1.0906
	C8T28SOI_LLP_-CNHLSX27_P0	**C8T28SOI_LLP_-CNHLSX27_P4**	**C8T28SOI_LLP_-CNHLSX27_P0**	**C8T28SOI_LLP_-CNHLSX27_P4**
CP to Q ↓	0.0229	0.0258	0.5403	0.5752
CP to Q ↑	0.0187	0.0211	0.6069	0.6632
	C8T28SOI_LLP_-CNHLSX27_P10	**C8T28SOI_LLP_-CNHLSX27_P16**	**C8T28SOI_LLP_-CNHLSX27_P10**	**C8T28SOI_LLP_-CNHLSX27_P16**
CP to Q ↓	0.0300	0.0339	0.6248	0.6692
CP to Q ↑	0.0246	0.0276	0.7434	0.8177

	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4
CP to Q ↓	0.0243	0.0274	0.4780	0.5092
CP to Q ↑	0.0200	0.0226	0.5390	0.5878
	C8T28SOI_LLP_-CNHLSX30_P10	**C8T28SOI_LLP_-CNHLSX30_P16**	**C8T28SOI_LLP_-CNHLSX30_P10**	**C8T28SOI_LLP_-CNHLSX30_P16**
CP to Q ↓	0.0319	0.0360	0.5531	0.5926
CP to Q ↑	0.0263	0.0294	0.6603	0.7254
	C8T28SOI_LLP_-CNHLSX38_P0	**C8T28SOI_LLP_-CNHLSX38_P4**	**C8T28SOI_LLP_-CNHLSX38_P0**	**C8T28SOI_LLP_-CNHLSX38_P4**
CP to Q ↓	0.0270	0.0301	0.3839	0.4093
CP to Q ↑	0.0223	0.0248	0.4353	0.4753
	C8T28SOI_LLP_-CNHLSX38_P10	**C8T28SOI_LLP_-CNHLSX38_P16**	**C8T28SOI_LLP_-CNHLSX38_P10**	**C8T28SOI_LLP_-CNHLSX38_P16**
CP to Q ↓	0.0352	0.0396	0.4450	0.4764
CP to Q ↑	0.0289	0.0323	0.5321	0.5854
	C8T28SOI_LLP_-CNHLSX54_P0	**C8T28SOI_LLP_-CNHLSX54_P4**	**C8T28SOI_LLP_-CNHLSX54_P0**	**C8T28SOI_LLP_-CNHLSX54_P4**
CP to Q ↓	0.0207	0.0232	0.2703	0.2875
CP to Q ↑	0.0184	0.0205	0.3140	0.3423
	C8T28SOI_LLP_-CNHLSX54_P10	**C8T28SOI_LLP_-CNHLSX54_P16**	**C8T28SOI_LLP_-CNHLSX54_P10**	**C8T28SOI_LLP_-CNHLSX54_P16**
CP to Q ↓	0.0271	0.0304	0.3124	0.3340
CP to Q ↑	0.0240	0.0268	0.3824	0.4201

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOI_-LLP1_-CNHLSX10_P0	C8T28SOI_-LLP1_-CNHLSX10_P4	C8T28SOI_-LLP1_-CNHLSX10_P10	C8T28SOI_-LLP1_-CNHLSX10_P16
CP ↓	min_pulse_width to CP	0.0477	0.0556	0.0634	0.0712
E ↓	hold_rising to CP	0.0026	0.0036	-0.0018	-0.0045
E ↑	hold_rising to CP	-0.0057	-0.0079	-0.0176	-0.0225
E ↓	setup_rising to CP	0.0214	0.0273	0.0295	0.0343
E ↑	setup_rising to CP	0.0353	0.0428	0.0498	0.0569
TE ↓	hold_rising to CP	0.0058	-0.0000	-0.0023	-0.0072
TE ↑	hold_rising to CP	-0.0079	-0.0127	-0.0176	-0.0247
TE ↓	setup_rising to CP	0.0215	0.0247	0.0296	0.0317
TE ↑	setup_rising to CP	0.0375	0.0423	0.0521	0.0591
		C8T28SOI_-LLP1_-CNHLSX14_P0	C8T28SOI_-LLP1_-CNHLSX14_P4	C8T28SOI_-LLP1_-CNHLSX14_P10	C8T28SOI_-LLP1_-CNHLSX14_P16
CP ↓	min_pulse_width to CP	0.0478	0.0556	0.0634	0.0725
E ↓	hold_rising to CP	0.0053	0.0026	-0.0028	-0.0045
E ↑	hold_rising to CP	-0.0057	-0.0079	-0.0176	-0.0225
E ↓	setup_rising to CP	0.0224	0.0220	0.0268	0.0294

E ↑	setup_rising to CP	0.0353	0.0423	0.0525	0.0596
TE ↓	hold_rising to CP	0.0048	0.0026	-0.0023	-0.0045
TE ↑	hold_rising to CP	-0.0079	-0.0127	-0.0176	-0.0247
TE ↓	setup_rising to CP	0.0198	0.0247	0.0273	0.0322
TE ↑	setup_rising to CP	0.0375	0.0423	0.0521	0.0591
		C8T28SOI_-LLP1_-CNHLSX19_P0	C8T28SOI_-LLP1_-CNHLSX19_P4	C8T28SOI_-LLP1_-CNHLSX19_P10	C8T28SOI_-LLP1_-CNHLSX19_P16
CP ↓	min_pulse_width to CP	0.0556	0.0635	0.0725	0.0815
E ↓	hold_rising to CP	-0.0022	-0.0013	-0.0067	-0.0116
E ↑	hold_rising to CP	-0.0079	-0.0128	-0.0225	-0.0274
E ↓	setup_rising to CP	0.0268	0.0289	0.0343	0.0392
E ↑	setup_rising to CP	0.0401	0.0450	0.0542	0.0644
TE ↓	hold_rising to CP	0.0009	-0.0049	-0.0062	-0.0116
TE ↑	hold_rising to CP	-0.0111	-0.0127	-0.0225	-0.0296
TE ↓	setup_rising to CP	0.0268	0.0296	0.0344	0.0387
TE ↑	setup_rising to CP	0.0401	0.0472	0.0569	0.0640
		C8T28SOI_-LLP1_-CNHLSX24_P0	C8T28SOI_-LLP1_-CNHLSX24_P4	C8T28SOI_-LLP1_-CNHLSX24_P10	C8T28SOI_-LLP1_-CNHLSX24_P16
CP ↓	min_pulse_width to CP	0.0556	0.0634	0.0725	0.0815
E ↓	hold_rising to CP	-0.0023	-0.0018	-0.0067	-0.0094
E ↑	hold_rising to CP	-0.0079	-0.0128	-0.0225	-0.0274
E ↓	setup_rising to CP	0.0273	0.0263	0.0343	0.0392
E ↑	setup_rising to CP	0.0401	0.0476	0.0570	0.0640
TE ↓	hold_rising to CP	0.0004	-0.0017	-0.0071	-0.0120
TE ↑	hold_rising to CP	-0.0111	-0.0127	-0.0225	-0.0296
TE ↓	setup_rising to CP	0.0242	0.0296	0.0312	0.0366
TE ↑	setup_rising to CP	0.0428	0.0472	0.0569	0.0666
		C8T28SOI_-LLP1_-CNHLSX29_P0	C8T28SOI_-LLP1_-CNHLSX29_P4	C8T28SOI_-LLP1_-CNHLSX29_P10	C8T28SOI_-LLP1_-CNHLSX29_P16
CP ↓	min_pulse_width to CP	0.0635	0.0727	0.0816	0.0941
E ↓	hold_rising to CP	-0.0023	-0.0039	-0.0094	-0.0143
E ↑	hold_rising to CP	-0.0128	-0.0177	-0.0274	-0.0371
E ↓	setup_rising to CP	0.0268	0.0322	0.0334	0.0388
E ↑	setup_rising to CP	0.0450	0.0521	0.0645	0.0732

TE ↓	hold_rising to CP	0.0009	-0.0045	-0.0094	-0.0143
TE ↑	hold_rising to CP	-0.0128	-0.0230	-0.0296	-0.0394
TE ↓	setup_rising to CP	0.0264	0.0296	0.0371	0.0419
TE ↑	setup_rising to CP	0.0476	0.0515	0.0635	0.0790
		C8T28SOI_-LLP1_-CNHLSX34_P0	C8T28SOI_-LLP1_-CNHLSX34_P4	C8T28SOI_-LLP1_-CNHLSX34_P10	C8T28SOI_-LLP1_-CNHLSX34_P16
CP ↓	min_pulse_width to CP	0.0635	0.0727	0.0850	0.0941
E ↓	hold_rising to CP	-0.0023	-0.0018	-0.0094	-0.0143
E ↑	hold_rising to CP	-0.0128	-0.0177	-0.0274	-0.0371
E ↓	setup_rising to CP	0.0268	0.0322	0.0343	0.0392
E ↑	setup_rising to CP	0.0450	0.0521	0.0671	0.0764
TE ↓	hold_rising to CP	0.0004	-0.0050	-0.0072	-0.0116
TE ↑	hold_rising to CP	-0.0128	-0.0230	-0.0296	-0.0394
TE ↓	setup_rising to CP	0.0268	0.0296	0.0371	0.0387
TE ↑	setup_rising to CP	0.0472	0.0574	0.0667	0.0790
		C8T28SOI_-LLP1_-CNHLSX38_P0	C8T28SOI_-LLP1_-CNHLSX38_P4	C8T28SOI_-LLP1_-CNHLSX38_P10	C8T28SOI_-LLP1_-CNHLSX38_P16
CP ↓	min_pulse_width to CP	0.0635	0.0727	0.0850	0.0941
E ↓	hold_rising to CP	-0.0023	-0.0018	-0.0067	-0.0090
E ↑	hold_rising to CP	-0.0128	-0.0177	-0.0274	-0.0371
E ↓	setup_rising to CP	0.0273	0.0289	0.0343	0.0392
E ↑	setup_rising to CP	0.0450	0.0515	0.0671	0.0764
TE ↓	hold_rising to CP	0.0004	-0.0017	-0.0072	-0.0121
TE ↑	hold_rising to CP	-0.0127	-0.0230	-0.0296	-0.0394
TE ↓	setup_rising to CP	0.0247	0.0296	0.0344	0.0392
TE ↑	setup_rising to CP	0.0472	0.0574	0.0667	0.0790
		C8T28SOI_-LLP1_-CNHLSX57_P0	C8T28SOI_-LLP1_-CNHLSX57_P4	C8T28SOI_-LLP1_-CNHLSX57_P10	C8T28SOI_-LLP1_-CNHLSX57_P16
CP ↓	min_pulse_width to CP	0.0694	0.0771	0.0943	0.1033
E ↓	hold_rising to CP	-0.0023	-0.0071	-0.0094	-0.0143
E ↑	hold_rising to CP	-0.0155	-0.0226	-0.0323	-0.0426
E ↓	setup_rising to CP	0.0263	0.0317	0.0366	0.0441
E ↑	setup_rising to CP	0.0499	0.0596	0.0716	0.0839
TE ↓	hold_rising to CP	-0.0017	-0.0045	-0.0120	-0.0137
TE ↑	hold_rising to CP	-0.0150	-0.0225	-0.0323	-0.0442

TE ↓	setup_rising to CP	0.0296	0.0312	0.0366	0.0415
TE ↑	setup_rising to CP	0.0525	0.0623	0.0742	0.0861
		C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP ↓	min_pulse_width to CP	0.0315	0.0361	0.0406	0.0467
E ↓	hold_rising to CP	-0.0106	-0.0123	-0.0198	-0.0242
E ↑	hold_rising to CP	0.0036	0.0010	-0.0013	-0.0035
E ↓	setup_rising to CP	0.0349	0.0430	0.0474	0.0523
E ↑	setup_rising to CP	0.0239	0.0293	0.0368	0.0384
TE ↓	hold_rising to CP	-0.0105	-0.0159	-0.0204	-0.0252
TE ↑	hold_rising to CP	0.0036	-0.0013	-0.0039	-0.0067
TE ↓	setup_rising to CP	0.0350	0.0399	0.0474	0.0518
TE ↑	setup_rising to CP	0.0265	0.0319	0.0367	0.0416
		C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP ↓	min_pulse_width to CP	0.0299	0.0332	0.0377	0.0422
E ↓	hold_rising to CP	-0.0078	-0.0127	-0.0171	-0.0252
E ↑	hold_rising to CP	0.0058	0.0036	-0.0013	-0.0039
E ↓	setup_rising to CP	0.0359	0.0372	0.0447	0.0495
E ↑	setup_rising to CP	0.0244	0.0265	0.0319	0.0367
TE ↓	hold_rising to CP	-0.0084	-0.0101	-0.0176	-0.0220
TE ↑	hold_rising to CP	0.0036	0.0036	-0.0013	-0.0035
TE ↓	setup_rising to CP	0.0360	0.0409	0.0453	0.0501
TE ↑	setup_rising to CP	0.0244	0.0260	0.0309	0.0389
		C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP ↓	min_pulse_width to CP	0.0299	0.0356	0.0401	0.0463
E ↓	hold_rising to CP	-0.0078	-0.0127	-0.0171	-0.0247
E ↑	hold_rising to CP	0.0058	0.0036	-0.0018	-0.0039
E ↓	setup_rising to CP	0.0359	0.0372	0.0446	0.0495
E ↑	setup_rising to CP	0.0244	0.0265	0.0319	0.0367
TE ↓	hold_rising to CP	-0.0084	-0.0101	-0.0176	-0.0220
TE ↑	hold_rising to CP	0.0036	0.0036	-0.0013	-0.0035
TE ↓	setup_rising to CP	0.0360	0.0409	0.0453	0.0501
TE ↑	setup_rising to CP	0.0244	0.0260	0.0335	0.0389

		C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP ↓	min_pulse_width to CP	0.0316	0.0356	0.0418	0.0469
E ↓	hold_rising to CP	-0.0078	-0.0127	-0.0171	-0.0247
E ↑	hold_rising to CP	0.0058	0.0036	-0.0018	-0.0039
E ↓	setup_rising to CP	0.0355	0.0372	0.0446	0.0495
E ↑	setup_rising to CP	0.0244	0.0265	0.0319	0.0367
TE ↓	hold_rising to CP	-0.0084	-0.0101	-0.0176	-0.0220
TE ↑	hold_rising to CP	0.0036	0.0036	-0.0013	-0.0035
TE ↓	setup_rising to CP	0.0360	0.0409	0.0453	0.0528
TE ↑	setup_rising to CP	0.0244	0.0261	0.0335	0.0389
		C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP ↓	min_pulse_width to CP	0.0316	0.0356	0.0424	0.0487
E ↓	hold_rising to CP	-0.0078	-0.0127	-0.0171	-0.0247
E ↑	hold_rising to CP	0.0058	0.0036	-0.0018	-0.0039
E ↓	setup_rising to CP	0.0359	0.0372	0.0446	0.0495
E ↑	setup_rising to CP	0.0244	0.0265	0.0319	0.0367
TE ↓	hold_rising to CP	-0.0084	-0.0101	-0.0176	-0.0220
TE ↑	hold_rising to CP	0.0036	0.0036	-0.0013	-0.0035
TE ↓	setup_rising to CP	0.0360	0.0409	0.0453	0.0528
TE ↑	setup_rising to CP	0.0244	0.0261	0.0335	0.0389
		C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP ↓	min_pulse_width to CP	0.0334	0.0380	0.0425	0.0470
E ↓	hold_rising to CP	-0.0127	-0.0181	-0.0220	-0.0295
E ↑	hold_rising to CP	0.0036	-0.0017	-0.0013	-0.0035
E ↓	setup_rising to CP	0.0371	0.0420	0.0495	0.0572
E ↑	setup_rising to CP	0.0265	0.0314	0.0368	0.0438
TE ↓	hold_rising to CP	-0.0101	-0.0149	-0.0225	-0.0269
TE ↑	hold_rising to CP	0.0036	-0.0013	-0.0039	-0.0093
TE ↓	setup_rising to CP	0.0408	0.0457	0.0502	0.0571
TE ↑	setup_rising to CP	0.0293	0.0313	0.0384	0.0465
		C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP ↓	min_pulse_width to CP	0.0334	0.0380	0.0424	0.0470
E ↓	hold_rising to CP	-0.0127	-0.0181	-0.0220	-0.0295

E ↑	hold_rising to CP	0.0036	-0.0017	-0.0013	-0.0067
E ↓	setup_rising to CP	0.0371	0.0420	0.0495	0.0572
E ↑	setup_rising to CP	0.0265	0.0314	0.0368	0.0438
TE ↓	hold_rising to CP	-0.0101	-0.0149	-0.0225	-0.0269
TE ↑	hold_rising to CP	0.0036	-0.0013	-0.0035	-0.0093
TE ↓	setup_rising to CP	0.0408	0.0425	0.0502	0.0571
TE ↑	setup_rising to CP	0.0293	0.0314	0.0384	0.0465
		C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP ↓	min_pulse_width to CP	0.0340	0.0362	0.0423	0.0492
E ↓	hold_rising to CP	-0.0127	-0.0181	-0.0220	-0.0295
E ↑	hold_rising to CP	0.0036	-0.0017	-0.0013	-0.0067
E ↓	setup_rising to CP	0.0371	0.0420	0.0495	0.0572
E ↑	setup_rising to CP	0.0265	0.0314	0.0368	0.0438
TE ↓	hold_rising to CP	-0.0101	-0.0149	-0.0225	-0.0269
TE ↑	hold_rising to CP	0.0004	-0.0013	-0.0035	-0.0093
TE ↓	setup_rising to CP	0.0408	0.0457	0.0502	0.0571
TE ↑	setup_rising to CP	0.0293	0.0314	0.0384	0.0465
		C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP ↓	min_pulse_width to CP	0.0335	0.0380	0.0425	0.0495
E ↓	hold_rising to CP	-0.0127	-0.0171	-0.0247	-0.0291
E ↑	hold_rising to CP	0.0036	0.0036	-0.0013	-0.0035
E ↓	setup_rising to CP	0.0404	0.0420	0.0527	0.0598
E ↑	setup_rising to CP	0.0265	0.0314	0.0385	0.0465
TE ↓	hold_rising to CP	-0.0133	-0.0176	-0.0252	-0.0328
TE ↑	hold_rising to CP	0.0036	-0.0017	-0.0039	-0.0035
TE ↓	setup_rising to CP	0.0408	0.0457	0.0528	0.0567
TE ↑	setup_rising to CP	0.0293	0.0309	0.0416	0.0491

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LLP1_CNHLSX10_P0	2.306e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX10_P4	4.407e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX10_P10	8.990e-07	1.000e-20
C8T28SOI_LLP1_CNHLSX10_P16	4.324e-07	1.000e-20
C8T28SOI_LLP1_CNHLSX14_P0	2.796e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX14_P4	5.279e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX14_P10	1.055e-06	1.000e-20

C8T28SOI_LLP1_CNHLSX14_P16	4.990e-07	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P0	3.637e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P4	6.871e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P10	1.367e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX19_P16	6.436e-07	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P0	4.100e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P4	7.706e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P10	1.518e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX24_P16	7.087e-07	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P0	5.032e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P4	9.306e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P10	1.793e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX29_P16	8.256e-07	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P0	5.496e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P4	1.014e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P10	1.944e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX34_P16	8.908e-07	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P0	5.959e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P4	1.098e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P10	2.096e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX38_P16	9.559e-07	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P0	8.104e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P4	1.507e-05	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P10	2.897e-06	1.000e-20
C8T28SOI_LLP1_CNHLSX57_P16	1.322e-06	1.000e-20
C8T28SOI_LLP_CNHLSX4_P0	1.818e-05	1.000e-20
C8T28SOI_LLP_CNHLSX4_P4	3.474e-06	1.000e-20
C8T28SOI_LLP_CNHLSX4_P10	7.054e-07	1.000e-20
C8T28SOI_LLP_CNHLSX4_P16	3.329e-07	1.000e-20
C8T28SOI_LLP_CNHLSX9_P0	2.587e-05	1.000e-20
C8T28SOI_LLP_CNHLSX9_P4	4.826e-06	1.000e-20
C8T28SOI_LLP_CNHLSX9_P10	9.460e-07	1.000e-20
C8T28SOI_LLP_CNHLSX9_P16	4.351e-07	1.000e-20
C8T28SOI_LLP_CNHLSX13_P0	3.001e-05	1.000e-20
C8T28SOI_LLP_CNHLSX13_P4	5.580e-06	1.000e-20
C8T28SOI_LLP_CNHLSX13_P10	1.082e-06	1.000e-20
C8T28SOI_LLP_CNHLSX13_P16	4.931e-07	1.000e-20
C8T28SOI_LLP_CNHLSX17_P0	3.527e-05	1.000e-20
C8T28SOI_LLP_CNHLSX17_P4	6.452e-06	1.000e-20
C8T28SOI_LLP_CNHLSX17_P10	1.228e-06	1.000e-20
C8T28SOI_LLP_CNHLSX17_P16	5.528e-07	1.000e-20
C8T28SOI_LLP_CNHLSX21_P0	3.767e-05	1.000e-20
C8T28SOI_LLP_CNHLSX21_P4	7.012e-06	1.000e-20
C8T28SOI_LLP_CNHLSX21_P10	1.348e-06	1.000e-20
C8T28SOI_LLP_CNHLSX21_P16	6.079e-07	1.000e-20
C8T28SOI_LLP_CNHLSX27_P0	5.428e-05	1.000e-20
C8T28SOI_LLP_CNHLSX27_P4	9.777e-06	1.000e-20
C8T28SOI_LLP_CNHLSX27_P10	1.828e-06	1.000e-20
C8T28SOI_LLP_CNHLSX27_P16	8.169e-07	1.000e-20
C8T28SOI_LLP_CNHLSX30_P0	5.928e-05	1.000e-20
C8T28SOI_LLP_CNHLSX30_P4	1.067e-05	1.000e-20
C8T28SOI_LLP_CNHLSX30_P10	1.988e-06	1.000e-20

C8T28SOI_LLP_CNHLSX30_P16	8.827e-07	1.000e-20
C8T28SOI_LLP_CNHLSX38_P0	6.844e-05	1.000e-20
C8T28SOI_LLP_CNHLSX38_P4	1.223e-05	1.000e-20
C8T28SOI_LLP_CNHLSX38_P10	2.252e-06	1.000e-20
C8T28SOI_LLP_CNHLSX38_P16	9.904e-07	1.000e-20
C8T28SOI_LLP_CNHLSX54_P0	1.023e-04	1.000e-20
C8T28SOI_LLP_CNHLSX54_P4	1.827e-05	1.000e-20
C8T28SOI_LLP_CNHLSX54_P10	3.349e-06	1.000e-20
C8T28SOI_LLP_CNHLSX54_P16	1.463e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LLP1_-CNHLSX10_P0	C8T28SOI_LLP1_-CNHLSX10_P4	C8T28SOI_LLP1_-CNHLSX10_P10	C8T28SOI_LLP1_-CNHLSX10_P16
CP (output stable)	1.350e-03	1.361e-03	1.403e-03	1.449e-03
E (output stable)	9.844e-04	9.561e-04	9.614e-04	9.954e-04
TE (output stable)	1.036e-03	1.032e-03	1.069e-03	1.125e-03
CP to Q	3.612e-03	3.522e-03	3.541e-03	3.614e-03
	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P10	C8T28SOI_LLP1_-CNHLSX14_P16
CP (output stable)	1.352e-03	1.362e-03	1.408e-03	1.452e-03
E (output stable)	9.845e-04	9.558e-04	9.611e-04	9.951e-04
TE (output stable)	1.036e-03	1.031e-03	1.069e-03	1.125e-03
CP to Q	4.529e-03	4.345e-03	4.318e-03	4.383e-03
	C8T28SOI_LLP1_-CNHLSX19_P0	C8T28SOI_LLP1_-CNHLSX19_P4	C8T28SOI_LLP1_-CNHLSX19_P10	C8T28SOI_LLP1_-CNHLSX19_P16
CP (output stable)	1.920e-03	1.954e-03	2.022e-03	2.068e-03
E (output stable)	1.072e-03	1.046e-03	1.056e-03	1.095e-03
TE (output stable)	1.124e-03	1.122e-03	1.164e-03	1.225e-03
CP to Q	5.698e-03	5.490e-03	5.485e-03	5.579e-03
	C8T28SOI_LLP1_-CNHLSX24_P0	C8T28SOI_LLP1_-CNHLSX24_P4	C8T28SOI_LLP1_-CNHLSX24_P10	C8T28SOI_LLP1_-CNHLSX24_P16
CP (output stable)	1.936e-03	1.969e-03	2.034e-03	2.080e-03
E (output stable)	1.073e-03	1.047e-03	1.056e-03	1.096e-03
TE (output stable)	1.125e-03	1.122e-03	1.165e-03	1.226e-03
CP to Q	6.819e-03	6.544e-03	6.519e-03	6.631e-03
	C8T28SOI_LLP1_-CNHLSX29_P0	C8T28SOI_LLP1_-CNHLSX29_P4	C8T28SOI_LLP1_-CNHLSX29_P10	C8T28SOI_LLP1_-CNHLSX29_P16
CP (output stable)	2.124e-03	2.162e-03	2.246e-03	2.300e-03
E (output stable)	1.146e-03	1.121e-03	1.138e-03	1.184e-03
TE (output stable)	1.196e-03	1.196e-03	1.246e-03	1.313e-03
CP to Q	7.808e-03	7.472e-03	7.436e-03	7.565e-03
	C8T28SOI_LLP1_-CNHLSX34_P0	C8T28SOI_LLP1_-CNHLSX34_P4	C8T28SOI_LLP1_-CNHLSX34_P10	C8T28SOI_LLP1_-CNHLSX34_P16
CP (output stable)	2.127e-03	2.166e-03	2.225e-03	2.300e-03
E (output stable)	1.145e-03	1.122e-03	1.138e-03	1.184e-03
TE (output stable)	1.197e-03	1.198e-03	1.246e-03	1.314e-03
CP to Q	8.889e-03	8.483e-03	8.491e-03	8.556e-03
	C8T28SOI_LLP1_-CNHLSX38_P0	C8T28SOI_LLP1_-CNHLSX38_P4	C8T28SOI_LLP1_-CNHLSX38_P10	C8T28SOI_LLP1_-CNHLSX38_P16
CP (output stable)	2.126e-03	2.165e-03	2.234e-03	2.303e-03
E (output stable)	1.146e-03	1.122e-03	1.139e-03	1.185e-03
TE (output stable)	1.197e-03	1.197e-03	1.246e-03	1.314e-03

CP to Q	9.930e-03	9.418e-03	9.363e-03	9.398e-03
	C8T28SOI_LLP1_-CNHLSX57_P0	C8T28SOI_LLP1_-CNHLSX57_P4	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP (output stable)	2.753e-03	2.823e-03	2.931e-03	3.034e-03
E (output stable)	1.220e-03	1.199e-03	1.219e-03	1.268e-03
TE (output stable)	1.272e-03	1.275e-03	1.327e-03	1.398e-03
CP to Q	1.447e-02	1.374e-02	1.364e-02	1.376e-02
	C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP (output stable)	1.825e-03	1.819e-03	1.862e-03	1.924e-03
E (output stable)	9.966e-04	9.540e-04	9.391e-04	9.478e-04
TE (output stable)	1.052e-03	1.034e-03	1.044e-03	1.074e-03
CP to Q	2.465e-03	2.357e-03	2.329e-03	2.372e-03
	C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP (output stable)	1.910e-03	1.909e-03	1.964e-03	2.032e-03
E (output stable)	9.613e-04	9.230e-04	9.108e-04	9.213e-04
TE (output stable)	1.018e-03	1.004e-03	1.017e-03	1.049e-03
CP to Q	3.331e-03	3.170e-03	3.125e-03	3.182e-03
	C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP (output stable)	1.951e-03	1.953e-03	2.007e-03	2.077e-03
E (output stable)	9.673e-04	9.290e-04	9.185e-04	9.297e-04
TE (output stable)	1.024e-03	1.010e-03	1.025e-03	1.057e-03
CP to Q	4.413e-03	4.184e-03	4.118e-03	4.189e-03
	C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP (output stable)	1.954e-03	1.955e-03	2.006e-03	2.079e-03
E (output stable)	9.679e-04	9.294e-04	9.187e-04	9.300e-04
TE (output stable)	1.025e-03	1.011e-03	1.025e-03	1.057e-03
CP to Q	5.473e-03	5.128e-03	5.040e-03	5.029e-03
	C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP (output stable)	1.951e-03	1.951e-03	2.008e-03	2.077e-03
E (output stable)	9.674e-04	9.298e-04	9.189e-04	9.300e-04
TE (output stable)	1.024e-03	1.011e-03	1.025e-03	1.057e-03
CP to Q	6.775e-03	6.282e-03	6.062e-03	6.071e-03
	C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP (output stable)	2.677e-03	2.714e-03	2.805e-03	2.906e-03
E (output stable)	1.087e-03	1.050e-03	1.045e-03	1.062e-03
TE (output stable)	1.144e-03	1.132e-03	1.152e-03	1.189e-03
CP to Q	7.832e-03	7.432e-03	7.383e-03	7.499e-03
	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP (output stable)	2.669e-03	2.706e-03	2.814e-03	2.907e-03
E (output stable)	1.086e-03	1.049e-03	1.045e-03	1.061e-03
TE (output stable)	1.143e-03	1.131e-03	1.151e-03	1.189e-03
CP to Q	8.838e-03	8.372e-03	8.324e-03	8.417e-03
	C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP (output stable)	2.674e-03	2.710e-03	2.824e-03	2.909e-03
E (output stable)	1.085e-03	1.049e-03	1.044e-03	1.060e-03

TE (output stable)	1.142e-03	1.130e-03	1.150e-03	1.188e-03
CP to Q	1.088e-02	1.007e-02	9.953e-03	1.003e-02
	C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP (output stable)	3.997e-03	4.124e-03	4.314e-03	4.482e-03
E (output stable)	1.181e-03	1.152e-03	1.158e-03	1.184e-03
TE (output stable)	1.238e-03	1.233e-03	1.264e-03	1.312e-03
CP to Q	1.443e-02	1.355e-02	1.353e-02	1.365e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	C8T28SOI_LLP1_-CNHLSX10_P0	C8T28SOI_LLP1_-CNHLSX10_P4	C8T28SOI_LLP1_-CNHLSX10_P10	C8T28SOI_LLP1_-CNHLSX10_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX14_P0	C8T28SOI_LLP1_-CNHLSX14_P4	C8T28SOI_LLP1_-CNHLSX14_P10	C8T28SOI_LLP1_-CNHLSX14_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX19_P0	C8T28SOI_LLP1_-CNHLSX19_P4	C8T28SOI_LLP1_-CNHLSX19_P10	C8T28SOI_LLP1_-CNHLSX19_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX24_P0	C8T28SOI_LLP1_-CNHLSX24_P4	C8T28SOI_LLP1_-CNHLSX24_P10	C8T28SOI_LLP1_-CNHLSX24_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX29_P0	C8T28SOI_LLP1_-CNHLSX29_P4	C8T28SOI_LLP1_-CNHLSX29_P10	C8T28SOI_LLP1_-CNHLSX29_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX34_P0	C8T28SOI_LLP1_-CNHLSX34_P4	C8T28SOI_LLP1_-CNHLSX34_P10	C8T28SOI_LLP1_-CNHLSX34_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP1_-CNHLSX38_P0	C8T28SOI_LLP1_-CNHLSX38_P4	C8T28SOI_LLP1_-CNHLSX38_P10	C8T28SOI_LLP1_-CNHLSX38_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

	C8T28SOI_LLP1_-CNHLSX57_P0	C8T28SOI_LLP1_-CNHLSX57_P4	C8T28SOI_LLP1_-CNHLSX57_P10	C8T28SOI_LLP1_-CNHLSX57_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX4_P0	C8T28SOI_LLP_-CNHLSX4_P4	C8T28SOI_LLP_-CNHLSX4_P10	C8T28SOI_LLP_-CNHLSX4_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX9_P0	C8T28SOI_LLP_-CNHLSX9_P4	C8T28SOI_LLP_-CNHLSX9_P10	C8T28SOI_LLP_-CNHLSX9_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX13_P0	C8T28SOI_LLP_-CNHLSX13_P4	C8T28SOI_LLP_-CNHLSX13_P10	C8T28SOI_LLP_-CNHLSX13_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX17_P0	C8T28SOI_LLP_-CNHLSX17_P4	C8T28SOI_LLP_-CNHLSX17_P10	C8T28SOI_LLP_-CNHLSX17_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX21_P0	C8T28SOI_LLP_-CNHLSX21_P4	C8T28SOI_LLP_-CNHLSX21_P10	C8T28SOI_LLP_-CNHLSX21_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX27_P0	C8T28SOI_LLP_-CNHLSX27_P4	C8T28SOI_LLP_-CNHLSX27_P10	C8T28SOI_LLP_-CNHLSX27_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX30_P0	C8T28SOI_LLP_-CNHLSX30_P4	C8T28SOI_LLP_-CNHLSX30_P10	C8T28SOI_LLP_-CNHLSX30_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX38_P0	C8T28SOI_LLP_-CNHLSX38_P4	C8T28SOI_LLP_-CNHLSX38_P10	C8T28SOI_LLP_-CNHLSX38_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

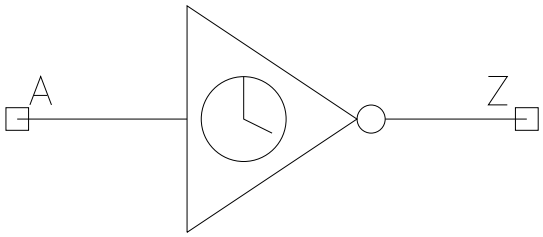
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LLP_-CNHLSX54_P0	C8T28SOI_LLP_-CNHLSX54_P4	C8T28SOI_LLP_-CNHLSX54_P10	C8T28SOI_LLP_-CNHLSX54_P16
CP (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
E (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
TE (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
CP to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNIV

Cell Description

Inverter with Balanced rise and fall delays for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_CNIVX2_P0	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX2_P4	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX2_-P10	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX2_-P16	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_P0	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_P4	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_-P10	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX4_-P16	0.800	0.272	0.2176
C8T28SOI_LL_CNIVX9_P0	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX9_P4	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX9_-P10	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX9_-P16	0.800	0.408	0.3264
C8T28SOI_LL_CNIVX14_-P0	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX14_-P4	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX14_-P10	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX14_-P16	0.800	0.544	0.4352
C8T28SOI_LL_CNIVX18_-P0	0.800	0.680	0.5440
C8T28SOI_LL_CNIVX18_-P4	0.800	0.680	0.5440
C8T28SOI_LL_CNIVX18_-P10	0.800	0.680	0.5440
C8T28SOI_LL_CNIVX18_-P16	0.800	0.680	0.5440

C8T28SOI_LL_CNIVX22_P0	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX22_P4	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX22_P10	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX22_P16	0.800	0.816	0.6528
C8T28SOI_LL_CNIVX27_P0	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX27_P4	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX27_P10	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX27_P16	0.800	0.952	0.7616
C8T28SOI_LL_CNIVX32_P0	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX32_P4	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX32_P10	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX32_P16	0.800	1.088	0.8704
C8T28SOI_LL_CNIVX37_P0	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX37_P4	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX37_P10	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX37_P16	0.800	1.224	0.9792
C8T28SOI_LL_CNIVX74_P0	0.800	2.312	1.8496
C8T28SOI_LL_CNIVX74_P4	0.800	2.312	1.8496
C8T28SOI_LL_CNIVX74_P10	0.800	2.312	1.8496
C8T28SOI_LL_CNIVX74_P16	0.800	2.312	1.8496
C8T28SOIDV_LL_CNIVX18_P0	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX18_P4	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX18_P10	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX18_P16	1.600	0.408	0.6528
C8T28SOIDV_LL_CNIVX28_P0	1.600	0.544	0.8704
C8T28SOIDV_LL_CNIVX28_P4	1.600	0.544	0.8704

C8T28SOIDV_LL_-CNIVX28_P10	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNIVX28_P16	1.600	0.544	0.8704
C8T28SOIDV_LL_-CNIVX37_P0	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX37_P4	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX37_P10	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX37_P16	1.600	0.680	1.0880
C8T28SOIDV_LL_-CNIVX55_P0	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX55_P4	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX55_P10	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX55_P16	1.600	0.952	1.5232
C8T28SOIDV_LL_-CNIVX74_P0	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNIVX74_P4	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNIVX74_P10	1.600	1.224	1.9584
C8T28SOIDV_LL_-CNIVX74_P16	1.600	1.224	1.9584

Truth Table

A	Z
A	!A

Pin Capacitance

Pin	C8T28SOI_LL_-CNIVX2_P0	C8T28SOI_LL_-CNIVX2_P4	C8T28SOI_LL_-CNIVX2_P10	C8T28SOI_LL_-CNIVX2_P16
A	0.0004	0.0004	0.0004	0.0004
	C8T28SOI_LL_-CNIVX4_P0	C8T28SOI_LL_-CNIVX4_P4	C8T28SOI_LL_-CNIVX4_P10	C8T28SOI_LL_-CNIVX4_P16
A	0.0005	0.0005	0.0006	0.0006
	C8T28SOI_LL_-CNIVX9_P0	C8T28SOI_LL_-CNIVX9_P4	C8T28SOI_LL_-CNIVX9_P10	C8T28SOI_LL_-CNIVX9_P16
A	0.0010	0.0010	0.0010	0.0011
	C8T28SOI_LL_-CNIVX14_P0	C8T28SOI_LL_-CNIVX14_P4	C8T28SOI_LL_-CNIVX14_P10	C8T28SOI_LL_-CNIVX14_P16
A	0.0014	0.0015	0.0016	0.0016
	C8T28SOI_LL_-CNIVX18_P0	C8T28SOI_LL_-CNIVX18_P4	C8T28SOI_LL_-CNIVX18_P10	C8T28SOI_LL_-CNIVX18_P16
A	0.0018	0.0019	0.0020	0.0022
	C8T28SOI_LL_-CNIVX22_P0	C8T28SOI_LL_-CNIVX22_P4	C8T28SOI_LL_-CNIVX22_P10	C8T28SOI_LL_-CNIVX22_P16
A	0.0024	0.0024	0.0026	0.0027

	C8T28SOI_LL_-CNIVX27_P0	C8T28SOI_LL_-CNIVX27_P4	C8T28SOI_LL_-CNIVX27_P10	C8T28SOI_LL_-CNIVX27_P16
A	0.0028	0.0029	0.0031	0.0032
	C8T28SOI_LL_-CNIVX32_P0	C8T28SOI_LL_-CNIVX32_P4	C8T28SOI_LL_-CNIVX32_P10	C8T28SOI_LL_-CNIVX32_P16
A	0.0033	0.0034	0.0036	0.0038
	C8T28SOI_LL_-CNIVX37_P0	C8T28SOI_LL_-CNIVX37_P4	C8T28SOI_LL_-CNIVX37_P10	C8T28SOI_LL_-CNIVX37_P16
A	0.0037	0.0039	0.0041	0.0043
	C8T28SOI_LL_-CNIVX74_P0	C8T28SOI_LL_-CNIVX74_P4	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A	0.0077	0.0080	0.0083	0.0089
	C8T28SOIDV_LL_-CNIVX18_P0	C8T28SOIDV_LL_-CNIVX18_P4	C8T28SOIDV_LL_-CNIVX18_P10	C8T28SOIDV_LL_-CNIVX18_P16
A	0.0018	0.0019	0.0020	0.0021
	C8T28SOIDV_LL_-CNIVX28_P0	C8T28SOIDV_LL_-CNIVX28_P4	C8T28SOIDV_LL_-CNIVX28_P10	C8T28SOIDV_LL_-CNIVX28_P16
A	0.0028	0.0029	0.0030	0.0032
	C8T28SOIDV_LL_-CNIVX37_P0	C8T28SOIDV_LL_-CNIVX37_P4	C8T28SOIDV_LL_-CNIVX37_P10	C8T28SOIDV_LL_-CNIVX37_P16
A	0.0036	0.0038	0.0040	0.0042
	C8T28SOIDV_LL_-CNIVX55_P0	C8T28SOIDV_LL_-CNIVX55_P4	C8T28SOIDV_LL_-CNIVX55_P10	C8T28SOIDV_LL_-CNIVX55_P16
A	0.0055	0.0057	0.0060	0.0065
	C8T28SOIDV_LL_-CNIVX74_P0	C8T28SOIDV_LL_-CNIVX74_P4	C8T28SOIDV_LL_-CNIVX74_P10	C8T28SOIDV_LL_-CNIVX74_P16
A	0.0076	0.0078	0.0082	0.0087

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-CNIVX2_P0	**C8T28SOI_LL_-CNIVX2_P4**	**C8T28SOI_LL_-CNIVX2_P0**	**C8T28SOI_LL_-CNIVX2_P4**
A to Z ↓	0.0060	0.0071	5.7454	6.0792
A to Z ↑	0.0100	0.0114	7.0326	7.7398
	C8T28SOI_LL_-CNIVX2_P10	**C8T28SOI_LL_-CNIVX2_P16**	**C8T28SOI_LL_-CNIVX2_P10**	**C8T28SOI_LL_-CNIVX2_P16**
A to Z ↓	0.0085	0.0096	6.5300	6.9342
A to Z ↑	0.0131	0.0146	8.7157	9.6140
	C8T28SOI_LL_-CNIVX4_P0	**C8T28SOI_LL_-CNIVX4_P4**	**C8T28SOI_LL_-CNIVX4_P0**	**C8T28SOI_LL_-CNIVX4_P4**
A to Z ↓	0.0046	0.0056	3.0302	3.2058
A to Z ↑	0.0087	0.0098	4.3610	4.7559
	C8T28SOI_LL_-CNIVX4_P10	**C8T28SOI_LL_-CNIVX4_P16**	**C8T28SOI_LL_-CNIVX4_P10**	**C8T28SOI_LL_-CNIVX4_P16**
A to Z ↓	0.0068	0.0077	3.4509	3.6678
A to Z ↑	0.0113	0.0124	5.3078	5.8117
	C8T28SOI_LL_-CNIVX9_P0	**C8T28SOI_LL_-CNIVX9_P4**	**C8T28SOI_LL_-CNIVX9_P0**	**C8T28SOI_LL_-CNIVX9_P4**
A to Z ↓	0.0036	0.0045	1.4630	1.5484
A to Z ↑	0.0072	0.0081	2.0010	2.1772
	C8T28SOI_LL_-CNIVX9_P10	**C8T28SOI_LL_-CNIVX9_P16**	**C8T28SOI_LL_-CNIVX9_P10**	**C8T28SOI_LL_-CNIVX9_P16**
A to Z ↓	0.0056	0.0064	1.6687	1.7734

A to Z ↑	0.0093	0.0104	2.4249	2.6501
	C8T28SOI_LL_-CNIVX14_P0	**C8T28SOI_LL_-CNIVX14_P4**	**C8T28SOI_LL_-CNIVX14_P0**	**C8T28SOI_LL_-CNIVX14_P4**
A to Z ↓	0.0040	0.0048	0.9905	1.0487
A to Z ↑	0.0073	0.0082	1.3643	1.4839
	C8T28SOI_LL_-CNIVX14_P10	**C8T28SOI_LL_-CNIVX14_P16**	**C8T28SOI_LL_-CNIVX14_P10**	**C8T28SOI_LL_-CNIVX14_P16**
A to Z ↓	0.0059	0.0067	1.1302	1.2017
A to Z ↑	0.0095	0.0106	1.6518	1.8066
	C8T28SOI_LL_-CNIVX18_P0	**C8T28SOI_LL_-CNIVX18_P4**	**C8T28SOI_LL_-CNIVX18_P0**	**C8T28SOI_LL_-CNIVX18_P4**
A to Z ↓	0.0043	0.0052	0.7801	0.8285
A to Z ↑	0.0074	0.0084	1.0328	1.1217
	C8T28SOI_LL_-CNIVX18_P10	**C8T28SOI_LL_-CNIVX18_P16**	**C8T28SOI_LL_-CNIVX18_P10**	**C8T28SOI_LL_-CNIVX18_P16**
A to Z ↓	0.0063	0.0073	0.8934	0.9518
A to Z ↑	0.0097	0.0109	1.2485	1.3653
	C8T28SOI_LL_-CNIVX22_P0	**C8T28SOI_LL_-CNIVX22_P4**	**C8T28SOI_LL_-CNIVX22_P0**	**C8T28SOI_LL_-CNIVX22_P4**
A to Z ↓	0.0040	0.0048	0.6272	0.6655
A to Z ↑	0.0070	0.0079	0.8232	0.8952
	C8T28SOI_LL_-CNIVX22_P10	**C8T28SOI_LL_-CNIVX22_P16**	**C8T28SOI_LL_-CNIVX22_P10**	**C8T28SOI_LL_-CNIVX22_P16**
A to Z ↓	0.0059	0.0068	0.7181	0.7639
A to Z ↑	0.0091	0.0102	0.9961	1.0884
	C8T28SOI_LL_-CNIVX27_P0	**C8T28SOI_LL_-CNIVX27_P4**	**C8T28SOI_LL_-CNIVX27_P0**	**C8T28SOI_LL_-CNIVX27_P4**
A to Z ↓	0.0044	0.0053	0.5218	0.5541
A to Z ↑	0.0073	0.0083	0.6846	0.7440
	C8T28SOI_LL_-CNIVX27_P10	**C8T28SOI_LL_-CNIVX27_P16**	**C8T28SOI_LL_-CNIVX27_P10**	**C8T28SOI_LL_-CNIVX27_P16**
A to Z ↓	0.0065	0.0073	0.5974	0.6367
A to Z ↑	0.0096	0.0107	0.8273	0.9050
	C8T28SOI_LL_-CNIVX32_P0	**C8T28SOI_LL_-CNIVX32_P4**	**C8T28SOI_LL_-CNIVX32_P0**	**C8T28SOI_LL_-CNIVX32_P4**
A to Z ↓	0.0044	0.0053	0.4310	0.4573
A to Z ↑	0.0074	0.0084	0.5847	0.6350
	C8T28SOI_LL_-CNIVX32_P10	**C8T28SOI_LL_-CNIVX32_P16**	**C8T28SOI_LL_-CNIVX32_P10**	**C8T28SOI_LL_-CNIVX32_P16**
A to Z ↓	0.0064	0.0073	0.4929	0.5252
A to Z ↑	0.0096	0.0107	0.7071	0.7733
	C8T28SOI_LL_-CNIVX37_P0	**C8T28SOI_LL_-CNIVX37_P4**	**C8T28SOI_LL_-CNIVX37_P0**	**C8T28SOI_LL_-CNIVX37_P4**
A to Z ↓	0.0044	0.0054	0.3815	0.4048
A to Z ↑	0.0074	0.0084	0.5158	0.5602
	C8T28SOI_LL_-CNIVX37_P10	**C8T28SOI_LL_-CNIVX37_P16**	**C8T28SOI_LL_-CNIVX37_P10**	**C8T28SOI_LL_-CNIVX37_P16**
A to Z ↓	0.0065	0.0073	0.4366	0.4653
A to Z ↑	0.0097	0.0108	0.6234	0.6815
	C8T28SOI_LL_-CNIVX74_P0	**C8T28SOI_LL_-CNIVX74_P4**	**C8T28SOI_LL_-CNIVX74_P0**	**C8T28SOI_LL_-CNIVX74_P4**
A to Z ↓	0.0067	0.0078	0.1937	0.2055
A to Z ↑	0.0095	0.0107	0.2607	0.2829

	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A to Z ↓	0.0090	0.0101	0.2218	0.2362
A to Z ↑	0.0120	0.0132	0.3152	0.3440
	C8T28SOIDV_LL_-CNIVX18_P0	**C8T28SOIDV_LL_-CNIVX18_P4**	**C8T28SOIDV_LL_-CNIVX18_P0**	**C8T28SOIDV_LL_-CNIVX18_P4**
A to Z ↓	0.0040	0.0048	0.7320	0.7771
A to Z ↑	0.0069	0.0078	0.9945	1.0828
	C8T28SOIDV_LL_-CNIVX18_P10	**C8T28SOIDV_LL_-CNIVX18_P16**	**C8T28SOIDV_LL_-CNIVX18_P10**	**C8T28SOIDV_LL_-CNIVX18_P16**
A to Z ↓	0.0060	0.0068	0.8384	0.8918
A to Z ↑	0.0092	0.0102	1.2071	1.3206
	C8T28SOIDV_LL_-CNIVX28_P0	**C8T28SOIDV_LL_-CNIVX28_P4**	**C8T28SOIDV_LL_-CNIVX28_P0**	**C8T28SOIDV_LL_-CNIVX28_P4**
A to Z ↓	0.0043	0.0051	0.4989	0.5301
A to Z ↑	0.0070	0.0079	0.6648	0.7236
	C8T28SOIDV_LL_-CNIVX28_P10	**C8T28SOIDV_LL_-CNIVX28_P16**	**C8T28SOIDV_LL_-CNIVX28_P10**	**C8T28SOIDV_LL_-CNIVX28_P16**
A to Z ↓	0.0062	0.0070	0.5722	0.6090
A to Z ↑	0.0092	0.0103	0.8067	0.8826
	C8T28SOIDV_LL_-CNIVX37_P0	**C8T28SOIDV_LL_-CNIVX37_P4**	**C8T28SOIDV_LL_-CNIVX37_P0**	**C8T28SOIDV_LL_-CNIVX37_P4**
A to Z ↓	0.0041	0.0049	0.3755	0.3990
A to Z ↑	0.0066	0.0076	0.4986	0.5425
	C8T28SOIDV_LL_-CNIVX37_P10	**C8T28SOIDV_LL_-CNIVX37_P16**	**C8T28SOIDV_LL_-CNIVX37_P10**	**C8T28SOIDV_LL_-CNIVX37_P16**
A to Z ↓	0.0060	0.0067	0.4303	0.4589
A to Z ↑	0.0089	0.0098	0.6046	0.6613
	C8T28SOIDV_LL_-CNIVX55_P0	**C8T28SOIDV_LL_-CNIVX55_P4**	**C8T28SOIDV_LL_-CNIVX55_P0**	**C8T28SOIDV_LL_-CNIVX55_P4**
A to Z ↓	0.0042	0.0050	0.2530	0.2690
A to Z ↑	0.0066	0.0075	0.3337	0.3632
	C8T28SOIDV_LL_-CNIVX55_P10	**C8T28SOIDV_LL_-CNIVX55_P16**	**C8T28SOIDV_LL_-CNIVX55_P10**	**C8T28SOIDV_LL_-CNIVX55_P16**
A to Z ↓	0.0060	0.0069	0.2902	0.3095
A to Z ↑	0.0087	0.0098	0.4044	0.4425
	C8T28SOIDV_LL_-CNIVX74_P0	**C8T28SOIDV_LL_-CNIVX74_P4**	**C8T28SOIDV_LL_-CNIVX74_P0**	**C8T28SOIDV_LL_-CNIVX74_P4**
A to Z ↓	0.0047	0.0055	0.1937	0.2055
A to Z ↑	0.0069	0.0079	0.2523	0.2741
	C8T28SOIDV_LL_-CNIVX74_P10	**C8T28SOIDV_LL_-CNIVX74_P16**	**C8T28SOIDV_LL_-CNIVX74_P10**	**C8T28SOIDV_LL_-CNIVX74_P16**
A to Z ↓	0.0065	0.0074	0.2220	0.2362
A to Z ↑	0.0091	0.0102	0.3056	0.3338

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_CNIVX2_P0	1.806e-06	1.000e-20
C8T28SOI_LL_CNIVX2_P4	3.546e-07	1.000e-20
C8T28SOI_LL_CNIVX2_P10	7.421e-08	1.000e-20
C8T28SOI_LL_CNIVX2_P16	3.444e-08	1.000e-20
C8T28SOI_LL_CNIVX4_P0	4.054e-06	1.000e-20

C8T28SOI_LL_CNIVX4_P4	7.761e-07	1.000e-20
C8T28SOI_LL_CNIVX4_P10	1.516e-07	1.000e-20
C8T28SOI_LL_CNIVX4_P16	6.549e-08	1.000e-20
C8T28SOI_LL_CNIVX9_P0	8.707e-06	1.000e-20
C8T28SOI_LL_CNIVX9_P4	1.663e-06	1.000e-20
C8T28SOI_LL_CNIVX9_P10	3.194e-07	1.000e-20
C8T28SOI_LL_CNIVX9_P16	1.361e-07	1.000e-20
C8T28SOI_LL_CNIVX14_P0	1.307e-05	1.000e-20
C8T28SOI_LL_CNIVX14_P4	2.446e-06	1.000e-20
C8T28SOI_LL_CNIVX14_P10	4.635e-07	1.000e-20
C8T28SOI_LL_CNIVX14_P16	1.983e-07	1.000e-20
C8T28SOI_LL_CNIVX18_P0	1.618e-05	1.000e-20
C8T28SOI_LL_CNIVX18_P4	3.069e-06	1.000e-20
C8T28SOI_LL_CNIVX18_P10	5.830e-07	1.000e-20
C8T28SOI_LL_CNIVX18_P16	2.488e-07	1.000e-20
C8T28SOI_LL_CNIVX22_P0	1.989e-05	1.000e-20
C8T28SOI_LL_CNIVX22_P4	3.768e-06	1.000e-20
C8T28SOI_LL_CNIVX22_P10	7.151e-07	1.000e-20
C8T28SOI_LL_CNIVX22_P16	3.057e-07	1.000e-20
C8T28SOI_LL_CNIVX27_P0	2.360e-05	1.000e-20
C8T28SOI_LL_CNIVX27_P4	4.468e-06	1.000e-20
C8T28SOI_LL_CNIVX27_P10	8.474e-07	1.000e-20
C8T28SOI_LL_CNIVX27_P16	3.628e-07	1.000e-20
C8T28SOI_LL_CNIVX32_P0	2.752e-05	1.000e-20
C8T28SOI_LL_CNIVX32_P4	5.231e-06	1.000e-20
C8T28SOI_LL_CNIVX32_P10	9.978e-07	1.000e-20
C8T28SOI_LL_CNIVX32_P16	4.298e-07	1.000e-20
C8T28SOI_LL_CNIVX37_P0	3.126e-05	1.000e-20
C8T28SOI_LL_CNIVX37_P4	5.939e-06	1.000e-20
C8T28SOI_LL_CNIVX37_P10	1.133e-06	1.000e-20
C8T28SOI_LL_CNIVX37_P16	4.882e-07	1.000e-20
C8T28SOI_LL_CNIVX74_P0	6.116e-05	1.000e-20
C8T28SOI_LL_CNIVX74_P4	1.160e-05	1.000e-20
C8T28SOI_LL_CNIVX74_P10	2.210e-06	1.000e-20
C8T28SOI_LL_CNIVX74_P16	9.556e-07	1.000e-20
C8T28SOIDV_LL_CNIVX18_P0	1.848e-05	1.000e-20
C8T28SOIDV_LL_CNIVX18_P4	3.477e-06	1.000e-20
C8T28SOIDV_LL_CNIVX18_P10	6.499e-07	1.000e-20
C8T28SOIDV_LL_CNIVX18_P16	2.693e-07	1.000e-20
C8T28SOIDV_LL_CNIVX28_P0	2.828e-05	1.000e-20
C8T28SOIDV_LL_CNIVX28_P4	5.193e-06	1.000e-20
C8T28SOIDV_LL_CNIVX28_P10	9.492e-07	1.000e-20
C8T28SOIDV_LL_CNIVX28_P16	3.911e-07	1.000e-20
C8T28SOIDV_LL_CNIVX37_P0	3.723e-05	1.000e-20
C8T28SOIDV_LL_CNIVX37_P4	6.791e-06	1.000e-20
C8T28SOIDV_LL_CNIVX37_P10	1.234e-06	1.000e-20
C8T28SOIDV_LL_CNIVX37_P16	5.084e-07	1.000e-20
C8T28SOIDV_LL_CNIVX55_P0	5.511e-05	1.000e-20
C8T28SOIDV_LL_CNIVX55_P4	9.984e-06	1.000e-20
C8T28SOIDV_LL_CNIVX55_P10	1.802e-06	1.000e-20
C8T28SOIDV_LL_CNIVX55_P16	7.429e-07	1.000e-20
C8T28SOIDV_LL_CNIVX74_P0	7.342e-05	1.000e-20

C8T28SOIDV_LL_CNIVX74_P4	1.325e-05	1.000e-20
C8T28SOIDV_LL_CNIVX74_P10	2.380e-06	1.000e-20
C8T28SOIDV_LL_CNIVX74_P16	9.804e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_-CNIVX2_P0	C8T28SOI_LL_-CNIVX2_P4	C8T28SOI_LL_-CNIVX2_P10	C8T28SOI_LL_-CNIVX2_P16
A to Z	4.175e-04	3.586e-04	3.208e-04	3.076e-04
	C8T28SOI_LL_-CNIVX4_P0	C8T28SOI_LL_-CNIVX4_P4	C8T28SOI_LL_-CNIVX4_P10	C8T28SOI_LL_-CNIVX4_P16
A to Z	6.232e-04	5.134e-04	4.398e-04	4.064e-04
	C8T28SOI_LL_-CNIVX9_P0	C8T28SOI_LL_-CNIVX9_P4	C8T28SOI_LL_-CNIVX9_P10	C8T28SOI_LL_-CNIVX9_P16
A to Z	1.225e-03	9.554e-04	7.789e-04	7.000e-04
	C8T28SOI_LL_-CNIVX14_P0	C8T28SOI_LL_-CNIVX14_P4	C8T28SOI_LL_-CNIVX14_P10	C8T28SOI_LL_-CNIVX14_P16
A to Z	1.884e-03	1.483e-03	1.225e-03	1.112e-03
	C8T28SOI_LL_-CNIVX18_P0	C8T28SOI_LL_-CNIVX18_P4	C8T28SOI_LL_-CNIVX18_P10	C8T28SOI_LL_-CNIVX18_P16
A to Z	2.516e-03	1.998e-03	1.673e-03	1.533e-03
	C8T28SOI_LL_-CNIVX22_P0	C8T28SOI_LL_-CNIVX22_P4	C8T28SOI_LL_-CNIVX22_P10	C8T28SOI_LL_-CNIVX22_P16
A to Z	2.967e-03	2.343e-03	1.916e-03	1.732e-03
	C8T28SOI_LL_-CNIVX27_P0	C8T28SOI_LL_-CNIVX27_P4	C8T28SOI_LL_-CNIVX27_P10	C8T28SOI_LL_-CNIVX27_P16
A to Z	3.650e-03	2.914e-03	2.414e-03	2.196e-03
	C8T28SOI_LL_-CNIVX32_P0	C8T28SOI_LL_-CNIVX32_P4	C8T28SOI_LL_-CNIVX32_P10	C8T28SOI_LL_-CNIVX32_P16
A to Z	4.286e-03	3.373e-03	2.759e-03	2.493e-03
	C8T28SOI_LL_-CNIVX37_P0	C8T28SOI_LL_-CNIVX37_P4	C8T28SOI_LL_-CNIVX37_P10	C8T28SOI_LL_-CNIVX37_P16
A to Z	4.910e-03	3.894e-03	3.214e-03	2.918e-03
	C8T28SOI_LL_-CNIVX74_P0	C8T28SOI_LL_-CNIVX74_P4	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A to Z	1.046e-02	8.355e-03	6.734e-03	6.018e-03
	C8T28SOIDV_LL_-CNIVX18_P0	C8T28SOIDV_LL_-CNIVX18_P4	C8T28SOIDV_LL_-CNIVX18_P10	C8T28SOIDV_LL_-CNIVX18_P16
A to Z	2.434e-03	1.889e-03	1.537e-03	1.378e-03
	C8T28SOIDV_LL_-CNIVX28_P0	C8T28SOIDV_LL_-CNIVX28_P4	C8T28SOIDV_LL_-CNIVX28_P10	C8T28SOIDV_LL_-CNIVX28_P16
A to Z	3.708e-03	2.934e-03	2.415e-03	2.191e-03
	C8T28SOIDV_LL_-CNIVX37_P0	C8T28SOIDV_LL_-CNIVX37_P4	C8T28SOIDV_LL_-CNIVX37_P10	C8T28SOIDV_LL_-CNIVX37_P16
A to Z	4.755e-03	3.715e-03	2.997e-03	2.660e-03
	C8T28SOIDV_LL_-CNIVX55_P0	C8T28SOIDV_LL_-CNIVX55_P4	C8T28SOIDV_LL_-CNIVX55_P10	C8T28SOIDV_LL_-CNIVX55_P16
A to Z	7.084e-03	5.539e-03	4.456e-03	3.986e-03
	C8T28SOIDV_LL_-CNIVX74_P0	C8T28SOIDV_LL_-CNIVX74_P4	C8T28SOIDV_LL_-CNIVX74_P10	C8T28SOIDV_LL_-CNIVX74_P16
A to Z	9.573e-03	7.479e-03	6.015e-03	5.389e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

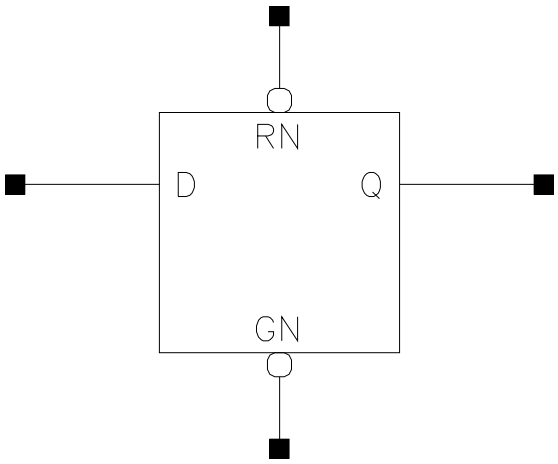
Pin Cycle (vdds)	C8T28SOI_LL_-CNIVX2_P0	C8T28SOI_LL_-CNIVX2_P4	C8T28SOI_LL_-CNIVX2_P10	C8T28SOI_LL_-CNIVX2_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX4_P0	C8T28SOI_LL_-CNIVX4_P4	C8T28SOI_LL_-CNIVX4_P10	C8T28SOI_LL_-CNIVX4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX9_P0	C8T28SOI_LL_-CNIVX9_P4	C8T28SOI_LL_-CNIVX9_P10	C8T28SOI_LL_-CNIVX9_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX14_P0	C8T28SOI_LL_-CNIVX14_P4	C8T28SOI_LL_-CNIVX14_P10	C8T28SOI_LL_-CNIVX14_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX18_P0	C8T28SOI_LL_-CNIVX18_P4	C8T28SOI_LL_-CNIVX18_P10	C8T28SOI_LL_-CNIVX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX22_P0	C8T28SOI_LL_-CNIVX22_P4	C8T28SOI_LL_-CNIVX22_P10	C8T28SOI_LL_-CNIVX22_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX27_P0	C8T28SOI_LL_-CNIVX27_P4	C8T28SOI_LL_-CNIVX27_P10	C8T28SOI_LL_-CNIVX27_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX32_P0	C8T28SOI_LL_-CNIVX32_P4	C8T28SOI_LL_-CNIVX32_P10	C8T28SOI_LL_-CNIVX32_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX37_P0	C8T28SOI_LL_-CNIVX37_P4	C8T28SOI_LL_-CNIVX37_P10	C8T28SOI_LL_-CNIVX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-CNIVX74_P0	C8T28SOI_LL_-CNIVX74_P4	C8T28SOI_LL_-CNIVX74_P10	C8T28SOI_LL_-CNIVX74_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX18_P0	C8T28SOIDV_LL_-CNIVX18_P4	C8T28SOIDV_LL_-CNIVX18_P10	C8T28SOIDV_LL_-CNIVX18_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX28_P0	C8T28SOIDV_LL_-CNIVX28_P4	C8T28SOIDV_LL_-CNIVX28_P10	C8T28SOIDV_LL_-CNIVX28_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX37_P0	C8T28SOIDV_LL_-CNIVX37_P4	C8T28SOIDV_LL_-CNIVX37_P10	C8T28SOIDV_LL_-CNIVX37_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX55_P0	C8T28SOIDV_LL_-CNIVX55_P4	C8T28SOIDV_LL_-CNIVX55_P10	C8T28SOIDV_LL_-CNIVX55_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOIDV_LL_-CNIVX74_P0	C8T28SOIDV_LL_-CNIVX74_P4	C8T28SOIDV_LL_-CNIVX74_P10	C8T28SOIDV_LL_-CNIVX74_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNLDLRQ

Cell Description

Active Low transparent Latch; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	1.600	1.360	2.1760
X19_P4	1.600	1.360	2.1760
X19_P10	1.600	1.360	2.1760
X19_P16	1.600	1.360	2.1760

Truth Table

IQ	Q
IQ	IQ

D	GN	RN	IQ	IQ
-	-	0	-	0
D	0	1	-	D
-	1	1	IQ	IQ

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
D	0.0010	0.0011	0.0011	0.0012
GN	0.0013	0.0013	0.0014	0.0015
RN	0.0005	0.0005	0.0005	0.0005

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	X19_P4	X19_P0	X19_P4

D to Q ↓	0.0381	0.0434	0.7228	0.7740
D to Q ↑	0.0383	0.0429	0.9805	1.0740
GN to Q ↓	0.0342	0.0390	0.7232	0.7746
GN to Q ↑	0.0419	0.0470	0.9827	1.0768
RN to Q ↓	0.0519	0.0591	0.7510	0.8076
RN to Q ↑	0.0431	0.0480	0.9807	1.0748
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
D to Q ↓	0.0514	0.0591	0.8466	0.9135
D to Q ↑	0.0498	0.0564	1.2086	1.3336
GN to Q ↓	0.0458	0.0523	0.8477	0.9143
GN to Q ↑	0.0547	0.0619	1.2119	1.3366
RN to Q ↓	0.0698	0.0799	0.8894	0.9647
RN to Q ↑	0.0553	0.0622	1.2101	1.3352

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X19_P0	X19_P4	X19_P10	X19_P16
D ↓	hold_rising to GN	-0.0052	-0.0101	-0.0145	-0.0220
D ↑	hold_rising to GN	-0.0039	-0.0066	-0.0110	-0.0159
D ↓	setup_rising to GN	0.0423	0.0472	0.0569	0.0667
D ↑	setup_rising to GN	0.0385	0.0460	0.0541	0.0611
GN ↓	min_pulse_width to GN	0.0470	0.0513	0.0603	0.0681
RN ↓	min_pulse_width to RN	0.0615	0.0686	0.0806	0.0925
RN ↑	recovery_rising to GN	0.0461	0.0536	0.0578	0.0681
RN ↑	removal_rising to GN	-0.0261	-0.0337	-0.0387	-0.0435

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X19_P0	3.366e-05	1.000e-20
X19_P4	6.048e-06	1.000e-20
X19_P10	1.129e-06	1.000e-20
X19_P16	5.059e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
D (output stable)	9.580e-05	5.895e-05	6.440e-05	7.333e-05
GN (output stable)	1.276e-03	1.175e-03	1.098e-03	1.091e-03
RN (output stable)	5.040e-05	3.632e-05	3.021e-05	2.566e-05
D to Q	8.400e-03	7.874e-03	7.685e-03	7.759e-03
GN to Q	1.028e-02	9.728e-03	9.548e-03	9.653e-03
RN to Q	6.680e-03	6.248e-03	6.044e-03	6.045e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

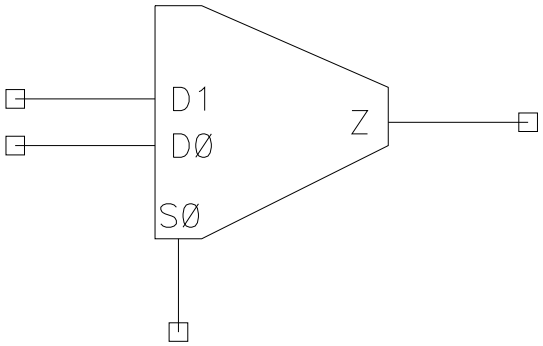
GN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
GN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00
RN to Q	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX21

Cell Description

2:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	1.632	1.3056
X9_P4	0.800	1.632	1.3056
X9_P10	0.800	1.632	1.3056
X9_P16	0.800	1.632	1.3056
X15_P0	0.800	2.312	1.8496
X15_P4	0.800	2.312	1.8496
X15_P10	0.800	2.312	1.8496
X15_P16	0.800	2.312	1.8496
X27_P0	0.800	2.584	2.0672
X27_P4	0.800	2.584	2.0672
X27_P10	0.800	2.584	2.0672
X27_P16	0.800	2.584	2.0672

Truth Table

D0	D1	S0	Z
D0	-	0	D0
-	D1	1	D1

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
D0	0.0006	0.0007	0.0007	0.0007
D1	0.0007	0.0007	0.0007	0.0008
S0	0.0011	0.0012	0.0013	0.0013
	X15_P0	X15_P4	X15_P10	X15_P16
D0	0.0010	0.0011	0.0011	0.0012
D1	0.0010	0.0011	0.0011	0.0012
S0	0.0011	0.0012	0.0013	0.0013
	X27_P0	X27_P4	X27_P10	X27_P16

D0	0.0011	0.0011	0.0012	0.0013
D1	0.0011	0.0011	0.0012	0.0012
S0	0.0014	0.0014	0.0015	0.0016

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
D0 to Z ↓	0.0278	0.0314	1.4245	1.5184
D0 to Z ↑	0.0225	0.0252	2.0732	2.2598
D1 to Z ↓	0.0277	0.0313	1.4228	1.5155
D1 to Z ↑	0.0218	0.0245	2.0716	2.2582
S0 to Z ↓	0.0236	0.0266	1.4169	1.5092
S0 to Z ↑	0.0224	0.0252	2.0696	2.2555
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
D0 to Z ↓	0.0365	0.0411	1.6486	1.7690
D0 to Z ↑	0.0291	0.0327	2.5288	2.7780
D1 to Z ↓	0.0365	0.0412	1.6465	1.7658
D1 to Z ↑	0.0283	0.0316	2.5233	2.7754
S0 to Z ↓	0.0310	0.0350	1.6419	1.7604
S0 to Z ↑	0.0293	0.0329	2.5261	2.7761
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
D0 to Z ↓	0.0259	0.0293	0.9550	1.0177
D0 to Z ↑	0.0252	0.0281	1.1148	1.2175
D1 to Z ↓	0.0276	0.0312	0.9559	1.0196
D1 to Z ↑	0.0240	0.0268	1.1131	1.2144
S0 to Z ↓	0.0287	0.0323	0.9521	1.0158
S0 to Z ↑	0.0282	0.0318	1.1127	1.2159
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
D0 to Z ↓	0.0343	0.0388	1.1062	1.1866
D0 to Z ↑	0.0325	0.0365	1.3637	1.5009
D1 to Z ↓	0.0366	0.0416	1.1085	1.1900
D1 to Z ↑	0.0309	0.0346	1.3628	1.4960
S0 to Z ↓	0.0376	0.0424	1.1050	1.1861
S0 to Z ↑	0.0369	0.0414	1.3620	1.4980
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0291	0.0329	0.5318	0.5678
D0 to Z ↑	0.0268	0.0299	0.6568	0.7163
D1 to Z ↓	0.0305	0.0346	0.5327	0.5697
D1 to Z ↑	0.0270	0.0301	0.6578	0.7172
S0 to Z ↓	0.0311	0.0350	0.5314	0.5679
S0 to Z ↑	0.0287	0.0322	0.6562	0.7162
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.0384	0.0436	0.6192	0.6653
D0 to Z ↑	0.0346	0.0389	0.8020	0.8802
D1 to Z ↓	0.0406	0.0461	0.6213	0.6681
D1 to Z ↑	0.0347	0.0388	0.8022	0.8816
S0 to Z ↓	0.0407	0.0460	0.6195	0.6662
S0 to Z ↑	0.0374	0.0421	0.8020	0.8806

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds

X9_P0	2.566e-05	1.000e-20
X9_P4	4.840e-06	1.000e-20
X9_P10	9.279e-07	1.000e-20
X9_P16	3.995e-07	1.000e-20
X15_P0	3.554e-05	1.000e-20
X15_P4	6.566e-06	1.000e-20
X15_P10	1.242e-06	1.000e-20
X15_P16	5.370e-07	1.000e-20
X27_P0	5.078e-05	1.000e-20
X27_P4	9.520e-06	1.000e-20
X27_P10	1.792e-06	1.000e-20
X27_P16	7.627e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	1.115e-03	1.016e-03	9.518e-04	9.271e-04
D1 (output stable)	1.088e-03	9.887e-04	9.235e-04	8.981e-04
S0 (output stable)	1.255e-03	1.184e-03	1.157e-03	1.168e-03
D0 to Z	3.621e-03	3.472e-03	3.452e-03	3.514e-03
D1 to Z	3.518e-03	3.372e-03	3.359e-03	3.423e-03
S0 to Z	4.041e-03	3.859e-03	3.820e-03	3.879e-03
	X15_P0	X15_P4	X15_P10	X15_P16
D0 (output stable)	1.480e-03	1.293e-03	1.173e-03	1.122e-03
D1 (output stable)	1.561e-03	1.391e-03	1.281e-03	1.236e-03
S0 (output stable)	1.237e-03	1.210e-03	1.222e-03	1.251e-03
D0 to Z	6.142e-03	5.836e-03	5.770e-03	5.851e-03
D1 to Z	6.044e-03	5.741e-03	5.676e-03	5.755e-03
S0 to Z	6.579e-03	6.298e-03	6.259e-03	6.355e-03
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	1.641e-03	1.429e-03	1.292e-03	1.230e-03
D1 (output stable)	1.668e-03	1.477e-03	1.351e-03	1.298e-03
S0 (output stable)	1.438e-03	1.396e-03	1.399e-03	1.429e-03
D0 to Z	9.291e-03	8.731e-03	8.533e-03	8.601e-03
D1 to Z	9.283e-03	8.710e-03	8.489e-03	8.547e-03
S0 to Z	9.851e-03	9.310e-03	9.125e-03	9.209e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

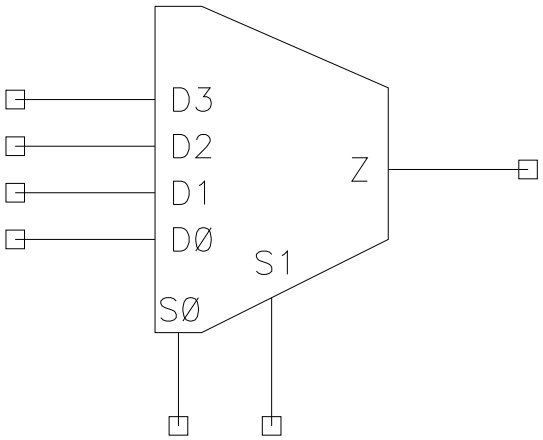
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNMUX41

Cell Description

4:1 non-inverting Multiplexer for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	1.600	1.768	2.8288
X9_P4	1.600	1.768	2.8288
X9_P10	1.600	1.768	2.8288
X9_P16	1.600	1.768	2.8288
X27_P0	1.600	2.584	4.1344
X27_P4	1.600	2.584	4.1344
X27_P10	1.600	2.584	4.1344
X27_P16	1.600	2.584	4.1344

Truth Table

D0	D1	D2	D3	S0	S1	Z
1	1	1	1	-	-	1
D0	-	-	-	0	0	D0
-	D1	-	-	1	0	D1
-	-	D2	-	0	1	D2
-	-	-	D3	1	1	D3

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
D0	0.0006	0.0006	0.0007	0.0007
D1	0.0005	0.0005	0.0005	0.0005
D2	0.0006	0.0006	0.0007	0.0007
D3	0.0005	0.0005	0.0005	0.0006
S0	0.0016	0.0016	0.0017	0.0018
S1	0.0008	0.0009	0.0009	0.0010

	X27_P0	X27_P4	X27_P10	X27_P16
D0	0.0009	0.0009	0.0010	0.0010
D1	0.0008	0.0008	0.0009	0.0009
D2	0.0009	0.0010	0.0010	0.0010
D3	0.0009	0.0009	0.0010	0.0010
S0	0.0023	0.0024	0.0026	0.0027
S1	0.0017	0.0017	0.0019	0.0020

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
D0 to Z ↓	0.0491	0.0558	1.4875	1.5902
D0 to Z ↑	0.0409	0.0456	2.0953	2.2885
D1 to Z ↓	0.0489	0.0556	1.4893	1.5917
D1 to Z ↑	0.0407	0.0454	2.0925	2.2895
D2 to Z ↓	0.0496	0.0562	1.4908	1.5944
D2 to Z ↑	0.0392	0.0439	2.0879	2.2821
D3 to Z ↓	0.0484	0.0549	1.4904	1.5928
D3 to Z ↑	0.0389	0.0435	2.0868	2.2800
S0 to Z ↓	0.0530	0.0606	1.4872	1.5899
S0 to Z ↑	0.0483	0.0546	2.0930	2.2902
S1 to Z ↓	0.0369	0.0420	1.4880	1.5905
S1 to Z ↑	0.0381	0.0426	2.0887	2.2836
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
D0 to Z ↓	0.0656	0.0749	1.7375	1.8730
D0 to Z ↑	0.0526	0.0593	2.5699	2.8274
D1 to Z ↓	0.0655	0.0748	1.7396	1.8752
D1 to Z ↑	0.0525	0.0591	2.5681	2.8261
D2 to Z ↓	0.0662	0.0758	1.7438	1.8800
D2 to Z ↑	0.0508	0.0573	2.5602	2.8195
D3 to Z ↓	0.0648	0.0742	1.7424	1.8791
D3 to Z ↑	0.0504	0.0568	2.5577	2.8177
S0 to Z ↓	0.0717	0.0824	1.7384	1.8740
S0 to Z ↑	0.0638	0.0724	2.5693	2.8277
S1 to Z ↓	0.0494	0.0558	1.7396	1.8759
S1 to Z ↑	0.0481	0.0525	2.5640	2.8215
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
D0 to Z ↓	0.0525	0.0595	0.5022	0.5386
D0 to Z ↑	0.0472	0.0527	0.7655	0.8383
D1 to Z ↓	0.0565	0.0640	0.5074	0.5444
D1 to Z ↑	0.0470	0.0525	0.7660	0.8379
D2 to Z ↓	0.0560	0.0634	0.5062	0.5431
D2 to Z ↑	0.0475	0.0530	0.7660	0.8388
D3 to Z ↓	0.0538	0.0610	0.5037	0.5404
D3 to Z ↑	0.0469	0.0524	0.7660	0.8385
S0 to Z ↓	0.0622	0.0706	0.5037	0.5403
S0 to Z ↑	0.0570	0.0642	0.7664	0.8387
S1 to Z ↓	0.0435	0.0493	0.5046	0.5413
S1 to Z ↑	0.0463	0.0516	0.7657	0.8378
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
D0 to Z ↓	0.0701	0.0803	0.5912	0.6394
D0 to Z ↑	0.0612	0.0693	0.9414	1.0363

D1 to Z ↓	0.0755	0.0864	0.5983	0.6481
D1 to Z ↑	0.0610	0.0690	0.9412	1.0363
D2 to Z ↓	0.0748	0.0856	0.5963	0.6458
D2 to Z ↑	0.0615	0.0695	0.9419	1.0370
D3 to Z ↓	0.0720	0.0825	0.5932	0.6420
D3 to Z ↑	0.0608	0.0687	0.9409	1.0375
S0 to Z ↓	0.0833	0.0955	0.5932	0.6417
S0 to Z ↑	0.0751	0.0855	0.9422	1.0375
S1 to Z ↓	0.0581	0.0655	0.5945	0.6437
S1 to Z ↑	0.0593	0.0659	0.9416	1.0370

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X9_P0	1.810e-05	1.000e-20
X9_P4	3.603e-06	1.000e-20
X9_P10	8.022e-07	1.000e-20
X9_P16	4.217e-07	1.000e-20
X27_P0	4.391e-05	1.000e-20
X27_P4	8.530e-06	1.000e-20
X27_P10	1.817e-06	1.000e-20
X27_P16	9.215e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	5.172e-05	4.006e-05	8.951e-05	1.005e-04
D1 (output stable)	7.046e-05	6.335e-05	1.009e-04	1.161e-04
D2 (output stable)	7.129e-05	4.917e-05	3.116e-05	3.988e-05
D3 (output stable)	7.110e-05	5.758e-05	7.301e-05	9.196e-05
S0 (output stable)	1.281e-03	1.287e-03	1.453e-03	1.616e-03
S1 (output stable)	1.385e-03	1.212e-03	1.074e-03	1.030e-03
D0 to Z	4.307e-03	4.109e-03	4.049e-03	4.100e-03
D1 to Z	4.291e-03	4.095e-03	4.050e-03	4.101e-03
D2 to Z	4.214e-03	4.010e-03	3.960e-03	4.011e-03
D3 to Z	4.191e-03	3.985e-03	3.938e-03	3.987e-03
S0 to Z	5.711e-03	5.565e-03	5.671e-03	5.854e-03
S1 to Z	4.622e-03	4.199e-03	3.978e-03	3.908e-03
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	1.028e-04	6.484e-05	1.011e-04	1.161e-04
D1 (output stable)	8.273e-05	6.650e-05	1.036e-04	1.242e-04
D2 (output stable)	1.076e-04	6.971e-05	4.472e-05	7.163e-05
D3 (output stable)	1.123e-04	8.497e-05	1.111e-04	1.426e-04
S0 (output stable)	2.391e-03	2.418e-03	2.654e-03	2.905e-03
S1 (output stable)	2.318e-03	2.091e-03	1.898e-03	1.830e-03
D0 to Z	1.198e-02	1.112e-02	1.072e-02	1.072e-02
D1 to Z	1.224e-02	1.135e-02	1.093e-02	1.092e-02
D2 to Z	1.229e-02	1.140e-02	1.099e-02	1.099e-02
D3 to Z	1.209e-02	1.123e-02	1.083e-02	1.084e-02
S0 to Z	1.473e-02	1.396e-02	1.382e-02	1.403e-02
S1 to Z	1.274e-02	1.144e-02	1.072e-02	1.053e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

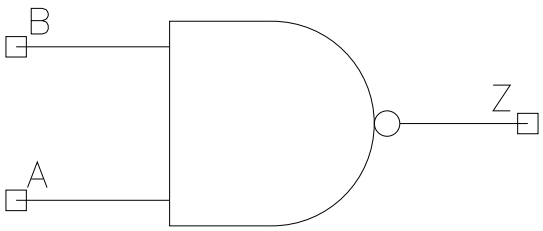
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
D0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D2 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D3 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S0 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S1 to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2

Cell Description

2 input NAND for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	0.800	0.952	0.7616
X8_P4	0.800	0.952	0.7616
X8_P10	0.800	0.952	0.7616
X8_P16	0.800	0.952	0.7616
X15_P0	0.800	1.224	0.9792
X15_P4	0.800	1.224	0.9792
X15_P10	0.800	1.224	0.9792
X15_P16	0.800	1.224	0.9792
X27_P0	0.800	1.632	1.3056
X27_P4	0.800	1.632	1.3056
X27_P10	0.800	1.632	1.3056
X27_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
1	1	0
0	-	1
-	0	1

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0011	0.0012	0.0013	0.0013
B	0.0010	0.0011	0.0011	0.0012
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0005	0.0005	0.0006	0.0006
B	0.0005	0.0005	0.0005	0.0005
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0006	0.0006	0.0006	0.0007
B	0.0006	0.0007	0.0007	0.0008

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0060	0.0073	1.8798	2.0021
A to Z ↑	0.0124	0.0139	2.2780	2.4851
B to Z ↓	0.0060	0.0070	1.9123	2.0392
B to Z ↑	0.0100	0.0112	2.2937	2.5036
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0090	0.0102	2.1763	2.3319
A to Z ↑	0.0161	0.0179	2.7747	3.0410
B to Z ↓	0.0083	0.0094	2.2175	2.3769
B to Z ↑	0.0127	0.0140	2.7977	3.0665
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0289	0.0330	0.9300	0.9902
A to Z ↑	0.0310	0.0352	1.0757	1.1761
B to Z ↓	0.0306	0.0347	0.9288	0.9904
B to Z ↑	0.0314	0.0357	1.0779	1.1757
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0387	0.0443	1.0753	1.1508
A to Z ↑	0.0411	0.0466	1.3157	1.4472
B to Z ↓	0.0407	0.0463	1.0752	1.1502
B to Z ↑	0.0417	0.0472	1.3164	1.4481
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0293	0.0331	0.4872	0.5193
A to Z ↑	0.0304	0.0345	0.6407	0.6972
B to Z ↓	0.0299	0.0339	0.4869	0.5192
B to Z ↑	0.0296	0.0336	0.6406	0.6971
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0387	0.0441	0.5644	0.6054
A to Z ↑	0.0403	0.0457	0.7800	0.8569
B to Z ↓	0.0396	0.0451	0.5646	0.6055
B to Z ↑	0.0391	0.0443	0.7805	0.8569

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	7.898e-06	1.000e-20
X8_P4	1.575e-06	1.000e-20
X8_P10	3.477e-07	1.000e-20
X8_P16	1.780e-07	1.000e-20
X15_P0	1.857e-05	1.000e-20
X15_P4	3.550e-06	1.000e-20
X15_P10	7.105e-07	1.000e-20
X15_P16	3.238e-07	1.000e-20
X27_P0	3.332e-05	1.000e-20
X27_P4	6.442e-06	1.000e-20
X27_P10	1.254e-06	1.000e-20
X27_P16	5.403e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	8.410e-05	7.161e-05	5.728e-05	4.766e-05
B (output stable)	2.501e-04	2.692e-04	2.744e-04	2.694e-04
A to Z	1.835e-03	1.699e-03	1.645e-03	1.644e-03

B to Z	1.445e-03	1.239e-03	1.104e-03	1.046e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.396e-05	1.242e-05	1.066e-05	9.370e-06
B (output stable)	2.990e-05	3.435e-05	3.586e-05	3.464e-05
A to Z	5.203e-03	5.175e-03	5.255e-03	5.447e-03
B to Z	5.134e-03	5.088e-03	5.147e-03	5.325e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.932e-05	1.728e-05	1.481e-05	1.316e-05
B (output stable)	3.625e-05	4.360e-05	4.591e-05	4.505e-05
A to Z	7.975e-03	7.844e-03	7.948e-03	8.191e-03
B to Z	7.901e-03	7.748e-03	7.823e-03	8.047e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

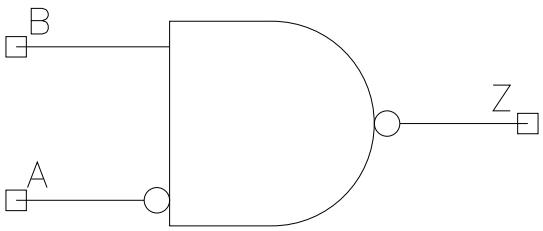
Pin Cycle (vdds)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNAND2A

Cell Description

2 input NAND with A input inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	0.952	0.7616
X9_P4	0.800	0.952	0.7616
X9_P10	0.800	0.952	0.7616
X9_P16	0.800	0.952	0.7616
X15_P0	0.800	1.360	1.0880
X15_P4	0.800	1.360	1.0880
X15_P10	0.800	1.360	1.0880
X15_P16	0.800	1.360	1.0880
X27_P0	0.800	2.856	2.2848
X27_P4	0.800	2.856	2.2848
X27_P10	0.800	2.856	2.2848
X27_P16	0.800	2.856	2.2848

Truth Table

A	B	Z
0	1	0
-	0	1
1	-	1

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
A	0.0005	0.0006	0.0006	0.0006
B	0.0006	0.0006	0.0006	0.0007
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0005	0.0005	0.0006	0.0006
B	0.0005	0.0006	0.0006	0.0006
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0017	0.0017	0.0018	0.0020
B	0.0035	0.0036	0.0038	0.0040

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
A to Z ↓	0.0234	0.0267	1.4031	1.4963
A to Z ↑	0.0185	0.0209	1.9590	2.1307
B to Z ↓	0.0248	0.0282	1.4000	1.4921
B to Z ↑	0.0254	0.0286	1.9563	2.1287
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
A to Z ↓	0.0314	0.0359	1.6241	1.7430
A to Z ↑	0.0243	0.0272	2.3836	2.6157
B to Z ↓	0.0335	0.0385	1.6220	1.7401
B to Z ↑	0.0332	0.0374	2.3804	2.6113
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0385	0.0440	0.9785	1.0420
A to Z ↑	0.0337	0.0385	1.0677	1.1641
B to Z ↓	0.0295	0.0336	0.9793	1.0411
B to Z ↑	0.0303	0.0344	1.0682	1.1644
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0520	0.0596	1.1312	1.2109
A to Z ↑	0.0455	0.0521	1.2998	1.4266
B to Z ↓	0.0396	0.0453	1.1310	1.2115
B to Z ↑	0.0401	0.0455	1.3005	1.4256
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0207	0.0235	0.6440	0.6872
A to Z ↑	0.0200	0.0226	0.6363	0.6970
B to Z ↓	0.0072	0.0080	0.6667	0.7111
B to Z ↑	0.0078	0.0089	0.5429	0.5890
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0274	0.0308	0.7494	0.8066
A to Z ↑	0.0263	0.0296	0.7824	0.8603
B to Z ↓	0.0091	0.0101	0.7737	0.8294
B to Z ↑	0.0104	0.0115	0.6551	0.7161

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X9_P0	1.522e-05	1.000e-20
X9_P4	3.013e-06	1.000e-20
X9_P10	6.058e-07	1.000e-20
X9_P16	2.666e-07	1.000e-20
X15_P0	1.851e-05	1.000e-20
X15_P4	3.657e-06	1.000e-20
X15_P10	7.596e-07	1.000e-20
X15_P16	3.522e-07	1.000e-20
X27_P0	4.093e-05	1.000e-20
X27_P4	7.715e-06	1.000e-20
X27_P10	1.559e-06	1.000e-20
X27_P16	7.464e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	2.989e-05	2.817e-05	2.812e-05	5.329e-05
B (output stable)	9.609e-04	8.636e-04	8.051e-04	7.923e-04
A to Z	2.719e-03	2.614e-03	2.615e-03	2.680e-03

B to Z	3.619e-03	3.516e-03	3.533e-03	3.630e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	7.939e-04	7.611e-04	7.619e-04	7.871e-04
B (output stable)	2.672e-05	3.297e-05	3.517e-05	3.433e-05
A to Z	5.779e-03	5.764e-03	5.921e-03	6.172e-03
B to Z	4.948e-03	4.882e-03	4.978e-03	5.182e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	4.592e-03	4.519e-03	4.816e-03	5.105e-03
B (output stable)	7.167e-04	7.754e-04	7.977e-04	7.702e-04
A to Z	9.946e-03	9.882e-03	1.016e-02	1.045e-02
B to Z	4.956e-03	4.099e-03	3.529e-03	3.269e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

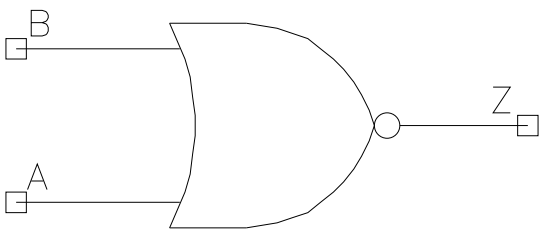
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2

Cell Description

2 input NOR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X8_P0	0.800	0.952	0.7616
X8_P4	0.800	0.952	0.7616
X8_P10	0.800	0.952	0.7616
X8_P16	0.800	0.952	0.7616
X15_P0	0.800	1.360	1.0880
X15_P4	0.800	1.360	1.0880
X15_P10	0.800	1.360	1.0880
X15_P16	0.800	1.360	1.0880
X27_P0	0.800	1.632	1.3056
X27_P4	0.800	1.632	1.3056
X27_P10	0.800	1.632	1.3056
X27_P16	0.800	1.632	1.3056

Truth Table

A	B	Z
-	1	0
1	-	0
0	0	1

Pin Capacitance

Pin	X8_P0	X8_P4	X8_P10	X8_P16
A	0.0013	0.0013	0.0014	0.0015
B	0.0012	0.0012	0.0013	0.0013
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0005	0.0005	0.0005	0.0006
B	0.0006	0.0006	0.0006	0.0006
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0005	0.0006	0.0006	0.0006
B	0.0006	0.0006	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X8_P0	**X8_P4**	**X8_P0**	**X8_P4**
A to Z ↓	0.0084	0.0097	1.6019	1.6969
A to Z ↑	0.0105	0.0124	2.7870	3.0136
B to Z ↓	0.0060	0.0070	1.6076	1.7023
B to Z ↑	0.0096	0.0107	2.8080	3.0420
	X8_P10	**X8_P16**	**X8_P10**	**X8_P16**
A to Z ↓	0.0113	0.0127	1.8283	1.9434
A to Z ↑	0.0149	0.0170	3.3486	3.6715
B to Z ↓	0.0083	0.0093	1.8366	1.9531
B to Z ↑	0.0123	0.0137	3.3859	3.7114
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0283	0.0323	0.9246	0.9851
A to Z ↑	0.0308	0.0352	1.0669	1.1654
B to Z ↓	0.0273	0.0312	0.9245	0.9848
B to Z ↑	0.0319	0.0362	1.0667	1.1638
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0382	0.0435	1.0694	1.1428
A to Z ↑	0.0416	0.0475	1.3064	1.4366
B to Z ↓	0.0369	0.0421	1.0691	1.1440
B to Z ↑	0.0424	0.0482	1.3057	1.4364
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0300	0.0345	0.5196	0.5549
A to Z ↑	0.0311	0.0356	0.6304	0.6879
B to Z ↓	0.0301	0.0346	0.5196	0.5544
B to Z ↑	0.0319	0.0364	0.6296	0.6877
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0406	0.0467	0.6034	0.6477
A to Z ↑	0.0420	0.0480	0.7694	0.8452
B to Z ↓	0.0407	0.0467	0.6035	0.6480
B to Z ↑	0.0427	0.0486	0.7684	0.8449

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X8_P0	1.119e-05	1.000e-20
X8_P4	2.103e-06	1.000e-20
X8_P10	4.131e-07	1.000e-20
X8_P16	1.921e-07	1.000e-20
X15_P0	2.641e-05	1.000e-20
X15_P4	4.796e-06	1.000e-20
X15_P10	8.921e-07	1.000e-20
X15_P16	3.865e-07	1.000e-20
X27_P0	4.560e-05	1.000e-20
X27_P4	8.035e-06	1.000e-20
X27_P10	1.418e-06	1.000e-20
X27_P16	5.904e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	1.321e-04	1.269e-04	1.259e-04	1.256e-04
B (output stable)	2.434e-04	1.157e-04	6.400e-05	5.221e-05
A to Z	2.047e-03	1.936e-03	1.925e-03	1.957e-03

B to Z	1.521e-03	1.288e-03	1.134e-03	1.071e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	2.528e-05	2.422e-05	2.416e-05	2.415e-05
B (output stable)	3.584e-05	1.841e-05	6.907e-06	4.604e-06
A to Z	5.253e-03	5.205e-03	5.345e-03	5.527e-03
B to Z	5.154e-03	5.077e-03	5.183e-03	5.349e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	3.066e-05	2.922e-05	2.932e-05	2.938e-05
B (output stable)	4.532e-05	2.551e-05	9.112e-06	5.804e-06
A to Z	7.799e-03	7.722e-03	7.758e-03	8.040e-03
B to Z	7.674e-03	7.562e-03	7.561e-03	7.816e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

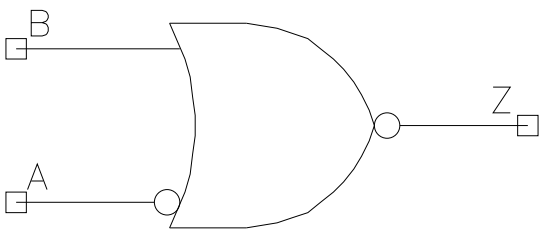
Pin Cycle (vdds)	X8_P0	X8_P4	X8_P10	X8_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNNOR2A

Cell Description

2 input NOR with A input Inverted for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	1.360	1.0880
X9_P4	0.800	1.360	1.0880
X9_P10	0.800	1.360	1.0880
X9_P16	0.800	1.360	1.0880
X15_P0	0.800	1.496	1.1968
X15_P4	0.800	1.496	1.1968
X15_P10	0.800	1.496	1.1968
X15_P16	0.800	1.496	1.1968
X27_P0	0.800	1.768	1.4144
X27_P4	0.800	1.768	1.4144
X27_P10	0.800	1.768	1.4144
X27_P16	0.800	1.768	1.4144

Truth Table

A	B	Z
0	-	0
-	1	0
1	0	1

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
A	0.0010	0.0010	0.0011	0.0011
B	0.0008	0.0008	0.0008	0.0009
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0006	0.0006	0.0007	0.0007
B	0.0007	0.0007	0.0007	0.0007
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0006	0.0007	0.0007	0.0008
B	0.0006	0.0006	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
A to Z ↓	0.0240	0.0270	1.3832	1.4700
A to Z ↑	0.0152	0.0175	2.0600	2.2440
B to Z ↓	0.0224	0.0256	1.3757	1.4633
B to Z ↑	0.0253	0.0285	2.0561	2.2424
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
A to Z ↓	0.0313	0.0352	1.5942	1.7031
A to Z ↑	0.0206	0.0233	2.5104	2.7566
B to Z ↓	0.0304	0.0347	1.5886	1.7007
B to Z ↑	0.0331	0.0371	2.5074	2.7549
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0370	0.0423	0.9255	0.9857
A to Z ↑	0.0352	0.0402	1.0692	1.1676
B to Z ↓	0.0275	0.0315	0.9248	0.9861
B to Z ↑	0.0330	0.0374	1.0695	1.1682
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0498	0.0569	1.0699	1.1455
A to Z ↑	0.0479	0.0549	1.3085	1.4376
B to Z ↓	0.0371	0.0423	1.0700	1.1451
B to Z ↑	0.0438	0.0498	1.3083	1.4385
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0373	0.0427	0.4986	0.5325
A to Z ↑	0.0363	0.0413	0.6340	0.6913
B to Z ↓	0.0308	0.0351	0.4988	0.5324
B to Z ↑	0.0326	0.0369	0.6340	0.6914
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0508	0.0587	0.5804	0.6231
A to Z ↑	0.0488	0.0562	0.7732	0.8489
B to Z ↓	0.0415	0.0478	0.5801	0.6232
B to Z ↑	0.0432	0.0494	0.7732	0.8479

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X9_P0	1.950e-05	1.000e-20
X9_P4	3.635e-06	1.000e-20
X9_P10	7.105e-07	1.000e-20
X9_P16	3.271e-07	1.000e-20
X15_P0	2.982e-05	1.000e-20
X15_P4	5.458e-06	1.000e-20
X15_P10	1.022e-06	1.000e-20
X15_P16	4.435e-07	1.000e-20
X27_P0	4.548e-05	1.000e-20
X27_P4	8.289e-06	1.000e-20
X27_P10	1.514e-06	1.000e-20
X27_P16	6.430e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	7.040e-05	5.710e-05	4.196e-05	3.396e-05
B (output stable)	1.341e-03	1.256e-03	1.105e-03	1.044e-03
A to Z	3.175e-03	3.097e-03	3.127e-03	3.203e-03

B to Z	4.016e-03	3.936e-03	4.000e-03	4.115e-03
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	1.018e-03	9.612e-04	9.531e-04	9.671e-04
B (output stable)	3.927e-05	3.436e-05	2.532e-05	8.483e-06
A to Z	6.329e-03	6.310e-03	6.444e-03	6.676e-03
B to Z	5.252e-03	5.198e-03	5.269e-03	5.455e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	1.049e-03	9.827e-04	9.684e-04	9.891e-04
B (output stable)	4.599e-05	4.025e-05	3.168e-05	1.173e-05
A to Z	9.077e-03	8.898e-03	9.035e-03	9.387e-03
B to Z	7.966e-03	7.728e-03	7.786e-03	8.073e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

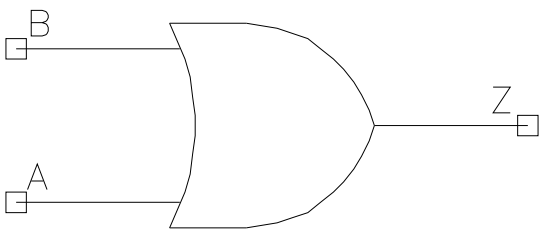
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR2

Cell Description

2 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	0.800	1.632	1.3056
X19_P4	0.800	1.632	1.3056
X19_P10	0.800	1.632	1.3056
X19_P16	0.800	1.632	1.3056
X37_P0	0.800	2.176	1.7408
X37_P4	0.800	2.176	1.7408
X37_P10	0.800	2.176	1.7408
X37_P16	0.800	2.176	1.7408

Truth Table

A	B	Z
0	0	0
-	1	1
1	-	1

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0015	0.0015	0.0016	0.0017
B	0.0015	0.0015	0.0016	0.0017
	X37_P0	X37_P4	X37_P10	X37_P16
A	0.0015	0.0016	0.0017	0.0017
B	0.0014	0.0015	0.0016	0.0016

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0216	0.0246	0.7142	0.7594
A to Z ↑	0.0184	0.0207	1.0003	1.0882
B to Z ↓	0.0217	0.0243	0.7146	0.7602
B to Z ↑	0.0165	0.0185	0.9985	1.0852
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**

A to Z ↓	0.0289	0.0331	0.8248	0.8837
A to Z ↑	0.0238	0.0267	1.2150	1.3329
B to Z ↓	0.0283	0.0320	0.8257	0.8847
B to Z ↑	0.0214	0.0240	1.2124	1.3311
	X37_P0	**X37_P4**	**X37_P0**	**X37_P4**
A to Z ↓	0.0270	0.0306	0.3667	0.3907
A to Z ↑	0.0229	0.0256	0.5228	0.5706
B to Z ↓	0.0278	0.0314	0.3665	0.3910
B to Z ↑	0.0211	0.0237	0.5215	0.5698
	X37_P10	**X37_P16**	**X37_P10**	**X37_P16**
A to Z ↓	0.0360	0.0414	0.4257	0.4572
A to Z ↑	0.0295	0.0331	0.6387	0.7012
B to Z ↓	0.0364	0.0417	0.4257	0.4577
B to Z ↑	0.0272	0.0307	0.6369	0.7010

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X19_P0	2.309e-05	1.000e-20
X19_P4	4.653e-06	1.000e-20
X19_P10	9.600e-07	1.000e-20
X19_P16	4.334e-07	1.000e-20
X37_P0	3.381e-05	1.000e-20
X37_P4	6.828e-06	1.000e-20
X37_P10	1.415e-06	1.000e-20
X37_P16	6.370e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	1.300e-04	1.244e-04	1.243e-04	1.231e-04
B (output stable)	2.392e-04	1.177e-04	6.667e-05	5.504e-05
A to Z	6.034e-03	5.823e-03	5.885e-03	6.076e-03
B to Z	5.506e-03	5.186e-03	5.125e-03	5.227e-03
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	1.308e-04	1.249e-04	1.251e-04	1.232e-04
B (output stable)	2.439e-04	1.212e-04	6.686e-05	5.524e-05
A to Z	1.057e-02	1.002e-02	9.873e-03	1.017e-02
B to Z	1.004e-02	9.397e-03	9.123e-03	9.348e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

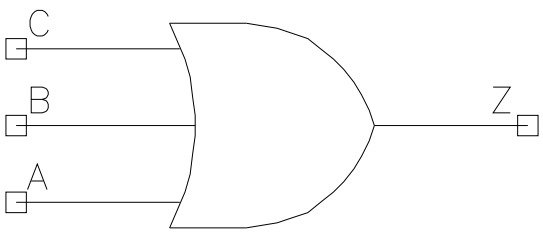
Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X37_P0	X37_P4	X37_P10	X37_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR3

Cell Description

3 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X14_P0	0.800	2.312	1.8496
X14_P4	0.800	2.312	1.8496
X14_P10	0.800	2.312	1.8496
X14_P16	0.800	2.312	1.8496
X19_P0	0.800	2.448	1.9584
X19_P4	0.800	2.448	1.9584
X19_P10	0.800	2.448	1.9584
X19_P16	0.800	2.448	1.9584
X27_P0	1.600	2.312	3.6992
X27_P4	1.600	2.312	3.6992
X27_P10	1.600	2.312	3.6992
X27_P16	1.600	2.312	3.6992

Truth Table

A	B	C	Z
0	0	0	0
-	1	-	1
1	-	-	1
-	-	1	1

Pin Capacitance

Pin	X14_P0	X14_P4	X14_P10	X14_P16
A	0.0004	0.0005	0.0005	0.0005
B	0.0005	0.0005	0.0005	0.0005
C	0.0005	0.0005	0.0005	0.0005
	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0004	0.0005	0.0005	0.0005
B	0.0005	0.0005	0.0005	0.0005
C	0.0005	0.0005	0.0005	0.0005
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0019	0.0020	0.0022	0.0023
B	0.0021	0.0022	0.0023	0.0024

C	0.0018	0.0019	0.0020	0.0021

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X14_P0	**X14_P4**	**X14_P0**	**X14_P4**
A to Z ↓	0.0460	0.0520	0.9279	0.9874
A to Z ↑	0.0418	0.0471	1.3031	1.4194
B to Z ↓	0.0472	0.0531	0.9283	0.9869
B to Z ↑	0.0410	0.0461	1.3028	1.4194
C to Z ↓	0.0395	0.0444	0.9278	0.9868
C to Z ↑	0.0367	0.0412	1.3034	1.4193
	X14_P10	**X14_P16**	**X14_P10**	**X14_P16**
A to Z ↓	0.0616	0.0703	1.0713	1.1487
A to Z ↑	0.0553	0.0626	1.5852	1.7425
B to Z ↓	0.0626	0.0712	1.0715	1.1485
B to Z ↑	0.0542	0.0614	1.5869	1.7429
C to Z ↓	0.0521	0.0589	1.0714	1.1477
C to Z ↑	0.0483	0.0546	1.5856	1.7435
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0480	0.0546	0.7010	0.7460
A to Z ↑	0.0434	0.0490	0.9760	1.0637
B to Z ↓	0.0492	0.0557	0.7004	0.7461
B to Z ↑	0.0425	0.0480	0.9765	1.0637
C to Z ↓	0.0415	0.0469	0.7004	0.7462
C to Z ↑	0.0382	0.0431	0.9756	1.0630
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0646	0.0737	0.8112	0.8683
A to Z ↑	0.0575	0.0649	1.1898	1.3049
B to Z ↓	0.0656	0.0746	0.8102	0.8685
B to Z ↑	0.0564	0.0637	1.1899	1.3056
C to Z ↓	0.0551	0.0622	0.8103	0.8688
C to Z ↑	0.0504	0.0568	1.1881	1.3064
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0264	0.0301	0.6079	0.6497
A to Z ↑	0.0244	0.0274	0.6285	0.6876
B to Z ↓	0.0260	0.0294	0.6081	0.6499
B to Z ↑	0.0230	0.0258	0.6278	0.6870
C to Z ↓	0.0202	0.0228	0.6028	0.6446
C to Z ↑	0.0187	0.0209	0.6313	0.6903
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0355	0.0405	0.7100	0.7645
A to Z ↑	0.0318	0.0357	0.7721	0.8484
B to Z ↓	0.0344	0.0389	0.7102	0.7648
B to Z ↑	0.0299	0.0336	0.7711	0.8484
C to Z ↓	0.0265	0.0296	0.7039	0.7572
C to Z ↑	0.0241	0.0269	0.7747	0.8514

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X14_P0	2.221e-05	1.000e-20
X14_P4	4.607e-06	1.000e-20

X14_P10	9.898e-07	1.000e-20
X14_P16	4.572e-07	1.000e-20
X19_P0	2.419e-05	1.000e-20
X19_P4	5.066e-06	1.000e-20
X19_P10	1.096e-06	1.000e-20
X19_P16	5.063e-07	1.000e-20
X27_P0	4.403e-05	1.000e-20
X27_P4	8.792e-06	1.000e-20
X27_P10	1.854e-06	1.000e-20
X27_P16	8.837e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	4.893e-04	4.948e-04	5.171e-04	5.457e-04
B (output stable)	4.659e-04	4.550e-04	4.640e-04	4.861e-04
C (output stable)	1.227e-03	1.197e-03	1.198e-03	1.205e-03
A to Z	6.940e-03	6.884e-03	7.146e-03	7.378e-03
B to Z	6.854e-03	6.778e-03	7.014e-03	7.234e-03
C to Z	6.715e-03	6.611e-03	6.820e-03	7.019e-03
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	4.895e-04	4.950e-04	5.172e-04	5.464e-04
B (output stable)	4.660e-04	4.551e-04	4.641e-04	4.863e-04
C (output stable)	1.225e-03	1.198e-03	1.200e-03	1.205e-03
A to Z	7.980e-03	7.930e-03	8.140e-03	8.350e-03
B to Z	7.894e-03	7.823e-03	8.012e-03	8.204e-03
C to Z	7.753e-03	7.656e-03	7.818e-03	7.989e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	2.243e-03	2.267e-03	2.437e-03	2.602e-03
B (output stable)	2.047e-03	1.906e-03	1.965e-03	2.057e-03
C (output stable)	4.470e-03	4.396e-03	4.353e-03	4.354e-03
A to Z	1.238e-02	1.238e-02	1.283e-02	1.333e-02
B to Z	1.148e-02	1.135e-02	1.163e-02	1.202e-02
C to Z	8.878e-03	8.576e-03	8.622e-03	8.769e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdds)	X14_P0	X14_P4	X14_P10	X14_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00

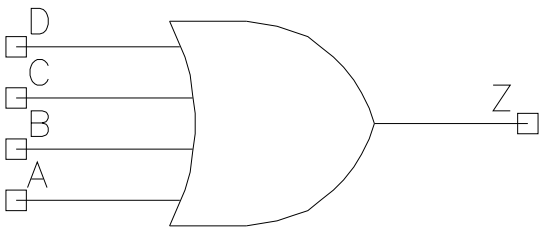
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNOR4

Cell Description

4 input OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X19_P0	0.800	2.448	1.9584
X19_P4	0.800	2.448	1.9584
X19_P10	0.800	2.448	1.9584
X19_P16	0.800	2.448	1.9584
X27_P0	1.600	2.584	4.1344
X27_P4	1.600	2.584	4.1344
X27_P10	1.600	2.584	4.1344
X27_P16	1.600	2.584	4.1344

Truth Table

A	B	C	D	Z
0	0	0	0	0
1	-	-	-	1
-	-	1	-	1
-	-	-	1	1
-	1	-	-	1

Pin Capacitance

Pin	X19_P0	X19_P4	X19_P10	X19_P16
A	0.0004	0.0005	0.0005	0.0005
B	0.0005	0.0005	0.0005	0.0005
C	0.0005	0.0006	0.0006	0.0006
D	0.0004	0.0005	0.0005	0.0005
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0020	0.0021	0.0023	0.0024
B	0.0019	0.0020	0.0021	0.0022
C	0.0020	0.0021	0.0023	0.0024
D	0.0020	0.0021	0.0022	0.0024

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X19_P0	**X19_P4**	**X19_P0**	**X19_P4**
A to Z ↓	0.0485	0.0551	0.7004	0.7459
A to Z ↑	0.0393	0.0445	0.9757	1.0616
B to Z ↓	0.0497	0.0562	0.7012	0.7466
B to Z ↑	0.0384	0.0435	0.9759	1.0617
C to Z ↓	0.0468	0.0531	0.7009	0.7463
C to Z ↑	0.0361	0.0409	0.9742	1.0621
D to Z ↓	0.0477	0.0539	0.7008	0.7462
D to Z ↑	0.0351	0.0398	0.9746	1.0620
	X19_P10	**X19_P16**	**X19_P10**	**X19_P16**
A to Z ↓	0.0650	0.0744	0.8112	0.8685
A to Z ↑	0.0520	0.0589	1.1875	1.3042
B to Z ↓	0.0660	0.0753	0.8112	0.8695
B to Z ↑	0.0509	0.0576	1.1880	1.3026
C to Z ↓	0.0626	0.0716	0.8109	0.8689
C to Z ↑	0.0478	0.0542	1.1873	1.3045
D to Z ↓	0.0633	0.0722	0.8112	0.8686
D to Z ↑	0.0466	0.0528	1.1873	1.3036
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0248	0.0283	0.6122	0.6548
A to Z ↑	0.0244	0.0274	0.6345	0.6936
B to Z ↓	0.0256	0.0290	0.6124	0.6549
B to Z ↑	0.0223	0.0251	0.6334	0.6923
C to Z ↓	0.0241	0.0273	0.6114	0.6538
C to Z ↑	0.0225	0.0252	0.6370	0.6959
D to Z ↓	0.0237	0.0265	0.6111	0.6538
D to Z ↑	0.0207	0.0230	0.6357	0.6949
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0336	0.0383	0.7158	0.7712
A to Z ↑	0.0318	0.0356	0.7779	0.8547
B to Z ↓	0.0339	0.0383	0.7162	0.7719
B to Z ↑	0.0291	0.0326	0.7768	0.8538
C to Z ↓	0.0321	0.0365	0.7149	0.7699
C to Z ↑	0.0290	0.0324	0.7809	0.8588
D to Z ↓	0.0309	0.0349	0.7145	0.7703
D to Z ↑	0.0264	0.0295	0.7797	0.8573

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X19_P0	2.205e-05	1.000e-20
X19_P4	4.627e-06	1.000e-20
X19_P10	1.017e-06	1.000e-20
X19_P16	4.814e-07	1.000e-20
X27_P0	4.028e-05	1.000e-20
X27_P4	8.207e-06	1.000e-20
X27_P10	1.810e-06	1.000e-20
X27_P16	9.125e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	5.951e-04	5.991e-04	6.220e-04	6.468e-04

B (output stable)	5.620e-04	5.492e-04	5.579e-04	5.747e-04
C (output stable)	4.854e-04	4.859e-04	5.009e-04	5.205e-04
D (output stable)	4.514e-04	4.337e-04	4.319e-04	4.381e-04
A to Z	7.429e-03	7.409e-03	7.578e-03	7.822e-03
B to Z	7.342e-03	7.301e-03	7.446e-03	7.677e-03
C to Z	7.122e-03	7.088e-03	7.229e-03	7.457e-03
D to Z	7.068e-03	7.010e-03	7.129e-03	7.343e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	2.749e-03	2.775e-03	2.902e-03	3.048e-03
B (output stable)	2.446e-03	2.325e-03	2.345e-03	2.449e-03
C (output stable)	2.561e-03	2.584e-03	2.713e-03	2.846e-03
D (output stable)	2.277e-03	2.135e-03	2.118e-03	2.109e-03
A to Z	1.196e-02	1.197e-02	1.238e-02	1.284e-02
B to Z	1.106e-02	1.095e-02	1.123e-02	1.159e-02
C to Z	1.017e-02	9.912e-03	1.006e-02	1.034e-02
D to Z	9.305e-03	8.902e-03	8.871e-03	9.045e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

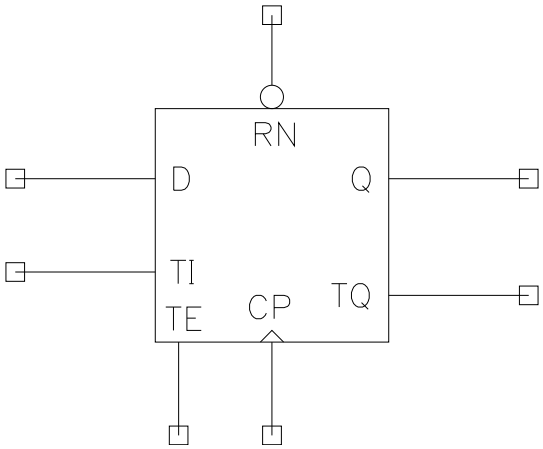
Pin Cycle (vdds)	X19_P0	X19_P4	X19_P10	X19_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D (output stable)	0.000e+00	0.000e+00	0.000e+00	0.000e+00
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
B to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
C to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
D to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

CNSDFPRQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	1.600	2.176	3.4816
X9_P4	1.600	2.176	3.4816
X9_P10	1.600	2.176	3.4816
X9_P16	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
CP	0.0005	0.0005	0.0005	0.0006
D	0.0005	0.0005	0.0005	0.0005
RN	0.0007	0.0008	0.0008	0.0009

TE	0.0008	0.0008	0.0009	0.0010
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	X9_P4	X9_P0	X9_P4
CP to Q ↓	0.0634	0.0715	1.4382	1.5328
CP to Q ↑	0.0666	0.0752	1.8554	2.0231
CP to TQ ↓	0.0651	0.0735	4.9599	5.2639
CP to TQ ↑	0.0697	0.0788	9.7969	10.9498
RN to Q ↓	0.0583	0.0661	1.4392	1.5329
RN to TQ ↓	0.0599	0.0681	4.9593	5.2634
	X9_P10	X9_P16	X9_P10	X9_P16
CP to Q ↓	0.0838	0.0954	1.6639	1.7828
CP to Q ↑	0.0881	0.0999	2.2654	2.4883
CP to TQ ↓	0.0862	0.0982	5.6867	6.0633
CP to TQ ↑	0.0923	0.1047	12.5065	13.8611
RN to Q ↓	0.0775	0.0882	1.6648	1.7809
RN to TQ ↓	0.0799	0.0910	5.6873	6.0629

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X9_P0	X9_P4	X9_P10	X9_P16
CP ↓	min_pulse_width to CP	0.0543	0.0636	0.0776	0.0934
CP ↑	min_pulse_width to CP	0.0360	0.0392	0.0437	0.0482
D ↓	hold_rising to CP	-0.0023	-0.0045	-0.0094	-0.0148
D ↑	hold_rising to CP	-0.0000	-0.0022	-0.0045	-0.0071
D ↓	setup_rising to CP	0.0370	0.0418	0.0538	0.0661
D ↑	setup_rising to CP	0.0249	0.0266	0.0319	0.0368
RN ↓	min_pulse_width to RN	0.0447	0.0491	0.0562	0.0659
RN ↑	recovery_rising to CP	0.0081	0.0103	0.0129	0.0178
RN ↑	removal_rising to CP	-0.0006	-0.0006	-0.0060	-0.0060
TE ↓	hold_rising to CP	0.0026	-0.0023	-0.0077	-0.0094
TE ↑	hold_rising to CP	-0.0044	-0.0098	-0.0147	-0.0169
TE ↓	setup_rising to CP	0.0345	0.0425	0.0517	0.0636
TE ↑	setup_rising to CP	0.0644	0.0737	0.0959	0.1154
TI ↓	hold_rising to CP	-0.0280	-0.0398	-0.0502	-0.0599
TI ↑	hold_rising to CP	-0.0049	-0.0104	-0.0169	-0.0182
TI ↓	setup_rising to CP	0.0624	0.0737	0.0946	0.1148
TI ↑	setup_rising to CP	0.0355	0.0361	0.0430	0.0522

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X9_P0	3.436e-05	1.000e-20
X9_P4	6.806e-06	1.000e-20
X9_P10	1.466e-06	1.000e-20
X9_P16	7.278e-07	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

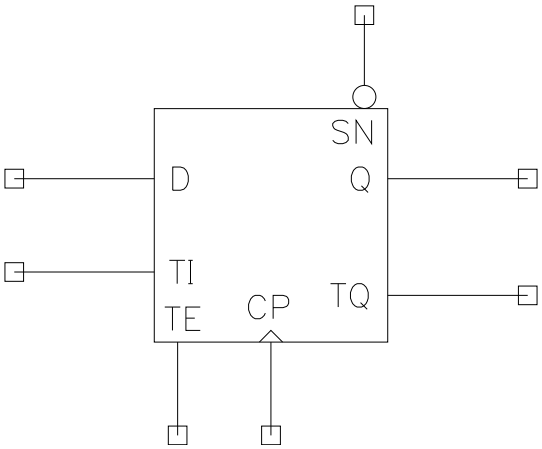
Pin Cycle	X9_P0	X9_P4	X9_P10	X9_P16
Clock 100Mhz Data 0Mhz	6.725e-03	6.725e-03	6.785e-03	6.863e-03
Clock 100Mhz Data 25Mhz	7.175e-03	7.186e-03	7.299e-03	7.440e-03
Clock 100Mhz Data 50Mhz	7.626e-03	7.647e-03	7.814e-03	8.016e-03
Clock = 0 Data 100Mhz	2.899e-03	2.927e-03	2.979e-03	3.039e-03
Clock = 1 Data 100Mhz	4.347e-05	4.022e-05	3.772e-05	3.598e-05

CNSDFPSQT

Cell Description

Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q and non-inverted test output TQ for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	1.600	2.176	3.4816
X9_P4	1.600	2.176	3.4816
X9_P10	1.600	2.176	3.4816
X9_P16	1.600	2.176	3.4816

Truth Table

IQ	Q
IQ	IQ

IQ	TQ
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI
-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
CP	0.0005	0.0005	0.0005	0.0006
D	0.0003	0.0003	0.0003	0.0004
SN	0.0008	0.0008	0.0009	0.0010

TE	0.0008	0.0009	0.0009	0.0010
TI	0.0004	0.0004	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	X9_P4	X9_P0	X9_P4
CP to Q ↓	0.0630	0.0712	1.4414	1.5332
CP to Q ↑	0.0648	0.0733	1.8570	2.0260
CP to TQ ↓	0.0644	0.0729	4.9688	5.2709
CP to TQ ↑	0.0676	0.0766	9.7812	10.9255
SN to Q ↑	0.0484	0.0550	1.8581	2.0279
SN to TQ ↑	0.0513	0.0584	9.7789	10.9310
	X9_P10	X9_P16	X9_P10	X9_P16
CP to Q ↓	0.0835	0.0952	1.6626	1.7778
CP to Q ↑	0.0859	0.0979	2.2658	2.4929
CP to TQ ↓	0.0857	0.0977	5.6970	6.0710
CP to TQ ↑	0.0900	0.1025	12.4875	13.8324
SN to Q ↑	0.0646	0.0737	2.2657	2.4926
SN to TQ ↑	0.0687	0.0783	12.4852	13.8365

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	X9_P0	X9_P4	X9_P10	X9_P16
CP ↓	min_pulse_width to CP	0.0591	0.0701	0.0859	0.0989
CP ↑	min_pulse_width to CP	0.0359	0.0391	0.0436	0.0481
D ↓	hold_rising to CP	-0.0077	-0.0094	-0.0143	-0.0197
D ↑	hold_rising to CP	0.0010	-0.0049	-0.0071	-0.0120
D ↓	setup_rising to CP	0.0419	0.0489	0.0587	0.0684
D ↑	setup_rising to CP	0.0266	0.0320	0.0368	0.0394
SN ↓	min_pulse_width to SN	0.0398	0.0447	0.0518	0.0540
SN ↑	recovery_rising to CP	-0.0071	-0.0017	-0.0017	0.0009
SN ↑	removal_rising to CP	0.0236	0.0259	0.0312	0.0335
TE ↓	hold_rising to CP	-0.0023	-0.0072	-0.0126	-0.0143
TE ↑	hold_rising to CP	-0.0023	-0.0049	-0.0098	-0.0147
TE ↓	setup_rising to CP	0.0403	0.0468	0.0587	0.0685
TE ↑	setup_rising to CP	0.0689	0.0839	0.1036	0.1199
TI ↓	hold_rising to CP	-0.0342	-0.0440	-0.0551	-0.0661
TI ↑	hold_rising to CP	-0.0043	-0.0056	-0.0104	-0.0169
TI ↓	setup_rising to CP	0.0673	0.0826	0.0994	0.1140
TI ↑	setup_rising to CP	0.0291	0.0355	0.0361	0.0417

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X9_P0	3.079e-05	1.000e-20
X9_P4	6.287e-06	1.000e-20
X9_P10	1.418e-06	1.000e-20
X9_P16	7.301e-07	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

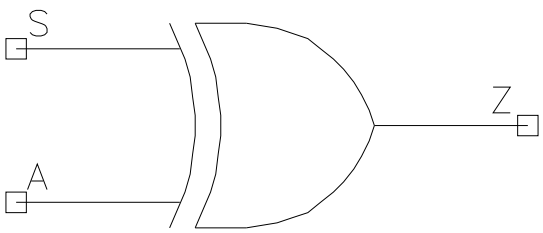
Pin Cycle	X9_P0	X9_P4	X9_P10	X9_P16
Clock 100Mhz Data 0Mhz	6.585e-03	6.587e-03	6.631e-03	6.684e-03
Clock 100Mhz Data 25Mhz	7.090e-03	7.106e-03	7.214e-03	7.347e-03
Clock 100Mhz Data 50Mhz	7.595e-03	7.624e-03	7.797e-03	8.011e-03
Clock = 0 Data 100Mhz	3.045e-03	3.072e-03	3.121e-03	3.179e-03
Clock = 1 Data 100Mhz	4.138e-05	3.924e-05	3.996e-05	4.074e-05

CNXOR2

Cell Description

2 input Exclusive OR for Clock network

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
X9_P0	0.800	1.496	1.1968
X9_P4	0.800	1.496	1.1968
X9_P10	0.800	1.496	1.1968
X9_P16	0.800	1.496	1.1968
X15_P0	0.800	2.312	1.8496
X15_P4	0.800	2.312	1.8496
X15_P10	0.800	2.312	1.8496
X15_P16	0.800	2.312	1.8496
X27_P0	0.800	2.584	2.0672
X27_P4	0.800	2.584	2.0672
X27_P10	0.800	2.584	2.0672
X27_P16	0.800	2.584	2.0672

Truth Table

A	S	Z
1	S	!S
0	S	S

Pin Capacitance

Pin	X9_P0	X9_P4	X9_P10	X9_P16
A	0.0006	0.0007	0.0007	0.0007
S	0.0013	0.0013	0.0014	0.0015
	X15_P0	X15_P4	X15_P10	X15_P16
A	0.0012	0.0012	0.0013	0.0014
S	0.0020	0.0021	0.0022	0.0023
	X27_P0	X27_P4	X27_P10	X27_P16
A	0.0010	0.0011	0.0012	0.0012
S	0.0020	0.0021	0.0022	0.0023

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	X9_P0	**X9_P4**	**X9_P0**	**X9_P4**
A to Z ↓	0.0311	0.0352	1.5047	1.6033
A to Z ↑	0.0296	0.0331	2.0770	2.2640
S to Z ↓	0.0242	0.0273	1.4993	1.5981
S to Z ↑	0.0235	0.0265	2.0746	2.2601
	X9_P10	**X9_P16**	**X9_P10**	**X9_P16**
A to Z ↓	0.0411	0.0466	1.7452	1.8733
A to Z ↑	0.0383	0.0430	2.5322	2.7808
S to Z ↓	0.0317	0.0357	1.7405	1.8687
S to Z ↑	0.0307	0.0346	2.5310	2.7798
	X15_P0	**X15_P4**	**X15_P0**	**X15_P4**
A to Z ↓	0.0288	0.0327	0.9483	1.0116
A to Z ↑	0.0274	0.0309	1.1006	1.2028
S to Z ↓	0.0215	0.0245	0.9473	1.0088
S to Z ↑	0.0201	0.0229	1.0997	1.2026
	X15_P10	**X15_P16**	**X15_P10**	**X15_P16**
A to Z ↓	0.0384	0.0436	1.0999	1.1786
A to Z ↑	0.0360	0.0405	1.3492	1.4838
S to Z ↓	0.0288	0.0326	1.0981	1.1775
S to Z ↑	0.0267	0.0301	1.3492	1.4838
	X27_P0	**X27_P4**	**X27_P0**	**X27_P4**
A to Z ↓	0.0346	0.0390	0.5452	0.5819
A to Z ↑	0.0336	0.0377	0.6628	0.7231
S to Z ↓	0.0270	0.0305	0.5445	0.5812
S to Z ↑	0.0256	0.0288	0.6624	0.7223
	X27_P10	**X27_P16**	**X27_P10**	**X27_P16**
A to Z ↓	0.0458	0.0521	0.6343	0.6821
A to Z ↑	0.0438	0.0494	0.8103	0.8914
S to Z ↓	0.0359	0.0408	0.6337	0.6814
S to Z ↑	0.0337	0.0381	0.8103	0.8916

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
X9_P0	2.923e-05	1.000e-20
X9_P4	5.473e-06	1.000e-20
X9_P10	1.022e-06	1.000e-20
X9_P16	4.218e-07	1.000e-20
X15_P0	5.205e-05	1.000e-20
X15_P4	9.546e-06	1.000e-20
X15_P10	1.747e-06	1.000e-20
X15_P16	7.182e-07	1.000e-20
X27_P0	6.417e-05	1.000e-20
X27_P4	1.152e-05	1.000e-20
X27_P10	2.064e-06	1.000e-20
X27_P16	8.422e-07	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	X9_P0	X9_P4	X9_P10	X9_P16
A to Z	4.765e-03	4.612e-03	4.612e-03	4.707e-03
S to Z	4.187e-03	4.001e-03	3.959e-03	4.019e-03
	X15_P0	X15_P4	X15_P10	X15_P16

A to Z	8.415e-03	8.131e-03	8.134e-03	8.281e-03
S to Z	5.944e-03	5.531e-03	5.362e-03	5.377e-03
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	1.150e-02	1.082e-02	1.061e-02	1.070e-02
S to Z	9.391e-03	8.571e-03	8.193e-03	8.165e-03

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

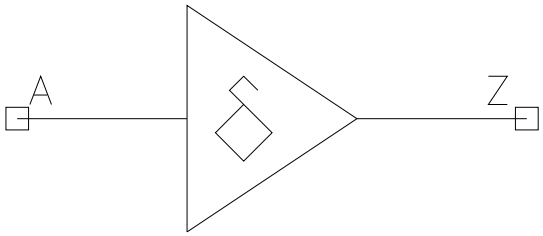
Pin Cycle (vdds)	X9_P0	X9_P4	X9_P10	X9_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X15_P0	X15_P4	X15_P10	X15_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	X27_P0	X27_P4	X27_P10	X27_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
S to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

DLYHF

Cell Description

Delay cell for Hold Time Fixing

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOI_LL_-DLYHFM4X4_P0	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X4_P4	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X4_P10	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X4_P16	0.800	1.224	0.9792
C8T28SOI_LL_-DLYHFM4X12_P0	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM4X12_P4	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM4X12_P10	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM4X12_P16	0.800	1.496	1.1968
C8T28SOI_LL_-DLYHFM8X4_P0	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X4_P4	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X4_P10	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X4_P16	0.800	3.536	2.8288
C8T28SOI_LL_-DLYHFM8X12_P0	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X12_P4	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X12_P10	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X12_P16	0.800	3.808	3.0464
C8T28SOI_LL_-DLYHFM8X30_P0	0.800	5.848	4.6784

C8T28SOI_LL_-DLYHFM8X30_P4	0.800	5.848	4.6784
C8T28SOI_LL_-DLYHFM8X30_P10	0.800	5.848	4.6784
C8T28SOI_LL_-DLYHFM8X30_P16	0.800	5.848	4.6784

Truth Table

A	Z
A	A

Pin Capacitance

Pin	C8T28SOI_LL_-DLYHFM4X4_P0	C8T28SOI_LL_-DLYHFM4X4_P4	C8T28SOI_LL_-DLYHFM4X4_P10	C8T28SOI_LL_-DLYHFM4X4_P16
A	0.0008	0.0008	0.0008	0.0009
	C8T28SOI_LL_-DLYHFM4X12_P0	C8T28SOI_LL_-DLYHFM4X12_P4	C8T28SOI_LL_-DLYHFM4X12_P10	C8T28SOI_LL_-DLYHFM4X12_P16
A	0.0007	0.0008	0.0008	0.0008
	C8T28SOI_LL_-DLYHFM8X4_P0	C8T28SOI_LL_-DLYHFM8X4_P4	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A	0.0007	0.0007	0.0007	0.0008
	C8T28SOI_LL_-DLYHFM8X12_P0	C8T28SOI_LL_-DLYHFM8X12_P4	C8T28SOI_LL_-DLYHFM8X12_P10	C8T28SOI_LL_-DLYHFM8X12_P16
A	0.0007	0.0007	0.0007	0.0007
	C8T28SOI_LL_-DLYHFM8X30_P0	C8T28SOI_LL_-DLYHFM8X30_P4	C8T28SOI_LL_-DLYHFM8X30_P10	C8T28SOI_LL_-DLYHFM8X30_P16
A	0.0007	0.0007	0.0007	0.0007

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOI_LL_-DLYHFM4X4_P0	**C8T28SOI_LL_-DLYHFM4X4_P4**	**C8T28SOI_LL_-DLYHFM4X4_P0**	**C8T28SOI_LL_-DLYHFM4X4_P4**
A to Z ↓	0.0696	0.0783	3.3518	3.5693
A to Z ↑	0.0659	0.0743	3.8922	4.2472
	C8T28SOI_LL_-DLYHFM4X4_P10	**C8T28SOI_LL_-DLYHFM4X4_P16**	**C8T28SOI_LL_-DLYHFM4X4_P10**	**C8T28SOI_LL_-DLYHFM4X4_P16**
A to Z ↓	0.0917	0.1049	3.8782	4.1552
A to Z ↑	0.0872	0.0997	4.7644	5.2395
	C8T28SOI_LL_-DLYHFM4X12_P0	**C8T28SOI_LL_-DLYHFM4X12_P4**	**C8T28SOI_LL_-DLYHFM4X12_P0**	**C8T28SOI_LL_-DLYHFM4X12_P4**
A to Z ↓	0.0784	0.0886	1.1874	1.2699
A to Z ↑	0.0730	0.0825	1.4850	1.6231
	C8T28SOI_LL_-DLYHFM4X12_P10	**C8T28SOI_LL_-DLYHFM4X12_P16**	**C8T28SOI_LL_-DLYHFM4X12_P10**	**C8T28SOI_LL_-DLYHFM4X12_P16**
A to Z ↓	0.1045	0.1202	1.3885	1.4964
A to Z ↑	0.0971	0.1115	1.8258	2.0106
	C8T28SOI_LL_-DLYHFM8X4_P0	**C8T28SOI_LL_-DLYHFM8X4_P4**	**C8T28SOI_LL_-DLYHFM8X4_P0**	**C8T28SOI_LL_-DLYHFM8X4_P4**
A to Z ↓	0.1333	0.1511	3.3443	3.5627
A to Z ↑	0.1188	0.1336	3.8210	4.1671

	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A to Z ↓	0.1797	0.2082	3.8651	4.1376
A to Z ↑	0.1570	0.1797	4.6688	5.1328
	C8T28SOI_LL_-DLYHFM8X12_P0	**C8T28SOI_LL_-DLYHFM8X12_P4**	**C8T28SOI_LL_-DLYHFM8X12_P0**	**C8T28SOI_LL_-DLYHFM8X12_P4**
A to Z ↓	0.1433	0.1626	1.1777	1.2608
A to Z ↑	0.1269	0.1429	1.4783	1.6162
	C8T28SOI_LL_-DLYHFM8X12_P10	**C8T28SOI_LL_-DLYHFM8X12_P16**	**C8T28SOI_LL_-DLYHFM8X12_P10**	**C8T28SOI_LL_-DLYHFM8X12_P16**
A to Z ↓	0.1939	0.2251	1.3782	1.4840
A to Z ↑	0.1683	0.1930	1.8153	1.9993
	C8T28SOI_LL_-DLYHFM8X30_P0	**C8T28SOI_LL_-DLYHFM8X30_P4**	**C8T28SOI_LL_-DLYHFM8X30_P0**	**C8T28SOI_LL_-DLYHFM8X30_P4**
A to Z ↓	0.1808	0.2051	0.4552	0.4854
A to Z ↑	0.1773	0.2009	0.5929	0.6479
	C8T28SOI_LL_-DLYHFM8X30_P10	**C8T28SOI_LL_-DLYHFM8X30_P16**	**C8T28SOI_LL_-DLYHFM8X30_P10**	**C8T28SOI_LL_-DLYHFM8X30_P16**
A to Z ↓	0.2442	0.2833	0.5282	0.5669
A to Z ↑	0.2383	0.2755	0.7257	0.7981

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOI_LL_DLYHFM4X4_P0	4.833e-06	1.000e-20
C8T28SOI_LL_DLYHFM4X4_P4	1.002e-06	1.000e-20
C8T28SOI_LL_DLYHFM4X4_P10	2.615e-07	1.000e-20
C8T28SOI_LL_DLYHFM4X4_P16	1.637e-07	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P0	1.169e-05	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P4	2.246e-06	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P10	4.931e-07	1.000e-20
C8T28SOI_LL_DLYHFM4X12_P16	2.639e-07	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P0	6.532e-06	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P4	1.606e-06	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P10	5.829e-07	1.000e-20
C8T28SOI_LL_DLYHFM8X4_P16	4.508e-07	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P0	1.312e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P4	2.785e-06	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P10	7.964e-07	1.000e-20
C8T28SOI_LL_DLYHFM8X12_P16	5.397e-07	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P0	3.260e-05	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P4	6.590e-06	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P10	1.691e-06	1.000e-20
C8T28SOI_LL_DLYHFM8X30_P16	1.059e-06	1.000e-20

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle (vdd)	C8T28SOI_LL_-DLYHFM4X4_P0	C8T28SOI_LL_-DLYHFM4X4_P4	C8T28SOI_LL_-DLYHFM4X4_P10	C8T28SOI_LL_-DLYHFM4X4_P16
A to Z	3.770e-03	3.839e-03	4.002e-03	4.186e-03
	C8T28SOI_LL_-DLYHFM4X12_P0	C8T28SOI_LL_-DLYHFM4X12_P4	C8T28SOI_LL_-DLYHFM4X12_P10	C8T28SOI_LL_-DLYHFM4X12_P16
A to Z	6.014e-03	5.877e-03	5.936e-03	6.107e-03

	C8T28SOI_LL_-DLYHFM8X4_P0	C8T28SOI_LL_-DLYHFM8X4_P4	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A to Z	1.114e-02	1.136e-02	1.189e-02	1.246e-02
	C8T28SOI_LL_-DLYHFM8X12_P0	C8T28SOI_LL_-DLYHFM8X12_P4	C8T28SOI_LL_-DLYHFM8X12_P10	C8T28SOI_LL_-DLYHFM8X12_P16
A to Z	1.295e-02	1.297e-02	1.340e-02	1.394e-02
	C8T28SOI_LL_-DLYHFM8X30_P0	C8T28SOI_LL_-DLYHFM8X30_P4	C8T28SOI_LL_-DLYHFM8X30_P10	C8T28SOI_LL_-DLYHFM8X30_P16
A to Z	2.389e-02	2.404e-02	2.488e-02	2.598e-02

Internal Energy (uW/MHz) at Minimum Output Load, 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

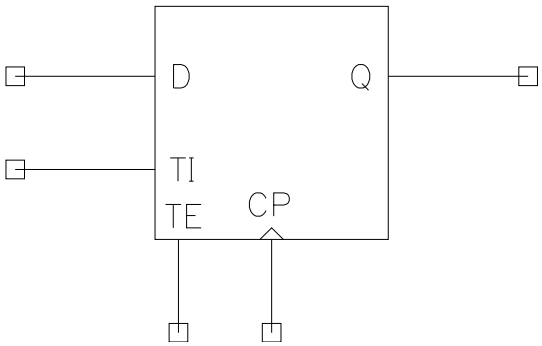
Pin Cycle (vdds)	C8T28SOI_LL_-DLYHFM4X4_P0	C8T28SOI_LL_-DLYHFM4X4_P4	C8T28SOI_LL_-DLYHFM4X4_P10	C8T28SOI_LL_-DLYHFM4X4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM4X12_P0	C8T28SOI_LL_-DLYHFM4X12_P4	C8T28SOI_LL_-DLYHFM4X12_P10	C8T28SOI_LL_-DLYHFM4X12_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM8X4_P0	C8T28SOI_LL_-DLYHFM8X4_P4	C8T28SOI_LL_-DLYHFM8X4_P10	C8T28SOI_LL_-DLYHFM8X4_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM8X12_P0	C8T28SOI_LL_-DLYHFM8X12_P4	C8T28SOI_LL_-DLYHFM8X12_P10	C8T28SOI_LL_-DLYHFM8X12_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00
	C8T28SOI_LL_-DLYHFM8X30_P0	C8T28SOI_LL_-DLYHFM8X30_P4	C8T28SOI_LL_-DLYHFM8X30_P10	C8T28SOI_LL_-DLYHFM8X30_P16
A to Z	0.000e+00	0.000e+00	0.000e+00	0.000e+00

SDFSYNCPQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	1.600	3.264	5.2224
C8T28SOIDV_LL1_-SDFSYNCPQX5_P4	1.600	3.264	5.2224
C8T28SOIDV_LL1_-SDFSYNCPQX5_P10	1.600	3.264	5.2224
C8T28SOIDV_LL1_-SDFSYNCPQX5_P16	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P0	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P4	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P10	1.600	3.264	5.2224
C8T28SOIDV_LL_-SDFSYNCPQX5_P16	1.600	3.264	5.2224

Truth Table

IQ	Q
IQ	IQ

D	CP	TI	TE	IQ	IQ
D	/	-	0	-	D
-	/	TI	1	-	TI
-	-	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	C8T28SOIDV_LL1_-SDFSYNCPQX5_P4	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16
CP	0.0007	0.0007	0.0007	0.0008
D	0.0009	0.0009	0.0010	0.0010
TE	0.0008	0.0009	0.0009	0.0010
TI	0.0004	0.0004	0.0004	0.0004
	C8T28SOIDV_LL_-SDFSYNCPQX5_P0	C8T28SOIDV_LL_-SDFSYNCPQX5_P4	C8T28SOIDV_LL_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPQX5_-P16
CP	0.0004	0.0005	0.0005	0.0005
D	0.0004	0.0004	0.0005	0.0005
TE	0.0008	0.0008	0.0009	0.0010
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	**C8T28SOIDV_LL1_-SDFSYNCPQX5_P4**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_P0**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_P4**
CP to Q ↓	0.0668	0.0753	3.0225	3.2716
CP to Q ↑	0.0780	0.0883	3.8907	4.2603
	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10	**C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10**	**C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16**
CP to Q ↓	0.0886	0.1011	3.6358	3.9816
CP to Q ↑	0.1043	0.1197	4.7983	5.2968
	C8T28SOIDV_LL_-SDFSYNCPQX5_P0	**C8T28SOIDV_LL_-SDFSYNCPQX5_P4**	**C8T28SOIDV_LL_-SDFSYNCPQX5_P0**	**C8T28SOIDV_LL_-SDFSYNCPQX5_P4**
CP to Q ↓	0.0985	0.1116	3.2668	3.5667
CP to Q ↑	0.1197	0.1364	3.9382	4.3157
	C8T28SOIDV_LL_-SDFSYNCPQX5_-P10	**C8T28SOIDV_LL_-SDFSYNCPQX5_-P16**	**C8T28SOIDV_LL_-SDFSYNCPQX5_-P10**	**C8T28SOIDV_LL_-SDFSYNCPQX5_-P16**
CP to Q ↓	0.1316	0.1506	4.0096	4.4356
CP to Q ↑	0.1626	0.1886	4.8661	5.3796

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P0	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P4	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P10	C8T28SOIDV_-LL1_SDF-SYNCPQX5_P16
CP ↓	min_pulse_width to CP	0.0960	0.1134	0.1392	0.1626
CP ↑	min_pulse_width to CP	0.0545	0.0590	0.0717	0.0810
D ↓	hold_rising to CP	-0.0196	-0.0268	-0.0343	-0.0420
D ↑	hold_rising to CP	-0.0049	-0.0066	-0.0120	-0.0169
D ↓	setup_rising to CP	0.0565	0.0646	0.0760	0.0911
D ↑	setup_rising to CP	0.0293	0.0314	0.0368	0.0416
TE ↓	hold_rising to CP	-0.0224	-0.0263	-0.0344	-0.0410
TE ↑	hold_rising to CP	-0.0212	-0.0266	-0.0315	-0.0386

TE ↓	setup_rising to CP	0.0561	0.0636	0.0787	0.0901
TE ↑	setup_rising to CP	0.1301	0.1519	0.1866	0.2180
TI ↓	hold_rising to CP	-0.0974	-0.1192	-0.1450	-0.1694
TI ↑	hold_rising to CP	-0.0223	-0.0277	-0.0341	-0.0403
TI ↓	setup_rising to CP	0.1323	0.1531	0.1839	0.2129
TI ↑	setup_rising to CP	0.0515	0.0576	0.0640	0.0701
		C8T28SOIDV_-LL_SDF-SYNCPQX5_P0	C8T28SOIDV_-LL_SDF-SYNCPQX5_P4	C8T28SOIDV_-LL_SDF-SYNCPQX5_P10	C8T28SOIDV_-LL_SDF-SYNCPQX5_P16
CP ↓	min_pulse_width to CP	0.1699	0.1981	0.2413	0.2846
CP ↑	min_pulse_width to CP	0.0779	0.0872	0.1044	0.1184
D ↓	hold_rising to CP	-0.0436	-0.0534	-0.0681	-0.0833
D ↑	hold_rising to CP	-0.0338	-0.0413	-0.0484	-0.0582
D ↓	setup_rising to CP	0.0981	0.1155	0.1376	0.1620
D ↑	setup_rising to CP	0.0638	0.0713	0.0783	0.0881
TE ↓	hold_rising to CP	-0.0414	-0.0512	-0.0632	-0.0728
TE ↑	hold_rising to CP	-0.0533	-0.0635	-0.0755	-0.0853
TE ↓	setup_rising to CP	0.0956	0.1102	0.1323	0.1572
TE ↑	setup_rising to CP	0.1616	0.1909	0.2326	0.2722
TI ↓	hold_rising to CP	-0.1026	-0.1277	-0.1576	-0.1834
TI ↑	hold_rising to CP	-0.0565	-0.0654	-0.0765	-0.0879
TI ↓	setup_rising to CP	0.1615	0.1918	0.2278	0.2675
TI ↑	setup_rising to CP	0.0905	0.0969	0.1122	0.1227

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL1_SDFSYNCPQX5_-P0	5.012e-05	1.000e-20
C8T28SOIDV_LL1_SDFSYNCPQX5_-P4	9.959e-06	1.000e-20
C8T28SOIDV_LL1_SDFSYNCPQX5_-P10	2.195e-06	1.000e-20
C8T28SOIDV_LL1_SDFSYNCPQX5_-P16	1.138e-06	1.000e-20
C8T28SOIDV_LL_SDFSYNCPQX5_-P0	5.165e-05	1.000e-20
C8T28SOIDV_LL_SDFSYNCPQX5_-P4	1.007e-05	1.000e-20
C8T28SOIDV_LL_SDFSYNCPQX5_-P10	2.178e-06	1.000e-20

C8T28SOIDV_LL_SDFSYNCPQX5_-P16	1.121e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

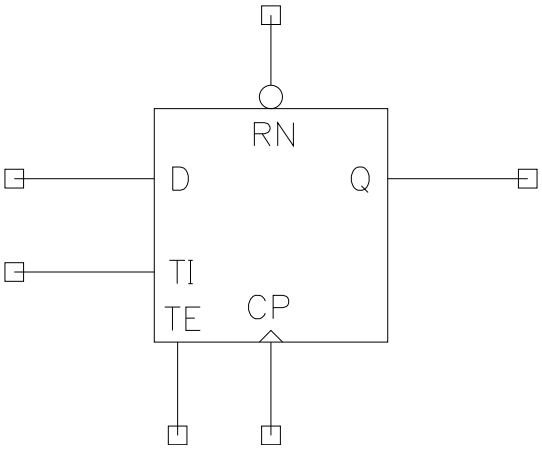
Pin Cycle	C8T28SOIDV_LL1_-SDFSYNCPQX5_P0	C8T28SOIDV_LL1_-SDFSYNCPQX5_P4	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPQX5_-P16
Clock 100Mhz Data 0Mhz	1.420e-02	1.434e-02	1.460e-02	1.492e-02
Clock 100Mhz Data 25Mhz	1.458e-02	1.465e-02	1.491e-02	1.531e-02
Clock 100Mhz Data 50Mhz	1.495e-02	1.496e-02	1.522e-02	1.570e-02
Clock = 0 Data 100Mhz	8.006e-03	7.986e-03	8.055e-03	8.167e-03
Clock = 1 Data 100Mhz	8.910e-05	8.342e-05	9.286e-05	1.112e-04
	C8T28SOIDV_LL_-SDFSYNCPQX5_P0	C8T28SOIDV_LL_-SDFSYNCPQX5_P4	C8T28SOIDV_LL_-SDFSYNCPQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPQX5_-P16
Clock 100Mhz Data 0Mhz	1.486e-02	1.490e-02	1.505e-02	1.527e-02
Clock 100Mhz Data 25Mhz	1.588e-02	1.590e-02	1.610e-02	1.644e-02
Clock 100Mhz Data 50Mhz	1.691e-02	1.689e-02	1.715e-02	1.762e-02
Clock = 0 Data 100Mhz	8.905e-03	9.265e-03	9.473e-03	9.662e-03
Clock = 1 Data 100Mhz	9.664e-05	8.612e-05	8.158e-05	8.080e-05

SDFSYNCPRQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Reset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P0	1.600	3.944	6.3104
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P4	1.600	3.944	6.3104
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P10	1.600	3.944	6.3104
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P16	1.600	3.944	6.3104
C8T28SOIDV_LL_-SDFSYNCPRQX5_P0	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPRQX5_P4	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPRQX5_P10	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPRQX5_P16	1.600	4.080	6.5280

Truth Table

IQ	Q
IQ	IQ

D	CP	RN	TI	TE	IQ	IQ
-	-	0	-	-	-	0
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI

-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16
CP	0.0007	0.0007	0.0007	0.0008
D	0.0009	0.0009	0.0010	0.0010
RN	0.0013	0.0013	0.0014	0.0015
TE	0.0008	0.0008	0.0009	0.0010
TI	0.0003	0.0003	0.0003	0.0003
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16
CP	0.0004	0.0004	0.0005	0.0005
D	0.0004	0.0005	0.0005	0.0005
RN	0.0019	0.0020	0.0022	0.0023
TE	0.0008	0.0008	0.0009	0.0010
TI	0.0003	0.0003	0.0003	0.0003

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	**Intrinsic Delay (ns)**		**Kload (ns/pf)**	
	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4**
CP to Q ↓	0.0745	0.0842	3.0183	3.2629
CP to Q ↑	0.0803	0.0909	3.8804	4.2485
RN to Q ↓	0.0729	0.0832	2.5956	2.7948
	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10**	**C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16**
CP to Q ↓	0.0990	0.1132	3.6250	3.9638
CP to Q ↑	0.1074	0.1232	4.7845	5.2786
RN to Q ↓	0.0979	0.1121	3.0734	3.3229
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4**
CP to Q ↓	0.1077	0.1214	3.2588	3.5537
CP to Q ↑	0.1258	0.1433	3.9499	4.3309
RN to Q ↓	0.0760	0.0867	2.6104	2.8151
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10**	**C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16**
CP to Q ↓	0.1426	0.1629	3.9965	4.4096
CP to Q ↑	0.1712	0.1989	4.8851	5.3918
RN to Q ↓	0.1025	0.1171	3.0938	3.3465

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P0	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P4	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P10	C8T28SOIDV_-LL1_SDF-SYNCPRQX5_-P16
CP ↓	min_pulse_width to CP	0.1032	0.1206	0.1464	0.1705
CP ↑	min_pulse_width to CP	0.0626	0.0685	0.0812	0.0918
D ↓	hold_rising to CP	-0.0218	-0.0267	-0.0371	-0.0436
D ↑	hold_rising to CP	-0.0098	-0.0114	-0.0169	-0.0218
D ↓	setup_rising to CP	0.0597	0.0662	0.0835	0.0981
D ↑	setup_rising to CP	0.0346	0.0395	0.0443	0.0491
RN ↓	min_pulse_width to RN	0.0854	0.0974	0.1143	0.1289
RN ↑	recovery_rising to CP	0.0005	0.0031	0.0027	0.0032
RN ↑	removal_rising to CP	0.0043	0.0047	0.0016	0.0047
TE ↓	hold_rising to CP	-0.0214	-0.0289	-0.0334	-0.0410
TE ↑	hold_rising to CP	-0.0261	-0.0315	-0.0413	-0.0462
TE ↓	setup_rising to CP	0.0588	0.0685	0.0836	0.0982
TE ↑	setup_rising to CP	0.1350	0.1568	0.1936	0.2283
TI ↓	hold_rising to CP	-0.0990	-0.1192	-0.1443	-0.1694
TI ↑	hold_rising to CP	-0.0315	-0.0326	-0.0439	-0.0486
TI ↓	setup_rising to CP	0.1336	0.1587	0.1885	0.2229
TI ↑	setup_rising to CP	0.0577	0.0625	0.0738	0.0786
		C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P0	C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P4	C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P10	C8T28SOIDV_-LL_SDF-SYNCPRQX5_-P16
CP ↓	min_pulse_width to CP	0.1581	0.1839	0.2254	0.2647
CP ↑	min_pulse_width to CP	0.0858	0.0964	0.1137	0.1324
D ↓	hold_rising to CP	-0.0289	-0.0393	-0.0491	-0.0540
D ↑	hold_rising to CP	-0.0266	-0.0311	-0.0419	-0.0484
D ↓	setup_rising to CP	0.0834	0.0986	0.1148	0.1349
D ↑	setup_rising to CP	0.0563	0.0611	0.0686	0.0783
RN ↓	min_pulse_width to RN	0.0903	0.1023	0.1196	0.1365
RN ↑	recovery_rising to CP	0.0027	0.0031	0.0004	0.0004
RN ↑	removal_rising to CP	0.0021	0.0021	0.0047	0.0047
TE ↓	hold_rising to CP	-0.0268	-0.0317	-0.0437	-0.0486
TE ↑	hold_rising to CP	-0.0488	-0.0559	-0.0657	-0.0755

TE ↓	setup_rising to CP	0.0819	0.0907	0.1107	0.1270
TE ↑	setup_rising to CP	0.1479	0.1724	0.2087	0.2429
TI ↓	hold_rising to CP	-0.0879	-0.1082	-0.1339	-0.1492
TI ↑	hold_rising to CP	-0.0524	-0.0570	-0.0683	-0.0794
TI ↓	setup_rising to CP	0.1479	0.1680	0.2034	0.2382
TI ↑	setup_rising to CP	0.0823	0.0868	0.0981	0.1134

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P0	5.517e-05	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P4	1.098e-05	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P10	2.481e-06	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPRQX5_P16	1.337e-06	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P0	5.438e-05	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P4	1.080e-05	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P10	2.465e-06	1.000e-20
C8T28SOIDV_LL_-SDFSYNCPRQX5_P16	1.361e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPRQX5_-P16
Clock 100Mhz Data 0Mhz	1.532e-02	1.547e-02	1.581e-02	1.622e-02
Clock 100Mhz Data 25Mhz	1.587e-02	1.592e-02	1.626e-02	1.670e-02
Clock 100Mhz Data 50Mhz	1.642e-02	1.636e-02	1.670e-02	1.718e-02
Clock = 0 Data 100Mhz	9.379e-03	9.312e-03	9.332e-03	9.419e-03
Clock = 1 Data 100Mhz	8.703e-05	8.202e-05	1.142e-04	1.578e-04
	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPRQX5_-P16
Clock 100Mhz Data 0Mhz	1.612e-02	1.614e-02	1.631e-02	1.658e-02
Clock 100Mhz Data 25Mhz	1.712e-02	1.707e-02	1.729e-02	1.767e-02

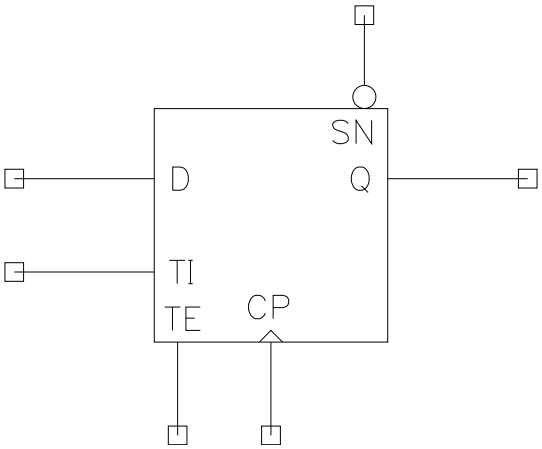
Clock 100Mhz Data 50Mhz	1.813e-02	1.799e-02	1.827e-02	1.875e-02
Clock = 0 Data 100Mhz	9.760e-03	9.896e-03	9.965e-03	1.004e-02
Clock = 1 Data 100Mhz	1.356e-04	1.203e-04	1.177e-04	1.210e-04

SDFSYNCPSQ

Cell Description

Metastable tolerant; Positive edge triggered Scan D flip-flop; with active low asynchronous Preset; having non-inverted output Q only

Logical Symbol



Cell size

Drive Strength	Height (um)	Width (um)	Area (um2)
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P0	1.600	4.080	6.5280
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P4	1.600	4.080	6.5280
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P10	1.600	4.080	6.5280
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P16	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P0	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P4	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P10	1.600	4.080	6.5280
C8T28SOIDV_LL_-SDFSYNCPSQX5_P16	1.600	4.080	6.5280

Truth Table

IQ	Q
IQ	IQ

D	CP	SN	TI	TE	IQ	IQ
-	-	0	-	-	-	1
D	/	1	-	0	-	D
-	/	1	TI	1	-	TI

-	-	1	-	-	IQ	IQ

Pin Capacitance

Pin	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16
CP	0.0006	0.0006	0.0006	0.0006
D	0.0006	0.0006	0.0007	0.0007
SN	0.0016	0.0015	0.0016	0.0017
TE	0.0009	0.0009	0.0010	0.0011
TI	0.0004	0.0004	0.0004	0.0004
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16
CP	0.0004	0.0004	0.0005	0.0005
D	0.0003	0.0003	0.0004	0.0004
SN	0.0014	0.0015	0.0016	0.0017
TE	0.0008	0.0008	0.0009	0.0010
TI	0.0003	0.0003	0.0004	0.0004

Propagation Delay at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Description	Intrinsic Delay (ns)		Kload (ns/pf)	
	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4**
CP to Q ↓	0.0820	0.0923	3.1948	3.4540
CP to Q ↑	0.0826	0.0935	3.9092	4.2825
SN to Q ↑	0.0885	0.0999	3.7439	4.1100
	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10**	**C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16**
CP to Q ↓	0.1077	0.1229	3.8382	4.1962
CP to Q ↑	0.1102	0.1258	4.8184	5.3170
SN to Q ↑	0.1175	0.1344	4.6145	5.0860
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4**
CP to Q ↓	0.1133	0.1277	3.3723	3.6827
CP to Q ↑	0.1295	0.1473	3.9762	4.3648
SN to Q ↑	0.0687	0.0778	3.8269	4.1891
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10**	**C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16**
CP to Q ↓	0.1495	0.1703	4.1328	4.5534
CP to Q ↑	0.1747	0.2018	4.9204	5.4276
SN to Q ↑	0.1028	0.1172	4.6190	5.0941

Timing Constraints (ns) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin	Constraint	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P0	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P4	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P10	C8T28SOIDV_-LL1_SDF-SYNCPSQX5_-P16
CP ↓	min_pulse_width to CP	0.0958	0.1116	0.1357	0.1602
CP ↑	min_pulse_width to CP	0.0688	0.0733	0.0873	0.0999
D ↓	hold_rising to CP	-0.0196	-0.0277	-0.0322	-0.0388
D ↑	hold_rising to CP	-0.0098	-0.0114	-0.0169	-0.0218
D ↓	setup_rising to CP	0.0543	0.0614	0.0765	0.0889
D ↑	setup_rising to CP	0.0342	0.0395	0.0469	0.0518
SN ↓	min_pulse_width to SN	0.0864	0.0962	0.1108	0.1255
SN ↑	recovery_rising to CP	-0.0088	-0.0066	-0.0060	-0.0056
SN ↑	removal_rising to CP	0.0282	0.0331	0.0381	0.0398
TE ↓	hold_rising to CP	-0.0192	-0.0241	-0.0312	-0.0415
TE ↑	hold_rising to CP	-0.0289	-0.0338	-0.0413	-0.0511
TE ↓	setup_rising to CP	0.0539	0.0636	0.0755	0.0885
TE ↑	setup_rising to CP	0.1307	0.1524	0.1838	0.2136
TI ↓	hold_rising to CP	-0.0925	-0.1085	-0.1345	-0.1587
TI ↑	hold_rising to CP	-0.0312	-0.0377	-0.0439	-0.0544
TI ↓	setup_rising to CP	0.1287	0.1482	0.1790	0.2090
TI ↑	setup_rising to CP	0.0569	0.0625	0.0737	0.0842
		C8T28SOIDV_-LL_SDFSYNCP-SQX5_P0	C8T28SOIDV_-LL_SDFSYNCP-SQX5_P4	C8T28SOIDV_-LL_SDFSYNCP-SQX5_P10	C8T28SOIDV_-LL_SDFSYNCP-SQX5_P16
CP ↓	min_pulse_width to CP	0.1635	0.1886	0.2319	0.2718
CP ↑	min_pulse_width to CP	0.0919	0.1046	0.1215	0.1371
D ↓	hold_rising to CP	-0.0338	-0.0387	-0.0540	-0.0605
D ↑	hold_rising to CP	-0.0257	-0.0337	-0.0435	-0.0484
D ↓	setup_rising to CP	0.0883	0.1034	0.1197	0.1398
D ↑	setup_rising to CP	0.0563	0.0611	0.0708	0.0783
SN ↓	min_pulse_width to SN	0.0903	0.1023	0.1218	0.1365
SN ↑	recovery_rising to CP	-0.0185	-0.0212	-0.0229	-0.0251
SN ↑	removal_rising to CP	0.0574	0.0673	0.0765	0.0895
TE ↓	hold_rising to CP	-0.0300	-0.0365	-0.0485	-0.0589
TE ↑	hold_rising to CP	-0.0484	-0.0554	-0.0706	-0.0804

TE ↓	setup_rising to CP	0.0858	0.0955	0.1182	0.1377
TE ↑	setup_rising to CP	0.1519	0.1763	0.2159	0.2527
TI ↓	hold_rising to CP	-0.0928	-0.1137	-0.1394	-0.1646
TI ↑	hold_rising to CP	-0.0524	-0.0621	-0.0732	-0.0830
TI ↓	setup_rising to CP	0.1518	0.1784	0.2125	0.2483
TI ↑	setup_rising to CP	0.0813	0.0920	0.1030	0.1185

Average Leakage Power (mW) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

	vdd	vdds
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P0	5.098e-05	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P4	1.058e-05	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P10	2.508e-06	1.000e-20
C8T28SOIDV_LL1_-SDFSYNCPSQX5_P16	1.389e-06	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P0	5.082e-05	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P4	1.041e-05	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P10	2.438e-06	1.000e-20
C8T28SOIDV_LL_SDFSYNCPSQX5_-P16	1.348e-06	1.000e-20

Internal Energy (uW/MHz) at 25C, 1.00V_0.00V_0.00V_0.00V, Typ process

Pin Cycle	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL1_-SDFSYNCPSQX5_-P16
Clock 100Mhz Data 0Mhz	1.427e-02	1.443e-02	1.469e-02	1.496e-02
Clock 100Mhz Data 25Mhz	1.527e-02	1.531e-02	1.556e-02	1.589e-02
Clock 100Mhz Data 50Mhz	1.628e-02	1.618e-02	1.643e-02	1.682e-02
Clock = 0 Data 100Mhz	8.901e-03	8.850e-03	8.884e-03	8.974e-03
Clock = 1 Data 100Mhz	9.298e-05	8.704e-05	9.042e-05	1.140e-04
	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P0	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P4	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P10	C8T28SOIDV_LL_-SDFSYNCPSQX5_-P16
Clock 100Mhz Data 0Mhz	1.511e-02	1.531e-02	1.557e-02	1.590e-02
Clock 100Mhz Data 25Mhz	1.663e-02	1.671e-02	1.697e-02	1.737e-02

Clock 100Mhz Data 50Mhz	1.816e-02	1.811e-02	1.838e-02	1.884e-02
Clock = 0 Data 100Mhz	9.599e-03	9.893e-03	1.005e-02	1.019e-02
Clock = 1 Data 100Mhz	1.005e-04	9.043e-05	8.476e-05	8.394e-05

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