Positive and Negative 1.8 V Dedicated supply IO library and ESD core clamp for substrate baising designed in 28 nm FDSOI technology

Overview

The library C28SOI_IO_EXT_ALLF_FBBRBB_SUBSTRATEBIAS_LR_EG is designed in 28 nm FDSOI technology. It contains cells for dedicated core supply and ESD core clamp for 1.8V positive and negative substrate biasing for logic.

Features

- Supports cells for Forward Back bias (FBB) and Reverse Back bias (RBB)
- Uses the standard process option and 28 Å gate oxide.
- Supports Compatible Standard Frame (CSF##) only
- Supports single row[1] configuration for IO ring
- FC (Flip-chip) and CL (Cluster) frames provided.

Product name contains ALLF due to legacy reasons although only CSF is supported

[1]Single row configuration is also called linear configuration.

Information Snapshot

Process Options

- GO1: SVT
- GO2: 28 Å

Packaging

- Flip-chip

Table 1 : Operating values

Symbol	Parameter	Min	Typ	Max	Unit
rbbfbb1v8neg bias	Negative power supply	-1.95	-1.8	0 (1)	V
rbbfbb1v8pos bias	Positive power supply	0	1.8	1.95	V
vdd	Supply voltage for 1.0 V node	0.6	1.0	1.1	V
vdde	Supply voltage for 1.8 V IO ring	1.65	1.8	1.95	V
$T_{junction}$	Operating junction temperature	- 40	25	125	°C

Notes:

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For more details about electrical specifications, please refer to *Section 3: Electrical Specifications*.

1. Quick References

	*The document uses the following convention to indicate logic levels:* *L indicates logic low.* *H indicates logic high.* *X indicates don't care state.* *Z indicates high impedance state.* *'-' (Hyphen) indicates 'No activity'.*

	** suffixed in library name indicates multiple metallization options.* *** suffixed in cell name indicates multiple packages / configurations.*

1.1 Metal Stacking Convention

The metallization option supported by this library can be referred from its product package. The following is the convention that can be used to decode the segment in the library name:

- 7 metal option (5U1X2T8XLB) known as 5002 refers as follows:
  - 5U1X refers to the first 5 levels with 1X pitch (thin) metal.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 8 metal option (6U1X2T8XLB) known as 6002 refers as follows:
  - 6U1X refers to the first 6 levels with 1X pitch (thin) metal in ultra-low-K.
  - 2T8X refers to 2 levels with 8X (thick) metal in oxide.
  - LB is the Alucap.

- 10 metal option (6U1X2U2X2T8XLB) known as 6202 refers as follows:
  - 6U1X refers to the first 6 levels with 1x pitch (thin) metal in ultra-low-K.
  - 2U2X refers to the next 2 levels with 2x pitch (thin) metal in ultra-low-K.
  - 2T8X refers to 2 levels with 8x (thick) metal in oxide.
  - LB is the Alucap.

1.2 Reference Documentation

For details on the following topics:

- Power Sequencing Recommendation in IOs
- Specifications and Analysis of Overshoots and Undershoots
- SSN Application Notes
- ESD qualification
- Latch-up qualification
- Maturity information
- RDL recommended rules
  - ST users, refer to the IO Reference catalog

    (http://ccds.st.com/cps/sections/library/io/io_reference_catalog/downloadFile/file/IO_Helpdesk_Solutions.pdf).
  - Non-ST users, contact Customer Support personnel

1.3 Reference Library

The C28SOI_IO_EXT_ALLF_FBBRBB_SUBSTRATEBIAS_LR_EG library refers to some cells from 28 nm FDSOI libraries listed below. For a correct usage, these libraries are mandatory:

- C28SOI_IO_ALLF_FRAMEKIT_EG
- C28SOI_IO_ALLF_IOSUPPLYKIT_EG

1.4 Acronyms and Abbreviations Used

Table 2 : Acronyms and Abbreviation

Acronym/Abbreviation	Description
B2B	Back-to-Back
CDM	Charge Device Model
DC	Direct Current
DRM	Design Rule Manual
ESD	Electrostatic Discharge
HBM	Human Body Model
FC	Flip-chip
CL	Cluster
MM	Machine Model
RMS	Root Mean Square
SVT	Standard V_T
2ROWS	Two rows

2. Functional Specifications

The C28SOI_IO_EXT_ALLF_CORESUPPLY_EG library includes 65 cells.

Table 3 : Cell List

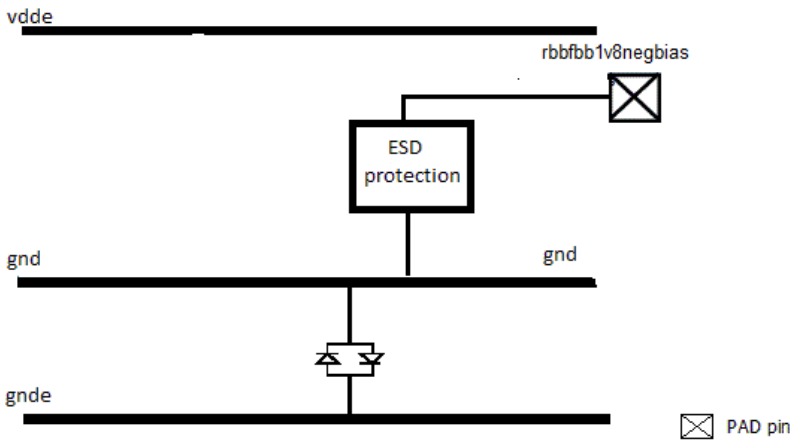
Cell Name	Width x Height (µm)	Cell Description
IO_NMOSBIAS_EXT_1V8_NEG_CSF_CL_LIN	40 x 106.3	Dedicated Negative 1.8V power supply referring to gnd ground node for NMOS biasing
IO_NMOSBIAS_EXT_1V8_NEG_CSF_FC_LIN	40 x 90.8	
IO_NMOSBIAS_EXT_1V8_POS_CSF_CL_LIN	40 x 106.3	Dedicated Positive 1.8V power supply referring to gnd ground node for NMOS biasing
IO_NMOSBIAS_EXT_1V8_POS_CSF_FC_LIN	40 x 90.8	
IO_PMOSBIAS_EXT_1V8_NEG_CSF_CL_LIN	40 x 106.3	Dedicated Negative 1.8V power supply referring to gnd ground node for PMOS biasing
IO_PMOSBIAS_EXT_1V8_NEG_CSF_FC_LIN	40 x 90.8	
IO_PMOSBIAS_EXT_1V8_POS_CSF_CL_LIN	40 x 106.3	Dedicated Positive 1.8V power supply referring to gnd ground node for PMOS biasing
IO_PMOSBIAS_EXT_1V8_POS_CSF_FC_LIN	40 x 90.8	
NMOSBIAS_EXT_NEGESDCLAMP_NOB2B_1V8	74.991 x 54.41	Core cell including negative 1.8 V ESD clamp for NMOS biasing with no B2B
NMOSBIAS_EXT_POSESDCLAMP_NOB2B_1V8	74.991 x 54.41	Core cell including positive 1.8 V ESD clamp for NMOS biasing with no B2B
PMOSBIAS_EXT_NEGESDCLAMP_NOB2B_1V8	74.991 x 54.41	Core cell including negative 1.8 V ESD clamp for PMOS biasing with no B2B
PMOSBIAS_EXT_POSESDCLAMP_NOB2B_1V8	74.991 x 54.41	Core cell including positive 1.8 V ESD clamp for PMOS biasing with no B2B
NMOSBIAS_EXT_NEGESDCLAMP_WITH_B2B_1V8	83.921 x 54.41	Core cell including negative 1.8 V ESD clamp for NMOS biasing with B2B
NMOSBIAS_EXT_POSESDCLAMP_WITH _B2B_1V8	83.921 x 54.41	Core cell including positive 1.8 V ESD clamp for NMOS biasing with B2B
PMOSBIAS_EXT_NEGESDCLAMP_WITH _B2B_1V8	83.921 x 54.41	Core cell including negative 1.8 V ESD clamp for PMOS biasing with B2B
PMOSBIAS_EXT_POSESDCLAMP_WITH _B2B_1V8	83.921 x 54.41	Core cell including positive 1.8 V ESD clamp for PMOS biasing with B2B

The ALLCELLS cells are not considered part of the Deliverable. These cells are specifically for QA check and hence subject to change, without prior notice.

2.1 IO_NMOSBIAS_EXT_1V8_NEG_CSF_CL_LIN /FC_LIN

2.1.1 Functional Diagram

Figure 1 : Block diagram



2.1.2 Interface Description

Table 4 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
rbbfbb1v8negbias	Input / Output	-1.95 V to 0V	Dedicated negative 1V8 power node for NMOS biasing , pad side
Track and core pins			
rbbfbb1v8negbias	Input / Output	-1.95 V to 0V	Dedicated negative 1V8 power node for NMOS biasing, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.1.3 Cell Information

Table 5 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8negbias node)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C ((rbbfbb1v8negbias node)	-	-	2.5	µA
I_{DC}	DC current Pad To Core [1]	110 °C (8 (rbbfbb1v8negbias node)	-	-	110	mA
		125 °C (rbbfbb1v8negbias node)	-	-	40	
	DC current Pad To Core [2]	110 °C (rbbfbb1v8negbias node)	-	-	38	
		125 °C ((rbbfbb1v8negbias node)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (rbbfbb1v8negbias node)	-	-	167	mA
	RMS current Pad To Core [2]	100 °C (rbbfbb1v8negbias node)	-	-	103	

[1] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[2] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

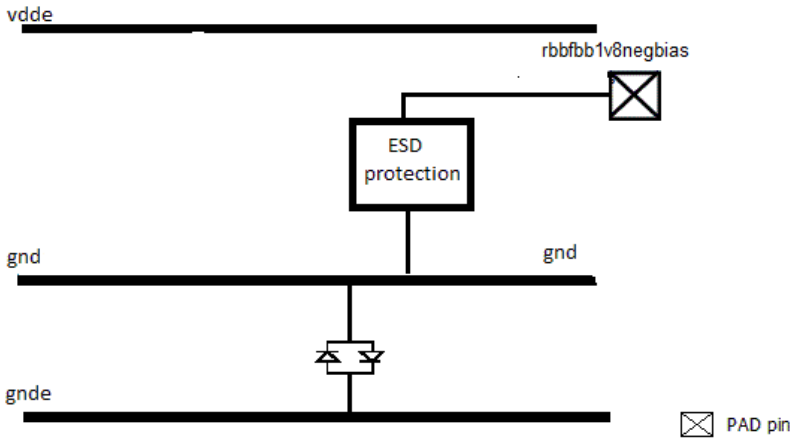
2.1.4 Functional Description

The cell IO_NMOSBIAS_EXT_1V8_NEG_CSF_CL_LIN /FC_LIN can be used to bias negative voltage to NMOS of logic blocks in order to operate them in FBB/RBB mode. This cell is to be placed in the IO Ring section.

2.2 IO_PMOSBIAS_EXT_1V8_NEG_CSF_CL_LIN /FC_LIN

2.2.1 Functional Diagram

Figure 2 : Block diagram



2.2.2 Interface Description

Table 6 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
rbbfbb1v8negbias	Input / Output	-1.95 V to 0V	Dedicated negative 1V8 power node for PMOS biasing , pad side
Track and core pins			
rbbfbb1v8negbias	Input / Output	-1.95 V to 0V	Dedicated negative 1V8 power node for PMOS biasing, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.2.3 Cell Information

Table 7 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8negbias node)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C ((rbbfbb1v8negbias node)	-	-	2.5	µA
I_{DC}	DC current Pad To Core [1]	110 °C (8 (rbbfbb1v8negbias node)	-	-	110	mA
		125 °C (rbbfbb1v8negbias node)	-	-	40	
	DC current Pad To Core [2]	110 °C (rbbfbb1v8negbias node)	-	-	38	
		125 °C ((rbbfbb1v8negbias node)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (rbbfbb1v8negbias node)	-	-	167	mA
	RMS current Pad To Core [2]	100 °C (rbbfbb1v8negbias node)	-	-	103	

[3] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[4] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

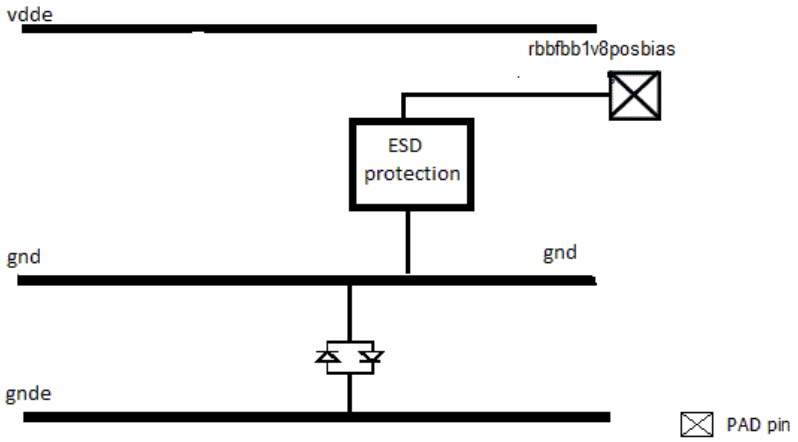
2.2.4 Functional Description

The cell IO_PMOSBIAS_EXT_1V8_NEG_CSF_CL_LIN /FC_LIN can be used to bias negative voltage to PMOS of logic blocks in order to operate them in FBB/RBB mode. This cell is to be placed in the IO Ring section.

2.3 IO_NMOSBIAS_EXT_1V8_POS_CSF_CL_LIN /FC_LIN

2.3.1 Functional Diagram

Figure 3 : Block diagram



2.3.2 Interface Description

Table 8 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
rbbfbb1v8posbias	Input / Output	-1.95 V to 0V	Dedicated positive 1V8 power node for NMOS biasing , pad side
Track and core pins			
rbbfbb1v8posbias	Input / Output	-1.95 V to 0V	Dedicated positive 1V8 power node for NMOS biasing, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.3.3 Cell Information

Table 9 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8posbias node)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C ((rbbfbb1v8posbias node)	-	-	2.5	µA
I_{DC}	DC current Pad To Core [1]	110 °C (8 (rbbfbb1v8posbias node)	-	-	110	mA
		125 °C (rbbfbb1v8posbias node)	-	-	40	
	DC current Pad To Core [2]	110 °C (rbbfbb1v8posbias node)	-	-	38	
		125 °C ((rbbfbb1v8posbias node)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (rbbfbb1v8posbias node)	-	-	167	mA
	RMS current Pad To Core [2]	100 °C (rbbfbb1v8posbias node)	-	-	103	

[5] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[6] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

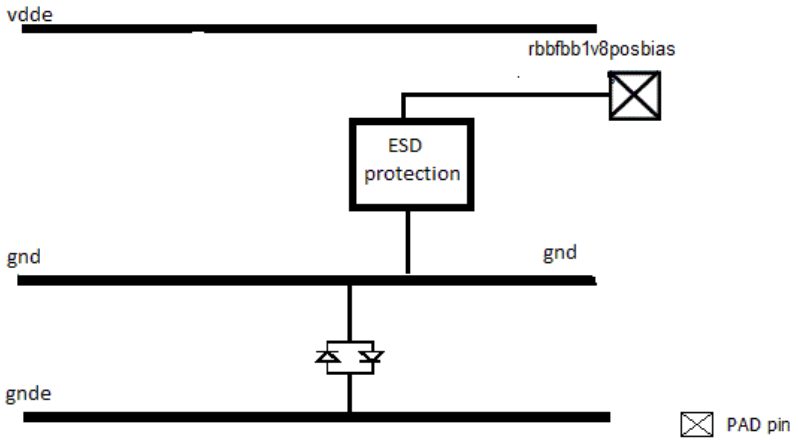
2.3.4 Functional Description

The cell IO_NMOSBIAS_EXT_1V8_POS_CSF_CL_LIN /FC_LIN can be used to bias positive voltage to NMOS of logic blocks in order to operate them in FBB/RBB mode. This cell is to be placed in the IO Ring section.

2.4 IO_PMOSBIAS_EXT_1V8_POS_CSF_CL_LIN /FC_LIN

2.4.1 Functional Diagram

Figure 4 : Block diagram



2.4.2 Interface Description

Table 10 : Pin description

Pin	Type	Voltage Level (V)	Description
Pad pins			
rbbfbb1v8posbias	Input / Output	-1.95 V to 0V	Dedicated positive 1V8 power node for PMOS biasing , pad side
Track and core pins			
rbbfbb1v8posbias	Input / Output	-1.95 V to 0V	Dedicated positive 1V8 power node for PMOS biasing, only core side
vdde	Input / Output	vdde	IO power node (1.8 V), only track side
gnde	Input / Output	0	IO ground node, only track side
gnd	Input / Output	0	Core and substrate ground node

2.4.3 Cell Information

Table 11 : Cell information

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8posbias node)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C ((rbbfbb1v8posbias node)	-	-	2.5	µA
I_{DC}	DC current Pad To Core [1]	110 °C (8 (rbbfbb1v8posbias node)	-	-	110	mA
		125 °C (rbbfbb1v8posbias node)	-	-	40	
	DC current Pad To Core [2]	110 °C (rbbfbb1v8posbias node)	-	-	38	
		125 °C ((rbbfbb1v8posbias node)	-	-	22	
I_{RMS}	RMS current Pad To Core [1]	100 °C (rbbfbb1v8posbias node)	-	-	167	mA
	RMS current Pad To Core [2]	100 °C (rbbfbb1v8posbias node)	-	-	103	

[7] Taking into account only RMS/DC current capability of the IO cell without RDL and BUMP constraints.

[8] Considering minimum RDL width to BUMP, that is, same width as the LB width in IO cell.

DC and RMS current information do not take into account RDL constraints which are dependent upon chip design, except for case [2].
DC/RMS current values of RDL should be checked accordingly at chip level.

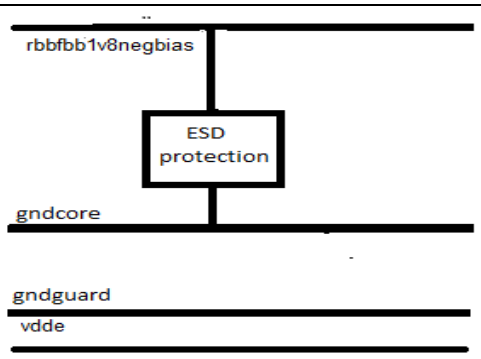
2.4.4 Functional Description

The cell IO_PMOSBIAS_EXT_1V8_POS_CSF_CL_LIN /FC_LIN can be used to bias positive voltage to PMOS of logic blocks in order to operate them in FBB/RBB mode. This cell is to be placed in the IO Ring section.

2.5 NMOSBIAS_EXT_NEGESDCLAMP_NOB2B_1V8

2.5.1 Functional Diagram

Figure 5 : Block diagram



2.5.2 Interface Description

Table 12 : Pin description

Pin	Type	Voltage Level (V)	Description
rbbfbb1v8negbias	Input / Output	-1.95 V to 0 Volts	Dedicated 1V8 negative power node for bulk biasing for NMOS of logic block
vdde	Input/Output	vdde	Deep Nwell guard ring biasing (1.8V)
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.5.3 Cell Information

Table 13 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8negbias)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C (rbbfbb1v8negbias node)	-	-	2.5	µA

2.5.4 Functional Description

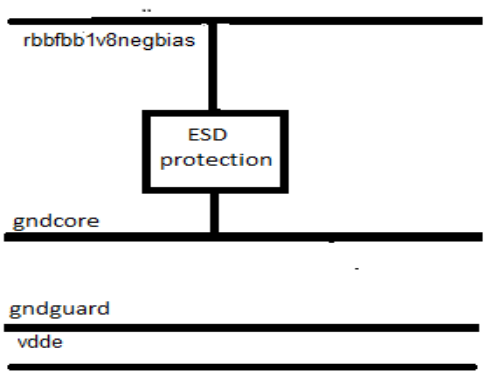
The cell is a core block that protects devices plugged between rbbfbb1v8negbias and gndcore for NMOS biasing of core logic. Pins are provided in metal 5.

As mentioned by cell name, there is no back to back diode between gndcore and gndguard . B2B diodes from C28SOI_IO_EXT_ALLF_CORESUPPLY_EG need to be added at core side between gndcore and gndgurad.

2.6 PMOSBIAS_EXT_NEGESDCLAMP_NOB2B_1V8

2.6.1 Functional Diagram

Figure 6 : Block diagram



2.6.2 Interface Description

Table 14 : Pin description

Pin	Type	Voltage Level (V)	Description
rbbfbb1v8negbias	Input / Output	-1.95 V to 0 Volts	Dedicated 1V8 negative power node for bulk biasing for PMOS of logic block
vdde	Input/Output	vdde	Deep Nwell guard ring biasing (1.8V)
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.6.3 Cell Information

Table 15 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8negbias)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C (rbbfbb1v8negbias node)	-	-	2.5	µA

2.6.4 Functional Description

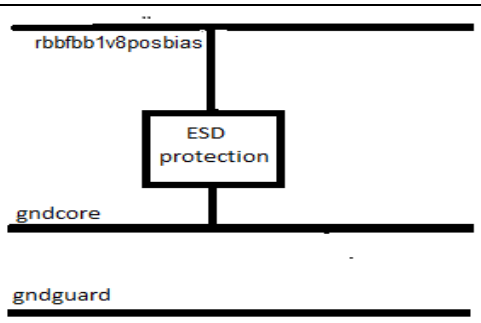
The cell is a core block that protects devices plugged between rbbfbb1v8negbias and gndcore for PMOS biasing of core logic. Pins are provided in metal 5.

As mentioned by cell name, there is no back to back diode between gndcore and gndguard. B2B diodes from C28SOI_IO_EXT_ALLF_CORESUPPLY_EG need to be added at core side between gndcore and gndgurad.

2.7 NMOSBIAS_EXT_POSESDCLAMP_NOB2B_1V8

2.7.1 Functional Diagram

Figure 7 : Block diagram



2.7.2 Interface Description

Table 16 : Pin description

Pin	Type	Voltage Level (V)	Description
rbbfbb1v8posbias	Input / Output	-1.95 V to 0 Volts	Dedicated 1V8 positive power node for bulk biasing for NMOS of logic block
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.7.3 Cell Information

Table 17 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8posbias)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C (rbbfbb1v8posbias node)	-	-	2.5	µA

2.7.4 Functional Description

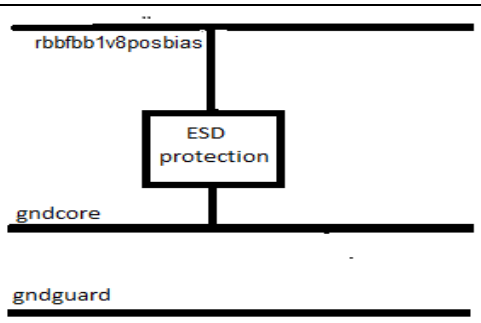
The cell is a core block that protects devices plugged between rbbfbb1v8posbias and gndcore for NMOS biasing of core logic. Pins are provided in metal 5.

As mentioned by cell name, there is no back to back diode between gndcore and gndguard. B2B diodes from C28SOI_IO_EXT_ALLF_CORESUPPLY_EG need to be added at core side between gndcore and gndgurad.

2.8 PMOSBIAS_EXT_POSESDCLAMP_NOB2B_1V8

2.8.1 Functional Diagram

Figure 8 : Block diagram



2.8.2 Interface Description

Table 18 : Pin description

Pin	Type	Voltage Level (V)	Description
rbbfbb1v8posbias	Input / Output	-1.95 V to 0 Volts	Dedicated 1V8 positive power node for bulk biasing for PMOS of logic block
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.8.3 Cell Information

Table 19 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8posbias)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C (rbbfbb1v8posbias node)	-	-	2.5	µA

2.8.4 Functional Description

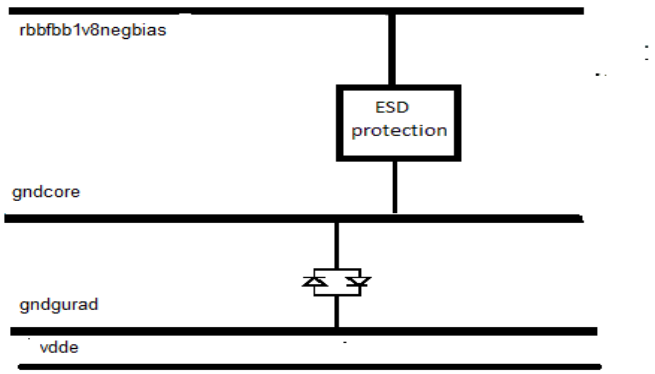
The cell is a core block that protects devices plugged between rbbfbb1v8posbias and gndcore for PMOS biasing of core logic. Pins are provided in metal 5.

As mentioned by cell name, there is no back to back diode between gndcore and gndguard. B2B diodes from C28SOI_IO_EXT_ALLF_CORESUPPLY_EG need to be added at core side between gndcore and gndgurad.

2.9 NMOSBIAS_EXT_NEGESDCLAMP_WITH_B2B_1V8

2.9.1 Functional Diagram

Figure 9 : Block diagram



2.9.2 . Interface Description

Table 20 : Pin description

Pin	Type	Voltage Level (V)	Description
rbbfbb1v8negbias	Input / Output	-1.95 V to 0 Volts	Dedicated 1V8 negative power node for bulk biasing for NMOS of logic block
vdde	Input/Output	vdde	Deep Nwell guard ring biasing (1.8V)
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.9.3 Cell Information

Table 21 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8negbias)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C (rbbfbb1v8negbias node)	-	-	2.5	µA

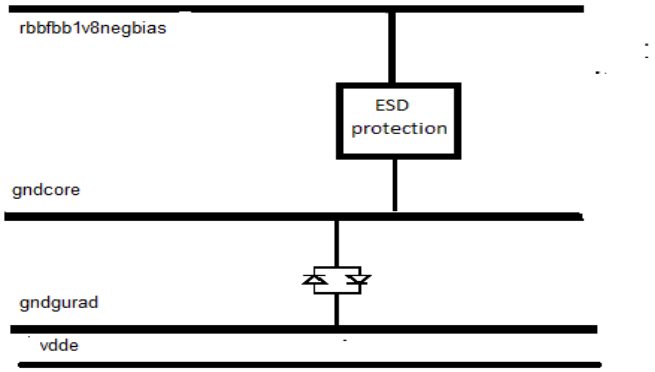
2.9.4 Functional Description

The cell is a core block that protects devices plugged between rbbfbb1v8negbias and gndcore for NMOS biasing of core logic. It also contains back to back diodes between gndcore and gndguard . Pins are provided in metal 5.

2.10 PMOSBIAS_EXT_NEGESDCLAMP_WITH_B2B_1V8

2.10.1 Functional Diagram

Figure 10 : Block diagram



2.10.2 . Interface Description

Table 22 : Pin description

Pin	Type	Voltage Level (V)	Description
rbbfbb1v8negbias	Input / Output	-1.95 V to 0 Volts	Dedicated 1V8 negative power node for bulk biasing for PMOS of logic block
vdde	Input/Output	vdde	Deep Nwell guard ring biasing (1.8V)
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.10.3 Cell Information

Table 23 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8negbias)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C (rbbfbb1v8negbias node)	-	-	2.5	µA

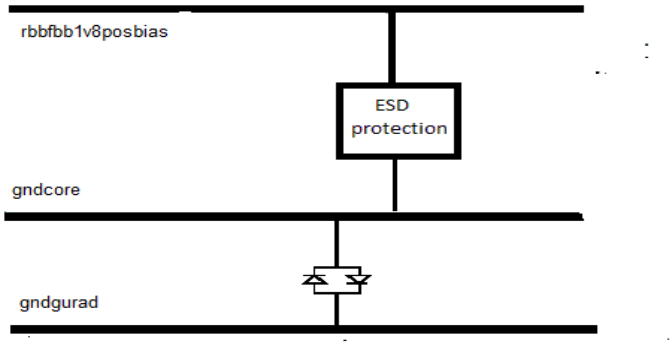
2.10.4 Functional Description

The cell is a core block that protects devices plugged between rbbfbb1v8negbias and gndcore for PMOS biasing of core logic. It also contains back to back diodes between gndcore and gndguard . Pins are provided in metal 5.

2.11 NMOSBIAS_EXT_POSESDCLAMP_WITH_B2B_1V8

2.11.1 Functional Diagram

Figure 11 : Block diagram



2.11.2 . Interface Description

Table 24 : Pin description

Pin	Type	Voltage Level (V)	Description
rbbfbb1v8posbias	Input / Output	-1.95 V to 0 Volts	Dedicated 1V8 positive power node for bulk biasing for NMOS of logic block
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.11.3 Cell Information

Table 25 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8posbias)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C (rbbfbb1v8posbias node)	-	-	2.5	µA

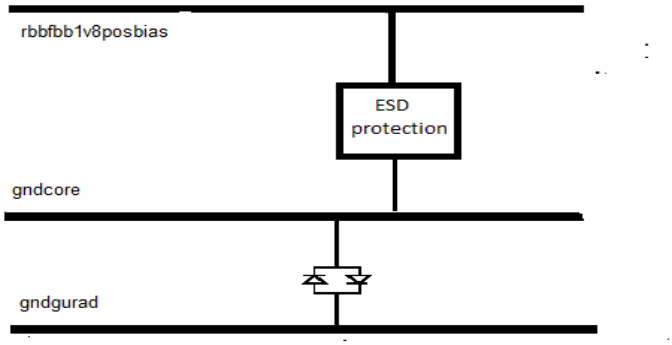
2.11.4 Functional Description

The cell is a core block that protects devices plugged between rbbfbb1v8posbias and gndcore for NMOS biasing of core logic. It also contains back to back diodes between gndcore and gndguard. Pins are provided in metal 5.

2.12 PMOSBIAS_EXT_POSESDCLAMP_WITH_B2B_1V8

2.12.1 Functional Diagram

Figure 12 : Block diagram



2.12.2 . Interface Description

Table 26 : Pin description

Pin	Type	Voltage Level (V)	Description
rbbfbb1v8posbias	Input / Output	-1.95 V to 0 Volts	Dedicated 1V8 positive power node for bulk biasing for PMOS of logic block
gndcore	Input / Output	0	Dedicated ground node
gndguard	Input / Output	0	Core and substrate ground node

2.12.3 Cell Information

Table 27 : Cell information

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$I_{leakage}$	Leakage current	Fast Process, Max voltage, 25 °C (rbbfbb1v8posbias)	-	-	0.40	µA
		Fast Process, Max voltage, 125 °C (rbbfbb1v8posbias node)	-	-	2.5	µA

2.12.4 Functional Description

The cell is a core block that protects devices plugged between rbbfbb1v8posbias and gndcore for PMOS biasing of core logic. It also contains back to back diodes between gndcore and gndguard. Pins are provided in metal 5.

3. Electrical Specifications

3.1 ESD and Latch-up Characteristics

Table 28 : ESD and Latch-up Characteristics

Symbol	Parameter	Condition	Target	Unit
V_{ESD}	Electrostatic discharge voltage	Human Body Model (HBM) [1]	2000	V
		Machine Model (MM) [1]	100	V
		Charge Device Model (CDM)	500V JEDEC	V
	Over-voltage stress		1.5* rbbfbb1v8posbias/ 1.5*rbbfbb1v8negbias	V

[1] ESD qualification: According to electrostatic discharge sensitivity measurement
[2] Latch-up qualification: According to latch-up sensitivity measurement.

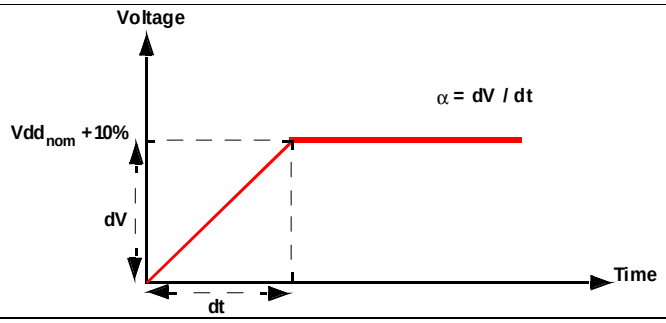
The level of CDM current seen at a given pre-charge voltage varies significantly with the chip size and package type. For instance, larger dies/packages generates higher CDM current.

However, this package size dependence has been considered during IO qualification, so that the above CDM commitment remains valid for any die/package size (even for large die/package sizes of hundreds of mm^2).

3.2 ESD Clamps Power-up Sensitivity

For correct power-up sequence without parasitic clamp switch-on, it is necessary to limit the power rise time as per next table.

Figure 13 : ESD Clamp Power-up Sensitivity



	Power Ramp-Up should be equal or slower than 0.5V/us.

4. Usage Guidelines

4.1 Design Requirements

Libraries given by the table below are required to be used with this library.

Table 29 : Mandatory Libraries

Library Name	Description
C28SOI_IO_EXT_CSF_BASIC_EG*	Contains supply, corner and place and route cells needed for a CSF IO ring construction

The C28SOI_IO_EXT_ALLF_FBBRBB_SUBSTRATEBIAS_LR_EG library supports the construction of an IO ring in various configurations and for various applications. The mandatory libraries required for developing the IO ring using the IO cells from this library are listed in the following table:.

Table 30 : Mandatory Cells

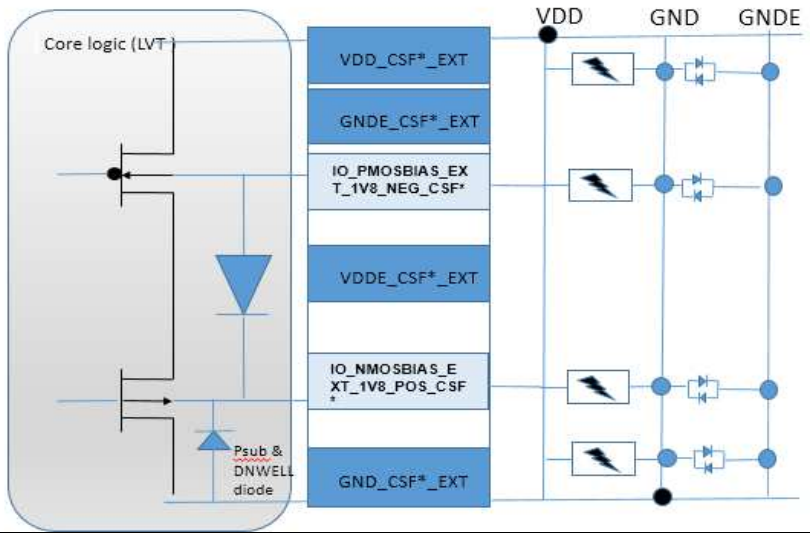
Library name	Cell Name	Cell Type	
C28SOI_IO_EXT_CSF_BASIC_EG*	VDDE_EXT_CSF_FC_LIN GNDE_EXT_CSF_FC_LIN VDD_EXT_CSF_FC_LIN GND_EXT_CSF_FC_LIN	Supply cell	Contains ESD protection cells, supply cells, corner cells, and place and route cells.
C28SOI_IO_ALLF_FRAMEKIT_EG*			Contains leaf cells used by all other libraries, specially
C28SOI_IO_ALLF_IOSUPPLYKIT_EG	*		Contains ESD protection cells, supply cells, corner cells, and place and route cells.
C28SOI_IO_EXT_ALLF_CORESUPPLY_EG*			Contains power and ground supply cells for core logic.

4.2 Cell usage for Different FBB/RBB modes

This section gives an overview on usage of cells to connect to bulk biasing of NMOS/PMOS of LVT/RVT buffer in order to be configured them in FBB/RBB modes.

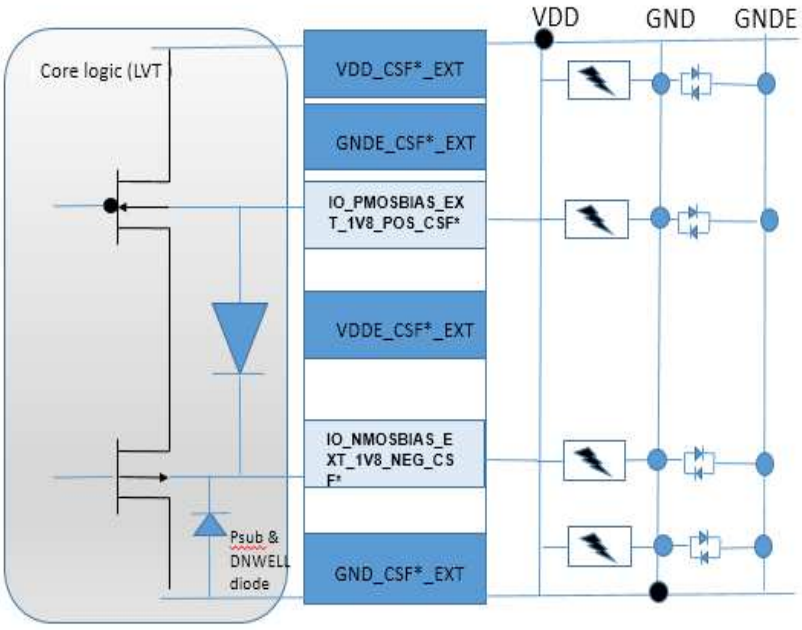
4.2.1 LVT buffer configured in FBB mode (For VDD_CSF*/GND_CSF* connected logic)

Figure 1 : IO usage : LVT Buffer configured in FBB mode



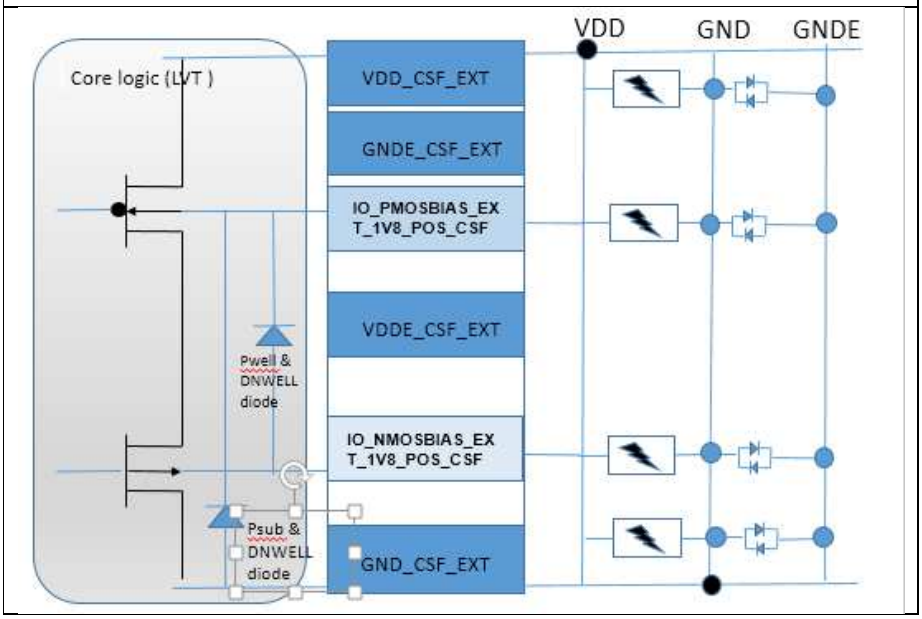
4.2.2 LVT buffer configured in RBB mode (For VDD_CSF*/GND_CSF* connected logic)

Figure 2 : IO usage : LVT Buffer configured in RBB mode



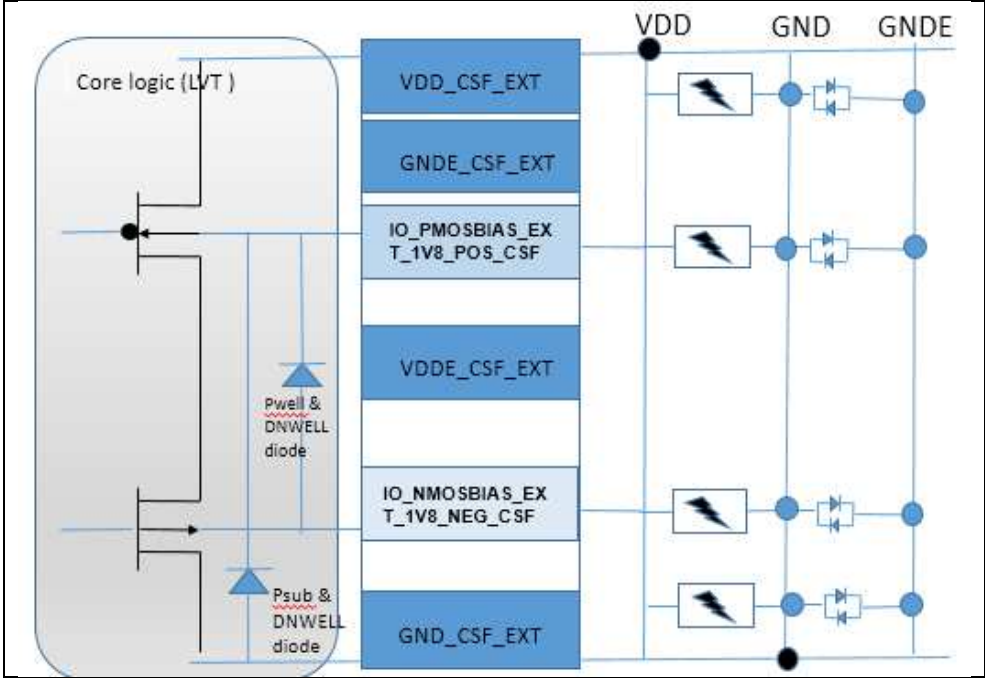
4.2.3 RVT buffer configured in FBB mode (For VDD_CSF*/GND_CSF* connected logic)

Figure 3 : IO usage : RVT Buffer configured in FBB mode



4.2.4 RVT buffer configured in RBB mode (For VDD_CSF*/GND_CSF* connected logic)

Figure 4 : IO usage : RVT Buffer configured in RBB mode



4.3 IO placement guidelines

4.3.1 IO cells can be used for logic connected to following supply cells

- **VDD_EXT_CSF ***
- **VDDCORE_GND_EXT_CSF***

Figure 1 : IO usage : LVT Buffer configured in FBB mode (For VDD_CSF*)

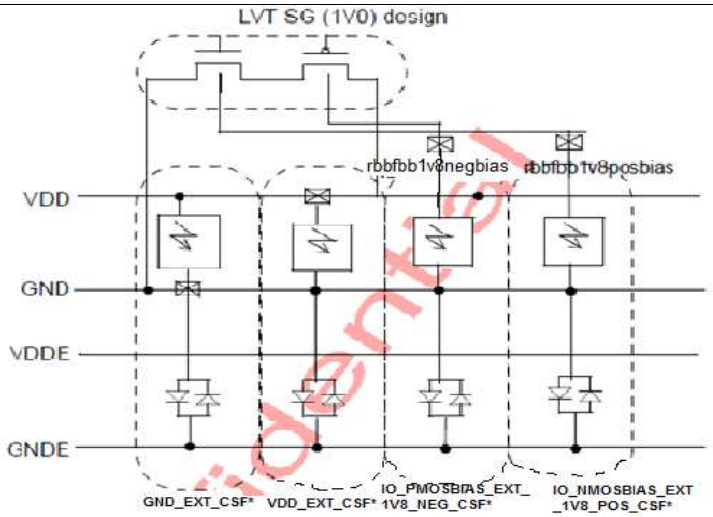
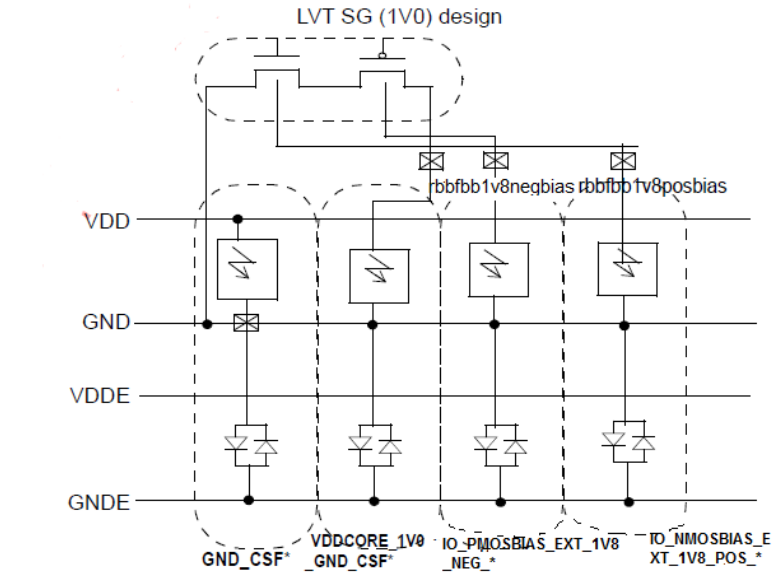


Figure 1 : IO usage : LVT Buffer configured in FBB mode (For VDDCORE_1V8_GND_CSF*)



4.3.2 IO cells are not allowed for logic connected to following supply cells:

- VDDCORE_GNDE_EXT_CSF *
- VDDCORE_GNDCORE_EXT_CSF*

Figure 1 : IO usage : LVT Buffer configured in FBB mode
(For VDDCORE_1V0_GNDE_CSF* - FORBIDDEN CONFIGURATION)

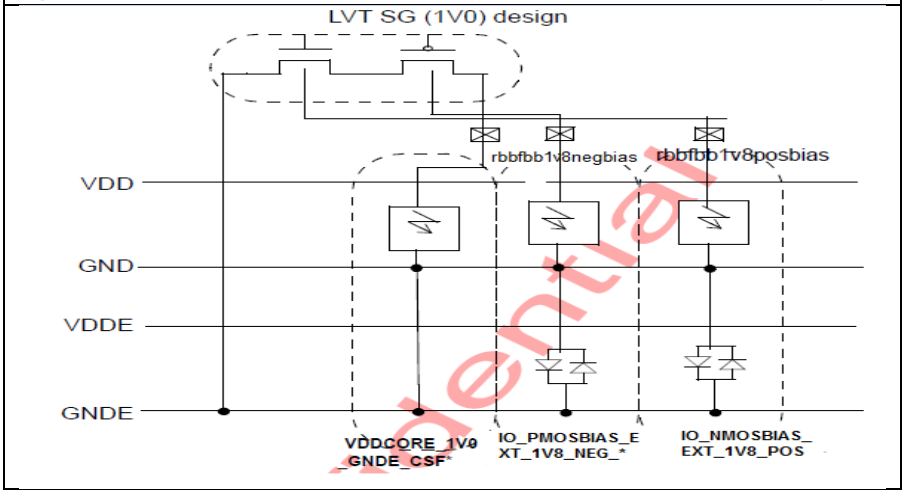
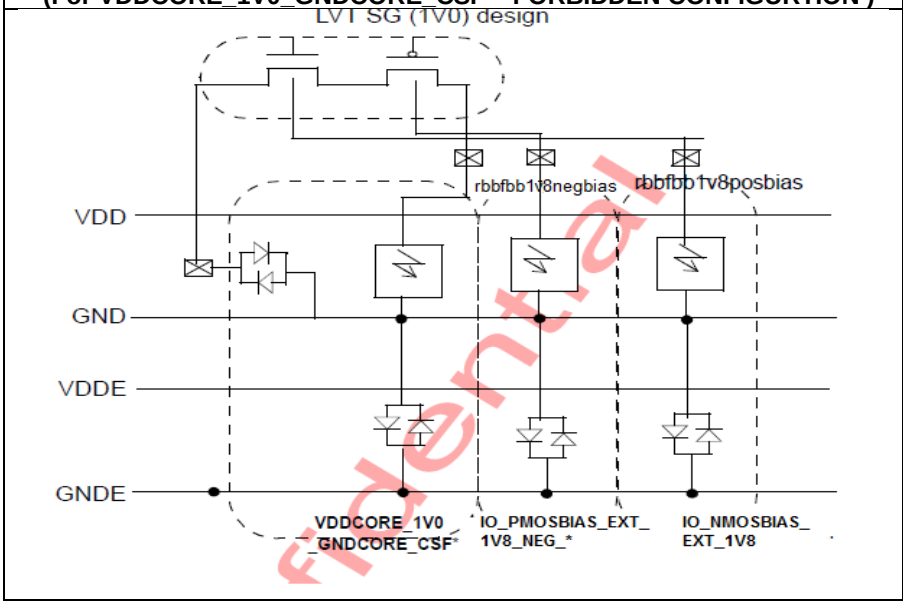


Figure 1 : IO usage : LVT Buffer configured in FBB mode
(For VDDCORE_1V0_GNDCORE_CSF – FORBIDDEN CONFIGURTION)



For these configuration, CORE clamps available in libraries can be used as mentioned in next section.

4.3.3 ESD CORE CLMPS cells can be used for logic connected to following supply cells:

- **VDDCORE_GNDE_EXT_CSF ***
- **VDDCORE_GNDCORE_EXT_CSF***

Figure 2 : IO usage : LVT Buffer configured in FBB mode

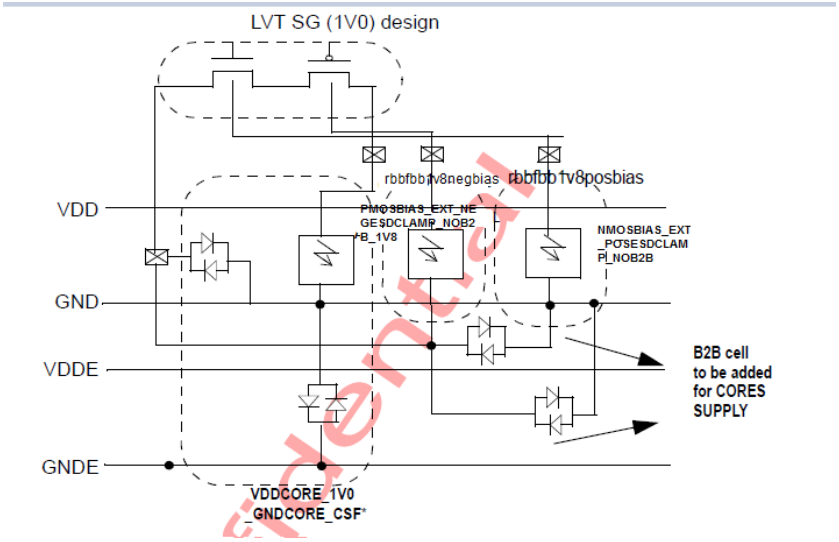
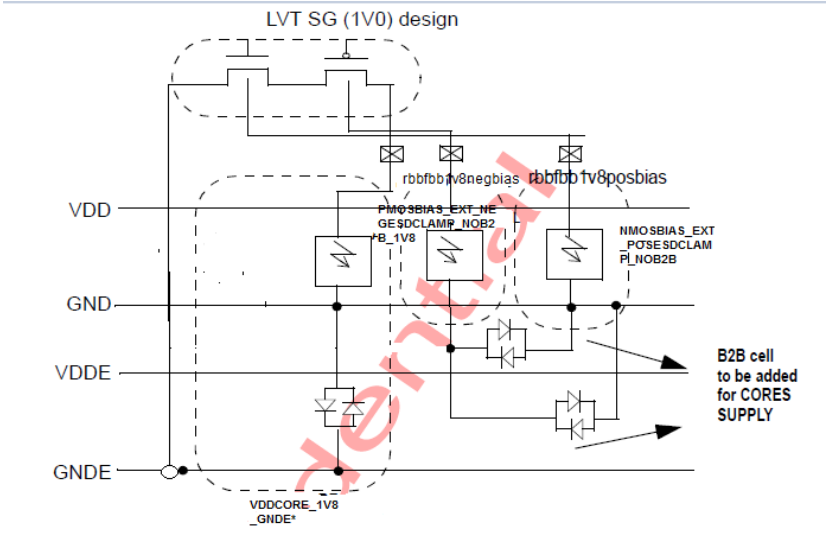


Figure 3 : IO usage : LVT Buffer configured in FBB mode



For above configuration, PMOSBIAS_EXT_NEGESDCLAMP_WITH_B2B2/ NMOSBIAS_EXT_POSEXTCLAMP_WITH B2B2 can also be used, in this case, no additional B2B2 need to be added as B2B between gndcore and gndgurad are already implemented in these cells.

4.3.4 General guidelines

- The IO_NMOS/PMOSBIAS_EXT_1V8_NEG_CSF_CL_LIN cell requires a power-up sequence. vdde is powered first, followed by rbbfbb1v8negbias.
- NMOS/PMOSBIAS_EXT_NEG_ESDCLAMP_* LIN cell requires a power-up sequence. vdde is powered first, followed by rbbfbb1v8negbias.

.

4.3.5 Guidelines for placement for IO_N/PMOSBIAS_EXT_1V8_NEG/POS_CSF* in IO ring

- IO cells can be used for logic connected to following supply cells
  - VDD_EXT_CSF *
  - VDDCORE_GND_EXT_CSF*
- IO cells are not allowed for logic connected to following supply cells, these configurations are forbidden.
  - VDDCORE_GNDE_EXT_CSF *
  - VDDCORE_GNDCORE_EXT_CSF*
- The maximum distance between IO cells and GND_CSF* clamp is 400 um

4.3.6 Guidelines for placement for core ESD clamps

- BUMP to NMOS/PMOSBIAS_EXT_POS/NEGESDCLAMP* core pin and LB routing should have resistance less than 0.5 and should be at least 3 µm wide.
- Back-to-Back diodes need to be placed between common ground substrate and ground (GNDCORE) of the clamp cell *_NOB2B* cells

5. Contact Information

ST users, login to **HELPDESK**. (http://col2.cro.st.com/helpdesk) for submitting queries or support requests.

Non-ST users, contact Customer Support personnel.

Appendix A: Cell Naming Convention

Table 31 : Naming Convention for Core Supply Cells

Segment Name	Description
Cell type	– IO : IO cell
1st suffix	– NMOS : For NMOS bulk biasing – PMOS : For PMOS bulk biasing
2nd suffix	- EXT : For external
3rd suffix	-1V8 : 1V8 supply range
4th suffix	- POS : Positive supply - NEG : Negative supply
5nd suffix	: – CSF: refers to compatible standard frame.
6rd suffix	Refers to the layout view of cell. It can have any of the following values: – FC: represents flip-chip configuration. – CL: represents cluster configuration.
7th suffix	Refers to the layout view of cell. It can have any of the following values: – LIN: represents single row configuration.

Appendix B: Document Revision History

Table 32 : Document Revision History

Date	Document Version	Comments
04-July-2017	1.0	• First release

Please Read Carefully: