Layout Finishing and SoC Tiling:
Embedded Metrology (eMetro) tiling

December 12th, 2012

CMOS and derivative PDK

life.augmented

Program Management & Services / Process Design Kit

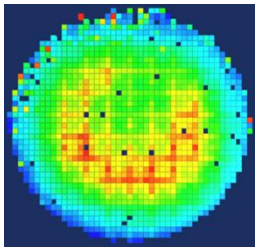
What is Embedded Metrology ?

- Formerly, structures for process monitoring were added in the scribe lines among chips
- Chips are bigger, lines are thinner:
  - ➔ Intrafield variability inside chip (proximity effect / circuit density etc…)
  - ➔ Intrafield variability chip to chip (Mask manufacturing uniformity, mask process on litho tools)
  - ➔ Intrawafer variability (different mask exposure, spatial uniformity of process chamber etc…)
  - ➔ wafer to wafer variability (inside one tool different process chambers can be used)
  - ➔ lot to lot process variability (drift over time / different tools used)

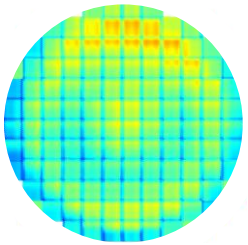
=> Similar structures must now also be added inside chips

- eMetro allow Advance Process Control (APC) to minimize standard variation on
  - •Critical Dimensions (CD)
  - •overlay
- The DoseMapper is one of the tool enabling this method

Some yield loss signature in 40nm...
Advanced CD control :



standard



with DoseMapper

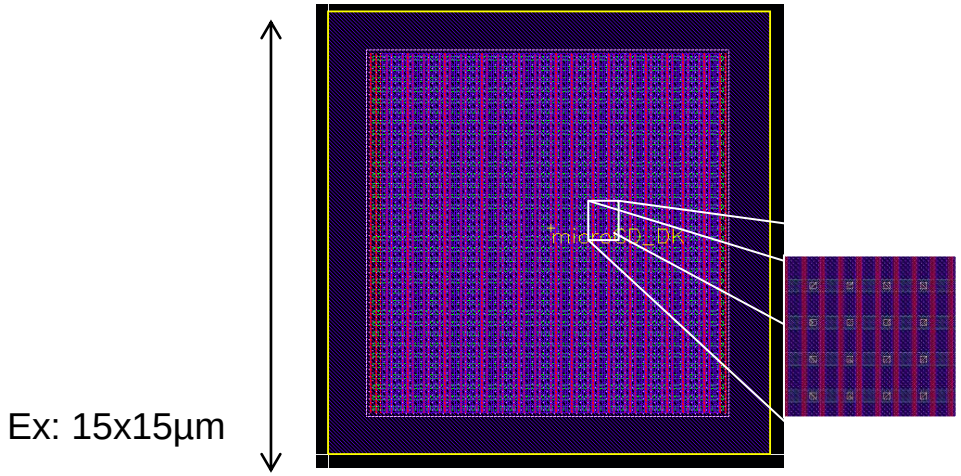
eMetro criticity

- **eMetro dramatically increase yield**
  by allowing an accurate process monitoring
  leading to an important CDs standard variation minimization

- eMetro to be placed **as early as possible** in the design-phase

About eMetro structures

- their instantiation can be enabled in the tiler GUI
- they can be flipped and rotated
- they may be swapped by more efficient ones at CAD2MASK level
- they are used from 40nm node
- they can use FE or BE layers (from 32nm)



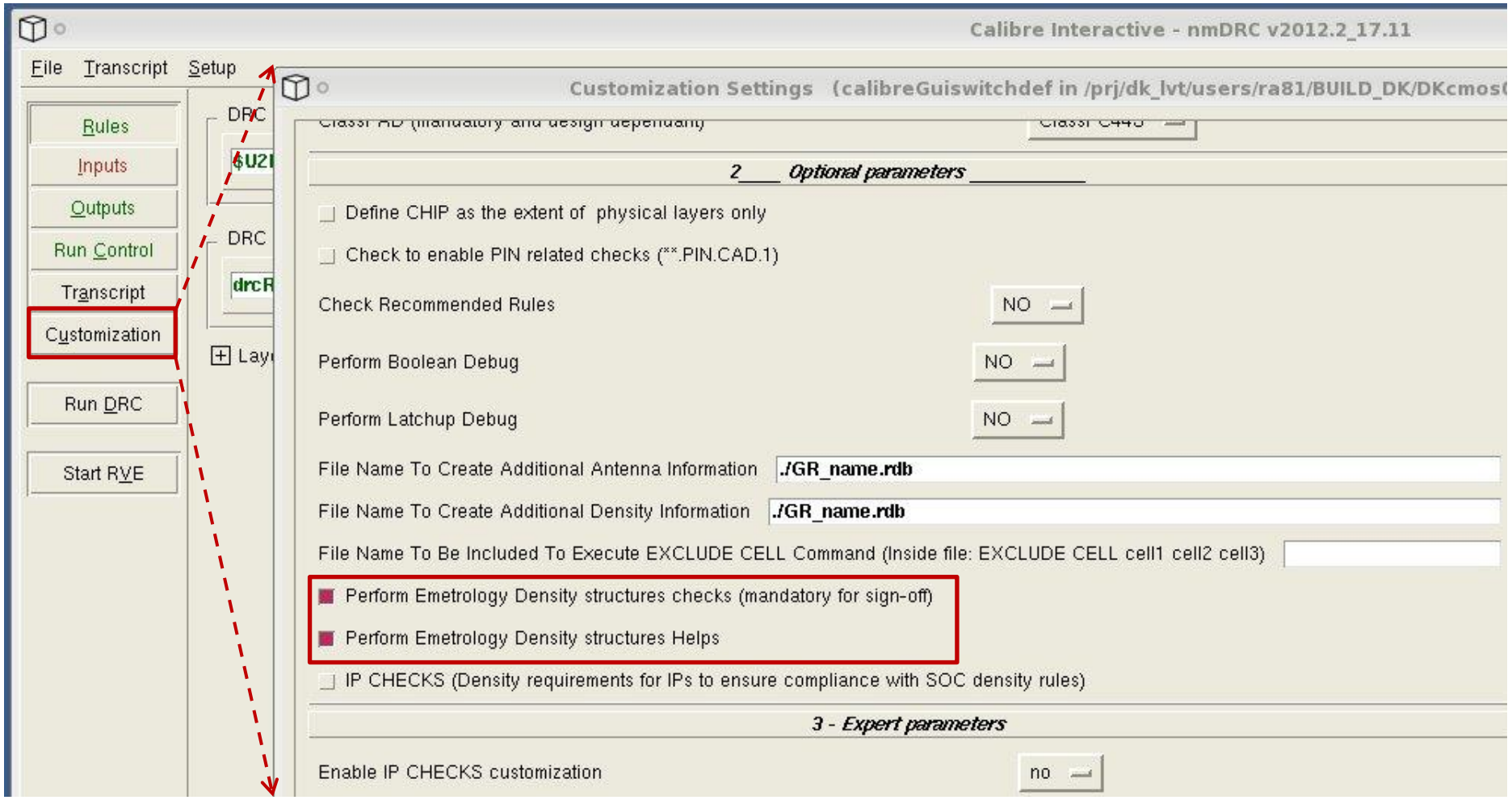
When to place Embedded Metrology ? (digital)

- For digital IPs, there is usually no room left enough for eMetro cell insertion at SoC Layout Finishing step
  - They must be considered during floor-planing
- In pure digital SoC flow, from recent 28nm DesignPlatforms, the eMetro insertion is automatically managed by the Floorplanner-tool before place&route step (refer to suitable Digital Implementation Kits)
- When SoC floorplanning is done, a DRC must be run to check whether emetro-insertion at PDK/Tiling-flow is required or not (to complement what has been already done at floorplanning level)

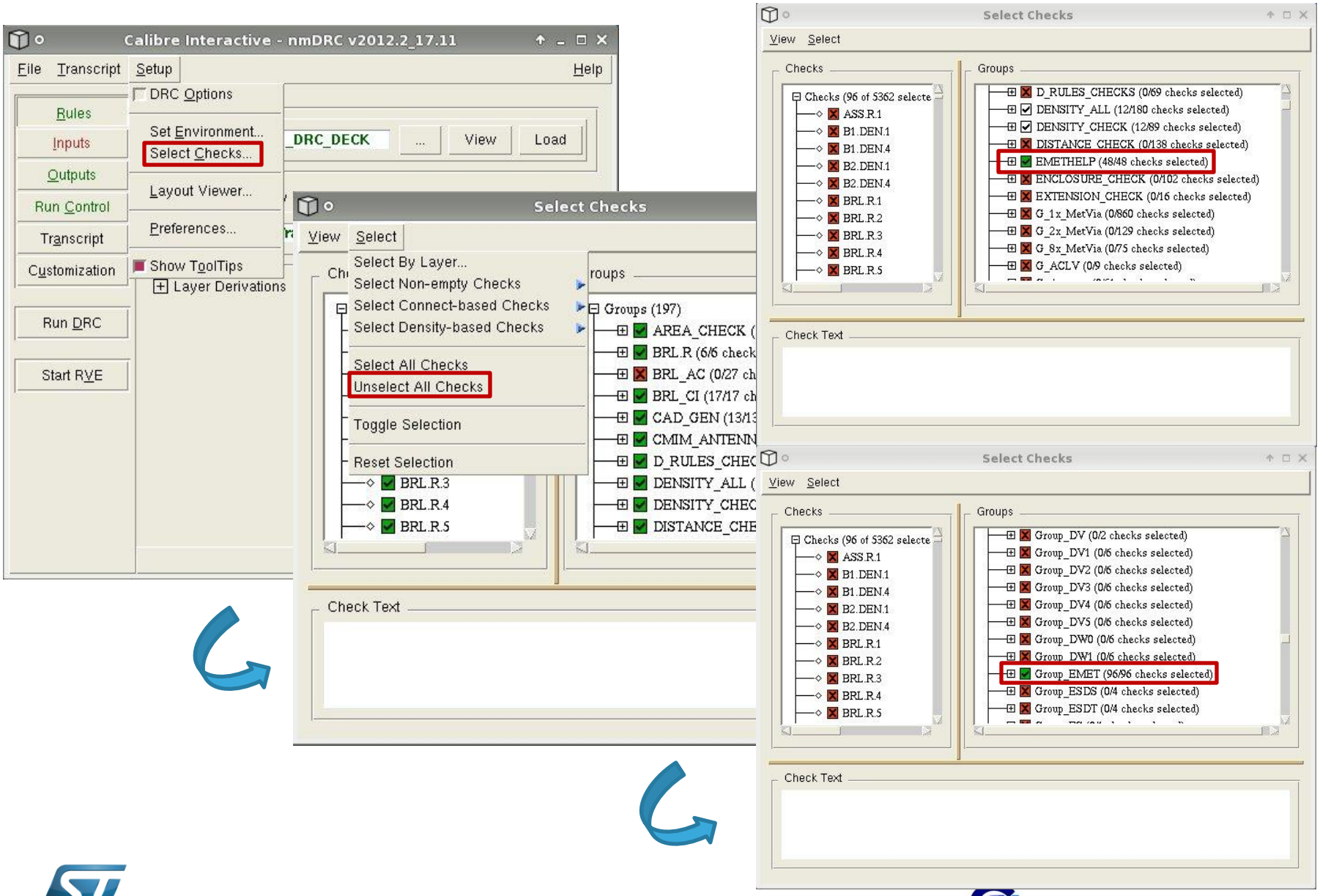
When to place Embedded Metrology ? (analog)

- For full custom physical design, these cells are inserted during layout finishing in empty spaces
- eMetro can then be managed by the tiler
- or they can be manually instantiated by picking them (FE or BE) from PDK/cmos28(32)_emetro library, for example.

GUI DRC Customization (1/2)



GUI DRC Check Selection (2/2)



eMetro flow (1/2)

The DK/tiling flow is built to ease later metal fix

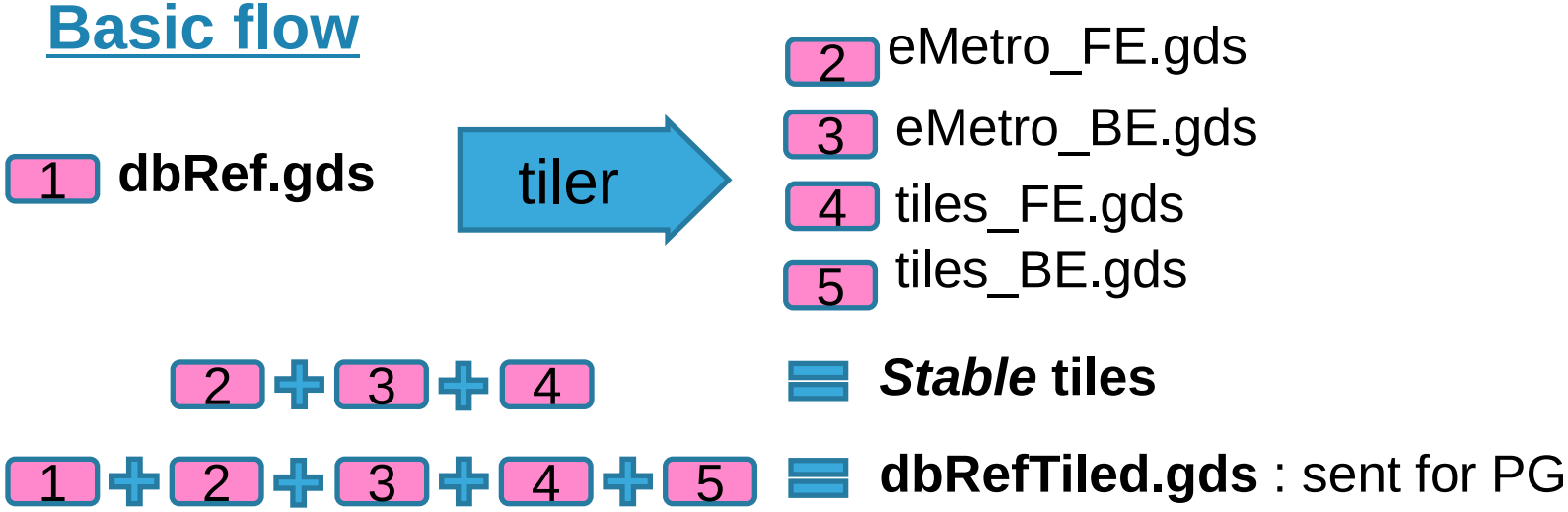
- When you tile your design before delivery, you archive the 4 generated gds:
  - ✓ design.eMetro_FE.gds
  - ✓ design.eMetro_BE.gds
  - ✓ design.tiles_FE.gds
  - ✓ **design.tiles_BE.gds**

- Depending on your working model, you may want to freeze:
  - ➢ FE layers only (eMetro and tiles)
    (non dense design allowing easy BE emetro tiling)
  - ➢ but most of the time: FE Layers plus BE eMetro
    (dense design not allowing easy BE emetro tiling)

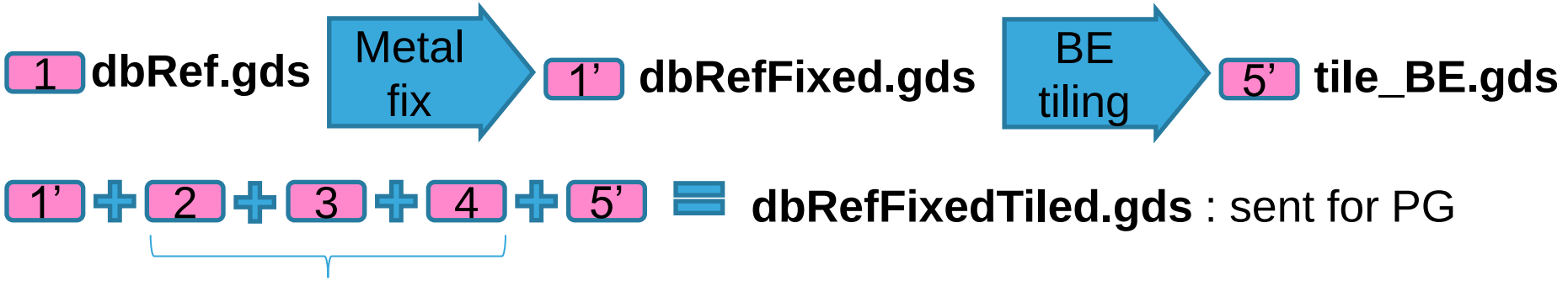
- Once your fix is done, the only gds to be re-generated by the tiler is usually **design.tiles_BE.gds**
- This will reduce tiling runtime, and ease final XOR between 1st and 2nd deliveries (no difference expected on FE layer for ex)

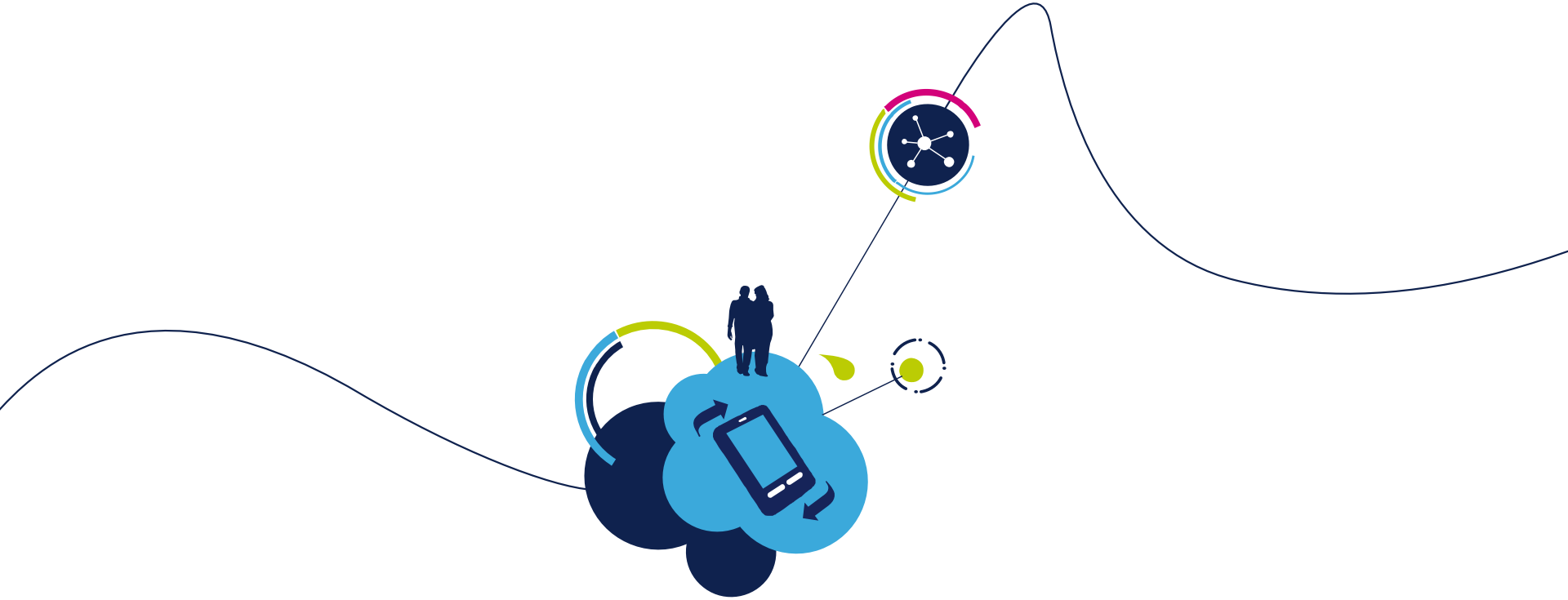
eMetro flow (2/2)

Basic flow



If need for a metal fix





Thank You